CELLULAR

NANO-S100

RPMA module

Data Sheet

Abstract

Technical data sheet describing the NANO-S100 cellular module.

The u-blox NANO-S100 module is an RPMA module in the LGA form factor and with the industry standard 4-wire Serial Peripheral Interface (SPI), allowing for easy integration with various host processors. Operating in the unlicensed 2.4 GHz ISM band, the RPMA network features a demonstrated up to 177 dB of link budget for superior connectivity. The module delivers unprecedented range, capacity, robustness and low power consumption, even in the most demanding of environments.

It is ideal for applications such as remote sensing that require up to 100 kB daily transmission. It features ultra-low power consumption for applications needing a 10-year or longer battery life.

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Contents

1 Functional description

1.1 Overview

The NANO-S100 is designed to easily integrate with any sensor, enabling robust wireless communication with any application processor. An AP (Access Point) typically can communicate with to up to 64,000 RPMA modules, covering an area of 50-200 sq-mi (130- 518 sq-km). Ingenu is aggressively deploying the Machine Network™, providing nationwide coverage in the USA. A NANO-S100 comes from the factory enabled to join any available network, worldwide.

1.2 Product features

Module	Region	Access Technology	Interfaces				Features								Grade		
		RPMA	UART	7-wire SPI	USB 2.0	GPIO	FOTA	Full hand-over	Global roaming	Ext. GNSS interface	AssistNow Software	CellLocate®	Integrated GNSS	Embedded programming	Standard	Professional	Automotive
NANO-S100	Global	2.4 GHz		•			•	•	•								

Table 1: NANO-S100 main features summary

1.3 Application block diagram

Figure 1 shows how a NANO-S100 interfaces with a Host application, running on an application processor.

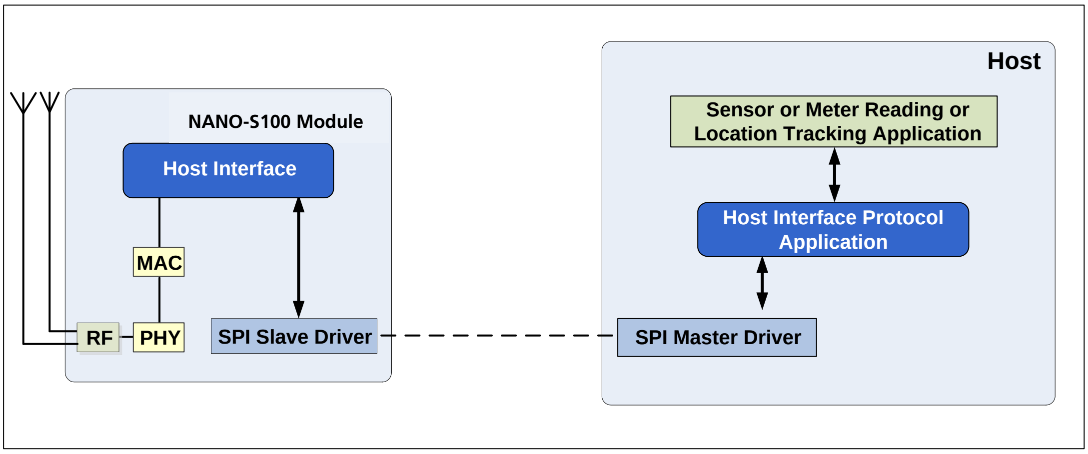


Figure 1: Typical application diagram

1.4 Product description

The NANO-S100 is a small form factor wireless network module that easily integrates with a microcontroller or application processor using a Serial Peripheral Interface (SPI). The top side of the printed circuit board (PCB) is enclosed with a radio frequency (RF) shield. The NANO-S100 is an LGA-style module designed to be soldered directly onto a host board via SMT processes.

NANO-S100 characteristics	
Single Band Mobile Station	
Single-band support: • 2.4 GHz ISM band	 2.4 GHz
Rx Sensitivity • 2.4 GHz ISM band	 -133 dBm
Tx Power conducted • 2.4 GHz ISM band	 +23.3 dBm

Table 2: NANO-S100 characteristics

2 Interfaces

2.1 Power management

2.1.1 VBATT

The pin supplies a low current of 2.2 V – 5.5 V for the module's internal supervisory circuitry. This pin should be decoupled with a 0.1 µF capacitor on the host processor board.

2.1.2 3V3

This pin drives the CPU, transceiver, RF PA section of the module. It can consume up to 800 mW. Allow for bypassing with a 47 µF low ESR cap (bulk) and a 0.1 µF ceramic cap for optimal performance. Depending on the host design, there are some nuances that are important regarding this signal:

- The **3V3** pin can be supplied continuously or only when the **WAKE** signal is asserted "high", as for battery powered applications.
- The module runs through various operating states when the **3V3** pin is supplied.
  - If the module internally is in a state that requires no RF, the supply to the **3V3** pin can be "noisy" (it can have +/-100 mV ripple). The RF state is defined by the **RF_SHDN** pin. This allows the host's 3.3 V regulator to work in low quiescent (power save) modes.
  - If the module internally is active and does require RF, the supply to the **3V3** pin must be "clean" (it can have +/-20 mV ripple). This forces the host's 3.3 V supply into a high precision mode and forces a high quiescent current of that regulator.

☞ If the module is operated in a battery mode, when the **3V3** pin is not always enabled, the **3V3** supply must power up and be stable within 2 ms of the **WAKE** signal going "high"

This switching of "noisy" and "clean" becomes clear (and important) when working with battery operated devices and optimal low power drain.

2.1.3 ON_OFF

This input signal controls the power-on of the LDO circuitry for the NANO-S100 module. This signal is controlled by the Host Common Library, compiled onto the user's apps processor. See u-blox Host Common Software Integration Application Note [2] for more details. For reference only: it must be shut off prior to starting the NANO-S100 power-up sequence as defined in the u-blox NANO-S100 System Integration Manual [1]. After the NANO-S100 powers up, this signal is to remain logic high during normal operational modes. This pin dually serves a power on/off function as well as a module reset function.

2.2 Serial interface

2.2.1 MRQ

The **MRQ** (Master Request) is the host's normal way of waking the NANO-S100 to initiate SPI communications. Logic "high" forces the NANO-S100 awake. This signal is controlled by the Host Common Library, compiled onto the user's application processor.

2.2.2 SRDY

SRDY (Slave Ready) is an indication from the NANO-S100 that it has fully booted its internal firmware image, initialized its hardware and interfaces, and is ready for communication (arbitration) with the host. Logic "high" indicates the NANO-S100 is ready for communications. This signal is controlled/handled by the Host Common Library, compiled onto the user's application processor. See the u-blox NANO-S100 Host Common Software Integration Application Note [2] for more details.

2.2.3 SRQ

The **SRQ** (Slave Request) signal is an indication from the NANO-S100 that it wants the host’s attention. When **SRQ** is asserted “high,” the host must read the status registers of NANO-S100. If **SRQ** is “high,” **SRDY** will also be “high.” This signal is controlled/handled by the Host Common Library, compiled onto the user’s application processor. See the u-blox NANO-S100 Host Common Software Integration Application Note [2] for more details.

For battery powered applications, **SRQ** must be connected to a pin that can wake the application processor from sleep.

2.2.4 SPI system

The SPI system is the generic term used for all SPI signals (**MOSI**, **MISO**, **CS**, **SCLK**) to be set up for SPI communications to occur between host and NANO-S100. The NANO-S100 SPI is the slave in the master/slave communications. For further details, see the u-blox NANO-S100 System Integration Manual [1].

⚠ **Other SPI slaves are not allowed to share the SPI signals.**

⚠ **CS must be controlled by the Host Common Library API to guarantee correct sequencing. Specifically, the user must ensure that the SPI CS is active (low) for the whole duration of a message transfer, with no gaps. This is implemented in HOST_CMN_HAL_ExchangeMsg in host_cmn_hal_k20.c, in the rACM example code (instructions provided on how to get the starter package with example code when you receive your rACM kit), and must be duplicated for your particular apps processor.**

2.2.5 TOUT

This signal is a time synchronizing signal that pulses high upon specific network timing events.

2.2.6 RF_TXENA

This signal indicates when the device is transmitting. When transmitting, it is recommended that the host processor use this opportunity as a trigger to read the system “**VBATT**” power line to show battery voltage under maximum load.

2.2.7 RF_SHDN

This module signal indicates status of the RF Transceiver of the NANO-S100. If low, the transceiver sleeps (no RX and no TX). This output of the module (3.3 V) indicates when the RF transceiver is on or off. When RF_SHDN is high, the RF is “ON” (RX or TX). In the RF “ON” mode, the module needs a “clean” 3.3 V (low ripple) to **3V3** pin

2.2.8 WAKE

☞ If **WAKE** is used to enable the Host's **3V3** supply for battery powered mode, then the **3V3** supply must be on and stable within 2 ms of **WAKE** going high.

The **WAKE** signal is generated by the module and is 1.8 V. It signals that it now requires a 3.3 V source to **3V3** pin. Generally, for a powered module, the **WAKE** is not required since 3.3 V already exists. In the case of battery powered modules, the WAKE turns on the host's main supply to regulate the battery to the required 3.3 V. See the u-blox NANO-S100 System Integration Manual [1] for a powered (non-battery) example circuit and a lithium battery example schematic.

2.3 RF antenna interface

2.3.1 ANT1 and ANT2

These pins are the RF ports (RX and TX) of the module. They are DC-coupled, 50 Ω and require special host routing of PCB. **ANT1** is the primary antenna and is always required. **ANT2** is a secondary antenna that the module can use for Antenna Diversity. A single or dual antenna (diversity) system can be configured during the provisioning process. For best results ensure the load termination (antenna) has a VSWR of 1.5:1 or better (return loss less than -10 dB).

3 Pin definition

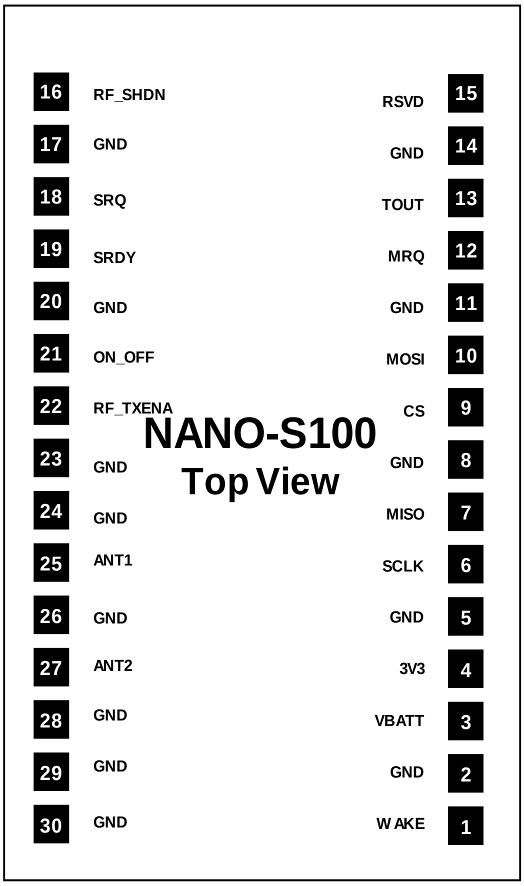


Figure 2: NANO-S100 pin assignment

No	Name	Power domain	I/O	Description	Remarks
1	WAKE	-	O	1.8V	This is a 1.8 V output signal that reflects the status of the module's power state. When WAKE is "high" the module is active in idle, RX, or TX states. When WAKE is "low", the module's 3.3 V is internally gated OFF and the module is in its lowest power state. This signal is to be used for "battery operating modes". Connect the WAKE pin directly to the enable pin of a voltage regulator or FET switch controlling 3.3 V
2	GND	-	N/A	Ground	All GND pads must be connected to ground.
3	VBATT	-	I	Input supply	Input power to the module. This power domain is low current but is used 100% of the time to supply internal supervisory domains.
4	3V3	-	I	Input supply	Module supply input. The 3V3 pin can be continuously supplied (line powered) or only when the WAKE pin is asserted "high" (battery powered). This power domain is high power (internal CPU, Transceiver, and RF PA) and should be decoupled with a low ESR, high capacitance capacitor.
5	GND	-	N/A	Ground	All GND pads must be connected to ground.
6	SCLK	GDI	I	SPI	SPI Clock
7	MISO	GDI	O	SPI	SPI Master Input Slave Output
8	GND	-	N/A	Ground	All GND pads must be connected to ground.
9	CS	GDI	I	SPI	SPI Chip Select (Note other slaves are prohibited on the SPI interface, but this pin must be controlled by the Host Common Library). It CANNOT be tied low on the PCB.
10	MOSI	GDI	I	SPI	SPI Master Output Slave Input
11	GND	-	N/A	Ground	All GND pads must be connected to ground.
12	MRQ	GDI	I	SPI Control Signal	SPI Master Request
13	TOUT	GDI	O	Network indication	TOUT is a normally low signal that pulses high in response to specific Network Timing Events. It allows an application to trigger a measurement with sub-1 ms accuracy.
14	GND	-	N/A	Ground	All GND pads must be connected to ground.
15	RSVD	RSVD	N/A	RSVD	RESERVED pin. Do not connect.
16	RF_SHDN	GDI	O	RF Transceiver status	This pin indicates the status of the RF Transceiver for the NANO-S100: • Low = Shutdown • High = Active • It can be used for WIFI/BT coexistence, and to reduce power supply current during low power states (see section 2.1.2)
17	GND	-	N/A	Ground	All GND pads must be connected to ground.
18	SRQ	GDI	O	SPI Control Signal	SPI Slave Request. SRQ must be connected to a pin that can wake the application processor from sleep, for battery powered applications.
19	SRDY	GDI	O	SPI Control Signal	SPI Slave Ready
20	GND	-	N/A	Ground	All GND pads must be connected to ground.
21	ON_OFF	GDI	I	ON/OFF control line	This is used to turn ON/OFF the internal power supplies of the NANO-S100. It is controlled by the Host Common Library. • Low: module consumes less than 1 µA • High: Module is active and will run through a wide range of power states.

No	Name	Power domain	I/O	Description	Remarks
22	RF_TXENA		O	PA status	This signal is used to indicate status of the power amplifier for the NANO-S100: • Low = OFF • High = Enabled (Transmitting) The rise edge can be used to trigger a Host CPU's ADC read of VBATT (battery voltage while under maximum load).
23	GND	-	N/A	Ground	All GND pads must be connected to ground.
24	GND	-	N/A	Ground	All GND pads must be connected to ground.
25	ANT1	ANT	I/O	Primary RF path	RF ports. They are 50 Ω port, DC coupled. RF1 is required but both ANT1 and ANT2 are desired for antenna diversity. Single port or dual antenna port can be configured in the provisioning process.
26	GND	-	N/A	Ground	All GND pads must be connected to ground.
27	ANT2	ANT	I/O	Diversity RF path	RF ports. They are 50 Ω port, DC coupled. ANT1 is required but both ANT1 and ANT2 are desired for antenna diversity. Single port or dual antenna port can be configured in the provisioning process.
28	GND	-	N/A	Ground	All GND pads must be connected to ground.
29	GND	-	N/A	Ground	All GND pads must be connected to ground.
30	GND	-	N/A	Ground	All GND pads must be connected to ground.

Table 3: NANO-S100 pinout

☞ Pins designated "RESERVED" should be left open and not connected.

☞ The VDD of the internal logic of the NANO-S100 is 3.3 V.

☞ The Host is the SPI Master and the NANO-S100 is the SPI Slave.

☞ CMOS_I: The module input voltages are 3.3V CMOS levels. VIH = 2.0V (min) and VIL = 0.8V (max).

☞ CMOS_O: The module output voltages are 3.3V CMOS levels (4mA). VOH = 2.4V (min) and VOL = 0.4V (max).

☞ SPI inputs to the module (**SCLK**, **MOSI**, **CS**) must be tri-stated or driven low when the module may be sleeping (**MRQ** and **SRQ** are both low). See u-blox NANO-S100 System Integration Manual [1] for more details.

4 Electrical specifications

Stressing the device above one or more of the ratings listed in the Absolute Maximum Rating section may cause permanent damage. These are stress ratings only. Operating the module at these or at any conditions other than those specified in the Operating Conditions sections (section 4.2) of the specification should be avoided. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Operating condition ranges define those limits within which the functionality of the device is guaranteed.

Where application information is given, it is advisory only and does not form part of the specification.

4.1 Absolute maximum rating

Symbol	Description	Condition	Min.	Max.	Unit
VBATT	Module supply voltage	Input DC voltage at VBATT pin	2.2	6.0	V
3.3V	Module supply current	Input DC voltage at 3.3V pin	3.1	3.5	V
GDI	Digital Interafce Signals	Input DC at digital I/O pin	3.1	3.5	V
Tstg	Storage Temperature		–40	85	°C
Topr	Operating Temperature		–40	85	°C

Table 4: Absolute maximum ratings

The product is not protected against overvoltage or reversed voltages. If necessary, voltage spikes exceeding the power supply voltage specification, given in table above, must be limited to values within the specified boundaries by using appropriate protection devices.

4.2 Operating conditions

Unless otherwise indicated, all operating condition specifications are at an ambient temperature of 25 °C.

Operation beyond the operating conditions is not recommended and extended exposure beyond them may affect device reliability.

4.2.1 Operating temperature range

Operating outside of these ranges may damage the unit. The NANO-S100 is MSL 3-rated and should be handled as an MSL 3 device per IPC/JEDEC J-STD-033.

Parameter	Min.	Typ.	Max.	Unit	Remarks
Normal operating temperature	–40		+85	°C	
Storage temperature	–40		+85	°C	
Humidity	5		95	%	Non-condensing humidity
Ramp Temperature			30	°C/Hr.	Maximum rate at which operating temperature should change
MTBF			6.4	MHrs	

Table 5: Environmental conditions

4.2.2 Supply/Power pins

Symbol	Parameter	Min.	Typ.	Max.	Unit
3V3	Module supply input voltage	3.2	3.3	3.4	V
VBATT	Module low power mode supply input voltage	2.2		5.5	V
ICC	Module supply peak current consumption*			300	mA

* Measured at +23.3 dBm TX output (Typ=50 Ω), 3.3 V, range includes VSWR ≤ 1.5:1 (PO not compensated).

Table 6: Input characteristics of Supply/Power pins

Symbol	Parameter	Min.	Typ.	Max.	Unit
VOL	VOL – Voltage Output, Low (4mA sink)	0		0.4	V
VOH	VOH – Voltage Output High (4mA source)	2.4		3.3	V
SPI	SPI Clock[1]	0.1		8.6	MHz

Table 7: Digital pin characteristics

☞ The SPI clock has a maximum rate of 26 MHz/3 and a minimum of 100 kHz. There is no physical limitation on the minimum clock rate but the 100 kHz is deemed "marginal" and is not absolute. Depending on the data traffic model and level of debug traffic, 100 kHz may cause a backup of SPI traffic, which then causes buffer overflow conditions. The application must be validated to ensure that the SPI clock is sufficient to support required traffic.

4.2.3 Power consumption

Table 8 reports NANO-S100 module power consumptions.

Mode	Min.	Typ.	Max.	Units	Remarks
Power Off[2]	0.05	0.1	2.0	µA	
Deep Sleep 2	10	15	30	µA	
Idle Mode 2	10	15	22	mA	
Active Mode - RX enabled 2	75	85	90	mA	
Active Mode - TX at max output	200	245	300	mA	Measured at +23.3 dBm TX output (Typ=50 Ω), 3.3 V, range includes VSWR ≤ 1.5:1 (PO not compensated).

Table 8: NANO-S100 Power consumption

☞ Tested at 3.3V input:

- There are power differences between the Voltage/Current numbers in this table and the data provided in Figure 3, Figure 4, and Figure 5. These figures show representative characterization of power over voltage/temperature characterization and are representative behavior.
- Table 8 refers to a maximal current draw that the host system should be designed to accommodate.

[1] The SPI clock has a maximum rate of 26 MHz/3 and a minimum of 100 kHz. There is no physical limitation on the minimum clock rate but the 100 kHz is deemed "marginal" and is not absolute. Depending on the data traffic model and level of debug traffic, 100 kHz may cause a backup of SPI traffic, which then causes buffer overflow conditions. The application must be validated to ensure that the SPI clock is sufficient to support required traffic.

[2] Tested at 3.3V input:

- There are power differences between the Voltage/Current numbers in this table and the data provided in Figure 3, Figure 4, and Figure 5. The figures show representative characterization of power over voltage/temperature characterization and are representative behavior
  - Table 8 refers to a maximal current draw that the host system should be designed to accommodate

4.2.4 RF performance

Parameter		Min.	Max.	Unit	Remarks
Frequency range SIM 2.4GHz	Uplink	2402	2482	MHz	Module transmit
	Downlink	2402	2482	MHz	Module receive

Table 9: Operating RF frequency bands

Parameter	Min.	Typ.	Max.	Unit	Remarks
Receiver input sensitivity	–130	–133	-135	dBm	Sensitivity at maximum DL spreading factor of 11 (2048) with 10% FER.
Receiver Image Reject	38	45	50	dBm	
Noise Figure	3.5	4.8	5.5	dBm	
Input IP3 (high LNA gain mode)		-11		dBm	
Maximum RF input level for specification compliance			-20	dBm	
Condition: 50 Ω source					

Table 10: Receiver sensitivity performance

Parameter	Min.	Typ.	Max.	Unit	Remarks
Frequency Range	2402	-	2482	MHz	The upper frequency range is market dependent: • FCC/ISED: CH38; 2475.63 MHz • ETSI: CH40; 2475.63 Hz • Japan: CH41; 2481.60 MHz
Channel Spacing	-	1.99	-	Mhz	
Condition: 50 Ω source					

Table 11: General RF characteristics

Parameter		Min.	Typ.	Max.	Unit	Remarks
Maximum output power (FCC/IC markets) [3]		-	23.3	-	dBm	
Maximum output power (ETSI markets)		8.5	9.5	10.0	dBm	
Carrier Rejection		-35	-40	-50	dBc	
Signal Modulation			DSSS-DBPSK			
Signal Bandwidth			1.0		MHz	
BT Factor			0.3			
Peak-to-Average Ratio			2.3		dB	
Spectral bandwidth at maximum RF power:	-6 dB BW		0.96		MHz	
	-20 dB Bw		1.75		MHz	
ACPR				-30	dBc	Spec and test method comes from FCC 15.247(d); Band Edge Emissions, 2 MHz offset.
Harmonics				-43	dBm	At any TX power level, VSWR ≤ 3:1. Harmonics fall into FCC restricted
Transmit Power Level Accuracy				+/-1.5	dB	Estimated sum of all contributors with VSWR ≤ 1.5:1. Normal link mode.
					dBm	At any TX power level, VSWR ≤ 3:1. Applies to spurious, not ACPR or harmonics. Generally the largest spurious output outside the 2.40-2.48GHz band is at 2/3LO and 4/3LO.
						Maximum VSWR for spec compliance applies at 25°C only. Slightly degraded ACPR/mask and power variation can be expected at temperature extremes.

Condition: 50 Ω output load

Table 12: Transmitter

4.3 Effects of temperature and voltage

The NANO-S100 is based largely on Complementary Metal–Oxide–Semiconductor (CMOS) technology. The current drain of CMOS circuitry can vary substantially over temperature. The RF circuitry and its performance also vary substantially over temperature. The NANO-S100 utilizes two main power domains, which are linked to the pins **VBATT** and **3V3**.

4.3.1 Power domains

4.3.1.1 VBATT (2.2-5.5V)

This pin powers the low current supervisory/housekeeping circuitry of the module, used while the module is asleep. This voltage supply must be continuous, not under software control. The module autonomously wakes up and synchronizes to the network periodically, without any knowledge by the host apps processor. Figure 3 shows the effect of **VBATT** on deep sleep power consumption at a nominal VBATT of 3.3 V.

[3] Maximum TX RF power is limited by FCC/IC grant to 23.3 dBm in these markets. Transmit power is configured during network join time to meet country-specific deployment and regulatory requirements. The configurable range is 0 – 23.3 dBm in 1 dB integer increments. For non-integer Power such as 23.3dBm, the module's MAX_TX Power must be set to 24dBm to force a maximum calibrated value

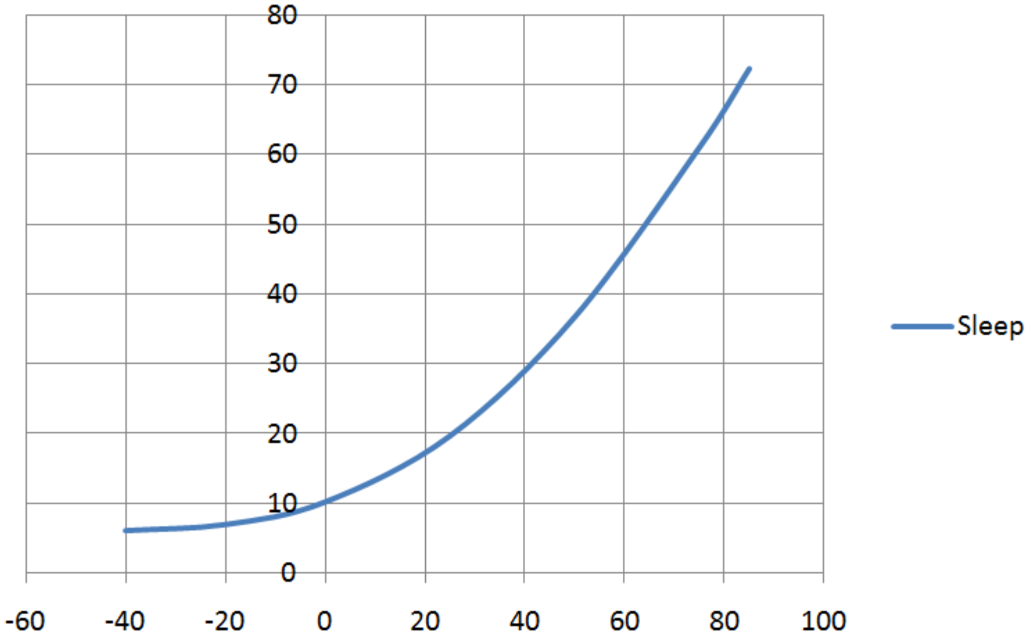


Figure 3: Sleep current (µA) vs Temperature (°C) at 3.3V Input

4.3.1.2 3V3 Supply

This domain needs a 3.3 V input to **3V3** when **WAKE** is asserted "high." This power domain is used for the majority of processing, transceiver, and RF Power Amplifier circuitry within the module. These blocks require a lot of power compared to the **VBATT** domain, and the module asserts **WAKE** only when this power (voltage) is required.

The following graphs show the relative differences across the operating voltages and their effect on current consumption.

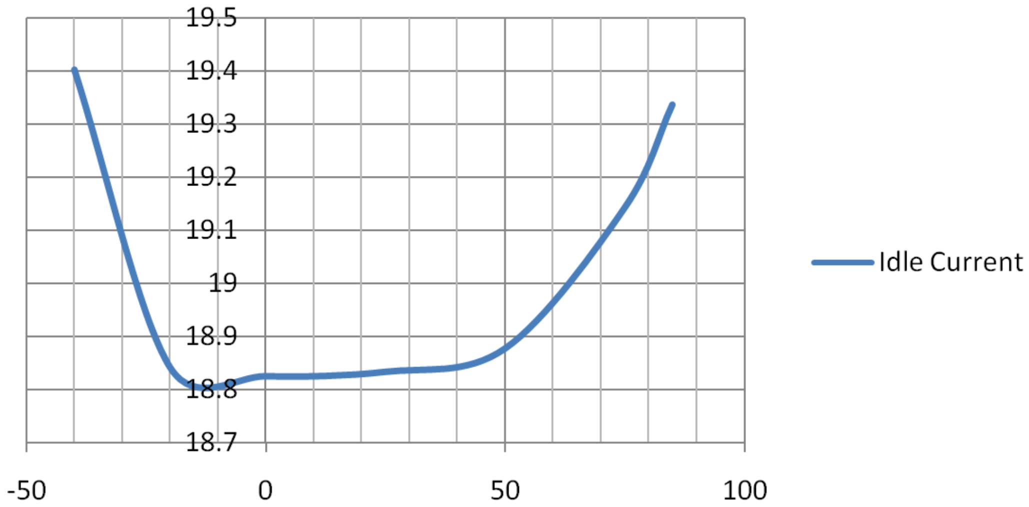


Figure 4: Idle current (mA) vs temperature (°C) at 3.3 V input to 3V3 pin

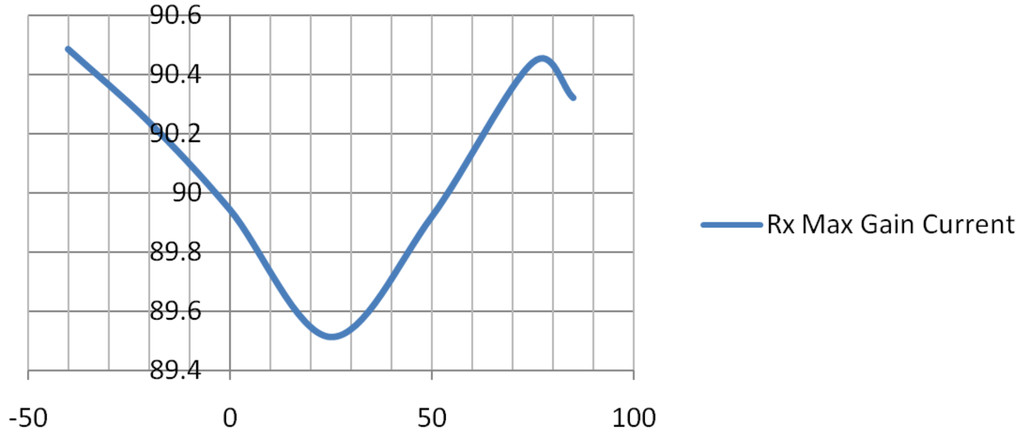


Figure 5: Max Rx gain current (mA) vs temperature (°C) at 3.3 V input to 3V3 pin

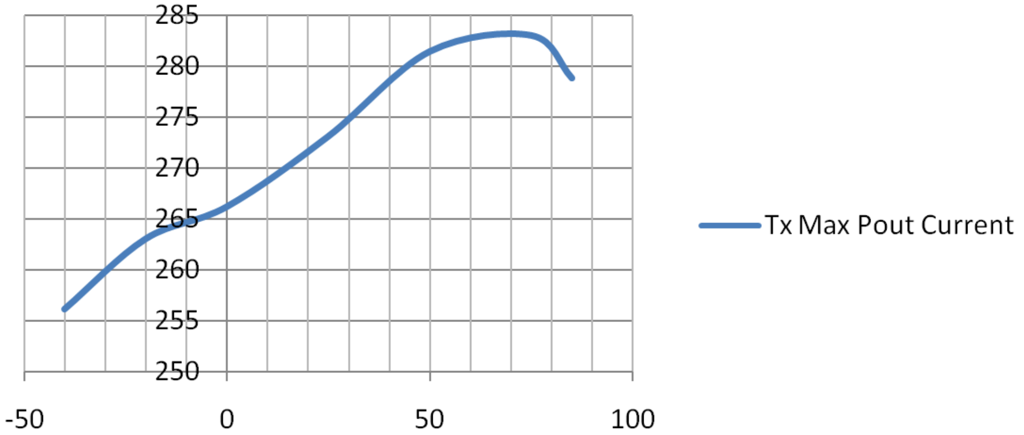
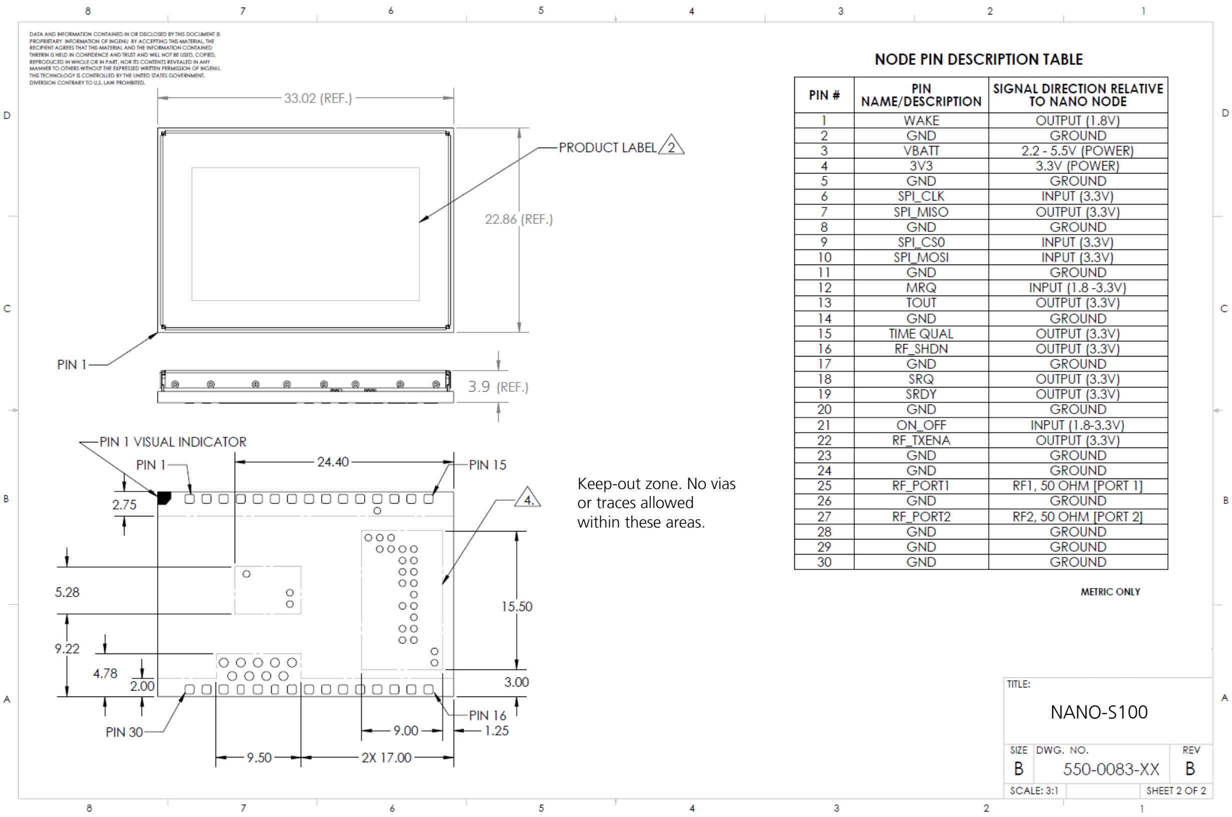


Figure 6: Max Tx (23.3 dBm) current (mA) vs temperature (°C) at 3.3 V input to 3V3 pin

5 Mechanical specifications



NODE PIN DESCRIPTION TABLE

PIN #	PIN NAME/DESCRIPTION	SIGNAL DIRECTION RELATIVE TO NANO NODE
1	WAKE	OUTPUT (1.8V)
2	GND	GROUND
3	VBATT	2.2 - 5.5V (POWER)
4	3V3	3.3V (POWER)
5	GND	GROUND
6	SPI_CLK	INPUT (3.3V)
7	SPI_MISO	OUTPUT (3.3V)
8	GND	GROUND
9	SPI_CS0	INPUT (3.3V)
10	SPI_MOSI	INPUT (3.3V)
11	GND	GROUND
12	MRQ	INPUT (1.8 -3.3V)
13	TOUT	OUTPUT (3.3V)
14	GND	GROUND
15	TIME QUAL	OUTPUT (3.3V)
16	RF_SHDN	OUTPUT (3.3V)
17	GND	GROUND
18	SRQ	OUTPUT (3.3V)
19	SRDY	OUTPUT (3.3V)
20	GND	GROUND
21	ON_OFF	INPUT (1.8-3.3V)
22	RF_TXENA	OUTPUT (3.3V)
23	GND	GROUND
24	GND	GROUND
25	RF_PORT1	RF1, 50 OHM [PORT 1]
26	GND	GROUND
27	RF_PORT2	RF2, 50 OHM [PORT 2]
28	GND	GROUND
29	GND	GROUND
30	GND	GROUND

Figure 7: Dimensions (NANO-S100 bottom, top and sides views). Pin 15 (TIME_QUAL) is a RSVD pin.

The mechanical drawing provides the dimensions of the NANO-S100 only and does not reflect the current labeling of the product. See the PCB Land Pattern and Keep-outs for exacting footprint and Keep-out dimensions in the NANO-S100 System Integration Manual [1].

6 Approvals

6.1 Approvals

Products marked with this lead-free symbol on the product label comply with the "Directive 2002/95/EC of the European Parliament and the Council on the Restriction of Use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).

NANO-S100 modules are RoHS compliant.

No natural rubbers, hygroscopic materials, or materials containing asbestos are employed.

NANO-S100 series modules are approved under the schemes reported in Table 13.

Country	Scope	ID
US	FCC	XPY2DXMNNN1N
Canada	Industry Canada (IC)	8595A-2DXMNNN1N
Europe	RED (Radio Equipment Directive)	No ID applicable to RED; just CE marking

Table 13: NANO-S100 certification approvals

For more details on latest country certification and network operators, see our website www.u-blox.com.

7 Product handling & soldering

7.1 Packaging

The NANO-S100 modules are packed in anti-static polystyrene alloy trays that hold up to 24 modules. Trays of modules are stacked up to 10 trays high. Dry packs are used to protect the module, and to notify the user of the moisture conditions within the package.

- Each dry pack will hold up to 240 modules
- Each shipping box will hold up to two dry packs for a total of 480 modules
- A shipping box of 480 modules weighs 6.1 kg, (13.6 lbs)
- Shipping box dimensions 558 x 478 x 186 mm (21.9 x 18.8 x 7.3 in)

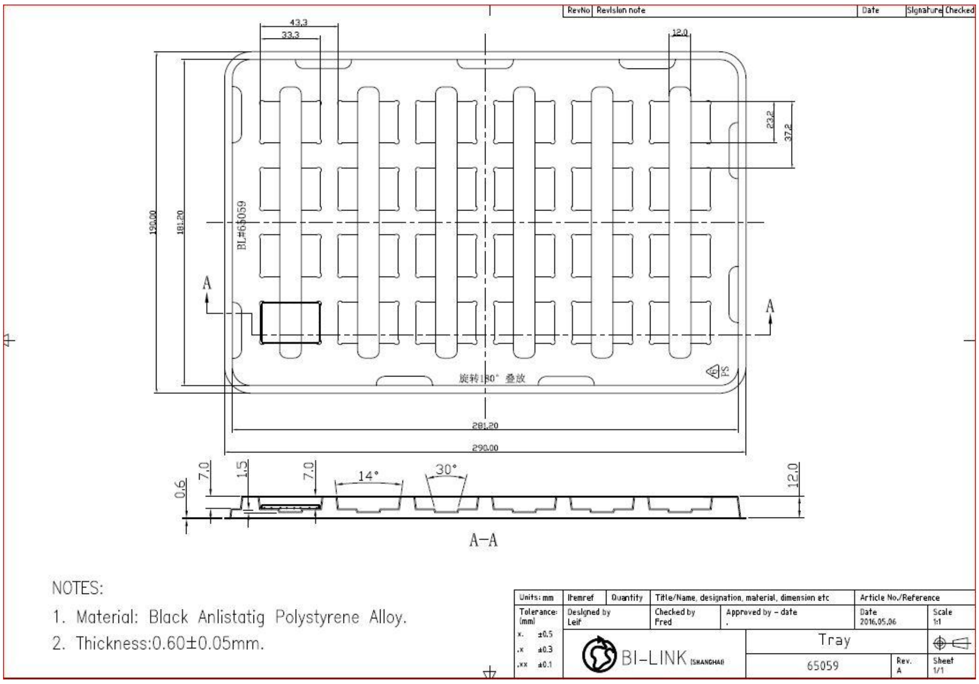


Figure 8: Anti-static polystyrene alloy tray

Modules are placed into the trays in the same direction. Figure 9 shows the direction of the modules in the tray.

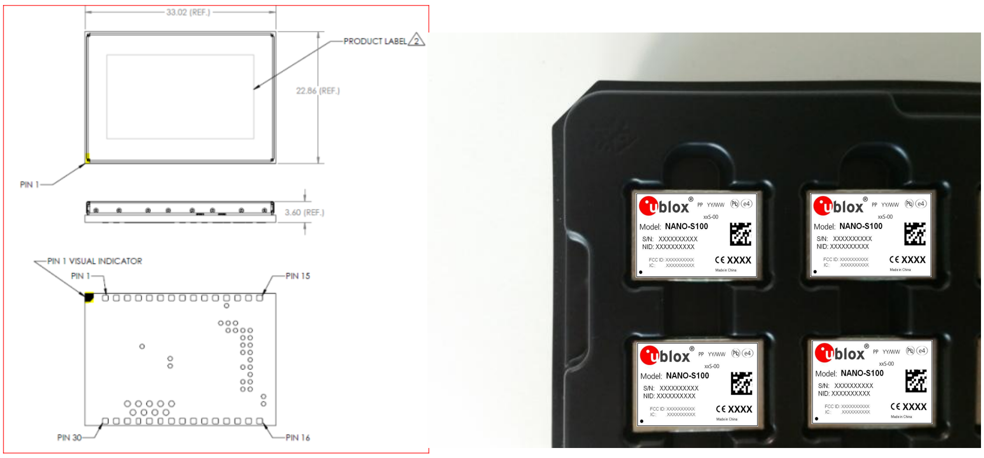


Figure 9: NANO-S100 in trays

Figure 10: Each dry pack contains a humidity indicator card and desiccant

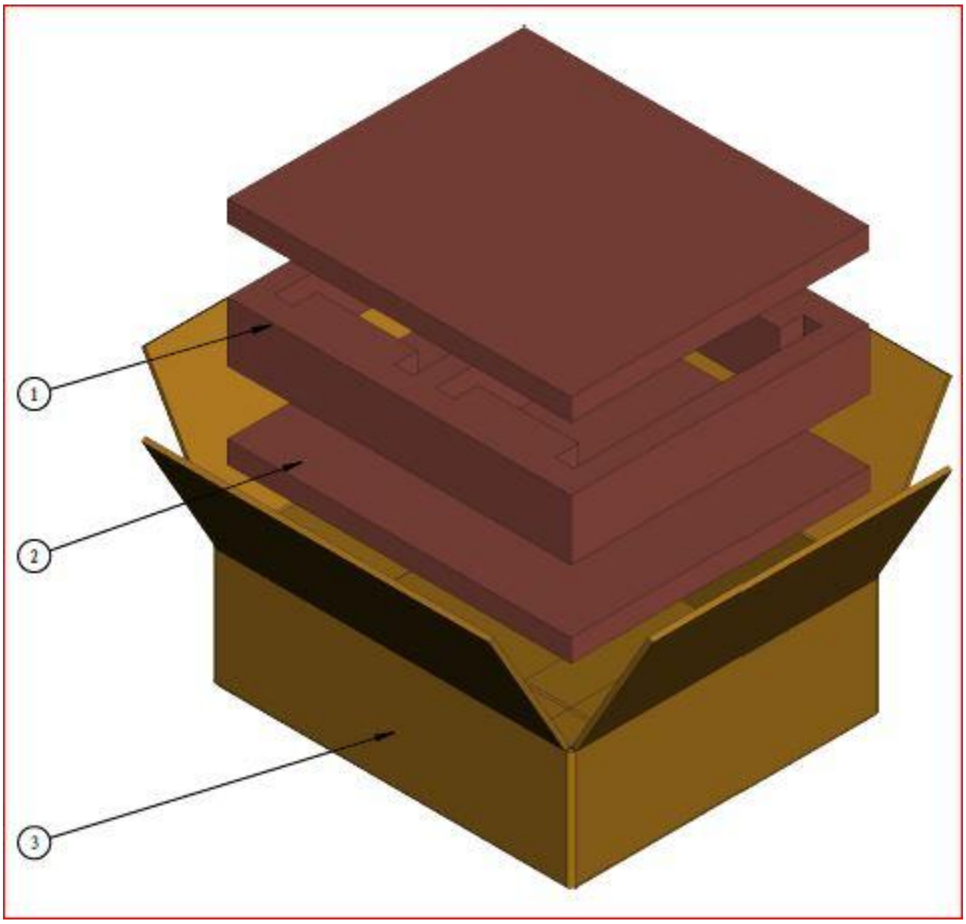


Figure 11: Shipping carton box

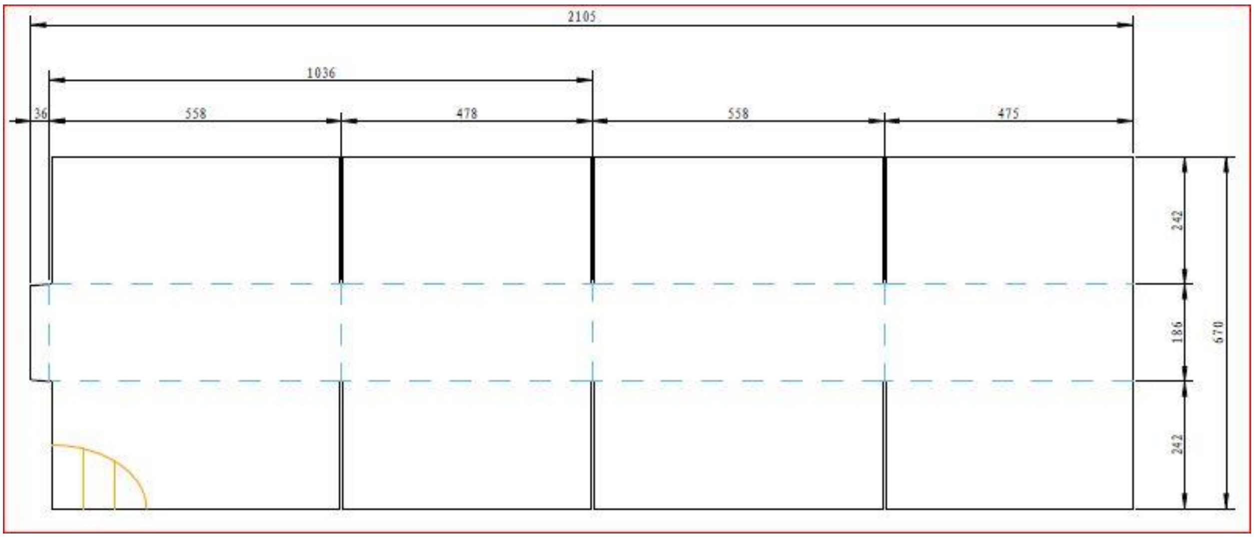


Figure 12: Shipping carton box dimensions (side view)

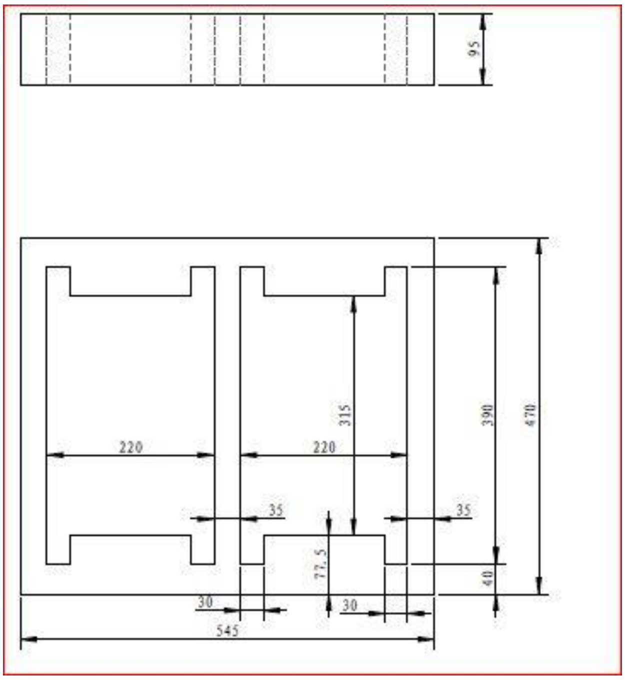


Figure 13: Shipping carton box dimensions (end view)

Figure 14: Sealed trays in shipping carton box

7.2 Moisture Sensitivity Levels

⚠ **NANO-S100 modules are Moisture Sensitive Devices (MSD) in accordance to the IPC/JEDEC specification.**

The Moisture Sensitivity Level (MSL) relates to the packaging and handling precautions required. NANO-S100 modules are rated at MSL level 3. For more information regarding moisture sensitivity levels see the u-blox Package Information Guide [3].

Modules are presented in trays which are dry packed in moisture barrier bags (MBB).

The Dry pack per IPC/JEDEC J-STD-033 for MSL3 conditions are: MBB, HIC, Desiccant, MSID label, Caution Label.

☞ For MSL standard see IPC/JEDEC J-STD-033 (can be downloaded from www.jedec.org).

7.3 Reflow soldering

The recommended reflow profile is SMT Reflow Profile IPC-7530.

⚠ **Failure to observe these recommendations can result in severe damage to the device!**

7.4 ESD precautions

The NANO-S100 is designed to be a truly embedded module and can almost be considered an IC. The NANO-S100 is to be placed as a direct-connect to the Host CPU. Therefore, the NANO-S100 has inherent minimal electrostatic discharge (ESD) protection on its I/O.

NANO-S100 modules are Electrostatic Sensitive Devices (ESD) and require special ESD precautions typically applied to ESD sensitive components.

Proper ESD handling and packaging procedures must be applied throughout the processing, handling and operation of any application that incorporates NANO-S100 module.

ESD model	Class	Min. voltage
HBM	Class 1C	> 1000 V
MM	Class A	> 1000 V

Table 14: ESD rating

⚠ **Failure to observe these precautions can result in severe damage to the device!**

RF pins have inherent ESD robustness due to the RF antenna cross switch and survive the 1 kV HBM test. With a shunt 27 nH inductor at the RF pin, the pin can survive direct 8 kV ESD strikes.

If the application is intended for harsh ESD or lightning strike scenarios it is recommended that the integrator take extra precautions to guard against accidental resets or ESD damage.

7.5 Harsh environments

The NANO-S100 employs miniature surface-mounted components in its assembly. If the target design is intended for high humidity or salt environments and intended to have a long service life, it is recommended that the designer take necessary precautions to guard against prolonged exposure to moisture and other contaminants. A sealed enclosure (IP67 or IP68) or potting may be required in extreme environments.

8 Labeling and ordering information

8.1 Product labeling

The label on u-blox modules includes important product information.

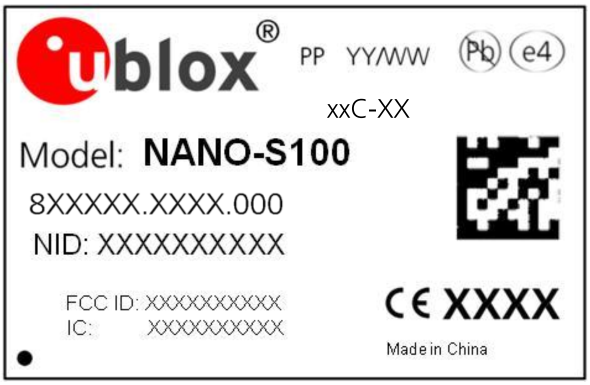


Figure 15: NANO-S100 module label

8.2 Explanation of codes

Three different product code formats are used. The **Product Name** is used in documentation such as this data sheet and identifies all u-blox products, independent of packaging and quality grade. The **Ordering Code** includes options and quality, while the **Type Number** includes the hardware and firmware versions. Table 15 shows the structure of these three different formats.

Format	Structure
Product Name	NANO-TGVV
Ordering Code	NANO-TGVV-MMQ
Type Number	NANO-TGVV-MMQ-XX

Table 15: Product code formats

Table 16 explains the parts of the product code:

Code	Meaning	Example
NANO	Form factor	NANO
TG	Platform (Technology and Generation) • Dominant technology: G: GSM; U: HSUPA; C: CDMA 1xRTT; N: NB-IoT; S: RPMA; R: LTE low data rate (Cat 1 and below); L: LTE high data rate (Cat 3 and above) • Generation: 1…9	S1
VV	Variant function set based on the same platform [00…99]	00
MM	Major product version [00…99]	00
Q	Product grade: • B = professional • A = automotive	B
XX	Minor product version (not relevant for certification)	Default value is 00

Table 16: Part identification code

8.3 Ordering information

Ordering No.	Product
NANO-S100-00C	Single band 2.4 GHz RPMA module

Table 17: Product ordering codes

Appendix

A Glossary

Name	Definition
ACPR	Adjacent Channel Power Ratio
AP	Access Point
ASIC	Application-Specific Integrated Circuit
BOM	Bill of Materials
BW	Bandwidth
CMOS	Complementary Metal-Oxide-Semiconductor
CPOL	Clock Polarity (for SPI)
CPU	Central Processing Unit
DBPSK	Differential Binary Phase Shift Keying
DFS	Dynamic Frequency Selection
DPLL	Digital Phase-Locked Loop
D-DSSS	Dynamic Direct Sequence Spread Spectrum
EIRP	Effective Isotropic Radiated Power
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
GDI	Generic Digital Interfaces (power domain)
ERS	Equivalent Series Resistance
H	High
HBM	Human Body Model
I	Input (means that this is an input port for NANO-S100)
ISR	Interrupt Service Routine
FFS	Local File System
L	Low
LGA	Land Grid Array
MISO	Master Input, Slave Output
MOSI	Master Output, Slave Input
MRQ	Master Request
MSL	Moisture Sensitivity Level
N/A	Not Applicable (used in the I/O field of pinout)
NC	Do not connect
O	Output (means that this is an output port of NANO-S100)
PCB	Printed Circuit Board
PD	Pull-Down
PO	“Power Output” for the RF Transmitter
POS	Power-On Input (power domain)
PU	Pull-Up
RSSI	Receive Signal Strength Indicator
RPMA	Random Phase Multiple Access
RTC	Real Time Clock
SPI	Synchronous Peripheral Interface

Name	Definition
SRDY	Slave Ready
SRQ	Slave Request
TCXO	Temperature Compensated Crystal Oscillator
T	Tristate
TX	Transmit
UART	Universal Asynchronous Receiver/Transmitter
VCO	Voltage Controlled Oscillator
VSWR	Voltage Standing Wave Ratio

Table 18: Explanation of abbreviations and terms used

Related documents

[1] u-blox NANO-S100 System Integration Manual, Docu No UBX-16026400

[2] u-blox NANO-S100 Host Common Software Integration Application Note, Docu No UBX-16025680

[3] u-blox Package Information Guide, Docu No UBX-14001652

[4] Ingenu rACM Developer Guide Docu No 010-0105-00

[5] u-blox EVK-S10NANO (rACM2) NANO-S100 cellular evaluation kit User Guide, Docu No UBX-16031276

☞ For regular updates to u-blox documentation and to receive product change notifications, register on our homepage.

Revision history

Revision	Date	Name	Comments / Product Status
R01	11-Nov-2016	clee	Initial release
R02	09-Mar-2017	clee	Early Production Information Correction to Figure 2: NANO-S100 pin assignment Updated: WAKE to 3V3 "ON" timing requirement Updated: Module packaging information Updated: Module label Updated: Module height in “Mechanical Specifications”
R03	17-Mar-2017	clee	Correction to Figure 2 Updated Table 2
R04	19-Oct-2017	clee	Updated NANO-S100-00C product status

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