DESCRIPTION

Demonstration circuit 638 is a 36-72V_{IN} to 3.3V@3.5A isolated synchronous Flyback converter featuring the LT1725. This circuit was designed primarily to meet Voice over IP requirements, providing 3.3V@3.5A from a 37-54V/350mA source. However, converter operation is seamless over the full 36-72V input range. Isolation voltage is 1500VDC. The circuit features feedback without an opto-isolator, programmable load regulation compensation, input under voltage lockout and short circuit cycling protection to minimize thermal stress.

Design files for this circuit board are available. Call the LTC factory.

Table 1. Performance Summary (T_A = 25°C)

PARAMETER	CONDITION	VALUE
Minimum Input Voltage		36V
Maximum Input Voltage		72V
Output Voltage (V_{OUT})	V_{IN} = 36V to 72V, I_{OUT} = 0A to 3.5A	3.3V± 3%
Maximum Input Current	V_{IN} = 37V, I_{OUT} = 3.5A	350mA
Inrush Transient	V_{IN} = 72V	0.1 A^2s
Nominal Switching Frequency		200kHz
Output Short Circuit Period	Cycling, Auto-restart at 36 V_{IN}	700ms
Dynamic Response	Peak Deviation Load Step 50% to 100% Settling Time (to within 10mV of set point)	200mV 100µs 200µs
Efficiency	V_{IN} = 48V, I_{OUT} = 3.5A	89.5% Typical
Output Ripple	V_{IN} = 48V, I_{OUT} = 3.5A (20MHz BW)	200mV_{P-P}
Isolation Voltage		1500VDC
Isolation Resistance		10MΩ
Isolation Capacitance		2200pF

OPERATING PRINCIPLES

CIRCUIT OVERVIEW

This synchronous Flyback converter operates at a nominal switching frequency of 200kHz. Output voltage control is done by U1, the LT1725 controller. Galvanic isolation is met with transformer T1 and T2. C7 is used as a local bypass to reduce common-mode currents.

The primary side power path is comprised of T1, C25 and Q1 (the primary switch). Power is transferred during the off time of Q1. MOSFET Q3 is the secondary synchronous rectifier. C1, C2 and C29 form the secondary output filter. L1 and C30 form the primary input filter. An auxiliary winding on T1 performs two functions; it provides output feedback information and supplies bias voltage to the

LT1725. A driver, comprised of Q12 and Q13, synchronizes with the LT1725 via T2, a small pulse transformer, to provide gate drive to the secondary switching MOSFET.

During an output short circuit, the primary bias supply collapses. This results in the converter harmlessly cycling on and off, reducing power dissipation. The cycling rate is nominally 1.4Hz with 36V input. When the short is removed, the converter returns to normal operation.

When input voltage is applied, R8 provides trickle charge current to C10 resulting in a turn on delay of approximately 1.5s at $36V_{IN}$.

SAFETY AND ISOLATION

The demo board is designed to meet the requirements of UL 60950, 3rd Edition for basic insulation in secondary circuits. The input is considered a TNV-2 circuit, and the output is SELV. The bridging capacitor C7 has an agency file number. A 5A fast blow type fuse must be placed in series with the ungrounded (hot) input line. The transformer is designed to meet the basic insulation requirement with an isolation voltage of 1500VDC. The core is considered part of the secondary circuit.

CONDUCTED EMI

Tests for conducted emissions were performed for the demo board. An external filter using a 5μH inductor and 10μF film capacitor is required for the CISPR 22 class B limit. No tests for radiated RFI were performed. Proper grounding and layout technique must be observed to minimize radiation. See Figure 2 for EMI test setup. For EMI graphs see Figures 3 and 4.

RELIABILITY

Reliability prediction for the circuit has been calculated using the Telcordia (formerly Bellcore) SR-332. The black box technique was used. The calculation was made assuming a grounded, fixed, controlled environment and quality level II. A 50% electrical stress at 40°C yields an MTBF (mean time between failures) of 5.3 million hours.

QUICK START PROCEDURE

Demonstration circuit 638 is easy to set up to evaluate the performance of the LT1725. Refer to Figure 1 for proper measurement equipment setup and follow the procedure below:

When measuring the output voltage ripple, refer to note included in Figure 1. Care must be taken to avoid a long ground lead on the oscilloscope probe. Measure the output voltage ripple by touching the probe tip directly across the output capacitor C29 as shown in Figure 1.

Connect a 36V supply to V_{IN} as shown on Figure 1. For normal operation, a minimum of 36V must be applied at the input. Input voltages lower than 36V will keep the converter from turning on due to the undervoltage lockout feature in the LT1725.

Connect a 0-5A load and meters to the V_{OUT} pins as shown on Figure 1.

After all connections are made, turn on the input power and verify the output voltage, regulation, ripple voltage, efficiency and other parameters.

If there is no output, temporarily disconnect the load to make sure that the load is not set too high.

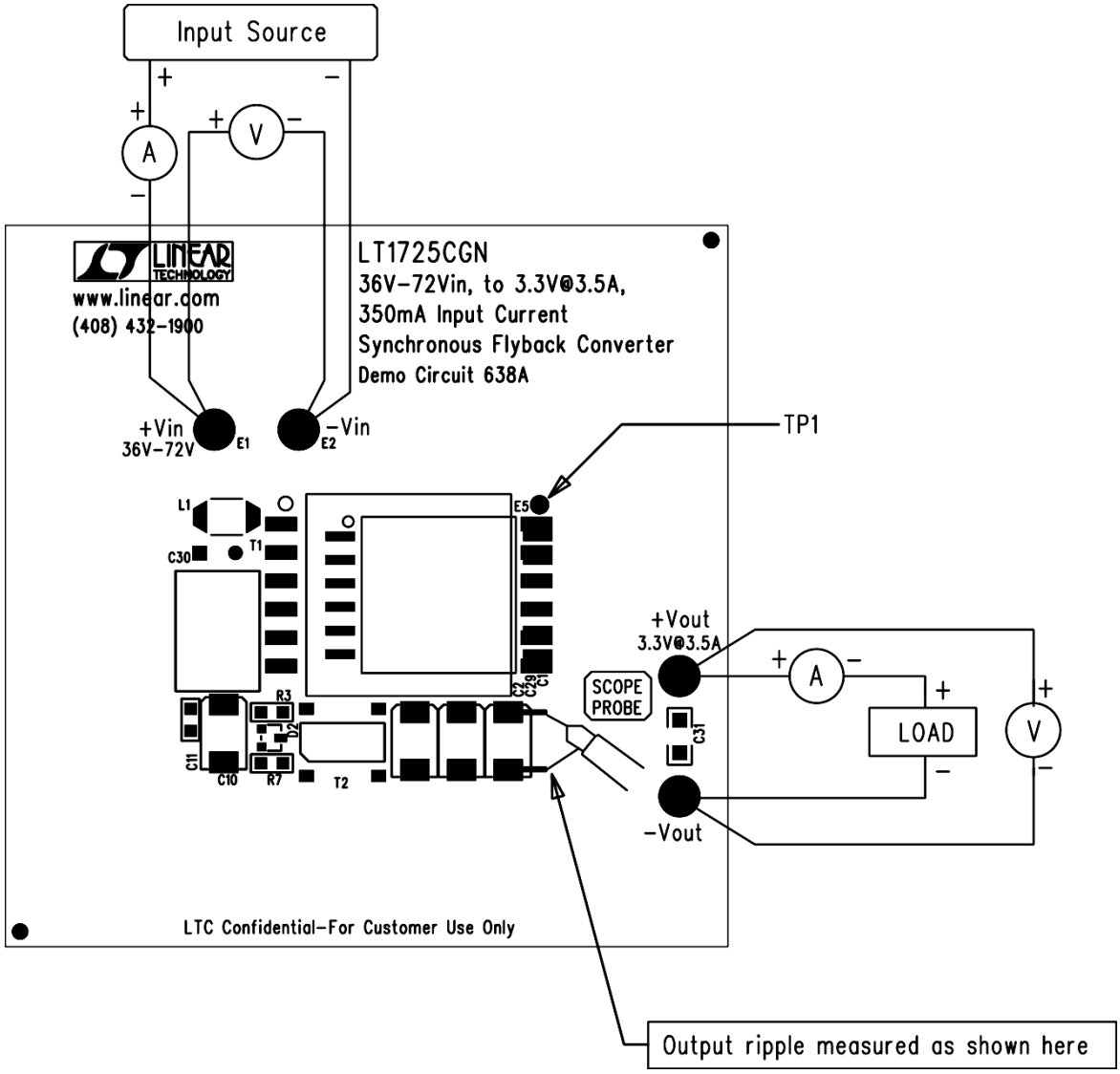


Figure 1. Proper Measurement Equipment Setup

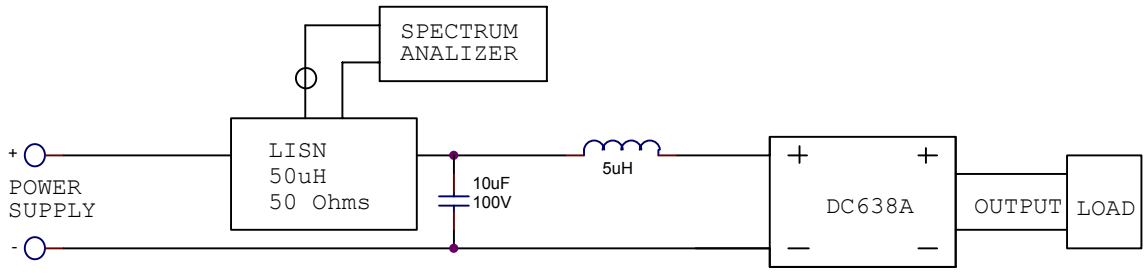


Figure 2. EMI Setup

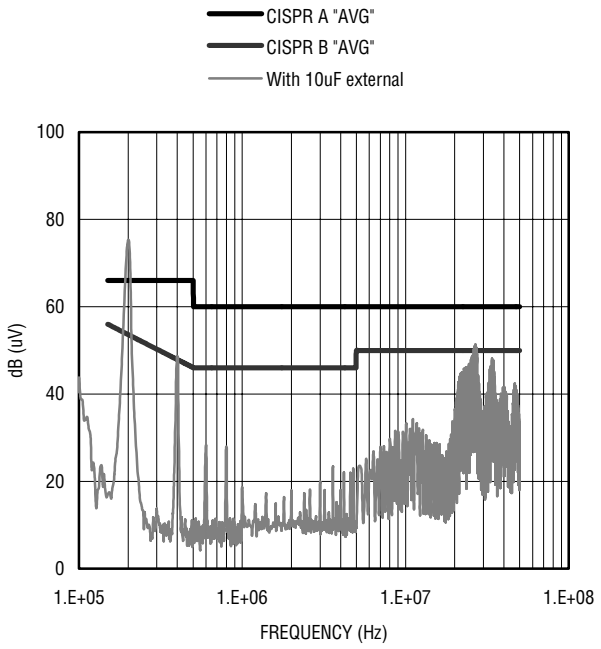


Figure 3. EMI Without Filter

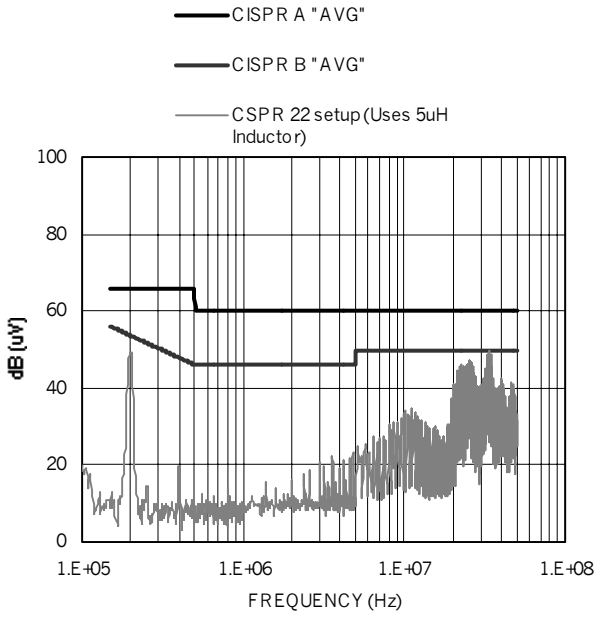
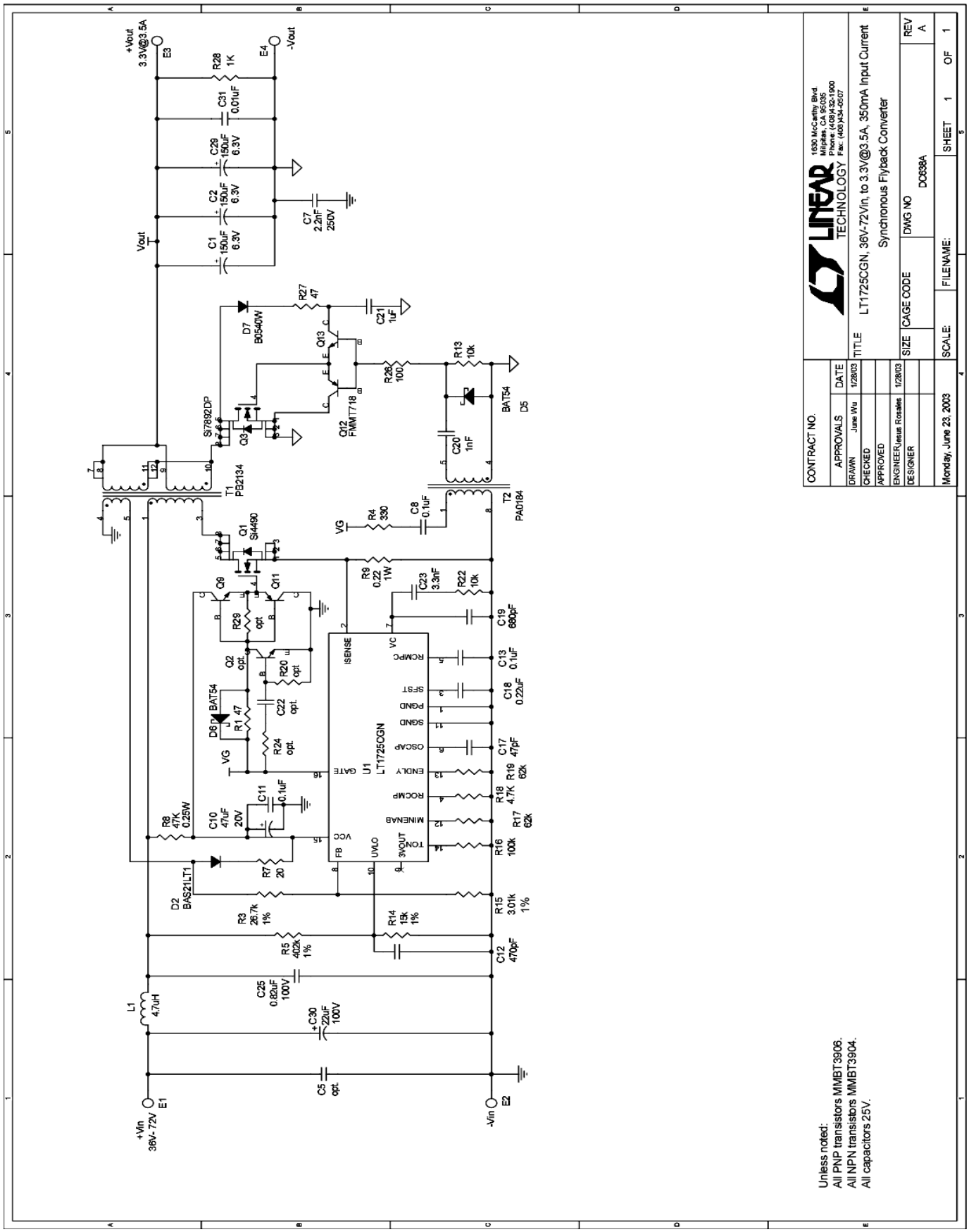


Figure 4. EMI With Filter


+Vout
3.3V@3.5A
E3
-Vout
E4
R28 1K
C31 0.01uF
C28 150uF 6.3V
C2 150uF 6.3V
C1 150uF 6.3V
C7 2.2nF 250V
Vout
D7 B0540W
R27 47
C21 1uF
Q13
R26 100
R13 10k
Q12 FMMT718
Si7892DP
Q3
BAT54 D5
C20 1nF
T1 PB2134
T2 PA0184
VG
R4 330
C8 0.1uF
Q1 Si4490
R9 0.22 1W
C23 3.3nF
R22 10k
Q9
Q11
R29 opt
Q2 opt
R20 opt
D6 BAT54
R1 47
C22 opt
R24 opt
C19 680pF
C13 0.1uF
C18 0.22uF
C17 47pF
R19 62k
R18 4.7K
R17 62k
R16 100k
C11 0.1uF
R8 47K 0.25W
C10 47uF 20V
R7 20
D2 BAS21LT1
R3 26.7k 1%
R5 402k 1%
R14 19k 1%
R15 3.01k 1%
C12 470pF
C25 0.82uF 100V
C30 22uF 100V
L1 4.7uH
C5 opt.
+Vin
36V-72V
E1
-Vin
E2
U1
LT1725CGN
ISENSE
VC
RCMPC
SFST
PGND
SGND
OSCAP
ENDLY
ROCMP
MINENAB
TONSET
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UVLO
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CONTRACT NO.
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APPROVED
ENGINEER Jesus Rosales 1/28/03
DESIGNER
TITLE
LT1725CGN, 36V-72Vin, to 3.3V@3.5A, 350mA Input Current
Synchronous Flyback Converter
SIZE
CAGE CODE
DWG NO
DC638A
REV
A
Monday, June 23, 2003
SCALE:
FILENAME:
SHEET 1 OF 1
Unless noted:
All PNP transistors MMBT3906.
All NPN transistors MMBT3904.
All capacitors 25V.