Application Note

DA14531/530 Hardware Guidelines

AN-B-075

Abstract

This Application Note provides the minimal reference schematic, circuit explanation, and design guidelines for BLE applications based on the DA14531 SoC.

The document also applies to the DA14530, but only the configuration in DCDC converter By-pass mode.

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1 Terms and Definitions

BLE	Bluetooth Low Energy
IC	Integrated Circuit
SoC	System on Chip
RF	Radio Frequency
PMU	Power Management Unit
SRAM	Static Random-Access Memory
OTP	One Time Programmable
UART	Universal Asynchronous Receiver Transmitter
GPIO	General Purpose Input Output (pin)
ILIM	DCDC Inductor peak current limit
JTAG	Joint Test Action Group
SWD	Serial Wire Debug
SPI	Serial Peripheral Interface
CS	Chip Select
SDK	Software Development Kit
PRO-Devkit	DA14531 PRO Development kit
PCB	Printed Circuit Board
PCBA	Printed Circuit Board Assembly
BOM	Bill Of Materials
DCR	DC Resistance
PTH	Plated Through Hole

2 References

[1] DA14531, Datasheet, Dialog Semiconductor.
[2] User Manual UM-B-008 DA14580 Production test tool
[3] User Manual UM-B-114 DA14531 Devkit-Pro-Hardware
[4] ETSI EN 300 328 and EN 300 440 Class 2 (Europe)
[5] FCC CFR47 Part 15 (US)
[6] ARIB STD-T66 (Japan)
[7] AN-B-073 DA14531 Filter for Spurious Emissions Reduction
[8] AN-B-072 DA14531 Booting Options
[9] AN-B-088 DA145xx Flash Selector Guide

3 Introduction

DA14531 is an ultra-low power SoC that integrates a 2.4 GHz transceiver and an ARM Cortex M0+™ microcontroller with 48 kB of RAM and 32 kB of OTP memory. DA14531 can be used as a standalone application processor, or as a data pump in hosted systems.
This document is valid for the DA14530 as well. Because of the missing DCDC converter, only the parts related to Bypass mode are applicable.

Key characteristics:

- Compatible with:
    - Bluetooth V5.1
    - ETSI EN 300 328 and EN 300 440 Class 2 (Europe)
    - FCC CFR47 Part 15 (US)
    - ARIB STD-T66 (Japan)
- Supports up to 3 Bluetooth LE connections
- Fast cold boot to radio-active in less than 30 ms
- Memories:
    - 32 kB One-Time-Programmable (OTP)
    - 48 kB Retainable System RAM
    - 14 kB ROM
    - Ram retainability configured in 3 blocks
        - SysRAM1(16 kB)
        - SysRAM2(12 kB)
        - SysRAM3(20 kB)
- Integrated Buck/Boost DCDC converter
    - Buck: 1.8 V ≤ VBAT_HIGH ≤ 3.3 V if OTP read needed
    - Buck: 1.1 V ≤ VBAT_HIGH ≤ 3.3 V if RAM retained
    - Boost: 1.1 V ≤ VBAT_LOW ≤ 1.65 V
    - Clock-less hibernation mode: Buck 270 nA, Boost 240 nA
    - Built-in temperature sensor for die temperature monitoring
- Digital interfaces
    - GPIOs: 6 (WLCSP17), 12 (FCGQFN24)
    - Two UARTs (one with flow control)
    - SPI Master/Slave - SPI data flash is connected to DA14531 on this development kit
    - I2C bus at 100 kHz, 400 kHz
    - 3-axes capable Quadrature Decoder – not applied in this development kit
    - Keyboard controller mode – not applied in this development kit
- Analog interfaces
    - 4-channel, 10-bit ADC
- Radio transceiver
    - Fully integrated 2.4 GHz CMOS transceiver
    - Single wire antenna: no RF matching or RX/TX switching required
- Two packages available, WLCSP with 17 balls and FCGQFN with 24 pins
    - WLCSP17: 6 GPIOs available
    - FCGQFN24: 12 GPIOs available

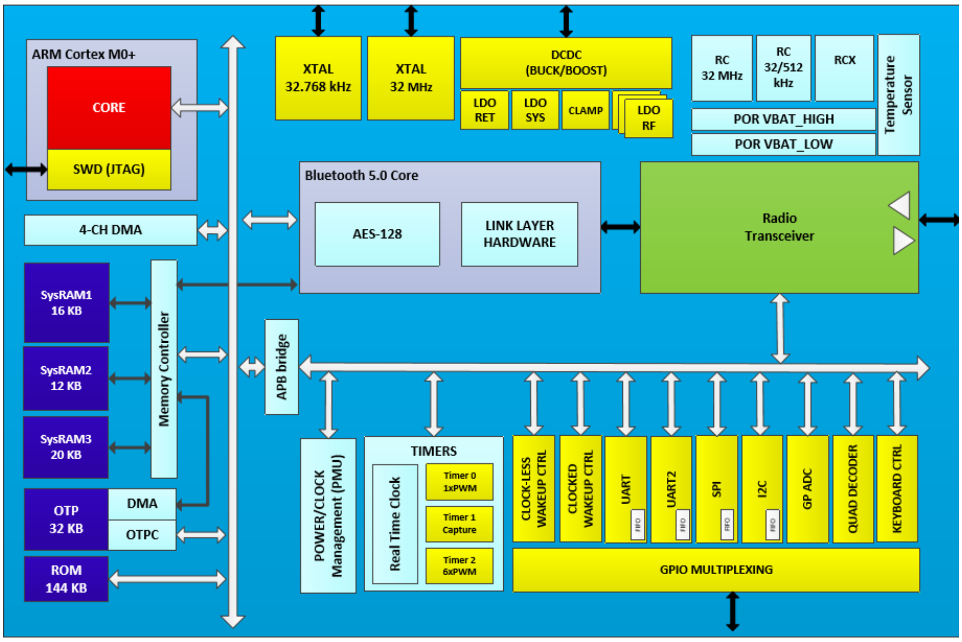


Figure 1: DA14531 Block Diagram

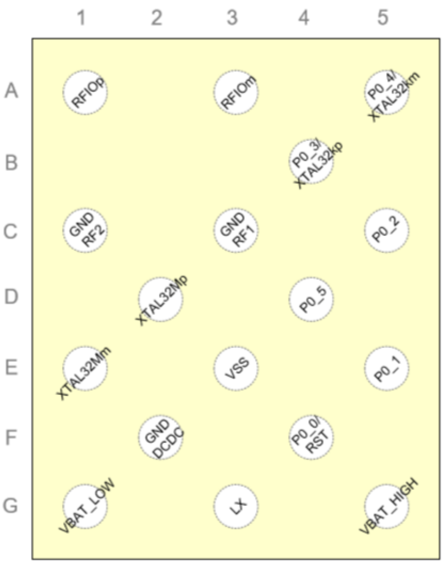


Figure 2: WLCSP17 Ball Assignment (Top View)

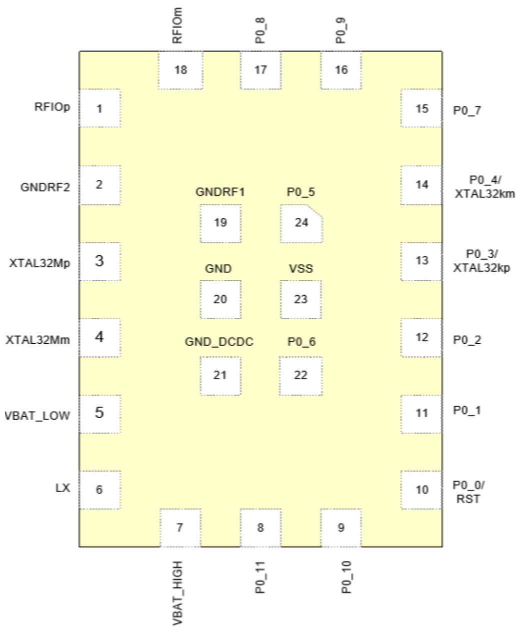


Figure 3: FCGQFN24 Pin Assignment (Top View)

Table 1: Ordering Information

Part Number	Package	Pitch (mm)	Size (mm)
DA14531-00000FX2	FCGQFN24	0.4	2.2 x 3.0
DA14531-00000OG2	WLCSP17	0.5	1.694 x 2.032

3.1 Device Revision Numbering and Marking

The revision number of the chip can be read from the device by reading the registers mentioned in Table 2 and Table 3. The result should be one of the options in Table 4.

Table 2: CHIP_REVISION_REG (0x50003214)

Bit	Mode	Symbol	Description	Reset
7:0	R	CHIP_REVISION	Chip version, corresponds with type number in ASCII 0x41 = 'A', 0x42 = 'B'.	-

Table 3: CHIP_TEST1_REG (0x500032F8)

Bit	Mode	Symbol	Description	Reset
7:0	R	CHIP_LAYOUT_REVISION	Chip layout version, corresponds with type number in ASCII	-

Table 4: Chip Revision Numbering

Commercial Number	Package	CHIP_REVISION_REG (0x50003214)	CHIP_TEST1_REG (0x500032F8)
DA14531-00000FX2	FCGQFN24	0x41 (A)	0x45 (E)
DA14531-00000OG2	WLCSP17	0x41 (A)	0x45 (E)

3.2 The DA14531 System

Only a few external components are required to have DA14531 operational. The necessary components are:

- Inductor, 2.2 µH for internal DCDC converter. Necessary for buck and boost configuration. In bypass configuration, the inductor can be removed
- Capacitors on VBAT_HIGH and VBAT_LOW for internal DCDC converter. Their value depends on the DCDC configuration and the type of power source
- XTAL 32 MHz, provides the main system and BLE clock
- XTAL 32 kHz, as the low-power clock in sleep mode. When RCX (less accurate) is used, XTAL 32 kHz can be omitted
- For some applications an RF low-power filter is required to supress spurious emissions.
- Antenna. Is either printed or ceramic

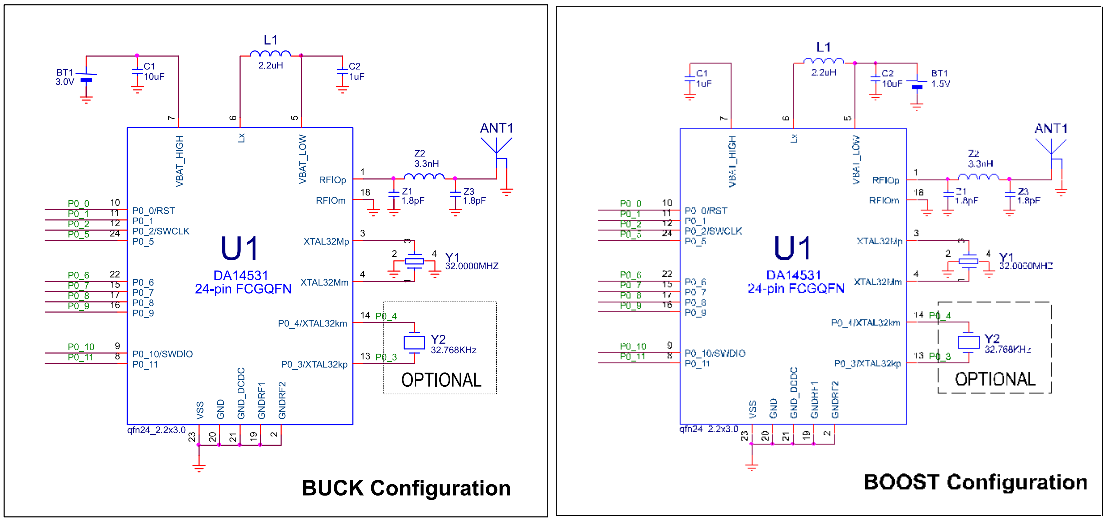


Figure 4: DA14531 System Configurations

3.2.1 The Power Section of DA14531

The DA14531 has a flexible power setup and can operate in three different power configurations: Buck, Boost and Bypass. Depending on the available power source, Buck mode is intended for use with higher voltage batteries, such as lithium primary cells (3 V) or 2x alkaline combinations, while Boost mode can be used with lower voltage Silver oxide cells. In Bypass mode, the DCDC converter is not used and because of that there is no need for an external inductor. This results in a cheaper BOM, but also in lower power efficiency.

The power management logic is fully integrated, and the user can select the desired mode with minor hardware modifications.

3.2.1.1 The PMU of DA14531

The DA14531 has an integrated Power Management Unit (PMU), which consists of a VDD Clamp, Power on Reset (POR) circuitry, a DCDC converter and various LDOs.

The PMU integrates two main power rails VBAT_HIGH and VBAT_LOW, and the internal VDD power rail.

- VBAT_HIGH voltage is in the range of 1.8 V – 3.3 V. This power rail is used for the blocks that require a higher supply voltage. The OTP and the GPIOs are connected to this power rail. The lowest voltage for OTP reading is 1.62 V whereas to write OTP this is 2.25 V.
  VBAT_HIGH is protected by the power-on-reset circuit POR_HIGH, which will generate a Power On Reset when the voltage drops below 1.66 V (V_IL) for more than 50 µs and will release the reset at typically 1.75V.
- VBAT_LOW is the main system supply, with the lowest voltage equal to 1.1 V. The functional range is between 1.1 V - 3.3 V.

When used in Boost mode, the default voltage range is **1.1 V - 1.65 V**. Within this range the boost converter can provide a VBAT_HIGH supply in the range of 1.8 V - 3.0 V.
As most internal blocks are powered from this power rail through LDOs (Figure 5), the most efficient voltage to apply is 1.1 V.
Higher input voltage is allowed when additional settings are made to regulate DCDC boost behavior. VBAT_LOW is protected with the power-on-reset circuit POR_LOW, which will generate a HW reset when the voltage drops below 1.0 V (V_IL) for more than 50 µs and release the reset at typically 1.66V. See Power On Reset section in datasheet of DA14531.

- The internal VDD power rail supplies the digital power domains including RAM blocks. It is generated internally, and the voltage is between 0.7 V and 0.9 V, depending on the power mode of the system (active, sleep, etc.).

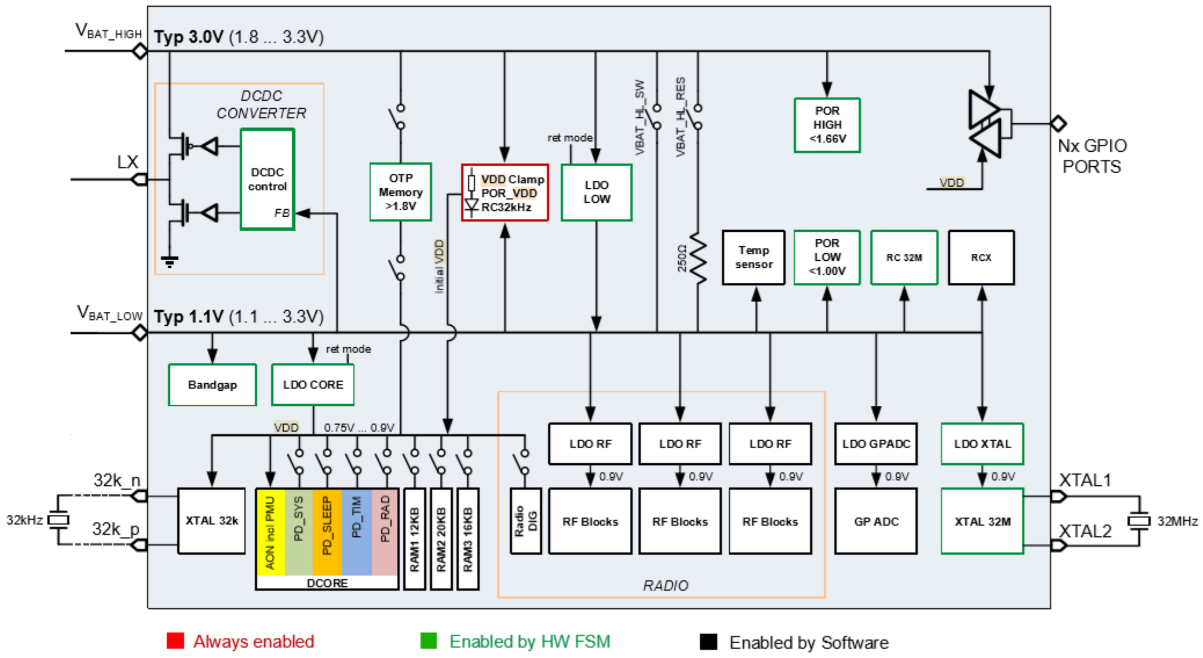


Figure 5: DA14531 SoC power management unit (PMU)

There are 3 setups for the DCDC converter of the PMU: buck, boost and bypass mode. The difference of this setups is given by where the battery voltage is applied (Figure 6).

Please notice that in bypass mode, VBAT_HIGH and VBAT_LOW rails are tied together and the DCDC converter is not used.

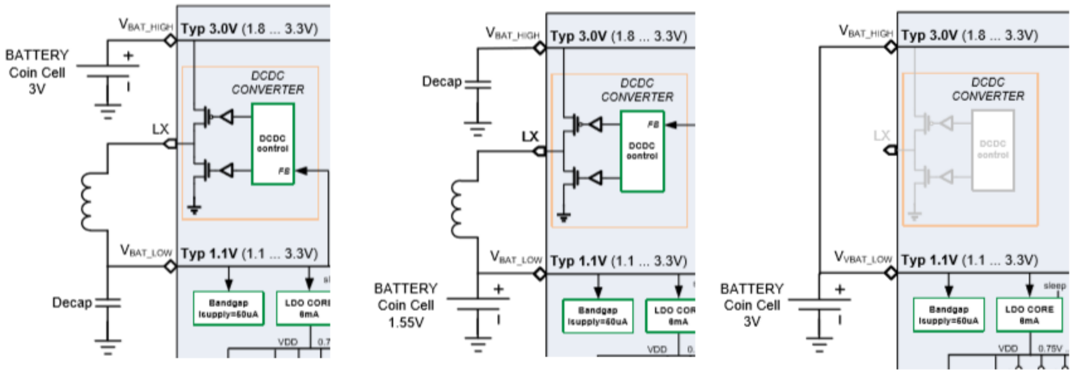


Figure 6: Battery Connection for Buck (Left), Boost (Middle) or Bypass (Right) Configuration

Table 5: Typical Rail Voltages and their Sources in the Various PMU Modes

Configuration	Mode	VBAT_HIGH		VBAT_LOW	
		Voltage range	supplied to / generated from	Voltage range	supplied to / generated from
BUCK *Supply on VBAT_HIGH*	Active	1.8 V to 3 V	VBAT	1.1 V	DCDC out
	Deep or Extended Sleep	1.8 V to 3 V	VBAT	1.1 V	LDO_LOW
	Hibernation	1.8 V to 3 V	VBAT	0 V	
BOOST *Supply on VBAT_LOW*	Active	1.8 V, 2.5 V or 3 V	DCDC out	1.1 V to 1.65 V	VBAT
	Deep or Extended Sleep	1.8 V - 1.55 V	none, drops then clamped to VBAT_LOW	1.1 V to 1.65 V	VBAT
	Hibernation	VBAT_LOW, diode drop		1.1 V to 1.65 V	VBAT
Bypass *Supply on VBAT_HIGH,* *VBAT_LOW*	Active	1.8 V to 3 V	VBAT	1.8 V to 3 V	VBAT
	Deep or Extended Sleep	1.8 V to 3 V	VBAT	1.8 V to 3 V	VBAT
	Hibernation	1.8 V to 3 V	VBAT	1.8 V to 3 V	VBAT

3.2.1.2 Important Notices for PMU

Boost Mode: any external circuit connected to the VBAT_HIGH rail must be disabled during boot, as any load on the rail may prevent the voltage from reaching the required value, which will in turn prevent the startup of the system. For a guaranteed startup, the load on VBAT_HIGH must not exceed 50 µA during system startup/wake-up.

A flash memory supplied by VBAT_HIGH might exceed this current limit during boot, even if the chip select pin (nCS) of the flash memory is pulled high. Therefor it is needed to cut off the flash supply during boot. A secondary bootloader is needed to control the supply switch in front of the flash to allow reading the flash after the DCDC converter has stabilized. In Figure 7 possible implementations are given.

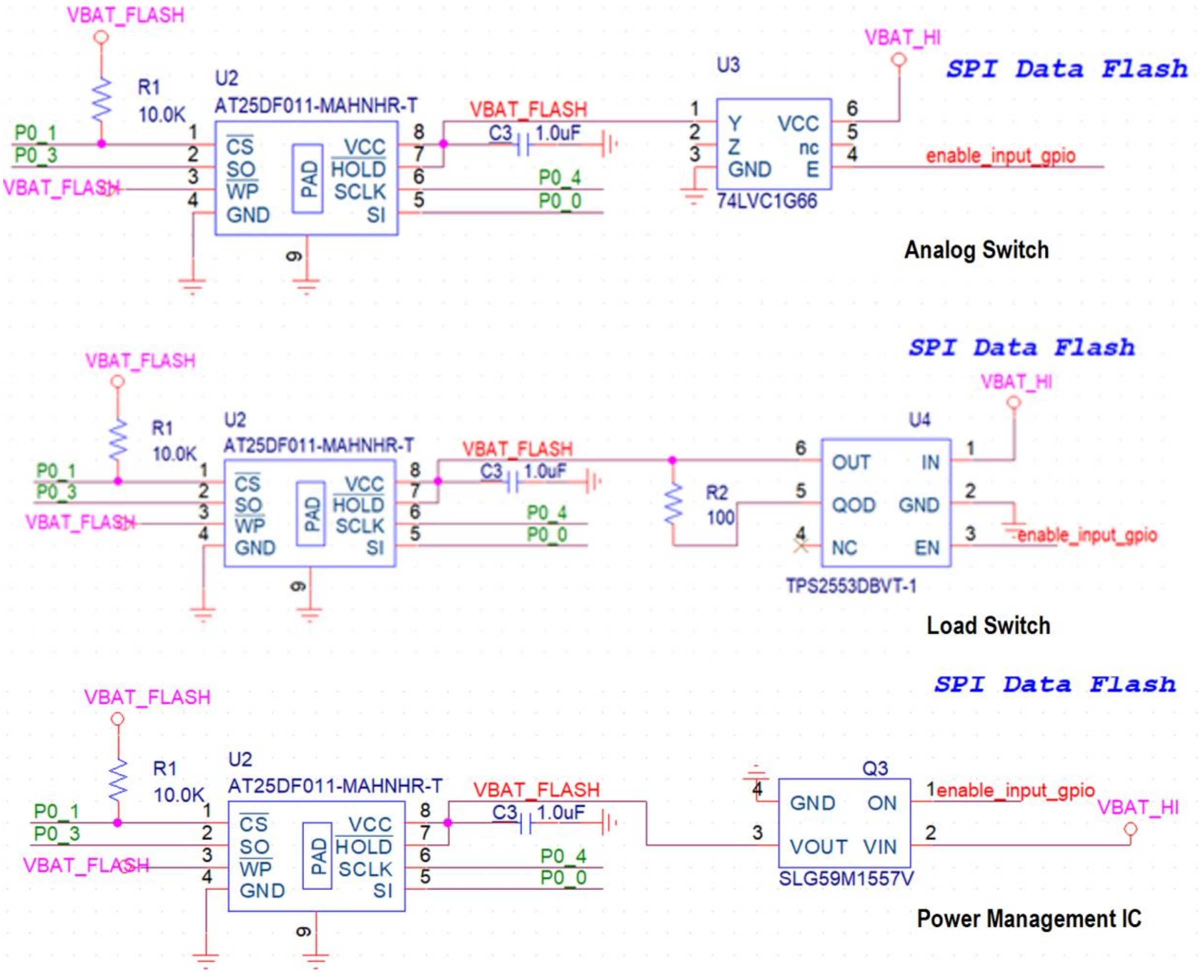


Figure 7: Supply switching of a flash memory in boost mode

Bypass mode: VBAT_HIGH and VBAT_LOW are shorted on the PCB. This mode is detected by the chip as boost mode. The software should set the CFG_POWER_MODE_BYPASS flag. Otherwise the software would stop after booting, when the supply is below 3V.

As the DCDC converter cannot boost VBAT_HIGH to 1.8V (default), the initial voltage on VBAT_HIGH must be above 1.75 V to release the POR_HIGH and allow booting.

If the voltage in the system drops below 1.66 V after booting, POR_HIGH must be masked or disabled to prevent a reset.

3.2.1.3 Supplying External Loads

The internal DCDC converter of the DA14531 can be used to supply external loads, in both buck and boost mode. Use the application software to select and trim the output voltage.

In Table 6, the external load driving capability of the DCDC converter is summarized.

Table 6: DA14531 DCDC External Load Supply Capability

Configuration	VBAT_High	VBAT_Low	Maximum load current
BUCK	3.0 V (in)	1.1 V (out)	20 mA
BOOST	1.8 V (out)	1.5 V (in)	20 mA
BOOST	2.5 V (out)	1.5 V (in)	10 mA
BOOST	3.0 V (out)	1.5 V (in)	10 mA

In buck mode, VBAT_LOW is the source for the load current, while in boost mode, VBAT_HIGH is the source for the load current.

From a system point of view, this is very interesting for boost mode, where the DA14531 can replace the step-up DCDC converters needed to supply loads like SPI data flash or sensors, and so on, and consequently reduce the BOM cost considerably. Note that, as mentioned in Important Notices for PMU, users must pay special attention to the load current during initialization, which in boost mode must not exceed 50 μA.

3.2.1.4 The Passive Components

The DCDC converter is internal to the SoC circuit and requires only three external components: two capacitors and one inductor. As the DCDC converter must meet the input and output voltage and load current specifications, proper selection of the external components is very important.

Capacitors

Two capacitors are required, C1 attached to the VBAT_HIGH rail pin, and C2 attached to the VBAT_LOW rail.

The capacitors are of the type Multi-Layer Ceramic Capacitor (MLCC). Note that in MLCC capacitors, the effective capacitance value depends on the DC voltage applied to the capacitor.

For example, GRM155R61E225ME15D is a 2.2 μF capacitor with a rated voltage of 25 V. With 3 VDC applied on its pins, the effective capacitance drops to 1.39 μF.

The user must take this into account and select the parts carefully, because a poor capacitor value can degrade system performance.

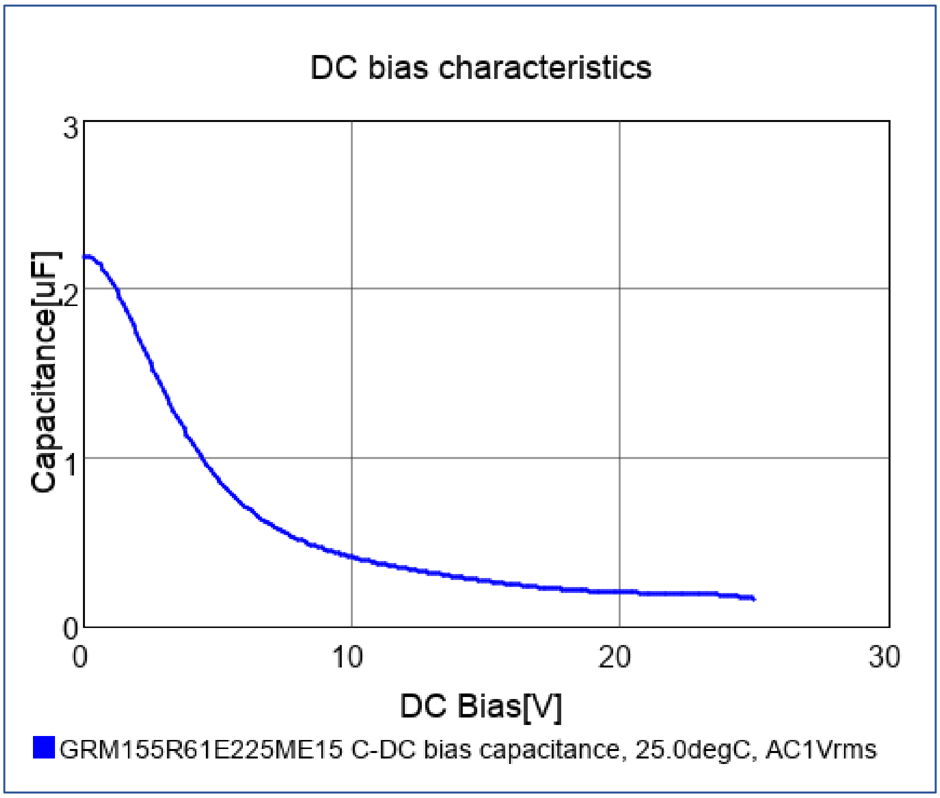


Figure 8: Effective Capacitance of a 2.2 µF Ceramic Capacitor

Example: on the DA14531 PRO-Devkit, the capacitor value for the C2 in boost mode affects the df2 characteristic of the radio.

For C2 = 2.2 µF, df2 is lower than the specification. The effective capacitance is 1.39 µF.

For C2= 10 µF, df2 is on 215 kHz, well above the limit.

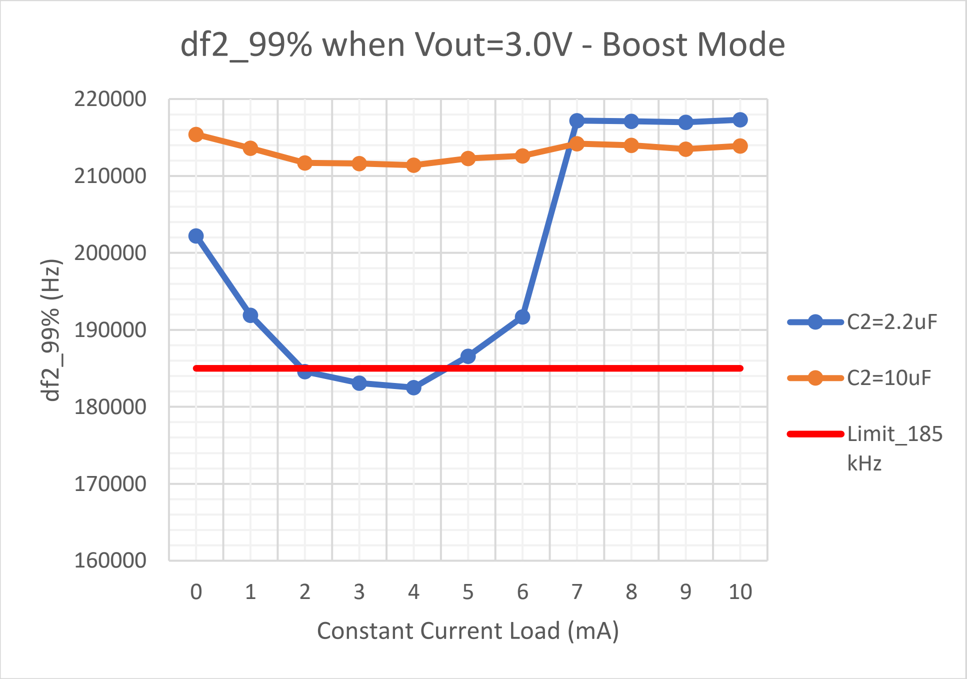


Figure 9: df2 Performance Versus C2 Value in Boost Mode

Buck mode

C1: 10 µF effective (input capacitor)

C2: 1 µF effective (output filter capacitor)

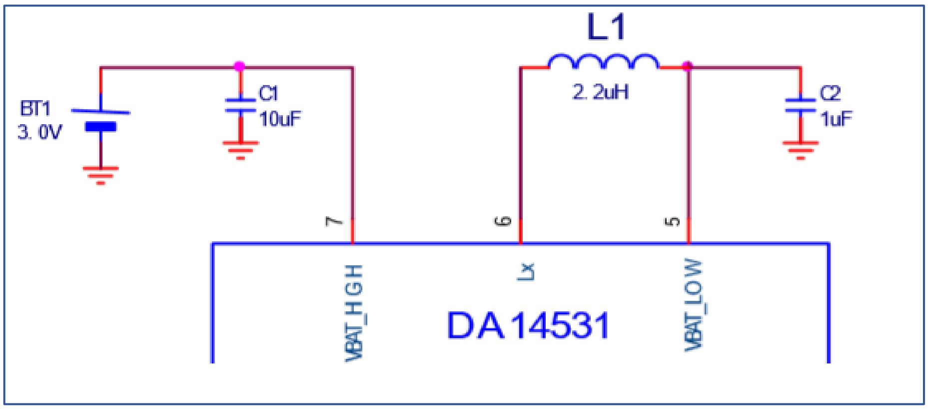


Figure 10: Buck Configuration

Boost mode

C1: 1 µF effective (output filter capacitor)

C2: 10 µF effective (input capacitor)

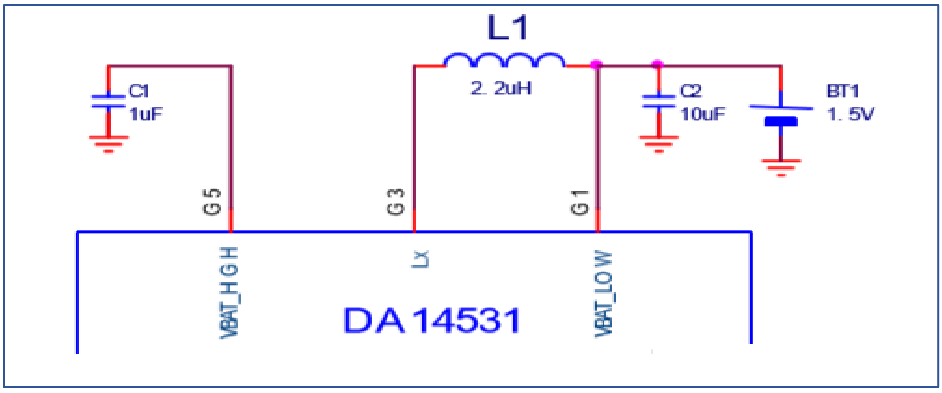


Figure 11: Boost Configuration

Bypass mode

In bypass mode, the DCDC converter is not used and C1, C2 are used for decoupling. As the two power pins (VBAT_High and VBAT_Low) are located very close, a capacitor of 1 µF is enough. See Figure 12.

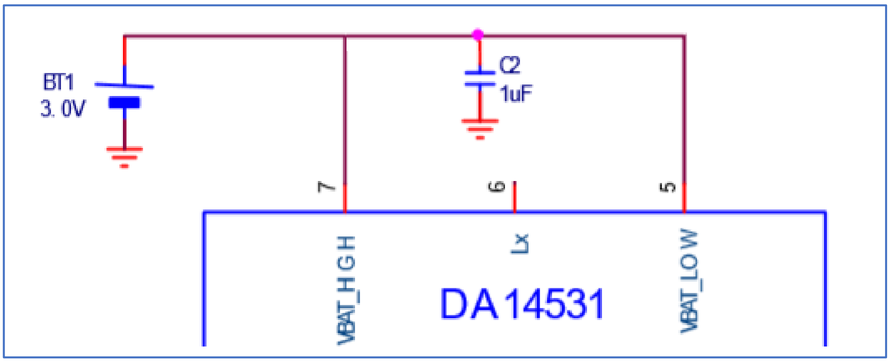


Figure 12: Bypass Configuration

Inductor

The DA14531 DCDC converter requires an external 2.2 µH inductor. The choice of inductor will impact the DCDC converter efficiency. Generally, larger inductors with alloy/metal composite cores, low DC resistance and high resonance frequency will give better efficiency.

For optimal operation of the DCDC converter, use the general criteria below to select a suitable part:

- 40 MHz Self resonance or higher
- 500 mOhm ESR or lower (the lower the better)
- 2.2 µH with 20% or lower tolerance
- Shielded inductors preferred over unshielded types

The inductor used on DA14531 PRO-development kit is the DFE2016E-2R2M of Murata.

Table 7: DFE2016E-2R2M Characteristics

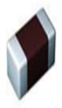
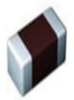
DCR	0.14 Ω
Imax	1.7 A
Package	0806
Shielded	yes

In Figure 13 to Figure 16 (notified as * DFE2016E-2R2M) below, the performance of the DCDC converter with DFE2016E-2R2M is presented. Performance justifies cost and size.

In cases where we need to reduce the size of the system, and the external load currents are negligible, it is possible to reduce the physical size of the power inductor. By doing so, the expectation is that some of the conversion efficiency is sacrificed. So, the user must find the optimal tradeoff among power efficiency, size and cost, depending on the intended application. The characteristics of selected inductors tested on the system are presented in Table 8.

Figure 13, Figure 14, Figure 15 and Figure 16 show the performance (efficiency) of the DCDC converter for buck and boost (3 V, 2.5 V and 1.8 V) configurations. The efficiency is measured for the load as described in Table 6.

Table 8: Tested Inductors on DA14531 PRO-Devkit

Image:												
Mfr.'s Part No:	DFE201610E-2R2M=P2	MAKK2016T2R2M	LPWI201610S2R2T	MLZ2012A2R2WT000	BRC2012T2R2MD	PFL1609-222MEU	LQM18FN2R2M00D	LQM18PN2R2NC0L	BRL1608T2R2M	LB2016T2R2M	CBMF1608T2R2M	LBR2012T2R2M
Manufacturer:	Murata	Taiyo Yuden	Littelfuse	TDK	Taiyo Yuden	Coilcraft	Murata	Murata	Taiyo Yuden	Taiyo Yuden	Taiyo Yuden	Taiyo Yuden
Description:	Fixed Inductors 0806 2.2uH 20% 5.5A RDC=0.026ohms	Fixed Inductors 0806 2.2uH 160mOhms +/- 20%Tol 1.5A HiCur	Fixed Inductors 2.2uH 20% 0806	Fixed Inductors 2.2uH 20%	Fixed Inductors 0805 2.2uH 143mOhms +/- 20%Tol 1000mA	Fixed Inductors PFL1609 Low Profile 2.2 uH 20 % 0.63 A	Fixed Inductors 2.2uH Power Supply Choke	Fixed Inductors 1.65x0.99mm 2.2uH 700mA+/-30%	Fixed Inductors 0603 2.2uH 520mOhms +/- 20%Tol 360mA	Fixed Inductors 0806 2.2uH 169mOhms +/- 20%Tol 375mA	Fixed Inductors 0603 2.2uH 221mOhms +/- 20% 190mA	Fixed Inductors 0805 2.2uH 169mOhms +/- 20%Tol 260mA
Lifecycle:	-	-	New Product	-	-	-	-	-	-	-	-	-
Datasheet:	Datasheet	Datasheet	Datasheet	Datasheet	Datasheet	Datasheet	Datasheet	Datasheet	Datasheet	Datasheet	Datasheet	Datasheet
Price 1:	0.419 €	0.201 €	0.279 €	0.122 €	0.297 €	0.951 €	0.131 €	0.314 €	0.314 €	0.148 €	0.227 €	0.096 €
Price 1k:	0.156 €	0.080 €	0.110 €	0.052 €	0.118 €	0.455 €	0.055 €	0.122 €	0.127 €	0.063 €	0.091 €	0.038 €
Package/Case:	0806 (2016 metric)	0806 (2016 metric)	0806 (2016 metric)	0805 (2012 metric)	0805 (2012 metric)	0603 (1608 metric)	0603 (1608 metric)	0603 (1608 metric)	0603 (1608 metric)	0806 (2016 metric)	0603 (1608 metric)	0805 (2012 metric)
Height:	1 mm	1 mm	1 mm	0.85 mm	1.4 mm	0.95 mm	0.9 mm	0.5 mm	0.7 mm	1.6 mm	0.8 mm	1.6 mm
Length:	2 mm	2 mm	2 mm	2 mm	2 mm	1.8 mm	1.6 mm	1.6 mm	1.6 mm	2 mm	1.6 mm	2 mm
Inductance:	2.2 uH	2.2 uH	2.2 uH	2.2 uH	2.2 uH	2.2 uH	2.2 uH	2.2 uH	2.2 uH	2.2 uH	2.2 uH	2.2 uH
Tolerance:	20%	20%	20%	20%	20%	20%	20%	30%	20%	20%	20%	20%
Test Frequency:	1 MHz	2 MHz	1 MHz	10 MHz	1 Mhz	7.9 MHz	1 MHz	1 MHz	1MHz	7.96 MHz	7.96 MHz	7.96 MHz
Maximum DC Current:	1.7 A	1.5 A	1.6 A	650 mA	1.1 A	630 mA	120 mA	700 mA	360 mA	375 mA	190 mA	260 mA
Saturation Current:	2.4 A (ΔL=30%)	1.5 A (ΔL=30%)	1.5 A (ΔL=30%)	210 mA (ΔL=50%)	1.1 A (ΔL=30%)	470 mA (ΔL=30%)	120 mA (ΔL=30%)	250mA (ΔL=30%)	360 mA (ΔL=30%)	375 mA (ΔL=10%)	190 mA (ΔL=30%)	260mA (ΔL=20%)
Maximum DC Res.:	140 mOhms	160 mOhms	150 mOhms	195 mOhms	110 mOhms	470 mOhms	400 mOhms	300 mOhms	400 mOhms	130 mOhms	170 mOhms	130 mOhms
Self Resonant Frequency:	50MHz*	50MHz*	70 MHz*	120 MHz	350 MHz	130 MHz	80 MHz	50 MHz	400 MHz	70 MHz	80 MHz	80 MHz
Minimum Operating Temperature:	- 40 C	- 40 C	- 40 C	- 55 C	- 40 C	- 40 C	- 55 C	- 55 C	- 40 C	- 40 C	- 40 C	- 40 C
Maximum Operating Temperature:	+ 125 C	+ 125 C	+ 125 C	+ 125 C	+ 105 C	+ 125 C	+ 125 C	+ 125 C	+ 105 C	+ 105 C	+ 105 C	+ 105 C
Shielding:	Shielded	Shielded	Shielded	Shielded	Unshielded	Shielded	Shielded	Shielded	Unshielded	Unshielded	Unshielded	Unshielded
Type:	Wirewound	Wirewound	Thin film	Multilayer	Wirewound	Wirewound	Multilayer	Multilayer	Wirewound	Wirewound	Wirewound	Wirewound
Core Material:	Metal Alloy	Metal	Metal Alloy	Ferrite	Ferrite	Composite	Ferrite	Ferrite	Ferrite	Ferrite	Ferrite	Ferrite

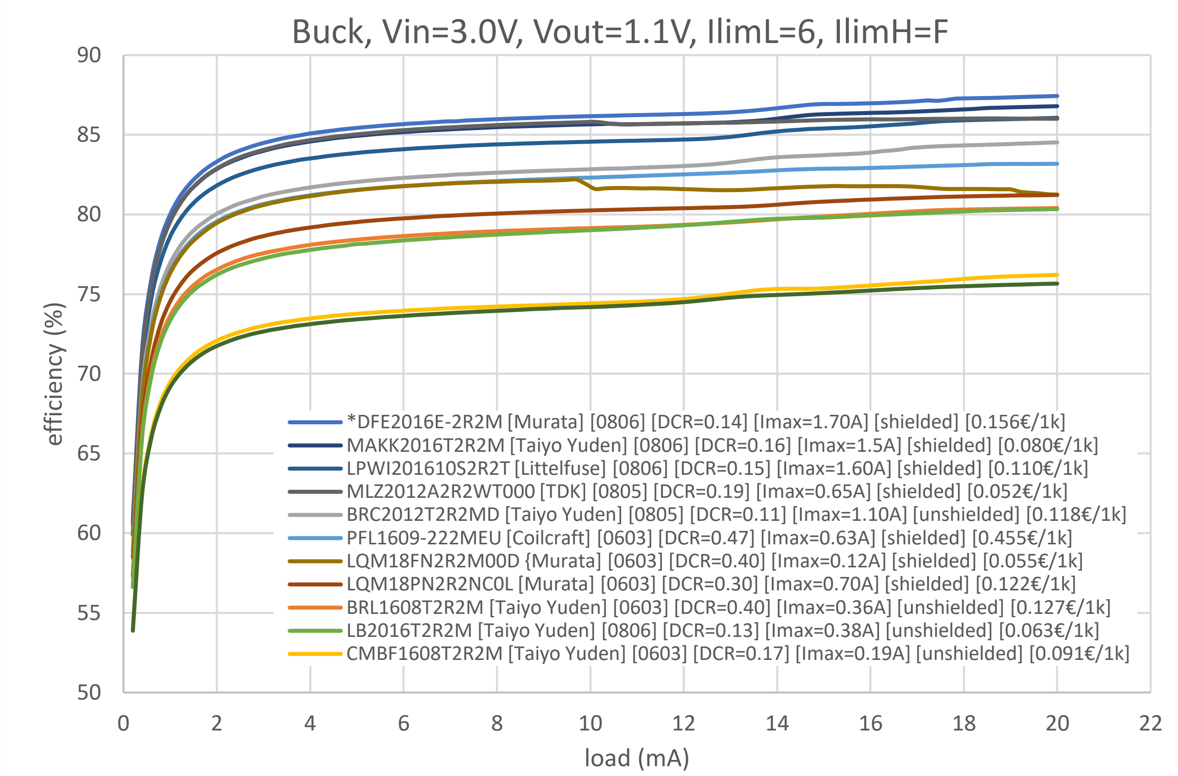


Figure 13: DA14531 DCDC Power Efficiency. DCDC is Configured in BUCK Mode

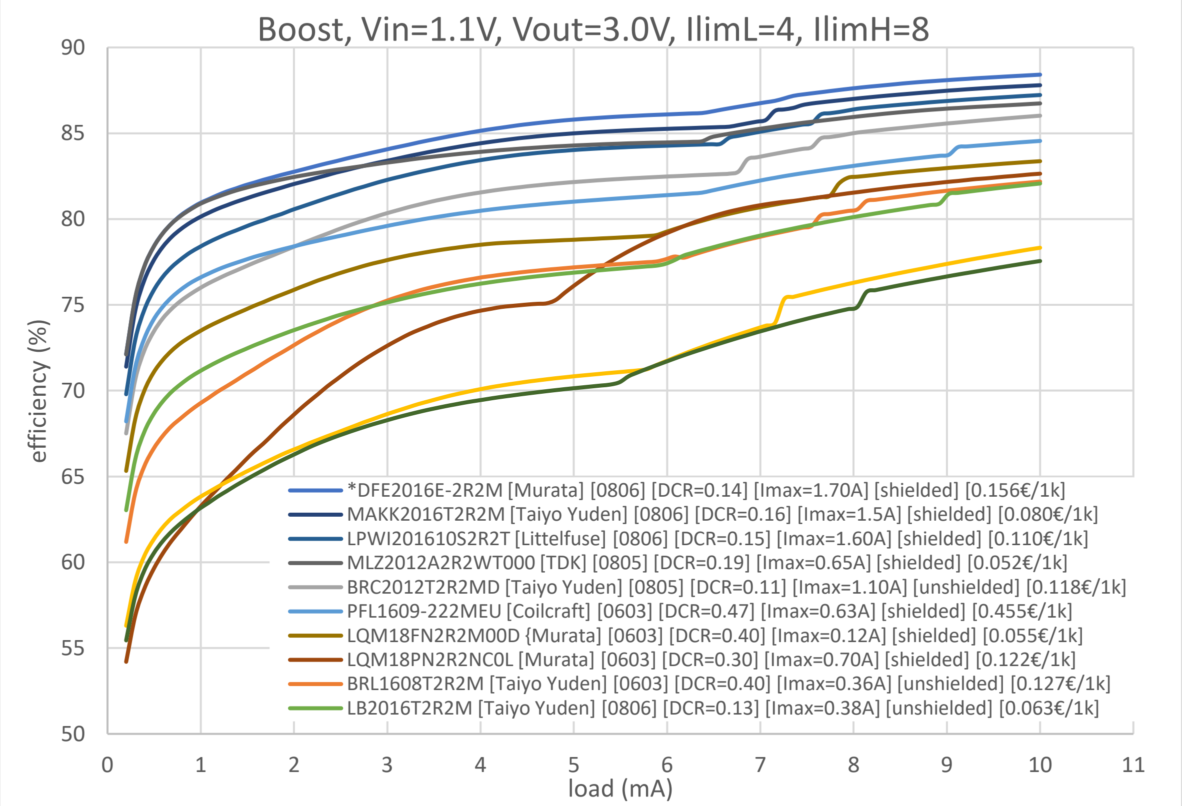


Figure 14: DA14531 DCDC Power Efficiency. Boost Mode, Produced Voltage VBAT_HIgh=3V

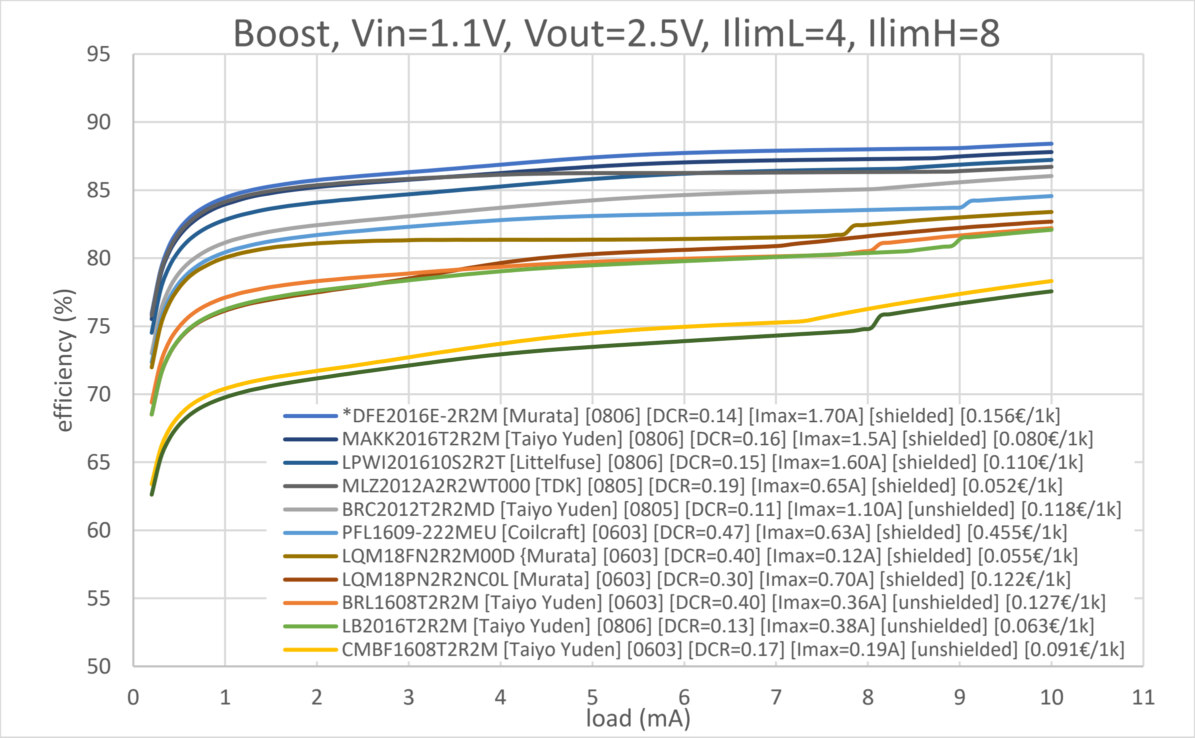


Figure 15: DA14531 DCDC Power Efficiency. Boost Mode, produced voltage VBAT_HIgh=2.5V

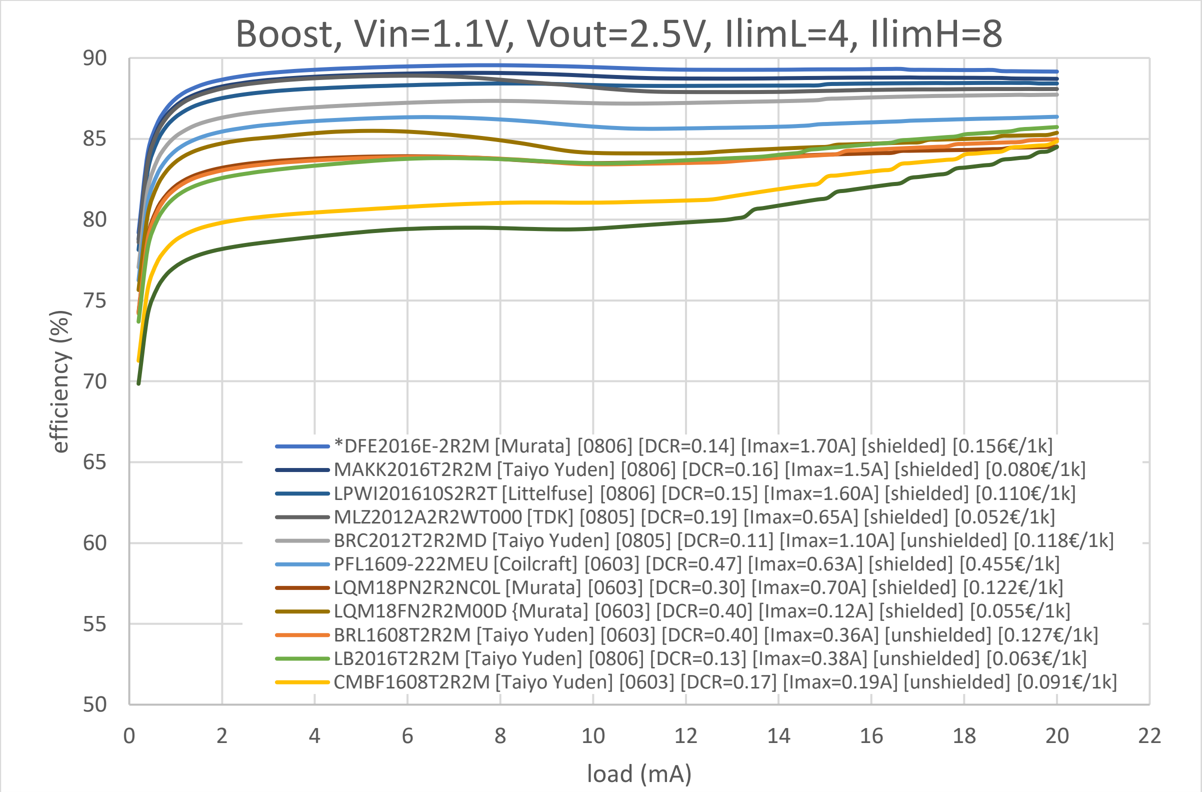


Figure 16: DA14531 DCDC Power Efficiency. Boost Mode, Produced Voltage VBAT_HIgh=1.8V

ILIM defines the peak current of the Inductor of the DCDC converter (L1). The peak current varies between DCDC_ILIM_MAX (iLimH) and DCDC_ILIM_MIN (liLimL). DCCD_ILIM_MAX is the maximum peak current that can pass through the Inductor. For a peak current higher than this limit, the internal switch of the DCDC converter is deactivated.

DCDC_ILIM_MIN and DCDC_ILIM_MAX can be set between 6 mA and 96 mA, with a 6 mA step.

Table 9: Inductor Peak Current Limit

Inductor peak current	DCDC_CTRL_REG (0x50000080)P bits	Default	Current
DCDC_ILIM_MAX	14:12	0x8	54mA
DCDC_ILIM_MIN	11:8	0x4	30mA

The current limit values in Table 9 are set in the SDK and will fit in most use cases. In general, the recommendation is to leave the current limit values as is, since the system performance is verified with these settings. In special cases, the user can adjust the settings to fit the needs of the application. Note however, that changes in these settings may affect system performance.

3.2.2 XTAL, 32 MHz (Y1)

The main clock of the DA14531 SoC is 16 MHz, which is generated from a 32 MHz crystal oscillator. The crystal oscillator consists of an external 32 MHz XTAL and the internal clock oscillator. The recommended operating conditions are given in Table 10.

Table 10: XTAL32 MHz Oscillator - Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
fXTAL_32M	crystal oscillator frequency			32		MHz
ΔfXTAL	crystal frequency tolerance	After optional trimming; including aging and temperature drift. Note 1	-20		20	ppm
ΔfXTAL_UNT	crystal frequency tolerance	Untrimmed; including aging and temperature drift. Note 2	-40		40	ppm
ESR_1	equivalent series resistance	C0=3pF			100	Ω
ESR_2	equivalent series resistance	C0=5pF			60	Ω
C0_1	shunt capacitance	ESR=100Ω			3	pF
C0_2	shunt capacitance	ESR=60Ω			5	pF
CL	load capacitance	No external capacitors are required	4	6	8	pF

Note 1 With the use of the internal varicaps there is the possibility to trim a wide range of crystals to the required tolerance.

Note 2 Maximum allowed frequency tolerance for compensation by the internal varicap trimming mechanism.

If the specification of the crystal meets the requirements of the DA14531 oscillator, the crystal package does not affect the operation of the system. Several crystals are tested successfully. A short list can be found in Table 11.

Table 11: Successfully Tested Crystals

Part number	Provider	Package
XRCGB32M000F1H00R0	Murata	2.0 mm x 1.6 mm
8Q32070005	TXC	1.6 mm x 1.2 mm
TZ3484B	Taisaw	1.6 mm x 1.2 mm
TZ3375C	Taisaw	2.0 mm x 1.6 mm
8J32070002	TXC	1.2 mm x 1.0 mm

The selected crystal for the DA14531 PRO-devkit is the XRCGB32M000F1H00R0 of Murata. The XTAL specification is presented in Table 12.

Table 12: Selected Main XTAL Specification

Parameter	Description	Min	Typ	Max	Unit
Frequency	Fo		32		MHz
Operating Temperature Range	Top	-30		85	°C
Load Capacitance	CL		6		pF
Drive Level	DL		150	300	µW
Equivalent Series Resistance	ESR			60	Ω
Frequency Tolerance	dF/Fo	-10		10	ppm
Frequency shift by Temperature	dF/F25	-10		10	ppm
Aging	dF/F25	-2		2	ppm
Package	2.0x1.6 mm				mm × mm

3.2.2.1 32 MHz XTAL Trimming

The 32 MHz (XTAL32M) crystal oscillator has trimming capability. The frequency is trimmed by two on-chip variable capacitor banks. See Figure 17. Both capacitor banks are controlled by the same 8-bit register, CLK_FREQ_TRIM_REG.

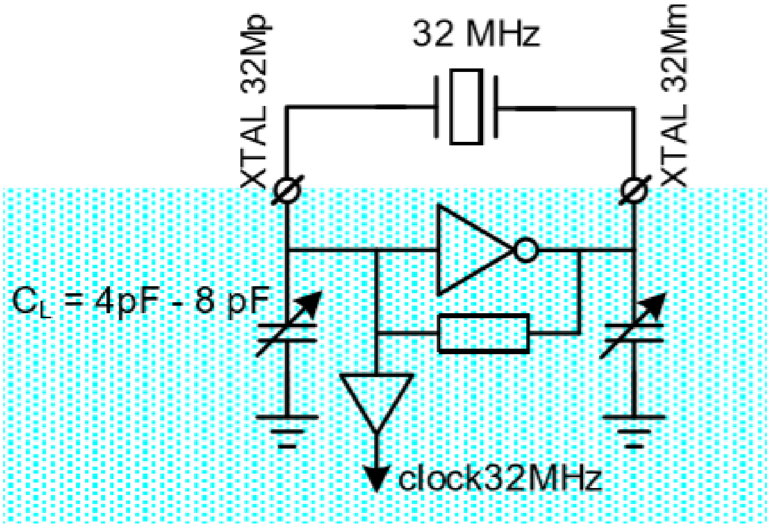


Figure 17: The Circuit of 32 MHz Crystal Oscillator

With CLK_FREQ_TRIM_REG[XTAL32M_TRIM] = 0x00, the minimum capacitance and thus the maximum frequency is selected.

With CLK_FREQ_TRIM_REG[XTAL32M_TRIM] = 0xFF, the maximum capacitance and thus the minimum frequency is selected.

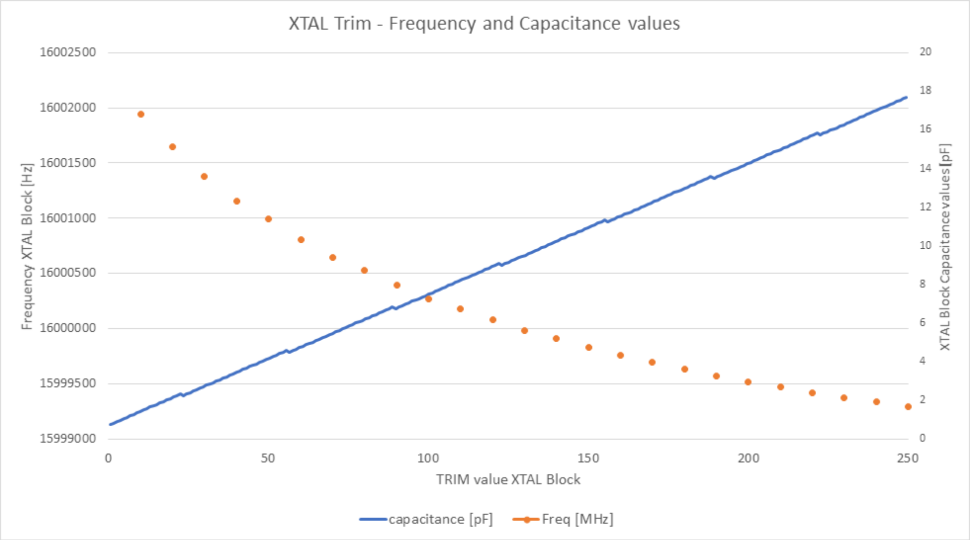


Figure 18: 32 MHz XTAL Oscillator Capacitance Value Versus Frequency

The advice is to trim the crystal (XTAL) to achieve optimal RF performance and power consumption.

Not trimming the crystal might lead to out of spec RF, when taking frequency drift into account due to temperature and aging.

Crystal trimming is fully supported by the PLT [2], without the need for external equipment or can be performed manually.

Crystal Trimming is an iterative algorithm:

1. Set the TRIM-value.
2. Measure the resulting frequency.
3. Adapt the TRIM value until Delta < 5 ppm.

3.2.2.2 Low loss XTALs

The default current and amplitude settings of the XTAL oscillator are optimized for standard XTALs matching the datasheet's specification.
If a low loss XTAL is used, which has a low shunt capacitance (C0<1pF) and a low equivalent series resistance ESR, the default oscillator settings might lead to an interruption of oscillation.
To prevent this, please use the following settings when using a low loss XTAL.

XTAL32M_CTRL0_REG: CORE_CUR_SET = 1
XTAL32M_CTRL0_REG: CORE_AMPL_TRIM = 5

To achieve this, the SDK must be adapted.
Please add a #define LOW_ESR_C0_XTAL in DA1458x_advanced_config.h file to distinguish between a standard XTAL and a low loss one.

Then change system_init() in arch_system.c and arch_hibernation_restore() in arch_hibernation.c like this:

Replace:

```
SetBits16(XTAL32M_CTRL0_REG, CORE_CUR_SET, 2);
```

With:

```
#ifdef LOW_ESR_C0_XTAL
   SetBits16(XTAL32M_CTRL0_REG, CORE_CUR_SET, 1);
   SetBits16(XTAL32M_CTRL0_REG, CORE_AMPL_TRIM, 5);
#else
   SetBits16(XTAL32M_CTRL0_REG, CORE_CUR_SET, 2);
#endif
```

Additionally, make sure not to set the CLK_FREQ_TRIM_REG to 0x0 before going to sleep. Please replace in arch_main.c

```
SetWord16(CLK_FREQ_TRIM_REG, 0);                    // Set zero value to CLK_FREQ_TRIM_REG
```

With:

```
#ifndef LOW_ESR_C0_XTAL

   SetWord16(CLK_FREQ_TRIM_REG, 0);      // Set zero value to CLK_FREQ_TRIM_REG
#endif
```

3.2.3 XTAL, 32.768 kHz (Y2)

Users can put an external crystal of 32.768 kHz on pins P0_3 and P0_4 of DA14531 (external digital clock can also be applied on pin P0_3).

This XTAL oscillator does not have varicap tuning, so the frequency accuracy of this clock will depend on the selected component. Select a crystal that matches the specification given in Table 14, or matches the crystal with external load capacitance. The recommended operating conditions for the 32.768 kHz crystal oscillator are given in Table 13.

Table 13: XTAL Oscillator 32kHz - Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
fXTAL_32M	crystal oscillator frequency		30	32.768	35	kHz
ESR	equivalent series resistance				100	KΩ
CL	load capacitance	No external capacitors are required for a 6pF or 7pF crystal	6	7	9	pF
C0	shunt capacitance			1	2	pF
PDRV_MAX	maximum drive power		0.1			µW
ΔfXTAL	crystal frequency tolerance (including aging)	Timing accuracy is dominated by crystal accuracy. A much smaller value is dominated	-250		250	ppm

A crystal that can be used is the SC20S-7PF20PPM of SEIKO Instruments. The specification is given in Table 14.

Table 14: Selected Main XTAL Specification

Parameter	Description	Min	Typ	Max	Unit
Frequency	Fo		32.768		KHz
Operating Temperature Range	Top	-40		+85	°C
Load Capacitance	CL		7		pF
Equivalent Series Resistance	ESR			90	KΩ
Shunt Capacitance	Co		1.3		pF
Frequency Tolerance	dF/Fo	-20		+20	ppm
Aging, per year	dF/F25		±3		ppm
Drive Level	DL		0.1	1	µW
Package	2.05 x 1.2 x 0.6				mm

Notice: There is no 32.768 kHz crystal used on the DA14531 PRO-development kit. An internal RCX oscillator is used instead.

In most applications the DA14531 can run with good accuracy with its internal RC oscillator (RCX) and therefore the XTAL32k is not needed. For applications with more demanding accuracy/drift characteristics, such as timekeeping, consider using the XTAL32k.

3.2.4 Reset

During power on and before booting, the reset pin is active high, and is assigned on P0_0. This is the HW reset. After boot, reset pin assignment and operation is handled by software.

At boot, P0_0 is also assigned as output to UART and SPI for the time required from each booting step. At the end of each boot step, P0_0 is assigned again to Reset.

Table 15: P0_0 Assignment During Boot

pin	Booting Sequence	State	Comments
P0_0	Before boot	RST	Input with pull down
	During boot	MISO, (Boot Step 1) UTX, (Boot Step 4) MOSI. (Boot Step 5) RST	P0_0 is handled from Booting sequence. At the end of each step, and before next booting step, P0_0 is assigned to Reset
	After boot	GPIO	Handled by the software.

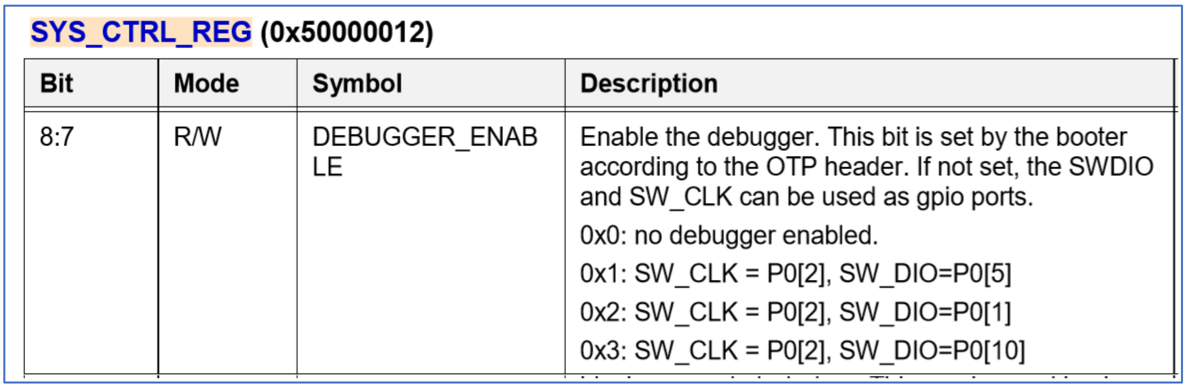
The RST functionality on P0_0 can be disabled by setting the HWR_CTRL_REG[DISABLE_HWR] bit.

3.2.5 JTAG

JTAG consists of SWDIO and SWCLK. In the WLCSP17 package, SWCLK and SWDIO are assigned to P0_2 and P0_5. For FCQFN24 devices, SWCLK is assigned to P0_2 and SWDIO is assigned to P0_10. But through software programming, SWDIO can also be assigned to P0_1.

During the booting sequence, JTAG is not enabled. If no bootable device is found on any of the serial interfaces, the booter can do two things depending on what was stored in the Configuration Script (CS). If the 'Debugger disable' (0x70000000) command is stored in the CS, the booter will start rescanning the peripherals. Otherwise it will enter an endless loop with the debugger (JTAG) being enabled.

To use the JTAG GPIOs as general-purpose pins, the JTAG function must be disabled by clearing the 'debugger enable' bits. See Figure 19. The same bits can be used to remap the JTAG pins.



SYS_CTRL_REG (0x50000012)

Bit	Mode	Symbol	Description
8:7	R/W	DEBUGGER_ENABLE	Enable the debugger. This bit is set by the booter according to the OTP header. If not set, the SWDIO and SW_CLK can be used as gpio ports. 0x0: no debugger enabled. 0x1: SW_CLK = P0[2], SW_DIO=P0[5] 0x2: SW_CLK = P0[2], SW_DIO=P0[1] 0x3: SW_CLK = P0[2], SW_DIO=P0[10]

Figure 19: Debugger Enabling

3.2.6 UART

There are three different UART configurations possible: 1-wire UART (preferable due to low pin number), 2-wire UART and 4-wire UART.

UART, Single-wire: UTX and URX are multiplexed together on a single pin of DA14531. On board level, a 1 kΩ resistor separates the two signals. See Figure 20.

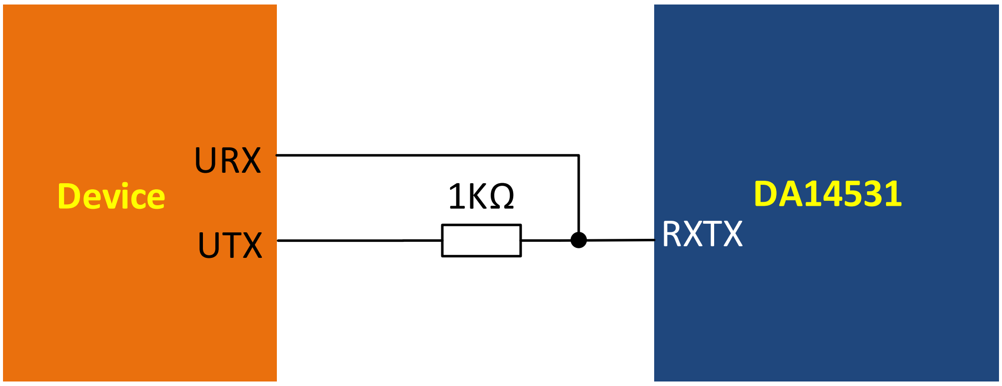


Figure 20: Single UART Hardware Configuration

In a regular UART bus, UTX and URX lines can be active simultaneously. In most use cases of the DA14531 (boot, HCI commands etc.), the traffic on the UART is half duplex and a single wire can be used for all UART transactions. On the DA14531 side, the SDK UART driver takes care of switching the pin direction.

On the host side, all data sent will be echoed back since Tx and Rx are shorted. For successful communication, the software should be able to discard the echo. Smart Snippets Toolbox implements such a feature and can be used with a 1-wire UART.

Single-wire UART is used on the booter. The DA14531 has two options to boot from single-wire UART: from P0_5 in boot step #2 and from P0_3 in boot step #3.
After the boot sequence, the application software can redefine any GPIO as single-wire UART.

UART, 2-wires: UTX and URX.

Two-wire UART is used in boot step #4. P0_0 and P0_1 are used for UTX (output) and URX (input) respectively.

After boot, the software can reassign the UTX and URX to other pins by setting the Pxx_MODE_REG.

UART, 4 wires: This is the full UART with flow control. Set the Pxx_MODE_REG to assign GPIOs. Hardware flow control is mainly needed for external host applications.

3.2.7 SPI Data Flash

There are two available SPI modes on DA14531, Ext-SPI master and Ext-SPI slave. In the Ext-SPI master mode, an external processor (master) can download code to the DA14531. In the Ext-SPI slave, the DA14531 can download code from a slave device such as an external SPI data Flash.

In this case, the bootloader will download the binary file to RAM and execute it. The default GPIOs during boot are given in Table 16.

Table 16: DA14531 Pins Assignment for SPI Data Slave on Booting

DA14531 Signals	SPI Data Flash
P0_0	MOSI
P0_1	CS
P0_3	MISO
P0_4	SCK

Booting GPIOs can be changed by either a secondary bootloader, or by declaring them in the OTP header boot-specific mapping.

Data flashes tested successfully are listed in AN-B-088 DA145xx Flash Selector Guide.

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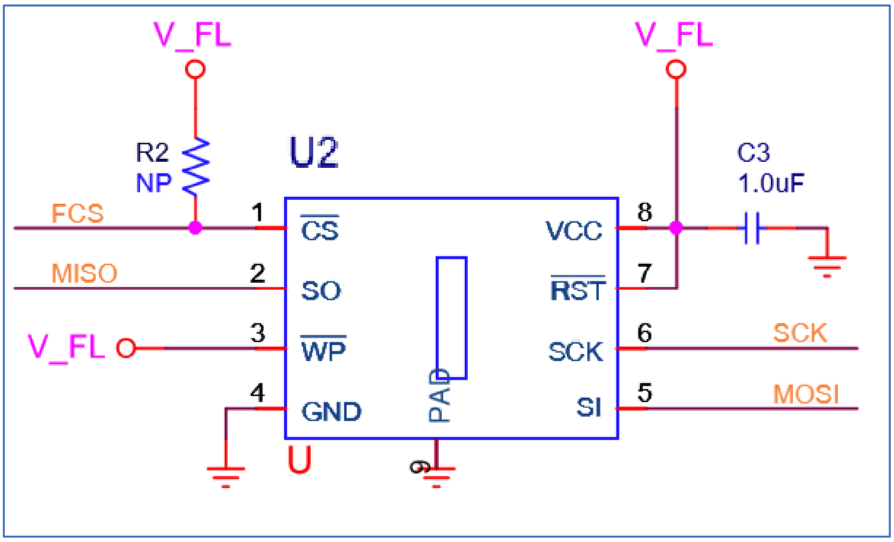

Figure 21: SPI Data Flash Hardware Setup

The SPI clock (SCK) frequency is configurable up to 32 MHz. Please note that the frequency depends on the physical connections between the DA14531 SoC and the SPI Data flash. On DA14531 DK-PRO, there is significant capacitive load on the SPI pins, due to signal multiplexing and long traces. On the software development kit (SDK), the frequency used is 2 MHz to boot and 4 MHz for SUOTA.

PCB Layout Notice

The SPI data flash Read / Write frequency depends on the PCB layout. The suggestion is to put the data flash as close as possible to the DA14531. In case that this is not feasible, consider adding termination resistors in the order of 30 Ω next to source pins. Add GND between routed traces to eliminate crosstalk.

3.3 RF Section

DA14531 provides a 50 Ω single RFIO port for Tx and Rx without requiring external balun or RF switch. The internal RF power amplifier provides Tx RF power from -19.5 dBm to +2.5 dBm.

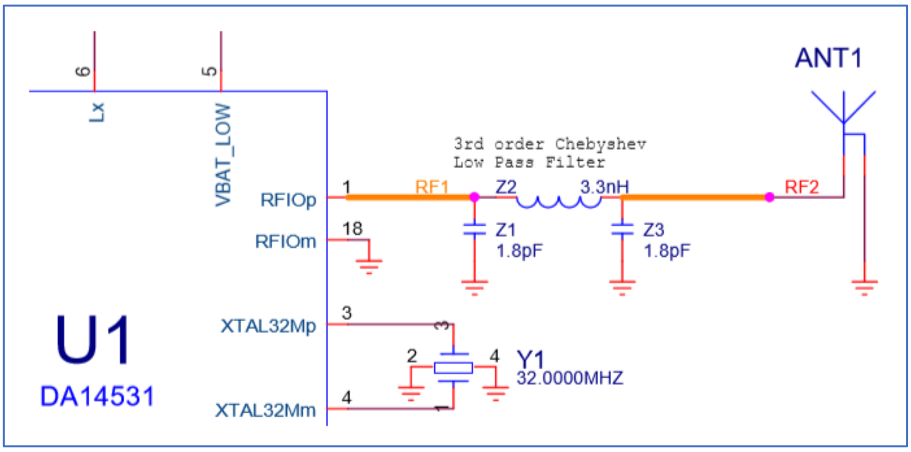

Figure 22: DA14531 RF Section

The Pi filter for Dialog Semiconductor's DA14531 System-on-Ship (SoC) in 2.4 GHz Bluetooth low energy applications specifically addresses the conducted and radiated performance.

The objective of the Pi-filter is to suppress the local oscillator leakage, which violates the conducted performance requirements of ETSI, ARIB (Japanese standard) and KC (Korean certification) standards.

There is no violation of FCC regulations. Consequently, the user can omit the Pi-filter if only the FCC regulations must be adhered to.

The Pi filter configuration is chosen, because it gives the best suppression with minimal power loss at fundamental frequencies. The filter is a 3rd order Chebyshev Lowpass Filter with a cut-off frequency at 2600 MHz, and passband ripple of 0.4 dB.

3.3.1 Pi Filter

The filter topology is shown in Figure 23.

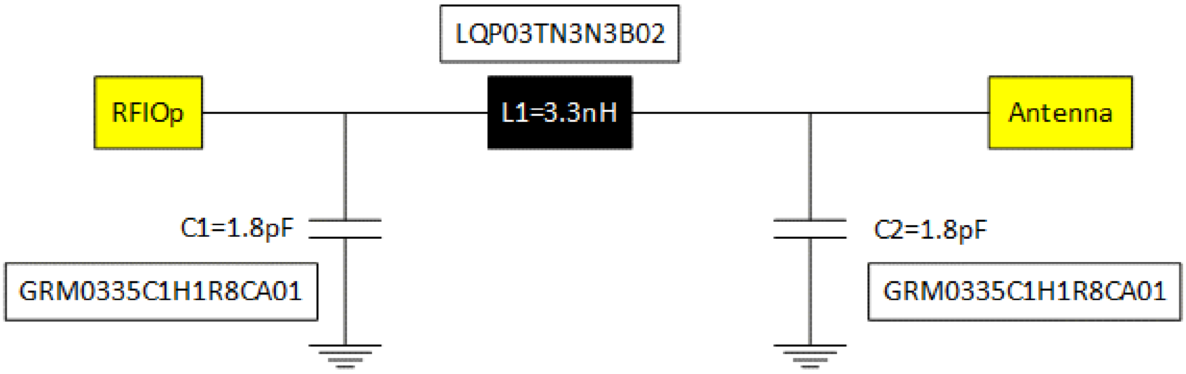

Figure 23: Pi Filter Topology

Components used:

- Capacitors: 1.8 pF, 0201, Murata, PN: GRM0335C1H1R8CA01
- Inductor: 3.3 nH, 0201, Murata, PN: LQP03TN3N3B02

Measured S21 parameters give a minimum -15 dBm attenuation at 4.8 GHz. The filter is giving a 0.7 dBm to 1.2 dBm loss in sensitivity and 0.2 to 0.7 dBm in Tx power.

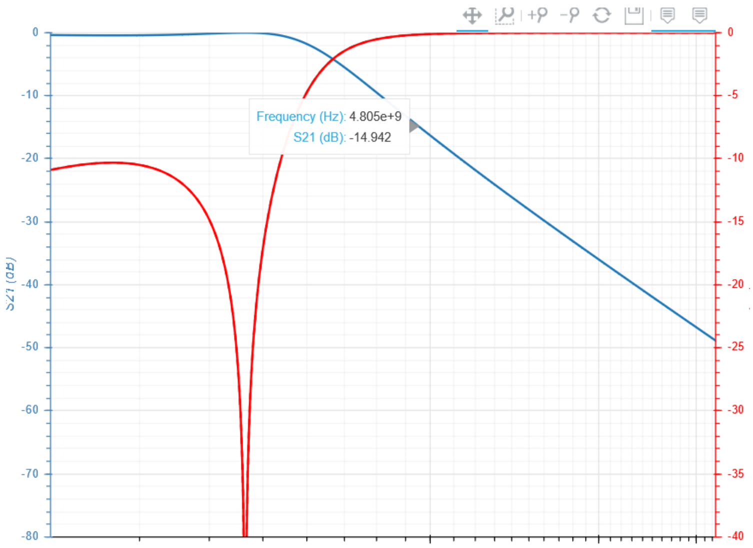

Figure 24. S21 Simulated Parameters

3.3.2 Conducted Performance

The measurements are done with a calibrated spectrum analyzer and RF cables. The levels are measured at the SMA output with the DUT.

All measurements are calibrated for cable losses.

3.3.2.1 TX Measurements

The test was done at ch19, room temperature, normal operating conditions. Measurements are done in burst mode, modulated signal.

Table 17: Fundamental Power and Harmonics, Conducted Mode, PA in 3 dBm Mode

	Fundamental	2nd harm	3rd harm	4th harm	5th harm
Without RFIO filter	2.54	-39.49	-43.95	-48.62	-38.03
With RFIO filter	1.81	-56.80	-62.72	-64.04	-55.06

Note 1 All values are in dBm

Note 2 Measurement accuracy < ± 0.3 dB

3.3.2.2 RX Measurements

The test was done at ch19, measurement frequency 2*2440+1 MHz = 4881 MHz.

Table 18: LO Leakage, Conducted Mode Results

	Without RFIO filter	With RFIO filter
LO leakage power	-41.3	-58.78

Note 1 All values are in dBm

Note 2 Measurement accuracy < ± 0.3 dB

3.3.3 Antenna and Current Measurements

The antenna’s transmit power is received from the RF circuitry through the Tx line (matched to an impedance of 50 Ω). Matching the input impedance of the antenna to 50 Ω is required, to ensure that the maximum power is transferred from the RF circuity to the antenna with only a negligible amount being reflected.

However, the matching circuits are not always perfect and the components present tolerances.

Also, if a printed antenna is in contact or close to other surfaces (especially conductive materials), it is detuned, and a lot of RF energy is not radiated, but reflected back to the RF transmitter.

Peak current measurements depend on the antenna matching. A not perfectly matched antenna results in a higher power consumption during RF transmission.

The safest way to measure the peak power consumption of the system (hardware and software) is to have instead of the antenna a 50 Ω termination (dummy load).

4 PCB Layout Guidelines

PCB guidelines for the DA14531 are presented below, using the daughterboards of the PRO-Devkit as reference:

- FCGQFN24: DA14531-00FXDB-P _ [376-04-F]
- WLCSP17: DA14531-00OGDB -P_ [376-05-E]

4.1 PCB Layout of DA14531-00FXDB-P PRO-Devkit-(FCGQFN24)

The implemented PCB layout is based on the schematic shown in Figure 25. The same layout can be used for buck, boost and bypass configurations (for bypass, L1 must be removed from the circuit).

A low-pass filter has been added on the RFIOp trace, which presents impedance on both sides, equal to 50 Ohm. The antenna is not shown in the schematic in Figure 25.

Finally, please notice that Y2, 32.768 kHz can be omitted.

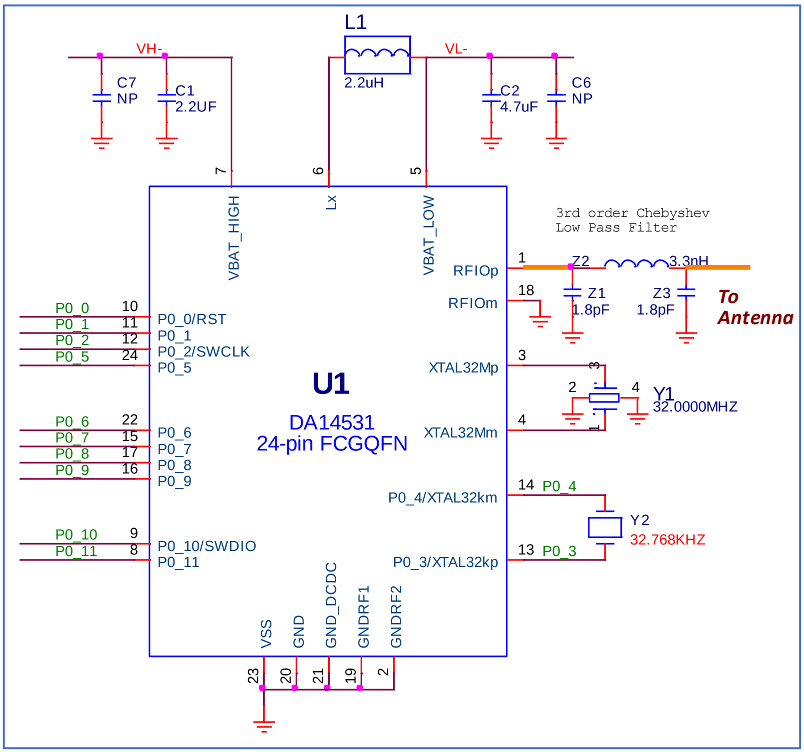

Figure 25: DA14531 FCGQFN24 Reference Circuit

PCB rules applied on the PRO-Daughterboard:

- Number of layers: 4
- Material: FR-4 – no microvias
- Vias: Mechanical
  - Under chip: Diameter 0.45 mm / drill 0.15 mm
  - Rest PCB areas: Diameter 0.5 mm / drill 0.15 mm
- Copper clearance: 0.1 mm
- Copper width: 0.1 mm

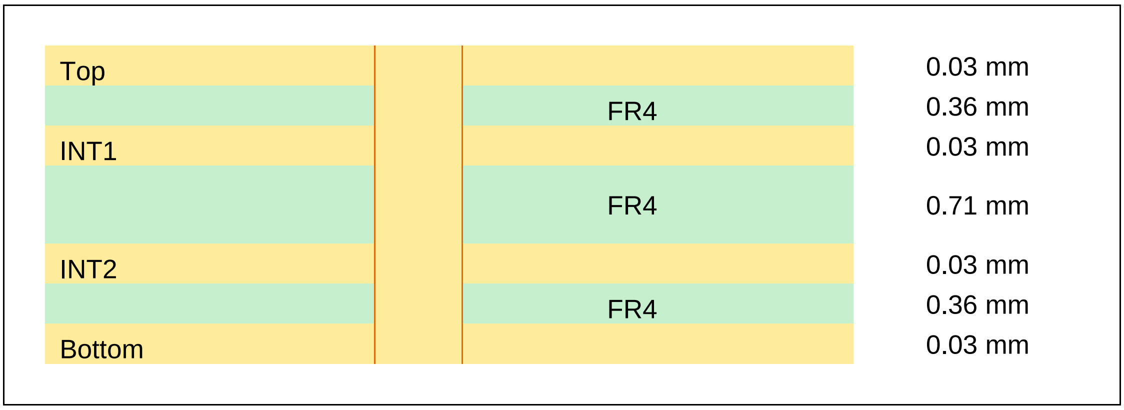

Figure 26: PCB Cross Section

PCB Layout guidelines

Grounding

- Use INT1 layer free of routing and assign it as reference ground
- Separate RF ground pins of DA14531 CFGQFN24 from the rest ground pins
- Connect pin 19 to GND with vias as shown in Figure 27
- Short 20, 21, 23 GND pins together and use two GND vias, as shown in Figure 27
- Add GND stitching vias to increase the performance of the system

Power management

- Put capacitors C1 and C2 close to the pins of DA14531. Apply a GND via per capacitor next to the GND pin
- Put L1 as close as possible to the chip. Remove grounding under the inductor to minimize any possible coupling from reference ground

XTALs

- Put XTALs close to the chip
- Try to have a ground shield around XTALs
- There is no need to route the two XTAL traces differentially

Remove the area on the INT1 ground layer under the pads of XTAL to reduce coupling as shown in Figure 28. Use the 3rd or 4th layer to shield the xtal pads.

RF strip

Calculate and route a 50 Ohm RF stripline between DA14531 RFIOp pin and antenna. A low-pass filter, consisting of three components (Z1, Z2, Z3) must be put as close as possible to the chip. Both capacitors must be grounded on the same side of the RF stripline preferably to RFIOm, which is the RF reference ground.

In case the antenna needs matching, put a matching circuit next to the antenna. Please ground the components on the same side of RF stripline, same as in the low-pass filter.

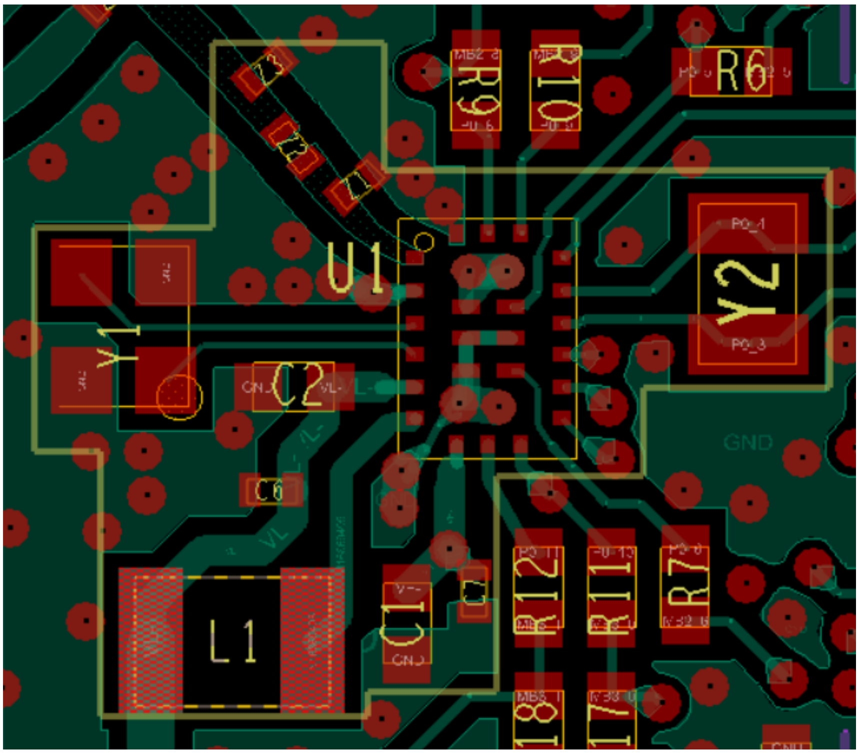

Figure 27: PCB Placement and Routing – Top Layer

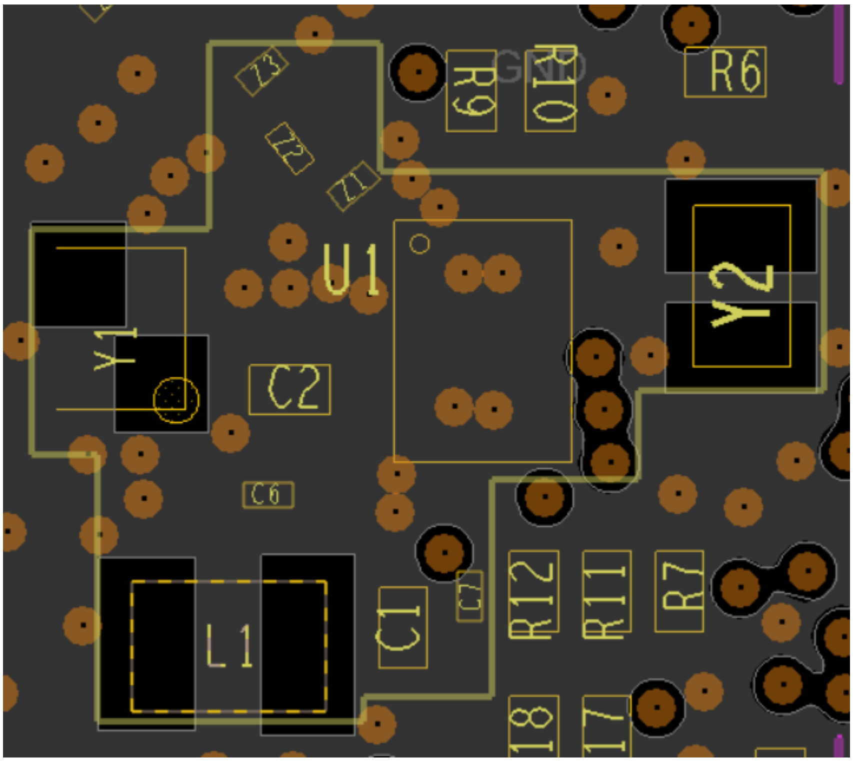

Figure 28: FCGQFN24 PCB Placement and Routing – GND Plane - INT1 Layer

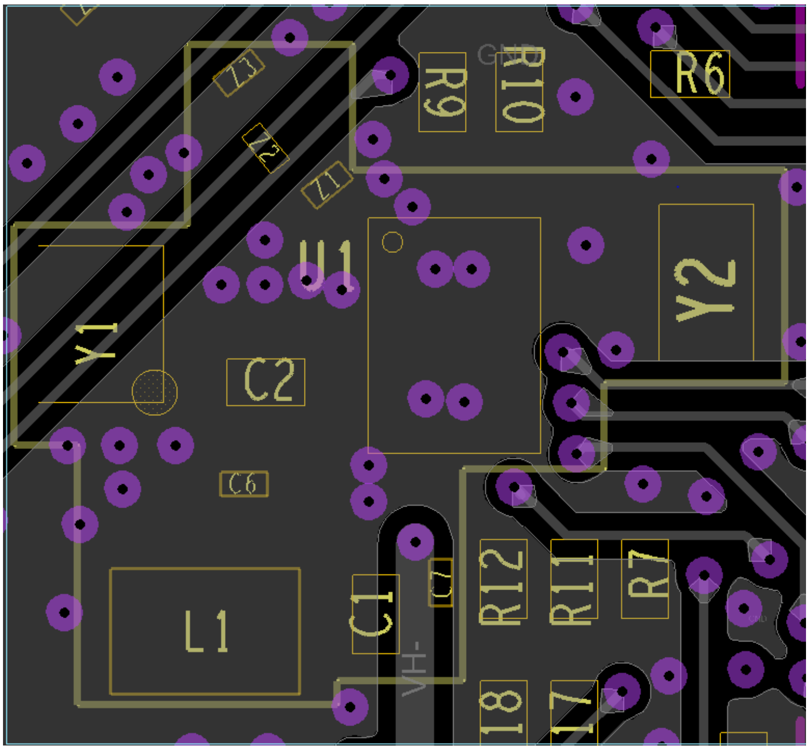

Figure 29: FCGQFN24 PCB Placement and Routing – INT2 Layer

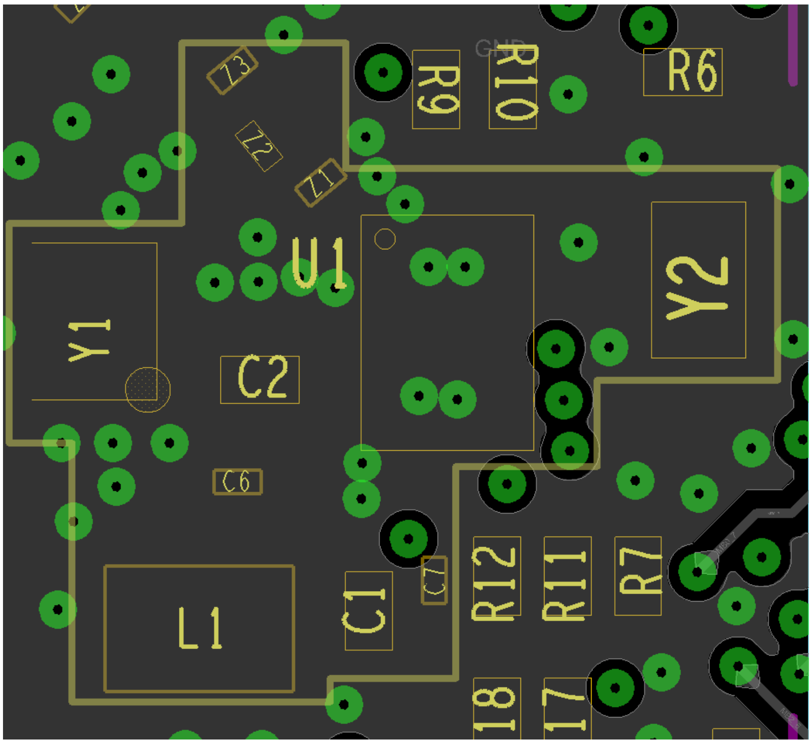

Figure 30: FCGQFN24 PCB Placement and Routing – GND Bottom Layer

4.1.1 Minimal System PCB Layout for FCQFN24

An example of the PCB layout occupied from the DA14531 system is given in Figure 31. This is for the FCQFN24.

The implemented system uses the necessary components. Please note that crystal 32 kHz is omitted. The inductor is the same as on the Pro-Devkit whereas all signals are fanned out. Component placement is much more efficient than the PRO-development kit, as there is no need for signals multiplexing. Dimensions of the area are 5.8 mm x 7.6 mm.

The PCB can be either 2 layers or 4 layers. For a two layer design, please close the openings under the xtal pads on the 2nd layer.

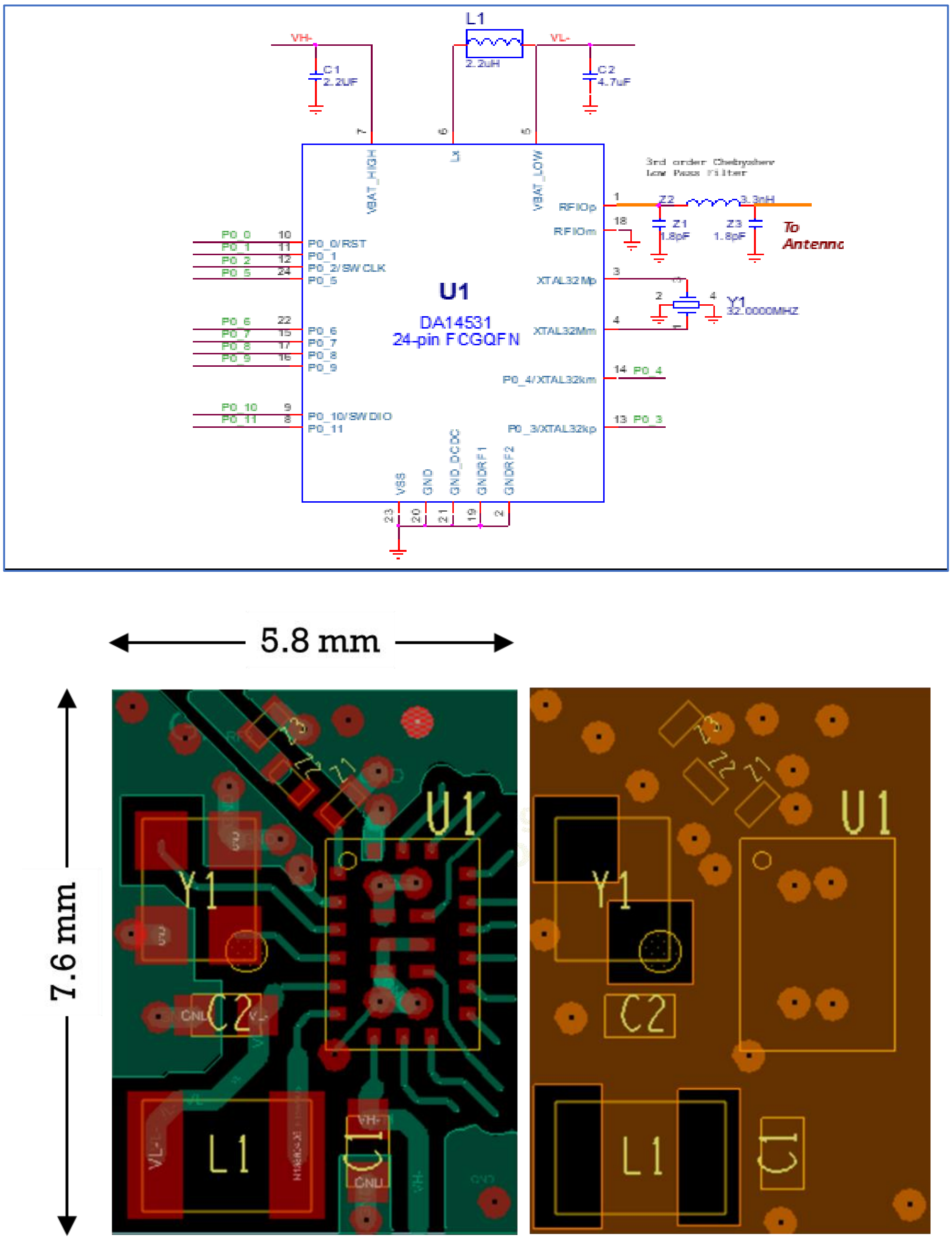

Figure 31: PCB Occupied Area for DA14531-FCGQFN24 System,
(above: the schematic; below: right the top layer and left, the INT1 layer)

4.2 PCB Layout of DA14531-0 OGDB-P PRO-Devkit (WLCSP)

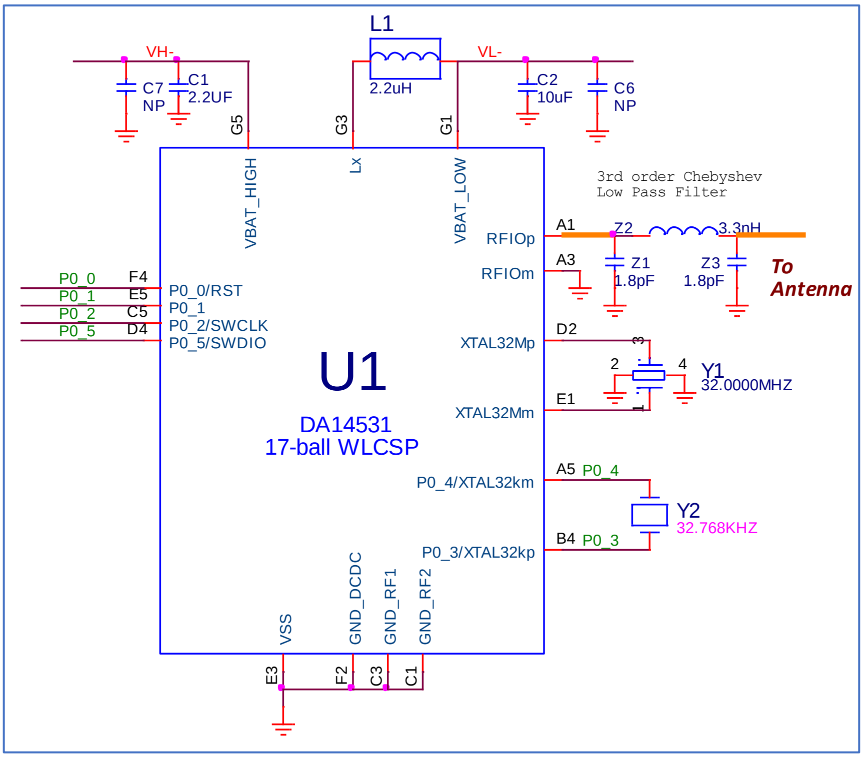

Figure 32: DA14531 WLCSP17 Reference Circuit

PCB rules applied on PRO-Daughterboard:

- Number of layers: 4
- Material: FR-4 – no microvias
- Vias: Mechanical
  - Under chip: no vias
  - Rest PCB areas: Diameter 0.5 mm / drill 0.15 mm
- Copper clearance: 0.1 mm
- Copper width: 0.1 mm

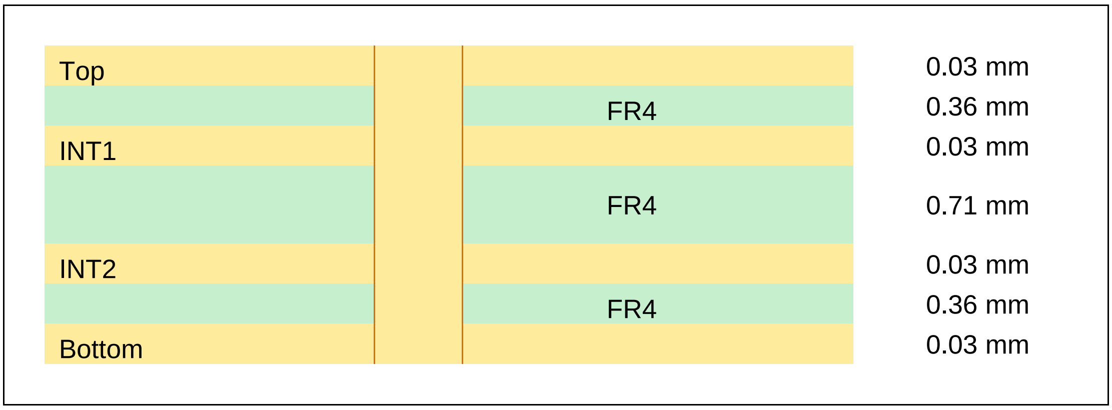

Figure 33: PCB Cross Section

4.2.1 PCB Layout Guidelines

Grounding

- Use INT1 layer free of routing and assign as reference ground
- Separate RF ground pins of DA14531 WLCSP17 from the rest ground pins
- Connect pin A3 to GND with a via as shown in Figure 34
- Short C1, C3, and E3 pins together and use two or more GND vias, as shown in Figure 34
- Add GND stitching vias to increase the performance of the system

Power management

- Put capacitors C1 and C2 close to the pins of DA14531. Apply a GND via per capacitor next to the GND pin
- Put L1 as close as possible to the chip. Remove the grounding under the inductor to minimize possible coupling from the reference ground

XTALs

- Put XTALs close to the chip
- Try to have a ground shield around XTALs
- There is no need to route the two XTAL traces differentially
- Remove the area on the INT1 ground layer under the pads of the XTAL to reduce the coupling as shown in Figure 35

SPI Data Flash: SPI data flash Read / Write speed depends on the PCB layout. The suggestion is to put the data flash as close as possible to the DA14531. If that is not feasible, consider adding termination resistors in the order of 30 Ω next to source pins. Add GND between routed traces to eliminate crosstalk.

RF strip: calculate and route a 50 Ohm RF stripline between the DA14531 RFIOp pin and the antenna. A low-pass filter that consists of three components (Z1, Z2, Z3) must be put as close as possible to the chip. Both capacitors must be grounded on the same side of the RF stripline (RFIOm). See Figure 34.

If the antenna needs matching, put a matching circuit next to antenna. Please ground components on the same side of RF stripline, the same as for the low-pass filter.

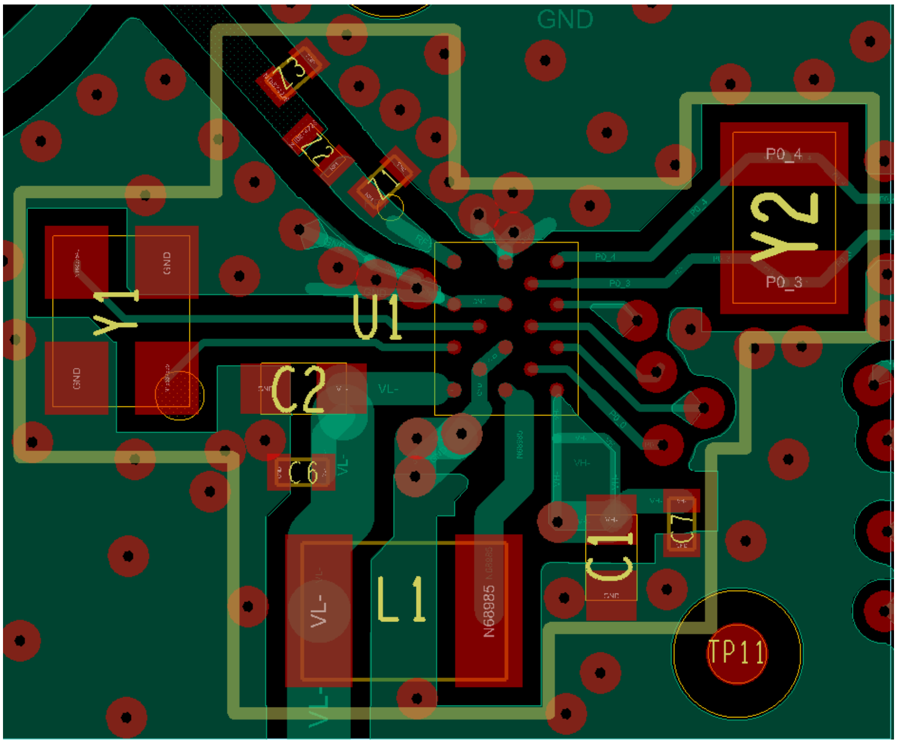

Figure 34: WLCSP17 - PCB Placement and Routing – Top Layer

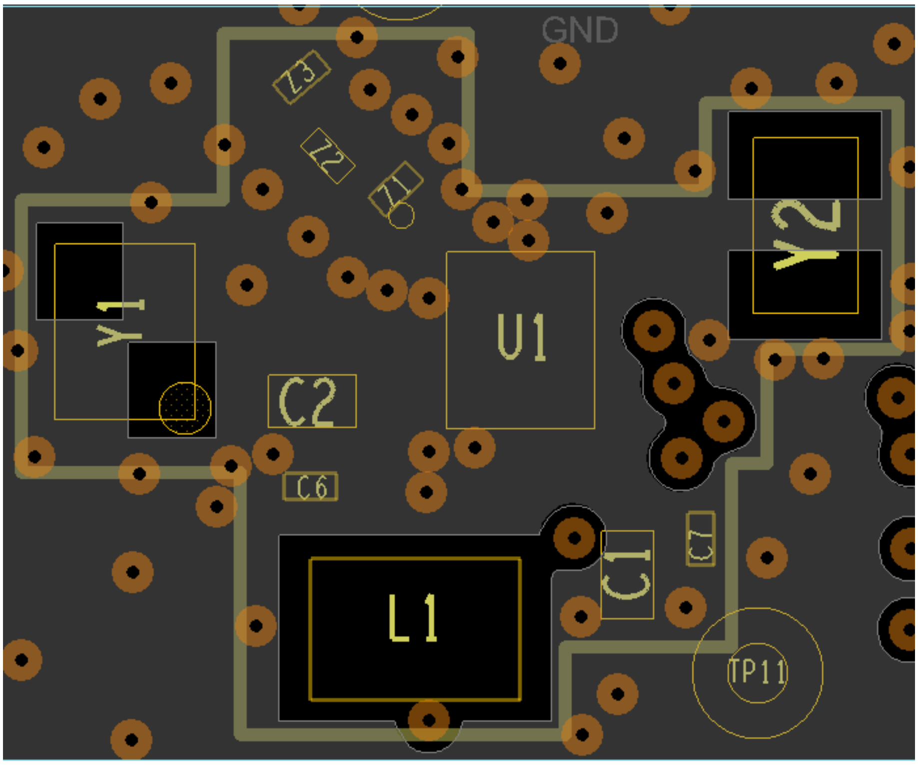

Figure 35: WLCSP17 PCB Placement and Routing – GND plane - INT1 Layer

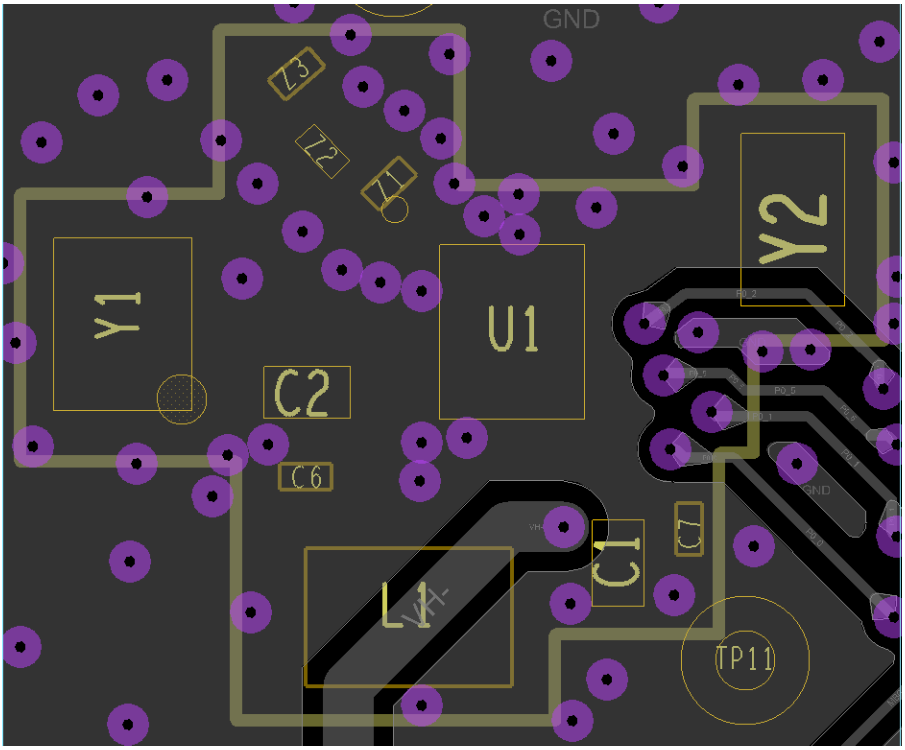

Figure 36: WLCSP17 PCB Placement and Routing - INT2 Layer

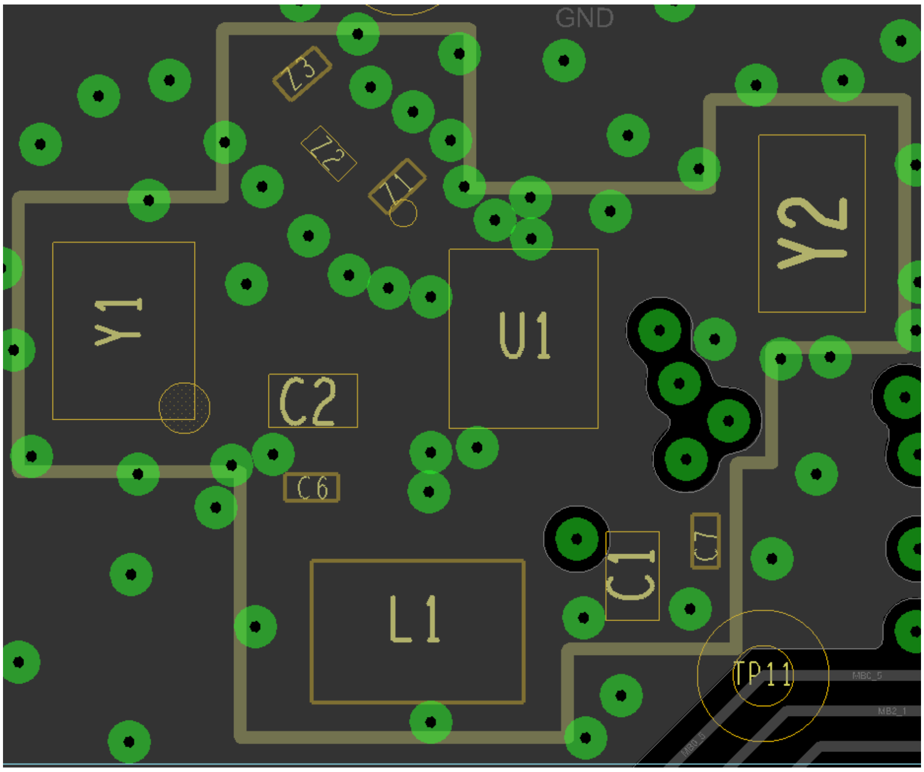

Figure 37: WLCSP17 PCB Placement and Routing – Bottom Layer

4.2.2 Minimal System PCB Layout for WLCSP17

An example of the PCB layout occupied from the DA14531 – WLCSP17 system is shown in Figure 38.

The crystal 32 kHz is omitted. The inductor is the same as on the Pro-Devkit, whereas all signals are fanned out. Components are much more efficiently positioned in comparison to PRO-development daughterboard as there is no signal multiplexing. Dimensions of the area are 5.2 mm x 7.4 mm. The PCB can be either 2 layers or 4 layers. For a two layer design, please close the openings under the xtal pads on the 2nd layer.

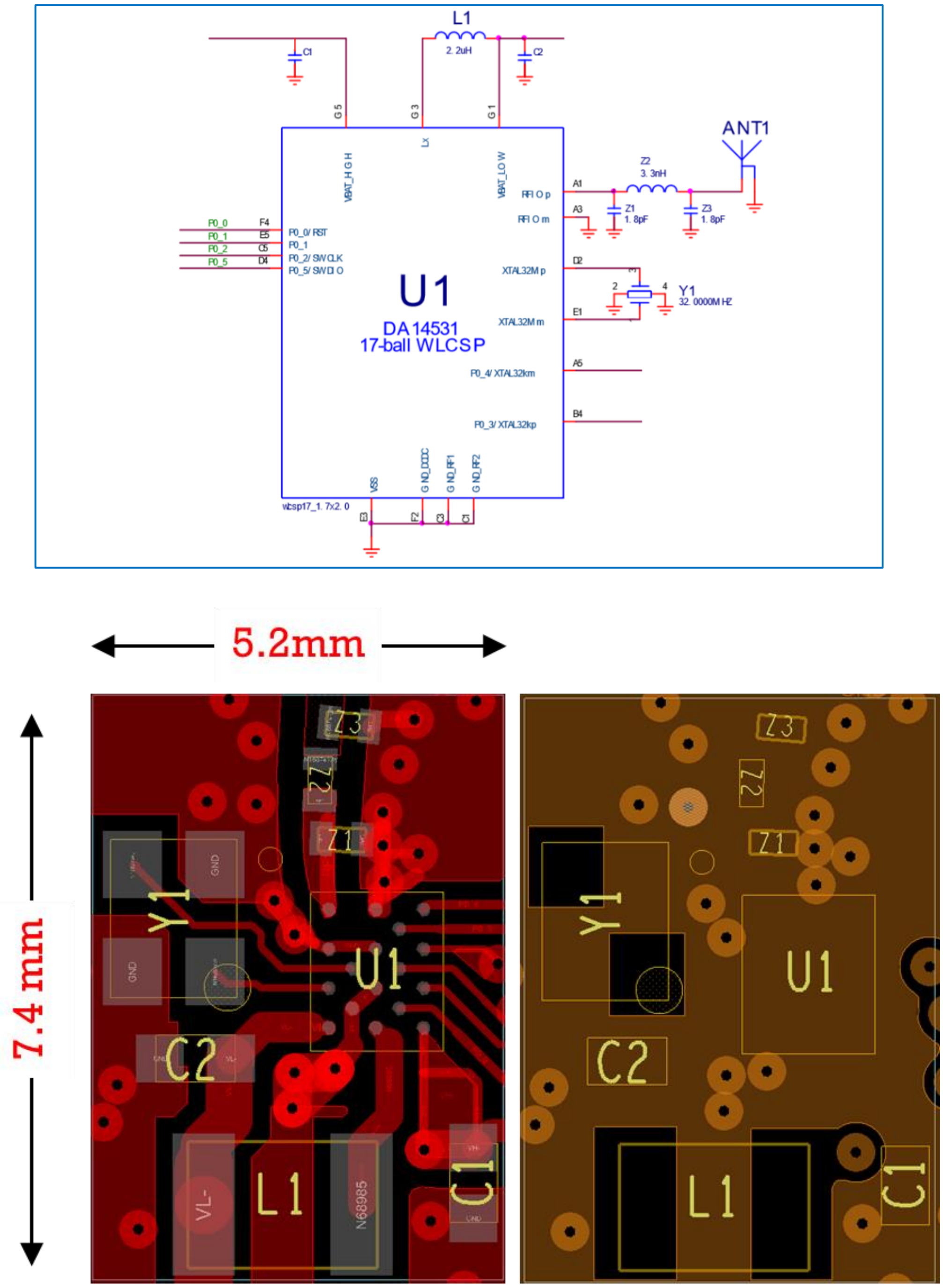

Figure 38: PCB Occupied Area for DA14531-WLCSP17 System

(above: the schematic; below: right the top layer and left, the INT1 layer)

Revision History

Revision	Date	Description
1.4	15-OCT-2020	Low loss XTALs added. DA14530 note added. Editorial changes
1.3	18-Mar-2020	POR voltage levels changed
1.2	31-Oct-2019	Small updates, removed Draft status, and finalized.
1.1	29-Oct-2019	Editorial review.
1.0	23-Oct-2019	Initial version

Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

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Contacting Dialog Semiconductor

United Kingdom (Headquarters)
Dialog Semiconductor (UK) LTD
Phone: +44 1793 757700

Germany
Dialog Semiconductor GmbH
Phone: +49 7021 805-0

The Netherlands
Dialog Semiconductor B.V.
Phone: +31 73 640 8822

Email:
enquiry@diasemi.com

North America
Dialog Semiconductor Inc.
Phone: +1 408 845 8500

Japan
Dialog Semiconductor K. K.
Phone: +81 3 5769 5100

Taiwan
Dialog Semiconductor Taiwan
Phone: +886 281 786 222

Web site:
www.dialog-semiconductor.com

Hong Kong
Dialog Semiconductor Hong Kong
Phone: +852 2607 4271

Korea
Dialog Semiconductor Korea
Phone: +82 2 3469 8200

China (Shenzhen)
Dialog Semiconductor China
Phone: +86 755 2981 3669

China (Shanghai)
Dialog Semiconductor China
Phone: +86 21 5424 9058