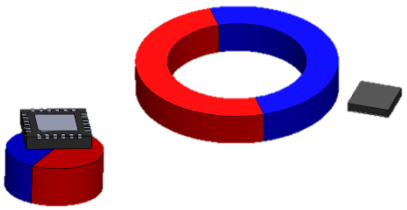
AEAT-9922-Q24

Magnetic Encoder IC
10-Bit to 18-Bit Programmable Angular Magnetic Encoder

Application Note



Description

AEAT-9922-Q24 is a CMOS magnetic sensor structure suitable for contactless 360° encoding based on the Hall Effect. It provides an angle output up to 18 bits of resolution and simultaneous incremental output of up to 10000 CPR. An integrated Hall structure at the core of the device uses a single 2-pole disc or ring magnet to convert the magnetic field vector in the chip plane into an AC signal whose amplitude and phase correspond to the magnitude and direction of the field.

An internal digital signal-processing unit then processes and conditions the raw AC signal from the sensor. The output signals are available in three different forms:

- Pulse Width Modulation (PWM)
- Absolute 18-bit position through the 3 wire ,2 wire Serial Synchronous Interface (SSI) and 4 wire Serial Protocol Interface (SPI)
- Incremental output (ABI and UVW signals)

These features can be programmed by configuring the internal registers in program mode.

More information about the product specifications of AEAT-9922-Q24 is available in the product data sheet.

Operation Mode

The AEAT-9922-Q24 features two types of operational modes that are normal operation mode and configuration mode.

Normal Operation Mode

The Normal mode is the normal operating mode of the chip. The absolute output (10-bit to 18-bit absolute position data) is available through serial protocol pin (M0, M1, M2 and M3). The following are the output signal conditions during AEAT-9922-Q24 initialization:

- PWM signals all 0s.
- ABI signals all 1s.
- UVW signals all 0s.

The incremental positions are indicated on ABI and UVW signals with user-configurable CPR from 0 to 10000 of ABI signals and pole pairs from 1 to 32 (2 to 64 poles) for UVW commutation signals.

Configuration Mode

AEAT-9922-Q24 has a built-in memory for multiple-time programming (MTP).

Programming of AEAT-9922-Q24 can be performed with the HEDS-9922 programming kit or any tester/programmer device using the guidelines provided.

Absolute and Incremental Programming

The absolute resolution can be set to 10, 11, 12, 13, 14, 15, 16, 17 or 18 bits. For incremental selection, ABI or UVW can be selected by following the instructions in the following sections. The PWM output is available as well.

The shadow registers are programmable using the SPI protocol. Writing specific commands to specific addresses of the internal registers will program values of shadow registers to memory. The memory can be program multiple-time.

Memory Map

The Broadcom AEAT-9922-Q24 uses nonvolatile EEPROM as shown in the tables that follow. The memory is separated into 32 pages with 8 bits per address. EEPROM programming, can be performed at 3.3V or 5V supply.

Nonvolatile Register (EEPROM)

1. MTP shadow registers are volatile registers that are loaded with corresponding MTP values after power on.
2. All bits (except addresses 0x10, and 0x20–0x27) are in LOCK mode by default after power on. To enter UNLOCK mode (to be able to write to the MTPshadow registers or registers), write 0xAB to address 0x10.
3. In UNLOCK mode, you may write to any MTP shadow registers or registers. Values written will remain until power off.
4. The UNLOCK state is maintained until the power supply is turned off or any value (except 0xAB) is written to address 0x10.

MTP Shadow Registers

1. MTP shadow registers are volatile (upon power up, reload values from EEPROM) and are not written to EEPROM automatically.
2. To write MTP shadow registers values to EEPROM (nonvolatile) memory, see EEPROM Programming section.
3. The MTP shadow registers will be from address 0x10 to 0x27.

The tables that follow show the registers.

Customer Configuration Registers

These registers are available for the users to store any information and configure the encoder as required.

- Address 0x00 to 0x06 is unlocked. User can directly write to these addresses.
- Address 0x08 to 0x0E, is locked. User need to write 8'hAB to address 0x10 to unlock.

Table 1 Customer Reserved Registers

Address	Bit(s)	Name	Description	Default
0x00	[7:0]	Customer Reserve 0	User programmable	8'h0
0x01	[7:0]	Customer Reserve 1	User programmable	8'h0
0x02	[7:0]	Customer Reserve 2	User programmable	8'h0
0x03	[7:0]	Customer Reserve 3	User programmable	8'h0
0x04	[7:0]	Customer Reserve 4	User programmable	8'h0
0x05	[7:0]	Customer Reserve 5	User programmable	8'h0
0x06	[7:0]	Customer Reserve 6	User programmable	8'h0

Table 2 Customer Configuration 0 Registers

Address	Bit(s)	Name	Description	Default
0x07	[7]	Hardware ST Zero	1: Enable external pin 0: Disable external pin	1
	[6]	Hardware Acc Cal	1: Enable external pin 0: Disable external pin	1
	[5]	Axis Mode	1: Off-axis 0: On-axis	0
	[4]	Reserved	0: Reserved	0
	[3:2]	I-Width Setting (ABI)	00: 90 electrical deg (e.deg) 01: 180 electrical deg (e.deg) 10: 270 electrical deg (e.deg) 11: 360 electrical deg (e.deg)	00
	[1:0]	I-Phase Setting (ABI)	00: 90 electrical deg (e.deg) 01: 180 electrical deg (e.deg) 10: 270 electrical deg (e.deg) 11: 360 electrical deg (e.deg)	00

a. Applicable during Off-axis mode only.

Address	Bit(s)	Name	Description	Default
0x08	[7:5]	Hysteresis Setting	000: 0.00 mechanical degree (mº) 001: 0.01 mechanical degree (mº) 010: 0.02 mechanical degree (mº) 011: 0.04 mechanical degree (mº) 100: 0.08 mechanical degree (mº) 101: 0.17 mechanical degree (mº) 110: 0.35 mechanical degree (mº) 111: 0.70 mechanical degree (mº)	100
	[4]	Direction Setting	1: Count up at counterclockwise rotation 0: Count up at clockwise rotation	0
	[3:0]	Absolute Resolution[b]	0000: 18-b absolute resolution (SSI) 0001: 17-b absolute resolution (SSI) 0010: 16-b absolute resolution (SSI) 0011: 15-b absolute resolution (SSI) 0100: 14-b absolute resolution (SSI) 0101: 13-b absolute resolution (SSI) 0110: 12-b absolute resolution (SSI) 0111: 11-b absolute resolution (SSI) 1000: 10-b absolute resolution (SSI) 1001 to 1111 : Reserved	0000

b. Flexible 18-bit Absolute resolution from 10-bit to 18-bit. Combination lower that 10-bit is invalid.

Table 3 Customer Configuration 1 Registers

Address	Bit(s)	Name	Description	Default
0x09	[7:6]	Reserved	00 ~11: Reserved	01
	[5:0]	Incremental Resolution [13:8][c]	00-0000-0000-0000 : 0 CPR (OFF) 00-0000-0000-0001 : 1 CPR 00-0000-0000-0010 : 2 CPR 00-0000-0000-0011 : 3 CPR 00-0000-1000-0000 : 128 CPR 00-0100-0000-0000 : 1024 CPR 10-0000-0000-0000 : 8192 CPR 10-0111-0001-0000 : 10000 CPR 10-0111-0001-0001 : Reserved 11-1111-1111-1111 : Reserved	00000 0000000
0x0A	[7:0]	Incremental Resolution [7:0][c]		

c. Flexible 14-bit Incremental resolution up to 10000CPR. Combination above 10000 is invalid.

Table 4 Customer Configuration 2 Registers

Address	Bit(s)	Name	Description	Default
0x0B	[7]	Reserved	0: Reserved	0
	[6:5]	PSEL Setting[d]	00: SSI3a/SPI4a 01: SSI3b/SPI4b 10: SSI2a/UVW 11: SSI2b/PWM	00
	[4:0]	UVW, PWM Setting[e]	00000: UVW = 1 pole pairs / PWM fixed period = 10bit 00001: UVW = 2 pole pairs / PWM fixed period = 11bit 00010: UVW = 3 pole pairs / PWM fixed period = 12bit 00011: UVW = 4 pole pairs / PWM fixed period = 13bit 00100: UVW = 5 pole pairs / PWM fixed period = 14bit 01000: UVW = 9 pole pairs / PWM fixed clock = 10bit 01001: UVW = 10 pole pairs / PWM fixed clock = 11bit 01010: UVW = 11 pole pairs / PWM fixed clock = 12bit 01011: UVW = 12 pole pairs / PWM fixed clock = 13bit 01100: UVW = 13 pole pairs / PWM fixed clock = 14bit	00000

d. In conjunction with MATS table for Input / Output configuration

e. UVW: Flexible 5-bit UVW resolution up to 32 pole pairs.
PWM: Only shown setting is available, other combination is invalid.

Table 5 Customer Single-turn Reset

Address	Bit(s)	Name	Description	Default
0x0C	[7:0]	Zero Reset 2	MSB bit-17 to bit-10 of Absolute Single-turn	0000-0000
0x0D	[7:0]	Zero Reset 1	Bit-9 to bit-2 of Absolute Single-turn	0000-0000
0x0E	[7:6]	Zero Reset 0	LSB bit-1 to bit-0 of Absolute Single-turn	00

EEPROM Programming

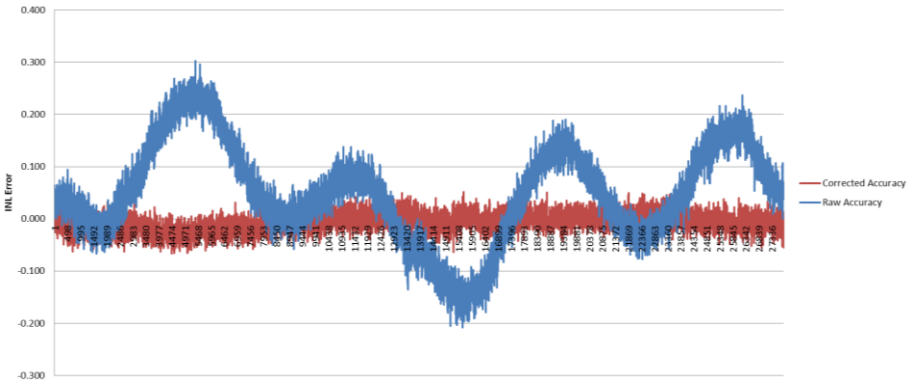
Perform the following steps to program MTP shadow register to EEPROM.

1. Write the desired values to the Customer Configuration MTP registers (0x00 – 0x0E).
2. Verify the written value by reading back all Customer Configuration MTP registers (0x00 – 0x0E).
3. Write value 8'hA1 to address 0x11 to program all Customer Configuration MTP registers to EEPROM.
4. Memory busy bit[8] address 0x22 will flag high for 40ms.
5. Once done, perform power cycle and check for Memory Error bit[4] address 0x21.
    - 0 : No memory error
    - 1 : Memory error

Encoder Calibration

Accuracy Angle Calibration

In order achieve high degree of angle accuracy; AEAT-9922-Q24 comes with a built-in correction algorithm. This algorithm will correct the error upon installation of encoder to the motor. Figure below shows the comparison between raw and corrected accuracy over one rotation.



Followings are the calibration procedure:

Via SPI register

1. Mount the encoder to the motor system (with magnet).
2. Rotate the magnet at constant speed ranging from 10RPM to 2000RPM.
3. Once the speed stabilizes, write value 8'h2 to address 0x12 to initiate calibration sequence.
4. Read the calibration status on bit [1:0] address 0x22
    - 10 : Calibration Pass
    - 11 : Calibration Fail
5. The calibration value is automatically stored in memory, no further programming is required.
    - To erase the calibration value, write value 8'h1 to address 0x12.

Via Hardware Pin M1

1. Mount the encoder to the motor system (with magnet).
2. Rotate the magnet at constant speed ranging from 10RPM to 2000RPM.
3. Once the speed stabilizes, pull the signal High, M1 for >50ms to initiate the calibration sequence.
4. Read the calibration status on output pin ABI
    a. If AB=1, I=0 : Calibration Pass
    b. If AB=1, I=1 : Calibration Fail
5. The calibration value is automatically stored in memory, no further programming is required.

Note Hardware pin calibration is automatically disable upon completion, to re-enable this function, user will need to write value 8'h64 to address 0x07.

Zero Reset Calibration

AEAT-9922-Q24 allows users to configure a zero reset position, followings are the calibration procedure:

Via SPI register

1. Stop the encoder to the motor system at desire location.
2. Once it is stationary, write value 8'h8 to address 0x12 to reset the absolute single-turn position.
3. Read the calibration status on bit [3:2] address 0x22
    - 10 : Calibration Pass
    - 11 : Calibration Fail
4. The offset value is automatically stored in memory, no further programming is required.
    - To erase the calibration value, write value 8'h4 to address 0x12.

Via Hardware Pin M2

1. Stop the encoder to the motor system at desire location.
2. Once it is stationary, pull the signal High, M2 for >50ms to reset the absolute single-turn position.
3. Read the calibration status on output pin ABI
    - If AB=1, I=0 : Calibration Pass
    - If AB=1, I=1 : Calibration Fail
4. The calibration value is automatically stored in memory, no further programming is required.

Note Hardware pin calibration is automatically disable upon completion, to re-enable this function, user will need to write value 8'h128 to address 0x07.

Safety Alarm

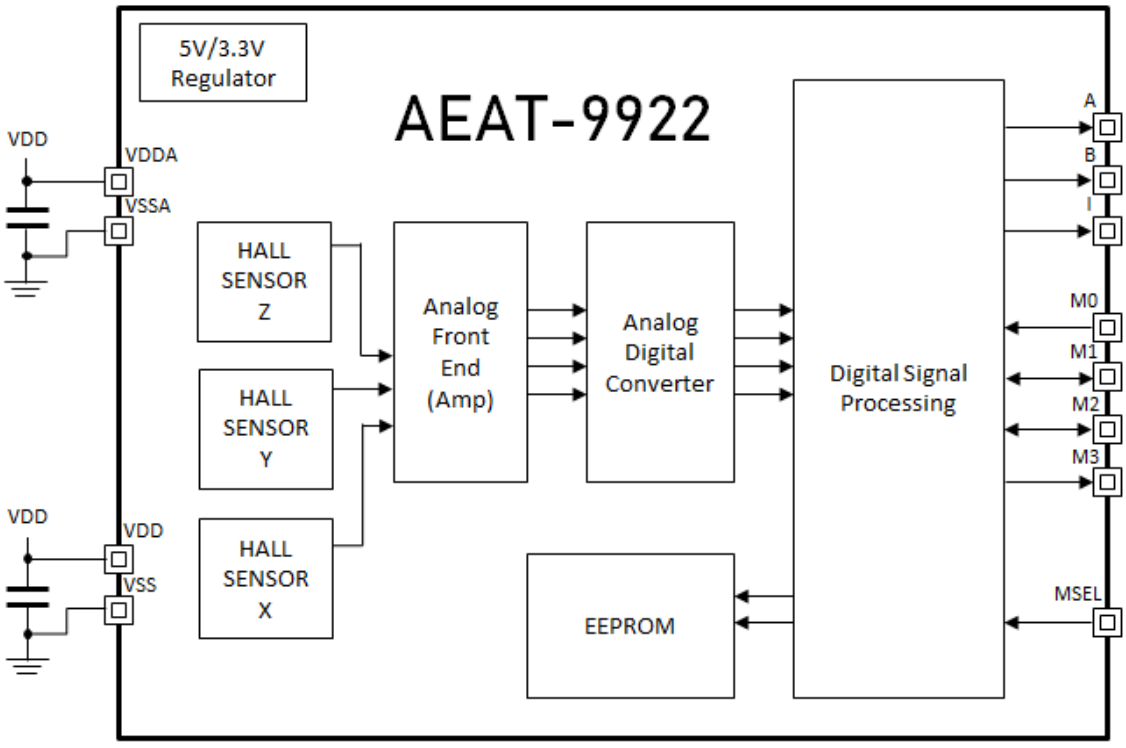
AEAT-9922-Q24 provides following safety alarms:

- Magnet High (MHI) error: This error indicates the magnet strength detected by chip is too strong. When this is flagged high consistently, change to a weaker magnet, or increase the distance between the chip and the magnet.
- Magnet Low (MLO) error: This error indicates the magnet strength detected by chip is too weak. When this is flagged high consistently, change to a stronger magnet, or decrease the distance between the chip and the magnet.

These alarms are read out from SSI interface as described in the "Absolute Output Format" section in the data sheet.

AEAT-9922-Q24 Circuit Diagram

Figure 2 Recommended Circuit Diagram for AEAT-9922-Q24



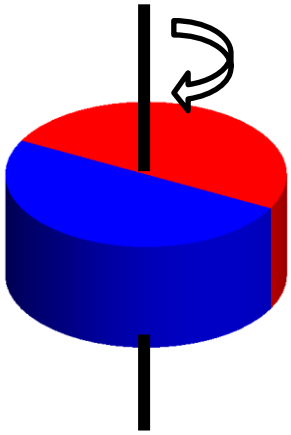
NOTE

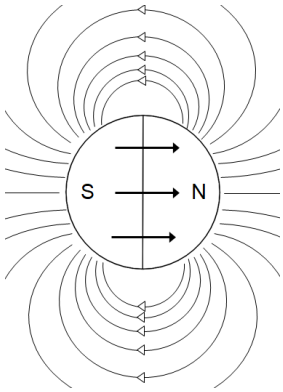
- Connect the 10 µF and 100 nF capacitors as close to the individually assigned power and ground pins as possible.

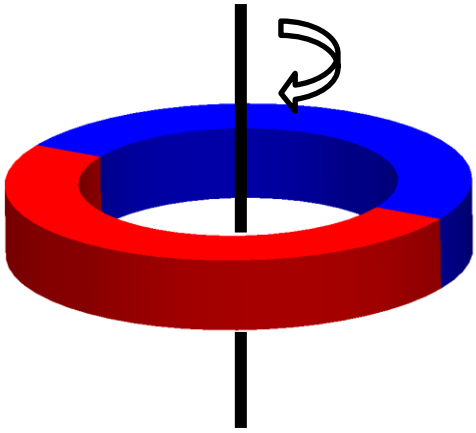
Recommended Magnetic Input Specifications

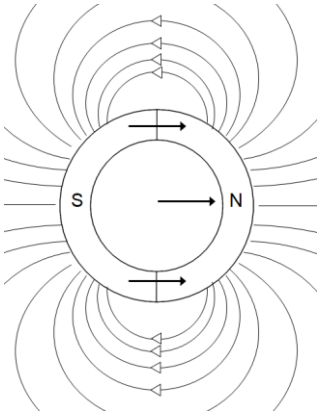
Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Diameter Disc magnet Ring magnet ID /OD	d	 4 -	 6 ID,15 OD,25	 - -	 mm mm	Recommended magnet: Cylindrical magnet or ring magnet diametrically magnetized & 1 pole pair.
Thickness Disc magnet Ring magnet	t	 - 2	 2.5 6	 - -	 mm mm	
Magnetic input filed magnitude On-axis (Disc Magnet) Off-axis (Ring Magnet)	Bpk	 45 30	 - -	 100 150	 mT mT	Required vertical/horizontal component of the magnetic field strength on the die's surface, measured along concentric circle.
Magnet displacement radius	R_m			0.25	mm	Displacement between magnet axis to the device center
Recommended magnet material and temperature drift			-0.12		%/K	NdFeB (Neodymium Iron Boron),grade N35SH

Diametrically Magnetized Magnet









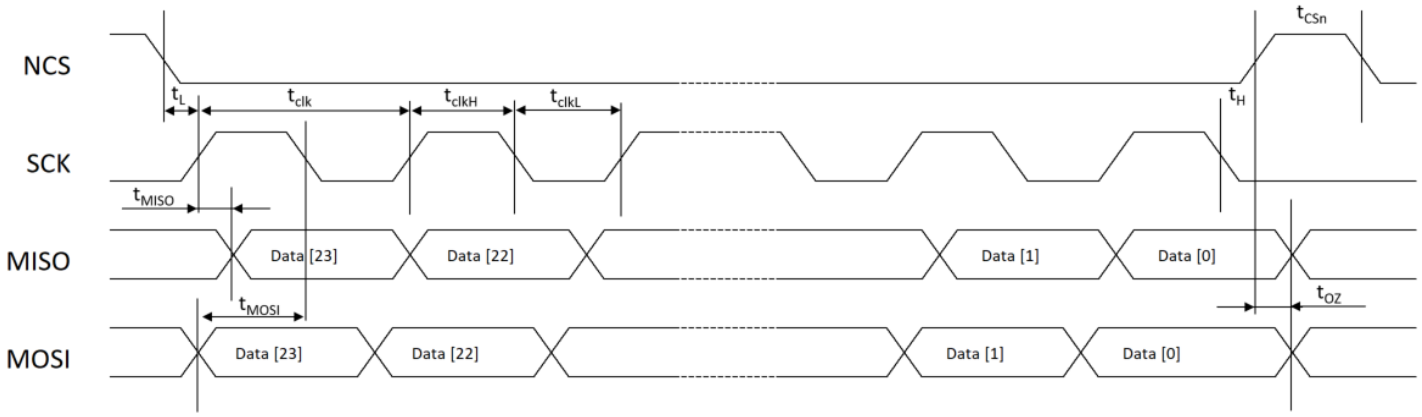
Absolute Output Format

SPI Protocol

SPI protocol uses four pins from AEAT-9922. These four pins are shared between UVW, SSI, SPI protocols. MSEL (input pin) selects either protocol at a time. Assert 1 on MSEL pin to select the SPI4 protocol.
SPI4 protocols allow user to access memory read or write and position data. It uses CPOL=0, CPHA=1 for triggering.

- M0 → SPI_Chip Select (NCS) signal for SPI protocol, input to AEAT-9922
- M1 → SPI_Data Input (MOSI) signal for SPI protocol, input to AEAT-9922
- M2 → SPI_Clock Input (SCK) signal for SPI protocol, input to AEAT-9922
- M3 → SPI_Data Output (MISO) signal for SPI protocol, output from AEAT-9922

SPI4 Timing Diagram



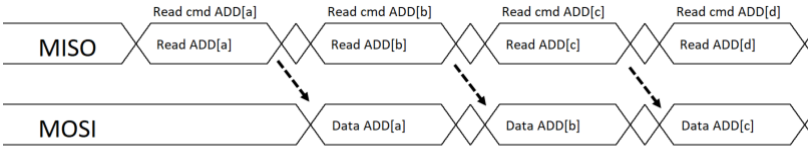
Symbol	Description	Min	Typ	Max	Unit
t_L	Time between SCn falling edge and CLK rising edge	350			ns
t_{clk}	Serial clock period	100			ns
t_{clkL}	Low period of serial clock	50			ns
t_{clkH}	High period of serial clock	50			ns
t_H	Time between last falling edge of CLK and rising edge of CSn	$t_{clk/2}$			ns
t_{CSn}	High time of CS between two transmission	350			ns
t_{MOSI}	Data input valide to clock ege	20			ns
t_{MISO}	CLK edge to data output valid		51		ns
t_{OZ}	Time between CSn rising dege and MISO HiZ		10		ns

NOTE

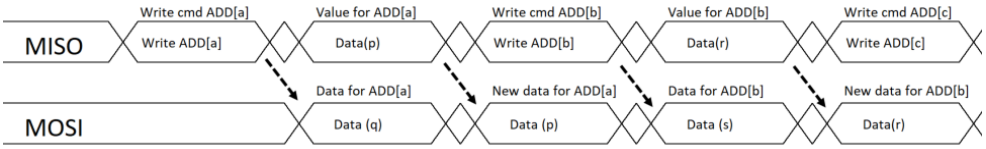
- The user should read back data to confirm data is written successfully

SPI4 Command and Data Frame

SPI4 Read sequence



SPI4 Write sequence



SPI-4(A) 16-bit (Parity)

By default the chip is configured to SPI4 16-bit selection, **PSEL [1] = 0, PSEL [0] = 0** in the register setting.

	Data Format																			
	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Master to Slave					P	RW	0	0	0	0	0	0	Addr/Data[7:0]							
Slave to Master (memory)					P	EF	0	0	0	0	0	0	Data[7:0]							
Slave to Master (pos 10b)					P	EF	Pos[9:0]										0	0	0	0
Slave to Master (pos 11b)					P	EF	Pos[10:0]											0	0	0
Slave to Master (pos 12b)					P	EF	Pos[11:0]												0	0
Slave to Master (pos 13b)					P	EF	Pos[12:0]													0
Slave to Master (pos 14b)					P	EF	Pos[13:0]													
Slave to Master (pos 15b)				P	EF	Pos[14:0]														
Slave to Master (pos 16b)			P	EF	Pos[15:0]															
Slave to Master (pos 17b)		P	EF	Pos[16:0]																
Slave to Master (pos 18b)	P	EF	Pos[17:0]																	

P: Parity

EF: Error Flag

RW: Read = 1, Write = 0

SPI4-(B) 24-bit (CRC)

To configure the chip to SPI4 24-bit selection, set **PSEL [1] = 0, PSEL [0] = 1** in the register setting.

	Data Format																											
	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Master to Slave					0	RW	0	0	0	0	0	0	Addr/Data[7:0]								CRC[7:0]							
Slave to Master (memory)					W	E	0	0	0	0	0	0	Data[7:0]								CRC[7:0]							
Slave to Master (pos 10b)					W	E	Pos[9:0]										0	0	0	0	CRC[7:0]							
Slave to Master (pos 11b)					W	E	Pos[10:0]											0	0	0	CRC[7:0]							
Slave to Master (pos 12b)					W	E	Pos[11:0]												0	0	CRC[7:0]							
Slave to Master (pos 13b)					W	E	Pos[12:0]													0	CRC[7:0]							
Slave to Master (pos 14b)					W	E	Pos[13:0]														CRC[7:0]							
Slave to Master (pos 15b)				W	E	Pos[14:0]															CRC[7:0]							
Slave to Master (pos 16b)			W	E	Pos[15:0]																CRC[7:0]							
Slave to Master (pos 17b)		W	E	Pos[16:0]																	CRC[7:0]							
Slave to Master (pos 18b)	W	E	Pos[17:0]																		CRC[7:0]							

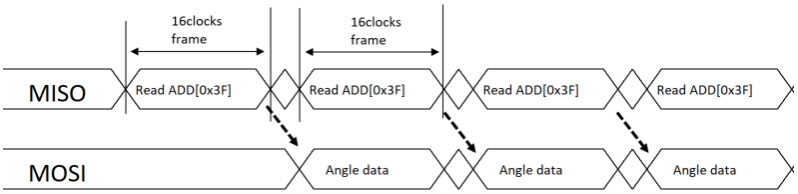
W: Warning

E: Error

RW: Read = 1, Write = 0

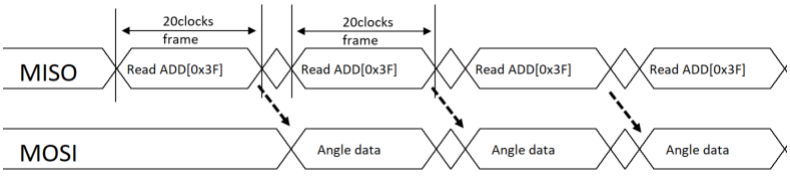
Position Read

Absolute position data can be obtained by sending read command to address **0x3F.**



In the event of higher single turn resolution (15-bit and above), the command and data frame size is adjusted accordingly.

Example: 18bit + 2bit (parity and error)



Warning and Error bit

Error bit is trigger if either Magnet High (MHI), Magnet Low (MLO), Memory Error (MEM_Err) or communication error.

Details of error bit is available in register address below:

Address	bit							
	7	6	5	4	3	2	1	0
0x21	RDY	MHI	MLO	MEM_Err				

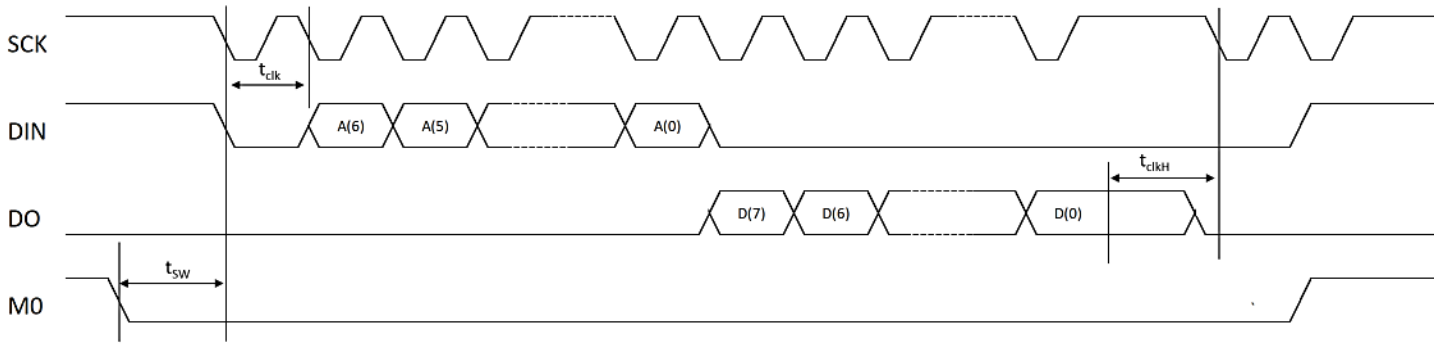
- **Magnet High (MHI) Error:** This indicates that the magnet strength detected by the chip is too strong. When this is flagged high consistently, change the weaker magnet or increase the distance between the chip and the magnet.
  The value for this alarm is represented as 1.
- **Magnet Low (MLO) Error:** This indicates that the magnet strength detected by the chip is too weak. When this is flagged high consistently, change the stronger magnet or decrease the distance between the chip and the magnet.
  The value for this alarm is represented as 1.
- **Ready:** The chip is ready, and the ready value is 1.

SPI3

SPI3 protocols only allow access to memory read write. Assert 0 on **MSEL** and **M0** pin to configure it.

- M0 → Set to low, input to AEAT-9922
- M1 → SPI_Data Input (DIN) signal for SPI protocol, input to AEAT-9922
- M2 → SPI_Clock Input (SCK) signal for SPI protocol, input to AEAT-9922
- M3 → SPI_Data Output (DO) signal for SPI protocol, output from AEAT-9922

SPI3 Timing Diagram

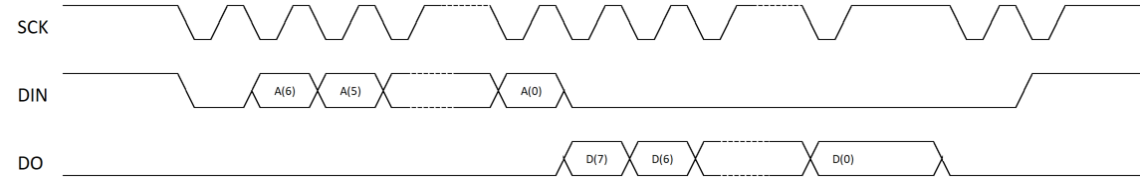


Symbol	Description	Min	Typ	Max	Unit
t_{SW}	Time between SCn falling edge and CLK rising edge	1	-	-	us
t_{clk}	Serial clock period	-	-	100	ns
t_{clkH}	CLK high time after end of last clock period	300	-	-	ns

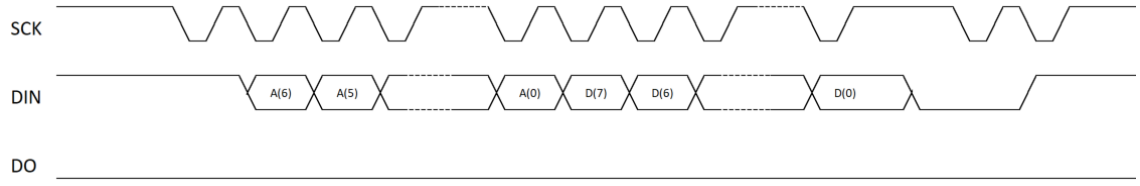
NOTE

- The user should read back data to confirm data is written successfully

SPI3 Read



SPI3 Write



Serial Synchronous Interface 3-wire (SSI3)

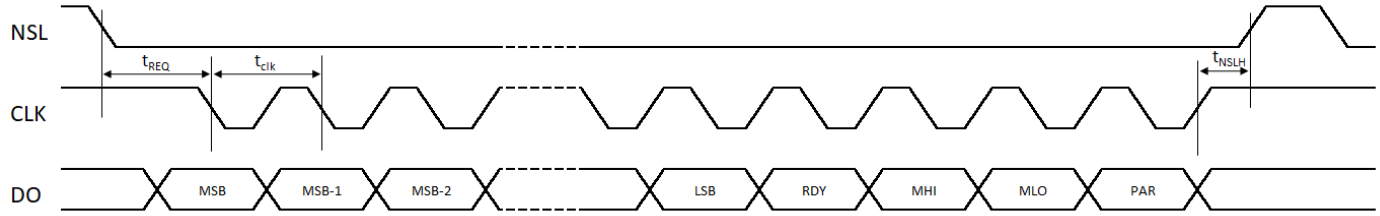
SSI3 protocol uses three pins from AEAT-9922. These three pins are shared between UVW, SSI, SPI protocols. MSEL (input pin) selects either protocol at a time. Assert 0 on **MSEL** pin and 1 on **M0** pin to select the SSI protocol.

- M1 → SSI_NSL Input (NSL) signal for SSI protocol, input to from AEAT-9922
- M2 → SSI_Clock Input (CLK) signal for SSI protocol, input to AEAT-9922
- M3 → SSI_Data Output (DO) signal for SSI protocol, output from AEAT-9922

It is available in 2 options per PSEL register setting:

Figure 8 SSI Protocol Timing Diagram

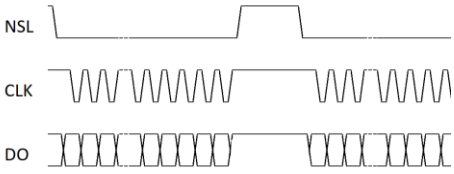
Default : Data Output with 3 wire SSI to 10Mhz clock rates



Symbol	Description	Min	Typ	Max	Unit
tclk	SSI_SPI_SEL switch time	1	-	-	Us
tREQ	SCL hight time between NLS falling edge and first SCL falling edge	300	-	-	ns
tNSLH	NSL high time between 2 successive SSI reads	200	-	-	ns

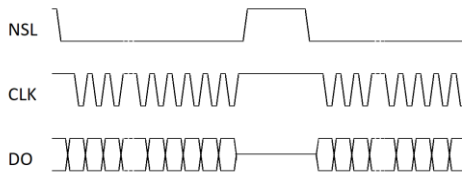
SSI-3(A)

DO pin is held at high state once NSL pin is high



SSI-3(B)

DO pin is tristate (high impedance) state once NSL pin is high

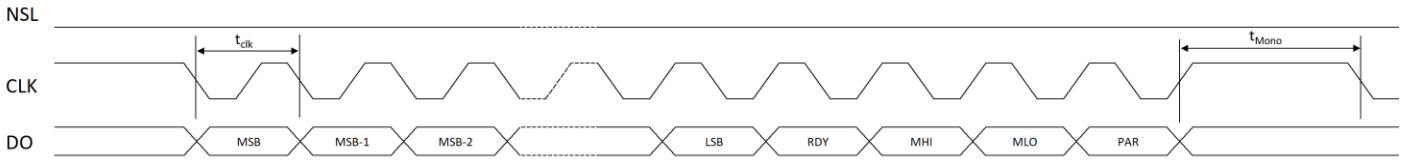


Serial Synchronous Interface 2-wire (SSI2)

SSI2 protocol uses two pins from AEAT-9922. These two pins are shared between UVW, SSI, SPI protocols. MSEL (input pin) selects either protocol at a time. Assert 0 on **MSEL** & **M1** pin and 1 on **M0** pin upon power up.

- M2 → SSI_Clock Input (CLK) signal for SSI protocol, input to AEAT-9922
- M3 → SSI_Data Output (DO) signal for SSI protocol, output from AEAT-9922

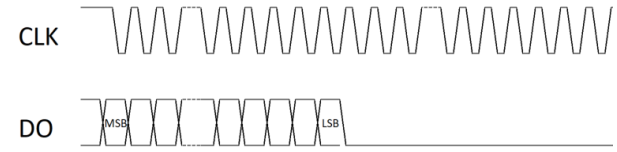
It is available in 2 options per PSEL register setting:



Symbol	Description	Min	Typ	Max	Unit
tClk	NSL low time after rising edge of last clock period for an SSI read	250	-	tM/2	ns
tM	NSL high time between 2 successive SSI reads	-	16.5	18.0	us

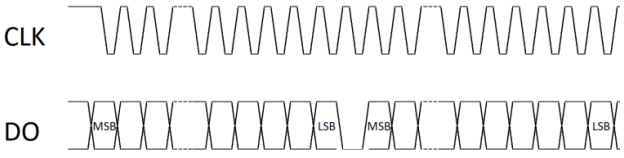
SSI-2(A)

Output single data position and remains low after LSB until the next monoflops (tM) expires.



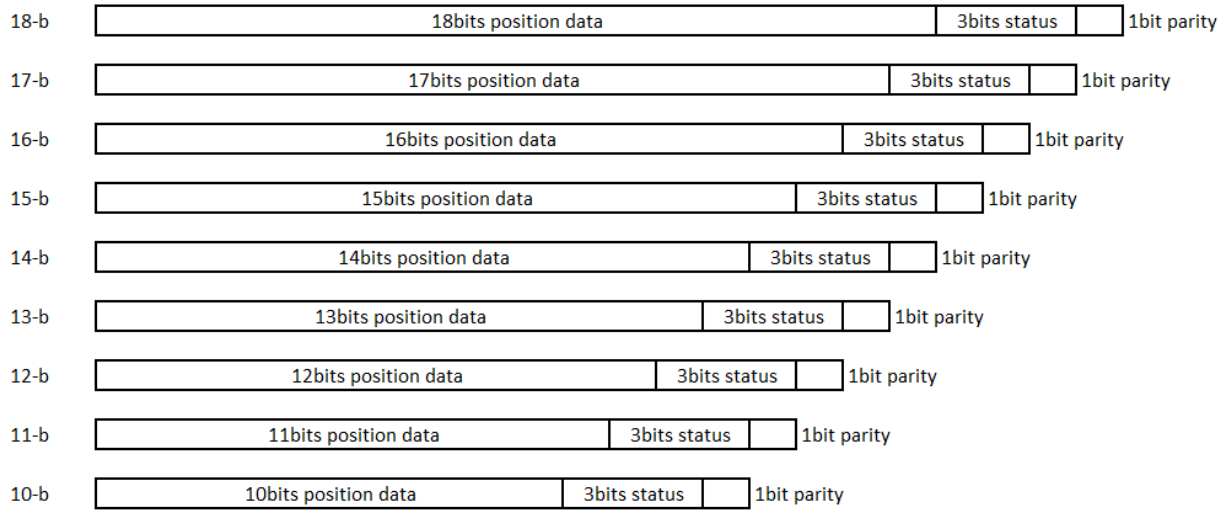
SSI-2(B)

The same position data can be continuously output by sending clock train and data is separated by a single low pulse.
Data will be refresh on the next monoflop (tM) expires.



SSI READ Data Format

Figure 9 SSI Output Format for Different Absolute Resolution Settings



NOTE

- 3-b status: {Ready, MHI, MLO}

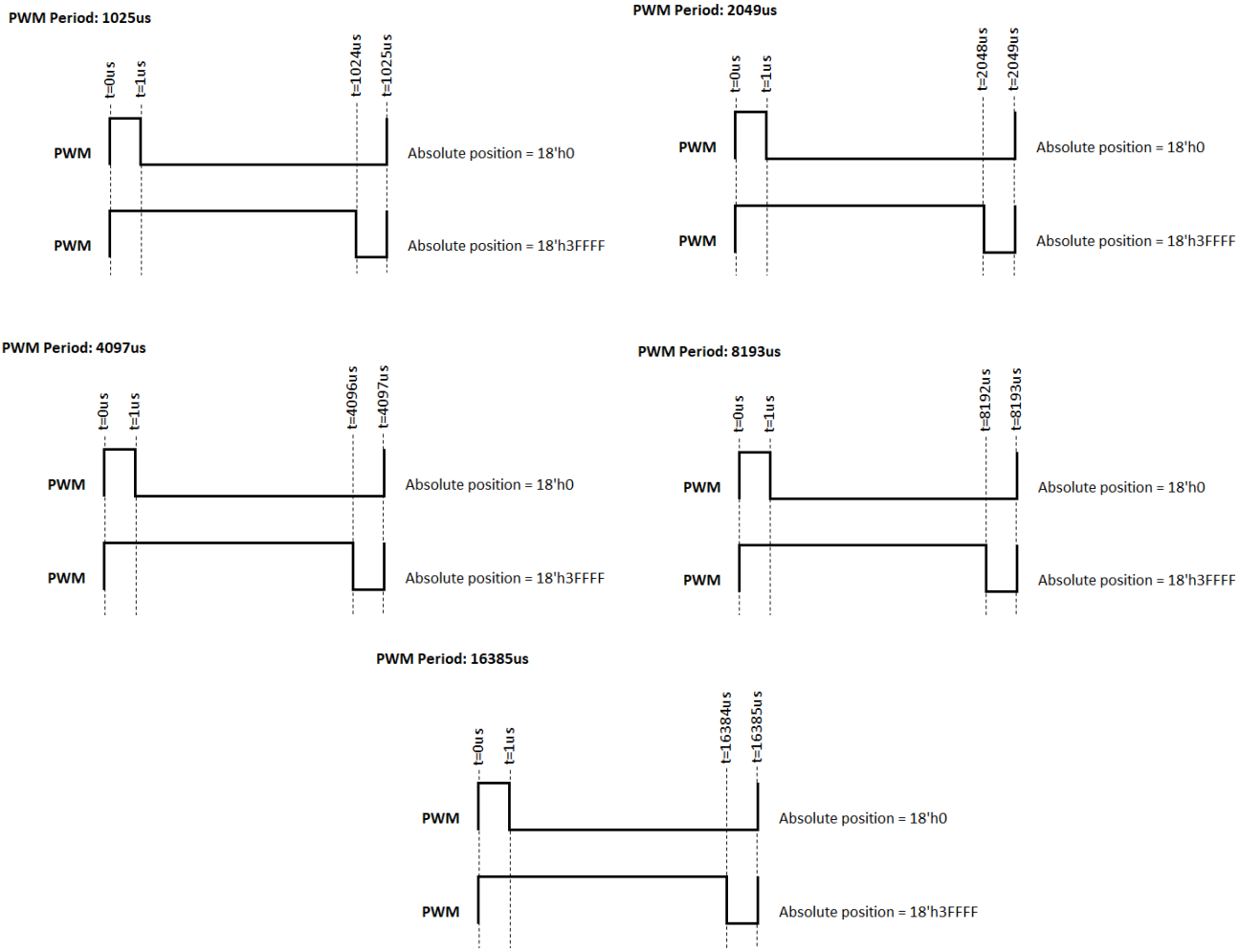
- **Magnet High (MHI) Error:** This indicates that the magnet strength detected by the chip is too strong. When this is flagged high consistently, change the weaker magnet or increase the distance between the chip and the magnet.
  The value for this alarm is represented as 1.
- **Magnet Low (MLO) Error:** This indicates that the magnet strength detected by the chip is too weak. When this is flagged high consistently, change the stronger magnet or decrease the distance between the chip and the magnet.
  The value for this alarm is represented as 1.
- **Ready:** The chip is ready, and the ready value is 1.
  1-b parity is even parity.

PWM

PWM protocol uses one output pin (W_PWM) from AEAT-9922. Note that W_PWM pin is shared between UVW and PWM protocols. The PWM signals are configurable to have period of 1025, 2049, 4097, 8193 or 16385 µs. During power-up, the PWM signal is 0 before chip ready.

PWM Signals (Period = 1025/2049/4097/8193/16385 µs)

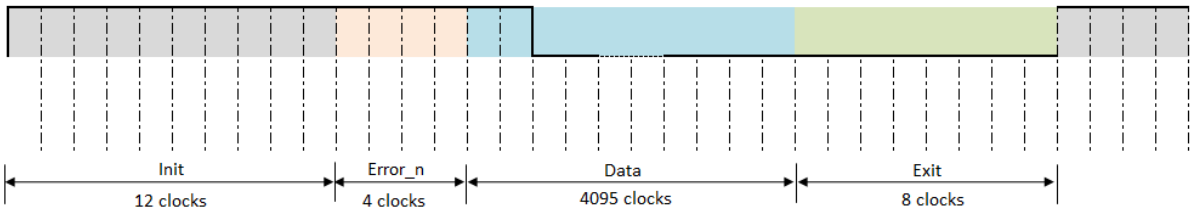
- PWM period: 1025, 2049, 4097, 8193, 16385 µs



PWM protocols is also available in with Init, Error_n, and Exit along with Data information.

PWM Signals (Period = 1047/2071/4119/8215/16407 µs)

PMW Period: 4119us



Incremental Output Format

The AEAT-9922 provides ABI and UVW signals to indicate incremental position of the motor.

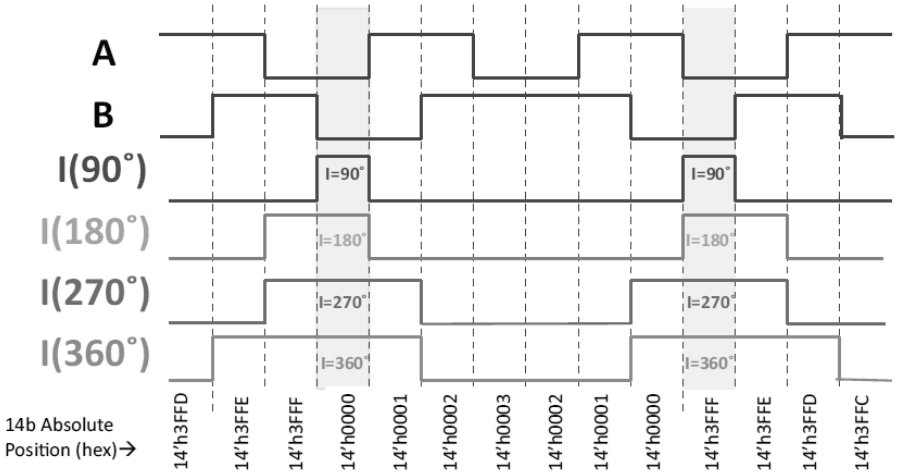
ABI

The ABI incremental interface is available to provide position data and direction data from the three output pins (A, B, and I).

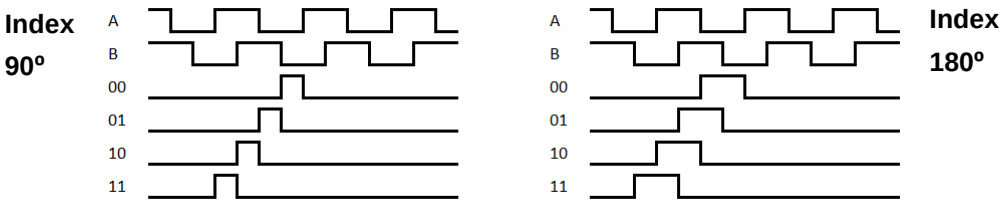
The index signal marks the absolute angular position and typically occurs once per revolution The ABI signal is configurable using the memory map registers. It supports the following configuration:

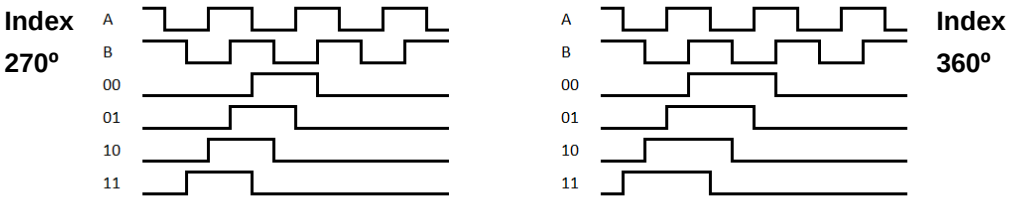
- Programmable CPR: 1 to 10000CPR
- Programmable I-width: 90, 180, 270, or 360 electrical degrees (edeg)

Figure 11 ABI Signal (4096 CPR, with Different I-Width Settings), Assuming User Sets Hysteresis at 0.02 Mechanical Degree



The Index position is configurable among the incremental state.
Index signal raise high once per turn at absolute zero position.

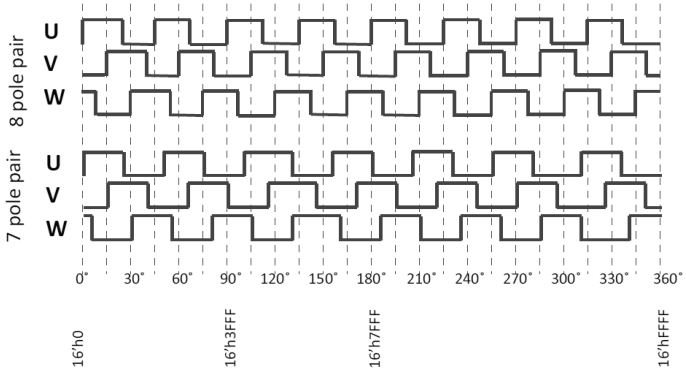


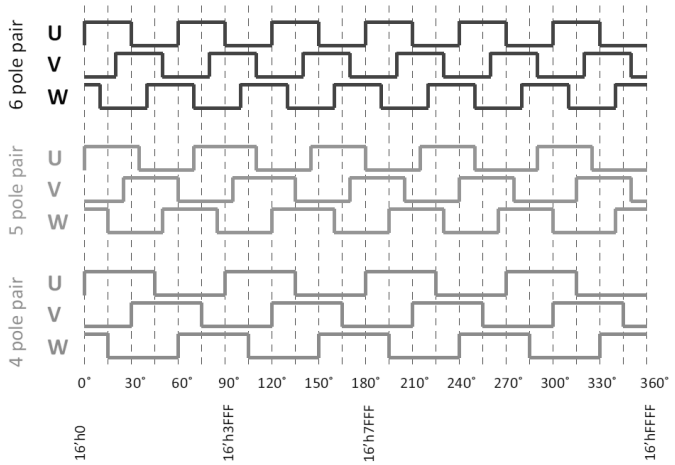


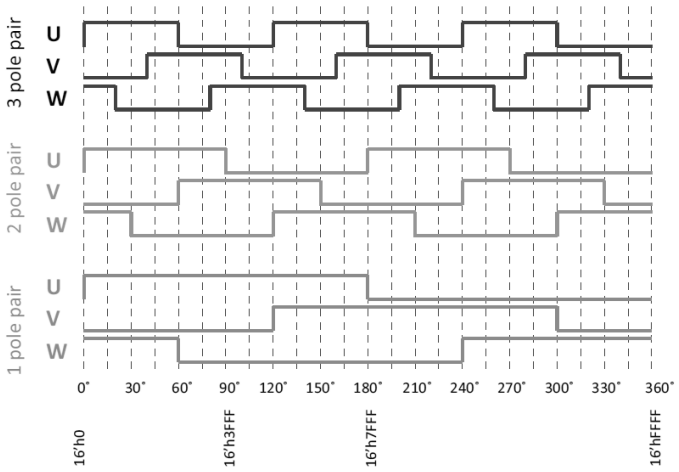
UVW

Three-channel integrated commutation output (U, V, W) emulates Hall sensor feedback and is available using three output pins. Note that W_PWM pin is shared between the UVW and PWM protocols.

AEAT-9922 can configure pole pairs from 1 to 8 equivalents to 2 to 16 poles.

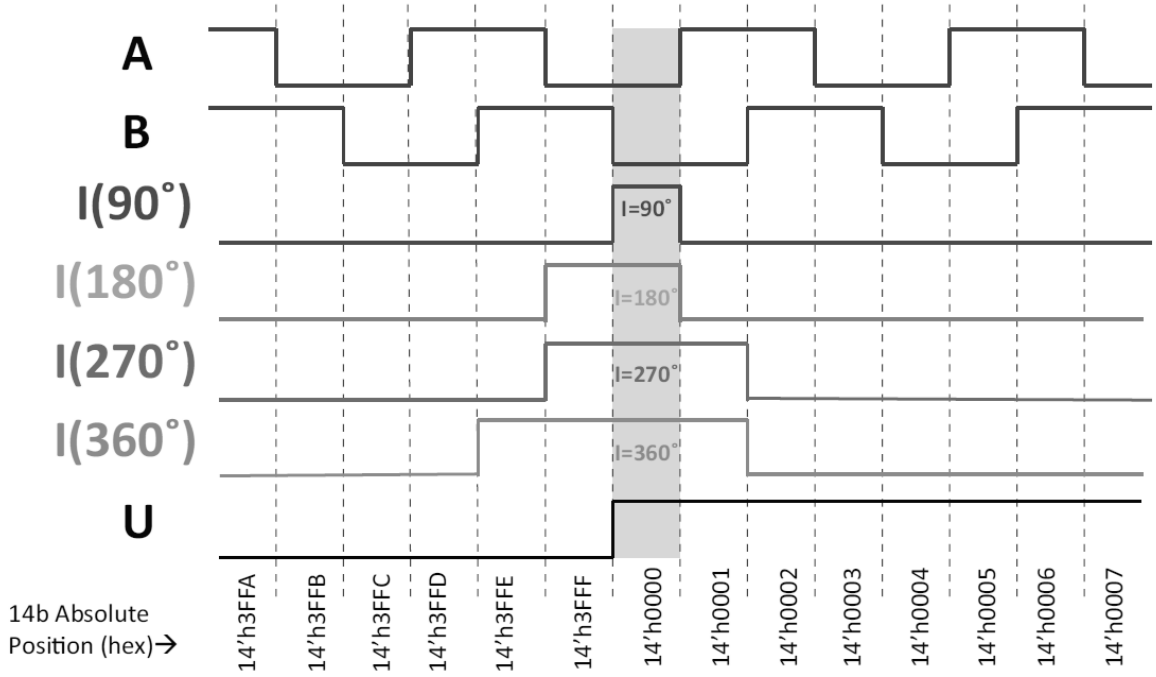






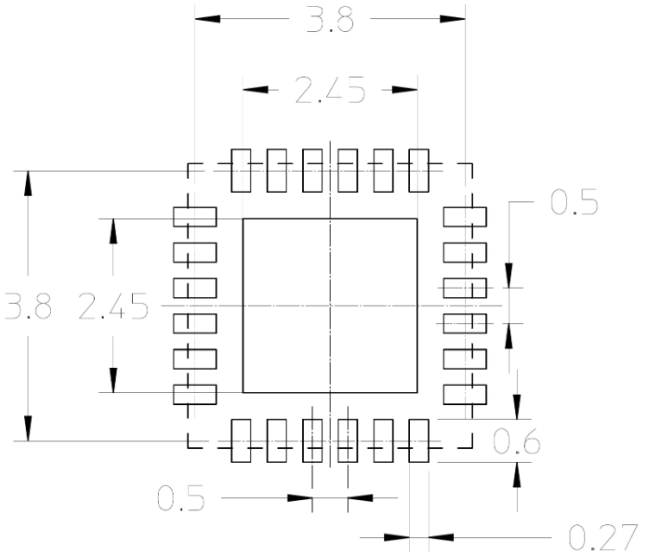
Note that signal U from UVW protocol is tagged to signal I from the ABI protocol as shown in the following figure.

Figure 13 U-to-I Tagging

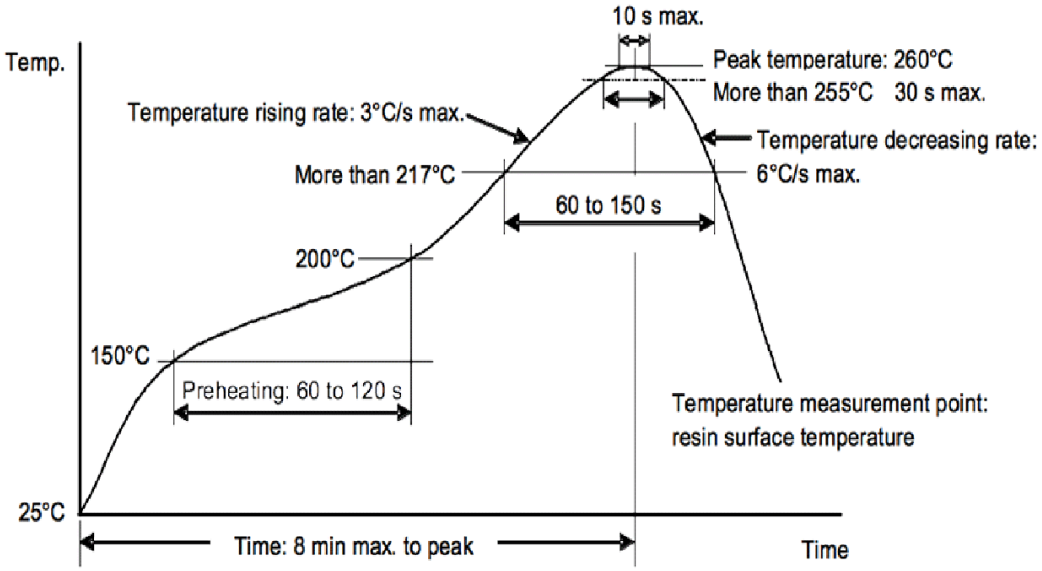


Recommended PCB Land Pattern (in mm)

Land Pattern Dimensions



Recommended Lead Free Solder Reflow Soldering Temperature Profile



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