

**TECHNICAL MANUAL
NS70/75
MEMORY CARD ASSEMBLY
(PDP-11/70 INSTALLATION)**



National Semiconductor
Memory Systems

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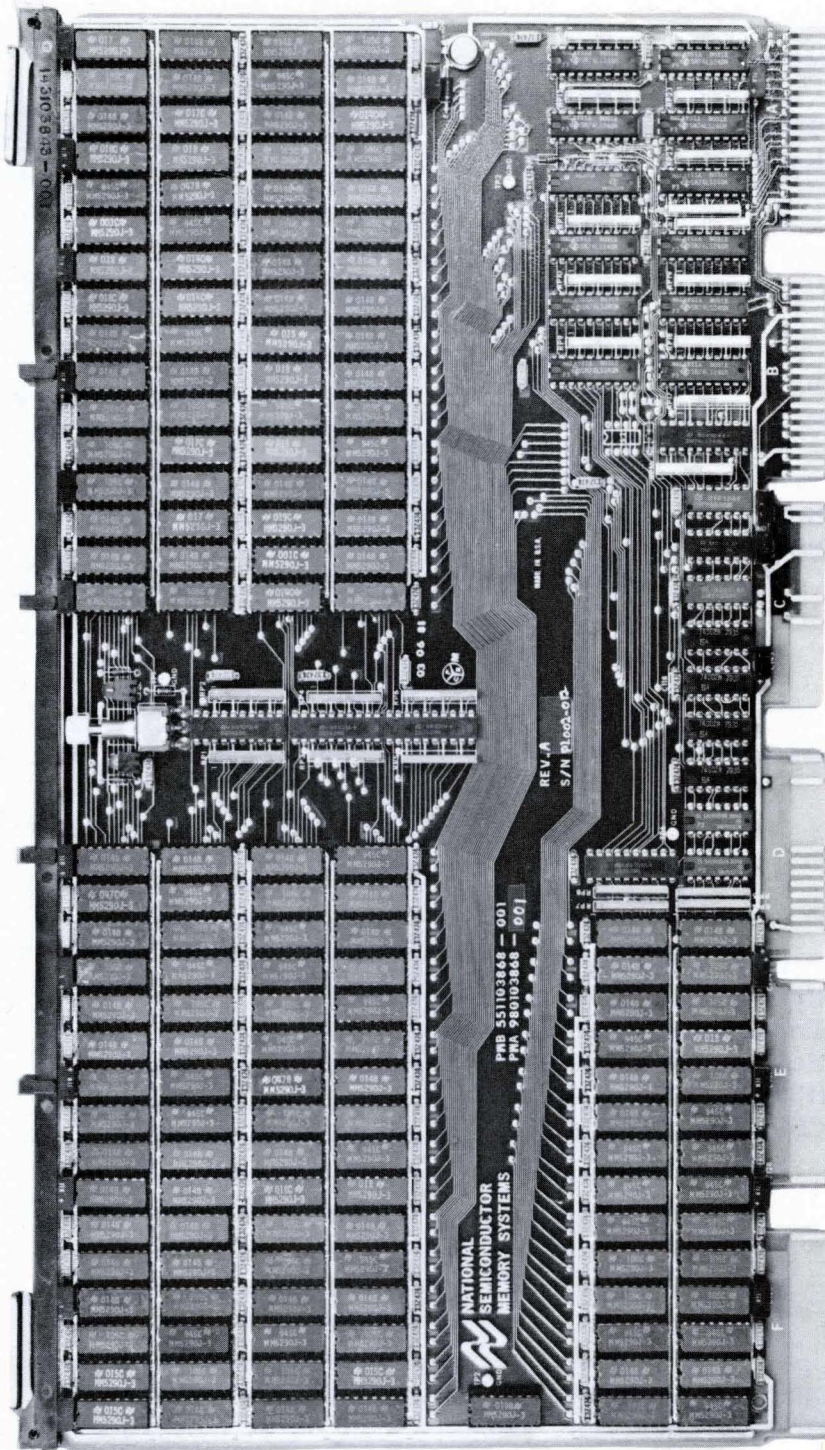


Figure 1-1 NS70/75

SECTION I

GENERAL DESCRIPTION

1.1 INTRODUCTION

This manual contains five sections which describe the NS70/75 add-in memory card. This information includes a general description, theory of operation, installation and maintenance, the console and diagnostic procedure, and a section containing schematics, assembly prints and a bill of materials. Figure 1-1 is a photograph of the NS70/75 memory card.

1.2 PURPOSE

The NS70/75 is designed as an add-in memory card for DEC's* PDP-11/70 MK11 MOS Memory System, and may be operated with, or in place of, the DEC model M7984 or M8728 storage cards.

NOTE: THE NS70/75 STORAGE CARD CANNOT
OPERATE IN THE DEC MJ11 CORE MEMORY
SYSTEM

1.3 PHYSICAL DESCRIPTION

The NS70/75 memory is contained on one multilayer printed circuit card. The physical dimensions are as follows:

THICKNESS	-	.480 inches
HEIGHT	-	8.680 inches
LENGTH	-	15.687 inches

* DEC and PDP are trademarks of Digital Equipment Corporation.

The card is designed to mount on a minimum center-to-center board spacing of 0.5 inches. Two card ejectors permit easy insertion and removal of the card.

1.4 FUNCTIONAL DESCRIPTION

The NS70/75 is organized as a 64K x 39 bit add-in memory for the DEC PDP-11/70 MK11 MOS Memory System. The card is hardware and software compatible with the MK11 system and its memory controller set, and is installed directly into the DEC semiconductor memory chassis without modification to the DEC hardware or cabling. Up to sixteen NS70/75 memory cards can be installed in a single chassis, allowing memory system expansion up to 4M Bytes without additional memory chassis.

Features include:

- . Battery backup capability
- . ON/OFF line switch
- . POWER ON and ON LINE LED indicators
- . All RAMS are socketed for easy field replacement
- . Spare burned-in RAM on board
- . Simplified installation: no jumpers or switches to change
- . Pre-shipment testing for 72 hours at 70°C
- . Two year warranty

1.5 GENERAL SPECIFICATIONS

The following tables list the general specifications of the NS70/75 memory card. Table 1-1 lists the power requirements, and Table 1-2 lists the cycle and access times to which the memory card is tested. The MK11 internal bus cycle and access times are set by the memory controller cards, and in all cases the MK11 requirements are met or exceeded by the NS70/75.

TABLE 1-1 POWER REQUIREMENTS

SUPPLY VOLTAGE	CURRENT		
	OPERATIONAL (MAX.)	STANDBY (MAX.)	BATT. BACKUP (MAX.)
+5V	.13A	.13A	N/A
+5VBB	1.1A	1.1A	1.1A
+12V	1.2A	.4A	.4A
-12V	30mA	30mA	30mA

TABLE 1-2 CYCLE AND ACCESS TIME

MODE	TIME
READ ACCESS	225ns
READ CYCLE	500ns
WRITE CYCLE	500ns
REFRESH CYCLE	500ns
R/M/W CYCLE	700ns

NOTE: Cycle time is defined as the leading edge of RAS TM to the leading edge of the next consecutive RAS TM signal on the MK11 internal bus. Access time is defined as the leading edge of RAS TM to valid data on the bus.

1.6 ENVIRONMENTAL SPECIFICATIONS

The NS70/75 is designed to operate over a variety of environmental conditions as listed below:

1.6.1 Operating Specifications

- . TEMPERATURE - Ambient air temperature range of 0°C to 50°C.
- . THERMAL SHOCK - Maximum rate of change of 30°C per hour during operation.

- . HUMIDITY - Relative humidity of up to 95% (non-condensing) during operation.
- . ALTITUDE - +10,000 feet msl to - 1,000 feet msl.
- . COOLING - Suggested minimum air flow is 25 cfm.

1.6.2 Shipping and Storage Specifications

- . TEMPERATURE - Ambient air temperature range of -40°C to +85°C.
- . THERMAL SHOCK - Max. rate of 10°C per minute.
- . ALTITUDE - 40,000 feet msl.
- . MECHANICAL SHOCK - THE NS70/75 memory, housed in its shipping container, can tolerate mechanical shock resulting from drop tests performed in accordance with MIL-STD-810B, Method 516, Procedure V without exhibiting damage or degradation.

1.7 RELIABILITY

This card is designed and manufactured to the best commercial standards of workmanship. Vigorous testing is conducted (including testing over operating temperature range) to ensure a reliable service of ten years at 14 hours per day usage (exclusive of routine maintenance time). The design is such that catastrophic failure occurrence is minimized and minimal propagation of such failure will be experienced.

SECTION II

THEORY OF OPERATION

2.1 OVERVIEW

The NS70/75 memory module is a MOS dynamic RAM array board. A minimal amount of logic is used to provide bus receivers, array drive and decode, and bus drivers. Figure 2-1 shows the block diagram of the NS70/75 memory board.

2.2 ADDRESS LOGIC

The low order addresses, A6-A0, provide the array row and column addresses. The address multiplexing is done by the MK11 controller. These addresses are received and gated with the board select signal before being driven to the RAMs. The high order addresses, MA14, and MA15, are decoded to select 1 of 4 rows of RAMs.

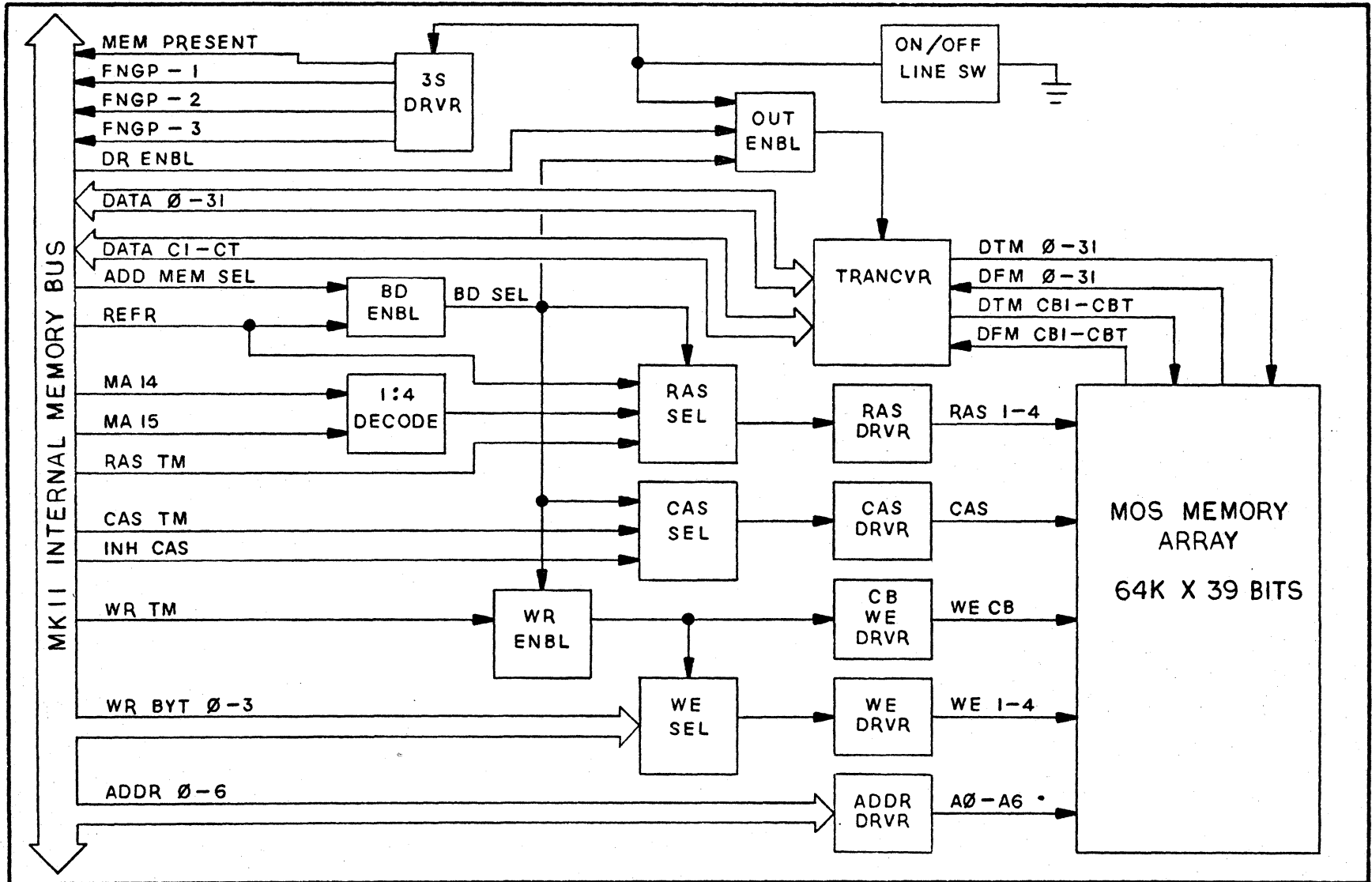
2.3 BOARD SELECT

Each board in the system is selected by its own "ADD MEM SEL" signal. Board selection is also enabled by the receipt of the "REF CYC" signal. Board select must be enabled before any memory operation can occur.

2.4 RAS AND CAS

The row address strobe (RAS) is received, gated with the row decode logic, and driven to the selected row of RAMs. The column address strobe (CAS) is received and driven to all of the RAMs.

Figure 2-1 NS70/75 SYSTEM BLOCK DIAGRAM



2.5 DATA LOGIC

The data register enable (DREN) signal is received and gated with board select to enable the data output drivers during a READ or the READ portion of a READ-MODIFY-WRITE cycle. The input data receivers are always enabled.

2.6 READ/WRITE LOGIC

The write timing signal (WR TM) is asserted any time a WRITE operation is going to be performed. The write timing signal is received, gated with board select, and driven to the Check Bit portion of the storage array (check bits are always written during any type of write operation). That same signal is also gated with the "write byte" signals (WR BYT 3-0) to allow a write byte operation. In the write byte mode, not all of the "WR BYT" signals are asserted.

2.7 REFRESH

A refresh cycle is initiated by the receipt of the "REF CYC" signal. The "REF CYC" signal, in conjunction with address, RAS, and CAS timing, will enable array refreshing once every 15 μ S. All memory cards in the system refresh simultaneously. The CAS signal is disabled by the receipt of the CAS inhibit signal (CAS INH TM). When initialization takes place, the "CAS INH TM" signal is not sent, and the entire system is initialized using refresh timing.

2.8 CONFIGURATION SIGNALS

The configuration, or "fingerprint" signals provide the memory controller with information regarding memory size:

<u>FNCP1</u>	<u>FNCP2</u>	<u>FNCP3</u>	<u>MEM SIZE</u>
low	low	low	64K x 39
high	low	low	16K x 39
high	high	high	not present

2.9 ON/OFF LINE SWITCH

When off line, the data output and fingerprint drivers are disabled (Hi - Z). When on line, the yellow LED is illuminated.

2.10 INTERFACE SIGNAL DESCRIPTION

2.10.1 Input Signals

<u>Signal</u>	<u>Pin(s)</u>	<u>Description</u>
BUS, ADDR 6-OH, MA14H, MA15H	AC1, AD2, AF2, AH1, AJ2, AK1, AL2, AP1, AV2	A6-0 are the 7 multiplexed addresses used by the memory array. MA14 and MA15 are used as array row select decode inputs.
BUS ADDR MEM SEL L	AE2	Memory board select. There are 16 ADD MEM SEL lines in the MK11 system.
BUS REF CYC L	AE1	When asserted, enables a refresh or initialization cycle to take place.
BUS CAS TM L	AM1	Column address strobe input to the array.
BUS WR TM L	AN2	When asserted, enables a WRITE, or the WRITE portion of a R/M/W cycle.
BUS WR BYT 3-OH	AV1, BB1, BE1, BM1	When asserted, and in conjunction with WR TM, enables data to be written into an 8-bit byte. For a full 39 bit write cycle, all four lines are asserted.

BUS DREN L	AM2	When asserted, enables data from the memory onto the data bus.
BUS INH CAS TM L	BN2	Disables the CAS drivers on the memory card. Used in conjunction with REFRESH.

2.10.2 Configuration Level Signals

<u>Signal</u>	<u>Pin(s)</u>	<u>Description</u>
MEM PRESENT L	AB2	Always asserted, not used by the MK11.
FNGP 1 L	CK1	Used to signal the controller that a storage card is present.
FNGP 2 L	CM1	
FNGP 3 L	BA1	

2.10.3 Bi-directional Signals

<u>Signal</u>	<u>Pin(s)</u>	<u>Description</u>
BUS DATA 0-31 CB (1,2,4,8,16 32,T)	See Table 2.1 for pin list- ings)	39 bi-directional data lines between the storage cards and the controller.

2.11 INTERFACE CONNECTOR PIN LIST AND TIMING DIAGRAMS

Table 2-1 contains the NS70/75 Interface Pin Listing.
Figure 2-2 contains the NS70/75 Timing Diagrams.

COMPONENT	SOLDER
SIDE 1	SIDE 2

BUS DATA 11	A	+5V
BUS DATA 10	B	MEM PRES L
BUS MA 15H	C	OV
BUS DATA 9	D	BUS MA 14H
BUS REF CYC L	E	BUS ADD MEM SEL L
BUS DATA 8	F	BUS A2 H
BUS A1 H	H	BUS DATA 27
BUS DATA 26	J	BUS A3 H
BUS AO H	K	BUS DATA 25
BUS DATA 24	L	BUS A6 H
BUS CAS TM L	M	BUS DR EN L
BUS DATA 15	N	BUS WR TM L
BUS A5 H	P	BUS DATA 31
+12V BATT	R	BUS DATA 14
-12V	S	BUS RAS TM L
OV	T	BUS DATA 13
+12V BATT	U	BUS DATA 12
BUS WR BYT 3H	V	BUS A4 H

Connector A

COMPONENT	SOLDER
SIDE 1	SIDE 2

FNGP 3L	A	
BUS WR BYT 1H	B	BUS DATA 29
BUS DATA 30	C	OV
+5V BATT	D	BUS DATA 28
BUS WR BYT 0H	E	BUS DATA 19
BUS DATA 18	F	BUS DATA 3
BUS DATA 17	H	BUS DATA 16
BUS DATA 2	J	BUS DATA 0
BUS DATA CB 8	K	BUS DATA 1
BUS DATA CB 2	L	BUS DATA CB 4
BUS WR BYT 2H	M	BUS DATA CB 1
-5V	N	BUS INH CAS TM L
BUS DATA 7	P	BUS DATA 6
BUS DATA 5	R	BUS DATA 4
BUS DATA 23	S	BUS DATA 22
OV	T	BUS DATA 21
BUS DATA 20	U	BUS DATA CBT
BUS DATA CB 32	V	BUS DATA CB 15

Connector B

Table 2-1 NS70/75 INTERFACE PIN LISTING

COMPONENT
SIDE 1

SOLDER
SIDE 2

	A	
NPG	B	
	C	
	D	
-5V TEST	E	
	F	
	H	
	J	
FNGP 1 L	K	
	L	
FNGP 2 L	M	
	N	
	P	
	R	
	S	
	T	
	U	
	V	

Connector C

COMPONENT
SIDE 1

SOLDER
SIDE 2

	A	+5V
	B	
	C	OV
	D	
	E	
	F	
	H	
	J	
	K	BG 7
	L	BG 7
	M	BG 6
	N	BG 6
	P	BG 5
	R	BG 5
	S	BG 4
OV	T	BG 4
	U	
	V	

Connector D

Table 2-1 (cont.)

INTERFACE TIMING (READ)

TIME (nS)

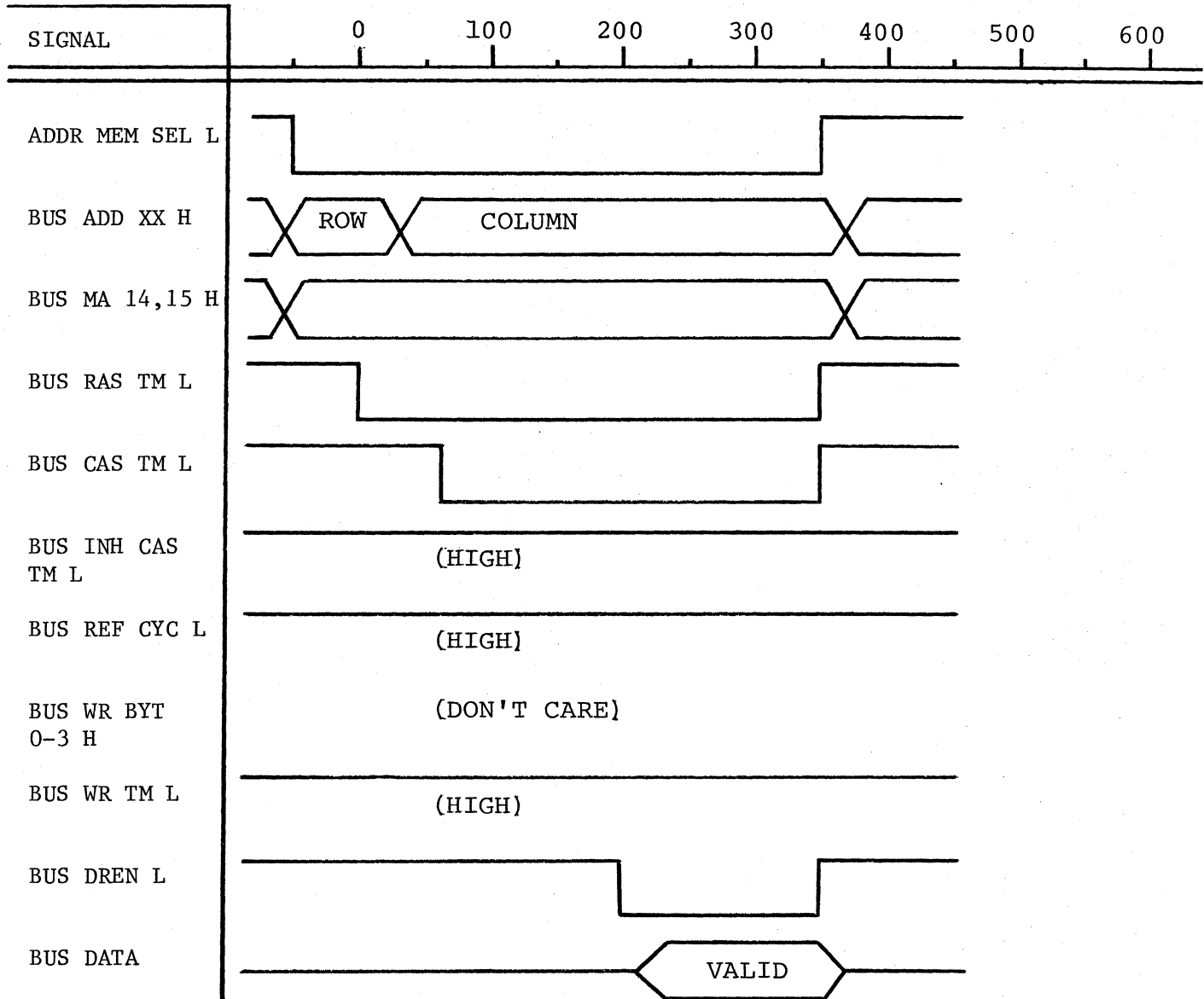


Figure 2-2 Timing Diagrams

INTERFACE TIMING (WRITE)

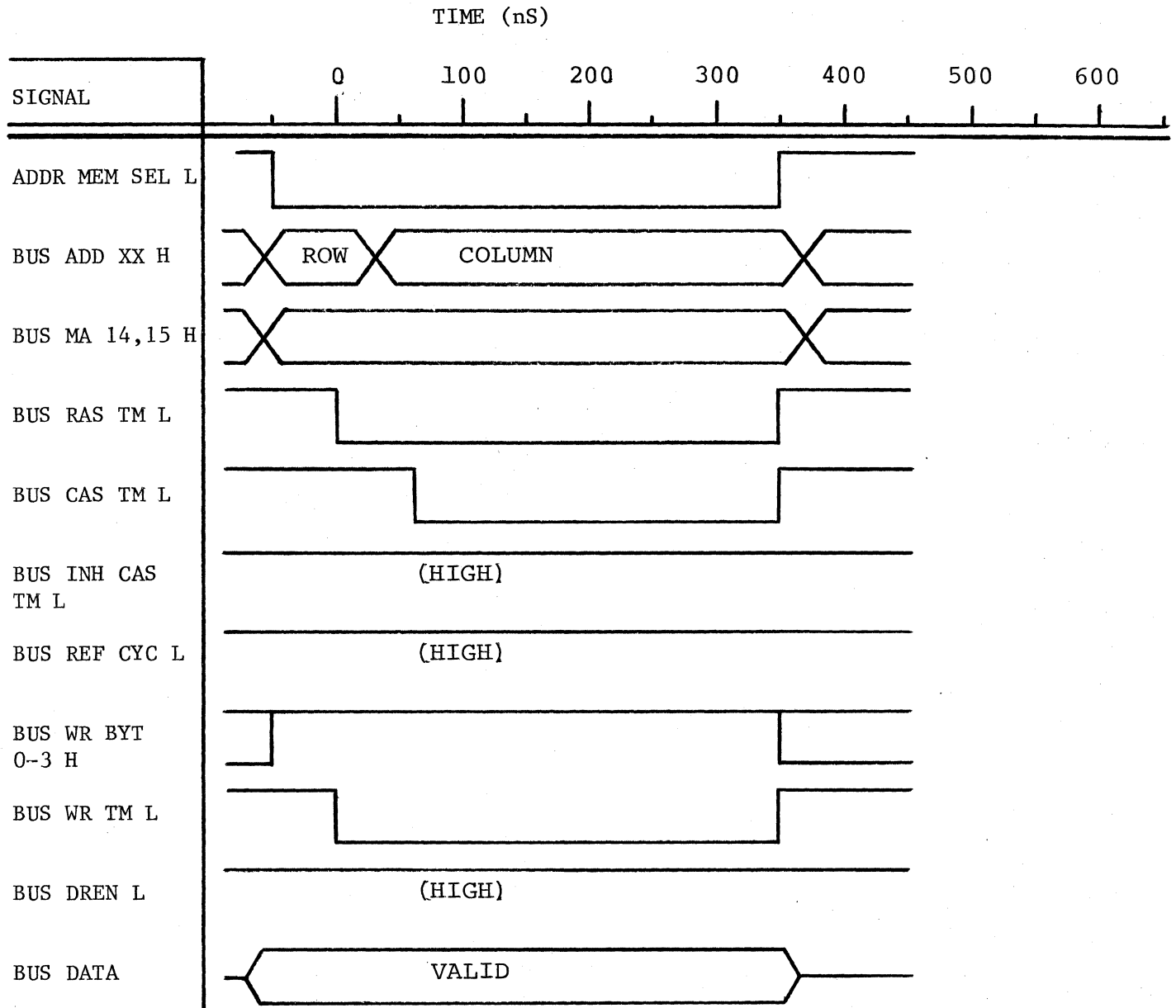


Figure 2-2 (cont.)

INTERFACE TIMING (READ-MODIFY-WRITE)

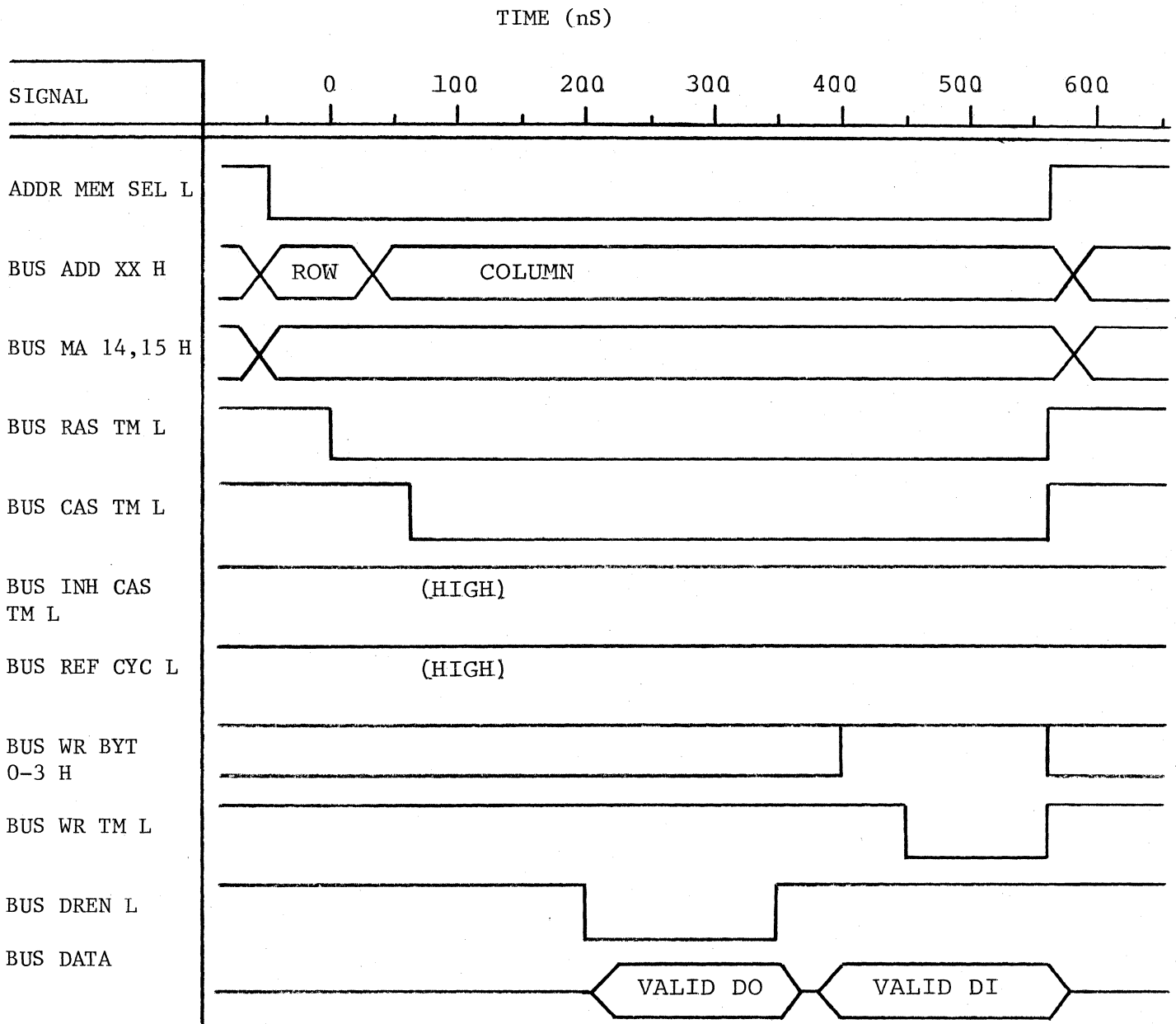


Figure 2-2 (cont.)

INTERFACE TIMING (REFRESH)

TIME (nS)

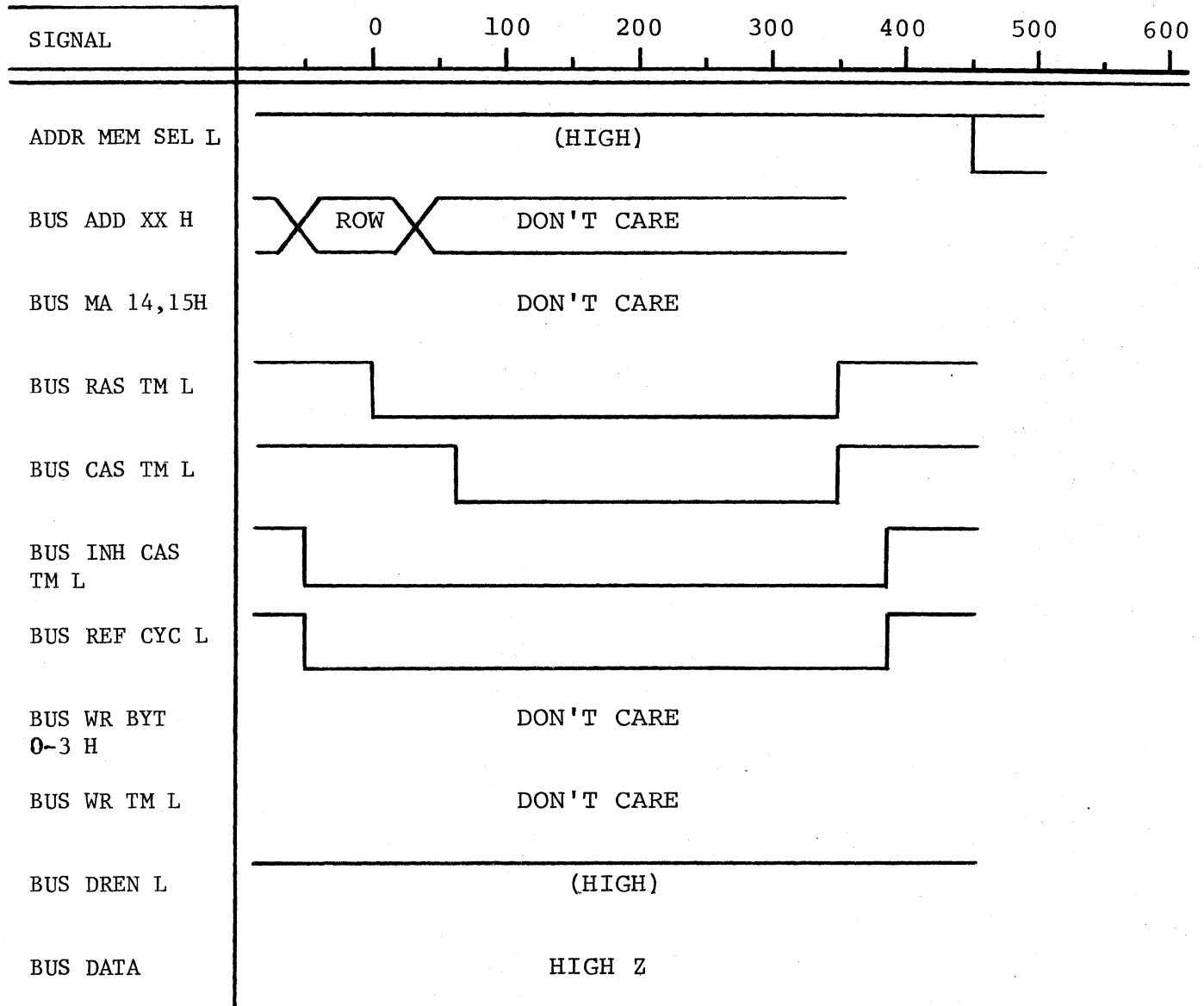


Figure 2-2 (Cont.)

INTERFACE TIMING (INITIALIZE)

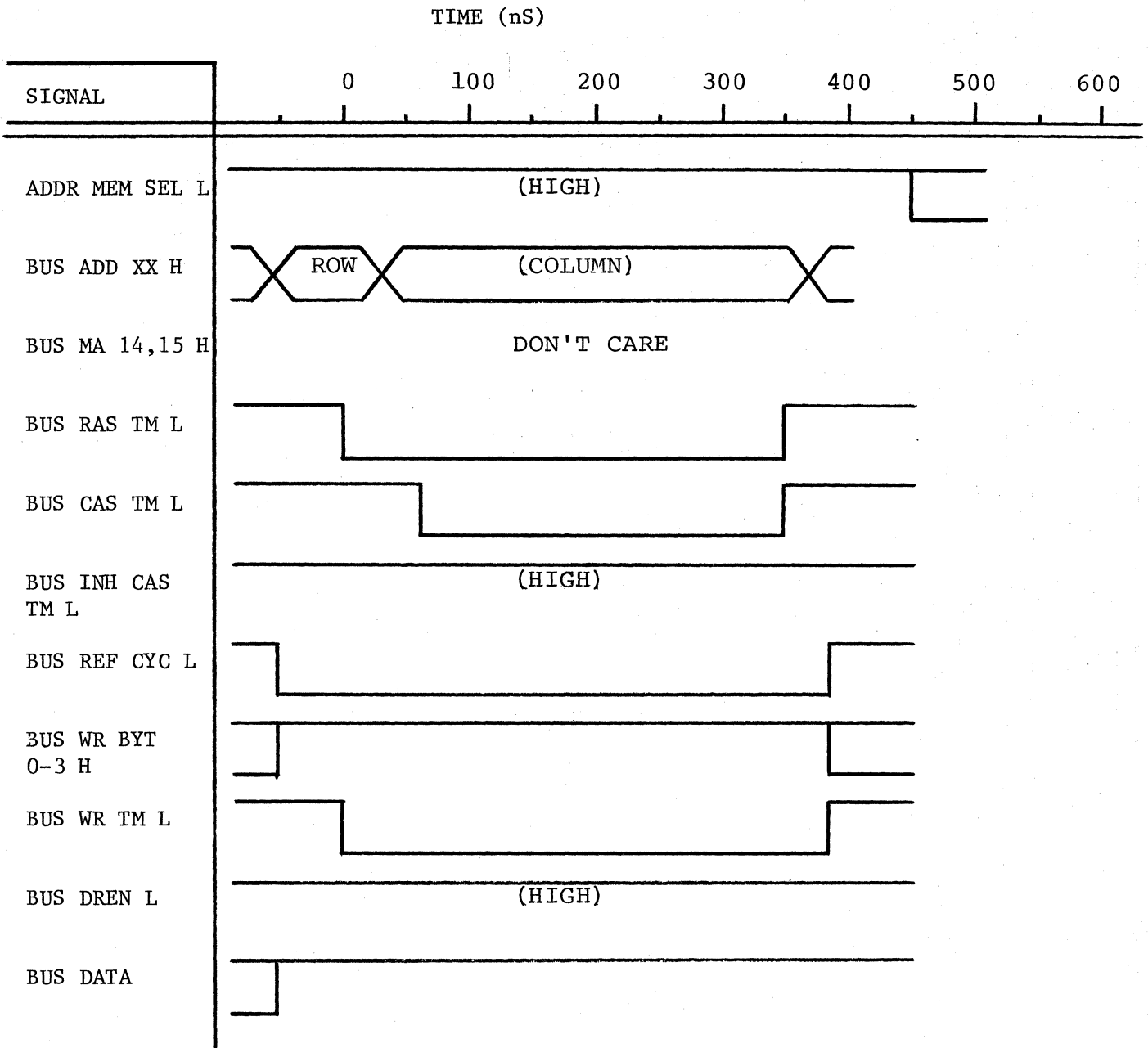


Figure 2-2 (cont.)

SECTION III

INSTALLATION AND MAINTENANCE

3.1 OVERVIEW

This section provides a comprehensive, step-by-step guide for installation of the NS70/75 memory card. Each specific step should be followed to prevent installation errors. Should problems arise, Section IV of this manual gives a detailed outline of the console operation and diagnostic procedure.

3.2 PRELIMINARY PROCEDURE

Inspect all NS70/75 cards for any shipping damage prior to installation. Should any damage be evident, the board should be returned. The address and phone number of the point of origin are listed on the Equipment Maintenance Agreement form, which is included in the shipping container.

Run the following diagnostic program on the PDP-11/70 computer prior to the installation, to insure the system integrity:

Required	-	MEMORY TEST	...	EMKAA0*
Optional	-	CPU INST TEST	..	EQKCB1*
	-	CPU EXER.	EKBAB0*
	-	CPU EXER.	EKBDB0*
	-	CACHE TEST	EKBCB0*
	-	CACHE TEST	EKBDB0*
	-	MEM MAN TEST	...	EKBEB0*

* Diagnostic name denotes typical revision level. Any later revision is also acceptable. The latest revision may be called by substituting "??" for the revision level.

3.3 NS70/75 INSTALLATION

- (1) Set all peripherals to "UNLOAD" condition.
- (2) Turn off power to the memory system. The power control is contained on the MK11 Box Controller. "MEM PWR READY" indicator on the box controller should go out when power is shut off.
- (3) On older PDP-11/70 MK11's, the memory cabinet may have a front door, which will have to be removed. The door is held by spring-loaded pins at the top and bottom of the cabinet.
- (4) The NS70/75 memory cards are directly installable into the MK11 chassis. See Figure 3-1 to determine the location of the storage array slots within the MK11 chassis.

NOTE: THE NS70/75 STORAGE CARD CANNOT OPERATE IN THE DEC MJ11 CORE MEMORY SYSTEM
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The following rules MUST be used to determine the proper storage array slots within the MK11 chassis:

- A. Memories must be installed in sequence, starting from array slot #0. No blank storage array slots are allowed in the sequence.
- B. If mixed chip types are present (4K RAMs and 16K RAMs), all boards with 4K RAMs must be placed in the low numbered slots, and boards with 16K RAMs must be placed in the higher numbered slots.

CARD TYPE

SLOT NO.

1	-----	BLANK	-----
2	-----	STORAGE ARRAY #14	-----
3	-----	STORAGE ARRAY #12	-----
4	-----	STORAGE ARRAY #10	-----
5	-----	STORAGE ARRAY # 8	-----
6	-----	STORAGE ARRAY # 6	-----
7	-----	STORAGE ARRAY # 4	-----
8	-----	STORAGE ARRAY # 2	-----
9	-----	STORAGE ARRAY # 0	-----
10	-----	CONTROL B M8161	-----
11	-----	CONTROL A M8160	-----
12	-----	BLANK	-----
13	-----	ADDRESS BUFFER M8158	-----
14	-----	BLANK	-----
15	-----	DATA BUFFER M8159	-----
16	-----	CONTROL A M8160	-----
17	-----	CONTROL B M8161	-----
18	-----	STORAGE ARRAY #1	-----
19	-----	STORAGE ARRAY #3	-----
20	-----	STORAGE ARRAY #5	-----
21	-----	STORAGE ARRAY #7	-----
22	-----	STORAGE ARRAY #9	-----
23	-----	STORAGE ARRAY # 11	-----
24	-----	STORAGE ARRAY # 13	-----
25	-----	STORAGE ARRAY # 15	-----
26	-----	BLANK	-----

FRONT 

(MK 11 TOP VIEW)
Backplane Slot Location, Figure 3-1

C. Internal interleaving will function automatically if an even number of memories exist in the same chassis. For external interleaving, the same memory capacity must exist in each memory chassis.

(5) Install the NS70/75 memory into the proper slot(s) in the MK11 chassis.

(6) Set the Box Controller "Box AC/Bat Pwr" switch to "ON". The "MEM PWR READY" indicator should come on.

(7) Check the NS70/75 module(s) to ensure they are "ON LINE". The yellow LED should be illuminated on each card. If not, depress the ON/OFF line switch (located at the center of each card) to illuminate the yellow LED.

NOTE: If any NS70/75 memory modules were not "ON LINE" when power was applied, turn the box power OFF and then ON again. This is to insure that the MK11 initializes all of the memories when power is first applied.

(8) Repeat the memory diagnostic test program EMKAA0. Make at least two passes with CPU console switches 11 and 6 UP. If the diagnostic fails, or the system fails to "load" or "boot", refer to Section IV in this manual. The configuration map from diagnostic EMKA will print "SYSTEM SIZE REGISTER LOW DOES NOT MATCH MEMORY", indicating that the system size register has not been changed to accommodate the increased memory size. The rest of the printout should show normal operation.

(9) If the diagnostic will not start or load, check the MK11 controller card error indicators for configuration or parity errors. Figure 3-4 shows the location of the lamps.

3.4 SYSTEM SIZE REGISTER EXPANSION

The PDP-11/70 System Size Register (located in the memory management unit) must be updated any time the memory configuration is changed. This section describes the methods required to reset the system size register.

3.4.1 Existing System Size Register Setting

To find the value of the existing system size register, do the following:

- (1) On the processor front panel
 - Set the HALT/ENABLE switch down.
 - Set the ADDRESS DISPLAY SELECT switch to "CONSOLE PHYSICAL" and the DATA DISPLAY SELECT switch to "DATA PATHS".
 - Set 17 777 760 into the switch register (22 switches).
 - Press "LOAD ADRS", followed by "EXAM". (On systems with no front panel, type CTRL P \$60 /).
 - Read memory system size register contents from the "DATA" display.

- (2) Find the existing memory size (in words) from Table 3-1. Compare this with the configuration printout obtained in Section 3.3 step (8). They should be the same.

- (3) Calculate the final memory size by adding the existing size to the add-in size.
$$\text{FINAL} = \text{EXISTING} + \text{ADD-IN}.$$

READ-OUT (octal)	MEMORY SIZE (K words)	READ-OUT (octal)	MEMORY SIZE (K words)
1 777	32	101 777	1056
3 777	64	103 777	1088
5 777	96	105 777	1120
7 777	128	107 777	1152
11 777	160	111 777	1184
13 777	192	113 777	1216
15 777	224	115 777	1248
17 777	256	117 777	1280
21 777	288	121 777	1312
23 777	320	123 777	1344
25 777	352	125 777	1376
27 777	384	127 777	1408
31 777	416	131 777	1440
33 777	448	133 777	1472
35 777	480	135 777	1504
37 777	512	137 777	1536
41 777	544	141 777	1568
43 777	576	143 777	1600
45 777	608	145 777	1632
47 777	640	147 777	1664
51 777	672	151 777	1696
53 777	704	153 777	1728
55 777	736	155 777	1760
57 777	768	157 777	1792
61 777	800	161 777	1824
63 777	832	163 777	1856
65 777	864	165 777	1888
67 777	896	167 777	1920
71 777	928	171 777	1952
73 777	960	173 777	1984
75 777	992	175 777	2016
77 777	1024	177 777	2048

Table 3-1 PDP-11/70 Memory Size Register
Console Read Out

MEMORY SIZE (Kilowords)	SWITCHES								MEMORY SIZE (Kilowords)	SWITCHES										
	1	2	3	4	5	6	7	8		1	2	3	4	5	6	7	8			
32					1			1		1056					1			1		1
64				1		1		1		1088			1		1			1		1
96	1					1		1		1120	1	1			1			1		1
128	1			1		1		1		1152	1	1		1			1		1	
160					1	1		1		1184				1	1			1		1
192				1	1	1		1		1216			1	1	1			1		1
224	1				1	1		1		1248	1	1			1	1		1		1
256	1			1	1	1		1		1260	1	1		1	1	1		1		1
288						1	1	1		1312				1			1	1	1	
320				1		1	1	1		1344			1		1	1	1	1		
352	1					1	1	1		1376	1	1			1	1	1	1		
384	1			1		1	1	1		1408	1	1		1		1	1	1		
416					1	1	1	1		1440				1	1	1	1	1		
448				1	1	1	1	1		1472			1	1	1	1	1	1		
480	1				1	1	1	1		1504	1	1			1	1	1	1		
512	1			1	1	1	1	1		1536	1	1		1	1	1	1	1		
544				1		1		1		1568		1	1		1			1		1
576				1	1			1		1600		1	1	1		1			1	
608	1			1				1		1632	1	1	1			1			1	
640	1			1	1			1		1644	1	1	1	1		1			1	
672				1		1		1		1696		1	1		1	1			1	
704				1	1	1		1		1728		1	1	1	1	1			1	
736	1			1	1			1		1760	1	1	1		1	1			1	
768	1			1	1	1		1		1792	1	1	1	1	1	1			1	
800				1		1	1	1		1824		1	1		1	1	1		1	
832				1	1			1		1856		1	1	1		1	1	1		
864	1			1				1		1888	1	1	1			1	1	1		
896	1			1	1			1		1920	1	1	1	1		1	1	1		
928				1		1	1	1		1952		1	1		1	1	1	1		
960				1	1	1	1	1		1984		1	1	1	1	1	1	1		
992	1			1	1	1	1	1		2016*	1	1	1		1	1	1	1		
1024	1			1	1	1	1	1		2048*	1	1	1	1	1	1	1	1		

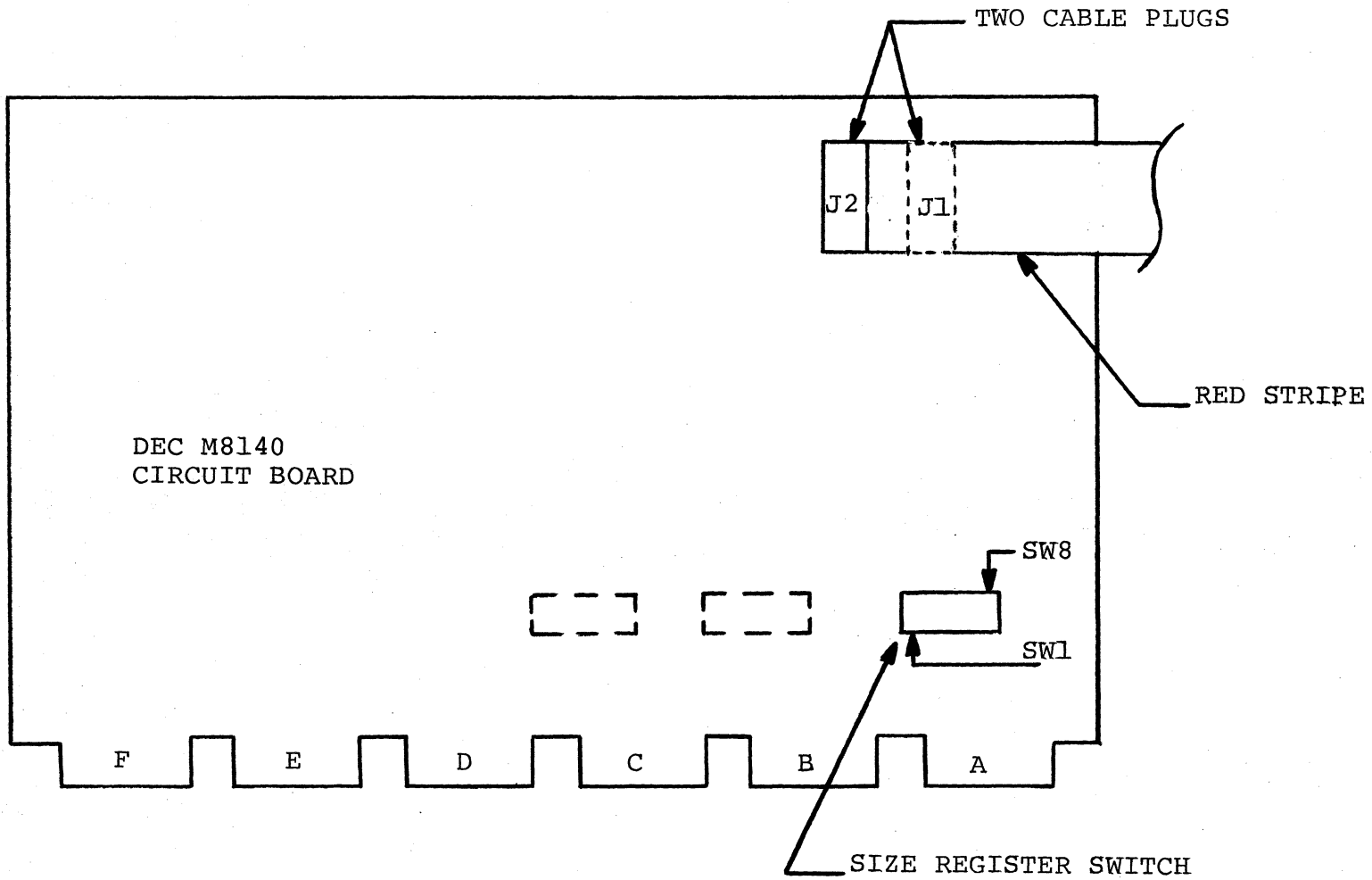
*Not allowed
blank = on
1 = off

Table 3-2. M8140 System Size Register
Switch Settings.

3.4.2 Resetting the System Size Register

- (1) Power down the PDP-11/70 computer and pull out the processor chassis. Remove the left side cover and open the top hatch cover.
- (2) To have access to the switch on card M8140, remove the adjacent M8137, M8138 and M8139 cards.
- (3) The size register switch on M8140 is an 8-position DIP switch located near the top of the card (see Figure 3-2). SW1 is at the bottom of the DIP switch; SW8 is at the top.
- (4) Compare the setting with Table 3-2 for the existing memory size. This will enable the installer to determine the 1's and 0's position of the individual switch.
- (5) Reset the switch settings to the FINAL MEMORY SIZE setting as determined from Table 3-2.
- (6) Re-install the M8137, M8138, and M8139 cards. Use the chart on the top hatch cover to determine the correct order.
- (7) Power on the CPU. Examine the size register per Section 3.4.1. The reading should correspond to the Final Memory Size in Table 3-1. Close the top hatch cover and install the side panel. Slide the CPU chassis back into the frame.

Figure 3-2 M8140 Size Register Switch Location



3.5 FINAL SYSTEM VERIFICATION TEST

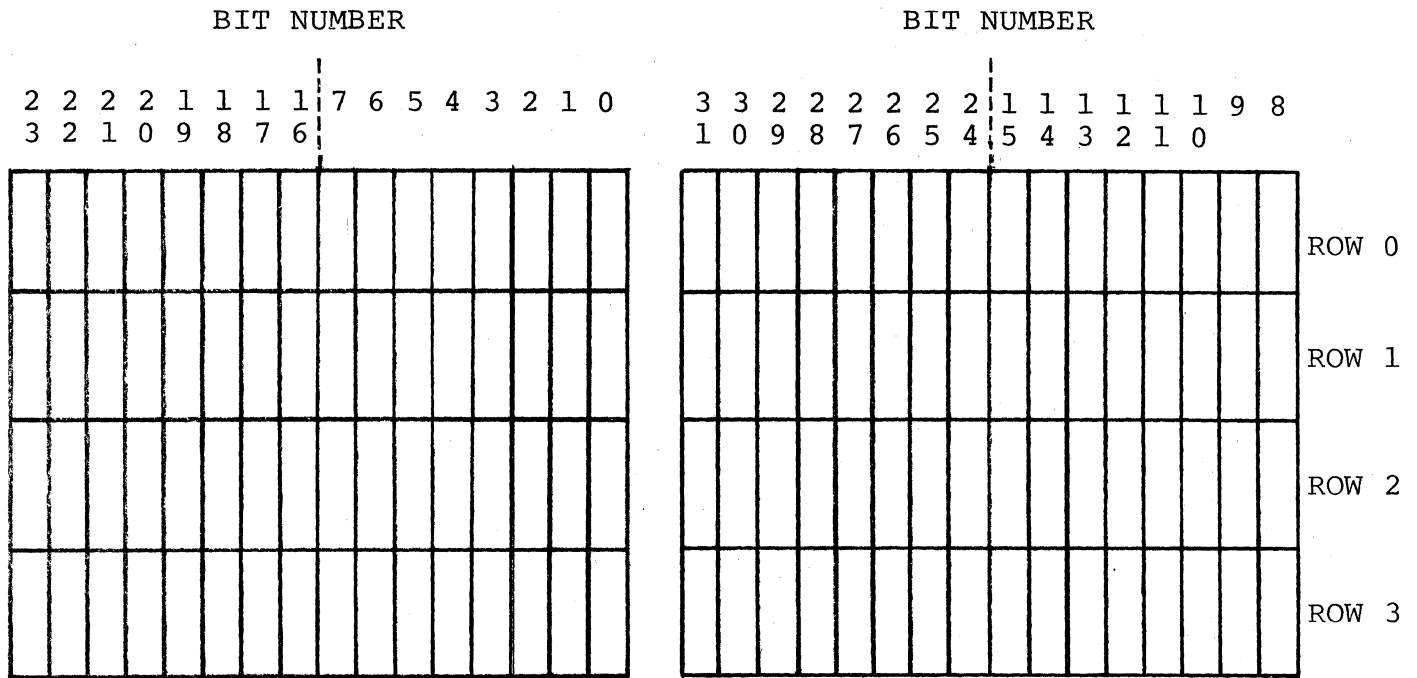
Re-run the same diagnostic programs that were run in Section 3.3 step (8). The configuration printout should now reflect the final memory size.

3.6 MAINTENANCE

The NS70/75 is designed to require no periodic maintenance. Any memory failure can be categorized into one of three failure modes:

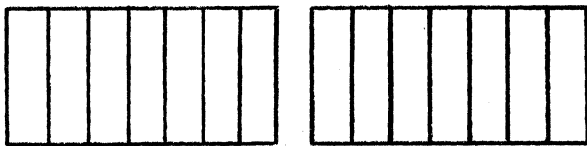
- RAM failure, single bit. The diagnostic procedure outlined in Section IV can point to the bit and row address of a single bit failure. By utilizing the Bit Locator chart, Figure 3-3, the failing RAM can be located and replaced with the on-board spare RAM.
- RAM failure, multiple bits. Unless the diagnostic procedure can isolate the failing RAMs, the board should be returned as per Section 3.2.
- Board inoperative. The board should be returned as per Section 3.2.

NS70/75 BIT MAP



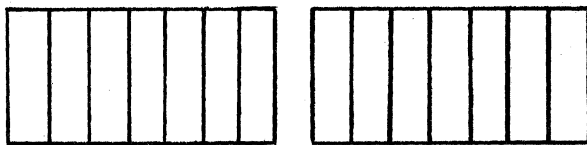
BIT NUMBER

C C C C C C C	C C C C C C C
B B B B B B B	B B B B B B B
T 3 1 8 4 2 1	T 3 1 8 4 2 1
2 6	2 6



ROW 0

ROW 1



ROW 2

ROW 3

Figure 3-3 NS 70/75 BIT LOCATOR CHART

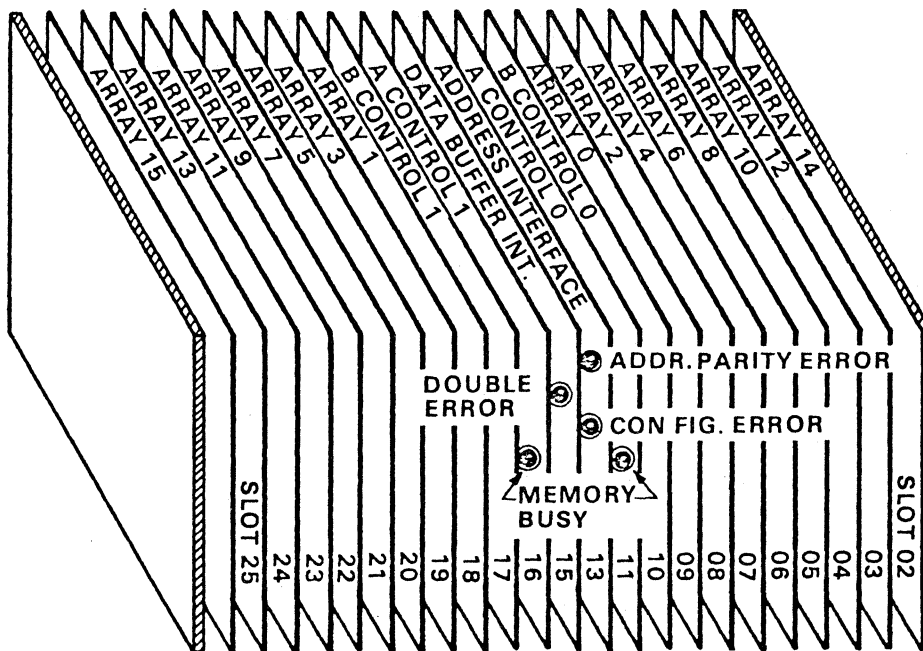


Figure 3-4 MK11 Controller Error Indicators

SECTION IV

CONSOLE AND DIAGNOSTIC PROCEDURE

4.1 CONSOLE OPERATION

The PDP-11/70 console is described in detail in chapter 11 of the PDP-11/70 Processor Handbook. This section of the NS70/75 manual will describe the necessary switch settings to run the memory diagnostics, and the procedure taken to boot the peripheral device containing the diagnostic.

4.1.1 Console Switch Settings

- a) ADDRESS Display Select Switch (8 position). The switch should always be set to "CONS PHY" (console physical).
- b) DATA Display Select Switch (4 position). The switch should always be set to "DATA PATHS".

4.1.2 Error Indicators

The two error indicators on the console front panel are described as follows:

- a) PAR ERR - Indicator is lit when a data parity error has occurred during a memory access.
- b) ADRS ERR - Addressing error. The indicator is on for any of the following error conditions:

An address and command parity error has been detected by memory, or non-existent memory has been accessed.

4.1.3 M9301-YC Bootstrap Loader

The M9301 contains bootstrap routines for a variety of storage media. It allows the bootstrapping of any drive unit on a particular controller, and runs basic diagnostic programs to test the CPU, Cache, and Main Memory.

4.1.4 Starting Procedure

To start operation of the M9301, first set the console switch register to 17765000 and press "LOAD ADRS". Then, set the switch register for the desired storage medium device code and unit number. The device code is set into switches 6-3, and the unit number into switches 2-0.

DEVICE		CODE
TU10	MAG TAPE	1
TU56	DEC TAPE	2
RK05	DISK CARTRIDGE	3
RP03	DISK	4
TU16	MAG TAPE	6
RP04	DISK	7
RS04	FIXED HEAD DISK	10
RX01	FLOPPY DISK	11

EXAMPLE: To boot from unit #1 on a RP04, switches 6-0 should be set to 0 111 001, or 71.

If the device does not properly boot, or another device fails the boot diagnostic routine, the program will halt. The address displayed on the console will index the number of the test that failed. Table 11-2 in the PDP-11/70 Processor Handbook lists the error halts and test descriptions.

4.2 DIAGNOSTIC DESCRIPTION AND PROCEDURE

This section describes the use of the memory diagnostic program EMKA and contains procedures for isolating faults in the memory

system. For a detailed description of the diagnostic program, refer to the diagnostic documentation AC-C644A-MC.

4.1.2 Diagnostic Program

The diagnostic program tests the memory and provides a configuration map, along with error printouts, to isolate memory problems. The operation of the diagnostic can be enhanced by selecting options with the CPU console switch register. A special field service mode allows access to certain routines from the terminal. The diagnostic requires a minimum of 64K words of MOS memory residing in a single box.

4.2.2 Console Switch Register Options

Prior to starting the diagnostic routine, select the desired options with the console switch register. If no console switch register exists, a software switch register may be accessed by typing CTRL G. This displays the current data in the switch register, and accepts new data from the terminal.

<u>CONSOLE SWITCH</u>	<u>OPTION</u>
15	Halt on error
14	Loop on test
13	Inhibit error printout
12	Inhibit relocation
11	Quick verify test
10	Bell on error
9	Loop on error
8	Halt program
7	Detailed error reports
6	Print configuration map
5	Limit no. of error prints
4	Fat terminal
3	Test mode
2	Test mode
1	Test mode
0	Detect single bit errors

- SWITCH 15 - Halts program on error. Allows changing options prior to continuing.
- SWITCH 14 - Causes looping on current test or pattern for an entire bank of memory.
- SWITCH 13 - Disables error message printout.
- SWITCH 12 - Inhibits program from being relocated out of the lowest bank of memory.
- SWITCH 11 - Shortens time required for each pass.
- SWITCH 10 - Bell on the terminal will ring for each error.
- SWITCH 9 - Causes looping from failure point back to last correctly initialized area of current test.
- SWITCH 8 - Halts the program.
- SWITCH 7 - After printing the normal error message, the terminal prints the contents of several registers and the high and low address of the error occurrence.
- SWITCH 6 - After sizing memory, a configuration map is printed. Refer to section 4.2.3 for details.
- SWITCH 5 - Limits the number of error printouts per bank to 10.
- SWITCH 4 - For terminals of 132 columns or wider.
- SWITCHES 3-1 Test Mode. For details on patterns, see the diagnostic documentation.
- SWITCH 0 - Disables error correction for reporting single-bit errors.

4.2.3 Memory Configuration Map

With console switch 6 up, the diagnostic will print the memory configuration map after sizing the memory. The map shows the memory capacity in 16K word banks, the type of interleaving, the type of memory (MOS or core), the box numbers, and the protected banks. The information contained in the map is formatted as follows:

- ERRORS - An X in this row indicates that a single or double bit error occurred in that bank while the sizing routine was writing 0's and 1's.
- ACCESSED - A "1" means that the indicated bank of memory exists. A "0" means that no memory was found at that bank.
- INTRLV - The number in this row (0,2,4 or 8) is the number of ways, internally and externally, that the memory is interleaved.
- 0 = NO INTERLEAVE
 - 2 = INTERNAL INTERLEAVE ONLY
 - 4 = EXTERNAL INTERLEAVE BETWEEN BOXES
 - 8 = INTERNAL AND EXTERNAL INTERLEAVE
- A question mark is printed for non-existent banks.
- MEMTYPE - The letter J or K is printed on this row to indicate the type of memory. J is for MJ11 core memory, and K is for MK11 MOS memory. A "0" indicates no memory present.
- BOX - The box number (0 through 3) corresponding to the CSR address of the box is

Figure 4-2 Configuration Map example 2

```

-----
MEMORY CONFIGURATION MAP
16K WORD BANKS
-----
              1              3              4              5              6              7
01234567012345670123456701234567012345670123456701234567
ERRORS                XXXX
-----
ACCESSED  11111111111111111111111110000000000000000000000000000000000000000000
INTRLV    00000000000000000000000000000000000000000000000000000000000000000000
MEMTYPE   KKKKKKKKKKKKKKKKKKKKKKKKKK00000000000000000000000000000000000000000000
-----
BOX       1111111111111111111111111???????????????????????????????????????????
PROTECT   P P
-----
* ERRORS FOUND
* 384K WORDS OF MEMORY (768KB)
* NO INTERLEAVE
* MOS MEMORY
* 1 BOX (BOX 1)

```

Figure 4-3 Configuration Map example 3

```

-----
MEMORY CONFIGURATION MAP
16K WORD BANKS
-----
              1              2              3              4              5              6              7
01234567012345670123456701234567012345670123456701234567
ERRORS                XX
-----
ACCESSED  11111111111111111111111111111111100000000000000000000000000000000000
INTRLV    22222222222222222000000000000000000000000000000000000000000000000000
MEMTYPE   KKKKKKKKKKKKKKKKKKJJJJJJJJJJJJJJJ00000000000000000000000000000000000000
-----
BOX       00000000000000000000000000000000000000000000000000000000000000000000
PROTECT   P P
-----
* ERRORS FOUND
* 512K WORDS OF MEMORY (1 MB)
* INTERNAL INTERLEAVE - 1 BOX
* MOS AND CORE MEMORY
* 2 BOXES, 1 CSR

```


4.2.4 Control Modes

Certain control modes are available to the operator which can be very useful in determining failures and/or the status of the CPU and associated hardware.

(CTRL) T	Console prints the number of the current test.
(CTRL) C	Stops the current test.
(CTRL) F	Enters the field service mode.
(CTRL) D	Enters the debug mode and allows utilization of ODT commands.
(CTRL) E	Exits the debug mode.

4.2.4.1 Field Service Mode Commands

In the field service mode, the following commands can be used:

0 = EXIT	7 = BATTERY BACKUP TEST
1 = READ CSR	8 = SOB-A-LONG TEST
2 = LOAD CSR	9 = SUPER TIGHT SCOPE LOOP
3 = EXAMINE MEMORY	10 = ERROR SUMMARY
4 = MODIFY MEMORY	11 = REFRESH TEST
5 = SELECT BANK, MARGIN AND PATTERN	12 = REFRESH TERMINAL FILL COUNT
6 = PRINT CONFIGURATION MAP	

A detailed description of each mode can be located in Chapter 9 of the MK11 MOS Memory Technical Manual.

4.2.5 Error Printout

The diagnostic will list any data errors found in the following format:

MEMORY DATA ERROR

```
PC BANK VADD PADD GOOD BAD XOR MAP BOX MTYPE INT PAT ARRAY
xxxxxx xx xxxxxxx xxxxxxxxx xxxxxxx xxxxxxx xxxxxxx x x MK11 x xxx x
```

ERROR PRINTOUT GLOSSARY

PC	Program counter.
BANK	16K word bank number in which the error was found. The bank number also appears in the most significant bits of the PADD.
VADD	Virtual address of the error - always between 60000 and 157776 for mapping purposes.

PADD Physical address of the error. Formatted as the bank number followed by the physical address within the bank. PADD addresses ending in 0 or 4 are for Data Bits 0-15, and addresses ending in 2 or 6 are for Data Bits 16-31.

GOOD Data pattern expected from memory.

BAD Data pattern received from memory.

XOR An exclusive-ORing of GOOD and BAD data.

MAR Margin test number:

0,4,5	= normal
2	= early MDR load
3	= late refresh

BOX Box number corresponding to CSR address.

MTYPE Type of memory; MK11 or MJ11.

INT Number of ways interleaved.

PAT The number of the test pattern.

ARRAY The array module number that contains the error.

The MK11 memory controller can distinguish between memory storage cards in the 16K x 39 bit configuration (4K RAMs), and those in the 64K x 39 bit configuration (16K RAMs).

The following two figures show how a MK11 addressing structure appears in the non-interleaved mode for a box containing only 16K or only 64K memory boards. A box containing both types would be a combination of both figures. Note that when mixing both card types in the same chassis, the 16K x 39 configuration must be installed in the lower numbered array slots (closest to the memory controllers).

The NS70/75 64K x 39 contains 10 Octal (8 decimal) banks. When the MK11 box is internally interleaved, the NS70/75 will contain 20 banks of storage. Determining the correct row in an error printout can be confusing if the box is in the internal interleave mode. Interleaving can be disabled by removing one storage card from the MK11 back plane. The ARRAY slot listed in the error printout will be accurate for any mode.

Figure 4-4

PDP-11/70 ADDRESSING STRUCTURE
MK11 NON-INTERLEAVE
NS70/75 64K x39 BIT MEMORY

11/70 Memory Bus Address

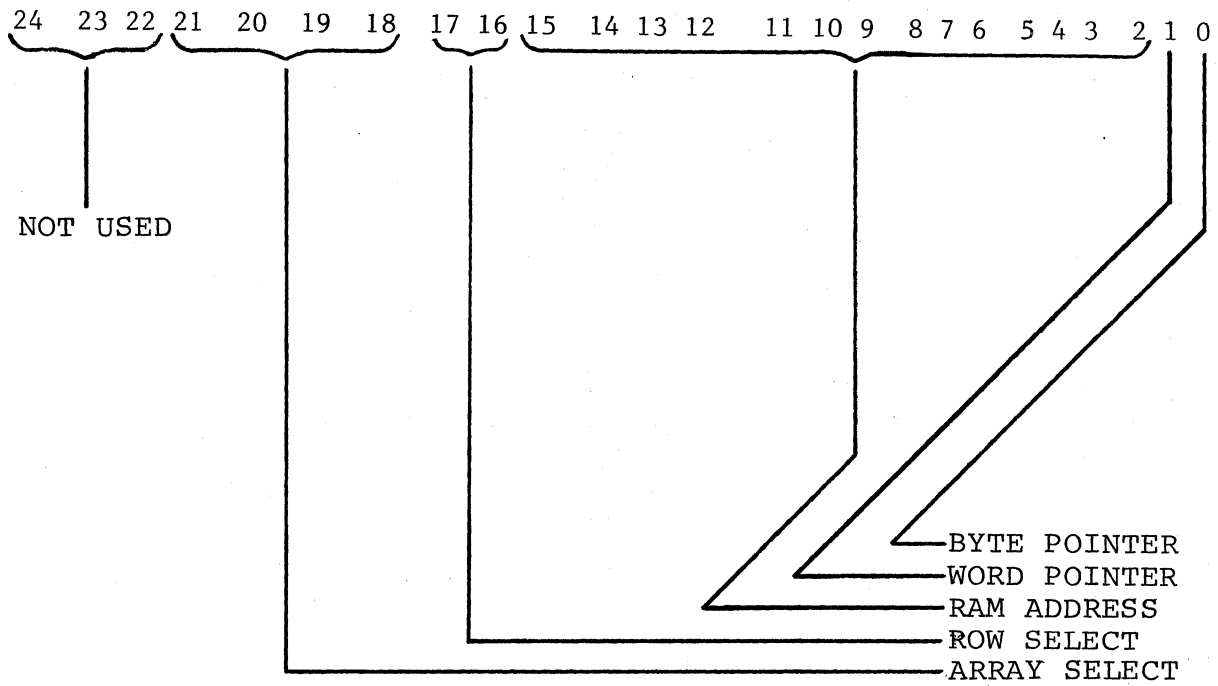


Figure 4-5

PDP-11/70 ADDRESSING STRUCTURE
MK11 NON-INTERLEAVE
16K x 39 BIT MEMORY (4K RAMS)

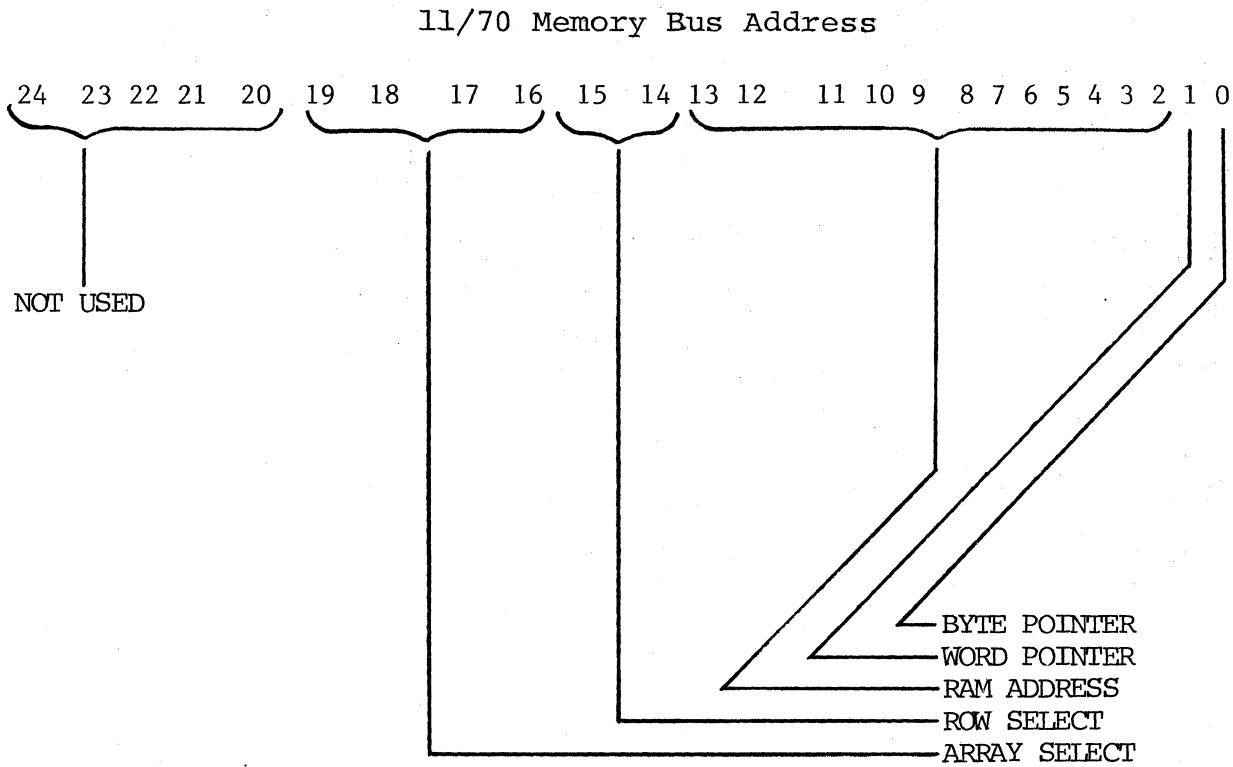


Figure 4-6 Error Printout Example 1

MEMORY DATA ERROR

PC	BANK	VADD	PADD	GOOD	BAD	XOR	MAR	BOX	MTYPE	INT	PAT	ARRAY
026514	4	157774	00477774	000377	000000	000377	0	1	MK11	2	17	1
026514	4	157776	00477776	000377	000000	000377	0	1	MK11	2	17	1

- * THE FAILING MODULE IS IN SLOT #1
- * SINCE PADD ENDS IN 4 AND 6, THE FAILING BITS ARE BITS 16-23.
- * WITH INTERNAL INTERLEAVING, THERE ARE 20 OCTAL BANKS PER ARRAY. THE FAILING ROW IS ROW 0.

Figure 4-7 Error Printout Example 2

MEMORY DATA ERROR

PC	BANK	VADD	PADD	GOOD	BAD	XOR	MAR	BOX	MTYPE	INT	PAT	ARRAY
026050	10	157772	01077772	177777	157777	020000	0	0	MK11	0	017	1

- * THE FAILING MODULE IS IN SLOT #1
- * SINCE PADD ENDS IN 2, THE FAILING BIT IS BIT 13.
- * THE FAILING ROW IS ROW 0.

The failing row can be determined from either Figure 4-4 or from the BANK number. Each RAM row on the MS70/75 contains two banks. Since there are four RAM rows per module, each module contains 10 octal banks. Since there is no interleaving in this example, banks 10 and 11 would reside in RAM row 0 of array #1.

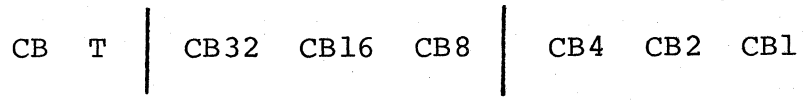
Figure 4-8 Error Printout Example 3

MEMORY DATA ERROR

PC	BANK	VADD	PADD	GOOD	BAD	XOR	MAR	BOX	MTYPE	INT	PAT	ARRAY
026374	33	157750	03377750	000	004	004	0	1	MK11	0	020	3

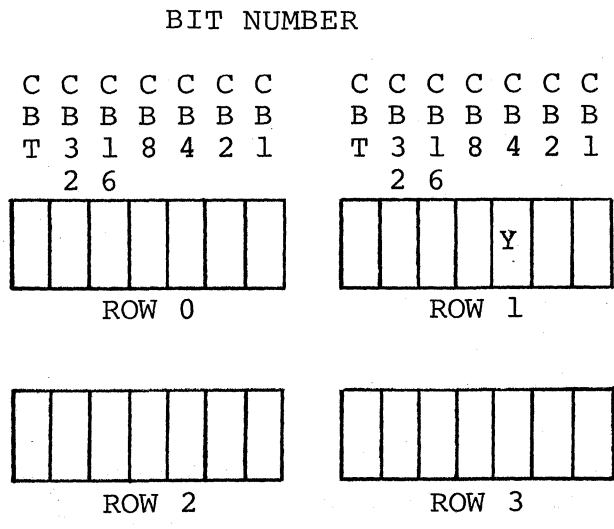
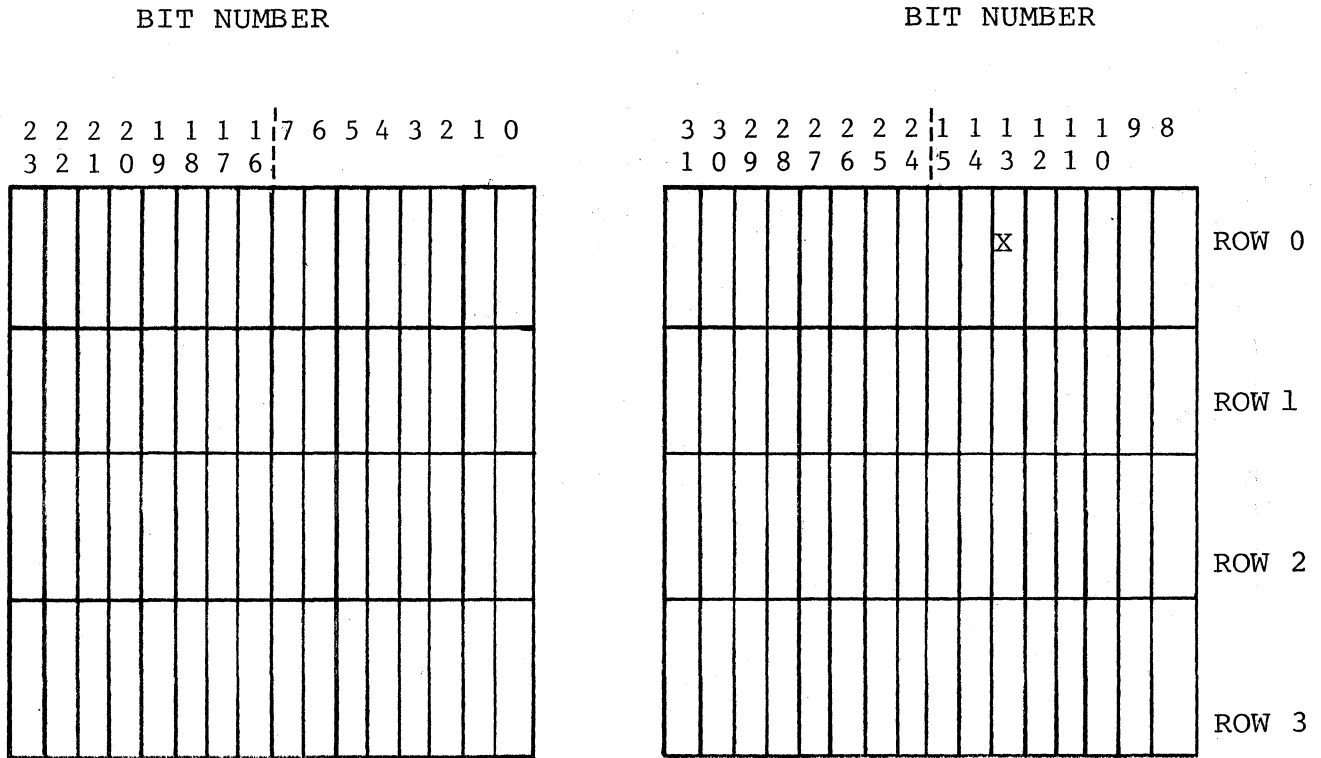
- * TEST OF THE CHECK BITS. PATTERN 20 IS CB TEST.
- * THE ARRAY IS NUMBER 3.
- * THE FAILING BIT IS CHECK BIT 4.
- * THE FAILING ROW IS ROW NUMBER 1.

For check-bit failures, only the seven check bits are printed for the good and bad data. The check-bit placement is as follows:



The row number is derived from the BANK number. Banks 30-37 reside in array number 3, and banks 32-33 reside in RAM row 1.

Figure 4-9 NS70/75 BIT MAP



NOTE: THE FAILING RAM IN ERROR PRINTOUT EXAMPLE 2 IS MARKED WITH A "X". THE FAILURE IN EXAMPLE 3 IS MARKED WITH A "Y".

4.2.6 Utilization of the CSR

Another helpful tool in finding a failing data bit is to examine the information contained in the MK11 CSR. The box CSR contains the data on the last error encountered by that box. To examine the CSR, enter " CTRL F" on the terminal (this allows entry into the Field Service mode), followed by "1 <RET>". If there is more than one CSR present, the terminal will print "WHICH CSR (0-7)". Answer with the desired CSR number followed by <RET>. The terminal will respond by printing both CSR words in octal. Figure 4-10 provides a definition of the CSR words.

Figure 4-10 Control and Status Registers

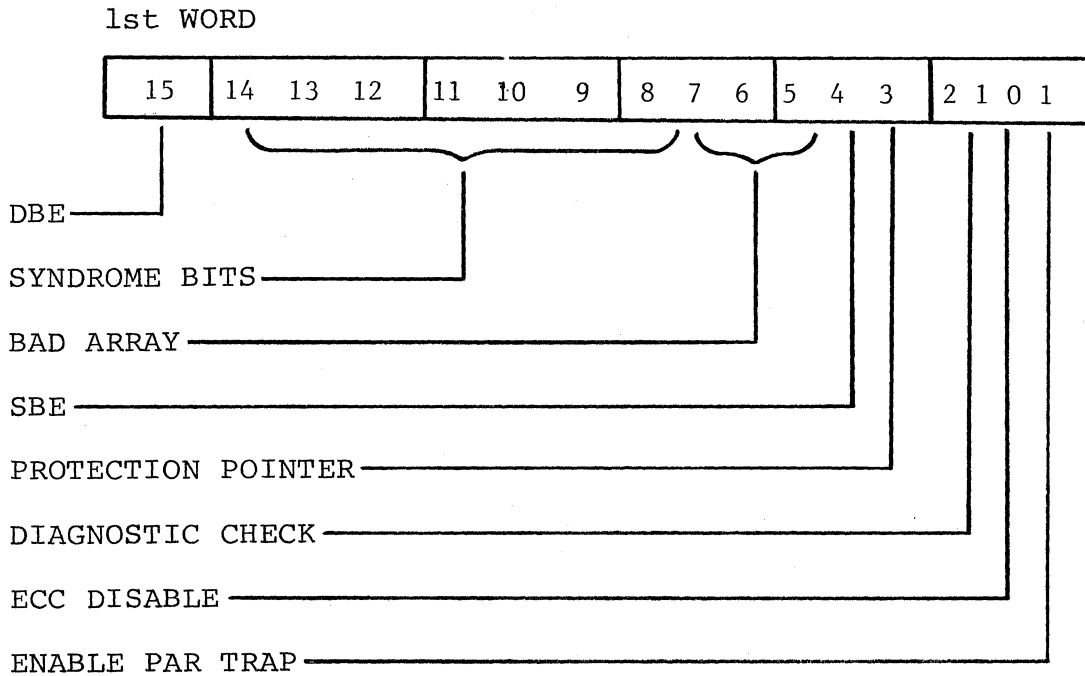


Figure 4-10 Continued

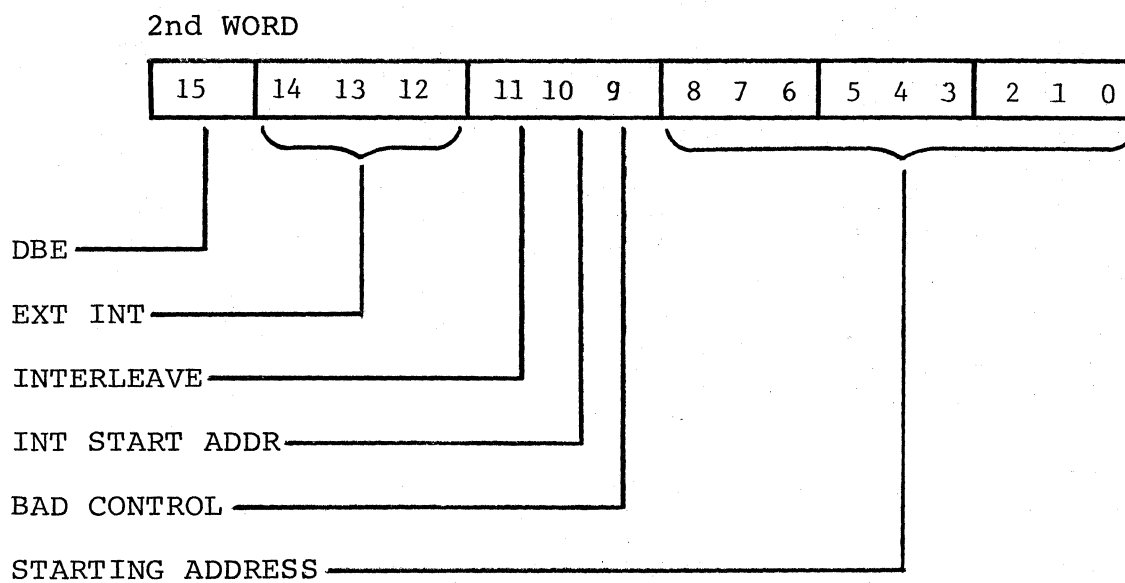


Table 4-1 contains the CSR syndrome table, which can be used to decode single bit errors. The table is only applicable if bit 15 (Double Bit Error) is not set in either CSR word.

Table 4-1 CSR (Word 1) Syndrome Table

MEMORY DATA BIT	CSR BITS							OCTAL PRINTOUT RANGE
	14	13	12	11	10	9	8	
0	1	0	1	1	0	0	0	0540XX-0543XX
1	0	0	1	1	0	0	1	0144XX-0147XX
2	0	0	1	1	0	1	0	0150XX-0153XX
3	1	0	1	1	0	1	1	0554XX-0557XX
4	0	0	1	1	1	0	0	0160XX-0163XX
5	1	0	1	1	1	0	1	0564XX-0567XX
6	1	0	1	1	1	1	0	0570XX-0573XX
7	0	0	1	1	1	1	1	0174XX-0177XX
8	1	1	0	1	0	0	0	0640XX-0643XX
9	0	1	0	1	0	0	1	0244XX-0247XX
10	0	1	0	1	0	1	0	0250XX-0253XX
11	1	1	0	1	0	1	1	0654XX-0657XX
12	0	1	0	1	1	0	0	0260XX-0263XX
13	1	1	0	1	1	0	1	0664XX-0667XX
14	1	1	0	1	1	1	0	0670XX-0673XX
15	0	1	0	1	1	1	1	0274XX-0277XX
16	1	1	1	0	0	0	0	0700XX-0703XX
17	0	1	1	0	0	0	1	0304XX-0307XX
18	0	1	1	0	0	1	0	0310XX-0313XX
19	1	1	1	0	0	1	1	0714XX-0717XX
20	0	1	1	0	1	0	0	0320XX-0323XX
21	1	1	1	0	1	0	1	0724XX-0727XX
22	1	1	1	0	1	1	0	0730XX-0733XX
23	0	1	1	0	1	1	1	0334XX-0337XX
24	0	1	1	1	0	0	0	0340XX-0343XX
25	1	1	1	1	0	0	1	0744XX-0747XX
26	1	1	1	1			0	0750XX-0753XX
27	0	1	1	1	0	1	1	0354XX-0357XX
28	1	1	1	1	1	0	1	0760XX-0763XX
29	0	1	1	1	1	0	1	0364XX-0367XX
30	0	1	1	1	1	1	0	0370XX-0373XX
31	1	1	1	1	1	1	1	0774XX-0777XX
CB 1	0	0	0	0	0	0	1	0004XX-0007XX
CB 2	0	0	0	0	0	1	0	0010XX-0013XX
CB 4	0	0	0	0	1	0	0	0020XX-0023XX
CB 8	0	0	0	1	0	0	0	0040XX-0043XX
CB16	0	0	1	0	0	0	0	0100XX-0103XX
CB32	0	1	0	0	0	0	0	0200XX-0203XX
CB T	1	0	0	0	0	0	0	0400XX-0403XX

SECTION V

APPENDIX A

This appendix contains the schematic, assembly drawing and bill of materials pertaining to the NS70/75 memory card.

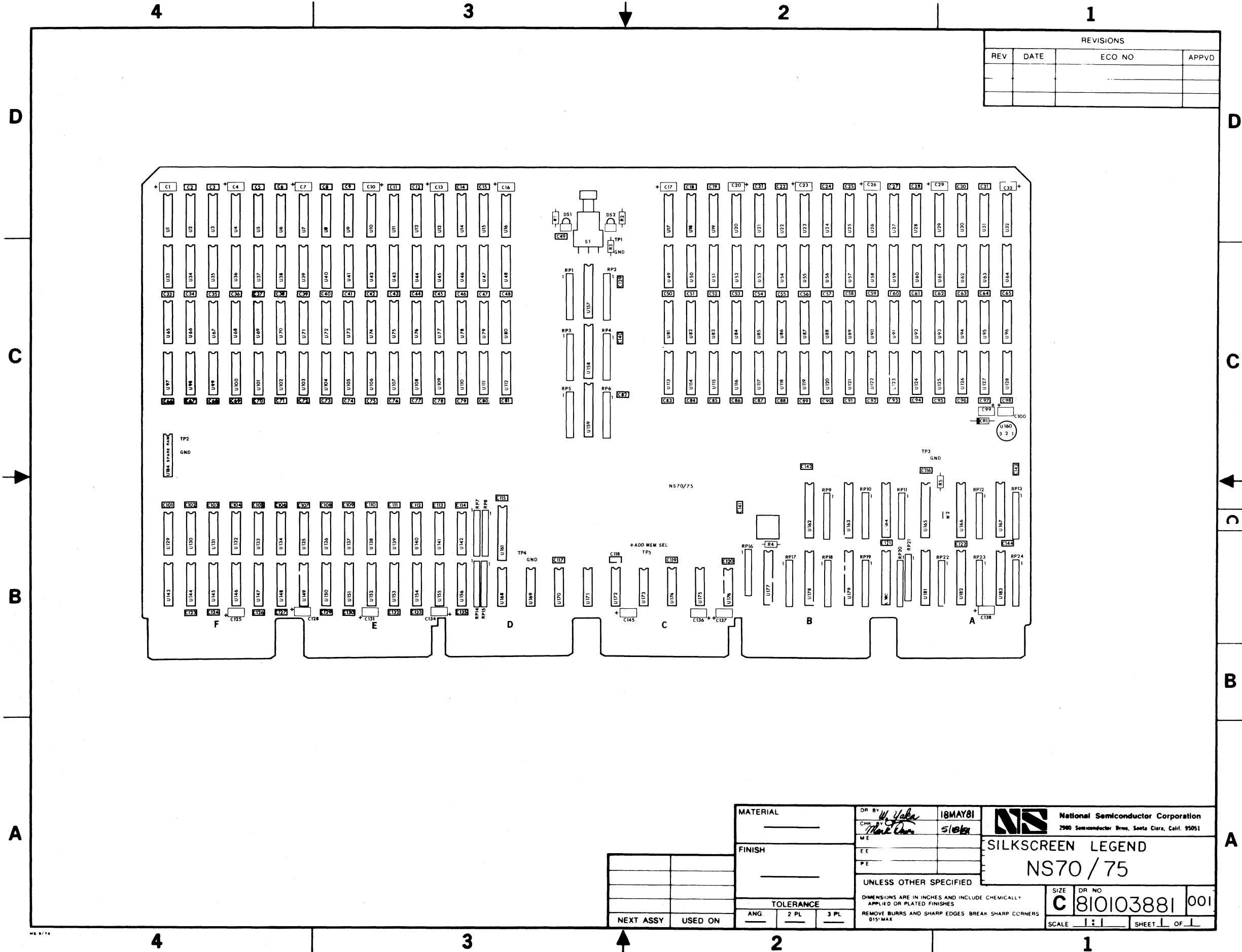
980103881 Assembly Drawing and Bill of Materials

870103881 Schematic Diagram

ITEM FIND NO	QUANTITY PER ASSEMBLY										UNIT OF MEAS	EA: EACH OF = IN: INCH FT: FEET	BK: BULK AR: AS REQ'D	BILL OF MATERIALS NO.		
														980103881 - 000		
														DESCRIPTION	REF DESIGNATOR	
1																
2																
3																
4																
5																
6																
7																
8																
9																
10																
11																
12																
13																
14																
15																
16																
17																
18																
19																
20																
21																
22																
REV	A	B											NOTES:	TITLE		
CHG NO	100	100												NS 70/75		
DATE	3/19/81	3/18/81												1/4 MB STORAGE CARD		
APPR	SLC	JCS														
PREPARED BY	CHECKED BY	APPROVED BY	National Semiconductor Corporation										SIZE	BILL OF MATERIALS NO.	SH	
DATE	DATE	DATE	2900 Semiconductor Drive										A	980103881 - 000	3	
3-19-81			Santa Clara, Calif. 95051												OF	

ITEM FIND NO	QUANTITY PER ASSEMBLY										UNIT OF MEAS	EA: EACH OF = IN: INCH FT: FEET	BK: BULK AR: AS REQ'D	BILL OF MATERIALS NO.		
														980103881 - 000		
														DESCRIPTION	REF DESIGNATOR	
23																
24																
25																
26																
27																
28																
29																
30																
31																
32																
33																
34																
35																
36																
37																
38																
39																
40																
41																
42																
43																
44																
REV	A	B											NOTES:	TITLE		
CHG NO	100	100												NS 70/75		
DATE	3/19/81	3/18/81												1/4 MB STORAGE CARD		
APPR	SLC	JCS														
PREPARED BY	CHECKED BY	APPROVED BY	National Semiconductor Corporation										SIZE	BILL OF MATERIALS NO.	SH	
DATE	DATE	DATE	2900 Semiconductor Drive										A	980103881 - 000	3	
3-19-81			Santa Clara, Calif. 95051												OF	

ITEM FIND NO	QUANTITY PER ASSEMBLY										UNIT OF MEAS	EA: EACH OF = IN: INCH FT: FEET	BK: BULK AR: AS REQ'D	BILL OF MATERIALS NO.		
														980103881 - 000		
														DESCRIPTION	REF DESIGNATOR	
45																
46																
47																
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61																
62																
63																
64																
65																
66																
REV	A	B											NOTES:	TITLE		
CHG NO	100	100												NS 70/75		
DATE	3/19/81	3/18/81												1/4 MB STORAGE CARD		
APPR	SLC	JCS														
PREPARED BY	CHECKED BY	APPROVED BY	National Semiconductor Corporation										SIZE	BILL OF MATERIALS NO.	SH	
DATE	DATE	DATE	2900 Semiconductor Drive										A	980103881 - 000	3	
3-19-81			Santa Clara, Calif. 95051												OF	



REVISIONS			
REV	DATE	ECO NO	APPVD

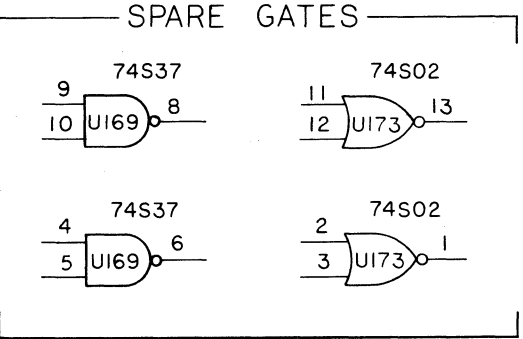
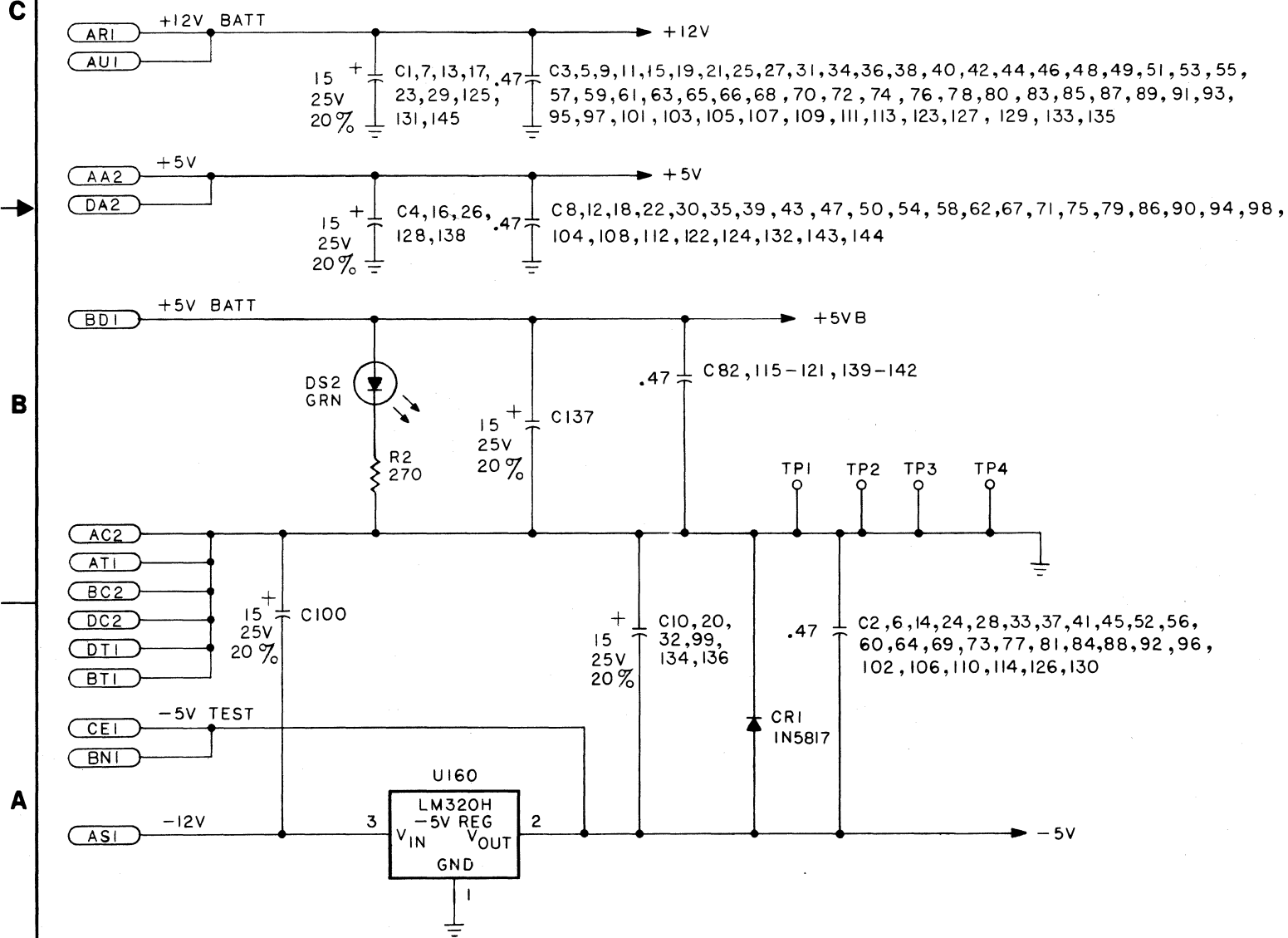
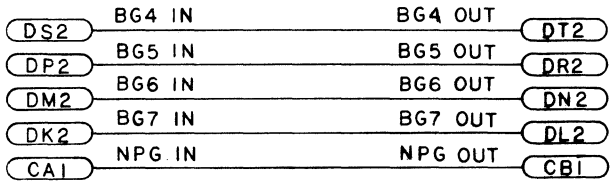
MATERIAL	DR BY	18MAY81	 National Semiconductor Corporation 2900 Semiconductor Drive, Santa Clara, Calif. 95051
	CHKD	5/18/81	
FINISH	ME		SILKSCREEN LEGEND NS70/75
	EE		
TOLERANCE	PE		UNLESS OTHER SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES REMOVE BURRS AND SHARP EDGES BREAK SHARP CORNERS 015-MAX
	ANG		
NEXT ASSY	USED ON		SIZE C DR NO 810103881 001 SCALE 1:1 SHEET 1 OF 1

8 7 6 5 4 3 2 1

REVISIONS			
REV	DATE	ECO NO.	APPVD
A	3/28/81	PCO 24085	SLS

REFERENCE DESIGNATION	
LAST USED	NOT USED
CI45	
CR1	
DS2	
R5	
RP24	
S1	
TP5	
UI83	
W2	W1

VOLTAGE TABLE					
TYPE	+5V	+5VB	-12V	GND	REFERENCE DESIGNATION
LM320H			3	1	UI60
3628		20		10	UI57-159,161
74S02		14		7	UI70-173
74S04		14		7	UI74
74S06		14		7	UI76
74S10		14		7	UI75
74S37		14		7	UI68,169
74LS240		20		10	UI62,164,178,180,181
74S241		20		10	UI65
74LS240	20			10	UI66,167,182,183
74LS241		20		10	UI77



NOTES: UNLESS OTHERWISE SPECIFIED.
 1. RESISTANCE VALUES ARE IN OHMS, 1/8W, ±5%.
 2. CAPACITANCE VALUES ARE IN MICROFARADS, 50V, ±10%.

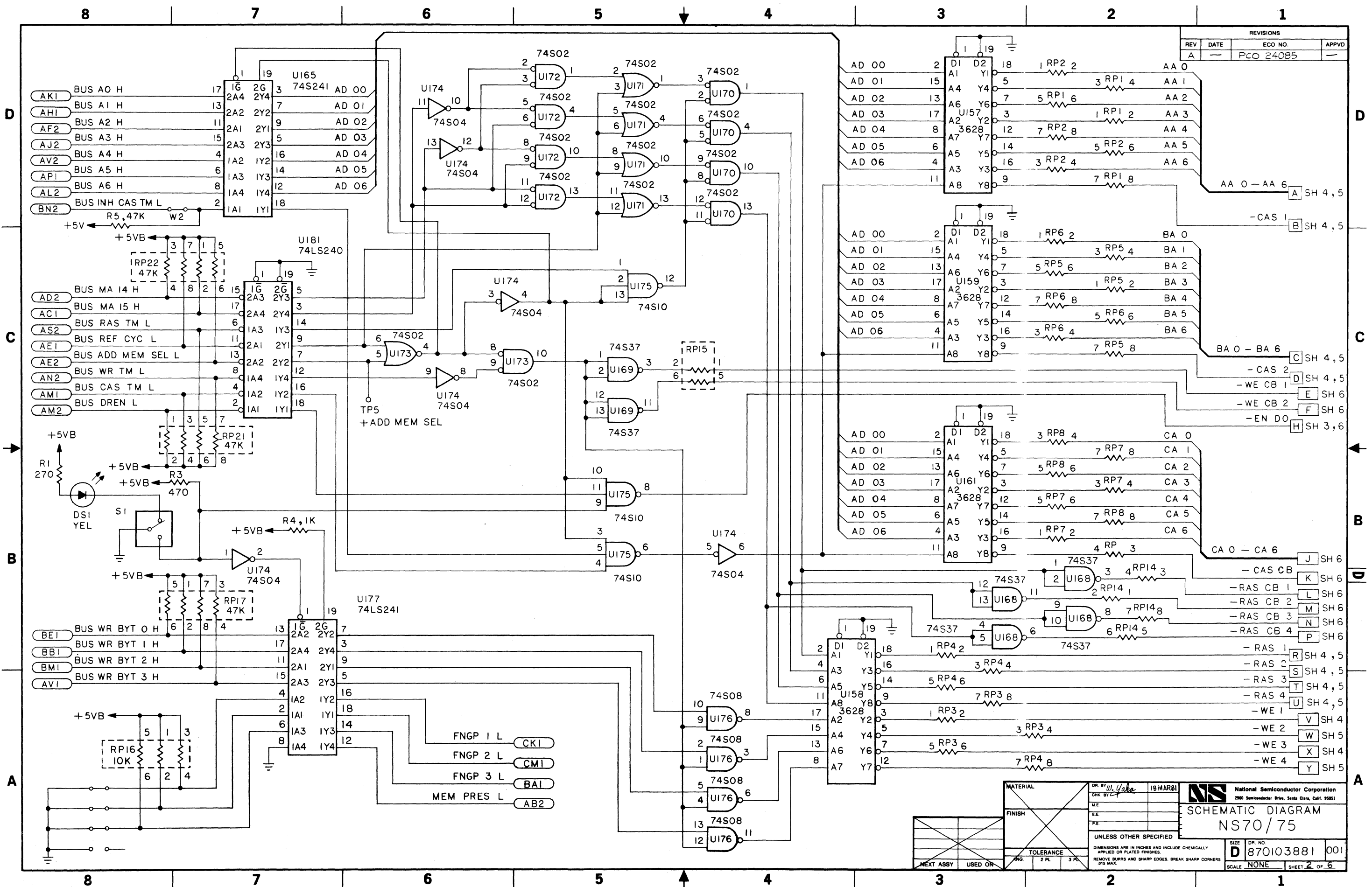
D
C
B
A

D
C
B
A

8 7 6 5 4 3 2 1

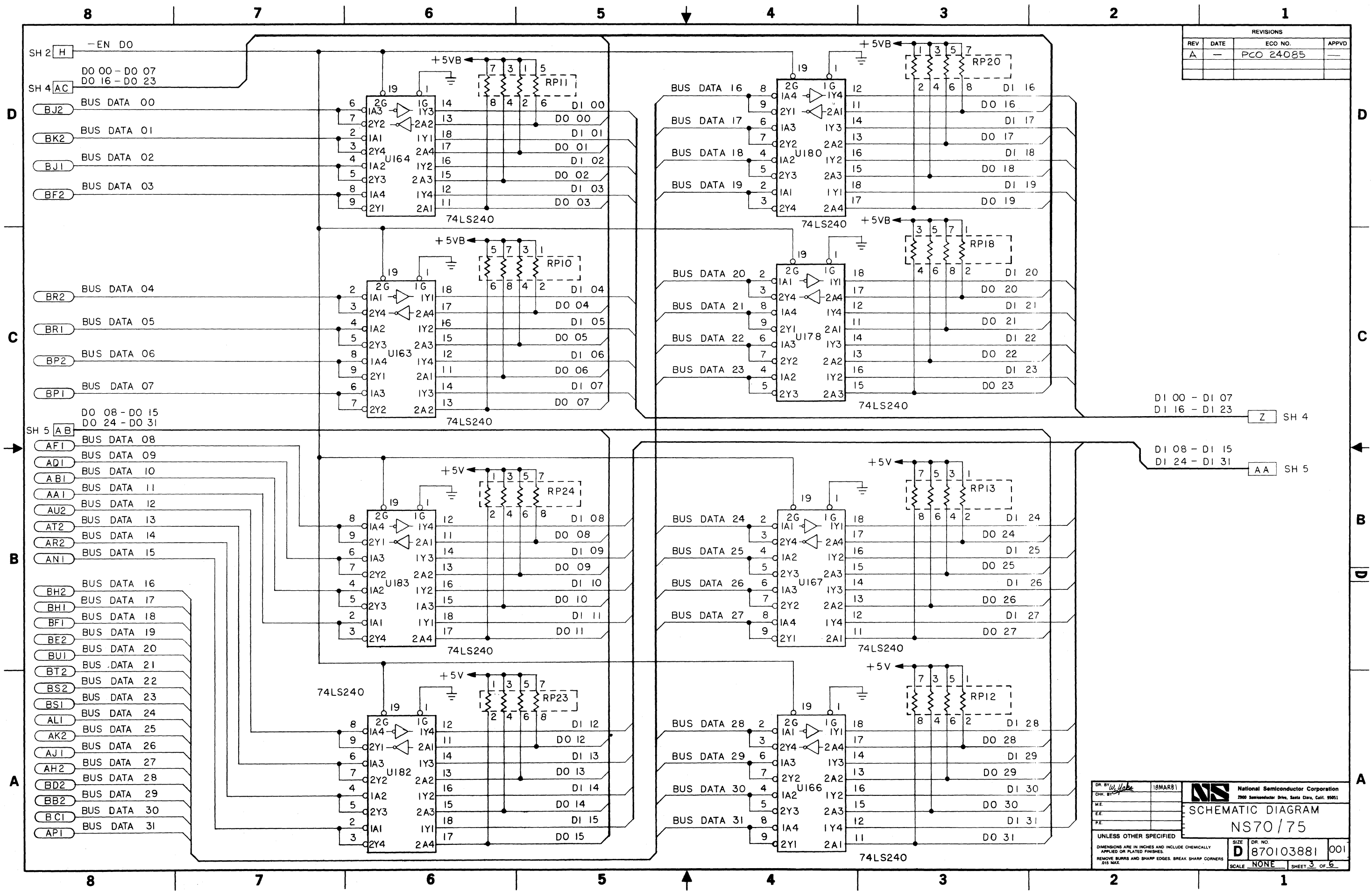
MATERIAL	DR. BY <i>U. Yeh</i>	18MAR81	 National Semiconductor Corporation 2900 Semiconductor Drive, Santa Clara, Calif. 95051
FINISH	EE <i>SLS</i>	3/28/81	
UNLESS OTHER SPECIFIED			
DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES. REMOVE BURRS AND SHARP EDGES. BREAK SHARP CORNERS .010 MAX.			SIZE DR. NO. D 870103881 001 SCALE NONE SHEET 1 OF 6
NEXT ASSY	USED ON	ANG.	TOLERANCE
		2 PL.	3 PL.

REVISIONS			
REV	DATE	ECO NO.	APPVD
A		PCO 24085	



MATERIAL	DR BY <i>W. Yabe</i>	18 MAR 81	 National Semiconductor Corporation 2900 Semiconductor Drive, Santa Clara, Calif. 95051
FINISH	CHK BY <i>W. Yabe</i>		
SCHEMATIC DIAGRAM NS70/75			DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES. REMOVE BURRS AND SHARP EDGES. BREAK SHARP CORNERS 915 MAX.
UNLESS OTHERWISE SPECIFIED TOLERANCE DIM: .010 2 PL 3 PL SCALE NONE SHEET 2 OF 6			

REVISIONS			
REV	DATE	ECO NO.	APPROV
A		PCO 24085	

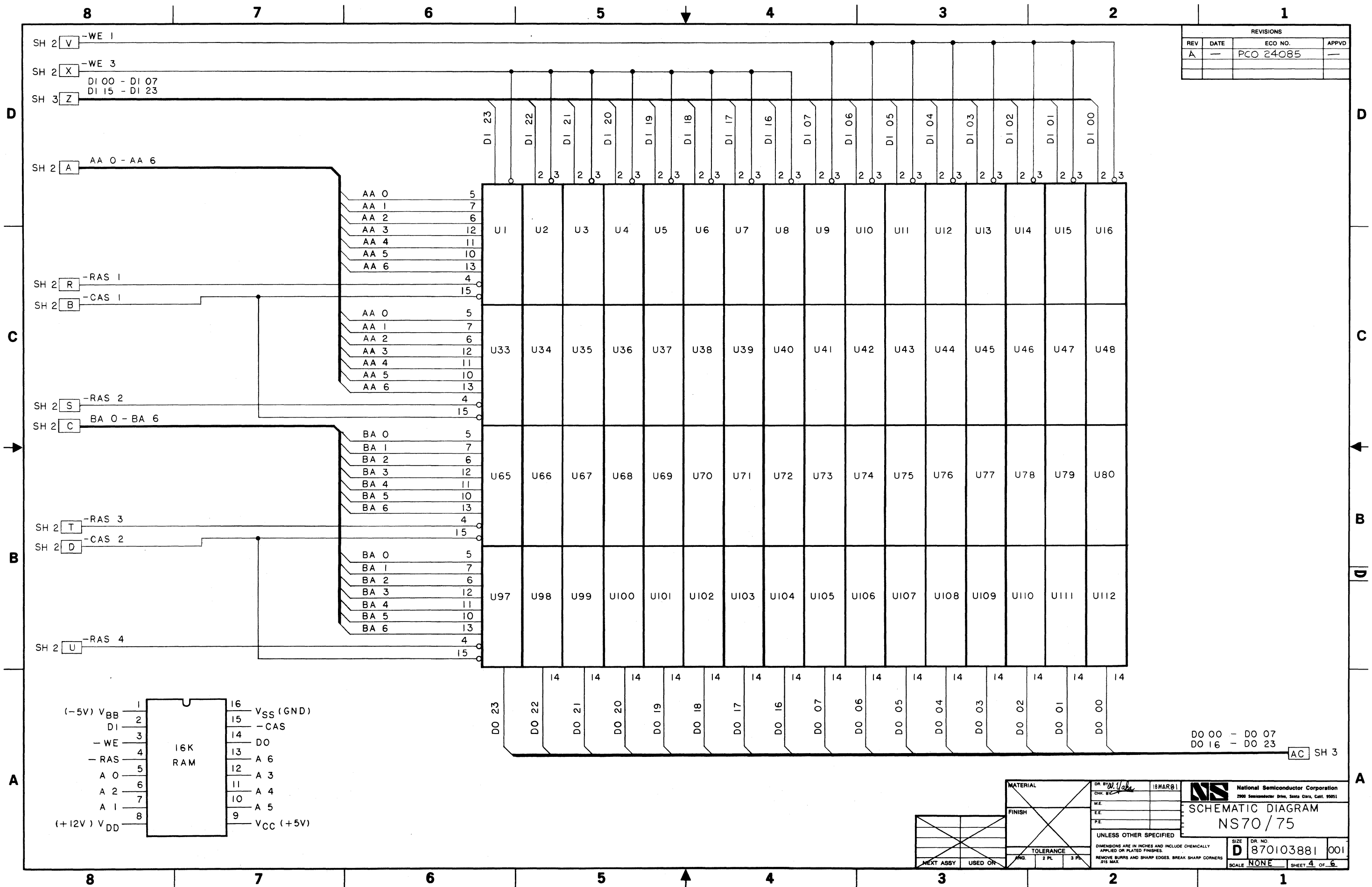


DI 00 - DI 07
DI 16 - DI 23

DI 08 - DI 15
DI 24 - DI 31

DR. BY <i>W. H. Hake</i>	18MAR81	 National Semiconductor Corporation 2900 Semiconductor Drive, Santa Clara, Calif. 95051	SCHEMATIC DIAGRAM NS70/75
CHK. BY			
ME		UNLESS OTHER SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES. REMOVE BURRS AND SHARP EDGES. BREAK SHARP CORNERS .015 MAX.	
EE		SIZE D DR. NO. 870103881 001	SCALE NONE SHEET 3 OF 5

REVISIONS			
REV	DATE	ECO NO.	APPVD
A	-	PCO 24085	-

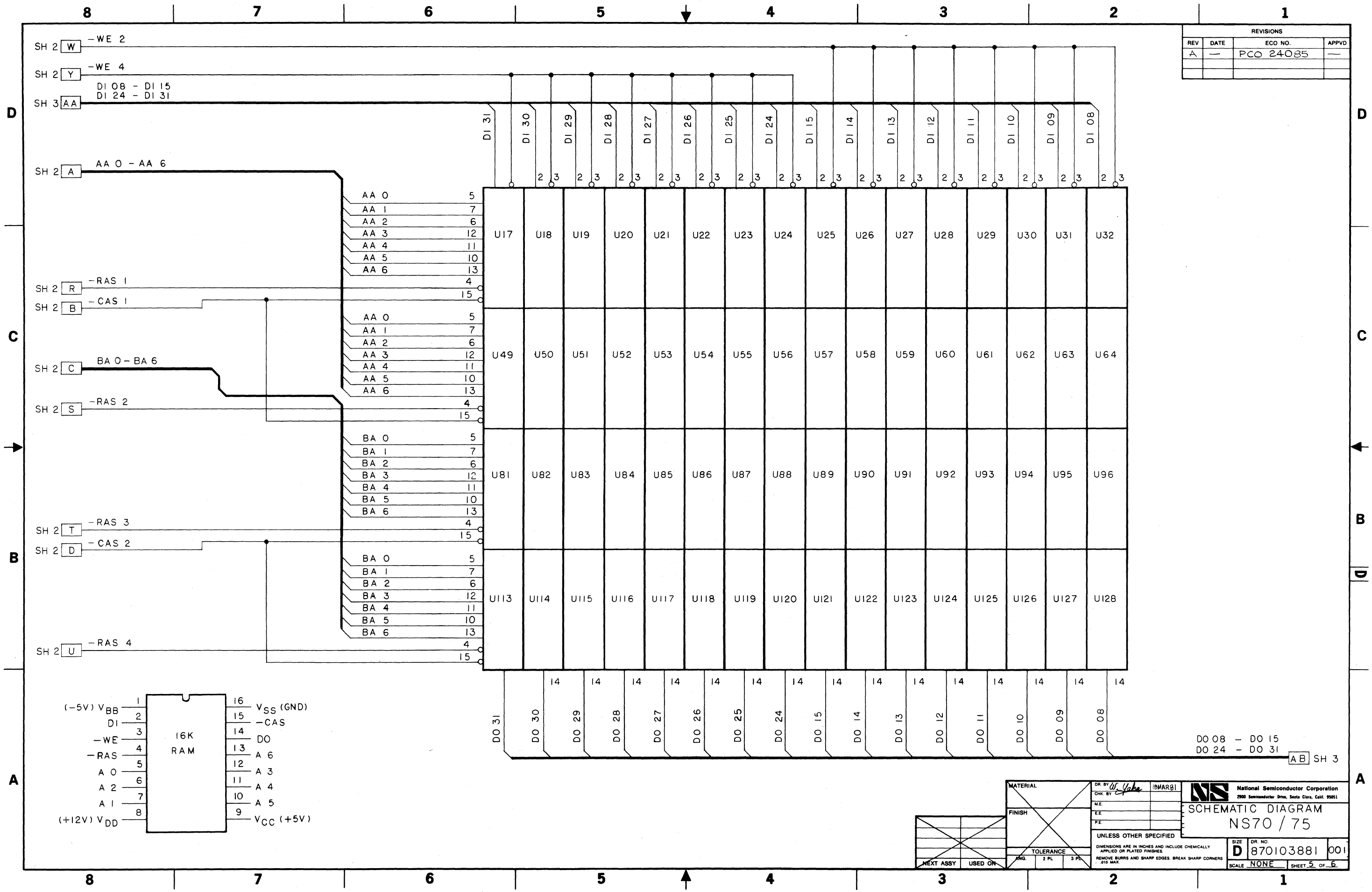


DO 00 - DO 07
DO 16 - DO 23

AC SH 3

MATERIAL	DR BY: <i>W. Yaba</i>	18MAR81	 National Semiconductor Corporation 2900 Semiconductor Drive, Santa Clara, Calif. 95051
FINISH	M.E.		
	E.E.		
	P.E.		
UNLESS OTHERWISE SPECIFIED			DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES. REMOVE BURRS AND SHARP EDGES. BREAK SHARP CORNERS 25 MAX.
TOLERANCE ANG. 2 PL 3 PL			
NEXT ASSY		USED ON	SIZE DR. NO. D 870103881 001 SCALE NONE SHEET 4 OF 6

REVISIONS			
REV	DATE	ECO NO.	APPVD
A	-	PCO 24085	-

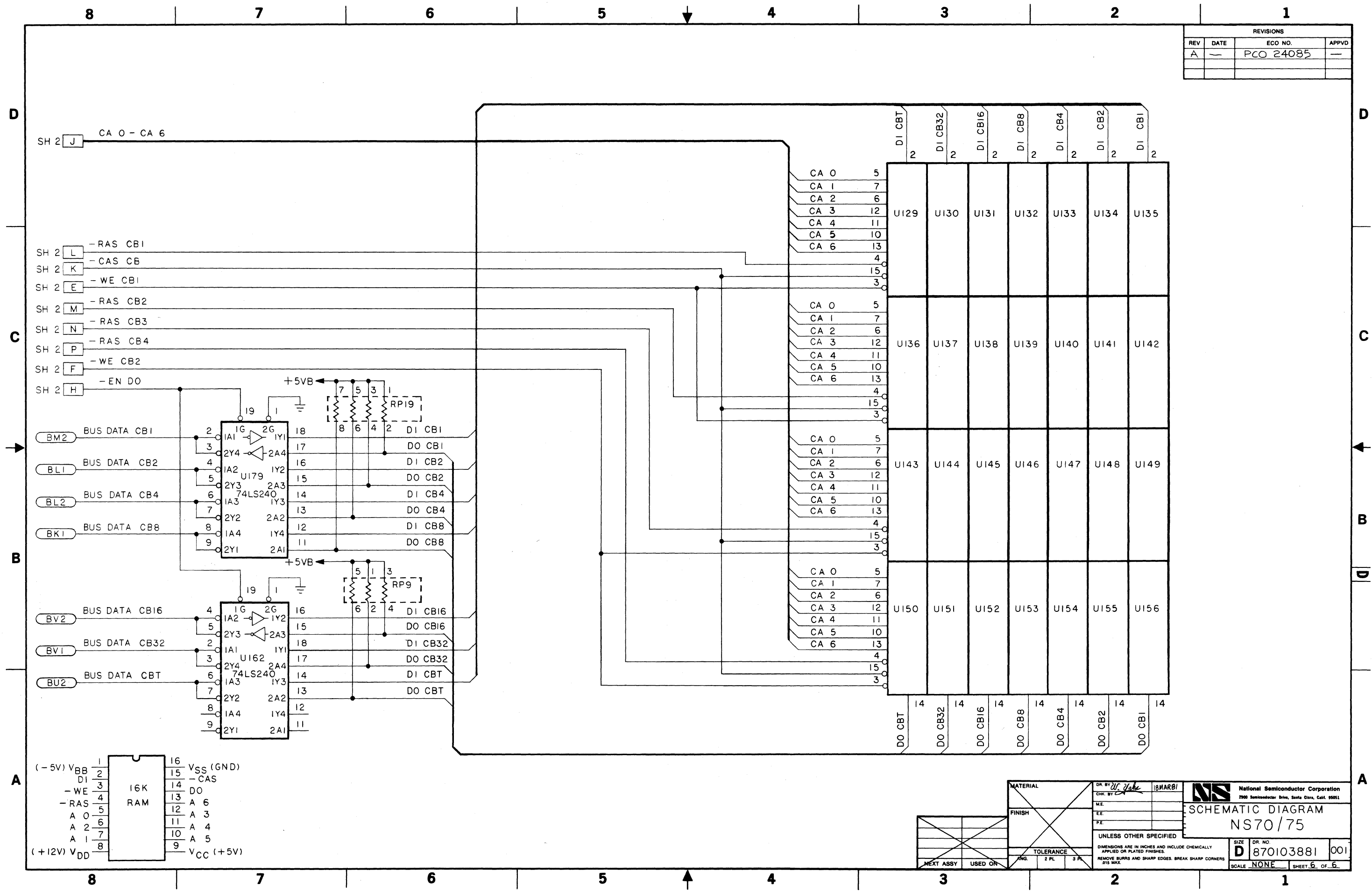


DO 08 - DO 15
DO 24 - DO 31

AB SH 3

MATERIAL	OR BY <i>W. Yabe</i>	BY <i>BMAR</i>	 National Semiconductor Corporation 2900 Semiconductor Drive, Santa Clara, Calif. 95051
FINISH	Schematic Diagram NS70/75		
TOLERANCE	DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES. REMOVE BURRS AND SHARP EDGES. BREAK SHARP CORNERS .015 MAX.		
SCALE	NONE	SHEET 5 OF 6	DR. NO. 870103881 001 SIZE D

REVISIONS			
REV	DATE	ECO NO.	APPVD
A		PCO 24085	

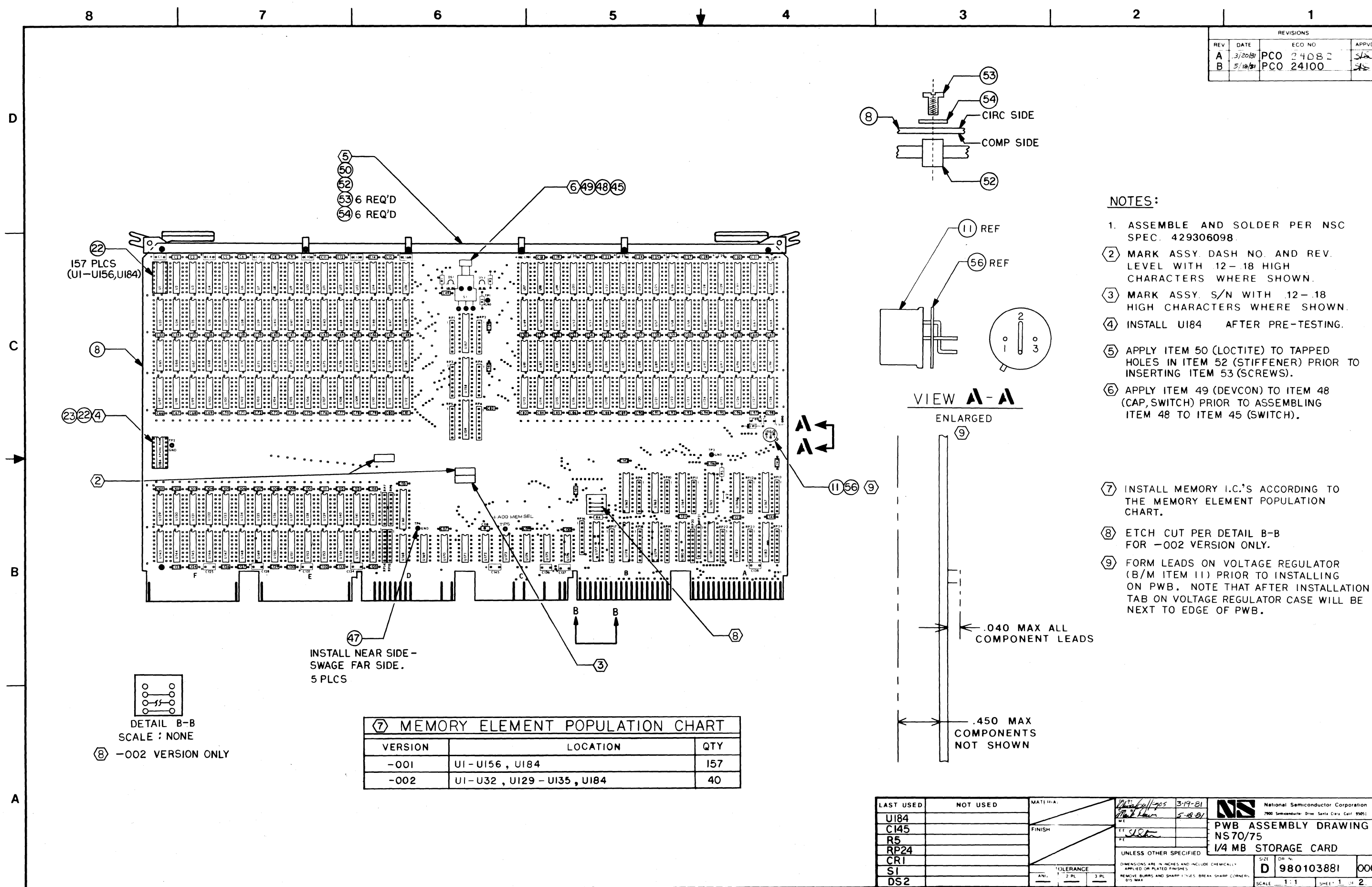


MATERIAL		DR. BY <i>W. Jabe</i> 18MAR81		 National Semiconductor Corporation 2900 Semiconductor Drive, Santa Clara, Calif. 95051
FINISH		M.E.		
TOLERANCE		E.E.		
UNLESS OTHER SPECIFIED		RE		SCHEMATIC DIAGRAM NS70/75
DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES.		REMOVE BURRS AND SHARP EDGES. BREAK SHARP CORNERS .015 MAX.		
SCALE NONE		SHEET 6 OF 6		SIZE D DR. NO. 870103881 001

NEXT ASSY	USED ON

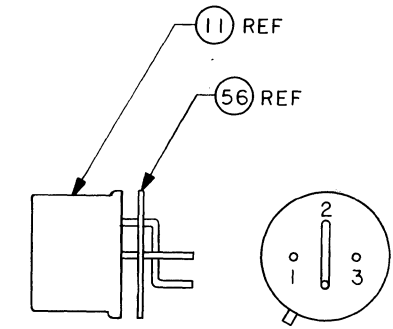
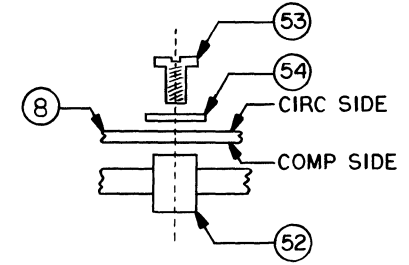
(-5V) V _{BB}	1	16	V _{SS} (GND)
DI	2	15	-CAS
-WE	3	14	DO
-RAS	4	13	A 6
A 0	5	12	A 3
A 2	6	11	A 4
A 1	7	10	A 5
(+12V) V _{DD}	8	9	V _{CC} (+5V)

REVISIONS			
REV	DATE	ECO NO	APPVD
A	3/20/81	PCO 24082	SLA
B	5/18/81	PCO 24100	SLA

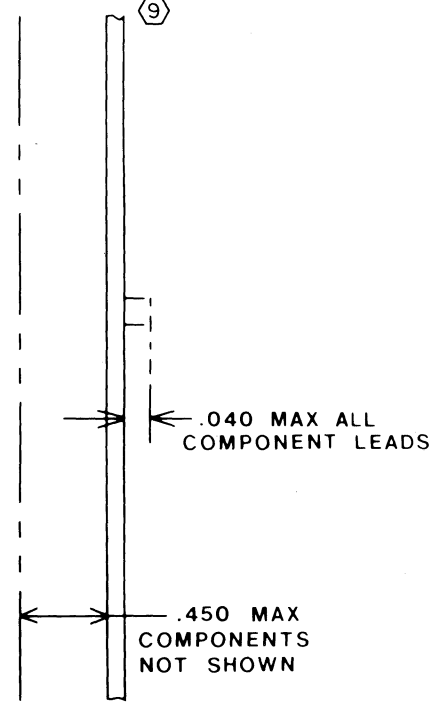


NOTES:

1. ASSEMBLE AND SOLDER PER NSC SPEC. 429306098.
2. MARK ASSY DASH NO. AND REV. LEVEL WITH 12-18 HIGH CHARACTERS WHERE SHOWN.
3. MARK ASSY S/N WITH 12-18 HIGH CHARACTERS WHERE SHOWN.
4. INSTALL UI84 AFTER PRE-TESTING.
5. APPLY ITEM 50 (LOCTITE) TO TAPPED HOLES IN ITEM 52 (STIFFENER) PRIOR TO INSERTING ITEM 53 (SCREWS).
6. APPLY ITEM 49 (DEVCON) TO ITEM 48 (CAP, SWITCH) PRIOR TO ASSEMBLING ITEM 48 TO ITEM 45 (SWITCH).
7. INSTALL MEMORY I.C.'S ACCORDING TO THE MEMORY ELEMENT POPULATION CHART.
8. ETCH CUT PER DETAIL B-B FOR -002 VERSION ONLY.
9. FORM LEADS ON VOLTAGE REGULATOR (B/M ITEM 11) PRIOR TO INSTALLING ON PWB. NOTE THAT AFTER INSTALLATION, TAB ON VOLTAGE REGULATOR CASE WILL BE NEXT TO EDGE OF PWB.



VIEW A-A
ENLARGED



157 PLCS
(UI-U156, UI184)

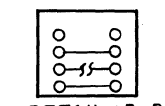
50
52
53 6 REQ'D
54 6 REQ'D

6 49 48 45

23 22 4

2

47
INSTALL NEAR SIDE -
SWAGE FAR SIDE.
5 PLCS



DETAIL B-B
SCALE: NONE

8 -002 VERSION ONLY

7 MEMORY ELEMENT POPULATION CHART		
VERSION	LOCATION	QTY
-001	UI-U156, UI184	157
-002	UI-U32, UI29-UI35, UI184	40

LAST USED	NOT USED	MATERIAL	DATE	BY
UI84			3-19-81	SLA
C145			5-18-81	SLA
R5				
RP24				
CR1				
SI				
DS2				

UNLESS OTHER SPECIFIED:		DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES.	
REMOVE BURRS AND SHARP EDGES. BREAK SHARP CORNERS.		SCALE: 1:1	

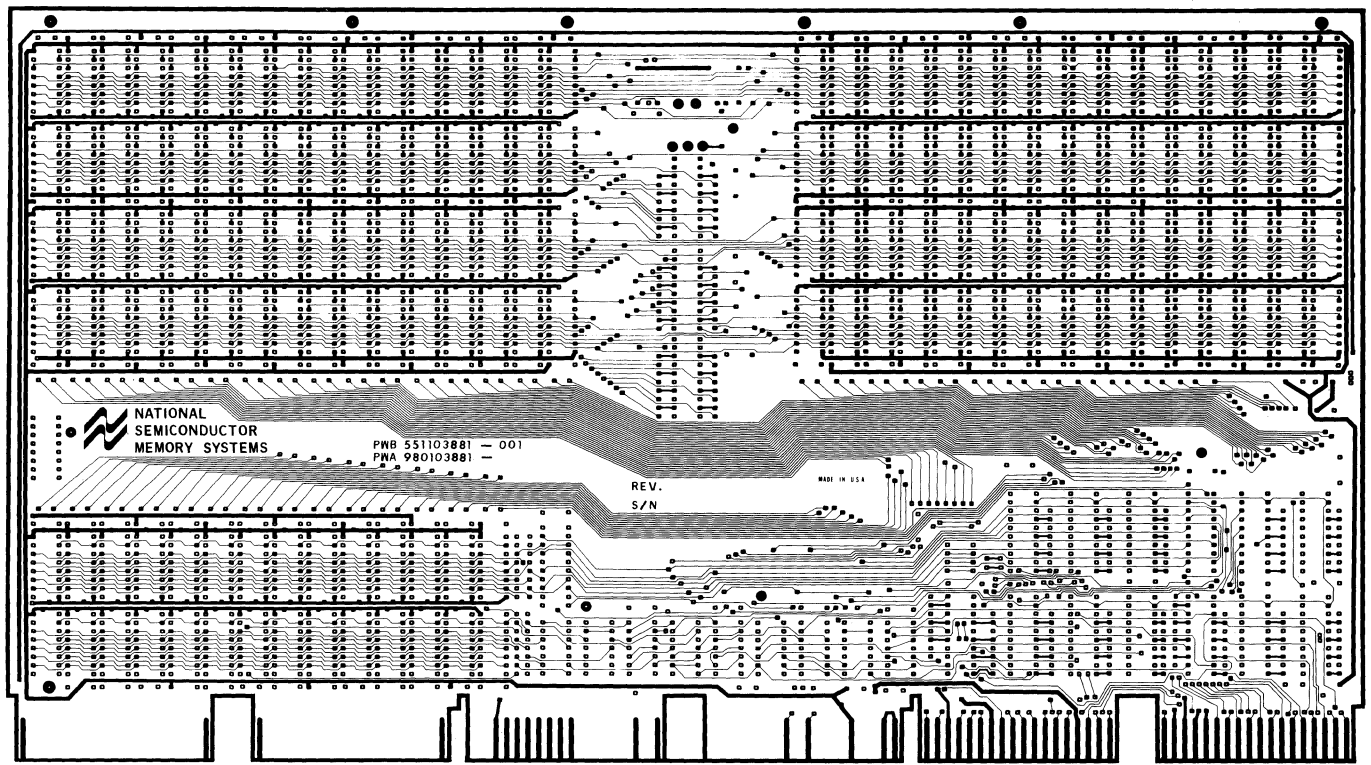
National Semiconductor Corporation 7900 Semiconductor Drive, Santa Clara, Calif. 95051	
PWB ASSEMBLY DRAWING NS70/75 1/4 MB STORAGE CARD	
SIZE: D	DR. NO.: 980103881
SHEET 1 OF 2	

8 7 6 5 4 3 2 1

REVISIONS			
REV	DATE	ECO NO	APPVD
		SEE SHEET 1	

COMPONENT SIDE

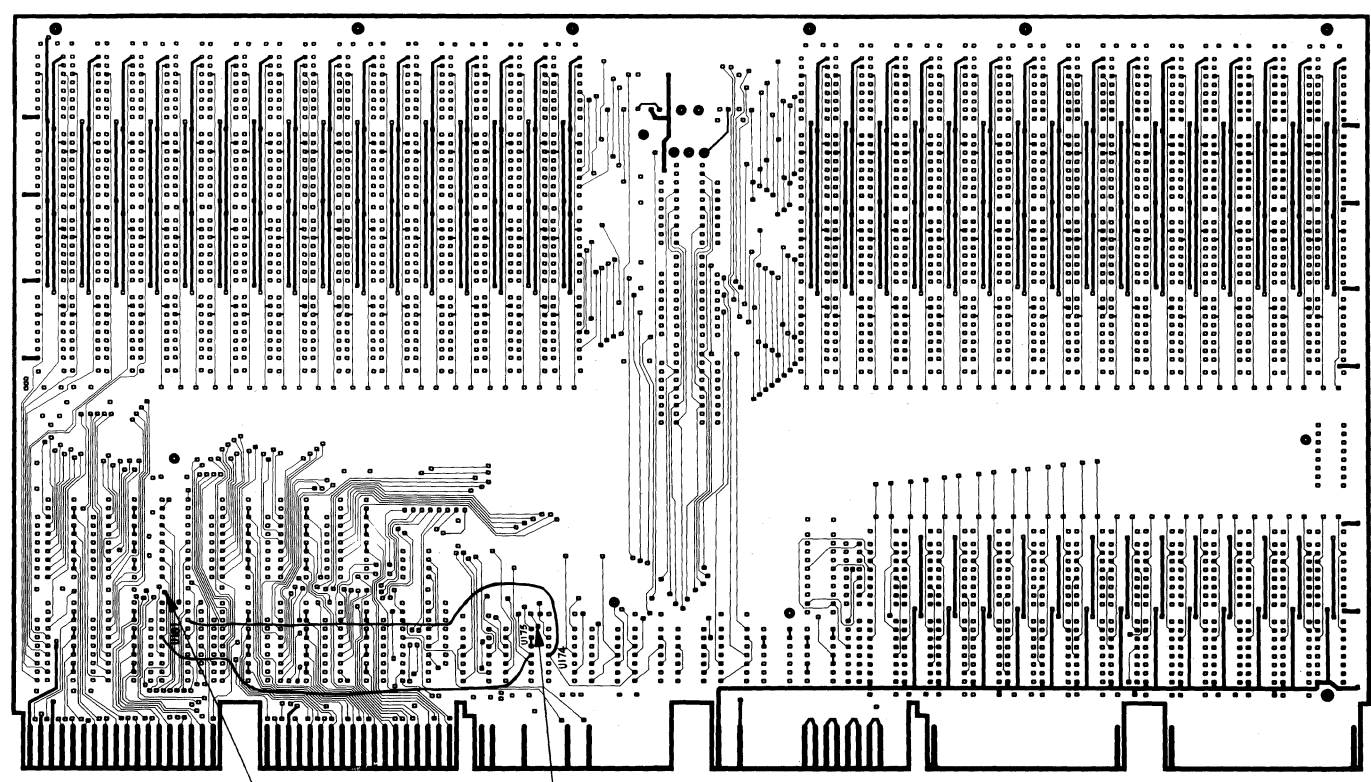
REWORK INSTRUCTIONS SHEET



CIRCUIT SIDE

- DRILL OUTS:
1. FEEDTHRU ABOVE U181-20
 2. FEEDTHRU NEAR U175-1

- ADD JUMPERS BETWEEN:
- 1 U181-3 TO U174-11
 - 2 U181-16 TO U175-4



DRILL OUT DRILL OUT

8 7 6 5 4 3 2 1

MATERIAL	DR BY:	 National Semiconductor Corporation 7900 Semiconductor Drive, Santa Clara, Calif. 95051	PWB ASSEMBLY DRAWING NS70/75 1/4 MB STORAGE CARD
	CHK BY:		
FINISH	WE:	UNLESS OTHER SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES REMOVE BLURBS AND SHARP EDGES BREAK SHARP CORNERS 015, MAX	SIZE DR NO D 980103881 000
	FE:		
TOLERANCE		SCALE	SHEET 2 OF 2
ANG	7 PL 3 PL	NONE	