1677 SONET Link
Product Information

PN 3EM13848AF 01
R06.02, Issue 01, September 2007

THIS PRODUCT COMPLIES WITH D.H.H.S. RADIATION PERFORMANCE STANDARDS 21 CFR, 1040.10, FOR A CLASS 1 LASER PRODUCT.

DANGER

Invisible laser radiation is present when the optic connector is open. AVOID DIRECT EXPOSURE TO BEAM.

WARNING

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case users will be required to correct the interference at their own expense.

NOTICE

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1677 SONET Link General System Description

1. INTRODUCTION

1.1 The 1677 SONET Link combines the capabilities of a Digital Cross-connect System (DCS) and a Dense Wavelength Division Multiplexing (DWDM) application into a single, compact 15RU or 18RU shelf. The system supports network and tributary interfaces ranging in speed from DS3 rates up to SONET OC-192 and GIGE rates, providing the flexibility needed to handle virtually any application.

1.2 The 1677 SONET Link uses an 80 Gb/s SONET switch as well as a VT1.5 switch to perform the DCS function. The DWDM application is performed with the use of a Modular Optical System (MOS) that connects to the 1677 SONET Link through a one-wire interface. The MOS uses ADME/W 013/014 Add/Drop Modules (ADMs), DWDME/W 101/102 Dense Wavelength Division Multiplexer (DWDM) modules, and DCME/W 020/040/060/080 Dispersion Compensation Modules (DCMs) that install directly into an ANSI and/or ETSI rack, either above or below the 15RU or 18RU shelf.

1.3 MOS modules perform add/drop of DWDM bands and individual optical channels to the 1677 SONET Link as well as dispersion compensation. With integrated DWDM support through the MOS, the 1677 SONET Link is capable of scaling the bandwidth of existing fiber infrastructures without adding new fiber. A total of 32 DWDM wavelengths can be put onto existing fiber to increase bandwidth availability on the network.

1.4 The 1677 SONET Link supports traditional network architectures such as 1+1 Automatic Protection Switching (APS), Unidirectional Path-Switched Rings (UPSR), Bidirectional Line-Switched Rings (BLSR), and Drop-and-Continue (DC) protection schemes in stacked rings and multi-ring hub network applications.

1.5 The 1677 SONET Link is a single-shelf system with removable modules. The shelf adheres to both ETSI and ANSI space requirements and supports front- and rear-access signal connection ports. Up to two 15RU or 18RU shelves can be installed into one 45RU-high, 19-inch or 23-inch equipment rack. Two 15RU or 18RU shelves together can aggregate up to 384 DS3, 384 EC1, 576 OC-3, 192 OC-12, 48 OC-48, or 8 OC-192 interfaces.

1.6 For additional information, refer to the following related documentation:

- Unit Data Sheets (UDSs) in this manual
- 1677 SONET Link Installation Practices manual (PN 3EM13849AF)
- 1677 SONET Link Turn-Up manual (PN 3EM13850AD)
- 1677 SONET Link Operation and Administration manual (PN 3EM13851AF)
- 1677 SONET Link Commands and Messages manual (PN 3EM13852AF)
- 1677 SONET Link Maintenance and Trouble Clearing (PN 3EM13853AF)
- 1677 SONET Link Address and Location Guide (PN 3EM13854AD)
- 1677 SONET Link Engineering Support Documentation (PN 3EM17362AD)

1.7 The following is a partial list of the standards that have influenced certain behavioral aspects of the 1677 SONET Link:

- ANSI Z136.1, 1993
- ANSI Z136.2, 1977
- GR-63-CORE, Issue 2, April 2002
- GR-78-CORE, September 1997
- GR-199-CORE, Issue 4, May 2001
- GR-253-CORE, Issue 3, September 2000
- GR-472-CORE, Issue 2, November 1996 with Revision 2, February 1999
- GR-474-CORE, Issue 1, December 1997
- GR-499-CORE, Issue 2, December 1998
- GR-818-CORE, Issue 1, December 1995
- GR-819-CORE
- GR-820-CORE, Issue 2, December 1997
- GR-831-CORE, Issue 1, November 1996
- GR-833-CORE, Issue 4, June 2000
- GR-929-CORE, December 2002
- GR-1089-CORE, Issue 2, February 1999
- GR-1093-CORE, Issue 2, June 2000
- GR-1230-CORE, Issue 4, December 1998
- GR-1339-CORE, Issue 1, March 1997
- GR-1400-CORE, Issue 2, January 1999
- GR-2914-CORE, Issue 4, December 1998
- GR-2996-CORE, Issue 1, January 1999
- GR-3008-CORE, Issue 2, December 1998

- IEC 60825-1
- IEC 60825-2
- SR-332, Issue 1, May 2001
- SR-3580, November 1995
- SR-TSY-001130, Issue 1, May 1989
- SR-TSY-001171, Issue 1, January 1989
- T1.105-2001, May 2001
- T1.107-1995, July 1995
- T1.107-2002, January 2002
- T1.231-1997, October 1997
- UL 60950, Third Edition

2. SYSTEM ADMINISTRATION

2.1 The 1677 SONET Link system administration can be performed using the following applications:

- 1353 Network Manager (NM) Element Management System (EMS)
- 1353 NM Lite EMS
- Craft
- Transaction Language 1 (TL1)

2.2 The 1353 NM EMS and 1353 NM Lite EMS allow the user to view all Network Elements (NEs) in a network by using TCP/IP through the Ethernet port (using an RJ-45 connector) located on remote 1677 SONET Link Timing Cards (TCs). The EMS uses the Element Management Layer (EML) version of the 1353 NM 1677 SONET Link Element Management Application (EMA) as an interface for performing provisioning, monitoring, and alarm management at the NE level.

2.3 See figure 2-1 for an illustration of a remote NE Ethernet port connection.

2.4 For a more detailed description of the Ethernet port on the TC, refer to the Unit Data Sheets (UDS) section of this manual.

2.5 For more information on the 1353 EMS, refer to the 1353 NM R10.00 Operation and Administration manual. For more information on the 1353 NM Lite EMS, refer to the 1353 NM Lite R10.00 Operation and Administration manual. For more information on the 1353 NM 1677 SONET Link EMA, refer to the 1677 SONET Link Operation and Administration manual (PN 3EM13851AF).

2.6 The 1677 SONET Link uses the 1353 NM Craft application to perform system administration on local NEs. The 1353 NM Craft interfaces to the NE using the EMA, where provisioning, monitoring, and alarm management are performed. A Craft connection is made by connecting a console cable from the DB-9 connection port of the PC to the RJ-11 console port on the 1677 SONET Link TC front panel. See figure 2-2.

2.7 Transaction Language 1 (TL1) commands can also be directly entered from a Customer Interface Terminal (CIT) to provision, monitor, and control the system. Connections between the CIT and the 1677 SONET Link NE are also made through the console port on the TC front panel. For a list of TL1 commands supported by the 1677 SONET Link, refer to the Commands and Messages manual (PN 3EM13852AF).

Figure 2-1. Ethernet Connection

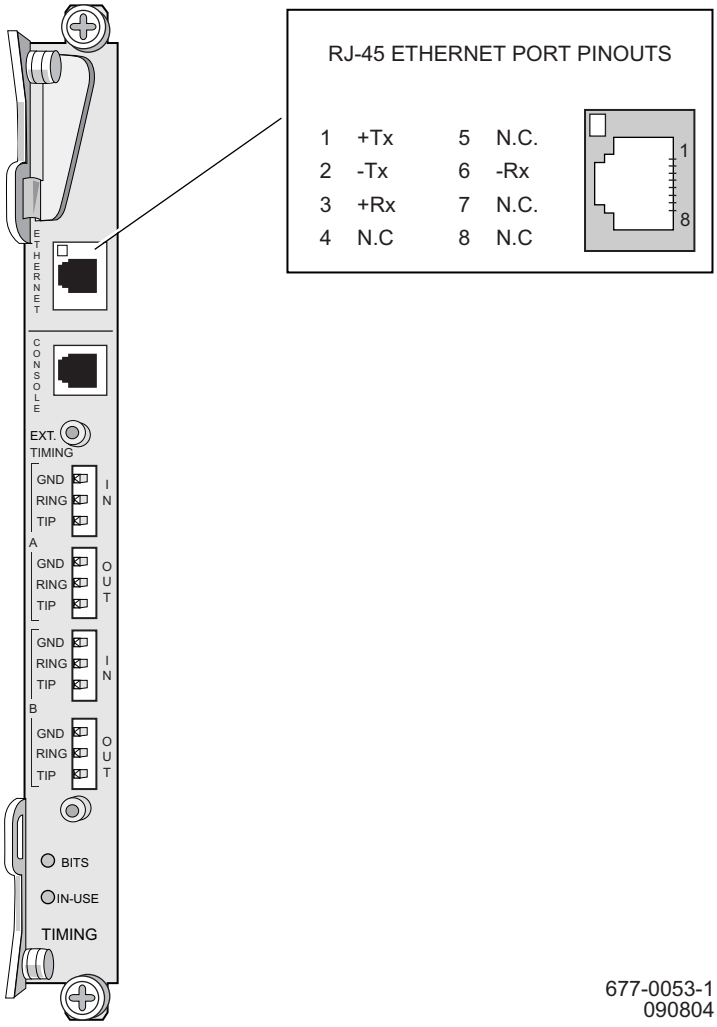
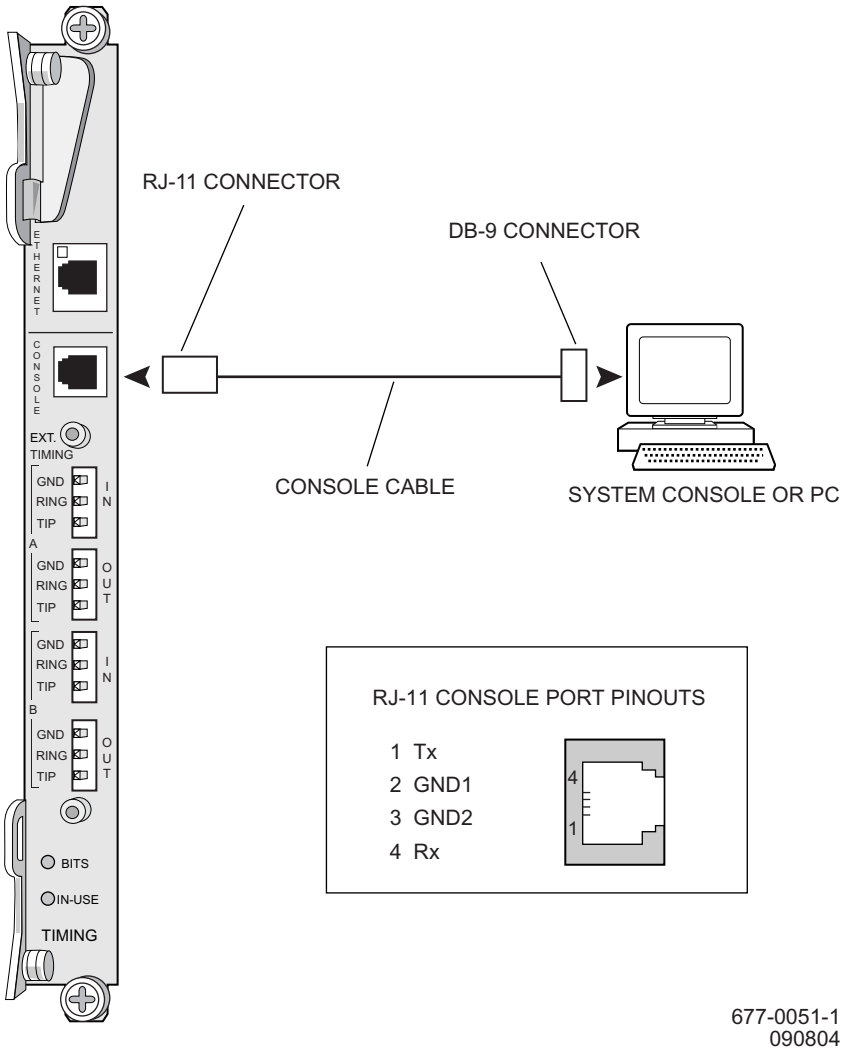


Figure 2-2. Data Terminal to TC Connection



3. FEATURES

3.1 This section describes 1677 SONET Link new features introduced by 1677 SONET Link R06.02 and baseline features.

New Features

3.2 The following paragraphs describe the new features of the system for R06.02. To administer these new features by executing Transaction Language 1 (TL1) commands, refer to the 1677 SONET Link Commands and Messages manual (PN 3EM13852AF) and the 1677 SONET Link manual (PN 3EM13851AF). To administer these new features through the 1677 SONET Link Element Management Application (EMA), refer to the 1677 SONET Link Operation and Administration manual (PN 3EM13851AF).

3.3 R06.02 provides the following new features:

System Architecture

- DS0 Grooming

Connection Types

- DS0 Connections

Facility Maintenance

- RAI Detection and Insertion

Loopback

- DS0 Loopback

Test Access

- DS0 Test Access

System Architecture

DS0 Grooming

3.4 One pair of DS0G DS0 Groomers (DS0Gs) in a 1+1, nonrevertive protection scheme may be provisioned in a system to provide 2.5 Gb/s of bandwidth for DS0 grooming. This supports a system total of 1344 DS1s.

3.5 The DS0G is a single-width, full-height module that installs into full-height (A and B) slots 3 and 4 or 14 and 15. The choice of the DS0G signal source is made at the SSC.

3.6 The system can retrieve the currently used DS0G capacity. The RTRV-PRMTR-NE command supports this function.

3.7 A DS1 embedded within a VT1 can be created and provisioned only if it is defined to be DS0 groomed using the DS0G parameter of the ENT-T1 TL1 command. When the DS0G parameter is provisioned the system automatically assigns a DS1 residing on the DS0G module.

3.8 All facilities with embedded DS0s destined for the DS0 Groomer must be routed through the VT Switch (VSC). Some of these facilities may require additional conversion through the TMUX prior to going through the VSC (depending on the STSMAP parameter). All connections between VSC, TMUX, and DS0G pass through the SSC. To support the DS0 Groomer, the 3EM12295AD SSC104 must be equipped.

Connection Types

DS0 Connections

3.9 When the system is equipped with a pair of DS0G modules, DS0-level 2-way cross-connections are supported. The DS0G provides non-blocking 32,256×32,256 (2.5 Gbps) DS0 cross-connections. An incoming DS0 embedded within a DS1 terminating on the DS0G can be cross-connected to any outgoing DS0 embedded within a DS1 terminating on the DS0G. The ED/ENT/DLT-CRS-T0 commands support this feature.

3.10 Short-term and long-term Trunk Conditioning (TC) and Insertion Word (IW) values can be specified when a DS0 cross-connection is established or deleted. In addition, TC/IW can be edited after a DS0 connection is established. The TC/IW provisioning is applied if a CGA alarm is active on the cross-connection. Upon deletion of a cross-connection, TC/IW provisioning is applied as soon as the DLT command is executed. Support for 4-state, 16-state, and transparent TC is provided.

Refer to the Connection Types section in Baseline Features for more information.

Facility Maintenance

RAI Detection and Insertion

The NE supports detection and generation of DS1 maintenance signals. For DS1s (SF and ESF formats) terminating on the DS0G, the system supports detection and generation of Remote Alarm Indication (RAI).

Loopback

DS0 Loopback

3.11 The system supports establishment of DS0 near-end, matrix loopback in the DS0G. Matrix loopback is supported for DS0 ports that are not cross-connected or are involved in a 2-WAY cross-connection. A matrix loopback is not allowed on a DS0 that is connected to a Test Access Port. The OPR-LPBK-T0 command is used to establish this functionality for T0 facilities.

3.12 Refer to the Loopback section in Baseline Features for more information.

Test Access

DS0 Test Access

3.13 Test access allows for the monitoring, injection, and isolation of signals to isolate facility and/or equipment faults. The user can assign a DS0 port to function as a test access Facility Access Digroup (FAD) to monitor incoming or outgoing DS0s. Two sequential DS0s are assigned as FAD A and FAD B to form a Test Access Port Pair (TAPP).

3.14 A DS0 residing within a DS1 terminating on the DS0G can be designated as a TAP. Two DS0s that reside within contiguous time slots within the DS1. When a DS1 is defined to support DS0-embedded TAPs, all 24 embedded DS0s functioning as TAPPs are autogrown into the logically removed state and are included in the specified TAPPOOL.

3.15 The Test Access Path (TAP) can be manipulated locally or remotely through software control. The system acts as a Digital Test Access Unit (DTAU) to a Generic Test System (GTS). The GTS uses a Remote Test Unit (RTU) to interface through the TAP to the system's TAPP. The system supports loop, monitor, and split test access connections.

3.16 The TACC0 parameter of the ENT-T1 or ED-T1 command is used to assign all 24 DS0s to TAPPs. The CONN-TACC-DIG command is then used to establish a test access connection to another DS0. Equipment-side (AID) ports can be assigned for testing.

3.17 MONE, MONEF, SPLTE, and SPLTEF test access modes are supported for test connections using the DS0 TAPs. For TL1 purposes only, these modes are referred to as SXMON, DXMON, SXSPLT, and DXSPLT, respectively.

3.18 When establishing a test access connection with the CONN-TACC-DIG command, MONE and MONEF are the only allowed modes. After the test access connection is established the CONN-MON and CHG-SPLIT commands can be used to change the mode. The CONN-MON command is used to change the mode to MONE or MONEF, and the CHG-SPLIT command is used to change the mode to SPLTE or SPLTEF. The RTRV-TACC command is used to retrieve information on configured test access ports.

3.19 Individual DS0s cannot be deprovisioned as TAPs. To deprovision a DS0 as a TAP, the DS1 in which it is embedded must be deleted with the DLT-T1 command; all 24 DS0s functioning as TAPPs are then autodeleted.

3.20 The TAP can be manipulated locally or remotely with TL1 commands. Users can passively monitor incoming or outgoing equipment or facility signal through TAPs. A test access connection can be made to a cross-connected circuit, a single port, a simplex-connected circuit, or the head of a conference connection.

3.21 TAPPs can be provisioned to be in a private or a public pool. A private pool is controlled by the user who created it, and only that user can access it. A public pool is accessible by any user. For either type of TAPP pool, only the user that establishes a TACC session can execute disconnect or change TACC commands. A user with the appropriate privilege level can disconnect a TACC connection established by another user, regardless of whether the TAPP belongs to a private or public pool.

3.22 The system supports up to 42 DS0 TAPPs in all combined private and public TAPP pools.

3.23 Refer to the Test Access section in Baseline Features for more information.

Baseline Features

3.24 The following paragraphs describe baseline features. To administer these features by executing Transaction Language 1 (TL1) commands, refer to the 1677 SONET Link Commands and Messages manual (PN 3EM13852AF) and the 1677 SONET Link Operation and Administration manual (PN 3EM13851AF). To administer these features through the 1677 SONET Link Element Management Application (EMA), refer to the 1677 SONET Link Operation and Administration manual (PN 3EM13851AF).

3.25 Baseline features are summarized as follows:

System Architecture

- 1+1 Automatic Protection Switching
- 15RU and 18RU Shelves
- Amplification
- Automatic In-Service Secondary State
- Bidirectional Line Switched Ring
- BLSR Ring Automap Generation
- BLSR Traffic Unaffected by Node Reset
- Configurations
- Customer Interface Over LAN
- Detection of SSC Memory Size
- Drop and Continue Architecture
- Electrical DS3/EC1 Hybrid IOC Module
- EMI/RFI Compliance
- Enhanced Diagnostic Troubleshooting Tools
- Fault Detection
- Forward Error Correction
- In-Service Growth
- In-Service Upgrade
- Modular Optical System
- NEBS Compliance
- Network Architecture
- One-Wire System Interface
- Redundancy
- Supported Client Signals
- Switching Architecture

- Timing
- Unidirectional Path Switched Ring

Network Applications

- Alcatel-Lucent 1603 SMX File Transfer
- Data Communications Channel
- Operations System Interface
- SONET Compatibility

Connection Types

- Simplex GigE Connections for Video Broadcast

Alarms

- System
- Equipment
- Facility

Hardware Maintenance

- Card Extraction Interlock
- Diagnostics
- Fault Isolation
- Remote Inventory

Performance Monitoring

Loopback

Test Access

- Loop
- Monitor
- Split

Administration

- Secure Password Identifier
- Simplified User Privilege Parameter Changes
- Telcordia Login
- User-Based REPT^DBCHG Autonomous Message Reporting
- User-Privilege-Level Command Retrieval
- User Security Levels

Distinctive Software Features

- Numeric Ranging and Grouping
- Two-Second Command Response

System Architecture

1+1 Automatic Protection Switching

3.26 The 1677 SONET Link supports pre-amplifier, 1+1 Automatic Protection Switching (APS) for client-side or line-side optical interfaces. In 1+1 APS, traffic is transmitted over one active (working) data path with a standby data path serving as a protection path. In the event of failure, traffic is automatically switched from the working path to the protection path, making the protection path the active path. 1+1 APS is a local action that involves no changes elsewhere in the network.

15RU and 18RU Shelves

3.27 The system supports 15RU and 18RU shelf chassis. The 18RU shelf chassis provides the following features not available with the 15RU shelf chassis:

- Temperature sensing capabilities
- DC power lugs in the back of the shelf
- Fiber management attached directly to the frame

3.28 The following equipment is available on both the 15RU and 18RU shelves however, they not interchangeable:

- DS3/EC1 48- or 96-port connector panels
- Fan tray

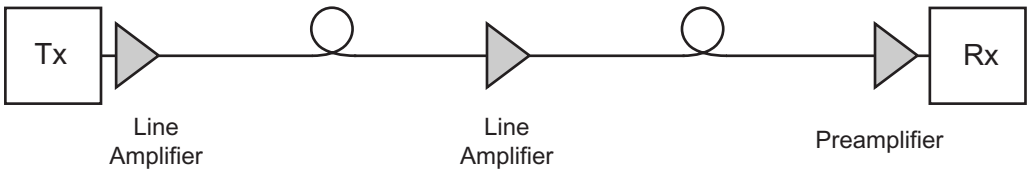
3.29 Both the 15RU and the 18RU shelf chassis configurations consist of one I/O shelf, power panel, fans, and rear DS3 panel. Each shelf chassis configuration supports two types of connector panels (48 or 96 port panel); the 18RU and 15RU connector panels are not interchangeable. Each shelf chassis configuration can also support a Modular Optical System (MOS) passive optics tray. The shelves are divided as follows:

- Common module area populated with two TCs, two SSCs, two CCCs
- Four quadrants, two in subshelf A and two in subshelf B
  - Low-capacity outer slots (1A, 1B, 2A, 2B, 3A, 3B, 4A, 4B, 14A, 14B, 15A, 15B, 16A, 16B, 17A, 17B)—can be populated with ECC, OC3, OC12, OC48, GIGE, EDFA. DS0G cards may populate the 3/4-AB or 14/15-AB slots.
  - High-capacity inner slots (5A, 5B, 6A, 6B, 12A, 12B, 13A, 13B)—can be populated with ECC, OC3, OC12, OC48, GIGE, OC192, TMUX, EDFA, VSC (ECC is not supported in slots 6A, 6B, 12A, or 12B)

Amplification

3.30 System amplification is achieved in DWDM applications through the Erbium Doped Fiber Amplifier (EDFA) module. The EDFA is available in both line-amplifier and pre-amplifier models. The line-amplifier EDFA amplifies input signals measuring -28dB or greater. The pre-amplifier EDFA amplifies input signals measuring less than -28 dB. See figure 3-1.

Figure 3-1. EDFA Line-Amplifier and Pre-amplifier Applications



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3.31 The EDFA also monitors the presence of SSC primary bits. If an absence of these primary bits occurs, the EDFA laser will be turned off. Assertion of a Loss Of Signal (LOS) alarm or a pump bias alarm is generated to the network management applications, while the assertion of over-temperature alarms shut down the EDFA. A pump bias alarm indicates the end-of-life of the EDFA.

Automatic In-Service Secondary State

3.32 The system supports the Automatic In-Service (AINS) secondary state. When the AINS secondary state is provisioned for a facility, the system automatically puts that facility in an in-service primary state after the facility has a customer signal without any of the specified conditions. Refer to table 3-A for supported facilities and applicable condition types and in-service states.

Table 3-A. AINS Provisioning Supported Facilities

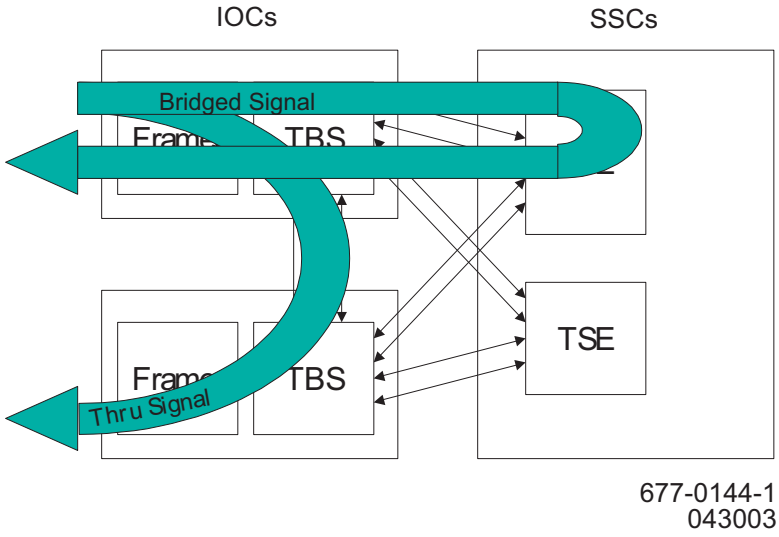
CUSTOMER SIGNAL	CONDITIONS	IN-SERVICE STATE
DS1	AIS, LOF	IS
DS3	AIC, AIS, ISD, LOF, LOS	IS
EC1	AIS-L, LOF, LOS	IS
OC-3	AIS-L, LOF, LOS	IS
OC-12	AIS-L, LOF, LOS	IS
OC-48	AIS-L, LOF, LOS	IS
OC-192	AIS-L, LOF, LOS	IS
STS-1 embedded in EC1, OC-3, OC-12, OC-48, or OC-192	AIS-P, LOP-P, PLM-P, TIM-P, UNEQ-P	IS
STS-3c embedded in OC-3, OC-12, OC-48, or OC-192	AIS-P, LOP-P	IS
STS-12c embedded in OC-12, OC-48, or OC-192	AIS-P, LOP-P	IS
STS-48c embedded in OC-48 or OC-192	AIS-P, LOP-P	IS
VT1.5 within embedded STS-1	AIS-V, LOP-V, PLM-V, UNEQ-V	IS

Bidirectional Line Switched Ring

3.33 The 1677 SONET Link supports Bidirectional Line Switched Ring (BLSR) protection switching on OC-48 and OC-192 optical line interfaces. In BLSR, traffic transmits in both directions of the ring. Each fiber divides its timeslots equally between working and protection bandwidths. In the event of failure on the working line, traffic is switched to the protection line causing a loopback to form, sending the traffic back through network. Figure 3-2 shows the basic signal flow through a BLSR network.

3.34 OC-192 BLSR is not supported in slots 6AB and 12AB.

Figure 3-2. BLSR



BLSR Ring Automap Generation

3.35 The AUTOMAP parameter of the ED/ENT-FFP-OC48/OC192 TL1 command is used to enable/disable automatic generation of squelch/ring maps. All nodes within the BLSR ring must be configured for automap generation for automap generation to occur. The maximum number of BLSR nodes for automap generation is 16. Each BLSR maintains its own maps; there is no master BLSR node. Automap messages are transmitted over the same BLSR ring; they do not cross BLSR rings (for example, dual-interconnected rings).

3.36 DCC must be enabled and operational for automap generation to occur. Automatic squelch and ring map generation is supported on DCC CLNP networks. The system discovers its immediate DCC neighbors and keeps track of the network address over which it communicates.

BLSR Traffic Unaffected by Node Reset

3.37 A reboot of both Common Control Cards (CCCs) does not affect BLSR traffic.

Configurations

3.38 Refer to table 3-B for descriptions of the modular configurations the system supports.

Table 3-B. Modular Configurations

ITEM	DESCRIPTION
15RU Shelf or 18RU Shelf	Power Panel I/O Modules Common Modules Air Filter Fan Assembly
I/O Modules	DS3/EC1 (ECC-12P) OC-3 (OC3-12P) OC-12 (OC12-4P) OC-48 (OC48-1P) OC-192 (OC192-1P) Gigabit Ethernet (GIGE-2P) Two optional DS0Gs (only two DS0Gs allowed per system)
Common Modules	Common Control Card (CCC) STS Switch Card (SWC) Timing Card (TC)
Modular Optical System	Add/Drop Modules (ADM) Dense Wavelength Division Multiplexer (DWDM) Modules Dispersion Compensation Modules (DCM)
Maximum number of shelves	Two 15RU or 18RU shelves per rack
Maximum number of I/O modules	24 half-height modules installed in slots 1-6 and 12-17
Maximum number of common modules	2 full-height CCC in slots 9 and 10 2 full-height SWC in slots 7 and 8 2 half-height TC in slots 11A and 11B
Battery feeds	Independent, redundant battery feeds Independent, redundant battery returns
Power supply redundancy	1+1 redundant battery feeds
Shelf power distribution	Backplane to each module in shelf

Customer Interface Over LAN

3.39 Customer interface over LAN allows a direct connection of a Customer Interface Terminal (CIT) through an 10BaseT Local Area Network (LAN) to any rack in the system. This allows the user to diagnose a complex problem by performing local tests or maintenance actions from a local shelf.

3.40 The CIT connects to the RS-232/RJ-11 console port of the Timing Card (TC) to set up the LAN interface.

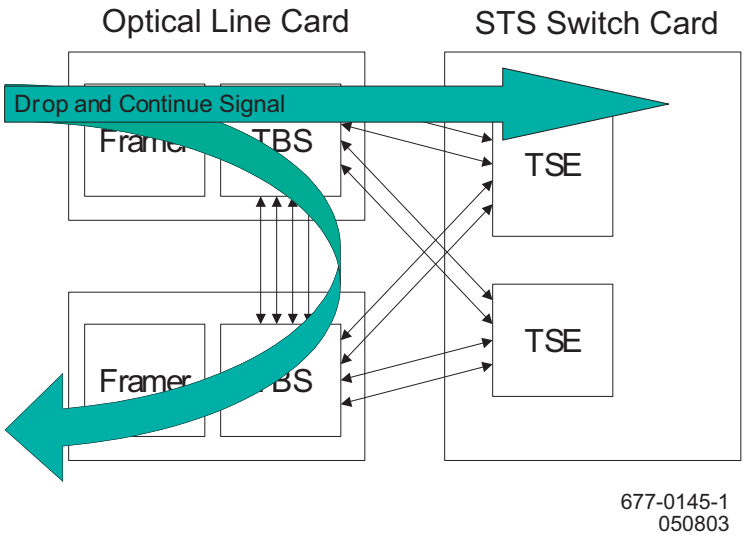
Detection of SSC Memory Size

3.41 The Remote Inventory (RI) function provides a mechanism for the user to determine the amount of RAM equipped on the SSC processors. If a SSC is equipped with smaller RAM size than its mate the system generates a System Resource Fault—SSC RAM (SRFLT-SSCRAM) alarm.

Drop and Continue Architecture

3.42 Drop and Continue network cross connections are used in dual ring interworking applications. The signal is both dropped for local distribution and passed through to the next node forming a special case of multicast. Such a multicast is implemented on the Telecom Bus Serializer (TBS) device on the line cards. Drop and Continue STS-1s are multicast to adjacent IOCs through the auxiliary bus and to the SSC over the working and protect telecom bus serial links. TSEs on the SSCs are used for protection decisions of local drop traffic only. Figure 3-3 illustrates signal flow for Drop and Continue networks.

Figure 3-3. Drop and Continue



3.43 Three types of signals are available in Drop and Continue applications:

- Ring interfaces (continue part of Drop and Continue)
- Drop interfaces (drop part of Drop and Continue)
- Local access (typical UPSR)

3.44 For ring interfaces, STS-1, STS-3c, STS12c, and STS48c paths can be configured as DRI protection groups. Drop interfaces can be protected or unprotected; they can even be drop interfaces from other Drop and Continue rings. Local assess is not supported at Drop and Continue drop nodes; it is supported only at other nodes on the Drop and Continue rings.

Electrical DS3/EC1 Hybrid IOC Module

3.45 The IFC 201 12-Port DS3/EC1 Interface Card (ECC-12P) supports the following facilities: EC1, standalone DS3, DS3 embedded in EC1, STS-1 embedded in EC1, VT1.5 embedded in EC1, DS1 embedded in VT1.5 in EC1, DS1 embedded in standalone DS3 or DS3 in EC1.

3.46 Each ECC-12P supports up to 12 EC1s or standalone DS3s. ECC-12Ps can carry a mix of DS3 and EC1 ports. The ECC-12P is compatible with the existing DS3/EC1 connector panel.

3.47 ECC-12Ps are 1:4 protected. Protection switching is revertive. The following groups of slots are used for 1:4 protection switching:

- 1A (P), 2A, 3A, 4A, 5A
- 1B (P), 2B, 3B, 4B, 5B
- 13A, 14A, 15A, 16A, 17A (P)
- 13B, 14B, 15B, 16B, 17B (P)

EMI/RFI Compliance

3.48 The system, including all internal cabling, is ElectroMagnetic Interference (EMI) and Radio Frequency Interference (RFI) compliant. The system complies to Federal Communications Commission (FCC) Code of Federal Regulations (CFR) Title 47, Part 15, Subpart B, Section 15.109.

Enhanced Diagnostic Troubleshooting Tools

3.49 The NE has the ability to retrieve the active internal physical paths through the NE, down to the board level, of all entities connecting the specified pair of endpoints through the system. This capability is provided by the TL1 command FLTLOC-PATH. The FLTLOC-PATH command is not required to report state or fault information associated with the reported physical entities.

3.50 To execute a FLTLOC-PATH command, the specified FROM and TO ports must identify a one-way or two-way cross-connection (an SST of ACT or BUSY and cross-connected together). The FROM and TO entities must not be in a Loopback or Test Access connection.

3.51 The successful response to a FLTLOC-PATH command contains several lines of nonparsable output data, with each line of output identifying an element of the data path through the system.

3.52 The RTRV-LOG TL1 command can be modified to retrieve the system debug logs including card failure data and system log file data. This provides the user with troubleshooting tools allowing faster, more efficient root-cause failure determination.

3.53 For more detailed information on the FLTLOC-PATH and RTRV-LOG commands, refer to the Commands and Messages manual (PN 3EM13852AF).

Fault Detection

3.54 The NE includes the ability to retrieve the active internal physical paths through the NE, down to the board level, of all entities connecting the specified pair of endpoints through the system. This capability is accomplished using the FLTLOC-PATH TL1 command. The FLTLOC-PATH command is not required to report state or fault information associated with the reported physical entities.

3.55 The NE supports the following methods to detect module internal failures caused by hardware failures:

- Data Path Error Detection—This method verifies the traffic and detects internal device-device or board-board faults.
- Periodic Health Checking – Some components have interfaces to communicate with a microprocessor and the microprocessor can configure and retrieve information from the components. Such types of components can be monitored and certain failures may be detected.

Forward Error Correction

3.56 Forward Error Correction (FEC) corrects receiver errors that can occur because of a weak input signal. FEC works on OC192-1P modules when the SONET input signal is encapsulated with a digital wrapper containing FEC coding. FEC can be disabled through software in cases of interfacing with other vendor equipment or when using the OC192-1P in an access application.

3.57 For more information on FEC, refer to the OC192-1P Unit Data Sheet (UDS) in the UDS section of this manual.

In-Service Growth

3.58 In-service growth allows system expansion up to the wired matrix size without disrupting traffic. New modules can be added to the shelf while the system is in-service and carrying traffic.

In-Service Upgrade

3.59 Systems can be upgraded to R06.02 software and hardware from previous releases, as specified in the upgrade procedure, while the system carries traffic. The upgrade procedure can be completed in less than eight hours and within one maintenance window. Default values used when upgrading to R06.02 are defined for all new R06.02 provisioning parameters. Refer to table 3-C for the database status of in-service upgrade functions.

Table 3-C. In-Service Upgrade Database Status

SAVED	NOT SAVED
Provisioning data	Current and historical PM data
Current command level authorizations	Event log file
Equipment provisioning	Diagnostics data
Connection data	
Facility provisioning	
PM provisioning	
User information	
Site ID information	
CPORT configuration	
Command group and security levels	
Alarm database/attributes	
Threshold settings	

3.60 In-service upgrade is implemented using TL1 commands. For in-service upgrades using TL1 commands, control of the new software upgrade procedure is through TL1 commands issued over any sufficiently privileged operations interface such as a Craft Interface Terminal (CIT) and/or an Element Management System (EMS). New software is downloaded from the Remote File Server (RFS) using the COPY-RFILE TL1 command. The new software release is activated using the OPR-DISK TL1 command. The system is rebooted with the new software using the INIT-SYS TL1 command against the CCC and the SWC/DCC processors. Finally, the TMUX modules are reprogrammed, if applicable.

Modular Optical System

3.61 For DWDM applications, the 1677 SONET Link is designed to work with a passive optical system called the Modular Optical System (MOS). The OC-48 and OC-192 Extra Long Reach (XLR) optics on 1677 SONET Link line modules are designed to work with the MOS to provide a cost effective and flexible solution for Optical Networking. The MOS is a passive, reliable, and flexible system used to add and drop light on and off a network fiber and deliver the light to or from the 1677 SONET Link line modules. A banded optical architecture is used to minimize the insertion loss on expressed channels throughout the node. Bundles of light are added and dropped from the network path, then multiplexed or demultiplexed into usable wavelengths and delivered to the 1677 SONET Link line modules. MOS modules install directly above or below the 1677 SONET Link in a standard rack.

3.62 The MOS uses the following modules to accomplish DWDM applications:

- Add/Drop Modules (ADMs)
- Dense Wavelength Division Multiplexer (DWDM) modules
- Dispersion Compensation Modules (DCMs)

3.63 For more information on MOS modules, refer to the Unit Data Sheets (UDS) section of this manual. For information on MOS signal flow, refer to the FUNCTIONAL OPERATION section of the manual.

NEBS Compliance

3.64 The 1677 SONET Link R06.02 is level-3 Network Equipment Building Systems (NEBS) compliant in accordance with SR-3580, GR-63-CORE, and GR-1089-CORE.

Network Architecture

3.65 There are two basic network configuration topologies used by the 1677 SONET Link to provide SONET connectivity and transport for the metro network environment; multi-ring and multi-node, single Ring.

3.66 In multi-ring architectures, a series of 1677 SONET Link systems are connected together with separate protected sets of SONET rings between each pair of nodes. For example, in a 3 ring node network, nodes 1 and 2 share a protected SONET ring and nodes 2 and 3 share a protected separate SONET ring. Here, node 2 acts as a bridge between the sets of rings. Node 2 cross connects the two sets of rings together to allow traffic to travel from node 1 to node 3.

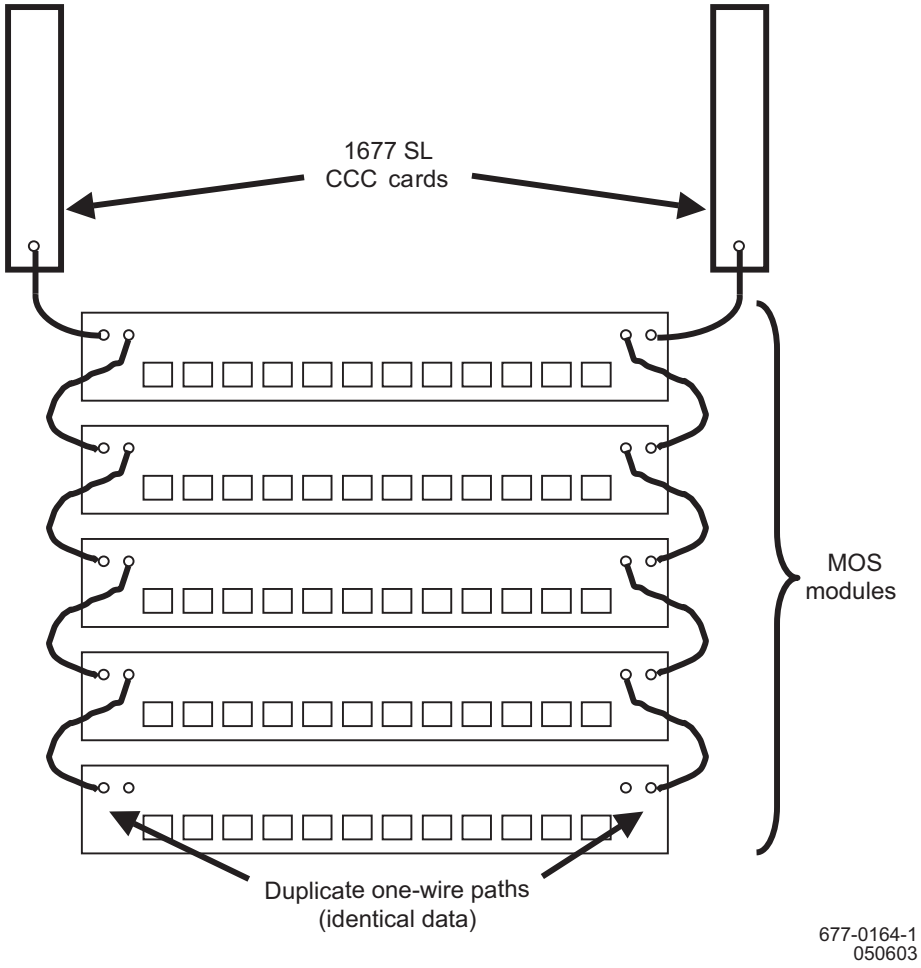
3.67 In multi-node, single ring architectures, there are multiple nodes connected together by a single, protected set of rings. In this case, each node has the ability to pass traffic through itself and back onto the ring in order for traffic to reach its destination.

One-Wire System Interface

3.68 The One-Wire System Interface provides the serial connection between the ADM, DWDM and DCM modules of the MOS to the 1677 SONET Link CCC module and supplies inventory information to the user. All MOS modules contain two Electronically Programmable Read-Only Memory (EPROM) devices that contain inventory information such as the module number, revision number, and CLEI code. The two EPROMS are programmed with identical information. The master EPROM on the CCC can query all EPROMs connected to it to retrieve the programmed information.

3.69 There may be one- or two-wire chains for each MOS system; a one-wire chain for non-redundant systems and a two-wire chain for redundant systems. One of the two EPROMs per MOS module is located on the left side of the module and the other on the right. For redundant systems, all left EPROMs are connected together and all right EPROMs are connected together forming two, independent one-wire chains. Each chain is connected to its own CCC creating two separate, but identical, one-wire paths. Either CCC can retrieve inventory data at anytime. For non-redundant system, only one side of EPROMS is connected together forming one, one-wire path. See figure 3-4.

Figure 3-4. One-Wire System Interface



Redundancy

3.70 The system detects and bypasses failures without affecting traffic or degrading service. All active circuits have redundant transmission and protection control. Modules operate as a pair with one being the working (active) module and the other the protection (standby). The working copy handles assigned processing tasks while the protection copy remains idle. If the working copy fails, the system activates alarms and switches to the protection copy, which becomes the working copy.

3.71 The 1677 SONET Link supports the following redundant equipment:

- Redundant switch matrixes
- Redundant control processors with independent operation
- Redundant disk storage devices for system database

3.72 The system has a redundant power protection scheme. Two power feeder inputs and returns feed each equipment rack.

Supported Client Signals

3.73 The 1677 SONET Link supports the following client signals:

- Digital Signals: DS3, EC1
- Optical Channels: OC-3, OC-12, OC-48, OC-192
- DWDM: OC-48, OC-192, Gigabit Ethernet (GIGE)

3.74 Optical channels frequencies are based on the C Band of the 100 GHz channel spacing allocation plan in the ITU-T standard grid.

3.75 The 1677 SONET Link provides Short-Reach (SR), Intermediate-Reach (IR), Long-Reach (LR), and Extra Long-Reach (XLR). Table 3-D gives the reach options for each optical channel.

Table 3-D. Optical Channel Reach Options

RATE	REACH-FIBER	WAVELENGTH	OPTICAL BUDGET
OC-3	IR-SM	1310 nm	0-12 dB
OC-12	IR-SM	1310 nm	0-12 dB
OC-48	SR-SM IR-SM LR-SM XLR-SM	1310 nm 1310 nm 1310 nm 15xx nm	0-7 dB 0-12 dB 12-24 dB 10-28 dB (400 km)
OC-192	LR-SM	15xx nm	8.5-22 dB

Switching Architecture

3.76 The 1677 SONET Link supports two switch architectures:

- 80Gb/s, 1536×1536 STS-1 Switch Fabric
- VT1.5 Switch Fabric

3.77 The 80 Gb/s, 1536×1536 switch fabric is based on a three stage Clos architecture with some added enhancements for mulitcast support. The first and third stages is performed by the IOC modules and the second stage is performed by the SSC modules. The three stage switch is a reconfigurable nonblocking switch. Therefore, every new connection has a possible path through the switch and some existing paths are moved to make room for new connections. Such changes in signal paths are done with no hits to traffic. The SSC switch fabric is redundant and supports optical protection switching and multi cast applications.

3.78 The VT1.5 switch fabric works only with SONET STS-1 signals. In order to switch other payload types, the VT1.5 architecture uses IOCs with no I/O information as switching co-processors for the system. The STS switch fabric transmits payloads to these co-processors and receives other payloads as if it were a true I/O module. The VT1.5 switch is performed by the VT Switch Card (VSC) and provides 5 Gb/s of STS-1 switching at the VT1.5 level.

3.79 For a more detailed description of the switch architectures, refer to the FUNCTIONAL OPERATION section of this manual.

Timing

3.80 Timing distribution for the 1677 SONET Link is administered by the Timing Card (TC). Timing references can be sourced through any OC-*n* interface or externally from a BITS source. The TC uses a Phased Locked Loop (PLL) to lock to one of two incoming reference signals or if both references fail, supports holdover by meeting Stratum 3 requirements. Furthermore, the TC supplies DS1s derived from incoming OC-*n* lines to provide local BITS with references traceable from the timing source of that OC-*n* signal.

3.81 For more information, refer to the TC Unit Data Sheet (UDS) in the UDS section of this manual.

Unidirectional Path Switched Ring

3.82 The system supports Unidirectional Path Switched Ring (UPSR) node configurations for path protection. UPSR is available on all optical line rates as well as OC-192 supported slot pairs. The UPSR is built from two adjacent Input/Output Cards (IOCs) of the 15RU or 18RU shelf provisioned to form UPSR nodes. The UPSR node operates with other Add-Drop Multiplexers in a ring to provide traffic protection between the nodes of the UPSR.

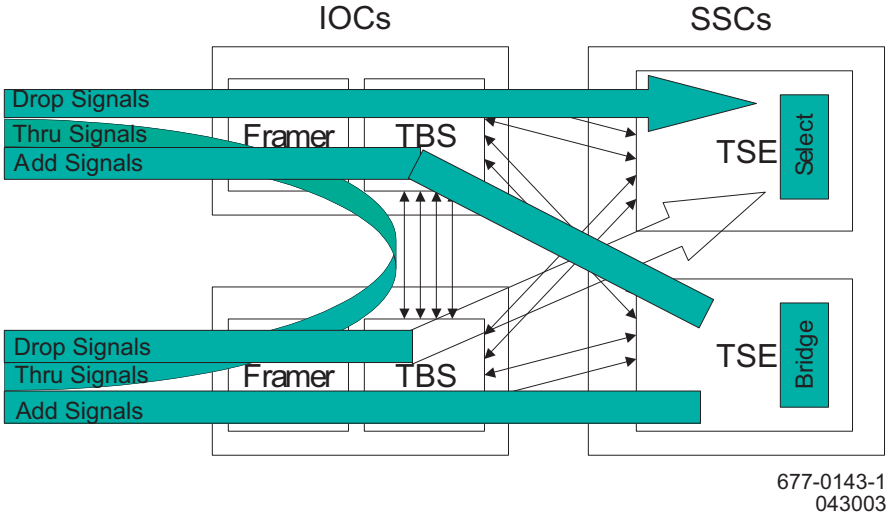
3.83 Data is transmitted simultaneously along the working and protection lines of the ring. The traffic for each line is transmitted in the clockwise and counterclockwise directions and is received by both facilities of each UPSR node. A path selector is provisioned in each two-way protection group and

selects the best signal. If a fiber cut occurs, the received signals at the protection and working lines of the node are interrupted causing the path selectors at each node to select the alternate facility in order to automatically restore traffic.

3.84 The system supports UPSR protection for line side optical interfaces. UPSR is configurable for Pass Through, Drop and Continue, Drop Terminated, Drop Non-Terminated, and Linear APS applications.

3.85 Figure 3-5 shows a basic UPSR network.

Figure 3-5. UPSR



BLSR Traffic Unaffected by Node Reset

3.86 A reboot of both Common Control Cards (CCCs) does not affect BLSR traffic.

Network Applications

Alcatel-Lucent 1603 SMX File Transfer

The system supports File Transfer Protocol (FTP) on the IP network to support file transfers to Alcatel-Lucent 1603 SMX nodes that reside on subtended rings. When the server receives a put request and the destination path name contains a special format indicating a specific TID, the FTP server opens an

OSI application layer session to a well known port on the node with that TID. All FTP data packets received are forwarded to that node.

Data Communications Channel

3.87 The Data Communications Channel (DCC) provides communication between the 1677 SONET Link shelves. Users can remotely access Network Elements (NEs) through a local NE called the Gateway Network Element (GNE). The DCC provides the system communications about configuration, software downloads, and protection state information. There is a serial DCC from each IOC to the DCC controller on the SSC. The DCC controller is responsible for maintenance and protection DCC messages. The DCC operates at a bandwidth of 4 Mb/s and at the 192 kb/s rate. The system supports a up to 66 DCCs (32 line DCCs and 34 section DCCs).

3.88 When an OC-3, OC-12, OC-48, or OC-192 is initially provisioned, DCC is disabled. Layer 1 through layer 7 provisioning parameters can be modified with the ED-ULLDCC/ULSDCC, ED-LLLDCC/LLSDCC, ED-LCPSDCC/LCPLDCC, ED-TARP, and ED-ULCOMPMR TL1 commands. The modified layer 1 through layer 7 provisioning parameters become effective when the ENT-NETIF TL1 command is used to enable DCC communications.

Operations System Interface

3.89 The 1677 SONET Link supports a full 7 layer Operations System Interface (OSI) stack with Level 1 routing. Each DCC interface can be configured to run OSI. A TL1 gateway routes TL1 commands to their provisioned destinations over the OSI network. While doing so, the system also supports destinations over Internet Protocol (IP).

SONET Compatibility

3.90 TR-TSY-000253 defines SONET standards that allow transmission products from different vendors to operate within the same network. The SONET hierarchy consists of synchronously interleaved tributaries starting with STS-1. The STS-1 rate is 51.84 Mb/s. The STS-1 frame is divided into two parts: Signal Payload Envelope (SPE) and overhead. The SPE can contain an embedded DS-3 or floating or locked Virtual Tributary (VT). Overhead is defined for maintenance, user channels and growth channels.

3.91 Overhead is layered, with overhead bandwidth allocated to each layer. Layers are assigned based on the functions performed by the different channels. This layered approach lets the equipment access information carried in a specific layer without disturbing other layers or having to demultiplex the signal.

3.92 Input/Output Cards (IOCs) accept the following facilities:

- DS3 (44.736 Mb/s)
- EC1 (51.84 Mb/s)
- OC3 (155.54 Mb/s)
- OC-12 (622.08 Mb/s)
- OC-48 (2.488 Gb/s)
- OC-192 (9.953 Gb/s)

Connection Types

3.93 The system supports termination and/or cross-connection for a variety of synchronous and asynchronous signal types. The following connection types are supported:

- Two-way (full-duplex) connections
- Two-way drop-and-continue connections
- BLSR secondary ring interconnect on working connections
- Bidirectional ring pass-through connections
- Dual-node UPSR-UPSR ring interconnections
- Drop and continue connections for GigE virtual concatenated cross-connections through OC-48 and OC-192 BLSR and UPSR configurations supporting broadcast video applications
- DS1/DS3 embedded entities within STS-1, EC1, OC-*n* or DS3 entities transmultiplexed without VSC module
- Drop and Continue connections for GigE virtual concatenated cross-connections through OC-48 and OC-192 UPSR and BLSR configurations for broadcast video applications.

3.94 Provisioning of DS1/DS3 embedded entities within STS-1, EC1, OC-*n* or DS3 entities can be transmultiplexed by the TMUX module without use of the VSC. The ENT-STS1 TL1 command provides this function.

3.95 The system allows retrieval of existing cross-connections based on the user-specified cross-connect type. The CCT parameter of the RTRV-CRS-ALL/STS1/STS3C/STS12C/STS48C/T1/T3/VT1 TL1 commands must be specified to retrieve cross-connections based on cross-connect type.

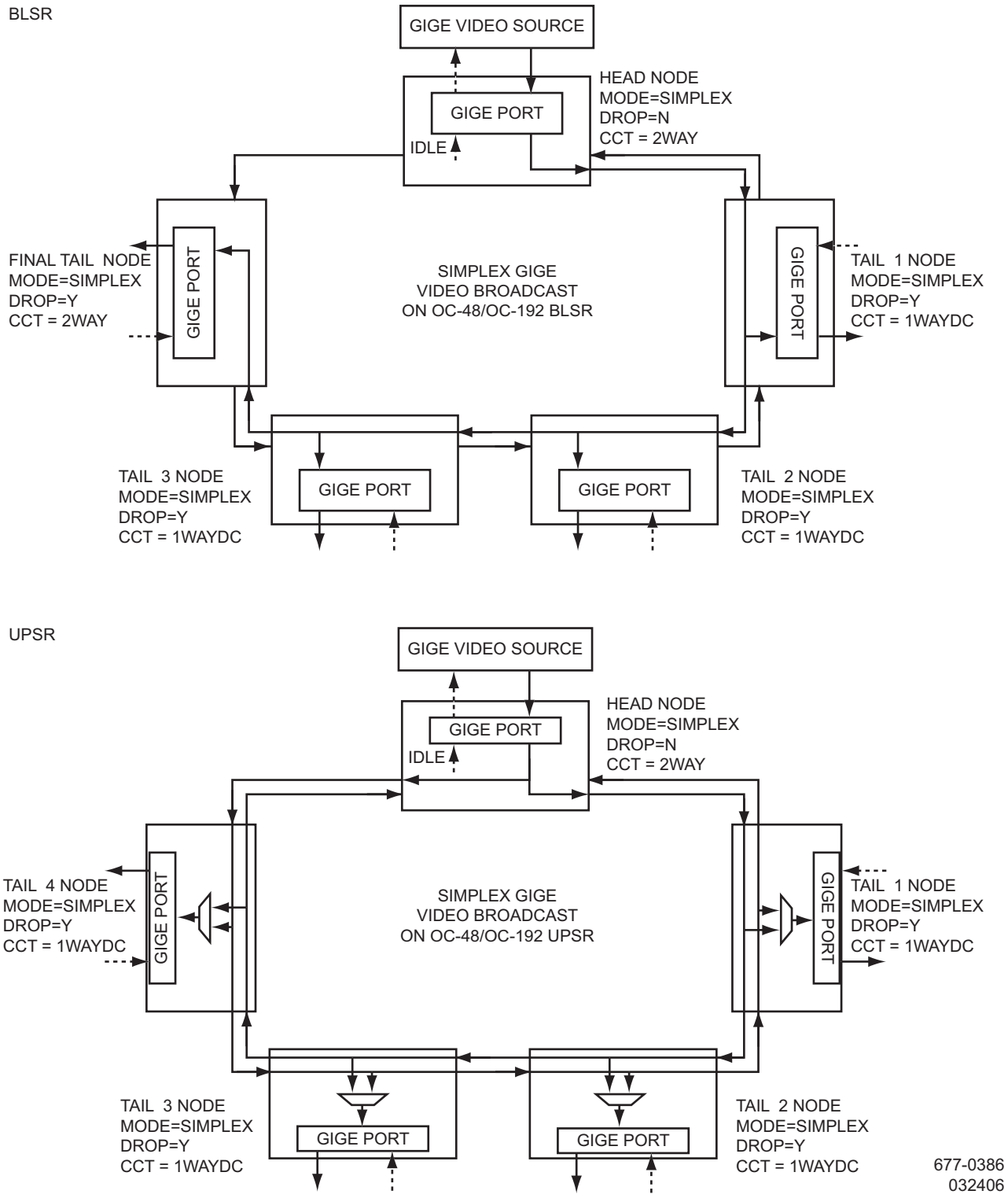
Simplex GigE Connections for Video Broadcast

3.96 The system supports drop and continue connections for GigE virtual concatenated cross-connections through OC-48 and OC-192 UPSR and BLSR configurations for broadcast video applications. The node at which the video signal is injected into the ring is designated as the head node. Other nodes on the ring that receive the signal from the head node are tail nodes. The last node to receive the signal from the head node is the final tail node. See figure 3-6.

3.97 All participating GigE facilities are provisioned for simplex mode. The provisioning parameter DROP= is set to NO (N) at the head node and YES (Y) at all of the tail nodes. This enables the head node GigE port to ignore the detected Loss Of Signal (LOS) on its incoming port. It does not matter what the head end receives from the matrix as its function is only transmission of data. The DROP= Y parameter on tail nodes enables alarms from the matrix side to the GigE facility input.

3.98 The head node is provisioned with a Cross-Connect Type (CCT) of 2WAY In both BLSR and UPSR. Tail nodes are provisioned with a CCT of 1WAYDC. The final tail node in the BLSR must have a CCT of 2WAY. If it is provisioned 1WAYDC, all the drop and continue paths around the ring will declare UNEQ-P and their cross-connections will go into the Out Of Service (OOS) state. The UPSR final tail node must be configured 1WAYDC. Because the head end in a UPSR broadcasts signal in both directions around the ring UPSR tail nodes will not show up UNEQ-P following a protection switch.

Figure 3-6. GigE Simplex Video Broadcast, BLSR and UPSR



Alarms

3.99 The 1677 SONET Link provides system, equipment, and facility alarms.

System

3.100 System alarms indicate detection of faults in the system, local office, or network. The system provides the following fault indications:

- Visible indicators on the equipment
- Contact closures that can be connected to an external alarm system

3.101 The 15RU or 18RU shelf contains one or two CCCs. The CCC provides the visual and physical interface for alarms. When alarms occur, the LEDs on the CCCs light.

3.102 The system logs all alarm and status information and maintains the status of current active alarms in the system status database. Summaries of active alarms can be retrieved on command. Alarms are reported automatically to network management equipment.

3.103 The system allows provisioning of autonomous message reporting on a user-session basis. A user can allow or inhibit all autonomous messages or specific categories of autonomous messages associated with the NE.

Equipment

3.104 Each active module contains a red status alarm indicator to identify module failure. Equipment alarms and parameters can be set system wide or individually. Equipment alarm provisioning allows the service provider to customize alarm designations. Equipment parameters define the notification code, condition type, and service effect for all equipment or individual modules. Notification codes of CR, MJ, and/or MN are system-generated autonomous messages. Internal equipment failures are declared immediately (no built-in delays).

Facility

3.105 The system provides facility alarms that indicate failures of DS1, DS3, EC1, VT1, OC-3, OC-12, OC-48, OC-192, and GIGE facility types. Facility alarms and parameters can be set system wide or individually. Facility alarm provisioning allows the service provider to customize facility alarm designations to support different service offerings.

3.106 Facility alarms have a built-in delay of 2.5 seconds before being declared and a delay of 10 seconds before being cleared.

Hardware Maintenance

Card Extraction Interlock

3.107 An extraction interlock mechanism is used by the 1677 SONET Link to notify the system that a module is about to be removed. Card Extraction Interlock requires a switch to be activated before the module is removed from the shelf. An electronic indicator notifies the control system that a module is about to be removed so that action can be taken to move signals away from the module being removed. A status LED informs the user when the module can be removed safely. All CCC, SSC, and TC modules contain card extraction interlock mechanisms.

Diagnostics

3.108 There are two forms of diagnostics performed on the 1677 SONET Link equipment: Self-Test diagnostics and Power-on diagnostics. Self-Test Diagnostics is used to test all CPU to peripheral data paths. System diagnostics ensure revision compatibility of all modules, detect fault, and isolate trouble to a replaceable module. Power-on diagnostics execute automatically when power is first applied to the system or when a module is replaced.

Fault Isolation

3.109 Fault isolation identifies fault conditions and traces them to a single module or channel. When the exact cause of a fault condition is not apparent, fault isolation generates a list of suspected components.

3.110 The user can retrieve the active internal physical paths through the NE, down to the board level, of all entities connecting the specified pair of endpoints through the system. This capability is provided by the TL1 command, FLTLOC-PATH.

3.111 The user can also retrieve the system debug logs, including card failure data and system log file data.

Remote Inventory

3.112 Remote Inventory (RI) enables the operator to remotely determine what equipment is installed in the 1677 SONET Link. The inventory data contains the following information for each replaceable unit in the system, where applicable:

- Software load revision information
- Software part number
- Firmware load revision information
- Part number/item change status/manufacturing revision
- Serial number
- Mnemonic
- Manufacturer
- Factory
- Date of manufacture
- Common Language Equipment Identifier (CLEI) code

3.113 The RTRV-EQPT command is used to provide current remote inventory information.

Performance Monitoring

3.114 The 1677 SONET Link collects path, line, and section Performance Monitoring (PM). A path is an end-to-end connection that transports digital signals at a specific rate. Path PM reflects the combined effects of multiple sources of signal degradation. In addition, any failure or degradation of signal performance can be isolated to a particular segment of the end-to-end path. PM detects problems throughout the network as well as within the system. A line connects two consecutive NEs and transports a single type of signal at a single-bit rate. A section is a portion of a line between the NE and a regenerator or between two consecutive regenerators. In the 1677 SONET Link system, Line and Section PM is for OC-*n* facilities only.

3.115 PM operates based on user provisioned PM thresholds set for support and embedded facilities. Certain parameter information defines threshold levels. The user can select the parameter types, threshold levels, direction and accumulation period for collection registers.

3.116 Collection registers store the following thresholds:

- One current 15-minute register
- One previous 15-minute register
- Thirty-one recent 15-minute registers
- One current 1-day register
- One previous 1-day register

3.117 At the end of an accumulation period, current register content transfers to the corresponding previous register and initializes to zero. Data in the previous register transfers to the top of a recent register stack, and data at the bottom of the stack is discarded.

3.118 INIT-REG commands are used to reset the collection registers to zero. Command execution initializes current 15-minute or 1-day registers to zero for monitored parameter types, monitored values, location and direction.

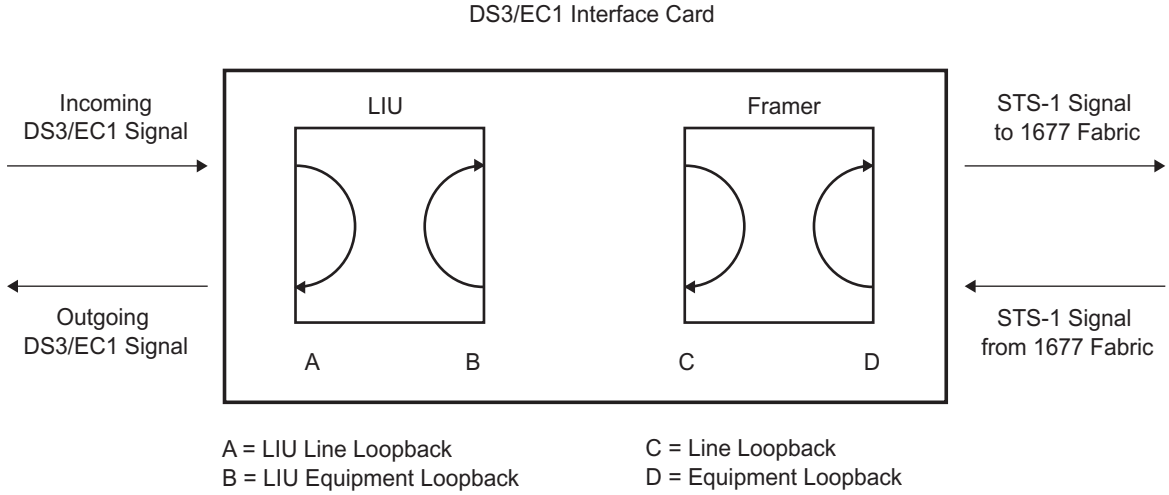
3.119 Current or historical 15-minute or 1-day PM data can also be accessed. The following PM data can be retrieved through TL1 command or software:

- Immediate or designated date and time PM
- A specific port, range of ports, or all ports
- Up to 32 historical 15-minute reports, 7 historical 24-hour reports

Loopback

3.120 The 1677 SONET Link supports DS1, DS3, EC1, OC-3, OC-12, OC-48, OC-192, and VT1 facility loopbacks. See figure 3-7 for DS3 and EC1 loopback, see figure 3-8 for OC-3, OC-12, OC-48, and OC-192 loopback, see figure 3-9 for VT1 loopback, and see figures 3-10, 3-11, and 3-12 for DS1 loopbacks. Facility loopback is loopback of a signal received from the network before the switch fabric. The AIS signal is forwarded to the switch fabric.

Figure 3-7. DS3/EC1 Loopback

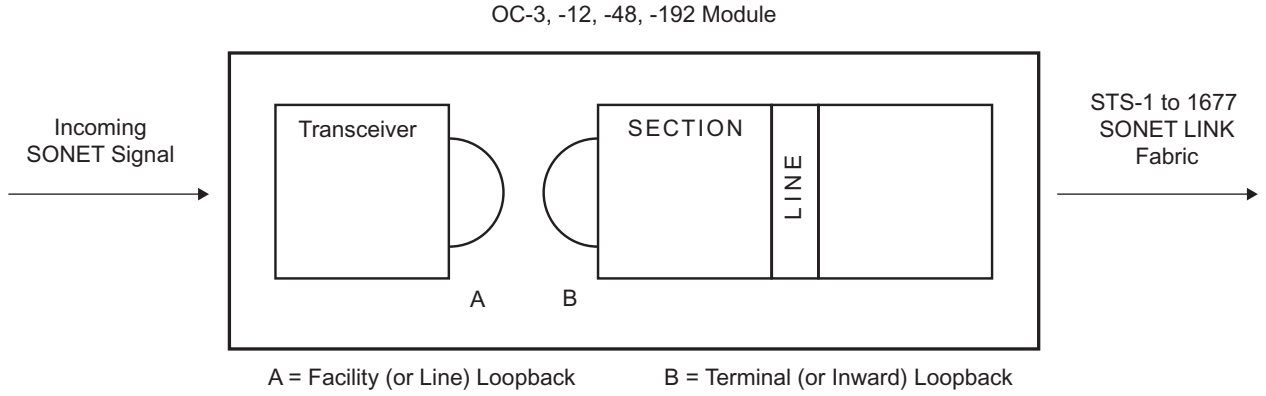


A = LIU Line Loopback
B = LIU Equipment Loopback
C = Line Loopback
D = Equipment Loopback

DS3 LIU Loopback supports a dual that is both A and B.

677-0080-1
102204

Figure 3-8. OC-3, -12, -48, and -192 Facility Loopback



A = Facility (or Line) Loopback
B = Terminal (or Inward) Loopback

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053003

Figure 3-9. VT1 Facility Loopback

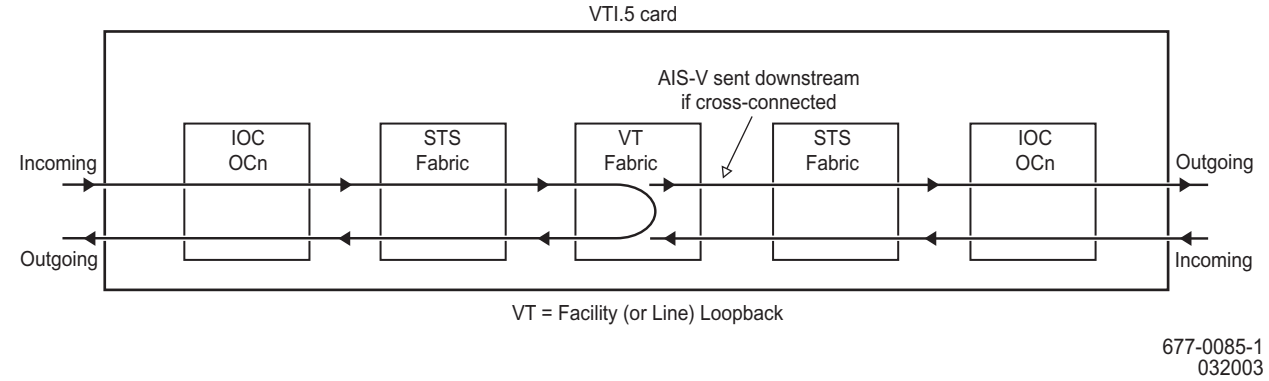


Figure 3-10. DS1(STS1-VT1-T1) Facility Loopback

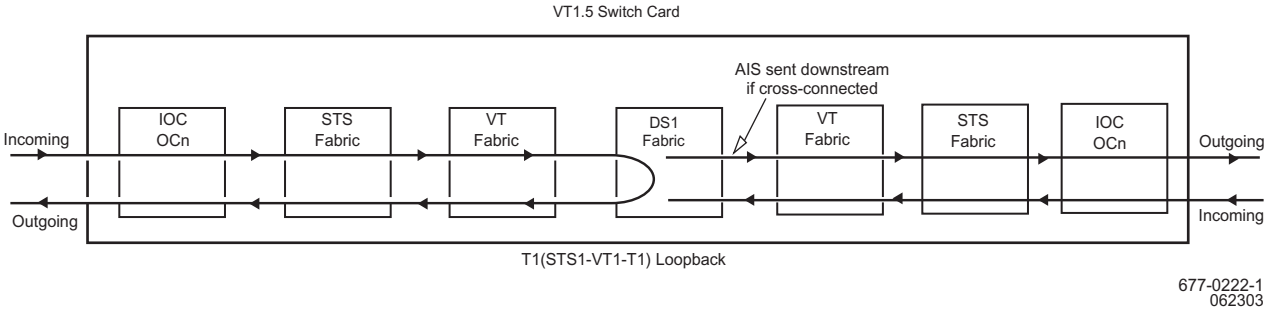


Figure 3-11. DS1(STS1-T3-T1) Facility Loopback

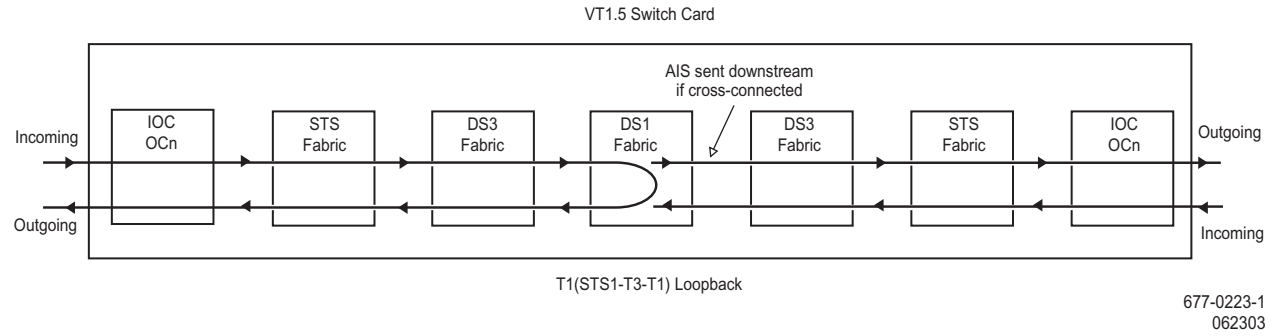
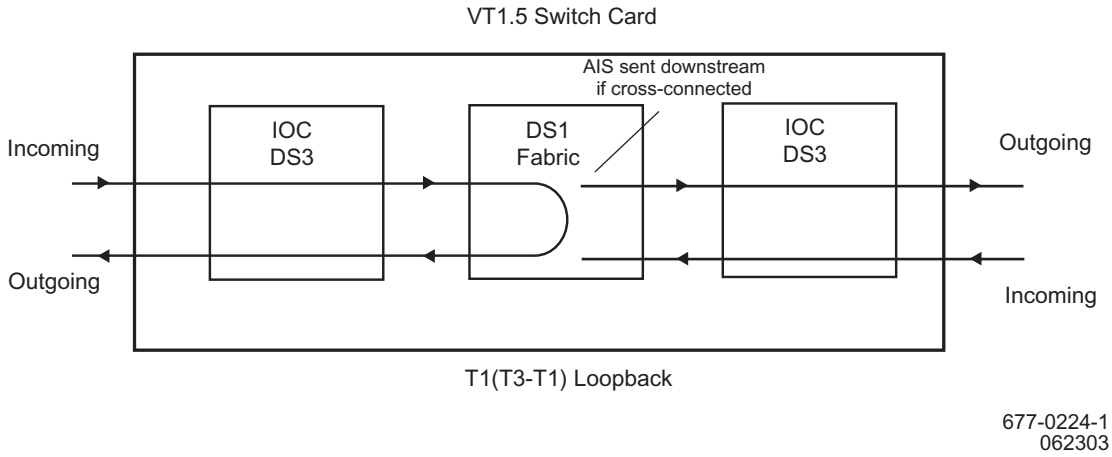


Figure 3-12. DS1(T3-T1) Facility Loopback



3.121 Equipment loopback is supported for DS3s, EC1s, OC-3s, OC-12s, OC-48s, and OC-192. Equipment loopback is loopback of a signal received from the switch fabric. The signal is still forwarded to the network.

3.122 Line loopback is supported for DS1s and DS3s. Line loopback is a complete loopback of the line signal by far-end equipment. The loopback request is sent through in-band control codes for SF and the Facility Data Link (FDL) for ESF.

3.123 ALLDS1LINE and dual loopback types are also supported for DS3s. ALLDS1LINE loopback is a line loopback of all embedded DS1 line signals by far-end equipment. The loopback request is sent through the Far-End Alarm and Control (FEAC) channel. Dual loopback is simultaneous line and equipment loopbacks at the LIU. LOCN must equal LIU for dual loopback.

3.124 DS1FEAC and payload loopback types are also supported for DS1s. DS1FEAC loopback is a complete line loopback of DS1 line signal by far-end equipment. The loopback request is sent through the FEAC channel of the DS3 in which the DS1 is embedded. Payload loopback is a loopback of DS1 payload by far-end equipment with newly-generated framing bit. The loopback request is sent through the DS1 ESF FDL.

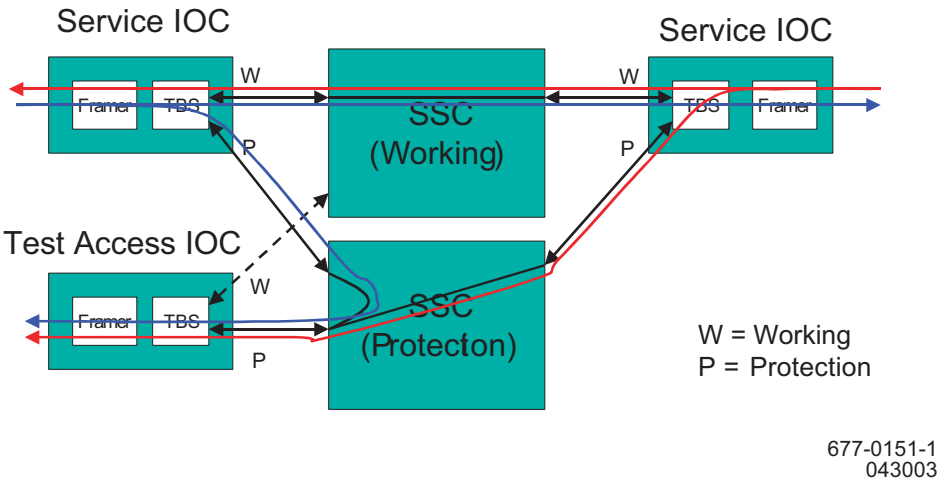
Test Access

3.125 The system supports DS0, DS1, DS3, STS-1, STS-3c, STS-12c, STS-48c, and VT1 test access.

3.126 Test access in the 1677 SONET Link system is accomplished with the use of an external test set. The 1677 SONET Link supports the standard Test Access TL1 commands, which control connectivity to the test set.

3.127 Test access on the 1677 SONET Link is accomplished by using the protection SSC to take the protection signal from the service IOC and connect it the test port. This connection is temporary and will be dropped in the event of an SSC fail-over. However, test access connections are remembered by the system and restored when both SSCs are operational. Figure 3-13 shows a multicast monitor cross connect.

Figure 3-13. Multicast Test Access Monitor



3.128 Test access allows for the monitoring, injection, and isolation of signals to isolate facility and/or equipment faults. The user can assign DS3s residing on an ECC, DS1s or VT1.5s embedded within an unprotected OC-3, or OC-12, or OC-48 or 1+1 linear APS OC-3, or DS1s embedded within a DS3 to function as a test access Facility Access Digroup (FAD) (or Test Access Digroup [TAD]) to monitor an incoming or outgoing STS-1 or DS3 embedded within an EC1, standalone DS3, or embedded DS1 or VT1.5. FAD/TAD ports can be consecutive or nonconsecutive and are assigned as FAD/TAD A and FAD/TAD B. FAD/TAD A and FAD/TAD B form a Test Access Port Pair (TAPP).

3.129 The two ports of a VT1.5 TAPP must be within the same STS-1, and the two ports of a DS1 TAPP must be within the same DS3. The two DS3 ports may reside on one ECC or two ECCs.

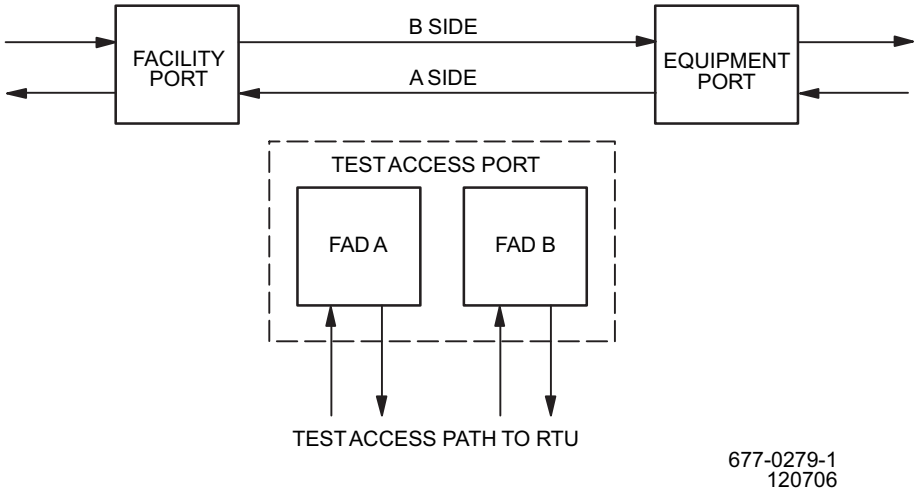
3.130 Up to 42 VT1.5 or DS1 TAPPs are allowed in one system. Up to six DS3/STS-1/STS-3c/STS-12c/STS-48c test access connections are allowed in one system.

3.131 Testing of a DS1 or VT1.5 connected to the DS0G is not permitted.

3.132 The Test Access Path (TAP) can be manipulated locally or remotely through software control. The system acts as a Digital Test Access Unit (DTAU) to a Generic Test System (GTS). The GTS uses a Remote Test Unit (RTU) to interface through the TAP to the system's TAPP. The system supports loop, monitor, and split test access connections.

3.133 The ENT-STS1/T1/T3/VT1 or ED-STS1/T1/T3/VT1 command is used to assign any ports as a TAPP (FAD/TAD A and FAD/TAD B). The CONN-TACC-STS1/T1/T3/VT1 command is then used to establish a test access connection. Equipment-side (AID) and facility-side (AID1) ports can be assigned for testing. See figure 3-14.

Figure 3-14. Test Access Model



3.134 The CONN-TACC-STS1/T1/T3/VT1 command is used to set the test mode. The CHG-ACCMD-STS1/T1/T3/VT1 command is used to change the test access mode to loop, monitor, or split connection. The RTRV-TACC command is used to retrieve information on configured test access ports.

3.135 The TAP can be manipulated locally or remotely with TL1 commands. Users can passively monitor any incoming or outgoing equipment or facility signal through TAPs. A test access connection can be made to a cross-connected circuit or a single port.

3.136 TAPPs are provisioned to be in a public pool. A public pool is accessible by any user. The user that establishes a TACC session or a user with the appropriate privilege level can execute disconnect or change TACC commands.

3.137 For more information on test access, refer to the 1677 SONET Link Operation and Administration manual (PN 3EM13851AF).

Loop

3.138 Loop test access configurations return, or loopback, a transmitted signal to the sending device after it passes through all or part of an NE or communications link. Loopbacks are created with a 1-way connection from the connection path being monitored to the appropriate FAD/TAD and another 1-way connection from the target port to itself. A technician (or a built-in diagnostic circuit) can then compare characteristics of the returned signal to those of the transmitted signal. The LOOPE (see figure 3-15) and LOOPF (see figure 3-16) modes are available. LOOPE and LOOPF interrupt service. LOOPE and LOOPF are not available for DS0 test access.

Figure 3-15. LOOPE Test Access

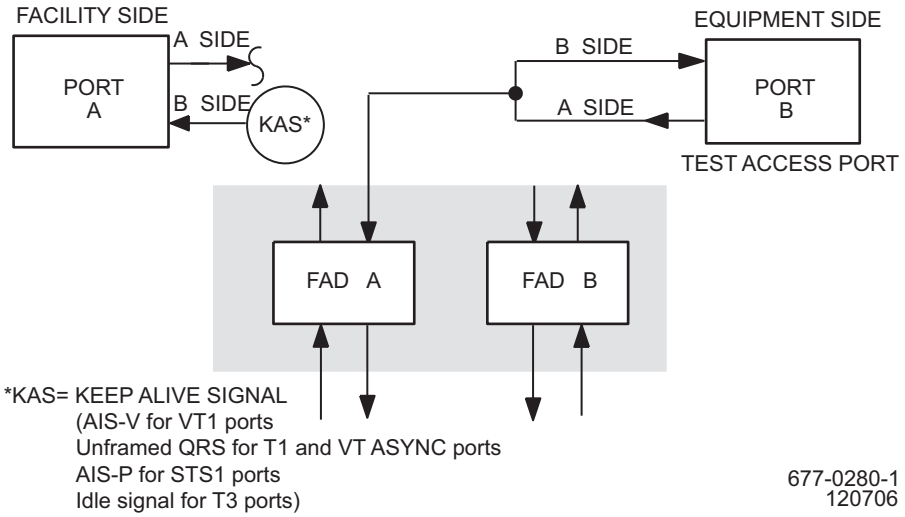
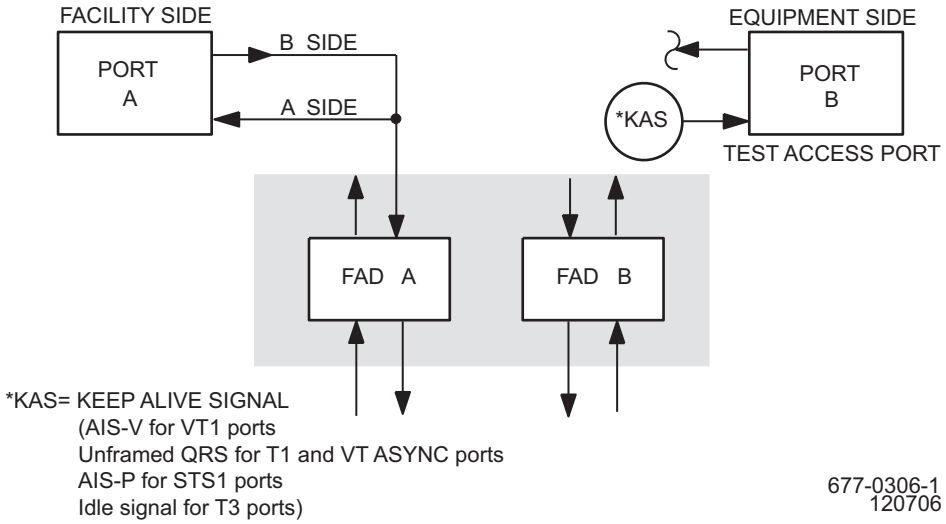


Figure 3-16. LOOPF Test Access



Monitor

3.139 Monitor connections establish a parallel connection (conference primitive to a FAD/TAD) with a DS0, DS1 or VT1.5 circuit, but normal signal transmission continues with the test access connection transparent to the signal. The incoming signal passes through the designated port and the assigned TAP at the same time. The user can execute monitor connection commands without interrupting service. The system monitors equipment (MONE) (see figure 3-17), facility (MONF) (see figure 3-18), or both (MONEF) (see figure 3-19). MONF is not available for DS0 test access.

Figure 3-17. MONE Test Access

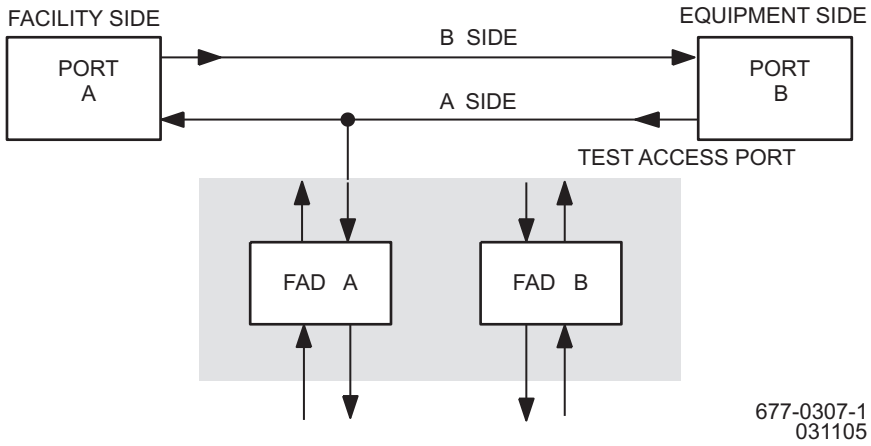


Figure 3-18. MONF Test Access

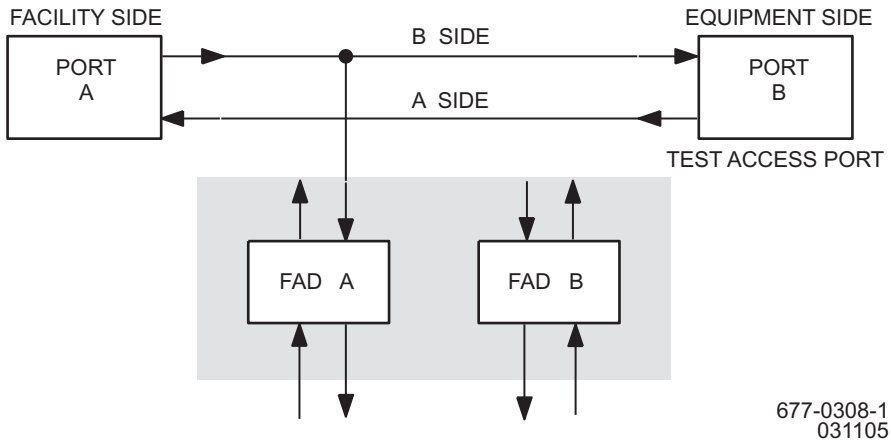
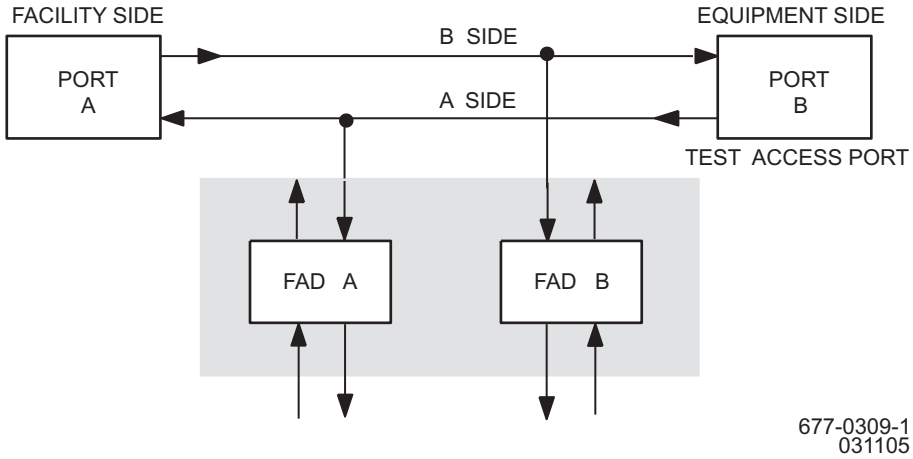


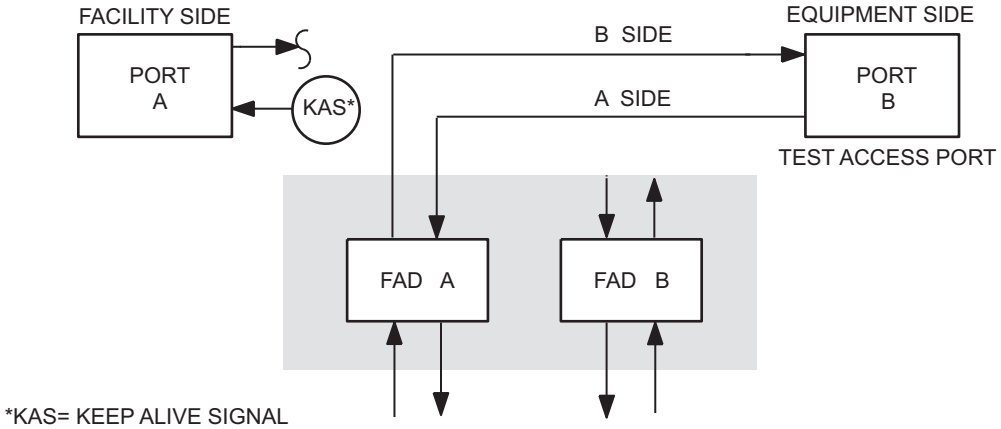
Figure 3-19. MONEF Test Access



Split

3.140 Split test access configurations separate an existing connection and form a temporary connection between a specified test port and the facility or equipment port under test. Split test access connects a normal port to the TAP (conference primitive) and also connects the TAP to the normal port (1-way primitive). This connection can be used to insert a signal onto a circuit. The following modes are available: SPLTE (see figure 3-20), SPLTF (see figure 3-21), and SPLTEF (see figure 3-22). SPLTE, SPLTF, and SPLTEF interrupt service. SPLTF is not available for DS0 test access.

Figure 3-20. SPLTE Test Access



*KAS= KEEP ALIVE SIGNAL
(AIS-V for VT1 ports
Unframed QRS for T1 and VT ASYNC ports
AIS-P for STS1 ports
Idle signal for T3 ports)

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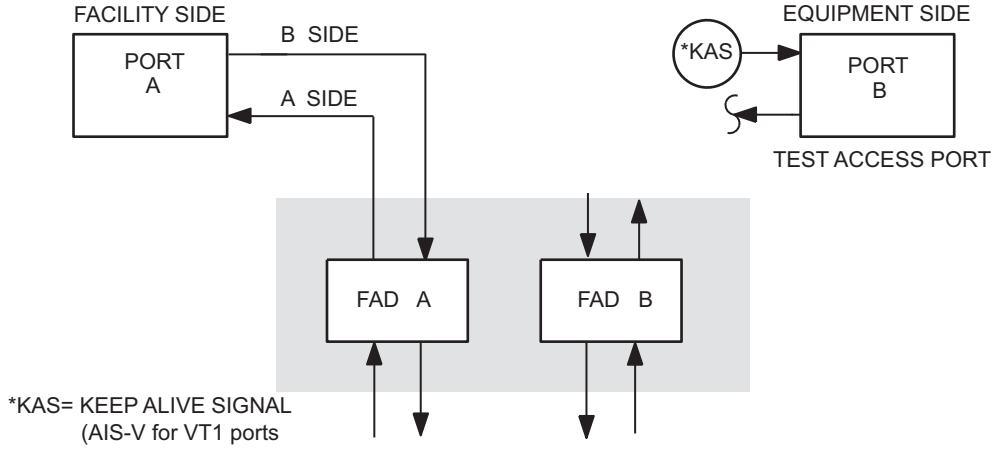
120706

Figure 3-21. SPLTF Test Access



*KAS= KEEP ALIVE SIGNAL
(AIS-V for VT1 ports
Unframed QRS for T1 and VT ASYNC ports
AIS-P for STS1 ports
Idle signal for T3 ports)

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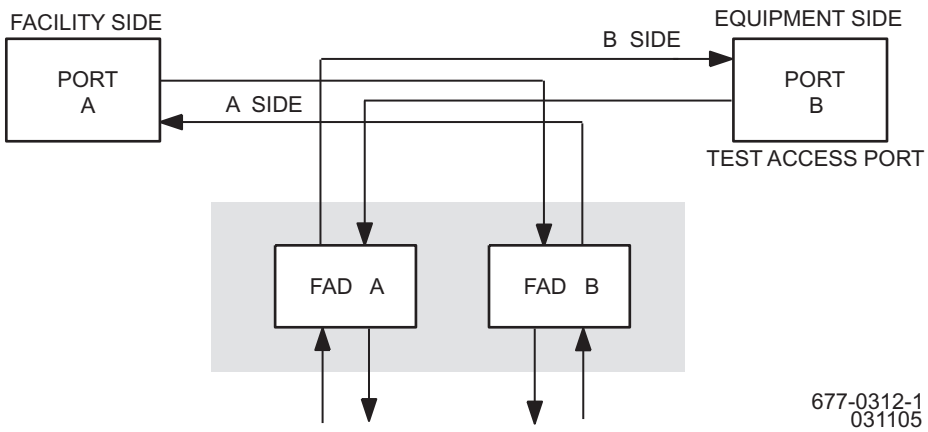
Figure 3-22. SPLTEF Test Access



Administration

Secure Password Identifier

3.141 Each UID has an associated Password Identifier (PID). A password must be a string of 1-32 case-sensitive characters. The PCONV parameter of the ED-SECU TL1 command can be provisioned to require that the password contain at least one numeric or one special character. Of these, there must be at least two alphabetic characters and one numeric character.

3.142 Password aging, deactivation on inactivity, and user account deletion on inactivity can be provisioned on accounts. Aging tracks each user to enforce periodic password changing. If a user's password age reaches the provisioned aging value and the user logs in after that time, a request for a new password is given, and a new password must be entered. If a new password is not entered before the end of the session, the user's password is deactivated when the user logs off of the system. Deactivation on inactivity deletes a password or a UID if a user has not logged into the system within a specified period of time. Only an administrator can reactivate a password or UID.

Simplified User Privilege Parameter Changes

3.143 The system accepts ED-USER-SECU parameter changes without the user having to log out and then log in. ED-USER-SECU parameter modifications are effective immediately upon command execution.

Telcordia Login

3.144 The system accepts a Correlation Tag (CTAG) and a Target ID (TID) as part of login, and compares the TID to the stored Site ID (SID). Successful and unsuccessful logins return the SID and CTAG. Successful logins also return the authorized-users-only warning message, which is provisionable with the SET-ATTR-SECULOG TL1 command.

User-Privilege-Level Command Retrieval

3.145 The system supports the RTRV-PRVG-CMD TL1 command to retrieve the commands available to users with a specified user level or Command Access Privilege (CAP). Six security levels are defined in the system:

1. READ (read only)—The user can retrieve information about the system.

2. TEST—In addition to having access to the commands available to READ user, the TEST user can initiate non-service-affecting test procedures.

3. PROV (provisioning)—In addition to having access to the commands available to TEST user, the PROV user can perform non-destructive provisioning of IOCs, ports, and interfaces.

4. CONF (configure)—In addition to having access to the commands available to PROV user, the CONF user can configure the system, performing provisioning and testing of all IOCs, ports, interfaces, and circuits. The CONF user may configure all subsystems that do not allow for system-wide effect.

5. NETADMIN (network administrator)—The NETADMIN user can configure anything in the system except user accounts.

6. SEC (security administrator)—The SEC level can be combined with any of the other five levels. It is an independent security level, whereas the first five security levels are hierarchical. A SEC user can create, delete, and modify user accounts.

User-Based REPT^DBCHG Autonomous Message Reporting

3.146 The system allows a user to enable or disable REPT^DBCHG autonomous message reporting for commands that the user issues during the current login session. Only the commands issued by the user that executed the INH-DBCHGMSG-ALL TL1 command are affected. The ALW-DBCHGMSG_ALL TL1 command can be used to enable REPT^DBCHG autonomous message reporting after it has been disabled for that session.

User Security Levels

3.147 Users can be provisioned within the following User Access Privilege (UAP) levels:

1. READ (read only)
2. TEST
3. PROV (provision)
4. CONF (configure)
5. NETADMIN (network administrator)
6. SEC (security administrator)

3.148 The first five security levels are hierarchical (lowest to highest priority). For example, a user provisioned into the PROV level has all of the privileges of the PROV level in addition to those of the READ and TEST levels. A user must be provisioned into one (and only one) of the first five levels and may or may not be provisioned within the SEC level, as well. In addition, each command is assigned to one of these privilege levels. Users with a privilege level the same as or higher than the level assigned to a command can execute that command. Unauthorized attempts to execute commands are denied.

Distinctive Software Features

3.149 The following paragraphs describe various distinctive software features. For more information on the TL1 commands used to implement them, refer to the 1677 SONET Link Commands and Messages manual (PN 3EM13852AF) for complete command descriptions.

Numeric Ranging and Grouping

3.150 Numeric ranging and grouping eliminates the repetitive entry of one command to each port. The user can specify a range or group of ports in the AID parameter of certain commands, thus reducing the amount of time to provision multiple ports. Users can provision several ports with a single command rather than one command per port.

Two-Second Command Response

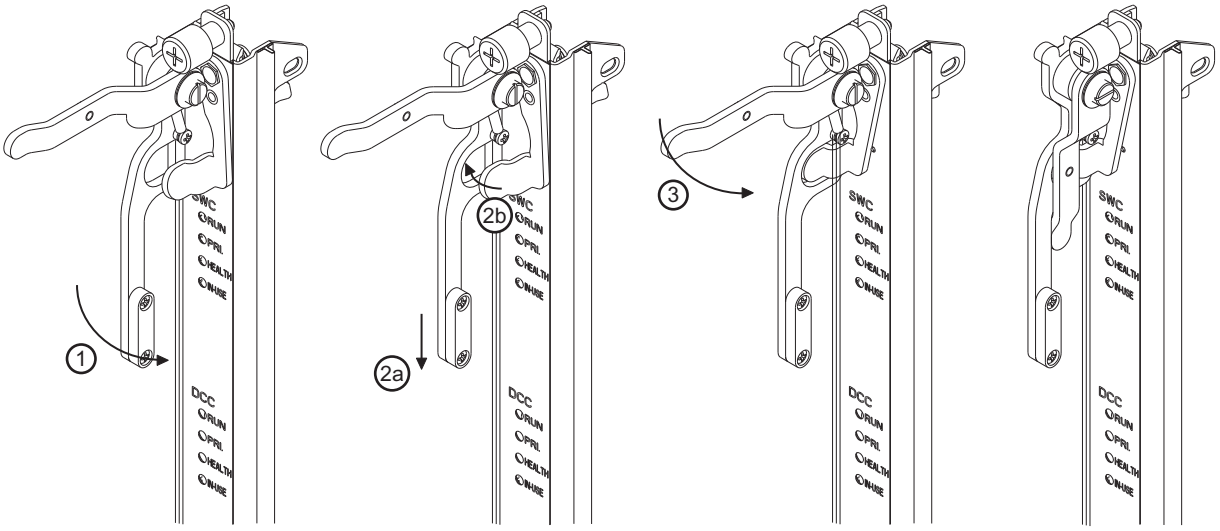
3.151 If the system is delayed in processing an input command, an in-progress message is sent to the user's VDT screen within 2 seconds of TL1 command entry.

4. EQUIPMENT LAYOUT

4.1 This section describes the 1677 SONET Link 15RU and 18RU shelf assemblies, optional standard rack configuration, modules, and mechanical equipment and the Modular Optical System (MOS) equipment. Optical and electrical connections are made on both the front and rear of the equipment. Vertical module orientation within each shelf allows air flow between modules. Insertion/extraction tabs on the faceplate of each plug-in module facilitate installation and removal. When snapped shut, the tabs also seat the module securely in the shelf connector. See figures 4-1 and 4-2 for illustrations of typical methods for module insertion and removal.

Figure 4-1. Module Insertion and Removal (Enhanced Lever Style)

INSERTION



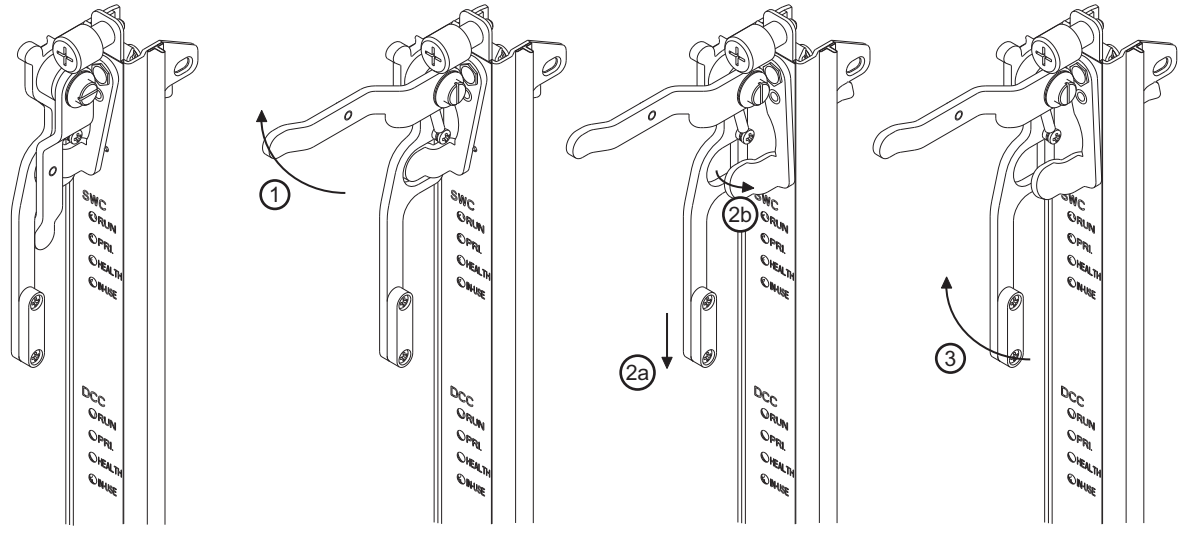
A
PUSH EJECTOR HANDLE DOWN (1) TO SEAT MODULE, THEN TIGHTEN THUMBSCREWS.

B
WHILE PULLING EJECTOR HANDLE DOWN (2a), PUSH INTERLOCK SWITCH IN (2b).

C
PUSH INTERLOCK LEVER DOWN (3).

D
LEVER FULLY LATCHED

REMOVAL



A
LEVER FULLY LATCHED

B
LIFT INTERLOCK LEVER UP (1).

C
WHILE PULLING EJECTOR HANDLE DOWN (2a), PUSH INTERLOCK SWITCH OUT (2b).

D
AFTER UNSCREWING THUMBSCREWS, PUSH EJECTOR HANDLE UP (3).

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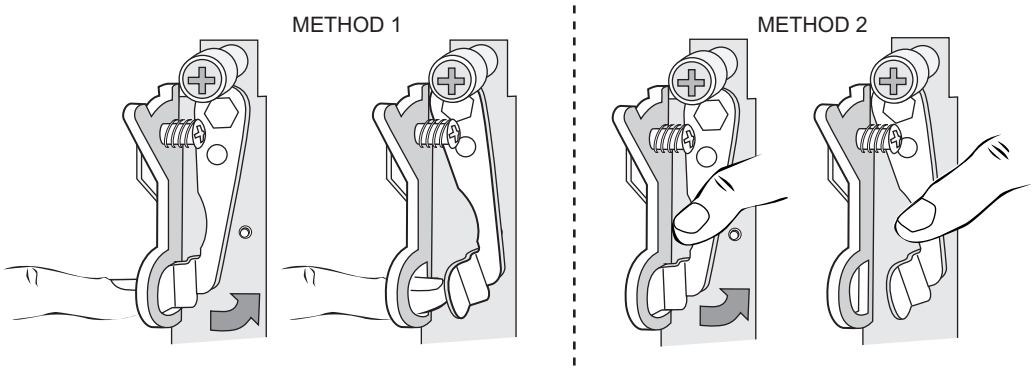
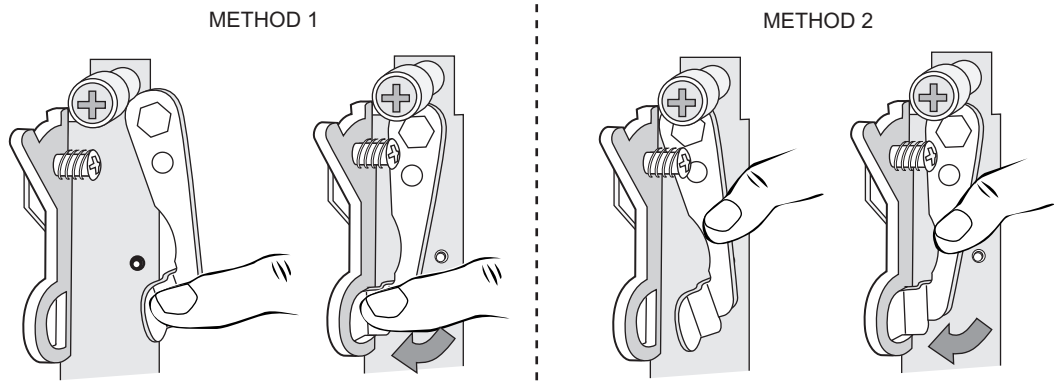
050505

Figure 4-2. Module Insertion and Removal (Old Lever Style)



UNLOCKING TABS (MODULE REMOVAL)



LOCKING TABS (MODULE INSERTION)

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110404

Rack Assembly

4.2 The 15RU or 18RU shelf is mounted into an American National Standards Institute (ANSI)-compliant customer rack. The customer is responsible for supplying the ANSI rack and Power Distribution Unit (PDU). Up to two 15RU or 18RU shelves can be installed into one ANSI rack. The 1677 SONET Link is sold as a single shelf when equipped in a customer rack.

4.3 Refer to table 4-A for ANSI rack specifications.

Table 4-A. ANSI Rack Specifications

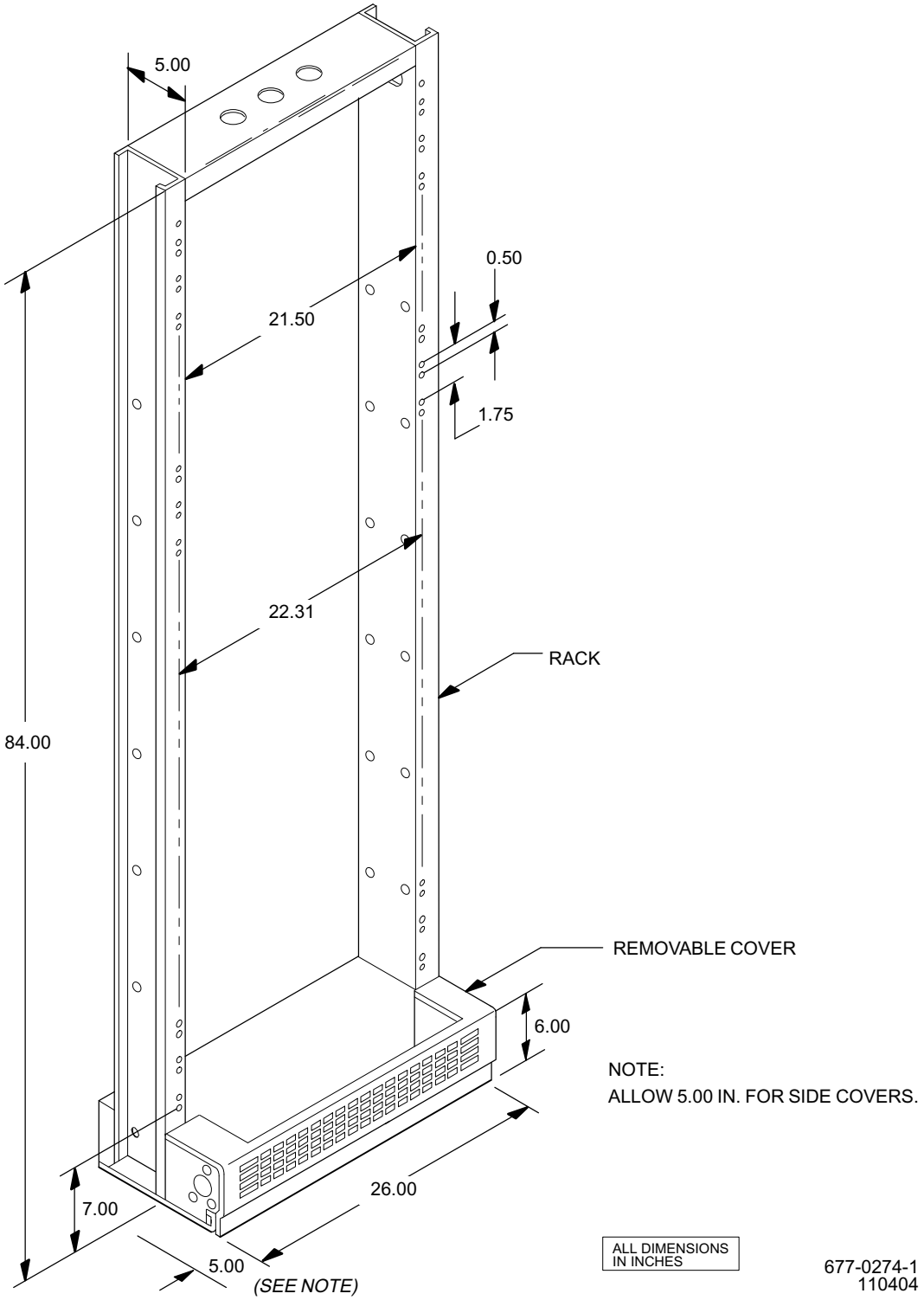
ITEM	CHARACTERISTICS
1. Description	Unequal-flange rack that provides mounting space for shelves
2. Physical dimensions	
Height	7 ft. 0 in.
Width	26 in.
Depth	12 in.
3. Circuit capacity	1536×1536 STS-1 switch (80 Gb/s); 2688 VT1.5s (80 Gb/s) per 15RU or 18RU shelf
4. Alarm Protocol	RS-232
5. Power requirement	
Input voltage	-48 V dc

4.4 Optionally, the 18RU shelf can be sold as part of a standard rack configuration. A standard rack configuration is equipped the following equipment:

- One or two 18RU shelves
- Supporting equipment such as DS1 splitters, DS3/EC1 connector panels, and a Quad Input Power Distribution Unit (PDU-Quad)
- Covers and trim panels

4.5 Standard rack assemblies are 23-inch, unequal-flange, closed-channel earthquake racks. A rack is 7 feet high, 26 inches wide, and 15.5 inches deep. The installed width of each rack, including trim and cable, is 36 inches. A rack without shelves, trim, and cable is 7 feet high, 25.94 inches wide, and 10.09 inches deep. See figure 4-3. Each rack uses 1.75-inch Electronic Industries Association (EIA) rack mounting increments. A standard 7-foot rack provides 43 EIA rack increments. Standard racks meet EIA specifications regarding earthquake resistance.

Figure 4-3. Equipment Rack (PN 1AD014120032)



4.6 Refer to table 4-B for equipment rack specifications for the standard rack assembly.

Table 4-B. Equipment Rack Specifications

ITEM	CHARACTERISTICS
1. Description	23-inch, unequal-flange earthquake rack that provides mounting space for shelves in areas where zone 4 earthquake compliance is necessary
2. Physical dimensions (rack) Height Width Depth	 7 ft 0 in. 26 in. 15.5 in.
3. Circuit capacity	1536×1536 STS-1 switch (80 Gb/s); 2688 VT1.5s (80 Gb/s) per 18RU shelf
4. Alarm Protocol	RS-232
5. Power requirement Input voltage	 -48 V dc

4.7 Modular Optical System (MOS) modules install directly into the ANSI rack and are sold as single modules. For more information on 1677 SONET Link or MOS shelf installation, refer to the 1677 SONET Link Installation Practices manual (PN 3EM13849AF).

Constraints

4.8 Certain constraints must be considered when integrating the system into a physical network environment. Each installation presents its own set of considerations.

Environment

4.9 The system is designed for placement in a conventional Central Office (CO) or switching center environment. Refer to table 4-C for environmental operating conditions.

Table 4-C. Environmental Condition Specifications

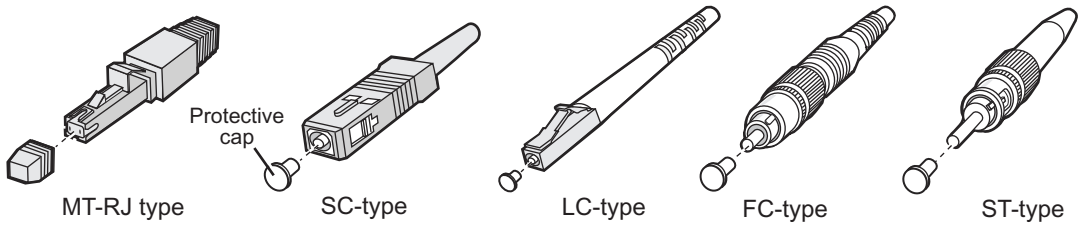
ITEM	Operating	Non-Operating
1. Ambient temperature Long term Short Term	 0 °C to 40 °C (32 °F to 104 °F) -5 °C to 50 °C (23 °F to 122 °F)	
2. Relative humidity	5 to 90% (without condensation)	5 to 90% (without condensation)
3. Altitude	0 to 3048 m (0 to 10,000 ft.)	0 to 3048 m (0 to 10,000 ft.)
4. Cooling	Forced air	
5. Vibration and shock	Earthquake requirements	
6. Duty cycle	Continuous, unattended	

Cables, Connectors, and Adapters

4.10 The 1677 SONET Link uses both metallic and fiber-optic cables. Fiber-optic cables connect between modules in the 1677 SONET Link, the network, and the optical modules of the Modular Optical System. They are available for the 1677 SONET Link in different lengths, connector styles, and fiber types.

4.11 Connector types include SC-type, LC-type, or MT-RJ type. The FC-type and ST-type connectors are not used on the 1677 SONET Link, but adapter cables are available for connecting network cables that have these types of connectors to the node. Fiber-optic cable types include both single-mode (SM) and multimode (MM) and are available in a simplex cable (one fiber conductor) or duplex cable (two fiber conductors). See figure 4-4 for an illustration of fiber optic cable connector types.

Figure 4-4. Fiber-optic Connector Types



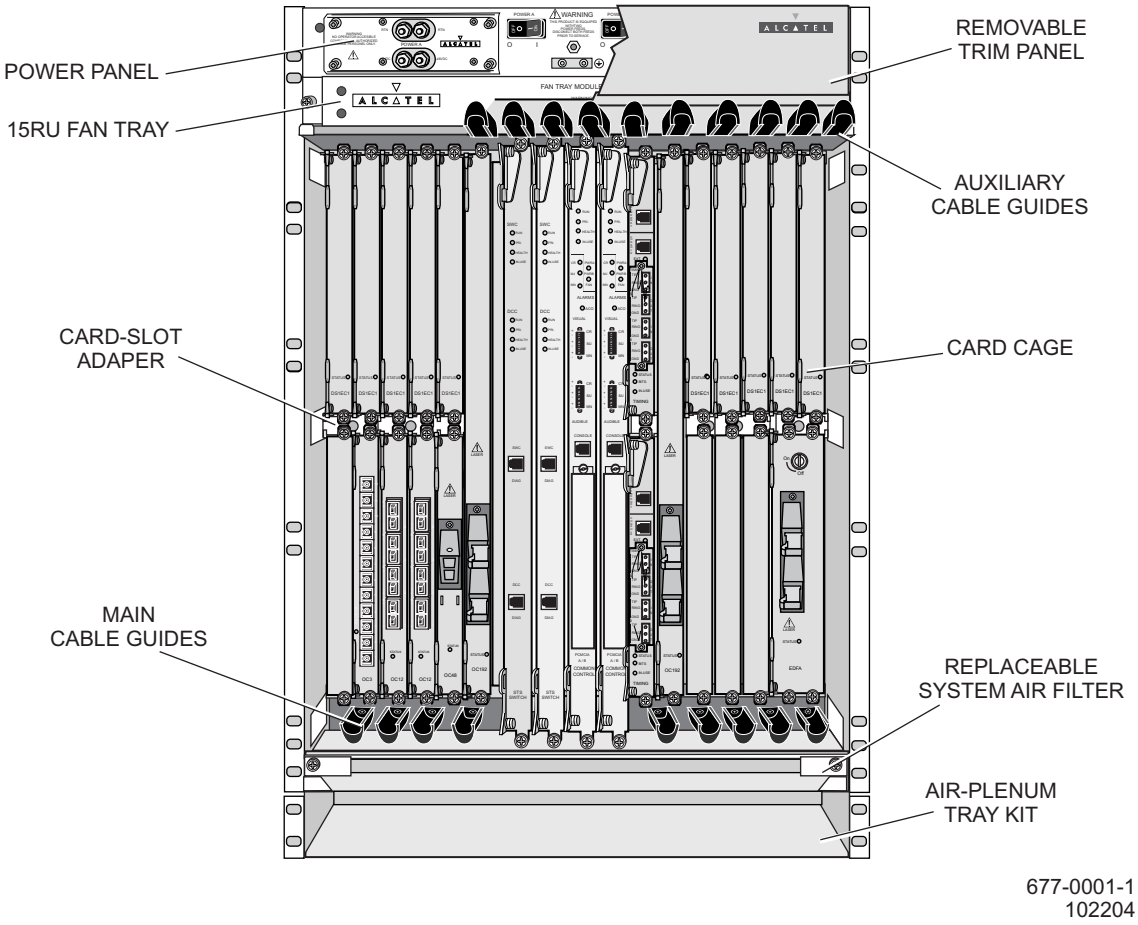
4.12 Metallic cables are used on the console port, the optical management bus jacks, the network management port (Ethernet port), and the DS3 ports on the connector panels. Refer to the unit Data Sheets (UDS) section of this manual to find out what type of cable and connectors individual modules use.

Shelf Assemblies

15RU Shelf

4.13 The 15RU shelf is a 19-inch wide, 12-inch deep, 26-inch high (15RU) rack-mount shelf. It is comprised of a card cage, a power panel, a field-replaceable 18RU fan tray, and a field-replaceable air filter. See figure 4-5.

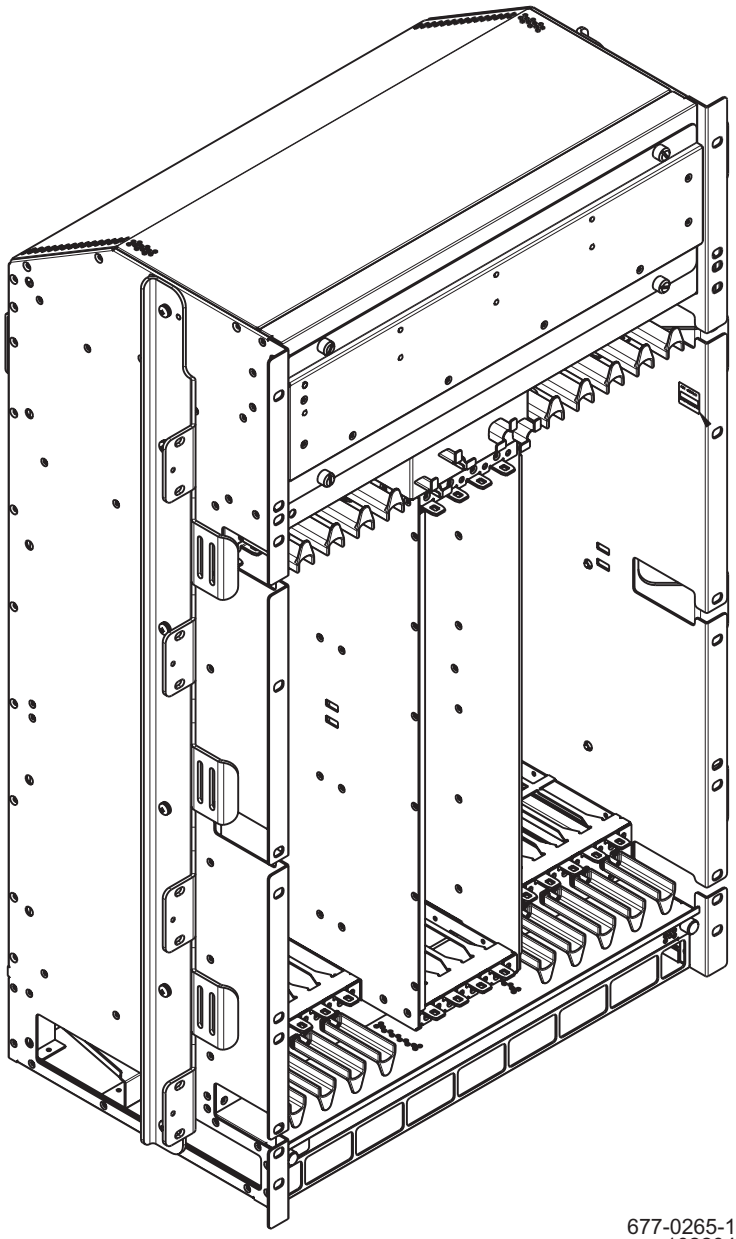
Figure 4-5. 15RU Shelf



18RU Shelf

4.14 The 18RU shelf is a 19.12-inch wide, 12.67-inch deep, 31.40-inch high (18RU) rack-mount shelf. It is comprised of a card cage, a power panel, a field-replaceable 18RU fan tray, and a field-replaceable air filter. See figure 4-6. The 18RU shelf provides access to the 18RU fan tray without disturbing cables mounted in the cable guide.

Figure 4-6. 18RU Shelf



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102204

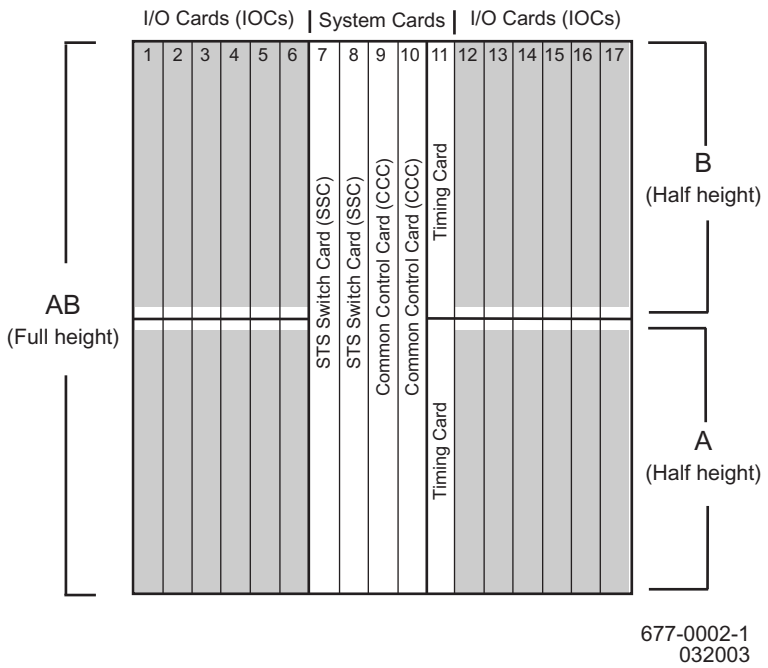
15RU or 18RU Shelf Card Cage

4.15 The 17-slot card cage holds the system modules and the Input/Output Cards (IOCs). System modules are located in the middle slots of the shelf, slots 7–11. IOCs are located in the left and right outside slots, 1–6 and 12–17. Slot numbers are labeled along the top edge and bottom edge of the card cage.

4.16 System modules and IOCs are either half-height or full-height size. When a slot contains a half-height module, the lower half of the slot is designated A and the upper half is designated B. When the slot contains a full-height module, the slot is designated AB. See figure 4-7. For example, two half-height modules in slot 3 are identified as the 3A module and the 3B module. One full-height module in slot 3 is identified as the 3AB module. Two types of removable card-slot adapters can convert either two adjacent IOC slots or three adjacent IOC slots for half-height module applications. A card-slot adapter to convert one slot is not supported.

4.17 System modules install into specific slots of the card cage. Mechanical keying prevents users from installing them in the wrong slots. IOCs, on the other hand, are generally installed in any available IOC slot. See figure 4-7. When an IOC requires installation in a specific slot, software keying notifies the user through a warning message or by lighting the module front panel LED if the module is in the wrong slot.

Figure 4-7. Card-Cage Numbering and Card Location



Modules

System Modules

4.18 System modules include the following:

- SSC 103 80 Gb STS Switch Card (SSC)
- CCC 104 Common Control Card (CCC)
- TC 301 Stratum 3 Timing Card (TC)

4.19 These modules occupy specific slots in the card cage. Mechanical keying prevents users from installing system modules of the same size in the wrong slots.

4.20 The system requires at least one SSC, a CCC, and a TC for minimum operation, and requires two of each module for redundant operation. The system also requires at least one IOC for minimum operation. For automatic protection switching (APS) the node requires 1+1 OC-*n* modules or 1*xN* ECC modules. To support the optional DS0 Groomer, the 3EM12295AD SSC104 must be equipped.

4.21 For fault protection, the system modules support redundancy. Redundancy is accomplished by installing a primary module and a secondary module in adjacent slots. During operation the first module to become operational is designated the primary module and the other as the secondary module. The modules remain in these operating states unless a problem with the primary module is detected or a user intentionally changes the module state through software or by activating a module interlock switch manually. If any of these actions occurs, the secondary module will become the primary module, and the old primary module will become the secondary module.

Input/Output Cards (IOCs)

4.22 Input/Output Cards (IOCs) include the DS0 Groomer (DS0G), Erbium-Doped Fiber Amplifier (EDFA), DS3/EC1 interface modules, the gigabit Ethernet, line modules, and the transmultiplex module. The DS0G module provides 2.5 Gb/s capacity of unidirectional DS0-level switching and grooming. The EDFA module is a system controllable in-line and/or pre-amplifier that provides up to +23dB of signal gain to the output signal. DS3/EC1 interface modules provide SONET section, line, and path termination. The gigabit Ethernet supports two IEEE 802.3-compliant ports

operating in serial mode. Line modules (all OC-*n* modules) provide SONET section termination and line termination. The TMUX performs DS3-structured STS-1 to VT-structured STS-1 translation and DS3-DS1 and VT-DS1 path monitoring. The following IOCs are supported by the 1677 SONET Link:

- DS0 Groomer Module (DS0G)
- EDFA 10*x* Erbium-Doped Fiber Amplifier (EDFA)
- IFC1 201 12-Port DS3/EC1 Interface Card (ECC-12P)
- IFC2 10*x* 2-Port Gigabit Ethernet, LX (GIGE-2P)
- IFC4 10*x* 2-Port Gigabit Ethernet, SX (GIGE-2P)
- LC1 10*x* 12-Port MM OC-3 Line Card (OC3-12P)
- LC2 10*x* 12-Port IR OC-3 Line Card (OC3-12P)
- LC3 10*x* 12-Port LR OC-3 Line Card (OC3-12P)
- LC4 10*x* 4-Port MM OC-12 Line Card (OC12-4P)
- LC5 10*x* 4-Port IR OC-12 Line Card (OC12-4P)
- LC6 10*x* 4-Port LR OC-12 Line Card (OC12-4P)
- LC10D *x*3*x* 1-Port XLR OC-48 Line Card (OC48-1P)
- LC7D 10*x* 1-Port SR OC-48 Line Card (OC48-1P)
- LC7ID 10*x* 1-Port IR OC-48 Line Card (OC48-1P)
- LC8D 10*x* 1-Port LR OC-48 Line Card (OC48-1P)
- LC12D *x*3*x* 1-Port LR OC-192 Line Card (OC192-1P)
- TMUX 201/301 2.5 Gb/s Transmux (TMUX)

Miscellaneous Assemblies

4.23 Other system assemblies include the power panel, 15RU or 18RU fan tray and related equipment, PDU-Quad, DS1 splitter, DS3/EC1 connector panel.

Power Panel

4.24 The power panel provides an interface for an external -48 V dc power source. Either a single external power source or two independent external power sources, labeled PWRA and PWRB for identification, can be connected to the node. When the node has one power source, a power source failure will cause the node to shut down. When the node has two independent power sources and one fails or is turned off, the node will still operate properly. The power panel also houses components that condition and filter the A and B input power.

4.25 The 15RU power panel is on the front of the 15RU shelf. See figure 4-8. The 18RU power panel is on the rear of the 18RU shelf. See figure 4-9.

Figure 4-8. 15RU Power Panel

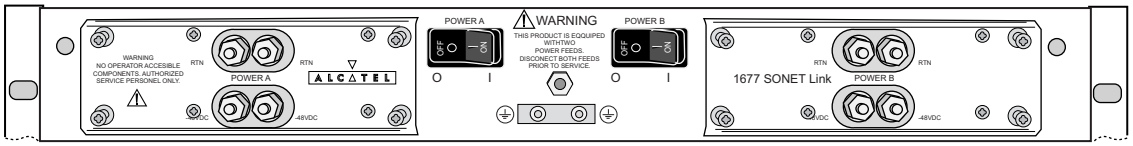


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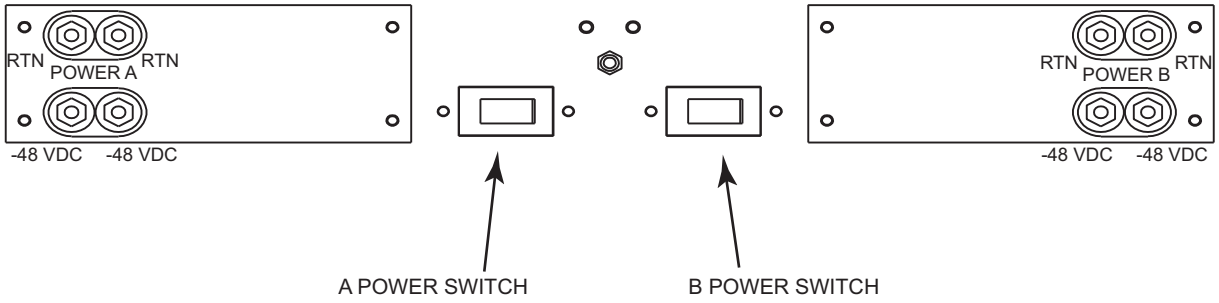
Figure 4-9. 18RU Power Panel



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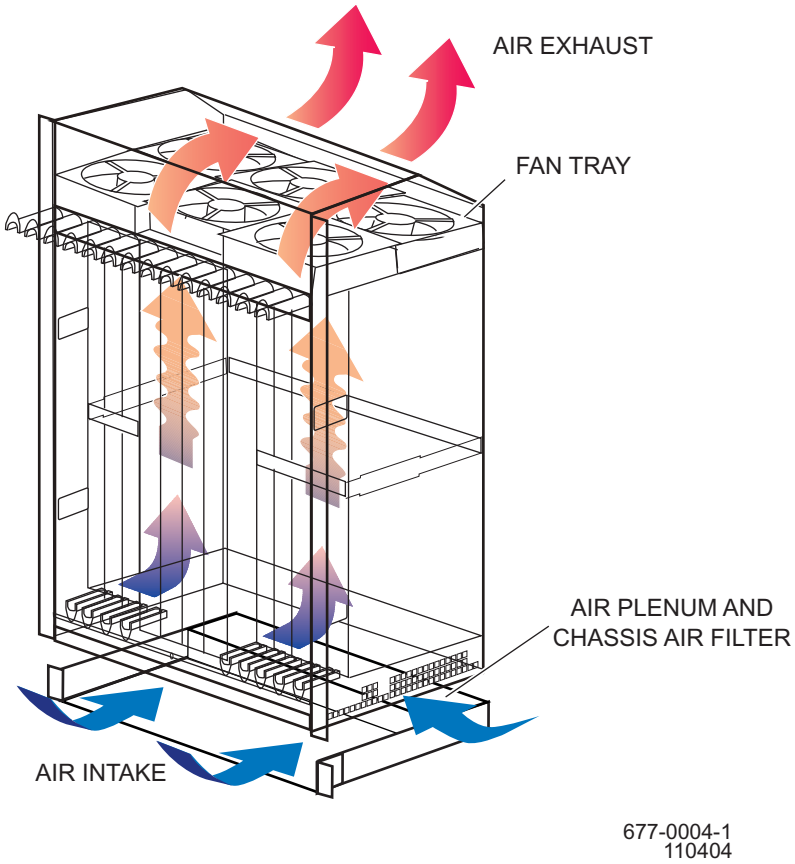
4.26 The PWRA and PWRB lights on the front panel of the CCC indicate when each power source is on, off, failed, or not connected. When the system is using two CCCs, both CCC LEDs light providing identical power information.

15RU or 18RU Fan Tray

4.27 The 1677 SONET Link uses a forced-air cooling system, which is driven by the 15RU or 18RU fan tray. See figure 4-10. The fan-tray, which is at the top of the shelf, draws ambient air into the shelf through the air plenum at the bottom of the shelf. The air is then sent through the bottom front and sides of the shelf. Air passes through a high dust-arresting polyurethane air filter, and over the surfaces of the modules. Heated air exits the top rear of the shelf. For the 15RU shelf, the 1RU-high air-plenum tray attaches to the rack using separate mounting brackets. The air-plenum tray is integrated into the 18RU shelf.

Figure 4-10. Forced-Air Cooling System



4.28 The removable fan tray contains six multi-speed fans and a fan-controller module. The six fans provide 1:N protection, which prevents the 1677 SONET Link from overheating if one of the fans fails. The fan-controller module monitors the rotational speed of each fan. When all fans are rotating at the correct speed, the FAN light on the CCC lights green to indicate the fan tray is without error. If one fan fails, all other fans speed up to provide more air

flow, and the FAN light turns amber, indicating a replacement of the fan tray is necessary within 72 hours. If two or more fans fail, the FAN light becomes red, indicating replacement of the fan tray is needed immediately to prevent the node from overheating.

PDU-Quad

4.29 The optional PDU-Quad provides battery power distribution for the standard rack configuration. An Alarm LED indicates either loss of A or B power or a tripped breaker or fuse.

DS1 Splitter

4.30 A DS1 splitter duplicates BITS inputs and sends primary and secondary BITS signal to the TC 301 Timing Cards (TCs) in the 18RU shelf. One DS1 splitter is equipped for each 18RU shelf in a standard rack configuration.

DS3/EC1 Connector Panel

4.31 A 48-port DS3/EC1 connector panel provides DS3/EC1 signal connections for up to four ECC-12Ps. A 96-port DS3/EC1 connector panel provides DS3/EC1 signal connections for up to eight ECC-12Ps. A DS3/EC1 provides the ability to switch all DS3/EC1 signals from a working ECC-12P to the associated protection ECC-12P. A DS3/EC1 connector panel is mounted on the rear of a 15-RU or 18-RU shelf when the shelf is equipped with ECC-12Ps.

Modular Optical System

4.32 The following Modular Optical System (MOS) modules are available:

- ADME 013 E-Band East Add/Drop Module (ADM)
- ADMW 013 E-Band West Add/Drop Module (ADM)
- ADME 014 F-Band East Add/Drop Module (ADM)
- ADMW 014 F-Band West Add/Drop Module (ADM)
- DCME 020 20 km East Dispersion Compensation Module (DCM)
- DCMW 020 20 km West Dispersion Compensation Module (DCM)
- DCME 040 40 km East Dispersion Compensation Module (DCM)
- DCMW 040 40 km West Dispersion Compensation Module (DCM)
- DCME 060 60 km East Dispersion Compensation Module (DCM)
- DCMW 060 60 km West Dispersion Compensation Module (DCM)
- DCME 080 80 km East Dispersion Compensation Module (DCM)
- DCMW 080 80 km West Dispersion Compensation Module (DCM)
- DWDME 101 E-Band E-Dense Wavelength Division Multiplexer (DWDM)
- DWDMW 101 E-Band W-Dense Wavelength Division Multiplexer (DWDM)
- DWDME 102 F-Band E-Dense Wavelength Division Multiplexer (DWDM)
- DWDMW 102 F-Band W-Dense Wavelength Division Multiplexer (DWDM)

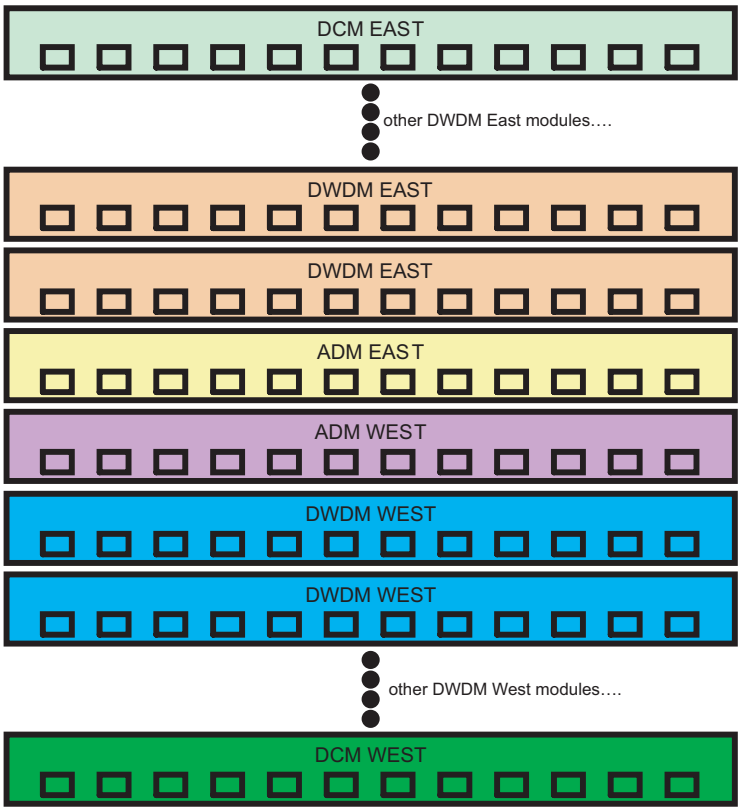
4.33 ADMs separate bands of 4 to 8 optical signals to be filtered by the DWDMs to individual optical carriers for the 1677 SONET Link line modules. DWDMs also separate Legacy 1310 nm signals. DCMs compensate for chromatic dispersion in OC-192 applications.

4.34 MOS modules are classified by using East and West logic, where the two fiber paths of a ring are divided into East and West portions for protection purposes. East and West modules are assembled into the rack to correspond with customer designated directions. Fiber coming from East modules is routed

to the right side of the rack. Fiber coming from West modules is routed to the left side of the rack. Network traffic entering an East module comes from the East side of the Central Office (CO) and/or from a node to the East. The reverse is true for West modules. Light paths from the left and right sides of every MOS module have two distinct light paths that never cross.

4.35 East modules mount above West modules and ADMs mount between DWDMs. When DCMs are used, they mount above ADMs and DWDMs for East DCMs and below ADMs and DWDMs for West DCMs. See figure 4-11 for the recommended MOS East/West module placement.

Figure 4-11. Recommended MOS Module Placement



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5. UNIT DESCRIPTIONS

5.1 Refer to table 5-A for brief descriptions of the racks, 15RU and 18RU shelves, supporting equipment, and modules.

Table 5-A. 1677 SONET Link Unit Descriptions

UNIT	DESCRIPTION
Rack PN: 1AD014120032 Qty: Configuration dependent	A single rack houses up to two 15RU or 18RU shelves and supporting equipment. It provides zone 4 earthquake compliance and is an unequal-flange rack. A single rack is 7 feet high, 26 inches wide, and 15.5 inches deep.
15RU Shelf PN: 3EM12277AA Qty: Up to 2 per ANSI rack	The 15RU shelf installs into a standard ANSI rack. It is comprised of a power panel (front of card cage), card cage, and a 15RUfan tray.
18RU Shelf PN: 3EM12334AC Qty: Up to 2 per ANSI rack	The 18RU shelf installs into a standard ANSI rack. It is comprised of a power panel (rear of card cage), card cage, and a 18RUfan tray.
15RU Fan Tray PN: 3EM12279AA Qty: 1 per 15RU shelf	The 15RU fan tray contains six multi-speed fans and a fan-controller to provide 1+n protection, preventing overheating of the system.
18RU Fan Tray PN: 3EM12307AA Qty: 1 per 18RU shelf	The 18RU fan tray contains six multi-speed fans and a fan-controller to provide 1+n protection, preventing overheating of the system.
15RU 48-Port DS3/EC1 Connector Panel PN: 3EM12220AA Qty: Up to 4 per 15RU shelf	15RU 48-port DS3/EC1 connector panels are mounted on either the equipment rack or the rear of the 15RU shelf. 48-port DS3/EC1 connector panels provide 48 DS3 connections and connect to ECC-12Ps through BNC connectors accessible at the rear of the 15RU shelf once connector covers are removed.
15RU 96-Port DS3/EC1 Connector Panel PN: 3EM12221AA Qty: Up to 2 per 15RU shelf	15RU 96-port DS3/EC1 connector panels are mounted on either the equipment rack or the rear of the 15RU shelf. 96-port DS3/EC1 connector panels provide 96 DS3/EC1 connections and connect to ECC-12Ps through BNC connectors accessible at the rear of the 15RU shelf once connector covers are removed.

Table 5-A. 1677 SONET Link Unit Descriptions (cont.)

UNIT	DESCRIPTION
18RU 48-Port DS3/EC1 Connector Panel PN: 3EM12329AA Qty: Up to 4 per 18RU shelf	18RU 48-port DS3/EC1 connector panels are mounted on either the equipment rack or the rear of the 18RU shelf. 48-port DS3/EC1 connector panels provide 48 DS3 connections and connect to ECC-12Ps through BNC connectors accessible at the rear of the 18RU shelf once connector covers are removed.
18RU 96-Port DS3/EC1 Connector Panel PN: 3EM12330AA Qty: Up to 2 per 18RU shelf	18RU 96-port DS3/EC1 connector panels are mounted on either the equipment rack or the rear of the 18RU shelf. 96-port DS3/EC1 connector panels provide 96 DS3/EC1 connections and connect to ECC-12Ps through BNC connectors accessible at the rear of the 18RU shelf once connector covers are removed.
Power Distribution Unit, Quad Input (PDU-Quad) PN: 3EM14200AB Qty: 1 per single or dual rack	The PDU-Quad distributes A1-, A2-, B1-, and B2-battery power that feeds shelves and fans. It provides redundant, fuse-protected connections to each shelf and fan powered within a bay. It contains front-panel alarm indicators that indicate loss of A1, A2, B1, or B2 power or a tripped breaker or blown fuse.
DS1 Splitter PN: 3EM14189AD/AE Qty: Up to two per rack (one per 18RU shelf)	The DS1 splitter terminates a 1.544 MHz DS1 BITS external clock reference. The DS1 splitter receives one primary and one secondary BITS reference and outputs two primary and two secondary BITS references. One primary and one secondary BITS reference is distributed to each of two TCs the associated 18RU shelf. The AD variant is equipped with shelf 1, and the AE variant is equipped with shelf 2.
ADME 01x East Add/Drop Module (ADM) PN: 3EM12215AA (E band) 3EM12217AA (F band) Qty: 1 per channel band, per East direction	ADMs add and drop light on/off network fiber. They are part of the MOS system and install directly into an ANSI rack. ADM East modules support E and F channel bands.
ADMW 01x West Add/Drop Module (ADM) PN: 3EM12216AA (E band) 3EM12218AA (F band) Qty: 1 per channel band, per West direction	ADMs add and drop light on/off network fiber. They are part of the MOS system and install directly into an ANSI rack. ADM West modules support E and F channel bands.

Table 5-A. 1677 SONET Link Unit Descriptions (cont.)

UNIT	DESCRIPTION
CCC 104 Common Control Card (CCC) PN: 3EM12219AB Qty: 2 per shelf, slots 9 and 10	The CCC is the main processing power in the node, controlling communication between the IOCs, SSCs, and the TC. The CCC records and controls node events, monitoring events, and alarm events. The CCC contains two removable flash disks that hold system image and configuration, statistics, logging, and billing-information files.The CCC supports audible and visual alarms.
DCME 0x0 East Dispersion Compensation Module (DCM) PN: 3EM12222AA (20 km) 3EM12224AA (40 km) 3EM12226AA (60 km) 3EM12228AA (80 km) Qty: Up to 2 in the East direction	East DCMs compensate for chromatic dispersion. They are part of the MOS system and install directly into an ANSI rack.
DCME 0x0 West Dispersion Compensation Module (DCM) PN: 3EM12223AA (20 km) 3EM12225AA (40 km) 3EM12227AA (60 km) 3EM12229AA (80 km) Qty: Up to 2 in the West direction	West DCMs compensate for chromatic dispersion. They are part of the MOS system and install directly into an ANSI rack.
DS0G 101 DS0 Groomer (DS0G) PN: 3EM17343AA Qty: 2 per shelf, slots 3 and 4 or 14 and 15	The DS0G 101 DS0 Groomer (DS0G) provides 2.5 Gb/s capacity of unidirectional DS0-level switching and grooming for VT-mapped traffic. One pair of DS0G 101 DS0 Groomers (DS0Gs) in a 1+1, nonrevertive protection scheme may be provisioned. This supports a system total of 1344 DS1s. To support the optional DS0 Groomer, the 3EM12295AD SSC104 must be equipped.
DWDME 10x East Dense Wavelength Division Multiplexer (DWDM) PN: 3EM12230AA (E band Ch. 35-38) 3EM12232AA (F band Ch. 30-33) Qty: Up to 2 in the East direction	DWDMs multiplex aggregate mixed-rate signals into one optical channel at the OC-48 rate. DWDMs also demultiplex the OC-48 optical channel into aggregate signals. DWDMs install directly into the ANSI rack and support E and F channels bands in East direction. They are part of the MOS system.
DWDMW 10x West Dense Wavelength Division Multiplexer (DWDM) PN: 3EM12231AA (E band Ch. 35-38) 3EM12233AA (F band Ch. 30-33) Qty: Up to 2 in the West direction	DWDMs multiplex aggregate mixed-rate signals into one optical channel at the OC-48 rate. DWDMs also demultiplex the OC-48 optical channel into aggregate signals. DWDMs install directly into the ANSI rack and support E and F channels bands in the West direction. They are part of the MOS system.

Table 5-A. 1677 SONET Link Unit Descriptions (cont.)

UNIT	DESCRIPTION
EDFA 10x Erbium Doped Fiber Amplifier (EDFA) PN: 3EM12297AA (Pre-Amp) 3EM12298AA (Line-Amp) Qty: Up to12 per shelf, two slots wide, slots 1A&2A, 1B&2B, 3A&4A, 3B&4B, 5A&6A, 5B&6B, 12A&13A, 12B&13B, 14A&15A, 14B&15B, 16A&17A, and 16B&17B	The EDFA is an optical amplifier provides a 23 dB signal gain and amplifies as many as 40 ITU C-Band channels simultaneously. The EDFA is available for either line-amplified or a pre-amplified applications. Each EDFA is installed into two adjacent half-high slots.
IFC1 201 12-Port DS3/EC1 Interface Card (ECC-12P) PN: 3EM12348AA Qty: Up to 20 per shelf, slots 1-5 and 12-16, A or B	The ECC-12P provides twelve DS3/EC1 interfaces. Up to 16 working ECC-12Ps (providing up to 192 DS3/EC1 interface connections) are supported in either an unprotected or APS 1 x n protected configuration. Up to four protection ECC-12Ps are supported in the APS 1 x n protected configuration.
IFC2 10x 2-Port Gigabit Ethernet, LX (GIGE-2P) PN: 3EM12310AA/AB Qty: Up to 24 per shelf, slots 1-6 and 12-17, A or B	The GIGE-2P supports two IEEE 802.3-compliant ports operating in serial mode. It supports Generic Framing Protocol (GFP) Encapsulation and Virtual Concatenation of up to 21 STS-1s.
IFC4 10x 2-Port Gigabit Ethernet, SX (GIGE-2P) PN: 3EM12311AA/AB Qty: Up to 24 per shelf, slots 1-6 and 12-17, A or B	The GIGE-2P supports two IEEE 802.3-compliant ports operating in serial mode. It supports Generic Framing Protocol (GFP) Encapsulation and Virtual Concatenation of up to 21 STS-1s.
LC2 10x 12-Port IR OC-3 Line Card (OC3-12P) PN: 3EM12238AA/AB Qty: Up to 24 per shelf, slots 1-6 and 12-17, A and B	The OC3-12P is an input/output (IOC) module that provides 12 OC-3, 1310 nm interfaces. This OC3-12P has an SM, IR laser transmitter and an LC connector type.
LC5 10x 4-Port IR OC-12 Line Card (OC12-4P) PN: 3EM12241AA/AB Qty: Up to 24 per shelf, slots 1-6 and 12-17, A and B	The OC12-4P provides four OC-12, 1310 nm interfaces. This OC12-4P has an SM, IR laser transmitter and an SC connector type.
LC7D 10x 1-Port SR OC-48 Line Card (OC48-1P) PN: 3EM12301AA/AB (DC-SM-SC) Qty: Up to 24 per shelf, slots 1-6 and 12-17, A and B	The OC48-1P provides one OC-48 interface with a 1310 nm interface port. This type of OC48-1P has a Short-Reach (SR) transmission laser and uses Single-Mode (SM) fiber connection with an SC connector type
LC7ID 10x 1-Port IR OC-48 Line Card (OC48-1P) PN: 3EM12302AA/AB (DC-SM-SC) Qty: Up to 24 per shelf, slots 1-6 and 12-17, A and B	The OC48-1P provides one OC-48 interface with a 1310 nm interface port. This type of OC48-1P has an Intermediate-Reach (IR) transmission laser and uses SM fiber connection with an SC connector type
LC8D 10x 1-Port LR OC-48 Line Card (OC48-1P) PN: 3EM12312AA/AB (DC-SM-SC) Qty: Up to 24 per shelf, slots 1-6 and 12-17, A and B	The OC48-1P provides one OC-48 interface with a 1310 nm interface port. This type of OC48-1P has a Long-Reach (LR) transmission laser and uses SM fiber connection with an SC connector type

Table 5-A. 1677 SONET Link Unit Descriptions (cont.)

UNIT	DESCRIPTION
LC10D x3x 1-Port XLR OC-48 Line Card (OC48-1P) PN: 3EM12250AA/AB (DC-SM-SC, 1553.33) 3EM12251AA/AB (DC-SM-SC, 1552.52) 3EM12252AA/AB (DC-SM-SC, 1551.72) 3EM12253AA/AB (DC-SM-SC, 1550.92) 3EM12254AA/AB (DC-SM-SC, 1549.31) 3EM12255AA/AB (DC-SM-SC, 1548.51) 3EM12256AA/AB (DC-SM-SC, 1547.72) 3EM12257AA/AB (DC-SM-SC, 1546.92) Qty: Up to 24 per shelf, slots 1-6 and 12-17, A and B	The OC48-1P provides one OC-48 interface with an interface port for one of the 32 ITU C-Band DWDM channels located on the 100 GHz spacing grid. The OC48-1P supports Drop and Continue (DC) configurations using an SM fiber type, an Extra-Long-Reach (XLR) transmission laser, and an SC connector type.
LC12D x3x 1-Port LR OC-192 Line Card (OC192-1P) PN: 3EM12266AA/AB (DC-SM-SC, 1553.33) 3EM12267AA/AB (DC-SM-SC, 1552.52) 3EM12268AA/AB (DC-SM-SC, 1551.72) 3EM12269AA/AB (DC-SM-SC, 1550.92) 3EM12270AA/AB (DC-SM-SC, 1549.32) 3EM12271AA/AB (DC-SM-SC, 1548.51) 3EM12272AA/AB (DC-SM-SC, 1547.72) 3EM12273AA/AB (DC-SM-SC, 1546.92) Qty: Up to of 4 per shelf, slots 5AB, 6AB,12AB, and 13AB	The OC192-1P provides one OC-192 interface for DC configurations. The OC192-1P has an ITU DWDM channel interface and uses single mode fiber, an LR laser transmitter, and an SC connector type. FEC is also supported on OC192-1Ps.
SSC 104 80 Gb/s STS Switch Card (SSC) PN: 3EM12295AC (128MB of SWC RAM) 3EM12295AD (256MB of SWC RAM) Qty: 2 per shelf, slots 7 and 8	The SSC is comprised of two controllers called the Switch Controller and the DCC Controller. The SSC manages the switch fabric (SWC) controller subsystem of the shelf. The SSC-SWC controls the center-stage 80-Gb/s switch and all IOCs. The SSC-DCC manages the DCC controller subsystem of the shelf. The DCC selects and switches up to 128 DCC channels. (However, the system software limits the system maximum to 66 DCCs—32 line DCCs and 34 section DCCs.) The DCC permits network administration, alarm surveillance, provisioning, and control of a network from its central location. To support the optional DS0 Groomer, the 3EM12295AD SSC104 must be equipped.

Table 5-A. 1677 SONET Link Unit Descriptions (cont.)

UNIT	DESCRIPTION
TC 301 Timing Card (TC) PN: 3EM12309AB Qty: 2 per shelf, slots 11A and 11B	The TC provides the timing reference signal for all modules in the node. The time is derived from the BITS DS1s or from any OC-*n* interface. A Stratum-3 quality holdover is supported when external timing fails. The TC contains an Ethernet port connection for remote management and a RS-232 port connection for local management. Redundancy requires TC in slots 11A and 11B.
TMUX x01 2.5 Gb/s Transmux (TMUX) PN: 3EM12308AA/AB Qty: Up to 4 per shelf, slots 1-6 and 12-17, A and B	The TMUX is capable of performing DS3-structured STS-1 to VT-structured STS-1 translation and DS3 DS1 and VT DS1 path monitoring. The TMUX supports 48 STS-1 port pairs in high-capacity 2.5 Gb/s slots.
VSC 101 5 Gb/s VT1.5 Switch Card (VSC) PN: 3EM12313AB Qty: Up to 4 per shelf, slots 1-6 and 12-17, A and B	The VSC supports VT1.5 grooming and cross-connections, and provides 5 Gb/s switching capacity in high-capacity slots 5A, 5B, 6A, 6B, 12A, 12B, 13A, or 13B when using an 80 Gbps STS switch. Redundancy is also supported.

6. FUNCTIONAL OPERATION

6.1 A fully loaded 1677 SONET Link system with two 15RU or 18RU shelves holds a DS3 port capacity of up to 384 DS3s, 576 OC-3s, 192 OC-12s, 48 OC-48s, or 8 OC-192s. It provides interfaces for DS3s, OC-3s, OC-12s, OC-48s, OC-192s, and Gigabit Ethernet (GIGE) traffic. The system functions using the following subsystem architectures:

- I/O Subsystem—Input Conditioning
- Matrix Switching
- DS0 Grooming/Switching
- I/O Subsystem—Output Conditioning
- Control
- Clock Distribution
- Modular Optical System

6.2 Each subsystem corresponds to hardware elements made up of one or more modules or assemblies. The Input/Output (I/O) and 3-stage Clos switch matrix perform signal processing functions. The remaining subsystems support signal processing and provide control, synchronization and power to the system.

I/O Subsystem—Input Conditioning

6.3 The system processes traffic in both transmit and receive directions simultaneously. In this section, input from the receive direction of signal flow will be discussed. The Output Signal Transmission section describes signal flow in the transmit direction.

6.4 DS3 input conditioning provides the interface for customer DS3s at the rate of 44.736 Mb/s. The signals are processed and output at the rate of 51.840 STS-1 Mb/s is sent to the switch matrix.

6.5 EC1 input conditioning provides the interface for customer EC1s at the rate of 51.840 Mb/s. The signals are processed and output at the rate of 51.840 STS-1 Mb/s is sent to the switch matrix.

6.6 OC-3 input conditioning provides the interface for customer OC-3s at the optical rate of 155.52 Mb/s. The signals are processed, demultiplexed and sent as 51.840 Mb/s STS-1 data output to the switch matrix.

6.7 OC-12 input conditioning provides interface for customer OC-12s at the optical rate of 622.08 Mb/s. The signals are processed, demultiplexed, and sent as 51.840 Mb/s STS-1 data output to the switch matrix.

6.8 OC-48 input conditioning provides interface for customer OC-48s at the optical rate of 2.488 Gb/s. The signals are processed, demultiplexed, and sent as 51.840 STS-1 Mb/s data output to the switch matrix.

6.9 OC-192 input conditioning provides interface for customer OC-192s at the optical rate of 9.953 Gb/s. The signals are processed, demultiplexed, and sent as 51.840 STS-1 Mb/s data output to the switch matrix.

6.10 GIGE input conditioning provides interface for customer GIGE client signals. The signals are processed, demultiplexed and sent as 51.840 Mb/s STS-1 data output to the switch matrix.

6.11 For more information about input conditioning within the individual components, refer to the Unit Data Sheets (UDS) in this manual.

DS3 Input Conditioning

6.12 The DS3 input conditioning subsystem provides the interface between the DS3s and the STS-1 format of the switch matrix. The DS3s are received by the 12-Port DS3/EC1 Interface Module (ECC-12P), terminated, and mapped into STS-1 structures to be sent to the switch matrix.

6.13 The components of the DS3 input subsystem are as follows:

- DS3/EC1 Connector Panel and/or Front Panel Connectors
- ECC-12P

DS3/EC1 Connector Panels and/or Front Panel Connectors

6.14 DS3 signal input is received by DS3/EC1 connector panels mounted on the rear of the 15RU or 18RU shelf. The DS3/EC1 Connector Panel holds BNC connectors for 48 DS3 signals (Tx and Rx) and uses protection relays to interface the DS3 signal to the ECC-12P. A 96-port remote, rack-mounted BNC connector panel is also supported. Either 2 rear-mounts and one rack-mount or two rack-mounts can be installed to achieve the full 192 DS3 ports.

ECC-12P

6.15 The ECC-12P terminates 12 DS3s. The transformers receives the analog signal and sends it to the framer/mapper. A Framer/Mapper receives the NRZ signal and maps it into a STS structure.The Framer/Mapper outputs the STS structure on a 8-bit parallel SONET Interface Bus where the signal is translated into Telecom Bus Signal (TBS) structure. The TBS encodes a SONET STS-12 data frame from the Framer/Mapper to the serial Telecom Bus links. This data is then sent on the Slave Bus to the switch matrix for processing.

6.16 The DS3/EC1 Connector Panel provides the interface between the DS3 signal and the working and protect ECC-12Ps. In the event of an ECC-12P failure, the DS3/EC1 Connector Panel transmits the DS3 signals, along with help from the SSC, to the protection ECC-12P.

EC1 Input Conditioning

6.17 The EC1 input conditioning subsystem provides the interface between the EC1s and the STS-1 format of the switch matrix. The EC1s are received by the 12-Port DS3/EC1 Interface Module (ECC-12P), terminated, and mapped into STS-1 structures to be sent to the switch matrix.

6.18 The components of the EC1 input subsystem are as follows:

- DS3/EC1 Connector Panel and/or Front Panel Connectors
- ECC-12P

DS3/EC1 Connector Panels and/or Front Panel Connectors

6.19 EC1 signal input is received by DS3/EC1 connector panels mounted on the rear of the 15RU or 18RU shelf. The DS3/EC1 Connector Panel holds BNC connectors for 48 EC1 signals (Tx and Rx) and uses protection relays to interface the EC1 signal to the ECC-12P. A 96-port remote, rack-mounted BNC connector panel is also supported. Either 2 rear-mounts and one rack-mount or two rack-mounts can be installed to achieve the full 192 EC1 ports.

ECC-12P

6.20 The ECC-12P terminates 12 EC1s. The transformers receives the analog signal and sends it to the framer/mapper. A Framer/Mapper receives the NRZ signal and maps it into a STS structure.The Framer/Mapper outputs the STS structure on a 8-bit parallel SONET Interface Bus where the signal is

translated into Telecom Bus Signal (TBS) structure. The TBS encodes a SONET STS-12 data frame from the Framer/Mapper to the serial Telecom Bus links. This data is then sent on the Slave Bus to the switch matrix for processing.

6.21 The DS3/EC1 Connector Panel provides the interface between the EC1 signal and the working and protect ECC-12Ps. In the event of an ECC-12P failure, the DS3/EC1 Connector Panel transmits the DS3 signals, along with help from the SSC, to the protection ECC-12P.

OC-3 Input Conditioning

6.22 The input conditioning subsystem provides the interface between the OC-3 and the 51.840 Mb/s modified STS-1 format of the switch matrix. OC-3 input conditioning is performed by the OC3-12P module.

6.23 In the receive direction of signal flow, a Framer receives the 155.52 Mb/s signal pair from the TBS and performs clock and data recovery functions as well as serial to parallel conversion on the SONET frame. The Framer then performs framing, descrambling pointer processing, and terminates SONET section and line frames. Transport overhead is extracted and the Synchronous Payload Envelope (SPE) is placed on the DROP telecom bus. The TBS encodes SONET frame data from the Framer on the incoming parallel telecom bus then sends the data to the SSC for matrix switching.

6.24 Additionally, data can be reassigned by the 48x48 STS Time Slot Interchange (TSI) before being sent to the SSC.

OC-12 Input Conditioning

6.25 The input conditioning subsystem provides the interface between the OC-12 and the 51.840 Mb/s modified STS-1 format of the switch matrix. OC-12 input conditioning is performed by the OC12-4P module.

6.26 In the receive direction of signal flow, a SERializer/DESerializer (SERDES) device receives the serial 622.08 Mb/s signal pair and converts it to 4x8-bit data bus, which is sent to the Framer. The Framer receives the SONET STS-12 frame data and performs framing, descrambling pointer processing, and termination of SONET section and line frames. Transport overhead is extracted and the Synchronous Payload Envelope (SPE) is placed on the DROP telecom bus. The TBS encodes SONET frame data from the Framer on the incoming parallel telecom bus then sends the data to the SSC for matrix switching.

OC-48 Input Conditioning

6.27 The input conditioning subsystem provides the interface between the OC-48 and the 51.840 Mb/s modified STS-1 format of the switch matrix. OC-48 input condition is performed by the OC48-1P module.

6.28 In the receive direction of signal flow, a deserializer device receives the serial 2.488 Mb/s signal pair and converts it to 16-bit data bus, which is sent to the Framer. The Framer receives the SONET STS-48 frame data and performs framing, descrambling pointer processing, and termination of SONET section and line frames. Transport overhead is extracted and the Synchronous Payload Envelope (SPE) is placed on the DROP telecom bus. The TBS encodes SONET frame data from the Framer on the incoming parallel telecom bus then sends the data to the SSC for matrix switching.

6.29 Additionally, the data can be reassigned by the 48x48 STS TSI before being sent the SSC for processing.

OC-192 Input Conditioning

6.30 The input conditioning subsystem provides the interface between the OC-192 and the 51.840 Mb/s modified STS-1 format of the switch matrix. OC-192 input conditioning is performed by the OC192-1P module.

6.31 In the receive direction of signal flow, the OC192-1P receives the signal through an embedded Transceiver module. The Transceiver performs optical and SERial/DESerialized (SERDES) functions. In the SERDES function, the deserializer performs clock recovery and the integrated PLL recovers the clock signal from the incoming data. The Transceiver on the module interfaces the signal to the Forward Error Correction (FEC)/Digital Wrapper device where performance monitoring occurs before the signal is sent to Framer. The Framer accepts STS-192 data and terminates the section and line overhead and performs pointer processing for alignment. The signal is then reframed into a serial STS-12 data stream where it is processed sent to the TSI to allow the STS input signal to be groomed to any STS output time slot within the frame for processing by the switch fabric (SSC).

Gigabit Ethernet Input Conditioning

6.32 Gigabit Ethernet (GIGE) input conditioning is performed by the GIGE module and is used to map Ethernet frames into SONET payload structures. SONET payload uses Virtual Concatenation (VC) to provide channels with up to 21 STS-1s.

6.33 On the receive side of signal flow, the GIGE inputs two gigabit Ethernet channels through the SERDES interface, maps the Ethernet frames into SONET signals and transmits the signals through a serial telecom bus. Basic frame integrity and validation of incoming signal frames is done by the Enhanced Gigabit Media Access Control (EGMAC). The EGMAC outputs the Ethernet frames to the buffering logic. The buffering logic instructs the EGMAC to halt receive data with a PAUSE frame when provisionable thresholds are crossed. When the entire frame has been buffered, it is sent to the Ethernet over SONET encapsulation (GFP) block.

6.34 The SONET encapsulation block performs data steam encapsulation of each Ethernet channel into GFP frames. When no frames are available in the buffering logic, IDLE frames are inserted into the channel, completing frame encapsulation. The virtual concatenation processor then splits the Gigabit Ethernet stream into multiple physical channels and fills in the appropriate Multi-frame and Sequence Indicators. The outgoing signal is sent to the Telecom bus.

Matrix Switching

6.35 The 1677 SONET Link supports two switch matrixes to accommodate STS-1 and VT data structures:

- STS-1 Switch Fabric
- VT1.5 Switch Fabric

6.36 The following descriptions of the STS-1 and VT1.5 switch fabrics give a high-level overview of the switch modules (IOCs, SSCs, VT1.5) and operation. For a more detailed description of module function and interface bus architectures, refer to the Unit Data Sheets (UDS) of this manual.

STS-1 Switch

6.37 The 1677 SONET Link provides an 80 Gb/s STS-1 switch fabric supporting a capacity of up to 1536x1536 STS-1s. The STS-1 switch is performed using the SSC module and two (one transmit and one receive) Input/Output modules (IOCs). The SSC is responsible for STS-1 channel switching and DCC Overhead processing. IOCs serve as the first and third stages with the SSC performing the second stage function.

6.38 A complete three-stage switch involves putting the appropriate number of Time Slot Interchanges (TSIs) together and interconnecting them to the IOC TSI switches on both transmit and receive sides. Each of the first stage outputs and each of the third stage inputs connects to every switch in the second stage. A fully interconnected second stage contains 256 connections on each side of the second stage; half of the protection side connections transmit and receive signals from the second SSC. See figure 6-1.

First Stage

6.39 The first stage of the STS-1 switch is performed on the receive IOC. For each half-height and full-height slot, a set of M (0 through 7 and 0-15 respectively) working (first half) and protection (second half) channels cross the high-speed backplane into the SSC. Up to 64 STS-12s for both low- and high-capacity slots send a total capacity of up to 128 STS-12 channels over the backplane to the SSC.

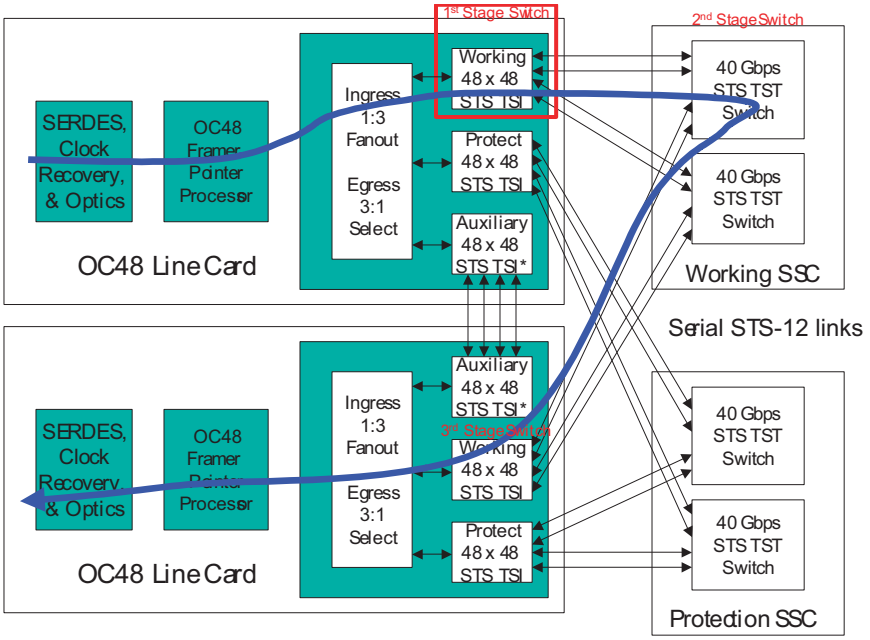
Second Stage

6.40 The SSC module performs the second (middle) stage switching operation. In the second stage, rearrangement in time (across time slots) and space (across physical channels) is performed by memory maps. For each time slot in each output channel, the address of the input channel and time slot from which data is taken is programmed by the SSC Control Processing Unit (CPU). As a result, after the SSC completes rearrangement of the STS-12 signal, connectivity between endpoints may change for some or all time periods. In this case, time slots arrive at different outputs from that which they came. Any receive STS-12 channel and any of it constituents (STS-1s) can be reassigned to any transmit STS-12 channel and any of its constituents.

Third Stage

6.41 The third stage of the STS-1 Switching Matrix is performed by the transmit IOC. The IOC receives STS-12 paths and conditions them for transmission on the optical fiber.

Figure 6-1. Clos Switch Architecture



DCC Processing

6.42 All IOCs use DCC channels for HDLC processing through the SSC. The DCC function is responsible for processing Section and Line Overhead in and out of the IOC using SONET DCC channels and is referred to as the DCC Processor. The DCC Processor passes HDLC channels to and from the Line Card Framer devices.

VT1.5 Switch

6.43 A half-height, high-capacity IOC slot has eight 622 Mb/s bidirectional serial links to the primary 80 Gb/s STS switch fabric. Each STS-12 supplies 12 STS-1 signals with each STS-1 supplying 28 VT1.5 signals. Therefore, the maximum number of VT1.5 signals per half-height, high-capacity IOC slot is 2,688.

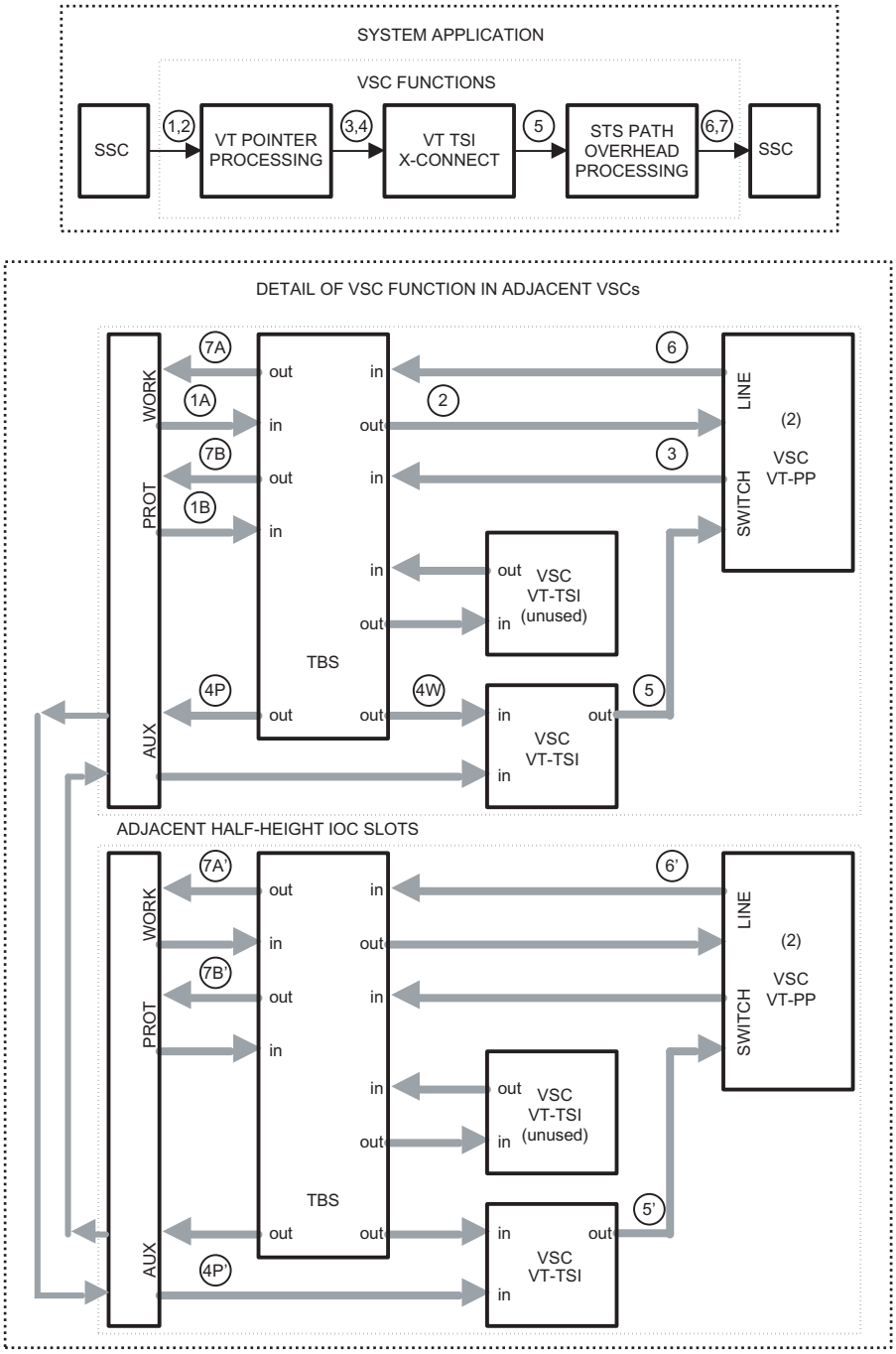
6.44 VT1.5 switching is accomplished using two hardware devices embedded on VT1.5 Switch Card (VSC); the Time Slot Interchange (TSI) and the Pointer Process and Column Aligner. The VT switching core is linked to the STS switching fabric by a Telecom Bus Serializer (TBS) interface located on the VSC. Each of two VSCs manages 2.5 G of VT1.5 pointer processing, path termination, and column alignment. A single VSC cross connects all 2,688 VT1.5 payloads that can be transmitted to the TBS.

6.45 The VSC has a total capacity of 5 Gb/s or 2688 VT1.5 payloads when installed in a high-capacity slot. When placed into a low-capacity slot, the total capacity is reduced to 2.5 Gb/s.

Single-Stage VT Switch

6.46 The Single-Stage switch consists of a Pointer Processor (PP) and a Time Slot Interchange (TSI) device. Typically, two VSC modules are used, each representing a single-stage switch and are connected through the Auxiliary port to provide a UPSR protection paths. See figure 6-2.

Figure 6-2. One-Stage Single Module VT Switch



NOTE: CIRCLED NUMBERS IN SYSTEM APPLICATION PORTION CORRESPOND TO CIRCLED NUMBERS IN DETAIL OF VSC FUNCTION.

677-0123-1
030805

6.47 In the single-stage VT switch, working and protection input signals enter the TBS for decoding from both the working and protection SSCs. Active input signals then enter the line receive port of the VT-PP. Here, pointer processing, column alignment and signal quality (B3) processing occurs. The signals exit the VT-PP and re-enter the TBS where there are two parallel output paths. Working signals then exit the TBS and enter the first VT-TSI on the same module. Simultaneously, protect signals exit the TBS and are sent through the backplane Auxiliary bus to the protection VT-TSI on the adjacent module. Signals exit the VT-TSI and enter the switch receive port of the VT-PP. Here, signal quality and performance monitoring processing occurs. Finally, signals exit the VT-PP and re-enter the TBS for encoding. Working and protection signals are output to the working and protect SSCs.

DS0 Grooming/Switching Subsystem

6.48 The DS0 grooming/switching subsystem consists of one 15RU or 18RU shelf that houses a pair of DS0G 101 DS0 Groomer (DS0G) modules. These modules provide 2.5 Gb/s of DS0 grooming and switching capability.

6.49 All facilities with embedded DS0s destined for the DS0 Groomer must be routed through the VSC. Some of these facilities may require additional conversion through the TMUX prior to going through the VSC (depending on the STSMAP parameter). All connections between VSC, TMUX, and DS0G pass through the SSC. To support the optional DS0 Groomer, the 3EM12295AD SSC104 must be equipped.

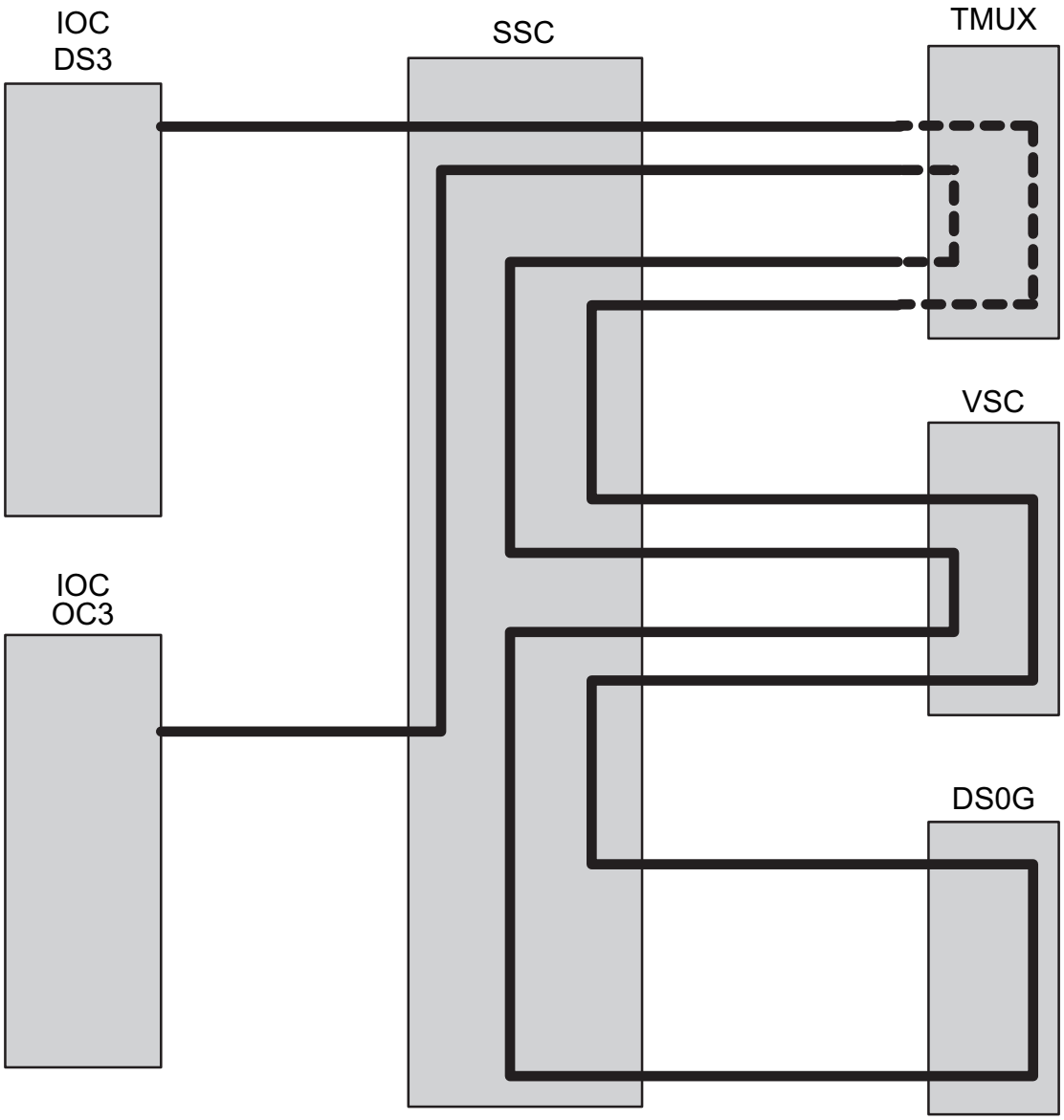
6.50 A DS1 embedded within a VT1 can be created and provisioned only if it is defined to be DS0 groomed using the DS0G parameter of the ENT-T1 TL1 command. When the DS0G parameter is provisioned, the system automatically assigns a DS1 residing on the DS0G module.

6.51 The components of the DS0 grooming/switching subsystem follow:

- VSC 101 5 Gb/s VT1.5 Switch Card (VSC)
- TMUX 201/301 2.5 Gb/s Transmux (TMUX) (optional)
- SSC 104 STS Switch Card (SSC)
- DS0G 101 DS0 Groomer (DS0G)

6.52 For more specific information about DS0 grooming/switching within the individual components, refer to the Unit Data Sheets (UDSs) in this manual and see figure 6-3 for signal flow through a DS0G-equipped shelf. Some facilities may not require conversion through the TMUX (depending on the STSMAP parameter.)

Figure 6-3. Signal Flow Through DS0G-Equipped Shelf



Input Function

6.53 The input function performs the following:

- Receives 2.5 Gb/s data from the VSC
- Provides protection switching
- Performs DS0 grooming and switching

VSC 101 5 Gb/s VT1.5 Switch Card (VSC)

6.54 The VSC supports VT1.5 grooming and cross-connections, and provides 5 Gb/s switching capacity in high-capacity slots 5A, 5B, 6A, 6B, 12A, 12B, 13A, or 13B when using an 80 Gbps STS switch. Redundancy is also supported. For more information, refer to UDS-128, VSC 101 5 Gb/s VT1.5 Switch Card.

SSC 104 STS Switch Card (SSC)

6.55 The SSC provides a static 80 Gb/s STS-1 switch fabric supporting a capacity of up to 1536×1536 STS-1s. The SSC performs STS-1 channel switching. STS-1 switching provides the facility and equipment protection switching that is localized to each I/O HDS.

6.56 The Time-Space-Time (TST) switches on the SSC perform static STS-1 switching. Rearrangement in time (across time slots) and space (across physical channels) is performed by memory maps. The rearrangement scheme is fixed so that a given input to the SSC is always directed to the same output from the SSC.

6.57 Switch fabrics on the SSCs select traffic from the copy 0 or copy 1 matrix on an STS-1 by STS-1 basis. The SSC then sends the data to the DS0Gs.

DS0G 101 DS0 Groomer (DS0G)

6.58 The DS0G 101 DS0 Groomer (DS0G) provides 2.5 Gb/s capacity of unidirectional DS0-level switching and grooming for VT-mapped traffic. The DS0G terminates the VT1.5 and the embedded DS1 in order to switch the DS0s. The DS0s are switched and new DS1/VT1.5 signals are generated. The data is then sent back to the SSCs.

6.59 The Telecom Bus Serializer (TBS) on the DS0G provides backplane interface for the DS0G. It receives four STS-12 signals from each SSC. The TBS selects the active SSC signals and converts the 777 Mb/s telecom bus format signal to 622 Mb/s STS-12 signals for the four hypermappers. Each hypermapper processes 12 STS-1s worth of traffic. The hypermappers terminates the VT1.5s and DS1s in the VT payload to access the DS0s. Each of the two switching FPGAs receives one STS-12 worth of DS0 signals from each of two hypermappers. The switching FPGA performs DS0 switching, then sends the data back to the hypermappers. The hypermappers multiplex the lines from the switching FPGAs to generate the STS-12s going back to the TBS. The TBS then processes and sends four STS-12 signals back to the SSCs.

1+1 Protection Switching for DS0Gs

6.60 DS0Gs are 1+1 protected. In the event of detected failure on the working DS0G, the active SSC directs traffic to and from the protect DS0G.

Output Function

6.61 The output function is a mirror image of the input function and provides receive path protection switching.

SSC 104 STS Switch Card (SSC)

6.62 Switch fabrics on the SSC select working traffic from the working DS0G.

Output Conditioning

6.63 The system processes traffic in both transmit and receive directions simultaneously. In this section, output conditioning for the transmit direction of signal flow will be discussed. The Input Conditioning section describes signal flow in the receive direction.

6.64 DS3 output conditioning receives 51.840 Mb/s modified STS-1 data from the switch matrix. The signals are processed back into their original DS3 rates (44.736 Mb/s) and conditioned for output on the new port.

6.65 EC1 output conditioning receives 51.840 Mb/s modified STS-1 data from the switch matrix. The signals are processed back into their original EC1 rates (51.840 Mb/s) and conditioned for output on the new port.

6.66 OC-3 output conditioning receives 51.840 Mb/s modified STS-1 data from the switch matrix. The signals are processed back into their original OC-3 rates (155.52 Mb/s) and conditioned for output on the new port.

6.67 OC-12 output conditioning receives 51.840 Mb/s modified STS-1 data from the switching matrix. The signals are processed back into their original OC-12 rates (622.08 Mb/s) and conditioned for output on the new port.

6.68 OC-48 output conditioning receives 51.840 Mb/s modified STS-1 data from the switching matrix. The signals are processed back into their original OC-48 rates (2.488 Gb/s) and conditioned for output on the new port.

6.69 OC-192 output conditioning receives 51.840 Mb/s modified STS-1 data from the switching matrix. The signals are processed back into their original OC-192 rates (9.953 Gb/s) and conditioned for output on the new port.

6.70 GIGE output conditioning receives 51.840 Mb/s modified STS-1 data from the switch matrix. The signal is processed back into the original GIGE format and conditioned for output on the new port.

DS3 Output Conditioning

6.71 The output subsystem provides the interface between the 51.840 Mb/s modified STS-1 format of the switch matrix and the DS3 interface. The ECC-12P performs DS3 output conditioning.

6.72 Output conditioning performed by the ECC-12P begins with the decoding of the SONET frame data from the SSC. This data interfaces onto the serial telecom bus links to the outgoing parallel telecom bus. The Frammer/Mapper receives the data from the telecom bus on its 8-bit parallel SONET interface bus. The interface bus aligns the data, removes the SONET overhead, outputs the data and clock, smooths the data/clock, and outputs the Non-Return to Zero (NRZ) interface at 44.736 Mhz to the Line Interface Unit (LIU). The LIU encodes the NRZ input, provides pulse shaping, and transmits the filtered waveform to the DS3/EC1 Connector Panel.

EC1 Output Conditioning

6.73 The output subsystem provides the interface between the 51.840 Mb/s modified STS-1 format of the switch matrix and the EC1 interface. The ECC-12P performs EC1 output conditioning.

6.74 Output conditioning performed by the ECC-12P begins with the decoding of the SONET frame data from the SSC. This data interfaces onto the serial telecom bus links to the outgoing parallel telecom bus. The Frammer/Mapper receives the data from the telecom bus on its 8-bit parallel SONET interface bus. The interface bus aligns the data, removes the SONET overhead, outputs the data and clock, smooths the data/clock, and outputs the Non-Return to Zero (NRZ) interface at 51.840 Mhz to the Line Interface Unit (LIU). The LIU encodes the NRZ input, provides pulse shaping, and transmits the filtered waveform to the DS3/EC1 Connector Panel.

OC-3 Output Conditioning

6.75 The output subsystem provides the interface between the 51.840 Mb/s modified STS-1 format of the switch matrix and OC-3. The 12 Port OC-3 module (OC3-12P) performs the output conditioning functions.

6.76 In the transmit direction, the TBS decodes SONET frame data from the SSC, or adjacent OC3-12P, on the 777.60 Mb/s telecom bus to the 32-bit outgoing parallel telecom bus. Also, reassignment of STS-1s by the Time Slot Interchanger (TSI) is supported. From the telecom bus, the Framer receives the signal on its ADD telecom bus, aligns the data, adds SONET overhead, then outputs the data through a serial interface to optical devices for transmission in the system.

OC-12 Output Conditioning

6.77 The output subsystem provides the interface between the 51.840 Mb/s modified STS-1 format of the switch matrix and OC-12. The 4 Port OC-12 module (OC12-4P) performs the output conditioning functions.

6.78 In the transmit direction of signal flow, the TBS decodes SONET frame data from the SSC, or adjacent IOC, on the 777.6 telecom bus and places the data on a 32-bit outgoing parallel Telecom Bus. Reassignment of STS-1s through a Tim Slot Interchange (TSI) is also supported. The outgoing telecom bus interfaces to the Framer. The Framer receives the data on its ADD telecom bus, aligns it, adds SONET overhead, and outputs through a 4x8-bit interface to the SERDES device. The SERDES converts the 4x8 bit data into a 622.08 Mb/s differential pair to be transmitted throughout the system.

OC-48 Output Conditioning

6.79 The output subsystem provides the interface between the 51.840 Mb/s modified STS-1 format of the switch matrix and OC-48. The 1 Port OC-48 module (OC48-1P) performs the output conditioning functions.

6.80 In the transmit direction of signal flow, the TBS decodes SONET frame data from the SSC, or adjacent IOC, on the 777.6 telecom bus and places the data on a 32-bit outgoing parallel Telecom Bus. Reassignment of STS-1s through a Time Slot Interchange (TSI) is also supported. The outgoing telecom bus interfaces to the Framer, which receives the data on its ADD telecom bus, aligns it, adds SONET overhead, and outputs it through a 16-bit interface to a Serializer device. The Serializer converts the 16-bit data into a 2.488 Gb/s differential pair to be transmitted throughout the system.

OC-192 Output Conditioning

6.81 The output subsystem provides the interface between the 51.840 Mb/s modified STS-1 format of the switch matrix and OC-192. The 1 Port OC-192 module (OC192-1P) performs the output conditioning functions.

6.82 In the transmit direction of signal flow, the TSI switch accepts data from the switch fabric. The data is processed and delivered to the Framer. In the Framer, SONET STS-192 frame with overhead is created and encoded by the Forward Error Correction (FEC) Digital Wrapper. The FEC sends the STS frame to the Transceiver.

Gigabit Ethernet Output Conditioning

6.83 On the transmit side of signal flow, the GIGE receives the signal from the SONET interface and outputs it on the Ethernet interface. The GIGE performs AU3/AU4 pointer processing to account for positive and negative pointer justifications on the incoming data streams.

6.84 The GIGE then reassembles received constituent channels of each of two Virtual Concatenation (VC) channels by processing the appropriate Multi-frame and Sequence Numbers. The number of physical channels used in the transmit/receive directions must be the same, but the GIGE supports arbitrary time-slot assignment to the physical channels. Each of the two VC channels can be configured independently without disruption to the operation of the other.

6.85 The transmit virtual concatenation processor outputs the two GIGE channels to the GFP processor. The GFP Decapsulation Processor processes the two channels with encapsulation being removed to recover two channels of native Ethernet frames. The native frames are output to the buffer logic of 28.8 kbytes. The EGMAC blocks provide 1 Gb/s and connectors to the SERDES interface or to the external Gigabit PHY of each Gigabit Ethernet port. The GEMAC incorporates functions such as Auto-Negotiation, statistics, and flow control.

Control

6.86 The control subsystem performs the high-level processing that supports the interactive administration, maintenance, and control function of the 1677 SONET Link system. Control is distributed between the following three physical levels in conjunction with software system and user interfaces:

- Common Control Card (CCC)
- STS-1 Switch Card (SSC)
- Timing Card (TC)

6.87 Communication buses provide the information paths between the three modules.

6.88 For more information about the control subsystem within each module, refer to the Unit Data Sheets (UDS) in the manual.

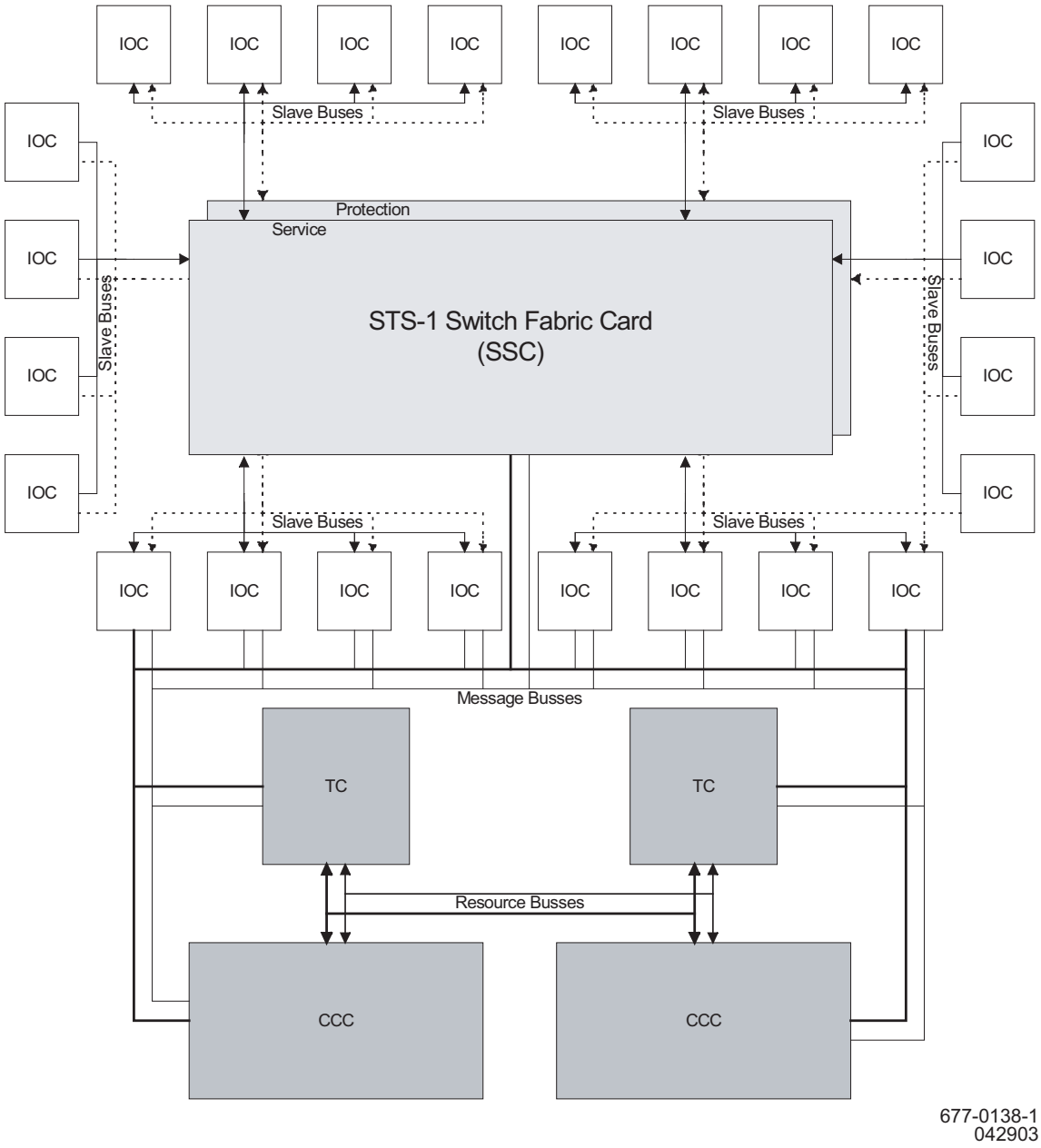
Communication Busses

6.89 Communication between the three modules of the control subsystem is done through the following key buses:

- Message Bus
- Slave Bus
- Resource Bus
- Health Signals
- Configuration Signals
- DCC Signal

6.90 See figure for an illustration of the key control subsystem buses.

Figure 6-4. Communication Buses



Message Bus

6.91 The message bus communicates messages from the CCC to the SSC. The CCC uses information in the descriptor to form a header. The data pointed to by the BP field in the descriptor becomes the payload. Together the header and payload form a message frame that is sent over the message bus.

Slave Bus

6.92 The slave bus is the communication link between the SSC and the IOC modules. Read/write frame formats are transmitted to the IOCs. Each IOC receives two busses, one from the primary SSC and the other from the secondary SSC. Each IOC also initiates primary bus and a secondary bus.

Resource Bus

6.93 The system resource bus is the communication link between the CCC and TC. The resource bus detects broken hardware and insertion/removal events.

6.94 The CCC converts writes into a resource bus message containing address/operation type, data, and Clock Recovery Counts (CRC). The CCC or TC checks the message CRC. If message is correct, a write operation occurs. If message fails, it is dropped and a CRC error message is returned to the CCC.

6.95 During read operations, the CCC converts operations into a resource bus message containing address/operation type and CRC. The CCC and TC check the message CRC. If the message is correct, an ISA bus read operation occurs followed by a status and read data message sent back to the CC. If the message fails, it is dropped and a CRC error message is returned to the CCC.

Health Signals

6.96 The 1677 SONET Link offers two kinds of health monitoring signals for the control subsystem modules: Global and Local. Global health monitoring applies to modules with control processors. Local health monitoring applies to the monitoring of modules without control processors, but are monitored by modules with control processors.

6.97 In global health monitoring, there are three major signal groupings:

- 14 presence bits: SSCs, CCCs and intelligent IOCs detect board insertion/removal events by monitoring these bits.
- 28 14-pair health status bits: Each SSC, CCC and intelligent IOC source two health status bits. SSCs and CCCs monitor all 14 pair. Two bits from each module are encoded to provide a level of health.
- Four CCC primary bits: Each CCC sources two primary bits. The CCCs, SSCs, and all IOCs monitor primary bits.

6.98 CCC local health monitoring includes the following:

- Peer activity strobe (CCC only): CCCs use a peer activity strobe to monitor each other's health. Each CCC asserts the strobe at a software-controlled interval. If a CCC does not detect a strobe from the other CCC within the interval time, it can assume the software has hung, and the other board may be reset.
- CCC front panel switch: The front panel switch indicates the module is about to be pulled and all access to the disk subsystem must stop.
- TC front panel switch: The switch detection allows the system to switch over the stratum timing source and message bus arbiter before a module removal event occurs.
- TC present signal

6.99 In local SSC health monitoring, IOCs monitor the two primary bits driven by the SSCs. These bits determine which SSC is the slave bus master and which is the reset source. SSCs also monitor 24 IOC presence bits.

6.100 In intelligent IOC local health monitoring, adjacent IOC pairs monitor each other's health status.

Configuration Signals

6.101 Configuration signals are also classified as global and local. Global applies to system wide resources controlled by the CCC. Local applies to non-system wide resources under control of a CCC or SSC. Many of the configuration signals may enable interrupt sources to control processors. Signals from the established primary CCC or SSC determine module configuration.

DCC Signals

6.102 DCC signals are used to interconnect SSCs and IOCs. DCC termination is performed on the SSC. The primary goal is to support both DCC channels from up to 16 OC-3 ports on a single IOC.

6.103 The interface between each IOC and the SSC consist of the following signals:

- TX line (SSC to SSC)
- RX line (IOC to SSC)
- CLK (SSC to IOC)
- SYNC (SSC to IOC)

Clock Distribution

6.104 System clock distribution is performed by the CCCs. Clocks are point-to-point pair transmissions distributed at a 50 Mhz frequency. All system modules receive two copies of the 50 Mhz clock, one copy from each CCC. Additionally, all non-physical modules receive a SYNC signal distributed through both the working and protection signal copies from the CCCs. The SYNC provides a common reference for the SSC to IOC slave bus and a 25 Mhz phase signal used by the message bus. An interface between the two CCCs allows the SYNC signals to be in phase with each other. The primary CCC determines which CCC SYNC signal is selected by the system modules.

6.105 Inside the CCC is a 50 Mhz oscillator, a system processor, and two clock fan-out buffers. The system processor is necessary for redundancy purposes. It initiates one of the fan-out buffers, which in turn, initiates two clock drivers. This action supplies up to 30 50 Mhz clock loads to the system.

6.106 On each system module, a processor feeds signals to TTL clocks. The CCCs send multiplexer selects to all of the other modules. The selects ensure glitches from CCC insertion, removal, or fail-over do not result in selection of the alternate clock source. The multiplexer select is synchronized with the negative clock edge. Therefore, glitches do not occur when the clock source is changed. The primary CCC controls multiplexer selections.

6.107 System modules contain two clock reset devices. These devices generate clock resets through pushbutton, watchdog and power monitoring functions. One device monitors power and the other monitors the TTL clock. If one device detects a missing clock, it generates an alarm that over-rides the CCC's multiplexer selection and forces use of the other clock.

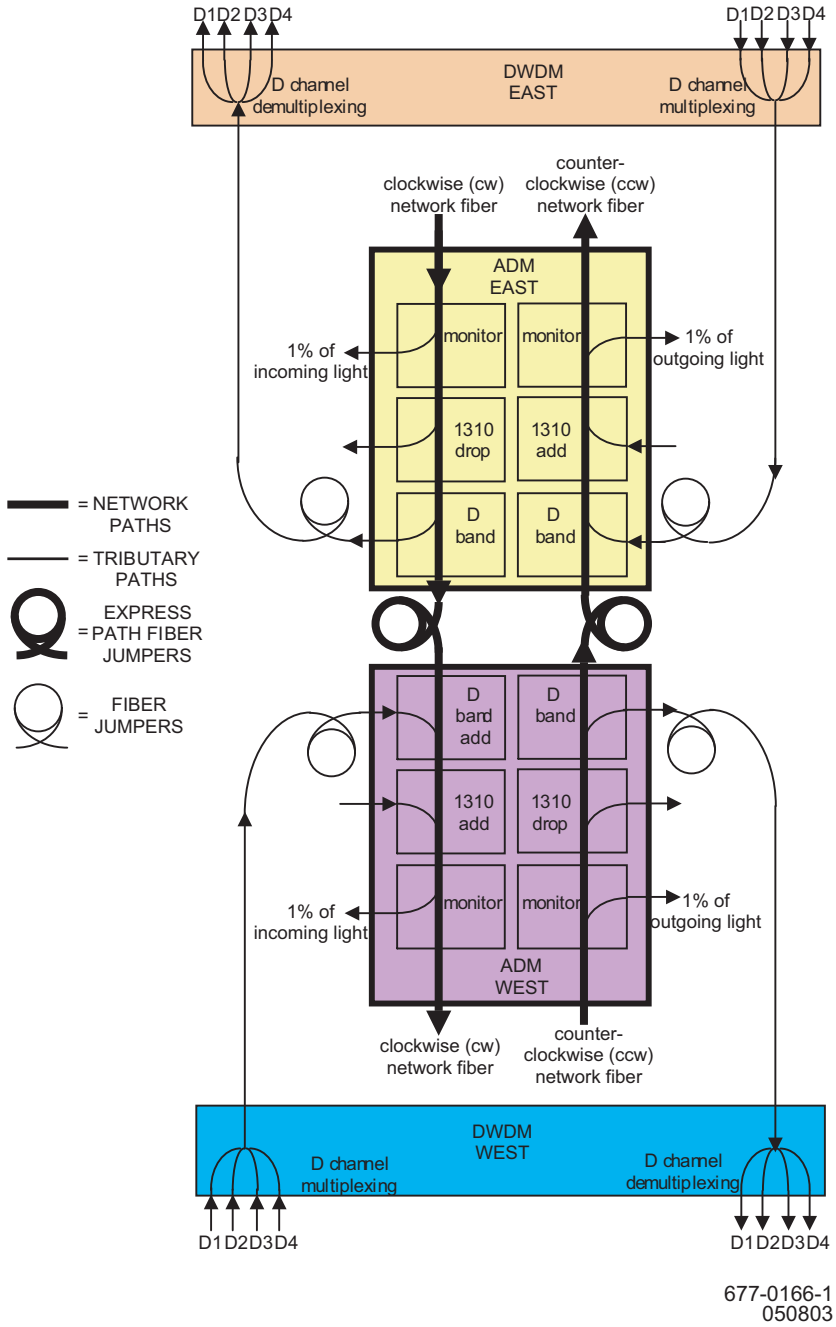
Modular Optical System

6.108 A typical DWDM ring has two, bidirectional fiber paths. MOS modules add/drop 1310 nm legacy traffic and 4 band channels on/off the two fiber paths. Monitors at the beginning and end of each light path tap off a small percentage of light to aid in setup and trouble shooting functions.

6.109 ADM and DWDM add and drop light off of the main network or tributary fibers respectively. The distinction between network light paths and tributary light paths is that any interruption in network light paths may affect other nodes in the network and will require a protection event. Therefore, components are separated into the appropriate modules (ADM or DWDM) so that system upgrades performed when only tributary paths are affected may be done without interruption to network traffic.

6.110 Figure describes the signal flow of the MOS system.

Figure 6-5. MOS Signal Flow



7. POWER DISTRIBUTION

Power and Ground Requirements

7.1 The system requires -48 V dc primary office power. Central Office (CO) battery A and battery B power connections are made at terminal blocks in the power panel at the front of the 15RU shelf or rear of the 18RU shelf. Battery A and battery B power is fused into separate -48 V dc buses. The return for each feeder is also independent. These feeders supply different power supplies whose outputs are load sharing. For a complete description of CO battery connections, refer to the 1677 SONET Link Installation Practices manual (PN 3EM13849AF).

Rack Power Requirements

7.2 For a complete description of the connections required for office power, refer to the 1677 SONET Link Installation Practices manual (PN 3EM13849AF). The power requirement for the 1677 SONET Link ANSI rack is as follows: Each ANSI rack requires battery A and battery B power feed to the PDU.

System Grounding

7.3 The positive primary power return is isolated from the CO ground by more than 100 kilohms, as measured per Telecordia TA-EOP-000295. The minimum isolation voltage is 600 V dc. For more information on system grounding, refer to the 1677 SONET Link Installation Practices manual (PN 3EM13849AF).

Primary Power Interface

7.4 Refer to table 7-A for the primary power interface specification.

Table 7-A. Power Interface Specifications

ITEM	CHARACTERISTICS
1. Location Power Panel	 A power in (APWR) B power in (BPWR) Separate power return (GND)
Front of 15RU shelf or rear of 18RU shelf	Central Office (CO) ground
2. Function	Separates office primary power and ground from rack
3. Input voltage -48 V (nominal) systems	 -40V to -60 V
4. Isolation	Positive primary power return is isolated from CO ground by more than 100 kilohms as measured per Telcordia TA-EOP-000295.
5. Input power	Power consumption varies with system size, fill, and options provided.
6. Power consumption	Maximum power consumption of a fully equipped 15RU or 18RU shelf at -48 V dc: 960 W

Power Distribution

7.5 The -48 volt input is distributed from the power panel to the backplane then to each module. Each module locally converts the -48 volts to the voltages needed to power module circuits. Local on-module overcurrent protection, power filtering, and power conditioning components protect each module to ensure reliable system performance. If the node has redundant power sources and one fails, diode protection prevents the active -48 volt source from backfeeding the inactive -48 volt source.

8. SYSTEM ENGINEERING SPECIFICATIONS

8.1 This section provides basic information and specifications relating to signal interface, alarm interface, and control interface. Information about connection points, connector types, and pin assignments is also provided. Refer to table 8-A for environmental specifications. Refer to table 8-B for engineering specifications.

Signal Interfaces

8.2 System signal interfaces comply with customer interface specifications. Supported signal interfaces include DS3, EC1 (STS-1), OC-3, OC-12, OC-48, OC-192, GIGE, intershelf optics, and cable connectors.

Signal Cable Connections

8.3 DS3/EC1 connector panels provide network connections through separate 48-port DS3/EC1 connector panels (up to 192 DS3/EC1 ports) mounted on either the equipment rack or the rear of the 15RU or 18RU shelf. Connections from the panels to the ECC modules are made through connectors at the rear of the 15RU or 18RU shelf.

DS3 Interface

8.4 Refer to table 8-C for DS3 interface specifications. See figure 8-1 for the DS3 mask template. The template specifies the signal waveshape boundaries. DS3 waveshape at the 1677 SONET Link connectors must fit within the template bounds. See figures 8-2, 8-3, and 8-4 for DS3 jitter characteristics.

STS-1 Interface

8.5 Refer to table 8-D for the STS-1 interface specifications. See figure 8-5 for the combined DS3/STS-1 format template. The template specifies the waveshape boundaries. STS-1 waveshape at the DSX must fit within the template bounds. See figures 8-6 and 8-7 for STS-1 jitter characteristics.

OC-3 Interface

8.6 Refer to table 8-E for OC-3 interface specifications. See figure 8-8 for the OC-3 mask template. The template specifies the signal waveshape boundaries. OC-3 waveshape at the 1677 SONET Link connectors must fit within the template bounds.

OC-12 Interface

8.7 Refer to table 8-F for OC-12 interface specifications. See figure 8-8 for the OC-12 mask template. The template specifies the signal waveshape boundaries. OC-12 waveshape at the 1677 SONET Link connectors must fit within the template bounds.

OC-48 Interface

8.8 Refer to table 8-G for OC-48 interface specifications. See figure 8-9 for the OC-48 mask template. The template specifies the signal waveshape boundaries. OC-48 waveshape at the 1677 SONET Link connectors must fit within the template bounds.

OC-192

8.9 Refer to table 8-H for OC-192 interface specifications. See figure 8-9 for the OC-192 mask template. The template specifies the signal waveshape boundaries. OC-192 waveshape at the 1677 SONET Link connectors must fit within the template bounds.

Table 8-A. Environmental Condition Specifications

ITEM	Operating	Non-Operating
1. Ambient temperature	5°C to 40°C (41° F to 104° F)	-40°C to 70°C (-40° F to 158° F)
2. Relative humidity	5% to 90% (without condensation)	5% to 90% (without condensation)
3. Altitude	0 to 3,048 m (0 to 10,000 ft.)	0 to 3,048 m (0 to 10,000 ft.)
4. Cooling	Forced air flow	
5. Vibration and shock	Earthquake requirements	
6. Duty cycle	Continuous, unattended	

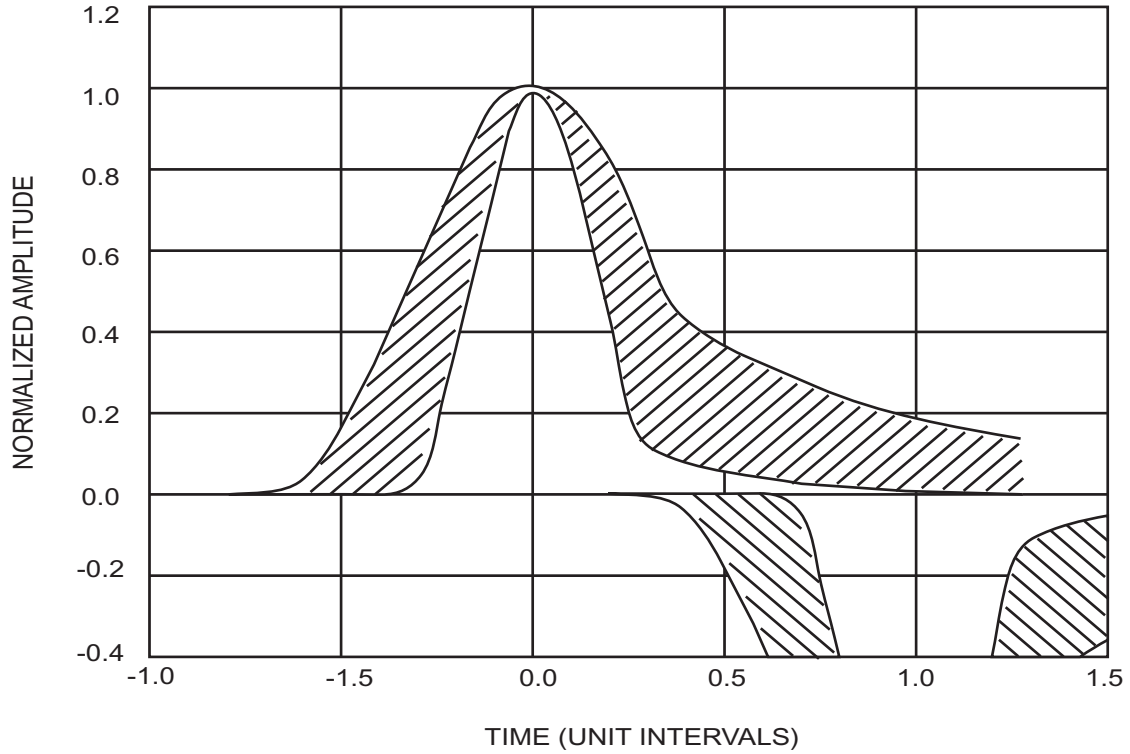
Table 8-B. 1677 SONET Link Engineering Data

SHELF (Fully Loaded)	WEIGHT	CURRENT DRAIN AND POWER CONSUMPTION @ -48V (AMPS)	VOLTAGE RANGE (VOLTS)
15RU shelf	Dependant on configuration	20 A, 960 W	-40 to -60 V dc
18RU shelf	Dependant on configuration	20 A, 960 W	-40 to -60 V dc

Table 8-C. DS3 Interface Specifications

ITEM	CHARACTERISTICS
1. Location	Input/Output Card slots 1-6A/B and 12-17A/B of the 15RU or 18RU shelf
2. Function	Maps DS3s for transport to STS switch matrix
3. Capacity Two 15RU or 18RU shelves	Up to 384 DS3s (192 DS3 ports per 18RU shelf) per fully loaded system
4. Frequency	44.736 MB/s ±20 ppm
5. Line code	AMI (bipolar) with B3ZS coding
6. Format	Asynchronous framed DS3 per T1X1/87-127. See figure 8-1.
7. Line Impedance	75 ohms ±5%
8. Pulse Amplitude	0.36 V to 0.85 V for an isolated pulse
9. Pulse Shape Output	See figure 8-1.
10. Power Level	A wideband power measurement of an AIS signal using a power level sensor with a working frequency range of 200 MHz is -4.7 dBm to +3.6 dBm, including the effects of a range of connecting cable lengths between 225 ft. and 450 ft. A low-pass filter having a flat passband and a frequency cutoff of 200 MHz is used.
11. Pulse Imbalance	Ratio of amplitudes of positive and negative isolated pulses is between 0.90 and 1.10. See figure 8-1.
12. Cable Type	75 ohm BNC coaxial cables
13. Jitter Tolerance Transfer	All measurements are made on a half-duplex cross connection. See figure 8-2. See figure 8-3.

Figure 8-1. Asynchronous DS3 Mask



INVERTED PULSE SHOWN TO AID OSCILLOSCOPE TIME-BASE ADJUSTMENT

CURVE	TIME UNIT INTERVALS	NORMALIZED AMPLITUDE
MAXIMUM CURVE	$-0.85 \le T \le -0.68$	0.03
	$-0.68 \le T \le 0.36$	$0.5\left\{1 + \sin\left[\left(\frac{\pi}{2}\right)\left(1 + \frac{T}{0.34}\right)\right]\right\} + 0.03$
	$0.36 \le T \le 1.4$	$0.08 + 0.407\, e^{-1.84\,(T - 0.36)}$
MINIMUM CURVE	$-0.85 \le T \le -0.36$	-0.03
	$-0.36 \le T \le 0.36$	$0.5\left\{1 + \sin\left[\left(\frac{\pi}{2}\right)\left(1 + \frac{T}{0.18}\right)\right]\right\} - 0.03$
	$0.36 \le T \le 1.4$	-0.03

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Figure 8-2. DS3 Input Jitter Accommodation

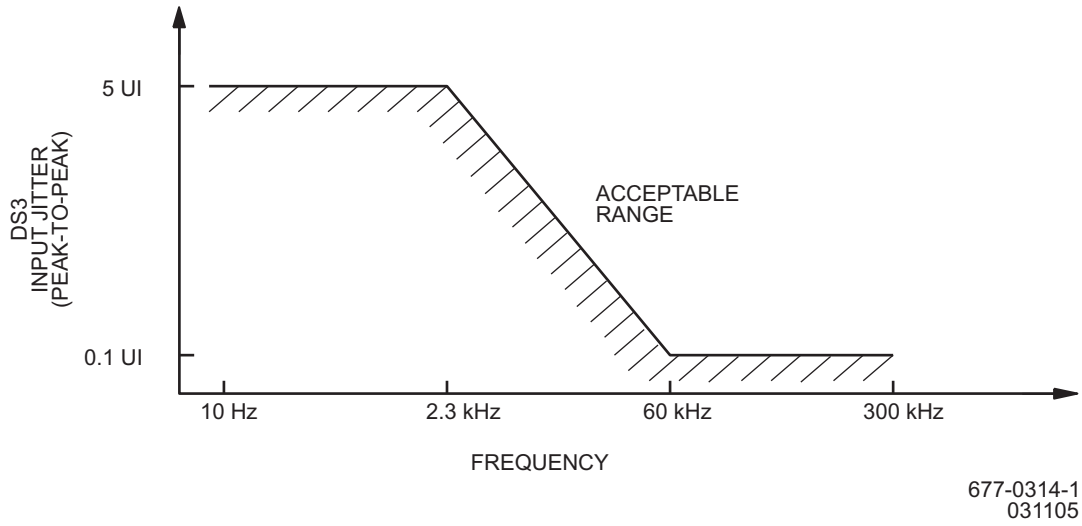


Figure 8-3. DS3 Jitter Transfer Characteristics

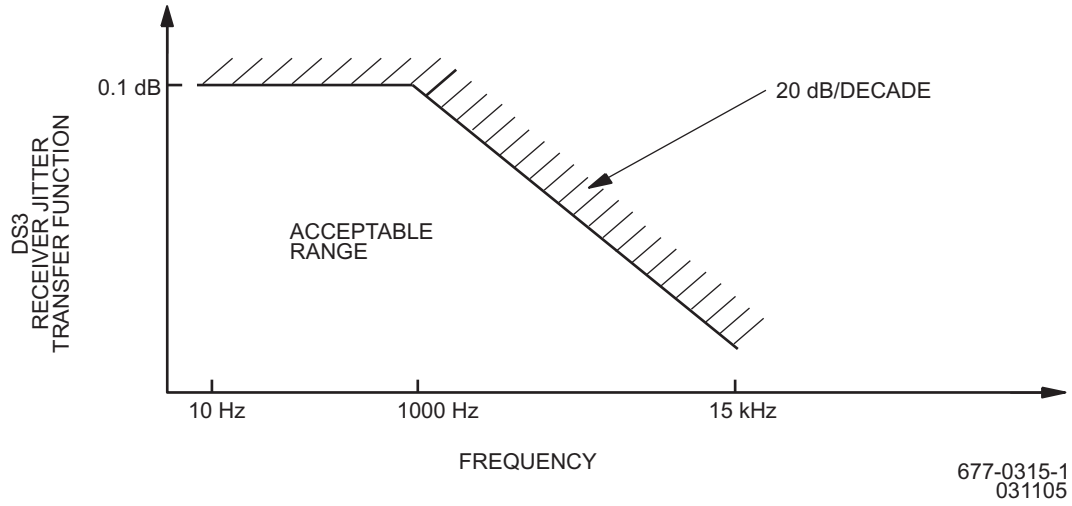


Figure 8-4. DS3 Jitter Measurement Characteristics

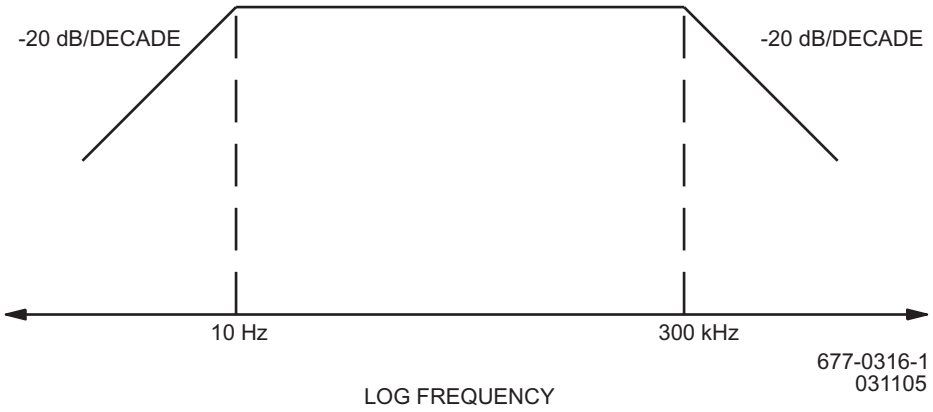
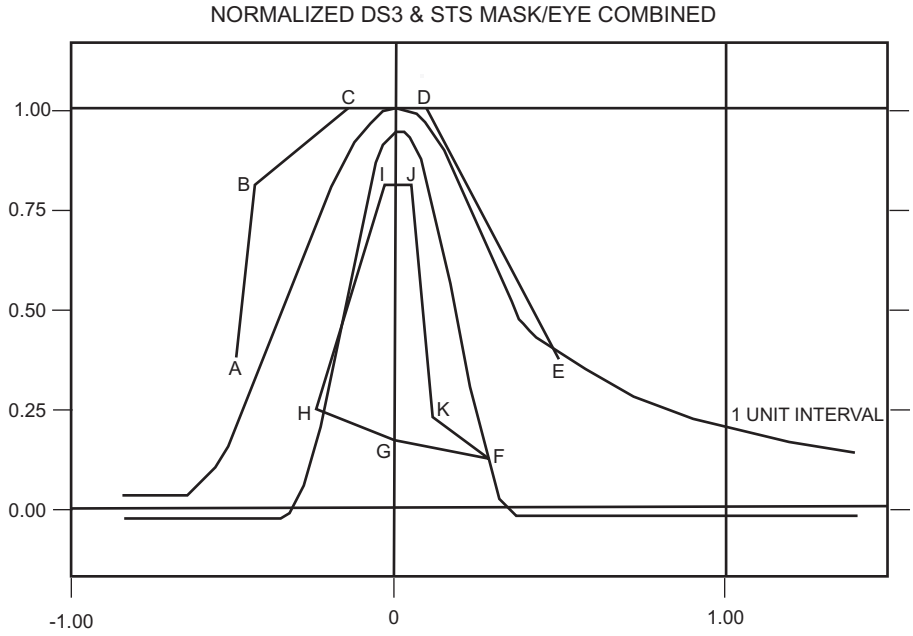


Table 8-D. STS-1 Interface Specifications

ITEM	CHARACTERISTICS
1. Location	ECC-12P
2. Function	Couples STS-1s into and out of shelf
3. Capacity	1 to 192 full-duplex STS-1 ports per shelf
4. Frequency	51.84 Mb/s ±20 ppm
5. Line code	B3ZS coding
6. Format	Synchronous (per ANSI). See figure 8-5.
7. Line impedance	75 ohms + 5%, unbalanced
8. Input return loss	More than 20 dB at 22 MHz
9. Level	Measured with all 1's signal and 3 kHz bandwidth centered @ 22 MHz plus 450 ft of 728A coaxial or equivalent
Input signal	-1.8 to +5.7 dBm
Input amplitude	35 to 534 mV p-p balanced
Output signal	-3.3 to +4.3 dBm
Output amplitude	293 to 841 mV p-p balanced
10. Pulse shape	See figure 8-5.
Output	Compliant with ANSI T1 standards
11. Cable type	75 ohm BNC coaxial cables
12. Jitter	All measurements are made on a half-duplex cross-connection.
Tolerance	See figure 8-6.
Transfer	See figure 8-7.

Figure 8-5. Combined STS-1 and DS3 Format Template



DS3 MASK

UPPER CURVE	AMPLITUDE
$-0.85 \le T \le -0.68$	0.03
$-0.68 \le T \le 0.36$	$0.5\left\{1 + \sin\left[\left(\frac{\pi}{2}\right)\left(1 + \frac{T}{0.34}\right)\right]\right\} + 0.03$
$0.36 \le T \le 1.4$	$0.08 + 0.407\, e^{-1.84\,(T - 0.36)}$
LOWER CURVE	
$-0.85 \le T \le -0.36$	-0.03
$-0.36 \le T \le 0.36$	$0.5\left\{1 + \sin\left[\left(\frac{\pi}{2}\right)\left(1 + \frac{T}{0.18}\right)\right]\right\} - 0.03$
$0.36 \le T \le 1.4$	-0.03

STS EYE DIAGRAM

OUTER REGION CORNER POINTS	TIME	AMPLITUDE	INNER REGION CORNER POINTS	TIME	AMPLITUDE
A	-0.50	0.37	F	0.28	0.12
B	-0.44	0.80	G	0.00	0.16
C	-0.15	1.00	H	-0.25	0.24
D	0.08	1.00	I	-0.04	0.80
E	0.50	0.37	J	0.04	0.80
			K	0.11	0.22

STS-1 MASK

UPPER CURVE	AMPLITUDE
$-0.85 \le T \le -0.68$	0.03
$-0.68 \le T \le 0.26$	$0.5\left\{1 + \sin\left[\left(\frac{\pi}{2}\right)\left(1 + \frac{T}{0.34}\right)\right]\right\} + 0.03$
$0.26 \le T \le 1.4$	$0.1 + 0.61\, e^{-2.4\,(T - 0.26)}$
LOWER CURVE	
$-0.85 \le T \le -0.36$	-0.03
$-0.36 \le T \le 0.36$	$0.5\left\{1 + \sin\left[\left(\frac{\pi}{2}\right)\left(1 + \frac{T}{0.18}\right)\right]\right\} - 0.03$
$0.36 \le T \le 1.4$	-0.03

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Figure 8-6. STS-1 Jitter Tolerance

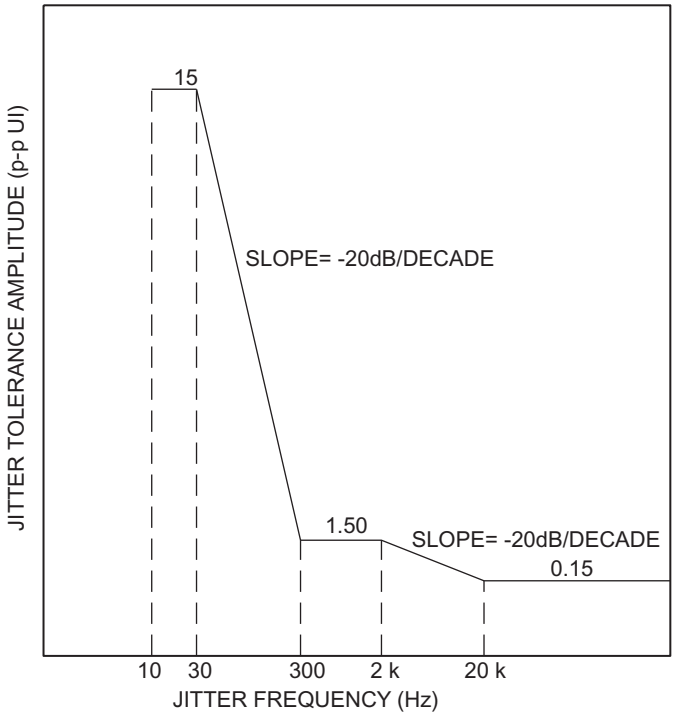


Figure 8-7. STS-1 Jitter Transfer

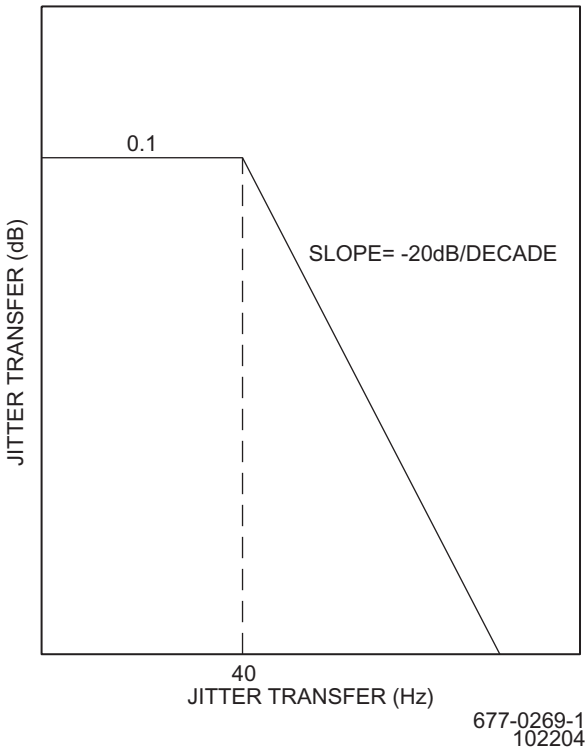
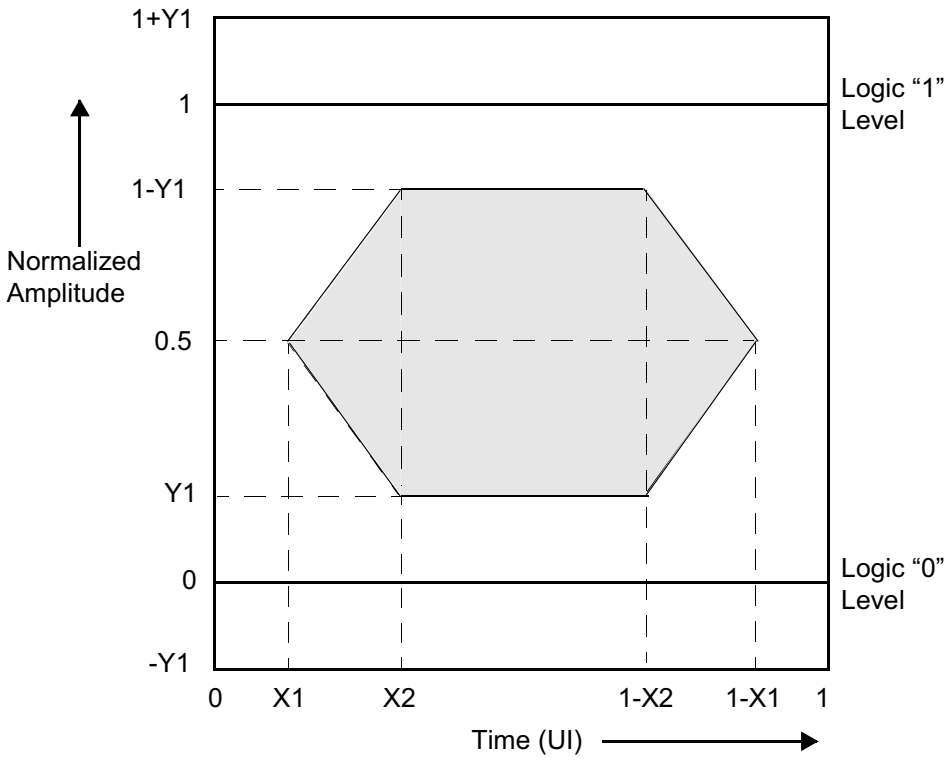


Table 8-E. OC-3 Interface Specifications

ITEM	CHARACTERISTICS
1. Location	Input/Output Card slots 1-6A/B and 12-17A/B of the 1677 SONET Link shelf
2. Function	Maps OC-3s (equivalent to 3 STS-1s) for transport to STS switch matrix
3. Capacity	Up to 864 OC-3s (288 OC-3 ports per shelf) per fully loaded system
4. Frequency	155.52 Mb/s
5. Line code	Nonreturn-to-zero (NRZ)
6. Format	Telecordia GR-253-CORE requirement
7. Pulse Shape Output	See figure 8-8.
8. Input Cable Output Cable	Single mode Single mode with 1.5 in. bending radius
9. Mating connector type	LC

Figure 8-8. SONET Eye Diagram Mask (OC-3 to OC-12)



RATES	X1	X2	Y1
OC-1 AND OC-3	0.15	0.35	0.20
OC-12	0.25	0.40	0.20

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Table 8-F. OC-12 Interface Specifications

ITEM	CHARACTERISTICS
1. Location	Input/Output Card slots 1-6A/B and 12-17A/B of the 1677 SONET Link shelf
2. Function	Maps OC-12s (equivalent to 12 STS-1s) for transport to STS switch matrix
3. Capacity	Up to 288 OC-12s (96 OC-12 ports per shelf) per fully loaded system
4. Frequency	622.08 Mb/s
5. Line code	Nonreturn-to-zero (NRZ)
6. Format	Telecordia GR-253-CORE requirement
7. Pulse Shape Output	See figure 8-8.
8. Input Cable Output Cable	Single mode 5D single mode with 3.0 in. bending radius
9. Mating connector type	SC[1]

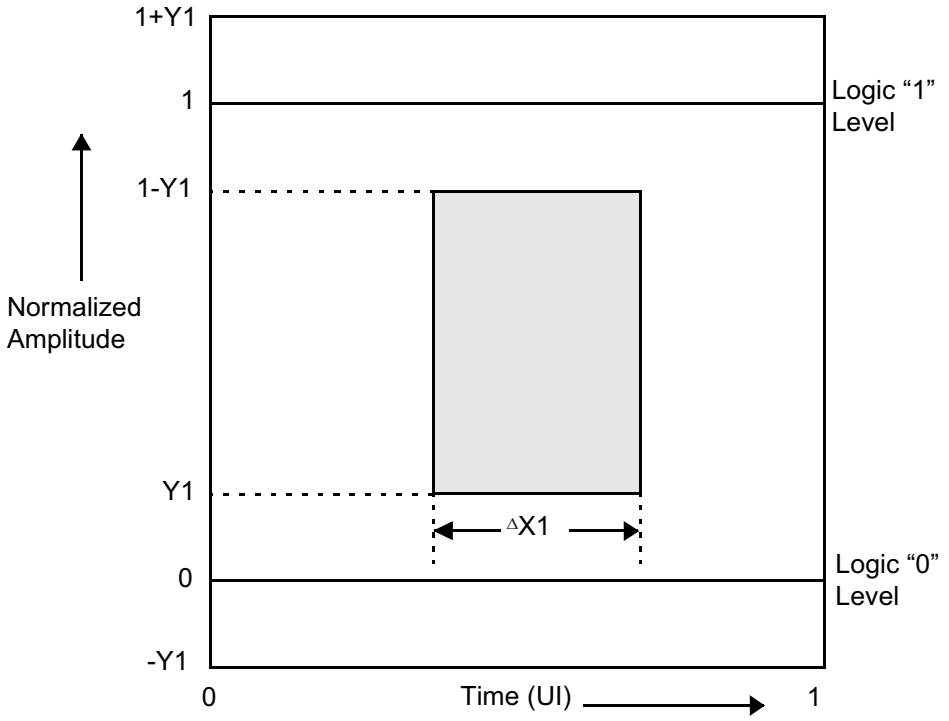
[1] The system uses an SC/UPC pigtailed laser and an SC/UPC pigtailed receiver. UPC is a type of domed polish that reduces back reflections to -55 dB. SC/UPC cables must be used with all SC-type connectors in the system. SC connectors cannot be Angle-Polished Connectors (APCs). If APC-type cable is inserted into the SC connectors, damage to the connector ferrule may result, and high insertion loss and back reflections could result.

Table 8-G. OC-48 Interface Specifications

ITEM	CHARACTERISTICS
1. Location	Input/Output Card slots 1-6A/B and 12-17A/B of the 1677 SONET Link shelf
2. Function	Maps OC-48 (equivalent to 48 STS-1s) for transport to STS switch matrix
3. Capacity	Up to 72 OC-48s (24 OC-48 ports per shelf) per fully loaded system
4. Frequency	2.488 Gb/s
5. Line code	Nonreturn-to-zero (NRZ)
6. Format	Telecordia GR-253-CORE requirement
7. Pulse Shape Output	See figure 8-9.
8. Input Cable Output Cable	Single mode 5D single mode with 3.0 in. bending radius
9. Mating connector type	SC[1]

[1] The system uses an SC/UPC pigtailed laser and an SC/UPC pigtailed receiver. UPC is a type of domed polish that reduces back reflections to -55 dB. SC/UPC cables must be used with all SC-type connectors in the system. SC connectors cannot be Angle-Polished Connectors (APCs). If APC-type cable is inserted into the SC connectors, damage to the connector ferrule may result, and high insertion loss and back reflections could result.

Figure 8-9. SONET Eye Diagram Mask (OC-48 and OC-192)



Rates	ΔX1	Y1
OC-48	0.20	0.25
OC-192 unamplified	0.20	0.25
OC-192 (a and c)[a]	FFS	FFS
OC-192 (b)[a]	0.20	Δ[b]+0.25

a. a, b and c refer to the dispersion accommodation technique used.

b. With X variable -.25<X<+.25

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Table 8-H. OC-192 Interface Specifications

ITEM	CHARACTERISTICS
1. Location	Input/Output Card slots 5AB,6AB, 12AB, and 13AB of the 1677 SONET Link shelf
2. Function	Maps OC-192 (equivalent to 192 STS-1s) for transport to STS switch matrix
3. Capacity	Up to 12 OC-192s (4 OC-192 ports per shelf) per fully loaded system
4. Frequency	9.95 Gb/s
5. Line code	Nonreturn-to-zero (NRZ)
6. Pulse Shape Output	See figure 8-9.
7. Input Cable Output Cable	Single mode 5D single mode with 3.0 in. bending radius
8. Mating connector type	SC[1]

[1] The system uses an SC/UPC pigtailed laser and an SC/UPC pigtailed receiver. UPC is a type of domed polish that reduces back reflections to -55 dB. SC/UPC cables must be used with all SC-type connectors in the system. SC connectors cannot be Angle-Polished Connectors (APCs). If APC-type cable is inserted into the SC connectors, damage to the connector ferrule may result, and high insertion loss and back reflections could result.

Optical Transmission and Receiver Levels

8.10 Refer to table 8-I for the optical transmission and receiver levels for the 1-Port OC-48 Line Card, 1-Port OC-192 Line Card, 4-Port OC-12 Line Card, and the 12-Port OC-3 Line Card.

Table 8-I. Optical Specifications

MODULE	TRANSMITTER REACH	TRANSMITTER OUTPUT POWER (dBm)		RECEIVER SENSITIVITY (dBm)	
		MINIMUM	MAXIMUM	MINIMUM	MAXIMUM
OC3-12P	MM IR LR	-20 -15 -5	-14 -8 0	-30 -28 -34	-14 -8 -10
OC12-4P	SR IR LR	-15 -15 -3	-8 -8 +2	-23 -28 -28	-8 -8 -8
OC48-1P	SR IR LR XLR	-10 -5 -2 -2	-3 0 +3 +3	-18 -18 -27 -27	-3 0 -9 -9
OC192-1P	LR (with FEC)	-0.2	+0.2	-25	-9

Table 8-J. Control Interface Specifications

ITEM	CHARACTERISIC
1. Message Bus	Communication link between CCC and SSC
2. Slave Bus	Communication link between SSC and IOC
3. Resource Bus	Communication link between CCC and TC
4. Health Signals	Control subsystem modules
5. Configuration Signals	Signals from primary CCC or SSC and determine module configuration.
6. DCC Signals	Interconnect SSCs to IOCs

Table 8-K. V3.1 Flash Disk Specifications

ITEM	CHARACTERISTICS	
PN 3EM12332AB		
1. Location	CCC front panel, Drives A and B	
2. Capacity	128 MB	
3. Power Consumption	3.3 V, 5.0 V	
4. Data Transfer Rate (to/from Host)	16.0 Mb/s	
	OPERATING	**NON-OPERATING**
5. Operating Temperature (Commercial) Operating Temperature (Extended)	0°C to 60°C -40°C to 85°C	-25°C to 85°C -50°C to 100°C
6. Relative Humidity	8% to 95% (without condensation)	8% to 95% (without condensation)
7. Altitude	80,000 feet (maximum)	80,000 feet (maximum)
8. Vibration	15 G peak to peak (maximum)	15 G peak to peak (maximum)
9. Shock	1,000 G (maximum)	1,000 G (maximum)

UDS-100
1677 SONET Link Unit Data Sheet Cross-Reference

Unit Data Sheet Cross-Reference by UDS Number

UDS NUMBER	DESCRIPTION	CLEI	STATUS	PART NUMBER
UDS-100	Unit Data Sheet Reference			
UDS-101	Rack	NA	Active	1AD014120032
UDS-102	15RU Shelf	WMM6DC0ARB	Active	3EM12277AA
UDS-103	18RU Shelf	WMM6FC0ARA	Active	3EM12334AC
UDS-104	Power Distribution Unit, Quad Input (PDU-Quad)	NA	Active	3EM14200AB
UDS-105	15RU 48-Port DS3/EC1 Connector Panel	WMM6BB0BRC	Active	3EM12220AA
UDS-106	15RU 96-Port DS3/EC1 Connector Panel	N/A	Active	3EM12221AA
UDS-107	18RU 48-Port DS3/EC1 Connector Panel	N/A	Active	3EM12329AA
UDS-108	18RU 96-Port DS3/EC1 Connector Panel	N/A	Active	3EM12330AA
UDS-109	15RU Fan Tray	WMPQAGSPAC	Active	3EM12279AA
UDS-110	18RU Fan Tray	NA	Active	3EM12307AA
UDS-111	DS1 Splitter, Shelf 1	NA	Active	3EM14189AD
	DS1 Splitter, Shelf 2	NA	Active	3EM14189AE
UDS-112	ADME 013 E-Band East Add/Drop Module (ADM)	WMM9W02JRB	Active	3EM12215AA
	ADMW 013 E-Band West Add/Drop Module (ADM)	WMM9W03JRB	Active	3EM12216AA
	ADME 014 F-Band East Add/Drop Module (ADM)	WMM9W04JRB	Active	3EM12217AA
	ADMW 014 F-Band West Add/Drop Module (ADM)	WMM9W05JRB	Active	3EM12218AA
UDS-113	CCC 101 Common Control Card (CCC)	WM3C20LJAE	Inactive	3EM12219AA
	CCC 104 Common Control Card (CCC)	WMUCAJDBAA	Active	3EM12219AB

UDS NUMBER	DESCRIPTION	CLEI	STATUS	PART NUMBER
UDS-114	DCME 020 20 km East Dispersion Compensation Module (DCM)	WMM9W01JRB	Active	3EM12222AA
	DCMW 020 20 km West Dispersion Compensation Module (DCM)	WMM9W0ZJRB	Active	3EM12223AA
	DCME 040 40 km East Dispersion Compensation Module (DCM)	WMM9WZ0JRB	Active	3EM12224AA
	DCMW 040 40 kM West Dispersion Compensation Module (DCM)	WMM9W10JRB	Active	3EM12225AA
	DCME 060 60 km East Dispersion Compensation Module (DCM)	WMM9W0XJRB	Active	3EM12226AA
	DCMW 060 60 km West Dispersion Compensation Module (DCM)	WMM9W0YJRB	Active	3EM12227AA
	DCME 080 80 km East Dispersion Compensation Module (DCM)	WMM9W20JRB	Active	3EM12228AA
	DCMW 080 80 km West Dispersion Compensation Module (DCM)	WMM9W30JRB	Active	3EM12229AA
UDS-115	DS0G 101 DS0 Groomer (DS0G)	SOUIARPAAA	Active	3EM17343AA
UDS-116	DWDME 101 E-Band E-Dense Wavelength Division Multiplexer (DWDM)	WMM9WX0JRB	Active	3EM12230AA
	DWDMW 101 E-Band W-Dense Wavelength Division Multiplexer (DWDM)	WMM9WY0JRB	Active	3EM12231AA
	DWDME 102 F-Band E-Dense Wavelength Division Multiplexer (DWDM)	WMM9W0WJRB	Active	3EM12232AA
	DWDMW 102 F-Band W-Dense Wavelength Division Multiplexer (DWDM)	WMM9W0VJRB	Active	3EM12233AA
UDS-117	EDFA 103 Erbium Doped Fiber Amplifier, Pre-Amplifier (EDFA)	WMANEF0DAA	Active	3EM12297AA
	EDFA 104 Erbium Doped Fiber Amplifier, Line-Amplifier (EDFA)	WMANFF0DAA	Active	3EM12298AA
UDS-118	IFC1 101 12-Port DS3 Interface Card (DS3-12P)	WMI9GDXLAA	Inactive	3EM12236AA
UDS-119	IFC1 201 12-Port DS3/EC1 Interface Card (ECC-12P)	WMI2CZ0CAA	Active	3EM12348AA

UDS NUMBER	DESCRIPTION	CLEI	STATUS	PART NUMBER
UDS-120	IFC2 101 2-Port Gigabit Ethernet, LX (GIGE-2P)	WM6IV0SAAA	Active	3EM12310AA
	IFC2 102 2-Port Gigabit Ethernet, LX (GIGE-2P)	TBD	Active	3EM12310AB
	IFC4 101 2-Port Gigabit Ethernet, SX (GIGE-2P)	WM6IV0TAAA	Active	3EM12311AA
	IFC4 102 2-Port Gigabit Ethernet, SX (GIGE-2P)	TBD	Active	3EM12311AB
UDS-121	LC2 101 12-Port IR OC-3 Line Card (OC3-12P)	WMOTAXNEAA	Active	3EM12238AA
	LC2 102 12-Port IR OC-3 Line Card (OC3-12P)	WMOTBBBEAA	Active	3EM12238AB
UDS-122	LC5 101 4-Port IR OC-12 Line Card (OC12-4P)	WMOTAXSEAA	Active	3EM12241AA
	LC5 102 4-Port IR OC-12 Line Card (OC12-4P)	WMOTBBEEAA	Active	3EM12241AB

UDS NUMBER	DESCRIPTION	CLEI	STATUS	PART NUMBER
UDS-123	LC10D 030 1-Port XLR OC-48 Line Card, DC-SM-SC, 1553.33 nm (OC48-1P)	WMOTAXXEAA	Active	3EM12250AA
	LC10D 130 1-Port XLR OC-48 Line Card, DC-SM-SC, 1553.33 nm (OC48-1P)	WMOTBBKEAA	Active	3EM12250AB
	LC10D 031 1-Port XLR OC-48 Line Card, DC-SM-SC, 1552.52 nm (OC48-1P)	WMOTAXYEAA	Active	3EM12251AA
	LC10D 131 1-Port XLR OC-48 Line Card, DC-SM-SC, 1552.52 nm (OC48-1P)	WMOTBBLEAA	Active	3EM12251AB
	LC10D 032 1-Port XLR OC-48 Line Card, DC-SM-SC, 1551.72 nm (OC48-1P)	WMOTAXZEAA	Active	3EM12252AA
	LC10D 132 1-Port XLR OC-48 Line Card, DC-SM-SC, 1551.72 nm (OC48-1P)	WMOTBBMEAA	Active	3EM12252AB
	LC10D 033 1-Port XLR OC-48 Line Card, DC-SM-SC, 1550.92 nm (OC48-1P)	WMOTAU4EAA	Active	3EM12253AA
	LC10D 133 1-Port XLR OC-48 Line Card, DC-SM-SC, 1550.92 nm (OC48-1P)	WMOTBBNEAA	Active	3EM12253AB
	LC10D 035 1-Port XLR OC-48 Line Card, DC-SM-SC, 1549.31 nm (OC48-1P)	WMOTAX0EAA	Active	3EM12254AA
	LC10D 135 1-Port XLR OC-48 Line Card, DC-SM-SC, 1549.31 nm (OC48-1P)	WMOTBBPEAA	Active	3EM12254AB
	LC10D 036 1-Port XLR OC-48 Line Card, DC-SM-SC, 1548.51 nm (OC48-1P)	WMOTAX1EAA	Active	3EM12255AA
	LC10D 136 1-Port XLR OC-48 Line Card, DC-SM-SC, 1548.51 nm (OC48-1P)	WMOTBBREAA	Active	3EM12255AB
	LC10D 037 1-Port XLR OC-48 Line Card, DC-SM-SC, 1547.72 nm (OC48-1P)	WMOTAX2EAA	Active	3EM12256AA

UDS NUMBER	DESCRIPTION	CLEI	STATUS	PART NUMBER
	LC10D 137 1-Port XLR OC-48 Line Card, DC-SM-SC, 1547.72 nm (OC48-1P)	WMOTBBSEAA	Active	3EM12256AB
	LC10D 038 1-Port XLR OC-48 Line Card, DC-SM-SC, 1546.92 nm (OC48-1P)	WM31808KAA	Active	3EM12257AA
	LC10D 138 1-Port XLR OC-48 Line Card, DC-SM-SC, 1546.92 nm (OC48-1P)	WMOTBBTEAA	Active	3EM12257AB
	LC7D 101 1-Port SR OC-48 Line Card, DC-SM-SC (OC48-1P)	WMOTAXUEAA	Active	3EM12301AA
	LC7D 102 1-Port SR OC-48 Line Card, DC-SM-SC (OC48-1P)	WMOTBBGEAA	Active	3EM12301AB
	LC7ID 101 1-Port IR OC-48 Line Card, DC-SM-SC (OC48-1P)	WMOTAXVEAA	Active	3EM12302AA
	LC7ID 102 1-Port IR OC-48 Line Card, DC-SM-SC (OC48-1P)	WMOTBBHEAA	Active	3EM12302AB
	LC8D 101 1-Port LR OC-48 Line Card, DC-SM-SC (OC48-1P)	WMOTAXWEAA	Active	3EM12312AA
	LC8D 102 1-Port LR OC-48 Line Card, DC-SM-SC (OC48-1P)	WMOTBBJEAA	Active	3EM12312AB
UDS-124	LC12D 030 1-Port LR OC-192 Line Card, DC-SM-SC, 1553.33 nm (OC192-1P)	WMOTAX3EAA	Active	3EM12266AA
	LC12D 031 1-Port LR OC-192 Line Card, DC-SM-SC, 1552.52 nm (OC192-1P)	WMOTAX4EAA	Active	3EM12267AA
	LC12D 032 1-Port LR OC-192 Line Card, DC-SM-SC, 1551.72 nm (OC192-1P)	WMI8702FAA	Active	3EM12268AA
	LC12D 033 1-Port LR OC-192 Line Card, DC-SM-SC, 1550.92 nm (OC192-1P)	WMI870YFAA	Active	3EM12269AA
	LC12D 035 1-Port LR OC-192 Line Card, DC-SM-SC, 1549.32 nm (OC192-1P)	WMI8804FAA	Active	3EM12270AA
	LC12D 036 1-Port LR OC-192 Line Card, DC-SM-SC, 1548.51 nm (OC192-1P)	WMI870NFAA	Active	3EM12271AA
	LC12D 037 1-Port LR OC-192 Line Card, DC-SM-SC, 1547.72 nm (OC192-1P)	WMI890WFAA	Active	3EM12272AA
	LC12D 038 1-Port LR OC-192 Line Card, DC-SM-SC, 1546.92 nm (OC192-1P)	WMI870PFAA	Active	3EM12273AA
UDS-125	SSC 101 80 Gb STS Switch Card (SSC)	WMEDK0MDAC	Inactive	3EM12295AA
	SSC 102 80 Gb STS Switch Card (SSC)	WMEC905AAA	Inactive	3EM12295AB
	SSC 103 80 Gb STS Switch Card (SSC)	WMUCALTBAA	Active	3EM12295AC
	SSC 104 80 Gb STS Switch Card (SSC)	WMUCAP7BAA	Active	3EM12295AD
	SSC 104 80 Gb STS Switch Card (SSC)	WMUCAP7BAA	Active	3EM12295AD

UDS NUMBER	DESCRIPTION	CLEI	STATUS	PART NUMBER
UDS-126	TC 201 Stratum 3 Timing Card (TC)	WMEDM0PDAB	Inactive	3EM12309AA
	TC 301 Stratum 3 Timing Card (TC)	WMUCAFMBAA	Active	3EM12309AB
UDS-127	TMUX 201 2.5 Gb/s Transmux (TMUX)	WM1DD6YCAA	Active	3EM12308AA
	TMUX 301 2.5 Gb/s Transmux (TMUX)	WM1DDCXCAA	Active	3EM12308AB
UDS-128	VSC 101 5 Gb/s VT1.5 Switch Card (VSC)	WMEC60TAAD	Inactive	3EM12313AA
	VSC 101 5 Gb/s VT1.5 Switch Card (VSC)	WMEC606AAA	Active	3EM12313AB

Unit Data Sheet Cross-Reference by Part Number

PART NUMBER	DESCRIPTION	CLEI	STATUS	UDS NUMBER
3EM12215AA	ADME 013 E-Band East Add/Drop Module (ADM)	WMM9W02JRB	Active	UDS-112
3EM12216AA	ADMW 013 E-Band West Add/Drop Module (ADM)	WMM9W03JRB	Active	UDS-112
3EM12217AA	ADME 014 F-Band East Add/Drop Module (ADM)	WMM9W04JRB	Active	UDS-112
3EM12218AA	ADMW 014 F-Band West Add/Drop Module (ADM)	WMM9W05JRB	Active	UDS-112
3EM12219AA	CCC 101 Common Control Card (CCC)	WM3C20LJAE	Inactive	UDS-113
3EM12219AB	CCC 104 Common Control Card (CCC)	WMUCAJDBAA	Active	UDS-113
3EM12220AA	15RU 48-Port DS3/EC1 Connector Panel	WMM6BB0BRC	Active	UDS-105
3EM12221AA	15RU 96-Port DS3/EC1 Connector Panel	N/A	Active	UDS-106
3EM12222AA	DCME 020 20 km East Dispersion Compensation Module (DCM)	WMM9W01JRB	Active	UDS-114
3EM12223AA	DCMW 020 20 km West Dispersion Compensation Module (DCM)	WMM9W0ZJRB	Active	UDS-114
3EM12224AA	DCME 040 40 km East Dispersion Compensation Module (DCM)	WMM9WZ0JRB	Active	UDS-114
3EM12225AA	DCMW 040 40 kM West Dispersion Compensation Module (DCM)	WMM9W10JRB	Active	UDS-114
3EM12226AA	DCME 060 60 km East Dispersion Compensation Module (DCM)	WMM9W0XJRB	Active	UDS-114
3EM12227AA	DCMW 060 60 km West Dispersion Compensation Module (DCM)	WMM9W0YJRB	Active	UDS-114
3EM12228AA	DCME 080 80 km East Dispersion Compensation Module (DCM)	WMM9W20JRB	Active	UDS-114

PART NUMBER	DESCRIPTION	CLEI	STATUS	UDS NUMBER
3EM12229AA	DCMW 080 80 km West Dispersion Compensation Module (DCM)	WMM9W30JRB	Active	UDS-114
3EM12230AA	DWDME 101 E-Band E-Dense Wavelength Division Multiplexer (DWDM)	WMM9WX0JRB	Active	UDS-116
3EM12231AA	DWDMW 101 E-Band W-Dense Wavelength Division Multiplexer (DWDM)	WMM9WY0JRB	Active	UDS-116
3EM12232AA	DWDME 102 F-Band E-Dense Wavelength Division Multiplexer (DWDM)	WMM9W0WJRB	Active	UDS-116
3EM12233AA	DWDMW 102 F-Band W-Dense Wavelength Division Multiplexer (DWDM)	WMM9W0VJRB	Active	UDS-116
3EM12236AA	IFC1 101 12-Port DS3 Interface Card (DS3-12P)	WMI9GDXLAA	Inactive	UDS-118
3EM12238AA	LC2 101 12-Port IR OC-3 Line Card (OC3-12P)	WMOTAXNEAA	Active	UDS-121
3EM12238AB	LC2 102 12-Port IR OC-3 Line Card (OC3-12P)	WMOTBBBEAA	Active	UDS-121
3EM12241AA	LC5 101 4-Port IR OC-12 Line Card (OC12-4P)	WMOTAXSEAA	Active	UDS-122
3EM12241AB	LC5 102 4-Port IR OC-12 Line Card (OC12-4P)	WMOTBBEEAA	Active	UDS-122
3EM12250AA	LC10D 030 1-Port XLR OC-48 Line Card, DC-SM-SC, 1553.33 nm (OC48-1P)	WMOTAXXEAA	Active	UDS-123
3EM12250AB	LC10D 130 1-Port XLR OC-48 Line Card, DC-SM-SC, 1553.33 nm (OC48-1P)	WMOTBBKEAA	Active	UDS-123
3EM12251AA	LC10D 031 1-Port XLR OC-48 Line Card, DC-SM-SC, 1552.52 nm (OC48-1P)	WMOTAXYEAA	Active	UDS-123
3EM12251AB	LC10D 131 1-Port XLR OC-48 Line Card, DC-SM-SC, 1552.52 nm (OC48-1P)	WMOTBBLEAA	Active	UDS-123
3EM12252AA	LC10D 032 1-Port XLR OC-48 Line Card, DC-SM-SC, 1551.72 nm (OC48-1P)	WMOTAXZEAA	Active	UDS-123
3EM12252AB	LC10D 132 1-Port XLR OC-48 Line Card, DC-SM-SC, 1551.72 nm (OC48-1P)	WMOTBBMEAA	Active	UDS-123
3EM12253AA	LC10D 033 1-Port XLR OC-48 Line Card, DC-SM-SC, 1550.92 nm (OC48-1P)	WMOTAU4EAA	Active	UDS-123
3EM12253AB	LC10D 133 1-Port XLR OC-48 Line Card, DC-SM-SC, 1550.92 nm (OC48-1P)	WMOTBBNEAA	Active	UDS-123
3EM12254AA	LC10D 035 1-Port XLR OC-48 Line Card, DC-SM-SC, 1549.31 nm (OC48-1P)	WMOTAX0EAA	Active	UDS-123
3EM12254AB	LC10D 135 1-Port XLR OC-48 Line Card, DC-SM-SC, 1549.31 nm (OC48-1P)	WMOTBBPEAA	Active	UDS-123

PART NUMBER	DESCRIPTION	CLEI	STATUS	UDS NUMBER
3EM12255AA	LC10D 036 1-Port XLR OC-48 Line Card, DC-SM-SC, 1548.51 nm (OC48-1P)	WMOTAX1EAA	Active	UDS-123
3EM12255AB	LC10D 136 1-Port XLR OC-48 Line Card, DC-SM-SC, 1548.51 nm (OC48-1P)	WMOTBBREAA	Active	UDS-123
3EM12256AA	LC10D 037 1-Port XLR OC-48 Line Card, DC-SM-SC, 1547.72 nm (OC48-1P)	WMOTAX2EAA	Active	UDS-123
3EM12256AB	LC10D 137 1-Port XLR OC-48 Line Card, DC-SM-SC, 1547.72 nm (OC48-1P)	WMOTBBSEAA	Active	UDS-123
3EM12257AA	LC10D 038 1-Port XLR OC-48 Line Card, DC-SM-SC, 1546.92 nm (OC48-1P)	WM31808KAA	Active	UDS-123
3EM12257AB	LC10D 138 1-Port XLR OC-48 Line Card, DC-SM-SC, 1546.92 nm (OC48-1P)	WMOTBBTEAA	Active	UDS-123
3EM12266AA	LC12D 030 1-Port LR OC-192 Line Card, DC-SM-SC, 1553.33 nm (OC192-1P)	WMOTAX3EAA	Active	UDS-124
3EM12267AA	LC12D 031 1-Port LR OC-192 Line Card, DC-SM-SC, 1552.52 nm (OC192-1P)	WMOTAX4EAA	Active	UDS-124
3EM12268AA	LC12D 032 1-Port LR OC-192 Line Card, DC-SM-SC, 1551.72 nm (OC192-1P)	WMI8702FAA	Active	UDS-124
3EM12269AA	LC12D 033 1-Port LR OC-192 Line Card, DC-SM-SC, 1550.92 nm (OC192-1P)	WMI870YFAA	Active	UDS-124
3EM12270AA	LC12D 035 1-Port LR OC-192 Line Card, DC-SM-SC, 1549.32 nm (OC192-1P)	WMI8804FAA	Active	UDS-124
3EM12271AA	LC12D 036 1-Port LR OC-192 Line Card, DC-SM-SC, 1548.51 nm (OC192-1P)	WMI870NFAA	Active	UDS-124
3EM12272AA	LC12D 037 1-Port LR OC-192 Line Card, DC-SM-SC, 1547.72 nm (OC192-1P)	WMI890WFAA	Active	UDS-124
3EM12273AA	LC12D 038 1-Port LR OC-192 Line Card, DC-SM-SC, 1546.92 nm (OC192-1P)	WMI870PFAA	Active	UDS-124
3EM12277AA	15RU Shelf	WMM6DC0ARB	Active	UDS-102
3EM12279AA	15RU Fan Tray	WMPQAGSPAC	Active	UDS-109
3EM12295AA	SSC 101 80 Gb STS Switch Card (SSC)	WMEDK0MDAC	Inactive	UDS-125
3EM12295AB	SSC 102 80 Gb STS Switch Card (SSC)	WMEC905AAA	Inactive	UDS-125
3EM12295AC	SSC 103 80 Gb STS Switch Card (SSC)	WMUCALTBAA	Active	UDS-125
3EM12295AD	SSC 104 80 Gb STS Switch Card (SSC)	WMUCAP7BAA	Active	UDS-125
3EM12297AA	EDFA 103 Erbium Doped Fiber Amplifier, Pre-Amplifier (EDFA)	WMANEF0DAA	Active	UDS-117
3EM12298AA	EDFA 104 Erbium Doped Fiber Amplifier, Line-Amplifier (EDFA)	WMANFF0DAA	Active	UDS-117

PART NUMBER	DESCRIPTION	CLEI	STATUS	UDS NUMBER
3EM12301AA	LC7D 101 1-Port SR OC-48 Line Card, DC-SM-SC (OC48-1P)	WMOTAXUEAA	Active	UDS-123
3EM12301AB	LC7D 102 1-Port SR OC-48 Line Card, DC-SM-SC (OC48-1P)	WMOTBBGEAA	Active	UDS-123
3EM12302AA	LC7ID 101 1-Port IR OC-48 Line Card, DC-SM-SC (OC48-1P)	WMOTAXVEAA	Active	UDS-123
3EM12302AB	LC7ID 102 1-Port IR OC-48 Line Card, DC-SM-SC (OC48-1P)	WMOTBBHEAA	Active	UDS-123
3EM12307AA	18RU Fan Tray	NA	Active	UDS-110
3EM12308AA	TMUX 201 2.5 Gb/s Transmux (TMUX)	WM1DD6YCAA	Active	UDS-127
3EM12308AB	TMUX 301 2.5 Gb/s Transmux (TMUX)	WM1DDCXCAA	Active	UDS-127
3EM12309AA	TC 201 Stratum 3 Timing Card (TC)	WMEDM0PDAB	Inactive	UDS-126
3EM12309AB	TC 301 Stratum 3 Timing Card (TC)	WMUCAFMBAA	Active	UDS-126
3EM12310AA	IFC2 101 2-Port Gigabit Ethernet, LX (GIGE-2P)	WM6IV0SAAA	Active	UDS-120
3EM12310AB	IFC2 102 2-Port Gigabit Ethernet, LX (GIGE-2P)	TBD	Active	UDS-120
3EM12311AA	IFC4 101 2-Port Gigabit Ethernet, SX (GIGE-2P)	WM6IV0TAAA	Active	UDS-120
3EM12311AB	IFC4 102 2-Port Gigabit Ethernet, SX (GIGE-2P)	TBD	Active	UDS-120
3EM12312AA	LC8D 101 1-Port LR OC-48 Line Card, DC-SM-SC (OC48-1P)	WMOTAXWEAA	Active	UDS-123
3EM12312AB	LC8D 102 1-Port LR OC-48 Line Card, DC-SM-SC (OC48-1P)	WMOTBBJEAA	Active	UDS-123
3EM12313AA	VSC 101 5 Gb/s VT1.5 Switch Card (VSC)	WMEC60TAAD	Inactive	UDS-128
3EM12313AB	VSC 101 5 Gb/s VT1.5 Switch Card (VSC)	WMEC606AAA	Active	UDS-128
3EM12329AA	18RU 48-Port DS3/EC1 Connector Panel	N/A	Active	UDS-107
3EM12330AA	18RU 96-Port DS3/EC1 Connector Panel	N/A	Active	UDS-108
3EM12334AC	18RU Shelf	WMM6FC0ARA	Active	UDS-103
3EM12348AA	IFC1 201 12-Port DS3/EC1 Interface Card (ECC-12P)	WMI2CZ0CAA	Active	UDS-119
3EM14189AD	DS1 Splitter, Shelf 1	NA	Active	UDS-111
3EM14189AE	DS1 Splitter, Shelf 2	NA	Active	UDS-111
3EM14200AB	Power Distribution Unit, Quad Input (PDU-Quad)	NA	Active	UDS-104
3EM17343AA	DS0G 101 DS0 Groomer (DS0G)	SOUIARPAAA	Active	UDS-115
1AD014120032	Rack	NA	Active	UDS-101

UDS-101
Rack

PART NUMBER/ MNEMONIC	NAME	CLEI	ECI/ BAR CODE	CPR	STATUS
1AD014120032	Rack	NA	NA	NA	Active

FEATURES AND APPLICATION NOTES

- Holds up to two shelves and supporting mechanical equipment
- Provides integrated fiber management to manage customer interface connectivity
- Is constructed with EMI/RFI shielding

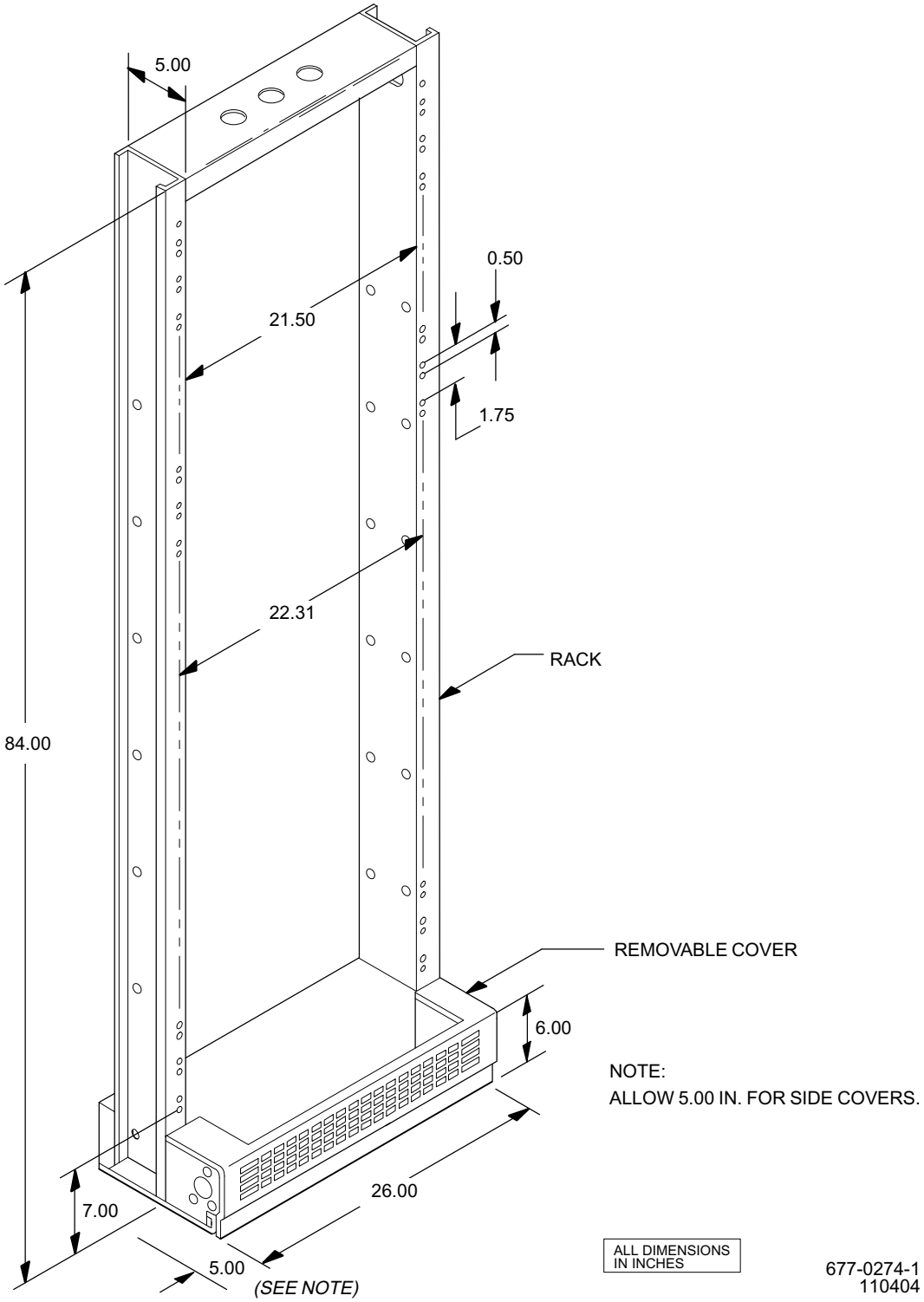
DESCRIPTION

The rack supports the shelves and mechanical equipment for up to 384 DS3, 384 EC1, 576 OC-3, 192 OC-12, 48 OC-48, or 8 OC-192 ports.

RACK

The rack is a 23-inch, unequal-flange, closed-channel earthquake rack. The rack is 7 feet high, 26 inches wide, and 15.5 inches deep. The installed width of the rack, including trim and cable, is 36 inches. A rack without shelves, trim, and cable is 7 feet high, 25.94 inches wide, and 10.09 inches deep. The rack provides 1.75-inch Electronic Industries Association (EIA) mounting increments. A standard 7-foot rack provides 43 EIA rack increments. See figure 101-1 for rack dimensions.

Figure 101-1. Seven-Foot Earthquake Rack, PN 1AD014120032

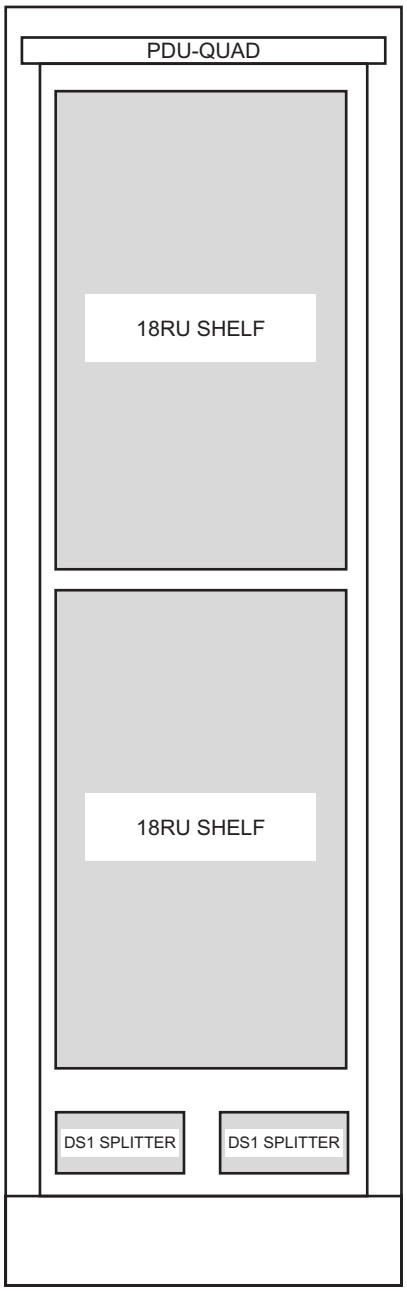


EQUIPMENT COMPLEMENT

A fully equipped rack contains up to two shelves and mechanical equipment that supports up to 384 DS3, 384 EC1, 576 OC-3, 192 OC-12, 48 OC-48, or 8 OC-192 ports. See figure 101-2. For more detailed information, refer to the appropriate unit data sheet:

- 15RU shelf, UDS-102 (includes module complement)
- 18RU shelf, UDS-103 (includes module complement)
- Power Distribution Unit, Quad Input (PDU-Quad), UDS-104
- DS1 Splitter, UDS-111

Figure 101-2. Rack



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UDS-102
15RU Shelf

PART NUMBER/ MNEMONIC	NAME	CLEI	ECI/ BAR CODE	CPR	STATUS
3EM12277AA	15RU Shelf	WMM6DC0ARB	443249	203330	Active

FEATURES AND APPLICATION NOTES

- Supports up to 192 DS3, 192 EC1, 288 OC-3, 96 OC-12, 24 OC-48, or 4 OC-192 ports
- Supports up to 80 Gb/s matrix switching
- Mounts in an American National Standards Institute (ANSI)-compliant customer rack
- Occupies 15 Electronic Industries Association (EIA) vertical rack spacing increments
- Is constructed with EMI/RFI shielding

DESCRIPTION

The 15RU shelf (see figure 102-1) houses the system modules and the Input/Output Cards (IOCs). The 15RU shelf consists of top, bottom, rear, and side panels; card guides; and a printed circuit backplane. Equipment connections are through connectors on the backplane.

The 15RU shelf, which mounts in a 23-inch unequal-flange rack, is 26 inches high, 19 inches wide, and 12 inches deep. The shelf requires 15 overall Electronic Industries Association (EIA) vertical increments of a 23-inch earthquake rack.

Mounting flanges on each side of the shelf secure the shelf to an ANSI rack. An ANSI rack holds up to two 15RU shelves.

The power panel is on the front of the 15RU shelf. See figure 102-2.

Figure 102-1. 15RU Shelf

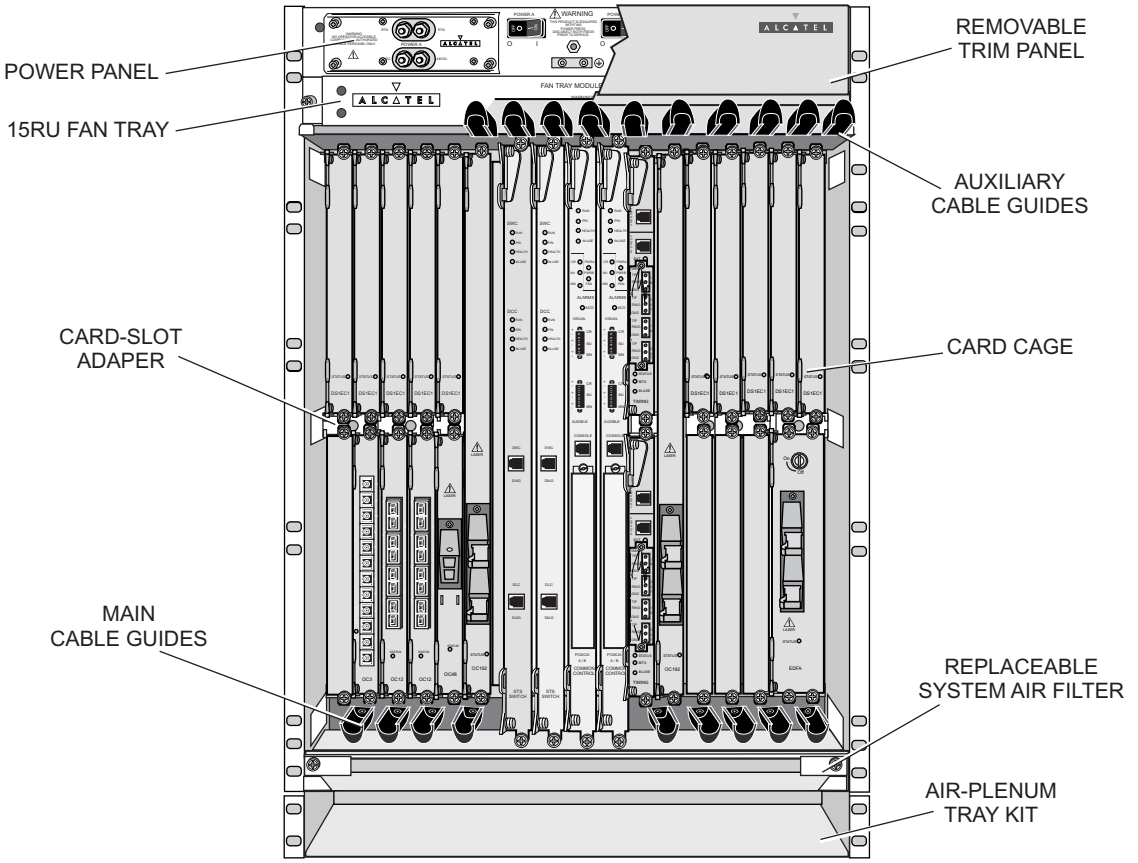
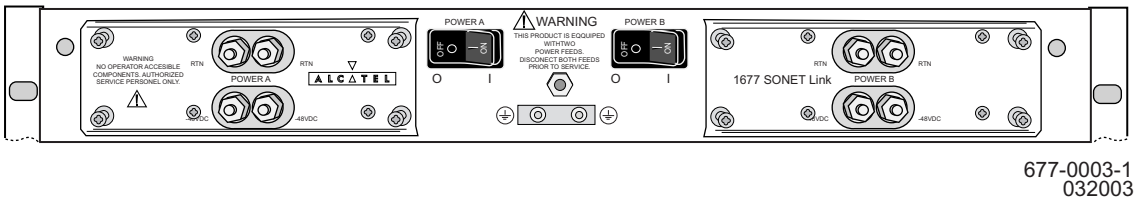


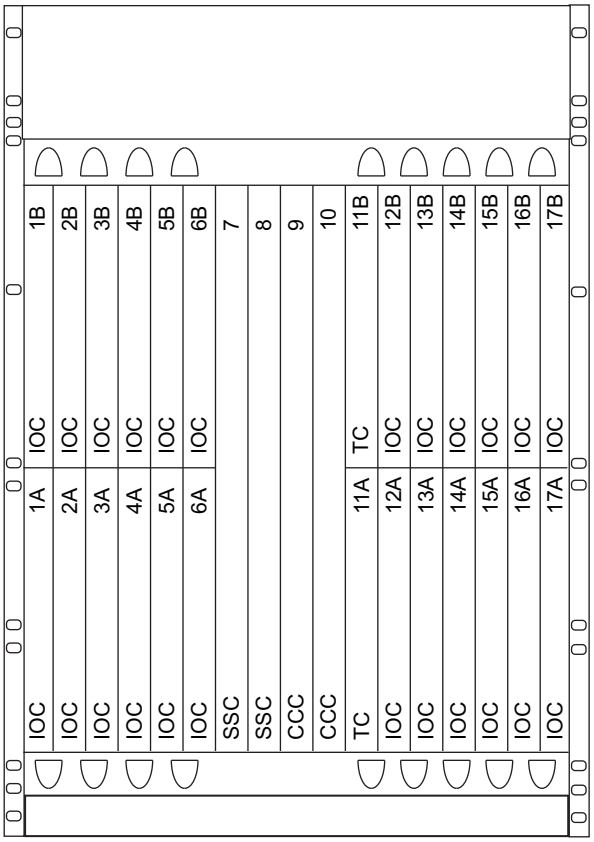
Figure 102-2. 15RU Power Panel



EQUIPMENT COMPLEMENT

See figure 102-3 for the module complement of a 15RU shelf that contains the plug-in equipment (refer to table 102-A). Refer to the appropriate unit data sheet for detailed information.

Figure 102-3. 15RU Shelf Module Complement



NOTES:
1. HALF-SIZED A AND B SLOTS CAN BE COMBINED TO FORM ONE FULL-SIZED AB SLOT.
2. ANY OF THE FOLLOWING MODULES CAN BE EQUIPPED IN AN IOC SLOT: DS3-12P, ECC-12P, EDFA (TWO ADJACENT HALF-SIZED SLOTS), GIGE-2P, OC3-12P, OC12-4P, OC48-1P, TMUX, VSC.
3. DS0Gs CAN BE EQUIPPED ONLY IN FULL-HEIGHT SLOTS 3 AND 4 OR 14 AND 15. ONLY ONE PAIR OF DS0Gs CAN BE EQUIPPED IN A SHELF.
4. OC192-1P INSTALLS INTO FULL-HEIGHT SLOTS 5, 6, 12, AND 13.

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Table 102-A. 15RU Module Complement

MODULE/ UNIT DATA SHEET	PART NO.	CLEI	QTY	SLOT
15RU Fan Tray/ UDS-109	3EM12279AA	WMPQAGSPAC	1	N/A
CCC 101 Common Control Card (CCC)/ UDS-113 OR	3EM12219AA	WM3C20LJAE	2	9, 10

Table 102-A. 15RU Module Complement (cont.)

MODULE/ UNIT DATA SHEET	PART NO.	CLEI	QTY	SLOT
CCC 104 Common Control Card (CCC)/ UDS-113	3EM12219AB	WMUCAJDBAA	2	9, 10
SSC 101 80 Gb STS Switch Card (SSC)/ UDS-125	3EM12295AA	WMEDK0MDAC	2	7, 8
OR				
SSC 102 80 Gb STS Switch Card (SSC)/ UDS-125	3EM12295AB	WMEC905AAA	2	7, 8
OR				
SSC 103 80 Gb STS Switch Card (SSC)/ UDS-125	3EM12295AC	WMUCALTBAA	2	7, 8
OR				
SSC 103 80 Gb STS Switch Card (SSC)/ UDS-125	3EM12295AD	WMUCAP7BAA	2	7, 8
TC 201 Stratum 3 Timing Card (TC)/ UDS-126	3EM12309AA	WMEDM0PDAB	2	11A, 11B
OR				
TC 301 Stratum 3 Timing Card (TC)/ UDS-126	3EM12309AB	WMUCAFMBAA	2	11A, 11B
DS0G 101 DS0 Groomer UDS-115	3EM17343AA	SOUIARPAAA	Up to 2	3/4-AB or 14/15-AB
OR				
EDFA 103 Erbium Doped Fiber Amplifier, Pre-Amplifier (EDFA)/ UDS-117	3EM12297AA	WMANEF0DAA	Up to12	1A&2A, 1B&2B, 3A&4A, 3B&4B, 5A&6A, 5B&6B, 12A&13A, 12B&13B, 14A&15A, 14B&15B, 16A&17A, 16B&17B
OR				

Table 102-A. 15RU Module Complement (cont.)

MODULE/ UNIT DATA SHEET	PART NO.	CLEI	QTY	SLOT
EDFA 104 Erbium Doped Fiber Amplifier, Line-Amplifier (EDFA)/ UDS-117	3EM12298AA	WMANFF0DAA	Up to12	1A&2A, 1B&2B, 3A&4A, 3B&4B, 5A&6A, 5B&6B, 12A&13A, 12B&13B, 14A&15A, 14B&15B, 16A&17A, 16B&17B
OR				
IFC1 101 12-Port DS3 Interface Card (DS3-12P)/ UDS-118	3EM12236AA	WMI9GDXLAA	Up to 20	1A-5A, 1B-5B, 12A-16A, 12B-16B
OR				
IFC1 201 12-Port DS3/EC1 Interface Card (ECC-12P)/ UDS-119	3EM12348AA	WMI2CZ0CAA	Up to 20	1A-5A, 1B-5B, 12A-16A, 12B-16B
OR				
IFC2 101 2-Port Gigabit Ethernet, LX (GIGE-2P)/ UDS-120	3EM12310AA	WM6IV0SAAA	Up to 24	1A-6A, 1B-6B, 12A-17A, 12B-17B
OR				
IFC2 102 2-Port Gigabit Ethernet, LX (GIGE-2P)/ UDS-120	3EM12310AB	TBD	Up to 24	1A-6A, 1B-6B, 12A-17A, 12B-17B
OR				
IFC4 101 2-Port Gigabit Ethernet, SX (GIGE-2P)/ UDS-120	3EM12311AA	WM6IV0TAAA	Up to 24	1A-6A, 1B-6B, 12A-17A, 12B-17B
OR				
IFC4 102 2-Port Gigabit Ethernet, SX (GIGE-2P)/ UDS-120	3EM12311AB	TBD	Up to 24	1A-6A, 1B-6B, 12A-17A, 12B-17B
OR				
LC2 101 12-Port IR OC-3 Line Card (OC3-12P)/ UDS-121	3EM12238AA	WMOTAXNEAA	Up to 24	1A-6A, 1B-6B, 12A-17A, 12B-17B

Table 102-A. 15RU Module Complement (cont.)

MODULE/ UNIT DATA SHEET	PART NO.	CLEI	QTY	SLOT
OR				
LC2 102 12-Port IR OC-3 Line Card (OC3-12P)/ UDS-121	3EM12238AB	WMOTBBBEAA	Up to 24	1A-6A, 1B-6B, 12A-17A, 12B-17B
OR				
LC5 101 4-Port IR OC-12 Line Card (OC12-4P)/ UDS-122	3EM12241AA	WMOTAXSEAA	Up to 24	1A-6A, 1B-6B, 12A-17A, 12B-17B
OR				
LC5 102 4-Port IR OC-12 Line Card (OC12-4P)/ UDS-122	3EM12241AB	WMOTBBEEAA	Up to 24	1A-6A, 1B-6B, 12A-17A, 12B-17B
OR				
LC10D 030 1-Port XLR OC-48 Line Card, DC-SM-SC, 1553.33 nm (OC48-1P)/ UDS-123	3EM12250AA	WMOTAXXEAA	Up to 24	1A-6A, 1B-6B, 12A-17A, 12B-17B
OR				
LC10D 130 1-Port XLR OC-48 Line Card, DC-SM-SC, 1553.33 nm (OC48-1P)/ UDS-123	3EM12250AB	WMOTBBKEAA	Up to 24	1A-6A, 1B-6B, 12A-17A, 12B-17B
OR				
LC10D 031 1-Port XLR OC-48 Line Card, DC-SM-SC, 1552.52 nm (OC48-1P)/ UDS-123	3EM12251AA	WMOTAXYEAA	Up to 24	1A-6A, 1B-6B, 12A-17A, 12B-17B
OR				
LC10D 131 1-Port XLR OC-48 Line Card, DC-SM-SC, 1552.52 nm (OC48-1P)/ UDS-123	3EM12251AB	WMOTBBLEAA	Up to 24	1A-6A, 1B-6B, 12A-17A, 12B-17B
OR				
LC10D 032 1-Port XLR OC-48 Line Card, DC-SM-SC, 1551.72 nm (OC48-1P)/ UDS-123	3EM12252AA	WMOTAXZEAA	Up to 24	1A-6A, 1B-6B, 12A-17A, 12B-17B
OR				

Table 102-A. 15RU Module Complement (cont.)

MODULE/ UNIT DATA SHEET	PART NO.	CLEI	QTY	SLOT
LC10D 132 1-Port XLR OC-48 Line Card, DC-SM-SC, 1551.72 nm (OC48-1P)/ UDS-123	3EM12252AB	WMOTBBMEAA	Up to 24	1A-6A, 1B-6B, 12A-17A, 12B-17B
OR				
LC10D 033 1-Port XLR OC-48 Line Card, DC-SM-SC, 1550.92 nm (OC48-1P)/ UDS-123	3EM12253AA	WMOTAU4EAA	Up to 24	1A-6A, 1B-6B, 12A-17A, 12B-17B
OR				
LC10D 133 1-Port XLR OC-48 Line Card, DC-SM-SC, 1550.92 nm (OC48-1P)/ UDS-123	3EM12253AB	WMOTBBNEAA	Up to 24	1A-6A, 1B-6B, 12A-17A, 12B-17B
OR				
LC10D 035 1-Port XLR OC-48 Line Card, DC-SM-SC, 1549.31 nm (OC48-1P)/ UDS-123	3EM12254AA	WMOTAX0EAA	Up to 24	1A-6A, 1B-6B, 12A-17A, 12B-17B
OR				
LC10D 135 1-Port XLR OC-48 Line Card, DC-SM-SC, 1549.31 nm (OC48-1P)/ UDS-123	3EM12254AB	WMOTBBPEAA	Up to 24	1A-6A, 1B-6B, 12A-17A, 12B-17B
OR				
LC10D 036 1-Port XLR OC-48 Line Card, DC-SM-SC, 1548.51 nm (OC48-1P)/ UDS-123	3EM12255AA	WMOTAX1EAA	Up to 24	1A-6A, 1B-6B, 12A-17A, 12B-17B
OR				
LC10D 136 1-Port XLR OC-48 Line Card, DC-SM-SC, 1548.51 nm (OC48-1P)/ UDS-123	3EM12255AB	WMOTBBREAA	Up to 24	1A-6A, 1B-6B, 12A-17A, 12B-17B
OR				
LC10D 037 1-Port XLR OC-48 Line Card, DC-SM-SC, 1547.72 nm (OC48-1P)/ UDS-123	3EM12256AA	WMOTAX2EAA	Up to 24	1A-6A, 1B-6B, 12A-17A, 12B-17B
OR				

Table 102-A. 15RU Module Complement (cont.)

MODULE/ UNIT DATA SHEET	PART NO.	CLEI	QTY	SLOT
LC10D 137 1-Port XLR OC-48 Line Card, DC-SM-SC, 1547.72 nm (OC48-1P)/ UDS-123	3EM12256AB	WMOTBBSEAA	Up to 24	1A-6A, 1B-6B, 12A-17A, 12B-17B
OR				
LC10D 038 1-Port XLR OC-48 Line Card, DC-SM-SC, 1546.92 nm (OC48-1P)/ UDS-123	3EM12257AA	WM31808KAA	Up to 24	1A-6A, 1B-6B, 12A-17A, 12B-17B
OR				
LC10D 138 1-Port XLR OC-48 Line Card, DC-SM-SC, 1546.92 nm (OC48-1P)/ UDS-123	3EM12257AB	WMOTBBTEAA	Up to 24	1A-6A, 1B-6B, 12A-17A, 12B-17B
OR				
LC7D 101 1-Port SR OC-48 Line Card, DC-SM-SC (OC48-1P)/ UDS-123	3EM12301AA	WMOTAXUEAA	Up to 24	1A-6A, 1B-6B, 12A-17A, 12B-17B
OR				
LC7D 102 1-Port SR OC-48 Line Card, DC-SM-SC (OC48-1P)/ UDS-123	3EM12301AB	WMOTBBGEAA	Up to 24	1A-6A, 1B-6B, 12A-17A, 12B-17B
OR				
LC7ID 101 1-Port IR OC-48 Line Card, DC-SM-SC (OC48-1P)/ UDS-123	3EM12302AA	WMOTAXVEAA	Up to 24	1A-6A, 1B-6B, 12A-17A, 12B-17B
OR				
LC7ID 102 1-Port IR OC-48 Line Card, DC-SM-SC (OC48-1P)/ UDS-123	3EM12302AB	WMOTBBHEAA	Up to 24	1A-6A, 1B-6B, 12A-17A, 12B-17B
OR				
LC8D 101 1-Port LR OC-48 Line Card, DC-SM-SC (OC48-1P)/ UDS-123	3EM12312AA	WMOTAXWEAA	Up to 24	1A-6A, 1B-6B, 12A-17A, 12B-17B
OR				
LC8D 102 1-Port LR OC-48 Line Card, DC-SM-SC (OC48-1P)/ UDS-123	3EM12312AB	WMOTBBJEAA	Up to 24	1A-6A, 1B-6B, 12A-17A, 12B-17B
OR				

Table 102-A. 15RU Module Complement (cont.)

MODULE/ UNIT DATA SHEET	PART NO.	CLEI	QTY	SLOT
LC12D 030 1-Port LR OC-192 Line Card, DC-SM-SC, 1553.33 nm (OC192-1P)/ UDS-124	3EM12266AA	WMOTAX3EAA	Up to 4	5AB, 6AB, 12AB, 13AB
OR				
LC12D 031 1-Port LR OC-192 Line Card, DC-SM-SC, 1552.52 nm (OC192-1P)/ UDS-124	3EM12267AA	WMOTAX4EAA	Up to 4	5AB, 6AB, 12AB, 13AB
OR				
LC12D 032 1-Port LR OC-192 Line Card, DC-SM-SC, 1551.72 nm (OC192-1P)/ UDS-124	3EM12268AA	WMI8702FAA	Up to 4	5AB, 6AB, 12AB, 13AB
OR				
LC12D 033 1-Port LR OC-192 Line Card, DC-SM-SC, 1550.92 nm (OC192-1P)/ UDS-124	3EM12269AA	WMI870YFAA	Up to 4	5AB, 6AB, 12AB, 13AB
OR				
LC12D 035 1-Port LR OC-192 Line Card, DC-SM-SC, 1549.32 nm (OC192-1P)/ UDS-124	3EM12270AA	WMI8804FAA	Up to 4	5AB, 6AB, 12AB, 13AB
OR				
LC12D 036 1-Port LR OC-192 Line Card, DC-SM-SC, 1548.51 nm (OC192-1P)/ UDS-124	3EM12271AA	WMI870NFAA	Up to 4	5AB, 6AB, 12AB, 13AB
OR				
LC12D 037 1-Port LR OC-192 Line Card, DC-SM-SC, 1547.72 nm (OC192-1P)/ UDS-124	3EM12272AA	WMI890WFAA	Up to 4	5AB, 6AB, 12AB, 13AB
OR				
LC12D 038 1-Port LR OC-192 Line Card, DC-SM-SC, 1546.92 nm (OC192-1P)/ UDS-124	3EM12273AA	WMI870PFAA	Up to 4	5AB, 6AB, 12AB, 13AB
OR				

Table 102-A. 15RU Module Complement (cont.)

MODULE/ UNIT DATA SHEET	PART NO.	CLEI	QTY	SLOT
TMUX 201 2.5 Gb/s Transmux (TMUX)/ UDS-127	3EM12308AA	WM1DD6YCAA	Up to 4	5A, 6A, 5B, 6B, 12A, 13A, 12B, 13B
OR				
TMUX 301 2.5 Gb/s Transmux (TMUX)/ UDS-127	3EM12308AB	WM1DDCXCAA	Up to 4	5A, 6A, 5B, 6B, 12A, 13A, 12B, 13B
OR				
VSC 101 5 Gb/s VT1.5 Switch Card (VSC)/ UDS-128	3EM12313AA	WMEC60TAAD	Up to 4	5A, 6A, 5B, 6B, 12A, 13A, 12B, 13B
OR				
VSC 101 5 Gb/s VT1.5 Switch Card (VSC)/ UDS-128	3EM12313AB	WMEC606AAA	Up to 4	5A, 6A, 5B, 6B, 12A, 13A, 12B, 13B

FUNCTIONAL OVERVIEW

Modules are either half-height or full-height size (see figure 102-3). Two types of removable card-slot adapters can convert either two adjacent slots or three adjacent slots for half-height module applications. A card-slot adapter to convert one slot is not supported.

Common equipment includes two half-high TCs, two full-high SSCs, and two full-high CCCs. The minimum 15RU shelf configuration that supports transmission is two CCCs, two TCs, two SSCs, and one IOC.

For fault protection, the system modules support redundancy. Redundancy is accomplished by installing a primary module and a secondary module in adjacent slots. During operation the first module to become operational is designated the primary module and the other as the secondary module. The modules remain in these operating states unless a problem with the primary module is detected or a user intentionally changes the module state through software or by activating a module interlock switch manually. If any of these actions occurs, the secondary module will become the primary module, and the old primary module will become the secondary module.

All IOCs are connected to the SSCs through multiple serial telecom busses (STS-12 serial links) running at 777 Mb/s. The serial telecom bus uses 8 B/10 B encoding to bring an STS-12 signal to a rate of 777 Mb/s. The IOCs are all cross-coupled to the working and protection SSCs.

All IOC slots share a common set of four serial telecom bus signals, which together are capable of delivering 48 STS-1s to the SSCs. Eight IOC slots are high-capacity slots, which have four additional serial telecom bus signals that provide 96 STS-1s to the SSC. The common set of four serial telecom bus signals in both the high and low-capacity slots allow IOCs with a capacity of 48 STS-1s to be inserted into any of the slots. Each SSC is connected to all IOCs, so the backplane must provide 128 serial telecom bus links (which represents 512 connections at 777 Mb/s) from each SSC to all IOCs.

The 15RU shelf backplane provides –48V and return distribution to all modules in addition to all signals required for system synchronization and the control system.

Airflow design is integrated into each shelf. The airflow design is a pull system consisting of redundant integrated fans in the individual shelves. Air is pulled from the inlet at the bottom-front of the shelf through the shelf and out the exhaust at the top rear of the shelf.

UDS-103
18RU Shelf

PART NUMBER/ MNEMONIC	NAME	CLEI	ECI/ BAR CODE	CPR	STATUS
3EM12334AC	18RU Shelf	WMM6FC0ARA	445920	207197	Active

FEATURES AND APPLICATION NOTES

- Supports up to 192 DS3, 192 EC1, 288 OC-3, 96 OC-12, 24 OC-48, or 4 OC-192 ports
- Supports up to 80 Gb/s matrix switching
- Mounts in a 26-inch unequal-flange earthquake rack
- Occupies 18 Electronic Industries Association (EIA) vertical rack spacing increments
- Is constructed with EMI/RFI shielding

DESCRIPTION

The 18RU shelf (see figure 103-1) houses the equipment that performs either matrix or I/O functions. The 18RU shelf consists of top, bottom, rear, and side panels; card guides; and a printed circuit backplane. Equipment connections are through connectors on the backplane.

The 18RU shelf, which mounts in a 23-inch unequal-flange rack, is 31.40 inches high, 19.12 inches wide, and 12.67 inches deep. See figure 103-2. The shelf requires 18 overall Electronic Industries Association (EIA) vertical increments of a 23-inch earthquake rack.

Mounting flanges on each side of the shelf secure the shelf to an American National Standards Institute (ANSI) rack. An ANSI rack holds up to two 18RU shelves.

The power panel is on the rear of the 18RU shelf. See figure 103-3.

Figure 103-1. 18RU Shelf

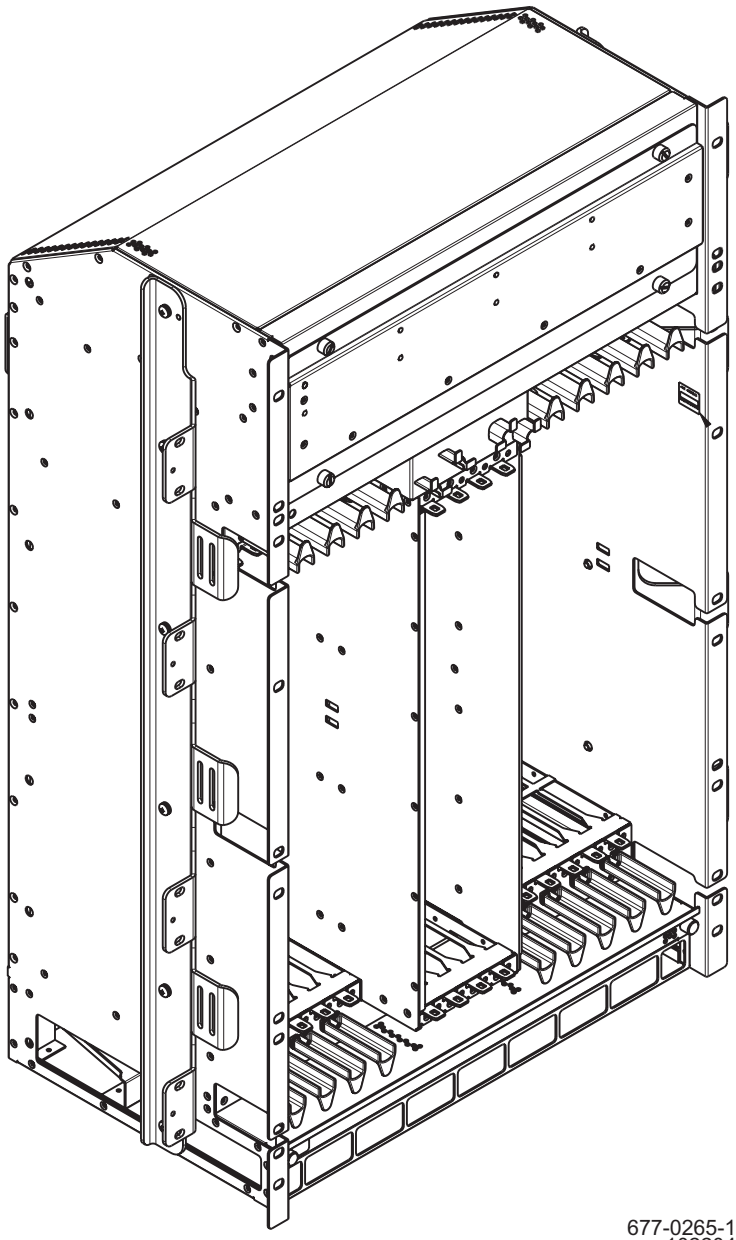

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Figure 103-2. 18RU Shelf Dimensions

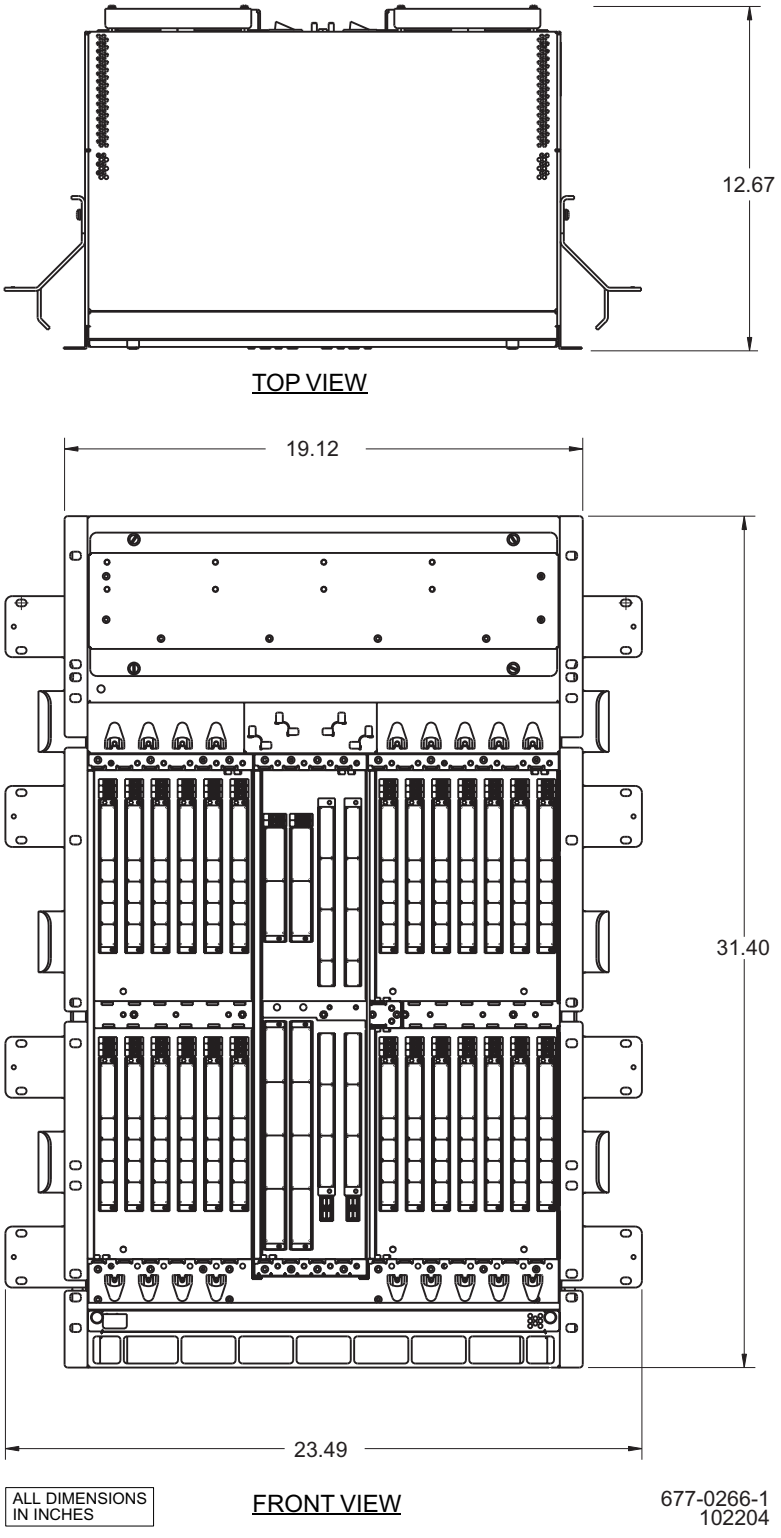
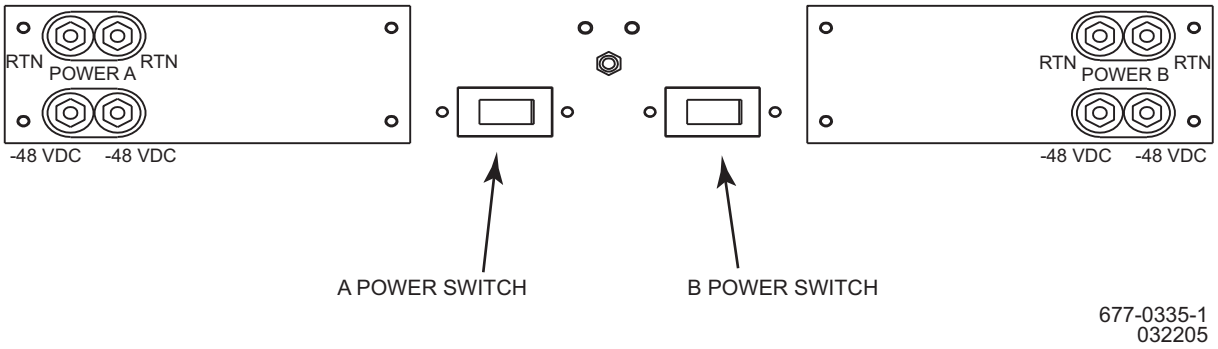


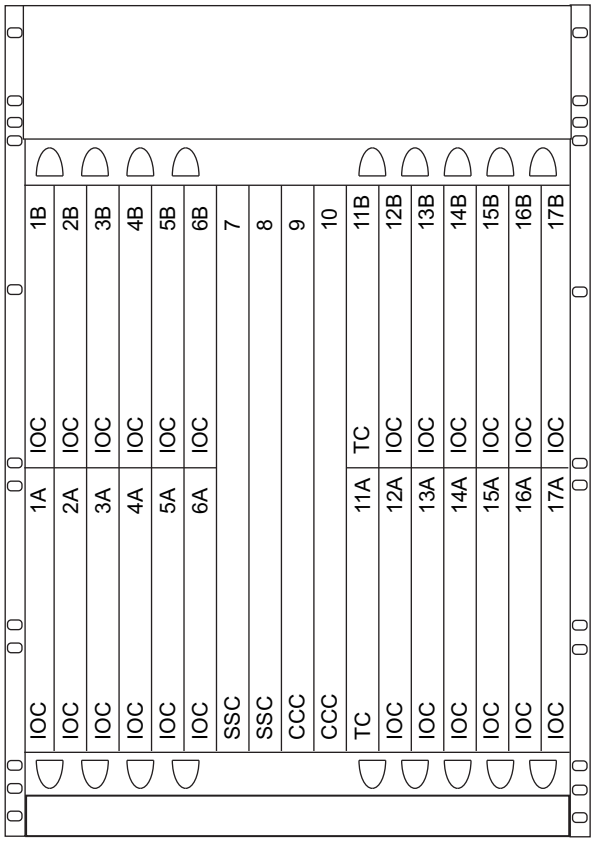
Figure 103-3. 18RU Power Panel



EQUIPMENT COMPLEMENT

See figure 103-4 for the module complement of an 18RU shelf that contains the plug-in equipment (refer to table 103-A). Refer to the appropriate unit data sheet for detailed information.

Figure 103-4. 18RU Shelf Module Complement



NOTES:
1. HALF-SIZED A AND B SLOTS CAN BE COMBINED TO FORM ONE FULL-SIZED AB SLOT.
2. ANY OF THE FOLLOWING MODULES CAN BE EQUIPPED IN AN IOC SLOT: DS3-12P, ECC-12P, EDFA (TWO ADJACENT HALF-SIZED SLOTS), GIGE-2P, OC3-12P, OC12-4P, OC48-1P, TMUX, VSC.
3. DS0Gs CAN BE EQUIPPED ONLY IN FULL-HEIGHT SLOTS 3 AND 4 OR 14 AND 15. ONLY ONE PAIR OF DS0Gs CAN BE EQUIPPED IN A SHELF.
4. OC192-1P INSTALLS INTO FULL-HEIGHT SLOTS 5, 6, 12, AND 13.

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Table 103-A. 18RU Module Complement

MODULE/ UNIT DATA SHEET	PART NO.	CLEI	QTY	SLOT
18RU Fan Tray/ UDS-110	3EM12307AA	NA	1	N/A
CCC 101 Common Control Card (CCC)/ UDS-113	3EM12219AA	WM3C20LJAE	2	9, 10
OR				
CCC 104 Common Control Card (CCC)/ UDS-113	3EM12219AB	WMUCAJDBAA	2	9, 10
SSC 101 80 Gb STS Switch Card (SSC)/ UDS-125	3EM12295AA	WMEDK0MDAC	2	7, 8
OR				
SSC 102 80 Gb STS Switch Card (SSC)/ UDS-125	3EM12295AB	WMEC905AAA	2	7, 8
OR				
SSC 103 80 Gb STS Switch Card (SSC)/ UDS-125	3EM12295AC	WMUCALTBAA	2	7, 8
OR				
SSC 103 80 Gb STS Switch Card (SSC)/ UDS-125	3EM12295AD	WMUCAP7BAA	2	7, 8
TC 201 Stratum 3 Timing Card (TC)/ UDS-126	3EM12309AA	WMEDM0PDAB	2	11A, 11B
OR				
TC 301 Stratum 3 Timing Card (TC)/ UDS-126	3EM12309AB	WMUCAFMBAA	2	11A, 11B
DS0G 101 DS0 Groomer UDS-115	3EM17343AA	SOUIARPAAA	Up to 2	3/4-AB or 14/15-AB
OR				

Table 103-A. 18RU Module Complement (cont.)

MODULE/ UNIT DATA SHEET	PART NO.	CLEI	QTY	SLOT
EDFA 103 Erbium Doped Fiber Amplifier, Pre-Amplifier (EDFA)/ UDS-117	3EM12297AA	WMANEF0DAA	Up to12	1A&2A, 1B&2B, 3A&4A, 3B&4B, 5A&6A, 5B&6B, 12A&13A, 12B&13B, 14A&15A, 14B&15B, 16A&17A, 16B&17B
OR				
EDFA 104 Erbium Doped Fiber Amplifier, Line-Amplifier (EDFA)/ UDS-117	3EM12298AA	WMANFF0DAA	Up to12	1A&2A, 1B&2B, 3A&4A, 3B&4B, 5A&6A, 5B&6B, 12A&13A, 12B&13B, 14A&15A, 14B&15B, 16A&17A, 16B&17B
OR				
IFC1 101 12-Port DS3 Interface Card (DS3-12P)/ UDS-118	3EM12236AA	WMI9GDXLAA	Up to 20	1A-5A, 1B-5B, 12A-16A, 12B-16B
OR				
IFC1 201 12-Port DS3/EC1 Interface Card (ECC-12P)/ UDS-119	3EM12348AA	WMI2CZ0CAA	Up to 20	1A-5A, 1B-5B, 12A-16A, 12B-16B
OR				
IFC2 101 2-Port Gigabit Ethernet, LX (GIGE-2P)/ UDS-120	3EM12310AA	WM6IV0SAAA	Up to 24	1A-6A, 1B-6B, 12A-17A, 12B-17B
OR				
IFC2 102 2-Port Gigabit Ethernet, LX (GIGE-2P)/ UDS-120	3EM12310AB	TBD	Up to 24	1A-6A, 1B-6B, 12A-17A, 12B-17B

Table 103-A. 18RU Module Complement (cont.)

MODULE/ UNIT DATA SHEET	PART NO.	CLEI	QTY	SLOT
OR				
IFC4 101 2-Port Gigabit Ethernet, SX (GIGE-2P)/ UDS-120	3EM12311AA	WM6IV0TAAA	Up to 24	1A-6A, 1B-6B, 12A-17A, 12B-17B
OR				
IFC4 102 2-Port Gigabit Ethernet, SX (GIGE-2P)/ UDS-120	3EM12311AB	TBD	Up to 24	1A-6A, 1B-6B, 12A-17A, 12B-17B
OR				
LC2 101 12-Port IR OC-3 Line Card (OC3-12P)/ UDS-121	3EM12238AA	WMOTAXNEAA	Up to 24	1A-6A, 1B-6B, 12A-17A, 12B-17B
OR				
LC2 102 12-Port IR OC-3 Line Card (OC3-12P)/ UDS-121	3EM12238AB	WMOTBBBEAA	Up to 24	1A-6A, 1B-6B, 12A-17A, 12B-17B
OR				
LC5 101 4-Port IR OC-12 Line Card (OC12-4P)/ UDS-122	3EM12241AA	WMOTAXSEAA	Up to 24	1A-6A, 1B-6B, 12A-17A, 12B-17B
OR				
LC5 102 4-Port IR OC-12 Line Card (OC12-4P)/ UDS-122	3EM12241AB	WMOTBBEEAA	Up to 24	1A-6A, 1B-6B, 12A-17A, 12B-17B
OR				
LC10D 030 1-Port XLR OC-48 Line Card, DC-SM-SC, 1553.33 nm (OC48-1P)/ UDS-123	3EM12250AA	WMOTAXXEAA	Up to 24	1A-6A, 1B-6B, 12A-17A, 12B-17B
OR				
LC10D 130 1-Port XLR OC-48 Line Card, DC-SM-SC, 1553.33 nm (OC48-1P)/ UDS-123	3EM12250AB	WMOTBBKEAA	Up to 24	1A-6A, 1B-6B, 12A-17A, 12B-17B
OR				
LC10D 031 1-Port XLR OC-48 Line Card, DC-SM-SC, 1552.52 nm (OC48-1P)/ UDS-123	3EM12251AA	WMOTAXYEAA	Up to 24	1A-6A, 1B-6B, 12A-17A, 12B-17B

Table 103-A. 18RU Module Complement (cont.)

MODULE/ UNIT DATA SHEET	PART NO.	CLEI	QTY	SLOT
OR				
LC10D 131 1-Port XLR OC-48 Line Card, DC-SM-SC, 1552.52 nm (OC48-1P)/ UDS-123	3EM12251AB	WMOTBBLEAA	Up to 24	1A-6A, 1B-6B, 12A-17A, 12B-17B
OR				
LC10D 032 1-Port XLR OC-48 Line Card, DC-SM-SC, 1551.72 nm (OC48-1P)/ UDS-123	3EM12252AA	WMOTAXZEAA	Up to 24	1A-6A, 1B-6B, 12A-17A, 12B-17B
OR				
LC10D 132 1-Port XLR OC-48 Line Card, DC-SM-SC, 1551.72 nm (OC48-1P)/ UDS-123	3EM12252AB	WMOTBBMEAA	Up to 24	1A-6A, 1B-6B, 12A-17A, 12B-17B
OR				
LC10D 033 1-Port XLR OC-48 Line Card, DC-SM-SC, 1550.92 nm (OC48-1P)/ UDS-123	3EM12253AA	WMOTAU4EAA	Up to 24	1A-6A, 1B-6B, 12A-17A, 12B-17B
OR				
LC10D 133 1-Port XLR OC-48 Line Card, DC-SM-SC, 1550.92 nm (OC48-1P)/ UDS-123	3EM12253AB	WMOTBBNEAA	Up to 24	1A-6A, 1B-6B, 12A-17A, 12B-17B
OR				
LC10D 035 1-Port XLR OC-48 Line Card, DC-SM-SC, 1549.31 nm (OC48-1P)/ UDS-123	3EM12254AA	WMOTAX0EAA	Up to 24	1A-6A, 1B-6B, 12A-17A, 12B-17B
OR				
LC10D 135 1-Port XLR OC-48 Line Card, DC-SM-SC, 1549.31 nm (OC48-1P)/ UDS-123	3EM12254AB	WMOTBBPEAA	Up to 24	1A-6A, 1B-6B, 12A-17A, 12B-17B
OR				
LC10D 036 1-Port XLR OC-48 Line Card, DC-SM-SC, 1548.51 nm (OC48-1P)/ UDS-123	3EM12255AA	WMOTAX1EAA	Up to 24	1A-6A, 1B-6B, 12A-17A, 12B-17B

Table 103-A. 18RU Module Complement (cont.)

MODULE/ UNIT DATA SHEET	PART NO.	CLEI	QTY	SLOT
OR				
LC10D 136 1-Port XLR OC-48 Line Card, DC-SM-SC, 1548.51 nm (OC48-1P)/ UDS-123	3EM12255AB	WMOTBBREAA	Up to 24	1A-6A, 1B-6B, 12A-17A, 12B-17B
OR				
LC10D 037 1-Port XLR OC-48 Line Card, DC-SM-SC, 1547.72 nm (OC48-1P)/ UDS-123	3EM12256AA	WMOTAX2EAA	Up to 24	1A-6A, 1B-6B, 12A-17A, 12B-17B
OR				
LC10D 137 1-Port XLR OC-48 Line Card, DC-SM-SC, 1547.72 nm (OC48-1P)/ UDS-123	3EM12256AB	WMOTBBSEAA	Up to 24	1A-6A, 1B-6B, 12A-17A, 12B-17B
OR				
LC10D 038 1-Port XLR OC-48 Line Card, DC-SM-SC, 1546.92 nm (OC48-1P)/ UDS-123	3EM12257AA	WM31808KAA	Up to 24	1A-6A, 1B-6B, 12A-17A, 12B-17B
OR				
LC10D 138 1-Port XLR OC-48 Line Card, DC-SM-SC, 1546.92 nm (OC48-1P)/ UDS-123	3EM12257AB	WMOTBBTEAA	Up to 24	1A-6A, 1B-6B, 12A-17A, 12B-17B
OR				
LC7D 101 1-Port SR OC-48 Line Card, DC-SM-SC (OC48-1P)/ UDS-123	3EM12301AA	WMOTAXUEAA	Up to 24	1A-6A, 1B-6B, 12A-17A, 12B-17B
OR				
LC7D 102 1-Port SR OC-48 Line Card, DC-SM-SC (OC48-1P)/ UDS-123	3EM12301AB	WMOTBBGEAA	Up to 24	1A-6A, 1B-6B, 12A-17A, 12B-17B
OR				
LC7ID 101 1-Port IR OC-48 Line Card, DC-SM-SC (OC48-1P)/ UDS-123	3EM12302AA	WMOTAXVEAA	Up to 24	1A-6A, 1B-6B, 12A-17A, 12B-17B
OR				

Table 103-A. 18RU Module Complement (cont.)

MODULE/ UNIT DATA SHEET	PART NO.	CLEI	QTY	SLOT
LC7ID 102 1-Port IR OC-48 Line Card, DC-SM-SC (OC48-1P)/ UDS-123	3EM12302AB	WMOTBBHEAA	Up to 24	1A-6A, 1B-6B, 12A-17A, 12B-17B
OR				
LC8D 101 1-Port LR OC-48 Line Card, DC-SM-SC (OC48-1P)/ UDS-123	3EM12312AA	WMOTAXWEAA	Up to 24	1A-6A, 1B-6B, 12A-17A, 12B-17B
OR				
LC8D 102 1-Port LR OC-48 Line Card, DC-SM-SC (OC48-1P)/ UDS-123	3EM12312AB	WMOTBBJEAA	Up to 24	1A-6A, 1B-6B, 12A-17A, 12B-17B
OR				
LC12D 030 1-Port LR OC-192 Line Card, DC-SM-SC, 1553.33 nm (OC192-1P)/ UDS-124	3EM12266AA	WMOTAX3EAA	Up to 4	5AB, 6AB, 12AB, 13AB
OR				
LC12D 031 1-Port LR OC-192 Line Card, DC-SM-SC, 1552.52 nm (OC192-1P)/ UDS-124	3EM12267AA	WMOTAX4EAA	Up to 4	5AB, 6AB, 12AB, 13AB
OR				
LC12D 032 1-Port LR OC-192 Line Card, DC-SM-SC, 1551.72 nm (OC192-1P)/ UDS-124	3EM12268AA	WMI8702FAA	Up to 4	5AB, 6AB, 12AB, 13AB
OR				
LC12D 033 1-Port LR OC-192 Line Card, DC-SM-SC, 1550.92 nm (OC192-1P)/ UDS-124	3EM12269AA	WMI870YFAA	Up to 4	5AB, 6AB, 12AB, 13AB
OR				
LC12D 035 1-Port LR OC-192 Line Card, DC-SM-SC, 1549.32 nm (OC192-1P)/ UDS-124	3EM12270AA	WMI8804FAA	Up to 4	5AB, 6AB, 12AB, 13AB
OR				

Table 103-A. 18RU Module Complement (cont.)

MODULE/ UNIT DATA SHEET	PART NO.	CLEI	QTY	SLOT
LC12D 036 1-Port LR OC-192 Line Card, DC-SM-SC, 1548.51 nm (OC192-1P)/ UDS-124	3EM12271AA	WMI870NFAA	Up to 4	5AB, 6AB, 12AB, 13AB
OR				
LC12D 037 1-Port LR OC-192 Line Card, DC-SM-SC, 1547.72 nm (OC192-1P)/ UDS-124	3EM12272AA	WMI890WFAA	Up to 4	5AB, 6AB, 12AB, 13AB
OR				
LC12D 038 1-Port LR OC-192 Line Card, DC-SM-SC, 1546.92 nm (OC192-1P)/ UDS-124	3EM12273AA	WMI870PFAA	Up to 4	5AB, 6AB, 12AB, 13AB
OR				
TMUX 201 2.5 Gb/s Transmux (TMUX)/ UDS-127	3EM12308AA	WM1DD6YCAA	Up to 4	5A, 6A, 5B, 6B, 12A, 13A, 12B, 13B
OR				
TMUX 301 2.5 Gb/s Transmux (TMUX)/ UDS-127	3EM12308AB	WM1DDCXCAA	Up to 4	5A, 6A, 5B, 6B, 12A, 13A, 12B, 13B
OR				
VSC 101 5 Gb/s VT1.5 Switch Card (VSC)/ UDS-128	3EM12313AA	WMEC60TAAD	Up to 4	5A, 6A, 5B, 6B, 12A, 13A, 12B, 13B
OR				
VSC 101 5 Gb/s VT1.5 Switch Card (VSC)/ UDS-128	3EM12313AB	WMEC606AAA	Up to 4	5A, 6A, 5B, 6B, 12A, 13A, 12B, 13B

FUNCTIONAL OVERVIEW

Modules are either half-height or full-height size (see figure 103-4). Two types of removable card-slot adapters can convert either two adjacent slots or three adjacent slots for half-height module applications. A card-slot adapter to convert one slot is not supported.

Common equipment includes two half-high TCs, two full-high SSCs, and two full-high CCCs. The minimum 18RU shelf configuration that supports transmission is two CCCs, two TCs, two SSCs, and one IOC.

For fault protection, the system modules support redundancy. Redundancy is accomplished by installing a primary module and a secondary module in adjacent slots. During operation the first module to become operational is designated the primary module and the other as the secondary module. The modules remain in these operating states unless a problem with the primary module is detected or a user intentionally changes the module state through software or by activating a module interlock switch manually. If any of these actions occurs, the secondary module will become the primary module, and the old primary module will become the secondary module.

All IOCs are connected to the SSCs through multiple serial telecom busses (STS-12 serial links) running at 777 Mb/s. The serial telecom bus uses 8 B/10 B encoding to bring an STS-12 signal to a rate of 777 Mb/s. The IOCs are all cross-coupled to the working and protection SSCs.

All IOC slots share a common set of four serial telecom bus signals, which together are capable of delivering 48 STS-1s to the SSCs. Eight IOC slots are high-capacity slots, which have four additional serial telecom bus signals that provide 96 STS-1s to the SSC. The common set of four serial telecom bus signals in both the high and low-capacity slots allow IOCs with a capacity of 48 STS-1s to be inserted into any of the slots. Each SSC is connected to all IOCs, so the backplane must provide 128 serial telecom bus links (which represents 512 connections at 777 Mb/s) from each SSC to all IOCs.

The 18RU shelf backplane provides –48V and return distribution to all modules in addition to all signals required for system synchronization and the control system.

Airflow design is integrated into each shelf. The airflow design is a pull system consisting of redundant integrated fans in the individual shelves. Air is pulled from the inlet at the bottom-front of the shelf through the shelf and out the exhaust at the top rear of the shelf.

UDS-104
Power Distribution Unit, Quad Input

PART NUMBER/ MNEMONIC	NAME	CLEI	ECI/ BAR CODE	CPR	STATUS
3EM14200AB PDU-Quad	Power Distribution Unit, Quad Input	NA	NA	NA	Active

FEATURES AND APPLICATION NOTES

- Distributes A1-, A2-, B1-, and B2-battery power that feeds shelves and fans
- Provides fused protection for individual shelves and fans
- Contains front-panel alarm indicators that indicate loss of A1, A2, B1, or B2 power or a blown fuse
- Mounts in any 23-inch unequal-flange earthquake bay and occupies one Electronic Industries Association (EIA) vertical increment

DESCRIPTION

The PDU-Quad provides redundant, fuse-protected connections to each shelf and fan powered within a rack. It provides the interface between multiple battery feeder cables and equipment that is mounted in the rack. See figure 104-1 for an illustration of the PDU-Quad. See figure 104-2 for PDU-Quad dimensions. See figure 104-3 for a typical system application of a PDU-Quad.

Figure 104-1. PDU-Quad

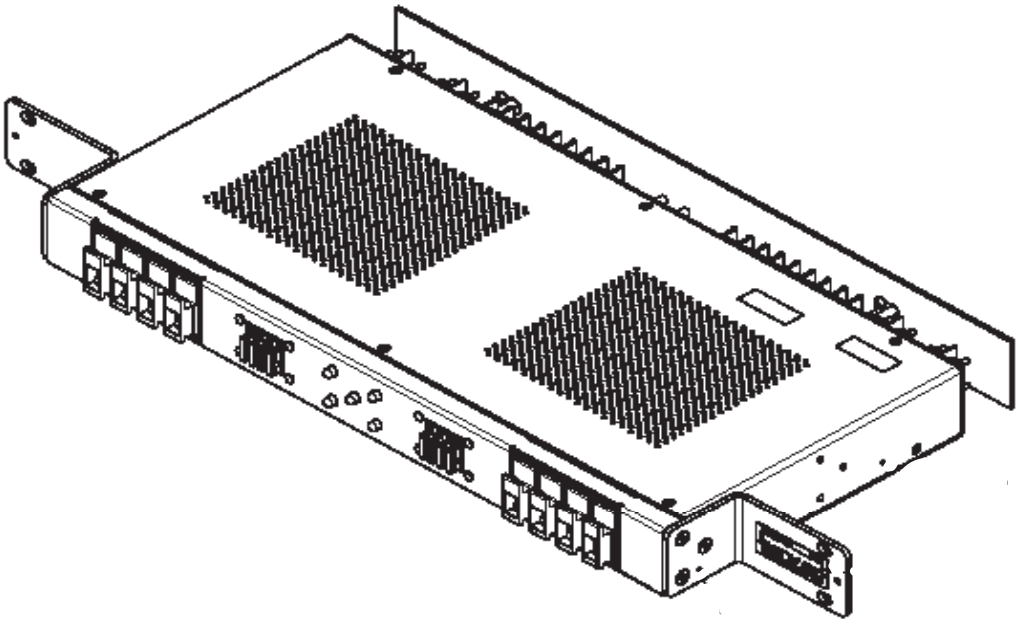

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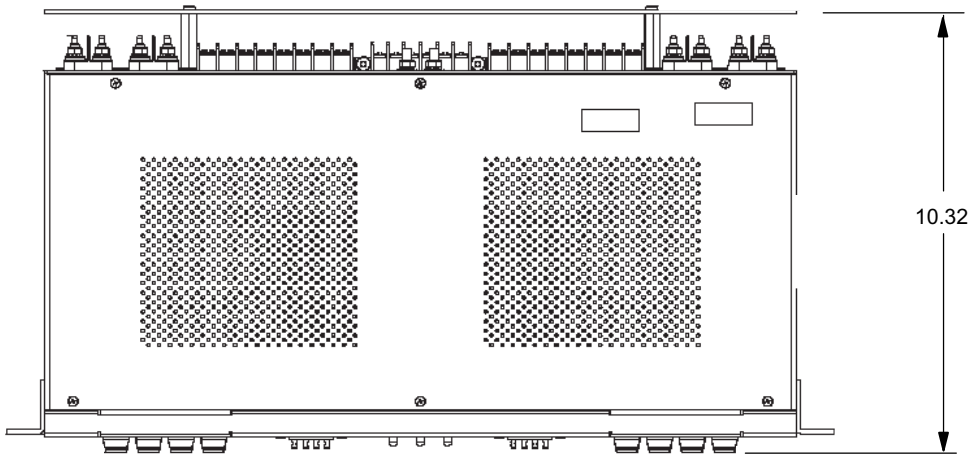
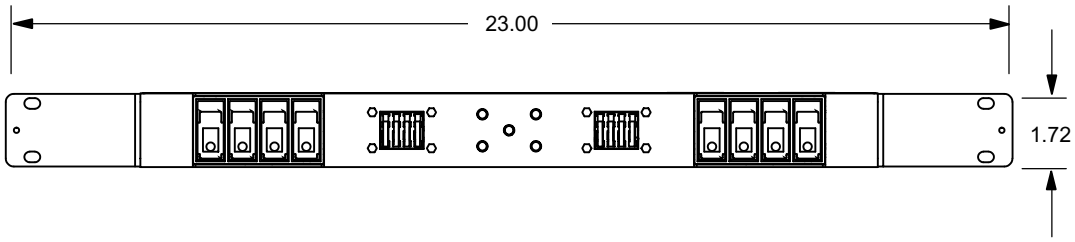
Figure 104-2. PDU-Quad Dimensions



TOP VIEW



FRONT VIEW

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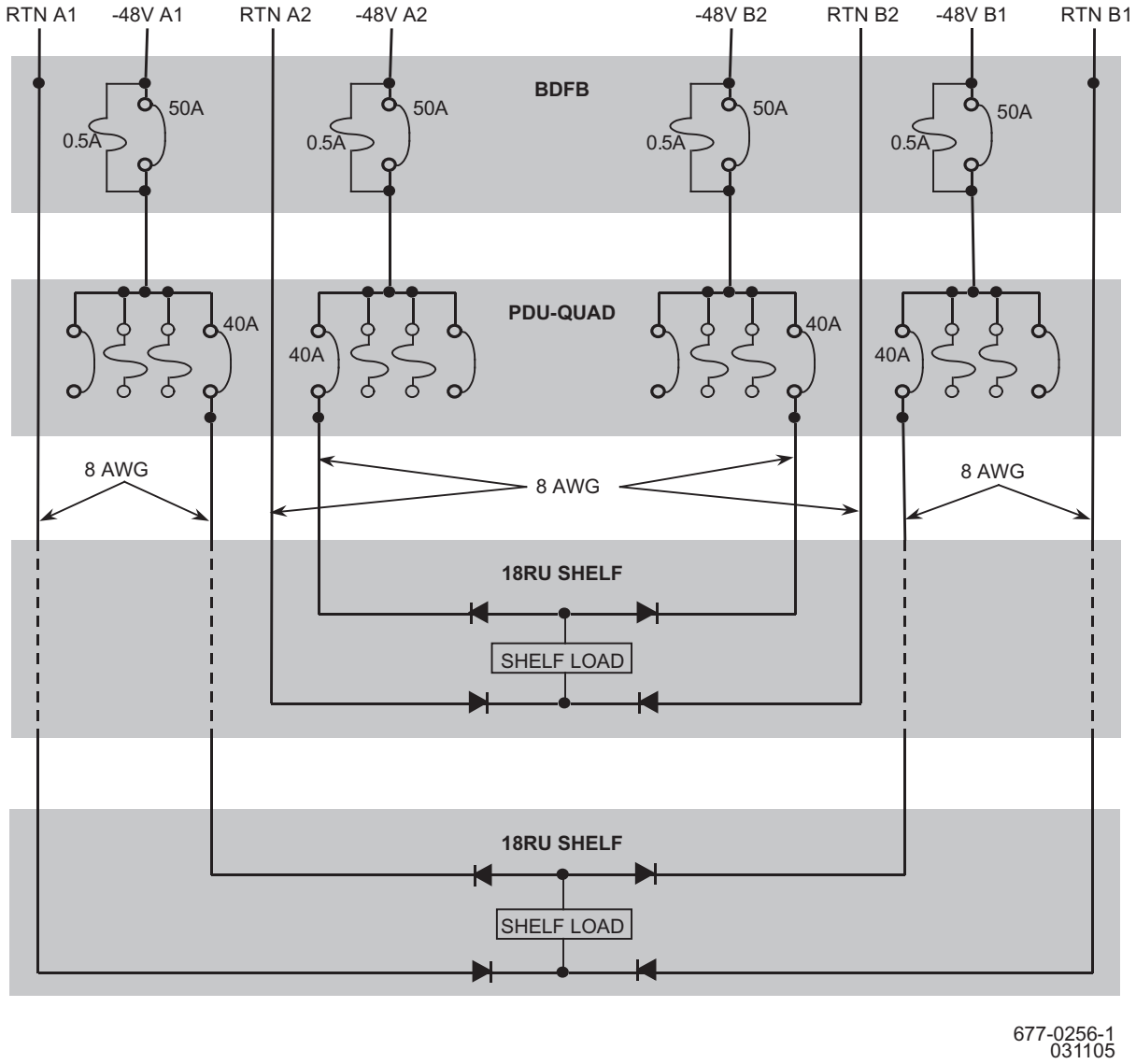
Figure 104-3. PDU-Quad Typical System Application



INDICATORS, CONNECTORS, AND FUSES

The PDU-Quad has the following indicators (see figure 104-4).

ITEM	FUNCTION
A1-1, TPA FUSE	Red indicator lights when fuse A1-1 blows.
A1-2, TPA FUSE	Red indicator lights when fuse A1-2 blows.
A2-1, TPA FUSE	Red indicator lights when fuse A2-1 blows.

ITEM	FUNCTION
A2-2, TPA FUSE	Red indicator lights when fuse A2-2 blows.
B1-1, TPA FUSE	Red indicator lights when fuse B1-1 blows.
B1-2, TPA FUSE	Red indicator lights when fuse B1-2 blows.
B2-1, TPA FUSE	Red indicator lights when fuse B2-1 blows.
B2-2, TPA FUSE	Red indicator lights when fuse B2-2 blows.
A1 POWER	Green indicator lights when A1 input power is present.
A2 POWER	Green indicator lights when A2 input power is present.
B1 POWER	Green indicator lights when B1 input power is present.
B2 POWER	Green indicator lights when B2 input power is present.
FUSE ALARM	Red indicator lights when a fuse alarm is present.

See figures 104-4 and 104-5 for connector and fuse locations on the PDU-Quad.

Figure 104-4. PDU-Quad Connectors and Indicators, Front View

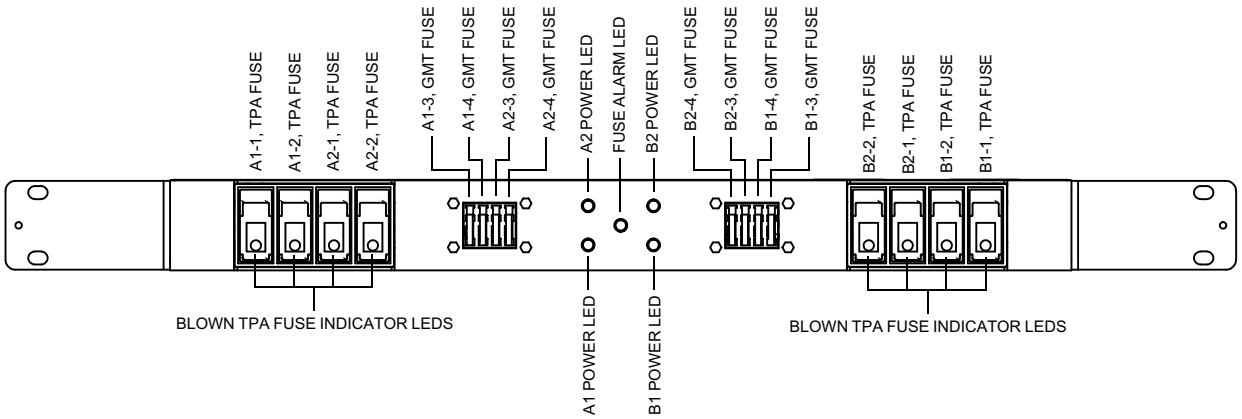
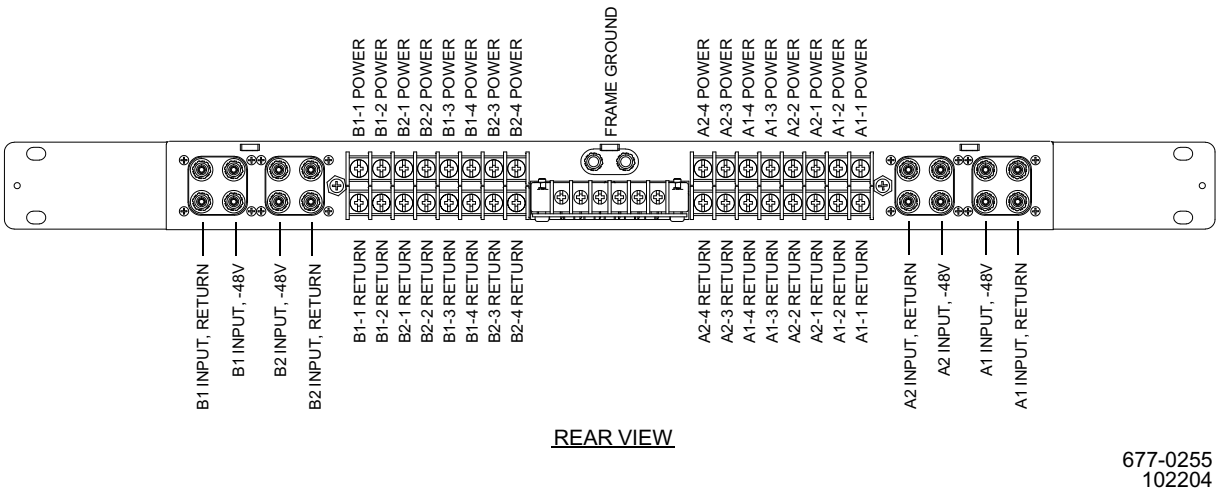


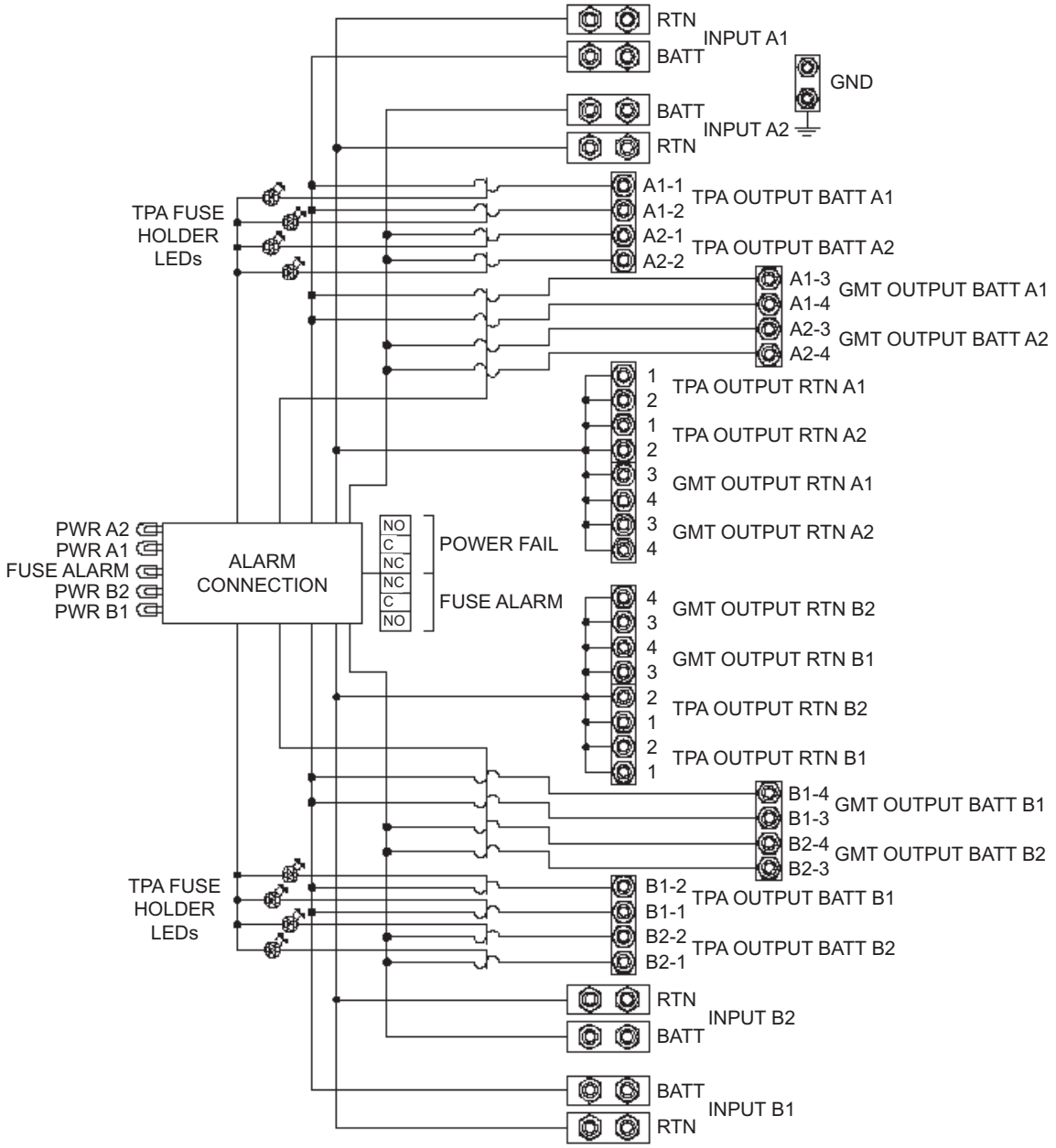
Figure 104-5. PDU-Quad Connectors, Rear View



FUNCTIONAL OVERVIEW

The PDU-Quad accepts four -48 V independent inputs and splits them into 16 separate, fuse-protected outputs. See figure 104-6 for a block diagram of the PDU-Quad. The input power interface consists of four pairs of -48 V (BATT) and RETURN (RTN) connections. These connections are rated at 100 A each. The PDU-Quad splits each -48 V (BATT) connection into four separate output connections, two protected by TPA fuses and two protected by GMT fuses. All fuses are accessible and replaceable from the front panel. The electrical input and output connections are accessible from the rear panel. The PDU-Quad also provides two sets of relay contacts (not used) that signal a fuse failure.

Figure 104-6. PDU-Quad Block Diagram



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UDS-105
15RU 48-Port DS3/EC1 Connector Panel

PART NUMBER/ MNEMONIC	NAME	CLEI	ECI/BAR CODE	CPR	STATUS
3EM12220AA	15RU 48-Port DS3/EC1 Connector Panel	WMM6BB0BRC	443248	203331	Active

FEATURES AND APPLICATION NOTES

- Up to four panels per node
- Front- and/or rear-mountable
- Each panel supports DS3 or ECC modules in a four-quadrant form

DESCRIPTION

Because of the high port-density design of the half-height DS3 and ECC line modules, the modules have no front-panel interface connectors. Instead, network connections are made through separate 48-port DS3/EC1 connector panels that are mounted either on the equipment rack or the rear of the shelf. The panels connect to DS3 or ECC modules through connectors that are accessible at the rear of the shelf once the connector covers are removed.

The system also supports a 96-port rack-mounted BNC connector panel. The customer can either install two 48-port rear-mounted and one 96-port rack-mount or two 96-port rack-mounts to get the full 192 DS3/EC1 ports.

The DS3/EC1 connector panel has 48 pairs of transmit (Tx) and receive (Rx) BNC connectors, providing interface connections for up to four 12-port DS3 or ECC modules. The 1677 SONET Link supports from 1 to 4 connector panels in the following three configurations:

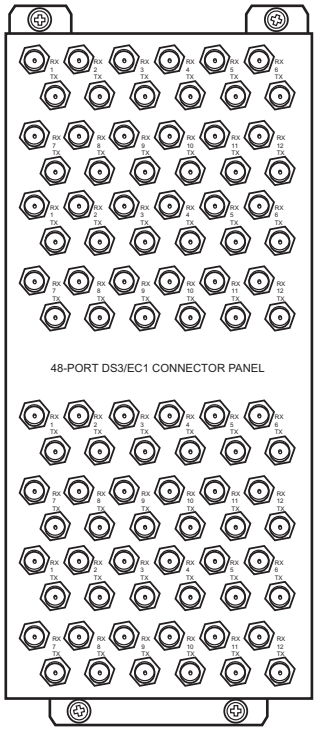
- First and second connector panels attach to the rear of the shelf (for DS3 or ECC modules in slots 1B–5B and 13B–17B), and the third and fourth attach to the rear of the equipment rack (for DS3 or ECC modules in slots 1A–5A and 13A–17A).
- First through fourth connector panels attach to the front of the equipment rack (for DS3 or ECC modules in slots 1B–5B, 13B–17B, 1A–5A, and 13A–17A).
- First and second connector panels attach to the rear of the shelf (for DS3 or ECC modules in slots 1B–5B and 13B–17B) and the third and fourth attach to the front of the equipment rack (for DS3 or ECC modules in slots 1A–5A and 13A–17A).

The chosen configurations depends on the number of connector panels required and the servicing space available.

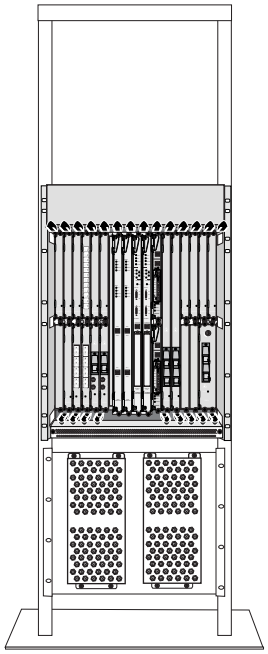
Connector Panel Kits

Each shelf-mounted connector-panel kit contains one 48-port DS3/EC1 connector panel. Each rack-mounted connector-panel kit contains two 48-port DS3/EC1 connector panels, two cables, four cable-tie brackets, a mounting plate, and mounting hardware. A kit to rack-mount one connector panel is not available. For the installation procedure, refer to the 1677 SONET Link Installation Practices manual (PN 3EM13849AF).

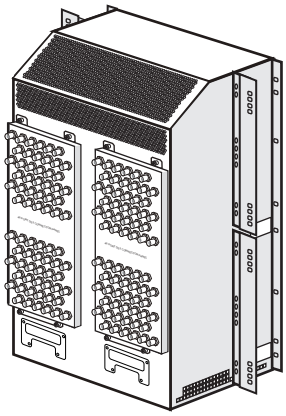
Figure 105-1. 48-Port DS3/EC1 Connector Panel Mounting Options



Up to 4 panels maximum per node



Front Mounted



Rear Mounted

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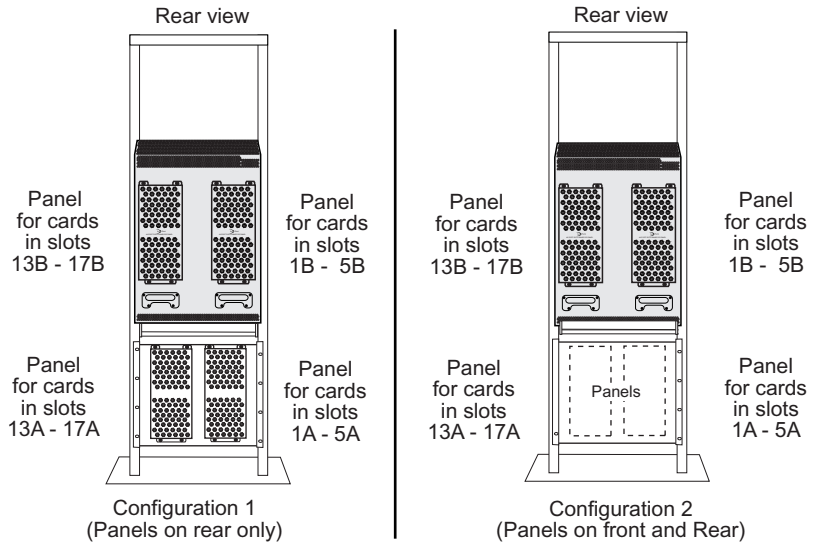
032003

Figure 105-2. 48-Port DS3/EC1 Connector Panel Mounting Configurations



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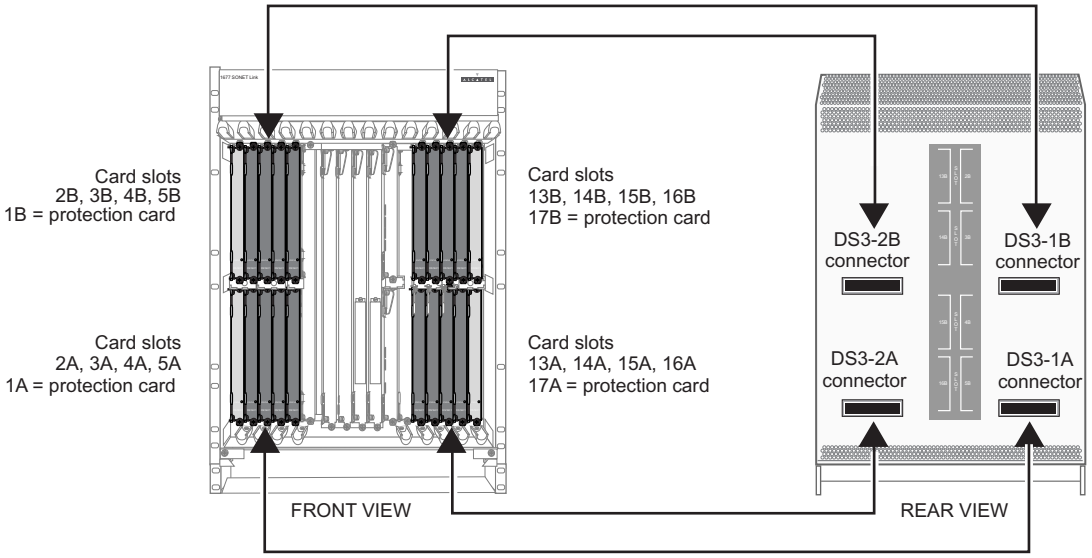
071305

Figure 105-3. Backplane to Front Panel Connections



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032003

UDS-106
15RU 96-Port DS3/EC1 Connector Panel

PART NUMBER/ MNEMONIC	NAME	CLEI	ECI/BAR CODE	CPR	STATUS
3EM12221AA	15RU 96-Port DS3/EC1 Connector Panel	N/A	N/A	N/A	Active

FEATURES AND APPLICATION NOTES

- Up to two panels per node
- Rack mountable
- Each panel supports DS3 or ECC modules in a four quadrant form

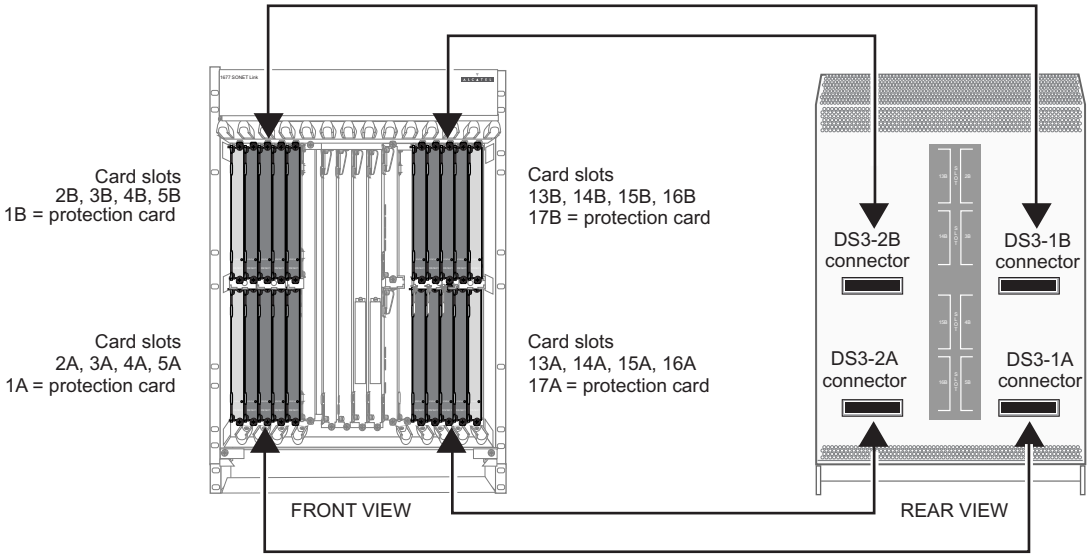
DESCRIPTION

Because of the high port-density design of the half-height DS3 or ECC line modules, the modules have no front-panel interface connectors. Instead, network connections are made through separate 96-port DS3/EC1 connector panels that are mounted on the equipment rack. The panels connect to DS3 or ECC modules through connectors that are accessible at the rear of the shelf once the connector covers are removed. See figure 106-1.

The system supports a 96-port rack-mounted BNC connector panel. The customer can either install two 48-port rear-mounted and one 96-port rack-mount or two 96-port rack-mounts to get the full 192 DS3/EC1 ports.

The DS3/EC1 connector panel has 96 pairs of transmit (Tx) and receive (Rx) BNC connectors, providing interface connections for up to eight 12-port DS3 or ECC modules. The 1677 SONET Link supports from 1 to 2 connector panels, depending on the number of connector panels required and the servicing space available.

Figure 106-1. Backplane to Front Panel Connections



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UDS-107
18RU 48-Port DS3/EC1 Connector Panel

PART NUMBER/ MNEMONIC	NAME	CLEI	ECI/BAR CODE	CPR	STATUS
3EM12329AA	18RU 48-Port DS3/EC1 Connector Panel	N/A	N/A	N/A	Active

FEATURES AND APPLICATION NOTES

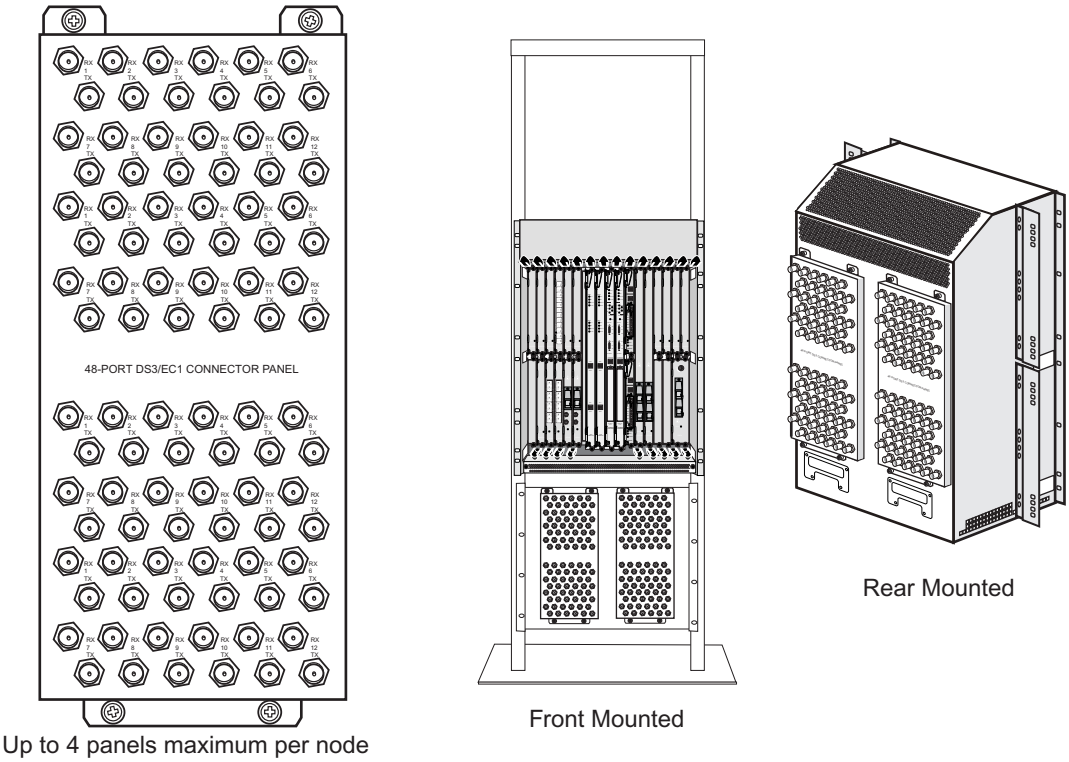
- Up to four panels per node
- Front- and/or rear-mountable
- Each panel supports DS3 or ECC modules in a four-quadrant form

DESCRIPTION

Because of the high port-density design of the half-height DS3 and ECC line modules, the modules have no front-panel interface connectors. Instead, network connections are made through separate 48-port DS3/EC1 connector panels that are mounted either on the equipment rack or the rear of the shelf. See figures 107-1 and 107-2. The panels connect to DS3 or ECC modules through connectors that are accessible at the rear of the shelf once the connector covers are removed. See figure 107-3.

The system also supports a 96-port rack-mounted BNC connector panel. The customer can either install two 48-port rear-mounted and one 96-port rack-mount or two 96-port rack-mounts to get the full 192 DS3/EC1 ports.

Figure 107-1. 48-Port DS3/EC1 Connector Panel Mounting Options



The DS3/EC1 connector panel has 48 pairs of transmit (Tx) and receive (Rx) BNC connectors, providing interface connections for up to four 12-port DS3 or ECC modules. The 1677 SONET Link supports from 1 to 4 connector panels in the following two configurations:

- First and second connector panels attach to the rear of the shelf (for DS3 or ECC modules in slots 1B–5B and 13B–17B), and the third and fourth attach to the rear of the equipment rack (for DS3 or ECC modules in slots 1A–5A and 13A–17A).
- First and second connector panels attach to the rear of the shelf (for DS3 or ECC modules in slots 1B–5B and 13B–17B) and the third and fourth attach to the front of the equipment rack (for DS3 or ECC modules in slots 1A–5A and 13A–17A).

The chosen configurations depends on the number of connector panels required and the servicing space available.

Figure 107-2. 48-Port DS3/EC1 Connector Panel Mounting Configurations

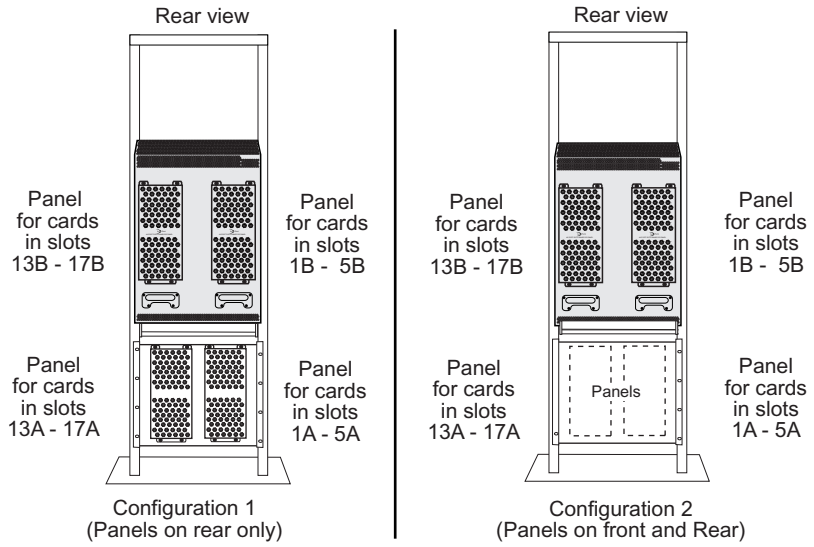


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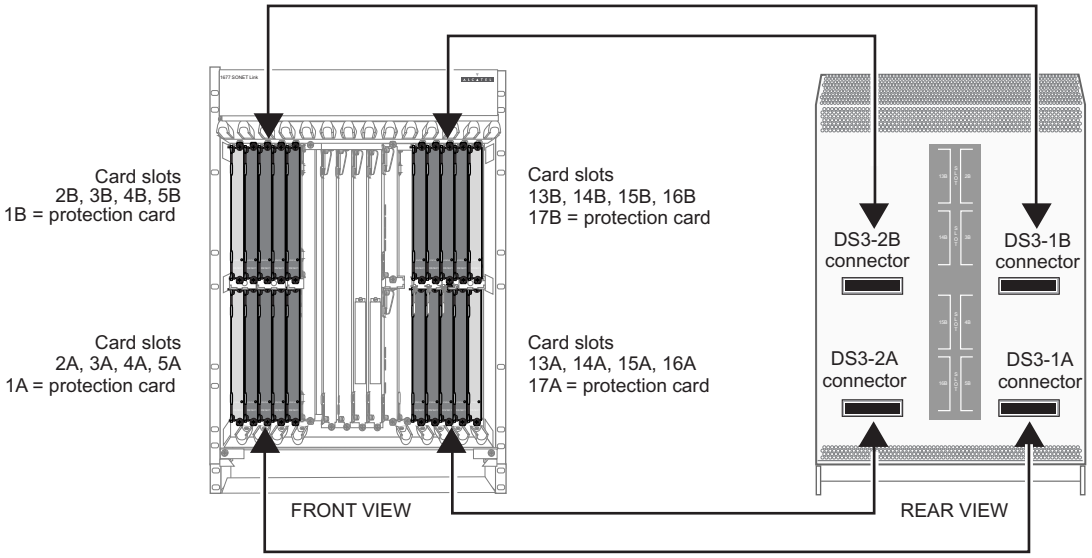
Figure 107-3. Backplane to Front Panel Connections



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Connector Panel Kits

Each shelf-mounted connector-panel kit contains one 48-port DS3/EC1 connector panel. Each rack-mounted connector-panel kit contains two 48-port DS3/EC1 connector panels, two cables, four cable-tie brackets, a mounting plate, and mounting hardware. A kit to rack-mount one connector panel is not available. For the installation procedure, refer to the 1677 SONET Link Installation Practices manual (PN 3EM13849AF).

UDS-108
18RU 96-Port DS3/EC1 Connector Panel

PART NUMBER/ MNEMONIC	NAME	CLEI	ECI/BAR CODE	CPR	STATUS
3EM12330AA	18RU 96-Port DS3/EC1 Connector Panel	N/A	N/A	N/A	Active

FEATURES AND APPLICATION NOTES

- Up to two panels per node
- Rack mountable
- Each panel supports DS3 or ECC modules in a four quadrant form

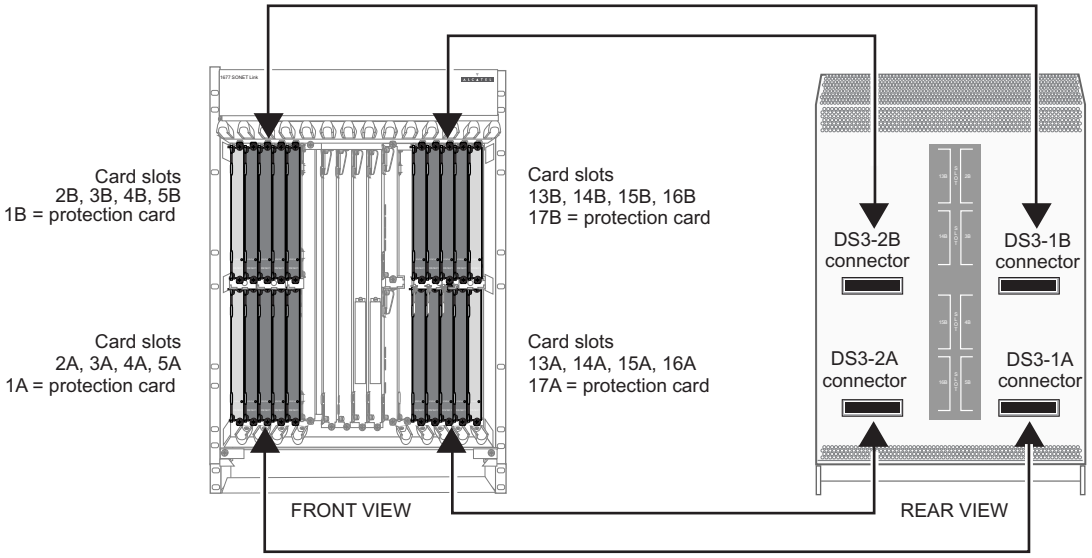
DESCRIPTION

Because of the high port-density design of the half-height DS3 or ECC line modules, the modules have no front-panel interface connectors. Instead, network connections are made through separate 96-port DS3/EC1 connector panels that are mounted on the equipment rack. The panels connect to DS3 or ECC modules through connectors that are accessible at the rear of the shelf once the connector covers are removed. See figure 108-1.

The system supports a 96-port rack-mounted BNC connector panel. The customer can either install two 48-port rear-mounted and one 96-port rack-mount or two 96-port rack-mounts to get the full 192 DS3/EC1 ports.

The DS3/EC1 connector panel has 96 pairs of transmit (Tx) and receive (Rx) BNC connectors, providing interface connections for up to eight 12-port DS3 or ECC modules. The 1677 SONET Link supports from 1 to 2 connector panels, depending on the number of connector panels required and the servicing space available.

Figure 108-1. Backplane to Front Panel Connections



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UDS-109
15RU Fan Tray

PART NUMBER/ MNEMONIC	NAME	CLEI	ECI/BAR CODE	CPR	STATUS
3EM12279AA	15RU Fan Tray	WMPQAGSPAC	113636	E73332	Active

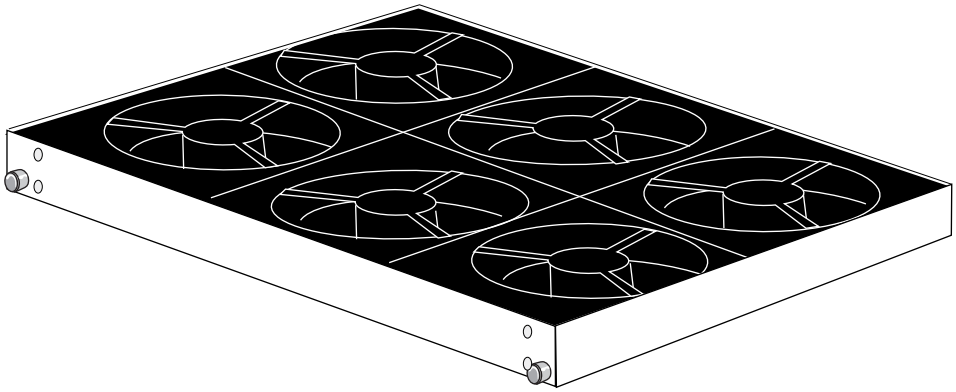
FEATURES AND APPLICATION NOTES

- Provides *n*+1 fan protection
- Self-contained fan controller continuously monitors fan operation
- Front-panel light indicates fan failure
- Designed for quick in-service replacement

DESCRIPTION

The removable fan tray contains six multi-speed fans and a fan-controller module. See figure 109-1. The six fans provide *n* +1 protection preventing the 1677 SONET Link from overheating if one of the fans fails. The fan-controller monitors the rotational speed of each fan. When all fans are rotating at the correct speed, the Fan light, located on the Common Control Card (CCC), lights green to indicate proper functionality. If one fan fails, another fan speeds up to provide more air flow. The Fan light on the CCC lights amber to indicate the fan tray must be replaced within 72 hours to maintain *n*+1 protection. If two or more fans fail, the Fan light on the CCC lights red, and the fan tray must be replaced immediately to prevent the node from overheating. Room temperature and the number of modules installed in the system determines how long the system will run without a fan.

Figure 109-1. Fan Tray



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UDS-110
18RU Fan Tray

PART NUMBER/ MNEMONIC	NAME	CLEI	ECI/ BAR CODE	CPR	STATUS
3EM12307AA FAN	18RU Fan Tray	NA	NA	NA	Active

FEATURES AND APPLICATION NOTES

- Provides forced airflow to cool equipment in an 18RU shelf
- Allows for hot insertion/removal of the fan tray in the event of a failure
- Contains sensors that determine if fan speed is too slow or stopped
- Has redundant input power feeds such that failure of any single fan does not disable any other fan
- Housed in an 18RU shelf

DESCRIPTION

The 18RU shelf uses forced-air cooling provided by a removable fan tray. The fan tray is located at the top of the 18RU shelf and draws ambient air into the 18RU shelf through the air plenum located under the 18RU shelf and through the bottom front and sides of the 18RU shelf. The air passes through a high dust arresting polyurethane air filter (PN 3EM12278AA) and over the surfaces of the modules. The heated air exits the top of the 18RU shelf at the rear.

The fan tray contains six multi-speed Air Movement Units (AMUs). The six AMUs provide 1:N protection. This prevents the 18RU shelf from overheating if one of the AMUs fails.

Four captive thumbscrews fasten the fan tray to the 18RU shelf. See figures 110-1 through 110-3.

Figure 110-1. Fan Tray

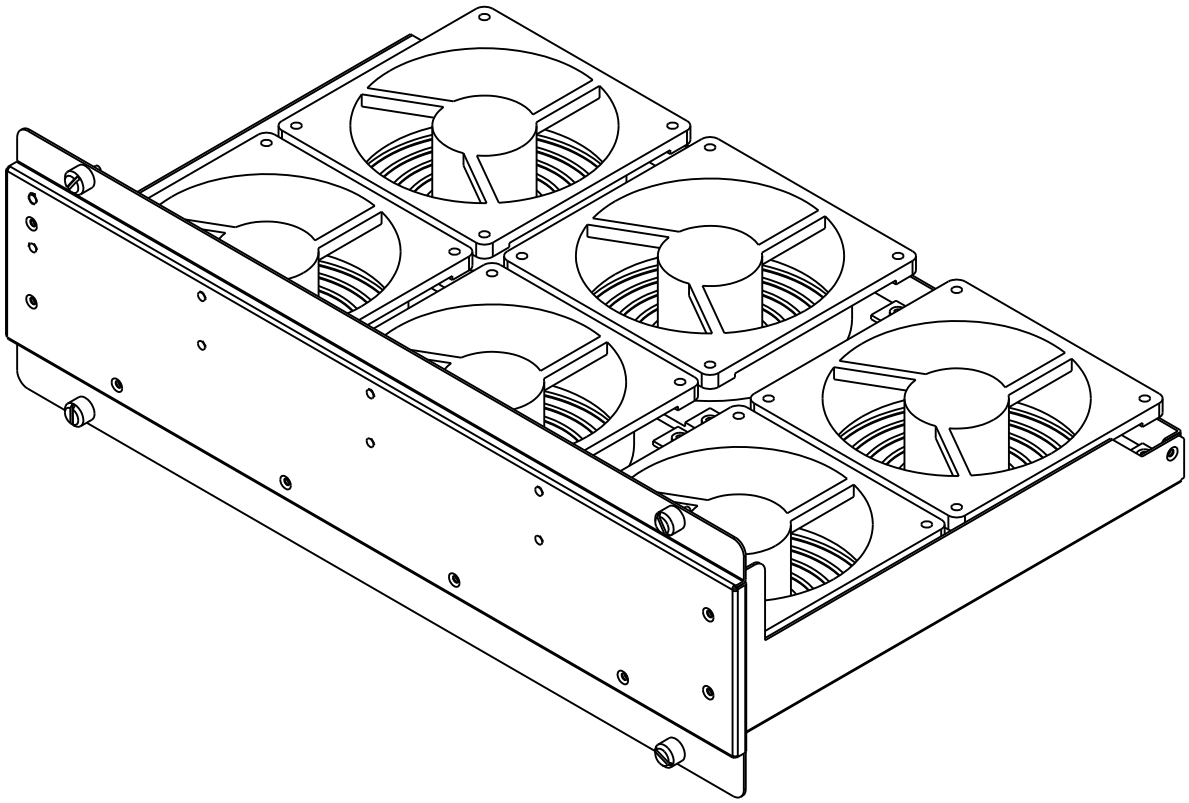

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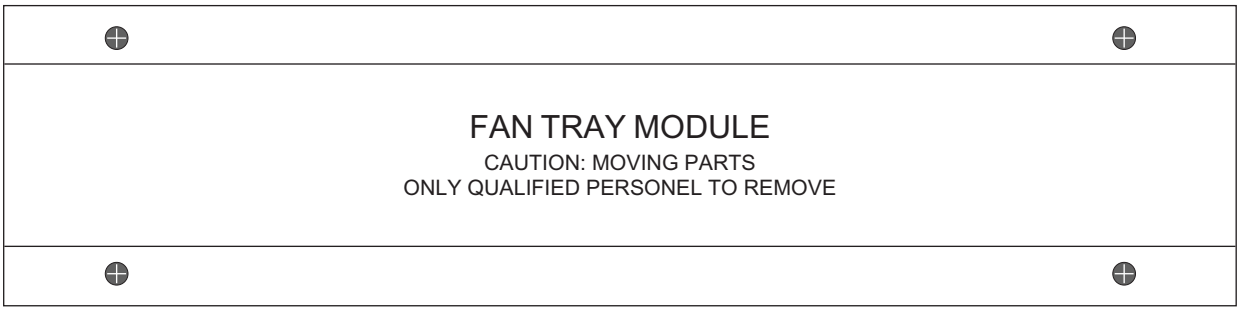
Figure 110-2. Fan Tray Front Panel (Front View)



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110904

Figure 110-3. Fan Tray Front Panel Connectors (Rear View)

CONNECTORS

The fan tray has the following connectors:

ITEM	FUNCTION
J1	4-pin connector for AMU 3 power, control, and fan speed detection. Refer to table 110-A.
J2	4-pin connector for AMU 2 power, control, and fan speed detection. Refer to table 110-B.
J3	4-pin connector for AMU 1 power, control, and fan speed detection. Refer to table 110-C.
J4	10-pin connector for fan tray A power and control. Refer to table 110-D.
J5	4-pin connector for AMU 6 power, control, and fan speed detection. Refer to table 110-E.
J6	4-pin connector for AMU 5 power, control, and fan speed detection. Refer to table 110-F.
J7	4-pin connector for AMU 4 power, control, and fan speed detection. Refer to table 110-G.
J8	10-pin connector for fan tray B power and control. Refer to table 110-H.

Table 110-A. Fan Tray, J1 Pinout Assignments

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	AMU 3 V+	2	AMU 3 V-	3	AMU 3 CONTROL	4	AMU 3 TACHOMETER

Table 110-B. Fan Tray, J2 Pinout Assignments

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	AMU 2 V+	2	AMU 2 V-	3	AMU 2 CONTROL	4	AMU 2 TACHOMETER

Table 110-C. Fan Tray, J3 Pinout Assignments

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	AMU 1 V+	2	AMU 1 V-	3	AMU 1 CONTROL	4	AMU 1 TACHOMETER

Table 110-D. Fan Tray, J4 Pinout Assignments

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	MAIN 48 V PRI PWR	2	MAIN 48 V PRI PWR	3	MAIN 48 V PRI PWR RTN	4	MAIN 48 V PRI PWR RTN
5	GND	6	GND	7	I2C CCC A SERIAL DATA	8	I2C CCC A SERIAL CLOCK
9	I2C CCC B SERIAL DATA	10	I2C CCC B SERIAL CLOCK				

Table 110-E. Fan Tray, J5 Pinout Assignments

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	AMU 6 V+	2	AMU 6 V-	3	AMU 6 CONTROL	4	AMU 6 TACHOMETER

Table 110-F. Fan Tray, J6 Pinout Assignments

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	AMU 5 V+	2	AMU 5 V-	3	AMU 5 CONTROL	4	AMU 5 TACHOMETER

Table 110-G. Fan Tray, J7 Pinout Assignments

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	AMU 4 V+	2	AMU 4 V-	3	AMU 4 CONTROL	4	AMU 4 TACHOMETER

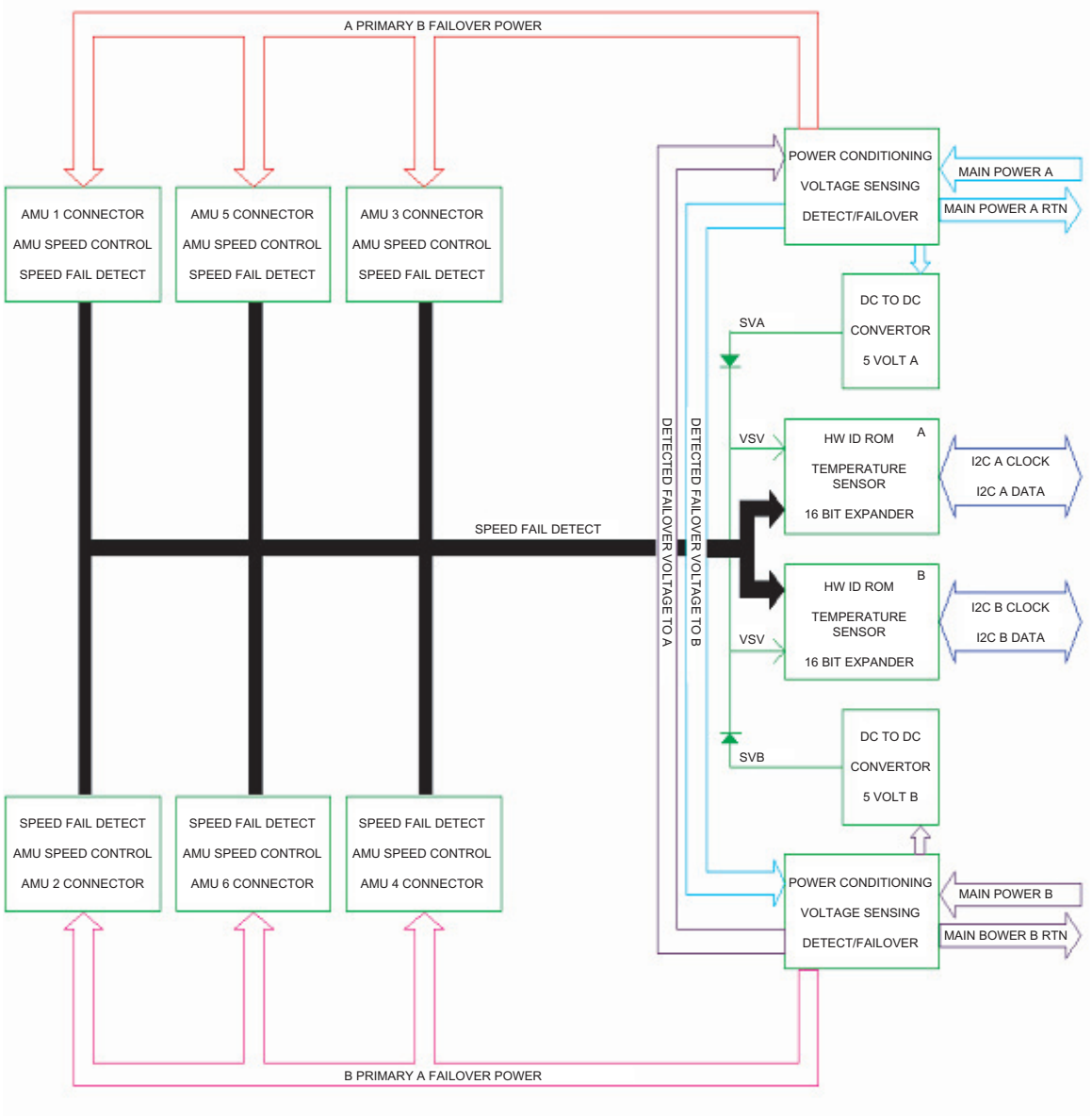
Table 110-H. Fan Tray, J8 Pinout Assignments

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	MAIN 48 V SEC PWR	2	MAIN 48 V SEC PWR	3	MAIN 48 V SEC PWR RTN	4	MAIN 48 V SEC PWR RTN
5	GND	6	GND	7	I2C CCC A SERIAL DATA	8	I2C CCC A SERIAL CLOCK
9	I2C CCCB SERIAL DATA	10	I2C CCC B SERIAL CLOCK				

FUNCTIONAL OVERVIEW

The fan tray is comprised of six AMUs and a fan controller board. See figure 110-4 for a simplified block diagram of the fan tray.

Figure 110-4. Fan Tray Simplified Block Diagram



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110904

Fan Controller Board

The fan controller board is a power conditioner, fan alarm generator, fan speed controller, and thermometer with presence on the I2C bus. It provides the following:

- Filtered 48 V to the six AMUs in the fan tray
- Soft-start circuitry on the 48 V to facilitate hot-swap
- Temperature monitoring through a temperature sensor over the I2C bus
- A monitor of the tachometer pulses from each of the fans (When the fan speed is low, an alarm signal is sent over the I2C bus.)
- Isolation from the 48 V power for the I2C circuitry using opto-isolators and redundant 48 V-to-5 V DC-to-DC converters
- Split power feed (Under normal operation, the A feed powers fans 1, 5, and 3 and one of the dc-dc converters, and the B feeds powers fans 4, 2, and 6 and the other dc-dc converter.)
- Failover when one of the feeds is offline (The voltage detection and failover circuitry powers the fan tray from the remaining single feed.)
- Return to equal current draw when feed is brought back online (The fan tray reverts to normal operation, and the power for the fan tray is drawn equally through both A and B feeds.)

The fan controller board monitors the rotational speed of each fan. When all fans are rotating at the correct speed, the FAN LED on the CCC 102 Common Control Card (CCC) is green, indicating normal operation. If one AMU fails, another fan speeds up to provide more air flow and the FAN LED turns amber, indicating that fan tray has experienced a failure and should be replaced. If two AMUs fail, the FAN LED turns red, indicating that fan tray should be replaced immediately.

All system communication for the fan tray is handled through the CCC over the I2C bus.

Power

The fan tray operates from two redundant DC power sources. Power is distributed from the backplane over a cable to the fan control board and the AMUs. The fan tray operates normally and does not sustain damage if either source is turned off or degrades below -37.5 V dc. The two input DC sources are electrically isolated from one another; this includes separate battery and battery return. Internal failure protection is provided by means of input fuses. The unit provides alarm to the shelf through the I2C bus.

The six AMUs are divided into two groups of three. Each group uses one of the inputs, A or B, as its primary power source. Although each AMU group uses the primary source, in case of primary source voltage drop to a certain level, the AMUs switch to the secondary source so the fan operation is not affected as a result of one power input failure.

The fan tray has redundant 48 V soft-start circuits and independent 48 V A and B power detection/failover circuits. Output voltages to the AMUs are filtered and fused.

Redundancy

The fan tray has the following redundant components:

- Dual 48 V input power detection and soft start circuitry
- Dual 48 V-to-5 V DC-to-DC converters
- Dual I2C serial ID ROM
- Dual I2C I/O controller
- Dual I2C temperature sensors

UDS-111
DS1 Splitter

PART NUMBER/ MNEMONIC	NAME	CLEI	ECI/ BAR CODE	CPR	STATUS
3EM14189AD	DS1 Splitter, Shelf 1	NA	NA	NA	Active
3EM14189AE	DS1 Splitter, Shelf 2	NA	NA	NA	Active

FEATURES AND APPLICATION NOTES

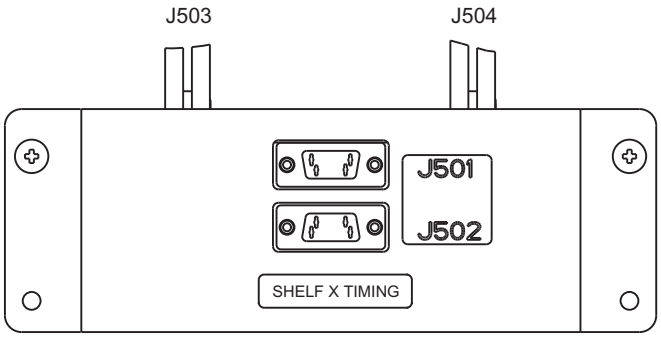
- Divides two external DS1 timing reference signals (primary and secondary) from a BITS clock into four timing reference outputs

DESCRIPTION

The external timing reference source enters the system through two DS1 splitters. One DS1 splitter serves the 18RU shelf 1, and the other serves the 18RU shelf 2. Each DS1 splitter receives two external DS1 timing reference signals (primary and secondary) from a BITS clock and divides the inputs into four timing reference outputs, designated as primary copy 0, primary copy 1, secondary copy 0, and secondary copy 1. These outputs then go to TCs in the 18RU shelves. See figure 111-1 for an outline of the DS1 splitter. See figure 111-2 for the typical system application of the DS1 splitter.

Both DS1 splitters are mounted at the bottom of the rack.

Figure 111-1. DS1 Splitter



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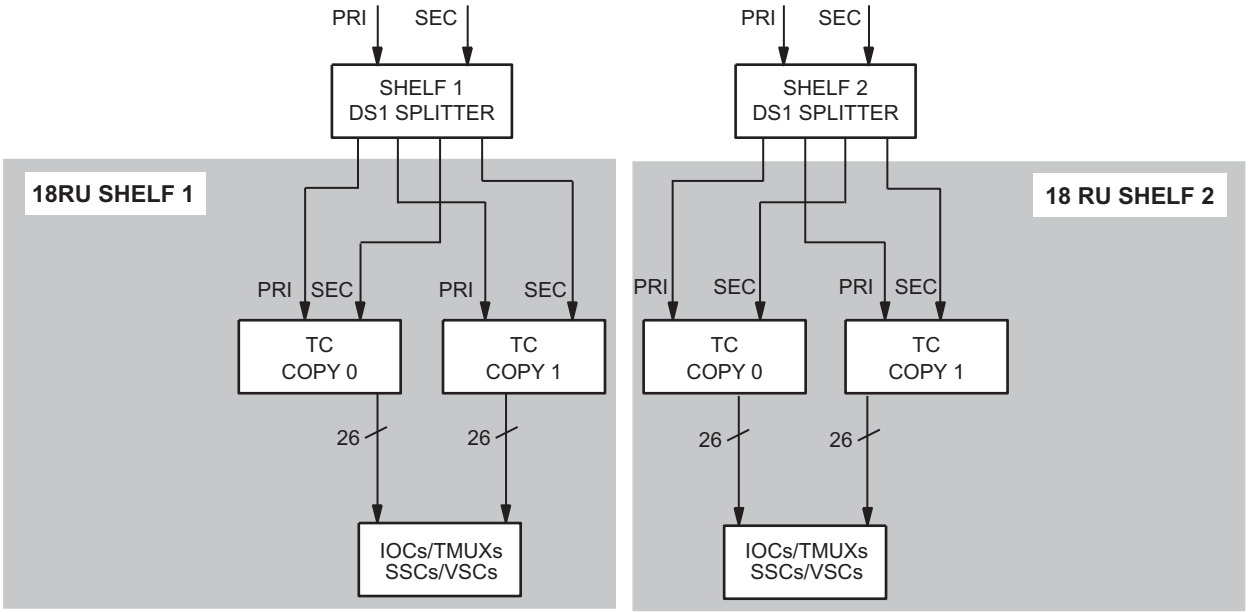
102204

Figure 111-2. DS1 Splitter Typical System Application



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102204

CONNECTORS

The DS1 splitter has the following connectors (see figure 111-1):

ITEM	FUNCTION
J501	9-pin primary DS1 clock reference connector. Refer to table 111-A (NC indicates not connected).
J502	9-pin secondary DS1 clock reference connector. Refer to table 111-B (NC indicates not connected).
J503	6-pin secondary DS1 clock reference output. Refer to table 111-C. (Used only when DS1 reference is required.)
J504	6-pin primary 0 DS1 clock reference output. Refer to table 111-C. (Used only when DS1 reference is required.)

Table 111-A. J501 DS1 Clock Reference (Copy 0) Connector Pinout Assignments

PINPIN	SIGNALsignal	PINPIN	SIGNALsignal	PINPIN	SIGNALsignal	PINPIN	SIGNALsignal
001	NC	002	NC	003	NC	004	NC
005	NC	006	NC	007	NC	008	BIT_CK_C0_T
009	BIT_CK_C0_F						

Table 111-B. J502 DS1 Clock Reference (Copy 1) Connector Pinout Assignments

PINPIN	SIGNALsignal	PINPIN	SIGNALsignal	PINPIN	SIGNALsignal	PINPIN	SIGNALsignal
001	NC	002	NC	003	NC	004	NC
005	NC	006	NC	007	NC	008	BIT_CK_C1_T
009	BIT_CK_C1_F						

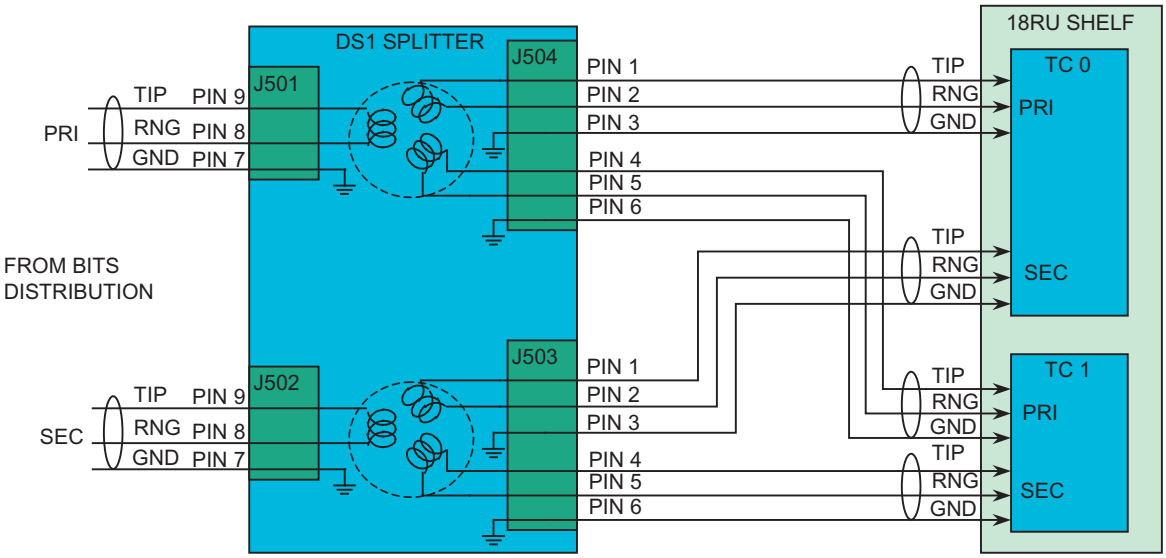
Table 111-C. J503/J504 Clock Reference Output Pinout Assignments

PINPIN	SIGNALsignal	PINPIN	SIGNALsignal	PINPIN	SIGNALsignal	PINPIN	SIGNALsignal
1	TIP	2	RING	3	SIGNAL GND	4	TIP
5	RING	6	SIGNAL GND				

FUNCTIONAL OVERVIEW

The DS1 splitters shelf reduce the total number of BITS facilities required by each 18RU shelf from two primary and two secondary facilities to one primary and one secondary facility. See figure 111-3 for a simplified block diagram of the DS1 splitter.

Figure 111-3. DS1 Splitter Simplified Block Diagram



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The DS1 splitter terminates an external clock reference. The external clock reference is a 1.544 MHz DS1 BITS that is used as either primary or secondary source input to the DS1 splitter. One DS1 splitter receives the primary source input, while the other DS1 splitter receives the secondary source input. Each splitter mounts at the bottom of the rack. The DS1 splitter divides each input and distributes one input to each TC in an 18RU shelf.

Inputs to the DS1 splitter are received through connectors J501 and J502. Connector J501 (primary input) provides copy 0 and copy 1 outputs through connector J504. The copy 0 output is cabled to the copy 0 TC, and the copy 1 output is cabled to the copy 1 TC. Connector J502 (secondary input) provides copy 0 and copy 1 outputs through connector J503. Typically, the primary BITS input is cabled to the shelf 1 DS1 splitter, and the secondary BITS input is cabled to the shelf 2 DS1 splitter.

UDS-112
ADME/W 01x E/F-Band East/West Add/Drop Module

PART NUMBER/ MNEMONIC	NAME	CLEI	ECI/ BAR CODE	CPR	STATUS
3EM12215AA ADM	ADME 013 E-Band East Add/Drop Module	WMM9W02JRB	443251	205280	Active
3EM12216AA ADM	ADMW 013 E-Band West Add/Drop Module	WMM9W03JRB	443252	205281	Active
3EM12217AA ADM	ADME 014 F-Band East Add/Drop Module	WMM9W04JRB	443253	205282	Active
3EM12218AA ADM	ADMW 014 F-Band West Add/Drop Module	WMM9W05JRB	443254	205283	Active

FEATURES AND APPLICATION NOTES

- Installs directly into ANSI rack in a stacked architecture
- East and West ADMs provide add/drop functions in both directions around the ring
- 12 add/drop ports
- 2 of each 6 ports are used for Network In/Out and Express In/Out

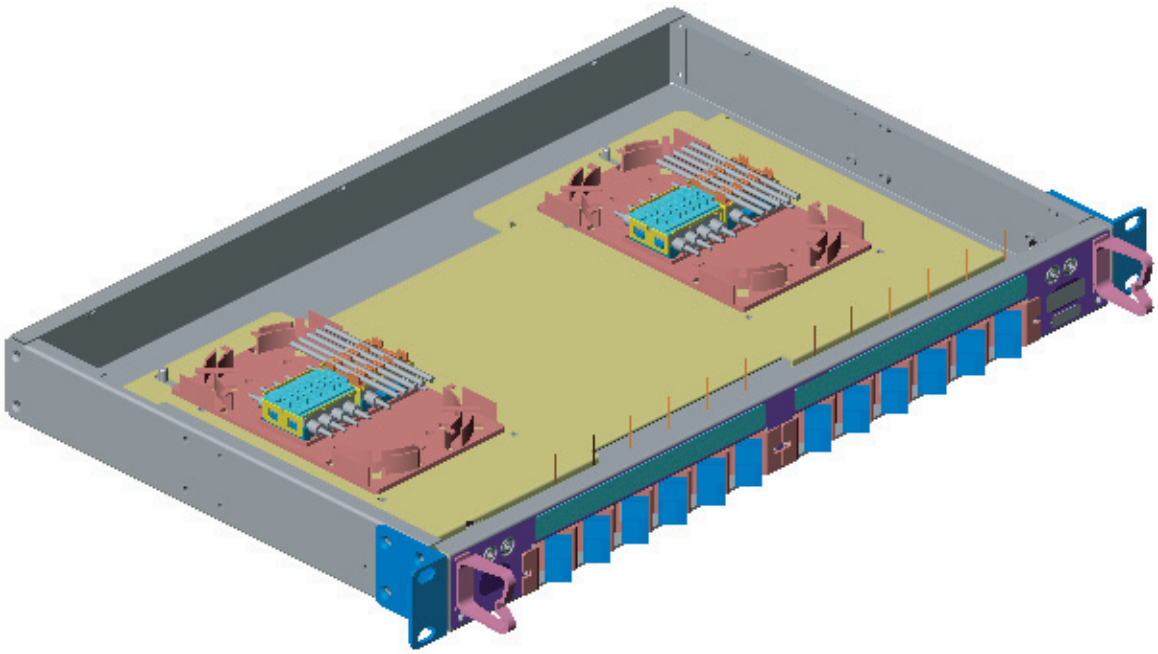
DESCRIPTION

The Modular Optical System uses the ADM to sort light on network fibers. ADMs contain optical components that add or drop light from the network fiber. Each add or drop requires its own front-panel port for light to enter or exit the 1677 SONET Link shelf.

The ADM is available in both an East and West version. It has 12 front-panel ports, six for drop functions and six for add functions. The left six ports are used for drop (East module) functions or add (West module) functions, and the right six ports are used for add (East module) functions and drop (West module) functions. Two of each of the six ports are used for the Network In/Out and the Express In/Out ports.

Two optical component trays are mounted on the universal tray inside the ADM. Each tray holds the optical components for either the drop or add light paths. The optical component trays are mounted on the right and left sides of the universal tray depending on if the ADM is being used as an East or West module. For East modules, optical trays are mounted to the right. For West modules, optical trays are mounted to the left. See figure 112-1. All terminated fibers have an internal service loop before the termination.

Figure 112-1. ADM Hardware Design



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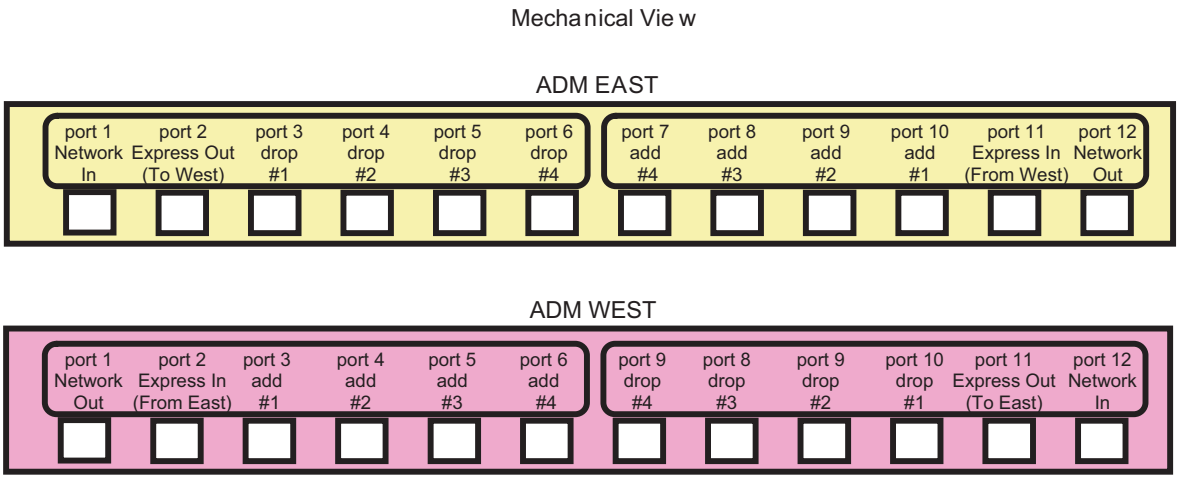
INDICATORS AND CONNECTORS

Figure 112-2 describes the ADM front panel indicators and connectors.

Figure 112-2. ADM Front Panel



function	add label	drop label
monitor	monitor	monitor
1310	1310 add	1310 drop
	1510 add	1510 drop
band	A add	A drop
	B add	B drop
	C add	C drop
	D add	D drop
	E add	E drop
	F add	F drop
	G add	G drop
	H add	H drop

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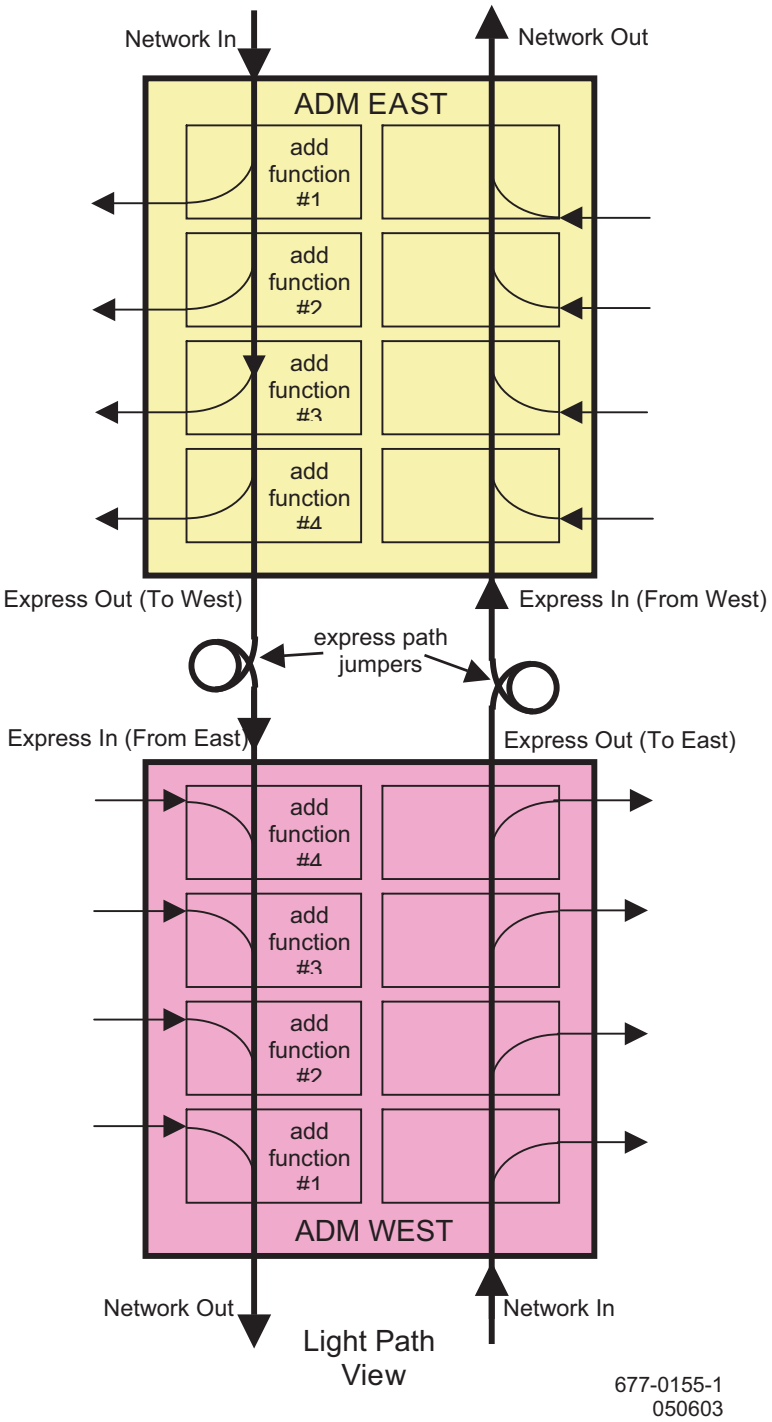
050603

FUNCTIONAL OPERATION

Each add or drop is considered an ADM function. The ADM is comprised of reliable, optical components that require no power. Such components are a monitoring block, a 1310 nm block, and band component block, where wavelengths in bands E and F are supported. To minimize optical loss of the network traffic passing through the node, all components are spliced together. Figure 112-3 illustrates an example of the ADM functionality.

Figure 112-3. ADM Functionality



UDS-113
CCC 101/104 Common Control Card

PART NUMBER/ MNEMONIC	NAME	CLEI	ECI/ BAR CODE	CPR	STATUS
3EM12219AA CCC	CCC 101 Common Control Card	WM3C20LJAE	124898	E73529	Inactive
3EM12219AB CCC	CCC 104 Common Control Card	WMUCAJDBAA	127938	W70111	Active

FEATURES AND APPLICATION NOTES

- Full-height, installed in slots 9 and10
- Flash disk subsystem
- Audible and visual alarms
- 50 Mhz system clock (used by all modules in the system)
- Synchronization (used by all modules in the system)
- CCC 104 has the following enhancements:
  - Improved 48 V over/under power performance
  - Improved power efficiency
  - Improved signal integrity
  - Protected/monitored power to backplane
  - Enhanced lever (most recent manufacturing revision)

DESCRIPTION

The CCC is the main processing power in the node. It controls communication between the Input/Output Cards (IOCs), the STS Switch Cards (SSCs), and the Timing Card (TC), and records and controls node events, including configuration events, monitoring events, and alarm events. The CCC also provides the visual and physical interface for alarms.

The flash disk subsystem is comprised of two logical drives, Dives A and B, where all “writes to” and “reads from” the drives within the system are made to logical Drives A and B. Logical Drive A and Logical Drive B each contain two physical flash disks, A9 and A10 and B9 and B10. A9/B9 resides on CCC-9 and A10/B10 resides on CCC-10. One of the physical drives is the primary drive and the other is the secondary drive. The system is responsible for ensuring all information written to the primary drive is also written to the secondary drive to keep the two disks in sync. Therefore, if either a physical disk fails, a CCC fails, a physical disk is deactivated, or a CCC is deactivated, the logical drive information will still function properly. When a CCC is installed with disks, the disks on that CCC should be activated as secondary if a primary disks are already present.

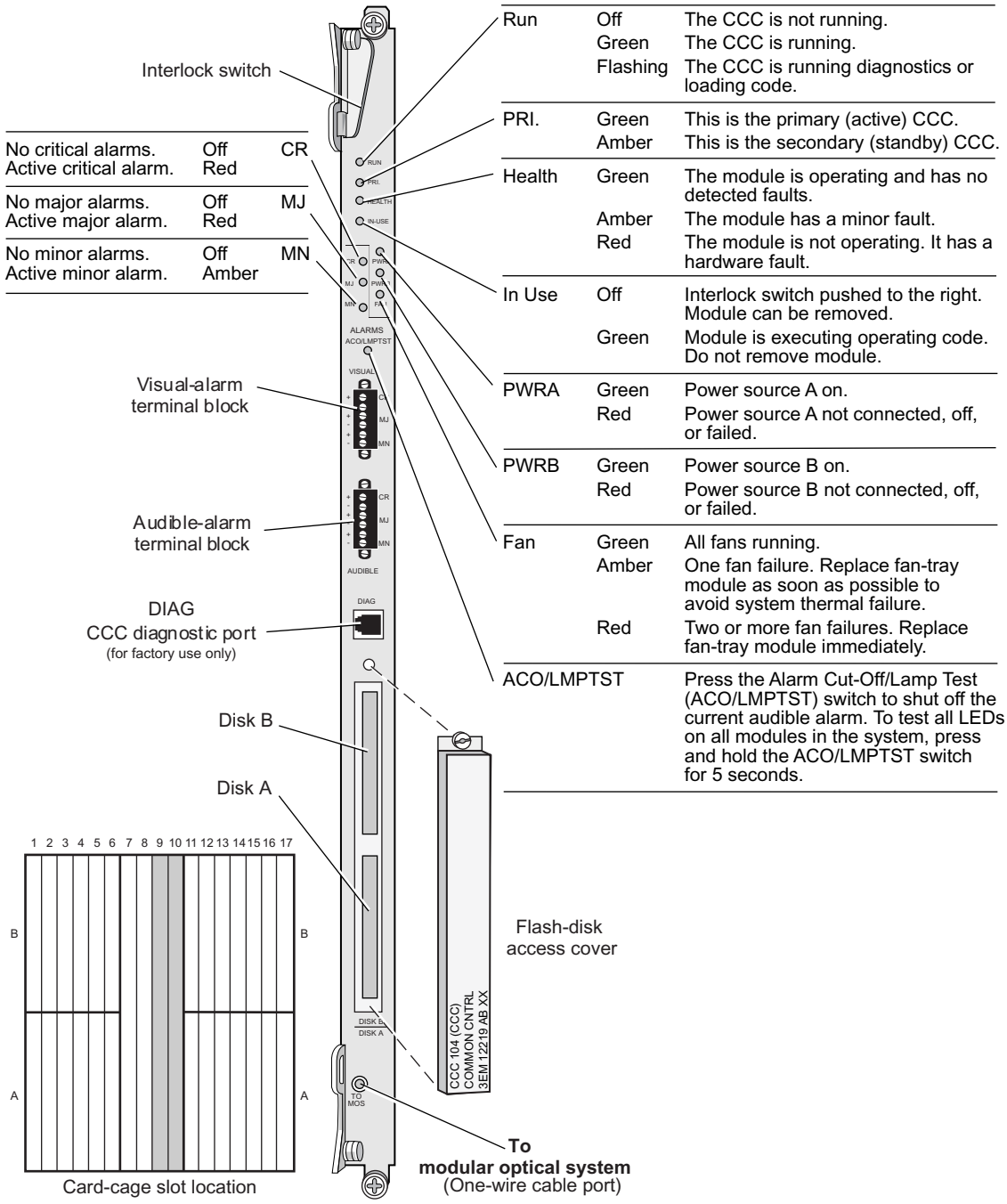
The CCC has two alarm-connection terminal blocks that connect to normally open relay contacts. One block controls minor, major, and critical visual alarms. The other controls minor, major, and critical audible alarms. At least one CCC is required for node operation. Two CCCs are required in slots 9 and 10 for redundant operation.

The two versions of the CCC can be mixed within the same protection group.

INDICATORS AND CONNECTORS

See figure 113-1 for descriptions of the CCC front panel indicators and connectors. See figure 113-2 for an illustration of the enhanced lever on the CCC 104.

Figure 113-1. CCC Front-Panel



Run	Off	The CCC is not running.
	Green	The CCC is running.
	Flashing	The CCC is running diagnostics or loading code.
PRI.	Green	This is the primary (active) CCC.
	Amber	This is the secondary (standby) CCC.
Health	Green	The module is operating and has no detected faults.
	Amber	The module has a minor fault.
	Red	The module is not operating. It has a hardware fault.
In Use	Off	Interlock switch pushed to the right. Module can be removed.
	Green	Module is executing operating code. Do not remove module.
PWRA	Green	Power source A on.
	Red	Power source A not connected, off, or failed.
PWRB	Green	Power source B on.
	Red	Power source B not connected, off, or failed.
Fan	Green	All fans running.
	Amber	One fan failure. Replace fan-tray module as soon as possible to avoid system thermal failure.
	Red	Two or more fan failures. Replace fan-tray module immediately.
ACO/LMPTST		Press the Alarm Cut-Off/Lamp Test (ACO/LMPTST) switch to shut off the current audible alarm. To test all LEDs on all modules in the system, press and hold the ACO/LMPTST switch for 5 seconds.

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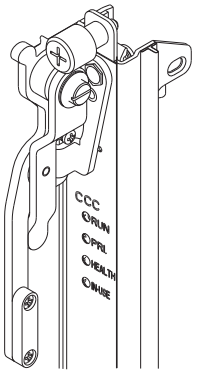
Figure 113-2. CCC 104 Enhanced Lever



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FUNCTIONAL OPERATION

The CCC is comprised of the following functional blocks (see figure 113-3):

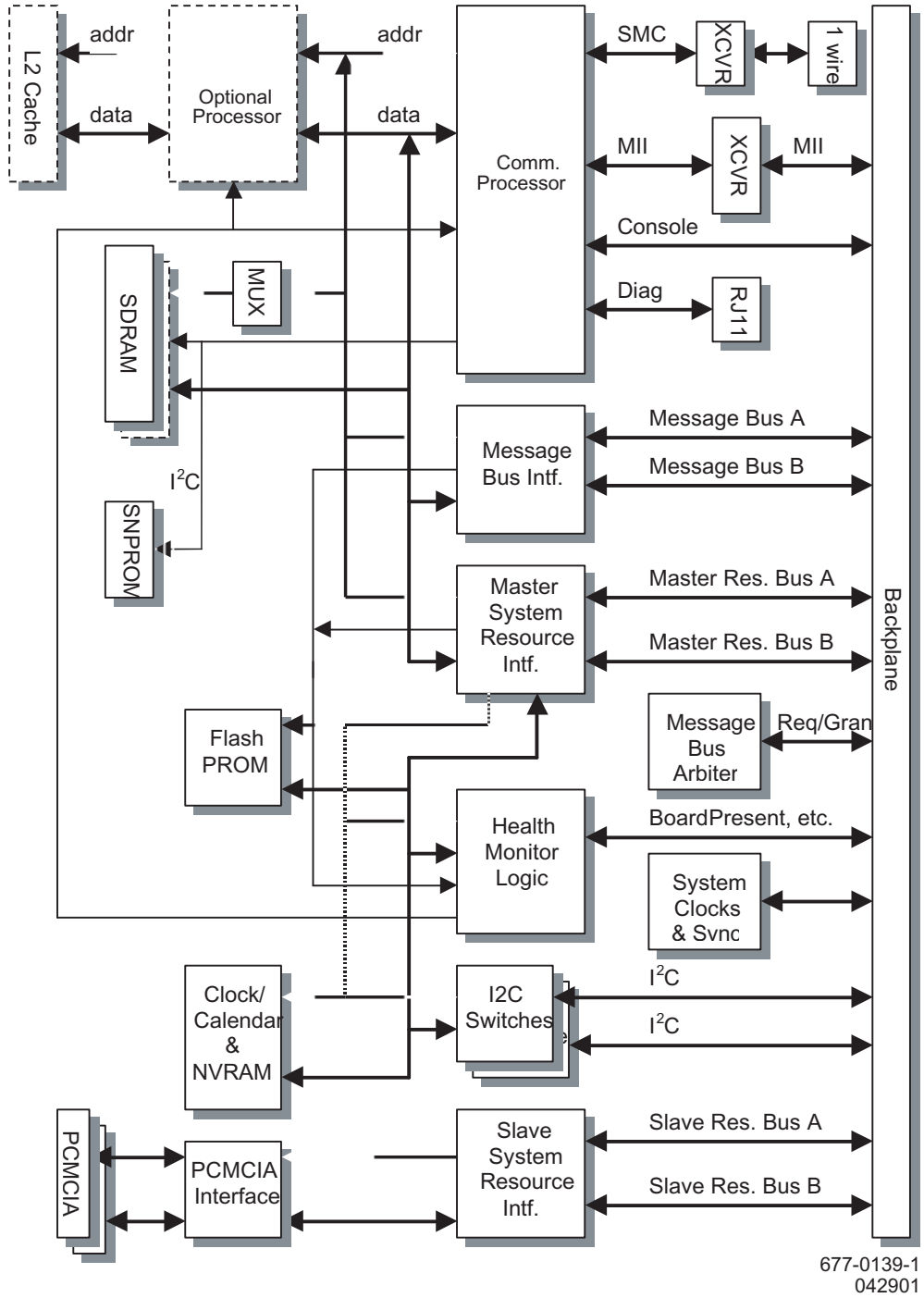
- Communications Processor
- L2 Cache
- Synchronous Dynamic RAM
- Flash PROM
- Interrupt Logic
- Message Bus Interface
- System Resource Interface
- Health Monitoring
- I^2C Bus
- Field Programmable Gate Array
- One-Wire Interface

The CCC contains an embedded communications controller that has two external buses to accommodate bandwidth requirements from the system core and communications channels. The communications controller is composed of three major functional blocks:

- Microprocessor
- System Interface Unit (SIU)
- Communications Processor Module (CPM)

The microprocessor is a high-performance low-power microprocessor that provides 32-bit effective addresses, integer data types of eight, 16, and 32 bits. It has a 64-bit split-transaction external data bus that is connected directly to the external communications controllers. The microprocessor also has an internal debug processor that allows access to internal scan chains for debugging purposes or can be used as a serial connection to the microprocessor for emulator support.

Figure 113-3. CCC Block Diagram



The SIU contains is a parallel system bus configurable to a 64-bit data width. The SIU arbitrates between internal components able to access the bus. It can be disabled, and an external arbiter can be used if necessary. The SIU also contains a memory controller supporting 12 memory banks allocated for system or local buses as well as a Test Access Port (TAP).

The CPM supports high bit rate protocols such as Fast Ethernet. The CPM performs lower layer tasks and DMA control functions on the local bus. A Serial Peripheral Interface (SPI), I^2C bus controllers, and Time-Slot Assigners (TSA) are also features of the CPM

An optional external processor can enabled to allow for a dual processor system. The L2 Cache can only be used with the external processor and is a system interface that contains 17 address bits, 64 data bits, and supports frequencies of up to 150 MhZ.

Two Synchronous Dynamic RAM (SDRAM) Small-outline Dual In-line Memory Modules (SODIMMs) are supported by the CCC, allowing the CCC to support memory sizes of 64 MB, 128 MB, 256 MB, and 512 MB. An SDRAM address mux is present between the 60x bus and the SDRAM and is required when the Communications Processor operates in the 60x interface bus mode. The SDRAM uses the I^2C interfaces for identification.

The CCC supports two 4 MB Flash (Programmable Read Only Memory (PROM) devices. Code stored in these devices supplies the initial reset vector, execution of power-up diagnostics, the system communicator driver, and the PCMCIA boot routine.

Interrupt logic merges internal and external interrupt states for presentation. Interrupt states are latched and made available through status registers. Features such as masking, clear on read, and polarity are supported, but are dependant on software.

The Message Bus Interface (MBI) provides the redundant communication link between the IOC and SSC modules. The following features are supported by the MBI:

- 64 bit 60X bus interface
- Packet based data transfers on two independent rails
- 400 Mb/s peak transmit rate
- 800 Mb/s peak receive rate
- CRC based error detection
- Flow control on both rails
- Field Programmable Gate Array

Each MIB requires a centralized arbitration resource. The system requires 32 request lines (for high and low priority) and 16 grant lines per message bus. Arbitration is done in a round-robin fashion with high priority requests taking precedence over low priority requests.

The CCC interfaces to the CCC PC Card and to the TC T1 framers through the System Resource Interface (SRI). The primary function of the SRI is to translate 60x bus operations to resource bus operations. The SRI permits the viewing of registers on the PC Card controller as if they were local to the CCC

Low Level Card Control and Peer Activity Monitor and Counting are the two primary functions of the Health Monitoring logic. Low Level Card Control is responsible for low level system control and status. It includes a Card Reset Register, Slot ID register, Card Present Register, Card Health Register, and a number of I^2C controllers. Peer Activity Monitor and Counter logic exists only on the CCC and consist of two components: a peer activity counter and peer activity monitor. The peer activity counter returns a 16 bit value and is incremented by a strobe signal generated by the other CCC. The peer activity monitor measures the time between strobes generated by the other CCC. If the provisioned time is exceeded, a processor interrupt is generated. One CCC contains a copy of the peer activity counter and timer and uses a strobe to loop back to the other CCC. This ensures the other CCC is receiving the strobe.

The SN Programmable Read-Only Memory (SNPROM) is a 256 byte device containing the board serial number and build date information and is accessed through the I^2C interface. I^2C controllers interface the CCC to a pair of backplane I^2C busses. Each bus connects to both CCC SN PROMS, the midplane SN PROMS, and the fan tray SN PROMS.

The Field Programmable Gate Array (FPGA) converts System Resource Bus (SRB) transactions to and from local ISA bus transaction.

The One-Wire Interface interfaces Modular Optical System (MOS) modules to the CCC for system control.

UDS-114
DCME/W 0x0 20/40/60/80 km East/West Dispersion Compensation Module

PART NUMBER/ MNEMONIC	NAME	CLEI	ECI/ BAR CODE	CPR	STATUS
3EM12222AA DCM	DCME 020 20 km East Dispersion Compensation Module	WMM9W01JRB	443250	205279	Active
3EM12223AA DCM	DCMW 020 20 km West Dispersion Compensation Module	WMM9W0ZJRB	443259	205278	Active
3EM12224AA DCM	DCME 040 40 km East Dispersion Compensation Module	WMM9WZ0JRB	443265	204959	Active
3EM12225AA DCM	DCMW 040 40 kM West Dispersion Compensation Module	WMM9W10JRB	443260	204960	Active
3EM12226AA DCM	DCME 060 60 km East Dispersion Compensation Module	WMM9W0XJRB	443257	205276	Active
3EM12227AA DCM	DCMW 060 60 km West Dispersion Compensation Module	WMM9W0YJRB	443258	205277	Active
3EM12228AA DCM	DCME 080 80 km East Dispersion Compensation Module	WMM9W20JRB	443261	204961	Active
3EM12229AA DCM	DCMW 080 80 km West Dispersion Compensation Module	WMM9W30JRB	443262	204962	Active

FEATURES AND APPLICATION NOTES

- SMF link compensation at 20 km, 40 km, 60 km, and 80 km
- Two ports; one IN and one OUT
- Installs in standard ANSI rack
- Connects to CCC through One-Wire Interface

DESCRIPTION

Dispersion Compensation Modules (DCMs) compensate for chromatic dispersion. See figure 114-1.Table 114-A lists the SMF length compensation and the average dispersion compensation provided by the DCM modules.

Figure 114-1. DCM Light Path

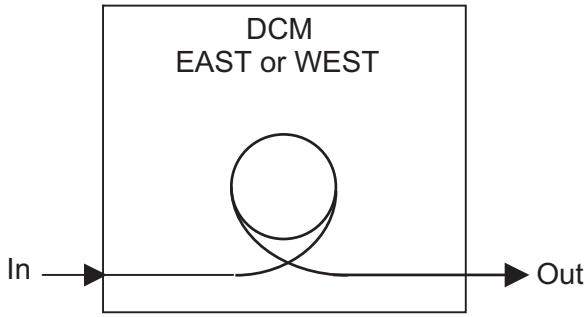


Table 114-A. DCM Module Variants

MODULE	SMF LENGTH COMPENSATION	AVERAGE DISPERSION COMPENSATION @ 1545nm
DCM-20-EAST, WEST	20 Km	-328.4 psec/nm
DCM-40-EAST, WEST	40 Km	-656.8 psec/nm
DCM-60-EAST, WEST	60 Km	-985.2 psec/nm
DCM-80-EAST, WEST	80 Km	-313.6 psec/nm

Only two of the 12 front-panel adaptor ports are used by the DCM. These two adapters reside on the opposite side of the cable routing side. East DCMs occupy the left two ports and West DCMs occupy the right two ports. The DCM has two face plates, one of which is replaced with a black panel and ports on the second face plate are replaced with caps. See figure 114-2. A dispersion compensation fiber sub-module is mounted onto a mounting plate inside the DCM. See figure 114-3.

Figure 114-2. DCM Module

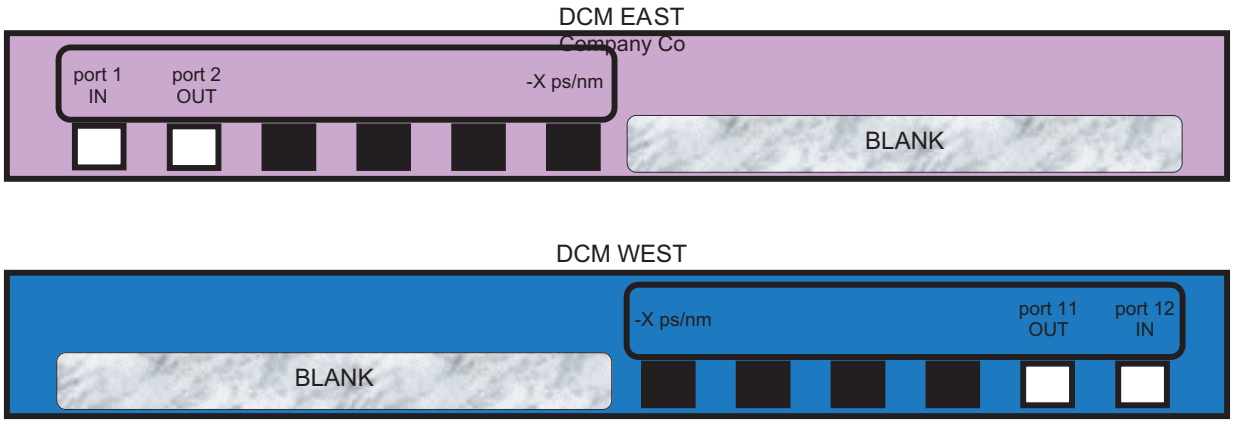
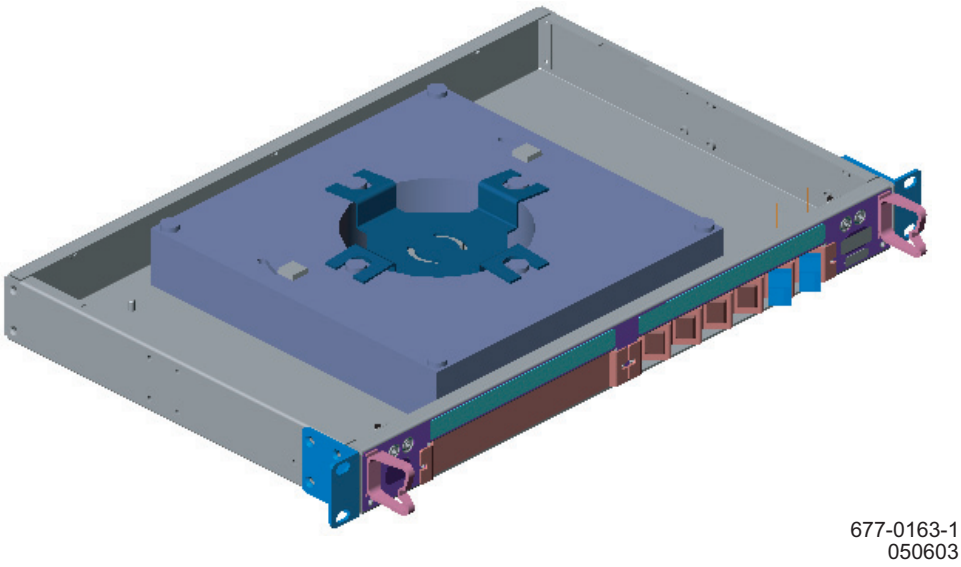


Figure 114-3. DCM Hardware Design



UDS-115
DS0G 101 DS0 Groomer (DS0G)

PART NUMBER/ MNEMONIC	NAME	CLEI	ECI/ BAR CODE	CPR	STATUS
3EM17343AA DS0G	DS0G 101 DS0 Groomer	SOUIARPAAA	138420	070AYA	Active

FEATURES AND APPLICATION NOTES

- Provides 2.5 Gb/s of DS0 switch capacity, equivalent to 48 DS3s or 1344 DS1s
- Provides DS1 facility termination
- Provides frame maintenance diagnostics and alarms
- Supports 2-way cross-connections
- Supports 4-state, 16-state, and transparent signaling formats
- Supports signaling fixing
- Supports DS0 test access
- Supports trunk conditioning and insertion word

DESCRIPTION

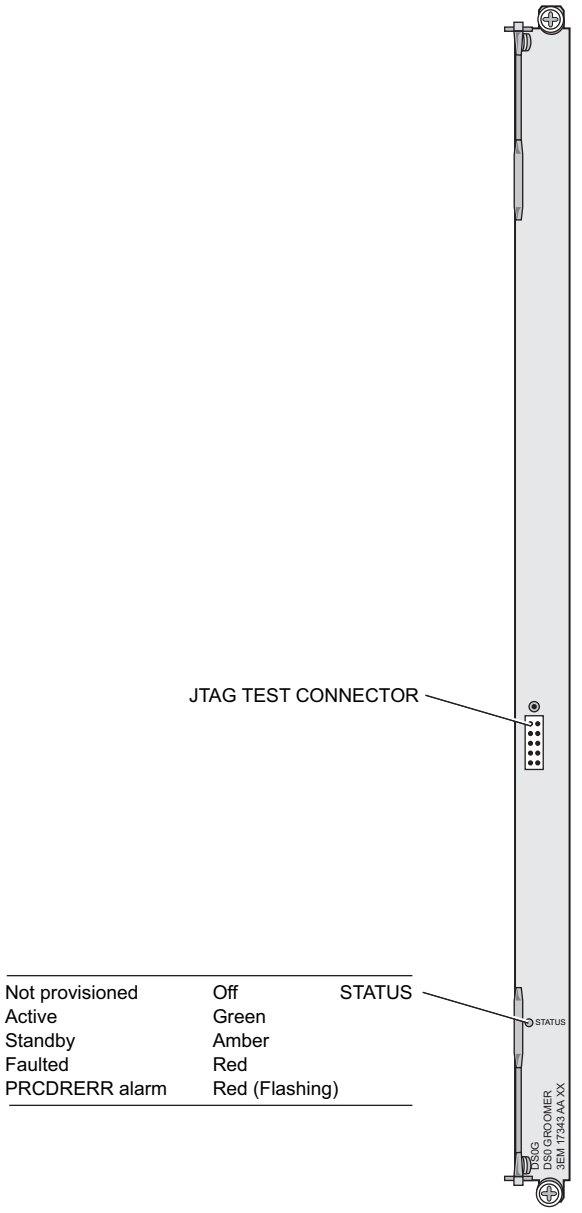
The DS0G 101 DS0 Groomer (DS0G) provides 2.5 Gb/s capacity of unidirectional DS0-level switching and grooming for VT-mapped traffic. The DS0G is a single-width, full-height module that installs into full-height slots 3/4-AB and 14/15-AB. It is 13.00 inches high, 1.00 inches wide, and 7.25 inches deep. See figure 115-1 for a front-panel outline of the DS0G. To support the DS0 Groomer, the SSC 104 80 Gb STS Switch Card (3EM12295AD) must be equipped.

Signals containing DS0 traffic can enter the system through any DS3, EC1, OC-3, OC-12, or OC-48 I/O port. The DS1/VT1.5 requiring DS0 grooming is cross-connected in the matrix to a DS1 port on the DS0G. The DS0G terminates the VT1.5 and the embedded DS1 in order to switch the DS0s. The DS0s are switched and new DS1/VT1.5 signals are generated. The VT1.5 is then sent back to the matrix for a second time for cross-connection to the outgoing I/O port.

INDICATORS AND CONNECTORS

Figure 115-1 describes the DS0G front panel indicators and connectors.

Figure 115-1. DS0G 101 DS0 Groomer (DS0G 101)



Not provisioned	Off	STATUS
Active	Green	
Standby	Amber	
Faulted	Red	
PRCDRERR alarm	Red (Flashing)	

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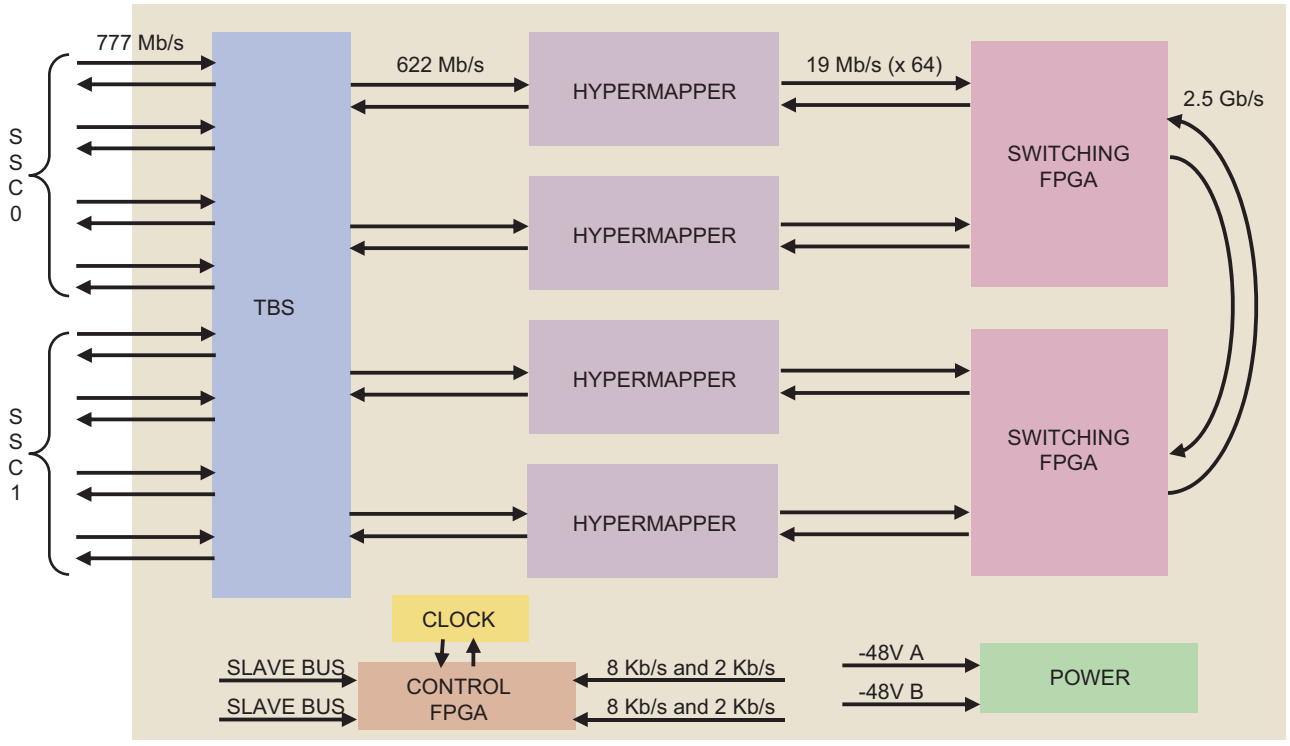
103106

FUNCTIONAL OPERATION

The functional components of the DS0G follow (see figure 115-2):

- Telecom Bus Serializer (TBS)
- Hypermapper
- Parallel Serial Bus (PSB) interface
- Switching Field Programmable Gate Array (FPGA)
- Control FPGA
- Clock

Figure 115-2. DS0G Block Diagram



TBS

The TBS provides backplane interface for the DS0G. It receives four STS-12 signals in 777 Mb/s telecom bus format from each SSC 103 STS Switch Card (SSC). It selects the active SSC signals and converts the 777 Mb/s telecom bus format signal to 622 Mb/s STS-12 signals for the hypermappers.

Hypermapper

The DS0G has four hypermappers. Each hypermapper processes 12 STS-1s worth of traffic. Each STS-1 is VT loaded. The VT1.5 and DS1 in the VT payload are terminated to access the DS0s.

In the receive direction, the hypermapper provides a high-speed interface, terminates section and line, performs STS-12 demultiplexing, provides pointer interpretation, performs path termination, performs STS-1 switching, performs VT pointer interpretation, provides VT termination, performs DS1 switching, serves as a DS1 framer, provides DS1 Performance Monitoring (PM), and serves as a signaling processor.

In the transmit direction, the PSB lines from the switching FPGA are multiplexed together at the hypermapper to generate the STS-12 going back to the TBS. In the transmit direction, the hypermapper serves as a DS1 frame formatter, performs DS1 switching, generates VTs, maps VTs into STS-1 payload, performs STS-1 switching, inserts section and line overhead, performs STS-12 multiplexing, and provides a high-speed interface.

PSB Interface

The PSB is the interface between the hypermappers and the switching FPGAs. The PSB is a 16-bit-wide data bus used for transferring DS0 traffic. There are eight sets of PSB lines between each hypermapper and switching FPGA (four sets for receive and four sets for transmit per hypermapper). A 19.4 MHz clock is used for synchronization for the PSB.

Switching FPGA

Each switching FPGA is connected to two hypermappers and receives one STS-12 worth of DS0 signals from each hypermapper. In the receive direction, each DS0 byte is accompanied with a signaling byte so the signal between the hypermapper and switching FPGA has the capacity of two STS-12 signals.

The switching FPGA is the DS0 switching device. To create a square matrix from two switching FPGAs, each switching FPGA transmits the signals it receives from two hypermappers to the other switching FPGA using 2.5 Gb/s interfaces. As a result, both switching FPGAs receive all traffic from all hypermappers.

Control FPGA

The control FPGA is responsible for the control of the DS0G. It receives both copies of the slave bus from copy 0 and copy 1 SSCs. The primary SSC signal indicates the active slave bus copy. The control FPGA has two main functions:

- Provide a slave bus interface to talk to the registers of all devices
- Provide a PM engine to process alarms and PM gathered from devices

There are no direct control interfaces from the control FPGA to the hypermappers. The control lines to the hypermappers are routed through the switching FPGAs to the hypermappers.

Clock

The DS0G receives two copies of 2 kHz and 8 kHz clock from both TC 301 Stratum 3 Timing Card II (TC) copies. The DS0G also receives clock copy selection signals from the CCC indicating which 2 kHz/8 kHz clock source should be selected as the board synchronization source. These signals are routed to the control FPGA. Based on the clock copy selection signals from the CCC and the presence of clocks, the control FPGA selects one 8 kHz signal as the board synchronization source.

The 8 kHz source is sent to the clock device to generate a 622 MHz clock. This clock then divided and buffered to generate all clocks required for all devices on the board. The control FPGA provides all necessary synchronization signals to all DS0G devices.

The switching FPGA generates 19 MHz clocks required for the PSB interface from the 78 MHz clock it receives from the control FPGA. The hypermapper requires four sets of two 19 MHz clocks (one for transmit data and one for receive data). The switching FPGA also forwards the 2 kHz/8 kHz composite signal required for the 622 Mb/s transmission from the control FPGA to the hypermappers.

UDS-116
DWDME/W 10x E/F-Band E/W-Dense Wavelength Division Multiplexer

PART NUMBER/ MNEMONIC	NAME	CLEI	ECI/ BAR CODE	CPR	STATUS
3EM12230AA DWDM	DWDME 101 E-Band E-Dense Wavelength Division Multiplexer	WMM9WX0JRB	443263	204957	Active
3EM12231AA DWDM	DWDMW 101 E-Band W-Dense Wavelength Division Multiplexer	WMM9WY0JRB	443264	204958	Active
3EM12232AA DWDM	DWDME 102 F-Band E-Dense Wavelength Division Multiplexer	WMM9W0WJRB	443256	205275	Active
3EM12233AA DWDM	DWDMW 102 F-Band W-Dense Wavelength Division Multiplexer	WMM9W0VJRB	443255	205274	Active

FEATURES AND APPLICATION NOTES

- Installs into standard ANSI rack
- Multiplexes/Demultiplexes optical channels in the E and F bands

DESCRIPTION

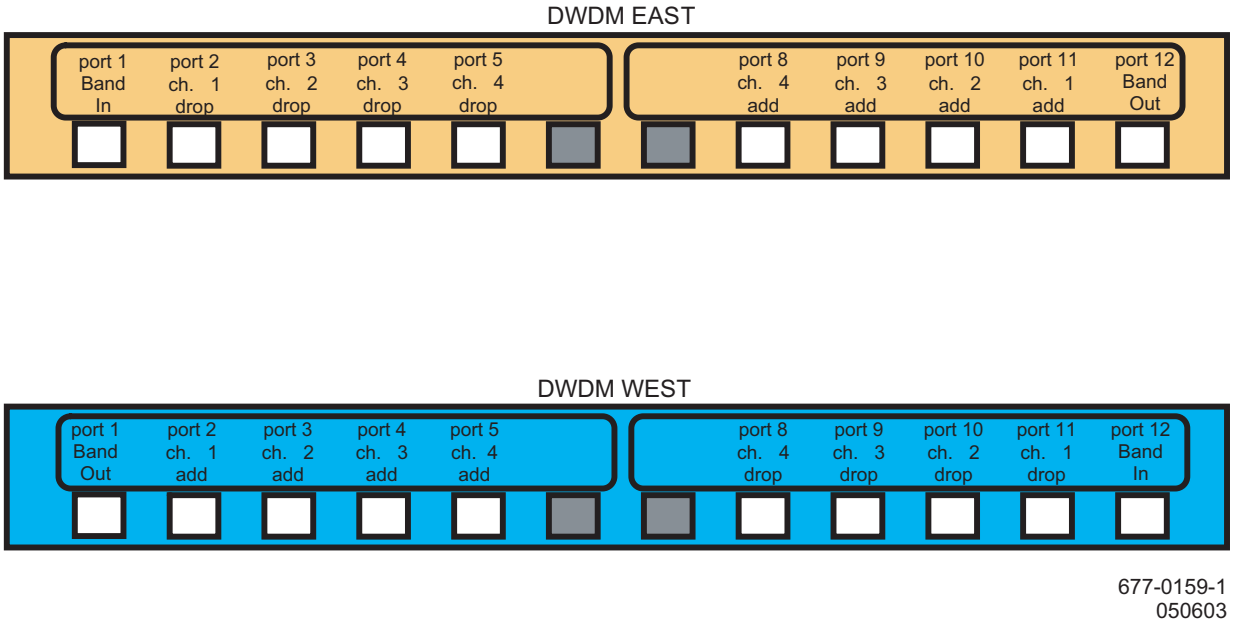
DWDM modules multiplex and demultiplex channels on tributary paths. When a band of channels is dropped by the Add/Drop Multiplexer (ADM) module, the channel enters the DWDM module on a single band of light. The DWDM module demultiplexes, or divides, the channel into separate, aggregate channels. When adding a group of channels to the ADM, the individual channels enter the DWDM module and are multiplexed, or combined, into one optical channel for transport.

Only 10 of the 12 front panel, DWDM ports are used for DWDM channels. For East DWDM modules, the left five ports are for demultiplexing and the right five ports are for multiplexing. For West DWDM modules, the left five ports are for multiplexing and the right five ports are for demultiplexing.

INDICATORS AND CONNECTORS

Figure 116-1 describes the DWDM front panel indicators and connectors.

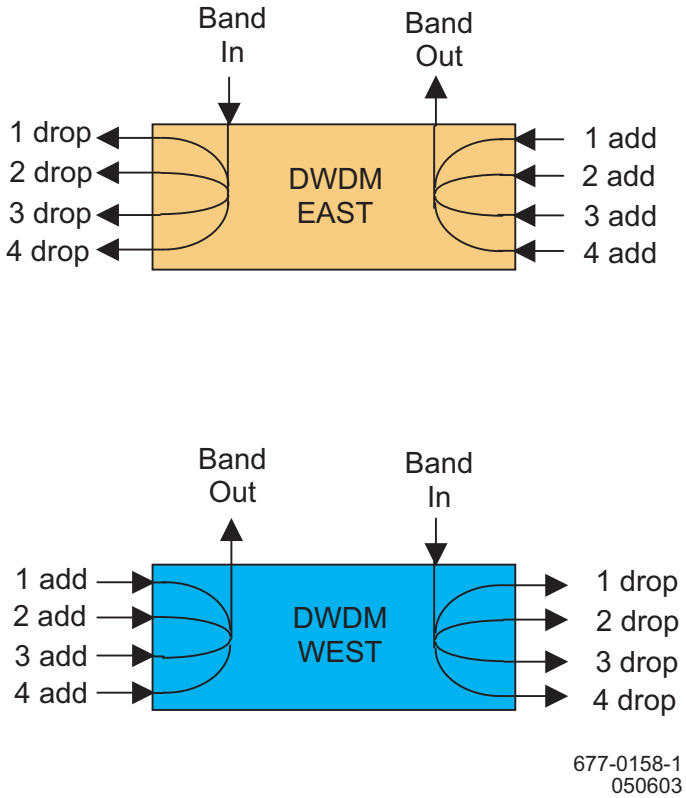
Figure 116-1. DWDM Front Panel



FUNCTIONAL OPERATION

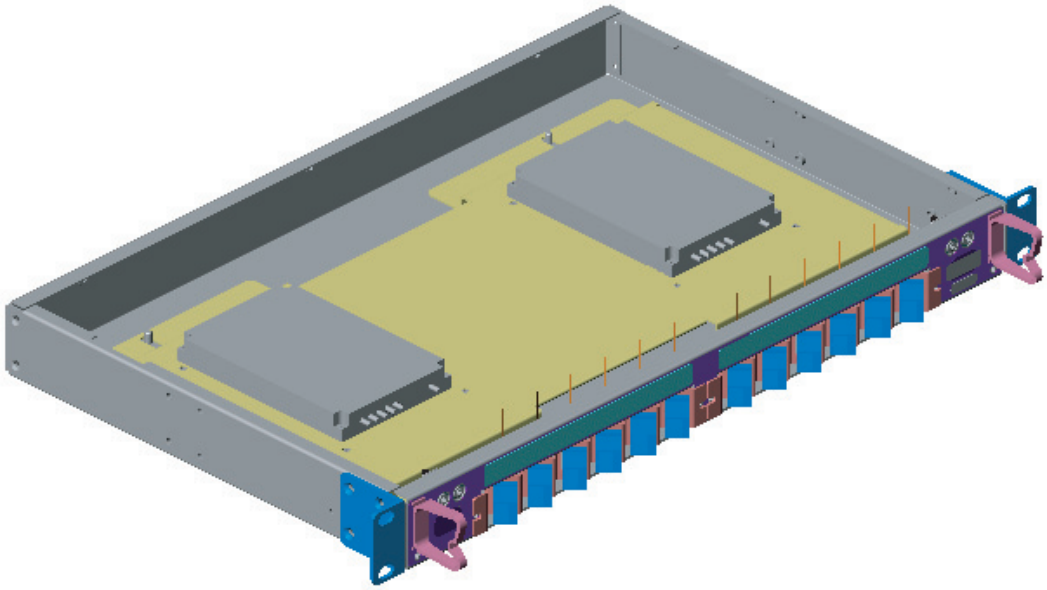
Currently, only bands E and F are considered standard configurations with short lead times. Channels 35 through 38 are available in the E band, and channels 30 through 33 are available in the F band. Both channel bands function in the East and West direction. See figure 116-2.

Figure 116-2. DWDM Signal Path



The DWDM module contains a sub-module that is mounted on different sides of the universal tray depending on whether the module is being used as an East or West module. If being used as an East module, the sub-module is mounted on the right side of the tray. The sub-module is mounted on the left side of the tray if being used as a West module. In order to function properly, fiber must be routed to the appropriately angled ports. See figure 116-3.

Figure 116-3. DWDM Hardware Design



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UDS-117
EDFA 10x Erbium Doped Fiber Amplifier

PART NUMBER/ MNEMONIC	NAME	CLEI	ECI/BAR CODE	CPR	STATUS
3EM12297AA EDFA	EDFA 103 Erbium Doped Fiber Amplifier, Pre-Amplifier	WMANEF0DAA	112423	M73377	Active
3EM12298AA EDFA	EDFA 104 Erbium Doped Fiber Amplifier, Line-Amplifier	WMANFF0DAA	112450	M73377	Active

FEATURES AND APPLICATION NOTES

- 23 dB signal gain
- Half-high (7.25”D x 8.49”H) 2-slots wide
- Slots 1&2, 3&4, 5&6, 12&13, 14&15, 16&17, A or B
- Number of channels 1 to 40
- SC shuttered connectors
- Maximum power input: 10 dBm
- Minimum EDFA power input:
  - Line amplifier: -28 dBm
  - pre-amplifier: -35 dBm
- Saturated power output:13 dBm

DESCRIPTION

The EDFA (Erbium-Doped Fiber Amplifier) module is an optical amplifier that can amplify as many as 40 ITU C-Band channels simultaneously. It is available as either a line amplifier or a pre-amplifier for the following general applications:

- The line amplifier—to amplify a signal after a transmitter and before the network fiber, or to amplify a signal at mid span.
- The pre-amplifier—to amplify a signal before a receiver.

The EDFA is a half-height, double-wide module that requires two adjacent half-height IOC slots. Figure 117-1 shows the module slot pairs recommended for EDFA installation. These slot pairs provide the most efficient use of the module slots in the node.

The length and type of fiber, age of fiber, number of fiber splices, and other factors affect fiber loss. Always submit the optical span characteristics to Alcatel-Lucent for analysis before determining whether or not an EDFA is needed and what amplifier type to use.

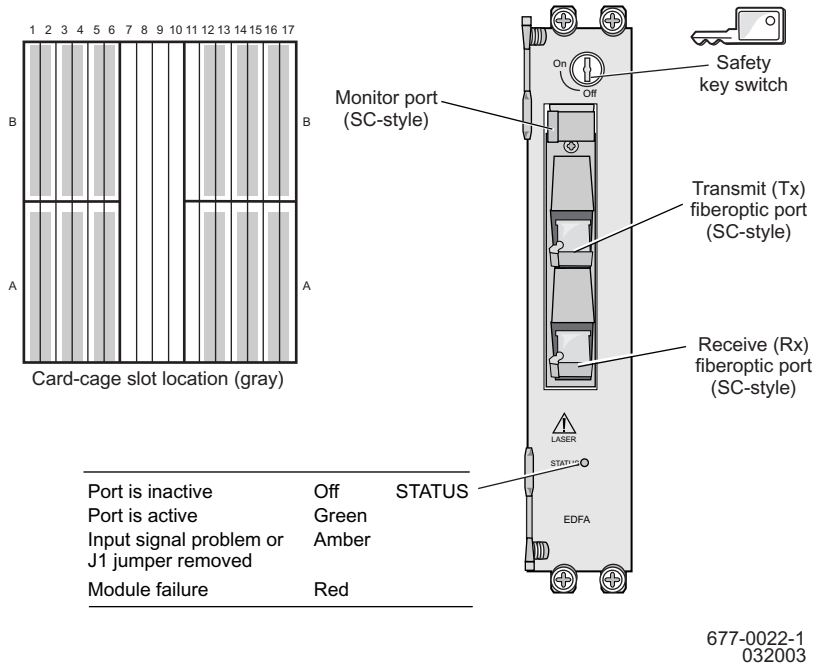
The On/Off key switch overrides software to ensure the module pump laser is turned off before any servicing occurs. With the switch turned off, nothing can activate the laser on the module. For safety, the user cannot remove the key unless the switch is in the off position. The line amplifier shuts down and generates an LOS (Loss Of Signal) alarm when the input signal falls below -28 dBm. The pre-amplifier does not.

The monitor port allows the measurement of the amplifier's output signal-to-noise ratio, using an optical spectrum analyzer.

INDICATORS AND CONNECTORS

Figure 117-1 describes the EDFA front panel indicators and connectors.

Figure 117-1. EDFA Front Panel



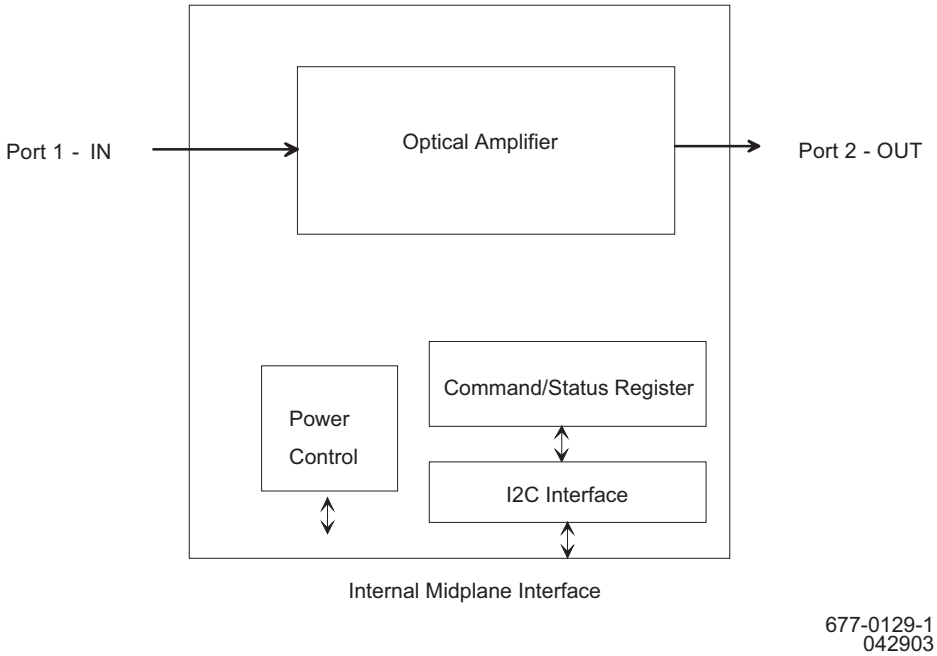
FUNCTIONAL OPERATION

Upon power up, the EDFA initializes, checks, and reports the amplifier alarm status before receiving a software command to begin operation. In Line Amplifier operation, if the input signal is less than -28 dBm, the amplifier shuts down and asserts a LOS alarm to the network manager. In the Pre-amplifier operation, if the input power level drops below the -28 dBm point, the amplifier remains turned on and a LOS alarm is not asserted.

The EDFA also monitors the presence of SSC primary bits. When the SSC primary bits are absent for more than 499 ms, the EDFA laser will shut down. The laser also shuts down after the assertion of over temperature alarms. LOS or Pump Bias alarms (indicating module end-of-life) are generated to network management applications.

Figure 117-2 illustrates the function of the EDFA.

Figure 117-2. EDFA Block Diagram



UDS-118
IFC1 101 12-Port DS3 Interface Card

PART NUMBER MNEMONIC	NAME	CLEI	ECI/BAR CODE	CPR	STATUS
3EM12236AA DS3-12P	IFC1 101 12-Port DS3 Interface Card	WMI9GDXLAA	126990	E73541	Inactive

FEATURES AND APPLICATION NOTES

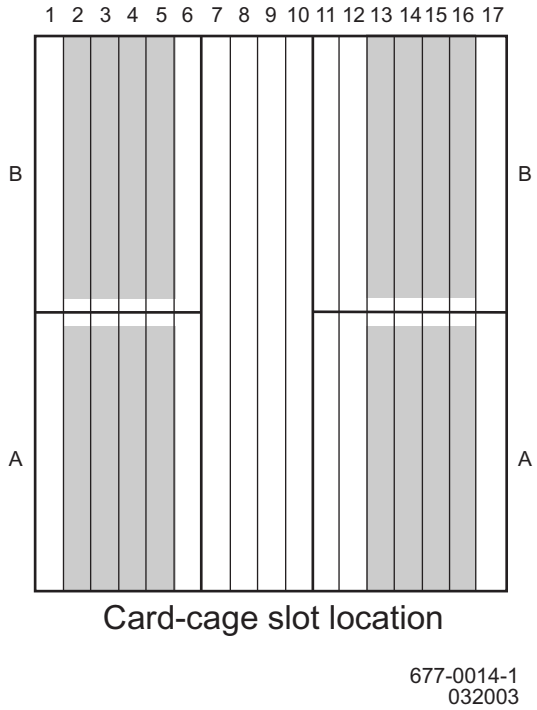
- 12 DS3 transports
- Half-height (7.25”D x 8.49”H), Slots 1–5, 13–17 A and B
- Accepts DS3 signals
- Automatic Protection Switching

DESCRIPTION

The DS3-12P provides 12 digital-service (DS) level 3 interfaces. The 1677 SONET Link supports up to sixteen 12-port DS3 modules in either unprotected or APS 1 x *n* protected states. Sixteen modules provide up to 192 DS3 interface port connections.

In unprotected configurations, DS3-12Ps are installed into slots 2-5B, 13B-16B, 2A-5A, and 13A-16A. If a module fails in unprotected operation mode, the traffic on the module will be interrupted.

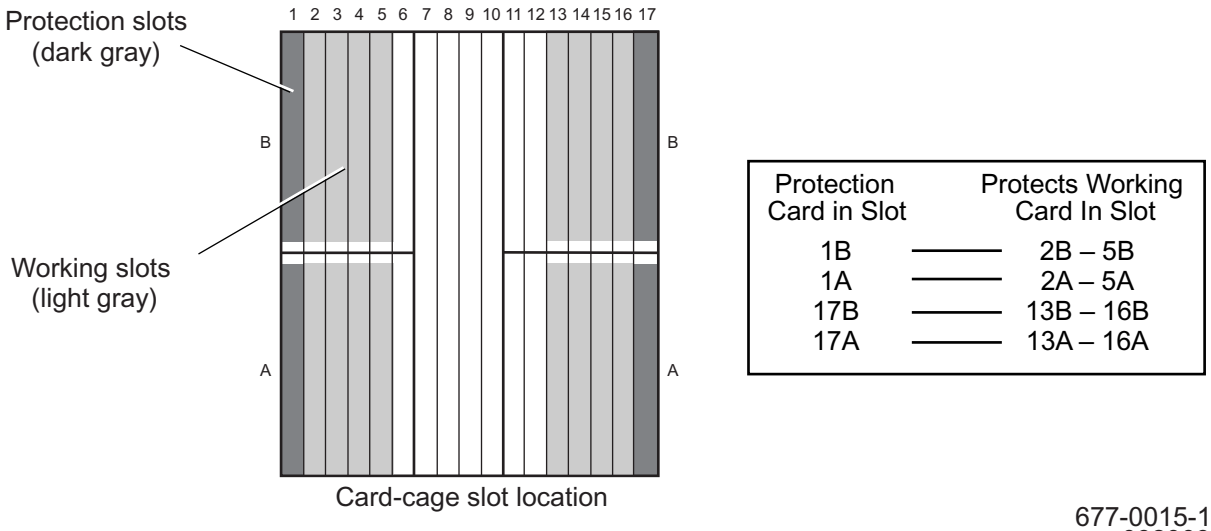
Figure 118-1. Unprotected DS3-12P Configuration



Protected Operation Mode (1 x *n*)

In protected configurations, a DS3-12P is installed into slots 1A, 1B, 17A, or 17B. The DS3-12P protects the DS3-12Ps installed in the adjacent four slots. One protection module protects any one of the four working modules. If a working DS3-12P fails, the protection DS3-12P working traffic is switched to the protection DS3-12P until the failed DS3-12P is replaced. Once the failed module is replaced the protection DS3-12P returns to the standby state after the Wait-To-Restore (WTR) timer expires.

Figure 118-2. Protected DS3-12P Configuration

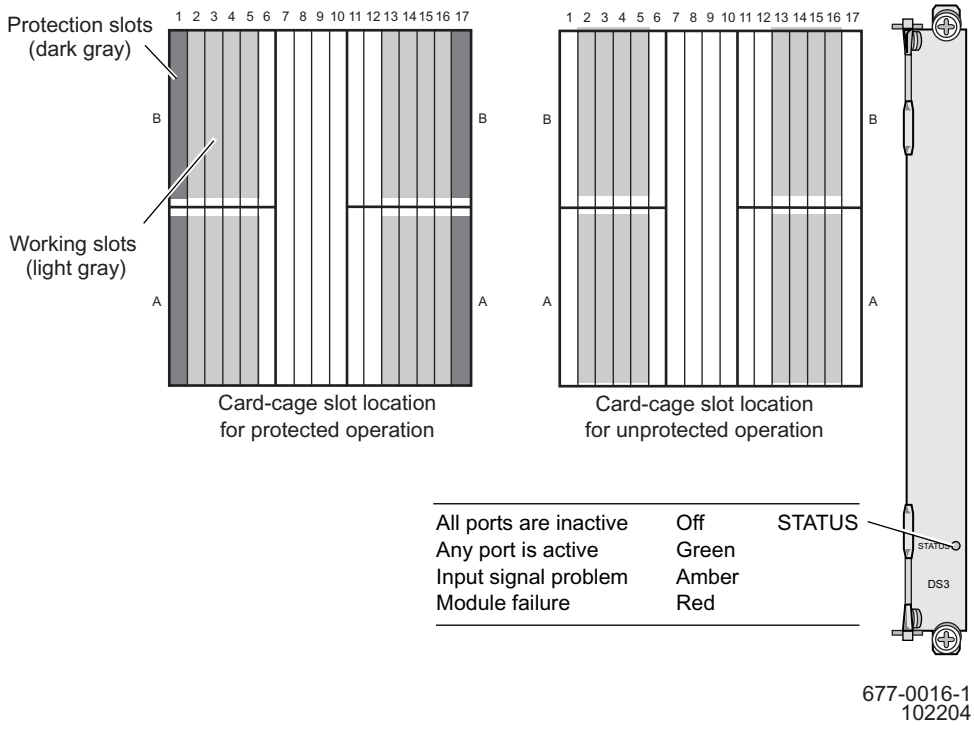


Working and protection DS3-12P are identical in nature. Working and protection functions are performed only when the module is installed into the associated working and protection slots.

INDICATORS AND CONNECTORS

Figure 118-3 describes the DS3-12P front panel indicators and connectors.

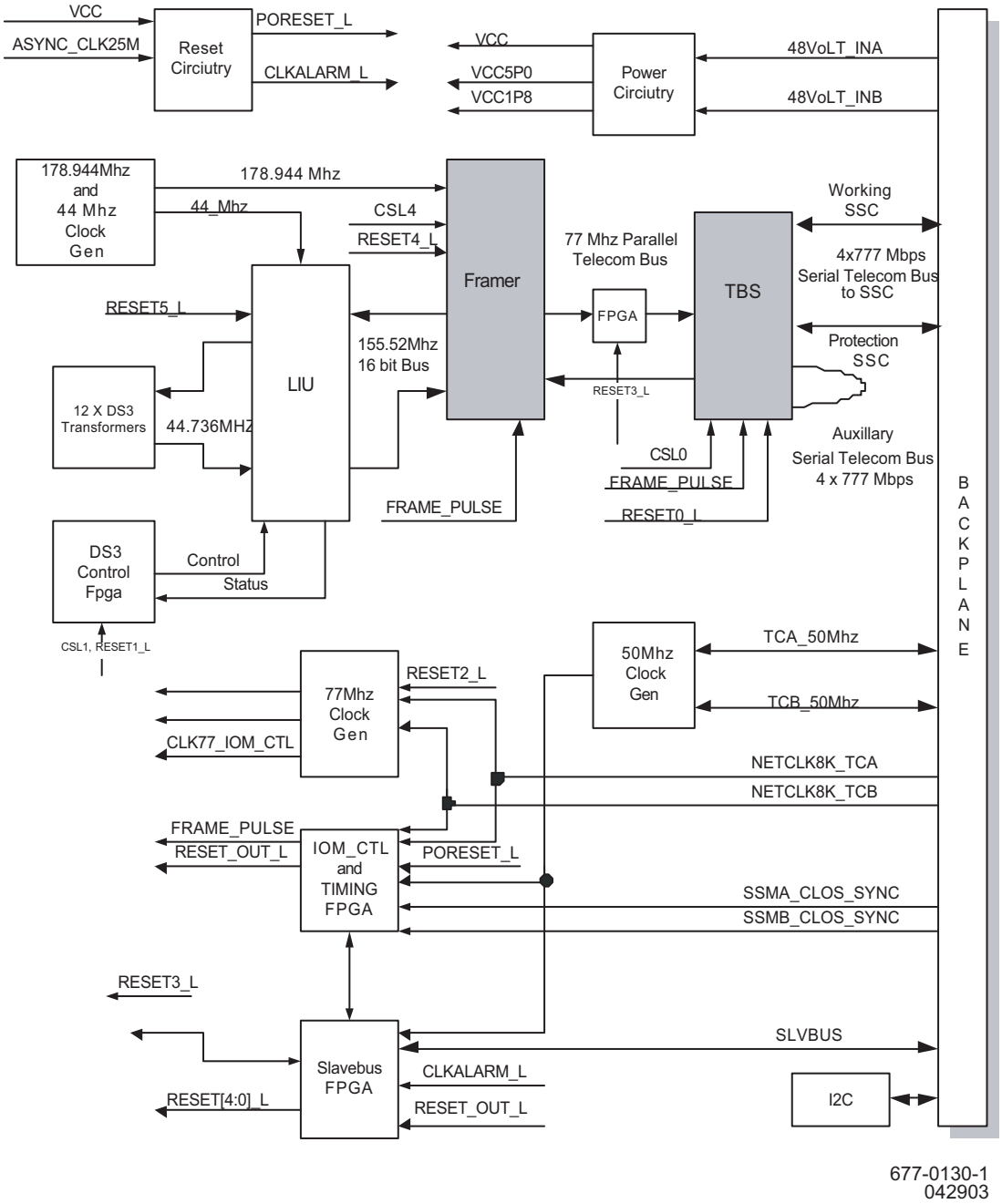
Figure 118-3. DS3-12P Front Panel



FUNCTIONAL OPERATION

Figure 118-4 illustrates the function of the DS3-12P and is followed by a brief description of the DS3-12P functional blocks.

Figure 118-4. DS3-12P Block Diagram



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The DS3-12P transmits and receives DS3 signals to/from the SSC switch matrix. The DS3-12P uses the following components:

- Telecom Bus Serializer
- DS3 Line Interface Unit
- Slave Bus Interface
- DS3 Control Field Programmable Gate Array
- Control Clock Distribution
- Reset Control
- System Clock and Frame Pulse Generation
- I^2C PROM
- Protection Drivers

The DS3-12P has three groups of four serial links connected to the backplane. One link connects to the working SSC, the second link connects to the protection SSC, and the third serial link connects to the adjacent IOC and is called the Auxiliary link. These buses connect directly to the Telecom Bus Serializer (TBS).

The TBS encodes Telecom Bus data in the receive direction from the Framer to the SCC through a 777.6 Mb/s Telecom Bus. In the transmit direction, the TBS decodes Telecom bus data from the SSC to an outgoing parallel Telecom Bus linking to the Framer. The TBS provides redundant working and protection streams for protection switching. The TBS also uses an auxiliary port loopback so that ports from both directions can be routed to local monitor ports.

The DS3 Line Interface Unit (LIU) is a triple layer unit with a physical layer interface between a Framer and the coaxial cable used for data transmission. LIU transceivers take a Non-Return to Zero (NRZ) input signal and encodes it into appropriate waveforms for transmission over coaxial cable. The receiver side takes the analog signal from the coaxial cable, equalizes, slices, and resychronizes it before decoding it to the NRZ output.

The Slave Bus Interface (SBI) connects the DS3-12P modules to the associated switch modules (SSCs). The SBI is split into two busses; a read bus and a write bus. All IOCs receive data on the write bus, while all SSCs receive data on the read bus.

The DS3 Control Field Programmable Gate Array (FPGA) configures and monitors the LIU for Power-down mode, Loop-back mode, Transmit Line Build-out, Transmit Output Enables/per channel, and sets the gain for the internal equalizer. The DS3 Control FPGA also monitors transmit and receive Loss Of Signal (LOS).

Two reset monitors are supported by the DS3-12P, one monitors power and the other monitors a 25 MHz clock. When the power monitoring device detects a power level not in the required 3.3 V range, a reset is administered. During power up, the reset is kept active for approximately 350 ms for the power supply to stabilize before being released.

The DC3-12P receives a system clock from the TC and is fed into two subsystems: System Clock Generator and Frame Pulse Generator with an 8 KHz loop clock reference. The System Clock Generator multiplies the 8KHz clock into a 77.76 MHz IOC system clock. The Frame Pulse Generator creates an 8 KHz frame pulse to align SONET payloads that pass from the IOC to the SSC.

The I^2C Serial Electrically Erasable Progammable Read-Only Memory (EEPROM) accesses the SSC and contains data such as board type, serial number, and manufacturing date. Such devices supply nonvolatile storage and allow the user to increase the amount of storage.

UDS-119
IFC1 201 12-Port DS3/EC1 Interface Card

PART NUMBER MNEMONIC	NAME	CLEI	ECI/BAR CODE	CPR	STATUS
3EM12348AA ECC-12P	IFC1 201 12-Port DS3/EC1 Interface Card	WMI2CZ0CAA	1127593	W70075	Active

FEATURES AND APPLICATION NOTES

- Provides 12 DS3/EC1 ports
- Accepts DS3 and EC1(electrical STS-1) signals
- Supports automatic protection switching

DESCRIPTION

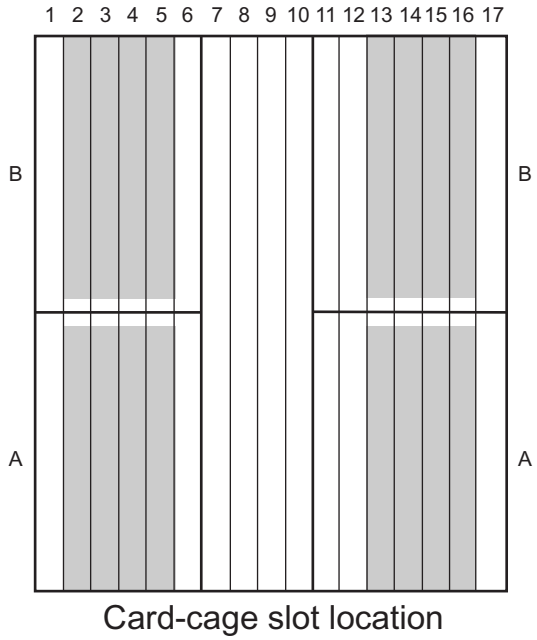
The IFC1 201 12-Port DS3/EC1 Interface Card (ECC-12P) provides 12 DS3 or EC1 interfaces. The 1677 SONET Link supports up to sixteen ECC-12Ps in either unprotected or APS 1 x *n* protected states. Sixteen ECC-12Ps provide up to 192 DS3 or EC1 interface port connections.

The ECC-12P is a half-height module that is 7.25 inches deep and 8.49 inches high.

Unprotected Operation Mode

In unprotected configurations, ECC-12Ps are installed into slots 2A-5A, 13A-16A, 2B-5B, and 13B-16B. See figure 119-1 for the unprotected ECC-12P configuration. If a module fails in unprotected operation mode, the traffic on the module will be interrupted.

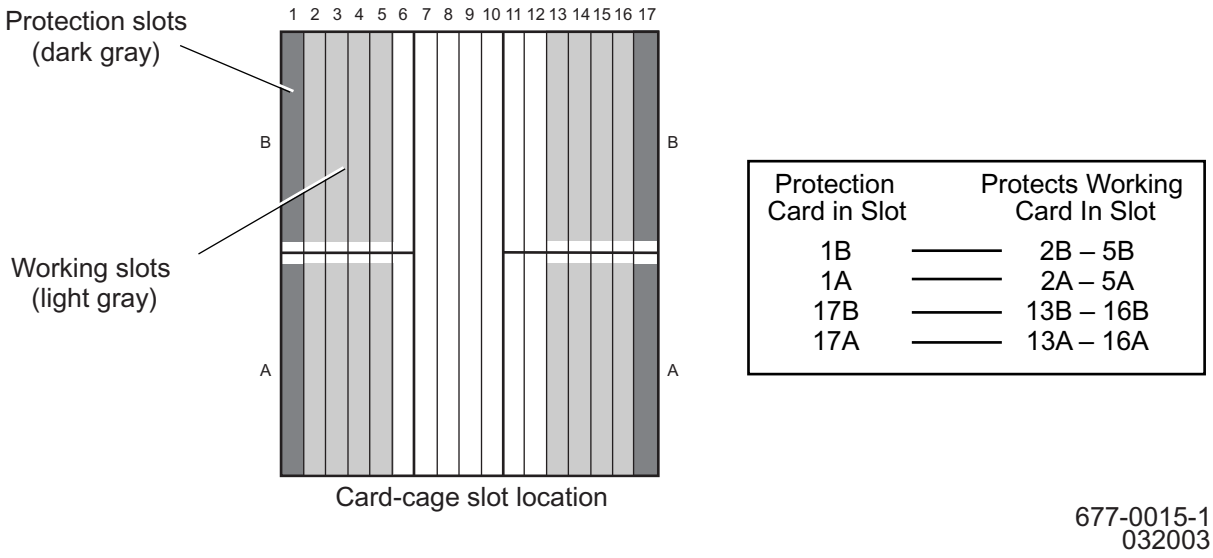
Figure 119-1. Unprotected ECC-12P Configuration



Protected Operation Mode (1:*N*)

For protected configurations, a protection ECC-12P is installed into slots 1A, 1B, 17A, or 17B. See figure 119-2 for the unprotected ECC-12P configuration. Each protection ECC-12P protects up to four ECC-12Ps installed in the adjacent slots. One protection ECC-12P protects any one of the four working ECC-12Ps. If a working ECC-12P fails, the working traffic is switched to the protection ECC-12P until the failed ECC-12P is replaced. Once the failed ECC-12P is replaced, the protection ECC-12P returns to the standby state after the Wait-To-Restore (WTR) timer expires.

Figure 119-2. Protected ECC-12P Configuration

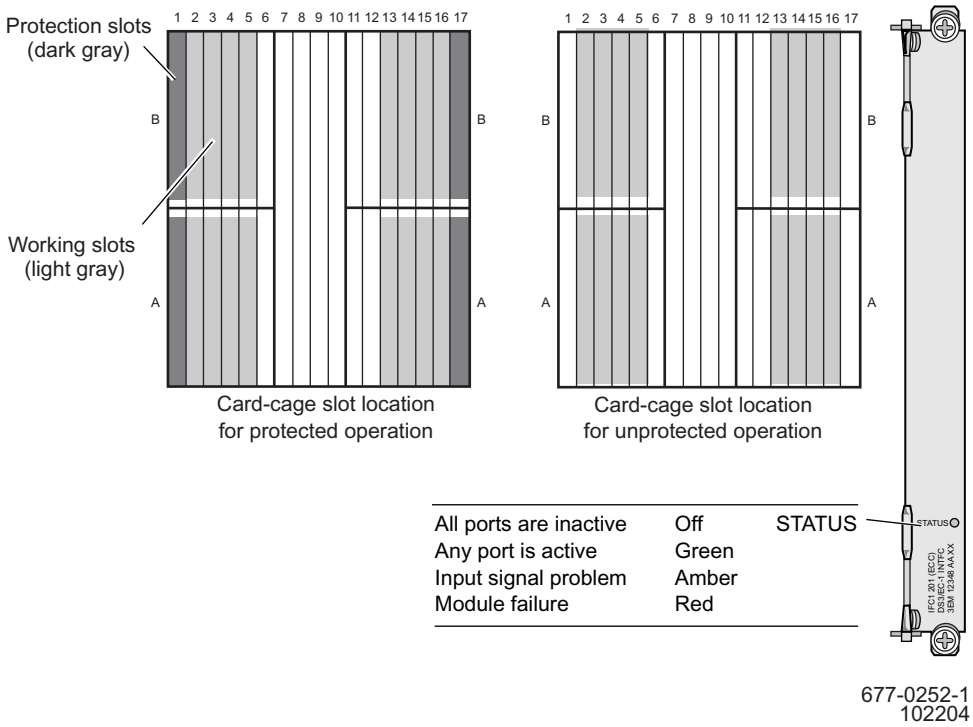


Working and protection ECC-12Ps are identical in nature. Working and protection functions are performed only when the module is installed into the associated working and protection slots.

INDICATORS

See figure 119-3 for ECC-12P front panel indicators.

Figure 119-3. ECC-12P Front Panel



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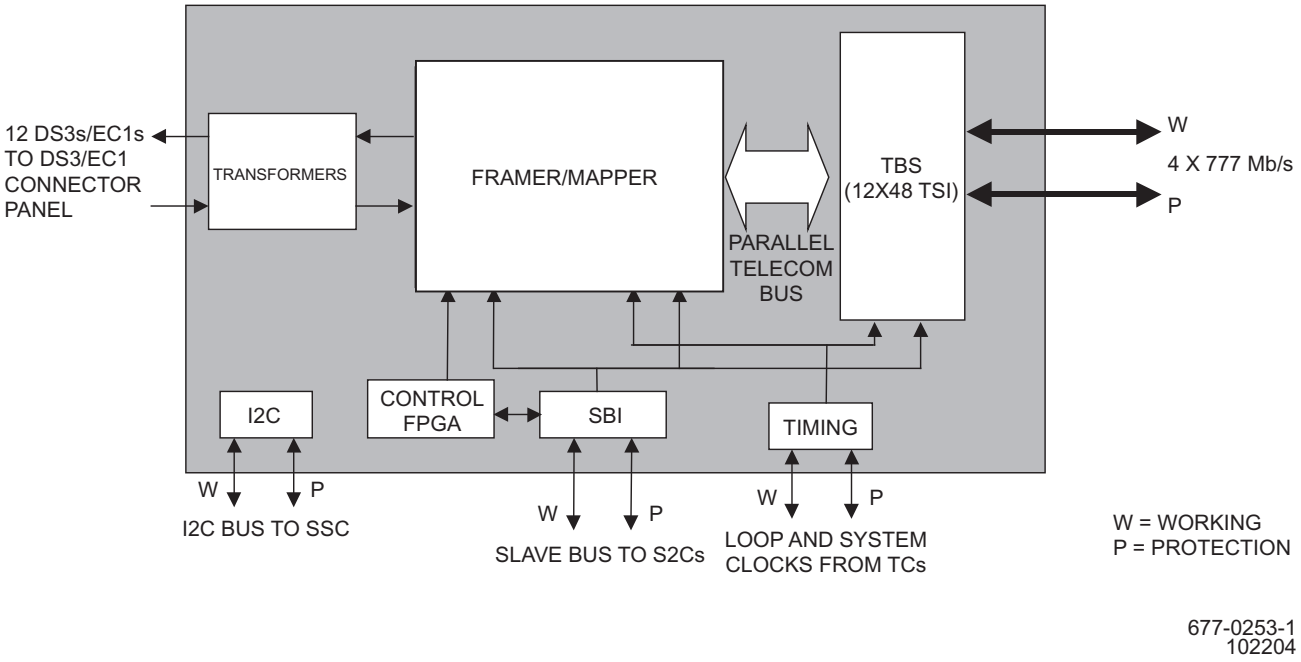
FUNCTIONAL OPERATION

The ECC-12P transmits and receives DS3 and/or EC1 signals to/from the SSC switch matrix. See figure 119-4. The ECC-12P uses the following components:

- Transformers
- Framer/mapper
- Telecom Bus Serializer (TBS)
- Slave Bus Interface (SBI)
- DS3 control Field Programmable Gate Array (FPGA)
- Protection drivers
- Reset control
- 50 MHz system clock
- System clock and frame pulse generators
- I^2C serial Electrically Erasable Programmable Read-Only Memory (EEPROM)

Figure 119-4. ECC-12P Block Diagram



Transformers

The ECC-12P contains 12 receive and 12 transmit transformers that serve as the DS3/EC1 interface to the DS3/EC1 connector panel.

Framer/Mapper

The framer/mapper is a complete DS3/EC1 line termination system for the physical layer. It includes 12 independent DS3/EC1 electrical Line Interface Units (LIUs) with built-in jitter attenuators, 12 DS3/EC1 framers, and 12 STS-1 framers. The line side interfaces of the framer/mapper support electrical DS3/EC1. The system side interface is a parallel 8×77.6 MHz telecom bus that encodes and decodes the parallel data stream it receives from the TBS.

Telecom Bus Serializer (TBS)

The ECC-12P has three groups of four serial links connected to the backplane. One link connects to the working SSC, the second link connects to the protection SSC, and the third serial link connects to the adjacent IOC and is called the auxiliary link. These buses connect directly to the TBS.

The TBS encodes telecom bus data in the receive direction from the framer/mapper to the SCC through a 777.6 Mb/s telecom bus. In the transmit direction, the TBS decodes telecom bus data from the SSC to an outgoing parallel telecom bus linking to the framer/mapper. The TBS provides redundant working and protection streams for protection switching. The TBS also uses an auxiliary port loopback so that ports from both directions can be routed to local monitor ports.

Slave Bus Interface (SBI)

The SBI connects the ECC-12P modules to the associated SSCs. The SBI is split into two busses; a read bus and a write bus. All IOCs receive data on the write bus, while all SSCs receive data on the read bus.

DS3 Control Field Programmable Gate Array (FPGA)

The DS3 control FPGA configures and monitors the LIU for power-down mode, loopback mode, transmit line build-out, transmit output enables per channel, and sets the gain for the internal equalizer. The DS3 control FPGA also monitors transmit and receive Loss Of Signal (LOS).

Protection Drivers

Protection drivers are used to control which ECC-12P signals are selected for protection.

Reset Control

Two reset monitors are supported by the ECC-12P, one monitors power and the other monitors a 25 MHz clock. When the power monitoring device detects a power level not in the required 3.3 V range, a reset is administered. During power up, the reset is kept active for approximately 350 ms for the power supply to stabilize before being released.

50 MHz System Clock

The ECC-12P receives a 50 MHz system clock from the two Common Control Cards (CCCs). A local clock monitor can flag an alarm condition, causing a switchover to the redundant 50 MHz clock.

System Clock and Frame Pulse Generation

The ECC-12P receives 8 kHz network timing from the TC routes it into two subsystems: System clock generator and frame pulse generator. The system clock generator multiplies the 8 kHz clock into a 77.76 MHz IOC clock for use by the framer/mapper, the TBS, and the DS3 FPGA. The frame pulse generator uses the 8 kHz clock to create an 8 kHz frame pulse to align SONET payloads that pass from the IOC to the SSC.

I^2C Serial Electrically Erasable Programmable Read-Only Memory (EEPROM)

The I^2C serial EEPROM accesses the SSC and contains board type, serial number, and manufacture date data. The I^2C serial EEPROM supplies 256 bytes of nonvolatile storage and allows the user to increase the amount of storage.

UDS-120
IFC2/4 10x 2-Port Gigabit Ethernet

PART NUMBER/ MNEMONIC	NAME	CLEI	ECI/BAR CODE	CPR	STATUS
3EM12310AA GIGE-2P	IFC2 101 2-Port Gigabit Ethernet, LX	WM6IV0SAAA	114319	P73113	Active
3EM12310AB GIGE-2P	IFC2 102 2-Port Gigabit Ethernet, LX	TBD	TBD	TBD	Active
3EM12311AA GIGE-2P	IFC4 101 2-Port Gigabit Ethernet, SX	WM6IV0TAAA	114326	P73114	Active
3EM12311AB GIGE-2P	IFC4 102 2-Port Gigabit Ethernet, SX	TBD	TBD	TBD	Active

FEATURES AND APPLICATION NOTES

- Two ports
- Half-height (7.25”D x 8.49”H), Slots 1-6 and 12-17, A or B
- 1000BASE-SX, LX Field Replaceable Optics
- Generic Framing Protocol Encapsulation
- Virtual Concatenation of up to 24 STS-1s
- 50 MHz Clock Distribution

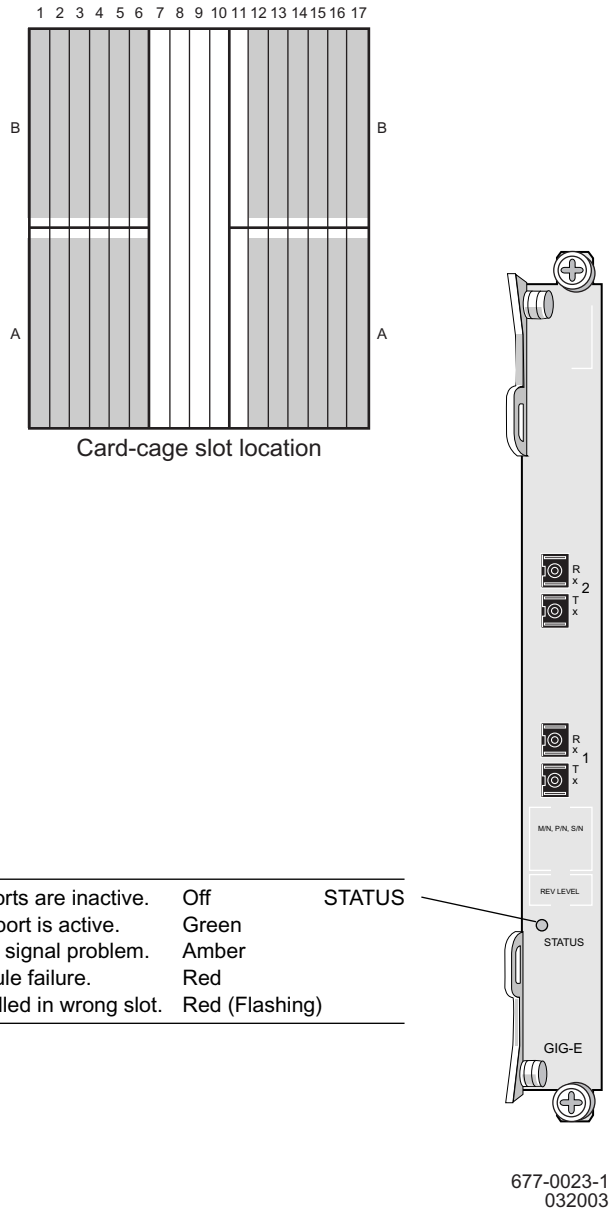
DESCRIPTION

The Gigabit Ethernet (GIGE) module supports two IEEE 802.3-compliant ports operating in serial mode. The GIGE is a half-height Input/Output Card (IOC) that can be installed into any IOC slot connecting to a 777 MHz backplane. It supports 1000BASE-SX, LX Field Replaceable Optics and Generic Framing Protocol (GFP) for mapping Ethernet frames into SONET payload.

INDICATORS AND CONNECTORS

Figure 120-1 describes the GIGE front panel indicators and connectors.

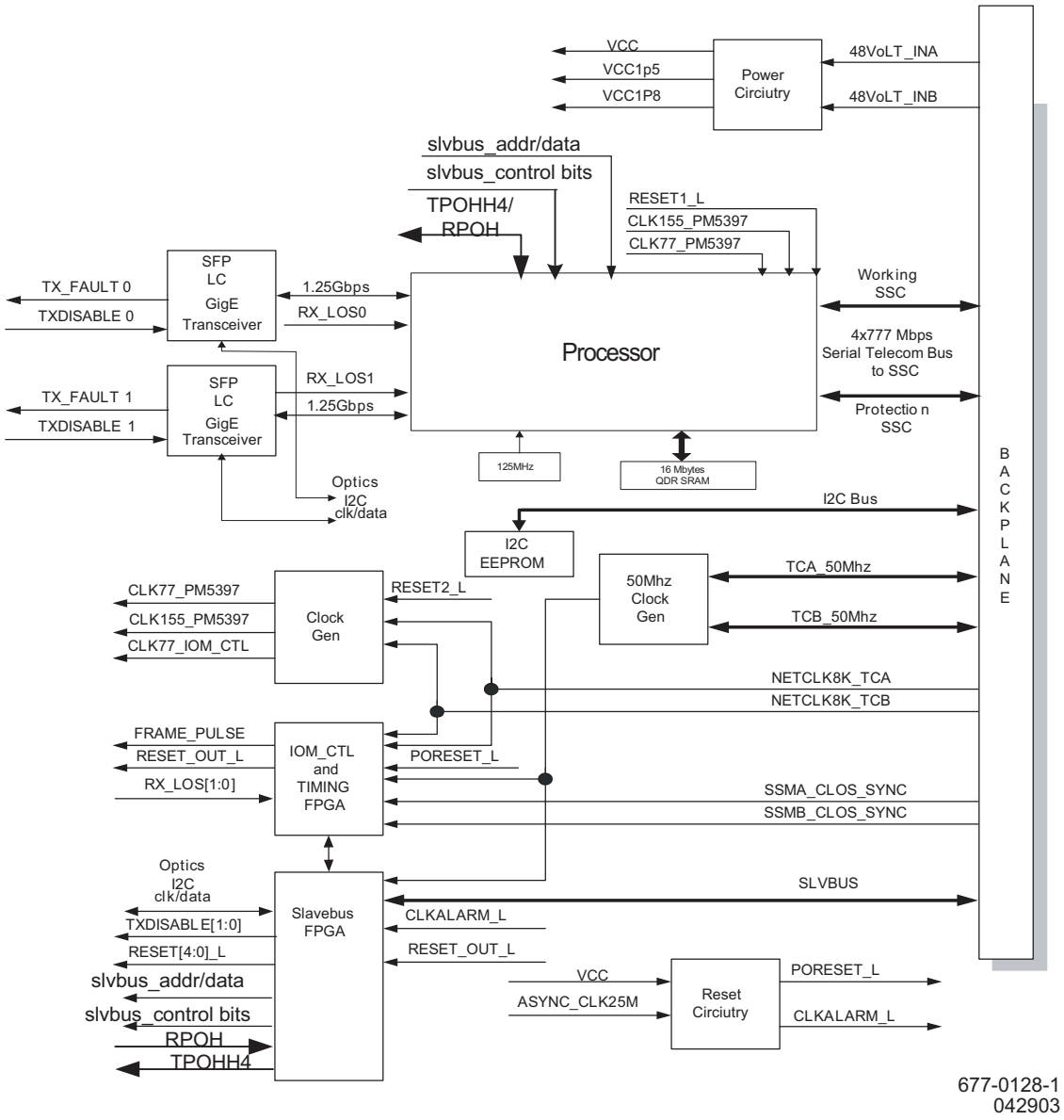
Figure 120-1. GIGE Front Panel



FUNCTIONAL OPERATION

Figure 120-2 illustrates the function of the GIGE and is followed by a brief description of the GIGE functional blocks.

Figure 120-2. 2.5 GIGE Block Diagram



The GIGE uses the following components to convert Ethernet signals into SONET payload frames.

- Processor
- Slave Bus Interface
- System clocks and Frame Pulse Generation
- 50 MHz Clock Distribution
- Reset Control
- I^2C Bus
- DC-DC Conversion

The main function of the processor is to map Ethernet frames into a SONET payload structures. The processor is configured, controlled and monitored by the Slave Bus. It integrates two Clock Synthesis Units (SIU) to allow the support of Gigabit Ethernet (GE) and SONET frames. The GE synthesizes a 1250 MHz clock while the SONET SIU synthesizes a 777.6 MHz and a 2.488 GHz clock for use in SONET transmit and data path interfaces.

The processor supports one working and one protect 4x777.6 MHz serial Telecom Bus, a 4x622.08 Mb/s SONET Signal Interface (SSI), or a 2.488 Gb/s SSI. The data pair (Working and Protect) is transferred over a 4x777.6 MHz stream with each 777.6 MHz carrying an STS-12 signal. The aggregate 2.4 Gb/s data rate is transferred across the four pairs. The data pair must be set to the same 4x777.6 MHz serial Telecom bus, 4x622.08 Mb/s SSI or 2.5 Gb/s SSI mode.

GE frames in each channel are encapsulated using GFP and mapped to SONET payload structures for transport. On the transmit side, the GFP encapsulation is removed to retrieve GE frames. GFP is accomplished in the same bandwidth as the native GE rate.

VC is performed by the processor for two GE channels. VC multiplexes data up to a 2.4 Gb/s aggregate rate into STS-1 channels. Time Slot Interchange (TSI) hardware downstream allows for arbitrary assignment of these STS-1 channels.

The Slave Bus Interface (SBI) supports two Field Programmable Gate Arrays (FPGA) and provides high-speed communications between the IOCs and the associated SSC. The SBI is divided into a Read SBI and a Write SBI where the IOCs receive on the Write SBI and the SSCs receive on the Read SBI.

The system clock from the TC is fed into two subsystems on the GIGE: System Clock Generator and the Frame Pulse Generator for SONET frames. The System Clock Generator provides a 155.52 MHz IOC system clock as well as a 777.76 MHz clock, both used by the Arrow device.The working SSC STS controller uses the slave bus to select a TC system clock reference for the GIGE. In the Frame Pulse Generator subsystem, an 8 KHz frame pulse is used to align all SONET payloads passing from the GIGE to the SSC.

The CCCs source the system clocks, which are all point-to-point PECL pairs distributed at 50 MHz. The GIGE receives two copies of the 50 MHz clock from each CCC.

Two reset monitors are supported by the GIGE, one monitors power and the other monitors a 25 MHz clock. When the power monitoring device detects a power level not in the required 3.3 V range, a reset is administered. During power up, the reset is kept active for approximately 350 ms for the power supply to stabilize before being released. When a missing clock event is detected, a clock alarm is generated to the CCC through the SBI, forcing the use of the other clock.

The I^2C Serial Electronically Erasable Programmable Read-Only Memory (EEPROM) contains data such as board type, serial number, and manufacturing date. Such devices supply nonvolatile storage and allow the user to increase the amount of storage. The I^2C bus is also used to read information from SFP Lasers on the GIGE.

DC power is converted onboard from the -48 V backplane supply. Most of the power is consumed at 1.8 and 3.3 V. In order to avoid over powering, the following power sequence is observed: 3.3 V power supply is powered up first, followed by the 1.8 V supply, then the 1.5 V supply.

UDS-121
LCx 10x 12-Port OC-3 Line Card

Card

PART NUMBER/ MNEMONIC	NAME	CLEI	ECI/BAR CODE	CPR	STATUS
3EM12238AA OC3-12P	LC2 101 12-Port IR OC-3 Line Card	WMOTAXNEAA	126566	J73865	Active
3EM12238AB OC3-12P	LC2 102 12-Port IR OC-3 Line Card	WMOTBBBEAA	130522	W70844	Active

FEATURES AND APPLICATION NOTES

- 12 SONET OC-3 ports
- Half-height (7.25”D x 8.49”H)
- Slots 1–6, 12–17, A and B
- LC-style connectors
- Data Communications Channel (DCC) selection
- UPSR and APS protection
- Line timing source for TC
- SONET performance monitoring

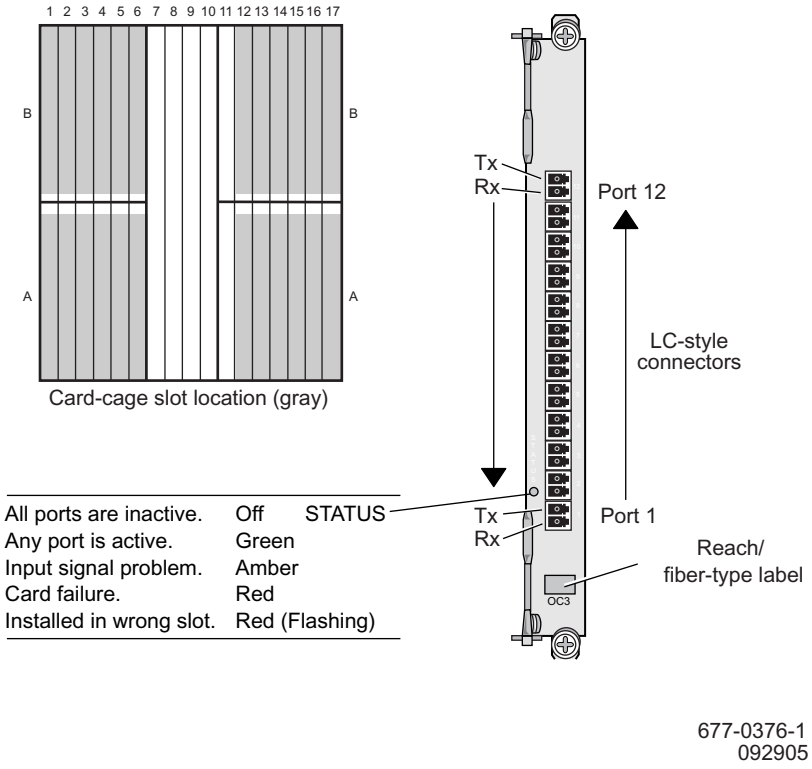
DESCRIPTION

The SONET OC-3 line card provides twelve optical-carrier (OC) level 3, 1310 nm interfaces. The module has a Single Mode (SM), Intermediate Reach (IR) laser transmitter.

INDICATORS AND CONNECTORS

Figure 121-1 describes the OC3-12P front panel indicators and connectors.

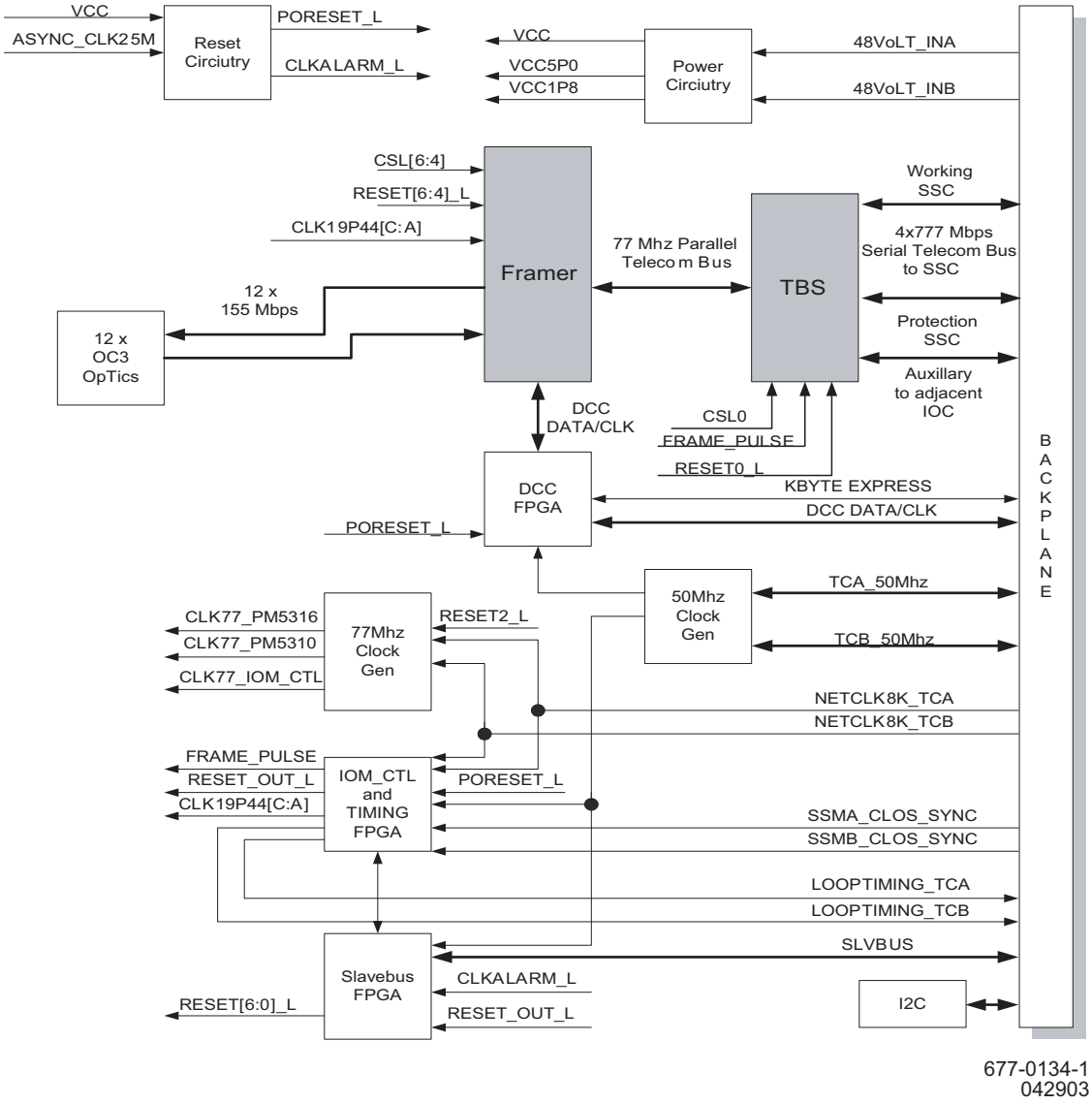
Figure 121-1. OC3-12P Front Panel



FUNCTIONAL OPERATION

Figure 121-2 illustrates the function of the OC3-12P and is followed by a brief description of the functional blocks.

Figure 121-2. OC3-12P Block Diagram



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The OC-3 IOC transmits STS-1 signals to the SSC through the following module components: (See figure 121-1.)

- OC3 Telecom Bus Serializer
- OC3 Framer/Processor
- Slave Bus Interface
- DCC Interface
- Control Clock Distribution
- Reset Control
- I^2C PROM

The OC3-12P has three groups of four serial link connections to the system backplane. One link connects to the working SSC, another link connects to the protection SSC, and a third serial link connects to the adjacent IOC and is called the Auxiliary link. These buses connect directly to the Telecom Bus Serializer (TBS).

The TBS encodes Telecom Bus data in the receive direction from the Framer to the SCC through a 777.6 Mb/s backplane Telecom Bus. In the transmit direction, the TBS decodes Telecom bus data from the SSC to an outgoing parallel Telecom Bus linking to the Framer. The TBS provides the capacity to carry an STS-3 stream as well as redundant working and protection streams for protection switching. The TBS also uses the auxiliary link to connect to the adjacent IOC for through and ring applications.

The framer receives SONET STS-3s from the optical devices on the OC3-12P and terminates the transport and path overhead. Transport over head, such as DCC, is extracted and the Synchronous Payload Envelope (SPE) is put on the DROP Telecom Bus for transport to the TBS. The framer receives data on the ADD Telecom Bus and prepares it for transmission to the optical devices at the 155.52 MHz rate.

The Slave Bus Interface (SBI) connects the Input/Output Cards (IOCs) to the associated switch modules (SSCs). The SBI is split into two busses; a read bus and a write bus. All IOCs receive data on the write bus while all SSCs receive data on the read bus.

DCC overhead is routed to and from the Framer to a DCC Field Programmable Gate Array (FPGA) on the OC3-12P. The DCC enables processors to communicate between multiple shelves.

The OC3-12P receives two copies of a 50 MHz clock, one from each CCC. The clocks are point-to-point PECL pairs.

Two reset monitors are supported by the OC3-12P; one monitors power and the other monitors a 25 MHz clock. When the power monitoring device detects a power level not in the required 3.3 V range, a reset is administered. During power up, the reset is kept active for approximately 350 ms for the power supply to stabilize before being released.

The OC3-12P receives a system clock from the Timing Card (TC) and is fed into two subsystems: System Clock Generator and Frame Pulse Generator with an 8 KHz loop clock reference. The System Clock Generator multiplies the 8KHz clock into a 77.76 MHz IOC system clock. The Frame Pulse Generator creates an 8 KHz frame pulse to align SONET payloads that pass from the IOC to the SSC.

The I^2C Serial Electronically Erasable Programmable Read Only Memory (EEPROM) interfaces to the SSC and contains data such as board type, serial number, and manufacturing date. Such devices supply nonvolatile storage and allow the user to increase the amount of storage.

UDS-122
LCx 10x 4-Port OC-12 Line Card

PART NUMBER/ MNEMONIC	NAME	CLEI	ECI/BAR CODE	CPR	STATUS
3EM12241AA OC12-4P	LC5 101 4-Port IR OC-12 Line Card	WMOTAXSEAA	126570	L73591	Active
3EM12241AB OC12-4P	LC5 102 4-Port IR OC-12 Line Card	WMOTBBEEAA	130526	W70847	Active

FEATURES AND APPLICATION NOTES

- 4 SONET OC-12 ports
- Half-height (7.25”D x 8.49”H)
- Slots 1–6, 12–17, A and B
- SC-style connectors
- DCC selection
- Line timing source for TC
- SONET performance monitoring
- UPSR and APS protection

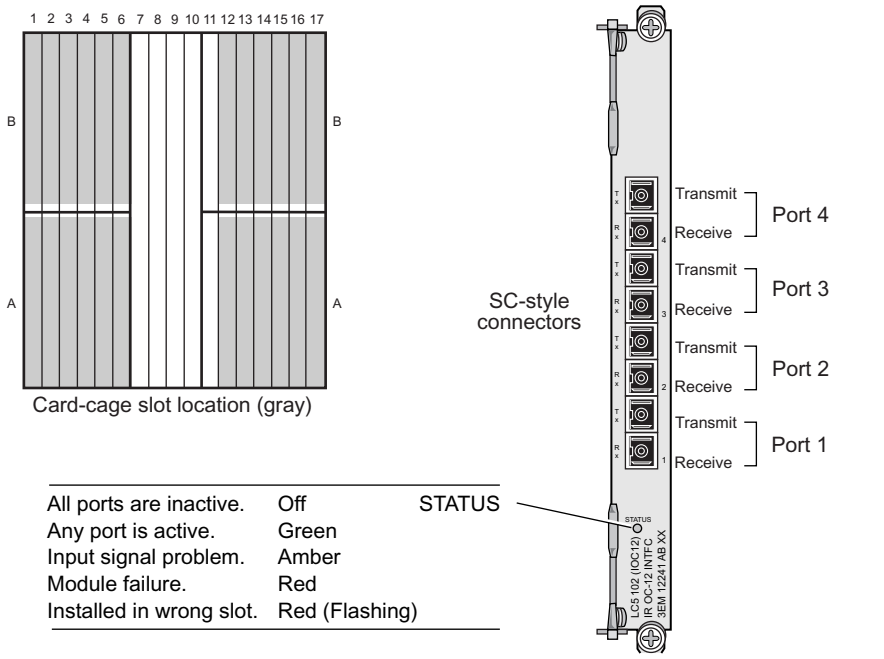
DESCRIPTION

The OC12-4P provides four optical-carrier (OC) level 12, 1310 nm interfaces. It is available with a Single Mode (SM), Intermediate Reach (IR) laser transmitter.

INDICATORS AND CONNECTORS

Figure 122-1 describes the OC12-4P front panel indicators and connectors.

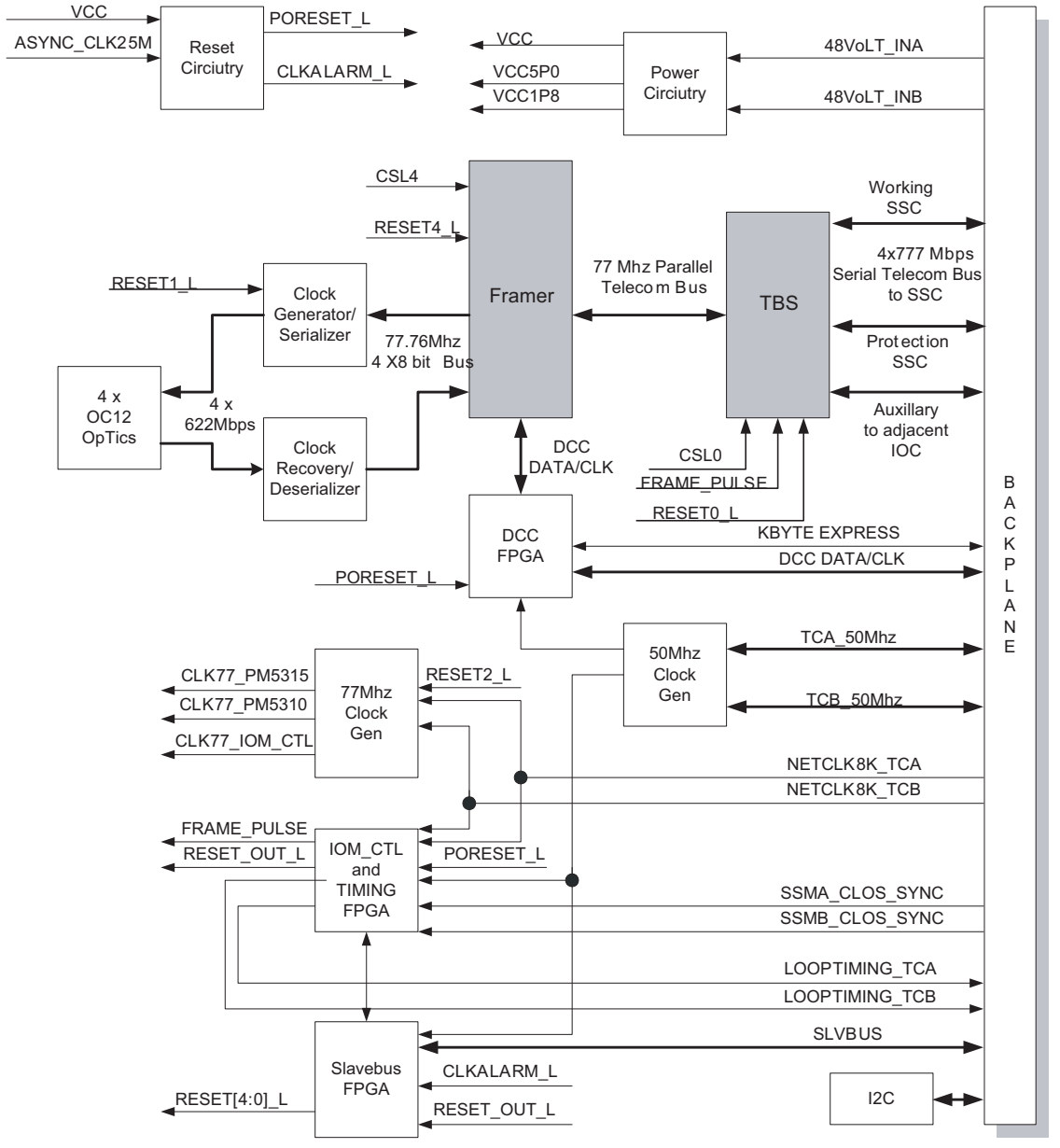
Figure 122-1. OC12-4P Front Panel



FUNCTIONAL OPERATION

Figure 122-2 illustrates the function of the OC12-4P and is followed by a brief description of the OC12-4P functional blocks.

Figure 122-2. OC12-4P Block Diagram



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The OC12-4P transmits 12 STS-1 signals to the SSC through the following module components:

- OC-12 Telecom Bus Serializer
- OC-12 Framer/Processor
- OC-12 Serializer/Deserializer
- Slave Bus Interface
- Data Communications Channel Interface
- Control Clock Distribution
- Reset Control
- System Clock and Frame Pulse Generation
- I^2C PROM

The OC12-4P has three groups of four serial links connection to the backplane. One link connects to the working SSC, the second link connects to the protection SSC, and the third serial link, called the Auxiliary link, connects to the adjacent IOC. These links connect directly to the Telecom Bus Serializer (TBS).

The TBS encodes Telecom Bus data in the receive direction from the Framer to the SCC through a 777.6 Mb/s backplane Telecom Bus. In the transmit direction, the TBS decodes Telecom bus data from the SSC to an outgoing parallel Telecom Bus linking to the Framer. The TBS provides the capacity to carry an STS-12 stream and redundant working and protection streams for protection switching. The TBS uses the auxiliary link to connect to the adjacent IOC for through and ring applications.

The framer receives SONET STS-12s from the SERializer/DESerializer (SERDES) device on the OC3-12P and terminates the transport and path overhead. Transport over head, such as DCC, is extracted and the Synchronous Payload Envelope (SPE) is put on the DROP Telecom Bus for transport to the TBS. The framer receives data on the ADD Telecom Bus and prepares it for transmission at the 155.52 MHz rate to the SERDES device.

The SERDES function is performed using SERDES device with clock recovery. In the deserialization stage, the integrated Phase Locked Loop (PLL) recovers the clock signal from the STS-12 622.08 Mb/s serial data and converts it to an 8 bit, 77.76 MHz bus that is transported to the Framer. In the serialization stage, the function is done in reverse.

The Slave Bus Interface (SBI) connects the IOCs to the associated switch modules (SSCs).

DCC overhead is routed to and from the Framer to a Data Communications Channel (DCC) Field Programmable Gate Array (FPGA) on the OC12-4P. The DCC enables processors to communicate between multiple shelves.

The OC12-4P receives two copies of a 50 MHz clock, one from each CCC. The clocks are point-to-point PECL pairs.

Two reset monitors are supported by the OC12-4P, one monitors power and the other monitors a 25 MHz clock. When the power monitoring device detects a power level not in the required 3.3 V range, a reset is administered. During power up, the reset is kept active for approximately 350 ms for the power supply to stabilize before being released.

The OC12-4P receives a system clock from the TC and feeds it into two subsystems: System Clock Generator and Frame Pulse Generator with an 8 KHz loop clock reference. The System Clock Generator multiplies the 8 KHz clock into a 77.76 MHz Input/Output Card (IOC) system clock. The Frame Pulse Generator creates an 8 KHz frame pulse to align SONET payloads that pass from the IOC to the SSC.

The I^2C Serial Electronically Erasable Programmable Read-Only Memory (EEPROM) accesses the SSC and contains data such as board type, serial number, and manufacturing date. Such devices supply nonvolatile storage and allow the user to increase the amount of storage.

UDS-123
LCxxx xxx 1-Port OC-48 Line Card

PART NUMBER/ MNEMONIC	NAME	CLEI	ECI/BAR CODE	CPR	STATUS
3EM12250AA OC48-1P	LC10D 030 1-Port XLR OC-48 Line Card, DC-SM-SC, 1553.33 nm	WMOTAXXEAA	126578	L73533	Active
3EM12250AB OC48-1P	LC10D 130 1-Port XLR OC-48 Line Card, DC-SM-SC, 1553.33 nm	WMOTBBKEAA	130531	W70865	Active
3EM12251AA OC48-1P	LC10D 031 1-Port XLR OC-48 Line Card, DC-SM-SC, 1552.52 nm	WMOTAXYEAA	126579	L73533	Active
3EM12251AB OC48-1P	LC10D 131 1-Port XLR OC-48 Line Card, DC-SM-SC, 1552.52 nm	WMOTBBLEAA	130567	W70865	Active
3EM12252AA OC48-1P	LC10D 032 1-Port XLR OC-48 Line Card, DC-SM-SC, 1551.72 nm	WMOTAXZEAA	126580	L73533	Active
3EM12252AB OC48-1P	LC10D 132 1-Port XLR OC-48 Line Card, DC-SM-SC, 1551.72 nm	WMOTBBMEAA	130572	W70865	Active
3EM12253AA OC48-1P	LC10D 033 1-Port XLR OC-48 Line Card, DC-SM-SC, 1550.92 nm	WMOTAU4EAA	126489	L73533	Active
3EM12253AB OC48-1P	LC10D 133 1-Port XLR OC-48 Line Card, DC-SM-SC, 1550.92 nm	WMOTBBNEAA	130575	W70865	Active
3EM12254AA OC48-1P	LC10D 035 1-Port XLR OC-48 Line Card, DC-SM-SC, 1549.31 nm	WMOTAX0EAA	126581	L73354	Active
3EM12254AB OC48-1P	LC10D 135 1-Port XLR OC-48 Line Card, DC-SM-SC, 1549.31 nm	WMOTBBPEAA	130576	W70865	Active
3EM12255AA OC48-1P	LC10D 036 1-Port XLR OC-48 Line Card, DC-SM-SC, 1548.51 nm	WMOTAX1EAA	126583	L73354	Active
3EM12255AB OC48-1P	LC10D 136 1-Port XLR OC-48 Line Card, DC-SM-SC, 1548.51 nm	WMOTBBREAA	130577	W70865	Active

PART NUMBER/ MNEMONIC	NAME	CLEI	ECI/BAR CODE	CPR	STATUS
3EM12256AA OC48-1P	LC10D 037 1-Port XLR OC-48 Line Card, DC-SM-SC, 1547.72 nm	WMOTAX2EAA	126584	L73354	Active
3EM12256AB OC48-1P	LC10D 137 1-Port XLR OC-48 Line Card, DC-SM-SC, 1547.72 nm	WMOTBBSEAA	130590	W70865	Active
3EM12257AA OC48-1P	LC10D 038 1-Port XLR OC-48 Line Card, DC-SM-SC, 1546.92 nm	WM31808KAA	128328	L73354	Active
3EM12257AB OC48-1P	LC10D 138 1-Port XLR OC-48 Line Card, DC-SM-SC, 1546.92 nm	WMOTBBTEAA	130531	W70891	Active
3EM12301AA OC48-1P	LC7D 101 1-Port SR OC-48 Line Card, DC-SM-SC	WMOTAXUEAA	126573	L73531	Active
3EM12301AB OC48-1P	LC7D 102 1-Port SR OC-48 Line Card, DC-SM-SC	WMOTBBGEAA	130528	W70862	Active
3EM12302AA OC48-1P	LC7ID 101 1-Port IR OC-48 Line Card, DC-SM-SC	WMOTAXVEAA	126574	L73532	Active
3EM12302AB OC48-1P	LC7ID 102 1-Port IR OC-48 Line Card, DC-SM-SC	WMOTBBHEAA	130529	W70863	Active
3EM12312AA OC48-1P	LC8D 101 1-Port LR OC-48 Line Card, DC-SM-SC	WMOTAXWEAA	126575	H73771	Active
3EM12312AB OC48-1P	LC8D 102 1-Port LR OC-48 Line Card, DC-SM-SC	WMOTBBJEAA	130530	W70864	Active

FEATURES AND APPLICATION NOTES

- 1 SONET OC-48 port
- Half-high (7.25”D x 8.49”H)
- Slots 1–6, 12–17, A and B
- SC connectors
- Line timing source for TC
- DCC selection
- UPSR, APS, BLSR, and Drop-and-Continue applications
- SONET performance monitoring
- Optical power monitoring (ITU DWDM channel modules only)

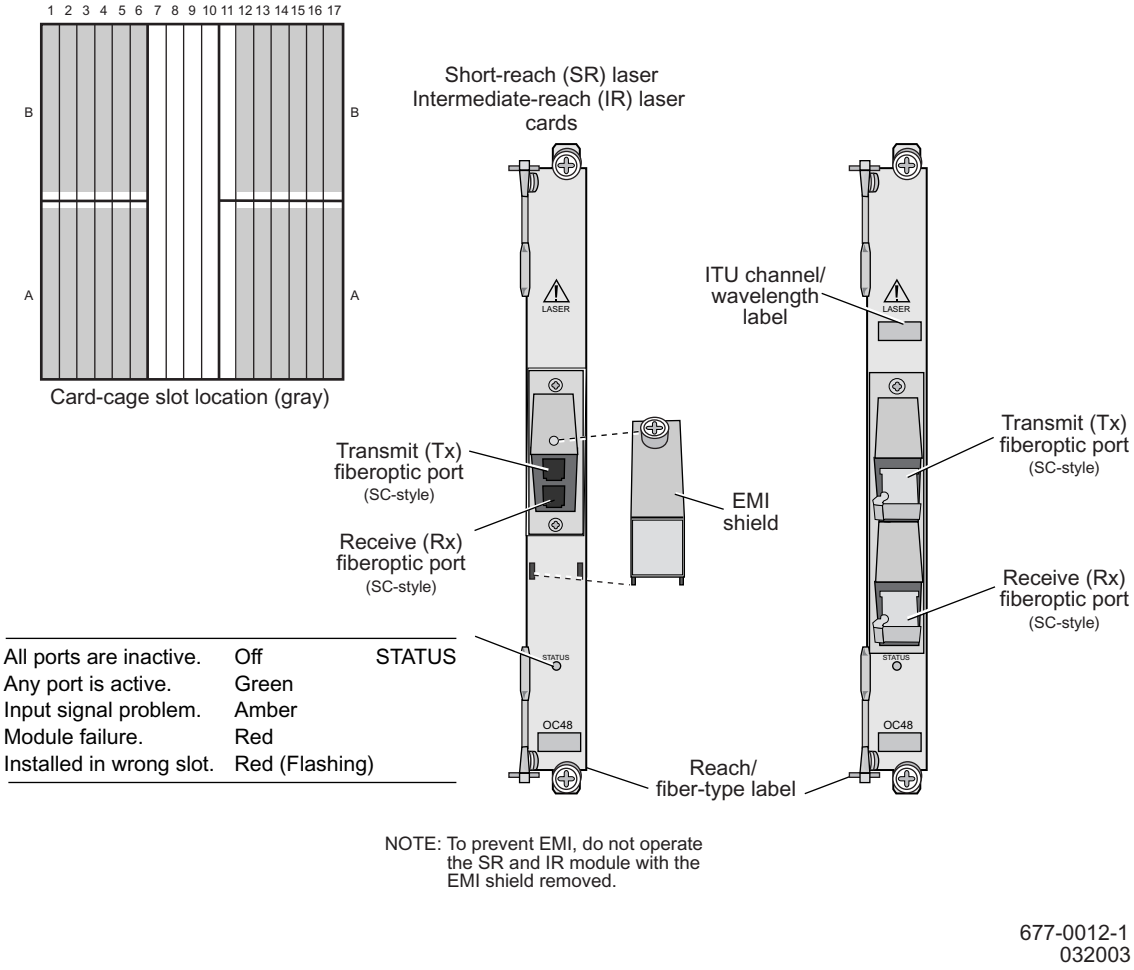
DESCRIPTION

The OC48-1P provides one optical-carrier (OC) level 48 interface. It is available with either a 1310 nm interface or an interface for one of the 32 ITU C-band, DWDM channels on 100 GHz spacing. The 1310 nm interface OC48-1P has either a Short-Reach (SR), Intermediate-Reach (IR), or Long-Reach (LR) laser transmitter. The ITU DWDM channel module has an Extra Long-Reach (XLR) laser transmitter.

INDICATORS AND CONNECTORS

Figure 123-1 describes the OC48-12P front panel indicators and connectors.

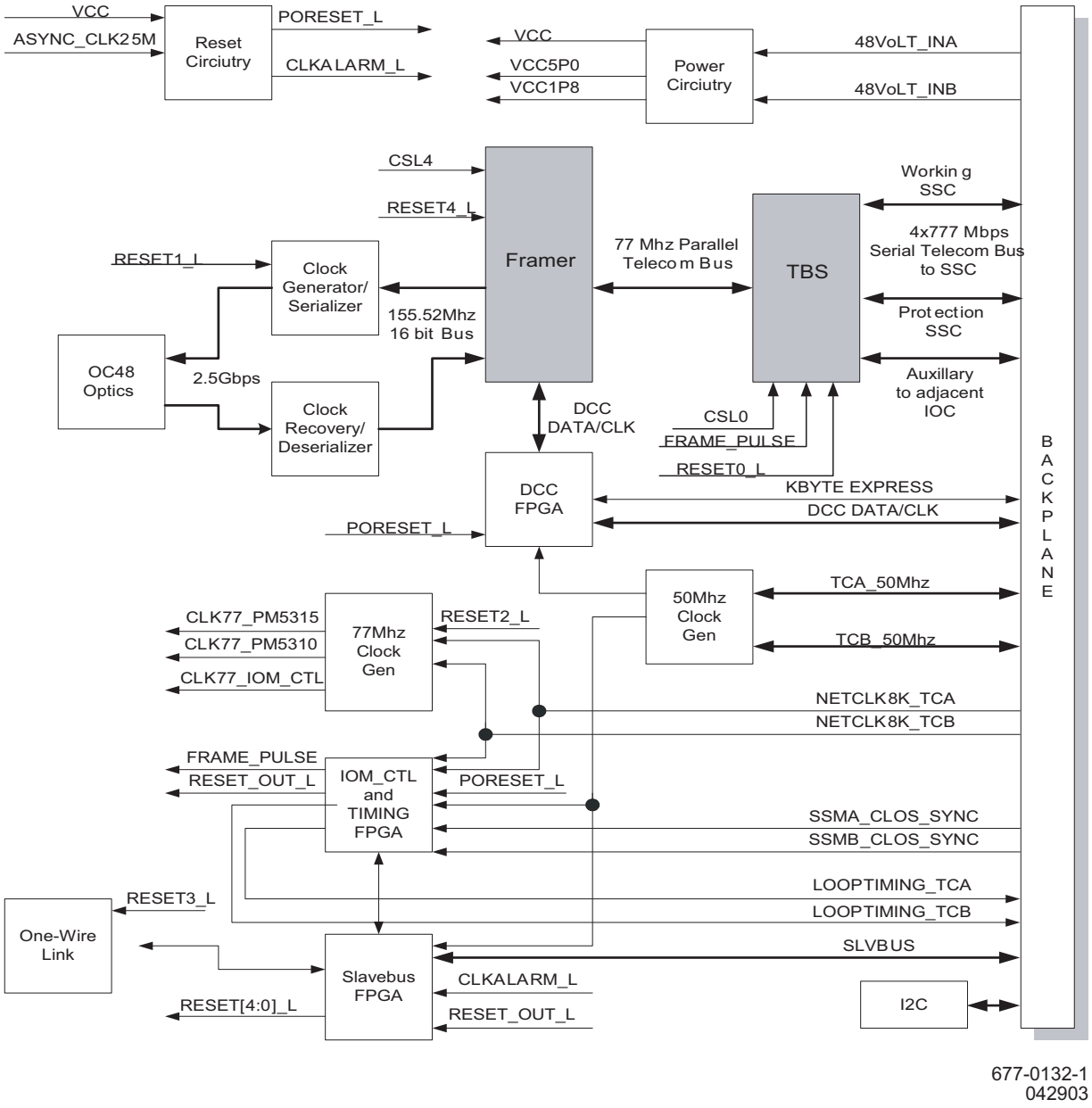
Figure 123-1. OC48-1P Front Panel



FUNCTIONAL OPERATION

Figure 123-2 illustrates the function of the OC48-1P and is followed by a brief description of the OC48-1P functional blocks.

Figure 123-2. OC48-1P Block Diagram



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The OC48-1P transmits 48 STS-1 signals to the SSC through the following module components:

- OC-48 Telecom Bus Serializer
- OC-48 Framer/Processor
- OC-48 SERDES
- Slave Bus Interface
- Data Communications Channel (DCC) Interface
- K-Byte Express
- Control Clock Distribution
- Reset Control
- System Clock and Frame Pulse Generation
- Optical Power Monitor (ITU DWDM channel modules only)
- I^2C PROM
- Add/Drop FPGA

The OC48-1P has three groups of four serial links connection to the backplane. One link connects to the working SSC, the second link connects to the protection SSC, and the third serial link, called the Auxiliary link, connects to the adjacent Input/Output (IOC). These links connect directly to the Telecom Bus Serializer (TBS).

The TBS encodes Telecom Bus data in the receive direction from the Framer to the SCC through 777.6 Mb/s backplane Telecom Bus. In the transmit direction, the TBS decodes Telecom bus data from the SSC to an outgoing parallel Telecom Bus linking to the Framer. The TBS provides the capacity to carry an STS-48 stream and redundant working and protection streams for protection switching. The TBS uses the auxiliary link to connect to the adjacent IOC for through and ring applications.

The framer receives SONET STS-48s from the SERDES device on the OC48-1P and terminates the transport and path overhead. Transport over head, such as DCC, is extracted and the Synchronous Payload Envelope (SPE) is put on the DROP Telecom Bus for transport to the TBS. The framer receives data on the ADD Telecom Bus and prepares it for transmission at the 155.52 MHz rate to the SERDES device.

The SERial/DESerial (SERDES) function is performed using SERDES device with clock recovery. In the deserialization stage, the integrated Phase Locked Loop (PLL) recovers the clock signal from the 2.5 Gb/s serial data and converts it to a 16 bit 155Mb/s parallel bus, which is transported to the Framer. In the serializer stage, the internal clock generator uses the PLL to multiply the 77.76 MHz clock from the Framer to provide the 2.5 Gb/s clock for output retiming. The serializer converts the 155 Mb/s data from the Framer to a 2.5 Gb/s data stream, which is transported to the optic device.

The Slave Bus Interface (SBI) connects the IOCs to the associated switch STS Switch Cards (SSCs).

DCC overhead is routed to and from the Framer to a DCC Field Programmable Gate Array (FPGA) on the OC48-1P. The DCC enables processors to communicate between multiple shelves. The OC48-1P has a single section and line DCC channel for the single OC port. This channel is time Division Multiplexed (TDM) into a single data stream that is initiated on the DCC bus through the backplane to the SSC. Line and section data are provided at the 576 KHz and 192 KHz rates respectively.

In BLSR applications, all optical modules support the K-Byte Express. The K-Byte Express is a connection between pairs of optical modules to pass SONET K-bytes. K-byte signals travel around a BLSR ring to provide fast protection switching decisions.

The OC48-1P receives two copies of a 50 MHz clock, one from each CCC. The clocks are point-to-point PECL pairs.

Two reset monitors are supported by the OC48-1P. One reset monitors power and the other monitors a 25 MHz clock. When the power monitoring device detects a power level not in the required 3.3 V range, a reset is administered. During power up, the reset is kept active for approximately 350 ms for the power supply to stabilize before being released.

The OC48-1P receives a system clock from the TC and feeds it into two subsystems: System Clock Generator and Frame Pulse Generator with an 8 KHz loop clock reference. The System Clock Generator multiplies the 8 KHz clock into a 77.76 MHz IOC system clock. The Frame Pulse Generator creates an 8 KHz frame pulse to align SONET payloads that pass from the IOC to the SSC.

The optical power monitor (ITU DWDM channel modules only) monitors laser bias, laser temperature, and laser power. It uses the Slave bus to communicate with the microprocessor containing an analog to digital converter.

The Add/Drop FPGA delays the IOC auxiliary port transmitter to ensure the TBS is adequately prepared to handle incoming data. The receiver is not affected. The FPGA can be disabled when a reset is initiated.

The I^2C Serial Electronically Erasable Programmable Read Only Memory (EEPROM) interfaces to the SSC and contains data such as board type, serial number, and manufacturing date. Such devices supply nonvolatile storage and allow the user to increase the amount of storage.

UDS-124
LC12D x3x 1-Port LR OC-192 Line Card

PART NUMBER/ MNEMONIC	NAME	CLEI	ECI/BAR CODE	CPR	STATUS
3EM12266AA OC192-1P	LC12D 030 1-Port LR OC-192 Line Card, DC-SM-SC, 1553.33 nm	WMOTAX3EAA	126585	L73358	Active
3EM12267AA OC192-1P	LC12D 031 1-Port LR OC-192 Line Card, DC-SM-SC, 1552.52 nm	WMOTAX4EAA	126586	L73358	Active
3EM12268AA OC192-1P	LC12D 032 1-Port LR OC-192 Line Card, DC-SM-SC, 1551.72 nm	WMI8702FAA	126635	L73358	Active
3EM12269AA OC192-1P	LC12D 033 1-Port LR OC-192 Line Card, DC-SM-SC, 1550.92 nm	WMI870YFAA	126637	L73358	Active
3EM12270AA OC192-1P	LC12D 035 1-Port LR OC-192 Line Card, DC-SM-SC, 1549.32 nm	WMI8804FAA	126638	H73774	Active
3EM12271AA OC192-1P	LC12D 036 1-Port LR OC-192 Line Card, DC-SM-SC, 1548.51 nm	WMI870NFAA	126639	L73358	Active
3EM12272AA OC192-1P	LC12D 037 1-Port LR OC-192 Line Card, DC-SM-SC, 1547.72 nm	WMI890WFAA	126641	L73358	Active
3EM12273AA OC192-1P	LC12D 038 1-Port LR OC-192 Line Card, DC-SM-SC, 1546.92 nm	WMI870PFAA	126642	L73358	Active
3EM20319AC OC192-1P	LC12D 1-port LR OC-192 Line Card, DC-SM-SC, 1550 nm	WMUIAGUCAA	150888	070HNW	Active

FEATURES AND APPLICATION NOTES

- 1 SONET OC-192 port
- Full-height (7.25”D x 18.00”H), Slots 5AB, 6AB, 12AB, 13AB
- Forward Error Correction (FEC)
- SC-style connectors
- Data Communications Channel (DCC) Support
- Line timing source for TC
- ITU DWDM channel interface
- UPSR, APS, BLSR and Drop-and-Continue protection
- SONET performance monitoring

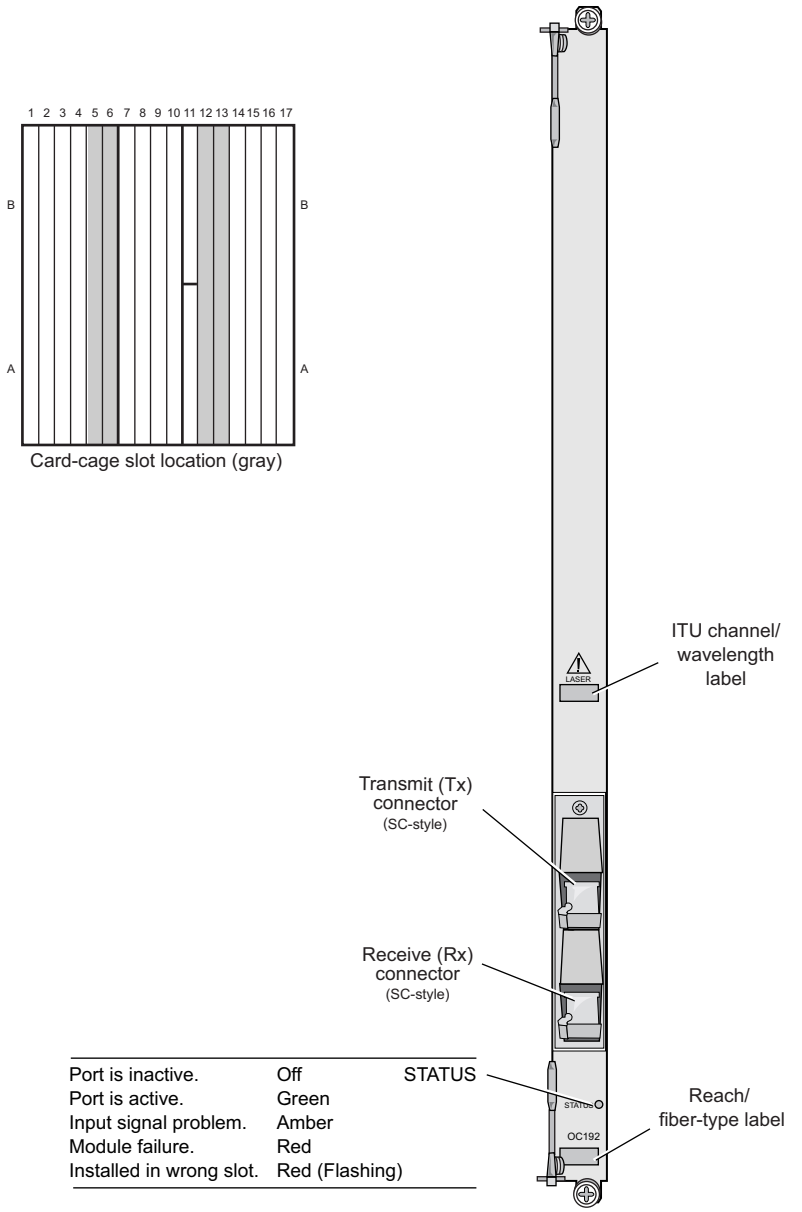
DESCRIPTION

The OC192-1P line card provides one optical-carrier (OC) level 192 interface. It has an ITU DWDM channel interface and uses a Long-Reach (LR) laser transmitter. The OC192-1P installs into full-height slots 5AB, 6AB, 12AB, and 13AB. To accommodate the maximum number of DS3 line modules (192 ports), OC192-1P installs into slots 6AB and 12AB.

INDICATORS AND CONNECTORS

Figure 124-1 describes the OC192-1P front panel indicators and connectors.

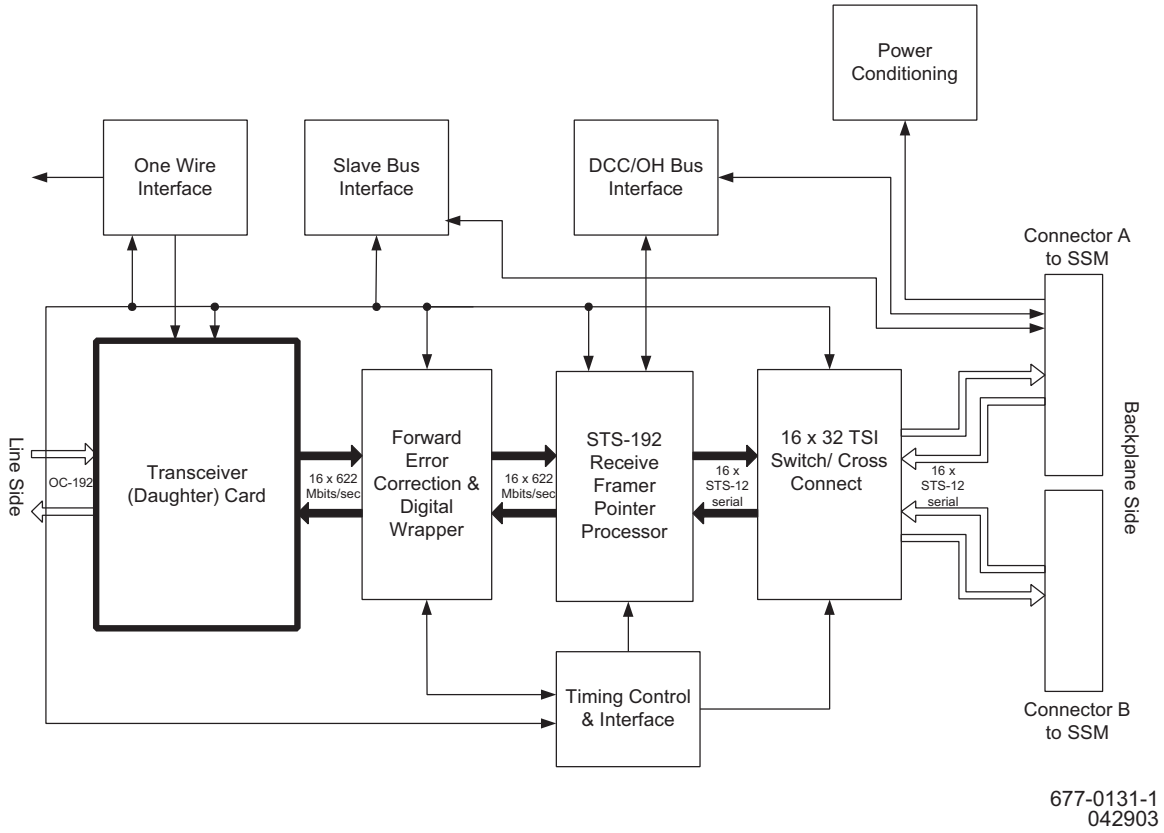
Figure 124-1. OC192-1P Front Panel



FUNCTIONAL OPERATION

Figure 124-2 illustrates the function of the OC192-1P and is followed by a brief description of the OC192-1P functional blocks.

Figure 124-2. OC192-1P Block Diagram



The OC192-1P transmits/receives 192 STS-1s to/from the SSC switch fabric. It is composed of the following main components:

- One Wire Interface
- Slave Bus Controller
- FEC/Digital Wrapper
- Framer
- TSI Switch
- Timing and Control Interface
- DCC + GCC FPGA
- I^2C Serial EEPROM
- Power Conditioning
- Optical Monitoring

The OC192-1P contains a one wire interface that is used as an optical management tool. The one wire interface allows the network management system to determine which modules are connected to the OC-192 fiber links.

The Slave Bus is the interface between the OC192-1P and the STS-1 Switch Card (SSC). The slave bus contains a read bus and a write bus, where the SSCs receive on the read bus and the OC192-1P receives on the write bus.

The Forward Error Correction (FEC)/Digital Wrapper provides the following capabilities:

- Accepts FEC encoded input data, corrects errors, then provides FEC output data to the system
- Outputs noncoded data with or without correcting errors
- Accepts noncoded input data providing encoded FEC output data
- Accepts/outputs encoded data - essentially not using FEC

The Digital Wrapper functions separately than the FEC. Here, overhead bytes for section and path are programmable. Also, the Digital Wrapper supplies error generation features and data used for internal performance monitoring. The FEC/Digital wrapper is controlled by the slave bus.

The Framer translates between STS-192 and STS-12 data rates. The line side of the FEC/Digital Wrapper receives 16 bit data at the 622 Mb/s rate and the backplane has a 16 bit, serial STS-12 interface. The Framer provides data alignment and accommodates for slight variations in data rate between the line and backplane sides. The Framer also terminates section, line and path information along with supporting any valid mix of STS-1 and STS-3c to STS-192c concatenated payloads.

Two different I/O data interfaces exist between the Framer and the Time Slot Interchange (TSI) switches. Two FPGA devices facilitate the translation between the two interfaces. The first FPGA device interfaces to the line side of the Framer. The second FPGA device encodes data from the incoming parallel Telecom Bus (or Time Slot Interchange) to a set of four 777.6 Mb/s serial telecom Bus links. The core of the first FPGA device supports the high-speed interface to the eight full-duplex 622 Mb/s serial data links to and from the Framer. It is programmed to support two Quad Telecom Bus sections for interfacing the TBS.

The TSI switch allows the OC192-1P to route any input time slot to any output time slot within the STS-1 granularity. The switch provides loopback capabilities, AIS insertion, and byte interleaving. Switch data is transferred between the OC192-1P and backplane at the 777 MHz bit rate.

The Timing and Control interface generates an external transmit clock reference to reduce and/or eliminate jitter propagation. The interface reduces jitter on the high frequency 622/666 MHz clock.

The OC192-1P has two I^2C serial Electronically Erasable Programmable Read-Only Memory (EEPROM) devices. The first serial EEPROM resides on the transceiver and contains information such as laser type and model number. The second serial EEPROM resides on the mother board and is preprogrammed with information such as module revisions and options.

Optical Monitoring provides module information such as received power, temperature, module bias points as well as capability to control the power and chip bias of the laser.

UDS-125
SSC 10x 80 Gb STS Switch Card

PART NUMBER/ MNEMONIC	NAME	ICS	CLEI	ECI/BAR CODE	CPR	STATUS
3EM12295AA SSC	SSC 101 80 Gb STS Switch Card	01	WMEDK0MDAC	115643	E73528	Inactive
3EM12295AB SSC	SSC 102 80 Gb STS Switch Card	01	WMEC903AAA	119518	R73289	Inactive
3EM12295AB SSC	SSC 102 80 Gb STS Switch Card	02	WMEC905AAA	126257	R73289	Inactive
3EM12295AC SSC	SSC 103 80 Gb STS Switch Card	01	WMUCALTBAA	130060	W70693	Active
3EM12295AD SSC	SSC 104 80 Gb STS Switch Card	01	WMUCAP7BAA	136940	W73913	Active

FEATURES AND APPLICATION NOTES

- 80 Gb/s nonblocking STS switch
- Redundancy
- 128 DCC channels (however, system software limits system maximum to 66 DCCs—32 line DCCs and 34 section DCCs)
- Audible and visual alarms
- Hitless protection switching
- Full-height, Slots 7 and 8
- 50 MHz clock distribution
- SSC 102 ICS 01 added a node reset to the SSC 101 design.
- SSC 102 ICS 02 added a sync enhancements to the SSC 102 ICS 01 design.
- SSC 103 has the following enhancements over SSC 102 ICS 02:
  - Improved 48 V over/under power performance
  - Improved power efficiency
  - Improved signal integrity
  - Protected/monitored power to backplane
  - Power monitoring and clock activity detector
  - Enhanced lever (most recent manufacturing revision)
- SSC 103 PN 3EM12295AC has 128MB of SWC RAM.
- SSC 104 PN 3EM12295AD has 256MB of SWC RAM.

DESCRIPTION

The SSC is a full-height common module that is installed into slots 7 and 8 of the 1677 SONET Link shelf. The SSC is 9.48 inches deep x 18.00 inches high. Front panel LEDs indicate normal operating conditions and alarm events. An RJ-11 connector is provided for Switch Controller (SWC) and DCC Controller (DCC) diagnostic connections.

INIDICATORS AND CONNECTORS

See figure 125-1 for descriptions of the SSC front-panel indicators and connectors. See figure 125-2 for an illustration of the enhanced lever on the SSC 103.

Figure 125-1. SSC Front-Panel

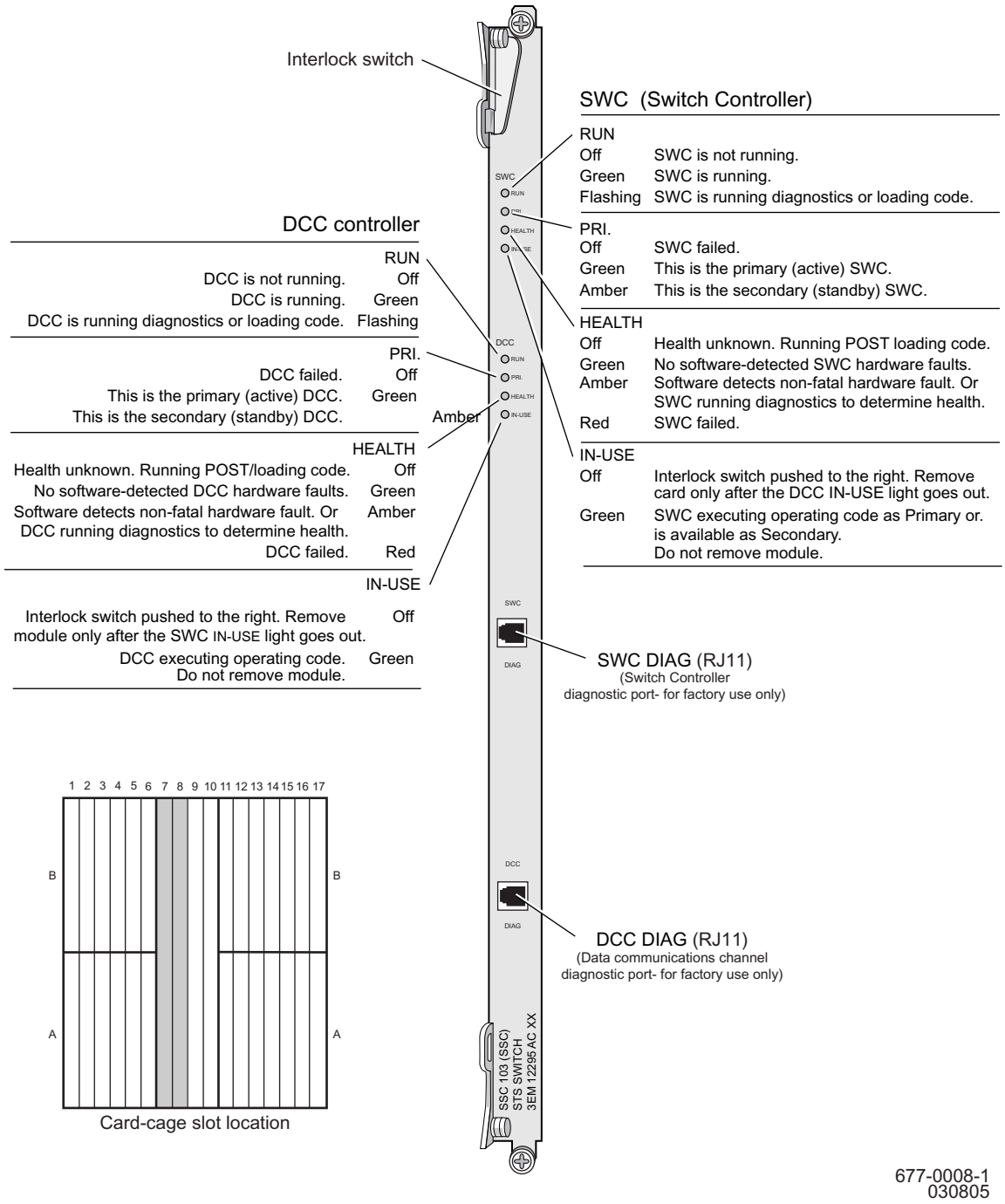
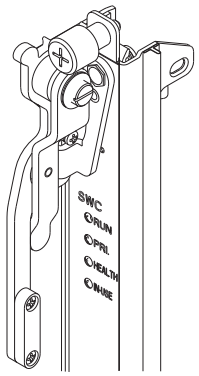


Figure 125-2. SSC 103 Enhanced Lever



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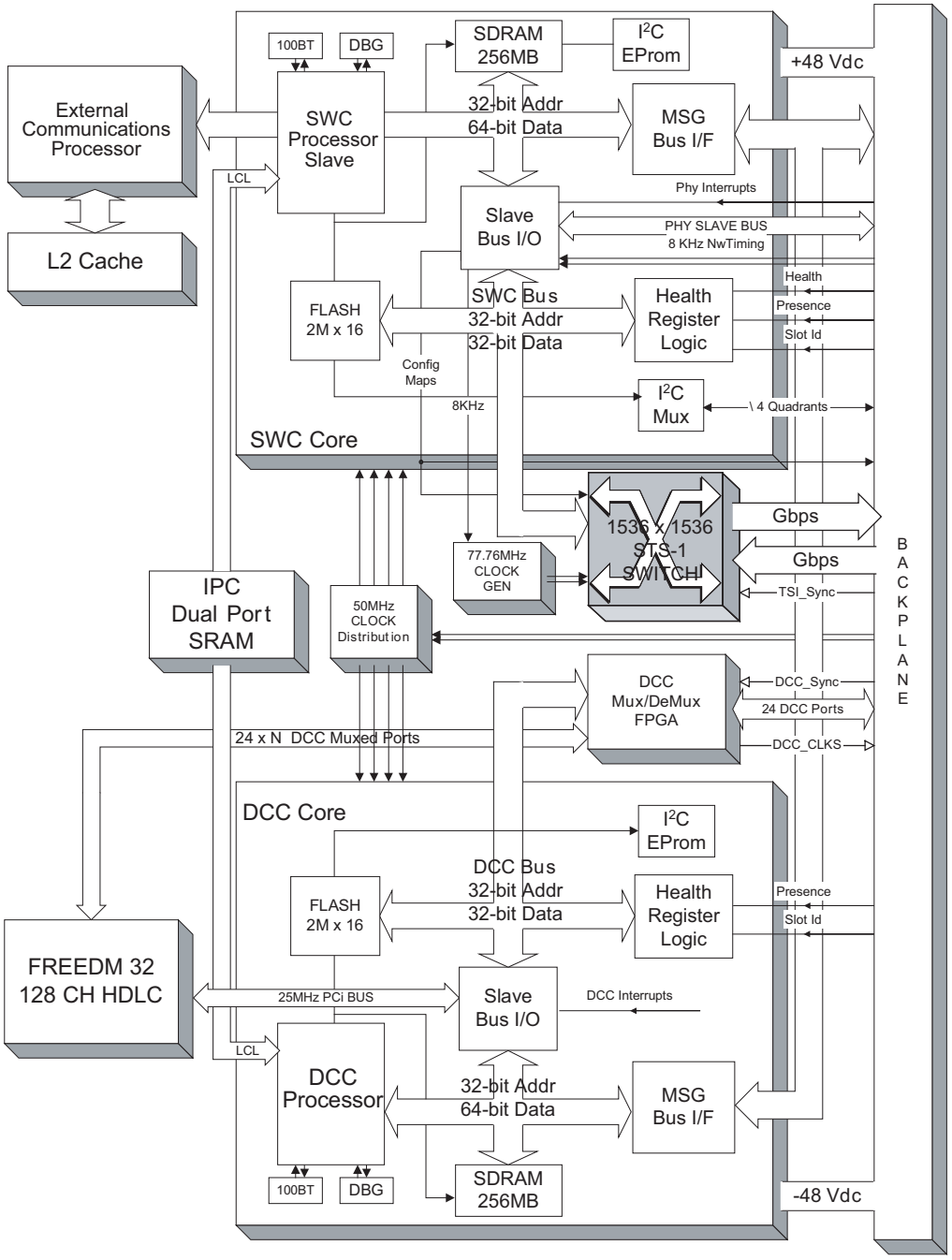
FUNCTIONAL OPERATION

The STS Switch Card (SSC) is a full-height module that manages the switch fabric and the data communications channel through two controller subsystems: the SWitch Controller (SWC) subsystem and the Data Communications Channel (DCC) Controller subsystem. Each subsystem has its own processor and status lights. The SWC controls the center-stage 80-Gbps switch and all Input/Output Cards (IOCs) in the node. It sets up the 1536 x 1536 (80 Gbps) switch matrix that routes network traffic within the node from one IOC port to another. The DCC is responsible for selecting and switching 128 DCC channels from any optical input. It permits network administration, alarm surveillance, provisioning, and control of a network from a central location. The DCC controller can communicate over the section and line DCC from any optical line up to a maximum of 128 section DCCs or 96 line DCCs. (However, the system software limits the system maximum to 66 DCCs—32 line DCCs and 34 section DCCs.) Both the SWC and the DCC obtain their software images from the flash disks on the Common Control Card (CCC).

Because the SWC and DCC controller are separate functions, but both operate on the same SSC module, if a fatal failure occurs in either circuit, the entire SSC is considered to have failed and processing will switch to the redundant SSC. Both the SWC and the DCC controller on the primary SSC are active, and both controllers on the secondary SSC are in standby. A 1677 SONET Link minimum configuration requires one SSC in either slot.

Figure 125-3 illustrate the function of the SSC and is followed by a brief description of the SSC functional blocks.

Figure 125-3. 80 Gb/s STS Switch Fabric Block Diagram



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The SSC performs two processing functions, one on the SWC and one on the DCC. These processing functions are performed using the following common components:

- Communications Processor
- SDRAM
- Flash EPROM
- Diagnostic port
- Message Bus Interface
- Slave Bus Interface
- Dual Port RAM
- I^2C Bus
- Interrupt Logic
- Health Monitoring

The SSC contains an embedded communications controller that has two external buses to accommodate bandwidth requirements from the system core and communications channels. The communications controller is composed of three major functional blocks:

- Microprocessor
- System Interface Unit (SIU)
- Communications Processor Module (CPM)

The microprocessor is a high-performance low-power microprocessor that provides 32-bit effective addresses, integer data types of eight, 16, and 32 bits. It has a 64-bit split-transaction external data bus that is connected directly to the external communications controllers. The microprocessor also has an internal debug processor that allows access to internal scan chains for debugging purposes or can be used as a serial connection to the microprocessor for emulator support.

The SIU contains is a parallel system bus configurable to a 64-bit data width. The SIU arbitrates between internal components able to access the bus. It can be disabled, and an external arbiter can be used if necessary. The SIU also contains a memory controller supporting 12 memory banks allocated for system or local buses as well as a Test Access Port (TAP).

The CPM supports high bit rate protocols such as Fast Ethernet. The CPM performs lower layer tasks and DMA control functions on the local bus. A Serial Peripheral Interface (SPI), I^2C bus controllers, and Time-Slot Assigners (TSA) are also features of the CPM.

Two 32Mx64 bit Synchronous Dynamic RAM (SDRAM) Small-outline Dual In-line Memory Modules (SODIMMs) are supported by both SWC and DCC processors. The two SDRAM SODIMMs allow the SSC to support memory sizes of 64 MB, 128 MB, 256 MB, and 512 MB. An SDRAM address mux is present between the 60X bus and the SDRAM and is required when the communication controller is run in the 60x interface bus mode. The SDRAM uses I^2C interfaces for identification. A Phase Locked Loop (PLL) supplies clock to the SDRAMs from one clock input. The SSCs must have at least 256M RAM installed to support the DS0G 101 DS0 Groomer (DS0G), if installed.

The SSC supports a 4 MB flash device that is upgradable to 16 MB with symmetrically blocked 128K sector sizes. Code stored in the flash supplies the PowerPC the initial reset vector, execution of power-up diagnostics, the system communicator driver, and the boot routine.

Interrupt logic merges internal and external interrupt states for presentation. Interrupt states are latched and made available through status registers. Features such as masking, clear on read, and polarity are supported but are dependant on software.

The Message Bus Interface (MBI) provides the redundant communication link between the SSC and the CCCs. On the SSC, there are two Message Bus Chip interfaces, one for SWC and the other for DCC. The two are multiplexed together and sent onto the backplane. Each MBI requires a centralized arbitration resource.

A Slave Bus Master manages handles all traffic in and out of the following attached buses:

- SWC Local Bus—Interfaces to Time Slot envelopes (TSEs) and provides FLASH memory and Health registers to processor
- DCC Local Bus—Interfaces to DCC Mux/Dmux FPGA and provides FLASH memory and health registers to processor
- PHY Slave Bus—Interfaces switch processor to all IOC in system
- PCI Local Bus—Provides PCI interface to the FREEDM-32 HDLC when operating on the DCC core.

Health Monitoring is provided both globally and locally. Global monitoring is performed by both the SWC and DCC. Each requires SlotID and Presence bit monitoring, but only the SWC is needed to monitor health bits.

The SDRAM is a 256 byte device containing the board serial number and build date information and is accessed through the I^2C interface.

Although the SSC subsections perform common functions, each subsection (SWC and DCC) has its own set of unique components.

SWC Components

The SWC subsystem contains the following components:

- Processor
- Switch Operation
- Switch Interconnection
- Synchronization
- Utilization

The enhanced processor provides performance enhancement and offers the possibility of a dual processor operation. The processor saves recently used page address translations. L2 cache is implemented with an on-chip two-way tag memory with external, DRAMs for data storage. The processor has a 32 bit address bus and a 32/64 bit data bus.

Switching operation is performed in the second stage of the three stage switch. Here, the 128x128 STS-12 switch fabric interconnects all IOCs in the system completing all three stages of the switch. In this second stage, rearrangement in time and space is done by filling in time slot memory maps. The time slot memory map is programmed by the CPU interface port.

The SSC initiates one synchronization signal, called the CONFIG signal, to support the System Interface for the IOCs. The CONFIG signal must be asserted after transferring TSI map data to any of the switch stages through the Slave Bus Master. CONFIG is an asychronous input with no setup/hold dependencies on other signals and can be asserted through writing the register location. Two other synchronization signals are initiated from the Timing Card (TC) to support the System Interface for the IOCs; one for frame SYNC and one 8KHz network timing.

DCC Components

The DCC subsystem contains the following components:

- Processor
- DCC FPGA
- FREEDM-32 HDLC
- Processor Utilization

In the DCC subsystem, an internal processor is enabled. Tasks running on this device control and process DCC termination of Section and Line Overhead DCC channels from IOCs.

The DCC FPGA takes all IOC DCC streams and concentrates them into specific physical links of the FRame EnginE and Data link Manager (FREEDM-32 HDLC). A channel mapper allows any link to be assigned to any HDLC channel by software provisioning and links are forwarded to the processor. This function is described in the receive direction. The reverse is true for DCC in the transmit direction.

UDS-126
TC x01 Stratum 3 Timing Card II

PART NUMBER/ MNEMONIC	NAME	CLEI	ECI/BAR CODE	CPR	STATUS
3EM12309AA TC	TC 201 Stratum 3 Timing Card	WMEDM0PDAB	119635	P73133	Inactive
3EM12309AB TC	TC 301 Stratum 3 Timing Card	WMUCAFMBAA	126898	T73926	Active

FEATURES AND APPLICATION NOTES

- Half-height (7.25”D x 8.49”H)
- Slots 11A and 11B
- Stratum3 Compliant
- TC 301 has the following enhancements:
  - Improved off-frequency reference rejection
  - Improved reference switching performance
  - Battery input and blown fuse alarms
  - Enhanced lever (most recent manufacturing revision)

DESCRIPTION

The TC provides the timing reference signal for all modules in the node. It derives timing for the system from the Building Integrated Timing Supply (BITS) DS1s or from any optical (OC-*n*) interface. It supports a Stratum-3 quality holdover if the external timing references fail. The TC front panel contains two Timing In connection terminal blocks for connecting two separate external BITS clocks, A-BITS and B-BITS. It also contains two Timing Out connection blocks for connecting two separate BITS clocks to other equipment.

The TC also contains the Ethernet port connection for a remote network management workstation or server as well as an RS-232 console port connection for a local system-console terminal. All input to and output from these ports is managed and processed on the Common Control Card (CCC). A 1677 SONET Link minimum configuration requires one TC in either slot. Redundancy requires a TC in both slots.

The TC Ethernet ports are redundant with only one being active at any given time. The primary CCC only uses the active Ethernet port and switches to the redundant Ethernet port if the active port loses link or the TC interlock switch is opened. A switch does not occur if only a single TC is present in the system. Therefore, only one signal is present on the TC internal Local Area Network (LAN). Switching of BITS timing sources from one TC to the other is independent of the Ethernet port making it possible to use a BITS timing source on one TC and the Ethernet port of the other TC simultaneously. The two Ethernet ports share the same Internet Protocol (IP) address and MAC addresses.

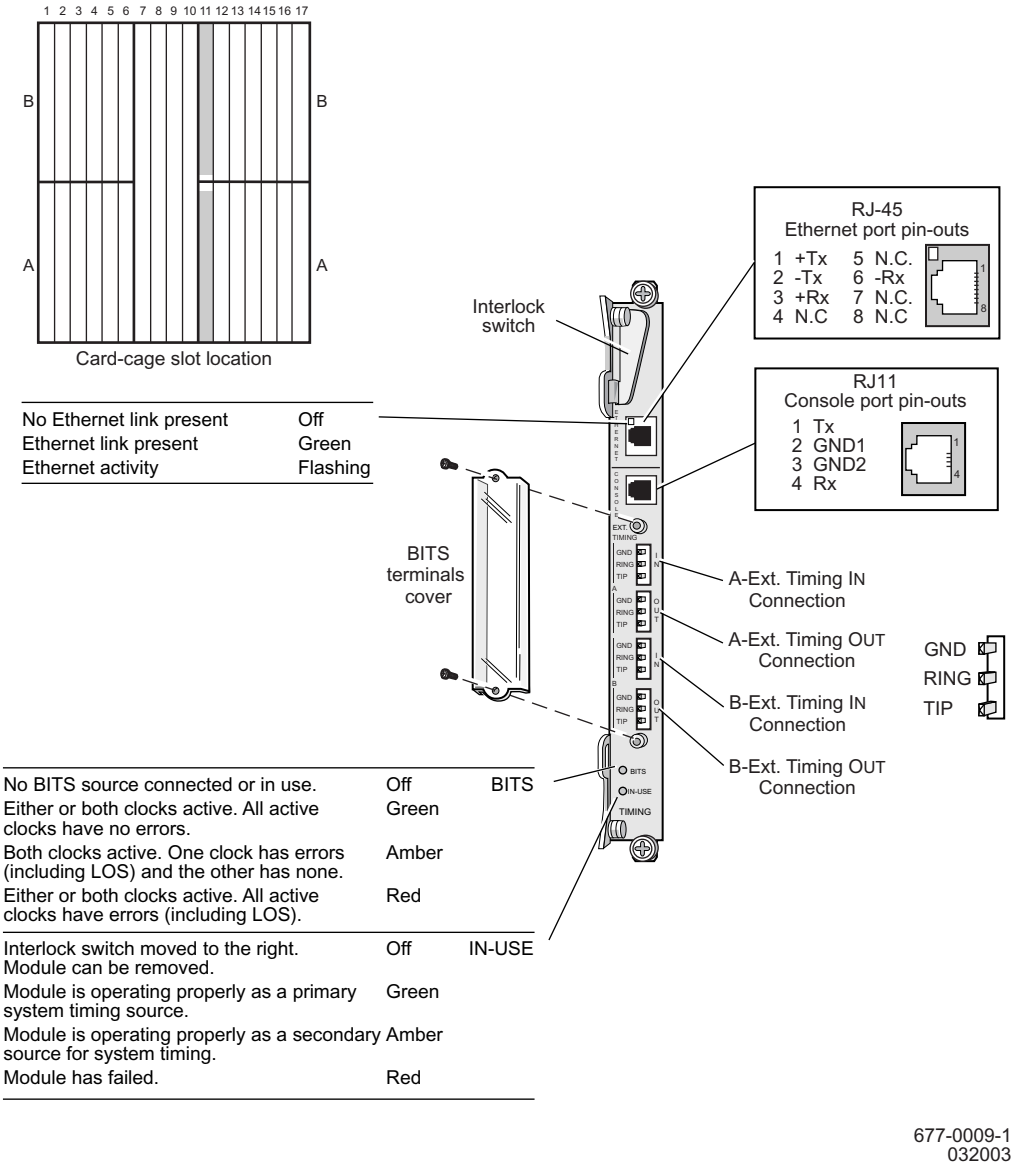
Both Ethernet ports connect directly to the internal LAN. This provides two paths from the 1677 SONET Link to the internal LAN. The protection of the data path from the Network Operating Center (NOC) to the 1677 SONET Link Ethernet interface is determined by the internal LAN design. If redundant paths to the router, switch, or HUB immediately upstream of the 1677 SONET Link are available, then a completely redundant path from the NOC to the 1677 SONET Link exists.

The two versions of the TC can be mixed within the same protection group.

INDICATORS AND CONNECTORS

See figure 126-1 for descriptions of the TC front panel indicators and connectors. See figure 126-2 for an illustration of the enhanced lever on the TC 301.

Figure 126-1. Timing Card Front Panel

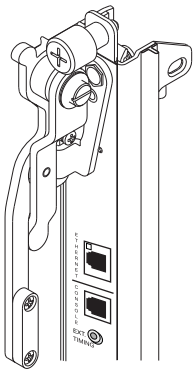


No Ethernet link present	Off
Ethernet link present	Green
Ethernet activity	Flashing

No BITS source connected or in use.	Off	BITS
Either or both clocks active. All active clocks have no errors.	Green	
Both clocks active. One clock has errors (including LOS) and the other has none.	Amber	
Either or both clocks active. All active clocks have errors (including LOS).	Red	
Interlock switch moved to the right. Module can be removed.	Off	IN-USE
Module is operating properly as a primary system timing source.	Green	
Module is operating properly as a secondary source for system timing.	Amber	
Module has failed.	Red	

677-0009-1
032003

Figure 126-2. TC 301 Enhanced Lever

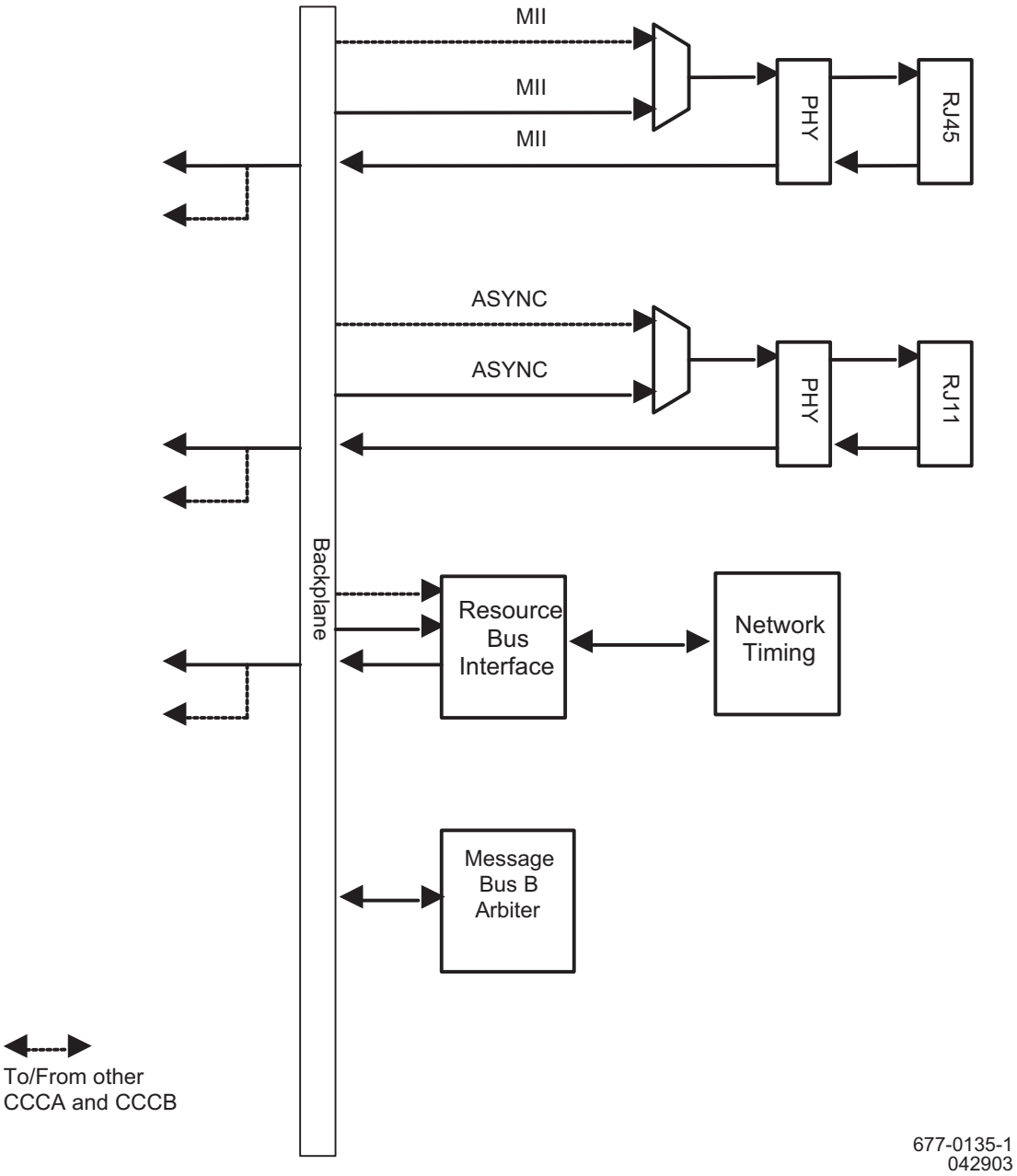


677-0344-1
041905

FUNCTIONAL OPERATION

Figure 126-3 illustrates the function of the TC and is followed by a brief description of the functional blocks.

Figure 126-3. TC Block Diagram



The TC provides Network Timing to the system through the following main components:

- TC Resource Bus Interface
- Message Bus B Arbitration
- Timing block

The Resource Bus Interface (RBI) interfaces RBI messages translated from the CCC to the Timing logic. This function translates memory operation or DMA controller operations into ISA bus operations. ISA bus slave resources on both TCs are visible to the primary CCC and appear in two different memory regions. The RBI detects failed hardware and insertion/removal events and relays these events through read/write operations.

Message Bus B arbitration is performed on each TC, with Message Bus A arbitration performed on the CCC. Both arbiters receive all requests, but only the CCC initiates granted signals.

The Timing block performs two types of clocking; Network and CLOSSYNC. In network clocking, the TC implements stratum3 clocking and distributes the stratum3 compliant, 8KHz clock to all modules in the system. In CLOSSYNC clocking, the TC provides an 8KHZ clock that is synchronized to a 77.76 MHz output clock. The system modules use this clock to create a pulse by sampling the signal with the local 77.76 MHz clock.

Nine interrupts sources are available on the TC and all are merged into a single interrupt sent back to the CCC. Interrupts are observable in the Interrupt Status Register as well as the LOS Status Change Register.

UDS-127
TMUX x01 2.5 Gb/s Transmux

PART NUMBER/ MNEMONIC	NAME	CLEI	ECI/BAR CODE	CPR	STATUS
3EM12308AA TMUX	TMUX 201 2.5 Gb/s Transmux	WM1DD6YCAA	126646	M73387	Active
3EM12308AB TMUX	TMUX 301 2.5 Gb/s Transmux	WM1DDCXCAA	122854	M73387	Active

FEATURES AND APPLICATION NOTES

- Performs DS3-structured STS-1 to VT-structured STS-1 translation
- Provides 2.5 Gb/s of transmultiplex capacity
- Accommodates STS-24 and STS-48 data rates
- Accommodates DS3 and VT1.5 signal structures
- TMUX 301 adds battery input and blown fuse alarms over TMUX 201 design.

DESCRIPTION

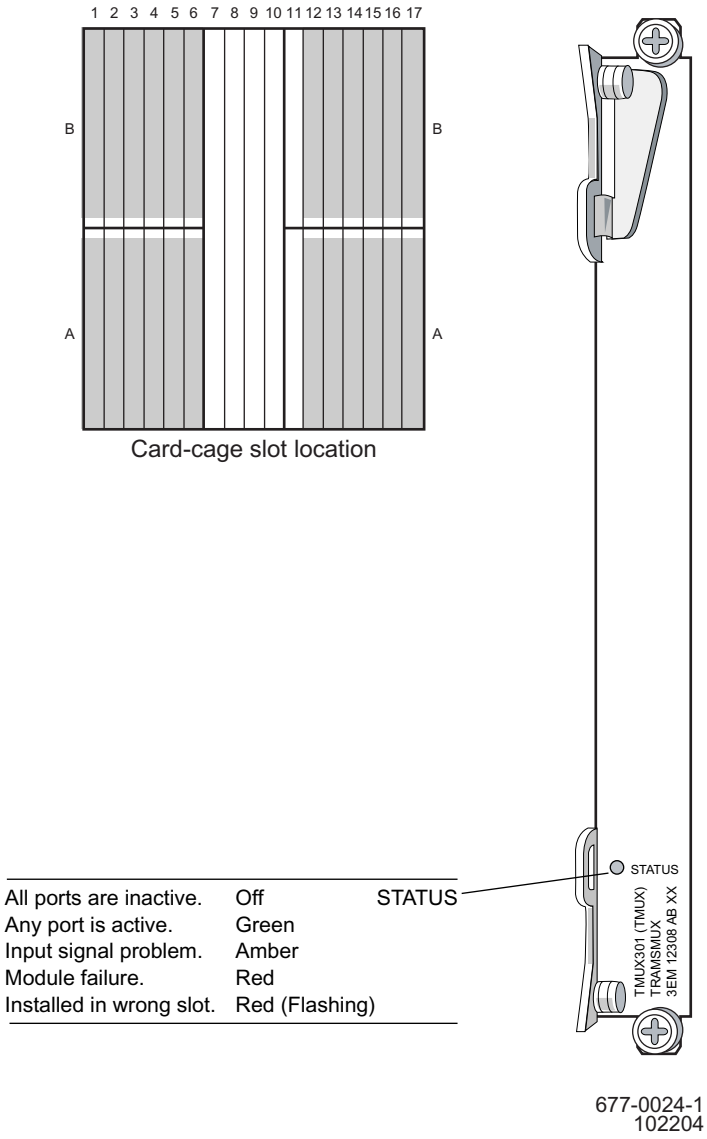
The 2.5 Gb/s TMUX x01 Transmux (TMUX) module is a half-height module that is 7.25 inches deep and 8.49 inches high. It is capable of performing DS3-structured STS-1 to VT-structured STS-1 translation, DS3 DS1 path monitoring, and Virtual Tributary (VT) DS1 path monitoring. In a high-capacity slot (5A, 5B, 6A, 6B, 12A, 12B, 13A, or 13B), the TMUX supports 48 STS-1 pairs.

The two versions of the TMUX can be mixed within the same protection group.

INDICATOR

See figure 127-1 for a description of the front-panel indicator on a typical TMUX.

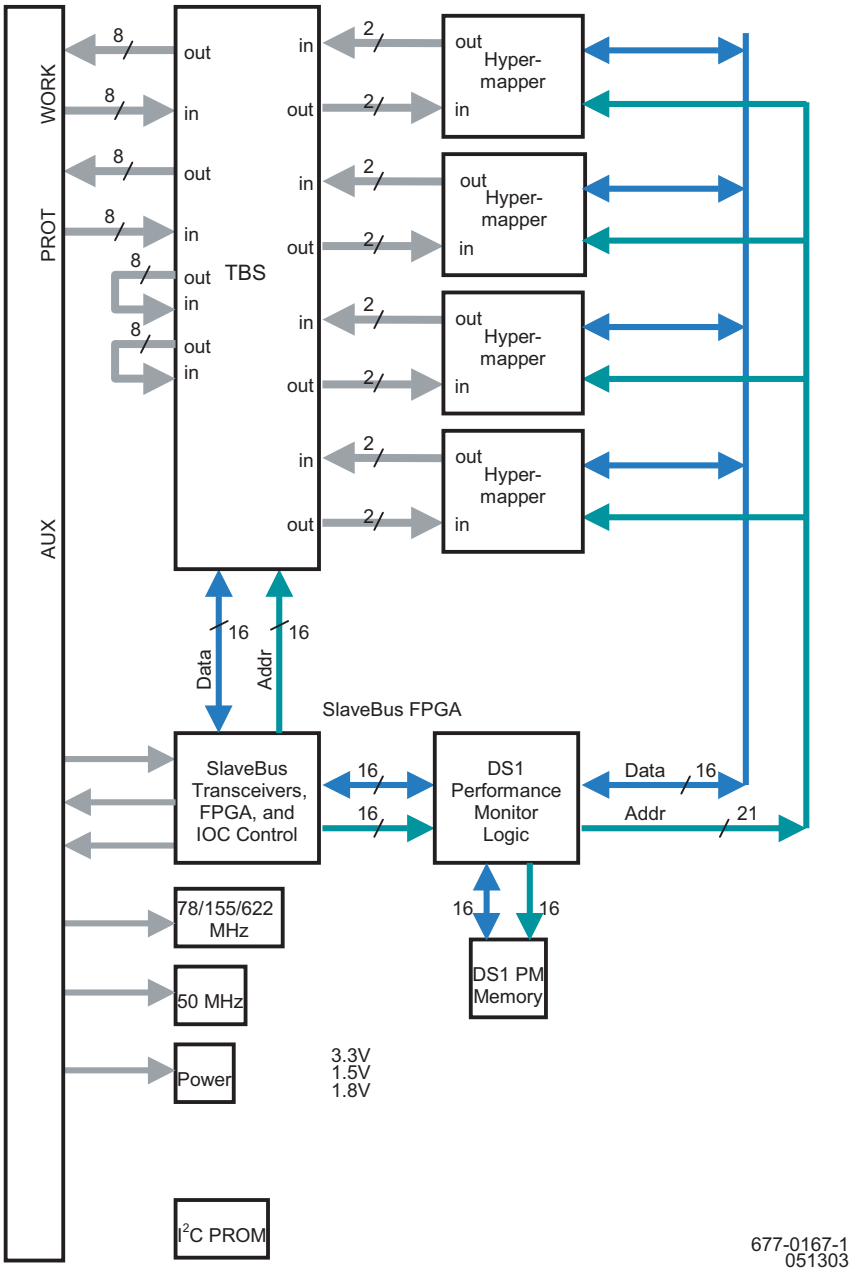
Figure 127-1. Typical TMUX Front Panel



FUNCTIONAL OPERATION

See figure 127-2 for a simplified block diagram of the TMUX.

Figure 127-2. 2.5 Gb/s TMUX Block Diagram



The TMUX is used to convert M13 or C-bit DS3s (carried in an electrical DS3, an EC1, or an OC-*n*) to DS1s that can be independently switched and groomed by VT switches. The TMUX can accept signals from any IOC on the same shelf. When operating as a transmultiplexer, it terminates the DS3 path and supports performance monitoring and maintenance signaling capabilities. The TMUX card can also accept VT1.5 signals to provide access to the DS1 signal

for Performance Monitoring (PM) and maintenance signaling. The DS3 is provided to the TMUX within an STS-1 through the SSC from an IOC. The DS3 is extracted from the STS, demultiplexed to DS1s, then mapped to VT1.5s to be switched by the VSC 101 5 Gb/s VT1.5 Switch Card (VSC).

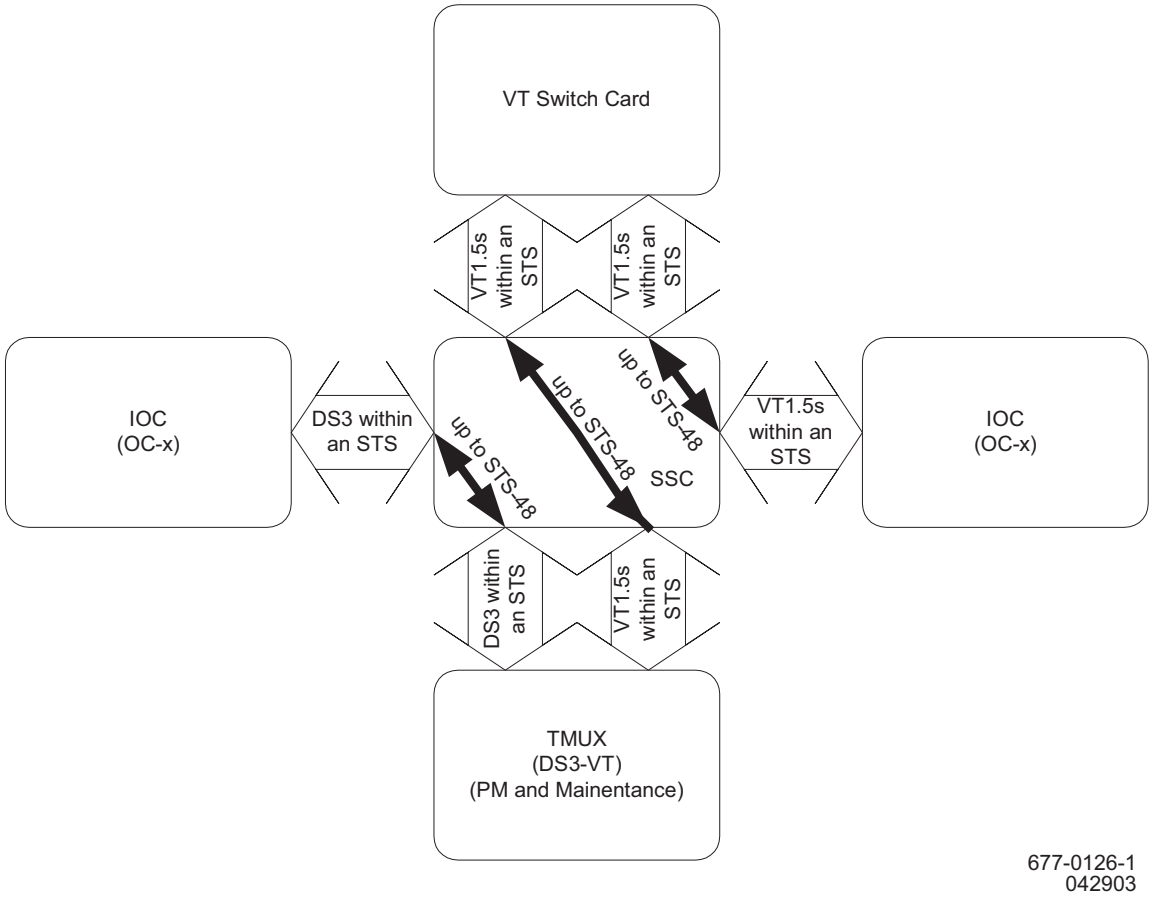
The alternative mode of operation (DS1PM) does not involve transmultiplexing, but is used to monitor DS1 signals passing through the system. In this mode, VT1.5s are sent to the TMUX where the DS1s are extracted from the VT1.5 for PM and then reformed back into a VT1.5. The STS-1 and VT1.5 paths are terminated when the DS1 is extracted for DS1 PM.

The transmultiplex and PM functions support both the DS1 Super Frame and DS1 Extended Super Frame formats. Although not strictly limited by the hardware architecture, the specific DS1 format is provisioned by the customer when the STS-1s are provisioned for transmultiplexing.

The TMUX provides 2.5 Gb of transmultiplex capacity. The TMUX supports mapping and demapping of up to 48 DS3 or 1344 DS1/VT1.5 tributaries and requires 5 Gb/s of backplane bandwidth.

The TMUX provides PM and Facility Data Link (FDL) functions for DS1 level signals in the DS3 to VT1.5 with PM mode. In this mode, DS3 data encapsulated into STS-12 data streams is switched from the SSC 103 STS Switch Card (SSC) to the 2.5 Gb/s TMUX, and demultiplexed to the D1 level where PM is collected. The DS1 data is then formatted into VT1.5 packets and transmitted to the SSC in an STS-12 stream. The data can then be switched to the VSC for grooming and transport. See figure 127-3.

Figure 127-3. DS3 to VT1.5 Signal Flow



The functional components of the 2.5 Gb/s TMUX follow:

- Telecom Bus Serializer (TBS)
- Hypermapper
- Clock distribution
- Reset and synchronization
- Slave Bus Interface (SBI) Field Programmable Gate Arrays (FPGAs)
- I^2C bus

TBS

The TBS uses internal switching as well as multiplex and broadcast capabilities to select source data and backplane data respectfully to/from the primary and secondary SSCs. It provides up to STS-96 data connections, local switching of source data and cross connections of STS-12 backplane data and STS-12 Hypermapper data.

Hypermapper

The hypermapper is a multi-chip component that has four ultramappers and performs the following functions:

- Maps SONET VT1.5 frames into SONET DS3 frames, performing PM at the DS1 level
- Maps SONET DS3 frames into SONET VT1.5 frames, performing PM at the DS1 level
- Performs PM at the VT1.5 level

Clock Distribution

The system clock from the TC is fed into two subsystems on the TMUX: system clock generator and the frame pulse generator for SONET framers. The system clock generator provides a 155.52 MHz IOC system clock as well as a 77.76 MHz clock. The working SSC STS controller uses the slave bus to select a TC system clock reference for the 2.5 Gb/s TMUX. In the frame pulse generator subsystem, an 8 kHz frame pulse is used to align all SONET payloads passing from a 2.5 Gb/s TMUX to the SSC. Unlike all other IOC interfaces, the 2.5 Gb/s TMUX does not provide an 8 kHz loop clock.

The CCC 102 Commom Control Cards (CCCs) source the system clocks, which are all point-to-point PECL pairs distributed at 50 MHz. The 2.5 Gb/s TMUX receives two copies of the 50 MHz clock from each CCC.

The TBS and hypermapper require various 622.08 MHz, 155.52 MHz, 77.76 MHz, and 19.44 MHz network clocks. All clocks are derived from the 8 kHz network timing signal present on the backplane. Status bits indicate loss of network timing source.

Reset and Synchronization

Two reset monitors are supported by the TMUX. One reset monitor monitors power and the other monitors a 25 MHz clock. When the power monitoring device detects a power level not in the required 3.3 V range, a reset is administered. During power up, the reset is kept active for approximately 350 ms until the power supply stabilizes. When a missing clock event is detected, a clock alarm is generated to the CCC through the SBI, forcing the use of the other clock.

SBI FPGAs

The SBI supports two FPGAs and provides high-speed communications between the IOC3s/IOC12s/IOC48s/TMUXs and the associated SSC. The SBI is divided into a read SBI and a write SBI, where the IOC3s/IOC12s/IOC48s/TMUXs receive on the write SBI and the SSCs receive on the read SBI.

I^2C Bus

The I^2C Serial Programmable Read Only Memory (PROM) accesses the SSC and contains data such as board type, serial number, and manufacturing date. These devices supply nonvolatile storage and allow the user to increase the amount of storage.

UDS-128
VSC 101 5 Gb/s VT1.5 Switch Card

PART NUMBER/ MNEMONIC	NAME	CLEI	ECI/BAR CODE	CPR	STATUS
3EM12313AA VSC	VSC 101 5 Gb/s VT1.5 Switch Card	WMEC60TAAD	123196	M73386	Inactive
3EM12313AB VSC	VSC 101 5 Gb/s VT1.5 Switch Card	WMEC606AAA	126643	M73386	Active

FEATURES AND APPLICATION NOTES

- Half-height (7.25”D x 8.49”H)
- 5 Gb/s switching capacity in slots 5,6,12, or 13, A or B when used with 80 Gb/s STS switch
- Supports enhanced RDI

DESCRIPTION

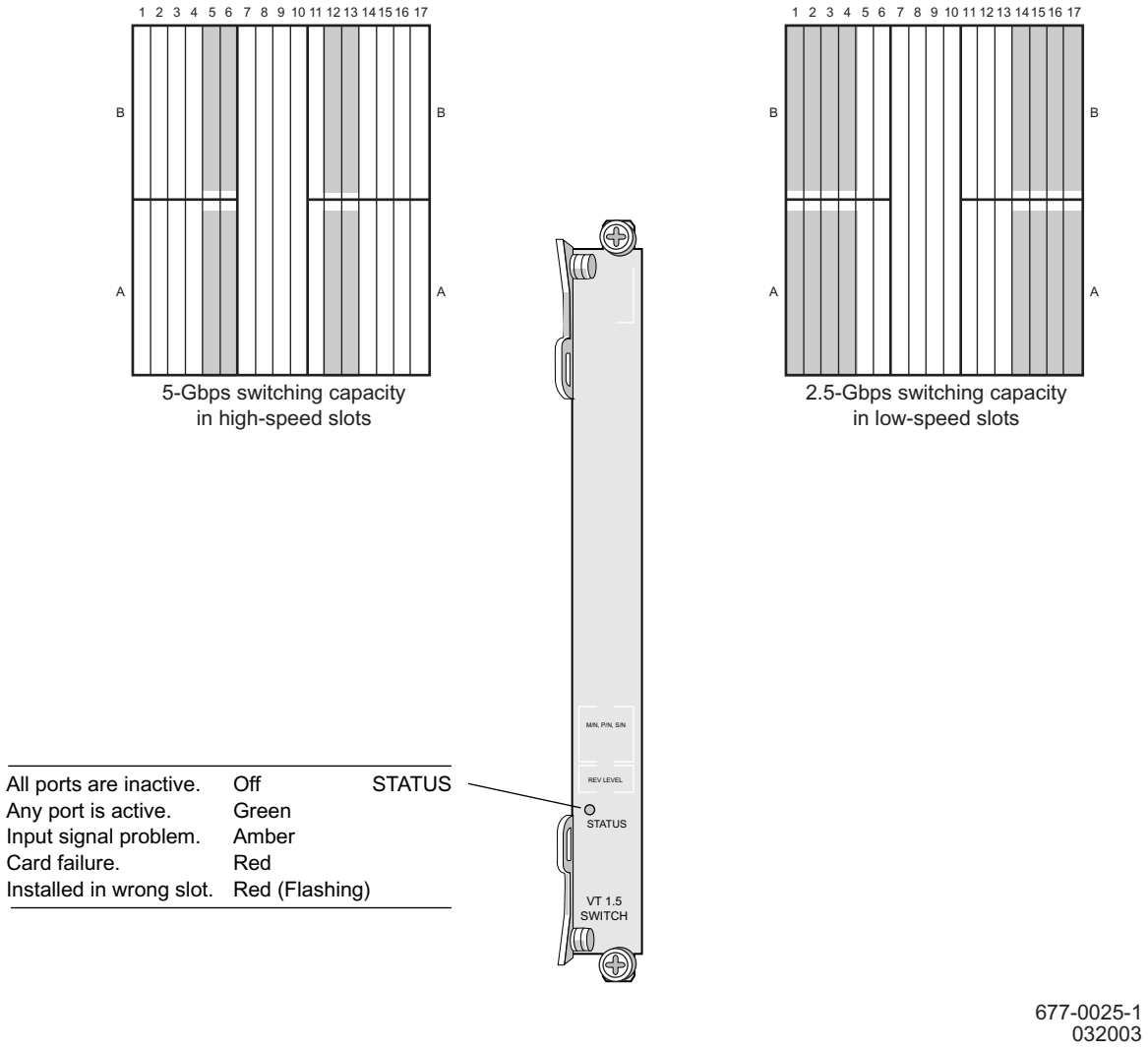
The VSC has a total capacity of 5 Gb/s or 2688 VT1.5 payloads when installed in a high-capacity slot.

The two versions of the VSC can be mixed within the same protection group.

INDICATORS AND CONNECTORS

Figure 128-1 describes the VSC front panel indicators and connectors.

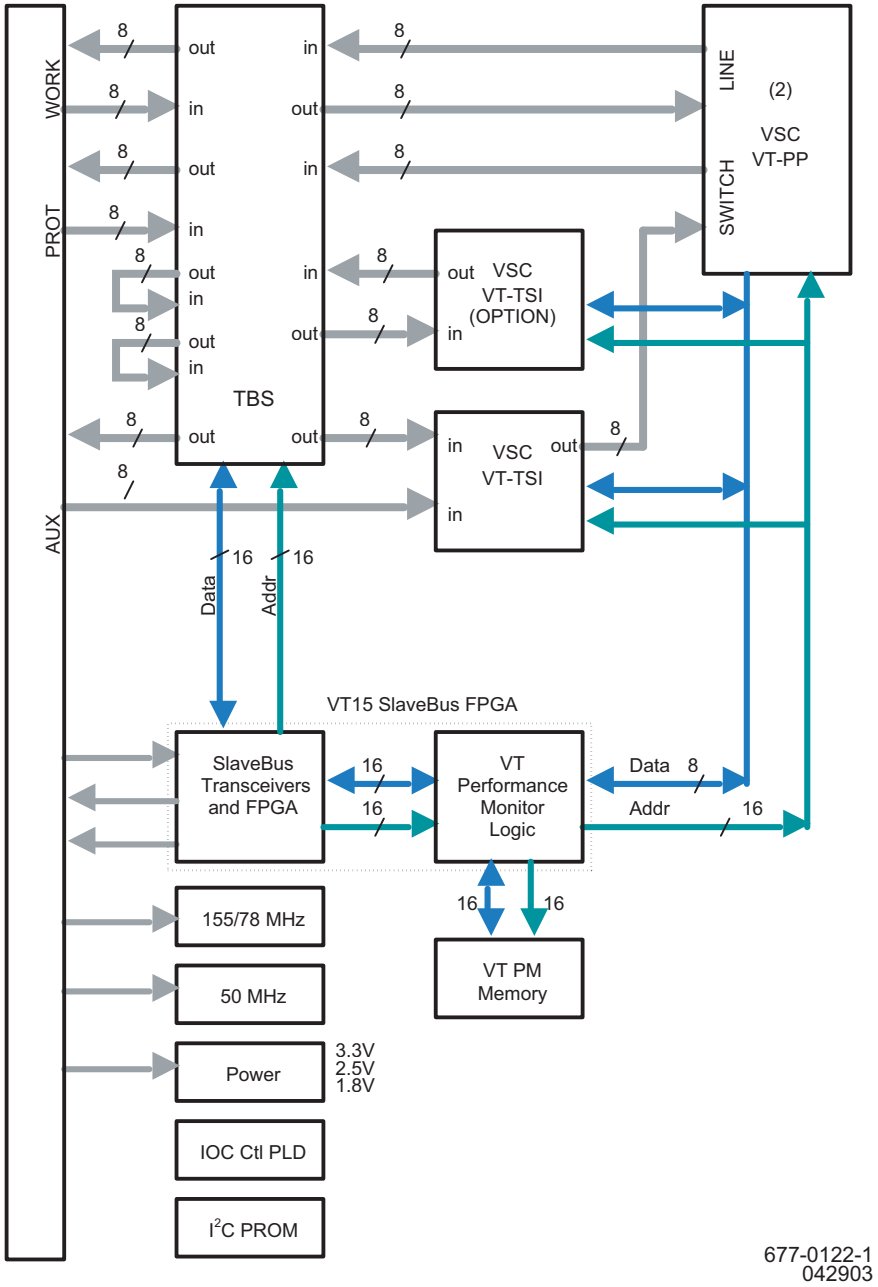
Figure 128-1. VSC Front Panel



FUNCTIONAL OPERATION

Figure 128-2 illustrates the function of the VSC and is followed by a brief description of the VSC functional blocks.

Figure 128-2. VSC Block Diagram



The VSC uses the following components to perform the VT1.5 switch:

- VT1.5 Chip Set
- Telecom Bus Serializer (TBS)
- VT Performance Monitoring (PM)
- Timing/Synchronization
- Slave Bus
- I^2C PROM
- DC-DC Conversion
- Reset and Power Monitor

The VT1.5 Chip set contains two processors that perform pointer processing, cross-connections, and path overhead processing with VT1.5 switching. The first processor provides column alignment and performance monitoring for VT1.5 payloads and interfaces them to the VT1.5 cross-connect. It receives four serial STS-12 622 Mb/s signals from a pointer processor or STS-groomer. The signals are terminated at the path level and are monitored and column aligned at the VT1.5 level. UPSR information is added to the VT overhead for use in the VT cross-connect.The four serial signals are then duplicated on working and protection STS-12 outputs to the protected VT switch fabrics. The second processor as a VT1.5 Time Slot Interchange (TSI) device. It provides a fully nonblocking cross connect for 3024 VT1.5s and requires all inputs are frequency, phase, and column aligned.

The TBS contains four groups of 16 bidirectional ports, each running between 622 Mb/s and 2.5 Gb/s. The VSC TBS functionality is equivalent to multiple TBS devices currently being used in all Input/Output Cards (IOCs). Two ports on the TBS are dedicated to backplane STS interfaces between the IOC and STS Switch Cards (SSCs). When installed with the 80Gb/s SSC, these ports provide 622 Mb/s bandwidth for each of the 16 STS-12 serial paths. With the exception of the Auxiliary port interface, all other TBS ports interface with the VT1.5 Chip Set processors.

The VT PM function monitors overhead bytes to provide PM information at the VT1.5 and STS-1 levels. The VT PM inhibits the B3 monitoring function provided by the Slave Bus Field Programmable Gate Array (FPGA).

Timing for the VSC is derived from a network timing source and a 50 MHz synchronous clock scheme. The VT1.5 Chip Set and TBS require various 155.52 MHz and 77.76 MHz network clocks. All network clocks are derived from the 8 KHz network timing signal presented at the backplane. Status bits indicate a

loss of the network timing source. All 50 MHz clocks are derived from two Common Control Cards (CCCs) and selected by the primary CCC. A local clock monitor flags an alarm condition, causing a switch to the redundant 50 MHz clock. The VSC uses either a 2 KHz synchronization clock from the Timing Cards (TCs) or an internally generated 2 KHz clock.

Because the VSC TBS is equivalent to multiple IOC TBSs, the VSC TBS is modified to supports Receive Time Slot Interchange (RTSI), Transmit Time Slot Interchange (TSLI), and Space Switch Element (SSWE) spaces specified by the Slave Bus FPGA. Generally, however, the VSC reuses the same, common Slave Bus design.

The Slave Bus Interface (SBI) supports two Field Programmable Gate Arrays (FPGA) and provides high speed communications between the IOCs and the associated SSC. The SBI is divided into a read SBI and a write SBI where the IOCs receive on the write SBI and the SSCs receive on the read SBI.

The I^2C Serial Programmable Read-Only Memory (PROM) access the SSC and contains data such as board type, serial number, and manufacturing date. Such devices supply nonvolatile storage and allow the user to increase the amount of storage.

DC power is converted onboard from the -48 V backplane supply. Most of the power is consumed at 1.8 and 3.3 V at the core power of the Arrow device. In order to avoid powering the I/O from the core supplies, the following power sequence is observed: 3.3 V power supply is powered up first, followed by the 1.8 V supply, then the 1.5 V supply.

Two reset monitors are supported by the VSC, one monitors power and the other monitors a 25 MHz clock. When the power monitoring device detects a power level not in the required 3.3 V range, a reset is administered. During power up, the reset is kept active for approximately 350 ms for the power supply to stabilize before being released. When a missing clock event is detected, a clock alarm is generated to the CCC through the SBI, forcing the use of the other clock.

Product Support Information

1. TELEPHONE SUPPORT

Customer Service Telephone Support

1.1 For telephone support for the customer services mentioned in this Product Support Information, call *888-ALCATEC (888-252-2832)* or *613-784-6100*, 8:00 a.m. to 5:00 p.m., Central Time, Monday through Friday. Ask the operator for the appropriate service to be connected to a qualified representative or engineer.

1.2 After-hours emergency telephone support is also available by calling *888-ALCATEC (888-252-2832)* or *613-784-6100*. An emergency is defined as an out-of-service, traffic-affecting problem or a nonoperating alarm system on traffic-bearing systems.

2. PRODUCT DOCUMENTATION AND TRAINING

Product Documentation

2.1 Product documentation is available on both paper and CD-ROM. The documentation can also be accessed through Alcatel-Lucent's Online Support Documentation and Software web site at *https://www1.alcatel-lucent.com/osds*. Product documentation updates appear on Alcatel-Lucent's Online Support Documentation and Software web site before they are available in any other format.

2.2 At Alcatel-Lucent's Online Support Documentation and Software web site, follow the on-screen instructions to register for access and obtain a login ID. In addition to accessing product documentation, the Alcatel-Lucent Online Support Documentation and Software web site allows the user to view the following:

- Application notes
- Configuration notes
- Data collections
- Frequently Asked Questions (FAQs)
- General information books
- General Release Documents (GRDs)
- Installation documents
- Methods of Procedure (MOPs)
- Product Change Notifications (PCNs)
- Product Information Bulletins (PIBs)
- Product manual updates
- Software patch and software load documents
- Software Update Documents (SUDs)
- Technical bulletins
- Training documents
- Urgent Product Warnings (UPWs)

Training

2.3 Equipment training is available to all customers. Crafts and maintenance personnel who are trained by Alcatel-Lucent's Training department can expect more effective assistance if they need to call the Technical Assistance Center. Regularly scheduled courses are available at the training facilities in Plano, Texas. If a customer cannot attend a standard course, the Training department can arrange a course for a specific requirement and conduct it at the customer's facility. For further information, call customer service telephone support and ask for a training coordinator or write to one of the following addresses:

IN USA:

Alcatel-Lucent USA
3400 W. Plano Pkwy.
Plano, Texas 75075
ATTN: Training M/S 1206-553

IN CANADA:

Alcatel-Lucent Canada
Network Services Division
P.O. Box 13600
Ottawa, Ontario K2K 2E6

2.4 The annual Product Training Catalog can be ordered by calling the training coordinator, or it can be viewed on-line at *http://www1.alcatel-lucent.com/us/product_training/catalog*.

3. TECHNICAL ASSISTANCE CENTER

3.1 The Technical Assistance Center staff is always ready to provide high-quality technical assistance. Customers can expect effective telephone assistance when their crafts and maintenance personnel have been trained by Alcatel-Lucent's Training department and are equipped with adequate test equipment, spares, and documentation at the site.

3.2 For technical assistance, call customer service telephone support.

After-hours Emergency Telephone Support

3.3 Emergency support is available after-hours through dispatch operators. Call customer service telephone support and ask for the Lightwave, Microwave, Operations Support System (OSS), Digital Loop Carrier (LMS), or Digital Cross-Connect emergency duty engineer.

3.4 An emergency is defined as an out-of-service, traffic-affecting problem or a nonoperating alarm system on traffic-bearing systems.

3.5 Nonemergency is defined as installation turn-ups, application questions, traffic cutover, routine maintenance, or other non-service-affecting maintenance. All non-service-affecting, after-hours telephone services are billable to the customer.

3.6 Please provide the operator with the following information:

- Company name
- Caller name
- A telephone number where caller can be reached
- A brief description of the problem, including the product involved

After-hours Nonemergency Telephone Support

3.7 After-hours telephone support to address new installations, system expansions, system operations, system application, or other non-service-affecting issues is available by contacting Alcatel-Lucent Customer Service at 1-888-252-2832 (1-888-ALCATEC) or 1-613-784-6100.

On-site Technical Support

3.8 On-site technical support is available when an issue cannot be resolved remotely. This determination is usually made by Alcatel-Lucent TAC during the problem investigation process. These services may or may not be billable to a customer. This depends on several factors such as what type of Service Level Agreement a customer has with Alcatel-Lucent, the age of the product, etc.

4. REPAIR AND RETURN SERVICES

4.1 As part of a comprehensive technical support program, Alcatel-Lucent provides factory repair services for equipment. This service is available both during and after the warranty period through Alcatel-Lucent's Return and Repair department.

Spare Parts and Replacement Circuit Packs

4.2 For spare parts, spare circuit packs, circuit pack exchange, and in-warranty replacement on a routine or emergency basis, call customer service telephone support.

4.3 Provide the following information:

- Company name
- Caller name
- A telephone number where caller can be reached
- A brief description of the problem, including product line, part number, and quantity of parts needed

4.4 For emergency assistance after normal business hours, call customer service telephone support, ask the operator for Emergency Parts Assistance, and provide the operator with the required information. The operator will contact an appropriate individual to respond.

Return for Credit or Warranty Exchange Procedure

4.5 Returned equipment must have a Return Authorization (RA) number. Obtain an RA number either by calling customer service telephone support or by fax *(972-519-4611)*.

4.6 No equipment should be returned without an RA number. The following information is required:

- Description and quantity of equipment to be returned
- Reason for return
- Order number the equipment was purchased against and approximate date of purchase

5. SERVICE CENTER

5.1 The Service Center tests, repairs, and modifies all circuit packs (both in and out of warranty). Circuit packs received for repair or modification are returned promptly.

Return for Repair Procedure

5.2 Refer to paragraph 4.5 for information on obtaining an RA number. Notification to the Service Center and issuance of an RA number by Alcatel-Lucent personnel *must be made prior to shipment of parts*. The following information must be furnished with the request for return authorization:

- Purchase order number or requisition number
- Description and quantity of equipment to be returned
- Reason for return:
  - Modification required
  - Defective equipment to be repaired
- Warranty status (in or out of warranty) and warranty date stamped on unit
- Specific nature of problem
- Name and telephone number of person who identified problem
- Special instruction/information

Shipping Instructions for Repair, Credit, or Warranty Exchange

5.3 Return equipment or parts prepaid to the address provided when the RA number was issued. The RA number must be prominently marked on the shipping label, the packing list, and any correspondence regarding the order.

- Include company name, address, and name of person to contact in case of a question.
- Include specific reason for return. (This aids prompt processing.)
- Include the same requisition number or purchase order number that was furnished with request for return authorization.
- Include type number and part number of unit.
- State whether equipment is in or out of warranty.
- Furnish shipping address for return of unit, if applicable, or other pertinent details.
- Mail purchase order, if applicable, to address shown under Return for Repair Procedure, Attention: Service Center.

6. INSTALLATION AND MAINTENANCE SERVICES

Engineering and Installation Service

6.1 Whether installation for specific equipment or a full turnkey network facility is needed, Installation Service can help. Alcatel-Lucent has experience in central office, outside plant, and customer premises applications, and specializes in flexible scheduling and high-quality service. Qualified staff are in place nationwide, so an installation can be started and completed promptly.

Contract Maintenance Service

6.2 Field service from Alcatel-Lucent offices nationwide is available if a maintenance contract is selected. Alcatel-Lucent field service is well-suited for private networks of any size. For a fixed annual fee, Alcatel-Lucent provides prompt response to service calls and provides scheduled preventive maintenance, including FCC-required measurements and record keeping.

6.3 Factory-trained service technicians are qualified on similar systems before they are allowed to maintain customer equipment. They have direct access to additional technical support around the clock and to all necessary tools and test equipment.