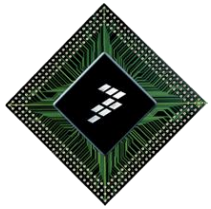
November, 2010

Effective PCB Design:
Techniques to Improve Performance



Daniel Beeker
Senior Field Applications Engineer

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- So…????
- What the heck is this all about?

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- What are the biggest differentiators between
- ***your*** product
- and your competitor's?

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Effective PCB Design:
Techniques to improve performance

- The packaging?
- The mix of parts you choose?
- The Microcontroller?

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Effective PCB Design:
Techniques to improve performance

- **Software**
  - Correct
  - Efficient
- **PCB design**

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PCB Design??

- Largest, most expensive component
- Usually the last piece of the hardware puzzle

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Effective PCB Design:
Techniques to improve performance

- Smaller device geometries and higher current switching capabilities have thrust us all into the world of RF, HF, UHF, and Microwave *Energy Management*

- Rise times on even the lowest tech devices now can exhibit Gigahertz impact.

- These changes directly impact product functionality and reliability.

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What has changed?

- IC technology was described as % shrink from IDR
  - Circuit based approach usually was close enough
- IC technology now described in nanometers
  - Circuit based approach falls completely apart
  - EM Field (physics) based approach essential
- EMC standards have changed
  - Lower frequency compliance requirements
  - Higher frequency compliance requirements
  - Lower emission levels allowed
  - Greater immunity required
- The playing field and the equipment have changed!!
- This really is a brand new game

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What can we do?

- The skills required are only taught in a few universities
  - Missouri University of Science and Technology, formerly the University of Missouri-Rolla
    - http://www.mst.edu/
  - Clemson University
    - http://www.cvel.clemson.edu/emc
- Our sagest mentors may not be able to help
- Nearly every rule of thumb is wrong!!
- To gain the skills needed, you have to actively seek them
- Industry Conferences
  - PCB East and West
  - IEEE EMC Society events
- Seminars hosted by your favorite semiconductor supplier!
  - Freescale, of course!

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- What can we do?

- There are many “myths” and folklore about the “art” of PCB design

- Old “rules of thumb” no longer apply
- Time to update our techniques and remove the mystery

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I had an epiphany at PCB West

- System designers do need to care about PCB design.
- Electromagnetic Field behavior is not “Black Magic”.
- Geometry IS critical.
- There are solutions that work.

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About Me: Daniel Beeker

- 30 years of experience at Motorola/Freescale designing and working with Microprocessor and Microcontroller development systems
- More than 20 years working with Automotive customers in one of the most demanding embedded control environments
- Championing the cause for increased awareness of advanced design technologies
- Used to believe in Black Magic, but Ralph Morrison set me straight!
- Firmly entrenched in Physics based design philosophy

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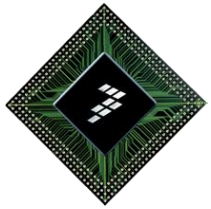
Electromagnetic Fields:

The Foundation of Electronics



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- Myths we *depended* on
  - Fields are invisible
  - Fields are well behaved
  - Fields follow the trace
  - Fields avoid open spaces
  - Fields are someone else's problem
  - Fields are only important in RF and Power supply designs
  - Fields are only for farmers

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- ***What is Electricity?***

- **IS IT VOLTS AND AMPERES?**

OR

- **IS IT ELECTRIC AND MAGNETIC FIELDS?**

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Fields are Basic to ALL Circuit Operation

- **VOLTS AND AMPERES MAKE THINGS PRACTICAL**
- **WE CAN MEASURE VOLTS AND AMPERES NOT E AND H FIELDS**
- **IN HIGH CLOCK RATE (*and* RISE TIME) CIRCUITS, FIELD CONTROL PLAYS A CRITICAL ROLE**
- **THIS MUST BE A CAREFULLY CONSIDERED PART OF ANY DESIGN**

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Maxwell's Equations

$$\oint \mathbf{E} \cdot d\mathbf{A} = \frac{q_{enc}}{\varepsilon_0}$$

$$\oint \mathbf{B} \cdot d\mathbf{A} = 0$$

$$\oint \mathbf{E} \cdot d\mathbf{s} = -\frac{d\Phi_B}{dt}$$

$$\oint \mathbf{B} \cdot d\mathbf{s} = \mu_0 \varepsilon_0 \frac{d\Phi_E}{dt} + \mu_0 i_{enc}$$

Slide compliments of http://www.physics.udel.edu/~watson/phys208/ending2.html

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Maxwell WAS smart!!

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A loose field is *not* a friendly field

- unHappy field in a sphere with an opening
  - Sneaks out and has a party
- unHappy field in a poor coaxial cable
  - Runs back along the outside of the cable and causes trouble
- unHappy field in a widely spaced transmission line pair
  - Reaches out as far as it can, looking for other paths to follow
- unHappy field between 2 widely spaced PCB planes
  - Low field density, has very little energy

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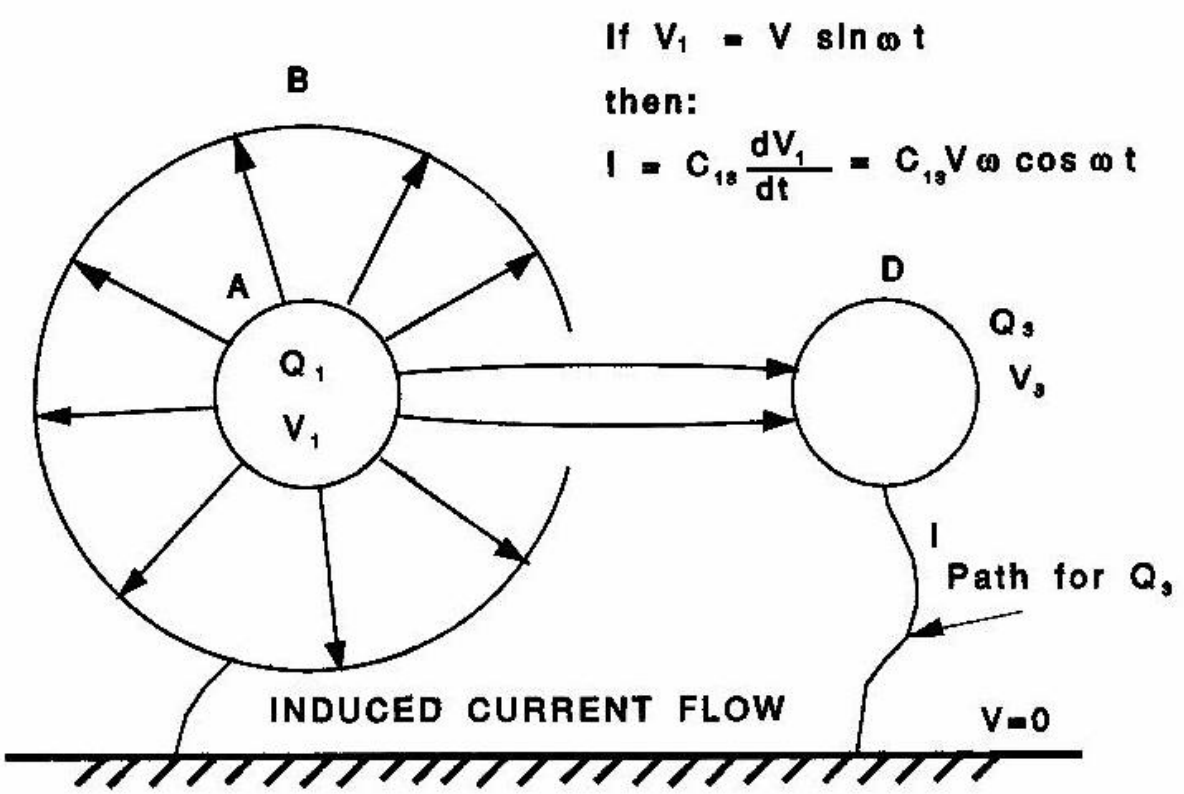
Fields are friendly?

A SHIELD ENCLOSURE WITH A HOLE



Field is not contained and looks for trouble

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ENERGY MANAGEMENT:

Fields store Energy in SPACE!

Energy is NOT stored in or on the conductors

A CAPACITOR IS:

- A CONDUCTOR GEOMETRY THAT CONCENTRATES THE STORAGE OF ELECTRIC FIELD ENERGY

AN INDUCTOR IS:

A CONDUCTOR GEOMETRY THAT CONCENTRATES THE STORAGE OF MAGNETIC FIELD ENERGY

IN A CAPACITOR

- FIELD ENERGY IS STORED IN
- THE SPACE BETWEEN THE
- PLATES

IN AN INDUCTOR

FIELD ENERGY IS STORED IN THE SPACE AROUND WIRES AND IN GAPS

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Fields behave the same in a component or in space

- IN A CAPACITOR:
  - A CHANGING VOLTAGE MEANS THE E FIELD IS CHANGING AND THAT CURRENT IS FLOWING
- IN SPACE:
  - A CHANGING E FIELD IS A DISPLACEMENT CURRENT THIS CURRENT CREATES A MAGNETIC FIELD

All components require fields to operate

- FIELDS CARRY ENERGY - NOT CONDUCTORS
  - WHAT ARE THE CONDUCTORS FOR?
  - THEY TELL THE ENERGY WHERE TO GO!

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- **Why does Energy follow conductors?**

- **WHY DOES WATER FLOW IN A STREAM?**

SAME REASON

- **NATURE FOLLOWS THE PATH THAT STORES THE LEAST ENERGY**

- **IT IS EASIER FOR FIELDS TO *FOLLOW* TRACES THAN TO GO OUT ACROSS SPACE**

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▶Transmission Lines are Convenient paths for Energy flow

- EVERY CONDUCTOR PAIR IS A TRANSMISSION LINE
- TRACE-TO-TRACE OR TRACE-TO-CONDUCTING PLANE
- THE FIELDS, AND THUS THE ENERGY FLOW, WILL CONCENTRATE BETWEEN TRACES OR BETWEEN A TRACE AND A CONDUCTING PLANE
- DRAW THE FIELDS TO LOCATE THE CURRENT

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Properties of Transmission Lines

- THEY DIRECT ENERGY FLOW
- THEY CAN STORE FIELD ENERGY
- THEIR POSITION IN A CIRCUIT IS CRITICAL
- THEY CROSS COUPLE ENERGY ONLY AT WAVE FRONTS
- THEY DELIVER ENERGY AT TERMINATIONS
- THEY ARE BI-DIRECTIONAL
- THEY CAN TRANSPORT ANY NUMBER OF WAVES AT ONE TIME
- THEY CAN RADIATE

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We Use Transmission Lines to Transport Energy and to Carry Logic Signals

- ***A TRANSMISSION LINE CAN CARRY ANY NUMBER OF SIGNALS IN EITHER DIRECTION AT THE SAME TIME***
- **BELOW 1 MHz THE GEOMETRY OF THESE LINES IS NOT TOO CRITICAL**
- **WITH TODAY'S CLOCK RATES AND RISE TIMES THE GEOMETRY OF THESE LINES IS KEY TO PERFORMANCE**

In a good design:

- **FIELDS ASSOCIATED WITH DIFFERENT SIGNALS DO NOT SHARE THE SAME PHYSICAL SPACE.**
- **IF THEY DO SHARE THE SAME SPACE, THERE IS CROSSTALK!**

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In a good design:

- ENERGY IS AVAILABLE WHENEVER THERE IS A DEMAND
- THE VOLTAGE SOURCE MUST BE REASONABLY CONSTANT
- ENERGY MUST BE REPLACED AFTER IT IS USED OR THERE WILL BE LOGIC PROBLEMS
- THIS IS CALLED ENERGY MANAGEMENT

Local Sources of Energy:

- DECOUPLING CAPACITORS
- THERE IS ALSO ENERGY AVAILABLE FROM THE GROUND/POWER PLANE CAPACITANCE

New Problem:

- IT TAKES TIME TO MOVE THIS ENERGY FROM STORAGE TO A LOAD

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How long does it take??

Wave Velocity

- FOR TRACES ON A CIRCUIT BOARD $v = c / €^{1/2}$
- WHERE c I S THE VELOCITY OF LIGHT AND € IS THE RELATIVE DIELECTRIC CONSTANT

v = 150 mm / ns or 6” / ns

All Energy is moved by Wave Action!!

- A DROP IN VOLTAGE SENDS A WAVE TO GET MORE ENERGY
- WAVES REFLECT AT DISCONTINUITIES
- A SOURCE OF VOLTAGE IS A DISCONTINUITY
- EACH REFLECTED WAVE CAN CARRY A LIMITED AMOUNT OF ENERGY

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▶What does this mean in my circuit board?

Initial power level in a 50 ohm line

5 OHM LOAD AND 5 V SOURCE **I = 0.1 AMPERES OR ½ WATT**

▶Now, how do I get 1 Ampere?

EVEN IF THE LINE IS ONLY 1/16 INCH LONG:

IT TAKES 10 ps FOR A WAVE TO GO 1/16 INCH IN FR4
IT TAKES 20 ps FOR A WAVE TO MAKE ONE ROUND TRIP
IT TAKE 30 ROUND TRIPS ON THAT LINE TO BRING THE CURRENT LEVEL UP TO NEAR 1 AMP
THAT IS 600 ps, ASSUMING ZERO RISE TIME

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Typical 1/16 inch connections:

- Traces to CAPACITORS
- CONNECTIONS to IC DIES
  - Lead frames and wire bonds
  - BGA interposers
- Traces to VIAs
- VIAs to GROUND/POWER PLANES

Slide compliments of Ralph Morrison, Consultant

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Capacitors are Short Transmission Lines!

- **WAVE ACTION IS REQUIRED TO MOVE ENERGY IN AND OUT OF A CAPACITOR**
- ***Don't forget the connections to the capacitor!***
- **SELF INDUCTANCE DOES NOT PROPERLY TELL THE STORY OF WHY IT TAKES TIME TO SUPPLY ENERGY**
- **CIRCUIT THEORY DOES NOT CONSIDER TIME DELAYS**

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All Energy is moved by Wave Action!!

When a switching element closes, this results in a drop in the voltage on the power supply. The resulting field energy *request* wave travels until this request is filled or it radiates.

The only way to reduce noise in a system is to reduce this distance and provide adequate sources of Electromagnetic Field energy.

Energy source hierarchy:

- **On-Chip Capacitance**
- **Power Planes if present**
- **Local bypass capacitors**
- **Field energy stored across the PCB structure**
- **Bulk storage capacitors**
- **Finally the power supply**

We have to keep the field happy and contained as far up the food chain as we can, to reduce system noise.

Slide comments are compliments of Ralph Morrison, Consultant

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-Logic Families/Rise Time/Max Length-

DEVICE TYPE	RISETIME	Max Line Length-Inner (Inch/mm)	Max Line Length-Outer (Inch/mm)
Standard TTL	5.0 nSec	7.27 / 185	9.23 / 235
Schottky TTL	3.0 nSec	4.36 / 111	5.54 / 141
10K ECL	2.5 nSec	3.63 / 92	4.62 / 117
ASTTL	1.9 nSec	2.76 / 70	3.51 / 89
FTTL	1.2 nSec	1.75 / 44	2.22 / 56
BICMOS	0.7 nSec	1.02 / 26	1.29 / 33
10KH ECL	0.7 nSec	1.02 / 26	1.29 / 33
100K ECL	0.5 nSec	.730 / 18	.923 / 23
GaAs	0.3 nSec	.440 / 11	.554 / 14

(Calculated assuming a nominal Er = 4.1)

Slide compliments of Rick Hartley, Consultant

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- Antenna size vs. Frequency

Frequency	¼ wave length
1 Hertz Rise time equivalent, who cares	246,000,000 feet (46,591 miles) Almost 6 times around the earth
10 Hertz Rise time equivalent, still who cares	24,600,000 feet (4,659 miles) Almost from New York to Honolulu
100 Hertz Rise time equivalent, .01 seconds	2,460,000 feet (466 miles) Almost from New York to Detroit
1 KHz Rise time equivalent, 1 millisecond	246,000 feet (46.6 miles) Almost from Orlando to Cocoa Beach
10 KHz Rise time equivalent, 100 microseconds	24,600 feet (4.659 miles) Almost from the J. W. Marriott to Disney's Magic Kingdom
100 KHz Rise time equivalent, 10 microseconds	2,460 feet (0.466 miles) Almost from the J. W. Marriott to the Central Florida Parkway
1 MHz Rise time equivalent, 1 microsecond	246 feet (0.0466 miles) Less than a football field
10 MHz Rise time equivalent, 100 nanoseconds Rise time distance, 100 feet	24.6 feet Across the room
100 MHz (TTL Logic) Rise time equivalent, 10 nanoseconds Rise time distance, 10 feet	2.46 feet Less than a yard
1 GHz (BiCMOS Logic) Rise time equivalent, 1 nanosecond Rise time distance, 1 foot	0.246 feet (2.952 inches) Less than your finger
10 GHz (GaAs Logic) Rise time equivalent, 100 picoseconds Rise time distance, 1.2 inches	0.0246 feet (0.2952 inches) Less than the diameter of a pencil
100 GHz (nanometer geometry HCMOS) Rise time equivalent, 10 picoseconds Rise time distance, 0.12 inches	0.00246 feet (0.0295 inches) Half the thickness of a standard FR4 PCB

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- Antenna size vs. Frequency

Frequency	¼ wave length
10 MHz HMOS Rise time equivalent, 100 nanoseconds Rise time distance, 100 feet	24.6 feet Across the room
100 MHz (TTL Logic) UDR HCMOS Rise time equivalent, 10 nanoseconds Rise time distance, 10 feet	2.46 feet Less than a yard
1 GHz (BiCMOS Logic) IDR HCMOS Rise time equivalent, 1 nanosecond Rise time distance, 1 foot	0.246 feet (2.952 inches) Less than your finger
10 GHz (GaAs Logic) 65 nM HCMOS Rise time equivalent, 100 picoseconds Rise time distance, 1.2 inches	0.0246 feet (0.2952 inches) Less than the diameter of a pencil
100 GHz 32 nM HCMOS Rise time equivalent, 10 picoseconds Rise time distance, 0.12 inches	0.00246 feet (0.0295 inches) Half the thickness of a standard FR4 PCB

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- From the previous table, a few things become apparent:
  - We got away with ignoring basic physics because IC switching speeds were *slow* and efficient antennas had to be **HUGE**.
  - At a switching speed of 1 nanosecond, it only takes a PCB feature (trace or slot) of 3 inches to be an efficient antenna (1/4 wave length)
  - Once you cross that magic boundary of 1 nanosecond, most PCB designs are capable of providing a wonderful source of antennas
  - At 10 picosecond speeds, almost every structure on a PCB can be an good antenna
- Fields are now very friendly and want to visit everywhere.

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Fields are friendly!

- Fields are in the spaces not in the traces[1]

- Is there something missing in our schematics?
  - Shouldn't there be something that helps us tell the field where it needs to be?

- We need a revolution in understanding and defining schematics and circuits.
  - Something to remind us to pay closer attention

[1] **Statement compliments of Ralph Morrison, Consultant**

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Fields are friendly!

- Component symbols must remind us to define the entire transmission line!

Field is free to roam
Open Range!

Field is kept out of trouble
Field fenced in!

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A contained field is a friendly field

- Happy field in a sphere
- Happy field in a *good* coaxial cable
- Happy field in a closely spaced transmission line pair
- Happy field between 2 closely spaced PCB planes

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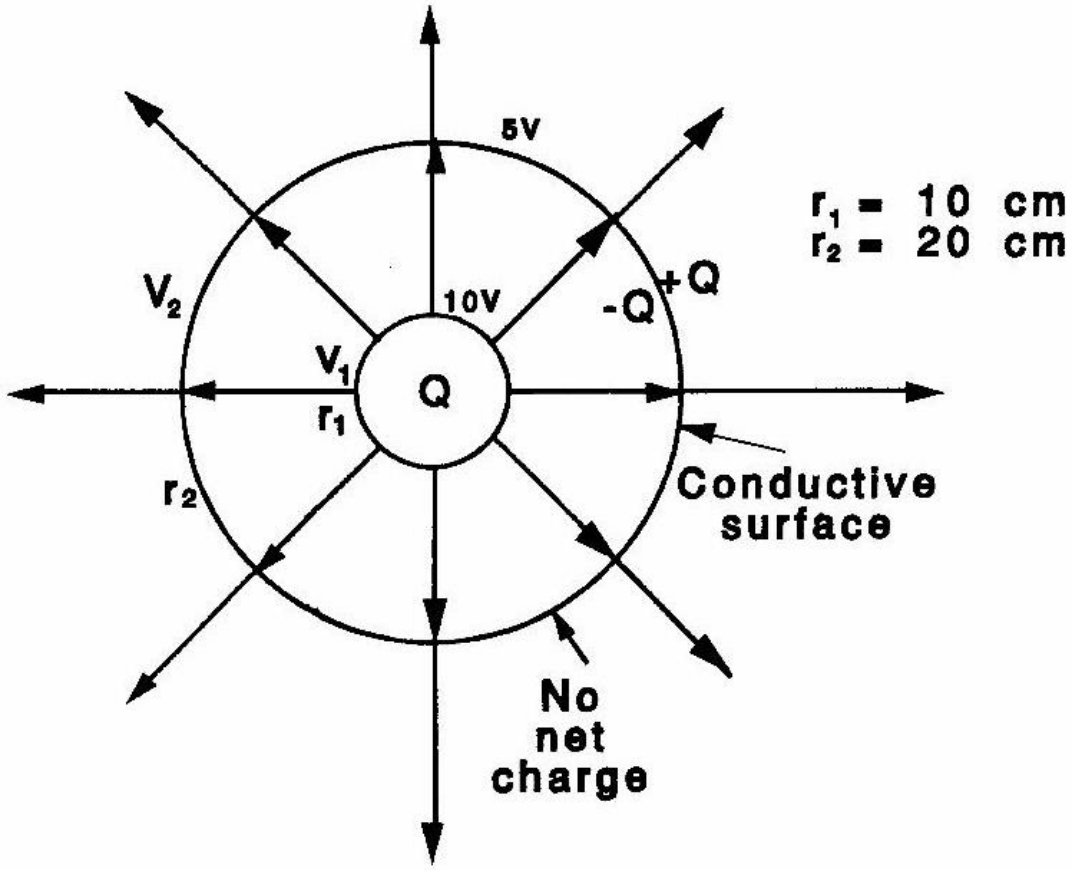
AN EQUIPOTENTIAL SURFACE AROUND A CHARGED SPHERE



Quite at home, no reason to roam

Slide compliments of Ralph Morrison, Consultant

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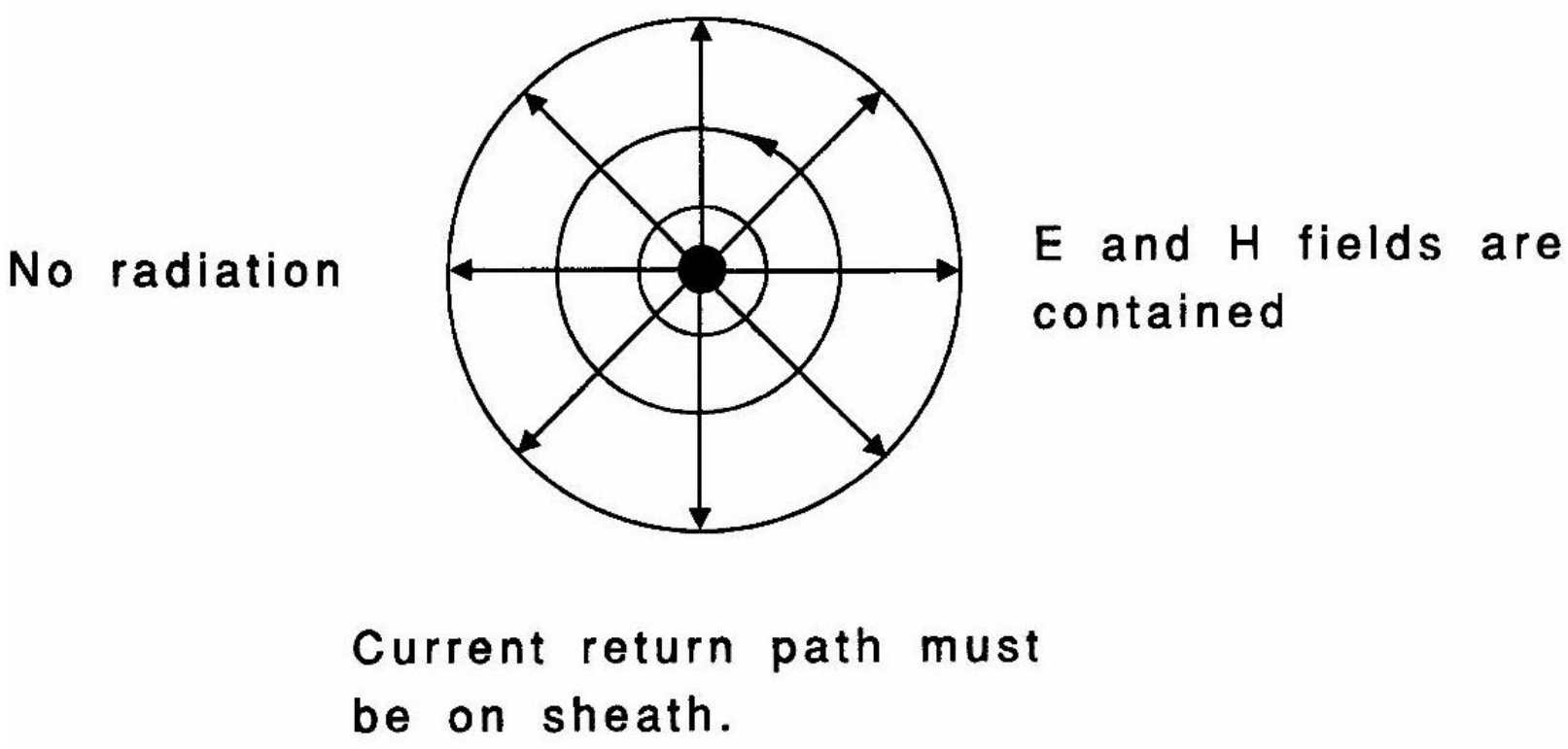
Fields are friendly!

COAXIAL TRANSMISSION



Quite at home, no reason to roam

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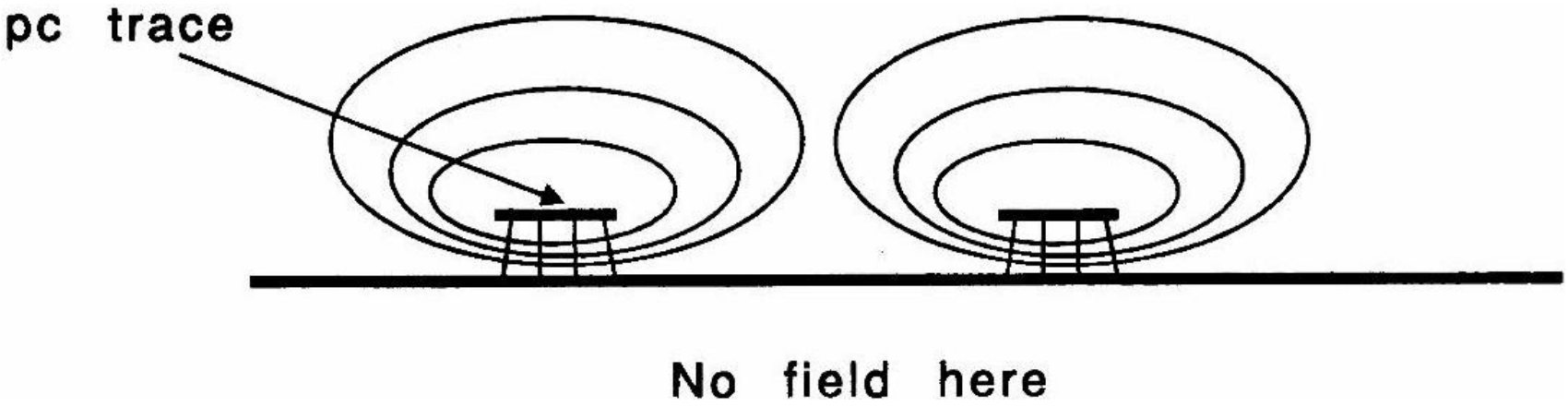
Fields are friendly

Fields concentrate under the traces and there is little crosstalk.



Fields don't penetrate the plane.

Quite at home, no reason to roam

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Fields are friendly?

- Fields need to be carefully managed
  - Every connection must be treated as part of a transmission line pair
  - Field *volumes* must be carefully managed

    (yes, this is now a 3 dimensional geometric design problem)

- Fields may not be friendly, but they can be *protected* and *tamed!*

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ENERGY AND LOGIC SIGNALS

THE TRANSMISSION OF A LOGIC SIGNAL MEANS THAT FIELD ENERGY IS SENT OUT ON A TRANSMISSION LINE

THIS IS TRUE EVEN IF THE LINE IS UNTERMINATED

THIS ENERGY MUST BE LOST IN HEAT OR RADIATION. IT CAN NOT BE RETURNED TO THE CIRCUIT

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Well-defined Transmission Line

- Signal trace MUST be one dielectric away from the return!

- Adjacent to Planar Copper
- Adjacent to Ground Trace

- Any deviation from this MUST be an engineered compromise, NOT an accident of signal routing

- Any deviation from this WILL increase radiated emissions, degrade signal integrity, and decrease immunity

- This is a very serious problem, and a big change from normal board design philosophy.

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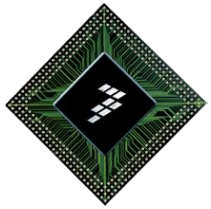
Electromagnetic Fields:



Now How do we use this wonderful information?

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Where do we start?

- Board outline
  - Usually pre-determined
    - Defined by previous product
    - Customer requirements
- Placement
  - 1. Pre-defined components
    - Usually Connectors
  - 2. Filter components
    - High priority, must be as close to the pins as allowed by manufacturing
  - 3. Power control
    - As close to connector involved as possible
      - Voltage regulators
      - Power switching devices
      - See number 2 above

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Schematic must be evaluated during layout

- Arbitrary connections can be redefined to improve layout
  - Unscrambling nets can result in:
    - Reduced complexity
    - Reduced trace length
    - Improved EMC performance
  - Signals which are not defined to specific pins
    - GPIO on MCUs
    - A/D pins on MCUs
    - Address and data lines to memories
      - No, the memory does not care what you call each pin
      - They are just address and data, not Addr14 or Data12

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Schematic must be evaluated during layout

- Pin assignment to connector signals
  - Most connectors do not have adequate signal returns defined
  - Unfortunately, these are often either legacy or defined by the wiring harness
  - When possible, this can result in significant improvement in EMC behavior
  - Can have significant impact on layout complexity

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- *Schematic must be evaluated during layout*
  - Pin assignment to connector signals
    - Ideal Connector Pin Assignment:

PGSGSGSGSGP

GSGSGSGSGSG

      - Not exactly economical or practical
    - More practical and fewer ground pins:

SSSGSSSGSSP

SGSSSGSSSGP

      - Each signal is only 1 pin spacing from Ground

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Schematic must be evaluated during layout

- Pin assignment to connector signals
  - Signals can be evaluated to route most critical signals adjacent to ground pins
    - Highest priority, adjacent to ground
      - labeled **A**,
    - Lower priority, diagonally adjacent to ground
      - labeled **B**,
    - Next lower priority, one pin position away from ground
      - labeled **C**
    - **…**

BAAGAAAGAAP

AGAAAGAAAGP

  - This can be applied when you are not allowed sufficient returns, but will improve EMC

DCAGACDCBAP

DCBABCDCAGP

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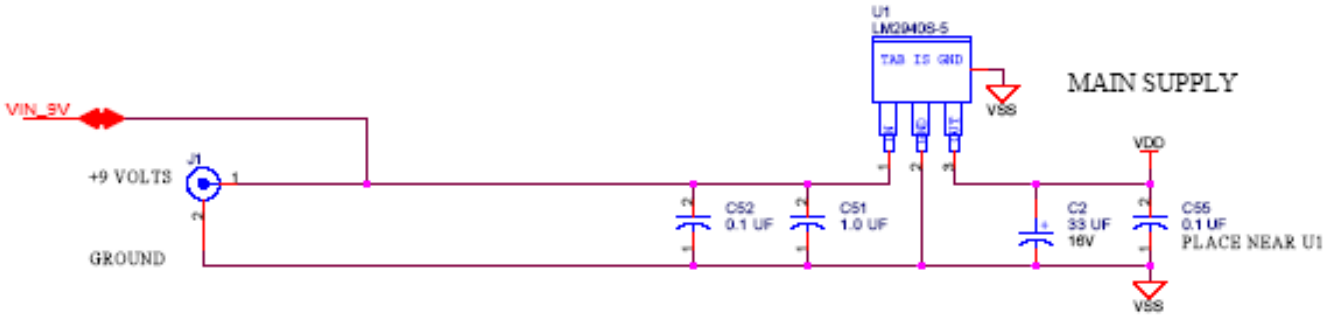
Schematic must be evaluated during layout

- Schematic is often lacking in order definition
  - Capacitors must be placed in the daisy chain in the correct order



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Uncontrolled component placement

- You get to decide!
- Placement not specified by customer or company requirements
- Evaluate component domain
  - Power
  - Sensor
  - Digital IC
- Place to limit signal mixing
  - Route Power only in Power realm
  - Route Sensor lines only where needed
  - Digital IC connections only in Digital realm

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Uncontrolled component placement

- Power Realm devices must be placed near connectors
  - Shorter traces
  - Cleaner returns
  - Reduced field volumes
    - Yes, this is a three dimensional consideration
  - Don't forget their supporting cast
    - Bypass capacitors, Inductors, resistors, etc.
    - Use the largest value capacitor in the smallest package allowed by manufacturing and reliability [3]
- Digital Realm devices
  - Technology (geometry) of each device
  - Function
  - Devices placed within lumped distance do not need terminating resistors
    - 1/12 wavelength of the IC *switching* frequency, not clock frequency
      - Determined by IC geometry
      - Yes, this is important to know
      - Sometimes controlled by variable drive strength
    - For 1 nSec switching speeds (1 GHz) this is about ½ inch!

[3] **Comment compliments of Dr. Todd Hubing, Clemson University**

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Uncontrolled component placement

- Remember, if you *do not* route signals where they don't need to be, there will not be any crosstalk or interference.
- This is easier if you *do not* mix the parts together.

- If the traces are not near each other, there is no magic that will cause them to interfere with each other…
- Can I say this any other ways? Is this important, YES!!

Now to move on to actually routing the board…

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PCB ~~Signal~~ TRANSMISSION LINE Routing

- The first and most important is to route the power distribution network, it is the source of all of the Electromagnetic energy you will be managing on the PCB.
- On low layer count boards, with no dedicated ground plane, the power lines MUST BE ROUTED IN PAIRS
  - Power *and* Ground
  - Side by Side
    - Trace width determined by current requirements
    - Spaced as close as manufacturing will allow them
  - Daisy chain from source to destination, connecting to each component, then finally to target devices
- Minimize the VOLUME of the Power TRANSMISSION network

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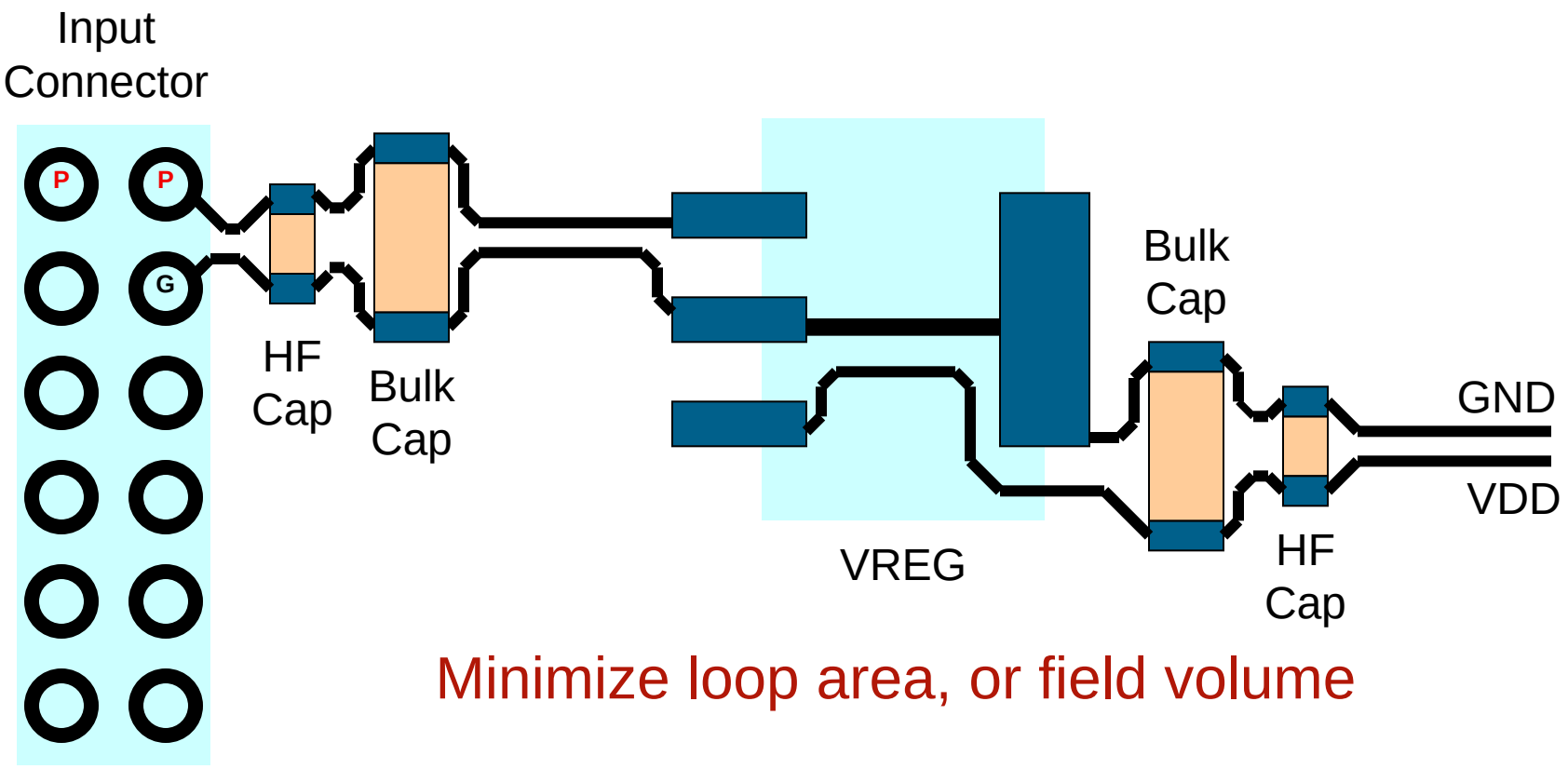
▶ *PCB ~~Signal~~ TRANSMISSION LINE Routing*



Minimize loop area, or field volume

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PCB ~~Signal~~ TRANSMISSION LINE Routing

- Route power and ground traces as close as manufacturing allows
  - Internal and customer separation requirements
  - PCB Fabrication limits for chosen supplier
    - Yes, you do need to know what the supplier can manufacture
    - Can have big impact on PCB cost
- Small changes in routing can have a large impact on performance
- Component placement is critical
  - Staying within lumped distance
    - Reduces component count
    - Reduces system cost
    - Improves EMC performance

- Minimize the VOLUME of the Power TRANSMISSION network

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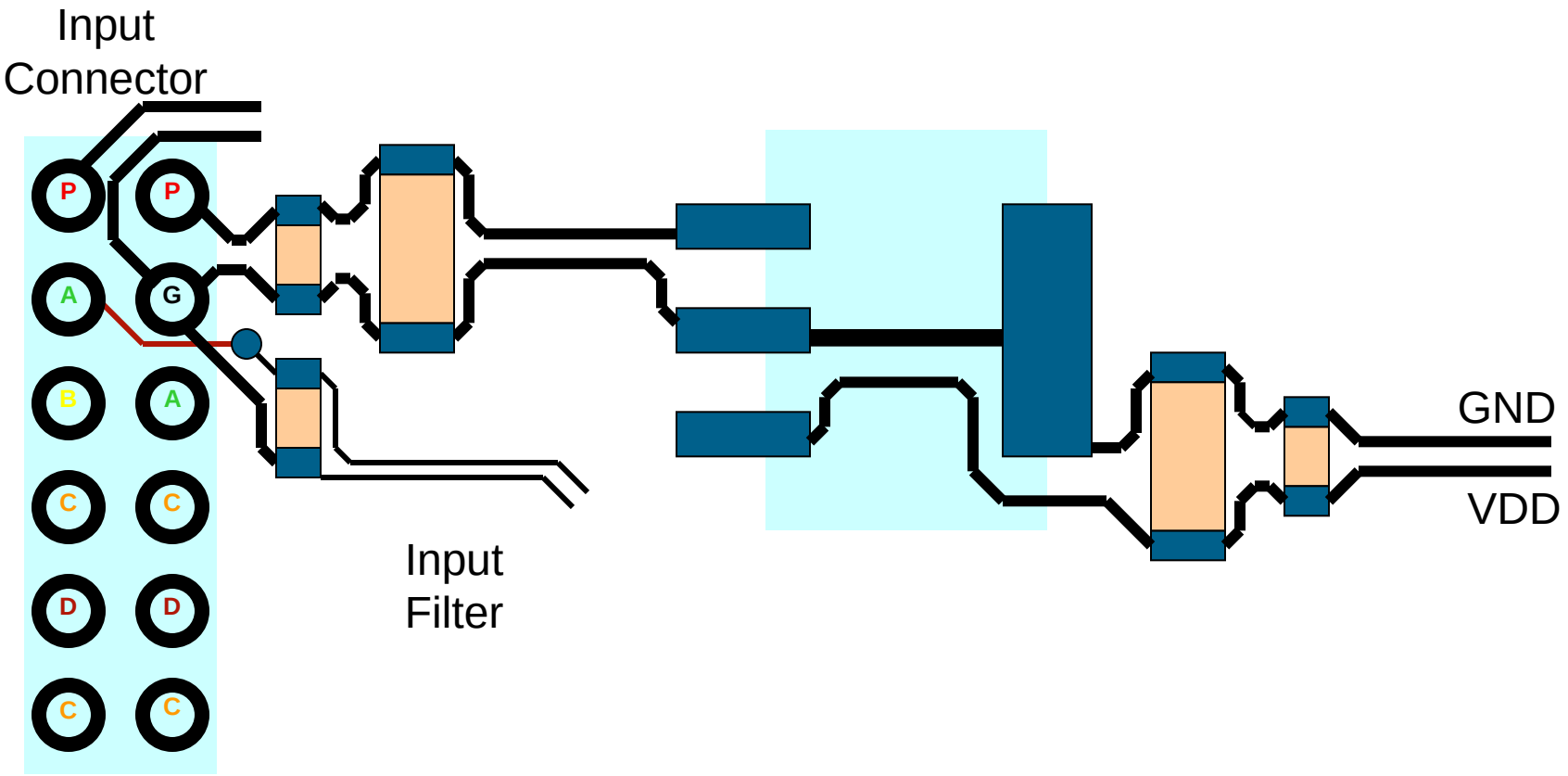

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PCB ~~Signal~~ TRANSMISSION LINE Routing

- Input filters must be placed as close as allowable to connectors
- Connections must be directly to the Connector Ground pins
- Route traces with well defined return path
- Minimize the VOLUME of the Signal TRANSMISSION network

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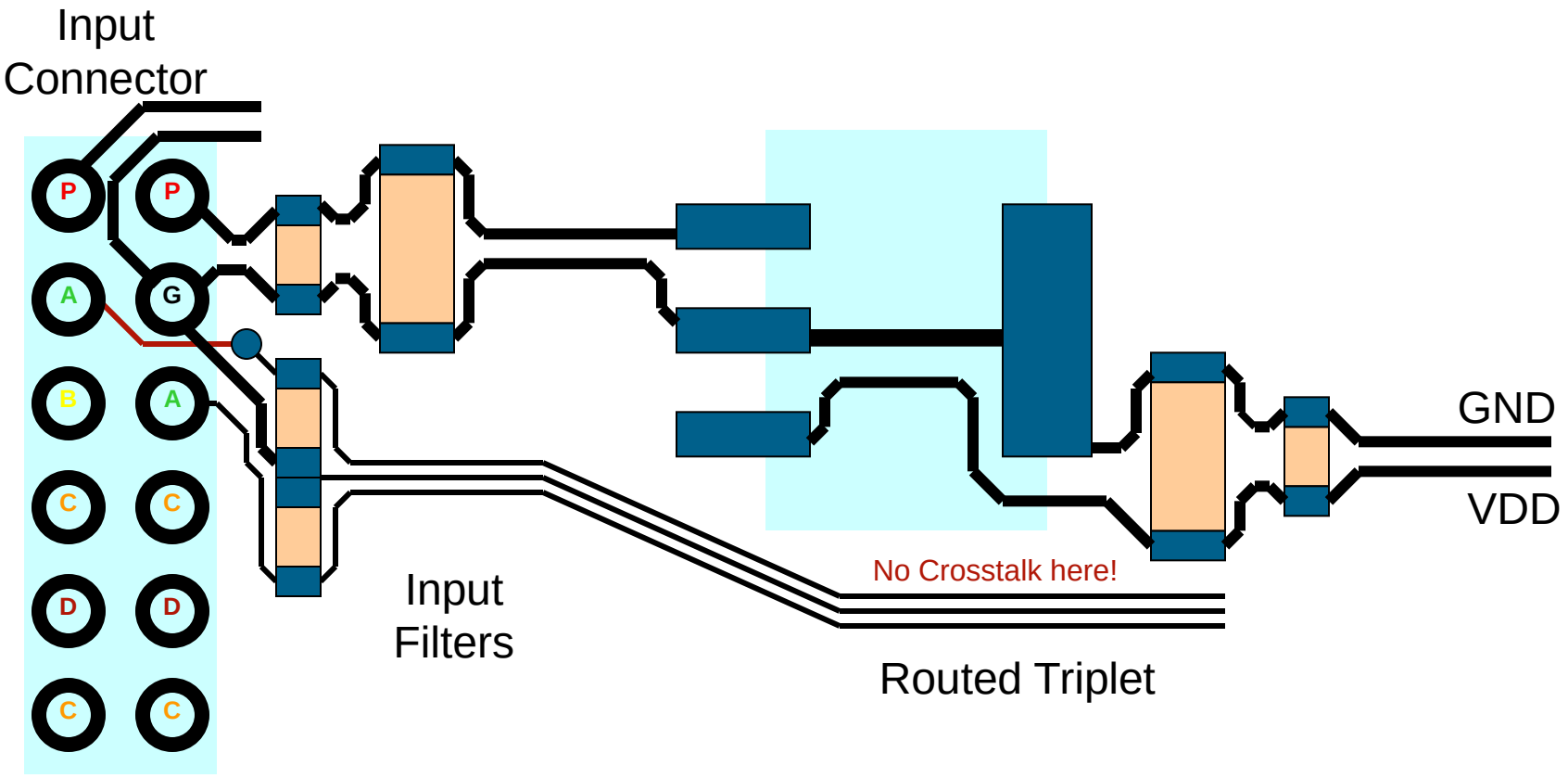

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PCB ~~Signal~~ TRANSMISSION LINE Routing

- Routing in “Triplets” (S-G-S) provide good signal coupling with relatively low impact on routing density
- Ground trace needs to be connected to the ground pins on the source and destination devices for the signal traces
- Spacing should be as close as manufacturing will allow
- Minimize the VOLUME of the Signal TRANSMISSION network

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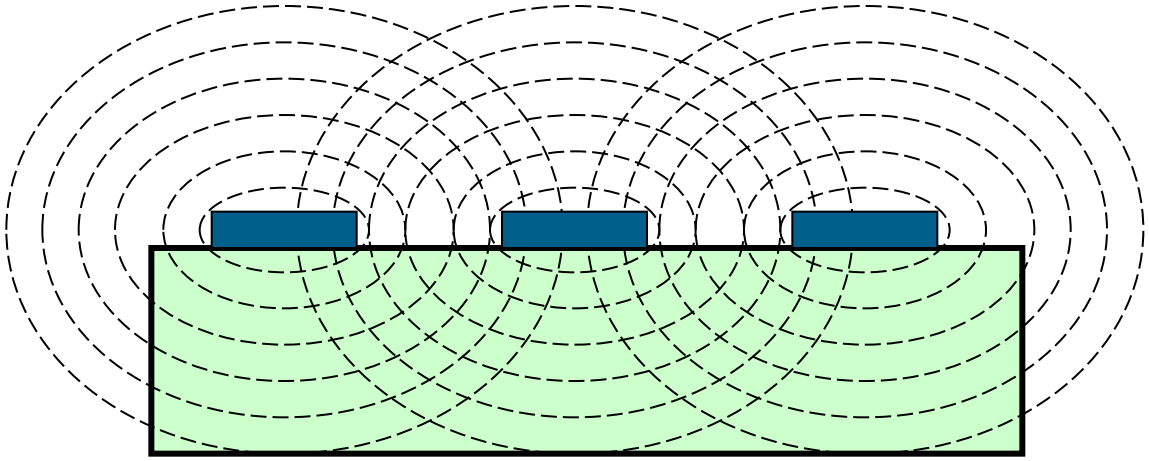
- You really want to make sure that the Field Energy is coupling to the conductor YOU choose!



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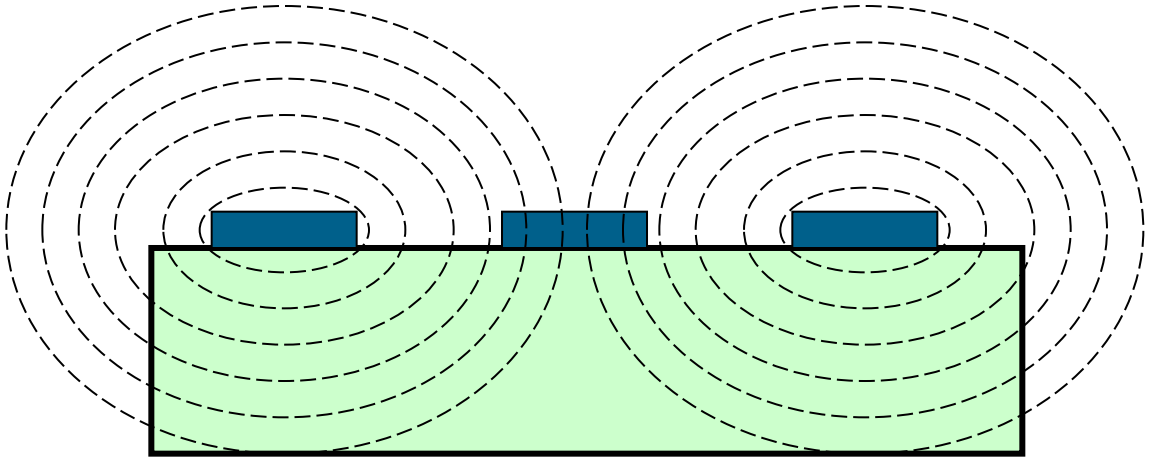

Maybe a “Triplet” makes sense???

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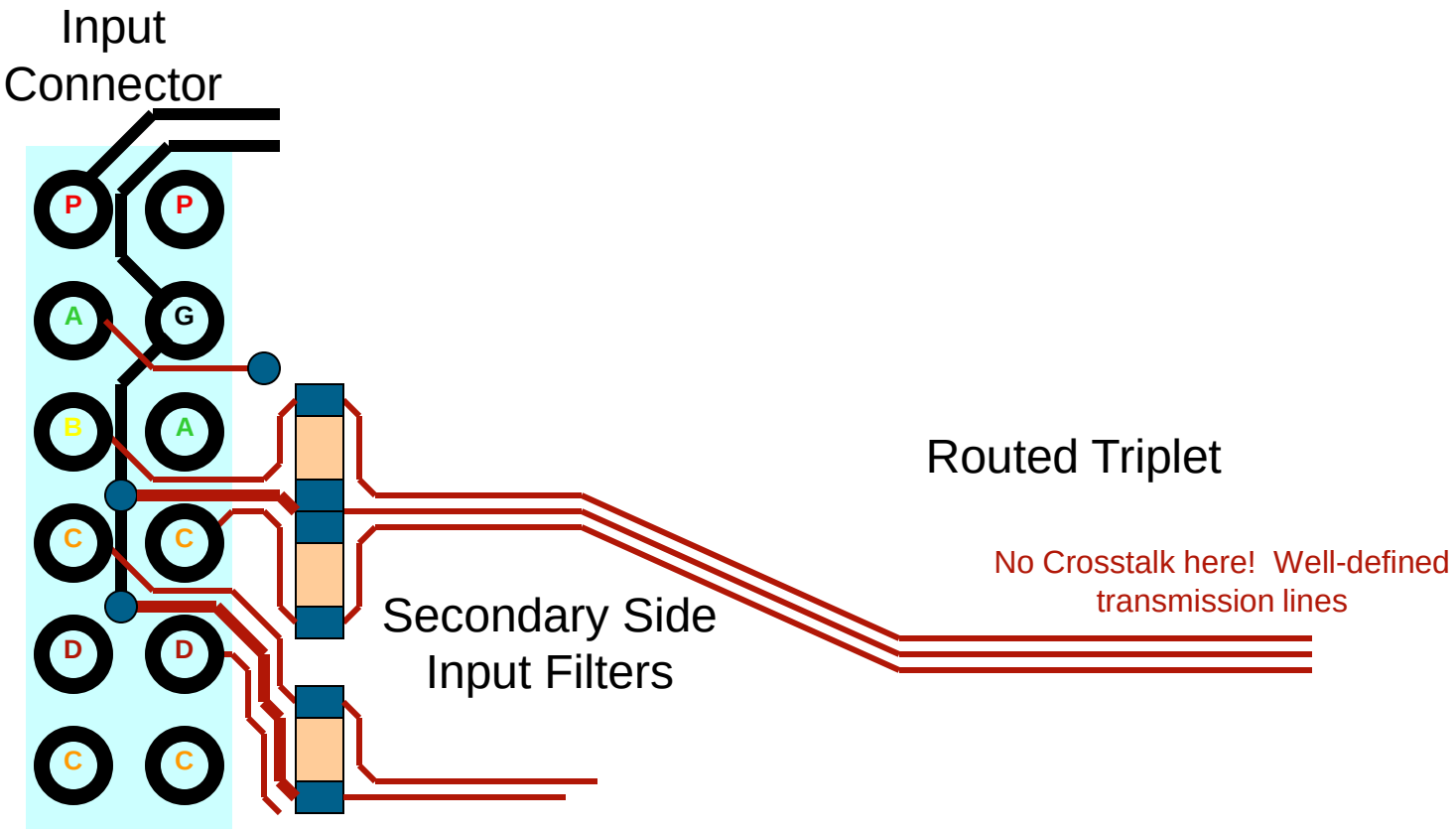

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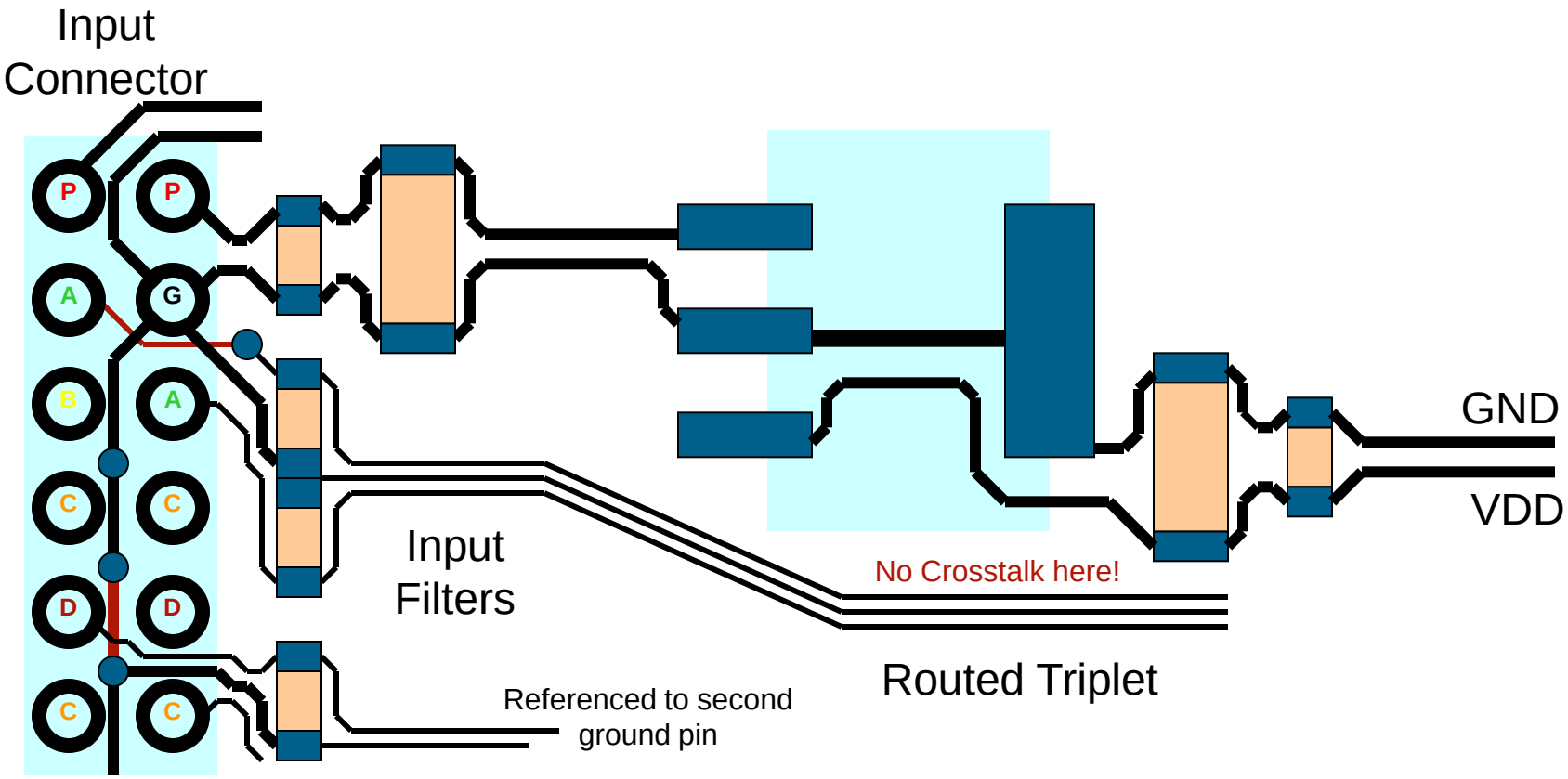
▶ PCB ~~Signal~~ TRANSMISSION LINE Routing



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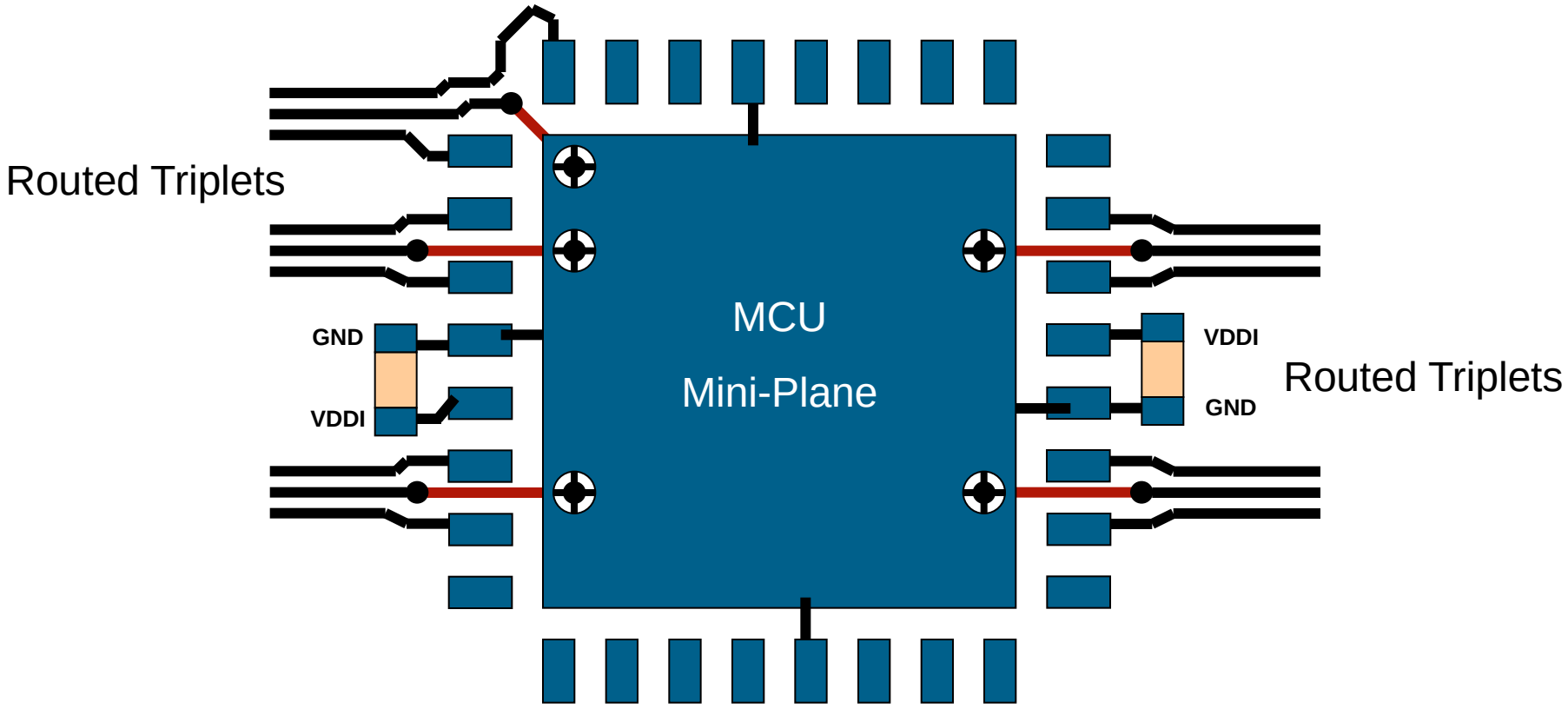

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PCB ~~Signal~~ TRANSMISSION LINE Routing

- Lead frame and wire bonds are parts of transmission lines, too.
- Mini-plane under the QFP provides improved EMC
- Triplet ground traces can be easily coupled to the Mini-plane on secondary side
- In high density applications, even routing with “Quints” (S-S-G-S-S) will provide some improvement
  - You know where most of the field energy is going!
- Last but not least, FLOOD everything with ground copper!
  - Must be able to tie each “island” with at least 2 via to adjacent layer ground

- Minimize the VOLUME of the Signal TRANSMISSION network

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- *Sure, but does this stuff REALLY work?*

- **Testing and Evaluation**

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The Proof is in the Testing

- **KIT33812ECUEVME Reference Design**
- Intended for motorcycle and other single/dual cylinder small engine control applications
- MC33812 analog power IC
  - Multifunctional Ignition and Injector Driver
- MC9S12XD128 MCU
  - Designed for either the MC9S12P128 or MC9S12XD128
  - Test results are for the older, noisier MCU
- Two Layer PCB
- Business Card dimensions
- Implements these Design and layout concepts
  - “Smart” connector pinout
  - MCU Mini-Plane
  - Triplet routing
  - Maximum Flooding

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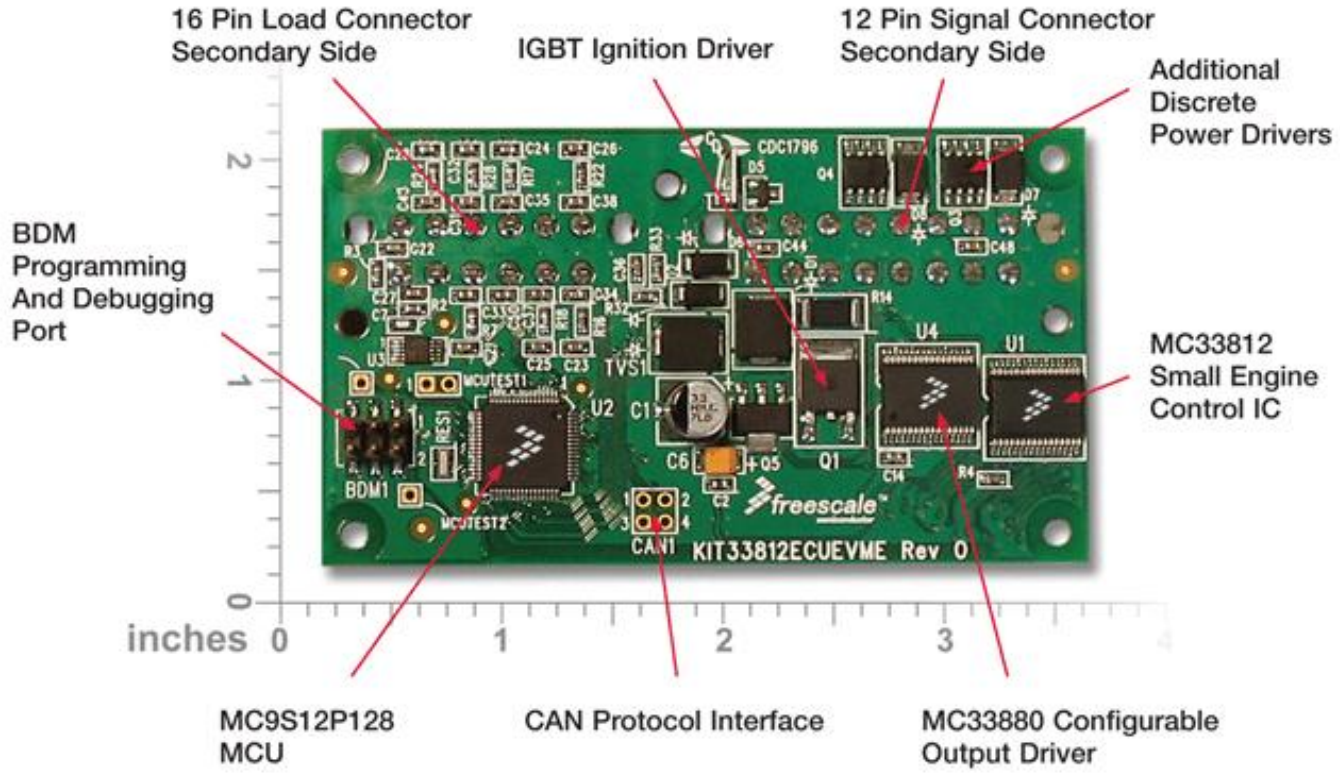

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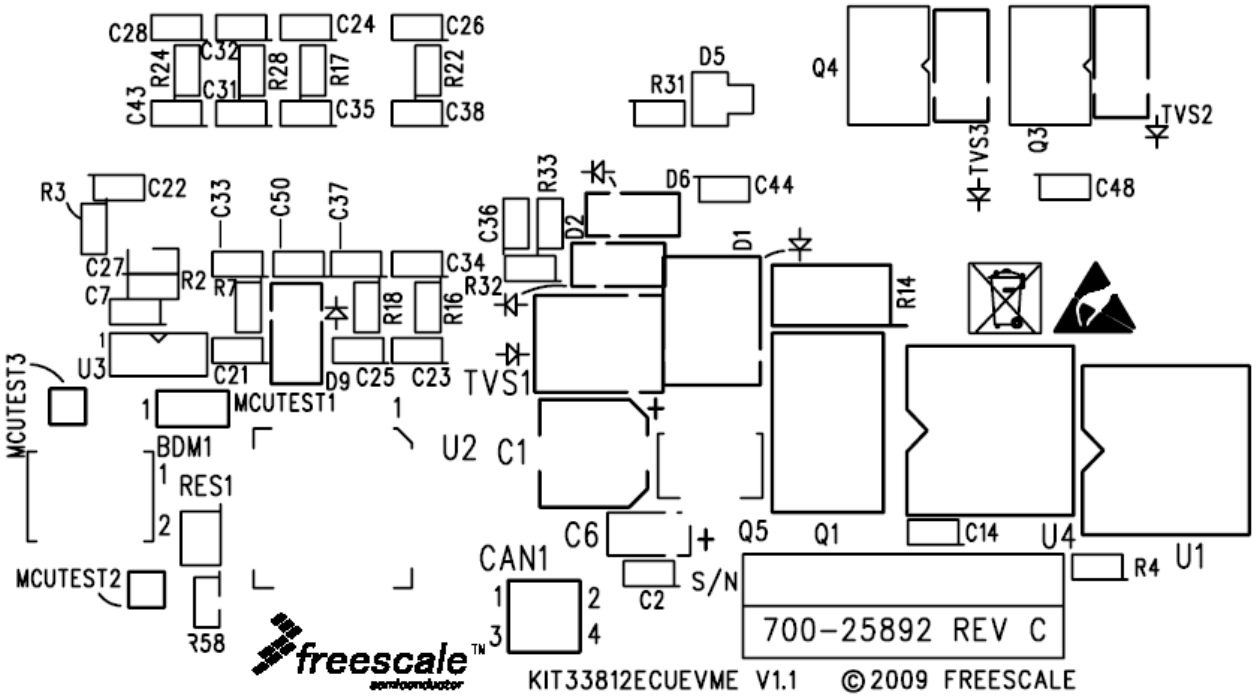
Primary Silk



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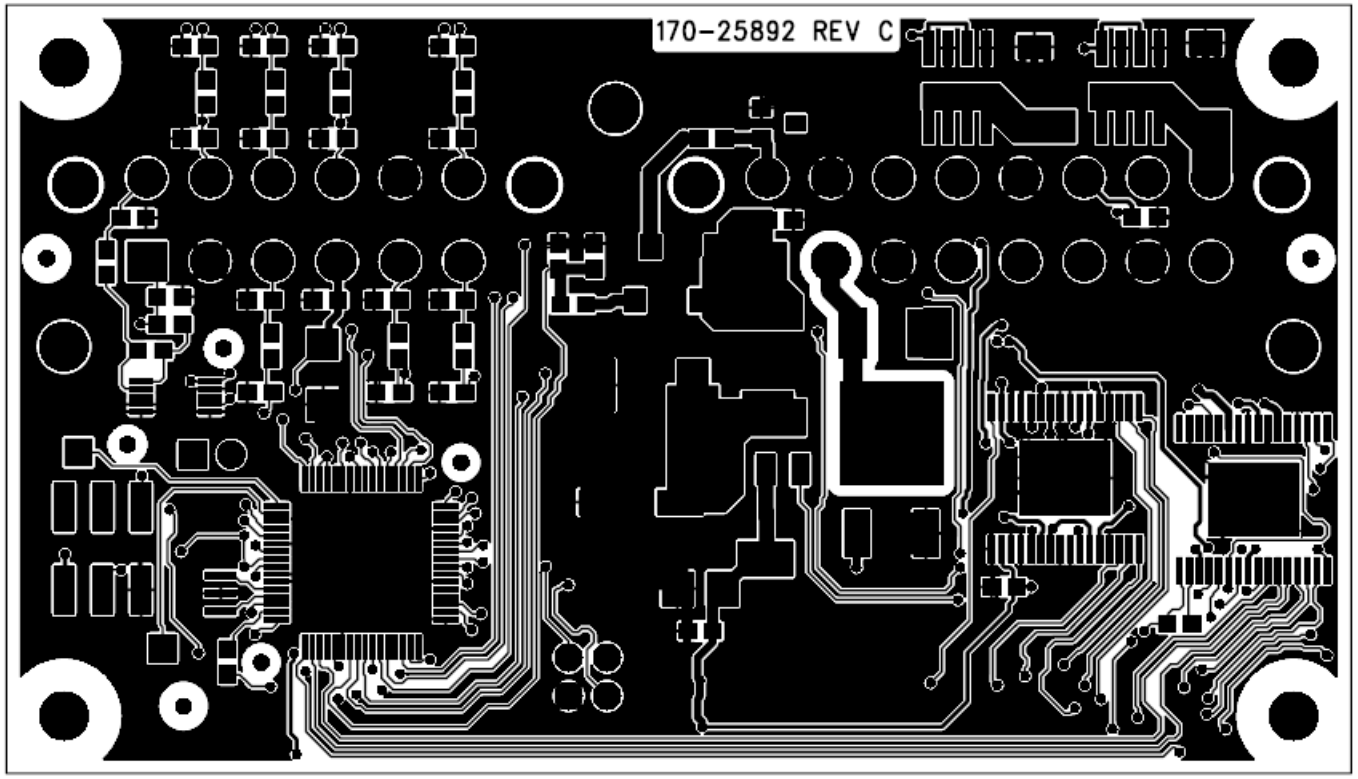
Primary Side



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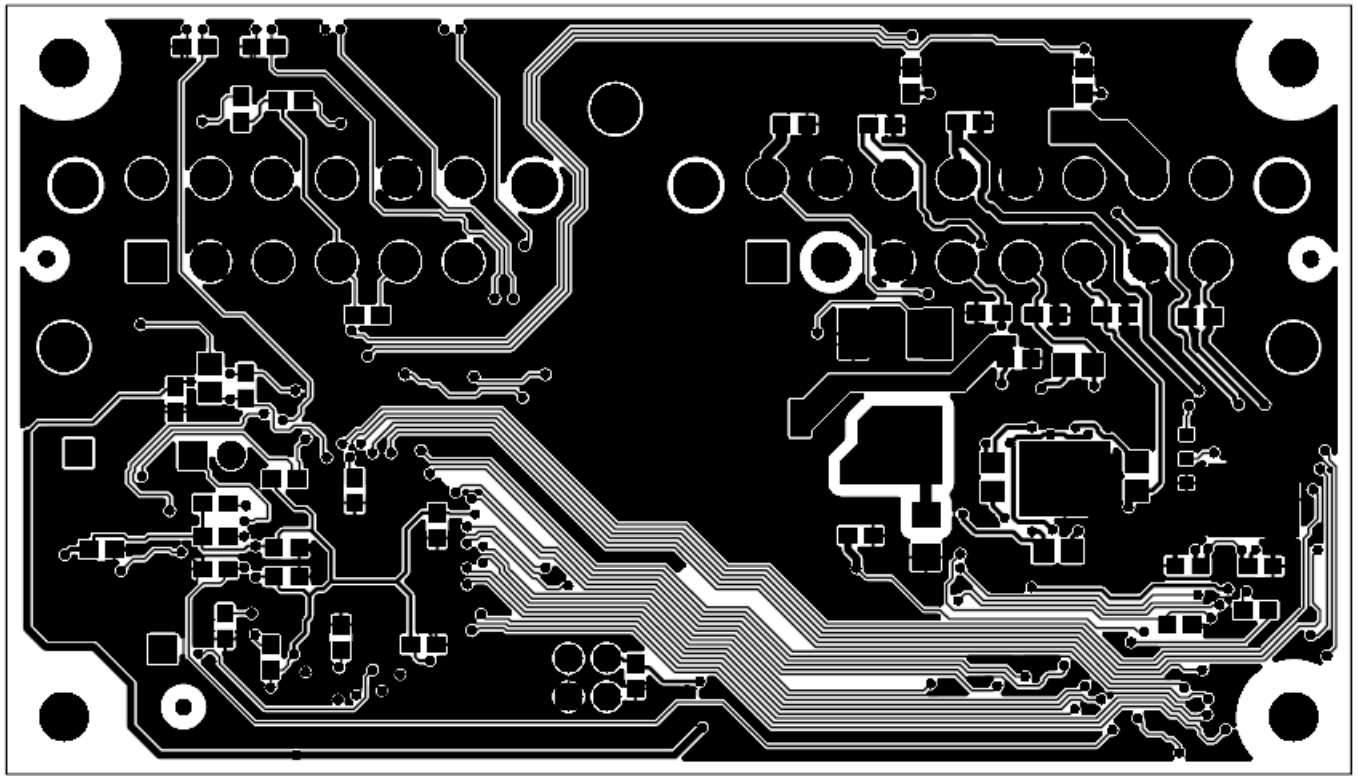
Secondary Side



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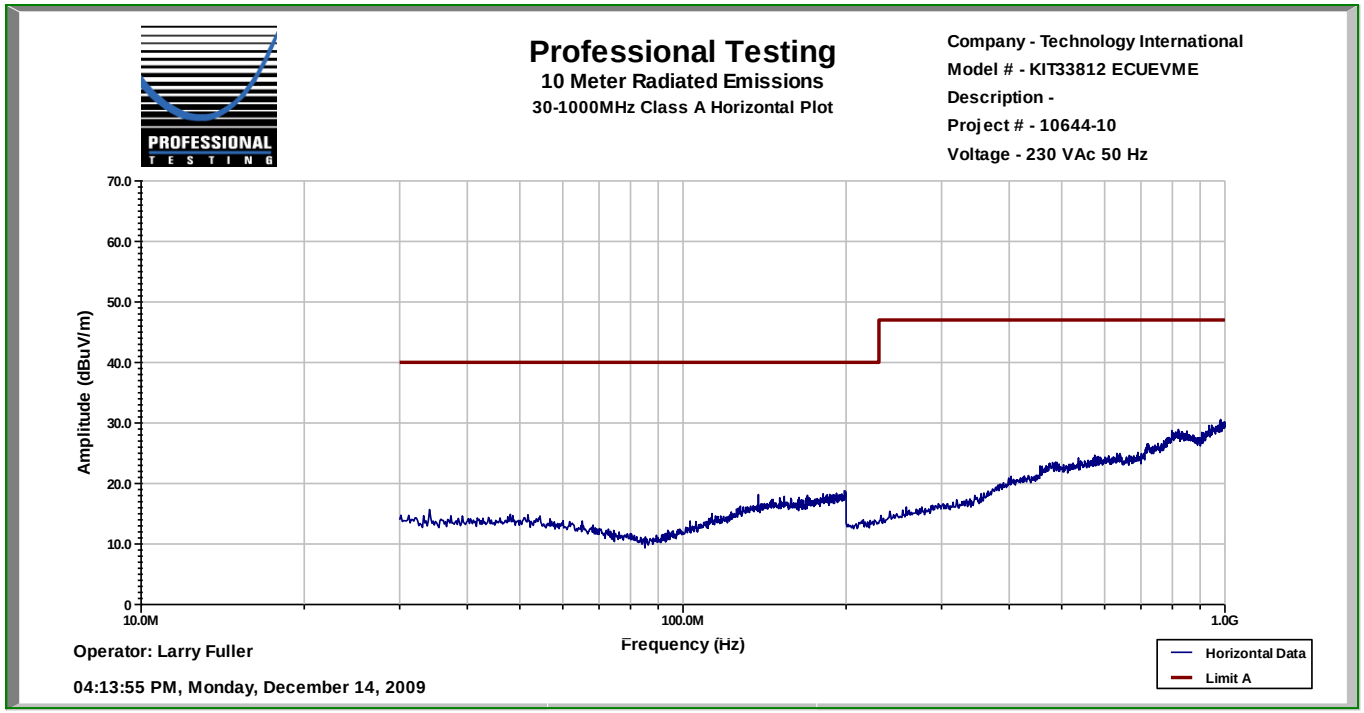

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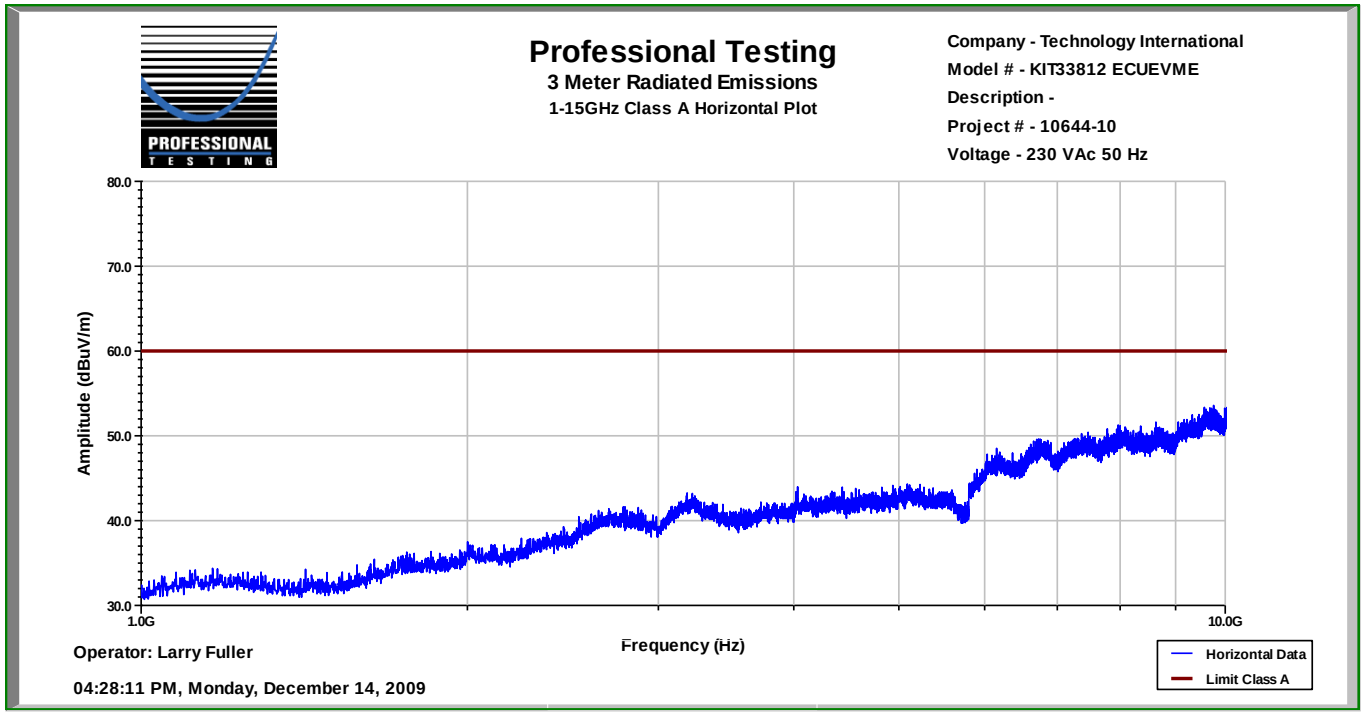

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EMC Test Board

- EMC test board with no Field control considered
- Two layers
- 112 pin MC9S12XD128 MCU
- All I/O lines routed to 10 K termination resistors using serpentine 6” traces
- All ground connections routed in “convenient” patterns
- Filter components placed “somewhere near”
- Line widths and spacing aimed for low cost FAB
- Software running at 40 MHz, toggling all I/O pins

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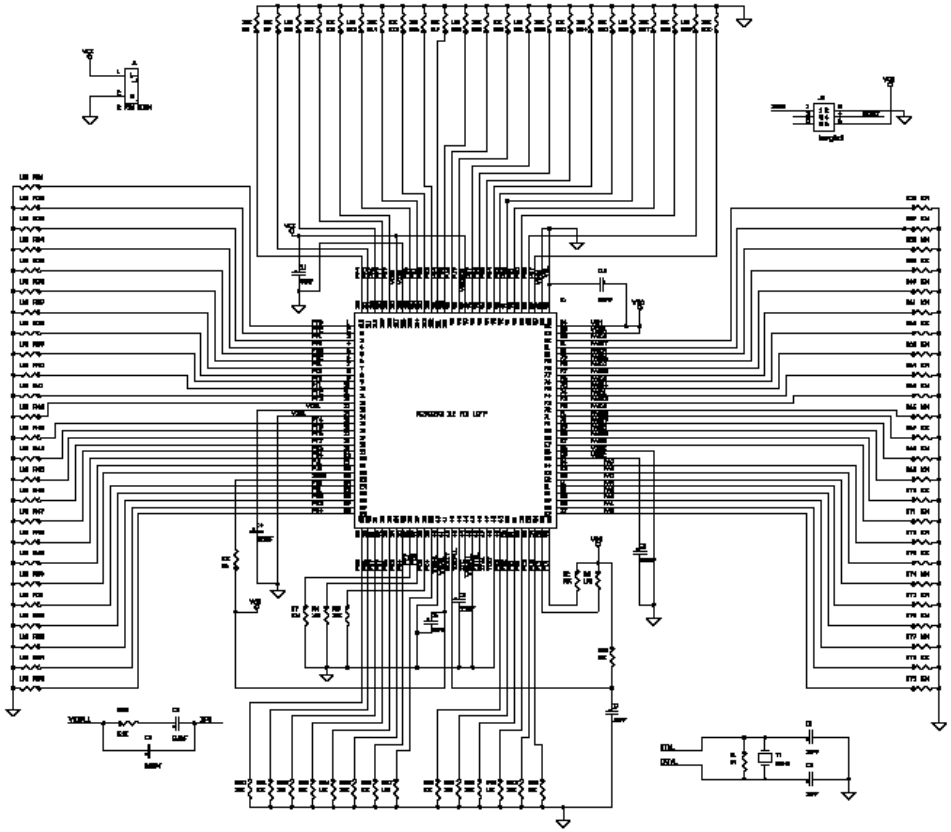
Effective PCB Design:
Techniques to improve performance



EMC Test Board Schematic

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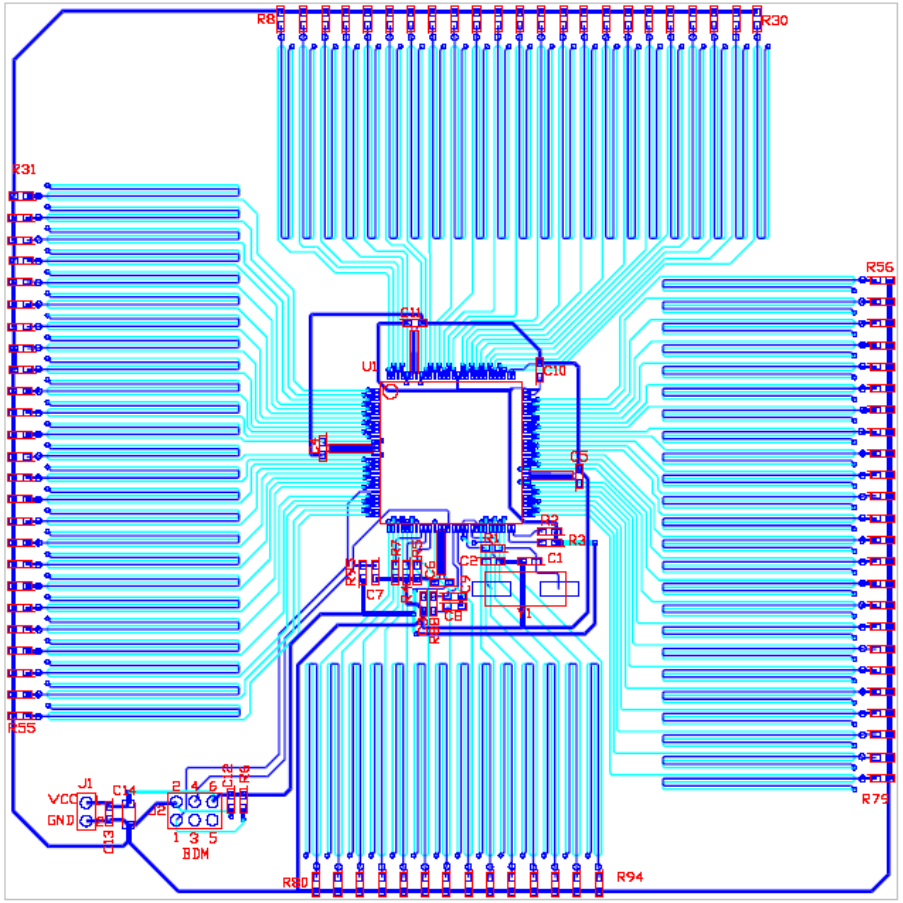
Techniques to improve performance



EMC Test Board Layout

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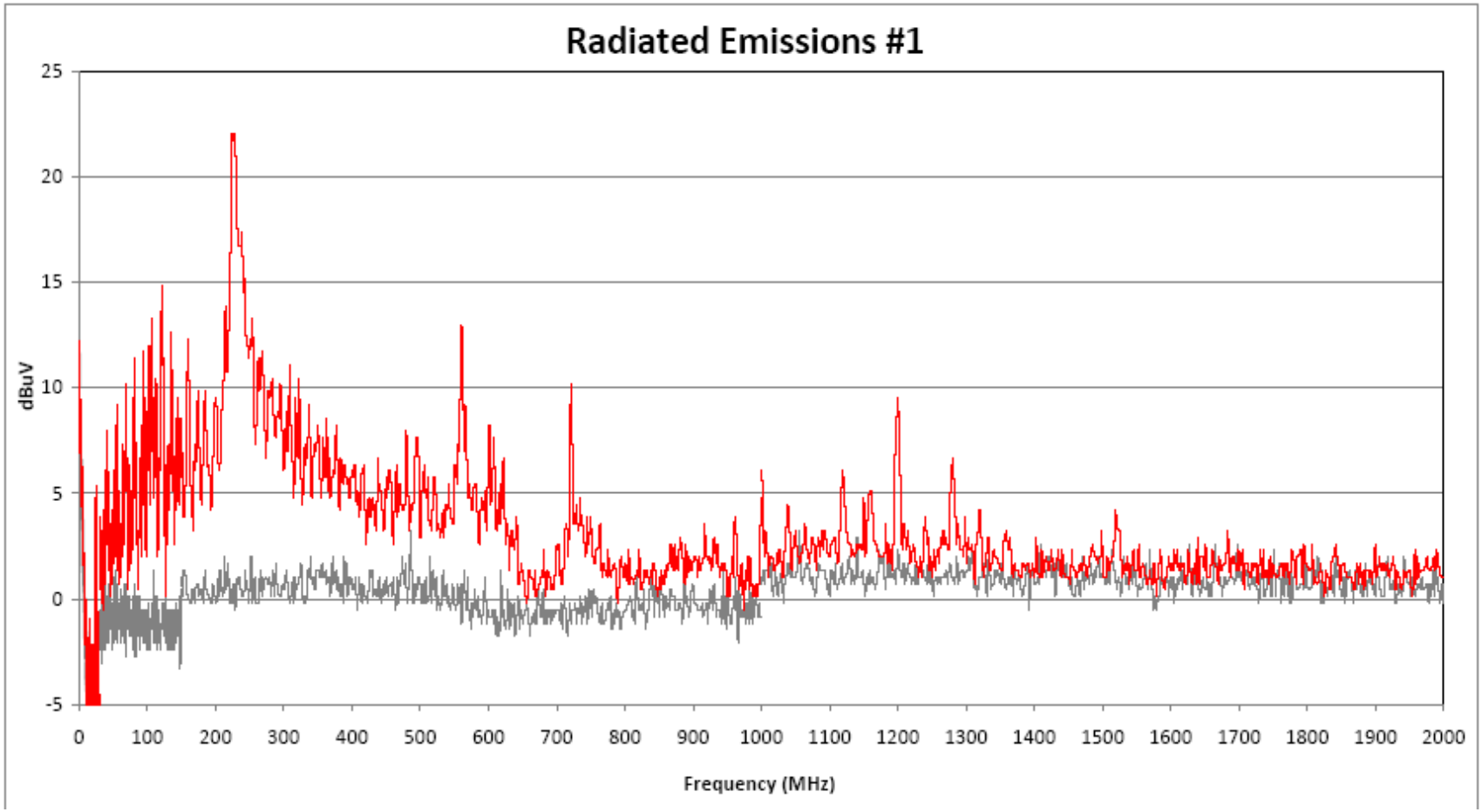
Techniques to improve performance



2 Layer EMC Test Board Radiated Emissions

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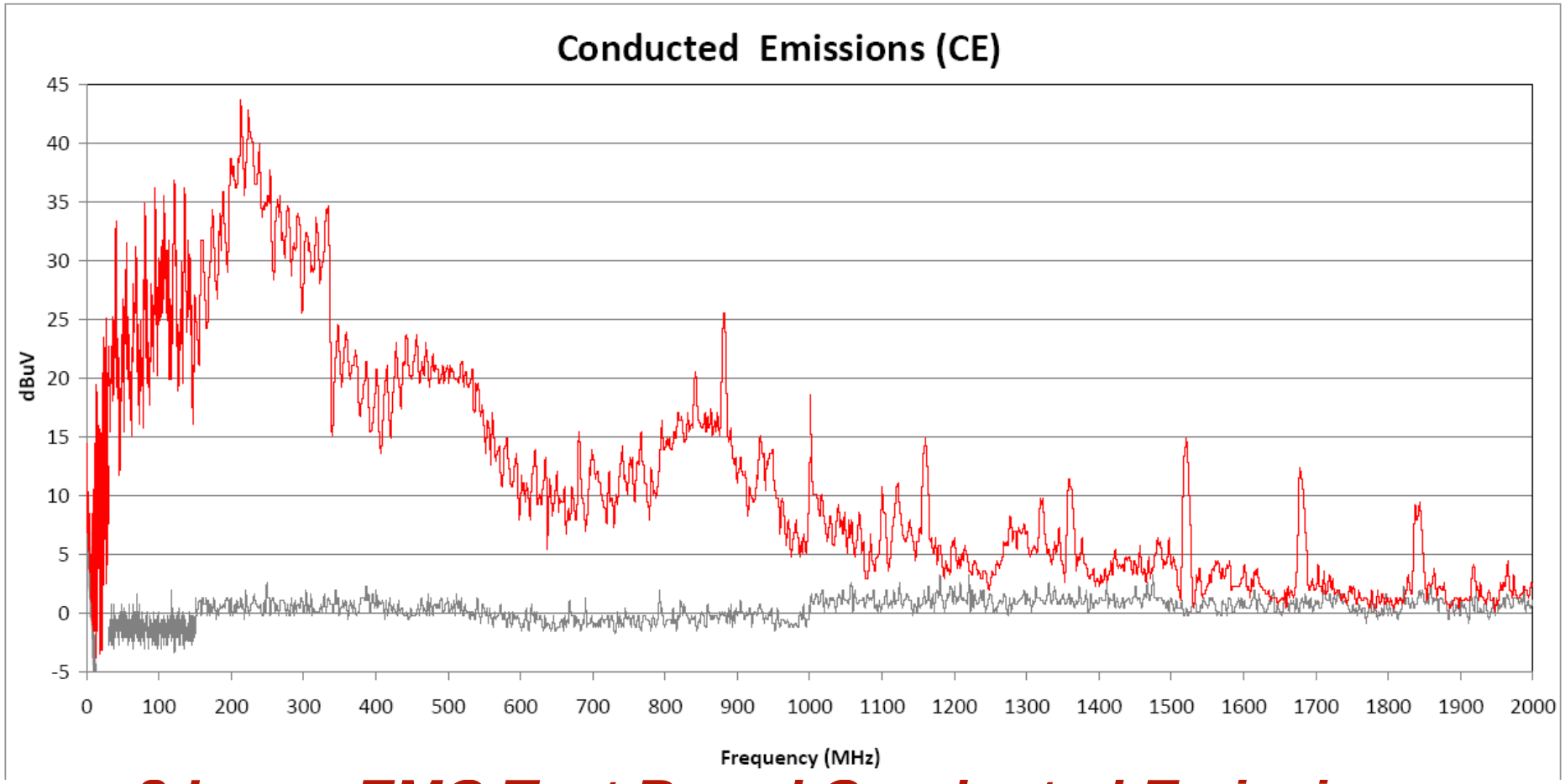
Effective PCB Design:
Techniques to improve performance



2 Layer EMC Test Board Conducted Emissions

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EMC Test Board, rev 2

- EMC test board with Tight Field control considered
- Same schematic
- Four layers
  - Core inserted with dedicated Ground Planes
- Outer layers exactly the same as 2 layer
- All ground connections made with via to ground planes
- Line widths and spacing aimed for low cost FAB
- Same software

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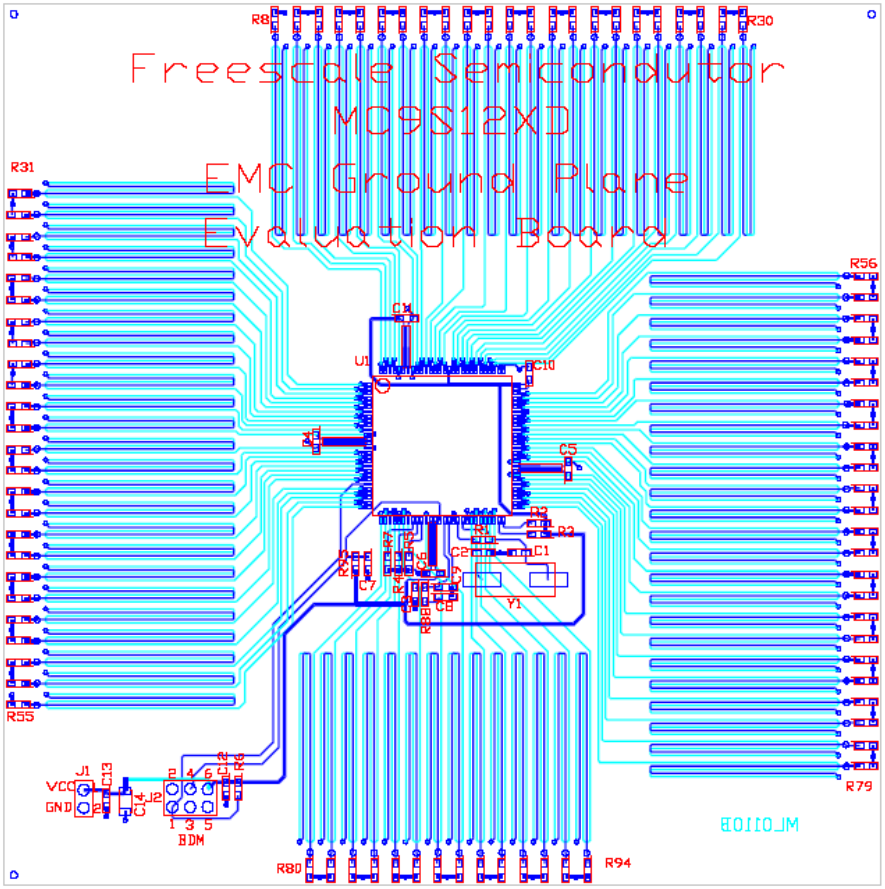
Effective PCB Design:
Techniques to improve performance



EMC Test Board Layout

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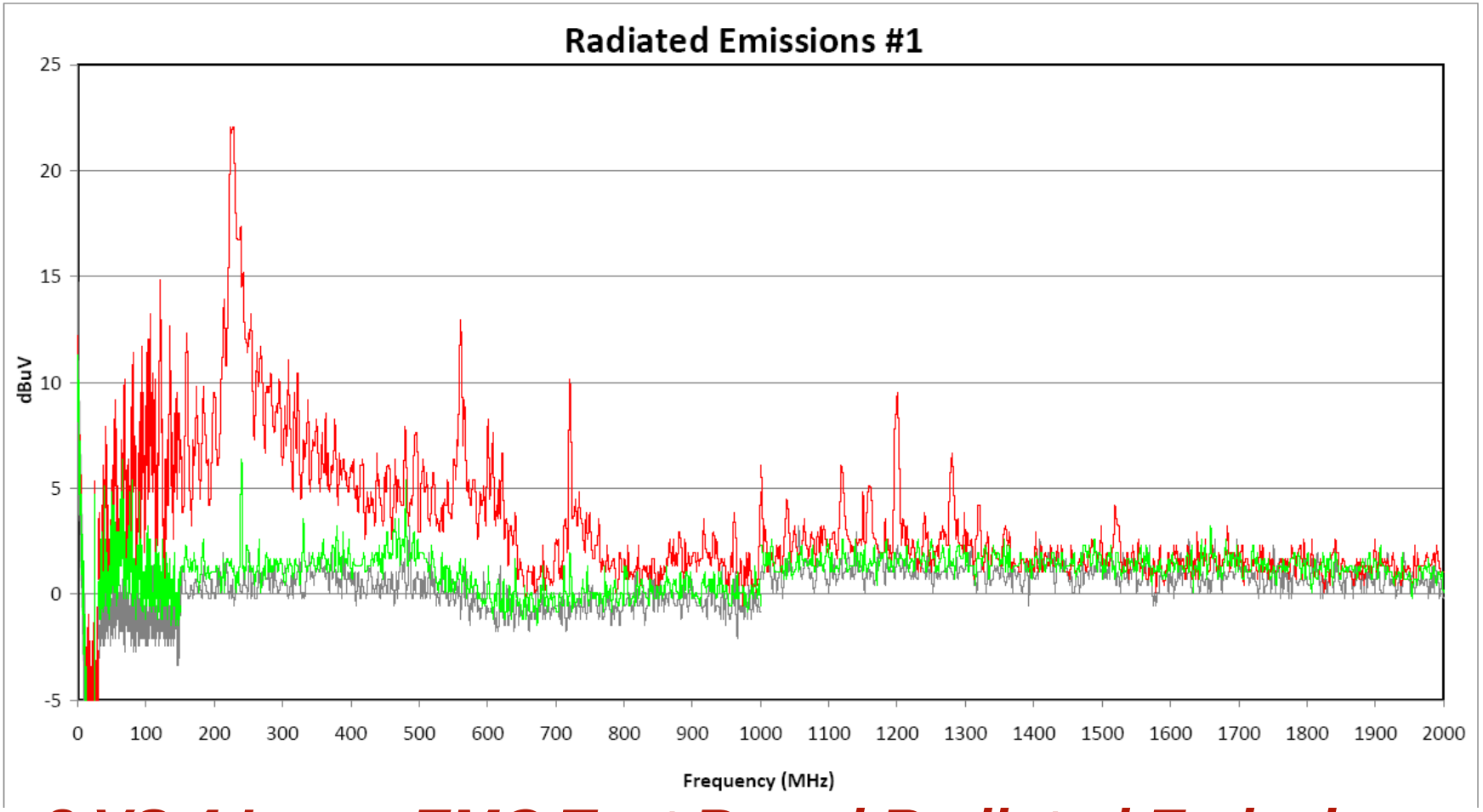

2 VS 4 Layer EMC Test Board Radiated Emissions

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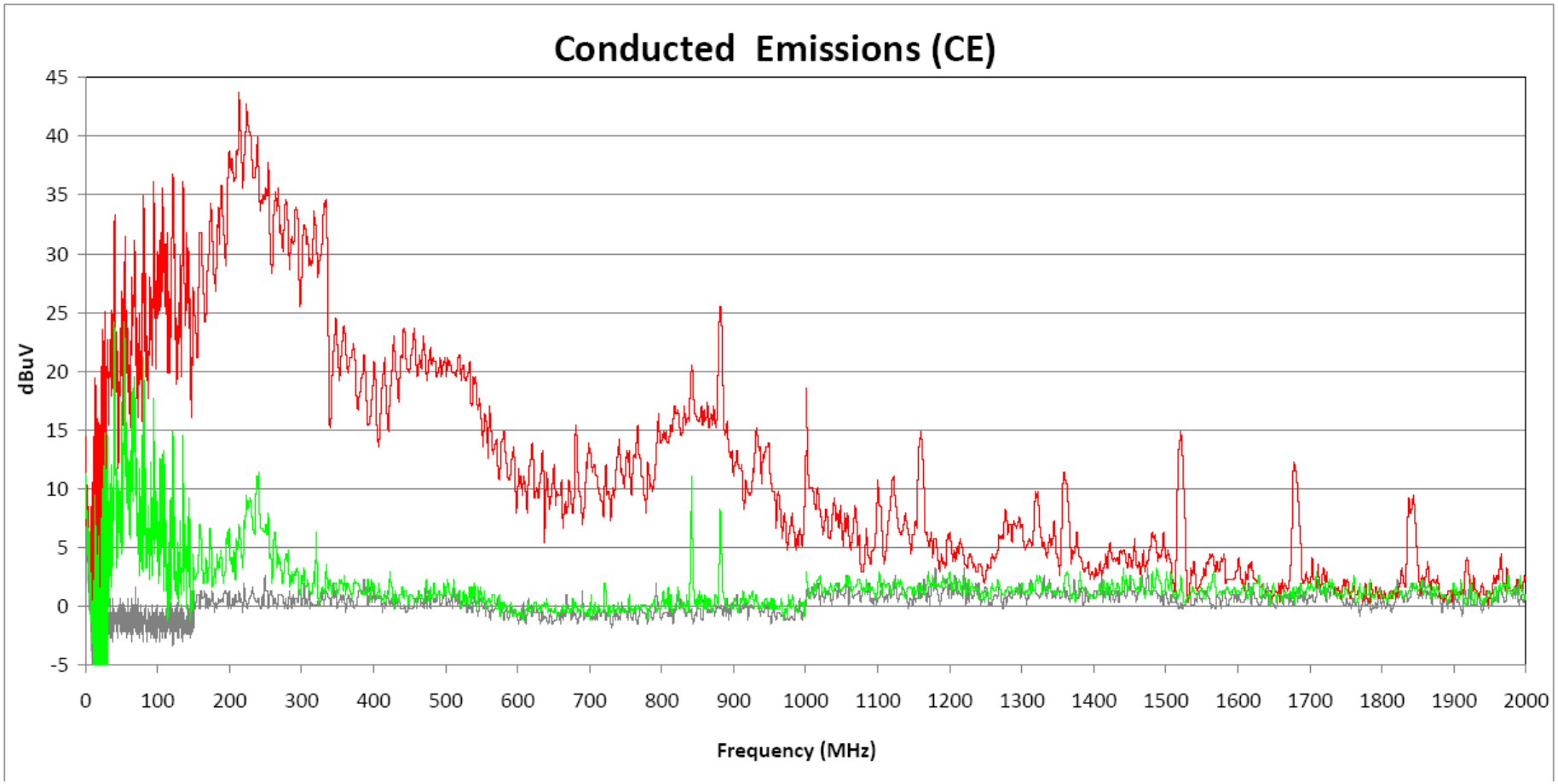

2 VS 4 Layer EMC Test Board Conducted Emissions

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WOW!

What would you do for 30 db?

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EMC Test Results

- EMC test results can be used to identify area of concern
- LFBDMPGMR FCC/CE test result first pass:
  - Radiated Immunity
  - "The EUT failed with all led's turning off. Manual restart worked. The frequencies that caused this fault were 110 MHz, 112 MHz, 134 MHz, and 136 MHz up to 149 MHz. After 149 MHz the EUT worked properly."
- Not what you want to see in your email
- This is a 4 layer board, the best I know how to design!!??
- I know, check the chart to see what the ¼ wave length would be
- About 1 meter, what? My board is only 4 inches square.
- Aha, the USB cable!! I forgot to put a filter on the USB power supply. Add a cap quick.
- Send new board for retest

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▶Antenna size vs. Frequency

Frequency	¼ wave length
1 Hertz Rise time equivalent, who cares	246,000,000 feet (46,591 miles) Almost 6 times around the earth
10 Hertz Rise time equivalent, still who cares	24,600,000 feet (4,659 miles) Almost from New York to Honolulu
100 Hertz Rise time equivalent, .01 seconds	2,460,000 feet (466 miles) Almost from New York to Detroit
1 KHz Rise time equivalent, 1 millisecond	246,000 feet (46.6 miles) Almost from Orlando to Cocoa Beach
10 KHz Rise time equivalent, 100 microseconds	24,600 feet (4.659 miles) Almost from the J. W. Marriott to Disney's Magic Kingdom
100 KHz Rise time equivalent, 10 microseconds	2,460 feet (0.466 miles) Almost from the J. W. Marriott to the Central Florida Parkway
1 MHz Rise time equivalent, 1 microsecond	246 feet (0.0466 miles) Less than a football field
10 MHz Rise time equivalent, 100 nanoseconds Rise time distance, 100 feet	24.6 feet Across the room
100 MHz (TTL Logic) **Rise time equivalent, 10 nanoseconds Rise time distance, 10 feet**	**2.46 feet** **Less than a yard**
1 GHz (BiCMOS Logic) Rise time equivalent, 1 nanosecond Rise time distance, 1 foot	0.246 feet (2.952 inches) Less than your finger
10 GHz (GaAs Logic) Rise time equivalent, 100 picoseconds Rise time distance, 1.2 inches	0.0246 feet (0.2952 inches) Less than the diameter of a pencil
100 GHz (nanometer geometry HCMOS) Rise time equivalent, 10 picoseconds Rise time distance, 0.12 inches	0.00246 feet (0.0295 inches) Half the thickness of a standard FR4 PCB

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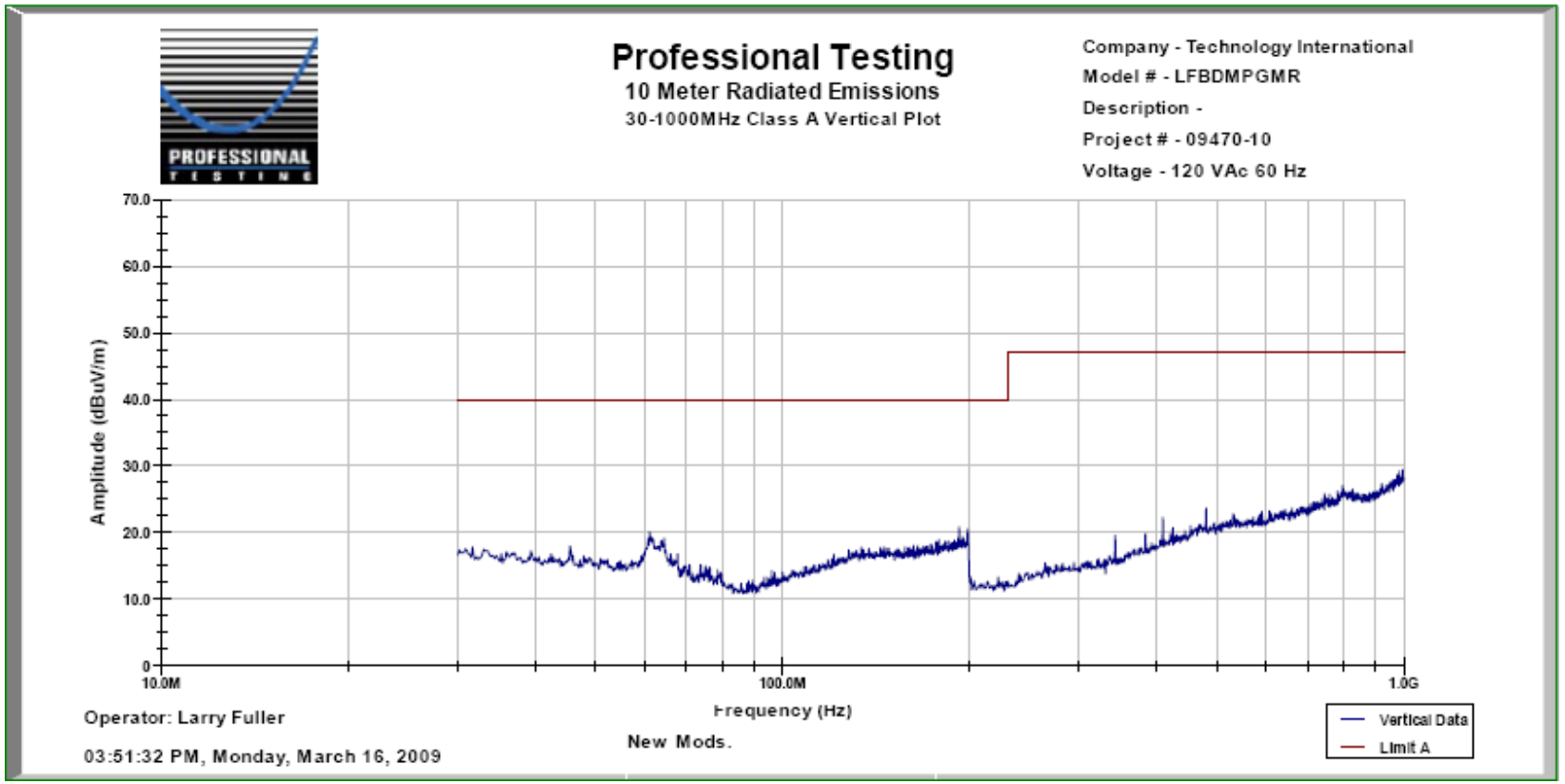
EMC Test Results



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EMC Test Results, Yeah!!

EN 61000-4-3
Radiated Immunity
Technology International
LFBDMPGMR

Test Date: March 13, 2009	**Client: Technology International**
Project #: 09470-10	**Supervisor: Jason Anderson**
EUT: LFBDMPGMR	**Technician: Dan Keenan**

EUT Power Source: 120VAC
Ambient Temperature: 22.6 ° C
Barometric Pressure: 29.97 inches
Relative Humidity: 55 %

EUT Face Illuminated	Frequency Range							
	80-200 MHz		200-1000 MHz		1.4-2.0 GHz		2.0-2.7 GHz	
	3 V/m		3 V/m		V/m		V/m	
	Horizonta l	Vertica l	Horizonta l	Vertica l	Horizonta l	Vertica l	Horizonta l	Vertica l
Front	X	X	X	X				
Right	X	X	X	X				
Rear	X	X	X	X				
Left	X	X	X	X				

Test Results: Pass [X] Fail [ ]

The EUT met performance criteria:

Criteria A	[X]
Criteria B	[ ]
Criteria C	[ ]
Manufacturers Specification	[ ]

Notes: The RF signal was modulated with 80% 1000 Hz modulation. The frequency step size was 1% of the preceding frequency. The dwell time at each frequency was 2 seconds.

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- *PCB Layout Considerations*

- **Some new “Rules of Thumb”**

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More PC Board Considerations

- Flooding unused spaces on the PCB
  - Properly implemented will improve EMC performance
  - Reduce cost by increasing PCB manufacturing yield
    - Less etch required
    - Balanced copper improves plating
    - Balanced copper improves final assembly
      - Reduced board warping

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More PC Board Considerations

- Use the minimum trace widths and spacing for signal transmission lines
  - Refer to PCB fabricator's capabilities without a cost adder
  - May be defined by either customer or internal requirements
  - Wider traces for power supply transmission line pairs
  - Provides maximum trace density
- Makes room for all of those ground traces!

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More PC Board Considerations

- Four layer boards
  - Made from a 2 layer core, L2 and L3
  - L1 and L4 made by adding pre-preg layers and copper foil
  - Use the “fattest” core and “thinnest” pre-preg possible without a cost adder from fabricator
    - You will have to find this out
    - Your company or customer may have some min-max specs for these materials
  - Maximum coupling is from L1 to L2 and from L3 to L4

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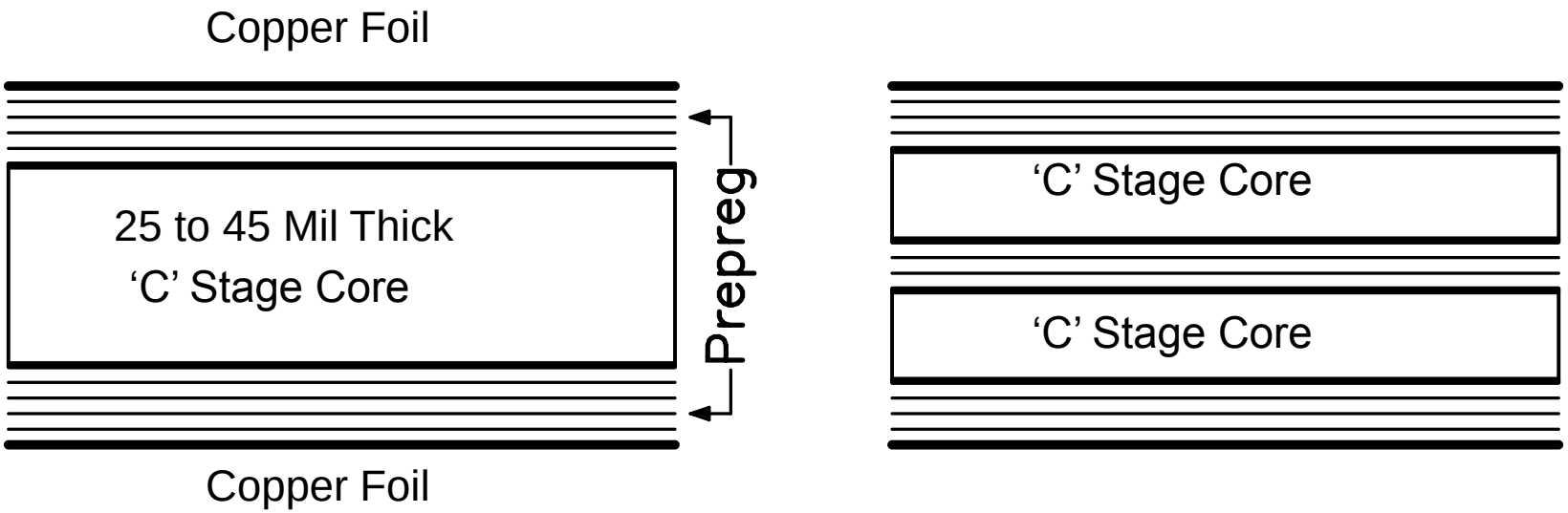
Techniques to improve performance



Most PC Boards are "Foil Laminated"

Slide compliments of Rick Hartley, Consultant

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More PC Board Considerations

- Layer count determinations
  - Technology of the devices used
  - Trace density
  - EMC certification level
    - Consumer/Commercial
    - Automotive
    - Aviation
    - Military, etc.

All must be considered, not just Trace Density!!!

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▶More PC Board Considerations

- Layer count determinations
  - Must be a conscious decision based on proper electromagnetic field control
  - Not just because you ran out of routing paths
  - Smaller IC geometries will require more layers and most likely power and ground planes
  - It will not be possible to provide a good power distribution network or good signal integrity without adding planes

▶System cost is ***NOT*** reduced by reducing IC geometries!!

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- More PC Board Considerations

I repeat:

System cost is ***NOT*** reduced by reducing IC geometries!!

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More PC Board Considerations

- Using Planes
  - Both Power and Ground can be used as signal references
    - ONLY if they are well coupled to each other
      - Capacitors
      - Adjacent to each other
  - Transition from one reference plane to another requires close proximity to a bypass capacitor
    - That is the only way the energy can go!

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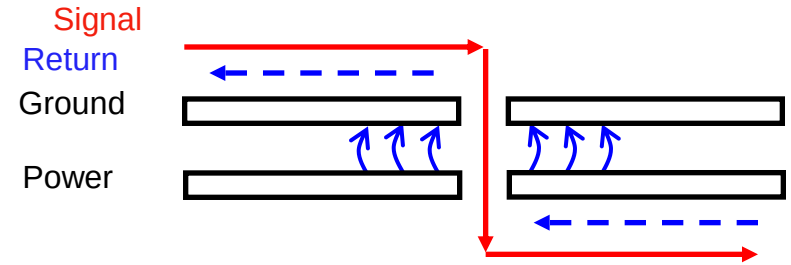
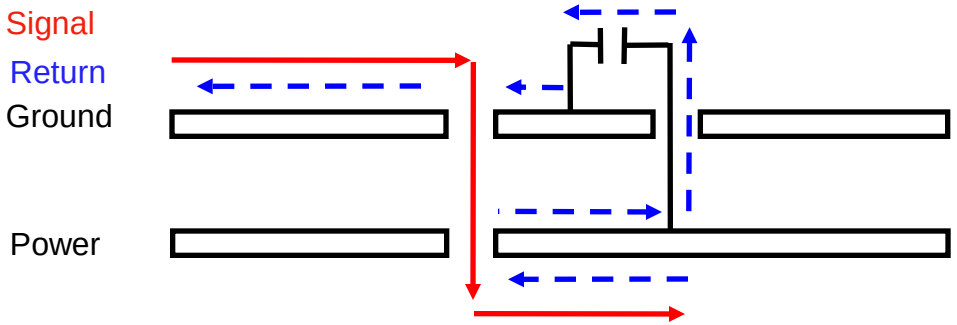
- When routing signals with returns between Power and Ground Planes, Return energy will transfer as follows -



Tightly Coupled Planes



Loosely Coupled Planes w/ Cap

Slide compliments of Rick Hartley, Consultant

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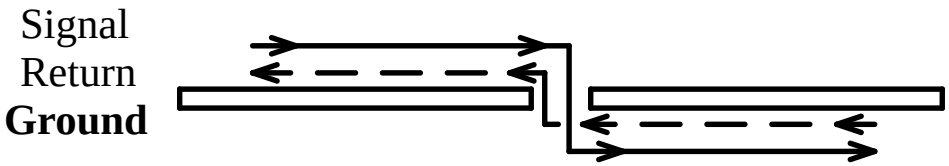
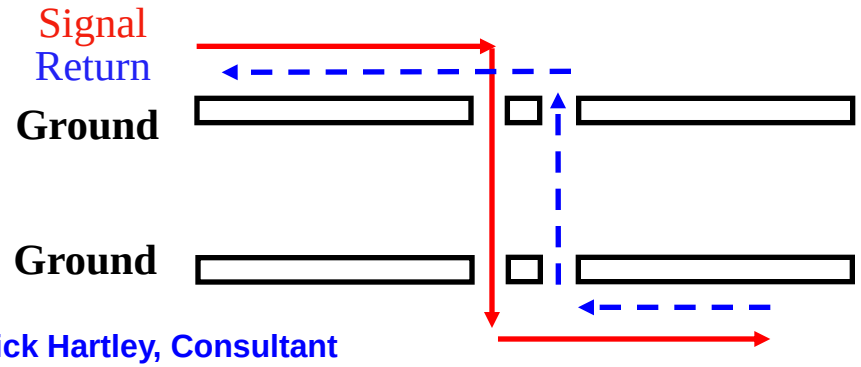
- **When moving signals between layers, route on either side of the same plane, as much as possible!!!**



- **When moving signals between 2 different planes, use a transfer via VERY near the signal via.**



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More PC Board Considerations

- Remember, Field energy moves in the space between or around the conductors and cannot go through them [1]
  - That means through the holes in the planes
    - Not inside or on the vias, around them!!
- You must provide the path you want, or the field will find its own path
  - It will most likely be the one that causes the most problems!

[1] **Statement compliments of Ralph Morrison, Consultant**

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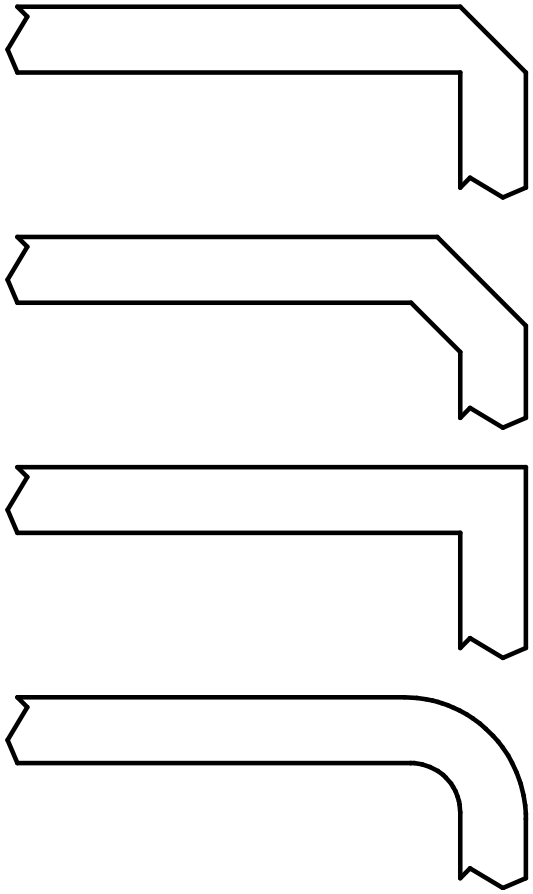
- PCB Trace Corners -



90 Degree Corner,
Cut at 45 Degrees.

45 Degree Corner.

90 Degree Corner.

Radius at Corner.

Which of these is BEST?

Slide compliments of Rick Hartley, Consultant

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More PC Board Considerations

- These small discontinuities are virtually invisible for all applications in the foreseeable future
- The best one is the 45 degree, because it is easier to manufacture and easier to draw!
- The 90 degree choices tend to be victims of under or over etching, and can form failure points in the future, as well as impacting PCB yields
- The radius is good, but most CAD packages do not support this option

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More PC Board Considerations

- Using Planes
  - Splitting Ground Planes is almost never a good idea
    - Only when required by customer or internal specifications
    - Question those requirements!!
  - If you have to split a plane, do not route traces across the split!
    - If you must, then you absolutely have to route a following ground trace across the split next to the signal trace

Splits in Planes are very efficient Slot Antennas!!

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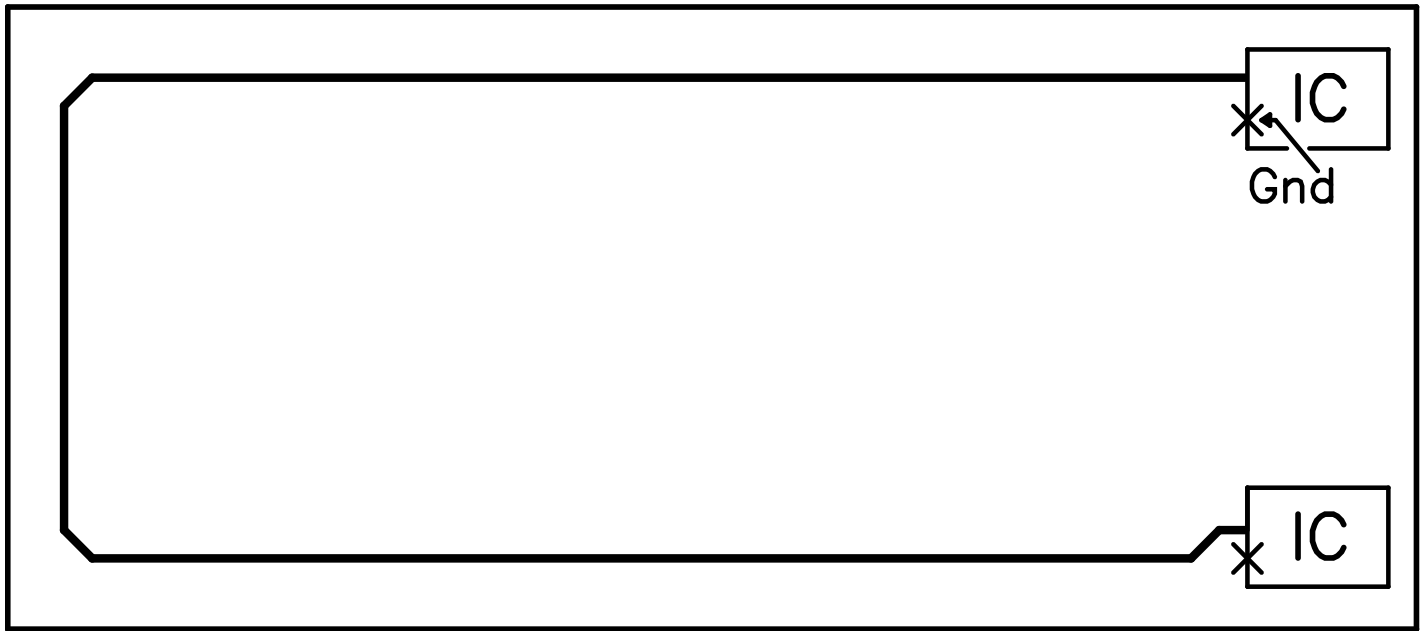
- 2 Layer Microwave Style PC Board -

L2- Ground.



Where does signal's return current flow?

Slide compliments of Rick Hartley, Consultant

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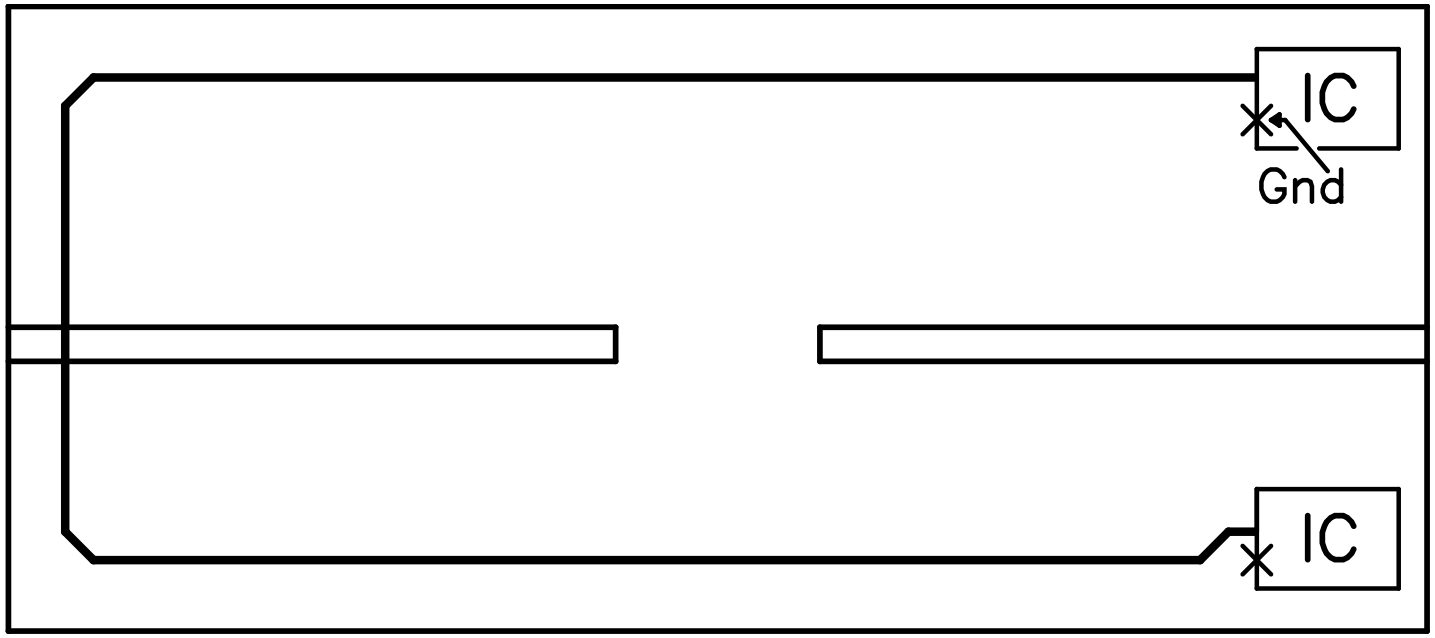
- What happens if Return Plane is Split???
  - Now where does return current flow?



Where does signal's return current flow?

Slide compliments of Rick Hartley, Consultant

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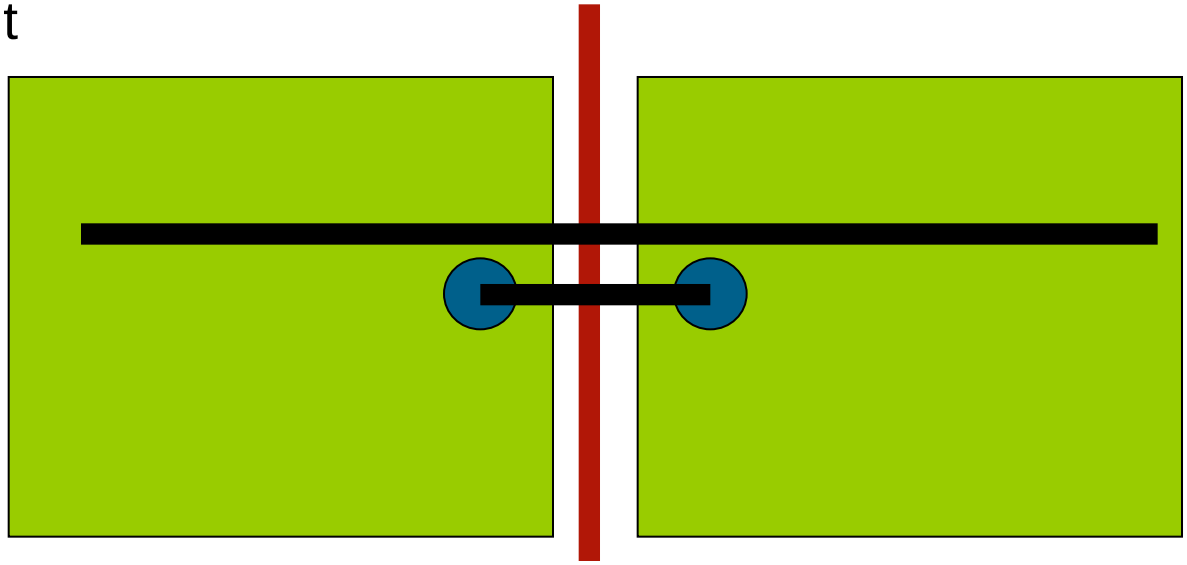
More PC Board Considerations

- Routing over Split Planes, Same Potential
  - Just use a bridge tied to each plane
  - Better to just not split it, but sometimes you have to route a trace in the split



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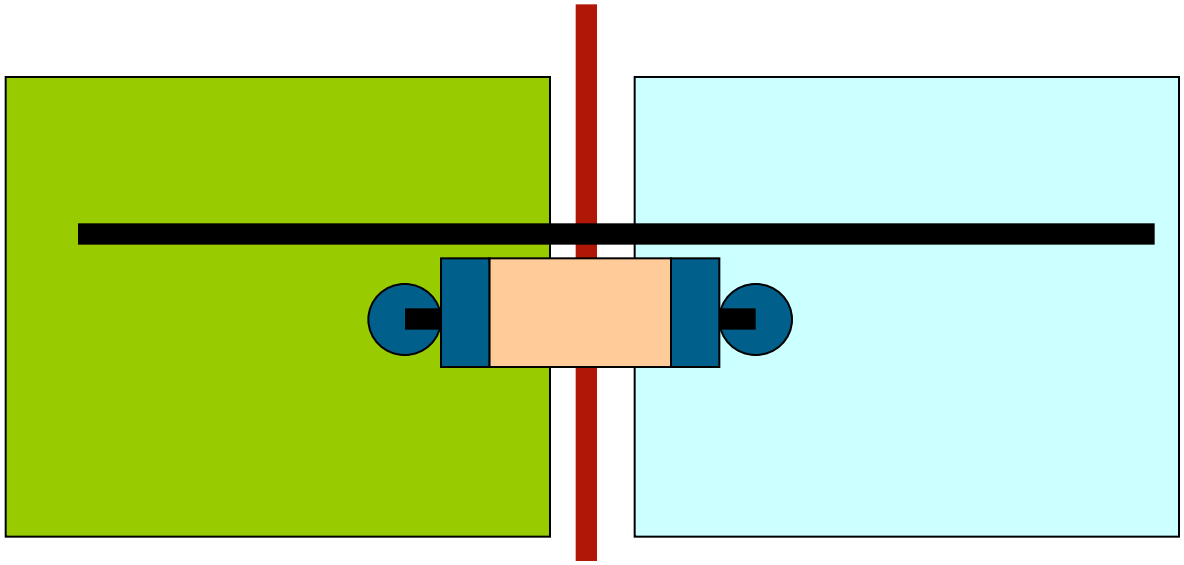
More PC Board Considerations

- Routing over Split Planes, Different Potential
  - Have to bridge with a capacitor



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More PC Board Considerations

- Routing Differential signals
  - Myth: They are coupled to each other
  - Fact: They are coupled to Ground
  - They do not have to be routed together
  - They do need to be about the same length
  - They do need to be treated as transmission lines
    - You knew I was going to say that, didn't you?
  - They would benefit from being routed as a "Triplet"
  - Designed to reject Common Mode noise

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More PC Board Considerations

- Routing Timing Critical Bus Signals
  - Myth: They have to be exactly the same length
    - Manufacturers often spec allowable trace length differential
    - PCB designers spend a lot of time and energy to do this using serpentines and other extreme routing methods
    - At high frequency, the serpentines are invisible anyway, and actually result in SHORTER travel times
  - Fact: What matters is the set up and hold time required by the devices
    - This is usually specified in time, i.e. ps
    - Remember this? **v = 150 mm / ns or 6" / ns**
- For a typical 500 MHz DDR memory interface, the data lines *only* need to be within 500 mils of each other in length [2]
  - Way easier than we have been led to believe

[2] **Statement compliments of Rick Hartley, Consultant**

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- Closing Remarks and Reference Materials

- **PCB Design is not a Black Art!**

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Effective PCB Design:
Techniques to improve performance

- Well defined transmission lines result in significantly improved EMC performance
- Careful routing of transmission lines can result in behavior similar to that gained by adding extra PCB ground layers
- Evaluating test results can lead you to solutions
- The Black Magic is tamed!

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▶My special thanks and accolades to my patient and extremely tolerant mentors:

- Rick Hartley, PCB designer extraordinaire, who started me down this trail in 2004 at PCB West.
- Ralph Morrison, Author, Inventor, and Musician, who has patiently and steadily moved me from the fuzzy realm of “Circuit Theory” and “Black Magic” into the solid world of physics.
- Dr. Todd Hubing, Researcher and Professor, whose research at UMR and Clemson have provided solid evidence that Maxwell and Ralph have got it right!

▶Finally, My team here at Freescale, we have really come a long way!

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High Speed Design Reading List

- 1. Right the First Time- A Practical Handbook on High Speed PCB and System Design - Volumes I & II - Lee W. Ritchey (Speeding Edge) - ISBN 0-9741936-0-7
- 2. High Speed Digital System Design- A handbook of Interconnect Theory and Practice - Hall, Hall and McCall (Wiley Interscience 2000) - ISBN 0-36090-2
- 3. High Speed Digital Design- A Handbook of Black Magic - Howard W. Johnson & Martin Graham (Prentice Hall) - ISBN 0-13-395724-1
- 4. High Speed Signal Propagation- Advanced Black Magic - Howard W. Johnson & Martin Graham - (Prentice Hall) - ISBN 0-13-084408-X
- 5. Signal Integrity Simplified - Eric Bogatin (Prentice Hall) - ISBN 0-13-066946-6
- 6. Signal Integrity Issues and Printed Circuit Design - Doug Brooks (Prentice Hall) - ISBN 0-13-141884-X

[2] **Slide compliments of Rick Hartley, Consultant**

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EMI Reading List

- 1. PCB Design for Real-World EMI Control - Bruce R. Archambeault (Kluwer Academic Publishers Group) - ISBN 1-4020-7130-2
- 2. Digital Design for Interference Specifications- A Practical Handbook for EMI Suppression - David L. Terrell & R. Kenneth Keenan (Newnes Publishing) - ISBN 0-7506-7282-X
- 3. Noise Reduction Techniques in Electronic Systems - Henry Ott (2nd Edition - John Wiley and Sons) - ISBN 0-471-85068-3
- 4. Introduction to Electromagnetic Compatibility - Clayton R. Paul (John Wiley and Sons) - ISBN 0-471-54927-4
- 5. EMC for Product Engineers - Tim Williams (Newnes Publishing) - ISBN 0-7506-2466-3
- 6. Grounding & Shielding Techniques - Ralph Morrison (5th Edition - John Wiley & Sons) - ISBN 0-471-24518-6

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Some additional references you may find useful:

- http://www.ralphmorrison.com/Ralph_Morrison/Welcome.html
- Ralph Morrison's website

- http://pcbwest.com/
- Best PCB design conference website

- http://www.emcesd.com/
- Doug Smith's website (He is the best at finding what is wrong! Lots of useful apnotes.)

- http://www.emcs.org/
- IEEE EMC Society website

- http://www.cvel.clemson.edu/auto
- Clemson's Automotive Electronics website

- http://www.cvel.clemson.edu/emc
- Clemson's EMC website

- http://www.mst.edu/about/
- Missouri University of Science and Technology website

- http://www.ipc.org/default.aspx
- IPC — Association Connecting Electronics Industries website

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- *"Buildings have walls and halls.*

  *People travel in the **halls** not the walls.*

- *Circuits have traces and spaces.*

  *Energy and signals travel in the **spaces** not the traces"*

Ralph Morrison

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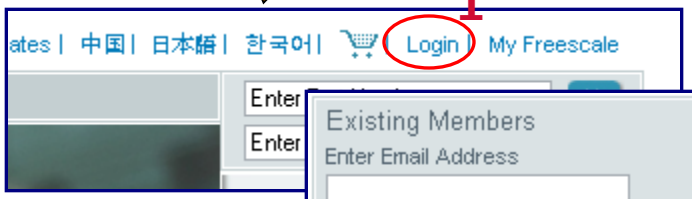

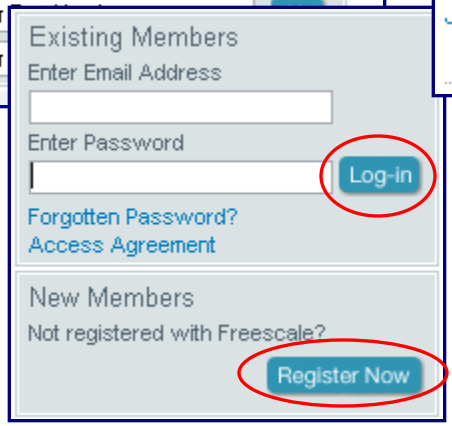

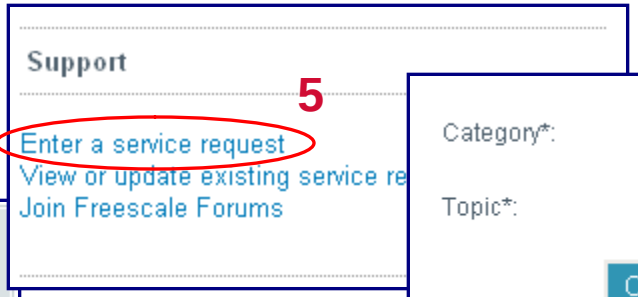

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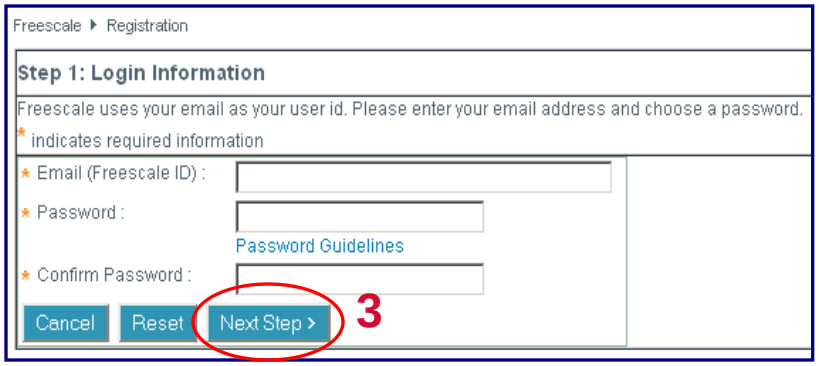

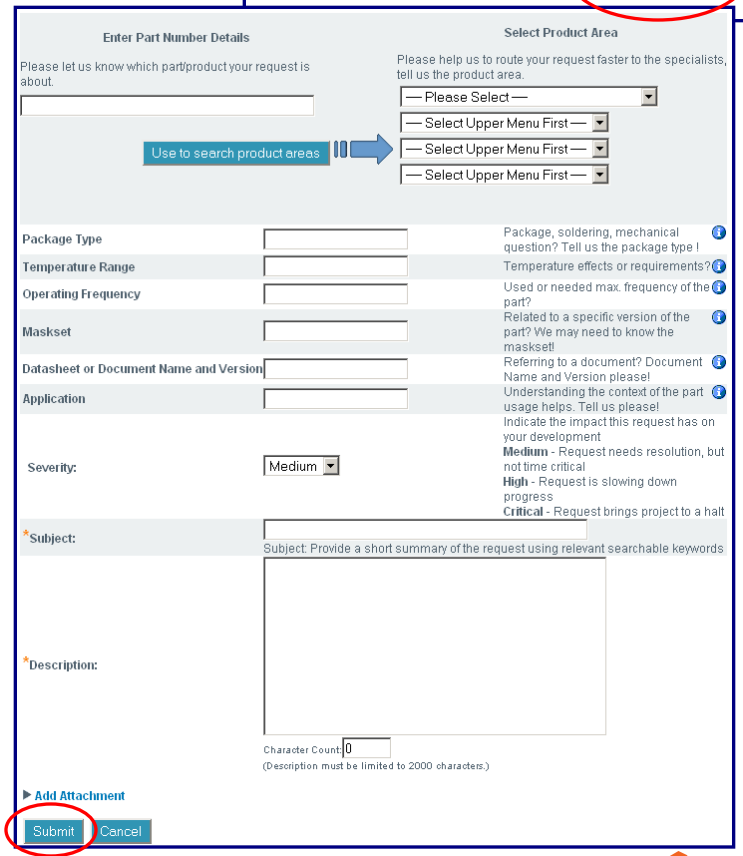

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