Partner-ETII

ROM In-Circuit Debugger

Freescale Semiconductor
Author, Jim Trudeau

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OVERVIEW

PARTNER-ETII combines the best features of in-circuit emulators, ROM emulators and debugging monitors to provide leading-edge debugging capabilities and power.

Freescale Semiconductor, Inc. and Kyoto Microcomputer KK

The PARTNER-ETII In-Circuit Debugger is a state-of-the-art, third generation tool that provides an efficient and easy-to-use development environment for embedded systems developers. PARTNER-ETII includes the integrated PARTNER software debugger that combines high speed with advanced debugging features for target RISC architectures.

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1. Main Functions and Technical Overview of PARTNER-ETII

Changes in embedded hardware designs and the limited capabilities of debugging tools make debugging tasks more difficult today. Surface-mounted packages make it difficult to attach an in-circuit emulator. ROM emulators suffer from high cost and a limited feature set. Debugging monitors have slow response times.

The PARTNER-ETII provides a new solution that combines the best and most appropriate features from the in-circuit emulator, debugging monitor, and in-circuit ROM emulator solutions. These features are integrated with software technology developed in the PARTNER source level debugger.

The design of the PARTNER-ETII hardware is based on concepts found in traditional ROM emulator solutions. However, the PARTNER-ETII does much more than simply rewrite ROM contents with a ROM writer using serial communications from the host.

The PARTNER-ETII system is a separate unit that contains its own RAM, which is used to emulate the target system's ROM. In addition, one section of the ROM emulator is reserved for a debug monitor that communicates with the target hardware. The monitor, via a special ROM socket connection, intercepts signals from the target system and uses these to operate the program and control the test system.

Downloads and debug communications occur over a high-speed link to the emulator, not to the test system. The PARTNER-ETII uses a special-purpose parallel interface to the host computer for ultra high-speed communications with a maximum throughput of 4 Mbytes/second.

As a result, PARTNER-ETII can easily execute time-consuming commands such as loading, saving large executable files, stepping through code, as well as displaying and editing the contents of RAM and I/O data. Moreover, PARTNER-ETII models 20, 30 and 31 all provide hardware breakpoint and real-time trace functions equivalent to those provided by in-circuit emulators.

This design provides high-level functionality equivalent to that of in-circuit emulators, yet at the same time also provides an easy-to-use and convenient interface. Figure 1 illustrates the PARTNER-ETII system and its connections to both the host computer and target hardware. The PARTNER-ETII system connects to the target system with a ROM connector to the target ROM socket and with a few probes to key target control signals.

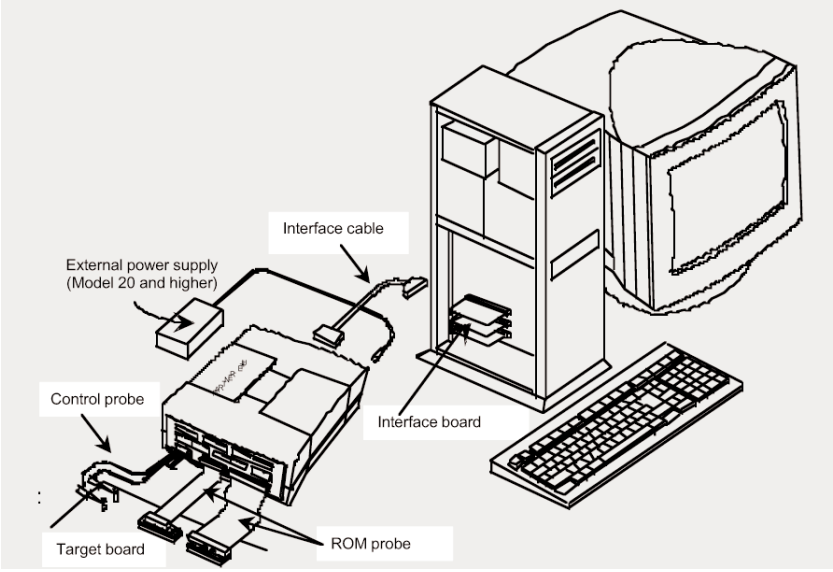

FIGURE 1: THE PARTNER-ETII HARDWARE AND CONNECTIONS

The PARTNER-ETII supports not only standard CPU targets that the software debugger supports, but also its core ASIC microprocessor. This flexibility allows you to support changes in your development targets and CPU.

The user interface for the PARTNER-ETII control software and the PARTNER software debugger remains the same as that of the PARTNER-ET. Previous users will have no difficulty upgrading to the PARTNER-ETII solution.

PARTNER-ETII models 30/31 also support JTAG/N-wire debug services such as those present in the latest RISC microprocessors. This feature provides developers with a powerful debug solution that can be easily connected and configured through a standardized debug port.

2. Features Upgraded From PARTNER-ET

- **Improved speed**-50ns access times
- **Large capacity**-up to 4 Mbytes emulation-ROM
- **High transmission speed**-file loading and quick command response times with a maximum transmission speed of 4 Mbytes/sec (PCI I/F)
- **Power supply flexibility**-support for 3V, 3.3V and normal 5V ROM without adapter converter
- **Support for JTAG/N-wire debugging** (models 30/31)
- **Increased number of debug functions**-including significant improvements in hardware breakpoint and real-time trace functions

Please note that there is no hardware or software compatibility (such as control software, ROM prob and interface board) between PARTNER-ETII and PARTNER-ET.

3. PARTNER-ETII Features

- **Multi-target, multi-purpose debugger solution**
  The PARTNER-ETII is CPU-independent, so there is no need to change PARTNER hardware if you change processors. The PARTNER-ETII is fully configurable via software, so users need only upgrade the debugger software. Moreover, the in-circuit ROM emulation method easily supports flat package CPUs. This is an all-purpose debugging tool that traditional in-circuit CPU emulation methods could not achieve.
- **Support for 8-, 16-, 32- and 64-bit (planned) CPUs with one hardware design**
  32 bit and 64 bit CPUs are supported by models 30/31 only. A 32-bit ROM bus width is supported now.
- **Support for higher speed, larger capacity ROM**
  All models support the high access speed of 50ns for ROM addresses. Maximum ROM capacity for the various models is listed in the table below.

MODEL	WITH 8-BIT BUS ROM	WITH 16-BIT BUS ROM
Model 10	2Mbit x 2	4Mbit x 1
Model 20	4Mbit x 2	8Mbit x 1
Model 30	4Mbit x 4	8Mbit x 2
Model 31	8Mbit x 4	16Mbit x 2

- **Support for low-voltage ROM**
  PARTNER-ETII supports all three major ROM power supply voltages: 3V, 3.3V and 5V. There is no need for power adapter converters, unlike earlier models.
- **Improved hardware break with multiple event conditions (models 20/30/31 only)**
  The PARTNER-ETII provides hardware breakpoint and real-time trace functions equivalent to those provided by in-circuit emulators. By using hardware breakpoints, the PARTNER-ETII can provide data-access breakpoints. This could not be implemented in earlier debugging monitor systems.

  Event conditions are defined by three items: data address, external trace signal and pass count. It is also possible to set an address range. The PARTNER-ETII supports AND and SEQ events, which combine timeout events and external input events.

- **Real-time trace (models 20/30/31 only)**
  The PARTNER-ETII can trace and display data from addresses supplied for the ROM probe, data bus and external trace signal for up to 64K frames.
  - The real-time trace feature provides three sample modes: full trace mode, sample trace mode and triggered trace mode.
  - An event condition (identical to those used for hardware breakpoints) can be used as a trigger.
  - A time stamp feature is also provided. Trace result displays C source as well.

MODEL	FRAME	ADDRESS	DATA	EXTERNAL TRACE	TIME STAMP
Model 20	64 bit x 64K	24 bit	16 bit	8 bit	11 bit
Model 30	96 bit x 64K	32 bit	32 bit	16 bit	11 bit
Model 31	96 bit x 64K	32 bit	32 bit	16 bit	11 bit

- **Real-time counting**
  The PARTNER-ETII provides functionality for measuring user program execution time (the time from the point a user program was executed until it stops) in 1µs units for periods up to 4294 seconds (all models).

  This feature can also measure the execution time between two points specified as event conditions. Maximum value, minimum value and average value are displayed in real time. Furthermore, execution time between two events exceeding a specified time can be used as a trigger (models 20/30/31 only).

- **On-the-fly features**
  The PARTNER-ETII supports inspection and modification of memory and registers while the user program is executing. However, these on-the-fly features temporarily stop user program execution. As a result, real-time performance is lost when they are used. Starting and stopping, inspecting and changing data, taking data into trace memory, conditions for taking-in and inspecting trace memory are features that can be freely used while the program is executing.

- **Forcible break**
  The PARTNER-ETII allows the user to force a break in the user program during execution.

4. PARTNER Software Debugging Environment

The PARTNER-ETII system comes with the Windows95/98/NT version of the PARTNER debugger software. The debugger software for PARTNER-ETII is compatible with earlier versions of the Windows PARTNER debugger software for the PARTNER-ET. The PARTNER debugger user-interface is common across all models of the PARTNER-ETII for all target microprocessors.

The PARTNER debugger software has many outstanding features:

- **High-speed processing in an easy-to-use operating environment**
  PARTNER-ETII allows time-consuming commands to execute at blazing-fast speed by providing a high-speed parallel interface (maximum 4 Mbytes/sec) and highly optimized software tools for fast response time in a debugging environment.

- **Source level debugging**
  Programs written in C can be debugged at the source level. Stepping through code by source line is supported and breakpoints can be set.

- **Data inspection**
  All C data types are supported, including char, int, pointers, structures, unions and arrays, as well as the evaluation of C expressions.

- **Data watching**
  This function displays data (such as variables, arrays and updated expression evaluations) in Watch windows.

- **Shell features**
  PARTNER-ETII has added functions to improve shell operation, such as a history buffer that remembers 1500 characters, line edit features, command search and symbol search. This makes command-line window input easier.

- **Macro features**
  PARTNER-ETII provides powerful macro features with a multi-purpose scripting/programming language that supports control structures (including if, for, while, do and break). The macro features can be used to define new commands that are a combination of other commands. Debugging operations can be performed efficiently by using macros in combination with the breakpoint functions. These features can be readily used for automated testing and production purposes.
- **Profiling**
  PARTNER-ETII can collect and display statistics on how much time was spent in each subroutine during program execution.
- **System call**
  PARTNER-ETII provides system calls that a program can use to output text to the screen and to read characters from a PC keyboard. The executing program can use these system calls to display the state of the program.
- **On-line help**
  On-line help is provided for the user.
- **Support for extended memory for V86 control software (debugger software)**
  A multi-module debugger is available that can load multiple debug information files. It supports 16 Mbytes of physical address space. PARTNER-ETII supports configurable MMU and banked memory spaces as well.
- **Support for bank mode in 80 control software (debugger software)**
  PARTNER-ETII supports the banked memory mode adopted for 68180 series and KC80 series. Supported languages are LSI-C80 Ver3.4, Ver3.5 and PROASM-IIVer3.0.

5. Features of PARTNER-ETII/Win for Windows95/98/NT

The Windows version of the control software provides users with a user-friendly, easy-to-operate, advanced GUI environment.

- **Basic compatibility between PARTNER-ET and PARTNER-ETII**
  Keyboard operation for the code and command windows (including function keys) is the same.
- **Simple configuration**
  A simple setup application displays a toolbar that guides you through the configuration process. Configuration (CFG) file editing, monitor file editing and building, and changes in operating options are sequentially set up. PARTNER-ETII also allows you to save your setup. You can then launch a debug session by double-clicking the icon for that setup.
- **Powerful data inspection, modification, and link features**
  PARTNER-ETII has significantly improved upon the highly reputed PARTNER's data inspection and modification features. Simply double-clicking a variable displayed in a source window opens the inspector window. This allows you to refer to and change the value of the variable. You can also inspect or change a variable in the Watch window or Local window. Furthermore, modifying data has also become much easier in the Register and Memory windows.
- **Easy-to-use, customizable windowing environment**
  Setting colors for the font and window background is simple. In addition, the tool bar enables you to display or hide any window with ease. The size and position of each window can be set at will, and its status memorized when the debugger is finished. You can also preserve and restore three different window layouts.

Figure 2 illustrates some of the debugger windows, followed by a table listing the available windows and what each window displays.

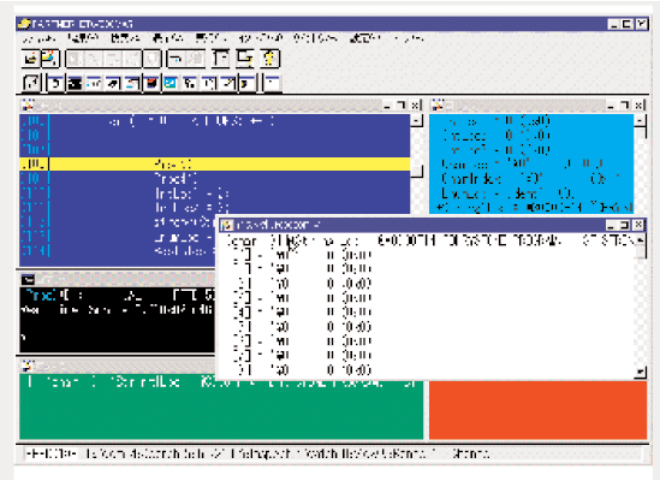

FIGURE 2: SAMPLE PARTNER ETII WINDOWS

PARTNER-ETII/WIN DEBUGGER USER INTERFACE

WINDOW	DISPLAY
Main Window	Main window for PARTNER-ET/Win
Code	Source code (two sources can be displayed)
Command	Command input
Memory	Memory dump
Register	Register data
Stack	Stack chain
Local	Local variables of current function
Watch	Specified updated address and variables
Back Trace	Which function is calling the current function
Break	Break set status
Memo	Inspecting and changing variable data
Inspect	Inspecting and changing function data
History	Real-time trace memory

- **Easy input for complicated commands**
  Dialog windows help you easily configure complex commands such as hardware break and real-time trace.
- **Suitability for notebook PCs**
  PARTNER-ETII's ability to customize the arrangement of the tool bar, status bar, and windows makes it useful even on screens with 640 x 480 resolution, such as those used on some notebook PCs.

6. Support for JTAG/N-Wire in PARTNER-ETII

JTAG/N-wire is a high-speed debugging protocol available in the latest RISC and system-on-silicon solutions. By connecting PARTNER-ETII to a JTAG/N-wire debug port, PARTNER-ETII provides debug functionality using CPU-specific debug resources.

When using a JTAG/N-wire connection, there is no need to connect control probes from the PARTNER-ETII to the target hardware. The only required connection is the JTAG probe (to a JTAG connector on the target board) and a ROM probe.

PARTNER-ETII has a high-speed operating performance that is far advanced from old JTAG tools. By receiving information directly from the CPU that is operating on a target board, PARTNER-ETII breaks traditional barriers of in-circuit ROM debuggers.

FEATURE	WITH JTAG/N-WIRE	PARTNER-ETII STANDARD
Easy connection	JTAG Probe and ROM Probes (Control probe can be omitted)	Requires ROM Probe, Address/Control Probe
Easy configuration	No configuration required	Requires configurations for each specific board
Trace on cache	Supported completely*	Not supported
Use for hardware debug	Possible	CPU, ROM and RAM must be operational at least

*Provides real-time trace in cache area and DRAM area with full spec operation

> Product upgrades for JTAG/N-wire
Users of PARTNER-ETII models 30/31 can support JTAG/N-wire with an optional upgrade kit. This kit includes special-purpose probes and control software.

JTAG/N-WIRE CPU PLANS. FOR PRICING INFORMATION, CONTACT SALES.

CPU*	SCHEDULE
V831	Available
	(V832 is under development)
SH4	Under development
SH3-DSP	Under development

*Support is planned for other CPUs

> **Additional note**
When designing a target board, users need to include a JTAG port (debug port) as suggested by the CPU manufacturer. For more information, please contact us.

7. PARTNER-ETII Supported Compilers

PROCESSOR	COMPILER
Zilog Z80	LSI-C80 Ver 3.3, 3.4, 3.5
	KMC PROASM-II Assembler Ver 3.0
Hitachi H8	Hitachi C Compiler* Ver 2.0, 3.0
Intel X86	MS-C* Ver 4.0, 5.1, 6.0, 7.0 Turbo-C++* Ver 1.0
	Borland C++* Ver 3.1, 5.x
	Turbo-C Ver 1.5, 2.0 MASM Assembler Ver 5.1, 6.0
	LSI-C86 Ver 3.1, 3.3, 3.5 TASM Assembler Ver1.0, 2.0 CodeWarrior® x86 Embedded Systems (under development)
Toshiba T900	Toshiba C Compiler Ver 4.x
Motorola 68K, CPU32	KMC exeGCC Ver 1.0
	MCC68K Ver 3.3, 4.4, 4.5G, 4.5R
	CodeWarrior 68K Embedded Systems (under development)
ARM	ARM-C Tool Kit Ver 2.00, 2.10
NEC V800	CodeWarrior V800 Embedded Systems KMC exeGCC V800 Ver 1.0
	NEC C Compiler (CA732) Ver 1.00J Green Hills C V800 Ver 1.8.8
NEC V850E	NEC C Compiler Green Hills C V800
	CodeWarrior V800 Embedded Systems (under development) KMC exeGCC V850E (under development)
Hitachi SuperH	KMC exeGCC SH Ver 1.0 Hitachi C Compiler Ver 3.0A, 3.0B, 4.1A, 4.1B Green Hills C SH Ver 1.8.8
	CodeWarrior SH Embedded Systems (under development)
MIPS, NEC VR	CodeWarrior MIPS Embedded Systems CodeWarrior VR Embedded Systems KMC exeGCC MIPS Ver 1.0
	Green Hills C MIPS 1.8.7
Mitsubishi M32R	KMC exeGCC M32R Ver 1.0
	Mitsubishi C Compiler
Matsushita MN103	Matsushita C Compiler

* C++ is not supported

8. PARTNER-ETII Supported CPUs

MODEL	PROCESSORS
PARTNER-ETII (Z80)	Z80, 64180, TMPZ84, KC80
PARTNER-ETII (H8)	H8/300, H8S(support advanced mode only, except 21xx)
PARTNER-ETII (X86)	8086, 8088, 80186, 80188, 80286
	V20/30, V40/50, V25/35, V25+/35+, V33/V53, V55PI, V30MX
PARTNER-ETII (68K)	68000, 68010, 68301, 68303
PARTNER-ETII (68K32)	68020, 68030, 68040, CPU32(68331, 68332, etc)
PARTNER-ETII (T900)	TLCS900/H, TLCS900/L, TLCS900, TLCS900/H2
PARTNER-ETII (ARM)	ARM60, 600, 610, 7 series, THUMB
PARTNER-ETII (V800)	V805, 810, 820, 821, 830, 831
PARTNER-ETII (V850E)	V850E
PARTNER-ETII (SH)	SH1, SH2, SH3
	SH4, SH3/DSP (under development)
PARTNER-ETII (MIPS)	R3900, R4650
	VR3800, VR4000, VR4100, VR4200, VR4300, VR4400, VR5000
PARTNER-ETII (M32R)	M32R/D
PARTNER-ETII (MN103)	MN103002

9. PARTNER-ETII Technical Specifications

> **Host environment**
OS: Windows95/98/NT
CPU: 80386 or higher

> **Host interface**
High-speed PC interfaces are available.

TYPE	PROTOCOL	BANDWIDTH
PCI	PCI bus	4Mbytes/sec
ISA	ISA bus	2Mbytes/sec
PC card	TYPE II PCMCIA2.1/JEIDA4.2*	

*Windows NT is supported - “Resource 0220H is occupied” issue must be resolved

> **Power supply**
Model 10 can use power from the PC. Use the optional power adapter if the PC power supply does not have adequate capacity, or with a notebook PC. Models 20 and higher come with a power adapter as standard equipment.

HARDWARE	CURRENT USED
Interface card	200mA
PARTNER-ETII Model 10 main unit	600mA

> **Outside dimensions and weight**
External dimensions of the main unit (inches): 6.1(W) x 7.1(D) x 2.6(H) Weight: about 18oz.

> **Operating environment**
Ambient temperature: 5-35 degrees Celsius (41-95 degrees Fahrenheit)
Relative humidity: 35-85 percent (non-condensing)

> **Supported ROM types**
The supported ROMs listed in the table below are all DIP ROMs. A conversion socket is required for systems that use PLCC package ROMs.

TYPE	RANGE	MAXIMUM PER MODEL
28 pin ROM	64-512Kbit	
32 pin ROM	1Mbit-8Mbit	2Mbit with Model 10 4Mbit with Model 20/30 8Mbit with Model 31
40 pin ROM	1Mbit-8Mbit	4Mbit with Model 10 8Mbit with Model 20/30/31
42 pin ROM	1Mbit-16Mbit	4Mbit with Model 10 16Mbit with Model 31

> **ROM capacity and other supported features**

> **ROM access speed**

PARTNER-ETII MODEL	CPU RANGE	MAXIMUM ROM CAPACITY (8BIT/16BIT BUS)	HARDWARE BREAK REAL-TIME TRACE	JTAG
Model 10	8/16 bit	2Mbit x 2 4Mbit x 1	Not supported	Not supported
Model 20	8/16 bit	4Mbit x 2 8Mbit x 1	Supported	Not supported
Model 30	8/16/32 bit	4Mbit x 4 8Mbit x 2	Supported	Optional
Model 31	8/16/32 bit	8Mbit x 4 16Mbit x 2	Supported	Optional

50ns from address 30ns from OE

10. Requirements for the Target System

Because PARTNER-ETII systems do not contain a CPU, a target board and a ROM socket are required. There must be at least one ROM socket for an 8-bit bus system, two for a 16-bit bus system (one or more for 16-bit bus width ROM) and four for a 32-bit bus system (two or more for 16-bit width ROM).

The monitor uses 128 to 512 bytes in ROM (it varies by CPU), and requires 16 to 128 bytes of RAM for stack space.

CPU TYPE	MONITOR USE OF ROM	STACK USE
8bit CPU	128bytes	About 16bytes
16bit CPU	256bytes	About 16bytes
32bit CPU	512bytes	About 32bytes

The target CPU must be provided with an NMI (level 7 for the 68 family) for the debugger. The target CPU must be provided with a reset signal. The CPU, ROM and RAM in the target board must be fully operational. For PARTNER-ETII to execute hardware and software breaks, some processor interrupts are occupied or limited (see the table below).

CPU	HARDWARE BREAK USES	SOFTWARE BREAK USES
Z80, TMPZ84 64180, KC80	NMI (Address 0x66)	One of RST8 to RST38
H8	NMI (Address 0x10)	One of TRAPA0-3
X86	NMI (INT2)	INT1, INT3
68K	One of Vector 24-31 (IPL7 is desirable)	Vector 0, 2, 3, 4
TLCS900	NMI	One Software Break instruction (SWI)
ARM	FIQ interrupt (0x1C-0x1F)	UNDEF (0x04-0x07)
V800	NMI	TRAP0 or TRAP10
SH	NMI (Address 0x2C)	Generic Unjust instruction
MIPS	NMI or External exception	BREAK
M32R	SBI (0x010)	One TRAP interrupt (0x040-0x07C)
MN103	NMI	Occupy Interrupt vector on PI instruction

For MIPS processors, 64-bit ROM access and address spaces greater than 32-bit are not supported at this time.

How to Reach Us:

Home Page:
www.freescale.com

e-mail:
support@freescale.com

USA/Europe or Locations Not Listed:
Freescale Semiconductor

Technical Information Center, CH370

1300 N. Alma School Road

Chandler, Arizona 85224

1-800-521-6274

480-768-2130

support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH

Technical Information Center

Schatzbogen 7

81829 Muenchen, Germany

+44 1296 380 456 (English)

+46 8 52200080 (English)

+49 89 92103 559 (German)

+33 1 69 35 48 48 (French)

support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.

Headquarters

ARCO Tower 15F

1-8-1, Shimo-Meguro, Meguro-ku,

Tokyo 153-0064, Japan

0120 191014

+81 3 5437 9125

support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.

Technical Information Center

2 Dai King Street

Tai Po Industrial Estate,

Tai Po, N.T., Hong Kong

+800 2666 8080

support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor

Literature Distribution Center

P.O. Box 5405

Denver, Colorado 80217

1-800-441-2447

303-675-2140

Fax: 303-675-2150

LDCForFreescaleSemiconductor

@hibbertgroup.com

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