SparX-5/5i

Hardware Design Checklist

1.0 INTRODUCTION

This document provides a hardware design checklist for the Microchip VSC7546, VSC7549, VSC7552, VSC7556, VSC7558, VSC7546TSN, VSC7549TSN, VSC7552TSN, VSC7556TSN, and VSC7558TSN. The checklist should be followed when utilizing the VSC part in a new design. A summary of these items is provided in Section 18.0, "Hardware Checklist Summary," on page 33. Detailed information on each subject can be found in the corresponding section:

- Section 2.0, "General Considerations"
- Section 3.0, "Power Supplies and Grounding"
- Section 4.0, "Reference Clocks"
- Section 5.0, "CPU System"
- Section 6.0, "Port Configuration"
- Section 7.0, "Serial GPIO Controller (SGPIO)"
- Section 8.0, "SGMII/XFI PHY Interface"
- Section 9.0, "Serial CPU Interface"
- Section 10.0, "UART Controllers"
- Section 11.0, "Parallel Interface Controller"
- Section 12.0, "DDR3/3L/4 Memory Controller – SDRAM Interface"
- Section 13.0, "JTAG Interface"
- Section 14.0, "System Reset"
- Section 15.0, "Temperature Sensor"
- Section 16.0, "Miscellaneous"
- Section 17.0, "GPIO Usage"

2.0 GENERAL CONSIDERATIONS

2.1 Required References

The implementer should have latest version of the following documents on hand:

- SparX-5/SparX-5i data sheets and errata found on the product page of the VSC device:
  - VSC7546: www.microchip.com/VSC7546
  - VSC7549: www.microchip.com/VSC7549
  - VSC7552: www.microchip.com/VSC7552
  - VSC7556: www.microchip.com/VSC7556
  - VSC7558: www.microchip.com/VSC7558
  - VSC7546TSN: www.microchip.com/VSC7546TSN
  - VSC7549TSN: www.microchip.com/VSC7549TSN
  - VSC7552TSN: www.microchip.com/VSC7552TSN
  - VSC7556TSN: www.microchip.com/VSC7556TSN
  - VSC7558TSN: www.microchip.com/VSC7558TSN
- Schematic
  - PCB134 FireAnt 20xSFP Refboard
  - PCB135 FireAnt 48xCu Refboard

- Layout file
  - PCB134 - with DDR4
  - PCB135 - with DDR3
- User Guide
  - *UG1071-RBM-VSC5640EV FireAnt 20xSFP Hardware Manual (PCB134)*
  - *UG1072-RBM-VSC5641EV FireAnt 48xCu Hardware Manual (PCB135)*

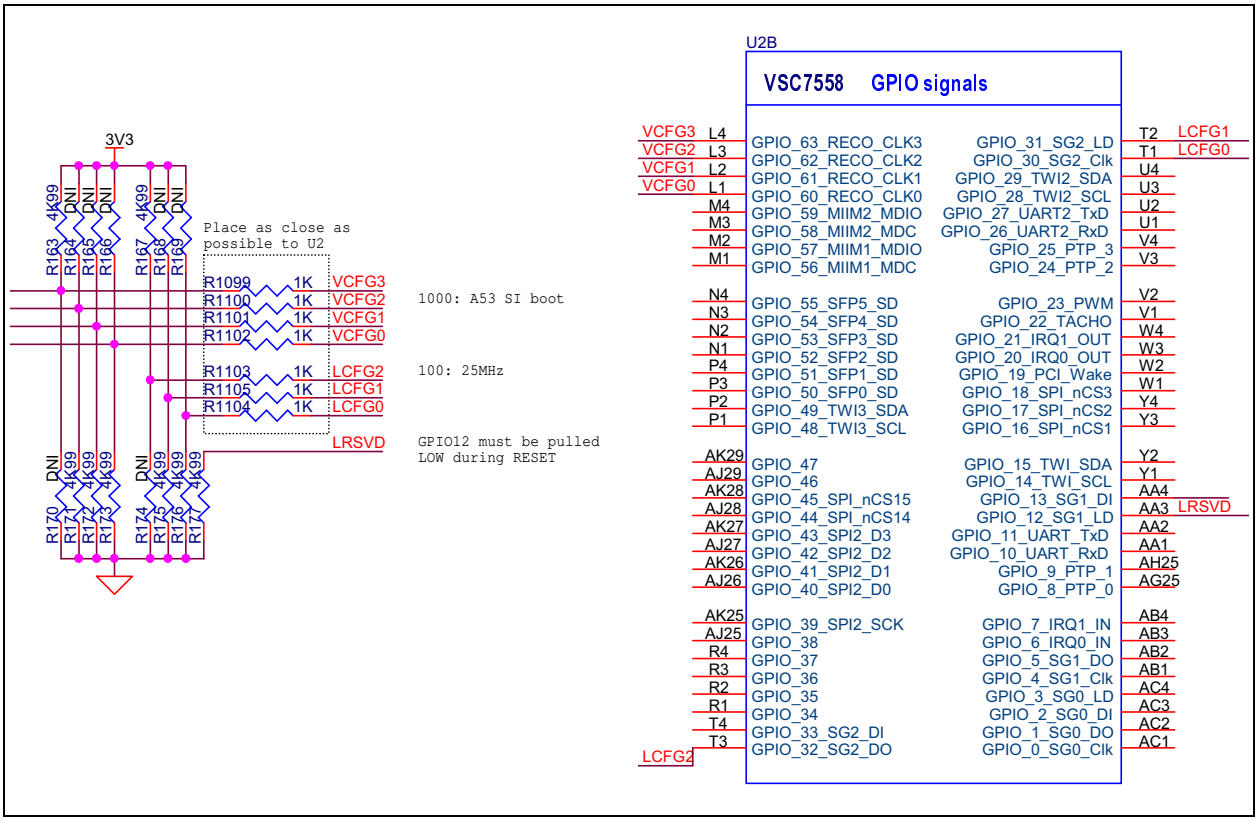
2.2 Pin Check

- Check the pinout of the part against the data sheet. Ensure that all pins match the data sheet and are configured as intended input, output, or bidirectional.
- It is highly recommended to follow one of the reference design schematics as a basis and retain the reference design's use of GPIO (parallel as well as serial) whenever possible to minimize software changes. Keep a log of major changes (for example, port numbering, PHY addresses, GPIO, and SGPIO), and provide this log when there is design review or when starting software customization. The device-tree provided with the VSC Switch Application is specifically made to be used together with the reference board use of the different features located at the GPIOs.

2.3 Strapping Pins

- Some of the GPIO pins are used as strapping pins at power-up for configuring the LC PLL0 reference clock frequency and for selecting CPU start-up modes. See Figure 2-1 and Table 2-1 for the description of the strapping pins and the corresponding configurations and modes. 1K-4.7K resistors are recommended for pulling the strapping high or low accordingly.

FIGURE 2-1: PIN STRAPPING OVERLAID WITH GPIO PINS



Note: All GPIO pins have an internal pull-up.

TABLE 2-1: PIN STRAPPING DESCRIPTIONS

Pin	Description
LCPLL_CONF[2:0]/LCFG[2:0] (Pin T[3:1] – GPIO_[32:30])	Configuration of VCORE reference clock frequency for LC-PLL 000: 125 MHz 001: 156.25 MHz 010: 250 MHz 011: 312.5 MHz 100: 25 MHz Other values are reserved and must not be used.
LCPLL_RSVD/LRSVD (Pin AA3 – GPIO_12)	*Should be held low during reset.*
VCORE_CFG[3:0]/VCFG[3:0] (Pin L[4:1] – GPIO_[63:60])	1000: ARM A53 core 0 boots from SI interface. 1101: No boot. SI client and PI client enabled. 1110: No boot. SI client and MIIM client enabled with MIIM address 0. 1111: No boot. SI client is enabled.

Note: Only the Switch core REFCLK0 is selectable. The two SerDes reference clocks, REFCLK1 and REFCLK2, are fixed at 156.25 MHz.

3.0 POWER SUPPLIES AND GROUNDING

3.1 Power Supplies

- The chip has a number of power domains that are compliant to different I/O standards.

FIGURE 3-1: POWER SUPPLY PINS

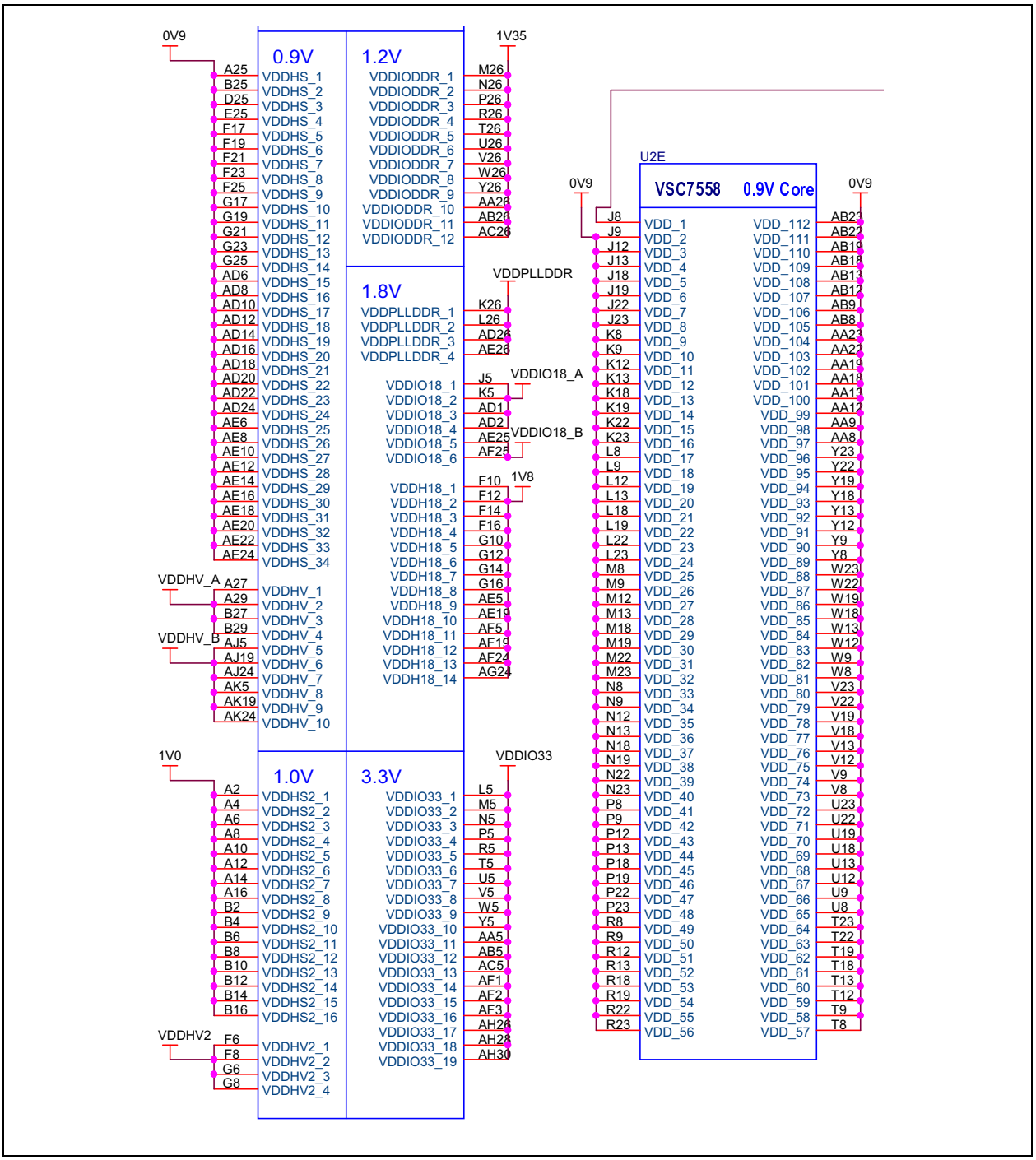


TABLE 3-1: POWER SUPPLY DESCRIPTIONS

Pin	Voltage	Description
VDD_[112:1]	0.9V	Core supply
VDDHS_[34:1]	0.9V	SERDES10G (S13-S24) and SERDES6G (S0-S12) *digital* supply
VDDHV_[10:1]	0.9V	SERDES10G (S13-S24) and SERDES6G (S0-S12) *analog* supply
VDDHS2_[16:1]	1.0V	SERDES25G (S25-S32) *digital* supply
VDDHV2_[4:1]	1.0V	SERDES25G (S25-S32) *analog* supply
VDDIODDR_[12:1]	1.2V, 1.35V, or 1.5V	DDR3/DDR4 interface The VDD_IODDR supply can remain at ground or left floating if not used. See Note 1.
VDDPLLDDR_[4:1]	1.8V	DDR3/DDR4 PLL supply
VDDH18_[14:1]	1.8V	SerDes analog circuits
VDDIO18_[6:1]	1.8V	I/O circuits
VDDIO33_[19:1]	3.3V	GPIO and miscellaneous I/O
VSS_[328:1]	NA	Ground reference

Note 1: If VDD_IODDR is grounded, DDR_Vref must also be grounded.

- Each power supply voltage should have both bulk and high-frequency decoupling capacitors. The recommended bulk capacitors are 10 µF. For DDR, a mix of 0.1 µF and minimum 1-2.2 µF should be used. Surface mount decoupling capacitors should be placed as close to the Switch power supply pins as possible.
- Analog supplies must be isolated from the remaining board supplies using ferrite beads.

3.2 Power Supply Sequencing

- The **nRESET** and **JTAG_nTRST** input pins must be held low until all power supply voltages have reached their recommended operating condition values.
- The overall strategy is to prevent higher powered supplies feeding lower level powered grids through the internal protection diode network. The general power sequence is thus:

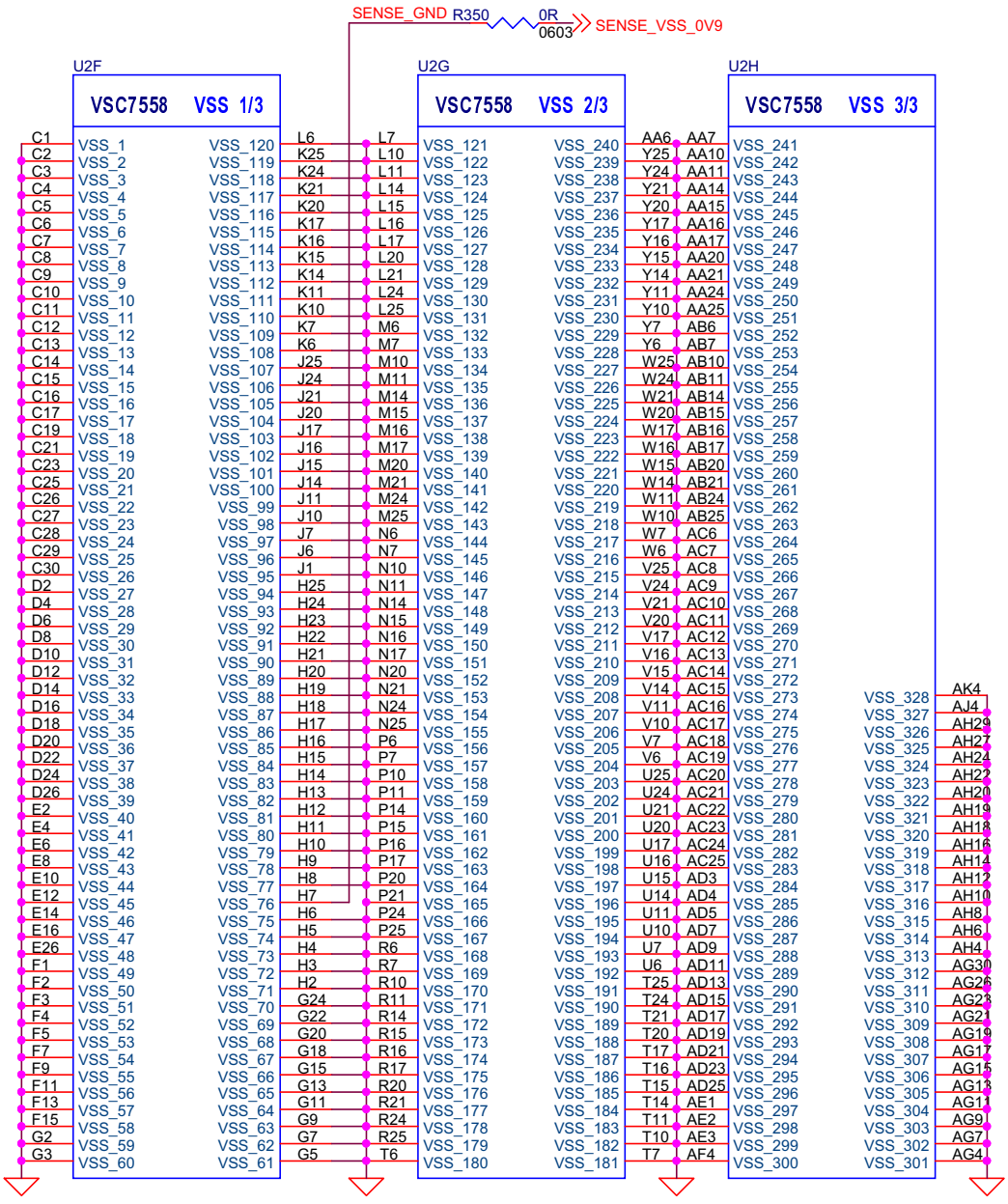
  0.9V → 1.0V → 1.2V → 1.8V → 3.3V

- Constraints:
  - During power-on and power-off, **VDDHS**, **VDDHS2**, **VDDHV**, and **VDDHV2** must never be more than 300 mV above VDD.
  - The maximum rising slope of **VDDHS**, **VDDHS2**, **VDDHV**, **VDDHV2**, and **VDDH18** during power-on must be below 5 V/ms (or greater than 200 µs) *to limit inrush current*.
  - The SerDes macro supplies (that is, **VDDHS**, **VDDHS2**, **VDDHV**, and **VDDHV2**) must be powered, even if the associated interface is not used. These power supplies must not remain grounded or left floating.
  - **VDD**, **VDDIODDR**, and **VDDPLLDDR** must power on simultaneously, or in the following sequence: **VDD > VDDIODDR > VDDPLLDDR**. There is no requirement from **VDD** to **VDDIODDR**, but a maximum delay of 100 ms from **VDDIODDR** to **VDD** is recommended.
  - During power-on and power-off, **VDDIO33** must never be more than 1.8V above **VDDIO18**.

3.3 Ground

- Create at least one unbroken ground plane (GND) layer in the stack-up.
- Normally, there should be a solid ground plane beneath each of the outer layers to ensure that the signals on these layers have a good reference plane.
- Shield ground on signal layers should serve as “quiet” ground for PHY copper media signals and SFP cages. It couples capacitively to the ground planes, providing a low-impedance return path for high-frequency noise.

FIGURE 3-2: GROUND PINS



4.0 REFERENCE CLOCKS

- The Switch has a number of reference clocks, which serve the different parts of the Switch.

FIGURE 4-1: REFERENCE CLOCKS

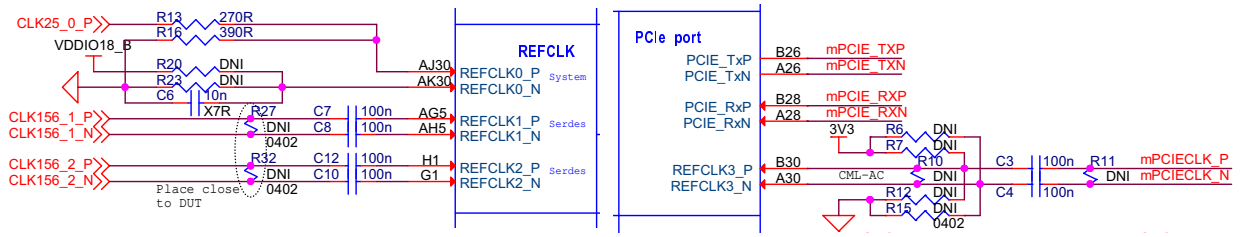


TABLE 4-1: REFERENCE CLOCK DESCRIPTION

Pin	In/Out	Description
REFCLK0_P/N (Pin AJ30/AK30)	In	This reference clock serves the System core clock. It can be 25 MHz, 125 MHz, 156.25 MHz, or 250 MHz, -100/+2000 ppm clock signal. The frequency is selected through LCPLL_CONF[2:0] as described in Table 2-1. PLL status can be found on GPIO 0 (or 62) in Alternate mode. See Note 1.
REFCLK1_P/N (Pin AG5/AH5)	In	Each reference clock serves the Ethernet SerDes macros placed at either North or South of the device. See Note 2. If the SerDes macros at either North or South is unused, the respective reference clock input can be floating or pulled to VDDIO18_A. The reference clock is fixed at 156.25 MHz ±100 ppm. A quality oscillator is then recommended. Check P/N must be AC-coupled.
REFCLK2_P/N (Pin H1/G1)		
REFCLK3_P/N (Pin AJ30/AK30)	In	PCIe® SerDes reference clock If unused, the clock input can be floating or pulled to VDDIO18. The reference clock is fixed at 100 MHz ±300 ppm. A quality oscillator is then recommended. Check P/N must be AC-coupled.

Note 1: GPIO 0 default is PLL status until the Switch is being set up.

2: REFCLK1 covers South-side SerDes macros S[0-16]. REFCLK2 covers North-side SerDes macros S[17-32].

Note: The data sheet requirements for maximum clock jitter must be accounted for in the board design when selecting clock source (oscillator) and clock distribution (buffer) components.

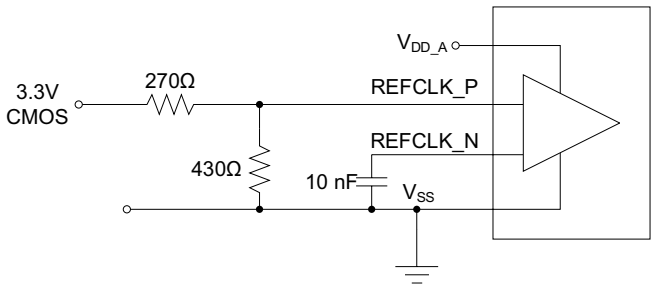
4.1 Differential Clock Input

- All four reference clocks are CML type and are best compatible with a Low Voltage Differential Signaling (LVDS). Each P/N pin of the clock input has an internal 50R termination to the common-mode voltage input, which results in a 100Ω differential termination from P to N.
- The System core reference clock, REFCLK0, common-mode input voltage is 0.7V, inherently biased to 0.39*VDDIO18. The data sheet prescribes an upper voltage limit on singled-ended input of 1800 mV (it must not exceed VDDIO18) and 1600 mV differential peak-to-peak.
- The SerDes reference clocks, REFCLK1-3, common-mode input voltage is 0.9V. The upper voltage limit on the single-ended input is 1100 mV and 1600 mV differential peak-to-peak.
- Some Low Voltage Positive Emitter-Couple Logic (LVPECL) might have a larger differential swing, so it should be attenuated using resistor dividers to meet the input specification for voltage swing. AC coupling is recommended to meet the reference clock input specification on common-mode input voltage using the internal termination as biasing.

4.2 Single-Ended Clock Input

- Although the SparX-5/5i reference clock input is differential, it is possible to use it with a single-ended clock source. This can be done by setting one differential input to the common-mode voltage and shaping the single-ended signal driving the other differential input, so that it toggles around this common-mode voltage with a voltage swing comparable to LVDS. The reference clock differential input buffer will see this as a valid differential signal.
- An external resistor network is required. The resistor network limits the amplitude and adjusts the center of the swing. Figure 4-2 shows the recommended circuit when using a 3.3V-powered single-ended oscillator as reference clock.

FIGURE 4-2: RESISTOR NETWORK FOR 3.3V CMOS SINGLE-ENDED CLOCK



- The differential input buffer has internal 100R termination. This is achieved by having one 50R from REFCLK_P to Vcm (0.39*VDD18 = 0.7V) and one 50R from REFCLK_N to Vcm. Setting the REFCLK_N input to the common-mode voltage is achieved with a decoupling capacitor to ground (this ensures a 0.7V level on the REFCLK_N input).
- Shaping the single-ended clock signal from an LVCMOS33 clock source to the levels required by the REFCLK_P input is achieved through a resistor divider.

Note: Because of the internal termination resistors in the reference clock input buffer, the 270R/430R external resistors proposed for dividing the clock signal do not decrease the voltage level on the REFCLK_P input to nominally 3.3V*430R/(270R + 430R) = 2.0V. Instead, the voltage level on the REFCLK_P input when voltage V is applied to the input of the resistor divider can be calculated as:

$$V_{ref} = (R_{bot}*R_{int}*V + R_{top}*R_{bot}*0.7V)/(R_{top}*R_{bot}+R_{bot}*R_{int}+R_{top}*R_{int})$$

- With R_{top} = 270R, R_{bot} = 430R, and R_{int} = 50R, then for V = 3.3V, the voltage level on the REFCLK_P input is calculated as 1.00V, and for V = 0V, the voltage level on the REFCLK_P input is calculated as 0.44V, so a swing of approximately ±250 mV is around the common-mode voltage of 0.7V.
- The voltage on any of the REFCLK0 pins should never exceed VDDIO18, as that would trigger the ESD protection diodes of input buffers.

Note: Differences in clock source output voltage levels, clock source output impedance, routing, and so on may induce changes to the external voltage divider. The value of the dividing resistors is not important per se, but the resulting signal as seen by the REFCLK_P input. The resulting signal should be toggling around the 0.7V with a 'swing' as high as possible. A swing of ±2-400 mV around the 0.7V common-mode voltage is safe in terms of ESD protection diode induced limits and is also high enough to offer reasonable noise margin.

- Rise time of the signal presented to the REFCLK_P input is important. A decrease in rise time will result in less jitter seen by the REFCLK_P input. Refer to the device data sheet for details and exact limits on rise time.

4.3 Recovered Output Clocks

The SparX-5/5i supports up to four recovered clock outputs coming from any of the SerDes interfaces. The recovered clocks, RECO_CLK[3:0], share the clock output pins overlaid on GPIOs and are shared with the VCORE_CFG strapping. For SyncE applications, the recovered clock output pins are typically connected to the inputs of an external digital phase locked loop (DPLL) for jitter cleanup. A DPLL output is then looped back to the SerDes reference clock inputs of the Switch. Make sure the DPLL outputs the correct clock frequency of 156.25 MHz to REFCLK1 and 2.

Note:	The VCORE_CFG strapping can also be controlled through a connector on the reference board. To eliminate stubs caused by the external VCORE_CFG strapping, a single buffer with three-state output is being used.

TABLE 4-2: RECOVERED CLOCK I/O

RECO_CLK	0	1	2	3
GPIO	60	61	62	63

4.4 PTP Engine - Input/Output Clocks

The SparX-5/5i offers input or output clocking for four of its five PTP engines, which are overlaid on GPIO pins. The PTP engines can be configured as 1PPS input or output, or they can be configured to output a programmable clock signal up to 125 MHz.

TABLE 4-3: PTP ENGINE I/O

PTP Engine	0	1	2	3
GPIO	8	9	24 or 54	25 or 55

The Switch has three Time-of-day (ToD) counters. UART2 is normally being used to send or receive ToD frames.

5.0 CPU SYSTEM

The Switch can be managed by either the internal VCORE CPU or an external CPU. The selection between internal or external CPU is made on the **VCORE_CFG[3:0]** strapping pins described in Section 2.3, "Strapping Pins".

The internal VCORE CPU system is based on a 1 GHz dual ARM A53 microprocessor. Core 0 can be enabled and boots from a Serial Peripheral Interface (SPI) NOR Flash when **VCORE_CFG[3:0]** strapping is configured to 1000. When **VCORE_CFG[3:0]** strapping is configured to 1101, 1110, or 1111, the internal CPU is disabled.

5.1 Internal CPU Auto Boot Mode

The Switch supports four SPI chip-select pins, but only **SI_nCS0** can be used for the internal CPU to boot from Flash. The Flash memory can be organized as 'NOR only', 'NOR/NAND', or 'NOR/eMMC'. In all cases, a NOR Flash is required because the Switch boot host starts from address 0. NAND/eMMC is organized as a file system. The boot loader (UBoot) stored in NOR knows how to address these. For 'NOR only' the minimum size of NOR Flash is 128 MB. For combination of Flash devices, the NOR Flash minimum size is 2 to 4 MB to store UBoot.

A Flash programming header can be used to support on-PCB Flash programming. It is important to have the Switch held in Reset during external Flash programming in order not to have both Switch and Programmer driving the SPI signals.

The **SI_nCS0** and **SI_CLK** signals have internal pull-up. The two signals will be high when the Switch is not driving them.

5.2 External CPU Mode

Some of the **VCORE_CFG** strapping options (see Table 2-1) disable the internal CPU and allow an external CPU to control the Switch through either the SPI client interface or the MIIM client interface. The MIIM client address is 0.

5.2.1 SPI CLIENT INTERFACE

The SPI client interface is enabled when **VCORE_CFG[3:0]** is 1101, 1110 or 1111. The SPI client interface shares the same pins as the SPI boot controller interface (see Table 9-1). Among the chip selection signals, only **SI_nCS0** supports Client mode.

When the external CPU uses the SPI client interface to read the Switch registers, the Switch must prepare read data after receiving the last address bit. The access time of the register that is read must be satisfied before shifting out the first bit of read data, so there must be a delay between the last address bit and the first data bit. The following are some ways to satisfy the needed delay:

- Use **SI_CLK** with a period of minimum twice the access time for the register target. For example, for normal switch core targets: 1/(2*1 µs) = 500 kHz (maximum).
- Pause the **SI_CLK** between shifting of serial address bit 0 and the first data bit with enough time to satisfy the access time for the register target.
- Configure the device to send out padding bytes before transmitting the read data to satisfy the access time for the register target. For example, 1 dummy byte allows enough read time for the SI clock to run up to 6 MHz in a single Host system. More dummy bytes can be used to increase speed and decrease the overall access time. Note that dummy bytes are not used on writes.

See Section 9.1, "SPI Boot and Primary QSPI Host Controller" for a description of the SPI client interface signals.

5.2.2 MIIM CLIENT INTERFACE

The MIIM client interface is enabled when **VCORE_CFG[3:0]** is 1110. The MIIM client pins on the device are overlaid functions on the GPIO interface (GPIO 52-54, respectively **MIIM_SLV_MDC**, **MIIM_SLV_MDIO**, and **MIIM_SLV_ADDR**). The MIIM client interface can be configured to answer on one of two different PHY addresses using the **MIIM_SLV_ADDR** pin. Setting the **MIIM_SLV_ADDR** pin to 0 configures the MIIM client to use PHY address 0, and setting it to 1 configures the MIIM client to use PHY address 31.

MIIM_SLV_MDIO is recommended to be pulled high through a 1.5 kΩ resistor.

5.2.3 PCIE® INTERFACE

The PCIe interface can also be used for an external CPU to read or write Switch registers. However, the PCIe interface can only be enabled by firmware or by using the SPI/MIIM client interface. AC coupling is recommended on the PCIe link between Switch and the external CPU.

The PCIe client interface supports a PCIe_wake signal on GPIO 19/55 as input interrupt instead of traditional beacon.

6.0 PORT CONFIGURATION

6.1 SerDes Interface

The Switch uses two different SerDes types: 25G (last 8) and 10G (all others). The data sheet operates with a third SerDes type, which is an additional 5G SerDes macro. This is only to reflect the maximum port speed of the possible devices that can be multiplexed to the SerDes macro.

REFCLK1 serves the lower 17 SerDes macros S[0-16], whereas REFCLK2 serves the upper 16 SerDes macros, S[17-32]. If one group is not populated (floating), then the corresponding REFCLK1/2 can be avoided from being populated.

All SparX-5/5i skews can use all SerDes macros, and all logical front ports or devices are available. It is only the maximum bridging bandwidth that is a limiting factor.

TABLE 6-1: SERDES MACROS

Macro Type	VSC7546	VSC7549	VSC7552	VSC7556	VSC7558
SerDes5G (NPI)/S0	1	1	1	1	1
SerDes5G/S1-S12	12	12	12	12	12
SerDes10G/S13-S24	12	12	12	12	12
SerDes25G/S25-S32	8	8	8	8	8

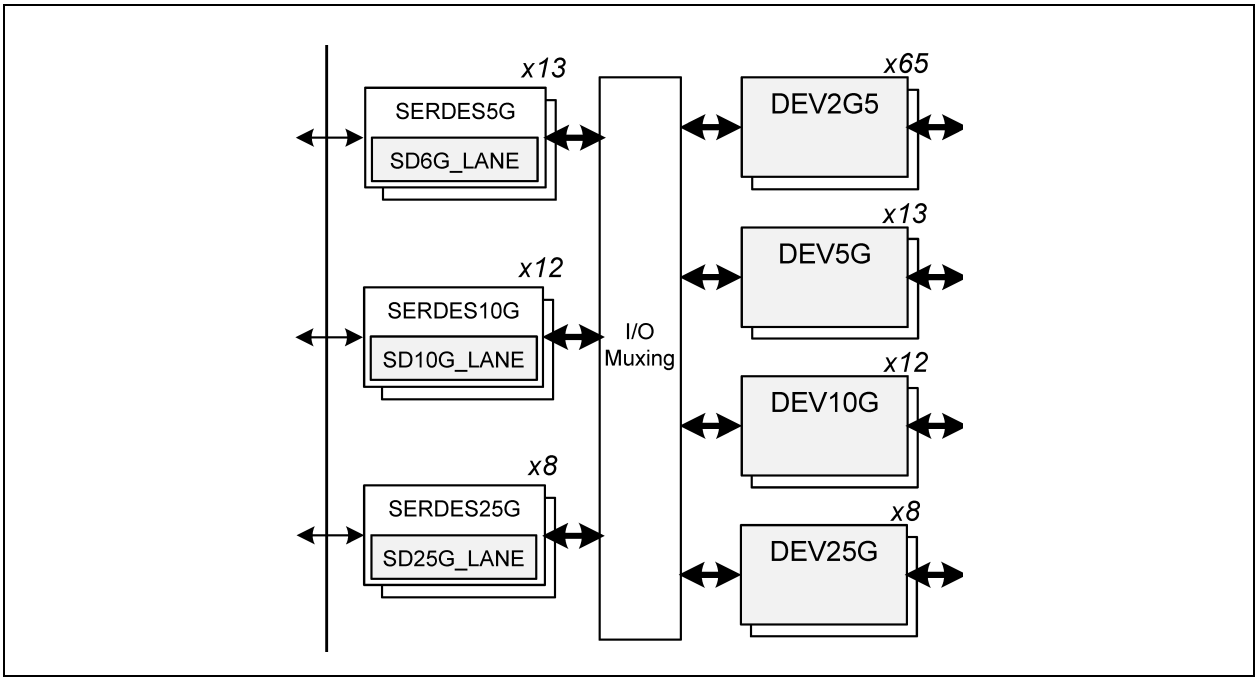
The SerDes macros have 100Ω internal termination and biasing. *Check the use of AC coupling for DC-level adjustment and EMI suppression.*

6.2 Port Mapping

Internally, the Switch can operate up to 65 logical front ports, called device D0-D64. A calendar is used for port scheduling and is controlling (and guaranteeing) the bandwidth given to each logical port.

Only, D64 is fixed allocated to SerDes5G_0 (S0). The remaining 64 ports can, with various I/O multiplexing, be connected to the remaining 32 SerDes, either by having a 1:1 mapping between the device and SerDes or by using QSGMII, USGMII, or USXGMII extenders to have multiple devices sharing a single SerDes.

FIGURE 6-1: PORT MAPPING



The 65 logical front ports are split up into the following blocks:

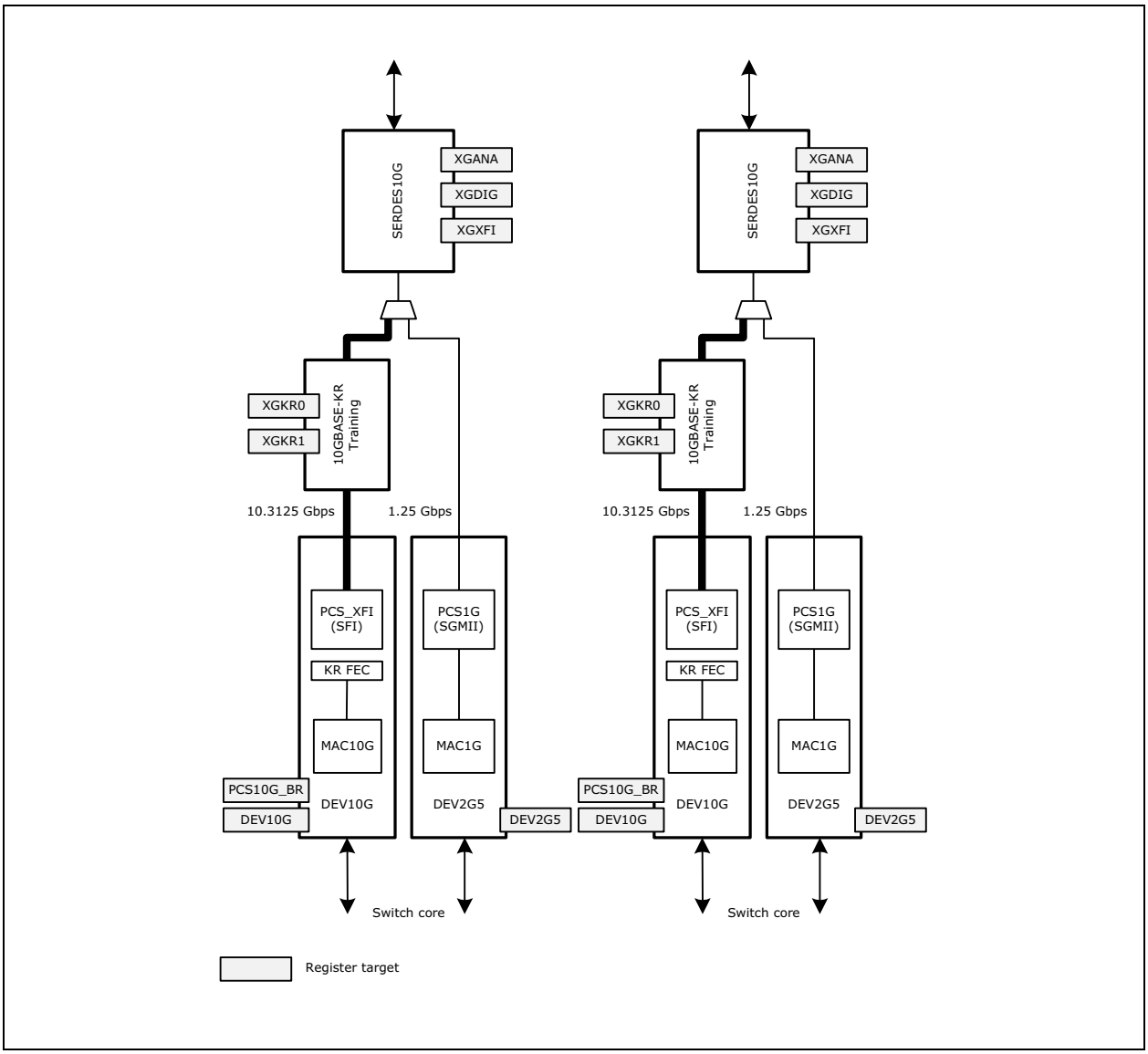
- 32 x 2G5 ports (D16-D47) - only available through multiplexing
- 13 x 5G ports (D0-D11, D64)
- 12 x 10G ports (D12-D15, D48-D55)
- 8 x 25G ports (D56-D63)

Additionally, the higher speed ports have a ‘shadow’ 2G5 device. See Figure 6-2.

- 32 x 2G5 ports (D0-D15, D48-D64)

Each logical front port supports different line speeds, and depending on the speeds supported, different device modules (MAC+PCS) are needed. A port supporting 5 Gbps, 10 Gbps, or 25 Gbps as maximum line speed will have a DEV5G, DEV10G, or DEV25G module. Also, it will have a shadow DEV2G5 port module to support lower speeds (10/100/1000/2500 Mbps). See Figure 6-2.

FIGURE 6-2: EXAMPLE OF 10G DEVICE AND SHADOW 2G5 DEVICE SHARING SERDES



To support 2G5, the IEEE 802.3 specified 1G device is timing closed to run 2G5 and is then being over-clocked by the SerDes macro. The same goes with the IEEE 802.3ae Specification for 10G device to support 25G.

Note: 100BASE-FX is only supported on S1-S24 for the associated direct port (that is, 100BASE-FX is not supported on the 25G SerDes macros, S25-S32).

Check that the customer application is not exceeding the maximum numbers for the Switch derivative used. The maximum numbers are given in Table 6-2.

TABLE 6-2: MAXIMUM PORT SPEEDS SUPPORTED

Port Mapping	VSC7546	VSC7549	VSC7552	VSC7556	VSC7558
Maximum bandwidth [Gbps]	64	90	128	160	200
Maximum number of ports	64	64	64	64	64
Max number of 1G ports	64	64	64	64	64
Max number of 1G SGMII ports	32	32	32	32	32
Max number of 100FX ports (Note 1)	24	24	24	24	24
Max number of 2.5G ports	24	36	48	64	64
Max number of 5G ports	12	18	24	32	32
Max number of 10G ports	6	9	12	16	20
Max number of 25G ports (Note 2)	0	0	4	6	8
NPI port (5G)	1	1	1	1	1

Note 1: Only on S1-S24.

2: 25G is not supported on VSC7546 and VSC7549 due to internal clock speed.

The default port mapping 1:1, where the device module matches the SerDes macro speed is similar to Figure 6-3. Note that D64 is fixed allocated to S0 and, therefore, not shown.

FIGURE 6-3: 1:1 PORT MAPPING

SerDes	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	S15	S16
Speed	5G	5G	5G	5G	5G	5G	5G	5G	5G	5G	5G	5G	10G	10G	10G	10G
Device	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15

SerDes	S17	S18	S19	S20	S21	S22	S23	S24	S25	S26	S27	S28	S29	S30	S31	S32
Speed	10G	10G	10G	10G	10G	10G	10G	10G	25G	25G	25G	25G	25G	25G	25G	25G
Device	D48	D49	D50	D51	D52	D53	D54	D55	D56	D57	D58	D59	D60	D61	D62	D63

The use of QSGMII, USGMII, or USXGMII extenders may give conflicts, so a specific device may be used multiple times, if mixing the different mapping modes. Check that the devices are not represented more than one time.

QSGMII is supported on S13-S24, whereas S13 connects to Q0, S14 to Q1, and so on. Figure 6-4 shows the attached devices to each QSGMII multiplex.

FIGURE 6-4: QSGMII (1G) MULTIPLEX

SerDes Speed	S13 10G	S14 10G	S15 10G	S16 10G	S17 10G	S18 10G	S19 10G	S20 10G	S21 10G	S22 10G	S23 10G	S24 10G
QSGMII	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	Q9	Q10	Q11
Device	D0	D4	D8	D12	D16	D20	D24	D28	D32	D36	D40	D44
Device	D1	D5	D9	D13	D17	D21	D25	D29	D33	D37	D41	D45
Device	D2	D6	D10	D14	D18	D22	D26	D30	D34	D38	D42	D46
Device	D3	D7	D11	D15	D19	D23	D27	D31	D35	D39	D43	D47

10G USGMII is supported on S17-S22, whereas S17 connects to X0, S18 to X1, and so on. Figure 6-5 shows the attached devices to each 10G USGMII multiplex.

FIGURE 6-5: 10G USGMII (1G) MULTIPLEX

SerDes Speed	S17 10G	S18 10G	S19 10G	S20 10G	S21 10G	S22 10G
USGMII	X0	X1	X2	X3	X4	X5
Device	D0	D8	D16	D24	D32	D40
Device	D1	D9	D17	D25	D33	D41
Device	D2	D10	D18	D26	D34	D42
Device	D3	D11	D19	D27	D35	D43
Device	D4	D12	D20	D28	D36	D44
Device	D5	D13	D21	D29	D37	D45
Device	D6	D14	D22	D30	D38	D46
Device	D7	D15	D23	D31	D39	D47

5G USXGMII is supported on S1-S32, whereas S1 connects to F0, S2 to F1, and so on. Figure 6-6 shows the attached devices to each 5G USXGMII multiplex.

FIGURE 6-6: 5G USXGMII (1G OR 2G5) MULTIPLEX

SerDes	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	S15	S16
Speed	5G	5G	5G	5G	5G	5G	5G	5G	5G	5G	5G	5G	10G	10G	10G	10G
USXGMII	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12	F13	F14	F15
Device	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
Device	D32	D33	D34	D35	D36	D37	D38	D39	D40	D41	D42	D43	D44	D45	D46	D47

SerDes	S17	S18	S19	S20	S21	S22	S23	S24	S25	S26	S27	S28	S29	S30	S31	S32
Speed	10G	10G	10G	10G	10G	10G	10G	10G	25G	25G	25G	25G	25G	25G	25G	25G
USXGMII	F16	F17	F18	F19	F20	F21	F22	F23	F24	F25	F26	F27	F28	F29	F30	F31
Device	D48	D49	D50	D51	D52	D53	D54	D55	D56	D57	D58	D59	D60	D61	D62	D63
Device	D16	D17	D18	D19	D20	D21	D22	D23	D24	D25	D26	D27	D28	D29	D30	D31

10G QSXGMII is supported on S17-S32, whereas S17 connects to R0, S18 to R1, and so on. Figure 6-7 shows the attached devices to each 10G QSXGMII multiplex.

FIGURE 6-7: 10G QSXGMII (1G OR 2G5) MULTIPLEX

SerDes	S17	S18	S19	S20	S21	S22	S23	S24	S25	S26	S27	S28	S29	S30	S31	S32
Speed	10G	10G	10G	10G	10G	10G	10G	10G	25G	25G	25G	25G	25G	25G	25G	25G
USXGMII	R0	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	R15
Device	D48	D49	D50	D51	D52	D53	D54	D55	D56	D57	D58	D59	D60	D61	D62	D63
Device	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
Device	D16	D17	D18	D19	D20	D21	D22	D23	D24	D25	D26	D27	D28	D29	D30	D31
Device	D32	D33	D34	D35	D36	D37	D38	D39	D40	D41	D42	D43	D44	D45	D46	D47

10G DXGMII is supported on S17-S32, whereas S17 connects to U0, S18 to U1, and so on. Figure 6-8 shows the attached devices to each 10G DXGMII multiplex.

FIGURE 6-8: 10G DXGMII (5G) MULTIPLEX

SerDes	S17	S18	S19	S20	S21	S22	S23	S24	S25	S26	S27	S28	S29	S30	S31	S32
Speed	10G	10G	10G	10G	10G	10G	10G	10G	25G	25G	25G	25G	25G	25G	25G	25G
DXGMII	U0	U1	U2	U3	U4	U5	U6	U7	U8	U9	U10	U11	U12	U13	U14	U15
Device	D48	D49	D50	D51	D52	D53	D54	D55	D56	D57	D58	D59	D60	D61	D62	D63
Device	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15

6.3 MAC-to-MAC Connections

The SerDes macros have 100Ω internal termination and biasing. *Check the use of AC coupling for DC-level adjustment and EMI suppression.* Make sure that the signal direction and polarity are correct. The SerDes macros can invert P and N to ease the layout.

It is highly recommended to simulate all 10G/25G traces, and to route them on top or bottom layer in order to avoid reflections from stubs when using vias and connectors. Trace bends of 90 degrees should not be made.

Signal detection can be omitted since MAC-to-MAC or backplane connection is always connected.

Unused SerDes interfaces must be left floating.

6.4 SFP Ports

It is important to track the individual SFP signals required by the SFP MSA. Not all must be controlled by the Switch, but must all be pulled up to 3V3. All SFP modules have built-in AC capacitors required by the SFP MSA.

TABLE 6-3: SFP SIGNALS PRESENT ON SFP CASING

SFP Pin	SFP In/Out	Remark
RX	Out	No AC-coupling as it is built into the module. No 100Ω differential termination across P and N.
TX	In	
SCL	In	Should have pull-up
SDA	In/Out	Should have pull-up
TX_FAULT	Out	4.7 kΩ pull-up to 3V3
TX_DISABLE	In	Should have pull-up, but some users prefer that the module emitting LED is powered. Normally, additional circuitry is required (like an inverter) to prevent the LED powered during reset.
MODULE_DETECT	Out	4.7 kΩ pull-up to 3V3
RATE_SEL1	In	Should have pull-up
RATE_SEL2	In	Should have pull-up
RX_LOS	Out	4.7 kΩ pull-up to 3V3

The Switch Application depends on the use of **MODULE_DETECT** to initiate I^2C reading of the SFP MSA ROM to automatically determine the SFP module type and speed.

Most SFP modules do not squelch the Rx signal when they lose signal from link partner. Therefore, the Rx signal will still be active and prevent the Switch internal Signal Detect circuitry to denote loss of signal to the PCS layer. It is crucial to route the SFP **RX_LOS** signal to the Switch. The Switch has several ways to internally route **RX_LOS** to the PCS layer, either as a GPIO input (parallel) or as an SGPIO input (serial).

The GPIO controller has 32 programmable parallel Signal Detect inputs **SFP0_SD** to **SFP31_SD**. These inputs take an SFP **RX_LOS** signal and direct it to a specific port PCS. The GPIOs operate in an Alternate mode.

All three SGPIOs can be used. It is easiest to map the **RX_LOS** signal to the PCS layer, if **RX_LOS** is the first signal in each boundary being clocked in. Otherwise, a more complicated bit mapping must take place.

6.5 TWI/I2C Interface

The two-wire serial interface (TWI) is compatible with I2C. It uses two pins that are overlaid on the GPIO pins. The controller supports standard speed of 100 kbps and fast speed of 400 kbps. Multiple bus hosts, as well as both 7-bit and 10-bit addressing, are also supported.

TABLE 6-4: I2C CONTROLLER SIGNALS

Signal	TWI	TWI_2	TWI_3
TWI_SCL	GPIO 14	GPIO 28	GPIO 48 or 50
TWI_SDA	GPIO 15	GPIO 29	GPIO 49 or 51

Note 1: TWI_SCL and TWI_SDA are recommended to be pulled high.

6.5.1 I2C CLOCK MULTIPLEXING

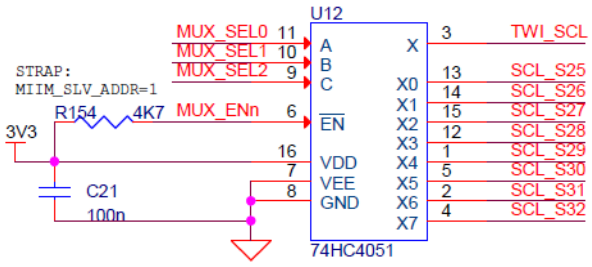
The Switch has built-in support for connecting to multiple I2C devices that use the same I2C address (for example, SFP modules). This is done using multiplexed clock outputs, **TWI_SCL_GATE[31:0]**.

Depending on which device it needs to communicate, the software can enable or disable the various clocks. **TWI_SCL_GATE[31:0]** are overlaid GPIO pins and *only available for the first TWI controller*.

Note: Clock stretching is not supported on **TWI_SCL_GATE[22]** and **TWI_SCL_GATE[23]**.

To preserve the GPIO usage or to provide it for the two other TWI Controllers, clock multiplexing can also be done externally on the PCB using fewer GPIOs for enabling and selecting signals. Figure 6-9 illustrates how to do this.

FIGURE 6-9: I2C CLOCK MULTIPLEXING



7.0 SERIAL GPIO CONTROLLER (SGPIO)

7.1 SGPIO Signals

Three serial GPIO controllers are available. Each serial GPIO controller uses a 4-pin serial interface to extend the number of available general purpose I/O pins. The 4-pin serial interface pins are overlaid on the GPIOs.

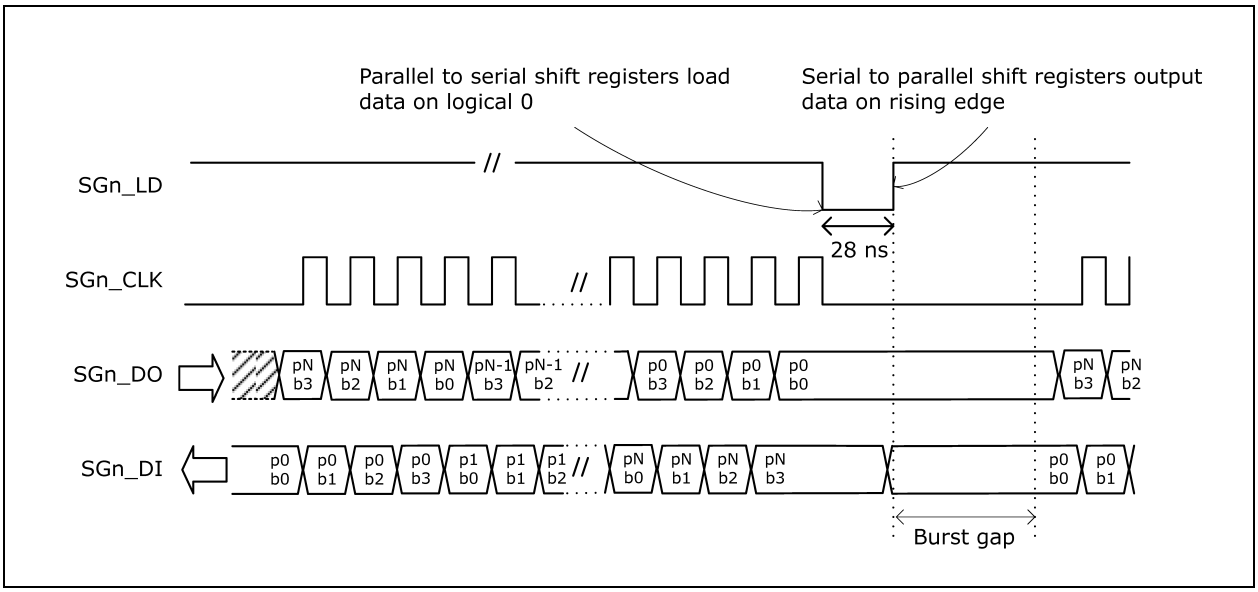
TABLE 7-1: SERIAL GPIO CONTROLLER SIGNALS

	SGPIO_0	SGPIO_1	SGPIO_2
Devices handled	**D0-D31**	**D32-D63**	**D64, D1-D15, D48-D63**
SGx_CLK (Note 1)	GPIO 0	GPIO 4	GPIO 30
SGx_DO	GPIO 1	GPIO 5	GPIO 32
SGx_DI	GPIO 2	GPIO 13	GPIO 33
SGx_LD	GPIO 3	GPIO 12	GPIO 31

Note 1: It is recommended to have footprint for a split end-termination on the CLK.

Figure 7-1 shows the I/O timing of the serial GPIO controller. Serial data are output on the SG_DO pin clocked by SG_CLK in bursts. After each burst, there is an assertion of the SG_LD signal. At the same time as shifting out serial outputs on SG_DO, the serial GPIO controller also samples the SG_DI input. The values sampled on SG_DI are made available to the software.

FIGURE 7-1: SGPIO TIMING



The maximum length of a burst is 128 bits data cycles organized by 32 ports with 4-bit port width. However, each port can be enabled or disabled individually, and the port width (number of bits per port) is also centrally configurable. All enabled ports have the same port width.

Note: The configuration of port enabling and port width applies to both serial input and output.

SG_LD can be used to ensure that outputs are stable when serial data are being shifted through the shift registers (for example, the TX_DIS output signals for the SFP modules). This can be done using the SG_LD signal to load the serial data onto shift registers parallel output pins after the burst has completed. 74HC595 is one of the shift registers that supports load input. If the serial GPIO controller is used for serial LED output, then SG_LD is optional because it is usually not detectable by the eye when serial data are updated (shift through the chain). In that case, 74HC164 can also be used, which does not have the load input.

7.2 SGPIO Constraints

When a serial output bit is configured to support link/activity LED, it must know which Switch port status to display on which SGPIO bit. The SGPIO controller uses a 1:1 mapping, which means SGPIO port 0 display link/activity for switch port 0, SGPIO port 1 display link/activity for switch port 1, and so on.

The serial input function of the SGPIO controller can automatically route Signal Detection (RX_LOS) to the internal PCS block of a certain port. Per default, the Signal Detection function also uses 1:1 mapping between the Switch port number and the SGPIO port number, so that bit 0 of each SGPIO port can be enabled for RX_LOS input.

There might be more serial output bits than serial input bits in a typical design especially when serial LED is supported. Since the port enabling and port width configuration are shared by the SGPIO output and input, the same number of serial bits in the output and input streams is present, which means the same number of external shift registers is required for both output and input chain. Hence, some shift registers are wasted on the serial input chain. To save the shift registers for the unused SGPIO input bits, the serial input bits can be looped; the SG_DI input signal is also connected to the serial input pins of the last shift register to create a loop, so that the bits in that loop can be duplicated and the length of the whole serial stream is expanded.

Note: The SGPIO2_CLK/GPIO 30 is also used for the LCPLL strapping, which must be low during reset. So if the SGPIO2_CLK is being used, it must either be buffered or AC-coupled, as the clock is not bursty.

8.0 SGMII/XFI PHY INTERFACE

When the SerDes interfaces are used to connect to an external PHY, then AC coupling is recommended between the Switch and the external PHY.

Take caution in naming the Rx and Tx pairs on the Switch and PHY. Normally, Rx is the output pair and Tx is the input pair on a PHY. This is different from how they are named on a Switch. Make sure that the output pair from the Switch is connected to the input pair of the PHY and vice versa.

8.1 MII Management Host Interfaces

In order for the software to access the external PHY registers, the MIIM interface should be connected from the Switch to the external PHY. The MIIM controller supports both Clause 22 and Clause 45. Maximum clock frequency is 25 MHz.

Apart from one hard-strapped MIIM interface, the Switch supports additional three overlaid on the GPIOs.

TABLE 8-1: MIIM CONTROLLER SIGNALS

Signal	MIIM_0	MIIM_1	MIIM_2	MIIM_3
MDC	MDC_0	GPIO 56	GPIO 58	GPIO 52 (Note 1)
MDIO	MDIO_0	GPIO 57	GPIO 59	GPIO 53 (Note 1)

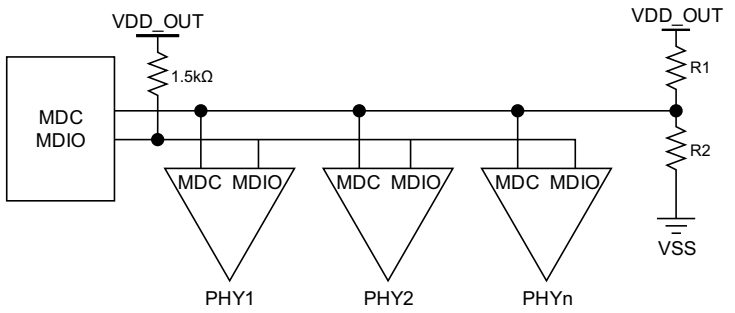
Note 1: The GPIOs used by the MIIM3 controller are shared with the MIIM_SLAVE register access functionality.

The MDIO signal is changed or sampled on the falling edge of the MDC clock by the controller. The **MDIO** pin is tri-stated between access and when expecting read data from the PHY.

Because MDIO is an open drain output, MDIO should be pulled high with a resistor around 1.5 kΩ. When connecting MDC/MDIO to multiple PHYs, the layout scheme in Figure 8-1 with split end termination on MDC is recommended.

The actual split-end termination resistor value used (for example, 330Ω) must be simulated.

FIGURE 8-1: CONNECTING MDC/MDIO TO MULTIPLE PHYS



The MIIM controller uses PHY addresses to select each of the external PHYs, so the PHY addresses must be configured differently for each PHY on the same MIIM interface (on each interface up to 32 (0-31) addresses are supported per IEEE).

Note: Sharing the Management interface between Clause 22 and Clause 45 PHYs is doable. However, some of the legacy VSC CuPHYs do respond to Clause 45 readings. This can be avoided by having the Clause 45 PHY addresses below 0x8 (b'00xxx) and the VSC CuPHY Clause 22 addresses starting at 0x10 or above (b'1xxxx). Normally, Clause 22 and Clause 45 PHYs would be on their own Management interface due to differences in their I/O level.

9.0 SERIAL CPU INTERFACE

9.1 SPI Boot and Primary QSPI Host Controller

The SPI Boot Controller shares the same I/Os as the primary QSPI Host Controller, except the D2 and D3 data signals. The SPI Boot Controller allows the Switch internal CPU to boot from a NOR Flash hooked up to the serial interface.

The SPI Boot Controller is operating in 24-bit address mode by default. In this mode, there are four programmable chip-select pins, which can each address up to 16 MB of memory. (In 32-bit mode, the entire SI region of 256 MB is addressed only via chip select 0.)

Although the Switch supports four SPI chip-select pins, only **SI_nCS0** is used by the internal CPU to perform the initial boot from a NOR Flash.

The Switch can only perform initial boot from a NOR Flash, but the Flash memory can be organized as 'NOR only', or combined 'NOR/NAND' or 'NOR/eMMC'. If the NOR Flash is greater than 16 MB, check that the nRESET_FLASH is controlled by the Switch GPIO in order to reset the NOR Flash back to page 0 on a soft reboot.

TABLE 9-1: SPI BOOT AND PRIMARY QSPI CONTROLLER SIGNALS

SPI Pin	In/Out	Remarks
SI_CLK	Out	Clock output using dedicated pin
SI_DO	Out	Data out (MOSI) using dedicated pin
SI_DI	In	Data in (MISO) using dedicated pin
SPI_D2	In/Out	Data found on overlaid GPIO 58
SPI_D3	In/Out	Data found on overlaid GPIO 59
SI_nCS0	In/Out	Active low chip-select using dedicated pin, but is also found on GPIO 51. Used as input by SI Client Controller.
SPI_nCS[3:1]	Out	Active low chip-selects overlaid on GPIO 16-18
SPI_nCS[15:4]	Out	Active low chip-selects overlaid on GPIO 25-33, 44-45, and 48

Depending on the topology, it is recommended to have **SI_CLK** pulled up to 3V3 or to use split end-termination. The **SI_CLK** is by default operating at approximately 8.1 MHz. All used SPI_nCSx must be pulled up to 3V3 using a 10 kΩ resistor.

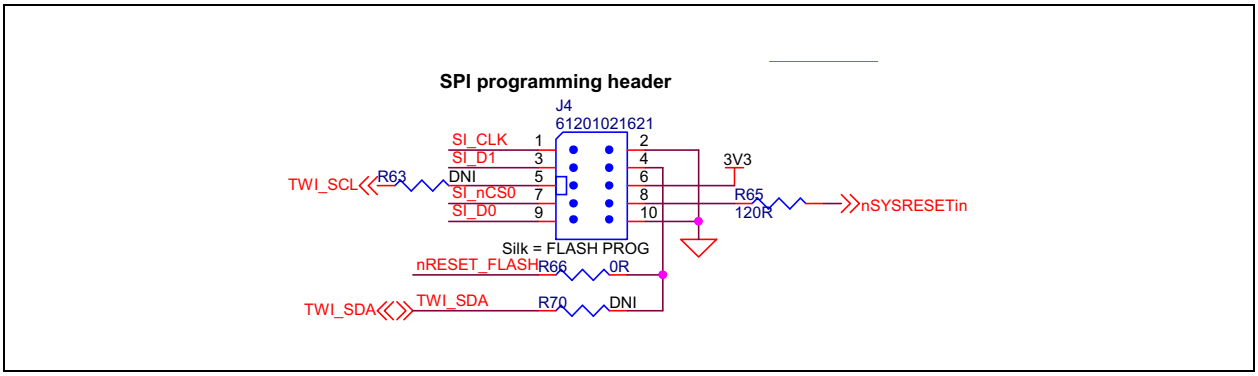
9.1.1 SPI CHIP SELECTS

The Switch implements a total of 16 SPI chip-select I/Os, **SPI_nCS[15:0]**, which are overlaid on GPIOs. The chip-select pins can be shared among the SI Client Controller, the SI Boot Controller, and the SI Host Controller. It is the programmer's responsibility to map the chip-select to the various drivers.

9.1.2 SPI FLASH PROGRAMMING HEADER

A Flash programming header in the Microchip reference design is used to support on-PCB Flash programming.

FIGURE 9-1: SPI FLASH PROGRAMMING HEADER (VSC STANDARD LAYOUT)



Pin 8 of the SPI programming header connects to nSYSRESETin, which is an input to the on-board Reset generator. The purpose of this signal is to make nSYSRESET output low during Flash programming, so that the Switch is held in reset and does not drive the SPI signals. Otherwise, both Switch and the Flash programmer drives the SPI signals, causing Flash programming failures. The nRESET_FLASH is used to enable the Flash for programming.

9.2 Secondary QSPI Host Controllers

The two secondary QSPI Host Controllers are used for accessing external SPI client devices, such as programming the serially attached Flash device on the SPI boot interface or using the SPI2 interface, which is typically connected to additional Flash memories like a Serial NAND Flash. The primary SPI signals can be found in Table 9-1, and the secondary SPI2 signals are shown in Table 9-2.

TABLE 9-2: SECONDARY QSPI CONTROLLER SIGNALS

SPI Pin	In/Out	Remarks
SPI2_SCK	Out	Clock output found on overlaid GPIO 39 (or 19)
SPI2_D0	In/Out	Data found on overlaid GPIO 40 (or 20)
SPI2_D1	In/Out	Data found on overlaid GPIO 41 (or 21)
SPI2_D2	In/Out	Data found on overlaid GPIO 42
SPI2_D3	In/Out	Data found on overlaid GPIO 43
SI_nCS[15:0]	Out	Active low chip-select found on GPIO 25-33, 44, 45, and 48

Note: The reference boards are using MX35LF2GE4AB-MI NAND.

9.3 Sub-CPU SPI Host Controllers

The two Sub-CPU/M3 SPI Host Controllers, SPI3 and SPI4, are mapped to alternate GPIO pins. The clock frequency is programmable up to 100 MHz and only one chip-select is supported – mapped from one of SI_nCS[7:5]. The SPI3 and SPI4 signals are shown in Table 9-3.

TABLE 9-3: SUB-CPU SPI CONTROLLER SIGNALS

SPI Pin	In/Out	Remarks
SPI3_SCK	Out	Clock output found on GPIO 22
SPI3_DO	Out	Data out (MOSI) found on GPIO 23
SPI3_DI	In	Data in (MISO) found on GPIO 24
SPI4_SCK	Out	Clock output found on GPIO 55
SPI4_DO	Out	Data out (MOSI) found on GPIO 56
SPI4_DI	In	Data in (MISO) found on GPIO 57
SI_nCS[7:5]	Out	Active low chip-select found on GPIO 26-28

9.4 SD/eMMC Storage Host Controller

The Storage Host Controller supports bus width of 1, 4, or 8, and frequencies of 25, 50, and 100 MHz. Table 9-4 shows the typical use for eMMC Flash interface.

TABLE 9-4: EMMC HOST CONTROLLER SIGNALS

Host Pin	In/Out	Remarks
EMMC_nRST	Out	Active low Reset overlaid on GPIO 34
EMMC_CMD	Out	Command overlaid on GPIO 38
EMMC_CK	Out	Clock overlaid on GPIO 39
EMMC_D0	In/Out	Data bit 0 overlaid on GPIO 40
EMMC_D1	In/Out	Data bit 1 overlaid on GPIO 41
EMMC_D2	In/Out	Data bit 2 overlaid on GPIO 42
EMMC_D3	In/Out	Data bit 3 overlaid on GPIO 43
EMMC_D4	In/Out	Data bit 4 overlaid on GPIO 44
EMMC_D5	In/Out	Data bit 5 overlaid on GPIO 45
EMMC_D6	In/Out	Data bit 6 overlaid on GPIO 46
EMMC_D7	In/Out	Data bit 7 overlaid on GPIO 47

Note: The reference boards are using IS21ES04G-JCLI as eMMC.

Additionally, signals specific for SD card handling can be found on the following GPIOs:

TABLE 9-5: ADDITIONAL SD CARD SIGNALS

Host Pin	In/Out	Remarks
CARD_nDETECT	In	Active low detect signal overlaid on GPIO 35
CARD_WP	In	Write protect signal overlaid on GPIO 36
CARD_LED	Out	LED signal overlaid on GPIO 37

10.0 UART CONTROLLERS

The Switch supports three UART interfaces. The UART is functionally based on the industry-standard 16550 UART (RS232 protocol). This implementation features a 16-byte receive and a 16-byte transmit FIFO.

The first UART interface is required by the Switch Application for CLI management through either RS-232 or USB. The second UART2 interface is normally used for TOD interface through RS-422.

The third UART3 is located in the Sub-CPU/M3 system.

TABLE 10-1: UART CONTROLLER INTERFACES

UART Pin	In/Out	Remarks
UART_RxD	In	Data in overlaid on GPIO 10
UART_TxD	Out	Data out overlaid on GPIO 11
UART2_RxD	In	Data in overlaid on GPIO 26
UART2_TxD	Out	Data out overlaid on GPIO 27
UART3_RxD	In	Data in overlaid on GPIO 24/49
UART3_TxD	Out	Data out overlaid on GPIO 23/48

11.0 PARALLEL INTERFACE CONTROLLER

11.1 PI Host Interface

The PI Controller in Host mode is pin-wise reduced to be dedicated to support parallel NAND devices only. When the PI Controller is in Host mode (for example, connected to a NAND device), **PI_nCS/GPIO_34** and **PI_nDONE/GPIO_37** are unused and cannot be used as ordinary GPIOs. The PI interface is shown for legacy reasons.

TABLE 11-1: PI HOST CONTROLLER INTERFACES (NAND SUPPORT)

PI Host	In/Out	Remarks
PI_nWR	Out	Active low write, active high read, overlaid on GPIO 35
PI_nOE	Out	Active low output enabled, overlaid on GPIO 36
PI_ADDR2	Out	Connects to ALE. Address. Overlaid on GPIO 38.
PI_ADDR3	Out	Connects to CLE. Command. Overlaid on GPIO 39.
PI_DATA[7:0]	In/Out	Data overlaid on GPIO 40-47

Note: NAND nCS should be pulled low at all times.

11.2 PI Client Interface

The PI Controller in Client mode allows an external CPU to do read and write to the 32-bit Switch registers. Table 11-2 lists the pins used for a Parallel Client interface.

TABLE 11-2: PI CLIENT CONTROLLER INTERFACES

PI Client i/f on Switch	In/Out	Remarks
PI_nCS	In	Chip-select overlaid on GPIO 34
PI_ADDR[1:0]	N/A	Unused, when auto (sub-word) addressing is enabled.
PI_ADDR2	In	Address signal overlaid on GPIO 38
PI_ADDR3	In	Address signal overlaid on GPIO 39
PI_SLV_PG_ADDR[3:0]	In	Client page access, overlaid on GPIO 48-51 (and 33)
PI_nWR	In	Active low write signal, overlaid on GPIO 35
PI_nOE	In	Active low output enabled, overlaid on GPIO 36
PI_DATA[7:0]	In/Out	Data overlaid on GPIO 40-47
PI_nDONE	Out/Z	An external CPU can use this signal to detect, when transfer is done, and hereby optimize the speed transfer. Overlaid on GPIO 37. Unused with NAND.

PI_DATA is driven by the Switch when PI_nCS and PI_nOE are both asserted. PI_nDone is driven when PI_nCS is asserted. The drive of PI_nDone is extended a short period after PI_nCS is deasserted, which gives time to tri-state the PI_nDone signal as inactive before it is released.

To access the Switch registers, the full 32-bit read and write must be performed. Because the PI width is 8-bit, four sequential accesses are required to read or write to a register. By default, the PI Client Controller automatically keeps track of outstanding accesses and aligns current PI_DATA appropriately. This feature is called auto (sub-word) addressing, which makes PI_ADDR[1:0] not needed.

11.3 Using Paged Access To Get Fixed PI Timing

By enabling paged access, all parallel accesses to the Switch have timing, as if they are directly accessing the fast targets on the register ring. This means that an external CPU can have a fixed I/O timing. Specific page registers are used for this purpose.

12.0 DDR3/3L/4 MEMORY CONTROLLER – SDRAM INTERFACE

The Memory Controller operates at maximum 625 MHz to support the speed of 2500 MT/s on the DDR interface. It supports 5-byte lanes (32-bit data bus, along with 8-bit sideband ECC). The Memory Controller supports SDRAM with data width = x8 or x16. It also supports half data-bus width operation, where it uses the lower 16-bit of the total 32-bit data bus.

The Memory Controller supports up to 18-bit address bus. The maximum amount of physical memory that can be attached to the controller (per byte lane) is 2 GB and therefore a total of 8 GB.

Note: Currently the maximum speed verified is 2000 MT/s for DDR3 and 1417 MT/s for DDR4.

TABLE 12-1: DDR CONTROLLER INTERFACES

DDR Interface	In/Out	Remarks
DDR_A[15:0]	Out	Address bus
DDR_BA[2:0], DDR_BG1	Out	Bank address
DDR_Ck_t/c, DDR_CKE[1:0]	Out	DDR_CK_t/c must be routed as 100Ω differential pair
DDR_3WE_n/DDR_3CAS_n/ DDR_3RAS_n	Out	—
DDR_DQ[7:0], DDR_DM0	In/Out	Data bus. Max skew 1 mm. On-die termination of DQ signals should be used as applicable. Bit swizzling is allowed for all bits within a byte lane. Byte lanes may be swapped freely. However, depending on the RAM, DQ0 may need to be connected directly if the design requires write leveling.
DDR_DQ[15:8], DDR_DM1	In/Out	
DDR_DQ[23:16], DDR_DM2	In/Out	
DDR_DQ[31:24], DDR_DM3	In/Out	
DDR_DQ[39:32], DDR_DM4, ECC	In/Out	
DDR_DQS[4:0]_t/c	Out	DDR_DQSx_t/c must be routed as 100Ω differential pairs.
DDR_CS_n[1:0]	Out	—
DDR_ODT[1:0]	Out	—
DDR_PAR	Out	—
DDR_ALERT_n	Out	Pulled to VDD
DDR_RESET_n	Out	—
DDR_RZQ	Out	Bias: 240Ω to VSS
DDR_ZCTRL	Out	—
DDR_VREFOCA, DDR_VREFODQ (Note 1)	Out	The reference voltage is generated internally, and is output to these pins. If buffered, this voltage can be used as reference voltage for the attached RAM. This is not currently supported, and the pin should be left floating.
DDR_VTT	—	Externally generated

Note 1: The internally generated references are available on these pins: one for Command/Address and one for Data. If only one RAM device is used (16-/32-bit wide), these can be connected directly to the RAM reference pins. In the current design using multiple RAMs, DDR_VREFOCA and DDR_VREFODQ cannot drive the RAM input reference without being buffered. The reference design shows how to use a resistor divider as the reference instead, or how to use a Sink/Source DDR Termination Regulator to buffer the DDR_VREF voltage.

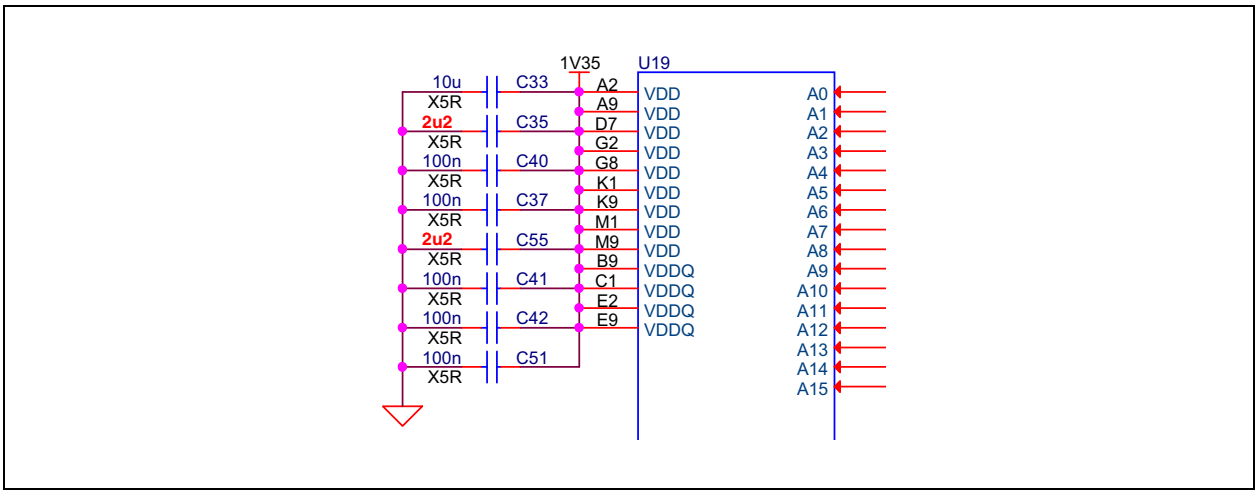
Command lane signals must use midpoint termination at the end of the trace. The trace lengths between each DDR RAM must also match in length. Maximum skew is 1 mm.

Trace impedance for the DDR traces should be in the range of 40Ω to 80Ω.

Termination resistors may not be needed if the DDR RAM are placed close enough to the Switch, so trace lengths become 35 mm maximum. This is more or less only possible when using a single 16-/32-bit DDR device.

The original design uses 100 nF capacitors on the supply pins of the DDR devices. It has been identified that this is not enough, so verify that some of the capacitors are changed to higher capacity (2.2 µF for example).

FIGURE 12-1: ADDITIONAL BULK CAPACITORS ON EACH DDR DEVICE



It is highly recommended to use the same DDR device as the reference designs use or to ensure that the substitute is fully compliant, that is, because the driver settings are currently hard-coded into UBoot. In case of using another DDR device than the two already provided, the VSC SW team does not provide any support – due to the lack of testing possibilities.

PCB134 uses 5x512MB DDR4, MT40A512M8RH-083E. PCB135 uses 5x512MB DDR3, IS43TR85120AL-107.

It is strongly recommended for customers to perform simulations on the DDR interface for the specific application and topology. Check also that the Switch DDR supply, Vdd_IODDR, matches the DDR RAM used: 1.5V on DDR3, 1.35 on DDR3L, and 1.2V on DDR4.

13.0 JTAG INTERFACE

The Switch incorporates multiple JTAG controllers sharing a single JTAG interface. The ownership of the JTAG interface is controlled through strapping.

TABLE 13-1: JTAG MODES

JTAG_SEL[1:0]	Mode
00	DDR interface
01	ICE ARM53
10	ICE ARM M3
11	JTAG boundary scan

The Switch JTAG interface has the following JTAG signals (see Table 13-2). Check that the required resistor pulls are fulfilled.

TABLE 13-2: JTAG SIGNALS

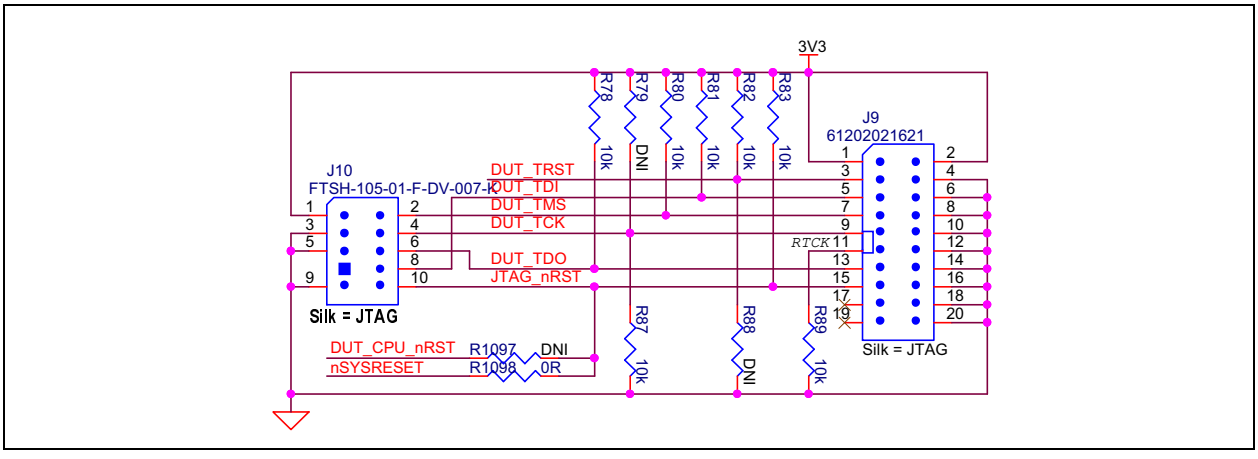
JTAG Signals (Note 1)	In/Out	Remarks
JTAG_SEL[1:0]	Input - IPU/IPD	JTAG multiplex selector. Without pull resistors – default mode is '10' ARM M3.
JTAG_nTRST (Note 2)	Input	Asynchronous initialization of JTAG. 10 kΩ pull-up required for normal operation.
JTAG_TMS	Input	Test mode select. Controls JTAG operation. Source termination and 10K pull-up.
JTAG_TCK	Input - IPU	Provides the clock for JTAG logic, 10 kΩ pull-down and footprint for pull-up
JTAG_TDI	Input - IPU	Data input provides serial instructions and data to the JTAG logic. 10 kΩ pull-up.
JTAG_TDO	Output	Provides serial data out from the JTAG logic. Source termination and 10K pull-up.
JTAG_CPU_nRST	Input - IPU	Internal pull-up

Note 1: The JTAG signals are not 5V tolerant.

2: JTAG_nTRST should be held low, until all power supply voltages are up and running.

A standard legacy ARM 20-pin (0.1") header or 10-pin (0.05") header is normally used for boundary scan and ICE.

FIGURE 13-1: JTAG CONNECTOR



The legacy header is kept for access to JTAG_nTRST. Likewise, JTAG_RTCK, Return Test Clock Input is found in the legacy header.

14.0 SYSTEM RESET

The **nRESET** and **JTAG_nTRST** inputs must be held low until all power supply voltages have reached their recommended operating condition values. When the JTAG interface is not used, JTAG_nTRST is recommended to be pulled high.

nRESET (active low) must be deasserted no less than 20 ms after the power supply voltages have all reached their recommended values and the core reference clock is stable. For this reason, a reset generator with Power-on Reset (POR) delay circuit must be used on the **nRESET** pin. The MIC6315 can be used to provide the POR delay after valid power supplies and clock.

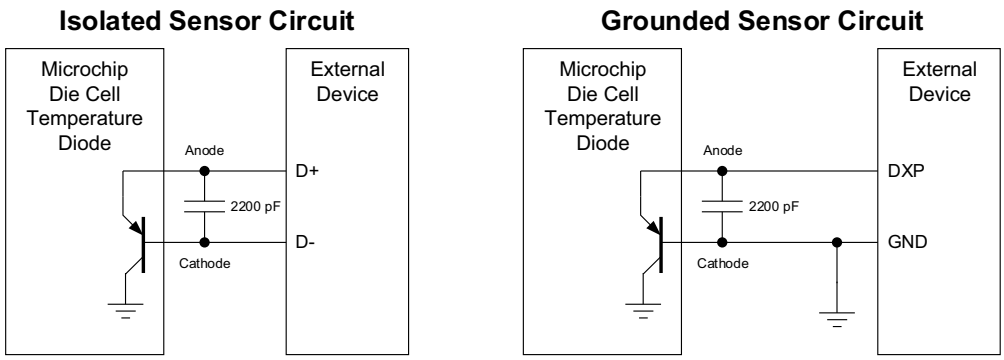
It is also recommended to use a reset generator with a manual input, so that the Switch can be put into reset during on-PCB Flash programming. While the reset signal resets the Switch, it also resets the Flash memory, external PHYs, shift registers for SGPIO, and other parts that must be put in known state.

15.0 TEMPERATURE SENSOR

The Switch includes an on-die diode and internal circuitry for monitoring die temperature (junction temperature). The operation and accuracy of the diode is not guaranteed and should only be used as a reference.

The on-die thermal diode requires an external thermal sensor located on the board or in a stand-alone measurement kit. Temperature measurement using a thermal diode is very sensitive to noise. The following illustration shows a generic application design.

FIGURE 15-1: THERMAL DIODE



Note: Microchip does not support or recommend operation of the thermal diode under reverse bias.

16.0 MISCELLANEOUS

16.1 GPIO Mapped Interrupts

It is possible to map the internal interrupt source to an output overlaid on the GPIO pins. It is possible to drive the output pin permanently or emulate an open-collector output. Likewise, external interrupts from PHYs can be made an input source. If input interrupt is being used, 10 kΩ pull-up to 3V3 is required. Polarity can be changed on the register level.

TABLE 16-1: INTERRUPT I/O

Interrupt	IRQ_0_IN	IRQ_1_IN	IRQ_0_OUT	IRQ_1_OUT
GPIO	6	7	6, 20, or 22	7 or 21

16.2 GPIO Mapped Fan Controller

The Switch includes a fan controller that can be used to control and monitor a system fan. A pulse-width-modulation (PWM) output regulates the fan speed. The fan speed is monitored using a TACHO input. The fan controller is especially powerful when combined with the internal temperature sensor.

TABLE 16-2: FAN I/O

Fan Signal	TACHO_IN	PWM_OUT
GPIO	21 or 22	23 or 30

The reference design demonstrates a PWM circuit connection to the fan(s) using a technique called ground-chopping.

16.3 Reserved Pins

There are a number of reserved pins that are crucial to be correctly handled.

TABLE 16-3: RESERVED I/O

Reserved	Pull	Remarks
0	Pull-up	LVCMOS
1	Pull-down	—
2	Leave floating	Analog
3	Leave floating	SSTL
4	Leave floating	SSTL
5	Leave floating	Analog
6	Leave floating	Analog
7	Leave floating	—
8	Leave floating	—
9	Leave floating	—
10	Leave floating	Analog

17.0 GPIO USAGE

Table 13-2 should be checked to avoid overlapping functions.

TABLE 17-1: GENERAL PURPOSE I/O USAGE

GPIO	ALT '01'	√	ALT '10'	√	ALT '11'	√	Interface Mode	X
0	SG0_CLK		PLL_STAT0		—		—	
1	SG0_DO		—		—		—	
2	SG0_DI		—		—		—	
3	SG0_LD		—		—		—	
4	SG1_CLK		—		—		—	
5	SG1_DO		—		—		—	
6	IRQ0_IN		IRQ0_OUT		SFP15_SD		—	
7	IRQ1_IN		IRQ1_OUT		SFP16_SD		—	
8	PTP_0		—		SFP17_SD		—	
9	PTP_1		SFP6_SD		TWI_SCL_GATE15		—	
10	UART_RxD		—		—		—	
11	UART_TxD		—		—		—	
12	SG1_LD		—		—		—	
13	SG1_DI		—		—		—	
14	TWI_SCL		TWI_SCL_GATE0		—		—	
15	TWI_SDA		—		—		—	
16	SPI_nCS1		TWI_SCL_GATE1		SFP18_SD		—	
17	SPI_nCS2		TWI_SCL_GATE2		SFP19_SD		—	
18	SPI_nCS3		TWI_SCL_GATE3		SFP20_SD		—	
19	PCI_wake		TWI_SCL_GATE4		SFP21_SD		SPI2_SCK	
20	IRQ0_OUT		TWI_SCL_GATE5		SFP22_SD		SPI2_D0	
21	IRQ1_OUT		TACHO		SFP23_SD		SPI2_D1	
22	TACHO		IRQ0_OUT		TWI_SCL_GATE16		SPI3_SCK	
23	PWM		UART3_TxD		TWI_SCL_GATE17		SPI3_DO	
24	PTP_2		UART3_RxD		TWI_SCL_GATE18		SPI3_DI	
25	PTP_3		SPI_nCS4		TWI_SCL_GATE19		—	
26	UART2_RxD		SPI_nCS5		TWI_SCL_GATE20		SPI_nCS5	
27	UART2_TxD		SPI_nCS6		TWI_SCL_GATE21		SPI_nCS6	
28	TWI2_SCL		SPI_nCS7		SFP24_SD		SPI_nCS7	
29	TWI2_SDA		SPI_nCS8		SFP25_SD		SPI_nCS8	
30	SG2_CLK		SPI_nCS9		PWM		—	
31	SG2_LD		SPI_nCS10		TWI_SCL_ GATE22_AD		—	
32	SG2_DO		SPI_nCS11		TWI_SCL_ GATE23_AD		—	
33	SG2_DI		SPI_nCS12		SFP26_SD		—	
34	—		TWI_SCL_GATE6		EMMC_nRST		PI_nCS	
35	SFP27_SD		TWI_SCL_GATE7		CARD_nDETECT		PI_nWR	
36	SFP28_SD		TWI_SCL_GATE8		CARD_WP		PI_nOE	
37	SFP29_SD		—		CARD_LED		PI_nDONE	
38	—		TWI_SCL_GATE9		EMMC_CMD		PI_ADDR2	
39	SPI2_SCK		TWI_SCL_GATE10		EMMC_CK		PI_ADDR3	

TABLE 17-1: GENERAL PURPOSE I/O USAGE (CONTINUED)

GPIO	ALT '01'	√	ALT '10'	√	ALT '11'	√	Interface Mode	X
40	SPI2_D0		TWI_SCL_GATE11		EMMC_D0		PI_DATA0	
41	SPI2_D1		TWI_SCL_GATE12		EMMC_D1		PI_DATA1	
42	SPI2_D2		TWI_SCL_GATE13		EMMC_D2		PI_DATA2	
43	SPI2_D3		TWI_SCL_GATE14		EMMC_D3		PI_DATA3	
44	SPI_nCS14		SFP7_SD		EMMC_D4		PI_DATA4	
45	SPI_nCS15		SFP8_SD		EMMC_D5		PI_DATA5	
46	—		SFP9_SD		EMMC_D6		PI_DATA6	
47	—		SFP10_SD		EMMC_D7		PI_DATA7	
48	TWI3_SCL		SPI_nCS13		SFP30_SD		UART3_TxD	
49	TWI3_SDA		—		SFP31_SD		UART3_RxD	
50	SFP0_SD		—		TWI_SCL_GATE24		TWI3_SCL	
51	SFP1_SD		SPI_nCS0		TWI_SCL_GATE25		TWI3_SDA	
52	SFP2_SD		MIIM3_MDC		TWI_SCL_GATE26		MIIM_SLV_MDC	
53	SFP3_SD		MIIM3_MDIO		TWI_SCL_GATE27		MIIM_SLV_MDIO	
54	SFP4_SD		PTP_2		TWI_SCL_GATE28		MIIM_SLV_ADDR	
55	SFP5_SD		PTP_3		PCI_Wake		SPI4_SCK	
56	MIIM1_MDC		SFP11_SD		TWI_SCL_GATE29		SPI4_DO	
57	MIIM1_MDIO		SFP12_SD		TWI_SCL_GATE30		SPI4_DI	
58	MIIM2_MDC		SFP13_SD		TWI_SCL_GATE31		SPI_D2	
59	MIIM2_MDIO		SFP14_SD		—		SPI_D3	
60	RECO_CLK0		—		—		—	
61	RECO_CLK1		—		—		—	
62	RECO_CLK2		PLL_STAT0		—		—	
63	RECO_CLK3		—		—		—	

NOTES:

18.0 HARDWARE CHECKLIST SUMMARY

TABLE 18-1: HARDWARE DESIGN CHECKLIST

Section	Check	Explanation	√	Notes
Section 2.0, "General Considerations"	Section 2.1, "Required References"	All necessary documents are on hand.		
	Section 2.2, "Pin Check"	The pins match the data sheet.		
	Section 2.3, "Strapping Pins"	The strapping pins are according to Table 2-1.		
Section 3.0, "Power Supplies and Grounding"	Section 3.1, "Power Supplies"	The individual power supplies are according to Table 3-1.		
	Section 3.2, "Power Supply Sequencing"	Check power-up (and power-down) sequence.		
	Section 3.3, "Ground"	Check for proper grounding and shielding on connectors.		
Section 4.0, "Reference Clocks"	Section 4.0, "Reference Clocks"	Check the individual clocks are according to Table 4-1.		
	Section 4.1, "Differential Clock Input"	Verify each reference clock is according to the differential or single-ended input sections, and the data sheet specified jitter requirements.		
	Section 4.2, "Single-Ended Clock Input"			
	Section 4.3, "Recovered Output Clocks"	Verify the use of the recovered clocks.		
	Section 4.4, "PTP Engine - Input/Output Clocks"	Verify the use of the PTP clocks.		
Section 5.0, "CPU System"	Section 5.1, "Internal CPU Auto Boot Mode"	Verify the use of SPI NOR Flash and Programming header.		
	Section 5.2, "External CPU Mode"	Verify the use of SPI or MIIM Client interface access.		
Section 6.0, "Port Configuration"	Section 6.1, "SerDes Interface"	Check connection and possible AC-coupling.		
	Section 6.2, "Port Mapping"	If multiplexing is being used, verify that ports are not represented multiple times.		
	Section 6.3, "MAC-to-MAC Connections"	Check connection and possible AC-coupling.		
	Section 6.4, "SFP Ports"	Verify each SFP signal.		
	Section 6.5, "TWI/I^{2}C Interface"	Check the use of I^{2}C controllers and clock multiplexing.		
Section 7.0, "Serial GPIO Controller (SGPIO)"	Section 7.1, "SGPIO Signals"	Verify SGPIO signals.		
	Section 7.2, "SGPIO Constraints"	Verify the use of RX_LOS and buffering SGPIO2_CLK.		
Section 8.0, "SGMII/XFI PHY Interface"	Section 8.1, "MII Management Host Interfaces"	Verify each Management interface being used.		

TABLE 18-1: HARDWARE DESIGN CHECKLIST (CONTINUED)

Section	Check	Explanation	√	Notes
Section 9.0, "Serial CPU Interface"	Section 9.1, "SPI Boot and Primary QSPI Host Controller"	Verify the Flash model, programming header, proper pull-up, and clock termination.		
	Section 9.2, "Secondary QSPI Host Controllers"	Verify proper pull-up and clock termination.		
	Section 9.3, "Sub-CPU SPI Host Controllers"	Verify Chip Select mapping, proper pull-up, and clock termination.		
	Section 9.4, "SD/eMMC Storage Host Controller"	Verify memory signals.		
Section 10.0, "UART Controllers"	Section 10.0, "UART Controllers"	Verify the use of UART controllers.		
Section 11.0, "Parallel Interface Controller"	Section 11.1, "PI Host Interface"	Verify the connection to Parallel NAND. GPIO 34 and 37 cannot be used.		
	Section 11.2, "PI Client Interface"	Verify the connection to Host CPU.		
Section 12.0, "DDR3/3L/4 Memory Controller – SDRAM Interface"	Section 12.0, "DDR3/3L/4 Memory Controller – SDRAM Interface"	Verify the connection to the DDR devices.		
Section 13.0, "JTAG Interface"	Section 13.0, "JTAG Interface"	Verify JTAG signals.		
Section 14.0, "System Reset"	Section 14.0, "System Reset"	Verify Reset circuitry.		
Section 15.0, "Temperature Sensor"	Section 15.0, "Temperature Sensor"	Verify Temperature Monitor circuitry.		
Section 16.0, "Miscellaneous"	Section 16.1, "GPIO Mapped Interrupts"	Verify interrupt circuitry.		
	Section 16.2, "GPIO Mapped Fan Controller"	Verify fan circuitry.		
	Section 16.3, "Reserved Pins"	Verify Reserved pins.		
Section 17.0, "GPIO Usage"	Section 17.0, "GPIO Usage"	Verify GPIO usage. Customer should make it as close to the reference design as possible to lower the software effort when bringing up the customer board.		

APPENDIX A: REVISION HISTORY

TABLE A-1:

Revision Level & Date	Section/Figure/Entry	Correction
DS00003911A (04-13-21)	Initial release	

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