Application Report
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System Design Guidelines for the TM4C123x Family of Tiva™ C Series Microcontrollers

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ABSTRACT

The Tiva™ C series TM4C123x microcontrollers are highly-integrated system-on-chip (SOC) devices with extensive interface and processing capabilities. Consequently, there are many factors to consider when creating a schematic and designing a circuit board. By following the recommendations in this design guide, you will increase your confidence that the board will work successfully the first time it is powered it up.

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1 Introduction

The General Design Information section of this guide contains design information that applies to most designs (Section 3). Topics include important factors in the schematic design and layout of power supplies, oscillators, and debug accessibility. The Feature-Specific Design Information section describes specific peripherals and their unique considerations that are relevant to your design (Section 4).

To further assist you with the design process, Texas Instruments provides a wide range of additional design resources, including application reports and reference designs. See the System Design Examples (Section 5) for links to these resources.

2 Using This Guide

The information in this design guide is intended to be general enough to cover a wide range of designs by describing solutions for typical situations. However, because every system is different, it is inevitable that there will be conflicting requirements and potential trade-offs, particularly in designs that include high-performance analog circuits, radio frequencies, high voltages, or high currents. If your design includes these features, then special considerations beyond the scope of this application report may be necessary.

Where possible, the distinction is made between *preferred practice* and *acceptable practice*. This distinction addresses the reality that constraints such as size, cost, and layout restrictions might not always allow for best-practice design.

When considering which practices to apply to a design, one of the most important factors is the I/O switching rate and current. If only low-speed, low-current switching on the Tiva™ C Series peripheral pins, then acceptable-practice rules are likely sufficient. If high-speed switching is present, particularly with simultaneous transitions, then best-practice rules are recommended.

NOTE: Some of the information in this guide comes directly from the individual Tiva™ C series microcontroller data sheets. The microcontroller data sheets are the defining documents for device usage and may contain specific requirements that are not covered in this design guide. You should always use the most current version of the data sheet and also check the most recent errata documents for the part number you have selected. Visit www.ti.com/tiva-c to sign up for email alerts specific to a Tiva C Series part number. This document defines system design guidelines for Tiva C Series microcontrollers with part numbers starting with *TM4C123*.

3 General Design Information

This section contains design information that applies to most Tiva™ C series microcontrollers including:

- Package Footprint
- PCB Stack-Up
- General Routing Rules
- Power
- Reset
- Oscillators
- JTAG Interface
- ETM Interface
- System
- All External Signals

3.1 Package Footprint

Packages for Tiva™ C devices are PBGA, TQFP or LQFP. Package details and dimensions can be found in the data sheet for the part. PCB footprints for the part should be created using the IPC-7351 standard. For BGA parts, the nominal ball diameter is used as a reference for the landing pad size and solder mask opening for each ball pad. For TQFP and LQFP parts, the package and lead dimensions maximum and minimum specifications along with standard tolerances are used to calculate the pad size and locations. Many PCB layout tools offer "package wizards" to perform these calculations.

3.1.1 157-Ball BGA Package (ZRB)

The 157-Ball BGA package is 9 mm x 9 mm x 1 mm in size. The ball array consists of a 13x13 ball array with a ball pitch of 0.65 mm. Selected balls are not populated in order to allow the BGA to be routed on a four-layer board. See Figure 1.

Ball J7 is populated in order to provide an obvious orientation of the part for both layout and assembly.

The IPC-7351 standard for a NSMD (Non Solder Mask Defined) pad for a 0.35-mm nominal ball diameter is a 0.28-mm land pad with a 0.33-mm solder mask opening as shown in the "Preferred Size" column of Table 1. The 0.28-mm land pad size results in a maximum 0.4-mm via pad size if 0.1-mm spacing is to be maintained, see Section 3.4.1 for details on the trace width and spacing.

A compromise can be made by decreasing the land pad size in order to increase the via pad size while still maintaining the 0.1-mm spacing as detailed in the "Acceptable Size" column of Table 1. The larger via pad size may mean cheaper PCB costs, however, the smaller land pad for the BGA ball may result in a decrease in assembly yield or increased assembly cost when manufactured in large volumes, due to the assembly manufacturer having to be more careful with alignment of the part to the footprint during assembly. Consult the PCB fab house and the assembly manufacturer to understand the cost tradeoffs associated with this choice.

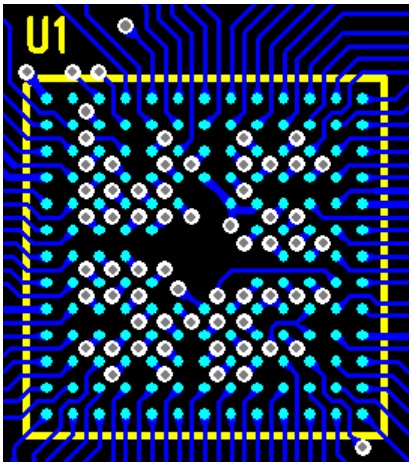


Figure 1. ZRB 157-Ball BGA Footprint Top View

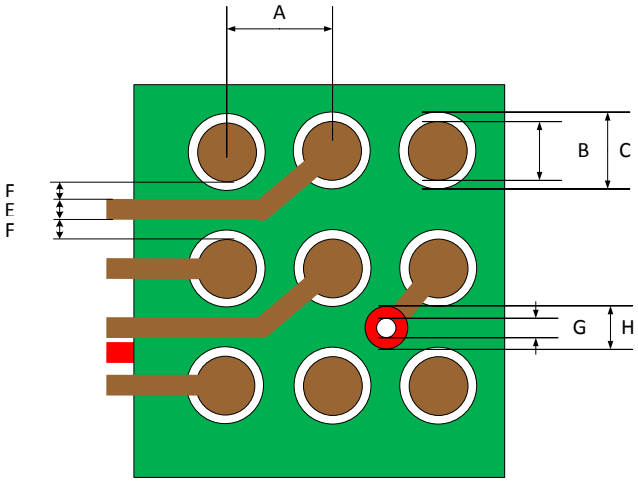


Figure 2. ZRB 157-Ball BGA Pad Dimensions

Table 1. Dimensions for Figure 2

Designator	Description	Preferred Size	Acceptable Size
A	Ball Pitch	0.65 mm / 25.59 mil	0.65 mm / 25.59 mil
B	Landing Pad Size	0.28 mm / 11.00 mil	0.2286 mm / 9.00 mil
C	Solder Mask Opening	0.33 mm / 13.00 mil	0.28 mm / 11.00 mil
D	Via to Landing Pad Spacing (D not shown in Figure)	0.1164 mm / 4.48 mil	0.1153 mm / 4.54 mil
E	Trace Width/Trace Spacing	0.1016 mm / 4.00 mil	0.1016 mm / 4.00 mil
F	Trace to Landing Pad Spacing	0.1342 mm / 5.28 mil	0.1592 mm / 6.27 mil
G	Via Drill Size	0.1524 mm / 6.00 mil	0.23 mm / 9.00 mil
H	Via Pad Size	0.4064 mm / 16.00 mil	0.46 mm / 18.00 mil

3.1.2 144-Pin LQFP Package (PGE)

The 144-Pin LQFP package is 20 mm x 20 mm x 1.6 mm in size. The package has 36 pins per side with a pin pitch of 0.5 mm. Figure 3 shows the results of a PCB footprint calculator that follows the IPC-7351 specification based on the package tolerances.

Solder Mask oversize is dependent on the tolerances and capabilities of the PCB fabrication shop being used. Two common options for a 0.5-mm pitch LQFP are:

1. Make the solder mask the same size as the pad (0 oversize) and allow the fab shop to make any required adjustments to the gerber files as required for their process.
2. Make the solder mask 0.08 mm/3.1 mil larger than the pad (0.05 mm/2.0 mil oversize) and confirm that the fab shop can handle the 0.12 mm/4.7 mil solder mask width between pads.

Paste Mask is typically the same size as the pad (0 oversize).

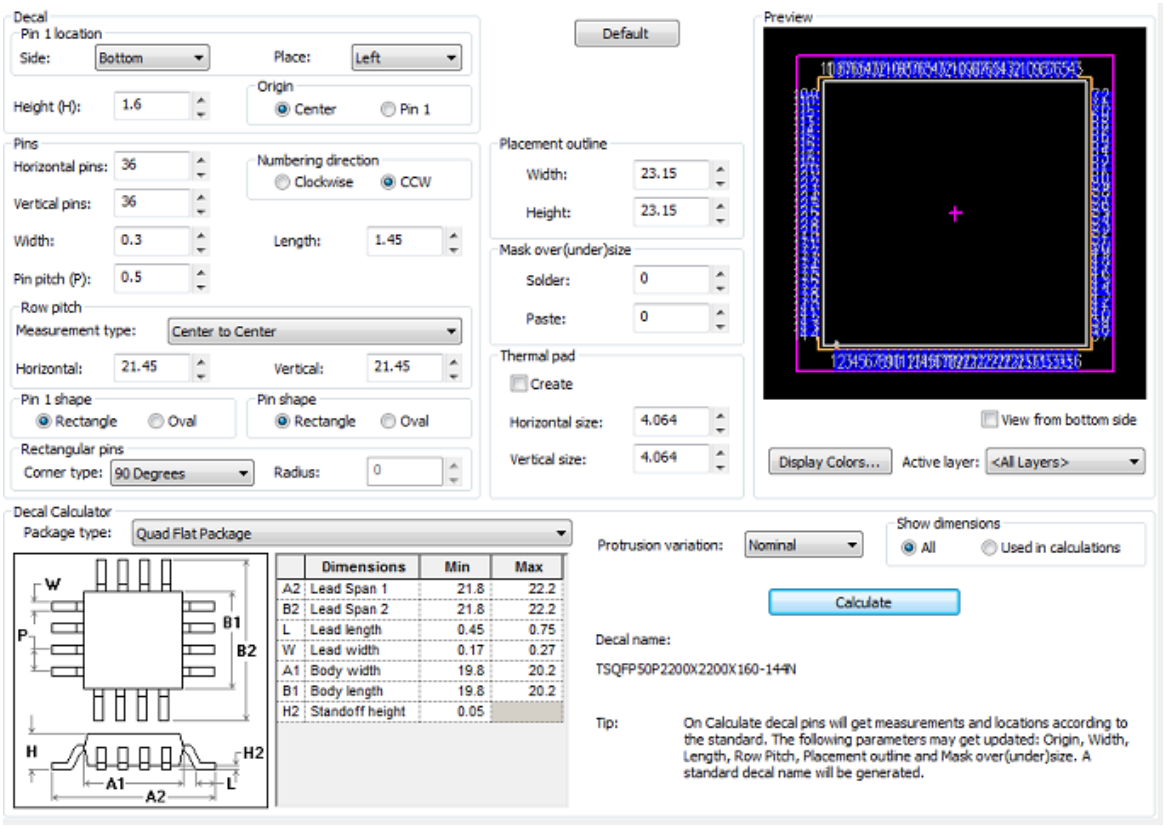


Figure 3. 144-Pin LQFP Footprint

Table 2. 144-Pin LQFP Footprint Dimensions

Designator	Description	Size
A	Pad Pitch	0.5 mm / 19.89 mil
B	Pad Width	0.3 mm / 11.81 mil
C	Pad Length	1.45 mm / 57.09 mil
D	Horizontal Row Pitch (Pad Center to Pad Center)	21.45 mm / 844.49 mil
E	Vertical Row Pitch (Pad Center to Pad Center)	21.45 mm / 844.49 mil
F	Solder Mask Oversize is dependent on fab capabilities and tolerances	0 mm / 0 mil to 0.08 mm / 3.15 mil
G	Solder Paste Oversize	0 mm / 0 mil

3.1.3 100-Pin LQFP Package (PZ)

The 100-Pin LQFP package is 14 mm x 14 mm x 1.6 mm in size. The package has 25 pins per side with a pin pitch of 0.5 mm. Figure 4 shows the results of a PCB footprint calculator that follows the IPC-7351 specification based on the package tolerances.

Solder Mask oversize is dependent on the tolerances and capabilities of the PCB fabrication shop being used. Two common options for a 0.5-mm pitch LQFP are:

1. Make the solder mask the same size as the pad (0 oversize) and allow the fab shop to make any required adjustments to the gerber files as required for their process.
2. Make the solder mask 0.08 mm/3.1 mil larger than the pad (0.05 mm/2.0 mil oversize) and confirm that the fab shop can handle the 0.12-mm/4.7-mil solder mask width between pads.

Paste Mask is typically the same size as the pad (0 oversize).

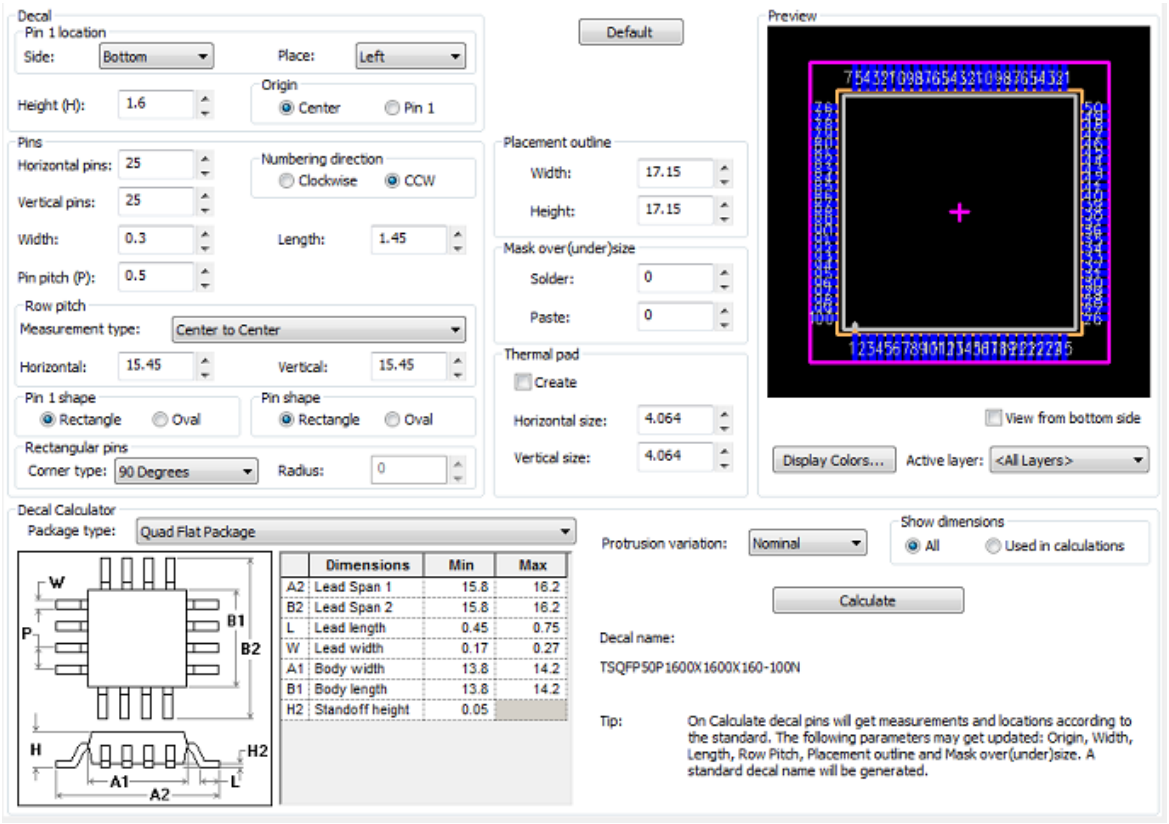


Figure 4. 100-Pin LQFP Footprint

Table 3. 100-Pin LQFP Footprint Dimensions

Designator	Description	Size
A	Pad Pitch	0.5 mm / 19.89 mil
B	Pad Width	0.3 mm / 11.81 mil
C	Pad Length	1.45 mm / 57.09 mil
D	Horizontal Row Pitch (Pad Center to Pad Center)	15.45 mm / 608.27 mil
E	Vertical Row Pitch (Pad Center to Pad Center)	15.45 mm / 608.27 mil
F	Solder Mask Oversize is dependent on fab capabilities and tolerances	0 mm / 0 mil to 0.08 mm /3.15 mil
G	Solder Paste Oversize	0 mm / 0 mil

3.2 64-Pin LQFP Package (PM)

The 64-Pin LQFP package is 10 mm x 10 mm x 1.4 mm in size. The package has 16 pins per side with a pin pitch of 0.5 mm. Figure 5 shows the results of a PCB footprint calculator that follows the IPC-7351 specification based on the package tolerances.

Solder Mask oversize is dependent on the tolerances and capabilities of the PCB fabrication shop being used. Two common options for a 0.5-mm pitch LQFP are:

1. Make the solder mask the same size as the pad (0 oversize) and allow the fab shop to make any required adjustments to the gerber files as required for their process.
2. Make the solder mask 0.08 mm/3.1 mil larger than the pad (0.05 mm/2.0 mil oversize) and confirm that the fab shop can handle the 0.12-mm/4.7-mil solder mask width between pads.

Paste Mask is typically the same size as the pad (0 oversize).

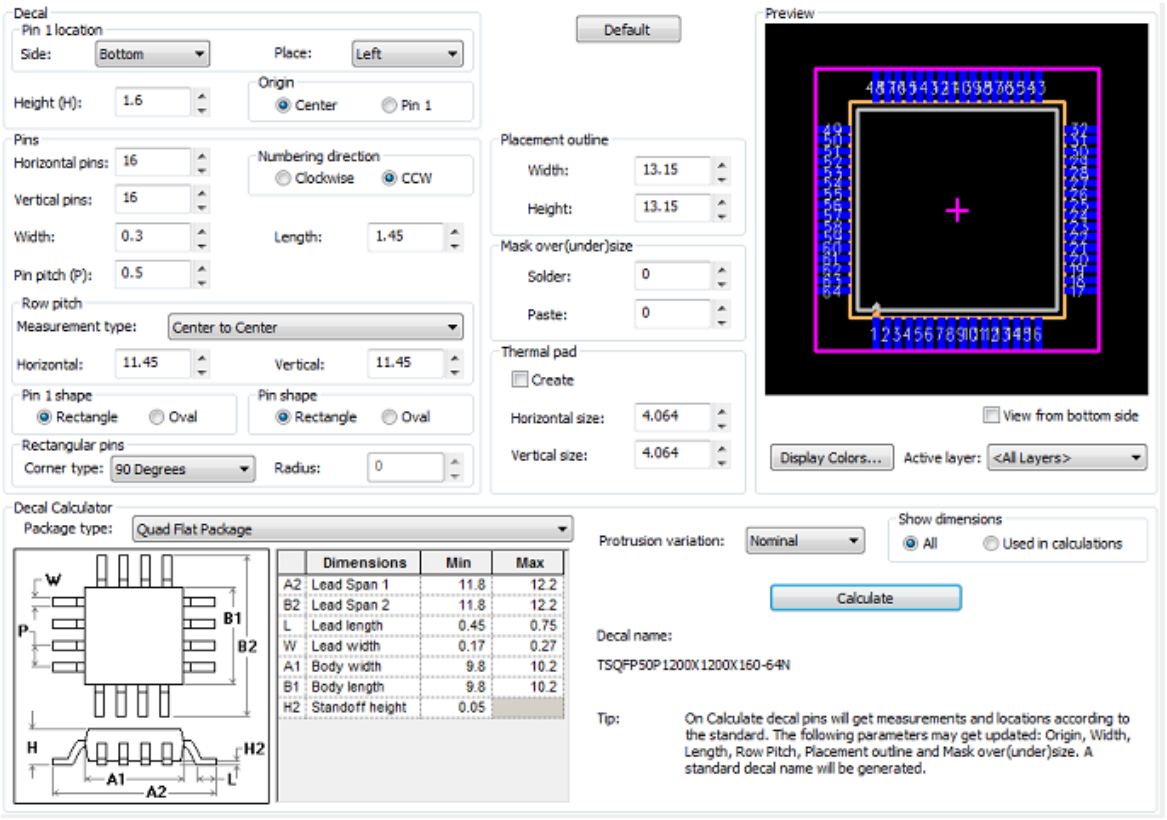


Figure 5. 64-Pin LQFP Footprint

Table 4. 64-Pin LQFP Footprint Dimensions

Designator	Description	Size
A	Pad Pitch	0.5 mm / 19.89 mil
B	Pad Width	0.3 mm / 11.81 mil
C	Pad Length	1.45 mm / 57.09 mil
D	Horizontal Row Pitch (Pad Center to Pad Center)	11.45 mm / 405.79 mil
E	Vertical Row Pitch (Pad Center to Pad Center)	11.45 mm / 405.79 mil
F	Solder Mask Oversize is dependent on fab capabilities and tolerances	0 mm / 0 mil to 0.08 mm / 3.15 mil
G	Solder Paste Oversize	0 mm / 0 mil

3.3 PCB Stack-up and Trace Impedance

An important component of any layout is determining what PCB stack-up to use. The PCB stack-up configuration determines several elements of the design:

- Number of layers available for routing
- Number of layers available for power and ground planes
- Single-ended trace impedance, capacitance per inch and propagation delay per inch of a trace of a particular width. These factors are important for longer trace lengths (typically longer than 6 inches) on critically timed interfaces or on interfaces that are near the maximum capacitive load.
- Trace width and spacing required to achieve the differential impedance targets for USB and Ethernet connections

3.3.1 Four-Layer Stack-up

A four-layer stack-up (two signal layers, two power planes) is recommended for most designs. A four-layer stack-up has the following benefits:

- A solid ground plane reference for USB signals that have a specific impedance target
- Low-impedance power and ground connections to components and decoupling capacitors through the planes
- High-speed signals have lower impedance, smaller propagation delay and more immunity to crosstalk due to the closer distance to the reference plane on a four-layer design as compared to a two-layer design
- Analog signals have more immunity to crosstalk, and the analog modules in the device can provide higher precision results when used with the solid ground plane reference that a four-layer stack-up provides

A typical configuration for an FR-4, 0.062 in (1.5748 mm) circuit board with four layers of 1-oz copper is shown in Figure 6.

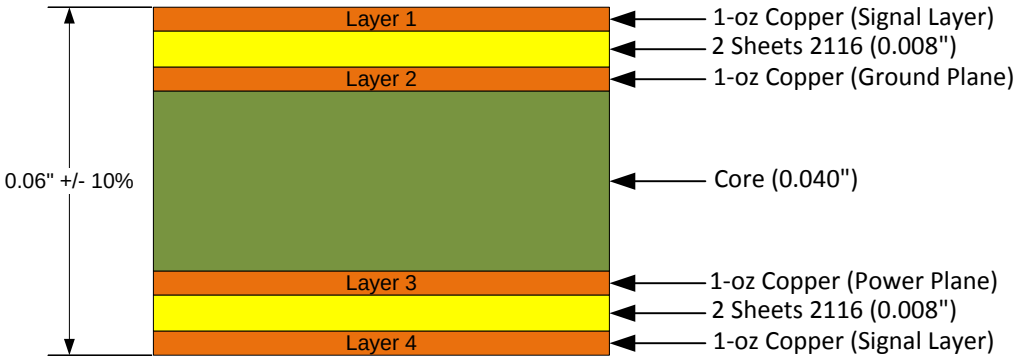


Figure 6. Typical Four-Layer PCB Stack with Routing Assignments

For this example, we place a solid ground plane on layer 2 and a power plane on layer 3. The outer signal layers each consist of 1/2-oz base copper with 1/2-oz plating to total 1-oz copper. Each 1-oz copper layer is 1.4 mils (.0014 in, or 0.0355 mm) thick. The height of traces above the ground plane is defined by the thickness of the PCB prepreg material—in this case, 0.008 in (0.2032 mm) thick. Therefore, total thickness is:

Total thickness = 0.062 in = 4 x 0.0014 in + 0.040 in + 2 x 0.008 in (1)

3.3.2 Two-Layer Stack-up

A two-layer stack-up may be acceptable given the following considerations:

- No timing-sensitive high-speed interfaces are being used
- USB is either not being used on the design or the distance to connectors is short
- The design allows for adequate power and ground routing with good decoupling placement and ESD protection

A typical configuration for an FR-4, 0.062 in (1.5748 mm) circuit board with two layers of 1-oz copper (no plating) is shown in Figure 7.

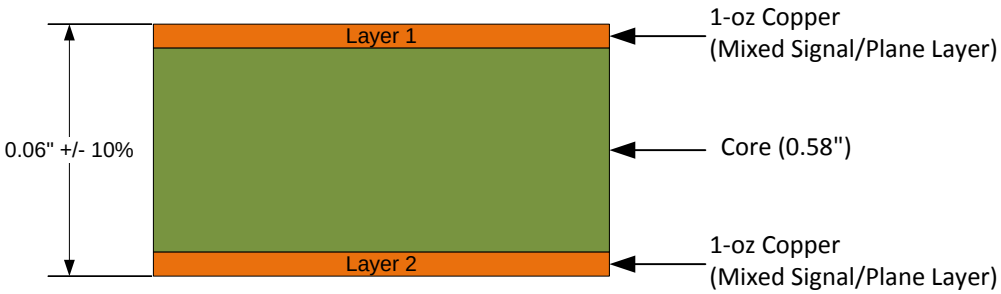


Figure 7. Typical Two-Layer PCB Stack with Routing Assignments

For this example, the top and bottom layers are used for both signal routing and copper power floods. The 1-oz copper mixed plane is 1.4 mils (.0014 in, or 0.0355 mm) thick. The height of traces above any ground pour is defined by the thickness of the PCB core material—in this case, 0.058 in (1.4732 mm) thick. Therefore, total thickness is:

Total thickness = 0.061 in = 2 x 0.0014 in + 0.058 in (2)

3.3.2.1 Six-Layer Stack-up

Stack-ups greater than four layers can be used if desired for high density designs.

A typical configuration for an FR-4, 0.062 in (1.5748 mm) circuit board with six layers of 1-oz copper (no plating) is shown in Figure 8.

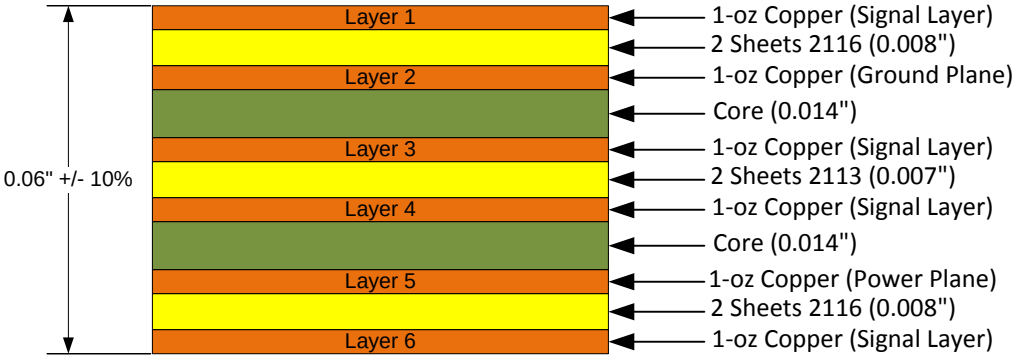


Figure 8. Typical Six-Layer PCB Stack with Routing Assignments

For this example, we place a solid ground plane on layer 2 and a power plane on layer 5. The 1-oz copper planes are 1.4 mils (.0014 in, or 0.0355 mm) thick. The height of traces on the outer layers (1, 2) above the planes is defined by the thickness of the PCB prepreg material—in this case, 0.008 in (0.2032 mm) thick. The height of the traces on the inner layers (3, 4) above the planes is defined by the thickness of the PCB core material--in this case, 0.040 in (1.016 mm) thick. In between layers 3 and 4 is additional prepreg material---in this case, 0.007 in (0.1778 mm) thick. Therefore, total thickness is:

Total thickness = 0.0594 in = 6 x 0.0014 in + 2x 0.008 + 2x 0.014 in + 0.007 in (3)

There are some additional routing considerations for the internal layers (3 and 4) when using a six-layer stack-up:

- These internal layers (3 and 4) are considered asymmetric stripline relative to the Ground and Power plane (layers 2 and 5). Refer to Figure 9. The calculations for impedance of traces on these layers are different than layers 1 and 6.
- Generally traces on layers 3 and 4 are higher in capacitance per inch and have a higher propagation delay
- Traces on layers 3 and 4 can impact each other via crosstalk if they are run parallel and over each

other.

- Traces on layers 3 and 4 are better shielded from external EMC radiation or interference because they are shielded by the power and ground planes.

3.3.3 Trace Properties: Impedance, Inductance, Capacitance, Propagation Delay

Impedance (Z_O), Capacitance per inch (C_O), Inductance per inch (L_O) and Propagation Delay (T_{PD}) are all important considerations when routing high-speed signals and low-impedance power nets. Differential trace impedance is important for USB differential signals. All of these properties are dependent on the trace width used (W), distance away from the reference plane (H), thickness of the trace (T) and relative permittivity of the dielectric (E_R), see Table 5. Differential impedance is also significantly affected by the distance between the differential traces (S).

Some PCB design tools have an integrated trace impedance calculator that factors in trace geometry, trace length, board stack-up, and the board material dielectric constant. Several free programs are also available that can perform similar calculations. The Saturn PCB Toolkit from Saturn PCB Design, Inc is an example of one of these free programs that has been used for most of the impedance calculations in this document.

3.3.3.1 Single-ended Trace Impedance

The first step in calculating these single-ended trace properties is to identify the transmission line type of the trace. The Microstrip transmission line type as shown in Figure 9 is most common on two-layer and four-layer boards as well as layers 1 and 6 of six-layer boards. The Asymmetric Stripline transmission line type is most common on layers 3 and 4 of six-layer boards.

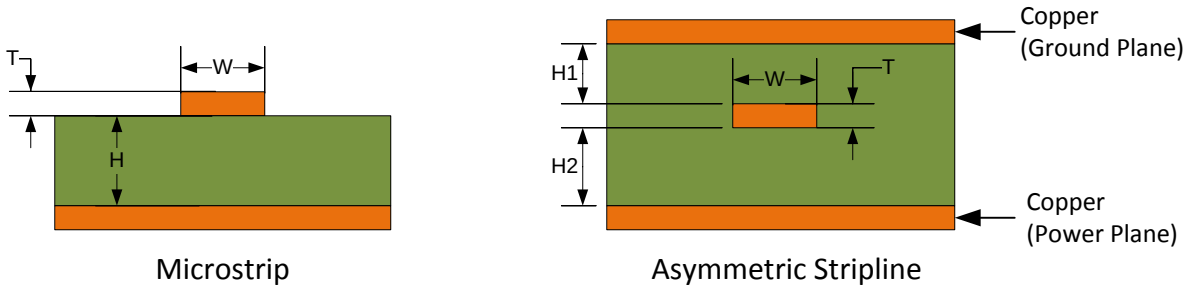


Figure 9. Transmission Line Type

The typical dielectric constant (E_R) for FR-4 material is about 4.3. The following examples use this parameter as well as the stack-ups defined in Section 3.3 to generate some typical PCB geometries. They are intended as starting points for PCB designs. You should repeat the calculations for your own design because even small changes in the PCB stack-up can significantly change the impedance.

Table 5. Single-ended Trace Properties by Width and Stack-up

Configuration and Layer	W (mil)	T (mil)	H, H1 (mil)	H2	E_R	Z_O (Ohms)	C_O (pF/in)	L_O (nH/in)	T_{PD} (ps/in)	Notes
Four-layer (1,4) Six-layer (1,6)	4	1.4	8	N/A	4.3	85.26	1.64	11.90	139.58	4 mil trace and space rules (0.8 mm routing rules) can be used to route I/O signals from the BGA package. This trace width can also be used to route I/O signals from the QFP packages.
Six-layer (3,4)	4	1.4	14	22.4	4.3	82.03	2.14	14.42	175.74	4 mil trace impedance of asymmetric stripline on internal layers 3 and 4 of a six-layer board. Note: H1, H2 results in similar impedance to outer layers but higher capacitance and propagation delay.
Two-layer (1)	4	1.4	58	N/A	4.3	N/A	N/A	N/A	N/A	4 mil traces are generally not applicable to two-layer designs and are outside the constraints of the PCB calculator used.

Table 5. Single-ended Trace Properties by Width and Stack-up (continued)

Configuration and Layer	W (mil)	T (mil)	H, H1 (mil)	H2	E_R	Z_O (Ohms)	C_O (pF/in)	L_O (nH/in)	T_{PD} (ps/in)	Notes
Four-layer (1,4) Six-layer (1,6)	5	1.4	8	N/A	4.3	79.42	1.76	11.09	139.58	5 mil trace and space rules can be used to route I/O signals from the QFP packages. These rules result in a slightly lower impedance but higher capacitance than 4 mil traces.
Six-layer (3,4)	5	1.4	14	22.4	4.3	76.82	2.29	13.50	175.74	5 mil trace impedance of asymmetric stripline on internal layers 3 and 4 of a six-layer board. Note: H1, H2 results in similar impedance to outer layers but higher capacitance and propagation delay.
Two-layer (1)	5	1.4	58	N/A	4.3	N/A	N/A	N/A	N/A	5 mil traces are generally not applicable to 2 layer designs and are outside the constraints of the PCB calculator used.
Four-layer (1,4) Six-layer (1,6)	7	1.4	8	N/A	4.3	69.98	1.99	9.77	139.58	7 mil trace and space rules can be used to route I/O signals from the QFP packages. 7 mil trace width is recommended for routing I/O signals from the QFP packages when space is available.
Six-layer (3,4)	7	1.4	14	22.4	4.3	68.67	2.56	12.07	175.74	7 mil trace impedance for the internal layers using asymmetric stripline.
Two-layer (1)	7	1.4	58	N/A	4.3	142.10	0.98	18.83	139.58	7 mil trace and space rules are recommended for routing I/O signals from the QFP packages on two-layer boards.
Four-layer (1,4) Six-layer (1,6)	10	1.4	8	N/A	4.3	59.24	2.36	8.27	139.58	10 mil wide traces are recommended for routing to power and ground pins of the QFP packages and the decoupling capacitors.
Six-layer (3,4)	10	1.4	14	22.4	4.3	59.69	2.94	10.49	175.74	10 mil trace impedance for the internal layers using asymmetric stripline.
Two-layer (1)	10	1.4	58	N/A	4.3	131.37	1.06	18.34	139.58	10 mil wide traces are recommended for routing to power and ground pins of the QFP packages and the decoupling capacitors.
Four-layer (1,4) Six-layer (1,6)	12	1.4	8	N/A	4.3	53.52	2.61	7.47	139.58	12 mil wide traces may be used for Ethernet differential signals. This row shows the single-ended characteristics of this trace width. Refer to Table 6 for the differential impedance.

3.3.3.2 Differential Trace Impedance

The USB interface has critical differential impedance requirements. The USB signal pair should be routed as a 90Ω +/- 10% differential pair on the top layer of the PCB with a ground plane as a reference. When possible, a single-ended impedance that is half of the differential impedance should be targeted to determine the initial trace width.

The optimal way to achieve a specific differential impedance is a two-step process. During PCB layout, the designer should use PCB tools to set the spacing and width of the traces to get close to the target characteristic impedance.

The second step is performed by the PCB fab house as they adjust the trace space and width to match their specific materials and process.

NOTE: The PCB fab notes should include annotations that specify which traces are to be *impedance controlled*.

Another key benefit of specifying controlled impedance is that the PCB manufacturer assumes on-going responsibility for maintaining the impedance of those traces. This stipulation can be a factor when lot-to-lot differences introduce variation.

While specifying controlled impedance is preferred, it may be acceptable not to if the trace length is less than approximately 2 in (50.8 mm). If good design rules are followed during layout, it should be possible to achieve routing that provides good signal integrity.

A slight variation of this method, which also avoids the additional cost of controlled-impedance PCBs, is sometimes called *controlled dielectric*. This approach involves the PCB designer using a dielectric specification that is either supplied or agreed to by the board fab house. The material and dielectric constant should be added to the PCB fab notes.

The differential impedance calculations use the Microstrip differential transmission line type as with a ground reference plane as shown in Figure 10.

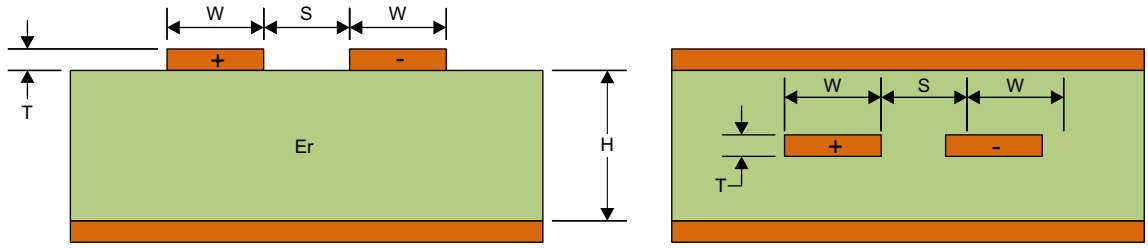


Figure 10. Differential Transmission Line Types

Table 6. Differential properties by width and stack-up

Configuration and Layer	W (mil)	T (mil)	H (mil)	S (mil)	E_R	Z_{DIFF} (Ohms)	Z_O (Ohms)	Notes
Four Layer or Six Layer	12	1.4	8	24	4.3	104.1	53.5	The Saturn PCB Toolkit was used to calculate the layer 1 trace width and spacing for a 100Ω +/- 10% differential impedance trace with a 50Ω +/- 10% single-ended impedance target using the stack-ups defined in Figure 6 and Figure 8.
Two Layer (1)	30	1.4	58	7	4.3	107.84	94.19	The Saturn PCB Toolkit was used to calculate the layer 1 trace width and spacing for a 100Ω +/- 10% differential impedance trace using the stack-up defined in Figure 7. A single-ended impedance target of 50Ω +/- 10% is not realistic with this stack-up.
Four Layer or Six Layer	15	1.4	8	24	4.3	90.1	46.3	The Saturn PCB Toolkit was used to calculate the layer 1 trace width and spacing for a 90Ω +/- 10% differential impedance trace with a 45Ω +/- 10% single-ended impedance target using the stack-ups defined in Figure 6 and Figure 8.
Two Layer	48	1.4	58	7	4.3	90.2	78.82	The Saturn PCB Toolkit was used to calculate the layer 1 trace width and spacing for a 90Ω +/- 10% differential impedance trace using the stack-up defined in Figure 7. A single-ended impedance target of 45Ω +/- 10% is not realistic with this stack-up.

NOTE: The PCB fab house knows their process and materials the best. They should be contacted to confirm stack-up heights, dielectric constant (E_R) and recommended trace widths and spacing for the targeted differential impedances.

The only way to guarantee the impedance target is met by the PCB manufacturer is to specify traces as *impedance controlled*.

3.4 General Layout Design Choices

There are a number of layout design choices that can affect PCB fabrication cost, assembly costs, and operational reliability. This section describes some of these choices and the thoughts behind them.

3.4.1 Trace Width and Spacing

Trace width and spacing impact the design in many ways. The minimum trace width and space on the PCB are two factors defining the cost of the PCB, and they are highly dependent on the capabilities of the PCB fab house. As a general guideline for low volume production, there is a cost increase for a minimum width/spacing less than 7 mils (0.1778 mm). A large number of PCB fab houses can produce boards with a minimum width/spacing of 4 mils (0.1016 mm) and a maximum 1-oz. finished copper weight on the outer layers. Another common minimum width/spacing capability point is 5 mil (0.1270 mm). These factors are some of the reasons behind the trace width choices in Table 5 and why 7-mil trace width/space is recommended for routing I/O signals from the QFP packages.

The BGA Package is denser and requires the 4 mil (0.1016 mm) trace and space rules to be able to route the I/Os from that package, refer to Section 3.4.3.

The routing of power and ground nets should be done with the wider, lower impedance traces wherever possible. Accordingly, trace width routes should be 10 mil (0.2540 mm) or wider from decoupling caps and for main power nets and 7 mil (0.1778 mm) or 10 mil (0.2450 mm) from the QFP power pins. For the BGA, it may be necessary to route using a 4 mil trace for a short distance until a wider 7 mil or 10 mil trace can be used.

When routing a signal that is going to be used as a fast edge rate clock, be sure to provide two times the spacing requirement from adjacent signals where possible to reduce crosstalk to and from the clock net. For example if routing with a 7 mil wide trace/space rule, make sure there is a 14 mil spacing between the clock and adjacent signals.

3.4.2 Via Sizes

PCB fab houses can vary in their capabilities for through-hole vias. Via size is often limited by the smallest mechanical drill diameter a PCB fab house uses. The minimum via pad size is usually required to be the drill size plus an additional adder. Drill size + 10 mil is quite common for a via pad size. Drill size + 8 mil and drill size + 12 mil are also common.

The amount of the adder is related to the IPC-6012 class of inspection requested by the customer and annular ring requirement of the customer. Boards fabricated and inspected with the IPC-6012 Class 2 requirement allow for one void per hole in not more than 5% of the holes. Boards fabricated and inspected with the IPC-6012 Class 3 requirements allow for no voids per hole. A PCB fab house usually requires a larger adder for Class 3 boards. A PCB fab house maintains a minimum annular ring, typically 1 mil, around each via hole, but the customer could choose to allow tangency where the hole is up to the edge of the pad but "breakout" has not occurred. This method can allow for a smaller diameter via pad if needed.

Table 7 lists some common via sizes along with some of characteristics calculated using the Saturn PCB Toolkit.

Table 7. Via Sizes and Properties

Via Type	Via Pad Size (mil)	Drill Size (mil)	Via Height (mil)	Ref Plane Opening Diam (mil)	E_R	Via Cap (pF)	Via Ind (nH)	Via Res (mOhms)	Via Impd (Ohms)	Notes
16D6	16	6	62	24	4.3	0.75	1.49	2.08	44.48	Small, lower capacitance but higher resistance via. Some PCB fab houses may not be able to accommodate this size. Useful for tight spaces and dense routes.
18D8	18	8	62	26	4.3	0.85	1.40	1.62	40.63	The largest via pad size (18mils) that can be used to break out route of the BGA package with 4 mil spacing. Pad size is 10 mils over drill size of 8.
18D9	18	9	62	26	4.3	0.85	1.36	1.46	40.01	The largest via pad size (18mils) that can be used to break out route of the BGA package with 4 mil spacing. Pad size is 9 mils over drill size of 9.

Table 7. Via Sizes and Properties (continued)

Via Type	Via Pad Size (mil)	Drill Size (mil)	Via Height (mil)	Ref Plane Opening Diam (mil)	E_R	Via Cap (pF)	Via Ind (nH)	Via Res (mOhms)	Via Impd (Ohms)	Notes
20D10	20	10	62	28	4.3	0.94	1.33	1.32	37.57	A standard via pad size (20 mils) that is 10 mils over the drill size of 10. Good for vias for power traces and general I/O traces. Achievable by a large number of PCB fab houses.
22D10	22	10	62	30	4.3	1.03	1.33	1.32	35.81	A standard via pad size (22 mils) that is 12 mils over the drill size of 10. Good for vias for power traces and general I/O traces. Achievable by an even wider number of PCB fab houses.

3.4.3 157-Ball BGA Escape routing

The populated balls on the 157-Ball BGA package (See Section 3.1.1) and the choice of their functions were arranged to allow all I/O signals to be routed from the BGA on a four-layer board (See Section 3.3.1) using 4 mil traces with 4 mil spacing. This section talks about how to route all I/O signals away from the BGA, also known as "Escaping the BGA" with the following considerations in mind:

- Standard process 4 mil trace/4 mil space and a via size, as indicated in Section 3.1.1, are the smallest needed to escape the BGA.
- The BGA can be routed using a minimum of a four-layer board with two routing layers on top and bottom, a ground plane and a power plane.
- The V_{DDC} and V_{DDA} nets are partially routed on the power plane.
- Required power routing and capacitor decoupling placement for all power rails can be achieved using 0402 sized capacitors.
- Routing of impedance-controlled traces is a priority.

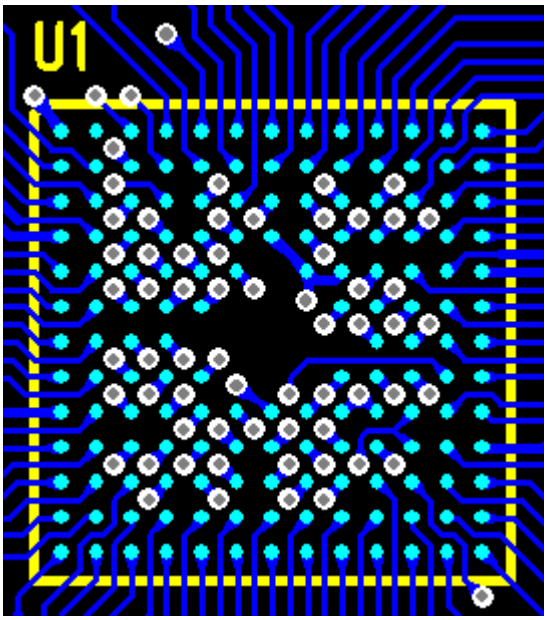


Figure 11. Top Layer 157-Ball BGA Escape Routing

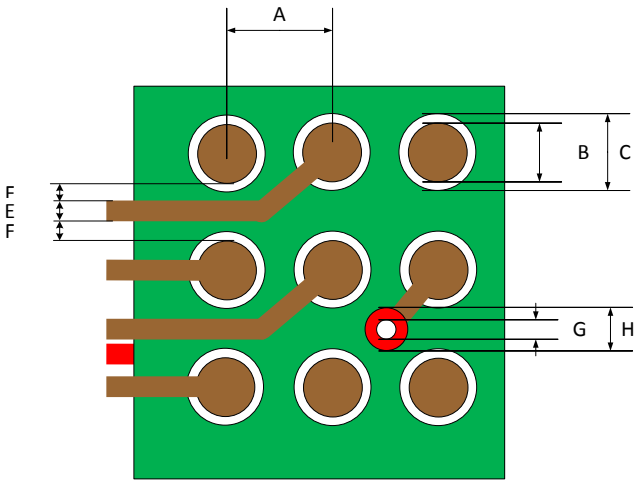


Figure 12. Escape Routing Through 157-Ball BGA

Figure 11 shows the recommended top layer routing pattern used to escape the BGA. The light blue dots are the BGA landing pads (Also shown as B in Figure 2). The white circles with black centers are vias.

Some things to note about Figure 11:

- For the outer two rows of balls, all signals route on the top layer to escape the BGA.
- Routing from the second row of balls between the first row of balls using a 0.1mm (4.0 mil) trace and spacing is possible as shown in Figure 12. Refer to Table 1 for pad and trace dimensions.
- With proper planning, a few select balls from the third row can be routed on the top layer as shown in Figure 11.
- All other balls require vias to the backside or power planes. The placement of the vias is important to enable all traces on the back side to escape and allow power and ground connections to the inner vias. See Figure 14. It may be necessary to use a very small grid spacing to align the vias with 4 mil spacing.
- The location of the vias in the center of the BGA allow for placement of two 0402 decoupling capacitors on the back side of the board directly under the BGA, as shown in Figure 14.
- Impedance controlled differential signals are routed with 0.1mm (4 mil) trace/spacing until they escape the perimeter of the BGA and can be routed with the desired trace width and spacing to meet the impedance target.
- All V_{DD}, V_{DDA}, GND, GNDA, VREFA+ and VREFA- signals are routed as 0.1524 mm (6 mil) traces within the BGA escape area wherever possible.
- All V_{DDC} balls are connected together with 0.2032 mm (8 mil) traces within the BGA escape area on the top layer and 0.254 mm (10 mil) or 0.508 mm (20 mil) traces on the power layer as shown in Figure 13.
- All other signals are routed as 1 mm (4 mil) traces within the BGA escape area.

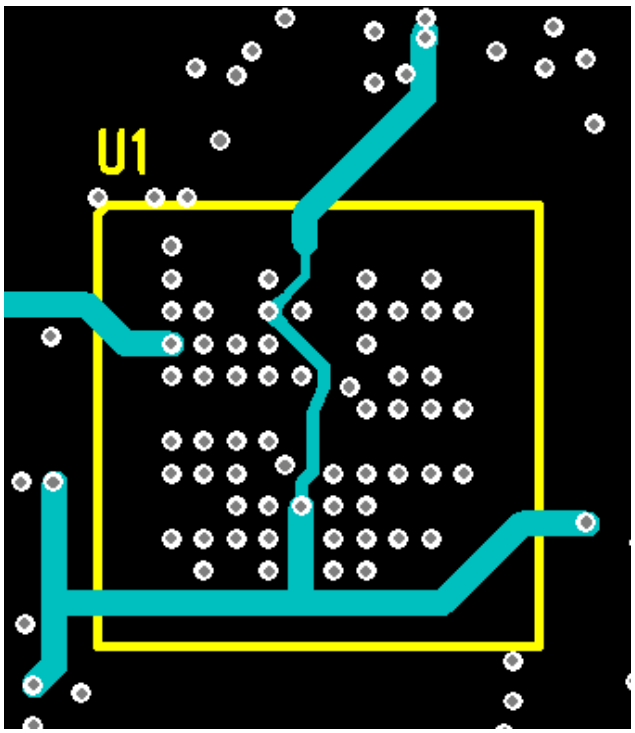


Figure 13. Power Layer 157-Ball BGA Escape Routing

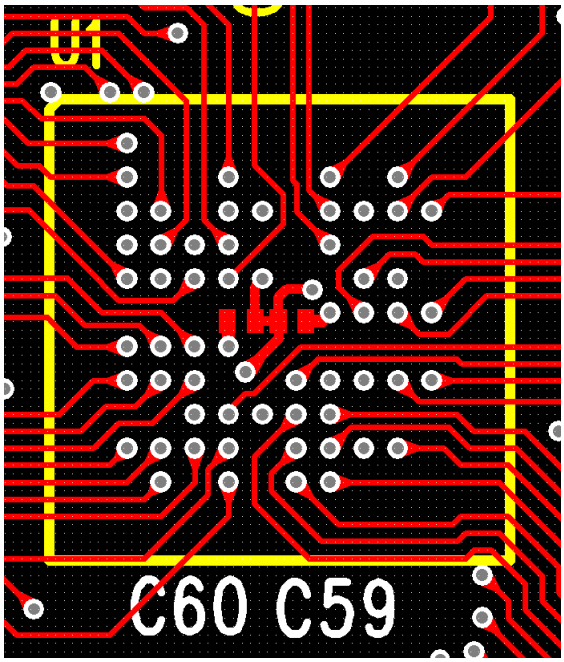


Figure 14. Bottom Layer 157-Ball BGA Escape Routing

Figure 13 shows the power layer routes of V_{DDC} and V_{DDA} nets. The rest of the layer is flooded around these traces with copper connected to the V_{DD} net.

Figure 14 shows the bottom layer escape routing under the BGA from the vias. In the center of the bottom layer are two 0402 sized 0.1µF decoupling capacitors connected between V_{DD} and GND.

3.4.4 PCB Design Rules: 90° PCB Traces

For many years, it has been common PCB design practice to avoid 90° corners in PCB traces. In fact, most PCB layout tools have a built-in miter capability to automatically replace 90° angles with two 45° angles.

The reality is that the signal-integrity benefits of avoiding 90° angles are insignificant at the frequencies and edge-rates seen in microcontroller circuits (even up to and past 1 GHz/100 ps). [Johnson, H and Graham, M, High-Speed Digital Design: a Handbook of Black Magic, Prentice Hall: New Jersey, 1993.]

Additionally, one report could find no measurable difference in radiated electromagnetic interference (EMI). [Montrose, Mark I, Right Angle Corners on Printed Circuit Board Traces, Time and Frequency Domain Analysis, undated.]

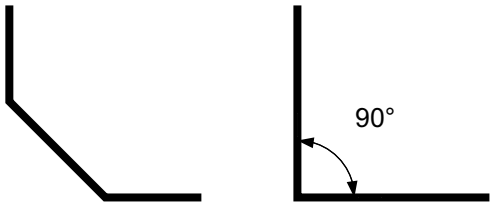


Figure 15. Acceptable PCB Trace Routing

NOTE: Loops in PCB traces are not acceptable, despite the references that indicate that the signal-integrity benefits of avoiding 90° angles is negligible. Loops in traces form antennas and add inductance. The data shows that if your layout does have antenna loops, then mitering the angles to 135° is not going to help. Avoid loops in PCB traces.

Despite these conclusions, there are a few simple reasons to continue to avoid 90° angles:

- There is a higher possibility of an acid-trap forming during etching on the inside of the angle (especially in acute angles). An acid trap causes over-etching which can be a yield issue in PCBs with small trace widths.
- Routing at 45° typically reduces overall trace length. This practice frees board area, reduces current loops, and improves both EMC emissions and immunity.
- It looks better. This consideration is an important factor for anyone who appreciates the art of PCB layout.

3.4.5 Copper Pours

While solid ground and power planes are highly desirable, small areas of copper pour should be used cautiously. It is often not a good idea to pour every available area on the routing layers of multi-layer boards. On one- and two-layer board designs, multiple pours might be necessary, because dedicated plane layers are not available.

If used, never leave small copper pours floating or unconnected. Isolated conductor areas can cause unwanted coupling and EMC problems if they act as antennae. Small copper pours should have solid connections to a ground net/trace. Ideally, use several vias to provide a low-impedance connection.

3.4.6 Chassis Ground

When properly designed, a chassis ground routed on the PCB can be a very effective feature for addressing a range of EMC challenges.

One specific benefit is improved electro-static discharge (ESD) immunity due to the provision of a safe discharge path that avoids sensitive circuitry in the center of the board.

In general, a chassis ground on the PCB works in conjunction with the overall enclosure to improve electro-magnetic emissions and especially immunity.

The chassis ground should be routed or poured copper around the perimeter of the PCB, ideally on all layers. If the ground is not present on all PCB layers, then other layers should be pulled back from the chassis ground to avoid coupling. The chassis ground should not route over the top of any power or ground layer.

Typically, the chassis ground should have a break or void in it to prevent loops that could cause loop antenna effects. However, depending on the size of the board, enclosure design, and ground connection point locations, it might still be acceptable or preferable to have a continuous chassis ground around the board.

A chassis ground is particularly important in systems with external connectors, metal enclosures, or apertures in the enclosure (see Figure 16).

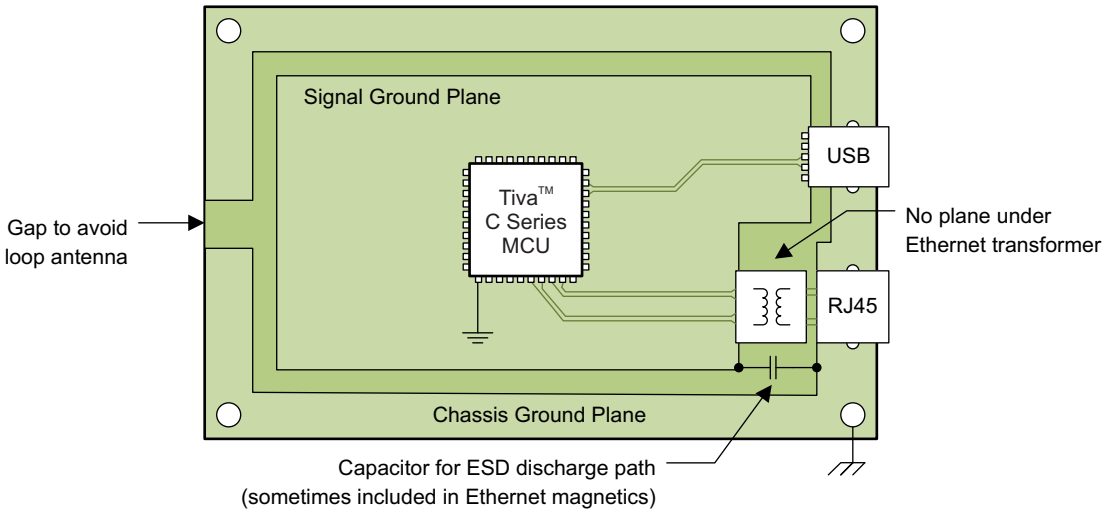


Figure 16. Chassis Ground Guidelines

3.4.7 Routing Across Plane Splits

Avoid discontinuities in ground planes and power planes under high-speed signals as shown in Figure 17. For all signals, a break in the ground plane removes a direct path for any return current to flow through. This consideration is important even for balanced differential pairs because perfect matching is seldom achievable and ground current is inevitable.

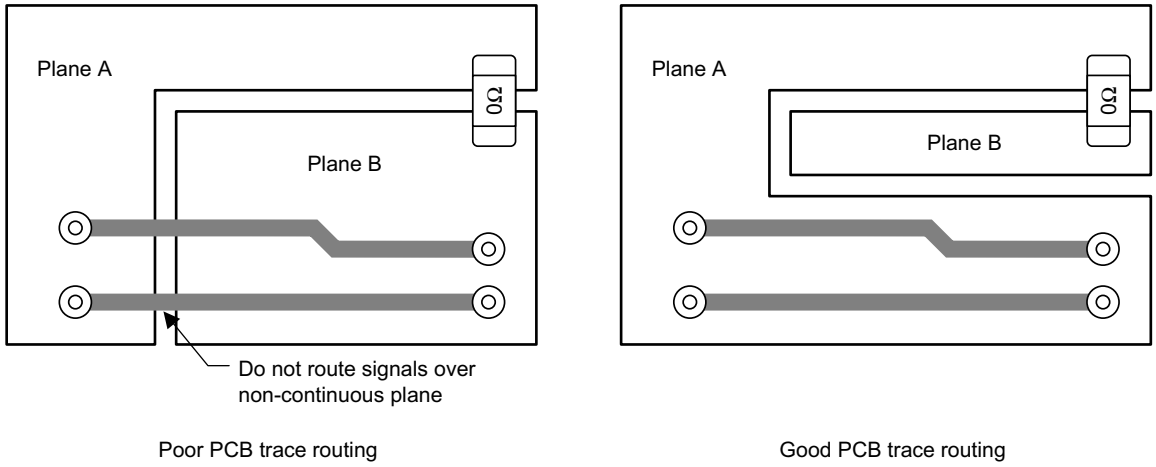


Figure 17. Examples of PCB Trace Layout

Tiva C Series microcontrollers provide programmable drive strength for all digital output pins. When initially bringing up the design, the drive strength for the output pins of a high-speed interface should be set to 8mA to avoid any marginal timing requirements associated with too low of a drive strength. However, if a signal is showing signal integrity issues such as ringing and reflections, the GPIO drive strength can be lowered to improve the performance as long as timing requirements are still met.

It is acceptable to route lower speed and slow edge rate signals such as the open collector I2C, UART signals and mostly static GPIOs across a plane split, however it is preferable to avoid this practice as it can be a source of EMI radiation due to the return current flow path.

3.4.8 Routing Differential Traces

- For each differential pair, the traces withing the pair should be run parallel to each other and be matched in length. Matched lengths minimize delay differences, avoiding an increase in common mode noise and increased EMI, as shown in Figure 18.
- It may be impossible to maintain parallelism immediately near the connector, ESD component or Tiva™ C series microcontroller. For these cases, minimize the distance the traces are not parallel and keep them localized near the start or endpoints of the traces.
- Ideally there should be no crossover or via on the signal paths. Vias present impedance discontinuities and should be minimized. Route an entire trace pair on a single layer if possible
- Choose ESD components in packages that support good differential routing of the signals they are protecting without the need for stubs or vias. Many packages have no-connect pins that allow routing of the differential signal through the protection circuit and a no-connect pin in order to maintain signal spacing.

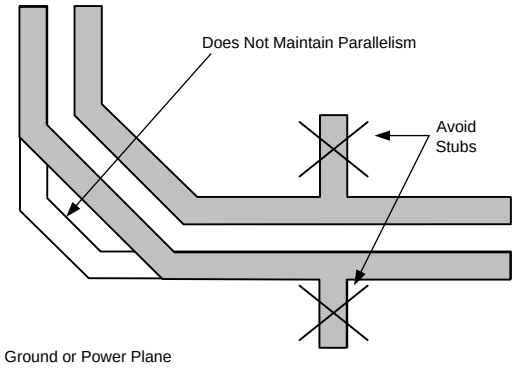


Figure 18. Differential Signal Pair

- Avoid stubs in differential signal pairs where possible, as shown in Figure 18 and Figure 19. Where termination or bias resistors are needed, one terminal should be located directly on the trace. Both resistors should be located at the same distance from the source and load.

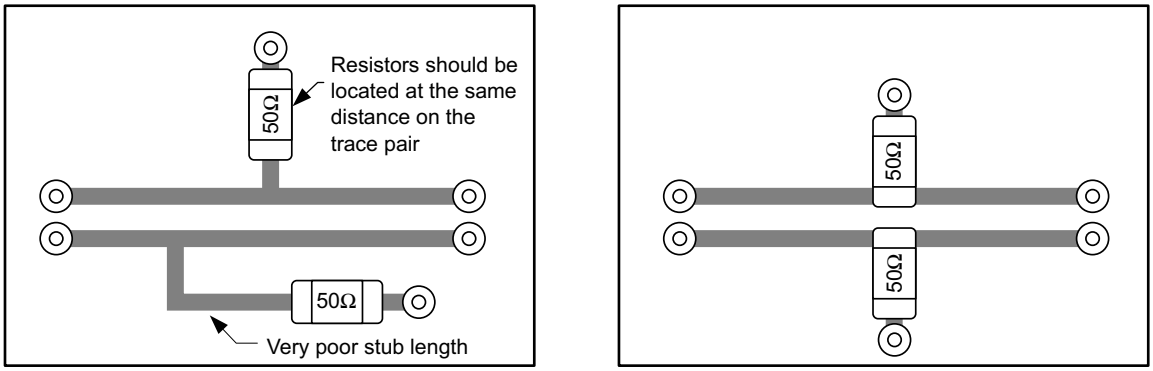


Figure 19. Examples of Differential Pair Layout

- PCB trace lengths should be kept as short as possible.

- Differential signal traces should not be run such that they cross a plane split, as shown in Figure 20. A signal crossing a plane split may cause unpredictable return current paths, resulting in an impedance mismatch, which can impact signal quality and potentially create EMI problems.

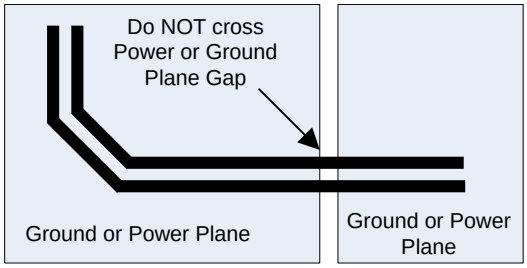


Figure 20. Differential Signal Pair-Plane Crossing

3.5 Power

This section describes design considerations related to the microcontroller power supply.

3.5.1 Microcontroller Power Supply

Tiva C Series microcontrollers require only a single +3.3V power supply connected to V_{DD} and V_{DDA}. Other supply rails are generated internally by on-chip, low drop-out (LDO) regulators. The most visible internal supply rail is the core voltage (V_{DDC}) because it has dedicated power pins for filter and decoupling capacitors.

During normal microcontroller operation, the power-supply rail must remain within the electrical limits listed in the microcontroller data sheet [V_{DD} (min) and V_{DD} (max)]. For optimal performance of the on-chip analog modules, the supply rail should be well regulated and have minimal ripple. Electrical noise sources such as motor drivers, relays, and other power-switching circuits should each have a separate supply rail, especially if analog-to-digital converter (ADC) performance is a factor.

The microcontroller has analog power-on reset (POR) and power-OK (POK) circuits that release and assert once the V_{DDA} power-supply rails reach specific thresholds. The microcontroller also has digital power-OK (POK) and brown-out reset (BOR) circuits that release and assert once the V_{DD} power-supply rails reach specific thresholds. Details on the operation and threshold levels of these circuits can be found in the data sheet for the part.

The supply connected to V_{DD} must accommodate a short period (40µSec to 60µSec) of additional inrush current that occurs as the decoupling capacitors connected to the LDO on the V_{DDC} rail charge up to the V_{DDC} voltage level. Internal circuitry limits the inrush to the I_{INRUSH}(max) specified in the data sheet for the part. The supply connected to V_{DD} can self limit the current it supplies to something less than the maximum I_{INRUSH}, however that extends the period it takes to bring V_{DDC} up to operating voltage.

External supervisors may also be used to assert the external reset signal $\overline{RST}$ under power-on, brown-out, or watchdog expiration conditions.

3.5.2 LDO Filter Capacitor (V_{DDC})

All Tiva™ C Series microcontrollers have an on-chip voltage regulator to provide power to the core. The voltage regulator requires a filter capacitor to operate properly (see the C_{LDO} parameter in the corresponding microcontroller data sheet for acceptable capacitor value range).

The C_{LDO} capacitance is the sum of the capacitor values on the V_{DDC} pins. The recommended V_{DDC} capacitor solution, taking tolerance into account, consists of two or more 10%-tolerance ceramic chip capacitors totaling 3.3µF to 3.4µF (examples are, one each of 3.3µF and 0.1µF capacitors or one each 2.2µF, 1.0µF and 0.1µF). Z5U dielectric capacitors are not recommended due to wide tolerance over temperature.

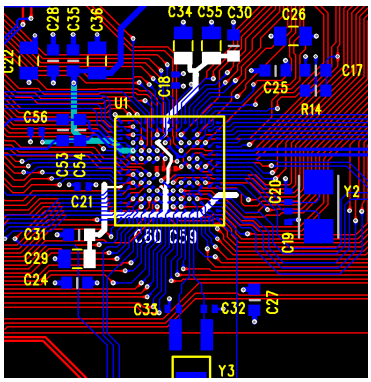
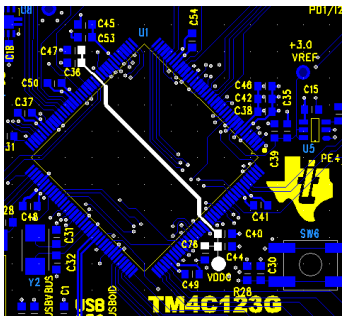
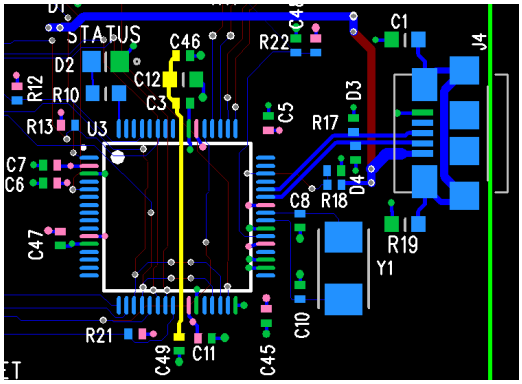
The following recommendations should be followed when placing and routing the capacitors connected to V_{DDC}.

- The larger values of capacitance should be placed closest to the pin specified in the data sheet and the 0.1uF capacitor can be placed near the other V_{DDC} pins.
- The ESR Max Specification in the data sheet for C_{LDO} must be adhered to and should include any via and trace resistance from the pin or ball to the capacitors.
- All V_{DDC} pins should be routed together using wide traces for lower resistance.

See Table 8 for examples of recommended V_{DDC} routing and C_{LDO} capacitor placement. An example for routing of the V_{DDC} net on the 100-Pin LQFP package is not shown. The routing of the V_{DDC} net on the 100-Pin LQFP package is done similar to the other LQFP packages shown.

Each routing example shows a slightly different V_{DDC} routing trace width and capacitor placement. All are acceptable and show a short, low-impedance route of the V_{DDC} net.

Table 8. V_{DDC} Routing and Capacitor Placement for TM4C123x Devices

157-Ball BGA Package	144-Pin LQFP Package	64-Pin LQFP Package
		
• Highlighted trace is VDDC routed with 0.2032 mm (8 mil) trace on the top layers and 0.254 mm(10 mil) and 0.50 8 mm (20 mil) traces on the power layer. • Two 1.0uF and one 0.1uF capacitors placed closest to ball D6 • One 1.0uF and one 0.1uF capacitor placed on the VDDC net that connects to balls J1, K13, and J6	• Highlighted trace is VDDC routed with a 0.254 mm (10mil) trace from the pins necked up to 0.508 mm(20 mil) between pins 126 and 49. • Two 1.0uF and one 0.1uF capacitors placed closest to pin 126 • One 1.0uF and one 0.1uF capacitor placed closest to pin 49.	• Highlighted trace is VDDC routed with a 0.254 mm (10 mil) trace between pins 56 and 25. • 2.2uF, 1.0uF and 0.1uF capacitors placed closest to pin 56 • One 0.1uF capacitor placed closest to pin 25.

NOTE: V_{DDC} is an internally generated voltage rail. V_{DDC} should only be connected to the C_{LDO} filter capacitors. V_{DDC} should not be connected to any kind of external source or load.

3.5.3 Decoupling Capacitors

Ideally, Tiva™ C Series microcontrollers should have one decoupling capacitor in close proximity to each power-supply pin. Decoupling capacitors are typically 0.1 µF in value and should be accompanied by a bulk capacitor near the microcontroller. The combined V_{DD} and V_{DDA} bulk capacitance of the microcontroller is typically between 2 µF and 22 µF, with values on the upper end of that range providing measurable ripple reduction in some applications, especially if the circuit board does not have solid power and ground planes. Bulk capacitance is particularly important if the microcontroller is connected to high-speed interfaces or must source significant GPIO current (that is, greater than 4mA) on more than a few pins.

For optimal performance, locate one decoupling capacitor adjacent to each V_{DD} power and ground pin pair. At a minimum, there should be one decoupling capacitor on each side of the microcontroller package connected between V_{DD} and Ground.

V_{DDA}/GNDA and packages that support V_{REFA+}/V_{REFA-} have specific decoupling requirements as defined by C_{REF} in the data sheet. Refer to Section 3.5.5 for additional details.

Decoupling capacitors should be 6.3 V to 25 V, X5R/X7R ceramic chip types. Z5U dielectric capacitors are not recommended due to wide tolerance over temperature.

The capacitance of most ceramic capacitors decreases with increasing voltage. Avoid using capacitors at close to their rated voltage unless reduced capacitance is acceptable. X7R capacitors may lose 15%-20% of their capacitance at rated voltage while Y5V capacitors may drop 75%-80%. [(Cain, Jeffrey, Comparison of Multilayer Ceramic and Tantalum Capacitors, AVX Technical Bulletin.)]

Figure 21 shows different options for routing PCB traces between the Tiva C Series microcontroller power pins and a decoupling capacitor.

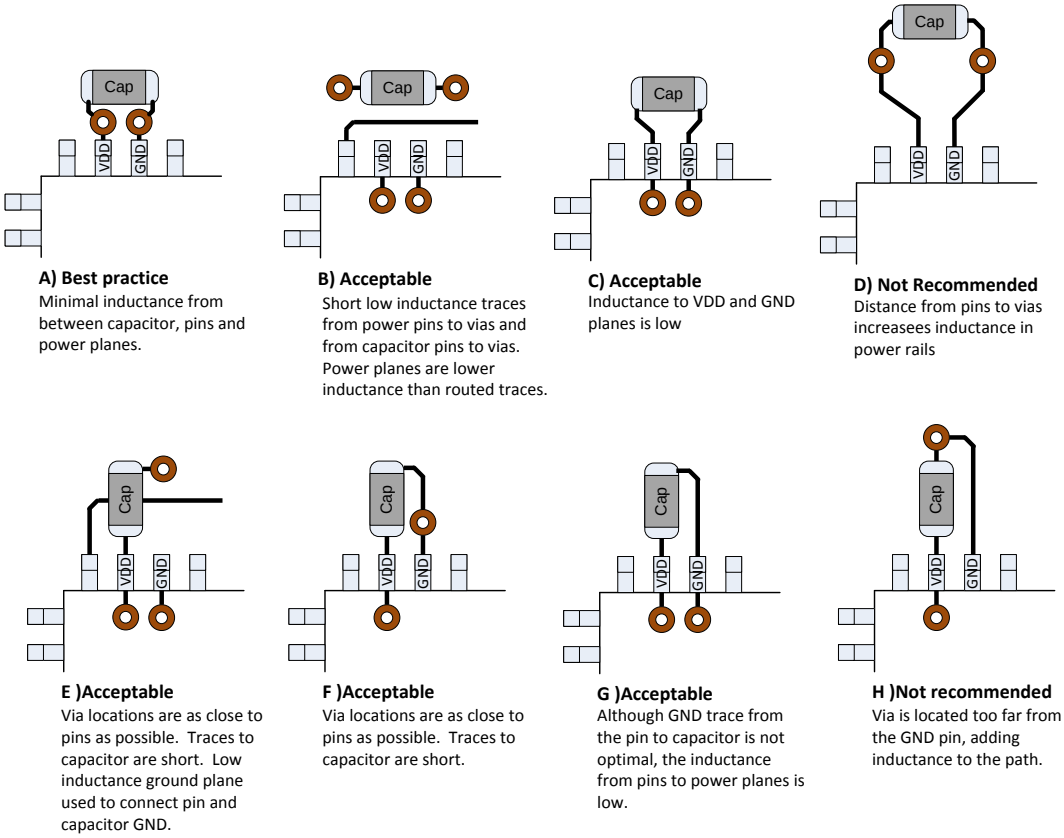
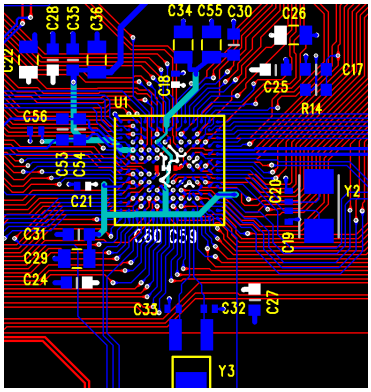
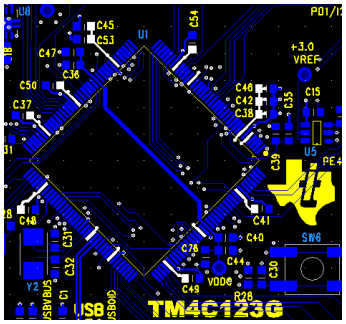
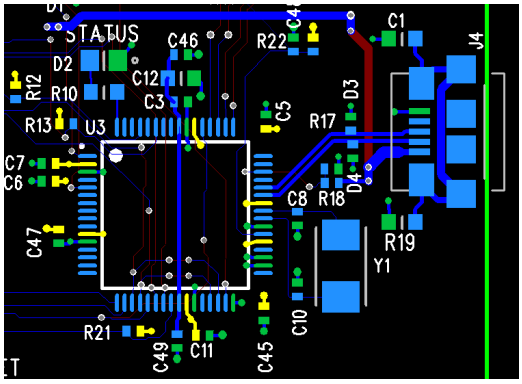


Figure 21. QFP PCB Routing Options

Table 9 shows recommended example placement and routing of the V_{DD} and V_{DDA} decoupling capacitors.

Table 9. V_{DD} Routing and Capacitor Placement Examples for TM4C123x Devices

157-Ball BGA Package	144-Pin LQFP Package	64-Pin LQFP Package
		
• The highlighted traces show the VDD net and decoupling cap locations. • Blue Traces and pads are on the top side. Red Traces and pads are on the bottom side. • Two decoupling caps are located on the back side directly under the BGA. • VDDA is routed as a separate net and decoupled with a 1uF, 0.1uF and a 0.01uF capacitor. See C36, C56, and C35 respectively.	• The highlighted traces show the VDD net and decoupling cap locations. • All components in this design are on the top side of the board. Bottom side traces are not shown. • There is at least one decoupling capacitor on each side of the chip. • VDDA is part of the VDD net and decoupled with a 1uF, 0.1uF and a 0.01uF capacitor. See C46, C42, and C38 respectively.	• The highlighted traces show the VDD net and decoupling cap locations. • Blue Traces and pads are on the top side. Red Traces and pads are on the bottom side. • All decoupling caps shown in this example are on the top side. • There is at least one decoupling capacitor on each side of the chip. • VDDA is part of the VDD net and decoupled with a 1uF, and 0.01uF capacitor. See C6 and C7 respectively.

3.5.4 Splitting Power Rails and Grounds

Tiva™ C Series microcontrollers are designed to operate with V_{DD} and V_{DDA} pins connected directly to the same +3.3V power source. Some applications may justify separation of V_{DDA} from V_{DD} to allow insertion of a filter to improve analog performance. Before deciding to split these power rails, the power architecture of the device should be reviewed to determine which on-chip modules are powered by each supply. The device data sheet contains a drawing that shows power architecture.

Filter options include filter capacitors in conjunction with either a low-value resistor or inductor/ferrite bead to form a low-pass filter.

If the V_{DD} and V_{DDA} pins are split, the designer must ensure that V_{DDA} power is applied before or simultaneously with V_{DD} and that V_{DDA} is removed after or simultaneously with V_{DD}.

If V_{DDA} is to be selected as a reference source for the ADC, the ADC will achieve better performance when powered with a separate V_{DDA} power rail and filtered with a 0.01uF and 1uF capacitor (C_{REF}) between V_{DDA} and GNDA.

The GND and GNDA pins should always be connected together—preferably to a solid ground plane or copper pour.

3.5.5 V_{REFA+}/V_{REFA-}

V_{REFA+} and V_{REFA-} can be selected to be the reference voltage for the ADC maximum and minimum conversion values.

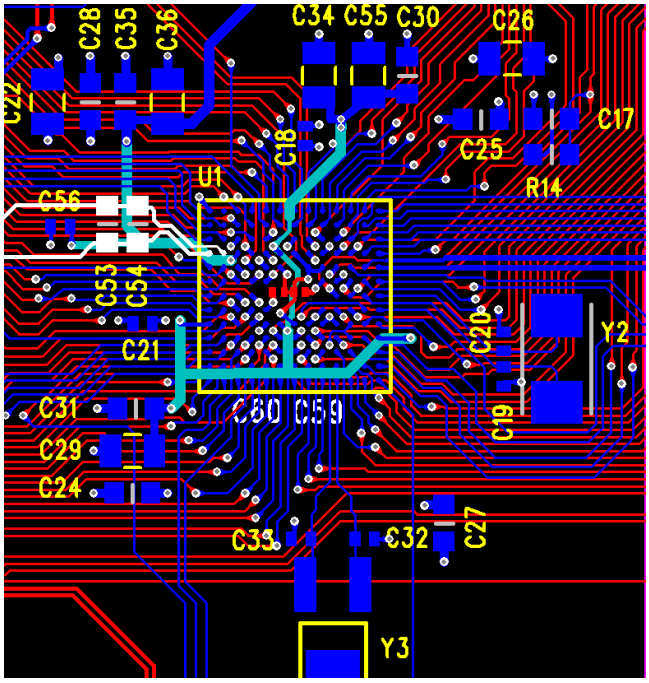
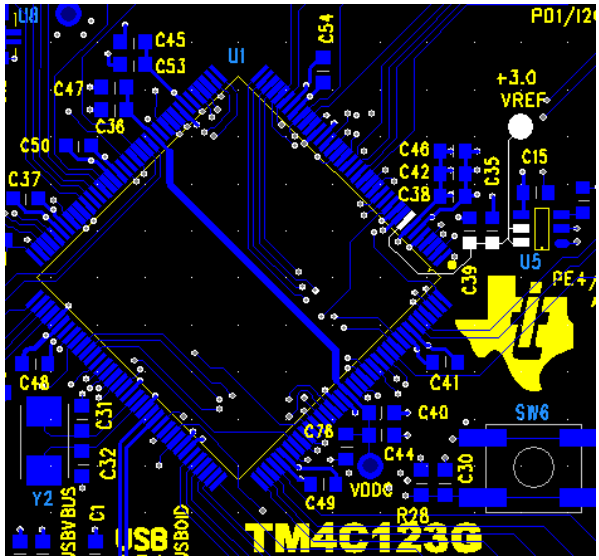
Some Tiva™ C Series parts have V_{REFA+} and V_{REFA-} brought out to dedicated pins and some parts do not have dedicated pins for V_{REFA+} or V_{REFA-}, and instead V_{REFA+} is internally connected to V_{DDA} and V_{REFA-} is internally connected to GNDA.

For designs that require high-precision ADC conversions and use MCUs that have dedicated V_{REFA+} or V_{REFA-} pins, should ensure that the references pins are connected to a high precision voltage reference. IF the ADC conversions are not required to be high precision, then V_{REFA+} should be externally connected to V_{DDA} and V_{REFA-} should be externally connected to GNDA.

NOTE: Do not leave V_{REFA+} or V_{REFA-} unconnected. V_{REFA+} must power up after or simultaneous to V_{DDA}.

For optimized ADC precision, V_{REFA+} should be supplied from a high-precision reference such as the TI REF3230. V_{REFA-} should be connected to GNDA and a 0.01uF and 1uF filter capacitor pair (C_{REF}) should be placed as close as possible to the V_{REFA+}/V_{REFA-} pins. The Enable and V_IN of the REF3230 should be driven from V_{DD} or V_{DDA} to ensure the correct power up sequence.

Table 10. Example V_{REFA+}/V_{REFA-} Routing and Capacitor Placement Examples for TM4C123x Devices

157-Ball BGA Package	144-Pin LQFP Package
	
• The highlighted traces are the is the VREFA+ and VREFA- nets. • C53 and C54 are the 1uF capacitor and 0.01uF capacitors required to filter the VREFA nets for highest performance. • In this example, VREFA- is a dedicated pin connected directly to GND at a point not shown in this image.	• The highlighted trace is the VREFA+ net • C35 and C39 are the 1uF and 0.01uF capacitors placed close to the device. • This device has VREFA- as a dedicated pin which is directly connected to GND on this design.

The 144-pin LQFP routing example for the V_{REFA+} and V_{REFA-} nets should be followed for the 100-Pin LQFP package, which is not shown in the table. The 64-pin LQFP package does not have dedicated V_{REFA+} or V_{REFA-} pins.

3.5.6 V_{BAT}

The TM4C123x family of devices supports a V_{BAT} supply for battery-backed RAM retention and RTC operations when the main VDD supply is not powered. V_{BAT} has a maximum ramp time, as specified in the data sheet as V_{BATRMP}. If V_{BAT} is to be driven from a coin cell battery or switched, an RC filter as shown in Figure 22 can be used adhere to the V_{BATRMP} rise time requirement.

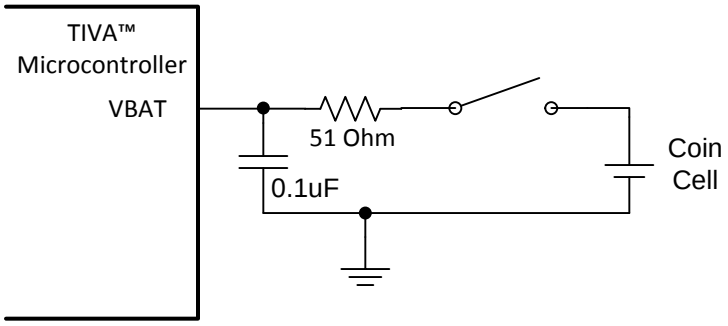


Figure 22. V_{BAT} RC Filter

If a dedicated battery is not going to be used, V_{BAT} can be connected to the same net driving the V_{DD} pins without adding the RC filter.

No dedicated decoupling is needed for the V_{BAT} pin.

NOTE: If a single-ended clock source is used to drive XOSC0 to the RTC/hibernation module, the voltage level of V_{BAT} impacts the acceptable XOSC0 input levels. Refer to the *HIB Oscillator Input Characteristics* in the data sheet.

3.6 Reset

This section describes design considerations related to reset.

3.6.1 External Reset Pin Circuits

A special external reset circuit is not normally required. Tiva C Series microcontrollers have an on-chip Power-On-Reset (POR) circuit with a delay to handle power-up conditions.

The $\overline{\text{RST}}$ input pin can be used to hold off initialization of the device if asserted prior to power on reset, or to create the equivalent of a power on reset if asserted after power has been applied. The input pin can be configured to perform either a system reset, power-on-reset, or a simulated full initialization. Refer to the *External RST Pin* section of the *System Control* chapter in the device data sheet for specific details.

The $\overline{\text{RST}}$ pin should never be left floating. It can be driven from a voltage supervisor or other control chip. It can be connected to an external RC combination or it can be pulled up using a 0 to 100K resistor connected to V_{DD}.

The $\overline{\text{RST}}$ pin input contains a glitch filter to prevent noise from causing a system reset.

The $\overline{\text{RST}}$ input pin is one of several device reset controls. Refer to the *System Control* chapter in the part data sheet for specific details.

Because the $\overline{\text{RST}}$ signal routes to the core as well as most on-chip peripherals, it is important to protect the $\overline{\text{RST}}$ signal from noise. This protection is particularly important in applications that involve power switching where fast transitions can couple into the reset line. The reset PCB trace should be routed away from noisy signals. Do not run the reset trace close to the edge of the board or parallel to other traces with fast transients.

If you choose to use a capacitor it should be located as close to the pin as possible.

If the $\overline{\text{RST}}$ signal source is another board, it is recommended to add a buffer IC on the Tiva C Series board to filter the signal.

A simple push-switch can be used to provide a manual reset. To protect against possible device damage due to electrostatic discharge and to avoid ringing on the $\overline{\text{RST}}$ signal caused by switch bounce and stray inductance, add a low-value resistor (100 Ω) in series with the switch.

Reset circuit options are shown in the microcontroller data sheets.

3.7 Crystal Oscillators

This section describes design considerations related to the microcontroller oscillators.

3.7.1 Crystal Oscillator Circuit Components

3.7.1.1 Main Oscillator Circuit

Tiva™ TM4C123x family of microcontrollers has a main oscillator circuit that can be used as a clock source for the device. This clock source is required for parts that contain and use the USB or CAN interfaces.

Some of the Tiva™ C family parts bring the GNDX2 signal of the main oscillator circuit out to a ball or pin on the part. When the GNDX2 signal is available, it should be connected to the digital ground plane as shown in Figure 23 for proper operation. Early designs may show the crystal load capacitors and GNDX2 pin connected only to each other without a connection to digital ground. Either is a valid configuration, however the low-impedance connection to the digital ground helps isolate the circuit from external system noise sources.

When the GNDX2 signal has not been brought out to a ball or pin, then it has been connected to a GND pin internally. These devices must be connected as shown in Figure 24.

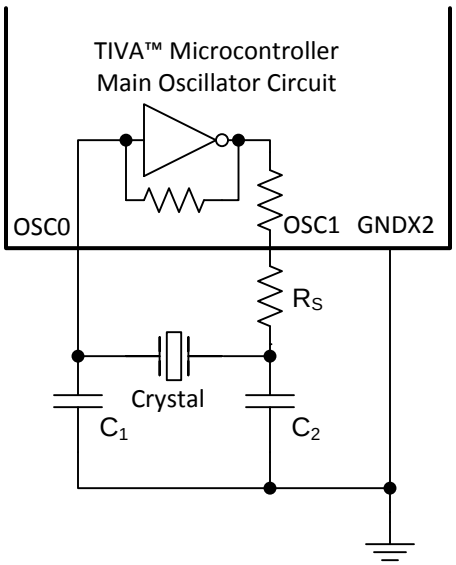


Figure 23. Main Oscillator Circuit with GNDX2

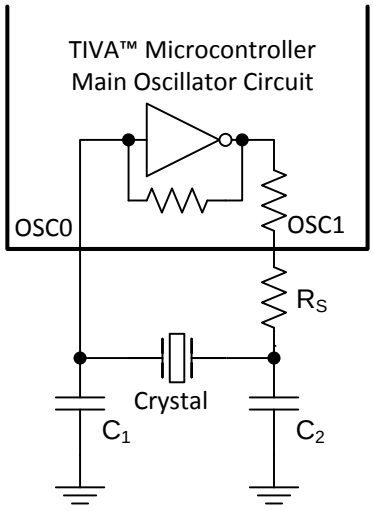


Figure 24. Main Oscillator Circuit without GNDX2

The device data sheet provides a list of recommended crystals that have been simulated to work with the main oscillator and includes recommended values for C_1, C_2 and R_S. It may be possible to substitute other manufacturer's crystals with like crystal parameters and frequencies. Crystals with C_L values of 18pF or greater or that support a maximum drive of less than 200µW are not robust enough to be used.

It is possible to use a single-ended clock source such as an external oscillator to drive the OSC0 input of the Main Oscillator Circuit. Refer to the device's data sheet for input specifications. When a single-ended clock source is used, the OSC1 pin should be left unconnected and GNDX2, if present, should be connected to GND.

3.7.1.2 Hibernate Oscillator Circuit

Some of the devices in the TM4C123x family have a hibernation module that runs from a 32.768-kHz clock source used to clock the Real Time Clock (RTC) circuit within the module accurate even when only V_{BAT} is supplied to the system. Refer to the device's data sheet for specifics on the Hibernation Module and the Hibernation Clock Source Specifications.

There are many readily available crystals that meet the Hibernation Clock Source Specification in the data sheet so there is no need to provide a specific recommended list.

Some of the Tiva™ C family parts bring the GNDX signal of the hibernate oscillator circuit out to a ball or pin on the part. When the GNDX signal is available, it should be connected to the digital ground plane as shown in Figure 25 for proper operation. Early designs may show the crystal load capacitors and GNDX pin connected only to each other without a connection to digital ground. Either is a valid configuration, however the low-impedance connection to the digital ground helps isolate the circuit from external system noise sources.

When the GNDX signal has not been brought out to a ball or pin, then it has been connected to a GND pin internally. For this configuration, implement the circuit shown in Figure 26.

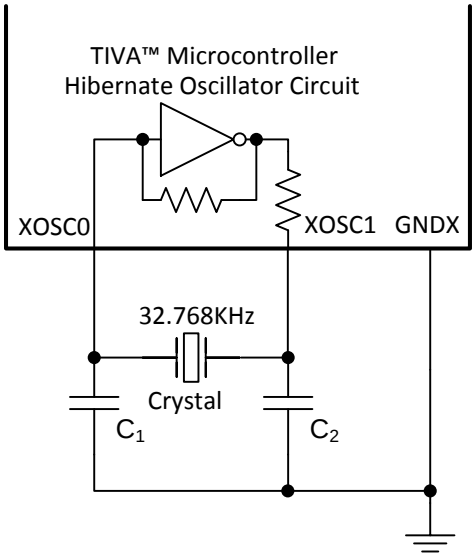


Figure 25. Hibernate Oscillator Circuit with GNDX

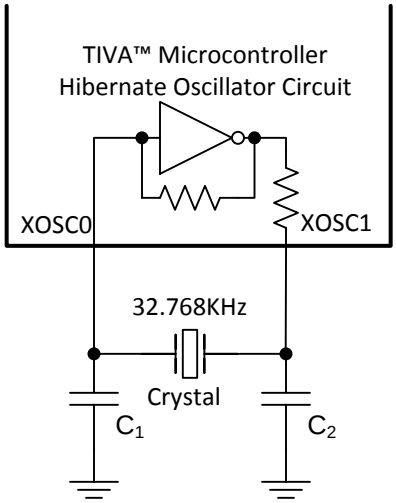


Figure 26. Hibernate Oscillator Circuite without GNDX

Capacitors C_1 and C_2 must be sized correctly for reliable and accurate oscillator operation. Crystal manufacturers specify a load capacitance (C_L) which should be used in the following formula to calculate the optimal values of C_1 and C_2.

$$C_L = (C_1 * C_2) / (C_1 + C_2) + C_S \quad (4)$$

C_S is the stray capacitance in the oscillator circuit. Stray capacitance is a function of trace lengths, PCB construction, and microcontroller pin design. For a typical design, C_S should be approximately 2pF to 4pF. Because C_1 and C_2 are normally of equal value, the calculation for a typical circuit simplifies slightly to:

$$C_1 \text{ and } C_2 = (C_L - 3pF) * 2 \quad (5)$$

C_1 and C_2 should stay within the maximum and minimum specifications listed in the *Hibernation Clock Source Specifications* section of the data sheet for the part. Capacitors with an NP0/C0G dielectric are recommended and are almost ubiquitous for small-value ceramic capacitors.

It is possible to use a single-ended clock source such as an external oscillator to drive the XOSC0 input of the Hibernate Oscillator Circuit. Refer to the device's data sheet for input specifications. When a single-ended clock source is used, the XOSC1 pin should be left unconnected and GNDX, if present, should be connected to GND.

3.7.2 Crystal Oscillator Circuit Layout

The key layout objectives should be to minimize both the loop area of the oscillator signals and the overall trace length. A poor oscillator layout can result in unreliable or inaccurate oscillator operation and can also be a noise source. Ideal trace length is less than 0.25 in or 6 mm. Do not exceed 0.75 in or 18 mm.

Figure 27 shows a preferred layout for a small surface-mount crystal. The GND side of each capacitor routes directly to a via that provides a low-impedance connection to the GND plane.

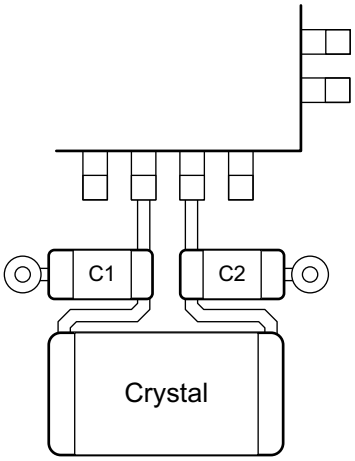


Figure 27. Recommended Layout for Small Surface-Mount Crystal

Some crystal circuits require a series resistor R_S in order to limit drive power delivered to the crystal. This component should be a small chip resistor located between capacitor C_2 and the OSC1 pin of the device.

Figure 28 shows a recommended layout for a small surface-mount crystal for a device that contains a GNDX pin between the XOSC0/XOSC1 signals. The GND side of each capacitor can share the via with the GNDX pin using a 10 mil wide trace to provide a low-impedance connection to the GND plane. If the distance between capacitors and the GNDX pin is greater than 200 mils, each should have their own via to GND.

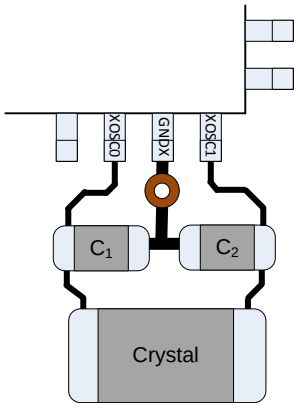


Figure 28. Recommended Layout for Crystal with GNDX Connection

3.8 JTAG Interface

This section describes design considerations related to the microcontroller JTAG interface.

3.8.1 Debug and Programming Connector

When designing a board that uses a Tiva™ C Series microcontroller, it is preferable to provide connections to all JTAG/SWD signals. In pin-constrained applications, SWD can be used instead of JTAG. SWD only requires two signals (SWCLK and SWDIO), instead of the four signals that JTAG requires, freeing up two additional signals for use as GPIOs. Check that your preferred tool-chain supports SWD before choosing this option. The LM Flash Programmer utility can program devices using SWD.

The most common ARM® debug connector is a 2x10-way, 0.1 in pitch header. Although it is robust, the 0.1 in header is too large for many boards and is considered legacy implementation. An alternate connector definition, which is now quite popular, uses a 0.05-in, half-pitch 2x5 connector known as the Cortex Debug Connector. The applicable assignments for both connectors are shown in Table 11.

Table 11. Applicable Debug Connector Pin Assignments

JTAG/SWD Signal	Legacy ARM 20-pin (0.1 in pitch)	Cortex Debug Connector 10-pin (0.05 in pitch)
TCK/SWCLK	9	4
TMS/SWDIO	7	2
TDI	5	8
TDO/SWO	13	6
$\overline{\text{RESET}}$	15	10
GND	4, 6, 8, 10, 12, 14, 16, 18, 20	3, 5, 9
TVCC	1	1

Tiva™ C Series microcontrollers have default internal pull-up resistors on TCK, TMS, TDI, and TDO signals. External pull-up resistors are not required if these connections are kept short. If the JTAG signals are greater than 2 in. (51 mm) or routed near an area where they could pick up noise, TCK should be externally pulled-up with a 10K or stronger resistor or pulled-down with a 1K or stronger resistor to prevent any transitions that could unexpectedly execute a JTAG instruction.

The TM4C123x family of devices has an errata that prevents the use of TCK(PC0) as a GPIO. Refer to the devices errata for additional details.

3.9 CoreSight ETM Trace Port Connections

The TM4C123x family of microcontrollers includes ARM's Embedded Trace Macrocell (ETM) for instruction trace capture. Trace data is output on pins TRD0-3 and clocked with TRCLK. Refer to the Signal Tables in the device's data sheet to determine which GPIOs the trace signals are available on. ARM defines a 2x10 0.05 in pitch connector with a key on pin 7 as a standard to interface to debuggers supporting JTAG with trace data capture. Figure 29 shows this connector definition with signal names corresponding to those found in the Tiva™ C device's data sheet.

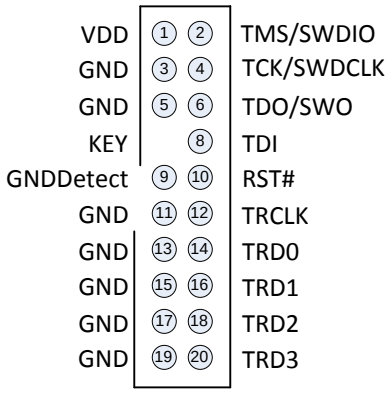


Figure 29. Cortex + ETM Connector

On TM4C123x family devices, TRCLK runs at 1/2 of the system clock speed, which can be a high frequency. TRD0-3 and TRCLK should be short traces less than 6 in. (152 mm) in length. The TRCLK and TRD0-3 I/O pads should be configured for 8mA drive strength initially and reduced on an individual basis if needed.

On some Tiva™ C microcontroller development kits, the 2x10 0.05 in pitch connector is used, however PA1 (U0TX) is connected to pin 14 (TRD0) and PA0 (U0RX) is connected to pin 16 (TRD1) in order to provide a debug UART interface to TI's on-board ICDI.

3.10 System

This section describes system-level design considerations related to the TM4C123x family of microcontrollers.

3.10.1 I/O Drive Strengths

The Tiva™ C series microcontrollers have GPIO pads with programmable drive strength. For outputs driving high-speed buses, higher capacitance loads greater than 15pF, or LEDs, the 8mA drive strength should be selected. Higher drive strengths can be selected based on the V_{OL}, V_{OH} and total GPIO current per side limits given in the parts data sheet.

Some Tiva™ C series microcontrollers have GPIO pads that are limited to 2mA drive strength. If these pads are to be used as outputs, they should be limited to low capacitance loads less than 15pF or signals that can support the longer rise/fall time associated with a 2mA drive strength. Refer to the device's data sheet for a list of GPIO pins supporting only 2mA drive.

The GPIOs that are shared with the USB functions USB0DP and USB0DM on TM4C123x microcontrollers are fixed at 4mA drive strength and cannot be configured as open drain. These limitations must be considered if these pins are used as outputs.

3.10.2 Series Termination Resistors

Series termination resistors provide two different functions. The first type of use is for outputs with fast rise/fall times driving light loads to help match the output impedance of the driver to the impedance of the net being driven. This configuration helps with several items:

- Lower over- or under-shoot at the input destination.
- Reduce ringing near the transition region of the input that could cause false clocking or timing violations.
- Limit crosstalk induced on neighboring signals.
- Reduce EMC emissions.

Output series termination is best placed within 0.5 in (12.7 mm) of the output pin. The values used are system dependent but often are one of 0Ω, 10Ω, 22Ω or 33Ω.

The second type of series termination resistor use is to protect input and output pins from ESD strikes by limiting the currents and voltages seen at these pins. This protection is particularly important for signals that go to connectors that are exposed externally to the system and for signals that go through connectors to other boards or cables that remain in the system. Higher speed signals that go from board to board typically have resistor values in the 10Ω to 33Ω range. Lower speed signals that connect to cables or external connectors typically have resistor values in the 50Ω to 150Ω range.

3.10.3 ESD/EMC Protection

Any signal from the Tiva™ C series microcontroller that is exposed outside the system enclosure via a connector should have ESD protection. Common examples are Ethernet and USB signals. ESD protection for USB is covered in Section 4.1.

In some system environments, signals that stay internal but come through a connector from another board or cable can be subject to radiated noise from electrical noise sources such as motor drivers, relays, and other power-switching circuits. Radiated noise is particularly a concern for two-layer boards that do not have a solid ground plane to shield the signals from this type of noise. For signals that fall into this category, it is recommended that PCB footprints be included in the design to allow for the components shown in Figure 30 or Figure 31. Package options for the TVS diodes that support multiple I/O are also available.

The exact resistor values and TVS diode configuration is highly system and environment dependent. Timing requirements of the interface, input or output signal direction, exposure to electrical noise sources, and IEC test level must be taken into account when determining what values to use.

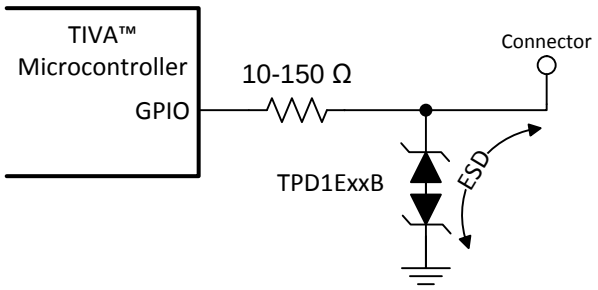


Figure 30. General Protection Using Bi-direction TVS Diode

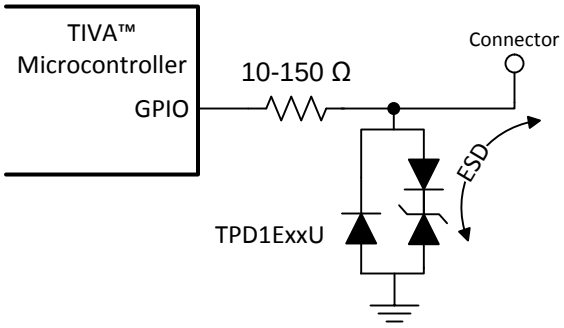


Figure 31. General ESD Protection Using Uni-direction TVS Diode

Table 12 lists some recommended TI ESD protection options for use with the Tiva™ C series microcontrollers.

Table 12. ESD Protection Options

Part#	Description
TPD1E10B06	Bi-Directional ESD protection for low-speed I/O with +/-6V breakdown voltage and 12pF IO capacitance.
TPD1E05U06	Uni-Directional ESD protection for high-speed I/O with +6.5V breakdown voltage and 0.45pF IO capacitance
TPD2E001	2-Channel Low-Capacitance ESD protection array for high-speed data interfaces
TPD4S012DRYR	4-Channel ESD Protection for USB-HS/USB OTG

3.10.4 Interrupt Pin Selection

Any GPIO pin in the microcontroller can be used as an interrupt input pin. In most cases, there is one interrupt vector per GPIO port, so the interrupt service routine must check status registers to determine which port pin generated the interrupt. The system designer must determine if it is more desirable to group more than one interrupt within a GPIO bank or separate interrupts to unique GPIO banks. Some Tiva™ C Series microcontrollers have one or two GPIO banks where each individual pin in that bank has a unique interrupt vector. Consult the device's data sheet to determine which GPIO pins have this capability.

3.10.5 Clock Routing

Special attention should be paid to any pins or nets that are used as clock signals. The cleanest clock is one that routes directly from an output pin to an input pin without stubs, tees, or multiple destinations. The following guidelines should be considered when routing clock signals:

- Give clocks 2x spacing from other signals. Fore example, if a 7 mil trace with 7 mil space routing rules are being used, give 14 mil spacing between the clock and any other signal. This distance limits any crosstalk from neighboring nets.
- Add a footprint for a series resistor close to the clock output pin in order to adjust for any ringing or EMI concerns beyond what changing the I/O drive strength can do. Typical series resistor values are 0Ω, 10Ω, 22Ω or 33Ω.
- If probe points are added for clocks, place them as close to the clock destination as possible. Consider adding a ground point nearby for ease of measurement. Clocks look their noisiest near the middle of the net due to reflections. Clocks measured at a location other than the destination are usually not representative of of how the signal appears at the destination.
- When routing a clock to multiple destinations, try to group the destination points in the same area. In most cases, it is best to daisy-chain route the clock instead of tee routing the clock to the destinations. Tee routing generally causes greater reflections unless carefully balanced.
- When routing a clock to multiple destinations, place the most timing sensitive and critical of the destination devices at the end of the net where the clock is the cleanest.
- The clock should follow the same general path as the data and control signals associated with the interface it clocks to help maintain any relative bus timings.
- Clocks should avoid crossing splits in the ground or power plane.

NOTE: Clocks that are open-collector, such as I2C clocks running at 400KHz, have a very slow rise time and are designed for multiple drops. These guidelines are not meant to restrict such clocks.

3.10.6 5-V Tolerant Inputs

Most GPIOs on the TM4C123x family of microcontrollers have 5V tolerant inputs. Each device has a few GPIO pins that are not 5-V tolerant. Refer to the device's data sheet for details on which GPIOs are 5V tolerant inputs and which are only 3.3V tolerant inputs.

3.10.7 Unused Pins

The preferred connection for an unused microcontroller pin depends on the pin function. Each Tiva™ C Series microcontroller data sheet has a table in the *Signals Tables* chapter that lists the fixed function pins as well as both the acceptable practice and the preferred practice for reduced power consumption and improved electromagnetic compatibility (EMC) characteristics. If a module is not used in a system, and its inputs are grounded, it is important that the clock to the module is never enabled by setting the corresponding bit in the RCGCx register.

3.10.8 Errata Documentation

Part of any good system design includes reviewing and understanding any errata associated with the revision of device being used. Each family of Tiva™ C series microcontrollers has a separate published errata document that describes any deviations from the data sheet. These advisories must be followed to ensure correct device operation.

3.11 All External Signals

This section describes design considerations related to signals that connect directly from the microcontroller to a connector that takes the signal to another board or external device.

The system design must ensure that the ground reference of any incoming signal is the same as the microcontroller ground. If the grounds do not match, the signal level seen at the input pin of the microcontroller might be significantly higher than what the data sheet specifies. Ground connections between boards should be low impedance and as short as possible.

The system design should avoid routing the V_{DD} 3.3V supply that connects to the microcontroller directly to a connector pin that can be subject to ESD or EMC radiated emissions. If V_{DD} does need to be routed to a connector, it should be routed through a ferrite bead and optionally a TVS diode.

I/O signals that are sourced from cables or other boards should not be driven prior to the power being applied to the microcontroller unless the strict guidelines for injection current and voltage limits from the data sheet are followed.

External I/O signals that come directly from the microcontroller should have layout options to implement ESD protection, as described in Section 3.10.3.

4 Feature-Specific Design Information

This section contains feature-specific design information and is grouped by function or peripheral:

- USB
- SSI Buses
- UART
- I2C/SMBUS
- ADC
- Comparators
- Timer/PWM
- Quadrature Encoder Interface (QEI)
- GPIO
- Hibernation Signals

4.1 USB

The TM4C123x family of microcontrollers includes devices that support an internal USB 2.0 PHY capable of full speed operation. Refer to the data sheet of the device being used to determine which of the following configurations the device supports: This internal PHY supports USB Device Only, USB Embedded Host, and USB OTG operation.

The critical component of the internal USB PHY is the bidirectional differential data pins USB0DM (D-) and USB0DP (D+). The following design rules and recommendations should be followed when routing the USB differential pair for best results:

- Route the USB differential pair on the top layer with a trace width and differential spacing tuned to the PCB stack-up for 90Ω differential impedance as detailed in Section 3.3.3.2.
  - It may be difficult to implement a trace geometry that achieves both 90Ω differential impedance and 45Ω single-ended impedance. The most critical parameter to optimize in this design is the 90Ω differential impedance.
  - The trace width and spacing to maintain the required 90Ω differential trace impedance directly at the pins of the microcontroller and directly at the ESD suppressor and USB connector may not be possible to achieve. Minimize these deviations as much as possible being sure to maintain symmetry.
- Follow the recommendations for routing differential pairs as detailed in Section 3.4.8. The individual traces within the differential pair should be length matched to within 0.150 in (3.81 mm).
- Avoid stubs when adding components to D+ and D– signals. Devices such as ESD suppressors should be located directly on the signal traces, as shown in Figure 19.
- Maintain symmetry when routing differential pairs. Some PCB layout tools can assist with this kind of routing. Avoid vias if possible. If it is necessary to switch layers, then both signals in the pair should pass through a via at the same distance on the trace.
- Total trace length for the USB differential pair should be limited to 12 in (30.48 cm).
- Place ESD suppressors as close as possible to the USB connector to minimize any areas of impedance discontinuities. Refer to Table 12 for recommended ESD suppressors.
- For best ESD and EMI performance, create a chassis ground to which the metal shield of the USB connector is connected, as shown in Section 3.4.6.
- Depending on the system design, a common mode choke may be helpful to pass EMI testing. An

ACM2012 common mode choke by TDK is one recommended device. If EMI is a concern for the design, it is recommended that a footprint for the choke be included in the design placed close to the USB connector. Figure 32 shows how two 0805 sized resistors (R29, R30) can be placed and later replaced with an ACM2012 choke if needed during system EMI testing.

- Additional High Speed USB Platform Design Guidelines including more details on using a common mode choke can be found at http://www.usb.org. Refer to http://www.usb.org/developers/docs/hs_usb_pdg_r1_0.pdf.

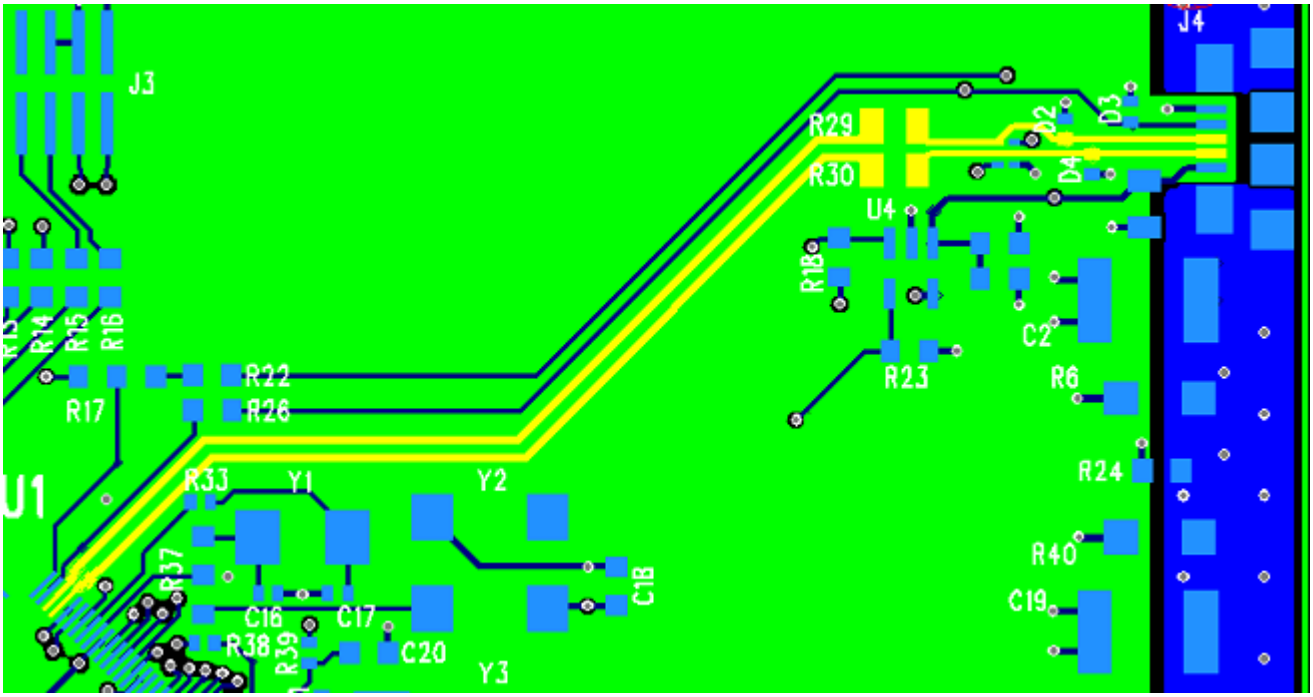


Figure 32. USB Routing Example

4.1.1 USB Device Only

For TM4C123x devices that are used in a device-only configuration, the only signal used in addition to USB0DM and USB0DP is USB0VBUS, which is located on port PB1. In USB device-only mode, USB0VBUS is used to detect when voltage has been applied to or removed from the USB connector, which triggers software to manage the internal USB PHY accordingly. When configured as USB0VBUS, this pin is 5-V tolerant. However, when used as a GPIO input, PB1 is NOT 5-V tolerant. An alternate 5-V tolerant Fail-Safe GPIO should be selected to do the VBUS detection if there is a chance 5V could be applied to the input prior to PB1 on the TM4C123x device being configured for VBUS, such as during power-up, while the device is in reset, and the while the initial boot sequence executes.

For a USB device-only configuration, a 100Ω resistor should be placed in series between VBUS on the USB connector and PB1 (or alternate 5-V tolerant GPIO) on the microcontroller in order to limit damage caused by any ESD events.

If PB1 must be used for a function other than USB0VBUS, any other available 5-V tolerant Fail-Safe GPIO could be used in its place.

4.1.2 USB Embedded Host

For TM4C123x devices that are used in a host-only configuration, the USB0EPEN and USB0PFLT signals may be used in the design in addition to USB0DM and USB0DP. These two signals typically connect to a power switch such as a TPS2051B, which controls power to the host's USB connector. Refer to the TM4C123x device's data sheet to determine which ports these functions are available on.

4.1.3 USB OTG

TM4C123x devices that support USB OTG mode include the signals for USB Device mode, signals for USB Host mode and an additional signal USB0ID located on pin PB0. This USB ID signal is the 5th pin found on a USB micro-AB connector. If a micro-A cable end is plugged into this connector, the ID pin on the cable is tied to ground causing the TM4C123x device to operate as a USB host. If a micro-B cable end is plugged into the USB connector, the ID pin is left floating. In this case, the TM4C123x device's internal pull-up on the USB0ID signal causes the controller to operate in device mode.

In order to limit damage from ESD events, a 100Ω resistor should be placed in series between the ID pin on the USB connector and USB0ID(PB0) on the microcontroller.

To support full USB OTG negotiation using the SRP and HNP protocols, VBUS from the USB connector must be directly connected to USB0VBUS(PB1) of the microcontroller without a series resistor in between. In this case, USB0VBUS should be connected to an ESD suppressor such as a TVS diode, or ESD resistant VBUS switch. PB1 on the TM4C123x family devices is not 5V tolerant until after PB1 has been configured for its USB0VBUS function. Until this configuration point (during power-up, while in reset and the during the initial boot sequence) the input voltage on PB1 must not exceed the voltage on V_{DD} + 0.3V.

4.2 SSI Buses

Up to four SSI modules (SSI0-SSI3) are available on TM4C123x family devices. All four are capable of being a master or a slave interface.

If the SSI bus is connected to a device, a 10K pull-up should be placed on SSIxFSS to prevent any unexpected accesses prior to code booting and the pins being configured.

The 8mA drive strength should be selected for all outputs in order to meet data sheet timings. Series termination should be used for on any outputs.

4.3 UART

There are 8 UART modules (U0-U7) available on TM4C123x family devices. Basic RX/TX functionality is the same between them. The following are important considerations when selecting UART pins to use:

- Example software commonly uses U0RX on PA0 and U0TX on PA1 for debug messages and input. If a debug port is to be implemented, this location is recommend.
- UART1 offers modem flow control and modem status, UART0, and UART2-UART7 offer only RX and TX.

4.4 I2C

A TM4C123x device can have up to six I2C buses. The buses appear on the I2C0SCL-I2C5SCL/I2C0SDA-I2C5SDA signals. Each bus is functionally equivalent to the others and can be either a master or a slave. Refer to the *Inter-Integrated Circuit (I2C) Interface*" chapter of the TM4C123x data sheet for detailed information.

The I2C bus requires signals to be configured in open-collector mode. The I2CSDA pin requires the associated GPIO to be configured as an open-collector signal in the GPIOODR register. The I2CSCL pin should not be configured in this manner as the pad is designed differently. The TivaWare GPIOPinTypeI2C() API should be used for the I2CSDA pin and the GPIOPinTypeI2CSCL() API should be used for the I2CSCL pin. The I2C pins must be externally pulled-up to 3.3V for proper operation. Typical pull-up values are 2.2KΩ resistors but the value used depends on bus speed and total bus capacitance. Refer to the *Pull-up resistor sizing* section of the UM10204 "I2C-bus specification and user manual" v.5 from NXP for details on how to calculate the minimum and maximum pull-up resistor values.

Only 3.3V I2C buses are directly supported. 5V or 1.8V buses can be supported with the use of external level shifting diodes.

4.4.1 Routing Considerations

An I2C bus should be routed such that the I2CxSCL and I2CxSDA signals follow similar layer transitions and stay within approximately 1000 mils of each other. It is not recommended that these signals be routed as a differential pair and there is no length-matching requirement for them.

I2C signals should not be routed next to signals that can cause significant cross talk to the I2CxSCL signal. Cross talk noise could interfere with the I2C transaction and cause a bus error requiring an I2C bus is reset.

4.5 ADC

This section describes design considerations related to the microcontroller ADC module.

4.5.1 ADC Inputs

In order to achieve the best possible conversion results from an ADC, it is important to start with a good schematic design.

All ADCs require a voltage reference (or occasionally a current reference), whether the voltage reference is provided from an on-chip source or via an external pin. Any deviation in the reference voltage from its ideal level results in additional gain error (or slope error) in the conversion result.

For optimal ADC performance, a precision voltage source should be used to supply the V_{REF+} pin when available as a separate pin on the part or V_{DDA} pin on parts that have V_{REF+} internally connected to V_{DDA}. Refer to Section 3.5.5 for additional details on the filter capacitance required for ADC performance. Refer to the part data sheet for I_{VREF} specification maximum that the precision voltage source must supply.

There are up to 24 pins on the TM4C123x family of devices that support analog inputs AIN00-AIN23. All inputs can be used in single-ended mode, while differential mode is supported for consecutive even/odd pairs. All analog inputs are equivalent in function and capability. Selection of which analog inputs to use should be based on ease of PCB routing and pin muxing selection.

Optimal ADC accuracy is achieved with a low-impedance source (R_S) and a large input filter capacitor (C_S) as shown in Figure 33. As the signal source impedance increases and capacitance decreases, noise on the conversion result increases. Noise sources include coupling from other signals, power supplies, external devices, and from the microcontroller itself.

Refer to the TM4C123x data sheet for specifics on the analog input impedance with respect to the sample and hold circuit. A 500Ω effective input impedance (Z_S) is required to support the maximum input sampling period of 250ns. This input impedance allows the voltage on the ADC input pin to charge C_{ADC} to the input pin voltage going through R_{ADC}. Refer to Figure 33 for the ADC Input Equivalency Diagram and to the part data sheet for the values of C_{ADC} and R_{ADC}.

If voltage rails are to be monitored, adequate capacitance is required to hold the voltage during the sampling period. The exact amount of capacitance (C_S) depends on the accuracy required, the amount of time between samples and the resistor values used for any voltage divider circuit.

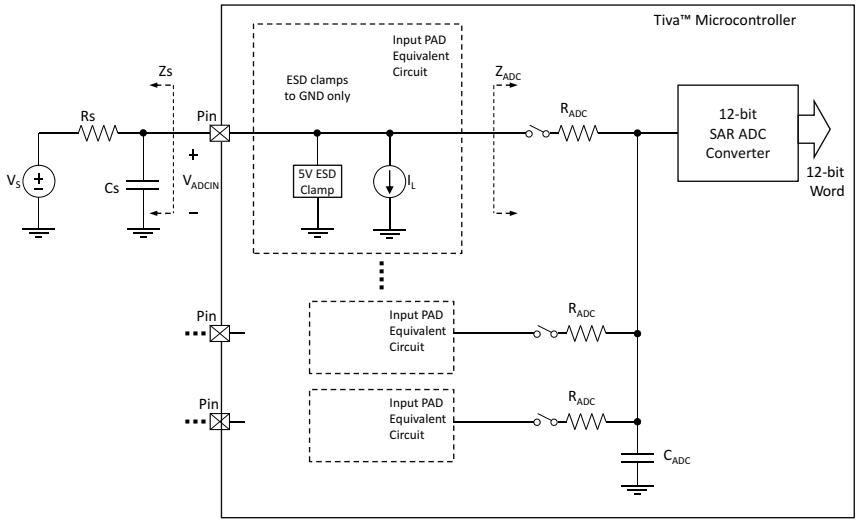


Figure 33. Tiva™ Microcontroller ADC Input Equivalency Diagram

If resistor dividers are used to scale an input voltage, then best results can be achieved with low-value resistors. The resistor from the ADC input to ground should ideally be less than 1 kΩ. Avoid values higher than 10 kΩ unless a large filter capacitor is present. If the voltage rail or other input being monitored is powered up when the V_{DD} and V_{DDA} supplies to the part are not, care must be taken not to exceed the input injection current specified in the data sheet.

Ceramic filter capacitors of 1 µF or more can substantially improve noise performance. The trade-off is a reduction in signal bandwidth (as a function of the source impedance) and phase shifting.

Input protection should also be considered, especially when converting signals from external devices or where transient voltages might be present. The ADC pins on some Tiva C Series devices (in ADC mode) are not 5V tolerant, but do allow some margin over the +3.0V span. See the respective microcontroller data sheet for specific information.

Increased source impedance can provide a degree of protection to the ADC. Semiconductor clamping circuits can also be used—typically zener diodes or clamping diodes to 3.3 V and GND. When specifying diodes, consider leakage current over temperature (I_R) because this parameter affects overall conversion accuracy.

4.6 Comparators

There are three independent integrated analog comparators available on TM4C123x devices. Refer to the *Analog Comparators* chapter of the part data sheet for specific details.

When selecting comparator pins, the following should be considered:

- C0+ (PC6) can be used as a common reference input to all three comparators.
- C0- (PC7), C1- (PC4) and C2- (PJ5) are the unique negative inputs for each comparator.

4.7 Timer/PWM

There are several general purpose timer pins available on a TM4C123x family devices. Refer to chapter *General-Purpose Timers* in the data sheet for specific details. Each timer module has a CCP0 and a CCP1 pin associated with it. There are two different timer module blocks. General-Purpose Timer Module (GPTM) blocks provide two 16-bit timers/counters that can be configured to operate independently or as one 32-bit timer. Wide General-Purpose Timer Module (WGPTM) blocks provide two 32-bit timers/counters that can be configured to operate independently or as one 64-bit timer.

When selecting timer pins, the following should be considered:

- Timers configured for 32-bit mode (GPTM) or 64-bit mode (WGPTM), use the CPP0 pin input. The CPP1 pin input is not used.
- Timer 32-bit modes (GPTM) and 64-bit modes (WGPTM) are one-shot input, periodic input and RTC input.
- PWM outputs operate in 16-bit mode (GPTM) and 32-bit mode (WGPTM) only and therefore both the CCP0 and CCP1 can be independently used as PWM outputs.

4.8 Quadrature Encoder Interface (QEI)

Some TM4C123x devices support connection to a quadrature encoder that tracks position, direction of rotation, and estimates velocity. The frequency of the QEI inputs can be as high as ¼ of the processor frequency. Pins used for the QEI are IDXn, PhAn, and PhBn.

A series resistor followed by a capacitor to digital ground should be placed on each QEI input to filter the inputs from noise that would violate the input electrical specifications of the device. A common value for the series resistor is 100Ω and for the capacitor is 1nF. The electrical specifications of the quadrature encoder being attached and the system environment determine the optimum resistor and capacitor values for the system.

4.9 GPIO

Most pins on a TM4C123x device can be used as a GPIO pin. GPIO pins are designated by the letter P followed by their port letter A-Q followed by their pin number 0-7. GPIO pins can be used for inputs sampled by software, inputs that generate interrupts, outputs that drive logic inputs high or low, or outputs that drive LEDs.

A PinMux Utility for Tiva™C Series MCUs is available, which allows a user to graphically configure the device GPIOs and peripherals.

Refer to the *Electrical Characteristics* chapter of the TM4C123x device data sheet where important operational conditions are detailed.

The following considerations should be taken into account when selecting and designing with pins configured as GPIO inputs:

- GPIOs muxed with ADC inputs are 5V tolerant for all functions except ADC. A pin configured for ADC input is NOT 5V tolerant.
- GPIOs muxed with USB0ID, USB0VBUS, USB0DP and USB0DM are NOT 5V tolerant and NOT Fail-Safe. Refer to the device datasheet for exact details on the limitations. The GPIOs affected vary by device part number.
- GPIO pins can be configured with an internal pull-up or pull-down. Refer to the *Electrical Characteristics* chapter of the TM4C123x device data sheet for specifics of the internal pull-up and pull-down values. It may be desirable to use external pull-ups or pull-downs in situations where a more consistent rise/fall time is required.
- GPIO pins PB0, PB1 and PE3 may draw additional leakage current at power-up and require a strong external pull-up to maintain levels above V_{IH}. Refer to the devices datasheet for specific details.
- Fail-Safe GPIO pins have a higher I_{LKG+} specification when the input voltage V_{IN} is between V_{DD} and 4.5V than when V_{IN} is between 4.5V and 5.5V. Refer to the "Electrical Characteristics" chapter of the device datasheet for details.

The following considerations should be taken into account when selecting and designing with pins configured as GPIO outputs:

- GPIO pins muxed with USB0DP and USB0DM have a fixed 4mA output drive strength and cannot operate in open-drain mode when configured as GPIOs.
- At system power-on reset, pins power up as GPIO inputs with no pull-up or pull-down configured. Pins used as outputs that are required to be at a high or low value at system power up should be externally pulled up or down. The exception to this statement is JTAG pins which power-on with internal pull-ups enabled and configures for JTAG.
- A total of four GPIO pins may be used simultaneously to each sink 18mA, but the V_{OL} is specified as 1.2V when operating in this manner. There should be a maximum of two high current pins per physical die side (defined in the *Recommended Operating Conditions* chapter of the TM4C123x device data sheet).

4.10 Hibernate Signals

Some of the TM4C123x family devices contain a Hibernation module that can be used to put the device in its lowest power state. Refer to the device data sheet for a detailed description of the Hibernation module.

The V_{BAT} pin can be used to power the Hibernation module. Refer to Section 3.5.6 for system considerations related to V_{BAT}.

The Hibernation module can be clocked by a 32.768KHz clock source. Refer to Section 3.7.1.2 for system level considerations of this clock source.

The $\overline{\text{WAKE}}$ pin on the TM4C123x device is used to wake the device from hibernation-mode. This pin is only functional when the device is in hibernation-mode. This pin cannot be accessed as an input when the device is in normal run-mode, sleep-mode or deep-sleep-mode. This pin is can be connected to a switch to ground, and pulled-up externally with a 1MΩ resistor connected to the same supply voltage that the V_{BAT} pin is connected to.

If the $\overline{\text{WAKE}}$ pin is not used, it should be connected to system ground.

The $\overline{\text{HIB}}$ pin on the TM4C123x device can be used to control the regulator supplying V_{DD}. Refer to the TM4C123x data sheet for more details on the Hibernate functionality.

If the $\overline{\text{HIB}}$ pin is not used, it can be left unconnected.

5 System Design Examples

For example designs using the TM4C123x family of microcontrollers, see Table 13 for the detailed list of TM4C123x Reference Design Kits (RDKs), Evaluation Kits (EKs), and Development Kits (DKs).

Table 13. TM4C123x Example Designs

Part Number	Description	Tiva C Series Device	Device Package	Key Features	PCB Layer Count
DK-TM4C123G	Development Kit	TM4C123GH6PGE	LQFP144	USB, CAN, Motion Sensor, hibernate, real-time clock	6
EK-TM4C123GXL	LaunchPad Evaluation Board	TM4C123GH6PM	LQFP64	Simple two-layer layout, LaunchPad Headers	2

6 Conclusion

Applying good system design practices from the earliest design stages ensures a successful board bring-up. The design process should include thorough design reviews using the information in this application report, other embedded system design resources, and reports created by the design team. These efforts will be rewarded with a reliable and properly performing Tiva C Series microcontroller-based design.

The use of the TivaWare™ for C Series Peripheral Driver Library also minimizes software changes to the start-up routines that configure the I/O, enabling application code to be moved to the new devices with minimal functional changes.

7 References

The following related documents and software are available on the Tiva C Series web site at www.ti.com/tiva-c:

- Tiva C Series TM4C Microcontroller Data Sheet (individual device documents available through product selection tool).
- TivaWare for C Series Driver Library. Available for download at www.ti.com/tool/sw-tm4c-drl.
- TivaWare for C Series Driver Library User's Manual (literature number SPMU298).
- Tiva™C Series PinMux Utility. Available for download at www.ti.com/tool/tm4c_pinmux

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