Renesas Synergy™ Platform

Guidelines to Reducing Power Consumption in the Active State for S3A7

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Introduction

This application note describes methods of reducing power consumption for S3A7 Synergy™ MCU Group.

Target Device

S3A7 Synergy MCU Group

Note: Before applying this application note to a different MCU, make any changes to suit the microcontroller you are using, and run sufficient tests for evaluation.

Contents

1. Overview of power consumption by microcontrollers

The power consumed by microcontrollers (MCU) falls into two types. The first type is dynamic power consumption which depends on the operating frequency of the MCU. Dynamic power consumption has the characteristic that the power consumption increases in proportion to the operating frequency. The second type is static power consumption which does not depend on the operating frequency. While static power consumption does not depend on the operating frequency, it can be affected by the power supply voltage and the ambient temperature. The key components of each type of power consumption are given below.

Dynamic power consumption

- Switching power consumption resulting from internal signal transitions
- Power consumption resulting from shoot-through current

Static power consumption

- Power consumption required for analog circuits to operate
- Power consumption resulting from leakage current

In embedded systems design, reducing dynamic power consumption is an important key to realizing low power consumption. Reducing dynamic power consumption has a tradeoff with the MCU's performance, and therefore requires optimal designing that suits the given embedded system. The static current is physical power consumption that cannot be reduced at the application level. A model of the power consumption is given in the figure below.

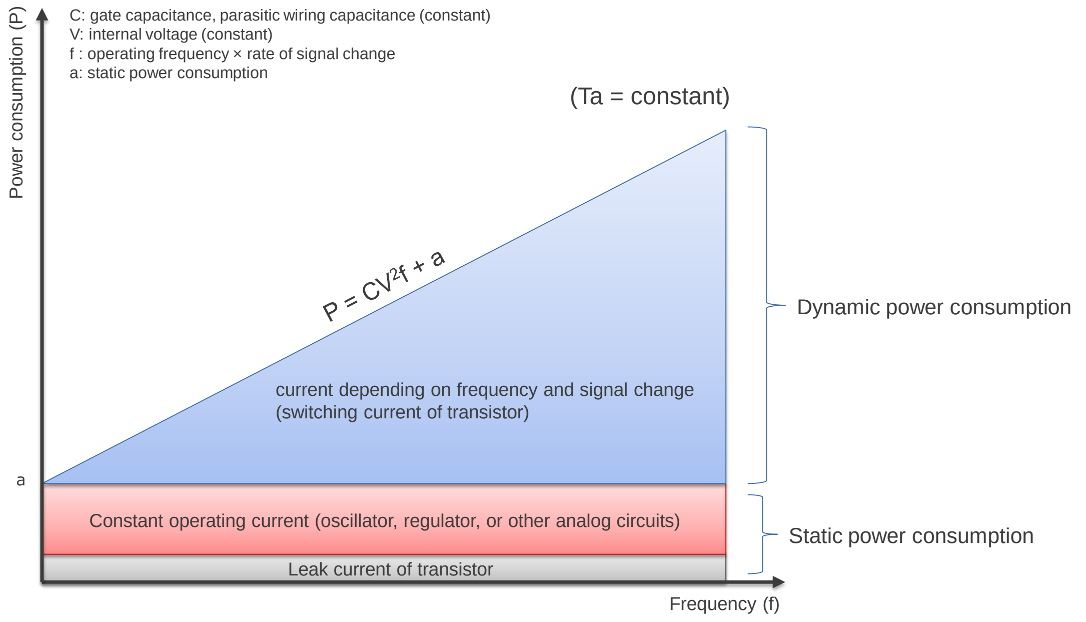


Figure 1 Model of power consumption

1.1 Dynamic power consumption

Dynamic power consumption refers to the power that is consumed when the MCU is operating. When the MCU operates, switching of the internal signals occur that is dependent on the operating frequency. During the signal transitions, PMOS and NMOS turn on simultaneously and causes a shoot-through current to flow. To convey the signal transition to the next stage, a current flows to charge (or discharge) the parasitic wiring capacitance and gate capacitance of the next stage. Under certain operating conditions, because the parasitic wiring capacitance or next stage gate capacitance and voltage are constant, the dynamic power consumption is considered proportional to the frequency. In other words, because signal transitions are dependent on the operating frequency, power can be reduced by lowering the frequency.

Dynamic power consumption $\propto CV^2f$

C: Gate capacitance, parasitic wiring capacitance (constant)

V: Voltage (constant)

f: Frequency

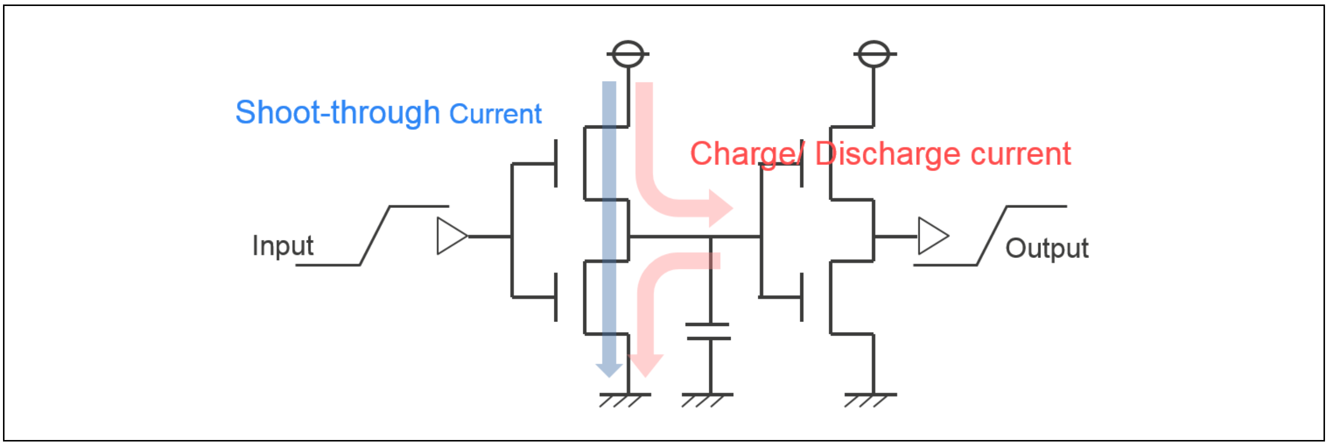


Figure 2 Circuit of current drawn in dynamic power consumption

1.2 Static power consumption

Static power consumption refers to steady-state power consumption that is not dependent on the MCU frequency. Analog circuits such as the low voltage detection circuit, comparator, and internal regulator have a steady draw of current resulting from operation of the circuit. The current drawn can be controlled by stopping the analog circuit or changing the operating mode.

Leakage current cannot be controlled through the application, because it is arbitrarily determined by the manufacturing process or the scale of the circuit that the power source is supplied. Because leakage voltage increases under conditions of high voltage and high humidity, an optimal setting of the power supply voltage, and keeping the ambient temperature from rising is required.

1.3 Summary

Reducing power consumption has a tradeoff with the MCU's performance. Optimization of the design to suit the specific target application is required.

When designing a system where power consumption is of the utmost concern, such as batteries and battery-driven systems, you want to choose a MCU that has the minimal processing speed to achieve your functional needs and supports only a minimal set of functions and memory.

In contrast, in an environment with a reliable power source, equipped with a cooling fan, and where the main purpose is arithmetic processing, a MCU that supports a high operation-guaranteed frequency and large memory size may be a good choice.

2. Low power consumption in the S3A7 Synergy MCU Group

The S3A7 Synergy MCU Group provides the following features for realizing low power consumption. Power consumption can be reduced by applying the right combination of the following controls and modes. The specification of the low power functions as specified in Section 11, Low Power Mode of the *S3A7 Series User's Manual*: *Microcontrollers* is given below.

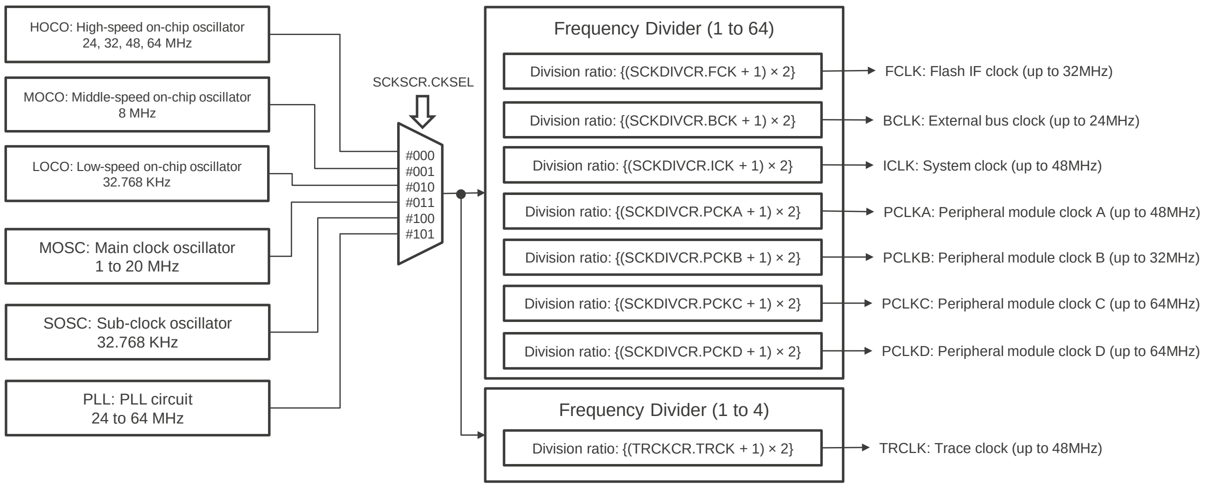
Table 1 Specification of low power mode functions

Item	Specification
Clock division	The frequency division ratio is settable independently for the system clock (ICLK), peripheral module clock (PCLKA, PCLKB, PCLKC, PCLKD), external bus clock (BCLK), and flash interface clock (FCLK).
EBCLK output control	The output from the EBCLK pin is selectable between clock output or H-level output.
Module stop function	Supply of the peripheral module clocks can be stopped for each peripheral module.
Low power modes	Sleep mode Software Standby mode Snooze mode
Power control modes	High-speed mode Mid-speed mode Low-speed mode Low-voltage mode Subosc-speed mode

2.1 Clock division

The lower the frequency of the system clock (ICLK), peripheral module clock (PCLKA, PCLKB, PCLKC, PCLKD), external bus clock (BCLK), and flash interface clock (FCLK), the greater the reduction in the power consumption. For clocks that are not in use (such as when no external bus is used), power consumption can be minimalized by setting a division value of 1/64 (maximum division value).

The figure below shows the relationship between the clock source and the clock frequency divider.



[Limitation]
Limitation of Frequency: ICLK ≥ PCLKA ≥ PCLKB, PCLKD ≥ PCLKA ≥ PCLKB, PCLKD ≥ PCLKB
Limitation of Frequency ratio: (N: integer and up to 64)
ICLK:FCLK = N:1, ICLK:BCLK = N:1,
ICLK:PCLKA = N:1, ICLK:PCLKB = N:1,
ICLK:PCLKC = N:1 or 1:N, ICLK:PCLKD = N:1 or 1:N
P/E flash frequency: FCLK ≥ 1MHz

Figure 3 Relationship between clock source and frequency divider

2.2 Controlling EBCLK

EBCLK is the operating clock for the external bus clock (BCLK) and external bus controller. It is also output externally from the EBCLK pin for the external connection bus. Because power consumption grows as EBCLK continues to output, it should be set to H-level output when it is no longer in use.

2.3 Module stop function

The S3A7 has a module stop function for stopping the clock supply to the peripheral modules. Power consumption can be reduced by stopping the peripheral modules that are not in use.

A module stop state is set on the peripheral modules using module stop control registers A to D (MSTPCRA to MSTPCRD). After a reset is released, the peripheral modules are in module stopped state. The following peripheral modules are released from the module stopped state after a reset, and may need to be placed in a module stop state as necessary.

- SRAM0: The MSTPA0 bit (b0) in the SYSTEM.MSTPCRA register
- SRAM1: The MSTPA1 bit (b1) in the SYSTEM.MSTPCRA register
- ECCSRAM: The MSTPA6 bit (b6) in the SYSTEM.MSTPCRA register

The figure below shows the relationship between the operating clock of each module and the module stop control bits.

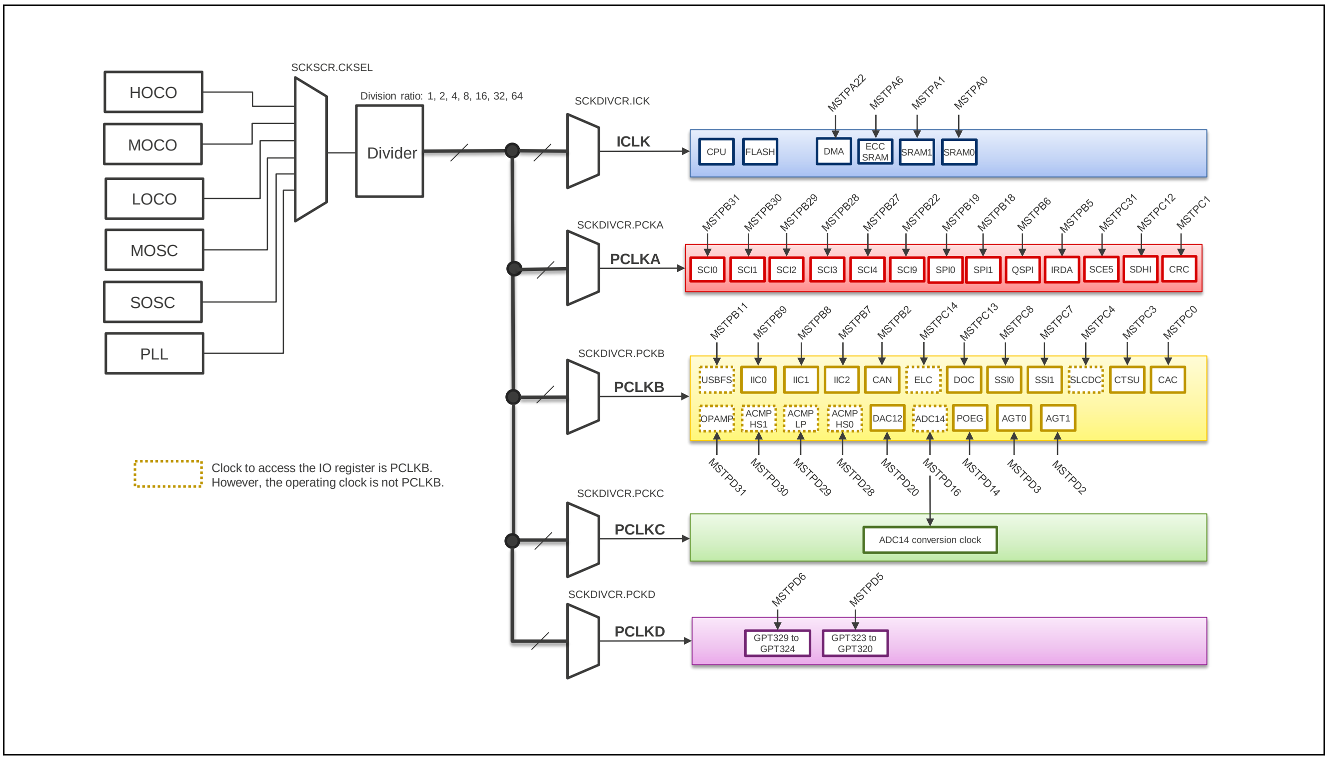


Figure 4 Clock types and the MSTP bits

Some peripheral modules have no module stop function. Disable the operation of such peripheral modules when it is not in use. The peripheral modules that have no module stop function are given below.

- KINT
- RTC
- LVD
- Clocks
- Code/Data Flash
- TSN

2.4 Low power modes

The S3A7 MCU has three low power modes for reducing power consumption. Each of these modes significantly reduces the power consumption but differ in their operating states. For details, see *S3A7 Series User’s Manual: Microcontrollers*.

2.4.1 Sleep mode

When a WFI instruction is executed while the SBYCR.SSBY bit is set to 0, the MCU enters sleep mode. In this mode, the CPU stops operating but the contents of its internal registers are retained. Other peripheral functions do not stop.

The available resets or interrupts in sleep mode cause the MCU to cancel sleep mode and transition to normal mode. If using a maskable interrupt to cancel sleep mode, set the interrupt to cancel sleep mode in the associated IELSRn register before executing a WFI instruction.

2.4.2 Software standby mode

When a WFI instruction is executed while the SBYCR.SSBY bit is 1, the MCU enters software standby mode. In this mode, the CPU, most of the on-chip peripheral functions and oscillators stop. The contents of the CPU internal registers and SRAM data, the states of on-chip peripheral functions and the I/O Ports are retained. The software standby mode significantly decreases the power consumption. To wake from software standby mode, use an interrupt with the wakeup function enabled.

2.4.3 Snooze mode

In software standby mode, when a request to switch to snooze mode occurs, the MCU transfers to snooze mode. In this mode, some peripheral modules operate without waking up the CPU.

2.5 Power control modes

By selecting the appropriate operating power control mode according to the clocks to be used, the frequency and operating voltage, power consumption can be reduced. The S3A7 Synergy MCU Group supports five different modes, high-speed mode, mid-speed mode, low-speed mode, low-voltage mode, and subosc-speed mode.

When switching to a mode with a small maximum frequency value, configure the registers as specified in section 11.5.1, Setting Operating Power Control Mode in the *S3A7 Series User's Manual: Microcontrollers*.

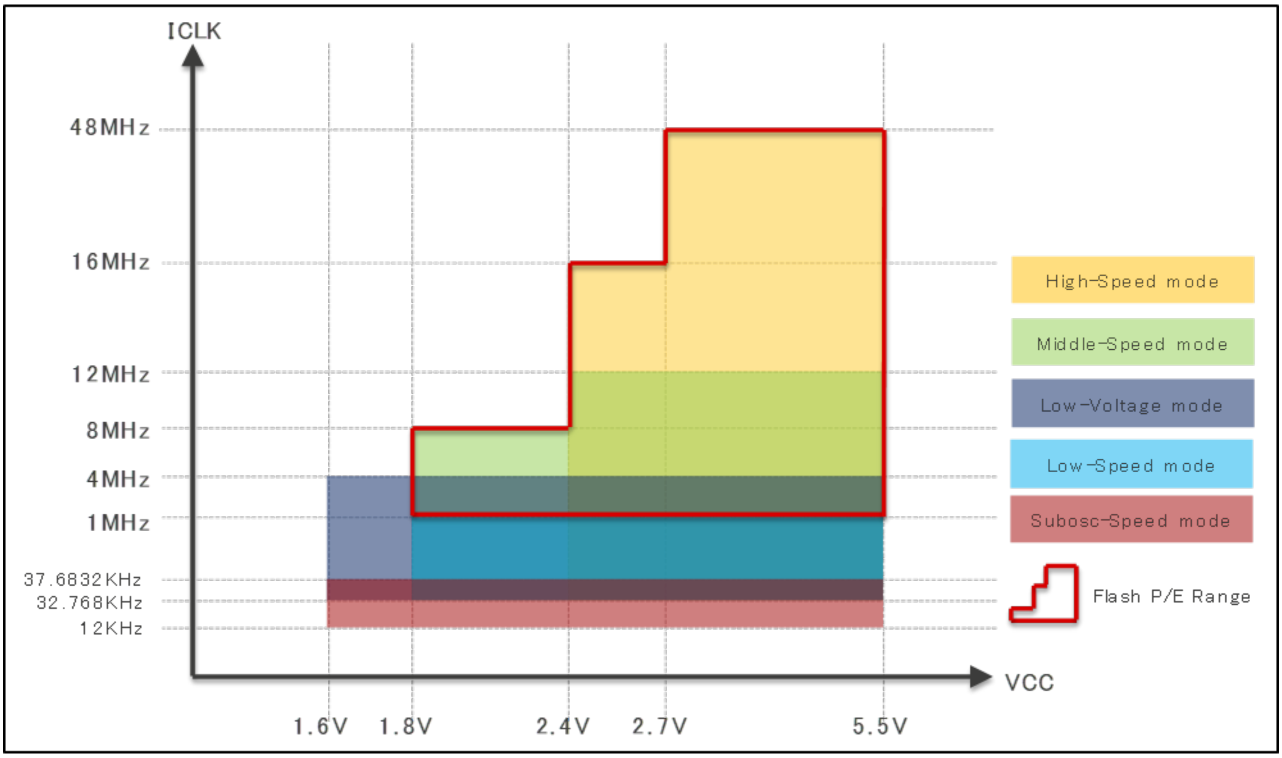


Figure 5 Operating Range

2.5.1 High-speed mode

In this mode, the MCU operates at the maximum frequency of 48 MHz. The power supply voltage range is 2.4 to 5.5 V. Select high-speed mode when performance-oriented high-speed processing is required.

Running systems that support intermittent operation in software standby mode for long periods can conserve power by minimizing the amount of time the CPU is in the active state, even if the system is performance-oriented for high-speed processing. Since the degree in reduction of power consumption that can be gained from intermittent operation largely depends on the system itself. You will need to evaluate the system adequately in terms of whether high-speed mode is required.

2.5.2 Mid-speed mode

In this mode, the MCU can operate over a wide power supply voltage range from 1.8 to 5.5 V and at frequencies up to 12 MHz. For example, in a battery-driven system, the MCU can perform high-speed processing when the battery has sufficient remaining energy, and drop to a lower frequency and a voltage of 1.8 V when the remaining battery energy becomes low.

2.5.3 Low-speed mode

In this mode, the maximum operating frequency is 1 MHz, and the operating voltage range is 1.8 to 5.5 V. Rewriting the flash memory, and use of the PLL is prohibited in this mode.

2.5.4 Low-voltage mode

In this mode, the maximum operating frequency is 4 MHz, and the operating voltage range is 1.6 to 5.5 V. When rewriting the flash memory, set the power supply voltage to 1.8 V or higher. Use of the PLL is prohibited in this mode.

2.5.5 Subosc-speed mode

In this mode, the maximum operating frequency is 32.768 kHz, and the operating voltage range is 1.6 to 5.5 V. Rewriting the flash memory is prohibited. For the clock circuit, only the sub-clock oscillator or low-speed on-chip oscillator can be used.

2.6 Summary

Power consumption can be reduced by controlling the clock divisors and the EBCLK, using the module stop function to stop peripheral modules that are not in use, or by using larger frequency divisors for the peripheral clocks.

Switching to low-power modes as appropriate for the CPU processing involved can also help to reduce the power consumption.

The table below lists the advantages and disadvantages of each power control mode. Use the table to select the appropriate modes to reduce the power consumption of your application.

Table 2 Power control mode features

Power Control Mode	**System clock maximum frequency** **Standard value for current drawn**	**Power supply voltage range**	**Flash P/E**	**Summary**
High-speed mode	48 MHz 11.8 mA	2.4 to 5.5 V	Power supply voltage 2.7 V or higher System clock frequency 1 MHz or higher	This mode allows operation at the maximum operating frequency. Select this mode to reduce the processing time during active state in intermittent operation.
Mid-speed mode	12 MHz 3.6 mA	1.8 to 5.5 V	System clock frequency 1 MHz or higher	This mode supports a power supply voltage range of 1.8 to 2.4 V, and a maximum operating frequency of 8 MHz.
Low-speed mode	1 MHz 0.5 mA	1.8 to 5.5 V	Not possible	This mode provides the lowest power consumption for applications when they require a CPU operating frequency no greater than 1 MHz.
Low-voltage mode	4 MHz 2.5 mA	1.6 to 5.5 V	Power supply voltage 1.8 V or higher System clock frequency 1 MHz or higher	This mode supports operation at the lower limit for the power supply voltage, 1.6 V.
Subosc-speed mode	37.6832 kHz 13.5 uA	1.6 to 5.5 V	Not possible	This mode provides the lowest power consumption while the CPU is running.

3. Examples of calculated results for current drawn using the DK-S3A7

The DK-S3A7 Synergy MCU Group has shunt resistors built into the digital power supply, analog power supply, and the battery backup power supply. Values for current draws of more than a few mA can be obtained by measuring the voltage applied to the ends of the resistors, without requiring a specific device for measuring current.

In this section, the power consumption per bit of the module stop bits, is estimated by measuring the differences in the current drawn when the module stop function is switched on and off.

3.1 Evaluation environment

ISDE: e^2 studio V4.2.0.012

Board: DK-S3A7 v1.1

3.2 Logic

To measure the current drawn by a specific module, we measure the MCU's operating current when the given module is running and stopped, and obtain the difference. This difference is the current drawn by the module.

Operating current of a given module =

(operating current of the MCU with the module enabled) - (operating current of the module with the module disabled)

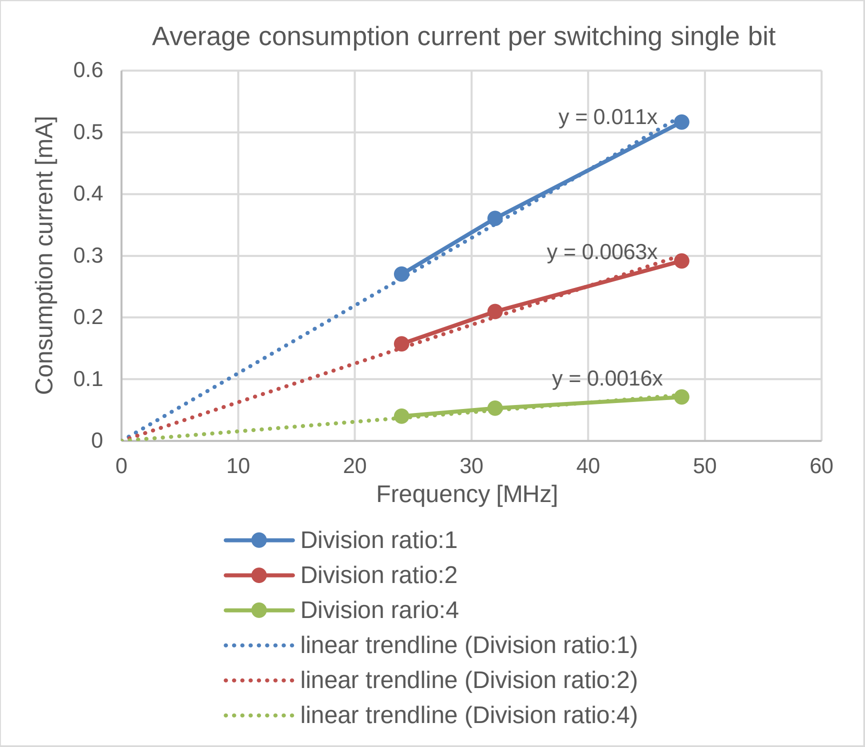
Note: Differences in the allocation of programs and compiler options can affect the MCU's operating current, the development environment conditions as well as the MCU's operating conditions must be the same.

3.3 Currents Drawn by peripheral clocks

The graph below shows the characteristics of frequency and current drawn from controlling single module stop bits.

In evaluation on the DK-S3A7 MCU, results are not accurate enough to obtain the differences in current from switching single bits on and off, so we conduct the measurement through the following procedure.

1. Measure the current with the module stop function for all modules set to the released state.
2. Measure the current with all modules stopped.
3. Get the difference between the results in 1 and 2, and divide by the number of module stop bits.



The frequency vs. current characteristics can be expressed by linear functions. Also, since the differences are being acquired, the measurement does not include the static current. Therefore, linear approximations can be drawn from the origin.

From this graph, we are able to predict how much power consumption can be reduced by enabling the module stop functions.

In the example above, we acquired the characteristics for current drawn by the module clock paths by stopping the modules. We can use the same method to measure the operating currents of the modules, by accurately measuring the currents and obtaining the differences between the values when the modules are and are not operating.

3.4 ULPBench

ULPBench is produced by the Embedded Microprocessor Consortium (EEMBC), the creator of various benchmark tests. This benchmark involves a defined task being performed every second, and repeatedly switching to a low power mode each time the defined task is completed. Quantifying the power consumption in this process provides baselines by which the power efficiency of given products can be compared.

The DK-S3A7 MCU has shunt resistors built into the board, making it impossible to run ULPBench. We thus made a board specifically to run ULPBench. We provide the optimal settings used in executing ULPBench below for reference.

Table 3 Reference Information

Function	Active State	Software Standby State	Additional Information
Code Flash	CPU instruction execution	Not accessed	
Data Flash	Not accessed	Not accessed	
SRAM0	Accessed	SRAM0 is OFF except for a 48 KB area	The PSMC bit in the PSMCR register is set to 01b
SRAM1	Not accessed	SRAM1 is OFF	
HOCO	32 MHz	Stopped	
MOSC/MOCO/LOCO/PLL	Stopped	Stopped	
SOCS	Low power mode3	Low power mode3	
PCLKA/B/C/D,BCLK,FCLK	× 1/16	Stopped	
ICU	Running	Running	Transitions from software standby to active induced by RTC interrupts at 1-second intervals.
RTC	SOCS is running	SOCS is running	Wakeup interrupts are generated at 1-second intervals
I/O Port	Running	Stopped	Run by using the ULPBench Core Profile Code
Other functions	Stopped	Stopped	

3.5 Summary

Reducing power consumption has a tradeoff with the MCU's performance. Determine a baseline based on the MCU's conditions of usage, then find an optimal point in terms of the combination of operating frequency and operating mode.

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Revision History

Rev.	Date	Description	
		Page	Summary
1.20	Oct 2, 2017	-	Initial release

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Renesas Electronics America Inc.
2801 Scott Boulevard Santa Clara, CA 95050-2549, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100191, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, P. R. China 200333
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL II Stage, Indiranagar, Bangalore, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
12F., 234 Teheran-ro, Gangnam-Gu, Seoul, 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

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