

**Granite River Labs DisplayPort™ PHY 1.4 Sink Calibration and  
Test User Guide & Method of Implementation (MOI)  
Using  
Tektronix BSX/BSA Series BERTScope™ and DPO/MSO70000  
Series Real-Time Oscilloscope  
with  
GRL-DP-SINK-BSX or GRL-DP-SINK DisplayPort 1.4 Sink  
Calibration and Test Automation Software**



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## TABLE OF CONTENTS

|  |           |
|--|-----------|
| <b>1 INTRODUCTION</b>  | <b>9</b>  |
| <b>2 REFERENCE DOCUMENTS</b>   | <b>9</b>  |
| <b>3 RESOURCE REQUIREMENTS</b>   | <b>10</b> |
| 3.1 EQUIPMENT REQUIREMENTS .....   | 10        |
| 3.2 EXTENDED CUSTOMIZATION .....   | 13        |
| <b>4 GRL-DP-SINK-BSX/DP-SINK SOFTWARE SETUP</b>                          | <b>13</b> |
| 4.1 SETUP .....  | 13        |
| 4.1.1 Download GRL-DP-SINK-BSX/DP-SINK Software .....                    | 13        |
| 4.1.2 Launch and Set Up GRL-DP-SINK-BSX/DP-SINK Software .....           | 13        |
| 4.2 CONFIGURING THE SOFTWARE BEFORE CALIBRATION AND TESTING .....        | 17        |
| 4.2.1 Session Info .....   | 17        |
| 4.2.2 Conditions for Testing and Calibration .....                       | 17        |
| 4.2.3 Setup Configuration for Testing and Calibration .....              | 19        |
| 4.3 CALIBRATION/TEST SELECTION PAGE .....                                | 21        |
| 4.4 CALIBRATION/TEST PARAMETERS CONFIGURATION PAGE .....                 | 22        |
| 4.5 CALIBRATION TARGET CONFIGURATION PAGE .....                          | 23        |
| 4.6 RUNNING THE CALIBRATION/TESTS .....                                  | 24        |
| <b>5 SINK CALIBRATION SETUPS</b>   | <b>25</b> |
| 5.1 PRE-CALIBRATION/TEST PROCEDURES .....                                | 25        |
| 5.2 CALIBRATION CONNECTION SETUPS .....                                  | 25        |
| 5.2.1 Calibration Setup at TP1 .....                                     | 26        |
| 5.2.2 Calibration Steps at TP1 .....                                     | 26        |
| 5.2.3 Calibration Setup at TP2/TP3 .....                                 | 28        |
| 5.2.4 Calibration Steps at TP1, TP2, and TP3 .....                       | 29        |
| 5.3 SAVING CALIBRATED SIGNALS .....                                      | 32        |
| <b>6 SINK DUT COMPLIANCE TEST SETUPS</b>                                 | <b>33</b> |
| 6.1 TEST CONNECTION SETUPS .....   | 34        |
| 6.1.1 DUT Jitter Tolerance Compliance Test Setup .....                   | 34        |
| 6.1.2 Margin Testing .....   | 36        |
| <b>7 TEST RESULTS AND REPORTS USING GRL-DP-SINK-BSX/DP-SINK SOFTWARE</b> | <b>38</b> |
| 7.1 TEST REPORT GENERATION .....   | 38        |
| 7.1.1 DUT Information .....  | 39        |

|           |   |           |
|-----------|---|-----------|
| 7.1.2     | Summary Table.....  | 39        |
| 7.1.3     | Test Results.....   | 39        |
| 7.1.4     | Calibration Data Plots .....                                      | 40        |
| 7.1.5     | Margin Test Plots.....  | 40        |
| 7.2       | DELETING TEST REPORTS.....  | 41        |
| <b>8</b>  | <b>SAVING AND LOADING TEST SESSIONS</b>                           | <b>42</b> |
| <b>9</b>  | <b>APPENDIX A: MANUAL CTS SINK CALIBRATION AND TEST PROCEDURE</b> | <b>43</b> |
| 9.1       | HBR3 SINK CALIBRATION/TEST SETUP .....                            | 43        |
| 9.1.1     | Calibration Setup and Procedure (at TP1).....                     | 43        |
| 9.1.2     | Calibration Setup and Procedure (at TP3).....                     | 46        |
| 9.1.3     | DUT Test Setup and Procedure (at TP3) .....                       | 49        |
| 9.1.4     | Calibration Procedure at TP2.....                                 | 50        |
| 9.2       | HBR2, HBR, AND RBR SINK CALIBRATION/TEST SETUP.....               | 52        |
| 9.2.1     | Calibration Setup and Procedure .....                             | 52        |
| 9.2.2     | DUT Test Setup and Procedure .....                                | 67        |
| <b>10</b> | <b>APPENDIX B: CONNECTING TEKTRONIX OSCILLOSCOPE TO PC</b>        | <b>69</b> |
| <b>11</b> | <b>APPENDIX C: ARTEK CLE1000-A2 INSTALLATION</b>                  | <b>71</b> |
| 11.1      | INSTALL ISI GENERATOR DRIVER.....                                 | 71        |
| 11.2      | INSTALL CLE1000 GUI.....  | 73        |
| <b>12</b> | <b>APPENDIX D: AUX CONTROLLER DRIVER INSTALLATION</b>             | <b>74</b> |
| 12.1      | INSTALL TEKTRONIX DP-AUX DRIVER .....                             | 74        |
| 12.2      | INSTALL UNIGRAF DPT-200 DRIVER.....                               | 77        |

## List of Figures

|  |    |
|--|----|
| Figure 1. Remote Client Window.....                                      | 14 |
| Figure 2. GRL Automated Test Solutions in Start Menu .....               | 14 |
| Figure 3. Rx Test Solutions in GRL Automated Test Solutions Window ..... | 15 |
| Figure 4. License Details Window.....                                    | 15 |
| Figure 5. Equipment Setup Window – View #1 .....                         | 16 |
| Figure 6. Equipment Setup Window – View #2.....                          | 16 |
| Figure 7. Session Info .....   | 17 |
| Figure 8. Select Lane Under Tests .....                                  | 18 |
| Figure 9. Select Test Points.....  | 18 |
| Figure 10. Select SSC Condition .....                                    | 18 |
| Figure 11. Select Data Rates .....                                       | 18 |
| Figure 12. Select SJ Frequencies .....                                   | 19 |
| Figure 13. Select Test Mode.....   | 19 |
| Figure 14. Select Aux Controller .....                                   | 19 |
| Figure 15. Select ISI Generator.....                                     | 20 |
| Figure 16. Configure Test Settings.....                                  | 20 |
| Figure 17. Configure Margin Test Parameters.....                         | 20 |
| Figure 18. Calibration Selection.....                                    | 21 |
| Figure 19. Tests Selection .....   | 22 |
| Figure 20. Parameters Configuration Page.....                            | 22 |
| Figure 21. Calibration Overwrite .....                                   | 24 |
| Figure 22. Run Tests Page.....   | 24 |
| Figure 23. Typical TP1 Sink Calibration Setup.....                       | 26 |
| Figure 24. Typical TP2/TP3 Sink Calibration Setup .....                  | 28 |
| Figure 25. Saved Calibration File Example .....                          | 33 |
| Figure 26. Calibration.cal File Example .....                            | 33 |
| Figure 27. Compliance Test Setup for DP Sink DUT Jitter Tolerance .....  | 34 |
| Figure 28. Sink Test Pre-Verification Selection .....                    | 35 |
| Figure 29. Sink Compliance Test Selection.....                           | 35 |
| Figure 30. Test Parameters for BER Measurement.....                      | 36 |
| Figure 31. Margin Test Configuration .....                               | 37 |
| Figure 32. Sink Margin Test Selection .....                              | 37 |
| Figure 33. Generate Report Page.....                                     | 38 |
| Figure 34. DUT Information .....   | 39 |
| Figure 35. Summary Table.....  | 39 |

|  |    |
|--|----|
| Figure 36. Compliance Test Results Page .....  | 40 |
| Figure 37. Calibration Results Page.....   | 40 |
| Figure 38. Margin Test Results Page.....   | 41 |
| Figure 39. Test Report Deleted .....   | 41 |
| Figure 40. Saving And Loading Calibration And Test Sessions .....                        | 42 |
| Figure 41. HBR3 Conceptual Setup for TP1 Calibration.....                                | 43 |
| Figure 42. HBR3 Conceptual Setup for TP3 Calibration.....                                | 47 |
| Figure 43. HBR3 Conceptual Setup for TP3 DUT Test .....                                  | 49 |
| Figure 44. Conceptual Calibration Setup at TP1.....                                      | 52 |
| Figure 45. Conceptual Calibration Setup at TP3/TP3_EQ (Standard Connection) .....        | 53 |
| Figure 46. Selecting High Frequency Sine Jitter .....                                    | 54 |
| Figure 47. Initial Jitter Setup.....   | 55 |
| Figure 48. BERTScope D24-3_Clock.ram Pattern .....                                       | 55 |
| Figure 49. BERTScope Rj Adjustment .....   | 56 |
| Figure 50. HBR2 Rj Measurement Example .....   | 57 |
| Figure 51. BERTScope SJ <sub>FIXED</sub> Adjustment Example for HBR2 .....               | 57 |
| Figure 52. HBR2 SJ <sub>FIXED</sub> Measurement Example (Not Showing Target 80mUI) ..... | 58 |
| Figure 53. Jitter Component Settings from CTS.....                                       | 59 |
| Figure 54. BERTScope SJ <sub>Sweep</sub> Adjustment.....                                 | 59 |
| Figure 55. HBR2 SJ <sub>Sweep</sub> Measurement Example.....                             | 60 |
| Figure 56. BERTScope HBR2 ISI Setup Example.....   | 61 |
| Figure 57. HBR2 ISI Measurement Example.....   | 62 |
| Figure 58. HBR2 Compliance Eye Pattern Setup Example .....                               | 63 |
| Figure 59. All Stresses Enabled except Crosstalk for HBR2.....                           | 63 |
| Figure 60. HBR2 Eye Height Adjustment Example.....                                       | 64 |
| Figure 61. HBR2 Eye Height Measurement Example .....                                     | 65 |
| Figure 62. HBR2 Eye Height Measurement with Crosstalk Adjustment.....                    | 66 |
| Figure 63. HBR2 Crosstalk Measurement.....   | 66 |
| Figure 64. Typical DUT Test Setup .....  | 67 |
| Figure 65. Table of Test Times For Each Link Rate Per CTS.....                           | 68 |
| Figure 66. OpenChoice Instrument Manager In Start Menu.....                              | 69 |
| Figure 67. OpenChoice Instrument Manager Menu .....                                      | 70 |
| Figure 68. Device Manager Window .....   | 71 |
| Figure 69. Update Driver Window.....   | 72 |
| Figure 70. Windows Security Window And Confirmation Window .....                         | 72 |
| Figure 71. Device Manager Window After Installation .....                                | 73 |

|   |    |
|---|----|
| Figure 72. CLE1000 GUI.....                     | 73 |
| Figure 73. Device Manager Window .....          | 74 |
| Figure 74. Select and Run Installer File .....  | 75 |
| Figure 75. Installation Dialog #1 .....         | 75 |
| Figure 76. Installation Dialog #2 .....         | 76 |
| Figure 77. DP-AUX Installation Completed .....  | 77 |
| Figure 78. Device Manager Window .....          | 78 |
| Figure 79. Installation Dialog.....             | 79 |
| Figure 80. DPT-200 Installation Completed ..... | 79 |

### List of Tables

|  |    |
|--|----|
| Table 1. Equipment Requirements – Systems.....         | 10 |
| Table 2. Equipment Requirements – Accessories.....     | 12 |
| Table 3. Calibration/Test Parameters Description ..... | 22 |
| Table 4. Run Options .....                             | 24 |

### Revision Record

| Version   | Revision Date      | Description of Changes               | Author(s)  |
|-----------|--------------------|--------------------------------------|--|
| 1.0 Draft | 4/2017             | GRL-DP-SINK-BSX/DP-SINK MOI Creation | Ong Gaik Pheng (GRL)<br><a href="mailto:gpong@graniteriverlabs.com">gpong@graniteriverlabs.com</a> |
| 1.2       | 2/2018             | GRL-DP-SINK-BSX/DP-SINK MOI Updates  | Ong Gaik Pheng (GRL)<br><a href="mailto:gpong@graniteriverlabs.com">gpong@graniteriverlabs.com</a> |
| 1.3       | 8/2018             | GRL-DP-SINK-BSX/DP-SINK MOI Updates  | Ong Gaik Pheng (GRL)<br><a href="mailto:gpong@graniteriverlabs.com">gpong@graniteriverlabs.com</a> |
| 1.4x      | 9/2018,<br>10/2018 | GRL-DP-SINK-BSX/DP-SINK MOI Updates  | Ong Gaik Pheng (GRL)<br><a href="mailto:gpong@graniteriverlabs.com">gpong@graniteriverlabs.com</a> |



# 1 Introduction

This User Guide & MOI describes the step-by-step calibration and procedures to perform DisplayPort 1.4 Sink tests of the VESA DisplayPort Logo Compliance Program using the Tektronix BERTScope (BSX or BSA Model) and DPO/MSO70000 Series Real-Time Oscilloscopes in conformance with the DisplayPort PHY 1.4 Compliance Test Specification (CTS). Sink tests are required to qualify a Sink product or silicon building block for Logo certification and listing on the DP Integrators List.

This User Guide & MOI also explains how to set up and use the GRL-DP-SINK-BSX/DP-SINK software to automate receiver calibration and compliance testing for DisplayPort 1.4 Sink conformance. GRL-DP-SINK-BSX is used with the Tektronix BSX Model BERTScope while GRL-DP-SINK is used with the Tektronix BSA Model BERTScope for testing DisplayPort Sink receivers per the Jitter Tolerance requirements of the DisplayPort PHY CTS version 1.4 and DisplayPort over USB Type-C CTS Rev 1.2a respectively.

The GRL-DP-SINK-BSX software automates stressed signal calibration and jitter tolerance testing at the following DisplayPort data rates– RBR (1.62 Gb/s), HBR (2.7 Gb/s), HBR2 (5.4 Gb/s), HBR3 (8.1 Gb/s) and supports USB Type-C and standard DisplayPort sink device-under-tests (DUT's). The GRL software also supports variable ISI generation through the Artek CLE1000-A2 which enables calibration to be performed with minimum reconfiguration of the setup, allowing measurements to be more fully automated. For link training, compliance, and margin testing through DPCD registers, the software provides automation control using the Tektronix DP-AUX or Unigraf DPT-200 AUX controller for standard DisplayPort connectors and the GRL-USB-PD-C2 USB Type-C Power Delivery Tester for USB Type-C connectors.

The following are the main topics covered by this User Guide & MOI:

1. Equipment required for calibration and testing.
2. GRL-DP-SINK-BSX/DP-SINK software setup for calibration and test automation.
3. Manual DisplayPort PHY CTS Sink calibration and test methodology.

The MOI reduces the CTS test description to practice using the specified test equipment and procedures in an effort to standardize testing across ATC's and equipment manufacturers who perform their own certification measurements.

GRL-DP-SINK-BSX/DP-SINK can be further customized by the user or GRL Engineering using GRL's full KayaQ™ automation framework license. Contact GRL at [support@graniteriverlabs.com](mailto:support@graniteriverlabs.com) or through your Tektronix Account Manager for further details.

# 2 Reference Documents

[1] VESA DisplayPort 1.4a PHY Layer Compliance Test Specification (PHY CTS), Version 1.4, Revision 1.0, 27 July 2018

[2] VESA DisplayPort (DP) Standard v1.4 Specifications

[3] VESA DisplayPort over USB Type-C CTS Rev. 1.2a

## 3 Resource Requirements

### 3.1 Equipment Requirements

TABLE 1. EQUIPMENT REQUIREMENTS – SYSTEMS

| System   | Qty | Description   | Key Specification Requirement   |
|--|-----|---|---|
| GRL-DP-SINK-BSX  | 1   | Granite River Labs DisplayPort 1.4 Sink Compliance Calibration & Test Automation Software for the BSX Model BERTScope – <a href="http://www.graniteriverlabs.com">www.graniteriverlabs.com</a><br>– with Node Locked License to single Oscilloscope/PC OS   |   |
| GRL-DP-SINK  | 1   | Granite River Labs DisplayPort 1.4 Sink Compliance Calibration & Test Automation Software for the BSA Model BERTScope – <a href="http://www.graniteriverlabs.com">www.graniteriverlabs.com</a><br>– with Node Locked License to single Oscilloscope/PC OS   |   |
| BERTScope  | 1   | Tektronix BSX or BSA (B or C Model)   | <ul style="list-style-type: none"> <li>Option STR for stress generation</li> <li>Proper test patterns<sup>[a]</sup></li> </ul>  |
| Real-time Oscilloscope                                       | 1   | Tektronix DPO/MSO70000DX or 70000SX Series Oscilloscope with DPOJET (Jitter and Eye Analysis) software  | <ul style="list-style-type: none"> <li>≥ 12.5GHz BW with Windows 7+ OS</li> <li>DPOJET software for calibration</li> <li>DPOJET setup files and SDLA filters<sup>[b]</sup></li> </ul> |
| ISI Generator  | 1   | Artek CLE1000-A2 <sup>[c]</sup>   | For variable ISI generation   |
| VISA (Virtual Instrument Software Architecture) API Software | 1   | VISA Software is required to be installed on the host PC running GRL-DP-SINK software. GRL's software framework has been tested to work with all three versions of VISA available on the Market:<br>1. NI-VISA: <a href="http://www.ni.com/download/ni-visa-17.0/6646/en/">http://www.ni.com/download/ni-visa-17.0/6646/en/</a><br>2. Keysight IO Libraries: <a href="http://www.keysight.com">www.keysight.com</a> (Search on IO Libraries)<br>3. Tektronix TekVISA: <a href="http://www.tek.com">www.tek.com</a> (Downloads > Software > TekVisa) |   |
| AUX Controller <sup>[d]</sup>                                | 1   | GRL-USB-PD-C2 USB Type-C Power Delivery Tester, Tektronix DP-AUX, or Unigraf DPT-200  | For link training and error detection   |
| Computer   | 1   | Laptop or desktop PC  | For external automation control   |

<sup>[a]</sup> BERTScope DisplayPort patterns are distributed with GRL-DP-SINK-BSX/DP-SINK software and are installed during installation process.

<sup>[b]</sup> DPOJET setup files and SDLA filters are distributed with the GRL-DP-SINK-BSX/DP-SINK software and are installed during installation process. The SDLA software is not required if .flt files have already been created.

*[c] If using the ARTEK CLE1000-A2 as the ISI generator, its USB driver software must be installed on the PC being used for testing and the ARTEK CLE1000-A2 must be connected to the PC via USB. The driver is available from the manufacturer. Refer to Appendix for the driver installation procedure.*

*[d] The USB driver software for the AUX Controller being used must be installed on the PC being used for testing, and the AUX controller must be connected to the PC via USB. The driver for the AUX controller is available from the AUX controller manufacturer. Refer to Appendix for driver installation information for Tektronix and Unigraf AUX controllers. For GRL-USB-PD-C2, refer to [www.graniteriverlabs.com](http://www.graniteriverlabs.com) for the GRL-C2 driver and related documentation.*

TABLE 2. EQUIPMENT REQUIREMENTS – ACCESSORIES

| Accessory  | Qty.   | Description  | Key Specification Requirement           |
|--|--------|--|---|
| VESA-Approved DisplayPort Mated Adapter Fixture Pair | 1      | Standard DP, mDP, or USB Type-C plug-receptacle mated pair adapter (Wilder-Tech, LS-ICT) – <i>DUT connector type dependent</i> | Meets DP1.4 CTS electrical requirements |
| Phase Matched SMA Cable Pair                         | 6      | Tek P/N: 174-4944-xx or equivalent   | Meter, 18 GHz, 50 ohms coaxial          |
| SMA Torque Wrench                                    | 1      | 8 in-lb SMA  |   |
| DC Block   | 2      | Weinchel Aeroflex Model 7006-1 20 GHz DC Block or equivalent   |   |
| TTC (Transition Time Converter)                      | 2      | For Data signals (TTC)<br>PSPL 5915-60PS or equivalent   | 60 ps (10-90)<br>40 ps (20-80)          |
|  | 2      | For Crosstalk signals<br>Keysight 15435A or equivalent   | 150 ps                                  |
| Attenuator   | 2      | For Data signals<br>ATT-0290-06-SMA-02 or equivalent   | 6 dB                                    |
|  | 2      | For Crosstalk (Clock) signals<br>ATT-0290-08-SMA-02 or equivalent  | 6 or 8 dB                               |
| ÷2 RF Splitter                                       | 2      | PSPL5331 or equivalent.<br>For CM if using BSX Series BERTScope  | 18 GHz                                  |
| ÷3 RF Splitter                                       | 2      | JFW Model 50PD-292   |   |
| SMA-Male to SMA-Male Adapter                         | 4      | Centric C3452B Male to Male Adapter or equivalent  | 18 GHz                                  |
| SMA-Female to SMA-Female Adapter                     | 4      | Centric C3371 Female to Female Adapter or equivalent   | 18 GHz                                  |
| 50 Ohm SMA Terminator                                | 12     | Huber+Suhner 455-65SMA5001111NE or equivalent  | 18 GHz                                  |
| LAN Switch   | 1      | Optional <sup>[a]</sup>  |   |
| LAN Cable  | 1 or 3 | For Oscilloscope and BERTScope <sup>[a]</sup>  |   |

<sup>[a]</sup> If the Scope OS is used for automation, one LAN cable can be connected directly from the Scope to BERTScope. If an external PC is used, two LAN cables will be required to connect to the network. *(These cables are not shown in the connection diagrams in this document.)*

## 3.2 Extended Customization

DP-SINK-BSX/DP-SINK can be further customized by the user or GRL Engineering using GRL's full KayaQ™ automation framework license. Contact GRL at [support@graniteriverlabs.com](mailto:support@graniteriverlabs.com) or through your Tektronix Account Manager for further details.

# 4 GRL-DP-SINK-BSX/DP-SINK Software Setup

## 4.1 Setup

This section provides procedures for installing, configuring and verifying the operation of the GRL-DP-SINK-BSX/DP-SINK automation software. It also helps you familiarize yourself with the basic operation of the application.

The software installer automatically creates shortcuts in the Desktop and Start Menu.

To open the application, follow the procedure in the following section.

### 4.1.1 Download GRL-DP-SINK-BSX/DP-SINK Software

Download and install the GRL-DP-SINK-BSX/DP-SINK software on a PC or an oscilloscope (where GRL-DP-SINK-BSX/DP-SINK software is referred to as 'Controller PC' or 'Scope' respectively in this User Guide & MOI):

1. Install VISA (Virtual Instrument Software Architecture) on to the PC/Scope where GRL-DP-SINK-BSX/DP-SINK is to be used (see Section 3.1).
2. Download the **DPSinkTest14VX.XX.XX.zip** package from Granite River Labs support site.
3. The ZIP file contains:
  - a) **DPSink14PatternFilesInstallation00xxxxxxxSetup.exe** – Run this on the BERTScope to install the DisplayPort 1.4 test pattern setup files. This will place the DisplayPort Configuration and Pattern files on the BERTScope in the 'D:\' directory hierarchy.
  - b) **DPSinkTest14Application14xxxxxxxSetup.exe** – Run this on the Controller PC or Oscilloscope to install the GRL-DP-SINK-BSX/DP-SINK application. This application will create the 'C:\GRL\Rx Test Solution\Applications\DPSinkTest14' directory hierarchy.
  - c) **DPSinkTest14ScopeSetupFilesInstallation00xxxxxxxSetup.exe** – Run this on the Oscilloscope to install the DPOJET setup files. This will place the DisplayPort Setup and Filter folders in the 'C:\TekApplications\DPOJET' directory hierarchy.

### 4.1.2 Launch and Set Up GRL-DP-SINK-BSX/DP-SINK Software

#### 4.1.2.1 On the BERTScope

1. Select **View > System > Tools Tab**.
2. Under **Utilities** Column, select the Remote button.
3. In Remote Client window, select **TCP/IP**.
4. Change **Terminator** to "LF". Select the **Connect** Button.

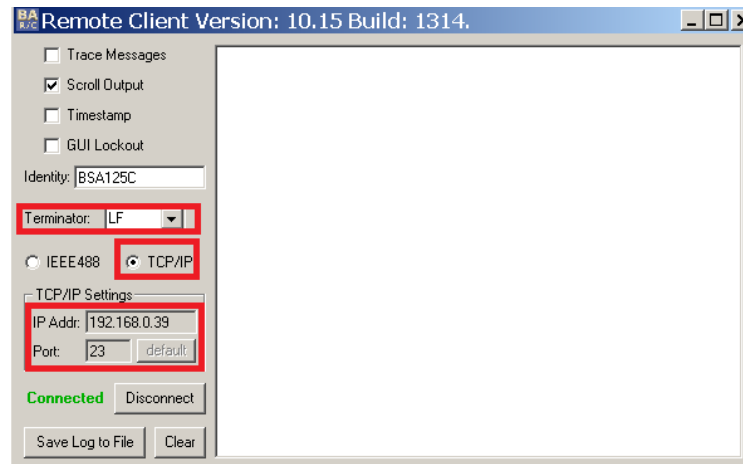


FIGURE 1. REMOTE CLIENT WINDOW

*Note: If you see an error pop-up when selecting the Connect button, try a different Port. For example, change Port 23 to 21.*

5. Note the IP Address and Port # on Remote Client. They will be needed to connect the BERTScope to the GRL automation software.
6. Minimize, but do not close, the *Remote Client* window.

#### 4.1.2.2 On the PC Used for GRL Framework Installation

1. Navigate to Start Menu > All Programs > GRL > GRL - Automated Test Solutions.

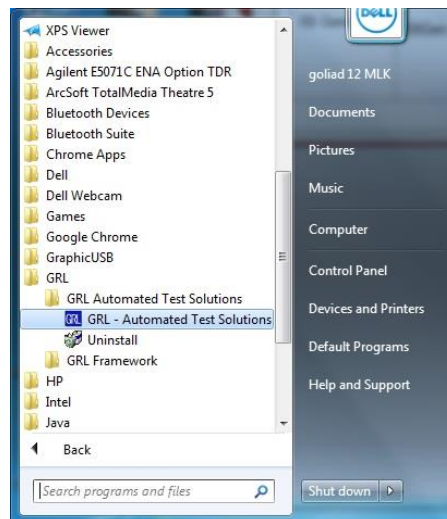


FIGURE 2. GRL AUTOMATED TEST SOLUTIONS IN START MENU

2. Click Application > Rx Test Solution > DisplayPort Sink Test 1.4 to open the application.



FIGURE 3. RX TEST SOLUTIONS IN GRL AUTOMATED TEST SOLUTIONS WINDOW

3. To enable license, go to License > License Details. The following dialog will pop up.

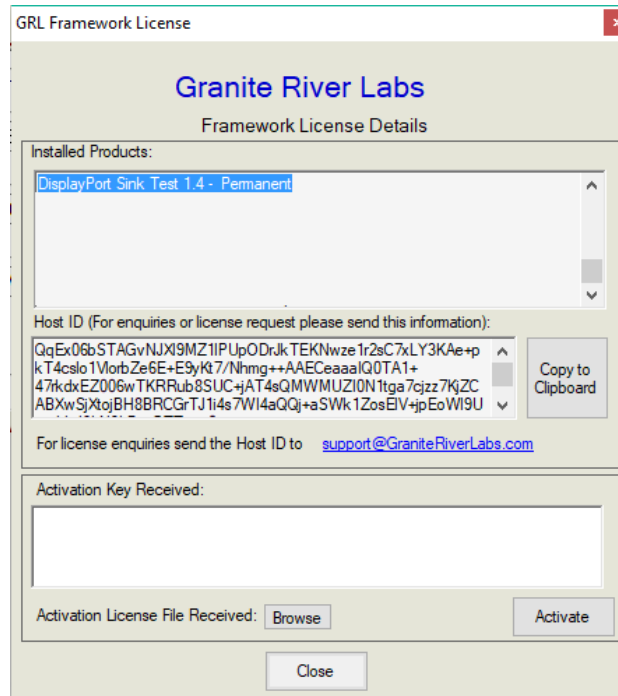



FIGURE 4. LICENSE DETAILS WINDOW

4. Activate License:
  - a) If you have an Activation Key, please enter in the box provided and select **Activate**.
  - b) If you do not have an Activation Key, select **Close** to use the software for 10 Days free of charge.

**Note:** Once the 10-day trial times out, you will need to request an activation key for future usage on the same computer or oscilloscope. The demo software is also limited in its capability in that it will only calibrate the maximum frequency for each data rate. Thus, the demo version cannot be used to fully calibrate and test a device. For Demo and Beta Customer License Keys, please request a License key by contacting [support@graniteriverlabs.com](mailto:support@graniteriverlabs.com).

5. Click on Equipment Setup icon  on the GRL Framework.
6. Enter the BERTScope IP address and Port number to match what is in the BERTScope *Remote Client* window shown in Section 4.1.2.1.

- Enter the Scope GPIB/IP Address. If the GRL software is installed on the Scope, ensure the Scope is connected via GPIB and type in the GPIB network address, for example “GPIB8::1::INSTR”. If the GRL software is installed on the PC to control the Scope, enter the Scope IP address, for example “TCPIP0::192.168.0.110::inst0::INSTR”. Note to **omit** the Port number from the address.

*(Note: The Scope IP address can be obtained, if not known, by typing CMD → IPCONFIG on the scope and observe the IP address listed.)*

- Enter the COM Address of the ISI Generator to be used.



FIGURE 5. EQUIPMENT SETUP WINDOW – VIEW #1

- Check the connection for each instrument by clicking the “lightning” ⚡ button. The “lightning” button should turn green if the connection has been verified.

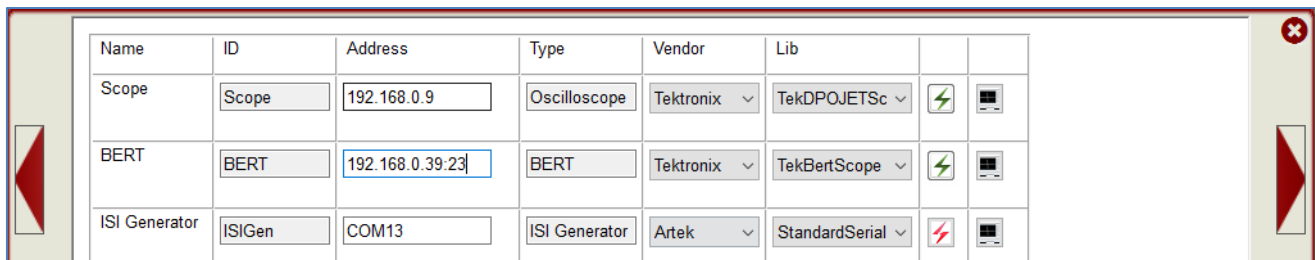


FIGURE 6. EQUIPMENT SETUP WINDOW – VIEW #2

*Additional notes:*

- Further information for connecting the Tektronix oscilloscope to the PC is provided in the Appendix of this document.
- The USB driver software for the ARTEK ISI Generator must be installed on the PC being used for testing, and the ISI generator must be connected to the PC via USB. The driver for the ISI generator is available from the ISI generator manufacturer. Refer to Appendix for the driver installation information.



## 4.2 Configuring the Software Before Calibration and Testing

### 4.2.1 Session Info

The information provided will be included in the report.

The **DUT Info** and **Test Info** are input by the user.

The **Software Info** is automatically populated.

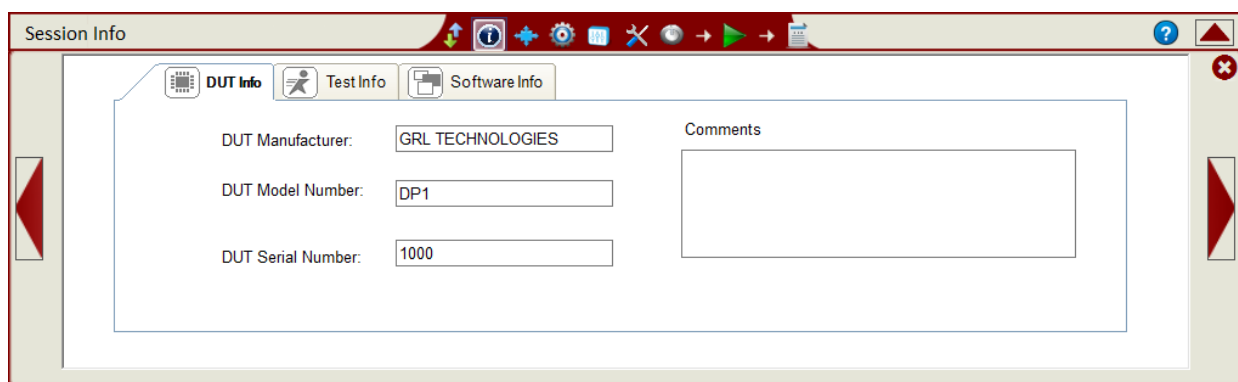



FIGURE 7. SESSION INFO

### 4.2.2 Conditions for Testing and Calibration

In this section, conditions for Testing and Calibration will need to be set. User selects Conditions  for testing and for calibration.

When calibrating, the application will calibrate for the selected Lanes, Test Points, Data Rates and Frequencies. The application will perform testing at these selected Lanes, Test Points, SSC Capabilities, Data Rates and Frequencies.

Recommended procedure:

- *Step 1:* When calibrating, select the desired conditions and perform the calibration tests.
- *Step 2:* When ready for testing, re-select the desired test conditions. For example, if required to test only one Lane at one Frequency for the RBR Data Rate, then select the appropriate conditions for testing.

a) **Lane tab:** Select the desired Lanes for calibration or testing.

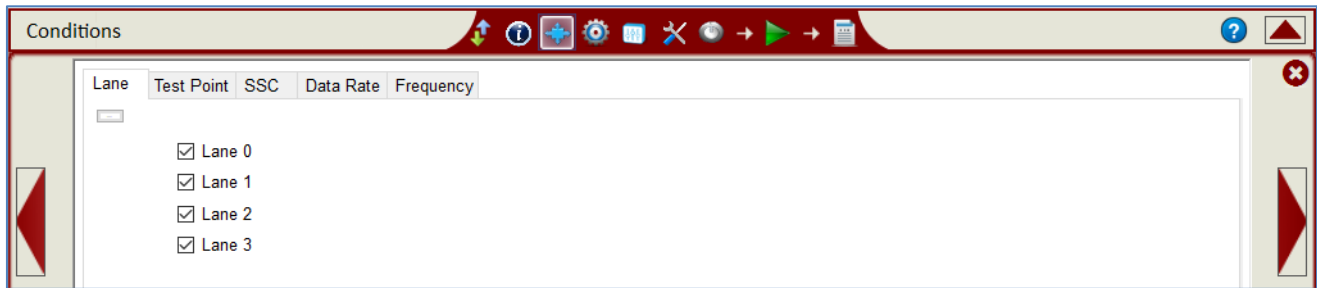


FIGURE 8. SELECT LANE UNDER TESTS

- b) **Test Point tab:** Select the test points for calibration and testing. Note 'TP2 CTLE Long' and 'TP2 CTLE Short' represent the TP2\_CTLE test points for Long and Short Channel measurements of the HBR3 Tethered cable DP Sink Device respectively.

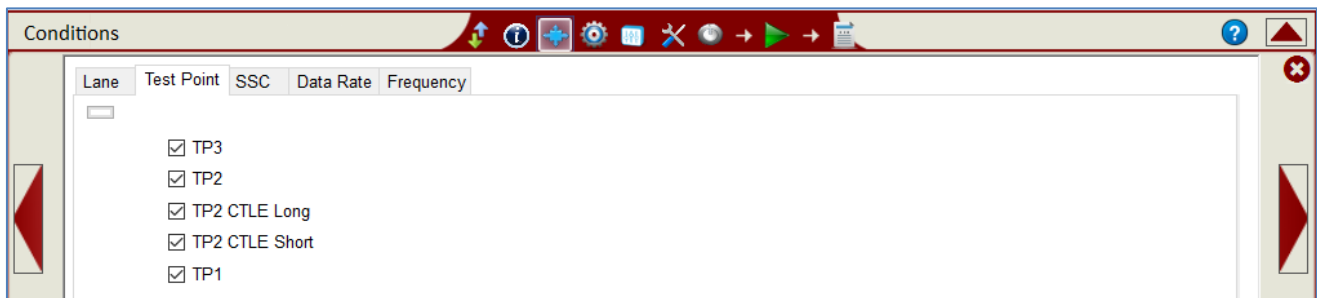


FIGURE 9. SELECT TEST POINTS

- c) **SSC tab:** Select to enable or disable SSC Capability supported by the DUT for testing.

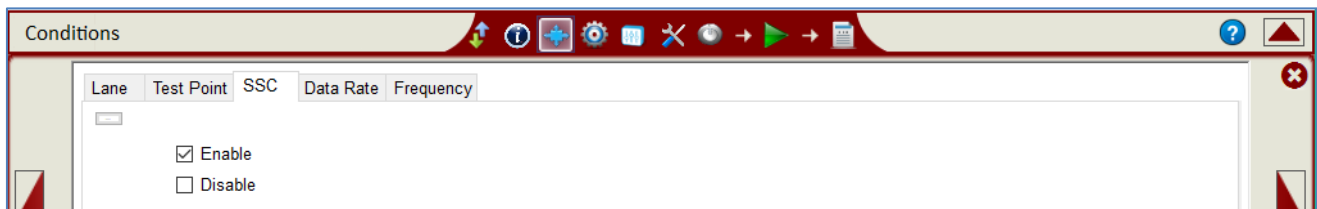


FIGURE 10. SELECT SSC CONDITION

- d) **Data Rate tab:** Select the desired data rates for calibration or testing.

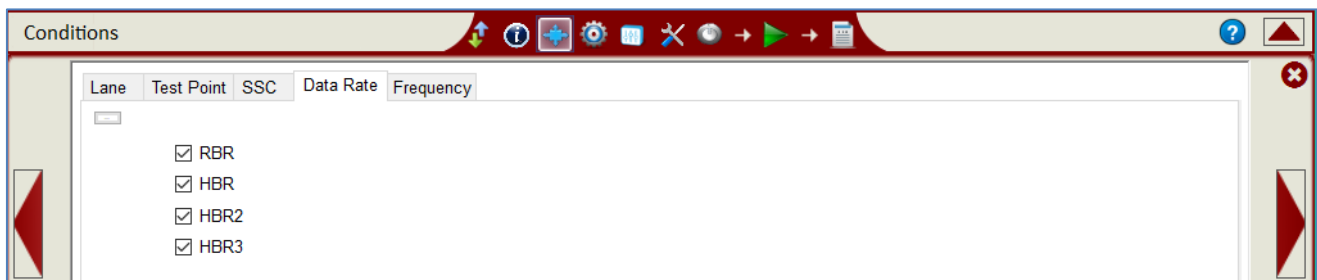


FIGURE 11. SELECT DATA RATES

e) **Frequency** tab: Select the desired SJ frequencies for calibration or testing.

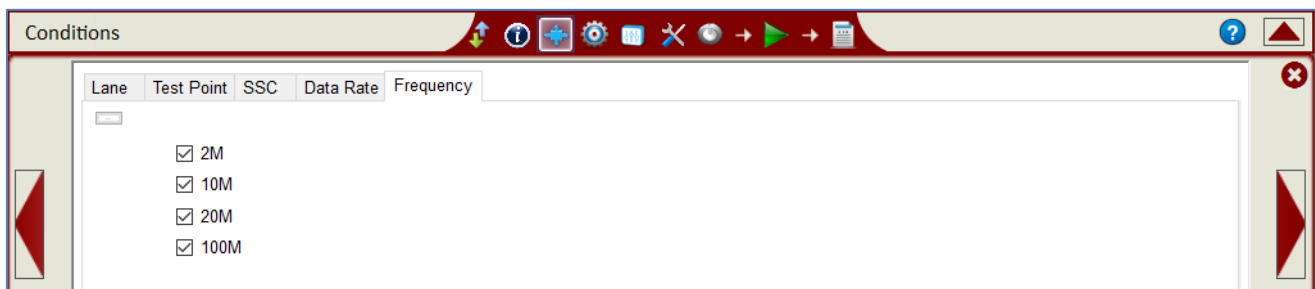



FIGURE 12. SELECT SJ FREQUENCIES

### 4.2.3 Setup Configuration for Testing and Calibration

Use the Setup Configuration  page to configure the necessary settings prior to running tests or calibration.

#### 4.2.3.1 Test Mode tab

Select to apply the Standard DisplayPort or 2+2 Alternate Mode test mode for calibration or testing.

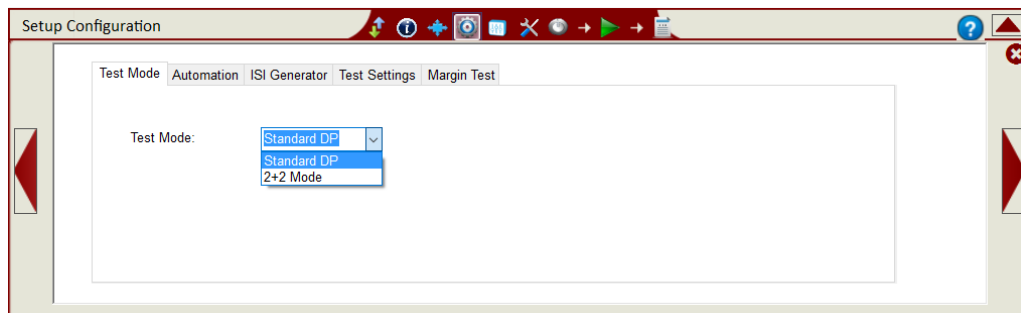


FIGURE 13. SELECT TEST MODE

#### 4.2.3.2 Automation tab

Select to use the GRL-USB-PD-C2 (GRL-C2) USB Type-C Power Delivery Tester, Tektronix DP Aux Controller, or Unigraf DPT-200 Aux Controller in the calibration or test setup. Select 'None' if not using an Aux Controller.

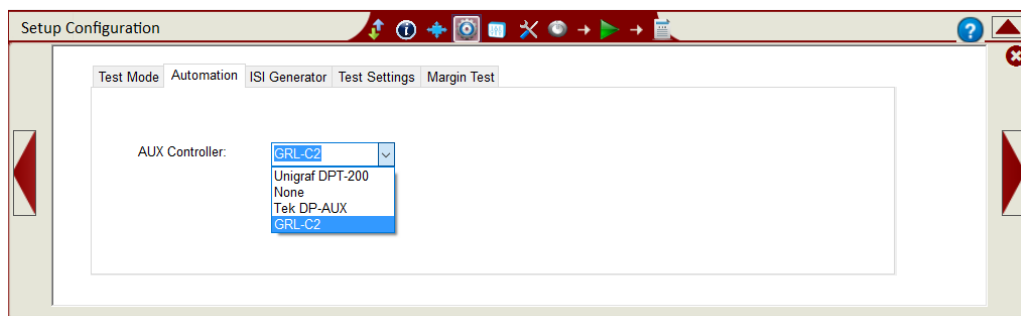


FIGURE 14. SELECT AUX CONTROLLER

#### 4.2.3.3 ISI Generator tab

Select the ISI Generator to be used in calibration or testing.

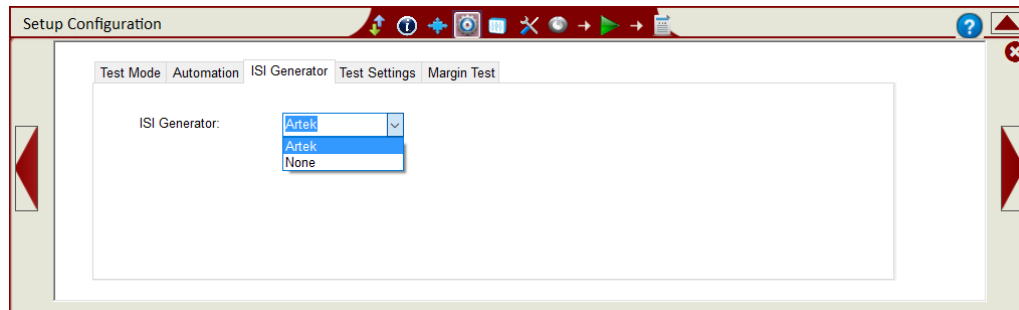


FIGURE 15. SELECT ISI GENERATOR

#### 4.2.3.4 Test Settings tab

Select the Symbol Lock Pattern. (Note: It is suggested to start with TPS2.) Also select the HBR2 Compliance Pattern and choose the option to enable the ESI Register.

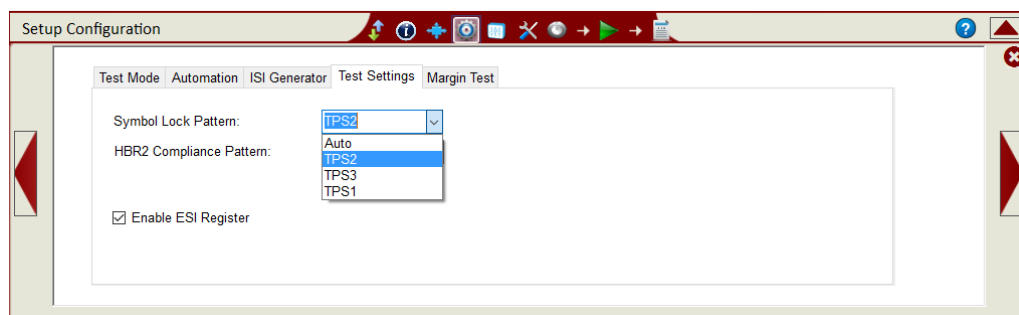


FIGURE 16. CONFIGURE TEST SETTINGS

#### 4.2.3.5 Margin Test tab

Configure the Search Mode Jitter Tolerance parameters for marginal testing. Also select the option to receive prompts to reset the DUT as required during testing.

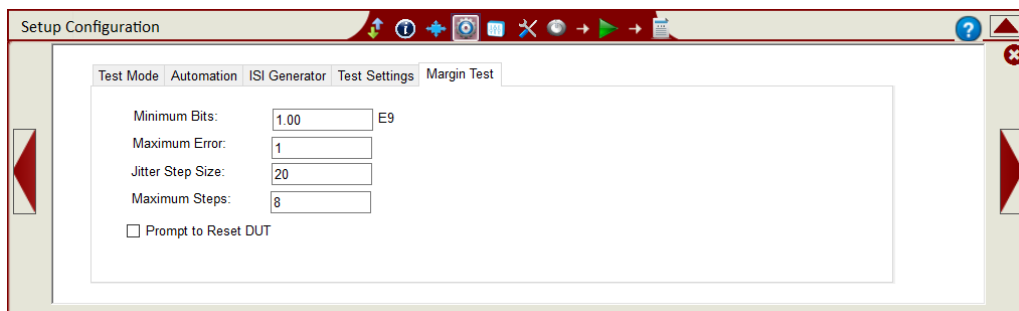



FIGURE 17. CONFIGURE MARGIN TEST PARAMETERS

### 4.3 Calibration/Test Selection Page

Select the  button in the main software menu to choose the calibration or tests to be performed on the **Select Tests** page. Initially, when starting for the first time or changing anything in the setup, it is suggested to run Calibration first. If the calibration is not completed, the Sink Tests will show an error message.

*Note: For calibration/testing, it is recommended to use a Variable ISI channel as it allows the channel to be more easily adjusted to meet the required specification. The application supports automated control of the ARTEK CLE1000-A2 variable ISI generator.*

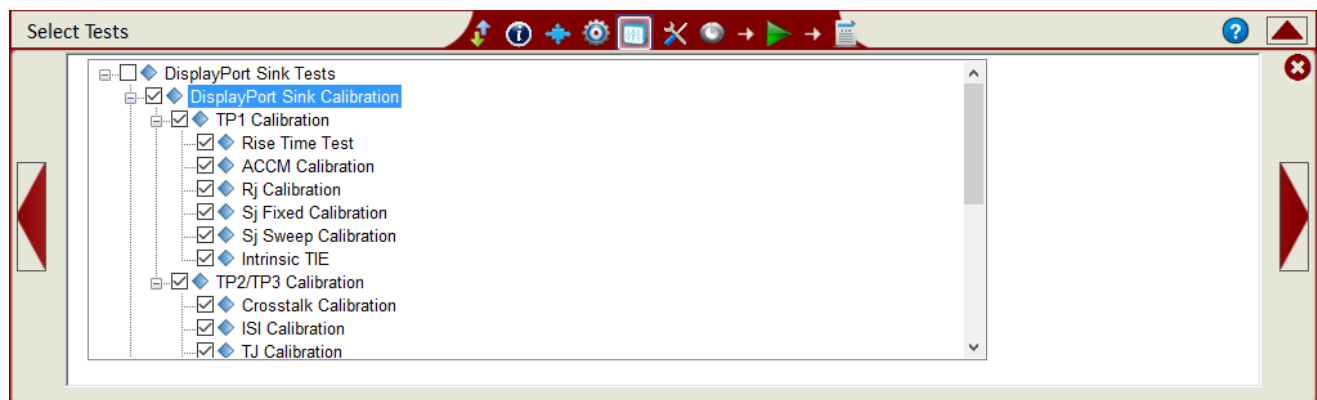


FIGURE 18. CALIBRATION SELECTION

Select the calibration groups to perform calibration for all DisplayPort Sink parameters. Note that while user can select individual calibration parameters, it is possible that a particular calibration may require the previous calibration to be completed before it can proceed. Thus, it is advisable to complete all previous calibration before going on to the next calibration.

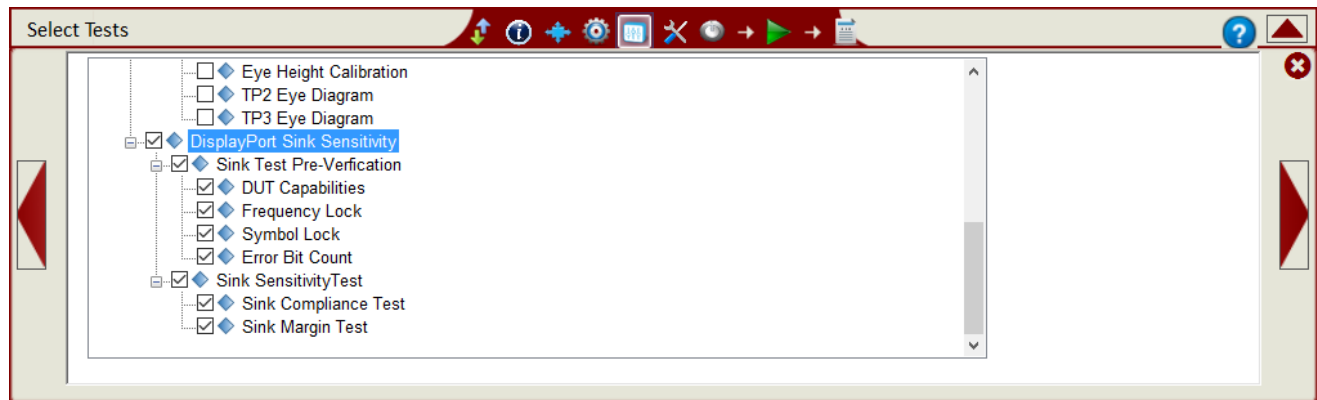



FIGURE 19. TESTS SELECTION

Select the test groups to perform DUT compliance tests for all DisplayPort Sink parameters.

*Note: The Sink Test Pre-Verification group is optional which when selected, performs “pre-test” link training before running the actual tests. These pre-verification tests are carried out mainly for debugging purposes and will not include any jitter tolerance testing.*

#### 4.4 Calibration/Test Parameters Configuration Page

Click the Configuration button  in the main software menu to access the Configurations page. Set all parameters for Sink calibration and testing as described in Table 3 below. To return all parameters to their default values, select the ‘Set Default’ button.

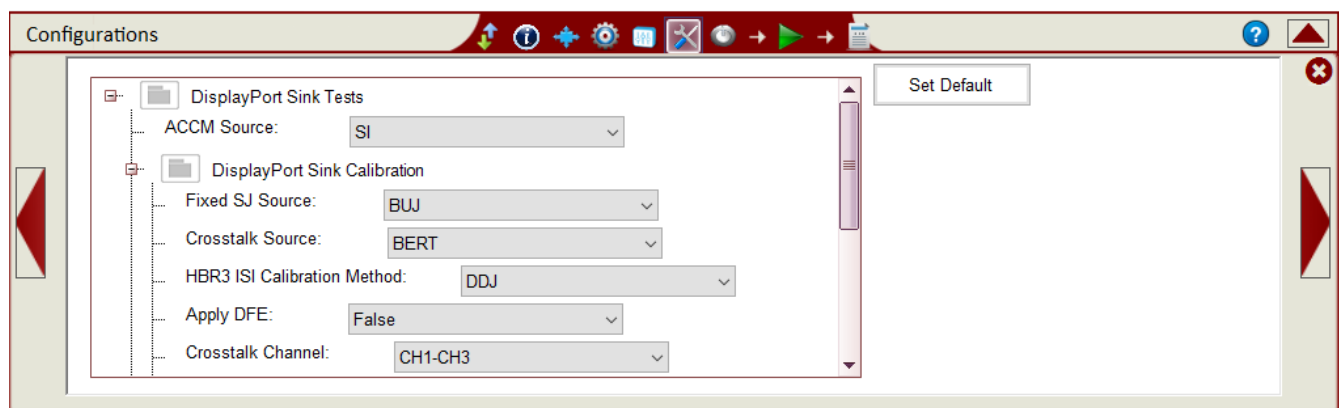


FIGURE 20. PARAMETERS CONFIGURATION PAGE

TABLE 3. CALIBRATION/TEST PARAMETERS DESCRIPTION

| Parameter Name         | Description   |
|------------------------|---|
| <b>ACCM Source</b>     | Select whether to manually set the ACCM source or apply the calibrated value from ACCM calibration.   |
| <b>Fixed SJ Source</b> | Select whether to use crosstalk Bounded Uncorrelated Jitter (BUJ) as the SJ <sub>FIXED</sub> source or apply the calibrated value from SJ Fixed calibration. <i>(Note: Only applicable for HBR2 and HBR3 data rates.)</i> |

|                                       |  |
|---------------------------------------|--|
| <b>Crosstalk Source</b>               | Select whether to use the BERTScope or an external source to generate crosstalk.   |
| <b>HBR3 ISI Calibration Method</b>    | Select whether to use the TIE Subtraction or DDJ method to calibrate ISI for HBR3 data rate.   |
| <b>Apply DFE</b>                      | Set to True to implement Decision Feedback Equalization (DFE) for the receiver to perform equalization on the decision threshold levels of the waveform. |
| <b>Crosstalk Channel</b>              | Select the channel pair to be connected for crosstalk source.  |
| <b>Data Channel</b>                   | Select the channel pair to be connected for data output.   |
| <b>Cable Model</b>                    | Select whether to use a Standard DisplayPort cable or a Type-C cable type for calibration.   |
| <b>HBR TP2 Calibration Test Point</b> | Select whether to use TP2 or TP3_EQ test point for calibrating for the HBR data rate.  |
| <b>PreEmphasis/Swing Loop Method</b>  | Select whether to use the incremental or DisplayPort Configuration Data (DPCD) register method for adjusting the Pre-emphasis and Swing voltage.         |
| <b>Reset Link Register</b>            | Set to True to perform link register reset during testing.   |
| <b>Test All Lanes with Lane 0 Cal</b> | Set to True to use the calibrated Lane 0 values to test for all lanes under test.  |

## 4.5 Calibration Target Configuration Page

User may change the calibration target value for any of the calibration items. By default, the target values are those defined in the specification. Change the values only when debugging.

To change the values, un-select the Use Default Value checkbox. Also at any point in time if the default values are required, just select the checkbox and the default values will replace all the current values.

*Note: The PID Control setting is used to adjust the step width for steps calculation if the target measurement cannot be met with the current step. To adjust, use a lower PID Control value to reduce the subsequent step or increase the control value to make the subsequent step bigger.*

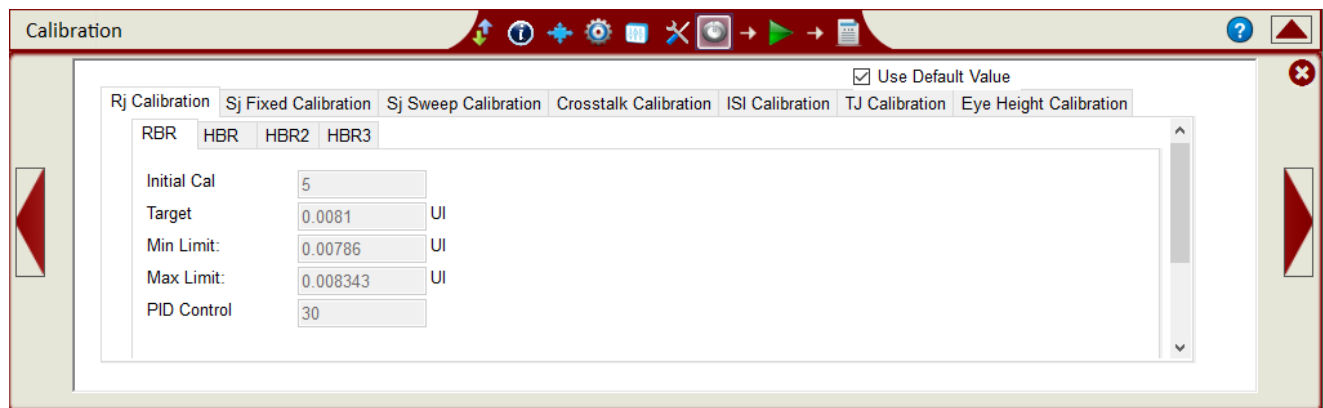


FIGURE 21. CALIBRATION OVERWRITE

## 4.6 Running the Calibration/Tests

From the pop-up menu, select the Run  icon to access the Run Tests page. Select the Run Option before clicking the Run Tests button to start calibration or testing.

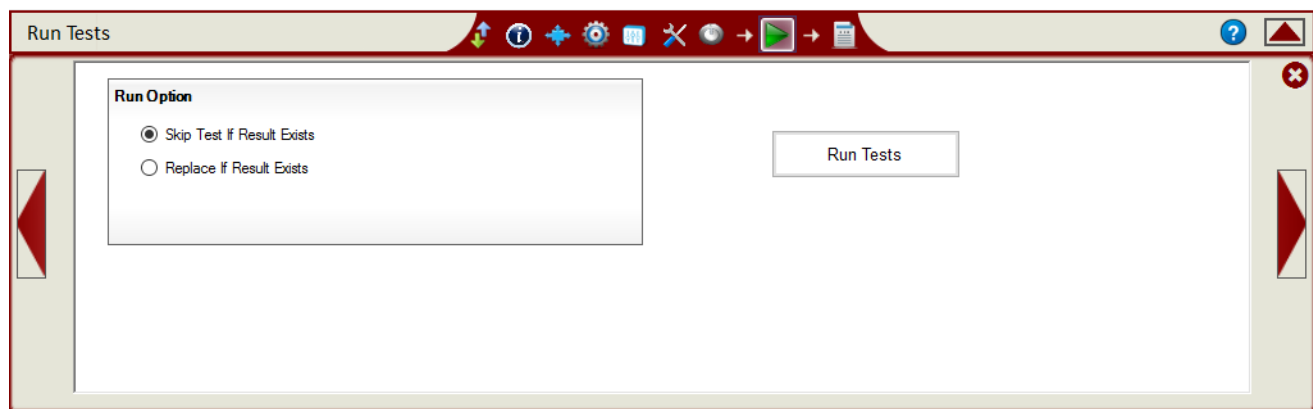


FIGURE 22. RUN TESTS PAGE

TABLE 4. RUN OPTIONS

| Parameter Name                    | Description  |
|-----------------------------------|--|
| <b>Skip Test if Result Exists</b> | If previous test or calibration results exists, then the software will <i>skip</i> the tests/calibration steps that have existing reports. |
| <b>Replace if Result Exists</b>   | If previous test/calibration results exist, then the software will replace each step in the test/calibration with new results.             |

If you need to re-run only certain test on certain conditions, please delete the tests from the Report tab and Run with **Skip Test if Result Exists**. GRL software will keep track of the missing tests in the report and perform those tests only. See Section 7 for more information on Test Reports.



## **5 Sink Calibration Setups**

This section shows the typical connection setups to perform automated Sink Test Calibration.

### **5.1 Pre-Calibration/Test Procedures**

Prior to running any calibration or test, the following steps must be taken to assure accurate measurements:

1. Allow a minimum of 20 minutes warm-up time for the Oscilloscope and BERTScope.
2. Run the scope's SPC calibration routine. It is necessary to remove all probes from the scope before running SPC.
3. Perform instrument calibration and deskew to compensate for skew between measurement channels per Tektronix user documentation on calibration.
4. Make sure you use a torque wrench with the proper torque specification to make all SMA connections.

### **5.2 Calibration Connection Setups**

*Note: Using a Variable ISI Generator enables calibration to be performed with minimum reconfiguration of the test setup, which allows testing to be more fully automated.*

### 5.2.1 Calibration Setup at TP1

Figure 23 below shows the typical setup for Sink signal calibration at Test Point 1.

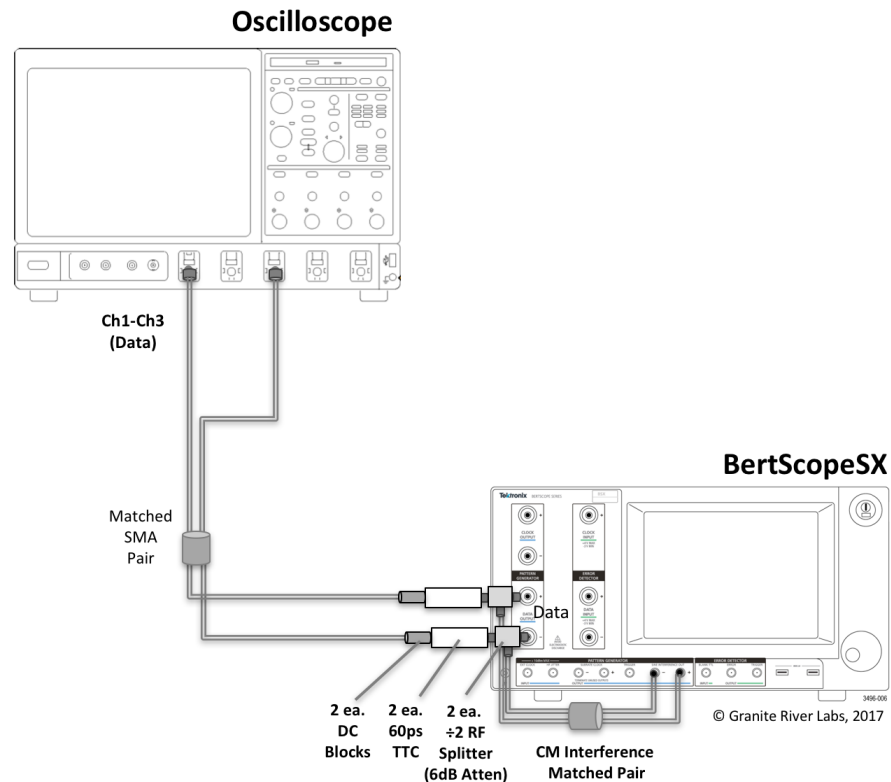


FIGURE 23. TYPICAL TP1 SINK CALIBRATION SETUP

Connect the DATA Outputs of the BERTScope directly to Channels 1 and 3 of the Oscilloscope.

### 5.2.2 Calibration Steps at TP1

The following table summarizes the DP1.4 PHY CTS steps and calibration target values for each data rate at TP1.

| Calibration Step                    | Unit | HBR3          | HBR2 | HBR | RBR |
|-------------------------------------|------|---------------|------|-----|-----|
| <b>Rise Time (20-80) [a]</b>        | ps   | 40            | NA   | NA  | NA  |
| TTC Value (10-90)                   | ps   | 60            | 60   | 60  | 60  |
| Pattern                             |      | 256 Bit Clock | NA   | NA  | NA  |
| <b>ACCM Calibration (pk-pk) [b]</b> | mV   | 100           | NA   | NA  | NA  |
| ACCM Pattern                        |      | Sine          | NA   | NA  | NA  |
| Frequency                           | MHz  | 400           | NA   | NA  | NA  |

|  |     |       |       |       |       |
|--|-----|-------|-------|-------|-------|
| <b>RJ Calibration (Amplitude RMS)</b> <sup>[c]</sup> | mUI | 13    | 16.7  | 13.5  | 8.1   |
| RJ Pattern   |     | D24.3 | D24.3 | D24.3 | D24.3 |
| <b>SJ Fixed Calibration (Amplitude pk-pk)</b>        | mUI | 130   | 80    | NA    | NA    |
| SJ Fixed Pattern                                     |     | D24.3 | D24.3 | NA    | NA    |
| SJ Fixed Frequency                                   | MHz | 297   | 297   | NA    | NA    |
| <b>SJ Sweep Calibration</b>                          |     |       |       |       |       |
| SJ Sweep Pattern                                     |     | D24.3 | D24.3 | D24.3 | D24.3 |
| 2 MHz SJ (Amplitude pk-pk)                           | mUI | 1013  | 505   | 904   | 981   |
| 10 MHz SJ (Amplitude pk-pk)                          | mUI | 137   | 116   | 225   | 111   |
| 20 MHz SJ (Amplitude pk-pk)                          | mUI | 109   | 104   | 182   | 80    |
| 100 MHz SJ (Amplitude pk-pk)                         | mUI | 100   | 100   | 168   | NA    |
| <b>SJ Sweep Calibration</b>                          |     |       |       |       |       |
| Intrinsic ISI Pattern                                |     | TPS4  | NA    | NA    | NA    |
| <b>TP1 TJ Calibration</b>                            | mUI | 430   | NA    | NA    | NA    |
| <b>TP1 Eye Height Calibration</b>                    | mV  | 280   | NA    | NA    | NA    |

<sup>[a]</sup> If testing only bit rates HBR2 and lower, Rise/Fall time is not calibrated and 60 ps (10-90) TTCs are not required.

<sup>[b]</sup> If testing only bit rates HBR2 and lower, ACCM signal is not required. Combiner is replaced by 6 dB Attenuator. If HBR3 is highest bit rate, ACCM Generator is turned off while testing HBR2, HBR, and RBR.

<sup>[c]</sup> RJ xxxxx.

### 5.2.3 Calibration Setup at TP2/TP3

Figure 24 below shows the typical setup for Sink signal calibration at Test Point 2 or 3 using the BERTScope as the crosstalk source.

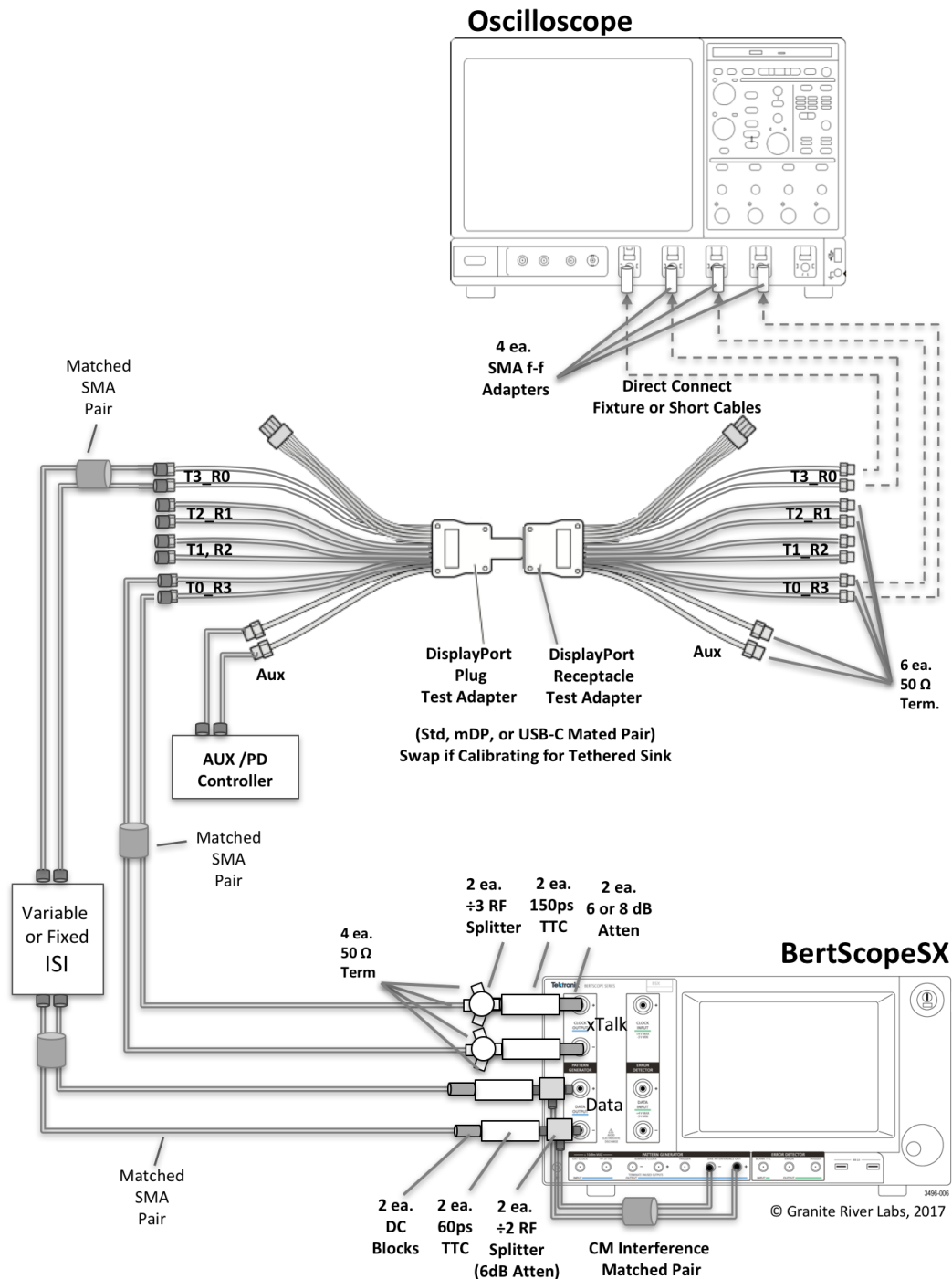


FIGURE 24. TYPICAL TP2/TP3 SINK CALIBRATION SETUP

Set up the equipment as shown in the above diagram. Connect the Clock Outputs of the BERTScope to the DP fixture and Scope. Connect the ISI Output to the selected Lane of the DP fixture and Scope.

#### 5.2.4 Calibration Steps at TP1, TP2, and TP3

The following table summarizes the DP1.4 PHY CTS steps and calibration target values for each data rate at TP1, TP2, and TP3.

| Calibration Step  | Unit | HBR3     | HBR2   | HBR    | RBR   |
|---|------|----------|--------|--------|-------|
| <b>Crosstalk</b>  | mV   | 300      | 300    | 450    | 138   |
| Pattern   | -    | D24.3    | D24.3  | D24.3  | D24.3 |
| TTC Value (10-90)                                       | ps   | 150      | 150    | 150    | 150   |
| <b>ISI &amp; TJ Data Pattern</b>                        | -    | TPS4     | CP2520 | PRBS7  | PRBS7 |
| <b>TP3 &amp; TP3_EQ ISI Calibration</b>                 | mUI  | 240      | 220    | 161    | 570   |
| Specified Test Point [a]                                | -    | TP3_CTLE | TP3_EQ | TP3_EQ | TP3   |
| <b>TP3_CTLE and TP3_EQ TJ Calibration [b]</b>           | mUI  | 600 [c]  | 600    | 471    | NA    |
| <b>TP3_CTLE, TP3_EQ, and TP3 Eye Height Calibration</b> | mV   | 50 [c]   | 100    | 160    | 46    |
| <b>TP2 ISI Calibration</b>                              | mUI  | 120      | NA     | 144    | 60    |
| Specified Test Point [d]                                | -    | TP2_CTLE | TP2    | TP2    | TP2   |
| <b>TP2_CTLE TJ Calibration</b>                          | mUI  | 480      | NA     | NA     | NA    |
| <b>TP2_CTLE Eye Height Calibration</b>                  | mV   | 170 [c]  | NA     | NA     | NA    |
| TP2_CTLE Short Channel [e]                              | mVpp | 250      | NA     | NA     | NA    |
| TP2_CTLE Long Channel [e]                               | mVpp | 170      | NA     | NA     | NA    |

[a] Notes about TP3 ISI Calibration:

- RBR ISI is measured directly without equalizer function applied.
- HBR and HBR2 are measured at TP3 with equalizer function in the scope for single TP3\_EQ function in the spec.

- *HBR3: TP3\_CTLE calibration shall be done using CTLE curve with -8 dB Adc. Physical measurement of the end-to-end ISI should be made to verify that it is within 22 to 24 dB insertion loss, including all cables, fixtures, and DC blocks.*

*[b] HBR3:  $S_{J_{FIXED}}$  is adjusted during calibration to achieve target TJ. TJ measurement for HBR2, HBR, or RBR is not performed directly. It is achieved by summation of measured jitter components.*

*[c] Eye Height Calibration target of 50 mV @TP3\_CTLE or 170 mV @TP2\_CTLE is achieved without crosstalk applied and will be reduced to approximately 40mV or 160mV respectively with crosstalk applied. HBR3 TJ is measured at TP3\_CTLE after the PLL transfer function over  $10^{-6}$  BER.*

*[d] Notes about TP2 ISI Calibration:*

- *RBR and HBR ISI are measured directly at TP2 without equalizer function applied.*
- *HB2 is measured with embedded S-parameter of HBR2 WC cable in place of HW ISI. This results in proper ISI being calibrated at TP2 when calibration fixture is removed.*
- *HBR3: TP2\_CTLE calibration shall be done using CTLE curve with -4dB Adc.*

*[e] Notes about TP2\_CTLE Short/Long Channel Eye Height Calibration:*

- *Only applicable for the HBR3 Tethered cable DP Sink Device to be measured at TP2\_CTLE.*
- *Below shows the CTS illustrated typical test setups for both Long and Short Channels.*
- *The Long Channel receiver for a tethered DP Sink device is tested to determine if the receiver can operate correctly with reduced amplitude signals due to a lossy source channel.*
- *The Short Channel receiver for a tethered DP Sink device is tested to determine if the receiver can operate correctly with a larger amplitude signal presented to the system connector.*

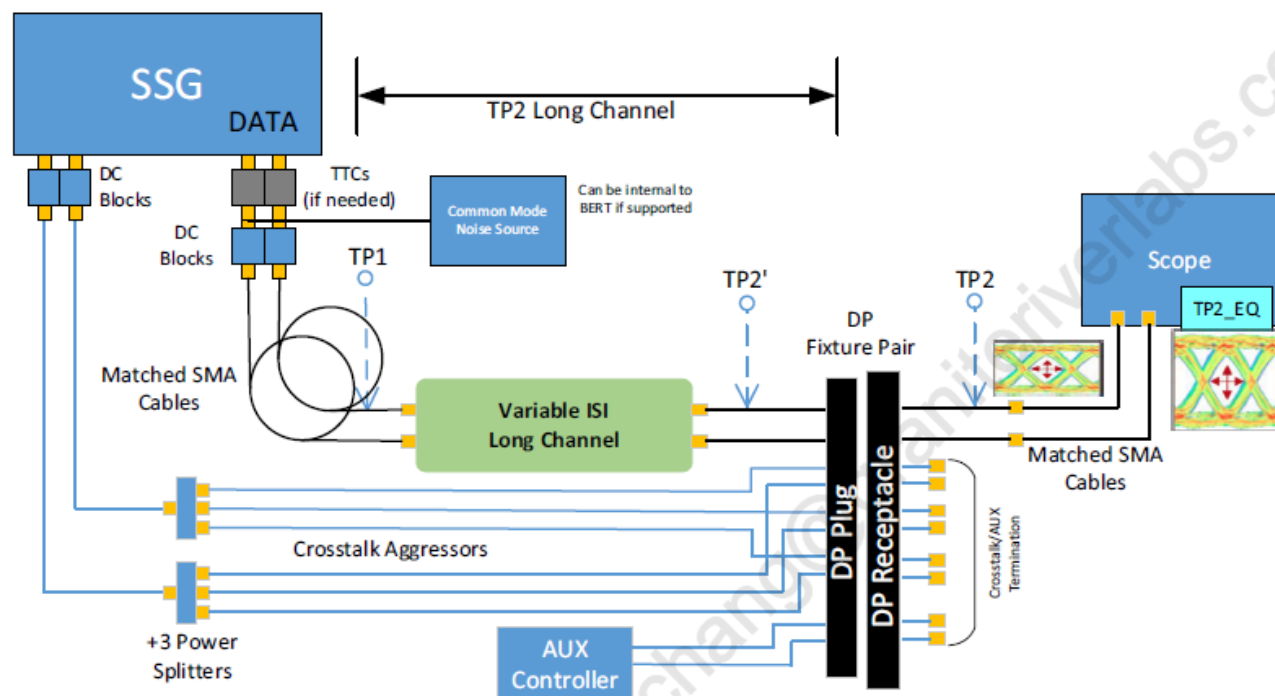


Figure 8-2: Tethered Long Channel DP Sink Device and Test Equipment Connection

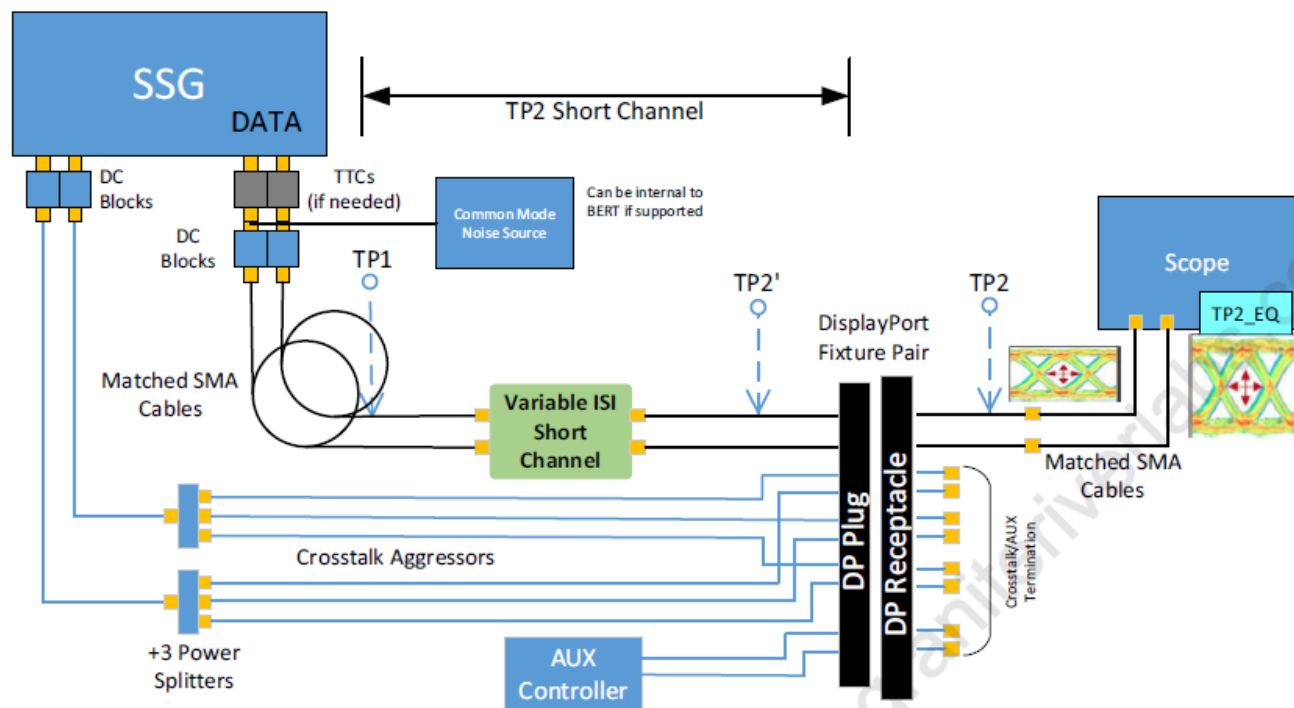


Figure 8-3: Tethered Short Channel DP Sink Device and Test Equipment Connection

### **5.3 Saving Calibrated Signals**

The application will save calibration files of calibrated stressed signals when running the calibration sequence. For example, on the BERTScope, the application will save the final configuration for LANE0-HBR2 to a file called *EYEHEIGHTCALIBRATION\_LANE0\_HBR2.CFG*.

This is the basic calibration file that will be recalled during testing.



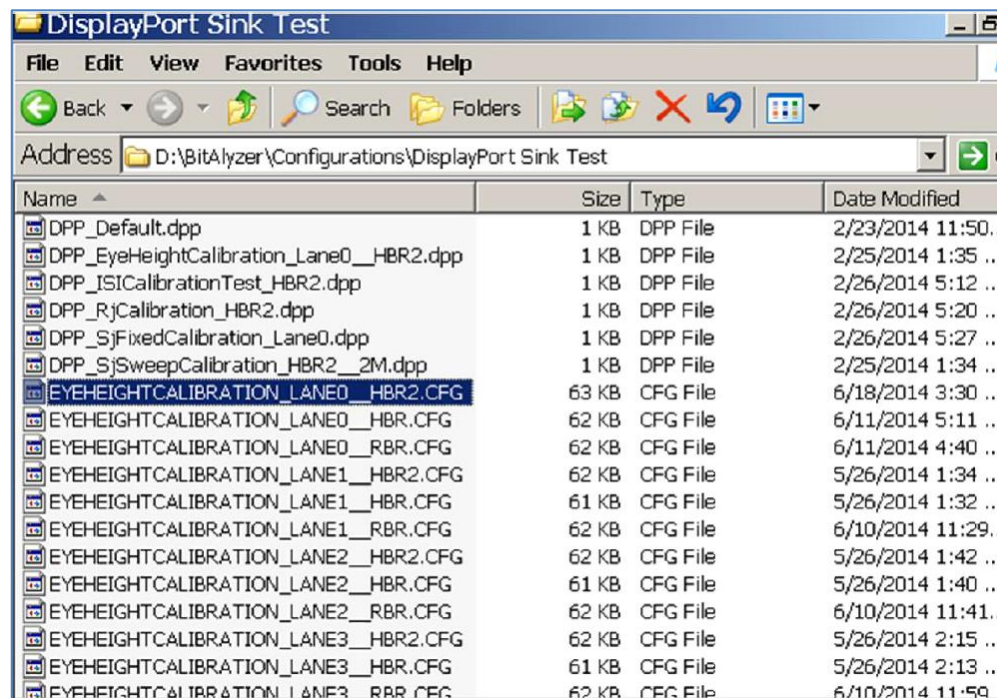


FIGURE 25. SAVED CALIBRATION FILE EXAMPLE

On the PC or Scope running the GRL application, a *calibration.cal* file will be created that contains the stored calibration values for each frequency that was calibrated.

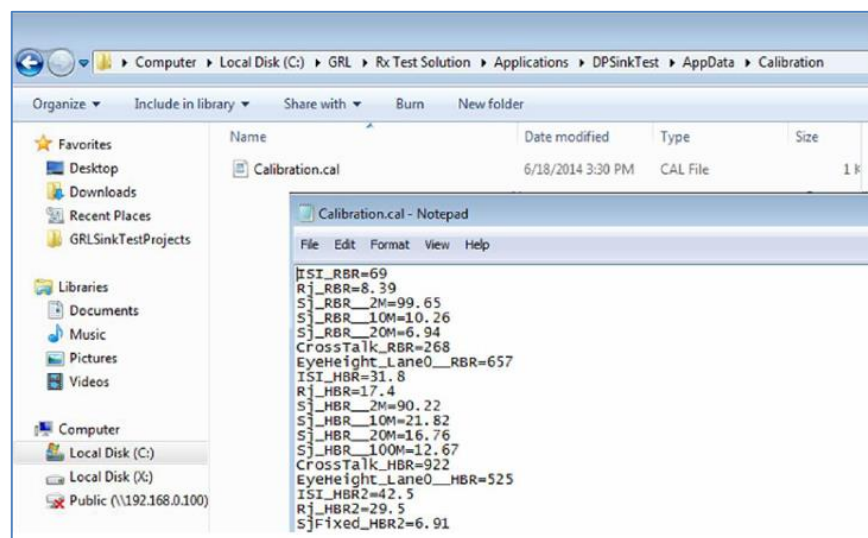


FIGURE 26. CALIBRATION.CAL FILE EXAMPLE

## 6 Sink DUT Compliance Test Setups

After calibration has completed, then testing the DP Sink DUT for CTS compliance can be performed. The GRL application supports automated testing of a DP Sink device if the device

supports standard DPCD through the AUX channel. *Note: The Aux controller is required for testing.*

## 6.1 Test Connection Setups

### 6.1.1 DUT Jitter Tolerance Compliance Test Setup

Figure 27 below shows the physical setup for the DP Sink DUT jitter tolerance test using the BERTScope as the crosstalk source.

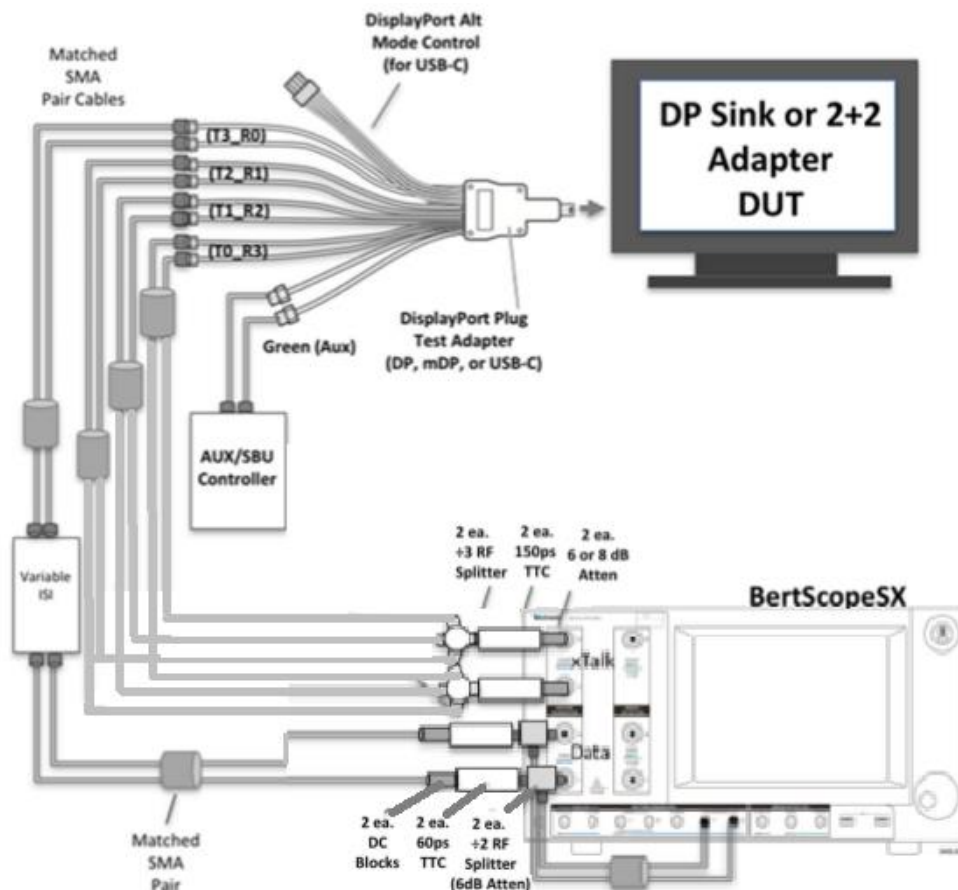


FIGURE 27. COMPLIANCE TEST SETUP FOR DP SINK DUT JITTER TOLERANCE

Set up the equipment as shown in the above diagram. Disconnect the 'P' (Plug) type adapter from the 'R' (Receptacle) calibration adapter and connect the 'P' type adapter to the DUT for testing. Change the connection from the ISI Output to the selected Lane under test of the DP fixture.

*Note: If the Unigraf DPT-200 Aux controller is used, an additional DP-Cable to AUX-SMA adapter is required. The Tektronix DP-AUX is connected directly to the DUT via SMAs. Both Aux control solutions have USB connection and drivers that need to be loaded on the Computer being used for the testing.*

General procedure to perform testing using the application:

- a) Select the “Sink Test Pre-Verification” test group to perform pre-test link training on the DUT. The tests under this group will train the DUT into test mode for receiver testing. This is mainly performed for debugging purposes. *Note: Any individual test from the group is also allowed to be selected as desired.*

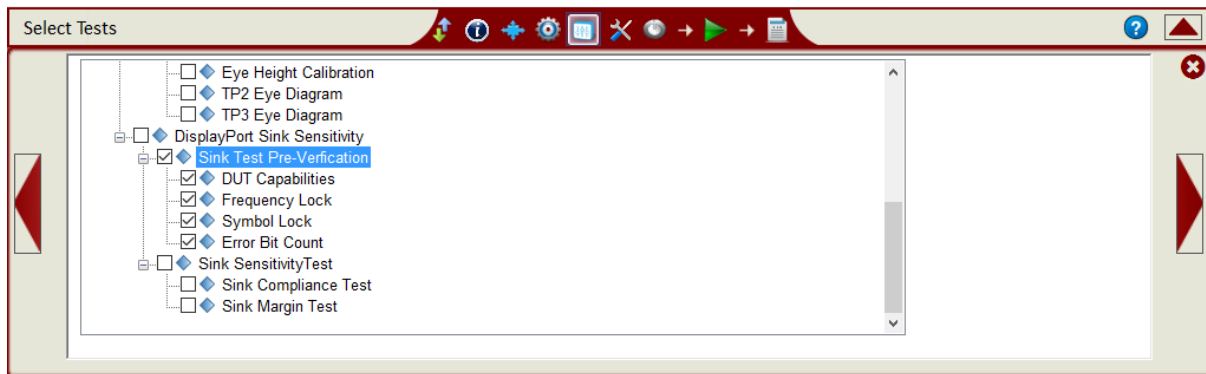


FIGURE 28. SINK TEST PRE-VERIFICATION SELECTION

|                  |   |
|------------------|---|
| DUT Capabilities | Lists the DUT capabilities in the Results window under the Report page.   |
| Frequency Lock   | Loads the Frequency Lock pattern on the BERTScope and verifies the Frequency Lock.  |
| Symbol Lock      | Loads the Symbol Lock pattern on the BERTScope and verifies the Symbol Lock.  |
| Error Bit Count  | Sends a random number of errors (1 to 5) from the BERTScope to the DUT, which then checks the DUT’s error count registers and confirms that the error counter is working correctly. |

- b) Select the “Sink Compliance Test”. The GRL application will perform link training followed by running the jitter tolerance compliance test at selected frequencies.

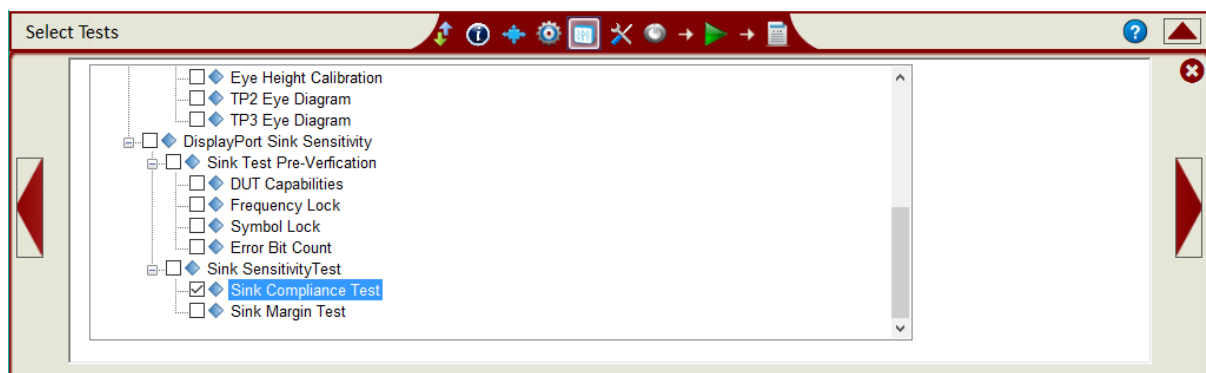


FIGURE 29. SINK COMPLIANCE TEST SELECTION

*Note: If running only a specific test, select only that test, e.g., Sink Compliance Test. If other tests/calibration that come before the desired test are selected, the application will complete those tests first following the sequence before running the desired test.*

c) Below shows the required test parameters for BER measurement from the CTS.

Table 4-3: BER Measurement Test Parameters

| Jitter Frequency (MHz) | Number of Bits   | Maximum Number of Allowable Bit Errors | Bit Rate | Observation Time (Seconds) <sup>a</sup> | Data Rate Offset |
|------------------------|------------------|--|----------|---|------------------|
| 2                      | 10 <sup>12</sup> | 1000                                   | HBR3     | 123                                     | 0                |
|                        |                  |  | HBR2     | 185                                     |                  |
|                        |                  |  | HBR      | 370                                     |                  |
|                        |                  |  | RBR      | 620                                     |                  |
| 10                     | 10 <sup>11</sup> | 100                                    | HBR3     | 13                                      | +350ppm          |
|                        |                  |  | HBR2     | 19                                      |                  |
|                        |                  |  | HBR      | 37                                      |                  |
|                        |                  |  | RBR      | 62                                      |                  |
| 20                     | 10 <sup>11</sup> | 100                                    | HBR3     | 13                                      | 0                |
|                        |                  |  | HBR2     | 19                                      |                  |
|                        |                  |  | HBR      | 37                                      |                  |
|                        |                  |  | RBR      | 62                                      |                  |
| 100                    | 10 <sup>11</sup> | 100                                    | HBR3     | 13                                      | 0                |
|                        |                  |  | HBR2     | 19                                      |                  |
|                        |                  |  | HBR      | 37                                      |                  |

a. To evaluate, the number of bits shall be multiplied by the unit interval (UI) in picoseconds (e.g., for HBR, 10<sup>11</sup> bits at HBR = 370ps/UI × 10<sup>11</sup>UI = 37 seconds).

FIGURE 30. TEST PARAMETERS FOR BER MEASUREMENT

d) Once testing is completed, repeat the test for each Lane supported by the DUT.

*Note: The link width and highest supported Link Frequency are determined by selecting “DUT Capabilities” under Sink Test Pre-Verification and then running the test.*

*Note: As DUTs may behave differently during testing, it is recommended to always reset the DUT before each test sequence.*

### 6.1.2 Margin Testing

While it is sufficient to perform the Compliance Test for each test condition to meet compliance specifications, it is also useful to determine how much Margin your design contains.

The Margin for each test condition can be verified as follows:

a) Under the Setup Configuration page, select the **Margin Test** tab.

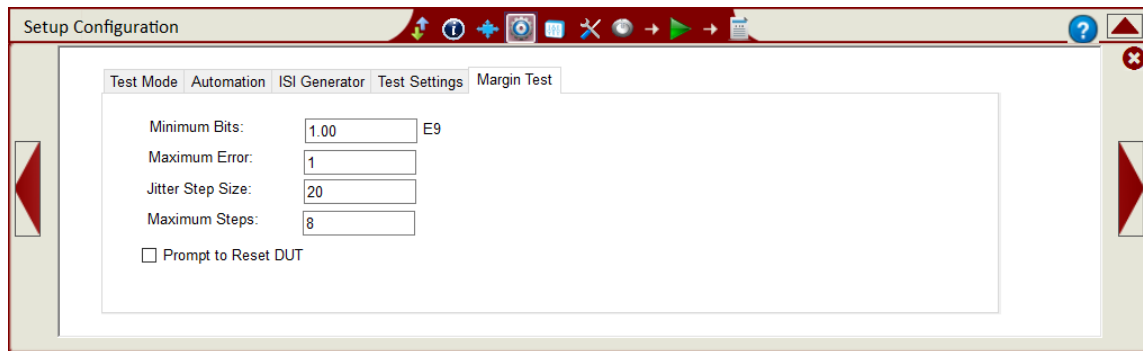


FIGURE 31. MARGIN TEST CONFIGURATION

b) For the desired Link Rate and Frequency pair, configure the following parameters:

- **Minimum Bits:** Minimum number of bits tested at each SJ amplitude.
- **Maximum Error:** Maximum number of errors allowed at each swept-SJ amplitude.
- **Jitter Step Size:** The swept-SJ amplitude will increase by the selected amplitude during testing. For example, if the initial swept-SJ is 100mUI, then the test points would be 100mUI, 120mUI, 140mUI, 160mUI, etc.
- **Minimum Steps:** Minimum number of steps to be implemented for margin testing.

c) Once configured, select and run the “Sink Margin Test” for the selected Link Rate/Frequency pair.

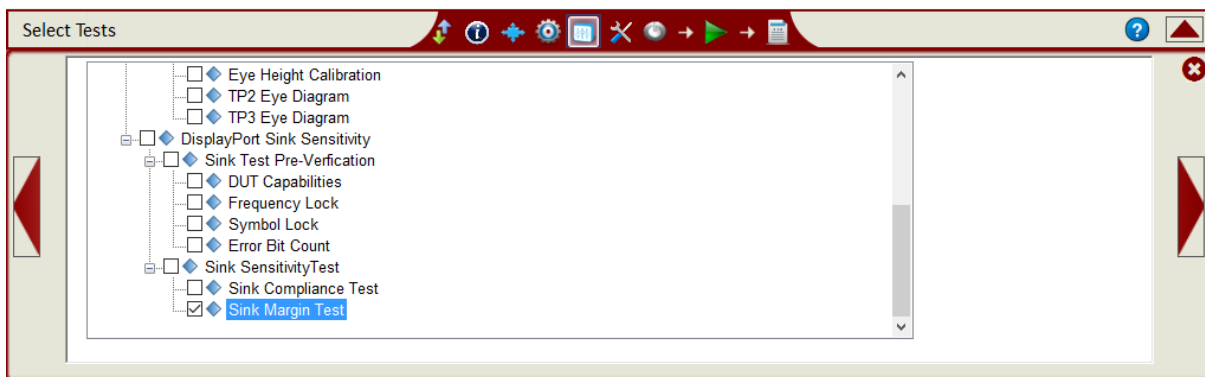



FIGURE 32. SINK MARGIN TEST SELECTION

*Note: If running only a specific test, select only that test, e.g., Sink Margin Test. If other tests/calibration that come before the desired test are selected, the application will complete those tests first following the sequence before running the desired test.*

## 7 Test Results and Reports Using GRL-DP-SINK-BSX/DP-SINK Software

The **Report**  page displays the results from all calibration and test runs. If some of the results are not desired, they can be individually deleted by using the **Delete** button. Also for a PDF report, click the **Generate report** button. To have the calibration data plotted in the report, make sure the **Plot Calibration Data** box is checked.

### 7.1 Test Report Generation

Click the **Generate report** button for the detailed calibration and tests report.

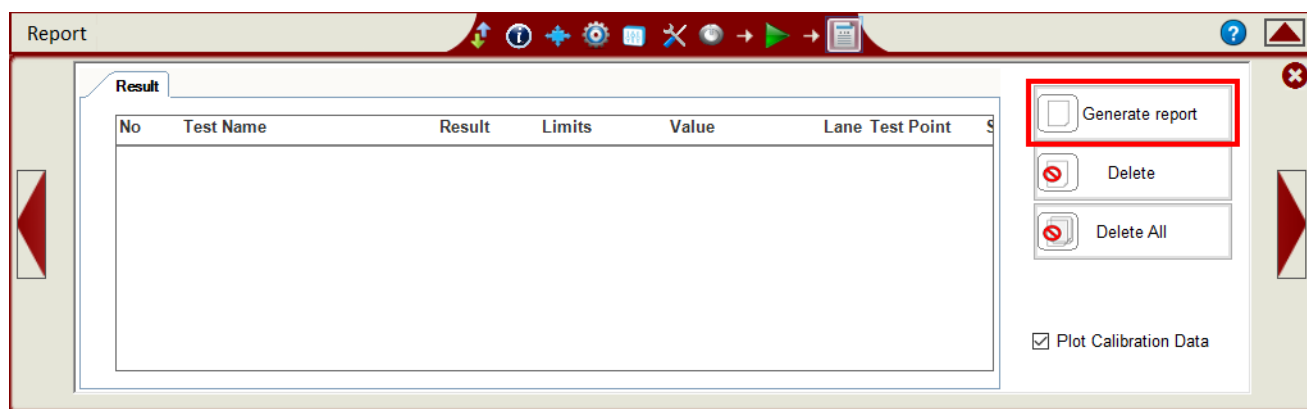


FIGURE 33. GENERATE REPORT PAGE

### 7.1.1 DUT Information

This portion is populated from the information in the DUT tab on the **Session Info** page.


DisplayPort Sink Test 1.4 Report

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### DisplayPort Sink Test 1.4 Report

**DUT Information**

DUT Manufacturer : DisplayPort Display Company

DUT Model Number : Ultra-Cool DP Sink

DUT Serial Number : 001001

**Tester Information**

Test Lab : GRL

Test Engineer : GRL ENG

Test Date : 01/16/2014

**SW Versions**

Software Revision : 0.08.000.001

BERTScope FW Revision : 10.15

Oscilloscope FW Revision : 6.4.0

DPOJET Revision : 6.0.1 Build 8

FIGURE 34. DUT INFORMATION

### 7.1.2 Summary Table

This portion is populated from the calibration and tests performed, which gives an overall view of all the results and test conditions.

| No | TestName             | Limits     | Value | Results | Lane  | Test Point | SSC    | Data Rate | Frequency |
|----|----------------------|------------|-------|---------|-------|------------|--------|-----------|-----------|
| 1  | Rise Time Test       | True/False | True  | Pass    | Lane0 | TP1        |        | HBR2      | 2M        |
| 2  | ACCM Calibration     | True/False | True  | Pass    | Lane1 | TP1        |        | HBR3      | 2M        |
| 3  | Rj Calibration       | True/False | True  | Pass    | Lane0 | TP1        | SSC_ON | HBR2      | 10M       |
| 4  | Sj Fixed Calibration | True/False | True  | Pass    | Lane0 | TP1        | SSC_ON | HBR3      | 100M      |

FIGURE 35. SUMMARY TABLE

### 7.1.3 Test Results

This portion is populated from each of the test results. Here the results are explained in depth with supporting data points and screenshots.



### 7.1.3.1 Compliance Test

This portion is populated from the results of all compliance tests performed.

#### Compliance Test(TP2,Enable,HBR2)

| Sj Frequency | 2M      | 10M     | 20M     | 100M    |
|--------------|---------|---------|---------|---------|
| Lane0        | PASS(0) | PASS(0) | PASS(0) | PASS(0) |
| Lane1        | PASS(0) | PASS(0) | PASS(0) | PASS(0) |
| Lane2        | PASS(0) | PASS(0) | PASS(0) | PASS(0) |
| Lane3        | PASS(0) | PASS(0) | PASS(0) | PASS(0) |

#### Compliance Test(TP2,Enable,HBR3)

| Sj Frequency | 2M      | 10M     | 20M     | 100M    |
|--------------|---------|---------|---------|---------|
| Lane0        | PASS(0) | PASS(0) | PASS(0) | PASS(0) |
| Lane1        | PASS(0) | PASS(0) | PASS(0) | PASS(0) |
| Lane2        | PASS(0) | PASS(0) | PASS(0) | PASS(0) |
| Lane3        | PASS(0) | PASS(0) | PASS(0) | PASS(0) |

FIGURE 36. COMPLIANCE TEST RESULTS PAGE

### 7.1.4 Calibration Data Plots

This portion is populated from each of the calibration steps. Below is an example of an ISI calibration plot showing the calibration points using the ARTEK CLE1000-A2.

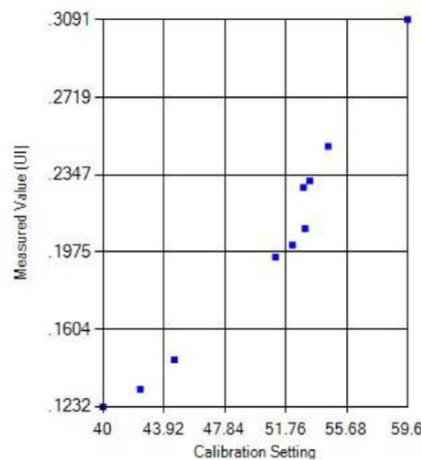


FIGURE 37. CALIBRATION RESULTS PAGE

### 7.1.5 Margin Test Plots

This portion is populated from the Margin Tests. Below is an example of a margin test plot showing pass results.



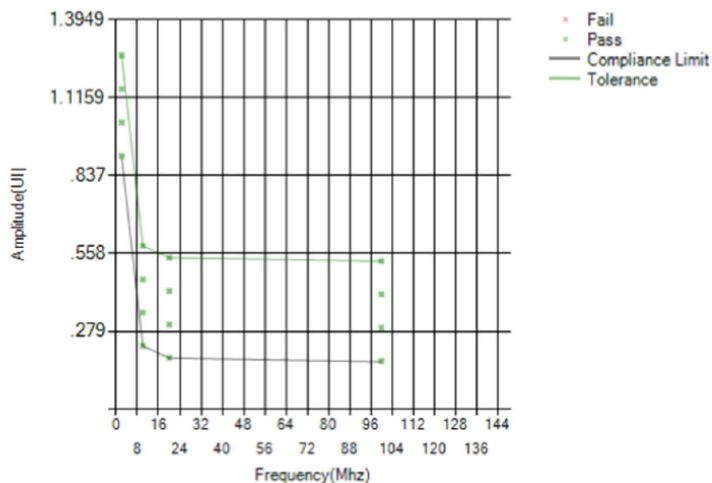


FIGURE 38. MARGIN TEST RESULTS PAGE

## 7.2 Deleting Test Reports

Click the **Delete** button to delete individual test results or **Delete All** to delete the entire test report.

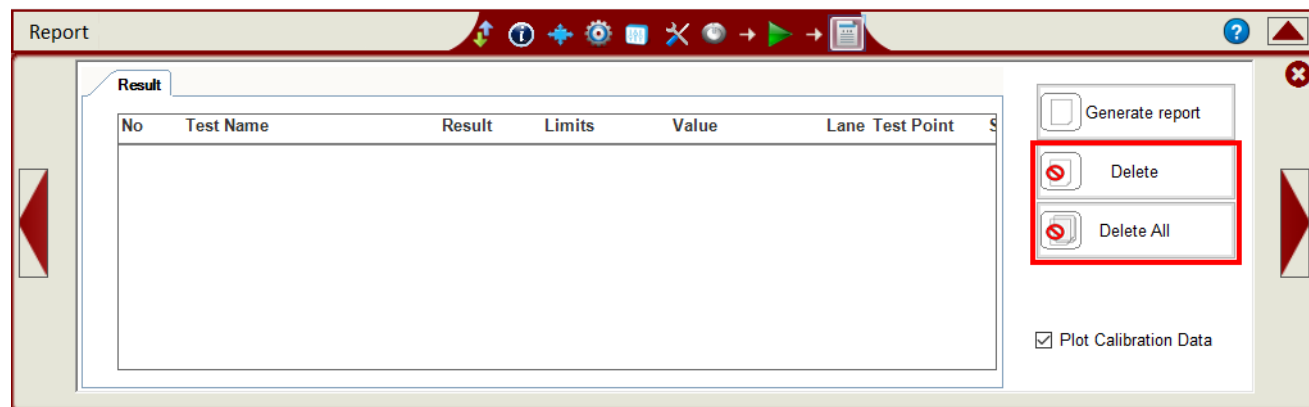


FIGURE 39. TEST REPORT DELETED

## 8 Saving and Loading Test Sessions

The usage model for the GRL-DP-SINK-BSX/DP-SINK software is that Calibration and Test Results are created and maintained as a 'Live Session' in the software. This allows you to Quit the software and return later to continue where you left off.

Save and Load Sessions are used to Save a Test Session that you may want to recall later. You can 'switch' between different sessions by Saving and Loading them when needed.

To Save a session, with all of the parameter information, test results, and any waveforms, select **Options** on the menu bar and select **Save Session**.

To Load a session back into the software, including the saved parameter settings, select **Options** on the menu bar and select **Load Session**.

To create a New session and return the software to the default configuration, select **Options** on the menu bar and select **New Session**.

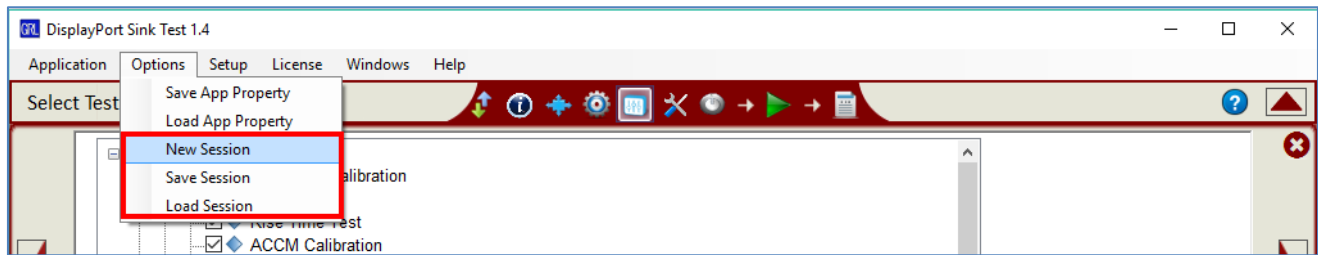


FIGURE 40. SAVING AND LOADING CALIBRATION AND TEST SESSIONS

The configuration and session results are saved in a file with the extension '.ses', which is a compressed zip-style file, containing a variety of information.

## 9 Appendix A: Manual CTS Sink Calibration and Test Procedure

The DisplayPort PHY CTS outlines the requirements for manual DisplayPort Sink Calibration and Testing in this section.

*Note: See Section 3, Resource Requirements for equipment required in the following setups.*

### 9.1 HBR3 Sink Calibration/Test Setup

The following methodology provides a typical example on how to calibrate and test the stressed impairments for HBR3 per the DP CTS. This method will be performed using the Tektronix BSA (C Model) BERTScope as SSG (Stressed Signal Generator) and Tektronix high performance Oscilloscope ( $\geq 16\text{GHz}$ ) as JMD (Jitter Measurement Device).

*Note: This is an early market MOI that may change as the DP1.4 CTS becomes final, however, it will be used to Certify early market DP Sinks per the DP1.4 Best Effort Test Program.*

#### 9.1.1 Calibration Setup and Procedure (at TP1)

Calibration for HBR3 will be performed at test points TP1, TP2, and TP3. The following figure shows the conceptual calibration setup at TP1.

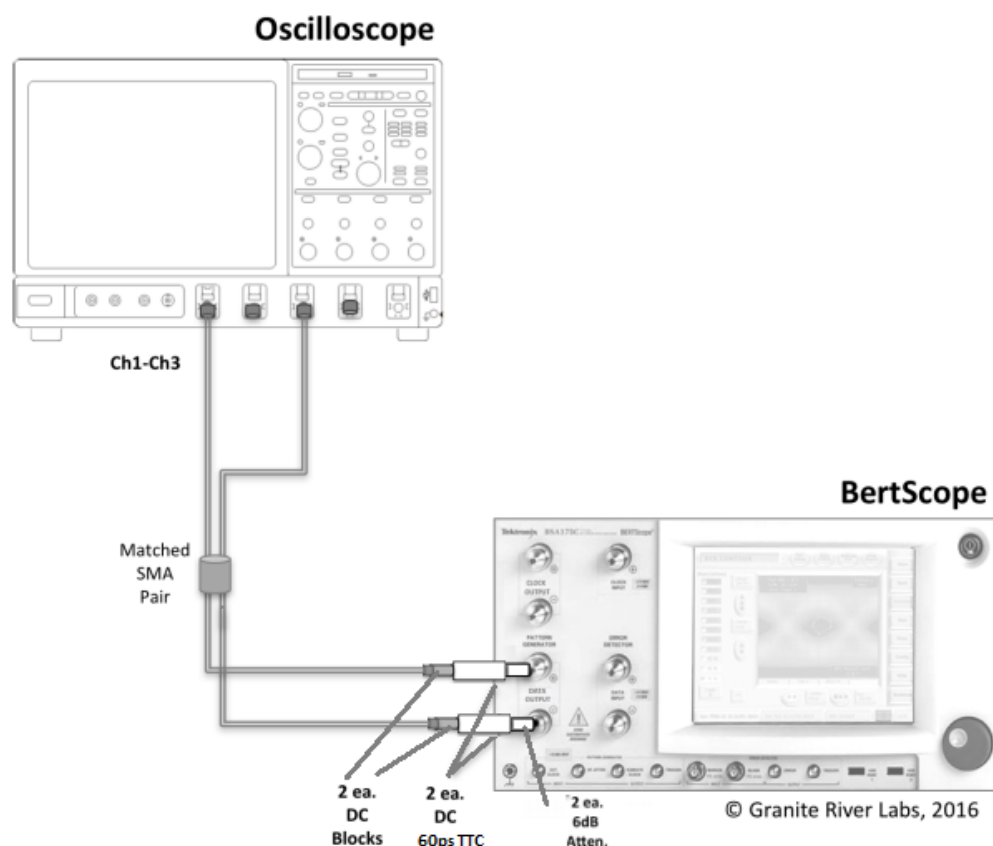


FIGURE 41. HBR3 CONCEPTUAL SETUP FOR TP1 CALIBRATION

1. Connect the equipment as shown in the above setup diagram.
2. Turn on DATA Output of the BERTScope.
3. Set up the BERTScope to recall *HBR3\_Risetime.cfg* as follows:
  - Bitrate: 8.1Gb/s
  - Launch Amplitude: 1.4V Differential (700mV with divider) to provide a voltage that is found to be close to the final value when calibration is complete.
  - Pattern: Clock/256
  - Jitter Terms enabled and set to zero

*Note: The HBR3\_Risetime.cfg BERTScope setup uses the Clock/256 pattern to provide a long run length in order to produce accurate rise time measurement when averaged.*

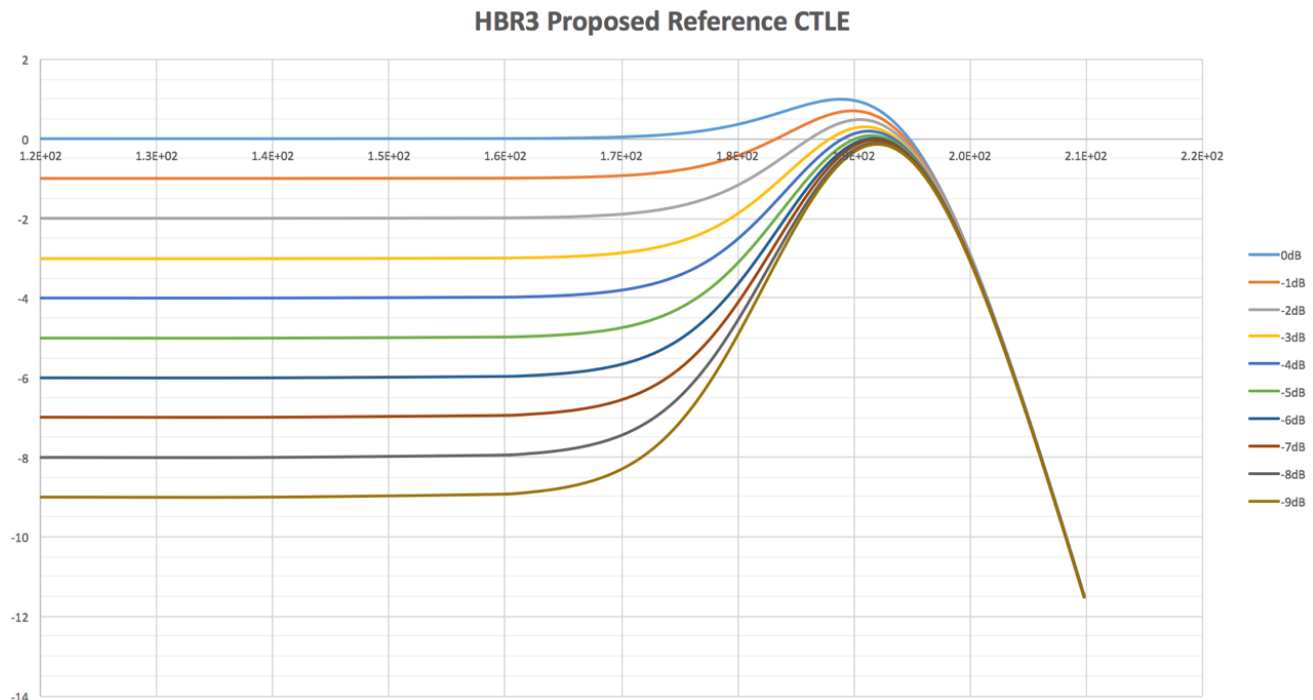
4. Set up the Oscilloscope to recall *Risetime.set* as follows:
  - Data: Ch1 – Ch3
  - Crosstalk: Ch2 – Ch4 BW = 16GHz
  - SR: 100GS/s (Ch1 – Ch3 or Ch2 – Ch4)
  - 60mV/div Differential Math
  - 20-80 Rise Time Measurement enabled
  - Averaged to 16 acquisitions as set in the Acquisition Menu of the oscilloscope.

*Note: The Risetime.set oscilloscope setup provides the Differential math signal which is optimized for swing of the BERTScope signal and averaged for accurate 20-80 rise time measurement.*

5. On the BERTScope, verify that the 20-80 rise time is between **40-60ps** (measured at the above BW).
6. Calibrate the AC Common Mode (ACCM) to **100mV pk-pk +/- 5% at 400MHz** as follows:
  - a) On the Scope, recall *CM.set*:
    - Math1: (Ch1 + Ch3)/2
    - Averaged to 16 acquisitions
    - Measure Pk-Pk (Math1)
  - b) On the BERTScope:
    - CM Control: On
    - CM Frequency: 400MHz
    - pk-pk Amplitude: 100mV
  - c) Calibrate the CM Amplitude to 100mV pk-pk +/- 5%.
  - d) Return the CM Amplitude to 0V, but leave the CM Source Enabled.
7. Calibrate **RJ** to **13mUI +/- 5% RMS (160mUI pk-pk)** and then return to zero as follows:
  - a) On the BERTScope, adjust RANDOM JITTER (10MHz to 1GHz).
  - b) On the BERTScope, recall *HBR3\_RjPj.cfg* using Pattern = D24.3 and 1100 Quarter Rate Clock.

*Note: The Quarter Rate Clock is used to maintain 50% Edge Density.*

- c) On the Scope, recall *HBR3\_RjPj.set* as follows:
    - DPOJET settings:
      - Clock Recovery: Mean
      - Pattern Length: 4UI
  - d) Calibrate to RJ = 13mUI +/- 5% RMS (160mUI pk-pk), measurement = RJ-DD.
  - e) Return the RJ Amplitude to the Intrinsic RJ on the BERTScope, but leave it Enabled.
8. Calibrate **SJ\_Fixed** to **130mUI pk-pk at 297MHz +/- 5%** as follows:
- a) On the BERTScope, adjust HIGH FREQ SINE JITTER.
  - b) Calibrate to SJ = 130mUI pk-pk, measurement = PJ1.
  - c) Return the SJ Fixed Amplitude to zero, but leave the HIGH FREQ SINE JITTER Enabled.
9. Calibrate **SJ\_Sweep** to **100mUI pk-pk at 100MHz +/- 5%** as follows:
- a) On the BERTScope, adjust SINE JITTER.
  - b) Calibrate to SJ = 100mUI +/- 5% pk-pk, measurement = PJ1.
  - c) Repeat steps (a) and (b) above for:
    - 1013mUI pk-pk at 2MHz +/- 5%
    - 137mUI pk-pk at 10MHz +/- 5%
    - 109mUI pk-pk at 20MHz +/- 5%
  - d) Return the SJ Sweep Amplitude to zero, but leave the SINE JITTER Enabled.
10. Measure **DATA TIE Reference** for ISI Measurement at TP1 as follows:
- a) On the Scope, change the DPOJET settings to:
    - Clock Recovery: 15MHz, Damping Factor = 1
    - Fixed Data Rate: 8.1GHz
    - Pattern Length: 4
    - Apply CTLE (fz = 806MHz, fp1 = 3.03GHz, fp2 = 5.6GHz) *(Note: This comes from worst case CTLE used in Tx testing – the -8dB curve from the below family of CTLEs.)*



Measurement = DATA TIE<sub>pk-pk</sub>(TP1)

*Note: Instead of using the DDJ measurement on the Scope for ISI measurement, a relative TIE (pk-pk) measurement from TP1 to TP3\_EQ is made. The reason is that if there is some non-zero ISI intrinsic from the Scope measurement, it will be calibrated out of the measurement. Here the same clock recovery and JTF is applied at TP3\_EQ before adding the channel, and then the DATA TIE (pk-pk) is measured with a clock pattern applied. This is a baseline intrinsic value to subtract from the TIE (pk-pk) value, which will give a true ISI value after applying the channel.*

### 9.1.2 Calibration Setup and Procedure (at TP3)

Figure 42 shows the conceptual calibration setup at TP3. This setup uses the ARTEK CLE1000-A2 as the variable ISI source and the BERTScope as the crosstalk source.

*Note: Using variable ISI generation enables calibration for all data rates to be performed using the same test setup. This only requires minimum reconfiguration of the test setup, which allows testing to be more fully automated.*

*Note: The following diagram shows an example of an equipment setup that provides adequate ISI. The actual ISI calibration results may vary depending on cables and adapters used. Additional cables and adapters may be needed to achieve a calibration value that is within +/-5% of the target value. It is up to the user to ensure that the ISI values in the DP CTS for ISI are achieved and measured. You should make sure to capture the screenshot of the ISI you calibrate to and keep it with your test results for future reference.*

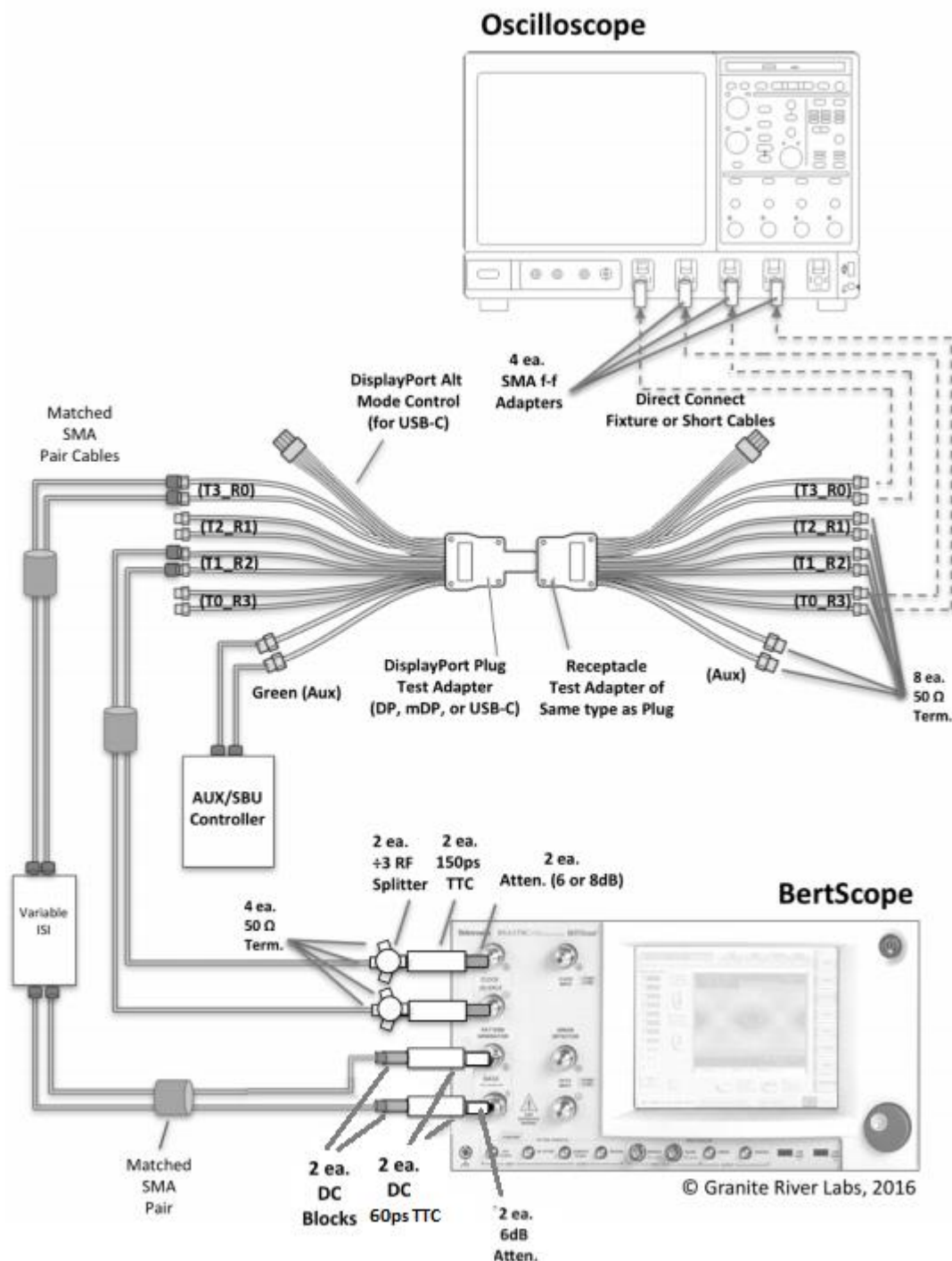


FIGURE 42. HBR3 CONCEPTUAL SETUP FOR TP3 CALIBRATION

1. Change the previous setup to the above setup.

2. Calibrate **ISI** = [DATA TIE<sub>pk-pk</sub>(TP3\_EQ) – DATA TIE<sub>pk-pk</sub>(TP1)] to **240mUI +/- 5%** as follows:

a) On the Scope, measure DATA TIE<sub>pk-pk</sub>(TP3\_EQ):

- Set up the Scope to recall *HBR3\_TP3\_EQ\_Eye.set* as follows:
  - Use the same Horizontal settings from the TP1 calibration.
  - Set the Vertical channels to 30mV/div.
  - Set up DPOJET as follows:
    - Clock Recovery: 15MHz, Damping Factor = 1
    - Fixed Data Rate: 8.1GHz
    - Pattern Length: 2520
    - Apply CTLE (fz = 806MHz, fp1 = 3.03GHz, fp2 = 5.6GHz)
- Subtract the measurement in Step 2(a) from the measurement in Step 10(b) of the TP1 calibration.
- Adjust ISI on the CLE1000-A2 until [DATA TIE<sub>pk-pk</sub>(TP3\_EQ) – DATA TIE<sub>pk-pk</sub>(TP1)] = 240mUI +/- 5%.

*Note: A physical measurement of the ISI channel and attached cables should be made with a VNA to verify it fits within 22-24dB Insertion Loss including all cables, mated pair fixture and DC Block.*

3. Calibrate **Complete Stressed Eye** at each SJ Frequency:

- Return Amplitude of CM, RJ, SJ\_Fixed, and SJ\_Sweep to add to the calibrated ISI.
- Turn on SSC on the BERTScope to -0.5.

4. Calibrate **TJ** to **600mUI +/- 5%** using SJ\_Fixed as Calibration Knob:

- Measure TJ at TP3\_EQ.
- Use Fixed RJ as the TJ method by fixing the RJ in the DPOJET Preference menu to be RJ measured in Step 7 from TP1.
- TJ = DJ + 12\*RJ; where RJ is the fixed value measured in Step 7 from TP1. This can be done by using TJ measurement in the DPOJET with the Fixed RJ Preference setting selected.

5. Repeat Step 4 to achieve **600mUI +/- 5%** for 2MHz, 10MHz, and 20MHz.

6. Calibrate **Eye Height** to **50mV -0%, +5%** by using the BERTScope's Amplitude Knob at each SJ\_Sweep Frequency. Measure Eye Height.

7. Measure or calibrate **Crosstalk** using the BERTScope Quarter Rate Clock Method as the crosstalk source as follows:

- Connect the crosstalk source to the fixture and scope as shown in Figure 42.



- Set the Clock Output on the BERTScope to  $\div 4$  at 8.1GHz. This represents a Quarter rate clock; 1100 (D24.3 HBR3 Pattern) from the BERTScope Clock output.
- Calibrate the Amplitude of the crosstalk signal to 500mV pk-pk at TP3.

8. Save the BERTScope configuration file for each SJ\_Sweep Stressed Eye.

### 9.1.3 DUT Test Setup and Procedure (at TP3)

The following figure shows the conceptual setup for testing the DUT at TP3 which follows up from the previous TP3 calibration setup.

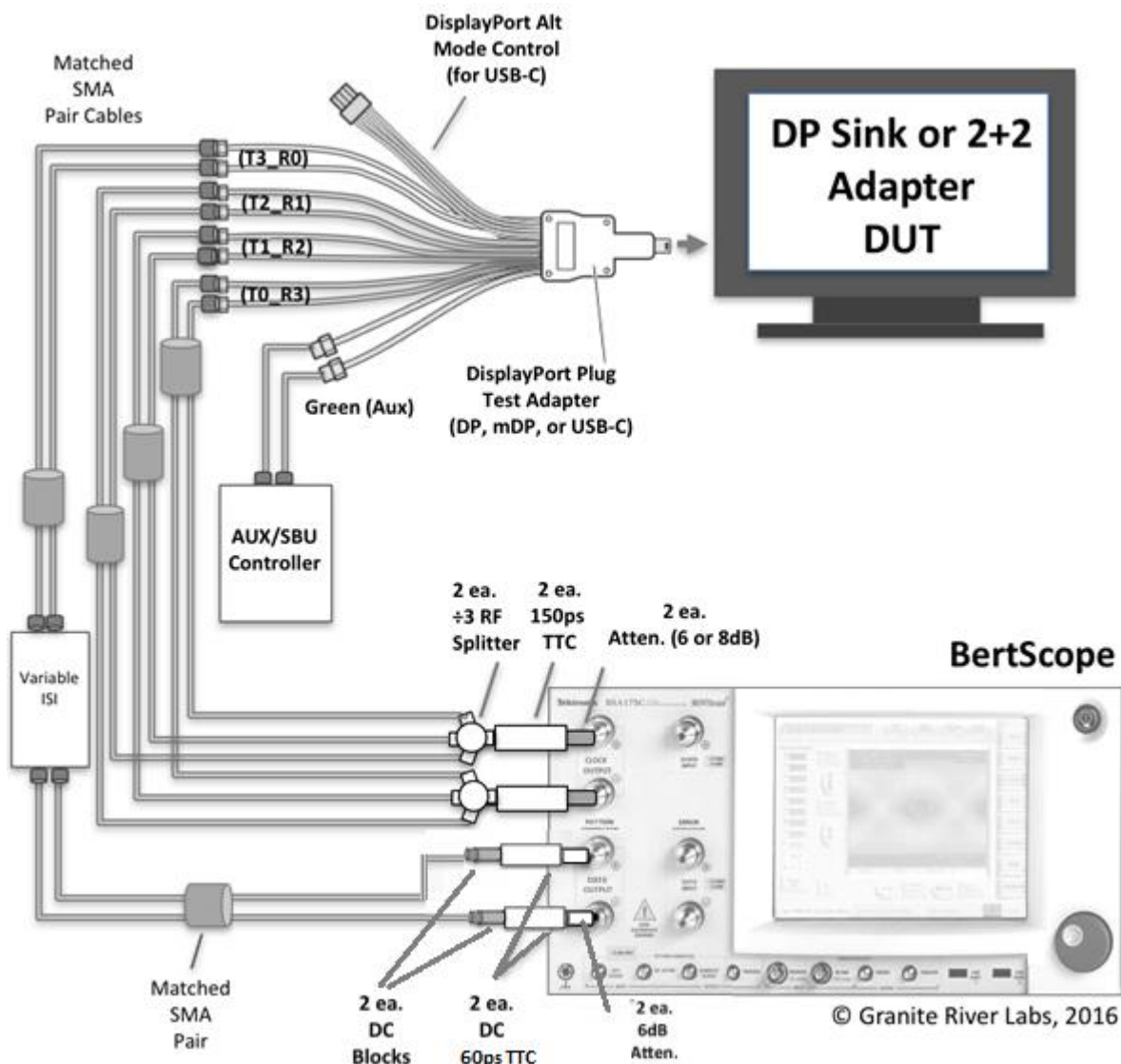


FIGURE 43. HBR3 CONCEPTUAL SETUP FOR TP3 DUT TEST

1. From the previous TP3 calibration setup, disconnect the 'P' (Plug) type adapter from the 'R' (Receptacle) calibration adapter and connect the 'P' type adapter to the DUT for testing.
2. Recall the BERTScope setup for SJ\_Sweep Stressed Eye at 100MHz.

3. Attach the Stressed Eye Signal to Lane 0 of the DUT.
4. If the DUT is a USB Type-C Sink, initiate the DP Alt Mode.
5. Test the DUT using the AUX/SBU Controller as follows:
  - Initiate the desired 'Alt Mode' if the DUT is a USB Type-C Sink.
  - Verify the Frequency Lock.
  - Verify the Symbol Lock.
  - Inject Errors and verify the correct amount of errors is being detected using the TPS4 Signal.
  - Test BER at the duration specified in the CTS.
6. Repeat Step 2 for 2MHz, 10MHz, and 20MHz SJ\_Sweep Frequencies.
7. For a 4-Lane DUT, repeat Steps 3 to 6 for Lanes 1, 2, and 3.

#### **9.1.4 Calibration Procedure at TP2**

If running calibration at TP2, perform the following steps:

1. Calibrate to the ISI target value (120mUI) at TP2 (with CTLE applied) as specified in the DP1.4 and DP Over Type-C CTS.
2. Calibrate to the target Eye Height (170mV) at TP2\_CTLE in a similar way as described in the previous TP3 calibration.
3. Substitute the TP2\_CTLE ISI value for TP3\_EQ to obtain the final calibrated signal.
4. Capture the TP2 Eye Diagram to be included in the test report.

*Notes:*

- *The TP2 Eye Diagram is captured using the same CDR/JTF function as at TP3\_EQ with CTLE applied.*
- *The final Eye Height at TP2 is established by TP34 Eye Height Calibration.*



## 9.2 HBR2, HBR, and RBR Sink Calibration/Test Setup

The following methodology describes how to calibrate the stressed impairments for HBR2, HBR, and RBR per the PHY CTS using the DisplayPort standard configuration at TP1 and TP3/TP3\_EQ. The detailed example shown is for HBR2.

RBR calibration is very similar to HBR/HBR2 calibration except that RBR calibration is done at TP3 instead of TP3\_EQ.

### 9.2.1 Calibration Setup and Procedure

The following diagrams show the conceptual setup at TP1 and TP3/TP3\_EQ as described in the CTS.

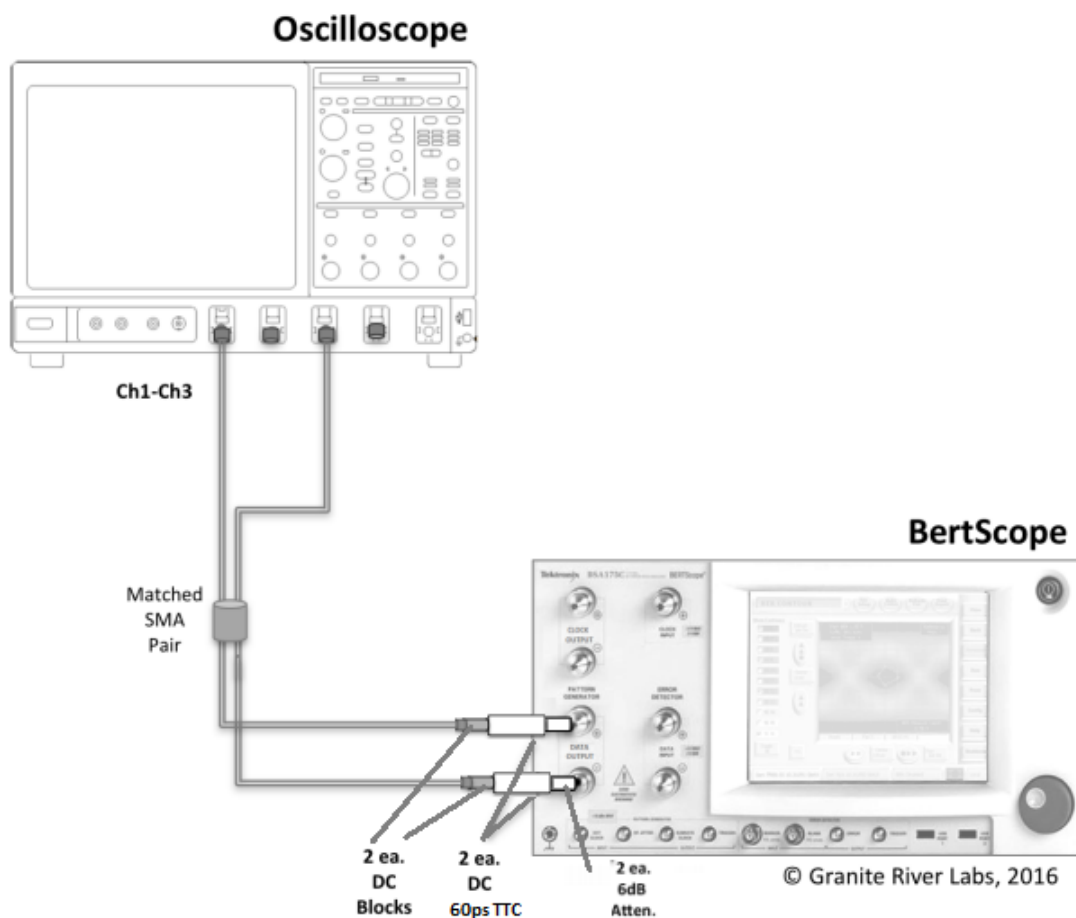


FIGURE 44. CONCEPTUAL CALIBRATION SETUP AT TP1

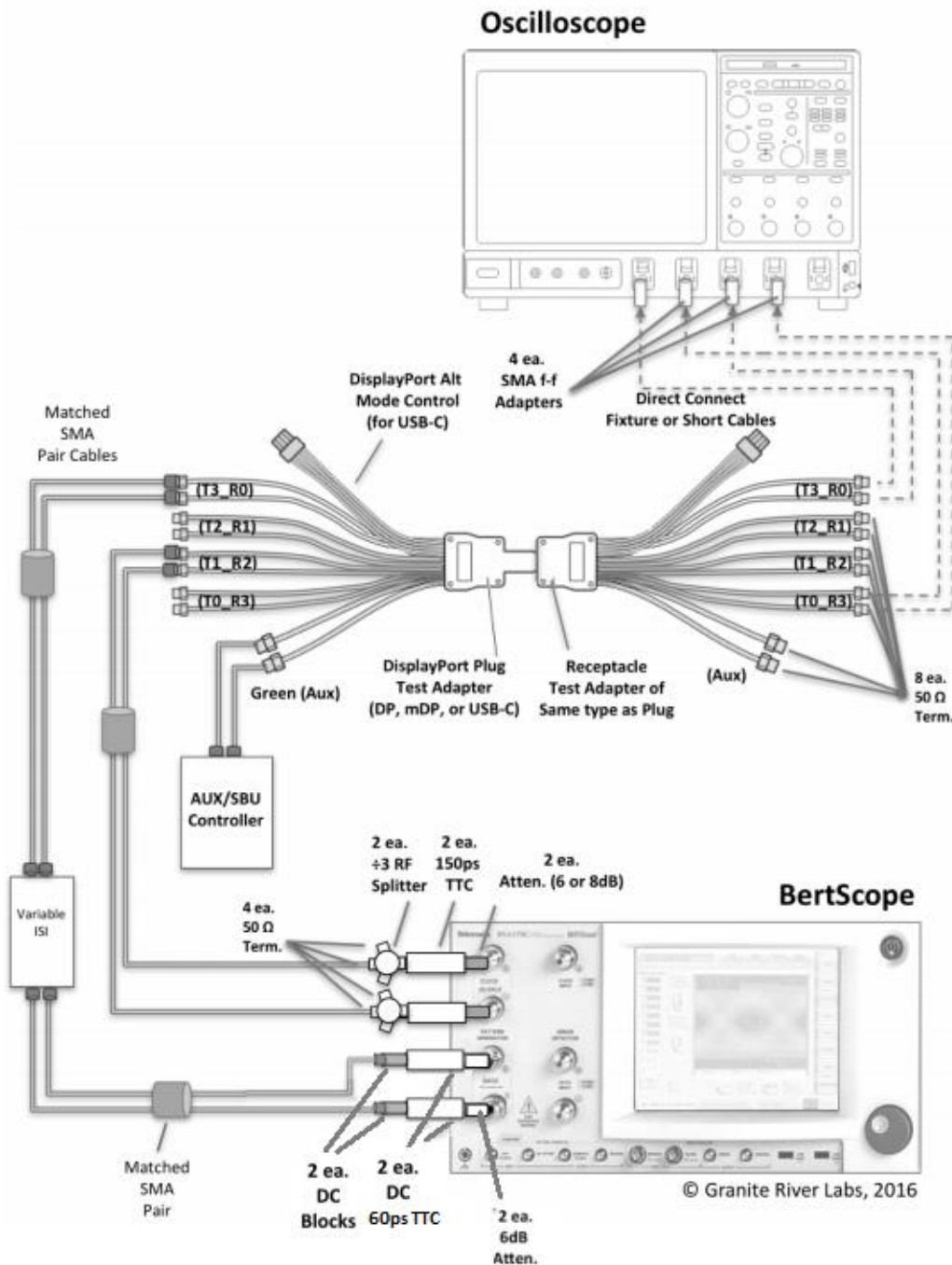


FIGURE 45. CONCEPTUAL CALIBRATION SETUP AT TP3/TP3\_EQ (STANDARD CONNECTION)

1. Set up the equipment for TP1 calibration. Turn on the BERTScope and apply Differential amplitude and AC coupling. (*Note: Use attenuators to maintain the large amplitude generated from the BERTScope.*)
  - Ensure that pre-calibration/test procedure have been performed for the BERTScope and Oscilloscope as described in Section 5.1.

- On the BERTScope, go to View > Generator and make sure the Outputs On/Off is set to Off while making connections.
- Connect the DATA outputs of the BERTScope directly to the Scope channels.
- Set up the BERTScope as follows:

| RBR  | HBR  | HBR2  |
|--|--|---|
| BERTScope: View > Generator: <ul style="list-style-type: none"> <li>▪ Synthesizer: 1,620.00MHz</li> <li>▪ DATA+: Ampl = 200mV (400mV Differential).<br/>DATA-: Linked to DATA+.</li> <li>▪ Outputs On/Off: On</li> </ul> | BERTScope: View > Generator: <ul style="list-style-type: none"> <li>▪ Synthesizer: 2,700.00MHz</li> <li>▪ DATA+: Ampl = 300mV (600mV Differential).<br/>DATA-: Linked to DATA+.</li> <li>▪ Outputs On/Off: On</li> </ul> | BERTScope: View > Generator: <ul style="list-style-type: none"> <li>▪ Synthesizer: 5,400.00MHz</li> <li>▪ DATA+: Ampl = 700mV (1.4V Differential).<br/>DATA-: Linked to DATA+.</li> <li>▪ Outputs On/Off: On</li> </ul> |

2. Perform Rj(rms) calibration at TP1. Apply the D24.3 user pattern and set constant clock for JMD.

#### Initialization of BERTScope for Jitter Composition:

- a) On the BERTScope, enable and set all jitter terms to zero before calibrating each term independently.
  - For HBR2 only, select HIGH FREQ SINE JITTER as shown below:

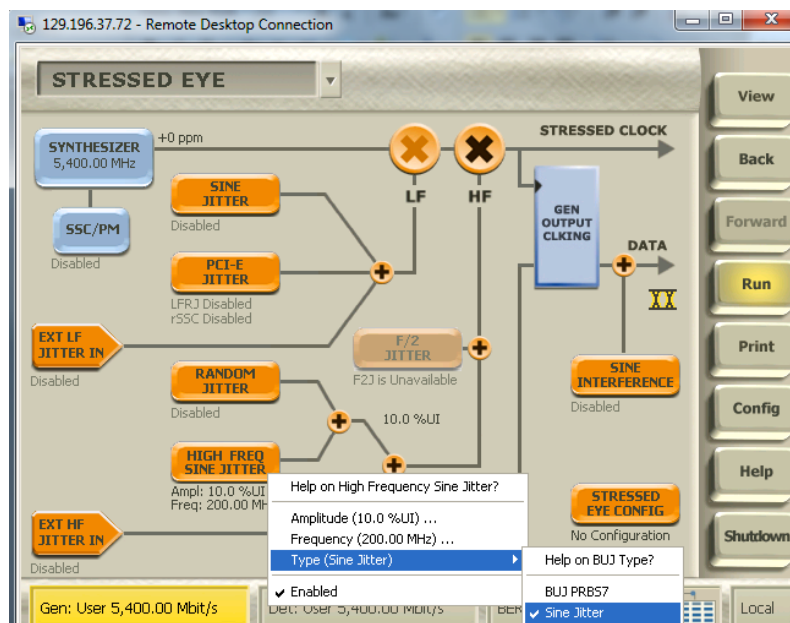


FIGURE 46. SELECTING HIGH FREQUENCY SINE JITTER

- Set the HIGH FREQ SINE JITTER frequency to 200MHz and amplitude to 0% UI.
- Turn on SINE JITTER and set the frequency to 10MHz and amplitude to 0% UI.

- Turn on RANDOM JITTER (1.5MHz to 100MHz) and set the amplitude to 0%.  
*Note: It will default to Intrinsic Limit.*

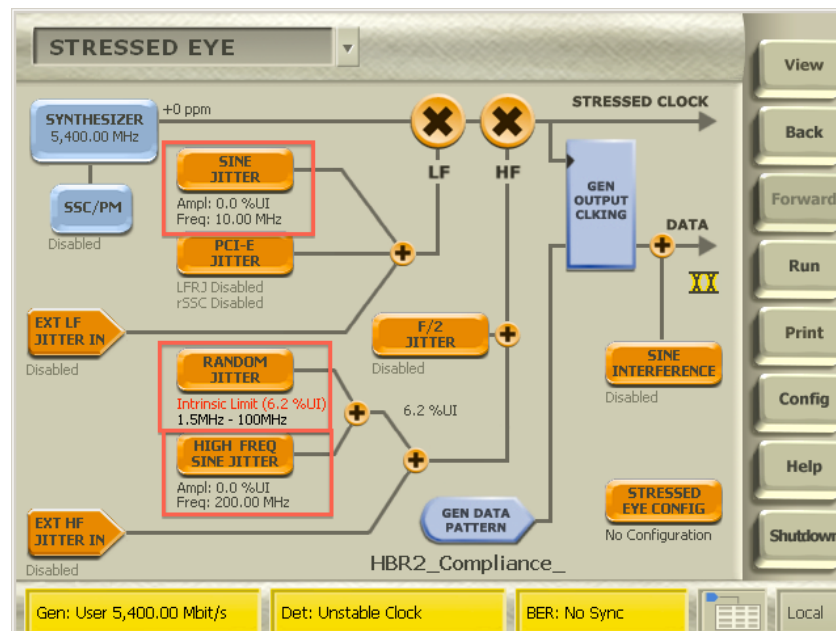


FIGURE 47. INITIAL JITTER SETUP

### Random Jitter Calibration:

- On the BERTScope, select View > Generator. Select the User Pattern and import the D24-3\_Clock.ram pattern file.

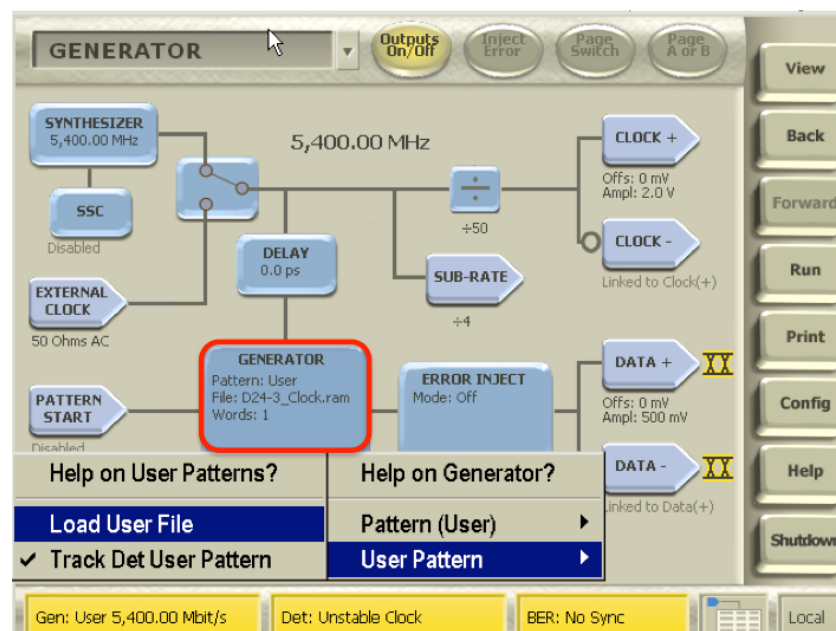


FIGURE 48. BERTSCOPE D24-3\_CLOCK.RAM PATTERN

- c) On the BERTScope, select View > Stressed Eye > Random Jitter.

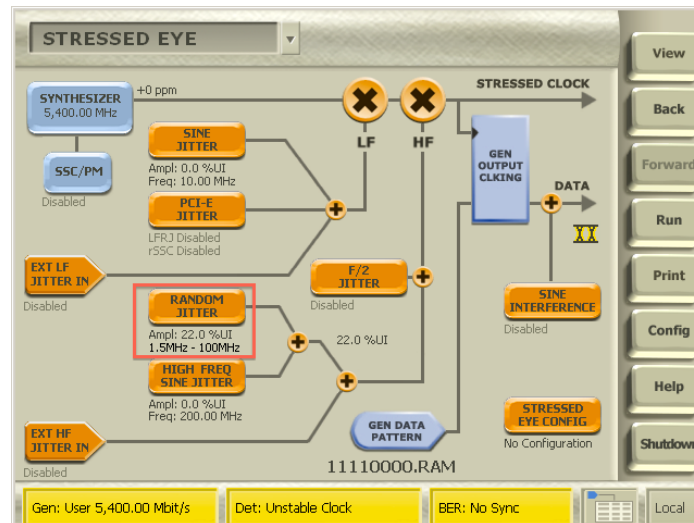


FIGURE 49. BERTSCOPE Rj ADJUSTMENT

- d) On the Scope DPOJET (Jitter and Eye Tools SW), calibrate Random Jitter for the desired data rate using the following setup files:
- C:\TekApplications\DPOJET\Setups\DisplayPort\HBR2\_RjPj.set*
  - C:\TekApplications\DPOJET\Setups\DisplayPort\HBR\_RjPj.set*
  - C:\TekApplications\DPOJET\Setups\DisplayPort\RBR\_RjPj.set*
- e) Adjust Rj on the BERTScope user interface while using the Single function on the DPOJET SW until Rj is calibrated to the following target values:
- **RBR: 8.1mUI RMS**
  - **HBR: 13.5mUI RMS**
  - **HBR2: 16.7mUI RMS, 200mUI pk-pk (16.7 RMS x 12.0)**



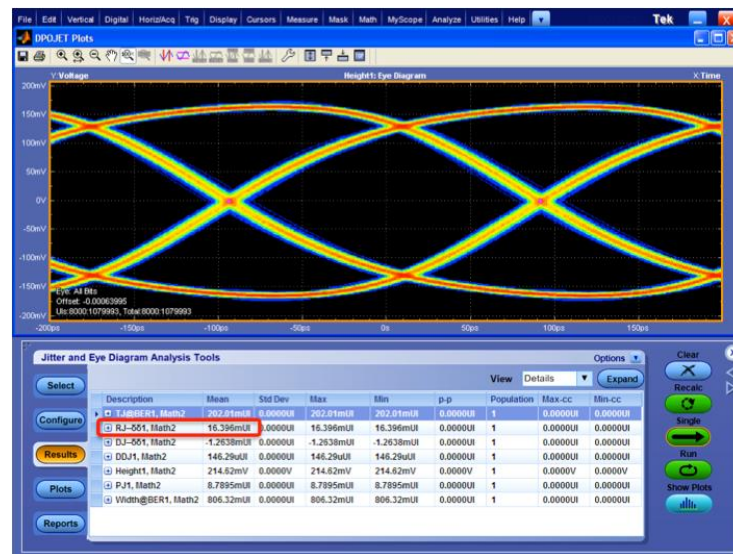


FIGURE 50. HBR2 RJ MEASUREMENT EXAMPLE

Note: The  $R_j$  value in this example is measured at 16.4mUI.

- f) Record the calibrated value for  $R_j$ .
  - g) Return the  $R_j$  value on the BERTScope to zero (Note: Intrinsic Jitter Limit will be displayed). The value will be returned to the above calibrated value in Step 7.
3. Perform calibration for  $S_{J\text{FIXED}}$  at TP1 for HBR2 only. Apply the D24.3 user pattern and set constant clock for JMD.
    - a) Set the HIGH FREQ SINE JITTER frequency to 200MHz and amplitude to 10% UI.

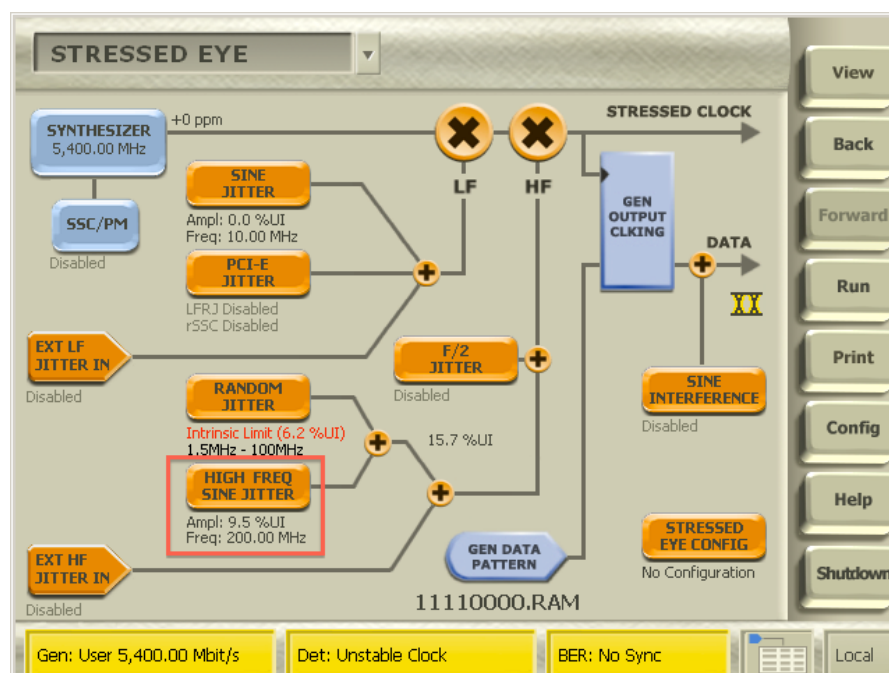


FIGURE 51. BERTSCOPE  $S_{J\text{FIXED}}$  ADJUSTMENT EXAMPLE FOR HBR2

- b) On the Scope DPOJET (Jitter and Eye Tools SW), use the *HBR2\_RjPj.set* configuration to calibrate the Sinusoidal Jitter.
- c) Adjust the HIGH FREQ SINE JITTER amplitude on the BERTScope while using the Single function on the DPOJET SW to calibrate Pj to the following target values:
  - RBR: NA
  - HBR: NA
  - HBR2: 80mUI

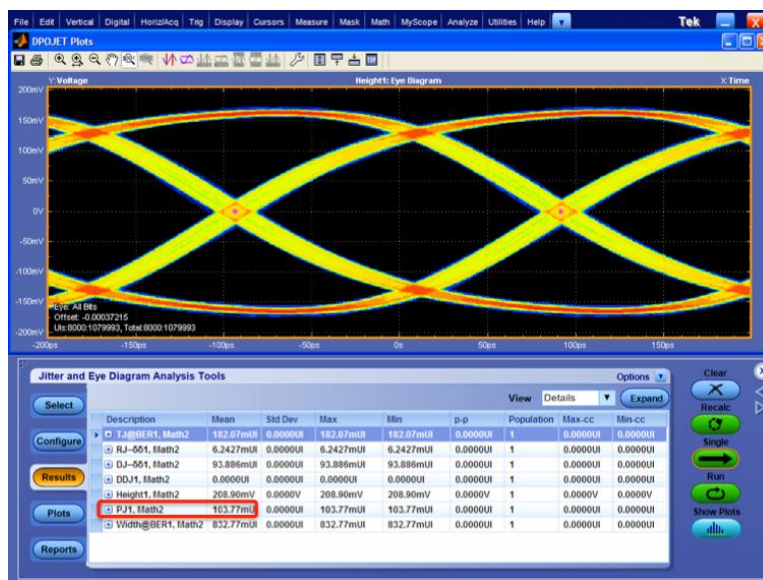


FIGURE 52. HBR2 SJ<sub>FIXED</sub> MEASUREMENT EXAMPLE (NOT SHOWING TARGET 80mUI)

- d) Record the calibrated value for SJ<sub>FIXED</sub>.
  - e) Return the HIGH FREQ SINE JITTER value on the BERTScope to zero. The value will be returned to the above calibrated value in Step 7.
4. Perform calibration for SJ<sub>SWEEP</sub> for each frequency at TP1. Set constant clock for JMD.

Table 4-16: RBR TP3 Jitter Component Settings<sup>a b</sup>

| Frequency (SJ)<br>(MHz) | TJ<br>(mUI) | ISI<br>(mUI) | RJ <sub>rms</sub><br>(mUI) | Approximate SJ<br>(mUI) |
|-------------------------|-------------|--------------|----------------------------|-------------------------|
| 2                       | 1648        | 570          | 8.1                        | 981                     |
| 10                      | 778         |              |                            | 111                     |
| 20                      | 747         |              |                            | 80                      |

a. See DP 1.4a, Figure 3-31.

b. This table does not account for crosstalk-injected jitter.

Table 4-11: HBR TP3\_EQ Jitter Component Settings<sup>a</sup>

| Frequency (SJ)<br>(MHz) | TJ<br>(mUI) | ISI<br>(mUI) | RJ <sub>rms</sub><br>(mUI) | Approximate<br>SJ <sub>SWEEP</sub><br>(mUI) |
|-------------------------|-------------|--------------|----------------------------|---|
| 2                       | 1227        | 161          | 13.5                       | 904   |
| 10                      | 548         |              |                            | 225   |
| 20                      | 505         |              |                            | 182   |
| 100                     | 491         |              |                            | 168   |

a. See DP 1.4a, Figure 3-30.

Table 4-9: HBR2 TP3\_EQ Jitter Component Settings<sup>a</sup>

| Frequency (SJ)<br>(MHz) | TJ<br>(mUI) | ISI<br>(mUI) | RJ <sub>rms</sub><br>(mUI) | Approximate<br>SJ <sub>SWEEP</sub><br>(mUI) | SJ <sub>FIXED</sub><br>at 297MHz<br>(mUI) | Crosstalk <sup>b</sup><br>(mUI) |
|-------------------------|-------------|--------------|----------------------------|---|---|---------------------------------|
| 2                       | 1026        | 220          | 16.7                       | 505   | 80  | 20                              |
| 10                      | 636         |              |                            | 116   |   |                                 |
| 20                      | 624         |              |                            | 104   |   |                                 |
| 100                     | 620         |              |                            | 100   |   |                                 |

a. See DP 1.4a, Figure 3-29.

b. Crosstalk jitter of 20mUI is assumed (not calibrated on the test fixture) to be generated from the fixed-amount aggressors.

FIGURE 53. JITTER COMPONENT SETTINGS FROM CTS

- a) On the BERTScope, turn on SINE JITTER.

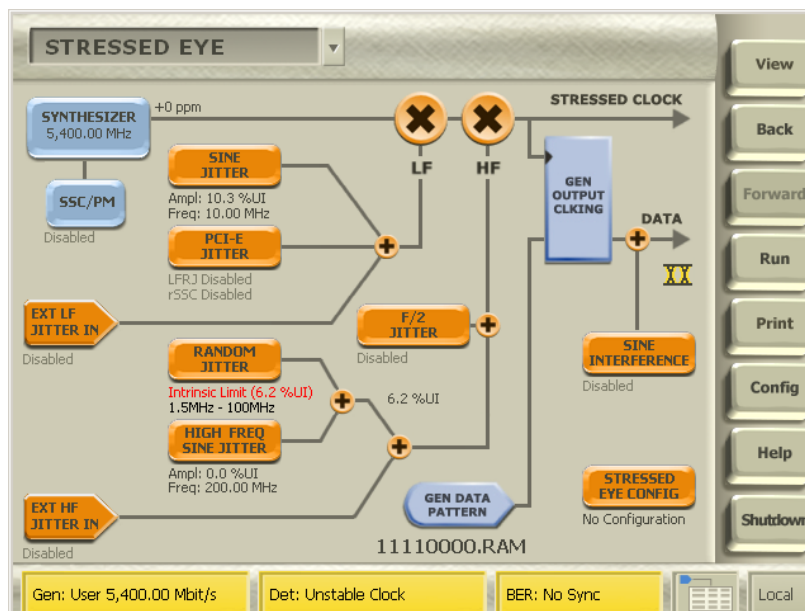


FIGURE 54. BERTSCOPE SJ<sub>SWEEP</sub> ADJUSTMENT

- b) Adjust the SINE JITTER amplitude on the BERTScope while using the Single function on the DPOJET SW to calibrate P<sub>j</sub> to the target values.

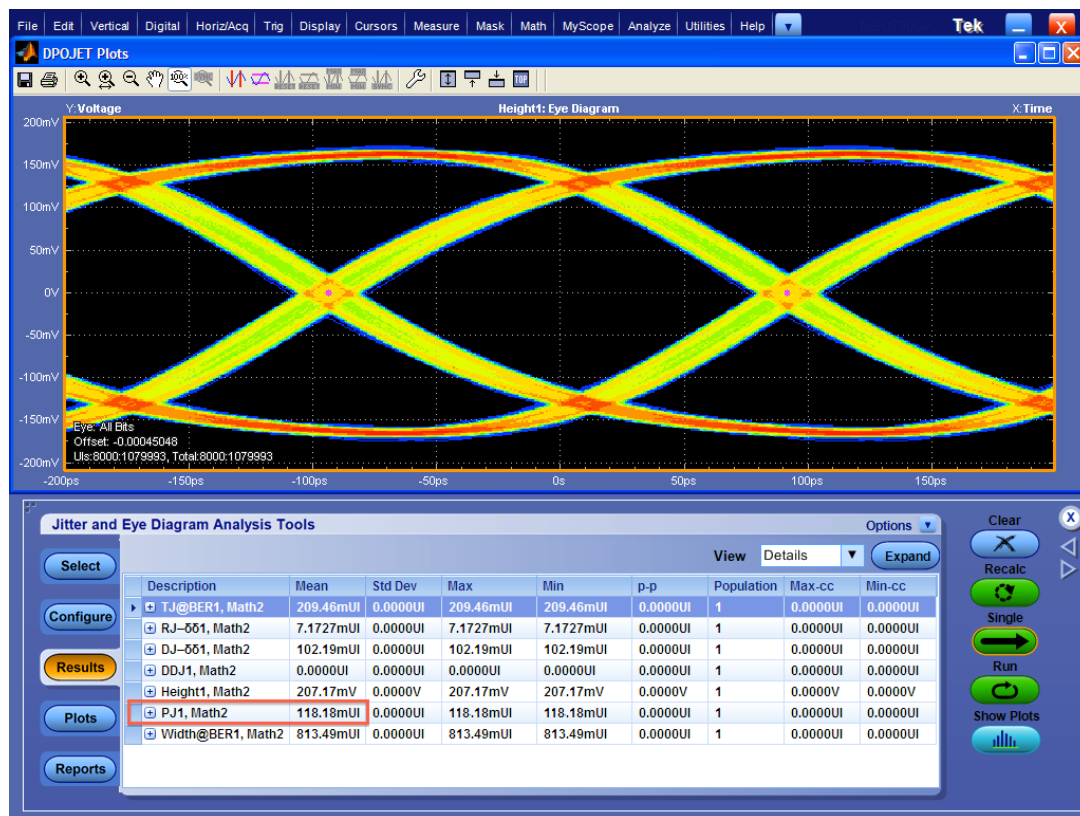


FIGURE 55. HBR2 SJ<sub>SWEEP</sub> MEASUREMENT EXAMPLE

*Note: In this example, PJ is measured at 118.2mUI.*

- Set up the equipment for TP3 calibration. Measure the ISI at TP3\_EQ to the target ISI values specified in the CTS for HBR or HBR2 respectively. Apply the PRBS7 test pattern for HBR or CP2520 for HBR2. Set the clock recovery of the JMD to 2nd Order as described in the CTS. For RBR, apply the PRBS7 test pattern and calibrate the ISI at TP3 without equalization.

*Note: Ensure that adequate ISI at TP3\_EQ (for HBR and HBR2) or TP3 (for RBR) is achieved by the ISI generator being used as required in the CTS.*

*Note: Actual ISI calibration results may vary depending on cables and adapters used in the physical setup. Additional cables and adapters may be needed to achieve a calibration value that is within +/-5% of the target value. It is recommended to capture the screenshot of the calibrated ISI and keep it with the test results for future reference.*

| RBR ISI Procedure   | HBR ISI Procedure   | HBR2 ISI Procedure   |
|---|---|--|
| On BERTScope > View > Generator: <ul style="list-style-type: none"> <li>Generator: Pattern = PRBS7</li> <li>Outputs On/Off: On</li> </ul> On Scope: | On BERTScope > View > Generator: <ul style="list-style-type: none"> <li>Generator: Pattern = PRBS7</li> <li>Outputs On/Off: On</li> </ul> On Scope: | On BERTScope > View > Generator: <ul style="list-style-type: none"> <li>Generator: Pattern = User.<br/>User File =<br/>Displayport/HBR2_Compliance_2520bits_Pattern1.ram.</li> </ul> |

|   |   |  |
|---|---|--|
| <ul style="list-style-type: none"> <li>Recall DPOJET setup file to make DDJ measurements:<br/>&lt;C:\TekApplications\DPOJET\Setups\DisplayPort\RBR_PLL_Eye.set&gt;</li> <li>DPOJET Sequence menu:<br/>Single</li> <li>Measure ISI = <b>570mUI +/- 5%</b></li> <li>Capture and save scope screenshot for compliance records</li> </ul> | <ul style="list-style-type: none"> <li>Recall DPOJET setup file to apply TP3_EQ filter and make DDJ measurements:<br/>&lt;C:\TekApplications\DPOJET\Setups\DisplayPort\HBR_PLL_Eye.set&gt;</li> <li>DPOJET Sequence menu:<br/>Single</li> <li>Measure ISI = <b>161mUI +/- 5%</b></li> <li>Capture and save scope screenshot for compliance records</li> </ul> | <ul style="list-style-type: none"> <li>Outputs On/Off: On</li> </ul> <p>On Scope:</p> <ul style="list-style-type: none"> <li>Recall DPOJET setup file to apply TP3_EQ filter and make DDJ measurements:<br/>&lt;C:\TekApplications\DPOJET\Setups\DisplayPort\HBR2_PLL_Eye.set&gt;</li> <li>DPOJET Sequence menu:<br/>Single</li> <li>Measure ISI = <b>220mUI +/- 5%</b></li> <li>Capture and save scope screenshot for compliance records</li> </ul> |
|---|---|--|

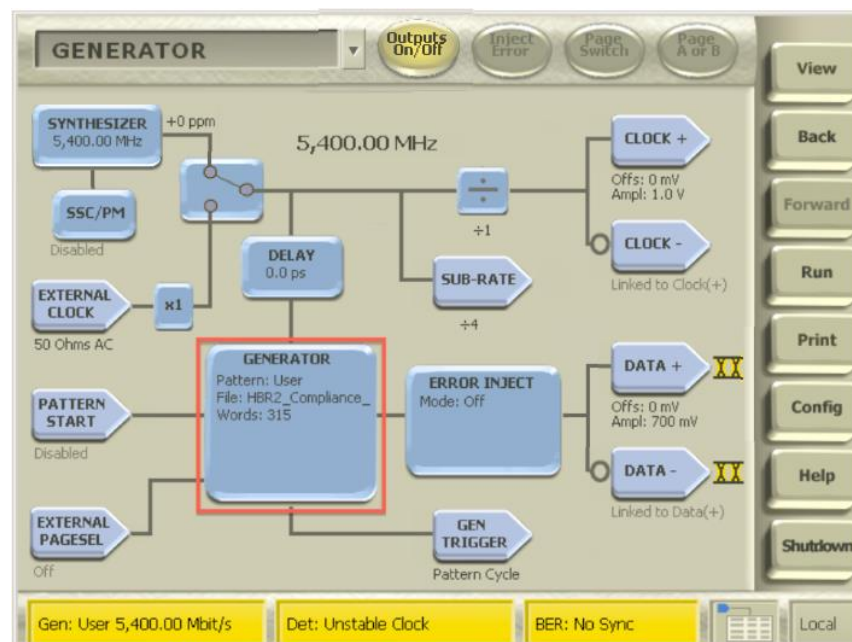


FIGURE 56. BERTSCOPE HBR2 ISI SETUP EXAMPLE



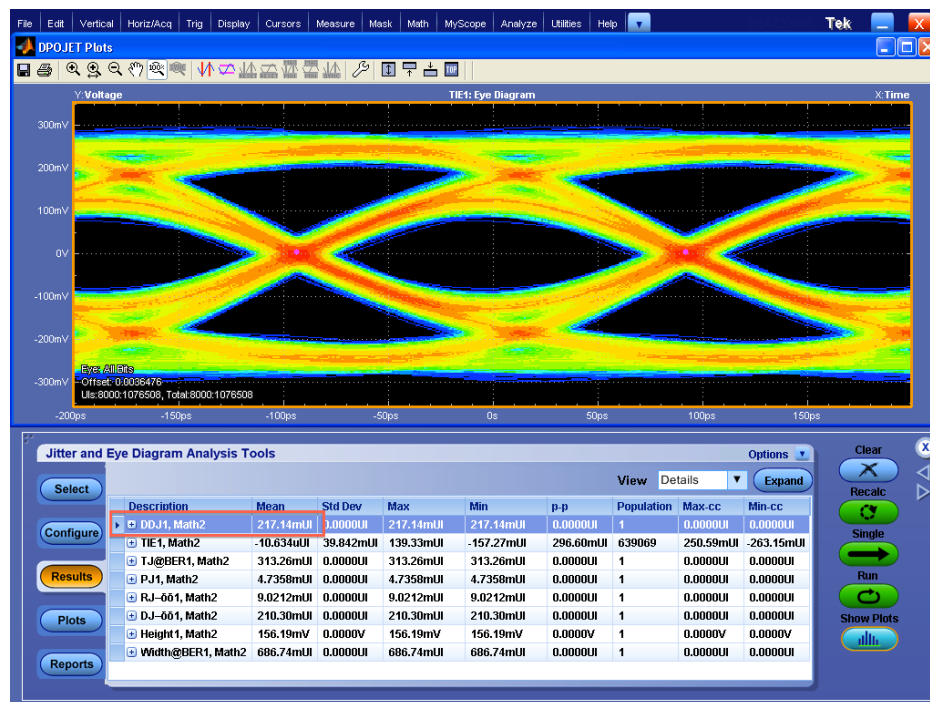


FIGURE 57. HBR2 ISI MEASUREMENT EXAMPLE

*Note: The ISI value in this example is measured at 217mUI. It is recommended to capture and save the screenshot of the scope measurement to demonstrate that the proper value has been achieved.*

*Note: To achieve the best measurements on the scope, ensure that its vertical signals are properly scaled without clipping before applying the Ch1-Ch3 function and Equalization.*

6. On the BERTScope, make sure that the test pattern is set to PRBS7 (for RBR and HBR) or CP2520 (for HBR2) from the previous step. In case the pattern has been changed, re-select as follows:
  - a) For HBR2, select the User Pattern and import *HBR2\_Compliance\_2520bits\_Pattern1.ram* from the DisplayPort folder. For HBR and RBR, select PRBS7 from the Pattern menu.

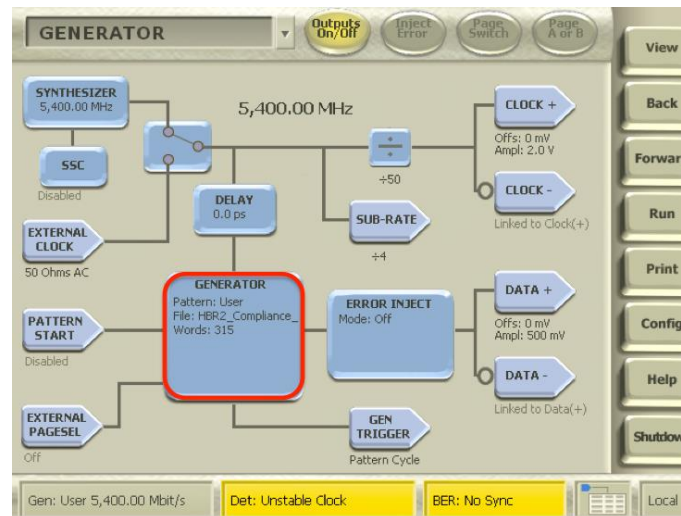


FIGURE 58. HBR2 COMPLIANCE EYE PATTERN SETUP EXAMPLE

7. On the BERTScope, enable ISI, RJ, SJ<sub>FIXED</sub>, SJ<sub>SWEEP</sub>, and SSC.
  - a) ISI is achieved in Step 5.
  - b) Select View > Stressed Eye:
    - Return the Ampl of RJ (RANDOM JITTER) to the value calibrated in Step 2.
    - For HBR2, return the Ampl of SJ<sub>FIXED</sub> (HIGH FREQ SINE JITTER) to the value calibrated in Step 3.
    - Turn on SJ<sub>SWEEP</sub> (SINE JITTER) as calibrated in Step 4.
    - Turn on SSC with 33KHz frequency and 5000ppm with a triangle profile.

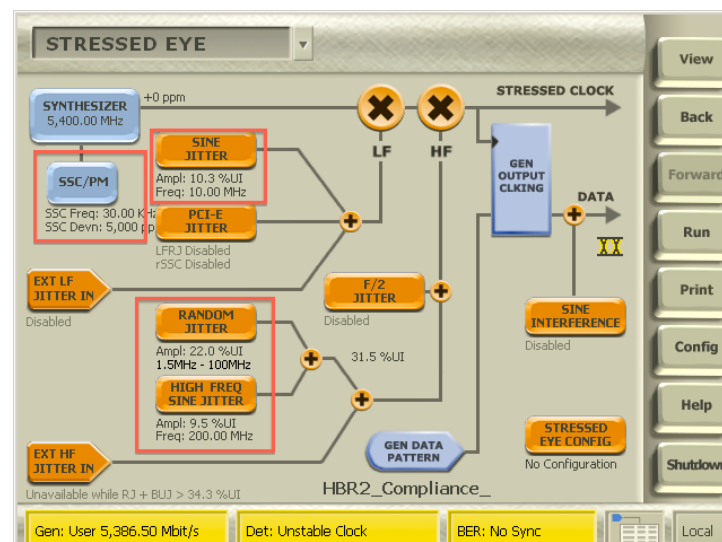


FIGURE 59. ALL STRESSES ENABLED EXCEPT CROSSTALK FOR HBR2

8. Perform calibration at TP3\_EQ for the BERTScope Amplitude to reach the target Eye Height of 160mV for HBR or 100.0mV without crosstalk for HBR2. Set the 2<sup>nd</sup> order clock recovery function for JMD as described in the DP specification.

- a) On the DPOJET (Jitter and Eye Tools SW), acquire and analyze the signal using the following setup files for each data rate:

*C:\TekApplications\DPOJET\Setups\DisplayPort\HBR2\_PLL\_Eye.set*

C:\TekApplications\DPOJET\Setups\DisplayPort\HBR\_PLL\_Eye.set

C:\TekApplications\DPOJET\Setups\DisplayPort\RBR\_PLL\_Eye.set

- b) Select View > Generator on the BERTScope and adjust the DATA+ Amplitude while using the Single function on the DPOJET SW to measure the Eye Height to the following target values:

- RBR: 56mV (+/- 3%)
- HBR: 160mV (+/- 3%)
- HBR2: 100mV (+/- 3%)

*Note: To achieve a repeatable Eye Opening measurement, capture a minimum of 2mUI with the JMD. Measure the vertical Eye Height as described in the CTS.*

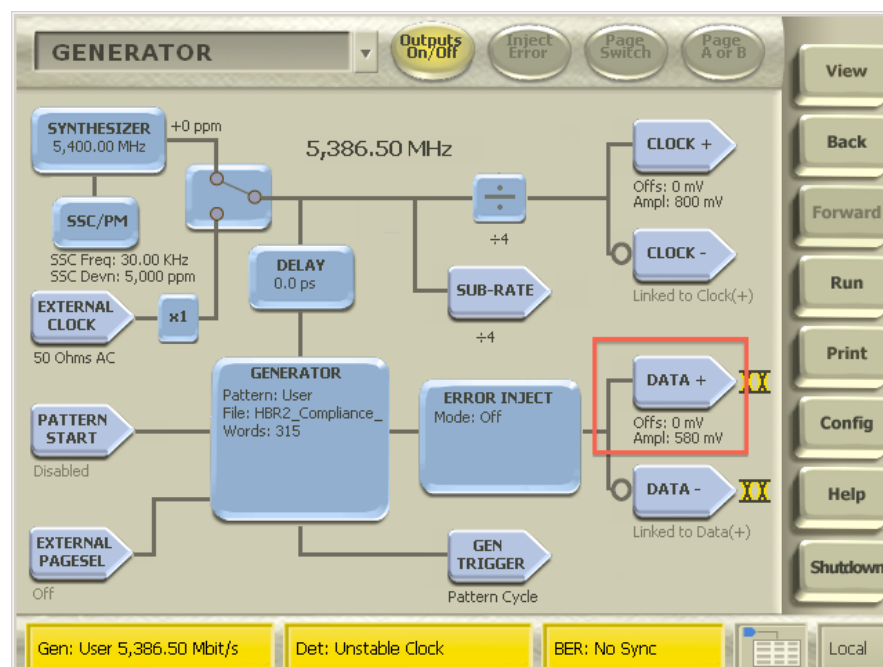


FIGURE 60. HBR2 EYE HEIGHT ADJUSTMENT EXAMPLE



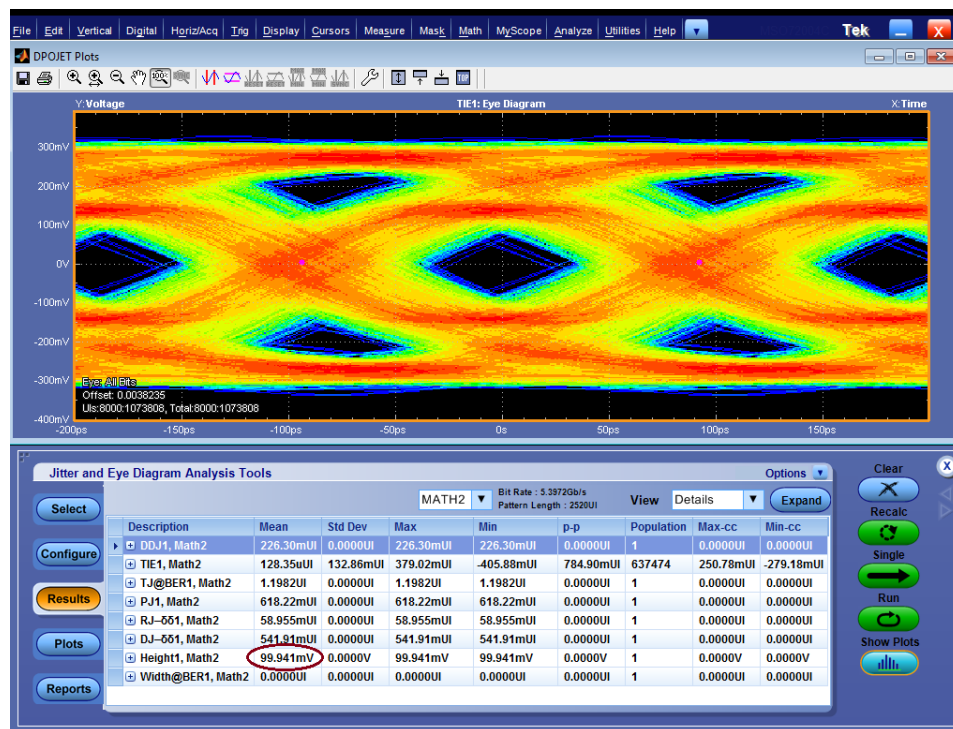


FIGURE 61. HBR2 EYE HEIGHT MEASUREMENT EXAMPLE

9. On the Scope, apply a non-phase aligned crosstalk aggressor signal to Ch2-Ch4 for all data rates. Use the D24.3 pattern and set the Differential amplitude to 800mV for the crosstalk signal. Adjust the crosstalk signal Amplitude to reach the target value for the appropriate link rate.

*Note: The Edge rate of the crosstalk signal is set to 130ps (20/80) measured at TP3.*

*Note: Crosstalk amplitude is dependent on the receptacle fixture being used. Refer to the respective manufacturer for details.*

- a) Select View > Generator on the BERTScope and adjust the CLOCK+ Amplitude while using the Single function on the DPOJET SW to measure Cycle Pk-Pk to the following target values:
  - RBR: 138mV +/- 2%
  - HBR: 450mV +/- 2%
  - HBR2: 300mV +/- 2%

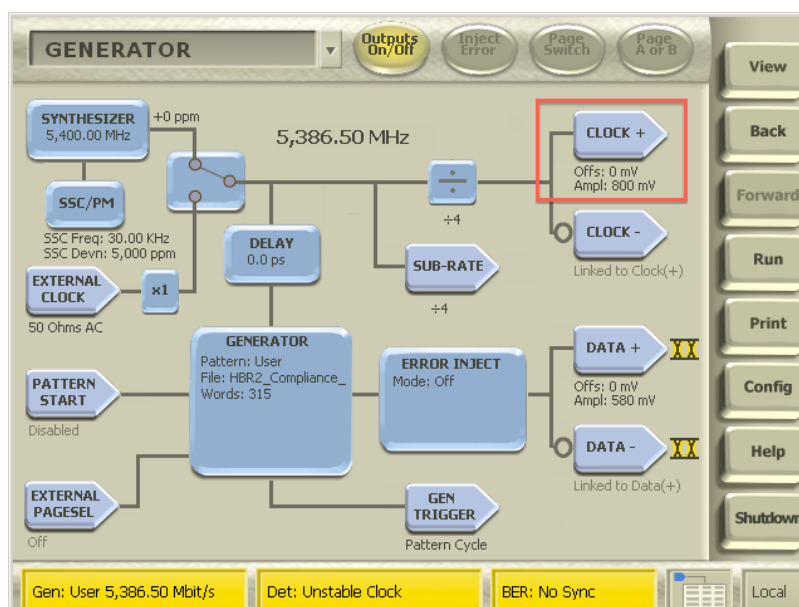


FIGURE 62. HBR2 EYE HEIGHT MEASUREMENT WITH CROSSTALK ADJUSTMENT



FIGURE 63. HBR2 CROSSTALK MEASUREMENT

### 9.2.2 DUT Test Setup and Procedure

The following diagram shows the typical setup for testing the DUT. At TP3, disconnect the 'P' (Plug) type adapter from the 'R' (Receptacle) calibration adapter and connect the 'P' type adapter to the DUT for testing.

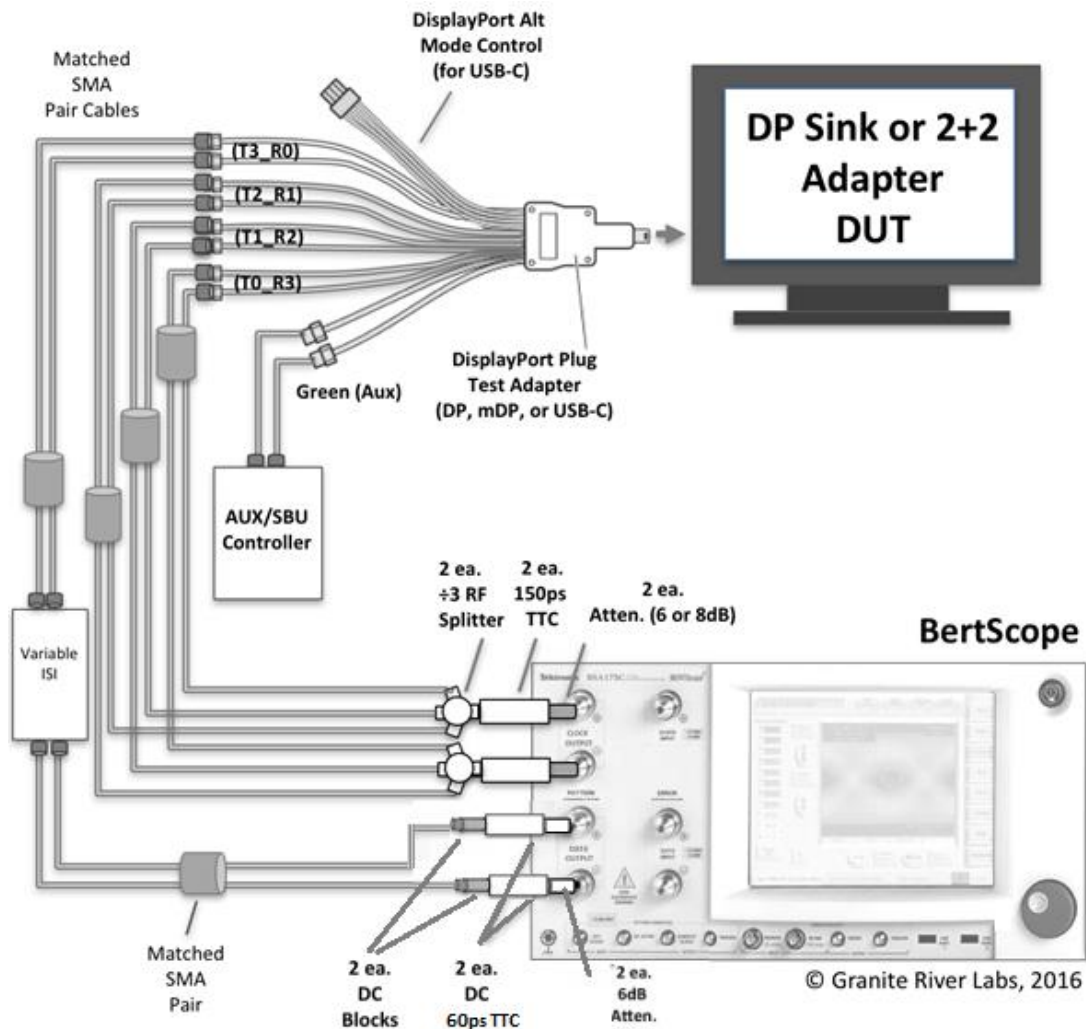


FIGURE 64. TYPICAL DUT TEST SETUP

Test the DUT for each frequency as follows:

1. Verify Frequency Lock using the D10.2 clock pattern for each data rate.
2. Verify Symbol Lock using the Symbol Lock pattern for each data rate and each frequency.
3. Inject Errors with the PRBS7 pattern (for RBR and HBR) or CP2520 Compliance Eye Pattern (for HBR2) and confirm the correct amount of errors is being detected.
4. Test the DUT at each data rate and duration as described in Table 4-3 of the CTS.

**Table 4-3: BER Measurement Test Parameters**

| Jitter Frequency (MHz) | Number of Bits   | Maximum Number of Allowable Bit Errors | Bit Rate | Observation Time (Seconds) <sup>a</sup> | Data Rate Offset |
|------------------------|------------------|--|----------|---|------------------|
| 2                      | 10 <sup>12</sup> | 1000                                   | HBR3     | 123                                     | 0                |
|                        |                  |  | HBR2     | 185                                     |                  |
|                        |                  |  | HBR      | 370                                     |                  |
|                        |                  |  | RBR      | 620                                     |                  |
| 10                     | 10 <sup>11</sup> | 100                                    | HBR3     | 13                                      | +350ppm          |
|                        |                  |  | HBR2     | 19                                      |                  |
|                        |                  |  | HBR      | 37                                      |                  |
|                        |                  |  | RBR      | 62                                      |                  |
| 20                     | 10 <sup>11</sup> | 100                                    | HBR3     | 13                                      | 0                |
|                        |                  |  | HBR2     | 19                                      |                  |
|                        |                  |  | HBR      | 37                                      |                  |
|                        |                  |  | RBR      | 62                                      |                  |
| 100                    | 10 <sup>11</sup> | 100                                    | HBR3     | 13                                      | 0                |
|                        |                  |  | HBR2     | 19                                      |                  |
|                        |                  |  | HBR      | 37                                      |                  |

a. To evaluate, the number of bits shall be multiplied by the unit interval (UI) in picoseconds (e.g., for HBR, 10<sup>11</sup> bits at HBR = 370ps/UI × 10<sup>11</sup>UI = 37 seconds).

**FIGURE 65. TABLE OF TEST TIMES FOR EACH LINK RATE PER CTS**

## 10 Appendix B: Connecting Tektronix Oscilloscope to PC

The following procedure explains how to connect the Tektronix DPOJET Series oscilloscope to be used with a PC. The Tektronix Scope can be connected to the PC through GPIB, USB, or LAN.

1. Download the latest version of the Tektronix TekVISA software from the Tektronix website and install on the PC.
2. When installed successfully, open the OpenChoice Instrument Manager application.

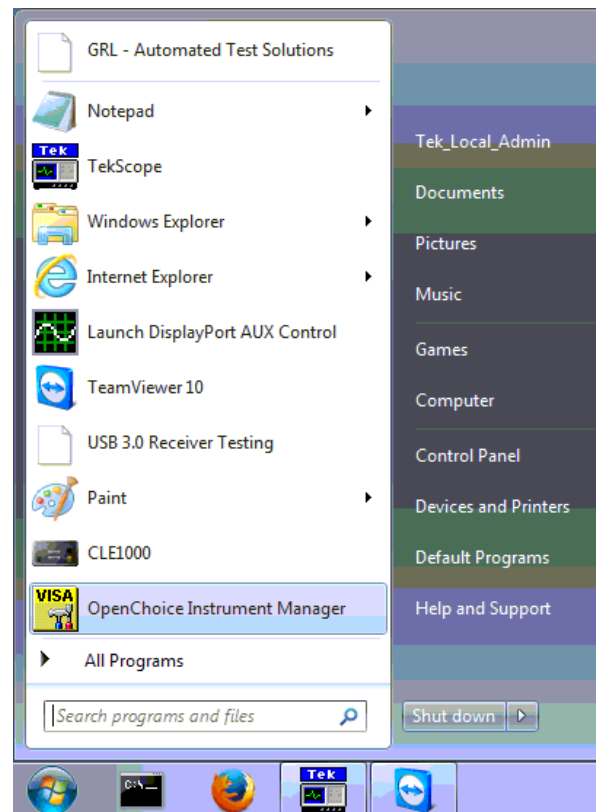


FIGURE 66. OPENCHOICE INSTRUMENT MANAGER IN START MENU

3. The left “Instruments” panel on the OpenChoice Instrument Manager will display all connected instruments. The functional buttons below the “Instruments” panel – “Instrument List Update”, “Search Criteria”, “Instrument Identify” and “Properties” can be used to detect the Scope in case it does not initially appear under “Instruments”.
  - a) “Instrument List Update”: Select to refresh the instrument list and locate new instruments connected to the PC.
  - b) “Search Criteria”: Select to configure the instrument search function.
  - c) “Instrument Identify”: Select to use a supported programming language to send a query to identify the selected instrument.
  - d) “Properties”: Select to display and view the selected instrument properties.

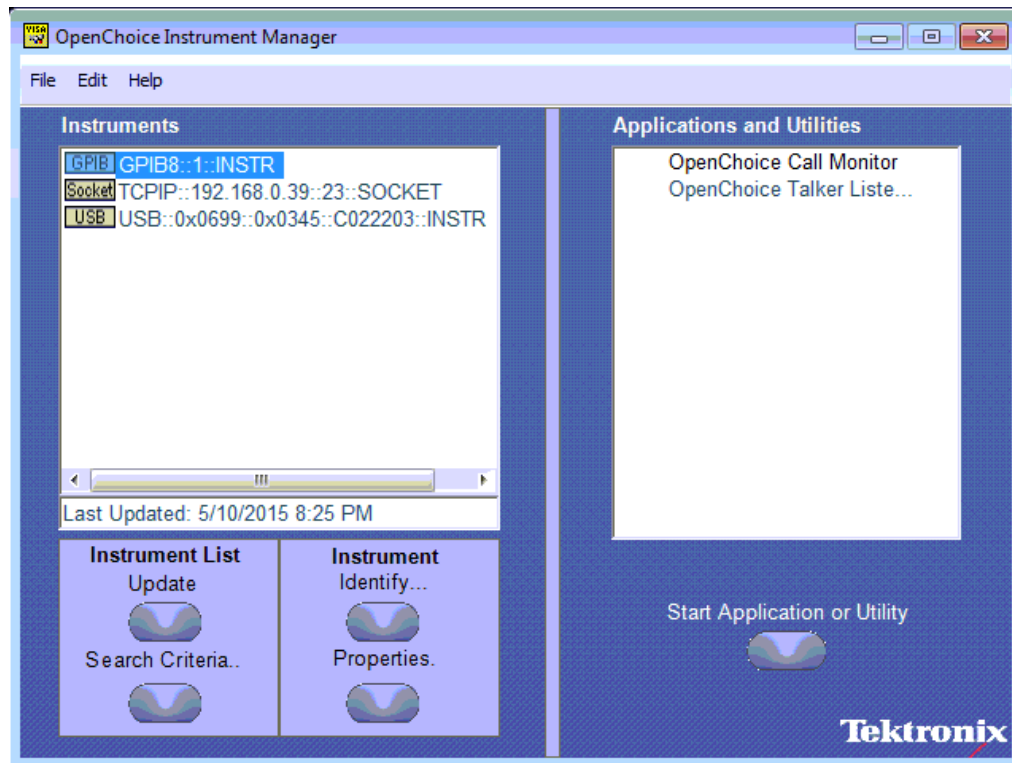


FIGURE 67. OPENCHOICE INSTRUMENT MANAGER MENU

4. If connecting the Tektronix Scope to the PC via USB, select the “Search Criteria” function to ensure that USB connection is enabled, and then select the “Instrument List Update” function. When the Scope appears on the “Instruments” panel, select it and then go to the “Instrument Identify” function. This will display the model and serial number of the Scope once detected. Select the “Properties” function to view the Scope address.
5. If connecting the Tektronix Scope to the PC via LAN, the Scope IP address must be pre-determined beforehand. Then select the “Search Criteria” function to ensure that LAN connection is enabled and type in the Scope IP address. When the Scope shows up in the list, select it followed by “Search”. The Scope should then appear on the “Instruments” panel. Select it and access the “Instrument Identify” function to view the Scope model and serial number as well as the “Properties” function to view the Scope address.
6. On the Equipment Setup page of the GRL DisplayPort 1.4 Sink Test Application, type in the Scope address into the ‘Address’ field. If the GRL DisplayPort 1.4 Sink Test Application is installed on the Tektronix Scope, ensure the Scope is connected via GPIB and type in the GPIB network address, for example “GPIB8::1::INSTR”. If the GRL software is installed on the PC to control the Scope, type in the Scope IP address, for example “TCPIP0::192.168.0.110::inst0::INSTR”. Note to omit the Port number from the address.

# 11 Appendix C: Artek CLE1000-A2 Installation

## 11.1 Install ISI Generator Driver

If using the Artek CLE1000-A2 for Variable ISI Calibration, follow these steps to install the ISI generator driver before selecting it as an ISI channel in the GRL software.

1. Connect the CLE1000-A2 to a controller PC using a USB 2.0 cable.
2. Turn on the front panel power switch on the CLE1000-A2.
3. Right-click on **My Computer > Manage > Device Manager**. If no software for the CLE1000-A2 has been installed, you will see a 'bang' in the Device Manager.

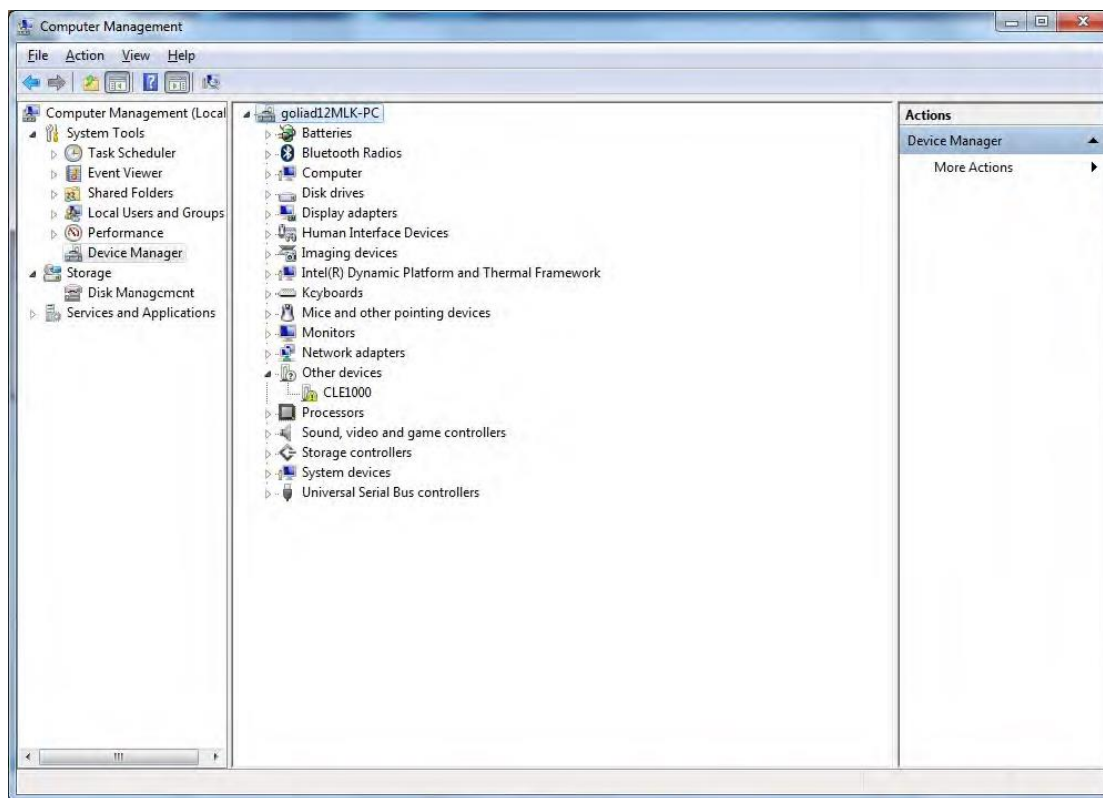


FIGURE 68. DEVICE MANAGER WINDOW

4. To install the CLE1000-A2, go to <http://www.aceunitech.com/support.html> and download the Control Software package for the CLE1000.
5. Unpack the CLE1000 Software .zip file.
6. Install the CLE1000 Driver:
  - a) In Device Manager, right-click on **CLE1000 > Update Driver**.
  - b) Select **Browse My Computer for Driver** from Windows dialog. See Figure 69.
  - c) Browse to the root directory of the unzipped CLE1000 Software folder.
  - d) Click **Next**. You will be asked to confirm your request to install a driver. See Figure 70.
  - e) Click **Install**. The driver software will complete the installation.



7. Once installation has completed, the CLE1000 should appear in Device Manager as shown in Figure 71.

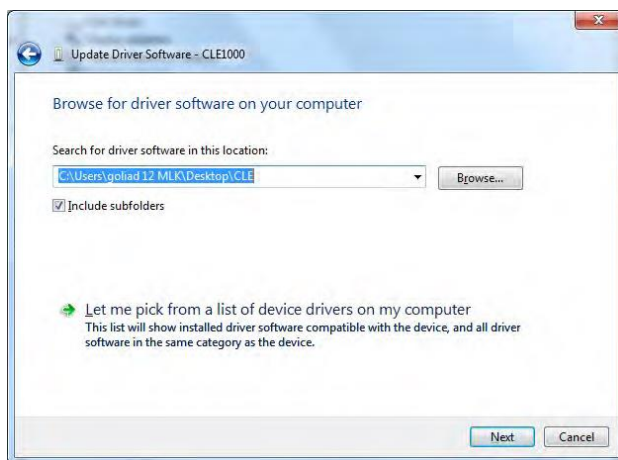


FIGURE 69. UPDATE DRIVER WINDOW

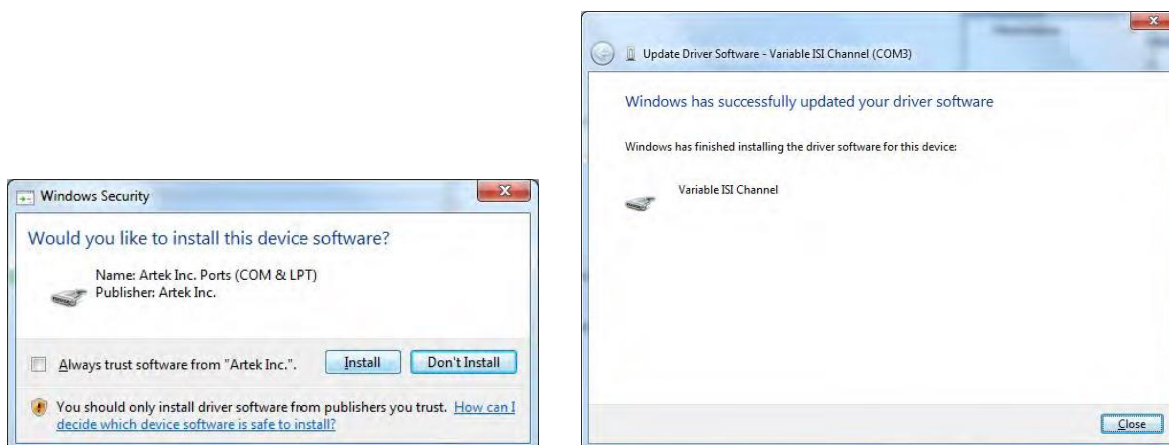


FIGURE 70. WINDOWS SECURITY WINDOW AND CONFIRMATION WINDOW



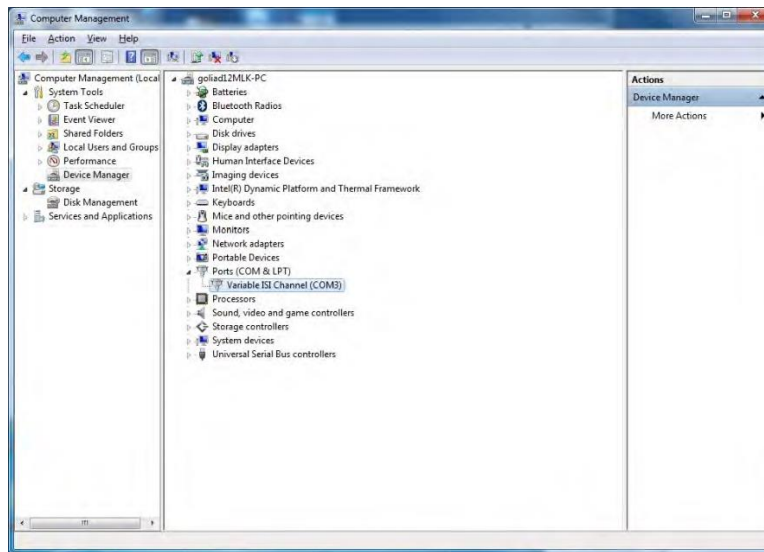


FIGURE 71. DEVICE MANAGER WINDOW AFTER INSTALLATION

The CLE1000 software driver is now installed and the CLE1000-A2 can now be selected for use remotely using the GRL software.

## 11.2 Install CLE1000 GUI

It may also be useful to install the CLE1000 GUI, so that the ISI channel can also be controlled manually from the controller PC. To install the software, do the following:

1. In the CLE1000 SW folder, click on the Setup.exe file. Once installed successfully, the following GUI will appear on the desktop.
2. You can now close the GUI if you do not want to have manual control.

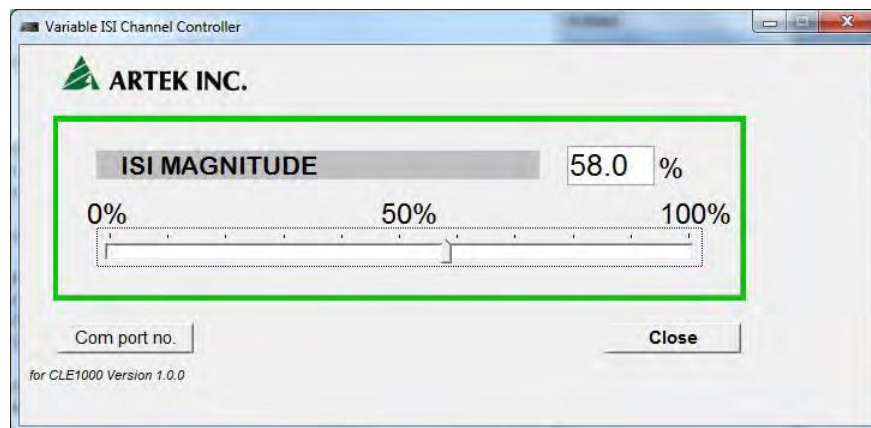


FIGURE 72. CLE1000 GUI

## 12 Appendix D: AUX Controller Driver Installation

### 12.1 Install Tektronix DP-AUX Driver

If the Tektronix DP-AUX is being used as the AUX controller, follow these steps to install the DP-AUX driver before selecting it as the AUX controller in the GRL software.

1. Connect the DP-AUX to a controller PC using a USB 2.0 cable.
2. Right-click on **My Computer > Manage > Device Manager**. If no software for the DP-AUX has been installed, you will see a 'bang' in the Device Manager as an Unknown device.

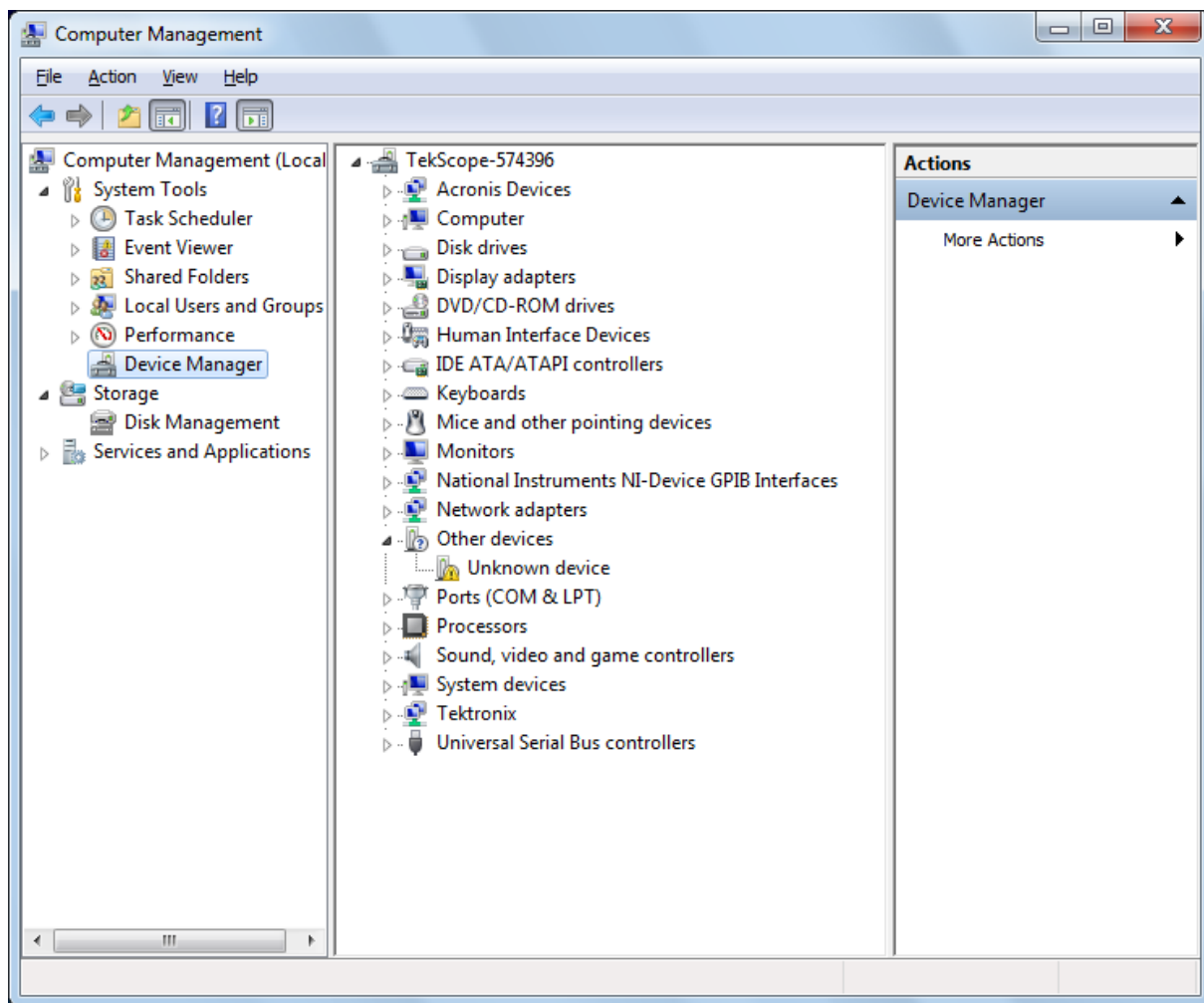


FIGURE 73. DEVICE MANAGER WINDOW

3. To install the DP-AUX driver software, go to [www.tek.com](http://www.tek.com) and download the Control Software package for the DP-AUX.
4. Open the DP-AUX Software .zip file and install the DP-AUX driver:
  - a) In the DP-AUX Software folder, run the setup installer file to start the installation.

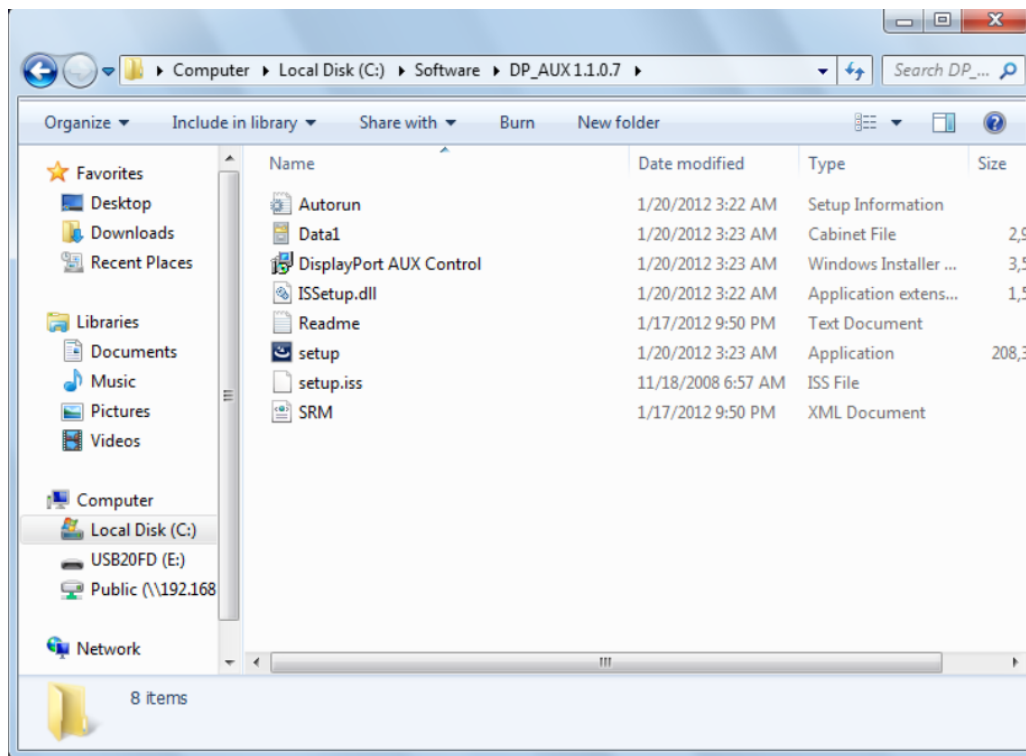


FIGURE 74. SELECT AND RUN INSTALLER FILE

- b) When installation is running, the following dialog will appear. Select 'Install this driver software anyway' to proceed.

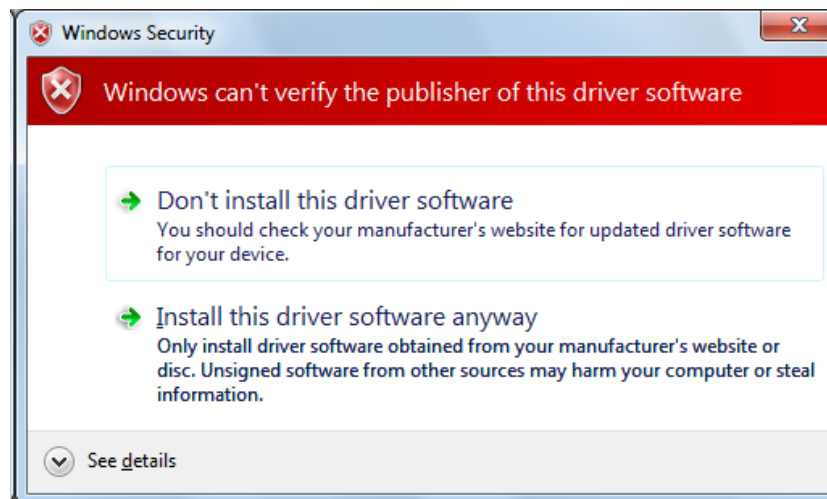


FIGURE 75. INSTALLATION DIALOG #1

- c) You will then be prompted with the following dialog. Select 'OK' (Note: This dialog is not applicable and can be ignored since the Found New Hardware wizard does not appear when the DP-AUX is plugged in).

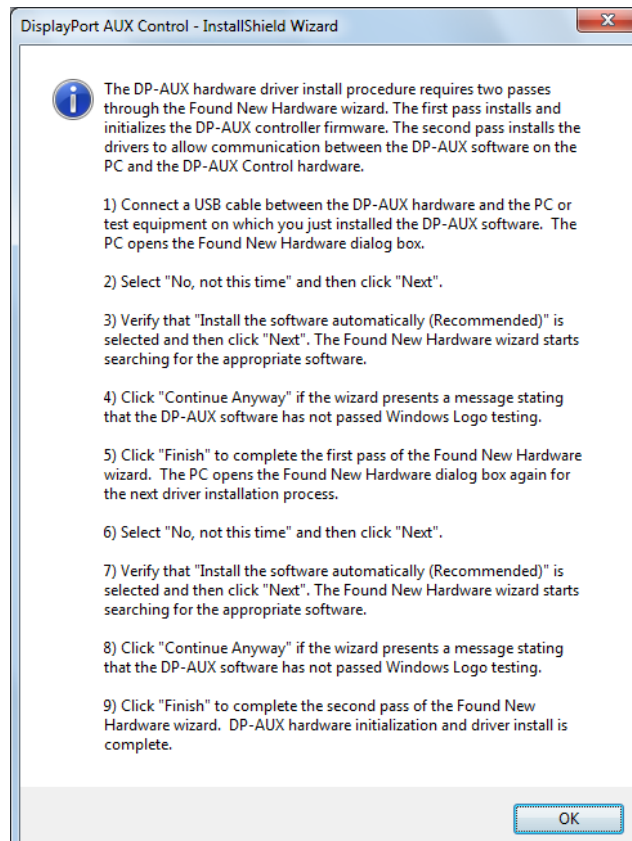


FIGURE 76. INSTALLATION DIALOG #2

d) Once installation has completed, the DP-AUX will show up in Device Manager as follows:

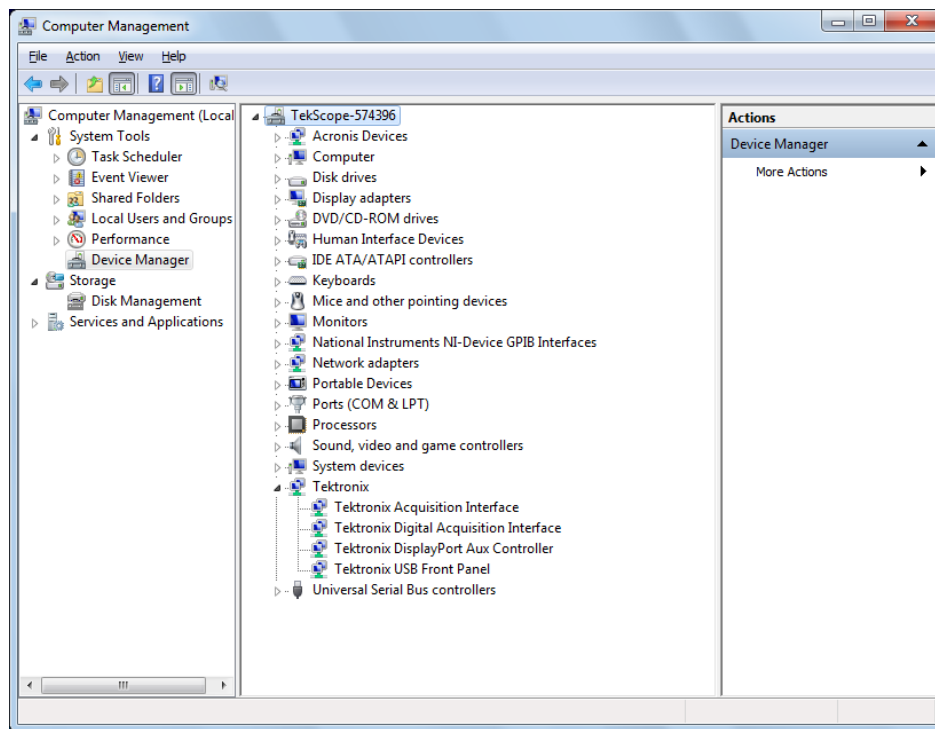


FIGURE 77. DP-AUX INSTALLATION COMPLETED

## 12.2 Install Unigraf DPT-200 Driver

If the Unigraf DPT-200 is being used as the AUX controller, follow these steps to install the DPT-200 driver before selecting it as the AUX controller in the GRL software.

1. Attach the Unigraf DPT-200 to a USB port on the oscilloscope.
2. On the scope, right-click on **My Computer > Manage > Device Manager**. If the DPT-200 driver has not been installed, it will appear as follows:

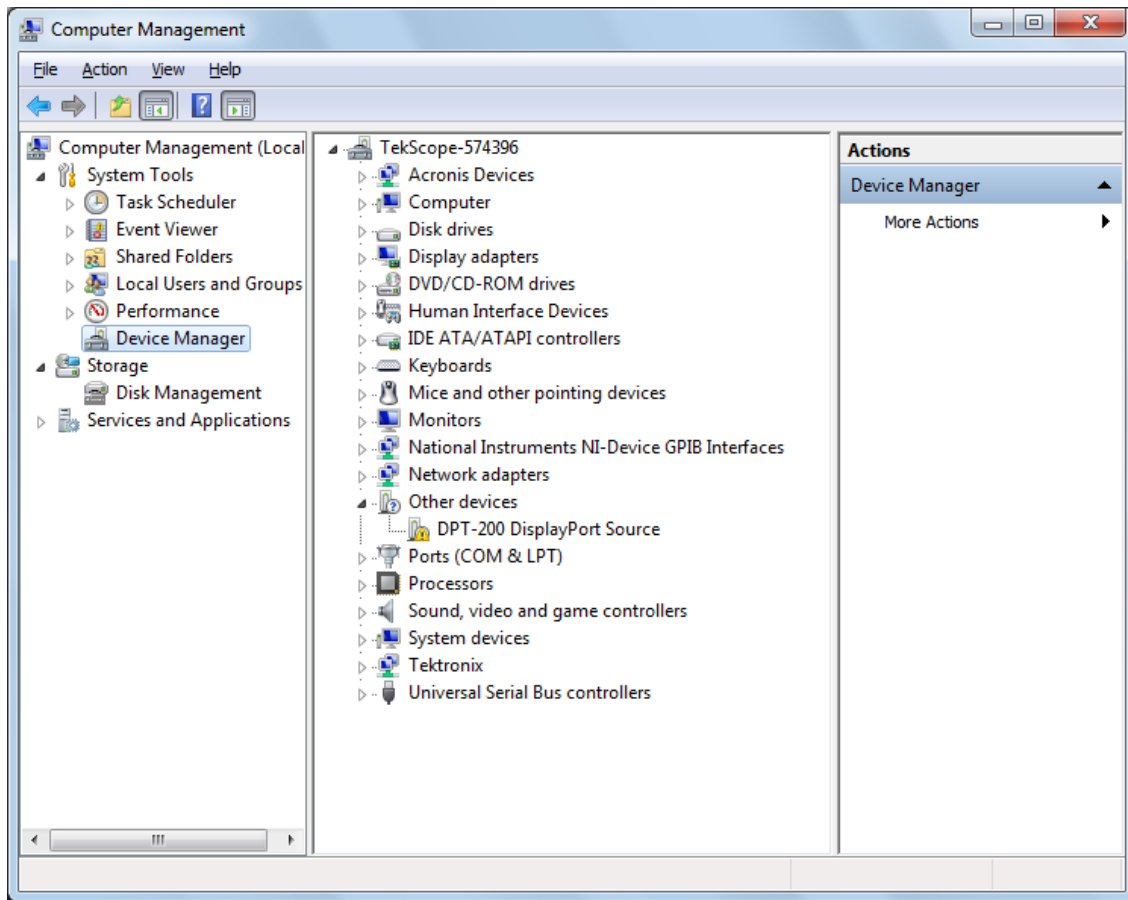


FIGURE 78. DEVICE MANAGER WINDOW

3. To install the DPT-200 driver software, go to [http://www.unigraf.fi.unixtemp.saunalahti.fi/files/download/DisplayPort/Reference%20Controller/UGDP-Reference-Controller-1\\_0.zip](http://www.unigraf.fi.unixtemp.saunalahti.fi/files/download/DisplayPort/Reference%20Controller/UGDP-Reference-Controller-1_0.zip) and download the Installer package to the hard drive of your PC.
4. Open the Installer package .zip file and install the DPT-200 driver:
  - a) Run the setup installer file to start the installation and follow the instructions on the screen.
  - b) During installation, the following dialog will appear. Select 'Install this driver software anyway' to proceed.

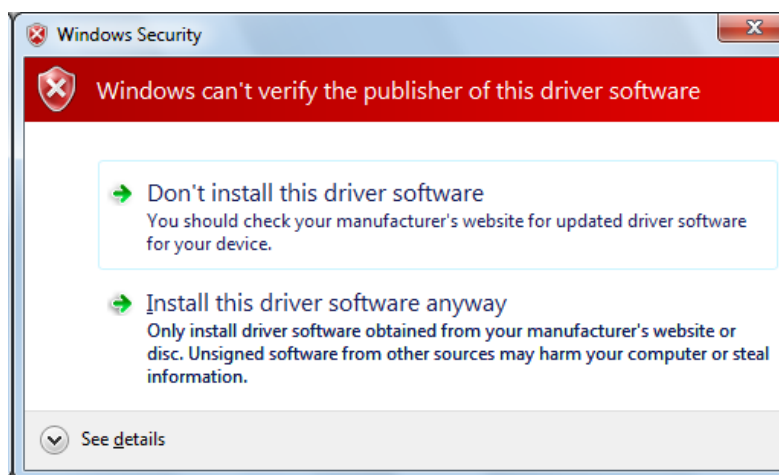


FIGURE 79. INSTALLATION DIALOG

c) Once installation has completed, the DPT-200 will appear in Device Manager as follows:

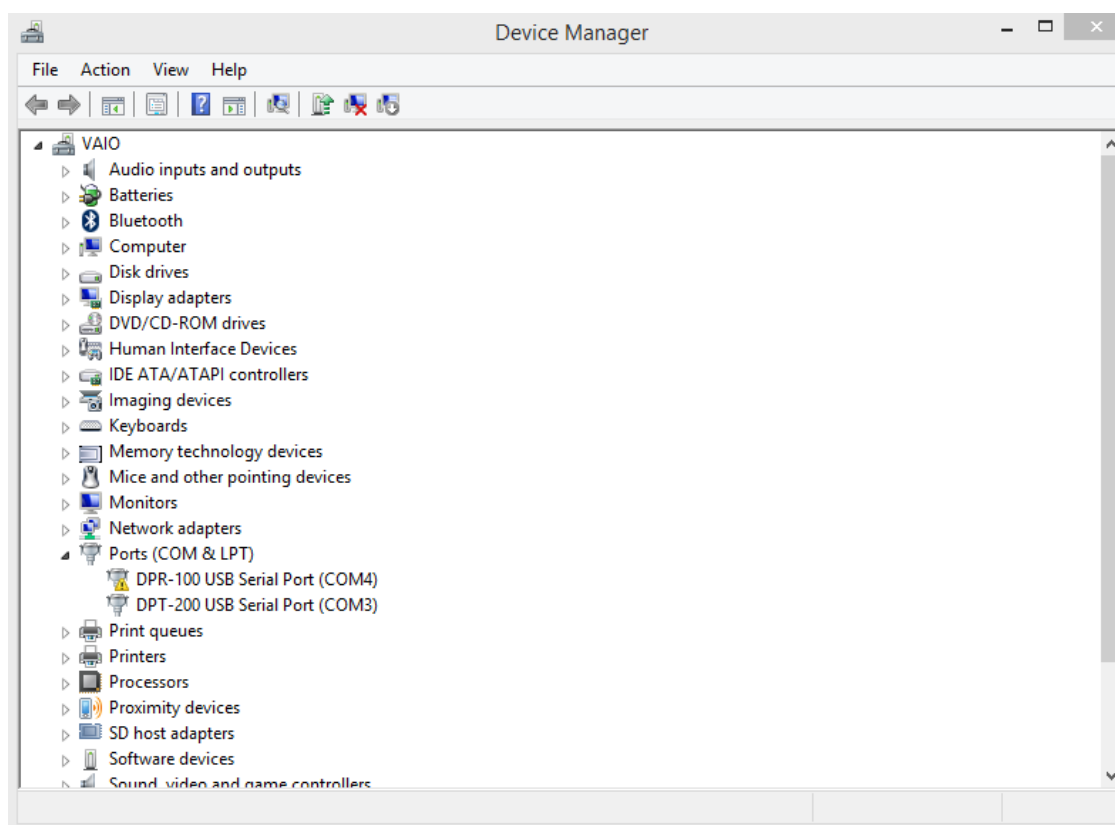


FIGURE 80. DPT-200 INSTALLATION COMPLETED

**END\_OF\_DOCUMENT**

*<Reserved for Internal GRL Use Only>*