# 60-Pin Emulation Header

# User's Guide

Literature Number: SPRU655C
March 2007

Texas Instruments

# Contents

# List of Figures

# List of Tables

# Read This First

## About This Manual

This technical reference describes how to incorporate Texas Instruments' next-generation emulation header on a board with a trace-enabled DSP.

## Key Changes

This document's organization has significantly changed from the previous version. It is now a quick reference guide with supplemental information as an appendix to each chapter. Additionally, this document includes material that covers multiprocessor configurations.

Note that each main section has a summary component to identify key areas addressed in that section:

**Table 1. Summary: Example**

| | |
|---|---|
| 1 | Key points or examples will go here. |
| 2 | Key points or examples will go here. |

## Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers are shown with the suffix h. For example, the following number is 40 hexadecimal (decimal 64): 40h.
- Registers in this document are shown in figures and described in tables.
  - Each register figure shows a rectangle divided into fields that represent the fields of the register. Each field is labeled with its bit name, its beginning and ending bit numbers above, and its read/write properties below. A legend explains the notation used for the properties.
  - Reserved bits in a register figure designate a bit that is used for future device expansion.
- Measurements are in English standard units (inches, pounds, etc.).

## Related Documentation From Texas Instruments

The following documents describe the C6000 DSP platform and related support tools. Copies of these documents are available on the Internet at www.ti.com. *Tip:* Enter the literature number in the search box provided at www.ti.com.

***Emulation Fundamentals for TI's DSP Solutions*** (SPRA439) This paper will explain the fundamentals of how the emulation logic and emulation tools work together with the TI digital signal processors. By understanding the fundamentals of emulation, you will be able to accelerate the process of setting up and performing software debug, as well as aid in troubleshooting potential problems in the debugging setup. A detailed explanation of the setup of the emulator hardware systems for single and multi-processor applications, along with a discussion of how the system components interact during debug will be discussed in the sections to follow. Also included is a troubleshooting guide to assist in common setup problems.

***TMS320C6000 DSP Designing for JTAG Emulation Reference Guide*** (SPRU641) This document assists you in meeting the design requirements of the XDS510 emulator with respect to JTAG designs and discusses the XDS510 cable. This cable supports both standard 3-volt and 5-volt target system power inputs.

***XDS560 Emulator Reference Guide*** (SPRU589) This technical reference describes the fundamentals of the XDS560 PCI Emulator and Pod and how to interface it to a target system.

***Standard Test Access Port and Boundary-Scan Architecture – Description*** (IEEE 1149.1) A standard defining test accessibility, also referred to as Boundary Scan.

***JTAG/MPSD Emulation Technical Reference*** (SPDU079) A reference guide that provides detailed information to be used when designing for JTAG emulation.

***Common Trace Transmission Problems and Solutions*** (SPRAAK6) This document provides guidelines for identifying and solving common problems associated with the collecting of high speed data. On a trace-capable device, the trace interface is one of the highest performance interfaces. Although only used during design, development, and debug, the trace interface must be implemented correctly for full functionality and performance.

## Trademarks

# 60-Pin Emulation Header

This technical reference describes the requirements necessary to incorporate Texas Instruments' next generation emulation header on a board that includes a trace-enabled DSP.

## 1 Introduction

The new 60-pin header replaces the standard 14-pin header. The 60-pin header supports existing JTAG scan and multiprocessor breakpoints, and provides additional EMU pins for future features. Even though the 60-pin header supports all the features provided by the original 14-pin header, not all emulators, target cables, and target device combinations support all features. See the documentation and device user guides for your specific emulator to confirm that the desired functionality is supported.

Two adapters are available. The first one allows a 14-pin target cable, such as the one provided with a XDS510™ or XDS560™ emulator, to be used with the 60-pin header (Figure 1). The other allows a 20-pin target cable, such as the REV D XDS560 Target Cable, to be used with the 60-pin header (Figure 2).

**Note:** Use of any adapter could have a negative impact on performance.

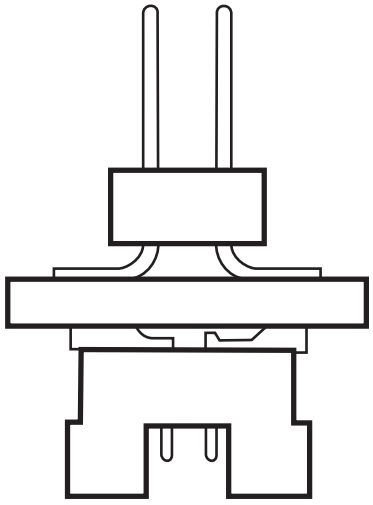


**Figure 1. 60-Pin Target to 14-Pin Emulator Adapter**

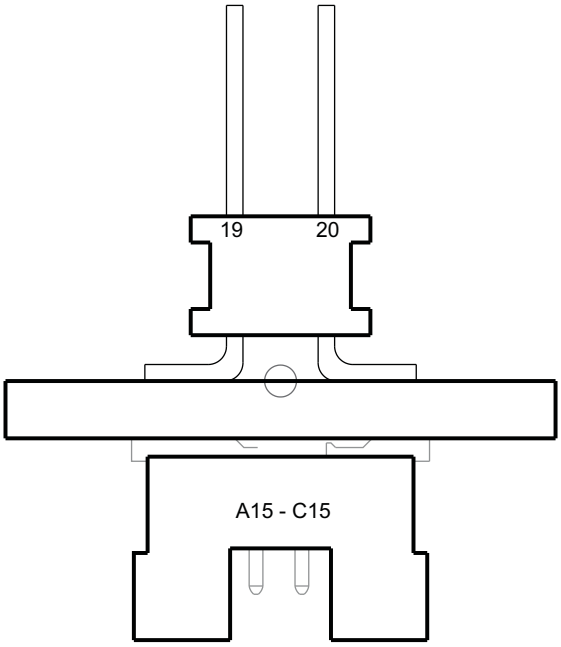



**Figure 2. 60-Pin Target to 20-Pin Emulator Adapter**

## 2 Fundamental Information

**Note:** TI does not recommend placing both 14-pin and 60-pin headers on a board since the performance of trace capabilities will be degraded, but if both headers are incorporated, the design must follow the guidelines within this document.

This technical reference offers guidance for creating new designs that take advantage of the extended emulation capabilities. This document is not intended to be the sole design guide.

In addition to this guide, good engineering practices for high-speed logic design and mechanical layout must be followed. Any deviation from such practices and design techniques will affect the end product performance.

## 3 Alternate Target Impedance Configurations

Within specific end use applications for TI's hardware emulation products, multiple printed circuit board (PCB) trace impedances may be required. The advanced emulation signals connecting to the 60-pin header require a 50 Ω trace impedance for optimal performance.

For DSP target applications that incorporate alternate interfaces including, but not limited to, PCI or external memory interfaces (EMIF), see Appendix A for additional information.

**Table 2. Summary: Alternate Target Impedance Configurations**

| | |
|---|---|
| 1 | Target boards without special considerations must be designed for a 50 Ω character impedance. |
| 2 | All header signals must be routed as if they are clock signal lines operating at 200 MHz. |

## 4 Header Information

The header selected for this next generation emulation interface is manufactured by Samtec™ USA. The next generation header is a surface mount connector containing a total of 60 interconnecting pins, 34 of which are allocated to signals (including static signals), with the remaining 26 pins providing an adequate ground.

Appendix B identifies the specific details of the header selected. Section 7 addresses the specific pin allocation assigned.

**Table 3. Summary: Header Information**

| | |
|---|---|
| 1 | Connector Manufacturer is Samtec USA. |
| 2 | Connector Model number is SOLC-115-02-S-Q-P. |
| 3 | Connector Drawing is located at URL http://www.samtec.com/ftppub/cpdf/SOLC-MKT.PDF |
| 4 | Connector Footprint Drawing is located at URL http://www.samtec.com/ftppub/cpdf/SOLC.PDF |

## 5 Header Footprint Comparisons

The new 60-pin emulation header was chosen because of its high pin count density, high frequency performance, and robustness. A key design constraint was to maintain a form factor for the new header that is similar as possible to the traditional 14-pin header. The following figures illustrate three of the four most common form factors available today, each inclusive of the mating connector when calculated. Figure 3 represents Texas Instruments' 60-pin header, Figure 4 and Figure 5 represent the traditional 14-pin emulator header in a through hole and surface mount configuration, respectively.

A quick calculation (see Table 4) of the new 60-pin header against three other common interfaces results in a modest increase (11.9%) in one case and a 3.2%-21.2% smaller form factor as compared to the remaining two interfaces.

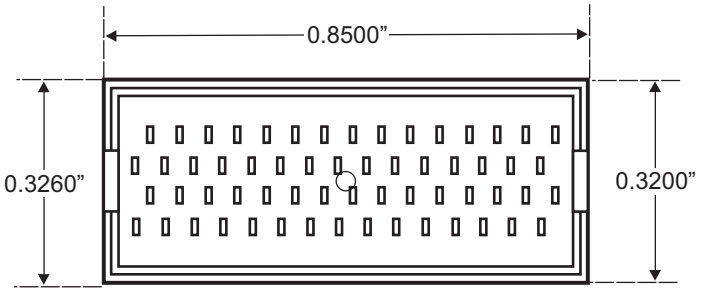



**Figure 3. 60-Pin Emulation Header**

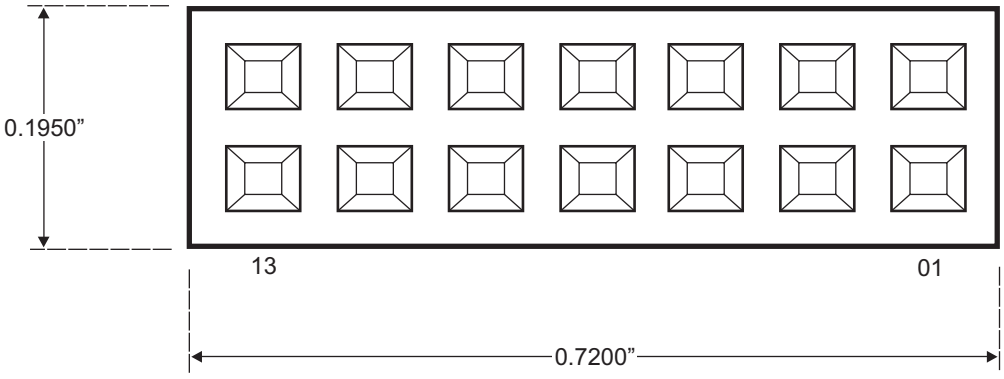



**Figure 4. 14-Pin Traditional Through Hole Emulation Interface**

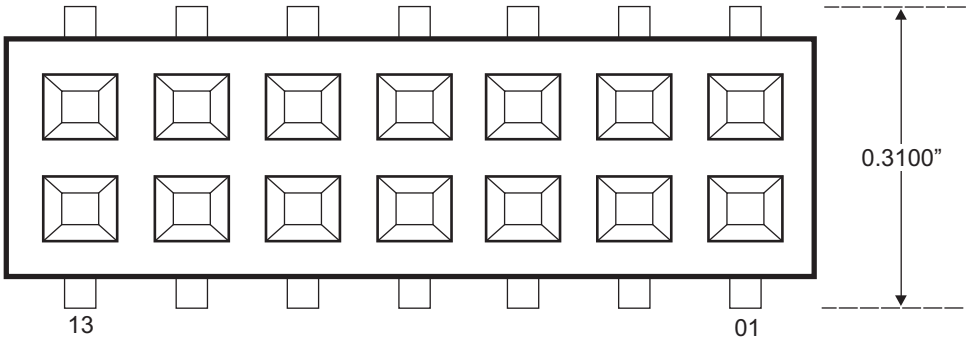



**Figure 5. 14-Pin Traditional SMT Emulation Interface Header**

**Table 4. Summary: Header Footprint Comparisons**

| | Common Emulation Interfaces | Square Inch | Notes |
|---|---|---|---|
| 1 | Original 14-pin SMT connector form factor | 0.2431” | Includes mounting pads |
| 2 | 60-pin next generation emulation header | 0.2720” | Includes mounting pads |
| 3 | Original through hole 14-pin connector form factor | 0.2808” | Includes both sides of PCB |
| 4 | 20-pin ARM™ ETM header | 0.3451” | Includes mounting pads |

## 6 Header Changes

Since the initial release of this document, a change was made to the emulation and debug pod connector to minimize potential pin-to-pin interface problems. This change does not have an impact on routing or layout beyond what is addressed in this document.

**Note:** All headers (emulator and target) should be examined for possible damage before being mated together. Damaged or bent pins may affect functionality and performance.

Never apply excessive force when mating connectors; if excessive force is required, the mating connector pairs are not parallel to one another.

**Table 5. Summary: Header Changes**

| | |
|---|---|
| 1 | Verify the target and emulator headers are intact and free of defects before mating. |
| 2 | Always use caution when mating connectors to ensure no damage occurs. |
| 3 | Verify connectors are parallel to one another before mating. |

# 7 Header Pin Assignment

**Table 6. 60-Pin Header Signal Naming Convention**

| | 60-Pin Header Interface Pinout | | | |
|---|---|---|---|---|
| **Column/Row** | **A** | **B** | **C** | **D** |
| 1 | GND(1) | ID0 | ID2 | NC |
| 2 | GND | TMS | EMU18(2) | GND |
| 3 | GND | EMU17(2) | $\overline{\text{TRST}}$ | GND |
| 4 | GND | TDI | EMU16(2) | GND |
| 5 | GND | EMU14(2) | EMU15(2) | GND |
| 6 | GND | EMU12(2) | EMU13(2) | GND |
| 7 | GND | TDO | EMU11 | GND |
| 8 | TYPE 0 | TVD | TCLKRTN | TYPE 1 |
| 9 | GND | EMU9 | EMU10 | GND |
| 10 | GND | EMU7 | EMU8 | GND |
| 11 | GND | EMU5 | EMU6 | GND |
| 12 | GND | TCLK | EMU4 | GND |
| 13 | GND | EMU2 | EMU3 | GND |
| 14 | GND | EMU0 | EMU1 | GND |
| 15 | $\overline{\text{TGTRST}}$ | ID1 | ID3 | GND |

(1) On some target applications, detection of the emulation pod is required. It is recommended that when this condition exists, pin A1 on the 60-pin header be used. Instead of grounding pin A1 on the target board, a pull-up resistor ≥ to 10K Ω should be connected to the pin. When the emulation pod header is connected, pin A1 will be grounded.

(2) The 60-pin header provides 19 EMU pins for advance emulation features. Not all devices support 19 EMU pins. Connect only the EMU pins present on the target DSP to the corresponding EMU pin on the header.

**Table 7. Summary: Header Pinout**

| | |
|---|---|
| 1 | Pin D1 should be left unconnected. |
| 2 | Pin A1, if required, enables or disables external multiplexers or buffers. |
| 3 | Only the appropriate trace pins should be connected. |

Figure 6 is a top view of Texas Instruments' new 60-pin emulation header, illustrating the orientation and pin location of the 60-pin emulation header. See Table 6 for specific pin assignments. Texas Instruments' new emulation and debug pod now incorporates a pin 1 (red dot) locator on the emulation and debug pod (Figure 7). Alignment with the pin 1 of the target board header is critical.

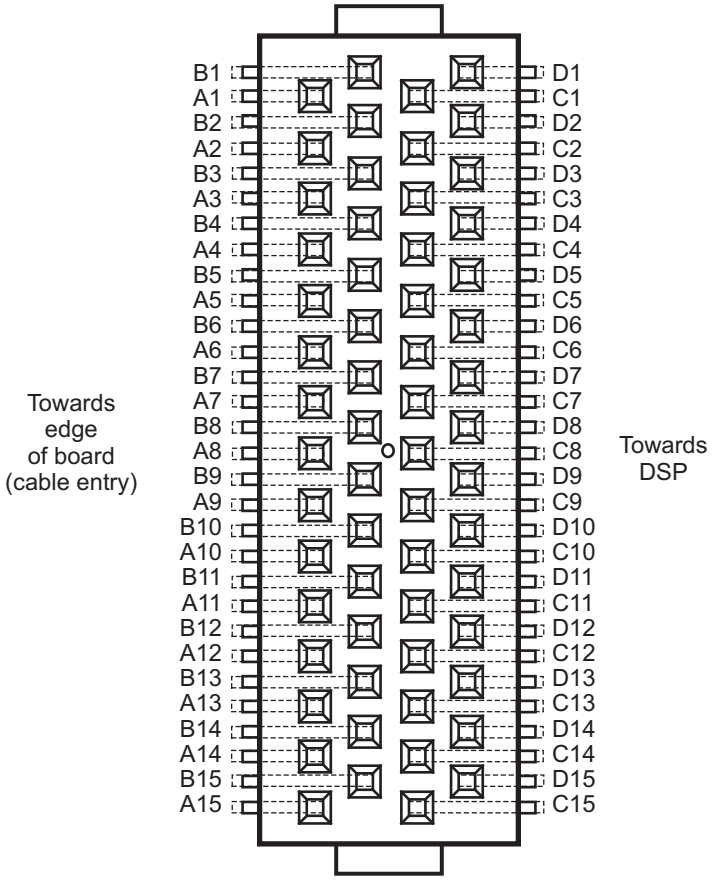



**Figure 6. 60-Pin Header Orientation**

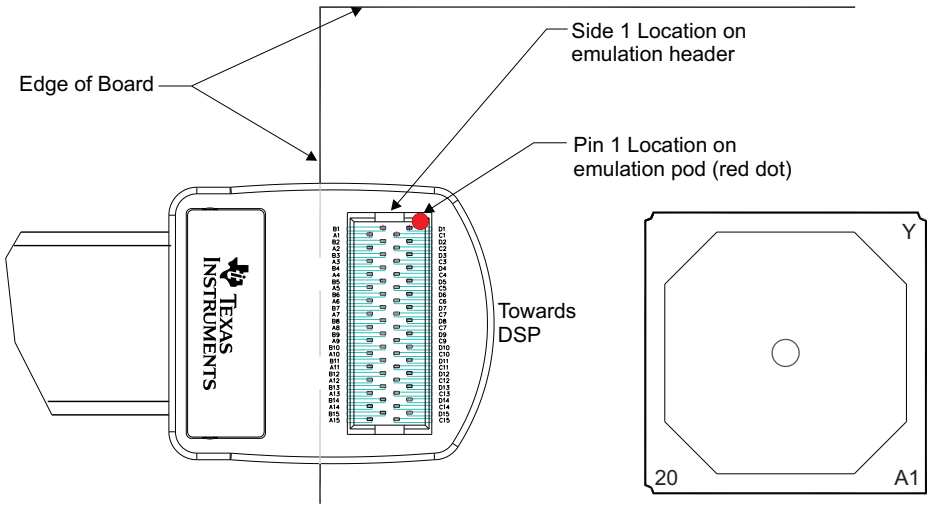



**Figure 7. Emulator Cable Connector Superimposed Over 60-Pin Header**

**Table 8. Summary: Header Pin Location**

| | |
|---|---|
| 1 | Header orientation is critical. |
| 2 | Align the emulation pod pin 1 locator with pin 1 on the target board header. |

## 8 Electrical Requirements

This section describes the basic electrical requirements. Deviation from these requirements may result in performance degradation.

Table 9 defines the chip pin input pull-up and pull-down characteristics.

**Table 9. JTAG Signal Directions**

| Signal Name | DSP Direction | Notes |
|---|---|---|
| EMU[N](1) | Bidirectional | Pull-up within device per device data sheet |
| TCLK | In | Pull-up within device per device data sheet |
| TDI | In | Pull-up within device per device data sheet |
| TDO | Out | Pull-up within device per device data sheet |
| TMS | In | Pull-up within device per device data sheet |
| TRST | In | Pull-down within device per device data sheet |

(1) Varies by device type, see the device data sheet for actual number of EMU pins.

Table 10 lists the header specifications where EMU pins do not exceed 19.

## 9 60-Pin Emulation Header Specifications

**Table 10. Header Connectivity**

| Signal Name | Emulator Signal Direction | Notes |
|---|---|---|
| TMS | Output | Connection to device pin of same name. |
| TDO | Input | Connection to device pin of same name. |
| TDI | Output | Connection to device pin of same name. |
| TRST | Output | Connection to device pin of same name. |
| TCLKRTN | Input | Connected to a board supplied TCLK if one is present. Connected to TCLK or a buffered version of TCLK otherwise. |
| TCLK | Output | Connection to device pin of same name, possibly through buffer. |
| TVD | Input | Chip I/O voltage current limited via 100 Ω resistor. |
| EMU[18:0] (1) | Bidir | Connection to device pin of same name. |
| ID[3:0] | Input | Only header type 0000 is currently supported, where 0 is GND and 1 is a No Connect. All other combinations are reserved. |
| TYPE[1:0] | Output | Pin A8 (Type 0) is an N/C; Pin D8 (Type 1) must be connected to GND. |
| $\overline{\text{TGTRST}}$ | Output | Currently not supported by TI tools. |

(1) Leave unused pins unconnected.

**Table 11. Summary: Electrical Requirements**

| | |
|---|---|
| 1 | Always refer to the device data sheet for number and connectivity of EMU pins. |
| 3 | Leave unused EMU pins unconnected. |

## 10 Terminations

All signals are assumed to operate at a minimum of 200 MHz and should be designed as if they were clock signals. All signals are assumed to have rise times of 500–1000 picoseconds. It is assumed that the impedance of the PCB traces from the DSP to the 60-pin header is controlled and is between 50 Ω and 55 Ω.

Table 12 describes the recommended termination values by signal names.

**Table 12. Termination Values and Use Cases**

| Signal Name | Serial Termination Value in Ωs | Notes |
|---|---|---|
| TMS | 42 (1) | Must be placed as closely as possible to the pin on the device, not to exceed 1” trace length from the pin. |
| TDO | 42 | Must be placed as closely as possible to the pin on the device, not to exceed 1” trace length from the pin. |
| TDI | 42 (1) | Must be placed as closely as possible to the pin on the device, not to exceed 1” trace length from the pin. |
| $\overline{\text{TRST}}$ | - | Input |
| TCLKRTN | - | If not buffered, this signal is routed from TCLK with a 22 Ω series resistor with a trace length as short as possible. If buffered, see Figure C-2. If unbuffered, see Figure C-3. |
| TCLK | See note (1) | 100 Ω in series with 8.2 pF parallel termination to ground for buffered TCLK configuration (Figure C-1). Use a 22 Ω series termination (near header) for unbuffered configuration (Figure C-2), unless the data sheet indicates this pin is an output, in which case use a 42 Ω resistor near the DSP. Values should be modeled to ensure proper value. |
| EMU[N:2] | 42 | Must be placed as close as possible to the EMU pin on the device, placement should not exceed 1” trace length from the pin at the DSP. See Figure C-3. |
| EMU[1:0] | 42 | Must be placed as close as possible to the EMU pin on the device, placement should not exceed 1” (0.5” recommended) trace length from the pin of the DSP. If a 14-pin header is used in parallel (not recommended), a separate 42 Ω resistor must be used to route these signals to the 14-pin header, see Figure C-4. |

(1) If the data sheet indicates these pins can be outputs, then the series termination resistors are required. Otherwise, no termination resistors are required.

See Section 16 and Appendix C for additional information on the trace lengths and impact of termination location.

**Table 13. Summary: Terminations**

| | |
|---|---|
| 1 | Use of 42 Ω terminations is based on 50 Ω target designs. |
| 2 | Alternate termination values should be used if indicated by detailed modeling. |
| 3 | Model all critical nets to ensure termination values are correct. |
| 4 | Placement of indicated terminations is critical. |

## 11 Buffering

The series termination value recommended assumes a source impedance between 5 Ω and 7 Ω. If the device output impedance is significantly different, the series termination values may need to be changed accordingly. The circuit should be simulated to determine the best value based on the device IBIS simulation models and/or data sheet.

If buffers are used, they should be selected based on the DSP source impedance and the potential load(s). In applications where multiple DSPs are used, selection of buffers and signals to be buffered are critical.

When buffering signals, it is imperative that timing, propagation delay, sink and source currents, and general buffer characteristics be considered.

See Appendix C for additional information on the buffering, location, and type of buffers to be used.

**Table 14. Summary: Buffering**

| | |
|---|---|
| 1 | Buffer signals based on loading and signal integrity. |
| 2 | In most cases, a single target board is better than a target board with daughter cards consisting of multiple headers. |
| 3 | Timing is a critical consideration for all active signals. |
| 4 | Model all critical nets to ensure termination values are correct. |

## 12 General Specifications

General specifications are shown in Table 15.

**Table 15. General Specifications**

| Item | Description/Specification |
|---|---|
| Impedance | Target board impedance should be in the range of 50 Ω (+5 / –0 Ω). |
| Connector Spacing | Maximum distance from header pin to respective emulation pin on DSP equals 2.0 inch trace length (1.5" recommended). |
| Board Material | Composite laminate FR–4. |
| Signal Skew | For EMU[18:00] signals, skew induced by the board should be 0 to 200 ps maximum between signals. |
| Capacitance | Maximum capacitance loading per pin (inclusive of all vias and components) equals 20 pF. |
| Signal Interconnect | Number of vias, not more than 2, and must be within the capacitive loading specified above. |
| Clock Source | TCLKRTN, pin number C8, is for a customer supplied clock source or TCLK return. A customer supplied clock source must not exceed a 3.3-V logic level. |
| Voltage Source | TVD, pin number B8, requires a current limited customer supplied voltage reference source. |
| Voltage Range | The TI emulation system is designed to operate between 0.5 V and 5.0 V. |
| Orientation Detect | Pin A8 is an N/C; pin D8 must be connected to GND. |
| Board Plating | Recommended is immersion gold, alternate is palladium or heavy gold. |
| Vertical Connector Clearance | Clearance for connector to be 1.2"× 1.0" min (include additional space for grasping). See Figure 13. |
| Horizontal Connector Clearance | Clearance surrounding the 60-pin emulator connector should be per Figure 14, Figure 15, and Figure 16. |
| Signal Frequency | All signals are assumed to be clock signals and operating at 200 MHz, any signal can change direction dynamically. |
| Rise and Fall times | All rising and falling edges are assumed to be within 500–1500 picoseconds. |

## 13 Acceptable Signal Qualifications

The criteria for determining an acceptable signal waveform during simulation at the LVDS receiver within the emulator, or in actual application are illustrated in Figure 8. All percentages listed are with respect to the $V^{High}$ reference levels ( LVTTL 3.3 V). See Figure 8 for the corresponding graph points for the following list.

A. Details the maximum amount of reflection, or protobations that may occur on the rising edge (pre-shoot). The magnitude of the reflections or protobations should be less than 20% of $V^{High}$.

B. Details the critical signal switching region. No inflections greater than 10% of the rise time or 5% greater than $V^{High}$ are allowed. It is preferred that the signal be able to increase monotonically.

C. Details the region of the rising edge above the critical signal switching area. Inflections and/or protobations are allowed within this region as long as they do not exceed 20% of $V^{High}$ or a duration less than the rise time of the pulse.

D. Details the top of the pulse. The amplitude of all noise, crosstalk and other protobations should be less than 10% of $V^{High}$. For a 3.3 V signal, the amplitude should not exceed 165 mV.

E. Details the maximum amount of reflection, or protobations that may occur on the falling edge. The magnitude of the reflections or protobations should be less than 20% of $V^{High}$.

F. Details the critical signal-switching region. No inflections greater than 10% of the fall time or 5% greater than $V^{High}$ are allowed. It is preferred that the signal be able to decrease monotonically.

G. Details the region of the falling edge below the critical signal switching area. Inflections and/or protobations are allowed within this region as long as they do not exceed 20% of $V^{High}$ or a duration less than the fall time of the pulse.

H. Details the bottom of the pulse. The amplitude of all noise, crosstalk and other protobations should be less than 10% of $V^{High}$.

- Duty cycle distortion should be less than 5%
- All waveforms should be treated as dual edge clocks
- Rise and fall times should be symmetrical
- Switching thresholds are assumed to be 50% of $V^{High}$

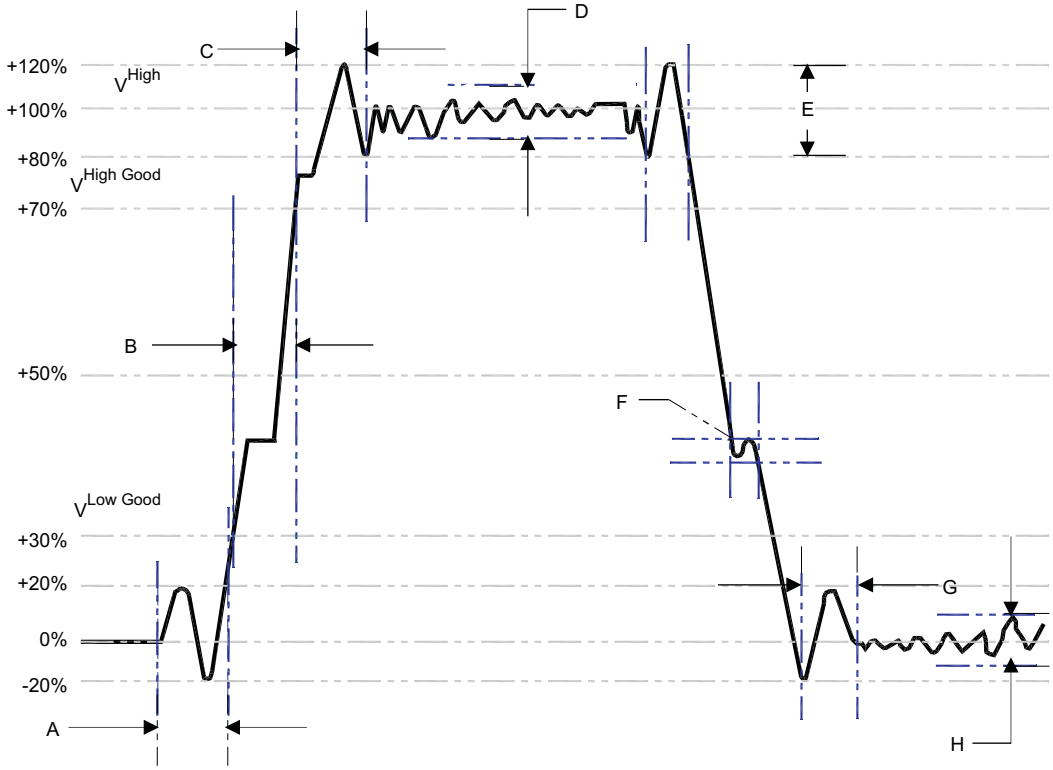



**Figure 8. Acceptable Wave Form Criteria**

**Table 16. Summary: Acceptable Signals**

| | |
|---|---|
| 1 | Calculate reflections to verify they will not fall within the switching regions. |
| 2 | Protobations should not exceed 20% of $V^{High}$. |
| 3 | Rise and fall times should be symmetrical. |
| 4 | The duration of overshoots should not exceed 20% of $V^{High}$ or less than the rise time of the pulse. |
| 5 | Noise and crosstalk should not exceed 10% of $V^{High}$ or 165 mV for a 3.3 V signal. |
| 6 | All wave forms should be treated as dual edge clocks. |
| 7 | Duty cycle distortion should be less than 5%. |
| 8 | Switching thresholds are assumed to be 50% of $V^{High}$. |

## 14 Connecting Alternate Headers

Traditional target designs commonly incorporated multiple headers. However, with the advent of higher speed DSPs and faster off chip emulation, it is strongly recommended that newer designs only use a single emulation header.

Traditional TI JTAG emulation operated at a maximum frequency of 10.368 MHz; however, more recent versions of basic scan JTAG now operate in excess of 35 to 50 MHz. More importantly, with the advent of Texas Instruments' new high speed trace that operates at a maximum of 333 MHz (167 dual edge, bi-phase), it is critical to use TI's 60-pin emulation header.

If alternate headers are used, consider how alternate headers, net lengths, timing, and the effect of stubs will impact performance and signal integrity.

### *14.1 14-Pin and 60-Pin Headers in Parallel*

If a board is designed with both (two and more) headers; for example a 14-pin and 60-pin header, the signals should be connected as shown in Figure 9 and Figure 10. Each figure represents a split termination configuration. The traces should be kept as short as possible. The distance from the terminations and the pins on the DSP must not exceed a 0.75 inch trace length. EMU[0] and EMU[1] are terminated in the same manner as TMS, TDI and TDO (see Figure 9 and Figure 10 for recommended terminations). The EMU[2]–EMU[n] terminations are not shown because they are not supported by the 14-pin header.

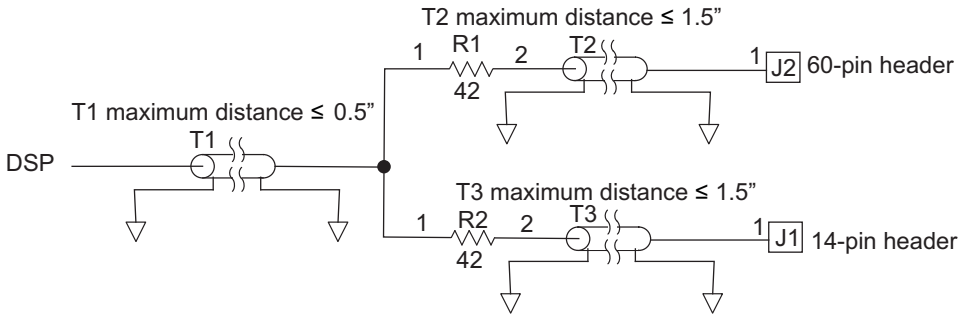



**Figure 9. Multi-Header TMS/TDI/TDO Terminations**

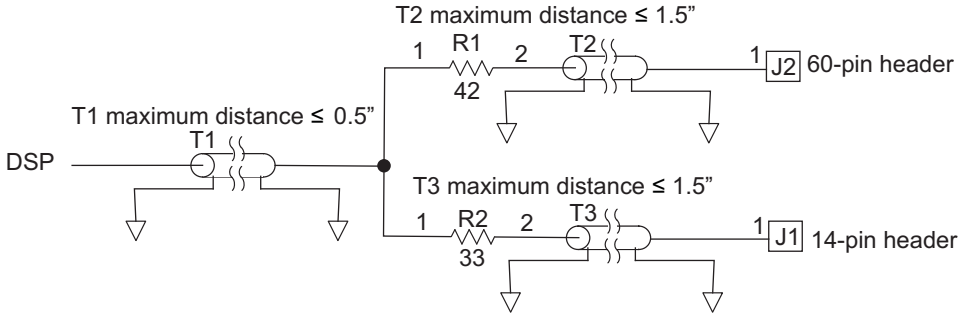



**Figure 10. Multi-Header EMU0/1 Terminations**

Final termination values should be selected based on signal quality. Examine all signals against simulations and functional application. All nodes (see Figure 11) should have symmetrical lengths to the terminations to prevent reflections.

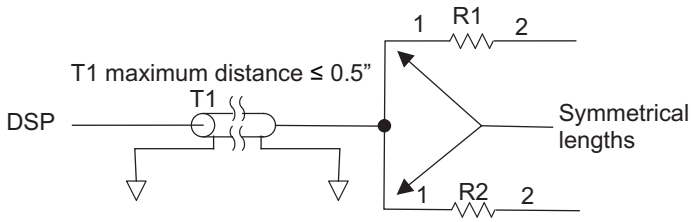



**Figure 11. Symmetrical Nets**

**Table 17. Summary: 14- and 60-Pin Headers in Parallel**

| | |
|---|---|
| 1 | The series termination closest to the DSP should be closer than 0.75”. |
| 2 | Traces originating at nodes should have symmetrical lengths. |
| 3 | The maximum distance originating from the node to the respective header should not exceed 1.5” in length. |
| 4 | Final termination values must be based on simulation and functional testing. |
| 5 | All terminations and nets should be void of stubs. |

# 15 Layout and Routing Requirements

## *15.1 Maximum Recommended Distances*

The layout requires certain specifications. Figure 12 illustrates the maximum recommended routing distance between the header pin and respective DSP EMU (emulation trace) pin. All emulation signals should be treated as a separate net class and routed accordingly. Take special care to meet the skew specifications. See Figure 12 for connector orientation.

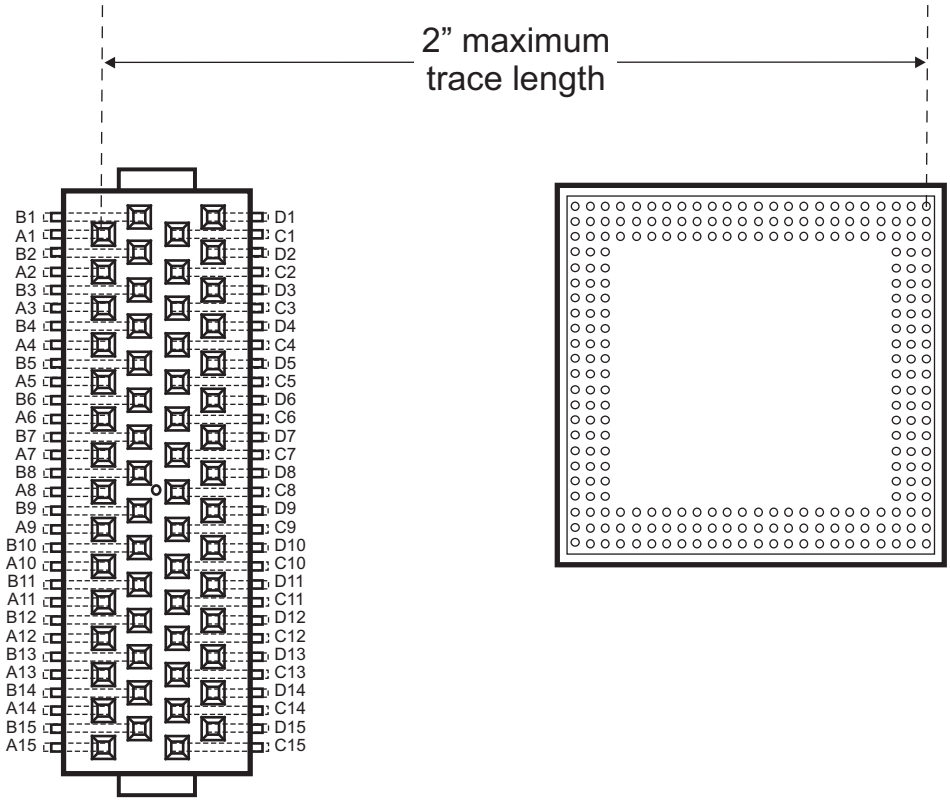



**Figure 12. Maximum Trace Lengths**

The maximum recommended routing distance between a specific DSP pin and the respective pin on the interconnecting 60-pin header should not exceed 2.0 inches.

## *15.2 Implications of Layout and Route Distance Deviations*

An increase in distance (DSP to Header) typically indicates an increased route distance. The implications to an extended route distance could not be fully summarized in this document, as all variables or possible routing methods cannot be considered and documented. Header proximity to the target device is critical for three main reasons: the speed of advanced emulation features, the higher speed traditional JTAG, and the faster rise times and logic speeds of the device itself.

# 16 Advanced Emulation – Layout and Route Distance Deviations

## *16.1 Signal to Signal Clearance*

Consider routing key emulation or clock signals when laying out your target board with respect to the 60-pin emulation header. The potential for signal noise, crosstalk, and coupling increases with the higher frequency of TI's next generation emulators. To minimize this variable, route all clock and emulation (EMU) signals with a minimum of a 5 mil (0.005") clearance, although 6 mil (0.006") is preferred.

## *16.2 Trace Lengths*

Trace length considerations take on two key variables: propagation and skew.

Propagation involves the distance between the header and the respective pin on the DSP. Excessive trace lengths present a problem, specifically with reflections. The key to minimizing the impact of reflections is to minimize trace lengths. When possible, lay out critical signals such that they propagate between the insertion and terminating points in a period of time that does not result in the reflected energy occurring in the switching region or the additive effect of multiple reflections does not fall in the switching regions on either the rising or falling edge. All active trace lengths (specifically for emulation, JTAG, and clock signals) should not exceed 2 inches in length. Lengths in excess of 2 inches increase the risk of reflections occurring in the critical regions of the signal waveform.

The remaining trace length variable is signal skew. For the purposes of this document, signal skew is the difference between the minimum and maximum propagation delays ($T_{pd}$) for a net class (grouping of signals belonging together). In most high speed applications, such as the new emulator, skew is as important as propagation delays. TI's new emulator will accommodate a certain amount of skew; however, excessive skew greater than 176 ps (or 1.0" for FR4) introduced during layout and routing also increases the potential for reduced performance.

Excessive skew or propagation delays increase the risk in potential bit errors, loss of data or faulty operation. Figure 12 illustrates the recommended header distance from the target processor (2" maximum).

While considering the routed length implications of propagation and skew, also consider the total circuit. Most traditional board designers are concerned with only the routes on their board. However, the target board is only one of three critical components of the typical emulation system. The interconnecting pod assembly and emulator are the other critical components. Consider all three components when designing a high-speed functional system.

The advanced emulation pins from the DSP to the header are grouped and routed as a net class to constrain the skew for all EMU[0] through EMU[n] signals. Emulation signals on the target board must be short because of the timing constraints. The distance for the EMU[n] net class of signals can also be interpreted as a maximum routed distance of 2 inches; this is inclusive of all supporting logic in each signal path on the target board. Maintaining a maximum routed length of ≤ 2 inches equals approximately 352 ps of propagation delay. This tight constraint is required because of the combinational/multi-functional logic contained within the interconnecting pod.

Appendix F provides a spice model representing the pod interconnect logic. Deviations from the recommended route distances, loading, or skew must be evaluated using this representative model to ensure optimum frequency operation and overall performance.

**Table 18. Summary: Advanced Emulation Layout and Routing**

| | |
|---|---|
| 1 | All high speed emulation signals (CLKS and EMU) should be spaced a minimum of 5 mil from other signals. |
| 2 | Trace lengths for all clock and EMU signals should not exceed 2" maximum. |
| 3 | Unused EMU pins on the header should be left unconnected. |
| 4 | Skew between signals within a net class should not exceed 176 ps. |
| 5 | Layout and routing should also take into account the emulator and target. |
| 6 | PCB stack up should have a character impedance of 50 Ω. |

# 17 Traditional JTAG Emulation Layout & Route Distance Deviations

Layout and routing considerations include traditional JTAG signals, such as TDI, TDO, TMS, TCLK, and TCLKRTN. The greater the distance (or skew) between the header and the target processor, the greater the potential for timing errors (set up and hold, etc.). Skewing routed signals such as TCLK and TDI, or TDO and TCLKRTN, dramatically reduces the margin of setup timing to and from the target processor. Figure 12 illustrates the recommended header distance from the target processor (2 inches maximum).

As with the advanced emulation features described above, the routed length is equally, if not more important. Traditional JTAG signals, especially in the interconnecting pod, may serve other purposes in future devices. The interconnecting pod assembly has a significant amount of support logic that contains a large portion of the allotted quota of the routed distance. That, coupled with the induced cable propagation delay, requires that the traditional JTAG emulation signals be short.

As stated previously, traditional board designers typically concern themselves with only the routes on the board they are designing. The basic emulation signals are critical, not because of their high speed, but because of their unique timing characteristics. As the TCLK and TCLKRTN rates increase, the margin for setup and hold times decrease, so both must be considered when designing a high speed functional system.

The distance for the traditional JTAG emulation signals can also be interpreted as a maximum routed distance of 2 inches; this is inclusive of all supporting logic in each signal path on the target board. Maintaining a maximum routed length of ≤ 2 inches is equal to approximately 352 ps of propagation delay. This tight constraint is required because of the combinational/multi-functional logic contained within the interconnecting pod. A spice model representing the pod interconnect logic is provided in Appendix F. Deviations from the recommended route distances, loading, or skew must be evaluated using this representative model to ensure optimum frequency operation and overall performance.

**Note: Follow routing guideline for best operating frequency**

Failure to follow the above routing guideline may result in a severely reduced operating frequency, resulting in lost bandwidth or the inability of the advanced features to function at full speed.

## *17.1 Layout and Routing – Mechanical Considerations*

In addition to routing and layout considerations and electrical clearances, certain mechanical clearances must be observed and followed.

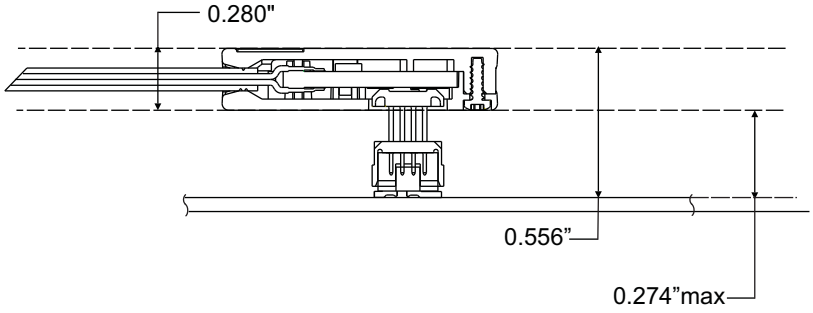



**Figure 13. Minimum Clearance - Height**

Figure 13 illustrates the target board header placement and clearances below the emulation and debug pod connector.

Figure 14 illustrates the top view of the emulation and debug pod header enclosure; additional spacing is required for installing and removing the pod target connector and for clearance of the emulator cable assembly.

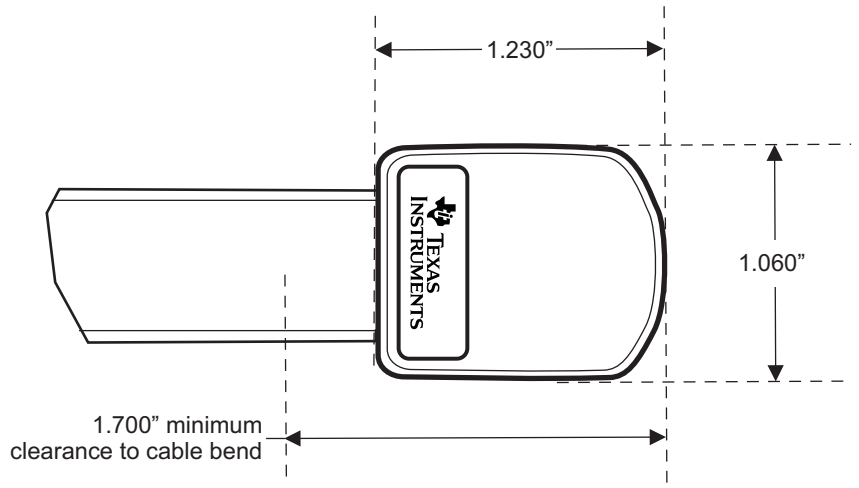



**Figure 14. Emulation and Debug Pod Header Enclosure Dimensions**

Figure 15 illustrates the top view of the emulation and debug pod header enclosure and includes clearances for gripping.

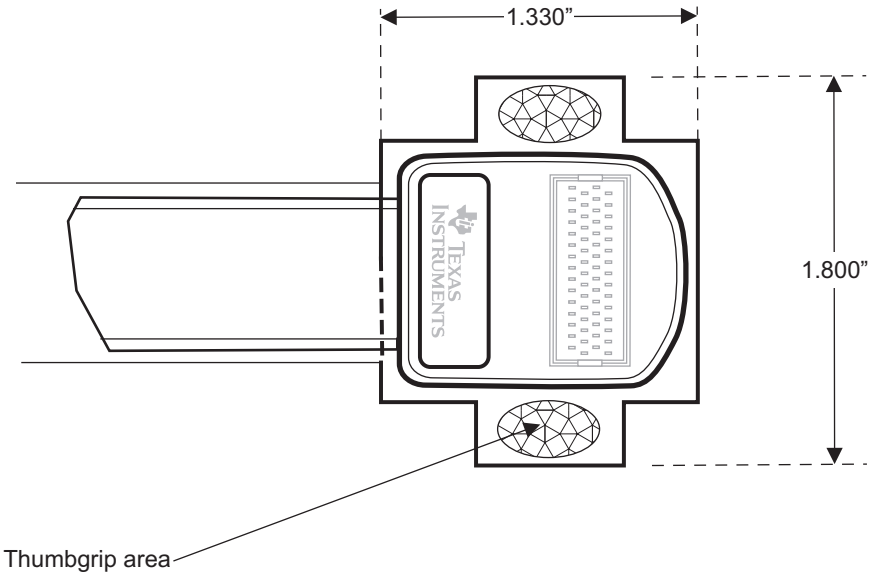



**Figure 15. Clearance Dimensions With Thumb Grips**

Figure 16 illustrates the clearance area beneath the emulation and debug pod header enclosure with the pod removed. Components inside this area must maintain the minimum height as specified by Figure 13.

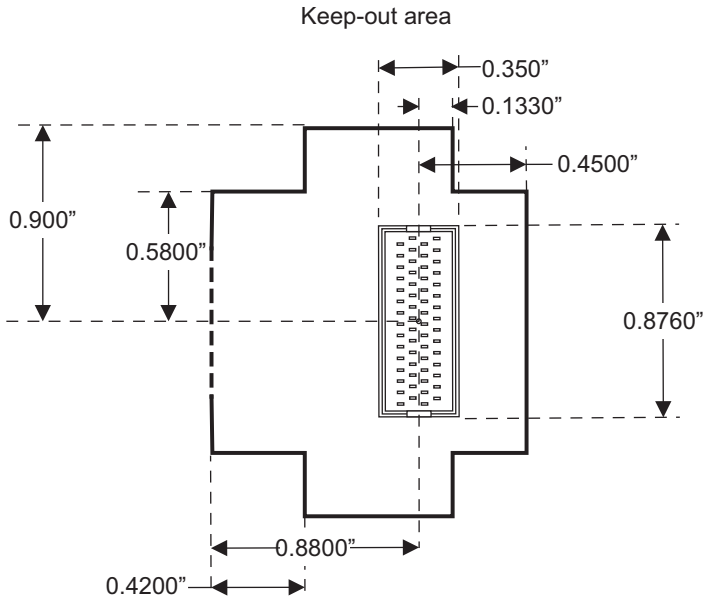



**Figure 16. Emulation and Debug Header and Keep-out Area**

**Table 19. Summary: Layout and Routing – Mechanical Considerations**

| | |
|---|---|
| 1 | The maximum height of components in the keep-out area cannot exceed 0.274”. |
| 2 | The basic area of concern beneath the pod header is 1.8” by 1.3”. |

## 18 Multiple DSP Considerations

There are two supported multiple device configurations: parallel and independent.

Figure 17 illustrates the basic parallel DSP interconnection method. This configuration supports global breakpoints using EMU0 or EMU1 routed in parallel between all processors. It also supports synchronous execution control by daisy-chaining the JTAG signals between processors, and advanced emulation capabilities with EMU[2:n] for a single processor. Given the source current capability of the individual devices, a maximum of 30 devices should never be exceeded. Exceeding this number of devices may severely impact performance. When designing target systems with a large number of DSPs, always minimize the number of vias and trace lengths, and pay special attention to the lengths of individual trace stubs.

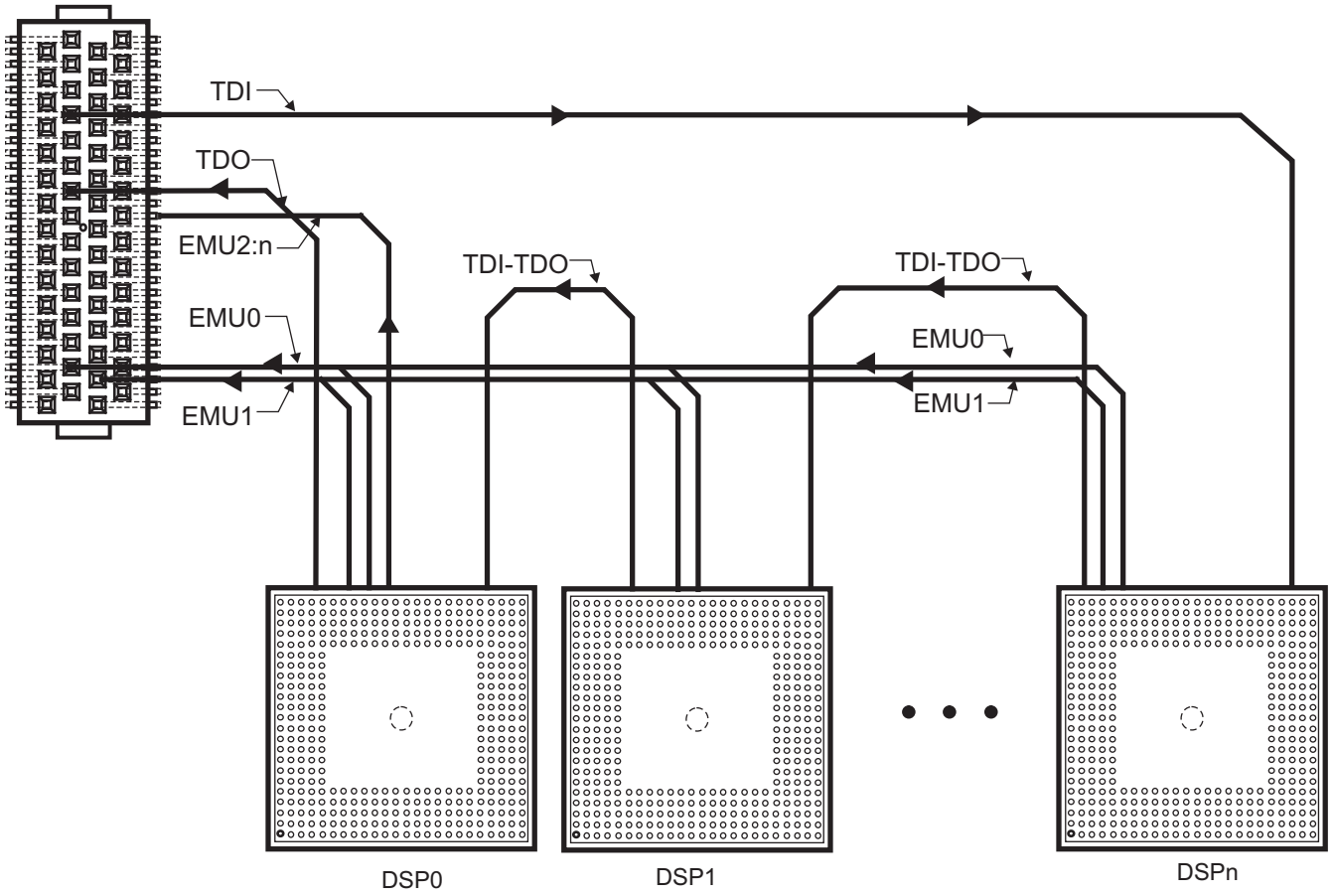



**Figure 17. Multiple DSP - Parallel Configuration**

Figure 18 illustrates the basic independent DSP interconnection method. Under the independent interconnection method, each DSP has its own independent emulation pins assigned per header. An independent configuration as indicated in Figure 18 minimizes the pin count efficiency but maximizes the performance.

In the illustrated independent configuration (Figure 18), each DSP is in its own scan chain. Scanning through each device or global breakpoints are not supported.

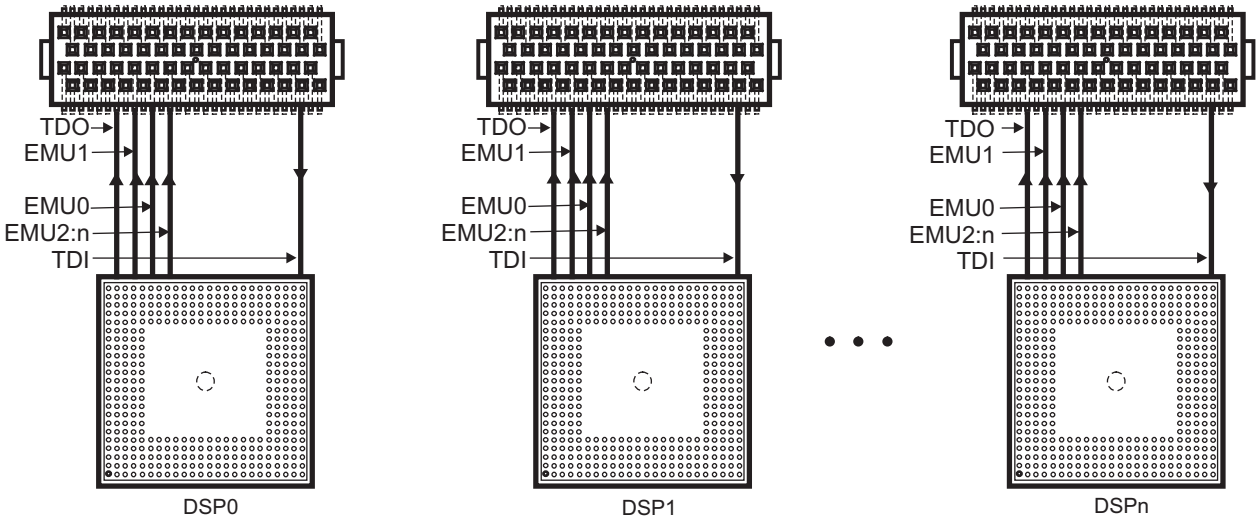



**Figure 18. Independent DSP Connection Method**

# Appendix A Alternate Target Impedance Configurations

## A.1 PCI Interfaces

Most TI DSPs are designed to operate on a 50 Ω character impedance target board. For Texas Instruments' DSP processors incorporating a built-in PCI, Ethernet, or memory interface, the trace impedance should also be 50 Ω. Other DSPs may require a different trace impedance in the range of 60 to 100 Ω.

Always see the DSP application reports or data sheets for detailed impedance requirements and confirm that the target board is designed accordingly.

Appendix G provides information to assist target board designers in obtaining the optimal interconnect impedance by varying widths of the appropriate traces. Various constraints are noted, such as the dielectric constant of the board material, the separation between layers, etc. This chart assumes an Er of 4.1, which is typical for FR-4 material. This appendix also shows how to design a multiple impedance printed circuit board.

All header signals are routed as if they were clock signal lines operating at 200 MHz.

# Appendix B Header Information

## B.1 Header Information

The header selected for Texas Instruments' next generation emulation interface is manufactured by Samtec USA. Table 6 lists the basic specifications for the 60-pin header.

**Table B-1. Next Generation Emulation Header Interface Specifications**

| Item | Value | Comments |
|---|---|---|
| Connector Type | SOLC-115-02-S-Q-P | Standard force |
| Contact Rating | 2.5 Ω | Per contact |
| Contact Material | | BeCu |
| Contact Plating | Au over Ni | Alternate is palladium |
| Contact Resistance | <15 Ω max | |
| Contact Insertion/Removal Cycles | 2,000 | Per manufacturer specifications and standard force |
| Contact Pitch (Row) | 0.050'' | Pitch between mating header contacts |
| Contact Capacitance | 0.4 pF | Average at 1 MHz |
| Propagation Delay | 57.3 ps | 100 ps rise time |
| Crosstalk @ 10 MHz | –51.6 dB | (G / S / S / G) average |
| Crosstalk @ 100 MHz | –32.0 dB | (G / S / S / G) average |
| Crosstalk @ 500 MHz | –16.0 dB | (G / S / S / G) average |
| Contact Inductance | 7.0 nH | Average at 1 MHz |
| Contact Pitch (A–B–C–D) | 0.025" | Pitch between board contacts |
| Contact Insertion Force | 4.0 oz–7.8 oz | SIF (standard insertion force) (nom = 4 oz) |
| Contact Removal Force | 3.8 oz–7.3 oz | SRF (standard removal force) (nom = 5 oz) |
| Connector Insertion Force | 15 lbs–29.25 lbs | SIF (standard insertion force) (nom = 15 lbs) |
| Connector Removal Force | 14.25 lbs–27.37 lbs | SRF (standard removal force) (nom = 18.75 lbs) |
| Connector Impedance @ 10 MHz | 50 Ω | Does not include board modifications to adjust impedance. |
| Connector Impedance @100 MHz | 50.7 Ω | Does not include board modifications to adjust impedance. |
| Connector Impedance @ 500 MHz | 51.3 Ω | Does not include board modifications to adjust impedance. |
| Insertion Depth | 0.066"–0.142" | 0.015" wipe |
| Connector Temperature Range | –65°C to + 125°C | |

Detailed drawings and specifications are available online from the connector manufacturer's web site at http://www.samtec.com.

# Appendix C Buffering – Methods, Techniques and Terminations

## C.1 Buffering – Methods, Techniques and Terminations

Figure C-1 represents the recommended buffering for TCLK; alternate buffers may be used if appropriate. See the manufacturer's data sheets to confirm timing, drive, and voltage characteristics for your specific target.

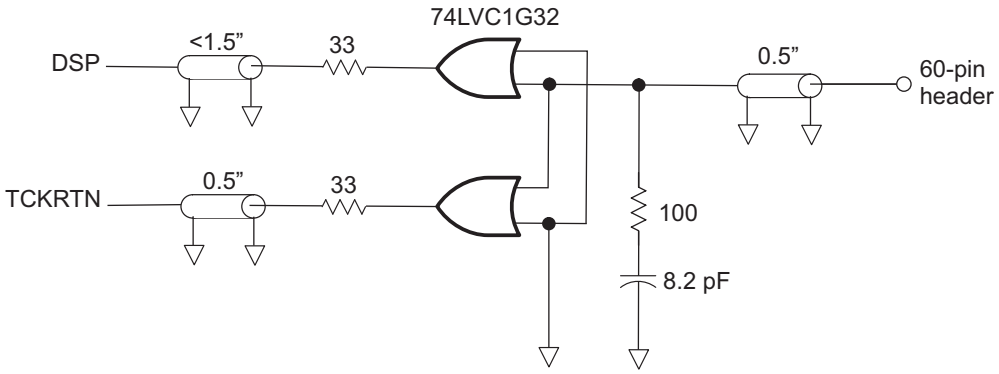



**Figure C-1. Recommended TCLK Buffered Configuration**

Figure C-2 represents the recommended termination for an unbuffered TCLK line. Termination values should be placed in close proximity to the 60-pin emulation header.

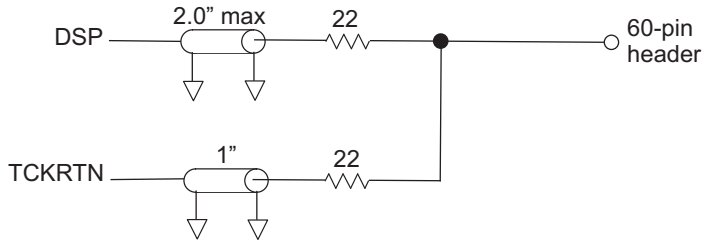



**Figure C-2. Recommended TCLK Unbuffered Configuration**

Figure C-3 illustrates the preferred placement for all emulation (EMU) terminations. Values and placements may vary depending on your DSP and trace lengths. Always model or simulate your design for optimal performance.

See your DSP data sheet for additional recommendations.

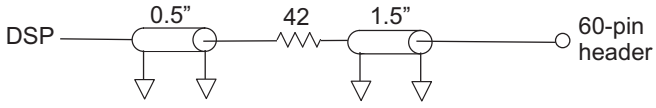



**Figure C-3. Recommended EMU Output Configuration**

Figure C-4 illustrates the preferred placement for EMU0 and EMU1 terminations when multiple headers are used. Values and placements may vary depending on your DSP and trace lengths. The trace lengths listed are maximum values. Always model or simulate your design for optimal performance.

See your DSP data sheet for additional recommendations.

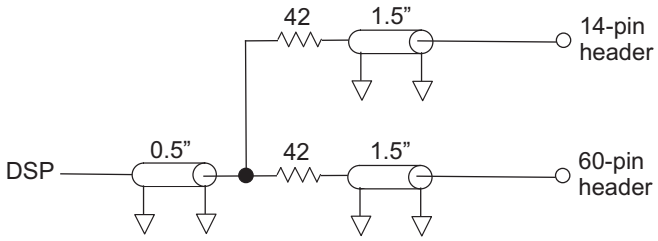



**Figure C-4. Preferred Configuration for EMU0 and EMU1 Terminations**

Figure C-1, Figure C-3, and Figure C-4 all recommend a maximum 0.5” trace distance between the DSP and the termination resistor. This distance for this node under all conditions cannot exceed 1.0”.

# Appendix D 14-Pin and 60-Pin Headers in Parallel

## D.1 14-Pin and 60-Pin Headers in Parallel

If a multi-header configuration is used, the TCLK signal must be buffered. See Figure D-1 for recommended terminations. The use of an FET style switch or multiplexer, such as a 74CBT3125 or 74CBT3257, is mandatory to minimize clock skew between TCLKRTN and the TCLK to the DSP.

The buffer, in this case a 74LVC1G32, is not mandatory, any suitable device can be used. The AC terminations and buffers must be located within 0.5-inch trace length of the header. The 33 Ω series termination should be located as close as possible to the buffer.

Designers should model their circuits including board impedance to determine the proper termination values. It should be noted that Texas Instruments does not recommend the use of the dual header scheme, as it has a potential impact on the overall performance of advanced emulation features.

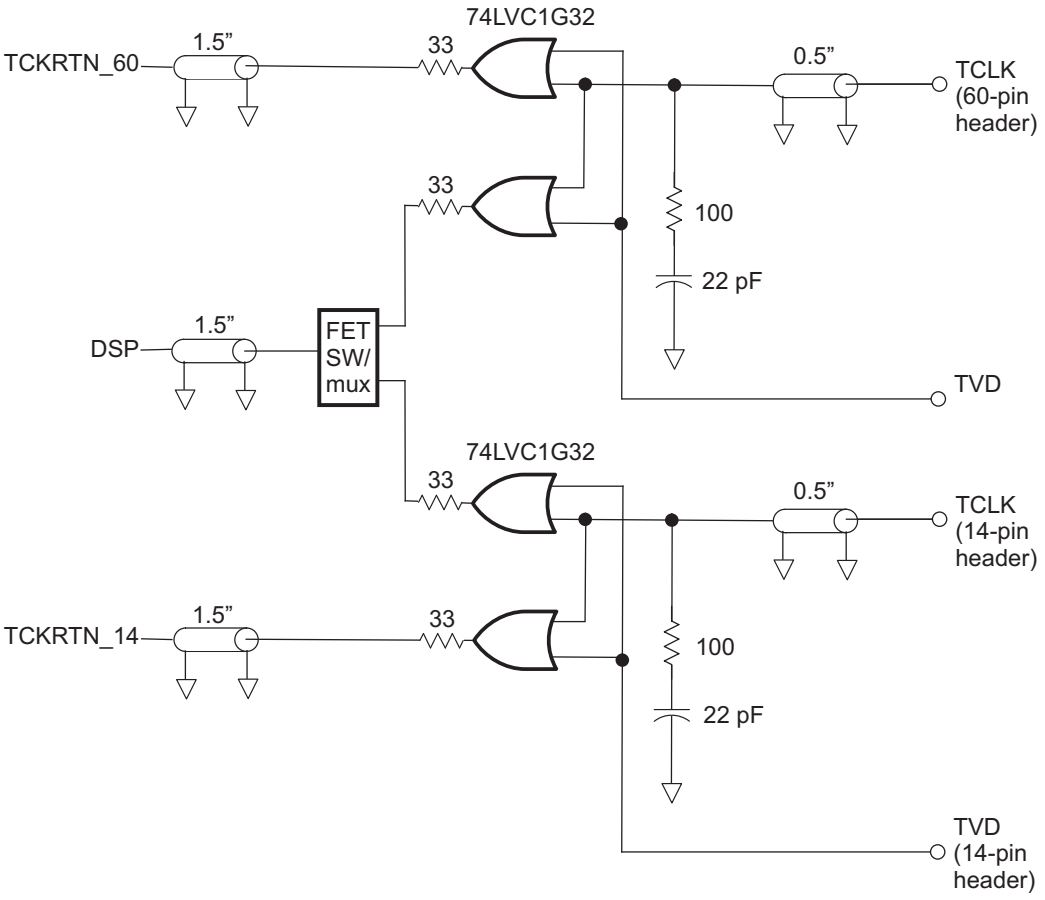



**Figure D-1. TCLK, Multiple Header Configuration**

# Appendix E Layout and Routing Requirements

## *E.1 Layout and Route Deviations [Advanced Emulation]*

To minimize routing deviations, provide a clean electrical environment for advance emulation capabilities. The greater the distance (or skew) between the header and the target processor, the greater the potential for timing errors. A small amount of skew is acceptable and can be accommodated. However, excessive propagation or skew, beyond an allotted amount, will produce bit errors, loss of data or faulty operation. Figure 15 illustrates the recommended header distance from the target processor (2 inches maximum).

A spice model representing the pod interconnect logic is provided in Appendix F. Deviations from the recommended route distances, loading, or skew must be evaluated using this representative model to ensure optimum frequency operation and overall performance.

# Appendix F Spice Model

## F.1 Spice Model

Figure F-1 illustrates the EMU0 spice model for TI's advanced emulation pod assembly and partial target board logic.

Example F-1 is the spice net list for the spice model in Figure F-1. This illustration references a 50 Ω characteristic impedance target PCB. Clock speeds are 200 MHz. Constraints to consider or modify are trace length and board supporting logic. Additional modeling should be done for signal cross talk.

Figure F-2 illustrates an acceptable waveform for Figure F-1 and Example F-1 using TI's new advanced emulation pod and a 50 Ω character-impedance target board.

Example F-2 illustrates the spice net list used to create the spice model for a 75 Ω target board impedance and TI's advanced emulation pod.

Figure F-3 illustrates the waveform for Figure F-1 and Example F-2 using TI's new advanced emulation pod and a 75 Ω character-impedance target board.

Figure F-4 illustrates the EMU2 type signals (see Table F-1) spice model for TI's advanced emulation pod assembly and partial target board logic.

Example F-3 is the spice net list for the spice model in Figure F-4. This illustration references a 50 Ω character-impedance target PCB. Clock speeds are 200 MHz. Constraints to consider or modify are trace length and board supporting logic. Additional modeling should be done for signal cross talk.

Figure F-5 illustrates an acceptable waveform for Figure F-4 and Example F-3 using TI's new advanced emulation pod and a 50 Ω character-impedance target board.

Figure F-6 illustrates the EMU18 type signals (see Table F-1) spice model for TI's advanced emulation pod assembly and partial target board logic.

Example F-4 is the spice net list for the spice model in Figure F-6. This illustration references a 50 Ω character-impedance target PCB. Clock speeds are 200 MHz. Constraints to consider or modify are trace length and board supporting logic. Additional modeling should be done for signal cross talk.

Figure F-7 illustrates an acceptable waveform for Figure F-6 and Example F-4 using TI's new advanced emulation pod and a 50 Ω character-impedance target board.

Figure F-8 illustrates the dual header configuration EMU0 spice model for TI's advanced emulation pod assembly and a partial target board logic. This model is provided to emphasize the advantages of using a single emulation header.

Example F-5 is the spice net list for the spice model in Figure F-8. This illustration references a 50 Ω character-impedance target PCB. Clock speeds are 200 MHz. Constraints to consider or modify are trace length and board supporting logic. Additional modeling should be done for signal cross talk.

Figure F-9 illustrates the waveform for Figure F-8 and Example F-5 using TI's new advanced emulation pod and a 50 Ω character impedance target board in a two-header configuration.

Certain characteristics of the target board may change – the spice net list must be modified and rerun to determine the outcome.

**Table F-1. EMU Pins Modeled as EMU2 or EMU18**

| Model as EMU2 | Model as EMU18 |
|---|---|
| EMU2 | EMU12 |
| EMU3 | EMU14 |
| EMU4 | EMU15 |
| EMU5 | EMU16 |
| EMU6 | EMU17 |
| EMU7 | EMU18 |
| EMU8 | |
| EMU9 | |
| EMU10 | |
| EMU11 | |
| EMU13 | |

Figure F-1 is a representative spice model for TI's XDS560T advanced emulation pod assembly. Clock speeds are 200 MHz. This illustration supports both a 75 Ω and 50 Ω character impedance target PCB. Constraints to consider or modify are trace length and board supporting logic. Additional modeling should be done for signal cross talk.

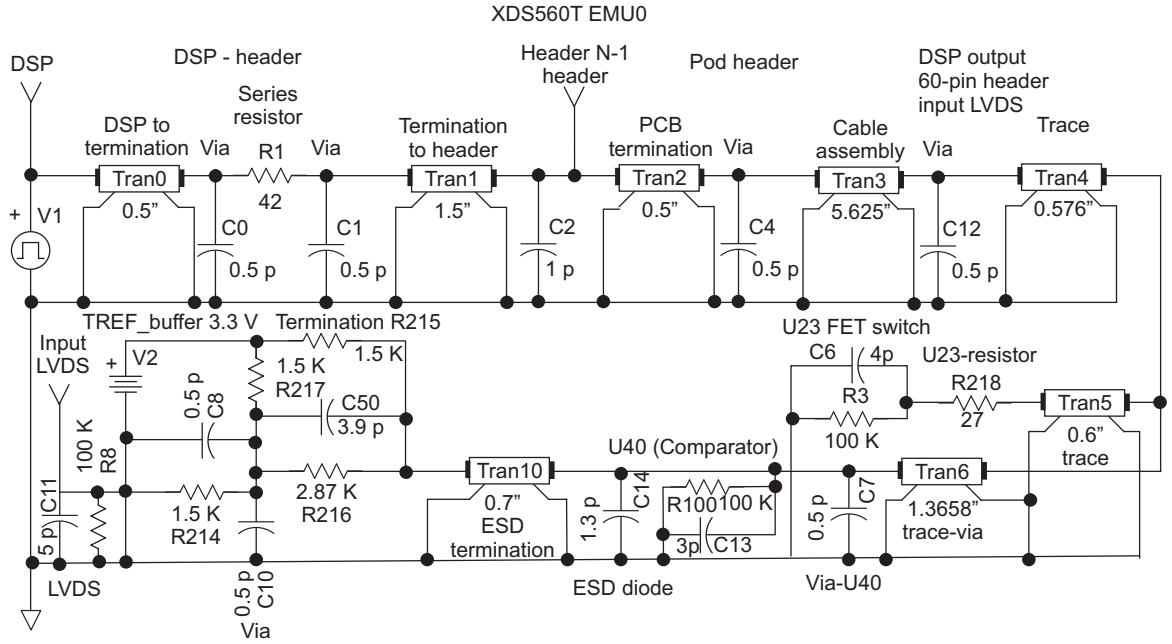



**Figure F-1. EMU0 Simulation Model – (Advanced Emulation Pod, 50 Ω, and 75 Ω Target and Pod Model)**

Example F-1 represents the spice net list used to create the spice model for a 50 Ω target board impedance and Texas Instruments' advanced emulation pod. Certain characteristics of the target board may change - the spice net list must be modified and re-run to determine the potential outcome.

***Example F-1. EMU0 Spice Net List (50 Ω Target And Pod Model)***

```
*** Top Level Netlist ***
C4     0 10 0.5p
C50     6 InputLVDS 3.9p
V1     DSP 0    DC 3.3V AC 0 0 PULSE 0 3.3V 0 800.00p 800.00p 2.20n 4.40n
Tran0     1 0 DSP 0 ZO=50 TD=.088ns F=200Meg NL=0.5
Tran1     Header 0 9 0 ZO=50 TD=.264ns F=200Meg NL=1.5
Tran2     10 0 Header 0 ZO=50 TD=.176ns F=200Meg NL=0.5
Tran3     10 0 13 0 ZO=50 TD=0.990ns F=200Meg NL=5.625
Tran6     2 0 20 0 ZO=50 TD=0.2403808ns F=200Meg NL=1.3658
C2     0 Header 1p
C7     0 2 0.5p
C6     0 4 4p
V2     12 0    DC 3.30 AC 0 0
C9     0 InputLVDS 0.5p
C0     0 1 0.5p
C1     0 9 0.5p
C10     0 InputLVDS 0.5p
C11     0 InputLVDS 5p
C12     13 0 0.5p
Tran5     8 0 20 0 ZO=50 TD=.1056ns F=200Meg NL=0.6
Tran10     6 0 2 0 ZO=50 TD=0.1232ns F=200Meg NL=0.7
C13     0 2 3p
C14     0 2 1.3p
Tran4     13 0 20 0 ZO=50 TD=0.176ns F=200Meg NL=0.576
R1     1 9 42
R216     InputLVDS 6 2.87K
R217     12 InputLVDS 1.5K
R215     12 6 1.5K
R100     2 0 100K
R3     0 4 100K
R218     4 8 27
R214     InputLVDS 0 1.5K
R8     InputLVDS 0 100K

***** Spice models and macro models *****

***** End of spice models and macro models *****

.tran 1n 100n 0.0 1n
.save all
.end
```

The result of your 50 Ω target PCB simulation and modeling should be an acceptable waveform, similar to that illustrated in Figure F-2.

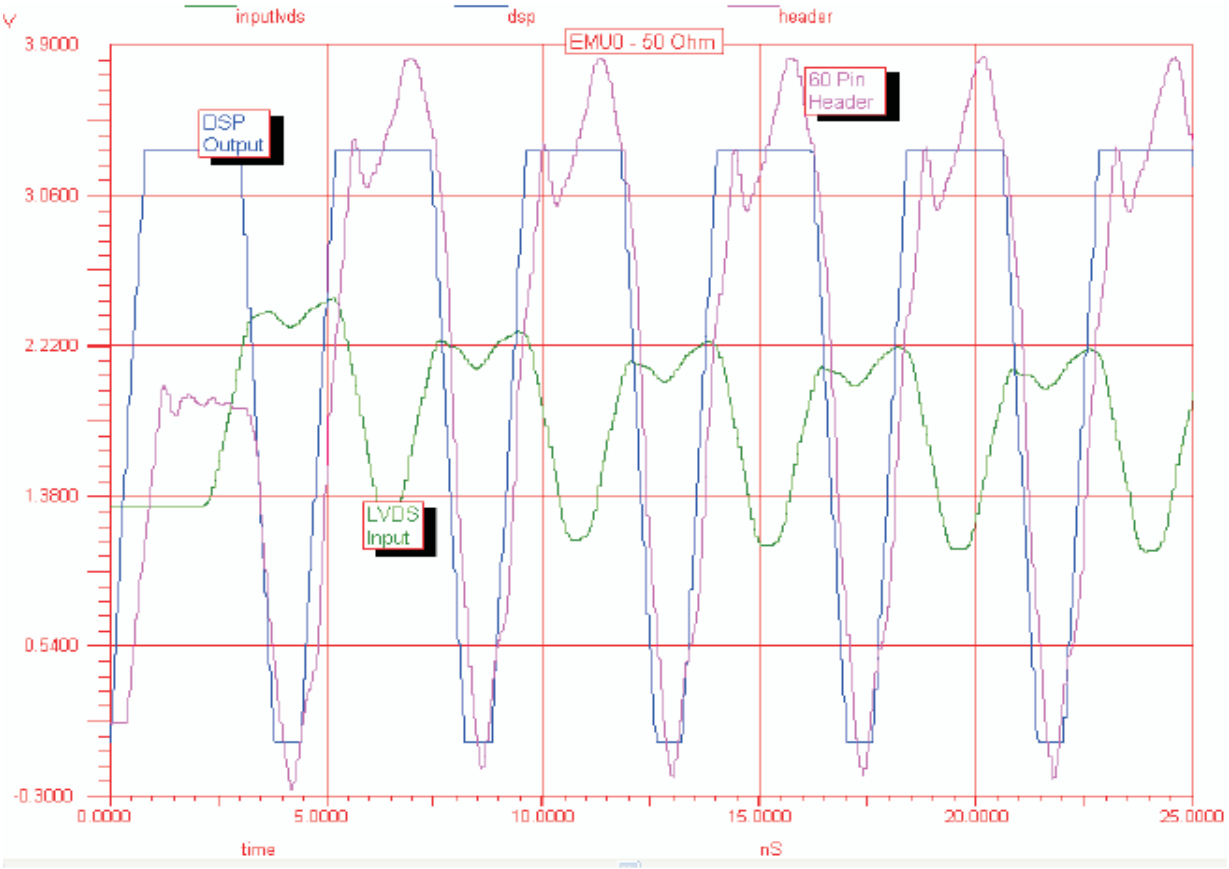



**Figure F-2. EMU0 Acceptable Wave Form (Host Side, Advanced Emulation Pod - 50 Ω)**

Example F-2 represents the spice net list used to create the spice model for a 75 Ω target board impedance and Texas Instruments' advanced emulation pod assembly.

***Example F-2. EMU0 Spice Net List (Host Side, Advanced Emulation Pod - 75 Ω)***

```
*** Top Level Netlist ***
C4     0 10 0.5p
C50     6 InputLVDS 3.9p
V1     DSP 0    DC 3.3V AC 0 0 PULSE 0 3.3V 0 800.00p 800.00p 2.20n 4.40n
Tran0     1 0 DSP 0 ZO=75 TD=.088ns F=200Meg NL=0.5
Tran1     Header 0 9 0 ZO=75 TD=.264ns F=200Meg NL=1.5
Tran2     10 0 Header 0 ZO=75 TD=.176ns F=200Meg NL=0.5
Tran3     10 0 13 0 ZO=75 TD=0.990ns F=200Meg NL=5.625
Tran6     2 0 20 0 ZO=75 TD=0.2403808ns F=200Meg NL=1.3658
C2     0 Header 1p
C7     0 2 0.5p
C6     0 4 4p
V2     12 0    DC 3.30 AC 0 0
C9     0 InputLVDS 0.5p
C0     0 1 0.5p
C1     0 9 0.5p
C10     0 InputLVDS 0.5p
C11     0 InputLVDS 5p
C12     13 0 0.5p
Tran5     8 0 20 0 ZO=75 TD=.1056ns F=200Meg NL=0.6
Tran10     6 0 2 0 ZO=75 TD=0.1232ns F=200Meg NL=0.7
C13     0 2 3p
C14     0 2 1.3p
Tran4     13 0 20 0 ZO=75 TD=0.176ns F=200Meg NL=0.576
R1     1 9 42
R216     InputLVDS 6 2.87K
R217     12 InputLVDS 1.5K
R215     12 6 1.5K
R100     2 0 100K
R3     0 4 100K
R218     4 8 27
R214     InputLVDS 0 1.5K
R8     InputLVDS 0 100K

***** Spice models and macro models *****


***** End of spice models and macro models *****

.tran 1n 100n 0.0 1n
.save all
.end
```

The result of your 75 Ω target PCB simulation and modeling from Example F-2 should be similar to the waveform illustrated in Figure F-3.

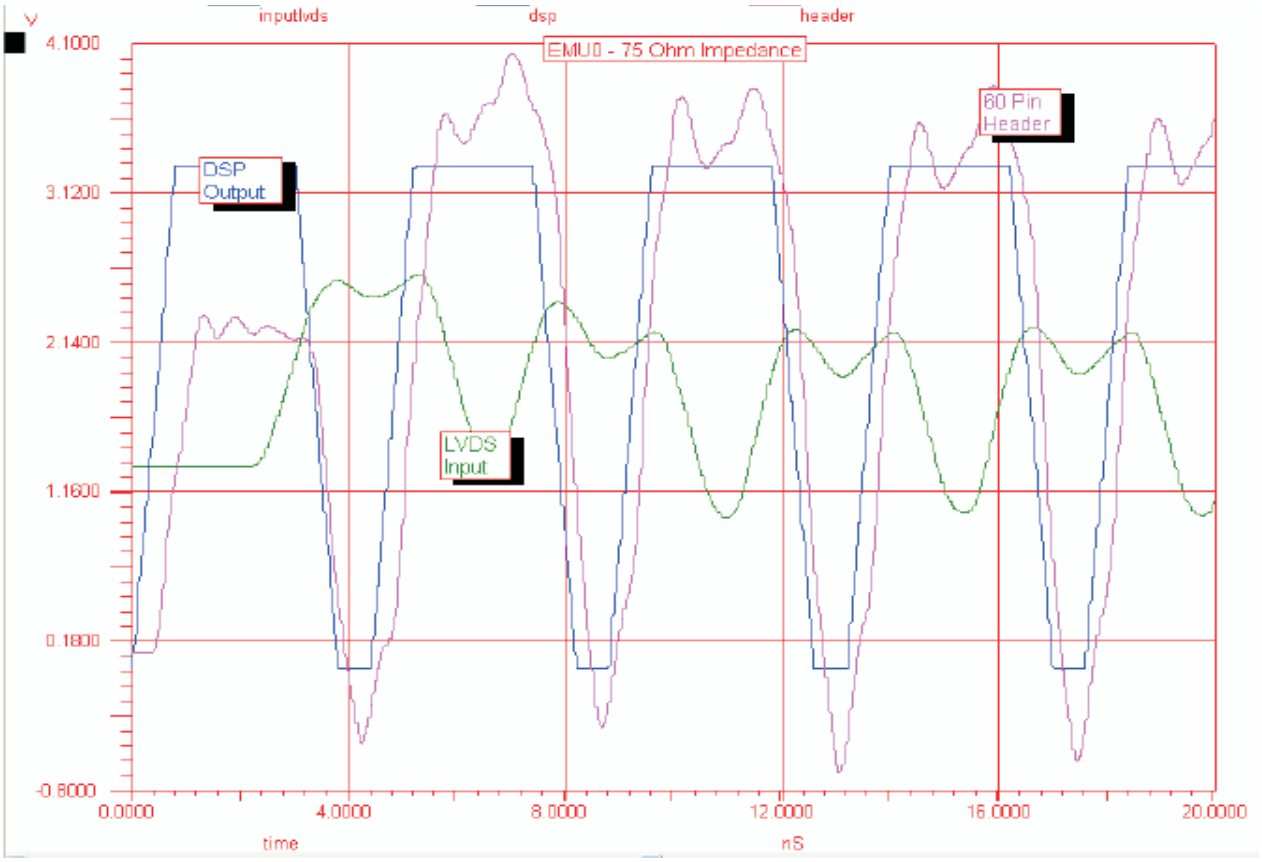



**Figure F-3. EMU0 Wave Form (Host Side, Advanced Emulation – 75 Ω)**

Figure F-4 is a representative spice model for TI's XDS560T advanced emulation pod assembly. Clock speeds are 200 MHz. This illustration supports a 50 Ω character impedance target PCB. Constraints to consider or modify are trace length and board supporting logic. Additional modeling should be done for signal cross talk.

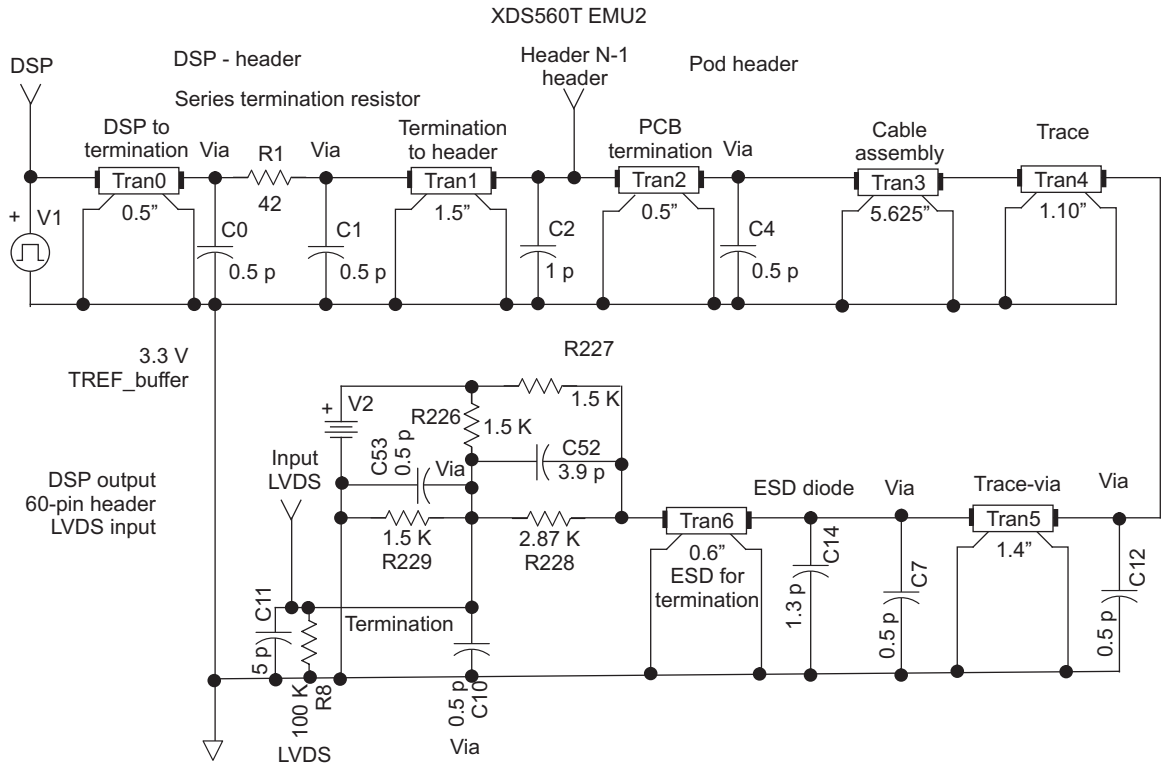



**Figure F-4. EMU2 Type Signals Simulation Model (Advanced Emulation Pod - 50 Ω Target and Pod Model)**

Example F-3 represents the spice net list used to create the spice model in Figure F-4 for a 50 Ω target board impedance and Texas Instruments' advanced emulation pod.

***Example F-3. EMU2 Type Signals Spice Net List (Host Side, Emulation Pod – 50 Ω)***

```
*** Top Level Netlist ***
C4     0 10 0.5p
C52     2 InputLVDS 3.9p
V1     DSP 0    DC 3.3V AC 0 0 PULSE 0 3.3V 0 1.00n 1.00n 1.50n 5.00n
Tran0     1 0 DSP 0 ZO=50 TD=.088ns F=200Meg NL=0.5
Tran1     Header 0 9 0 ZO=50 TD=.264ns F=200Meg NL=1.5
Tran2     10 0 Header 0 ZO=50 TD=.176ns F=200Meg NL=0.5
Tran3     10 0 13 0 ZO=50 TD=0.990ns F=200Meg NL=5.625
Tran5     17 0 3 0 ZO=50 TD=0.2464n F=200Meg NL=1.4
C2     0 Header 1p
C7     0 17 0.5p
V2     7 0    DC 3.30 AC 0 0
C0     0 1 0.5p
C1     0 9 0.5p
C10     0 InputLVDS 0.5p
C11     0 InputLVDS 5p
C12     0 3 0.5p
Tran6     2 0 17 0 ZO=50 TD=0.1056ns F=200Meg NL=0.6
C14     0 17 1.3p
Tran4     13 0 3 0 ZO=50 TD=0.0176ns F=200Meg NL=0.1
R1     1 9 42
R228     InputLVDS 2 2.87K
R226     7 InputLVDS 1.5K
R227     7 2 1.5K
R8     InputLVDS 0 100K
C53     0 InputLVDS 0.5p
R229     InputLVDS 0 1.5K

***** Spice models and macro models *****


***** End of spice models and macro models *****

.tran 10p 100n 0.0 5p
.save all
.end
```

The result of your 50 Ω target PCB simulation and modeling from Example F-3 should be an acceptable waveform, similar to that illustrated in Figure F-5.

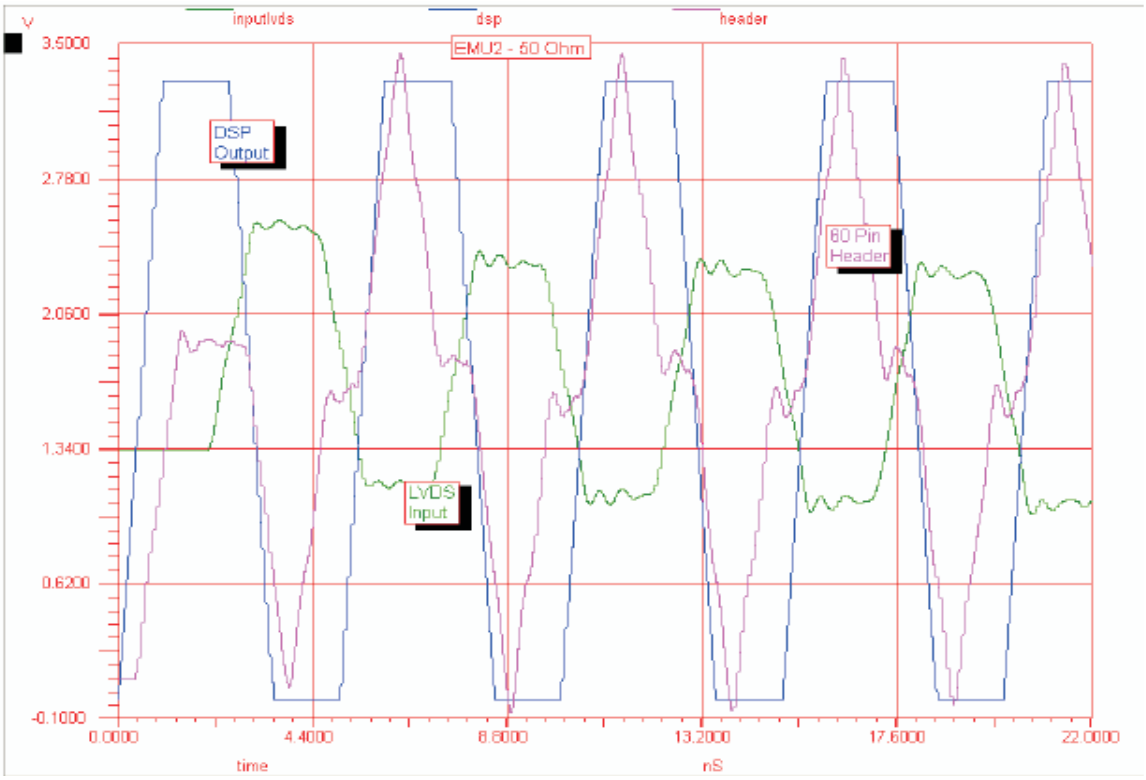



**Figure F-5. EMU2 Type Signals Acceptable Wave Form (Host Side, Emulation Pod – 50 Ω)**

Figure F-6 is a representative spice model for TI's XDS560T advanced emulation pod assembly. Clock speeds are 200 MHz. This illustration supports a 50 Ω character impedance target PCB. Constraints to consider or modify are trace length and board supporting logic. Additional modeling should be done for signal cross talk.

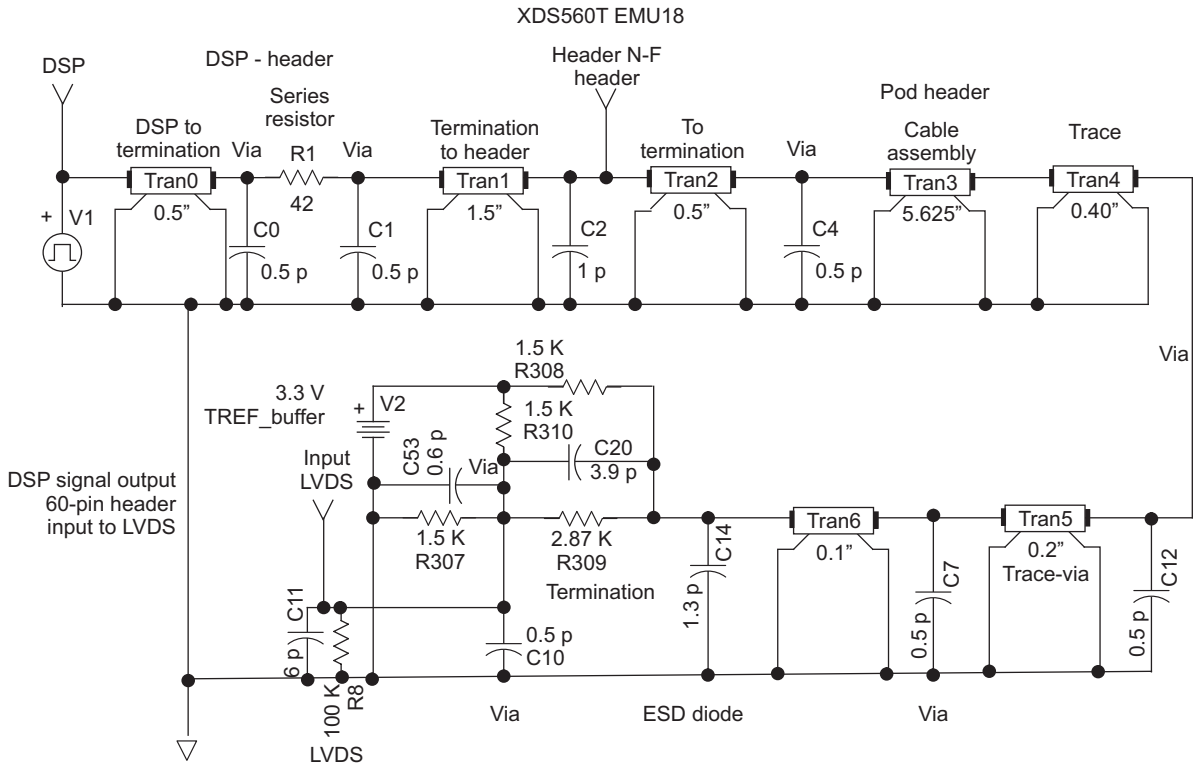



**Figure F-6. EMU18 Type Signals Simulation Model (Advanced Emulation Pod - 50 Ω Target and Pod Model)**

Example F-4 represents the spice net list used to create the spice model in Figure F-6 for a 50 Ω target board impedance and Texas Instruments' advanced emulation pod.

***Example F-4. EMU18 Type Signals Spice Net List (Host Side, Emulation Pod – 50 Ω)***

```
*** Top Level Netlist ***
C4     0 10 0.5p
C70     6 InputLVDS 3.9p
V1     DSP 0    DC 3.3V AC 0 0 PULSE 0 3.3V 0 1.00n 1.00n 1.50n 5.00n
Tran0     1 0 DSP 0 ZO=50 TD=.088ns F=200Meg NL=0.5
Tran1     Header 0 9 0 ZO=50 TD=.264ns F=200Meg NL=1.5
Tran2     10 0 Header 0 ZO=50 TD=.176ns F=200Meg NL=0.5
Tran3     10 0 13 0 ZO=50 TD=0.990ns F=200Meg NL=5.625
Tran5     18 0 8 0 ZO=50 TD=0.0352n F=200Meg NL=0.2"
C2     0 Header 1p
C7     0 18 0.5p
V2     7 0    DC 3.30 AC 0 0
C0     0 1 0.5p
C1     0 9 0.5p
C10     0 InputLVDS 0.5p
C11     0 InputLVDS 5p
C12     0 8 0.5p
Tran6     6 0 18 0 ZO=50 TD=0.0176ns F=200Meg NL=0.1
C14     0 6 1.3p
Tran4     13 0 8 0 ZO=50 TD=0.0704ns F=200Meg NL=0.4
R1     1 9 42
R309     InputLVDS 6 2.87K
R310     7 InputLVDS 1.5K
R308     7 6 1.5K
R8     InputLVDS 0 100K
C53     0 InputLVDS 0.5p
R307     InputLVDS 0 1.5K

***** Spice models and macro models *****


***** End of spice models and macro models *****

.tran 2n 100n 0.0 2n
.save all
.end
```

The result of your 50 Ω target PCB simulation and modeling from Figure F-6 should be an acceptable waveform, similar to that illustrated in Figure F-7.

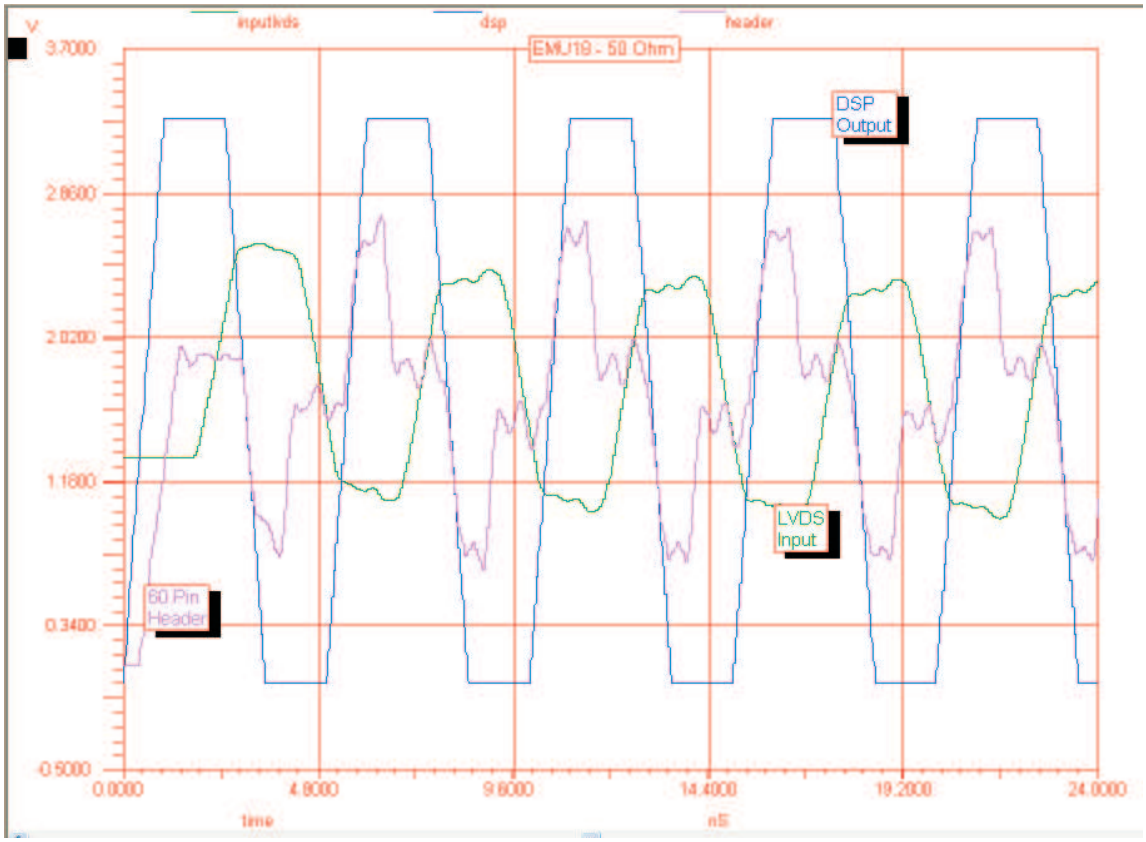



**Figure F-7. EMU18 Type Signals – Acceptable Wave Form (Host Side, Emulation Pod – 50 Ω)**

Figure F-8 is a spice model for a dual-header configuration using TI's XDS560T advanced emulation pod assembly. Clock speeds are 200 MHz. This illustration supports a 50 Ω character impedance target PCB. Dual-header configurations are not recommended and require a variety of constraints to be modeled (trace length and supporting logic). Additional modeling should be done for signal cross talk.

It is strongly recommended that only TI's emulation header be used.

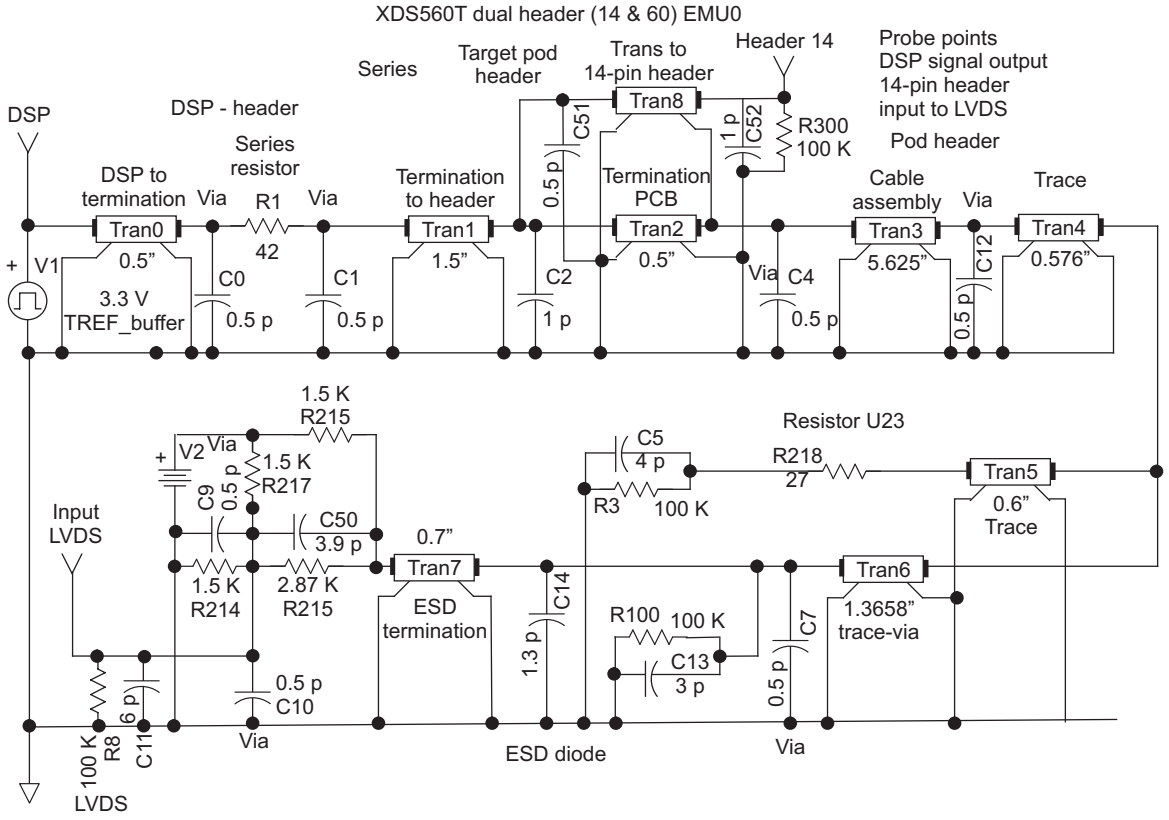



**Figure F-8. EMU0 Dual-Header Simulation Model (Advanced Emulation Pod - 50 Ω Target and Pod Model)**

Example F-5 represents the spice net list used to create the spice model in Figure F-8 for a 50 Ω dual-header target board impedance and Texas Instruments' advanced emulation pod.

***Example F-5. EMU0 Dual-Header Spice Net List (Host Side, Emulation Pod – 50 Ω)***

```
*** Top Level Netlist ***
C4     0 10 0.5p
C50     12 InputLVDS 3.9p
V1     DSP 0    DC 3.3V AC 0 0 PULSE 0 3.3V 0 800.00p 800.00p 2.20n 4.40n
Tran0     1 0 DSP 0 ZO=50 TD=.088ns F=200Meg NL=0.5
Tran1     5 0 9 0 ZO=50 TD=.264ns F=200Meg NL=1.5
Tran2     10 0 5 0 ZO=50 TD=.176ns F=200Meg NL=0.5
Tran3     10 0 13 0 ZO=50 TD=0.990ns F=200Meg NL=5.625
Tran6     2 0 18 0 ZO=50 TD=0.2403808ns F=200Meg NL=1.3658
C2     0 5 1p
C7     2 0 0.5p
C6     8 0 4p
V2     16 0    DC 3.30 AC 0 0
C9     0 InputLVDS 0.5p
C0     0 1 0.5p
C1     0 9 0.5p
C10     0 InputLVDS 0.5p
C11     0 InputLVDS 5p
C12     13 0 0.5p
Tran5     14 0 18 0 ZO=50 TD=.1056ns F=200Meg NL=0.6
Tran7     12 0 2 0 ZO=50 TD=0.1232ns F=200Meg NL=0.7
C13     0 2 3p
C14     0 2 1.3p
Tran4     13 0 18 0 ZO=50 TD=0.176ns F=200Meg NL=0.576
R1     1 9 42
R216     InputLVDS 12 2.87K
R217     16 InputLVDS 1.5K
R215     16 12 1.5K
R100     2 0 100K
R3     8 0 100K
R218     8 14 27
R214     InputLVDS 0 1.5K
R8     InputLVDS 0 100K
Tran8     5 0 Header14 0 ZO=50 TD=0.2816ns F=200Meg NL=1.6
C51     0 5 0.5p
C52     0 Header14 1p
R300     Header14 0 100K

***** Spice models and macro models *****


***** End of spice models and macro models *****

.tran 1n 100n 0.0 1n
.save all
.end
```

The result of your 50 Ω dual-header target PCB simulation and modeling from Figure F-8 should be an acceptable waveform, similar to that illustrated in Figure F-9.

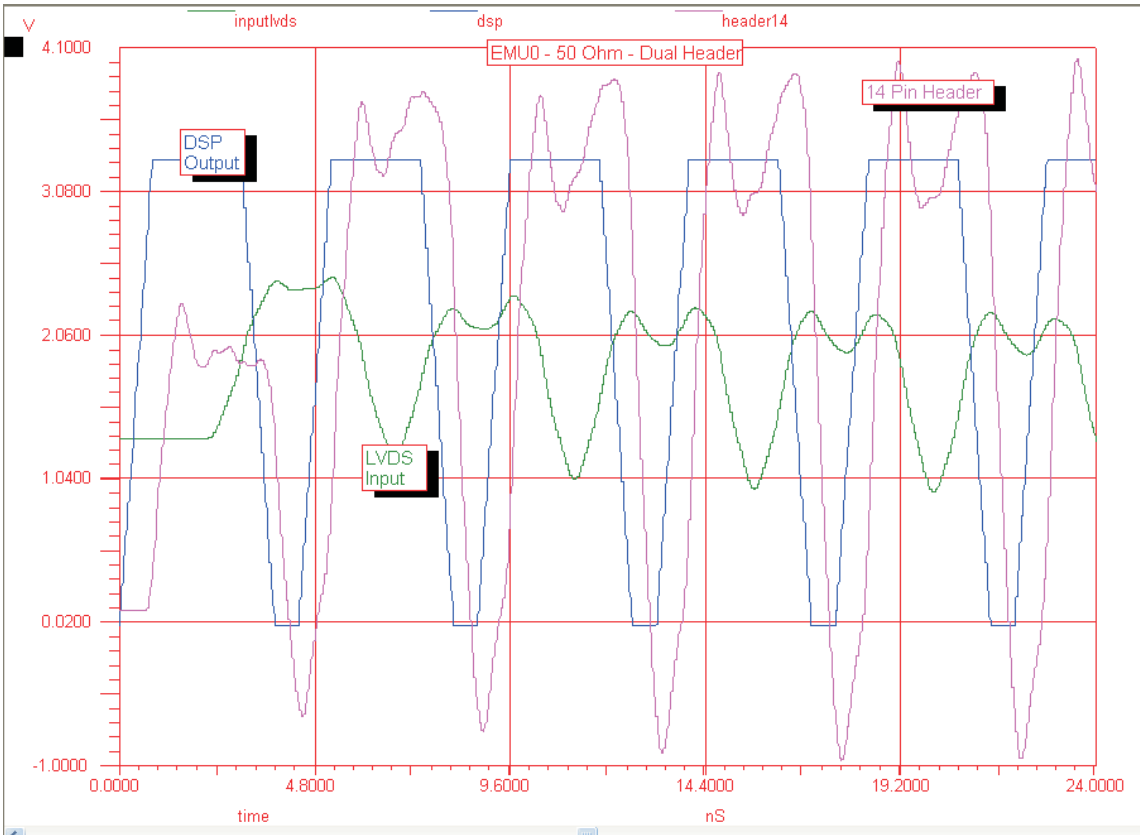



**Figure F-9. EMU0 Dual-Header – Wave Form (Host Side, Emulation Pod – 50 Ω)**

# Appendix G Variable Board Impedance

## G.1 Variable Board Impedance

Figure G-1 illustrates the ability to alter individual printed circuit board impedances by varying the dielectric thickness and spacing for specific signal layers to reference planes.

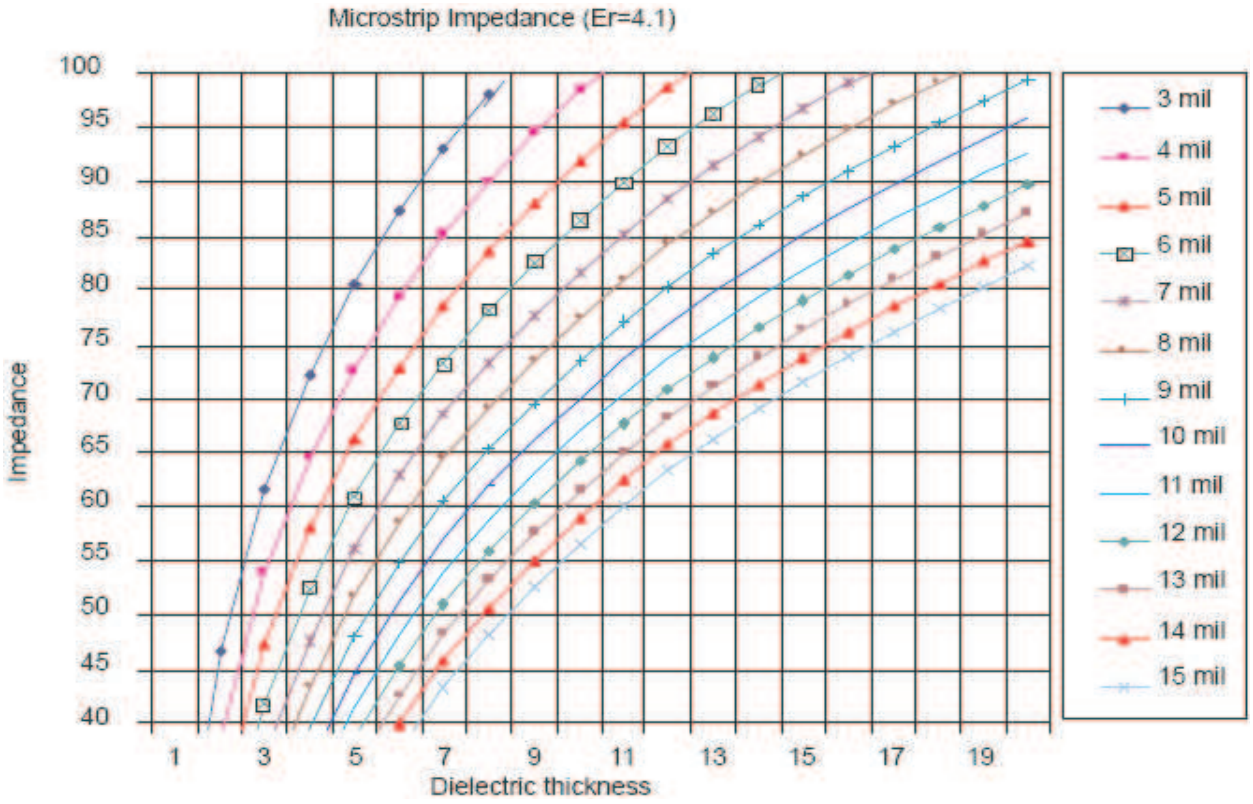
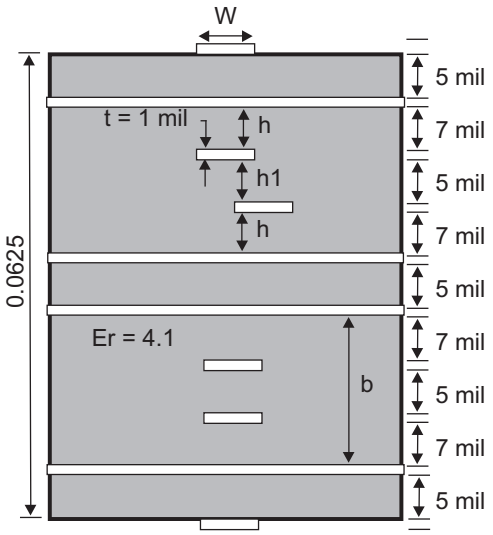



**Figure G-1. Various PCB Impedance Calculations**




A typical layer stackup is shown to the left, all copper layers are assumed to be 1 mil thick. Total board thickness is 0.063.

If h=7 mils, and h1 = 5 mils, a 7.5-mil wide trace has a 50-Ω impedance and a 3.5-mil wide trace has a 71-Ω impedance.

Example of 10-layer PCB construction

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

| **Products** | | **Applications** | |
|---|---|---|---|
| Amplifiers | amplifier.ti.com | Audio | www.ti.com/audio |
| Data Converters | dataconverter.ti.com | Automotive | www.ti.com/automotive |
| DSP | dsp.ti.com | Broadband | www.ti.com/broadband |
| Interface | interface.ti.com | Digital Control | www.ti.com/digitalcontrol |
| Logic | logic.ti.com | Military | www.ti.com/military |
| Power Mgmt | power.ti.com | Optical Networking | www.ti.com/opticalnetwork |
| Microcontrollers | microcontroller.ti.com | Security | www.ti.com/security |
| Low Power Wireless | www.ti.com/lpw | Telephony | www.ti.com/telephony |
| | | Video & Imaging | www.ti.com/video |
| | | Wireless | www.ti.com/wireless |

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265