UM10998

NXP USB Type-C 1 – 3 reference design

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Document information

Info	Content
Keywords	USB Type-C, USB Power Delivery, Adapter, 1 – 3, Schematic, USB PD Kernel
Abstract	This application note introduces NXP's USB Type-C 1 – 3 Multiport Adapter. The reference design and features will be explained in a hardware and software level in order to educate customers on what to expect when building and evaluating NXP's USB Type-C 1 – 3 Multiport Adapter.

Revision history

Rev	Date	Description
1	20160624	Initial version

Contact information

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1. Introduction

Improving upon the previous Type-A and Type-B USB connectors, the Type-C connector is far more user-friendly, offering reversible plug orientation, cable direction and the ability to transfer power and data simultaneously as well as support different protocols, such as DisplayPort, Mobile High-Definition Link, and Thunderbolt for alternate modes. The bi-directional power flow support allows a device to either source or sink power. In addition, Type-C connectors offer scalable power solutions, ranging from 5 V at 0.5 A for handheld devices up to 20 V at 5.0 A for rapid charging and power delivery.

The total USB Type-C ecosystem from NXP includes microcontrollers, high speed switches, USB3 redrivers, ESD protection and filtering devices, USB PD PHY, CC logic controllers, authentication, load switches, AC/DC power solutions, MOSFETs and more.

This application note acts as a user manual to help vendors build and evaluate NXP's USB Type-C 1 – 3 Multiport Adapter based on the reference design by providing steps on setting up the board and explaining the functional specification, including providing a binary of NXP's USB PD kernel. The schematic for the board is also provided to act as a reference for vendors interested in prototyping their own boards. This solution would expand a host's USB Type-C port into three different ports in order to support the following:

- USB Type-A receptacle to allow for the use of legacy USB 2.0 and 3.0 devices.
- VGA output capable of up to 1080p HD.
- USB Power Delivery enabled Type-C port with charge-through functionality, capable of sinking up and passing this power through to the USB Type-C port facing the host. This charge-through functionality supports 5 V at 1.5 A or up to 20 V at 3 A.

2. Package contents

This application note contains two additional folders: one folder contains the reference schematic while the other folder contains the software binary and firmware update tool.

Fig 1 shows the extracted contents of the package.

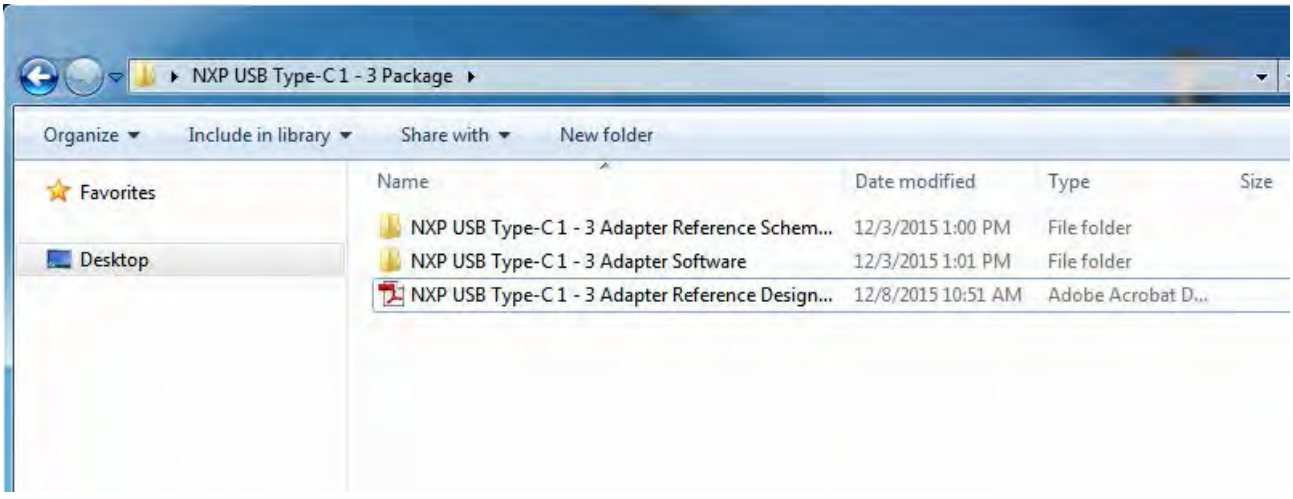

Fig 1. Extracted package contents

3. Getting started

The NXP USB Type-C 1 – 3 reference design is meant to allow customers to quickly build and evaluate NXP's USB Type-C Multiport adapter. This adapter transforms a host's USB Type-C port into a VGA connector, USB Type-A receptacle, and another USB Type-C port that is USB Power Delivery enabled.

Fig 2 shows a picture of the NXP USB Type-C 1 – 3 multiport dongle.

The reference design is meant for a pigtail with a Type-C plug that plugs into a Type-C receptacle on the host side.

Fig 2. NXP USB Type-C to VGA 1 – 3 dongle

3.1 Programming NXP's USB Type-C 1 – 3 multiport adapter

To program the binary onto the adapter, hold down the SW1 switch while plugging the adapter into a Windows machine to receive power. This will put the MCU into a USB In-System Programming (ISP) mode. In USB ISP mode, the MCU will enumerate itself as a Mass Storage Class device. See Fig 3.

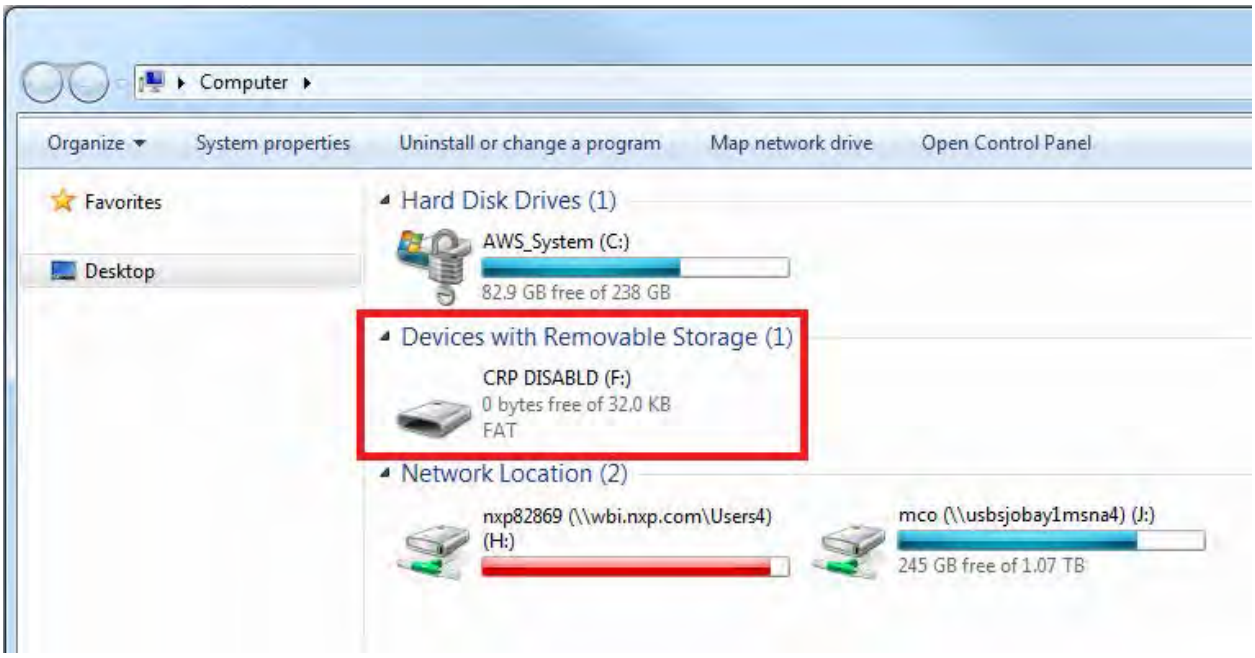

Fig 3. LPC11U35 USB ISP mode

To program the LCP11U35, delete the current firmware.bin in the device and drag and drop the given binary into the device like you would with a flash drive. Power cycling the adapter should now execute the USB PD kernel, enabling all the functions on the NXP USB Type-C 1 – 3 Multiport Adapter.

3.1.1 NXP USB Type-C 1 – 3 multiport adapter features

The software included in this application note is comprised of a fully featured USB PD kernel compiled into a binary. The PD kernel has been configured to have the following characteristics:

- Port 0 (host facing port)
  - DRP receptacle type.
  - Provider Source PDO not supported until charger plug-in. Source capabilities will then be overwritten to be 5 V at 1.5 A and the highest voltage PDO from the charger.
  - Consumer Sink PDO configured to 5 V at 3 A.
  - Automatically negotiate DP alternate mode with 2 DP lanes with multifunction bit set.
  - Supports USB 2.0 DFU device class using NXP VID:PID of 0x1FC9:0x5002 and USB Billboard string descriptors.
- Port 1 (charger facing port)
  - UFP sink receptacle type.
  - Consumer Sink PDO configured to 5 V at 3 A and will automatically request the highest voltage PDO from the charger.

To make the USB Power Delivery features more engaging, the FW will also blink an LED at a frequency relative to the voltage level on VBUS. As per the USB Power Delivery specification, the voltage on VBUS can be negotiated to be in the range of 5 V to 20 V. The following is the frequency that is programed into the binary given with this application note:

- 5 V is a 1 Hz blink.
- 20 V is a 10 Hz blink.
- Any voltage in between 5 V and 20 V is a 5 Hz blink.

For customized design requirements related to the software, please contact NXP directly either through the following support email address or other means:

USBTypeC@nxp.com

3.1.2 Firmware updates

In addition to a fully featured USB PD kernel, the binary was extended with a secondary bootloader (SBL), allowing for field updates for the application code via DFU device class. This SBL adds the following features to the software:

- FW updates via DFU device class, allowing for customer facing field updates.
- FW updates can be encrypted by the 128-bit XXTEA encryption algorithm and Code Read Protection, adding security.
- SBL always calculates and validates CRC checksum of application code, checking the integrity of the FW.

Since the MacBook is the most popular USB Type-C host available, attached with this application note is an OS X version of the DFU update tool.

For more information on the SBL and the related tools on different platforms, see AN11732 on http://www.nxp.com.

3.1.2.1 DFU updates on OS X

To perform field updates, the DFU device class is used along with the open source dfu-util tool. In order for the dfu-util tool to work with our DFU SBL, an NXP patch was applied. This dfu-util is dependent on libusb so this library must be installed on the MacBook first. Out of the box, OS X is very sandboxed, so you must install a command line command called “brew” to enable most of the typical Linux commands. To do so, open terminal on the MacBook and copy and paste the following command. Follow the installation directions afterwards:

```
ruby -e "$(curl -fsSL https://raw.githubusercontent.com/Homebrew/install/master/install)"
```

Next, install libusb with the following command:

```
brew install libusb
```

With libusb installed, the dfu-util tool can now be used. In the software folder is the dfu-util with the nxp patch and a shell script. The shell script can be double clicked to execute in order to easily perform the FW update. The shell script automatically searches for any .dfu files in the working directory and will use the dfu-util tool to communicate with the MCU and perform a DFU update. Only one .dfu can be present in the same directory as the shell script and will not execute if it finds more than one.

3.1.2.2 DFU update versus USB ISP mode

This application note presents two different ways to update the MCU FW. The difference between these two methods is that a DFU update requires a binary with a valid CRC

checksum and a DFU SBL inside the target MCU. This means that USB ISP mode should only be used on binaries that contain the application code and DFU SBL in order to enable DFU updates in the future. These binaries end with a .bin extension and have a size of 64 kB. Binaries meant for DFU updates already have the CRC checksum inserted and do not have the DFU SBL. These binaries end with a .dfu extension and have a size of 56 kB.

3.1.3 Board behavior

The binary provided with this application note is a two port implementation of NXP's USB PD kernel.

Fig 4 shows a high level state machine that illustrates the state transitions when there is a Type-C attach or detach on either Type-C ports.

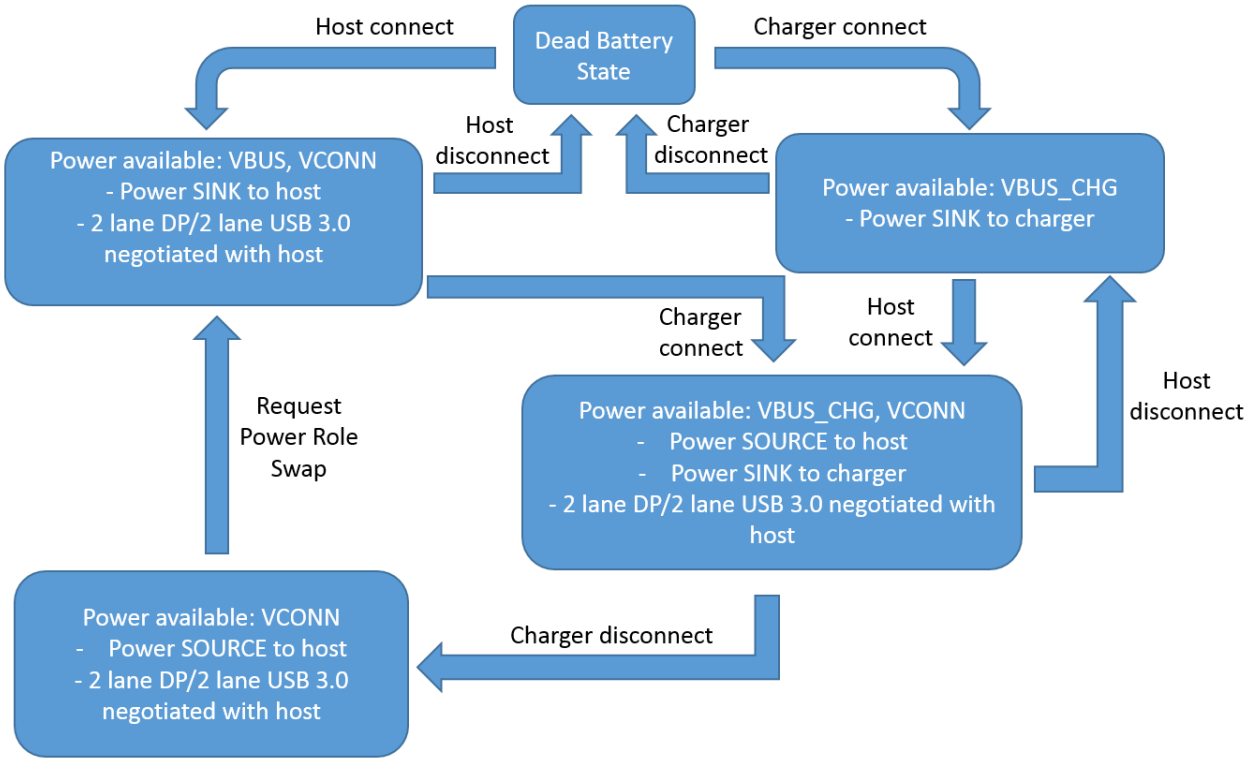

Fig 4. Software behavior state machine

3.1.3.1 Functional caveats

While each of the three ports on the NXP USB Type-C 1 – 3 Multiport Adapter are fully functional at all points in time, there are two caveats to be considered with this design:

1. As shown in Fig 4, when the adapter is connected to both a host and a charger, the board will source voltage to the host through VBUS, leaving only two available power options: VBUS from the charger and VCONN from the host. If the charger is unplugged while the adapter is still connected to the host, VCONN will be the only power source available for a brief moment in time. Depending on power consumed by USB 3.0 device, VCONN may not be able to provide enough current for the board to maintain power and cause the board to power cycle. There currently is no provision in the USB PD 2.0 specification for this specific scenario. In order to

minimize the occurrence of this, the USB PD kernel provided will disable the USB Type-A device when the charger disconnect is detected and turn it back on once the adapter successfully negotiates a power role swap and becomes a sink. This also means that since the board relies on VCONN power, it is assumed that the host supplies VCONN at 5 V.

2. As with all emerging technology with an ever-changing specification, the interpretation of the specification can vary from vendor to vendor and cause interoperability problems. The NXP USB Type-C 1 – 3 Multiport Adapter was tested and verified working with Apple's 2015 MacBook with OS X El Capitan Version 10.11.1. NXP cannot guarantee compatibility with any current or future USB Type-C products released by vendors nor continued compatibility when vendors update the software on their products.
3. Since we use a buck to regulate the charger VBUS down to 5 V, using a 5 V only charger in the charge-through port will result in the output of the buck to be less than 5 V. This output voltage may be under the minimum VBUS voltage outlined in the USB Type-C specification, which may result in compliance issues and interoperability issues when the adapter is a source. This means that this design is only compatible with chargers that support a voltage greater than 5 V.
4. The diodes used in this design have a forward voltage that causes a noticeable voltage drop in certain power paths. These drops affect the adapter's ability to source VSafe5V on the Type-C VBUS during a positive voltage transition as well as on the USB Type-A's VBUS. This causes compliance issues and may even cause certain USB Type-A devices to not work properly, particularly devices that draw large amounts of power.

4. Design flow

NXP provides the reference design schematic as a starting point for customers interested in manufacturing their own NXP USB Type-C 1 – 3 Multiport Adapters. To ensure correct operation, it is strongly advised to read through the rest of this chapter to understand the interoperability between each of the ICs involved. The important parts of the schematic are described at a high level, the power distribution methodology is discussed.

4.1 Schematic overview

The NXP USB Type-C 1 – 3 Multiport Adapter expands one USB Type-C connector into three connectors: a USB Type-A receptacle compatible with USB 2.0 and USB 3.0 devices, a VGA connector, and a USB PD enabled USB Type-C port capable of sinking voltage and passing high speed data. Each of these connectors operates independent of each other and can be seen as its own subsystem. The MCU acts as the USB PD policy manager, which manages the operation of each of the three ports. The role of each major component involved with this design is explained.

4.1.1 PTN5100D

The NXP PTN5100D is the USB Type-C PHY, including all the CC logic needed to communicate with the PHY on the other side of the USB Type-C connector. The PTN5100D is controlled by the MCU via SPI. The PTN5100D also has a V_MCUPWR pin which is capable of outputting 3.3 V at up to 30 mA if either the VBUS or VDD pins are powered. For adapters that consume less than 30 mA, the V_MCUPWR pin can be used as the primary 3.3 V power rail.

For more information, see the PTN5100D datasheet on http://www.nxp.com.

4.1.2 LPC11U35FHI33/CP3337

The NXP LPC11U35FHI33/CP3337 is a small, low cost Cortex-M0 microcontroller, acting as the USB PD policy manager. It is responsible for controlling the PTN5100D on each of the Type-C ports in order to negotiate the correct power contracts in order to sink and source voltage to the host depending on if a charger is connected, as well as negotiate DisplayPort alternate mode. The MCU also controls the analog switch for the DisplayPort AUX signal and a current limiter for the USB Type-A VBUS.

The LPC11U35FHI33/CP3337 also has USB 2.0 functionality, which is used to fulfill the USB 2.0 Billboard device class required by the DisplayPort alternate mode specification. In addition, the MCU's USB 2.0 functionality can be used to enable DFU field updates for the MCU firmware with NXP's DFU secondary bootloader.

For more information, see the LPC11U3x datasheet on http://www.nxp.com.

4.1.3 PTN3356

The NXP PTN3356 is a DP to VGA converter. Due to the current consumption of this IC, the PTN5100D V_MCUPWR pin will not be able to power the 3.3 V power rail that the PTN3356 is connected to.

In order to meet DP_ALT_mode compliance specification, DP main links cannot have termination till DP_ALT_mode is established.

For more information, see the PTN3356 datasheet on http://www.nxp.com.

4.1.4 NX3L2TG66

The NXP NX3L2TG66 are analog switches used to keep the DP AUX lines tri-stated until DP alternate mode has been negotiated, as required by the DP alternate mode specification. The switch is controlled by the XSDN signal on the MCU.

New FW version F2 is required to support this function. For more information, see the NX3L2TG66 datasheet on http://www.nxp.com.

4.1.5 ESD/TVS protection diodes

To protect the adapter from the outside world, it is required to place an ESD or TVS protection diode on all of the exposed USB Type-C pins. Table 1 indicates the part number recommended for the various USB Type-C pins.

For more information, see the datasheet for the specific part on http://www.nxp.com.

Table 1. ESD/TVS protection diodes

USB Type-C Pin	ESD/TVS part number
VBUS	PTVS24VS1UR
CC1/CC2	PESD5V0S1UL
Data lines	PESD5V0H1BSF

Failure to add protection diodes will leave the adapter design susceptible to permanent damage.

4.1.6 NX20P5090UK and NX5P3090UK

The NXP NX20P5090UK and NX5P3090UK are load switches designed for USB PD domain isolation applications to offer essential protection and enhance reliability. These load switches have protection circuitry such as over-voltage lockout and over-current

protection in order to safely operate with the high amounts of current and voltage that USB PD allows.

For more information, see the datasheet for the specific part on http://www.nxp.com.

4.1.7 GL3523

The Genesys Logic GL3523 is a USB 3.1 Gen 1 Hub controller. Due to the current consumption of this IC and potential upstream USB Type-A devices, the PTN5100D V_MCUPWR pin should not be used to power anything in the USB Type-A receptacle subsystem.

Please contact Genesys Logic for more information.

4.1.8 CBTL02043A

The NXP CBTL02043A is a 2 differential channel, 2-to-1 multiplexer/demultiplexer switch for USB 3.1, PCI express Generation 3, or other high-speed serial interface applications. The CBTL02043A/B can switch two differential signals to one of two locations.

High speed data from USB Hub GL3523 is sent to CBTL02043A to switch the differential signals to one of two locations on USB type-C connector, to support type-C cable flip function.

For more information, see the datasheet for the specific part on http://www.nxp.com.

4.1.9 Power distribution methodology

As a USB Type-C adapter that supports charge-through functionality, this design has multiple ways of being powered and needs to be robust when transitioning from one scenario to another. See Fig 5 for a high level block diagram of how the power is distributed.

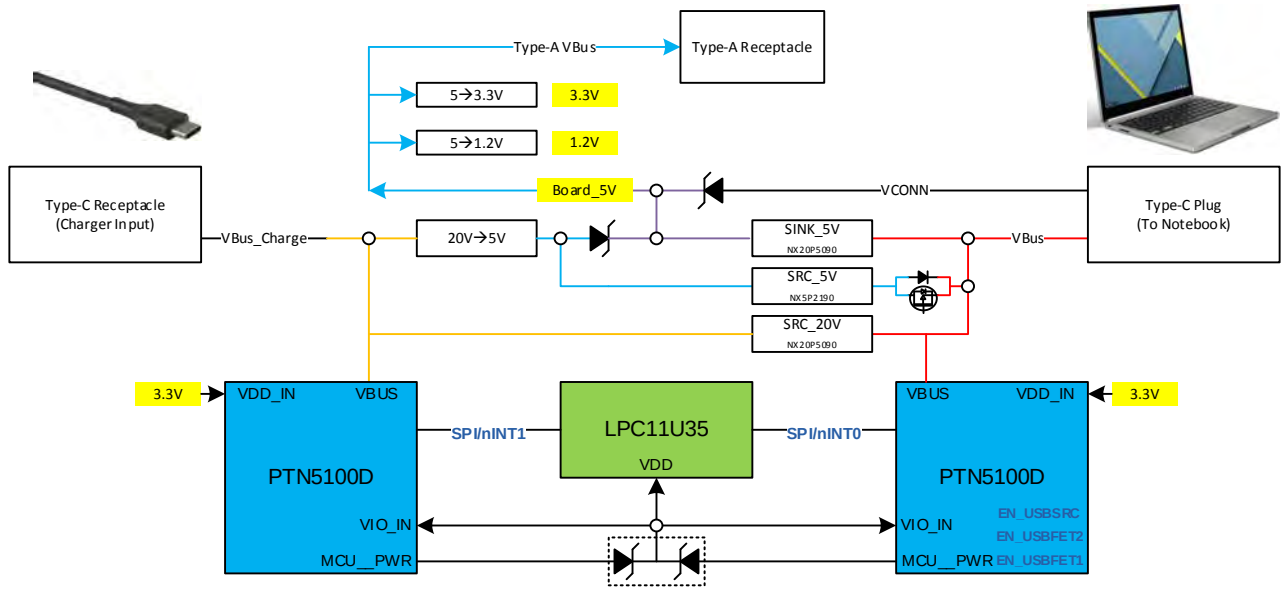

Fig 5. NXP USB Type-C 1 – 3 power distribution high level block diagram

The fundamental idea of this design is to “DIODE OR” all the potential power sources with DIODEs in order to accept any available power source. This includes the host’s

VBUS, host's VCONN, and charger VBUS. After ORing these power rails together, the output is used to power board components from the VGA and USB Type-A subsystems. The MCU receives power from ORing the MCU_PWR pins from both PTN5100D. Should a USB Type-C connection be established with either the charger or host, one of the PTN5100D should receive VBUS, thus powering the PTN5100D as well as the MCU.

4.1.9.1 Sourcing voltage

The simplest solution to implement charge-through functionality is to simply pass through the VBUS voltage from the charger to the host. While this may work functionally, it is not a fully reliable solution that will meet the worst case timing requirements of the USB PD specification. In order to provide a robust solution, it is necessary for the board to always have access to a 5 V power rail when acting as a power source. Power contracts as a source always start with providing 5 V on VBUS before transitioning to higher voltages.

In order to implement this with a load switch, some additional circuitry will need to be added in order to correctly do negative voltage transitions on VBUS from a higher voltage to 5 V. Without the external circuitry, the load switch's overvoltage lockout feature will render it unusable for a period of time when the adapter is sourcing a higher voltage such as 12 V. Should the sink request a 5 V PDO, the load switch will not be able to exit overvoltage lockout while VBUS is ramping down and cause the voltage on VBUS to drop below VSafe5V voltage levels momentarily. This additional circuitry will be controlled by the MCU in order to disconnect the load switch from the VBUS power rail while VBUS is still in a voltage level that would trigger the overvoltage lockout feature. See Fig 6 for a snapshot of the related circuitry.

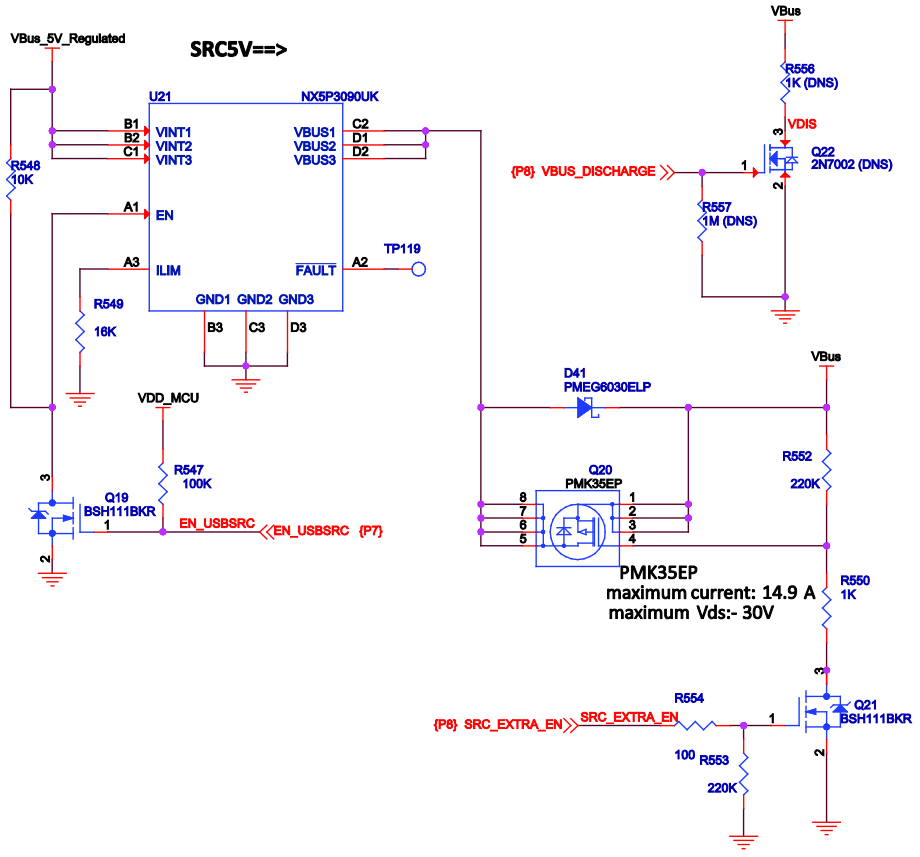

Fig 6. External 5 V load switch circuitry

4.1.9.2 Use VCONN as a power rail

The Type-C specification specifies VCONN as a power rail that can vary between 2.7 V to 5.5 V. In the case where the host does not supply VCONN at 5 V, a buck-boost converter is required to regulate VCONN to 5 V and avoid any voltage conflicts. Please refer to the schematic for the VCONN boost design.

Contact NXP either through the following support email or other means to get the latest reference design.

USBTypeC@nxp.com

5. Conclusion

The NXP USB Type-C 1 – 3 reference design user manual contains everything a vendor would need to quickly evaluate and build a prototype NXP USB Type-C 1 – 3 Multiport Adapter. The schematic provides a starting point while the included software is a fully functional USB PD kernel that can be programmed into the LPC11U35FHI33/CP3337 USB PD policy manager to seamlessly enable the schematic design. The USB PD kernel binary can be extended to include a DFU SBL to enable field updates in a user friendly way, minimizing the work required by the vendor from start to finish.

For any questions or concerns regarding NXP's USB Type-C solutions, please send an email to the following email address to get direct support:

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