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DATA BOOK

DRAM

SAMSUNG

Certified ISO 9001

BSI REGISTERED FIRM

NATIONAL ACCREDITATION OF CERTIFICATION BODIES

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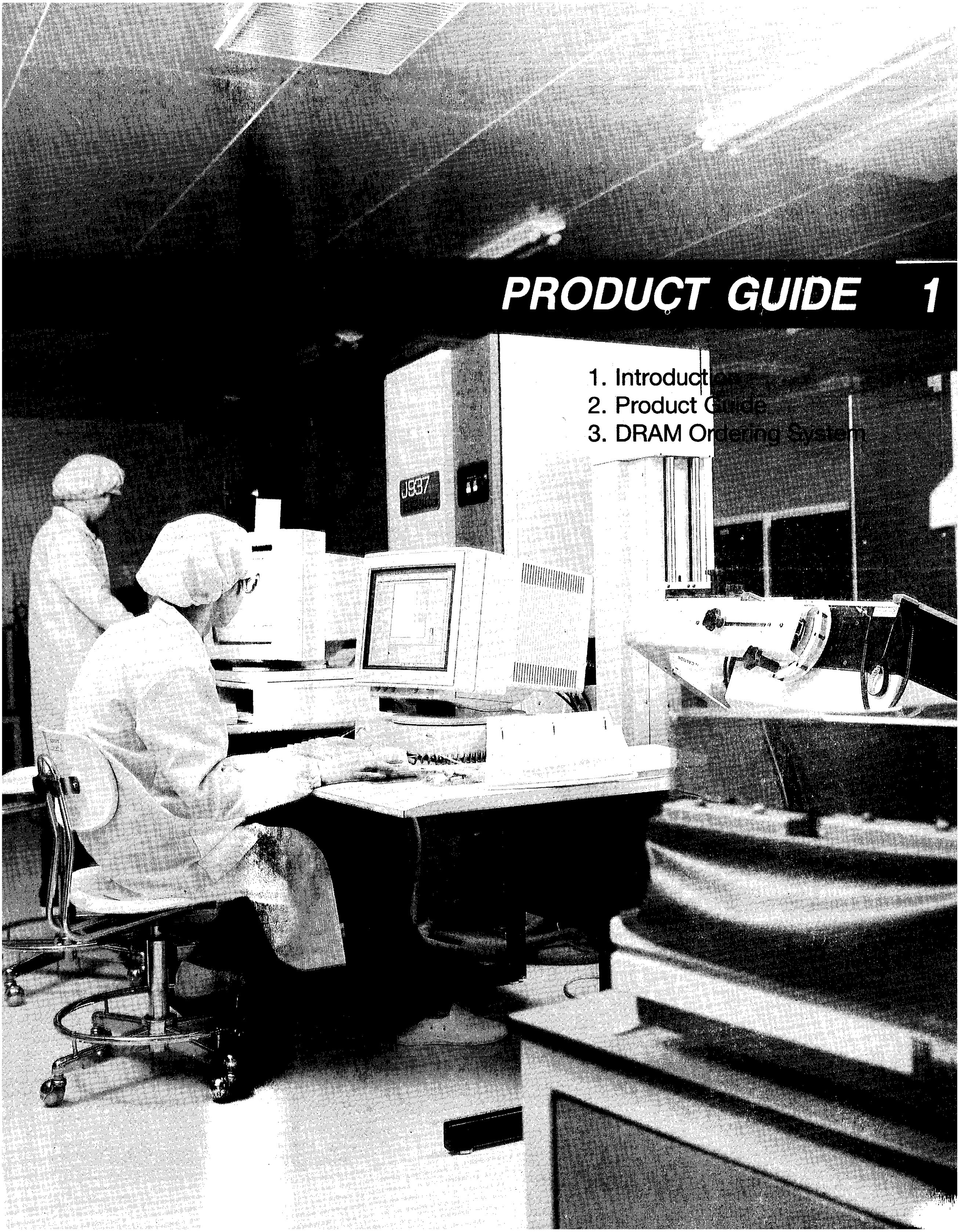

1. INTRODUCTION (DRAM)

1M bit	1Mx1		KM41C1000D-6	KM41C1000D-7	KM41C1000D-8
			KM41C1000D-L6	KM41C1000D-L7	KM41C1000D-L8
	256Kx4		KM44C256D-6	KM44C256D-7	KM44C256D-8
			KM44C256D-L6	KM44C256D-L7	KM44C256D-L8
4M bit	4Mx1	KM41C4000C-5	KM41C4000C-6	KM41C4000C-7	KM41C4000C-8
		KM41C4000CL-5	KM41C4000CL-6	KM41C4000CL-7	KM41C4000CL-8
		KM41C4002C-5	KM41C4002C-6	KM41C4002C-7	KM41C4002C-8
			KM41V4000C-6	KM41V4000C-7	KM41V4000C-8
			KM41V4000CL-6	KM41V4000CL-7	KM41V4000CL-8
	1Mx4	KM44C1000C-5	KM44C1000C-6	KM44C1000C-7	KM44C1000C-8
		KM44C1000CL-5	KM44C1000CL-6	KM44C1000CL-7	KM44C1000CL-8
		KM44C1010C-5	KM44C1010C-6	KM44C1010C-7	KM44C1010C-8
		KM44C1002C-5	KM44C1002C-6	KM44C1002C-7	KM44C1002C-8
		KM44C1003C-5	KM44C1003C-6	KM44C1003C-7	KM44C1003C-8
		KM44C1003CL-5	KM44C1003CL-6	KM44C1003CL-7	KM44C1003CL-8
		KM44C1004C-5	KM44C1004C-6	KM44C1004C-7	KM44C1004C-8
		KM44C1004CL-5	KM44C1004CL-6	KM44C1004CL-7	KM44C1004CL-8
			KM44V1000C-6	KM44V1000C-7	KM44V1000C-8
			KM44V1000CL-6	KM44V1000CL-7	KM44V1000CL-8
			KM44V1004C-6	KM44V1004C-7	KM44V1004C-8
			KM44V1004CL-6	KM44V1004CL-7	KM44V1004CL-8

4M B/W	512Kx8	KM48C512B-5	KM48C512B-6	KM48C512B-7	KM48C512B-8
		KM48C512BL-5	KM48C512BL-6	KM48C512BL-7	KM48C512BL-8
		KM48C514B-5	KM48C514B-6	KM48C514B-7	KM48C514B-8
		KM48C514BL-5	KM48C514BL-6	KM48C514BL-7	KM48C514BL-8
			KM48V512B-6	KM48V512B-7	KM48V512B-8
			KM48V512BL-6	KM48V512BL-7	KM48V512BL-8
			KM48V514B-6	KM48V514B-7	KM48V514B-8
			KM48V514BL-6	KM48V514BL-7	KM48V514BL-8
	512Kx9		KM49C512B-6	KM49C512B-7	KM49C512B-8
			KM49C512BL-6	KM49C512BL-7	KM49C512BL-8
	256Kx16	KM416C256B-5	KM416C256B-6	KM416C256B-7	KM416C256B-8
		KM416C256BL-5	KM416C256BL-6	KM416C256BL-7	KM416C256BL-8
		KM416C254B-5	KM416C254B-6	KM416C254B-7	KM416C254B-8
		KM416C254BL-5	KM416C254BL-6	KM416C254BL-7	KM416C254BL-8
			KM416V256B-6	KM416V256B-7	KM416V256B-8
			KM416V256BL-6	KM416V256BL-7	KM416V256BL-8
			KM416V254B-6	KM416V254B-7	KM416V254B-8
			KM416V254BL-6	KM416V254BL-7	KM416V254BL-8
	256Kx18		KM418C256B-6	KM418C256B-7	KM418C256B-8
			KM418C256BL-6	KM418C256BL-7	KM418C256BL-8

16M bit	16Mx1	KM41C16000A-5	KM41C16000A-6	KM41C16000A-7	KM441C16000A-8
		KM41C16000AL-5	KM41C16000AL-6	KM41C16000AL-7	KM41C16000AL-8
		KM41C16000ASL-5	KM41C16000ASL-6	KM41C16000ASL-7	KM41C16000ASL-8
		KM41C16002A-5	KM41C16002A-6	KM41C16002A-7	KM41C16002A-8
			KM41V16000A-6	KM41V16000A-7	KM41V16000A-8
			KM41V16000AL-6	KM41V16000AL-7	KM41V16000AL-8
			KM41V16000ASL-6	KM41V16000ASL-7	KM41V16000ASL-8
	4Mx4	KM44C4000A-5	KM44C4000A-6	KM44C4000A-7	KM44C4000A-8
		KM44C4000AL-5	KM44C4000AL-6	KM44C4000AL-7	KM44C4000AL-8
		KM44C4000ASL-5	KM44C4000ASL-6	KM44C4000ASL-7	KM44C4000ASL-8
		KM44C4100A-5	KM44C4100A-6	KM44C4100A-7	KM44C4100A-8
		KM44C4100AL-5	KM44C4100AL-6	KM44C4100AL-7	KM44C4100AL-8
		KM44C4100ASL-5	KM44C4100ASL-6	KM44C4100ASL-7	KM44C4100ASL-8
		KM44C4002A-5	KM44C4002A-6	KM44C4002A-7	KM44C4002A-8
		KM44C4102A-5	KM44C4102A-6	KM44C4102A-7	KM44C4102A-8
		KM44C4003A-5	KM44C4003A-6	KM44C4003A-7	KM44C4003A-8
		KM44C4003AL-5	KM44C4003AL-6	KM44C4003AL-7	KM44C4003AL-8
		KM44C4003ASL-5	KM44C4003ASL-6	KM44C4003ASL-7	KM44C4003ASL-8
		KM44C4103A-5	KM44C4103A-6	KM44C4103A-7	KM44C4103A-8
		KM44C4103AL-5	KM44C4103AL-6	KM44C4103AL-7	KM44C4103AL-8
		KM44C4103ASL-5	KM44C4103ASL-6	KM44C4103ASL-7	KM44C4103ASL-8
		KM44C4004A-5	KM44C4004A-6	KM44C4004A-7	KM44C4004A-8
		KM44C4004AL-5	KM44C4004AL-6	KM44C4004AL-7	KM44C4004AL-8
		KM44C4004ASL-5	KM44C4004ASL-6	KM44C4004ASL-7	KM44C4004ASL-8

16M bit	4Mx4	KM44C4104A-5	KM44C4104A-6	KM44C4002A-7	KM44C4002A-8
		KM44C4104AL-5	KM44C4104AL-6	KM44C4104AL-7	KM44C4104AL-8
		KM44C4104ASL-5	KM44C4104ASL-6	KM44C4104ASL-7	KM44C4104ASL-8
		KM44C4010A-5	KM44C4010A-6	KM44C4010A-7	KM44C4010A-8
		KM44C4110A-5	KM44C4110A-6	KM44C4110A-7	KM44C4110A-8
			KM44V4000A-6	KM44V4000A-7	KM44V4000A-8
			KM44V4000AL-6	KM44V4000AL-7	KM44V4000AL-8
			KM44V4000ASL-6	KM44V4000ASL-7	KM44V4000ASL-8
			KM44V4100A-6	KM44V4100A-7	KM44V4100A-8
			KM44V4100AL-6	KM44V4100AL-7	KM44V4100AL-8
			KM44V4100ASL-6	KM44V4100ASL-7	KM44V4100ASL-8
			KM44V4004A-6	KM44V4004A-7	KM44V4004A-8
			KM44V4004AL-6	KM44V4004AL-7	KM44V4004AL-8
			KM44V4004ASL-6	KM44V4004ASL-7	KM44V4004ASL-8
			KM44V4104A-6	KM44V4104A-7	KM44V4104A-8
			KM44V4104AL-6	KM44V4104AL-7	KM44V4104AL-8
			KM44V4104ASL-6	KM44V4104ASL-7	KM44V4104ASL-8

16M B/W — 2Mx8

KM48C2000A-5	KM48C2000A-6	KM48C2000A-7	KM48C2000A-8
KM48C2000AL-5	KM48C2000AL-6	KM48C2000AL-7	KM48C2000AL-8
KM48C2000ASL-5	KM48C2000ASL-6	KM48C2000ASL-7	KM48C2000ASL-8
KM48C2100A-5	KM48C2100A-6	KM48C2100A-7	KM48C2100A-8
KM48C2100AL-5	KM48C2100AL-6	KM48C2100AL-7	KM48C2100AL-8
KM48C2100ASL-5	KM48C2100ASL-6	KM48C2100ASL-7	KM48C2100ASL-8
KM48C2004A-5	KM48C2004A-6	KM48C2004A-7	KM48C2004A-8
KM48C2004AL-5	KM48C2004AL-6	KM48C2004AL-7	KM48C2004AL-8
KM48C2004ASL-5	KM48C2004ASL-6	KM48C2004ASL-7	KM48C2004ASL-8
KM48C2104A-5	KM48C2104A-6	KM48C2104A-7	KM48C2104A-8
KM48C2104AL-5	KM48C2104AL-6	KM48C2104AL-7	KM48C2104AL-8
KM48C2104ASL-5	KM48C2104ASL-6	KM48C2104ASL-7	KM48C2104ASL-8
	KM48V2000A-6	KM48V2000A-7	KM48V2000A-8
	KM48V2000AL-6	KM48V2000AL-7	KM48V2000AL-8
	KM48V2000ASL-6	KM48V2000ASL-7	KM48V2000ASL-8
	KM48V2100A-6	KM48V2100A-7	KM48V2100A-8
	KM48V2100AL-6	KM48V2100AL-7	KM48V2100AL-8
	KM48V2100ASL-6	KM48V2100ASL-7	KM48V2100ASL-8
	KM48V2004A-6	KM48V2004A-7	KM48V2004A-8
	KM48V2004AL-6	KM48V2004AL-7	KM48V2004AL-8
	KM48V2004ASL-6	KM48V2004ASL-7	KM48V2004ASL-8
	KM48V2104A-6	KM48V2104A-7	KM48V2104A-8
	KM48V2104AL-6	KM48V2104AL-7	KM48V2104AL-8
	KM48V2104ASL-6	KM48V2104ASL-7	KM48V2104ASL-8

16M B/W	1Mx16	KM416C1000A-6	KM416C1000A-7	KM416C1000A-8
		KM416C1000A-L6	KM416C1000A-L7	KM416C1000A-L8
		KM416C1200A-6	KM416C1200A-7	KM416C1200A-8
		KM416C1200A-L6	KM416C1200A-L7	KM416C1200A-L8
		KM416C1004A-6	KM416C1004A-7	KM416C1004A-8
		KM416C1004A-L6	KM416C1004A-L7	KM416C1004A-L8
		KM416C1204A-6	KM416C1204A-7	KM416C1204A-8
		KM416C1204A-L6	KM416C1204A-L7	KM416C1204A-L8
		KM416V1000A-6	KM416V1000A-7	KM416V1000A-8
		KM416V1000A-L6	KM416V1000A-L7	KM416V1000A-L8
		KM416V1200A-6	KM416V1200A-7	KM416V1200A-8
		KM416V1200A-L6	KM416V1200A-L7	KM416V1200A-L8
		KM416V1004A-6	KM416V1004A-7	KM416V1004A-8
		KM416V1004A-L6	KM416V1004A-L7	KM416V1004A-L8
		KM416V1204A-6	KM416V1204A-7	KM416V1204A-8
		KM416V1204A-L6	KM416V1204A-L7	KM416V1204A-L8
	512Kx32		KM432V502-7	KM432V502-8
			KM432V502-L7	KM432V502-L8
			KM432V522-7	KM432V522-8
			KM432V522-L7	KM432V522-L8
			KM432V504-7	KM432V504-8
			KM432V504-L7	KM432V504-L8
			KM432V524-7	KM432V524-8
			KM432V524-7	KM432V524-L8

64M bit
* 1st Gen.

Density	Organization			
64M bit	16Mx4	KM44V16000-5	KM44V16000-6	KM44V16000-7
		KM44V16100-5	KM44V16100-6	KM44V16100-7
	8Mx8	KM48V8000-5	KM48V8000-6	KM48V8000-7
		KM48V8100-5	KM48V8100-6	KM48V8100-7

64M bit
* 2nd Gen.

Density	Organization			
64M bit	16Mx4	KM44V16000A-5	KM44V16000A-6	KM44V16000A-7
		KM44V16000A-L5	KM44V16000A-L6	KM44V16000A-L7
		KM44V16100A-5	KM44V16100A-6	KM44V16100A-7
		KM44V16100A-L5	KM44V16100A-L6	KM44V16100A-L7
	8Mx8	KM48V8000A-5	KM48V8000A-6	KM48V8000A-7
		KM48V8000A-L5	KM48V8000A-L6	KM48V8000A-L7
		KM48V8100A-5	KM48V8100A-6	KM48V8100A-7
		KM48V8100A-L5	KM48V8100A-L6	KM48V8100A-L7

2. PRODUCT GUIDE (DRAM)

Density	Org.	Power Supply	Part Number	Speed(ns)	Features	Packages (#)
1M bit	1Mx1	5V±10%	KM41C1000D# KM41C1000D-L#	60/70/80	Fast Page	P:18 Pin DIP (1Mx1) 20 Pin DIP (256Kx4) J:20 Pin SOJ Z:20 Pin ZIP
	256Kx4	5V±10%	KM44C256D# KM44C256D-L#	60/70/80	Fast Page	
4M bit	4Mx1	5V±10%	KM41C4000C# KM41C4000CL# KM41C4002C#	50/60/70/80	Fast Page Static Column	P:20 Pin DIP J:20 Pin SOJ Z:20 Pin ZIP T:20 Pin TSOP-II (Forward) TR:20 Pin TSOP-II (Reverse)
		3.3V±0.3V	KM41V4000C# KM41V4000CL#	60/70/80	Fast Page	
	1Mx4	5V±10%	KM44C1000C# KM44C1000CL# KM44C1010C# KM44C1002C# KM44C1003C# KM44C1003CL# KM44C1004C# KM44C1004CL#	50/60/70/80	Fast Page Fast Page with WPB Static Column Quad CAS EDO	*Quad CAS J:24 Pin SOJ T:24 Pin TSOP-II (Forward) TR:24 Pin TSOP-II (Reverse)
		3.3V±0.3V	KM44V1000C# KM44V1000CL# KM44V1004C# KM44V1004CL#	60/70/80	Fast Page EDO	
4M B/W	512Kx8	5V±10%	KM48C512B# KM48C512BL# KM48C514B# KM48C514BL#	50/60/70/80	Fast Page EDO	J:28 Pin SOJ T:28 Pin TSOP-II(Forward) TR:28 Pin TSOP-II(Reverse)
		3.3V±0.3V	KM48V512B# KM48V512BL# KM48V514B# KM48V514BL#	60/70/80	Fast Page EDO	
	512Kx9	5V±10%	KM49C512B# KM49C512BL#	60/70/80	Fast Page	
	256Kx16	5V±10%	KM416C256B# KM416C256BL# KM416C254B# KM416C254BL#	50/60/70/80	Fast Page EDO	J:40 Pin SOJ T:40 Pin TSOP-II (Forward) TR:40 Pin TSOP-II(Reverse)

Density	Org.	Power Supply	Part Number	Speed(ns)	Features	Packages (#)
4M B/W	256Kx16	3.3V±0.3V	KM416V256B#	60/70/80	Fast Page(4K)	J:40 Pin SOJ
			KM416V256BL#			T:40 Pin TSOP-II(Forward)
			KM416V254B#		EDO	TR:40 Pin TSOP-II(Reverse)
			KM416V254BL#			
	256Kx18	5V±10%	KM418C256B#	60/70/80	Fast Page	
			KM418C256BL#			
16M bit	16Mx1	5V±10%	KM41C16000A#	50/60/70/80	Fast Page(4K)	J:24 Pin SOJ (400mil)
			KM41C16000AL#			T:24 Pin TSOP-II (Forward)
			KM41C16000ASL#			(400mil)
			KM41C16002A#		Static Column(4K)	TR:24 Pin TSOP-II (Reverse)
		3.3V±0.3V	KM41V16000A#	60/70/80	Fast Page(4K)	(400mil)
			KM41V16000AL#			K:24 Pin SOJ (300mil)
			KM41V16000ASL#			S:24 Pin TSOP-II(Forward)
	4Mx4	5V±10%	KM44C4000A#	50/60/70/80	Fast Page(4K)	(300mil)
			KM44C4000AL#			SR:24 Pin TSOP-II(Reverse)
			KM44C4000ASL#			(300mil)
			KM44C4100A#		Fast Page(2K)	
			KM44C4100AL#			
			KM44C4100ASL#			
			KM44C4002A#		Static Column(4K)	
			KM44C4102A#		Static Column(2K)	
			KM44C4003A#		Quad CAS(4K)	*Quad CAS
			KM44C4003AL#			J:28 Pin SOJ
			KM44C4003ASL#			T:28 Pin TSOP-II(Forward)
			KM44C4103A#		Quad CAS(2K)	TR:28 Pin TSOP-II(Reverse)
			KM44C4103AL#			
			KM44C4103ASL#			
			KM44C4004A#		EDO(4K)	
			KM44C4004AL#			
			KM44C4004ASL#			
			KM44C4104A#		EDO(2K)	
			KM44C4104AL#			
			KM44C4104ASL#			
			KM44C4010A#		Fast Page with WPB(4K)	

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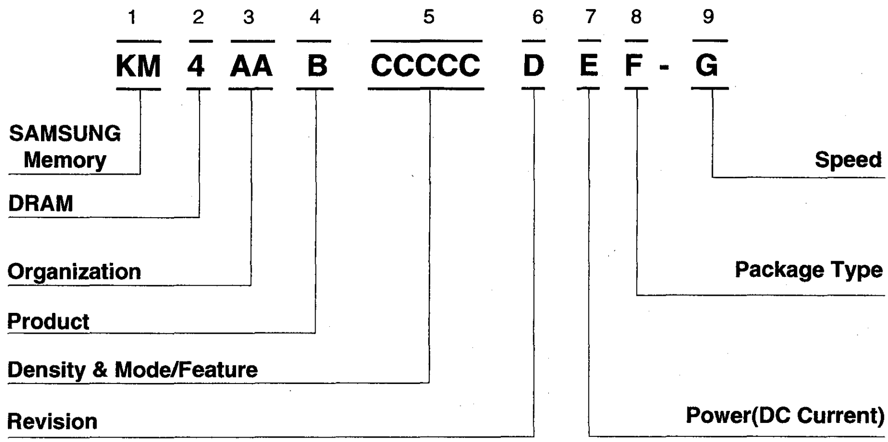
Density	Org.	Power Supply	Part Number	Speed(ns)	Features	Packages (#)
16M bit	4Mx4	5V±10%	KM44C4110A#	50/60/70/80	Fast Page with WPB(2K)	J:24 Pin SOJ (400mil)
		3.3V±0.3V	KM44V4000A#	60/70/80	Fast Page(4K)	T:24 Pin TSOP-II (Forward) (400mil)
			KM44V4000AL#			TR:24 Pin TSOP-II (Reverse) (400mil)
			KM44V4000ASL#			K:24 Pin SOJ(300mil)
			KM44V4100A#		Fast Page(2K)	S:24 Pin TSOP-II(Forward) (300mil)
			KM44V4100AL#			SR:24 Pin TSOP-II(Reverse) (300mil)
			KM44V4100ASL#			
			KM44V4004A#		EDO(4K)	
			KM44V4004AL#			
			KM44V4004ASL#			
			KM44V4104A#		EDO(2K)	
			KM44V4104AL#			
			KM44V4104ASL#			
16M B/W	2Mx8	5V±10%	KM48C2000A#	50/60/70/80	Fast Page(4K)	J:28 Pin SOJ
			KM48C2000AL#			T:28 Pin TSOP-II (Forward)
			KM48C2000ASL#			TR:28 Pin TSOP-II (Reverse)
			KM48C2100A#		Fast Page(2K)	
			KM48C2100AL#			
			KM48C2100ASL#			
			KM48C2004A#		EDO(4K)	
			KM48C2004AL#			
			KM48C2004ASL#			
			KM48C2104A#		EDO(2K)	
			KM48C2104AL#			
			KM48C2104ASL#			
		3.3V±0.3V	KM48V2000A#	60/70/80	Fast Page(4K)	
			KM48V2000AL#			
			KM48V2000ASL#			
			KM48V2100A#		Fast Page(2K)	
			KM48V2100AL#			
			KM48V2100ASL#			
			KM48V2004A#		EDO(4K)	
			KM48V2004AL#			
			KM48V2004ASL#			

Density	Org.	Power Supply	Part Number	Speed(ns)	Features	Packages (#)
16M B/W	2Mx8	3.3V±0.3V	KM48V2104A#	60/70/80	EDO(2K)	J:28 Pin SOJ
			KM48V2104AL#			T:28 Pin TSOP-II (Forward)
			KM48V2104ASL#			TR:28 Pin TSOP-II(Reverse)
	1Mx16	5V±10%	KM416C1000A#	60/70/80	Fast Page(4K)	J:42 Pin SOJ
			KM416C1000A#-L			T:44 Pin TSOP-II (Forward)
			KM416C1200A#		Fast Page(1K)	R:44 Pin TSOP-II(Reverse)
			KM416C1200A#-L			
			KM416C1004A#		EDO(4K)	
			KM416C1004A#-L			
			KM416C1204A#		EDO(1K)	
			KM416C1204A#-L			
		3.3V±0.3V	KM416V1000A#	60/70/80	Fast Page(4K)	
			KM416V1000A#-L			
			KM416V1200A#		Fast Page(1K)	
			KM416V1200A#-L			
			KM416V1004A#		EDO(4K)	
			KM416V1004A#-L			
			KM416V1204A#		EDO(1K)	
			KM416V1204A#-L			
	512Kx32	3.3V±0.3V	KM432V502#	70/80	Fast Page(4K)	T:70 Pin TSOP-II (Forward)
			KM432V502#-L			R:70 Pin TSOP-II(Reverse)
			KM432V522#		Fast Page(1K)	
			KM432V522#-L			
			KM432V504#		EDO(4K)	
			KM432V504#-L			
			KM432V524#		EDO(1K)	
			KM432V524#-L			

Density	Org.	Power Supply	Part Number	Speed(ns)	Features	Packages (#)
64M bit	16Mx4	3.3V±0.3V	KM44V16000#	50/60/70	Fast Page(8K)	J : 34 Pin SOJ
			KM44V16100#		Fast Page(4K)	
	8Mx8	3.3V±0.3V	KM48V8000#	50/60/70	Fast Page(8K)	
			KM48V8100#		Fast Page(4K)	
64M bit	16Mx4	3.3V±0.3V	KM44V16000A#	50/60/70	Fast Page(8K)	J : 32 Pin SOJ
			KM44V16000A#-L			T : 32 pin TSOP II(Forward)
			KM44V16100A#		Fast Page(4K)	R : 32 pin TSOP II(Reverse)
			KM44V16100A#-L			
	8Mx8	3.3V±0.3V	KM48V8000A#	50/60/70	Fast Page(8K)	
			KM48V8000A#-L			
			KM48V8100A#		Fast Page(4K)	
			KM48V8100A#-L			

3. DRAM ORDERING SYSTEM



1. SAMSUNG Memory

2. DRAM(4)

3. Organization

1	x 1
4	x 4
8	x 8
9	x 9
16	x 16
18	x 18
32	x 32

4. Product

C	5V
V	3.3V

5. Density & Mode/Feature

Refer to the previous "Chapter 2. Product Guide."

6. Revision

Blank	1st Gen.
A	2nd Gen.
B	3rd Gen.
C	4th Gen.
D	5th Gen.

7. Power(DC Current)

Blank	Normal
L	Low power with Self refresh
SL	Super Low power

8. Package Type

J	SOJ
T	TSOP II (Forward)
TR	TSOP II (Reverse)
P	DIP
Z	ZIP
K	SOJ(Shrinked PKG,SOJ)
S	TSOP II (Shrinked PKG,Forward)
SR	TSOP II (Shrinked PKG,Reverse)

9. Speed

- 5	50 ns
- 6	60 ns
- 7	70 ns
- 8	80 ns

* NEW DRAM ORDERING SYSTEM

This new DRAM ordering system will be used for all SAMSUNG's New DRAM products from 1995.
In '95 DRAM Databook, only used for 1M 5th Gen., 16M Byte Word Wide 2nd Gen. and 64M DRAM.

1	2	3	4	5	6	7		8	9
KM	4	AA	B	CCCCC	D	E	-	F	GG

- KM — SAMSUNG Memory
- 4 — DRAM
- AA — Organization
- B — Product
- CCCCC — Density & Mode/Feature
- D — Revision
- E — Package Type
- F — Power(DC Current)
- GG — Speed

1. SAMSUNG Memory

2. DRAM(4)

3. Organization

1	x 1
4	x 4
8	x 8
9	x 9
16	x 16
18	x 18
32	x 32

4. Product

C	5V
V	3.3V

5. Density & Mode/Feature (Same)

6. Revision

Blank	1st Gen.
A	2nd Gen.
B	3rd Gen.
C	4th Gen.
D	5th GEn.

7. Package Type

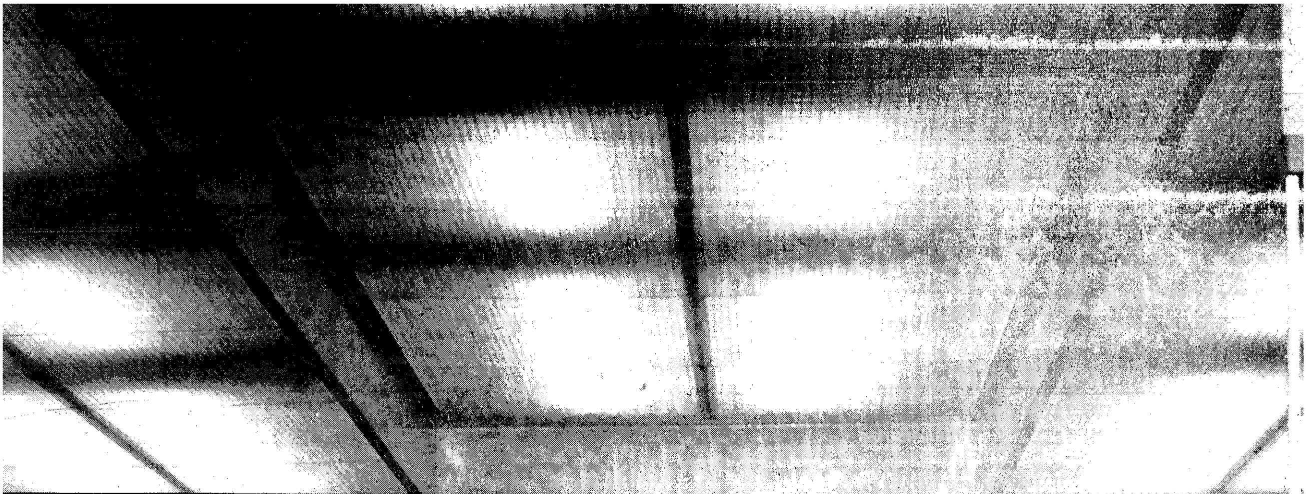
J	SOJ
T	TSOP II (Forward)
R	TSOP II (Reverse)
P	DIP
Z	ZIP
K	SOJ(Shrinked PKG,SOJ)
S	TSOP II (Shrinked PKG,Forward)
W	TSOP II (Shrinked PKG,Reverse)

8. Power(DC Current)

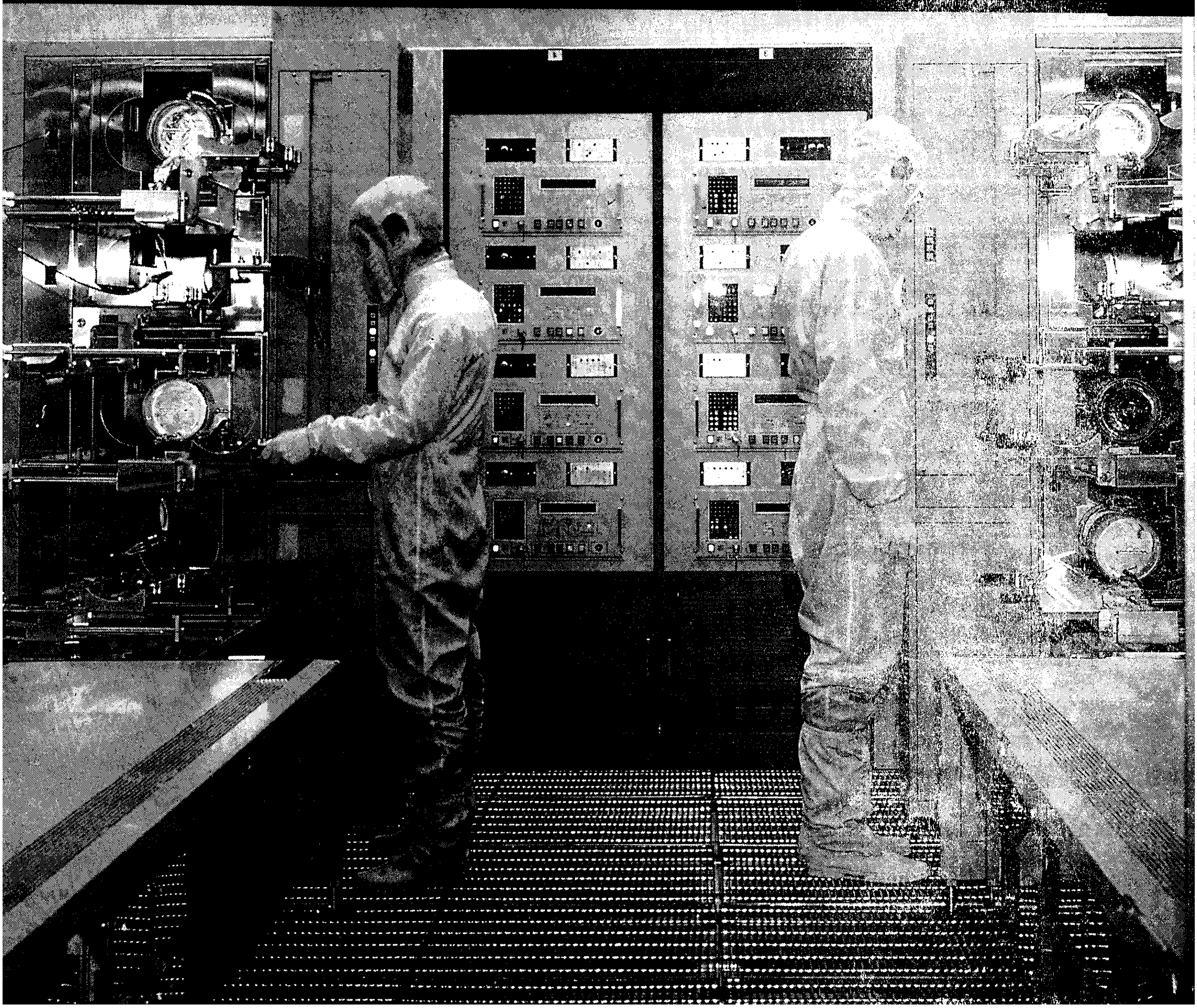
Blank	Normal
L	Low power with Self refresh
H	Super Low power

9. Speed

- 5	50 ns
- 6	60 ns
- 7	70 ns
- 8	80 ns



DATA SHEETS 2



1M DRAM

- KM41C1000D
- KM44C256D

1M x 1 Bit CMOS Dynamic RAM with Fast Page Mode

DESCRIPTION

This is a family of 1,048,576 x 1 bit Fast Page Mode CMOS DRAMs. Fast Page Mode offers high speed random access of memory cells within the same row. Access time(-6, -7 or -8), power consumption (Normal or Low power) , and package type (SOJ, ZIP,DIP) are optional features of this family. All of this family have $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$-only refresh and Hidden refresh capabilities.
This 1Mx1 Fast Page Mode DRAM Family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability.

FEATURES

- Part Identification
  - KM41C1000D/D-L(5V)

- Active Power Dissipation

Unit : mW

Speed	Active Power Dissipation
-6	385
-7	358
-8	330

- Refresh cycles

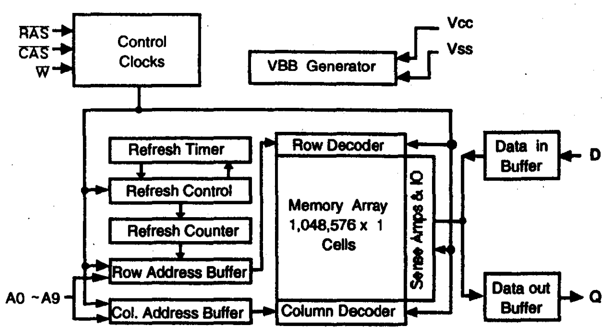
Part No.	Refresh Cycle	Refresh period	
		Normal	L
KM41C1000D	512	8ms	128ms

- Performance range:

Speed	tRAC	tCAC	tRC	tPC
-6	60ns	15ns	110ns	40ns
-7	70ns	20ns	130ns	45ns
-8	80ns	20ns	150ns	50ns

- Fast Page Mode operation
- $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh capability
- $\overline{\text{RAS}}$-only and Hidden refresh capability
- TTL(5V) compatible inputs and outputs
- 256K x 4 fast test mode
- JEDEC Standard pinout
- Available in Plastic SOJ, ZIP and DIP packages
- Single +5V±10% power supply

FUNCTIONAL BLOCK DIAGRAM



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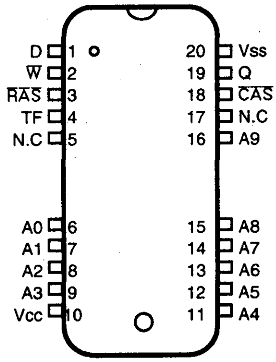
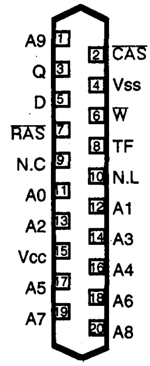
PIN CONFIGURATION (Top Views)

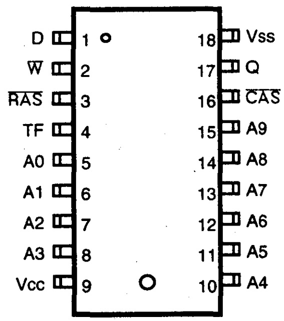
• KM41C1000DJ



• KM41C1000DZ



• KM41C1000DP



Pin Name	Pin Function
A0 - A9	Address Inputs
D	Data In
Q	Data Out
Vss	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
Vcc	Power(+5.0V)
N.C	No Connection
TF	Test Function
NL	No Lead

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	V_{CC}	-1 to +7.0	V
Storage temperature	Tstg	-55 to +150	°C
Power dissipation	P_D	600	mW
Short circuit output current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to Vss, T_A= 0 to 70 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input high voltage	V_{IH}	2.4	-	Vcc+1[*1]	V
Input low voltage	V_{IL}	-1.0[*2]	-	0.8	V

*1 : Vcc+2.0V at pulse width ≤ 20ns (pulse width is measured at Vcc)

*2 : -2.0V at pulse width ≤ 20ns (pulse is measured at Vss)

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Units
Input leakage current (Any input $0 \leq V_{IN} \leq V_{CC}+0.5V$ all other pins not under test=0 volts.)	$I_{I(L)}$	- 5	5	μA
Output leakage current (Data out is disabled, $0V \leq V_{OUT} \leq V_{CC}$)	$I_{O(L)}$	- 5	5	μA
Output high voltage level(I_{OH}=-5mA)	V_{OH}	2.4	-	V
Output low voltage level(I_{OL}=4.2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Symbol	Power	Speed	Max KM41C1000D	Units
I_{CC1}	Don't care	-6 -7 -8	60 55 50	mA mA mA
I_{CC2}	Don't care	Don't care	2	mA
I_{CC3}	Don't care	-6 -7 -8	60 55 50	mA mA mA
I_{CC4}	Don't care	-6 -7 -8	50 45 40	mA mA mA
I_{CC5}	Normal L	Don't care	1 100	mA µA
I_{CC6}	Don't care	-6 -7 -8	60 55 50	mA mA mA
I_{CC7}	L	Don't care	100	µA

I_{CC1}* : Operating current ($\overline{RAS}$ and $\overline{CAS}$, Address cycling @tRC=min.)

I_{CC2} : Standby current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}* : $\overline{RAS}$-only refresh current ($\overline{CAS}$=V_{IH}, $\overline{RAS}$,Address cycling @tRC=min.)

I_{CC4}* : Fast Page Mode current ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address cycling @tPC=min.)

I_{CC5} : Standby current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)

I_{CC6}* : $\overline{CAS}$-before-$\overline{RAS}$ refresh current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode
Input high voltage(V_{IH})=V_{CC}-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{CAS}$=$\overline{CAS}$-before-$\overline{RAS}$ cycling or 0.2V
D_{IN}=$\overline{W}$=A0 ~ A9 = V_{CC}-0.2V or 0.2V , T_{RC}= 125µs(L-ver), T_{RAS}=T_{RAS}min~300 ns

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1}, I_{CC3} and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, Address can be changed maximum once within one fast page mode cycle time tPC.

CAPACITANCE(T_A=25°C,Vcc=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [D]	C_{IN1}	-	5	pF
Input capacitance [A0 - A9]	C_{IN2}	-	6	pF
Input capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$]	C_{IN3}	-	7	pF
Output capacitance [Q]	C_{OUT}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 1,2)
Test condition : Vcc=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.0/0.8V

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	110		130		150		ns	
Read-modify-write cycle time	tRWC	130		150		170		ns	
Access time from $\overline{RAS}$	tRAC		60		70		80	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		15		20		20	ns	3,4,5
Access time from column address	tAA		30		35		40	ns	3,9
$\overline{CAS}$ to output in Low-Z	tCLZ	0		0		0		ns	3
Output buffer turn-off delay	tOFF	0	15	0	20	0	20	ns	6
Transition time (rise and fall)	tT	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	tRP	40		50		60		ns	
$\overline{RAS}$ pulse width	tRAS	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ hold time	tRSH	15		20		20		ns	
$\overline{CAS}$ hold time	tCSH	60		70		80		ns	
$\overline{CAS}$ pulse width	tCAS	15	10K	20	10K	20	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	30	15	35	15	40	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	
Column address hold time	tCAH	15		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	tAR	50		55		60		ns	14
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		ns	
Write command hold time	tWCH	10		10		10		ns	
Write command hold time referenced to $\overline{RAS}$	tWCR	45		50		55		ns	14
Write command pulse width	tWP	10		10		10		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		15		15		ns	
Write command to $\overline{CAS}$ lead time	tCWL	15		15		15		ns	

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 2)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		ns	9
Data hold time	tDH	15		15		15		ns	9
Data hold time referenced to $\overline{RAS}$	tDHR	50		55		60		ns	14
Refresh period(Normal)	tREF		8		8		8	ms	
Refresh period(L -ver)	tREF		128		128		128	ms	
Write command set-up time	tWCS	0		0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	15		20		20		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	60		70		80		ns	7
Column address to $\overline{W}$ delay time	tAWD	30		35		40		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	35		40		45		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	5		5		5		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	15		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		ns	
$\overline{CAS}$ precharge time($\overline{CBR}$ counter test cycle)	tCPT	20		25		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		35		35		45	ns	3
Fast Page mode cycle time	tPC	40		45		50		ns	
Fast Page mode read-modify-write cycle time	tPRWC	60		60		65		ns	
$\overline{CAS}$ precharge time (Fast page cycle)	tCP	10		10		10		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	60	200K	70	200K	80	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	40		45		50		ns	

NOTES

1. An initial pause of 200µs is required after power up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD(max) is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS≥tWCS(min),the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
11. Normal operation requires the "TF" pin to be connected to Vss or TTL logic low level or left unconnected on the printed wiring board.
12. When the "TF" pin is connected to a defined positive voltage, the internal test function may be activated. Contact Samsung for specific operational details of the "test function".
13. In a test mode cycle, the value of tRAC, tCAC, tAA is delayed for 3ns.
14. tAR, tWCR, and tDHR are referenced to tRAD(MAX).

2

256K x 4 Bit CMOS Dynamic RAM with Fast Page Mode

DESCRIPTION

This is a family of 262,144 x 4 bit Fast Page Mode CMOS DRAMs. Fast Page Mode offers high speed random access of memory cells within the same row. Access time(-6, -7 or -8), power consumption (Normal or Low power), and package type (SOJ, ZIP,DIP) are optional features of this family. All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities.
This 256Kx4 Fast Page Mode DRAM Family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability.

FEATURES

- Part Identification
  - KM44C256D/D-L(5V)

- Active Power Dissipation

Unit : mW

Speed	Active Power Dissipation
-6	385
-7	358
-8	330

- Refresh cycles

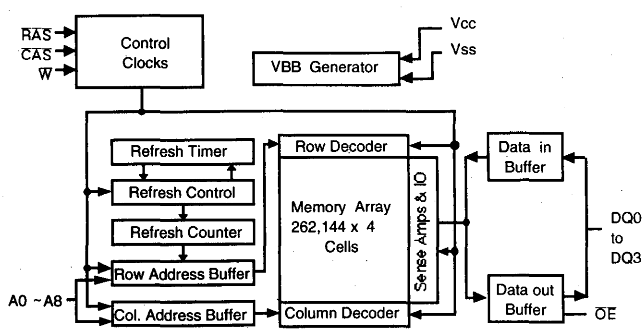
Part No.	Refresh Cycle	Refresh period	
		Normal	L
KM44C256D	512	8ms	128ms

- Performance range:

Speed	tRAC	tCAC	tRC	tPC
-6	60ns	15ns	110ns	40ns
-7	70ns	20ns	130ns	45ns
-8	80ns	20ns	150ns	50ns

- Fast Page Mode operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- TTL(5V) compatible inputs and outputs
- Early write or Output Enable controlled write
- JEDEC Standard pinout
- Available in Plastic SOJ, ZIP, and DIP packages
- Single +5V±10% power supply

FUNCTIONAL BLOCK DIAGRAM



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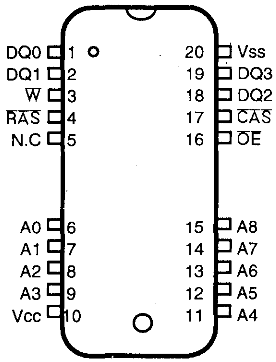
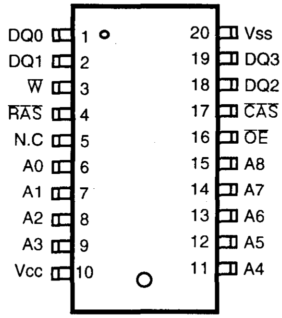
PIN CONFIGURATION (Top Views)

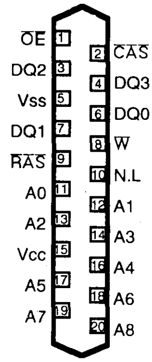
• **KM44C256DJ**



• **KM44C256DP**



• **KM44C256DZ**



Pin Name	Pin Function
A0 - A8	Address Inputs
DQ0~3	Data In/out
Vss	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Outputs Enable
Vcc	Power(+5.0V)
N.C	No Connection
NL	No Lead

2

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	V_{CC}	-1 to +7.0	V
Storage temperature	Tstg	-55 to +150	°C
Power dissipation	P_D	600	mW
Short circuit output current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to Vss, T_A= 0 to 70 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input high voltage	V_{IH}	2.4	-	Vcc+1[*1]	V
Input low voltage	V_{IL}	-2.0[*2]	-	0.8	V

*1 : Vcc+2.0V at pulse width ≤ 20ns (pulse width is measured at Vcc)

*2 : -2.0V at pulse width ≤ 20ns (pulse is measured at Vss)

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Units
Input leakage current (Any input $0 \le V_{IN} \le Vcc+0.5V$ all other pins not under test=0 volts.)	$I_{I(L)}$	-5	5	µA
Output leakage current (Data out is disabled, $0V \le V_{OUT} \le Vcc$)	$I_{O(L)}$	-5	5	µA
Output high voltage level(I_{OH}=-5mA)	V_{OH}	2.4	-	V
Output low voltage level(I_{OL}=4.2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Symbol	Power	Speed	Max KM44C256D	Units
I_{CC1}	Don't care	-6 -7 -8	60 55 50	mA mA mA
I_{CC2}	Don't care	Don't care	2	mA
I_{CC3}	Don't care	-6 -7 -8	60 55 50	mA mA mA
I_{CC4}	Don't care	-6 -7 -8	50 45 40	mA mA mA
I_{CC5}	Normal L	Don't care	1 100	mA μA
I_{CC6}	Don't care	-6 -7 -8	60 55 50	mA mA mA
I_{CC7}	L	Don't care	100	μA

I_{CC1}* : Operating current ($\overline{RAS}$ and $\overline{CAS}$, Address cycling @tRC=min.)

I_{CC2} : Standby current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}* : $\overline{RAS}$-only refresh current ($\overline{CAS}$=V_{IH}, $\overline{RAS}$,Address cycling @tRC=min.)

I_{CC4}* : Fast Page Mode current ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address cycling @tPC=min.)

I_{CC5} : Standby current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)

I_{CC6}* : $\overline{CAS}$-before-$\overline{RAS}$ refresh current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode
Input high voltage(V_{IH})=V_{CC}-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{CAS}$=$\overline{CAS}$-before-$\overline{RAS}$ cycling or 0.2V
D_{IN}=$\overline{W}$=A0 ~ A8= V_{CC}-0.2V or 0.2V , T_{RC}= 125μs(L-ver), T_{RAS}=T_{RAS}min~300 ns

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1}, I_{CC3} and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, Address can be changed maximum once within one fast page mode cycle time tPC.

CAPACITANCE(T_A=25°C,Vcc=5V , f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A8]	C_{IN1}	-	6	pF
Input capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$,$\overline{OE}$]	C_{IN2}	-	7	pF
Output capacitance [DQ0~DQ3]	C_{OUT}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 1,2)
Test condition : Vcc=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.0/0.8V

Parameter	Symbol	- 6		- 7		- 8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	110		130		150		ns	
Read-modify-write cycle time	tRWC	155		175		195		ns	
Access time from $\overline{RAS}$	tRAC		60		70		80	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		15		20		20	ns	3,4,5
Access time from column address	tAA		30		35		40	ns	3,9
$\overline{CAS}$ to output in Low-Z	tCLZ	0		0		0		ns	3
Output buffer turn-off delay	tOFF	0	15	0	20	0	20	ns	6
Transition time (rise and fall)	tT	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	tRP	40		50		60		ns	
$\overline{RAS}$ pulse width	tRAS	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ hold time	tRSH	15		20		20		ns	
$\overline{CAS}$ hold time	tCSH	60		70		80		ns	
$\overline{CAS}$ pulse width	tCAS	15	10K	20	10K	20	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	30	15	35	15	40	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	
Column address hold time	tCAH	15		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	tAR	50		55		60		ns	11
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		ns	8
Write command hold time	tWCH	10		10		10		ns	
Write command hold time referenced to $\overline{RAS}$	tWCR	45		50		55		ns	11
Write command pulse width	tWP	10		10		10		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		15		15		ns	
Write command to $\overline{CAS}$ lead time	tCWL	15		15		15		ns	

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 2)

Parameter	Symbol	-6 Min	-6 Max	-7 Min	-7 Max	-8 Min	-8 Max	Units	Notes
Data set-up time	tDS	0		0		0		ns	9
Data hold time	tDH	15		15		15		ns	9
Data hold time referenced to $\overline{RAS}$	tDHR	50		55		60		ns	11
Refresh period(Normal)	tREF		8		8		8	ms	
Refresh period(L -ver)	tREF		128		128		128	ms	
Write command set-up time	tWCS	0		0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	40		45		45		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	85		95		105		ns	7
Column address to $\overline{W}$ delay time	tAWD	55		60		65		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	60		65		70		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	5		5		5		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	15		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		ns	
$\overline{CAS}$ precharge time($\overline{CBR}$ counter test cycle)	tCPT	20		25		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		35		35		40	ns	3
Fast Page mode cycle time	tPC	40		45		50		ns	
Fast Page mode read-modify-write cycle time	tPRWC	80		85		90		ns	
$\overline{CAS}$ precharge time (Fast page cycle)	tCP	10		10		10		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	60	100K	70	100K	80	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	40		45		50		ns	
$\overline{OE}$ access time	tOEA		15		20		20	ns	
$\overline{OE}$ to data delay	tOED	15		20		20		ns	
Output buffer turn off delay time from $\overline{OE}$	tOEZ	0	15	0	20	0	20	ns	
$\overline{OE}$ command hold time	tOEH	15		20		20		ns	

NOTES

1. An initial pause of 200μs is required after power up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD(max) is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS≥tWCS(min),the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
11. tAR, tWCR, and tDHR are referenced to tRAD(MAX).

4M DRAM

- KM41C4000C
  KM41V4000C
- KM41C4002C
- KM44C1000C
  KM44V1000C
- KM44C1002C
- KM44C1003C
- KM44C1004C
  KM44V1004C
- KM44C1010C
- KM48C512B
  KM48V512B
- KM48C514B
  KM48V514B
- KM49C512B
- KM416C256B
  KM416V256B
- KM416C254B
  KM416V254B
- KM418C256B

4M x 1 Bit CMOS Dynamic RAM with Fast Page Mode

DESCRIPTION

This is a family of 4,194,304 x 1 bit Fast Page Mode CMOS DRAMs. Fast Page Mode offers high speed random access of memory cells within the same row. Power supply voltage (+5.0V or +3.3V), access time(-5, -6, -7 or -8), power consumption (Normal, Low power), and package type (SOJ, ZIP, TSOP-II) are optional features of this family. All of this family have $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$-only refresh and Hidden refresh capabilities. Further more, self-refresh operation is available in Low power version.
This 4Mx1 Fast Page Mode DRAM Family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability. It may be used as main memory for main frames, mini computers, personal computer and high performance microprocessor systems.

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FEATURES

- Part Identification
  - KM41C4000C/CL(5V)
  - KM41V4000C/CL(3.3V)

- Active Power Dissipation Unit : mW

Speed	3.3V	5V
-5	-	470
-6	220	415
-7	200	360
-8	180	305

- Refresh cycles

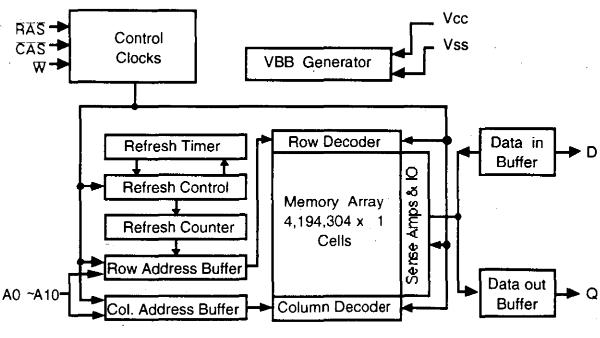
	Vcc	Refresh cycle	Refresh time	
			Normal	L
C1000C	5V	1K	16ms	128ms
V1000C	3.3V			

- Performance range:

Speed	tRAC	tCAC	tRC	tPC	Remark
-5	50ns	13ns	90ns	35ns	5V Only
-6	60ns	15ns	110ns	40ns	5V/3.3V
-7	70ns	20ns	130ns	45ns	5V/3.3V
-8	80ns	20ns	150ns	50ns	5V/3.3V

- Fast Page Mode operation
- $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh capability
- $\overline{\text{RAS}}$-only and Hidden refresh capability
- Self-refresh capability (3.3V,L-ver only)
- Fast parallel test mode capability
- TTL(5V)/LVTTL(3.3V) compatible inputs and outputs
- Common I/O using early write
- JEDEC Standard pinout
- Available in Plastic SOJ, ZIP, TSOP(II) packages
- Single +5V±10% power supply(5V product)
- Single +3.3V±0.3V power supply(3.3V product)

FUNCTIONAL BLOCK DIAGRAM



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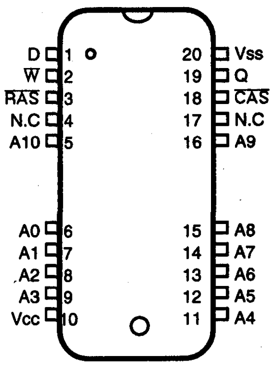
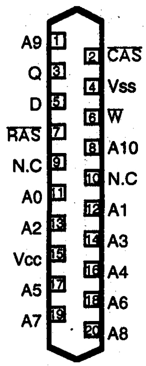
PIN CONFIGURATION (Top Views)

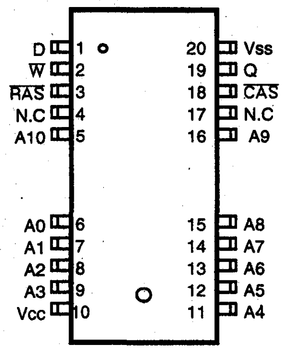
• KM41C/V4000CJ



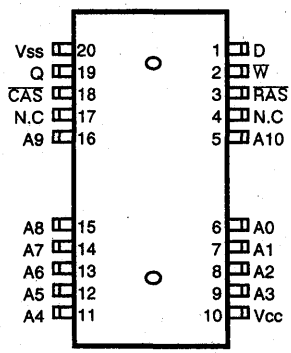
• KM41C/V4000CZ



• KM41C/V4000CT



• KM41C/V4000CTR



Pin Name	Pin Function
A0 - A10	Address Inputs
D	Data In
Q	Data Out
Vss	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
N.C	No Connection
Vcc	Power(+5.0V)
	Power(+3.3V)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Units
		3.3V	5V	
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to +4.6	-1 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.5 to +4.6	-1 to +7.0	V
Storage temperature	Tstg	-55 to +150	-55 to +150	°C
Power dissipation	P_D	600	600	mW
Short circuit output current	I_{OS}	50	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A= 0 to 70 °C)

Parameter	Symbol	3.3V			5V			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply voltage	V_{CC}	3.0	3.3	3.6	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	0	0	0	V
Input high voltage	V_{IH}	2.0	-	Vcc+0.3*1	2.4	-	Vcc+1*1	V
Input low voltage	V_{IL}	-0.3*2	-	0.8	-1.0*2	-	0.8	V

*1 : Vcc+1.3V/15ns(3.3V),Vcc+2.0V/20ns(5V), Pulse width is measured at Vcc

*2 : -1.3V/15ns(3.3V), -2.0V/20ns(5V),Pulse width is measured atVss

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

	Parameter	Symbol	Min	Max	Units
3.3V	Input leakage current (Any input 0≤V_{IN}≤Vcc+0.3V , all other pins not under test=0 volts.)	$I_{I(L)}$	-5	5	μA
	Output leakage current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	-5	5	μA
	Output high voltage level(I_{OH}=-2mA)	V_{OH}	2.4	-	V
	Output low voltage level(I_{OL}=2mA)	V_{OL}	-	0.4	V
5V	Input leakage current (Any input 0≤V_{IN}≤Vcc+0.5V all other pins not under test=0 volts.)	$I_{I(L)}$	-5	5	μA
	Output leakage current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	-5	5	μA
	Output high voltage level(I_{OH}=-5mA)	V_{OH}	2.4	-	V
	Output low voltage level(I_{OL}=4.2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Symbol	Power	Speed	Max		Units
			KM41V4000C	KM41C4000C	
Icc1	Don't care	-5 -6 -7 -8	- 60 55 50	85 75 65 55	mA mA mA mA
Icc2	Don't care	Don't care	1	2	mA
Icc3	Don't care	-5 -6 -7 -8	- 60 55 50	85 75 65 55	mA mA mA mA
Icc4	Don't care	-5 -6 -7 -8	- 45 40 35	65 55 45 35	mA mA mA mA
Icc5	Normal L	Don't care	0.5 100	1 200	mA µA
Icc6	Don't care	-5 -6 -7 -8	- 60 55 50	85 75 65 55	mA mA mA mA
Icc7	L	Don't care	200	300	µA
Iccs	L	Don't care	150	-	µA

Icc1 *: Operating current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

Icc2 : Standby current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

Icc3 *: $\overline{RAS}$-only refresh current ($\overline{CAS}$=V_{IH}, $\overline{RAS}$,Address cycling @tRC=min.)

Icc4 *: Fast Page Mode current ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address cycling @tPC=min.)

Icc5 : Standby current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

Icc6 *: $\overline{CAS}$-before-$\overline{RAS}$ refresh current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

Icc7 : Battery back-up current, Average power supply current, Battery back-up mode
Input high voltage(V_{IH})=Vcc-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{CAS}$=0.2V
D_{IN} = Don't care, T_{RC}= 125µs(L-ver), T_{RAS}=T_{RAS}min~300 ns

Iccs : Self refresh current
$\overline{RAS}$=$\overline{CAS}$=V_{IL}, $\overline{W}$=$\overline{OE}$=A0 ~ A10= D= Vcc-0.2V or 0.2V

* NOTE : Icc1, Icc3, Icc4 and Icc6 are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In Icc1, Icc3, and Icc6, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In Icc4, Address can be changed maximum once within one fast page mode cycle time tPC.

CAPACITANCE(T_A=25°C,Vcc=5V or 3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [D]	C_{IN1}	-	5	pF
Input capacitance [A0 - A10]	C_{IN2}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$]	C_{IN3}	-	7	pF
Output capacitance [Q]	C_{OUT}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 1,2)
Test condition(5V device) : Vcc=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.4/0.4V
Test condition(3.3V device) : Vcc=3.3V±0.3V, V_{ih}/V_{il}=2.0/0.8V, V_{oh}/V_{ol}=2.0/0.8V

Parameter	Symbol	-5 *1		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		130		150		ns	
Read-modify-write cycle time	tRWC	108		130		155		175		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70		80	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		13		15		20		20	ns	3,4,5
Access time from column address	tAA		25		30		35		40	ns	3,10
$\overline{CAS}$ to output in Low-Z	tCLZ	0		0		0		0		ns	3
Output buffer turn-off delay	tOFF	0	13	0	15	0	20	0	20	ns	6
Transition time (rise and fall)	tT	3	50	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		60		ns	
$\overline{RAS}$ pulse width	tRAS	50	10K	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ hold time	tRSH	13		15		20		20		ns	
$\overline{CAS}$ hold time	tCSH	50		60		70		80		ns	
$\overline{CAS}$ pulse width	tCAS	13	10K	15	10K	20	10K	20	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	35	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	15	40	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	
Column address hold time	tCAH	10		10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	tAR	40		45		55		60		ns	15
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		0		ns	8
Write command hold time	tWCH	10		10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	tWCR	40		45		55		60		ns	15
Write command pulse width	tWP	10		10		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	13		15		20		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	13		15		20		20		ns	

Note) *1 : 5V only

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AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 2)

Parameter	Symbol	-5*1		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		0		ns	9
Data hold time	tDH	10		10		15		15		ns	9
Data hold time referenced to $\overline{RAS}$	tDHR	40		45		55		60		ns	15
Refresh period(Normal)	tREF		16		16		16		16	ms	
Refresh period(L-ver)	tREF		128		128		128		128	ms	
Write command set-up time	tWCS	0		0		0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	13		15		20		20		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	50		60		70		80		ns	7
Column address to $\overline{W}$ delay time	tAWD	25		30		35		40		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	30		35		40		45		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	10		10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		5		ns	
$\overline{CAS}$ precharge time($\overline{CBR}$ counter test cycle)	tCPT	20		20		25		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		30		35		40		45	ns	3
Fast Page mode cycle time	tPC	35		40		45		50		ns	
Fast Page mode read-modify-write cycle time	tPRWC	53		60		70		75		ns	
$\overline{CAS}$ precharge time (Fast page cycle)	tCP	10		10		10		10		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	50	200K	60	200K	70	200K	80	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		45		ns	
Write command set-up time(Test mode in)	tWTS	10		10		10		10		ns	
Write command hold time(Test mode in)	tWTH	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		10		ns	
$\overline{RAS}$ pulse width($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		100		µs	14
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	90		110		130		150		ns	14
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		-50		ns	14

Note) *1 : 5V only

TEST MODE CYCLE

(Note. 11)

Parameter	Symbol	-5*1		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	95		115		135		155		ns	
Read-modify-write cycle time	tRWC	113		135		160		180		ns	
Access time from $\overline{RAS}$	tRAC		55		65		75		85	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		18		20		25		25	ns	3,4,5
Access time from column address	tAA		30		35		40		45	ns	3,10
$\overline{RAS}$ pulse width	tRAS	55	10K	65	10K	75	10K	85	10K	ns	
$\overline{CAS}$ pulse width	tCAS	18	10K	20	10K	25	10K	25	10K	ns	
$\overline{RAS}$ hold time	tRSH	18		20		25		25		ns	
$\overline{CAS}$ hold time	tCSH	55		65		75		85		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		45		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	18		20		25		25		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	55		65		75		85		ns	7
Column address to $\overline{W}$ delay time	tAWD	30		35		40		45		ns	7
Fast Page mode cycle time	tPC	40		45		50		55		ns	
Fast page mode read-modify-write cycle time	tPRWC	58		65		75		80		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	55	200K	65	200K	75	200K	85	200K	ns	
Access time form $\overline{CAS}$ precharge	tCPA		35		40		45		50	ns	3

Note) *1 : 5V only

2

NOTES

1. An initial pause of 200μs is required after power up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL(5V device)/1 TTL(3.3V device) loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD(max) is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS≥tWCS(min),the cycles is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-modify-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
11. These specifications are applied in the test mode.
12. In test mode read cycle, the value of tRAC, tAA, tCAC is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
13. tOFF(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
14. 1024cycles of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.(3.3V L-ver.)
15. tAR , tWCR, tDHR are referenced to tRAD(max.).

4M x 1 Bit CMOS Dynamic RAM with Static Column Mode

DESCRIPTION

This is a family of 4,194,304 x 1 bit Static Column Mode CMOS DRAMs. Static Column Mode offers high speed random or sequential access of memory cells within the same row. Access time(-5, -6, -7 or -8) and package type (SOJ , ZIP, TSOP-II) are optional features of this family.
All of this family have $\overline{CS}$-before-$\overline{RAS}$ Refresh, $\overline{RAS}$-only refresh and Hidden Refresh capabilities.
This 4Mx1 Static Column Mode DRAM Family is fabricated using Samsung's advanced CMOS process to realize high band-width and high reliability. It may be used as main memory for main frames, mini computers and high performance microprocessor systems.

2

FEATURES

- Part Identification
  - KM41C4002C

- Active Power Dissipation

Unit : mW

Speed	Active power dissipation
-5	470
-6	415
-7	360
-8	305

- Refresh cycles

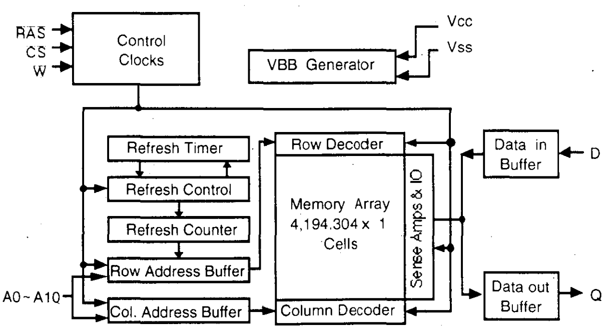
	Vcc	Refresh cycle	Refresh Period
C4002C	5V	1K	16ms

- Performance range:

Speed	tRAC	tCAC	tRC	tSC
-5	50ns	13ns	90ns	30ns
-6	60ns	15ns	110ns	35ns
-7	70ns	20ns	130ns	40ns
-8	80ns	20ns	150ns	45ns

- Static Column Mode operation
- $\overline{CS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- Fast parallel test mode capability
- TTL compatible inputs and outputs
- Common I/O using Early Write
- JEDEC Standard pinout
- Available in Plastic SOJ, ZIP, TSOP(II) packages
- Single +5V±10% power supply

FUNCTIONAL BLOCK DIAGRAM



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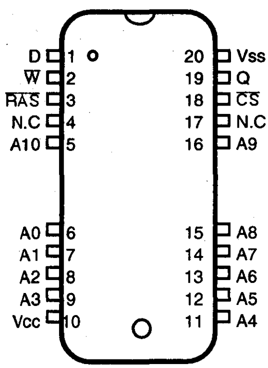
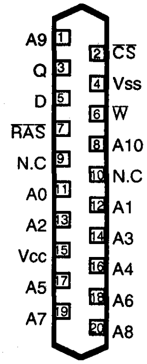
PIN CONFIGURATION (Top Views)

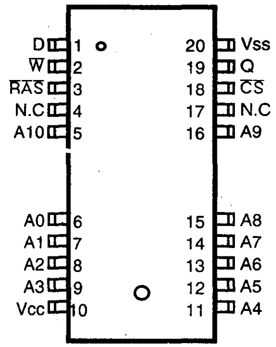
• **KM41C4002CJ**



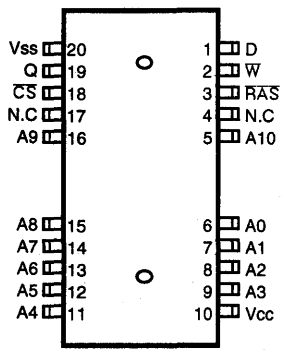
• **KM41C4002CZ**



• **KM41C4002CT**



• **KM41C4002CTR**



Pin Name	Pin Function
A0 - A10	Address Inputs
D	Data In
Q	Data Out
Vss	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Chip select input
$\overline{W}$	Read/Write Input
N.C	No Connection
Vcc	Power(+5.0V)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-1 to +7.0	V
Storage temperature	Tstg	-55 to +150	°C
Power dissipation	P_D	600	mW
Short circuit output current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to Vss, T_A= 0 to 70 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input high voltage	V_{IH}	2.4	-	Vcc+1.0 *1	V
Input low voltage	V_{IL}	-1.0 *2	-	0.8	V

*1 : Vcc+2.0V/20ns(5V), Pulse width is measured at Vcc

*2 : -2.0V/20ns(5V),Pulse width is measured atVss

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Units
Input leakage current (Any input $0 \le V_{IN} \le V_{CC}+0.5V$ all other pins not under test=0 volts.)	$I_{I(L)}$	-5	5	μA
Output leakage current (Data out is disabled, $0V \le V_{OUT} \le V_{CC}$)	$I_{O(L)}$	-5	5	μA
Output high voltage level(I_{OH}=-5mA)	V_{OH}	2.4	-	V
Output low voltage level(I_{OL}=4.2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Symbol	Power	Speed	Max	Units
			KM41C4002C	
I_{CC1}	Don't care	-5 -6 -7 -8	85 75 65 55	mA mA mA mA
I_{CC2}	Normal	Don't care	2	mA
I_{CC3}	Don't care	-5 -6 -7 -8	85 75 65 55	mA mA mA mA
I_{CC4}	Don't care	-5 -6 -7 -8	65 55 45 35	mA mA mA mA
I_{CC5}	Normal	Don't care	1	mA
I_{CC6}	Don't care	-5 -6 -7 -8	85 75 65 55	mA mA mA mA

I_{CC1} *: Operating current ($\overline{RAS}$ and $\overline{CS}$ cycling @tRC=min.)

I_{CC2} : Standby current ($\overline{RAS}$=$\overline{CS}$=$\overline{W}$=V_{IH})

I_{CC3} *: $\overline{RAS}$-only refresh current ($\overline{CS}$=V_{IH}, $\overline{RAS}$,Address cycling @tRC=min.)

I_{CC4} *: Static column Mode current ($\overline{RAS}$=V_{IL}, $\overline{CS}$, Address cycling @tSC=min.)

I_{CC5} : Standby current ($\overline{RAS}$=$\overline{CS}$=$\overline{W}$=V_{CC}-0.2V)

I_{CC6} *: $\overline{CS}$-before-$\overline{RAS}$ refresh current ($\overline{RAS}$ and $\overline{CS}$ cycling @tRC=min.)

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1}, I_{CC3}, and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once during a Static Column mode cycle time tSC.

CAPACITANCE(T_A=25°C,Vcc=5V , f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [D]	C_{IN1}	-	5	pF
Input capacitance [A0 - A10]	C_{IN2}	-	5	pF
Input capacitance [$\overline{\text{RAS}}$, $\overline{\text{CS}}$, $\overline{\text{W}}$]	C_{IN3}	-	7	pF
Output Capacitance [Q]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, Vcc=5.0V±10%, See note 1,2)
Test condition : Vcc=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.4/0.4V

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		130		150		ns	
Read-modify-write cycle time	tRWC	108		130		150		170		ns	
Access time from $\overline{\text{RAS}}$	tRAC		50		60		70		80	ns	3,4,10
Access time from $\overline{\text{CS}}$	tCAC		13		15		20		20	ns	3,4,5
Access time from column address	tAA		25		30		35		40	ns	3,10
Access time from last write	tALW		50		55		65		75	ns	3
$\overline{\text{CS}}$ to output in Low-Z	tCLZ	0		0		0		0		ns	6
Output buffer turn-off delay from $\overline{\text{CS}}$	tOFF	0	13	0	15	0	20	0	20	ns	2
Transition time (rise and fall)	tT	3	50	3	50	3	50	3	50	ns	
$\overline{\text{RAS}}$ precharge time	tRP	30		40		50		60		ns	
$\overline{\text{RAS}}$ pulse width	tRAS	50	10K	60	10K	70	10K	80	10K	ns	
$\overline{\text{RAS}}$ hold time	tRSH	13		15		20		20		ns	
$\overline{\text{CS}}$ hold time	tCSH	50		60		70		80		ns	
$\overline{\text{CS}}$ pulse width	tCS	13	10K	15	10K	20	10K	20	10K	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CS}}$ delay time	tRCD	20	37	20	45	20	50	20	60	ns	4
$\overline{\text{RAS}}$ to column address delay time	tRAD	15	25	15	30	15	35	15	40	ns	10
$\overline{\text{CS}}$ to $\overline{\text{RAS}}$ precharge time	tCRP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	
Column address hold time	tCAH	10		10		15		15		ns	
Column address hold time referenced to $\overline{\text{RAS}}$	tAR	40		45		55		60		ns	13
Column address to $\overline{\text{RAS}}$ lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{\text{CS}}$	tRCH	0		0		0		0		ns	8
Read command hold time referenced to $\overline{\text{RAS}}$	tRRH	0		0		0		0		ns	8
Write command hold time	tWCH	10		15		15		15		ns	
Write command hold time referenced to $\overline{\text{RAS}}$	tWCR	40		45		55		60		ns	13
Write command pulse width	tWP	10		15		15		15		ns	
Write command to $\overline{\text{RAS}}$ lead time	tRWL	15		15		20		20		ns	
Write command to $\overline{\text{CS}}$ lead time	tCWL	13		15		20		20		ns	
Data set-up time	tDS	0		0		0		0		ns	9

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 1, 2)

Parameter	Symbol	-5 Min	-5 Max	-6 Min	-6 Max	-7 Min	-7 Max	-8 Min	-8 Max	Units	Notes
Data hold time	tDH	10		10		15		15		ns	9
Data hold time referenced to $\overline{RAS}$	tDHR	40		45		55		60		ns	12
Refresh period(1024cycles)	tREF		16		16		16		16	ms	
Write command set-up time	tWCS	0		0		0		0		ns	7
$\overline{CS}$ to $\overline{W}$ delay time	tCWD	13		15		15		15		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	50		60		70		80		ns	7
Column address to $\overline{W}$ delay time	tAWD	25		30		35		40		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	30		35		40		45		ns	
$\overline{CS}$ set-up time ($\overline{CS}$-before-$\overline{RAS}$ refresh)	tCSR	10		10		10		10		ns	
$\overline{CS}$ hold time ($\overline{CS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		10		10		ns	
$\overline{RAS}$ to $\overline{CS}$ precharge time	tRPC	5		5		5		5		ns	
$\overline{CS}$ precharge time($\overline{C}$-B-$\overline{R}$ counter test cycle)	tCPT	20		20		25		30		ns	
Static Column mode cycle time	tSC	30		35		40		45		ns	
Static Column mode read-modify-write cycle time	tSRWC	53		65		75		85	75	ns	
Access time from last write	tALW		50		55		65			ns	3,11
Output data hold time from column address	tAOH	5		5		5		5	55	ns	
Output data enable time from $\overline{W}$	tOW		35		40		45			ns	
Output data hold time from $\overline{W}$	tWOH	0		0		0		0		ns	
$\overline{CS}$ precharge time (Static Column cycle)	tCP	10		10		10		10	100K	ns	
$\overline{RAS}$ pulse width (Static Column cycle)	tRASC	50	100K	60	100K	70	100K	80	10K	ns	
$\overline{CS}$ pulth width (Static Column cycle)	tCSC	13	10K	15	10K	20	10K	20		ns	
Column address hold time referenced to $\overline{RAS}$ rising	tAH	5		5		5		5	40	ns	
Last write to column address delay time	tLWAD	20	25	20	30	25	35	25		ns	11
Last write to column address hold time	tAHLW	50		55		65		75		ns	
Write command inactive time	tWI	10		10		10		10		ns	
Write command set-up time(Test mode in)	tWTS	10		10		10		10		ns	
Write command hold time(Test mode in)	tWTH	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		10		ns	

TEST MODE CYCLE

(Note. 12)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	95		115		135		155		ns	
Read-modify-write cycle time	tRWC	113		135		155		175		ns	
Access time from $\overline{RAS}$	tRAC		55		65		75		85	ns	3,4,10
Access time from $\overline{CS}$	tCAC		18		20		25		25	ns	3,4,5
Access time from column address	tAA		30		35		40		45	ns	3,10
$\overline{RAS}$ pulse width	tRAS	55	10K	65	10K	75	10K	85	10K	ns	
$\overline{CS}$ pulse width	tCS	18	10K	20	10K	25	10K	25	10K	ns	
$\overline{RAS}$ hold time	tRSH	18		20		25		25		ns	
$\overline{CS}$ hold time	tCSH	55		65		75		85		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		45		ns	
$\overline{CS}$ to $\overline{W}$ delay time	tCWD	18		20		20		20		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	55		65		75		85		ns	7
Column address to $\overline{W}$ delay time	tAWD	30		35		40		45		ns	7
Static Column mode cycle time	tSC	35		40		45		50		ns	
Static Column mode read-modify-write cycle time	tSRWC	58		70		80		90		ns	
$\overline{RAS}$ pulse width (Static Column cycle)	tRASC	55	100K	65	100K	75	100K	85	100K	ns	
Access time form last write	tALW		55		65		75		85	ns	3,11
$\overline{CS}$ pulse width(static column cycle)	tCSC	18	100K	20	100K	25	100K	25	100K	ns	

NOTES

1. An initial pause of 200μs is required after power up followed by any 8 $\overline{CBR}$ or $\overline{ROR}$ cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD(max) is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS≥tWCS(min),the cycles is an early write cycle and the data output will remain high imped-ance for theduration of the cycle. If tCWD≥ tCWD(min), tRWD≥tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
11. Operation within the tLWAD(max) limit insures that tALW(max) can be met. tLWAD(max) is specified as a reference point only. If tLWAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
12. These specifications are applied in the test mode.
13. tAR , tWCR , tDHR are referenced to tRAD(max).

1M x 4 Bit CMOS Dynamic RAM with Fast Page Mode

DESCRIPTION

This is a family of 1,048,576 x 4 bit Fast Page Mode CMOS DRAMs. Fast Page Mode offers high speed random access of memory cells within the same row. Power supply voltage (+5.0V or +3.3V), access time(-5, -6, -7 or -8), power consumption (Normal or Low power) , and package type (SOJ , DIP, ZIP or TSOP-II) are optional features of this family. All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities. Further more, self-refresh operation is available in 3.3V Low power version.
This 1Mx4 Fast Page Mode DRAM Family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability. It may be used as main memory for main frames and mini computers, personal computer and high performance microprocessor systems.

2

FEATURES

- Part Identification
  - KM44C1000C/CL(5V)
  - KM44V1000C/CL(3.3V)

- Active Power Dissipation

Unit : mW

Speed	3.3V	5V
-5	-	470
-6	220	415
-7	200	360
-8	180	305

- Refresh cycles

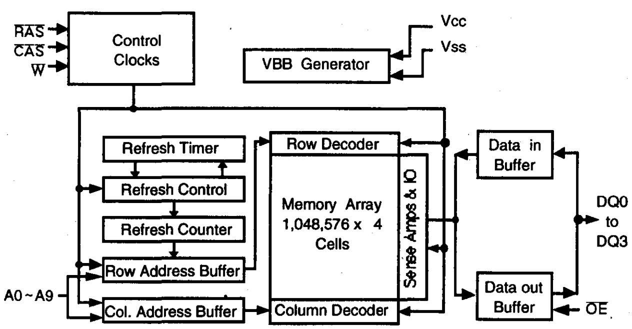
	Vcc	Refresh cycle	Refresh time	
			Normal	L
C1000C	5V	1K	16ms	128ms
V1000C	3.3V	1K	16ms	128ms

- Performance range:

Speed	tRAC	tCAC	tRC	tPC	Remark
-5	50ns	13ns	90ns	35ns	5V Only
-6	60ns	15ns	110ns	40ns	5V/3.3V
-7	70ns	20ns	130ns	45ns	5V/3.3V
-8	80ns	20ns	150ns	50ns	5V/3.3V

- Fast Page Mode operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- Self-refresh capability (3.3V,L-ver only)
- Fast parallel test mode capability
- TTL(5V)/LVTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC Standard pinout
- Available in Plastic SOJ, ZIP, DIP,TSOP(II) packages
- Single +5V±10% power supply(5V product)
- Single +3.3V±0.3V power supply(3.3V product)

FUNCTIONAL BLOCK DIAGRAM



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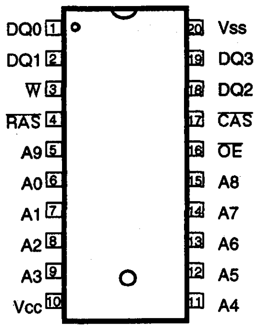
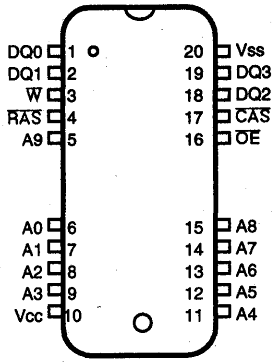
PIN CONFIGURATION (Top Views)

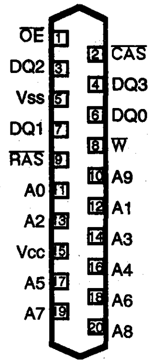
• KM44C/V1000CP



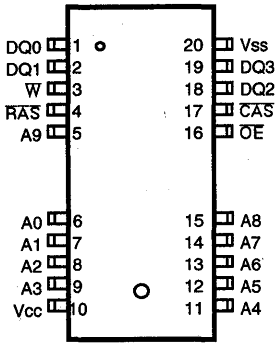
• KM44C/V1000CJ



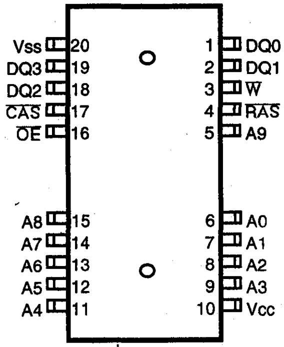
• KM44C/V1000CZ



• KM44C/V1000CT



• KM44C/V1000CTR



Pin Name	Pin Function
A0 - A9	Address Inputs
DQ0 -3	Data In/Out
V_{SS}	Ground
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{W}}$	Read/Write Input
$\overline{\text{OE}}$	Data Outputs Enable
V_{CC}	Power(+5.0V)
	Power(+3.3V)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Units
		3.3V	5V	
Voltage on any pin relative to Vss	V_{IN},V_{OUT}	-0.5 to +4.6	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	V_{CC}	-0.5 to +4.6	-1 to +7.0	V
Storage temperature	Tstg	-55 to +150	-55 to +150	°C
Power dissipation	P_D	600	600	mW
Short circuit output current	I_{OS}	50	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to Vss, T_A= 0 to 70 °C)

Parameter	Symbol	3.3V			5V			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply voltage	V_{CC}	3.0	3.3	3.6	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	0	0	0	V
Input high voltage	V_{IH}	2.0	-	Vcc+0.3*1	2.4	-	Vcc+1.0*1	V
Input low voltage	V_{IL}	-0.3*2	-	0.8	-1.0*2	-	0.8	V

*1 : Vcc+1.3V/15ns(3.3V),Vcc+2.0V/20ns(5V), Pulse width is measured at Vcc

*2 : -1.3V/15ns(3.3V), -2.0V/20ns(5V),Pulse width is measured atVss

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

	Parameter	Symbol	Min	Max	Units
3.3V	Input leakage current (Any input 0≤V_{IN}≤Vcc+0.3V, all other pins not under test=0 volts.)	$I_{I(L)}$	-5	5	μA
	Output leakage current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	-5	5	μA
	Output high voltage level(I_{OH}=-2mA)	V_{OH}	2.4	-	V
	Output low voltage level(I_{OL}=2mA)	V_{OL}	-	0.4	V
5V	Input leakage current (Any input 0≤V_{IN}≤Vcc+0.5V all other pins not under test=0 volts.)	$I_{I(L)}$	-5	5	μA
	Output leakage current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	-5	5	μA
	Output high voltage level(I_{OH}=-5mA)	V_{OH}	2.4	-	V
	Output low voltage level(I_{OL}=4.2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Symbol	Power	Speed	Max		Units
			KM44V1000C	KM44C1000C	
I_{CC1}	Don't care	-5 -6 -7 -8	- 60 55 50	85 75 65 55	mA mA mA mA
I_{CC2}	Don't care	Don't care	1	2	mA
I_{CC3}	Don't care	-5 -6 -7 -8	- 60 55 50	85 75 65 55	mA mA mA mA
I_{CC4}	Don't care	-5 -6 -7 -8	- 45 40 35	65 55 45 35	mA mA mA mA
I_{CC5}	Normal L	Don't care	0.5 100	1 200	mA µA
I_{CC6}	Don't care	-5 -6 -7 -8	- 60 55 50	85 75 65 55	mA mA mA mA
I_{CC7}	L	Don't care	200	300	µA
I_{CCS}	L	Don't care	150	-	µA

I_{CC1} *: Operating current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC2} : Standby current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3} *: $\overline{RAS}$-only refresh current ($\overline{CAS}$=V_{IH}, $\overline{RAS}$,Address cycling @tRC=min.)

I_{CC4} *: Fast Page Mode current ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address cycling @tPC=min.)

I_{CC5} : Standby current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)

I_{CC6} *: $\overline{CAS}$-before-$\overline{RAS}$ refresh current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode
Input high voltage(V_{IH})=V_{CC}-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{CAS}$=0.2V
$DQ_{0\text{-}3}$ = Don't care, T_{RC}= 125µs(L-ver) ,T_{RAS}=T_{RAS}min~300 ns

I_{CCS} : Self refresh current
$\overline{RAS}$=$\overline{CAS}$=V_{IL}, $\overline{W}$=$\overline{OE}$=A0 ~ A9= V_{CC}-0.2V or 0.2V,
DQ0 ~ DQ3= V_{CC}-0.2V, 0.2V or OPEN

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1}, I_{CC3} and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one fast page mode cycle time tPC.

CAPACITANCE(T_A=25°C,Vcc=5V or 3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A9]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output capacitance [DQ0 - DQ3]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 1,2)
Test condition(5V device) : Vcc=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.4/0.4V
Test condition(3.3V device) : Vcc=3.3V±0.3V, V_{ih}/V_{il}=2.0/0.8V, V_{oh}/V_{ol}=2.0/0.8V

Parameter	Symbol	-5 *1		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		130		150		ns	
Read-modify-write cycle time	tRWC	133		155		185		205		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70		80	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		13		15		20		20	ns	3,4,5
Access time from column address	tAA		25		30		35		40	ns	3,10
$\overline{CAS}$ to output in Low-Z	tCLZ	0		0		0		0		ns	3
Output buffer turn-off delay	tOFF	0	13	0	15	0	20	0	20	ns	6
Transition time (rise and fall)	tT	3	50	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		60		ns	
$\overline{RAS}$ pulse width	tRAS	50	10K	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ hold time	tRSH	13		15		20		20		ns	
$\overline{CAS}$ hold time	tCSH	50		60		70		80		ns	
$\overline{CAS}$ pulse width	tCAS	13	10K	15	10K	20	10K	20	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	37	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	15	40	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	
Column address hold time	tCAH	10		10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	tAR	40		45		55		60		ns	15
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		0		ns	
Write command hold time	tWCH	10		10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	tWCR	40		45		55		60		ns	15
Write command pulse width	tWP	10		10		15		15		ns	
Write command to $\overline{RAS}$ lead tim	tRWL	15		15		20		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	13		15		20		20		ns	

Note) *1 : 5V only

AC CHARACTERISTICS (0°C≤TA≤70°C, See note 2)

Parameter	Symbol	-5 *1		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		0		ns	9
Data hold time	tDH	10		10		15		15		ns	9
Data hold time referenced to $\overline{RAS}$	tDHR	40		45		55		60		ns	15
Refresh period(Normal)	tREF		16		16		16		16	ms	
Refresh period(L-ver)	tREF		128		128		128	0	128	ms	
Write command set-up time	tWCS	0		0		0		50		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	36		40		50		110		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	73		85		100		70		ns	7
Column address to $\overline{W}$ delay time	tAWD	48		55		65		75		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	53		60		70		10		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	10		10		10		15		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		15		5		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		30		ns	
$\overline{CAS}$ precharge time($\overline{CBR}$ counter test cycle)	tCPT	20		20		25				ns	
Access time from $\overline{CAS}$ precharge	tCPA		30		35		40	50	45	ns	3
Fast Page mode cycle time	tPC	35		40		45		105		ns	
Fast Page mode read-modify-write cycle time	tPRWC	76		85		100		10		ns	
$\overline{CAS}$ precharge time (Fast page cycle)	tCP	10		10		10		80		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	50	200K	60	200K	70	200K	45	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40				ns	
$\overline{OE}$ access time	tOEA		13		15		20	20	20	ns	
$\overline{OE}$ to data delay	tOED	13		15		20		0		ns	
Out put buffer turn off delay time from $\overline{OE}$	tOEZ	0	13	0	15	0	20	20	20	ns	
$\overline{OE}$ command hold time	tOEH	13		15		20		10		ns	
Write command set-up time(Test mode in)	tWTS	10		10		10		10		ns	
Write command hold time(Test mode in)	tWTH	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		100		ns	
$\overline{RAS}$ pulse width($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		150		us	14
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	90		110		130		-50		ns	14
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50				ns	14

Note) *1 : 5V only

TEST MODE CYCLE

(Note. 11)

Parameter	Symbol	-5*1 Min	-5*1 Max	-6 Min	-6 Max	-7 Min	-7 Max	-8 Min	-8 Max	Units	Notes
Random read or write cycle time	tRC	95		115		135		155		ns	
Read-modify-write cycle time	tRWC	138		160		190		210		ns	
Access time from $\overline{RAS}$	tRAC		55		65		75		85	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		18		20		25		25	ns	3,4,5
Access time from column address	tAA		30		35		40		45	ns	3,10
$\overline{RAS}$ pulse width	tRAS	55	10K	65	10K	75	10K	85	10K	ns	
$\overline{CAS}$ pulse width	tCAS	18	10K	20	10K	25	10K	25	10K	ns	
$\overline{RAS}$ hold time	tRSH	18		20		25		25		ns	
$\overline{CAS}$ hold time	tCSH	55		65		75		85		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		45		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	41		45		55		55		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	78		90		105		115		ns	7
Column address to $\overline{W}$ delay time	tAWD	53		60		70		75		ns	7
Fast Page mode cycle time	tPC	40		45		50		55		ns	
Fast page mode read-modify-write cycle time	tPRWC	81		90		105		110		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	55	200K	65	200K	75	200K	85	200K	ns	
Access time form $\overline{CAS}$ precharge	tCPA		35		40		45		50	ns	3
$\overline{OE}$ access time	tOEA		20		20		25		25	ns	
$\overline{OE}$ to data delay	tOED	18		20		25		25		ns	
$\overline{OE}$ command hold time	tOEH	18		20		25		25		ns	

Note) *1 : 5V only

2

NOTES

1. An initial pause of 200µs is required after power up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL(5V device)/1 TTL(3.3V device) loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD(max) is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS≥tWCS(min),the cycles is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-modify-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
11. These specifications are applied in the test mode.
12. In test mode read cycle, the value of tRAC, tAA, tCAC is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
13. tOFF(max) and tOEZ(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
14. 1024cycles of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.(3.3V L-ver.)
15. tAR, tWCR , tDHR are referenced to tRAD(max).

1M x 4 Bit CMOS Dynamic RAM with Static Column Mode

DESCRIPTION

This is a family of 1,048,576 x 4 bit Static Column Mode CMOS DRAMs. Static Column Mode offers high speed random or sequential access of memory cells within the same row. Access time(-5, -6, -7 or -8) and package type (SOJ , DIP, ZIPor TSOP-II) are optional features of this family.
All of this family have $\overline{CS}$-before-$\overline{RAS}$ Refresh, $\overline{RAS}$-only refresh and Hidden Refresh capabilities.
This 1Mx4 Static Column Mode DRAM Family is fabricated using Samsung's advanced CMOS process to realize high band-width and high reliability. It may be used as main memory for main frames and mini computers and high performance microprocessor systems.

FEATURES

- Part Identification
  - KM44C1002C

- Active Power Dissipation

Unit : mW

Speed	Active power dissipation
-5	470
-6	415
-7	360
-8	305

- Refresh cycles

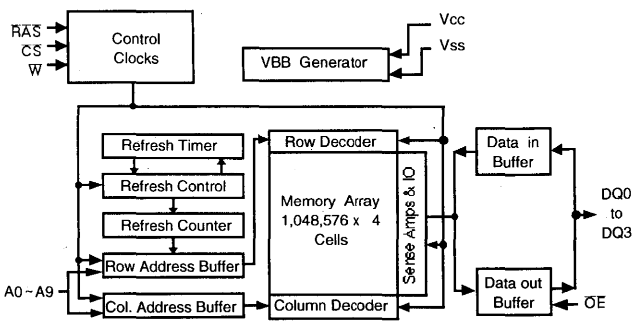
	Vcc	Refresh cycle	Refresh Period
C1002C	5V	1K	16ms

- Performance range:

Speed	tRAC	tCAC	tRC	tSC
-5	50ns	13ns	90ns	30ns
-6	60ns	15ns	110ns	35ns
-7	70ns	20ns	130ns	40ns
-8	80ns	20ns	150ns	45ns

- Static Column Mode operation
- $\overline{CS}$-before-$\overline{RAS}$ refresh capability
- RAS-only and Hidden refresh capability
- Fast parallel test mode capability
- TTL compatible inputs and outputs
- Early Write or Output enable controlled write
- JEDEC Standard pinout
- Available in Plastic SOJ, ZIP, DIP,TSOP(II) packages
- Single +5V±10% power supply

FUNCTIONAL BLOCK DIAGRAM



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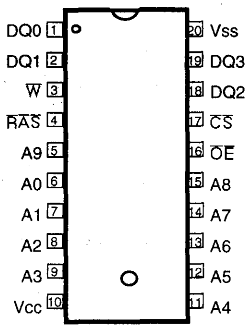
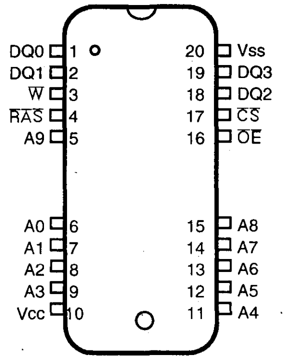
PIN CONFIGURATION (Top Views)

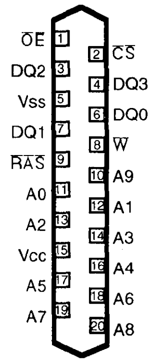
• KM44C1002CP



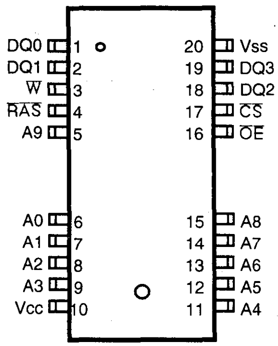
• KM44C1002CJ



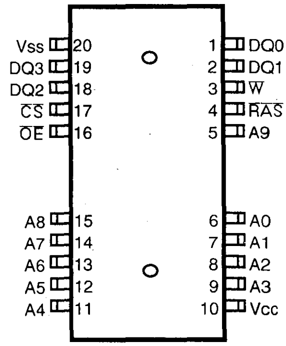
• KM44C1002CZ



• KM44C1002CT



• KM44C1002CTR



Pin Name	Pin Function
A0 - A9	Address Inputs
$\overline{W}$	Read/Write input
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Chip Select Input
DQ0/DQ3	Data In/Out
$\overline{OE}$	Data Outputs Enable
V_{CC}	Power(+5.0V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to Vss	V_{IN},V_{OUT}	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	V_{CC}	-1 to +7.0	V
Storage temperature	Tstg	-55 to +150	°C
Power dissipation	P_D	600	mW
Short circuit output current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to Vss, T_A= 0 to 70 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input high voltage	V_{IH}	2.4	-	Vcc+1.0*1	V
Input low voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : Vcc+2.0V/20ns(5V), Pulse width is measured at Vcc

*2 : -2.0V/20ns(5V),Pulse width is measured atVss

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Units
Input leakage current (Any input $0 \le V_{IN} \le Vcc+0.5V$ all other pins not under test=0 volts.)	$I_{I(L)}$	-5	5	μA
Output leakage current (Data out is disabled, $0V \le V_{OUT} \le Vcc$)	$I_{O(L)}$	-5	5	μA
Output high voltage level(I_{OH}=-5mA)	V_{OH}	2.4	-	V
Output low voltage level(I_{OL}=4.2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Symbol	Power	Speed	Max	Units
			KM44C1002C	
I_{CC1}	Don't care	-5 -6 -7 -8	85 75 65 55	mA mA mA mA
I_{CC2}	Normal	Don't care	2	mA
I_{CC3}	Don't care	-5 -6 -7 -8	85 75 65 55	mA mA mA mA
I_{CC4}	Don't care	-5 -6 -7 -8	65 55 45 35	mA mA mA mA
I_{CC5}	Normal	Don't care	1	mA
I_{CC6}	Don't care	-5 -6 -7 -8	85 75 65 55	mA mA mA mA

I_{CC1} *: Operating current ($\overline{RAS}$ and $\overline{CS}$ cycling @tRC=min.)

I_{CC2} : Standby current ($\overline{RAS}$=$\overline{CS}$=$\overline{W}$=V_{IH})

I_{CC3} *: $\overline{RAS}$-only refresh current ($\overline{CS}$=V_{IH}, $\overline{RAS}$,Address cycling @tRC=min.)

I_{CC4} *: Static Column Mode current ($\overline{RAS}$=V_{IL}, $\overline{CS}$, Address cycling @tSC=min.)

I_{CC5} : Standby current ($\overline{RAS}$=$\overline{CS}$=$\overline{W}$=V_{CC}-0.2V)

I_{CC6} *: $\overline{CS}$-before-$\overline{RAS}$ refresh current ($\overline{RAS}$ and $\overline{CS}$ cycling @tRC=min.)

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} , I_{CC3} and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one Static Column mode cycle time tSC.

CAPACITANCE(T_A=25°C,Vcc=5V , f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A9]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{CS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ0 - DQ3]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, Vcc=5.0V±10%, See note 1,2)
Test condition : Vcc=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.4/0.4V

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		130		150		ns	
Read-modify-write cycle time	tRWC	133		155		185		205		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70		80	ns	3,4,10
Access time from $\overline{CS}$	tCAC		13		15		20		20	ns	3,4,5
Access time from column address	tAA		25		30		35		40	ns	3,10
$\overline{CS}$ to output in Low-Z	tCLZ	0		0		0		0		ns	6
Output buffer turn-off delay from $\overline{CS}$	tOFF	0	13	0	15	0	20	0	20	ns	
Transition time (rise and fall)	tT	3	50	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		60		ns	
$\overline{RAS}$ pulse width	tRAS	50	10K	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ hold time	tRSH	13		15		20		20		ns	
$\overline{CS}$ hold time	tCSH	50		60		70		80		ns	
$\overline{CS}$ pulse width	tCS	13	10K	15	10K	20	10K	20	10K	ns	
$\overline{RAS}$ to $\overline{CS}$ delay time	tRCD	20	37	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	15	40	ns	10
$\overline{CS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	
Column address hold time	tCAH	10		10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	tAR	40		45		55		60		ns	13
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{CS}$	tRCH	0		0		0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		0		ns	8
Write command hold time	tWCH	10		15		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	tWCR	40		45		55		60		ns	13
Write command pulse width	tWP	10		15		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		15		20		20		ns	
Write command to $\overline{CS}$ lead time	tCWL	13		15		20		20		ns	
Data set-up time	tDS	0		0		0		0		ns	9

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AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 1, 2)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Data hold time	tDH	10		15		15		15		ns	9
Data hold time referenced to $\overline{RAS}$	tDHR	40		45		55		60		ns	13
Refresh period(1024cycles)	tREF		16		16		16		16	ms	
Write command set-up time	tWCS	0		0		0		0		ns	7
$\overline{CS}$ to $\overline{W}$ delay time	tCWD	36		40		50		50		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	73		85		100		110		ns	7
Column address to $\overline{W}$ delay time	tAWD	48		55		65		70		ns	7
$\overline{CS}$ set-up time ($\overline{CS}$-before-$\overline{RAS}$ refresh)	tCSR	10		10		10		10		ns	
$\overline{CS}$ hold time ($\overline{CS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		10		10		ns	
$\overline{RAS}$ to $\overline{CS}$ precharge time	tRPC	5		5		5		5		ns	
$\overline{CS}$ precharge time($\overline{C}$-B-$\overline{R}$ counter test cycle)	tCPT	20		20		25		30		ns	
Static Column mode cycle time	tSC	30		35		40		45		ns	
Static Column mode read-modify-write cycle time	tSRWC	80		85		100		110		ns	
Access time from last write	tALW		50		55		65		75	ns	3,11
Output data hold time from column address	tAOH	5		5		5		5		ns	
Output data enable time from $\overline{W}$	tOW		35		40		45		55	ns	
$\overline{CS}$ precharge time (Static Column cycle)	tCP	10		10		10		10		ns	
$\overline{RAS}$ pulse width (Static Column cycle)	tRASC	50	100K	60	100K	70	100K	80	100K	ns	
$\overline{CS}$ pulth width (Static Column cycle)	tCSC	13	10K	15	10K	20	10K	20	10K	ns	
Column address hold time referenced to $\overline{RAS}$ rising	tAH	5		5		5		5		ns	
Last write to column address delay time	tLWAD	20	25	20	25	25	35	25	40	ns	11
Last write to column address hold time	tAHLW	50		60		70		80		ns	
Write command inactive time	tWI	10		10		10		10		ns	
$\overline{OE}$ access time	tOEA		13		15		20		20	ns	
$\overline{OE}$ to data delay	tOED	13		15		20		20		ns	
Out put buffer turn off delay time from $\overline{OE}$	tOEZ	0	13	0	15	0	20	0	20	ns	
$\overline{OE}$ command hold time	tOEH	13		15		15		15		ns	
Write command set-up time(Test mode in)	tWTS	10		10		10		10		ns	
Write command hold time(Test mode in)	tWTH	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		10		ns	

TEST MODE CYCLE

(Note. 12)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	95		115		135		155		ns	
Read-modify-write cycle time	tRWC	138		160		190		210		ns	
Access time from $\overline{RAS}$	tRAC		55		65		75		85	ns	3,4,10
Access time from $\overline{CS}$	tCAC		18		20		25		25	ns	3,4,5
Access time from column address	tAA		30		35		40		45	ns	3,10
$\overline{RAS}$ pulse width	tRAS	55	10K	65	10K	75	10K	85	10K	ns	
$\overline{CS}$ pulse width	tCS	18	10K	20	10K	25	10K	25	10K	ns	
$\overline{RAS}$ hold time	tRSH	18		20		25		25		ns	
$\overline{CS}$ hold time	tCSH	55		65		75		85		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		45		ns	
$\overline{CS}$ to $\overline{W}$ delay time	tCWD	41		45		55		55		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	78		90		105		115		ns	7
Column address to $\overline{W}$ delay time	tAWD	53		60		70		75		ns	7
Static Column mode cycle time	tSC	35		40		45		50		ns	
Static Column mode read-modify-write cycle time	tSRWC	85		90		105		110		ns	
$\overline{RAS}$ pulse width (Static Column cycle)	tRASC	55	100K	65	100K	75	100K	85	100K	ns	
Access time form last write	tALW		55		60		70		80	ns	3,11
$\overline{OE}$ access time	tOEA		18		25		25		30	ns	
$\overline{OE}$ to data delay	tOED	18		20		25		25		ns	
$\overline{OE}$ command hold time	tOEH	18		20		25		25		ns	

NOTES

1. An initial pause of 200μs is required after power up followed by any 8 $\overline{CBR}$ or $\overline{ROR}$ cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD(max) is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS≥tWCS(min),the cycles is an early write cycle and the data output will remain high imped-ance for theduration of the cycle. If tCWD≥ tCWD(min), tRWD≥tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
11. Operation within the tLWAD(max) limit insures that tALW(max) can be met. tLWAD(max) is specified as a reference point only. If tLWAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
12. These specifications are applied in the test mode.
13. tAR , tWCR , tDHR are referenced to tRAD(max).

1M x 4 Bit CMOS Quad CAS DRAM with Fast Page Mode

DESCRIPTION

This is a family of 1,048,576 x 4 bit Fast Page Mode Quad CAS CMOS DRAMs. Fast Page Mode offers high speed random access of memory cells within the same row. Access time(-5, -6, -7 or -8), power consumption (Normal, Low power) , and package type (SOJ or TSOP-II) are optional features of this family. All of this family have $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$-only refresh and Hidden refresh capabilities.
All inputs and outputs are fully TTL compatible and four seperate $\overline{\text{CAS}}$ pins provide for seperate I/O operation allowing this device to operate in parity mode.
This 1Mx4 Fast Page Mode DRAM Family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability.

2

FEATURES

- Part Identification
  - KM44C1003C/CL(5V)

- Active Power Dissipation

Unit : mW

Speed	Active power dissipation
-5	470
-6	415
-7	360
-8	305

- Refresh cycles

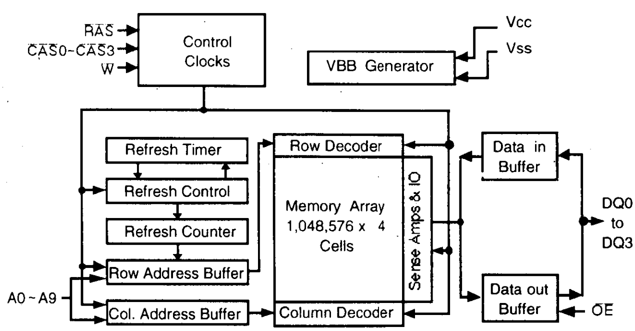
Part NO.	Refresh Cycle	Refresh Period	
		Normal	L
C1003C	1K	16ms	128ms

- Performance range:

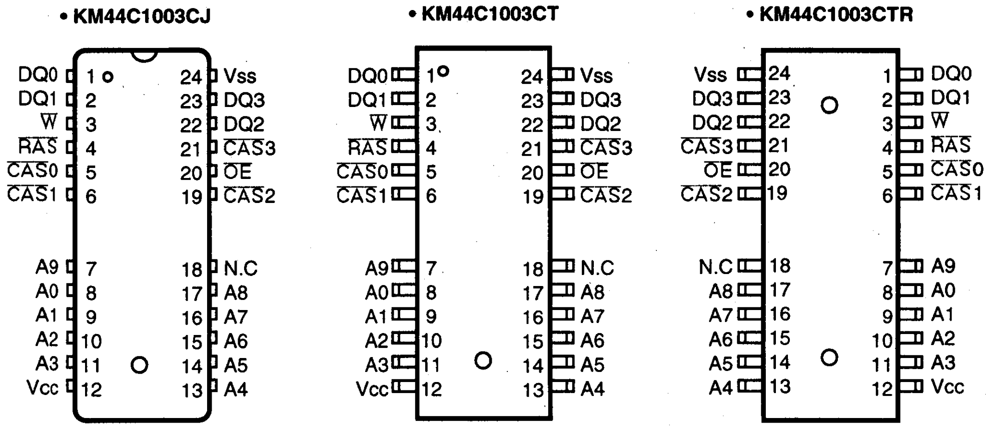
Speed	tRAC	tCAC	tRC	tPC
-5	50ns	13ns	90ns	35ns
-6	60ns	15ns	110ns	40ns
-7	70ns	20ns	130ns	45ns
-8	80ns	20ns	150ns	50ns

- Fast Page Mode operation
- Four seperate $\overline{\text{CAS}}$ pins provide for seperate I/O operation
- $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh capability
- RAS-only and Hidden refresh capability
- Fast parallel test mode capability
- TTL compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC Standard pinout
- Available in Plastic SOJ, TSOP(II) packages
- Single +5V±10% power supply

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top Views)



Pin Name	Pin Function
A0 - A9	Address Inputs
DQ0 -3	Data In/Out
Vss	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS0}$-$\overline{CAS3}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Outputs Enable
Vcc	Power(+5.0V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	V_{CC}	-1 to +7.0	V
Storage temperature	Tstg	-55 to +150	°C
Power dissipation	P_D	600	mW
Short circuit output current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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RECOMMENDED OPERATING CONDITIONS (Voltages referenced to Vss, T_A= 0 to 70 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input high voltage	V_{IH}	2.4	-	Vcc+1.0*1	V
Input low voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : Vcc+2.0V/20ns(5V), Pulse width is measured at Vcc
*2 : -2.0V/20ns(5V),Pulse width is measured at Vss

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Units
Input leakage current (Any input $0 \le V_{IN} \le V_{CC}+0.5V$ all other pins not under test=0 volts.)	$I_{I(L)}$	-5	5	μA
Output leakage current (Data out is disabled, $0V \le V_{OUT} \le V_{CC}$)	$I_{O(L)}$	-5	5	μA
Output high voltage level(I_{OH}=-5mA)	V_{OH}	2.4	-	V
Output low voltage level(I_{OL}=4.2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Symbol	Power	Speed	Max KM44C1003C	Units
I_{CC1}	Don't care	-5 -6 -7 -8	85 75 65 55	mA mA mA mA
I_{CC2}	Normal L	Don't care	2 1	mA mA
I_{CC3}	Don't care	-5 -6 -7 -8	85 75 65 55	mA mA mA mA
I_{CC4}	Don't care	-5 -6 -7 -8	65 55 45 35	mA mA mA mA
I_{CC5}	Normal L	Don't care	1 200	mA µA
I_{CC6}	Don't care	-5 -6 -7 -8	85 75 65 55	mA mA mA mA
I_{CC7}	L	Don't care	300	µA

I_{CC1} *: Operating current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC2} : Standby current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3} *: $\overline{RAS}$-only refresh current ($\overline{CAS}$=V_{IH}, $\overline{RAS}$,Address cycling @tRC=min.)

I_{CC4} *: Fast Page Mode current ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address cycling @tPC=min.)

I_{CC5} : Standby current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)

I_{CC6} *: $\overline{CAS}$-before-$\overline{RAS}$ refresh current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode
Input high voltage(V_{IH})=V_{CC}-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{CAS}$=0.2V
DQ0~3 = Don't care, T_{RC}= 125µs(L-ver), T_{RAS}=T_{RAS}min~300 ns

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1}, I_{CC3}, and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one fast page mode cycle time tPC.

CAPACITANCE(T_A=25°C,Vcc=5V , f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A9]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{CAS0}$-$\overline{CAS3}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output capacitance [DQ0 - DQ3]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 1,2)
Test condition : Vcc=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.4/0.4V

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		130		150		ns	
Read-modify-write cycle time	tRWC	133		155		185		205		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70		80	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		13		15		20		20	ns	3,4,18
Access time from column address	tAA		25		30		35		40	ns	3,10
$\overline{CAS}$ to output in Low-Z	tCLZ	0		0		0		0		ns	3,18
Output buffer turn-off delay	tOFF	0	13	0	15	0	20	0	20	ns	6,18
Transition time (rise and fall)	tT	3	50	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		60		ns	
$\overline{RAS}$ pulse width	tRAS	50	10K	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ hold time	tRSH	13		15		20		20		ns	16
$\overline{CAS}$ hold time	tCSH	50		60		70		80		ns	17
$\overline{CAS}$ pulse width	tCAS	13	10K	15	10K	20	10K	20	10K	ns	23
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	37	20	45	20	50	20	60	ns	4,16
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	15	40	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		5		ns	17
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	16
Column address hold time	tCAH	10		10		15		15		ns	16
Column address hold time referenced to $\overline{RAS}$	tAR	40		45		55		60		ns	
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		40		ns	26
Read command set-up time	tRCS	0		0		0		0		ns	16
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		0		ns	8,17
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		0		ns	8
Write command hold time	tWCH	10		10		15		15		ns	24
Write command hold time referenced to $\overline{RAS}$	tWCR	40		45		55		60		ns	26
Write command pulse width	tWP	10		10		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		15		20		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	13		15		20		20		ns	17

SAMSUNG ELECTRONICS

AC CHARACTERISTICS (0°C≤TA≤70°C, See note 2)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		0		ns	10
Data hold time	tDH	10		10		15		15		ns	10
Data hold time referenced to $\overline{RAS}$	tDHR	40		45		55		60		ns	26
Refresh period(Normal)	tREF		16		16		16		16	ms	
Refresh period(L-ver)	tREF		128		128		128		128	ms	
Write command set-up time	tWCS	0		0		0		0		ns	7,16
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	36		40		50		50		ns	7,16
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	73		85		100		110		ns	7
Column address to $\overline{W}$ delay time	tAWD	48		55		65		70		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	53		60		70		75		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	10		10		10		10		ns	16
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		15		15		ns	17
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		5		ns	
$\overline{CAS}$ precharge time($\overline{CBR}$ counter test cycle)	tCPT	20		20		30		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		30		35		40		45	ns	3,18
Fast Page mode cycle time	tPC	35		40		45		50		ns	19
Fast Page mode read-modify-write cycle time	tPRWC	76		85		100		105		ns	19
$\overline{CAS}$ precharge time (Fast page cycle)	tCP	10		10		10		10		ns	20
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	50	200K	60	200K	70	200K	80	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		45		ns	
$\overline{OE}$ access time	tOEA		13		15		20		20	ns	21
$\overline{OE}$ to data delay	tOED	13		15		20		20		ns	21
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	53		60		70		75		ns	
Out put buffer turn off delay time from $\overline{OE}$	tOEZ	0	13	0	15	0	20	0	20	ns	
$\overline{OE}$ command hold time	tOEH	13		15		20		20		ns	
Write command set-up time(Test mode in)	tWTS	10		10		10		10		ns	
Write command hold time(Test mode in)	tWTH	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	5		5		5		5		ns	
Hold time $\overline{CAS}$ low to $\overline{CAS}$ high	tCLCH	5		5		5		5		ns	14,25

TEST MODE CYCLE

(Note. 11)

Parameter	Symbol	-5 Min	-5 Max	-6 Min	-6 Max	-7 Min	-7 Max	-8 Min	-8 Max	Units	Notes
Random read or write cycle time	tRC	95		115		135		155		ns	
Read-modify-write cycle time	tRWC	138		160		190		210		ns	
Access time from $\overline{RAS}$	tRAC		60		65		75		85	ns	3,4,10,12
Access time from $\overline{CAS}$	tCAC		18		20		25		25	ns	3,4,5,12
Access time from column address	tAA		30		35		40		45	ns	3,10,12
$\overline{RAS}$ pulse width	tRAS	55	10K	65	10K	75	10K	85	10K	ns	
$\overline{CAS}$ pulse width	tCAS	18	10K	20	10K	25	10K	25	10K	ns	
$\overline{RAS}$ hold time	tRSH	18		20		25		25		ns	
$\overline{CAS}$ hold time	tCSH	55		65		75		85		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		45		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	41		45		55		55		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	78		90		105		115		ns	7
Column address to $\overline{W}$ delay time	tAWD	53		60		70		75		ns	7
Fast Page mode cycle time	tPC	40		45		50		55		ns	
Fast page mode read-modify-write cycle time	tPRWC	81		90		105		110		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	55	200K	65	200K	75	200K	85	200K	ns	
Access time form $\overline{CAS}$ precharge	tCPA		35		40		45		50	ns	3
$\overline{OE}$ access time	tOEA		20		20		25		25	ns	
$\overline{OE}$ to data delay	tOED	18		20		25		25		ns	
$\overline{OE}$ command hold time	tOEH	18		20		25		25		ns	

NOTES

1. An initial pause of 200μs is required after power up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD(max) is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS≥tWCS(min),the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
11. These specifications are applied in the test mode.
12. In test mode read cycle, the value of tRAC, tAA, tCAC is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
13. tOFF(max) and tOEZ(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
14. In order to hold the address latched by the first $\overline{CAS}$x going low, the parameter tCLCH must be met.
15. If at least one $\overline{CAS}$ is low at the falling edge of $\overline{RAS}$, DQ will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, all four $\overline{CAS}$ must be pulsed high for tCP.
16. The first $\overline{CAS}$x edge to transition low.
17. The last $\overline{CAS}$x edge to transition low.
18. Output parameter is referenced to corresponding $\overline{CAS}$x input.
19. Last rising $\overline{CAS}$x edge to next cycle's last rising $\overline{CAS}$x edge.
20. Last rising $\overline{CAS}$x edge to first falling $\overline{CAS}$x edge.
21. First DQx controlled by the first $\overline{CAS}$x to go low.
22. Last DQx controlled by the first $\overline{CAS}$x to go low.
23. Each $\overline{CAS}$x must meet minimum pulse width.
24. Last $\overline{CAS}$x to go low.
25. The last falling $\overline{CAS}$x edge to the first rising $\overline{CAS}$x edge
26. tAR,tWCR,tDHR are referenced to tRAD(max).

1M x 4 Bit CMOS Dynamic RAM with Extended Data Out

DESCRIPTION

This is a family of 1,048,576 x 4 bit Extended Data Out CMOS DRAMs. Extended Data Out offers high speed random access of memory cells within the same row. Power supply voltage(+5.0V or +3.3V), access time (-5, -6, -7 or -8), power consumption (Normal or Low power) and package type(SOJ or TSOP-II) are optional features of this family.
All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities.
This 1Mx4 Extended Data Out DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability.
It may be used as main memory unit for microcomputer, personal computer and portable machines.

FEATURES

- Part Identification
  - KM44C1004C/CL (5V)
  - KM44V1004C/CL (3.3V)

- Active Power Dissipation

Unit : mW

Speed	3.3V	5V
-5	-	468
-6	220	413
-7	200	358
-8	180	303

- Refresh cycles

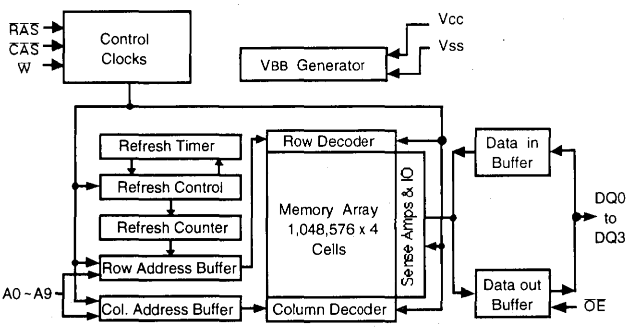
	Vcc	Refresh cycle	Refresh Period	
			Normal	L
C1004C	5V	1K	16ms	128ms
V1004C	3.3V			

- Performance range:

Speed	tRAC	tCAC	tRC	tPC	Remark
-5	50ns	15ns	90ns	35ns	5V Only
-6	60ns	15ns	110ns	40ns	5V/3.3V
-7	70ns	20ns	130ns	45ns	5V/3.3V
-8	80ns	20ns	150ns	50ns	5V/3.3V

- Extended Data Out operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- Self-refresh capability (3.3V,L-ver only)
- TTL(5V)/LVTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC standard pinout
- Available in plastic SOJ ,DIP ,ZIP and TSOP(II) packages
- Single +5V±10% power supply (5V product)
- Single +3.3V±0.3V power supply (3.3V product)

FUNCTIONAL BLOCK DIAGRAM



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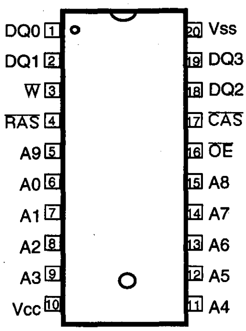
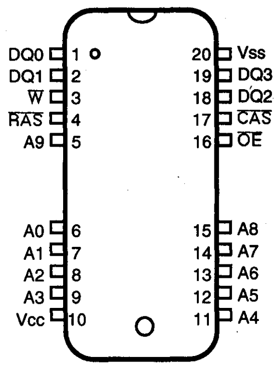
PIN CONFIGURATION (Top Views)

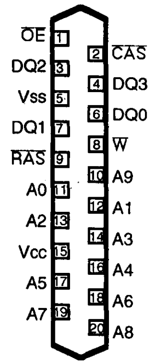
• KM44C/V1004CP



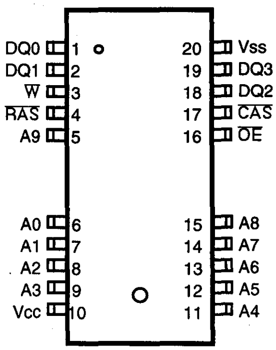
• KM44C/V1004CJ



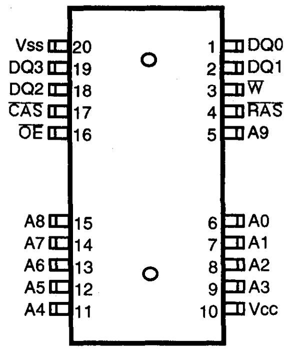
• KM44C/V1004CZ



• KM44C/V1004CT



• KM44C/V1004CTR



Pin Name	Pin Function
A0 - A9	Address Inputs
DQ0 -3	Data In/Out
V_{SS}	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Outputs Enable
V_{CC}	Power(+5.0V)
	Power(+3.3V)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Units
		3.3V	5V	
Voltage on any pin relative to V_{SS}	V_{IN},V_{OUT}	-0.5 to +4.6	-1.0 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.5 to +4.6	-1.0 to +7.0	V
Storage Temperature	Tstg	-55 to +150	-55 to +150	°C
Power Dissipation	P_D	600	600	W
Short Circuit Output Current	I_{OS}	50	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A= 0 to 70 °C)

Parameter	Symbol	3.3V			5V			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V_{CC}	3.0	3.3	3.6	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	Vcc+0.3*1	2.4	-	Vcc+1.0*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	-1.0*2	-	0.8	V

*1 : Vcc+1.3V/15ns(3.3V),Vcc+2.0V/20ns(5V), Pulse width is measured at Vcc

*2 : -1.3V/15ns(3.3V), -2.0V/20ns(5V),Pulse width is measured atVss

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

	Parameter	Symbol	Min	Max	Units
3.3V	Input Leakage Current (Any input $0 \le V_{IN} \le V_{CC}+0.3V$, all other pins not under test=0V)	$I_{I(L)}$	-5	5	μA
	Output Leakage Current (Data out is disabled, $0V \le V_{OUT} \le V_{CC}$)	$I_{O(L)}$	-5	5	μA
	Output High Voltage Level (I_{OH}=-2mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level (I_{OL}=2mA)	V_{OL}	-	0.4	V
5V	Input Leakage Current (Any input $0 \le V_{IN} \le V_{CC}+0.5V$, (Any input $0 \le V_{IN} \le V_{CC}+0.5V$, all other pins not under test=0V)	$I_{I(L)}$	-5	5	μA
	Output Leakage Current (Data out is disabled, $0V \le V_{OUT} \le V_{CC}$)	$I_{O(L)}$	-5	5	μA
	Output High Voltage Level (I_{OH}=-5mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level (I_{OL}=4.2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Symbol	Power	Speed	Max		Units
			KM44V1004C	KM44C1004C	
I_{CC1}	Don't care	-5 -6 -7 -8	- 60 55 50	85 75 65 55	mA mA mA mA
I_{CC2}	Don't care	Don't care	1	2	mA
I_{CC3}	Don't care	-5 -6 -7 -8	- 60 55 50	85 75 65 55	mA mA mA mA
I_{CC4}	Don't care	-5 -6 -7 -8	- 60 55 50	85 75 65 55	mA mA mA mA
I_{CC5}	Normal L	Don't care	0.5 100	1 200	mA μA
I_{CC6}	Don't care	-5 -6 -7 -8	- 60 55 50	85 75 65 55	mA mA mA mA
I_{CC7}	L	Don't care	200	300	μA
I_{CCS}	L	Don't care	150	-	μA

I_{CC1}* : Operating current ($\overline{RAS}$, $\overline{CAS}$, Address cycling @tRC=min.)

I_{CC2} : Standby current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}* : $\overline{RAS}$-only refresh current ($\overline{CAS}$=V_{IH}, $\overline{RAS}$, Address cycling @tRC=min.)

I_{CC4}* : EDO Mode current ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address cycling @tPC=min.)

I_{CC5} : Standby current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6}* : $\overline{CAS}$-before-$\overline{RAS}$ Refresh current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode
Input high voltage(V_{IH})=Vcc-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{CAS}$= 0.2V
DQ0~3 = Don't care, T_{RC}=125μs, T_{RAS}=T_{RAS} min~300 ns

I_{CCS} : Self refresh current
$\overline{RAS}$=$\overline{CAS}$=V_{IL}, $\overline{W}$=$\overline{OE}$=A0 ~ A9 = Vcc-0.2V or 0.2V,
DQ0 ~ DQ3= Vcc-0.2V, 0.2V or open

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1} , I_{CC3} and I_{CC6}, address can be changed maximum two times while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one hyper page cycle.

CAPACITANCE (T_A=25°C,Vcc=5V or 3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 ~ A9]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ0 ~ DQ3]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 1,2)

Test condition (5V device) : Vcc=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.0/0.8V
Test condition (3.3V device) : Vcc=3.3V±0.3V, V_{ih}/V_{il}=2.0/0.8V, V_{oh}/V_{ol}=2.0/0.8V

Parameter	Symbol	-5 *1		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	84		104		124		144		ns	
Read-modify-write cycle time	tRWC	116		140		165		190		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70		80	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		13		15		20		20	ns	3,4,5
Access time from column address	tAA		25		30		35		40	ns	3,10
$\overline{CAS}$ to output in Low-Z	tCLZ	3		3		3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	tCEZ	3	13	3	15	3	20	3	20	ns	7,13
Transition time (rise and fall)	tT	2	50	2	50	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		60		ns	
$\overline{RAS}$ pulse width	tRAS	50	10K	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ hold time	tRSH	13		15		20		20		ns	
$\overline{CAS}$ hold time	tCSH	40		50		60		70		ns	
$\overline{CAS}$ pulse width	tCAS	8	10K	10	10K	15	10K	20	10K	ns	11
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	33	20	43	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	15	40	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	
Column address hold time	tCAH	8		10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	tAR	35		42		52		57		ns	17
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		0		ns	8
Write command hold time	tWCH	10		10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	tWCR	37		42		52		57		ns	17
Write command pulse width	tWP	10		10		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	13		15		20		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	8		10		15		20		ns	

Note) *1 : 5V only

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AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 1,2)

Parameter	Symbol	-5 *1		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		0		ns	9
Data hold time	tDH	8		10		15		15		ns	9
Data hold time referenced to $\overline{RAS}$	tDHR	35		42		52		57		ns	17
Refresh period(Normal)	tREF		16		16		16		16	ms	
Refresh period(L-ver)	tREF		128		128		128		128	ms	
Write command set-up time	tWCS	0		0		0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	30		34		44		44		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	67		79		89		99		ns	7
Column address to $\overline{W}$ delay time	tAWD	42		49		59		64		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	45		54		64		69		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	5		5		5		5		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		5		ns	
$\overline{CAS}$ precharge time($\overline{CBR}$ counter test cycle)	tCPT	20		20		25		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		28		35		40		45	ns	3
Hyper Page mode cycle time	tHPC	20		25		30		35		ns	15
Hyper Page mode read-modify-write cycle time	tHPRWC	47		56		71		81		ns	
$\overline{CAS}$ precharge time (Hyper page cycle)	tCP	8		10		10		10		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	tRASP	50	200K	60	200K	70	200K	80	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		45		ns	
$\overline{OE}$ access time	tOEA		13		15		20		20	ns	
$\overline{OE}$ to data delay	tOED	13		15		20		20		ns	
Out put buffer turn off delay time from $\overline{OE}$	tOEZ	3	13	3	15	3	20	3	20	ns	6,13
$\overline{OE}$ to output in low-Z	tOLZ	3		3		3		3		ns	
$\overline{OE}$ command hold time	tOEH	13		15		20		20		ns	
Output data hold time	tDOH	5		5		5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	tREZ	3	13	3	15	3	20	3	20	ns	6,13
Output buffer turn off delay from $\overline{W}$	tWEZ	3	13	3	15	3	20	3	20	ns	6,13
$\overline{W}$ to data delay	tWED	15		15		20		20		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	tOCH	5		5		5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	tCHO	5		5		5		5		ns	
$\overline{OE}$ precharge time	tOEP	5		5		5		5		ns	
$\overline{W}$ pulse width (hyper page cycle)	tWPE	5		5		5		5		ns	
$\overline{RAS}$ pulse width($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		100		μs	16
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	90		110		130		150		ns	16
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		-50		ns	16

Note) *1 : 5V only

TEST MODE CYCLE

(Note. 11)

Parameter	Symbol	-5*1		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	89		109		129		149		ns	
Read-modify-write cycle time	tRWC	121		145		170		195		ns	
Access time from $\overline{\text{RAS}}$	tRAC		55		65		75		85	ns	3,4,10
Access time from $\overline{\text{CAS}}$	tCAC		18		20		25		25	ns	3,4,5
Access time from column address	tAA		30		35		40		45	ns	3,10
$\overline{\text{RAS}}$ pulse width	tRAS	55	10K	65	10K	75	10K	85	10K	ns	
$\overline{\text{CAS}}$ pulse width	tCAS	13	10K	15	10K	20	10K	25	10K	ns	
$\overline{\text{RAS}}$ hold time	tRSH	18		20		25		25		ns	
$\overline{\text{CAS}}$ hold time	tCSH	45		55		65		75		ns	
Column address to $\overline{\text{RAS}}$ lead time	tRAL	30		35		40		45		ns	
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	tCWD	35		39		49		49		ns	7
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	tRWD	72		84		94		104		ns	7
Column address to $\overline{\text{W}}$ delay time	tAWD	47		54		64		69		ns	7
Hyper Page mode cycle time	tHPC	25		30		35		40		ns	15
Hyper page mode read-modify-write cycle time	tPRWC	52		61		76		86		ns	
$\overline{\text{RAS}}$ pulse width (Hyper page cycle)	tRASP	55	200K	65	200K	75	200K	85	200K	ns	
Access time form $\overline{\text{CAS}}$ precharge	tCPA		33		40		45		50	ns	3
$\overline{\text{OE}}$ access time	tOEA		18		20		25		25	ns	
$\overline{\text{OE}}$ to data delay	tOED	18		20		25		25		ns	
$\overline{\text{OE}}$ command hold time	tOEH	18		20		25		25		ns	

Note) *1 : 5V only

NOTES

1. An initial pause of 200µs is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 2ns for all inputs.
3. Measured with a load equivalent to 2 TTL(5V)/1 TTL(3.3V) loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS≥ tWCS(min), the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥ tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
11. These specifications are applied in the test mode.
12. In test mode read cycle, the value of tRAC, tAA, tCAC is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
13. tCEZ(max),tREZ(max),tOEZ(max) and tWEZ(max) define the time at which the output achives the open circuit condition and are not referenced to output voltage level.
14. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going.
15. tASC≥6ns, Assume tT=2.0ns.
16. 1024 cycles of burst refresh must be executed within 16ms before and after self refresh,in order to meet refresh specification.(3.3V L-Ver.)
17. tAR , tWCR ,tDHR are referenced to tRAD(max).

1M x 4 Bit CMOS Dynamic RAM with Fast Page Mode (Write Per Bit Mode)

DESCRIPTION

This is a family of 1,048,576 x 4 bit Fast Page Mode CMOS DRAMs. Fast Page Mode offers high speed random access of memory cells within the same row. Access time(-5, -6, -7 or -8) and package type (SOJ , DIP, ZIP, TSOP-II) are optional features of this family.
All of this family have $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ Refresh, $\overline{\text{RAS}}$-only refresh and Hidden Refresh capabilities.
This 1Mx4 Fast Page Mode DRAM Family is fabricated using Samsung's advanced CMOS process to realize high band-width and high reliability.

FEATURES

- Part Identification
  - KM44C1010C

- Active Power Dissipation

Unit : mW

Speed	Active power dissipation
-5	470
-6	415
-7	360
-8	305

- Refresh cycles

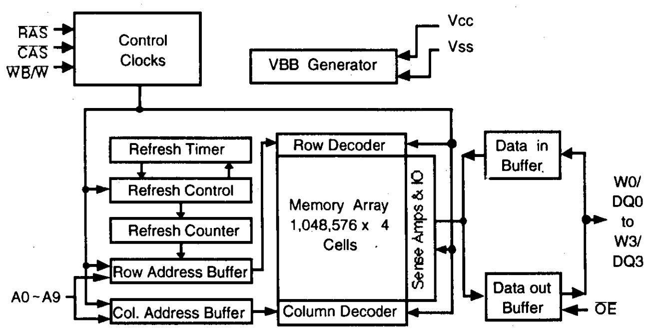
	Vcc	Refresh cycle	Refresh time
C1010C	5V	1K	16ms

- Performance range:

Speed	tRAC	tCAC	tRC	tPC
-5	50ns	13ns	90ns	35ns
-6	60ns	15ns	110ns	40ns
-7	70ns	20ns	130ns	45ns
-8	80ns	20ns	150ns	50ns

- Fast Page Mode operation
- Write Per Bit Mode Capability
- $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh capability
- $\overline{\text{RAS}}$-only and Hidden refresh capability
- Fast parallel test mode capability
- TTL compatible inputs and outputs
- Early Write or Output enable controlled write
- JEDEC Standard pinout
- Available in Plastic SOJ, ZIP, DIP,TSOP(II) packages
- Single +5V$\pm$10% power supply

FUNCTIONAL BLOCK DIAGRAM



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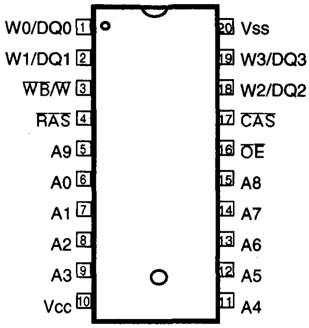
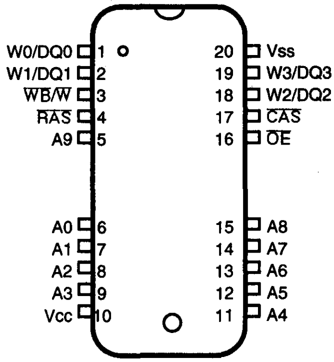
PIN CONFIGURATION (Top Views)

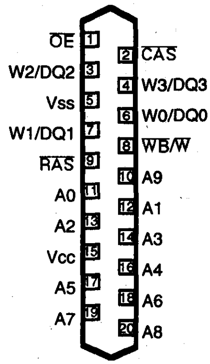
• KM44C1010CP



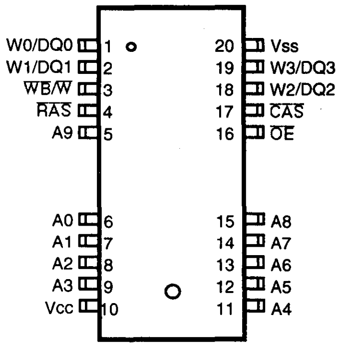
• KM44C1010CJ



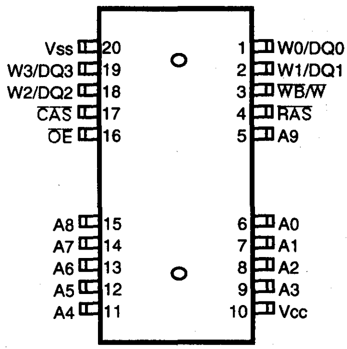
• KM44C1010CZ



• KM44C1010CT



• KM44C1010CTR



Pin Name	Pin Function
A0 - A9	Address Inputs
$\overline{\text{WB}}/\overline{\text{W}}$	Write per bit/Read/Write input
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
W0/DQ0 ~W3/DQ3	Write select/Data In/Out
$\overline{\text{OE}}$	Data Outputs Enable
Vcc	Power(+5.0V)
Vss	Ground

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	V_{CC}	-1 to +7.0	V
Storage temperature	Tstg	-55 to +150	°C
Power dissipation	P_D	600	mW
Short circuit output current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to Vss, T_A= 0 to 70 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input high voltage	V_{IH}	2.4	-	Vcc+1.0*1	V
Input low voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : Vcc+2.0V/20ns(5V), Pulse width is measured at Vcc

*2 : -2.0V/20ns(5V),Pulse width is measured atVss

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Units
Input leakage current (Any input $0 \le V_{IN} \le Vcc+0.5V$ all other pins not under test=0 volts.)	$I_{I(L)}$	-5	5	μA
Output leakage current (Data out is disabled, $0V \le V_{OUT} \le Vcc$)	$I_{O(L)}$	-5	5	μA
Output high voltage level(I_{OH}=-5mA)	V_{OH}	2.4	-	V
Output low voltage level(I_{OL}=4.2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Symbol	Speed	Max	Units
		KM44C1010C	
I_{CC1}	-5 -6 -7 -8	85 75 65 55	mA mA mA mA
I_{CC2}	Don't care	2	mA
I_{CC3}	-5 -6 -7 -8	85 75 65 55	mA mA mA mA
I_{CC4}	-5 -6 -7 -8	65 55 45 35	mA mA mA mA
I_{CC5}	Don't care	1	mA
I_{CC6}	-5 -6 -7 -8	85 75 65 55	mA mA mA mA

I_{CC1}* : Operating current($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC2} : Standby current ($\overline{RAS}=\overline{CAS}=\overline{W}=V_{IH}$)

I_{CC3}* : $\overline{RAS}$-only refresh current ($\overline{CAS}=V_{IH}$, $\overline{RAS}$,Address cycling @tRC=min.)

I_{CC4}* : Fast Page Mode current ($\overline{RAS}=V_{IL}$, $\overline{CAS}$, Address cycling @tPC=min.)

I_{CC5} : Standby current ($\overline{RAS}=\overline{CAS}=\overline{W}=V_{CC}$-0.2V)

I_{CC6}* : $\overline{CAS}$-before-$\overline{RAS}$ refresh current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} , I_{CC3} and I_{CC6}, address can be changed maximum once while $\overline{RAS}=V_{IL}$. In I_{CC4}, address can be changed maximum once within one fast page mode cycle time tPC.

CAPACITANCE(T_A=25°C,Vcc=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A9]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ0 - DQ3]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, Vcc=5.0V±10%, See note 1,2)
Test condition : Vcc=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.4/0.4V

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		130		150		ns	
Read-modify-write cycle time	tRWC	133		155		185		205		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70		80	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		13		15		20		20	ns	3,4,5
Access time from column address	tAA		25		30		35		40	ns	3,10
$\overline{CAS}$ to output in Low-Z	tCLZ	0		0		0		0		ns	3
Output buffer turn-off delay	tOFF	0	13	0	15	0	20	0	20	ns	6
Transition time (rise and fall)	tT	3	50	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		60		ns	
$\overline{RAS}$ pulse width	tRAS	50	10K	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ hold time	tRSH	13		15		20		20		ns	
$\overline{CAS}$ hold time	tCSH	50		60		70		80		ns	
$\overline{CAS}$ pulse width	tCAS	13	10K	15	10K	20	10K	20	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	37	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	15	40	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	
Column address hold time	tCAH	10		10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	tAR	40		45		55		60		ns	12
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		0		ns	8
Write command hold time	tWCH	10		10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	tWCR	40		45		55		60		ns	12
Write command pulse width	tWP	10		10		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		15		20		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	13		15		20		20		ns	

AC CHARACTERISTICS (0°C≤TA≤70°C, See note 1, 2)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		0		ns	9
Data hold time	tDH	10		10		15		15		ns	9
Data hold time referenced to $\overline{RAS}$	tDHR	40		45		55		60		ns	12
Refresh period	tREF		16		16		16		16	ms	
Write command set-up time	tWCS	0		0		0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	36		40		50		50		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	73		85		100		110		ns	7
Column address to $\overline{W}$ delay time	tAWD	48		55		65		70		ns	7
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	10		10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		5		ns	
$\overline{CAS}$ precharge time($\overline{CBR}$ counter test cycle)	tCPT	20		20		25		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		30		35		40		45	ns	3
Fast Page mode cycle time	tPC	35		40		45		50		ns	
Fast Page mode read-modify-write cycle time	tPRWC	76		85		100		105		ns	
$\overline{CAS}$ precharge time (Fast page cycle)	tCP	10		10		10		10		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	50	200K	60	200K	70	200K	80	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		45		ns	
$\overline{OE}$ access time	tOEA		13		15		20		20	ns	
$\overline{OE}$ to data delay	tOED	13		15		20		20		ns	
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	53		60		70		75		ns	
Out put buffer turn off delay time from $\overline{OE}$	tOEZ	0	13	0	15	0	20	0	20	ns	
$\overline{OE}$ command hold time	tOEH	13		15		20		20		ns	
Write command set-up time(Test mode in)	tWTS	10		10		10		10		ns	
Write command hold time(Test mode in)	tWTH	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		10		ns	
Write per bit set-up time	tWBS	0		0		0		0		ns	
Write per bit hold time	tWBH	10		10		10		15		ns	
Write per bit selection set-up time	tWDS	0		0		0		0		ns	
Write per bit hold time	tWDH	10		10		10		10		ns	

TEST MODE CYCLE

(Note. 11)

Parameter	Symbol	-5 Min	-5 Max	-6 Min	-6 Max	-7 Min	-7 Max	-8 Min	-8 Max	Units	Notes
Random read or write cycle time	tRC	95		115		135		155		ns	
Read-modify-write cycle time	tRWC	138		160		190		210		ns	
Access time from $\overline{RAS}$	tRAC		55		65		75		85	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		18		20		25		25	ns	3,4,5
Access time from column address	tAA		30		35		40		45	ns	3,10
$\overline{RAS}$ pulse width	tRAS	55	10K	65	10K	75	10K	85	10K	ns	
$\overline{CAS}$ pulse width	tCAS	18	10K	20	10K	25	10K	25	10K	ns	
$\overline{RAS}$ hold time	tRSH	18		20		25		25		ns	
$\overline{CAS}$ hold time	tCSH	55		65		75		85		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		45		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	41		45		55		55		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	78		90		105		115		ns	7
Column address to $\overline{W}$ delay time	tAWD	53		60		70		75		ns	7
Fast Page mode cycle time	tPC	40		45		50		55		ns	
Fast page mode read-modify-write cycle time	tPRWC	81		85		100		105		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	55	200K	65	200K	75	200K	85	200K	ns	
Access time form $\overline{CAS}$ precharge	tCPA		35		40		45		50	ns	3
$\overline{OE}$ access time	tOEA		20		20		25		25	ns	
$\overline{OE}$ to data delay	tOED	18		20		25		25		ns	
$\overline{OE}$ command hold time	tOEH	18		20		25		25		ns	

2

NOTES

1. An initial pause of 200μs is required after power up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD(max) is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS≥tWCS(min),the cycles is an early write cycle and the data output will remain high imped-ance for theduration of the cycle. If tCWD≥ tCWD(min), tRWD≥tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
11. These specifications are applied in the test mode.
12. tAR, tWCR, tDHR are referenced to tRAD(max).

512K x 8 Bit CMOS Dynamic RAM with Fast Page Mode

DESCRIPTION

This is a family of 524,288 x 8 bit Fast Page Mode CMOS DRAMs. Fast Page Mode offers high speed random access of memory cells within the same row. Power supply voltage(+5.0V or +3.3V), access time (-5, -6, -7 or -8), power consumption (Normal or Low power) and package type (SOJ or TSOP-II) are optional features of this family.

All of this family have $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$-only refresh and Hidden refresh capabilities. Further more, Self-refresh operation is available in Low power version.

This 512Kx8 Fast Page Mode DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability.

It may be used as main memory unit for personal computer and portable machines.

2

FEATURES

- Part Identification
  - KM48C512B/BL (5V, 1K Ref.)
  - KM48V512B/BL (3.3V, 1K Ref.)

- Active power dissipation

Unit : mW

Speed	3.3V (1K Ref.)	5V (1K Ref.)
-5	-	470
-6	255	385
-7	235	360
-8	220	330

- Refresh cycles

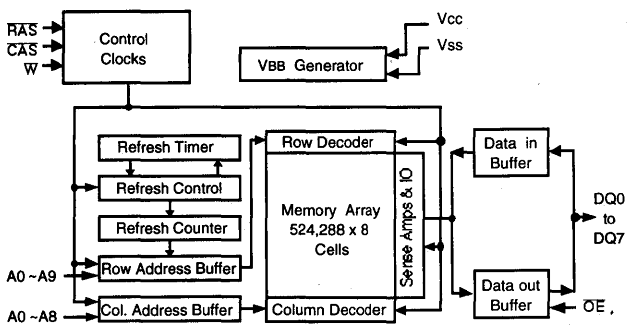
Part NO.	Vcc	Refresh cycle	Refresh period	
			Normal	L
C512B	5V	1K	16ms	128ms
V512B	3.3V			

- Performance range

Speed	tRAC	tCAC	tRC	tPC	Remark
-5	50ns	15ns	90ns	35ns	5V Only
-6	60ns	15ns	110ns	40ns	5V/3.3V
-7	70ns	20ns	130ns	45ns	5V/3.3V
-8	80ns	20ns	150ns	50ns	5V/3.3V

- Fast Page Mode operation
- Byte Read/Write operation
- $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh capability
- $\overline{\text{RAS}}$-only and Hidden refresh capability
- Self-refresh capability (L-ver only)
- TTL(5V)/LVTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC standard pinout
- Available in plastic SOJ and TSOP(II) packages
- Dual+5V±10% power supply (5V product)
- Dual +3.3V±0.3V power supply (3.3V product)

FUNCTIONAL BLOCK DIAGRAM



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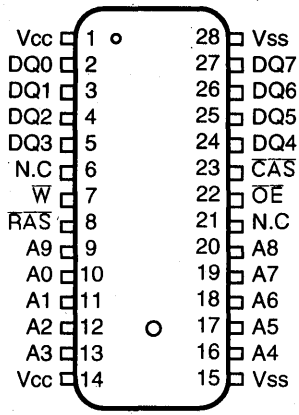
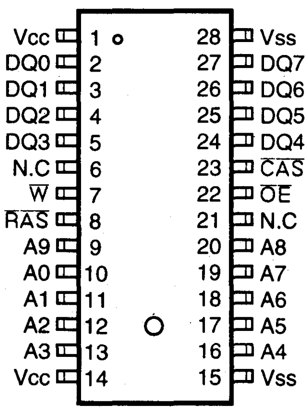
PIN CONFIGURATION (Top Views)

• KM48C/V512BJ



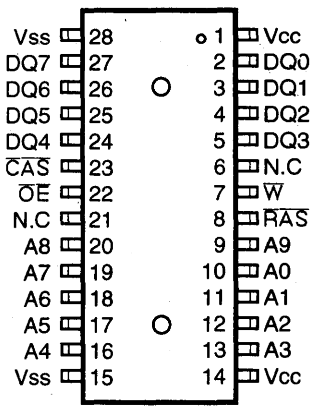
(SOJ)

• KM48C/V512BT



(TSOP(II)-Forward Type)

• KM48C/V512BTR



(TSOP(II)-Reverse Type)

Pin Name	Pin Function	Pin Name	Pin Function
A0 - A9	Address Inputs	$\overline{W}$	Read/Write Input
DQ0 -7	Data In/Out	$\overline{OE}$	Data Output Enable
Vss	Ground	Vcc	Power (+5V)
$\overline{RAS}$	Row Address Strobe		Power (+3.3V)
$\overline{CAS}$	Column Address Strobe	N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Units
		3.3V	5V	
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-0.5 to +4.6	-1.0 to +7.0	V
Voltage on Vcc supply relative to Vss	V_{CC}	-0.5 to +4.6	-1.0 to +7.0	V
Storage Temperature	Tstg	-55 to +150	-55 to +150	°C
Power Dissipation	P_D	1	1	W
Short Circuit Output Current	I_{OS}	50	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to Vss, T_A= 0 to 70 °C)

Parameter	Symbol	3.3V			5V			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V_{CC}	3.0	3.3	3.6	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	0	0	0	V
Input High Voltage	V_{IH}	2.1	-	Vcc+0.3*1	2.4	-	Vcc+1.0*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	-1.0*2	-	0.8	V

*1 : Vcc+1.3V/15ns(3.3V), Vcc+2.0V/20ns(5V), Pulse width is measured at Vcc.

*2 : -1.3V/15ns(3.3V), -2.0V/20ns(5V), Pulse width is measured at Vss.

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

	Parameter	Symbol	Min	Max	Units
3.3V	Input Leakage Current (Any input $0 \le V_{IN} \le Vcc+0.3V$, all other pins not under test=0V)	$I_{I(L)}$	-5	5	µA
	Output Leakage Current (Data out is disabled, $0V \le V_{OUT} \le Vcc$)	$I_{O(L)}$	-5	5	µA
	Output High Voltage Level (I_{OH}=-2mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level (I_{OL}=2mA)	V_{OL}	-	0.4	V
5V	Input Leakage Current (Any input $0 \le V_{IN} \le Vcc+0.5V$, (Any input $0 \le V_{IN} \le Vcc+0.5V$, all other pins not under test=0V)	$I_{I(L)}$	-5	5	µA
	Output Leakage Current (Data out is disabled, $0V \le V_{OUT} \le Vcc$)	$I_{O(L)}$	-5	5	µA
	Output High Voltage Level (I_{OH}=-5mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level (I_{OL}=4.2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Symbol	Power	Speed	Max		Units
			KM48V512B	KM48C512B	
Icc1	Don't care	-5 -6 -7 -8	- 70 65 60	85 70 65 60	mA mA mA mA
Icc2	Don't care	Don't care	1	2	mA
Icc3	Don't care	-5 -6 -7 -8	- 70 65 60	85 70 65 60	mA mA mA mA
Icc4	Don't care	-5 -6 -7 -8	- 55 50 45	65 55 50 45	mA mA mA mA
Icc5	Normal L	Don't care	0.5 100	1 150	mA μA
Icc6	Don't care	-5 -6 -7 -8	- 70 65 60	85 70 65 60	mA mA mA mA
Icc7	L	Don't care	200	300	μA
Iccs	L	Don't care	100	200	μA

Icc1* : Operating current ($\overline{RAS}$, $\overline{CAS}$, Address cycling @tRC=min.)

Icc2 : Standby current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=VIH)

Icc3* : $\overline{RAS}$-only refresh current ($\overline{CAS}$=VIH, $\overline{RAS}$, Address cycling @tRC=min.)

Icc4* : Fast Page Mode current ($\overline{RAS}$=VIL, $\overline{CAS}$, Address cycling @tPC=min.)

Icc5 : Standby current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

Icc6* : $\overline{CAS}$-before-$\overline{RAS}$ Refresh current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

Icc7 : Battery back-up current, Average power supply current, Battery back-up mode
Input high voltage(VIH)=Vcc-0.2V, Input low voltage(VIL)=0.2V, $\overline{CAS}$= 0.2V
Din = Don't care, TRC=125μs, TRAS=TRAS min~300 ns

Iccs : Self refresh current
$\overline{RAS}$=$\overline{CAS}$=VIL, $\overline{W}$=$\overline{OE}$=A0 ~ A9 = Vcc-0.2V or 0.2V,
DQ0 ~ DQ7= Vcc-0.2V, 0.2V or open

* NOTE : Icc1, Icc3, Icc4 and Icc6 are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In Icc1, Icc3, and Icc6, address can be changed maximum once while $\overline{RAS}$=VIL. In Icc4, address can be changed maximum once within one fast page mode cycle time, tPC.

CAPACITANCE (T_A=25°C,Vcc=5V or 3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 ~ A9]	C_{IN1}	-	5	pF
Input capacitance [$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{W}}$, $\overline{\text{OE}}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ0~ DQ7]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 1,2)

Test condition (5V device) : Vcc=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol} =2.4/0.4V
Test condition (3.3V device): Vcc=3.3V±0.3V, V_{ih}/V_{il}=2.1/0.8V, V_{oh}/V_{ol} =2.0/0.8V

Parameter	Symbol	- 5(*)		- 6		- 7		- 8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		130		150		ns	
Read-modify-write cycle time	tRWC	135		155		185		205		ns	
Access time from $\overline{\text{RAS}}$	tRAC		50		60		70		80	ns	3,4,10
Access time from $\overline{\text{CAS}}$	tCAC		15		15		20		20	ns	3,4,5
Access time from column address	tAA		25		30		35		40	ns	3,10
$\overline{\text{CAS}}$ to output in Low-Z	tCLZ	0		0		0		0		ns	3
Output buffer turn-off delay	tOFF	0	15	0	15	0	15	0	15	ns	6
Transition time (rise and fall)	tT	3	50	3	50	3	50	3	50	ns	2
$\overline{\text{RAS}}$ precharge time	tRP	30		40		50		60		ns	
$\overline{\text{RAS}}$ pulse width	tRAS	50	10K	60	10K	70	10K	80	10K	ns	
$\overline{\text{RAS}}$ hold time	tRSH	15		15		20		20		ns	
$\overline{\text{CAS}}$ hold time	tCSH	50		60		70		80		ns	
$\overline{\text{CAS}}$ pulse width	tCAS	15	10K	15	10K	20	10K	20	10K	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	tRCD	20	35	20	45	20	50	20	60	ns	4
$\overline{\text{RAS}}$ to column address delay time	tRAD	15	25	15	30	15	35	15	40	ns	10
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	tCRP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	
Column address hold time (5V)	tCAH	10		10		15		15		ns	
Column address hold time (3.3V)	tCAH	-		15		15		15		ns	
Column address to $\overline{\text{RAS}}$ lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{\text{CAS}}$	tRCH	0		0		0		0		ns	8
Read command hold time referenced to $\overline{\text{RAS}}$	tRRH	0		0		0		0		ns	8
Write command set-up time	tWCS	0		0		0		0		ns	
Write command hold time	tWCH	10		10		10		10		ns	
Write command pulse width	tWP	10		10		10		10		ns	
Write command to $\overline{\text{RAS}}$ lead time	tRWL	15		15		15		20		ns	
Write command to $\overline{\text{CAS}}$ lead time	tCWL	15		15		15		20		ns	

(*) : 50ns product : Vcc=5V±5%, Output Loading(C_L)=50pF

AC CHARACTERISTICS (0°C≤TA≤70°C, See note 1,2)

Parameter	Symbol	-5(*)		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		0		ns	9
Data hold time (5V)	tDH	10		10		15		15		ns	9
Data hold time (3.3V)	tDH	-		15		15		15		ns	9
Refresh period (Normal)	tREF		16		16		16		16	ms	
Refresh period (L-ver)	tREF		128		128		128		128	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	40		40		50		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	75		85		95		105		ns	8
Column address to $\overline{W}$ delay time	tAWD	50		55		60		65		ns	8
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	55		60		65		70		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	5		5		5		5		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		5		ns	
$\overline{CAS}$ precharge time($\overline{CBR}$ counter test cycle)	tCPT	20		20		25		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		30		35		40		45	ns	3
Fast Page mode cycle time	tPC	35		40		45		50		ns	
Fast Page mode read-modify-write cycle time	tPRWC	80		80		95		105		ns	
$\overline{CAS}$ precharge time (Fast page cycle)	tCP	10		10		10		10		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	50	100K	60	100K	70	100K	80	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		45		ns	
$\overline{OE}$ access time	tOEA		15		15		20		20	ns	
$\overline{OE}$ to data delay	tOED	15		15		20		20		ns	
Out put buffer turn off delay time from $\overline{OE}$	tOEZ	0	15	0	15	0	20	0	20	ns	
$\overline{OE}$ command hold time	tOEH	15		15		20		20		ns	
$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		100		μs	11
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	90		110		130		150		ns	11
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		-50		ns	11

(*) : 50ns product : Vcc=5V±5%, Output Loading(CL)=50pF

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL(5V)/1 TTL(3.3V) loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. tOFF(max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS≥ tWCS(min), the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥ tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
11. 1024 cycle of burst refresh must be executed within 16ms before and after self refresh in order to meet refresh specification (L-version).

2

512K x 8 Bit CMOS Dynamic RAM with Extended Data Out

DESCRIPTION

This is a family of 524,288 x 8 bit Extended Data Out CMOS DRAMs. Extended Data Out offers high speed random access of memory cells within the same row. Power supply voltage (+5.0V or +3.3V), access time (-5, -6, -7 or -8), power consumption (Normal or Low power) and package type (SOJ or TSOP-II) are optional features of this family.

All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities. Further more, Self-refresh operation is available in Low power version.

This 512Kx8 Extended Data Out DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability.

It may be used as main memory unit for personal computer and portable machines.

FEATURES

- Part Identification
  - KM48C514B/BL (5V, 1K Ref.)
  - KM48V514B/BL (3.3V, 1K Ref.)

- Active power dissipation

Unit : mW

Speed	3.3V (1K Ref.)	5V (1K Ref.)
-5	-	470
-6	255	385
-7	235	360
-8	220	-

- Refresh cycles

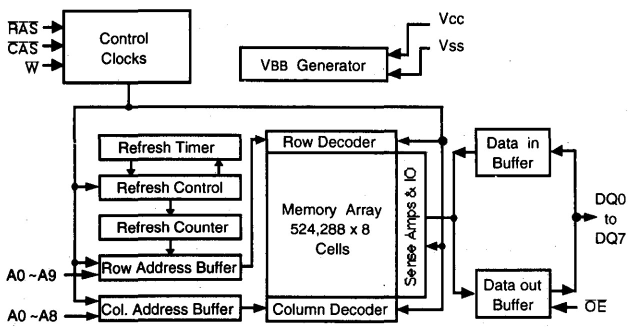
Part NO.	Vcc	Refresh cycle	Refresh Period	
			Normal	L
C514B	5V	1K	16ms	128ms
V514B	3.3V			

- Performance range

Speed	tRAC	tCAC	tRC	tHPC	Remark
-5	50ns	15ns	90ns	20ns	5V Only
-6	60ns	15ns	110ns	25ns	5V/3.3V
-7	70ns	20ns	130ns	30ns	5V/3.3V
-8	80ns	20ns	150ns	35ns	3.3V Only

- Extended Data Out operation
- Byte Read/Write operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- Self-refresh capability (L-ver only)
- TTL(5V)/LVTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC standard pinout
- Available in plastic SOJ and TSOP(II) packages
- Dual +5V±10% power supply (5V product)
- Dual +3.3V±0.3V power supply (3.3V product)

FUNCTIONAL BLOCK DIAGRAM



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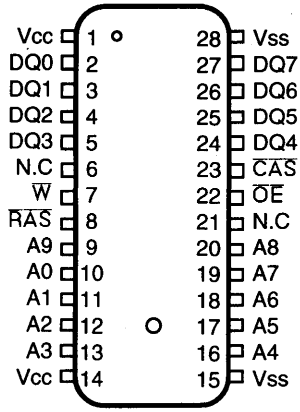
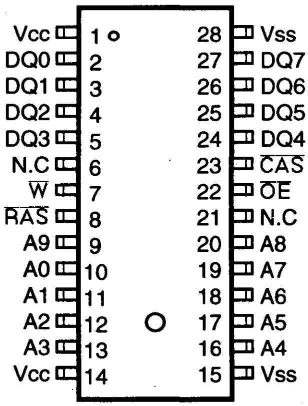
PIN CONFIGURATION (Top Views)

• KM48C/V514BJ



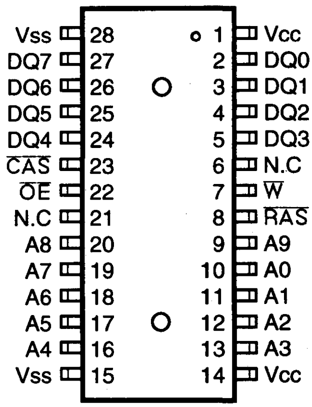
(SOJ)

• KM48C/V514BT



(TSOP(II)-Forward Type)

• KM48C/V514BTR



(TSOP(II)-Reverse Type)

Pin Name	Pin Function	Pin Name	Pin Function
A0 - A9	Address Inputs	$\overline{W}$	Read/Write Input
DQ0 -7	Data In/Out	$\overline{OE}$	Data Output Enable
Vss	Ground	Vcc	Power (+5V)
$\overline{RAS}$	Row Address Strobe		Power (+3.3V)
$\overline{CAS}$	Column Address Strobe	N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Units
		3.3V	5V	
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-0.5 to +4.6	-1.0 to +7.0	V
Voltage on Vcc supply relative to Vss	V_{CC}	-0.5 to +4.6	-1.0 to +7.0	V
Storage Temperature	Tstg	-55 to +150	-55 to +150	°C
Power Dissipation	P_D	1	1	W
Short Circuit Output Current	I_{OS}	50	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to Vss, T_A= 0 to 70 °C)

Parameter	Symbol	3.3V			5V			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V_{CC}	3.0	3.3	3.6	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	0	0	0	V
Input High Voltage	V_{IH}	2.1	-	Vcc+0.3*1	2.4	-	Vcc+1.0*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	-1.0*2	-	0.8	V

*1 : Vcc+1.3V/15ns(3.3V), Vcc+2.0V/20ns(5V), Pulse width is measured at Vcc.

*2 : -1.3V/15ns(3.3V), -2.0V/20ns(5V), Pulse width is measured at Vss.

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

	Parameter	Symbol	Min	Max	Units
3.3V	Input Leakage Current (Any input $0 \le V_{IN} \le Vcc+0.3V$, all other pins not under test=0V)	$I_{I(L)}$	-5	5	μA
	Output Leakage Current (Data out is disabled, $0V \le V_{OUT} \le Vcc$)	$I_{O(L)}$	-5	5	μA
	Output High Voltage Level (I_{OH}=-2mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level (I_{OL}=2mA)	V_{OL}	-	0.4	V
5V	Input Leakage Current (Any input $0 \le V_{IN} \le Vcc+0.5V$, (Any input $0 \le V_{IN} \le Vcc+0.5V$, all other pins not under test=0V)	$I_{I(L)}$	-5	5	μA
	Output Leakage Current (Data out is disabled, $0V \le V_{OUT} \le Vcc$)	$I_{O(L)}$	-5	5	μA
	Output High Voltage Level (I_{OH}=-5mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level (I_{OL}=4.2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Symbol	Power	Speed	Max		Units
			KM48V514B	KM48C514B	
I_{CC1}	Don't care	-5 -6 -7 -8	- 70 65 60	85 70 65 -	mA mA mA mA
I_{CC2}	Don't care	Don't care	1	2	mA
I_{CC3}	Don't care	-5 -6 -7 -8	- 70 65 60	85 70 65 -	mA mA mA mA
I_{CC4}	Don't care	-5 -6 -7 -8	- 55 50 45	65 55 50 -	mA mA mA mA
I_{CC5}	Normal L	Don't care	0.5 100	1 150	mA µA
I_{CC6}	Don't care	-5 -6 -7 -8	- 70 65 60	85 70 65 -	mA mA mA mA
I_{CC7}	L	Don't care	200	300	µA
I_{CCS}	L	Don't care	100	200	µA

I_{CC1}* : Operating current ($\overline{RAS}$, $\overline{CAS}$, Address cycling @tRC=min.)

I_{CC2} : Standby current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}* : $\overline{RAS}$-only refresh current ($\overline{CAS}$=V_{IH}, $\overline{RAS}$, Address cycling @tRC=min.)

I_{CC4}* : Hyper Page Mode current ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address cycling @tHPC=min.)

I_{CC5} : Standby current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)

I_{CC6}* : $\overline{CAS}$-before-$\overline{RAS}$ Refresh current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode
Input high voltage(V_{IH})=V_{CC}-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{CAS}$= 0.2V
Din = Don't care, T_{RC}=125µs, T_{RAS}=T_{RAS} min~300 ns

I_{CCS} : Self refresh current
$\overline{RAS}$=$\overline{CAS}$=V_{IL}, $\overline{W}$=$\overline{OE}$=A0 ~ A9 = V_{CC}-0.2V or 0.2V,
DQ0 ~ DQ7 = V_{CC}-0.2V, 0.2V or open

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1}, I_{CC3}, and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one hyper page cycle time, tHPC

CAPACITANCE (T_A=25°C,Vcc=5V or 3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 ~ A9]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ0 ~ DQ7]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 1,2)

Test condition (5V device) : Vcc=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.0/0.8V
Test condition (3.3V device) : Vcc=3.3V±0.3V, V_{ih}/V_{il}=2.1/0.8V, V_{oh}/V_{ol}=2.0/0.8V

Parameter	Symbol	-5(*)		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	84		104		124		144		ns	
Read-modify-write cycle time	tRWC	116		140		165		190		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70		80	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		17		17		20		20	ns	3,4,5
Access time from column address	tAA		25		30		35		40	ns	3,10
$\overline{CAS}$ to output in Low-Z	tCLZ	3		3		3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	tCEZ	3	13	3	15	3	15	3	15	ns	6, 13
Transition time (rise and fall)	tT	2	50	2	50	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		60		ns	
$\overline{RAS}$ pulse width	tRAS	50	10K	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ hold time	tRSH	17		17		20		20		ns	
$\overline{CAS}$ hold time	tCSH	40		50		60		70		ns	
$\overline{CAS}$ pulse width	tCAS	8	10K	10	10K	15	10K	20	10K	ns	11
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	33	20	43	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	15	40	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	
Column address hold time (5V)	tCAH	8		10		15		-		ns	
Column address hold time (3.3V)	tCAH	-		15		15		15		ns	
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		0		ns	8
Write command set-up time	tWCS	0		0		0		0		ns	7
Write command hold time	tWCH	10		10		10		10		ns	
Write command pulse width	tWP	10		10		10		10		ns	
Write command to $\overline{RAS}$ lead time	tRWL	13		15		15		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	8		10		15		20		ns	

(*) : 50ns product : Vcc=5V±5%, Output Loading(C_L)=50pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 1,2)

Parameter	Symbol	- 5(*)		- 6		- 7		- 8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		0		ns	9
Data hold time (5V)	tDH	8		10		15		-		ns	9
Data hold time (3.3V)	tDH	-		15		15		15		ns	
Refresh period (Normal)	tREF		16		16		16		16	ms	
Refresh period (L-ver)	tREF		128		128		128		128	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	34		36		44		44		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	67		79		94		104		ns	7
Column address to $\overline{W}$ delay time	tAWD	42		49		59		64		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	45		54		64		69		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	5		5		5		5		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{CBR}$ counter test cycle)	tCPT	20		20		25		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		28		35		40		45	ns	3
Hyper Page mode cycle time	tHPC	20		25		30		35		ns	11
Hyper Page mode read-modify-write cycle time	tHPRWC	47		56		71		81		ns	11
$\overline{CAS}$ precharge time (Hyper page cycle)	tCP	8		10		10		10		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	tRASP	50	100K	60	100K	70	100K	80	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		45		ns	
$\overline{OE}$ access time	tOEA		15		15		20		20	ns	3
$\overline{OE}$ to data delay	tOED	13		15		20		20		ns	
Out put buffer turn off delay time from $\overline{OE}$	tOEZ	3	13	3	15	3	20	3	20	ns	6
$\overline{OE}$ to output in low-Z	tOLZ	3		3		3		3		ns	
$\overline{OE}$ command hold time	tOEH	13		15		20		20		ns	
Output data hold time	tDOH	5		5		5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	tREZ	3	13	3	15	3	20	3	20	ns	6, 13
Output buffer turn off delay from $\overline{W}$	tWEZ	3	13	3	15	3	20	3	20	ns	6
$\overline{W}$ to data delay	tWED	13		15		20		20		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	tOCH	5		5		5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	tCHO	5		5		5		5		ns	
$\overline{OE}$ precharge time	tOEP	5		5		5		5		ns	
$\overline{W}$ pulse width (hyper page cycle)	tWPE	5		5		5		5		ns	
$\overline{RAS}$ pulse width($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		100		µs	12
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	90		110		130		150		ns	12
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		-50		ns	12

(*) : 50ns product : Vcc=5V±5%, Output Loading(C_L)=50pF

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NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 2ns for all inputs.
3. Measured with a load equivalent to 2 TTL(5V)/1 TTL(3.3V) loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS≥ tWCS(min), the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥ tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
11. tASC≥6ns, Assume tT=2.0ns.
12. 1024 cycle of burst refresh must be executed within 8ms before and after self refresh in order to meet refresh specification (L-version).
13. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going.

512K x 9 Bit CMOS Dynamic RAM with Fast Page Mode

DESCRIPTION

This is a family of 524,288 x 9 bit Fast Page Mode CMOS DRAMs. Fast Page Mode offers high speed random access of memory cells within the same row. Access time (-6, -7 or -8), power consumption (Normal or Low power) and package type (SOJ or TSOP-II) are optional features of this family.
All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities. Further more, Self-refresh operation is available in Low power version.
This 512Kx9 Fast Page Mode DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability.
It may be used as main memory unit for personal computer and portable machines.

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FEATURES

- Part Identification
  - KM49C512B/BL (5V, 1K Ref.)

- Active power dissipation

Unit : mW

Speed	Active power dissipation
-6	415
-7	385
-8	360

- Refresh cycles

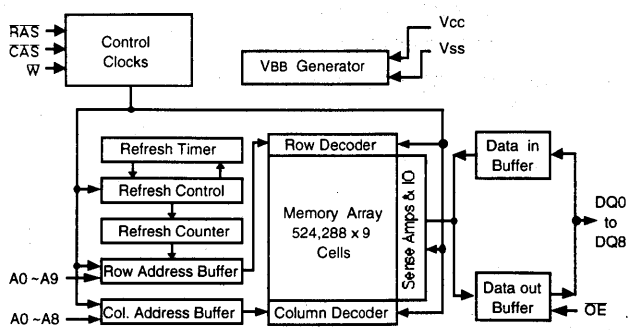
Part NO.	Refresh cycle	Refresh period	
		Normal	L
C512B	1K	16ms	128ms

- Performance range

Speed	tRAC	tCAC	tRC	tPC
-6	60ns	15ns	110ns	40ns
-7	70ns	20ns	130ns	45ns
-8	80ns	20ns	150ns	50ns

- Fast Page Mode operation
- Byte Read/Write operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- Self-refresh capability (L-ver only)
- TTL(5V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC standard pinout
- Available in plastic SOJ and TSOP(II) packages
- Dual +5V±10% power supply

FUNCTIONAL BLOCK DIAGRAM



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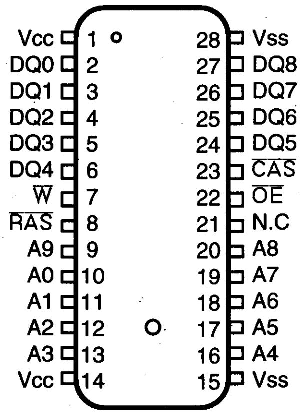
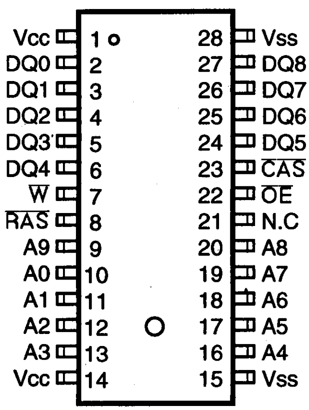
PIN CONFIGURATION (Top Views)

• KM49C512BJ



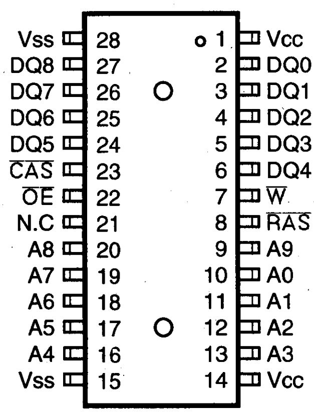
(SOJ)

• KM49C512BT



(TSOP(II)-Forward Type)

• KM49C512BTR



(TSOP(II)-Reverse Type)

Pin Name	Pin Function
A0 - A9	Address Inputs
DQ0 -8	Data In/Out
Vss	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe

Pin Name	Pin Function
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
Vcc	Power (+5V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 to +7.0	V
Voltage on Vcc supply relative to Vss	V_{CC}	-1.0 to +7.0	V
Storage Temperature	Tstg	-55 to +150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to Vss, T_A= 0 to 70 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	Vcc+1.0 [*1]	V
Input Low Voltage	V_{IL}	-1.0 [*2]	-	0.8	V

*1 : Vcc+2.0V/20ns, Pulse width is measured at Vcc.

*2 : -2.0V/20ns, Pulse width is measured at Vss.

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	V
Input Leakage Current (Any input $0 \le V_{IN} \le Vcc+0.5V$, (Any input $0 \le V_{IN} \le Vcc+0.5V$, all other pins not under test=0V)	$I_{I(L)}$	-5	5	μA
Output Leakage Current (Data out is disabled, $0V \le V_{OUT} \le Vcc$)	$I_{O(L)}$	-5	5	μA
Output High Voltage Level (I_{OH}=-5mA)	V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=4.2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Symbol	Power	Speed	Max	Units
I_{CC1}	Don't care	-6	75	mA
		-7	70	mA
		-8	65	mA
I_{CC2}	Don't care	Don't care	2	mA
I_{CC3}	Don't care	-6	75	mA
		-7	70	mA
		-8	65	mA
I_{CC4}	Don't care	-6	55	mA
		-7	50	mA
		-8	45	mA
I_{CC5}	Normal	Don't care	1	mA
	L		150	µA
I_{CC6}	Don't care	-6	75	mA
		-7	70	mA
		-8	65	mA
I_{CC7}	L	Don't care	300	µA
I_{CCS}	L	Don't care	200	µA

I_{CC1}* : Operating current ($\overline{RAS}$, $\overline{CAS}$, Address cycling @tRC=min.)

I_{CC2} : Standby current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}* : $\overline{RAS}$-only refresh current ($\overline{CAS}$=V_{IH}, $\overline{RAS}$, Address cycling @tRC=min.)

I_{CC4}* : Fast Page Mode current ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address cycling @tPC=min.)

I_{CC5} : Standby current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)

I_{CC6}* : $\overline{CAS}$-before-$\overline{RAS}$ Refresh current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode
Input high voltage(V_{IH})=V_{CC}-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{CAS}$= 0.2V
Din = Don't care, T_{RC}=125µs, T_{RAS}=T_{RAS} min~300 ns

I_{CCS} : Self refresh current
$\overline{RAS}$=$\overline{CAS}$=V_{IL}, $\overline{W}$=$\overline{OE}$=A0 ~ A9 = V_{CC}-0.2V or 0.2V,
DQ0 ~ DQ8= V_{CC}-0.2V, 0.2V or open

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1}, I_{CC3}, and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one fast page mode cycle time, tPC.

CAPACITANCE (T_A=25°C, Vcc=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 ~ A9]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ0 ~ DQ8]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 1,2)

Test condition : Vcc=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.4/0.4V

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	110		130		150		ns	
Read-modify-write cycle time	tRWC	155		185		205		ns	
Access time from $\overline{RAS}$	tRAC		60		70		80	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		15		20		20	ns	3,4,5
Access time from column address	tAA		30		35		40	ns	3,10
$\overline{CAS}$ to output in Low-Z	tCLZ	0		0		0		ns	3
Output buffer turn-off delay	tOFF	0	15	0	15	0	15	ns	6
Transition time (rise and fall)	tT	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	tRP	40		50		60		ns	
$\overline{RAS}$ pulse width	tRAS	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ hold time	tRSH	15		20		20		ns	
$\overline{CAS}$ hold time	tCSH	60		70		80		ns	
$\overline{CAS}$ pulse width	tCAS	15	10K	20	10K	20	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	30	15	35	15	40	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	
Column address hold time	tCAH	10		15		15		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		ns	8
Write command set-up time	tWCS	0		0		0		ns	
Write command hold time	tWCH	10		10		10		ns	
Write command pulse width	tWP	10		10		10		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		15		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	15		15		20		ns	

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 1,2)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		ns	9
Data hold time	tDH	10		15		15		ns	9
Refresh period (Normal)	tREF		16		16		16	ms	
Refresh period (L-ver)	tREF		128		128		128	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	40		50		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	85		95		105		ns	8
Column address to $\overline{W}$ delay time	tAWD	55		60		65		ns	8
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	60		65		70		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	5		5		5		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		ns	
$\overline{CAS}$ precharge time($\overline{CBR}$ counter test cycle)	tCPT	20		25		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		35		40		45	ns	3
Fast Page mode cycle time	tPC	40		45		50		ns	
Fast Page mode read-modify-write cycle time	tPRWC	80		95		105		ns	
$\overline{CAS}$ precharge time (Fast page cycle)	tCP	10		10		10		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	60	100K	70	100K	80	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	35		40		45		ns	
$\overline{OE}$ access time	tOEA		15		20		20	ns	
$\overline{OE}$ to data delay	tOED	15		20		20		ns	
Out put buffer turn off delay time from $\overline{OE}$	tOEZ	0	15	0	20	0	20	ns	
$\overline{OE}$ command hold time	tOEH	15		20		20		ns	
$\overline{RAS}$ pulse width($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		μs	11
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	110		130		150		ns	11
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		ns	11

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. tOFF(max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS≥ tWCS(min), the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥ tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
11. 1024 cycle of burst refresh must be executed within 16ms before and after self refresh in order to meet refresh specification (L-version).

256K x 16 Bit CMOS Dynamic RAM with Fast Page Mode

DESCRIPTION

This is a family of 262,144 x 16 bit Fast Page Mode CMOS DRAMs. Fast Page Mode offers high speed random access of memory cells within the same row. Power supply voltage (+5.0V or +3.3V), access time (-5, -6, -7 or -8), power consumption (Normal or Low power) and package type (SOJ or TSOP-II) are optional features of this family.

All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities. Further more, Self-refresh operation is available in Low power version.

This 256Kx16 Fast Page Mode DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability.

It may be used as graphic memory unit for microcomputer, personal computer and portable machines.

FEATURES

- Part Identification
  - KM416C256B/BL (5V, 512 Ref.)
  - KM416V256B/BL (3.3V, 512 Ref.)

- Active power dissipation

Unit : mW

Speed	3.3V (512 Ref.)	5V (512 Ref.)
-5	-	605
-6	325	495
-7	290	440
-8	270	415

- Refresh cycles

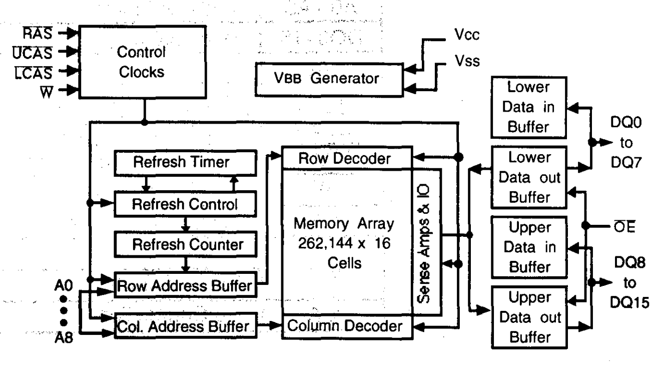
Part NO.	Vcc	Refresh cycle	Refresh period	
			Normal	L
C256B	5V	512	8ms	128ms
V256B	3.3V	512	8ms	128ms

- Performance range:

Speed	tRAC	tCAC	tRC	tPC	Remark
-5	50ns	15ns	90ns	35ns	5V Only
-6	60ns	15ns	110ns	40ns	5V/3.3V
-7	70ns	20ns	130ns	45ns	5V/3.3V
-8	80ns	20ns	150ns	50ns	5V/3.3V

- Fast Page Mode operation
- 2 $\overline{CAS}$ Byte/Word Read/Write operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- Self-refresh capability (L-ver only)
- TTL(5V)/LVTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC standard pinout
- Available in plastic SOJ and TSOP(II) packages
- Triple +5V±10% power supply (5V product)
- Triple +3.3V±0.3V power supply (3.3V product)

FUNCTIONAL BLOCK DIAGRAM



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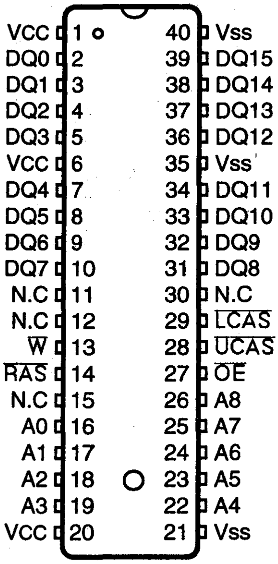
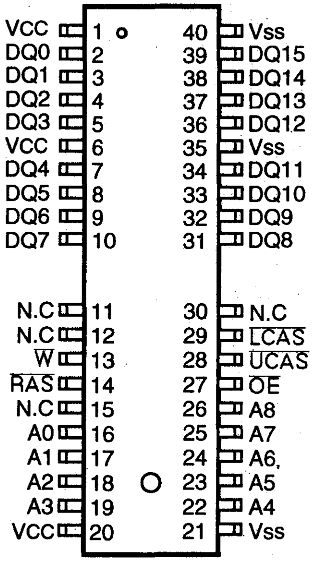
PIN CONFIGURATION (Top Views)

• KM416C/V256BJ



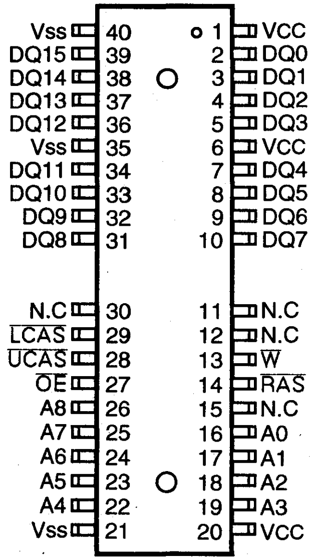
(SOJ)

• KM416C/V256BT



(TSOP(II)-Forward Type)

• KM416C/V256BTR



(TSOP(II)-Reverse Type)

Pin Name	Pin Function
A0 - A8	Address Inputs
DQ0 -15	Data In/Out
Vss	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Upper Column Address Strobe
$\overline{LCAS}$	Lower Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
Vcc	Power (+5V)
	Power (+3.3V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating 3.3V	Rating 5V	Units
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to +4.6	-1.0 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.5 to +4.6	-1.0 to +7.0	V
Storage Temperature	Tstg	-55 to +150	-55 to +150	°C
Power Dissipation	P_D	1	1	W
Short Circuit Output Current	I_{OS}	50	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to Vss, T_A= 0 to 70 °C)

Parameter	Symbol	3.3V Min	3.3V Typ	3.3V Max	5V Min	5V Typ	5V Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	0	0	0	V
Input High Voltage	V_{IH}	2.1	-	Vcc+0.3*1	2.4	-	Vcc+1.0*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	-1.0*2	-	0.8	V

*1 : Vcc+1.3V/15ns(3.3V), Vcc+2.0V/20ns(5V), Pulse width is measured at Vcc.

*2 : -1.3V/15ns(3.3V), -2.0V/20ns(5V), Pulse width is measured at Vss.

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

	Parameter	Symbol	Min	Max	Units
3.3V	Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.3V, all other pins not under test=0V)	$I_{I(L)}$	-5	5	µA
	Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	-5	5	µA
	Output High Voltage Level (I_{OH}=-2mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level (I_{OL}=2mA)	V_{OL}	-	0.4	V
5V	Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0V)	$I_{I(L)}$	-5	5	µA
	Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	-5	5	µA
	Output High Voltage Level (I_{OH}=-5mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level (I_{OL}=4.2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Symbol	Power	Speed	Max		Units
			KM416V256B	KM416C256B	
I_{CC1}	Don't care	-5 -6 -7 -8	- 90 80 75	110 90 80 75	mA mA mA mA
I_{CC2}	Don't care	Don't care	1	2	mA
I_{CC3}	Don't care	-5 -6 -7 -8	- 90 80 75	110 90 80 75	mA mA mA mA
I_{CC4}	Don't care	-5 -6 -7 -8	- 60 55 50	70 60 55 50	mA mA mA mA
I_{CC5}	Normal L	Don't care	0.5 100	1 150	mA µA
I_{CC6}	Don't care	-5 -6 -7 -8	- 90 80 75	110 90 80 75	mA mA mA mA
I_{CC7}	L	Don't care	200	300	µA
I_{CCS}	L	Don't care	100	200	µA

I_{CC1}* : Operating current ($\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, Address cycling @tRC=min.)

I_{CC2} : Standby current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{IH})

I_{CC3}* : $\overline{RAS}$-only refresh current ($\overline{UCAS}$=$\overline{LCAS}$=V_{IH}, $\overline{RAS}$, Address cycling @tRC=min.)

I_{CC4}* : Fast Page Mode current ($\overline{RAS}$=V_{IL}, $\overline{UCAS}$ or $\overline{LCAS}$, Address cycling @tPC=min.)

I_{CC5} : Standby current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6}* : $\overline{CAS}$-before-$\overline{RAS}$ Refresh current ($\overline{RAS}$, $\overline{UCAS}$ or $\overline{LCAS}$ cycling @tRC=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode
Input high voltage(V_{IH})=Vcc-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{UCAS}$, $\overline{LCAS}$= 0.2V
Din = Don't care, T_{RC}= 125µs, T_{RAS}=T_{RAS}min~300 ns

I_{CCS} : Self refresh current
$\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=V_{IL}, $\overline{W}$=$\overline{OE}$=A0 ~ A8 = Vcc-0.2V or 0.2V,
DQ0 ~ DQ15= Vcc-0.2V, 0.2V or open

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1}, I_{CC3}, and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one fast page mode cycle time, tPC.

CAPACITANCE (T_A=25°C,Vcc=5V or 3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A8]	C_{IN1}	-	5	pF
Input capacitance [$\overline{\text{RAS}}$, $\overline{\text{UCAS}}$,$\overline{\text{LCAS}}$, $\overline{\text{W}}$, $\overline{\text{OE}}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ0 - DQ15]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 1,2)

Test condition (5V device) : Vcc=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol} =2.4/0.4V
Test condition (3.3V device) : Vcc=3.3V±0.3V, V_{ih}/V_{il}=2.1/0.8V, V_{oh}/V_{ol} =2.0/0.8V

Parameter	Symbol	-5(*)		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		130		150		ns	
Read-modify-write cycle time	tRWC	135		155		185		205		ns	
Access time from $\overline{\text{RAS}}$	tRAC		50		60		70		80	ns	3,4,10
Access time from $\overline{\text{CAS}}$	tCAC		15		15		20		20	ns	3,4,5
Access time from column address	tAA		25		30		35		40	ns	3,10
$\overline{\text{CAS}}$ to output in Low-Z	tCLZ	0		0		0		0		ns	3
Output buffer turn-off delay	tOFF	0	15	0	15	0	15	0	15	ns	6
Transition time (rise and fall)	tT	3	50	3	50	3	50	3	50	ns	2
$\overline{\text{RAS}}$ precharge time	tRP	30		40		50		60		ns	
$\overline{\text{RAS}}$ pulse width	tRAS	50	10K	60	10K	70	10K	80	10K	ns	
$\overline{\text{RAS}}$ hold time	tRSH	15		15		20		20		ns	
$\overline{\text{CAS}}$ hold time	tCSH	50		60		70		80		ns	
$\overline{\text{CAS}}$ pulse width	tCAS	15	10K	15	10K	20	10K	20	10K	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	tRCD	20	35	20	45	20	50	20	60	ns	4
$\overline{\text{RAS}}$ to column address delay time	tRAD	15	25	15	30	15	35	15	40	ns	10
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	tCRP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	
Column address hold time (5V)	tCAH	10		10		15		15		ns	
Column address hold time (3.3V)	tCAH	-		15		15		15		ns	
Column address to $\overline{\text{RAS}}$ lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{\text{CAS}}$	tRCH	0		0		0		0		ns	8
Read command hold time referenced to $\overline{\text{RAS}}$	tRRH	0		0		0		0		ns	8
Write command set-up time	tWCS	0		0		0		0		ns	
Write command hold time	tWCH	10		10		10		10		ns	
Write command pulse width	tWP	10		10		10		10		ns	
Write command to $\overline{\text{RAS}}$ lead time	tRWL	15		15		15		20		ns	
Write command to $\overline{\text{CAS}}$ lead time	tCWL	15		15		15		20		ns	

(*) : 50ns product : Vcc=5V±5%, Output Loading(C_L)=50pF

AC CHARACTERISTICS (0°C≤TA≤70°C, See note 1,2)

Parameter	Symbol	- 5(*)		- 6		- 7		- 8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		0		ns	9
Data hold time (5V)	tDH	10		10		15		15		ns	9
Data hold time (3.3V)	tDH	-		15		15		15		ns	9
Refresh period (Normal)	tREF		8		8		8		8	ms	
Refresh period (L-ver)	tREF		128		128		128		128	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	40		40		50		50		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	75		85		95		105		ns	7
Column address to $\overline{W}$ delay time	tAWD	50		55		60		65		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	55		60		65		70		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	5		5		5		5		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		5		ns	
$\overline{CAS}$ precharge time($\overline{CBR}$ counter test cycle)	tCPT	20		20		25		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		30		35		40		45	ns	3
Fast Page mode cycle time	tPC	35		40		45		50		ns	
Fast Page mode read-modify-write cycle time	tPRWC	80		80		95		105		ns	
$\overline{CAS}$ precharge time (Fast page cycle)	tCP	10		10		10		10		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	50	100K	60	100K	70	100K	80	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		45		ns	
$\overline{OE}$ access time	tOEA		15		15		20		20	ns	
$\overline{OE}$ to data delay	tOED	15		15		20		20		ns	
Out put buffer turn off delay time from $\overline{OE}$	tOEZ	0	15	0	15	0	20	0	20	ns	
$\overline{OE}$ command hold time	tOEH	15		15		20		20		ns	
$\overline{RAS}$ pulse width($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		100		μs	11
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	90		110		130		150		ns	11
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		-50		ns	11

(*) : 50ns product : Vcc=5V±5%, Output Loading(CL)=50pF

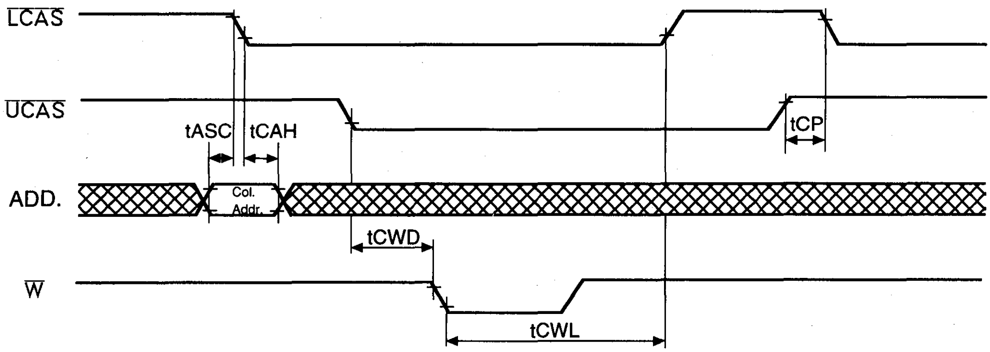
NOTES

1. An initial pause of 200µs is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL(5V)/1 TTL(3.3V) loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS≥ tWCS(min), the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥ tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.

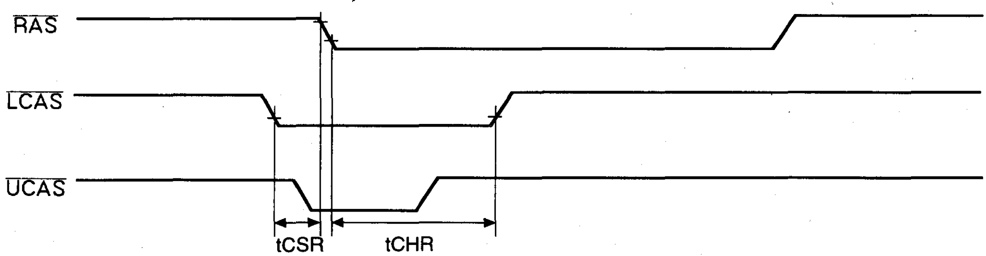
KM416C/V256B/BL Truth Table

$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	DQ0 -DQ7	DQ8 - DQ15	STATE
H	H	H	H	H	Hi-Z	Hi-Z	Standby
L	H	H	H	H	Hi-Z	Hi-Z	Refresh
L	L	H	H	L	DQ-OUT	Hi-Z	Byte Read
L	H	L	H	L	Hi-Z	DQ-OUT	Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-IN	-	Byte Write
L	H	L	L	H	-	DQ-IN	Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	Hi-Z	Hi-Z	-

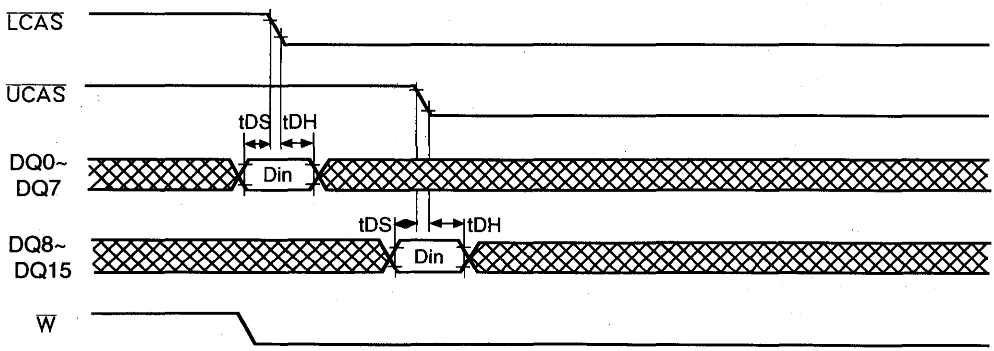
11. 512 cycle of burst refresh must be executed within 8ms before and after self refresh in order to meet refresh specification (L-version).
12. tASC, tCAH are referenced to the earlier $\overline{CAS}$ falling edge.
13. tCP is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.
14. tCWD is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.
15. tCWL is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.



17. tCSR is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.
18. tCHR is referenced to the later $\overline{CAS}$ rising high after $\overline{RAS}$ transition low.



19. tDS, tDH is independently specified for lower byte DIN(0~7), upper byte DIN(8~15).



256K x 16 Bit CMOS Dynamic RAM with Extended Data Out

DESCRIPTION

This is a family of 262,144 x 16 bit Extended Data Out CMOS DRAMs. Extended Data Out offers high speed random access of memory cells within the same row. Power supply voltage (+5.0V or +3.3V), access time (-5, -6, -7 or -8), power consumption (Normal or Low power) and package type(SOJ or TSOP-II) are optional features of this family.
All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities. Further more, Self-refresh operation is available in Low power version.
This 256Kx16 Extended Data Out DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability.
It may be used as graphic memory unit for microcomputer, personal computer and portable machines.

FEATURES

- Part Identification
  - KM416C254B/BL (5V, 512 Ref.)
  - KM416V254B/BL (3.3V, 512 Ref.)

- Active power dissipation

Unit : mW

Speed	3.3V (512 Ref.)	5V (512 Ref.)
-5	-	605
-6	255	495
-7	235	440
-8	220	-

- Refresh cycles

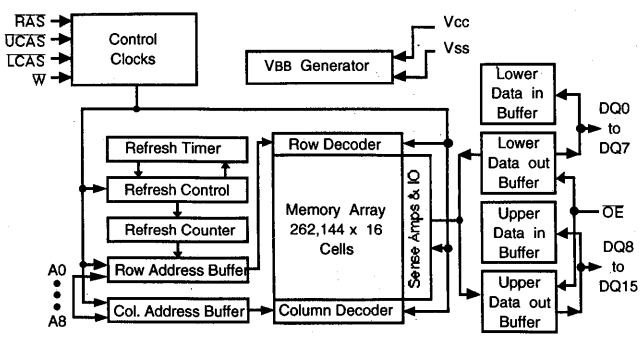
Part NO.	Vcc	Refresh cycle	Refresh Period	
			Normal	L
C254B	5V	512	8ms	128ms
V254B	3.3V			

- Performance range

Speed	tRAC	tCAC	tRC	tHPC	Remark
-5	50ns	17ns	84ns	20ns	5V Only
-6	60ns	17ns	104ns	25ns	5V/3.3V
-7	70ns	20ns	124ns	30ns	5V/3.3V
-8	80ns	20ns	144ns	35ns	3.3V Only

- Extended Data Out operation
- 2 $\overline{CAS}$ Byte/Word Read/Write operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- Self-refresh capability (L-ver only)
- TTL(5V)/LVTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC standard pinout
- Available in plastic SOJ and TSOP(II) packages
- Triple +5V±10% power supply (5V product)
- Triple +3.3V±0.3V power supply (3.3V product)

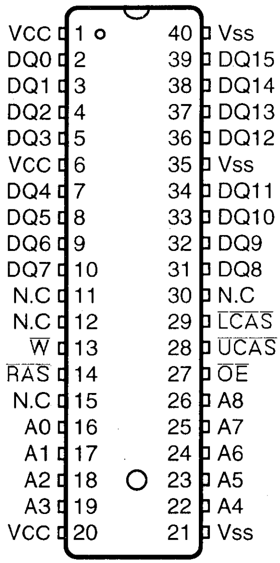
FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONIC CO. , LTD. reserves the right to change products and specifications without notice.

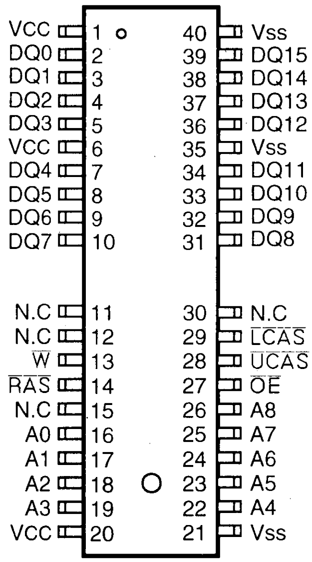
PIN CONFIGURATION (Top Views)

• KM416C/V254BJ



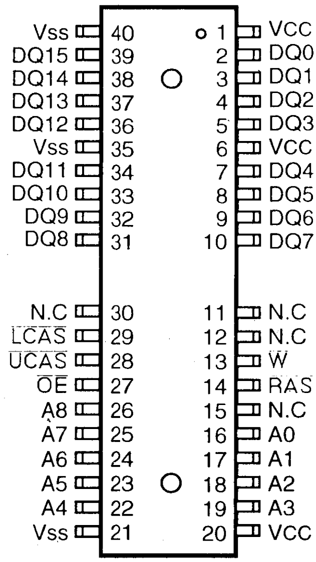
(SOJ)

• KM416C/V254BT



(TSOP(II)-Forward Type)

• KM416C/V254BTR



(TSOP(II)-Reverse Type)

Pin Name	Pin Function
A0 - A8	Address Inputs
DQ0 -15	Data In/Out
Vss	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Upper Column Address Strobe
$\overline{LCAS}$	Lower Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
Vcc	Power (+5V)
	Power (+3.3V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Units
		3.3V	5V	
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-0.5 to +4.6	-1.0 to +7.0	V
Voltage on Vcc supply relative to Vss	V_{CC}	-0.5 to +4.6	-1.0 to +7.0	V
Storage Temperature	Tstg	-55 to +150	-55 to +150	°C
Power Dissipation	P_D	1	1	W
Short Circuit Output Current	I_{OS}	50	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to Vss, T_A= 0 to 70 °C)

Parameter	Symbol	3.3V			5V			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V_{CC}	3.0	3.3	3.6	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	0	0	0	V
Input High Voltage	V_{IH}	2.1	-	Vcc+0.3*1	2.4	-	Vcc+1.0*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	-1.0*2	-	0.8	V

*1 : Vcc+1.3V/15ns(3.3V), Vcc+2.0V/20ns(5V), Pulse width is measured at Vcc.

*2 : -1.3V/15ns(3.3V), -2.0V/20ns(5V), Pulse width is measured at Vss.

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

	Parameter	Symbol	Min	Max	Units
3.3V	Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.3V, all other pins not under test=0V)	$I_{I(L)}$	-5	5	μA
	Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	-5	5	μA
	Output High Voltage Level (I_{OH}=-2mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level (I_{OL}=2mA)	V_{OL}	-	0.4	V
5V	Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0V)	$I_{I(L)}$	-5	5	μA
	Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	-5	5	μA
	Output High Voltage Level (I_{OH}=-5mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level (I_{OL}=4.2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Symbol	Power	Speed	Max		Units
			KM416V254B	KM416C254B	
I_{CC1}	Don't care	-5 -6 -7 -8	- 70 65 60	110 90 80 -	mA mA mA mA
I_{CC2}	Don't care	Don't care	1	2	mA
I_{CC3}	Don't care	-5 -6 -7 -8	- 70 65 60	110 90 80 -	mA mA mA mA
I_{CC4}	Don't care	-5 -6 -7 -8	- 60 55 50	70 60 50 -	mA mA mA mA
I_{CC5}	Normal L	Don't care	0.5 100	1 150	mA µA
I_{CC6}	Don't care	-5 -6 -7 -8	- 70 65 60	110 90 80 -	mA mA mA mA
I_{CC7}	L	Don't care	200	300	µA
I_{CCS}	L	Don't care	100	200	µA

I_{CC1}* : Operating current ($\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, Address cycling @tRC=min.)

I_{CC2} : Standby current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{IH})

I_{CC3}* : $\overline{RAS}$-only refresh current ($\overline{UCAS}$=$\overline{LCAS}$=V_{IH}, $\overline{RAS}$, Address cycling @tRC=min.)

I_{CC4}* : Hyper Page Mode current ($\overline{RAS}$=V_{IL}, $\overline{UCAS}$ or $\overline{LCAS}$, Address cycling @tHPC=min.)

I_{CC5} : Standby current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{CC}-0.2V)

I_{CC6}* : $\overline{CAS}$-before-$\overline{RAS}$ Refresh current ($\overline{RAS}$, $\overline{UCAS}$ or $\overline{LCAS}$ cycling @tRC=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode
Input high voltage(V_{IH})=Vcc-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{UCAS}$,$\overline{LCAS}$= 0.2V
Din = Don't care, T_{RC}= 125µs, T_{RAS}=T_{RAS}min~300 ns

I_{CCS} : Self refresh current
$\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=V_{IL}, $\overline{W}$=$\overline{OE}$=A0 ~ A8 = V_{CC}-0.2V or 0.2V,
DQ0 ~ DQ15= V_{CC}-0.2V, 0.2V or open

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1}, I_{CC3}, and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one hyper page cycle time, tHPC.

CAPACITANCE (T_A=25°C,Vcc=5V or 3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A8]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ0 - DQ15]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 1,2)

Test condition (5V device) : Vcc=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.0/0.8V
Test condition (3.3V device) : Vcc=3.3V±0.3V, V_{ih}/V_{il}=2.1/0.8V, V_{oh}/V_{ol}=2.0/0.8V

Parameter	Symbol	-5(*)		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	84		104		124		144		ns	
Read-modify-write cycle time	tRWC	116		140		165		190		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70		80	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		17		17		20		20	ns	3,4,5
Access time from column address	tAA		25		30		35		40	ns	3,10
$\overline{CAS}$ to output in Low-Z	tCLZ	3		3		3		3		ns	3
Output Buffer turn-off delay from $\overline{CAS}$	tCEZ	3	13	3	15	3	20	3	20	ns	6, 13
Transition time (rise and fall)	tT	2	50	2	50	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		60		ns	
$\overline{RAS}$ pulse width	tRAS	50	10K	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ hold time	tRSH	17		17		20		20		ns	
$\overline{CAS}$ hold time	tCSH	40		50		60		70		ns	
$\overline{CAS}$ pulse width	tCAS	8	10K	10	10K	15	10K	20	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	33	20	43	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	15	40	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	14
Column address hold time (5V)	tCAH	8		10		15		-		ns	14
Column address hold time (3.3V)	tCAH	-		15		15		15		ns	
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		0		ns	8
Write command set-up time	tWCS	0		0		0		0		ns	7
Write command hold time	tWCH	10		10		10		10		ns	
Write command pulse width	tWP	10		10		10		10		ns	
Write command to $\overline{RAS}$ lead time	tRWL	13		15		15		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	8		10		15		20		ns	17

(*) : 50ns product : Vcc=5V±5%

AC CHARACTERISTICS (0°C≤TA≤70°C, See note 1,2)

Parameter	Symbol	- 5(*)		- 6		- 7		- 8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		0		ns	9,20
Data hold time (5V)	tDH	8		10		15		-		ns	9,20
Data hold time (3.3V)	tDH	-		15		15		15		ns	
Refresh period (Normal)	tREF		8		8		8		8	ms	
Refresh period (L-ver)	tREF		128		128		128		128	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	34		36		44		44		ns	7,16
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	67		79		94		104		ns	7
Column address to $\overline{W}$ delay time	tAWD	42		49		59		64		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	45		54		64		69		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	5		5		5		5		ns	18
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		10		10		ns	19
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{CBR}$ counter test cycle)	tCPT	20		20		25		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		28		35		40		45	ns	3
Hyper Page mode cycle time	tHPC	20		25		30		35		ns	11
Hyper Page mode read-modify-write cycle time	tHPRWC	47		56		71		81		ns	11
$\overline{CAS}$ precharge time (Hyper page cycle)	tCP	8		10		10		10		ns	15
$\overline{RAS}$ pulse width (Hyper page cycle)	tRASP	50	100K	60	100K	70	100K	80	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		45		ns	
$\overline{OE}$ access time	tOEA		15		15		20		20	ns	3
$\overline{OE}$ to data delay	tOED	13		15		20		20		ns	
Output buffer turn off delay time from $\overline{OE}$	tOEZ	3	13	3	15	3	20	3	20	ns	6
$\overline{OE}$ command hold time	tOEH	13		15		20		20		ns	
Output data hold time	tDOH	5		5		5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	tREZ	3	15	3	15	3	20	3	20	ns	6,13
Output buffer turn off delay from $\overline{W}$	tWEZ	3	13	3	15	3	20	3	20	ns	6
$\overline{W}$ to data delay	tWED	13		15		20		20		ns	
$\overline{OE}$ to CAS hold time	tOCH	5		5		5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	tCHO	5		5		5		5		ns	
$\overline{OE}$ precharge time	tOEP	5		5		5		5		ns	
$\overline{W}$ pulse width (Hyper page cycle)	tWPE	5		5		5		5		ns	
$\overline{RAS}$ pulse width($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		100		μs	12
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	90		110		130		150		ns	12
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		-50		ns	12

(*) : 50ns product : Vcc=5V±5%

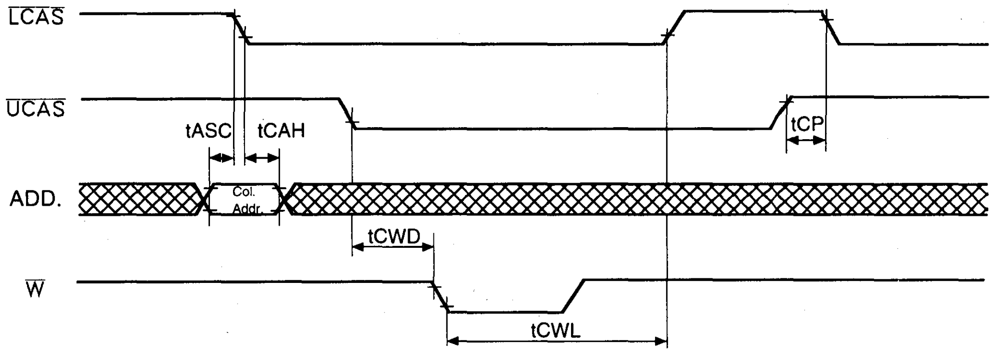
NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 2ns for all inputs.
3. Measured with a load equivalent to 2 TTL(5V)/1 TTL(3.3V) loads and 50pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS≥ tWCS(min), the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥ tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
11. tASC ≥ 6ns, Assume tT=2.0ns.
12. 512 cycle of burst refresh must be executed within 8ms before and after self refresh in order to meet refresh specification (L-version).

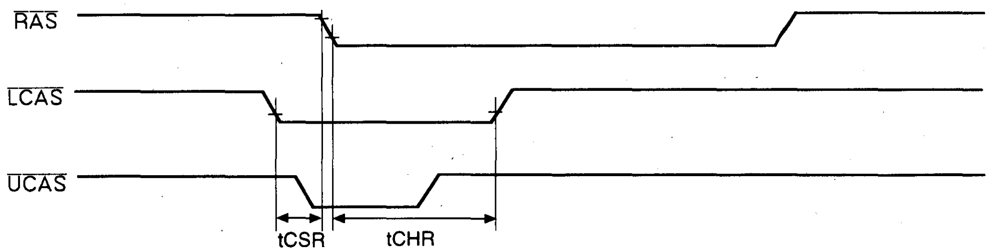
KM416C/V254B/BL Truth Table

$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	DQ0 -DQ7	DQ8 - DQ15	STATE
H	H	H	H	H	Hi-Z	Hi-Z	Standby
L	H	H	H	H	Hi-Z	Hi-Z	Refresh
L	L	H	H	L	DQ-OUT	Hi-Z	Byte Read
L	H	L	H	L	Hi-Z	DQ-OUT	Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-IN	-	Byte Write
L	H	L	L	H	-	DQ-IN	Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	Hi-Z	Hi-Z	-

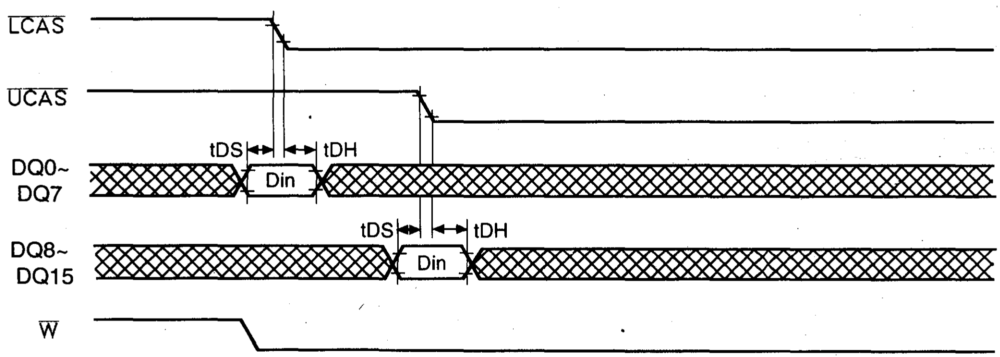
13. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ going.
14. tASC, tCAH are referenced to the earlier $\overline{CAS}$ falling edge.
15. tCP is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.
16. tCWD is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.
17. tCWL is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge



18. tCSR is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.
19. tCHR is referenced to the later $\overline{CAS}$ rising high after $\overline{RAS}$ transition low.



20. tDS, tDH is independently specified for lower byte DIN(0~7), upper byte DIN(8~15).



256K x 18 Bit CMOS Dynamic RAM with Fast Page Mode

DESCRIPTION

This is a family of 262,144 x 18 bit Fast Page Mode CMOS DRAMs. Fast Page Mode offers high speed random access of memory cells within the same row. Access time (-6, -7 or -8), power consumption (Normal or Low power) and package type (SOJ or TSOP-II) are optional features of this family.
All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities. Further more, Self-refresh operation is available in Low power version.
This 256Kx18 Fast Page Mode DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability.

FEATURES

- Part Identification
  - KM418C256B/BL (5V, 512 Ref.)

- Active Power Dissipation

Unit : mW

Speed	Active Power Dissipation
-6	525
-7	470
-8	440

- Refresh cycles

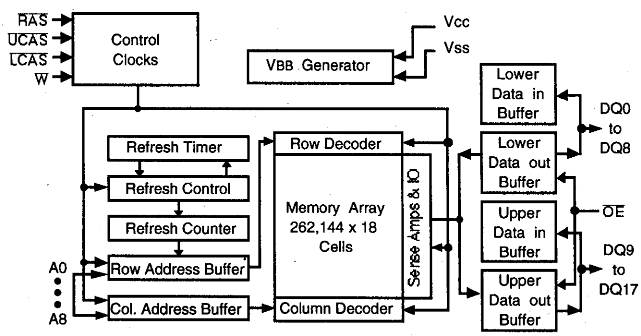
Part NO.	Refresh cycle	Refresh Period	
		Normal	L
C256B	512	8ms	128ms

- Performance range

Speed	tRAC	tCAC	tRC	tPC
-6	60ns	15ns	110ns	40ns
-7	70ns	20ns	130ns	45ns
-8	80ns	20ns	150ns	50ns

- Fast Page Mode operation
- 2 $\overline{CAS}$ Byte/Word Read/Write operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- Self-refresh capability (L-ver only)
- TTL compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC standard pinout
- Available in plastic SOJ and TSOP(II) packages
- Triple +5V±10% power supply

FUNCTIONAL BLOCK DIAGRAM



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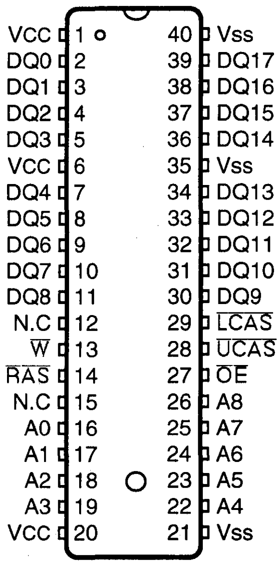
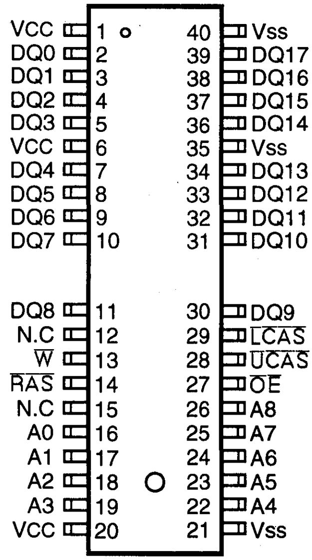
PIN CONFIGURATION (Top Views)

• KM418C256BJ



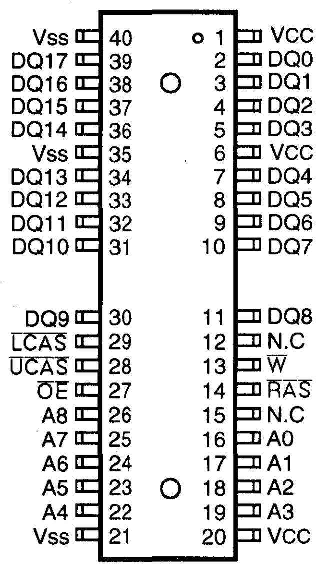
(SOJ)

• KM418C256BT



(TSOP(II)-Forward Type)

• KM418C256BTR



(TSOP(II)-Reverse Type)

2

Pin Name	Pin Function
A0 - A8	Address Inputs
DQ0 -17	Data In/Out
Vss	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Upper Column Address Strobe
$\overline{LCAS}$	Lower Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
Vcc	Power (+5V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 to +7.0	V
Voltage on Vcc supply relative to Vss	V_{CC}	-1.0 to +7.0	V
Storage Temperature	Tstg	-55 to +150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to Vss, T_A= 0 to 70 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	Vcc+1.0*1	V
Input Low Voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : Vcc+2.0V/20ns, Pulse width is measured at Vcc.

*2 : -2.0V/20ns, Pulse width is measured at Vss.

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input $0 \le V_{IN} \le Vcc+0.5V$, (Any input $0 \le V_{IN} \le Vcc+0.5V$, all other pins not under test=0V)	$I_{I(L)}$	-5	5	μA
Output Leakage Current (Data out is disabled, $0V \le V_{OUT} \le Vcc$)	$I_{O(L)}$	-5	5	μA
Output High Voltage Level (I_{OH}=-5mA)	V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=4.2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Symbol	Power	Speed	Max	Units
I_{CC1}	Don't care	-6 -7 -8	95 85 80	mA mA mA
I_{CC2}	Don't care	Don't care	2	mA
I_{CC3}	Don't care	-6 -7 -8	95 85 80	mA mA mA
I_{CC4}	Don't care	-6 -7 -8	60 55 50	mA mA mA
I_{CC5}	Normal L	Don't care	1 150	mA μA
I_{CC6}	Don't care	-6 -7 -8	95 85 80	mA mA mA
I_{CC7}	L	Don't care	300	μA
I_{CCS}	L	Don't care	200	μA

I_{CC1}* : Operating current ($\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, Address cycling @tRC=min.)

I_{CC2} : Standby current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{IH})

I_{CC3}* : $\overline{RAS}$-only refresh current ($\overline{UCAS}$=$\overline{LCAS}$=V_{IH}, $\overline{RAS}$, Address cycling @tRC=min.)

I_{CC4}* : Fast Page Mode current ($\overline{RAS}$=V_{IL}, $\overline{UCAS}$ or $\overline{LCAS}$, Address cycling @tPC=min.)

I_{CC5} : Standby current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{CC}-0.2V)

I_{CC6}* : $\overline{CAS}$-before-$\overline{RAS}$ Refresh current ($\overline{RAS}$, $\overline{UCAS}$ or $\overline{LCAS}$ cycling @tRC=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode
Input high voltage(V_{IH})=V_{CC}-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{UCAS}$,$\overline{LCAS}$= 0.2V
Din = Don't care, T_{RC}= 125μs, T_{RAS}=T_{RAS}min~300 ns

I_{CCS} : Self refresh current
$\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=V_{IL}, $\overline{W}$=$\overline{OE}$=A0 ~ A8 = V_{CC}-0.2V or 0.2V,
DQ0 ~ DQ17= V_{CC}-0.2V, 0.2V or open

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1}, I_{CC3}, and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one fast page mode cycle time tPC.

CAPACITANCE (T_A=25°C,Vcc=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A8]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ0 - DQ17]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 1,2)

Test condition : Vcc=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.4/0.4V

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	110		130		150		ns	
Read-modify-write cycle time	tRWC	155		185		205		ns	
Access time from $\overline{RAS}$	tRAC		60		70		80	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		15		20		20	ns	3,4,5
Access time from column address	tAA		30		35		40	ns	3,10
$\overline{CAS}$ to output in Low-Z	tCLZ	0		0		0		ns	3
Output buffer turn-off delay	tOFF	0	15	0	15	0	15	ns	7
Transition time (rise and fall)	tT	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	tRP	40		50		60		ns	
$\overline{RAS}$ pulse width	tRAS	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ hold time	tRSH	15		20		20		ns	
$\overline{CAS}$ hold time	tCSH	60		70		80		ns	
$\overline{CAS}$ pulse width	tCAS	15	10K	20	10K	20	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	30	15	35	15	40	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	
Column address hold time	tCAH	10		15		15		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		ns	8
$\overline{W}$rite command set-up time	tWCS	0		0		0		ns	7
Write command hold time	tWCH	10		10		10		ns	
Write command pulse width	tWP	10		10		10		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		15		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	15		15		20		ns	

AC CHARACTERISTICS (0°C≤TA≤70°C, See note 1,2)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		ns	9
Data hold time	tDH	10		15		15		ns	9
Refresh period (Normal)	tREF		8		8		8	ms	
Refresh period (L-ver)	tREF		128		128		128	ms	
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	tCWD	40		50		50		ns	7
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	tRWD	85		95		105		ns	7
Column address to $\overline{\text{W}}$ delay time	tAWD	55		60		65		ns	7
$\overline{\text{CAS}}$ precharge to $\overline{\text{W}}$ delay time	tCPWD	60		65		70			
$\overline{\text{CAS}}$ set-up time ($\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh)	tCSR	5		5		5		ns	
$\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh)	tCHR	10		10		10		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	tRPC	5		5		5		ns	
$\overline{\text{CAS}}$ precharge time($\overline{\text{CBR}}$ counter test cycle)	tCPT	20		25		30		ns	
Access time from $\overline{\text{CAS}}$ precharge	tCPA		35		40		45	ns	3
Fast Page mode cycle time	tPC	40		45		50		ns	
Fast Page mode read-modify-write cycle time	tPRWC	85		95		105		ns	
$\overline{\text{CAS}}$ precharge time (Fast page cycle)	tCP	10		10		10		ns	
$\overline{\text{RAS}}$ pulse width (Fast page cycle)	tRASP	60	100K	70	100K	80	100K	ns	
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	tRHCP	35		40		45		ns	
$\overline{\text{OE}}$ access time	tOEA		15		20		20	ns	
$\overline{\text{OE}}$ to data delay	tOED	15		20		20		ns	
Out put buffer turn off delay time from $\overline{\text{OE}}$	tOEZ	0	15	0	20	0	20	ns	
$\overline{\text{OE}}$ command hold time	tOEH	15		20		20		ns	
$\overline{\text{RAS}}$ pulse width($\overline{\text{C}}$-B-$\overline{\text{R}}$ self refresh)	tRASS	100		100		100		μs	11
$\overline{\text{RAS}}$ precharge time ($\overline{\text{C}}$-B-$\overline{\text{R}}$ self refresh)	tRPS	110		130		150		ns	11
$\overline{\text{CAS}}$ hold time ($\overline{\text{C}}$-B-$\overline{\text{R}}$ self refresh)	tCHS	-50		-50		-50		ns	11

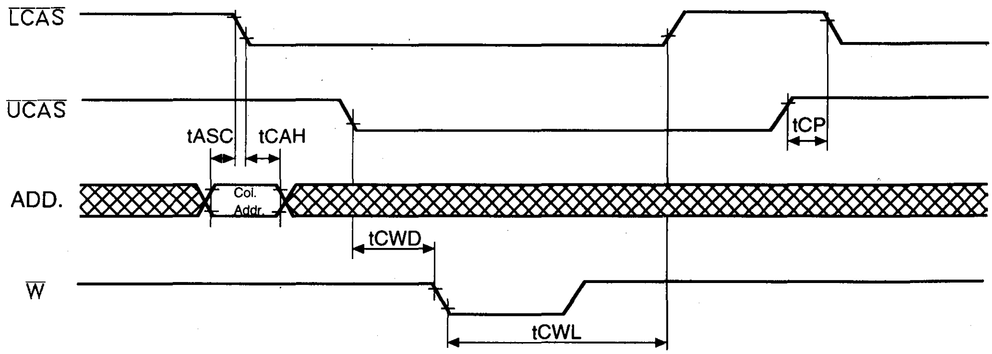
NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS≥ tWCS(min), the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥ tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.

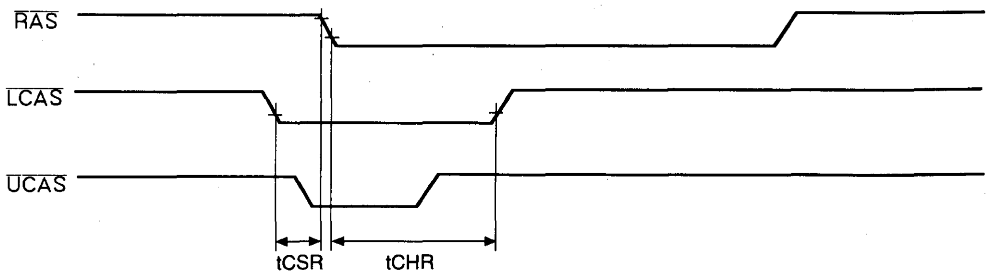
KM418C256B/BL Truth Table

$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	DQ0 -DQ8	DQ9 - DQ17	STATE
H	H	H	H	H	Hi-Z	Hi-Z	Standby
L	H	H	H	H	Hi-Z	Hi-Z	Refresh
L	L	H	H	L	DQ-OUT	Hi-Z	Byte Read
L	H	L	H	L	Hi-Z	DQ-OUT	Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-IN	-	Byte Write
L	H	L	L	H	-	DQ-IN	Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	Hi-Z	Hi-Z	-

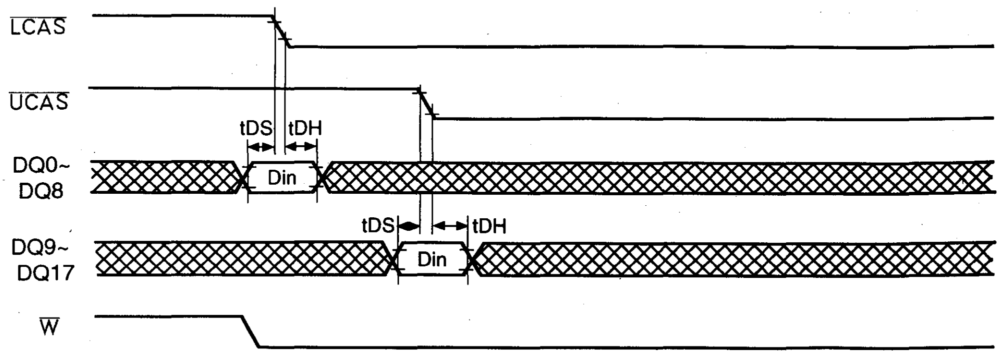
11. 512 cycle of burst refresh must be executed within 8ms before and after self refresh in order to meet refresh specification (L-version).
12. tASC, tCAH are referenced to the earlier $\overline{CAS}$ falling edge.
13. tCP is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.
14. tCWD is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.
15. tCWL is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge



16. tCSR is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.
17. tCHR is referenced to the later $\overline{CAS}$ rising high after $\overline{RAS}$ transition low.



18. tDS, tDH is independently specified for lower byte DIN (0~8), upper byte DIN(9~17).



2

16M DRAM

- KM41C16000A
  KM41V16000A
- KM41C16002A
- KM44C4000A, KM44C4100A
  KM44V4000A, KM44V4100A
- KM44C4002A
  KM44C4102A
- KM44C4003A
  KM44C4103A
- KM44C4004A, KM44C4104A
  KM44V4004A, KM44V4104A
- KM44C4010A
  KM44C4110A
- KM48C2000A, KM48C2100A
  KM48V2000A, KM48V2100A
- KM48C2004A, KM48C2104A
  KM48V2004A, KM48V2104A
- KM416C1000A, KM416C1200A
  KM416V1000A, KM416V1200A
- KM416C1004A, KM416C1204A
  KM416V1004A, KM416V1204A
- KM432V502
  KM432V522
- KM432V504
  KM432V524

16M x 1 Bit CMOS Dynamic RAM with Fast Page Mode

DESCRIPTION

This is a family of 16,777,216 x 1 bit Fast Page Mode CMOS DRAMs. Fast Page Mode offers high speed random access of memory cells within the same row. Power supply voltage(+5.0V or +3.3V), access time(-5, -6, -7 or -8), power consumption(Normal, Low power or Super-Low power) and package type(SOJ or TSOP-II) are optional features of this family. All of this family have $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$-only refresh and Hidden refresh capabilities. Further more, Self-refresh operation is available in L & SL version.
This 16Mx1 Fast Page mode DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability. It may be used as main memory unit for high level computer and microcomputer.

FEATURES

- Part Identification
  - KM41C16000A/AL/ASL (5V, 4K Ref.)
  - KM41V16000A/AL/ASL (3.3V, 4K Ref.)

- Active Power Dissipation

Unit : mW

Speed	3.3V	5V
-5	-	495
-6	288	440
-7	252	385
-8	216	330

- Refresh cycles

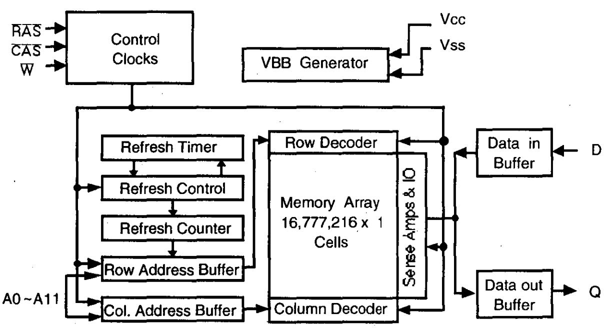
Part NO.	Vcc	Refresh cycle	Refresh period		
			Normal	L	SL
C16000A	5V	4K	64ms	128ms	256ms
V16000A	3.3V				

- Performance range:

Speed	tRAC	tCAC	tRC	tPC	Remark
-5	50ns	13ns	90ns	35ns	5V Only
-6	60ns	15ns	110ns	40ns	5V/3.3V
-7	70ns	20ns	130ns	45ns	5V/3.3V
-8	80ns	20ns	150ns	50ns	5V/3.3V

- Fast Page Mode operation
- $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh capability
- $\overline{\text{RAS}}$-only and Hidden refresh capability
- Self-refresh capability(L & SL-ver)
- Fast parallel test mode capability
- TTL(5V)/LVTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC Standard pinout
- Available in Plastic SOJ and TSOP(II) packages
- Single +5V±10% power supply(5V product)
- Single +3.3V±0.3V power supply(3.3V product)

FUNCTIONAL BLOCK DIAGRAM



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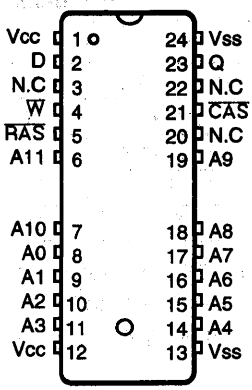
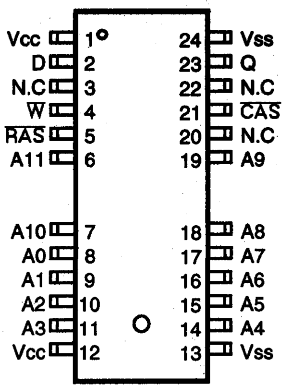
PIN CONFIGURATION (Top Views)

• KM41C/V16000AJ



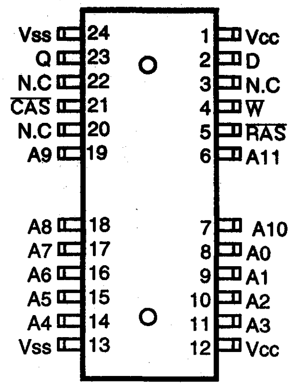
J : 400 mil 24(28) SOJ

• KM41C/V16000AT



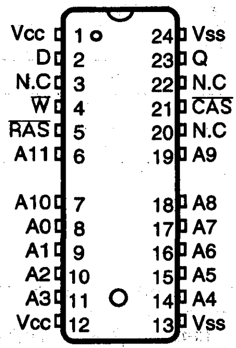
T : 400 mil 24(28) TSOP II

• KM41C/V16000ATR



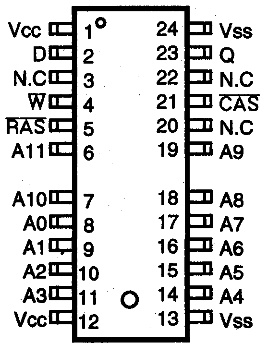
TR : 400 mil 24(28) TSOP II(Rev.)

• KM41C/V16000AK



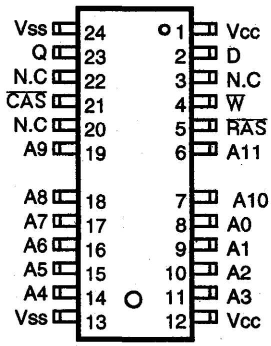
K : 300 mil 24(26) SOJ

• KM41C/V16000AS



S : 300 mil 24(26) TSOP II

• KM41C/V16000ASR



SR : 300 mil 24(26) TSOP II(Rev.)

Pin Name	Pin Function
A0 - A11	Address Inputs
D	Data in
Q	Data out
Vss	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
Vcc	Power(+5.0V)
	Power(+3.3V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Units
		3.3V	5V	
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-0.5 to +4.6	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	V_{CC}	-0.5 to +4.6	-1 to +7.0	V
Storage Temperature	Tstg	-55 to +150	-55 to +150	°C
Power Dissipation	P_D	1	1	W
Short Circuit Output Current	I_{OS}	50	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to Vss, T_A= 0 to 70 °C)

Parameter	Symbol	3.3V			5V			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V_{CC}	3.0	3.3	3.6	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	Vcc+0.3*1	2.4	-	Vcc+1*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	-1.0*2	-	0.8	V

*1 : Vcc + 1.3V/15ns(3.3V), Vcc+2.0V/20ns(5V), Pulse width is measured at Vcc.
*2 : - 1.3V/15ns(3.3V), - 2.0V/20ns(5V), Pulse width is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

	Parameter	Symbol	Min	Max	Units
3.3V	Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.3V, all other pins not under test=0 volt.)	$I_{I(L)}$	-5	5	μA
	Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	-5	5	μA
	Output High Voltage Level(I_{OH}=-2mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level(I_{OL}=2mA)	V_{OL}	-	0.4	V
5V	Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 volt.)	$I_{I(L)}$	-5	5	μA
	Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	-5	5	μA
	Output High Voltage Level(I_{OH}=-5mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level(I_{OL}=4.2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS (Continued.)

Symbol	Power	Speed	Max		Units
			KM41V16000A	KM41C16000A	
ICC1	Don't care	-5 -6 -7 -8	- 80 70 60	90 80 70 60	mA mA mA mA
ICC2	Normal L/SL	Don't care	2 1	2 1	mA mA
ICC3	Don't care	-5 -6 -7 -8	- 80 70 60	90 80 70 60	mA mA mA mA
ICC4	Don't care	-5 -6 -7 -8	- 70 60 50	80 70 60 50	mA mA mA mA
ICC5	Normal L SL	Don't care	1 300 200	1 300 200	mA µA µA
ICC6	Don't care	-5 -6 -7 -8	- 80 70 60	90 80 70 60	mA mA mA mA
ICC7	L SL	Don't care	450 350	450 350	µA µA
ICCS	L/SL	Don't care	250	300	µA

ICC1* : Operating Current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

ICC2 : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

ICC3* : $\overline{RAS}$-only Refresh Current ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @tRC=min.)

ICC4* : Fast Page Mode Current ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address cycling @tPC=min.)

ICC5 : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

ICC6* : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

ICC7 : Battery back-up current, Average power supply current, Battery back-up mode
Input high voltage(V_{IH})=Vcc-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{CAS}$= 0.2V
Din = Don't care, T_{RC}= 31.25µs(L-ver), 62.5µs(SL-ver), T_{RAS}=T_{RAS}min~300 ns

ICCS : Self Refresh Current
$\overline{RAS}$=$\overline{CAS}$=0.2V, $\overline{W}$=A0 ~ A11 = Vcc-0.2V or 0.2V, D,Q = Vcc-0.2V, 0.2V or Open

* NOTE : ICC1, ICC3, ICC4 and ICC6 are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In ICC1, ICC3, and ICC6, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In ICC4, address can be changed maximum once within one fast page mode cycle time tPC.

CAPACITANCE(T_A=25°C,Vcc=5V or 3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [D]	C_{IN1}	-	7	pF
Input capacitance [A0 - A11]	C_{IN2}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$]	C_{IN3}	-	7	pF
Output Capacitance [Q]	C_{OUT}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 1,2)
Test condition(5V device) : Vcc=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.4/0.4V
Test condition(3.3V device) : Vcc=3.3V±0.3V, V_{ih}/V_{il}=2.0/0.8V, V_{oh}/V_{ol}=2.0/0.8V

Parameter	Symbol	-5 *1		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		130		150		ns	
Read-modify-write cycle time	tRWC	110		130		155		175		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70		80	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		13		15		20		20	ns	3,4,5
Access time from column address	tAA		25		30		35		40	ns	3,10
$\overline{CAS}$ to output in Low-Z	tCLZ	0		0		0		0		ns	3
Output buffer turn-off delay	tOFF	0	13	0	15	0	20	0	20	ns	6
Transition time (rise and fall)	tT	3	50	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		60		ns	
$\overline{RAS}$ pulse width	tRAS	50	10K	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ hold time	tRSH	13		15		20		20		ns	
$\overline{CAS}$ hold time	tCSH	50		60		70		80		ns	
$\overline{CAS}$ pulse width	tCAS	13	10K	15	10K	20	10K	20	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	37	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	15	40	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	
Column address hold time	tCAH	10		10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	tAR	40		45		55		60		ns	15
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		0		ns	
Write command hold time	tWCH	10		10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	tWCR	40		45		55		60		ns	15
Write command pulse width	tWP	10		10		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		15		20		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	13		15		20		20		ns	

Note) *1 : 5V only

AC CHARACTERISTICS (Continuecd)

Parameter	Symbol	-5 *1		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		0		ns	9
Data hold time	tDH	10		10		15		15		ns	9
Data hold time referenced to $\overline{RAS}$	tDHR	40		45		55		60		ns	15
Refresh period(Normal)	tREF		64		64		64		64	ms	
Refresh period(L-ver)	tREF		128		128		128		128	ms	
Refresh period(SL-ver)	tREF		256		256		256		256	ms	
Write command set-up time	tWCS	0		0		0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	13		15		20		20		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	50		60		70		80		ns	7
Column address to $\overline{W}$ delay time	tAWD	25		30		35		40		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	30		35		40		45		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	5		5		5		5		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		5		ns	
$\overline{CAS}$ precharge time($\overline{CBR}$ counter test cycle)	tCPT	20		20		30		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		30		35		40		45	ns	3
Fast Page mode cycle time	tPC	35		40		45		50		ns	
Fast Page mode read-modify-write cycle time	tPRWC	53		60		70		80		ns	
$\overline{CAS}$ precharge time (Fast page cycle)	tCP	10		10		10		10		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	50	200K	60	200K	70	200K	80	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		45		ns	
Write command set-up time(Test mode in)	tWTS	10		10		10		10		ns	11
Write command hold time(Test mode in)	tWTH	10		10		10		10		ns	11
$\overline{W}$ to $\overline{RAS}$ precharge time($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		10		ns	
$\overline{RAS}$ pulse width($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		100		us	14
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	90		110		130		150		ns	14
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		-50		ns	14

Note) *1 : 5V only

TEST MODE CYCLE

(Note. 11)

Parameter	Symbol	-5*1		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	95		115		135		155		ns	
Read-modify-write cycle time	tRWC	138		160		190		210		ns	
Access time from $\overline{RAS}$	tRAC		55		65		75		85	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		18		20		25		25	ns	3,4,5
Access time from column address	tAA		30		35		40		45	ns	3,10
$\overline{RAS}$ pulse width	tRAS	55	10K	65	10K	75	10K	85	10K	ns	
$\overline{CAS}$ pulse width	tCAS	18	10K	20	10K	25	10K	25	10K	ns	
$\overline{RAS}$ hold time	tRSH	18		20		25		25		ns	
$\overline{CAS}$ hold time	tCSH	55		65		75		85		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		45		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	18		20		25		25		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	55		65		75		85		ns	7
Column address to $\overline{W}$ delay time	tAWD	30		35		40		45		ns	7
Fast Page mode cycle time	tPC	40		45		50		55		ns	
Fast page mode read-modify-write cycle time	tPRWC	58		65		75		85		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	55	200K	65	200K	75	200K	85	200K	ns	
Access time form $\overline{CAS}$ precharge	tCPA		35		40		45		50	ns	3

Note) *1 : 5V only

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL(5V device)/1 TTL(3.3V device) loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If tWCS≥tWCS(min), the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a re ference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
11. These specifications are applied in the test mode.
12. In test mode read cycle, the value of tRAC, tAA, tCAC is delayed by 2ns to 5ns for the specified values. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
13. tOFF(max) defines the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
14. 4096 cycles of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.
15. tAR, tWCR, and tDHR are referenced to tRAD(MAX).

16M x 1Bit CMOS Dynamic RAM with Static Column Mode

DESCRIPTION

This is a family of 16,777,216 x 1 bit Static Column Mode CMOS DRAMs. Static Column Mode offers high speed random access of memory cells within the same row. Access time(-5, -6, -7 or -8) and package type (SOJ or TSOP-II) are optional features of this family.
All of this family have $\overline{\text{CS}}$-before-$\overline{\text{RAS}}$ Refresh, $\overline{\text{RAS}}$-only refresh and Hidden Refresh capabilities.
This 16Mx1 Static Column Mode DRAM Family is fabricated using Samsung's advanced CMOS process to realize high band-width and high reliability. It may be used as main memory unit for high level computer and high performance microprocessor systems.

FEATURES

- Part Identification
  - KM41C16002A(5V, 4K Ref.)

- Active Power Dissipation

Unit : mW

Speed	Power dissipation
-5	495
-6	440
-7	385
-8	330

- Refresh cycles

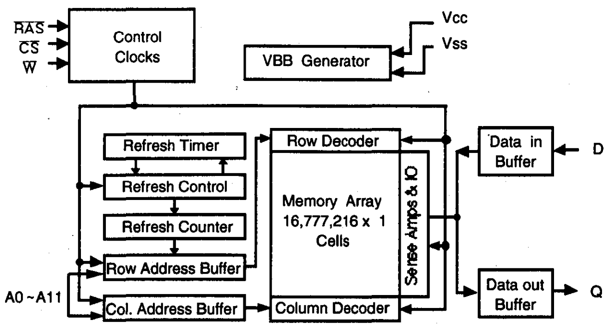
	Refresh cycle	Refresh Period
KM41C16002A	4K	64ms

- Performance range:

Speed	tRAC	tCAC	tRC	tSC
-5	50ns	13ns	90ns	30ns
-6	60ns	15ns	110ns	35ns
-7	70ns	20ns	130ns	40ns
-8	80ns	20ns	150ns	45ns

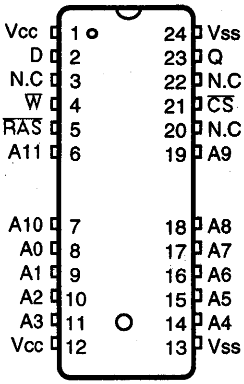
- Static Column Mode operation
- $\overline{\text{CS}}$-before-$\overline{\text{RAS}}$ refresh capability
- RAS-only and Hidden refresh capability
- Fast parallel test mode capability
- TTL compatible inputs and outputs
- Early Write or Output enable controlled write
- JEDEC Standard pinout
- Available in Plastic SOJ and TSOP(II) packages
- Single +5V±10% power supply

FUNCTIONAL BLOCK DIAGRAM



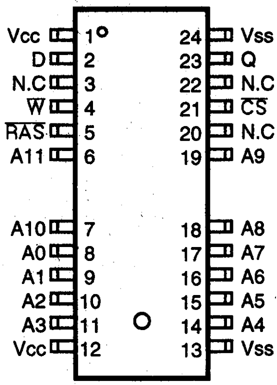
PIN CONFIGURATION (Top Views)

• KM41C16002AJ



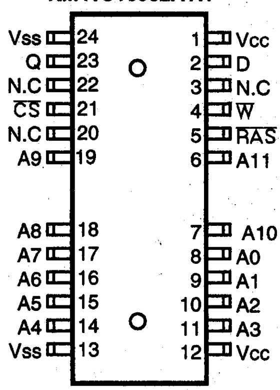
J : 400 mil 24(28) SOJ

• KM41C16002AT



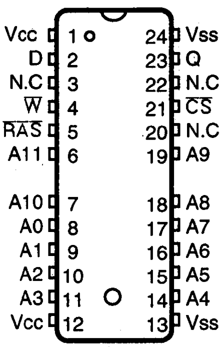
T : 400 mil 24(28) TSOP II

• KM41C16002ATR



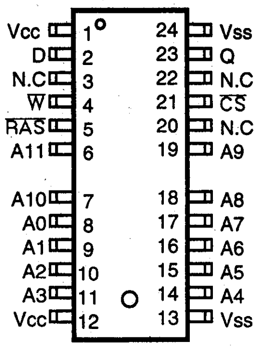
TR : 400 mil 24(28) TSOP II(Rev.)

• KM41C16002AK



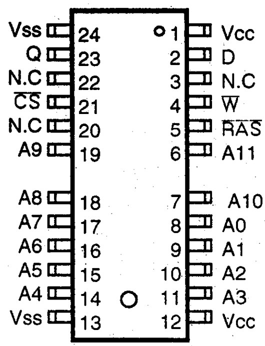
K : 300 mil 24(26) SOJ

• KM41C16002AS



S : 300 mil 24(26) TSOP II

• KM41C16002ASR



SR : 300 mil 24(26) TSOP II(Rev.)

Pin Name	Pin Function
A0 - A11	Address Inputs
D	Data in
Q	Data out
Vss	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Chip select input
$\overline{W}$	Read/Write Input
Vcc	Power(+5.0V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	V_{CC}	-1 to +7.0	V
Storage temperature	Tstg	-55 to +150	°C
Power dissipation	P_D	1	W
Short circuit output current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to Vss, T_A= 0 to 70 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input high voltage	V_{IH}	2.4	-	Vcc+1.0*1	V
Input low voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : Vcc+2.0V at pulse width ≤ 20ns (pulse width is measured at Vcc)

*2 : -2.0V at pulse width ≤ 20ns (pulse width is measured at Vss)

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Units
Input leakage current (Any input $0 \le V_{IN} \le Vcc+0.5V$ all other pins not under test=0 volts.)	$I_{I(L)}$	- 5	5	µA
Output leakage current (Data out is disabled, $0V \le V_{OUT} \le Vcc$)	$I_{O(L)}$	- 5	5	µA
Output high voltage level(I_{OH}=-5mA)	V_{OH}	2.4	-	V
Output low voltage level(I_{OL}=4.2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS (Continued)

Symbol	Speed	Max KM41C16002A	Units
I_{CC1}	-5 -6 -7 -8	90 80 70 60	mA mA mA mA
I_{CC2}	Don't care	2	mA
I_{CC3}	-5 -6 -7 -8	90 80 70 60	mA mA mA mA
I_{CC4}	-5 -6 -7 -8	80 70 60 50	mA mA mA mA
I_{CC5}	Don't care	1	mA
I_{CC6}	-5 -6 -7 -8	90 80 70 60	mA mA mA mA

I_{CC1} *: Operating current ($\overline{RAS}$ and $\overline{CS}$ cycling @tRC=min.)

I_{CC2} : Standby current ($\overline{RAS}$=$\overline{CS}$=$\overline{W}$=V_{IH})

I_{CC3} *: $\overline{RAS}$-only refresh current ($\overline{CS}$=V_{IH}, $\overline{RAS}$,Address cycling @tRC=min.)

I_{CC4} *: Static Column Mode current ($\overline{RAS}$=V_{IL}, $\overline{CS}$, Address cycling @tSC=min.)

I_{CC5} : Standby current ($\overline{RAS}$=$\overline{CS}$=$\overline{W}$=V_{CC}-0.2V)

I_{CC6} *: $\overline{CS}$-before-$\overline{RAS}$ refresh current ($\overline{RAS}$ and $\overline{CS}$ cycling @tRC=min.)

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} , I_{CC3} and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one Static Column mode cycle time tSC.

CAPACITANCE(T_A=25°C,Vcc=5V , f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A9]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{CS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ0 - DQ3]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 1,2)
Test condition : Vcc=5.0V±10%, Vih/Vil = 2.4/0.8V, Voh/Vol = 2.4/0.4V

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		130		150		ns	
Read-modify-write cycle time	tRWC	110		130		155		175		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70		80	ns	3,4,10
Access time from $\overline{CS}$	tCAC		13		15		20		20	ns	3,4,5
Access time from column address	tAA		25		30		35		40	ns	3,10
$\overline{CS}$ to output in Low-Z	tCLZ	0		0		0		0		ns	3
Output buffer turn-off delay from $\overline{CS}$	tOFF	0	13	0	15	0	20	0	20	ns	6
Transition time (rise and fall)	tT	3	50	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		60		ns	
$\overline{RAS}$ pulse width	tRAS	50	10K	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ hold time	tRSH	13		15		20		20		ns	
$\overline{CS}$ hold time	tCSH	50		60		70		80		ns	
$\overline{CS}$ pulse width	tCS	13	10K	15	10K	20	10K	20	10K	ns	
$\overline{RAS}$ to $\overline{CS}$ delay time	tRCD	20	37	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	15	40	ns	10
$\overline{CS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	
Column address hold time	tCAH	10		10		15		15		ns	
Column address hold time	tAR	40		50		55		60		ns	14
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{CS}$	tRCH	0		0		0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		0		ns	8
Write command hold time	tWCH	10		10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	tWCR	40		45		55		60		ns	14
Write command pulse width	tWP	10		10		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		15		20		20		ns	
Write command to $\overline{CS}$ lead time	tCWL	13		15		20		20		ns	
Data set-up time	tDS	0		0		0		0		ns	9

AC CHARACTERISTICS (Continued)

Parameter	Symbol	- 5		- 6		- 7		- 8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Data hold time	tDH	10		10		15		15		ns	9
Data hold time referenced to $\overline{RAS}$	tDHR	40		45		55		60		ns	14
Refresh period	tREF		64		64		64		64	ms	
Write command set-up time	tWCS	0		0		0		0		ns	7
$\overline{CS}$ to $\overline{W}$ delay time	tCWD	13		15		20		20		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	50		60		70		80		ns	7
Column address to $\overline{W}$ delay time	tAWD	25		30		35		40		ns	7
$\overline{CS}$ set-up time ($\overline{CS}$-before-$\overline{RAS}$ refresh)	tCSR	5		5		5		5		ns	
$\overline{CS}$ hold time ($\overline{CS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		10		10		ns	
$\overline{RAS}$ to $\overline{CS}$ precharge time	tRPC	5		5		5		5		ns	
$\overline{CS}$ precharge time($\overline{C}$-B-$\overline{R}$ counter test cycle)	tCPT	20		20		30		30		ns	
Static Column mode cycle time	tSC	30		35		40		45		ns	
Static Column mode read-modify-write cycle time	tSRWC	53		60		70		80		ns	
Access time from last write	tALW		50		55		65		75	ns	3,11
Output data hold time from column address	tAOH	5		5		5		5		ns	
Output data enable time from $\overline{W}$	tOW		35		40		45		55	ns	
$\overline{CS}$ precharge time (Static Column cycle)	tCP	10		10		10		10		ns	
$\overline{RAS}$ pulse width (Static Column cycle)	tRASC	50	200K	60	200K	70	200K	80	100K	ns	
$\overline{CS}$ pulth width (Static Column cycle)	tCSC	13	200K	15	200K	20	200K	20	200K	ns	
Column address hold time referenced to $\overline{RAS}$ rising	tAH	5		5		5		5		ns	
Last write to column address delay time	tLWAD	20	25	20	25	25	30	25	35	ns	
Last write to column address hold time	tAHLW	50		55		65		75		ns	
Write command inactive time	tWI	10		10		10		10		ns	
Write address hold time referenced to $\overline{RAS}$	tAWR	40		45		55		60		ns	
Write command set-up time(Test mode in)	tWTS	10		10		10		10		ns	
Write command hold time(Test mode in)	tWTH	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		10		ns	

TEST MODE CYCLE

(Note. 11)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	95		115		135		155		ns	
Read-modify-write cycle time	tRWC	140		160		190		210		ns	
Access time from $\overline{\text{RAS}}$	tRAC		55		65		75		85	ns	3,4,10
Access time from $\overline{\text{CS}}$	tCAC		18		20		25		25	ns	3,4,5
Access time from column address	tAA		30		35		40		45	ns	3,10
$\overline{\text{RAS}}$ pulse width	tRAS	55	10K	65	10K	75	10K	85	10K	ns	
$\overline{\text{CS}}$ pulse width	tCS	18	10K	20	10K	25	10K	25	10K	ns	
$\overline{\text{RAS}}$ hold time	tRSH	20		20		25		25		ns	
$\overline{\text{CS}}$ hold time	tCSH	55		65		75		85		ns	
Column address to $\overline{\text{RAS}}$ lead time	tRAL	30		35		40		45		ns	
$\overline{\text{CS}}$ to $\overline{\text{W}}$ delay time	tCWD	18		20		25		25		ns	7
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	tRWD	55		65		75		85		ns	7
Column address to $\overline{\text{W}}$ delay time	tAWD	30		35		40		45		ns	7
Static Column mode cycle time	tSC	35		40		45		50		ns	
Static Column mode read-modify-write cycle time	tSRWC	58		65		75		85		ns	
$\overline{\text{RAS}}$ pulse width (Static Column cycle)	tRASC	55	200K	65	200K	75	200K	85	200K	ns	
Access time form last write	tALW		55		60		70		80	ns	3,11

NOTES

1. An initial pause of 200µs is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If tWCS≥tWCS(min), the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a re ference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
11. These specifications are applied in the test mode.
12. In test mode read cycle, the value of tRAC, tAA, tCAC is delayed by 2ns to 5ns for the specified values. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
13. tOFF(max) defines the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
14. tAR, tWCR, and tDHR are referenced to tRAD(MAX).

4M x 4 Bit CMOS Dynamic RAM with Fast Page Mode

DESCRIPTION

This is a family of 4,194,304 x 4 bit Fast Page Mode CMOS DRAMs. Fast Page Mode offers high speed random access of memory cells within the same row. Power supply voltage(+5.0V or +3.3V), refresh cycle(2K Ref. or 4K Ref.), access time(-5, -6, -7 or -8), power consumption(Normal, Low power or Super-Low power) and package type(SOJ or TSOP-II) are optional features of this family. All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities. Further more, Self-refresh operation is available in L & SL version.

This 4Mx4 Fast Page mode DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability. It may be used as main memory unit for high level computer, microcomputer and personal computer.

2

FEATURES

- Part Identification
  - KM44C4000A/AL/ASL (5V, 4K Ref.)
  - KM44C4100A/AL/ASL (5V, 2K Ref.)
  - KM44V4000A/AL/ASL (3.3V, 4K Ref.)
  - KM44V4100A/AL/ASL (3.3V, 2K Ref.)

- Active Power Dissipation

Unit : mW

Speed	3.3V		5V	
	4K	2K	4K	2K
-5	-	-	495	605
-6	288	360	440	550
-7	252	324	385	495
-8	216	288	330	440

- Refresh cycles

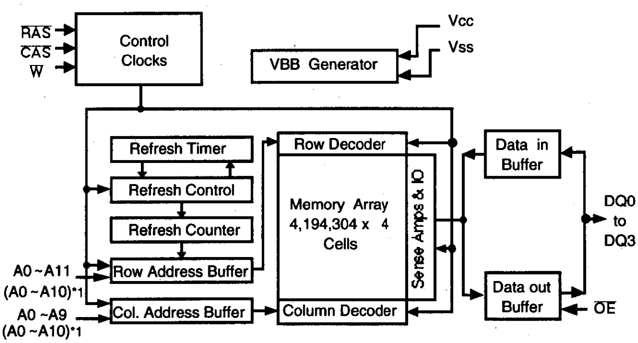
Part NO.	Vcc	Refresh cycle	Refresh period		
			Normal	L	SL
C4000A	5V	4K	64ms	128ms	256ms
V4000A	3.3V				
C4100A	5V	2K	32ms		
V4100A	3.3V				

- Performance range:

Speed	tRAC	tCAC	tRC	tPC	Remark
-5	50ns	13ns	90ns	35ns	5V Only
-6	60ns	15ns	110ns	40ns	5V/3.3V
-7	70ns	20ns	130ns	45ns	5V/3.3V
-8	80ns	20ns	150ns	50ns	5V/3.3V

- Fast Page Mode operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- Self-refresh capability(L & SL - ver)
- Fast parallel test mode capability
- TTL(5V)/LVTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC Standard pinout
- Available in Plastic SOJ and TSOP(II) packages
- Single +5V±10% power supply(5V product)
- Single +3.3V±0.3V power supply(3.3V product)

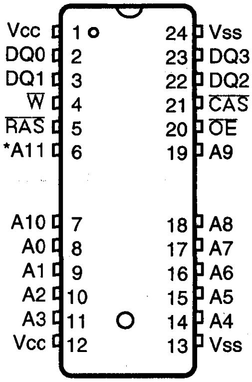
FUNCTIONAL BLOCK DIAGRAM



Note) *1 : 2K Refresh

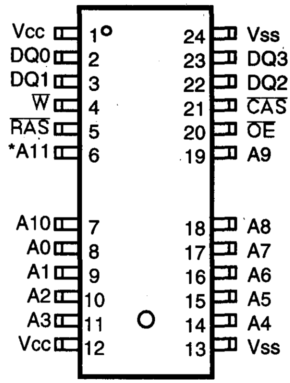
PIN CONFIGURATION (Top Views)

• KM44C/V40(1)00AJ



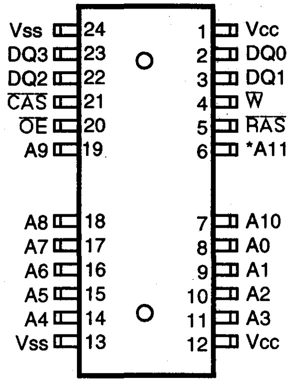
J : 400 mil 24(28) SOJ

• KM44C/V40(1)00AT



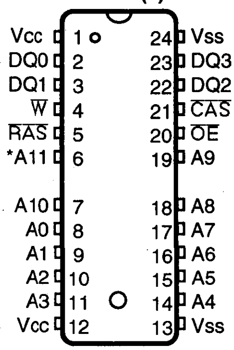
T : 400 mil 24(28) TSOP II

• KM44C/V40(1)00ATR



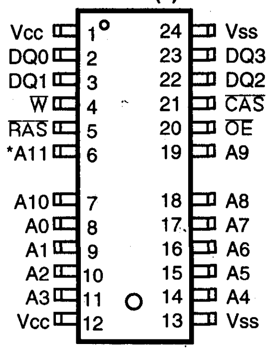
TR : 400 mil 24(28) TSOP II(Rev.)

• KM44C/V40(1)00AK



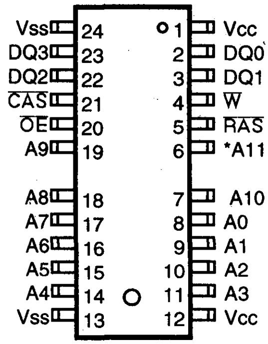
K : 300 mil 24(26) SOJ

• KM44C/V40(1)00AS



S : 300 mil 24(26) TSOP II

• KM44C/V40(1)00ASR



SR : 300 mil 24(26) TSOP II(Rev.)

* A11 is N.C for KM44C/V4100A(5V/3.3V, 2K Ref. product)

Pin Name	Pin Function
A0 - A11	Address Inputs(4K Product)
A0 - A10	Address Inputs(2K Product)
DQ0 -3	Data In/Out
V_{SS}	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Outputs Enable
V_{CC}	Power(+5.0V)
	Power(+3.3V)
N.C	No Connection(2K Refresh)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Units
		3.3V	5V	
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to +4.6	-1 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.5 to +4.6	-1 to +7.0	V
Storage Temperature	Tstg	-55 to +150	-55 to +150	°C
Power Dissipation	P_D	1	1	W
Short Circuit Output Current	I_{OS}	50	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A= 0 to 70 °C)

Parameter	Symbol	3.3V			5V			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V_{CC}	3.0	3.3	3.6	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	V_{CC}+0.3*1	2.4	-	V_{CC}+1*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	-1.0*2	-	0.8	V

*1 : Vcc + 1.3V/15ns(3.3V), Vcc+2.0V/20ns(5V), Pulse width is measured at Vcc.
*2 : - 1.3V/15ns(3.3V), - 2.0V/20ns(5V), Pulse width is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

	Parameter	Symbol	Min	Max	Units
3.3V	Input Leakage Current (Any input $0 \le V_{IN} \le V_{CC}+0.3V$, all other pins not under test=0 volt.)	$I_{I(L)}$	- 5	5	µA
	Output Leakage Current (Data out is disabled, $0V \le V_{OUT} \le V_{CC}$)	$I_{O(L)}$	- 5	5	µA
	Output High Voltage Level(I_{OH}=-2mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level(I_{OL}=2mA)	V_{OL}	-	0.4	V
5V	Input Leakage Current (Any input $0 \le V_{IN} \le V_{CC}+0.5V$, all other pins not under test=0 volt.)	$I_{I(L)}$	- 5	5	µA
	Output Leakage Current (Data out is disabled, $0V \le V_{OUT} \le V_{CC}$)	$I_{O(L)}$	- 5	5	µA
	Output High Voltage Level(I_{OH}=-5mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level(I_{OL}=4.2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS (Continued.)

Symbol	Power	Speed	Max				Units
			KM44V4000A	KM44V4100A	KM44C4000A	KM44C4100A	
ICC1	Don't care	-5 -6 -7 -8	- 80 70 60	- 100 90 80	90 80 70 60	110 100 90 80	mA mA mA mA
ICC2	Normal L/SL	Don't care	2 1	2 1	2 1	2 1	mA mA
ICC3	Don't care	-5 -6 -7 -8	- 80 70 60	- 100 90 80	90 80 70 60	110 100 90 80	mA mA mA mA
ICC4	Don't care	-5 -6 -7 -8	- 70 60 50	- 80 70 60	80 70 60 50	90 80 70 60	mA mA mA mA
ICC5	Normal L SL	Don't care	1 300 200	1 300 200	1 300 200	1 300 200	mA µA µA
ICC6	Don't care	-5 -6 -7 -8	- 80 70 60	- 100 90 80	90 80 70 60	110 100 90 80	mA mA mA mA
ICC7	L SL	Don't care	450 350	400 300	450 350	400 300	µA µA
ICCS	L/SL	Don't care	250	250	300	300	µA

I_{CC1}* : Operating Current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}* : $\overline{RAS}$-only Refresh Current ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @tRC=min.)

I_{CC4}* : Fast Page Mode Current ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address cycling @tPC=min.)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)

I_{CC6}* : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode
Input high voltage(V_{IH})=V_{CC}-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{CAS}$= 0.2V
Din = Don't care, T_{RC}= 31.25µs(4K/L-ver), 62.5µs(4K/SL-ver, 2K/L-ver), 125µs(2K/SL-ver) ,
T_{RAS}=T_{RAS}min~300 ns

I_{CCS} : Self Refresh Current
$\overline{RAS}$=$\overline{CAS}$=0.2V, $\overline{W}$=$\overline{OE}$=A0 ~ A11 = V_{CC}-0.2V or 0.2V, DQ0 ~ DQ3= V_{CC}-0.2V, 0.2V or Open

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1}, I_{CC3}, and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one fast page mode cycle time tPC.

CAPACITANCE(T_A=25°C,Vcc=5V or 3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A11]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ0 - DQ3]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 1,2)
Test condition(5V device) : Vcc=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol} =2.4/0.4V
Test condition(3.3V device) : Vcc=3.3V±0.3V, V_{ih}/V_{il}=2.0/0.8V, V_{oh}/V_{ol} =2.0/0.8V

Parameter	Symbol	-5 *1		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		130		150		ns	
Read-modify-write cycle time	tRWC	133		155		185		205		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70		80	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		13		15		20		20	ns	3,4,5
Access time from column address	tAA		25		30		35		40	ns	3,10
$\overline{CAS}$ to output in Low-Z	tCLZ	0		0		0		0		ns	3
Output buffer turn-off delay	tOFF	0	13	0	15	0	20	0	20	ns	6
Transition time (rise and fall)	tT	3	50	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		60		ns	
$\overline{RAS}$ pulse width	tRAS	50	10K	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ hold time	tRSH	13		15		20		20		ns	
$\overline{CAS}$ hold time	tCSH	50		60		70		80		ns	
$\overline{CAS}$ pulse width	tCAS	13	10K	15	10K	20	10K	20	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	37	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	15	40	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	
Column address hold time	tCAH	10		10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	tAR	40		45		55		60		ns	15
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		0		ns	
Write command hold time	tWCH	10		10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	tWCR	40		45		55		60		ns	15
Write command pulse width	tWP	10		10		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		15		20		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	13		15		20		20		ns	

Note) *1 : 5V only

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5 *1		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		0		ns	9
Data hold time	tDH	10		10		15		15		ns	9
Data hold time referenced to $\overline{\text{RAS}}$	tDHR	40		45		55		60		ns	15
Refresh period(2K, Normal)	tREF		32		32		32		32	ms	
Refresh period(4K, Normal)	tREF		64		64		64		64	ms	
Refresh period(L-ver)	tREF		128		128		128		128	ms	
Refresh period(SL-ver)	tREF		256		256		256		256	ms	
Write command set-up time	tWCS	0		0		0		0		ns	7
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	tCWD	36		40		50		50		ns	7
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	tRWD	73		85		100		110		ns	7
Column address to $\overline{\text{W}}$ delay time	tAWD	48		55		65		70		ns	7
$\overline{\text{CAS}}$ precharge to $\overline{\text{W}}$ delay time	tCPWD	53		60		70		75		ns	
$\overline{\text{CAS}}$ set-up time ($\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh)	tCSR	5		5		5		5		ns	
$\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh)	tCHR	10		10		15		15		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	tRPC	5		5		5		5		ns	
$\overline{\text{CAS}}$ precharge time($\overline{\text{CBR}}$ counter test cycle)	tCPT	20		20		30		30		ns	3
Access time from $\overline{\text{CAS}}$ precharge	tCPA		30		35		40		45	ns	
Fast Page mode cycle time	tPC	35		40		45		50		ns	
Fast Page mode read-modify-write cycle time	tPRWC	76		85		100		105		ns	
$\overline{\text{CAS}}$ precharge time (Fast page cycle)	tCP	10		10		10		10		ns	
$\overline{\text{RAS}}$ pulse width (Fast page cycle)	tRASP	50	200K	60	200K	70	200K	80	200K	ns	
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	tRHCP	30		35		40		45		ns	
$\overline{\text{OE}}$ access time	tOEA		13		15		20		20	ns	
$\overline{\text{OE}}$ to data delay	tOED	13		15		20		20		ns	
Out put buffer turn off delay time from $\overline{\text{OE}}$	tOEZ	0	13	0	15	0	20	0	20	ns	
$\overline{\text{OE}}$ command hold time	tOEH	13		15		20		20		ns	
Write command set-up time(Test mode in)	tWTS	10		10		10		10		ns	11
Write command hold time(Test mode in)	tWTH	10		10		10		10		ns	11
$\overline{\text{W}}$ to $\overline{\text{RAS}}$ precharge time($\overline{\text{C}}$-B-$\overline{\text{R}}$ refresh)	tWRP	10		10		10		10		ns	
$\overline{\text{W}}$ to $\overline{\text{RAS}}$ hold time($\overline{\text{C}}$-B-$\overline{\text{R}}$ refresh)	tWRH	10		10		10		10		ns	
$\overline{\text{RAS}}$ pulse width($\overline{\text{C}}$-B-$\overline{\text{R}}$ self refresh)	tRASS	100		100		100		100		us	14
$\overline{\text{RAS}}$ precharge time ($\overline{\text{C}}$-B-$\overline{\text{R}}$ self refresh)	tRPS	90		110		130		150		ns	14
$\overline{\text{CAS}}$ hold time ($\overline{\text{C}}$-B-$\overline{\text{R}}$ self refresh)	tCHS	-50		-50		-50		-50		ns	14

Note) *1 : 5V only

TEST MODE CYCLE

(Note. 11)

Parameter	Symbol	-5*1 Min	-5*1 Max	-6 Min	-6 Max	-7 Min	-7 Max	-8 Min	-8 Max	Units	Notes
Random read or write cycle time	tRC	95		115		135		155		ns	
Read-modify-write cycle time	tRWC	138		160		190		210		ns	
Access time from $\overline{RAS}$	tRAC		55		65		75		85	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		18		20		25		25	ns	3,4,5
Access time from column address	tAA		30		35		40		45	ns	3,10
$\overline{RAS}$ pulse width	tRAS	55	10K	65	10K	75	10K	85	10K	ns	
$\overline{CAS}$ pulse width	tCAS	18	10K	20	10K	25	10K	25	10K	ns	
$\overline{RAS}$ hold time	tRSH	18		20		25		25		ns	
$\overline{CAS}$ hold time	tCSH	55		65		75		85		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		45		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	41		45		55		55		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	78		90		105		115		ns	7
Column address to $\overline{W}$ delay time	tAWD	53		60		70		75		ns	7
Fast Page mode cycle time	tPC	40		45		50		55		ns	
Fast page mode read-modify-write cycle time	tPRWC	81		90		105		110		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	55	200K	65	200K	75	200K	85	200K	ns	
Access time form $\overline{CAS}$ precharge	tCPA		35		40		45		50	ns	3
$\overline{OE}$ access time	tOEA		18		20		25		25	ns	
$\overline{OE}$ to data delay	tOED	18		20		25		25		ns	
$\overline{OE}$ command hold time	tOEH	18		20		25		25		ns	

Note) *1 : 5V only

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL(5V device)/1 TTL(3.3V device) loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If tWCS≥tWCS(min), the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a re ference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
11. These specifications are applied in the test mode.
12. In test mode read cycle, the value of tRAC, tAA, tCAC is delayed by 2ns to 5ns for the specified values. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
13. tOFF(max) and tOEZ(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
14. 4096 (4K Ref.)/2048(2K Ref.) cyclesof burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.
15. tAR, tWCR, and tDHR are referenced to tRAD(MAX).

4M x 4 Bit CMOS Dynamic RAM with Static Column Mode

DESCRIPTION

This is a family of 4,194,304 x 4 bit Static Column Mode CMOS DRAMs. Static Column Mode offers high speed random access of memory cells within the same row. Refresh cycle(2K Ref. or 4K Ref.), access time(-5, -6, -7 or -8) and package type (SOJ or TSOP-II) are optional features of this family.
All of this family have $\overline{\text{CS}}$-before-$\overline{\text{RAS}}$ Refresh, $\overline{\text{RAS}}$-only refresh and Hidden Refresh capabilities.
This 4Mx4 Static Column Mode DRAM Family is fabricated using Samsung's advanced CMOS process to realize high band-width and high reliability. It may be used as main memory unit for high level computer and high performance microprocessor systems.

2

FEATURES

- Part Identification
  - KM44C4002A(5V, 4K Ref.)
  - KM44C4102A(5V, 2K Ref.)

- Active Power Dissipation

Unit : mW

Speed	Power dissipation	
	4 K	2 K
-5	495	605
-6	440	550
-7	385	495
-8	330	440

- Refresh cycles

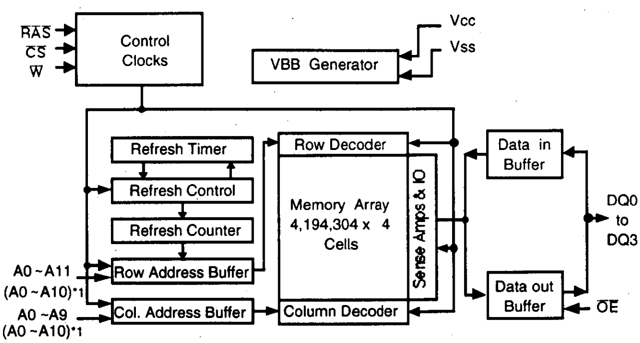
	Refresh cycle	Refresh Period
KM44C4002A	4K	64ms
KM44C4102A	2K	32ms

- Performance range:

Speed	tRAC	tCAC	tRC	tSC
-5	50ns	13ns	90ns	30ns
-6	60ns	15ns	110ns	35ns
-7	70ns	20ns	130ns	40ns
-8	80ns	20ns	150ns	45ns

- Static Column Mode operation
- $\overline{\text{CS}}$-before-$\overline{\text{RAS}}$ refresh capability
- RAS-only and Hidden refresh capability
- Fast parallel test mode capability
- TTL compatible inputs and outputs
- Early Write or Output enable controlled write
- JEDEC Standard pinout
- Available in Plastic SOJ and TSOP(II) packages
- Single +5V±10% power supply

FUNCTIONAL BLOCK DIAGRAM



Note) *1 : 2K Refresh

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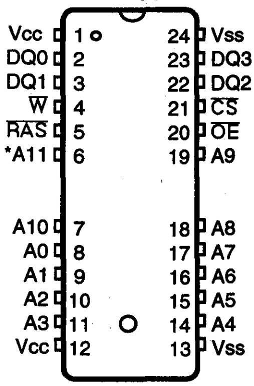
SAMSUNG ELECTRONICS

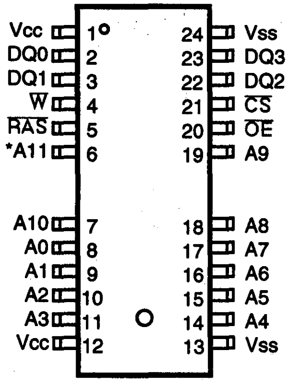
PIN CONFIGURATION (Top Views)

• KM44C40(1)02AJ



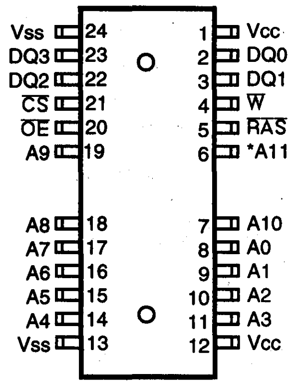
J : 400 mil 24(28) SOJ

• KM44C40(1)02AT



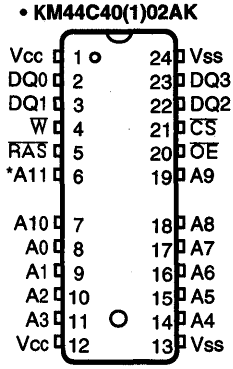
T : 400 mil 24(28) TSOP II

• KM44C40(1)02ATR



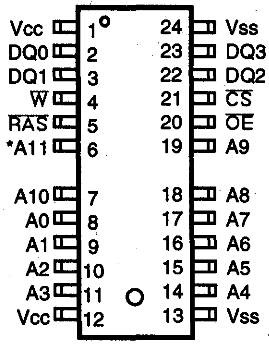
TR : 400 mil 24(28) TSOP II(Rev.)

• KM44C40(1)02AK



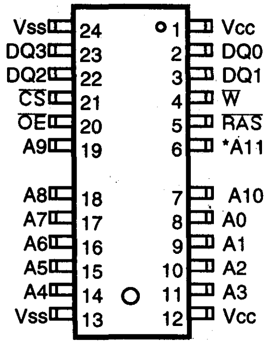
K : 300 mil 24(26) SOJ

• KM44C40(1)02AS



S : 300 mil 24(26) TSOP II

• KM44C40(1)02ASR



SR : 300 mil 24(26) TSOP II(Rev.)

* A11 is N.C for KM44C4102A(5V, 2K Ref. product)

Pin Name	Pin Function
A0 - A11	Address Inputs(4K Product)
A0 - A10	Address Inputs(2K Product)
DQ0~3	Data in/out
Vss	Ground
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CS}}$	Chip select input
$\overline{\text{W}}$	Read/Write Input
$\overline{\text{OE}}$	Data Output Enable
Vcc	Power(+5.0V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-1 to +7.0	V
Storage temperature	Tstg	-55 to +150	°C
Power dissipation	P_D	1	W
Short circuit output current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A= 0 to 70 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input high voltage	V_{IH}	2.4	-	Vcc+1.0*1	V
Input low voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : Vcc+2.0V at pulse width ≤ 20ns (pulse width is measured at Vcc)

*2 : -2.0V at pulse width ≤ 20ns (pulse width is measured at Vss)

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Units
Input leakage current (Any input $0 \le V_{IN} \le V_{CC}+0.5V$ all other pins not under test=0 volts.)	$I_{I(L)}$	- 5	5	μA
Output leakage current (Data out is disabled, $0V \le V_{OUT} \le V_{CC}$)	$I_{O(L)}$	-5	5	μA
Output high voltage level(I_{OH}=-5mA)	V_{OH}	2.4	-	V
Output low voltage level(I_{OL}=4.2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS (Continued)

Symbol	Speed	Max		Units
		KM44C4002A	KM44C4102A	
I_{CC1}	-5	90	110	mA
	-6	80	100	mA
	-7	70	90	mA
	-8	60	80	mA
I_{CC2}	Don't care	2	2	mA
I_{CC3}	-5	90	110	mA
	-6	80	100	mA
	-7	70	90	mA
	-8	60	80	mA
I_{CC4}	-5	80	90	mA
	-6	70	80	mA
	-7	60	70	mA
	-8	50	60	mA
I_{CC5}	Don't care	1	1	mA
I_{CC6}	-5	90	110	mA
	-6	80	100	mA
	-7	70	90	mA
	-8	60	80	mA

I_{CC1} *: Operating current ($\overline{RAS}$ and $\overline{CS}$ cycling @tRC=min.)

I_{CC2} : Standby current ($\overline{RAS}$=$\overline{CS}$=$\overline{W}$=V_{IH})

I_{CC3} *: $\overline{RAS}$-only refresh current ($\overline{CS}$=V_{IH}, $\overline{RAS}$,Address cycling @tRC=min.)

I_{CC4} *: Static Column Mode current ($\overline{RAS}$=V_{IL}, $\overline{CS}$, Address cycling @tSC=min.)

I_{CC5} : Standby current ($\overline{RAS}$=$\overline{CS}$=$\overline{W}$=V_{CC}-0.2V)

I_{CC6} *: $\overline{CS}$-before-$\overline{RAS}$ refresh current ($\overline{RAS}$ and $\overline{CS}$ cycling @tRC=min.)

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} , I_{CC3} and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one Static Column mode cycle time tSC.

CAPACITANCE(T_A=25°C,Vcc=5V , f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A9]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{CS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ0 - DQ3]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 1,2)
Test condition : Vcc=5.0V±10%, Vih/Vil = 2.4/0.8V, Voh/Vol = 2.4/0.4V

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		130		150		ns	
Read-modify-write cycle time	tRWC	133		155		185		205		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70		80	ns	3,4,10
Access time from $\overline{CS}$	tCAC		13		15		20		20	ns	3,4,5
Access time from column address	tAA		25		30		35		40	ns	3,10
$\overline{CS}$ to output in Low-Z	tCLZ	0		0		0		0		ns	3
Output buffer turn-off delay from $\overline{CS}$	tOFF	0	13	0	15	0	20	0	20	ns	6
Transition time (rise and fall)	tT	3	50	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		60		ns	
$\overline{RAS}$ pulse width	tRAS	50	10K	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ hold time	tRSH	13		15		20		20		ns	
$\overline{CS}$ hold time	tCSH	50		60		70		80		ns	
$\overline{CS}$ pulse width	tCS	13	10K	15	10K	20	10K	20	10K	ns	
$\overline{RAS}$ to $\overline{CS}$ delay time	tRCD	20	37	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	15	40	ns	10
$\overline{CS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	
Column address hold time	tCAH	10		10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	tAR	40		50		55		60		ns	14
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{CS}$	tRCH	0		0		0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		0		ns	8
Write command hold time	tWCH	10		10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	tWCR	40		45		55		60		ns	14
Write command pulse width	tWP	10		10		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		15		20		20		ns	
Write command to $\overline{CS}$ lead time	tCWL	13		15		20		20		ns	
Data set-up time	tDS	0		0		0		0		ns	9

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Data hold time	tDH	10		10		15		15		ns	9
Data hold time referenced to $\overline{RAS}$	tDHR	40		45		55		60		ns	14
Refresh period(2K Ref.)	tREF		32		32		32		32	ms	
Refresh period(4K Ref.)	tREF		64		64		64		64	ms	
Write command set-up time	tWCS	0		0		0		0		ns	7
$\overline{CS}$ to $\overline{W}$ delay time	tCWD	36		40		50		50		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	73		85		100		110		ns	7
Column address to $\overline{W}$ delay time	tAWD	48		55		65		70		ns	7
$\overline{CS}$ set-up time ($\overline{CS}$-before-$\overline{RAS}$ refresh)	tCSR	5		5		5		5		ns	
$\overline{CS}$ hold time ($\overline{CS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		10		10		ns	
$\overline{RAS}$ to $\overline{CS}$ precharge time	tRPC	5		5		5		5		ns	
$\overline{CS}$ precharge time($\overline{C}$-B-$\overline{R}$ counter test cycle)	tCPT	20		20		30		30		ns	
Static Column mode cycle time	tSC	30		35		40		45		ns	
Static Column mode read-modify-write cycle time	tSRWC	76		85		100		110		ns	
Access time from last write	tALW		50		55		65		75	ns	3,11
Output data hold time from column address	tAOH	5		5		5		5		ns	
Output data enable time from $\overline{W}$	tOW		35		40		45		55	ns	
$\overline{CS}$ precharge time (Static Column cycle)	tCP	10		10		10		10		ns	
$\overline{RAS}$ pulse width (Static Column cycle)	tRASC	50	200K	60	200K	70	200K	80	100K	ns	
$\overline{CS}$ pulth width (Static Column cycle)	tCSC	13	200K	15	200K	20	200K	20	200K	ns	
Column address hold time referenced to $\overline{RAS}$ rising	tAH	5		5		5		5		ns	
Last write to column address delay time	tLWAD	20	25	20	25	25	30	25	35	ns	
Last write to column address hold time	tAHLW	50		55		65		75		ns	
Write command inactive time	tWI	10		10		10		10		ns	
Write address hold time referenced to $\overline{RAS}$	tAWR	40		45		55		60		ns	
$\overline{OE}$ access time	tOEA		13		15		20		20	ns	
$\overline{OE}$ to data delay	tOED	13		15		20		20		ns	
Output buffer turn off delay from $\overline{OE}$	tOEZ	0	13	0	15	0	20	0	20	ns	
$\overline{OE}$ command hold time	tOEH	13		15		20		20		ns	
Write command set-up time(Test mode in)	tWTS	10		10		10		10		ns	
Write command hold time(Test mode in)	tWTH	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		10		ns	

TEST MODE CYCLE

(Note. 11)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	95		115		135		155		ns	
Read-modify-write cycle time	tRWC	138		160		190		210		ns	
Access time from $\overline{RAS}$	tRAC		55		65		75		85	ns	3,4,10
Access time from $\overline{CS}$	tCAC		18		20		25		25	ns	3,4,5
Access time from column address	tAA		30		35		40		45	ns	3,10
$\overline{RAS}$ pulse width	tRAS	55	10K	65	10K	75	10K	85	10K	ns	
$\overline{CS}$ pulse width	tCS	18	10K	20	10K	25	10K	25	10K	ns	
$\overline{RAS}$ hold time	tRSH	20		20		25		25		ns	
$\overline{CS}$ hold time	tCSH	55		65		75		85		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		45		ns	
$\overline{CS}$ to $\overline{W}$ delay time	tCWD	45		45		55		55		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	80		90		105		115		ns	7
Column address to $\overline{W}$ delay time	tAWD	55		60		70		75		ns	7
Static Column mode cycle time	tSC	35		40		45		50		ns	
Static Column mode read-modify-write cycle time	tSRWC	81		90		105		110		ns	
$\overline{RAS}$ pulse width (Static Column cycle)	tRASC	55	100K	65	100K	75	100K	85	100K	ns	
Access time form last write	tALW		55		60		70		80	ns	3,11
$\overline{OE}$ access time	tOEA		18		20		25		30	ns	
$\overline{OE}$ to data delay	tOED	18		20		25		25		ns	
$\overline{OE}$ command hold time	tOEH	18		20		25		25		ns	

2

NOTES

1. An initial pause of 200µs is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If tWCS≥tWCS(min), the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
11. These specifications are applied in the test mode.
12. In test mode read cycle, the value of tRAC, tAA, tCAC is delayed by 2ns to 5ns for the specified values. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
13. tOFF(max) and tOEZ(max) defines the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
14. tAR, tWCR, and tDHR are referenced to tRAD(MAX).

4M x 4 Bit CMOS Quad CAS DRAM with Fast Page Mode

DESCRIPTION

This is a family of 4,194,304 x 4 bit Fast Page Mode Quad CAS DRAMs. Fast Page Mode offers high speed random access of memory cells within the same row. Refresh cycle(2K Ref. or 4K Ref.), access time(-5, -6, -7 or -8), power consumption(Normal, Low power or Super-Low power) and package type(SOJ or TSOP-II) are optional features of this family. All of this family have CAS-before-RAS refresh, RAS-only refresh and Hidden refresh capabilities. Further more, Self-refresh operation is available in L & SL version.

This 4Mx4 Fast Page mode Quad CAS DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability.

FEATURES

- Part Identification
  - KM44C4003A/AL/ASL (5V, 4K Ref.)
  - KM44C4103A/AL/ASL (5V, 2K Ref.)

- Active Power Dissipation

Unit : mW

Speed	Refresh Cycle	
	4K	2K
-5	495	605
-6	440	550
-7	385	495
-8	330	440

- Refresh cycles

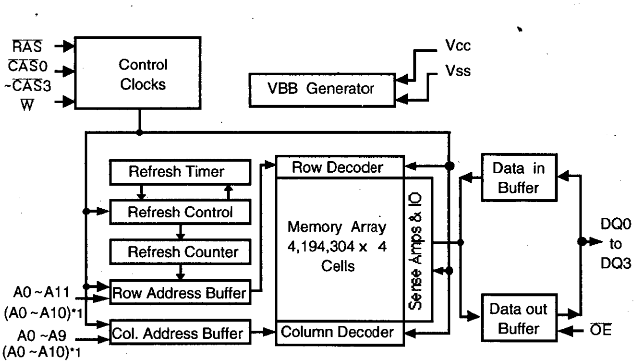
Part NO.	Refresh cycle	Refresh period		
		Normal	L	SL
C4002A	4K	64ms	128ms	256ms
C4102A	2K	32ms		

- Performance range:

Speed	tRAC	tCAC	tRC	tPC
-5	50ns	13ns	90ns	35ns
-6	60ns	15ns	110ns	40ns
-7	70ns	20ns	130ns	45ns
-8	80ns	20ns	150ns	50ns

- Fast Page Mode operation
- Four separate CAS pins provide for separate I/O operation
- CAS-before-RAS refresh capability
- RAS-only and Hidden refresh capability
- Self-refresh capability(L & SL ver)
- Fast parallel test mode capability
- TTL compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC Standard pinout
- Available in Plastic SOJ and TSOP(II) packages
- Single +5V±10% power supply

FUNCTIONAL BLOCK DIAGRAM

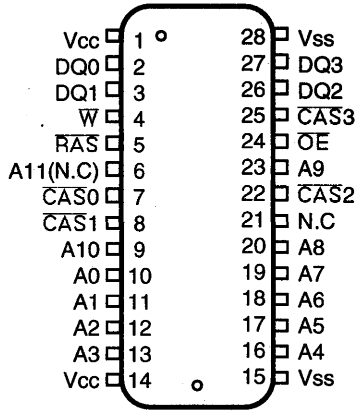


Note) *1 : 2K Refresh

SAMSUNG ELECTRONIC CO. , LTD. reserves the right to change products and specifications without notice.

PIN CONFIGURATION (Top Views)

• **KM44C40(1)03AJ/ALJ/ASLJ**

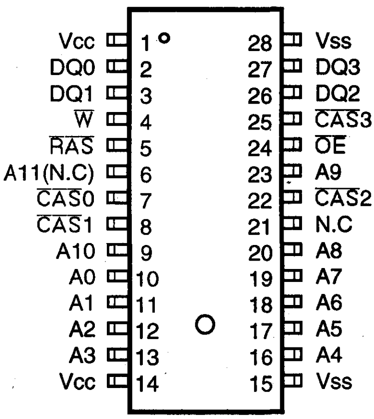


J : 400 mil 28 SOJ

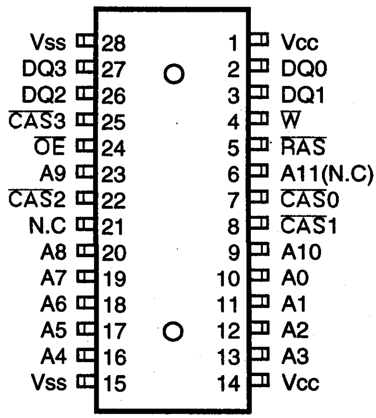
T : 400 mil 28 TSOP II

TR : 400 mil 28 TSOP II(Rev.)

• **KM44C40(1)03AT/ALT/ASLT**



• **KM44C40(1)03ATR/ALTR/ASLTR**



* Note : ( ) --> 2K Product

Pin Name	Pin Function
A0 - A11	Address Inputs(4K product)
A0 - A10	Address Inputs(2K product)
DQ0 - 3	Data In/Out
Vss	Ground
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS0}}$~$\overline{\text{CAS3}}$	Column Address Strobe
$\overline{\text{W}}$	Read/Write Input
$\overline{\text{OE}}$	Data Output Enable
Vcc	Power(+5.0V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-1 to +7.0	V
Storage Temperature	Tstg	-55 to +150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A= 0 to 70 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	Vcc+1*1	V
Input Low Voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : Vcc+2.0V at pulse width ≤ 20ns, Pulse width is measured at Vcc.
*2 : - 2.0V at pulse width ≤ 20ns, Pulse width is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input $0 \le V_{IN} \le V_{CC}+0.5V$ all other pins not under test=0 volt.)	$I_{I(L)}$	- 5	5	μA
Output Leakage Current (Data out is disabled, $0V \le V_{OUT} \le V_{CC}$)	$I_{O(L)}$	- 5	5	μA
Output High Voltage Level(I_{OH}=-5mA)	V_{OH}	2.4	-	V
Output Low Voltage Level(I_{OL}=4.2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS (Continued.)

Symbol	Power	Speed	Max		Units
			KM44C4003A	KM44C4103A	
I_{CC1}	Don't care	-5 -6 -7 -8	90 80 70 60	110 100 90 80	mA mA mA mA
I_{CC2}	Normal L/SL	Don't care	2 1	2 1	mA mA
I_{CC3}	Don't care	-5 -6 -7 -8	90 80 70 60	110 100 90 80	mA mA mA mA
I_{CC4}	Don't care	-5 -6 -7 -8	80 70 60 50	90 80 70 60	mA mA mA mA
I_{CC5}	Normal L SL	Don't care	1 300 200	1 300 200	mA µA µA
I_{CC6}	Don't care	-5 -6 -7 -8	90 80 70 60	110 100 90 80	mA mA mA mA
I_{CC7}	L SL	Don't care	450 350	400 300	µA µA
I_{CCS}	L/SL	Don't care	300	300	µA

I_{CC1}* : Operating Current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}* : $\overline{RAS}$-only Refresh Current ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @tRC=min.)

I_{CC4}* : Static Column Mode Current ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address cycling @tPC=min.)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)

I_{CC6}* : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode
Input high voltage(V_{IH})=V_{CC}-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{CAS}$= 0.2V
Din = Don't care, T_{RC}= 31.25µs(4K/L-ver), 62.5µs(4K/SL-ver, 2K/L-ver), 125µs(2K/SL-ver) ,
T_{RAS}=T_{RAS}min~300 ns

I_{CCS} : Self Refresh Current
$\overline{RAS}$=$\overline{CAS}$=0.2V, $\overline{W}$=$\overline{OE}$=A0 ~ A11 = V_{CC}-0.2V or 0.2V, DQ0 ~ DQ3= V_{CC}-0.2V, 0.2V or Open

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1}, I_{CC3}, and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one fast page mode cycle time tPC.

CAPACITANCE(T_A=25°C,Vcc=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A11]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{CAS}$x, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ0 - DQ3]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 1,2)
Test condition : Vcc=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.4/0.4V

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		130		150		ns	
Read-modify-write cycle time	tRWC	133		155		185		205		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70		80	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		13		15		20		20	ns	3,4,5,18
Access time from column address	tAA		25		30		35		40	ns	3,10
$\overline{CAS}$ to output in Low-Z	tCLZ	0		0		0		0		ns	3,18
Output buffer turn-off delay	tOFF	0	13	0	15	0	20	0	20	ns	7,18
Transition time (rise and fall)	tT	3	50	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		60		ns	
$\overline{RAS}$ pulse width	tRAS	50	10K	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ hold time	tRSH	13		15		20		20		ns	16
$\overline{CAS}$ hold time	tCSH	50		60		70		80		ns	17
$\overline{CAS}$ pulse width	tCAS	13	10K	15	10K	20	10K	20	10K	ns	23
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	37	20	45	20	50	20	60	ns	4,16
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	15	40	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		5		ns	17
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	16
Column address hold time	tCAH	10		10		15		15		ns	16
Column address hold time referenced to $\overline{RAS}$	tAR	40		45		55		60		ns	25
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	16
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		0		ns	8,17
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		0		ns	8
Write command hold time	tWCH	10		10		15		15		ns	24
Write command hold time referenced to $\overline{RAS}$	tWCR	40		45		15		15		ns	25
Write command pulse width	tWP	10		10		55		60		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		15		20		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	13		15		20		20		ns	17

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		0		ns	9
Data hold time	tDH	10		10		15		15		ns	9
Data hold time referenced to $\overline{RAS}$	tDHR	40		45		55		60		ns	25
Refresh period(2K, Normal)	tREF		32		32		32		32	ms	
Refresh period(4K, Normal)	tREF		64		64		64		64	ms	
Refresh period(L -ver)	tREF		128		128		128		128	ms	
Refresh period(SL-ver)	tREF		256		256		256		256	ms	
Write command set-up time	tWCS	0		0		0		0		ns	7,16
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	36		40		50		50		ns	7,16
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	73		85		100		110		ns	7
Column address to $\overline{W}$ delay time	tAWD	48		55		65		70		ns	7
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	5		5		5		5		ns	16
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		15		15		ns	17
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		5		ns	
$\overline{CAS}$ precharge time($\overline{CBR}$ counter test cycle)	tCPT	20		20		30		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		30		35		40		45	ns	3,18
Fast Page mode cycle time	tPC	35		40		45		50		ns	19
Fast Page mode read-modify-write cycle time	tPRWC	76		85		100		105		ns	19
$\overline{CAS}$ precharge time (Fast page cycle)	tCP	10		10		10		10		ns	20
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	50	200K	60	200K	70	200K	80	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		45		ns	
$\overline{OE}$ access time	tOEA		13		15		20		20	ns	21
$\overline{OE}$ to data delay	tOED	13		15		20		20		ns	22
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	53		60		70		75		ns	
Out put buffer turn off delay time from $\overline{OE}$	tOEZ	0	15	0	15	0	20	0	20	ns	
$\overline{OE}$ command hold time	tOEH	13		15		20		20		ns	
Write command set-up time(Test mode in)	tWTS	10		10		10		10		ns	
Write command hold time(Test mode in)	tWTH	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		10		ns	
$\overline{RAS}$ pulse width($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		100		us	14
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	90		110		130		150		ns	14
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		-50		ns	14
Hold time $\overline{CAS}$ low to $\overline{CAS}$ high	tCLCH	5		5		5		5		ns	15

TEST MODE CYCLE

(Note. 11)

Parameter	Symbol	-5		-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	95		115		135		155		ns	
Read-modify-write cycle time	tRWC	138		160		190		210		ns	
Access time from $\overline{RAS}$	tRAC		55		65		75		85	ns	3,4,10,12
Access time from $\overline{CAS}$	tCAC		18		20		25		25	ns	3,4,5,12
Access time from column address	tAA		30		35		40		45	ns	3,10
$\overline{RAS}$ pulse width	tRAS	55	10K	65	10K	75	10K	85	10K	ns	
$\overline{CAS}$ pulse width	tCAS	18	10K	20	10K	25	10K	25	10K	ns	
$\overline{RAS}$ hold time	tRSH	18		20		25		25		ns	
$\overline{CAS}$ hold time	tCSH	55		65		75		85		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		45		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	41		45		55		55		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	78		90		105		115		ns	7
Column address to $\overline{W}$ delay time	tAWD	53		60		70		75		ns	7
Fast Page mode cycle time	tPC	40		45		50		55		ns	
Fast page mode read-modify-write cycle time	tPRWC	81		90		105		110		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	55	200K	65	200K	75	200K	85	200K	ns	
Access time form $\overline{CAS}$ precharge	tCPA		35		40		45		50	ns	3
$\overline{OE}$ access time	tOEA		18		20		25		25	ns	
$\overline{OE}$ to data delay	tOED	18		20		25		25		ns	
$\overline{OE}$ command hold time	tOEH	18		20		25		25		ns	

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a re ference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in thedata sheet as electric characteristics only. If tWCS≥tWCS(min), the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
11. These specifications are applied in the test mode.
12. In test mode read cycle, the value of tRAC, tAA, tCAC is delayed by 2ns to 5ns for the specified values. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
13. tOFF(max) and tOEZ(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
14. 4096(4K Ref.)/2048(2K Ref.) cycles of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.
15. In order to hold the address latched by the first $\overline{CAS}$ going low, the parameter tCLCH must be met.
16. The first $\overline{CAS}$x edge to transition low.
17. The last $\overline{CAS}$x edge to transition high.
18. Output parameter is referenced to corresponding $\overline{CAS}$x input.
19. Last rising $\overline{CAS}$x edge to next cycle's last rising $\overline{CAS}$x edge.
20. Last rising $\overline{CAS}$x edge to first falling $\overline{CAS}$ edge.
21. First DQx controlled by the first $\overline{CAS}$x to go low.
22. Last DQx controlled by the last $\overline{CAS}$x to go high.
23. Each $\overline{CAS}$x must meet minimum pulse width.
24. Last $\overline{CAS}$x to go low.
25. tAR, tWCR, and tDHR are referenced to tRAD(MAX).

4M x 4 Bit CMOS Dynamic RAM with Extended Data Out

DESCRIPTION

This is a family of 4,194,304 x 4 bit Extended Data Out CMOS DRAMs. Extended Data Out Mode offers high speed random access of memory cells within the same row, so called Hyper Page Mode. Power supply voltage(+5.0V or +3.3V), refresh cycle(2K Ref. or 4K Ref.), access time(-5, -6, -7 or -8), power consumption(Normal, Low power or Super-Low power) and package type(SOJ or TSOP-II) are optional features of this family. All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities. Further more, Self-refresh operation is available in L & SL version.
This 4Mx4 EDO DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability. It may be used as main memory unit for high level computer, microcomputer and personal computer.

FEATURES

- Part Identification
  - KM44C4004A/AL/ASL (5V, 4K Ref.)
  - KM44C4104A/AL/ASL (5V, 2K Ref.)
  - KM44V4004A/AL/ASL (3.3V, 4K Ref.)
  - KM44V4104A/AL/ASL (3.3V, 2K Ref.)
- Active Power Dissipation

Unit : mW

Speed	3.3V		5V	
	4K	2K	4K	2K
-5	-	-	495	605
-6	288	360	440	550
-7	252	324	385	495
-8	216	288	330	440

- Refresh cycles

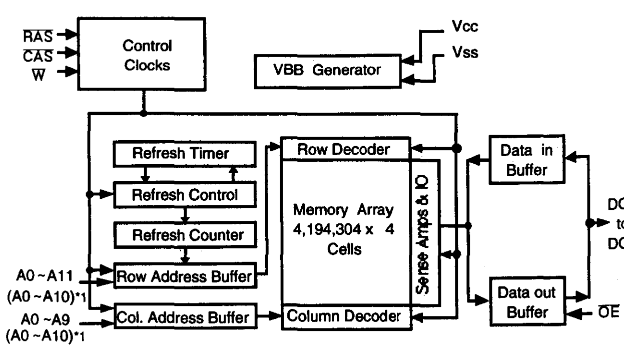
Part NO.	Vcc	Refresh cycle	Refresh period		
			Normal	L	SL
C4004A	5V	4K	64ms	128ms	256ms
V4004A	3.3V				
C4104A	5V	2K	32ms		
V4104A	3.3V				

- Performance range:

Speed	tRAC	tCAC	tRC	tHPC	Remark
-5	50ns	13ns	90ns	20ns	5V Only
-6	60ns	15ns	110ns	25ns	5V/3.3V
-7	70ns	20ns	130ns	30ns	5V/3.3V
-8	80ns	20ns	150ns	35ns	5V/3.3V

- Extended Data Out mode operation (Fast Page Mode with Extended data out)
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- Self-refresh capability(L & SL - ver)
- Fast parallel test mode capability
- TTL(5V)/LVTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC Standard pinout
- Available in Plastic SOJ and TSOP(II) packages
- Single +5V±10% power supply(5V product)
- Single +3.3V±0.3V power supply(3.3V product)

FUNCTIONAL BLOCK DIAGRAM



Note) *1 : 2K Refresh

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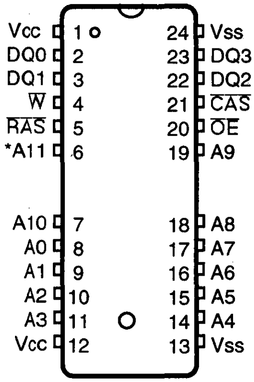
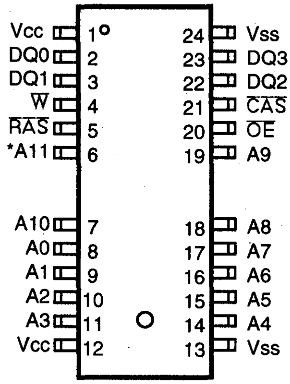
PIN CONFIGURATION (Top Views)

• KM44C/V40(1)04AJ



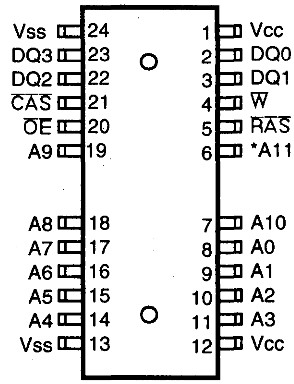
J : 400 mil 24(28) SOJ

• KM44C/V40(1)04AT



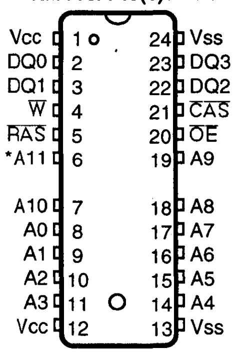
T : 400 mil 24(28) TSOP II

• KM44C/V40(1)04ATR



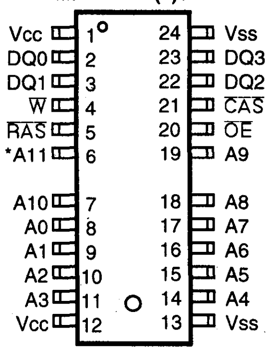
TR : 400 mil 24(28) TSOP II(Rev.)

• KM44C/V40(1)04AK



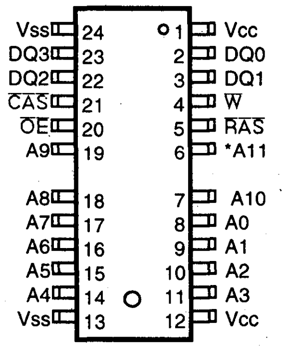
K : 300 mil 24(26) SOJ

• KM44C/V40(1)04AS



S : 300 mil 24(26) TSOP II

• KM44C/V40(1)04ASR



SR : 300 mil 24(26) TSOP II(Rev.)

* A11 is N.C for KM44C/V4104A(5V/3.3V, 2K Ref. product)

Pin Name	Pin Function
A0 - A11	Address Inputs(4K Product)
A0 - A10	Address Inputs(2K Product)
DQ0 -3	Data In/Out
Vss	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Outputs Enable
Vcc	Power(+5.0V)
	Power(+3.3V)
N.C	No Connection(2K Refresh)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating 3.3V	Rating 5V	Units
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to +4.6	-1 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.5 to +4.6	-1 to +7.0	V
Storage Temperature	Tstg	-55 to +150	-55 to +150	°C
Power Dissipation	P_D	1	1	W
Short Circuit Output Current	I_{OS}	50	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A= 0 to 70 °C)

Parameter	Symbol	3.3V Min	3.3V Typ	3.3V Max	5V Min	5V Typ	5V Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	Vcc+0.3*1	2.4	-	Vcc+1*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	-1.0*2	-	0.8	V

*1 : Vcc + 1.3V/15ns(3.3V), Vcc+2.0V/20ns(5V), Pulse width is measured at Vcc.
*2 : - 1.3V/15ns(3.3V), - 2.0V/20ns(5V), Pulse width is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

	Parameter	Symbol	Min	Max	Units
3.3V	Input Leakage Current (Any input $0 \le V_{IN} \le V_{CC}+0.3V$, all other pins not under test=0 volt.)	$I_{I(L)}$	-5	5	μA
	Output Leakage Current (Data out is disabled, $0V \le V_{OUT} \le V_{CC}$)	$I_{O(L)}$	-5	5	μA
	Output High Voltage Level(I_{OH}=-2mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level(I_{OL}=2mA)	V_{OL}	-	0.4	V
5V	Input Leakage Current (Any input $0 \le V_{IN} \le V_{CC}+0.5V$, all other pins not under test=0 volt.)	$I_{I(L)}$	-5	5	μA
	Output Leakage Current (Data out is disabled, $0V \le V_{OUT} \le V_{CC}$)	$I_{O(L)}$	-5	5	μA
	Output High Voltage Level(I_{OH}=-5mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level(I_{OL}=4.2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS (Continued.)

Symbol	Power	Speed	Max				Units
			KM44V4004A	KM44V4104A	KM44C4004A	KM44C4104A	
ICC1	Don't care	-5 -6 -7 -8	- 80 70 60	- 100 90 80	90 80 70 60	110 100 90 80	mA mA mA mA
ICC2	Normal L/SL	Don't care	2 1	2 1	2 1	2 1	mA mA
ICC3	Don't care	-5 -6 -7 -8	- 80 70 60	- 100 90 80	90 80 70 60	110 100 90 80	mA mA mA mA
ICC4	Don't care	-5 -6 -7 -8	- 90 80 70	- 100 90 80	100 90 80 70	110 100 90 80	mA mA mA mA
ICC5	Normal L SL	Don't care	1 300 200	1 300 200	1 300 200	1 300 200	mA µA µA
ICC6	Don't care	-5 -6 -7 -8	- 80 70 60	- 100 90 80	90 80 70 60	110 100 90 80	mA mA mA mA
ICC7	L SL	Don't care	450 350	400 300	450 350	400 300	µA µA
ICCS	L/SL	Don't care	250	250	300	300	µA

ICC1* : Operating Current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

ICC2 : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=VIH)

ICC3* : $\overline{RAS}$-only Refresh Current ($\overline{CAS}$=VIH, $\overline{RAS}$ cycling @tRC=min.)

ICC4* : Hyper Page Mode Current ($\overline{RAS}$=VIL, $\overline{CAS}$, Address cycling @tHPC=min.)

ICC5 : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

ICC6* : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

ICC7 : Battery back-up current, Average power supply current, Battery back-up mode
Input high voltage(VIH)=Vcc-0.2V, Input low voltage(VIL)=0.2V, $\overline{CAS}$= 0.2V
Din = Don't care, TRC= 31.25µs(4K/L-ver), 62.5µs(4K/SL-ver, 2K/L-ver), 125µs(2K/SL-ver) ,
TRAS=TRASmin~300 ns

ICCS : Self Refresh Current
$\overline{RAS}$=$\overline{CAS}$=0.2V, $\overline{W}$=$\overline{OE}$=A0 ~ A11 = Vcc-0.2V or 0.2V, DQ0 ~ DQ3= Vcc-0.2V, 0.2V or Open

* NOTE : ICC1, ICC3, ICC4 and ICC6 are dependent on output loading and cycle rates. Specified values are obtained with the output open. ICC is specified as an average current. In ICC1, ICC3, and ICC6, address can be changed maximum once while $\overline{RAS}$=VIL. In ICC4, address can be changed maximum once within one hyper page mode cycle time tHPC.

CAPACITANCE(T_A=25°C,Vcc=5V or 3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A11]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ0 - DQ3]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 1,2)
Test condition(5V device) : Vcc=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol} =2.0/0.8V
Test condition(3.3V device) : Vcc=3.3V±0.3V, V_{ih}/V_{il}=2.0/0.8V, V_{oh}/V_{ol} =2.0/0.8V

Parameter	Symbol	-5 *1		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	84		104		124		144		ns	
Read-modify-write cycle time	tRWC	116		140		170		190		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70		80	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		13		15		20		20	ns	3,4,5
Access time from column address	tAA		25		30		35		40	ns	3,10
$\overline{CAS}$ to output in Low-Z	tCLZ	3		3		3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	tCEZ	3	13	3	15	3	20	3	20	ns	6,14
$\overline{OE}$ to output in Low-Z	tOLZ	3		3		3		3		ns	3
Transition time (rise and fall)	tT	2	50	2	50	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		60		ns	
$\overline{RAS}$ pulse width	tRAS	50	10K	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ hold time	tRSH	13		15		20		20		ns	
$\overline{CAS}$ hold time	tCSH	38		45		50		60		ns	
$\overline{CAS}$ pulse width	tCAS	8	10K	10	10K	15	10K	20	10K	ns	15
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	37	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	15	40	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	
Column address hold time	tCAH	8		10		15		15		ns	
Column address hold time referenced $\overline{RAS}$	tAR	35		42		52		57		ns	17
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		0		ns	8
Write command hold time	tWCH	10		10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	tWCR	37		42		52		57		ns	17
Write command pulse width	tWP	10		10		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	13		15		20		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	8		10		15		20		ns	

Note) *1 : 5V only

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AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5 *1		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		0		ns	9
Data hold time	tDH	8		10		15		15		ns	9
Data hold time referenced to $\overline{RAS}$	tDHR	37		42		52		57		ns	17
Refresh period(2K, Normal)	tREF		32		32		32		32	ms	
Refresh period(4K, Normal)	tREF		64		64		64		64	ms	
Refresh period(L-ver)	tREF		128		128		128		128	ms	
Refresh period(SL-ver)	tREF		256		256		256		256	ms	
Write command set-up time	tWCS	0		0		0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	30		34		44		44		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	67		79		94		104		ns	7
Column address to $\overline{W}$ delay time	tAWD	42		49		59		64		ns	7
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	5		5		5		5		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		5		ns	
$\overline{CAS}$ precharge time($\overline{CBR}$ counter test cycle)	tCPT	20		20		30		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		28		35		40		45	ns	3
Hyper Page cycle time	tHPC	20		25		30		35		ns	16
Hyper Page read-modify-write cycle time	tHPRWC	47		56		71		81		ns	16
$\overline{CAS}$ precharge time (Hyper page cycle)	tCP	8		10		10		10		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	tRASP	50	200K	60	200K	70	200K	80	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		45		ns	
$\overline{OE}$ access time	tOEA		13		15		20		20	ns	
$\overline{OE}$ to data delay	tOED	13		15		20		20		ns	
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	45		54		64		69		ns	
Out put buffer turn off delay time from $\overline{OE}$	tOEZ	3	13	3	15	3	20	3	20	ns	6
$\overline{OE}$ command hold time	tOEH	13		15		20		20		ns	
Write command set-up time(Test mode in)	tWTS	10		10		10		10		ns	11
Write command hold time(Test mode in)	tWTH	10		10		10		10		ns	11
$\overline{W}$ to $\overline{RAS}$ precharge time($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		10		ns	
Output data hold time	tDOH	5		5		5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	tREZ	3	15	3	15	3	20	3	20	ns	6,15
Output buffer turn off delay from $\overline{W}$	tWEZ	3	13	3	15	3	20	3	20	ns	6
$\overline{W}$ to data delay	tWED	15		15		20		20		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	tOCH	5		5		5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	tCHO	5		5		5		5		ns	
$\overline{OE}$ precharge time	tOEP	5		5		5		5		ns	
$\overline{W}$ pulth width(Hyper Page Cycle)	tWPE	5		5		5		5		ns	
$\overline{RAS}$ pulse width($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		100		us	14

Note) *1 : 5V only

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5 *1		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{\text{RAS}}$ precharge time ($\overline{\text{C}}$-B-$\overline{\text{R}}$ self refresh)	tRPS	90		110		130		150		ns	14
$\overline{\text{CAS}}$ hold time ($\overline{\text{C}}$-B-$\overline{\text{R}}$ self refresh)	tCHS	-50		-50		-50		-50		ns	14

TEST MODE CYCLE

(Note. 11)

Parameter	Symbol	-5 *1		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	89		109		129		149		ns	
Read-modify-write cycle time	tRWC	121		145		175		195		ns	
Access time from $\overline{\text{RAS}}$	tRAC		55		65		75		85	ns	3,4,10
Access time from $\overline{\text{CAS}}$	tCAC		18		20		25		25	ns	3,4,5
Access time from column address	tAA		30		35		40		45	ns	3,10
$\overline{\text{RAS}}$ pulse width	tRAS	55	10K	65	10K	75	10K	85	10K	ns	
$\overline{\text{CAS}}$ pulse width	tCAS	13	10K	15	10K	20	10K	25	10K	ns	
$\overline{\text{RAS}}$ hold time	tRSH	18		20		25		25		ns	
$\overline{\text{CAS}}$ hold time	tCSH	43		50		55		65		ns	
Column address to $\overline{\text{RAS}}$ lead time	tRAL	30		35		40		45		ns	
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	tCWD	35		39		49		49		ns	7
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	tRWD	72		84		99		109		ns	7
Column address to $\overline{\text{W}}$ delay time	tAWD	47		54		64		69		ns	7
Hyper Page cycle time	tHPC	25		30		35		40		ns	
Hyper page read-modify-write cycle time	tHPRWC	53		61		76		86		ns	
$\overline{\text{RAS}}$ pulse width (Hyper page cycle)	tRASP	55	200K	65	200K	75	200K	85	200K	ns	
Access time form $\overline{\text{CAS}}$ precharge	tCPA		33		40		45		50	ns	3
$\overline{\text{OE}}$ access time	tOEA		18		20		25		25	ns	
$\overline{\text{OE}}$ to data delay	tOED	18		20		25		25		ns	
$\overline{\text{OE}}$ command hold time	tOEH	18		20		25		25		ns	

Note) *1 : 5V only

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SAMSUNG ELECTRONICS

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 2ns for all inputs.
3. Measured with a load equivalent to 2 TTL(5V device)/1 TTL(3.3V device) loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a re ference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If tWCS≥tWCS(min), the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a re ference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
11. These specifications are applied in the test mode.
12. In test mode read cycle, the value of tRAC, tAA, tCAC is delayed by 2ns to 5ns for the specified values. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
13. tCEZ(max), tREZ(max), tWEZ(max) and tOEZ(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
14. 4096(4K Ref.)/2048(2K Ref.) cycles of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.
15. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going.
16. tASC ≥ tCPmin , Assume tT = 2.0 ns
17. tAR, tWCR, and tDHR are referenced to tRAD(MAX).

4M x 4 Bit CMOS DRAM with Fast Page Mode(Write per Bit Mode)

DESCRIPTION

This is a family of 4,194,304 x 4 bit Fast Page Mode(Write per Bit mode) CMOS DRAMs. Fast Page Mode offers high speed random access of memory cells within the same row. Refresh cycle(2K Ref. or 4K Ref.), access time(-5, -6, -7 or -8) and package type(SOJ or TSOP-II) are optional features of this family. All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities.

This 4Mx4 Fast Page mode(write per bit mode) DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability. It may be used as main memory unit for high level computer, microcomputer and personal computer.

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FEATURES

- Part Identification
  - KM44C4010A(5V, 4K Ref.)
  - KM44C4110A(5V, 2K Ref.)

- Power Range

Unit : mW

Speed	4K	2K
-5	495	605
-6	440	550
-7	385	495
-8	330	440

- Refresh cycles

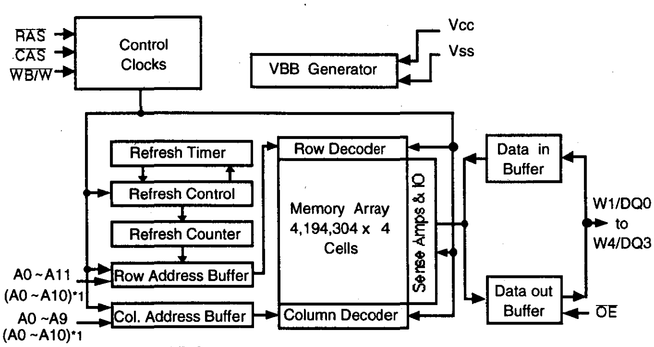
Part NO.	Refresh cycle	Refresh period
KM44C4000A	4K	64ms
KM44C4100A	2K	32ms

- Performance range:

Speed	tRAC	tCAC	tRC	tPC
-5	50ns	13ns	90ns	35ns
-6	60ns	15ns	110ns	40ns
-7	70ns	20ns	130ns	45ns
-8	80ns	20ns	150ns	50ns

- Fast Page Mode operation
- Write per bit mode capability
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- Fast parallel test mode capability
- TTL compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC Standard pinout
- Available in Plastic SOJ and TSOP(II) packages
- Single +5V±10% power supply(5V product)

FUNCTIONAL BLOCK DIAGRAM



Note) *1 : 2K Refresh

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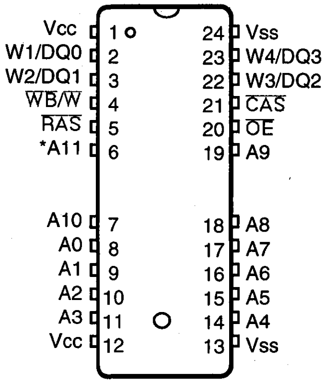
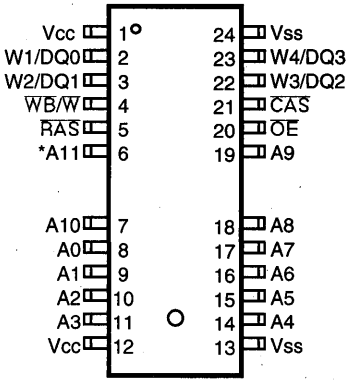
PIN CONFIGURATION (Top Views)

• KM44C40(1)10AJ



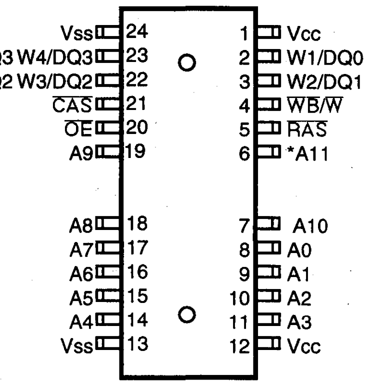
J : 400 mil 24(28) SOJ

• KM44C40(1)10AT



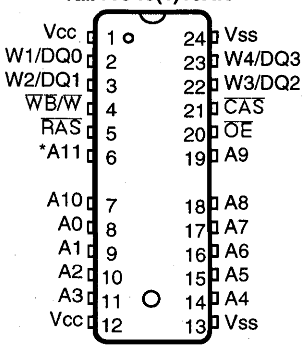
T : 400 mil 24(28) TSOP II

• KM44C40(1)10ATR



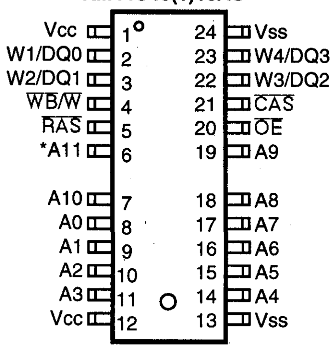
TR : 400 mil 24(28) TSOP II(Rev.)

• KM44C40(1)10AK



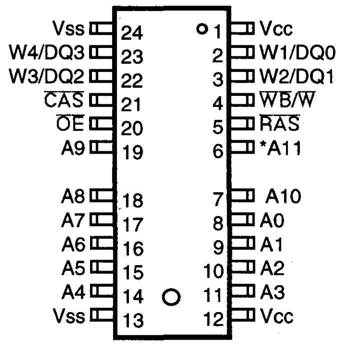
K : 300 mil 24(26) SOJ

• KM44C40(1)10AS



S : 300 mil 24(26) TSOP II

• KM44C40(1)10ASR



SR : 300 mil 24(26) TSOP II(Rev.)

* A11 is N.C for KM44C4110A(2K Ref. product)

Pin Name	Pin Function
A0 - A11	Address Inputs(4K Product)
A0 - A10	Address Inputs(2K Product)
W/DQ0 -3	Write select/ Data In,Out
V_{SS}	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WB}/\overline{W}$	Write per bit/ Read,Write Input
$\overline{OE}$	Data Output Enable
V_{CC}	Power(+5.0V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-1 to +7.0	V
Storage Temperature	Tstg	-55 to +150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A= 0 to 70 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	Vcc+1*1	V
Input Low Voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : Vcc+2.0V at pulse width ≤ 20ns, Pulse width is measured at Vcc.

*2 : - 2.0V at pulse width ≤ 20ns, Pulse width is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input $0 \le V_{IN} \le V_{CC}+0.5V$, all other pins not under test=0 volt.)	$I_{I(L)}$	- 5	5	μA
Output Leakage Current (Data out is disabled, $0V \le V_{OUT} \le V_{CC}$)	$I_{O(L)}$	- 5	5	μA
Output High Voltage Level(I_{OH}=-5mA)	V_{OH}	2.4	-	V
Output Low Voltage Level(I_{OL}=4.2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS (Continued.)

Symbol	Speed	Max		Units
		KM44C4010A	KM44C4110A	
I_{CC1}	-5	90	110	mA
	-6	80	100	mA
	-7	70	90	mA
	-8	60	80	mA
I_{CC2}	Don't care	2	2	mA
I_{CC3}	-5	90	110	mA
	-6	80	100	mA
	-7	70	90	mA
	-8	60	80	mA
I_{CC4}	-5	80	90	mA
	-6	70	80	mA
	-7	60	70	mA
	-8	50	60	mA
I_{CC5}	Don't care	1	1	mA
I_{CC6}	-5	90	110	mA
	-6	80	100	mA
	-7	70	90	mA
	-8	60	80	mA

I_{CC1}* : Operating Current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{WB}/\overline{W}$=$V_{IH}$)

I_{CC3}* : $\overline{RAS}$-only Refresh Current ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @tRC=min.)

I_{CC4}* : Fast Page Mode Current ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address cycling @tPC=min.)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{WB}/\overline{W}$=$V_{CC}$-0.2V)

I_{CC6}* : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1}, I_{CC3}, and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one fast page mode cycle time tPC.

CAPACITANCE(T_A=25°C,Vcc=5V , f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A11]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{WB}/W$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output Capacitance [W/DQ0 - W/DQ3]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 1,2)
Test condition : Vcc=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.0/0.8V

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		130		150		ns	
Read-modify-write cycle time	tRWC	133		155		185		205		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70		80	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		13		15		20		20	ns	3,4,5
Access time from column address	tAA		25		30		35		40	ns	3,10
$\overline{CAS}$ to output in Low-Z	tCLZ	0		0		0		0		ns	3
Output buffer turn-off delay	tOFF	0	13	0	15	0	20	0	20	ns	6
Transition time (rise and fall)	tT	3	50	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		60		ns	
$\overline{RAS}$ pulse width	tRAS	50	10K	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ hold time	tRSH	13		15		20		20		ns	
$\overline{CAS}$ hold time	tCSH	50		60		70		80		ns	
$\overline{CAS}$ pulse width	tCAS	13	10K	15	10K	20	10K	20	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	37	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	15	40	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	
Column address hold time	tCAH	10		10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	tAR	40		45		55		60		ns	14
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		0		ns	
Write command hold time	tWCH	10		10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	tWCR	40		45		55		60		ns	14
Write command pulse width	tWP	10		10		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		15		20		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	13		15		20		20		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5 Min	-5 Max	-6 Min	-6 Max	-7 Min	-7 Max	-8 Min	-8 Max	Units	Notes
Data set-up time	tDS	0		0		0		0		ns	9
Data hold time	tDH	10		10		15		15		ns	9
Data hold time referenced to $\overline{RAS}$	tDHR	40		45		55		60		ns	14
Refresh period(2K, Normal)	tREF		32		32		32		32	ms	
Refresh period(4K, Normal)	tREF		64		64		64		64	ms	
Write command set-up time	tWCS	0		0		0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	36		40		50		50		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	73		85		100		110		ns	7
Column address to $\overline{W}$ delay time	tAWD	48		55		65		70		ns	7
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	5		5		5		5		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		5		ns	
$\overline{CAS}$ precharge time($\overline{CBR}$ counter test cycle)	tCPT	20		20		30		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA	-	30		35		40		45	ns	3
Fast Page mode cycle time	tPC	35		40		45		50		ns	
Fast Page mode read-modify-write cycle time	tPRWC	76		85		100		105		ns	
$\overline{CAS}$ precharge time (Fast page cycle)	tCP	10		10		10		10		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	50	200K	60	200K	70	200K	80	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		45		ns	
$\overline{OE}$ access time	tOEA		13		15		20		20	ns	
$\overline{OE}$ to data delay	tOED	13		15		20		20		ns	
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	53		60		70		75		ns	
Out put buffer turn off delay time from $\overline{OE}$	tOEZ	0	13	0	15	0	20	0	20	ns	
$\overline{OE}$ command hold time	tOEH	13		15		20		20		ns	
Write command set-up time(Test mode in)	tWTS	10		10		10		10		ns	11
Write command hold time(Test mode in)	tWTH	10		10		10		10		ns	11
$\overline{W}$ to $\overline{RAS}$ precharge time($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		10		ns	
Write per bit set-up time	tWBS	0		0		0		0		ns	
Write per bit hold time	tWBH	10		10		10		10		ns	
Write selection set-up time	tWDS	0		0		0		0		ns	
Write per bit selection hold time	tWDH	10		10		10		10		ns	

TEST MODE CYCLE

(Note. 11)

Parameter	Symbol	-5[*1] Min	-5[*1] Max	-6 Min	-6 Max	-7 Min	-7 Max	-8 Min	-8 Max	Units	Notes
Random read or write cycle time	tRC	95		115		135		155		ns	
Read-modify-write cycle time	tRWC	138		160		190		210		ns	
Access time from $\overline{RAS}$	tRAC		55		65		75		85	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		18		20		25		25	ns	3,4,5
Access time from column address	tAA		30		35		40		45	ns	3,10
$\overline{RAS}$ pulse width	tRAS	55	10K	65	10K	75	10K	85	10K	ns	
$\overline{CAS}$ pulse width	tCAS	18	10K	20	10K	25	10K	25	10K	ns	
$\overline{RAS}$ hold time	tRSH	18		20		25		25		ns	
$\overline{CAS}$ hold time	tCSH	55		65		75		85		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		45		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	41		45		55		55		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	78		90		105		115		ns	7
Column address to $\overline{W}$ delay time	tAWD	53		60		70		75		ns	7
Fast Page mode cycle time	tPC	40		45		50		55		ns	
Fast page mode read-modify-write cycle time	tPRWC	81		90		105		110		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	55	200K	65	200K	75	200K	85	200K	ns	
Access time form $\overline{CAS}$ precharge	tCPA		35		40		45		50	ns	3
$\overline{OE}$ access time	tOEA		18		20		25		25	ns	
$\overline{OE}$ to data delay	tOED	18		20		25		25		ns	
$\overline{OE}$ command hold time	tOEH	18		20		25		25		ns	

NOTES

1. An initial pause of 200µs is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If tWCS≥tWCS(min), the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a re ference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
11. These specifications are applied in the test mode.
12. In test mode read cycle, the value of tRAC, tAA, tCAC is delayed by 2ns to 5ns for the specified values. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
13. tOFF(max) and tOEZ(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
14. tAR, tWCR, and tDHR are referenced to tRAD(MAX).

2M x 8 Bit CMOS Dynamic RAM with Fast Page Mode

DESCRIPTION

This is a family of 2,097,152 x 8 bit Fast Page Mode CMOS DRAMs. Fast Page Mode offers high speed random access of memory cells within the same row. Power supply voltage(+5.0V or +3.3V), refresh cycle(2K Ref. or 4K Ref.), access time(-5, -6, -7 or -8), power consumption(Normal, Low power or Super-Low power) and package type(SOJ or TSOP-II) are optional features of this family. All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities. Further more, Self-refresh operation is available in L & SL version.

This 2Mx8 Fast Page mode DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability. It may be used as main memory unit for high level computer, microcomputer and personal computer.

FEATURES

- Part Identification
  - KM48C2000A/AL/ASL (5V, 4K Ref.)
  - KM48C2100A/AL/ASL (5V, 2K Ref.)
  - KM48V2000A/AL/ASL (3.3V, 4K Ref.)
  - KM48V2100A/AL/ASL (3.3V, 2K Ref.)

- Active Power Dissipation

Unit : mW

Speed	3.3V		5V	
	4K	2K	4K	2K
-5	-	-	495	605
-6	288	360	440	550
-7	252	324	385	495
-8	216	288	330	440

- Refresh cycles

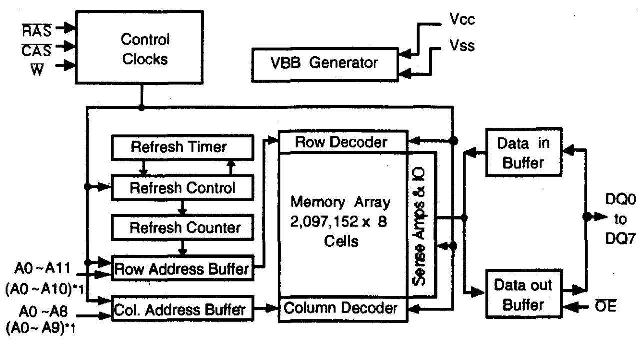
Part NO.	Vcc	Refresh cycle	Refresh period		
			Normal	L	SL
C2000A	5V	4K	64ms	128ms	256ms
V2000A	3.3V				
C2100A	5V	2K	32ms		
V2100A	3.3V				

- Performance range:

Speed	tRAC	tCAC	tRC	tPC	Remark
-5	50ns	13ns	90ns	35ns	5V Only
-6	60ns	15ns	110ns	40ns	5V/3.3V
-7	70ns	20ns	130ns	45ns	5V/3.3V
-8	80ns	20ns	150ns	50ns	5V/3.3V

- Fast Page Mode operation
- Byte Read/Write operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- Self-refresh capability(L & SL -ver)
- Fast parallel test mode capability
- TTL(5V)/LVTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC Standard pinout
- Available in Plastic SOJ and TSOP(II) packages
- Single +5V±10% power supply(5V product)
- Single +3.3V±0.3V power supply(3.3V product)

FUNCTIONAL BLOCK DIAGRAM

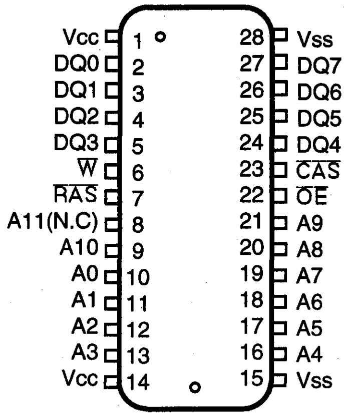


Note) *1 : 2K Refresh

SAMSUNG ELECTRONIC CO., LTD. reserves the right to change products and specifications without notice.

PIN CONFIGURATION (Top Views)

• KM48C/V20(1)00AJ/ALJ/ASLJ

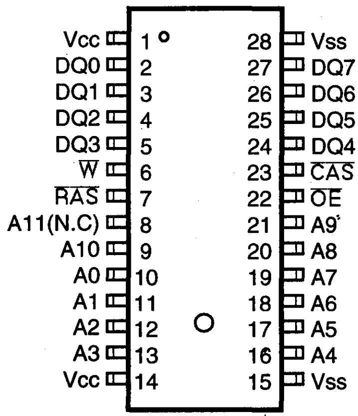


J : 400 mil 28 SOJ

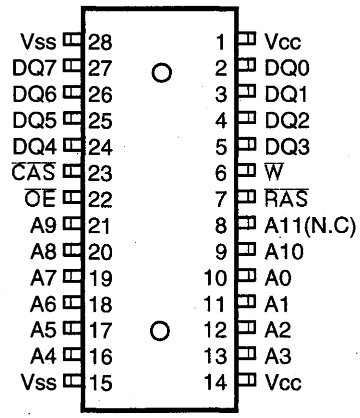
T : 400 mil 28 TSOP II

TR : 400 mil 28 TSOP II(Rev.)

• KM48C/V20(1)00AT/ALT/ASLT



• KM48C/V20(1)00ATR/ALTR/ASLTR



* Note : ( ) --> 2K Product

Pin Name	Pin Function
A0 - A11	Address Inputs(4K product)
A0 - A10	Address Inputs(2K product)
DQ0 -7	Data In/Out
Vss	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Outputs Enable
Vcc	Power(+5.0V)
	Power(+3.3V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Units
		3.3V	5V	
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to +4.6	-1 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.5 to +4.6	-1 to +7.0	V
Storage Temperature	Tstg	-55 to +150	-55 to +150	°C
Power Dissipation	P_D	1	1	W
Short Circuit Output Current	I_{OS}	50	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A= 0 to 70 °C)

Parameter	Symbol	3.3V			5V			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V_{CC}	3.0	3.3	3.6	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	Vcc+0.3*1	2.4	-	Vcc+1*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	-1.0*2	-	0.8	V

*1 : Vcc + 1.3V/15ns(3.3V), Vcc+2.0V/20ns(5V), Pulse width is measured at Vcc.
*2 : - 1.3V/15ns(3.3V), - 2.0V/20ns(5V), Pulse width is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

	Parameter	Symbol	Min	Max	Units
3.3V	Input Leakage Current (Any input $0 \le V_{IN} \le V_{CC}+0.3V$, all other pins not under test=0 volt.)	$I_{I(L)}$	- 5	5	μA
	Output Leakage Current (Data out is disabled, $0V \le V_{OUT} \le V_{CC}$)	$I_{O(L)}$	- 5	5	μA
	Output High Voltage Level(I_{OH}=-2mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level(I_{OL}=2mA)	V_{OL}	-	0.4	V
5V	Input Leakage Current (Any input $0 \le V_{IN} \le V_{CC}+0.5V$ all other pins not under test=0 volt.)	$I_{I(L)}$	- 5	5	μA
	Output Leakage Current (Data out is disabled, $0V \le V_{OUT} \le V_{CC}$)	$I_{O(L)}$	- 5	5	μA
	Output High Voltage Level(I_{OH}=-5mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level(I_{OL}=4.2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS (Continued)

Symbol	Power	Speed	Max				Units
			KM48V2000A	KM48V2100A	KM48C2000A	KM48C2100A	
I_{CC1}	Don't care	-5 -6 -7 -8	- 80 70 60	- 100 90 80	90 80 70 60	110 100 90 80	mA mA mA mA
I_{CC2}	Normal L/SL	Don't care	2 1	2 1	2 1	2 1	mA mA
I_{CC3}	Don't care	-5 -6 -7 -8	- 80 70 60	- 100 90 80	90 80 70 60	110 100 90 80	mA mA mA mA
I_{CC4}	Don't care	-5 -6 -7 -8	- 70 60 50	- 80 70 60	80 70 60 50	90 80 70 60	mA mA mA mA
I_{CC5}	Normal L SL	Don't care	1 300 200	1 300 200	1 300 200	1 300 200	mA µA µA
I_{CC6}	Don't care	-5 -6 -7 -8	- 80 70 60	- 100 90 80	90 80 70 60	110 100 90 80	mA mA mA mA
I_{CC7}	L SL	Don't care	450 350	400 300	450 350	400 300	µA µA
I_{CCS}	L/SL	Don't care	250	250	300	300	µA

I_{CC1}* : Operating Current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}* : $\overline{RAS}$-only Refresh Current ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @tRC=min.)

I_{CC4}* : Fast Page Mode Current ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address cycling @tPC=min.)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6}* : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode
Input high voltage(V_{IH})=Vcc-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{CAS}$= 0.2V
Din = Don't care, T_{RC}= 31.25µs(4K/L-ver), 62.5µs(4K/SL-ver, 2K/L-ver), 125µs(2K/SL-ver) ,
T_{RAS}=T_{RAS}min~300 ns

I_{CCS} : Self Refresh Current
$\overline{RAS}$=$\overline{CAS}$=0.2V, $\overline{W}$=$\overline{OE}$=A0 ~ A11 = Vcc-0.2V or 0.2V, DQ0 ~ DQ7= Vcc-0.2V, 0.2V or Open

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1}, I_{CC3}, and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one fast page mode cycle time tPC.

CAPACITANCE(T_A=25°C,Vcc=5V or 3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A11]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ0 - DQ7]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 1,2)
Test condition(5V device) : Vcc=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol} =2.4/0.4V
Test condition(3.3V device) : Vcc=3.3V±0.3V, V_{ih}/V_{il}=2.0/0.8V, V_{oh}/V_{ol} =2.0/0.8V

Parameter	Symbol	-5 *1		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		130		150		ns	
Read-modify-write cycle time	tRWC	133		155		185		205		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70		80	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		13		15		20		20	ns	3,4,5
Access time from column address	tAA		25		30		35		40	ns	3,10
$\overline{CAS}$ to output in Low-Z	tCLZ	0		0		0		0		ns	3
Output buffer turn-off delay	tOFF	0	13	0	15	0	20	0	20	ns	6
Transition time (rise and fall)	tT	3	50	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		60		ns	
$\overline{RAS}$ pulse width	tRAS	50	10K	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ hold time	tRSH	13		15		20		20		ns	
$\overline{CAS}$ hold time	tCSH	50		60		70		80		ns	
$\overline{CAS}$ pulse width	tCAS	13	10K	15	10K	20	10K	20	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	37	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	15	40	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	
Column address hold time	tCAH	10		10		15		15		ns	
Column address hold time referenced $\overline{RAS}$	tAR	40		45		55		60		ns	15
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		0		ns	
Write command hold time	tWCH	10		10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	tWCR	40		45		55		60		ns	15
Write command pulse width	tWP	10		10		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		15		20		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	13		15		20		20		ns	

Note) *1 : 5V only

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5 *1		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		0		ns	9
Data hold time	tDH	10		10		15		15		ns	9
Data hold time referenced to $\overline{RAS}$	tDHR	40		45		55		60		ns	15
Refresh period(2K, Normal)	tREF		32		32		32		32	ms	
Refresh period(4K, Normal)	tREF		64		64		64		64	ms	
Refresh period(L-ver)	tREF		128		128		128		128	ms	
Refresh period(SL-ver)	tREF		256		256		256		256	ms	
Write command set-up time	tWCS	0		0		0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	36		40		50		50		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	73		85		100		110		ns	7
Column address to $\overline{W}$ delay time	tAWD	48		55		65		70		ns	7
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	5		5		5		5		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		5		ns	
$\overline{CAS}$ precharge time($\overline{CBR}$ counter test cycle)	tCPT	20		20		30		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		30		35		40		45	ns	3
Fast Page mode cycle time	tPC	35		40		45		50		ns	
Fast Page mode read-modify-write cycle time	tPRWC	76		85		100		105		ns	
$\overline{CAS}$ precharge time (Fast page cycle)	tCP	10		10		10		10		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	50	200K	60	200K	70	200K	80	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		45		ns	
$\overline{OE}$ access time	tOEA		13		15		20		20	ns	
$\overline{OE}$ to data delay	tOED	13		15		20		20		ns	
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	53		60		70		75		ns	
Out put buffer turn off delay time from $\overline{OE}$	tOEZ	0	13	0	15	0	20	0	20	ns	
$\overline{OE}$ command hold time	tOEH	13		15		20		20		ns	
Write command set-up time(Test mode in)	tWTS	10		10		10		10		ns	11
Write command hold time(Test mode in)	tWTH	10		10		10		10		ns	11
$\overline{W}$ to $\overline{RAS}$ precharge time($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		10		ns	
$\overline{RAS}$ pulse width($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		100		us	14
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	90		110		130		150		ns	14
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		-50		ns	14

Note) *1 : 5V only

TEST MODE CYCLE

(Note. 11)

Parameter	Symbol	-5*1		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	95		115		135		155		ns	
Read-modify-write cycle time	tRWC	138		160		190		210		ns	
Access time from $\overline{\text{RAS}}$	tRAC		55		65		75		85	ns	3,4,10
Access time from $\overline{\text{CAS}}$	tCAC		18		20		25		25	ns	3,4,5
Access time from column address	tAA		30		35		40		45	ns	3,10
$\overline{\text{RAS}}$ pulse width	tRAS	55	10K	65	10K	75	10K	85	10K	ns	
$\overline{\text{CAS}}$ pulse width	tCAS	18	10K	20	10K	25	10K	25	10K	ns	
$\overline{\text{RAS}}$ hold time	tRSH	18		20		25		25		ns	
$\overline{\text{CAS}}$ hold time	tCSH	55		65		75		85		ns	
Column address to $\overline{\text{RAS}}$ lead time	tRAL	30		35		40		45		ns	
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	tCWD	41		45		55		55		ns	7
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	tRWD	78		90		105		115		ns	7
Column address to $\overline{\text{W}}$ delay time	tAWD	53		60		70		75		ns	7
Fast Page mode cycle time	tPC	40		45		50		55		ns	
Fast page mode read-modify-write cycle time	tPRWC	81		90		105		110		ns	
$\overline{\text{RAS}}$ pulse width (Fast page cycle)	tRASP	55	200K	65	200K	75	200K	85	200K	ns	
Access time form $\overline{\text{CAS}}$ precharge	tCPA		35		40		45		50	ns	3
$\overline{\text{OE}}$ access time	tOEA		18		20		25		25	ns	
$\overline{\text{OE}}$ to data delay	tOED	18		20		25		25		ns	
$\overline{\text{OE}}$ command hold time	tOEH	18		20		25		25		ns	

Note) *1 : 5V only

NOTES

1. An initial pause of 200µs is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL(5V device)/1 TTL(3.3V device) loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If tWCS≥tWCS(min), the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a re ference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
11. These specifications are applied in the test mode.
12. In test mode read cycle, the value of tRAC, tAA, tCAC is delayed by 2ns to 5ns for the specified values. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
13. tOFF(max) and tOEZ(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
14. 4096 (4K Ref.)/2048(2K Ref.) cyclesof burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.
15. tAR, tWCR, and tDHR are referenced to tRAD(MAX).

2M x 8 Bit CMOS Dynamic RAM with Extended Data Out

DESCRIPTION

This is a family of 2,097,152 x 8 bit Extended Data Out CMOS DRAMs. Extended Data Out Mode offers high speed random access of memory cells within the same row, so called Hyper Page Mode. Power supply voltage(+5.0V or +3.3V), refresh cycle(2K Ref. or 4K Ref.), access time(-5, -6, -7 or -8), power consumption(Normal, Low power or Super-Low power) and package type(SOJ or TSOP-II) are optional features of this family. All of this family have $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$-only refresh and Hidden refresh capabilities. Further more, Self-refresh operation is available in L & SL version.

This 2Mx8 EDO DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability. It may be used as main memory unit for high level computer, microcomputer and personal computer.

FEATURES

- Part Identification
  - KM48C2004A/AL/ASL(5V, 4K Ref.)
  - KM48C2104A/AL/ASL(5V, 2K Ref.)
  - KM48V2004A/AL/ASL(3.3V, 4K Ref.)
  - KM48V2104A/AL/ASL(3.3V, 2K Ref.)
- Active Power Dissipation

Unit : mW

Speed	3.3V		5V	
	4K	2K	4K	2K
-5	-	-	495	605
-6	288	360	440	550
-7	252	324	385	495
-8	216	288	330	440

- Refresh cycles

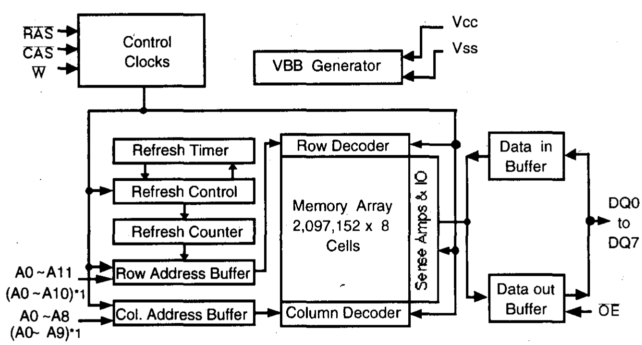
Part NO.	Vcc	Refresh cycle	Refresh period		
			Normal	L	SL
C2004A	5V	4K	64ms	128ms	256ms
V2004A	3.3V				
C2104A	5V	2K	32ms		
V2104A	3.3V				

- Performance range:

Speed	tRAC	tCAC	tRC	tHPC	Remark
-5	50ns	13ns	90ns	20ns	5V Only
-6	60ns	15ns	110ns	25ns	5V/3.3V
-7	70ns	20ns	130ns	30ns	5V/3.3V
-8	80ns	20ns	150ns	35ns	5V/3.3V

- Extended Data Out mode operation (Fast Page mode with Extended data out)
- Byte Read/Write operation
- $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh capability
- $\overline{\text{RAS}}$-only and Hidden refresh capability
- Self-refresh capability(L & SL-ver)
- Fast parallel test mode capability
- TTL(5V)/LVTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC Standard pinout
- Available in Plastic SOJ and TSOP(II) packages
- Single +5V±10% power supply(5V product)
- Single +3.3V±0.3V power supply(3.3V product)

FUNCTIONAL BLOCK DIAGRAM



Note) *1 : 2K Refresh

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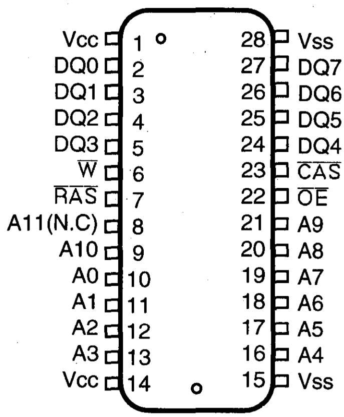
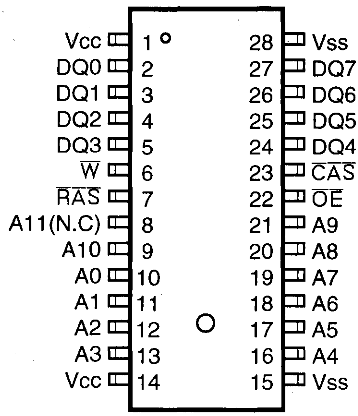
PIN CONFIGURATION (Top Views)

• **KM48C/V20(1)04AJ/ALJ/ASLJ**

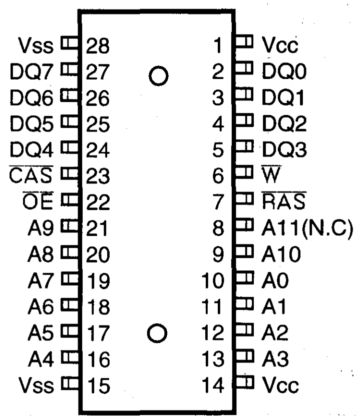


J : 400 mil 28 SOJ
T : 400 mil TSOP II
TR : 400 mil TSOP II(Rev.)

• **KM48C/V20(1)04AT/ALT/ASLT**



• **KM48C/V20(1)04ATR/ALTR/ASLTR**



* Note : ( ) --> 2K Product

Pin Name	Pin Function
A0 - A11	Address Inputs(4K product)
A0 - A10	Address Inputs(2K product)
DQ0 -7	Data In/Out
Vss	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Outputs Enable
Vcc	Power(+3.3V)
	Power(+5.5V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Units
		3.3V	5V	
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to +4.6	-1 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.5 to +4.6	-1 to +7.0	V
Storage Temperature	Tstg	-55 to +150	-55 to +150	°C
Power Dissipation	P_D	1	1	W
Short Circuit Output Current	I_{OS}	50	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A= 0 to 70 °C)

Parameter	Symbol	3.3V			5V			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V_{CC}	3.0	3.3	3.6	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	Vcc+0.3*1	2.4	-	Vcc+1*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	-1.0*2	-	0.8	V

*1 : Vcc + 1.3V/15ns(3.3V), Vcc+2.0V/20ns(5V), Pulse width is measured at Vcc.
*2 : - 1.3V/15ns(3.3V), - 2.0V/20ns(5V), Pulse width is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

	Parameter	Symbol	Min	Max	Units
3.3V	Input Leakage Current (Any input $0 \le V_{IN} \le V_{CC}+0.3V$, all other pins not under test=0 volt.)	$I_{I(L)}$	- 5	5	µA
	Output Leakage Current (Data out is disabled, $0V \le V_{OUT} \le V_{CC}$)	$I_{O(L)}$	- 5	5	µA
	Output High Voltage Level(I_{OH}=-2mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level(I_{OL}=2mA)	V_{OL}	-	0.4	V
5V	Input Leakage Current (Any input $0 \le V_{IN} \le V_{CC}+0.5V$, all other pins not under test=0 volt.)	$I_{I(L)}$	-10	10	µA
	Output Leakage Current (Data out is disabled, $0V \le V_{OUT} \le V_{CC}$)	$I_{O(L)}$	-10	10	µA
	Output High Voltage Level(I_{OH}=-5mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level(I_{OL}=4.2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS (Continued.)

Symbol	Power	Speed	Max				Units
			KM48V2004A	KM48V2104A	KM48C2004A	KM48C2104A	
ICC1	Don't care	-5 -6 -7 -8	- 80 70 60	- 100 90 80	90 80 70 60	110 100 90 80	mA mA mA mA
ICC2	Normal L/SL	Don't care	2 1	2 1	2 1	2 1	mA mA
ICC3	Don't care	-5 -6 -7 -8	- 80 70 60	- 100 90 80	90 80 70 60	110 100 90 80	mA mA mA mA
ICC4	Don't care	-5 -6 -7 -8	- 90 80 70	- 100 90 80	100 90 80 70	110 100 90 80	mA mA mA mA
ICC5	Normal L SL	Don't care	1 300 200	1 300 200	1 300 200	1 300 200	mA µA µA
ICC6	Don't care	-5 -6 -7 -8	- 80 70 60	- 100 90 80	90 80 70 60	110 100 90 80	mA mA mA mA
ICC7	L SL	Don't care	450 350	400 300	450 350	400 300	µA µA
ICCS	L/SL	Don't care	250	250	300	300	µA

I_{CC1}* : Operating Current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}* : $\overline{RAS}$-only Refresh Current ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @tRC=min.)

I_{CC4}* : Hyper Page Mode Current ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address cycling @tHPC=min.)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6}* : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode
Input high voltage(V_{IH})=Vcc-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{CAS}$=$\overline{CAS}$-before-$\overline{RAS}$ cycling or 0.2V
Din = Don't care, T_{RC}= 31.25µs(4K/L-ver), 62.5µs(4K/SL-ver, 2K/L-ver), 125µs(2K/SL-ver) ,
T_{RAS}=T_{RAS}min~300 ns

I_{CCS} : Self Refresh Current
$\overline{RAS}$=$\overline{CAS}$=0.2V, $\overline{W}$=$\overline{OE}$=A0 ~ A11 = Vcc-0.2V or 0.2V, DQ0 ~ DQ7= Vcc-0.2V, 0.2V or Open

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1}, I_{CC3}, and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one hyper page mode cycle time tHPC.

CAPACITANCE(T_A=25°C,Vcc=5V or 3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A11]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ0 - DQ7]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 1,2)
Test condition(5V device) : Vcc=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol} =2.0/0.8V
Test condition(3.3V device) : Vcc=3.3V±0.3V, V_{ih}/V_{il}=2.0/0.8V, V_{oh}/V_{ol} =2.0/0.8V

Parameter	Symbol	-5 *1		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	84		104		124		144		ns	
Read-modify-write cycle time	tRWC	116		140		170		190		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70		80	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		13		15		20		20	ns	3,4,5
Access time from column address	tAA		25		30		35		40	ns	3,10
$\overline{CAS}$ to output in Low-Z	tCLZ	3		3		3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	tCEZ	3	13	3	15	3	20	3	20	ns	6,13
$\overline{OE}$ to output in Low-Z	tOLZ	3		3		3		3		ns	3
Transition time (rise and fall)	tT	2	50	2	50	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		60		ns	
$\overline{RAS}$ pulse width	tRAS	50	10K	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ hold time	tRSH	13		15		20		20		ns	
$\overline{CAS}$ hold time	tCSH	38		45		50		60		ns	
$\overline{CAS}$ pulse width	tCAS	8	10K	10	10K	15	10K	20	10K	ns	15
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	37	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	15	40	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	
Column address hold time	tCAH	8		10		15		15		ns	
Column address hold time referenced $\overline{RAS}$	tAR	35		42		52		57		ns	17
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		0		ns	8
Write command hold time	tWCH	10		10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	tWCR	37		42		52		57		ns	17
Write command pulse width	tWP	10		10		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	13		15		20		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	8		10		15		20		ns	

Note) *1 : 5V only

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5 *1		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		0		ns	9
Data hold time	tDH	8		10		15		15		ns	9
Data hold time referenced to $\overline{RAS}$	tDHR	37		42		52		57		ns	17
Refresh period(2K, Normal)	tREF		32		32		32		32	ms	
Refresh period(4K, Normal)	tREF		64		64		64		64	ms	
Refresh period(L-ver)	tREF		128		128		128		128	ms	
Refresh period(SL-ver)	tREF		256		256		256		256	ms	
Write command set-up time	tWCS	0		0		0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	30		34		44		44		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	67		79		94		104		ns	7
Column address to $\overline{W}$ delay time	tAWD	42		49		59		64		ns	7
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	5		5		5		5		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		15		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		5		ns	
$\overline{CAS}$ precharge time($\overline{CBR}$ counter test cycle)	tCPT	20		20		30		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		28		35		40		45	ns	3
Hyper Page cycle time	tHPC	20		25		30		35		ns	16
Hyper Page read-modify-write cycle time	tHPRWC	47		56		71		81		ns	16
$\overline{CAS}$ precharge time (Hyper page cycle)	tCP	8		10		10		10		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	tRASP	50	200K	60	200K	70	200K	80	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		45		ns	
$\overline{OE}$ access time	tOEA		13		15		20		20	ns	
$\overline{OE}$ to data delay	tOED	13		15		20		20		ns	
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	45		54		64		69		ns	
Out put buffer turn off delay time from $\overline{OE}$	tOEZ	3	13	3	15	3	20	3	20	ns	6,13
$\overline{OE}$ command hold time	tOEH	13		15		20		20		ns	
Write command set-up time(Test mode in)	tWTS	10		10		10		10		ns	11
Write command hold time(Test mode in)	tWTH	10		10		10		10		ns	11
$\overline{W}$ to $\overline{RAS}$ precharge time($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		10		ns	
Output data hold time	tDOH	5		5		5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	tREZ	3	13	3	15	3	20	3	20	ns	6,13
Output buffer turn off delay from $\overline{W}$	tWEZ	3	13	3	15	3	20	3	20	ns	6,13
$\overline{W}$ to data delay	tWED	15		15		20		20		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	tOCH	5		5		5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	tCHO	5		5		5		5		ns	
$\overline{OE}$ precharge time	tOEP	5		5		5		5		ns	
$\overline{W}$ pulth width(Hyper Page Cycle)	tWPE	5		5		5		5		ns	
$\overline{RAS}$ pulse width($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		100		us	14

Note) *1 : 5V only

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5 *1		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	90		110		130		150		ns	14
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		-50		ns	14

TEST MODE CYCLE

(Note. 11)

Parameter	Symbol	-5 *1		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	89		109		129		149		ns	
Read-modify-write cycle time	tRWC	121		145		175		195		ns	
Access time from $\overline{RAS}$	tRAC		55		65		75		85	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		18		20		25		25	ns	3,4,5
Access time from column address	tAA		30		35		40		45	ns	3,10
$\overline{RAS}$ pulse width	tRAS	55	10K	65	10K	75	10K	85	10K	ns	
$\overline{CAS}$ pulse width	tCAS	13	10K	15	10K	20	10K	25	10K	ns	
$\overline{RAS}$ hold time	tRSH	18		20		25		25		ns	
$\overline{CAS}$ hold time	tCSH	43		50		55		65		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		45		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	35		39		49		49		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	72		84		99		109		ns	7
Column address to $\overline{W}$ delay time	tAWD	47		54		64		69		ns	7
Hyper Page cycle time	tHPC	25		30		35		40		ns	16
Hyper page read-modify-write cycle time	tHPRWC	53		61		76		86		ns	16
$\overline{RAS}$ pulse width (Hyper page cycle)	tRASP	55	200K	65	200K	75	200K	85	200K	ns	
Access time form $\overline{CAS}$ precharge	tCPA		33		40		45		50	ns	3
$\overline{OE}$ access time	tOEA		18		20		25		25	ns	
$\overline{OE}$ to data delay	tOED	18		20		25		25		ns	
$\overline{OE}$ command hold time	tOEH	18		20		25		25		ns	

Note) *1 : 5V only

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 2ns for all inputs.
3. Measured with a load equivalent to 2 TTL(5V device)/1 TTL(3.3V device) loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a re ference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If tWCS≥tWCS(min), the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a re ference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
11. These specifications are applied in the test mode.
12. In test mode read cycle, the value of tRAC, tAA, tCAC is delayed by 2ns to 5ns for the specified values. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
13. tCEZ(max), tREZ(max), tWEZ(max) and tOEZ(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
14. 4096(4K Ref.)/2048(2K Ref.) cycles of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.
15. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going.
16. tASC ≥ tCPmin , Assume tT = 2.0 ns
17. tAR, tWCR, and tDHR are referenced to tRAD(MAX).

1M x 16Bit CMOS Dynamic RAM with Fast Page Mode

DESCRIPTION

This is a family of 1,048,576 x16 bit Fast Page Mode CMOS DRAMs. Fast Page Mode offers high speed random access of memory cells within the same row. Power supply voltage(+5.0V or +3.3V), refresh cycle(1K Ref. or 4K Ref.), access time(-6, -7 or -8), power consumption(Normal or Low power) and package type(SOJ or TSOP-II) are optional features of this family.
All of this family have $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$-only refresh and Hidden refresh capabilities. Further more, self-refresh operation is available in self-refresh version.
This 1Mx16 Fast Page mode DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability. It may be used as main memroy unit for microcomputer, personal computer and portable machines.

2

FEATURES

- Part Identification
  - KM416C1000A/A-L (5V, 4K Ref.)
  - KM416C1200A/A-L (5V, 1K Ref.)
  - KM416V1000A/A-L (3.3V, 4K Ref.)
  - KM416V1200A/A-L (3.3V, 1K Ref.)
- Active Power Dissipation Unit : mW

Speed	3.3V		5V	
	4K	1K	4K	1K
-6	324	540	550	880
-7	288	504	495	825
-8	252	468	440	770

- Refresh cycles

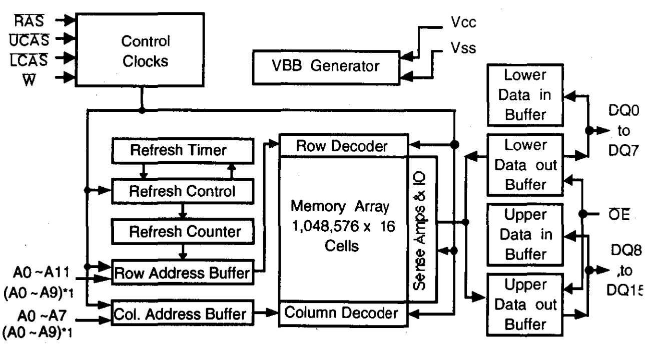
Part NO.	Vcc	Refresh cycle	Refresh time	
			Normal	L-ver
C1000A	5V	4K	64ms	128ms
V1000A	3.3V			
C1200A	5V	1K	16ms	
V1200A	3.3V			

- Performance range:

Speed	tRAC	tCAC	tRC	tPC
-6	60ns	15ns	110ns	40ns
-7	70ns	20ns	130ns	45ns
-8	80ns	20ns	150ns	50ns

- Fast Page Mode operation
- 2 $\overline{\text{CAS}}$ Byte/Word Read/Write operation
- $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh capability
- $\overline{\text{RAS}}$-only and Hidden refresh capability
- Self-refresh capability(L-ver only)
- TTL(5V)/LVTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC Standard pinout
- Available in Plastic SOJ and TSOP(II) packages
- Triple +5V±10% power supply(5V product)
- Triple +3.3V±0.3V power supply(3.3V product)

FUNCTIONAL BLOCK DIAGRAM



Note) *1 : 1K Refresh

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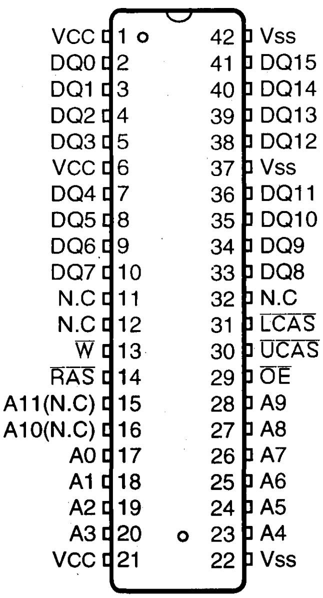
PIN CONFIGURATION (Top Views)

• KM416C/V10(2)00AJ



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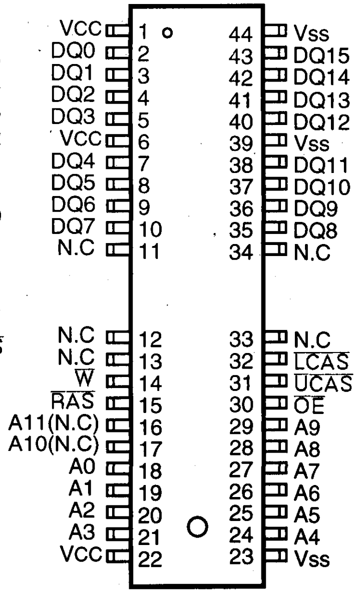
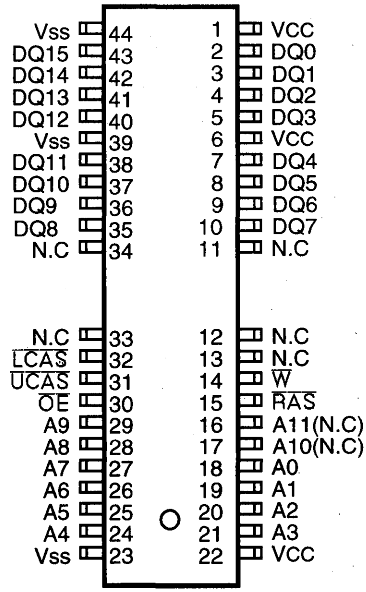


• KM416C/V10(2)00ATR



* Note : ( ) --> 1K Product

Pin Name	Pin Function
A0 - A11	Address Inputs(4K Product)
A0 - A9	Address Inputs(1K Product)
DQ0 -15	Data In/Out
V_{SS}	Ground
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{UCAS}}$	Upper Column Address Strobe
$\overline{\text{LCAS}}$	Lower Column Address Strobe
$\overline{\text{W}}$	Read/Write Input
$\overline{\text{OE}}$	Data Outputs Enable
VCC	Power(+5.0V)
	Power(+3.3V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating 3.3V	Rating 5V	Units
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to +4.6	-1 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.5 to +4.6	-1 to +7.0	V
Storage Temperature	Tstg	-55 to +150	-55 to +150	°C
Power Dissipation	P_D	1	1	W
Short Circuit Output Current	I_{OS}	50	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A= 0 to 70 °C)

Parameter	Symbol	3.3V Min	3.3V Typ	3.3V Max	5V Min	5V Typ	5V Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	0	0	0	V
Input High Voltage	V_{IH}	2.1	-	Vcc+0.3*1	2.4	-	Vcc+1*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	-1.0*2	-	0.8	V

*1 : Vcc + 1.3V/15ns(3.3V), Vcc+2.0V/20ns(5V), Pulse width is measured at Vcc.
*2 : - 1.3V/15ns(3.3V), - 2.0V/20ns(5V), Pulse width is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

	Parameter	Symbol	Min	Max	Units
3.3V	Input Leakage Current (Any input $0 \le V_{IN} \le Vcc+0.3V$, all other pins not under test=0 volt.)	$I_{I(L)}$	- 5	5	μA
	Output Leakage Current (Data out is disabled, $0V \le V_{OUT} \le Vcc$)	$I_{O(L)}$	- 5	5	μA
	Output High Voltage Level(I_{OH}=-2mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level(I_{OL}=2mA)	V_{OL}	-	0.4	V
5V	Input Leakage Current (Any input $0 \le V_{IN} \le Vcc+0.5V$, all other pins not under test=0 volt.)	$I_{I(L)}$	- 5	5	μA
	Output Leakage Current (Data out is disabled, $0V \le V_{OUT} \le Vcc$)	$I_{O(L)}$	- 5	5	μA
	Output High Voltage Level(I_{OH}=-5mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level(I_{OL}=4.2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Symbol	Power	Speed	Max				Units
			KM416V1000A	KM416V1200A	KM416C1000A	KM416C1200A	
I_{CC1}	Don't care	-6 -7 -8	90 80 70	150 140 130	100 90 80	160 150 140	mA mA mA
I_{CC2}	Normal L	Don't care	2 1	2 1	2 1	2 1	mA mA
I_{CC3}	Don't care	-6 -7 -8	90 80 70	150 140 130	100 90 80	160 150 140	mA mA mA
I_{CC4}	Don't care	-6 -7 -8	90 80 70	100 90 80	100 90 80	110 100 90	mA mA mA
I_{CC5}	Normal L	Don't care	1 200	1 200	1 200	1 200	mA µA
I_{CC6}	Don't care	-6 -7 -8	90 80 70	150 140 130	100 90 80	160 150 140	mA mA mA
I_{CC7}	L	Don't care	400	300	450	350	µA
I_{CCS}	L	Don't care	200	200	250	250	µA

I_{CC1}* : Operating Current ($\overline{RAS}$,$\overline{UCAS}$,$\overline{LCAS}$,Address cycling @tRC=min.)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{IH})

I_{CC3}* : $\overline{RAS}$-Only Refresh Current ($\overline{UCAS}$=$\overline{LCAS}$=V_{IH}, $\overline{RAS}$,Address cycling @tRC=min.)

I_{CC4}* : Fast Page Mode Current ($\overline{RAS}$=V_{IL}, $\overline{UCAS}$ or $\overline{LCAS}$, Address cycling @tPC=min.)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{CC}-0.2V)

I_{CC6}* : $\overline{CAS}$-before-$\overline{RAS}$ Refresh Current ($\overline{RAS}$, $\overline{UCAS}$ or $\overline{LCAS}$ cycling @tRC=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode
Input high voltage(V_{IH})=V_{CC}-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{UCAS}$,$\overline{LCAS}$= 0.2V,
Din = Don't care, T_{RC}= 31.25µs(4K/L-ver), 125µs(1K/L-ver), T_{RAS}=T_{RAS}min~300 ns

I_{CCS} : Self Refresh Current
$\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=V_{IL}, $\overline{W}$=$\overline{OE}$=A0 ~ A11 = V_{CC}-0.2V or 0.2V,
DQ0 ~ DQ15= V_{CC}-0.2V, 0.2V or Open

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1}, I_{CC3}, and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one fast page mode cycle time tPC.

CAPACITANCE(T_A=25°C,Vcc=5V or 3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A11]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{UCAS}$,$\overline{LCAS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ0 - DQ15]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 2)
Test condition(5V device) : Vcc=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.4/0.4V
Test condition(3.3V device) : Vcc=3.3V±0.3V, V_{ih}/V_{il}=2.1/0.8V, V_{oh}/V_{ol}=2.0/0.8V

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	110		130		150		ns	
Read-modify-write cycle time	tRWC	155		185		205		ns	
Access time from $\overline{RAS}$	tRAC		60		70		80	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		15		20		20	ns	3,4,5
Access time from column address	tAA		30		35		40	ns	3,10
$\overline{CAS}$ to output in Low-Z	tCLZ	0		0		0		ns	3
Output buffer turn-off delay	tOFF	0	15	0	15	0	15	ns	6
Transition time (rise and fall)	tT	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	tRP	40		50		60		ns	
$\overline{RAS}$ pulse width	tRAS	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ hold time	tRSH	15		20		20		ns	
$\overline{CAS}$ hold time	tCSH	60		70		80		ns	
$\overline{CAS}$ pulse width	tCAS	15	10K	20	10K	20	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	30	15	35	15	40	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	11
Column address hold time	tCAH	10		15		15		ns	11
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		ns	8
Write command set-up time	tWCS	0		0		0		ns	7
Write command hold time	tWCH	10		15		15		ns	
Write command pulse width	tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		15		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	15		15		20		ns	

AC CHARACTERISTICS (0°C≤TA≤70°C, See note 2)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		ns	9,17
Data hold time	tDH	10		15		15		ns	9,17
Refresh period(1K, Normal)	tREF		16		16		16	ms	
Refresh period(4K, Normal)	tREF		64		64		64	ms	
Refresh period(L -ver)	tREF		128		128		128	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	40		50		50		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	85		95		105		ns	7
Column address to $\overline{W}$ delay time	tAWD	55		60		65		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	60		65		70		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	5		5		5		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		ns	
$\overline{CAS}$ precharge time($\overline{C}$B$\overline{R}$ counter test cycle)	tCPT	20		25		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		35		40		45	ns	3
Fast Page mode cycle time	tPC	40		45		50		ns	
Fast Page mode read-modify-write cycle time	tPRWC	80		95		100		ns	
$\overline{CAS}$ precharge time (Fast page cycle)	tCP	10		10		10		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	60	200K	70	200K	80	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	35		40		45		ns	
$\overline{OE}$ access time	tOEA		15		20		20	ns	3
$\overline{OE}$ to data delay	tOED	15		20		20		ns	
Out put buffer turn off delay time from $\overline{OE}$	tOEZ	0	15	0	20	0	20	ns	
$\overline{OE}$ command hold time	tOEH	15		20		20		ns	
$\overline{RAS}$ pulse width($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		us	18
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	110		130		150		ns	18
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		ns	18

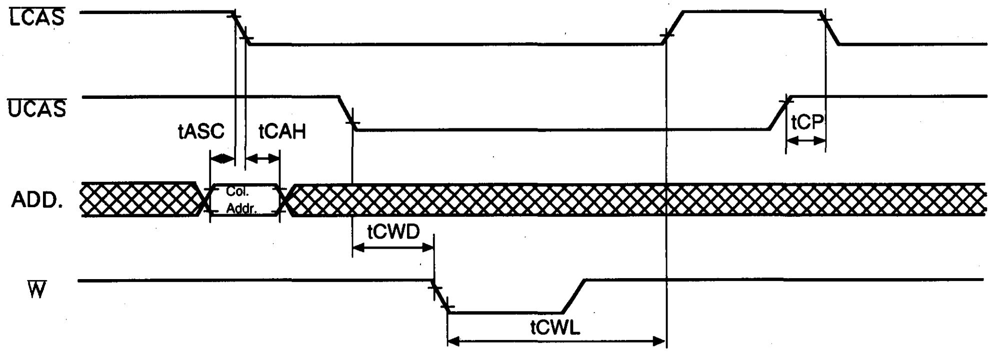
NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL (5V device)/ 1 TTL(3.3V device) loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. tOFF(max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS≥ tWCS(min), the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥ tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.

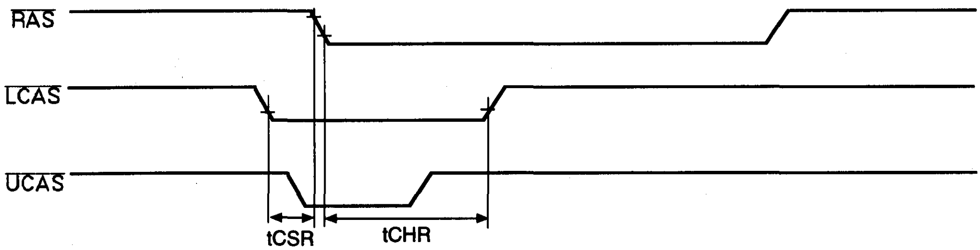
KM416C/V10(2)00A/A-L Truth Table

$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	DQ0 -DQ7	DQ8 - DQ15	STATE
H	X	X	X	X	Hi-Z	Hi-Z	Standby
L	H	H	X	X	Hi-Z	Hi-Z	Refresh
L	L	H	H	L	DQ-OUT	Hi-Z	Byte Read
L	H	L	H	L	Hi-Z	DQ-OUT	Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-IN	-	Byte Write
L	H	L	L	H	-	DQ-IN	Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	Hi-Z	Hi-Z	-

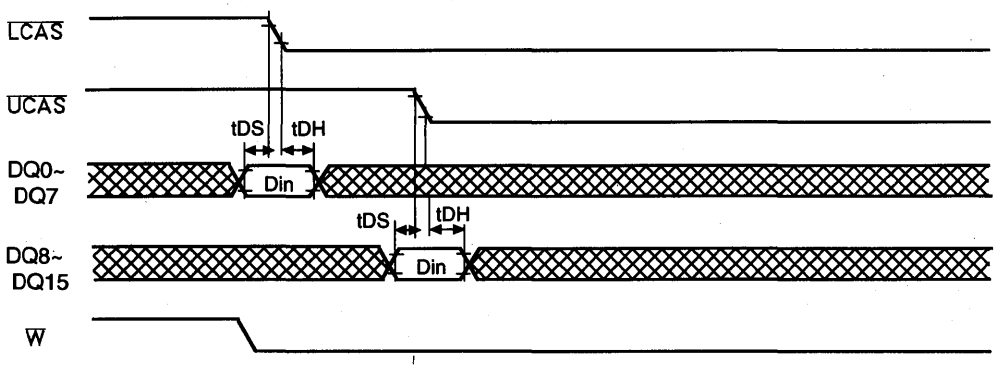
11. tASC, tCAH are referenced to the earlier $\overline{CAS}$ falling edge.
12. tCP is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.
13. tCWD is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.
14. tCWL is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.



15. tCSR is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.
16. tCHR is referenced to the later $\overline{CAS}$ rising high after $\overline{RAS}$ transition low.



17. tDS, tDH is independently specified for lower byte D_{IN}(0~7), upper byte D_{IN}(8~15).



18. 4096 cycle(1024 cycle) of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification(L-version).

1M x 16Bit CMOS Dynamic RAM with Extended Data Out

DESCRIPTION

This is a family of 1,048,576 x16 bit Dxtended Data Out CMOS DRAMs. Dxtended Data Out mode offers high speed random access of memory cells within the same row, so called Hyper Page Mode. Power supply voltage(+5.0V or +3.3V), refresh cycle(1K Ref. or 4K Ref.), access time(-6, -7 or -8), power consumption(Normal or Low power) and package type(SOJ or TSOP-II) are optional features of this family. All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities. Further more, self-refresh operation is available in Low power version.

This 1Mx16 Extended Data Out mode DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability. It may be used as main memroy unit for microcomputer, personal computer and portable machines.

2

FEATURES

- Part Identification
  - KM416C1004A/A-L (5V, 4K Ref.)
  - KM416C1204A/A-L (5V, 1K Ref.)
  - KM416V1004A/A-L (3.3V, 4K Ref.)
  - KM416V1204A/A-L (3.3V, 1K Ref.)

- Active Power Dissipation

Unit : mW

Speed	3.3V		5V	
	4K	1K	4K	1K
-6	324	540	550	880
-7	288	504	495	825
-8	252	468	440	770

- Extended Data Out mode operation (Fast Page mode with Extended Data Out)
- 2$\overline{CAS}$ Byte/Word Read/Write operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- Self-refresh capability(L-ver only)
- TTL(5V)/LVTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC Standard pinout
- Available in Plastic SOJ and TSOP(II) packages
- Triple +5V±10% power supply(5V product)
- Triple +3.3V±0.3V power supply(3.3V product)

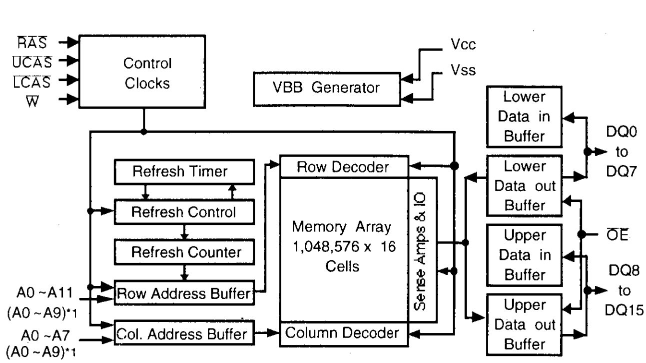
- Refresh cycles

Part NO.	Vcc	Refresh cycle	Refresh period	
			Normal	L-ver
C1004A	5V	4K	64ms	128ms
V1004A	3.3V			
C1204A	5V	1K	16ms	
V1204A	3.3V			

- Performance range:

Speed	tRAC	tCAC	tRC	tHPC
-6	60ns	17ns	104ns	25ns
-7	70ns	20ns	124ns	30ns
-8	80ns	20ns	144ns	35ns

FUNCTIONAL BLOCK DIAGRAM



Note) *1 : 1K Refresh

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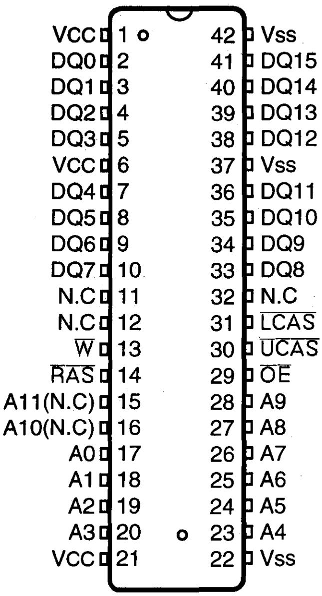
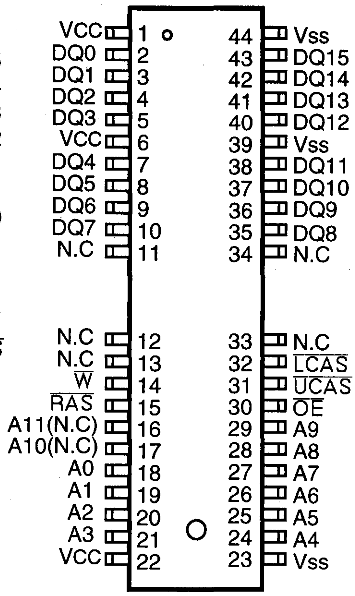
PIN CONFIGURATION (Top Views)

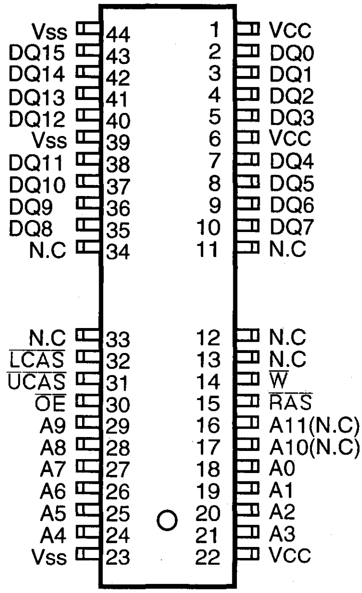
• KM416C/V10(2)04AJ



• KM416C/V10(2)04AT



• KM416C/V10(2)04ATR



* Note : (N.C) --> 1K Product

Pin Name	Pin Function
A0 - A11	Address Inputs(4K Product)
A0 - A9	Address Inputs(1K Product)
DQ0 -15	Data In/Out
V_{SS}	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Upper Column Address Strobe
$\overline{LCAS}$	Lower Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Outputs Enable
Vcc	Power(+5.0V)
	Power(+3.3V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Units
		3.3V	5V	
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to +4.6	-1 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.5 to +4.6	-1 to +7.0	V
Storage Temperature	Tstg	-55 to +150	-55 to +150	°C
Power Dissipation	P_D	1	1	W
Short Circuit Output Current	I_{OS}	50	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to Vss, T_A= 0 to 70 °C)

Parameter	Symbol	3.3V			5V			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V_{CC}	3.0	3.3	3.6	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	0	0	0	V
Input High Voltage	V_{IH}	2.1	-	Vcc+0.3*1	2.4	-	Vcc+1*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	-1.0*2	-	0.8	V

*1 : Vcc + 1.3V/15ns(3.3V), Vcc+2.0V/20ns(5V), Pulse width is measured at Vcc.
*2 : - 1.3V/15ns(3.3V), - 2.0V/20ns(5V), Pulse width is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

	Parameter	Symbol	Min	Max	Units
3.3V	Input Leakage Current (Any input $0 \le V_{IN} \le Vcc+0.3V$, all other pins not under test=0 volt.)	$I_{I(L)}$	- 5	5	μA
	Output Leakage Current (Data out is disabled, $0V \le V_{OUT} \le Vcc$)	$I_{O(L)}$	- 5	5	μA
	Output High Voltage Level(I_{OH}=-2mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level(I_{OL}=2mA)	V_{OL}	-	0.4	V
5V	Input Leakage Current (Any input $0 \le V_{IN} \le Vcc+0.5V$, all other pins not under test=0 volt.)	$I_{I(L)}$	- 5	5	μA
	Output Leakage Current (Data out is disabled, $0V \le V_{OUT} \le Vcc$)	$I_{O(L)}$	- 5	5	μA
	Output High Voltage Level(I_{OH}=-5mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level(I_{OL}=4.2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Symbol	Power	Speed	Max				Units
			KM416V1004A	KM416V1204A	KM416C1004A	KM416C1204A	
I_{CC1}	Don't care	-6 -7 -8	90 80 70	150 140 130	100 90 80	160 150 140	mA mA mA
I_{CC2}	Normal L	Don't care	2 1	2 1	2 1	2 1	mA mA
I_{CC3}	Don't care	-6 -7 -8	90 80 70	150 140 130	100 90 80	160 150 140	mA mA mA
I_{CC4}	Don't care	-6 -7 -8	110 100 90	120 110 100	120 110 100	130 120 110	mA mA mA
I_{CC5}	Normal L	Don't care	1 200	1 200	1 200	1 200	mA µA
I_{CC6}	Don't care	-6 -7 -8	90 80 70	150 140 130	100 90 80	160 150 140	mA mA mA
I_{CC7}	L	Don't care	400	400	450	350	µA
I_{CCS}	L	Don't care	200	200	250	250	µA

I_{CC1}* : Operating Current ($\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, Address cycling @tRC=min.)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{IH})

I_{CC3}* : $\overline{RAS}$-Only Refresh Current ($\overline{UCAS}$=$\overline{LCAS}$=V_{IH}, $\overline{RAS}$, Address cycling @tRC=min.)

I_{CC4}* : Hyper Page Mode Current ($\overline{RAS}$=V_{IL}, $\overline{UCAS}$ or $\overline{LCAS}$, Address cycling @tHPC=min.)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{CC}-0.2V)

I_{CC6}* : $\overline{CAS}$-before-$\overline{RAS}$ Refresh Current ($\overline{RAS}$, $\overline{UCAS}$ or $\overline{LCAS}$ cycling @tRC=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode
Input high voltage(V_{IH})=V_{CC}-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{UCAS}$, $\overline{LCAS}$= 0.2V,
Din = Don't care, T_{RC}= 31.25µs(4K/L-ver), 125µs(1K/L-ver), T_{RAS}=T_{RAS}min~300 ns

I_{CCS} : Self Refresh Current
$\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=V_{IL}, $\overline{W}$=$\overline{OE}$=A0 ~ A11 = V_{CC}-0.2V or 0.2V,
DQ0 ~ DQ15= V_{CC}-0.2V, 0.2V or Open

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1}, I_{CC3}, and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one hyper page mode cycle time tHPC.

CAPACITANCE(T_A=25°C,Vcc=5V or 3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A11]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{UCAS}$,$\overline{LCAS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ0 - DQ15]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 2)
Test condition(5V device) : Vcc=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.0/0.8V
Test condition(3.3V device) : Vcc=3.3V±0.3V, V_{ih}/V_{il}=2.1/0.8V, V_{oh}/V_{ol}=2.0/0.8V

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	104		124		144		ns	
Read-modify-write cycle time	tRWC	140		170		190		ns	
Access time from $\overline{RAS}$	tRAC		60		70		80	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		17		20		20	ns	3,4,5
Access time from column address	tAA		30		35		40	ns	3,10
$\overline{CAS}$ to output in Low-Z	tCLZ	3		3		3		ns	3
$\overline{OE}$ to output in Low-Z	tOLZ	3		3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	tCEZ	3	15	3	20	3	20	ns	6,13
Transition time (rise and fall)	tT	2	50	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	tRP	40		50		60		ns	
$\overline{RAS}$ pulse width	tRAS	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ hold time	tRSH	17		20		20		ns	
$\overline{CAS}$ hold time	tCSH	50		60		70		ns	
$\overline{CAS}$ pulse width	tCAS	10	10K	15	10K	20	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	43	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	30	15	35	15	40	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	14
Column address hold time	tCAH	10		15		15		ns	14
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		ns	8
Write command set-up time	tWCS	0		0		0		ns	7
Write command hold time	tWCH	10		15		15		ns	
Write command pulse width	tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		20		20		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Write command to $\overline{CAS}$ lead time	tCWL	10		15		20		ns	17
Data set-up time	tDS	0		0		0		ns	9,20
Data hold time	tDH	10		15		15		ns	9,20
Refresh period(1K, Normal)	tREF		16		16		16	ms	
Refresh period(4K, Normal)	tREF		64		64		64	ms	
Refresh period(L -ver)	tREF		128		128		128	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	36		44		44		ns	7,16
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	79		94		104		ns	7
Column address to $\overline{W}$ delay time	tAWD	49		59		64		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	54		64		69		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	5		5		10		ns	18
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		10		ns	19
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		ns	
$\overline{CAS}$ precharge time($\overline{CBR}$ counter test cycle)	tCPT	20		25		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		35		40		45	ns	3
Hyper Page mode cycle time	tHPC	25		30		35		ns	11
Hyper Page mode read-modify-write cycle time	tHPRWC	56		71		81		ns	11
$\overline{CAS}$ precharge time Hyper page cycle)	tCP	10		10		10		ns	15
$\overline{RAS}$ pulse width (Hyper page cycle)	tRASP	60	200K	70	200K	80	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	35		40		45		ns	
$\overline{OE}$ access time	tOEA		15		20		20	ns	3
$\overline{OE}$ to data delay	tOED	15		20		20		ns	
Out put buffer turn off delay time from $\overline{OE}$	tOEZ	3	15	3	20	3	20	ns	6
$\overline{OE}$ command hold time	tOEH	15		20		20		ns	
Output data hold time	tDOH	5		5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	tREZ	3	15	3	20	3	20	ns	6,13
Output buffer turn off delay from $\overline{W}$	tWEZ	3	15	3	20	3	20	ns	6
$\overline{W}$ to data delay	tWED	15		20		20		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	tOCH	5		5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	tCHO	5		5		5		ns	
$\overline{OE}$ precharge time	tOEP	5		5		5		ns	
$\overline{W}$ pulse width	tWPE	5		5		5		ns	
$\overline{RAS}$ pulse width($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		us	12
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	110		130		150		ns	12
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		ns	12

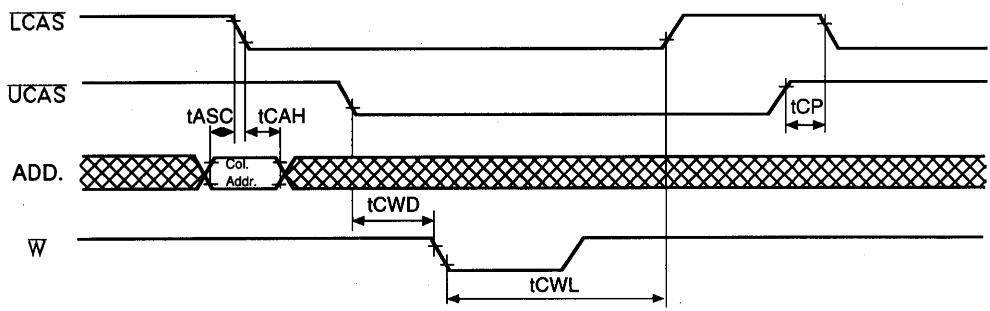
NOTES

1. An initial pause of 200µs is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 2ns for all inputs.
3. Measured with a load equivalent to 2 TTL (5V device)/ 1 TTL(3.3V device) loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS≥ tWCS(min), the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥ tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.

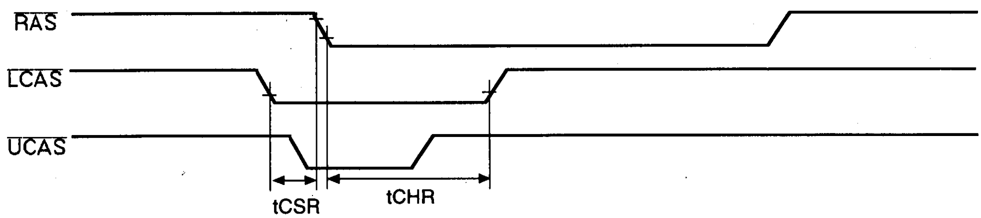
KM416C/V10(2)04A/A-L Truth Table

$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	DQ0 -DQ7	DQ8- DQ15	STATE
H	X	X	X	X	Hi-Z	Hi-Z	Standby
L	H	H	X	X	Hi-Z	Hi-Z	Refresh
L	L	H	H	L	DQ-OUT	Hi-Z	Byte Read
L	H	L	H	L	Hi-Z	DQ-OUT	Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-IN	-	Byte Write
L	H	L	L	H	-	DQ-IN	Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	Hi-Z	Hi-Z	-

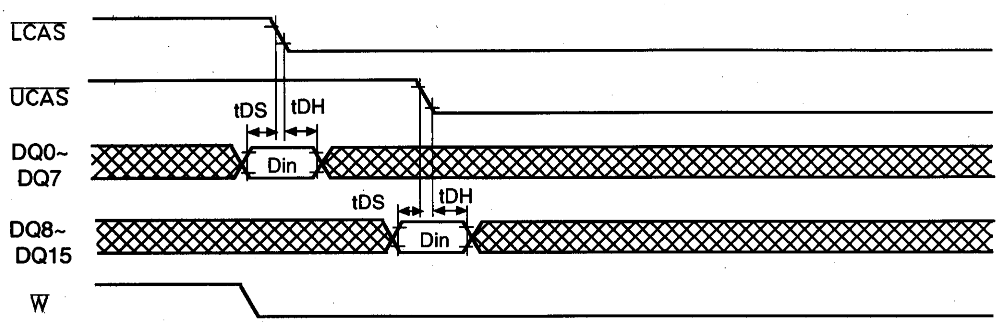
11. tASC≥ 6 ns, Assume tT = 2.0 ns
12. 4096 cycle(1024 cycle) of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification(L-version).
13. If $\overline{RAS}$ goes to high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes to high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going.
14. tASC, tCAH are referenced to the earlier $\overline{CAS}$ falling edge.
15. tCP is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.
16. tCWD is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.
17. tCWL is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.



18. tCSR is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.
19. tCHR is referenced to the later $\overline{CAS}$ rising high after $\overline{RAS}$ transition low.



20. tDS, tDH is independently specified for lower byte DIN(0~7), upper byte DIN(8~15).



512K x 32Bit CMOS Dynamic RAM with Fast Page Mode

DESCRIPTION

This is a family of 524,288 x 32 bit Fast Page Mode CMOS DRAMs. Fast Page Mode offers high speed random access of memory cells within the same row. Refresh cycle(1K Ref. or 4K Ref.), access time(-7 or -8), power consumption(Normal or Low power) are optional features of this family.
All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities. Further more, self-refresh operation is available in Low power version.
This 512Kx32 Fast Page mode DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability.

FEATURES

- Part Identification
  - KM432V502/-L (3.3V, 4K Ref.)
  - KM432V522/-L (3.3V, 1K Ref.)

- Active Power Dissipation

Unit : mW

Speed	Active Power Dissipation	
	4K	1K
-7	324	504
-8	288	468

- Refresh cycles

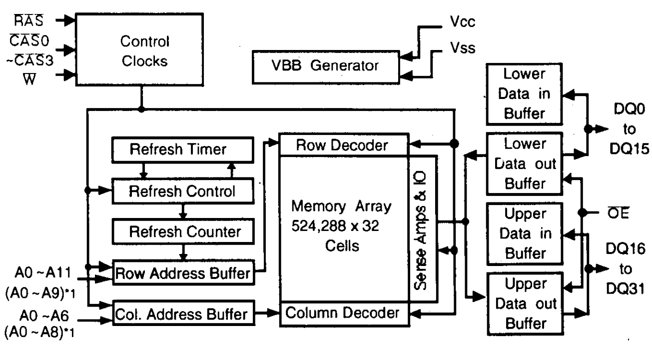
Part NO.	Refresh cycle	Refresh time	
		Normal	L-ver
V502	4K	64ms	128ms
V522	1K	16ms	

- Performance range:

Speed	tRAC	tCAC	tRC	tPC
-7	70ns	20ns	130ns	45ns
-8	80ns	20ns	150ns	50ns

- Fast Page Mode operation
- 4 $\overline{CAS}$ Byte/Word Read/Write operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- Self-refresh capability(L-ver only)
- LVTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC Standard pinout
- Available in TSOP(II) package
- Single +3.3V$\pm$0.3V power supply

FUNCTIONAL BLOCK DIAGRAM



Note) *1 : 1K Refresh

PIN CONFIGURATION (Top Views)

• KM432V502T

Vcc	1	70	VSS
DQ0	2	69	DQ31
DQ1	3	68	DQ30
DQ2	4	67	DQ29
DQ3	5	66	DQ28
Vcc	6	65	VSS
DQ4	7	64	DQ27
DQ5	8	63	DQ26
DQ6	9	62	DQ25
DQ7	10	61	DQ24
N.C	11	60	N.C
Vcc	12	59	VSS
DQ8	13	58	DQ23
DQ9	14	57	DQ22
DQ10	15	56	DQ21
DQ11	16	55	DQ20
Vcc	17	54	VSS
DQ12	18	53	DQ19
DQ13	19	52	DQ18
DQ14	20	51	DQ17
DQ15	21	50	DQ16
N.C	22	49	N.C
N.C	23	48	$\overline{CAS}$0
N.C	24	47	$\overline{CAS}$1
N.C	25	46	$\overline{CAS}$2
N.C	26	45	$\overline{CAS}$3
$\overline{RAS}$	27	44	$\overline{W}$
A0	28	43	$\overline{OE}$
A1	29	42	N.C
A2	30	41	A11(N.C)
A3	31	40	A10(N.C)
A4	32	39	A9
A5	33	38	A8
A6	34	37	A7
Vcc	35	36	VSS

• KM432V502R

VSS	70	1	Vcc
DQ31	69	2	DQ0
DQ30	68	3	DQ1
DQ29	67	4	DQ2
DQ28	66	5	DQ3
VSS	65	6	Vcc
DQ27	64	7	DQ4
DQ26	63	8	DQ5
DQ25	62	9	DQ6
DQ24	61	10	DQ7
N.C	60	11	N.C
VSS	59	12	Vcc
DQ23	58	13	DQ8
DQ22	57	14	DQ9
DQ21	56	15	DQ10
DQ20	55	16	DQ11
VSS	54	17	Vcc
DQ19	53	18	DQ12
DQ18	52	19	DQ13
DQ17	51	20	DQ14
DQ16	50	21	DQ15
N.C	49	22	N.C
$\overline{CAS}$0	48	23	N.C
$\overline{CAS}$1	47	24	N.C
$\overline{CAS}$2	46	25	N.C
$\overline{CAS}$3	45	26	N.C
$\overline{W}$	44	27	$\overline{RAS}$
$\overline{OE}$	43	28	A0
N.C	42	29	A1
A11(N.C)	41	30	A2
A10(N.C)	40	31	A3
A9	39	32	A4
A8	38	33	A5
A7	37	34	A6
VSS	36	35	Vcc

* (N.C) : 1K Ref. Product

Pin Name	Pin Function
A0 - A11	Address Inputs
DQ0 -31	Data In/Out
Vss	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$0	1st Byte Column Address Strobe
$\overline{CAS}$1	2nd Byte Column Address Strobe
$\overline{CAS}$2	3rd Byte Column Address Strobe
$\overline{CAS}$3	4th Byte Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Outputs Enable
Vcc	Power(+3.3V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-0.5 to Vcc+0.5V	V
Voltage on Vcc supply relative to Vss	V_{CC}	-0.5 to +4.6	V
Storage Temperature	Tstg	-55 to +150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to Vss, T_A= 0 to 70 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	-	Vcc+0.3 *1	V
Input Low Voltage	V_{IL}	-0.3 *2	-	0.8	V

* 1 : Vcc+1.3V at pulse width ≤ 15ns (pulse width is measured at Vcc)
*2 : -1.3V at pulse width ≤ 15ns (pulse width is measured at Vss)

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input $0 \le V_{IN} \le$ Vcc+0.3V, all other pins not under test=0 volt.)	$I_{I(L)}$	- 5	5	µA
Output Leakage Current (Data out is disabled, $0V \le V_{OUT} \le Vcc$)	$I_{O(L)}$	- 5	5	µA
Output High Voltage Level(I_{oh}=-2mA)	V_{OH}	2.4	-	V
Output Low Voltage Level(I_{OL}=2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS (Continued)

Symbol	Power	Speed	Max		Units
			KM432V502	KM432V522	
I_{CC1}	Don't care	-7 -8	80 70	140 130	mA mA
I_{CC2}	Don't care	Don't care	1	1	mA
I_{CC3}	Don't care	-7 -8	80 70	140 130	mA mA
I_{CC4}	Don't care	-7 -8	70 60	80 70	mA mA
I_{CC5}	Don't care	Don't care	500	500	µA
I_{CC6}	Don't care	-7 -8	80 70	140 130	mA mA
I_{CC7}	L	Don't care	450	350	µA
I_{CCS}	L	Don't care	200	200	µA

I_{CC1}* : Operating Current ($\overline{RAS}$,$\overline{XCAS}$,Address cycling @tRC=min.)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{XCAS}$=$\overline{W}$=V_{IH})

I_{CC3}* : $\overline{RAS}$-Only Refresh Current ($\overline{XCAS}$=V_{IH}, $\overline{RAS}$,Address cycling @tRC=min.)

I_{CC4}* : Fast Page Mode Current ($\overline{RAS}$=V_{IL}, $\overline{XCAS}$, Address cycling @tPC=min.)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{XCAS}$=$\overline{W}$=V_{CC}-0.2V)

I_{CC6}* : $\overline{CAS}$-before-$\overline{RAS}$ Refresh Current ($\overline{RAS}$ and $\overline{XCAS}$ cycling @tRC=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode
Input high voltage(V_{IH})=V_{CC}-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{XCAS}$= 0.2V,
Din = Don't care, Extended T_{RC}= 32.3µs(4K)/125µs(1K), T_{RAS}=T_{RAS}min~200 ns

I_{CCS} : Self Refresh Current
$\overline{RAS}$=$\overline{XCAS}$=0.2V, $\overline{W}$=$\overline{OE}$=A0 ~ A11 = V_{CC}-0.2V or 0.2V,
DQ0 ~ DQ31= V_{CC}-0.2V, 0.2V or Open

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1}, I_{CC3}, and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one fast page mode cycle time tPC.

CAPACITANCE(T_A=25°C,Vcc= 3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A11]	C_{IN1}	-	6	pF
Input capacitance [$\overline{\text{RAS}}$, $\overline{\text{XCAS}}$, $\overline{\text{W}}$, $\overline{\text{OE}}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ0 - DQ31]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 2)
Test condition : Vcc=3.3V±0.3V, V_{ih}/V_{il} =2.2/0.8V, V_{oh}/V_{ol} =2.0/0.8V, Output Loading C_L = 50pF

Parameter	Symbol	- 7		- 8		Units	Notes
		Min	Max	Min	Max		
Random read or write cycle time	tRC	130		150		ns	
Read-modify-write cycle time	tRWC	185		205		ns	
Access time from $\overline{\text{RAS}}$	tRAC		70		80	ns	3,4,10
Access time from $\overline{\text{CAS}}$	tCAC		20		20	ns	3,4,5
Access time from column address	tAA		35		40	ns	3,10
$\overline{\text{CAS}}$ to output in Low-Z	tCLZ	0		0		ns	3
Output buffer turn-off delay	tOFF	0	15	0	15	ns	6
Transition time (rise and fall)	tT	3	50	3	50	ns	2
$\overline{\text{RAS}}$ precharge time	tRP	50		60		ns	
$\overline{\text{RAS}}$ pulse width	tRAS	70	10K	80	10K	ns	
$\overline{\text{RAS}}$ hold time	tRSH	20		20		ns	
$\overline{\text{CAS}}$ hold time	tCSH	70		80		ns	
$\overline{\text{CAS}}$ pulse width	tCAS	20	10K	20	10K	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	tRCD	20	50	20	60	ns	4
$\overline{\text{RAS}}$ to column address delay time	tRAD	15	35	15	40	ns	10
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	tCRP	5		5		ns	
Row address set-up time	tASR	0		0		ns	
Row address hold time	tRAH	10		10		ns	
Column address set-up time	tASC	0		0		ns	
Column address hold time	tCAH	15		15		ns	
Column address to $\overline{\text{RAS}}$ lead time	tRAL	35		40		ns	
Read command set-up time	tRCS	0		0		ns	
Read command hold time referenced to $\overline{\text{CAS}}$	tRCH	0		0		ns	8
Read command hold time referenced to $\overline{\text{RAS}}$	tRRH	0		0		ns	8
Write command set-up time	tWCS	0		0		ns	7
Write command hold time	tWCH	15		15		ns	
Write command pulse width	tWP	15		15		ns	
Write command to $\overline{\text{RAS}}$ lead time	tRWL	15		20		ns	
Write command to $\overline{\text{CAS}}$ lead time	tCWL	15		20		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-7		-8		Units	Notes
		Min	Max	Min	Max		
Data set-up time	tDS	0		0		ns	9
Data hold time	tDH	15		15		ns	9
Refresh period(1K, Normal)	tREF		16		16	ms	
Refresh period(4K, Normal)	tREF		64		64	ms	
Refresh period(L -ver)	tREF		128		128	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	50		50		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	95		105		ns	7
Column address to $\overline{W}$ delay time	tAWD	60		65		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	65		70		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	5		5		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		ns	
$\overline{CAS}$ precharge time($\overline{C}$B$\overline{R}$ counter test cycle)	tCPT	25		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		40		45	ns	3
Fast Page mode cycle time	tPC	45		50		ns	
Fast Page mode read-modify-write cycle time	tPRWC	95		100		ns	
$\overline{CAS}$ precharge time (Fast page cycle)	tCP	10		10		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	70	200K	80	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	40		45		ns	
$\overline{OE}$ access time	tOEA		20		20	ns	
$\overline{OE}$ to data delay	tOED	20		20		ns	
Out put buffer turn off delay time from $\overline{OE}$	tOEZ	0	20	0	20	ns	
$\overline{OE}$ command hold time	tOEH	20		20		ns	
$\overline{RAS}$ pulse width($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		us	18
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	130		150		ns	18
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		ns	18

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{\text{RAS}}$-only or $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 1 TTL loads and 50pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. tOFF(max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS≥ tWCS(min), the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥ tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{\text{CAS}}$ leading edge in early write cycles and to the $\overline{\text{W}}$ leading edge in read-modify-write cycles.

2

KM432V50(2)2 Truth Table

$\overline{\text{RAS}}$	$\overline{\text{CAS1}}$	$\overline{\text{CAS2}}$	$\overline{\text{CAS3}}$	$\overline{\text{CAS4}}$	$\overline{\text{W}}$	$\overline{\text{OE}}$	DQ0 -DQ7	DQ8 - DQ15	DQ16 - DQ23	DQ24 - DQ31	STATE
H	X	X	X	X	X	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Standby
L	H	H	H	H	X	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Refresh
L	L	H	H	H	H	L	DQ-OUT	Hi-Z	Hi-Z	Hi-Z	Byte Read
L	H	L	H	H	H	L	Hi-Z	DQ-OUT	Hi-Z	Hi-Z	Byte Read
L	H	H	L	H	H	L	Hi-Z	Hi-Z	DQ-OUT	Hi-Z	Byte Read
L	H	H	H	L	H	L	Hi-Z	Hi-Z	Hi-Z	DQ-OUT	Byte Read
L	L	L	L	L	H	L	DQ-OUT	DQ-OUT	DQ-OUT	DQ-OUT	2Word Read
L	L	H	H	H	L	H	DQ-IN	-	-	-	Byte Write
L	H	L	H	H	L	H	-	DQ-IN	-	-	Byte Write
L	H	H	L	H	L	H	-	-	DQ-IN	-	Byte Write
L	H	H	H	L	L	H	-	-	-	DQ-IN	Byte Write
L	L	L	L	L	L	H	DQ-IN	DQ-IN	DQ-IN	DQ-IN	2Word Write
L	L	L	L	L	H	H	Hi-Z	Hi-Z	Hi-Z	Hi-Z	-

SAMSUNG ELECTRONICS

10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
11. tASC, tCAH are referenced to the earlier $\overline{CAS}$ falling edge.
12. tCP is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.
13. tCWD is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.
14. tCWL is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.
15. tCSR is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.
16. tCHR is referenced to the later $\overline{CAS}$ rising high after $\overline{RAS}$ transition low.
17. tDS, tDH is independently specified for 1st byte D_{IN}(0~7), 2nd byte D_{IN}(8~15), 3rd byte D_{IN}(16~23), 4th byte D_{IN}(24~31).
18. 4096 cycle(1024 cycle) of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification(L-version).

512Kx 32Bit CMOS Dynamic RAM with Extended Data Out

DESCRIPTION

This is a family of 524,288 x32 bit Extended Data Out CMOS DRAMs. Extended Data Out mode offers high speed random access of memory cells within the same row, so called Hyper Page Mode. Refresh cycle (1K Ref. or 4K Ref.), access time (-7 or -8), power consumption(Normal or Low power) are optional features of this family.

All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities. Further more, self-refresh operation is available in Low power version.

This 512Kx32 Extended Data Out mode DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability.

FEATURES

- Part Identification
  - KM432V504/-L (3.3V, 4K Ref.)
  - KM432V524/-L (3.3V, 1K Ref.)

- Active Power Dissipation Unit : mW

Speed	Active Power Dissipation	
	4K	1K
-7	324	504
-8	288	468

- Refresh cycles

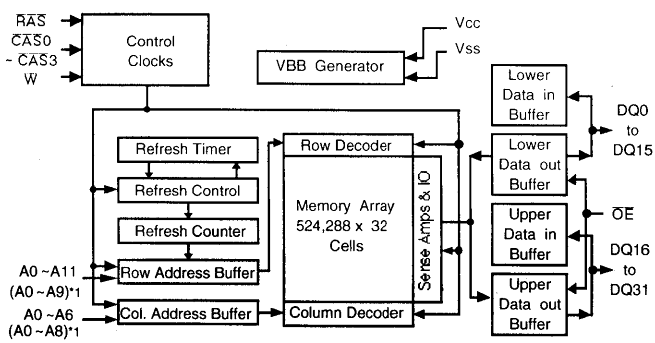
Part NO.	Refresh cycle	Refresh time	
		Normal	L-ver
V504	4K	64ms	128ms
V524	1K	16ms	

- Performance range:

Speed	tRAC	tCAC	tRC	tHPC
-7	70ns	20ns	130ns	30ns
-8	80ns	20ns	150ns	35ns

- Extended Data Out mode operation (Fast Page mode with Extended Data Out)
- 4$\overline{CAS}$ Byte/Word Read/Write operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- Self-refresh capability(L-ver only)
- LVTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC Standard pinout
- Available in Plastic TSOP(II) packages
- Single +3.3V±0.3V power supply

FUNCTIONAL BLOCK DIAGRAM



Note) *1 : 1K Refresh

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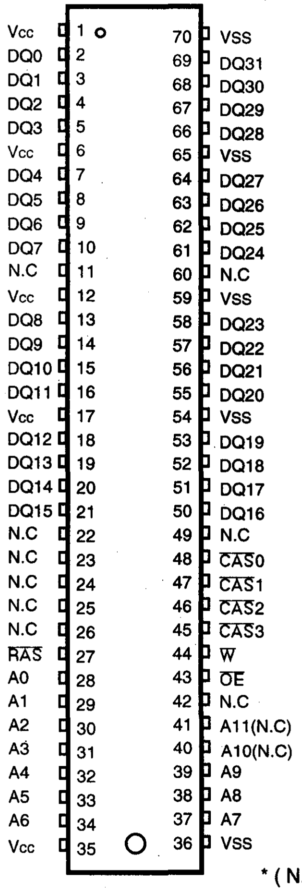
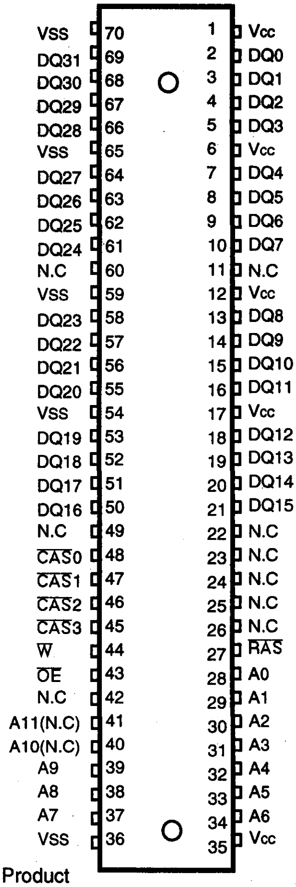
PIN CONFIGURATION (Top Views)

• **KM432V50(2)4T**



• **KM432V50(2)4R**



* (N.C) : 1K Ref. Product

Pin Name	Pin Function
A0 - A11	Address Inputs
DQ0 -31	Data In/Out
V_{SS}	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$0	1st Byte Column Address Strobe
$\overline{CAS}$1	2nd Byte Column Address Strobe
$\overline{CAS}$2	3rd Byte Column Address Strobe
$\overline{CAS}$3	4th Byte Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Outputs Enable
V_{CC}	Power(+3.3V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN},V_{OUT}	-0.5 to Vcc+0.5V	V
Voltage on V_{CC} supply relative to Vss	V_{CC}	-0.5 to +4.6	V
Storage Temperature	Tstg	-55 to +150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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RECOMMENDED OPERATING CONDITIONS (Voltages referenced to Vss, T_A= 0 to 70 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	-	Vcc+0.3*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	V

* 1 : Vcc+1.3V at pulse width ≤ 15ns (pulse width is measured at Vcc)
*2 : - 1.3V at pulse width ≤ 15ns (pulse width is measured at Vss)

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input $0 \le V_{IN} \le Vcc+0.3V$, all other pins not under test=0 volt.)	$I_{I(L)}$	- 5	5	μA
Output Leakage Current (Data out is disabled, $0V \le V_{OUT} \le Vcc$)	$I_{O(L)}$	- 5	5	μA
Output High Voltage Level(I_{OH}=-2mA)	V_{OH}	2.4	-	V
Output Low Voltage Level(I_{OL}=2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS (Continued)

Symbol	Power	Speed	Max		Units
			KM432V504	KM432V524	
I_{CC1}	Don't care	-7 -8	80 70	140 130	mA mA
I_{CC2}	Don't care	Don't care	1	1	mA
I_{CC3}	Don't care	-7 -8	80 70	140 130	mA mA
I_{CC4}	Don't care	-7 -8	80 70	90 80	mA mA
I_{CC5}	Don't care	Don't care	500	500	µA
I_{CC6}	Don't care	-7 -8	80 70	140 130	mA mA
I_{CC7}	L	Don't care	350	250	µA
I_{CCS}	L	Don't care	200	200	µA

I_{CC1}* : Operating Current ($\overline{RAS}$,$\overline{XCAS}$,Address cycling @tRC=min.)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{XCAS}$=$\overline{W}$=V_{IH})

I_{CC3}* : $\overline{RAS}$-Only Refresh Current ($\overline{XCAS}$=V_{IH}, $\overline{RAS}$,Address cycling @tRC=min.)

I_{CC4}* : Hyper Page Mode Current ($\overline{RAS}$=V_{IL}, $\overline{XCAS}$, Address cycling @tHPC=min.)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{XCAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6}* : $\overline{CAS}$-before-$\overline{RAS}$ Refresh Current ($\overline{RAS}$ and $\overline{XCAS}$ cycling @tRC=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode
Input high voltage(V_{IH})=Vcc-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{XCAS}$= 0.2V,
Din = Don't care, Extended T_{RC}= 32.3µs(4K)/125µs(1K), T_{RAS}=T_{RAS}min~200 ns

I_{CCS} : Self Refresh Current
$\overline{RAS}$=$\overline{XCAS}$=0.2V, $\overline{W}$=$\overline{OE}$=A0 ~ A11 = Vcc-0.2V or 0.2V,
DQ0 ~ DQ31= Vcc-0.2V, 0.2V or Open

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1}, I_{CC3}, and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one Hyper page mode cycle time tHPC.

CAPACITANCE(T_A=25°C, 3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A11]	C_{IN1}	-	6	pF
Input capacitance [$\overline{RAS}$, $\overline{XCAS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ0 - DQ31]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 2)
Test condition : Vcc=3.3V±0.3V, V_{ih}/V_{il} =2.2/0.8V, V_{oh}/V_{ol} =2.0/0.8V

Parameter	Symbol	-7		-8		Units	Notes
		Min	Max	Min	Max		
Random read or write cycle time	tRC	124		144		ns	
Read-modify-write cycle time	tRWC	170		190		ns	
Access time from $\overline{RAS}$	tRAC		70		80	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		20		20	ns	3,4,5
Access time from column address	tAA		35		40	ns	3,10
$\overline{CAS}$ to output in Low-Z	tCLZ	3		3		ns	3
$\overline{OE}$ to output in Low-Z	tOLZ	3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	tCEZ	3	15	3	15	ns	6,13
Transition time (rise and fall)	tT	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	tRP	50		60		ns	
$\overline{RAS}$ pulse width	tRAS	70	10K	80	10K	ns	
$\overline{RAS}$ hold time	tRSH	20		20		ns	
$\overline{CAS}$ hold time	tCSH	60		70		ns	
$\overline{CAS}$ pulse width	tCAS	15	10K	20	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	35	15	40	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		ns	
Row address set-up time	tASR	0		0		ns	
Row address hold time	tRAH	10		10		ns	
Column address set-up time	tASC	0		0		ns	14
Column address hold time	tCAH	15		15		ns	14
Column address to $\overline{RAS}$ lead time	tRAL	35		40		ns	
Read command set-up time	tRCS	0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		ns	8
Write command set-up time	tWCS	0		0		ns	7
Write command hold time	tWCH	15		15		ns	
Write command pulse width	tWP	15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	20		20		ns	

2

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-7		-8		Units	Notes
		Min	Max	Min	Max		
Write command to $\overline{CAS}$ lead time	tCWL	15		20		ns	17
Data set-up time	tDS	0		0		ns	9
Data hold time	tDH	15		15		ns	9
Refresh period(1K, Normal)	tREF		16		16	ms	
Refresh period(4K, Normal)	tREF		64		64	ms	
Refresh period(L -ver)	tREF		128		128	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	44		44		ns	7,16
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	94		104		ns	7
Column address to $\overline{W}$ delay time	tAWD	59		64		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	64		69		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	5		5		ns	18
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		ns	19
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		ns	
$\overline{CAS}$ precharge time($\overline{CBR}$ counter test cycle)	tCPT	25		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		40		45	ns	3
Hyper Page mode cycle time	tHPC	30		35		ns	11
Hyper Page mode read-modify-write cycle time	tHPRWC	71		81		ns	11
$\overline{CAS}$ precharge time Hyper page cycle)	tCP	10		10		ns	15
$\overline{RAS}$ pulse width (Hyper page cycle)	tRASP	70	200K	80	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	40		45		ns	
$\overline{OE}$ access time	tOEA		20		20	ns	3
$\overline{OE}$ to data delay	tOED	20		20		ns	
Out put buffer turn off delay time from $\overline{OE}$	tOEZ	3	20	3	20	ns	6
$\overline{OE}$ command hold time	tOEH	20		20		ns	
Output data hold time	tDOH	5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	tREZ	3	20	3	20	ns	6,13
Output buffer turn off delay from $\overline{W}$	tWEZ	3	20	3	20	ns	6
$\overline{W}$ to data delay	tWED	20		20		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	tOCH	5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	tCHO	5		5		ns	
$\overline{OE}$ precharge time	tOEP	5		5		ns	
$\overline{W}$ pulse width	tWPE	5		5		ns	
$\overline{RAS}$ pulse width($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		us	12
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	130		150		ns	12
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		ns	12

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 2ns for all inputs.
3. Measured with a load equivalent to 1 TTL loads and 50pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS≥ tWCS(min), the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥ tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.

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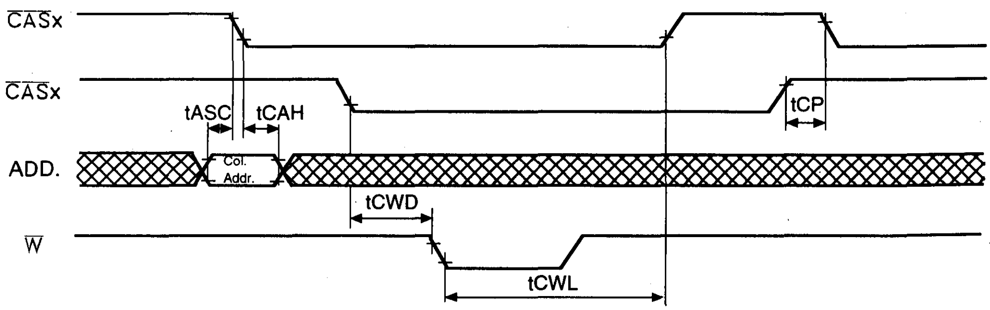
KM432V50(2)4 Truth Table

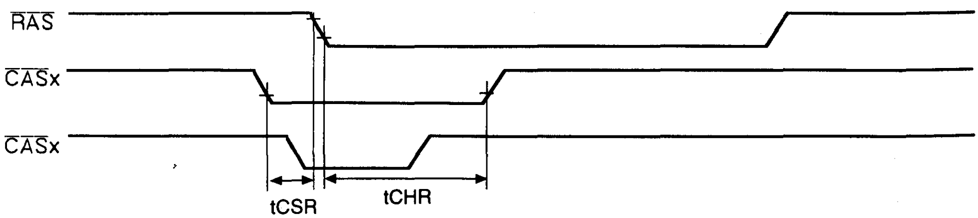
$\overline{RAS}$	$\overline{CAS1}$	$\overline{CAS2}$	$\overline{CAS3}$	$\overline{CAS4}$	$\overline{W}$	$\overline{OE}$	DQ0 -DQ7	DQ8 - DQ15	DQ16 - DQ23	DQ24 - DQ31	STATE
H	X	X	X	X	X	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Standby
L	H	H	H	H	X	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Refresh
L	L	H	H	H	H	L	DQ-OUT	Hi-Z	Hi-Z	Hi-Z	Byte Read
L	H	L	H	H	H	L	Hi-Z	DQ-OUT	Hi-Z	Hi-Z	Byte Read
L	H	H	L	H	H	L	Hi-Z	Hi-Z	DQ-OUT	Hi-Z	Byte Read
L	H	H	H	L	H	L	Hi-Z	Hi-Z	Hi-Z	DQ-OUT	Byte Read
L	L	L	L	L	H	L	DQ-OUT	DQ-OUT	DQ-OUT	DQ-OUT	2Word Read
L	L	H	H	H	L	H	DQ-IN	-	-	-	Byte Write
L	H	L	H	H	L	H	-	DQ-IN	-	-	Byte Write
L	H	H	L	H	L	H	-	-	DQ-IN	-	Byte Write
L	H	H	H	L	L	H	-	-	-	DQ-IN	Byte Write
L	L	L	L	L	L	H	DQ-IN	DQ-IN	DQ-IN	DQ-IN	2Word Write
L	L	L	L	L	H	H	Hi-Z	Hi-Z	Hi-Z	Hi-Z	-

SAMSUNG ELECTRONICS

11. tASC≥ 7.0ns, Assume tT = 2.0 ns
12. 4096 cycle(1024 cycle) of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification(L-version).
13. If $\overline{RAS}$ goes to high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes to high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going.
14. tASC, tCAH are referenced to the earlier $\overline{CAS}$ falling edge.
15. tCP is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.
16. tCWD is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.
17. tCWL is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.



18. tCSR is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.
19. tCHR is referenced to the later $\overline{CAS}$ rising high after $\overline{RAS}$ transition low.



64M DRAM

- KM48V8000
  KM48V8100
- KM44V16000
  KM44V16100
- KM48V8000A
  KM48V8100A
- KM44V16000A
  KM44V16100A

8M x 8 Bit CMOS Dynamic RAM with Fast Page Mode

DESCRIPTION

This is a family of 8,388,608 x 8 bit Fast Page Mode CMOS DRAMs. Fast Page Mode offers high speed random access of memory cells within the same row. Refresh cycle(4K Ref. or 8K Ref.), access time(-5, -6, or -7) are optional features of this family.
All of this family have $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$-only refresh and Hidden refresh capabilities.
This 8Mx8 Fast Page mode DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability.

FEATURES

- Part Identification
  - KM48V8000 (3.3V, 8K Ref.)
  - KM48V8100 (3.3V, 4K Ref.)

- Active Power Dissipation

Unit : mW

Speed	8K	4K
-5	432	612
-6	396	576
-7	360	540

- Refresh cycles

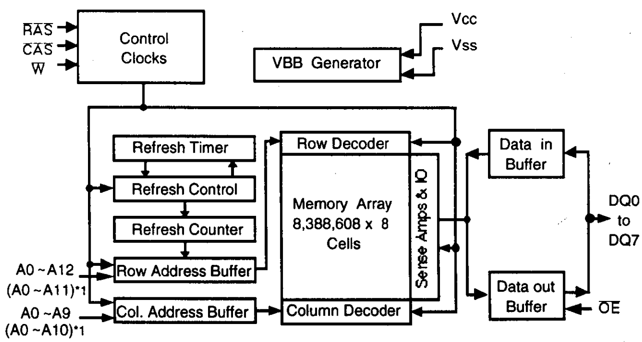
Part NO.	Refresh cycle	Refresh period
V8000	8K	128ms
V8100	4K	64ms

- Performance range:

Speed	tRAC	tCAC	tRC	tPC
-5	50ns	13ns	90ns	35ns
-6	60ns	15ns	110ns	40ns
-7	70ns	20ns	130ns	45ns

- Fast Page Mode operation
- $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh capability
- $\overline{\text{RAS}}$-only and Hidden refresh capability
- Fast parallel test mode capability
- LVTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC Standard pinout
- Available in Plastic SOJ package
- +3.3V$\pm$0.3V power supply

FUNCTIONAL BLOCK DIAGRAM

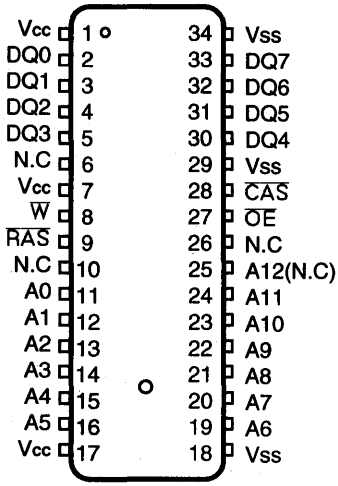


Note) *1 : 4K Refresh

SAMSUNG ELECTRONIC CO. , LTD. reserves the right to change products and specifications without notice.

PIN CONFIGURATION (Top Views)

• **KM48V80(1)00J**



* ( ) : N.C for 4K Refresh product

Pin Name	Pin Function
A0 - A12	Address Inputs(8K Product)
A0 - A11	Address Inputs(4K Product)
DQ0 -7	Data In/Out
Vss	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Outputs Enable
Vcc	Power(+3.3V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-0.5 to +4.6	V
Voltage on Vcc supply relative to Vss	V_{CC}	-0.5 to +4.6	V
Storage Temperature	Tstg	-55 to +150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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RECOMMENDED OPERATING CONDITIONS (Voltages referenced to Vss, T_A= 0 to 70 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	Vcc+0.3 *1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	V

*1 : Vcc+1.3V at pulse width ≤ 15ns (pulse width is measured at Vcc)
*2 : -1.3V at pulse width ≤ 15ns (pulse is measured at Vss)

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.3V, all other pins not under test=0 volt.)	$I_{I(L)}$	- 5	5	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	- 5	5	μA
Output High Voltage Level(I_{OH}=-2mA)	V_{OH}	2.4	-	V
Output Low Voltage Level(I_{OL}=2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Symbol	Speed	Max		Units
		KM48V8000	KM48V8100	
I_{CC1}	-5 -6 -7	120 110 100	170 160 150	mA mA mA
I_{CC2}	Don't care	1	1	mA
I_{CC3}	-5 -6 -7	120 110 100	170 160 150	mA mA mA
I_{CC4}	-5 -6 -7	90 80 70	100 90 80	mA mA mA
I_{CC5}	Don't care	500	500	μA
I_{CC6}	-5 -6 -7	120 110 100	170 160 150	mA mA mA

I_{CC1}* : Operating Current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}* : $\overline{RAS}$-only Refresh Current ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @tRC=min.)

I_{CC4}* : Fast Page Mode Current ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address cycling @tPC=min.)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)

I_{CC6}* : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1}, I_{CC3}, and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one fast page mode cycle time tPC.

CAPACITANCE(T_A=25°C,Vcc= 3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A12]	C_{IN1}	-	10	pF
Input capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	10	pF
Output Capacitance [DQ0 - DQ7]	C_{DQ}	-	15	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 2)
Test condition : Vcc=3.3V±0.3V, V_{ih}/V_{il}=2.0/0.8V, V_{oh}/V_{ol}=2.0/0.8V

Parameter	Symbol	-5		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		130		ns	
Read-modify-write cycle time	tRWC	133		155		185		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		13		15		20	ns	3,4,5
Access time from column address	tAA		25		30		35	ns	3,10
$\overline{CAS}$ to output in Low-Z	tCLZ	0		0		0		ns	3
Output buffer turn-off delay	tOFF	0	13	0	15	0	20	ns	6
Transition time (rise and fall)	tT	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		ns	
$\overline{RAS}$ pulse width	tRAS	50	10K	60	10K	70	10K	ns	
$\overline{RAS}$ hold time	tRSH	13		15		20		ns	
$\overline{CAS}$ hold time	tCSH	50		60		70		ns	
$\overline{CAS}$ pulse width	tCAS	13	10K	15	10K	20	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	37	20	45	20	50	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	
Column address hold time	tCAH	10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	tAR	40		50		55		ns	
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		ns	
Write command hold time	tWCH	10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	tWCR	40		50		55		ns	
Write command pulse width	tWP	10		10		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		15		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	13		15		20		ns	

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 2)

Parameter	Symbol	-5		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		ns	9
Data hold time	tDH	10		15		15		ns	9
Data hold time referenced to $\overline{RAS}$	tDHR	40		50		55		ns	
Refresh period(4K)	tREF		64		64		64	ms	
Refresh period(8K)	tREF		128		128		128	ms	
Write command set-up time	tWCS	0		0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	36		40		50		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	73		85		100		ns	7
Column address to $\overline{W}$ delay time	tAWD	48		55		65		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	53		60		70		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		ns	
$\overline{CAS}$ precharge time($\overline{CBR}$ counter test cycle)	tCPT	20		20		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		30		35		40	ns	3
Fast Page mode cycle time	tPC	35		40		45		ns	
Fast Page mode read-modify-write cycle time	tPRWC	76		85		100		ns	
$\overline{CAS}$ precharge time (Fast page cycle)	tCP	10		10		10		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	50	200K	60	200K	70	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		ns	
$\overline{OE}$ access time	tOEA		13		15		20	ns	
$\overline{OE}$ to data delay	tOED	13		15		20		ns	
Out put buffer turn off delay time from $\overline{OE}$	tOEZ	0	13	0	15	0	20	ns	13
$\overline{OE}$ command hold time	tOEH	13		15		20		ns	
Write command set-up time(Test mode in)	tWTS	10		10		10		ns	11
Write command hold time(Test mode in)	tWTH	10		10		10		ns	11
$\overline{W}$ to $\overline{RAS}$ precharge time($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		ns	

TEST MODE CYCLE

(Note. 12)

Parameter	Symbol	-5		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	95		115		135		ns	
Read-modify-write cycle time	tRWC	138		160		190		ns	
Access time from $\overline{RAS}$	tRAC		55		65		75	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		18		20		25	ns	3,4,5
Access time from column address	tAA		30		35		40	ns	3,10
$\overline{RAS}$ pulse width	tRAS	55	10K	65	10K	75	10K	ns	
$\overline{CAS}$ pulse width	tCAS	18	10K	20	10K	25	10K	ns	
$\overline{RAS}$ hold time	tRSH	18		20		25		ns	
$\overline{CAS}$ hold time	tCSH	55		65		75		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	41		45		55		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	78		90		105		ns	7
Column address to $\overline{W}$ delay time	tAWD	53		60		70		ns	7
Fast Page mode cycle time	tPC	40		45		50		ns	
Fast page mode read-modify-write cycle time	tPRWC	81		90		105		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	55	200K	65	200K	75	200K	ns	
Access time form $\overline{CAS}$ precharge	tCPA		35		40		45	ns	3
$\overline{OE}$ access time	tOEA		18		20		25	ns	
$\overline{OE}$ to data delay	tOED	18		20		25		ns	
$\overline{OE}$ command hold time	tOEH	18		20		25		ns	

2

NOTES

1. An initial pause of 200µs is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 1 TTL loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If tWCS≥tWCS(min), the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
11. These specifications are applied in the test mode.
12. In test mode read cycle, the value of tRAC, tAA, tCAC is delayed by 2ns to 5ns for the specified values. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
13. tOFF(max) and tOEZ(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.

16M x 4 Bit CMOS Dynamic RAM with Fast Page Mode

DESCRIPTION

This is a family of 16,777,216 x 4 bit Fast Page Mode CMOS DRAMs. Fast Page Mode offers high speed random access of memory cells within the same row. Refresh cycle(4K Ref. or 8K Ref.), access time(-5, -6, or -7) are optional features of this family.
All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities.
This 16Mx4 Fast Page mode DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability.

FEATURES

- Part Identification
  - KM44V16000 (3.3V, 8K Ref.)
  - KM44V16100 (3.3V, 4K Ref.)

- Active Power Dissipation

Unit : mW

Speed	8K	4K
-5	432	612
-6	396	576
-7	360	540

- Refresh cycles

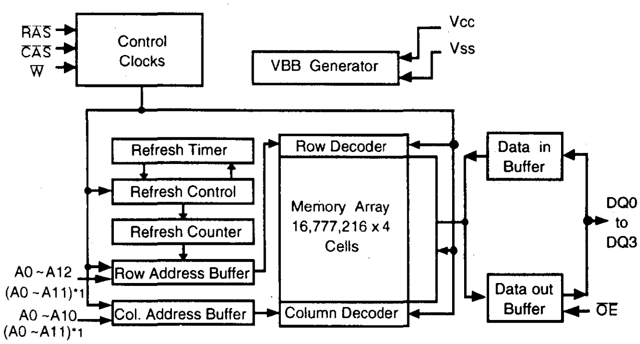
Part NO.	Refresh cycle	Refresh period
V16000	8K	128ms
V16100	4K	64ms

- Performance range:

Speed	tRAC	tCAC	tRC	tPC
-5	50ns	13ns	90ns	35ns
-6	60ns	15ns	110ns	40ns
-7	70ns	20ns	130ns	45ns

- Fast Page Mode operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- Fast parallel test mode capability
- LVTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC Standard pinout
- Available in Plastic SOJ package
- +3.3V±0.3V power supply

FUNCTIONAL BLOCK DIAGRAM



Note) *1 : 4K Refresh

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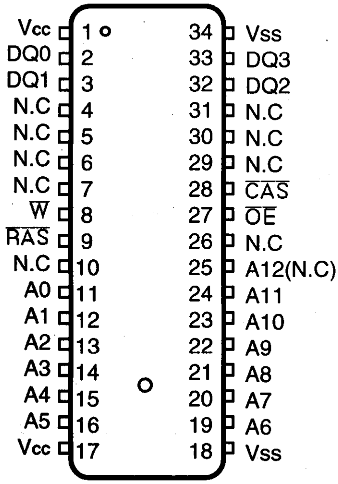
PIN CONFIGURATION (Top Views)

• KM44V160(1)00J



* ( ) : N.C for 4K Refresh product

Pin Name	Pin Function
A0 - A12	Address Inputs(8K Product)
A0 - A11	Address Inputs(4K Product)
DQ0 -3	Data In/Out
Vss	Ground
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{W}}$	Read/Write Input
$\overline{\text{OE}}$	Data Outputs Enable
Vcc	Power(+3.3V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to +4.6	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.5 to +4.6	V
Storage Temperature	Tstg	-55 to +150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to Vss, T_A= 0 to 70 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	Vcc+0.3*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	V

*1 : Vcc+1.3V at pulse width ≤ 15ns (pulse width is measured at Vcc)
*2 : -1.3V at pulse width ≤ 15ns (pulse is measured at Vss)

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.3V, all other pins not under test=0 volt.)	$I_{I(L)}$	- 5	5	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	- 5	5	μA
Output High Voltage Level(I_{OH}=-2mA)	V_{OH}	2.4	-	V
Output Low Voltage Level(I_{OL}=2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Symbol	Speed	Max		Units
		KM44V16000	KM44V16100	
I_{CC1}	-5 -6 -7	120 110 100	170 160 150	mA mA mA
I_{CC2}	Don't care	1	1	mA
I_{CC3}	-5 -6 -7	120 110 100	170 160 150	mA mA mA
I_{CC4}	-5 -6 -7	90 80 70	100 90 80	mA mA mA
I_{CC5}	Don't care	500	500	µA
I_{CC6}	-5 -6 -7	120 110 100	170 160 150	mA mA mA

I_{CC1}* : Operating Current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}* : $\overline{RAS}$-only Refresh Current ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @tRC=min.)

I_{CC4}* : Fast Page Mode Current ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address cycling @tPC=min.)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)

I_{CC6}* : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1}, I_{CC3}, and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one fast page mode cycle time tPC.

CAPACITANCE(T_A=25°C,Vcc= 3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A12]	C_{IN1}	-	10	pF
Input capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	10	pF
Output Capacitance [DQ0 - DQ3]	C_{DQ}	-	15	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 2)
Test condition : Vcc=3.3V±0.3V, V_{ih}/V_{il}=2.0/0.8V, V_{oh}/V_{ol}=2.0/0.8V

Parameter	Symbol	-5		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		130		ns	
Read-modify-write cycle time	tRWC	133		155		185		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		13		15		20	ns	3,4,5
Access time from column address	tAA		25		30		35	ns	3,10
$\overline{CAS}$ to output in Low-Z	tCLZ	0		0		0		ns	3
Output buffer turn-off delay	tOFF	0	13	0	15	0	20	ns	6
Transition time (rise and fall)	tT	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		ns	
$\overline{RAS}$ pulse width	tRAS	50	10K	60	10K	70	10K	ns	
$\overline{RAS}$ hold time	tRSH	13		15		20		ns	
$\overline{CAS}$ hold time	tCSH	50		60		70		ns	
$\overline{CAS}$ pulse width	tCAS	13	10K	15	10K	20	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	37	20	45	20	50	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	
Column address hold time	tCAH	10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	tAR	40		50		55		ns	
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		ns	
Write command hold time	tWCH	10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	tWCR	40		50		55		ns	
Write command pulse width	tWP	10		10		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		15		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	13		15		20		ns	

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 2)

Parameter	Symbol	-5		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		ns	9
Data hold time	tDH	10		15		15		ns	9
Data hold time referenced to $\overline{RAS}$	tDHR	40		50		55		ns	
Refresh period(4K)	tREF		64		64		64	ms	
Refresh period(8K)	tREF		128		128		128	ms	
Write command set-up time	tWCS	0		0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	36		40		50		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	73		85		100		ns	7
Column address to $\overline{W}$ delay time	tAWD	48		55		65		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	53		60		70		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		ns	
$\overline{CAS}$ precharge time($\overline{CBR}$ counter test cycle)	tCPT	20		20		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		30		35		40	ns	3
Fast Page mode cycle time	tPC	35		40		45		ns	
Fast Page mode read-modify-write cycle time	tPRWC	76		85		100		ns	
$\overline{CAS}$ precharge time (Fast page cycle)	tCP	10		10		10		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	50	200K	60	200K	70	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		ns	
$\overline{OE}$ access time	tOEA		13		15		20	ns	
$\overline{OE}$ to data delay	tOED	13		15		20		ns	
Out put buffer turn off delay time from $\overline{OE}$	tOEZ	0	13	0	15	0	20	ns	13
$\overline{OE}$ command hold time	tOEH	13		15		20		ns	
Write command set-up time(Test mode in)	tWTS	10		10		10		ns	11
Write command hold time(Test mode in)	tWTH	10		10		10		ns	11
$\overline{W}$ to $\overline{RAS}$ precharge time($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		ns	

TEST MODE CYCLE

(Note. 12)

Parameter	Symbol	-5		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	95		115		135		ns	
Read-modify-write cycle time	tRWC	138		160		190		ns	
Access time from $\overline{RAS}$	tRAC		55		65		75	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		18		20		25	ns	3,4,5
Access time from column address	tAA		30		35		40	ns	3,10
$\overline{RAS}$ pulse width	tRAS	55	10K	65	10K	75	10K	ns	
$\overline{CAS}$ pulse width	tCAS	18	10K	20	10K	25	10K	ns	
$\overline{RAS}$ hold time	tRSH	18		20		25		ns	
$\overline{CAS}$ hold time	tCSH	55		65		75		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	41		45		55		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	78		90		105		ns	7
Column address to $\overline{W}$ delay time	tAWD	53		60		70		ns	7
Fast Page mode cycle time	tPC	40		45		50		ns	
Fast page mode read-modify-write cycle time	tPRWC	81		90		105		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	55	200K	65	200K	75	200K	ns	
Access time form $\overline{CAS}$ precharge	tCPA		35		40		45	ns	3
$\overline{OE}$ access time	tOEA		18		20		25	ns	
$\overline{OE}$ to data delay	tOED	18		20		25		ns	
$\overline{OE}$ command hold time	tOEH	18		20		25		ns	

2

NOTES

1. An initial pause of 200µs is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 1 TTL loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If tWCS≥tWCS(min), the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
11. These specifications are applied in the test mode.
12. In test mode read cycle, the value of tRAC, tAA, tCAC is delayed by 2ns to 5ns for the specified values. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
13. tOFF(max) and tOEZ(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.

8M x 8 Bit CMOS Dynamic RAM with Fast Page Mode

DESCRIPTION

This is a family of 8,388,608 x 8 bit Fast Page Mode CMOS DRAMs. Fast Page Mode offers high speed random access of memory cells within the same row. Refresh cycle(4K Ref. or 8K Ref.), access time(-5, -6, or -7), power consumption(Normal, Low power, or Self-refresh power) and package type(SOJ or TSOP-II) are optional features of this family.

All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities. Further more, Self-refresh operation is available in self-refresh version.

This 8Mx8 Fast Page mode DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability.

FEATURES

- Part Identification
  - KM48V8000A/A-L(3.3V, 8K Ref.)
  - KM48V8100A/A-L(3.3V, 4K Ref.)

- Active Power Dissipation

Unit : mW

Speed	8K	4K
-5	396	540
-6	288	504
-7	252	468

- Refresh cycles

Part NO.	Refresh cycle	Refresh	
		Normal	L
V8000*	8K	64ms	256ms
V8100	4K		

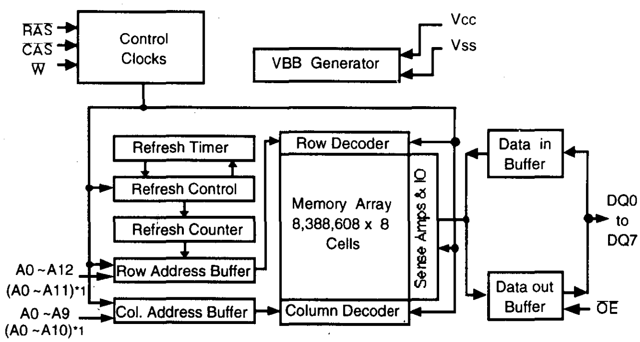
* Access mode & $\overline{RAS}$ only refresh mode
: 8K cycle/64ms
$\overline{CAS}$-before-$\overline{RAS}$ & Hidden refresh mode
: 4K cycle/64ms

- Performance range:

Speed	tRAC	tCAC	tRC	tPC
-5	50ns	13ns	90ns	35ns
-6	60ns	15ns	110ns	40ns
-7	70ns	20ns	130ns	45ns

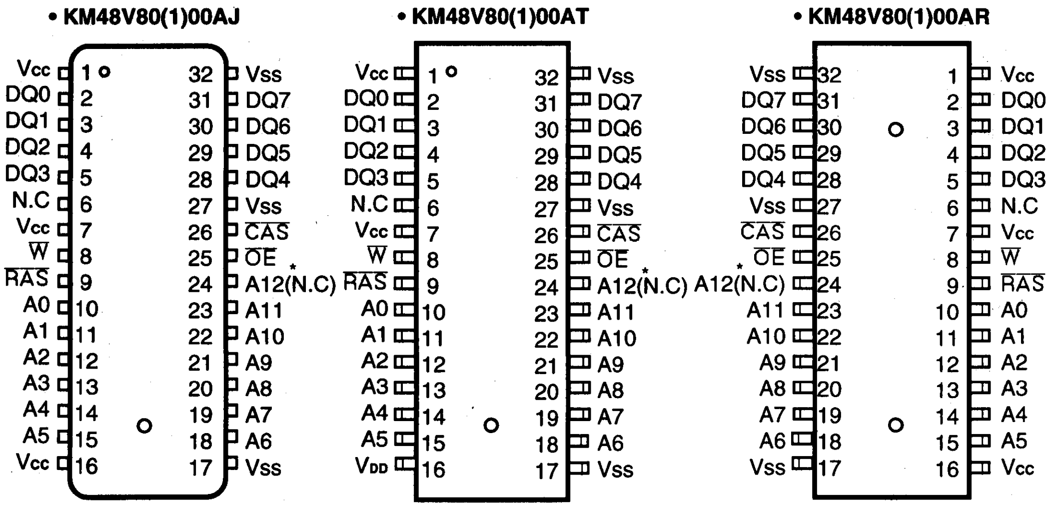
- Fast Page Mode operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$ only and Hidden refresh capability
- Self-refresh capability(L-ver only)
- Fast parallel test mode capability
- LVTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC Standard pinout
- Available in Plastic SOJ and TSOP(II) packages
- +3.3V±0.3V power supply

FUNCTIONAL BLOCK DIAGRAM



Note) *1 : 4K Refresh

PIN CONFIGURATION (Top Views)



* (N.C) : N.C for 4K Refresh product

Pin Name	Pin Function
A0 - A12	Address Inputs(8K Product)
A0 - A11	Address Inputs(4K Product)
DQ0 -7	Data In/Out
V_{SS}	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Outputs Enable
Vcc	Power(+3.3V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-0.5 to +4.6	V
Voltage on Vcc supply relative to Vss	V_{CC}	-0.5 to +4.6	V
Storage Temperature	Tstg	-55 to +150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to Vss, T_A= 0 to 70 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	Vcc+0.3*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	V

*1 : Vcc+1.3V at pulse width ≤ 15ns (pulse width is measured at Vcc)
*2 : -1.3V at pulse width ≤ 15ns (pulse is measured at Vss)

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input $0 \le V_{IN} \le Vcc+0.3V$, all other pins not under test=0 volt.)	$I_{I(L)}$	- 5	5	μA
Output Leakage Current (Data out is disabled, $0V \le V_{OUT} \le Vcc$)	$I_{O(L)}$	- 5	5	μA
Output High Voltage Level(I_{OH}=-2mA)	V_{OH}	2.4	-	V
Output Low Voltage Level(I_{OL}=2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS (Continued.)

Symbol	Power	Speed	Max		Units
			KM48V8000	KM48V8100	
I_{CC1}	Don't care	-5 -6 -7	110 100 90	150 140 130	mA mA mA
I_{CC2}	Normal L	Don't care	1 1	1 1	mA mA
I_{CC3}	Don't care	-5 -6 -7	110 100 90	150 140 130	mA mA mA
I_{CC4}	Don't care	-5 -6 -7	80 70 60	95 85 75	mA mA mA
I_{CC5}	Normal L	Don't care	500 500	500 500	µA µA
I_{CC6}	Don't care	-5 -6 -7	150 140 130	150 140 130	mA mA mA
I_{CC7}	L	Don't care	450	450	µA
I_{CCS}	L	Don't care	450	450	µA

I_{CC1}* : Operating Current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}* : $\overline{RAS}$-only Refresh Current ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @tRC=min.)

I_{CC4}* : Fast Page Mode Current ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address cycling @tPC=min.)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6}* : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode
Input high voltage(V_{IH})=Vcc-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{CAS}$=$\overline{CAS}$-before-$\overline{RAS}$ cycling or 0.2V
$\overline{W}$, $\overline{OE}$ = VIH, Address = Don't care, DQ=Open, T_{RC}= 62.5µs
T_{RAS}=T_{RAS}min~300 ns

I_{CCS} : Self Refresh Current
$\overline{RAS}$=$\overline{CAS}$=0.2V, $\overline{W}$=$\overline{OE}$=A0 ~ A12(A11) = Vcc-0.2V or 0.2V, DQ0 ~ DQ7= Vcc-0.2V, 0.2V or Open

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1}, I_{CC3}, and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one fast page mode cycle time tPC.

CAPACITANCE(T_A=25°C,Vcc= 3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A12]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ0 - DQ7]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 2)
Test condition : Vcc=3.3V±0.3V, V_{ih}/V_{il}=2.0/0.8V, V_{oh}/V_{ol}=2.0/0.8V

2

Parameter	Symbol	-5		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		130		ns	
Read-modify-write cycle time	tRWC	133		155		185		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		13		15		20	ns	3,4,5
Access time from column address	tAA		25		30		35	ns	3,10
$\overline{CAS}$ to output in Low-Z	tCLZ	0		0		0		ns	3
Output buffer turn-off delay	tOFF	0	13	0	15	0	20	ns	6,13
Transition time (rise and fall)	tT	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		ns	
$\overline{RAS}$ pulse width	tRAS	50	10K	60	10K	70	10K	ns	
$\overline{RAS}$ hold time	tRSH	13		15		20		ns	
$\overline{CAS}$ hold time	tCSH	50		60		70		ns	
$\overline{CAS}$ pulse width	tCAS	13	10K	15	10K	20	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	37	20	45	20	50	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	
Column address hold time	tCAH	10		10		15		ns	
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		ns	
Write command hold time	tWCH	10		10		15		ns	
Write command pulse width	tWP	10		10		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		15		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	13		15		20		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		ns	9
Data hold time	tDH	10		10		15		ns	9
Refresh period(4K, Normal)	tREF		64		64		64	ms	
Refresh period(8K, Normal)	tREF		64		64		64	ms	
Refresh period(L -ver)	tREF		256		256		256	ms	
Write command set-up time	tWCS	0		0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	36		40		50		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	73		85		100		ns	7
Column address to $\overline{W}$ delay time	tAWD	48		55		65		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	53		60		70		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		ns	
$\overline{CAS}$ precharge time($\overline{CBR}$ counter test cycle)	tCPT	20		20		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		30		35		40	ns	3
Fast Page mode cycle time	tPC	35		40		45		ns	
Fast Page mode read-modify-write cycle time	tPRWC	76		85		100		ns	
$\overline{CAS}$ precharge time (Fast page cycle)	tCP	10		10		10		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	50	200K	60	200K	70	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		ns	
$\overline{OE}$ access time	tOEA		13		15		20	ns	
$\overline{OE}$ to data delay	tOED	13		15		20		ns	
Output buffer turn off delay time from $\overline{OE}$	tOEZ	0	13	0	15	0	20	ns	13
$\overline{OE}$ command hold time	tOEH	13		15		20		ns	
Write command set-up time(Test mode in)	tWTS	10		10		10		ns	11
Write command hold time(Test mode in)	tWTH	15		15		15		ns	11
$\overline{W}$ to $\overline{RAS}$ precharge time($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		ns	
$\overline{RAS}$ pulse width($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		us	14
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	90		110		130		ns	14
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		ns	14

TEST MODE CYCLE

(Note. 11)

Parameter	Symbol	-5		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	95		115		135		ns	
Read-modify-write cycle time	tRWC	138		160		190		ns	
Access time from $\overline{RAS}$	tRAC		55		65		75	ns	3,4,10,12
Access time from $\overline{CAS}$	tCAC		18		20		25	ns	3,4,5,12
Access time from column address	tAA		30		35		40	ns	3,10,12
$\overline{RAS}$ pulse width	tRAS	55	10K	65	10K	75	10K	ns	
$\overline{CAS}$ pulse width	tCAS	18	10K	20	10K	25	10K	ns	
$\overline{RAS}$ hold time	tRSH	18		20		25		ns	
$\overline{CAS}$ hold time	tCSH	55		65		75		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	41		45		55		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	78		90		105		ns	7
Column address to $\overline{W}$ delay time	tAWD	53		60		70		ns	7
Fast Page mode cycle time	tPC	40		45		50		ns	
Fast page mode read-modify-write cycle time	tPRWC	81		90		105		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	55	200K	65	200K	75	200K	ns	
Access time form $\overline{CAS}$ precharge	tCPA		35		40		45	ns	3
$\overline{OE}$ access time	tOEA		18		20		25	ns	
$\overline{OE}$ to data delay	tOED	18		20		25		ns	
$\overline{OE}$ command hold time	tOEH	18		20		25		ns	

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NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 100pF and Voh = 2.0V(Iout= -2mA), Vol =0.8V(Iout = 2mA)
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If tWCS ≥ tWCS (min), the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read- modify -write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
11. These specifications are applied in the test mode.
12. In test mode read cycle, the value of tRAC, tAA, tCAC, tOEA, and tCPA is delayed by 2ns to 5ns for the specified values. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
13. tOFF(max) and tOEZ(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
14. 8192(8K Ref.)/4096(4K Ref.) cycles of burst refresh must be executed within 64ms before and after self refresh, in order to meet refresh specification.

16M x 4 Bit CMOS Dynamic RAM with Fast Page Mode

DESCRIPTION

This is a family of 16,777,216 x 4 bit Fast Page Mode CMOS DRAMs. Fast Page Mode offers high speed random access of memory cells within the same row. Refresh cycle(4K Ref. or 8K Ref.), access time(-5, -6, or -7), power consumption(Normal, Low power, or Self-refresh power) and package type(SOJ or TSOP-II) are optional features of this family.

All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities. Further more, Self-refresh operation is available in self-refresh version.

This 16Mx4 Fast Page mode DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability.

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FEATURES

- Part Identification
  - KM44V16000A/A-L(3.3V, 8K Ref.)
  - KM44V16100A/A-L(3.3V, 4K Ref.)

- Active Power Dissipation

Unit : mW

Speed	8K	4K
-5	396	540
-6	288	504
-7	252	468

- Refresh cycles

Part NO.	Refresh cycle	Refresh period	
		Normal	L
V16000*	8K	64ms	256ms
V16100	4K		

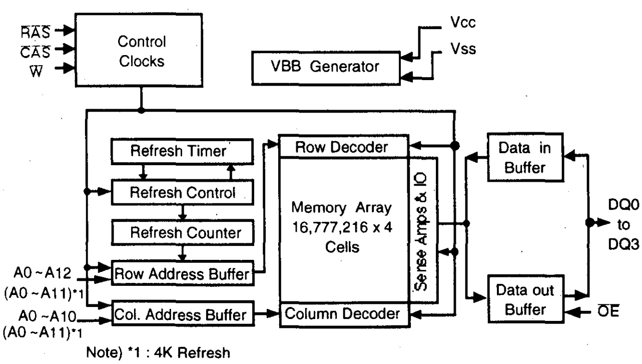
* Access mode & $\overline{RAS}$ only refresh mode
: 8K cycle/64ms
$\overline{CAS}$-before-$\overline{RAS}$ & Hidden refresh mode
: 4K cycle/64ms

- Performance range:

Speed	tRAC	tCAC	tRC	tPC
-5	50ns	13ns	90ns	35ns
-6	60ns	15ns	110ns	40ns
-7	70ns	20ns	130ns	45ns

- Fast Page Mode operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$ only and Hidden refresh capability
- Self-refresh capability(L-ver only)
- Fast parallel test mode capability
- LVTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC Standard pinout
- Available in Plastic SOJ and TSOP(II) packages
- +3.3V±0.3V power supply

FUNCTIONAL BLOCK DIAGRAM



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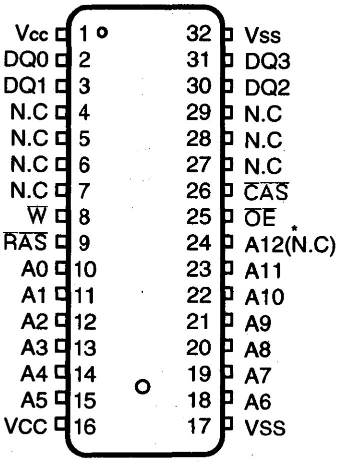
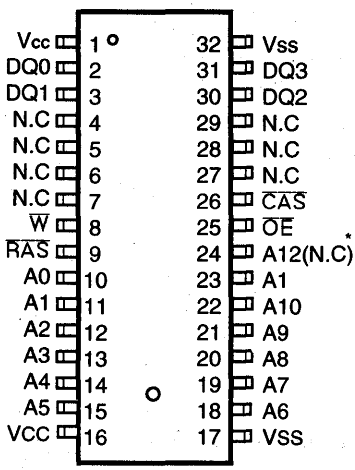
PIN CONFIGURATION (Top Views)

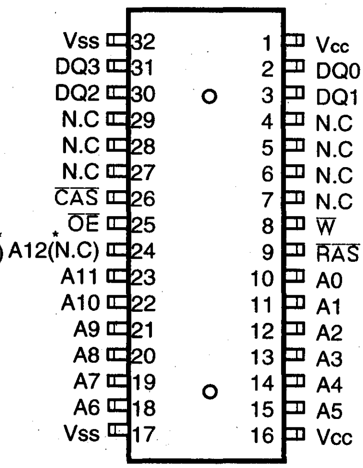
• KM44V160(1)00AJ



• KM44V160(1)00AT



• KM44V160(1)00AR



* (N.C) : N.C for 4K Refresh product

Pin Name	Pin Function
A0 - A12	Address Inputs(8K Product)
A0 - A11	Address Inputs(4K Product)
DQ0 -3	Data In/Out
Vss	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Outputs Enable
Vcc	Power(+3.3V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-0.5 to +4.6	V
Voltage on Vcc supply relative to Vss	V_{CC}	-0.5 to +4.6	V
Storage Temperature	Tstg	-55 to +150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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RECOMMENDED OPERATING CONDITIONS (Voltages referenced to Vss, T_A= 0 to 70 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	Vcc+0.3*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	V

*1 : Vcc+1.3V at pulse width ≤ 15ns (pulse width is measured at Vcc)
*2 : -1.3V at pulse width ≤ 15ns (pulse is measured at Vss)

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input $0 \le V_{IN} \le Vcc+0.3V$, all other pins not under test=0 volt.)	$I_{I(L)}$	- 5	5	μA
Output Leakage Current (Data out is disabled, $0V \le V_{OUT} \le Vcc$)	$I_{O(L)}$	- 5	5	μA
Output High Voltage Level(I_{OH}=-2mA)	V_{OH}	2.4	-	V
Output Low Voltage Level(I_{OL}=2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS (Continued.)

Symbol	Power	Speed	Max		Units
			KM44V16000	KM44V16100	
I_{CC1}	Don't care	-5 -6 -7	110 100 90	150 140 130	mA mA mA
I_{CC2}	Normal L	Don't care	1 1	1 1	mA mA
I_{CC3}	Don't care	-5 -6 -7	110 100 90	150 140 130	mA mA mA
I_{CC4}	Don't care	-5 -6 -7	80 70 60	95 85 75	mA mA mA
I_{CC5}	Normal L	Don't care	500 500	500 500	µA µA
I_{CC6}	Don't care	-5 -6 -7	150 140 130	150 140 130	mA mA mA
I_{CC7}	L	Don't care	450	450	µA
I_{CCS}	L	Don't care	450	450	µA

I_{CC1}* : Operating Current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}* : $\overline{RAS}$-only Refresh Current ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @tRC=min.)

I_{CC4}* : Fast Page Mode Current ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address cycling @tPC=min.)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6}* : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode
Input high voltage(V_{IH})=Vcc-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{CAS}$=$\overline{CAS}$-before-$\overline{RAS}$ cycling or 0.2V
$\overline{W}$, $\overline{OE}$ = VIH, Address = Don't care, DQ = Open, T_{RC}= 62.5µs
T_{RAS}=T_{RAS}min~300 ns

I_{CCS} : Self Refresh Current
$\overline{RAS}$=$\overline{CAS}$=0.2V, $\overline{W}$=$\overline{OE}$=A0 ~ A12(A11) = Vcc-0.2V or 0.2V, DQ0 ~ DQ3= Vcc-0.2V, 0.2V or Open

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1}, I_{CC3}, and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one fast page mode cycle time tPC.

CAPACITANCE(T_A=25°C,Vcc= 3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A12]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ0 - DQ3]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 2)
Test condition : Vcc=3.3V±0.3V, V_{ih}/V_{il}=2.0/0.8V, V_{oh}/V_{ol}=2.0/0.8V

Parameter	Symbol	-5		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		130		ns	
Read-modify-write cycle time	tRWC	133		155		185		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		13		15		20	ns	3,4,5
Access time from column address	tAA		25		30		35	ns	3,10
$\overline{CAS}$ to output in Low-Z	tCLZ	0		0		0		ns	3
Output buffer turn-off delay	tOFF	0	13	0	15	0	20	ns	6,13
Transition time (rise and fall)	tT	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		ns	
$\overline{RAS}$ pulse width	tRAS	50	10K	60	10K	70	10K	ns	
$\overline{RAS}$ hold time	tRSH	13		15		20		ns	
$\overline{CAS}$ hold time	tCSH	50		60		70		ns	
$\overline{CAS}$ pulse width	tCAS	13	10K	15	10K	20	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	37	20	45	20	50	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	
Column address hold time	tCAH	10		10		15		ns	
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		ns	
Write command hold time	tWCH	10		10		15		ns	
Write command pulse width	tWP	10		10		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		15		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	13		15		20		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		ns	9
Data hold time	tDH	10		10		15		ns	9
Refresh period(4K, Normal)	tREF		64		64		64	ms	
Refresh period(8K, Normal)	tREF		64		64		64	ms	
Refresh period(L-ver)	tREF		256		256		256	ms	
Write command set-up time	tWCS	0		0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	36		40		50		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	73		85		100		ns	7
Column address to $\overline{W}$ delay time	tAWD	48		55		65		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	53		60		70		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		ns	
$\overline{CAS}$ precharge time(CB$\overline{R}$ counter test cycle)	tCPT	20		20		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		30		35		40	ns	3
Fast Page mode cycle time	tPC	35		40		45		ns	
Fast Page mode read-modify-write cycle time	tPRWC	76		85		100		ns	
$\overline{CAS}$ precharge time (Fast page cycle)	tCP	10		10		10		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	50	200K	60	200K	70	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		ns	
$\overline{OE}$ access time	tOEA		13		15		20	ns	
$\overline{OE}$ to data delay	tOED	13		15		20		ns	
Out put buffer turn off delay time from $\overline{OE}$	tOEZ	0	13	0	15	0	20	ns	13
$\overline{OE}$ command hold time	tOEH	13		15		20		ns	
Write command set-up time(Test mode in)	tWTS	10		10		10		ns	11
Write command hold time(Test mode in)	tWTH	15		15		15		ns	11
$\overline{W}$ to $\overline{RAS}$ precharge time($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		ns	
$\overline{RAS}$ pulse width($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		us	14
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	90		110		130		ns	14
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		ns	14

TEST MODE CYCLE

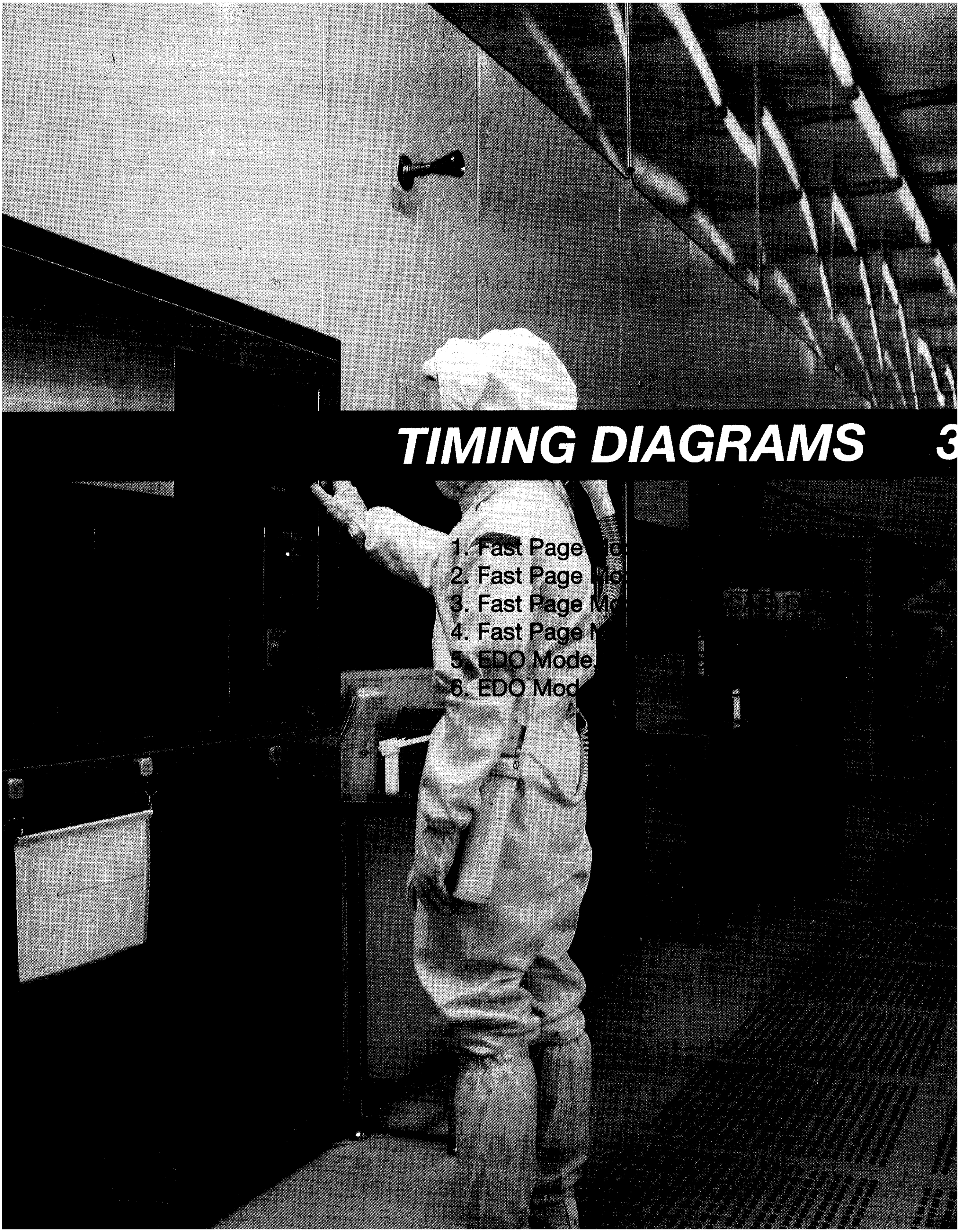
(Note. 11)

Parameter	Symbol	-5		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	95		115		135		ns	
Read-modify-write cycle time	tRWC	138		160		190		ns	
Access time from $\overline{RAS}$	tRAC		55		65		75	ns	3,4,10,12
Access time from $\overline{CAS}$	tCAC		18		20		25	ns	3,4,5,12
Access time from column address	tAA		30		35		40	ns	3,10,12
$\overline{RAS}$ pulse width	tRAS	55	10K	65	10K	75	10K	ns	
$\overline{CAS}$ pulse width	tCAS	18	10K	20	10K	25	10K	ns	
$\overline{RAS}$ hold time	tRSH	18		20		25		ns	
$\overline{CAS}$ hold time	tCSH	55		65		75		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	41		45		55		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	78		90		105		ns	7
Column address to $\overline{W}$ delay time	tAWD	53		60		70		ns	7
Fast Page mode cycle time	tPC	40		45		50		ns	
Fast page mode read-modify-write cycle time	tPRWC	81		90		105		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	tRASP	55	200K	65	200K	75	200K	ns	
Access time form $\overline{CAS}$ precharge	tCPA		35		40		45	ns	3
$\overline{OE}$ access time	tOEA		18		20		25	ns	
$\overline{OE}$ to data delay	tOED	18		20		25		ns	
$\overline{OE}$ command hold time	tOEH	18		20		25		ns	

2

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 100pF and Voh=2.0V(Iout = -2mA), Vol=0.8V(Iout = 2mA)
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a re ference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If tWCS≥tWCS(min), the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a re ference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
11. These specifications are applied in the test mode.
12. In test mode read cycle, the value of tRAC, tAA, tCAC is delayed by 2ns to 5ns for the specified values. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
13. tOFF(max) and tOEZ(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
14. 8192(8K Ref.)/4096(4K Ref.) cycles of burst refresh must be executed within 64ms before and after self refresh, in order to meet refresh specification.



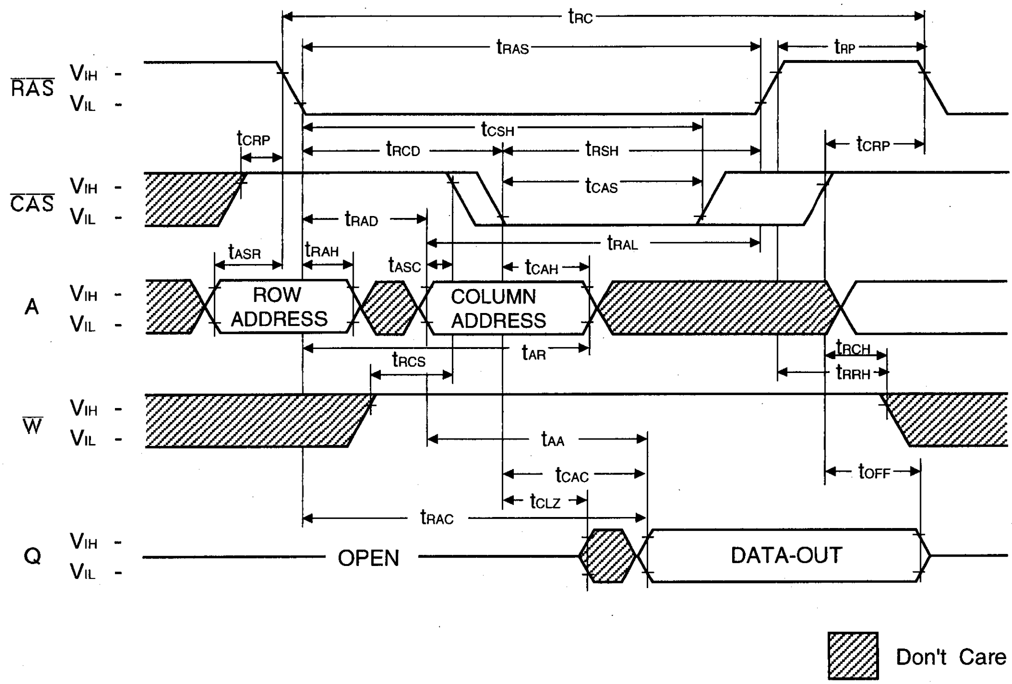
TIMING DIAGRAMS 3

1. Fast Page
2. Fast Page
3. Fast Page
4. Fast Page
5. EDO Mode
6. EDO Mod

Fast Page Mode, x1 Device

TIMING DIAGRAM

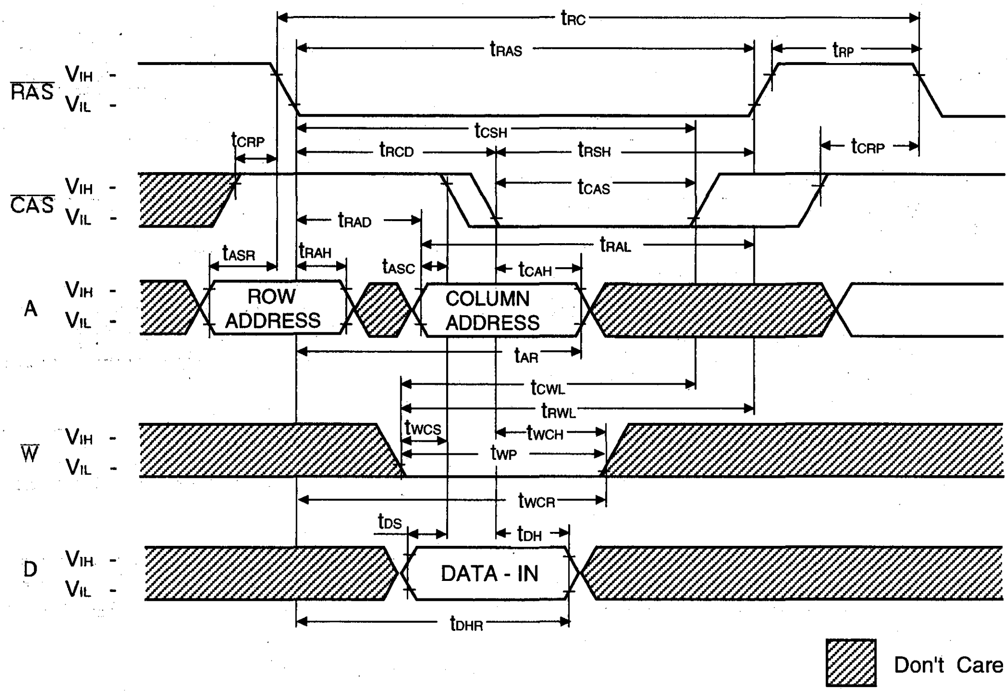
READ CYCLE



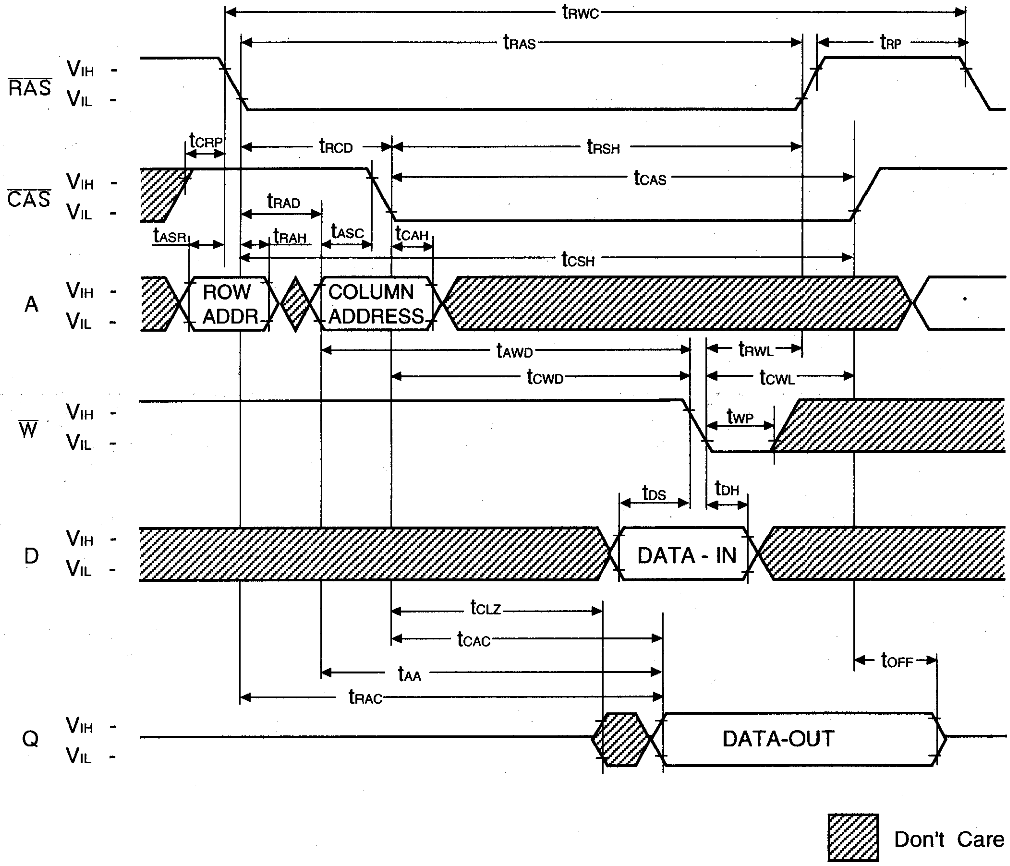
3

SAMSUNG ELECTRONICS

WRITE CYCLE (EARLY WRITE)

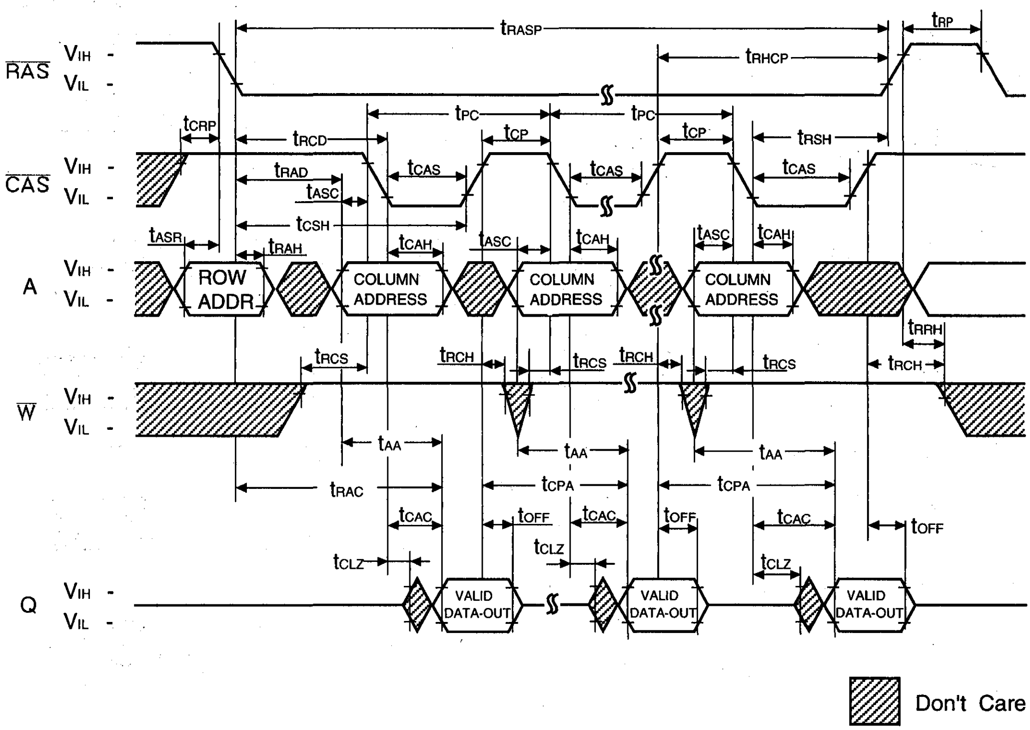


READ-WRITE / READ - MODIFY - WRITE CYCLE

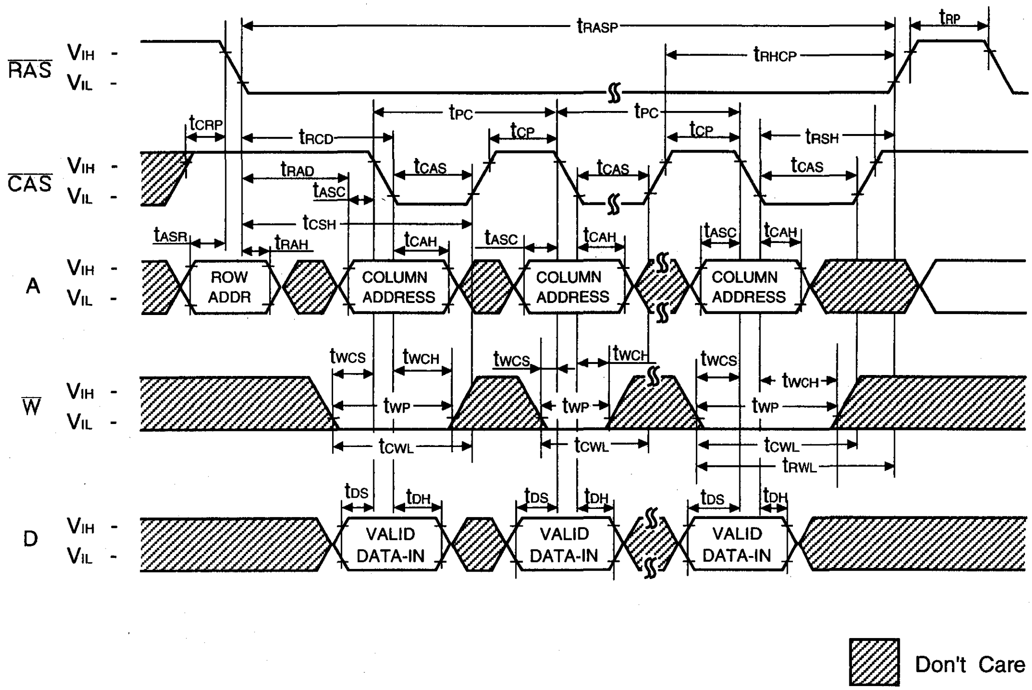


3

FAST PAGE MODE READ CYCLE

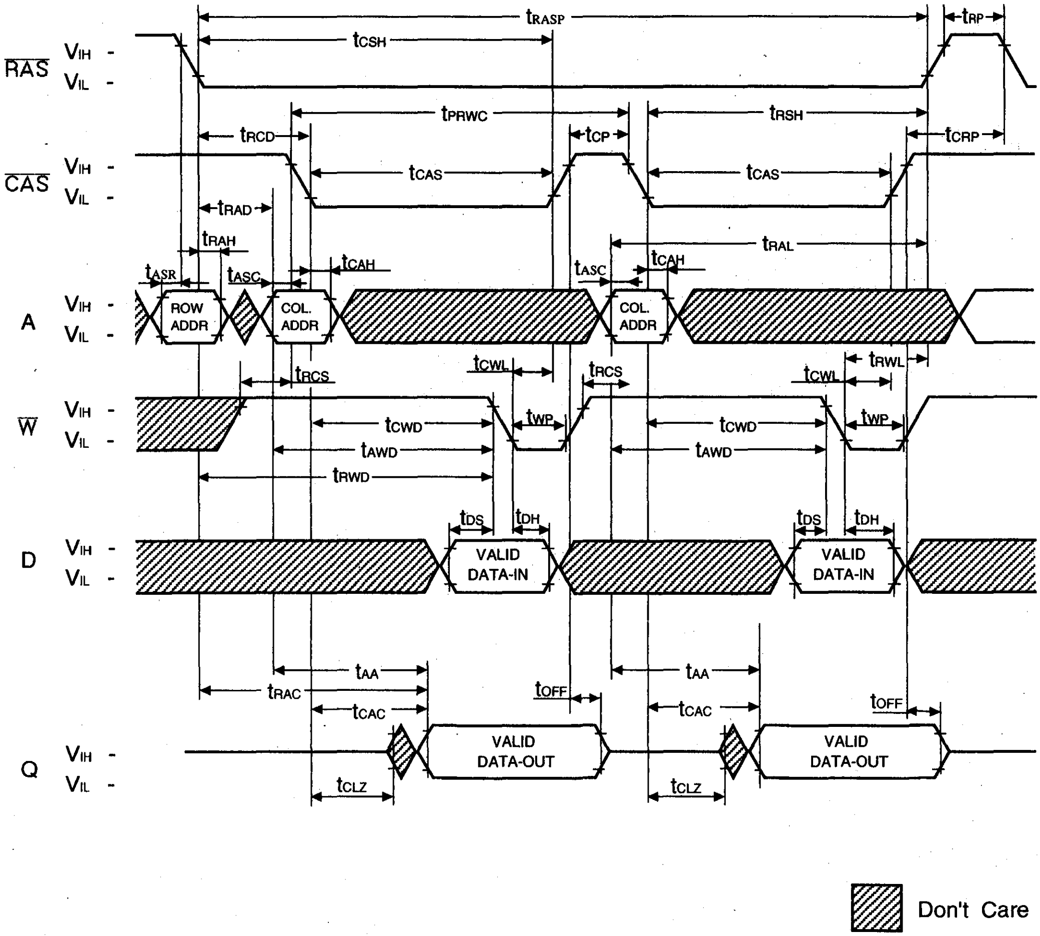


FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



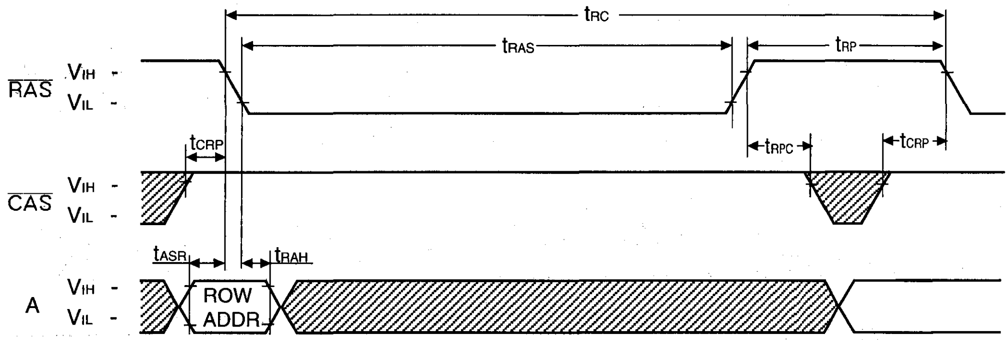
3

FAST PAGE MODE READ-MODIFY-WRITE CYCLE



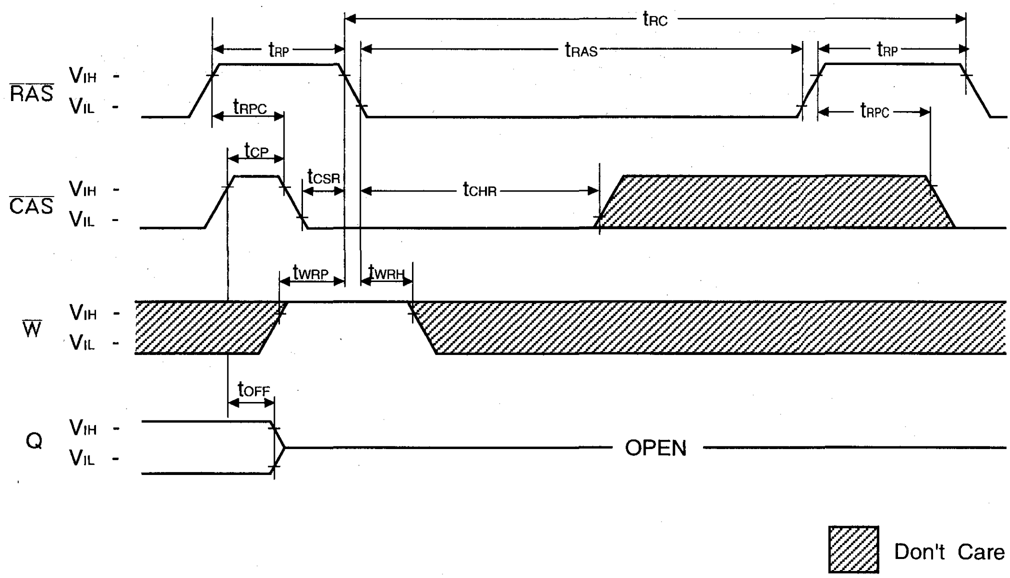
$\overline{RAS}$-ONLY REFRESH CYCLE

NOTE : $\overline{W}$, D_{IN} = Don't care
D_{OUT} = Open



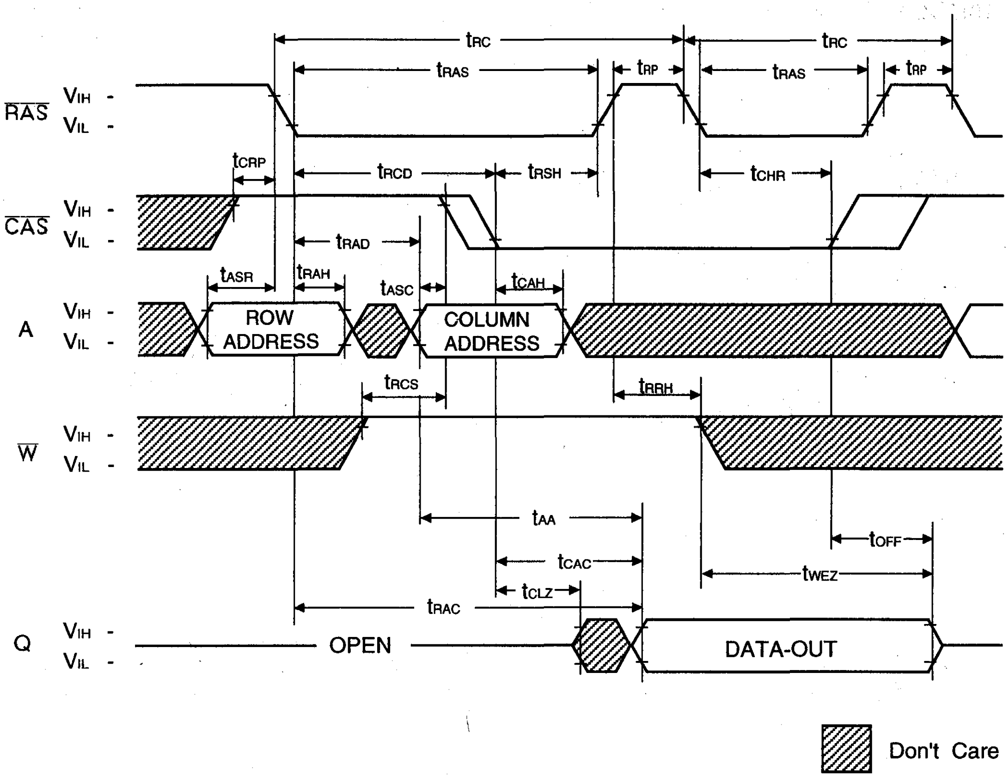
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE : A = Don't Care



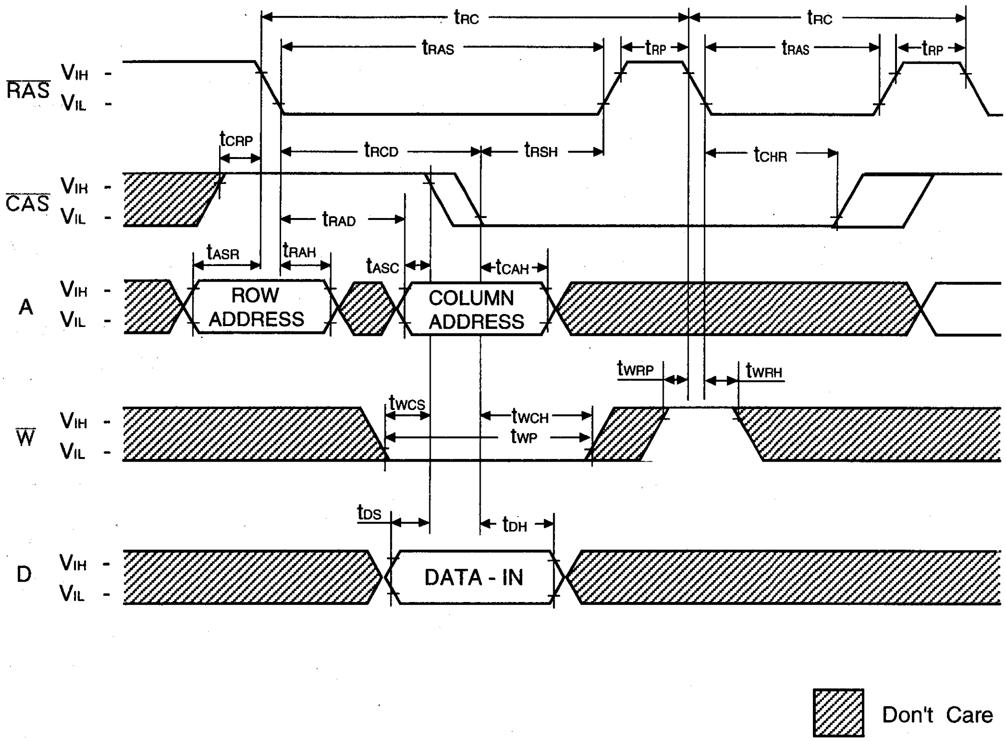
3

HIDDEN REFRESH CYCLE (READ)



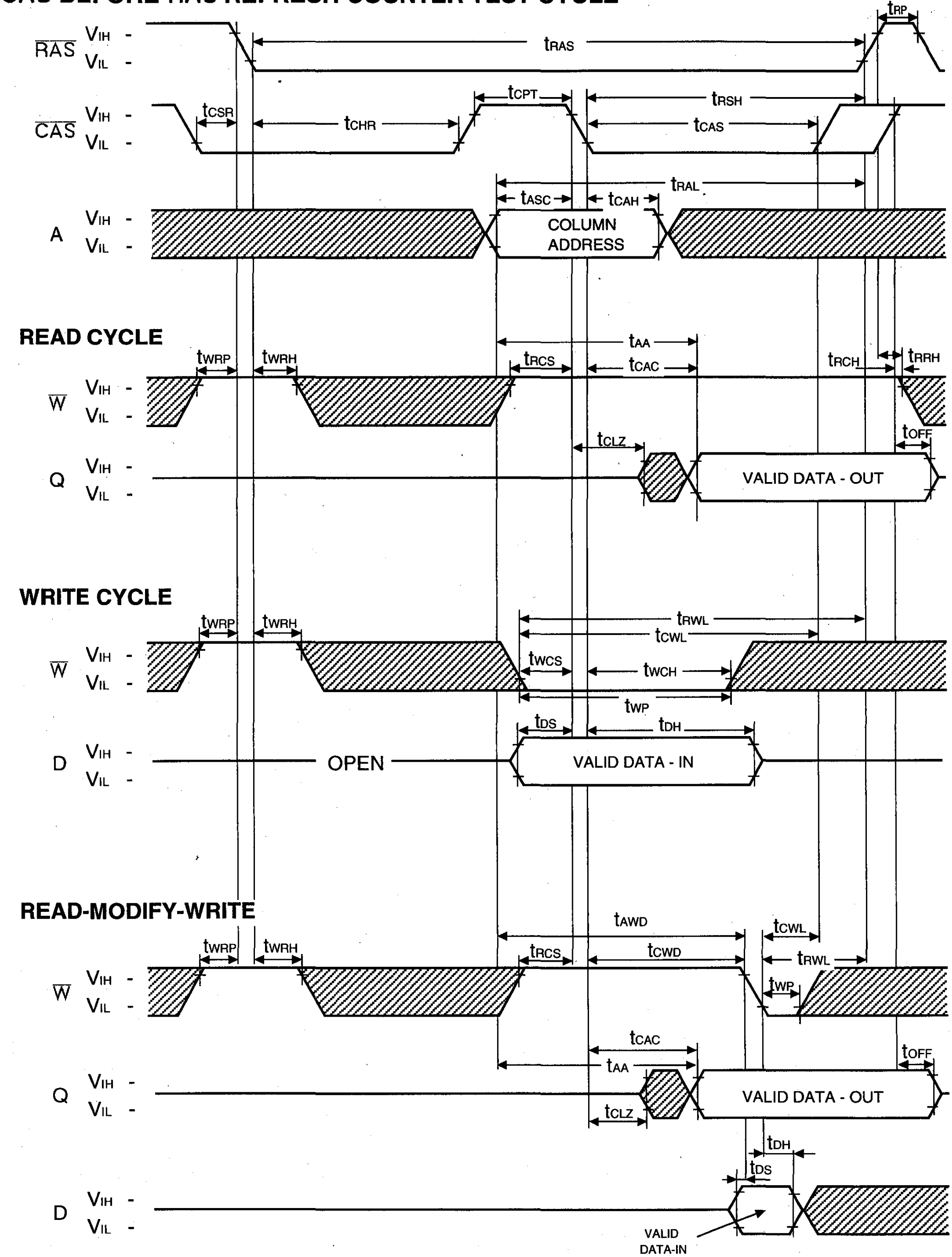
HIDDEN REFRESH CYCLE (WRITE)

NOTE : D_{OUT} = OPEN



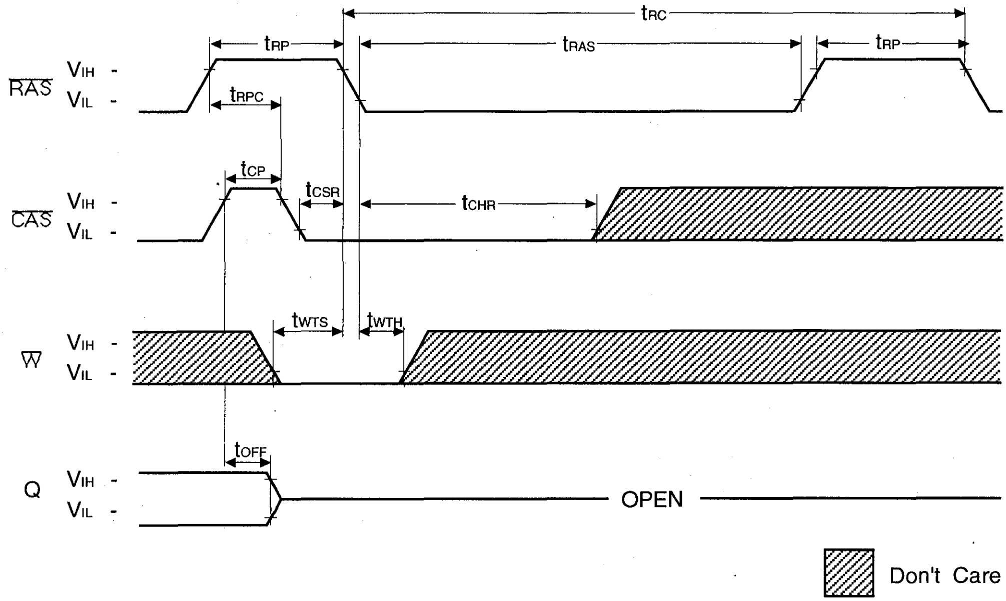
3

$\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE



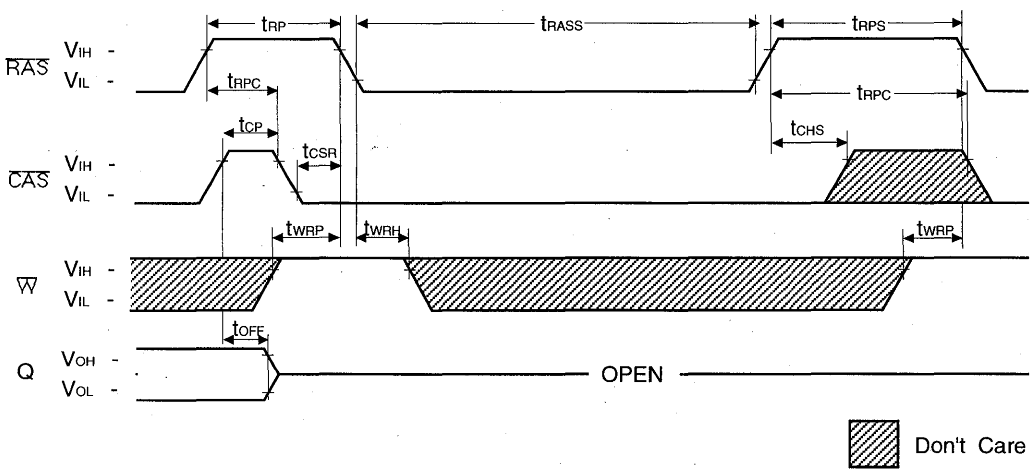
TEST MODE IN CYCLE

NOTE : D, A = Don't Care



CAS-BEFORE-RAS SELF REFRESH CYCLE

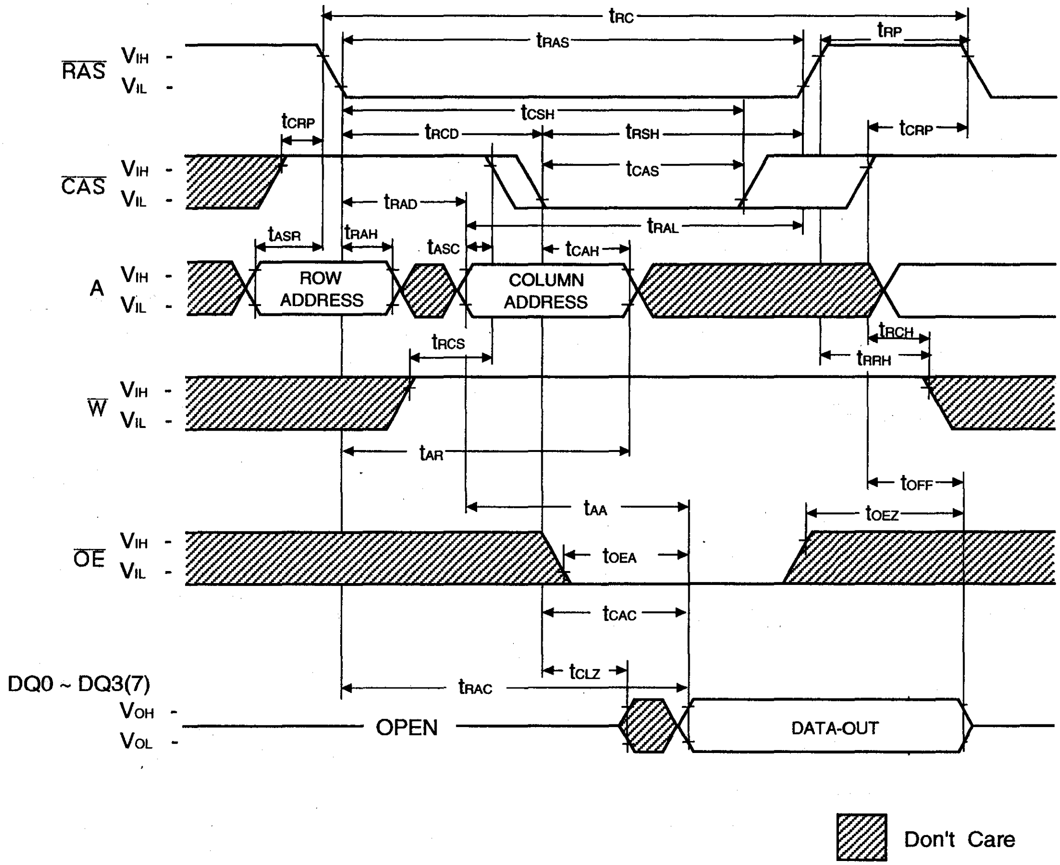
NOTE : A ddress = Don't Care



Fast Page Mode, x4 and x8 Device

TIMING DIAGRAM

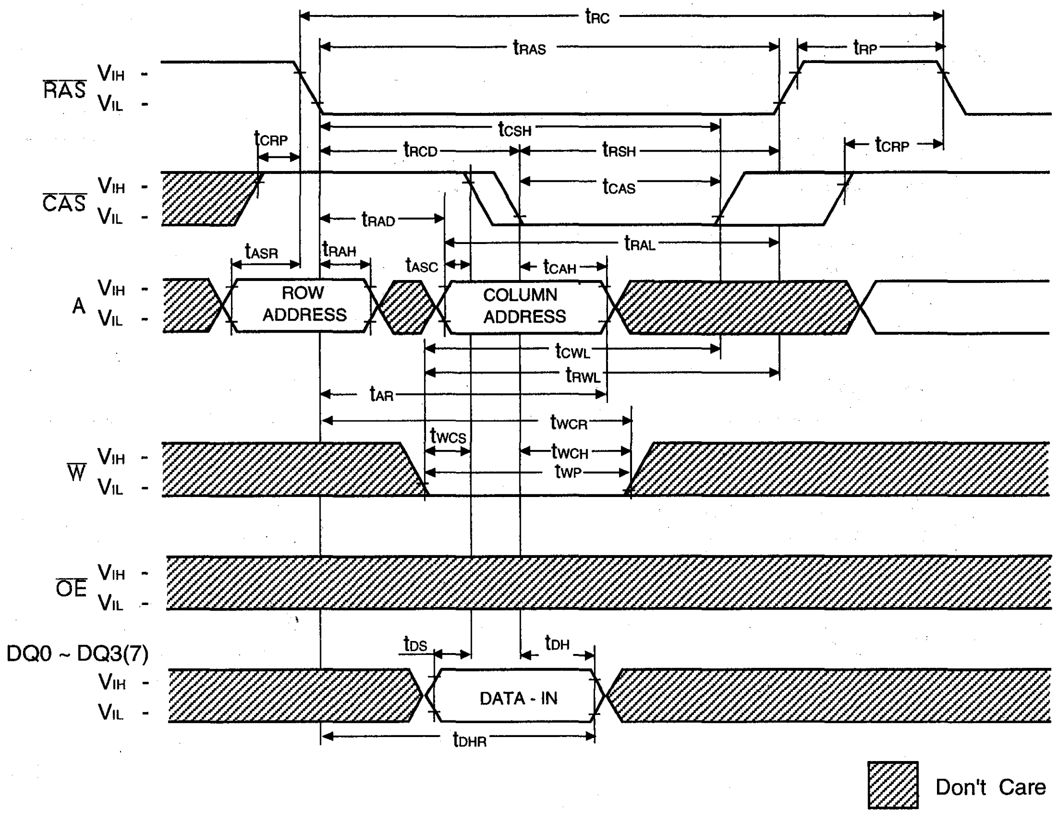
READ CYCLE



3

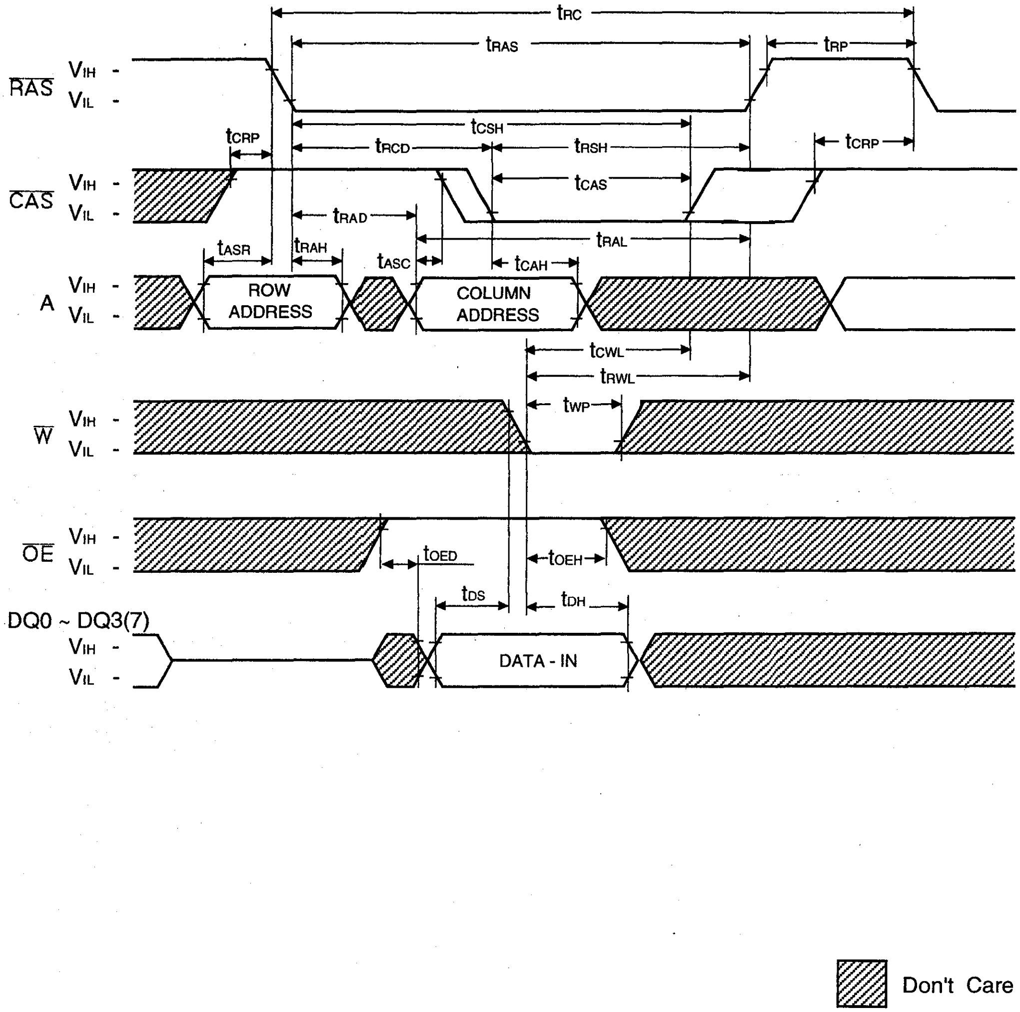
WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = OPEN



WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

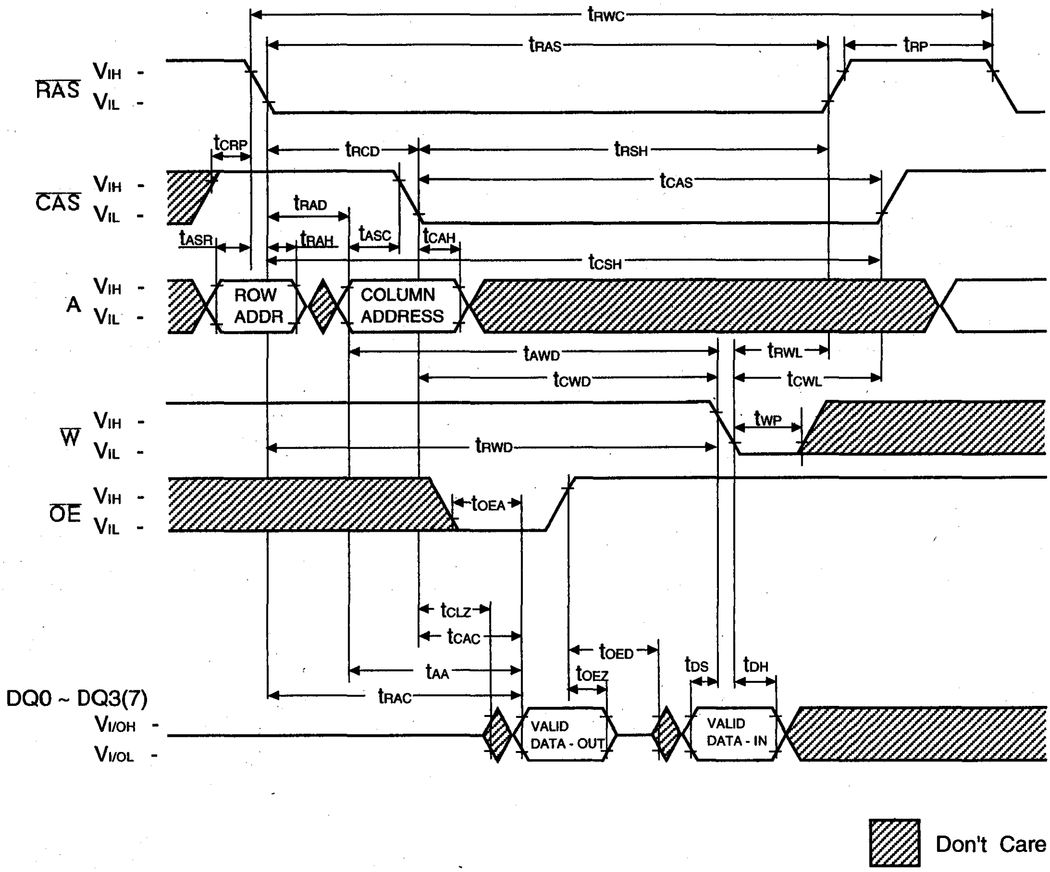
NOTE : D_{OUT} = OPEN



3

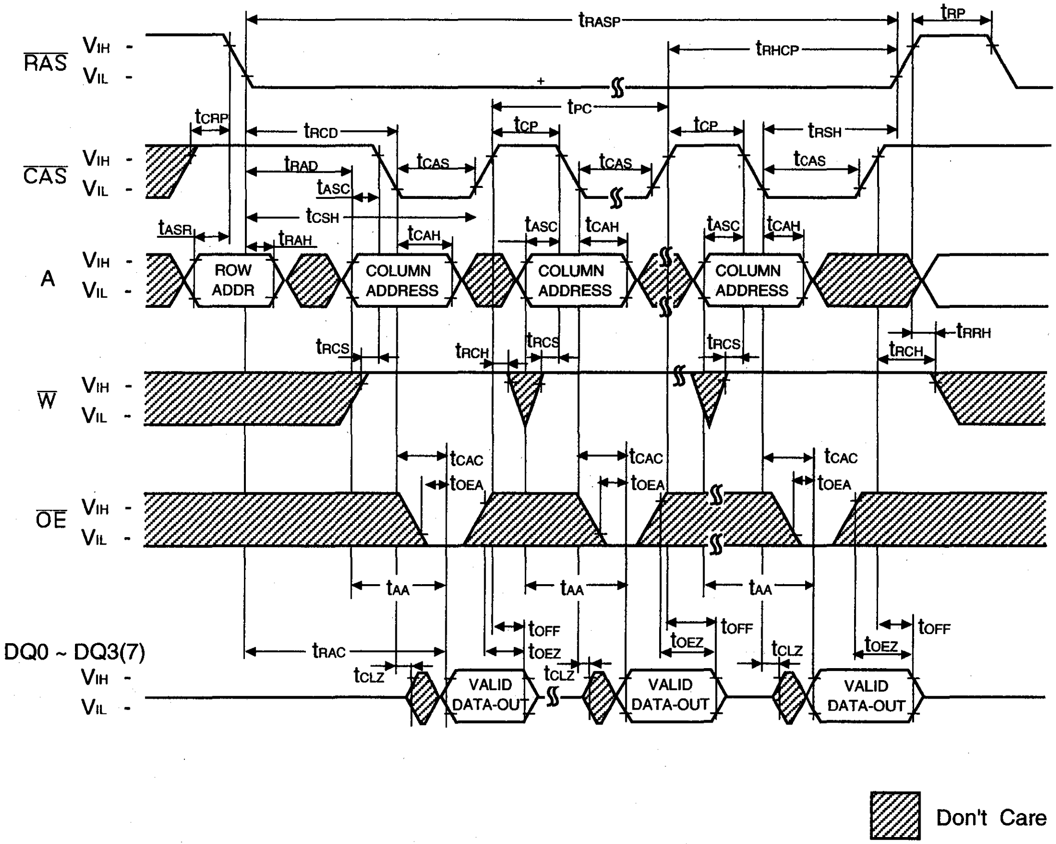
SAMSUNG ELECTRONICS

READ - MODIFY - WRITE CYCLE



FAST PAGE READ CYCLE

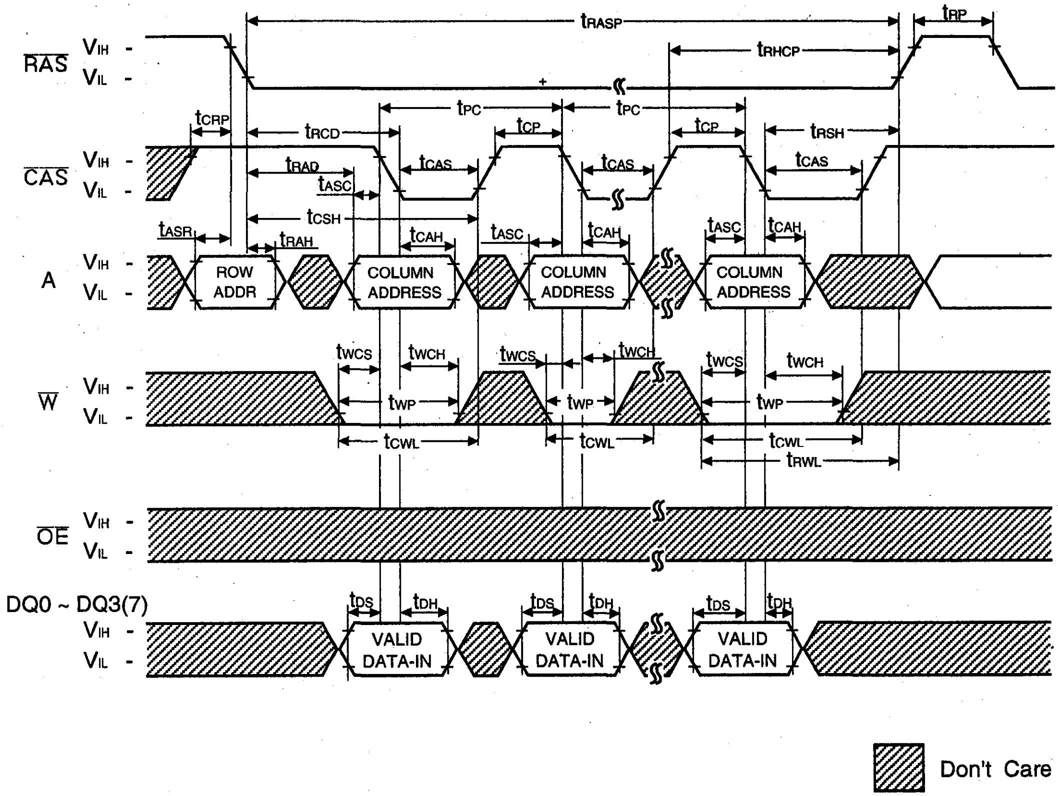
NOTE : D_{OUT} = Open



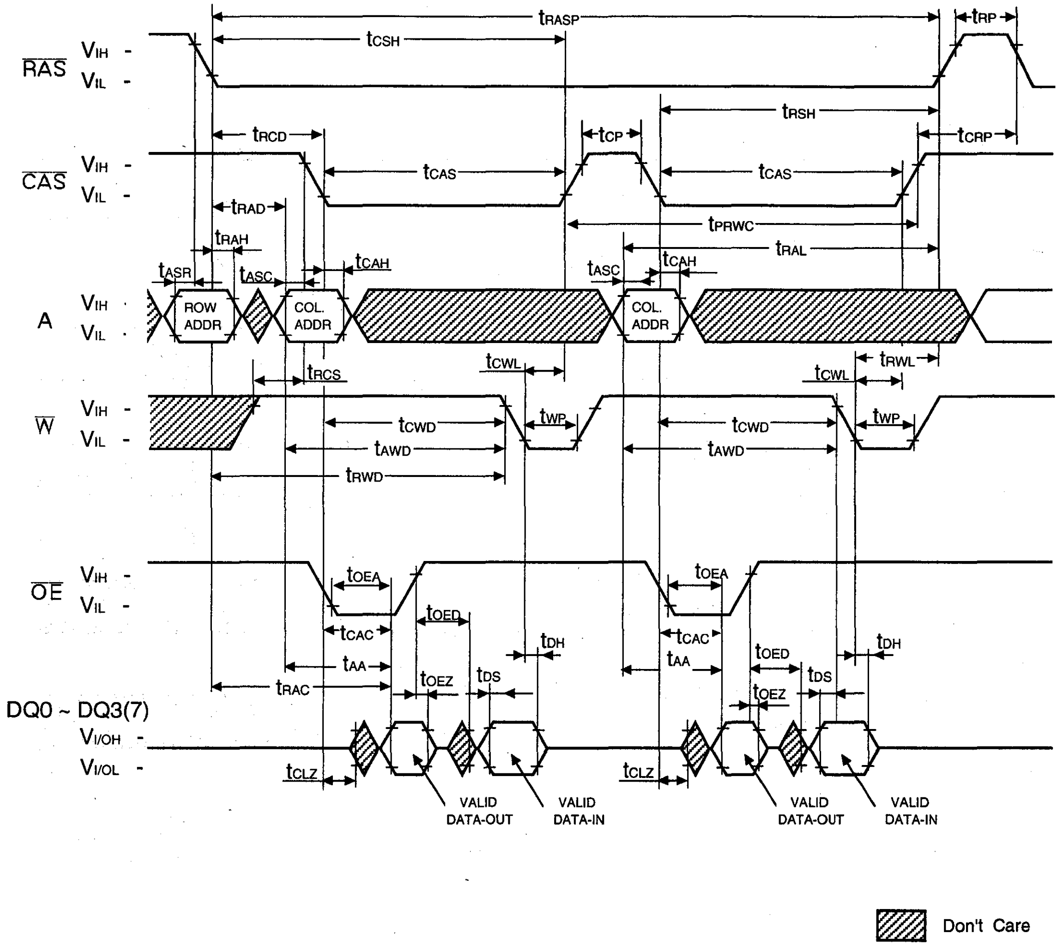
SAMSUNG ELECTRONICS

FAST PAGE WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = Open



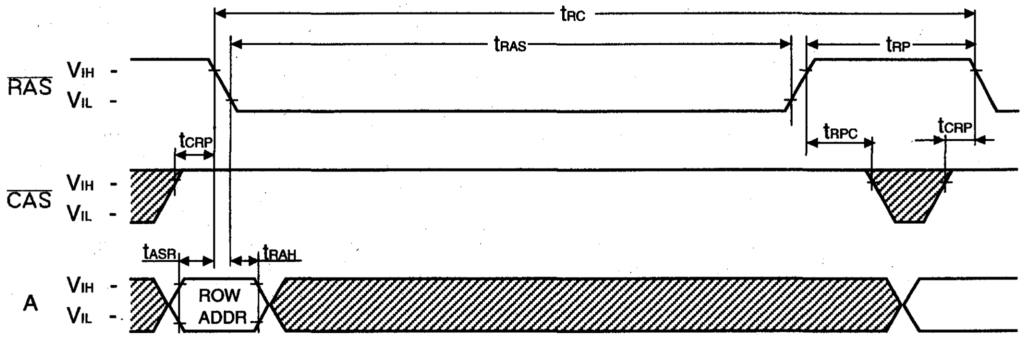
FAST PAGE READ-MODIFY-WRITE CYCLE



3

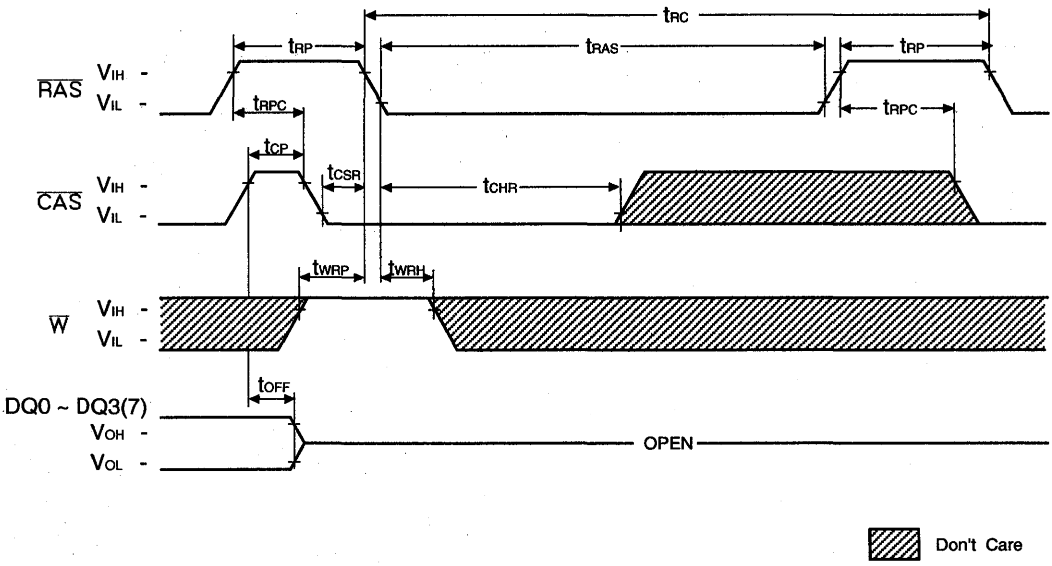
$\overline{RAS}$-ONLY REFRESH CYCLE

NOTE : $\overline{W}$, $\overline{OE}$, D_{IN} = Don't care
D_{OUT} = Open

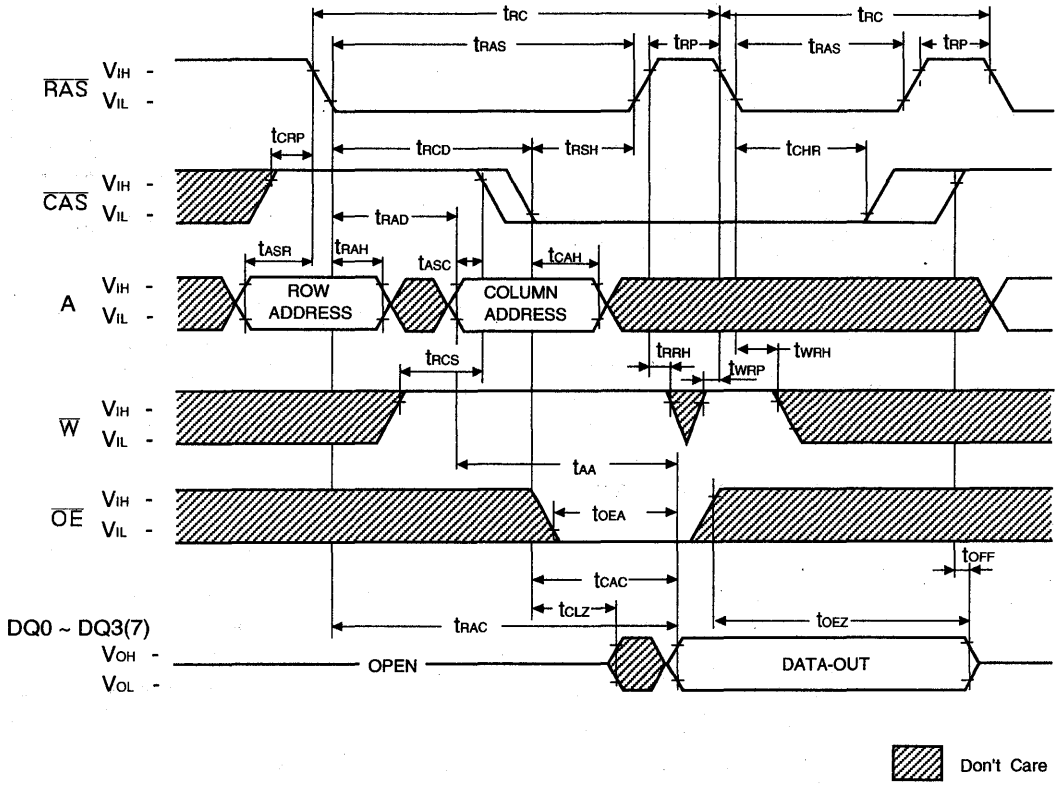


$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE : $\overline{W}$, $\overline{OE}$, A = Don't Care



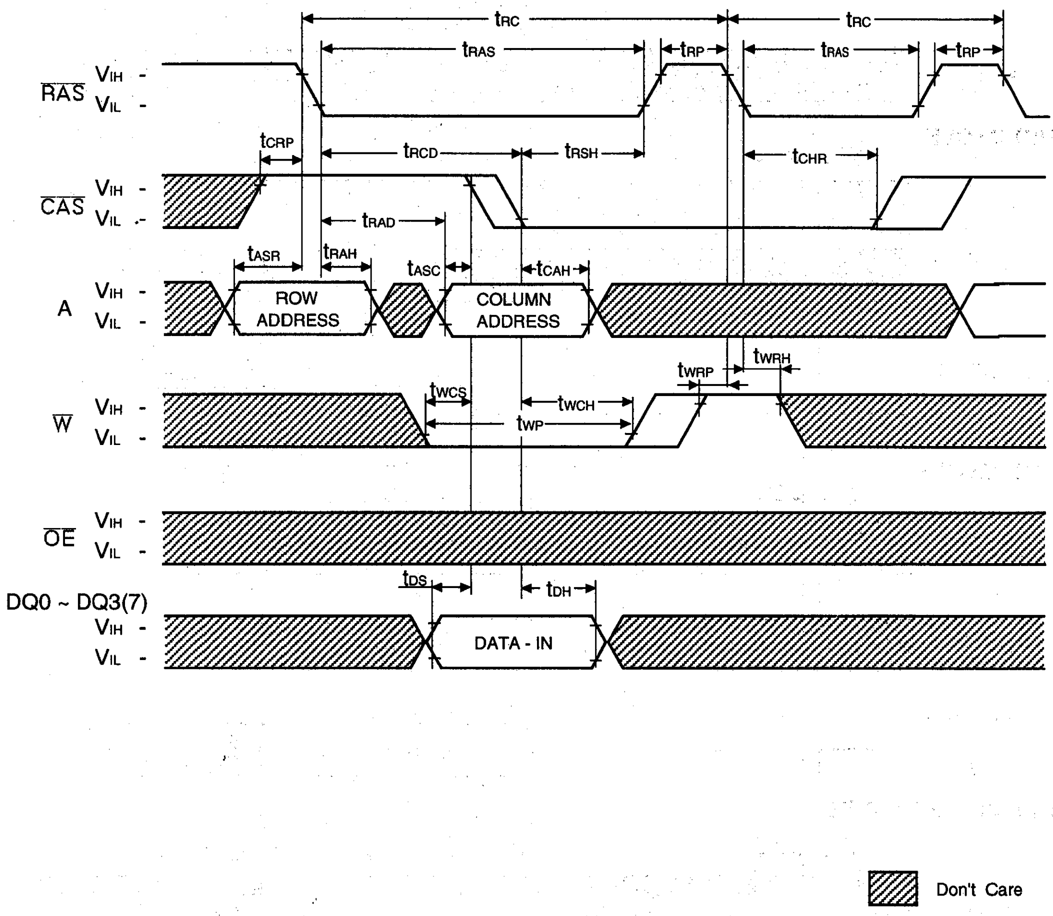
HIDDEN REFRESH CYCLE (READ)



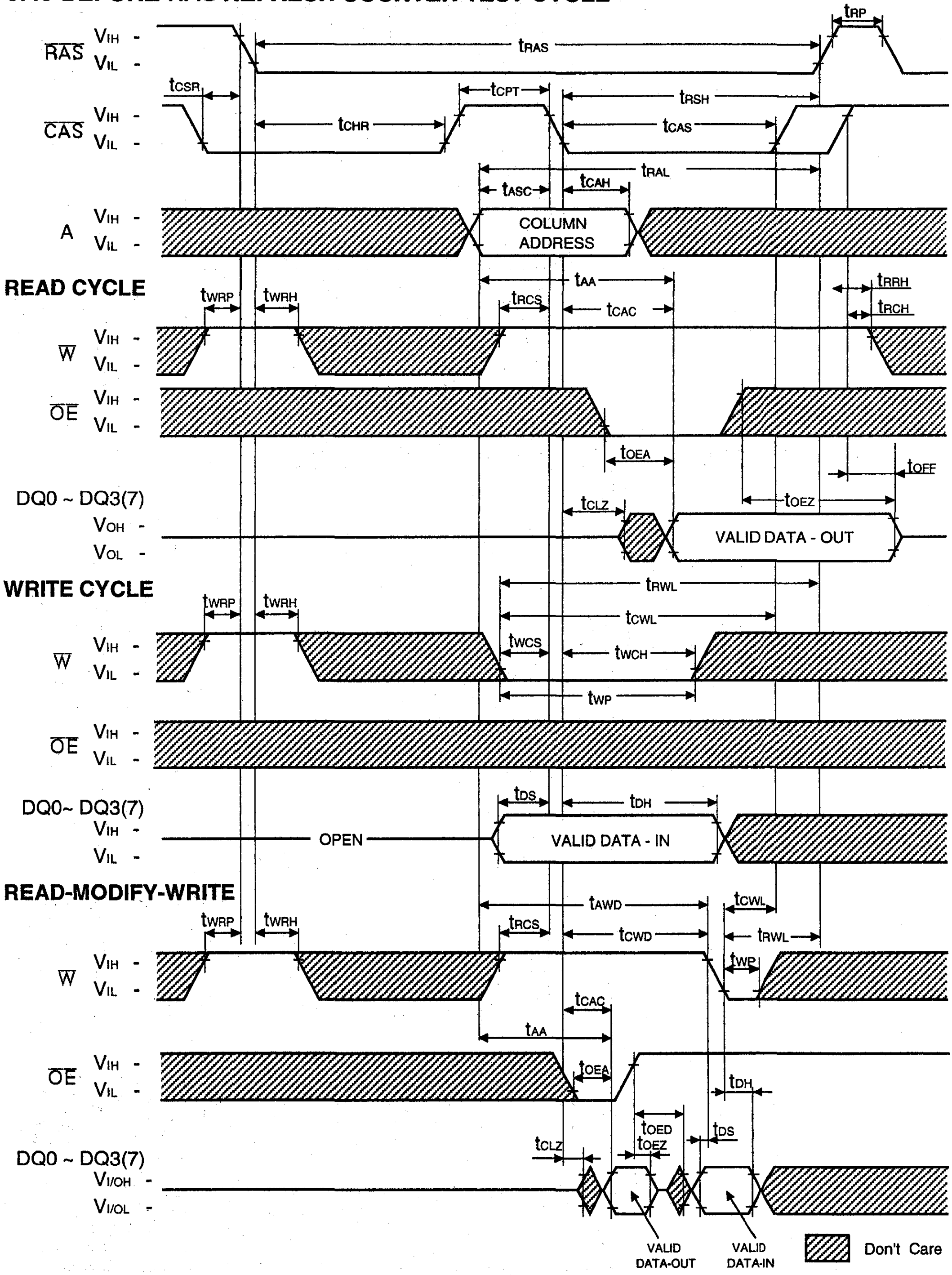
3

HIDDEN REFRESH CYCLE (WRITE)

NOTE : D_{OUT} = OPEN

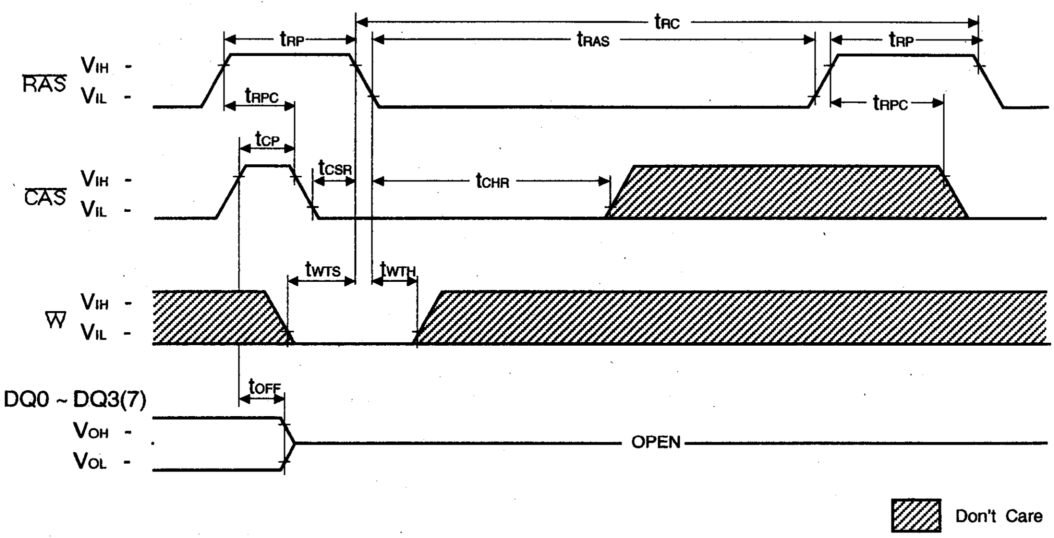


CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



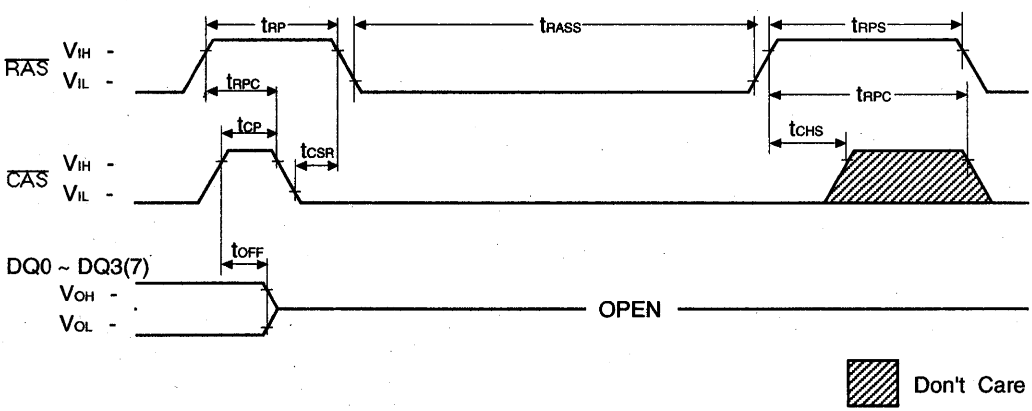
TEST MODE IN CYCLE

NOTE : $\overline{OE}$, A = Don't Care



$\overline{CAS}$-BEFORE-$\overline{RAS}$ SELF REFRESH CYCLE

NOTE : $\overline{W}$, $\overline{OE}$, A = Don't Care

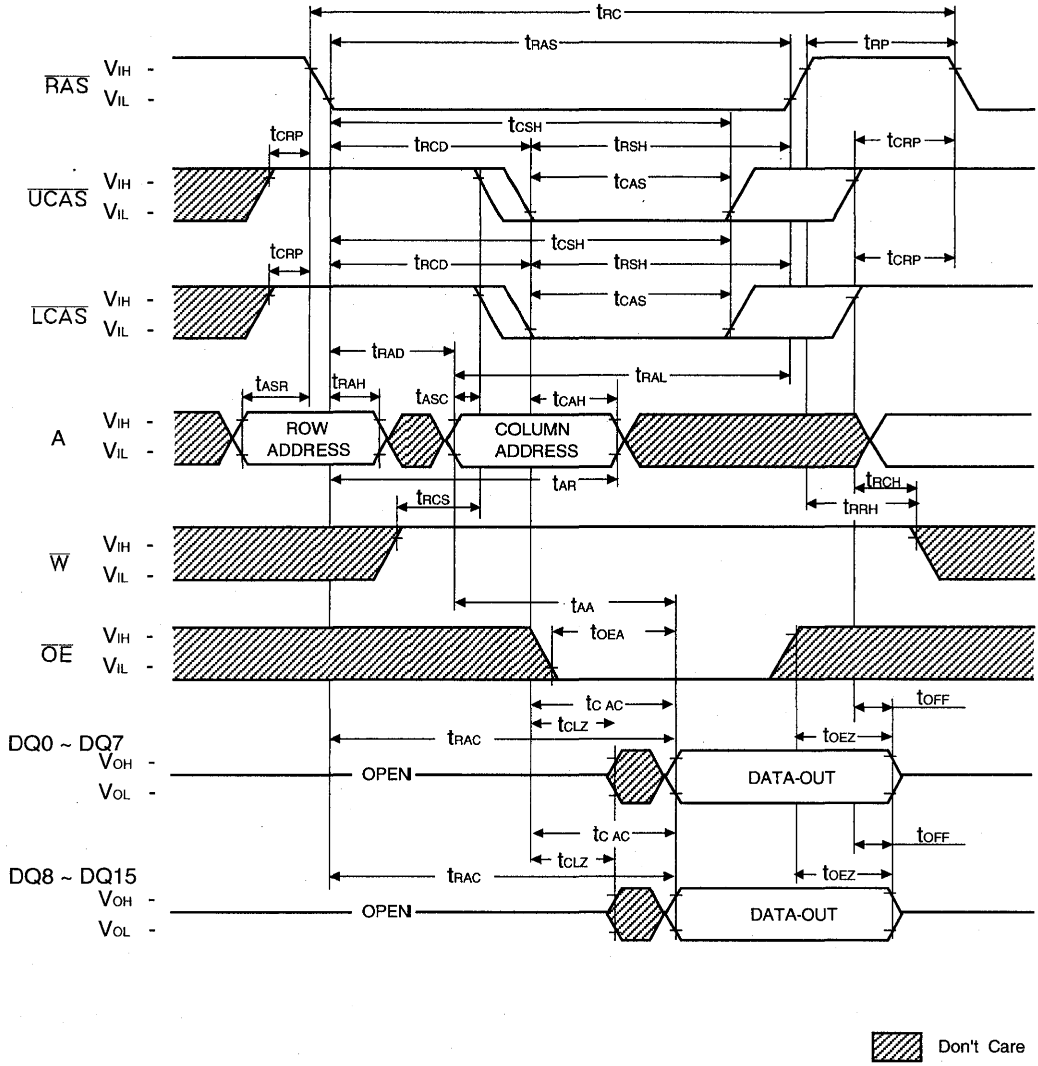


Fast Page Mode, x16 (2$\overline{CAS}$) Device

TIMING DIAGRAM

WORD READ CYCLE

NOTE : D_{IN} = OPEN



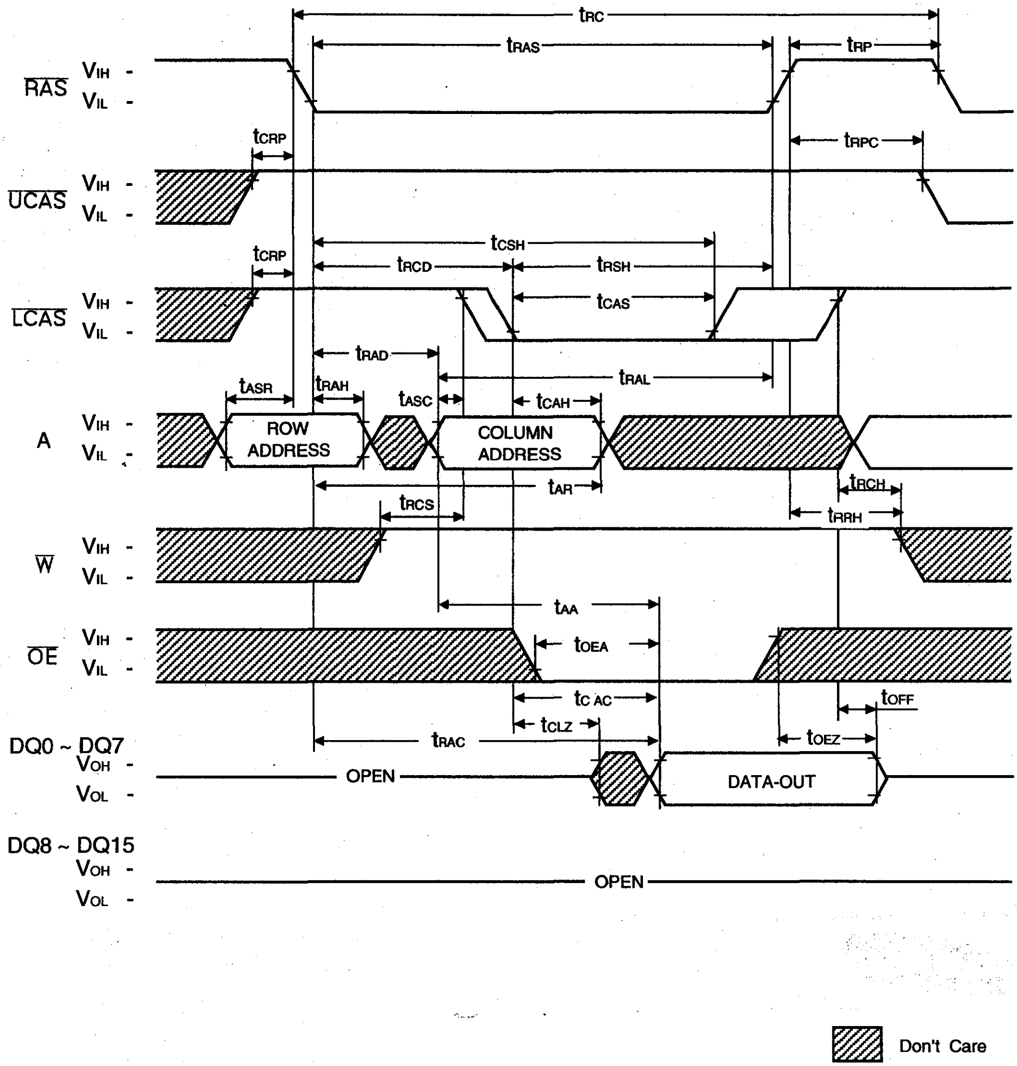
3

SAMSUNG ELECTRONICS

TIMING DIAGRAM

LOWER BYTE READ CYCLE

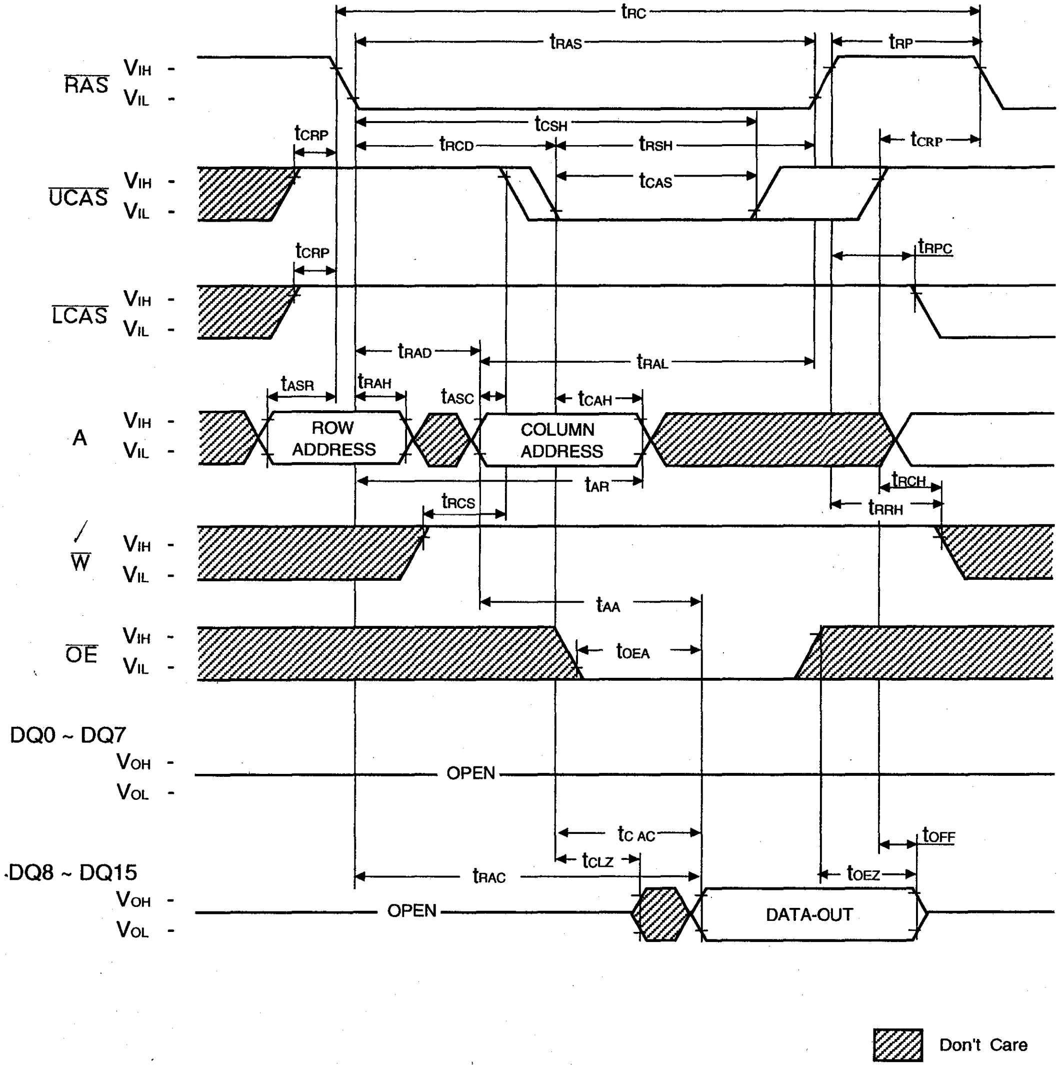
NOTE : D_{IN} = OPEN



TIMING DIAGRAM

UPPER BYTE READ CYCLE

NOTE : D_{IN} = OPEN

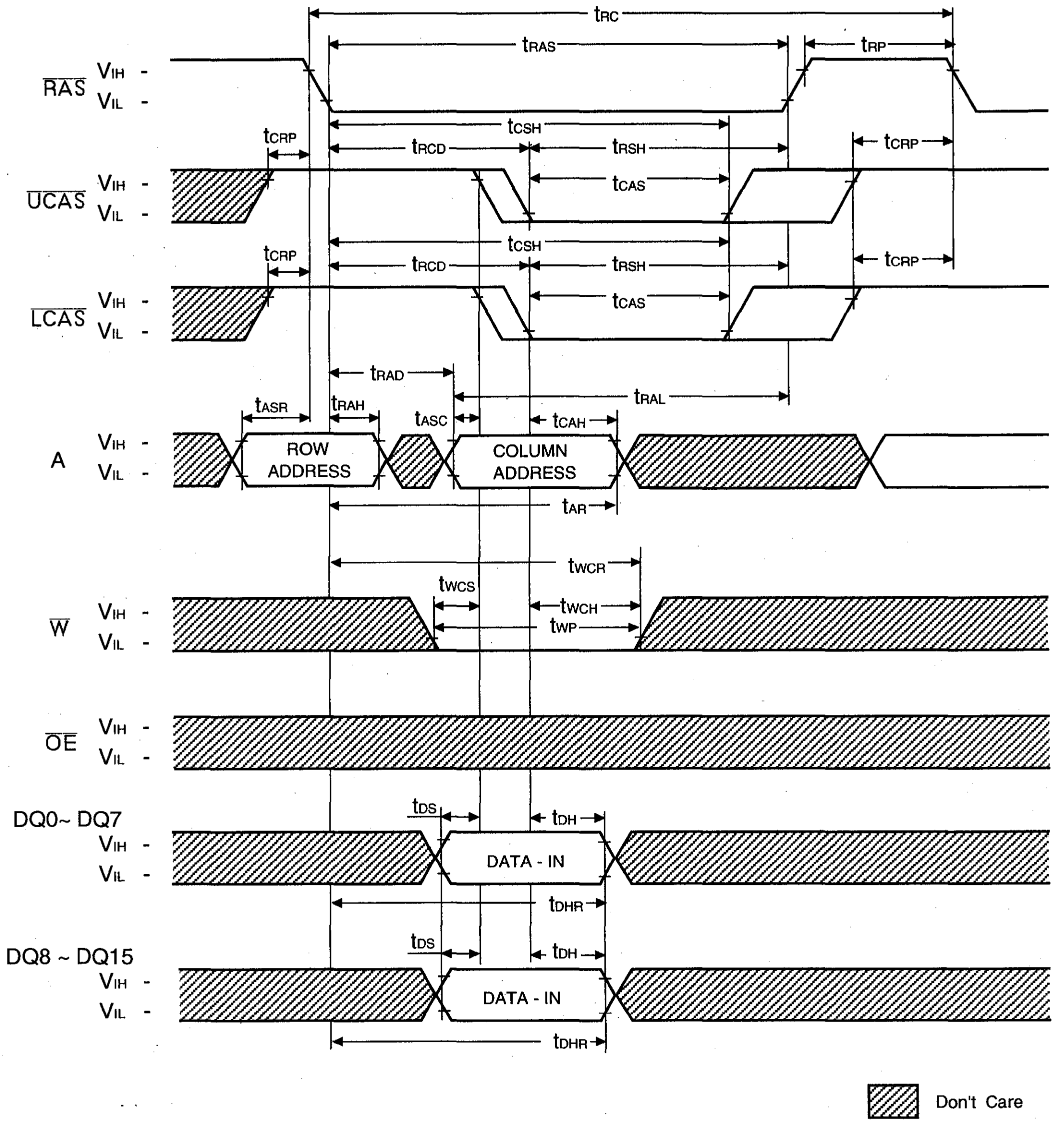


3

SAMSUNG ELECTRONICS

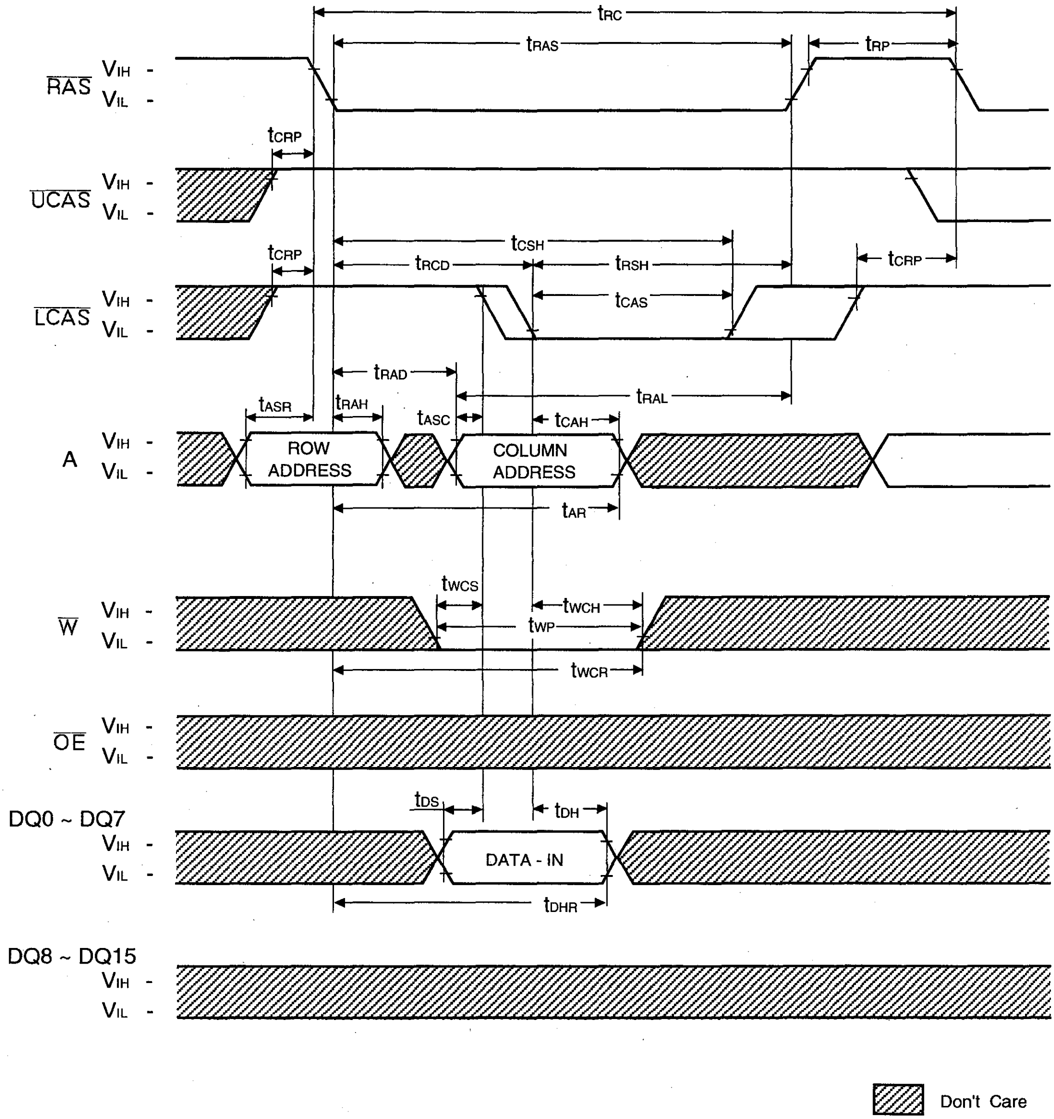
WORD WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = OPEN



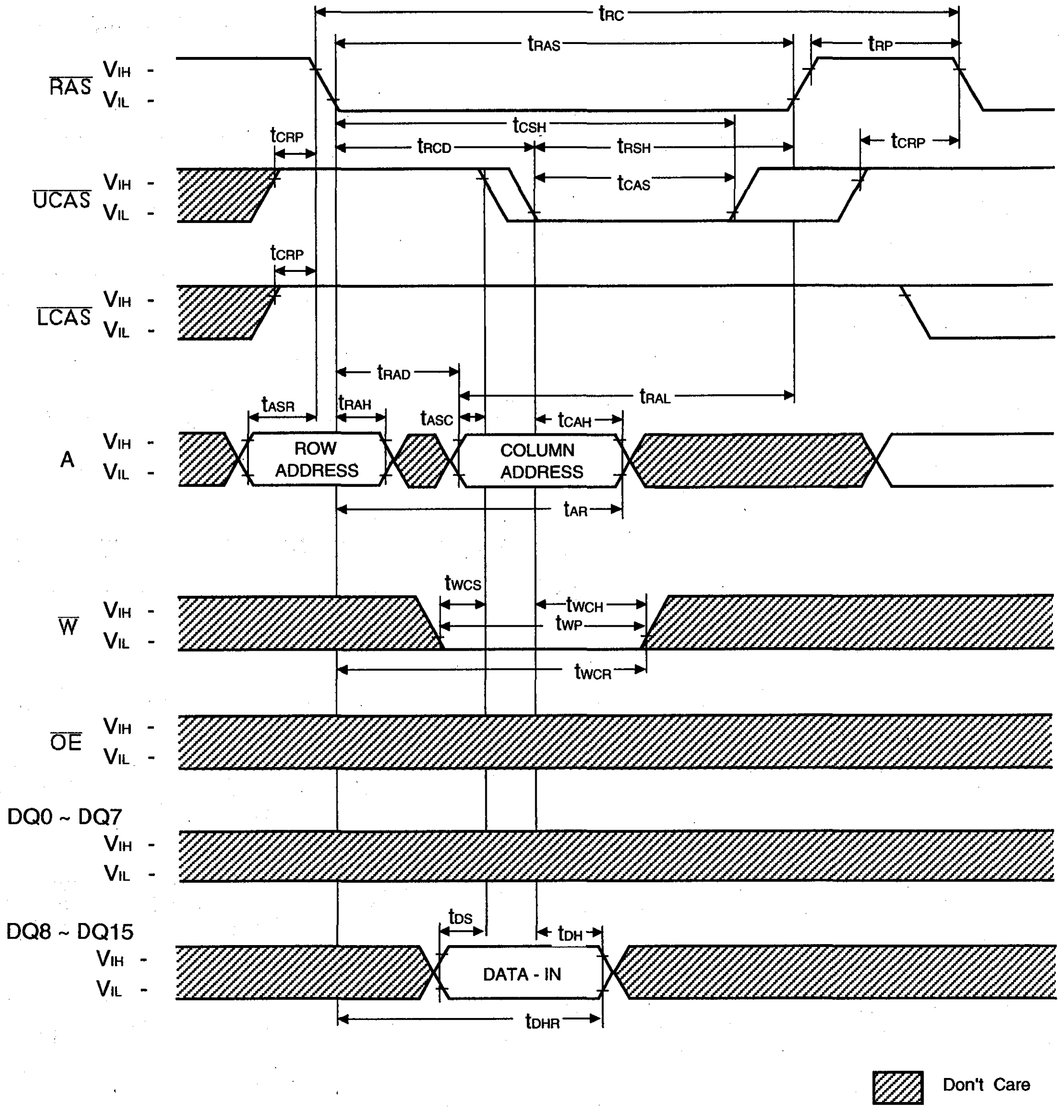
LOWER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = OPEN



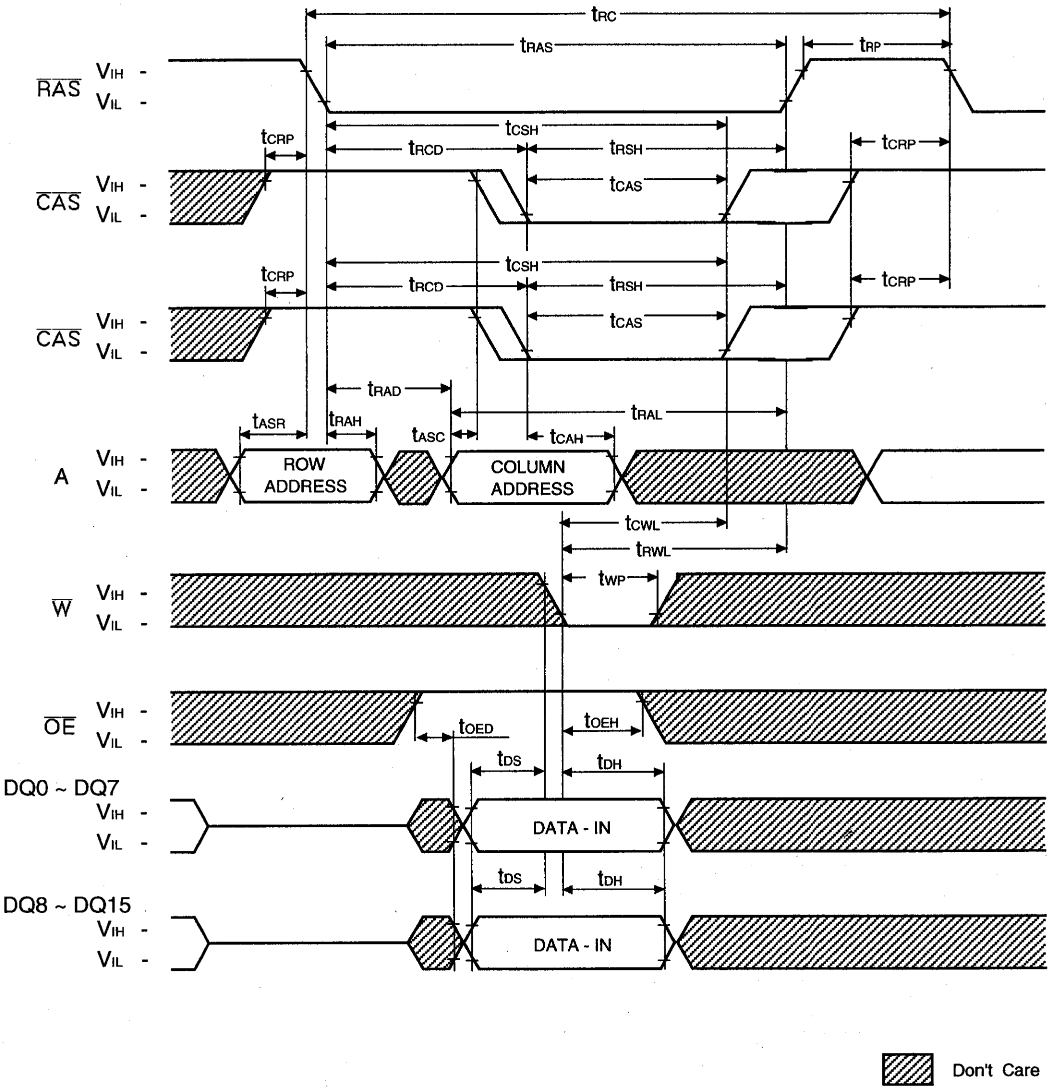
UPPER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = OPEN



WORD WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

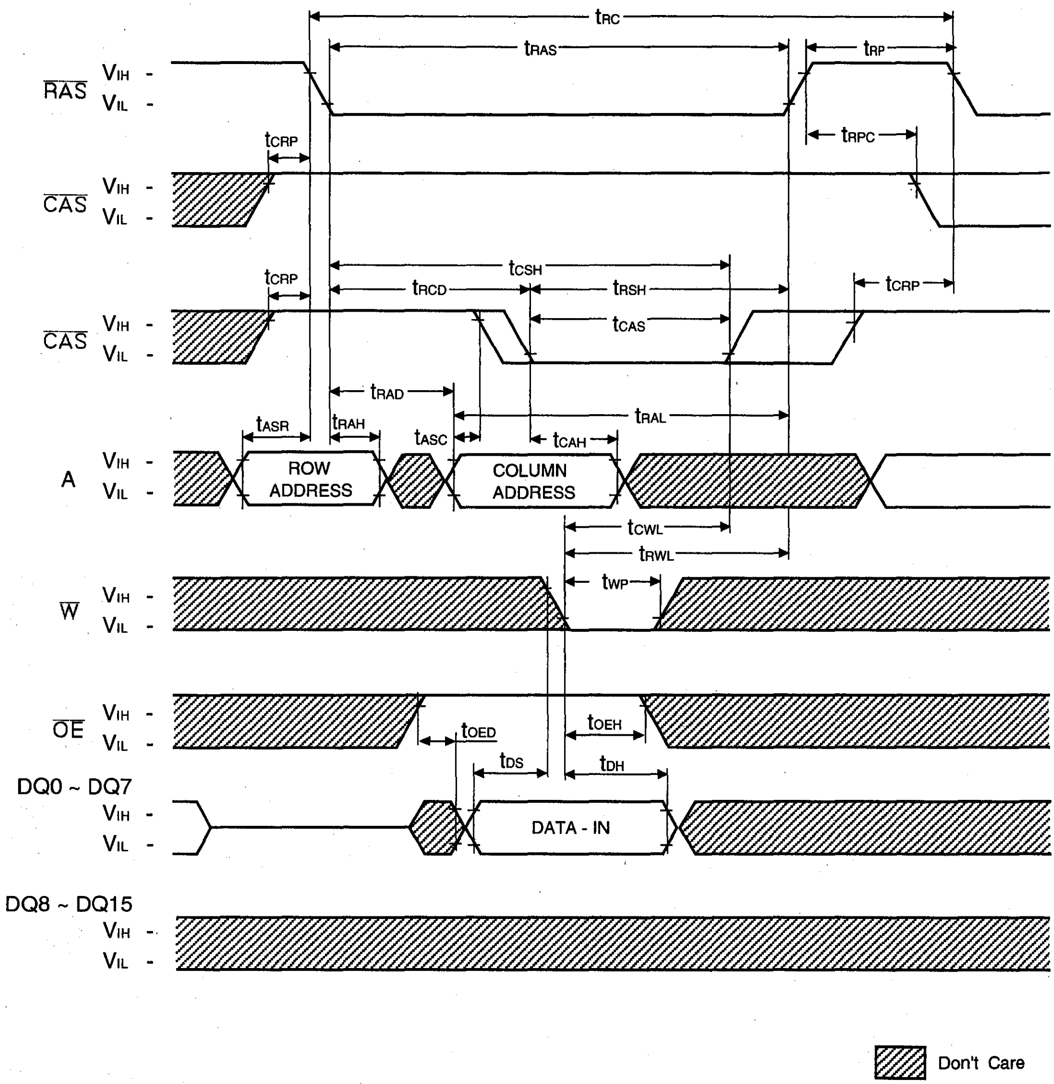
NOTE : D_{OUT} = OPEN



3

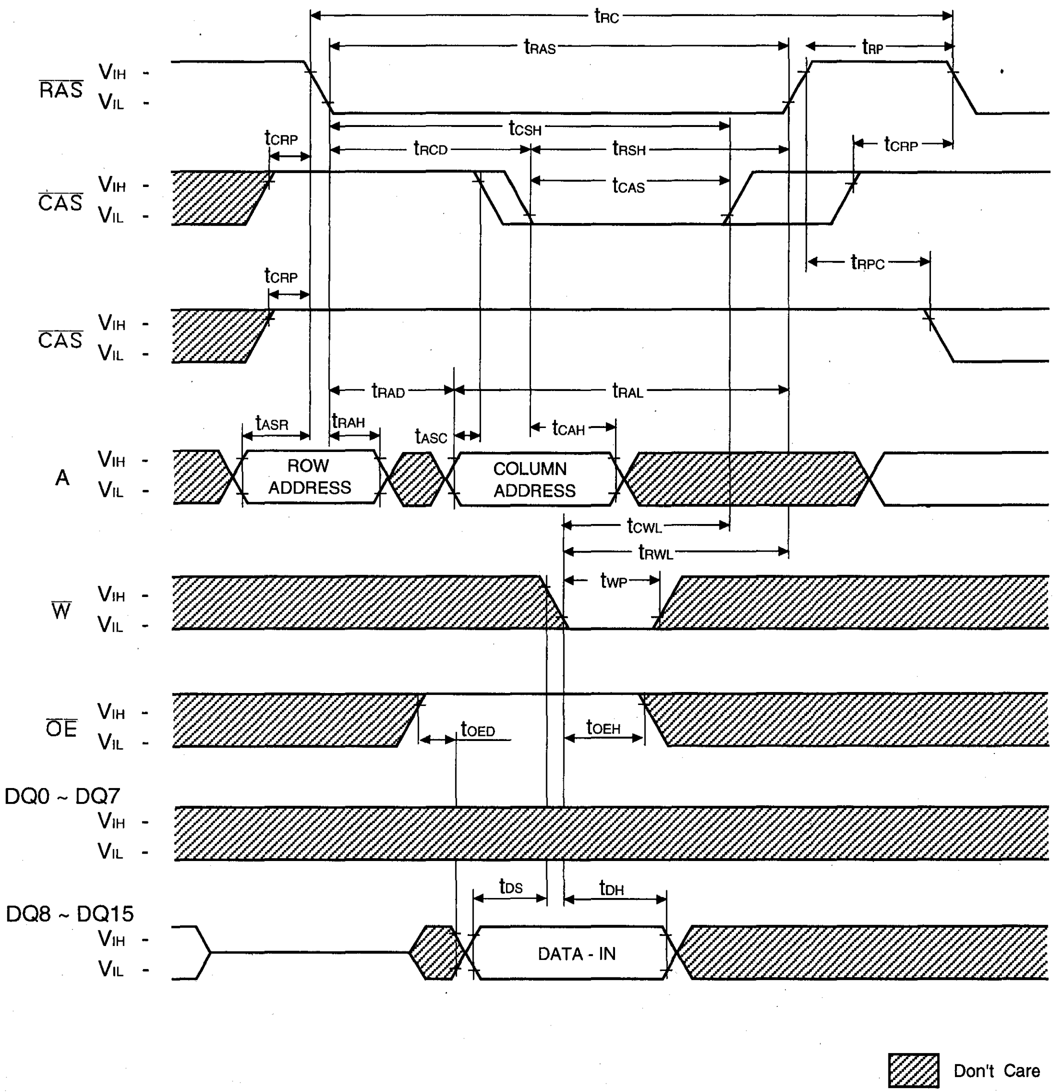
LOWER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

NOTE : D_{OUT} = OPEN

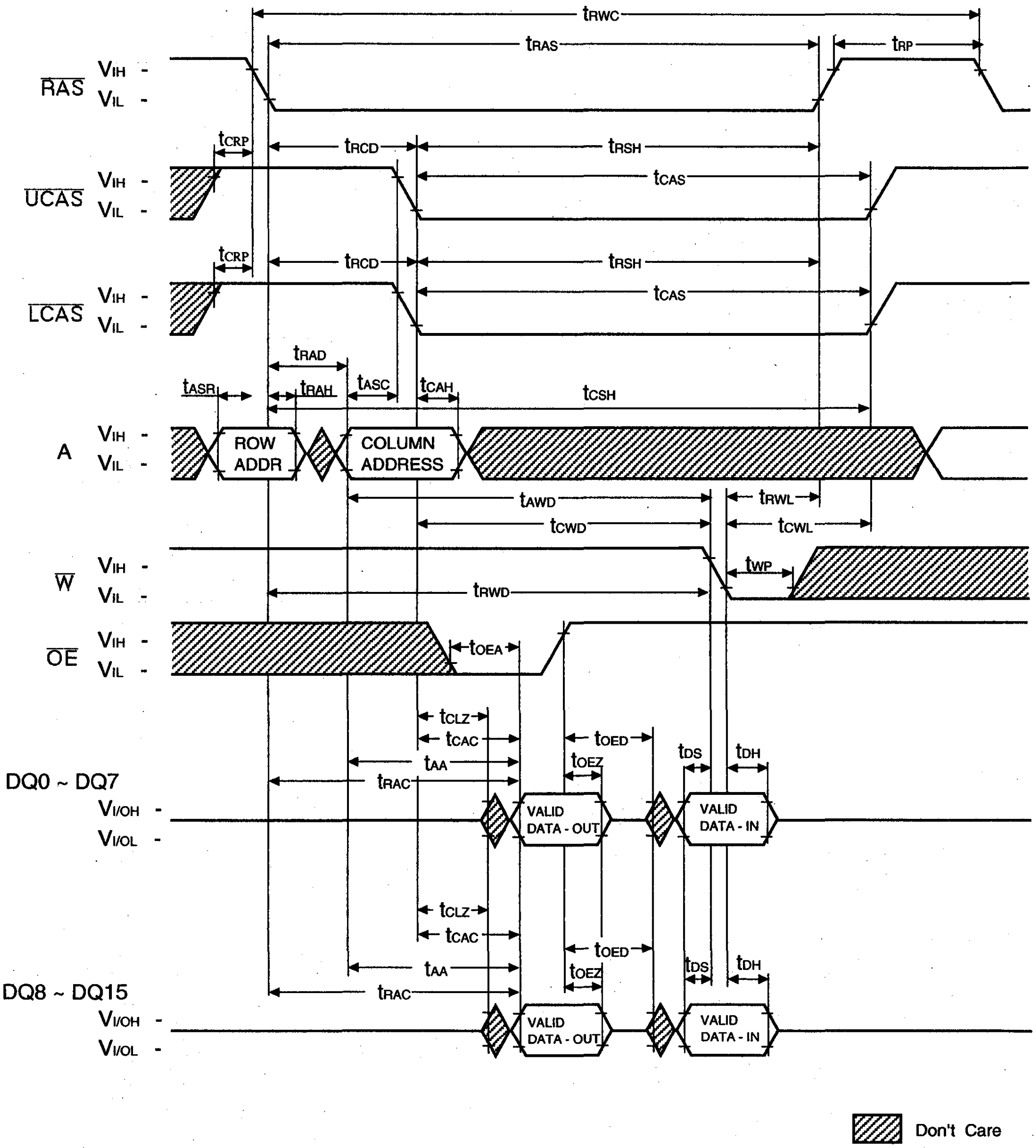


UPPER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

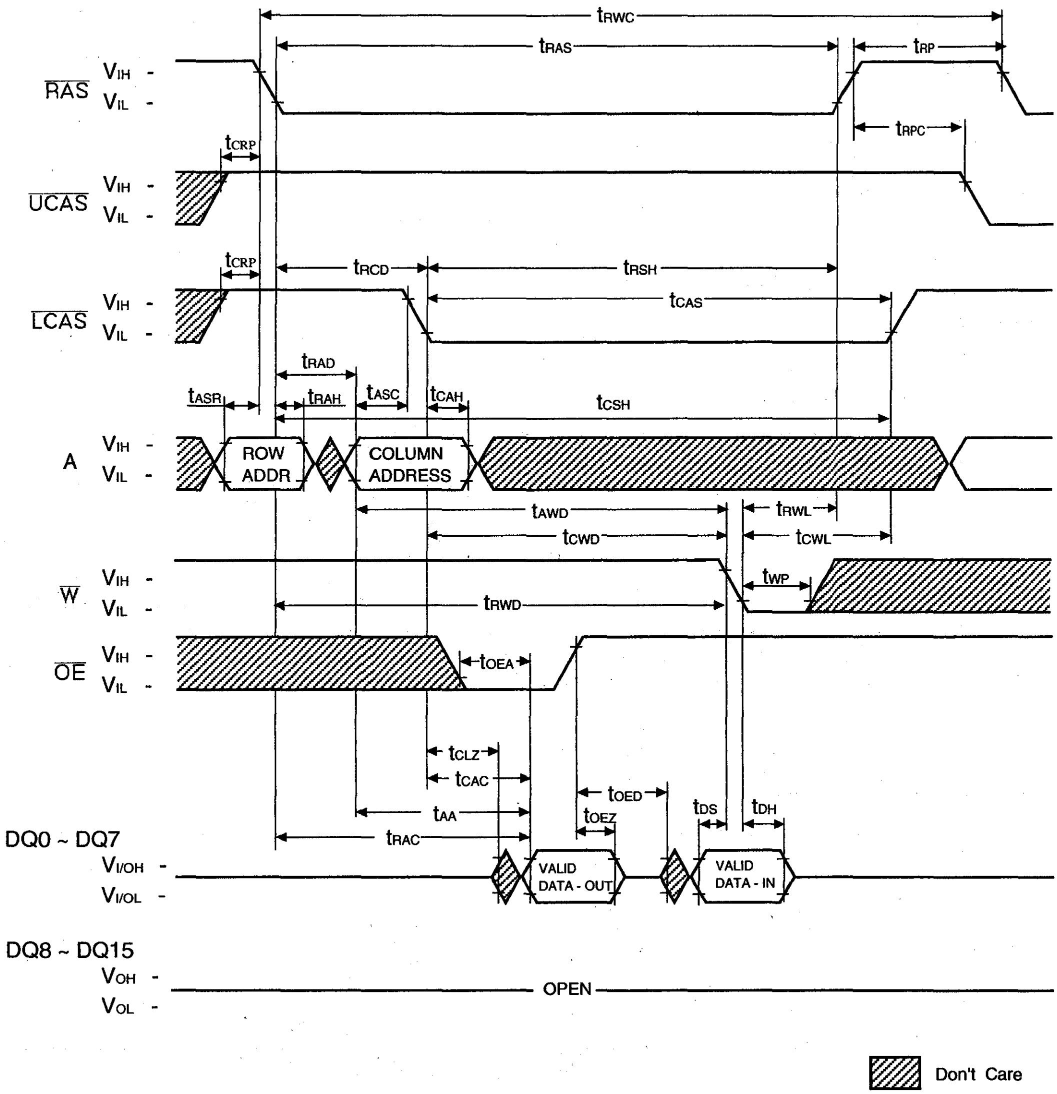
NOTE : D_{OUT} = OPEN



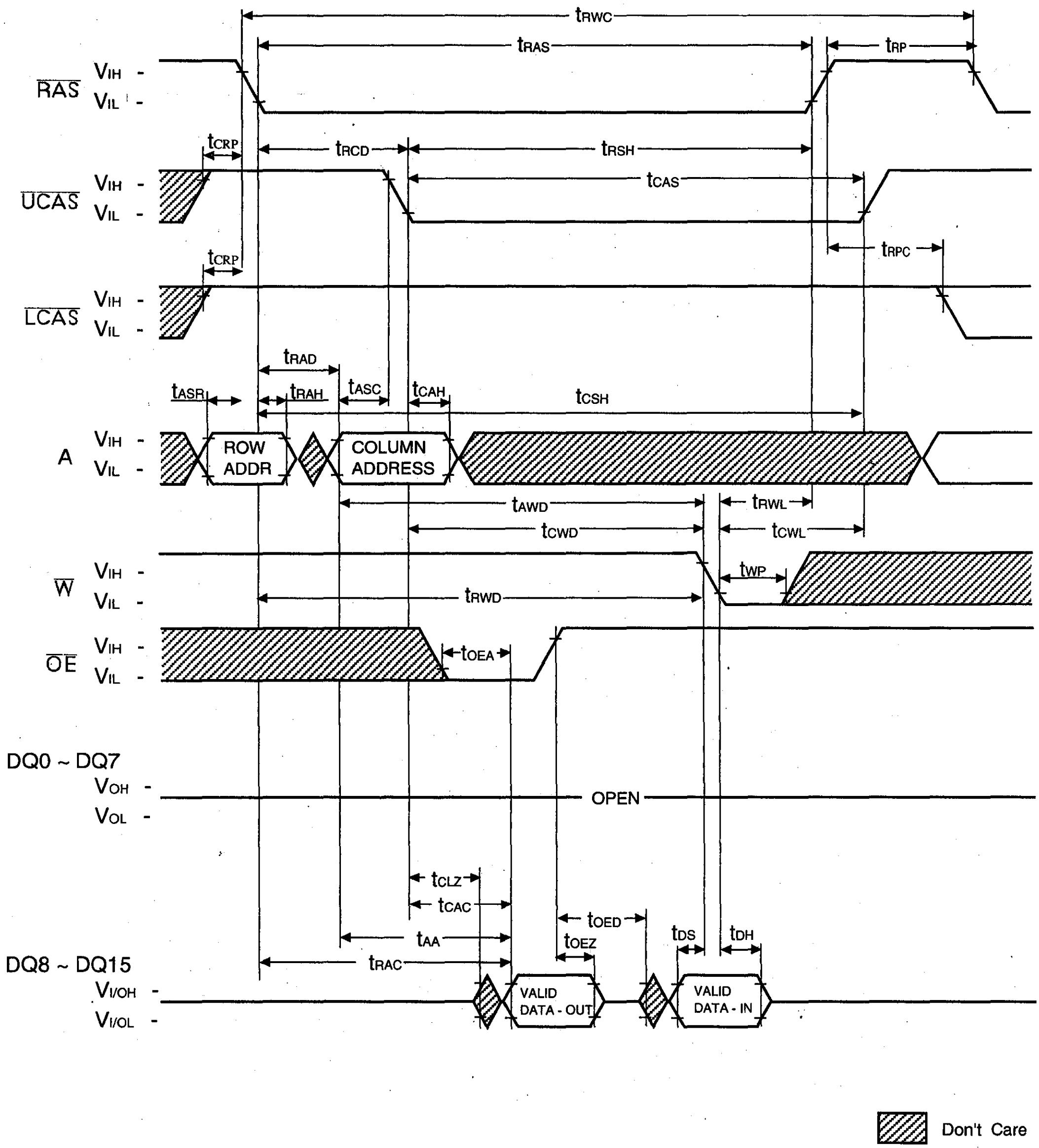
WORD READ - MODIFY - WRITE CYCLE



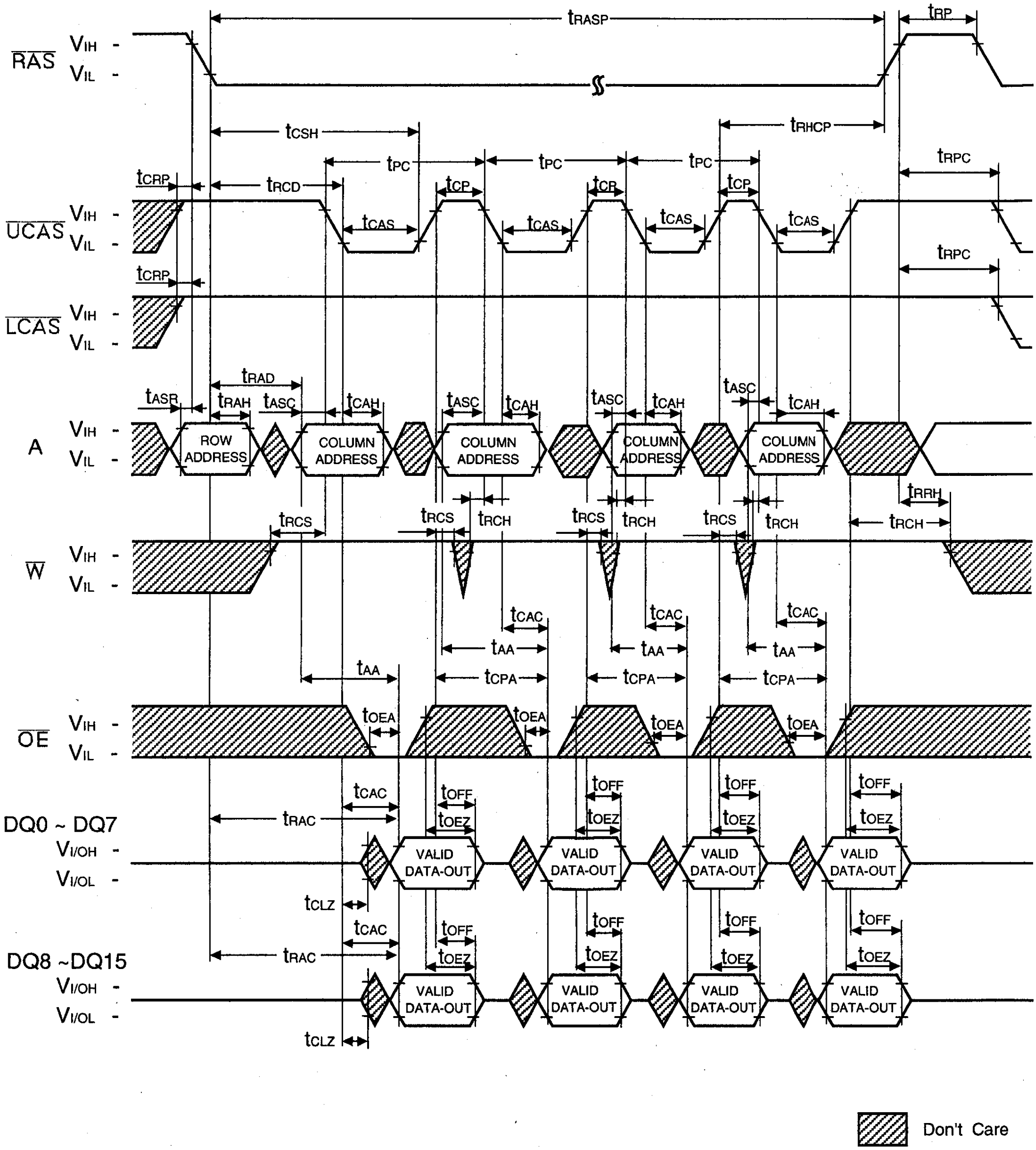
LOWER-BYTE READ - MODIFY - WRITE CYCLE



UPPER-BYTE READ - MODIFY - WRITE CYCLE



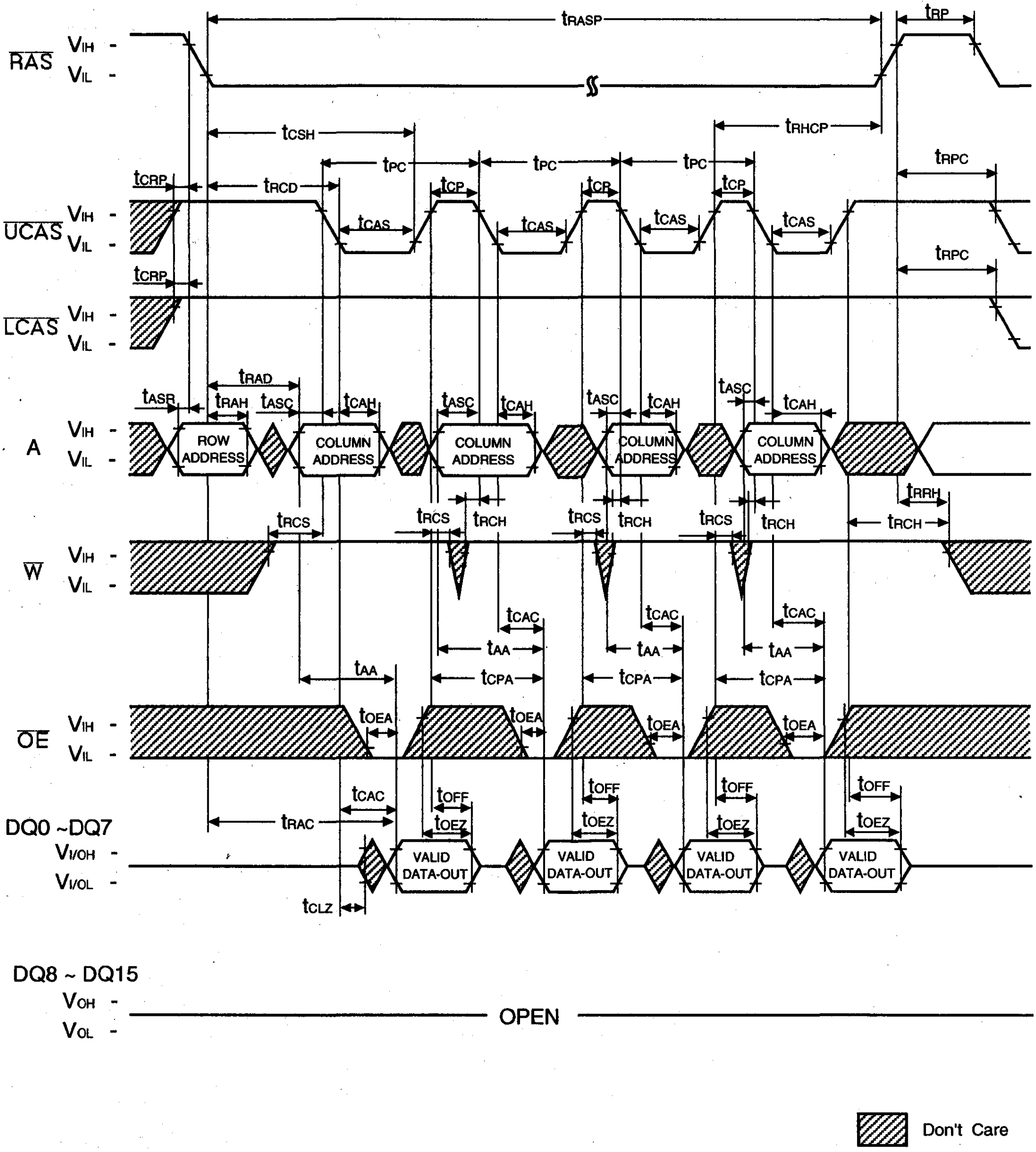
FAST PAGE MODE WORD READ CYCLE



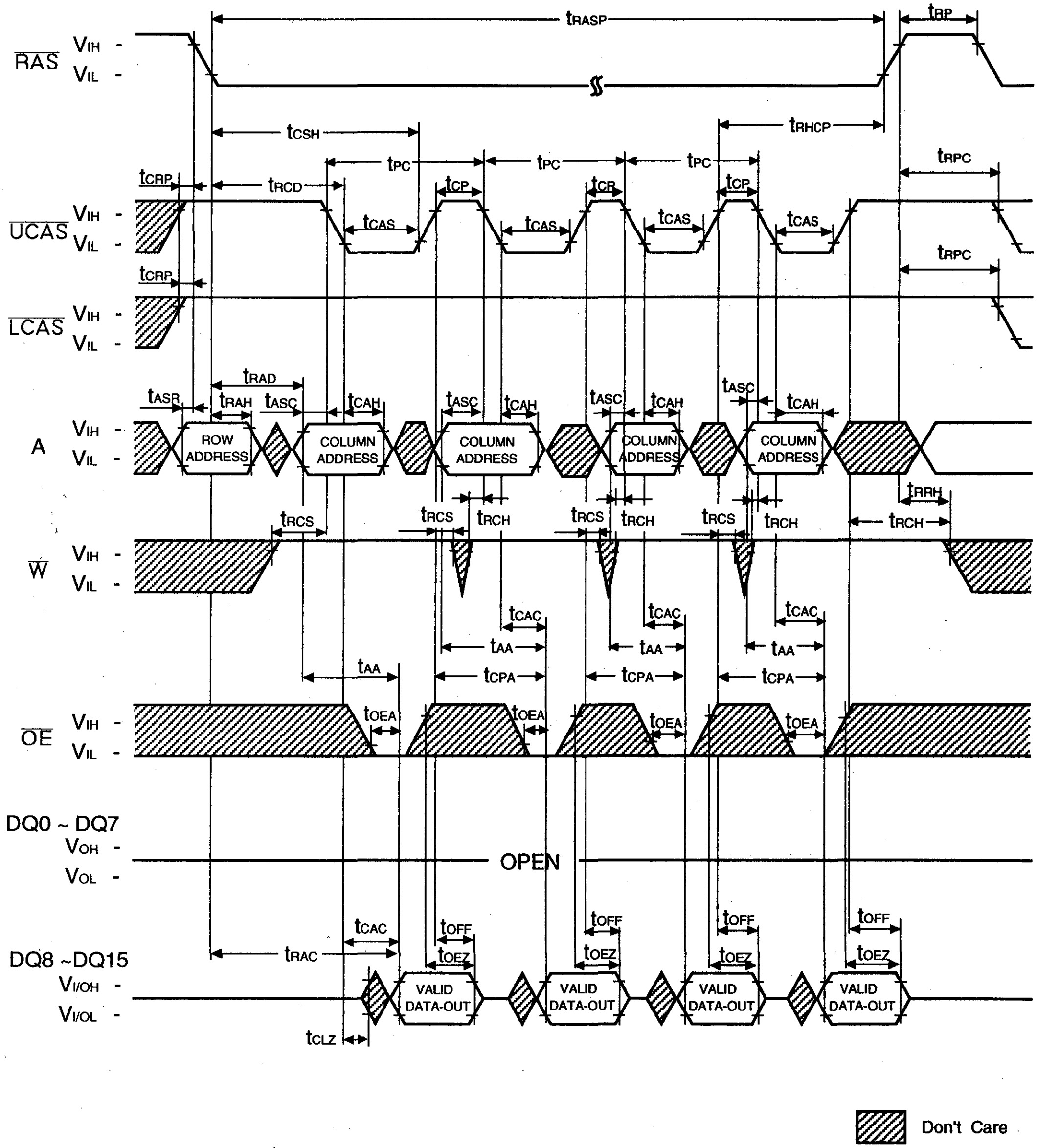
3

SAMSUNG ELECTRONICS

FAST PAGE MODE LOWER BYTE READ CYCLE



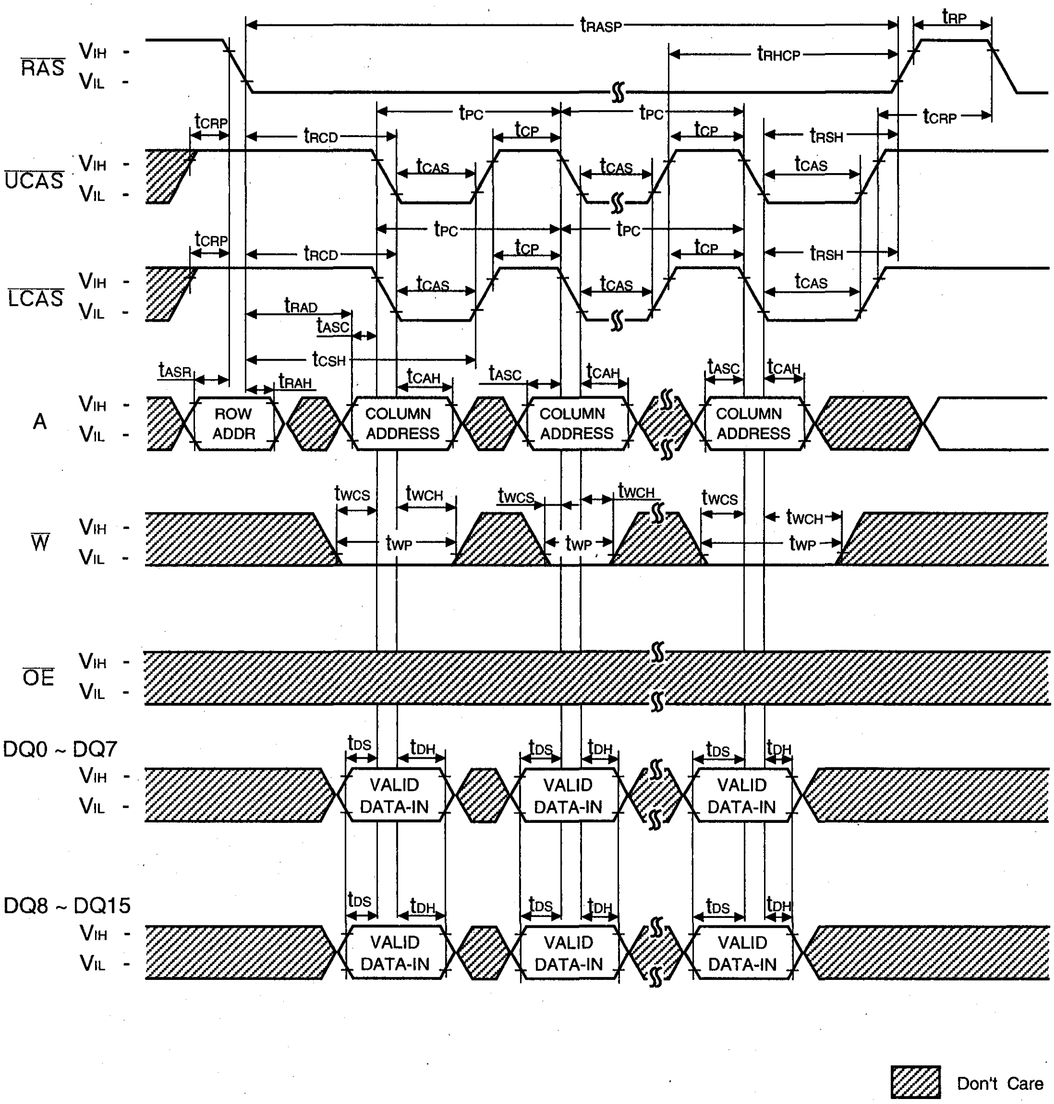
FAST PAGE MODE UPPER BYTE READ CYCLE



3

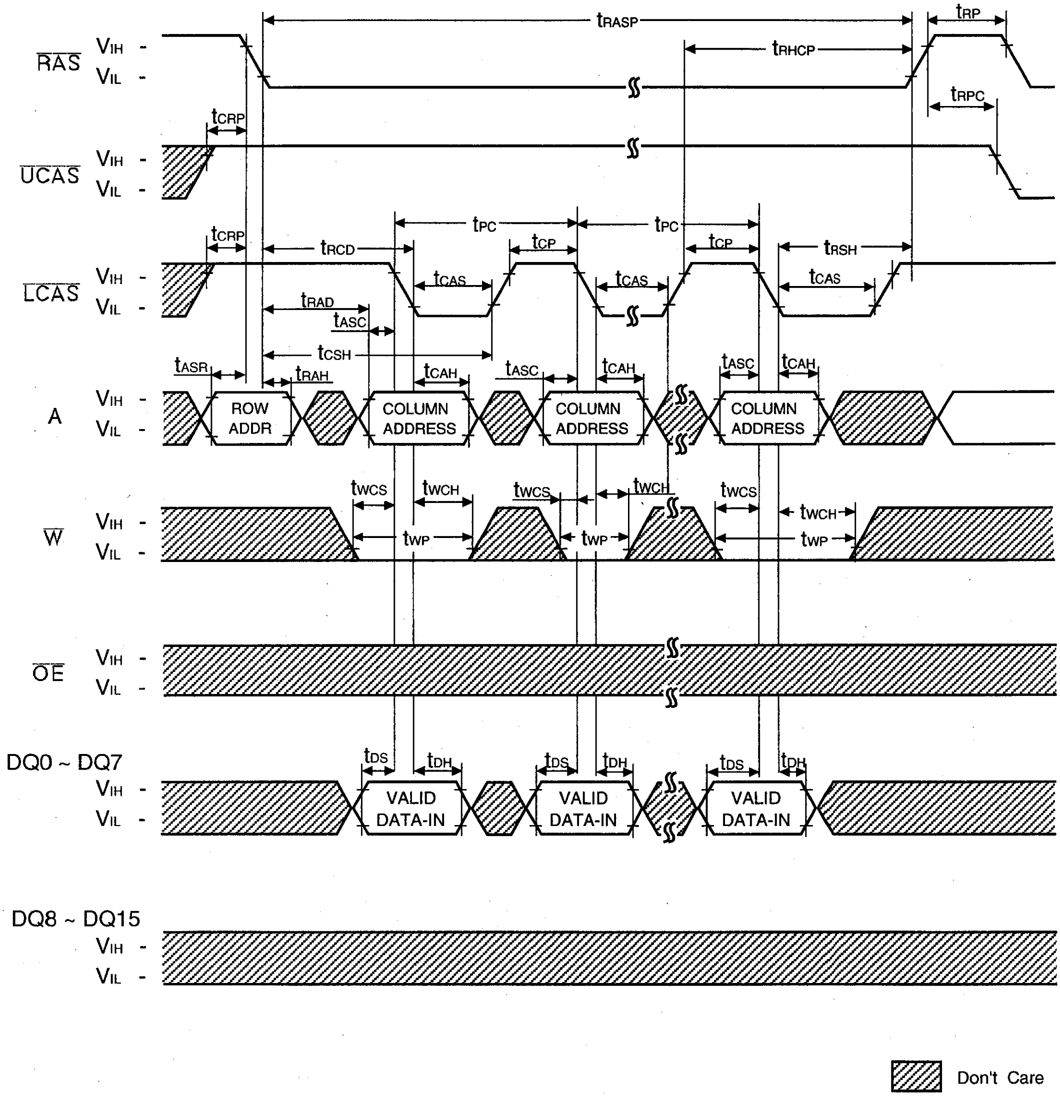
FAST PAGE MODE WORD WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = Open



FAST PAGE MODE LOWER BYTE WRITE CYCLE (EARLY WRITE)

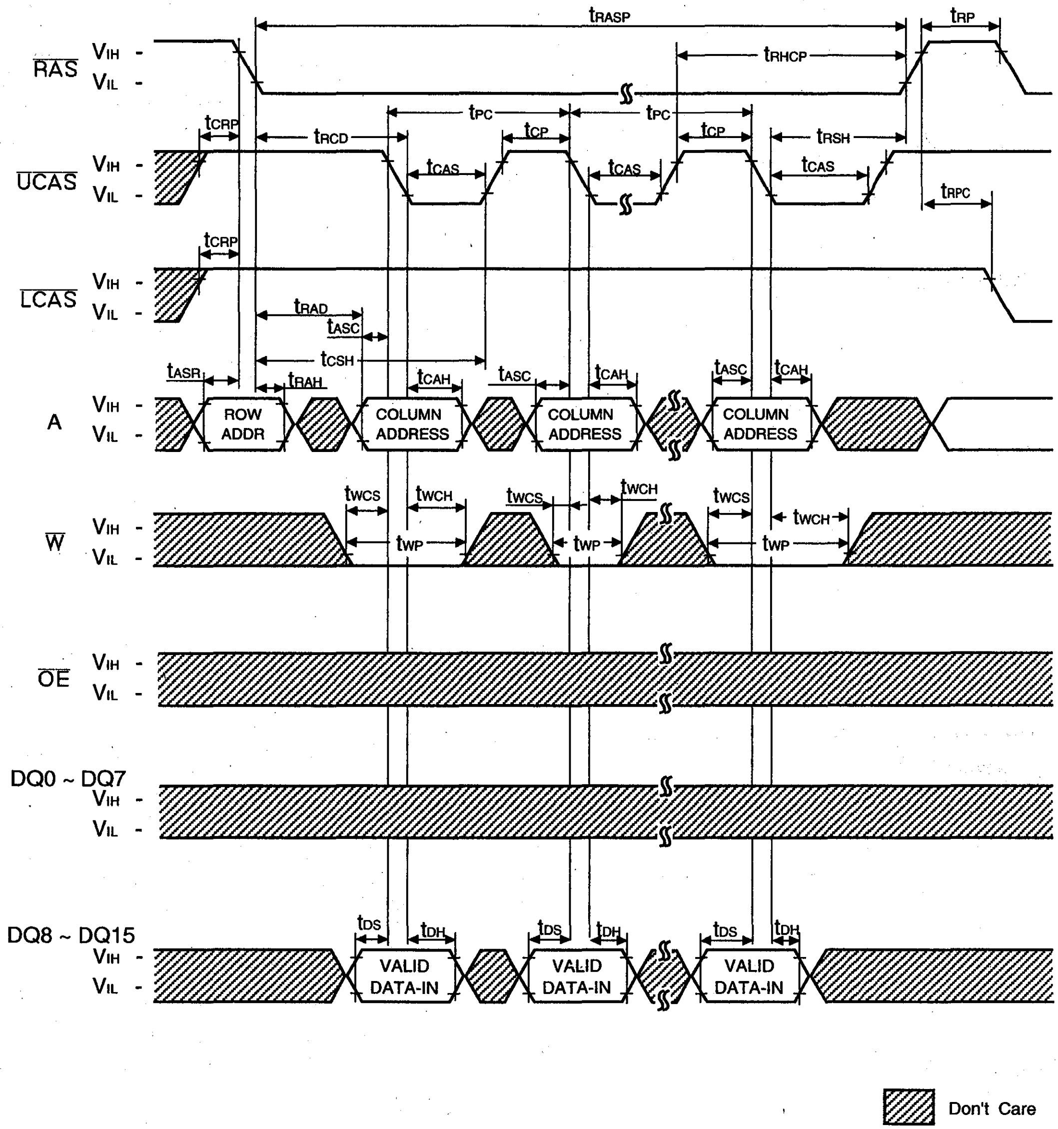
NOTE : D_{OUT} = Open



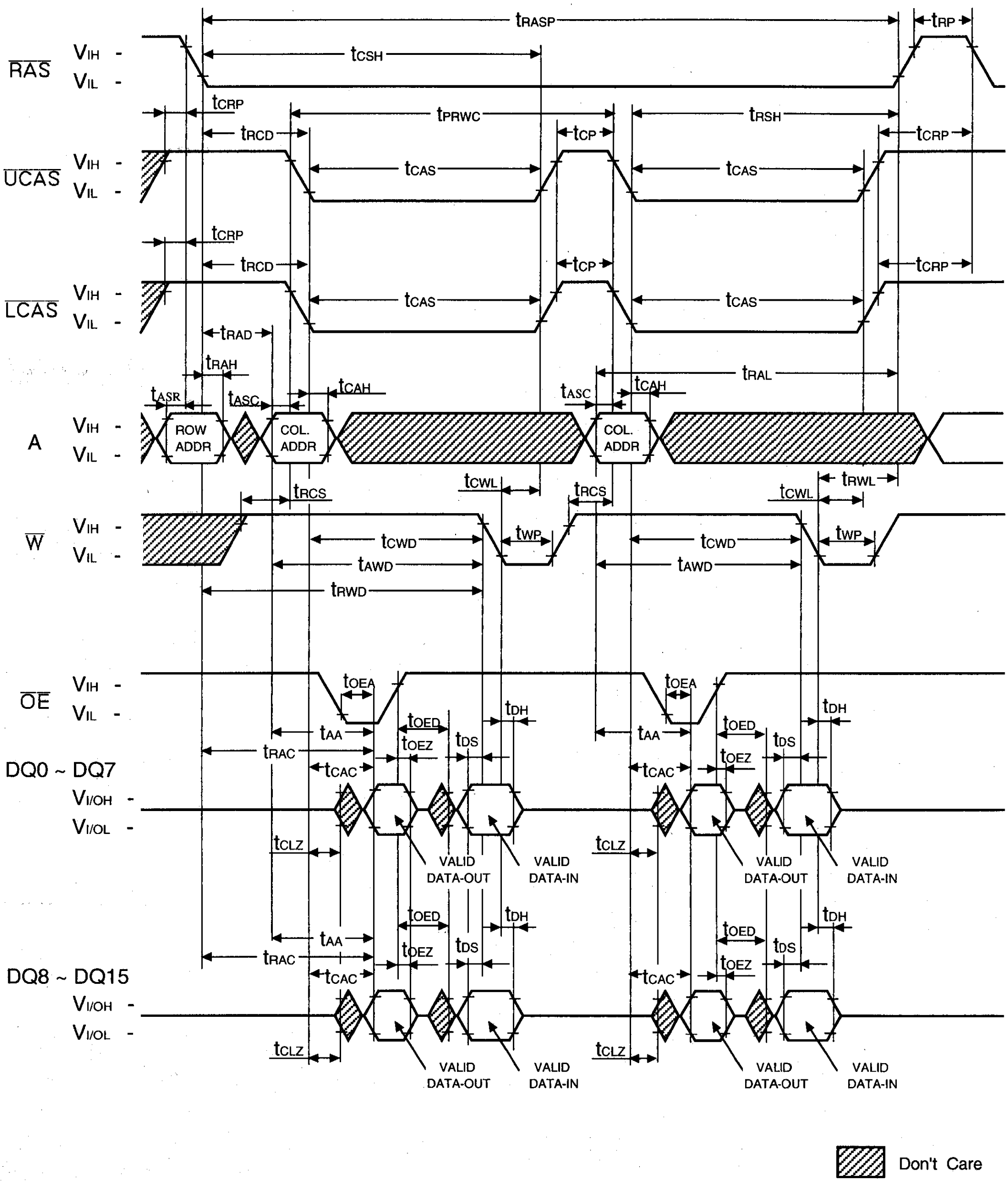
3

FAST PAGE MODE UPPER BYTE WRITE CYCLE (EARLY WRITE)

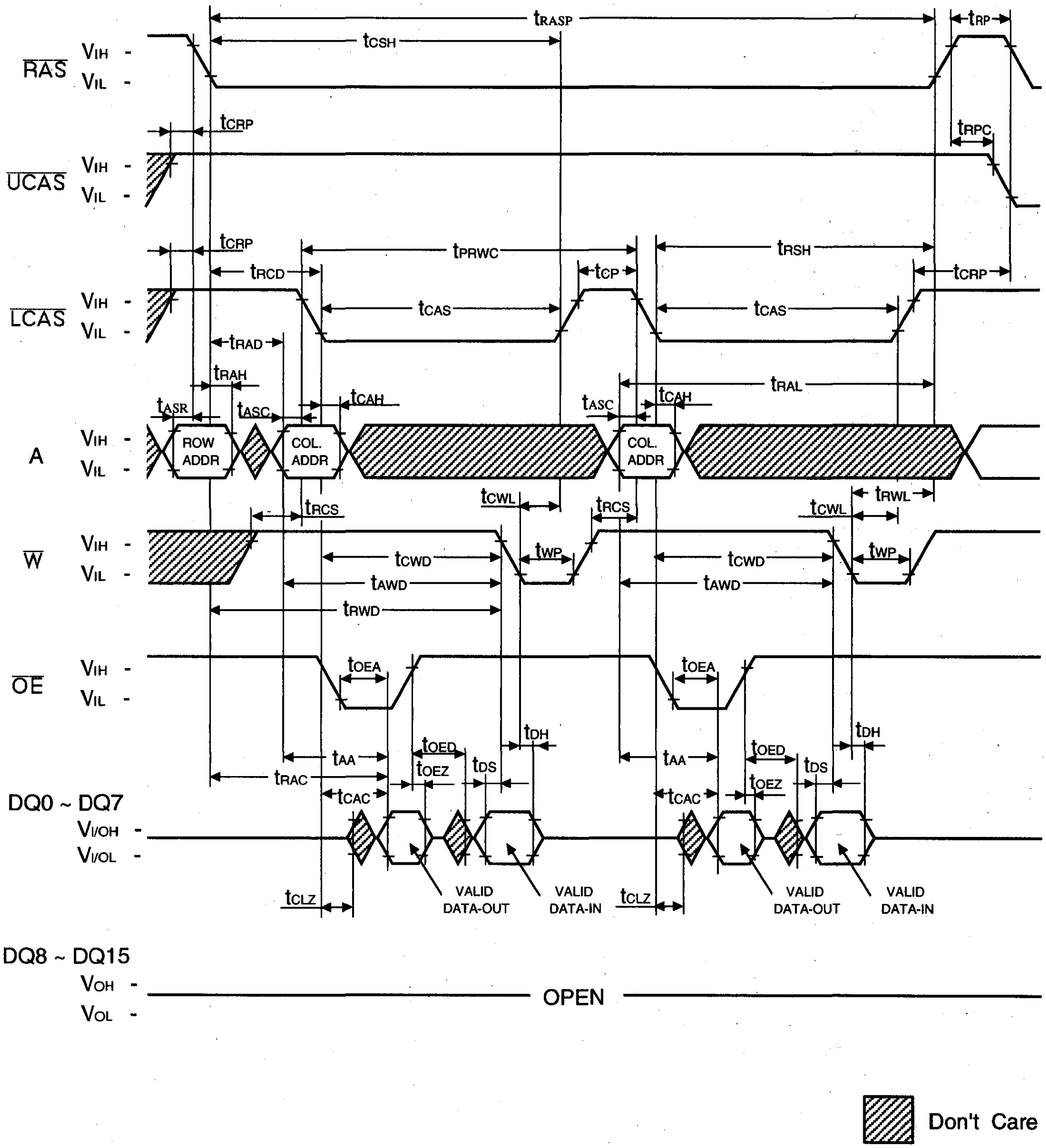
NOTE : D_{OUT} = Open



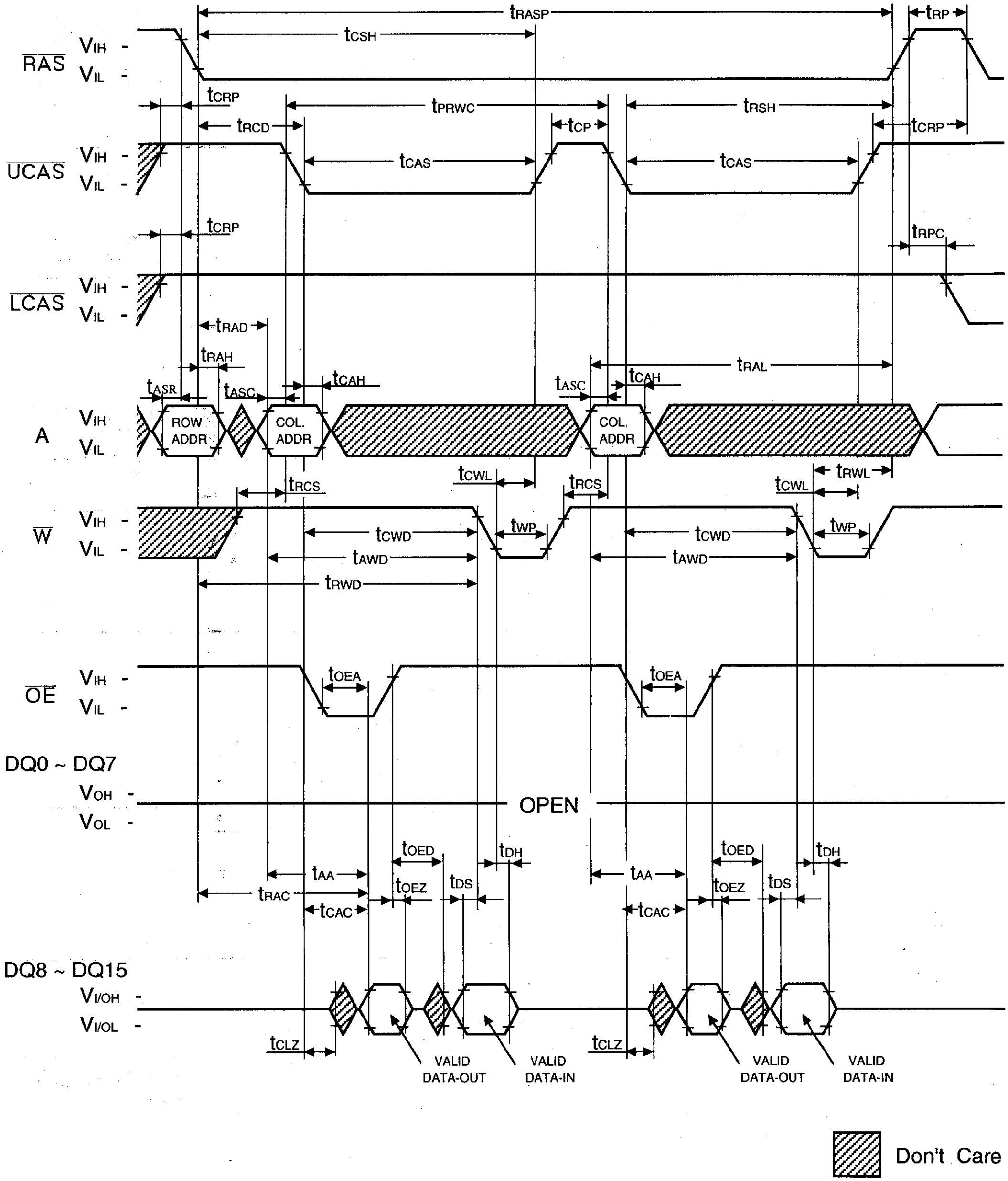
FAST PAGE MODE WORD READ-MODIFY-WRITE CYCLE



FAST PAGE MODE LOWER-BYTE-READ-MODIFY-WRITE CYCLE

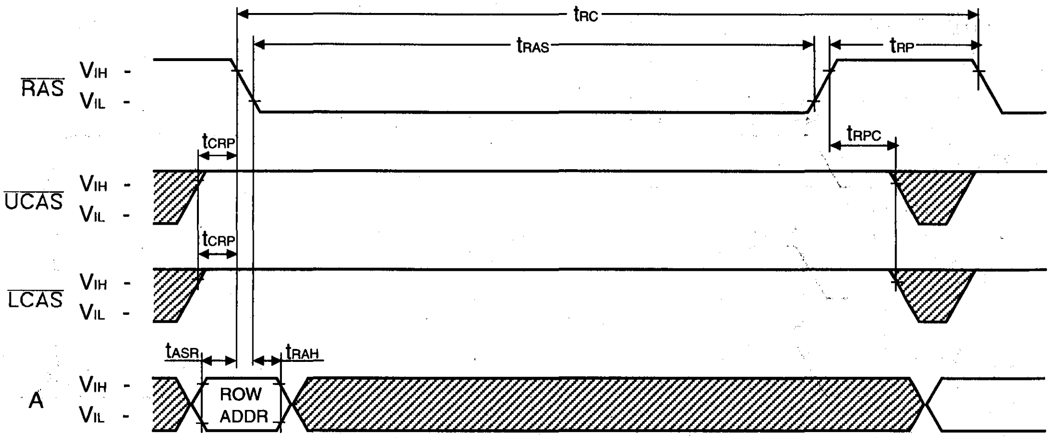


FAST PAGE MODE UPPER-BYTE-READ-MODIFY-WRITE CYCLE



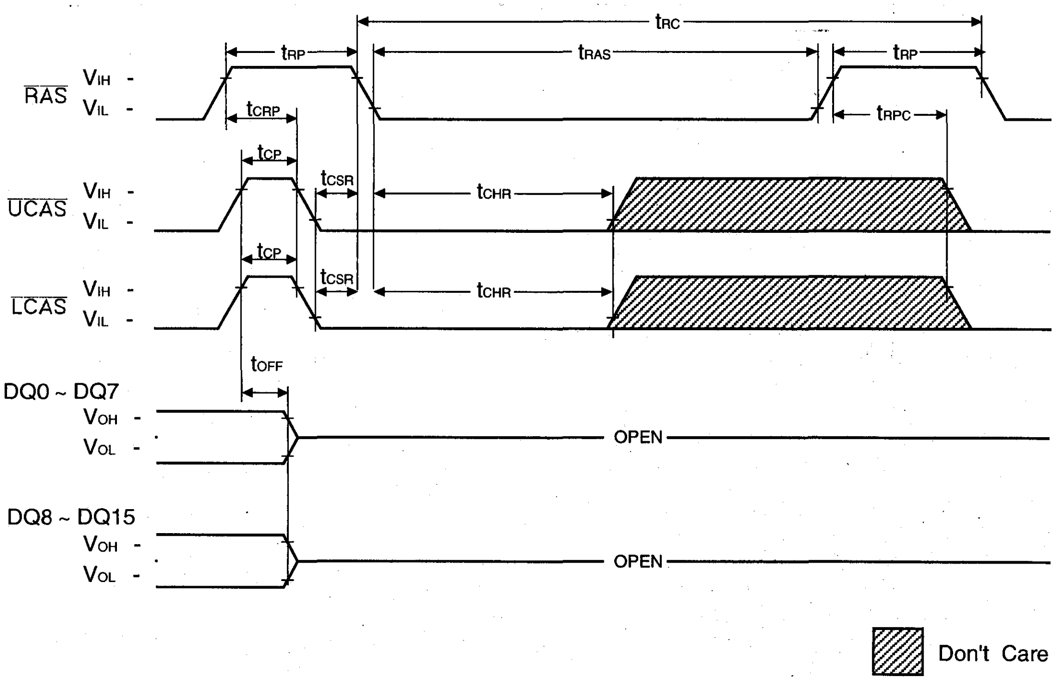
$\overline{RAS}$-ONLY REFRESH CYCLE

NOTE : $\overline{W}$, $\overline{OE}$, D_{IN} = Don't care
D_{OUT} = Open



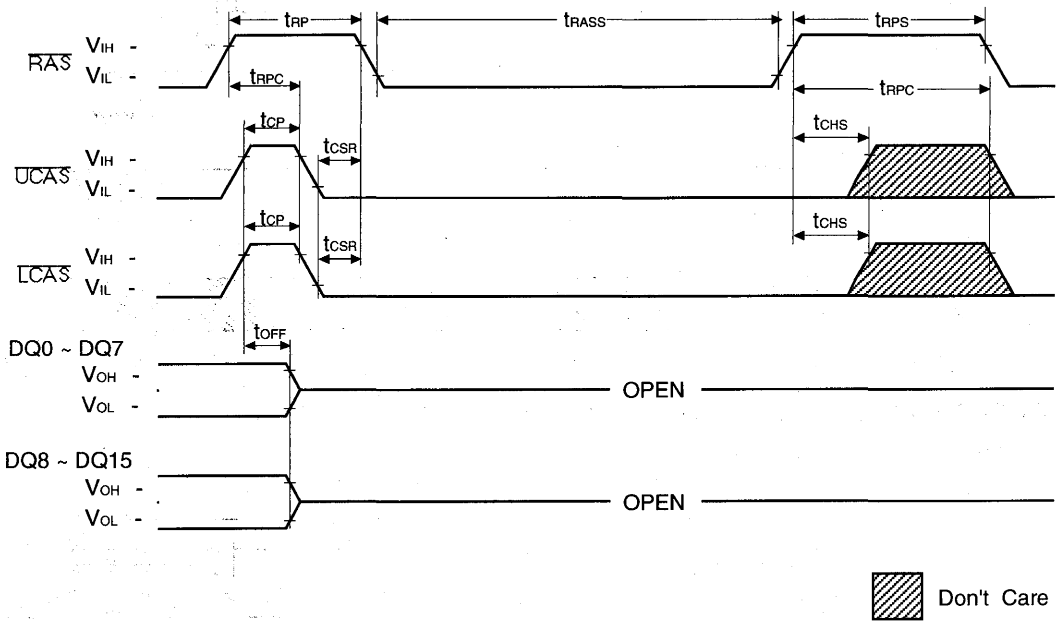
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE : $\overline{W}$, $\overline{OE}$, A = Don't Care



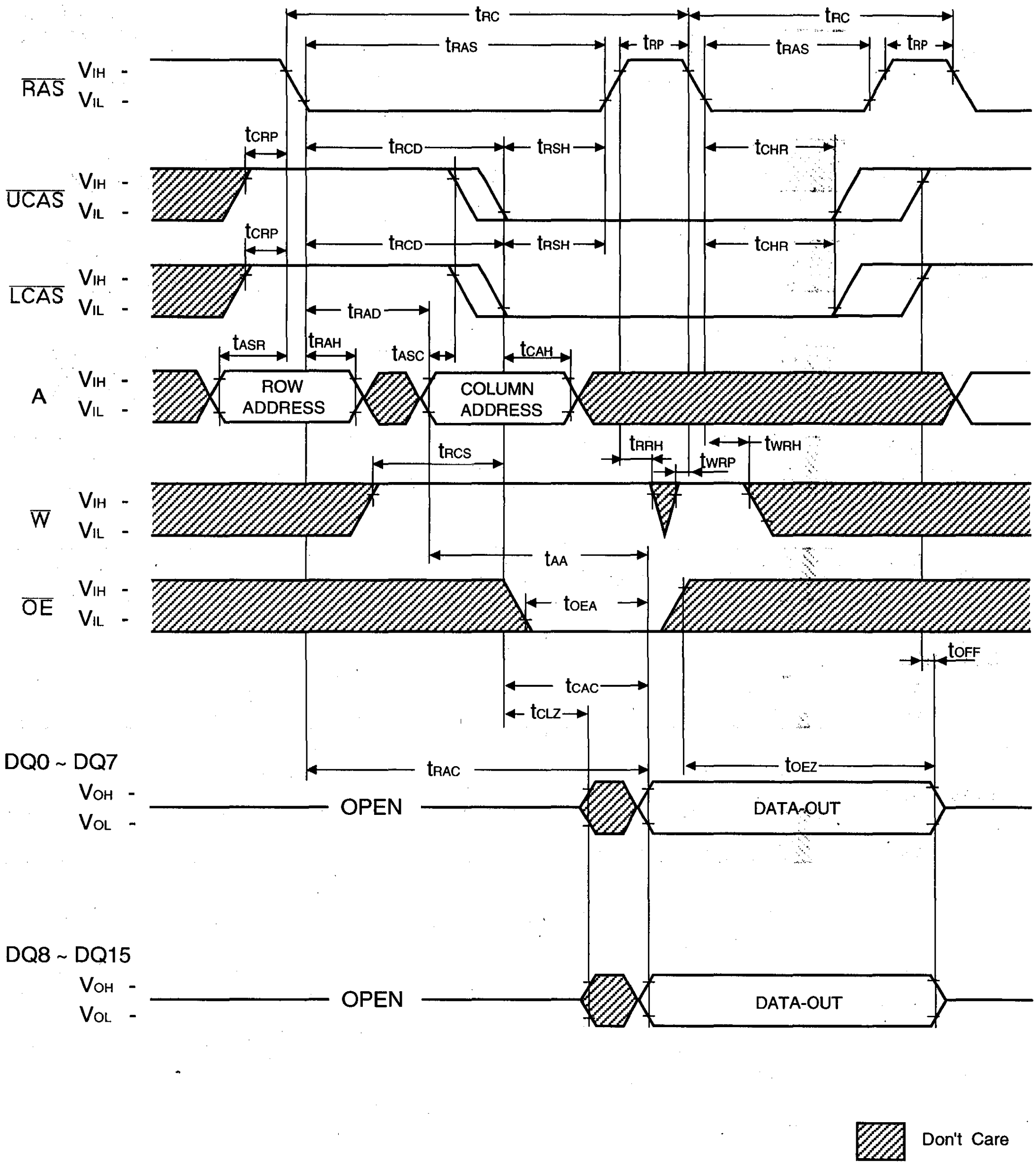
$\overline{CAS}$-BEFORE-$\overline{RAS}$ SELF REFRESH CYCLE

NOTE : $\overline{W}$, $\overline{OE}$, A = Don't Care



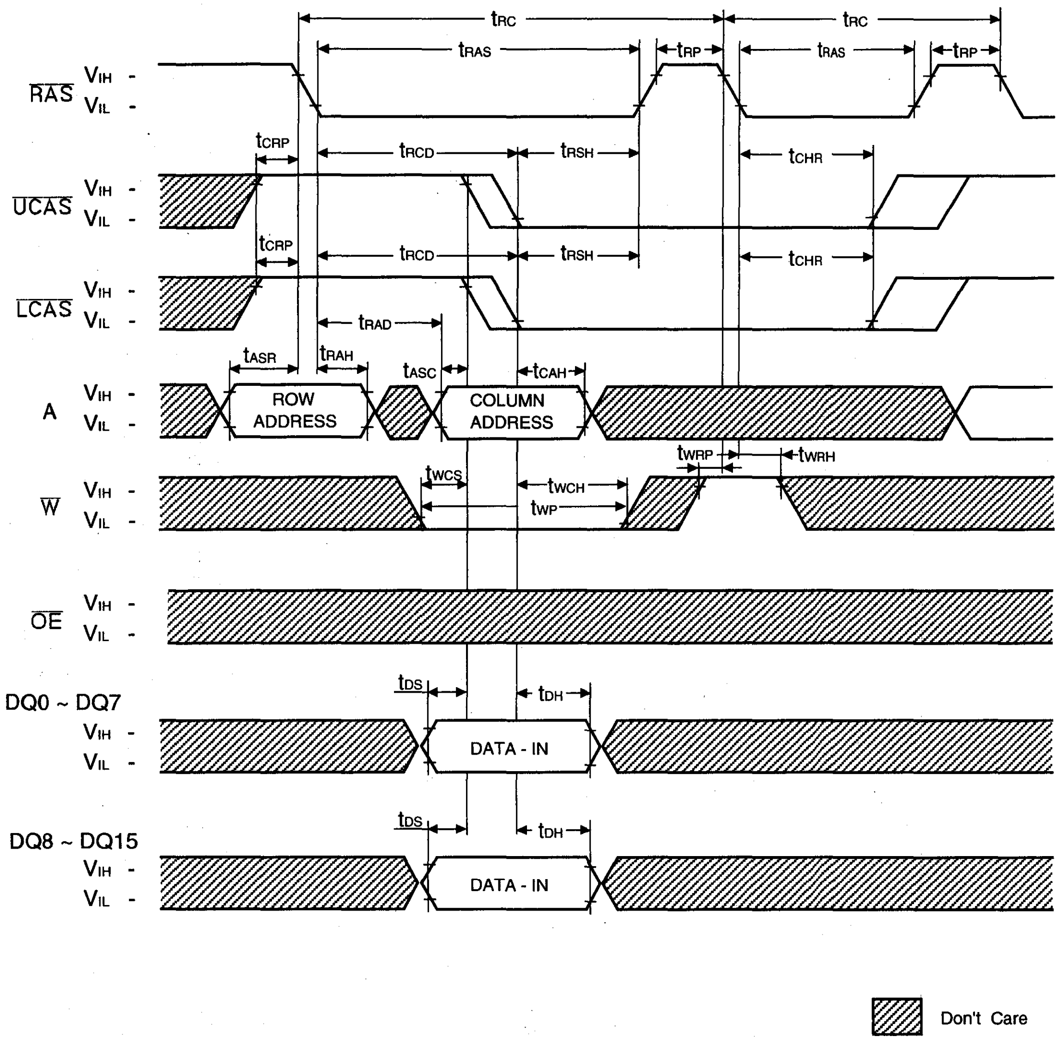
3

HIDDEN REFRESH CYCLE (READ)

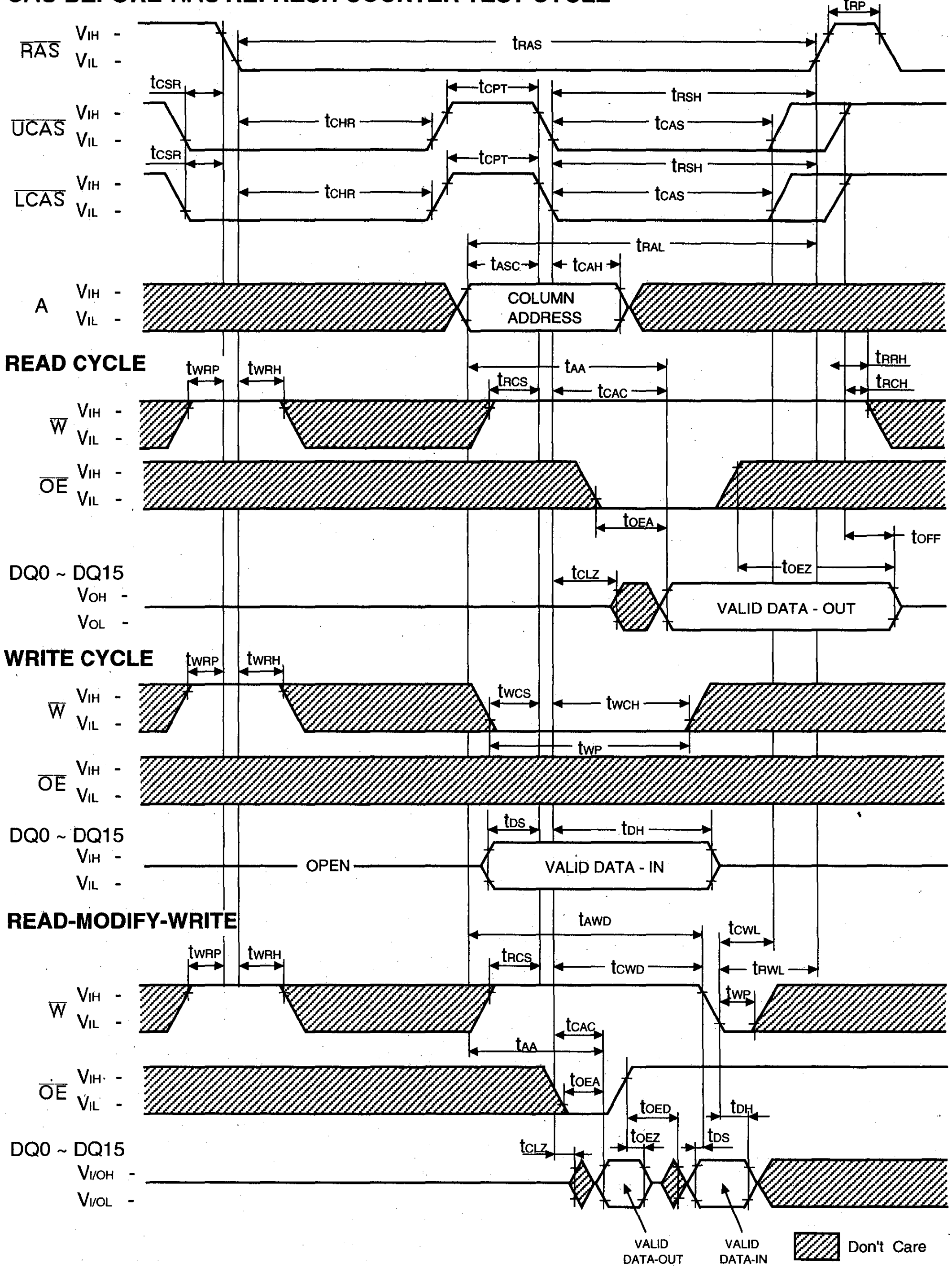


HIDDEN REFRESH CYCLE (WRITE)

NOTE : DOUT = OPEN



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE

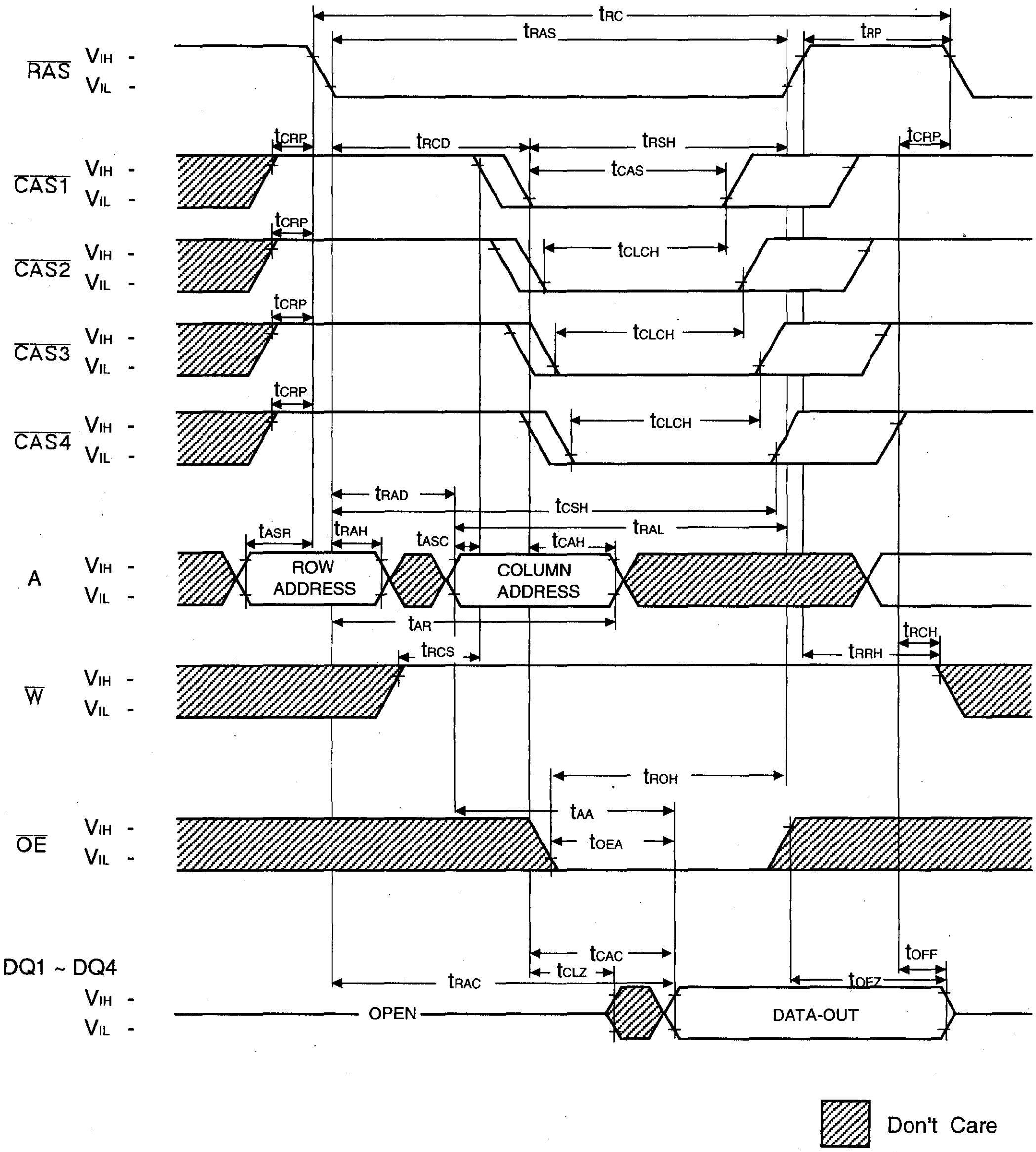


Fast Page Mode, Quad $\overline{CAS}$ Device

TIMING DIAGRAM

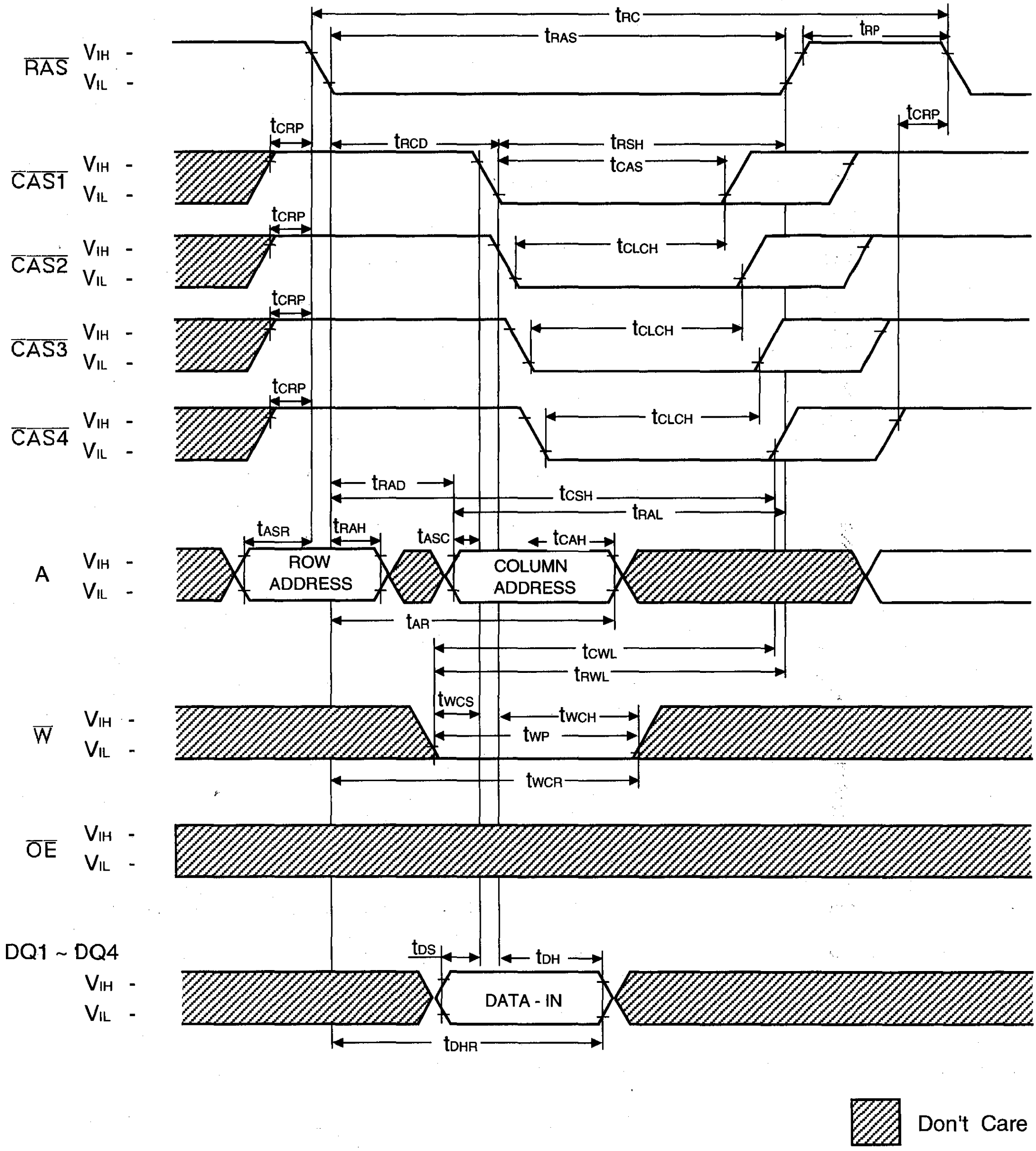
READ CYCLE

NOTE : D_{IN} = OPEN



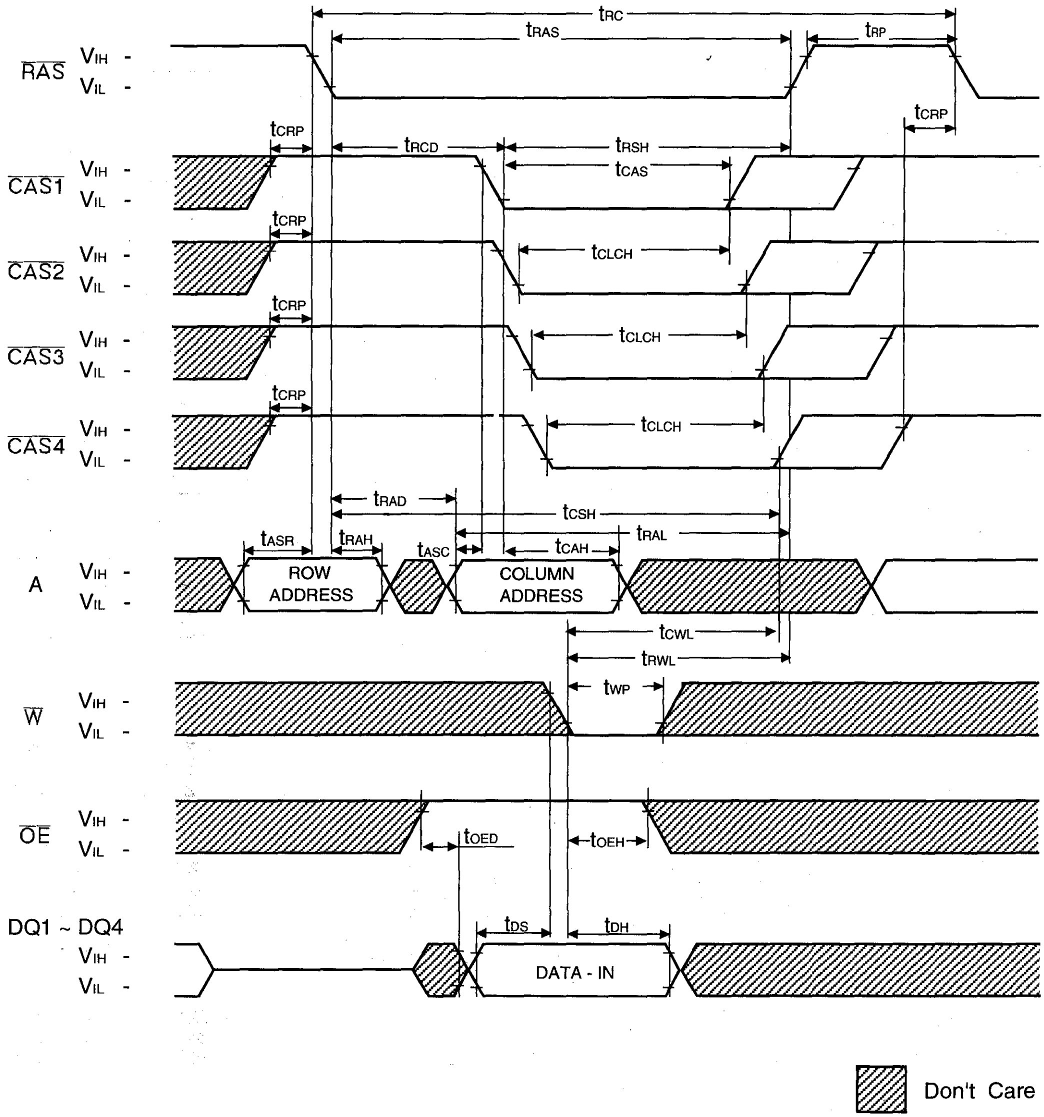
TIMING DIAGRAM

WRITE CYCLE (EARLY WRITE)



TIMING DIAGRAM

WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

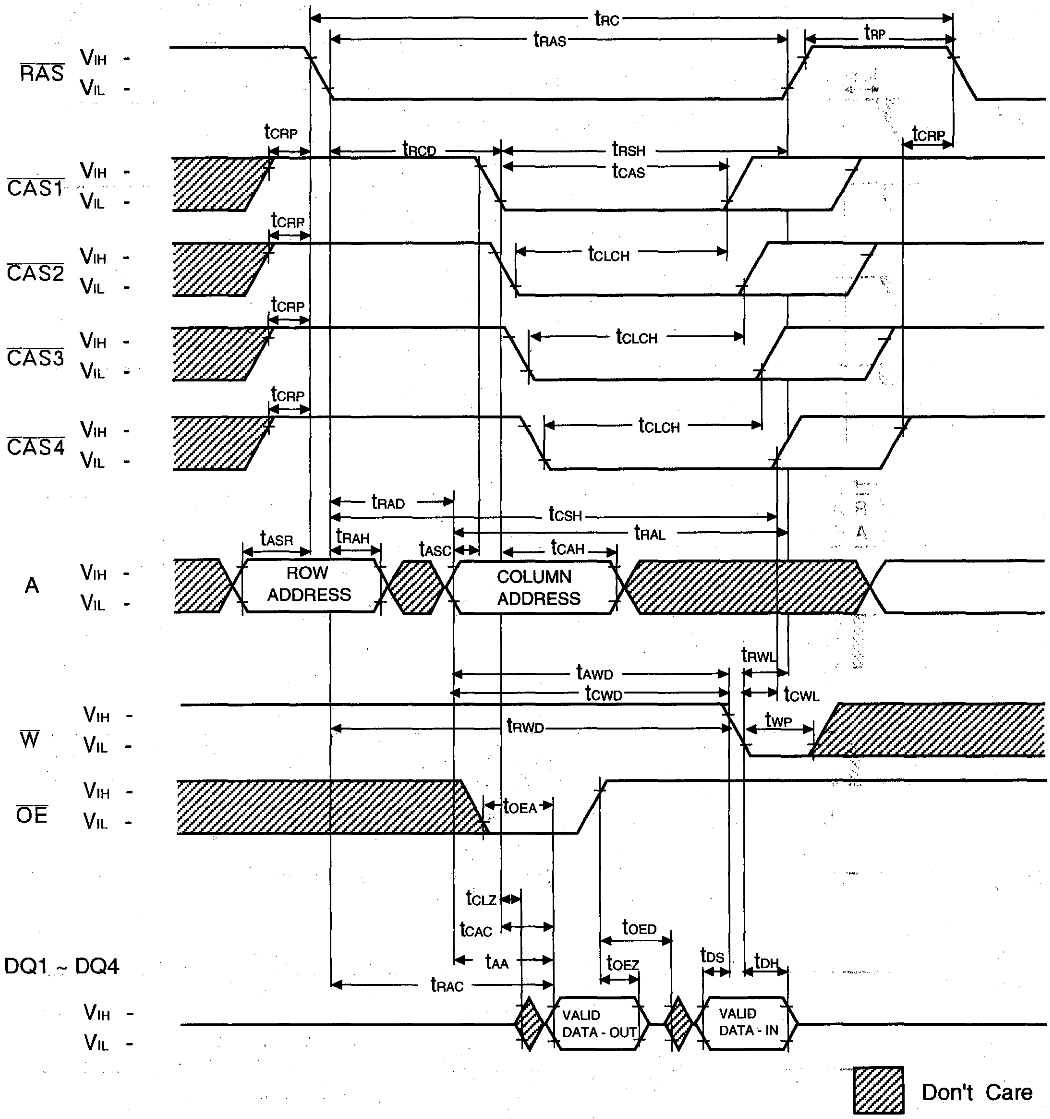


3

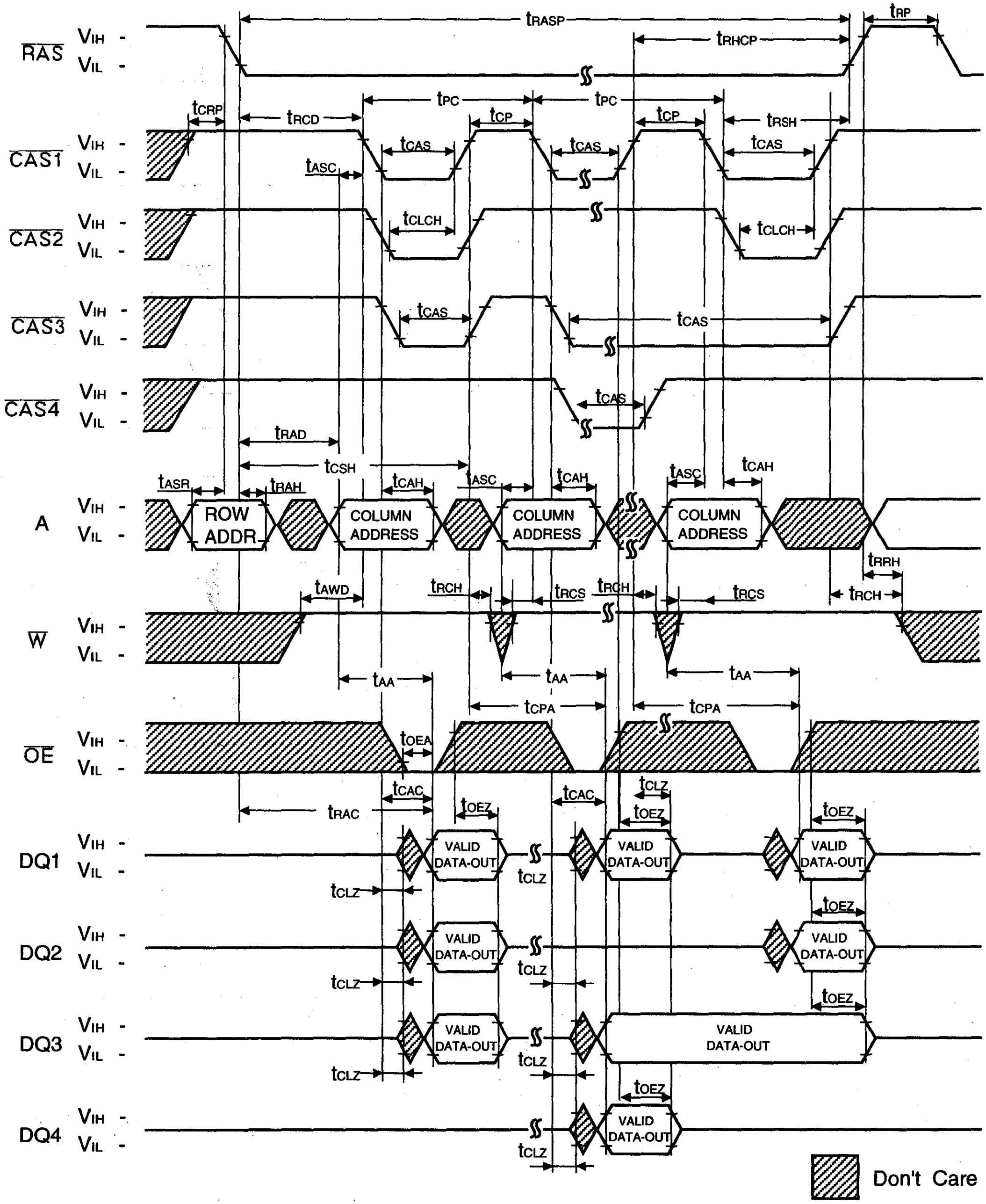
SAMSUNG ELECTRONICS

TIMING DIAGRAM

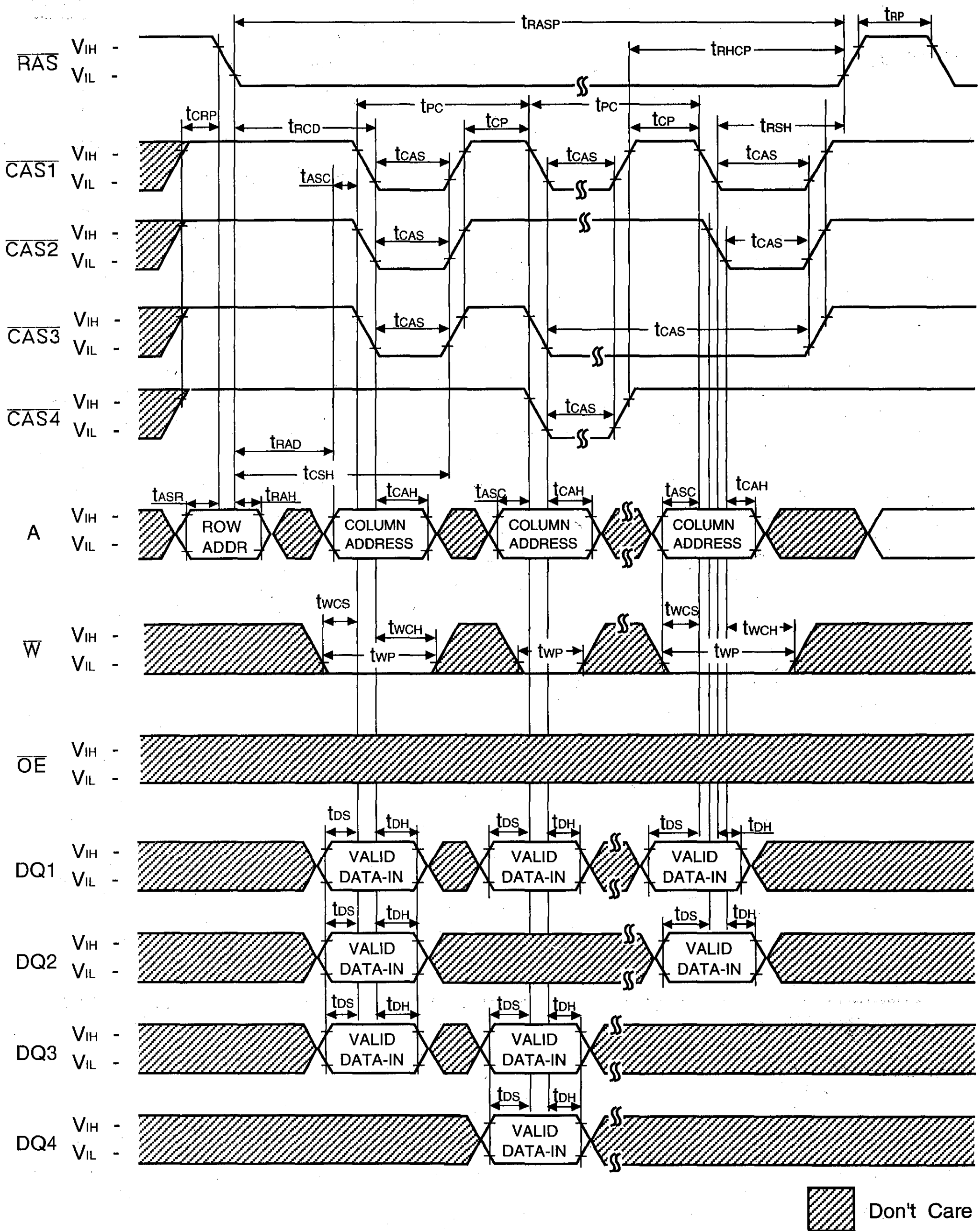
READ - MODIFY - WRITE CYCLE



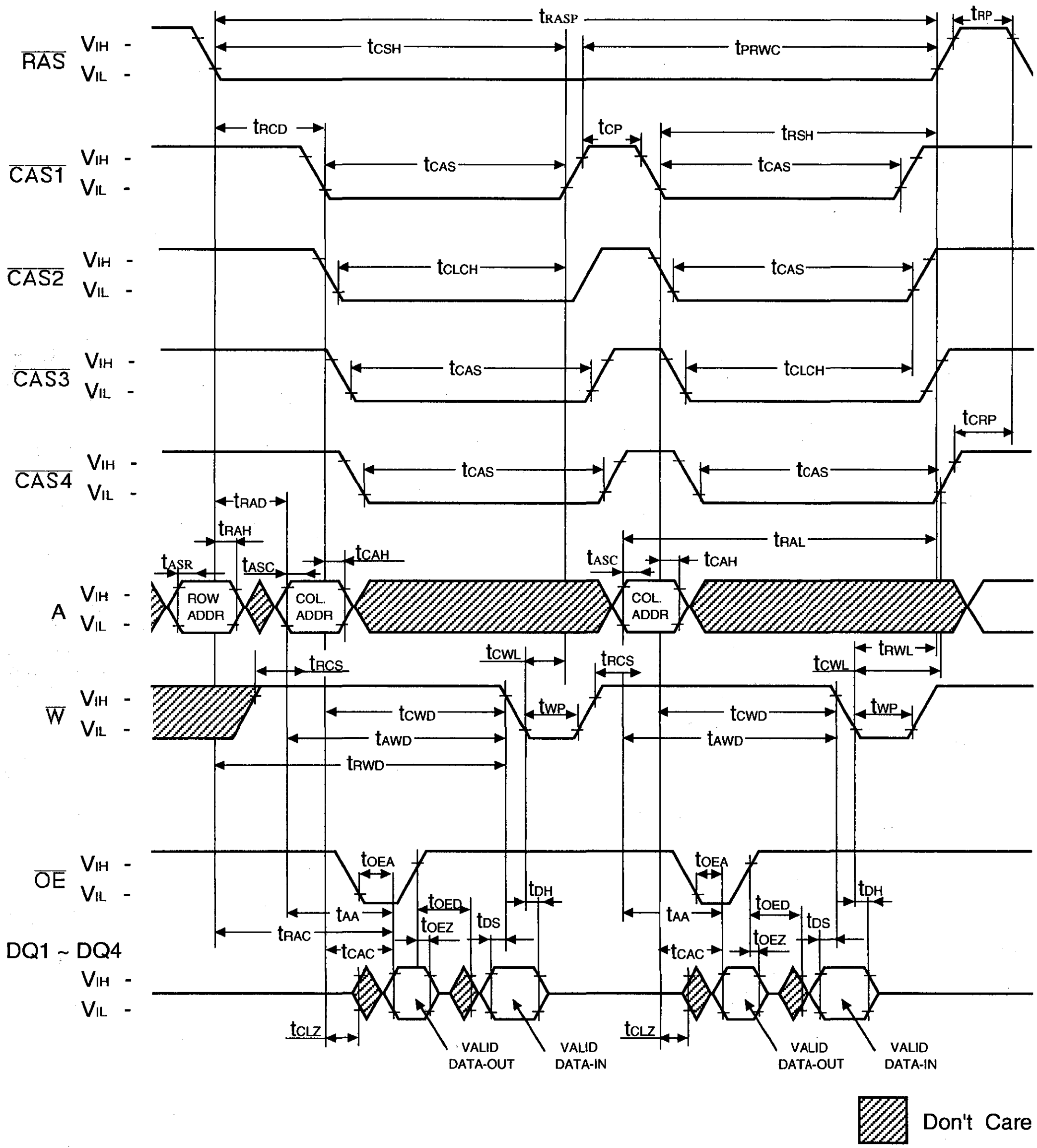
FAST PAGE MODE READ CYCLE



FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



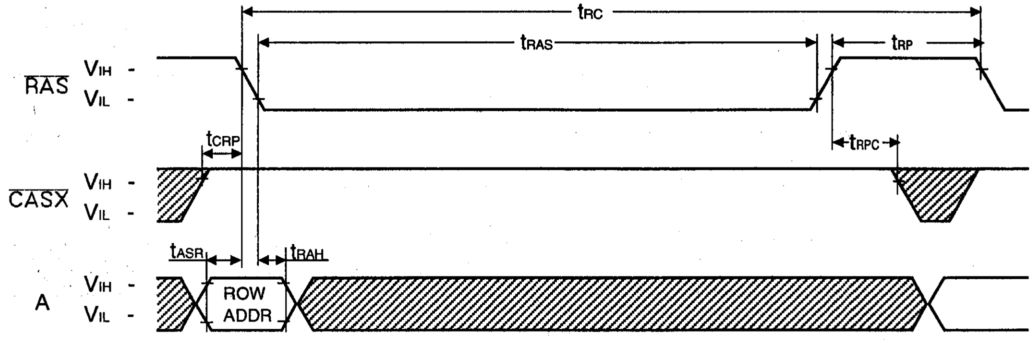
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



3

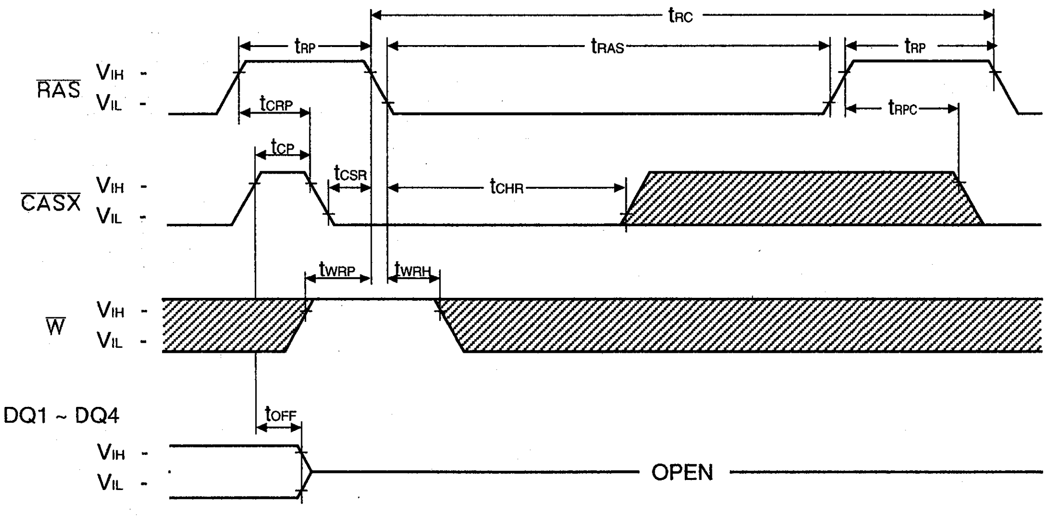
$\overline{\text{RAS}}$-ONLY REFRESH CYCLE

NOTE : $\overline{\text{W}}$, $\overline{\text{OE}}$, D_{IN} = Don't care
D_{OUT} = Open



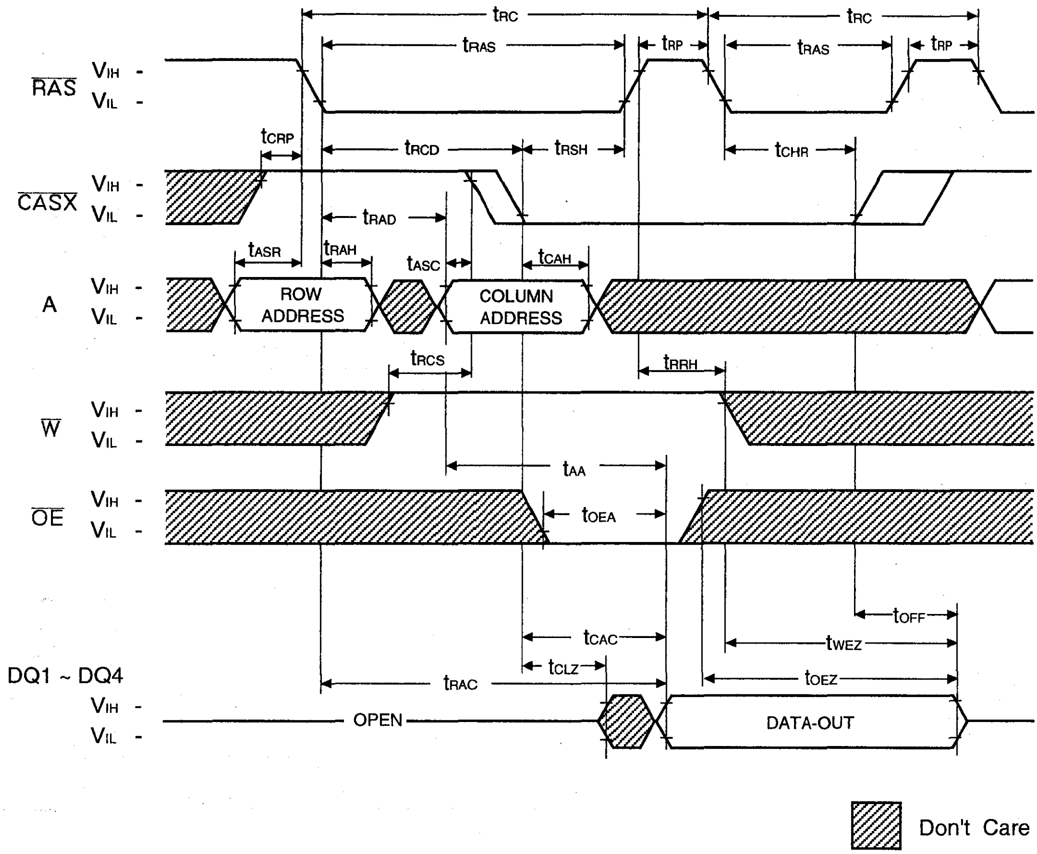
$\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH CYCLE

NOTE : $\overline{\text{W}}$, $\overline{\text{OE}}$, A = Don't Care



Don't Care

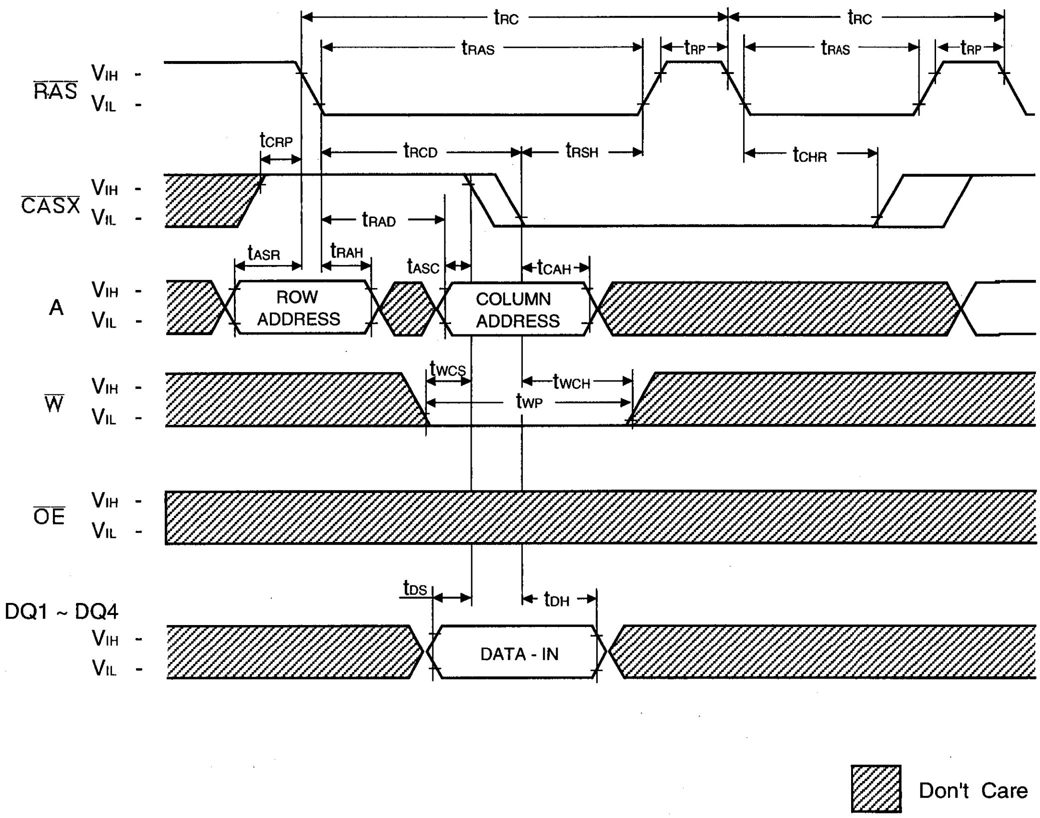
HIDDEN REFRESH CYCLE (READ)



3

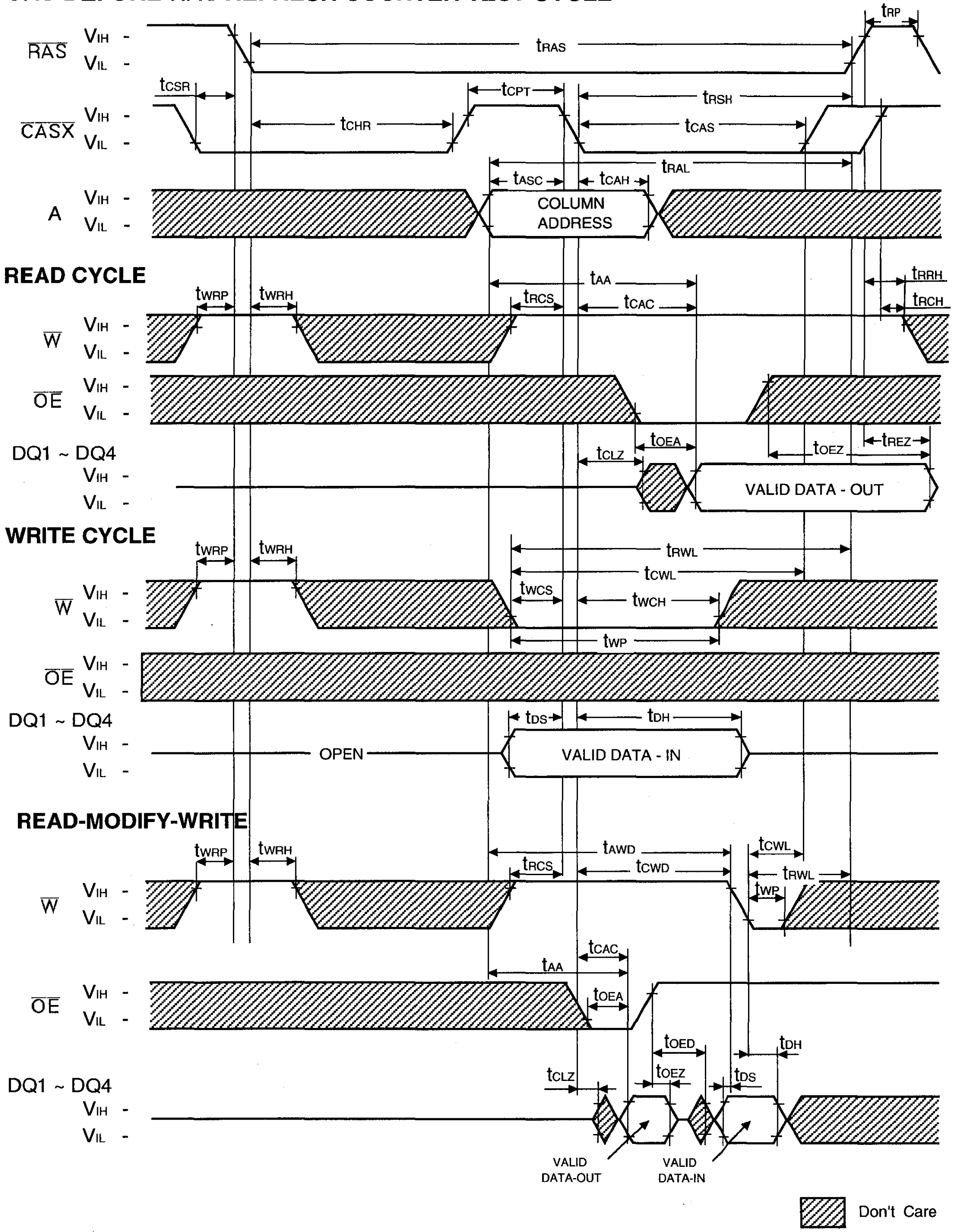
HIDDEN REFRESH CYCLE (WRITE)

NOTE : D_{OUT} = OPEN



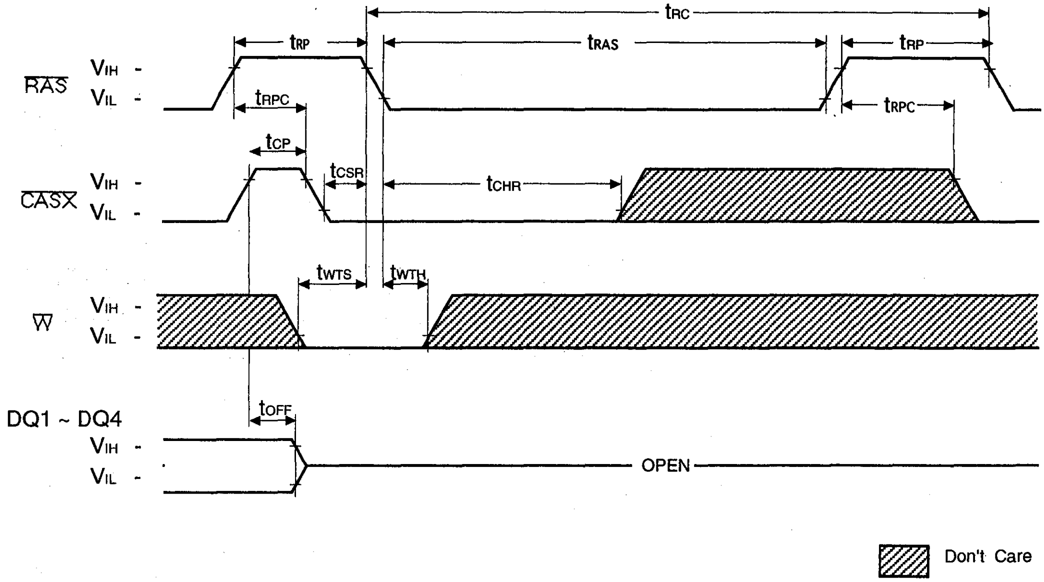
3

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



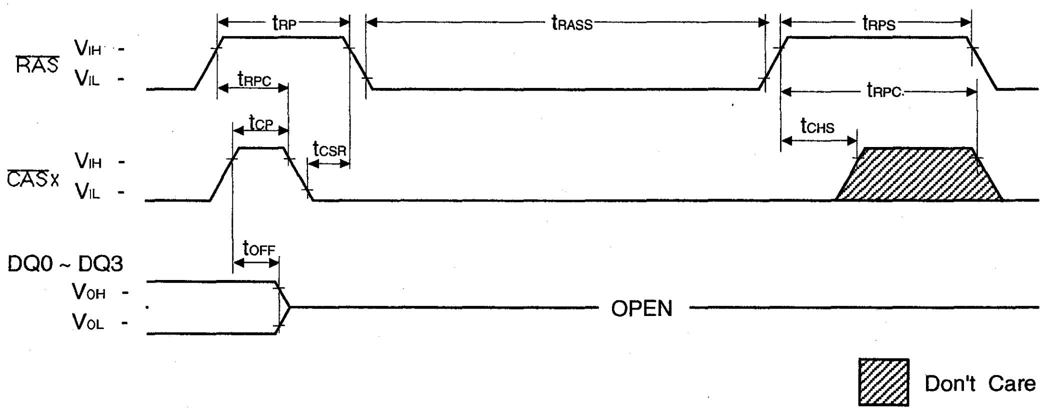
TEST MODE IN CYCLE

NOTE : $\overline{OE}$, A = Don't Care



$\overline{CAS}$-BEFORE-$\overline{RAS}$ SELF REFRESH CYCLE

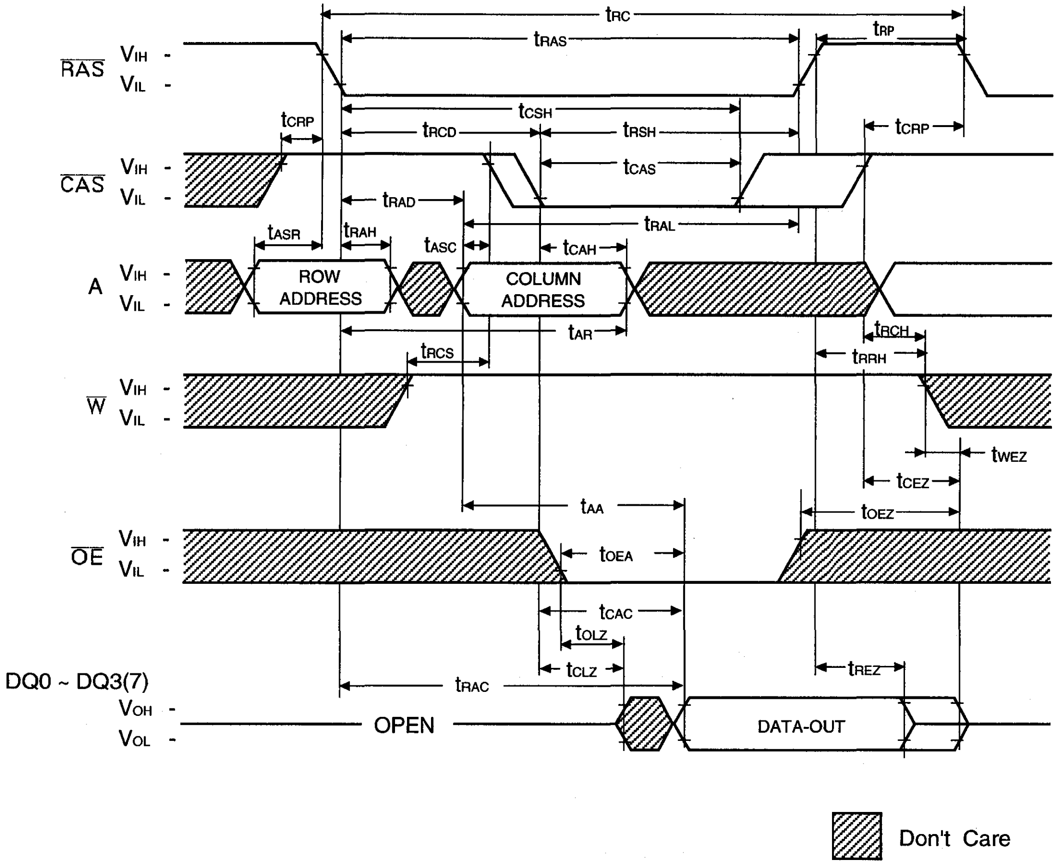
NOTE : $\overline{W}$, $\overline{OE}$, A = Don't Care



EDO Mode, x4 and x8 Device

TIMING DIAGRAM

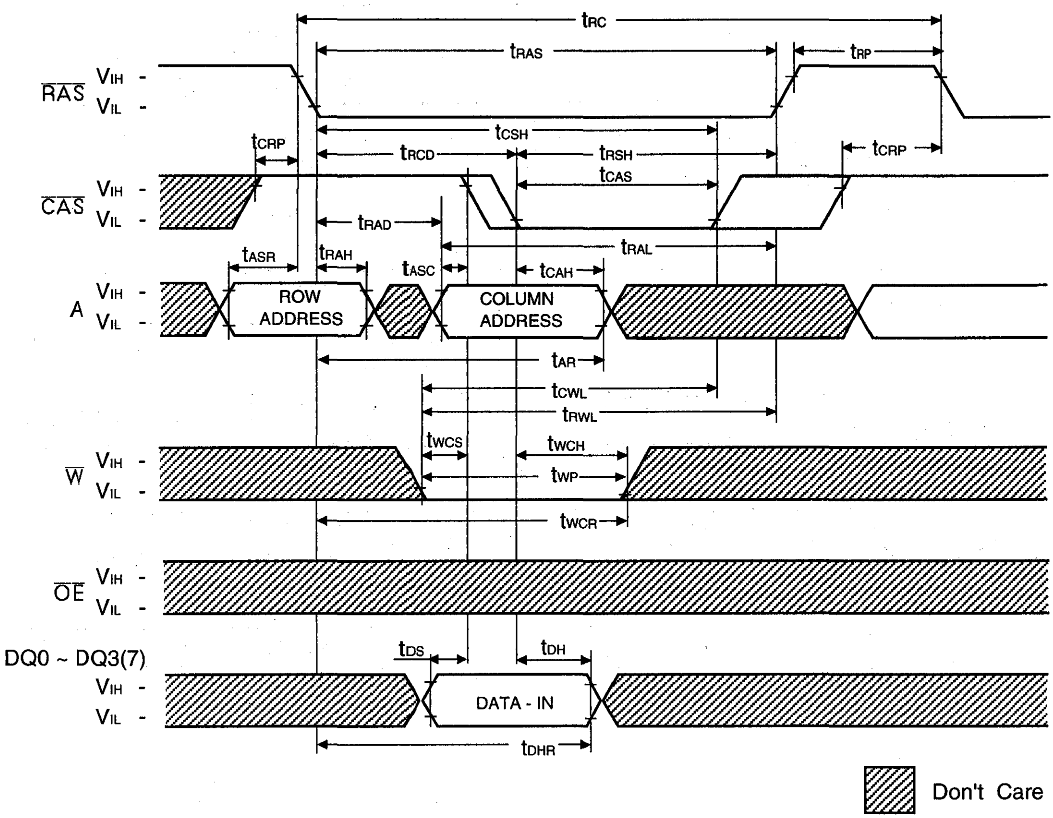
READ CYCLE



3

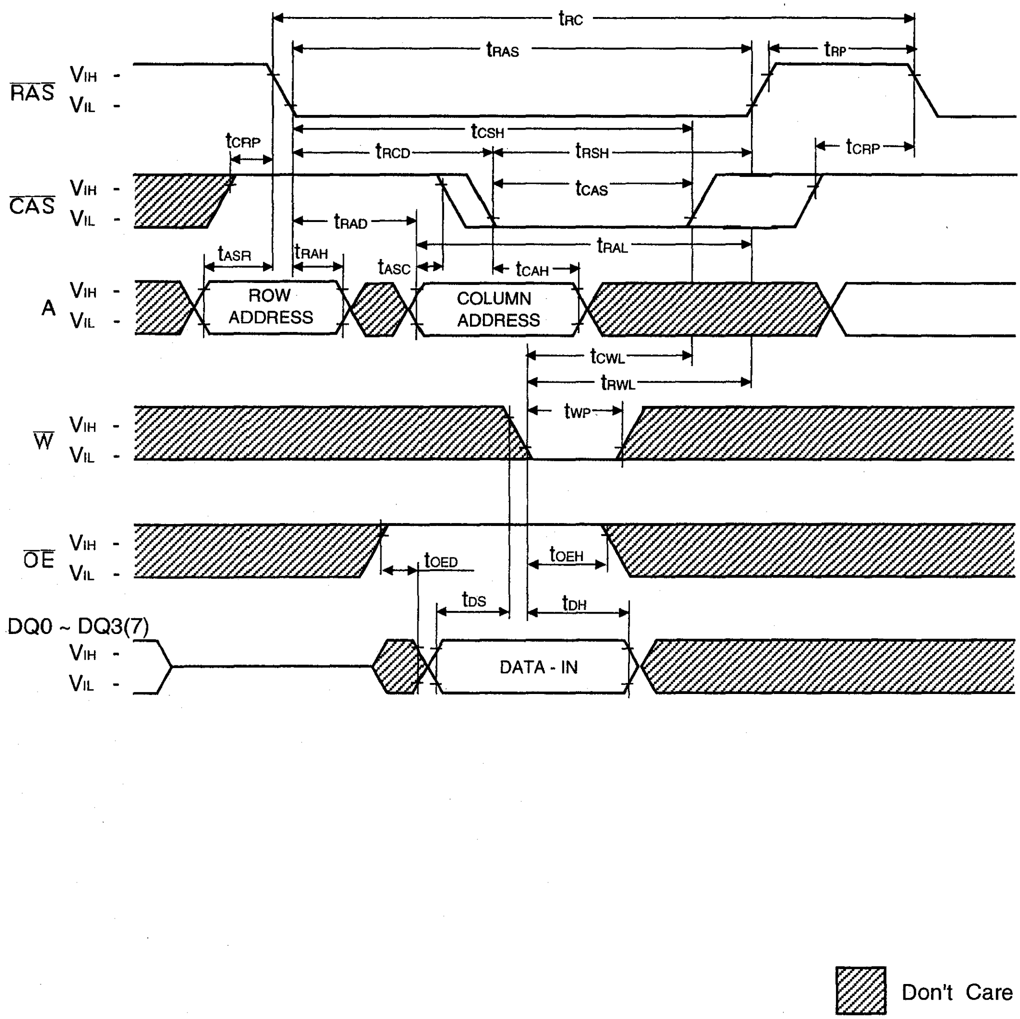
WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = OPEN

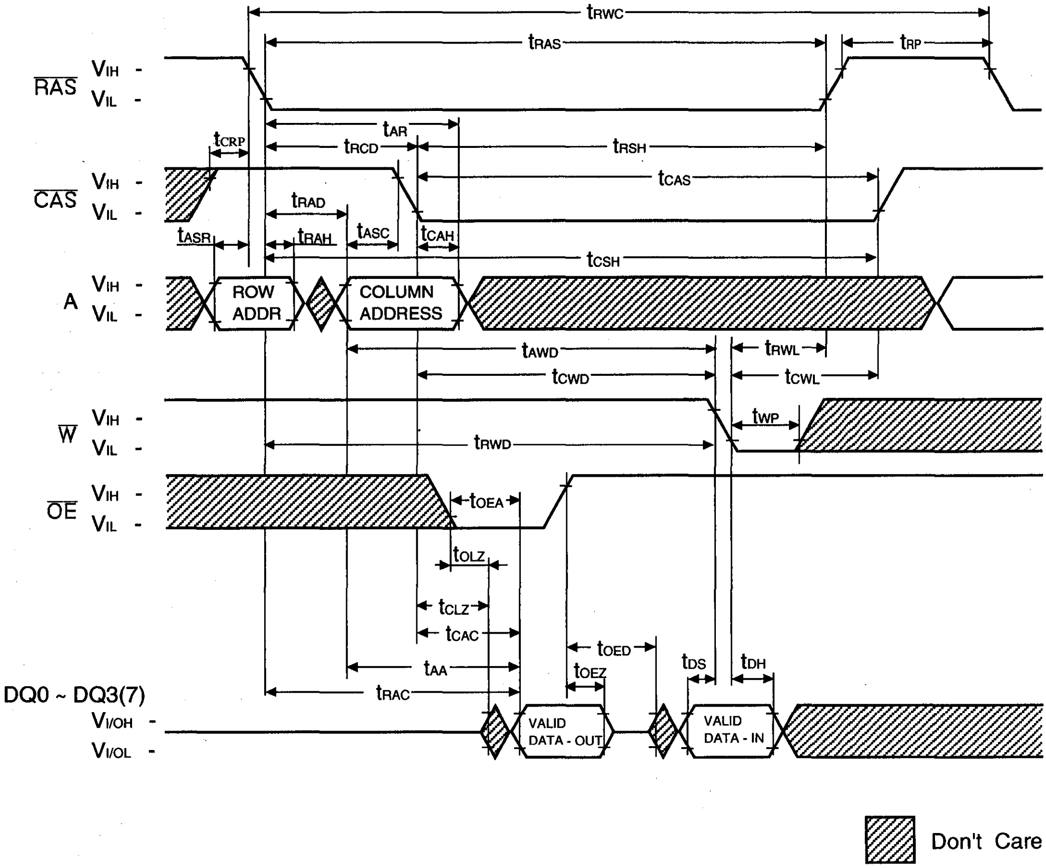


WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

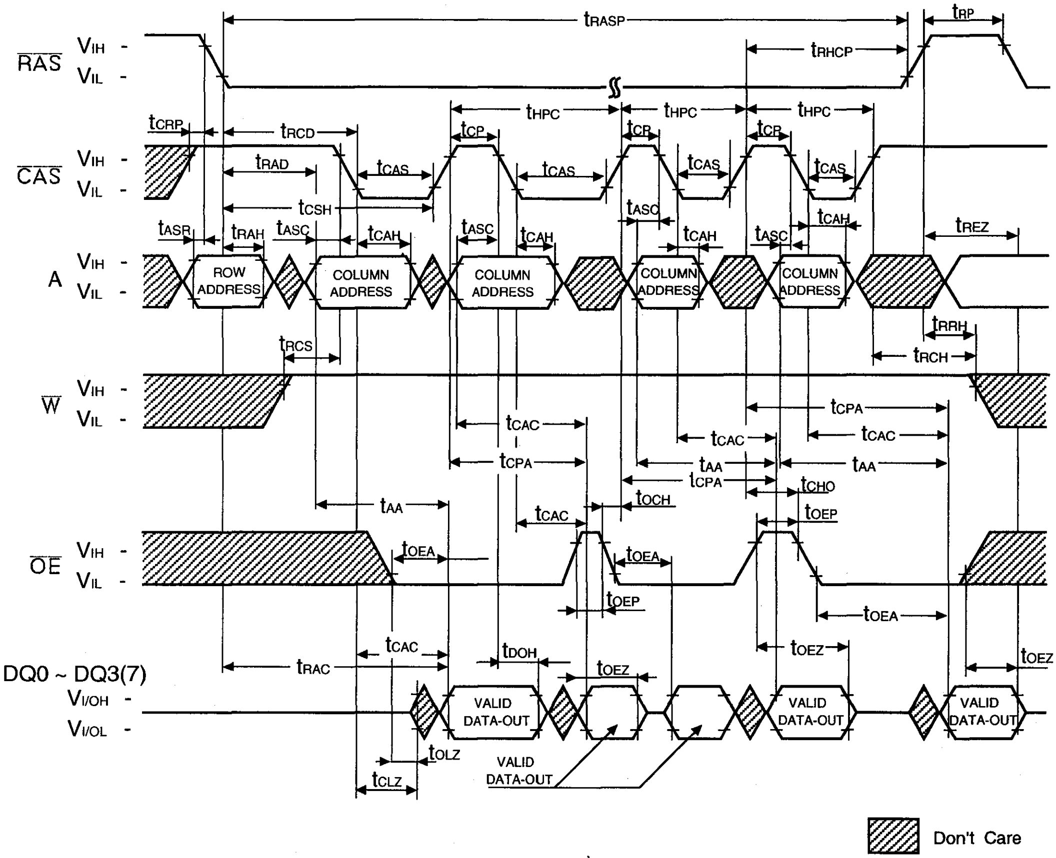
NOTE : DOUT = OPEN



READ - MODIFY - WRITE CYCLE

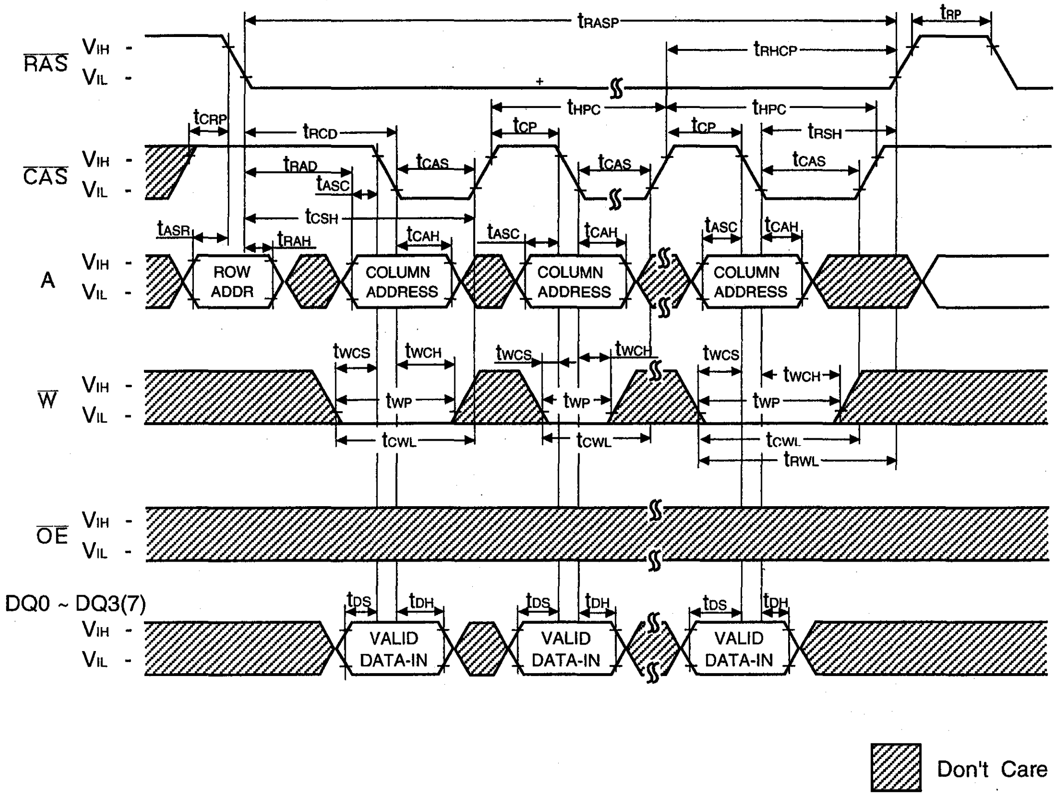


HYPER PAGE READ CYCLE

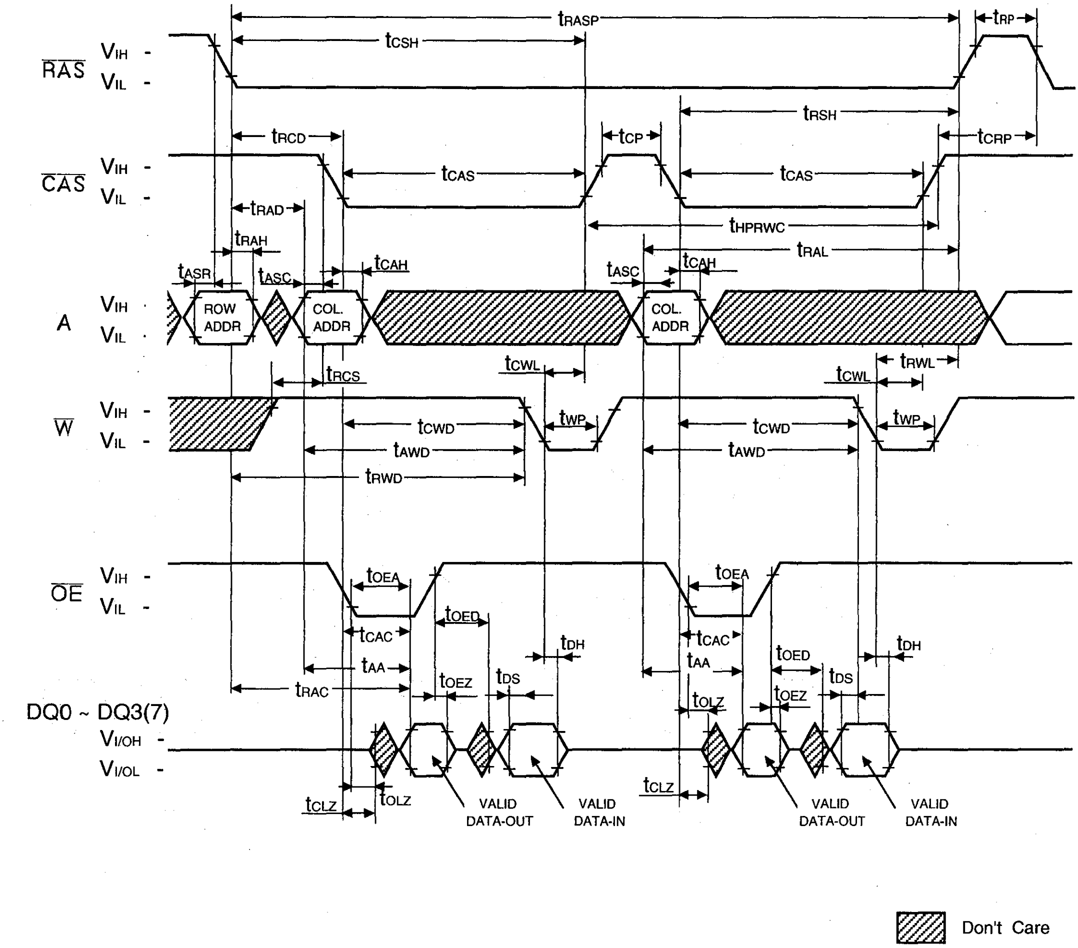


HYPER PAGE WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = Open

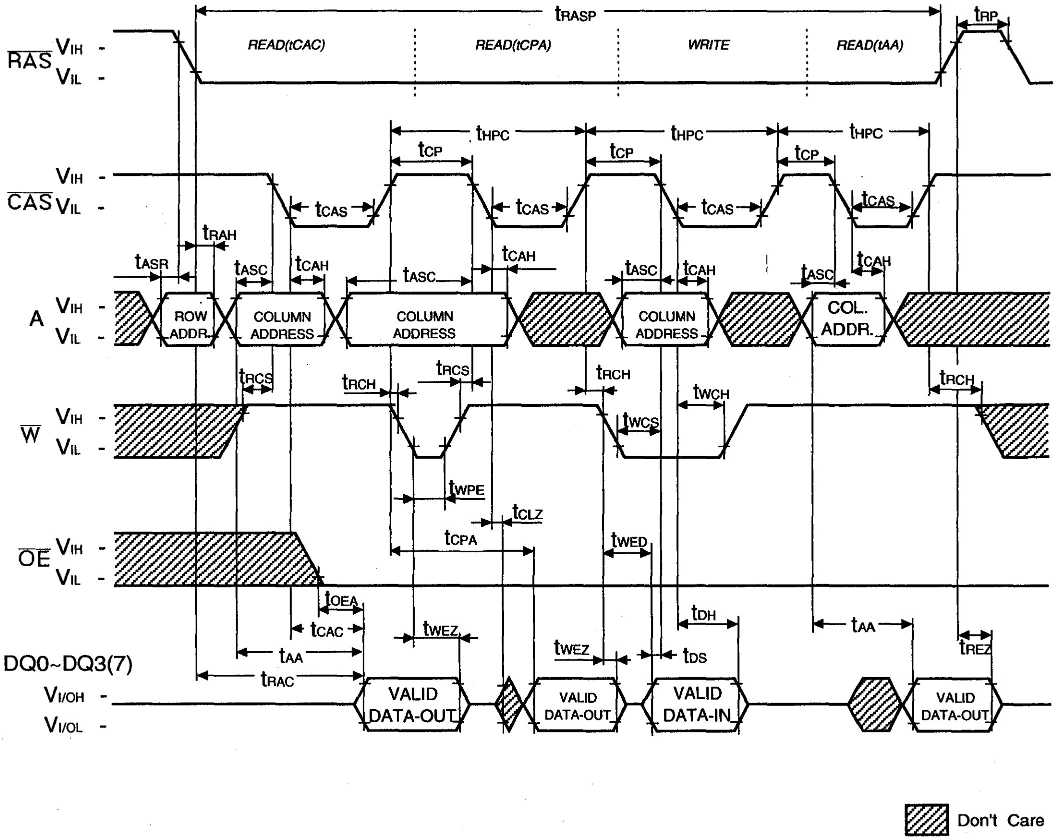


HYPER PAGE READ-MODIFY-WRITE CYCLE



3

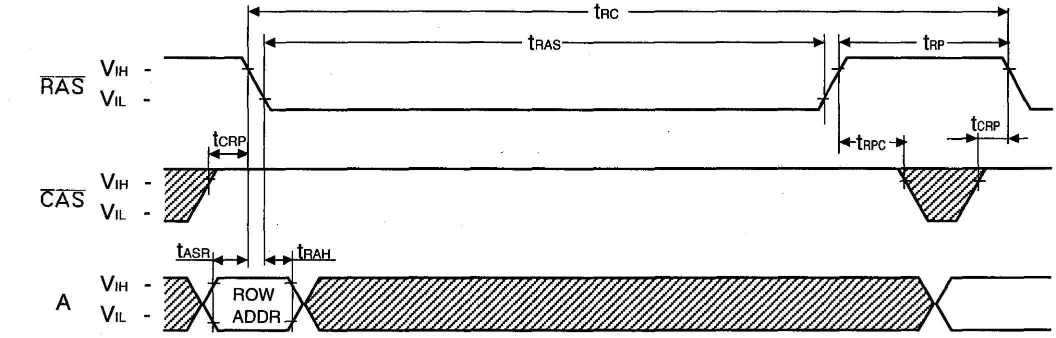
HYPER PAGE READ AND WRITE MIXED CYCLE



SAMSUNG ELECTRONICS

$\overline{RAS}$-ONLY REFRESH CYCLE

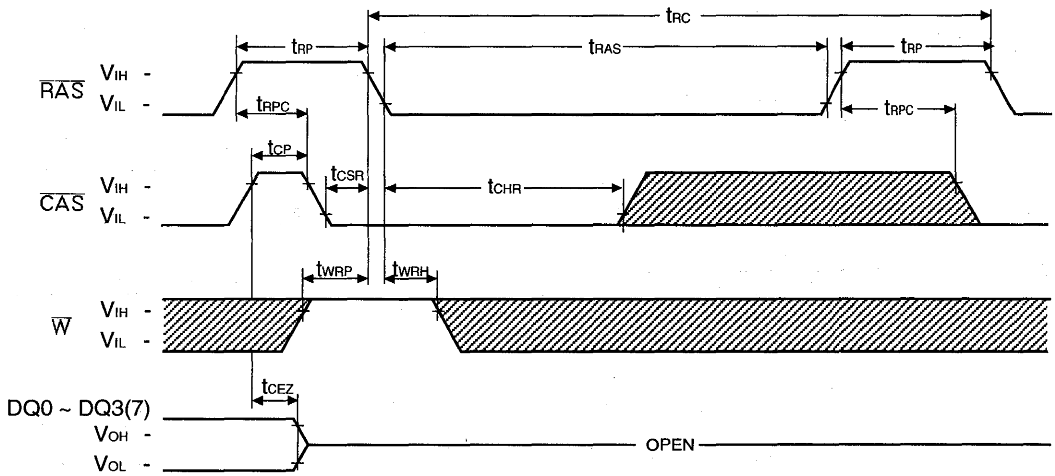
NOTE : $\overline{W}$, $\overline{OE}$, D_{IN} = Don't care
D_{OUT} = Open



3

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

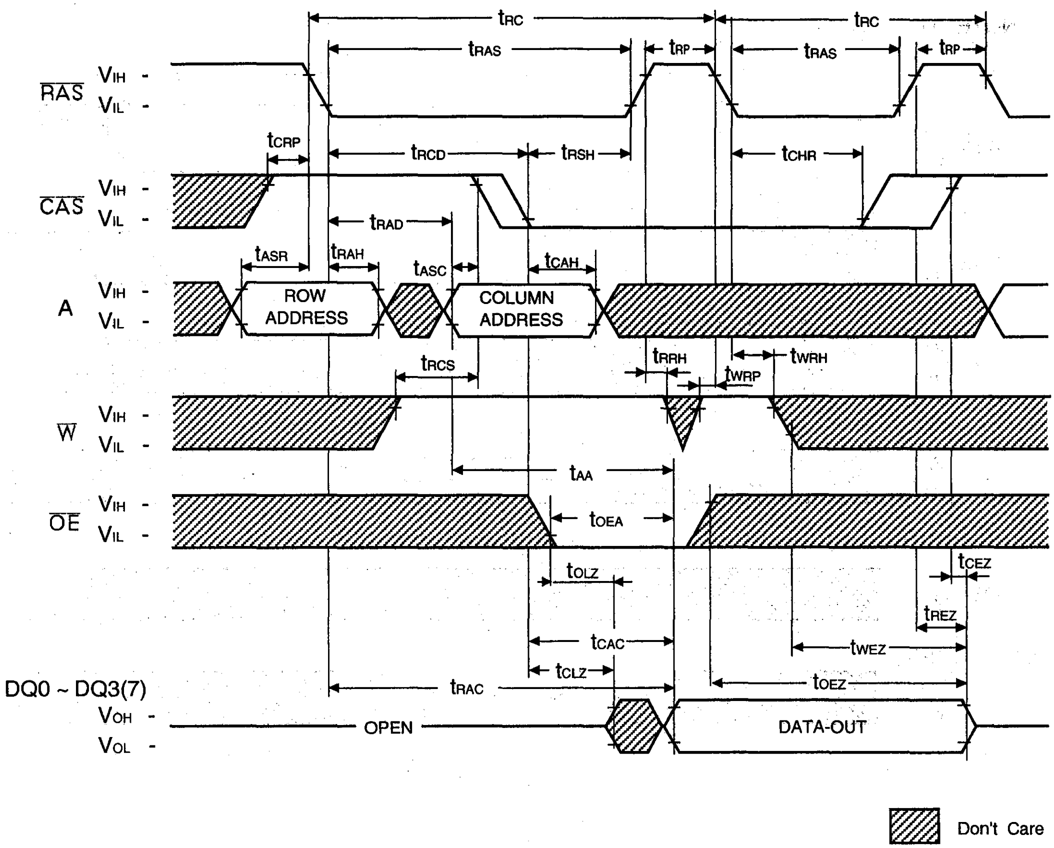
NOTE : $\overline{W}$, $\overline{OE}$, A = Don't Care



Don't Care

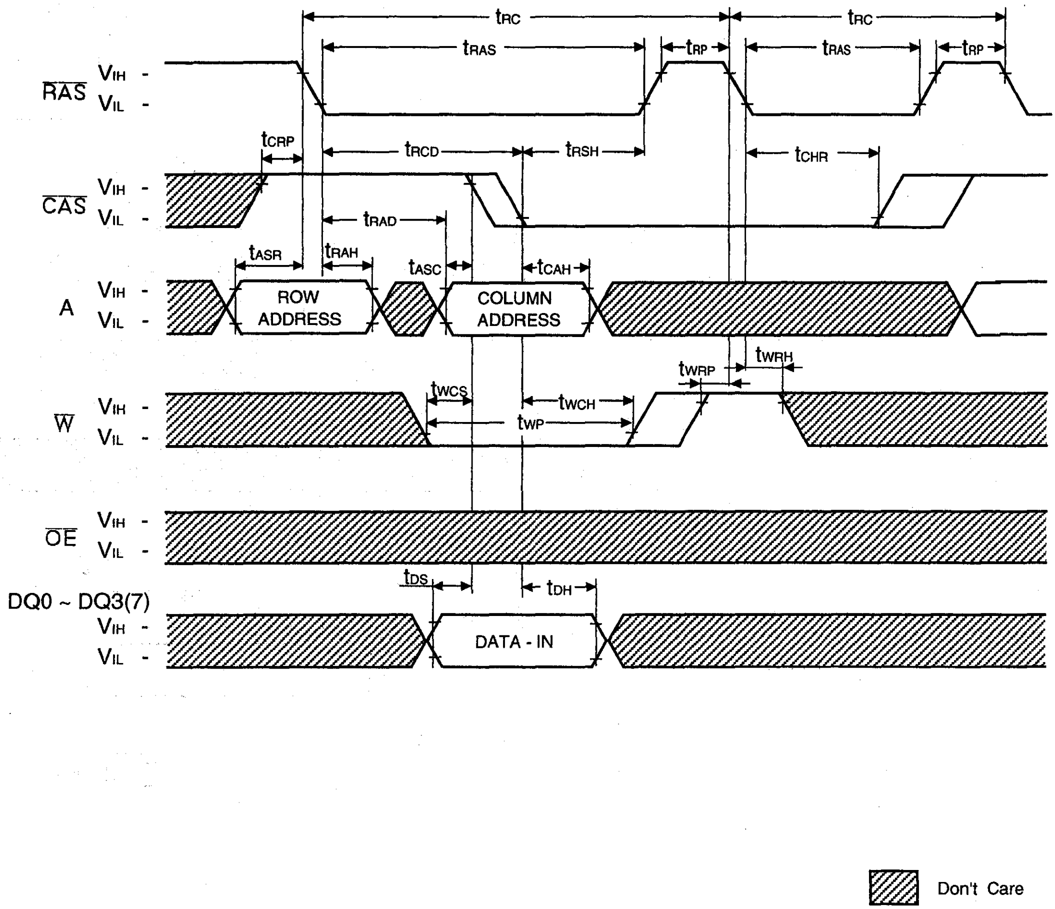
SAMSUNG ELECTRONICS

HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)

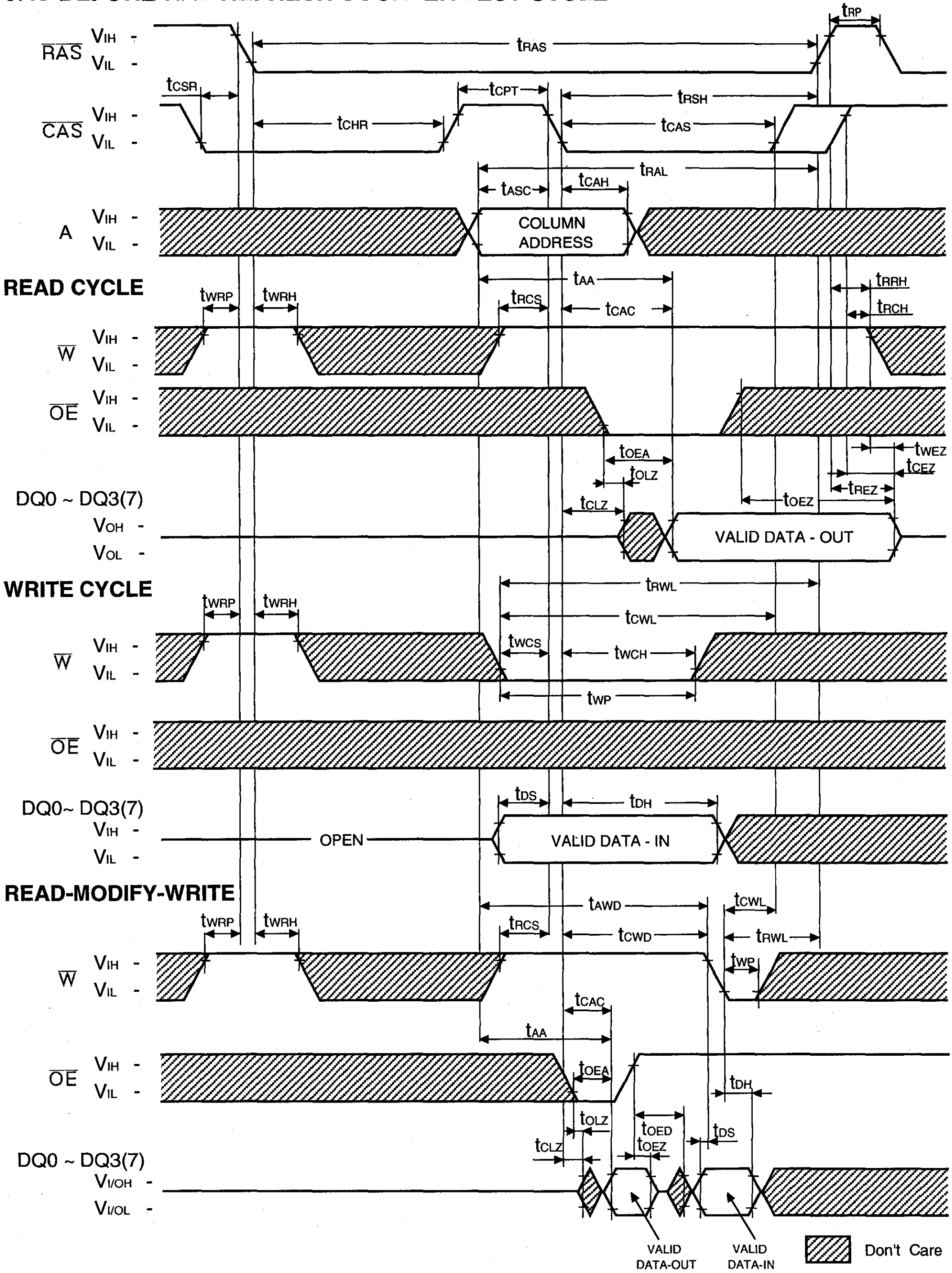
NOTE : DOUT = OPEN



3

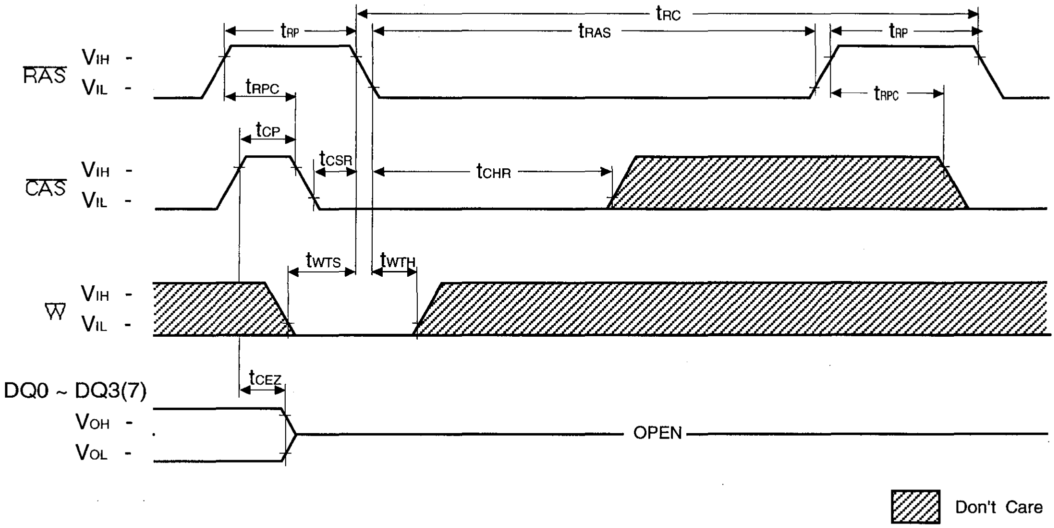
SAMSUNG ELECTRONICS

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



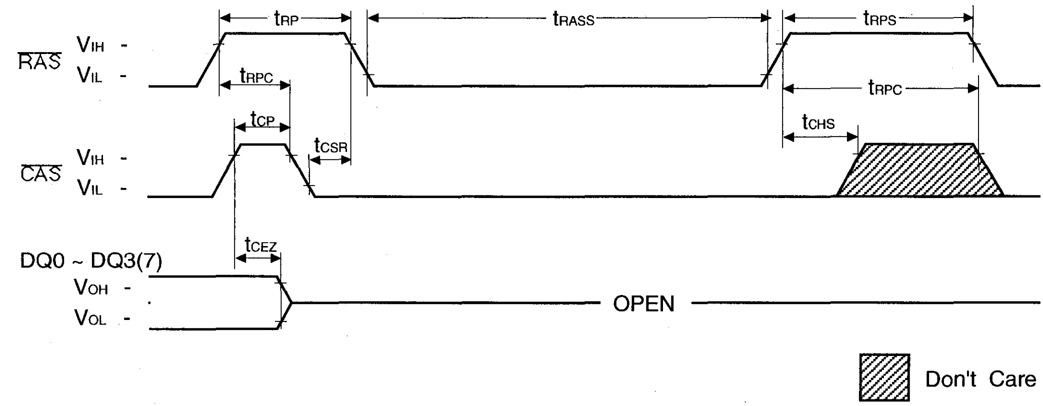
TEST MODE IN CYCLE

NOTE : $\overline{OE}$, A = Don't Care



$\overline{CAS}$-BEFORE-$\overline{RAS}$ SELF REFRESH CYCLE

NOTE : $\overline{W}$, $\overline{OE}$, A = Don't Care

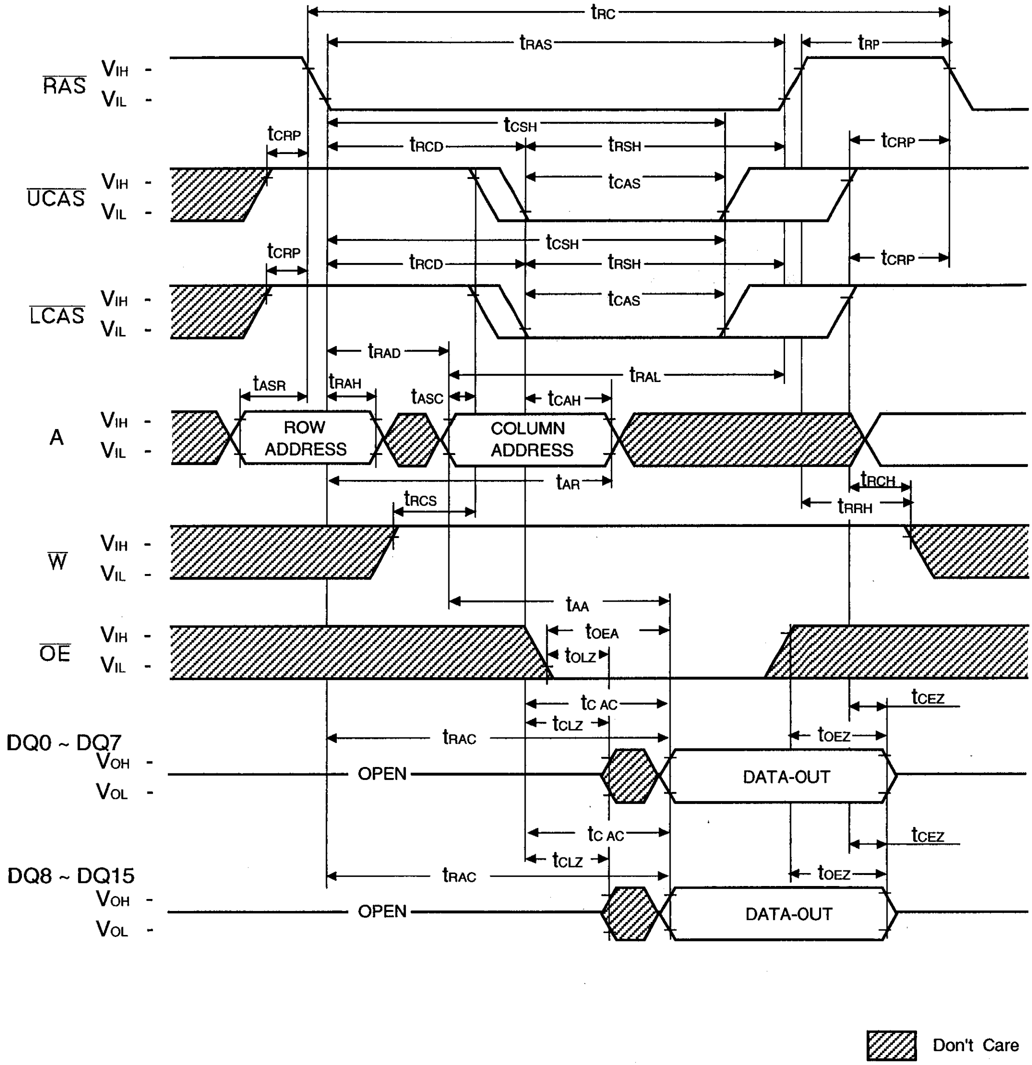


EDO Mode, x16 (2$\overline{CAS}$) Device

TIMING DIAGRAM

WORD READ CYCLE

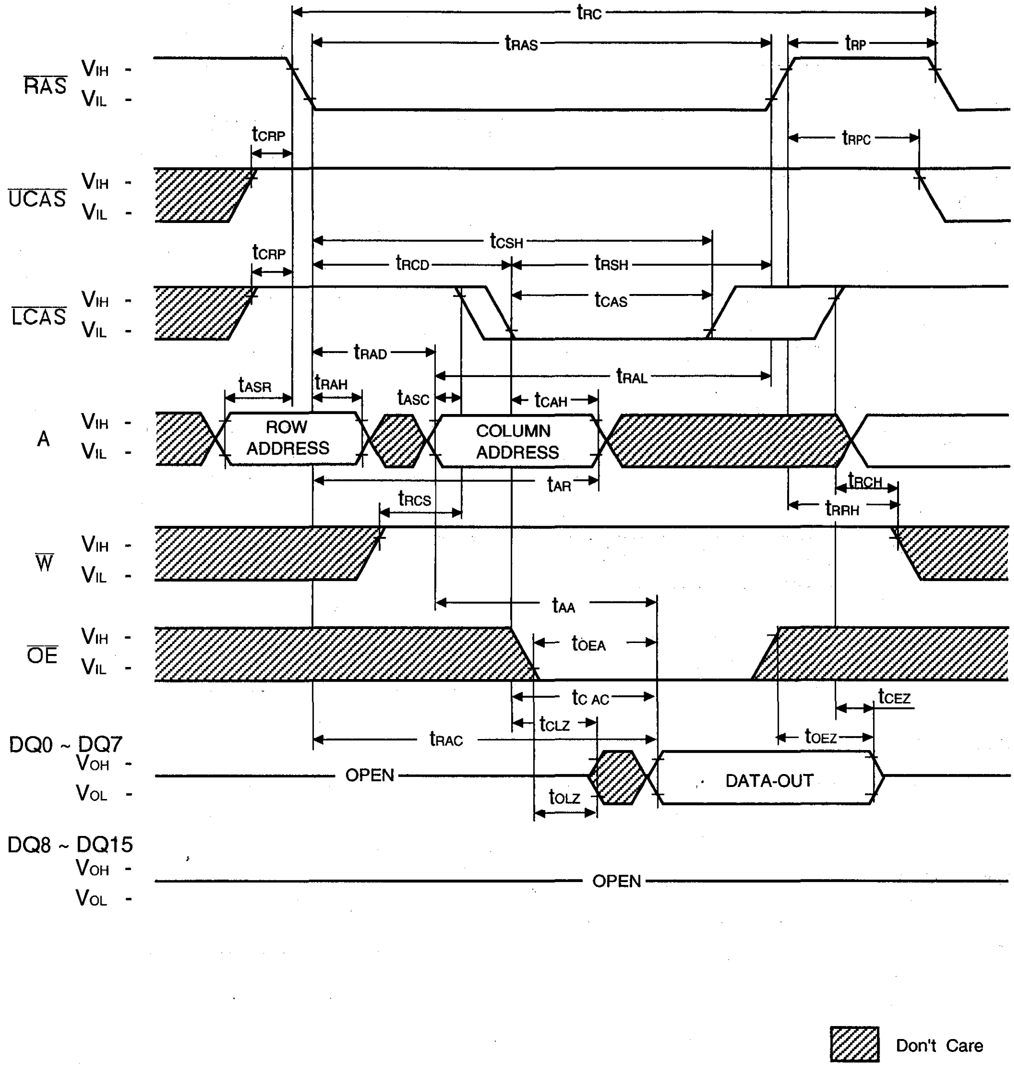
NOTE : D_{IN} = OPEN



TIMING DIAGRAM

LOWER BYTE READ CYCLE

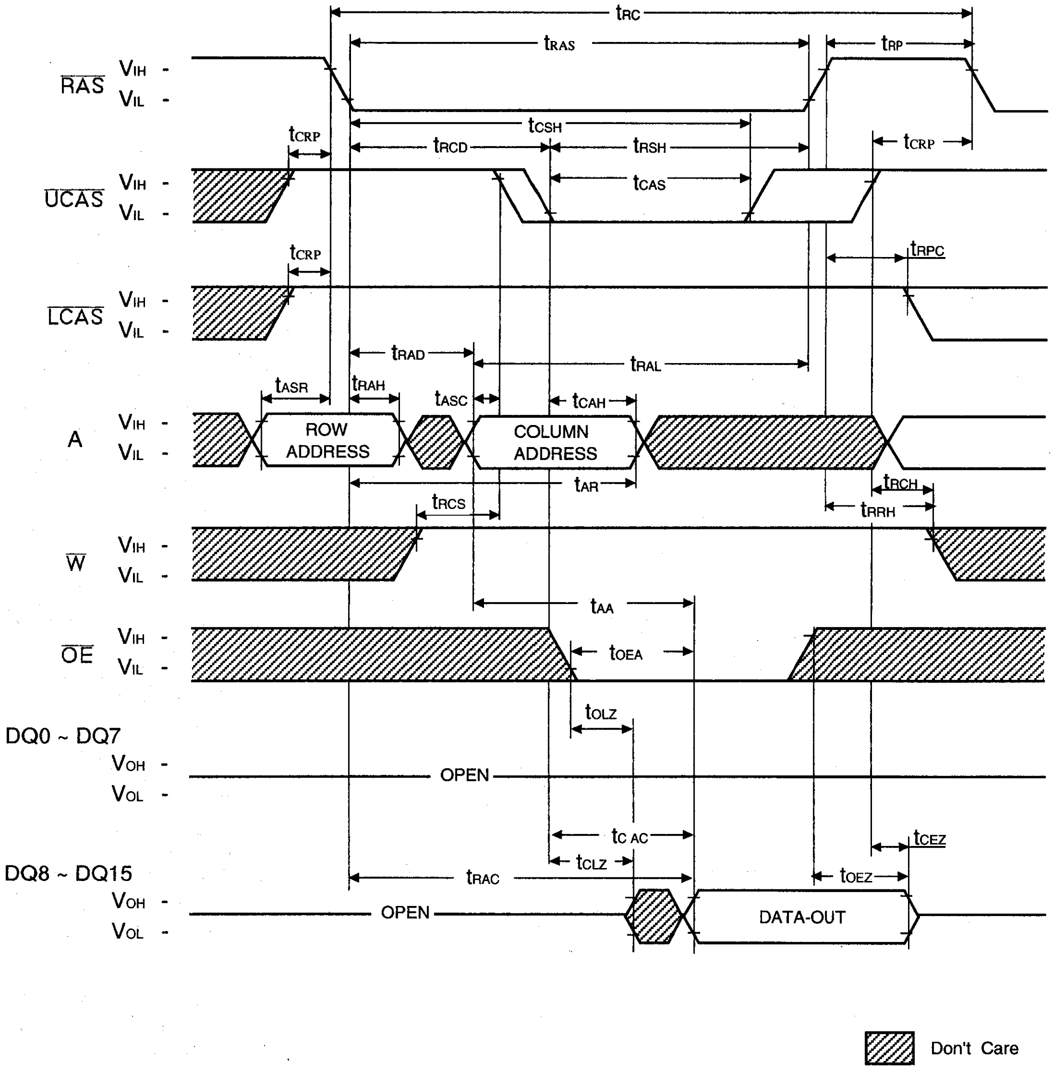
NOTE : D_{IN} = OPEN



TIMING DIAGRAM

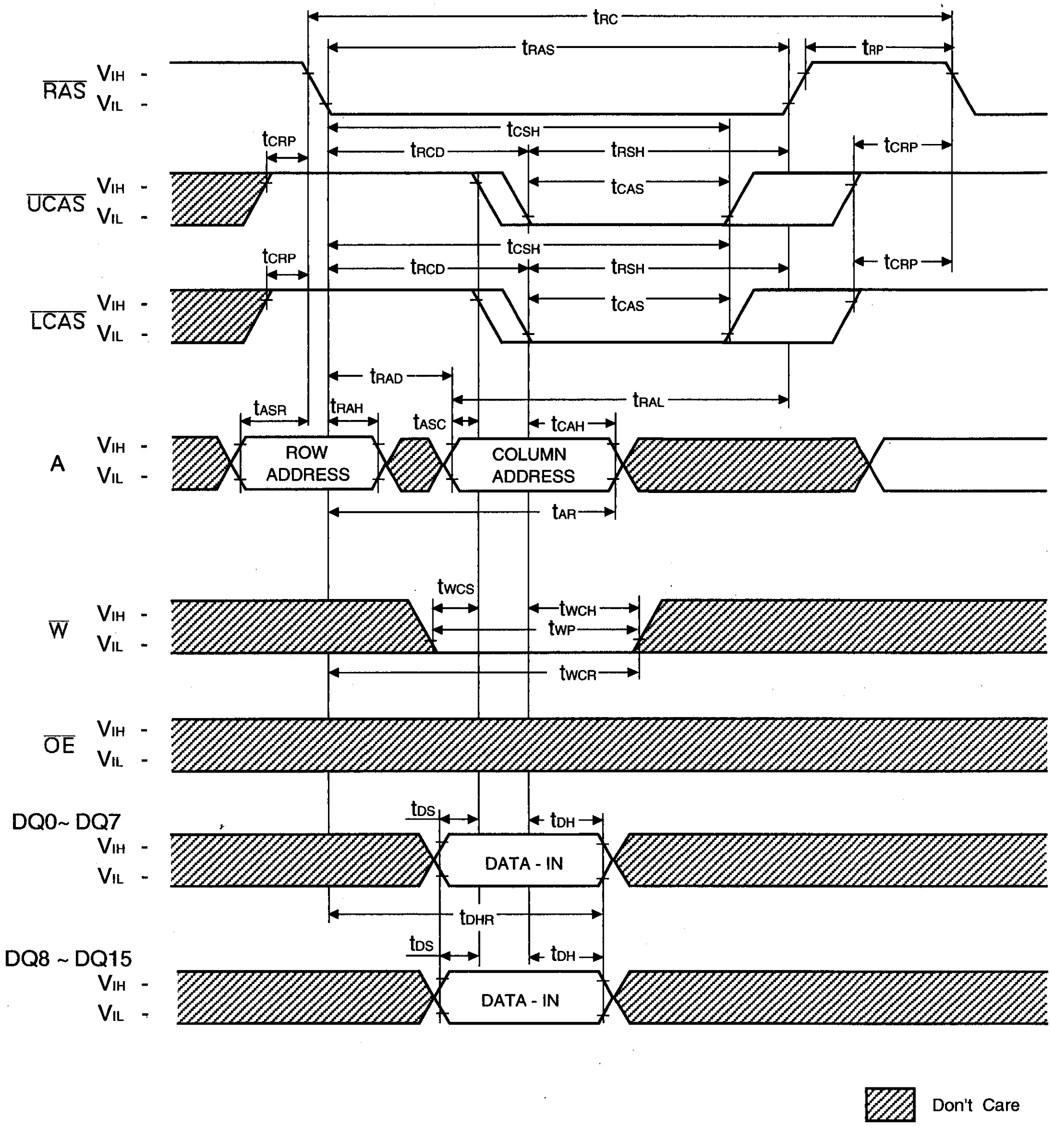
UPPER BYTE READ CYCLE

NOTE : D_{IN} = OPEN



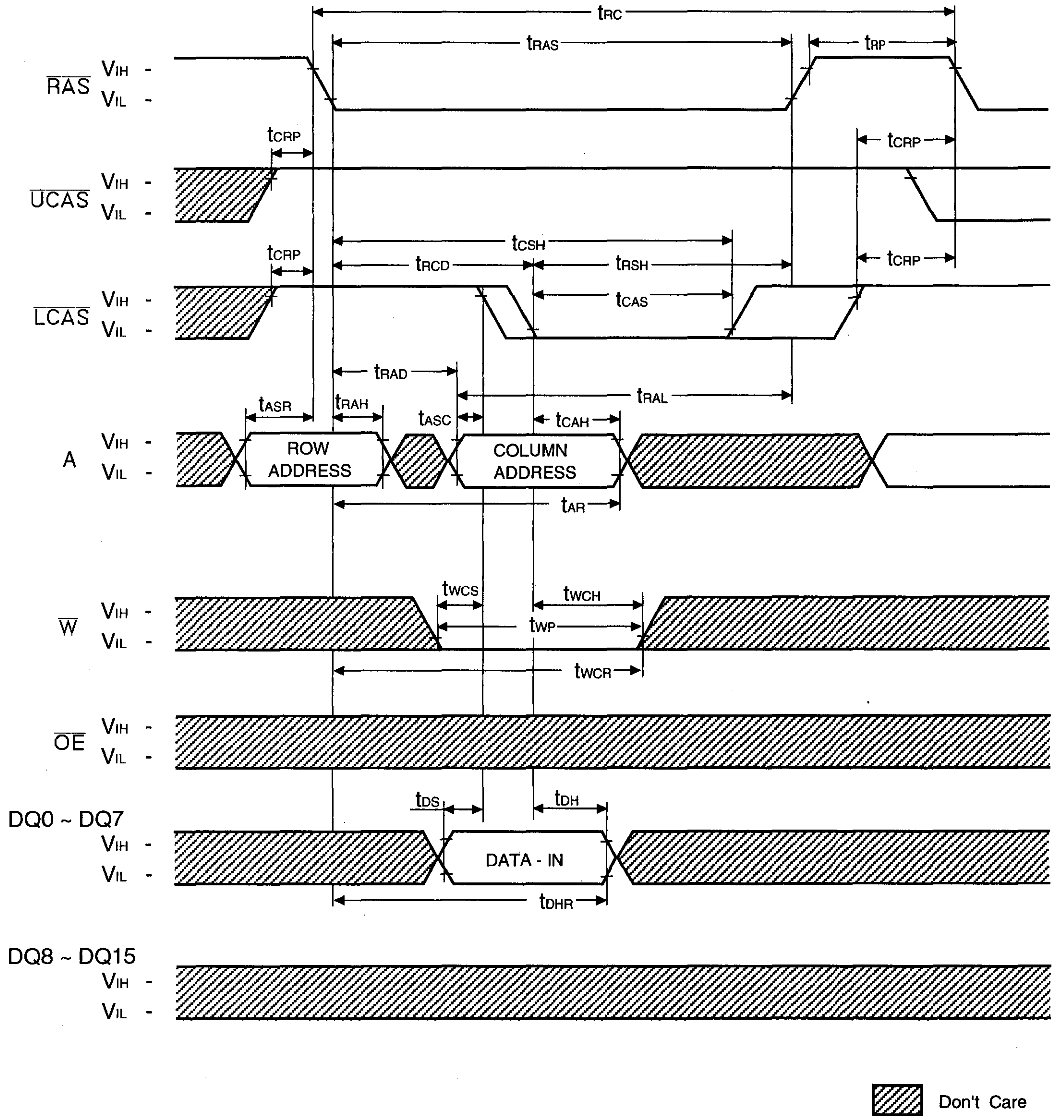
WORD WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = OPEN



LOWER BYTE WRITE CYCLE (EARLY WRITE)

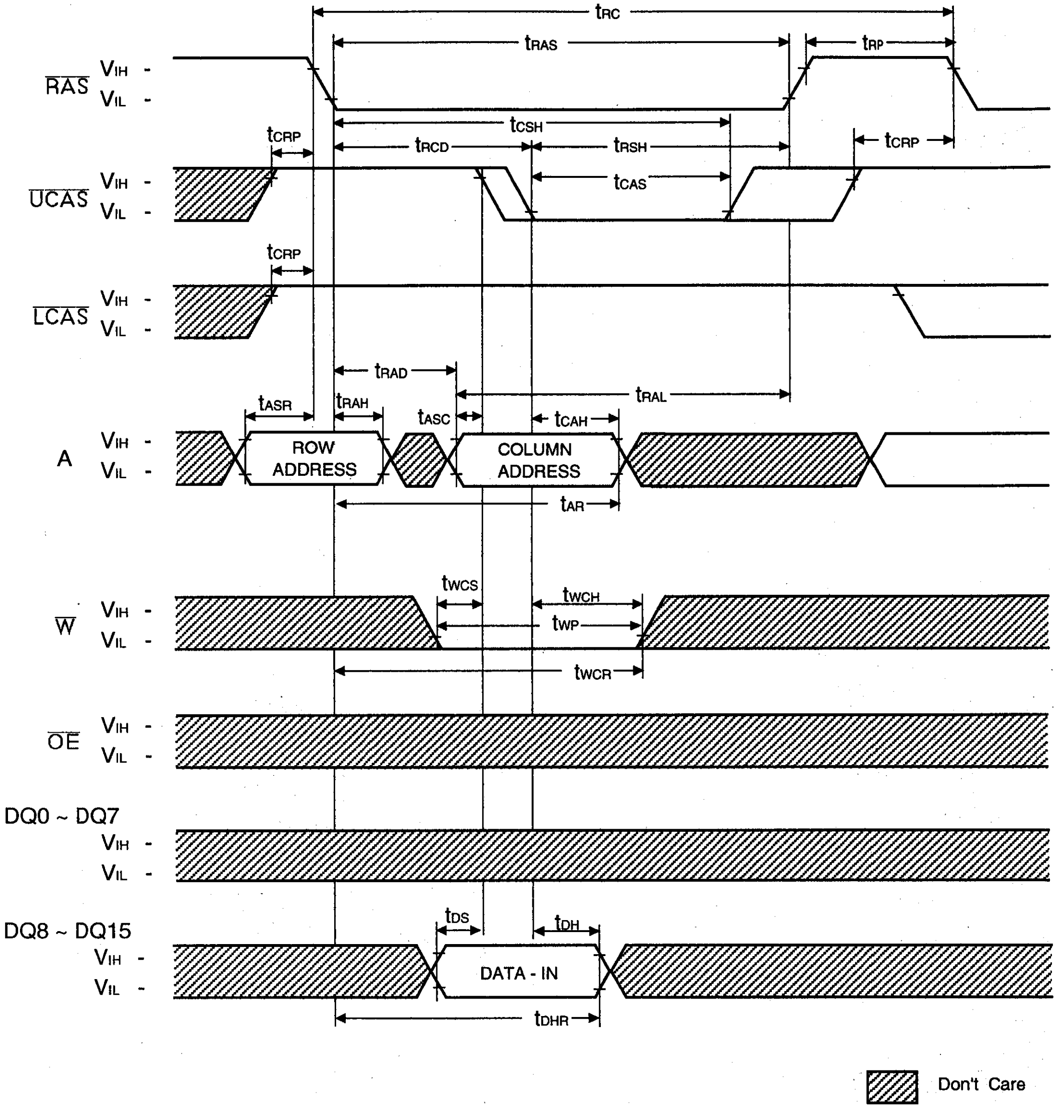
NOTE : D_{OUT} = OPEN



3

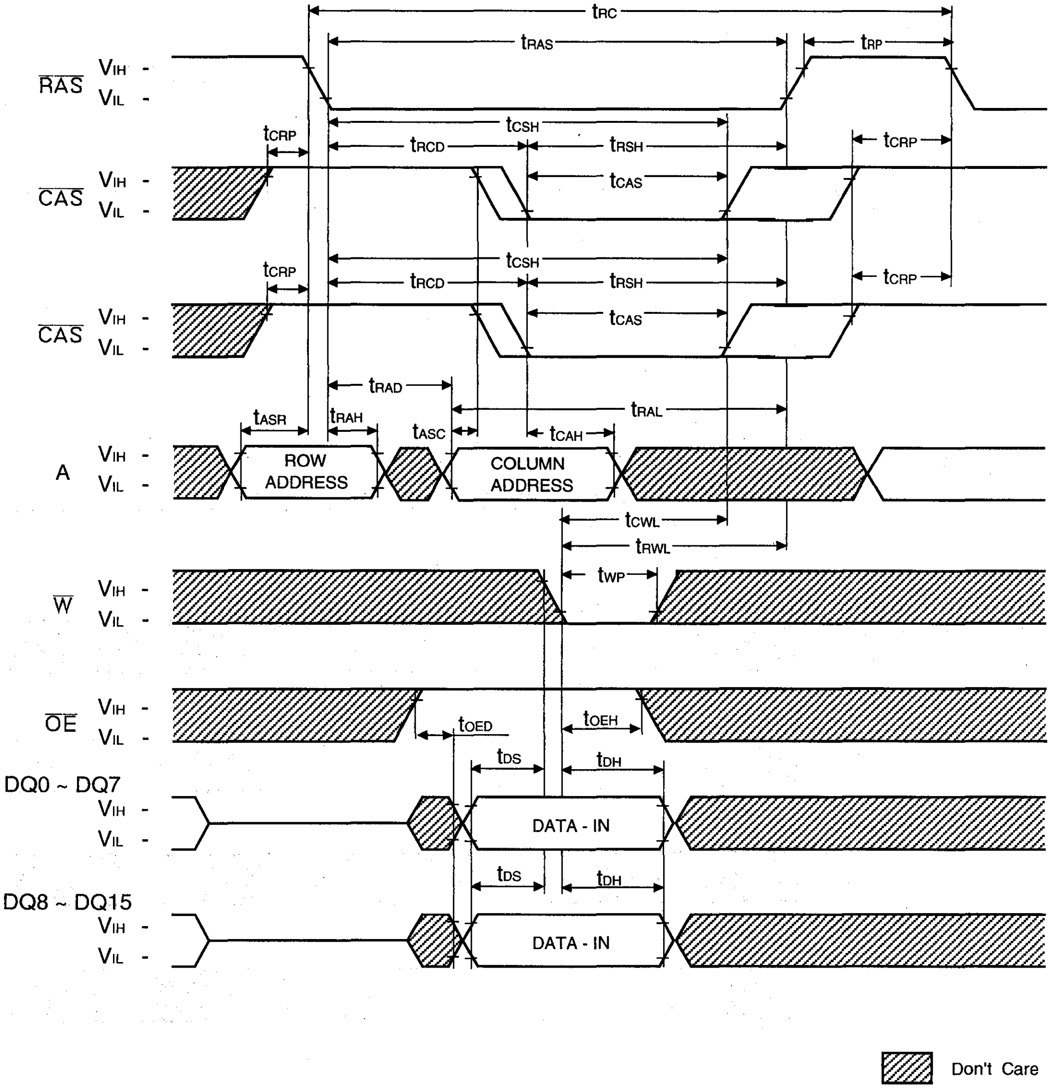
UPPER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = OPEN



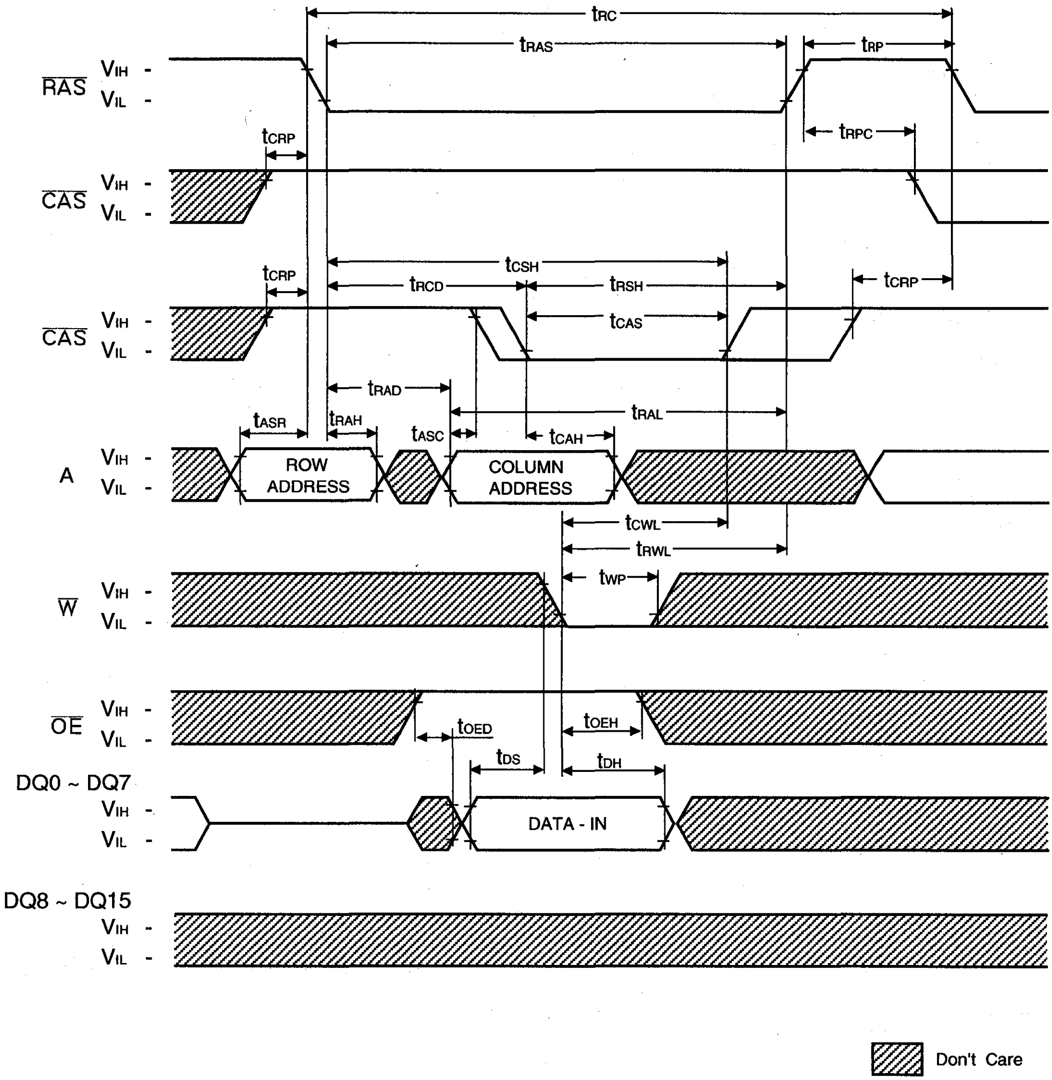
WORD WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

NOTE : D_{OUT} = OPEN



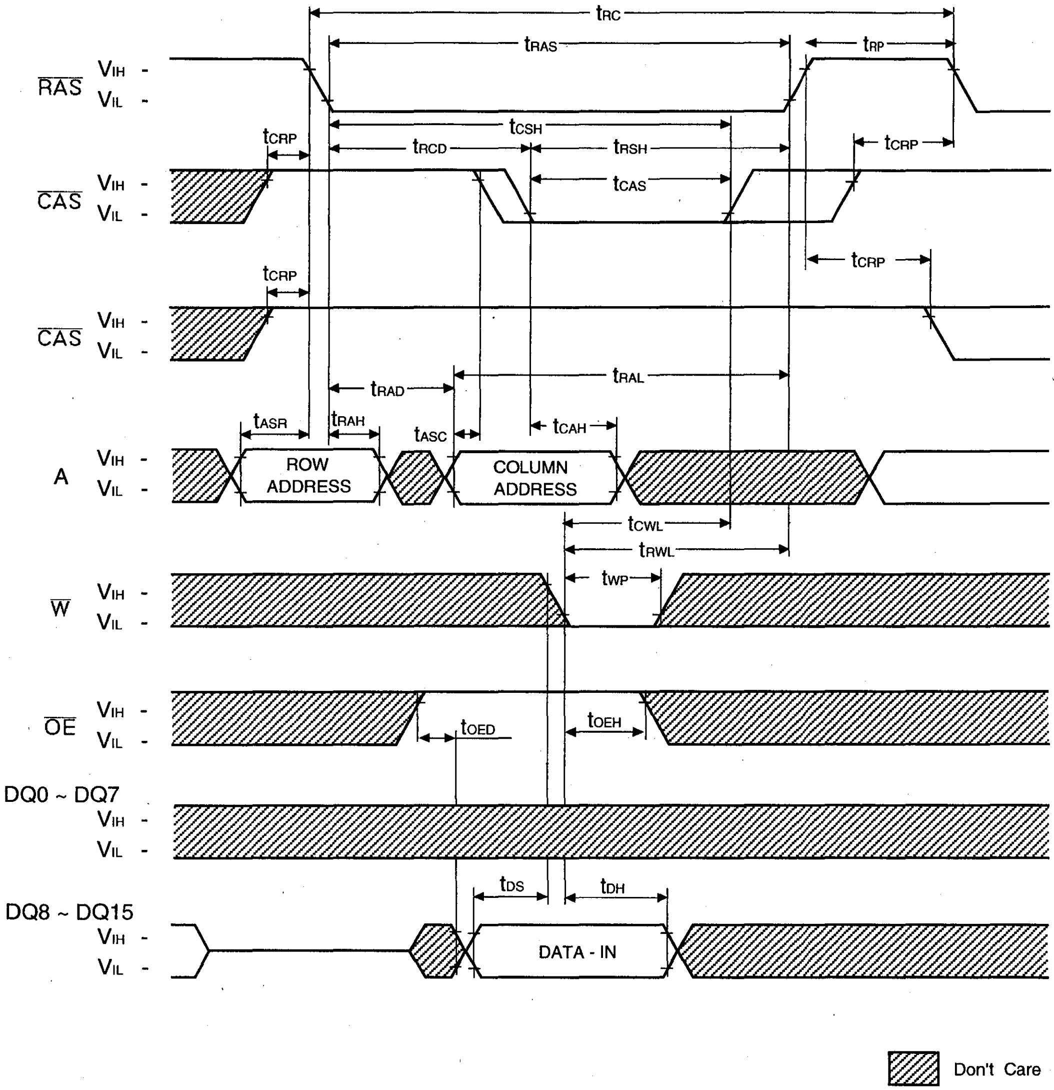
LOWER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

NOTE : D_{OUT} = OPEN



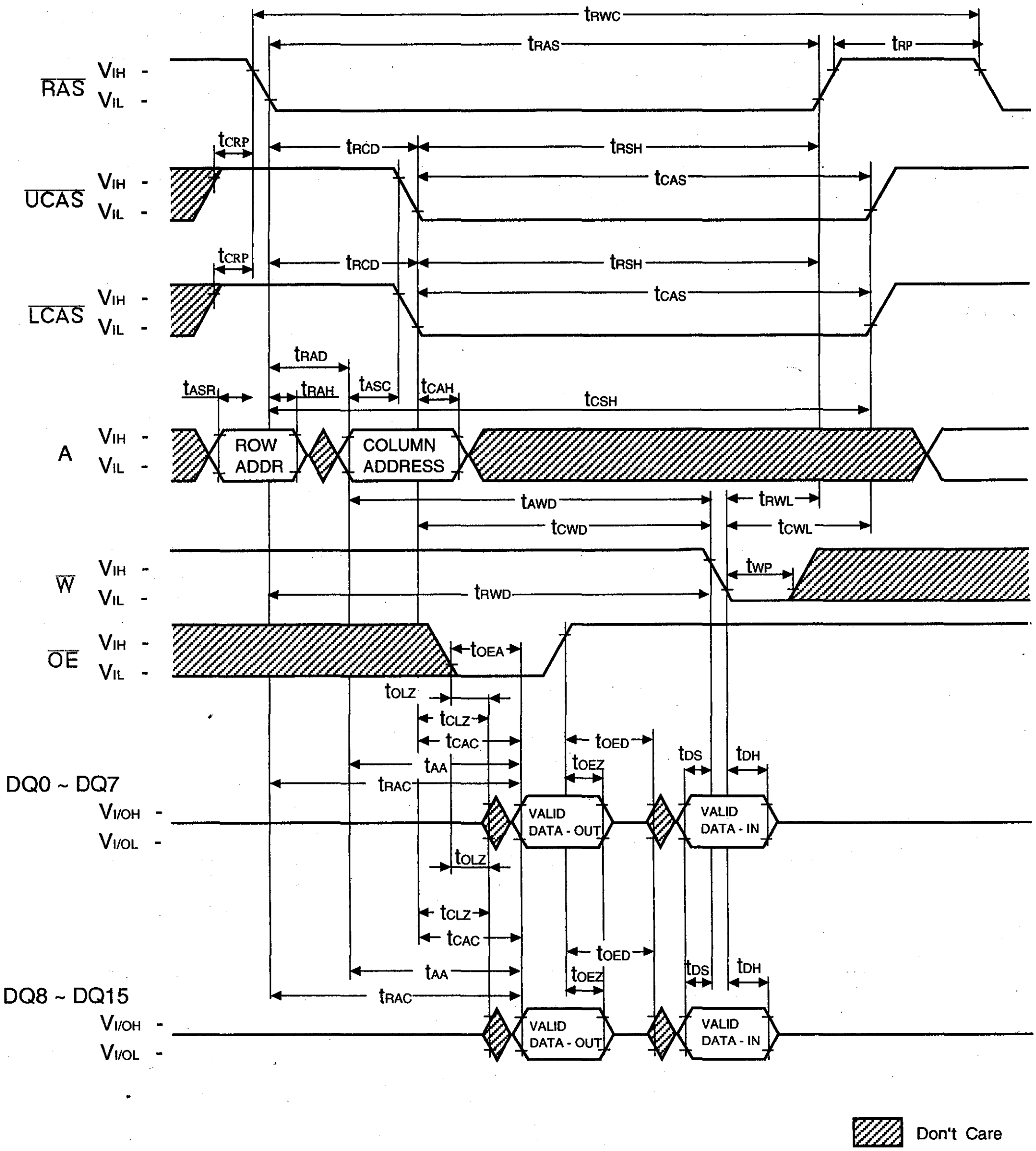
UPPER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

NOTE : DOUT = OPEN

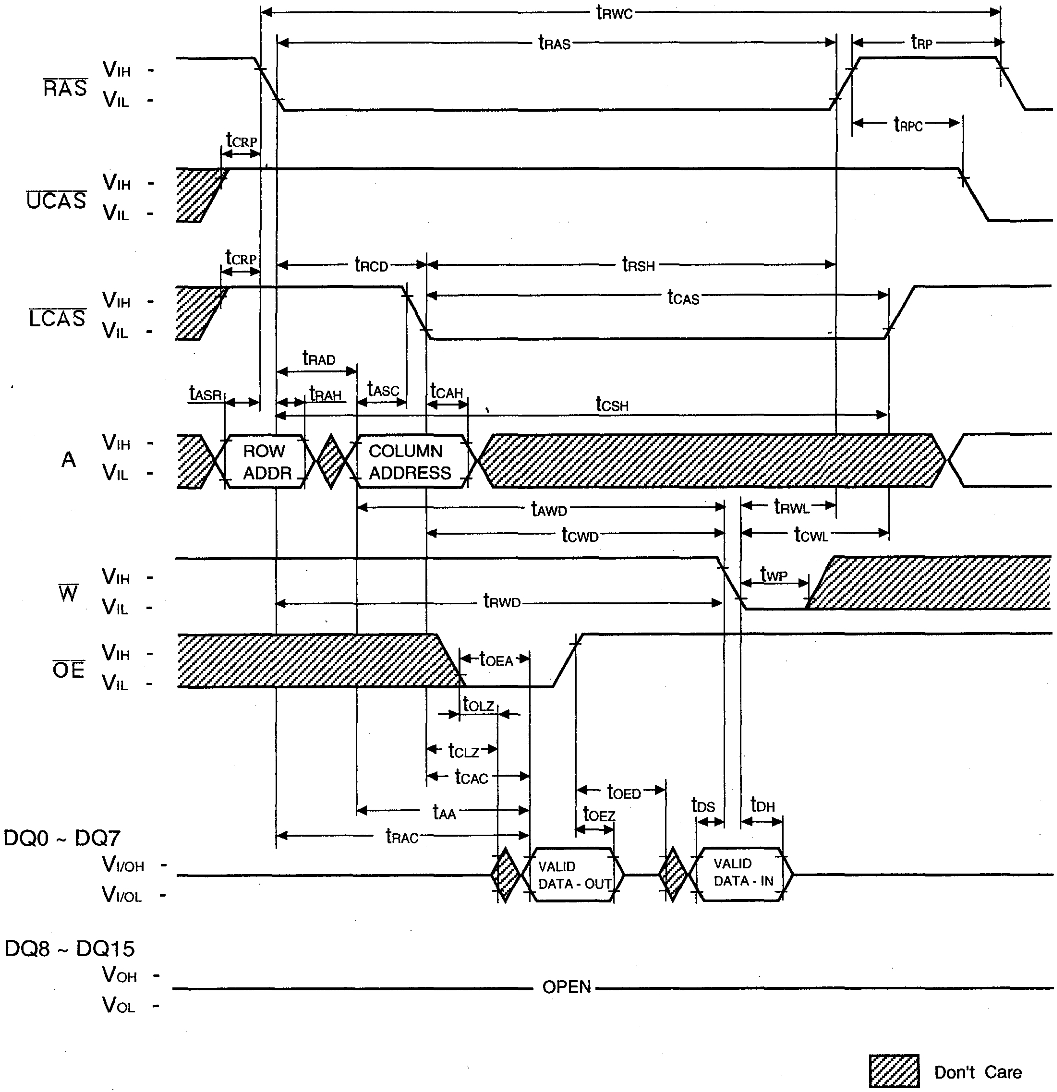


3

WORD READ - MODIFY - WRITE CYCLE



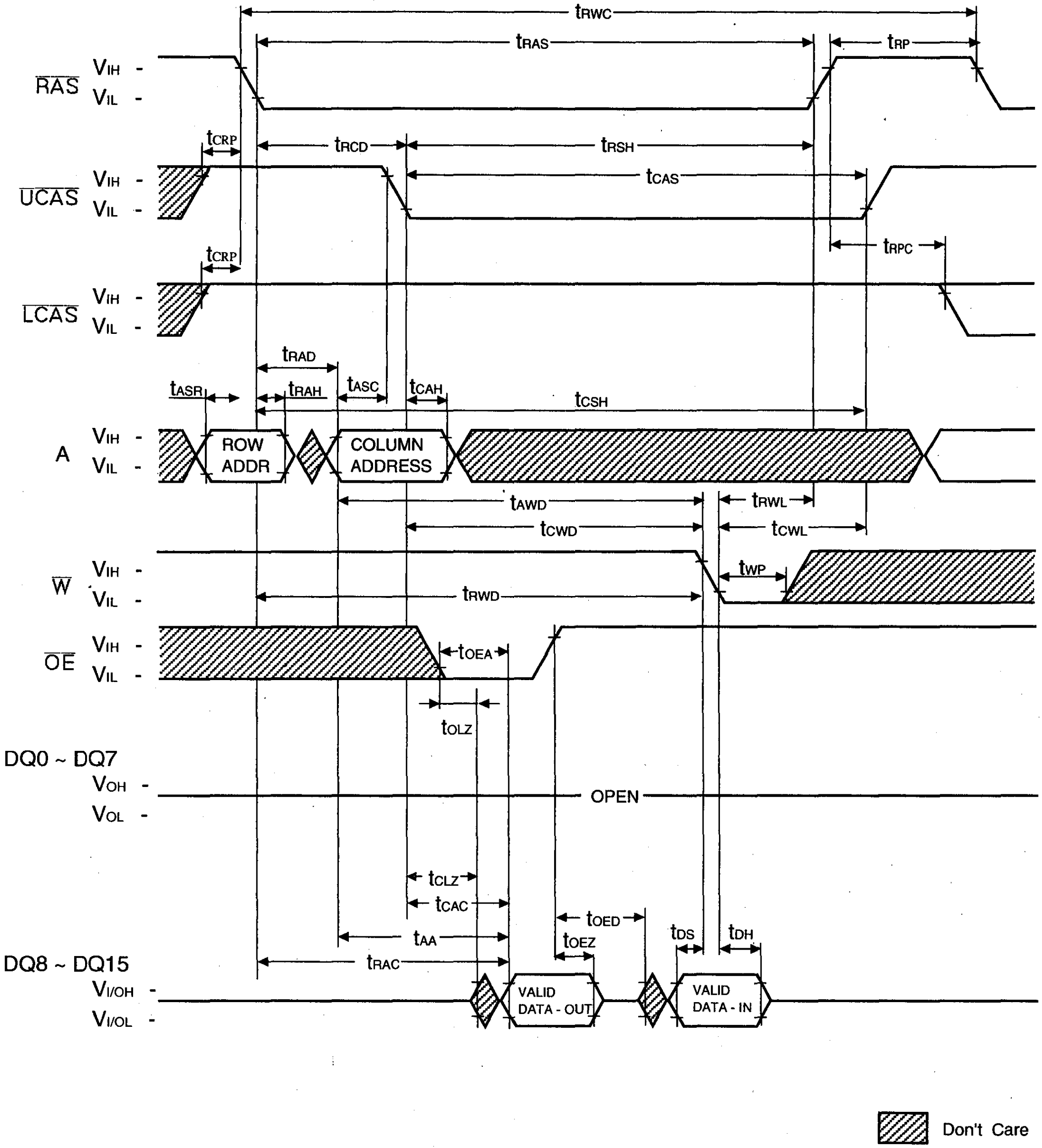
LOWER-BYTE READ - MODIFY - WRITE CYCLE



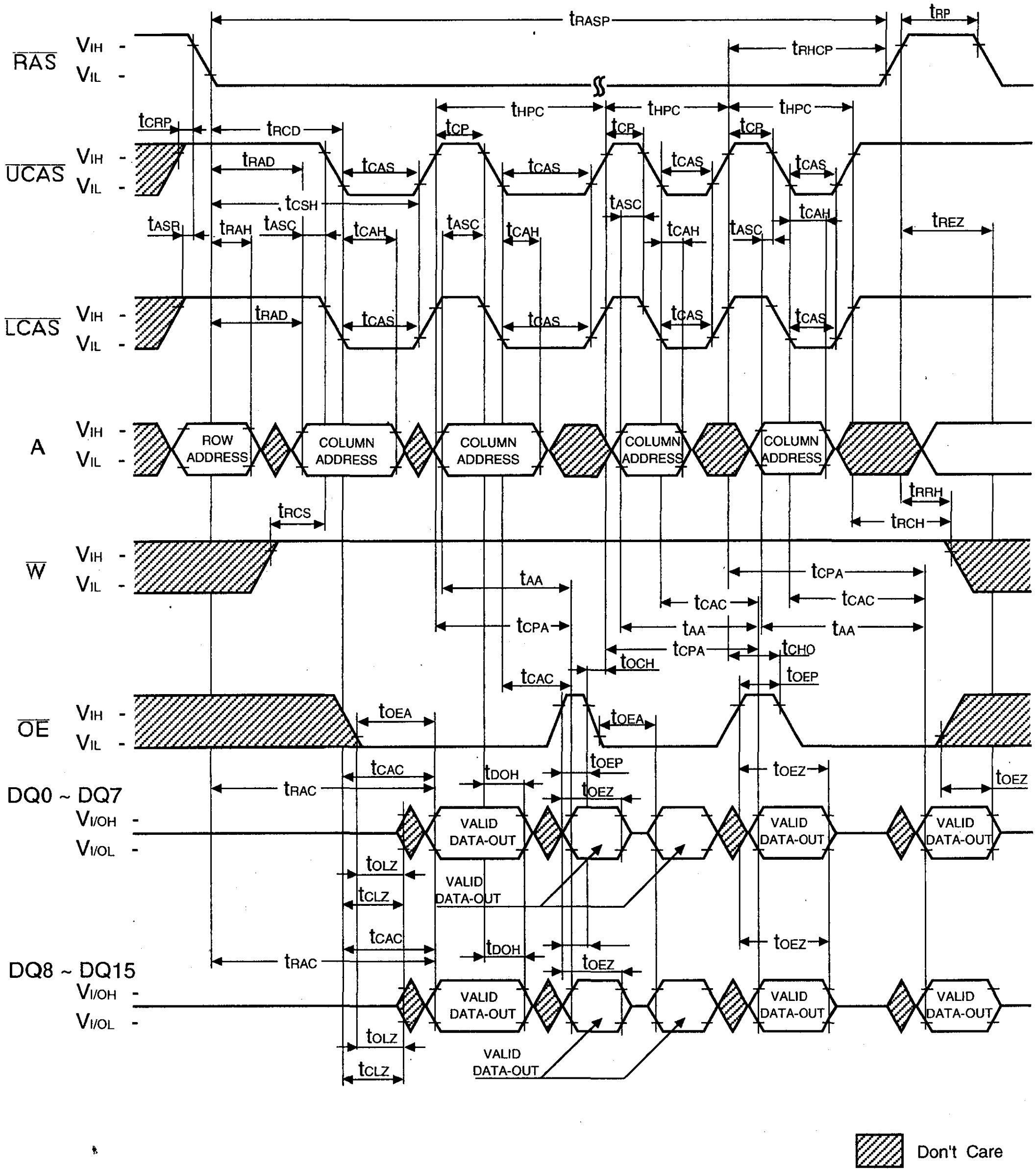
3

SAMSUNG ELECTRONICS

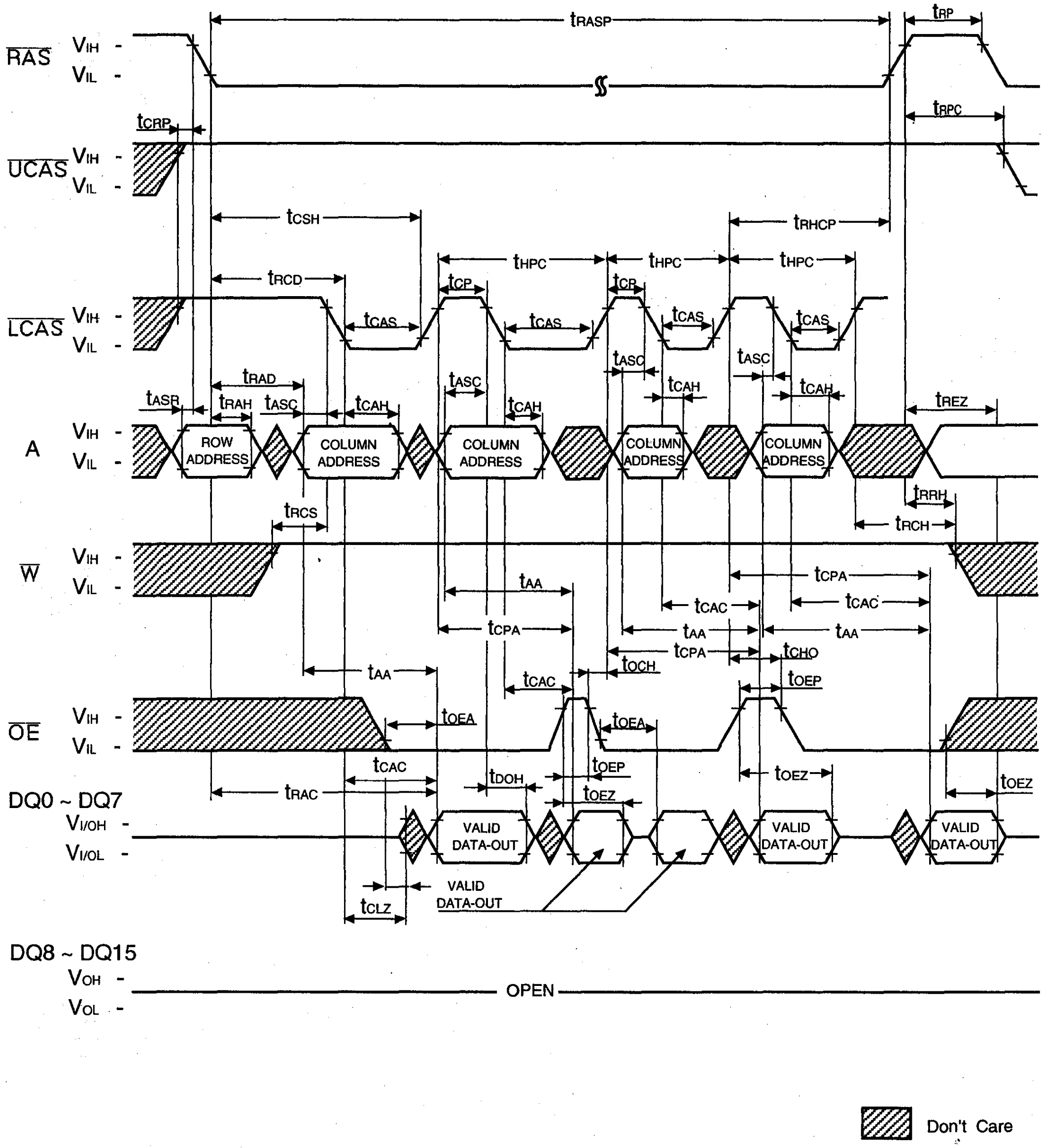
UPPER-BYTE READ - MODIFY - WRITE CYCLE



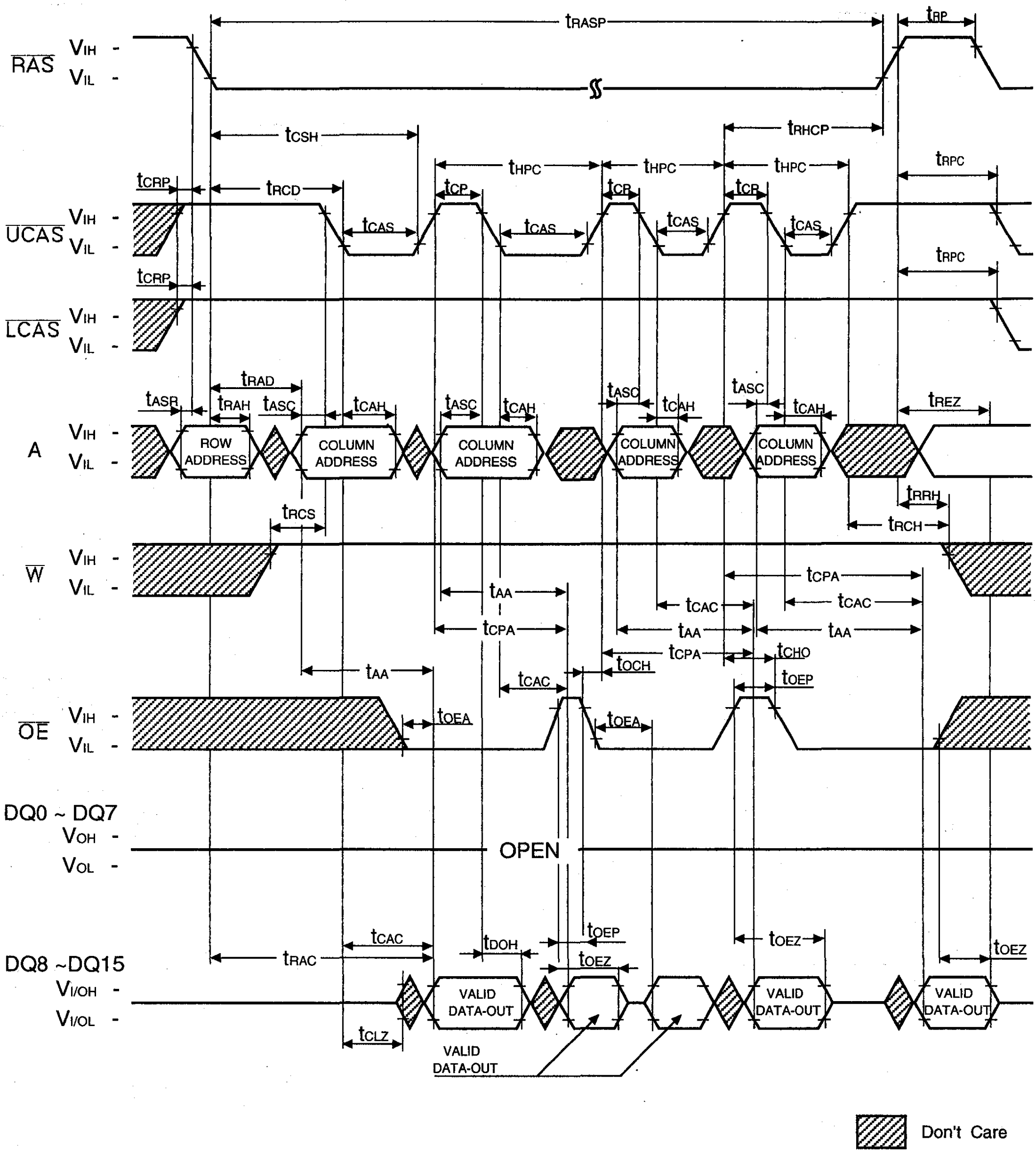
HYPER PAGE MODE WORD READ CYCLE



HYPER PAGE MODE LOWER BYTE READ CYCLE



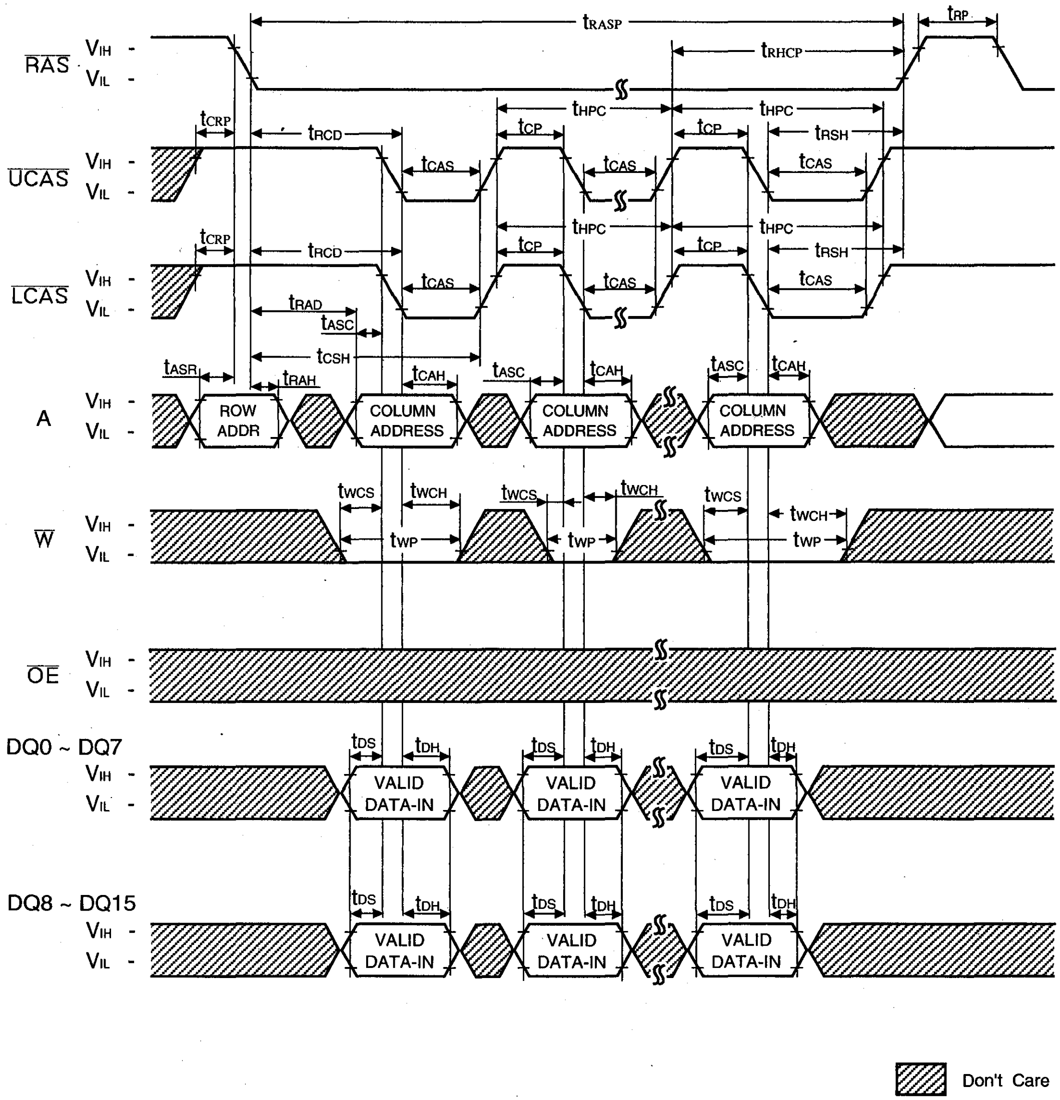
HYPER PAGE MODE UPPER BYTE READ CYCLE



SAMSUNG ELECTRONICS

HYPER PAGE MODE WORD WRITE CYCLE (EARLY WRITE)

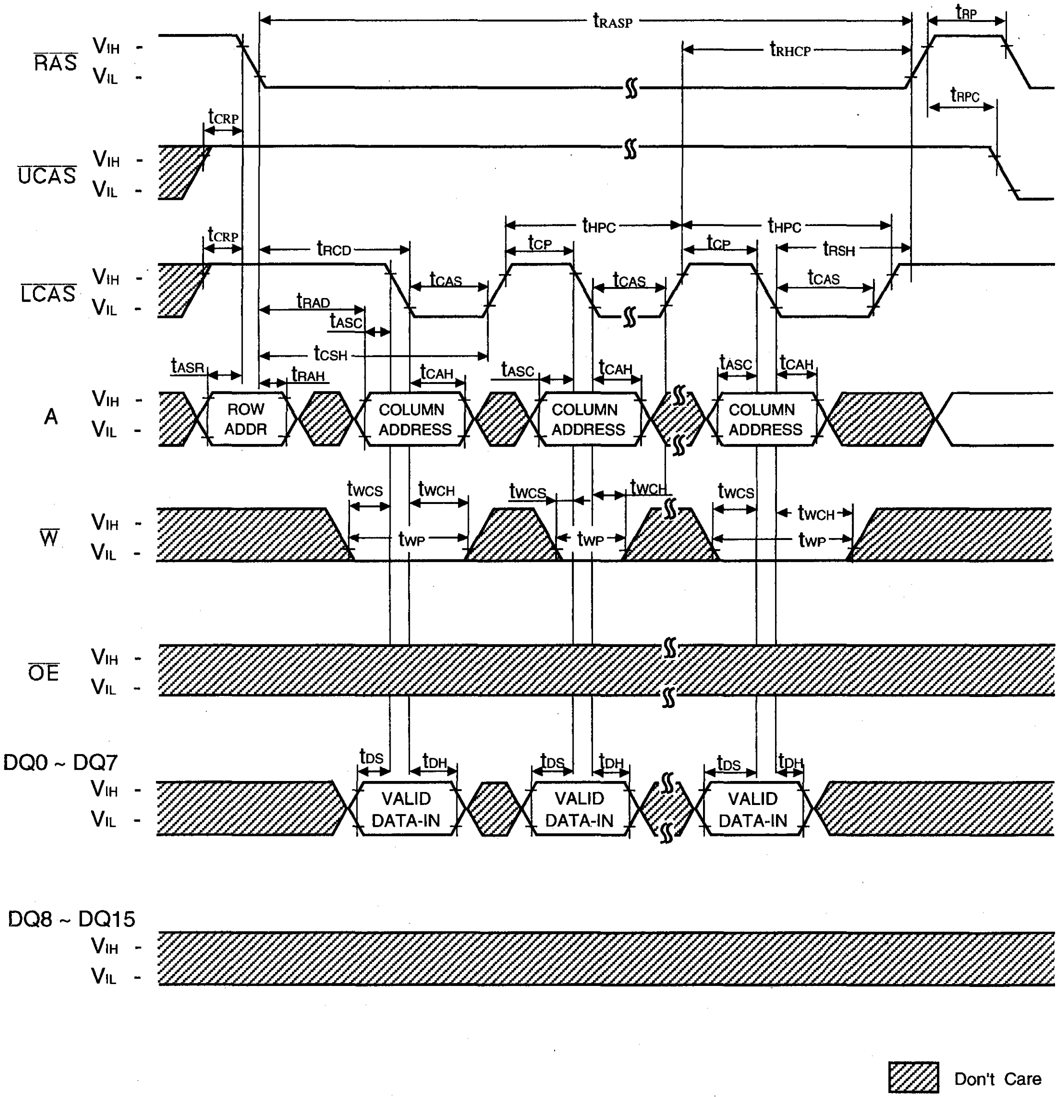
NOTE : D_{OUT} = Open



SAMSUNG ELECTRONICS

HYPER PAGE MODE LOWER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = Open

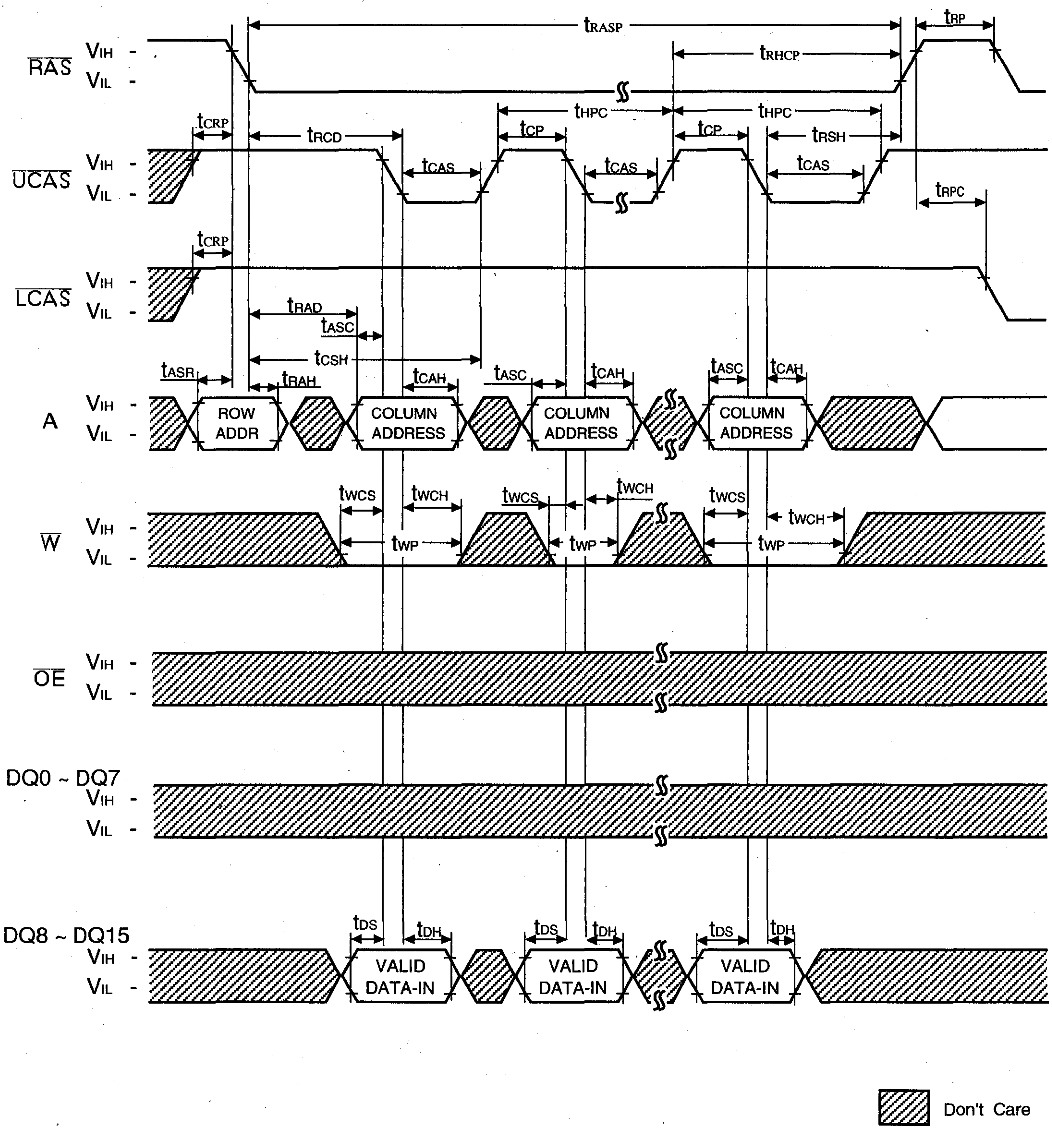


3

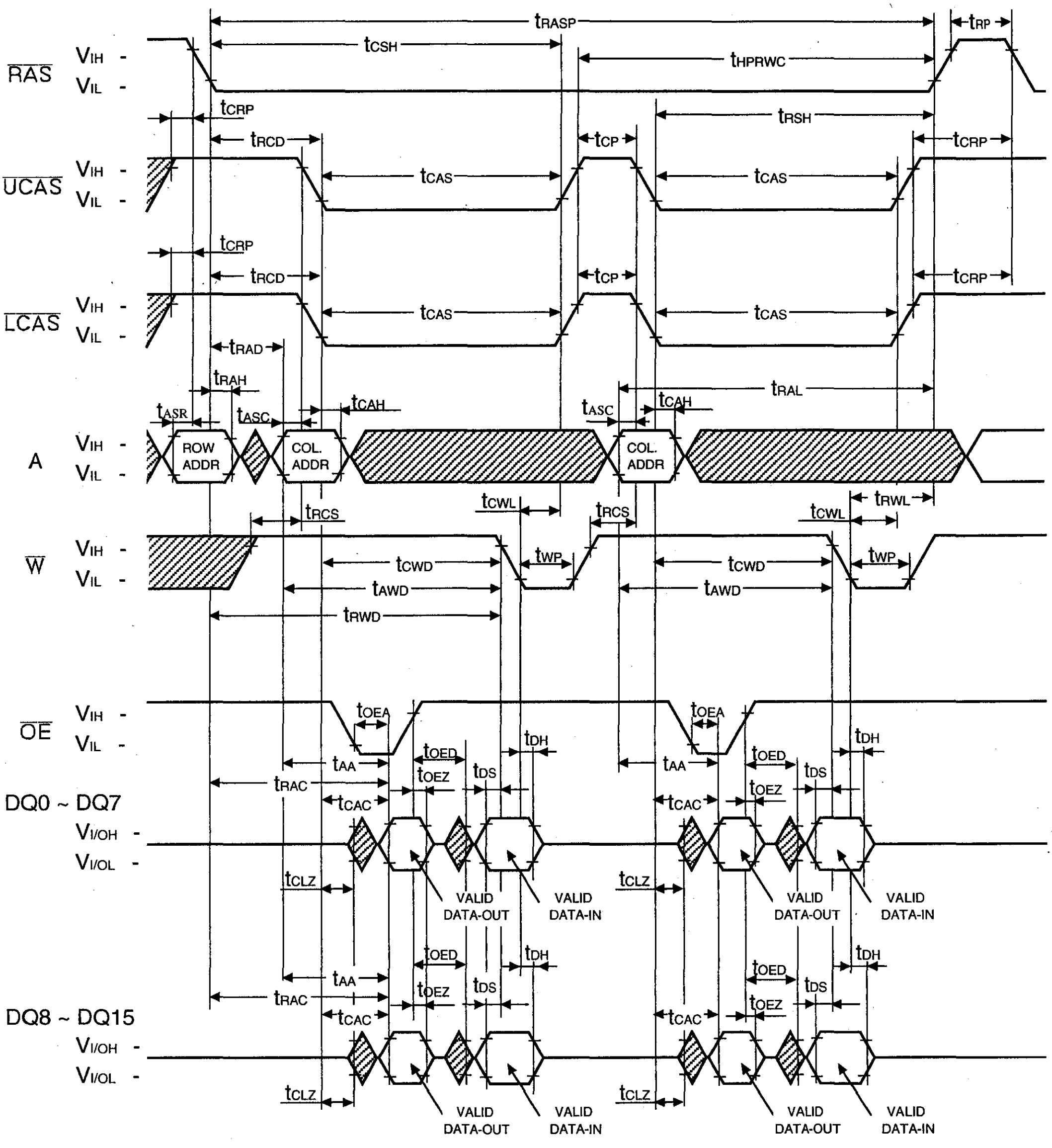
SAMSUNG ELECTRONICS

HYPER PAGE MODE UPPER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = Open



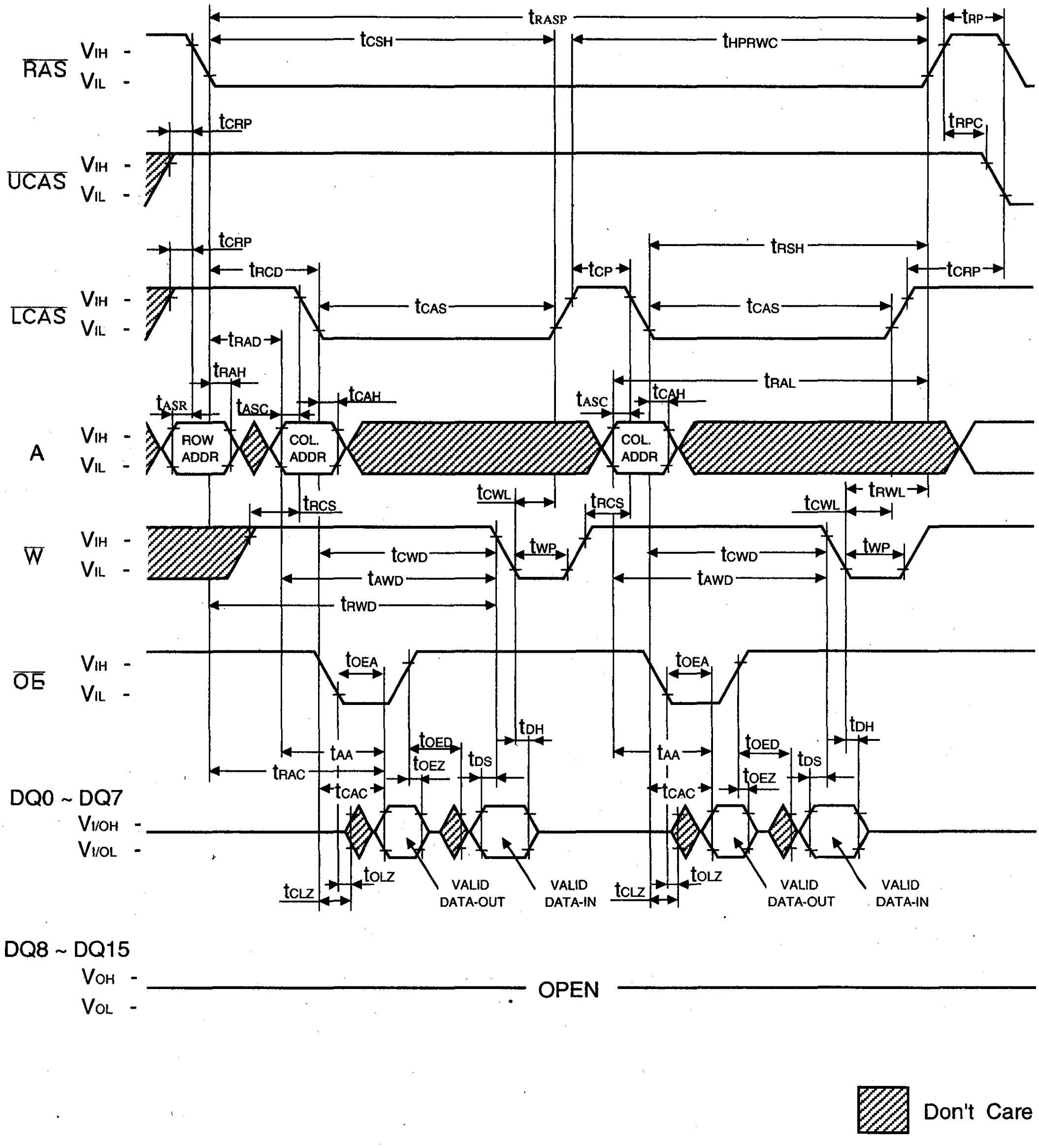
HYPER PAGE MODE WORD READ-MODIFY-WRITE CYCLE



Don't Care

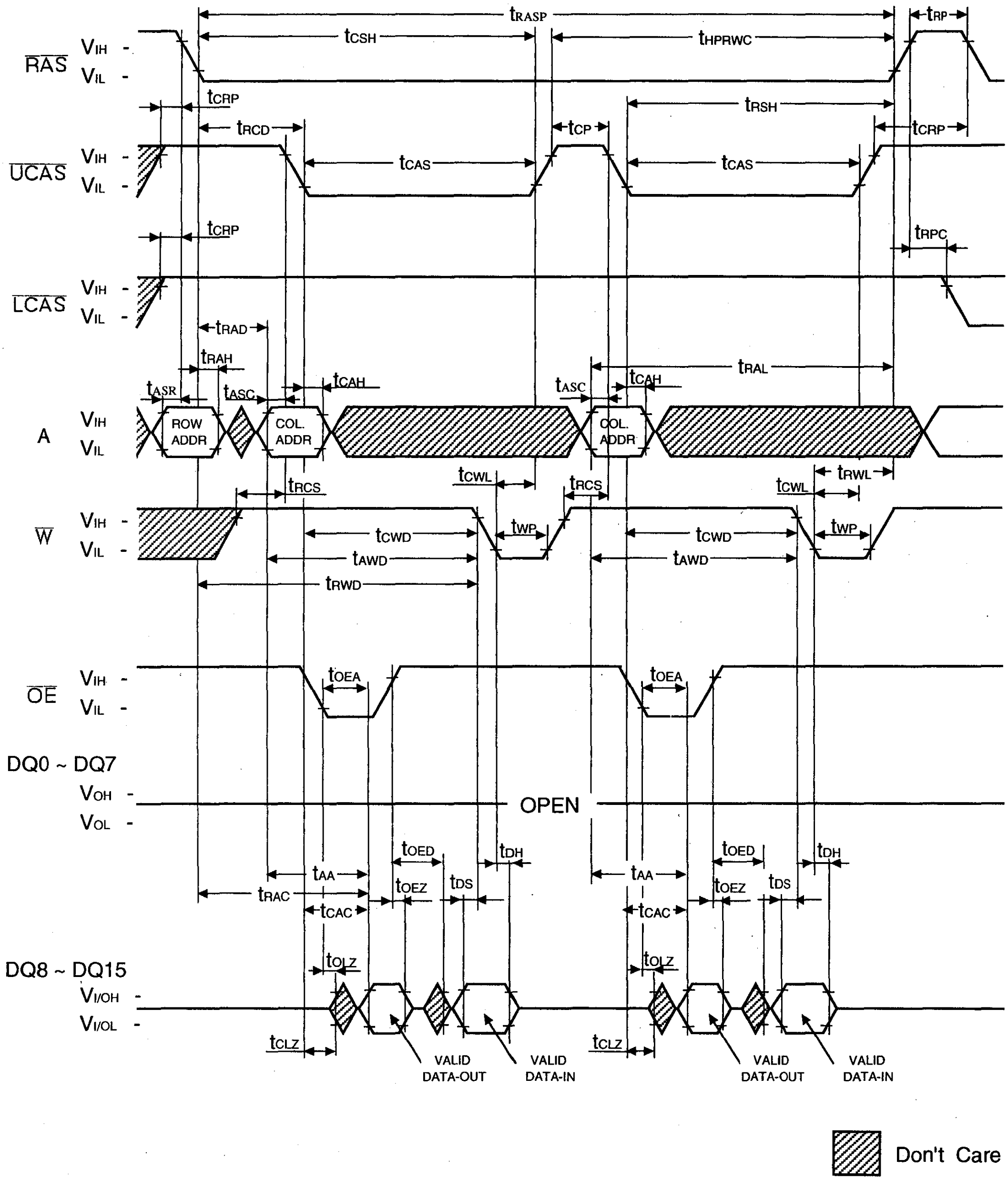
3

HYPER PAGE MODE LOWER-BYTE-READ-MODIFY-WRITE CYCLE

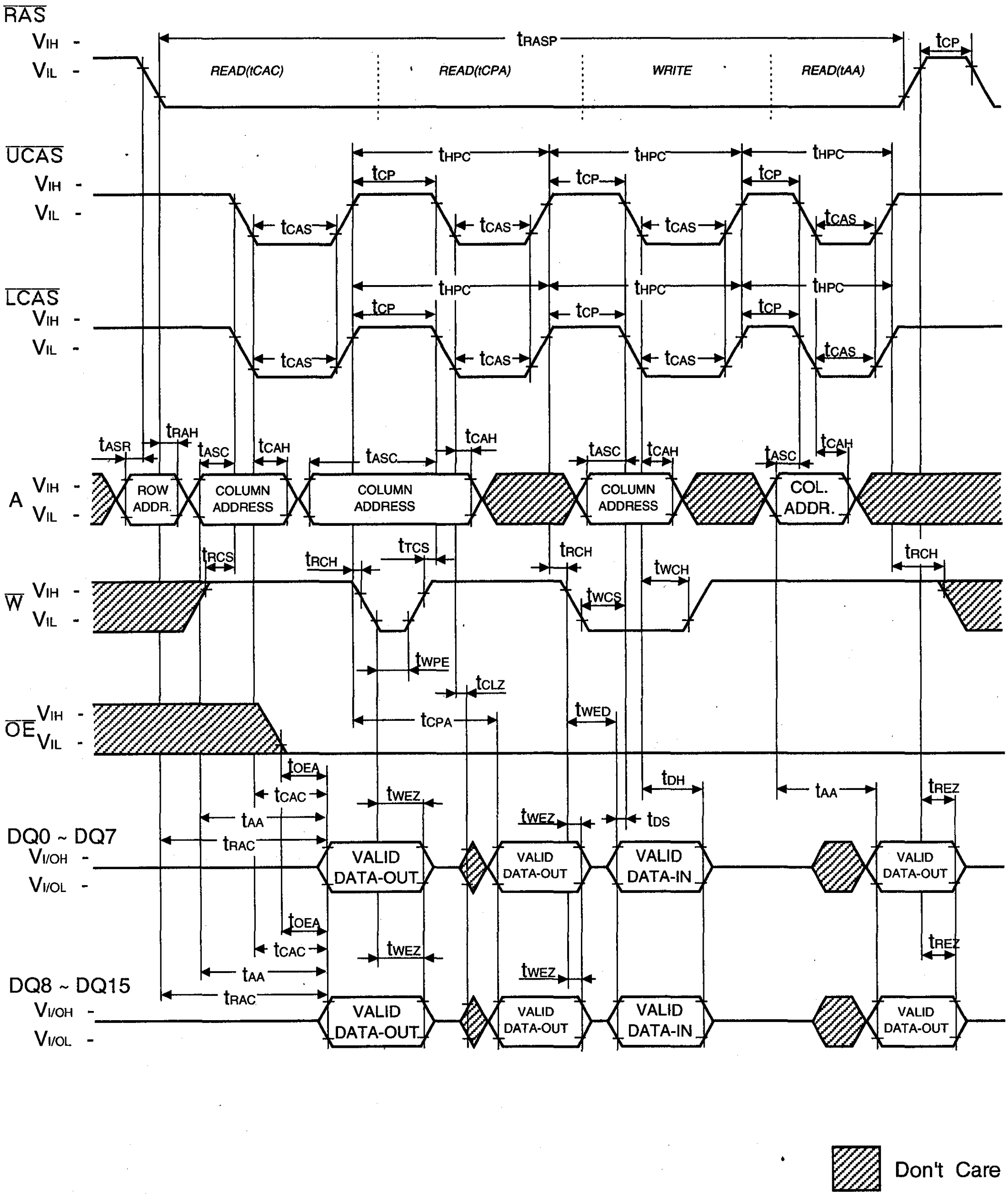


SAMSUNG ELECTRONICS

HYPER PAGE MODE UPPER-BYTE-READ-MODIFY-WRITE CYCLE

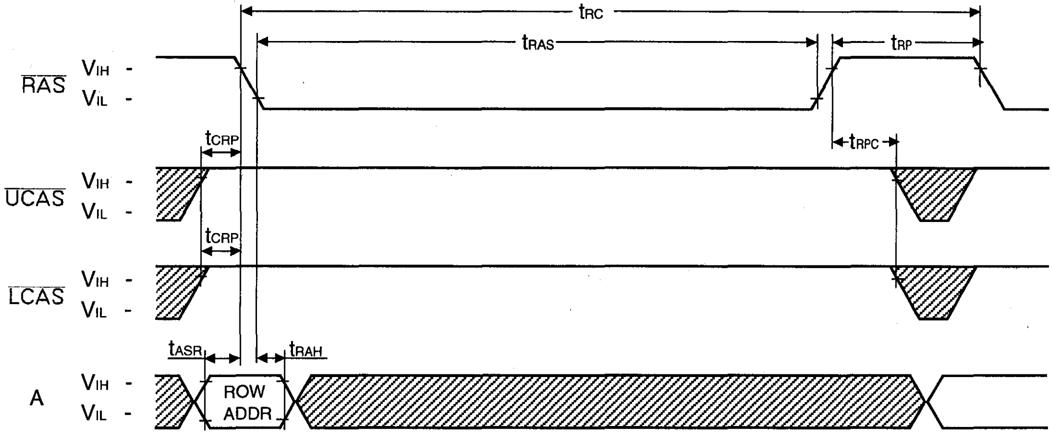


HYPER PAGE READ AND WRITE MIXED CYCLE



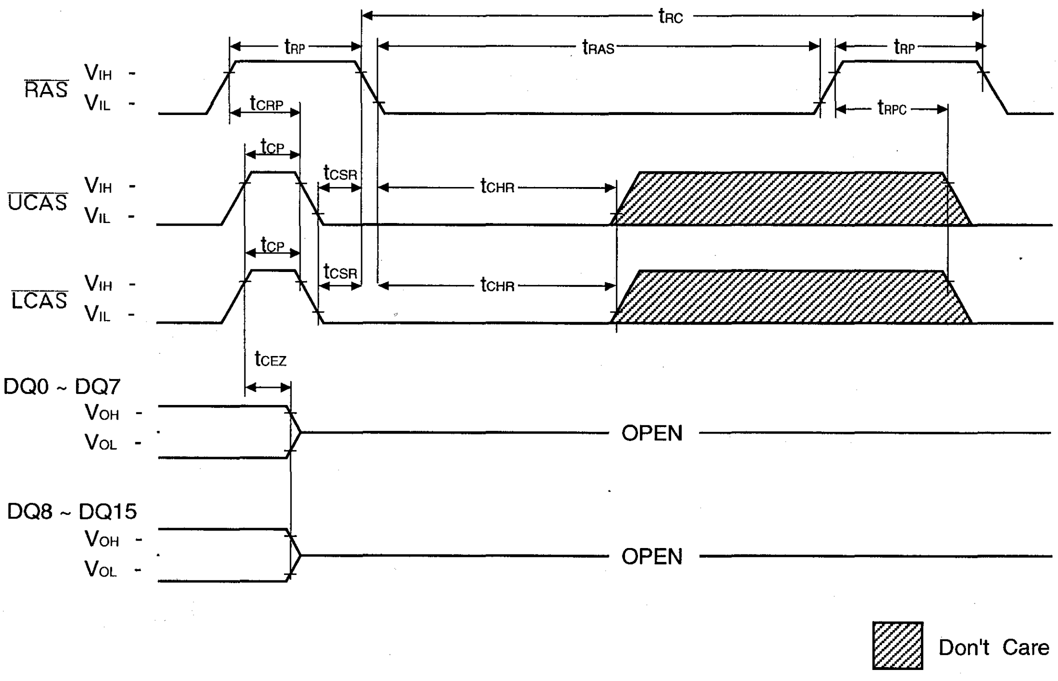
$\overline{RAS}$-ONLY REFRESH CYCLE

NOTE : $\overline{W}$, $\overline{OE}$, D_{IN} = Don't care
D_{OUT} = Open



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE : $\overline{W}$, $\overline{OE}$, A = Don't Care

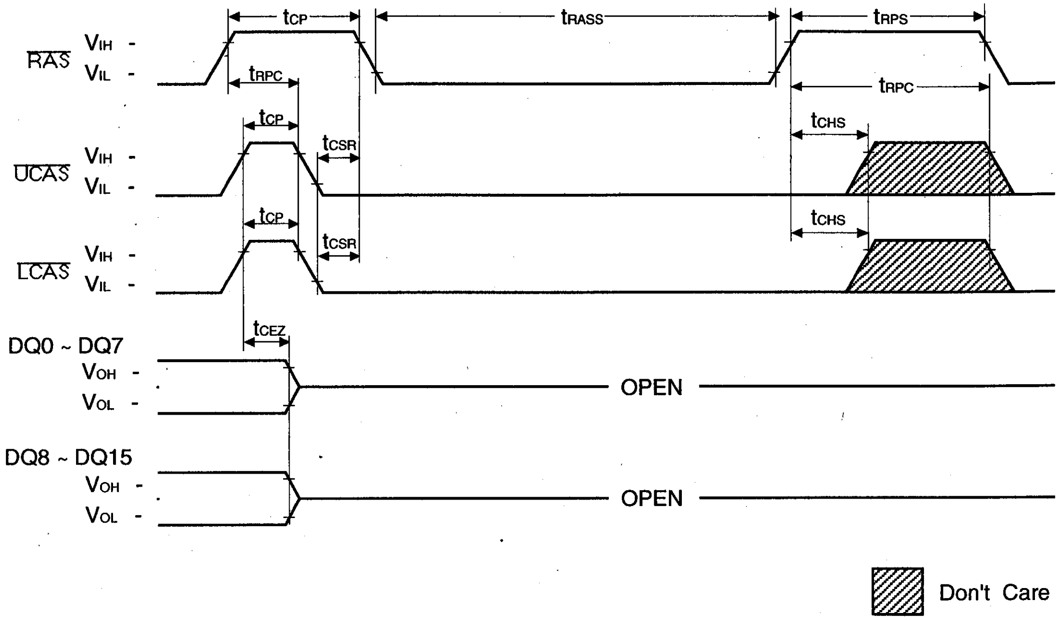


3

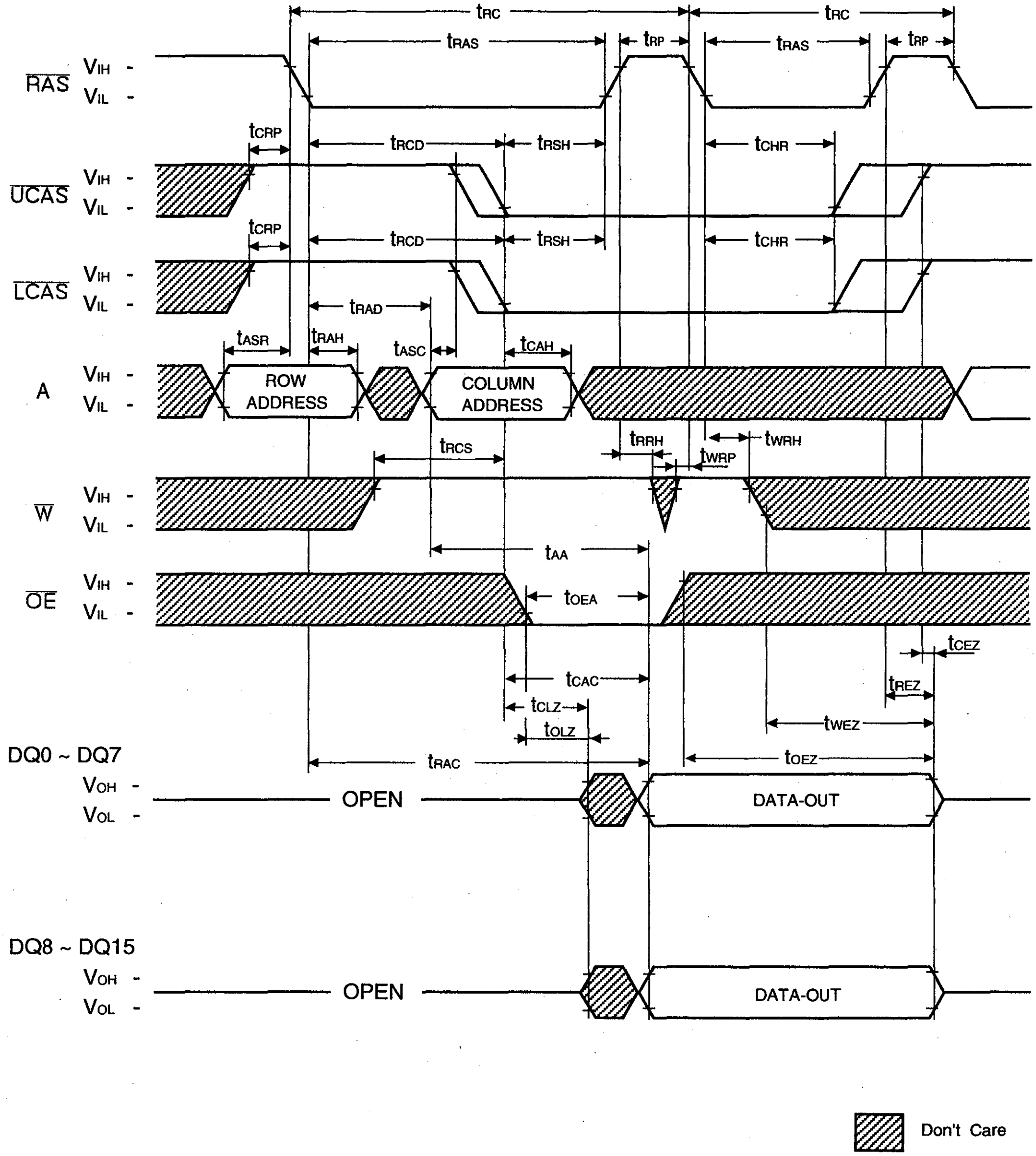
SAMSUNG ELECTRONICS

$\overline{CAS}$-BEFORE-$\overline{RAS}$ SELF REFRESH CYCLE

NOTE : $\overline{W}$, $\overline{OE}$, A = Don't Care



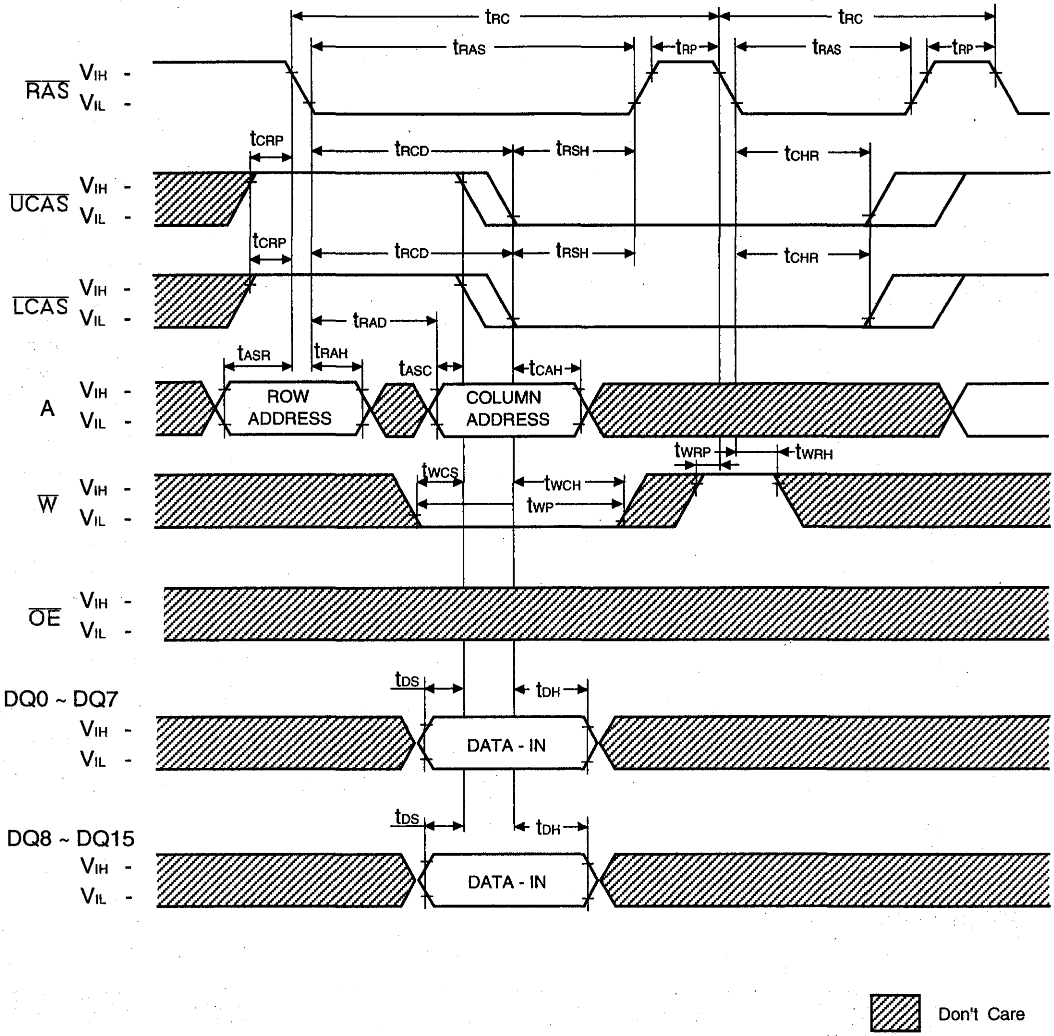
HIDDEN REFRESH CYCLE (READ)



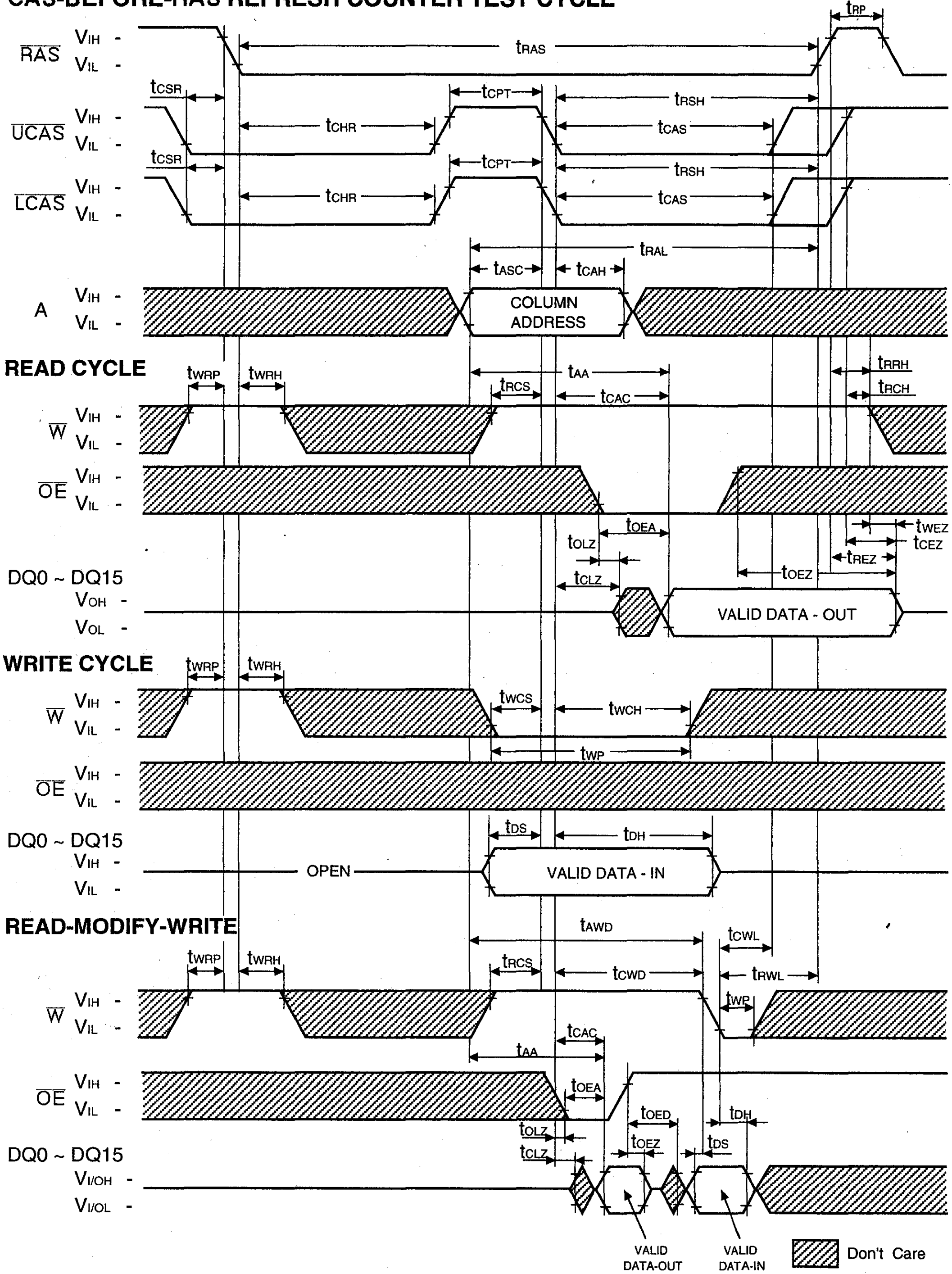
3

HIDDEN REFRESH CYCLE (WRITE)

NOTE : D_{OUT} = OPEN



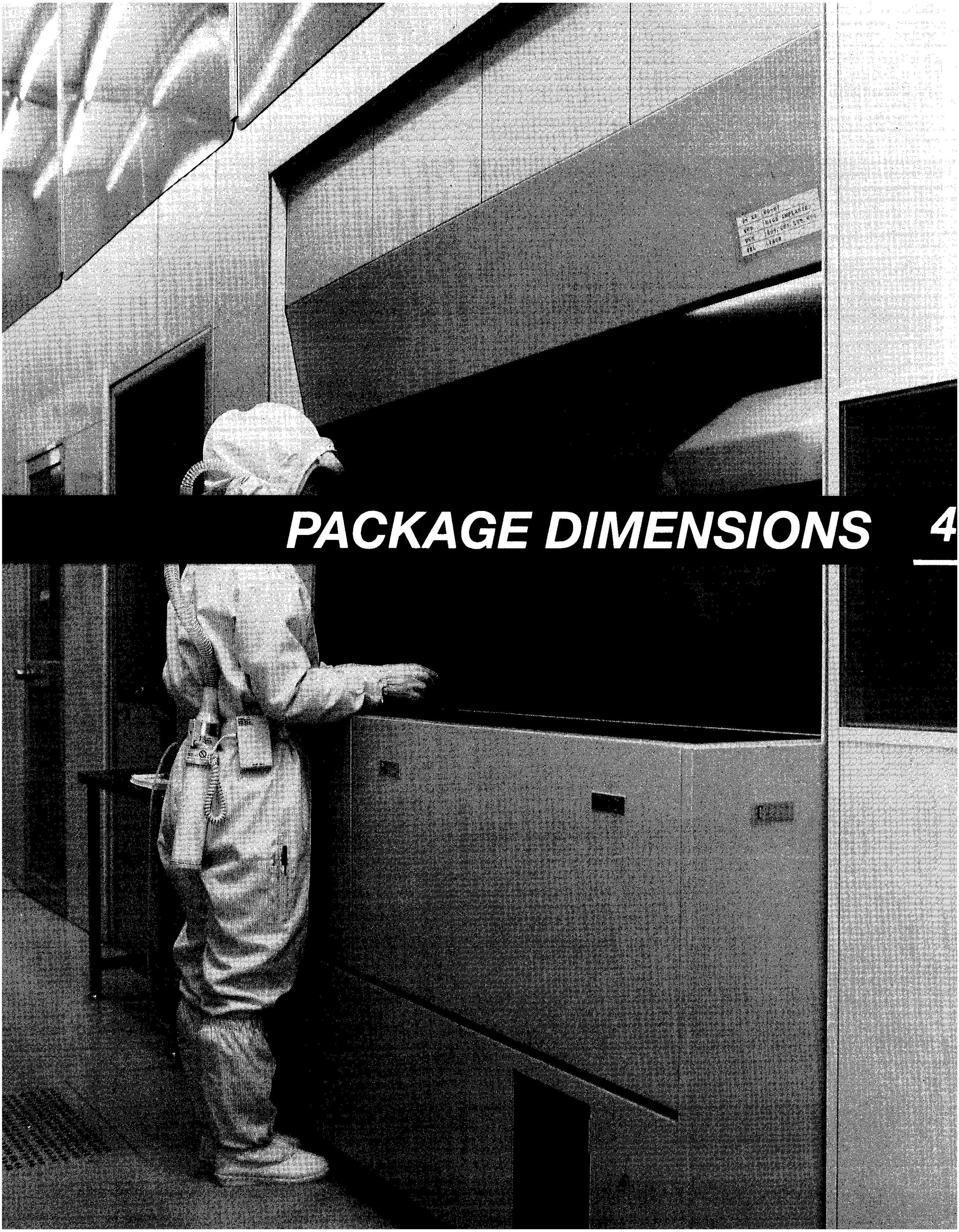
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



3

SAMSUNG ELECTRONICS

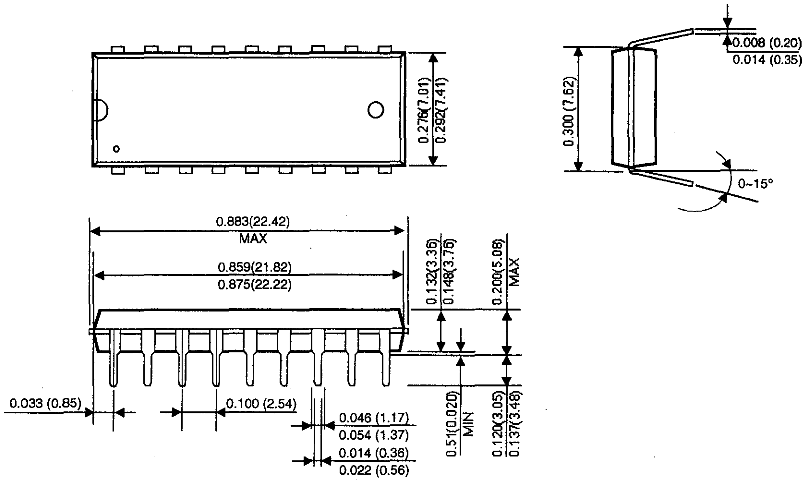
PACKAGE DIMENSIONS 4



PLASTIC DUAL IN-LINE PACKAGE

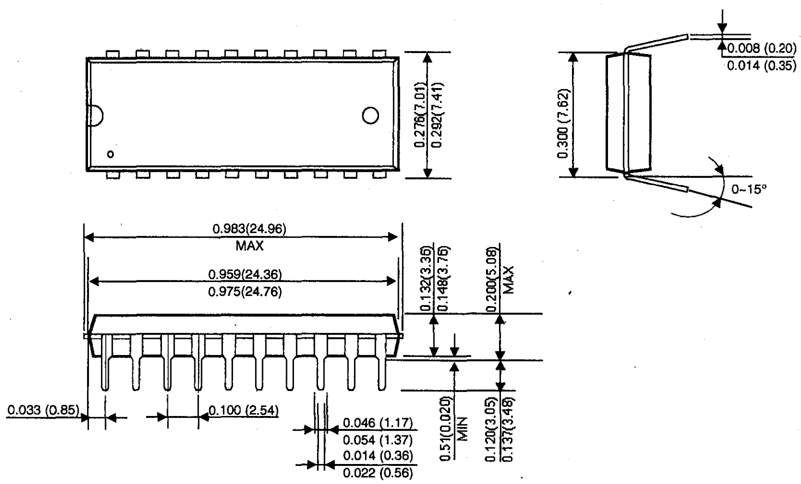
18 DIP 300 mil

Unit : Inches (millimeters)



20 DIP 300 mil

Unit : Inches (millimeters)

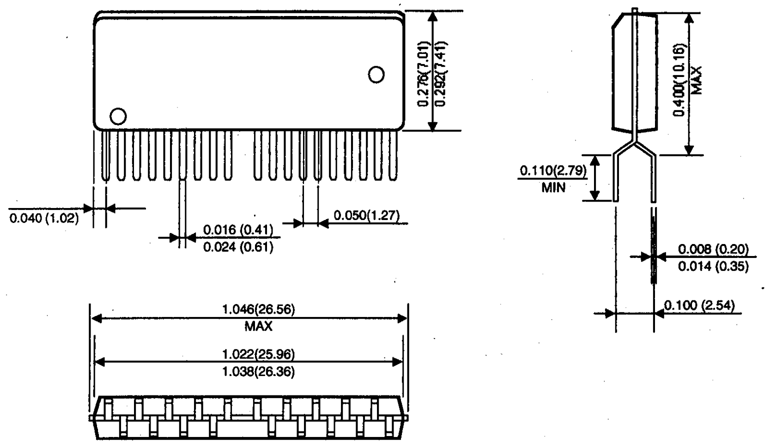


4

PLASTIC ZIGZAG IN-LINE PACKAGE

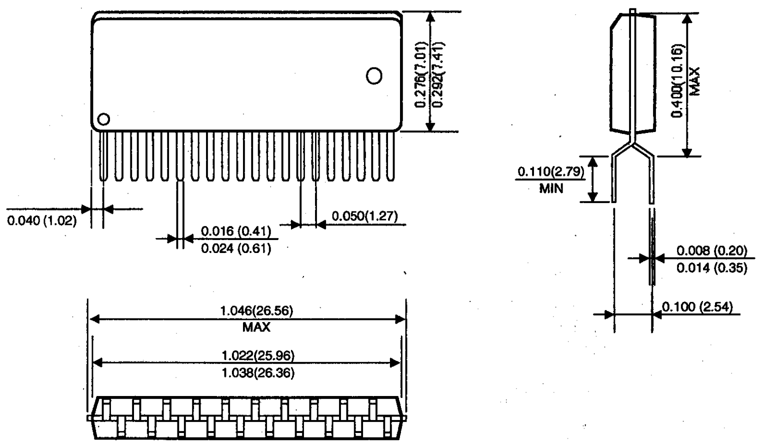
19(20)ZIP 400 mil

Unit : Inches (millimeters)



20 ZIP 400 mil

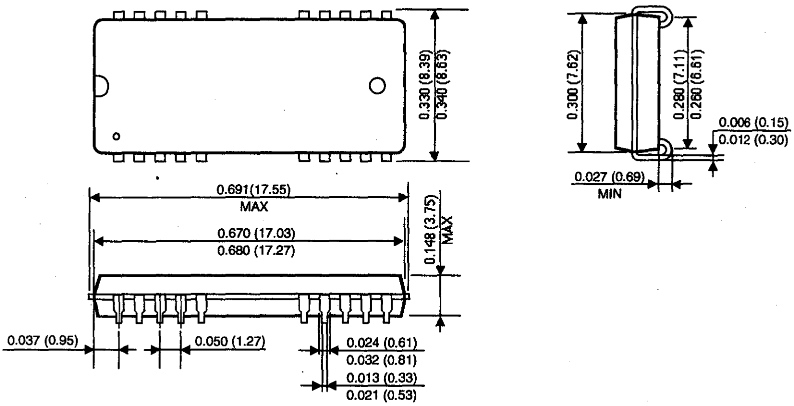
Unit : Inches (millimeters)



PLASTIC SMALL OUT-LINE J-LEAD

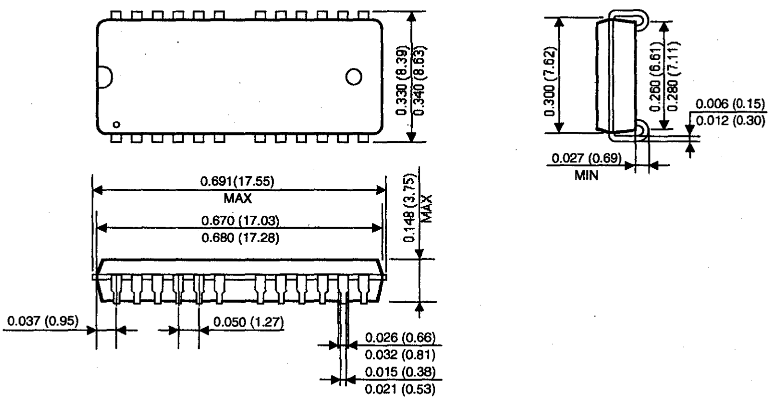
20(26) SOJ 300 mil

Unit : Inches (millimeters)



24(26) SOJ 300 mil

Unit : Inches (millimeters)

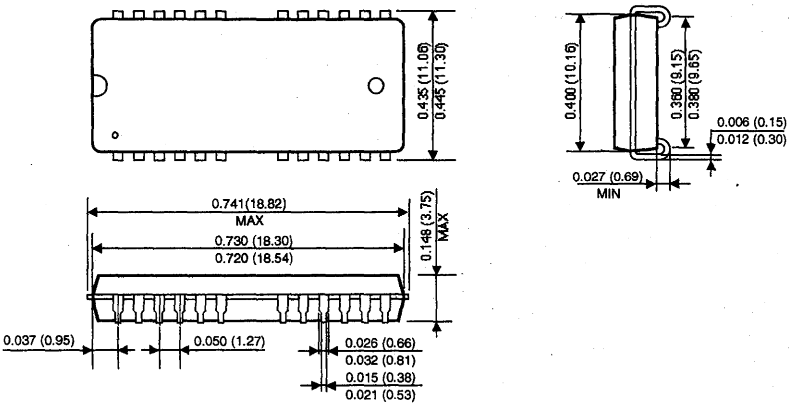


4

PLASTIC SMALL OUT-LINE J-LEAD

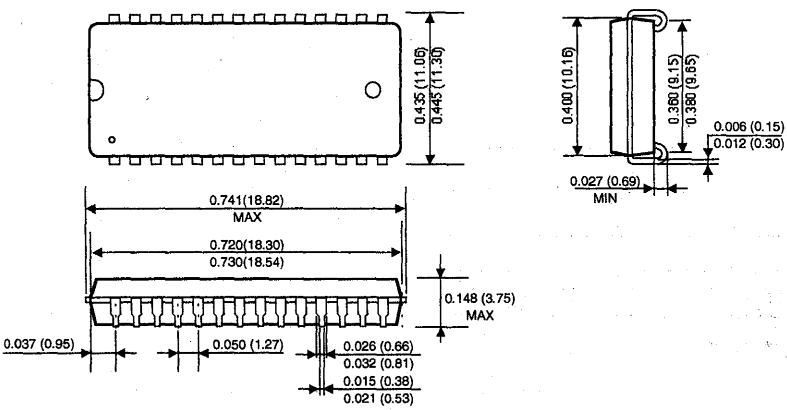
24(28) SOJ 400 mil

Unit : Inches (millimeters)



28 SOJ 400 mil

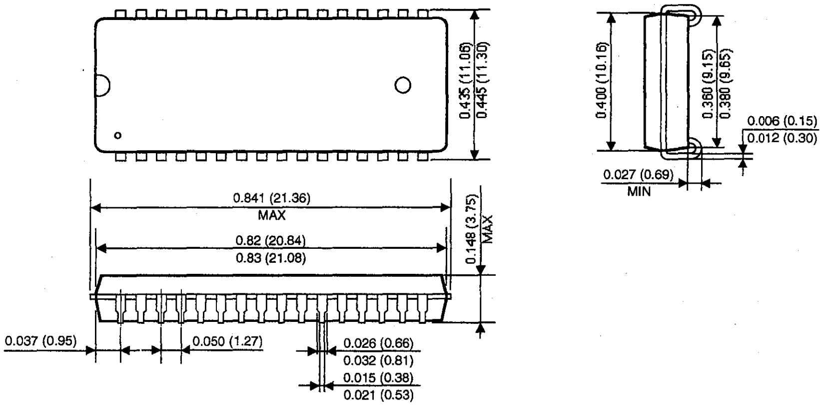
Unit : Inches (millimeters)



PLASTIC SMALL OUT-LINE J-LEAD

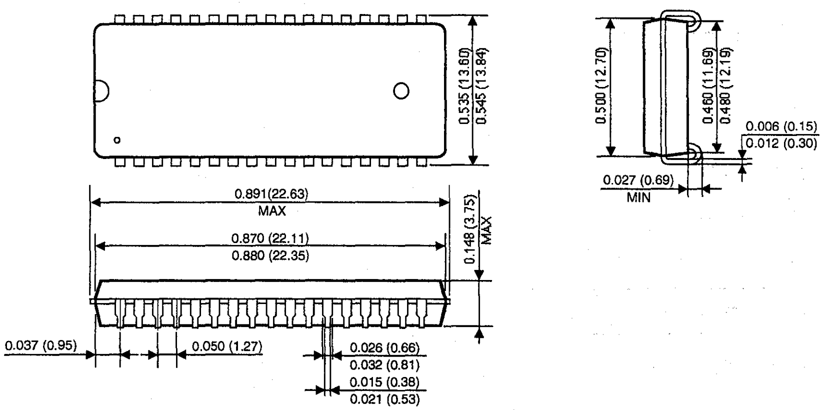
32 SOJ 400 mil

Unit : Inches (millimeters)



34 SOJ 500 mil

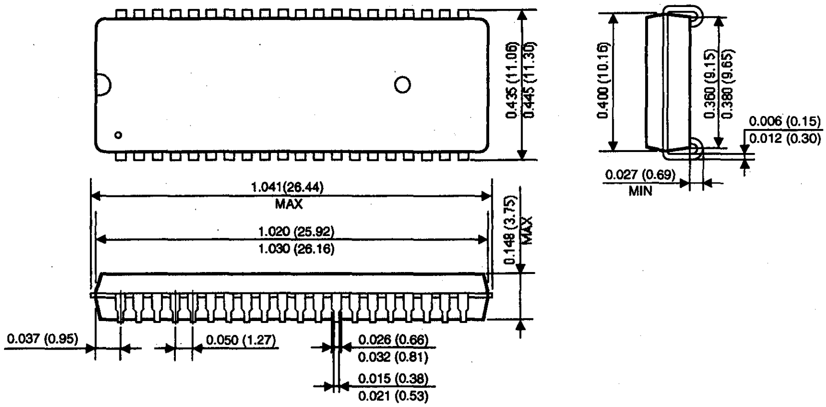
Unit : Inches (millimeters)



PLASTIC SMALL OUT-LINE J-LEAD

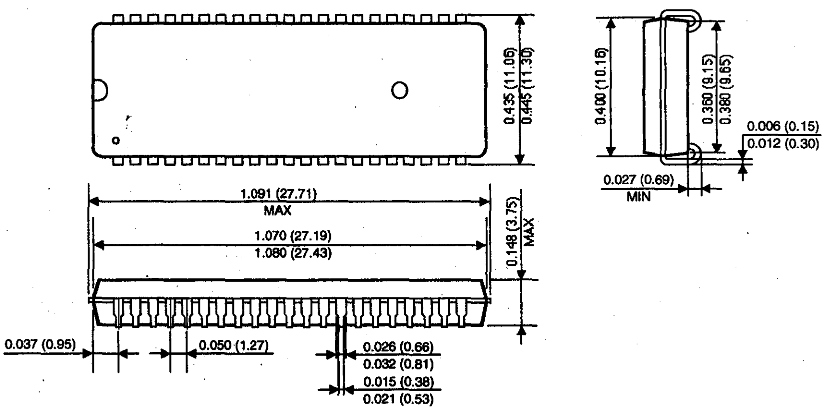
40SOJ 400 mil

Unit : Inches (millimeters)



42 SOJ 400 mil

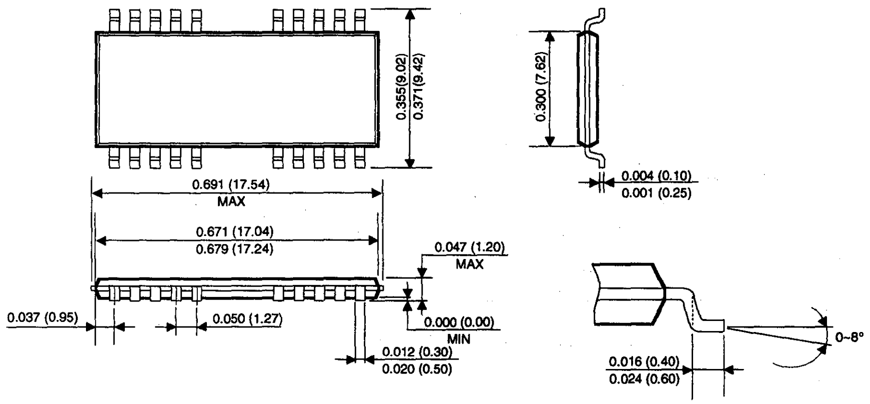
Unit : Inches (millimeters)



PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(II)
(Forward and Reverse Type)

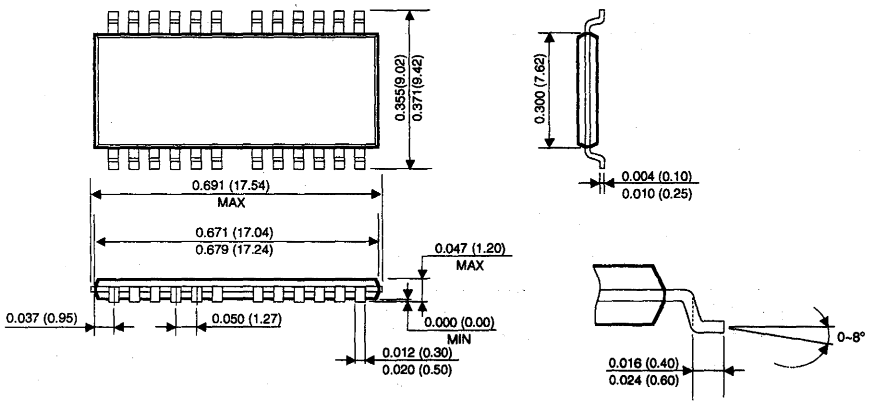
20(26) TSOP(II) 300 mil

Unit : Inches (millimeters)



24(26) TSOP(II) 300 mil

Unit : Inches (millimeters)



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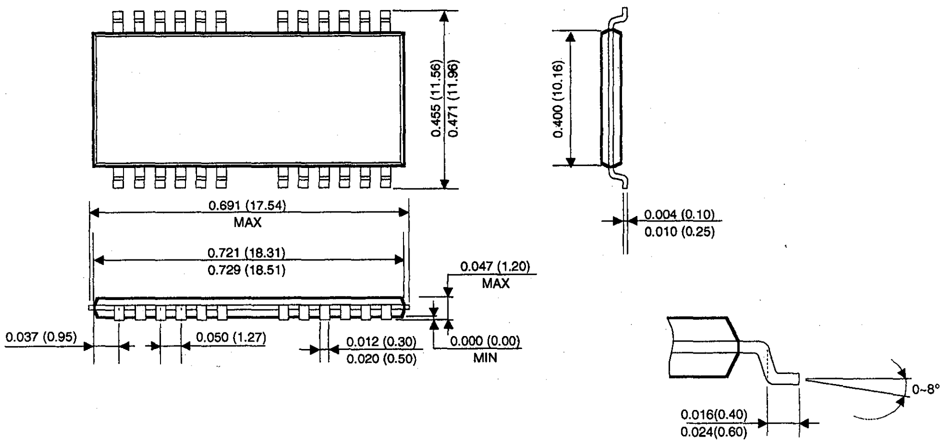
SAMSUNG ELECTRONICS

PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(II) (Forward and Reverse Type)

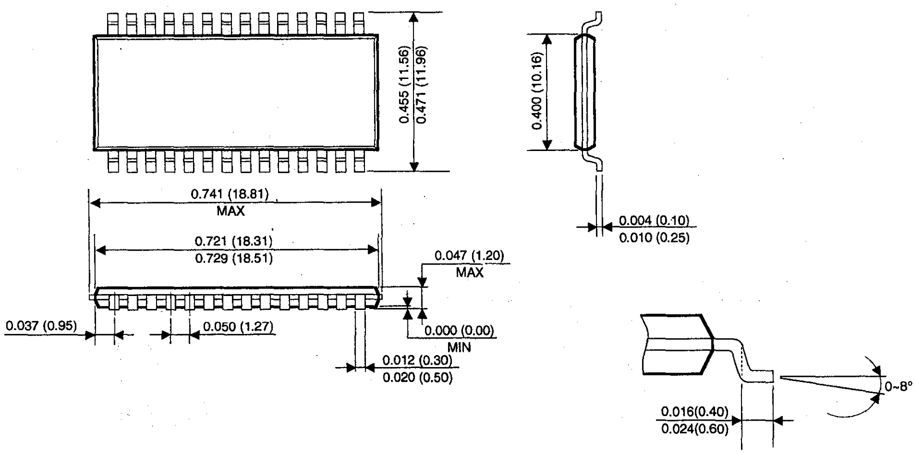
24(28) TSOP(II) 400 mil

Unit : Inches (millimeters)



28 TSOP(II) 400 mil

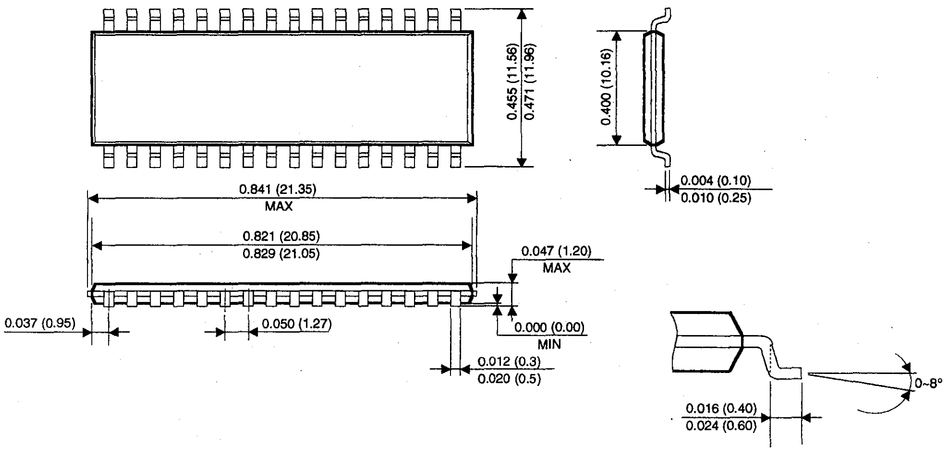
Unit : Inches (millimeters)



PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (II)
(Forward and Reverse Type)

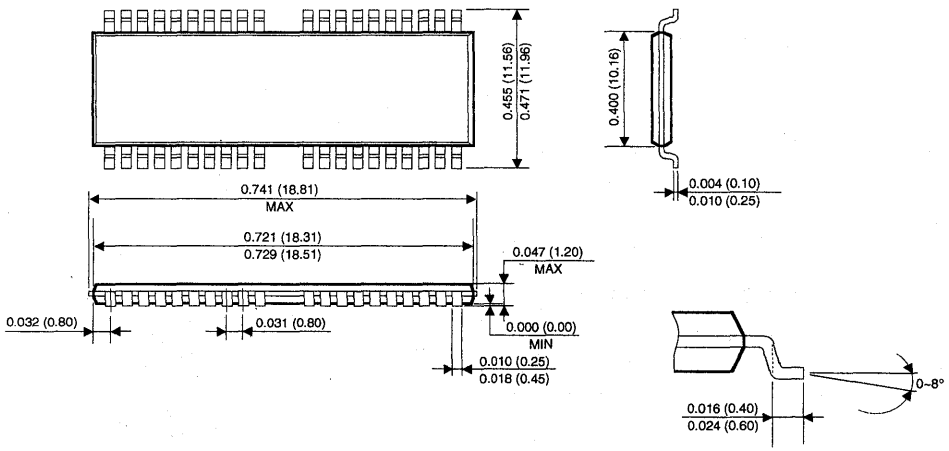
32 TSOP(II) 400 mil

Unit : Inches (millimeters)



40(44) TSOP(II) 400 mil

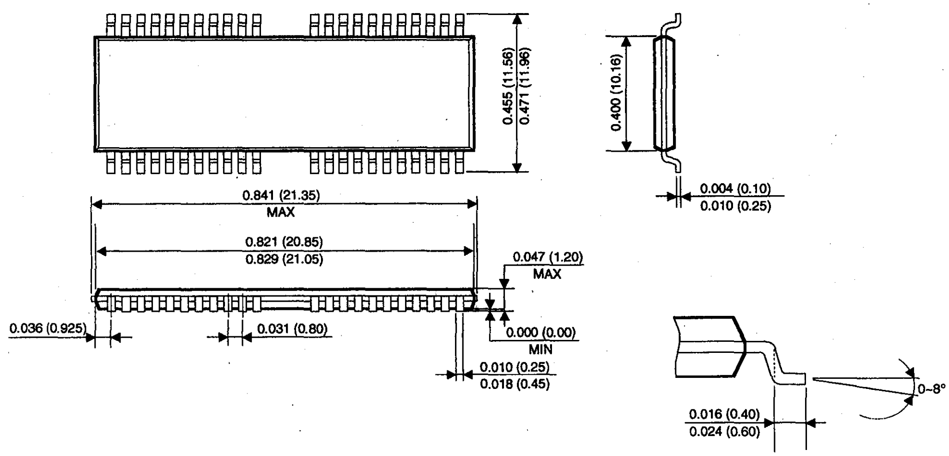
Unit : Inches (millimeters)



PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (II)
(Forward and Reverse Type)

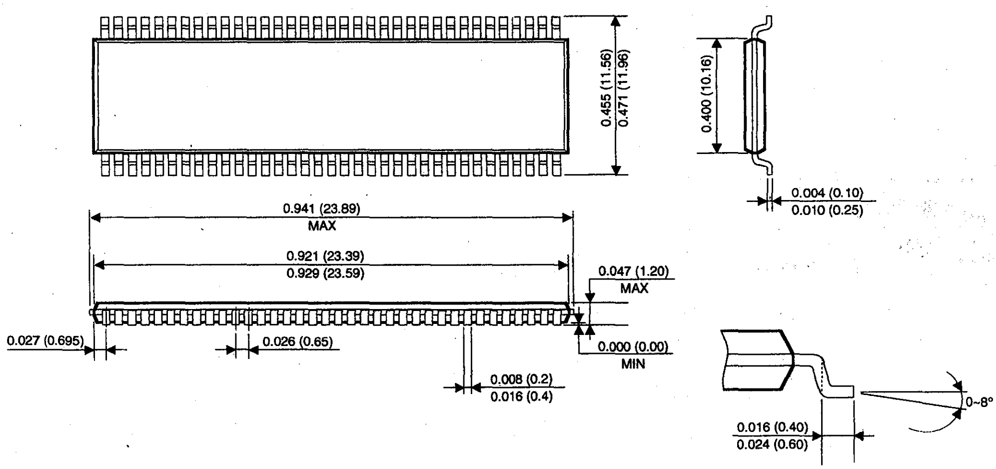
44(50) TSOP(II) 400 mil

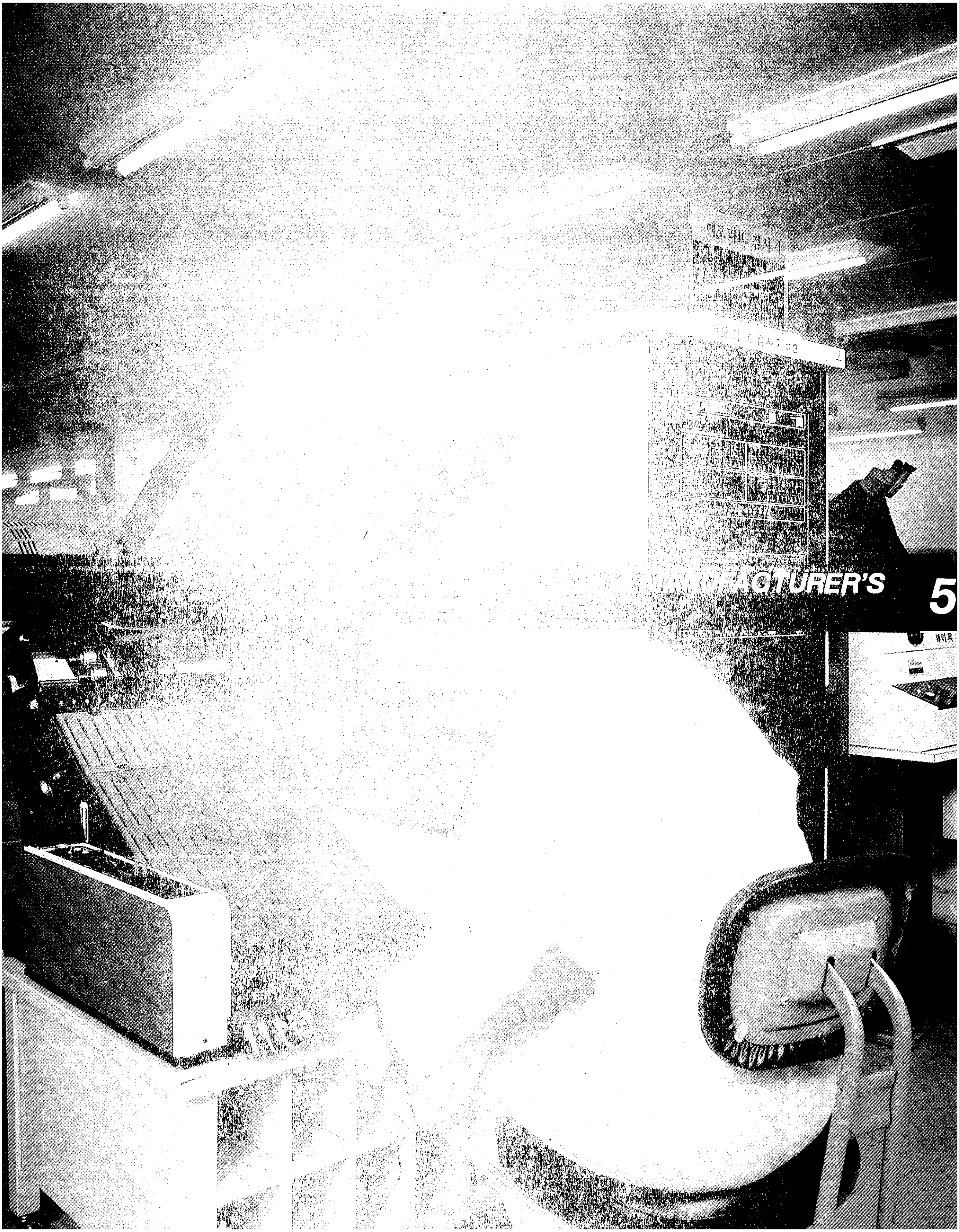
Unit : Inches (millimeters)



70 TSOP(II) 400 mil

Unit : Inches (millimeters)

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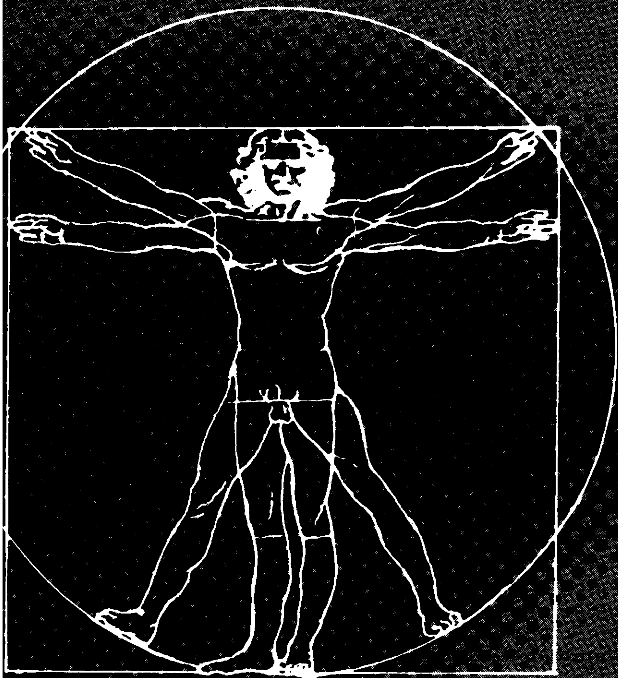

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