

# MJD5731

## High Voltage PNP Silicon Power Transistors

Designed for line operated audio output amplifier, SWITCHMODE power supply drivers and other switching applications.

### Features

- PNP Complements to the MJD47 thru MJD50 Series
- Epoxy Meets UL 94 V-0 @ 0.125 in
- These Devices are Pb-Free and are RoHS Compliant

### MAXIMUM RATINGS

Rating	Symbol	Max	Unit
Collector-Emitter Voltage	$V_{CEO}$	350	Vdc
Emitter-Base Voltage	$V_{EB}$	5	Vdc
Collector Current – Continuous	$I_C$	1.0	Adc
Collector Current – Peak	$I_{CM}$	3.0	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	15 0.12	W W/ $^\circ\text{C}$
Total Power Dissipation (Note 1) @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	1.56 0.0125	W W/ $^\circ\text{C}$
Unclamped Inductive Load Energy (See Figure 10)	E	20	mJ
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$
ESD – Human Body Model	HBM	3B	V
ESD – Machine Model	MM	C	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. These ratings are applicable when surface mounted on the minimum pad sizes recommended.

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	8.33	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	80	$^\circ\text{C}/\text{W}$
Lead Temperature for Soldering	$T_L$	260	$^\circ\text{C}$

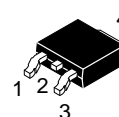
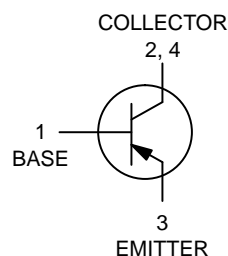
2. These ratings are applicable when surface mounted on the minimum pad sizes recommended.



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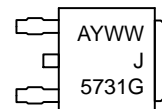
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## SILICON POWER TRANSISTORS 1.0 AMPERE 350 VOLTS, 15 WATTS



DPAK  
CASE 369C  
STYLE 1

### MARKING DIAGRAM



A = Assembly Location  
Y = Year  
WW = Work Week  
J5731 = Device Code  
G = Pb-Free Package

### ORDERING INFORMATION

Device	Package	Shipping†
MJD5731T4G	DPAK (Pb-Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MJD5731

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector-Emitter Sustaining Voltage (Note 3) ( $I_C = 30\text{ mAdc}$ , $I_B = 0$ )	$V_{CEO(sus)}$	350	–	Vdc
Collector Cutoff Current ( $V_{CE} = 250\text{ Vdc}$ , $I_B = 0$ )	$I_{CEO}$	–	0.1	mAdc
Collector Cutoff Current ( $V_{CE} = 350\text{ Vdc}$ , $V_{BE} = 0$ )	$I_{CES}$	–	0.01	mAdc
Emitter Cutoff Current ( $V_{BE} = 5.0\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	–	0.5	mAdc
<b>ON CHARACTERISTICS (Note 3)</b>				
DC Current Gain ( $I_C = 0.3\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ ) ( $I_C = 1.0\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ )	$h_{FE}$	30 10	175 –	–
Collector-Emitter Saturation Voltage ( $I_C = 1.0\text{ Adc}$ , $I_B = 0.2\text{ Adc}$ )	$V_{CE(sat)}$	–	1.0	Vdc
Base-Emitter On Voltage ( $I_C = 1.0\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ )	$V_{BE(on)}$	–	1.5	Vdc
<b>DYNAMIC CHARACTERISTICS</b>				
Current Gain – Bandwidth Product ( $I_C = 0.2\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ , $f = 2.0\text{ MHz}$ )	$f_T$	10	–	MHz
Small-Signal Current Gain ( $I_C = 0.2\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ , $f = 1.0\text{ kHz}$ )	$h_{fe}$	25	–	–

3. Pulse Test: Pulse Width  $\leq 300\text{ }\mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

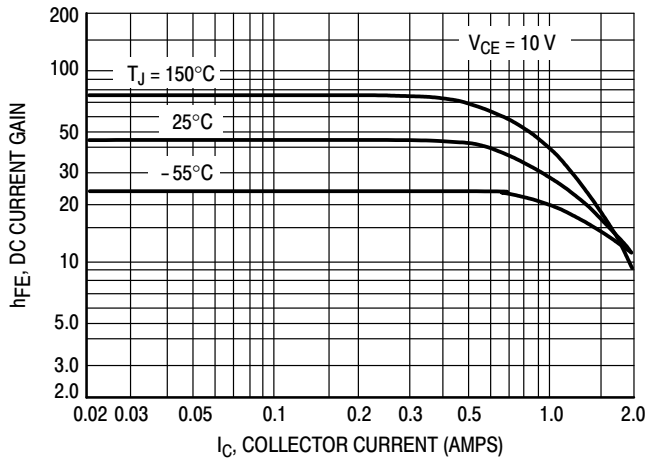


Figure 1. DC Current Gain

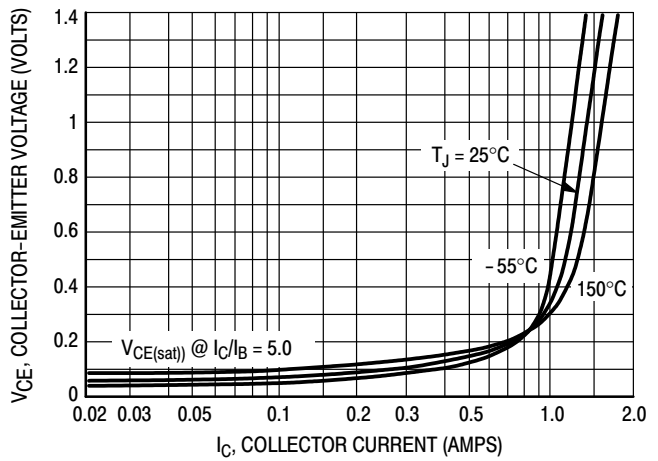


Figure 2. Collector-Emitter Saturation Voltage

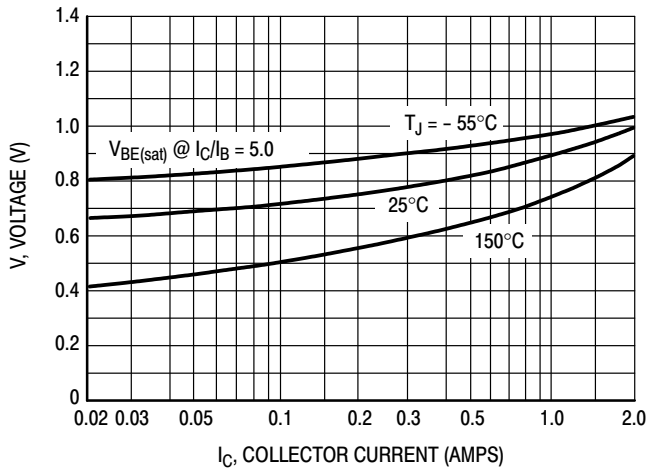


Figure 3. Base-Emitter Voltage

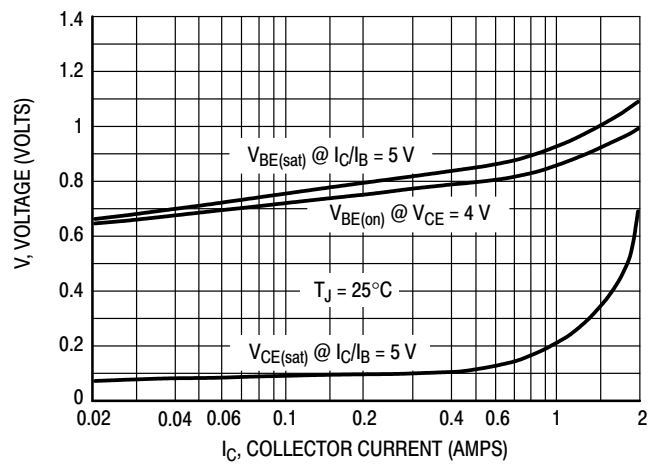


Figure 4. "On" Voltages

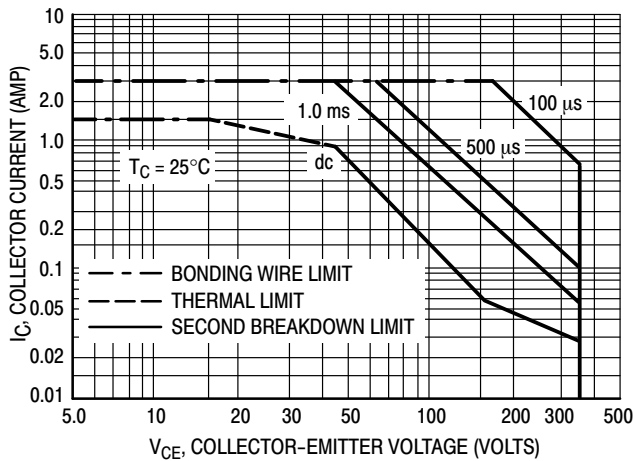


Figure 5. Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 6. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

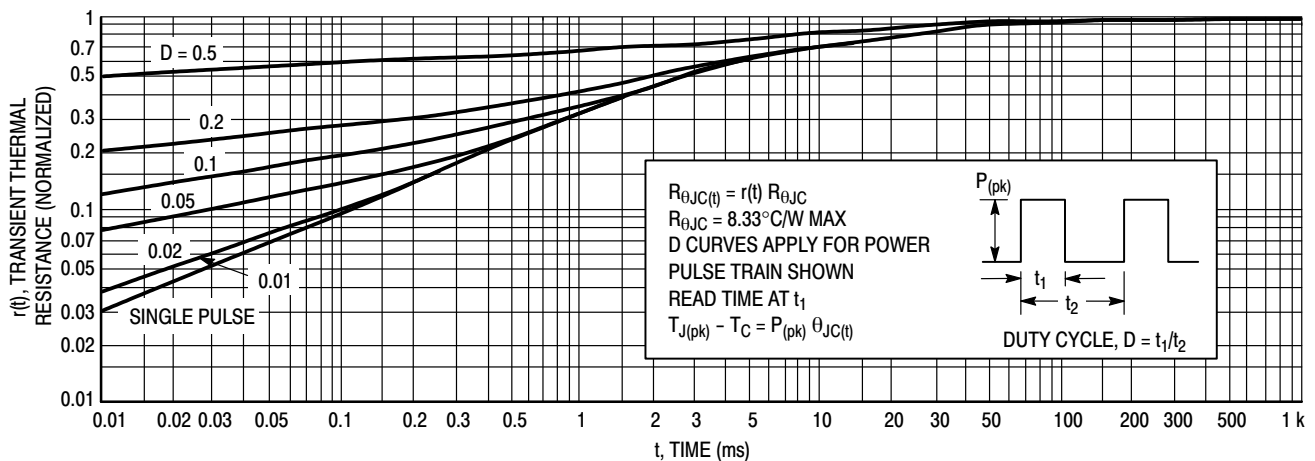
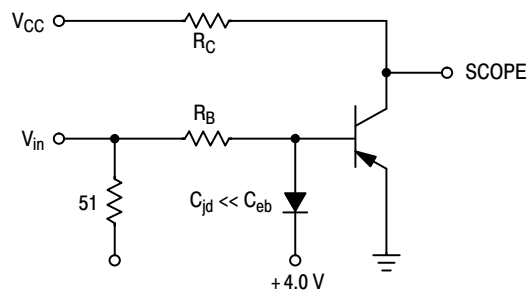
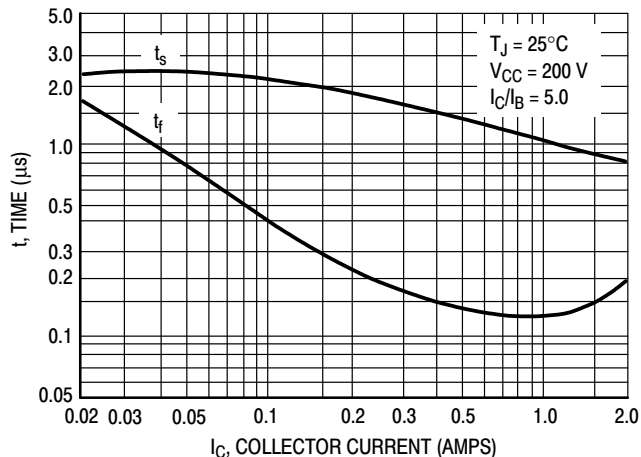


Figure 6. Thermal Response

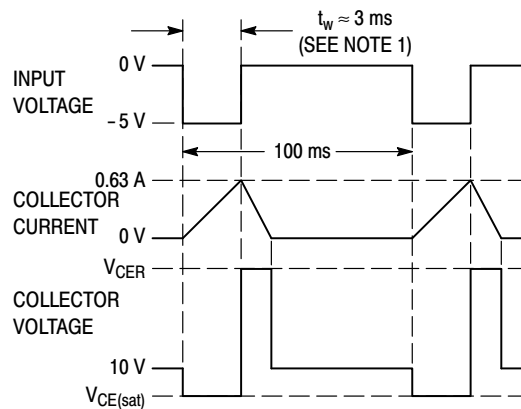


### Figure 7. Switching Time Equivalent Circuit



### Figure 8. Turn-On Resistive Switching Times

### Figure 9. Resistive Turn-Off Switching Times



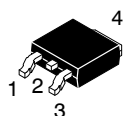
### Figure 10. Inductive Load Switching

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

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ON



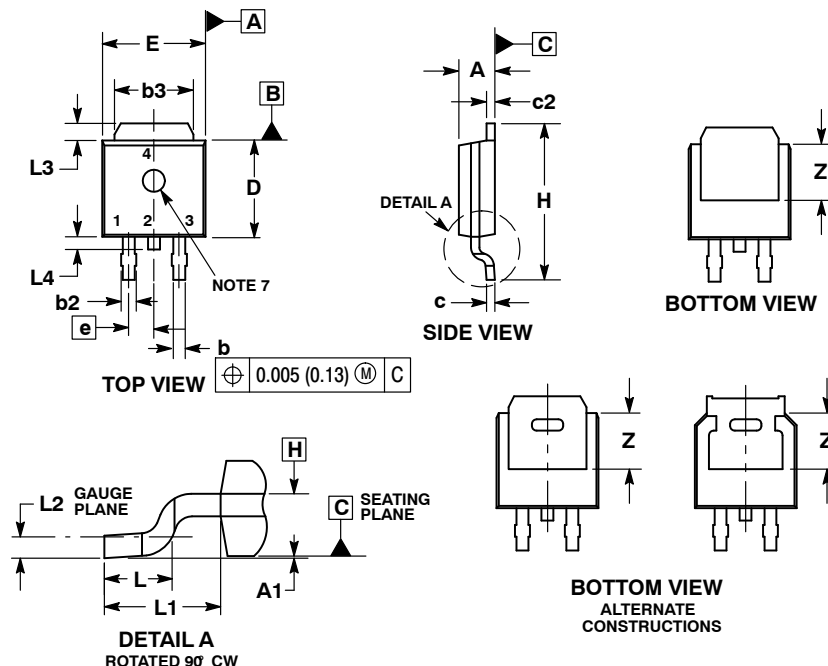
SCALE 1:1

### DPAK (SINGLE GAUGE)

#### CASE 369C

#### ISSUE F

DATE 21 JUL 2015

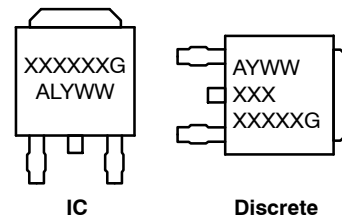


#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114 REF		2.90 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

### GENERIC MARKING DIAGRAM\*

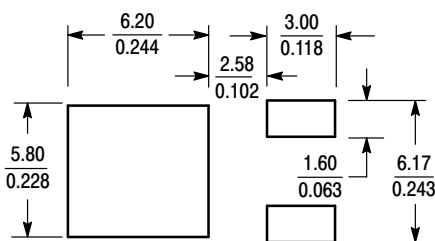


XXXXXX = Device Code  
 A = Assembly Location  
 L = Wafer Lot  
 Y = Year  
 WW = Work Week  
 G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking.

- STYLE 1:**  
 PIN 1. BASE  
 2. COLLECTOR  
 3. EMITTER  
 4. COLLECTOR
- STYLE 2:**  
 PIN 1. GATE  
 2. DRAIN  
 3. SOURCE  
 4. DRAIN
- STYLE 3:**  
 PIN 1. ANODE  
 2. CATHODE  
 3. ANODE  
 4. CATHODE
- STYLE 4:**  
 PIN 1. CATHODE  
 2. ANODE  
 3. GATE  
 4. ANODE
- STYLE 5:**  
 PIN 1. GATE  
 2. ANODE  
 3. CATHODE  
 4. ANODE
- STYLE 6:**  
 PIN 1. MT1  
 2. MT2  
 3. GATE  
 4. MT2
- STYLE 7:**  
 PIN 1. GATE  
 2. COLLECTOR  
 3. EMITTER  
 4. COLLECTOR
- STYLE 8:**  
 PIN 1. N/C  
 2. CATHODE  
 3. ANODE  
 4. CATHODE
- STYLE 9:**  
 PIN 1. ANODE  
 2. CATHODE  
 3. RESISTOR ADJUST  
 4. CATHODE
- STYLE 10:**  
 PIN 1. CATHODE  
 2. ANODE  
 3. CATHODE  
 4. ANODE

### SOLDERING FOOTPRINT\*



SCALE 3:1 (mm inches)

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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