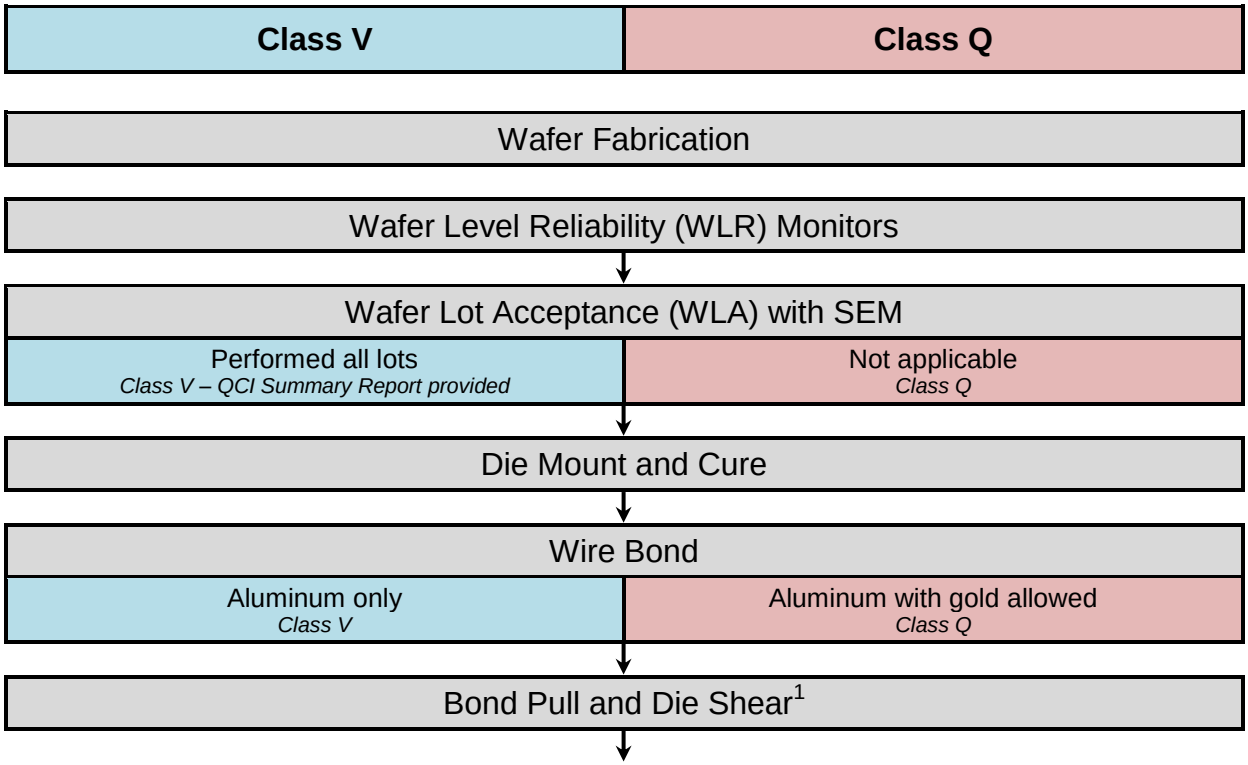
QML flow, its importance, and obtaining lot information

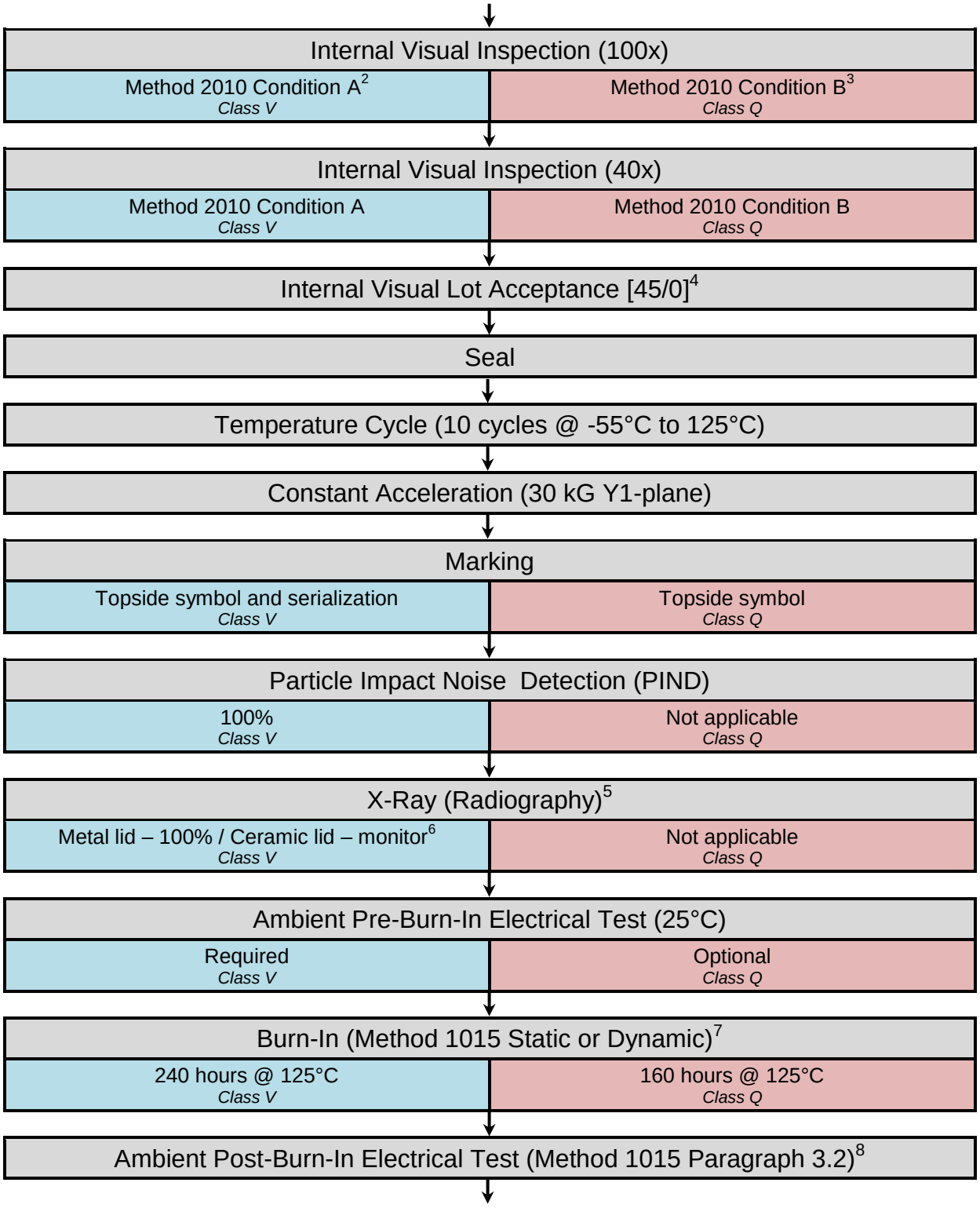
Texas Instruments

Qualifying and manufacturing a space or military part is an important step in verifying that the device will withstand the harsh environment and/or radiation in space, and will also operate as intended over the duration of a mission. Texas Instruments is a certified manufacturer on the Defense Logistics Agency Land and Maritime (DLA) list of Qualified Manufacturers List (QML) for both QML Class V (space) and QML Class Q (military) microcircuits. This QML manufacturing flow is a single controlled baseline that follows military standard MIL-PRF-38535 in accordance with MIL-STD-883 as a means to ensure product quality and reliability, from design to fabrication. QML lots ship with a Certificate of Conformance per MIL-PRF-38535, a Processing Conformance Report (PCR) summarizing traceability and testing performed, and with Quality Conformance Inspection (QCI) reports available (see Appendix I). For examples of various QCI reports, see Appendix II. (For more information regarding TI's optimization of certain QML processes per MIL-PRF-38535, refer to QML Process Optimizations.) With over 50% of Texas Instruments' fabs QML Class V certified, TI is a trusted partner to deliver high quality, reliable products for all space and military application needs.

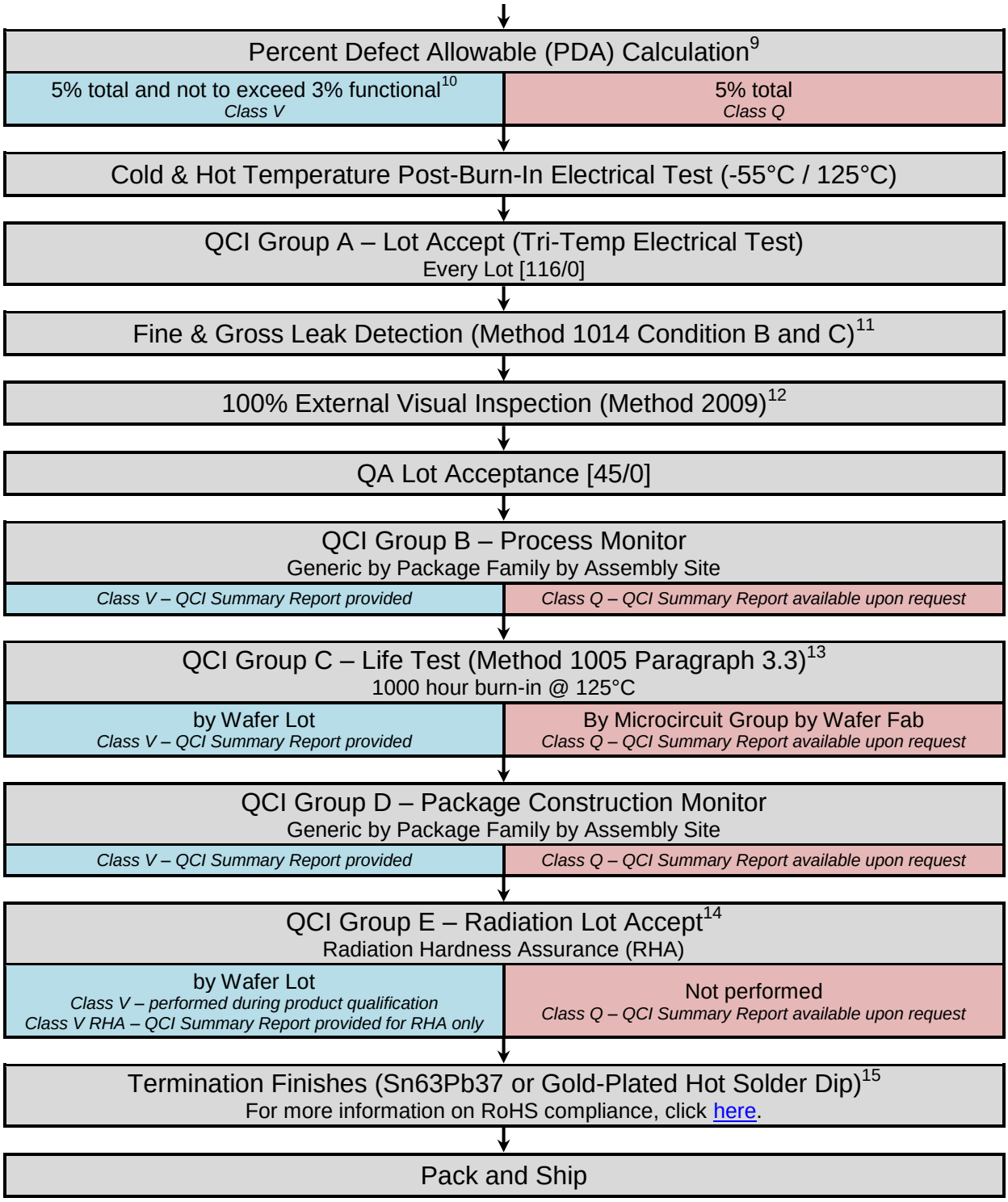
The QML flow is outlined below with Class V in the blue on the left and Class Q on the right in red.



[1] Bond pull and die shear is an inline process monitor for both Class V and Class Q



[2] Method 2010 Condition A is an internal visual test to check internal materials, construction, and workmanship of microcircuits per MIL-STD-883
[3] Method 2010 Condition B is an internal visual test to check internal materials, construction, and workmanship of microcircuits per MIL-STD-883
[4] [45/0] means 45 samples tested with 0 fails
[5] CSAM can be used as an alternative to X-ray on some devices
[6] X-ray for ceramic lids is an optimization; otherwise it is required at 100%
[7] Method 1015 is a burn-in test performed to screen out marginal devices per MIL-STD-883
[8] Method 1015 paragraph 3.2 states post burn-in measurement must be completed within 96 hours after removal of the devices from the specified burn-in test condition and must consist of all 25°C DC parameter measurements per MIL-STD-883



[9] PDA includes both parametric and DC functional reject fails after burn-in; if there is >5% total reject fails, the entire lot is scrapped
[10] For Class V, the lot is scrapped if there is >5% total reject fails and/or if there is >3% functional reject fails; in addition, failure analysis will be performed on burn-in screen failures to a degree sufficient to establish failure mode
[11] Method 1014 is a test designed to determine the hermeticity of the seal of the microelectronic device per MIL-STD-883
[12] Method 2009 is a test method to verify workmanship of packaged devices per MIL-STD-883
[13] Method 1005 paragraph 3.3 states the test must be completed with 96 hours of removal from burn-in oven; if measurements cannot be completed within 96 hours, devices must return to burn-in oven for 24 hours to establish a new 96 hour electrical test window per MIL-STD-883
[14] For Class V devices, the Radiation Lot Accept test occurs for each qualification; for Class V RHA devices, the Radiation Lot Accept test occurs for each wafer lot
[15] Depending on the device, the hot solder dip can be done at different places in the flow

Appendix I

Texas Instruments provides Certificate of Conformance documents for all QML lots. Additionally, TI automatically ships QCI Summary Reports with all Class V lots and may be ordered for Class Q lots. All PCR and QCI documents may be downloaded from the TI website, https://qci.ext.ti.com/.

Document	Class V	Class Q
Certificate of Conformance per MIL-PRF-38535	Yes	Yes
Processing Conformance Report (example): a) Assembly lot traceability b) Wafer lot traceability c) 100% screen performed d) QCI Group A testing e) QCI Group B testing f) QCI Group C testing g) QCI Group E testing (QMLV RHA only) h) QCI WLA testing (QMLV only)	Yes	Yes
QCI Group B Summary Report (example)	Yes	Upon request
QCI Group C Summary Report (example)	Yes	Upon request
QCI Group D Summary Report (example)	Yes	Upon request
QCI Group E Summary Report (example)	RHA only	N/A
QCI WLA Summary Report (example)	Yes	N/A

To obtain copies of QML lot specific documents, follow the instructions below.

1. Log on to https://qci.ext.ti.com/ using a MYTI account. For first time users, an additional two-factor authorization is required. (For any difficulties in logging on, please contact qci_2fa@list.ti.com.)
2. To download a QCI Summary Report (Groups B, C, D, E, or WLA):
   a. Under ‘Reports’ tab, highlight ‘Lot Test Summary,’ and click on desired report
   b. Enter either the ‘PCR Lot Number’ (listed as Q.C. Reference number in PCR report) or the ‘Group Lot Number’ (listed as QA Lot Number in Certificate of Conformance) into the corresponding box
   c. Click ‘Show Report’
3. There is an additional Radiation Hardness Assured (RHA) Lot Acceptance Report option for RHA lots.
   a. At bottom of screen, scroll to ‘File Attachment’ to access the report
4. To download the PCR:
   a. Under ‘Reports’ tab, click on ‘PCR Listing’
   b. Enter the ‘PCR Lot Number’ and click ‘Show Report’
5. For assistance, click ‘Help’ in upper right corner of screen

Appendix II

The following QCI Summary Report examples refer to part number TPS7A4501-RHA with PCR Lot Number 4015079. Reports pulled from https://qci.ext.ti.com/ will look like these.

Example – Processing Conformance Report

Texas Instruments Incorporated
Military Products Department
Military High Reliability Integrated Circuits
Processing Conformance Report

Device Type: **5962R1222403VXC**
SMD: **5962R1222403VXC**
Processing Type: **RHA**
PCR Lot Number: **4015079**
Device Description:

Assembly Location: **MMT** Assembly Date Code Year: **2014** Week: **45** Lot Window: **A**
Wafer Lot #: **3305886** Wafer Lot Date Code Year: **2013** Qtr: **4Q** Die Rev: **D** W/F Code: **S**
Wafer #: **8**

Integrated Circuits referenced above have received the following processing per recorded lot history.

SCREEN	METHOD	(MIL-STD-883)		
☑ INTERNAL VISUAL PRECAP	2010	CONDITION A (100X)		
☑ INTERNAL VISUAL PRECAP	2010	CONDITION A (40X)		
☑ INTERNAL VISUAL PRECAP	2010	CONDITION A (L/A)		
Wafer Number(s) used in Production:	8			
☑ TEMPERATURE CYCLING	1010	CONDITION C		
☑ CENTRIFUGE	2001	CONDITION E,Y1 PLANE		
☑ PIND TEST	2020	CONDITION A		
☑ RADIOGRAPHY	2012	☑ MONITOR OR ☐ 100%		
☑ INTERIM ELECTRICAL TEST		25c DC / FUNCTIONAL		
☑ BURN IN	1015	TEMP (°C) 125	TIME (Hrs) 240	
FINAL ELECTRICAL TEST TEMP	☑ 25c ☑ 125c ☑ -55c ☐ N/A		☐ N/A	
TEST PROGRAM #(s)	EF5560R01	EF5560R01	EF5560R01	
☑ HERMETICITY	1014			
FINE LEAK		CONDITION A OR B		
GROSS LEAK		CONDITION C		
☑ EXTERNAL VISUAL	2009	(100%)		
☑ EXTERNAL VISUAL	2009	(L/A)		

QUALITY CONFORMANCE ATTRIBUTE DATA GROUP "A" SUMMARY

SUBGROUP	TEST & TEMP	SAMPLE SIZE
☑ A-1/4/7	DC ELECTRICAL - AMBIENT	116 OR 100%
☑ A-2/5/8	DC ELECTRICAL - MAXIMUM	116 OR 100%
☑ A-3/6/8	DC ELECTRICAL - MINIMUM	116 OR 100%
☑ A-9	AC ELECTRICAL - AMBIENT	116 OR 100%
☑ A-10	AC ELECTRICAL - MAXIMUM	116 OR 100%
☑ A-11	AC ELECTRICAL - MINIMUM	116 OR 100%

Device Lead-Finish complies with MIL-PRF-38535 A.3.5.6.3 Microcircuit finishes: "Finishes of all external leads or terminals and all external package elements shall conform to either A.3.5.6.3.2 or A.3.5.6.3.3 as applicable. The use of pure tin, as an underplate or final finish, is prohibited both internally and externally. The tin content of solder shall not exceed 97 percent. Tin shall be alloyed with a minimum of 3 percent lead by weight.

SOLDER PROCESSING DATE (IF APPLICABLE): **N/A**

NOTE: The following documents MUST be pulled and sent with each lot.
(A copy to be placed in each box)
1) PROCESS CONFORMANCE REPORT
2) GENERIC GROUP B QCI SUMMARY REPORT
3) GENERIC GROUP D QCI SUMMARY REPORT
4) WAFER LOT ACCEPTANCE REPORT FOR THE WAFER LOT USED IN THIS ASSEMBLY LOT.

Product has passed Group E RHA QCI in accordance with MIL-PRF-38535.

Prepared By: Date: **01/19/2015**

QCI Group B - Lot #: **4015101**	Date Code: **1445B**	Pkg Type: **164HFG**	Lead Finish: **A**
QCI Group C - Lot #: **4005420**	Date Code: **1420A**	MCG: **52**	Wafer Lot Date Code: **3D**
QCI Group D - Lot #: **4005420**	Date Code: **1420A**	Pkg Type: **10HKU**	Lead Finish: **NIAU**
QCI Group E - Lot #: **3305886**	Wafer Lot #: **3305886**		
Wafer Lot Accept - Lot #: **4005420**	Wafer Lot #: **3305886**		

Example – QCI Group B Summary Report

Group B Summary Report

Copy | Print | Excel | Share via Email

Lot Number: 4015101 **Device Name:** SMJ320VC33HFGM150

Date Code: 2014-45-B **Assembly Site:** MMT

Test Start: 11/11/2014 **Test Complete:** 11/12/2014 **Lead Finish:** A

Pin: 164 **Package:** HFG **Package Family:** GROUP 8

66666 Sub-Group	Test	Method	Sample Size	Rejects / Data	Notes
B2	RESISTANCE TO SOLVENTS	TM2015	3	0	1
B3	SOLDERABILITY	TM2003	3	0	1
B5	BOND STRENGTH	2011	4	0	1
B5	DIE ATTACH STRENGTH	2019 OR 2027	4	0	

Notes:
1.Resistance to solvents testing required only on devices using inks or paints as a marking medium.
1. 22 leads / 3 packages minimum. Not required for solder columns
1. 15 wires / 4 units mimimum

Comments:

Prepared By: Vut Kangkamanee **Prepared By Email:** x0194988@ti.com **Prepare Date:** 11/11/2014

Example – QCI Group C Summary Report

Group C Summary Report

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Lot Number: 4005420 **Device Name:** 5962R1222403VXC **Assembly Site:** MMT

Lot Date Code: 2014-20-A **Wafer Lot Date Code:** 2013-4Q-D-S **Wafer Lot Number:** 3305886

Parent Die: STLADJC1963DVS **Die Attach:** QMI **Window:** 4Q 2013 to 4Q 2014

Pin: 10 **Package:** HKU **MCG:** 52

Test Start: 07/04/2014 **Test Complete:** 08/20/2014

Sub-Group	Test	Method	Sample Size	Rejects / Data	Notes
C1	Steady-state life test	1005		0	1
C1	Endpoint Electrical Test		45	0	2

Notes:
1. 1,000 hours/125C or equivalent. (If greater than 1,000 hours/125C enter actual conditions into comments below)
2. Endpoint electrical testing in accordance with device test specification.

Comments:

46/0 TESTED

Prepared By: Vut Kangkamanee **Prepared By Email:** x0194988@ti.com **Prepare Date:** 08/22/2014

Example – QCI Group D Summary Report

Group D Summary Report

Copy Print Excel Share via Email

Lot Number: 4005420 **Device Name:** 5962R1222403VXC

Date Code: 2014-20-A **Assembly Site:** MMT

Test Start: 06/26/2014 **Test Complete:** 07/10/2014 **Lead Finish:** NIAU

Pin: 10 **Package:** HKU **Package Family:** GROUP 8

Window: 20 2014 to 04 2015

66666 Sub-Group	Test	Method	Sample Size	Rejects / Data	Notes
D1	Physical Dimensions	2016	15	0	
D2	Lead Integrity	2004 and 2028	45	0	1
D2	Seal (Fine and Gross)	1014		0	
D3	Thermal Shock	1011	15	0	2
D3	Temperature Cycle	1010		0	3
D3	Moisture Resistance	1004		0	
D3	Visual Examination	1004 and 1010		0	
D3	Seal (Fine and Gross)	1014		0	
D3	End-point electrical test			0	4
D4	Mechanical Shock	2002	15	0	5
D4	Vibration, Variable Freq	2007		0	6
D4	Constant acceleration	2001		0	7
D4	Seal (Fine and Gross)	1014		0	
D4	Visual Examination	1010 and 1011		0	
D4	End-point electrical test			0	4
D5	Salt Atmosphere	1009	15	0	10
D5	Visual Inspection	1009		0	
D5	Seal (Fine and Gross)	1014		0	
D6	Internal water vapor	1018	3 (5)	0 (1)	8
D7	Adhesion of lead finish	2025	15	0	9
D8	Lid Torque	2024	5	0	11

Notes:
1. Condition B2, 3 devices, 45 leads total. For PGA and rigid leads use Condition B1 or Method 2028. For LCCC packages only, use condition D and SS of 15 based on the number of pads tested from 3 devices minimum.
2. Condition B, 15 cycles.
3. Condition C, 100 cycles.
4. Endpoint electrical testing in accordance with device test specification.
5. Condition B.
6. Condition A.
7. Condition E (20KG) Y1 axis only.
4. Endpoint electrical testing in accordance with device test specification.
10. Condition A.
8. 5000 PPM and 100C. Sample size is 3/0 or 5/1.
9. 15 leads, not performed for LCCC. Any deviations to test methods or conditions, such as centrifuge, will be specificed in the device travler.
11. Glass Frit Seal Only - N/A for MMT Assembly.

Comments:

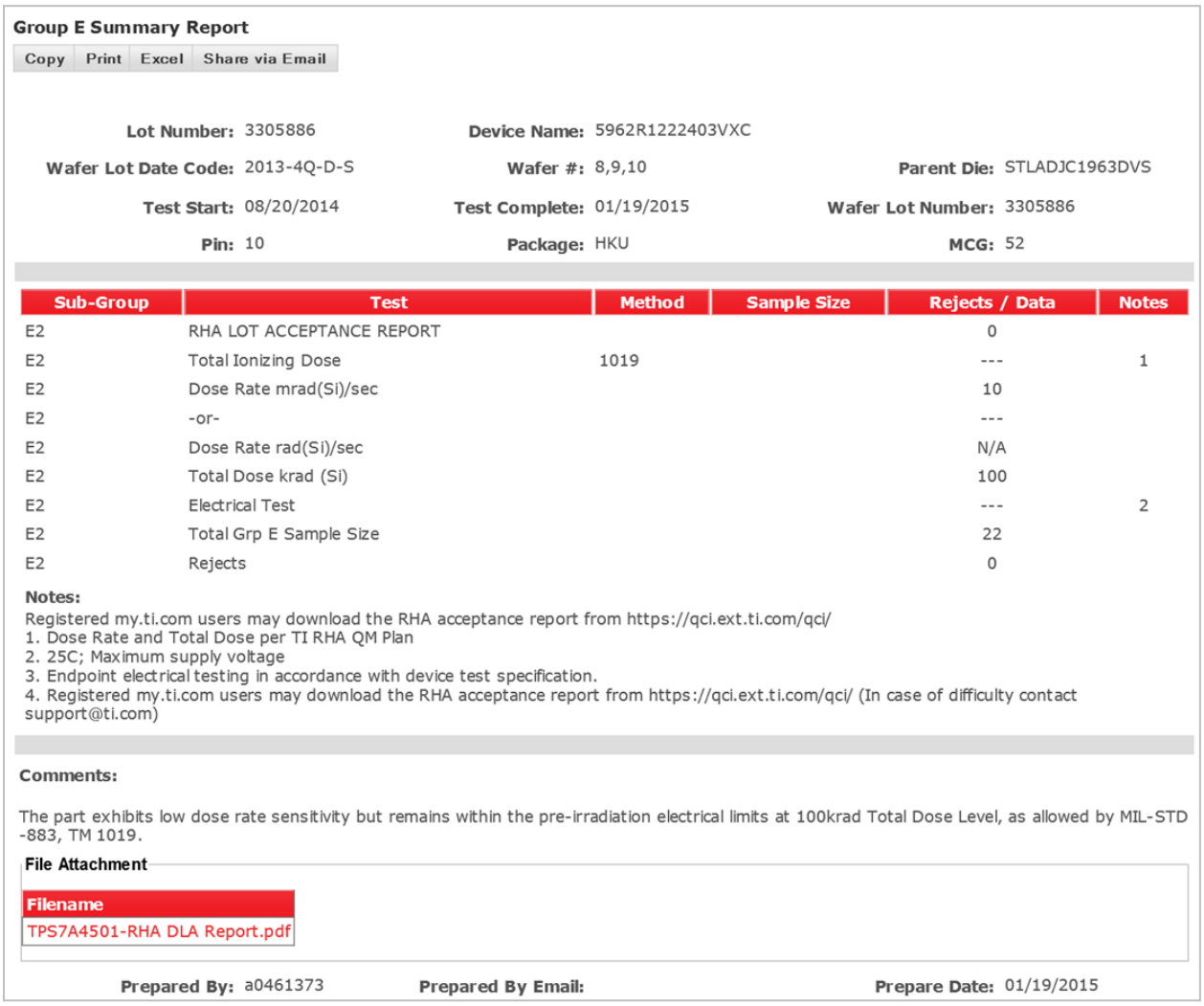
Performed D3 and D4

File Attachment

Filename
No Files Uploaded

Prepared By: Vut Kangkamanee **Prepared By Email:** x0194988@ti.com **Prepare Date:** 07/17/2014

Example – QCI Group E Summary Report



Group E Summary Report

Copy | Print | Excel | Share via Email

Lot Number: 3305886 **Device Name:** 5962R1222403VXC

Wafer Lot Date Code: 2013-4Q-D-S **Wafer #:** 8,9,10 **Parent Die:** STLADJC1963DVS

Test Start: 08/20/2014 **Test Complete:** 01/19/2015 **Wafer Lot Number:** 3305886

Pin: 10 **Package:** HKU **MCG:** 52

Sub-Group	Test	Method	Sample Size	Rejects / Data	Notes
E2	RHA LOT ACCEPTANCE REPORT			0	
E2	Total Ionizing Dose	1019		---	1
E2	Dose Rate mrad(Si)/sec			10	
E2	-or-			---	
E2	Dose Rate rad(Si)/sec			N/A	
E2	Total Dose krad (Si)			100	
E2	Electrical Test			---	2
E2	Total Grp E Sample Size			22	
E2	Rejects			0	

Notes:

Registered my.ti.com users may download the RHA acceptance report from https://qci.ext.ti.com/qci/
1. Dose Rate and Total Dose per TI RHA QM Plan
2. 25C; Maximum supply voltage
3. Endpoint electrical testing in accordance with device test specification.
4. Registered my.ti.com users may download the RHA acceptance report from https://qci.ext.ti.com/qci/ (In case of difficulty contact support@ti.com)

Comments:

The part exhibits low dose rate sensitivity but remains within the pre-irradiation electrical limits at 100krad Total Dose Level, as allowed by MIL-STD -883, TM 1019.

File Attachment

Filename
TPS7A4501-RHA DLA Report.pdf

Prepared By: a0461373 **Prepared By Email:** **Prepare Date:** 01/19/2015

To download the full RHA DLA report, click the link under ‘Filename.’

Example – QCI Wafer Lot Acceptance Summary Report

WLA Summary Report

Copy | Print | Excel | Share via Email

Lot Number: 4005420 **Device Name:** 5962R1222403VXC

Wafer Lot Date Code: 2013-4Q-D-S **Wafer Lot Number:** 3305886

Parent Die: STLADJC1963DVS **Lead Finish:** NIAU **MCG:** 52

Test Start: 08/28/2014 **Test Complete:** 08/28/2014

Sub-Group	Test	Method	Sample Size	Rejects / Data	Notes
WLA-1	Wafer Thickness	5007	2 wafers/lot	0	1
WLA-2	Metallization Thickness	5007	1 wafer/lot	0	2
WLA-3	Thermal Stablility	5007	1 wafer/lot	0	2,3
WLA-4	SEM Inspection Lot Acceptance	2018	2 wafers/lot	0	2
WLA-4	Lab Performing Analysis:			TI	
WLA-5	Glassivation Thickness	5007	1 wafer/lot	0	2
WLA-6	Gold Backing Thickness	5007	1 wafer/lot	0	2,4
WLA-7	Steady-state life test	1005		0	5
WLA-7	Endpoint Electrical Test	1005	45	0	6

Notes:
1. This test is not required when the finished wafer design thickness is greater than 10 mils before backgrind.
2. In-line monitor data for this wafer lot may be used.
3. Applicable to all linear, all MOS, all bipolar digital operating at 10V or more. (VFB/VT/C-V)
4. Gold backed wafers only.
5. 1,000 hours/125C or equivalent
6. Endpoint electrical testing in accordance with device test specification

Comments:

Prepared By: Vut Kangkamanee **Prepared By Email:** x0194988@ti.com **Prepare Date:** 08/27/2014

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