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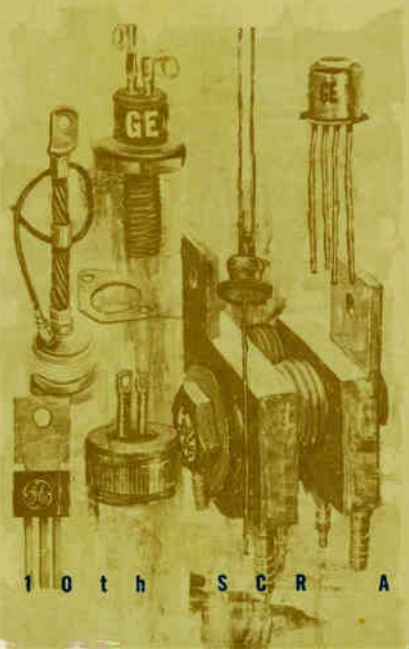
SILICON CONTROLLED RECTIFIER MANUAL,
INCLUDING THE TRIAC AND THE
INDUSTRY'S BROADEST LINE OF
THYRISTOR AND RECTIFIER COMPONENTS

SCR Manual

4th Edition



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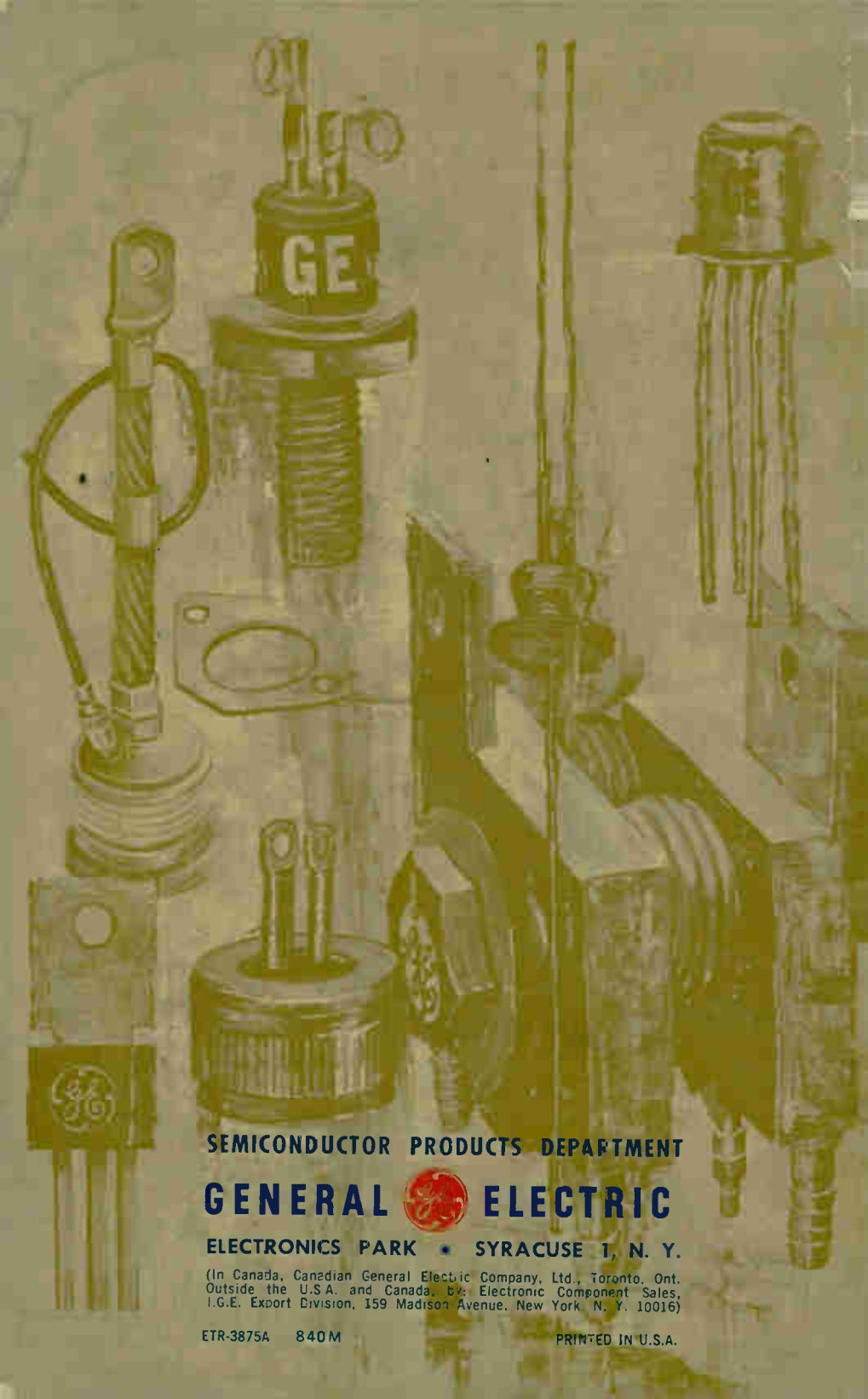

SEMICONDUCTOR PRODUCTS DEPARTMENT

GENERAL ELECTRIC

ELECTRONICS PARK • SYRACUSE 1, N. Y.

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FOREWORD

TO THE TENTH ANNIVERSARY EDITION OF THE G-E SCR MANUAL

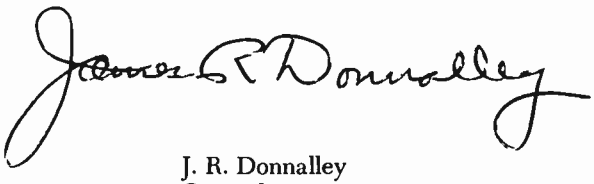
Publication of this 4th Edition marks ten years since General Electric introduced the first commercial SCR. In this short decade, the SCR has grown rapidly from a high-priced curiosity to a basic and economical design element in every field of electrical power control and conversion.

The fast-growing success story of the SCR is paralleled by the growth of the General Electric SCR Manual. First published as an application note in 1958, the General Electric SCR Manual has grown about thirty times to the present 513 pages. During this interval the Manual has kept the basic theme of a practical rather than theoretical circuit and application guide for design engineers, students, teachers, and experimenters. It is written by a group of engineers that includes those who were instrumental in helping General Electric introduce the first SCR in 1957. These authors have gained their insight and experience by contributing to literally thousands of successful thyristor design projects that are noteworthy both for their diversity as well as the ingenuity and pioneering spirit displayed in their implementation.

Since the last edition, G-E's introduction of the triac has greatly influenced AC control circuits. This is reflected in both a new chapter on the triac and many new circuits throughout the Manual. The fourth edition also contains much other original and updated material. For instance, new chapters have been written on regulating circuits and motor controls. Additional new material on triggering has been introduced, and specs on hundreds of new higher-performance thyristors have been added.

Considerable effort has been spent in keeping the SCR Manual concise and general in nature. For those desiring in-depth treatment of highly specialized subjects, we refer them to the comprehensive application notes listed on page 497.

I sincerely hope that you will find this new Manual useful and informative.



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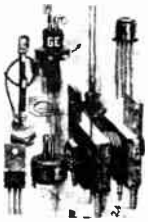

INTRODUCTION

HOW TO LEARN ABOUT THE SCR

If you, the reader, are already familiar with the SCR and wish guidance in the design of practical applications, this Manual is ideal for your needs. If you wish more detailed information on a specialized subject, consider the references listed at the end of each chapter, as well as the comprehensive list of General Electric application notes (p.497) which are available on request.

If you wish to explore thyristors in a more analytical sense, either as a semiconductor or as a circuit element, we refer you to "Semiconductor Controlled Rectifiers . . . Principles and Applications of p-n-p-n Devices," a book published by Prentice-Hall, Englewood Cliffs, New Jersey. It shares several authors with this Manual.

If you have heard of the SCR but would like to start from scratch in learning how it can help you, as indeed all of us were doing just a short time ago, we suggest that you obtain a copy of the General Electric "Electronic Components Hobby Manual." The term "Hobby Manual" is somewhat of a misnomer. It is a serious engineering effort with some 40 ingenious circuits and projects useful in teaching the fundamentals of electronics while constructing projects having lasting value in the automobile, home, workshop and campsite. This book was written by our application engineers on the assumption that the reader, although learned in his own field of competence, is new to the SCR and other semiconductors as well.

If you are really impatient to see how a basic thyristor circuit can work with your equipment load, or if you have no facilities to assemble your own circuit from electronic components, you may wish to experiment with one of several standard assemblies available from your G-E distributor. A typical standard triac variable voltage control is shown above. They are described further in Chapter 21.

A BRIEF DESCRIPTION OF THE SCR

The SCR is senior and most influential member of the thyristor family of semiconductor components. Younger members of the thyristor family share the latching (regenerative) characteristics of the SCR. They include the triac, bidirectional diode switch, the silicon controlled switch (SCS), the silicon unilateral and bilateral switches (SUS, SBS), and light activated devices like the LASCR and LASCS.

Let's go back to the head of the family after whom this Manual was named. The SCR is a semiconductor . . . a rectifier . . . a static latching switch . . . capable of operating in microseconds . . . and a sensitive amplifier. It *isn't* an overgrown transistor, since it has far greater power capabilities, both voltage and current, under both continuous and surge conditions, and can control far more watts per dollar.

As a *silicon semiconductor*—the SCR is compact, static, capable of being hermetically sealed, silent in operation and free from the effects of vibration and shock. A properly designed and fabricated SCR has no inherent failure mechanism. When properly chosen and protected, it should have virtually limitless operating life even in harsh atmospheres. Thus countless billions of operations can be expected, even in explosive and corrosive environments.

As a *rectifier*—the SCR will conduct current in only one direction. But this serves as an advantage when the load requires DC, for here the SCR serves both to control *and* rectify—as in a regulated battery charger.

As a *latching switch*—the SCR is an ON-OFF switch, unlike the vacuum tube and transistor which are basically variable resistances (even though they too can be used as on-off switches). The SCR can be turned on by a momentary application of control current to the gate (a pulse as short as a fraction of a microsecond will do), while tubes or transistors (and the basic relay) require a continuous ON signal. In short the SCR *latches* into conduction, providing an inherent memory useful for many functions. The SCR can be turned ON in about one microsecond, and OFF in 10 to 20 microseconds; further improvements in switching speed are being made all along.

Just as a switch or relay contact is commonly rated in terms of the current it can safely carry and interrupt, as well as the voltage at which it is capable of operating, the SCR is rated in terms of peak voltage and forward current. General Electric offers a complete family of SCR's with current carrying capacities from ½ amp to 850 amps RMS, and up to 1800 volts at this writing. (See Frontispiece.) Higher voltage and current loads are readily handled by series and parallel connection of SCR's.

As an *amplifier*—the smallest General Electric SCR's can be latched into conduction with control signals of only a few microwatts and a few microseconds duration. These SCR's are capable of switching up to 200 watts. The resulting control power gain of over 10 million makes the small SCR one of the most sensitive control devices available. With a low cost unijunction transistor firing circuit driving the larger SCR's, stable turn-on control power gains of many billions are completely practical. This extraordinary control gain makes possible inexpensive control circuits using very low level signals, such as produced by thermistors, cadmium sulfide light sensitive resistors, and other transducers.

Most of the foregoing list of assets of the SCR apply equally well to the other members of the thyristor family as you will see in this Manual. Meanwhile the shortcomings and limitations of thyristors become less significant as the years pass. Newly introduced high voltage and bidirectional types lift the transient and operating voltage barriers. High speed thyristors allow operation at ultrasonic frequencies and under severe dynamic conditions, and lower semiconductor costs permit use of higher current rated thyristors instead of critically designed and expensive overcurrent protection systems.

Best of all, SCR's and thyristors for every type of application . . . industrial, military, aerospace, commercial, consumer . . . are *more economical than ever.* Best indication of this is the rapidly increasing tempo of applications of the triac and new plastic-encapsulated SCR's in high volume small appliance applications where every penny is critical.

Here are just some of the conventional types of controls and elements that thyristors are busy replacing and improving upon:

Thyratrons
Relays
Magnetic Amplifiers
Ignitrons
M-G Sets
Rheostats
Power Transistors
Motor Starters
Transformers
Limit Switches
Constant Voltage Transformers
Saturable Reactors
Contactors
Variable Autotransformers
Fuses
Timers
Vacuum Tubes
Thermostats
Mechanical Speed Changers
Centrifugal Switches
Ignition Points

Welcome to the exciting world of the thyristor family, its circuits and applications. Please bear in mind that the material in this Manual is intended only as a general guide to circuit approaches. It is not all-encompassing. However, our years of experience in offering application help have shown that, given some basic starting points like those in this Manual, you the circuit designer inevitably come up with the best, and often unique, approach for your particular problems.

You will find the "Application Index" on pages 506-507 a useful roadmap in starting the search for the ideal circuit for your application. The list of Application Notes starting on page 497 will also provide specialized help beyond the detail of this Manual.

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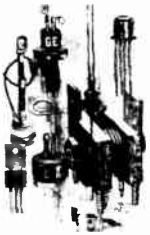
SILICON CONTROLLED RECTIFIER MANUAL, INCLUDING THE TRIAC AND THE INDUSTRY'S BROADEST LINE OF **THYRISTOR** AND RECTIFIER COMPONENTS

1 CONSTRUCTION AND BASIC THEORY OF OPERATION



1.1 WHAT IS A THYRISTOR?

The name thyristor[1] defines any semiconductor switch whose bistable action depends on p-n-p-n regenerative feedback. Thyristors can be two, three, or four terminal devices, and both unidirectional and bi-directional devices are available.

1.2 CLASSIFICATIONS OF THYRISTORS

The silicon controlled rectifier (SCR) is by far the best known of all thyristor devices. Because it is a unidirectional device (current flows from anode to cathode only) and has three terminals (anode, cathode and control gate) the SCR is classified as a *reverse blocking triode thyristor*. Other members of the reverse blocking triode thyristor family include the silicon unilateral switch (SUS), the light activated silicon controlled rectifier (LASCR), and the gate turn-off switch. The silicon controlled switch (SCS) is a reverse blocking *tetrode* thyristor (it has two control gates), while the Shockley diode is a reverse blocking diode thyristor. Bidirectional thyristors are classified as p-n-p-n devices that can conduct current in either direction; commercially available bidirectional triode thyristors include the triac (for *tri*ode *AC* switch), and the silicon bilateral switch (SBS).

1.3 THYRISTOR CONSTRUCTION

The successful and reliable operation of a thyristor is predicated on its proper design and construction. The fabrication methods chosen for a particular thyristor type depend a great deal therefore on the service expected from that type. A seventy ampere SCR destined for use in a harsh military environment may differ radically in design from a six ampere triac intended for the light industrial or consumer markets.

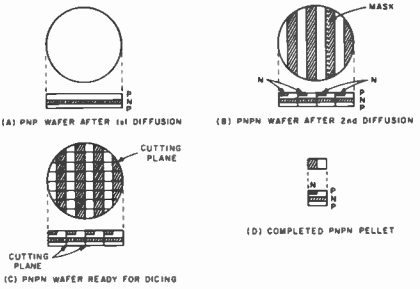


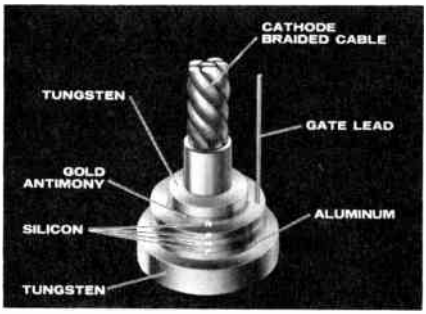
FIGURE 1.1 ALL-DIFFUSED PELLET FORMATION

1.3.1 Pellet Fabrication

The heart of a p-n-p-n device is its multi-layered "pellet" of alternate p and n type semiconductor material. This semiconductor is almost always silicon, although germanium has been used. Pellets may be fabricated by any one of several methods, depending on the desired characteristics, complexity, and size of the finished device. The most popular pellet fabrication methods are:

Alloy diffused
Diffused
Planar-diffused

The manufacture of both alloy-diffused and all-diffused p-n-p-n pellets starts with the preparation of large area *p-n-p wafers*. These are formed by gaseously diffusing p-type impurities simultaneously into both faces of a thin wafer of n-type silicon. Where specific device characteristics require it, a second diffusion step is used to complete the final p-n-p-n structure. To do this, each p-n-p wafer is selectively masked (on one side only), and subsequently diffused with n-type impurities through the windows in the mask. The finished p-n-p-n wafers are then diced into individual pellets. Triacs and other more complex structures are fabricated using similar techniques. In the manufacture of some higher current SCR's, where only a limited number of pellets (sometimes only one) can be obtained from each wafer, it is often more convenient to pelletize the original p-n-p wafers *before* adding the final n-region. Where this is the case, precision alloying techniques are used after pelletizing to fuse a gold-antimony preform into each p-n-p pellet, thus forming the required p-n-p-n structures. Figure 1.1 shows the cross section of a typical all-diffused SCR structure, while Figure 1.2 is a pictorial of an alloy-diffused type.



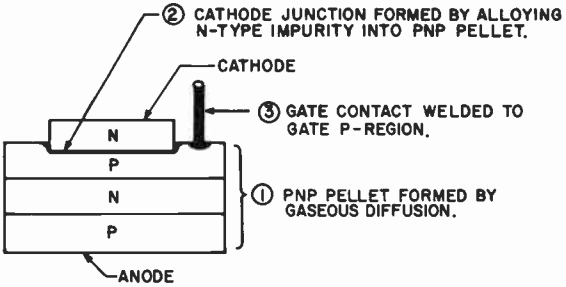


FIGURE 1.2 ALLOY-DIFFUSED PELLET FORMATION

A *planar* structure describes a type of pellet where all the p-n junctions come out to a single surface on the silicon pellet. The principal advantage of planar construction is that junction formation always takes place (see Figure 1.3) underneath a thin layer of moisture and contaminant resistant silicon dioxide grown over the silicon wafer before diffusion commences. As a result planar pellets are to a large degree protected from the outside environment—hence the term "planar-passivated." Disadvantages of planar construction are that more silicon is required per ampere of current carrying capability, and that more wafer processing steps are needed. Planar structures are best suited therefore to low current devices where many pellets can be obtained from a single wafer.

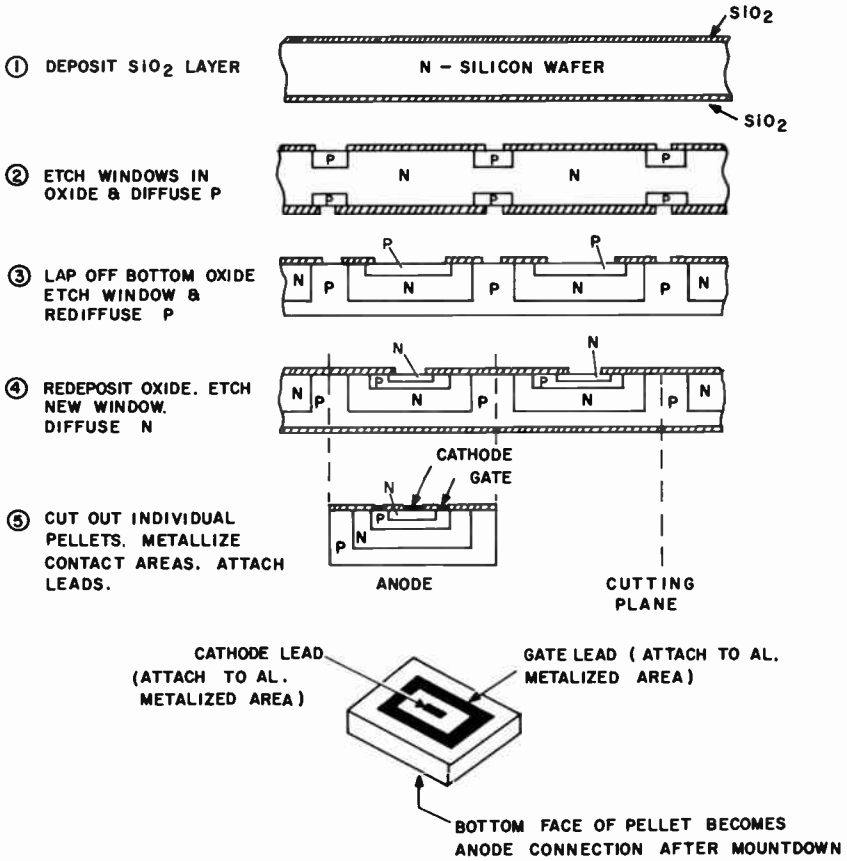


FIGURE 1.3 TYPICAL PLANAR PNPN PELLET FABRICATION
(Geometry exaggerated for clarity.)

1.3.2 Pellet Encapsulation

Pellet encapsulation methods vary widely, depending on the in-service environment expected of the finished device and on the type of pellet being encapsulated. Where a device must operate over a very wide temperature range, or where severe thermal cycling is expected, pellets generally are hard soldered between a pair of thermally matched back-up plates, one of which is then hard soldered to a copper stud. The copper stud serves as one terminal, the base for the device housing, and the thermal path for conducting heat losses to the ambient. For this latter reason the stud is usually threaded or bolted to a heatsink. Use of hard solder with this type of construction minimizes the possibility of thermal fatigue destroying the joint between copper and back-up plate when the thyristor is subjected to the temperature induced stresses of wide and frequent thermal cycling. Hard solder is used for the joint between cathode-plate and cathode terminal for the same reason. Figure 1.4 shows a section through a typical thermal-fatigue-resistant high current SCR.

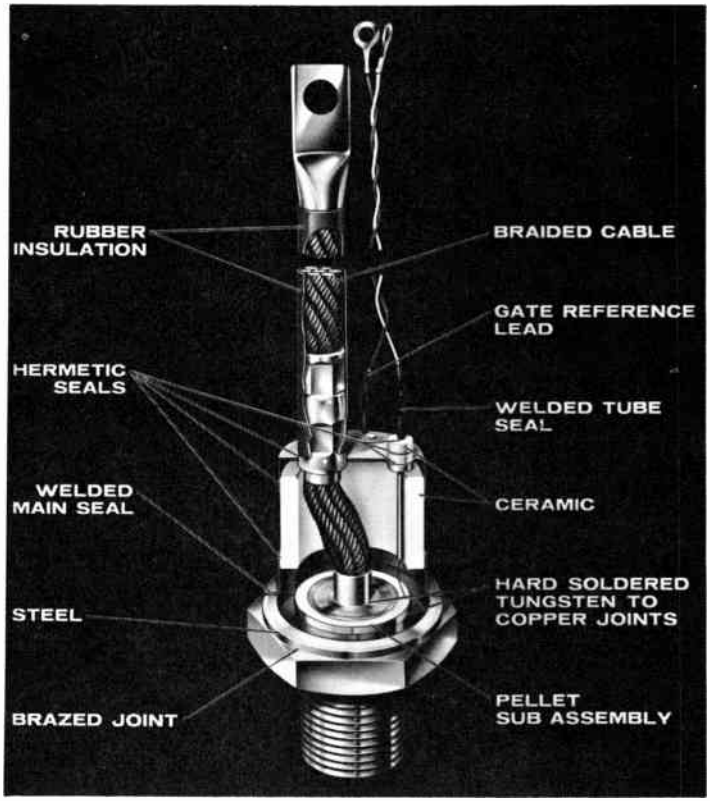


FIGURE 1.4 THERMAL FATIGUE RESISTANT SCR CONSTRUCTION

Another method of encapsulation involves replacement by pressure contacts[2] of the top and bottom solder joints between the copper and the tungsten (or molybdenum) back-up plates of the semiconductor pellet assembly in Figure 1.4. The force required to develop the necessary pressure to ensure adequate electrical and thermal contacts at the joints may be either retained internally to the encapsulating housing or retained external to the encapsulation. A particular advantage to retaining the force externally is that this method allows cooling the semiconductor pellet assembly from both sides for improved heat transfer.

Figure 1.5 shows such a PRESS PAK encapsulation for a semiconductor pellet assembly suitable for double-sided air or water cooling.

FIGURE 1.5 PRESS PAK ENCAPSULATION FOR A 230 AMPERE SEMICONDUCTOR PELLET ASSEMBLY.

Figure 1.6 shows a typical double-sided cooling arrangement for a forced-air-cooled application.

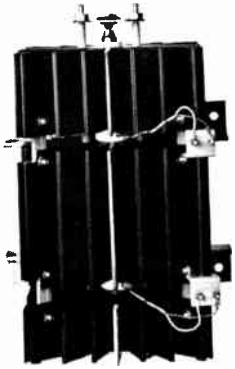


FIGURE 1.6 TYPICAL APPLICATION OF PRESS PAK ENCAPSULATION IN A DOUBLE-SIDED COOLING ARRANGEMENT.

When a thyristor is designed specifically for use in the light industrial and consumer markets, environments usually characterized by limited temperature excursions and an absence of wide range cyclical loading, the premium-type structure described above is not required. Here, the silicon pellet is mounted *directly* onto the copper stud, or case, with a special tin-lead solder alloy. The solder joint then absorbs the stresses set up by differential expansion between silicon and copper. *Providing these stresses are not too great*, this "soft solder" construction is satisfactorily thermal fatigue free. In addition to making possible a lower-cost device, the method allows better heat transfer from silicon to copper, which reduces cell heatsinking requirements.

The entire thyristor assembly is fabricated in a super-clean environment to assure long term stability of the SCR's electrical characteristics. To maintain the stability of these characteristics throughout the long life of the thyristor, the finished assembly is sealed off from the outside atmosphere by welded hermetic seals. Electrical connections are also made by welding. Extensive electrical and mechanical tests at room temperature and both extremes of the operating temperature range assure that the individual thyristors meet their specification sheet ratings and characteristics. Cycled life tests on significant samples continuously monitor and control the long-term reliability of all devices coming off the production line.

Because planar type pellet fabrication inherently gives a large degree of environmental protection to the pellet electrical characteristics, hermetic glass-metal packaging is often not required for planar type devices. Planar pellets generally are encapsulated in an injection-moulded plastic package, which provides good mechanical integrity to the finished device. Figure 1.7 is a cutaway view of a two ampere planar SCR.

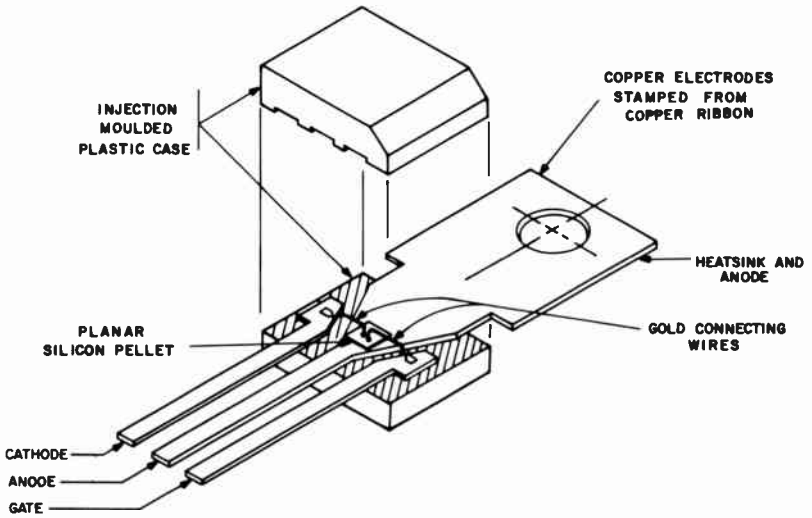


FIGURE 1.7 C106 PLANAR SCR

1.4 TWO TRANSISTOR ANALOGY OF p-n-p-n OPERATION[3]

A simple p-n-p-n structure like the conventional SCR is best visualized as consisting of two transistors, a p-n-p and an n-p-n interconnected to form a regenerative feedback pair as shown in Figure 1.8. Current gain around the internal feedback loop $G = h_{FE1} \times h_{FE2}$, where h_{FE1} and h_{FE2} are the common emitter current gains of the individual transistor sections. If I_{CO1} is the collector to base leakage current of the n-p-n, and I_{CO2} is the leakage of the p-n-p, then

For the p-n-p section: $I_{C1} = h_{FE1}(I_{C2} + I_{CO1}) + I_{CO1}$

For the n-p-n section: $I_{C2} = h_{FE2}(I_{C1} + I_{CO2}) + I_{CO2}$ and total anode-to-cathode current $I_A = (I_{C1} + I_{C2})$.

Solving these three equations for I_A gives

$$I_A = \frac{(1 + h_{FE1})(1 + h_{FE2})(I_{CO1} + I_{CO2})}{1 - h_{FE1} \cdot h_{FE2}} \qquad 1.1$$

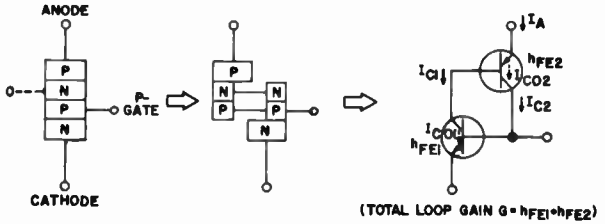


FIGURE 1.8 TWO TRANSISTOR ANALOGUE OF SCR

With proper bias applied (*positive* anode to cathode voltage), h_{FE1} and h_{FE2} are both low, and G is much less than unity. The denominator of Equation 1.1 approaches one, and I_A is little higher than the sum of the individual transistor leakage currents. Under these conditions the p-n-p-n structure is said to be in its *forward blocking* or high impedance "off" state. The switch to the low impedance "on" state is initiated simply by raising the loop gain G to unity. Inspection of Equation 1.1 shows that as $h_{FE1} \cdot h_{FE2} \rightarrow 1$, $I_A \rightarrow \infty$. Physically, as the loop gain approaches unity and the circuit starts to regenerate, each transistor drives its mate into saturation. Once in saturation, all junctions assume a forward bias, and total potential drop across the device approximates that of a single p-n junction. Anode current is limited only by the external circuit.

The p-n-p-n structure may also be analysed in terms of its component transistor "alphas." The p-n-p section has an α_1 which defines the fraction of hole current injected at its emitter that reaches its collector (Figure 1.9).

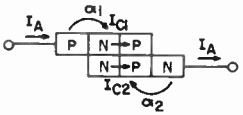


FIGURE 1.9 "ALPHA" ANALYSIS OF SCR OPERATION

$$I_{C1} = \alpha_1 I_A$$

The n-p-n section similarly has an α_2 which defines the fraction of electron current injected at its emitter that reaches its collector.

$$I_{C2} = \alpha_2 I_A$$

Total anode current must equal the sum of these two components *plus* a leakage term:

$$I_A = \alpha_1 I_A + \alpha_2 I_A + I_{CX}$$

where I_{CX} is the leakage current of the center junction. Rearranging and solving for I_A gives

$$I_A = \frac{I_{CX}}{1 - (\alpha_1 + \alpha_2)} \qquad 1.2$$

Equation 1:2 is the "alpha" equivalent of Equation 1:1 when $(\alpha_1 + \alpha_2) << 1$ $I_A \rightarrow I_{CX}$ and this corresponds to the p-n-p-n forward blocking state. When $(\alpha_1 + \alpha_2) \rightarrow 1$, $I_A \rightarrow \infty$, and this corresponds to the p-n-p-n forward conduction state.

There are several mechanisms available for increasing h_{FE} in a transistor, so that in the p-n-p-n structure $h_{FE1} \cdot h_{FE2} \rightarrow 1$, and the device may be switched on. All make use of the emitter-current dependence of h_{FE}. In most silicon transistors, h_{FE} is quite low at low emitter currents, but increases fairly rapidly as emitter current is increased. This effect (Figure 1.10) is due to the presence in the silicon of special impurity centers. Any mechanism which causes a temporary increase in transistor emitter current is therefore potentially capable of turning on a p-n-p-n device. The most important of these mechanisms are:

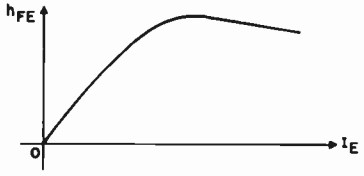


FIGURE 1.10 EMITTER-CURRENT DEPENDENCE OF h_{fe} IN A SILICON TRANSISTOR

1. Voltage. As the collector-to-emitter voltage of a transistor is increased, eventually a point is reached where the energy of the (leakage) current carriers arriving at the collector junction is sufficient to dislodge additional carriers. These carriers in turn dislodge more carriers, and the whole junction goes into a form of avalanche breakdown characterized by a sharp increase in collector current. In a p-n-p-n device, when the avalanche current makes $G \rightarrow 1$, switching takes place. This is the turn-on mechanism normally employed to switch four layer diodes into conduction.

2. Rate of change of voltage. Any p-n junction has capacitance—the larger the junction area, the larger the capacitance. If a step function of voltage is impressed suddenly across the anode-to-cathode terminals of a p-n-p-n

device, a charging current i will flow from anode to cathode to charge the device capacitance:

$$i = C\, dv/dt$$

When i equals the value necessary for G → 1, the device will switch on. This phenomenon is known as the "dv/dt effect."

3. Temperature. At high temperatures, leakage current in a reverse biased silicon p-n junction doubles approximately with every 8°C increase in junction temperature. When the temperature generated leakage current in a p-n-p-n structure has risen sufficiently for G → 1, switching occurs.

4. Transistor Action. Collector current is increased in conventional transistor manner by temporarily injecting additional ("gate") current carriers into a transistor base region. This is the mechanism normally employed to turn-on SCR's and other p-n-p-n devices which have an external connection ("gate" lead) to one or more of the transistor bases.

By convention, SCR's that are turned on by injecting current into the lower p-base (via an external connection to this base) are called "conventional" SCR's, while those that utilize the upper n-base are called "complementary" SCR's. The four-terminal silicon controlled switch (SCS) has connections made to *both* bases and either or both bases may be used to initiate switching. It should be noted that because the upper n-base is a region of high resistivity (the upper p-n junction supports the major part of any applied reverse voltage) more external gate current is required to trigger an SCR via the n-gate than with the p-gate.

5. Radiant energy ("light"). Incident radiant energy within the spectral bandwidth of silicon (Figure 11.2) impinging on and penetrating into the silicon lattice releases considerable numbers of hole-electron pairs. When the resultant device leakage current climbs above the critical level for G → 1, triggering will ensue. This triggering mechanism makes possible the light activated SCR. In these devices a translucent "window" is provided in the device encapsulation in order that "light" may reach the silicon pellet. The LASCR, because it is provided with a gate lead, may be triggered either by light or by electrical gate current.

1.5 SIMPLIFIED TRIAC THEORY

Four basic thyristor concepts provide a foundation for the theory of bidirectional thyristor operation. These concepts are:

a) The basic reverse blocking triode thyristor (or SCR)

See Section 1.4.

b) The shorted emitter thyristor

Figure 1.11 shows a "shorted emitter" thyristor structure. Externally applied gate current I_G flows from gate to cathode *laterally* through the gate p-region. The voltage drop developed across the lateral base resistance of p forward biases the right hand edge of the cathode junction. If gate current is sufficiently large, electrons are injected from this point, and the device turns on in normal p-n-p-n fashion when regeneration begins.

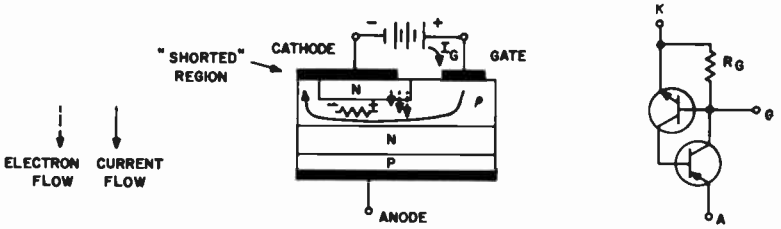


FIGURE 1.11 SHORTED EMITTER STRUCTURE

Shorted emitter structures are often used in thyristor designs. The effect of the partial gate to cathode short is the same as placing a resistor in parallel with the gate cathode junction of a conventional nonshorted emitter device.[3] This resistor (R_{GK} in Figure 1.11) diverts some of the thyristor's thermally generated leakage current and/or dv/dt induced capacitive charging current around the gate-cathode junction, by providing an alternative lower impedance path to the cathode. Regeneration is reduced and a shorted emitter thyristor has, as a result, superior high temperature characteristics and dv/dt capability.

c) Junction gate thyristor

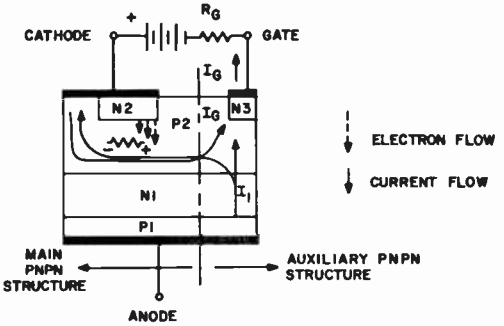


FIGURE 1.12 JUNCTION GATE THYRISTOR

Figure 1.12 shows a typical junction gate thyristor structure. Initially, gate current I_G forward biases the gate junction p_2-n_3 of the auxiliary p_1-n_1-p_2-n_3 structure, and this structure turns on in conventional p-n-p-n fashion. As p_1-n_1-p_2-n_3 turns on, the voltage drop across it falls, and the *right hand section* of region p_2 moves towards anode potential. Since the *left hand section* of p_2 is clamped to cathode potential, a transverse voltage gradient now exists across p_2, and current flows laterally through p_2. As the right hand edge of p_2-n_2 becomes forward biased, electrons are injected at this point and the main structure turns on (compare this action to that of the shorted emitter structure).

d) Remote gate thyristor

A remote gate thyristor is one that can be triggered without an ohmic contact to either of its internal base regions. Figure 1.13 depicts a typical remote base structure.

The external gate current I_G causes p_1-n_3 to become forward biased, and inject electrons as shown. These electrons diffuse through region p_1 and are collected by junction p_1-n_1. Note that junction p_1-n_1 can still act as a collector even though it is forward biased,[4] since the

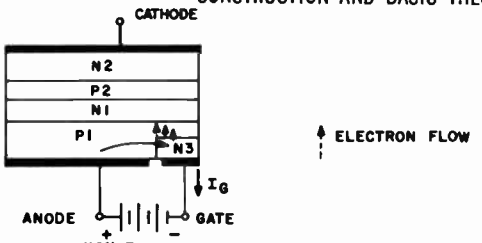


FIGURE 1.13 REMOTE GATE THYRISTOR

electric field associated with it is in the same direction as it would be if p_1-n_1 were reverse biased, as a "collector" normally is. The electrons from n_3 collected by p_1-n_1 cause an increase of current across p_1-n_1, regeneration starts, and the structure turns on.

The salient features of the four devices just described can be combined into a single device—the "triac"—which can block voltage in either direction, conduct current in either direction, and be triggered on in either direction by positive or negative gate signals. Figure 1.14 is a pictorial view of a typical device. Operation is as follows:

a) Terminal #2 positive, positive gate current

In this mode the triac behaves strictly like a conventional thyristor. Active parts are p_1-n_1-p_2-n_2.

b) Terminal #2 positive, negative gate current

Operation is analogous to the junction gate thyristor. p_1-n_1-p_2-n_2 is the main structure, with n_3 acting as the junction gate region.

c) Terminal #2 negative, negative gate current

Remote gate mode. p_2-n_1-p_1-n_4 is the main structure, with junction p_2-n_3 injecting electrons which are collected by p_2-n_1.

d) Terminal #2 negative, positive gate current

p_2-n_2 is forward biased and injects electrons which are collected by p_2-n_1. p_2-n_1 becomes more forward biased. Current through the p_2-n_1-p_1-n_4 portion increases and this section switches on. This mode, too, is analogous to remote gate operation.

Reference 5 gives a more detailed description of triac behaviour.

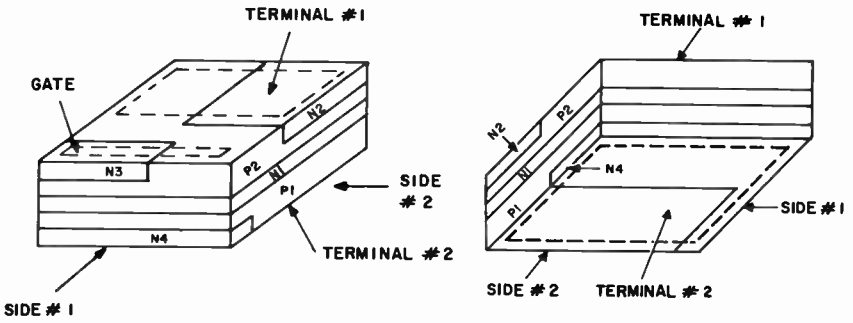


FIGURE 1.14 TYPICAL TRIAC STRUCTURE

1.6 V-I CHARACTERISTICS OF p-n-p-n DEVICES

1.6.1 V-I Characteristics of Reverse Blocking Triode or Tetrode Thyristors

Figure 1.15 illustrates the V-I characteristics of a typical gate-controlled reverse blocking thyristor. In the forward blocking region, increasing the forward voltage does not tend to increase leakage current until the point is reached where avalanche multiplication begins to take place. Past this point, the leakage current increases quite rapidly until the total current through the device is sufficient to raise the internal loop gain ≥ 1. At this point the device will go into the high conduction region, provided that anode current remains in excess of a minimum value called the *holding current*. When anode current drops below the holding current, the p-n-p-n device reverts to its forward blocking state. In the reverse direction the p-n-p-n structure looks like two reverse-biased p-n junctions in series, so that it exhibits characteristics very similar to an ordinary back-biased silicon rectifier. For most commercially available devices (SCR, SCS, LASCR, four layer diode), the peak *reverse* voltage capability is designed to be at least equal in magnitude to the minimum forward breakover voltage.

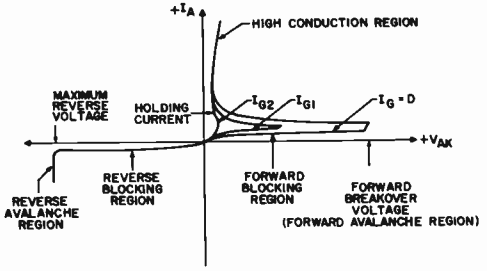


FIGURE 1.15 V-I CHARACTERISTICS OF A REVERSE BLOCKING THYRISTOR

For increasing magnitudes of gate current, the region of characteristics between breakover current and holding current (Figure 1.15) is narrowed and the forward breakover voltage is reduced. For sufficiently high gate currents, the entire forward blocking region is removed, and the V-I characteristics are essentially identical to those of a p-n rectifier.

In typical operation the reverse blocking thyristor is biased well below its minimum forward breakover voltage, and triggering is accomplished by injecting current into the gate lead. ("Light" is of course used in place of gate current to trigger the LASCR.) This is a very advantageous mode of operation, since it is possible to use a device with a forward breakover voltage much higher than any voltage likely to be encountered in the circuit, and to use only a moderate amount of trigger power to start the high conduction state. Circuit design and reliability are thus greatly enhanced. Once the gate has been used to trigger the thyristor into conduction it loses control, and the only method of turning a conducting device off is to reduce anode current below the holding current level. *(This applies to LASCR likewise, once it has been triggered.) Typically a ten to fifty microsecond gate pulse will initiate conduction.

* The gate turn-off switch (GTO), as its name suggests, can be turned off by means of its gate terminal. See Section 1.7.

As already mentioned, leakage current through a thyristor increases with temperature. The forward breakover voltage therefore tends to be quite temperature sensitive. At a high enough temperature (well above its maximum *rated* temperature) the thyristor loses completely its ability to block forward voltage and assumes characteristics just like a p-n diode.

In smaller SCR's, SCS's, or LASCR's this temperature effect on the breakover voltage can be minimized by extracting the forward leakage current from the gate. This prevents current from passing through the emitter of the n-p-n section of the device and maintains a low alpha in this section. It is also possible to actually increase the forward breakover voltage point on some small SCR's by this means. The effect of negative gate current on the forward blocking characteristics, however, becomes negligible on higher current SCR's due to the ineffectiveness of the gate in removing leakage current from the entire broad area of the n-p-n base region.

As might be expected, the gate cathode V-I characteristics of a gate-operated thyristor are essentially those of a p-n junction diode. Since the increase in h_{FE} with current is utilized, these devices are *current triggered* as opposed to voltage triggered, like a gas thyratron. This distinction must be kept in mind when designing triggering circuits, in that a relatively low impedance voltage source, or a current source is required.

1.6.2 V-I Characteristics of the Bidirectional Triode Thyristor (Triac)

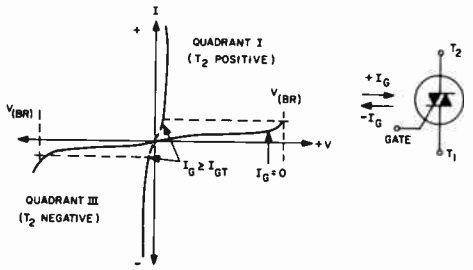


FIGURE 1.16 V-I CHARACTERISTIC OF TRIAC

Figure 1.16 is a plot of the V-I characteristics of a typical bidirectional triode thyristor, or triac. Note that the triac can block voltages of either polarity and conduct current in either direction (first quadrant and third quadrant). Conduction in either quadrant can be initiated by a positive or a negative gate signal. This gives the triac four possible operating modes, or "degrees of freedom."

First quadrant (T_2 positive with respect to T_1)—positive gate; (I^+)

First quadrant—negative gate; (I^-)

Third quadrant (T_2 negative with respect to T_1)—positive gate; (III^+)

Third quadrant—negative gate; (III^-)

Being analogous to two conventional SCR's in inverse parallel, the triac behaves in both quadrant I and quadrant III rather like a forward biased SCR. With $I_G = 0$ the device blocks voltage in either direction up to its rated $V_{(BR)}$, and only a small leakage current flows. With applied voltage greater than specified $V_{(BR)}$, the triac will "avalanche" and turn itself on. Because this avalanche phenomenon occurs in both directions the triac, unlike the

SCR, is "self protecting" against the effects of high voltage transients. Should a transient appear, the triac will merely turn on and be undamaged, providing the load current that flows is within its capabilities.

With gate current applied (either positive or negative) the region of the V-I characteristic between open gate breakover and conduction in either direction is removed, and the V-I characteristic becomes essentially that of a p-n rectifier. The triac has holding current characteristics similar to an SCR, and is affected by temperature in much the same way.

1.7 REVERSE BLOCKING THYRISTOR (SCR) TURN-OFF MECHANISM

When a reverse blocking thyristor is in the conducting state, each of the three junctions of Figure 1.17 are in a condition of forward bias and the two base regions (B_P, B_N) are heavily saturated with holes and electrons (stored charge).

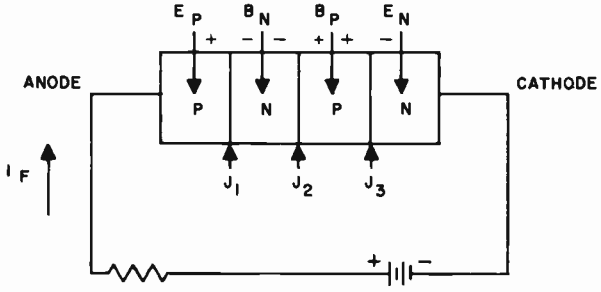


FIGURE 1.17 THYRISTOR BIASED IN CONDUCTING STATE (GATE OPEN CIRCUITED)

To turn-off the thyristor in a minimum time, it is necessary to apply a reverse voltage. When this reverse voltage is applied the holes and electrons in the vicinity of the two end junctions (J_1, J_3) will diffuse to these junctions and result in a reverse current in the external circuit. The voltage across the thyristor will remain at about +0.7 volts as long as an appreciable reverse current flows. After the holes and electrons in the vicinity of J_1 and J_3 have been removed, the reverse current will cease and the junctions J_1 and J_3 will assume a blocking state. The reverse voltage across the thyristor will then increase to a value determined by the external circuit. Recovery of the device is not complete, however, since a high concentration of holes and electrons still exists in the vicinity of the center junction (J_2). This concentration decreases by the process of recombination in a manner which is largely independent of the external bias conditions. After the hole and electron concentration at J_2 has decreased to a low value, J_2 will regain its blocking state and a forward voltage (less than $V_{(BR)}$) may be applied to the thyristor without causing it to turn-on. The time that elapses after the cessation of forward current flow and before forward voltage may safely be reapplied is called the thyristor "turn-off time," t_o, and is usually in the order of 10-15 microseconds long.

1.8 TRIAC TURN-OFF MECHANISM

Because the triac is capable of conducting current in both directions, it

cannot be turned off like a conventional reverse blocking thyristor. If the voltage across a conducting triac were instantaneously reversed for instance, the "recovery" current that flowed would merely turn the device on in the opposite direction! To turn a triac off successfully, the current through it must be reduced below the holding current by reduction of the applied voltage *to zero.* Sufficient time must then elapse before the reapplication of voltage (in either direction) to allow natural recombination of any stored charge. In 50 or 60 Hertz AC circuits, which are the main applications for the triac, the rate of change of voltage near the zero current point does allow proper commutation* in this manner.

1.9 COMPARISON OF THYRISTORS WITH OTHER POWER SEMICONDUCTORS

It will be noted that the low current h_{FE} of the p-n-p and n-p-n parts of a thyristor must be low in order to have the device block in the forward direction. In an ordinary three layer silicon power transistor, it is desirable to have h_{FE} as high as possible in order to achieve a high current gain. Unfortunately, however, high h_{FE} is obtained in most silicon transistors by using very thin base regions, and a thin base between two low resistivity regions is incompatible with high voltage. The wide base regions in the thyristor, necessary to achieve low h_{FE} are compatible with high voltages so that the thyristor is inherently a higher voltage device. The use of wide base regions is also an advantage from the standpoint of ease of manufacture and reproducibility of characteristics. An advantage of the thyristor over power transistors is the amount of drive necessary to full conduction. In many silicon power transistors, it is necessary to inject up to half an ampere of continuous base current in order to conduct 5 amperes from collector to emitter. In a thyristor, the amount of current conducted is dependent only on the external circuit once the device has been triggered. Thus a trigger current of 50 ma applied for only a few microseconds is all that is necessary to allow conduction of any current from a few milliamperes to hundreds of amperes. The high current capabilities of the thyristor, as contrasted to a transistor, are due to more effective use of junction area for current conduction.

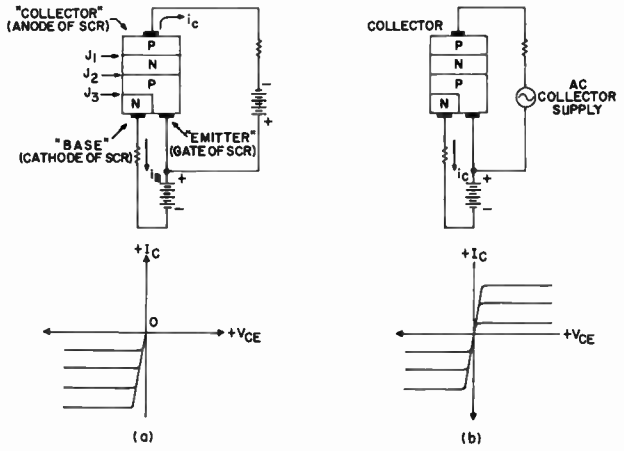
1.10 THYRISTOR USED AS A REMOTE BASE TRANSISTOR

As already described, a reverse blocking thyristor structure may be visualized as consisting of two interconnected transistors. When the structure is conventionally biased, i.e., *positive* anode to cathode voltage, *positive* gate to cathode voltage, the transistors act as a regenerative pair and give the p-n-p-n device its normal bistable characteristics. A p-n-p-n structure may be biased, however, so that the transistors are *unable* to regenerate, and in this case the bistable action is eliminated. The device, when so biased, exhibits the linear characteristics of an amplifier. Referring to Figure 1.18, a negative bias on the base lead with respect to the emitter lead causes electrons to be injected across junction J3 for collection at J2. Upon collection at J2 these electrons furnish base drive for the p-n-p section in much the same way as if a lead were attached directly to it. Hence the name "remote base" transistor. Com-

*See Section 7.1.4 and Section 19.10.

mon-emitter current gains (beta) vary from much less than unity to above five (5), depending on the characteristics of the parent p-n-p-n device. Since in most cases the "inverse beta"* is approximately equal to the forward beta, the devices are also usable as symmetrical AC amplifiers or switches.

*Beta with collector used as the emitter, and vice versa.



(a) p-n-p-n Structure Biased as p-n-p Transistor

(b) p-n-p-n Structure Used as Symmetrical Transistor

FIGURE 1.18 REMOTE BASE TRANSISTOR

1.11 GATE TURN-OFF SWITCH OR GATE CONTROLLED SWITCH

The gate turn-off switch is a four layer p-n-p-n device similar in construction to the SCR. Like the SCR, the GTO is triggered into conduction by raising its loop gain to unity. In the simple two transistor p-n-p-n analogue of Figure 1.8 with the device switched on, assume that h_{FE1} equals h_{FE2} so that equal currents flow in each transistor section. If the p-n-p transistor's collector current were diverted away from the n-p-n transistor's base region and out of the gate lead, the n-p-n transistor would cut-off, $h_{FE1} \times h_{FE2}$ would drop below unity, and the p-n-p-n device would revert to its forward blocking state. Turn-off gain, defined as the ratio of anode current flowing prior to turn-off to negative gate current required to effect turn-off, in this case would be at least two (2). If h_{FE2} is now made much less than unity when the device is in its "on" state, and h_{FE1} is made greater than unity to maintain $h_{FE} \cdot h_{FE1} = 1$, only a small percentage of the total anode current will flow in the collector of the p-n-p transistor. It is this current that is withdrawn to turn the GTO "off." For a typical device, gains from 5 to 25 are realizable depending on current, temperature gate pulse duration and other variables. Because of the difficulties in ensuring that control can be maintained by the gate contact at high cathode current densities (due to cross-biasing effects), gate turn-off devices operate at much lower current densities than SCR's and are therefore less economical. In addition, the recent availability of high voltage high gain silicon power transistors with superior saturation ("on" voltage) characteristics has tended to reduce the demand for gate turn-off devices.

REFERENCES

1. "Nomenclature and Definitions for Semiconductor Devices," International Electrotechnical Commission, Geneva, Switzerland, IEC Document 47 (Central Office) 43, August 1964.

2. Warburton, Lootens, Staviski, "Pressure Contact Semiconductor Devices," IEEE IGA Conference Record, October 1966.

3. Gentry, Gutzwiller, Holonyak and Von Zastrow, "Semiconductor Controlled Rectifiers . . . Principles and Application of p-n-p-n Devices," Prentice-Hall, 1964.

4. Moll et al, "PNPN Transistor Switches," Proceedings IRE, Vol. 44, Septemper 1956, p. 1174-1182.

5. Gentry, Scace and Flowers, "Bidirectional Triode p-n-p-n Switches," Proceedings of the IEEE, Vol. 53, No. 4, April 1965.

2 SYMBOLS AND TERMINOLOGY

2.1 SEMICONDUCTOR GRAPHICAL SYMBOLS

Fig. 2.1 shows graphical symbols of the types of semiconductors discussed and employed in the circuits of this Manual. At the time of this writing (Summer 1966) a revision of the standards for semiconductor device graphical symbols is in process. We do not feel that it would serve any useful purpose at this time to arbitrarily introduce symbols through any proposed but non-approved standards. We feel it to be more appropriate to confine Fig. 2.1 to the symbols used in this Manual. These symbols are mostly popular usage ones, and conform to existing and most probable future standards as much as possible. The symbols are circuit-oriented. The V-I characteristic of a device in a four-quadrant representation relates the graphical symbol to its basic terminal electrical characteristic of interest to the circuit engineer rather than to its semiconductor device geometry.

2.2 SCR TERMINOLOGY

The following tabulation defines the terminology used in SCR specifications. As in the case of graphical symbols (Section 2.1) we try to conform to existing standards wherever possible. At the time of this writing, letter symbols are again under consideration by standards groups. However, in view of existing industry specification sheets this Manual uses the currently accepted letter symbols from the proposed IEEE Standards on Solid State Devices (4/16/63).

2.2.1 SCR Ratings

A rating is a limiting condition or capability (either maximum or minimum) established for the device within which the device will perform in accordance with its design objectives.

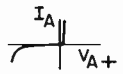
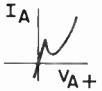
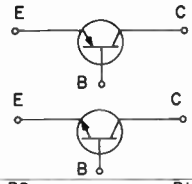
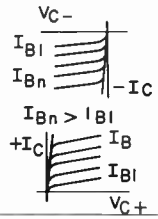
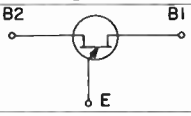
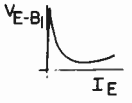
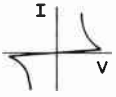
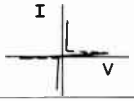
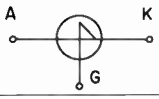
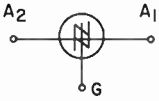
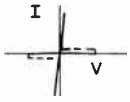
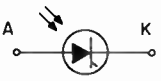
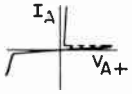
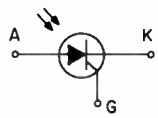
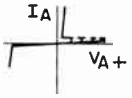
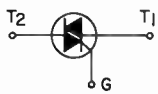
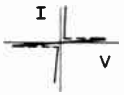
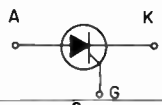
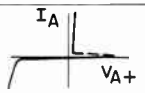
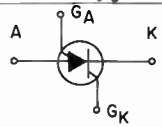
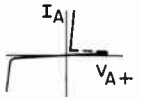
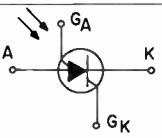
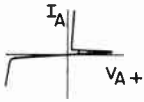
NAME OF SEMICONDUCTOR DEVICE	GRAPHICAL SYMBOLS USED IN THIS MANUAL	MAIN TERMINAL V – I CHARACTERISTIC
DIODES		
RECTIFIER DIODE		
BREAKDOWN (ZENER AND AVALANCHE) DIODE a) UNIDIRECTIONAL	PREFERRED:  ALTERNATE: 	
b) BIDIRECTIONAL (ALSO USED FOR THYRECTOR SELENIUM A C VOLTAGE SUPPRESSOR)	PREFERRED:  ALTERNATE: 	
TUNNEL DIODE	PREFERRED:  ALTERNATE: 	
TRANSISTORS		
p – n – p n – p – n		
UNIJUNCTION (n – BASE)		
TRIGGER DIAC		

FIGURE 2.1 SEMICONDUCTOR GRAPHICAL SYMBOLS

THYRISTORS

DIAC (BIDIRECTIONAL DIODE THYRISTOR)		
SUS (SILICON UNILATERAL SWITCH)		
SBS (SILICON BILATERAL SWITCH)		
LAS (LIGHT ACTIVATED SWITCH) LIGHT ACTIVATED REVERSE BLOCKING DIODE THYRISTOR	* 	
LASCR (LIGHT ACTIVATED SEMICONDUCTOR CONTROLLED RECTIFIER) LIGHT ACTIVATED REVERSE BLOCKING TRIODE THYRISTOR	* 	
TRIAC (BIDIRECTIONAL TRIODE THYRISTOR)		
SCR (SEMICONDUCTOR CONTROLLED RECTIFIER) REVERSE BLOCKING TRIODE THYRISTOR		
SCS (SILICON CONTROLLED SWITCH), REVERSE BLOCKING TETRODE THYRISTOR		
LASCS (LIGHT ACTIVATED SILICON CONTROLLED SWITCH); LIGHT ACTIVATED REVERSE BLOCKING TETRODE THYRISTOR.	* 	

A = ANODE E = EMITTER
B = BASE G = GATE
C = COLLECTOR K = CATHODE

NOTE: CIRCLES AROUND GRAPHICAL SYMBOLS ARE OPTIONAL EXCEPT WHERE SHOWN *. IN THESE CASES CIRCLE DENOTES AN ENVELOPE THAT EITHER ENCLOSES A NON-ACCESSIBLE TERMINAL OR TIES A DESIGNATOR INTO SYMBOL.

FIGURE 2.1 SEMICONDUCTOR GRAPHICAL SYMBOLS

TERMINOLOGY	SYMBOL	DEFINITION
Repetitive Peak Reverse Voltage gate open	V_{ROM}(rep)	Maximum allowable instantaneous value of repetitive reverse (negative) voltage that may be applied to the reverse blocking thyristor anode terminal with gate terminal open. While this value of voltage does not necessarily represent a "breakdown" voltage, it should never be exceeded except by the transient rating if the device has such a rating. General Electric reverse blocking thyristor's are capable of handling this voltage satisfactorily with negative gate voltage also.
Non-Repetitive Peak Reverse Voltage, gate open	V_{ROM}(non-rep)	Maximum allowable instantaneous value of reverse (negative) voltage including all non-repetitive transient voltages, but excluding all repetitive transient voltages, that may be applied to the reverse blocking thyristor anode terminal with gate terminal open. General Electric reverse blocking thyristors are capable of handling this voltage satisfactorily with negative gate voltage also.
Peak Forward Blocking Voltage, gate open	V_{FOM}	Maximum instantaneous value of forward blocking voltage (anode terminal positive) including transient voltages permitted by the manufacturer under stated conditions and which will not switch the reverse blocking thyristor to the on-state.
Peak Forward Voltage	PFV	Maximum instantaneous value of forward voltage permitted by the manufacturer under stated conditions and which may cause the reverse blocking thyristor to switch to the on-state. If anode breakover occurs at a voltage lower than the PFV, no damage to the reverse blocking thyristor will occur.
Average Forward Current, On-State	$I_{F(AV)}$	Maximum continuous DC current which may be permitted to flow in the forward direction (from anode to cathode) under stated conditions of frequency, temperature, reverse voltage, and current waveform.

2.2.2 SCR Characteristics

A characteristic is a measurable device parameter given to describe the performance of the device.

TERMINOLOGY	SYMBOL	DEFINITION
Forward Break-over Voltage	$V_{(BR)F}$	Maximum positive voltage on the anode terminal with respect to the cathode terminal for which the small-signal resistance is zero with stated gate termination. This is also the voltage at which a thyristor switches into the conductive state.
Instantaneous Forward Current, On-State	i_F	Instantaneous value of anode current flowing into the thyristor in the conducting state.
Instantaneous On-Voltage (Forward Voltage Drop)	v_F	Instantaneous voltage drop between anode and cathode terminals during conduction of current from anode to cathode terminals while the device is in the on-state.
Full Cycle Average On-Voltage (Forward Voltage Drop)	$V_{F(AV)}$	On-voltage averaged over one complete cycle with stated forward current flowing in a 60 Hertz single phase half wave rectifier with resistive load and no circuit triggering angle delay.
Instantaneous Forward Gate Current	i_{GF}	Instantaneous current flowing between gate and cathode terminals in a direction to forward bias the gate junction.
Instantaneous Forward Gate Voltage	v_{GF}	Instantaneous forward voltage between gate and cathode terminals with anode terminal open.
DC Gate Trigger Current	I_{GT}	Forward gate current required to trigger a thyristor at stated temperature conditions.
DC Gate Trigger Voltage	V_{GT}	Gate voltage with I_{GT} flowing but prior to start of anode conduction.
Effective Irradiance to Trigger	H_{ET}	The amount of incident radiant flux density which is effective in causing a light activated device to switch to the conducting state. This is the integral of the product of the spectral response curve of the cell and the spectral distribution of the energy source, expressed in watts per square centimeter, which causes the device to switch.

TERMINOLOGY	SYMBOL	DEFINITION
	I_O	$I_{F(AV)}$ under specific condition of half-wave rectified sine-wave current, 180° conduction angle.
RMS Forward Current, On-State	I_f	Maximum continuous RMS current which may be allowed to flow in the forward direction under stated conditions. "Average forward current" rating above applies simultaneously.
Peak One-Cycle Surge Forward Current	I_{FM}(surge)	Maximum allowable non-recurrent peak current of a single forward cycle (8.3 milliseconds duration) in a 60-cps single-phase resistive load system. The surge may be preceded and followed by maximum rated voltage, current, and junction temperature conditions, and maximum allowable gate power may be concurrently dissipated. However, specified limitations on anode current during switching should not be exceeded.
I squared t	I^2t	This is a measure of maximum forward non-recurring overcurrent capability for very short pulse durations (8.3 milliseconds or less, unless otherwise specified). I is in RMS amperes, and t is pulse duration in seconds. The same conditions as listed above for I_{FM} (surge) apply.
Peak Reverse Gate Voltage	V_{GRM}	Maximum allowable peak reverse voltage between the gate terminal and the cathode terminal.
Peak Gate Power Dissipation	P_{GM}	Maximum instantaneous value of gate power dissipation.
Average Gate Power Dissipation	$P_{G(AV)}$	Maximum allowable value of gate power dissipation averaged over a full cycle.

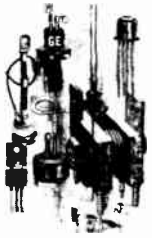
TERMINOLOGY	SYMBOL	DEFINITION
Holding Current	I_{H}	Value of i_F below which thyristor returns to forward blocking state after having been in forward conduction under stated temperature and gate termination conditions.
Latching Current	I_L	Value of minimum anode current in order for thyristor to switch to the on-state, and to remain in the on-state after removal of the gate trigger pulse under specified condition.
Instantaneous Forward Blocking Current	i_F	Instantaneous anode current at stated conditions of forward blocking voltage, junction temperature, and gate termination.
Instantaneous Reverse Blocking Current	i_R	Instantaneous anode current at stated conditions of negative anode voltage, junction temperature, and gate termination.
Delay Time	t_d	Time interval between the time the gate current pulse reaches 10% of its final value and the time when the resulting forward current reaches 10% of its maximum value during switching from the off-state to the on-state into a resistive load under stated conditions.
Rise Time	t_r	Time interval between the time the forward current reaches 10% of its maximum value and the time the forward current reaches 90% of its maximum value during switching from the off-state to the on-state into a resistive load under stated conditions.
Turn-On Time	t_{on}	Sum of delay time and rise time.
Turn-Off Time	t_{off}	The time interval between zero current and the time of reapplication of positive forward blocking voltage under specified conditions with the device remaining in the off-state after having been in the on-state.

TERMINOLOGY	SYMBOL	DEFINITION
Reverse Recovery Time	t_{rr}	The time interval between zero current and the time at which the reverse current through the device has reached a specified value (usually 10% of the peak reverse recovery current) under specified conditions after having been in the on-state.
Thermal Resistance	θ	Temperature rise per unit power dissipation of a designated point above the temperature of a stated external reference point under conditions of thermal equilibrium.
Transient Thermal Impedance	$\theta_{(t)}$	Temperature rise per unit power dissipation of junction above stated reference point for specified period of time after application of step increase of junction power dissipation with device case or ambient temperature held constant.
Junction Temperature	T_J	Virtual junction temperature.
Case Temperature	T_C	Case Temperature.
Ambient Temperature	T_A	Ambient temperature.
Storage Temperature	T_{stg}	Storage temperature.

NOTE: Symbol to be used where asterisk (*) is shown in above tables:

O = Gate terminal is open-circuited or device has no gate terminal.
S = Gate terminal is short-circuited to the terminal of the adjacent region.
R = Gate terminal is returned to the terminal of the adjacent region through a stated resistance.
V = Gate terminal is biased with respect to the adjacent region at stated voltage.
X = Termination unspecified.

3 RATINGS AND CHARACTERISTICS OF THYRISTORS



The family of thyristor devices has in common a switching capability in one or two quadrants of its V-I characteristics. Thyristor devices used as power switches have in common the necessity for proper design and specification of their heat dissipation and heat transfer properties. Furthermore, thyristors are switched into the on-state either by applying a triggering signal to their gate or by increasing forward voltage until it exceeds the forward breakover voltage characteristic. These and other common properties of thyristor devices allow a uniform approach to thyristor characterization which need differ only in detail when applied to a specific thyristor device like, for example, an SCR or a triac.

In the following sections of this chapter the discussion is largely in terms of SCR's. Most of this material is applicable, however, to other thyristor devices. Specialized characterization information is presented in Chapter 7 for triacs and in Chapter 13 for light-activated thyristors.

3.1 JUNCTION TEMPERATURE

The operating junction temperature range of thyristors varies for the individual types. A low temperature limit may be required to limit stress in the silicon crystal to safe values. This type of stress is due to the difference in the thermal coefficients of expansion of the materials used in fabricating the cell subassembly. The upper operating temperature limit is imposed because of the temperature dependence of the forward breakover voltage and because of thermal stability considerations. The upper storage temperature limit in some cases may be higher than the operating limit. It is selected to achieve optimum reliability and stability of characteristics with time.

The rated maximum operating junction temperature can be used to determine steady-state and recurrent overload capability for a given heatsink system and maximum ambient temperature. Conversely, the required heatsink system may be determined for a given loading of the semiconductor device by means of the classic thermal impedance approach presented in Sections 3.3 and 3.4.

Transiently the device may actually operate beyond its specified maximum operating junction temperature and still be applied within its ratings. An example of this type of operation occurs within the specified forward nonrecurrent surge current rating. Another example is the local temperature rise of the junction due to the switching dissipation during the turn-on of a thyristor under some conditions. It is impractical at this time to establish temperature limits for these types of operating stresses from both a rating as well as an applications point of view. Therefore, such higher-than-rated temperature operation must remain implicit in other ratings established for the device.

3.2 POWER DISSIPATION

The power generated in the junction region in typical thyristor operation consists of the following five components of dissipation:

a. Turn-on switching
b. Conduction
c. Turn-off or Commutation
d. Blocking
e. Triggering

Forward conduction losses are the major source of junction heating for normal duty cycles and power frequencies. However, for very steep (high di/dt) current waveforms or high operating frequencies turn-on switching losses may become the limiting consideration. Such cases are discussed in Sections 3.7 and 3.8.

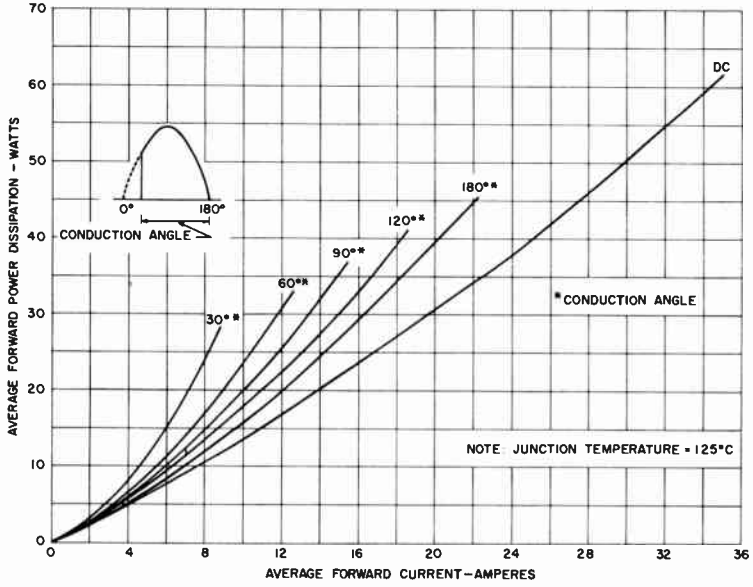


FIGURE 3.1 AVERAGE FORWARD POWER DISSIPATION FOR C35 SERIES SCR

Figure 3.1 gives forward conduction loss in average watts for the C35 SCR as a function of average current in amperes for various conduction angles for operation up to 400 Hz. This type of information is given on the specification sheet for each type of SCR. These curves are based on a current waveform which is the remainder of a half-sine wave which results when delayed angle triggering is used in a single phase resistive load circuit. They are conservative for rectangular current waveforms with the same average value and conduction angle. These power curves are the integrated product of the instantaneous anode current and forward voltage drop. This integration can be performed graphically or analytically for conduction angles other than those listed, using the forward voltage-current characteristic curves for the specific device.

Both the forward and reverse blocking losses are determined by integration of the appropriate blocking E-I curves on the specification sheet.

Gate losses are negligible for pulse types of triggering signals. Losses may become more significant for gate signals with a high duty cycle, or for SCR's in a TO-5 or smaller package. The losses may be calculated from the gate E-I curves shown on the triggering characteristics for the specific type of SCR. Highest gate dissipation will occur for an SCR whose gate characteristics intersect the gate circuit load line at its midpoint. For a more detailed discussion of the gate characteristic and its load line, see Chapter 4.

Turn-on switching ratings are discussed in Section 3.8. Turn-off is discussed in Chapter 5.

3.3 THERMAL RESISTANCE

The heat developed at the junctions by the foregoing power losses flows into the case and thence to the heatsink. The junction temperature rises above the stud, or case, temperature in direct proportion to the amount of heat flowing from the junction and the thermal resistance of the device to the flow of heat. The following equation defines the relationship under steady-state conditions:

$$T_J - T_C = P\theta \tag{3.1}$$

where T_J = average junction temperature, °C
T_C = case temperature, °C
P = average heat generation at junction, watts
θ = steady-state thermal resistance between junctions and bottom face of hex or case, °C/watt

Equation 3.1 can be used to determine the allowable power dissipation and thus the continuous pure DC forward current rating of an SCR for a given case temperature through use of the forward E-I curves. For this purpose, T_J is the maximum allowable junction temperature for the specific device. The maximum values of θ and T_J are given in the specifications.

3.4 TRANSIENT THERMAL IMPEDANCE

Equation 3.1 is not satisfactory for finding the peak junction temperature when the heat is applied in pulses such as the recurrent conduction periods in an AC circuit. Solution of Equation 3.1 using the peak value of P is over-conservative in limiting the junction temperature rise. On the other hand, using the average value of P over a full cycle will underestimate the peak temperature of the junction. The reason for this discrepancy lies in the thermal capacity of the semiconductor, that is, its characteristic of requiring time to heat up, its ability to store heat, and its cooling before the next pulse.

Compared to other electrical components such as transformers and motors, semiconductors have a relatively low thermal capacity, particularly in the immediate vicinity of the junction. As a result, devices like the SCR heat up very quickly upon application of load, and the temperature of the junction may fluctuate during the course of a cycle of power frequency. Yet, for very short overloads this relatively low thermal capacity may be significant in

arresting the rapid rise of junction temperature. In addition, the heatsink to which the semiconductor is attached may have a thermal constant of many minutes. Both of these effects can be used to good advantage in securing attractive intermittent and pulse ratings sometimes well in excess of the published continuous DC ratings for a device.

The thermal circuit of the SCR can be simplified to that shown in Figure 3.2. This is an equivalent network emanating in one direction from the junctions and with the total heat losses being introduced at the junctions only. This simplification is valid for current amplitudes at which I^2R losses are small in comparison with the junction losses. In Figure 3.2 the ambient is the reference level. If a small stud type device is mounted to an infinite heatsink, the heatsink temperature can be used as a reference. However, with larger devices, the case to heatsink thermal resistance is relatively large compared to the junction-case thermal resistance. In such cases the case or hex temperature should be used as a reference.

When a step pulse of heating power P is introduced at the junctions of the SCR (and of the thermal circuit) as shown in Figure 3.3A, the junction temperature will rise at a rate dependent upon the response of the thermal network. This is represented by the curve T_{heat} in Figure 3.3B. After some sufficiently long time t_1, the junction temperature will stabilize at a point $\Delta T = P\theta$ above the ambient (or case) temperature. This is the steady-state value which is given by Equation 3.1. θ is the sum of R_1 through R_n in the equivalent thermal circuit of Figure 3.2.

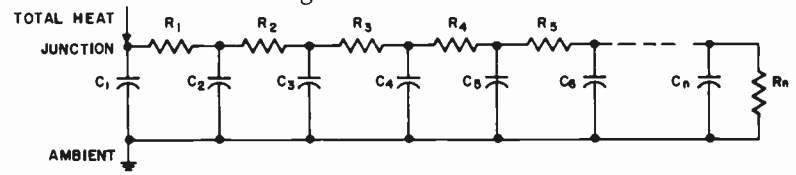


FIGURE 3.2 SIMPLIFIED EQUIVALENT THERMAL CIRCUIT FOR A POWER SEMICONDUCTOR.

If the power input is terminated at time t_2 after the junction temperature has stabilized, the junction temperature will return to ambient along the locus indicated by T_{cool} in Figure 3.3B. It can be shown that curves T_{heat} and T_{cool} are conjugates of one another,[1] that is,

$$T_{cool} = \Delta T - T_{heat} = P\theta - T_{heat} \qquad (3.2)$$

By dividing the instantaneous temperature rise of curve T_{heat} in Figure 3.3B by the power P causing the rise, the dimensions of the ordinate can be converted from °C to °C/watt. This latter set of dimensions is that of thermal resistance, or as it is more precisely termed: the transient thermal impedance $\theta_{(t)}$. Figure 3.4 shows a plot of transient thermal impedance for the C35 SCR both when mounted to an infinite heatsink and to a four-inch square copper fin.

Transient thermal impedance information for a device can be obtained by monitoring junction temperature at the end of a well-defined power pulse or after a known steady-state load has been removed. Junction temperature is measured by use of one of the temperature-sensitive junction characteristics such as forward voltage drop at low currents. Conversion of heating data to cooling data, or vice versa, can be accomplished through the use of Equation 3.2.

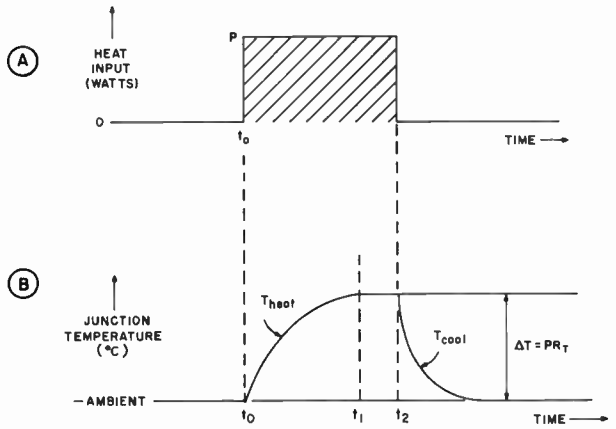


FIGURE 3.3 RESPONSE FOR SCR JUNCTION TO STEP PULSE OF HEATING POWER

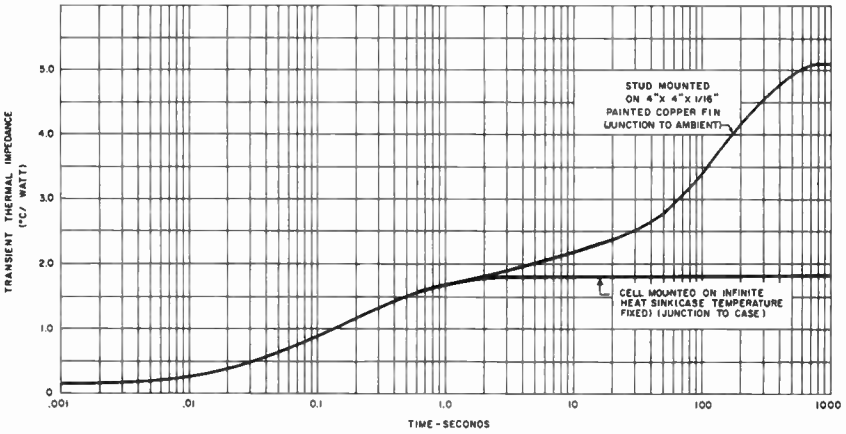


FIGURE 3.4 TRANSIENT THERMAL IMPEDANCE OF C35 SCR

In order to be able to use the transient thermal impedance curve with confidence in equipment designs, the curve represents the highest values of thermal impedance for each time interval that can be expected from the manufacturing distribution of the products. An additional slight safety factor is included to provide conservative application under all types of repetitive pulse loads.

The transient thermal impedance curve approaches asymptotic values at both the long time and short time extremes. For very long time intervals the transient thermal impedance approaches the steady-state thermal resistance θ.

For times less than 1 millisecond the value at 1 millisecond may be extrapolated by $1/\sqrt{t}$. This is based on assuming that the time of interest is sufficiently small so that all heat generated at the semiconductor junction may be considered to flow by one-dimensional diffusion within the silicon pellet. For times small compared to the thermal time constant of the path junction-to-face of the silicon pellet this assumption is valid. For extremely short times, however, during which current density, and hence heating, is non-uniform thermal resistance is not a valid approach.

For example the C35 transient thermal impedance at 10 μ seconds may be estimated as $\frac{0.14}{\sqrt{10^{-3}/10^{-5}}} = .014°\ C/W$

However, the extrapolated values are valid only for times after the SCR has turned on fully. These values should, in other words, not be used during the switching interval (see Section 3.8). It is, furthermore, not suggested to extrapolate below 10 μ seconds. For maximum utilization of semiconductor devices in the microsecond region additional factors must be considered and other methods of rating and life testing must be used.

3.5 RECURRENT AND NON-RECURRENT CURRENT RATINGS

3.5.1 Introduction

The discussion under all parts of this section and Section 3.6 applies to the conventional rating system presently used for thyristors when turn-on switching dissipation is negligible. Turn-on switching characterization is discussed in Section 3.7; current ratings for high frequency operation which cannot neglect turn-on switching losses are discussed in Section 3.8.

When a semiconductor device is applied in such a manner that its maximum allowable peak junction temperature is not exceeded the device is applied on a *recurrent* basis. Any condition that is a normal and repeated part of the application or equipment in which the semiconductor device is used must meet this condition if the device is to be applied on a recurrent basis. Section 3.6 gives methods of checking peak junction temperature. These enable the designer to properly apply the device on a recurrent duty basis.

A class of ratings that makes the SCR and the triac truly power semiconductors are the *non-recurrent* current ratings. These ratings allow the maximum (recurrent) operating junction temperature of the device to be exceeded for a brief instant. This gives the device an instantaneous overcurrent capability allowing it to be coordinated with circuit protective devices. The specification bulletin gives these ratings in terms of surge current and I^2t. These ratings, then, should only be used to accommodate unusual circuit conditions not normally a part of the application, such as fault currents. Non-recurrent ratings are understood to apply to load conditions that will not occur more than a limited number of times in the course of the operating life of the equipment in which the SCR is finding application. Also, non-recurrent ratings are understood to apply only when they are not repeated before the peak junction temperature has returned to its maximum rated value or less.

3.5.2 Average Current Rating (Recurrent)

Average current rating versus case temperature is shown in the specification sheet as for the C35 series SCR in Figure 3.5. These curves specify the maximum allowable average anode current ratings of the SCR as a function of case temperature and conduction angle. Points on these curves are selected so that the junction temperature under the slated conditions does not exceed the maximum allowable value. The maximum rated junction temperature of the C35 SCR is 125°C.

The curves of Figure 3.5 include the effects of the small contribution to total dissipation by reverse blocking, gate drive, and switching up to 400 Hz. For devices which are lead mounted or housed in small packages, like the TO-5 or TO-18, the forward current rating may be substantially affected by gate drive dissipation. Where this becomes important it is so indicated on the specification sheet.

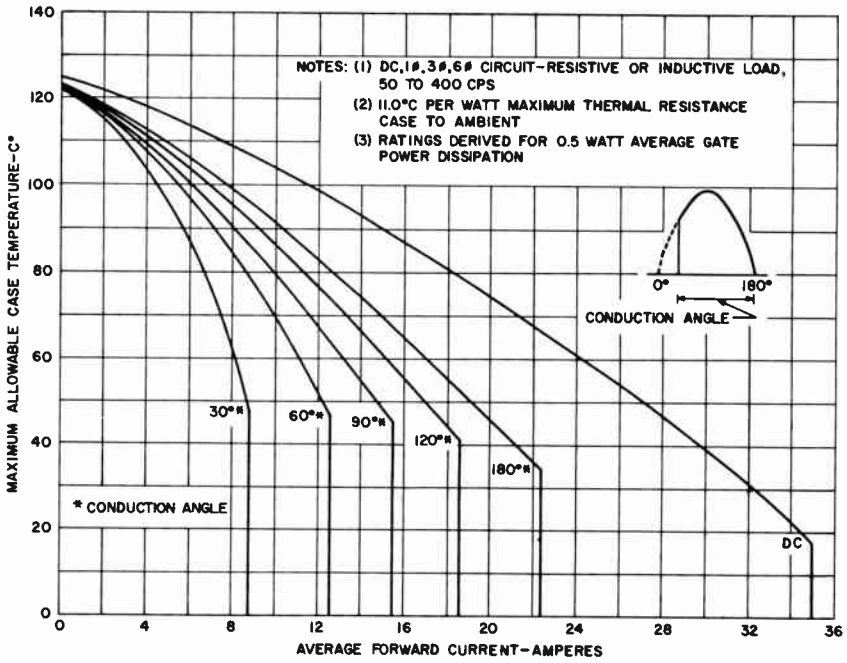


FIGURE 3.5 MAXIMUM AVERAGE CURRENT RATINGS FOR C35 SERIES SCR

If the C35 in a single phase resistive load circuit is triggered as soon as its anode swings positive, the device will conduct for 180 electrical degrees. If the case temperature is maintained at 80°C or less, the C35 is capable of handling 13 amperes average current as indicated in Figure 3.5. If the triggering angle is retarded by 120 degrees, the C35 will conduct for only the 60 remaining degrees of the half cycle. Under these conditions, the maximum rated average current at 80°C stud temperature is 9 amperes, substantially less than for 180 degrees conduction angle.

3.5.3 RMS Current (Recurrent)

It will be noted in Figure 3.5 that the curves for the various conduction waveshapes have definite end points. These points represent identical RMS values, and as such an RMS rating is implicit in the curves of Figure 3.5.

For example, the C35 is rated 35 amperes DC or $\frac{35}{1.57} = 22.3$ amperes average in a half-wave, or 180° conduction angle, circuit. The factor 1.57 is the form factor giving the ratio of RMS to average values for a half wave sinusoidal waveform. By the definition of RMS values, the RMS and average values are identical for a direct current. The RMS current rating, as shown on the specification sheet for individual SCR's, is necessary to prevent excessive heating in resistive elements of the SCR, such as joints, leads, etc.

The RMS current rating can be of importance when applying thyristors to high peak current, low duty cycle waveforms. Although the average value of the waveform may be well within the ratings, it may be that the allowable RMS rating is being exceeded.

The average current values shown as phase control ratings in Figure 3.5 for a given and fixed basic RMS device current rating are for the resistive current waveform shown in the figure. Since the current form factor for the case of resistive loading is greatest, and since inductance in the path of the thyristor current will reduce its form factor, the average current ratings in Figure 3.5 are conservative for inductive current waveforms.

For inductive waveforms in which the thyristor current waveform is essentially rectangular, such as may occur in a phase-controlled rectifier operating near full output, most specification sheets show separate rating curves to reflect the improvement in form factor. However, such current waveforms are, of course, subject to the restriction of the allowable turn-on current rating of the device.

In other cases in which the current waveform may be half-sinusoidal in shape but of a base width less than half a period of the supply frequency as, for example, with discontinuous AC line current in an AC switch application[9] at large phase retard, greater utilization of the thyristor in terms of its average current versus temperature ratings (like in Figure 3.5) can be obtained by taking into account the improvement of form factor due to decreasing load power factor (greater inductance) when applying the device within its RMS current rating.

3.5.4 Arbitrary Current Waveshapes And Overloads (Recurrent)

Recurrent application of arbitrary waveshapes, varying duty cycles, and overloads requires that the maximum peak allowable junction temperature of the SCR not be exceeded. Section 3.6 gives information for determining this.

3.5.5 Surge And I^2t Ratings (Non-Recurrent)

In the event that a type of overload or short circuit can be classified as non-recurrent, the rated junction temperature can be exceeded for a brief instant, thereby allowing additional overcurrent rating. Ratings for this type of non-recurrent duty are given by the Surge Current curve and by the I^2t rating.

Figure 3.6 shows the maximum allowable non-recurrent surge current at rated load conditions. Note that the junction temperature is assumed to be at its maximum rated value (125°C for the C35); it is therefore apparent that the junction temperature will exceed its rated value for a short time.

The data shown in this curve are values of peak rectified sinusoidal waveforms on a 60 Hz basis in a half-wave circuit. The "one-cycle" point, therefore, gives an allowable non-recurrent half sine wave of 0.00834 seconds' duration (half period of 60 Hz frequency) of a peak amplitude of 150 amperes. The "20 cycle" point shows that 20 rectified half sine waves are permissible (separated by equal "off" times), *each* of an *equal* amplitude of 80 amperes.

I^2t ratings apply for non-recurrent overloads shorter than one half cycle. For such times the SCR behaves essentially like a resistance with a fixed thermal capacity and negligible power dissipating means, and displays a current capability which can be expressed as a constant I^2t, where I is the RMS value of current over an interval t. The I^2t rating of the SCR is given in the specifications. This rating assumes that the SCR is already in the conducting state. If the SCR is turned on into a fault, the current-time relationships (di/dt) during the turn-on interval must be within the device's switching capabilities. Section 3.7 discusses turn-on switching dissipation in greater detail.

Provided the above precautions are observed, fault and overcurrent protection can be approached in the same manner as for power rectifier diodes. Protection methods are discussed in Chapter 14.

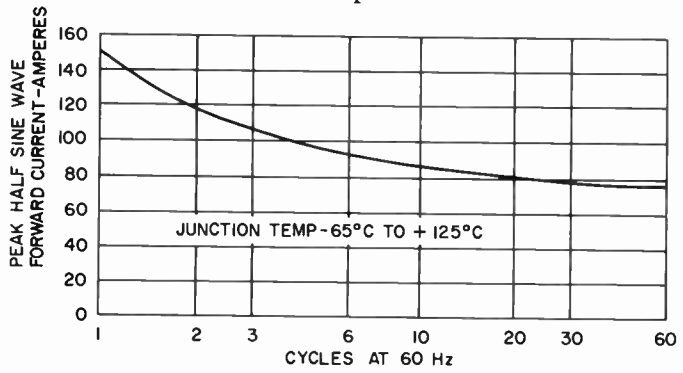


FIGURE 3.6 MAXIMUM ALLOWABLE NON-RECURRENT PEAK SURGE FORWARD CURRENT AT RATED LOAD CONDITIONS FOR C35 SERIES SCR.

3.6 BASIC LOAD CURRENT RATING EQUATIONS

3.6.1

In order for a device to be properly applied for recurrent load duty its

maximum allowable peak operation junction temperature must not be exceeded. By knowing the dissipation of a semiconductor device and its thermal response it is possible to meet this requirement by the method shown in Section 3.4.

The information given on the G-E specification sheet, in conjunction with the proper equation in Figure 3.7, allows the designer to calculate power semiconductor ratings for a variety of conditions (Ref. 1).

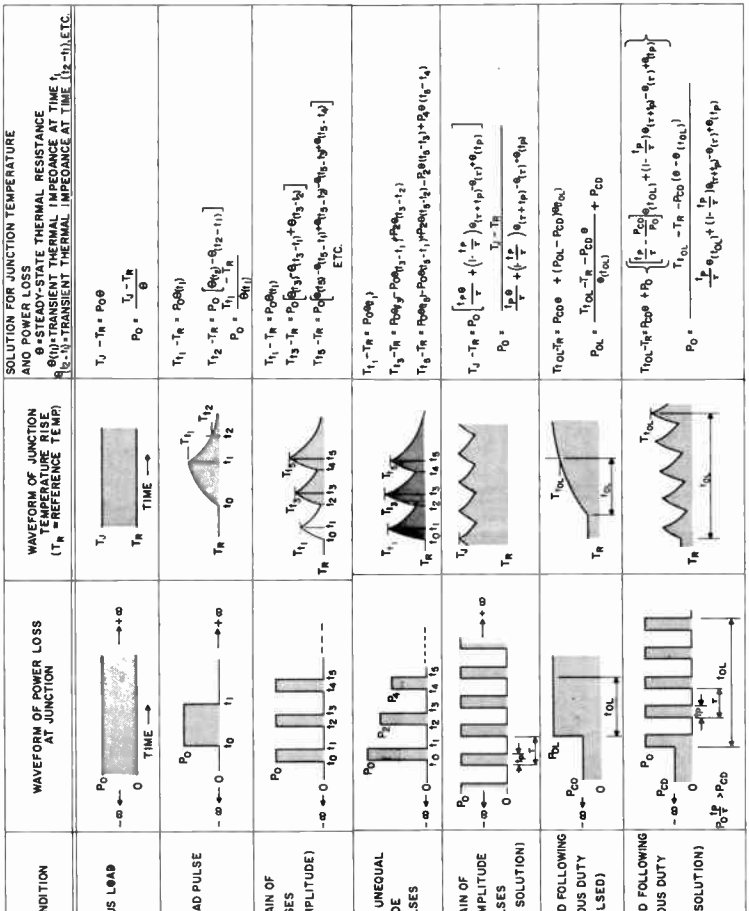


FIGURE 3.7 BASIC LOAD CURRENT RATING EQUATIONS

3.6.2 Treatment Of Irregularly Shaped Power Pulses—Approximate Method

In the preceding section solutions for junction temperature were given in response to step functions of power input. In many practical applications, the power pulse is not of this ideal shape for computation, and appropriate approximations must be made to convert the actual waveshape into a rec-

tangular form if the subsequent calculations are to be made as outlined.

Figure 3.8A illustrates the arbitrary waveshape of a power pulse that re-occurs at a period of τ seconds and has a peak value of P_{pk} watts and a full-cycle average of P_{avg} watts. For the purpose of calculating peak junction temperatures, this waveshape can be approximated by the rectangular waveshape of Figure 3.8B. This rectangular waveshape is selected to have the identical values of peak power P_{pk} and average power P_{avg} as Figure 3.8A by altering the pulse duration by a constant N to maintain the peak to average relationship. N is defined as the ratio of P_{avg} to P_{pk}.

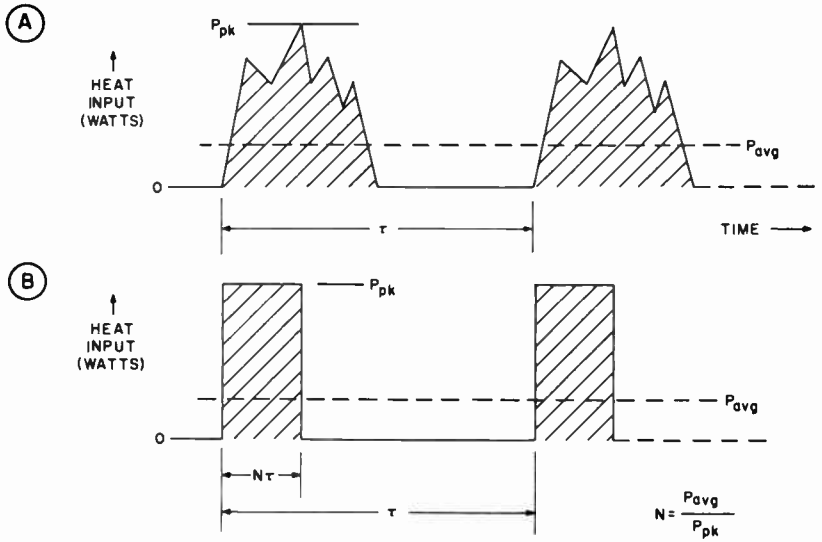


FIGURE 3.8 APPROXIMATING IRREGULARLY SHAPED HEATING PULSE WITH RECTANGULAR WAVESHAPES.

This translation into rectangular pulses of power ensures a "worst case" approximation since a rectangular pulse of power will always have an effect on temperature rise which is equal to or greater than the effect of any other pulse having the same peak and average power. In other words, a rectangular power pulse will raise the junction temperature higher than any other waveshape with the same peak and average values since it concentrates its heating effects into a shorter period of time, thus minimizing cooling during the pulse.

Figure 3.9A illustrates a case where a similar type of approximation can be used to shorten the calculations for peak junction temperature when the problem would otherwise be too laborious. It involves the case where a sequence of power pulses is periodically interrupted by a longer "off" period of zero power. This is typical of any repetitive or cyclical on-off type of load. Each burst of pulses can be represented by a single square-wave with introduction of only a relatively small error. This error will always yield a junction temperature higher than actual, and will thus provide a conservative application. In the equivalent waveshape shown in Figure 3.9B, the peak value of power P_{pk} is maintained the same as in Figure 3.9A. The duration of the equivalent rectangular waveshape is reduced to Nt_p where N is defined as P_{avg}/P_{pk}.

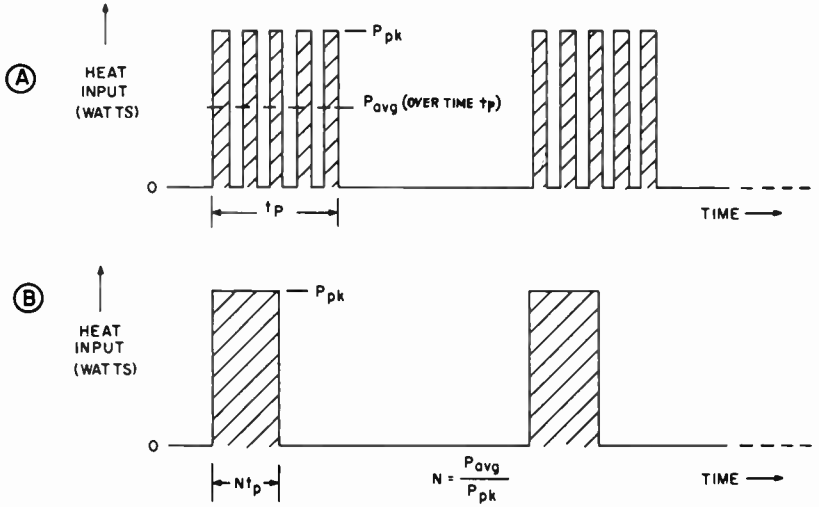


FIGURE 3.9 APPROXIMATING BURSTS OF PULSES WITH SINGLE RECTANGULAR PULSE OF POWER.

Sample Problem: Half wave sinusoidal current flows through a C35 SCR at 60 Hz. The full cycle average value of this current is 10 amperes. Approximate the heating effect of a sequence of four cycles of current by a single rectangular wave of power.

Solution:

$$I_{peak} = \pi\, I_{avg} = 10\,\pi = 31.4 \text{ amperes}$$

$V_{peak} = 1.7$ volts at 31.4 amps from published specifications on C35

$$P_{peak} = I_{peak} \times V_{peak} = 31.4 \times 1.7 = 53.4 \text{ watts}$$

Full cycle average P = 16 watts at 10 amps average current from published specifications on C35

$$P_{avg} \text{ over } 3\tfrac{1}{2} \text{ cycles (actual duration of heating)} = 16 \times \frac{4}{3\tfrac{1}{2}} = 18.3 \text{ watts}$$

$$N = P_{avg}/P_{peak} = 18.3/53.4 = 0.34$$

$$t = 3.5 \text{ cycles} \times 1/60 \text{ cps} = .0585 \text{ second}$$

$$Nt = 0.34 \times .0585 = 0.020 \text{ second}$$

Thus the heating effect of the four cycles of current can be approximated by a single rectangular pulse of power with amplitude of 53.4 watts and a duration of 0.020 second. This is a conservative approximation.

3.6.3 The Effect of Heatsink Design on the Transient Thermal Resistance Curve

Since the heatsink is a major component in the heat transfer path between junction and ambient, its design affects the transient thermal imped-

ance curve (Figure 3.4) substantially. When a semiconductor is manufactured and shipped to the user the manufacturer has no control over the ultimate heatsink and can only provide data on the heat transfer system between junction and case which is the part he manufactured. These type of data are presented in Figure 3.4 as the "Cell Mounted to Infinite Heatsink" curve.

The equipment designer can use this curve in developing a transient thermal impedance curve for the cell when mounted to a particular heatsink of his own design by means of a few simple calculations. These calculations assume that the temperature throughout the heatsink is uniform even under transient loading, thus permitting the heatsink to be represented by a single time constant. This is a good assumption for fins of relatively thick cross-section and fine effectiveness close to unity. This approach also assumes that the thermal capacity of the heatsink is large compared to the thermal capacity of the cell. By adding the calculated (or measured) transient thermal impedance of the fin to the "Infinite Heatsink" curve for the cell, the applicable curve can be plotted for the complete thermal system. The method can best be explained through an example illustrating how the second curve on Figure 3.4 (4" x 4" fin) can be calculated.

3.6.4 Example of Calculating the Transient Thermal Impedance Curve For a Specific Heatsink Design

Problem: A cell is mounted on a painted copper fin 1/16" thick and 4" on a side. The fin is subjected to free convection air conditions. Find the transient thermal impedance curve for a device mounted on this fin if the infinite heatsink curve in Figure 3.4 represents the thermal characteristics of the stud-mounted semiconductor. Assume that the case to fin contact resistance is negligible. In cases where the case to fin thermal resistance is a significant part of the total (as in some high power systems) this assumption cannot be made and the case to fin thermal resistance has to be added to the infinite heatsink curve.

Solution: From fin design curves (See Chapter 17):

$h_r = .005$ watt/inch^2 °C $\qquad h_c = .005$ watt/inch^2 °C

$h_{total} = h_r + h_c = .010$ watt/inch^2 °C

Fin thermal conductance $k = h \times A = .01 \times 4 \times 4$ inches$^2 \times 2$ sides $=$ 0.32 watt/°C

$$\text{Fin thermal resistance } \theta_f = \frac{1}{k} = \frac{1}{0.32} = 3.1 \text{ °C/watt}$$

$$\text{Fin thermal capacity } C = c\rho V = \frac{175 \text{ watt-seconds}}{\text{lb °C}} \times 0.32 \text{ lb/in}^3$$

$$\times 4 \text{ in.} \times 4 \text{ in.} \times 1/16 \text{ in.} = \frac{56 \text{ watt-seconds}}{\text{°C}}$$

$$\text{Thermal RC time constant} = 3.1 \text{ °C/watt} \times \frac{56 \text{ watt-seconds}}{\text{°C}} = 174 \text{ seconds}$$

Equation of transient fin thermal impedance, $\theta_{(t)F}$:

$$\theta_{(t)F} = \theta_F (1 - e^{-t/RC}) = 3.1 (1 - e^{-t/174})$$

The values of $\theta_{(t)F}$ are added to the infinite heatsink curve to secure the over-all $\theta_{(t)}$ of the system as indicated in Figure 3.4. Note that this fin makes a negligible contribution to the over-all thermal impedance of the cell-heatsink system at periods of time one second or less after application of power. In this area the fin behaves like an infinite heatsink, that is, one of zero thermal resistance. The fin-heatsink system reaches equilibrium around 1000 seconds. Thereafter the thermal capacity is no longer effective in holding down the junction temperature.

3.7 TURN-ON SWITCHING CHARACTERIZATION

In many cases the SCR may be assumed to turn on instantaneously. This assumption is valid if the rate of rise of anode current (di/dt) is slow compared to the time required for the semiconductor junctions to reach a state of full forward conduction at uniform current density.

The current ratings discussed in the preceding sections are based on such a condition of uniform current density. In other words, the peak junction temperature, on which the recurrent and non-recurrent current ratings are based, is assumed to occur uniformly across the entire junction interfaces.

In cases where the rate of rise of anode current (di/dt) is very rapid compared to the spreading velocity of the turn-on process across the junctions, local "hot spot" heating will occur due to high current density in those junction regions that have started to conduct.[7] Particularly, if the SCR is switched from a high blocking voltage at a very large value of di/dt, turn-on switching dissipation in localized regions of the SCR may lead to an excessive temperature rise and cause device failure at a "hot spot."

3.7.1 Definition of Rate of Rise of Anode Current (di/dt)

A definition of di/dt for an SCR must consist of a meaningful waveform, test conditions, and a reproducible test circuit. The waveform shown in Figure 3.10(a) is taken at a fairly linear rate of rise and at a somewhat critically damped tail-off. The reason for this is:

1. It is desirable to have the device subjected to a rate of rise of current that is fairly linear for a minimum amount of time t_1. It has been shown that if the device is going to fail under a di/dt stress, it is most likely to occur in a time less than 1 μsecond; therefore t_1 was chosen to be equal to or greater than 1 μsecond.

2. The form of tail-off of the current wave was chosen so that it does not include a significant reverse recovery interval, which, under some conditions, could impose an additional stress on the device thus obscuring the primary phenomenon with which the test is concerned, namely, di/dt.

This circuit lends itself to both the establishing of di/dt ratings by test to failure; or the circuit can be employed for go-no go testing in the verification of established ratings.

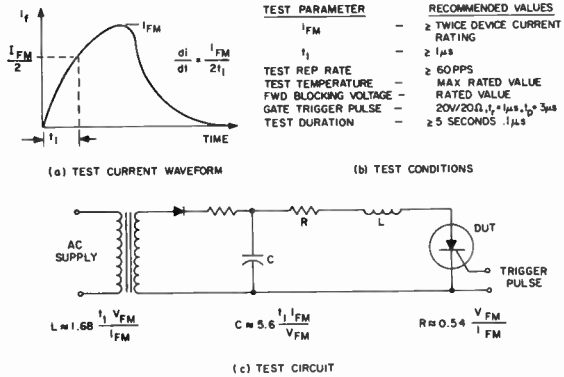
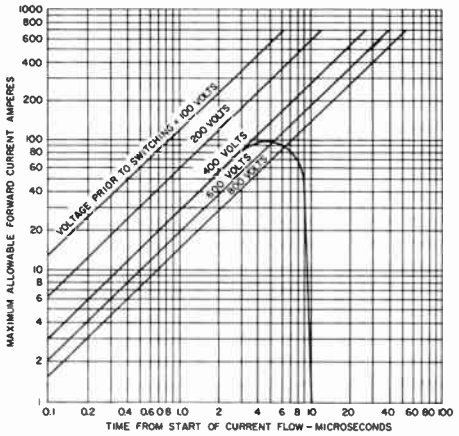


FIGURE 3.10 DI/DT TEST CIRCUIT

3.7.2 Turn-On Current Limit

A useful way to show the amount of anode current into which an SCR may switch in a given amount of time is in a presentation like that shown for the C35 type SCR in Figure 3.11. The curves, given for various forward blocking voltages from which the device is switched to the on-state, are valid up to 400 Hz.



NOTES
(1) INSTANTANEOUS VALUE OF ANODE CURRENT MUST NEVER EXCEED TURN-ON CURRENT LIMIT LINES SHOWN.
(2) DC TO 400 Hz
(3) CASE TEMPERATURE: -65°C TO +125°C
(4) GATE SUPPLY: 7 VOLTS OPEN CIRCUIT, 80 OHMS; RISE TIME = 4 MICROSECONDS (10% TO 90%)

FIGURE 3.11 TURN-ON CURRENT LIMIT

As an illustration in the use of these curves a half-sinusoidal current waveform of 10 microseconds pulse width switched from 400 volts is drawn on Figure 3.11. It shows that a sinusoidal current of 100 amps peak can be accommodated. If initial linear rate of rise of anode current is required for a specified period of time, values may be read directly from Figure 3.11. It must be borne in mind that specified gate drive as well as other test conditions must apply when using these curves.

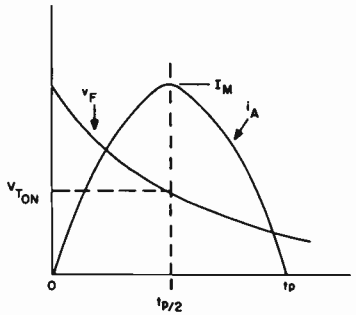


FIGURE 3.12 DEFINITION OF TURN-ON VOLTAGE

3.7.3 Turn-On Voltage

A convenient indirect relative measure of an SCR's di/dt performance is the value of its turn-on voltage characteristic at a given current and time and under specified test conditions. Figure 3.12 shows a frequently used sinusoidal anode test current waveform i_A and the simultaneous fall of SCR anode to cathode voltage v_F; turn-on voltage $V_{T_{ON}}$ is defined as the value of voltage at the time of peak current I_M. Common values used for current pulse width t_p are 10 microseconds, peak current 150 A, with typical values of $V_{T_{ON}}$ in the range of 3 to 30 volts.

The significance of $V_{T_{ON}}$ lies in the fact that it is a measure of the current density in the device at the time it is measured. A lower voltage drop indicates a greater amount of active device area turned on, and thus better turn-on switching, or di/dt, performance. Relative tests of this nature can be conducted in the test circuit shown in Figure 19.10.

3.8 HIGH FREQUENCY CURRENT RATINGS

As the frequency of switching is increased the contribution of the per cycle turn-on switching loss integrated over the period of one cycle of operation becomes an increasingly significant part of the total average power dissipation of the thyristor. In order to properly apply the device under this condition switching losses must be taken into account. Figure 3.13 shows

current ratings for the C140/C141 type SCR in a rating system designed especially for high frequency applications of SCR's. The figure shows peak allowable current versus pulse width for a half-sinusoidal current waveform (with variable duty cycles) over a repetition rate range of 10 to 25000 Hz at a constant case temperature and for a constant minimum circuit turn-off time and specified gate drive.

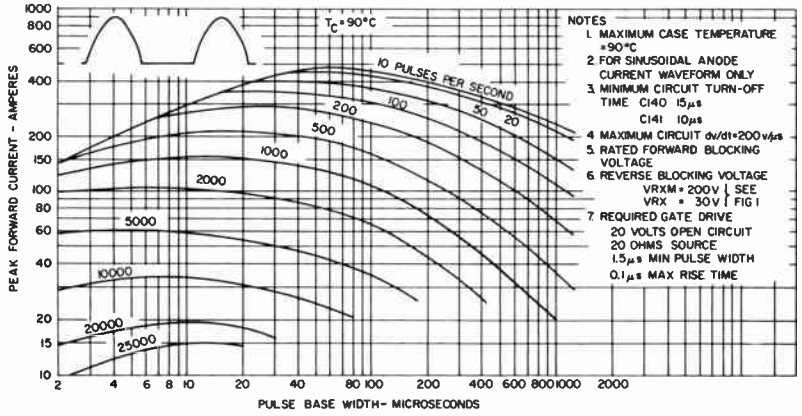


FIGURE 3.13 MAXIMUM ALLOWABLE PEAK FORWARD CURRENT vs. PULSE WIDTH (T_C = 90°C) FOR C140/C141 SCR.

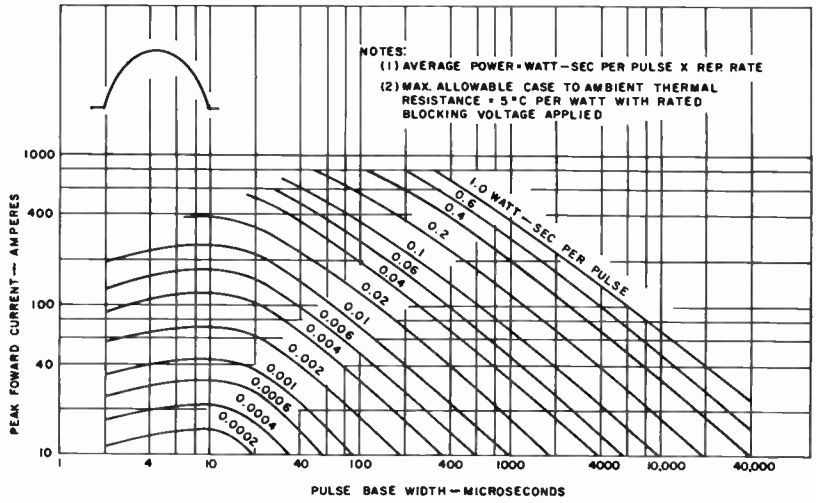


FIGURE 3.14 ENERGY PER PULSE FOR SINUSOIDAL PULSES FOR C140/C141 SCR.

Average power dissipation can be obtained from Figure 3.14. For a given peak current and pulse width a value of energy per pulse is read from the figure. This value, when multiplied by repetition rate, yields the average

power which must be dissipated by the heatsinking system. The specification sheets for high frequency SCR's like the C140 give more detail on the use of this rating system and show application examples.

3.9 SATURABLE REACTOR FOR INCREASING TURN-ON SWITCHING CAPABILITY

A saturable reactor in series with the SCR during its turn-on switching interval will greatly reduce switching dissipation in the SCR.[8] When the SCR is triggered on, the amount of current that will flow during the turn-on interval is limited to the magnetizing current of the reactor. The reactor is designed to go into magnetic saturation sometime after the SCR has been triggered. The delay time is employed to bring operation of the SCR within its turn-on current limit capability. Sufficient SCR active area is then available to assume full load current at minimum dissipation. Since the load current is delayed, the output of the SCR-reactor combination is delayed relative to the SCR trigger signal. Realistic pulse repetition rates are achievable by this technique, notably in many pulse modulator applications.

The delay time t of the saturable reactor is given by the time to saturate

$$t_s = \frac{NA\,\triangle B}{E} \quad \text{(seconds), where} \tag{3.3}$$

N = number of turns

A = cross sectional area of core in square centimeters

$\triangle B$ = total flux density change in Gauss

E = maximum circuit voltage being switched in volts

The current required at the time of saturable reactor switching I_s should be made small compared to the peak load current being switched. It is:

$$I_s = \frac{H_s\, l_m}{0.4\pi N}\,\text{(amperes)}, \text{ where} \tag{3.4}$$

H_s = magnetizing force required for core flux to reach saturation flux density B_s in Oersteds (1 Oersted = 2.021 ampere-turns/inch)

l_m = mean length of core in centimeters

N = number of turns

Provision must be made to properly reset the core before the next current pulse. Depending on the details of the circuit, reset may be accomplished by the resonant reversal of current (reverse recovery current) or by auxiliary means.

3.10 VOLTAGE RATINGS

The voltage ratings of SCR's are designated by the suffix letter in the

model number of the device (e.g., C35B) or by its JEDEC number. The designation is translated in the specifications and defines the continuous ratings and characteristics of thyristors peak voltage which the device will withstand in both the forward and reverse directions without breaking down. It is applicable to any junction temperature within the specified operating range. This symmetry of forward and reverse voltage ratings is characteristic of all standard SCR's today. The following discusses each voltage rating in more detail.

3.10.1 Reverse Voltage ($V_{ROM(rep)}$) and ($V_{ROM(non\text{-}rep)}$)

In the reverse direction (anode negative with respect to cathode), the SCR behaves like a conventional rectifier diode. General Electric assigns two types of reverse voltage ratings: repetitive peak reverse voltage with gate open, V_{ROM}(rep) (formerly designated by "repetitive PRV"); and non-repetitive peak reverse voltage with gate open, V_{ROM}(non-rep) (formerly designated by "non-repetitive PRV").

If these ratings are substantially exceeded, the device will go into breakdown and may destroy itself. Where transient reverse voltages are excessive, additional V_{ROM} margin may be built into the circuit by inserting a rectifier diode of equivalent current rating in series with the controlled rectifier to assist it in handling reverse voltage. For a detailed discussion on voltage transients, see Chapter 15; for series operation, see Chapter 6.

A specified minimum heatsink is required for a device to meet its maximum V_{ROM}(rep) rating. The reverse stability criterion of a semiconductor rectifier requires that the total junction-to-ambient thermal resistance be kept below a critical maximum value.[2] The size of the required minimum heatsink for dissipating the blocking losses is always very small (high thermal resistance) compared to the heatsink normally applied to the device in order to achieve its full current output rating.

3.10.2 Peak Forward Blocking Voltage (V_{FXM})

The peak forward blocking voltage V_{FXM} is given on the specification bulletin at maximum allowable junction temperature (worst case) with a specified gate bias condition. The larger SCR's are specified for a peak forward blocking voltage rating with the gate open, V_{FOM}; smaller SCR's are usually characterized for a peak forward blocking voltage with a specified gate-to-cathode bias resistor. The SCR will remain in the off-state if its peak forward voltage rating is not exceeded.

3.10.3 Peak Forward Voltage (PFV)

An SCR can be turned on in the absence of gate drive by exceeding its forward breakover voltage characteristic $V_{(BR)FX}$ at the prevailing temperature conditions. Although SCR's, in contrast to diode thyristors, are designed to be brought into conduction by means of driving the gate, breakover in the forward direction is generally not damaging provided the allowable di/dt under this condition is not exceeded.

Some SCR's are assigned a PFV rating. This rating is usually at or above the V_{FXM} rating. Forward voltage which causes the device to switch from a voltage in excess of its PFV rating may cause occasional degradation or eventual failure. Figure 3.15 illustrates the relationship between PFV and peak forward blocking voltage rating V_{FXM}.

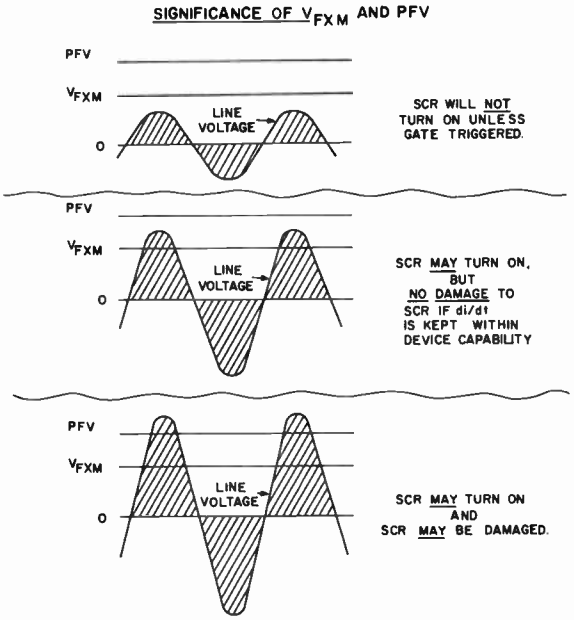


FIGURE 3.15 SIGNIFICANCE OF V_{FXM} AND PFV RATINGS

The PFV rating is often of practical importance when SCR's are tested for their actual breakover voltage characteristic $V_{(BR)FX}$ at room temperature; often a unit will have a $V_{(BR)FX}$ beyond its PFV rating at temperatures lower than maximum rated junction temperature. A proper test for $V_{(BR)FX}$ under these circumstances would be to conduct it at elevated temperature provided that $V_{(BR)FX}$ is lower than PFV.

In applications where the PFV rating of an SCR may be exceeded it is suggested that a network be connected anode to gate so that the device will trigger by gate drive rather than by forward breakover. A zener diode may be used to effect gate triggering at a predetermined level, or a Thyrector diode may be used to obtain a similar action.

3.11 RATE OF RISE OF FORWARD VOLTAGE (dv/dt)

A high rate of rise of forward (anode-to-cathode) voltage may cause an SCR to switch into the "on" or low impedance forward conducting state. In the interest of circuit reliability it is, therefore, of practical importance to characterize the device with respect to its dv/dt withstand capability.

General Electric SCR's are characterized with respect to dv/dt withstand capability in two contexts:

1. The so-called static dv/dt withstand capability. This specification covers the case of initially energizing the circuit or operating the device from an anode voltage source which has superposed fast rise-time transients. Such transients may arise from the operation of circuit switching devices or result from other SCR's operating in adjacent circuits. Interference and interaction phenomena of this type are discussed further in Chapter 16.
2. The maximum allowable rate of reapplication of forward blocking voltage, while the SCR is regaining its rated forward blocking voltage V_{FXM}, following the device's turn-off time t_{off} under stated circuit and temperature conditions. In this context dv/dt is an important part of the overall SCR turn-off time characterization. This type of dv/dt specification is covered in more detail in Chapter 5.

Figure 3.17 shows the typical static dv/dt withstand capability of the General Electric C38 type medium current SCR as a function of temperature with its gate open. The rate of rise of anode voltage shown on the ordinate is the slope of a straight line starting at zero anode voltage and extending through the one time constant (τ) point on an exponentially rising voltage. The upper right hand portion of Figure 3.17 illustrates this definition.

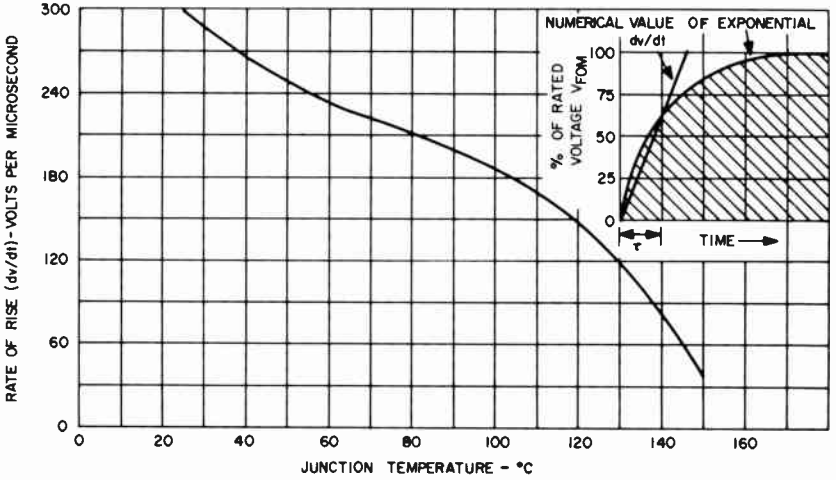


FIGURE 3.17 RATE OF RISE (dv/dt) OF FORWARD VOLTAGE THAT WILL NOT TURN ON C38 SCR.

The definition used in Figure 3.17 is the one that has come into standard industry usage. Some specification sheets give the time constant τ under specified conditions rather than a curve like Figure 3.17.

It will be noted that

$$\tau = \frac{0.632 \times \text{Rated SCR Voltage } (V_{FXM})}{dv/dt} \tag{3.5}$$

The initial dv/dt withstand capability will be recognized as being greater than the value defined in Figure 3.17. In terms of specified minimum time constant it is

$$\left.\frac{dv}{dt}\right|_{t=0+} = \frac{\text{Rated SCR Voltage } (V_{FXM})}{\tau} \tag{3.6}$$

In terms of specified maximum dv/dt capability, the allowable initial dv/dt withstand capability is

$$\left.\frac{dv}{dt}\right|_{t=0+} = \frac{1}{0.632}\, dv/dt = 1.58\, dv/dt \tag{3.7}$$

The shaded area shown in the insert of Figure 3.17 represents the area of dv/dt values that will not trigger the SCR. These data enable the circuit designer to tailor his circuitry in such a manner that reliable circuit operation is assured.

Since a high circuit-imposed dv/dt effectively reduces $V_{(BR)FX}$ (the actual anode voltage at which the particular device being observed switches into the on state) under given temperature conditions, a higher voltage classification unit will allow a higher rate of rise of forward voltage for a given peak circuit voltage. As an illustration of this, consider a C38B (V_{FOM} = 200 volts) at T_J = 130°C operating under a peak circuit voltage of E = 150 volts, or $\frac{150}{200} \times 100 = 75\%$ of rated voltage. Figure 3.17 shows that we may apply a dv/dt = 120 volts/microsecond to the one time constant (τ) point of an exponentially rising voltage. In our example, by Equation 3.5, $\tau_1 = \frac{.632 \times 200}{120} = 1.06$ microseconds. Accordingly, the time in which the anode of the C38B may reach 150 volts, or 75% of rated voltage, is, from Figure 3.17, $t_1 = 1.5\, \tau_1 = 1.5 \times 1.06 \approx 1.6$ microseconds.

Had we selected a C38D type (V_{FOM} = 400 volts) under the same conditions we find, using the ratio of rated voltages in Equation 3.5, that $\tau_2 = \tau_1 \frac{400}{200} = 2\tau_1 = 2 \times 1.06 = 2.12$ microseconds to reach 63.2% of 400 or 374 volts. Since, in our example, we need to reach only 150 volts, or $\frac{150}{400} = 38.6\%$ of the rated C38D V_{FOM}, we see from the insert of Figure 3.17, that $t_2 \approx 0.5\, \tau_2 = 0.5\,(2.12) = 1.06$ microseconds.

By selecting a 400 volt device the time to reach the operating circuit voltage can, in this example, be reduced to $\frac{t_2}{t_1} = \frac{1.06}{1.6}\,(100) \approx 67\%$.

Reverse biasing of the gate with respect to the cathode may increase dv/dt withstand capability beyond that shown in Figure 3.17. The reader is referred to Chapter 4 for further discussion.

The circuit shown in Figure 3.18 can be used to suppress excessive rate of rise of anode voltage. The time constant of the load resistance R_L in ohms and capacitor C in microfarads should be selected so that

$\tau \leq R_L\, C$ (microseconds), where (3.8)

τ = minimum time constant of exponential forward voltage rise specified for SCR.

SCR discharges C via R_d. R_d should be selected on the basis of limiting

the peak capacitor discharge current $\frac{E}{R_d}$ during the SCR turn-on interval to a value within the device's capability (see Section 3.7). For best results, the circuit of Figure 3.18 should be wired and placed in close proximity to the SCR in order to minimize inductive effects. Also, the capacitor should have good high frequency characteristics.

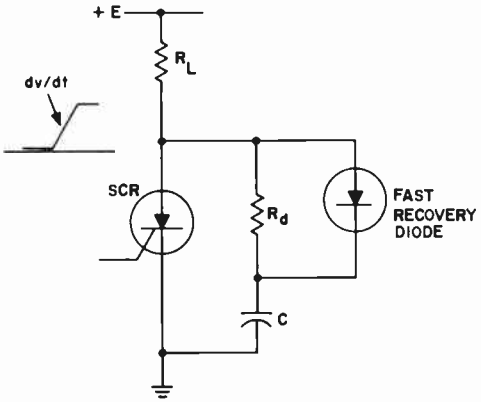


FIGURE 3.18 RATE OF RISE OF ANODE VOLTAGE (dv/dt) SUPPRESSION CIRCUIT

3.12 GATE CIRCUIT RATINGS

Maximum ratings for the gate circuit are discussed in Chapter 4.

3.13 HOLDING AND LATCHING CURRENT

Somewhat analogous to the solenoid of an electromechanical relay, an SCR requires a certain minimum anode current to maintain it in the "closed" or conducting state. If the anode current drops below this minimum level, designated as the holding current, the SCR reverts to the forward blocking or "open" state. The holding current for a typical SCR has a negative temperature coefficient; that is, as its junction temperature rises, its holding current requirement decreases.

A somewhat higher value of anode current than the holding current is required for the SCR to initially "pickup." If this higher value of anode latching current is not reached, the SCR will revert to the blocking state as soon as the gate signal is removed. After this initial pickup action, however, the anode current may be reduced to the holding current level. Where circuit inductance limits the rate of rise of anode current and thereby prevents the SCR from switching solidly into the conducting state, it may be necessary to make alterations in the circuit. This is discussed further in Chapter 4.

A meaningful test for the combined effects of holding and latching current is shown in Figure 3.19. The SCR under test is triggered by a specified gate signal. The test circuit allows the SCR to latch into conduction at a

current level I_{F1}. The test circuit then reduces the current to a continuously variable level I_{F2}. The current I_{F2} at which the SCR reverts to the off state is the desired value of holding current. See Section 19.5 for details of a suitable test circuit.

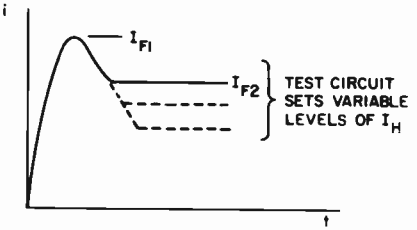


FIGURE 3.19 HOLOING CURRENT TEST WAVEFORM

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*Refer to Chapter 22 for availability and ordering information.

4 GATE TRIGGER CHARACTERISTICS, RATINGS, AND METHODS

The ability of the triode thyristor (SCR or triac) to switch from non-conducting to conducting state in response to a small control signal is the key factor in its widespread utility for control of power. Proper triggering of the thyristor requires that the source of the trigger signal should supply adequate gate current and voltage, without exceeding the thyristor gate ratings, in accordance with the characteristics of the thyristor and the nature of its load and supply. The trigger source impedance, time of occurrence and duration of the trigger signal, and off-state conditions are also important design factors. Since all applications of thyristors require some form of triggering, this chapter is devoted to the fundamentals of the gate triggering process, gate characteristics and ratings, interaction with the load circuit, characteristics of active trigger-circuit components, and basic examples of trigger circuits. Specific trigger circuits for performing various control functions are shown in subsequent chapters.

4.1 THE TRIGGERING PROCESS

In Chapter 1, Sections 1.4, 1.5, 1.6, and 1.10 describe the two-transistor analogy of the SCR, the junction gate and remote gate operation of the triac, and the remote-base transistor action of the SCR. From those discussions, it can be seen that the transition of a thyristor from the non-conducting to the conducting state is determined by internal transistor-like action.

The switching action, with slowly increasing DC gate current, is preceded by symmetrical transistor action in which anode current increases proportionally to gate current. As shown in Figure 4.1, with a positive anode voltage, the anode current is relatively independent of anode voltage up to a point where a form of avalanche multiplication causes the current to increase. At this point, the small-signal (or instantaneous) impedance (dv/dI) of the thyristor changes rapidly, but smoothly, from a high positive resistance to zero resistance, and thence to increasing values of negative resistance as increasing current is accompanied by decreasing voltage. The negative resistance region continues until saturation of the "transistors" is approached, wherein the impedance smoothly reverts from negative, to zero, to positive resistance.

The criteria for triggering depends upon the nature of the external anode circuit impedance and the supply voltage, as well as the gate current. This can be seen by constructing a load line on the curves of Figure 4.1, connecting between the open-circuit supply voltage, V_L, and the short-circuit

load current, I_A. With zero-gate current, the thyristor characteristic curve intersects the load line at a stable point (1). At a gate current of I_{G1}, the characteristic curve becomes tangential to the load line at a point (2) where the negative resistance of the thyristor is equal in magnitude to the external load resistance. Since this condition is unstable, the thyristor switches to the low-impedance state at stable operating point (3). The gate current may now be removed and conduction will be maintained at point (3). If the supply voltage is reduced to V_{L2} the load line will shift and the operating point (3) will move toward the origin. When the load line becomes tangential to the characteristic curve at point (4), the condition is again unstable, and the thyristor reverts back to the high-impedance "off state."

The anode current at point (4) is the "holding" current for this set of conditions. If, instead of reducing supply voltage to reach point (4), the load resistance were increased, the point (5) at which the characteristic curve becomes tangential to the load line occurs at a lower current, which is the holding current for that set of conditions. If the gate current I_{G1} were maintained while supply voltage was reduced to V_{L3}, turn-off would have occurred at point (6), at a lower anode current. A higher gate current, I_{G2} would then be required to trigger the SCR, but reduction of this gate signal below I_{G1} would allow it to switch off, hence the SCR would not have been truly latched in the on-state. The latching current is at least as high as the holding current (at $I_G = 0$), and is higher in some SCR's because of nonuniform areas of conduction at low currents. In those cases, the triggering criterion is not only meeting a negative-resistance intercept condition such as point (2), but also reaching a certain minimum anode current at point (3).

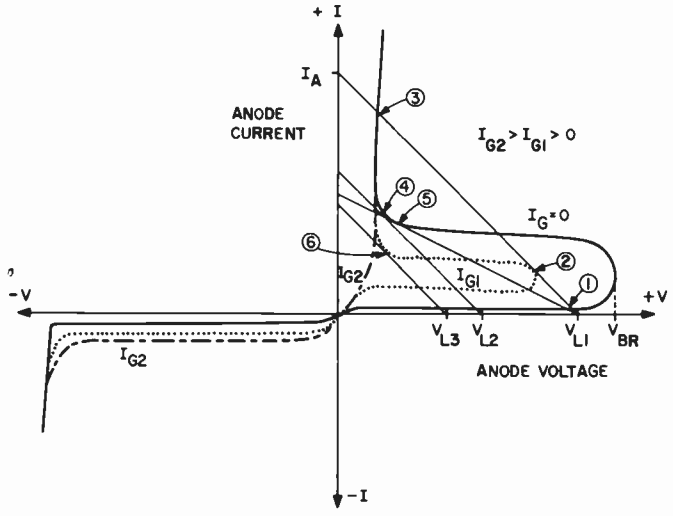


FIGURE 4.1 SCR ANODE-CATHODE CHARACTERISTICS WITH GATE CURRENT

Thyristor triggering requirements are dependent on both anode and gate conditions. Therefore, specifications on a given SCR's requirements for gate voltage and gate current to trigger (V_{GT} and I_{GT}) also define the anode circuit voltage and load resistance conditions.

4.2 SCR GATE-CATHODE CHARACTERISTICS

Trigger circuits must be designed to produce proper current flow between the gate and cathode terminals of the SCR. The nature of the impedance which these two terminals present to the trigger circuit is a determining factor in circuit design.

From basic construction and theory of operation, it can be seen that the electrical characteristics presented between the gate and cathode terminals are basically those of a p-n junction—a diode. This is not the whole story.

4.2.1 Characteristics Prior to Triggering

Figure 4.2 shows the low-frequency full and simplified equivalent circuits of the gate-to-cathode junction with no anode current flowing (open anode circuit). The series resistance R_L represents the lateral resistance of the p-type layer to which the gate terminal is connected. The shunt resistance R_S represents any intentional or inadvertent "emitter short" that may exist in the structure. The magnitudes of R_L and R_S are variables resulting both from structure design and manufacturing process. For example, R_S is extremely high in the C5 type SCR and quite low in the C180 type. The diodes are shown as avalanche ("zener") diodes because the reverse avalanche voltages of SCR gate junctions are typically in the range from 5 to 20 volts, a condition easily encountered in trigger circuits.

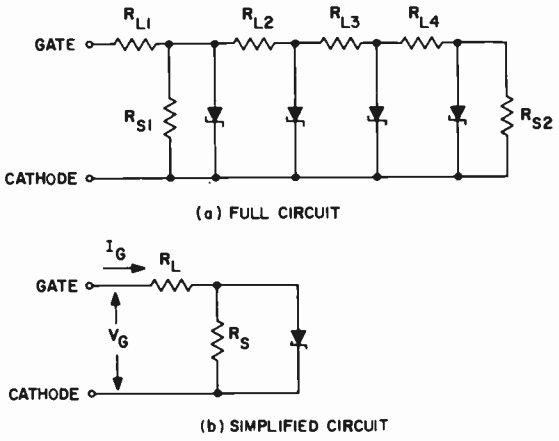


FIGURE 4.2 GATE-CATHODE EQUIVALENT CIRCUIT ($I_A = 0$)

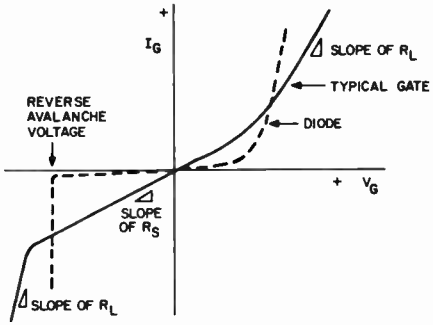


FIGURE 4.3 GATE-CATHODE CHARACTERISTIC CURVE ($I_A = 0$)

The difference between a typical gate characteristic and an ordinary diode junction is shown in Figure 4.3. The relative effects of R_L and R_S are apparent in different regions of the curve.

The equivalent circuit and characteristics shown here are valid only when anode current is zero or small as compared with gate current. This information is, therefore, useful for reverse gate bias, for very low forward gate current, and for examination of trigger circuits with anode disconnected.

4.2.2 Characteristics at Triggering Point

With the anode supply connected, the equivalent gate circuit must be modified, Figure 4.4, to include the anode current flow across the gate junction. Since anode current is a function of gate current (see Chapter 1), the total current through the junction and the voltage drop across the junction will increase more rapidly than with gate drive alone. As anode current increases (Figure 4.5), the small-signal impedance between the gate and cathode terminals changes smoothly from positive, to zero, to negative resistance. When the characteristic curve becomes tangential with the load line of the gate signal source impedance at point (1), the anode current becomes regenerative and the SCR can then trigger. For specification purposes, "I_{GT}" is the maximum gate supply current required to trigger, hence is measured at the peak of the curve.

Thus it is apparent that the impedance of the gate signal source is another factor in the criteria for thyristor triggering.

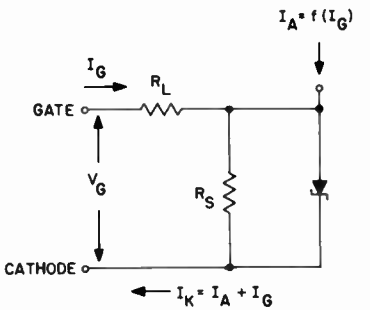


FIGURE 4.4 GATE-CATHODE EQUIVALENT CIRCUIT [$I_A = f(I_G)$]

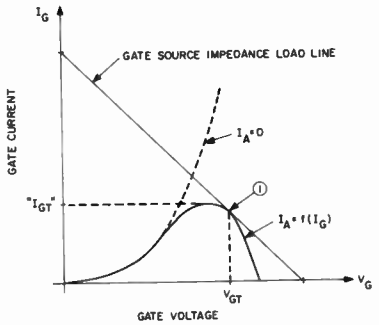


FIGURE 4.5 GATE CHARACTERISTICS, ANODE CONNECTED

4.2.3 Characteristics After Triggering

After the thyristor has been triggered and anode current flow across the gate-cathode junction is sufficient to maintain conduction, the gate impedance changes. It becomes a source, Figure 4.4, having a voltage equal to the gate-cathode junction drop (at the existing anode current) and an internal impedance R_L. This voltage is very nearly equal to the voltage drop between anode and cathode. The characteristics under this condition are shown in Figure 4.6. The curvature in the fourth quadrant is effectively the result of an increasing R_L as more current is taken out of the gate. This is the result of the distributed nature of the gate junction, as shown in Figure 4.2. As the gate-to-cathode terminal voltage is reduced by withdrawing current, the current flow through the lateral resistance of the p-type layer causes current to cease flowing through that portion of the p-n junction nearest the gate terminal. This causes an increase in current density in areas remote from the gate terminal. The higher current density and power dissipation in the lateral resistance can cause thermal damage to the thyristor.

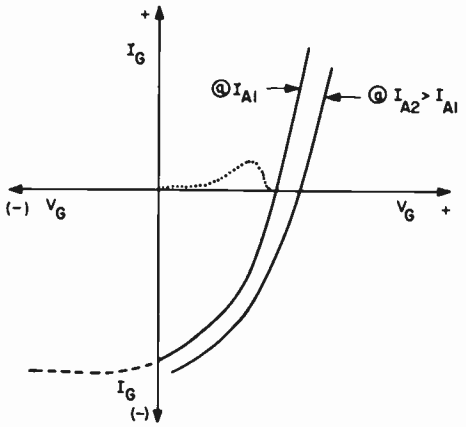


FIGURE 4.6 GATE CHARACTERISTICS AFTER TRIGGERING

If two SCR's are connected with gates and cathodes common, the gate voltage produced by conduction of one SCR can, in some cases, produce adequate triggering current in the gate of the other SCR. In many instances, this may be a desired effect—turning both SCR's on simultaneously. In other cases, however, as when the anode supply voltages of the two are 180 degrees out of phase, the existence of gate current in the reverse-biased SCR can cause triggering at the instant it becomes forward-biased because of stored charge in the p-type layer. It can also cause excessive reverse current by the remote-base transistor action.

4.3 EFFECTS OF GATE-CATHODE IMPEDANCE AND BIAS

The preceding sections have shown that the criteria for triggering involves the gate current, gate signal source impedance, and anode supply (load) impedance. The interaction between gate and anode circuits demands examination in some depth.

4.3.1 Gate-Cathode Resistance

The two-transistor analogy shows that a low external resistance between gate and cathode bypasses some current around the gate junction, thus requiring a higher anode current to initiate and maintain conduction. Low-current, high sensitivity SCR's are triggered by such a low current through the gate junction that a specified external gate-cathode resistance is required in order to prevent triggering by thermally generated leakage current. This resistance also bypasses some of the internal anode current caused by rapid rate-of-change of anode voltage (dv/dt, see Chapter 3). It raises the forward breakover voltage by reducing the efficiency of the n-p-n "transistor" region, thus requiring a somewhat higher avalanche multiplication effect to initiate triggering. The latching and holding anode currents are also affected by the current which bypasses the gate junction.

The relative effect of the external resistance is dependent upon the magnitudes of the internal resistances, R_L and R_S of Figure 4.2. For low-current thyristors, the type of construction used generally leads to high values of R_S (virtually no emitter shorting) and low values of R_L because of the small pellet size. Figure 4.7 shows the effect of external gate-to-cathode resistance upon holding current for the type C106 low-current SCR. The spread between maximum and minimum values represents production variations of the internal resistances and variations in current-gain of the equivalent "transistor" regions.

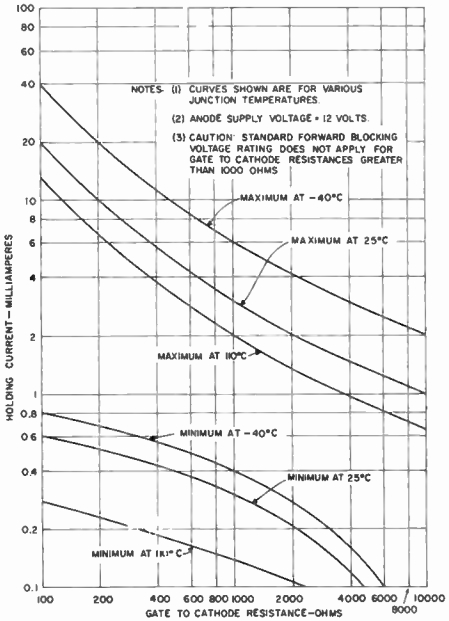


FIGURE 4.7 MAXIMUM AND MINIMUM HOLDING CURRENT VARIATION WITH EXTERNAL GATE-TO-CATHODE RESISTANCE FOR C106 SCR.

External shunt gate resistance also reduces the turn-off time of the SCR by assisting in recovering stored charge, by raising the anode holding current, and by requiring higher anode current to initiate re-triggering.

4.3.2 Gate-Cathode Capacitance

A low shunt capacitive reactance at high frequencies can reduce the sensitivity of a thyristor to dv/dt of anode voltage (see Chapter 3), in much the same manner as a resistor, while maintaining higher sensitivity to DC and low frequency gate signals. This integrating effect is particularly useful where high-frequency "noise" is present in either the anode or gate circuits.

At the point of triggering, however, the gate voltage (see Figure 4.5) must increase as anode current increases. Therefore, a capacitor connected between gate and cathode will tend to retard the triggering process, yielding longer delay-time and rise-time of anode current. This action can be detrimental when a high di/dt of anode current is required (see Chapters 3 and 11).

After the SCR has been turned on, the gate acts as a voltage source, charging the capacitor to the voltage drop across the gate junction. Since this voltage (depending on value of anode current) is generally higher than the gate voltage required to trigger the SCR (V_{GT}), the energy stored in the capacitor can supply triggering current for a period of time after removal of anode current, thereby possibly causing the SCR to fail to commutate. In low-current SCR's, a capacitor on the order of 10 microfarads can maintain gate current for over 8.3 milliseconds, hence can prevent commutation in a half-wave, 60 Hertz circuit.

If the gate triggering signal is a low-impedance pulse generator in series with a capacitor, the capacitor can be charged by gate current during the pulse and the polarity will be such that at the end of the pulse the SCR gate will be driven negative. For low values of anode current at this instant, the negative drive may raise the holding current requirement above the anode current and turn off the SCR.

4.3.3 Gate-Cathode Inductance

Inductive reactance between gate and cathode reduces sensitivity to slowly changing anode current or gate source current while maintaining sensitivity to rapid changes. This differentiating effect is useful in improving thermal stability since changes in thermal leakage current are slow. When used with the light-activated SCR, it provides sensitivity to a flash of light with insensitivity to steady-state ambient light (see Chapter 13).

With anode current flowing, the gate voltage causes current to flow out of the gate, through the inductance. The rate at which this current builds up after triggering is a function of the L/R ratio of the inductance to both internal and external resistance. As this negative gate current rises, the holding current of the thyristor also rises. If anode current is low, or increasing more slowly than negative gate current, the thyristor may drop out of conduction.

After the SCR anode current ceases, negative gate current will continue for a period of time, decaying according to the L/R time-constant. This negative gate current during the turn-off condition can reduce turn-off time (by nearly 10:1 in small SCR's) and can permit a faster rate of re-applied forward voltage (higher dv/dt).

If a triggering current pulse is applied in parallel with an inductor and the gate, the pulse can produce a current flow through the inductor. At the termination of the pulse, the inductor current will continue to flow as a negative gate current, thereby raising holding current and possibly causing turn-off of the SCR.

4.3.4. Gate-Cathode LC Resonant Circuit

A parallel LC resonant circuit connected between gate and cathode can provide a frequency-selective response, and can also produce a condition of oscillation.

The oscillating condition is obtained by making the anode current value intermediate between the normal ($I_G = 0$) holding current and the holding current with maximum negative gate current flowing through the inductor. As explained in Section 4.3.3, the SCR can be turned on, then negative gate current will increase until the SCR turns off. After turn-off, inductor current will charge the capacitor to a negative voltage, then the capacitor will discharge into the inductor in a resonant manner. When the capacitor voltage swings positive again, it can re-trigger the SCR and the process will repeat indefinitely. Damping is required to avoid such oscillation.

4.3.5 Positive Gate Bias

The presence of positive current in the gate when reverse voltage is applied to the anode increases reverse blocking (leakage) current through the device substantially. As a result, the SCR must dissipate additional power. It is, therefore, necessary either to make provision for this additional loss or to take steps to limit it to a negligible value.

Figure 4.8 gives the temperature derating for different SCR lines at various gate drive duty cycles (per cent of full cycle or 360 electrical degrees) for values of peak positive gate voltage. For proper application, this loss must be included in the total device dissipation. The temperature derating, ΔT, found from Figure 4.8, must be subtracted from the maximum allowable stud temperature (found from the device rating curve) for the proper cell type and conduction angle. For lead mounted devices, subtract from the ambient temperature curve. Derating becomes negligible if the gate voltage is less than 0.25 volt or the temperature derating turns out to be 1°C or less.

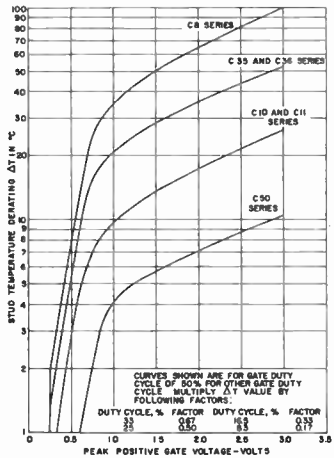


FIGURE 4.8 TEMPERATURE DERATING CURVE FOR SIMULTANEOUS APPLICATION OF POSITIVE GATE PULSE WHEN ANODE IS NEGATIVE.

A means of limiting the additional reverse dissipation to a negligible value is given by a gate clamping circuit of the type shown in Figure 4.9 for low and medium current SCR's (C10 and C35 series). Resistor R_A and a diode are connected from gate to anode to attenuate positive gate signals whenever the anode is negative. For a given peak value of open circuit gate source voltage, Figure 4.9 gives the maximum ratio of the value of R_A to R_G that will safely clamp the gate for all values of reverse voltage within the reverse voltage rating of the SCR.

An alternate way to limit additional reverse leakage dissipation due to positive gate voltage is to insert in series with the SCR a rectifier diode that has a lower reverse blocking current. In this manner the diode will assume the greater share of the reverse voltage applied to the series string, significantly reducing reverse dissipation in the SCR.

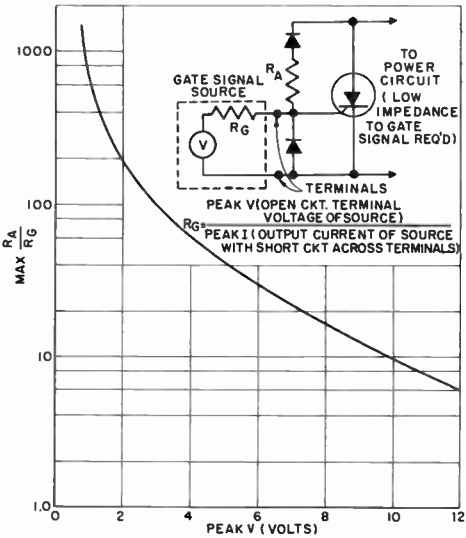


FIGURE 4.9 GATE CLAMP CIRCUIT FOR CONTROLLED RECTIFIER

4.3.6 Negative Gate Bias

The gate should never be allowed to become more negative with respect to the cathode than is indicated on the specification bulletin. For example, the gate of the C35 (2N681) type has a rated peak reverse voltage of 5 volts. If there is a possibility that the gate will swing more negative than the rated value, a diode should be connected either in series with the gate, or from cathode to gate to limit the reverse gate voltage. A considerable negative gate current (conventional current flow out of the gate) can be caused to flow if the cathode circuit between cathode and gate is opened for any reason while the SCR is conducting forward load current (conventional current flow from anode to cathode). This current would initially be limited only by the impedance of the gate circuit and could cause the allowable gate dissipation to be exceeded, thus leading to possible failure of the SCR.

Negative gate bias, when the anode is positive, tends to increase the forward breakover voltage $V_{(BR)FX}$ (Section 3.8.3) and the dv/dt withstand capability (Section 3.9) of the SCR for a given junction temperature.

The effect of negative gate bias on $V_{(BR)FX}$ is greatest for the smaller junction area devices. For example, the C5 types (2N1595, etc.) have $V_{(BR)FR}$ specified for a certain value of gate-to-cathode resistance (R_{GC} = 1000 ohms) and at a specified junction temperature. For more detail on the effect of negative gate bias on small SCR's the reader is referred to Reference 1.

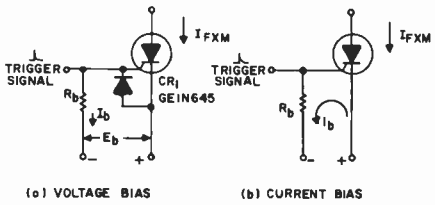


FIGURE 4.10 NEGATIVE GATE BIAS ARRANGEMENTS

Figure 4.10(a) shows a voltage bias arrangement. Resistor R_b is taken to a negative supply instead of being merely returned to the cathode. The voltage source E_b establishes a current $I_b \cong \frac{E_b - D}{R}$, where D is the voltage drop across diode CR1 (typical value 0.7 volt). The diode provides a fixed negative bias voltage gate-to-cathode for the SCR. The disadvantage of this approach, however, is the loss of input sensitivity due to resistor R_b.

Figure 4.10(b) shows a current bias scheme useful for smaller junction diameter SCR's. Resistor R and the bias source are selected so that a bias current $I_b \cong I_{FXM}$ is established through resistor R in the direction indicated; I_{FXM} is the maximum forward blocking (leakage) current of the SCR under the prevailing junction temperature and anode voltage. Selection of I_b in this manner yields a "worst case" design on the assumption that most, if not all, of I_{FXM} will be diverted from the SCR emitter (gate-cathode junction). This approach is limited to SCR's which have sufficient reverse gate power ratings to handle reverse current I_b at its associated reverse gate voltage. The scheme of Figure 4.10(b) is suitable, for example, for General Electric C5 type SCR's which allow operation of the gate-to-cathode junction in reverse avalanche.

With increasing area of the semiconductor junctions in the SCR, however, negative gate bias has less effect. Unless $V_{(BR)FR}$ (with bias resistor) is specified, conservative circuit design practice should not depend on increasing $V_{(BR)FX}$ by negative gate biasing.

The improvement in dv/dt withstand capability that can be achieved by negative gate biasing is shown in Figure 4.11 for a typical C35 type SCR. It shows the effect of gate bias on the allowable time constant of application of forward blocking voltage without having the SCR switch on. The zero gate voltage curve corresponds to the time constant values given on the C35 specification sheet for the open gate condition. Figure 4.11 extends the usefulness of this information for different values of gate bias.

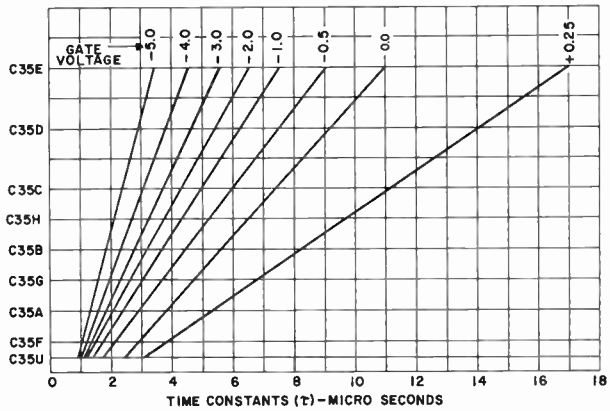


FIGURE 4.11 EFFECT OF GATE BIAS ON ALLOWABLE TIME CONSTANT OF APPLICATION OF FORWARD BLOCKING VOLTAGE.

4.4 EFFECTS OF ANODE CIRCUIT UPON GATE CIRCUIT

In Section 4.1 it was shown that the anode circuit voltage and impedance were determining factors in triggering. The effect of anode current was discussed in Section 4.2.3. Two other effects are worth noting. Junction capacitance in the SCR can couple high-frequency signals from the anode to the gate circuit which, although they may not cause triggering in themselves, may interfere with normal operation of the trigger circuit.

When the anode voltage of the SCR reaches either the forward breakover or reverse avalanche voltage, a voltage will appear at the gate terminal. In the case of forward breakover voltage, a forward anode current starts flowing which produces a positive gate voltage, as in normal conduction (see Section 4.2.3). When the reverse avalanche voltage is reached, the gate junction becomes reverse biased. Depending on the magnitude of R_S (Figure 4.2) the negative voltage appearing at the gate terminal may rise to the avalanche voltage of the gate junction. If a reverse voltage transient on the anode exceeds reverse avalanche, the reverse-blocking junction of the SCR no longer blocks, thereby applying the transient energy to the gate junction in reverse. The gate junction and any external circuit connected to the gate may then receive excessive voltage and current from this process.

When the SCR is conducting, its gate is essentially at the same potential as its anode. When the SCR is non-conducting, the gate potential is not related to anode potential within the normal operating range. However, during the commutating transition from conduction to non-conduction, the gate goes through an intermediate phase which can result in a large negative voltage appearing at the gate terminal. If an SCR is commutated, as in a DC chopper or flip-flop circuit, by the step application of a reverse bias, the gate voltage will initially be the normal forward gate-cathode junction drop until that junction recovers, whereupon both anode and the gate will go negative. The gate voltage will then follow anode voltage until the main reverse-blocking (p-n) junction recovers, at which time the gate reverts to its normal charac-

teristics. These transitions are readily observed on small SCR's in particular. On larger SCR's, the effects are somewhat masked by lower values of internal shunt resistance R_S. The negative transient at the gate can cause malfunction or damage in the external gate circuit.

4.5 DC GATE TRIGGERING SPECIFICATIONS

The DC gate trigger characteristics of an SCR are presented in the form of a graph similar to Figure 4.12 which applies to the C35 (2N681) type SCR. The graph shows gate-to-cathode voltage as a function of positive gate current (flow from gate to cathode) between limit lines (A) and (B) for all SCR's of the type indicated. These data apply to a zero-anode-current condi tion (anode open).

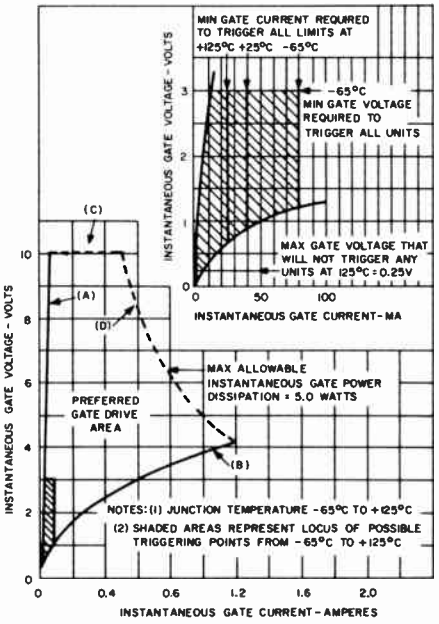


FIGURE 4.12 DC GATE TRIGGERING CHARACTERISTICS (FOR C35 TYPE SCR)

The basic function of the trigger circuit is to simultaneously supply the gate current to trigger I_{GT} and its associated gate voltage to trigger V_{GT}. The shaded area shown in Figure 4.12 contains all the possible trigger points (I_{GT}, V_{GT}) of all SCR's conforming to this specification. The trigger circuit must, therefore, provide a signal (I_{GT}, V_{GT}) *outside* of the shaded area in order to reliably trigger all SCR's of that specification.

The area of trigger circuit—SCR gate operation is indicated as the "preferred gate drive area." It is bounded by the shaded area in Figure 4.12 which represents the locus of all specified triggering points (I_{GT}, V_{GT}), the limit lines (A) and (B), line (C) representing rated peak allowable forward gate voltage V_{GF}, and line (D) representing rated peak power dissipation P_{GM}. Some SCR's may also have a rated peak gate current I_{GFM} which would appear as a vertical line joining curves (B) and (D).

The insert in the upper right hand portion of Figure 4.12 shows the detail of the locus of all specified trigger points, and the temperature dependence of the minimum gate current to trigger $I_{GT_{min}}$. The lower the junction temperature, the more gate drive is required for triggering. (Some specifications may also show the effect of forward anode voltage on trigger sensitivity.

Increased anode voltage, particularly with small SCR's, tends to reduce the gate drive requirement.) Also shown is the small positive value of gate voltage below which no SCR of the particular type will trigger.

The reverse quadrant of the gate characteristic is usually specified in terms of maximum voltage and power ratings. The application of reverse bias voltage and the extraction of reverse gate current for increased SCR off-state stability was discussed in Section 4.3.6.

4.6 LOAD LINES

The trigger circuit load line must intersect the individual SCR gate characteristic in the region indicated as "preferred gate drive area" in Figure 4.12. The intersection, or maximum operating point, should furthermore be located as close to the maximum applicable (peak, average, etc.) gate power dissipation curve as possible. Gate current rise times should be in the order of several amperes per microsecond in the interest of minimizing anode turn-on time particularly when switching into high currents. This in turn results in minimum turn-on anode switching dissipation and minimum jitter.

Construction of a "load line" is a convenient means of placing the maximum operating point of the trigger circuit-SCR gate combination into the preferred triggering area. Figure 4.13(a) illustrates a basic trigger circuit of source voltage e_s and internal resistance R_G driving an SCR gate. Figure 4.13(b) shows the placement of the maximum operating point well into the "preferred trigger" area close to the rated dissipation curve. The load line is constructed by connecting a straight line between the trigger circuit open circuit voltage E_{oc}, entered on the ordinate, and the trigger circuit short circuit current $I_{sc} = \frac{E_{oc}}{R_G}$ entered on the absissa.

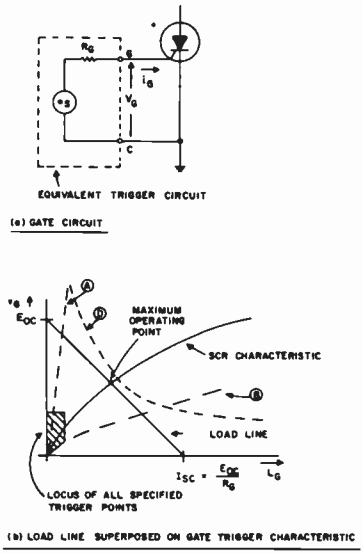


FIGURE 4.13 GATE CIRCUIT AND CONSTRUCTION OF LOAD LINE

If the trigger circuit source voltage is a function of time e_s (t), the load line sweeps across the graph, starting as a point at the origin and reaching its maximum position, the load line, at the peak trigger circuit output voltage.

The applicable gate power curve is selected on the basis of whether average or peak allowable gate power dissipation is limiting. For example, if a DC trigger is used, the average maximum allowable gate dissipation (0.5 watt for C35) must not be exceeded. If a trigger pulse is used the peak gate power curve is applicable (for the C35, the 5 watt peak power curve labelled

D in Figure 4.12). For intermediate gate trigger waveforms the limiting allowable gate power dissipation curve is determined by the duty cycle of the trigger signal according to: peak gate drive power × pulse width × pulse repetition rate ≦ allowable average gate power.

4.7 POSITIVE GATE VOLTAGE THAT WILL NOT TRIGGER SCR

Figure 4.12 also indicates the maximum gate voltage that will not trigger the SCR. For example, for the C35 (2N681) type, Figure 4.12 shows that at 125°C junction temperature this value is 0.25 volt. This limit is important when designing a trigger circuit which has a standby leakage current when no trigger signal is present. Examples of this are saturable reactors and directly coupled unijunction transistor trigger circuits. To prevent false triggering under these circumstances, a resistor should be connected across the output of the trigger circuit. Its value of resistance in ohms should not exceed the maximum gate voltage that will not trigger divided by the maximum trigger circuit standby current.

4.8 PULSE TRIGGERING

Thyristors are commonly specified in terms of the continuous DC gate voltage and current required to trigger. For trigger pulse widths down to 100 microseconds, the DC data apply. For shorter pulse widths, V_{GT} and I_{GT} increase.

On a short-time basis, thyristors may be generally considered to be charge controlled, as are transistors. The free charge stored within the gate p-type layer of an SCR may be considered to be the difference between the incoming charge flow rate ($dq/dt = I_G$) and the internal recombination rate. Under DC conditions and for a given recombination rate, the free charge is directly a function of gate current. When the free charge reaches a certain level, the device triggers. To get the required charge into the gate in a time that is short compared with the recombination time requires higher current (hence higher voltage) than for DC triggering.

Figure 4.14(a) shows the relationship between pulse width and peak current for a rectangular pulse to trigger the C-106 type SCR. Note that the current curves approach a constant-charge slope at the smaller pulse widths. The point at which the pulse current curve departs from the DC current level is about 200 microseconds for this small thyristor. Other SCR types, with shorter recombination times, can be triggered with pulse current equal to the DC level down to about 20 microseconds.

It should not be inferred from Figure 4.14(a) that only rectangular pulses are acceptable. Any unidirectional waveshape which does not exceed gate current, voltage, and power ratings may be used if the total charge is adequate. Proper charge criteria may be determined by plotting, as in Figure 4.14(b), the integral of the actual current wave and the integral of the rectangular pulse current. If the two curves cross, the triggering charge is adequate.

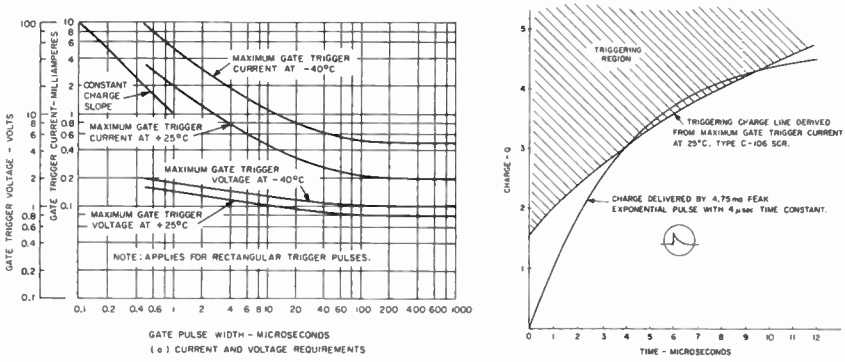


FIGURE 4.14 EFFECT OF TRIGGER PULSE WIDTH (C-106 SCR)

Figure 4.15 shows the increase in gate drive required for triggering five types of SCR's with trigger signals of short pulse duration. In order for the SCR to trigger, the anode current must be allowed to build up rapidly enough so that the latching current of the SCR is reached before the pulse is terminated. (Latching current may be assumed to be three times the value of the holding current given on the specification sheet.) For highly inductive anode circuits it is, therefore, advisable to use a maintained type of trigger signal which assures gate drive until latching current has been attained. Also, in certain rectifier and inverter circuits that require re-triggering, a square wave type of trigger circuit might be considered.

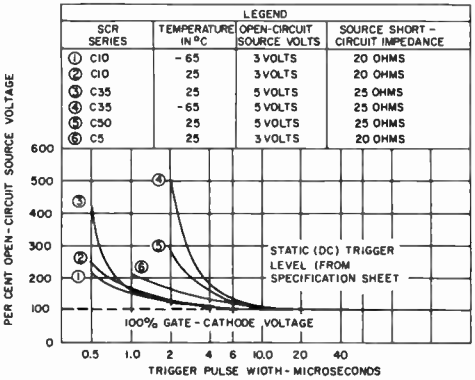


FIGURE 4.15 GATE DRIVE REQUIRED FOR SHORT TRIGGER PULSE DURATION

The DC gate trigger characteristics are measured on a 100% basis in production for all SCR's, but the pulse trigger characteristics are measured only on a sampling basis. For applications where the pulse trigger characteristics are critical, a special specification should be requested so that satisfactory pulse triggering will be assured.

4.9 TRIGGERING SCR WITH A NEGATIVE PULSE

Some applications may make it desirable to trigger an SCR with a negative pulse rather than with one of the conventional positive polarity. In low power level SCR circuits a diode connected in series with the SCR allows negative triggering conveniently and economically. Figure 4.16 shows this arrangement for a C5 type SCR.

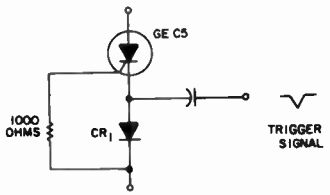


FIGURE 4.16 NEGATIVE PULSE TRIGGERING

4.10 ANODE TURN-ON INTERVAL CHARACTERISTICS

Figure 4.17 shows the turn-on, or switching, characteristics of a typical C10 type SCR. It is representative of other SCR types as well. Per cent anode voltage is shown as a function of time, following application of the trigger signal at zero time, for switching from 500 volts and from 100 volts for two different circuit current levels.

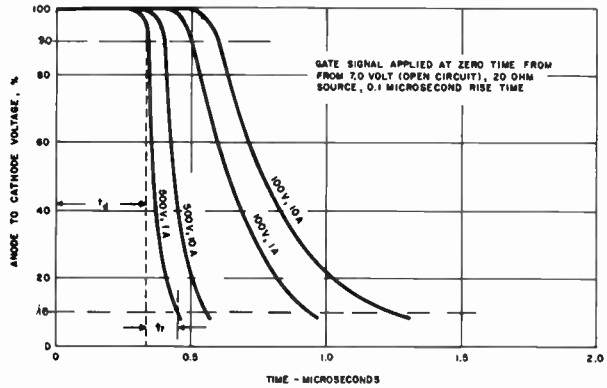


FIGURE 4.17 TYPICAL TURN-ON CHARACTERISTICS OF C10 TYPE SCR

Delay time t_d is shown for the 500 volt/1 ampere switching characteristic. It is defined as the time between the 10% point of the leading edge of the gate current pulse and the 10% point of the anode voltage waveform. The delay time decreases as the amplitude of the gate current pulse is increased, but approaches a minimum value of 0.2 to 0.5 μsec for gate current pulses of 500 ma or more.

Rise time t_r is defined as the time required for the anode voltage to drop from 90% of its initial value to 10%, as indicated for the 500 volt/1 ampere curve in Figure 4.17. The rise of current as the voltage across the SCR falls is determined largely by the circuit. In a purely resistive circuit the current will rise in the same manner as the voltage falls; hence the term rise time. It is important that the instantaneous voltage-current product during the turn-on interval not exceed the dissipation capability of the SCR. For this reason, the rate of rise of anode current (di/dt) must be limited (see Chapter 3). Rise time, as well as delay time, tends to be reduced by a large gate drive within the allowable gate dissipation ratings of the SCR. Therefore, in order to minimize turn-on switching dissipation, the gate should be driven in the area of "preferred triggering" close to the allowable gate power dissipation curve shown in Figure 4.12.

Total turn-on time is defined as $t_{on} = t_d + t_r$. It is important to note that large turn-on switching dissipation can still occur after the termination of the turn-on time as defined above. Particularly, when switching from a high voltage into a large current, applicable switching ratings such as discussed in Chapter 3 should be consulted.

The jitter, or variation of switching time from one cycle to the next, is usually less than 2 mμsec at constant temperature if the gate is driven at two to three times the minimum amplitude required for triggering.

4.11 SIMPLE RESISTOR AND RC TRIGGER CIRCUITS

It is sometimes required to find the simplest and most economical means for triggering an SCR when some performance compromise can be made, particularly with regard to repeatibility over a temperature range. The reader is referred to Reference 2 for a more detailed treatment of simple and low cost SCR trigger circuits.

Figure 4.18 shows a simple method of obtaining gate current for triggering the SCR from the main AC supply whenever the anode is positive with respect to the cathode. As soon as the SCR has triggered, the anode voltage drops to the conduction value and the gate current decreases to zero. Resistor R limits the peak gate current. The diode in the gate circuit is provided to prevent reverse voltage from being applied between cathode and gate during the reverse part of the cycle. If desired, the diode can be connected between gate and cathode rather than in series with R. Conduction is initiated by closing contact S_1 in Figure 4.18(a) or by opening contact S_2 in Figure 4.18(b). Interruption of load current occurs within one-half cycle after opening S_1 or closing S_2 due to line voltage reversal. For more complete static switching circuits, see Chapter 8.

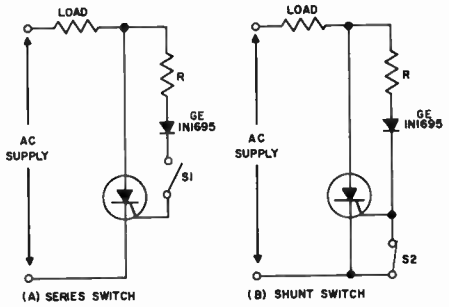


FIGURE 4.18 HALF-WAVE STATIC SWITCH

Simple resistor-capacitor-diode combinations will trigger and control SCR's over the full 180 electrical degree range, giving very good performance at commercial temperatures. Since in a scheme of this type a resistor will have to supply all of the gate drive required to turn on the SCR, these types of circuits operate most satisfactorily with SCR's having fairly good gate sensitivities. The less sensitive the gate, the lower the resistance must be, and the greater power rating.

A very simple variable resistance half-wave circuit is shown in Figure 4.19. It provides phase retard from essentially zero (full on) to 90 electrical degrees of the anode voltage wave. Diode CR1 blocks reverse gate voltage on the negative half cycle of anode supply voltage. It must be rated to block at least the peak value of the AC supply voltage. The retard angle cannot be extended beyond the 90 degree point because the trigger circuit supply voltage and the trigger voltage producing the gate current to fire, I_{GF}, are in phase. When $e_{ac} = E_m$, at the peak of the AC supply voltage, the SCR can still be triggered with the maximum value of resistance between anode and gate. Since the SCR will trigger and latch into conduction the first time I_{GT} is reached, its conduction cannot be delayed beyond 90 electrical degrees with this circuit. This circuit, therefore, provides continuously variable control from the SCR full "on" (100% half-wave output) to the SCR half "on" (50% half-wave output).

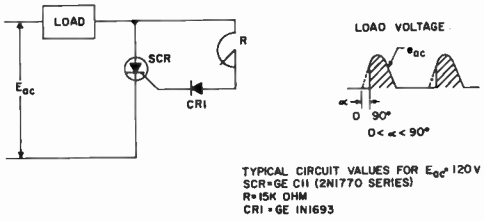


FIGURE 4.19 SIMPLE HALF-WAVE VARIABLE RESISTOR PHASE CONTROL (LIMITED RANGE OF CONTROL)

Figure 4.20 shows an R-C-Diode circuit giving full half-cycle control (180 electrical degrees). On the positive half-cycle of SCR anode voltage the capacitor will charge to the trigger point of the SCR in a time determined by the RC time constant and the rising anode voltage. On the negative half-cycle, the top plate of the capacitor charges to the peak of the negative voltage cycle through diode CR2, thus resetting it for the next charging cycle.

Since triggering current must be supplied by the line voltage through the resistor, the capacitor must be selected such that its charging current is high compared with I_{GT}, at the instant of the latest desired firing angle. Conversely, select the maximum value of R to produce I_{GT} at the latest desired firing angle, using the line voltage less IR drop in the load at that point, then select C to produce V_{GT} at that point in time.

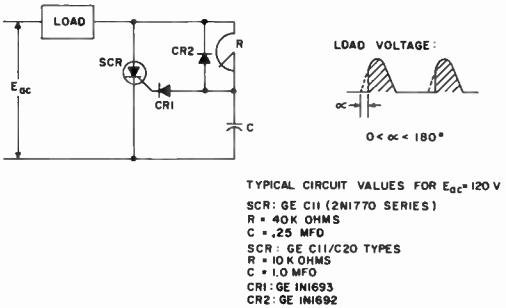


FIGURE 4.20 SIMPLE HALF-WAVE RC-DIODE PHASE CONTROL (FULL 180° CONTROL RANGE)

Figure 4.21 illustrates a slave circuit arrangement in which an independent half-wave circuit (SCR_2) is triggered on one half-cycle at a predetermined phase angle. On the following half-cycle the slave circuit will trigger SCR_1 at the same phase angle relative to that half-cycle. When SCR_2 does not trigger, capacitor C will charge and discharge to the same voltage at the same time constant. The voltage across C will not be sufficient to trigger SCR_1. As SCR_2 is triggered, capacitor C on discharging sees a time integral of line voltage that is different from the one on charging by the time integral of voltage appearing across the load. This action resets the capacitor to a voltage level related to the trigger delay angle of SCR_2. On the next half-cycle, when the anode of SCR_1 swings positive, it will trigger at the end of this delay angle.

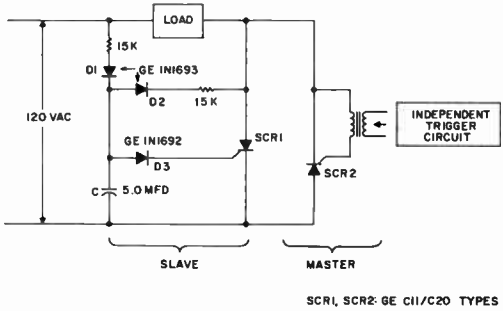


FIGURE 4.21 THREE TERMINAL, FULL WAVE, RC-DIODE SLAVING CIRCUIT FOR FULL-WAVE PHASE CONTROL.

4.12 AC THYRATRON-TYPE PHASE SHIFT TRIGGER CIRCUITS

Figure 4.22 illustrates a full-wave phase controlled rectifier employing an R-C or R-L phase shift network to delay the gate signal with respect to the anode voltage on the SCR's. Many variations of this type of phase shift circuit have been worked out for thyratrons.

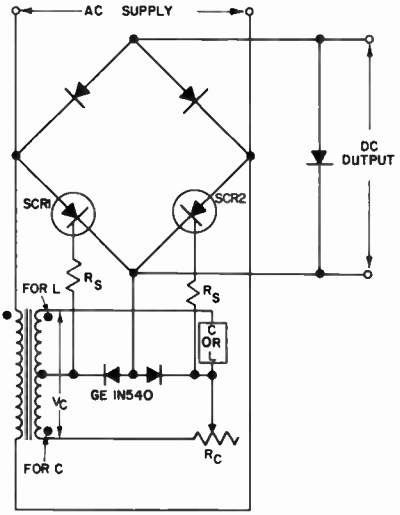


FIGURE 4.22 R-C OR R-L PHASE SHIFT NETWORK CONTROL OF SINGLE PHASE BRIDGE OUTPUT.

When using SCR's (C8, C10, C11, C35, C36, and C50 series), the following criteria should be observed to provide the maximum range of phase shift and positive triggering over the particular SCR's temperature range without exceeding the gate voltage and current limitations:

A. The peak value of V_c should be greater than 25 volts.

B. $\frac{1}{2\pi fC}$ or $2\pi fL \leqq \frac{V_c}{2} - 9$

where C = capacitance in farads
L = inductance in henries
V_c = peak end-to-end secondary voltage of control transformer
f = frequency of power system

C. $R_s = \frac{V_c - 20}{0.2}$

where R_s = series resistance in ohms

D. $R_c \geqq \frac{10}{2\pi fC}$ or $10\ (2\pi fL)$

Because of the frequency dependence of this type of phase shift circuit, the selection of adequate L or C components becomes easier at higher operating frequencies.

4.13 SATURABLE REACTOR TRIGGER CIRCUITS

Saturable reactors can provide a fairly steep wavefront of gate current together with a convenient means of control from a low level DC or AC signal. This type of control is adaptable to feedback systems and provides the additional advantage of multiple, electrically-isolated inputs and outputs for more complex circuits.

4.13.1 Continuously Variable Control

A typical half-wave magnetic amplifier type trigger circuit is shown in Figure 4.23. The gate signal for triggering the SCR is obtained from winding 3-4 of transformer T_1. When the core of T_2 is unsaturated, the winding 3-4 of T_2 presents a high impedance to the gate signal so that only a small voltage is developed across R_3. When the core of T_2 saturates, the impedance of winding 3-4 of T_2 decreases by several orders of magnitude so that a large voltage appears at the gate of the SCR, causing it to trigger. Resistor R_2 limits the gate current to the rated value and resistor R_3 limits the gate voltage produced by the magnetizing current of winding 3-4 of T_2 so that the SCR will not trigger before the core of T_2 saturates. Diode CR_2 serves the dual purpose of preventing a reverse voltage on the gate of the SCR and preventing any reverse current through winding 3-4 which would produce an undesired reset of the core T_2.

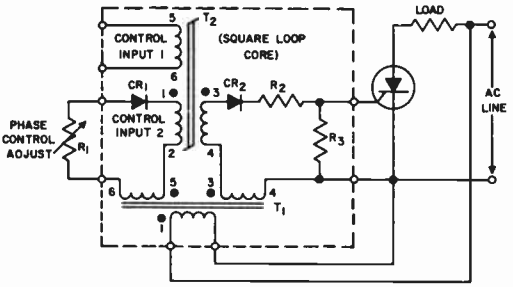


FIGURE 4.23 TYPICAL HALF-WAVE MAGNETIC TRIGGER CIRCUIT

Control signals can be applied to either input 1 or input 2 or both. Input 2 operates in the reset mode by controlling the reset voltage on winding 1-2 of T_2 during the negative half cycle. The setting of the potentiometer R_1 determines the amount of reset of the core during the negative half cycle, which in turn determines the phase angle of the SCR conduction during the positive half cycle. Other control circuits, such as a transistor amplifier stage, can be used in place of R_1. Since power is furnished by winding 5-6 of T_1, no auxiliary power supply is needed. Input 1 operates in the MMF (magnetomotive force) made by controlling the current through the winding 5-6 and the core flux level, which in turn determines the trigger angle. The current for input 1 must be obtained from an external power supply or from a current generating type of transducer.

Additional output windings can be added to T_2 for triggering several SCR's in parallel or in series. Also, additional control windings of the reset or

MMF type can be added to T_2. Full wave and multiple phase operation can be achieved by combining two or more half wave circuits.

4.13.2 On-Off Magnetic Trigger Circuits

Magnetic trigger circuits designed for phase control applications such as the one shown in Figure 4.23 require the use of saturable cores which are large enough to allow the output winding to sustain the gate voltage signal for a full half cycle without saturating. For simple on-off control applications, the magnetic trigger circuits shown in Figure 4.24 permit the use of smaller and less expensive cores since the output winding is not required to sustain the gate voltage signal for a full half cycle. In addition, these circuits have the advantage of not requiring the use of an auxiliary supply transformer.

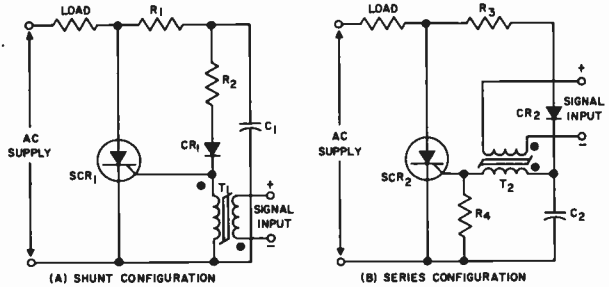


FIGURE 4.24 HALF-WAVE ON-OFF MAGNETIC TRIGGER CIRCUITS

In Figure 4.24(a), one winding of saturable transformer T_1 is connected in shunt with the gate of SCR_1. If T_1 is unsaturated, the current through R_1, R_2 and CR_1 will flow into the gate of SCR_1 during the first part of the positive half cycle and cause SCR_1 to turn on. If T_1 is saturated, the current through R_1, R_2 and CR_1 will be diverted from the gate by the low saturated impedance of the winding on T_1. When T_1 is saturated it can be reset, and the SCR can be made to trigger by a positive voltage on the signal input. Capacitor C_1 provides filtering for the gate signal to prevent undesired triggering due to fast transients on the AC supply.

In Figure 4.24(b), one winding of saturable transformer T_2 is connected in series with capacitor C_2 and the gate of SCR_2. If T_2 is unsaturated the current through R_3 and CR_2 will charge C_2 during the initial part of the positive half cycle. T_2 will saturate after a few degrees of the positive half cycle and permit a rapid discharge of C_2 into the gate of SCR_2, thus causing SCR_2 to trigger. If T_2 is initially saturated at the beginning of the positive half cycle, the winding of T_2 will divert the current from C_2 and prevent C_2 from being charged. Resistor R_4 prevents the voltage at the gate of SCR_2 produced by the current through R_3 from exceeding the maximum gate voltage that will not trigger the SCR. When T_2 is saturated, it can be reset and the SCR can be made to trigger by a positive voltage at the signal input.

The circuits of Figure 4.24 permit the SCR to perform the function of an AC contactor with an isolated DC control winding. Modifications of these circuits permit full wave operation with normally open, normally closed or latching operation. The reader is referred to Chapter 8 for further discussion of static switching circuits.

4.14 SEMICONDUCTOR TRIGGER-PULSE GENERATORS

The simple resistor and capacitor triggering circuits described in Sections 4.12 and 4.13 depend heavily on the specific triggering characteristic of each SCR used. In addition, the power level in the control circuit is high because the entire triggering current must flow through the resistance. Furthermore, they do not readily lend themselves to automatic, self-programmed, or feedback control systems.

Pulse triggering, on the other hand, can accommodate wide tolerances in triggering characteristics by overdriving the gate. The power level in pulse control circuits may also be quite low since the required triggering energy (I_{GT} V_{GT} t) can be stored slowly, then discharged rapidly at the desired instant of triggering. The use of pulse triggering enables small, low-power, signal-type components and transducers to control large, high-current thyristors, as is shown in later chapters.

While there are a multitude of semiconductors and circuits which can produce adequate triggering pulses, this chapter will consider only those most adept at performing this function.

4.14.1 Basic Relaxation Oscillation Criteria

Most devices used to produce trigger pulses (such as: the unijunction transistor, diac trigger diode, the silicon unilateral and bilateral switches, neon lamps, etc.) operate by discharging a capacitor into the thyristor gate. They function in a basic relaxation oscillator circuit by means of a negative resistance characteristic. Specifications for these devices usually include the voltage and current required to achieve negative resistance when approached from either the conducting or non-conducting states. (See also Section 4.1.)

To relate these specifications to the criteria for oscillation, consider the elementary relaxation oscillator circuit of Figure 4.25(a) using a trigger device with voltage to switch V_S, current to switch I_S, holding voltage V_H, and holding current I_H. The device characteristic curve is plotted in Figure 4.25(b), along with load lines representing R_1 and R_2. If R_1 is increased to the maximum value which will sustain oscillations, we will find that its load line intersects the device curve at a point (1) where the negative resistance slope of the device curve is equal to the load line for R_2. This point (1) is very close to I_S and V_S, but not quite the same since the specification of these values is made at the point where the slope of the curve is vertical, representing zero dynamic resistance.

When the triggering point (1) is reached, the operating point transfers to point (2), discharging the capacitor with a peak pulse current, i_p, and producing a peak pulse voltage e_p, across the load resistor R_2 (which includes the thyristor gate impedance). The discharge of the capacitor follows the device curve from point (2) to point (3), where the negative resistance slope is once again tangential with the R_2 load line. The operation then transfers from point (3) to point (4), the capacitor re-charges through R_1 and the oscillation continues.

If R_1 is changed to the minimum value which will sustain oscillation, its new load line will intersect the device curve at point (3). Any smaller value will cause the device to remain conducting at some stable operating point be-

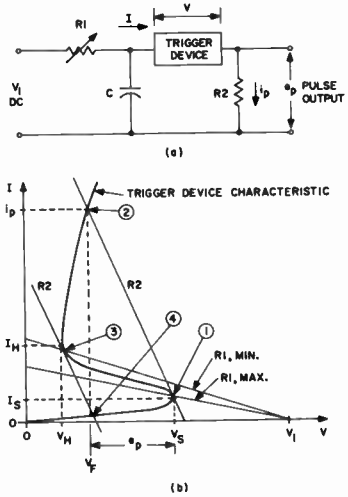


FIGURE 4.25 BASIC RELAXATION OSCILLATOR CIRCUIT AND CHARACTERISTICS

tween (2) and (3). Increasing R_1 beyond the maximum oscillating value causes operation to cease at some point between (1) and the origin.

A very important factor not apparent in Figure 4.25, and often not specified for a device, is switching time, or rise time. A device which slowly switches from point (1) to point (2) will never get there since it is discharging the capacitor as it goes and will reach the device curve somewhere between points (2) and (3). This switching time can be a limiting factor if it is a significant fraction of the discharge time-constant, R_2C.

The magnitude of pulse voltage, e_p, and pulse current, i_p, appearing at the load, resistor R_2 in this circuit, is dependent upon the characteristic curve of the device and the relation between its switching time and the discharge time-constant, R_2C. For values of R_2C large ($> 10X$) in comparison with the switching time of the device, the peak pulse voltage, e_p, is simply the difference between the switching voltage V_S and the conduction voltage drop V_F. The peak pulse current under this condition is found from the intersection of the R_2 load line and the characteristic curve.

When R_2C is smaller, approaching the switching time, both e_p and i_p are reduced by the effective device resistance during switching. As was shown in Section 4.8, reducing peak current, and extending the pulse time accordingly, decreases the probability of triggering a thyristor.

Since the effect of switching time is not readily apparent from the characteristic curve, devices intended for thyristor triggering generally specify the peak pulse voltage across R_2 (where the value of R_2 is chosen to represent typical gate impedance) when discharging a given size capacitor typical for its application.

The following table shows the correlation of the parameter terminologies used in various switching devices with the points on the general characteristic curve:

TABLE 4.1

Terminology on Figure 4.25	UJT	SUS	Diac	Neon
V_S	V_P	V_S	$V_{(BR)}$	V_f
I_S	I_P	I_S	$I_{(BR)}$	
V_H	V_V	V_H		V_e
I_H	I_V	I_H		
e_p	V_{OB1}	V_O	e_p	
i_p				i_p

4.14.2 Unijunction Transistor

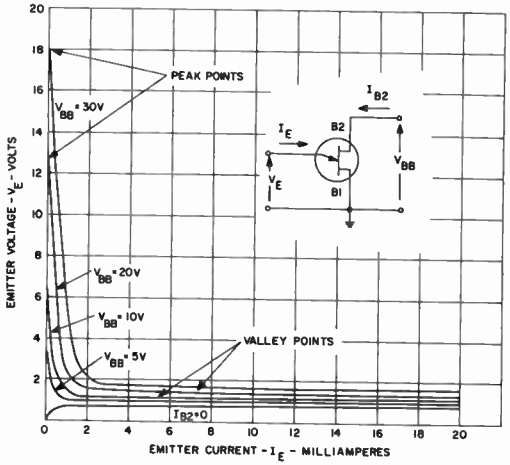


FIGURE 4.26 GE 2N2646 UNIJUNCTION TRANSISTOR SYMBOL AND EMITTER INPUT CHARACTERISTICS.

The UJT has three terminals which are called the emitter (E), base-one (B_1), and base-two (B_2). Between B_1 and B_2 the unijunction has the characteristics of an ordinary resistance. This resistance is the interbase resistance (R_{BB}) and at 25°C has values in the range from 4.7K to 9.1K.

The normal biasing conditions for a typical UJT are indicated in Figure 4.26. If the emitter voltage, V_E, is less than the emitter peak point voltage, V_P, the emitter will be reverse biased and only a small reverse leakage current, I_{EO}, will flow. When V_E is equal to V_P and the emitter current, I_E, is greater than the peak point current, I_P, the UJT will turn on. In the on condition, the resistance between the emitter and base-one is very low and the emitter current will be limited primarily by the series resistance of the emitter to base-one external circuit.

The peak point voltage of the UJT varies in proportion to the interbase voltage, V_{BB}, according to the equation:

$$V_P = \eta V_{BB} + V_D \qquad (4.1)$$

The parameter η is called the intrinsic standoff ratio. The value of η lies between 0.51 and 0.82, and the voltage V_D, the equivalent emitter diode voltage, is in the order of .5 volt at 25°C, depending on the particular type of UJT. It is found that V_P decreases with temperature, the temperature coeffi-

cient being about −3mv/°C for the 2N2646-47 (−2mv/°C for 2N489 series). The variation of the peak point voltage with temperature may be ascribed to the change in V_D (also η for 2N2646-47 series). It is possible to compensate for this temperature change by making use of the positive temperature coefficient of R_{BB}. If a resistor R_{B2} is used in series with base-two as shown in Figure 4.27, the temperature variation of R_{BB} will cause V_{BB} to increase with temperature. If R_{B2} is chosen correctly, this increase in V_{BB} will compensate for the decrease in V_P in Equation 4.1. Over a temperature range of −40°C to 100°C, Equation 4.3(a) gives an approximate value of R_{B2} for the majority of 2N2646 and 2N2647 UJT's. Equation 4.3(b) gives R_{B2} for the 2N489 MIL series, 2N1671A and B, and the 2N2160.

$$R_{B2} \approx \frac{10000}{\eta V_1} \tag{4.3a}$$

$$R_{B2} \approx \frac{0.40 R_{BB}}{\eta V_1} + \frac{(1-\eta) R_{B1}}{\eta} \tag{4.3b}$$

For a more detailed discussion of the characteristics of the various types of UJT's the reader is referred to Reference 8. Quantitative data and techniques for temperature compensation on an individual and general basis in very high performance circuits over extreme temperature ranges are discussed in Reference 9.

4.14.2.1 Basic UJT Pulse Trigger Circuit

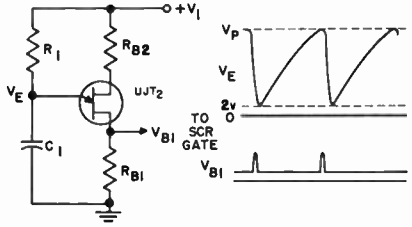


FIGURE 4.27 BASIC UNIJUNCTION TRANSISTOR RELAXATION OSCILLATOR-TRIGGER CIRCUIT WITH TYPICAL WAVEFORMS.

The basic UJT trigger circuit used in applications with the SCR is the simple relaxation oscillator shown in Figure 4.27. In this circuit, the capacitor C_1 is charged through R_1 until the emitter voltage reaches V_P, at which time the UJT turns on and discharges C_1 through R_{B1}. When the emitter voltage reaches a value of about 2 volts, the emitter ceases to conduct, the UJT turns off and the cycle is repeated. The period of oscillation, T, is fairly independent of the supply voltage and temperature, and is given by:

$$T = \frac{1}{f} \approx R_1 C_1 \ln \frac{1}{1-\eta} = 2.3\, R_1 C_1 \log_{10} \frac{1}{1-\eta} \tag{4.4}$$

For an approximate nominal value of intrinsic standoff ratio of $\eta = 0.63$, $T = R_1 C_1$.

The design conditions of the UJT firing circuit are very broad. In general, R_{B1} is limited to a value below 100 ohms although values up to 2 or 3K

are possible in some applications. The resistor R_1 is limited to a value between 3K and 3 Meg. The lower limit on R_1 is set by the requirement that the load line formed by R_1 and V_1 intersect the emitter characteristic curve of Figure 4.26 to the left of the valley point, otherwise the UJT in Figure 4.27 will not turn off. The upper limit on R_1 is set by the requirement that the current flowing into the emitter at the peak point must be greater than I_P for the UJT to turn on. The recommended range of supply voltage V_1 is from 10 volts to 35 volts. This range is determined on the low end by the acceptable values of signal amplitude and at the high end by the allowable power dissipation of the UJT.

If the pulse output (V_{B1}) of the circuit of Figure 4.27 is coupled directly, or through series resistors, to the gates of the SCR's, the value of R_{B1} should be low enough to prevent the DC voltage at the gate due to interbase current from exceeding the maximum voltage that will not trigger the SCR's (see Figure 4.12) V_{GT} (max) at the maximum junction temperature at which the SCR's are expected to operate. To meet this criterion, R_{B1} should be chosen in accordance with the following inequality:

$$\frac{R_{B1}\, V_1}{R_{BB}\,(\text{min}) + R_{B1} + R_{B2}} < V_{GT(\text{max})} \tag{4.5}$$

For the C35 (2N681) types at a maximum junction temperature of 125°C, V_{GT} (max) is 0.25 volt, hence for a supply voltage of 35 volts or less, R_{B1} should be 50 ohms or less. If the pulse output from the UJT firing circuit is coupled to the gates of the SCR's by means of transformers or capacitors, these limitations do not apply.

4.14.2.2 Designing the Unijunction Transistor Trigger Circuit

The type 2N2646 and 2N2647 UJT's are specifically characterized for SCR trigger circuits and are factory tested to ensure reliable operation with all types of G-E SCR's over their respective temperature ranges. Their condensed specifications are given in Chapter 21.

The design of a suitable UJT trigger circuit can be achieved rapidly and easily by using the design curves given in Figures 4.28(a) and 4.28(b) for the 2N2646 and 2N2647, respectively. These curves give the minimum supply voltage V_1 required to guarantee triggering of various types of SCR's over the indicated temperature range as a function of the UJT emitter capacitor C_1 and the base-one coupling resistor R_{B1} or base-one coupling transformer. The value of resistor R_1 is not important for the purposes of the design provided that it is within the limits required for the UJT to oscillate. If R_{B2} is significantly greater than 100 ohms the minimum supply voltage which is required V_1' should be calculated from the minimum supply voltage V_1 given by Figures 4.28(a) and 4.28(b) using the equation:

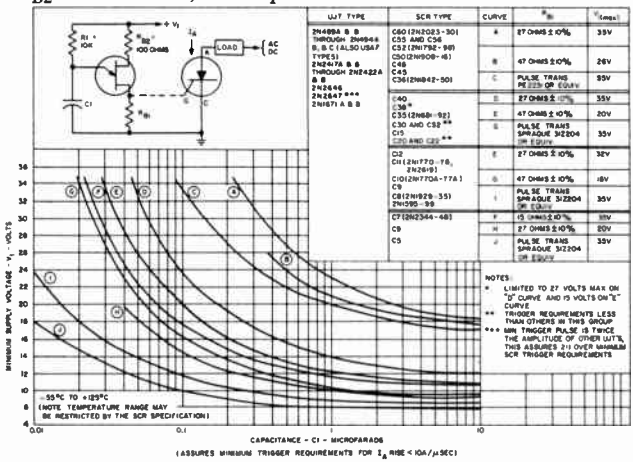
$$V_1' = \frac{(2200 + R_{B2})\, V_1}{2300} \tag{4.6}$$

It is recommended in all cases that a resistance of 100 ohms or greater be used in series with either base-two or in series with the power supply to protect the UJT from possible thermal runaway. This is particularly important when operating at high ambient temperatures, at high supply voltages, or with large values of emitter capacitance.

As an example of the use of Figure 4.28 in the practical design of an SCR trigger circuit, consider the following problem:

Example: A circuit is required to trigger a C11 type (2N1773 series) SCR at the lowest possible supply voltage with a 2N2646 UJT and pulse transformer coupling. The value of capacitance, chosen on the basis of operating frequency, is 0.1 μf, and temperature compensation is desired. Assume $\eta = 0.66$ for a nominal value.

Solution: From the chart in Figure 4.28(a) it can be seen that Curve I should be considered and that the supply voltage V_1 should not exceed $V_{1(max)} = 35V$. On Curve I the minimum supply voltage for a value of $C_1 = 0.1$ μf is about $V_1 = 12$ volts. The value for R_{B2} is determined from Equation 4.3(a) as $R_{B2} \approx \dfrac{10000}{(.66)(12)} = 1260 \approx$ 1000 ohms (nearest standard value). With this value of R_{B2} the supply voltage must be increased to a value V_1' in accordance with Equation 4.6 from which $V_1' = \dfrac{(2200 + 1000)}{2300}(12) \approx 17$ volts. Thus, a suitable design for this example would be $C_1 = 0.1$ μf, $R_{B2} = 1$ K ohms, and $V_1' = 17$ volts.



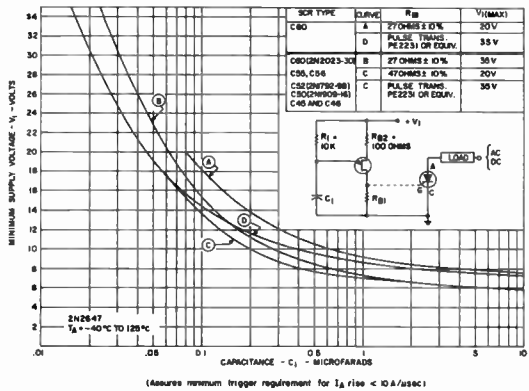


FIGURE 4.28 UJT TRIGGER CIRCUIT DESIGN CURVES

If, in the case of the 2N2646 and 2N2647 UJT's, R_{B2}, as determined from Equation 4.3(a) causes V_1' (from Equation 4.6) to be larger than can be attained practically or economically, the use of the 2N489 series, the 2N1671A or the 2N1671B is suggested. [Equation 4.3(b) yields a lower value of R_{B2}] alternatively, if extreme temperature compensation is not required, or if the temperature range to which the 2N2646/47 UJT's are subjected is not great, a value of $R_{B2} \geq 100$ ohms may be used.

4.14.2.3 Synchronization Methods

In the basic trigger circuit of Figure 4.27, the UJT can be triggered at any intermediate part of the cycle by reducing either the interbase voltage alone or the supply voltage, V_1. This results in an equivalent decrease in V_P in accordance with Equation 4.1 (or 4.3) and causes the UJT to trigger if V_P drops below the instantaneous value of V_E. Thus, the base-two terminal or the main supply voltage can be used to synchronize the basic trigger circuit. Figure 4.29 illustrates the use of a negative synchronizing pulse at base-two.

Two methods of achieving synchronization with the AC line are illustrated in Figure 4.30. A full wave rectified signal obtained from a rectifier bridge or a similar source is used to supply both power and a synchronizing signal to the trigger circuit. Zener diode CR_1 is used to clip and regulate the peaks of the AC as indicated in Figures 4.30(a) and (b).

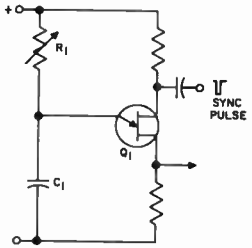


FIGURE 4.29 PULSE SYNCHRONIZATION OF UJT RELAXATION OSCILLATOR

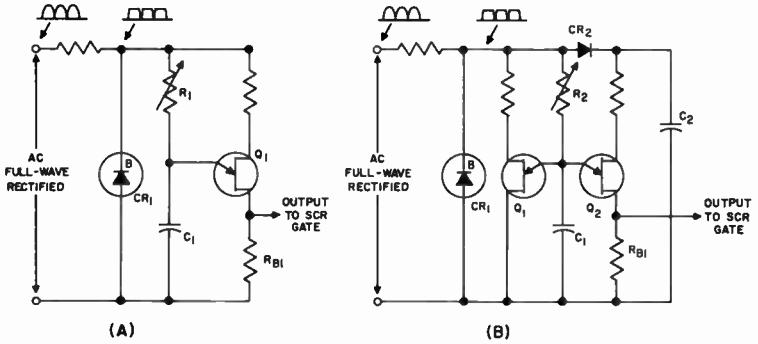


FIGURE 4.30 CIRCUITS FOR SYNCHRONIZATION TO AC LINE

At the end of each half-cycle the voltage at base-two of Q_1 will drop to zero, causing Q_1 to trigger. The capacitors C_1 are thus discharged at the beginning of each half cycle and the trigger circuits are thus synchronized with the line. In Figure 4.30(a) a pulse is produced at the output at the end of each half cycle which can cause the SCR to trigger and produce a small current in the load. If this is undesirable, a second UJT can be used for discharging the capacitor at the end of the half cycle as illustrated in Figure 4.30(b). Diode CR_1 and capacitor C_2 are used to supply a constant DC voltage to Q_2. The voltage across Q_1 will drop to zero each half-cycle causing C_1 to be discharged through Q_1 rather than through the load R_{B1}. The UJT's should be chosen so that Q_1 has a higher standoff ratio than Q_2.

4.14.3 Silicon Unilateral Switch (SUS)[12]

The SUS, such as the type D13D1, is essentially a miniature SCR having an anode gate (instead of the usual cathode gate) and a built-in low-voltage avalanche diode between the gate and cathode. The symbol for the SUS and its equivalent circuit are shown in Figure 4.31. Its anode-to-cathode electrical characteristic is shown in Figure 4.32 for no external connection to the gate terminal.

The SUS is usually used in the basic relaxation oscillator circuit shown in Figure 4.25(a) and its characteristics follow the same criteria for oscillation. The type D13D1 has the following specifications:

Switching Voltage, V_S	6 to 10 volts
Switching Current, I_S	0.5 ma, maximum
Holding Voltage, V_H	Not specified ($\approx$ 0.7 V at 25°C)
Holding Current, I_H	1.5 ma, maximum
Forward Voltage, V_F (at $I_F = 200$ ma)	1.75 volts
Reverse Voltage Rating, V_R	30 volts
Peak Pulse Voltage, V_O	3.5 volts minimum

The Peak Pulse Voltage, V_O, specification is very important for thyristor triggering applications since it is the only realistic figure-of-merit that indicates the ability of the triggering device to transfer charge from the capacitor to the thyristor gate. This voltage is measured with the SUS operating in the circuit of Figure 4.25(a), where $V_1 = 15$ volts, $R_1 = 100$ K ohms, $C = 0.1$ μf, and $R_2 = 20$ ohms. The peak pulse voltage is measured across resistor R_2. The magnitude of the pulse voltage depends both upon the difference between V_S and V_F and upon switching time, as explained in Section 4.14.1. The component values used in the pulse test are adequate for triggering most thyristors.

The major difference in function between the SUS and the UJT is that the SUS switches at a fixed voltage, determined by its internal avalanche diode, rather than a fraction (η) of another voltage. It should also be noted that I_S is much higher in the SUS than in the UJT, and is also very close to I_H. These factors restrict the upper and lower limits of frequency or time-delay which are practical with the SUS.

For synchronization, lock-out, or forced switching, bias or pulse signals may be applied to the gate terminal of the SUS.

4.14.4 Silicon Bilateral Switch (SBS)[12]

The SBS, such as the type D13E1, is essentially two identical SUS

structures arranged in inverse-parallel, as shown in Figures 4.33 and 4.34. Since it operates as a switch with both polarities of applied voltage, it is particularly useful for triggering the bidirectional triode thyristors (triacs) with alternate positive and negative gate pulses. This operation is obtained by using an alternating voltage supply for V_1 of Figure 4.25, rather than the DC supply shown.

Specifications for the SBS type D13E1 are identical to those of the SUS type D13D1 with the exception of reverse voltage rating, which is not applicable to the SBS.

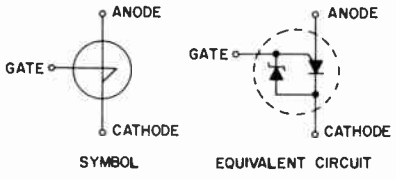


FIGURE 4.31
THE SILICON UNILATERAL SWITCH (SUS)

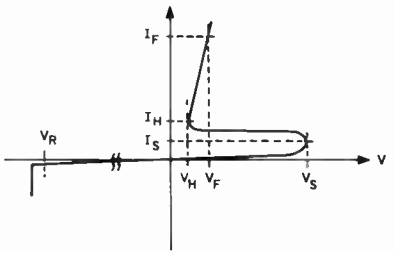


FIGURE 4.32
SUS CHARACTERISTIC CURVE

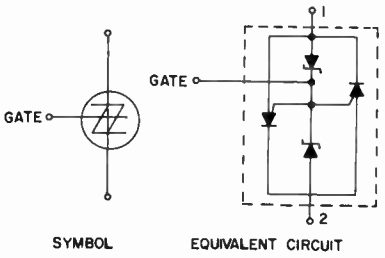


FIGURE 4.33
THE SILICON BILATERAL SWITCH (SBS)

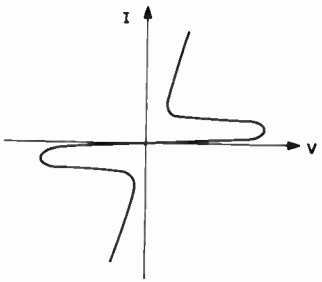


FIGURE 4.34
SBS CHARACTERISTIC CURVE

4.14.5 Bilateral Trigger Diode (Diac)

The diac, such as the type ST-2 is essentially a transistor structure, Figure 4.35, which exhibits a negative resistance characteristic above a given switching current $I_{(BR)}$. The characteristic curve of Figure 4.36 shows that this negative resistance region extends over the full operating range of currents above $I_{(BR)}$ hence the concept of a holding current I_H does not apply.

The diac is used in the simple relaxation oscillator circuit of Figure 4.25, and the criteria for oscillation are the same. For alternating pulse output, the supply voltage for the oscillator circuit, V_1, may be an alternating voltage.

FIGURE 4.35 SYMBOL OF BILATERAL TRIGGER DIODE (DIAC)

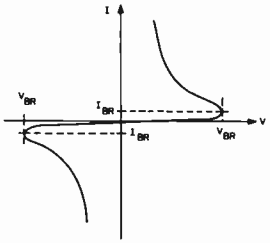


FIGURE 4.36 DIAC CHARACTERISTIC CURVE

The type ST-2 diac has the following specifications:

$V_{(BR)}$ ..... 28 to 36 volts
$I_{(BR)}$ ..... 200 μamp (maximum)
e_p ..... 3 volts (minimum)

The peak pulse voltage, e_p, is measured under the same conditions used with the SUS and SBS, namely: $R_2 = 20$ ohms; $C = 0.1$ microfarad. Since the ST-2 is primarily used to trigger triacs, this minimum value of e_p has been established to ensure proper triggering of all G-E triacs, assuming, of course, the proper conditions of supply voltage and load impedance in the power circuit of the triac.

4.14.6 Other Semiconductor Trigger Devices

Several other unilateral and bilateral switching devices exist, having characteristics similar to those discussed above. In general, all operate as relaxation oscillators and are subject to the same criteria for oscillation. If the peak pulse voltage (or current) output is not specified, then the maximum switching time must be known. Otherwise, the trigger circuit must be overdesigned by a factor depending upon the uncertainty of the unknowns.

4.15 NEON GLOW LAMPS AS TRIGGER DEVICES

The low price of neon glow lamps has led many to consider their use for triggering thyristors. The characteristics of the glow lamp are quite similar, but for magnitude, to those of the diac. The switching voltage is generally on the order of 90 volts and the switching current is extremely small (below 1 μa). However, the switching time is large in comparison with semiconductor devices, and the peak pulse voltage is usually not specified.

The G-E type 5AH is an isotope-stabilized neon glow lamp now being used in many low-cost SCR control circuits. The 5AH lamp has the following specifications:

V_S . . . . . 60 to 100 volts
I_S . . . . . Not specified
V_F . . . . . Approx. 60 volts at 5 ma
V_H . . . . . Not specified
I_H . . . . . Not specified
i_p . . . . . 25 ma (minimum)

The peak pulse current, i_p, is measured in a 20 ohm resistor when discharging a 0.1 μf capacitor. The minimum peak pulse voltage is, therefore, 0.5 volts under this condition. The specification also includes an indication of the operating life of the lamp: 5000 hours operation, on the average, at 5 ma DC results in a 5 volt change in V_S or V_F. This has not been correlated to hours operation in a relaxation oscillator at 120 Hz.

Glow lamps are useful for thyristor triggering under the following conditions:

(a) Thyristor I_{GT} on the order of 10 ma or less
(b) Wide tolerance in V_S is acceptable
(c) Minimum pulse voltage measured in sample lot several times minimum required to trigger the thyristor
(d) Change in V_S and pulse output with operating time is acceptable
(e) Cost of primary importance

4.16 PULSE TRANSFORMERS

Pulse transformers are often used to couple a trigger-pulse generator to a thyristor in order to obtain electrical isolation between the two circuits. There are many vendors of pulse transformers suitable for this purpose. Although several specific model numbers are shown on circuit diagrams in this manual, it is not our purpose nor intent to serve as a testing or approval function.

The transformers usually used for thyristor control are either 1:1, two-winding, or 1:1:1 three-winding types. As shown in Figure 4.37, the transformer may be connected directly between gate and cathode, or may have a series resistor R to either reduce the SCR holding current or to balance gate currents in a three-winding transformer connected to two SCR's, or may have a series diode D to prevent reverse gate current in the case of ringing or reversal of the pulse transformer output voltage. The diode also reduces holding current of the SCR. In some cases where high noise levels are present, it may be necessary to load the secondary of the transformer with a resistor to prevent false triggering.

Figure 4.38 shows several ways of using a transformer to drive an inverse-parallel pair of SCR's. Full isolation is provided by the three-winding transformer in Figure 4.38(a). Where such isolation is not required, a two-winding transformer may be used either in a series mode, Figure 4.38(b), or a parallel mode, Figure 4.38(c). In any case, the pulse generator must supply enough energy to trigger both SCR's, and the pulse transformer (plus any additional balancing resistors) must supply sufficient gate current to both SCR's under worst-case conditions of unbalanced gate impedances.

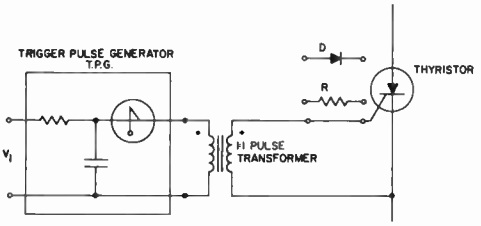


FIGURE 4.37 BASIC PULSE TRANSFORMER COUPLING

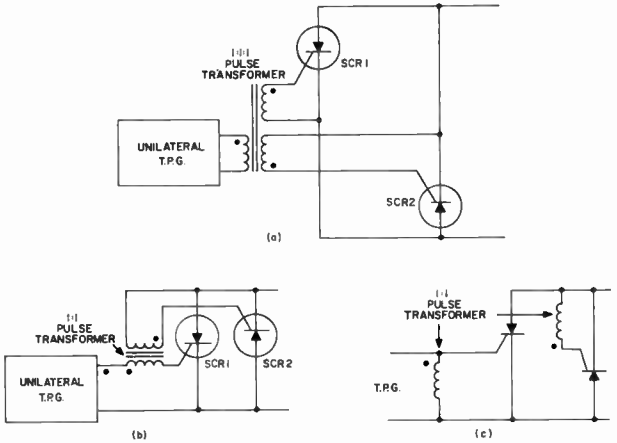


FIGURE 4.38 PULSE TRANSFORMER CONNECTIONS FOR TWO SCR'S

The prime requirement of a trigger pulse transformer is one of efficiency. The simplest test is to use the desired trigger pulse generator to drive a 20 ohm resistor alone and then drive the same resistor through the pulse transformer. If the pulse waveforms across the resistor are the same under both conditions, the transformer is perfect. Some loss is to be expected, however, and must be compensated by increased drive from the generator.

Some of the transformer design factors to be considered are:

(a) Primary magnetizing inductance should be high enough so that magnetizing current is low, in comparison with pulse current, during the pulse time.

(b) Since most pulse generators are unilateral, core saturation must be avoided.

(c) Coupling between primary and secondary should be tight, for single-SCR control, or may have specified leakage reactance to assist in balancing currents for multiple-SCR control.

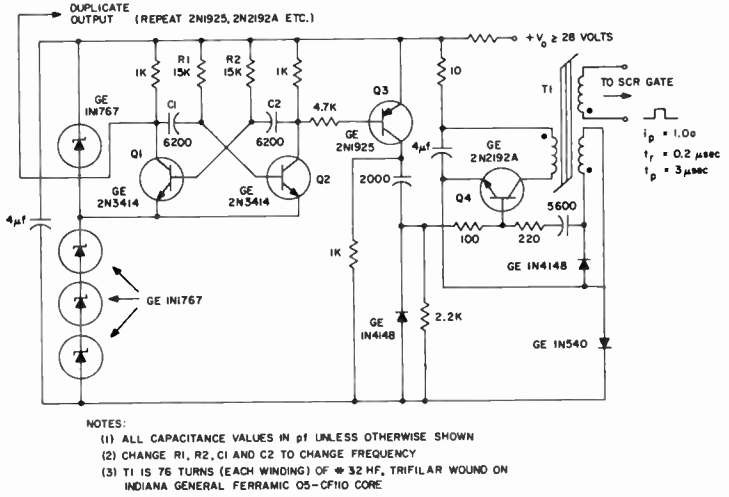
(d) Insulation between windings must be adequate for the application, including transients.

(e) Interwinding capacitance is usually insignificant but may be a path for undesirable stray signals at high frequencies.

4.17 TRANSISTOR BLOCKING OSCILLATOR

Most of the semiconductor triggering devices discussed thus far produce pulse rise times on the order of 0.5 to 5 microseconds. Where the thyristor must handle a large current in a short time (i.e., a high di/dt), these devices may be inadequate. The blocking oscillator transistor circuit, using a high-speed switching transistor, is capable of producing high-current triggering pulses with very short rise times.

Figure 4.39 employs a blocking oscillator,[13] driven from a multivibrator, to produce rectangular gate pulses of 1.0 ampere with 0.2 microsecond rise time and 3 microsecond pulse width. The purpose of the multivibrator, rather than a relaxation oscillator, is to permit triggering of two SCR's alternately by using a second blocking oscillator driven from the collector of transistor Q_1.



NOTES:
(1) ALL CAPACITANCE VALUES IN pf UNLESS OTHERWISE SHOWN
(2) CHANGE R1, R2, C1 AND C2 TO CHANGE FREQUENCY
(3) T1 IS 76 TURNS (EACH WINDING) OF # 32 HF, TRIFILAR WOUND ON INDIANA GENERAL FERRAMIC 05-CF110 CORE

FIGURE 4.39 HIGH SPEED TRANSISTOR BLOCKING OSCILLATOR DRIVEN BY A MULTIVIBRATOR.

The circuit of Figure 4.39 is particularly useful for triggering thyristors in inverters, pulse modulators, and other circuits which impose fast turn-on requirements. Frequency of the multivibrator may be changed by changing the indicated component values, or may be varied by controlling the voltage to which resistors R_1 and R_2 are returned.

4.18 TRANSISTOR FLIP-FLOP

The transistor flip-flop circuit[8] is also useful for driving SCR or triac gates. The transistors may drive the gates directly, as described in Section 8.9.2, or through a transformer as shown in Figure 4.40. This transformer must, of course, be designed to avoid saturation at the lowest operating frequency and highest supply voltage. The circuit of Figure 4.40 provides

square-wave gate signals, alternating from 7 volts positive to 7 volts negative (on open circuit) and up to 800 ma gate current. The flip-flop is driven by a unijunction transistor for precise timing, but may be connected as a free-running multivibrator.

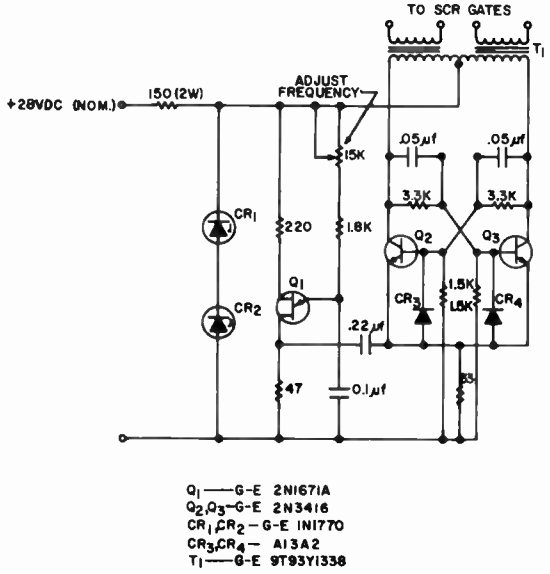


FIGURE 4.40 FLIP-FLOP TRIGGER CIRCUIT FOR 400 Hz

4.19 SCR'S AS GATE SIGNAL AMPLIFIERS

The availability of SCR's with highly sensitive gates permits use of these devices to trigger higher rated SCR's as shown in Figure 4.41. Here, for example, a C5B as SCR_1 requires less than 200 microamperes of gate signal to trigger. Current then flows through R_2, SCR_1, and into the gate of SCR_2. When the current reaches the triggering requirements of SCR_2, this device turns on and shunts the main power away from SCR_1. In addition to providing a means of triggering high current SCR's by low level signals from high impedance sources, this type of triggering yields positive triggering from pulsed gate signals even with highly inductive loads due to the much lower latching current requirements of the C5 in comparison with the higher rated SCR's. With SCR_1 latched into conduction, the gate of SCR_2 is driven by a trigger signal which is maintained until SCR_2 is forced into conduction. R_2 limits the current through SCR_1 to a value within its rating. SCR_1 must meet the same voltage requirements as SCR_2. However, its current duty is generally of a pulsed nature, and hence negligible.

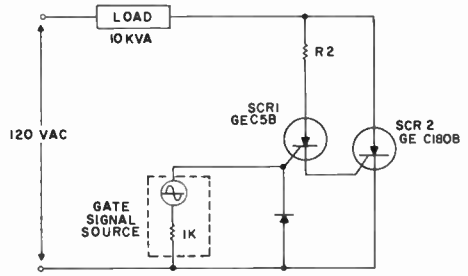


FIGURE 4.41 USE OF LOW CURRENT SCR AS A GATE SIGNAL AMPLIFIER

Depending on the nature of the control input signal other types of SCR's can be considered for triggering larger SCR's. The LASCR (Chapter 13) can be used where direct triggering by light is required. Also, the LASCR in conjunction with a suitable light source provides a simple way in which to obtain electrical isolation in SCR control circuitry.

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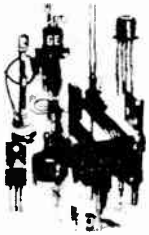
13. "A 15KC, DC to DC Converter," J. A. Pirraglia and R. Rando, IEEE Conference Record of the Industrial Static Power Conversion Conference, No. 34C20, The Institute of Electrical and Electronic Engineers, New York, N. Y., 1965.

*Refer to Chapter 22 for availability and ordering information.

5 SCR TURN-OFF CHARACTERISTICS AND METHODS



5.1 SCR TURN-OFF CHARACTERISTICS

If forward voltage is applied to a unidirectional thyristor (hereafter referred to as "SCR") too soon after anode current ceases to flow, the SCR will go into the conduction state again. It is necessary to wait for a definite interval of time after cessation of current flow before forward voltage can be reapplied. Chapter 1 describes the physical reasons for this required interval. For turn-off-time as it affects bi-directional thyristors, see Chapter 7.

To measure the required interval, the SCR is operated with current and voltage waveforms shown in Figure 5.1. The interval between t_3 and t_8 is then decreased until the point is found when the SCR will just support reapplied forward voltage.

This interval is not a constant, but is a function of several parameters. Thus, the minimum time t_3 to t_8 will increase with:

1. An increase in junction temperature.
2. An increase in forward current amplitude (t_1 to t_2).
3. An increase in the rate of decay of forward current (t_2 to t_3).
4. A decrease in peak reverse current (t_4).
5. A decrease in reverse voltage (t_5 to t_7).
6. An increase in the rate of reapplication of forward blocking voltage (t_8 to t_9).
7. An increase in forward blocking voltage (t_9 to t_{10}).
8. An increase in external gate impedance.
9. A more positive gate bias voltage.

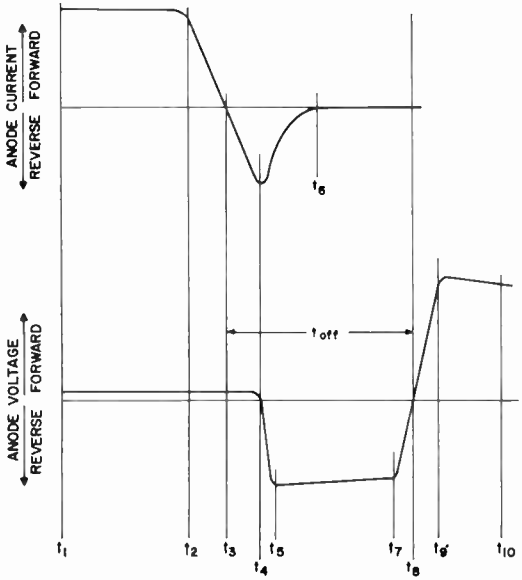


FIGURE 5.1 SCR WAVEFORM FOR TURN-OFF TIME MEASUREMENTS

5.1.1 SCR Turn-off Time (t_{off})

The turn-off time of an SCR is defined as the shortest interval between the time (t_3) when forward current reaches zero and the time (t_8) when the SCR is able to block reapplied forward voltage without turning on; it is measured under specified conditions of current, voltage and temperature.

Changes in the specified conditions change the SCR turn-off time. Figure 5.2 for example gives a typical curve of the change in SCR turn-off time with junction temperature and 5.3 shows the change with forward current.

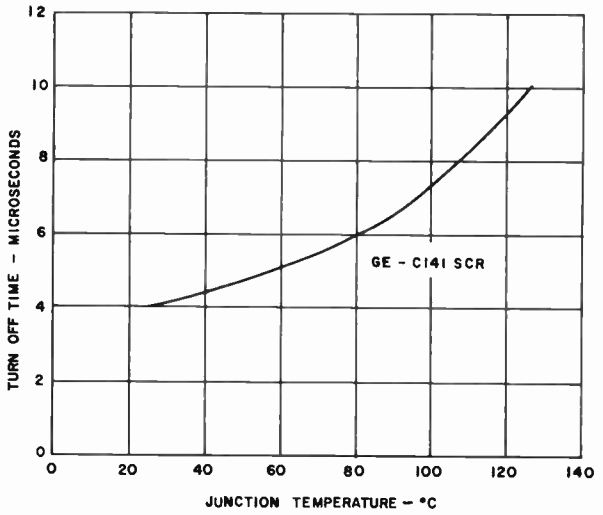


FIGURE 5.2 VARIATION OF TURN-OFF TIME WITH JUNCTION TEMPERATURE

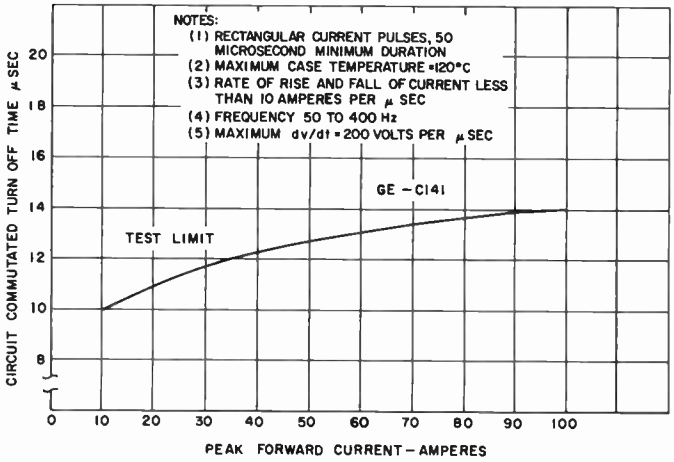


FIGURE 5.3 VARIATION OF TURN-OFF TIME WITH PEAK FORWARD CURRENT FOR A HIGH SPEED SCR.

5.1.2 Circuit Turn-off Time (t_c)

The circuit turn-off time is the turn-off time that the circuit presents to the SCR.

The circuit turn-off time (t_c) must always be greater than the turn-off time of the SCR (t_{off}); otherwise the SCR will turn on.

The turn-off times of standard SCR's are usually given as typical values. Wide deviations from the typical values can occur. In those circuits where turn-off time is a critical characteristic, it is necessary for the circuit designer to have control over the maximum value of SCR turn-off time. For this reason General Electric offers a range of SCR's with guaranteed maximum turn-off times under specified standard conditions of waveform and temperature.

5.2 PULSE TURN-OFF TIME

Pulse turn-off time ($t_{off(pulse)}$) is a measure of hot-spot temperature and reflects the di/dt capability of the SCR. This characteristic is discussed further in Chapter 3.

5.3 REVERSE RECOVERY CURRENT AND REVERSE RECOVERY TIME

The time during which reverse recovery current flows in the SCR (t_3 to t_6 in Figure 5.1) is known as the reverse recovery time. This is the time required before the SCR can block *reverse* voltage. This should not be confused with turn-off time which is the time that has to elapse before the SCR can block reapplied *forward* voltage. The reverse recovery phenomenon is also common in junction diodes.

Reverse recovery time in typical SCR's is of the order of a few microseconds. Recovery time increases as forward current increases and also increases as the rate of decay of forward current decreases.

The reverse recovery current phenomenon plays a minor but important part in the application of SCR's:

1. In full wave rectifier circuits using SCR's as the rectifying elements the reverse recovery current has to be carried in the forward direction by the complementary SCR's. This can give rise to high values of turn-on current.
2. In certain inverter circuits such as the McMurray-Bedford circuit (Chapter 11) where one SCR is turned off by turning another on, the reverse recovery current of the first gives rise to high values of turn-on current in the second.
3. The cessation of reverse current, which can be very sudden, may produce damaging voltage transients and radio frequency interference.
4. When SCR's are connected in series the reverse voltage distribution may be seriously affected by mismatch of reverse recovery times (Chapter 6).

5.4 TURN-OFF METHODS

The gate has no control over the SCR once anode-to-cathode current is flowing. External measures therefore have to be applied to stop the flow of current. There are two basic methods available for commutation, as the turn-off process is called.

5.4.1 Current Interruption

The current through the SCR may be interrupted by means of a switch in either of two positions, Figure 5.4. The switch must be operated for the required turn-off time. Note that the operation of the switch will cause the SCR to see high values of dv/dt.

As it is seldom that a mechanical switch is suitable for commutation, various static switching circuits have been developed for this purpose.

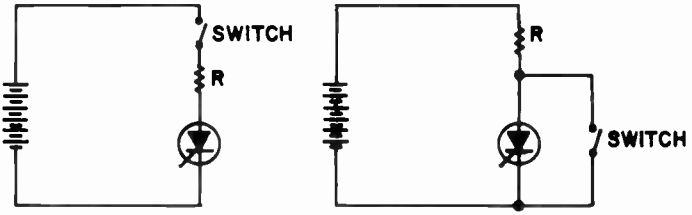


FIGURE 5.4 COMMUTATION BY CURRENT INTERRUPTION

5.4.2 Forced Commutation

When the above methods of current interruption are not acceptable, then forced commutation must be used. The essence of the forced commutation method is to switch current from some energy source so as to force more current through the SCR in the reverse direction than is trying to flow in the forward direction. Forced commutation is the preferred method as it tends to give shortened device turn-off time.

5.5 CLASSIFICATION OF FORCED COMMUTATION METHODS

There are six distinct classes by which the energy is switched across the SCR to be turned off:

Class A Self commutated by resonating the load
Class B Self commutated by an LC circuit
Class C C or LC switched by another load-carrying SCR
Class D C or LC switched by an auxiliary SCR
Class E An external pulse source for commutation
Class F AC line commutation

Examples of circuits which correspond to these classes will now be given. These examples show the classes as choppers (Chapter 11). The commutation classes may be used in practice in configurations other than choppers. References to literature covering the different classes will be found in Chapter 11.

5.5.1 Class A—Self commutated by resonating the load

When SCR_1 is triggered, anode current flows and charges up C in the polarity indicated. Current will then attempt to flow through the SCR in the reverse direction and the SCR will be turned off.

The condition for commutation is that the LCR circuit must be underdamped.

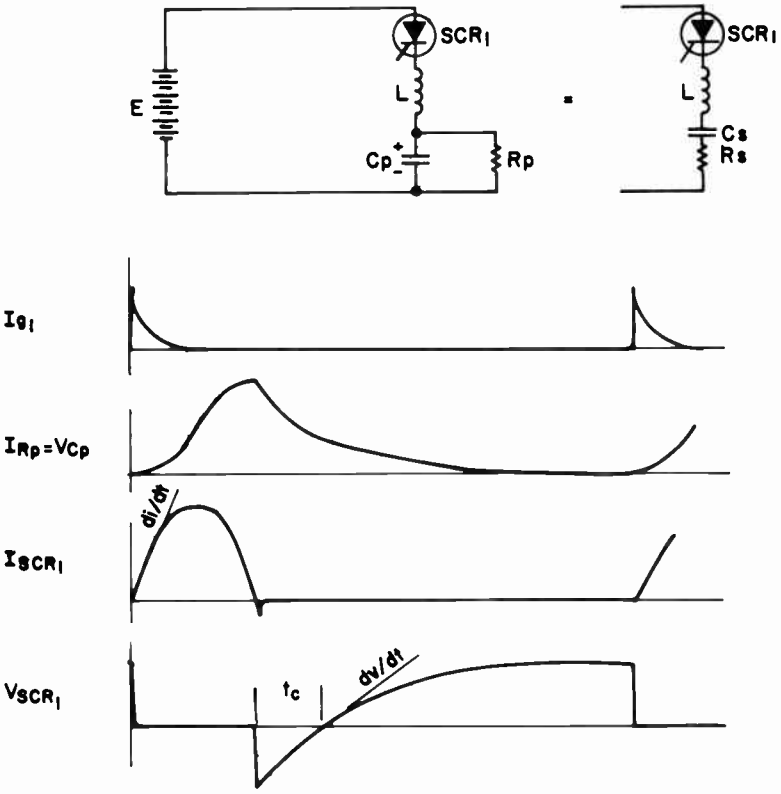


FIGURE 5.5 CLASS A COMMUTATION

5.5.2 Class B—Self commutated by an LC circuit

Example 1

Before the gate pulse is applied, C charges up in the polarity indicated. When SCR_1 is triggered, current flows in two directions.

1. The load current I_R flows through R.
2. A pulse of current flows through the resonant LC circuit and charges C up in the reverse polarity. The resonant-circuit current will then reverse and attempt to flow through the SCR in opposition to the load current. The SCR will turn off when the reverse resonant-circuit current is greater than the load current.

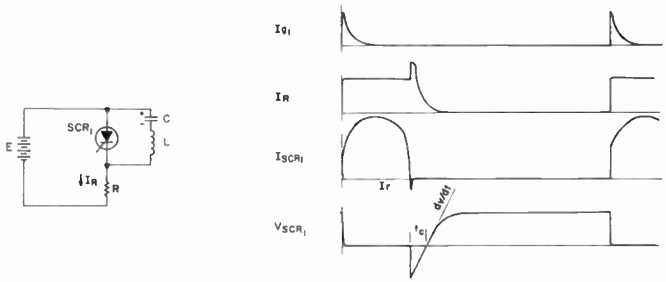


FIGURE 5.6 CLASS B COMMUTATION (EXAMPLE 1)

Class B—Self commutated by an LC circuit

Example 2—The Morgan Circuit

From the previous cycle the capacitor is charged as shown in Figure 5.7 and the reactor core has been saturated "positively."

When SCR_1 is triggered, the capacitor voltage is applied to the reactor winding L_2. The polarity of the applied voltage immediately pulls the core out of saturation. For the time t_1 to t_2 (Figure 5.7) the load current is flowing through R. Simultaneously the capacitor is being discharged.

When the voltage across L_2 has been applied for the prescribed time, the core goes into "negative" saturation. The inductance of L_2 changes from the high unsaturated value to the low saturated value.

The resonant charging of C now proceeds much more rapidly from time t_2 to t_3. As soon as the peak of current is reached and current starts to decrease, the voltage across L_2 reverses.

As soon as the voltage reverses, the core comes out of saturation again, the inductance rises to the high value and the recharging of C proceeds at a more leisurely pace (t_3 to t_4).

The voltage across the inductor is held for the prescribed time and then positive saturation occurs (t_4).

Now the capacitor is switched directly across the SCR via the saturated inductance of L_2. If the reverse current exceeds the load current SCR_1 will be turned off. The remaining charge in C then is dissipated in the load and C is charged up as in Figure 5 ready for the next cycle (t_5).

It is quite possible in practice to design L so that negative saturation does not occur. In this case the anode-current pulse from t_2 to t_3 is omitted.

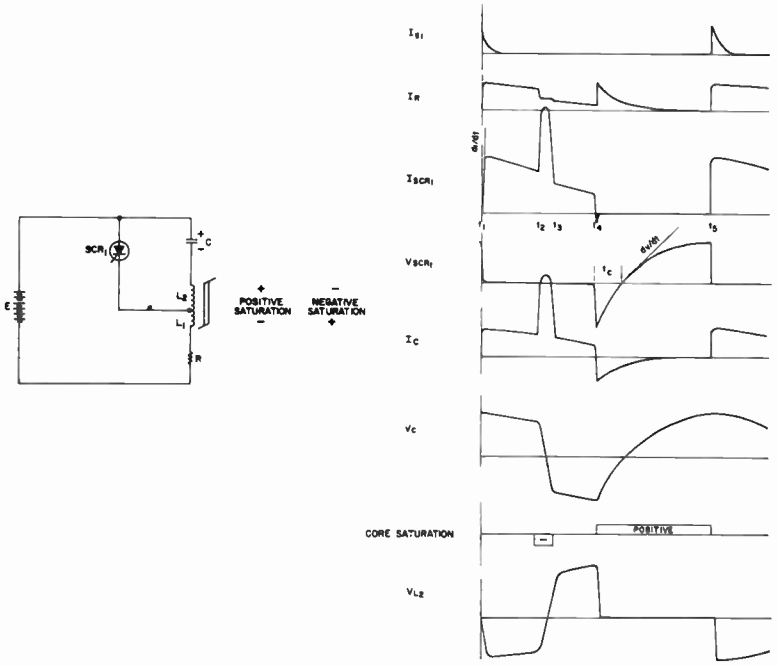


FIGURE 5.7 CLASS B COMMUTATION (EXAMPLE 2)

5.5.3 Class C—C or LC switched by another load-carrying SCR

Assume SCR_2 is conducting. C then charges up in the polarity shown. When SCR_1 is triggered, C is switched across SCR_2 via SCR_1 and the discharge current of C opposes the flow of load current in SCR_2.

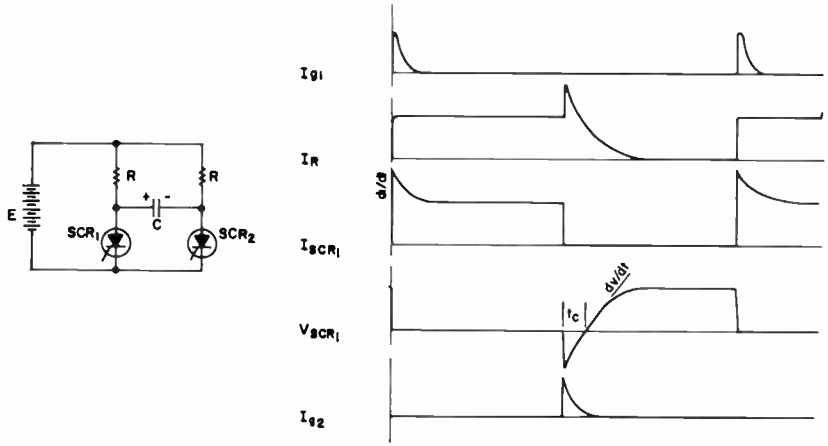


FIGURE 5.8 CLASS C COMMUTATION

5.5.4 Class D—LC or C switched by an auxiliary SCR

Example 1

The circuit shown in Figure 5.8 (Class C) can be converted to Class D if the load current is carried by only one of the SCR's, the other acting as an auxiliary turn-off SCR. The auxiliary SCR would have a resistor in its anode lead of say ten times the load resistance.

Example 2

SCR_2 must be triggered first in order to charge up the capacitor in the polarity shown. As soon as C is charged, SCR_2 will turn off due to lack of current.

When SCR_1 is triggered the current flows in two paths: Load current flows in R; commutating current flows through C, SCR_1, L, and D, and the charge on C is reversed and held with the hold-off diode D. At any desired time SCR_2 may be triggered which then places C across SCR_1 via SCR_2 and SCR_1 is turned off.

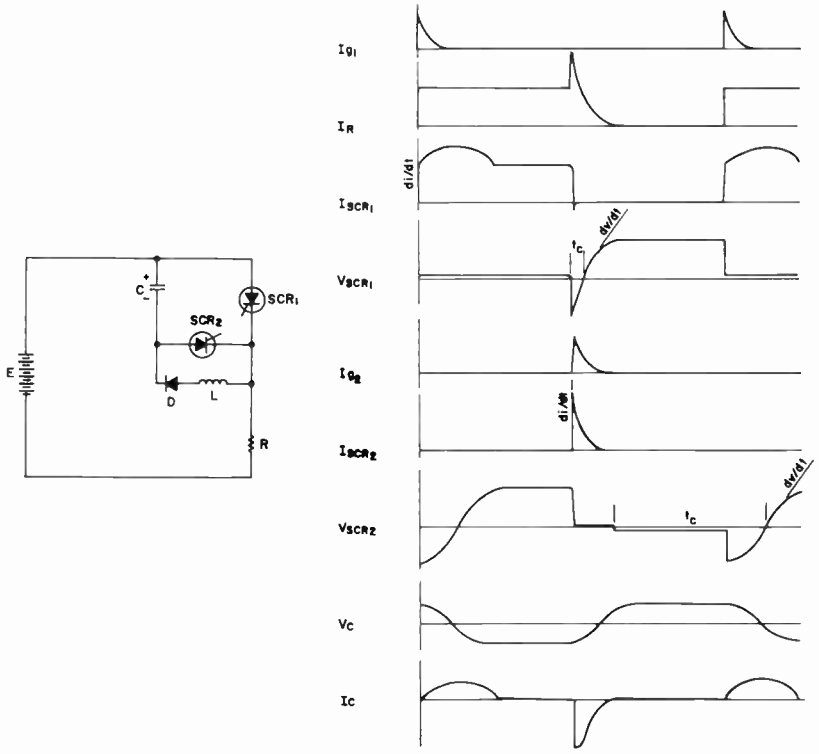


FIGURE 5.9 CLASS D COMMUTATION (EXAMPLE 2)

Class D—LC or C switched by an auxiliary SCR

Example 3—The Jones Circuit

The outstanding feature of this circuit is its ability to start commutating reliably.

If C were discharged, then, on triggering SCR_1, voltage would be induced into L_2 by closely coupled L_1, and C would become charged in the polarity shown. As soon as SCR_2 is triggered, SCR_1 is turned off. C now becomes charged in the opposite polarity.

The next time SCR_1 is triggered, C discharges via SCR_1, and L_2, and its polarity is reversed ready for the next commutating pulse. The voltage to which C is charged (in the polarity shown in Figure 5.10), depends on which is greater: the voltage induced by load current flowing in L_1 or the reversal of the positive charge built up while SCR_2 was conducting.

With heavy loads, the induced voltage increases, thus tending to offset the decrease of turn-off time. Better turn-off times are obtained with this circuit as compared with Example 2 at the cost of higher voltages appearing across the SCR's. This circuit is discussed in more detail in Chapter 11.

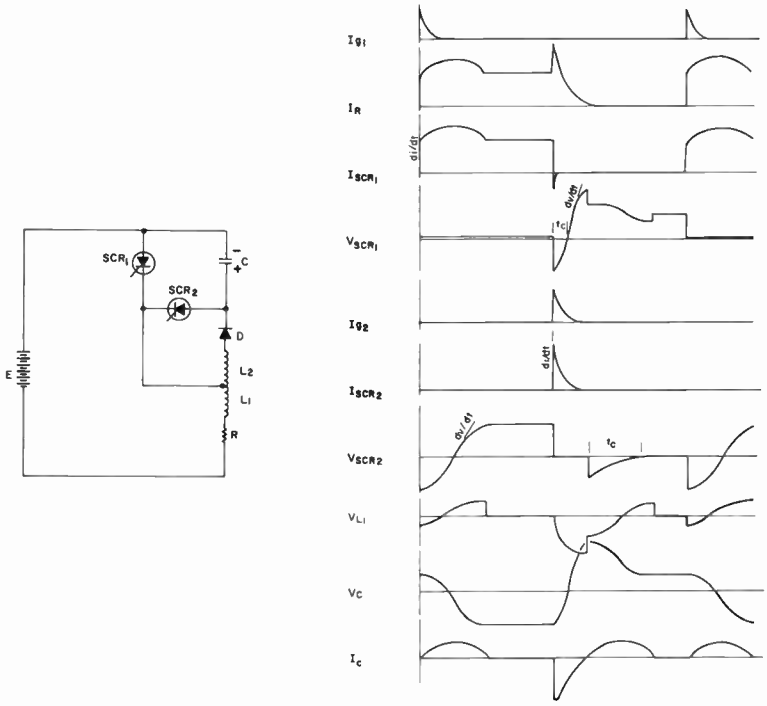


FIGURE 5.10 CLASS D COMMUTATION (EXAMPLE 3)

5.5.5 Class E—External pulse source for commutation

Example 1

When SCR_1 is triggered, current will flow into the load. To turn SCR_1 off base drive is applied to the transistor Q_1. This will connect auxiliary supply E_2 across SCR_1 turning it off. Q_2 is held on for the duration of the turn-off time.

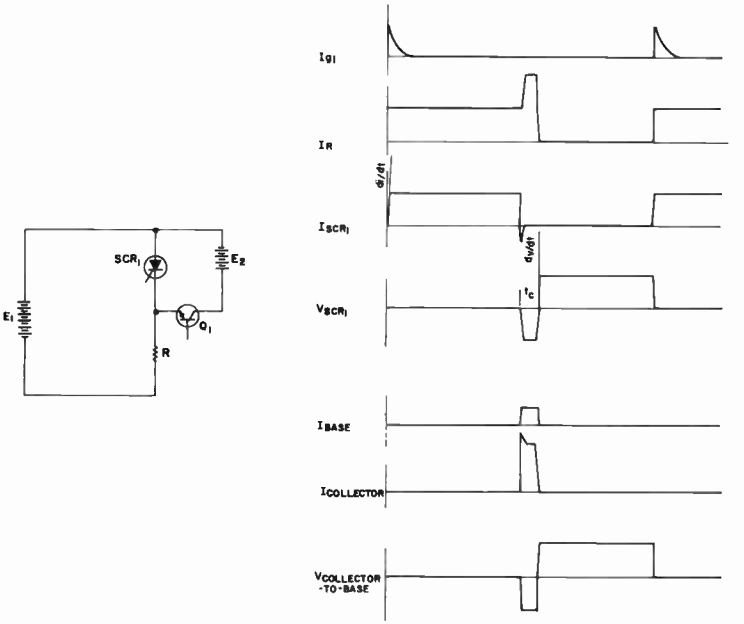


FIGURE 5.11 CLASS E COMMUTATION (EXAMPLE 1)

Class E—External pulse source for commutation

Example 2

The transformer is designed with sufficient iron and air gap so as not to saturate. It is capable of carrying the load current with a small voltage drop compared with the supply voltage.

When SCR_1 is triggered, current flows through the load and pulse transformer. To turn SCR_1 off a positive pulse is applied to the cathode of the SCR from an external pulse generator via the pulse transformer. The capacitor C is only charged to about 1 volt and for the duration of the turn-off pulse it can be considered to have zero impedance. Thus the pulse from the transformer reverses the voltage across the SCR, and it supplies the reverse recovery current and holds the voltage negative for the required turn-off time.

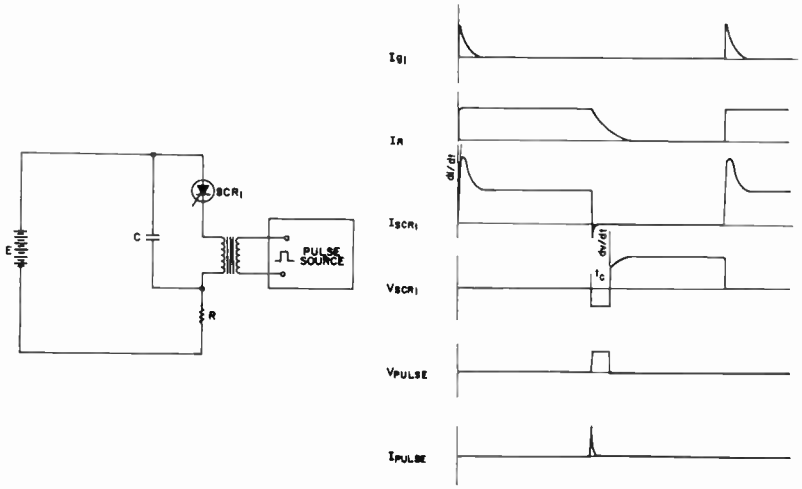


FIGURE 5.12 CLASS E COMMUTATION (EXAMPLE 2)

Class E—External pulse source for commutation

Example 3

When the SCR is turned on, the pulse transformer saturates and presents a low impedance path for the load current. When the time comes for turning off the SCR, the first step is to de-saturate the pulse transformer. This is done by means of a pulse in the polarity shown. This de-saturating pulse momentarily increases the voltage across the load and also the load current. Once the pulse transformer is de-saturated, a pulse in the reverse polarity is injected, reversing the voltage across the SCR and turning it off. The pulse is held for the required turn-off time.

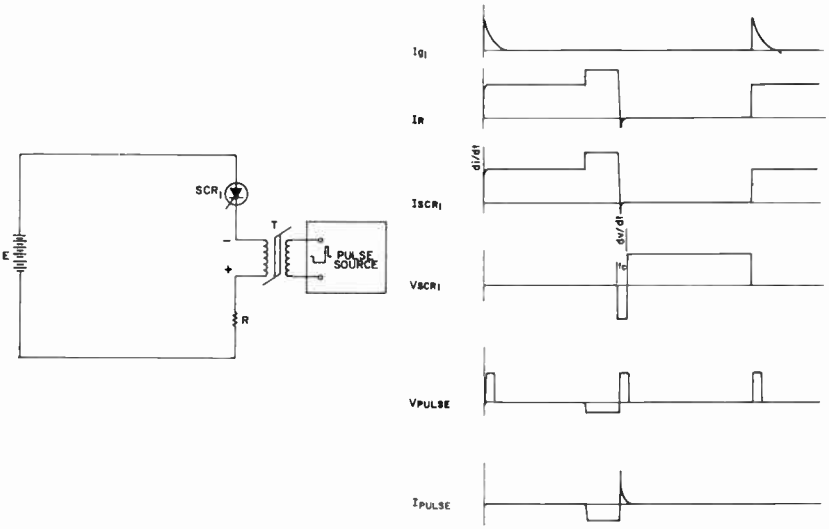


FIGURE 5.13 CLASS E COMMUTATION (EXAMPLE 3)

Class E—External pulse source for commutation

Example 4

This circuit is important because no capacitor-charging pulse flows through the load.

Assume C is charged in the polarity shown to some voltage greater than the supply voltage E. When SCR_1 is triggered, load current flows in R and L_2. SCR_2 is in a resonant circuit consisting of C and L_2. When SCR_2 is triggered, a pulse of current flows through L_2. A voltage is developed across L_2 which is greater than the supply voltage E. Reverse voltage is therefore applied to SCR_1 which turns it off. The termination of the discharge pulse through SCR_2 turns it off, and C is now charged in the opposite polarity. L_1 is much larger than L_2, and C is now resonantly charged via L_1 and D to some voltage greater than the supply voltage.

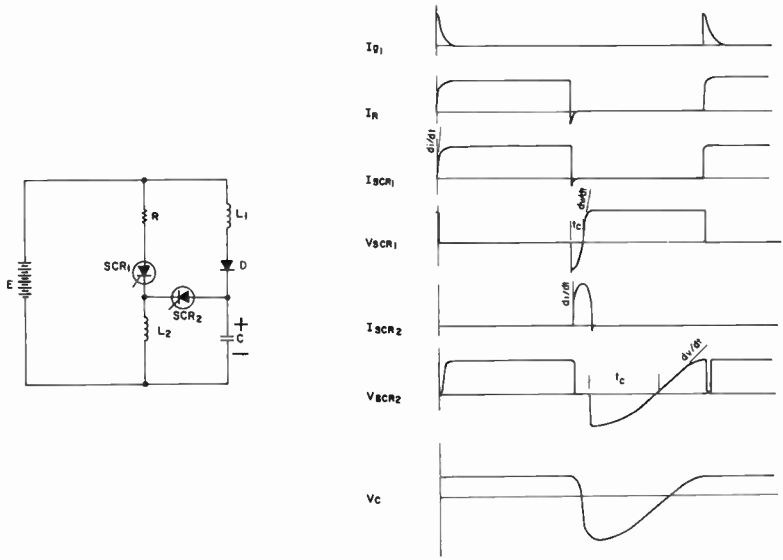


FIGURE 5.14 CLASS E COMMUTATION (EXAMPLE 4)

5.5.6 Class F—AC line commutated

If the supply is an alternating voltage, load current will flow during the positive half cycle. During the negative half cycle the SCR will turn off due to the negative polarity across the SCR. The duration of the half cycle must be longer than the turn-off time of the SCR.

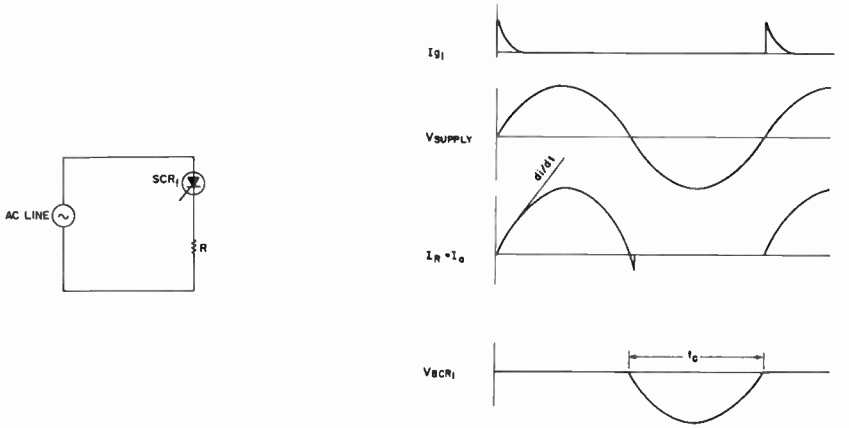


FIGURE 5.15 CLASS F COMMUTATION

5.6 CAPACITORS FOR COMMUTATION CIRCUITS

The capacitors used in the various methods of turning off SCR's need care in their selection and specification. The following properties are desirable:

1. The capacitor life should be long, at the operating ambient temperature, and comparable with that of the SCR.
2. The losses should be low for two reasons:
   a. To avoid high internal temperatures which would shorten the capacitor life.
   b. To maintain the advantage of high efficiency which the SCR gives to the over-all circuit.
3. The capacitor's equivalent series inductance should be known. In many circuits, inductance in series with the commutating capacitor plays an important part in controlling the initial rate of rise of anode current through the SCR.

The equipment designer is advised to take the following steps:

1. For the breadboard, standard inverter capacitors may be purchased from the General Electric Capacitor Department, Hudson Falls, New York. The following extract from the catalog gives the ratings of standard capacitors.

2. After completion of the breadboard tests, the voltage and current waveforms and temperature data should be submitted to the capacitor manufacturer for optimization of life, size, and cost.

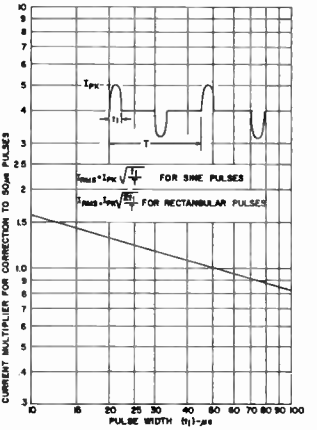


FIGURE 5.16 CURRENT MULTIPLIER FOR CAPACITORS

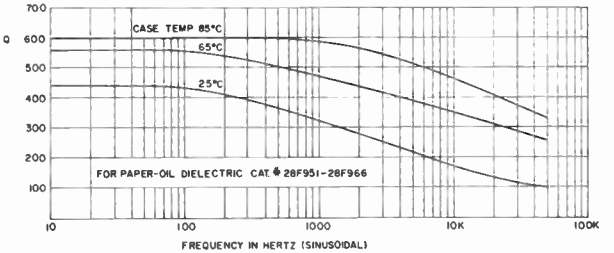


FIGURE 5.17 Q VERSUS FREQUENCY FOR CAPACITORS

TABLE 5.1 Extracts From G-E Capacitor Catalog

RMS Volts AC Max	DC Volts Max	μf ± 10%	Catalog Number	Dielectric	Configuration	Case Base		Case Height	Max RMS Amps at Given Max Temp†			
						Width	Depth		80°C Amb.	70°C Amb.	60°C Amb.	50°C Amb.
									87°C Case	83°C Case	80°C Case	77°C Case
500		8/8/8	17F405		Rect.	8	4	6	30	66	90	120
165	200	3	28F951		Oval	2 5/32	1 5/16	2 5/16	7.0	10.0	12.3	14.2
		5	28F952		Oval	2 5/32	1 5/16	3 1/16	9.8	14.2	17.4	19.9
		10	28F953		Rect.	3 1/4	1 1/4	4 1/4	22.0	31.6	39.5	42.9
		20	28F954		Rect.	3 1/4	2 1/4	4 1/2	38.0	43.0	43.1	43.4
200	250	2	28F955		Oval	2 5/32	1 5/16	2 5/16	5.7	7.9	9.8	11.7
330	600	2	28F956	*	Oval	2 5/32	1 5/16	2 13/16	6.3	8.8	11.0	12.6
		3	28F957	Oil	Oval	2 5/32	1 5/16	3 13/16	8.5	12.3	14.8	17.4
		5	28F958	Impreg-	Rect.	3 1/4	1 1/4	4 3/4	15.8	22.1	28.4	31.6
		10	28F959	nated	Rect.	3 1/4	2 1/4	4 1/2	25.3	37.9	42.9	43.0
		20	28F960	Paper	Rect.	3 1/4	3 3/16	5 1/2	43.0	43.0	43.0	43.0
400	800	1	28F961		Oval	2 5/32	1 5/16	2 5/16	4.1	5.7	6.9	8.2
660	1500	0.5	28F5033		Oval	2 5/32	1 5/16	2 1/16	3.0	4.3	5.6	6.7
700	2000	1	28F962		Oval	2 5/32	1 5/16	4 3/8	5.3	7.2	9.1	10.7
		2	28F963		Rect.	3 1/4	1 1/4	4 3/4	10.7	15.2	18.3	21.2
		3	28F964		Rect.	3 1/4	2 1/4	4 1/2	14.5	20.5	25.3	28.4
		5	28F965		Rect.	3 1/4	3 3/16	5 1/8	22.1	30.6	36.3	42.6
		10	28F966		Rect.	4 1/16	3 3/4	6	36.3	43.0	43.0	43.0
330	600	20	28F1202	§	Oval	3 21/32	1 31/32	6	43	43	43	43
700	2000	10	28F1203	Poly-carbonate	Rect.	4 1/16	3 3/4	5 1/8	43	43	43	43
									Max VA at Given Max Temp			
115		25	28F1101		Oval	2 11/16	1 1/16	2 1/8	33	125	230	350
		50	28F1102	**	Oval	2 11/16	1 1/16	2 7/8	42	160	290	430
		100	28F1103	Metalized	Oval	3 21/32	1 31/32	3 1/8	65	245	440	670
		125	28F1104	Paper	Oval	3 21/32	1 31/32	3 7/8	76	285	520	782

† Based on 50 microseconds current pulse width (t_1). For pulse widths other than 50 microseconds see Fig. 5.16.

* See Fig. 5.17 for Q values. Estimated life for 28F type oil impregnated paper units for 95 percent survival is 40,000 hours, provided temperature, voltage and rms current limitations are adhered to.

§ Loss factor for polycarbonate is generally ten times less than for paper.

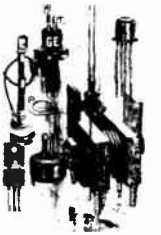
**Peak current must not exceed 10 amps per μf regardless of pulse width.

A check list of the required data for capacitors follows:

1. Capacitance Required:_____ Tolerance (if less than ±10%)_____
2.* Peak Voltage:_____ RMS Voltage:_____
3.* Peak Current:_____ RMS Current:_____
4.* Repetition Rate:_____ Duty Cycle:_____
   (time on—time off)
5. Minimum Q:_____ Series Inductance if other than 0.1 μH ±50%_____
6. Ambient Temperature:_____ Max._____ Min._____
7. Desired Operating Life:_____ (total cycles)
   _____ (total hours)
8. Physical Size Limitations:_____
3. Mounting Requirements:_____
10. Unusual atmospheric conditions: (dust, chemicals, humidity, corrosion, etc.)_____
11. Other special requirements: (high altitude, shock, vibration, etc.)_____
12. What kind cooling available: (fins, heatsink, forced air, etc.)_____

*Show sketch of voltage wave shape vs. time.

6 SERIES AND PARALLEL OPERATION OF SCR'S



6.1 SERIES OPERATION OF SCR's

Since the introduction of the SCR in 1957, its blocking capabilities have been steadily improving. SCR's are today available with rated blocking voltages significantly above 1000 volts. Still, there are numerous applications where a single SCR does not have sufficient blocking capability for the job. Additionally, some specialized SCR's such as high speed inverter types, are somewhat limited in voltage capability. This is done intentionally in order to attain the required high speed characteristics. When circuit requirements dictate operation at higher voltages than can be realized within the blocking capabilities of a single SCR, series combinations can be employed if certain design precautions are taken. These precautions are primarily the equalization of the voltages, both forward and reverse, between individual SCR's.

Little work has been done on series connection of triacs; it appears the guidelines outlined here for SCR's generally apply to triacs.

To date, the triac has been primarily employed in consumer/appliance/light industrial applications where slightly lower cost of trigger circuitry can be an important factor. As requirements for operation from higher source voltages appear, the applications will almost certainly fall in the realm of heavy industrial applications. While cost is important everywhere, performance tends to dominate in heavy industry. Therefore, inverse parallel high-voltage SCR's with their high degree of dynamic capability are in general more appropriate to provide the function of AC switching at higher currents and voltages, and at greater levels of dynamic performance, than are currently available in series/parallel combinations of discrete triac devices.

6.1.1 General

Shown in Fig. 6.1 are hypothetical voltage/current characteristics for two randomly selected SCR's. If the two SCR's are connected in series one might expect them to have a total forward blocking capability of at least 2 (V_2). Yet without forced voltage equalization the total peak forward blocking voltage must be limited to approximately ($V_1 + V_2$) in order to keep the voltage across SCR_2 from exceeding $V_{(BR)F_2}$.

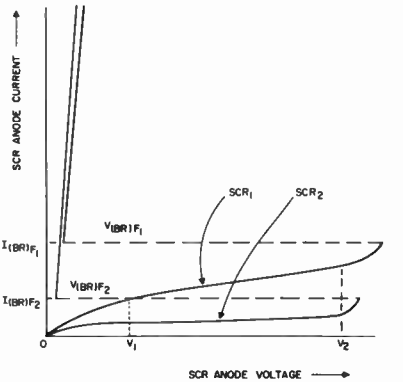


FIGURE 6.1 SCR CHARACTERISTICS

Fig. 6.2 shows, diagramatically, the six operating states that can occur in a random sample of SCR's, connected in series, without forced equalization. It is seen that the equivalent individual impedances change continuously as the SCR series connection switches from state to state.

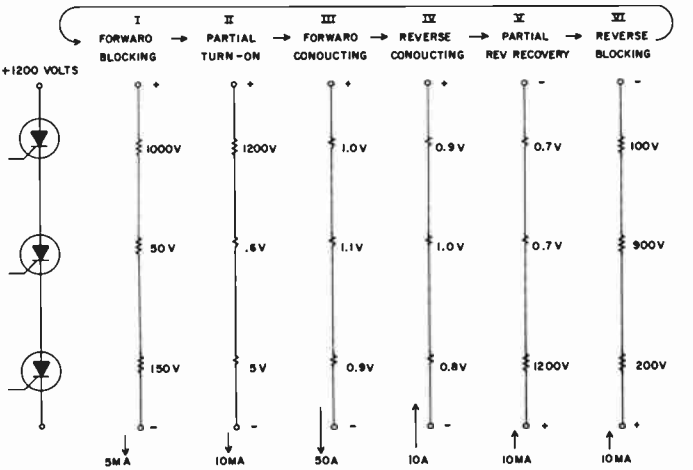


FIGURE 6.2 POSSIBLE OPERATING STATES OF AN UNEQUALIZED SERIES STRING OF SCR'S

During forward and reverse blocking (State I and VI) the differences in blocking characteristics result in unequal voltage sharing. This could be harmful to an SCR with inherently low blocking current since it might cause excessive voltage to appear across that SCR. In order to equalize the blocking voltages a shunt resistor is connected across each SCR. The conducting States (III and IV) represent no problem of voltage equalization.

States II and V shown in Fig. 6.2 represent undesirable conditions since each presents a momentary excessive voltage to at least one SCR. Inasmuch as these states cannot be eliminated, some form of forced voltage sharing during this time is necessary. Voltage can be virtually equalized during State II by simultaneous turn-on of all SCR's (simultaneous triggering). Triggering of series SCR's will be discussed later (See Section 6.1.4.). State V results from the fact that in a randomly chosen series string of SCR's, all SCR's will not recover their reverse blocking ability at the same instant. As soon as the first SCR recovers, the reverse voltage intended for the entire string tends to appear across that one member. To equalize the voltage during this period, a capacitor is connected across each SCR. If the impedance of the capacitor is low enough during the reverse recovery time (a transient phenomenon), the voltage buildup on the fastest SCR to recover is limited until the slowest SCR in the string recovers. Addition of shunt capacitors limits forward voltage rise during turn-on also thus alleviating the undesirable condition of State II.

In summary, States III and IV present no equalization problem. Shunt resistors equalize the voltage during States I and VI. Shunt capacitors equalize the voltage during States II and V. Virtual simultaneous triggering reduces, and all but eliminates, inequalities during State II.

While capacitors provide excellent transient voltage equalization, they also produce high switching currents through the SCR's during the turn-on interval.[1,2] Switching currents can be limited by means of damping resistors

in series with each capacitor. The value of the damping resistors must be kept to a reasonably low value in order not to reduce the effectiveness of the capacitors in equalizing voltage during the reverse recovery time. Also, low values of damping resistance preclude excessive voltage build-up due to the IR drop during flow of reverse recovery current in the series connection after the first SCR has recovered.

Fig. 6.3 shows the voltage equalization scheme described above. Diodes can be placed across the damping resistors R_D to increase the effectiveness of the capacitors in preventing misfiring due to excessive rate of rise of forward voltage on the SCR's. Fast recovery diodes should be employed so that the damping resistors still limit the switching current duty on the SCR's.

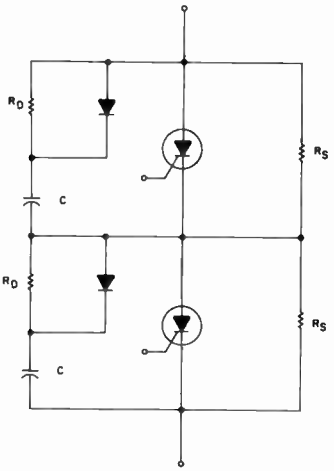


FIGURE 6.3 SERIES EQUALIZING ARRANGEMENT

6.1.2 Equalizing Network Design

6.1.2.1 Selection of Voltage Equalizing Resistors

For any given random group of SCR's there will be a given range of forward and reverse blocking current at given circuit conditions. Naturally, SCR's with low inherent blocking current will assume a greater portion of a steady state blocking voltage than will units with higher blocking current when all are connected in series. If the range of blocking current is defined as

$$I_b(\max) - I_b(\min) = \Delta I_b \qquad (6.1)$$

it is seen that the maximum unbalance in blocking voltage to SCR's of a series string occurs when one member has a blocking current of $I_b(\min)$ and all remaining SCR's have $I_b(\max)$. Fig. 6.4 represents just such a case.

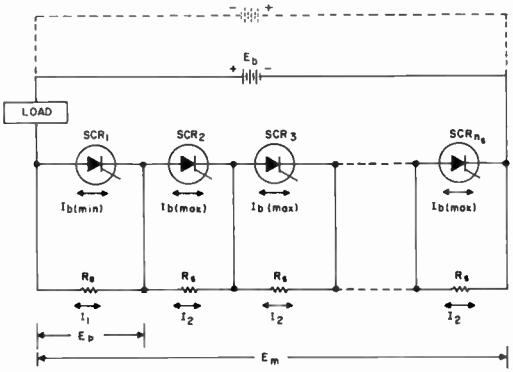


FIGURE 6.4 USE OF SHUNT RESISTORS TO EQUALIZE BLOCKING VOLTAGES TO SERIES SCR'S

Choose E_p as the maximum blocking voltage which we will allow across any one SCR. By inspection $I_1 > I_2$. Therefore:

$$E_p = I_1 R_s$$

Also:

$$E_m = E_p + (n_s - 1) R_s I_2$$

where:

E_m = peak blocking voltage to entire series string
n_s = number of SCR's in series string
$I_2 = I_1 - \Delta I_b$

$$E_m = E_p + (n_s - 1) R_s (I_1 - \Delta I_b)$$
$$= n_s E_p - (n_s - 1) R_s \Delta I_b$$

Now:

$$R_s \leq \frac{n_s E_p - E_m}{(n_s - 1) \Delta I_b} \qquad (6.2)$$

In general, only the maximum blocking currents for a particular SCR type are provided by the manufacturer. If one wishes to be conservative, I_b(min) can be assumed to be zero. The required value for R_s then becomes

$$R_s \leq \frac{n_s E_p - E_m}{(n_s - 1) I_b(\max)} \qquad (6.3)$$

Equalization resistors represent power consumers and as such it is desirable to use as large a resistance as possible. In a given group of SCR's, chances are good that one can select ΔI_b to be considerably less than I_b(max). For this reason the ΔI_b approach is recommended. When determining ΔI_b, it is best to measure blocking currents at maximum rated junction temperature and blocking voltage. After ΔI_b groups are selected, the ΔI_b should be checked at 25°C. To allow for differences in SCR temperatures when operating, a safety factor on ΔI_b should be used for design purposes.

Up to this point nothing has been said whether one must consider forward or reverse blocking current, or both. In general an SCR specification sheet gives one figure to cover both forward and reverse blocking current; when both are specified, they are usually the same. In general one would want to design around the larger of the blocking currents. More often than

not the forward blocking current is slightly higher than reverse. One would generally be safe using $\Delta I_b = \Delta I_{FOM}$ When using the conservative approach one must use $\Delta I_b = I_{FOM}$ from the SCR specification sheet, not $I_{FX(AV)}$, the full cycle average.

Figure 6.5 is a useful aid for finding the required voltage equalizing resistance for series strings up to eight SCR's long. Enter the chart with a known E_m/E_p and read up to the curve designating the number of SCR's per string. Read across to find $\frac{R_s}{E_m/\Delta I_b}$. With a knowledge of E_m and ΔI_b, determine R_s(max).

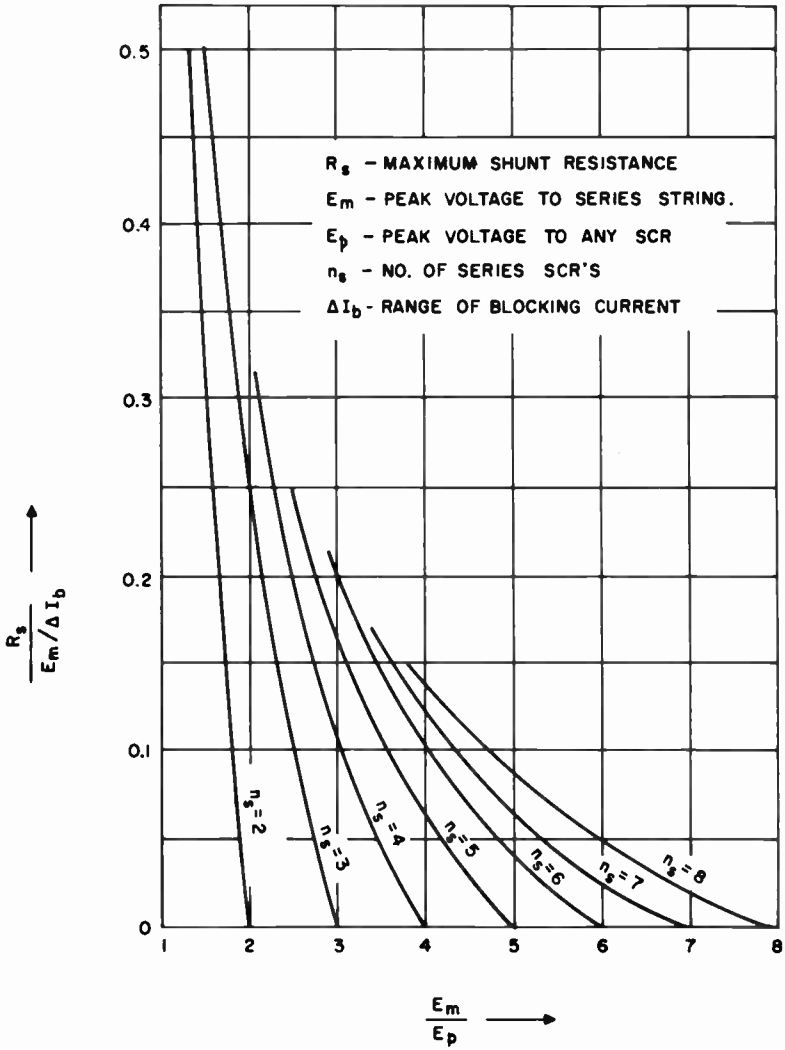
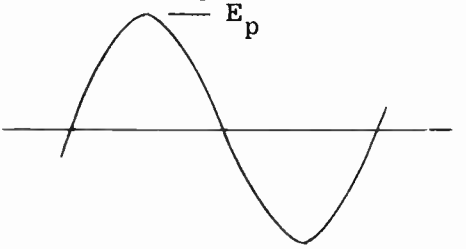


FIGURE 6.5 VOLTAGE EQUALIZING RESISTANCE FOR SERIES OPERATION OF SCR'S

To determine the power rating of the shunt resistors one must consider the resistor which experiences the highest peak voltage. The resistor power dissipation can be expressed as:

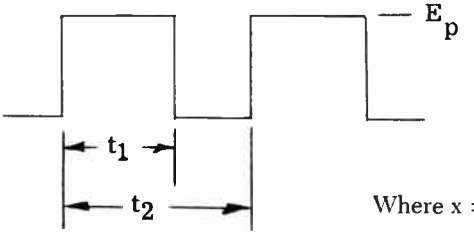
$$P_D = \frac{(E_{RMS})^2}{R_s} \tag{6.4}$$

For phase control applications the maximum power dissipation occurs at zero conduction angle:



$$P_D = \frac{E_p^2}{2R_s} \tag{6.5}$$

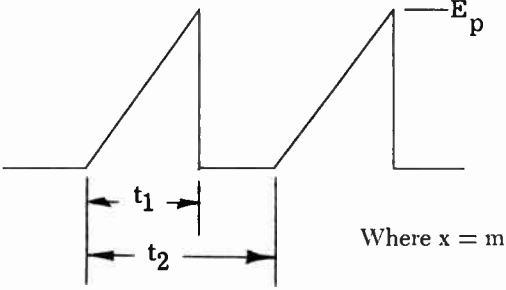
For square wave inverter or chopper:



$$P_D = \frac{x\,E_p^2}{R_s} \tag{6.6}$$

Where x = maximum blocking duty cycle (t_1/t_2)

For sawtooth wave:



$$P_D = \frac{E_p^2\,x}{3R_s} \tag{6.7}$$

Where x = maximum blocking duty cycle (t_1/t_2)

6.1.2.2 Selection of Shunt Capacitors

As mentioned earlier, shunt capacitors are required to limit rate of rise of voltage on the SCR's. Also during the reverse recovery interval such capacitors provide a reverse recovery current path for slow SCR's around those SCR's which recover first. Since the problem we are trying to correct arises from a difference in recovery characteristics within a given type of SCR we must take some time to discuss this characteristic.[4] The reverse recovery phenomenon in an SCR results from an attempt to place reverse voltage to the device while it is in the forward conducting condition. There is a period of time between the application of reverse voltage to the SCR and the assumption of such by the SCR. The time period between crossover from forward to reverse

current and the point where reverse current has decayed to 10% of the peak value is defined as reverse recovery time. In those cases observed to date it has been found that SCR's exhibit the triangular reverse current characteristic as shown in Figure 6.6. Empirically it has been found that $t_s \cong 0.6\ t_{rr}$ for a number of different commutating conditions.

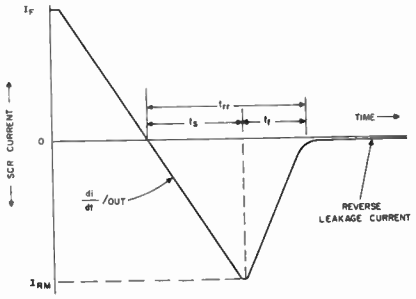


FIGURE 6.6 TYPICAL SCR REVERSE RECOVERY CURRENT

The time integral of the current over the period t_{rr} is the total recovered charge. The recovered charge as we speak of it here is a portion of the total stored at the junction and throughout the bulk of the pellet during forward conduction. If natural recombination of electrons and holes was negligible during t_{rr}, then all the stored charge would be recovered. In those semiconductor devices such as some diodes which exhibit a "snap-off" characteristic, the time period t_f essentially does not exist. So far as has been observed, SCR's do not have a severe snap characteristic.

Two SCR's with a sizeable difference in reverse recovery current are depicted in Figure 6.7. The difference in the enclosed area is the differential charge (designated ΔQ).

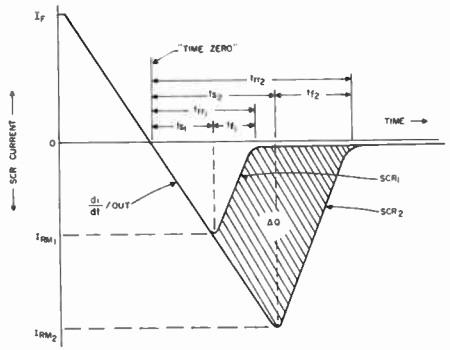


FIGURE 6.7 REVERSE RECOVERY CURRENTS FOR TWO UNMATCHED SCR'S OF THE SAME TYPE

Note that Figure 6.7 shows $t_{s2} > t_{rr1}$. This will not necessarily be true for two randomly chosen SCR's. However if one has two SCR's which represent the limit cases for a given type (i.e. worst case reverse recovery mismatch) then t_{s2} is generally greater than t_{rr1}. For design purposes this is a valid assumption.

Figure 6.8 shows current and voltage waveforms, during the reverse recovery interval, for two mismatched, series connected SCR's with shunt capacitors. The commutation interval begins when forward current begins to decrease abruptly.

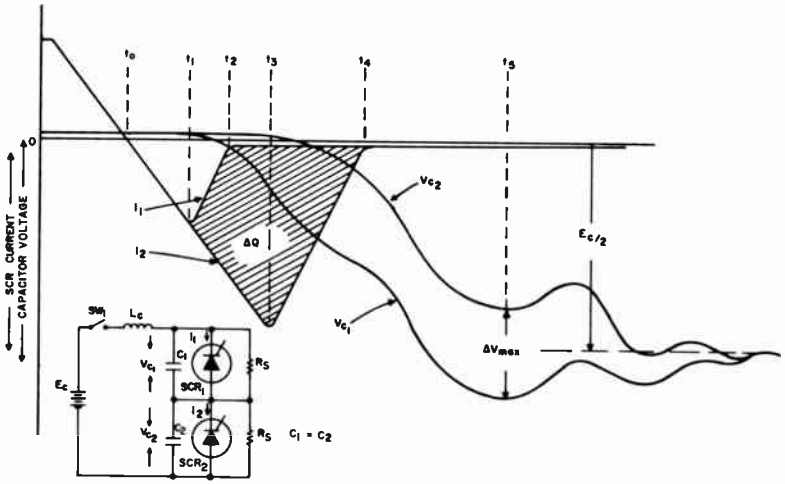


FIGURE 6.8 RECOVERY VOLTAGES OF CAPACITORS SHUNTING MISMATCHED, SERIES CONNECTED SCR'S

From t_0 to t_1 both SCR's present a short circuit to the flow of reverse current. Reverse current is applied at a rate determined by the commutating voltage E_c and the circuit commutating reactance L_c. During the period t_1 to t_2, capacitor C_1 begins to charge as SCR_1 begins to regain its blocking capability. The rate of charge of C_1 increases during this interval as the current in SCR_1 "tails-off." From t_2 to t_3 SCR_1 has fully recovered. The voltage and rate of charging C_1 further increases due to the increasing reverse current in SCR_2. At t_3, SCR_2 begins to recover and the current through SCR_2 begins to decrease thus reducing the charging rate of C_1. C_2 begins to charge as soon as SCR_2 begins to regain its blocking ability. At time t_4 both SCR's are fully recovered so that the only current path is through the capacitors. This means that at time t_4 the slopes of the voltage waveforms must be equal. From time t_4 on, the circuit behaves as a simple LC circuit (C being a series combination of n discrete capacitors). Due to the difference in SCR recovery characteristics, the shunt capacitors when charged to peak voltage are not charged equally. The maximum difference in voltage is designated as ΔV_{max}. This ΔV_{max} can be simply represented by

$$\Delta V_{max} = \frac{\Delta Q_{max}}{C_x} \qquad (6.8)$$

$$x = 1, 2, 3 \ldots . n$$

For steady state reverse blocking the shunt resistors share voltage to the designed degree. In Figure 6.8, the voltage difference between the two shunt capacitors varies from ΔV_{max} at t_5 to that determined by the shunt resistors at some time later than t_5. Assuming that the resistors share the steady state reverse voltage perfectly, ΔV after t_5 can be represented by:

$$\Delta V = \Delta V_{max} \epsilon^{-[t/R_s C]} \quad (6.9)$$

(time zero at t_5)

The worst combination of recovery characteristics for a series string of SCR's is with one fast recovery SCR and all the remaining ones being the slowest of that type. In this situation the peak voltages across the shunt capacitors are as follows:

$$V_{c'} \text{ (fast SCR)} = (1/n_s)\,[E_{c'} + (n_s - 1)\,\Delta V_{max}] \quad (6.10)$$

$$V_{c'} \text{ (slow SCR)} = (1/n_s)\,(E_{c'} - \Delta V_{max})$$

Using relationships (6.8) and (6.10) and setting $V_{c'}$ (fast SCR) $= E_p$

$$C \geq \frac{(n_s - 1)\,\Delta Q_{max}}{n_s E_p - E_{c'}} \quad (6.11)$$

One might say: "This relationship for C is fine but how do I find ΔQ_{max} for a given type of SCR"? As of this writing no such thing as a ΔQ is specified for SCR's. Following is a table of typical spread of ΔQ for some General Electric SCR types.

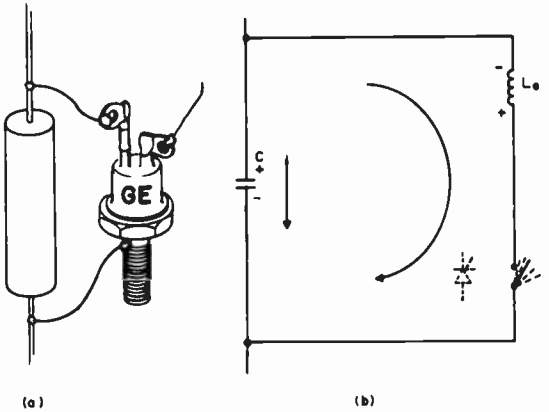
TABLE 6.1 Typical Recovered Charge for Some SCR Types

SCR Line	C10	C20	C35	C30	C140	C135
Related SCR Types	C11 C12 C15	C22	C36 C37 C38 C40	C31 C32 C33	C141	
ΔQ_{max} (μ coulombs)	10	12	20	40	4	35

($T_j = 25°C$)

Recovered charge is a function of commutation conditions. It is interesting to note that although the magnitudes of recovered charge vary with conditions at $T_j = 25°C$, for high reverse dI_f/dt, ΔQ remains relatively constant as conditions vary. The values for ΔQ shown in Table 6.1 are for rated forward currents and high rates of rise of reverse current. For this reason commutating conditions have not been attached to Table 6.1. For light commutating conditions where, due to natural recombination, not all charge is recovered, actual ΔQ_{max} will be less than that given in the table. ΔQ_{max} increases modestly with junction temperature. An *approximate* temperature coefficient for ΔQ_{max} is $+0.2\%/°C$.

Note that up to this point we have talked about voltages across the capacitors and tacitly assumed that such voltages are those on the SCR's. In practice this is usually not true. As shown in Figure 6.9 a certain amount of stray inductance is found in the physical capacitor-SCR loop.



(a) (b)

FIGURE 6.9 STRAY INDUCTANCE OF SCR-CAPACITOR LOOP

During the period t_f (Figure 6.6), current is changing in such a fashion as to set up a voltage in the stray inductance as shown. Realizing that this inductance is composed of wiring inductance, capacitor inductance and that inherent in the SCR, it is not hard to visualize, say, 1 μh in the loop. The induced voltage as shown represents additional reverse voltage to the SCR. During t_f the current can be changing at the rate of 200 amperes per microsecond when the commutation conditions are severe. This (with 1 μh) would mean an additional 200 volts reverse to the SCR. It cannot be overemphasized that the inductance of the capacitor-SCR loop should be held to as low a value as possible.

Since the shunt capacitors discharge through the SCR's during turn-on, it is necessary to insert a small amount of resistance in series with each capacitor. The value of the resistance is chosen to limit the discharge current within the turn-on current limit of the SCR. Usually, the required value of resistance will fall between 5 and 50 ohms. In addition to limiting capacitor discharge current, high frequency oscillations due to interaction between the capacitors and circuit inductance are suppressed. It must be remembered that, although the damping resistance must be large enough to limit turn-on current, it must not be so large that it either destroys the effect of the shunt capacitors or establishes an excessively high voltage during flow of reverse recovery current through it.

6.1.3 Other Voltage Equalizing Arrangements

The arrangement of Figure 6.3 provides voltage sharing under all conditions of forward and reverse blocking. In applications where the increase in blocking losses due to current through the equalizing resistors must be avoided, as in SCR radar modulator switches, voltage sharing may be successfully accomplished by replacing each shunt equalizing network with a silicon controlled avalanche rectifier as shown in Figure 6.10(a). When maximum avalanche voltage is chosen correctly, total forward blocking current through the circuit need be only slightly higher than the maximum blocking current of the worst SCR. Maximum avalanche voltage of the shunt rectifier should be equal to, or slightly below, the SCR forward breakover voltage

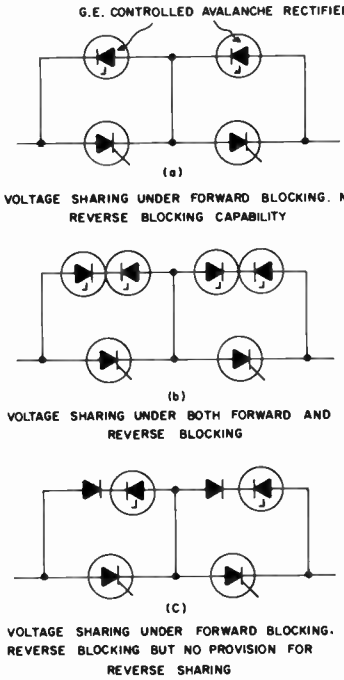


FIGURE 6.10 SERIES EQUALIZING ARRANGEMENTS USING CONTROLLED AVALANCHE RECTIFIERS

specification. Minimum avalanche voltage must be higher than E_m/n_s when measured at the controlled avalanche rectifier's minimum operating temperature. To provide optimum equalization it is desirable to have as narrow a tolerance as possible on the avalanche voltage of the shunt rectifier. Where a series string has to block appreciable reverse as well as forward voltage, inverse series controlled avalanche rectifiers may be substituted for the single units (see Figure 6.10(b)). In cases where reverse blocking requirements are not severe, some reverse blocking ability can be obtained using controlled avalanche rectifiers and conventional silicon rectifiers arranged as in Figure 6.10(c).

6.1.4 Triggering Series Operated SCR's

There are two primary methods in common use for triggering series SCR's, namely:

1. Simultaneous triggering;
2. Slave triggering whereby one "master" SCR is triggered, and as its forward blocking voltage begins to collapse, a gate signal is thereby applied to the "slave" SCR.

Simultaneous triggering of all SCR gates is the preferred method. Slave triggering, while it is a unique way to provide gate isolation, produces some time delay between master and slave. Fortunately the capacitors used for

voltage equalization during the reverse recovery period also limit the forward voltage rise. As long as the shunt capacitance is sufficient to limit forward voltage within the PFV ratings of the SCR's until all SCR's are "on," slave triggering can be reliably employed. The designer is cautioned to observe gate drive requirements of the SCR when employing slave triggering, particularly if switching into a fast rising anode current.

6.1.4.1 Simultaneous Triggering Via Pulse Transformer

When using pulse transformers particular attention should be given to the insulation between windings. This insulation must be able to support at least the peak of the supply voltage.

Triggering requirements may differ quite widely between individual SCR's. To prevent a cell with a low impedance gate characteristic from shunting the trigger signal away from a cell with a high impedance gate characteristic, resistance should be inserted in each gate lead, or impedance built into the transformer via leakage reactance.

Where the total energy available to trigger is limited, as may well be the case in a pulse triggering arrangement, it is preferable to replace these resistors with capacitors in series with each gate lead. Series capacitors tend to equalize the charge coupled to each SCR gate during trigger pulses, thus reducing the effects of unequal loading without additional energy dissipation. When capacitors are used in this manner a resistor should be connected from gate to cathode of each SCR to provide a discharge path for the capacitor. The circuit must be able to pass a fast rise time pulse, preferably less than 1 μsecond.

It must be emphasized again that marginal triggering is discouraged. Most SCR specification sheets today show a preferred triggering area on the gate characteristics curve. Particularly when switching into high currents, operation below this preferred area can be disastrous.

6.1.4.2 Simultaneous Triggering by Means of Light

Figure 6.11 shows an approach whereby simultaneous triggering of series connected SCR's is achieved by triggering LASCR's[8] in the gate circuit of each SCR. This method of triggering provides the required gate isolation along with simultaneous turn-on when a single light source is used to turn on all LASCR's. The series combination of R_1 and R_2 is made equal to the required shunt resistance R_s. R_2 is made fairly small compared to R_1 so that low voltage LASCR's can be employed. The R_1C_1 time constant must be made sufficiently small so that C_1 is fully charged to the voltage dictated by R_2 at turn-on. Resistor R_4 limits the peak gate current. A useful trigger circuit (for LASCR's) employing Xenon flashtubes[10] is shown in Figure 6.12. The circuit as shown operates well in the 60-400 Hz frequency range. The unijunction transistor relaxation oscillator provides alternate trigger pulses to the two C5 SCR's. As the C5 SCR's turn-on, the .22 μf capacitors discharge into the primaries of the high voltage trigger transformers thus providing approximately a 6 KV pulse at the flashtube. As the Xenon is ionized by this high voltage pulse the flashtubes conduct and emit a pulse of light.

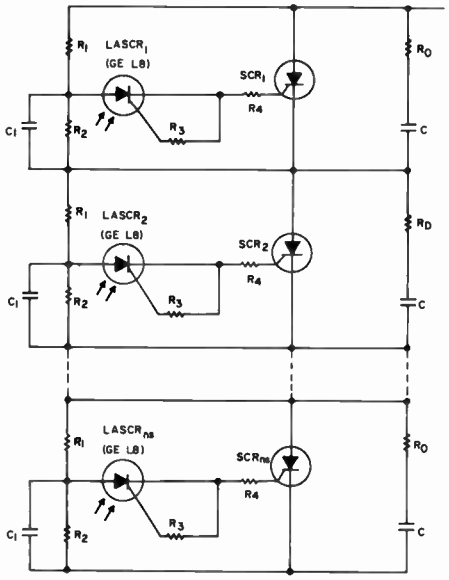


FIGURE 6.11 TRIGGERING OF SERIES CONNECTED SCR'S WITH LIGHT

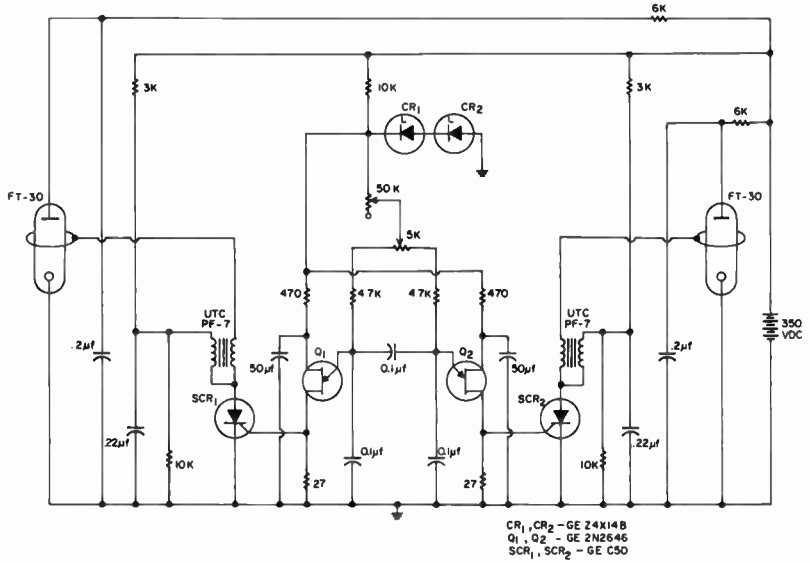


FIGURE 6.12 TRIGGER CIRCUIT FOR LIGHT TRIGGERING OF SERIES SCR'S

6.1.4.3 Slave Triggering for Series SCR's

Slave triggering is a technique for obtaining turn-on of more than one SCR by applying a trigger signal to only one SCR.[3,6] This approach, although a simple one to implement, has a rather serious limitation. Rather than simul-

taneous turn-on, one obtains staggered triggering so that total turn-on-time can be many times that of a single SCR. After the first few SCR's of a series string turn-on, the forward blocking voltage intended for the entire string must be supported by those units which have not yet switched. If the forward voltage to any one SCR exceeds its PFV rating, permanent damage to the SCR may result. The use of shunt capacitors tends to limit the rate of rise of forward voltage on the later SCR's to switch.

Figure 6.13 illustrates a slave triggering technique. A voltage equalizing network as previously described is connected across the cells. Only SCR_1 is directly triggered by the pulse source. The gate of SCR_2 is triggered by the surge of discharge current from capacitor C_1 when the voltage across SCR_1 decreases abruptly as it switches into conduction. Since the capacitor-resistor shunts, in conjunction with the SCR's present a balanced bridge to the zener, the triggering circuit to the SCR's is essentially insensitive to ordinary cyclical variations and transients from the supply voltage. In many cases the equalization network, optimized according to the procedure described earlier, will supply the required gate current to trigger. Rectifiers CR_2 and CR_3 can be paralleled with the damping resistors to inhibit triggering from dv/dt of the line voltage.

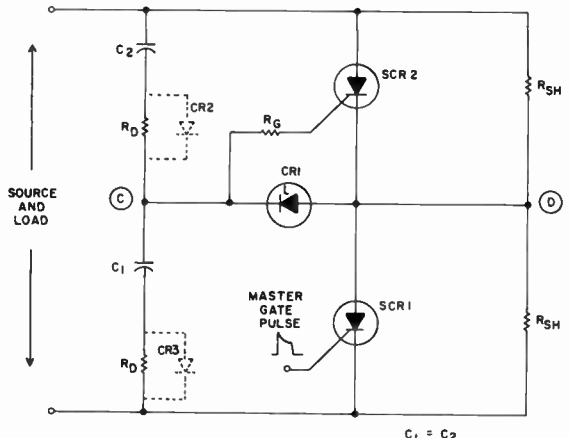


FIGURE 6.13 SERIES OPERATION OF SCR'S USING SLAVE TRIGGERING

The minimum capacitance required to supply sufficient gate current to trigger under all conditions is given by:

$$C_1 \geqq \frac{10}{R_G + \dfrac{V_{GT(max)}}{I_{GT(max)}}} \ \mu\text{fd} \tag{6.12}$$

and

$$R_G = \frac{(V_z/2.7) - V_{GT(max)}}{I_{GT(max)}} \text{ ohms} \tag{6.13}$$

where V_z = nominal zener breakdown voltage of CR_1 (volts)

$I_{GT(max)}$ = maximum gate current to trigger under any of the circuit's operating conditions (milliamps)

$V_{GT(max)}$ = maximum gate voltage to trigger at $I_{GT(max)}$ (volts)

It is necessary that points C and D of Figure 6.13 be as closely balanced as possible. This is to prevent the flow of current in the bridge due to normal cyclical and transient variations of the supply voltage. Depending on the direction of an unbalance, a positive gate current to SCR_2 can result from either a falling or rising supply voltage. The slave triggering technique of Figure 6.13 is expandable to more than two SCR's in series.

Figure 6.14 shows another method of slave triggering series connected SCR's. Capacitors C_1, C_2 . . . C_n serve a dual purpose in this configuration. First, they provide transient voltage equalization and secondly they provide the slave triggering current at turn-on. As SCR_1 is triggered by the master signal, it begins to discharge capacitor C_1 through the gate of SCR_2 thus triggering SCR_2. As SCR_2 turns on capacitor C_2 begins to discharge through the gate of SCR_3, and so on. Resistors R_1, R_2 . . . R_{n-1} limit the SCR gate currents. Resistor R_n limits the di/dt to SCR_n. Figure 6.15 shows what overvoltage can be expected at each SCR during the turn-on interval when employing slave triggering. Overvoltage as used here is a percentage of E_p.

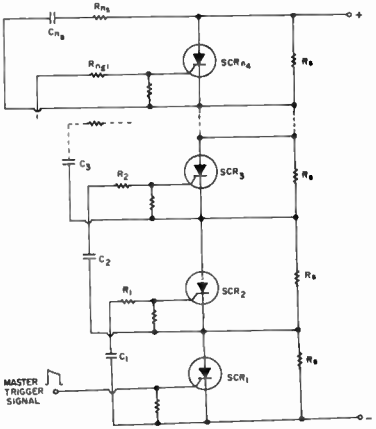


FIGURE 6.14 SLAVE TRIGGERING OF SERIES CONNECTED SCR'S

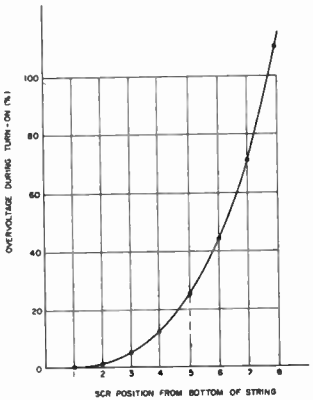


FIGURE 6.15 SCR OVERVOLTAGE AT TURN-ON WHEN SLAVE TRIGGERED VS SCR POSITION IN STRING

6.1.4.4 The Triggering Pulse

For series operation it is imperative to operate the gate well beyond the locus of minimum triggering (see Figure 4.12) in order to obtain turn-on in the minimum possible time. In addition, the pulse should have a very steep rise (ideally about 100 nanoseconds). The width of the pulse should be sufficient to insure that the SCR will latch into conduction under all operating conditions. If anode current swings momentarily to zero during the conducting cycle, the gate pulse must be maintained over the entire conduction period. The amplitude of the gate pulse should be the maximum permissible within the average and peak gate power dissipation ratings of the SCR.

6.2 PARALLEL OPERATION OF SCR's

With the advent of higher current SCR's in the early 1960's the need for parallel combinations of SCR's appeared to diminish. It was (and is) a rare case when it was more economical for an equipment designer to parallel smaller devices rather than use one large SCR for a given current requirement. Of course, when the requirement for special electrical characteristics only available in smaller SCR's are paramount, then there is no alternative but to parallel. More will be said on this subject later in this chapter (see Section 6.2.5).

Now, in the latter 1960's, current carrying requirements for SCR's appear to be out-running those available with a single silicon crystal. Again we are looking at parallel operation of cells for very high current applications using large crystal building blocks.

The main design consideration for operating SCR's in parallel is the equalization of forward current through the parallel paths. When paralleling low resistance elements, variations in the magnetic flux linked by the parallel circuits can often be the most significant cause of unequal current balance. In SCR circuits, this general situation is aggravated by non-uniformity between the SCR forward characteristics.

As regards parallel operation of triacs, a similar philosophy as that outlined under Section 6.1 is suggested; that is, for higher current triac applications, inverse parallel arrangements of high current SCR's are suggested rather than parallel arrangements of triacs.

6.2.1 Current Unbalance Due to External Circuitry

When forced current sharing is not employed, particular care must be taken to assure that impedance in series with each individual parallel path is maintained as nearly equal as possible. Wiring and connections should be uniform in all respects. The tendency for current to crowd to the outer branches or paths of a parallel network due to reactive effects is of particular significance at higher frequencies, and during the switching interval at the beginning and end of each conduction period. Mutual and self-inductance in series with each parallel path should be equalized where this phenomenon poses a problem.[14]

6.2.2 Current Unbalance Due to Differences in SCR Forward Characteristics

There are two primary methods of minimizing current unbalance due to the differences in SCR characteristics. One is to reduce these differences by using SCR's with matched characteristics in the conduction region and the other is to employ forced current sharing by external means.

6.2.2.1 Use of Standard SCR's with no Externally Forced Current Sharing

The method used to parallel standard SCR's with unmatched forward characteristics is best described by an example design problem. We shall assume that our current carrying requirement is in excess of the capability of General Electric's largest stud or flat-base package SCR's at this writing; namely the type C290/C291 SCR.

Assume we have a three phase waveform. What average current can two unmatched C291 type SCR's handle? Begin by assuming that the SCR with the lowest V_F (call this device SCR_1) will be allowed to run at maximum rated junction temperature and maximum allowable RMS current. For the type C291 SCR this is 125°C and 470 amperes respectively. For three phase operation we shall assume a rectangular current waveshape of 0.333 duty cycle. The RMS value for a rectangular waveshape is given by the following relationship

$$I_{RMS} = I_{PK} \sqrt{\text{Duty Cycle}} \tag{6.14}$$

For the type C291 SCR in a three phase circuit:

$$470 = I_{PK} \cdot \sqrt{0.333}$$
$$I_{PK} = 815 \text{ amperes}$$

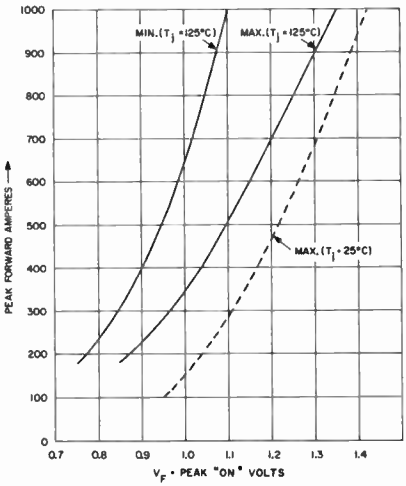


FIGURE 6.16—FORWARD CHARACTERISTICS TYPE C290/291 SCR

During the "on" portion of the cycle, SCR_1 may conduct 815 amperes. Remember that SCR_1 takes a disproportionate share of the total current. This is the SCR with the lowest forward voltage drop at a given current and temperature among the SCR's of that type connected in parallel. SCR_1 is represented by the curve designated "min (T_j = 125°C)" in Figure 6.16. From this curve we may calculate the power dissipation in SCR_1 when conducting at maximum allowable junction temperature.

$$P_{diss(SCR_1)} = (I_{PK})\, V_{FM}\, (\text{Duty Cycle}) \qquad (6.15)$$
$$= (815)\,(1.05)\,(0.333) = 290 \text{ watts}$$

The problem now is to find *how little* current other SCR's in the cluster will conduct. As we have seen, the forward drop across the parallel combination must go no higher than that permitted by SCR_1 when conducting maximum RMS current at maximum rated junction temperature. For our assumed example this was 1.05 volts. Note now that two *maximum* forward voltage drop curves are shown in Figure 6.16; one at T_j = 125°C and one at T_j = 25°C. A common heat exchanger for paralleled SCR's is desirable from the standpoint of thermal stability between SCR's. Let's assume we are following this suggested practice. This means that the temperature of the heat exchanger surface to which the SCR's are mounted can be assumed to be at one temperature for all devices. With SCR_1 running at maximum rated junction temperature it follows that high-forward-drop units will be running at considerably cooler junction temperatures since they are conducting less current and hence dissipating less power. It is seen that the lower the junction temperature the less the current conducted at the forward voltage drop determined by SCR_1. Naturally, use of the T_j = 25°C curve will give an ultra-

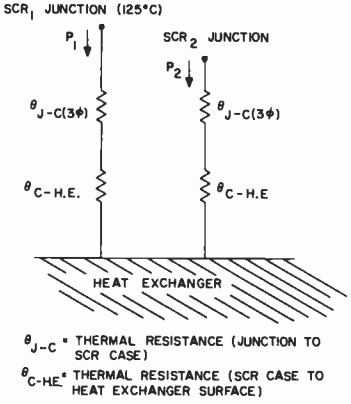


FIGURE 6.17 THERMAL PATHS—UNMATCHED PARALLEL CONNECTED SCR'S

conservative estimate of the mismatch between units. Conversely, use of the T_j = 125°C curve is inappropriate since it makes the degree of mismatch look better than it really may be. We must estimate at what temperature the junction of this device is operating and then check our estimate.

Assume, as an arbitrary starting point, that T_j = 75°C. Find the point (Figure 6.16) where V_F = 1.05 and is midway between the T_j = 125°C and T_j = 25°C. We see that this occurs at a current of 320 amps.

First we calculate at what temperature we must hold the surface of the heat exchanger on which the SCR's are mounted. This is done from a knowledge of the power dissipated in SCR_1 and the maximum thermal resistance from junction to heat exchanger surface. Figure 6.17 shows the thermal circuits for the two parallel SCR's of our problem. In order to find the lowest temperature at which the heat exchanger surface must be held, we use maximum thermal resistance ($\Theta_{J\text{-}C}$ and $\Theta_{C\text{-}H.E.}$). For SCR type C291

$$\Theta_{J\text{-}C(3\,\phi)} = 0.138^\circ C/\text{watt (maximum)}$$
$$\Theta_{C\text{-}H.E.} = 0.08^\circ C/\text{watt (maximum—for a properly mounted SCR)}$$

J—Junction
C—Case
H.E.—Heat Exchanger

$$T_j - T_{H.E.} = [P_{diss(SCR_1)}] \times [\Theta_{J\text{-}C(3\,\phi)} + \Theta_{C\text{-}H.E.}]$$
$$125^\circ C - T_{H.E.} = 290\,(0.138 + 0.08)$$
$$= 290\,(0.218)$$
$$T_{H.E.} = 125^\circ C - 63^\circ C$$
$$= 62^\circ C$$

We see immediately that the junction temperature of SCR_2 will be higher than 62°C. We are interested in finding the lowest temperature any type C291 SCR will run.

The power dissipation in SCR_2 is

$$P_{diss(SCR_2)} = (320)\,(1.05)\,(0.333)$$
$$= 110 \text{ watts}$$

In order to get the lowest probable junction temperature we must use minimum thermal resistances. Usually, minimum thermal resistances are not given on specification sheets. For the type C291 SCR the following thermal resistances may be considered as minimum values.

$$\Theta_{J\text{-}C(1\,\phi)} = 0.09^\circ C/\text{watt}$$
$$\Theta_{J\text{-}C(1\,\phi)} = 0.10^\circ C/\text{watt}$$
$$\Theta_{J\text{-}C(3\,\phi)} = 0.11^\circ C/\text{watt}$$
$$\Theta_{C\text{-}H.E.} = 0.04^\circ C/\text{watt}$$

We can now compute the junction temperature of SCR_2.

$$T_j - T_{H.E.} = P_{diss(SCR_2)} \times (\Theta_{J\text{-}C(3\,\phi)}\,(\text{min}) + \Theta_{C\text{-}H.E.}\,(\text{min}))$$
$$T_j - 62^\circ C = 110 \times (0.11 + 0.04)$$
$$= 16$$
$$T_j = 78^\circ C$$

We see now that our first guess of $T_j = 75^\circ C$ was a pretty good one and no further calculation is necessary. Naturally if our assumption did not correlate with the answer, a new assumption and interpolation would be necessary.

We can now formulate a general relationship for the maximum three phase average current that a parallel group of standard C291's can handle.

$$I_{AV(max)} = \frac{815 + (n_p - 1)\,320}{3} \tag{6.16}$$

where n_p = number of C291's in parallel

If it is found that heat exchange surface temperature cannot be held at 62°C, then full RMS current capability of SCR_1 cannot be realized. One must start with heat exchanger temperature and adjust average current in SCR_1 to maintain junction temperature at +125°C.

It can be seen that in our example we have derated current 30% for parallel operation of two unmatched C291 SCR's. Section 6.2.2.2 defines "% parallel current derating."

If we had assumed single phase current rather than three-phase, the approach would be quite similar. Using the peak current in SCR_1, peak power is obtained from the "min (T_j = 125°C)" curve. For 180° half sine wave conduction, average power dissipation is given by the following empirical relationship:

$$P_{ave} = (0.286)\, P_{pk} \tag{6.17}$$

The remainder of the calculation follows that outlined for the three phase example.

Note that all calculations have been made assuming the SCR's to be in full conduction. With a constant impedance load, if you are operating within SCR rating at full conduction, you will remain within rating as conduction angle is decreased. However, with a variable impedance load, particularly back EMF loads, required current at maximum retard angle is used to choose the proper SCR. Assuming operation at maximum allowable RMS current at 120° conduction angle, the average power dissipation is about 15% less than that at 180° conduction angle and full RMS rating. When phasing back to less than 120° conduction angle, *average* power dissipation decreases about 12-15% more for every additional 30° of retard down to 30° conduction angle. These rules-of-thumb are used to determine power dissipation in the one low-forward-voltage-drop cell for which the specification sheet rating curves do not apply. For all other cells (high-forward-voltage-drop units) the specification sheet curves apply.

6.2.2.2 Use of SCR's with Matched Forward Characteristics

As we have seen from Figure 6.16, the range of forward characteristics for a given SCR production line can be quite wide. If we define percent derating for parallel operation as follows

$$\%\ \text{Parallel Derating} = \left(1 - \frac{I_T}{n_p I_M}\right) \times 100\% \tag{6.18}$$

where:

I_T = Total required load current through parallel arrangement

I_M = Maximum allowable current for a single cell operating alone

n_p = No. of cells in parallel

then we see that in our previous example of Section 6.2.2.1, 30% derating was required when operating two standard cells in parallel

$$\left(1 - \frac{815 + 320}{2 \times 815}\right) \times 100\% = 30\%$$

In order to allow for less derating, General Electric supplies C290/291 type SCR's with matched forward characteristics. The entire production is divided into a number of "forward grades." If devices of one "forward grade are paralleled, extremely good current sharing is obtained. If cells from two consecutive "forward grades" are paralleled, the sharing is still quite good but slightly higher current derating is required. When paralleling devices from three or four consecutive "forward grade" groups, the amount of required current derating increases further. It is interesting to investigate what increase in total current capability matched SCR's would give in our previous example of Section 6.2.2.1. Table 6.2 gives such a comparison.

TABLE 6.2 % Current Derating vs. Number of Consecutive "Forward Grades" Employed for C290/291 SCR

	Peak Current (example of 6.2.2.1)		% Parallel Current Derating
	SCR 1	SCR 2	
Standard Units	815 Amps	320 Amps	30
One Fwd. Grade	815 Amps	770 Amps	3
Two Consecutive Fwd. Grades	815 Amps	730 Amps	5
Three Consecutive Fwd. Grades	815 Amps	690 Amps	8
Four Consecutive Fwd. Grades	815 Amps	650 Amps	10

The procedure for designing parallel arrangements with matched SCR's is quite similar to that outlined in Section 6.2.2.1 with the following possible exception. Since little derating usually accompanies the use of matched cells, all cells are operating near maximum rated junction temperature. As such the $T_J = 125°C$ forward characteristics can usually be used exclusively with very little error.

6.2.2.3 External Forced Current Sharing

If less than approximately 30% current derating is required when paralleling SCR's with unmatched forward characteristics, external forced sharing is required. Returning to our example of Section 6.2.2.1 we found that SCR_1 carried an average current of 272 amperes and SCR_2 carried 107 amperes giving a total capability of 379 amperes.

The maximum average capability of one cell is 272 amperes; it follows that with varying degrees of forced current sharing, one could approach about 540 average amperes for two cells in parallel. Let's see how we go about designing such an arrangement. Figure 6.18 shows such an arrangement. Let's assume we want to force share just enough to allow 500 amperes of 3 phase average current.

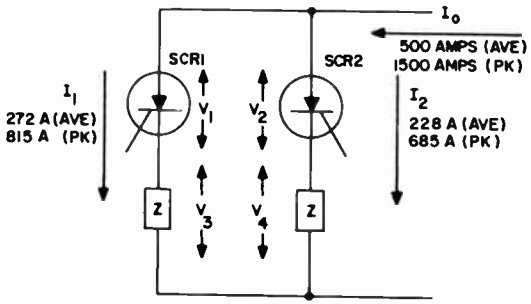


FIGURE 6.18 PARALLEL OPERATION OF SCR'S WITH FORCED SHARING

At ⅓ duty cycle (three phase operation) the current through the pair during the on portion of the cycle must be 1500 amperes. With 815 amperes allowable in SCR_1, SCR_2 must handle 685 amperes. Reading on-voltages from Figure 6.16, the relationship $V_1 + V_3 = V_2 + V_4$ can be solved.

$$\begin{aligned} V_1 + V_3 &= V_2 + V_4 \\ 1.05 + 815\,Z &= 1.2 + 685\,Z \\ Z &= 1.2 \times 10^{-3} \text{ ohms} \end{aligned} \tag{6.19}$$

If we use resistors to effect the sharing, they will indeed be effective but necessarily inefficient. In our example, the 1.2 milliohm resistor in series with SCR_1 will dissipate 256 watts.

Current sharing via inductors is more efficient than with resistors, but considering the currents involved the reactors can become rather expensive and physically cumbersome. In our example, at a frequency of 60 Hz about 3 μhenrys are required.

6.2.3 Surge Current Sharing

So far, our discussions of current sharing have dealt with continuous or load level currents. It is usually imperative that surge currents be adequately shared amongst parallel SCR's. Fortunately, there are factors going for, rather than against, current sharing at surge current levels.

First, above the crossover point (see Figure 6.19) the temperature coefficient of the SCR's on-voltage goes positive. Thus, as an individual SCR tends to hog current, its junction temperature increases, increasing its on-voltage, thus forcing more of the available current through the remainder of SCR's in the parallel arrangement. The high level forward characteristics for SCR type C290/291 are shown in Figure 6.19. Note that the crossover of temperature coefficient occurs at approximately 2700 amperes. The one-cycle surge rating of this device is 5500 amperes: a point well above the crossover.

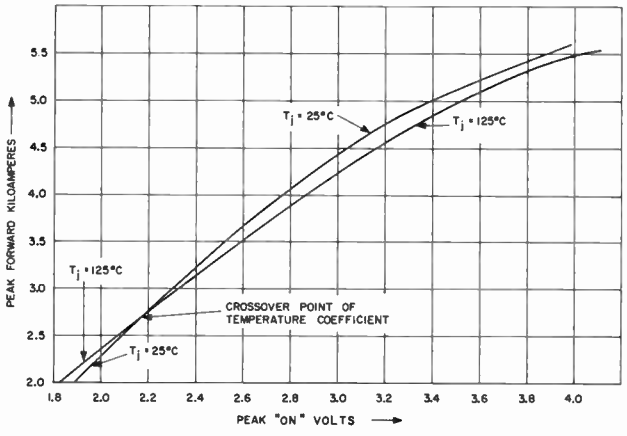


FIGURE 6.19 SURGE LEVEL—FORWARD CHARACTERISTIC SCR TYPE C290/291

Secondly, circuit and device impedances, previously insignificant at low level, begin to come into the picture. Take for instance the cathode "pigtail." The forward characteristics as shown are determined for a device before the pigtail is attached; the pigtail has a resistance of about 20 μohms. At a surge current of 5000 amperes, the voltage drop across the pigtail is 100 millivolts. Thus the pigtail actually helps to externally force-share current at surge levels. Other impedances such as the stud contact resistance, pigtail terminal contact resistance and external wiring resistance also perform the same function.

6.2.4 Triggering of Parallel Connected SCR's

If parallel SCR's are triggered from a common source, which is an essential requirement when switching high currents to large resistive or capacitive loads, each cell must be supplied with sufficient drive to exceed its own specific triggering needs. As previously pointed out, triggering requirements may differ quite widely between individual SCR's, whether or not units are parallel matched. As such the suggestions of Section 6.1.4.1 apply. In addition, it is necessary to drive the gates hard, commensurate with the peak and average gate power dissipation ratings in order to insure fast turn-on. This will help the SCR's to share the switching duty.

At low values of anode current the forward voltage-current characteristic changes from a positive to a negative resistance as it is reduced towards the minimum holding current. Below this value, the SCR will turn off by reverting to the forward blocking state. This transition point between positive and negative resistance is represented by the valley indicated in Figure 6.20, i.e., the current at which minimum forward voltage drop occurs. It is very difficult to match SCR's satisfactorily for identical characteristics in this region, particularly over wide ranges of temperature. This poses no problem when the gate signal is supplied to the parallel SCR's throughout the anode conduction period, since any instability in current-sharing or a tendency of one SCR to turn off will not overheat the other device(s) in parallel because of the low current level in the region of the valley. As long as gate current is maintained, an SCR with a tendency to turn off at low anode current levels will switch into conduction again as soon as the total load current moves out of this valley area. It will thus assume its share of the load before overloading on its partner can occur. When a pulse type of gate signal is employed for triggering paralleled SCR's, instability may be encountered at low anode current levels which may have serious consequences if high levels of current follow. Pulsed gate signals are typical of unijunction transistor triggering circuits and some types of saturable reactor triggering schemes. Unless the total load current has reached a sufficiently high level to keep all of the parallel cells above the valley point by the time the gate pulse is removed, a cell such as A in Figure 6.20 will turn off. In the absence of any further gate signal, it will remain in the non-conducting state through the remainder of that cycle, thus failing to carry its share of the load. This phenomenon is likely to occur when operating at very large conduction angles in phase controlled AC circuits and when triggering from reactive lines or into inductive loads where the buildup of load current to normal levels is restrained by the inductive effect.

For the above reasons use of a maintained gate signal is recommended for triggering parallel SCR's whenever possible.[16]

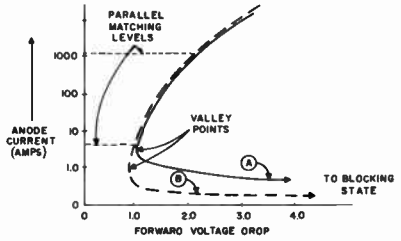


FIGURE 6.20 ANODE VOLTAGE-CURRENT RELATIONSHIP OF SCR'S WITH MATCHED FORWARD CHARACTERISTICS

6.2.5 Cluster SCR's for High Frequency Power

As mentioned earlier in Section 6.2, when special electrical characteristics only available in smaller SCR's are required, parallel operation is in order for higher power capability.

FIGURE 6.21a HIGH FREQUENCY CLUSTER THYRISTOR

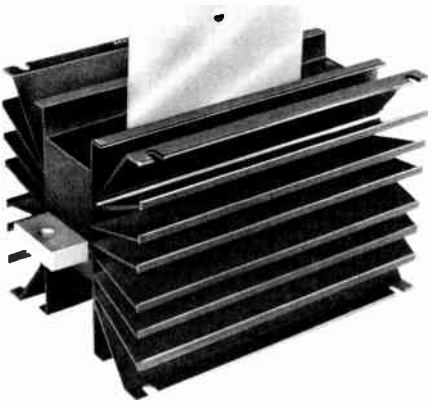


FIGURE 6.21b HIGH FREQUENCY CLUSTER THYRISTOR IN HEAT EXCHANGER

Figure 6.21 shows a high frequency power thyristor which is a cluster arrangement of smaller SCR packages. These clusters are supplied and specified as a single power thyristor by General Electric. Increased power handling capability is obtained by increasing the number of paralleled SCR's up to a given maximum. For more than two SCR's in parallel, a "pilot" SCR, as shown in Figure 6.22, is used. High frequency current capability for a cluster thyristor is shown in Figure 6.23. This is for the type C14043 or C14143 thyristor. Not only does this thyristor find a home in high power, high frequency applications, but in any application requiring an extremely high di/dt capability as evidenced by its turn-on current limit curve of Figure 6.24. These thyristor packages are designed to be compatible with the Wakefield GN-1251, WN-1245 and WN-1541 heat exchangers.

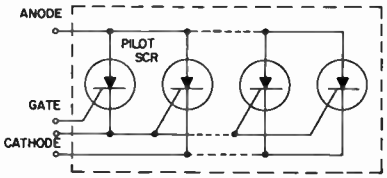


FIGURE 6.22 PARALLELING OF CELLS IN CLUSTER THYRISTOR

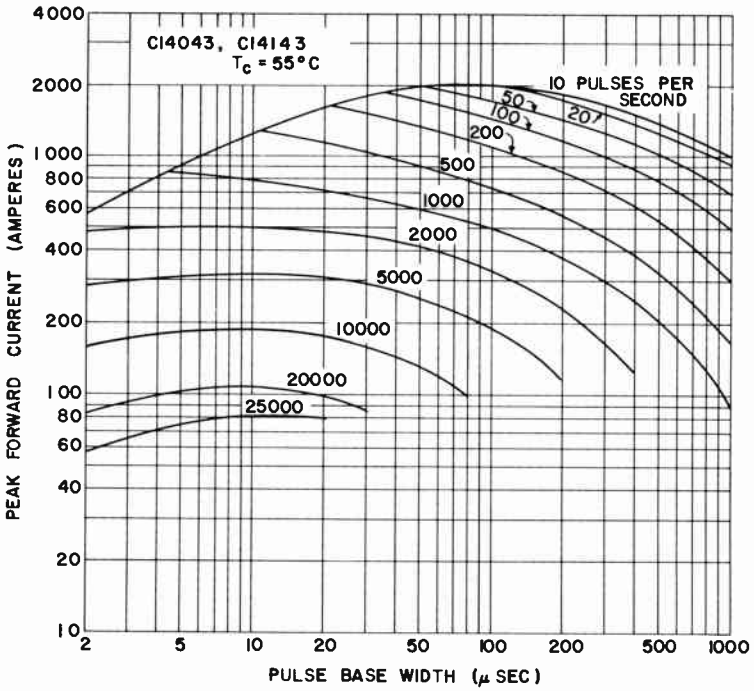


FIGURE 6.23 PEAK FORWARD CURRENT VS PULSE WIDTH AND FREQUENCY FOR C14043 & C14143 THYRISTOR

For further details on these cluster thyristors consult specification sheet 160.38.

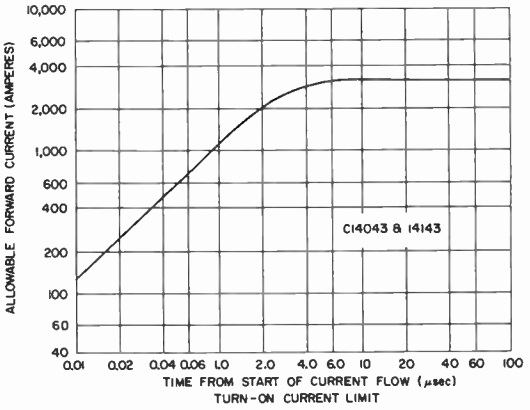


FIGURE 6.24 TURN-ON CURRENT LIMIT—C14043 & C14143 THYRISTORS

REFERENCES

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2. "Overcoming Turn-On Effects in Silicon Controlled Rectifiers," Neville Mapham, Electronics, August 17, 1962.
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4. "Commutation Behavior of Diffused High Current Rectifier Diodes," E. E. Von Zastrow and J. H. Galloway, General Electric Company, Auburn, New York, Application Note 200.42.*
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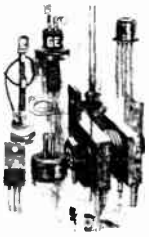
*Refer to Chapter 22 for availability and ordering information.

7

THE TRIAC



7.1 DESCRIPTION

"TRIAC" is a generic term that has been coined to identify the *tri*ode (three-electrode) *AC* semiconductor switch which is triggered into conduction by a gate signal in a manner similar to the action of an SCR. The triac, first developed by General Electric (patent No. 3,275,909 and other applications), differs from the SCR in that it can conduct in both directions of current flow in response to a positive or negative gate signal.

The primary objective underlying development of the triac was to provide a means for producing improved controls for AC power. The use of SCR's has proven the technical feasibility and benefits of the basic functions of solid-state switching and phase-control. In many cases, however, use of these functions has been limited by cost, size, complexity, or reliability. The triac development was based upon a continuing study of various ways for improving overall feasibility of the basic functions, including evaluation of circuits and components. To this end, the development appears to have been notably successful, particularly in the most simple functions.

7.1.1 Main Terminal Characteristics

The basic triac structure is shown in Figure 7.1(a). The region directly between terminal T_1 and terminal T_2 is a p-n-p-n switch in parallel with an n-p-n-p switch. The gate region is a more complex arrangement which may be considered to operate in any one of four modes: direct gate of normal SCR; junction gate of normal SCR; remote gate of complementary SCR with positive gate drive; and remote gate of complementary SCR with negative gate drive. For more detailed explanation of triac operation, see Section 1.5.

Figure 7.1 also shows the triac symbol, oriented in proper relationship to the structure diagram. Note that the symbol, although not fully definitive, is composed of the popularly accepted SCR symbol, combined with the complementary SCR symbol. Since the terms "anode" and "cathode" are not applicable to the triac, connections are simply designated by number. Terminal T_1 is the reference point for measurement of voltages and currents at the gate terminal and at terminal T_2

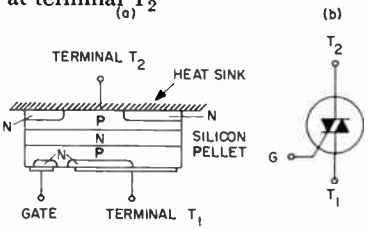


FIGURE 7.1 THE TRIAC; (A) PELLET STRUCTURE, (B) CIRCUIT SYMBOL

Initially the triac was made available in both the press-fit (cup) type package and with a stud attached, in 6 to 10 ampere RMS ratings, and with 200 and 400 volt minimum voltage breakover for 120 volt and 240 volt AC lines. Details on these and more recent types can be obtained from applicable specification sheets available from General Electric. Abbreviated specs are shown in Chapter 21.

The AC volt-ampere characteristic of the triac, Figure 7-2, is based on terminal T_1 as the reference point. The first quadrant, Q-I, is the region wherein T_2 is positive with respect to T_1, and vice versa for Q-III. The breakover voltage, $V_{(BR)}$, in either quadrant (with no gate signal) must be higher than the peak of the normal AC waveform applied in order to retain control by the gate. A gate current of specified amplitude of either polarity will trigger the triac into conduction in either quadrant, provided the applied voltage is less than $V_{(BR)}$. If $V_{(BR)}$ is exceeded, even transiently, the triac will switch to the conducting state and remain conducting until current drops below the "holding current", I_H. This action provides inherent immunity for the triac from excessive transient voltages and generally eliminates the need for auxiliary protective devices. *In some applications the turning on of the triac by a transient could have undesirable or hazardous results on the circuit being controlled, in which case transient suppression is required to prevent turn-on, even though the triac itself is not damaged by transients.*

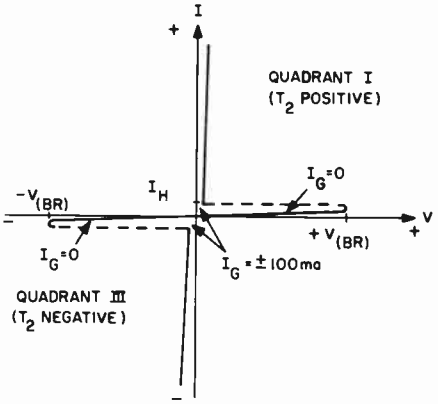


FIGURE 7.2 AC VOLT-AMPERE CHARACTERISTIC OF THE TRIAC

Triac current ratings are based on maximum junction temperature, similar to SCR's. The current rating is determined by conduction drop, i.e., power dissipation, and thermal resistance junction to case, and is predicated on proper heat-sinking. If the case temperature is allowed to go above its rated value, as determined from the specification sheet, the triac can no longer be guaranteed to block its rated voltage, or to reliably turn off when main terminal current goes through zero. For more details on current ratings of SCR's and triacs, see Chapter 3. For information on proper heat sink design, see Chapter 16.

For inductive loads, the phase-shift between line current and line voltage means that at the time that current drops to the I_H value and the triac changes to the non-conducting state, a certain line voltage exists which must then appear across the triac. If this voltage appears too rapidly, the triac will immediately resume conduction. In order to achieve proper commutation

with certain inductive loads, the dv/dt must be limited by a series RC circuit in parallel with the triac, or current, voltage, phase-shift, or junction temperature reduced. For further information on the use of triacs with inductive loads, see Section 7.1.4.

7.1.2 Gate Trigger Modes

Since the triac may be triggered with low energy positive or negative gate current in both the first and third quadrants, the circuit designer has a wide latitude for selection of the control means. Triggering can be obtained from DC, rectified AC, AC, or pulse sources such as unijunction transistors, neon lamps, and switching diodes such as the ST-2 "diac", and the silicon bilateral switch (SBS).

The triggering modes for the triac are:

I+; First quadrant, positive gate current and voltage.
I−; First quadrant, negative gate current and voltage.
III+; Third quadrant, positive gate current and voltage.
III−; Third quadrant, negative gate current and voltage.

The sensitivity of the triac, at present, is greatest in the I+ and III− modes, slightly lower in the I− mode, and much less sensitive in the III+ mode. The III+ mode should not be used, therefore, unless special circumstances dictate it. In such a case, triacs which are specially selected for the application should be requested.

The V-I characteristic of the triac gate shows a low non-linear impedance between gate and terminal T_1. The characteristic is similar to a pair of diodes connected in a back-to-back configuration. Since in any given mode this characteristic is similar to an SCR gate, the gate requirements are rated exactly like SCR's. For details on gate trigger ratings, see Chapter 4.

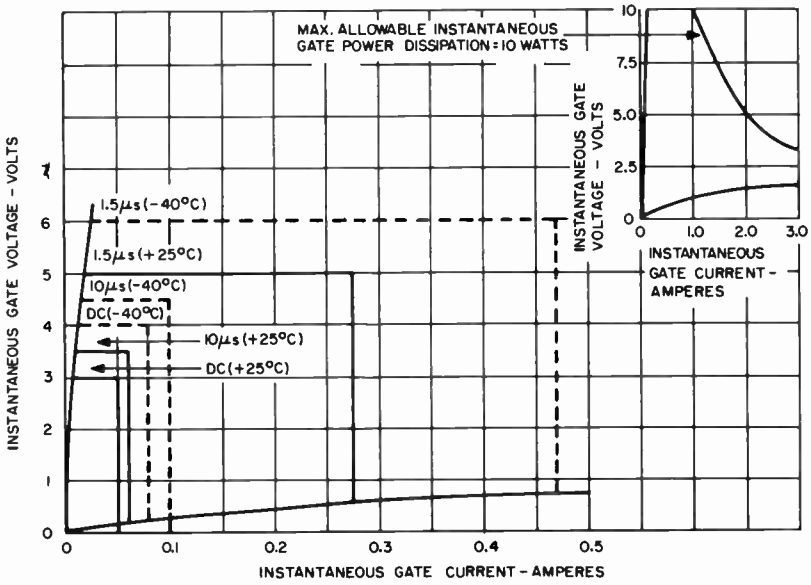
7.1.3 Pulse Triggering

Since the triac is quite often used with trigger sources which generate short duration pulses, such as a unijunction transistor or a trigger diode such as a diac or an SBS, the triac gate requirements are also specified in terms of short duration pulses. Figure 7.3 shows a triac gate trigger characteristic. Note that this shows the required gate drive for pulse widths of 1.5 and 10 microseconds, as well as for DC drive, at junction temperatures of 25°C and −40°C.

For pulse durations of 5 microseconds or less, the triac gate requirements may be expressed as a quantity of charge required to fire. The amount of charge required may be determined from the 1.5 microsecond gate current requirements.

For example, from Figure 7.3, the gate requirement for 25°C at 1.5 microseconds is 275 ma. This is a charge of $1.5 \times 0.275 = 0.4125$ μcoulombs. This would mean that a 0.1 μf capacitor would have to be discharged a minimum of 4.125 volts to insure triggering. Obviously, a 0.05 μfarad capacitor discharged 8.25 volts would also suffice.

The triac is designed to be reliably fired by the ST-2 diac discharging a 0.1 μfd capacitor. This is for pulse firing in the I+ and III− modes of gate triggering. The triac will also fire reliably with pulses from a 2N2646 unijunction transistor, with V_{BB} at 20 volts, and discharging a 0.1 μf capacitor. For unijunction triggering, negative gate pulses must be used (I− and III−) for reliable triggering.



NOTES
(1) RECTANGULAR GATE SOURCE VOLTAGE PULSES APPLIED WITH PULSE RISE TIME EQUAL TO 10% OF PULSE WIDTH
(2) ANODE SUPPLY
12 VOLTS, 100 OHMS AT +25°C
12 VOLTS, 50 OHMS AT -40°C
(3) GATE VOLTAGE IS REFERED TO ANODE 1

FIGURE 7.3 TYPICAL MAXIMUM PULSE AND DC GATE TRIGGER CHARACTERISTICS FOR A TRIAC

7.1.4 Commutation of Triacs

One important difference between use of a pair of SCR's and use of a triac in an A-C circuit is that with SCR's each SCR has an entire half cycle to turn off, while the triac must turn off during the brief instant while the load current is passing through zero. For this reason, operation of present triacs is limited to 60 Hz line frequency. The ability of the triac to commutate, or turn off, is a strong function of temperature. The failure of a triac to turn off when the gate drive is removed is a good sign that its maximum junction temperature has been exceeded.

Inductive load applications of the triac may exhibit some particular problems which must be taken into account. The most common of these problems is that of commutation dv/dt. This dv/dt is that rate of rise of voltage which is impressed on the triac by the circuit immediately following turn off at current zero. This is illustrated by Figure 7.4. In an inductive circuit, the current lags the voltage, and reaches zero sometime after the voltage has reached a value in the opposite polarity. Since the triac tries to open at current zero and there is no current in the inductance, the instantaneous line voltage appears across the triac at a rate limited only by the stray capacitance and the capacitance of the triac, C_s. For the triac to turn off reliably in this kind of circuit it is therefore necessary to limit the rate of voltage rise with additional capacitance, C_1. It is also necessary to put in resistance R_1

to damp the ringing of the capacitance with the load inductance (overshoot), and to limit the surge of current from the capacitor when the triac fires.

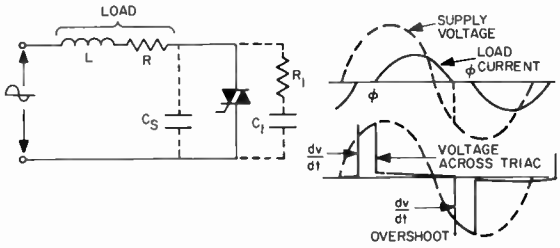


FIGURE 7.4 COMMUTATION dv/dt DUE TO INDUCTIVE LOADS

For almost all practical inductive loads, values of 100 ohms and 0.1 μfd for R_1 and C_1 respectively will limit the commutation dv/dt to about 1 volt per microsecond. The exact value of R_1 should be determined for proper damping for each individual application.

In addition to the use of the R-C network, it is important to use a triac which has been rated with a minimum commutation dv/dt capability on inductive loads. These are available from General Electric by contacting your local semiconductor sales representative regarding types which guarantee a commutation dv/dt capability of at least 2 volts per microsecond.

7.2 USE OF THE TRIAC

The versatility of the triac and the simplicity of its use make it ideal for a wide variety of applications involving AC power control.

7.2.1 Static Switching

The use of the triac as a static switch in AC circuits gives many definite advantages over mechanical switching. It allows the control of relatively high currents with a very low power control source. Since the triac "latches" each half cycle, there is no contact bounce. Since the triac always opens at current zero, there is no arcing or transient voltage developed due to stored inductive energy in the load or power lines. In addition, there is a dramatic reduction in component count compared to other semiconductor static switches.

The most striking example of circuit simplification is seen in the elementary static switch shown in Figure 7.5(a). The glass-enclosed magnetic reed switch provides many million operations from a permanent magnet or from a DC electromagnet "relay" coil. Since the contacts only handle current during the few microseconds required to trigger the triac, a wide variety of small switching elements may be used in place of the reed switch, such as relays, thermostats, pressure switches, and program/timer switches. In many cases, snap action of triggering contacts can be eliminated, thus reducing their cost as well. This circuit uses gate firing modes I+ and III—. Figure 7.5(b) shows the use of a low current diode in series with the surge limiting resistor, and a three position switch, to obtain a simple three position power

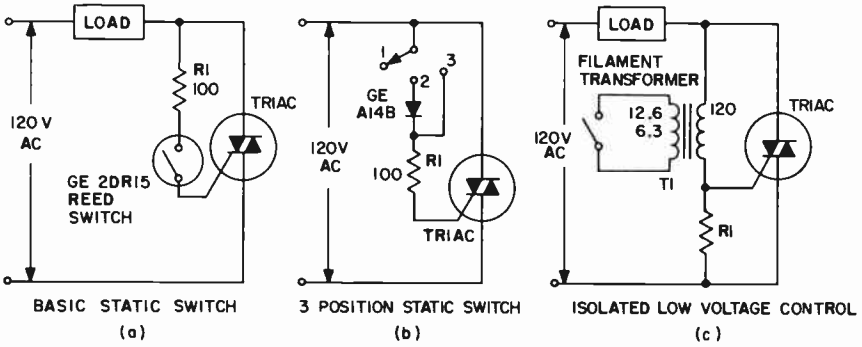


FIGURE 7.5 STATIC AC SWITCHING APPLICATIONS OF THE TRIAC

control. In position one, there is no gate connection, and the power is off. In position two, gate current is allowed in one half cycle only, and the power in the load is half-wave. In position three, there is gate current for both half cycles, and the power is on full. As shown in Figure 7.5(c), the switch can be replaced by a transformer winding. This circuit makes use of the difference in primary impedance between the open circuit and shorted secondary cases. The resistance R is chosen to shunt the magnetizing current of the primary to ground. This circuit provides control with isolated low voltage contacts.

Resonant-reed relays have also been used with the triac in the circuit of Figure 7.5(a) to provide very sharp frequency-selective switching in response to coded audio input signals in multi-channel operations. At the lower frequencies some modulation of triggering point results from beating with line frequency.

Other useful switching circuits are shown in Figure 7.6, showing DC and AC triggering for the triac. Switch S_1 may be replaced by a transistor which is controlled by a thermistor or a photocell, or other electrical signal as shown in Figure 7.7. The AC signal of Figure 7.6(b) could be 60 Hz if phased properly to trigger early in each half cycle of the supply wave. Higher frequencies, above 600 Hz, are also effective and reduce the size of T, but produce very slight irregularities in triggering point, which are usually negligible. Frequency selectivity may be obtained by tuning T or by use of other static or dynamic filter circuits for remote-control work or for tape-recorder programming of a system. In any case the trigger signal should be significantly ON or OFF since the trigger sensitivity of the triac is not quite uniform in both polarities or both quadrants and should not be used, therefore, as a threshold detector.

The transistor connections of Figure 7.7 are ideal for driving the triac, or an array of triacs, from a low level DC logic source. One example of this is illustrated by Figure 7.8 which shows two triacs being driven by a transistor flip-flop circuit in an AC power flasher arrangement.

For further informative details on static switching, see Chapter 8.

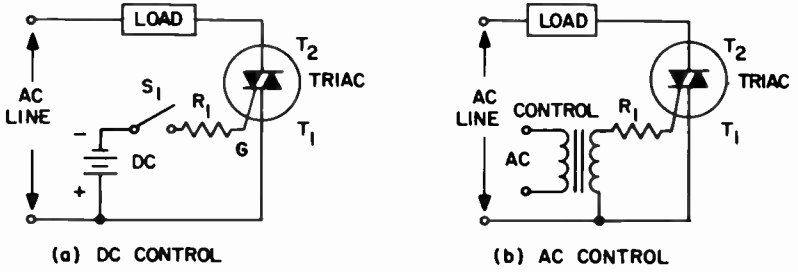


FIGURE 7.6 ELECTRICALLY ACTUATED AC STATIC SWITCHES

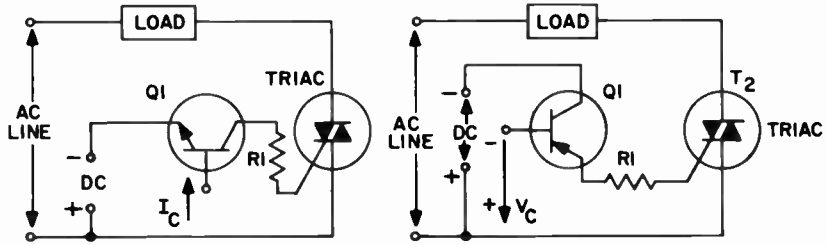


FIGURE 7.7 TRANSISTOR GATING CONTROL

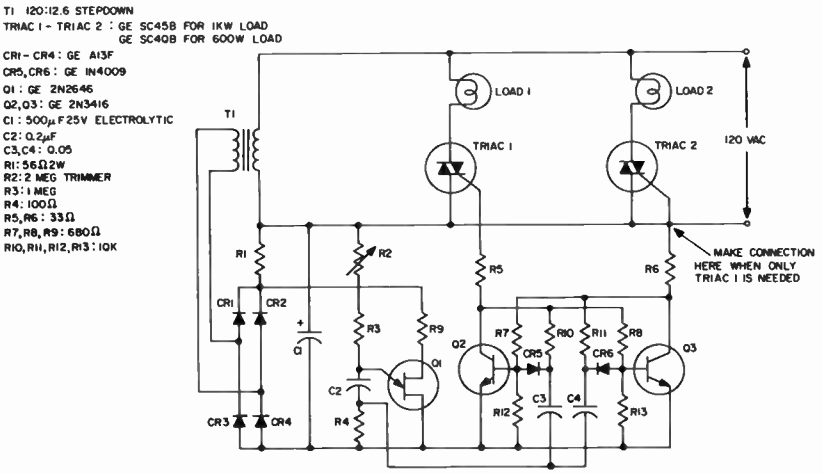


FIGURE 7.8 A-C POWER FLASHER. TRIACS 1 AND 2 ALTERNATE THEIR ON-STATE AT A FREQUENCY DETERMINED BY THE SETTING OF R2.

7.2.2 Firing With a Trigger Diode

Only four components are required to form the basic full wave triac phase control circuit shown in Figure 7.9 Adjustable resistor R_1 and capacitor C_1 are a single-element phase-shift network. When the voltage across C_1 reaches breakover voltage, $V_{(BR)}$, of the diac, a bi-directional trigger diode,

C_1 is partially discharged by the diac into the triac gate. This pulse triggers the triac into the conduction mode for the remainder of that half-cycle. Triggering is in the I+ and III— modes in this circuit. Although this circuit has a limited control range, and a large hysteresis effect at the low-output end of the range, its unique simplicity makes it suitable for many small-range applications such as lamp, heater and fan-speed controls.

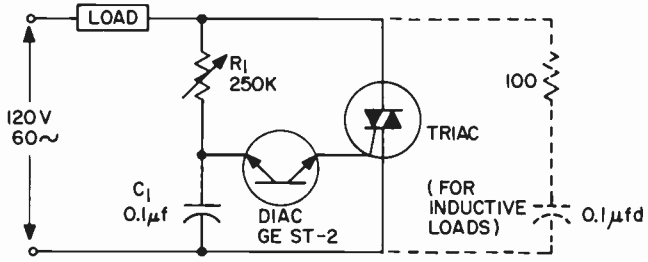


FIGURE 7.9 BASIC DIAC-TRIAC PHASE CONTROL

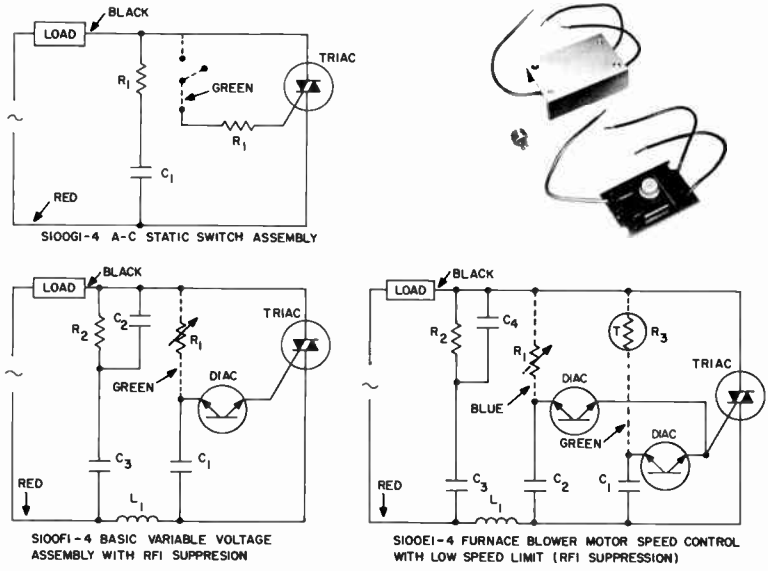
To eliminate some of the problems of this basic circuit, more sophisticated circuits are generally used where the full control range is required. Other types of bidirectional trigger diodes, such as the silicon bilateral switch (SBS), may also be used. More details on this type of firing circuit will be found in Chapter 9.

7.2.3 Firing With a Unijunction Transistor

For more complex control functions, particularly closed loop controls, the unijunction transistor may be used for the triggering device in a ramp-and-pedestal type of firing circuit. An example is the temperature control of Figure 12.15. Additional explanation of this type of firing circuit and the many functions that can be performed is given in Chapter 9. In this type of connection, the pulse transformer should be connected to give negative pulses to the triac.

7.3 TRIAC ASSEMBLIES

Because the triac has found wide acceptance in areas where there is little experience in constructing electronic controls, the General Electric Company has introduced a line of triac assemblies to perform a variety of basic control functions. All necessary components (except potentiometers) to do the functions of manual phase control, static switching, and radio frequency filtering as required, are mounted in an electrically isolated standard aluminum channel as shown in Figure 7.11. This channel may be mounted in the users equipment to obtain proper heatsinking for up to 10 amperes current rating. Figure 7.11 shows some of the circuit variations available. Details on these assemblies may be obtained from local General Electric Electronic Components Sales Offices.



NOTE: FOR 120V RMS UNITS USE R_1 = 250,000 OHMS, 2 WATTS

FOR 240V RMS UNITS USE R_1 = 500,000 OHMS, 2 WATTS

FIGURE 7.10 A TYPICAL STANDARD G-E TRIAC ASSEMBLY AND SOME OF THE AVAILABLE CIRCUIT VARIATIONS.

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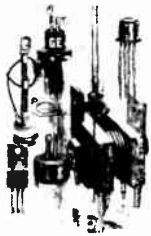


STATIC SWITCHING CIRCUITS

8.1 INTRODUCTION

Since the SCR and the triac are bistable devices, one of their broad areas of application is in the realm of signal and power switching. This chapter describes circuits in which these thyristors are used to perform simple switching functions of a general type that might also be performed non-statically by various mechanical and electromechanical switches. In these applications the thyristors are used to open or close a circuit completely, as opposed to applications in which they are used to control the magnitude of average voltage or energy being delivered to a load. These latter types of applications are covered in detail in succeeding chapters.

Static switching circuits can be divided into two main categories: AC switching circuits and DC switching circuits. AC circuits, as the name implies, operate from an AC supply and the reversal of the line voltage turns a thyristor off. Since most triacs are designed for 60 Hz operation, applications requiring a higher frequency would dictate the use of two SCR's in inverse-parallel connection. The maximum frequency of operation of SCR's however is limited to approximately 30 K Hz by the turn-off time requirement of the SCR. Above these frequencies the SCR's may not recover their blocking ability between successive cycles of the supply. DC switching circuits on the other hand operate from a DC (or a rectified and filtered AC) source and an SCR must be turned off by one of the methods described in Chapter 5. In applications where the circuit turn-off time is limited, special inverter type SCR's such as the C9, C12, C40, C55, C140 or C154 series may be required. These types have tested maximum turn-off time specifications.

8.2 STATIC AC SWITCHES

8.2.1 Simple Triac Circuit and Inverse-Parallel ("Back-to-Back") SCR Connection

The circuits of Figure 8.1 provide high speed switching of AC power loads, and are ideal for applications with a high duty cycle. They eliminate completely the contact sticking, bounce, and wear associated with conventional electro-mechanical relays, contactors, etc. As a substitute for control relays, thyristors can overcome the differential problem, that is the spread in current or voltage between pickup and dropout, because thyristors effectively drop out every half-cycle. Also, providing resistor R is chosen correctly, the circuits are operable over a much wider voltage range than is a comparable relay. Resistor R is provided to limit gate current peaks. Its resistance (which can include any "contact" resistance of the control device and load resistance)

should be just greater than the peak supply voltage divided by the peak gate current rating of the SCR. If R is made too high, the SCR's may not trigger at the beginning of each cycle, and "phase control" of the load will result with consequent loss of load voltage and waveform distortion. The control device indicated can be either electrical or mechanical in nature. Light dependent resistors, magnetic cores, and magnetic reed switches are all suitable control elements. In particular, the use of hermetically sealed reed switches as control elements in combination with SCR's and triacs offers many advantages. The reed switch can be actuated by passing AC or DC current through a small winding around it, or by the proximity of a small magnet. In either case complete electrical isolation exists between the control signal input, which may be derived from many sources, and the switched power output. Long life is assured the SCR or triac/reed switch combination by the minimal volt-ampere switching load placed on the reed switch by the SCR or triac triggering requirements. The thyristor ratings determine the amount of load power that can be switched.

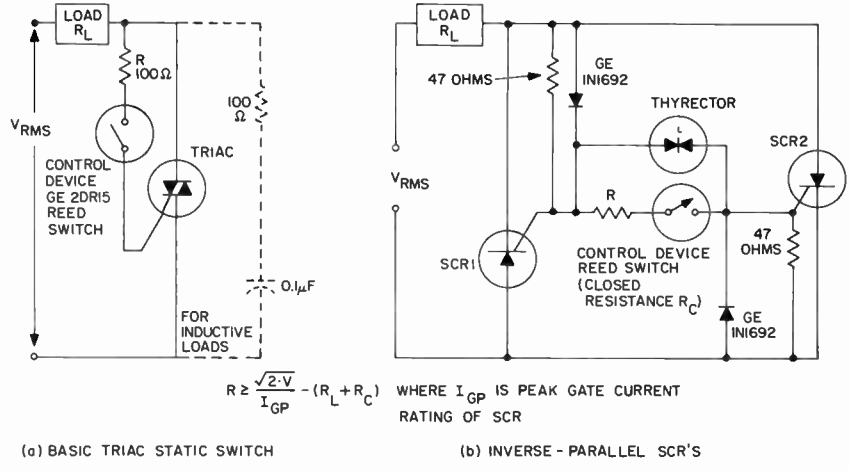


FIGURE 8.1 STATIC AC SWITCHES

For simple static AC switching, the circuit of Figure 8.1(a) has the advantage over that of Figure 8.1(b) in that it has fewer (⅓) components. The circuit of Figure 8.1(b), and those circuits to follow using the inverse-parallel SCR configuration, should be kept in mind for applications where the commercially available triacs cannot handle severe load requirements such as high frequency, voltage, and current.

8.2.2 Static Switching With Separate Trigger Source

Where DC isolation between control signal input and load is desired *without* the use of a mechanical switch, light, or saturable core intermediary, or where a widely varying AC supply precludes satisfactory triggering of the

type shown in Figure 8.1, a triac or a back-to-back pair of SCR's may be triggered from a separate source as shown in Figure 8.2. Here, the high frequency output of a transistor blocking oscillator, or a UJT free-running oscillator is transformer coupled to the triac or SCR gates. Suitable oscillator circuits are discussed in Section 4.14. For minimum load waveform distortion and minimum generated RFI, oscillator frequency should be high enough to ensure that the triac or SCR's trigger early in the AC cycle. Other types of UJT trigger circuits suitable for use with AC static switching arrays are described in the next chapter.

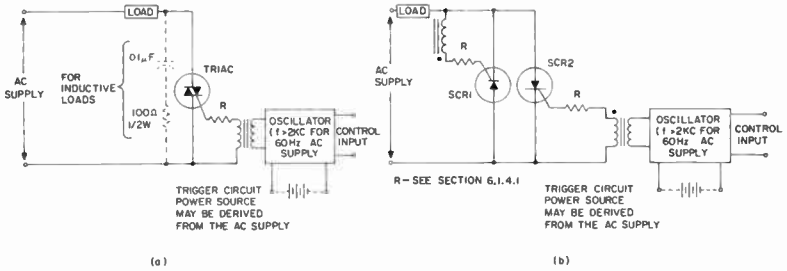


FIGURE 8.2 OSCILLATOR DRIVEN AC STATIC SWITCH

8.2.3 Alternate Connections For Full Wave AC Static Switching

Full wave static AC switching can also be performed by various combinations of SCR's and conventional rectifiers, or simply by a triac. The most useful of these arrays are shown in Figure 8.3.

The circuit of Figure 8.3(a) uses a single SCR connected across the DC output of a rectifier bridge, to switch an AC load connected in series with the supply line. The bridge rectifies the incoming AC to full wave pulsating DC, so that one SCR can control both half cycles of the AC. In this circuit the SCR turns off at the end of each half cycle when the supply voltage is zero. Unsmoothed DC can be made to flow in the load, if desired, by removing the load from the AC supply line, and placing it in series with the SCR as shown in Figure 8.3(b). In this case, for proper commutation of the SCR, a "free-wheeling" diode must be connected across the load if the load is at all inductive. The circuit of Figure 8.3(c) uses two SCR's and two rectifiers to switch an AC load, SCR1 and CR1 conducting on one half cycle of the supply, SCR2 and CR2 conducting on the other. The "DC load" equivalent to Figure 8.3(c) is shown in Figure 8.3(d). If the AC supply has significant inductance, the AC bridge in Figures 8.3(a) and (b) will reverse so rapidly that the SCR may not have time to commutate. In such a case Figures 8.3(c) and (d) will give a better result. The circuit of Figure 8.3(e) shows how a triac may be triggered with a DC control signal. Unlike the circuit of Figure 8.1(b), the static switching configurations of Figure 8.3 may be triggered directly by a single-ended (DC) non-isolated control signal, because the SCR cathodes are tied together. In low voltage switching applications, the multiple voltage drops in series with the load for Figures 8.3(a) through (d) may be a disadvantage.

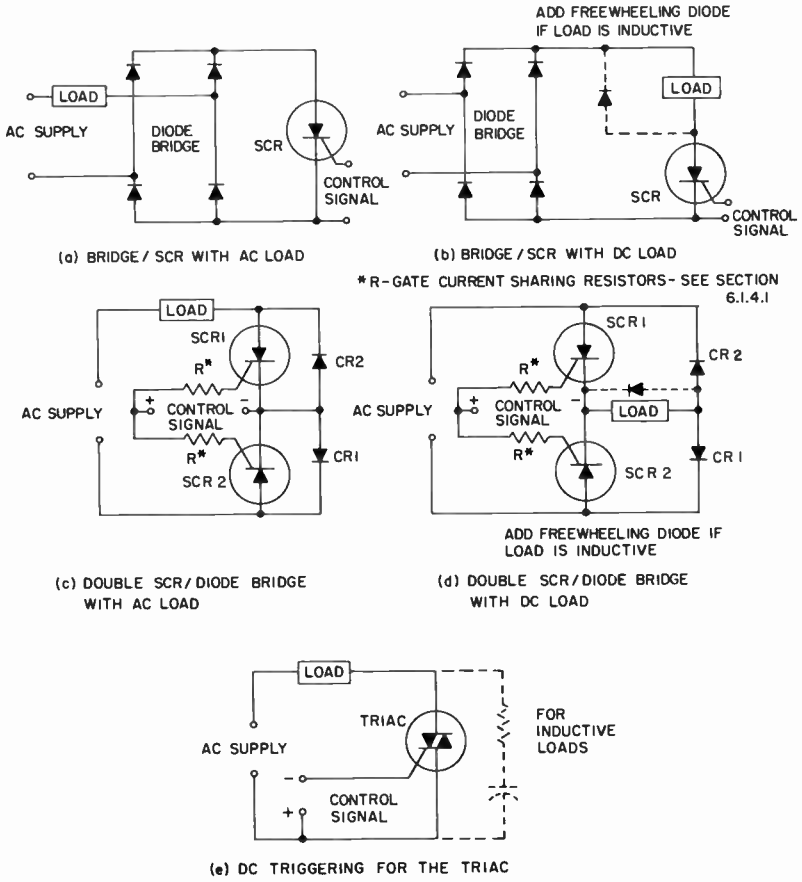


FIGURE 8.3 SCR/DIODE AND TRIAC STATIC SWITCH CONFIGURATIONS

8.3 ZERO-VOLTAGE OR SYNCHRONOUS SWITCHING, AC LATCHING AND PROPORTIONAL CONTROL

When any switch is closed, be it mechanical or thyristor, the resulting step change in current causes a considerable amount of radio frequency interference (RFI) to be generated. In switching heavy resistive loads, such as heaters, it is desirable to minimize the amount of RFI generated. One of the possible ways of accomplishing this is by switching the SCR or triac as nearly as possible to the point when the line voltage passes through zero. This method is known as synchronous or zero-voltage switching. Zero-voltage switching is used widely in temperature control circuits along with another technique known as proportional control. These methods vary the average power applied to a load by changing the on-off duty cycle, thus providing controlled bursts of complete cycles to the load.

8.3.1 Triac Latching Technique

The circuits of Figure 8.4 show a basic triac latching switch. When voltage is applied to the circuit of Figure 8.4(a), the triac is initially blocking, and the full line voltage appears across the triac. This means that no voltage appears across the load, and since the gate must be at the same level as T_1 of the triac, there is no voltage across R_1 and C_1, and no current in the gate. After the triac has been triggered, the line voltage appears across the load, and across R_1 and C_1. The quadrature current through R_1, C_1 and the triac gate is at its peak when the load voltage goes through zero, retriggering the triac each half cycle. Since this circuit uses firing modes III+ and I−, a specially selected triac must be used (Chapter 7).

Similarly, in Figure 8.4(b), when a trigger pulse is applied, the triac turns on. The line voltage which now appears across the load causes the flow of current through inductor L_1 and resistor R_2. This gate current is about 90° out of phase with the supply voltage. When the line voltage reverses polarity, this current continues to flow out of the gate to inductor L_1 causing the triac to turn on as the line voltage on T_2 goes negative. Unlike the circuit of Figure 8.4(a), the circuit in Figure 8.4(b) uses firing modes I+, III− and therefore does not require a specially selected triac as was the case for Figure 8.4(a).

The instantaneous current through the gate networks (R_1-C_1 or R_2-L_1) at the instant the line current reverses polarity determines if the triac will latch on. It is therefore necessary to select the values of R_1-C_1 or R_2-L_1 to produce a sufficient quadrature current to trigger the triac each half cycle. For reactive loads, the sinusoidal gate current is sufficiently phase shifted from the line current such that R_1 or R_2 alone (without C_1 or L_1) may be used to trigger the triac provided that enough gate drive is available when the line current goes through zero.

It will be noted that if the triac is triggered by a transient on the line, the latching characteristic of the circuit will cause the load to remain energized until the circuit is reset.

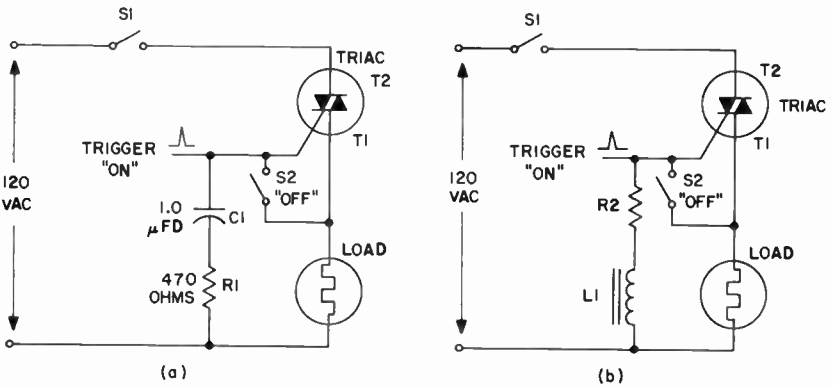


FIGURE 8.4 TRIAC LATCHING CIRCUIT

Figure 8.5 shows a time delay circuit using the triac latching technique. When capacitor C_1 charges to the breakover voltage of the diac, the triac fires and energizes the load. The time delay is determined by the time constant of $(R_1 + R_2)$ and C_1. To reset the circuit, capacitor C_1 is discharged through R_3 and R_4.

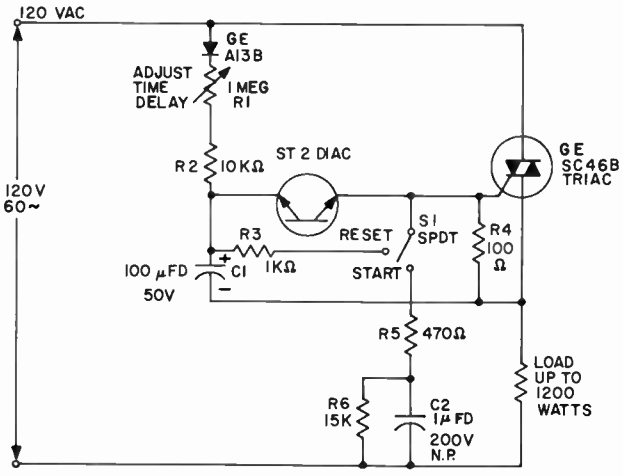


FIGURE 8.5 A SIXTY-SECOND TRIAC TIME DELAY CIRCUIT

8.3.2 Negative Half Cycle SCR Slaving Techniques

The circuit of Figure 8.6 shows how one SCR, in a back-to-back configuration, can be latched on to fire at the beginning of a negative half cycle as a slave of another SCR. When SCR_1 is fired, capacitor C_1 is charged through diode CR_1 and resistor R_1. C_1 then discharges through R_2 and the gate of SCR_2, supplying the necessary gate current to fire SCR_2 at the beginning of the negative half cycle.

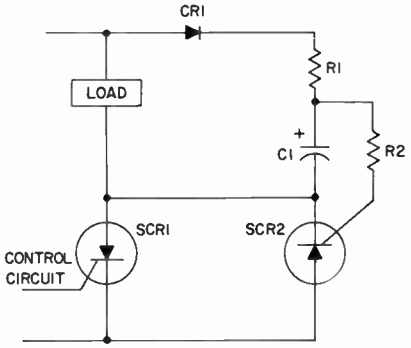


FIGURE 8.6 NEGATIVE HALF CYCLE SCR SLAVING CIRCUIT

In order to fire SCR_1 again when the AC line goes positive, the control circuit must supply the necessary trigger current; otherwise both SCR's would stay off. This circuit therefore is not a latching circuit.

Figure 8.7 shows another combination of SCR slaving and synchronous switching. Here the absence of an "open" signal causes the SCR's to deliver full wave power to the load. Regardless of the phasing of the control signal, load voltage is always applied in full cycles with negligible discontinuities, hence minimum radio frequency interference. SCR_2 operates as a "slave" of SCR_1 because the energy stored in inductor L_1 fires SCR_2 at the beginning of the next half cycle, thus always delivering an even number of half cycles to the load, and reducing magnetic saturation effects in inductive loads. By applying a gate signal to SCR_3, the gate drive to SCR_1 is diverted and its gate is essentially clamped to its cathode. When the line goes positive on the anode of SCR_1, since there is no gate signal present, SCR_1 is kept off, thus de-energizing the load. These circuits are ideal wherever RFI and audio filtering is undesirable, where magnetizing inrush current to transformers causes nuisance fuse blowing, and where sensitive test equipment operates in the vicinity of power switches.

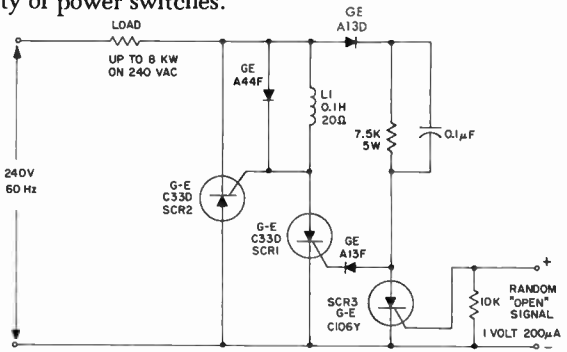


FIGURE 8.7 ZERO VOLTAGE SWITCHING FOR LOW RFI OPERATION

8.3.3 Proportional Control With Zero-Voltage Switching

The circuit of Figure 8.8 switches only complete half cycles of power to the load, i.e., the SCR is either fired at the beginning of alternate half cycles or biased off completely.

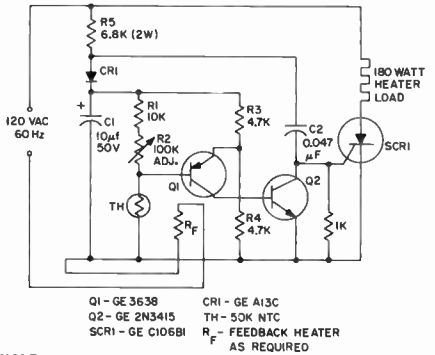


FIGURE 8.8 HALF WAVE ZERO-VOLTAGE SWITCHING TEMPERATURE CONTROLLER

This low cost solid state temperature controller duplicates the proportional control function of the bimetal switch normally supplied with automatic blankets. It is equally effective for use with other low power heating loads below 180 watts. The circuit works as follows: Rectifier CR_1 and capacitor C_1 form a simple DC power supply for the resistance bridge consisting of $(R_1 + R_2)$, the thermistor, R_3, and R_4. The base-emitter input terminals of transistor Q_1 are connected across the output terminals of this bridge, and Q_1 amplifies bridge unbalance, if any. When the bridge is balanced (adjustable via R_2), there is no output, Q_1 is cut off, and transistor Q_2 receives no base drive. During the initial portion of each positive half cycle of the AC supply, before diode CR_1 starts to conduct, capacitor C_2 couples current into the gate of SCR_1, and SCR_1 triggers and energizes the load. Note that, once CR_1 starts to conduct, C_2 is clamped to a DC voltage established by capacitor C_1 and gate current ceases to flow. Thus, SCR_1 can only trigger at the start of each positive half cycle. In this way RFI is minimized.

With current flowing through the heater load, the feedback resistor R_F raises the temperature of the monitoring thermistor TH. As the thermistor's resistance drops, the bridge unbalances and transistor Q_1 starts to conduct. Transistor Q_2, which receives base drive from Q_1, is driven into saturation and shunts gate current away from SCR_1. SCR_1 turns off and removes power from the load. SCR_1 comes back on again only when the monitoring thermistor cools toward room ambient. The on-off cycle repeats itself at a rate determined by room temperature, with on-time increasing if room temperature falls, decreasing if the room heats. If R_F is designed to be the thermal analog of the load, this circuit can be made to regulate load temperature against variations in ambient temperature and live voltage.

Figure 8.9 shows a more elaborate proportional control circuit supplying full wave power to the load. It is ideal for applications where variable-gain proportional control with zero-voltage switching is desired.

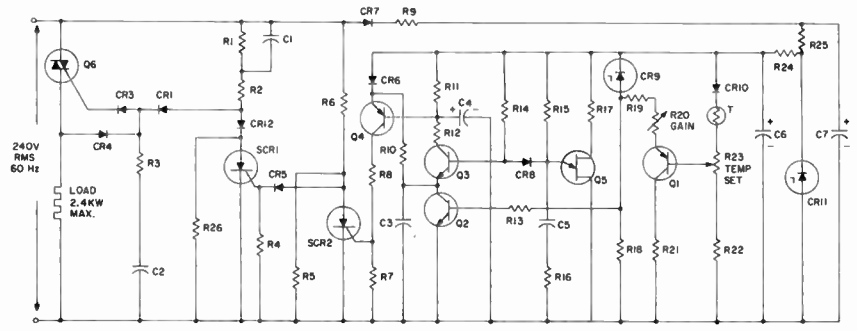


FIGURE 8.9 FULL WAVE PROPORTIONAL ZERO VOLTAGE SWITCHING TEMPERATURE CONTROL.

The operation of the circuit is as follows: CR_7, R_9, R_{25}, C_7, CR_{11}, R_{24}, and C_6 comprise a DC regulated, highly filtered, power supply. A bridge circuit is formed by CR_9, R_{19}, R_{20}, Q_1, R_{21}, CR_{10}, T, R_{23}, and R_{22}. As the thermistor increases or decreases its resistance with temperature, an offset voltage is produced at the base of Q_1 which is amplified by Q_2. This produces a DC bias level at the emitter of Q_3. The unijunction (Q_5), C_5, and R_{15} provide a *constant low-frequency* sawtooth voltage at the emitter of Q_5, the amplitude of the sawtooth excursion being fixed by the triggering potential of Q_5. When Q_5 triggers, capacitor C_5 discharges rapidly and diode CR_8 follows the charging potential of C_5 keeping Q_3 turned off which in turn turns off Q_4 and SCR_2. This allows SCR_1 to conduct and remove the triac gate voltage thus removing load voltage. When the potential on C_5 reaches the approximate potential on the collector of Q_2, semiconductors Q_3, Q_4, and SCR_2 conduct; SCR_1 turns off; and load voltage is applied. Thus the bias voltage on the collector of Q_2 provides different periods of time when Q_3 is turned on, and these periods of time are controlled by the resistance of the thermistor. Figure 8.10 illustrates the load duty cycle. The latching action of the triac and SCR_1 always provides zero-voltage switching of the load.

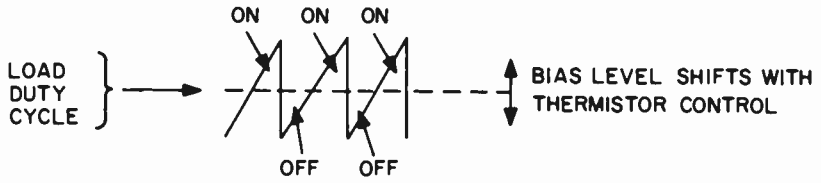
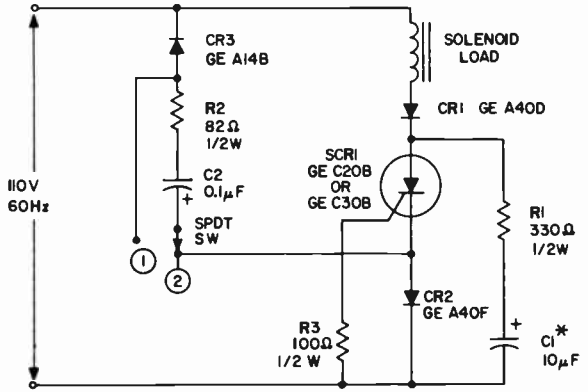


FIGURE 8.10

For more information on proportional control the reader is referred to Chapter 12 and to Reference 2 at the end of this chapter.

8.4 "ONE SHOT" SCR TRIGGER CIRCUIT

A circuit to trigger an SCR for one complete half cycle only of the AC supply is shown in Figure 8.11. Triggering is initiated by closing push button switch SW, and the SCR triggers always *near the beginning* of a positive half cycle, even though the switch may be closed randomly at any time during the two preceding half cycles. The SCR will not trigger again until SW is opened and then reclosed. This type of logic is required for some test equipment supplies and for the solenoid drives of electrically operating stapling guns, impulse hammers, etc., where load current must flow for one complete half cycle only.



*TIME CONSTANT OF C1 R1 MAY NEED TAILORING DEPENDING ON HOLDING CURRENT OF SCR1. SEE TEXT.

FIGURE 8.11 ONE SHOT SCR TRIGGER CIRCUIT

During half cycles of the AC line when the SCR anode is positive, capacitor C_1 will be charged through the load, CR_1 and R_1. As long as switch SW is maintained in position 1, the SCR will be non-conducting. When SW is flipped to position 2 and the line voltage is negative, the charging current of C_2 (through the series-network of R_3, the gate to cathode junction of the SCR, SW, C_2, R_2 and CR_3) will trigger the SCR even though the line voltage is negative because the anode of the SCR sees the positive voltage on C_1. SCR_1 is thus only turned on when the line voltage is negative and maintained on by supplying holding current from capacitor C_1, through resistor R_1. The series network of R_1 and C_1 is selected to supply a sufficient amount of holding current for one-half cycle only since providing holding current for a longer duration than one-half cycle would keep the SCR on for succeeding half cycles. The SCR holding current therefore determines R_1 C_1. Once C_2 has been charged, there will be no gate current through the SCR even if SW is maintained in position 2. To fire the SCR again, SW would have to be flipped to position 1 in order to discharge C_2.

8.5 BATTERY CHARGING REGULATOR

Figure 8.12 illustrates an inexpensive means of utilizing the SCR as a battery charging regulator, thus eliminating the problems inherent in electromechanical voltage relays—contact sticking, burning, wide range of pickup and drop out, wear, etc. As shown the circuit is capable of charging a 12 volt battery at up to a six ampere rate. Other voltages and currents, from 6 to 600 volts and up to 300 amperes, can be accommodated by suitable component selection.[3] When the battery voltage reaches its fully charged level, the charging SCR shuts-off, and a trickle charge as determined by the value of R_4 continues to flow.

CR_4 and CR_5 deliver full-wave rectified DC to SCR_1 in series with the battery to be charged. With the battery voltage low, SCR_1 is triggered on each half cycle via resistor R_1 and diode CR_1. Under these conditions, the pick-off voltage V_R at the wiper of potentiometer R_3 is less than the breakdown voltage V_Z of zener diode CR_2, and SCR_2 cannot fire. As the battery approaches full charge, its terminal voltage rises, the magnitude of V_R equals V_Z (plus gate voltage required to fire SCR_2), and SCR_2 starts to trigger each half cycle. At first SCR_2 fires at $\pi/2$ radians after the start of each half cycle, coincident with peak supply voltage, peak charging current and maximum battery voltage. As the battery voltage climbs yet higher as charging continues, the firing angle of SCR_2 advances each half cycle until eventually SCR_2 is firing *before* the input sine wave has sufficient magnitude to fire SCR_1. With SCR_2 on first in a half-cycle, the voltage divider action of R_1 and R_2 keeps CR_1 back-biased, and SCR_1 is unable to fire. Heavy charging then ceases. Diode CR_3 and resistor R_4 may be added, if desired, to trickle charge the battery during the normal "off" periods. Heavy charging will recommence automatically when V_R drops below V_Z and SCR_2 stops firing each cycle.

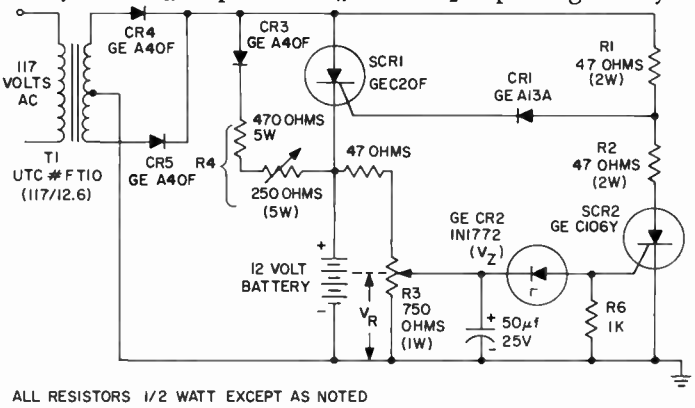


FIGURE 8.12 BATTERY CHARGING REGULATOR

8.6 DC STATIC SWITCH

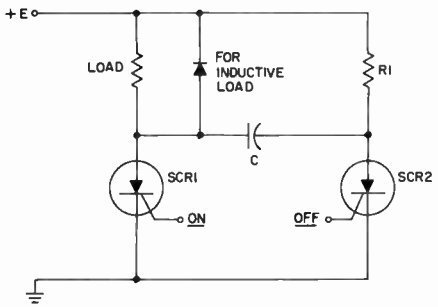


FIGURE 8.13 DC STATIC SWITCH

Figure 8.13 illustrates a static SCR switch for use in a DC circuit. When a low power signal is applied to the gate of SCR_1, this SCR is triggered and voltage is applied to the load. The right hand plate of C charges positively with respect to the left hand plate through R_1. When SCR_2 is triggered on, capacitor C is connected across SCR_1, so that this SCR is momentarily reverse biased between anode and cathode. This reverse voltage turns SCR_1 off and interrupts the load current, provided the gate signal is not applied simultaneously to both gates.

SCR_1 should be selected so that the maximum load current is within its rating. SCR_2 need conduct only momentarily during the turn-off action, it can be smaller in rating than SCR_1. The minimum value of commutating capacitance C can be determined by the following equations:

$$\text{For Resistive Load: } C \geqq \frac{1.5\, t_{off} I}{E}\ \mu fd \tag{8.1}$$

$$\text{For Inductive Load: } C \geqq \frac{t_{off} I}{E}\ \mu fd \tag{8.2}$$

Where t_{off} = Turn-off time of SCR in μ seconds (See specification for inverter-type SCR)

I = Maximum load current (including possible overloads) in amperes at time of commutation

E = Minimum DC supply voltage

The resistance of R_1 should be ten to one hundred times less than the minimum effective value of the forward blocking resistance of SCR_2. This latter value can be derived from the published leakage current curves for the SCR under consideration.

In some cases a mechanical switch may be substituted for SCR_2, to turn off SCR_1 when it (the switch) is momentarily closed. Many other useful variations of this basic DC static switch can be devised, among them the following circuits.

8.7 DC LATCHING RELAY AND POWER FLIP-FLOP

By replacing resistor R_1 with a second driven load, and selecting SCR_2 to suit, the circuit of Figure 8.13 becomes the static analog of a single pole double throw latching relay. In this case commutating capacitor C should be selected on the basis of the heavier of the two loads. By driving the gates with a train of pulses as shown in Figure 8.14, the circuit becomes a high power flip-flop or multivibrator. Sine wave or square wave sources may also be used to drive the gates in this configuration.

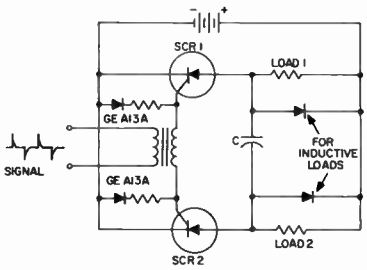


FIGURE 8.14 POWER FLIP-FLOP AND LATCHING RELAY

8.8 PROTECTIVE SCR CIRCUITS

The fast switching characteristic of the SCR makes possible some interesting protective circuits against line transients, excessive voltages, and short circuit currents.

8.8.1 Overvoltage Protection on AC Circuits

Figure 8.15 illustrates a method by which SCR's may be used as a substitute for a dynamic braking contactor to protect a rectifier equipment feeding a regenerative load as typified by a DC shunt motor. An SCR in series with a current limiting resistor R is connected across each of two of the rectifier legs adjacent to one of the AC lines. Under normal operation, neither SCR_1 nor SCR_2 conducts and no energy is lost in the resistors. However, when the DC bus voltage rises to a point determined by the avalanche voltage of the regulating diodes, SCR_1 and SCR_2 are fired, connecting the resistors across the bus thus preventing the DC voltage from damaging the rectifier equipment. As soon as the DC bus voltage drops below the AC supply, SCR_1 and SCR_2 are commutated by the AC line and return to their non-conducting state.

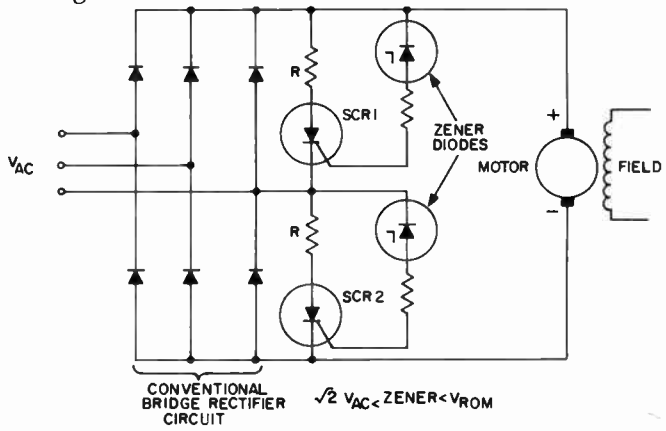


FIGURE 8.15 REGENERATIVE VOLTAGE PROTECTION

Since SCR's switch into their highly conductive state in a matter of microseconds, they can be used for suppressing transient voltages with a much higher rate of rise than could be handled by electromechanical devices such as relays. Figure 8.16 illustrates a circuit that may be employed for general transient protective service on AC lines. When the line exceeds the avalanche voltage of the zener diode, either SCR_1 or SCR_2 triggers, depending on the polarity of the AC line at that instant. Resistor R_1 limits the current to the short term surge capabilities of the SCR's. For the C35, R_1 must limit the one cycle peak current to less than 150 amperes. This loading effect on the circuit drops the transient voltage across line impedance. Alternation of the AC line voltage turns off the current through the conducting SCR at the end of the cycle.

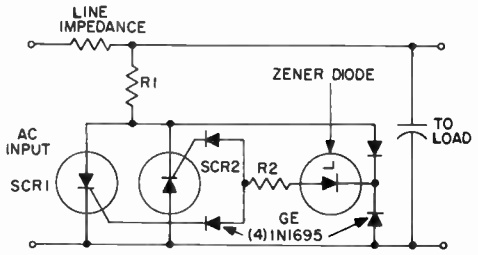


FIGURE 8.16 TRANSIENT VOLTAGE PROTECTION USING SILICON CONTROLLED RECTIFIERS.

8.8.2 SCR Current-Limiting Circuit Breakers

In some phase controlled applications, the fault current due to a short circuit may reach destructive proportions within one-half cycle. This would prohibit use of conventional circuit breakers for protection. Also, in some types of inverters operating on DC it may be desirable to have a fast electronic circuit breaker in the event of loss of commutation in the inverter for any reason.

An SCR current limiting circuit breaker of the type shown in its simplest form in Figure 8.17 will provide these protective functions very nicely. This package can be inserted in series with the DC output of a phase-controlled rectifier or in series with the DC input to an inverter circuit.

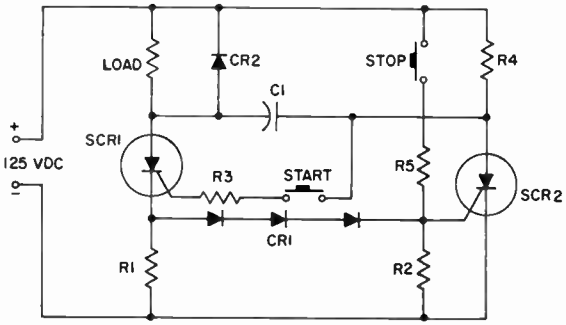


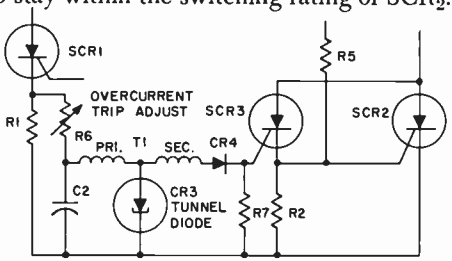
FIGURE 8.17 16 AMPERE DC CIRCUIT BREAKER

The circuit breaker is basically a parallel capacitor commutated flip-flop. When the "Start" button is momentarily depressed, SCR_1 starts to conduct and delivers power to the load provided the load current is above the minimum holding current of SCR_1. Capacitor C_1 then charges to the load voltage

through R_4, the right hand terminal of C_1 being positive with respect to the left hand terminal. When SCR_2 is fired by momentary closing of the "Stop" button, the positive terminal of capacitor C_1 is connected to the cathode of SCR_1, reversing the polarity across this SCR and turning it off. This interrupts the flow of load current and opens the circuit. SCR_2 will also be fired by the voltage developed across R_1 by load current if this exceeds the forward voltage drop of the string of series diodes CR_1 plus the gate firing requirements of SCR_2. By adjustment of the value of R_1 and by selecting the proper number of series diodes CR_1, the circuit can be made to trip out and interrupt overload or fault current at any predetermined level. For a more consistent tripping level under temperature variations, a zener diode can be substituted in place of all but one of the series diodes at CR_1. For still more precise tripping, a UJT overcurrent sensor can be used.

The characteristics of the germanium tunnel diode are also very useful in developing a gate signal when a specific level of current is exceeded. The tunnel diode has a very stable peak current at which it switches from a low resistance to a relatively high resistance. This, combined with a very low voltage drop, makes it almost ideal for this type of application. A tunnel diode overcurrent detecting network for the circuit breaker of Figure 8.17 is shown in Figure 8.18. Main load current flows through SCR_1 and R_1. Part of the load is shunted through R_6, tunnel diode CR_3, and the primary winding of T_1, R_1 and R_6 are selected so that less than 20 ma. flows through the tunnel diode at maximum rated load. Under this condition CR_3 remains in its low resistance state. If the main load current rises to the point where more than 20 ma. flows through CR_3, it switches instantaneously to its high resistance state. If the current through the tunnel diode is maintained constant through the switching interval, the voltage across it increases about five-fold. This sudden change in voltage across CR_3 induces a pulse of voltage in the primary of T_1 which is stepped up by autotransformer action and applied to the gate of SCR_3, thereby tripping the circuit breaker. The tripping point is stable within a few percent over a wide temperature range and is independent of the firing characteristics of SCR_3.

The component values in Figure 8.17 apply for a 125 volt DC system. When using the C40 SCR, the tripping current level should not exceed 100 amperes in order to stay within the switching rating of SCR_2.



SCR3 - GE C106B
R1 = $-3/I_{trip}$ OHMS, NON-INDUCTIVE
R6 - 250 OHM LINEAR POT
R7 - 1000 OHMS, 1/2 WATT
C2 - 2MFD, 10 VOLT
CR3 - GERMANIUM TUNNEL DIODE GE IN3150
CR4 - GE IN91
T1 - AIR CORE TRANSFORMER, 1/4" DIA.,
P = 50T, S = 500T, # 26AWG

FIGURE 8.18 TUNNEL DIODE SENSING NETWORK FOR FIGURE 8.17

Because of the fast switching action of SCR's, short circuit current can be interrupted long before it reaches destructive levels. In typical stiff systems with rates of fault current rise on the order of 10 million amperes per second, this type of switch has limited the peak fault current to less than 50 amperes and has interrupted the fault in as little as 20 microseconds after its inception.

In some high reliability applications the flip-flop action of this circuit can be used as a high speed transfer switch in the event of a fault in one load. For instance, both the load in series with SCR_1 and the load represented by R_4 in Figure 8.17 could be DC motors, driving a common load. If the main drive motor in series with SCR_1 should fail short, it would be disconnected from the line and power would be applied to the standby motor R_4 within a matter of microseconds after the fault occurred.

C_1 must have sufficient capacitance to commutate the fault current at the point of tripping. Expressed another way, it must reverse bias SCR_1 for at least 12 microseconds if SCR_1 is to reliably recover its open state and block further flow of fault current. If SCR's other than the C40 are employed in this circuit C_1 must be adjusted to provide the necessary turn-off time for the particular SCR type chosen.

8.8.3 High Speed Switch or "Electronic Crowbar"

A form of "electronic crowbar," shown in Figure 8.19, has proved very useful for protecting DC circuits against input line voltage transients and short circuit load conditions. If the DC supply exceeds the desired maximum value as determined by the setting of potentiometer R_1, the voltage at the emitter of UJT_1 exceeds the peak point voltage causing UJT_1 to fire which in turn triggers the SCR. The full supply voltage is then applied to the circuit breaker trip coil causing the circuit breaker to open the main DC supply bus. Besides increasing the speed of the circuit breaker action this circuit instantly loads down the DC bus, preventing the voltage on the load from rising until the circuit breaker has time to operate. The circuit also protects the load and the supply against short circuit conditions by monitoring the current through resistor R_3. When the voltage across R_3 exceeds the desired maximum value as determined by the setting of potentiometer R_2 the voltage at the emitter of UJT_2 exceeds the peak point voltage, causing UJT_2 and the SCR to fire as before. Due to the stable firing voltage of the UJT the trip voltage across R_3 can be very low, a value in the range from 100 millivolts to 500 millivolts being suitable for most applications. If only overvoltage protection is desired the circuit of Figure 8.19 can be simplified by eliminating UJT_2 and its associated circuitry. Similarly, if only overcurent protection is desired UJT_1 and its associated circuitry can be eliminated.

In the circuit of Figure 8.19 rectifier CR_1 and capacitor C_3 are used to provide filtering against negative voltage transients which would otherwise result in false tripping of the circuit. The values of potentiometer R_1 and R_2 are chosen to have appropriate time constants with C_1 and C_2 so as to give the desired voltage-time response in the tripping action.

The SCR is ideal for this type of circuit because of its ability to switch on within a few microseconds after being triggered.

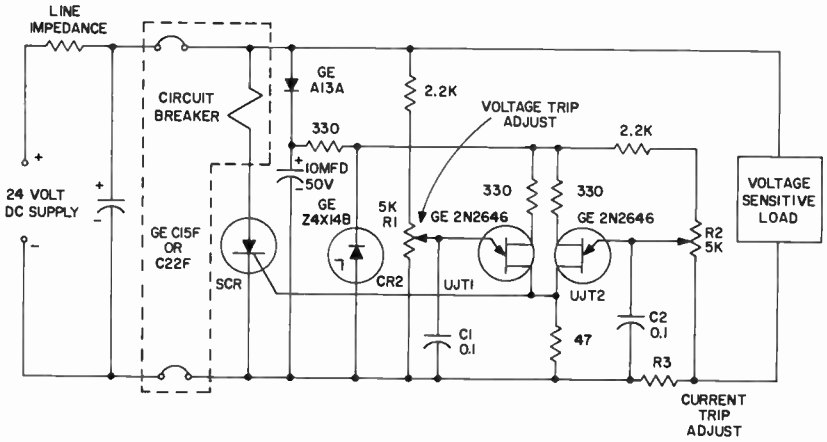


FIGURE 8.19 ELECTRONIC CROWBAR PROTECTION OF DC CIRCUITS AGAINST OVERVOLTAGE AND/OR OVERCURRENT.

For higher capacity circuits, the C35F or C50F SCR's can be substituted for the C22F shown. With the C50F SCR this circuit is capable of carrying momentary currents as high as 2000 amps for 2 milliseconds without damage to the SCR.

8.9 FLASHER CIRCUITS

Flasher circuits for incandescent lamps are widely used in a variety of applications such as traffic lights, navigational beacons, aircraft beacons, and illuminated signs. The SCR and the triac are ideally suited for this type of application since they can function over a wide range of current and voltage with a much higher degree of reliability than the commonly used electromechanical systems. The SCR and the triac also offer an advantage over power transistors because they do not require an excessive derating of current in order to handle the high inrush currents of incandescent lamps. The UJT and the transistor however make an ideal partner as trigger devices for the SCR and triac in this type of application since they permit an economical method for obtaining a wide frequency range and a high degree of frequency stability. More information on flashers will be found in Reference 4.

8.9.1 DC Flashers

The circuit shown in Figure 8.20 has been chosen to illustrate the basic principles of an SCR/UJT flasher which can be easily simplified or modified to meet specific application requirements.

Unijunction transistor Q_1 operates as a relaxation oscillator, delivering a train of trigger pulses to the two SCR gates via resistor R_1. Assume SCR_2 is "on" and the lamp is energized. When the next trigger pulse comes along it triggers SCR_1 and SCR_2 is turned off by the commutation pulse coupled to its anode via capacitor C_2. Because the commutation pulses have longer duration than the trigger pulses, SCR_2 cannot be re-triggered inadvertently at this time. SCR_2 is re-triggered properly by the *next* trigger pulse from R_2. "Lock-up" (failure to flash caused by both SCR's being on together) is prevented by making SCR_1's turn off independent of the commutating capacitor. This is done by operating SCR_1 in a "starved" mode, that is by making resistor R_2 so large that SCR_2 is unable to remain "on", except to discharge C_2. During the remainder of the cycle SCR_1 is off, and C_2, therefore, is always able to develop commutating voltage for SCR_2. With the components shown, the flash rate is adjustable by potentiometer R_3 within the range 36 flashes per minute to 160 flashes per minute.

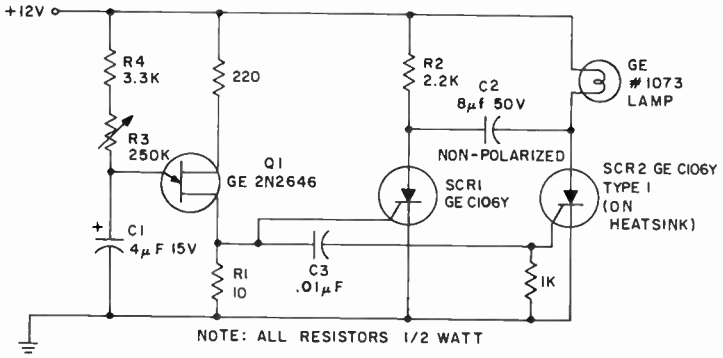


FIGURE 8.20 DC LOW POWER FLASHER

8.9.2 AC Flasher

For heavy load requirements, the DC flashers have the disadvantage of requiring a large commutating capacitor. In such applications, the use of AC flashers ends up being more economical. Figure 8.21 illustrates a power flip-flop flasher circuit that can handle two independent loads up to 1 KW each. Transformer T_1, diodes CR_1 through CR_4, resistor R_1 and capacitor C_1 provide the DC supply to the free running unijunction oscillator and the transistor flip-flop of Q_2, Q_3. The interbase voltage for Q_1 is taken directly from the positive side of the bridge rectifier in order to synchronize the free running unijunction oscillator with the supply frequency. The negative going output pulses developed across R_4 trigger the transistors of the flip-flop which alternately turn the triacs on and off. The flashing rate is determined by the time constant of R_2, R_3 and C_2.

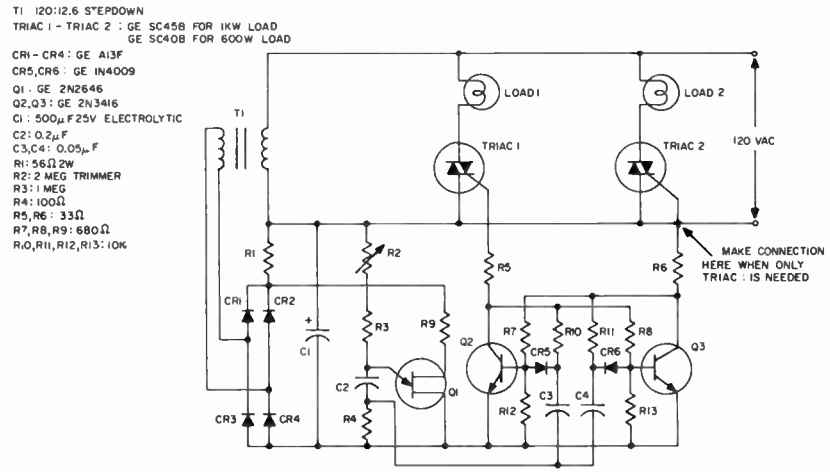


FIGURE 8.21 AC POWER FLASHER

8.10 RING COUNTERS

A ring counter may be considered as a circuit that sequentially transfers voltage from one load to the next, when a number of loads are connected in parallel from a common supply. Transfer along the string proceeds always in the same direction, and each transfer is initiated by pulsing a common input line. The ring counter is an extremely useful tool in digital applications, and SCR ring counters in particular excel in low speed applications that require high voltage, high current or both. As an example a ten stage SCR ring counter can function as a decade counter with direct lamp or glowtube (Nixie) readout. The circuit of Figure 8.22 is a three stage cathode coupled ring counter, suitable for driving high voltage loads up to 50 mA. Additional stages may be added as required. Assume SCR_1 is conducting load current, and SCR_2 and SCR_3 are both blocking. Capacitors C_3 and C_1 charge to the supply voltage through R_3/R_{L2} and R_1/R_{L3} respectively, while capacitors C_5 and C_6 charge through R_{L2} and R_{L3}. Because SCR_1 is conducting, C_2 and C_4 cannot charge. When a shift pulse arrives at the shift line only SCR_2 can be triggered, since its gate steering diode CR_2 is the only diode not reverse biased by a pre-charged capacitor. In any ring counter only the SCR following the conducting SCR will trigger. As SCR_2 turns on, capacitor C_5 is connected across R_4, which drives the common cathode line momentarily to the supply voltage, reverse biasing SCR_1 and forcing it to turn off. When the next shift pulse arrives, SCR_3 turns on and SCR_2 turns off and so on. The advantage of the cathode coupled ring counter is that undistorted square waves free from commutation transients appear across each load. Its major disadvantage is that relatively large value commutating capacitors (C_4, C_5, C_6) are required with consequent limitations on circuit speed. In applications where commutation transients can be tolerated and/or higher speed operation is required (lamp driving circuits for instance), the ring counter circuit can be modified as follows:

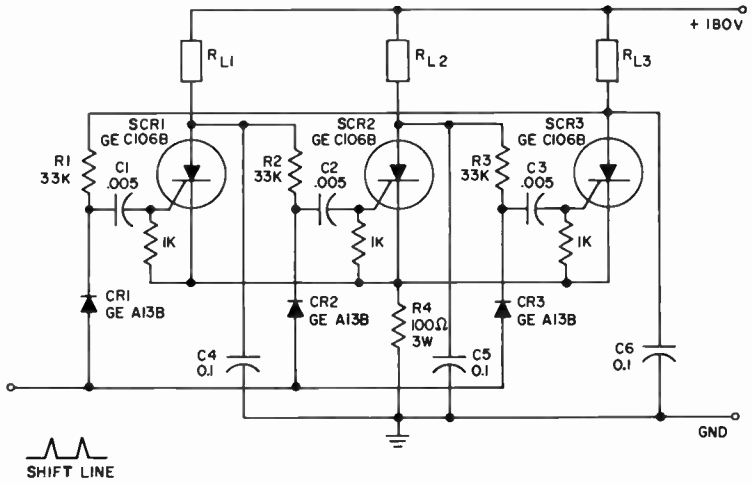


FIGURE 8.22 CATHODE COUPLED RING COUNTER

1. Remove resistor R_4, and ground the common cathode line.
2. Remove C_4, C_5, and C_6.
3. Connect a .005 μf capacitor between each pair of SCR anodes.

Figure 8.23 shows the modified circuit being used to drive a #6844A Nixie Decade Readout Tube.[5]

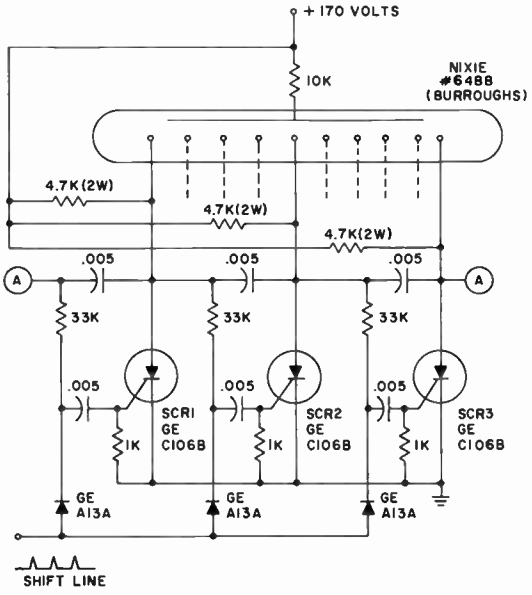
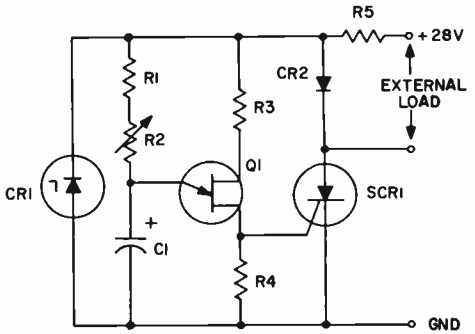


FIGURE 8.23 ANODE COUPLED RING COUNTER (DECADE READOUT)

8.11 TIME DELAY CIRCUITS

Time delay circuits are used frequently in industrial controls and aircraft and missile systems to apply or remove power from a load a predetermined time after an initiating signal is applied. Cascaded time delay circuits can be used to sequentially perform a series of timed operations.



R1 - 2.2K, 1/2 WATT
R2 - 1K TO 500K LINEAR POT
R3 - 150Ω, 1/2 WATT
R4 - 27, Ω , 1/2 WATT
R5 - 560Ω, 2 WATT
C1 - 0.2 TO 100 MFD, 15V
SCR1 - GE C22F OR C11F
CR1 - 18V, 10%, 1 WATT ZENER, IN1776
CR2 - GE A13A
Q1 - GE 2N1671B

FIGURE 8.24 PRECISION SOLID STATE DC TIME DELAY CIRCUIT

8.11.1 UJT/SCR Time Delay Relay

Figure 8.24 illustrates an extremely simple yet accurate and versatile solid state time delay circuit. The operating current and voltage of the circuit depend only on the proper choice of the SCR. Resistor R_5 and Zener diode CR_1 provide a stable voltage supply for the UJT. Initially SCR_1 is off and there is no voltage applied to the load. Timing is initiated either by applying supply voltage to the circuit or by opening a shorting contact across C_1. The timing capacitor C_1 is charged through R_1 and R_2 until the voltage across C_1 reaches the peak point voltage of the UJT at which time the UJT fires, generating a pulse across R_4 which triggers SCR_1. The full supply voltage minus the SCR drop then appears across the external load terminals. Holding current for SCR_1 is provided by the current through R_5 and CR_2. Thus the external load may be removed or connected at any time without affecting the performance of the circuit. When SCR_1 triggers, the voltage across the UJT drops to less than 2 volts due to the clamping action of CR_2. This acts to rapidly set and maintain a low voltage on C_1 so that the time interval is maintained with reasonable accuracy if the circuit is rapidly recycled. For the highest accuracy, however, additional means must be used to rapidly and accurately set the initial voltage on C_1 to zero at the beginning of the timing cycle. A pair of mechanical contacts connected across C_1 is ideal for this purpose.

The time delay of the circuit depends on the time constant $(R_1 + R_2)$ C_1 and can be set to any desired value by appropriate choice of R_1, R_2, and C_1. The upper limit of time delay which can be achieved depends on the

required accuracy, the peak point current of the UJT, the maximum ambient temperature, and the leakage current of the capacitor and UJT (I_{EO}) at the maximum ambient temperature. The absolute upper limit for the resistance $R_1 + R_2$ is determined by the requirement that the current to the emitter of the UJT be large enough to permit it to fire (i.e., be greater than the peak point current) or

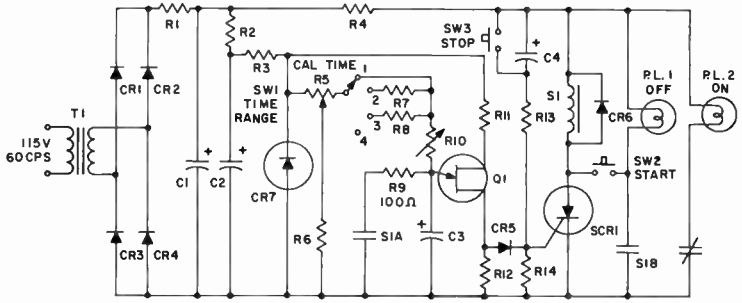
$$R_1 + R_2 < \frac{(1 - \eta)\, V_1}{\frac{25 I_p}{V_1} + I_c} \tag{8.3}$$

where η is the maximum value of intrinsic standoff ratio, V_1 is the minimum supply voltage on the UJT, I_p is the maximum peak point current measured at an interbase voltage of 25 volts, and I_c is the maximum leakage current of the capacitor at a voltage of ηV_1. If high values of capacitance are required it is desirable to use stable, low leakage types of tantalytic capacitors. If tantalytic or electrolytic capacitors are used it is necessary to consider forming effects which will cause the effective capacitance and hence the period to change as a function of the voltage history of the capacitor. These effects can be reduced by applying a low bias voltage to the capacitor in the standby condition.

The resistor R_3 can serve as a temperature compensation for the circuit, increasing the value of R_3 causes the time delay interval to have a more positive temperature coefficient. The over-all temperature coefficient can be set exactly zero at any given temperature by careful adjustment of R_3. However, ideal compensation is not possible over a wide range because of the nonlinear effects involved. To reset the circuit in preparation for another timing cycle SCR_1 must be turned off either by momentarily shorting it with a switch contact or by opening the DC supply.

8.11.2 AC Powered Time Delay Relay

Figure 8.25 illustrates a time delay circuit using a relay output with a push button initiation of the timing sequence. In the quiescent state SCR_1 is on and relay S_1 is energized. Contact S_1A is closed, shorting out the timing capacitor C_3. To initiate the timing cycle push button switch SW_2 is momentarily closed which shorts SCR_1 through contact S_1B causing SCR_1 to turn off. When SW_2 is released S_1 is deenergized and the timing sequence begins. The particular configuration of SW_2 and S_1B is used to prevent improper operation in case SW_2 is closed again during the timing cycle. Capacitor C_3 is charged through R_5 and R_{10} until the voltage across C_3 reaches the peak point voltage of Q_1 causing Q_1 to fire. The positive pulse generated across R_{12} triggers SCR_1 which pulls in the relay and ends the timing cycle. The timing cycle can be terminated at any time by push button switch SW_3 which causes current to flow in R_{13} thus triggering SCR_1. Capacitor C_4 supplies current through R_{13} during the instant after the supply is turned on thus triggering SCR_1 and setting the circuit in the proper initial state.



R1 - 2Ω, 1 WATT
R2, R3 - 330Ω, 1/2 WATT
R4 - 35Ω, 5 WATT
R5 - 2.5K, LINEAR POT
R6 - 25K, 1/2 WATT
R7 - 100K, 1/2%, 1/2 WATT
R8 - 200K, 1/2%, 1/2 WATT
R9 - 100Ω, 1/2 WATT
R10 - 100K, 10 TURN HELIPOT
R11 - 150Ω, 1/2 WATT
R12 - 18Ω, 1/2 WATT
R13 - 1.2K, 2 WATT
R14 - 100Ω, 1/2 WATT
C1 - 500μF0, 50V
C2 - 100μF0, 50V
C3 - 100μF0, 20V TANTALUM
C4 - 10μF0, 50V
SCR1 - GE C15F OR C11F
CR1 - CR6 - G E A13A
CR7 - 18V, 10% 1 WATT ZENER
Q1 - GE 2N16718
S1 - GE CR2791G122A4 4POT RELAY
PL1, PL2 - GE 1447, 24V LAMP
T1 - 115V/25V 1A TRANSFORMER

FIGURE 8.25 VARIABLE TIME CONTROL CIRCUIT

The timing interval is determined by the setting of a precision ten turn Helipot R_{10} which may be set from 0.25 to 10.25 seconds in increments of 0.01 second. The initial setting of 0.25 seconds takes into account the added series resistance of the time calibration potentiometer R_5. Additional series resistance of 100K and 200K may be added by SW_1 to extend the time range by 10 seconds and 20 seconds. A fourth position of SW_1 open circuits the timing resistors and thus permits unrestricted on-off control of the circuit.

Tests of the circuit have shown an absolute accuracy of 0.5% after initial calibration and a repeatability of 0.05% or better.

8.11.3 Ultra-Precise Long Time Delay Relay

Predictable time delays from as low as 0.3 milliseconds to over 3 min-

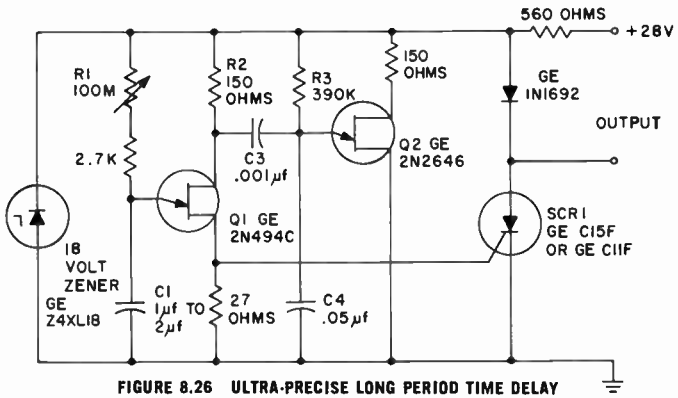


FIGURE 8.26 ULTRA-PRECISE LONG PERIOD TIME DELAY

utes are obtainable from the circuit of Figure 8.26, without resorting to a large value electrolytic-type timing capacitor. Instead, a stable low leakage paper or mylar capacitor is used and the peak point current of the timing UJT (Q_1) is effectively reduced, so that a large value emitter resistor (R_1) may be substituted. The peak point requirement of Q_1 is lowered up to 1000 times, by pulsing its upper base with a ¾ volt negative pulse derived from free-running oscillator Q_2. This pulse momentarily drops the peak point voltage of Q_1, allowing peak point current to be supplied from C_1 rather than via R_1. Pulse rate of Q_2 is not critical, but it should have a period τ that is less than .02 ($R_1 \cdot C_1$). With $R_1 = 2000$ megohms and $C_1 = 2\ \mu f$ (mylar), the circuit has given stable time delays of over one hour. R_2 is selected for best stabilization of the firing point over the required temperature range. Because the input impedance of the 2N494C UJT is greater than 1500 megohms before it is fired, the maximum time delay that can be achieved is limited mainly by the leakage characteristics of C_1.

8.12 NANOAMPERE SENSING CIRCUIT WITH 100 MEGOHM INPUT IMPEDANCE

The circuit of Figure 8.27 may be used as a sensitive current detector, or as a voltage detector having high input impedance. A sampling technique similar to that described in the previous section is used to give an input current sensitivity (I_{IN}) of less than 35 nanoamperes. Input impedance is better than 100 megohms.

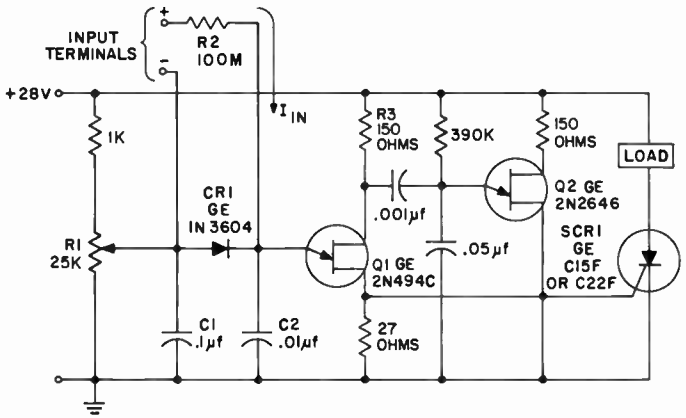


FIGURE 8.27 NANOAMPERE SENSING CIRCUIT

Current gain between output and input of the circuit as shown is greater than (200×10^{-6}).

Resistor R_1 is adjusted so that the circuit will not fire in the absence of the current input signal I_{IN}. I_{IN} then charges C_2 through the 100 megohm input resistor R_2 towards the emitter firing voltage of Q_1. R_2 however, cannot supply the peak point current (2 μA) necessary to fire Q_1, and this current is obtained from C_2 itself by dropping Q_1's firing voltage momentarily below V_{C2}. Relaxation oscillator Q_2 supplies a series of .75 volt negative pulses to

base two of Q_1 for this purpose. The period of oscillation of Q_2 is not critical but should be less than .02 times the period of Q_1. Capacitor C_2 can be kept small for fast response time because C_1 stores the energy required to fire SCR_1. Rapid recovery is possible because both capacitors are charged initially from R_1. Some temperature compensation is provided by the leakage current of CR_1 subtracting from the leakage current of Q_1. Further compensation is obtainable by adjusting the value of R_3. A floating power supply for the UJT trigger circuit with pulse transformer coupling from Q_1 to SCR_1, enables one of the two input terminals to be grounded, where this may be desirable.

8.13 MISCELLANEOUS SWITCHING CIRCUITS USING THE G.E. C5, C6, AND C106 LOW CURRENT SCR'S

The C5, C6 and C106 series of SCR's have a high gate sensitivity. Gate triggering can therefore be achieved from such low level elements as thermistors and light sensitive resistors. When used as a gate amplifier for the higher rated SCR's, either of these devices makes possible a multitude of solid state thyratron tube analogues. The C5 SCR is also suitable for use as a very high voltage remote-base transistor. For more detailed application information on the low current SCR's, see Reference 5.

8.13.1 Dual Output, Over-Under Temperature Monitor

The circuit of Figure 8.28 is ideal for use as an over-under temperature monitor, where its dual output feature can be used to drive "HIGH" and "LOW" temperature indicator lamps, relays, etc.

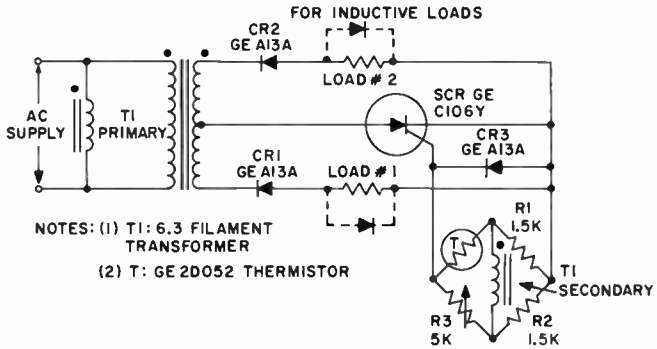


FIGURE 8.28 TEMPERATURE MONITOR

T_1 is a 6.3 volt filament transformer whose secondary winding is connected inside a four arm bridge. When the bridge is balanced, its AC output is zero, and the C5 (or C7) receives no gate signal. The bridge's DC resistance is sufficiently low to stabilize the SCR during forward blocking periods.* If now the bridge is unbalanced by raising or lowering the thermistor's ambient temperature, an AC voltage will appear across the SCR's gate cathode terminals. Depending in which sense the bridge is unbalanced, positive gate voltage will be in phase with, or 180° out of phase with the AC supply. If

*See Section 4.3.6 "Negative Gate Biasing."

positive gate voltage is in phase, SCR will deliver load current through diode CR_1 to load (1), diode CR_2 blocking current to load (2). Conversely, if positive gate voltage is 180° out of phase, diode CR_2 will conduct and deliver power to load (2), CR_1 being reverse biased under these conditions. CR_3 prevents excessive negative voltage from appearing across the SCR's gate/cathode terminals. With component values shown, the circuit will respond to changes in temperature of approximately 1–2°C. Substitution of other variable-resistance sensors, such as cadmium sulphide light dependent resistors (LDR) or strain gauge elements, for the thermistor shown is of course permissible. The balanced bridge concept of Figure 8.28 may also be used to trigger conventional SCR-series load combinations. As a low power temperature controller for instance, a C5 could be used to switch a heater element, with a thermistor providing temperature feedback information to the trigger bridge.

8.13.2 Mercury Thermostat/SCR Heater Control

The mercury-in-glass thermostat is an extremely sensitive measuring instrument, capable of sensing changes in temperature as small as 0.1°C. Its major limitation lies in its very low current handling capability—for reliability and long life, contact current should be held below 1 mA. In the circuit of Figure 8.29 the General Electric C5B or C106B SCR serve as both current amplifier for the Hg thermostat and as the main load switching element.

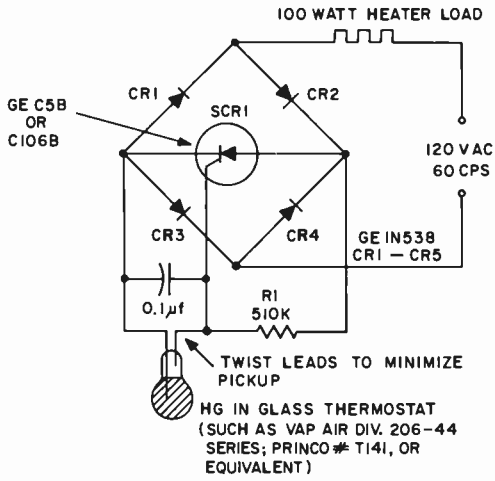


FIGURE 8.29 TEMPERATURE CONTROLLER

With the thermostat open, the SCR will trigger each half cycle and deliver power to the heater load. When the thermostat closes, the SCR can no longer trigger, and the heater shuts off. Maximum current through the thermostat in the closed position is less than 250 μA rms.

8.13.3 Proximity Switch

Figure 8.30 is a solid state proximity switch. Capacitor C_1, resistors R_1, R_2, and the sensor plate ("capacitor" C_2) form a capacitive voltage divider connected directly across the AC supply. The AC voltage across C_1 will depend on the ratio (C_1/C_2) and the line voltage. The capacitance of C_2 in turn depends on the proximity to the sensor plate of any reasonably conductive and grounded object (metals, human body, etc.). As soon as the voltage across C_1 exceeds the breakover potential of the 5AH neon, capacitors C_1 and C_2 discharge through the base of transistor Q_1. Q_1 amplifies this discharge current and supplies the necessary gate drive to turn SCR_1 on, which energizes the load.

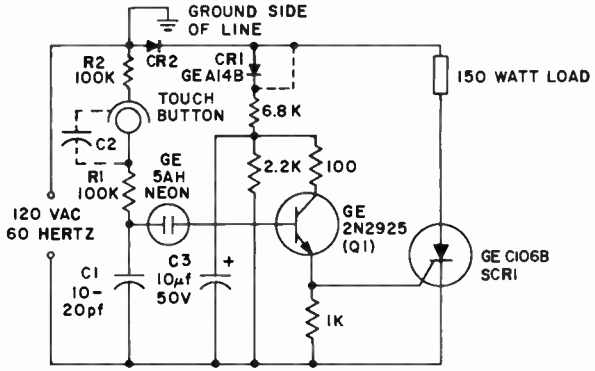


FIGURE 8.30 PROXIMITY SWITCH

The load will remain energized as long as the button is touched. When the button is released, the load is de-energized. Latching action can be accomplished by removing CR_1 as shown in Figure 8.30 and replacing with a short circuit. Reset must then be accomplished by an auxiliary contact in series with the SCR. This circuit is ideally suited for use in elevators (both for door safety controls and floor selector button arrays), supermarket door control, bank-safe monitors, flow switch actuation, and conveyor belt counting systems.

8.13.4 Thyratron Replacement

The C5 makes an ideal trigger element for the larger size SCR's. (See also Section 4.19.) Such a combination possesses many of the characteristics of a thyratron gas tube. A thyratron tube is characterized by a very high signal input impedance, low pick-up and drop-out currents, and good power handling capabilities. On the other hand, it is fragile, requires filament power, is frequency limited by a long deionization time, and has a fairly high forward drop. While the solid-state equivalents to this device, using the C5, can match the thyratron in input impedance, current handling ability and low pick-up current, they possess none of the gas tube's limitations. At the present time, however, the maximum forward blocking voltage attainable using a single C5 is 400 volts. This can be increased by series connecting additional SCR's (see Section 6.1).

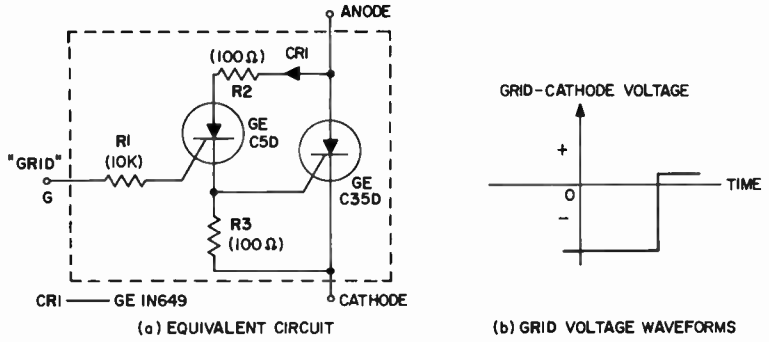


FIGURE 8.31 SIMPLE THYRATRON REPLACEMENT

Referring to Figure 8.31; with a negative potential on grid terminal "G", stabilizing gate bias is provided thru R1 and R3 for the C5. When the "Grid" is driven positive however, a maximum current of 200 microamps will trigger the smaller SCR into conduction. The C35D is triggered in turn by the C5, and can conduct up to 25 amps rms load current. With the voltage grades shown, the "device" is capable of blocking voltages up to 400 volts. Over-all pick-up current is determined by the C5 rather than by the C35, a useful feature when the "thyratron" is operating into a highly inductive load. Diode CR_1 prevents transistor action in the C5 if positive grid voltage should coincide with negative anode potential.

8.14 SWITCHING CIRCUITS USING THE C5 SCR AS A REMOTE-BASE TRANSISTOR

8.14.1 "Nixie"® and Neon Tube Driver

The C5 SCR, when biased as a remote-base transistor, makes an excellent high voltage transistor suitable for driving Nixie, neon and other type of high voltage digital readout displays. Collector voltage rating of the equivalent transistor equals or exceeds the $V_{BR(FX)}$ rating of the parent SCR (400 volts) while the common emitter current gain is approximately two (2). The circuit of Figure 8.32 is self-explanatory; note however the connections to the C5 terminals. Where a memory feature is desirable (pulse initiation with load remaining energized until reset externally), the same basic circuit may be used, but with the C5 connected conventionally as an SCR.

® Trademark Burroughs Corporation.

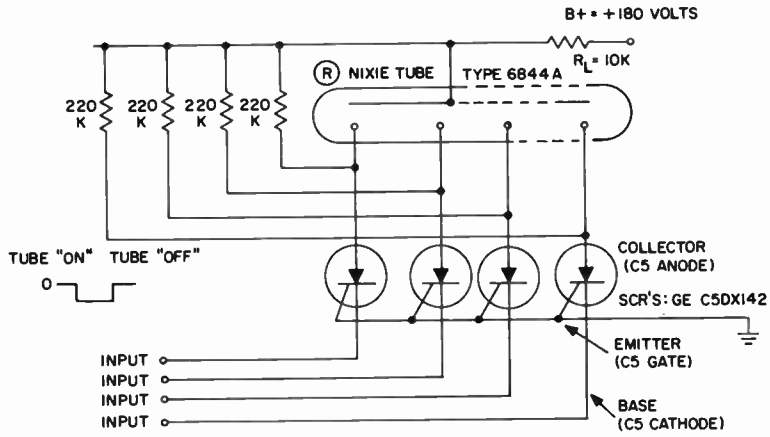


FIGURE 8.32 TRANSISTORIZED NIXIE® DRIVER

8.14.2 Electroluminescent Panel Driver

Either of the circuits of Figure 8.33 may be used to drive the elements of an electroluminescent display panel, depending on the input logic required. Here, the high voltage capabilities of the C5 SCR are again combined with its usefulness as a transistor, in this case a *symmetrical* transistor, to control full-wave AC drive at high voltage and frequency, low current.

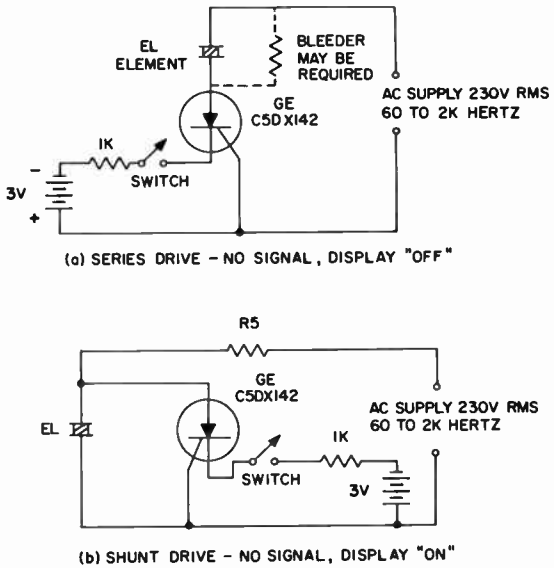


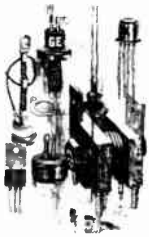
FIGURE 8.33 ELECTROLUMINESCENT PANEL DRIVER

REFERENCES

1. "Using the Triac for Control of AC Power," J. H. Galloway, General Electric Company, Auburn, New York, Application Note 200.35.*
2. "Temperature Controls Incorporating Zero Voltage Switching," J. L. Brookmire, General Electric Company, Auburn, New York, Application Note 200.45.*
3. "Regulated Battery Chargers Using the Silicon Controlled Rectifier," D. R. Grafham, General Electric Company, Auburn, New York, Application Note 200.33.*
4. "Flashers, Ring Counters and Chasers," A. A. Adem, General Electric Company, Auburn, New York, Application Note 200.48.*
5. "Using Low Current SCR's," D. R. Grafham, General Electric Company, Auburn, New York, Application Note 200.19.*

*Refer to Chapter 22 for availability and ordering information.

9 AC PHASE CONTROL



9.1 PRINCIPLE OF PHASE CONTROL

"Phase Control" is the process of rapid ON-OFF switching which connects an AC supply to a load for a controlled fraction of each cycle. This is a highly efficient means of controlling the average power to loads such as lamps, heaters, motors, DC supplies, etc. Control is accomplished by governing the phase angle of the AC wave at which the thyristor is triggered. The thyristor will then conduct for the remainder of that half-cycle.

There are many forms of phase control possible with the thyristor, as shown in Figure 9.1. The simplest form is the half-wave control of Figure 9.1(a) which uses one SCR for control of current flow in one direction only.

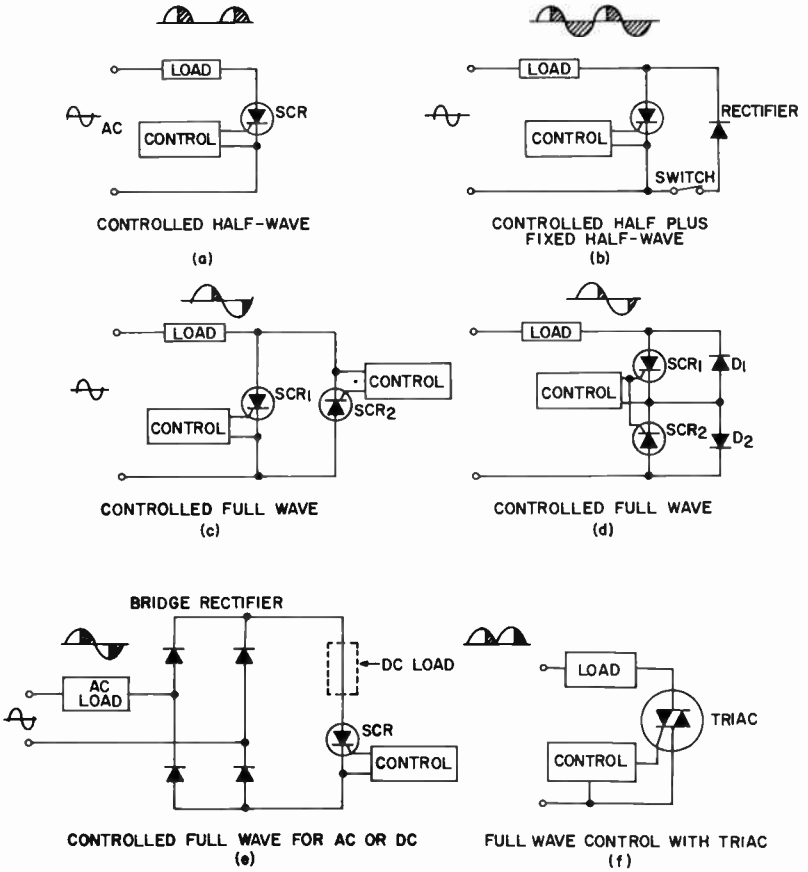


FIGURE 9.1 BASIC FORMS OF AC PHASE CONTROL

This circuit is used for loads which require power control from zero to one-half of full-wave maximum and which also permit (or require) direct current. The addition of one rectifier, Figure 9.1(b), provides a fixed half-cycle of power which shifts the power control range to half-power minimum and full-power maximum but with a strong DC component. The use of two SCR's, Figure 9.1(c), controls from zero to full-power and requires isolated gate signals, either as two control circuits or pulse-transformer coupling from a single control. Equal triggering angles of the two SCR's produce a symmetrical output wave with no DC component. Reversible half-wave DC output is obtained by controlling symmetry of triggering angle.

An alternate form of full-wave control is shown in Figure 9.1(d). This circuit has the advantage of a common cathode and gate connection for the two SCR's. While the two rectifiers prevent reverse voltage from appearing across the SCR's, they reduce circuit efficiency by their added power loss during conduction.

The most flexible circuit, Figure 9.1(e), uses one SCR inside a bridge rectifier and may be used for control of either AC or full-wave rectified DC. Losses in the rectifiers, however, make this the least efficient circuit form, and commutation is sometimes a problem (see Section 9.3). On the other hand, using one SCR on both halves of the AC wave is a more efficient utilization of SCR capacity, hence the choice of circuit form is based on economic factors as well as performance requirements.

By far the most simple, efficient and reliable method of controlling AC power is the use of the bidirectional triode thyristor, the triac, as shown in Figure 9.1(f). Triac characteristics are discussed in Chapter 7. The fact that the triac is controlled in both directions by one gate and is self-protecting against damage by high-voltage transients has made it the leading contender for 120 and 240 VAC power control up to 3.6 KW at this writing.

9.2 ANALYSIS OF PHASE CONTROL

Rectifiers and SCR's are rated in terms of *average* current since this is easily found by a DC ammeter. Most AC loads are more concerned, however, with the *RMS*, or effective, current.

Figures 9.2 and 9.3 show the relationships as a function of phase-angle, α, at turn-on, of average, RMS, and peak voltages, as well as power in a resistive load. Since the SCR is a switch, it will apply this voltage to the load, but the value of current will depend on load impedance.

As an example of the use of these charts, suppose it is desired to operate a 1200 watt resistive load, rated at 120 volts, from a 240 volt supply. Connection of this load directly to the supply would result in 4800 watts, therefore the desired operation is at ¼ maximum power capability. We may use, for this case, either a half-wave or full-wave form of control circuit.

Starting with the half-wave case and Figure 9.2, the ¼ power point is a triggering phase angle of 90 degrees. Peak output voltage E_{PO} is equal to peak input voltage, 1.41 × 240 volts or 340 volts. Oddly enough, the RMS voltage is .353 × 340 volts or 120 volts. Average voltage is .159 × 340 volts or 54 volts, which would be indicated by a DC voltmeter across the load. Since the load resistance is 12 ohms ($120^2/1200$), peak current is 340/12 = 28.3 amperes; RMS current is 120/12 = 10 amperes; and average current is 54/12 = 4.5 amperes, which would be indicated by a DC ammeter in series with the load. Power is $E_{RMS} \times I_{RMS}$ (since the load is pure resistance) which is 1200 watts. Note carefully that $E_{AVG} \times I_{AVG}$ is 243 but is *not* true power

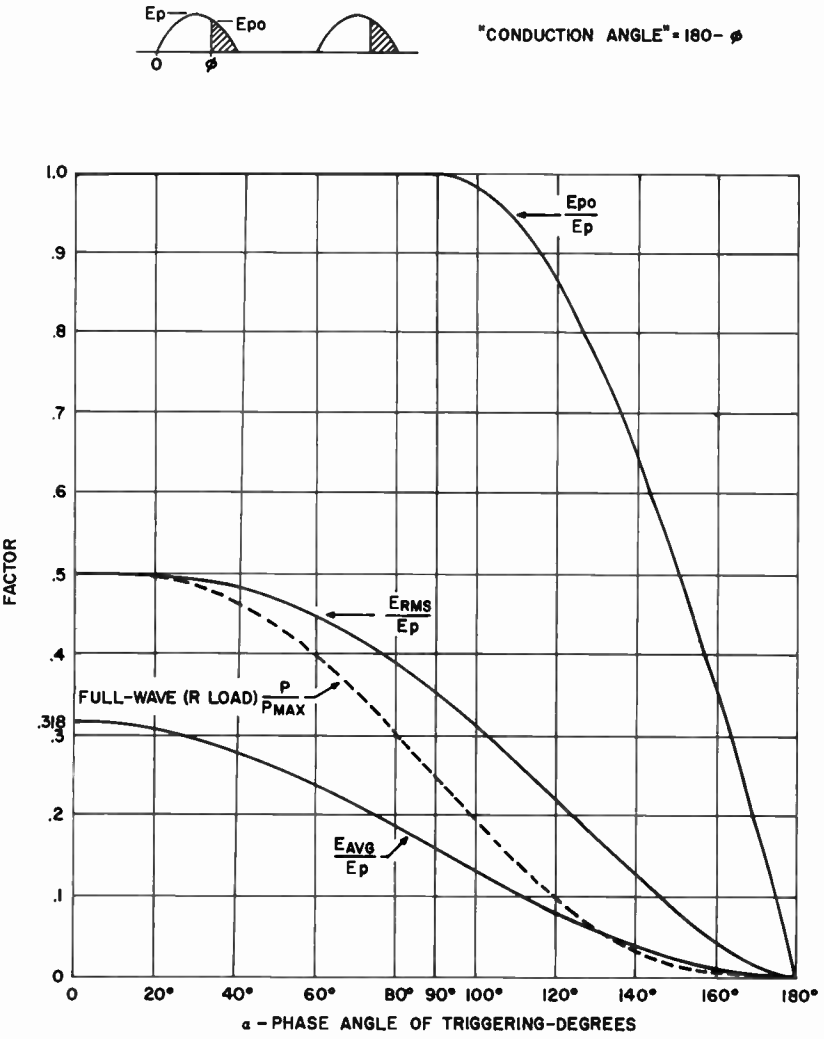


FIGURE 9.2 HALF-WAVE PHASE CONTROL ANALYSIS CHART

in the load. The SCR must be rated for 4.5 amperes (average) at a conduction angle (180 − α) of 90 degrees. Furthermore, the load must be able to accept the high peak voltage and current, and the line "power-factor" is 0.5 (if defined as $P_{LOAD} \div E_{LINE} \times I_{LINE\ RMS}$).

The other alternative is a symmetrical full-wave circuit, such as Figure 9.1(c), for which Figure 9.3 is used. The phase-angle of triggering is found to be 113 degrees for ¼ power. Peak voltage is .92 × 340 = 312 volts, only a slight reduction from the half-wave case. RMS voltage is again .353 × 340 = 120 volts. Average voltage is zero, presuming symmetrical wave form. RMS current is 10 amperes and power is 1200 watts, but peak current has been reduced to 26 amperes. To determine rating required of the two SCR's, each can be considered as a single half-wave circuit. From Figure 9.2, the average voltage, at 113 degrees, is .097 × 340 = 33 volts. Average current in each SCR is then 33/12 = 2.75 amperes at a conduction angle of 180 − 113 = 67 degrees.

In the case of a bridged SCR circuit, Figure 9.1(e), used for this same load, the average current through each rectifier is 2.75 amperes but the average current through the SCR is 5.5 amperes, corresponding to a total conduction angle of 134 degrees.

Of particular importance to note in the analysis charts is the nonlinearity of these curves. The first and last 30 degrees of each half-cycle contribute only 6 per cent (1.5% each) of the total power in each cycle. Consequently, a triggering range from 30° to 150° will produce a power-control range from 3% to 97% of full power, excluding voltage drop in the semiconductors.

Figure 9.4 shows a large variety of SCR circuits for the control of DC loads, along with the appropriate equations for voltages and currents. This information may be used in the selection of the best circuit for a particular use, and for determining the proper ratings of the semiconductors. Figure 9.4 is from reference 8, which also gives the approach for derivation of the equations shown in the chart.

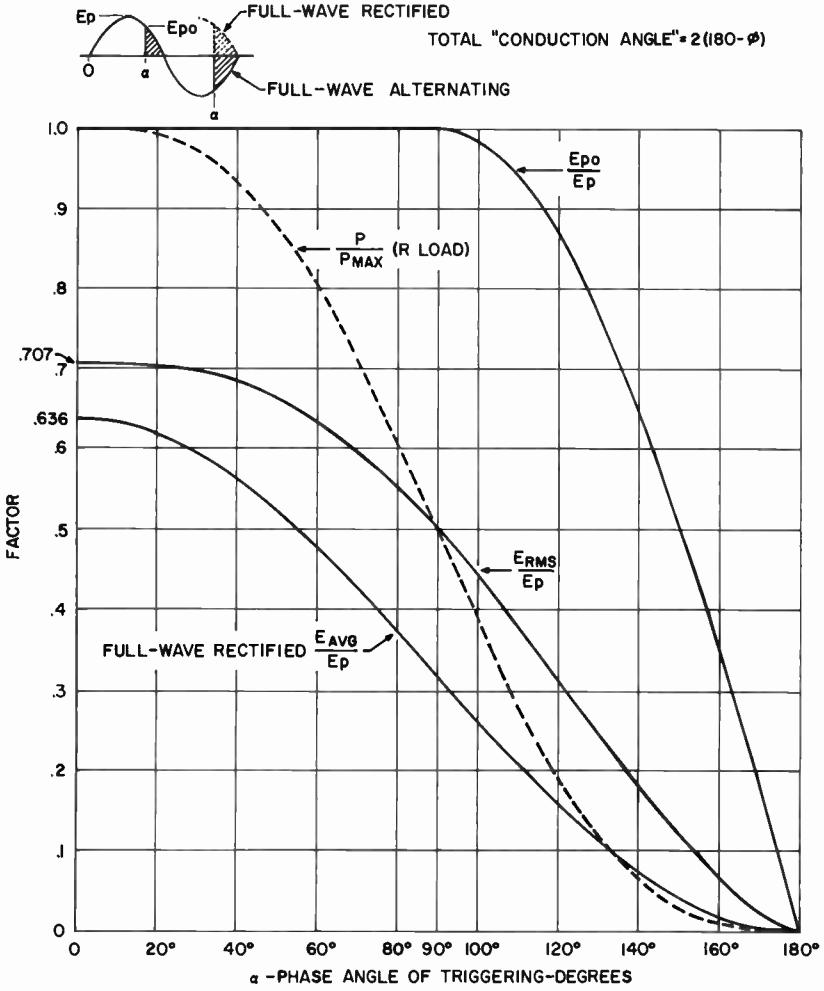
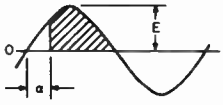
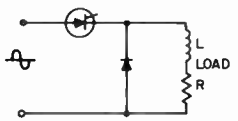
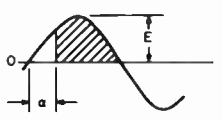
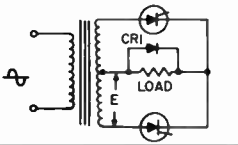
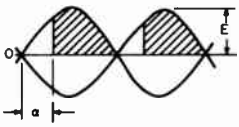
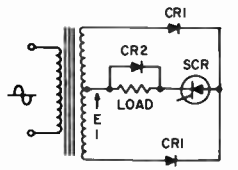
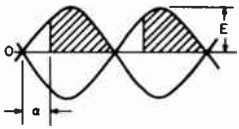
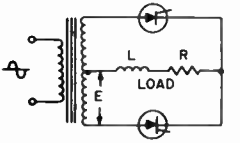
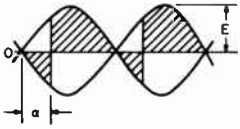
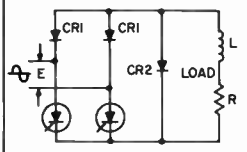
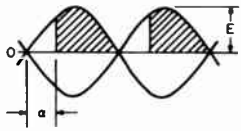


FIGURE 9.3 SYMMETRICAL FULL-WAVE PHASE CONTROL ANALYSIS CHART

CIRCUIT		(c)	(d)	PEAK REVERSE VOLTAGE		(g)
(a) NAME	(b) CONNECTIONS	LOAD VOLTAGE WAVEFORMS	PEAK FORWARD VOLTAGE ON SCR	(e) ON SCR	(f) ON DIODE	MAX. LOAD VOLTAGE ($\alpha = 0$) E_D = AVERAGE D-C VALUE E_a = RMS A-C VALUE
(1) HALF-WAVE RESISTIVE LOAD			E	E	—	$E_D = \frac{E}{\pi}$ $E_a = \frac{E}{2}$
(2) HALF-WAVE INDUCTIVE LOAD WITH FREE-WHEELING RECTIFIER			E	E	E	$E_D = \frac{E}{\pi}$
(3) CENTERTAP WITH RESISTIVE LOAD, OR INDUCTIVE LOAD WITH FREE-WHEELING RECTIFIER			E (POSSIBLY 2E IF LOAD OPEN)	2E	E	$E_D = \frac{2E}{\pi}$
(4) CENTERTAP WITH RESISTIVE OR INDUCTIVE LOAD–SCR IN D-C CIRCUIT			E	0	2E ON CR1 / E ON CR2	$E_D = \frac{2E}{\pi}$
(5) CENTERTAP WITH INDUCTIVE LOAD (NO FREE-WHEELING RECTIFIER)			2E	2E	—	$E_D = \frac{2E}{\pi}$
(6) SINGLE-PHASE BRIDGE WITH 2 SCR'S WITH COMMON ANODE OR CATHODE. RESISTIVE LOAD, OR INDUCTIVE LOAD WITH FREE-WHEELING RECTIFIER			E	E	E (CR1 AND CR2)	$E_D = \frac{2E}{\pi}$

† ASSUMES ZERO FORWARD DROP IN SEMICONDUCTORS WHEN CONDUCTING, AND ZERO CURRENT WHEN BLOCKING; ALSO ZERO α-c LINE AND SOURCE REACTANCE. INDUCTIVE d-c LOADS HAVE PURE d-c CURRENT.

FIGURE 9.4 CIRCUIT CONSTANTS OF SOME MAJOR PHASE CONTROLLED CIRCUITS FOR DC LOADS.†

(h) LOAD VOLTAGE VS TRIGGER DELAY ANGLE α	(j) TRIGGER ANGLE RANGE FULL ON TO FULL OFF	MAX STEADY-STATE CURRENT IN SCR		MAX STEADY-STATE CURRENT IN DIODE RECTIFIER		(p) ABILITY TO PUMPBACK INDUCTIVE LOAD ENERGY TO SUPPLY LINE	(q) FUNDAMENTAL FREQUENCY OF LOAD VOLTAGE (f = SUPPLY FREQUENCY)	(r) NOTES AND COMMENTS
		(k) AVERAGE AMP	(l) COND ANGLE	(m) AVERAGE AMP	(n) COND ANGLE FOR MAX CURRENT			
$E_D = \frac{E}{2\pi}(1+\cos\alpha)$ $E_a = \frac{E}{2\sqrt{\pi}}(\pi-\alpha+\frac{1}{2}\sin 2\alpha)^{1/2}$	180°	$\frac{E}{\pi R}$	180°	—	—	—	f	
$E_D = \frac{E}{2\pi}(1+\cos\alpha)$	180°	$\frac{E}{2\pi R}$ (LOAD HIGHLY INDUCTIVE)	180°	$0.54(\frac{E}{\pi R})$	210°	NO	f	
$E_D = \frac{E}{\pi}(1+\cos\alpha)$	180°	$\frac{E}{\pi R}$	180°	$0.26(\frac{2E}{\pi R})$	148°	NO	2f	
$E_D = \frac{E}{\pi}(1+\cos\alpha)$	180°	$\frac{2E}{\pi R}$	360°	CR1 = $\frac{E}{\pi R}$ CR2 = $0.26(\frac{2E}{\pi R})$ WITH HIGHLY INDUCTIVE LOAD	180° 148°	NO	2f	CR2 NECESSARY WHEN LOAD IS NOT PURELY RESISTIVE. FREQUENCY LIMITED BY RECOVERY CHARACTERISTICS OF RECTIFIERS AND SCR.
$E_D = \frac{2E}{\pi}\cos\alpha$ (ASSUMING CONTINUOUS CURRENT IN LOAD)	180°	$\frac{E}{\pi R}$	180°	—	—	YES	2f	
$E_D = \frac{E}{\pi}(1+\cos\alpha)$	180°	$\frac{E}{\pi R}$	180°	CR1 = $\frac{E}{\pi R}$ CR2 = $0.26(\frac{2E}{\pi R})$	180° 148°	NO	2f	WITHOUT CR2, SCR'S MAY BE UNABLE TO TURN OFF AN INDUCTIVE LOAD. ALSO, CR2 RELIEVES SCR'S FROM FREEWHEELING DUTY.

FIGURE 9.4 (CONTINUED)

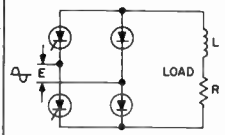
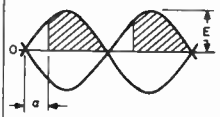
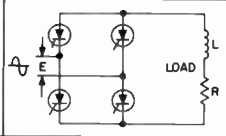
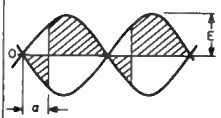
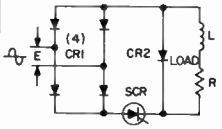
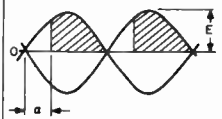
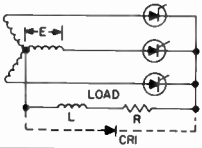
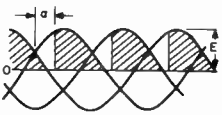
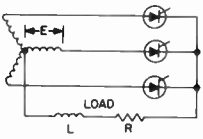
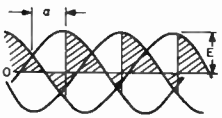
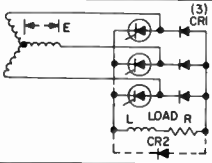
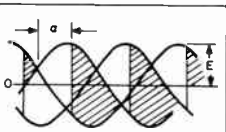
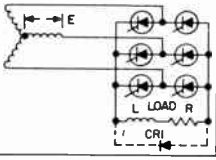
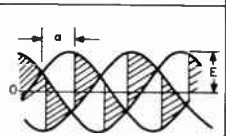
CIRCUIT		LOAD VOLTAGE WAVEFORMS	(d) PEAK FORWARD VOLTAGE ON SCR	PEAK REVERSE VOLTAGE		(g) MAX. LOAD VOLTAGE ($\alpha = 0$) E_D = AVERAGE D-C VALUE E_A = RMS A-C VALUE
(a) NAME	(b) CONNECTIONS			(e) ON SCR	(f) ON DIODE	
(7) SINGLE-PHASE BRIDGE WITH 2 SCR'S ON COMMON A-C LINE, RESISTIVE OR INDUCTIVE LOAD			E	E	E	$E_D = \frac{2E}{\pi}$
(8) SINGLE-PHASE BRIDGE WITH 4 SCR'S AND INDUCTIVE LOAD			E	E	–	$E_D = \frac{2E}{\pi}$
(9) SINGLE-PHASE BRIDGE WITH SINGLE SCR IN D-C CIRCUIT. RESISTIVE OR INDUCTIVE LOAD.			E	0	E (CR1 AND CR2)	$E_D = \frac{2E}{\pi}$
(10) THREE-PHASE HALF-WAVE WITH RESISTIVE LOAD OR INDUCTIVE LOAD WITH FREE-WHEELING RECTIFIER			E (POSSIBLY $\sqrt{3}$ E IF LOAD OPEN AND IF SCR'S HAVE HIGH REVERSE CURRENTS	$\sqrt{3}E$	E	$E_D = \frac{3\sqrt{3}E}{2\pi}$
(11) THREE-PHASE HALF-WAVE WITH INDUCTIVE LOAD (NO FREE-WHEELING RECTIFIER)			$\sqrt{3}$ E	$\sqrt{3}E$	–	$E_D = \frac{3\sqrt{3}E}{2\pi}$
(12) THREE-PHASE BRIDGE WITH 3 SCR'S RESISTIVE LOAD OR INDUCTIVE LOAD WITH FREE-WHEELING RECTIFIER			$\sqrt{3}$ E	$\sqrt{3}E$	$\sqrt{3}$ E	$E_D = \frac{3\sqrt{3}E}{\pi}$
(13) THREE-PHASE BRIDGE WITH 6 SCR'S. RESISTIVE LOAD, OR INDUCTIVE LOAD WITH FREE-WHEELING RECTIFIER			$\sqrt{3}$ E (1.5 E IF SCR'S SHUNTED BY RESISTANCE)	$\sqrt{3}E$	$\sqrt{3}$ E	$E_D = \frac{3\sqrt{3}E}{\pi}$

FIGURE 9.4 (CONTINUED)

(h) LOAD VOLTAGE VS TRIGGER DELAY ANGLE α	(j) TRIGGER ANGLE RANGE FULL ON TO FULL OFF	MAX STEADY-STATE CURRENT IN SCR (k) AVERAGE AMP	(l) COND ANGLE	MAX STEADY-STATE CURRENT IN DIODE RECTIFIER (m) AVERAGE AMP	(n) COND ANGLE FOR MAX CURRENT	(p) ABILITY TO PUMPBACK INDUCTIVE LOAD ENERGY TO SUPPLY LINE	(q) FUNDAMENTAL FREQUENCY OF LOAD VOLTAGE (f = SUPPLY FREQUENCY)	(r) NOTES AND COMMENTS
$E_D = \frac{E}{\pi}(1+\cos\alpha)$	180°	$\frac{E}{\pi R}$	180°	$\frac{E}{\pi R}$	180°	NO	2f	DIODE RECTIFIERS ACT AS FREE-WHEELING PATH, CONDUCT $(\pi+\alpha)$ DEGREES WITH INDUCTIVE LOAD.
$E_D = \frac{2E}{\pi}\cos\alpha$ (ASSUMING CONTINUOUS CURRENT IN LOAD)	180°	$\frac{E}{\pi R}$	180°	—	—	YES	2f	WITH RESISTIVE LOAD OPERATION IS SAME AS CIRCUIT (7)
$E_D = \frac{E}{\pi}(1+\cos\alpha)$	180°	$\frac{2E}{\pi R}$	360°	$CR1 = \frac{E}{\pi R}$	180°	NO	2f	CR2 NECESSARY WHEN LOAD IS NOT PURELY RESISTIVE, FREQUENCY LIMITED BY RECOVERY CHARACTERISTICS OF RECTIFIERS AND SCR'S
				$CR2 = 0.16(\frac{2E}{\pi R})$	148°			
$E_D = \frac{3\sqrt{3}E}{2\pi}\cos$ $(0<\alpha<30°)$	150°	$\frac{\sqrt{3}E}{2\pi R}$	120°	$0.16(\frac{3\sqrt{3}E}{2\pi R})$	134°	NO	3f	
$E = \frac{3E}{2\pi}[1+\cos(\alpha+30°)]$ $(30°<\alpha<150°)$								
$E_D = \frac{3\sqrt{3}E}{2}\cos$ (ASSUMING CONTINUOUS CURRENT IN LOAD)	150°	$\frac{\sqrt{3}E}{2\pi R}$	120°	—	—	YES	3f	
$E_D = \frac{3\sqrt{3}E}{2\pi}(1+\cos\alpha)$	180°	$\frac{\sqrt{3}E}{\pi R}$	120°	$CR1 = \frac{\sqrt{3}E}{\pi R}$	120°	NO	3f	WITHOUT CR2, SCR'S MAY BE UNABLE TO TURN OFF AN INDUCTIVE LOAD, ALSO CR2 RELIEVES SCR'S FROM FREE-WHEELING DUTY
				$CR2 = 0.14(\frac{3\sqrt{3}E}{\pi R})$	132°			
$E_D = \frac{3\sqrt{3}E}{\pi}\cos$ $(0<\alpha<60°)$	120°	$\frac{\sqrt{3}E}{\pi R}$	120°	$0.056(\frac{3\sqrt{3}E}{\pi R})$	212°	NO	6f	SCR'S REQUIRE TWO GATE SIGNALS 60° APART EACH CYCLE, ALTERNATELY A GATE SIGNAL DURATION >60°
$E_D = \frac{3\sqrt{3}E}{\pi}(1+\frac{\cos\alpha}{2}-\frac{\sqrt{3}}{2}\sin\alpha)$ $(60°<\alpha<120°)$								

FIGURE 9.4 (CONTINUED)

CIRCUIT (a) NAME	CIRCUIT (b) CONNECTIONS	(c) LOAD VOLTAGE WAVEFORMS	(d) PEAK FORWARD VOLTAGE ON SCR	PEAK REVERSE VOLTAGE (e) ON SCR	PEAK REVERSE VOLTAGE (f) ON DIODE	(g) MAX LOAD VOLTAGE ($\alpha = 0$) E_D = AVERAGE D-C VALUE E_a = RMS A-C VALUE	(h) LOAD VOLTAGE VS TRIGGER DELAY ANGLE α	(j) TRIGGER ANGLE RANGE FULL ON TO FULL OFF	MAX STEADY-STATE CURRENT IN SCR (k) AVERAGE AMP	MAX STEADY-STATE CURRENT IN SCR (l) COND ANGLE	MAX STEADY-STATE CURRENT IN DIODE RECTIFIER (m) AVERAGE AMP	MAX STEADY-STATE CURRENT IN DIODE RECTIFIER (n) COND. ANGLE FOR MAX CURRENT	(p) ABILITY TO PUMPBACK INDUCTIVE LOAD ENERGY TO SUPPLY LINE	(q) FUNDAMENTAL FREQUENCY OF LOAD VOLTAGE (f = SUPPLY FREQUENCY)	(r) NOTES AND COMMENTS
(14) THREE-PHASE BRIDGE WITH 6 SCR'S WITH INDUCTIVE LOAD			$\sqrt{3}E$ (1.5E IF SCR'S SHUNTED BY RESISTANCE)	$\sqrt{3}E$	—	$E_0 = \frac{3\sqrt{3}E}{\pi}$	$E_0 = \frac{3\sqrt{3}E}{\pi}\cos\alpha$ (ASSUMING CONTINUOUS CURRENT IN LOAD)	120°	$\frac{\sqrt{3}E}{\pi R}$	120°	—	—	YES	6f	SCR'S REQUIRE TWO GATE SIGNALS 60° APART EACH CYCLE, ALTERNATELY A GATE SIGNAL DURATION > 60°
AC RESISTIVE LOADS															
(15) TRIAC OR INVERSE PARALLEL SCR'S WITH RESISTIVE LOAD			E	E	—	$E_a = \frac{E}{\sqrt{2}}$	$E_a = \frac{E}{\sqrt{2\pi}}(\pi - \alpha + \frac{1}{2}\sin 2\alpha)^{1/2}$	180°	$\frac{E_a}{2.2R}$ OR $\frac{E}{\pi R}$	180°	—	—	—	f	WITH INDUCTIVE LOAD, LOAD VOLTAGE AND CURRENT DEPEND ON $\omega L/R$ AS WELL AS R AND α.
(16) SCR INSIDE BRIDGE WITH A-C RESISTIVE LOAD			E	0	E	$E_a = \frac{E}{\sqrt{2}}$	$E_a = \frac{E}{\sqrt{2\pi}}(\pi - \alpha + \frac{1}{2}\sin 2\alpha)^{1/2}$	180°	$\frac{E_a}{1.1R}$ OR $\frac{2E}{\pi R}$	360°	$\frac{E_a}{2.2R}$ OR $\frac{E}{\pi R}$	180°	—	f	INDUCTANCE IN D-C CIRCUIT MUST BE MINIMUM. FREQUENCY LIMIT DETERMINED BY RECOVERY CHARACTERISTICS OF RECTIFIERS AND SCR'S. WITH INDUCTIVE LOAD, LOAD VOLTAGE AND CURRENT DEPEND ON $\omega L/R$ AS WELL AS R AND α.

FIGURE 9.4 (CONTINUED)

9.3 COMMUTATION IN AC CIRCUITS

Commutation of the thyristor in AC circuits is usually no problem because of the normal periodic reversal of supply voltage. There are cases, however, which can lead to failure to commutate properly as the result of insufficient time for turn-off, or of excessive dv/dt of reapplied forward voltage, or both. Supply frequency and voltage, and inductance in load or supply, are determining factors.

Consider the inverse-parallel SCR circuit of Figure 9.5, with an inductive load. At the time that current reaches zero so that the conducting SCR can commutate (point A), a certain supply voltage exists which must then appear as a forward bias across the other SCR. The rate-of-change of this voltage is dependent on inductance and capacitance in the load circuit, as well as reverse recovery time of the SCR. In certain cases, an L di/dt transient may be observed as the result of the SCR turning off when current drops below holding current, I_H. The addition of a series RC circuit in parallel with the SCR's, or with the load, can reduce the dv/dt to acceptable limits. The magnitude of C is determined by the load impedance and the dv/dt limitation of the SCR. The value of R should be such as to damp any LC oscillation, with a minimum value determined by the repetitive peak SCR current produced when the SCR's discharge the capacitor.

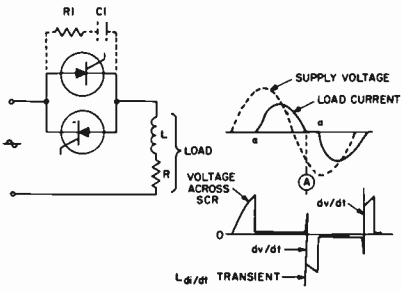


FIGURE 9.5 SUPPRESSION OF DV/DT AND TRANSIENTS FOR INDUCTIVE LOAD

An alternate solution is, obviously, the use of SCR's capable of turning off in a short time with a high applied dv/dt and a high voltage. In high-power circuits, this is often the best approach because of the size and cost of adequate RC networks.

Inductive AC loads in the bridged SCR circuit of Figure 9.6 have a slightly different effect. The rapid reversal of voltage at the input terminals of the bridge rectifier not only represents a high dv/dt, but it also reduces the time available for commutation. If the rectifiers used in the bridge have slow reverse-recovery time, compared with turn-off time of the SCR, the reverse-recovery current is usually enough to provide adequate time for commutation. Where this is not practical, a series R_1C_1 circuit at the input terminals of the bridge may be used. An alternate form of suppression is to use R_2C_2 across the SCR, which will limit dv/dt, but a resistor R_3 is then required to provide a circulating current path (for current on the order of I_H) to allow sufficient commutating time. If capacitor C_2 is large, it can provide holding current to the SCR during the normal commutation period, and thus prevent turn-off until the capacitor is discharged.

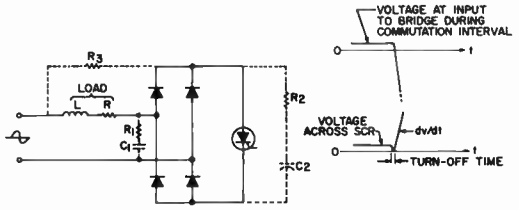


FIGURE 9.6 SUPPRESSION OF DV/DT AND INCREASING TURN-OFF TIME

The inductive AC load has a similar effect upon the commutation of the triac, and the solution is to either obtain a faster triac or suppress dv/dt with an RC network. This is discussed further in Section 7.1.4.

Inductive DC loads often require the addition of a free-wheeling diode, D_1 in Figure 9.7, to maintain current flow when the SCR is OFF. When an inductive DC load is used in the bridge circuit, Figure 9.7(c), the inductance causes a holding current to flow through the SCR and the bridge rectifier during the time line voltage goes through zero, preventing commutation. The addition of a free-wheeling diode, D_1, is required to by-pass this current around the SCR. The average current rating required for the diode D_1 is ½ maximum average load current for (a) and ¼ maximum average load current for (b) and (c).

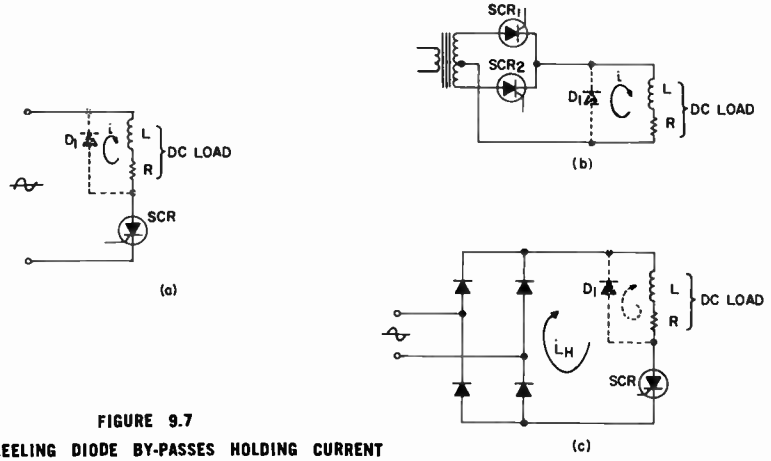


FIGURE 9.7
FREE-WHEELING DIODE BY-PASSES HOLDING CURRENT

9.4 BASIC TRIGGER CIRCUITS FOR PHASE CONTROL

Any of the relaxation oscillator pulse generators described in Chapter 4 may be adapted to phase control work. Since these are simply timing circuits, provision must be made for synchronizing them with the AC supply. This is usually done by taking the oscillator input voltage from the supply. There are many ways of connecting the various versions of the basic oscillator circuit, using the different semiconductor triggering devices and the thyristor, supply, and load circuits. Each combination has unique properties which must be considered in the selection of a circuit to perform a desired function.

9.4.1 Half-Wave Phase Control

The circuit of Figure 9.8 uses the basic relaxation oscillator to trigger the SCR at controlled triggering angles, α_t, during the positive half-cycles of line voltage. Since the adjustable resistor R_1 may go to zero resistance, diode D_1 is used to protect the triggering device and the gate of the SCR during the negative half-cycles. Certain triggering devices will permit the use of a fixed resistor R_2 instead of the diode, as will be shown later.

The waveforms of supply voltage, e, and voltage V_C, across the capacitor are shown in Figure 9.9. The magnitudes of R_1, C, E_p, and V_S determine the rate of charging the capacitor and the phase angle, α_t, at which triggering occurs. The earliest and latest possible triggering angles which can be obtained are indicated by α_1 and α_2 on the waveforms of Figure 9.9(a). If the switching current, I_S (see Chapter 4), of the trigger device is considered, the following relationships exist:

$$V_S = E_p \sin \alpha_1 \tag{9.1}$$

and

$$V_S + I_S R_1 = E_p \sin \alpha_2 \tag{9.2}$$

Since the maximum useful value of R_1 produces triggering at α_2, R_1 may be calculated for given values of e, C and V_S, but ignoring I_S for the moment, using the following equation:

$$R_1 = \frac{2\,E_p}{\omega C\,(V_S - V_O)} \tag{9.3}$$

Conversely, the peak voltage across the capacitor is

$$V_{CP} = \frac{2\,E_p}{\omega R_1\,C} + V_O \tag{9.4}$$

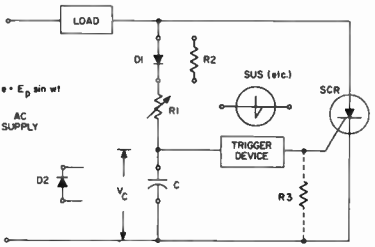


FIGURE 9.8 BASIC HALF-WAVE PHASE CONTROL CIRCUIT

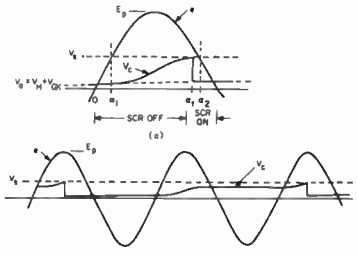


FIGURE 9.9 WAVE FORMS FOR FIGURE 9.8 (WITH D, AND SUS.)

Equations 9.3 and 9.4 assume a low value of V_S compared with E_p, as would be the case when using an SUS trigger device on a 120 volt AC line.

From equation 9.4 it can be seen that the residual (or initial) voltage, V_O, left on the capacitor has a pronounced effect upon this simple trigger circuit. The residual voltage, V_O, is usually the sum of the minimum holding voltage, V_H, of the trigger, and the gate-to-cathode source voltage, V_{GK}, which appears when the SCR turns on.

If the switching voltage is not reached during one positive half-cycle, the trigger device does not switch and a high residual voltage is left on the capacitor. The result, as shown in Figure 9.9(b) is "cycle-skipping" as the capacitor continues to charge each positive half-cycle until the trigger device switches. If the range of R_1 can be limited so that triggering always occurs each half-cycle under worst-case tolerance conditions of minimum E_p, minimum C, maximum V_S, minimum I_S, and minimum V_O, this cycle-skipping can be avoided. On the other hand, with the opposite tolerance condition, the latest possible triggering angle may produce an unacceptable minimum power in the load.

The ultimate solution to cycle-skipping is to automatically reset the capacitor to a known voltage, V_O, at the end of each half-cycle even though V_S was never reached. One way of doing this is to substitute resistor R_2 in the place of diode D_2 in Figure 9.8. This causes the capacitor voltage to reverse on the negative half-cycle, yielding a negative value of V_O at the start of the positive half-cycle. If the triggering device does not conduct during the negative excursion of V_C, then V_O will be predictable for any given value of R_1. This connection provides one cycle for the residual voltage on C to decay, and eliminates cycle skipping. If the triggering device conducts when V_C is negative, a second diode, D_2, may be used to clamp V_C to approximately −1 volt during the negative half-cycle.

If a bilateral trigger is used, such as the SBS or a neon lamp, the diode D_2 is not required (provided R_2 adequately limits the negative current) but V_O, at the beginning of the positive half-cycle, will depend on the number of oscillations occurring during the negative half-cycle, hence upon setting of R_1. Changing R_1 will make an integral change in the number of negative oscillations, hence will make step changes in V_O. This action results in step changes in triggering angle.

Automatic reset of capacitor voltage is achieved in the circuits of Figure 9.10 by forcing the triggering device to switch at the end of the positive half-cycle. In circuit (a), resistor R_2 provides a negative current out of the gate of the SUS (see Chapter 4) when the line voltage goes negative, thus causing the SUS to switch and discharge the capacitor. Since the switching

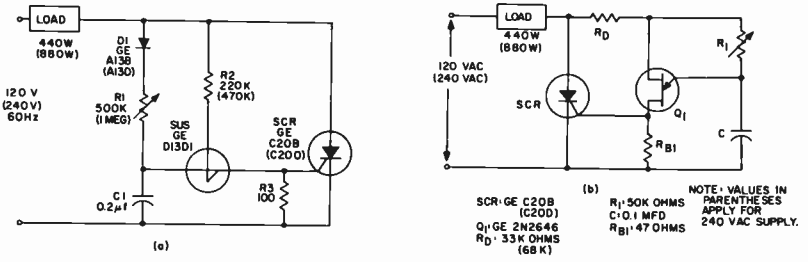


FIGURE 9.10 HALF-WAVE PHASE CONTROL WITH CAPACITOR RESET

voltage of the unijunction transistor is a function (η) of the interbase voltage, the capacitor in circuit (b) is reset through the UJT at the end of the positive half-cycle when the interbase voltage dips toward zero.

In the preceding examples, the supply voltage for the triggering circuit collapses when the SCR turns on. This connection avoids multiple oscillations and permits decreasing R_1 to zero without damage to the control circuit. If the triggering circuit were connected directly to the supply voltage instead of to the SCR anode, a fixed resistor, approximately 5000 ohms, in series with R_1 would be required to limit current. Since this latter connection changes the control circuit from a two-terminal to a three-terminal circuit, wiring considerations in certain applications may prohibit its use.

9.4.2 Full-Wave Phase Control

Either of the half-wave control circuits of Figure 9.10 may be used for full-wave power control by connecting them "inside" the bridge rectifier circuit shown in Figure 9.1(e). The UJT circuit of Figure 9.10(b) requires no modification for this use, but the SUS circuit (a) requires changing R_2 to 22 K ohms, adding another 22 K ohms between gate of SUS and cathode of SCR, and deleting diode D_1. These revisions are needed to obtain the reset action of the SUS.

The most elementary form of full-wave phase control is the simple diac/triac circuit of Figure 9.11. The waveform of capacitor voltage, V_C in Figure 9.12, is quite similar to the half-wave case with the major exception that the residual capacitor voltage, V_O, at the start of each half-cycle is opposite in polarity to the next succeeding switching voltage, V_S, that must be reached. The waveform shown for V_C is a steady-state condition, triggering late in each half-cycle. If the resistor R_1 is increased slightly, the dotted waveform, V_C', shows what happens in the next cycle after the last triggering. At the start of this cycle, V_O is the same as steady-state since the diac had switched in the preceding half-cycle. At the end of the first half-cycle, however, the capacitor voltage is just below V_S, and the diac remains dormant. This changes V_O to $+V_S$ at the beginning of the second half-cycle. The peak capacitor voltage in the negative half-cycle is, therefore, considerably below V_S, as shown earlier by equation 9.4. In all succeeding cycles $V_O = V_{C_0}$, and the peak value of V_C will then remain well below V_S until the value of R_1 is reduced.

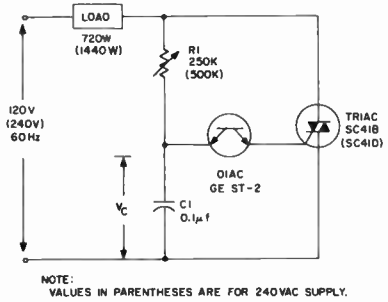


FIGURE 9.11
BASIC DIAC-TRIAC FULL-WAVE PHASE CONTROL

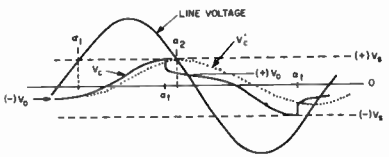


FIGURE 9.12
WAVEFORMS FOR FIGURE 9.11

Once triggering has ceased, reducing R_1 will raise V_C, but when V_S is reached again and the diac switches, V_O is suddenly reduced. This action increases the value of V_C on the next half-cycle, which causes triggering to occur at a much earlier phase angle. As a result, the load current suddenly snaps from zero to some intermediate value, from which point it may be smoothly controlled over the full range from α_1 to α_2.

The "snap-on" effect may be reduced by connecting the control circuit to the supply, as shown in Figure 9.13. The improvement is obtained by allowing the capacitor to re-charge slightly between the triggering point, α_t, and the end of the half-cycle. This raises V_O, hence reduces the effect when V_O becomes V_S. Since the triac does not remove power from the control circuit after triggering, a 15 K ohm fixed resistor is used to limit control power. This has the disadvantage of also limiting maximum load power by increasing the minimum firing angle, α_1.

Full load power may be achieved by using a diode circuit to reset the capacitor at the end of each positive half-cycle, as shown in Figure 9.14. During the positive half-cycle, both diodes are reverse-biased and capacitor C_1 charges through R_1 to a positive voltage. If V_C is just short of V_S, the diac will not switch but when the positive supply voltage becomes less than V_C, the capacitor is discharged through diode D_1 and R_2. After the line voltage crosses zero and becomes negative, diode D_2 conducts and the capacitor then charges to a negative voltage. No resetting is obtained at the end of the negative half-cycle. However, the snap-on effect is reduced to an insignificant level by this circuit.

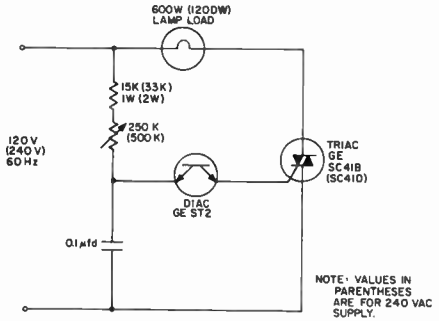


FIGURE 9.13 FULL-WAVE PHASE CONTROL WITH REDUCED "SNAP-ON"

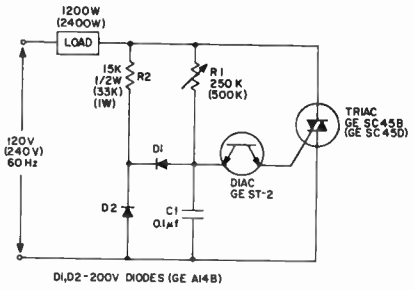


FIGURE 9.14 FULL-WAVE PHASE CONTROL WITH ALTERNATE RESET

Figure 9.15 shows another circuit with very little snap-on effect. This circuit uses a second capacitor, C_2, to recharge C_1 after triggering, thus raising V_O to approximately V_S. The maximum, or latest, triggering angle, α_2, with this circuit is not limited to the point where the supply voltage is equal to V_S because the second capacitor will permit greater than 90° phase shift of V_{C1}. If, however, the diac should switch after the 180° point on the supply wave, it could very well trigger the triac at the beginning of the next half-cycle. Since this condition usually needs to be avoided, coupling resistor R_3 should be adjustable to permit compensation for wide-tolerance component values. If desired, R_3 may be set for a minimum power level in the load at maximum setting of R_1.

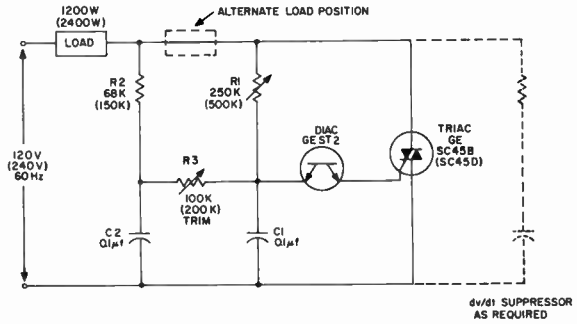


FIGURE 9.15 EXTENDED RANGE FULL-WAVE PHASE CONTROL CIRCUIT

9.5 HIGHER "GAIN" TRIGGER CIRCUITS FOR PHASE CONTROL

All of the previous circuits control phase angle of triggering by a resistor. To control over the full range, from minimum to maximum power, with the simple RC timing circuit requires a very large change in the value of R, presenting a low control "gain." For manual control, this is most adequate. For systems which must perform a function, in response to some signal, the simple RC circuits are usually inadequate, although a photoconductor or a thermistor could be used for control but only over very wide range of light or temperature change.

9.5.1 Manual Control

Figure 9.16 shows a conventional, manually-controlled SCR circuit with a unijunction transistor. A zener diode clamps the control circuit voltage to a fixed level, as shown in Figure 9.17. Since the peak-point (or triggering) voltage, e_p, of the unijunction transistor emitter is a fixed fraction of the interbase voltage, V_{BB}, as indicated by the dashed curve, the capacitor will charge on an exponential curve toward V_{BB} until its voltage reaches e_p. Assuming, for convenience, that e_p is 0.63 V_{BB}, triggering will occur at one time-constant. Therefore, to cover the range from 0.3 to 8.0 milliseconds, the product R_2C must change by the same amount. Since C is fixed, R_2 must then be

varied over a 27:1 range. Not only is this a very large range, but the transfer characteristic from R_2 to average load voltage, V_L, is quite non-linear, as shown in Figure 9.18. These characteristics are usually satisfactory, however, for manual control.

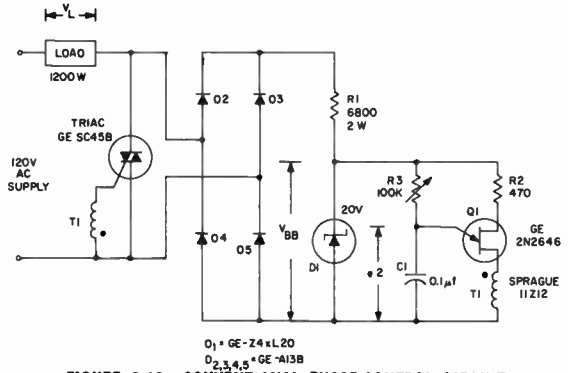


FIGURE 9.16 CONVENTIONAL PHASE-CONTROL CIRCUIT

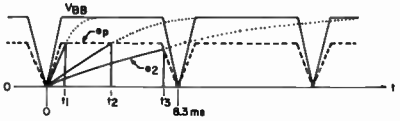


FIGURE 9.17 UNIJUNCTION TRANSISTOR WAVEFORMS

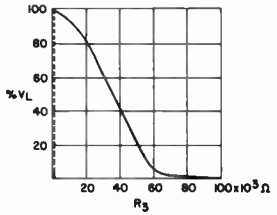


FIGURE 9.18 TRANSFER CHARACTERISTIC OF CONVENTIONAL CIRCUIT

Replacing the manually controlled resistor with a p-n-p transistor, shown in Figure 9.19(a), and applying a DC signal between emitter and base results in a higher current-gain but the range of base current must again be 27:1. The transfer characteristic, Figure 9.19(b), also remains non-linear.

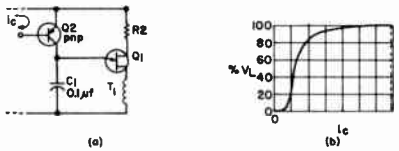


FIGURE 9.19 SERIES TRANSISTOR CONTROLLED RAMP

Control gain can be made very high by the use of a low resistance potentiometer, connected as shown in Figure 9.20(a). Since the exponential charging of C is very fast, and limited by the voltage-division of the pot, the transfer characteristic is again non-linear, as shown in Figure 9.20(b). If the zener clamp has any significant zener impedance, the clamped voltage will not be flat, but will have a slight peak at 90 degrees. This curvature can produce an abrupt discontinuity, or "snap," in the transfer characteristic as indicated by the dashed curve of Figure 9.20(b).

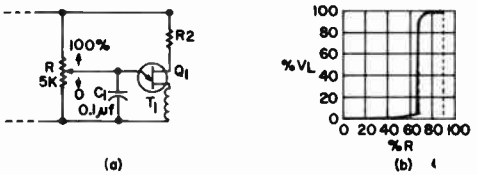


FIGURE 9.20 RESISTANCE CONTROLLED PEDESTAL

The use of an n-p-n transistor, Figure 9.21(a), will provide a high current-gain, but non-linearity and possible snap are still present, as indicated in Figure 9.21(b).

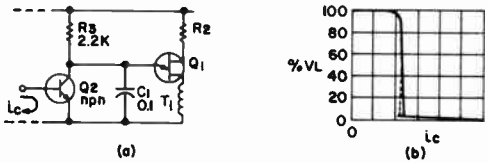


FIGURE 9.21 SHUNT TRANSISTOR CONTROLLED PEDESTAL

9.5.2 Ramp-and-Pedestal Control

If the circuits of Figure 9.16 and 9.20(a) are combined with diode coupling, as in Figure 9.22(a), the exponential ramp function can be caused to start from a higher voltage pedestal, as determined by the potentiometer. Transfer characteristic Curve 1 of Figure 9.22(b) is obtained when R_2 is set

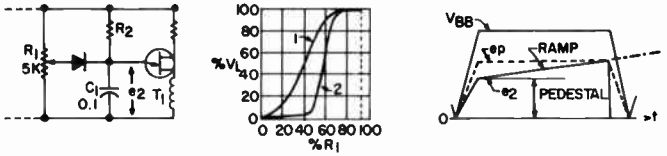


FIGURE 9.22 RESISTANCE CONTROLLED PEDESTAL WITH LINEAR RAMP

for a time-constant of 8 milliseconds. Higher control gain is obtained (Curve 2) by making the R_2C_1 time-constant about 25 milliseconds. The voltage wave-shape observed across C_1 is a nearly-linear ramp sitting on a variable-height pedestal, as in Figure 9.22(c). Small changes in pedestal height produce large changes in phase-angle of triggering. The linear relationship be-

tween height and phase-angle results, however, in a non-linear transfer function because of the shape of the sine-wave supply.

Both high gain and linearity are obtained by charging C_1 from the unclamped sinusoidal waveform, as in Figure 9.23(a). This adds a cosine wave to the linear ramp to compensate for the sinusoidal supply waveform, resulting in the linear transfer characteristics shown in Figure 9.23(b). System gain can be adjusted over a wide range by changing the magnitude of charging resistor, R_2, as indicated in Figure 9.23(c). By selecting a ramp amplitude of one volt, for example, and assuming a zener diode of 20 volts, then a change in potentiometer setting of only 5 per cent results in the linear, full-range change in output.

The values shown in Figure 9.23(a) are typical for a 60 Hz circuit. The potentiometer resistance must be low enough to charge capacitor C_1 rapidly, in order to be able to trigger early in the cycle. This is the limiting factor on control impedance level. The logarithmic characteristic of diodes limits the control gain that can be achieved with a reasonably linear transfer characteristic. At a one-volt ramp amplitude, diode non-linearity is not pronounced,

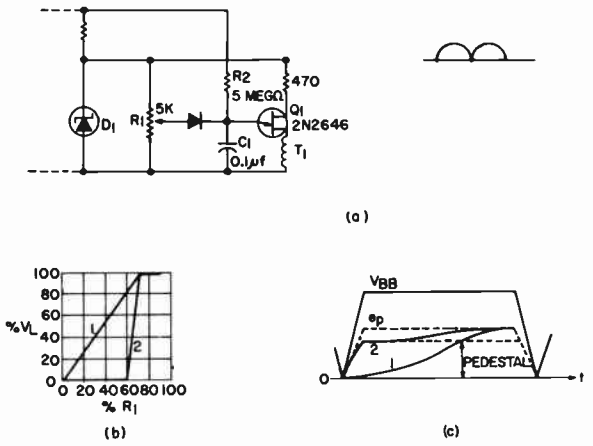


FIGURE 9.23 RESISTANCE CONTROLLED PEDESTAL WITH COSINE-MODIFIED RAMP.

but at 0.1 volt ramp voltage, the capacitor is charged primarily by diode current, thus obliterating the cosine-modified ramp. The sharper knee of a zener diode may be used to obtain higher gains, at the expense of requiring a higher voltage across the potentiometer. The third limiting factor is the peak-point current of the unijunction transistor. This current must be supplied entirely by R_2 and should be no higher than one-tenth the charging current on C_1, at the end of the half-cycle, in order to avoid distortion of the waveform. The 2N2647 unijunction transistor used in the example has a maximum peak-point current of two microamperes, hence is particularly well suited for high-gain systems. The fourth limitation is the zener impedance of diode D_1. This impedance must be very low in order to keep the peak-point voltage (triggering level) constant during the half-cycle. If this voltage changes 0.1 volt, then the ramp voltage should be on the order of 1 volt. Temperature effects on the

unijunction transistor, and other components, must also be taken into consideration when attempting to work at very low ramp voltages.

In Figure 9.24(a), manual control is replaced by a bridge circuit for feedback control. Zener diode D_2 has a slightly lower zener-voltage than D_1 in order to hold the top of the clamped waveform more nearly flat. Resistors R_1 and R_2 form the voltage divider which determines pedestal height. Variation in either of these resistors can therefore provide the control function, although R_2 is generally used as the variable. Figures 9.24(b) and (c) show the use of a thermistor for temperature regulation and a photoconductor for light control, in either open-loop or closed-loop systems.

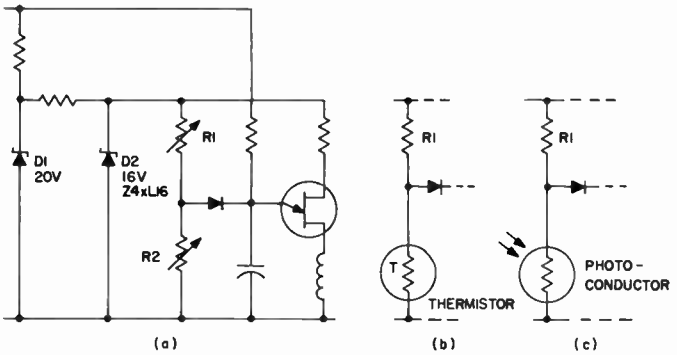


FIGURE 9.24 OHMIC-TRANSDUCER PEDESTAL CONTROL

To obtain a higher input impedance, an n-p-n transistor may be used as an emitter-follower, as shown in Figure 9.25(a). If the transistor has a current gain of 100, the values of R_1 and R_2 can be increased from 3000 ohms to 300 K ohms, thus greatly reducing power dissipation in the sensing element. This is particularly important when R_1 or R_2 is a thermistor. Resistor R_3 is required in the collector circuit of the transistor in order to limit charging current available to the UJT capacitor and thus prevent premature triggering of the UJT.

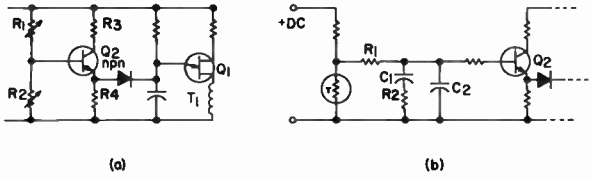


FIGURE 9.25 TRANSISTOR EMITTER-FOLLOWER CONTROL FOR AC OR DC INPUT

In many feedback-control systems, high gain and phase-shifts often produce instability, ranging from excessive overshoot to large oscillations, or hunting (see Chapter 12). The transistor permits use of a DC sensing circuit followed by an appropriate RC "notch-network" (R_1 C_1, R_2 C_2) to produce the required degree of damping. Since the cosine-modified ramp results in a uniform, linear response, system gain is constant and proper damping is much easier to obtain than in the case of the linear ramp where gain changes

with phase-angle. System gain is controlled by the ramp charging resistor (R_2 of Figure 9.23), which can be made a secondary variable through the use of a thermistor or a photoconductor. To avoid excessive loading on the DC sensing circuit, a resistor is required in series with the base of the transistor. Upper and lower control limits may be obtained by the use of diode clamps.

The capability of working from a DC control signal permits a soft-start and soft-stop circuit, shown in Figure 9.26(a). This circuit features individually adjustable rates of start and stop, good linearity, upper and lower limit clamps, and manual or resistive master phase control by means of the top clamping level. For a typical UJT peak-point of 2/3 the interbase voltage, the ramp amplitude may be set at 1/3 interbase voltage and the pedestal clamped at 1/3 and 2/3 this voltage. The resulting performance characteristic is shown in Figure 9.26(b) and (c) for this condition, with the switch turned ON at t_1 and OFF at t_3.

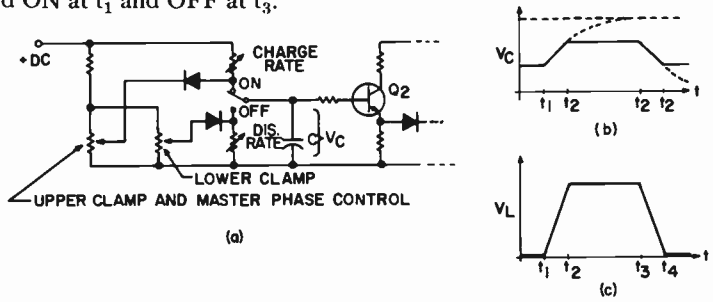


FIGURE 9.26 SOFT START AND STOP CONTROL

Remote control from an AC signal, such as an audio-frequency from a tape recorder or from a tachometer, or an RF carrier alone or with audio modulation, is shown in Figure 9.27. The offset voltage characteristic of a high-gain system provides immunity to noise and effectively decreases the band-width of the input resonant circuit. If offset is not desired, but high-gain is required, the input circuit may be biased, by the dotted resistors R_4 and R_5, to a voltage just below offset. The use of a standard ratio-detector will permit control by an FM signal directly.

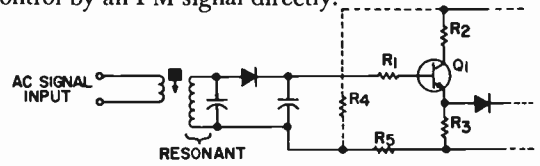


FIGURE 9.27 FREQUENCY-SELECTIVE AC AMPLITUDE CONTROL CIRCUIT

Alternate transistor connections are shown in Figure 9.28, providing a wide variety of performance characteristics. The emitter-follower circuit is simplified in Figure 9.28(a) for low-gain use. At high control gain (low ramp voltage) the emitter current requirement is very low, and the decrease in beta at such low currents causes excessive non-linearity. Standard common-emitter connections for n-p-n and p-n-p transistors, Figures 9.28(b) and (c), provide lower input impedance and higher voltage gain, but require temperature

compensation in high-gain applications. In addition, the n-p-n circuit of Figure 9.28(b) results in a sense inversion which may or may not be desirable. Sense inversion is also obtained in the p-n-p emitter-follower of Figure 9.28(d). The excellent performance characteristics and low cost of the 2N2923 silicon n-p-n transistor, however, make the choice of the n-p-n emitter-follower circuit attractive, particularly since the temperature changes have very little effect on operation of this circuit.

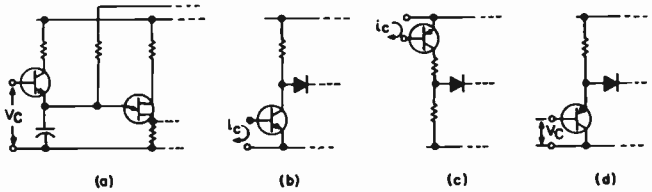


FIGURE 9.28 ALTERNATE TRANSISTOR PEDESTAL CONTROL CIRCUITS

An alternate form of the soft-start circuit is shown in Figure 9.29, using the clamping diode, D_1, to control pedestal height on a linear ramp. Capacitor C_1 may be several hundred microfarads and is charged slowly through R_2. R_1 continues the charging beyond emitter peak-point voltage to completely remove the effect of C_1 and to provide a discharge path when power is removed. The supply for this circuit must be obtained from the line, rather than from voltage across the triac, in order to completely charge C_1.

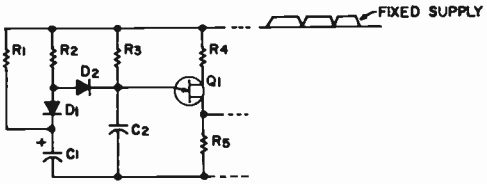


FIGURE 9.29 ALTERNATE SOFT-START CIRCUIT

In Figure 9.30, compensation for changes in supply voltage is obtained by R_2 and C_1 which add to the zener diode voltage a DC voltage proportional to supply voltage. This is used to supply interbase voltage for the UJT. Since pedestal height is fixed by the zener diode, reducing supply voltage reduces interbase and peak-point voltages of the UJT, thus causing triggering to occur earlier on the ramp. The size of R_2 is dependent on ramp amplitude, hence upon R_5. The voltage compensation feature does not interfere with use of the pedestal height in any other control form, such as a feedback control system. This system has been found capable of holding RMS output voltage constant within 5% for a 50% change in supply voltage. The bottom end of control is reached when supply voltage drops to desired output voltage.

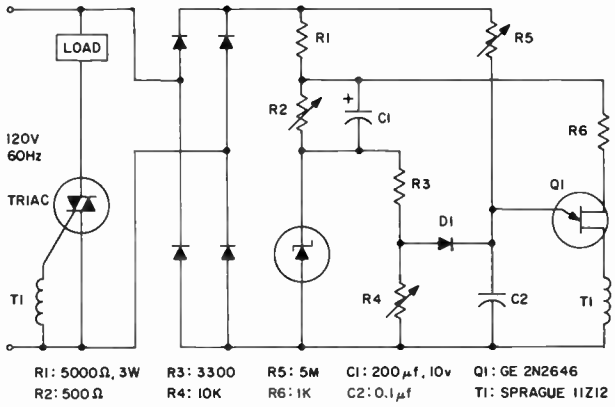


FIGURE 9.30 WIDE RANGE LINE-VOLTAGE COMPENSATION CONTROL

Current feedback control can be obtained by the use of voltage across a shunt resistor, but this requires rectification and filtering when AC is to be controlled since no current flows prior to triggering. In addition, a lamp may be used as the shunt, with a photoconductor sensing lamp output (see Chapter 12). Response time of the lamp and photoconductor is generally long enough to provide filtering, and the control is on the *square* of current, hence will hold constant RMS value rather than average value. A resistor-thermistor combination will also provide RMS control. A current-transformer may be used to produce a higher output voltage signal on AC with less power loss. If power loss in the shunt is detrimental, a magnetic-flux sensitive element such as the Mistor* resistance transducer or a Hall-effect element may be used in a suitable coil and core. In these magnetic-flux sensors, the output will be a function of average current.

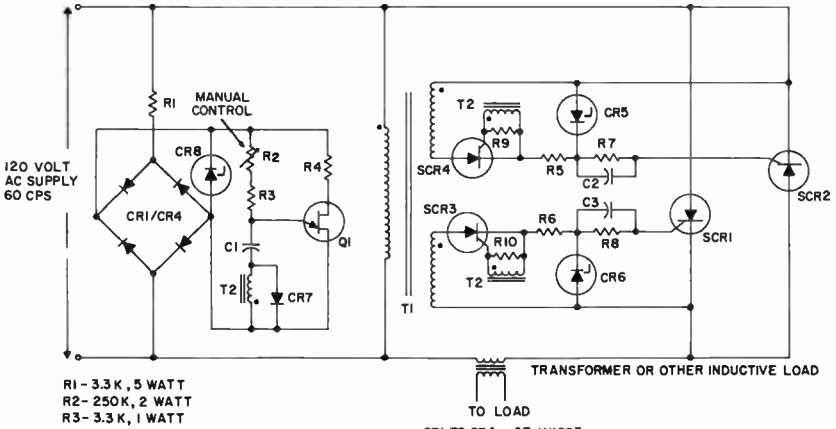
These circuits are typical of a wide variety, based on the ramp-and-pedestal concept for transfer from voltage, current, or impedance level to phase-angle of triggering for SCR's. Adjustable gain, linearity, selection of high or low input impedance, and operation from a DC input signal are attractive features for use in feedback or open-loop control systems, or in special function systems.

9.6 TRIGGER CIRCUIT FOR INDUCTIVE AC LOADS

Inductive AC loads present two basic requirements of the trigger circuits in order to provide symmetry and proper control: a) synchronization must be obtained from the supply voltage rather than SCR voltage; b) the trigger signal must be continuous during most of the desired conduction period. Figure 9.31 shows a trigger circuit specifically designed to meet these requirements.

Unijunction transistor Q_1 is connected across the AC supply line by means of the bridge rectifier, CR_1 through CR_4, thus permitting Q_1 to trigger on both halves of the AC cycle.

*TM American Aerospace Controls, Inc.



R1 - 3.3 K, 5 WATT
R2 - 250K, 2 WATT
R3 - 3.3 K, 1 WATT
R4 - 330, 1/2 WATT
R5, R6 - 22Ω, 2 WATT
R7, R8 - 33Ω, 2 WATT
R9, R10 - 47Ω, 1/2 WATT
C1, C2, C3 - 0.1 MFD
Q1 - GE 2N2646
SCR1, SCR2 — CONTROLLED RECTIFIERS, AS REQUIRED
SCR3, SCR4 - GE 2N1595

CR1 TO CR4 - GE IN1693
CR5, CR6 - GE IN1765
CR7 - GE IN1692
CR8 - GE IN1776
T1 - ISOLATION TRANSFORMER 120/12.6/12.6 VAC; PRIMARY VOLTAGE DEPENDS ON LINE VOLTAGE (UTC FT-10 FOR 120V.)
T2 - PULSE TRANSFORMER PE2229, UTC H51 OR SPRAGUE 93Z20 EQUIVALENT

FIGURE 9.31 TRIGGER CIRCUIT FOR PHASE CONTROLLED SCR's FEEDING INDUCTIVE LOAD.

The time constant of potentiometer R_2 in conjunction with capacitor C_1 determines the delay angle α at which the unijunction transistor delivers its first pulse to the primary of pulse transformer T_2 during each half-cycle. These pulses are coupled directly to the gates of SCR_3 and SCR_4. Whichever of these SCR's has positive anode voltage during that specific half-cycle triggers and delivers voltage to its respective main SCR, firing it in turn. The low voltage AC supply for the "pilot" SCR's (SCR_3 and SCR_4) is derived from a "filament" type transformer T_1. Zener diodes CR_5 and CR_6, in conjunction with resistors R_5 and R_6, clip the AC gate voltage to prevent excessive power dissipation in the gates of the main SCR's. The RC networks (R_7—C_2 and R_8—C_3) also limit gate dissipation in the main SCR's while delivering a momentarily higher gate pulse at the beginning of the conduction period to accelerate the switching action in the main SCR's.

If electrical isolation of a DC control signal from the AC voltage is required, the entire unijunction trigger circuit with its bridge rectifier and associated components can be connected to an additional secondary winding (approximately 110 volts) on transformer T_1. Total loading of this particular part of the circuit is less than 30 milliamperes. Of course, low level phase control signals for SCR_3 and SCR_4 can be secured from other circuits than the specific one shown, but this is incidental to the main objectives: driving SCR_1 and SCR_2 from a square wave source synchronized to the AC line.

Figure 9.32 is a smaller and lower-cost version of the inductive load phase control. The bridge rectifier D_1-D_4 supplies power to the UJT trigger circuit and supplies holding current to the SCR. If triggering should occur prior to turn-off of the triac, the SCR will be turned on and held by current through R_1. When the triac turns-off at a current zero, triac gate current will flow, depending on polarity, through D_5 or D_6, the SCR, and D_4 or D_2, thus re-triggering the triac. At the expense of higher voltage diodes and SCR, this circuit eliminates all transformers with their attendant cost, size and weight.

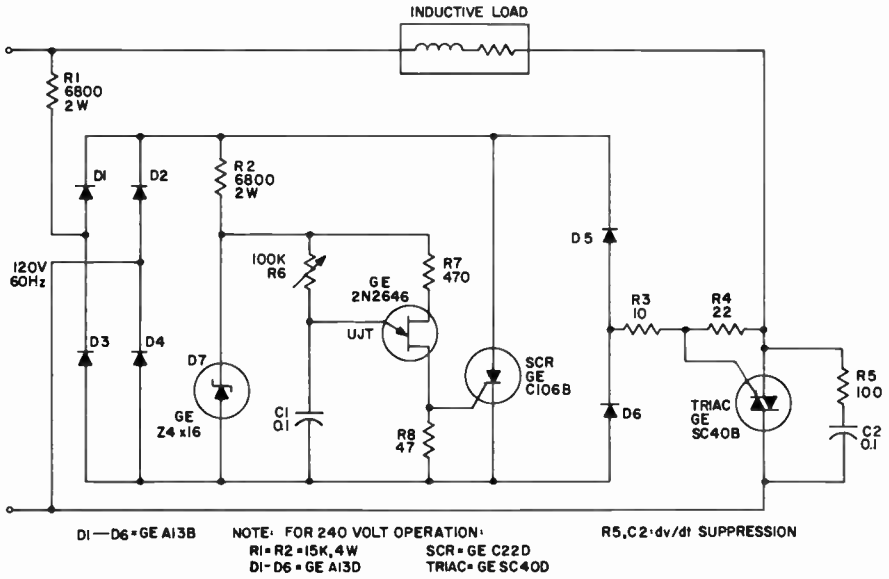


FIGURE 9.32 FULL-WAVE PHASE CONTROL FOR INDUCTIVE LOADS

For higher power-factor inductive loads, and where a small dissymmetry is permissible, the two-capacitor diac/triac circuit of Figure 9.15 may be used, with the load connected in the alternate position shown in that circuit. When R_1 is small, calling for maximum power, the trigger circuit supply is essentially the voltage across the triac, hence cannot attempt to trigger before commutation. When R_1 is large, the trigger circuit is largely powered from the supply voltage, thus providing good symmetry and very little DC component of load current.

9.7 NEON LAMP TRIGGER CIRCUITS

Neon lamp SCR phase-controlled trigger circuits have the promise of combining the low cost of the RC diode circuit with improved performance. In addition, the possibility exists in such a relatively simple yet high impedance circuit to exercise control over the charging rate of the trigger capacitor with suitable devices responsive to light, heat, pressure, etc.

Figure 9.33 shows a half wave AC phase-controlled circuit using a 5AH as the trigger for a two terminal system. The 5AH will trigger when the voltage across the two 0.1 MFD capacitors reaches the breakdown voltage of the lamp. Control can be obtained full off to 95% of the half wave RMS output voltage. Full power can be obtained with the addition of the switch across the SCR.

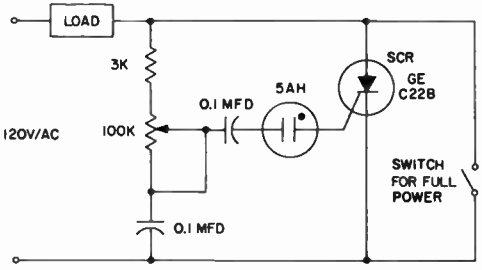


FIGURE 9.33 HALF WAVE/TWO TERMINAL PHASE CONTROL

Figure 9.34 is a transformer coupled full-wave AC phase-controlled circuit using a 5AH as the trigger for a two terminal system. The 5AH will perform the same as in the half-wave circuit but the pulse transformer will allow the SCR's to alternate in firing. The resistor R and the pulse transformer should be chosen to give proper shape of the pulse to the gate of the SCR. Some loss of load voltage will occur but will amount to only about 5% in terms of total RMS output voltage.

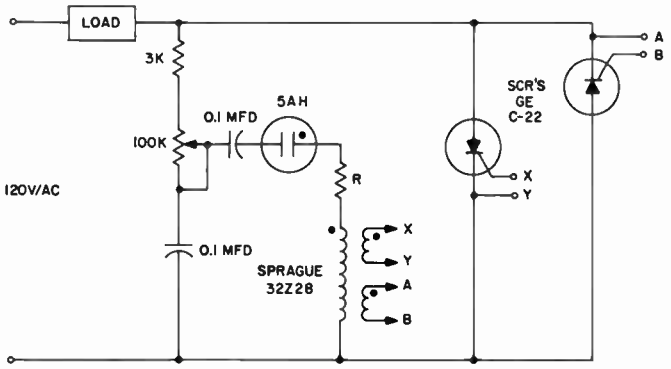


FIGURE 9.34 FULL WAVE TRANSFORMER COUPLED/TWO TERMINAL PHASE CONTROL

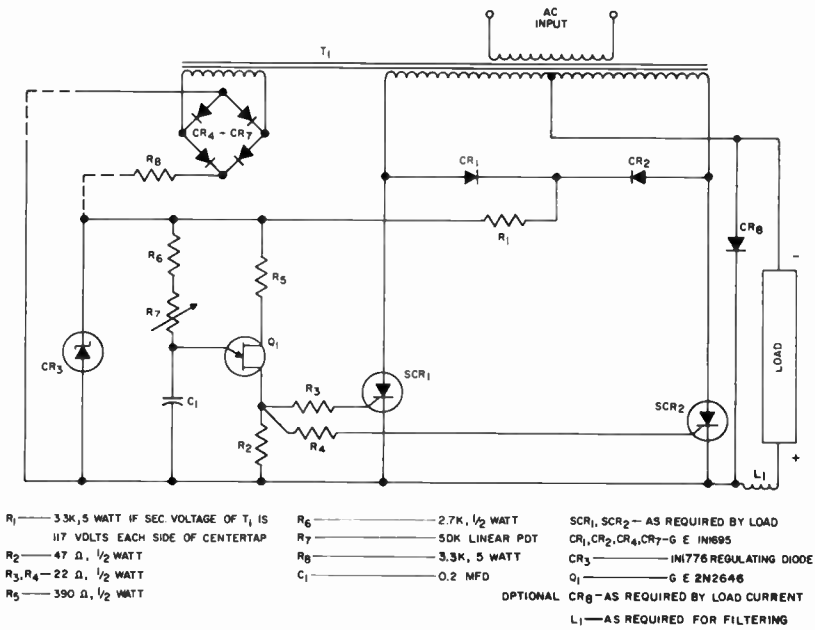
9.8 TYPICAL PHASE-CONTROLLED CIRCUITS FOR DC LOADS

Figure 9.35 illustrates the use of SCR's in a typical single phase center-tap phase-controlled rectifier. By varying R_7, the DC voltage across the load can be steplessly adjusted from its maximum value down to zero. As in the AC phase-controlled switch, a single UJT (Q_1) is used to develop a gate signal to fire both SCR's on alternate half-cycles. Whichever of the two SCR's has positive anode voltage at the time the gate pulse occurs will fire, thus applying voltage to the load for the remainder of that half-cycle. The firing angle can be adjusted by means of R_7. At 60 Hz, the firing angle of this circuit can be varied from approximately 10° to 180° (fully off).

If the secondary voltage applied to the SCR anodes is less than approximately 100 volts RMS, a separate voltage supply should be used for the UJT control. In Figure 9.35 an additional 117 VAC winding on T_1 in conjunction

with a diode bridge CR_4—CR_7 can be substituted for CR_1, CR_2, and R_1 if the main secondary voltage is low. A more steeply rising square wave of voltage with sufficient amplitude is thereby provided for control purposes. If the load requires filtering, inductance L_1 and free-wheeling diode CR_8 may be added, as shown.

For feedback-controlled regulated power supplies, see Chapter 12.



R_1 —— 3.3K, 5 WATT IF SEC. VOLTAGE OF T_1 IS 117 VOLTS EACH SIDE OF CENTERTAP
R_2 —— 47 Ω, ½ WATT
R_3, R_4 — 22 Ω, ½ WATT
R_5 —— 390 Ω, ½ WATT
R_6 —— 2.7K, ½ WATT
R_7 —— 50K LINEAR PDT
R_8 —— 3.3K, 5 WATT
C_1 —— 0.2 MFD
SCR_1, SCR_2 — AS REQUIRED BY LOAD
CR_1, CR_2, CR_4, CR_7 — G E IN1695
CR_3 —— IN1776 REGULATING DIODE
Q_1 —— G E 2N2646
OPTIONAL CR_8 — AS REQUIRED BY LOAD CURRENT
L_1 — AS REQUIRED FOR FILTERING

FIGURE 9.35 PHASE-CONTROLLED DC POWER SUPPLY

9.9 POLYPHASE SCR CIRCUITS

The use of controlled rectifiers is by no means limited to single-phase AC circuits. They may be used in polyphase circuits just as conventional two element semiconductor rectifiers. Regardless of the particular circuit configuration the two basic requirements that must be met are the supplying of a trigger turn-on signal at the appropriate time and provision in the circuit external to the controlled rectifier for turn-off.

With regard to turn-off, the reversal of the line voltage across the device in common rectifier circuit configurations will return the controlled rectifier to a forward blocking state; this is often referred to as line commutation. On commutating, the rectifier is subjected to reverse voltage which facilitates the turn-off process. For this reason, common AC rectifier circuits do not impose unusual turn-off requirements on the controlled rectifier as do certain types of inverter or DC chopper circuits in which forward voltage is reapplied to the controlled rectifier immediately following turn-off. However, depending on the amount of phase retard the controlled rectifier and its associated rectifiers may be subjected to full peak reverse blocking voltage immediately after

having conducted full rated current. This type of service is conducive to the generation of recovery voltage transients. Particularly, in cases where SCR's are used in series in a leg of such a circuit, steps must be taken to force proper sharing of these transients between all the devices in the leg. This is discussed more fully in Chapter 6.

The question of utilizing controlled rectifiers in polyphase circuits involves providing appropriately timed triggering signals in accordance with the type of circuit used and the degree of phase control required. For example, the circuit of Figure 9.36 shows the popular three phase bridge circuit in which the forward legs are controlled and the back legs consist of uncontrolled conventional two terminal rectifiers. This circuit will give full continuous control from zero to 100% of its DC output when triggering signals capable of being phase shifted over 180 electrical degrees are supplied as shown in Figure 9.37(a).

The triggering circuit discussed in Section 9.9.2 will provide such triggering signals. If triggering signals are supplied as shown in Figure 9.37(b) such that they can be phase-shifted over 120 electrical degrees, the circuit will deliver full control from about 25% to 100% of full output power to the load. A circuit to do this is discussed in Section 9.9.1.

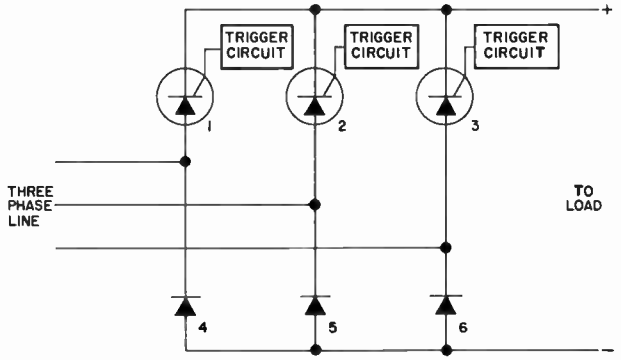


FIGURE 9.36 THREE PHASE BRIDGE CIRCUIT WITH THREE CONTROLLED LEGS

In some special cases it is desirable to control all six elements of the three phase bridge circuit. Regenerative braking of a DC machine where either field or armature reversing is provided is an example of such a case. For this case, triggering signals capable of being phase-shifted over 120 electrical degrees must be supplied as shown in Figure 9.37(c).

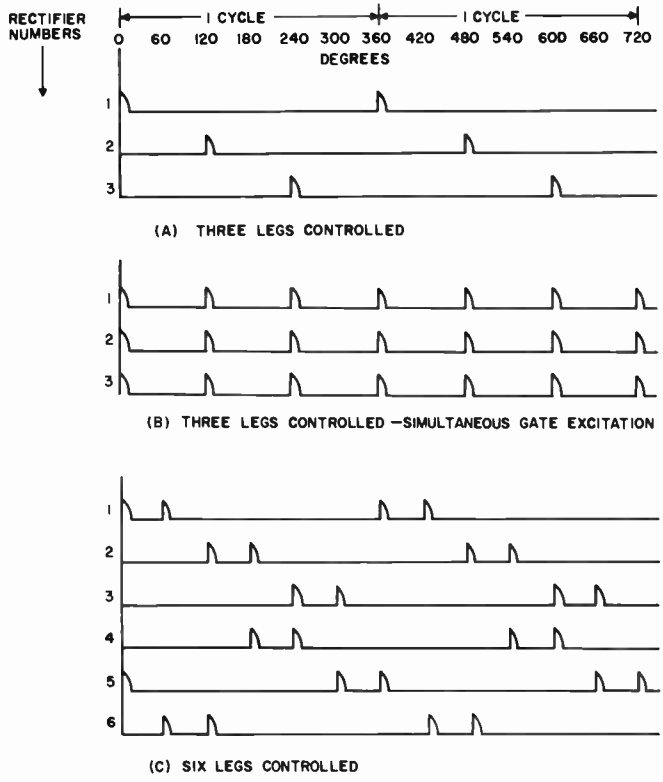


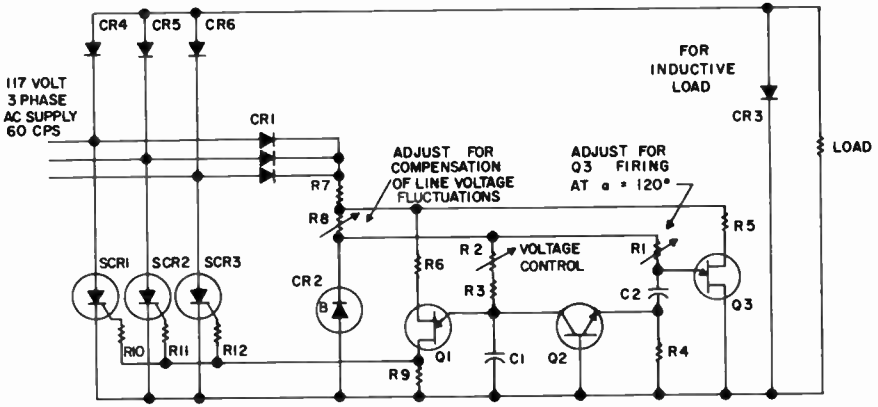
FIGURE 9.37 TRIGGERING PULSES FOR THREE PHASE BRIDGE CIRCUIT

9.9.1 Simple Three Phase Firing Circuit (25% to 100% Control)

This section describes a simple three-transistor SCR firing circuit that provides stepless control of the DC output voltage from a three-phase bridge between 25% and 100% of maximum output voltage, and also full interruption of output voltage. Means are incorporated to provide automatic compensation for line voltage fluctuations and for phase unbalance without closed-loop feedback.

This circuitry is readily applicable wherever stepless control is not required over the full range from zero to 100% of the maximum DC output voltage. Its main features are its simplicity, low cost, compactness, and reliability. Its inherent characteristics provide symmetrical output in all three phases without the need for special matching and adjustment of individual

circuits, and the circuit is insensitive to power factor or phase reversal. It lends itself readily to electrical feedback techniques and does not require a separate control voltage supply. No magnetic components are needed.



CR1 — (3) G E IN1695
CR2 — 20 VOLT, 1 WATT ZENER DIODE, IN1527
CR3, CR4, CR5, CR6 — AS REQUIRED FOR LOAD (e.g. IN2156)
SCR1, SCR2, SCR3 — AS REQUIRED FOR LOAD (e.g. C358)
Q1, Q3 — G E 2N2646 Q2 — G E 2N2923
R1 — 10K POT
R2 — 20K POT
R3 — 470 Ω
R4 — 100 Ω
R5, R6 — 390 Ω
R7 — 3.3K, 2W
R8 — 500 Ω POT, 2W
R9 — 100 Ω
R10, R11, R12 — 25 Ω
C1 — 0.5 MFD
C2 — 1.0 MFD

FIGURE 9.38 SIMPLE THREE PHASE FIRING CIRCUIT

Figure 9.38 illustrates the complete firing circuit. CR_1 supplies positive line voltage to the control circuit whenever the anode voltage on an SCR swings positive with respect to the positive DC bus. This voltage is clipped at 20 volts by zener regulator CR_2 and supplies a conventional unijunction transistor relaxation oscillator firing circuit of a type described in detail in Chapter 4. R_2 controls the firing angle of Q_1 by regulating the charging rate to capacitor C_1. The pulse of voltage developed across R_9 as unijunction Q_1 discharges C_1 is coupled simultaneously to the gates of all three controlled rectifiers, SCR_1, SCR_2, and SCR_3, through R_{10}, R_{11}, and R_{12}. Whichever SCR has the most positive anode voltage at the instant of the gate pulse starts conduction at that point.

The circuit composed of transistors Q_2 and Q_3 prevents Q_1 from firing at any delay angle greater than 120°. If triggering pulses are retarded beyond 120°, the output voltage rises abruptly to 100% as the following phase is fired at the beginning of its cycle. Q_3 is an independent unijunction oscillator which initiates its timing cycle at the same instant as Q_1. R_1 is set at a fixed value so that Q_3 fires at an angle slightly less than 120°. Two modes of operation are possible:

1. If Q_1 triggers before retard angle $\delta = 120°$; it fires the SCR whose positive anode voltage is providing the interbase bias for the unijunctions through CR_1. Firing this SCR shorts the control circuit supply voltage. The interbase bias voltage of Q_3 drops to zero, causing Q_3 to fire and discharge C_2 in preparation for the next cycle. This is the mode of operation when Q_1 is controlling the DC output voltage between 25% and 100% of maximum. In this mode, Q_2 and Q_3 have no effect on the functioning of the bridge.
2. If Q_1 is delayed beyond $\delta = 120°$, Q_3 fires, discharging C_2 through the base-emitter junction of Q_2, saturating this device, and discharging C_1 through Q_2. This alternate mode of discharging C_1 does not impose a pulse on the SCR gates, and the DC output voltage is therefore zero in this mode.

Instead of mechanical manipulation of potentiometer R_2 to control the DC output voltage, electrical signals can be used to control the output by inserting a transistor in series with R_2 in the charging path for C_1, or alternately a transistor in shunt with C_1. Both methods are readily useful in conjunction with feedback systems and are described in Chapter 4, and in Section 9.5.

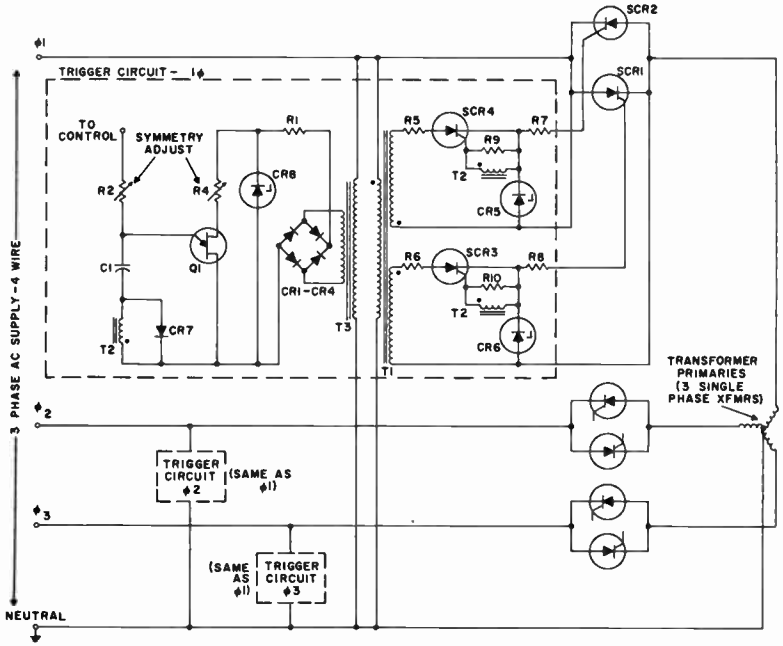
The success of this circuit depends on Q_3 maintaining its firing angle at slightly less than 120°. For this reason, base 2 of unijunction transistor Q_3 is connected through R_5 to a point separated from the clipped and regulated voltage across CR_2 by resistor R_8. This acts to maintain the timing cycle of Q_3 fixed at slightly less than 120° regardless of normal line voltage variations. Without this precaution, a drop in line voltage would make Q_3 fire at a somewhat greater angle than 120° due to the lesser slope on the front of the clipped sine wave voltage being applied to R_1.

R_8 serves another useful purpose. By connecting base 2 of unijunction transistor Q_1 to the top of R_8, a marked degree of regulation of the DC output voltage is provided for AC line voltage fluctuations. If the line voltage rises, the interbase bias voltage and therefore the peak-point emitter voltage on Q_1 rises depending on the setting of R_8. Since the emitter charging circuit through R_2 is connected to the fixed voltage across regulator CR_2, the firing angle is phased back and the output DC voltage is maintained constant. For a decrease in line voltage, this action advances the firing angle to maintain the output constant. This inherent action is instantaneous and does not depend on a change in the actual output voltage to take corrective action. Where unequal phase voltages exist, this circuit also acts to balance the contribution of the individual phases to the DC output voltage, thus reducing the fundamental frequency ripple content in the DC. Since the compensation provided by R_8 is not constant at all firing angles, R_8 should be adjusted for optimum action near the voltage level at which operation will normally take place.

With a three-phase 117 VAC supply, the circuit in Figure 9.38 can be varied steplessly over DC output voltages from 40 volts to 150 volts DC, a range of 3.75 to 1. It can also be turned off completely. With line voltage variations of ±10%, R_8 can be adjusted to provide essentially constant DC output voltage at both extremes of line voltage. Test data with $R_8 = 350$ ohms, with 10 ohms of load, and with G-E C35B cells as the SCR's showed that for a variation in AC line input voltage from 130 volts to 100 volts the DC output varied from 93 volts to 92 volts.

9.9.2 Full Range Three Phase Control System

Figure 9.39 illustrates a phase-controlled circuit for a four wire AC system feeding three wye-connected transformers. One pair of SCR's is connected in series with each of the lines and the transformer neutral is connected to the system neutral. Trigger circuits similar to the single phase type are connected from line to neutral of each phase. For illustrative purposes, a unijunction transistor is used to trigger the pilot SCR's. So that all three trigger circuits can be controlled simultaneously with a single adjustment or electrical signal, each unijunction circuit is isolated from the power circuit by a transformer T_3. This permits the three unijunction circuits to be electrically inter-connected at any convenient point. Several variations for controlling the three unijunctions from a master signal are shown in Figure 9.40. The most suitable type depends on whether manual or electrical control is desired, also the magnitude and impedance level of the available master control signal.



R1 - 3.3K, 5 WATT
R2 - SEE FIG. 8
R4 - 10K, 1 WATT
R5, R6 - 22Ω, 2 WATT
R7, R8 - 33Ω, 2 WATT
R9, R10 - 47Ω, 1/2 WATT

C1 - 0.1 MFD
Q1 - G E 2N2646
SCR1, SCR2 - AS REQUIRED
SCR3, SCR4 - G E 2N1595
CR1 TO CR4 - G E 1N1693
CR5, CR6 - G E 1N1765
CR7 - G E 1N1692
CR8 - G E 1N1776

T1 - ISOLATION TRANSFORMER WITH 12.6 VOLT, 1/4 AMP, SECONDARIES, PRIMARY AS REQUIRED FOR SPECIFIC LINE VOLTAGE

T2 - PULSE TRANSFORMER PE 2229, UTC H51 OR EQUIVALENT

T3 - ISOLATION TRANSFORMER WITH 120 VOLT, 50 MA SECONDARY, PRIMARY AS REQUIRED FOR SPECIFIC LINE VOLTAGE (FOR 120 VOLT PRIMARY, TRIAD N-51X)

FIGURE 9.39 PHASE CONTROL FOR THREE PHASE, FOUR WIRE POWER SYSTEM FEEDING WYE CONNECTED TRANSFORMERS.

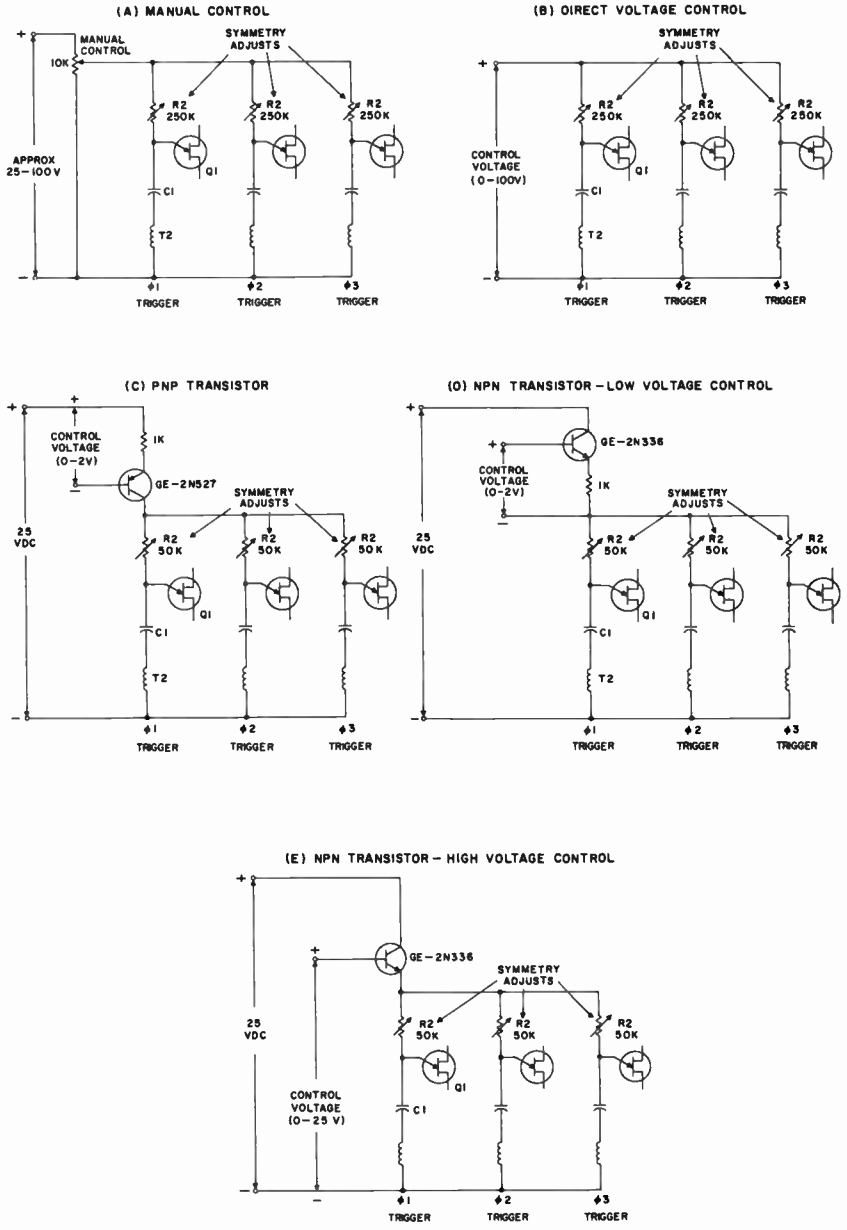


FIGURE 9.40 CONTROL CIRCUITS FOR THREE PHASE CIRCUIT OF FIGURE 9.39

Adjustments are provided in each unijunction circuit for establishing symmetrical firing between the phases. R_4 in each circuit is set so that all three unijunctions trigger at the same emitter voltage (voltage across C_1 and primary of T_2). R_2 is then adjusted for equal tracking of all three phases to a single control signal, such as the manual control setting in Figure 9.40(a).

Proper operation of the circuit of Figure 9.39 requires significant currents to be carried in the neutral connection and care must be taken in designing the power conductors and supply for this purpose. This circuit will not work over the complete voltage range with a delta connected transformer. Neither will it provide smooth control of the load voltage without the neutral connection between the supply and the wye connected transformers. In either of these two cases discontinuities in the load voltage occur as the control signal is varied.

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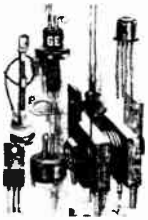
2. "The Silicon Controlled Rectifier in Lamp Dimming and Heating Control Service," E. E. Von Zastrow, General Electric Company, Auburn, N. Y., Application Note 200.14.*
3. "Phase-Controlling Kilowatts With Silicon Semiconductors," F. W. Gutzwiller, *Control Engineering*, May, 1959.
4. "Application of Silicon Controlled Rectifiers in a Transistorized High-Response DC Servo System," C. Cantor, AIEE CP 60-864, American Institute of Electrical Engineers, Summer General Meeting, June, 1960.
5. "Speed Controls for Universal Motors," A. A. Adem, General Electric Company, Auburn, N. Y., Application Note 200.47.*
6. "Phase Control of SCR's With Transformer and Other Inductive AC Loads," F. W. Gutzwiller and J. D. Meng, General Electric Company, Auburn, N. Y., Application Note 200.31.*
7. "Using the Triac for Control of AC Power," J. H. Galloway, General Electric Company, Auburn, N. Y., Application Note 200.35.*
8. Semiconductor Controlled Rectifiers—Principles and Applications of p-n-p-n Devices, F. E. Gentry, et al., Prentice-Hall, Inc., Englewood Cliffs, N. J., 1964.

*Refer to Chapter 22 for availability and ordering information.

10 MOTOR CONTROLS EMPLOYING PHASE CONTROL



10.1 INTRODUCTION

Since the AC power line is so universally convenient, and since phase control is the most convenient way of regulating this power source, it is little wonder that phase control has been used to control such a wide variety of motor types. Most of the motors so controlled however were not designed for this type of operation and were used because they were available or were low priced. Often the simplicity of the control circuits is due to a dependence on motor characteristics, and an improper motor selection will cause poor circuit operation. Also, even the best control circuit is only part of an overall system, and can be no more successful than the overall system design.

Most motors are given their ratings based on operation at a single speed, and depend on this speed for proper cooling. Attempts to use a motor at a lower speed can cause heating problems. The lubrication of bearings can be inadequate for low-speed operation. The presence of odd order harmonics in the phase-controlled wave form, can produce some odd side effects in induction motors. The speed vs. torque characteristic of a particular induction motor may make it totally unsuitable for use with a variable voltage control system. Some controls for universal series motors depend heavily on the existence of a significant residual magnetism in their magnetic structures, a characteristic that the motor vendor could be inadvertently trying to minimize.

These potential problems are brought up to point out the importance of checking with the motor manufacturer to insure that the motor used is the proper one for this type of use.

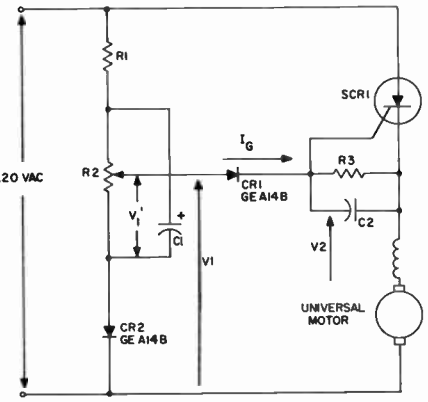
The use of a properly chosen and designed motor with a control of this type can however allow a wide versatility in application. For instance with a temperature compensated furnace blower control, a wide variety of motor sizes and speeds need no longer be used. A single, standard motor could be used with the variable requirements in different installations being compensated by means of electrical adjustments at the control. In some cases, where the maximum speed of the motor is set by the control, the need for designing overvoltage capability into the motor is eliminated, thus allowing some saving in the motor design.

10.2 BRUSH-TYPE MOTORS CONTROLLED BY BACK EMF FEEDBACK

In order for a circuit to control the speed of a motor, it must be able to somehow sense the speed of that motor. The most easily available way to get this information from brush-type motors is by looking at the back EMF generated by the motor during the time that the controlling SCR is off. In the case of separately excited shunt field wound, and permanent magnet field motors, this EMF is directly proportional to speed. In series motors, the field

is not energized at this time, and residual magnetism must provide the back EMF used by the circuit. Unfortunately, the residual magnetism is a function of the past history of motor current, so the voltage the circuit sees is not a function of speed alone.

Care must also be taken in these circuits that brush noise does not interfere with circuit operation.

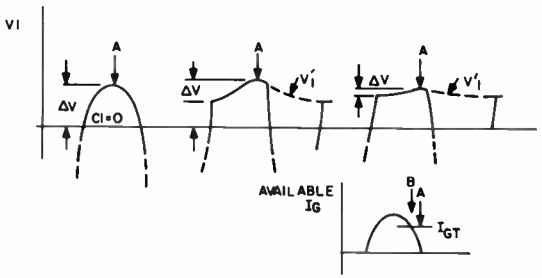


(A)

	LOW UP TO 1 AMP NAMEPLATE	MEDIUM UP TO 3 AMP NAMEPLATE	HIGH UP TO 15 AMP NAMEPLATE
R2	10K 1W	1K 2W	1K 2W
R1	47K 1/2 W	3.3K 2W	3.3K 2W
R3	1K 1/2W	150K 1/2W OPTIONAL	150K 1/2W OPTIONAL
C1	0.5μf 50V	10μf 50V	10μf 50V
C2	0.1 μf 10V	0.1μf 10V OPTIONAL	0.1μf 10V OPTIONAL
SCR1	GE C106B	GE C22BX70	GE C33B

(B)

FIGURE 10.1 UNIVERSAL SERIES MOTOR CONTROL WITH FEEDBACK



(a) WITHOUT C1 (b) WITH C1 (c) WITH LARGER C1

FIGURE 10.2 WAVESHAPES FOR FIGURE 10.1

10.2.1 Half-Wave Universal Series Motor Controls

The universal series motor finds use in a wide variety of consumer and light industrial applications. It is used in blenders, hand tools, vacuum cleaners, mixers, and in many other places. The control circuits to be described here can provide in effect an infinitely variable tap on the motor.

The half-wave circuits of Figures 10.1 and 10.3 supply half wave DC to the motor. In order to have full-speed operation with these circuits, the motor must be designed for a nominal voltage of around 80 volts for operation on 120 volt AC lines. Brush life of a motor driven by a half-wave supply may be

somewhat shorter than for a corresponding motor on full-wave AC.

The two half-wave circuits shown, both employ residual back-EMF feedback to provide increased motor power as the speed of the motor is reduced by mechanical loading. This back EMF voltage is dependent on the residual magnetism of the motor which is determined by the magnetic structure of the motor and the characteristics of the iron. Care must be taken to ensure that the motor used has sufficient residual magnetism. For more information see Reference 1.

The circuit of Figure 10.1 operates by comparing the residual back EMF of the motor V_2 with a circuit generated reference voltage V_1. If the capacitor C_1 is not present, the voltage V_1 is the result of the divider network composed of R_1 and the potentiometer R_2. Current flows in this branch only during the positive half-cycle due to diode CR_2. The voltage at V_1 then is a half sine wave with a maximum value at time "A" (Figure 10.2(a)). If the residual back EMF is greater than this maximum (the motor is going faster than the selected speed), CR_1 will be reverse biased and the SCR will not be triggered and will not supply power to the motor during this half cycle. As the motor slows down and its back EMF drops, V_2 will become slightly less than V_1 at time "A," causing current to flow through CR_1 and the gate of SCR_1, thus triggering the SCR. The speed at which this occurs may be varied by changing the magnitude of V_1 by adjusting potentiometer R_2. Notice that the smallest impulse of power that can be applied to the motor is one-quarter cycle, since the latest point in the cycle that the SCR can trigger is at the peak of the AC line voltage.

If the motor is loaded down so that its speed and back-EMF continue to drop, the time at which V_1 becomes greater than V_2 comes earlier in the cycle causing the SCR to trigger earlier, supplying more power to the motor. If, however, the motor is lightly loaded and running at a low speed, one-quarter cycle power may be enough to change the motor speed by a considerable amount. If this happens, it may take a considerable number of cycles to return to the speed at which the SCR will again trigger. This causes a hunting or "cogging" effect which is usually accompanied by an objectionable amount of mechanical noise.

In order to alleviate this problem, the smallest increment of power available must be reduced from a full-quarter cycle to that amount required to just compensate for the motor energy lost per cycle. To accomplish this, capacitor C_1 is added to the circuit. The capacitor voltage becomes a sinusoid in shape during the positive half cycle. This voltage is phase shifted by an amount determined by the circuit time constant and an exponential decay during the negative half cycle.

Figure 10.2(b) shows the results on V_1. Two main effects may be observed. The first is that the latest possible triggering point "A" is delayed, thereby considerably reducing the smallest increment of power. The second is that the amount of change of V_2 required to go from minimum power to full power, ΔV, is reduced, providing a more effective control. Increasing C_1 even more produces the results of Figure 10.2(c). It can be seen that the triggering point "A" comes still later, and ΔV becomes still smaller. Care must be taken however not to go too far in this direction, for increasing C_1 decreases ΔV and increases the loop gain of the system which could lead again to instability and hunting (see Chapter 12).

It is important that the impedance level of the network formed by R_1, R_2 and C_1 be low enough to supply the current required to trigger the SCR

without undue loading. It can be seen in Figure 10.2(c) that this current available for triggering from this network approaches a sine wave, with its peak at 90°. If the current required to trigger the SCR is I_{GT} as shown, the latest possible firing point would be at "B," not at "A" as one would believe from the voltage wave shape.

In many cases, good low-speed operation without a restrictive specification on gate current to fire would require such a low impedance network that the power ratings of the resistors and the capacitor size would become unwieldly and expensive. In such cases, a low-voltage trigger device such as an SUS can act as a gate amplifier as in Figure 10.3. Use of the SUS in this circuit allows a much higher impedance network to be used for R_1, R_2 and C_1, hence allowing smaller size and lower cost components. In this circuit the reference voltage V_1 must exceed the back EMF V_2 by the breakover voltage of SUS_1, which is about 8 to 10 volts. When SUS_1 triggers it discharges C_2 into the gate, supplying a strong pulse of current to trigger SCR_1. This eliminates any need to select SCR's for gate trigger current, and eliminates any circuit dependence on the trigger current of the particular SCR used.

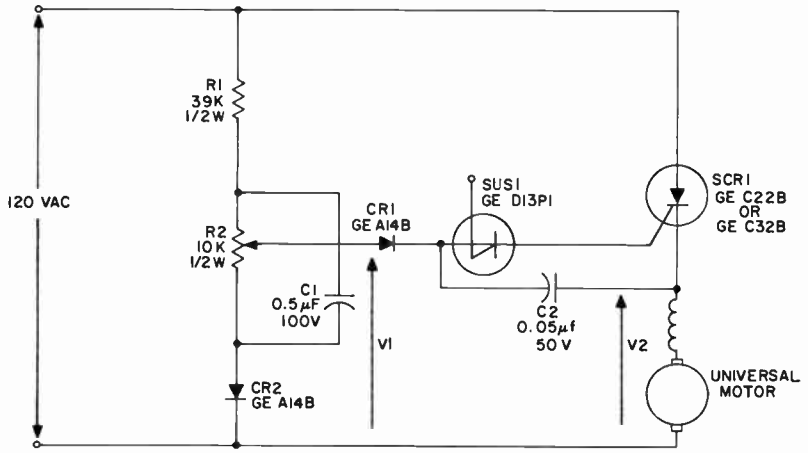


FIGURE 10.3 SUS TRIGGERED UNIVERSAL SERIES MOTOR SPEED CONTROL WITH FEEDBACK.

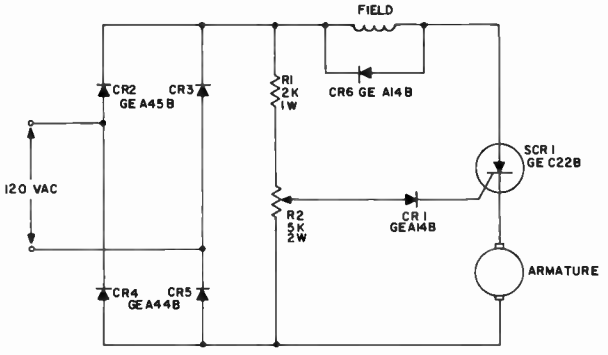


FIGURE 10.4 FULL WAVE DC CONTROL WITH FEEDBACK

10.2.2 Full Wave Universal Series Motor Control

Figure 10.4 shows the circuit of a full wave series motor speed control with feedback which requires that separate connections be available for the motor armature and field. The full wave bridge supplies power to the series networks of motor field, SCR_1 and armature, and R_1 and R_2. Basically this circuit works on the same principle as that of Figure 10.1(a) using the counter EMF of the armature as a feedback signal. When the motor starts running, the SCR fires as soon as the reference voltage across the arm of R_2 exceeds the forward drop of CR_1 and the gate to cathode drop of SCR_1. The motor then builds up speed, and as the back EMF increases, the speed of the motor adjusts to the setting of R_2 in the same manner as the circuit of Figure 10.1(a).

One of the drawbacks of this circuit is that at low speed settings, because of the decreased back EMF, the anode to cathode voltage of the SCR may not be negative for a sufficient time for the SCR to turn off. When this happens, the motor receives full power for the succeeding half cycle and the motor starts hunting. Furthermore, this circuit is limited by the fact that SCR_1 cannot be fired consistently later than 90°. A capacitor on the arm of R_2 is not a cure because there will be no phase shift on the reference due to full wave rectified charging.

10.2.3 Shunt Wound and P-M Field Motor Control

The shunt-wound DC motor is well suited for use with solid state speed control systems to provide smooth, wide-range control of speed. The speed of a shunt motor is inherently reasonably constant with changes in torque, thus permitting speed control to be achieved by controlling the voltage applied to the armature. The use of a small compound series winding can make the speed virtually independent of torque. Likewise, a small amount of feedback of speed information into the control that supplies armature voltage will reduce variations of speed with torque.

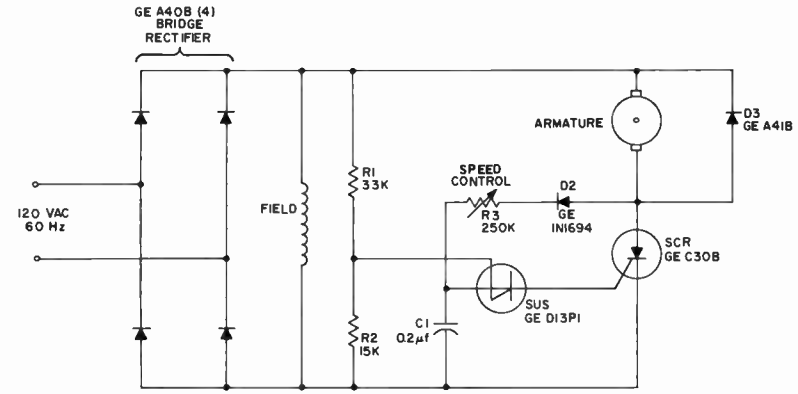


FIGURE 10.5 SPEED CONTROL FOR ½ HP, 115 VOLT SHUNT-WOUND DC MOTOR

Figure 10.5 shows a simple and low-cost solid state speed control for shunt-wound DC motors. This circuit uses a bridge rectifier to provide full wave rectification of the AC supply. The field winding is permanently connected across the DC output of the bridge rectifier. Armature voltage is supplied through the SCR and is controlled by turning the SCR on at various points in each half cycle, the SCR turning off only at the end of each half cycle. Rectifier D_3 provides a circulating current path for energy stored in the inductance in the armature at the time the SCR turns off. Without D_3, the current will circulate through the SCR and the bridge rectifier thus preventing the SCR from turning off.

At the beginning of each half cycle the SCR is in the OFF state and capacitor C_1 starts charging by current flow through the armature, rectifier D_2, and the adjustable resistor R_3. When the voltage across C_1 reaches the breakover voltage of the SUS trigger diode, a pulse is applied to the SCR gate, turning the SCR on and applying power to the armature for the remainder of that half cycle. At the end of each half cycle, C_1 is discharged by the triggering of the SUS, resistor R_1, and current through R_1 and R_2. The time required for C_1 to reach breakover voltage of the SUS governs the phase angle at which the SCR is turned on and this is controlled by the magnitude of resistor R_3 and the voltage across the SCR. Since the voltage across the SCR is the output of the bridge rectifier minus the counter EMF across the armature, the charging of C_1 is partially dependent upon this counter EMF, hence upon the speed of the motor. If the motor runs at a slower speed, the counter EMF will be lower and the voltage applied to the charging circuit will be higher. This decreases the time required to trigger the SCR, hence increases the power supplied to the armature and thereby compensates for the loading on the motor.

Energy stored in armature inductance will result in the current flow through rectifier D_3 for a short time at the beginning of each half cycle. During this time, the counter EMF of the armature cannot appear hence the voltage across the SCR is equal to the output voltage of the bridge rectifier. The length of time required for this current to die out and for the counter EMF to appear across the armature is determined by both speed and armature current. At lower speeds and at higher armature currents the rectifier D_3 will remain conducting for a longer period of time at the beginning of each half cycle. This action also causes faster charging of capacitor C_1, hence provides compensation that is sensitive to both armature current and to motor speed.

This circuit provides a very large range of speed control adjustment. The feedback signal derived from speed and armature current improves the speed regulation over the inherent characteristics of the motor.

Inductance of the field winding of a shunt motor is generally rather large, resulting in a significant length of time required for the field current to build up to its normal value after the motor is energized. In general, it is desirable to prevent application of power to the armature until after the field current has reached approximately normal value. This sort of soft start function is readily added. For information on soft starting, see Chapter 9 and Reference 2.

This relatively simple approach is capable of moderately good speed regulation on the order of 10 percent. For higher performance, a tachometer feedback circuit as discussed in Section 10.4.3 can be substituted for the trigger circuit.

Permanent magnet motors behave quite similarly to shunt wound motors, since they both have field strengths independent of armature current. Hence the circuit of Figure 10.5 may also be used with a P-M motor.

Some special types of P-M motors, such as the so-called "printed circuit" motors, do not lend themselves readily to phase control. The effect of the low inductance, low resistance, and low operating voltage of these motors makes the peak-to-average current ratio excessive to an extreme, using phase control, causing high RMS currents in the line and therefore possible de-magnetization effects in the motor field magnets. This type of motor would therefore be more suitably controlled by means of a "chopper" type of circuit. This type of circuit will be discussed in Section 11.2.3.

10.3 BRUSH-TYPE MOTOR CONTROL—NO FEEDBACK

In many cases speed regulation is not required in the control. Where the load characteristics are relatively fixed, or where the motor drive is part of a larger overall servo system, a non-regulating control circuit may be used. In some cases, these non-regulating circuits can provide a considerable cost saving over regulated types.

10.3.1 Half-Wave Drive for Universal, Shunt or P-M Motors

Figure 10.6 illustrates one of the simplest and least expensive half wave circuits. It uses one SCR with a minimum amount of components. The series network of R_1, P_1, and C_1 supplies a phase shift signal to the neon bulb which triggers the SCR. Thus, by varying the setting of potentiometer P_1, the gate signal of the SCR is phase shifted with respect to the supply voltage to turn the SCR on at varying times in the positive AC half cycles. V_c fires the neon bulb on both positive and negative half cycles. The negative half cycles can be disregarded since both the trigger pulses and the anode voltage of the SCR are negative.

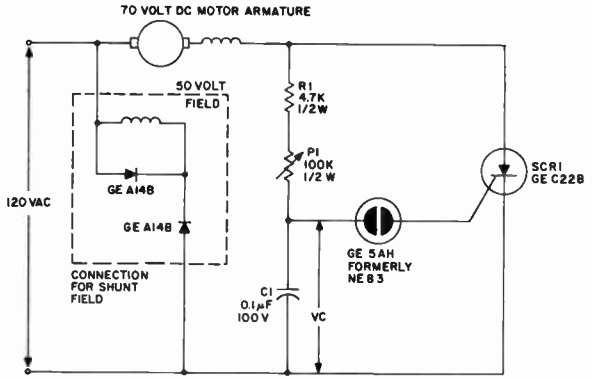


FIGURE 10.6 HALF-WAVE CONTROL WITHOUT FEEDBACK (NEON TRIGGERED)

By replacing the neon with a trigger device, such as a Diac (the GE ST2) or a Silicon Unilateral Switch (the GE D13PD1), the performance and reliability of the circuit of Figure 10.6 can be improved considerably because semiconductor trigger devices are longer-lived and have a more stable firing point than neon bulbs. Also, because of their lower trigger voltage, these solid state trigger devices give a wider control range. The values of the R-C phase shift network would have to be increased to compensate for the lower breakover voltages of these devices.

10.3.2 Full-Wave AC Drive for Universal Series Motors

Since the universal series motor is generally designed to run on the 60 Hz AC line, the simplest approach to a non-regulating control is the full wave phase control circuit of Figure 10.7. More details on the operation of this type of circuit can be found in Chapter 9.

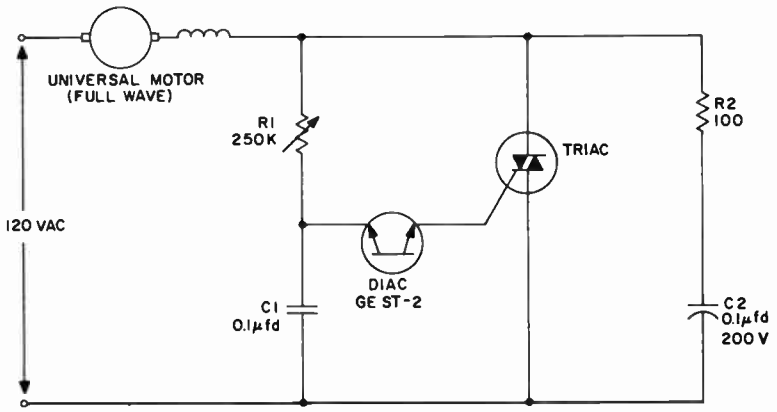


FIGURE 10.7 BASIC NON-REGULATED FULL-WAVE AC PHASE CONTROL FOR UNIVERSAL MOTORS.

10.3.3 Full Wave DC Motor Drives

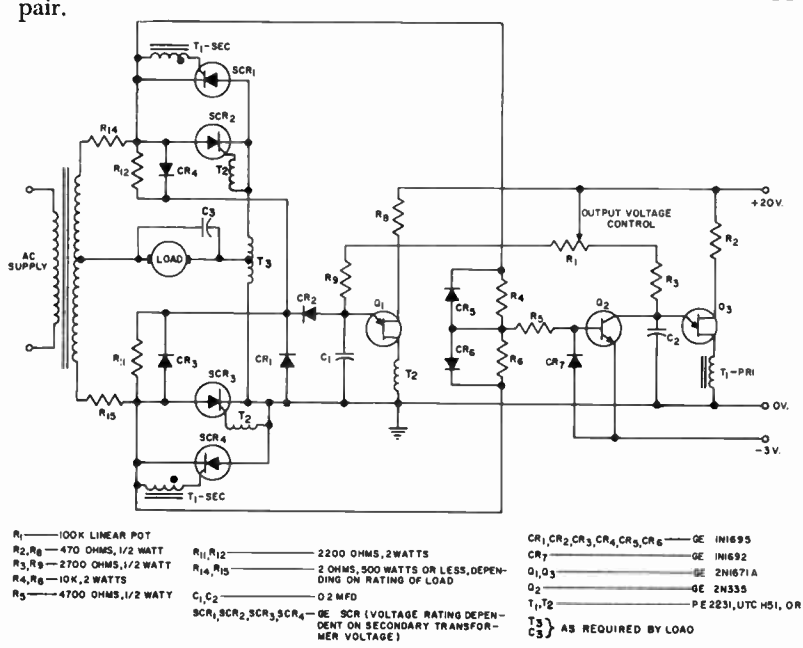
SCR's are well suited for supplying both armature power and field excitation to DC machines.

A full wave reversing control or servo as shown in Figure 10.8 can be designed around two SCR's with common cathode (SCR_2, SCR_3) and two SCR's with common anodes (SCR_1, SCR_4). In this circuit SCR_2 and SCR_3 are controlled by UJT Q_1 and the other pair, SCR_1 and SCR_4, are controlled by UJT Q_3. Transistor clamp Q_2 synchronizes the firing of Q_3 to the anode voltages across SCR_1 and SCR_4.

Potentiometer R_1 can be used to regulate the polarity and the magnitude of output voltage across the load. With R_1 at its center position, neither UJT fires and no output voltage appears across the load. As the arm of R_1 is moved to the left, Q_1 and its associated SCR's begin to fire. At the extreme left-hand position of R_1, full output voltage appears across the load. As the

arm of R_1 is moved to the right of center, similar action occurs except the polarity across the load is reversed.

If the load is a DC motor, plugging action occurs if R_1 is reversed abruptly. R_{14} and R_{15} are used in series with each end of the transformer to limit fault current in the event a voltage transient should fire an odd- or even-numbered SCR pair simultaneously. Commutating reactor T_3 and capacitor C_3 limit the dv/dt which one pair of SCR's can impress upon the opposite pair.



R_1 —— 100K LINEAR POT
R_2, R_8 — 470 OHMS, 1/2 WATT
R_3, R_9 — 2700 OHMS, 1/2 WATT
R_4, R_6 — 10K, 2 WATTS
R_5 —— 4700 OHMS, 1/2 WATT

R_{11}, R_{12} —— 2200 OHMS, 2 WATTS
R_{14}, R_{15} —— 2 OHMS, 300 WATTS OR LESS, DEPENDING ON RATING OF LOAD
C_1, C_2 —— 0.2 MFD
$SCR_1, SCR_2, SCR_3, SCR_4$ — GE SCR (VOLTAGE RATING DEPENDENT ON SECONDARY TRANSFORMER VOLTAGE)

$CR_1, CR_2, CR_3, CR_4, CR_5, CR_6$ —— GE IN1695
CR_7 —— GE IN1692
Q_1, Q_3 —— GE 2N1671A
Q_2 —— GE 2N335
T_1, T_2 —— PE 2231, UTC H51, OR EQUIVALENT
T_3, C_3 } AS REQUIRED BY LOAD

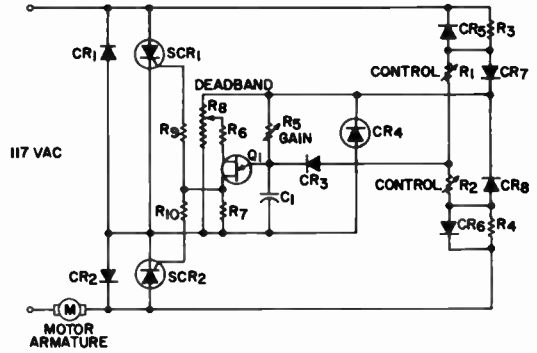
FIGURE 10.8 FULL WAVE REVERSING DRIVE

10.3.4 Balanced-Bridge Reversing Servo Drive

A phase-sensitive servo drive supplying reversible half wave power to the armature of a small permanent magnet or shunt motor is shown in Figure 10.9. The power circuit consists of two half-wave circuits back-to-back (SCR_1, CR_1; and SCR_2, CR_2) fired by unijunction transistor, Q_1, on either the positive or negative half-cycle of line voltage depending on the direction of unbalance of the reference bridge resulting from the value of the sensing element R_1. R_1 can be a photo-resistor, a thermistor, a potentiometer, or an output from a control amplifier.

The potentiometer R_8 is set so that the DC bias on the emitter of unijunction transistor, Q_1, is slightly below the peak-point voltage at which Q_1 fires, by an amount dependent upon the deadband desired. With R_1 equal to R_2 the bridge will be balanced, UJT (Q_1) will not fire and no output voltage appears across the load. If R_1 is increased thus unbalancing the bridge, an AC signal will appear at the emitter of the UJT causing the emitter to be biased above the firing voltage during one half-cycle of the AC. Q_1 will fire

and, since SCR_2 is forward biased, SCR_2 will fire. When R_1 is decreased, similar action occurs except that SCR_1 will fire, reversing the polarity across the load.



CR1, CR2, SCR1, SCR2 : AS REQUIRED BY LOAD

R1 : 3.3K } SEE NOTE	R6 : 1K		C1 : 0.1μf
R2 : 3.3K }	R7 : 47Ω		Q1 : GE 2N2646
R3 : 3.3K, 2W	R8 : 2500Ω		CR4 : GE IN1776
R4 : 3.3K, 2W	R9 : 47Ω		CR5-8 : GE IN1695
R5 : 2 MEGOHMS	R10 : 47Ω		CR3 : GE IN1692

NOTE:
EITHER R1 OR R2 MAY BE A VARIABLE RESISTANCE TRANSDUCER, SUCH AS THE GE B4258 PHOTOCONDUCTOR, OR THE GE ID301 THERMISTOR, OR A POSITION SENSING POTENTIOMETER.

FIGURE 10.9 BALANCED-BRIDGE REVERSING SERVO DRIVE FOR SHUNT-WOUND MOTOR.

10.4 INDUCTION MOTOR CONTROLS

There are a wide variety of induction motor types and within these a wide range of possible characteristics. Some of these characteristics can make a given motor type unsuited for control by means of phase control. The most obvious difficulty is that induction motors tend to be more frequency sensitive than voltage sensitive, while phase control generates a variable-voltage, constant-frequency source. If the motor was not designed for use with phase control, the motor designer may have accentuated this problem in order to get better speed regulation. In general, the motor used should be as voltage sensitive as possible. Variable voltage drive of induction motors is a compromise, one usually dictated by economics but very satisfactory in properly implemented applications. A variable frequency drive would be superior in some applications, but generally far more expensive than phase control. Information on variable frequency inverters that can be used for drives can be found in Chapter 11.

Certain types of single phase induction motors, notably split-phase and capacitor start motors, require a switched start winding. Since there is a torque discontinuity when the start switch cuts in or drops out, it would be impossible to control the speed of the motor around these points. This means that where the higher starting torque of a switched start winding is required, the motor should be designed so that the switching point is below the range of speed over which phase control is desired.

Another important consideration is the power factor of the motor. An

overly inductive motor can require a fair degree of sophistication in the control in order to avoid the problems associated with phase control of inductive loads. This topic is covered in detail in Section 9.6.

10.4.1 Non-Feedback Controls

Unlike brush type motors, induction motors give no convenient electrical indication of their mechanical speed. This means that direct speed feedback is not nearly as easily available. For some applications like fixed fan loads, direct voltage adjustment with no feedback yields satisfactory performance. An example is the circuit of Figure 10.7 when working with a permanent split capacitor motor or with a shaded pole motor. The need for the proper motor-load combination is shown by the speed torque curves of Figure 10.10. In the case of a low rotor resistance, Figure 10.10(a), it can be seen that varying the voltage of this motor will produce very little speed variation, while the higher rotor resistance motor of Figure 10.10(b) would give satisfactory results.

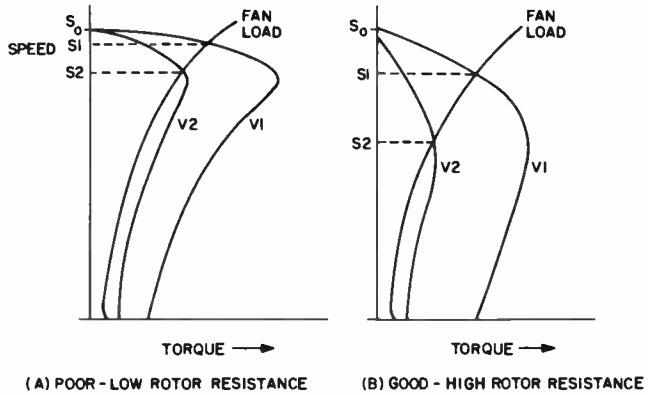


FIGURE 10.10 INDUCTION MOTOR SPEED-TORQUE CURVES FOR USE WITH A FAN-TYPE LOAD.

10.4.2 Indirect Feedback

Often the problem of speed regulation of induction motors may be bypassed by considering the complete system control problem. As an example, consider the problem of controlling the speed of the blower in a hot air heating system in response to the temperature of the air. It can be seen that what is of prime interest is the temperature of the air, not the precise speed of the motor. This kind of analysis can lead to the circuit of Figure 10.11.

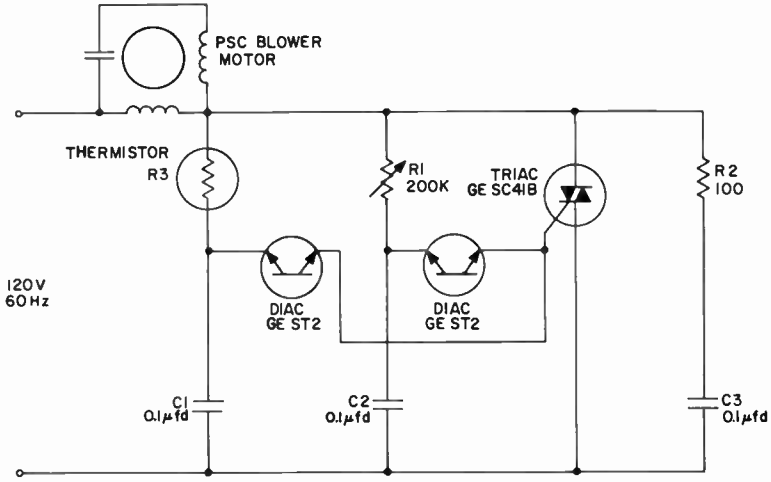
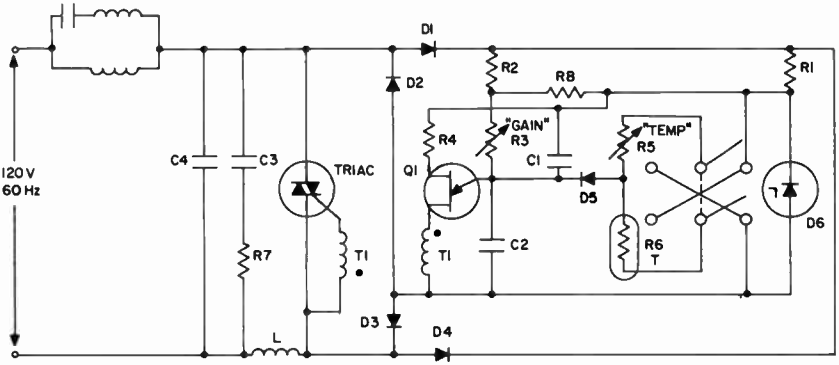


FIGURE 10.11 FURNACE BLOWER CONTROL

In this circuit, thermistor R_3 acts in response to air temperature to control the power supplied to the motor. Resistor R_1 and its phase control network serve to set a minimum blower speed, to provide continuous air circulation and to maintain motor bearing lubrication.

Figure 10.12 gives an example of a more sophisticated control system, capable of a much higher control gain. This could be used to control a blower motor in response to room temperature for heating control, or in response to cooling coil temperature to prevent air conditioner freeze-up.



D1→D4 : GE A148
D5 : GE A14 A
D6 : GE IN1776
Q1 : GE 2N2646
C1 & C2 : 0.1μf, 50V

R1 : 6800Ω 2W
R2 : 470KΩ 1/2W
R3 : 5 MEG 1/2 W
R4 : 1KΩ 1/2W
R5 : 10KΩ 1W
R6 : SEE NOTE

R7 : 33Ω 1/2 W
C3 : 0.02μf, 200V
T1 : XFMR 1:1
:SPRAGUE 11Z12 OR EQUIV.
C4 : 0.1μf 400V
R8 : 470KΩ 1/2W

NOTE: IN THE ABOVE ARRANGEMENT CIRCUIT IS SET UP FOR A HEATING APPLICATION. IN A COOLING APPLICATION R6 & R5 ARE INTERCHANGED. R6 SHOULD BE A THERMISTOR WHICH WILL AFFORD 3KΩ TO 5KΩ AT TEMPERATURE DESIRED. "TEMP ADJ" R5 SHOULD BE SET UP TO PROVIDE FULL "ON" AT DESIRED UPPER TEMP. OF THE THERMISTOR R6. "GAIN" R3 OR "BANDWIDTH" MAY THEN BE SET FOR "FULL OFF" (ZERO SPEED) CONDITION AT DESIRED "LOWER TEMP" OF R6.

FIGURE 10.12 TEMPERATURE CONTROL OF SPEED; SHADED POLE AND PSC MOTORS.

This is a ramp-and-pedestal system designed for the control of fan or blower motors of the shaded pole or permanent split capacitor type in response to temperature of a thermistor. The circuit includes RF noise suppression and dv/dt suppression.

10.4.3 Speed Regulating Control of Induction Motors

In order to actually regulate the speed of an AC induction motor by means of phase control, it is necessary to provide speed information to the circuit by means of a small tachometer generator. Such a generator could be made quite inexpensively, as high precision is not necessarily required. In addition, the speed torque characteristics of the motor should be quite voltage sensitive such as that of Figure 10.10(b). A motor such as that of Figure 10.10(a) would be quite difficult to control in a stable manner, as the open loop system characteristics would be highly nonlinear through the controlled speed range. The drop-out point of the start switch, if present, should be below the lowest desired controlled speed.

Figure 10.13 shows a general block diagram of such a control system. For a practical circuit, a ramp and pedestal control circuit, with inductive load considerations (as shown in Figure 9.32) can be combined with the input connection shown in Figure 10.14. This connection is shown for an AC

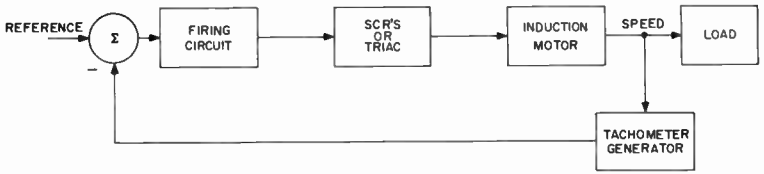


FIGURE 10.13 BLOCK DIAGRAM OF AN INDUCTION MOTOR SPEED CONTROL SYSTEM.

tachometer in the 4 to 6 volt range. The R_1-C_2 time constant is chosen to give adequate filtering at the lowest desired speed and tachometer frequency, consistent with system stability requirements (see Chapter 12). This system is also applicable to multiphase controls as well as DC motor drives.

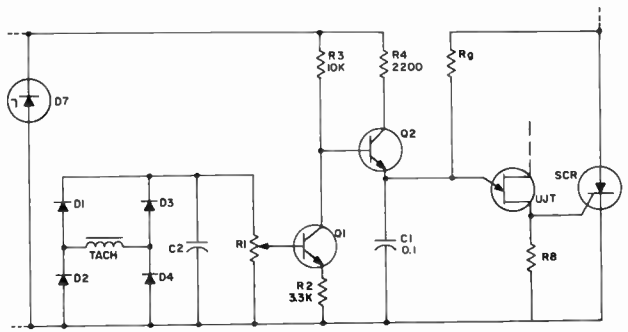


FIGURE 10.14 AC TACHOMETER CONNECTION TO A RAMP AND PEDESTAL FIRING CIRCUIT.

10.5 SOME OTHER MOTOR CONTROL POSSIBILITIES

In addition to controlling or varying the speed of a motor, there are several other control functions which can be done using solid-state control.

One of the simplest functions is the use of a triac as a static switch for contactor replacement. When used with a reversing-type permanent split capacitor motor, a pair of triacs can provide a rapidly responding, reversing motor control, as shown in Figure 10.15. S_1 and S_2 can be reed switches, or

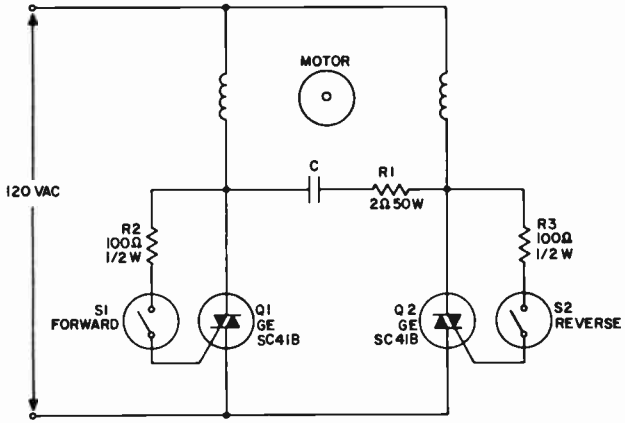


FIGURE 10.15 TRIAC CONTROL OF A REVERSIBLE PERMANENT SPLIT CAPACITOR MOTOR.

the triacs can be gated by any of a number of other methods. Also, use of a solid-state static switching circuit, with an appropriate firing circuit, can provide a motor overtemperature control which senses motor winding temperature directly.

10.5.1 Single-Phase Induction Motor Starters

In many cases, a capacitor start or a split-phase motor must operate where there is a high frequency of starts, or where arcing of the mechanical start switch is undesirable, such as where explosive fumes could be present in the neighborhood of the motor. In such cases, the mechanical start switch may be replaced by a triac. The gating and dropout information may be given to the triac in several ways.

Perhaps the simplest form of connection is to use a conventional current or voltage sensitive starting relay as pilot contacts for a simple triac static switch as shown in Figure 8.1(a).

Another method is that shown in Figure 10.16 which shows the triac gated on by the motor current through a small current transformer. As the motor speeds up, the current drops off and no longer fires the triac. A variation of this is to replace the current transformer with a small pickup coil, which is mounted near the end windings of the motor. This gives a somewhat more precise signal for the triac.

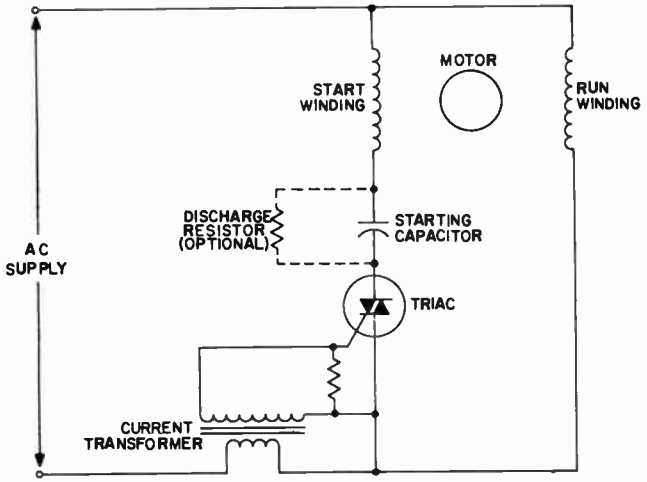


FIGURE 10.16 TRIAC MOTOR STARTING SWITCH

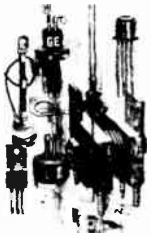
Where a tachometer generator is already sensing the speed of the motor, this same signal can be used to control a firing circuit for the triac. With this arrangement the dropout speed can be precisely set, so as to be outside the desired speed control range.

REFERENCES

1. "Speed Controls for Universal Motors," A. A. Adem, General Electric Company, Auburn, New York, Application Not 200.47.*
2. "Speed Control for Shunt-Wound DC Motors," E. Keith Howell, General Electric Company, Auburn, New York, Application Note 200.44.*
3. "Phase Control of SCR's With Transformer and Other Inductive AC Loads," F. W. Gutzwiller and J. D. Meng, General Electric Company, Auburn, New York, Application Note 200.31.*
4. "Using the Triac for Control of AC Power," J. H. Galloway, General Electric Company, Auburn, New York, Application Note 200.35.*

*Refer to Chapter 22 for availability and ordering information.

11 CHOPPERS, INVERTERS AND CYCLOCONVERTERS



This chapter describes choppers, inverters and cycloconverters using SCR's which perform the functions previously performed by electrical machines, mechanical contacts, spark gaps, vacuum tubes, thyratrons and power transistors. These functions include standby power supplies, vibrator power supplies, radio transmitters, sonar transmitters, variable-speed AC motor drives, battery-vehicle drives, ultrasonic generators, ignition systems, pulse-modulator switches, etc.

The advantages of using equipment with solid-state switches to perform these functions are:

Low maintenance
Reliability
Long life
Small size
Light weight
Silent operation
Insensitivity to atmospheric cleanliness or pressure
Tolerance of freezing temperatures
Operable in any attitude
Instantaneous starting
High efficiency
Low cost

11.1 CLASSIFICATION OF INVERTER CIRCUITS

The following definitions are used in this chapter:

Rectifier:	Equipment for transforming AC to DC
Inverter:	Equipment for transforming DC to AC
Converter:	Equipment for transforming AC to AC
DC Converter:	Equipment for transforming DC to DC
Cycloconverter:	Equipment for transforming a higher frequency AC to a lower frequency without a DC link
Cycloinverter:	The combination of an inverter and a cycloconverter
Chopper:	A "single ended" inverter for transforming DC to DC or DC to AC

Note: The term inverter is also used in this chapter as a generic term covering choppers, inverters, and the several forms of converters. Thus "Classification of Inverters" covers classification of Choppers, Inverters, Converters, and DC Converters.

11.1.1 Classes of Inverter Circuits (Table 11.1)

The basic classification of inverter circuits is by methods of turn-off. These have been described in Chapter 5. There are six classes:

Class A Self commutated by resonating the load[1]
Class B Self commutated by an LC circuit[2]
Class C C or LC switched by a load-carrying SCR[3]
Class D C or LC switched by an auxiliary SCR[4]
Class E External pulse source for commutation[5]
Class F AC line commutated[6]

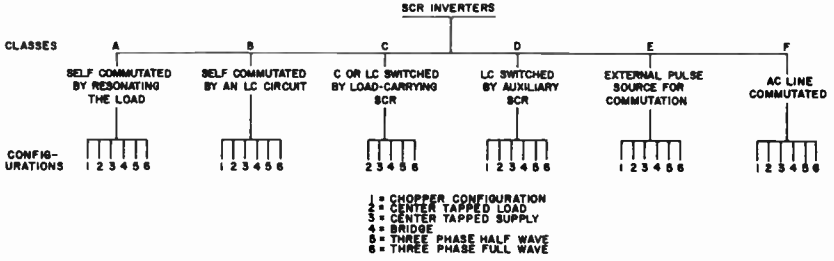


TABLE 11.1

11.1.2 Properties of the Inverter Classes

Class A—Self commutated by resonating the load. These inverters are most suitable for high-frequency operation, i.e., above about 1000 cps, because of the need for an LC resonant circuit which carries the full load current. The current through the SCR is nearly sinusoidal and so the initial di/dt is relatively low. Class A inverters lend themselves to output regulation by varying the frequency of a pulse of fixed width (time ratio control).

Class B—Self commutated by an LC circuit. The great merit of this class is circuit simplicity, the Morgan chopper being an outstanding example. Regulation is by time ratio control. Where saturable reactors are used, some skill is necessary in the design of these components, and manufacturing repeatability must be checked.

Class C—C or LC switched by a load-carrying SCR. An example of this class of inverter is the well known McMurray-Bedford inverter. With the aid of certain accessories this class is very useful at frequencies below about 1000 cps. External means must be used for regulation.

Class D—L or LC switched by an auxiliary SCR. This type of inverter is very versatile as both time-ratio and pulse-width regulation is readily incorporated. The commutation energy may readily be transferred to the load and so high efficiencies are possible.

Class E—External pulse source for commutation. This type of commutation has been neglected. It is capable of very high efficiency as only enough energy is supplied from the external source for commutation. Both time-ratio and pulse-width regulation are easily incorporated.

Class F—AC line commutated. The use of this type of inversion is limited to those applications where a large amount of alternating power is already available. Efficiencies are very high.

11.1.3 Inverter Configurations

Rectifier circuits occur in several configurations such as half-wave, full-wave, bridge, etc. Inverter circuits may be grouped in an analogous manner.

Figure 11.1 shows the different types of configurations. Methods of triggering and commutation have been left out for clarity.

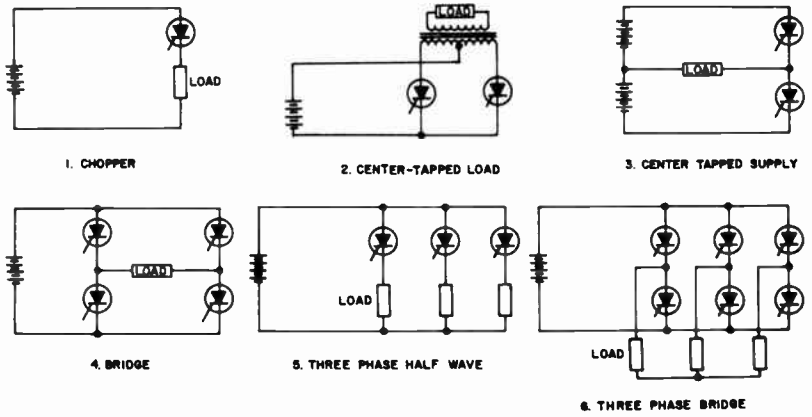


FIGURE 11.1 INVERTER CONFIGURATIONS

11.1.4 Properties of the Different Inverter Configurations

CONFIGURATION	1	2	3	4	5	6
	Chopper	CT Load	CT Supply	Bridge	3φ Half-Wave	3φ Bridge
Blocking Volts (1)	E	2E	E	E	E	E
Peak Load-Volts	E	E (2)	½ E	E	E	E (3)
DC in Load	yes	no	no	no	yes	no (4)
Number of SCR's	1	2	2	4	3	6
Ripple Frequency in Supply	f	2f	f	2f	3f	6f
Ave SCR Current (1) / Supply Current	1	1/2	1	1/2	1/3	1/3
Transformer-less Operation Possible	yes	no	yes	yes	yes	yes

(1) Ignoring overshoot due to commutation.
(2) Using a 1:1:1 transformer.
(3) Line-to-line voltage.
(4) Assuming symmetrical loading.

11.1.5 Discussion of Classification System

This method of classification gives thirty-five (35) different classes and configurations. However there are many circuits which could fall into the same classification and which are yet different. This occurs particularly in Class D where the method of commutating the auxiliary SCR may take many forms. There must therefore be several hundred possible inverter circuits.

In the following pages three examples are given to illustrate the scope of SCR inverters and the design procedure. The examples cover perhaps 1% of the possible circuit variations. It is for the equipment designer to use the classes and configurations together with the accessories to be described as building blocks to form the best combination for his particular application.

11.2 TYPICAL INVERTER CIRCUITS

11.2.1 A Class A Inverter

The design of Class A inverters has been well covered in the literature.[1] The following data, taken from Reference 1.11, illustrates the performance of one Class A inverter. Space does not permit the inclusion of the development of design procedures.

11.2.1.1 Circuit Description

The operation of the circuit is as follows. In Figure 11.2.1 when SCR_1 is triggered, current flows from the supply E_1 charging up capacitor C to a voltage approaching $2E_1$. The current then reverses and flows back to the supply via diode D_1 and C discharges. During the reverse current flow, turn-off time is presented to SCR_1. SCR_2 is triggered next and a similar cycle occurs in the lower half of the circuit with a negative going pulse of voltage appearing across C. SCR_1 is now triggered again and so the cycles repeat.

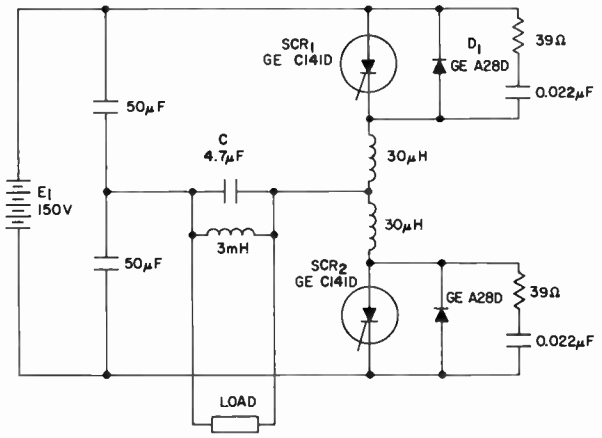
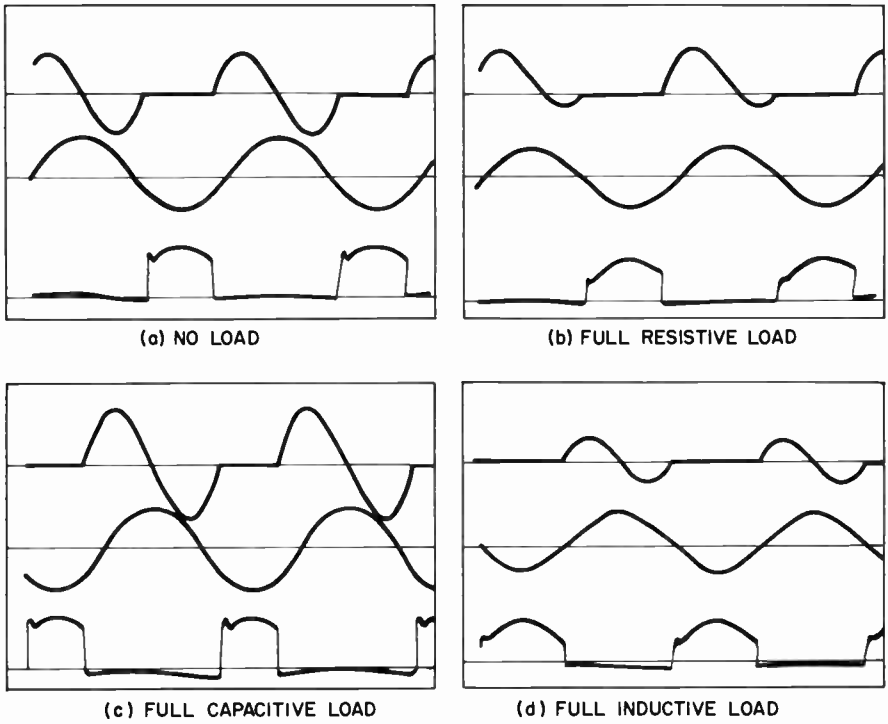


FIGURE 11.2.1 A CLASS A INVERTER CIRCUIT

Figures 11.2.2(a) and (b) show the circuit waveforms with no load and full load respectively. A comparison reveals some of the features of this new inverter. The output voltage, the peak SCR voltage, and the output voltage waveform remain virtually unchanged.



(A) SCR and Diode Current

(B) Output Voltage

(C) SCR Voltage (Anode to Cathode)

FIGURE 11.2.2 CLASS A INVERTER WAVEFORMS FOR CIRCUIT OF FIGURE 11.2.1

Figure 11.2.2(c) shows the effect of a heavy capacitive load on the circuit waveform. Note the broadening of the current pulses and the increase in output voltage. Figure 11.2.2(d) shows the effect of a heavy inductive load with an opposite trend. Neither leading nor lagging zero power factor loads have any serious effects on turn-off time or component voltages in this inverter circuit.

Figure 11.2.3 shows the effect of varying the triggering frequency (f_o) on the output voltage waveform while keeping the resonant frequency (f_r) of the LC circuit constant. Lowest distortion is seen to occur at a ratio of $f_r/f_o = 1.35$.

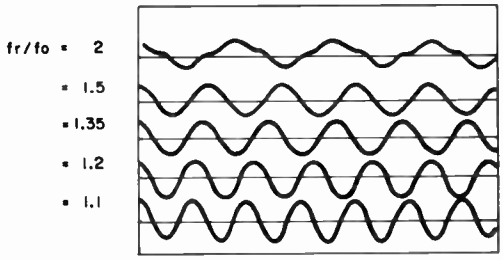


FIGURE 11.2.3 EFFECT OF VARYING RATIO OF RESONANT FREQUENCY OF LC CIRCUIT f_r TO TRIGGERING FREQUENCY f_o ON OUTPUT WAVEFORM OF CLASS A INVERTER (CIRCUIT OF FIGURE 11.2.1).

The features of this inverter are:

1. Good output waveform.
2. Excellent load regulation.
3. Ability to operate into an open circuit.
4. Ability to work into a wide range of reactive loads.
5. Relatively low and constant value of SCR voltage.

Figure 11.2.4 gives the calculated and measured load regulation curves for reactive and resistive loads of the design described in detail in Reference 1.11.

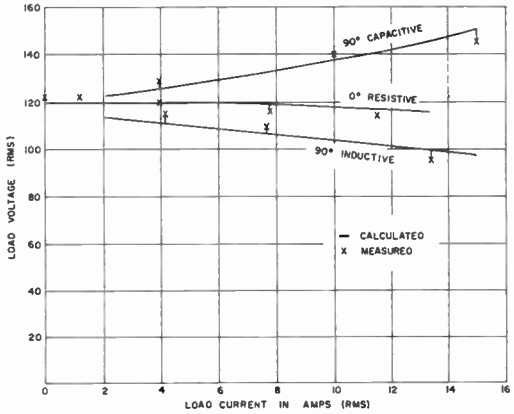


FIGURE 11.2.4 LOAD REGULATION OF CLASS A INVERTER OF FIGURE 11.2.1

A suitable trigger circuit for this type of inverter is shown in Fig. 4.39.

11.2.1.2 Applications

The following are some of the uses for Class A inverters:

- Ultrasonic cleaning, welding and mixing equipment
- Induction heaters
- Radio transmitters in the VLF band
- Sonar transmitters
- Cycloconverter supplies, the output of the cycloconverter itself being useful for all applications where AC power is used
- DC to DC converters where the advantages of light weight, small size, low cost and fast response time due to the high-frequency link are very apparent

11.2.2 Class C Inverters

Typical of the Class C inverter is the well-known "McMurray-Bedford Inverter."[3.2] This inverter circuit is shown in Figure 11.2.5. It operates as follows. Assume SCR_1 conducting and SCR_2 blocking. Current from the DC supply flows through the left side of the transformer primary. Autotransformer action produces a voltage of $2E_b$ at the anode of SCR_2 charging capacitor C to $2E_b$ volts. When SCR_2 is triggered, point (A) rises to approximately $2E_b$ volts, reverse biases SCR_1, and turns it off. Capacitor C maintains the reverse bias for the required turn-off time. When SCR_1 is again triggered, the inverter returns to the first state. It follows that the DC supply current flows alternately through each side of the transformer primary producing a square-wave AC voltage at the secondary.

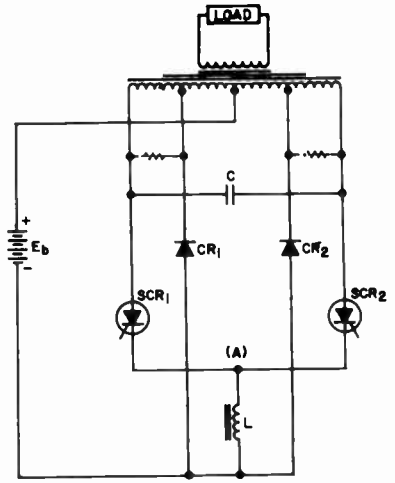


FIGURE 11.2.5 McMURRAY BEDFORD INVERTER

Rectifiers CR_1 and CR_2 feed back, to the DC supply, reactive power associated with capacitive and inductive loads. With inductive loads, energy stored in the load at the end of a half cycle of AC voltage is returned to the supply at the beginning of the next half cycle. Conversely with capacitive

loads, energy stored in the load at the beginning of a half cycle is returned to the supply later in that half cycle.

The feedback rectifiers are connected between the negative supply terminal and taps on the transformer primary. In applications where losses would not be excessive, the diodes may be returned to the SCR anodes through small resistances as indicated by the dashed lines in Figure 11.2.5. In the tap connection some energy trapped in L is fed to the load. Use of the tap connection results in some variation of output with load power factor. but far less than with no feedback rectifiers.

Optimum values for the commutating elements of a "McMurray-Bedford Circuit" are:

$$C = \frac{t_c\, I_{com}}{1.7\, E_b}$$

$$L = \frac{t_c\, E_b}{0.425\, I_{com}}$$

where t_c = minimum turn-off time presented to the SCR

I_{com} = maximum value of load current at commutation

Inverter waveshapes for different load power factors are shown in Figure 11.2.6.

The above relations define C and L such that commutation is insured for maximum lagging load current.

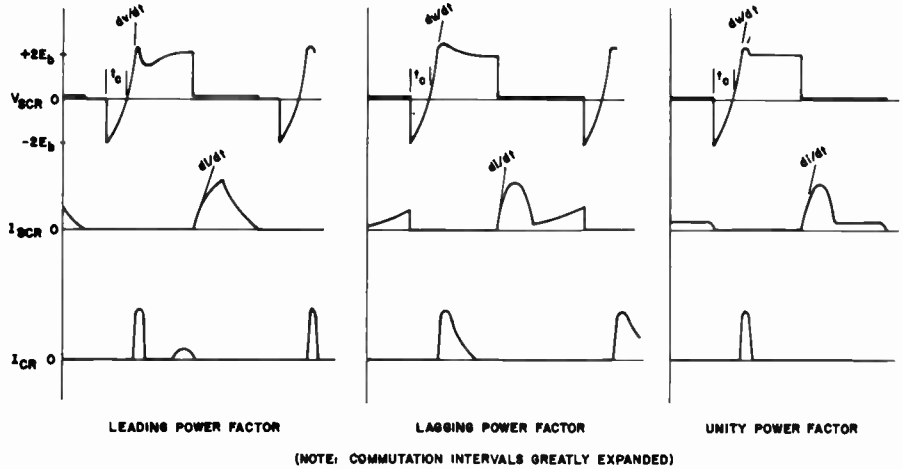


FIGURE 11.2.6 INVERTER WAVESHAPES FOR VARIOUS LOAD POWER FACTORS

A useful accessory which may gainfully be employed with the Class C inverter is the Ott filter (see Section 11.3.3.2). This filter provides a sine wave output with good load regulation while presenting a capacitive load to the inverter over a large range of load power factor. This capacitive load to the inverter aids the SCR commutation situation. The filter circuit is shown in

Figure 11.3.5(a). Figure 11.3.5(b) relates load impedance to filter input impedance. The radial lines emanating from the origin represent loci of constant load phase angle, the circles with centers at the origin are loci of constant load impedance magnitude. The other two sets of loci represent filter input impedance (magnitude and phase angle). All impedance magnitudes are normalized to the filter design impedance. Note that for the input impedance to be capacitive for any load power factor, the normalized, rated, load impedance must be two or greater.

11.2.2.1 Design Procedure

The following is the design procedure for a Class C square wave inverter used in connection with the Ott filter to produce sinusoidal voltage.

Required Specifications

Output voltage (E_o)—Volts (RMS)
Output power (P_o)—watts
Output frequency (f)—Hz
Rated load power factor (pf)
Available DC supply (E_b)—volts

FILTER DESIGN

Load Resistance

$$R_L = \frac{E_o^2 \times pf^2}{P_o} \text{ (ohms)}$$

Load Reactance

$$X_L = \frac{R_L}{pf} \quad 1 - pf^2 \text{ (ohms)}$$

Load Impedance

$$|Z_L| = \sqrt{R_L^2 + X_L^2} \text{ (ohms)}$$
$$\angle Z_L = \cos^{-1} pf \text{ (degrees)}$$

Filter Design Impedance

$$Z_D \leqq \frac{|Z_L|}{3} \text{ (ohms)}$$

Design Radian Frequency

$$\omega_D = 2\,\pi\,f \text{ (radians/sec)}$$

Filter Element Values

$$C_1 = \frac{1}{6\,Z_D\,\omega_D} \qquad C_2 = \frac{1}{3\,Z_D\,\omega_D} \text{ (farads)}$$

$$L_1 = \frac{9\,Z_D}{2\,\omega_D} \qquad L_2 = \frac{Z_D}{\omega_D} \text{ (henrys)}$$

Filter Input Impedance

Z_{IN}, R_{IN} and X_{IN} are determined from Figure 11.3.5(b)

Input Voltage to Filter

$$E_{(SQ)} = \frac{\sqrt{2}}{4}\,\pi \left|Z_{IN}\right| \quad \frac{P_o}{R_{IN}} \text{ (volts)}$$

INVERTER DESIGN

Transformer Turns Ratio

$$n = \frac{E_{(SQ)}}{E_b}$$

Input Power, assuming 85% efficiency

$$P_I = P_o \times \frac{100}{85} \text{ (watts)}$$

Average Current in SCR

$$I_{AV(SCR)} \cong \frac{P_o |Z_{IN}|}{2 E_b R_{IN}}$$

Peak Forward Voltage Across SCR's

$$V_{PK(SCR)} < 2.5 E_b$$

From the expressions for $I_{AV(SCR)}$ and $V_{PK(SCR)}$ a preliminary choice of SCR may be made.

Peak Current in SCR's

$$I_{PK(SCR)} = 4E_b \quad \frac{C}{L}$$

Turn-Off Time

$$t_c = \frac{2\pi}{3} \sqrt{LC}$$

Rate of Reapplication of Forward Blocking Voltage

$$dv/dt = \frac{0.85 E_b}{\sqrt{LC}}$$

Turn-on di/dt

$$di/dt \Big|_{t=0} = \frac{2 E_b}{L}$$

From the preceding four relationships, L and C may be determined as follows

$$L = \frac{6E_b t_c}{\pi I_{PK(SCR)}}$$

Choose the desired t_c and $I_{PK(SCR)}$ and determine L. Check dv/dt with the following

$$dv/dt = \frac{3.44 E_b^2}{L I_{PK(SCR)}}$$

If dv/dt is too high, increase L accordingly and recalculate $I_{PK(SCR)}$. Now:

$$C = \frac{3 t_c I_{PK(SCR)}}{8\pi E_b}$$

The minimum value of L should be such as to keep the turn-on di/dt well below specification.

11.2.2.2 A 400 Hz Inverter With Sine Wave Output

The design procedure for a 400 Hz inverter with sine wave output is given to illustrate the application of a Class C inverter used in conjunction with the Ott filter.

Required Specifications

Output power = 360 watts
Output voltage = 120 volts (RMS)
Output frequency = 400 Hz
Rated load power factor = 0.7 lagging
Available DC supply = 28 VDC

FILTER DESIGN

Load Resistance

$$R_L = \frac{(120)^2 \times (.7)^2}{360} = 20 \text{ ohms}$$

Load Reactance

$$X_L = \frac{20}{.7}\sqrt{1 - (.7)^2} = 20 \text{ ohms}$$

Load Impedance

$$|Z_L| = \sqrt{(20)^2 + (20)^2} = 28.3 \text{ ohms}$$

$$\angle Z_L = \cos^{-1}(.7) = \frac{\pi}{4}$$

Filter Design Impedance

$$Z_D \leqq \frac{28.3}{2}$$

Choose $Z_D = 15$ ohms

Design Radian Frequency

$$\omega_D = (2)(3.14)(400) = 2500 \text{ radians/sec}$$

Filter Element Values

$$C_1 = \frac{1}{(6)(15)(2500)} = 4.5 \times 10^{-6} \text{ farads}$$

$$C_2 = \frac{1}{(3)(15)(2500)} = 9 \times 10^{-6} \text{ farads}$$

$$L_1 = \frac{(9)(15)}{2(2500)} = 27 \times 10^{-3} \text{ henrys}$$

$$L_2 = \frac{15}{2500} = 6 \times 10^{-3} \text{ henrys}$$

Filter Input Impedance

From Figure 11.3.5(b) (point marked X)

$$Z_{IN} = (15)\, 5.5 \angle -16^\circ$$
$$= 80 - j\,23$$
$$R_{IN} = 80 \text{ ohms}$$
$$X_{IN} = 23 \text{ ohms}$$
$$|Z_{IN}| = 83 \text{ ohms}$$

Input Voltage to Filter

$$E_{SQ} = \frac{\sqrt{2}}{4}(3.14)(83) \quad \frac{360}{80} = 195 \text{ volts}$$

INVERTER DESIGN

Transformer turns ratio

$$n = \frac{195}{28} = 7$$

Input Power (assuming 85% efficiency)

$$P_I = 360 \times \frac{100}{85} = 424 \text{ watts}$$

Average Current in SCR's

$$I_{AV(SCR)} \cong \frac{(360)\,(83)}{(2)\,(28)\,(80)} = 6.8 \text{ amps}$$

Peak Forward Voltage Across SCR's

$$V_{PK(SCR)} = (2.5)\,(28) = 70 \text{ volts}$$

From the above a G-E type C141A is chosen.

Commutating Elements

The C141A has a maximum turn-off time of 10μ sec and maximum dv/dt of 200 volts/μsec. Choose $t_c = 12$ μsec and $I_{PK(SCR)} = 14$ amps.

$$L = \frac{6\,(28)\,(12)}{(14)\,(3.14)} = 45 \times 10^{-6} \text{ henrys}$$

Checking dv/dt,

$$dv/dt = \frac{(3.44)\,(790)}{(45 \times 10^{-6})\,(14)} = 4.3 \text{ volts}/\mu\text{sec}$$

$$C = \frac{(3)\,(12 \times 10^{-6})\,(14)}{(8)\,(3.14)\,(28)} = .75 \times 10^{-6} \text{ farads}$$

Turn-On di/dt

$$di/dt\Big|_{t=0} = \frac{2 \times 28}{45} = 1.25 \text{ A}/\mu\text{sec}$$

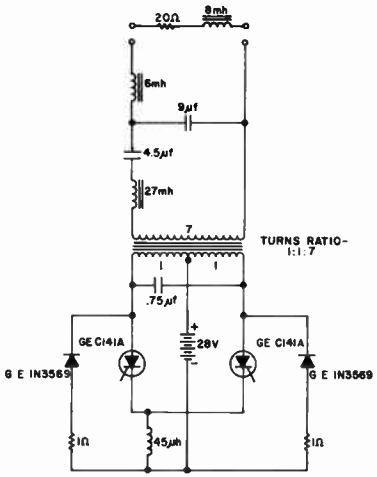


FIGURE 11.2.7 A 400 Hz INVERTER WITH THE OTT FILTER

NOTES:

1. Feedback rectifiers are chosen to have current and voltage capability similar to the SCR's.
2. One ohm series resistors are used to limit power dissipation in the feedback rectifiers.
3. The composite inverter-filter circuit for the 400 Hz inverter is shown in Figure 11.2.7.
4. A suitable trigger circuit for the Class C inverter is shown in Fig. 4.40.

11.2.3 Designing a Battery Vehicle Motor-Controller Using The Jones SCR Chopper (Class D)

11.2.3.1 Introduction

Three methods are available for controlling the voltage to, and hence the speed of, a battery-driven DC series motor of any appreciable power:

1. A rheostat may be inserted in series with the motor. This method has a smooth action but power is wasted in the rheostat.

2. The battery or the field winding may be switched in series or parallel. This method is virtually lossless but the action is jerky.

3. The third method involves the use of a rapid-acting switch, called a chopper, in series with the motor.

The action of the chopper is shown in Figure 11.2.8.

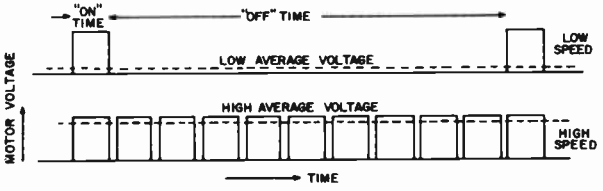


FIGURE 11.2.8 CHOPPER WAVEFORMS

At low speeds the "on" time is much less than the "off" time. The result is that the average voltage across the motor is low. As the "off" time is decreased so the average voltage increases. The change in the average voltage is as smooth as the "off" time may be readily adjusted by a potentiometer controlled timer. This method combines the advantages of the two previous methods in that both smooth control and high efficiency are achieved simultaneously. The SCR makes an ideal switch for this chopper application.

Figure 11.2.9 shows a diagram complete except for the method of turning the SCR on and off. This will be discussed later.

S_2, S_3, S_4 and S_5 are field-reversing relays. With S_2 and S_5 closed the direction is forward, whereas with S_3 and S_4 closed the direction is reverse.

This SCR chopper has a practical duty cycle ranging from about 20% to about 80%.

For the standstill state all four switches, S_2, S_3, S_4 and S_5, are open. When S_2 and S_5 are closed, and with the chopper operating at low speed,

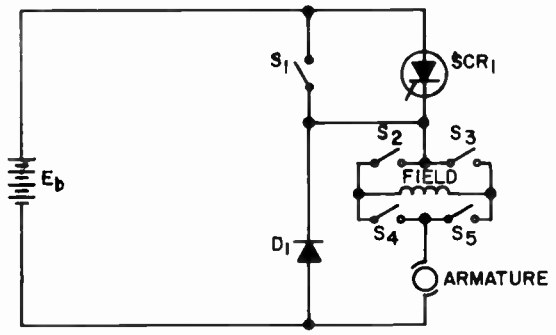


FIGURE 11.2.9 BASIC VEHICLE CONNECTIONS

about 20% of the supply voltage is applied to the motor. This voltage may be increased to 80% of the battery voltage as more torque is required. When 80% is reached relay S_1 is closed applying full voltage to the motor and maximum torque is obtained.

The diode D_1 is the well known free-wheeling diode. Its purpose is to carry the inductive current when the SCR is turned off, thus preventing high voltages appearing across the motor.

The controller to be described uses a variable-frequency constant-pulse-width system. A variation is for the frequency to be held constant and the pulse width changed.

11.2.3.2 The Jones Commutation Circuit

Figure 11.2.10 shows the basic circuit.

SCR_1 is the load-current-carrying SCR. When the gate is triggered, current flows from the battery via winding L_1 of the autotransformer T_1 to the motor represented by an inductor L_m and a resistor R_m.

The start of the current flow induces a voltage into winding L_2 which charges up the capacitor C. This charge is held until "off" SCR_2 is triggered. The voltage across SCR_1 is then reversed and it is turned off.

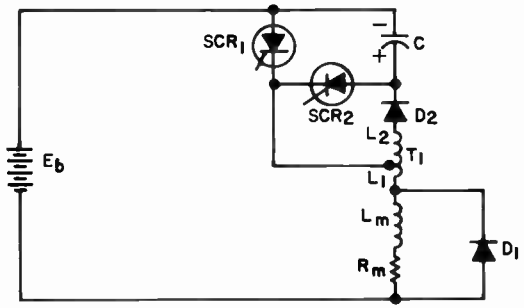


FIGURE 11.2.10 THE JONES CHOPPER

One of the advantages of the Jones circuit over others is its ability to start reliably. Due to the autotransformer the capacitor is always charged up whenever load-current starts to flow and thus commutation energy is always available.

The turn-off time t_c that the circuit presents to the SCR is shortest during the first pulse of operation as the capacitor C must be assumed to be completely discharged. It is therefore important that calculations and measurements of turn-off are made with the capacitor starting at zero voltage.

Typical circuit waveforms are shown in Figure 11.2.11.

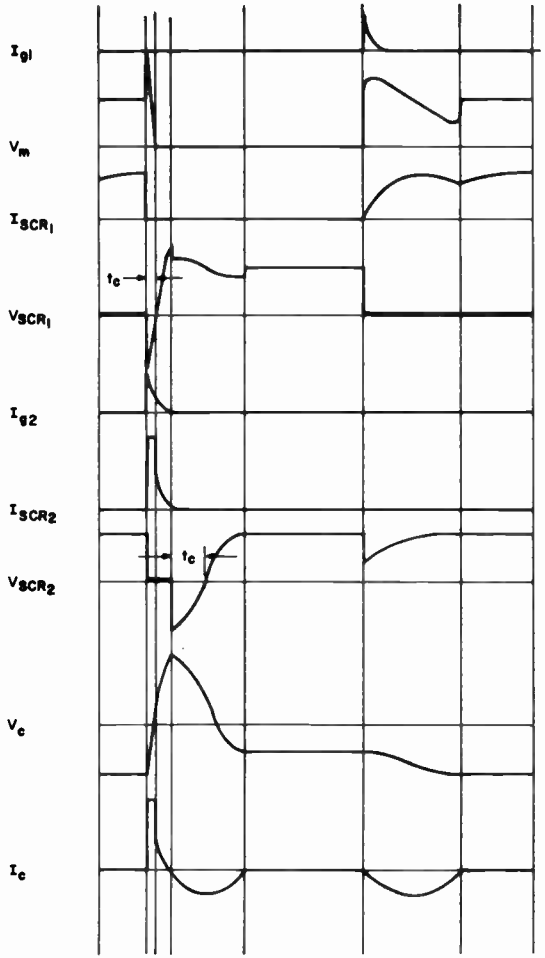


FIGURE 11.2.11 WAVEFORMS IN THE JONES CHOPPER

11.2.3.3 Design Notes

The following equations are given as a rough guide to the design engineer to enable him to construct a working circuit. The calculations must be checked in a breadboard model before components are specified. See 11.2.3.6 if plugging is to be used.

The following information is required: The battery voltage E_b; the locked rotor current of the motor, I_m.

Selection of SCR_1

When a bypass switch is used, such as S_1 in Figure 11.2.9, the following rule-of-thumb holds in practice. The RMS rating of $SCR_1 \geqq I_m$. This assumes an adequate heatsink for SCR_1.

Capacitor C

$$C = \frac{t_{off} \times I_m}{E_b} \mu F$$

where t_{off} is the turn-off time of the SCR. Use a safety factor of 20% for vehicles.

L_2 and Pulse Repetition Rate for 80% Voltage

The minimum pulse width that can be used must be greater than the charging time of C which is determined by L_2 and C.

Minimum pulse width $> \pi \sqrt{L_2 C}$ where L_2 is the unsaturated inductance. A reasonable pulse width to use is $2\pi\sqrt{L_2 C}$.

For 80% voltage the period is $\frac{100}{80} \times 2\pi\sqrt{L_2 C}$

Thus, maximum pulse repetition rate

$$f = \frac{0.8}{2\pi\sqrt{L_2 C}}$$

In practice this frequency extends from 100 Hz to about 400 Hz. If the frequency is too low, the motor thumps at slow speeds. If too high, the motor heats up excessively.

Also

$$L_2 = \frac{16 \times 10^9}{f^2 C} \mu H$$

(where C is in μF and f in Hz)

Transformer T_1

A turns ratio of about 7:1 is used to achieve the desired turn-off time during the first pulse.

Thus

$$\frac{\text{Primary Turns}}{\text{Secondary Turns}} = \frac{N_1}{N_2} = \frac{1}{7} = \sqrt{\frac{L_1}{L_2}}$$

thus

$$L_1 = \frac{L_2}{49}$$ (L_1 is the unsaturated inductance.)

If the transformer core has an air gap made up of the ends of the laminations butting together with no spacer, the number of turns may be found from the following approximate relation.

$$N_2^2\,A = \frac{L_2}{6}$$

The core is assumed to be of the stacked type where A is the core cross sectional area in square inches and L_2 is in μH.

The choice of number of turns and core size must be checked regarding the maximum flux density in the core.

$$\text{Flux density} = \frac{15\,E_b\sqrt{L_2\,C}}{N_1\,A}$$

This flux density may be run just below saturation.

Free-Wheeling Diode D_1

A rule-of-thumb for the maximum average current in D_1 is a quarter of the motor locked-rotor current I_m. (Assume 180° conduction angle.)

Average Current in SCR_2, D_2, C and L_2

The same average current flows in all four components.

$$I_{avg} = f\,(CE_b + 2\,I_m\sqrt{L_1\,C}) \times 10^{-6} \text{ amps average}$$

RMS Current in L_1

A rule-of-thumb for the RMS current in winding L_1: half the motor locked-rotor current I_m.

Voltage Rating of SCR_1, SCR_2, D_1, and C

The peak forward and reverse blocking voltage across SCR_1 and SCR_2, the peak reverse voltage across D_1, and the peak voltage across C are found from the expression

$$V_{PK(SCR_1)} \leq E_b + I_m\sqrt{\frac{L_1}{C}} \text{ volts peak}$$

Voltage Rating of D_2

$$V_{PK(D2)} = \frac{N_2}{N_1}\,V_{PK(SCR_1)}$$

SCR Dynamic Characteristics

SCR_1:

$$dv/dt = \frac{I_m}{C} \text{ volts per } \mu s$$

$$\text{Initial } di/dt = \frac{E_b}{L_1} \text{ amps per } \mu s$$

$$\text{Circuit Turn-off time } t_c = \frac{E_b C}{I_m}\ \mu s$$

SCR_2:

$$dv/dt = \frac{V_{PK(SCR)_1}}{\sqrt{L_2\,C}} \text{ volts per } \mu s$$

$$\text{Initial } di/dt = \frac{V_{PK(SCR)_1}}{\text{Stray Inductance in Loop Formed by } SCR_1,\ SCR_2 \text{ and C}}$$

$$\text{Circuit Turn-off time } t_c = (\pi/2)\sqrt{L_2\,C}\ \mu s$$

11.2.3.4 Worked Example

Given: $E_b = 36$ volts

$I_m = 110$ amps

Selection of SCR_1:

The G-E C154 has an RMS rating of 110 amps.

The turn-off time t_{off} is 10 μs at 50 amps.

Capacitor C

$$C = \frac{12 \times 110}{36} = 37\ \mu f \quad \text{Use a 50 } \mu f \pm 10\% \text{ capacitor}$$

L_2 and Pulse Repetition Rate for 80% Voltage

Choose 300 pulses per second.

$$L_2 = \frac{16 \times 10^9}{300^2 \times 50} = 3600\ \mu H$$

Transformer T_1

$$L_1 = \frac{3600}{49} = 73\ \mu H$$

$$N_2{}^2 A = \frac{3600}{6} = 600$$

If a core of .75 sq inch cross sectional area is used

$$N_2 = \sqrt{\frac{600}{.75}} = 28 \text{ turns}$$

$$N_1 = 4 \text{ turns}$$

$$\text{Flux Density} = \frac{15 \times 36 \times \sqrt{3600 \times 50}}{4 \times .75}$$

$$= 76{,}000 \text{ lines per square inch}$$

With this flux density most of the silicon steel materials will do for the core.

Free-Wheeling Diode D_1

$$\frac{I_m}{4} = \frac{110}{4} = 27.5 \text{ amps}$$

Average Current in SCR_2, D_2, C and L_2

$$I_{AV(SCR_1)} = 300\,(50 \times 36 + 110 \times 2\sqrt{73 \times 50}) \times 10^{-6}$$

$$= 4.6 \text{ amps average}$$

RMS Current in L_1

$$\frac{I_m}{2} = 55 \text{ amps RMS}$$

Voltage Rating of SCR_1, SCR_2, D_1, and C

$$V_{PK(SCR_1)} \leq 36 + 110\sqrt{\frac{73}{50}}$$

$$= 170 \text{ volts}$$

Voltage Rating of D_2

$$V_{PK(D2)} \leq 7 \times 170$$

$$\approx 1200 \text{ volts (in Figure 11.3.12 this voltage is clipped by means of a thyrector)}$$

SCR Dynamic Characteristics

SCR_1

$$dv/dt = \frac{110}{50} = 2 \text{ volts per } \mu s$$

$$\text{Initial } di/dt = \frac{36}{73} = 0.5 \text{ amps per } \mu s$$

$$t_c = \frac{36 \times 50}{110} = 16 \ \mu s$$

SCR_2

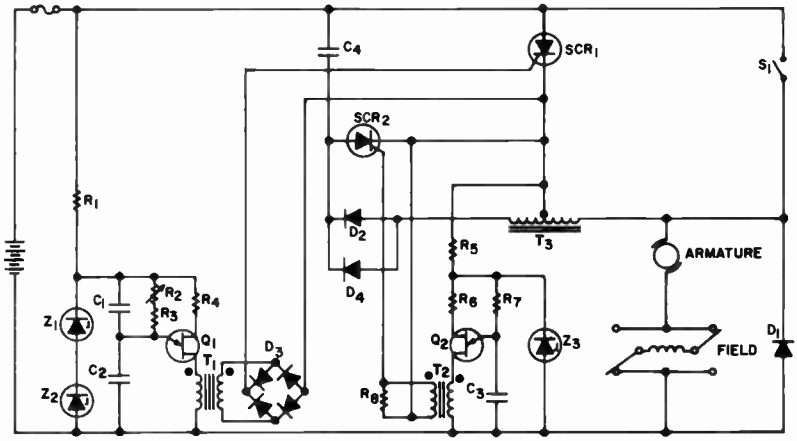
$$dv/dt = \frac{170}{\sqrt{3600 \times 50}} = 0.4 \text{ volts per } \mu s$$

$$\text{Initial } di/dt = \frac{170}{\text{Estimated } 2 \ \mu H}$$

$$= 85 \text{ amps per } \mu s$$

$$t_c = (\pi/2)\sqrt{3600 \times 50} = 560 \ \mu s$$

The chosen components are listed in the complete schematic in Figure 11.2.12.



C_1 — 0.1 μf, 100V
C_2 — 0.1 μf, 100V
C_3 — 0.22 μf, 100V
C_4 — 50 μf, 115 VAC GE 28F1102
D_1 — G E IN2155
D_2 — G E IN3673A
D_3 — THYRECTOR GE 6RS2IVA20D
Q_1 — G E 2N2646
Q_2 — G E 2N2647

R_1 — 220Ω, 2W
R_2 — 0 TO 100K POTENTIOMETER (TAPER Z)
R_3 — 20K, 1/2W
R_4 — 330Ω, 1/2W
R_5 — 270Ω, 2W
R_6 — 330Ω, 1/2W
R_7 — 15K, 1/2W
R_8 — 100Ω, 1/2W

SCR_1 — G E C154B
SCR_2 — G E C140B
T_1, T_2 } PULSE ENGINEERING TYPE PE2229
T_3 — G E 9T48Y7008
Z_1 — G E IN1771
Z_2 — G E IN1771
Z_3 — G E IN1773

FIGURE 11.2.12 BATTERY VEHICLE CONTROLLER USING THE JONES CHOPPER

11.2.3.5 Testing Procedure

The circuit should first be tested with a resistor of 1 ohm in place of the motor. The frequency range and pulse width should be checked. The turn-off time should be measured and should be from 50 to 70 μs.

The 1-ohm resistor should be removed and the motor connected. After the operation has been confirmed, the turn-off time of SCR_1 should be measured with the heaviest load using a fully charged battery. The turn-off time (t_c) must be greater than 10 μs in the worked example.

11.2.3.6 A Note on Motor Plugging

Plugging means throwing the motor in reverse while it is coasting forward. The result is that the motor acts as a generator with the polarity reversed. High values of current flow in the free-wheeling diode and the load resistance seen by SCR_1 is extremely small.

In these circumstances the value of C or alternately the product $L_1 \times L_2$ must be increased in order to increase the circuit turn-off time.

11.3 INVERTER ACCESSORIES

In practical applications of inverters it is often necessary to modify the design to accommodate one or more of the following requirements:

1. The ability to operate into inductive loads
2. Over-current protection
3. Open-circuit operation
4. Sine wave output
5. Regulated output

11.3.1 The Ability to Operate Into Inductive Loads

When an inverter sees a reactive load as opposed to a purely resistive load several changes occur in the operation of the inverter. Without attention, a reactive load can cause high voltage transients to exist in the inverter resulting in loss of efficiency and power and jeopardizing the components.

Consider Figure 11.3.1. Assume that SCR_1 is conducting. Current is flowing in the primary of the transformer as shown by arrow "a" and in the load by "b". When SCR_1 is turned off, current "b" still needs to flow. If no path were provided in the primary, the voltage would rise excessively.

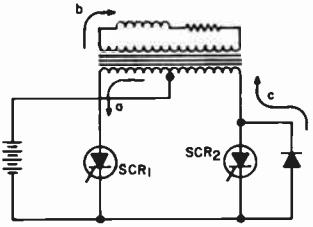


FIGURE 11.3.1 FLOW OF REACTIVE CURRENT

A convenient means of providing a current path is to place a diode across SCR_2. Now current "c" can flow and this is magnetically the same path as current "a". The dv/dt that the circuit applies to the SCR is greatly increased. Figure 11.3.2 shows the effect of a diode across the SCR on the voltage waveform. In Figure 11.3.2(b) it is seen that the voltage across the SCR is held at a low negative value while current is flowing through the diode. When the diode ceases to carry current, the voltage across the SCR suddenly snaps up to a high value. As the rise time is commonly less than 1 μs, the value of dv/dt can be very high. Where possible, it is preferable to avoid placing the diode directly across the SCR. The circuit of Figure 11.2.5 for example shows how an inductor can be used between the SCR and the diode. By this means both the high values of dv/dt and the low amount of reverse voltage can be avoided.

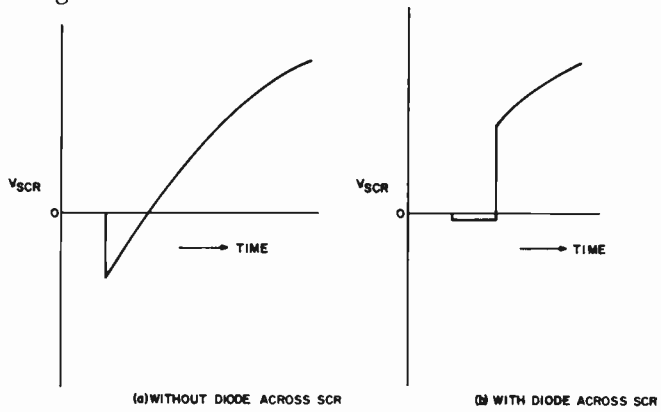


FIGURE 11.3.2 VOLTAGE WAVEFORM ACROSS THE SCR

11.3.2 Overcurrent Protection

If the load current in an inverter is increased beyond the rated output, some means must be provided for the protection of the components. The following methods may be considered.

11.3.2.1 Fuses and Circuit Breakers in the DC Supply

This, the most obvious of steps, has the advantage of simplicity. It is however necessary to match the overload capabilities of the SCR with the current-time rating of the fuses or circuit breakers. Thus the I^2t rating of the SCR must be greater than that of the fuse. This is complicated by the fact that the I^2t rating of the SCR drops substantially during the SCR turn-on time, and fuses or circuit breakers do not afford very good protection in this short time.

Another snag is the location of the fuse in the DC supply. Invariably a ripple current due to the load current flows in the DC supply. Thus the fuse will see a relatively high RMS current and may, in the case of high frequency inverters, have to be derated because of skin effect. If on the other hand a large filter capacitor is placed between the fuse and the inverter to carry the ripple current then the fuse does not isolate the SCR from the energy in the capacitor.

11.3.2.2 Current Limiting by Pulse-Width Control

The inverter components may be protected by sensing the output current and using this information to narrow down the pulse width when the output current exceeds the rated value. With a very heavy load the current pulses then become narrow and have a high amplitude. The circuit is then liable to present short values of turn-off time and high values of di/dt to the SCR. If the load is distributed to more than one piece of apparatus, there may not be enough current in the case of a current limited supply to blow the local fuse where a short circuit occurs.

11.3.2.3 Current Limiting by LC Resonance

The bridge circuit in the output lead of the inverter in Figure 11.3.3 is in series resonance at the output frequency. If the Q of the capacitors and inductors is high, the overall efficiency of the inverter will not be appreciably changed.

In the event of a current overload a fast acting switch is connected between points A and B. The bridge circuit then becomes a parallel resonant circuit at the operating frequency and the impedance to the load current becomes very high.

The fast-acting switch may be either a saturating reactor or one of the forms of SCR AC switches described in Chapter 8.

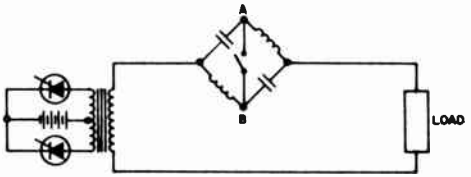


FIGURE 11.3.3 CURRENT LIMITING BY L. C. RESONANCE

11.3.2.4 Current Limiting in Class A Circuits by Means of Series Capacitors

Class A circuits such as Figure 11.2.1 can be made current limiting by connecting a capacitor C_1 in series with the load R. See Figure 11.3.4. The value of capacitor is chosen so that, when the load is shorted, the resonant frequency of the LC circuit is still appreciably greater than the triggering frequency. Figure 11.3.5 shows a typical curve of load current versus load voltage.

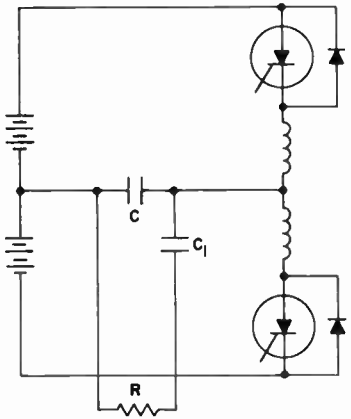


FIGURE 11.3.4 CURRENT LIMITING IN A CLASS A INVERTER CIRCUIT

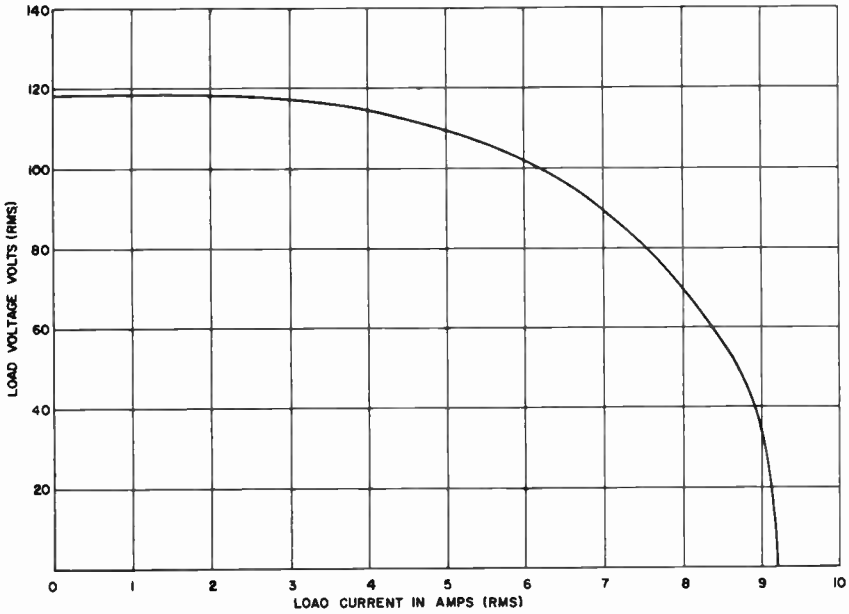


FIGURE 11.3.5 LOAD REGULATION CURVE OF A CURRENT LIMITING CLASS A INVERTER.

11.3.3 Sine-Wave Output[7]

Most applications of DC to AC inverters prefer a sine-wave rather than a square wave output. In conflict with this we are faced with the fact that the SCR is essentially a switch and switching a battery gives square waves. In fact the great efficiency with which SCR inverters operate is mainly due to the fact that the SCR switches at high speed from the fully-off to the fully-on mode.

Sine-wave output-waveforms may be obtained from SCR inverters by the following approaches:

1. Resonating the load
2. Harmonic attenuation by means of an LC filter
3. An LC filter plus optimum pulse-width selection
4. Synthesis by means of output voltage switching
5. Synthesis by control of the relative phase of multiple inverters
6. Multiple pulse width control
7. Selected harmonic reduction
8. Cycloinversion

11.3.3.1 Resonating the Load[1]

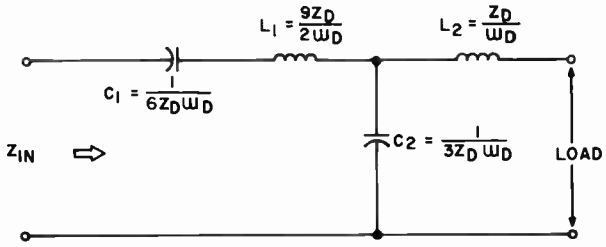
The waveform in the load may be made sinusoidal by inserting the load in a resonant circuit of a Q high enough to achieve the desired harmonic content. A typical circuit using this approach is found in Class A inverters. Owing to the large size of the LC components this circuit only becomes attractive above about 400 Hz.

11.3.3.2 Harmonic Attenuation by Means of an LC Filter[7.1, 7.4]

This filter can take many forms. The most attractive is that by Ott described in Reference 7.4. The circuit is shown in Figure 11.3.5. The Ott filter has the following very desirable characteristics:

1. Good voltage transfer characteristics.
2. Attenuation independent of the load.
3. The input impedance can be designed to be capacitive over the working load range.

For details see the Class C inverter example in Section 11.2.2.



Z_D —— FILTER DESIGN IMPEDANCE
ω —— FILTER DESIGN FREQUENCY

(a)

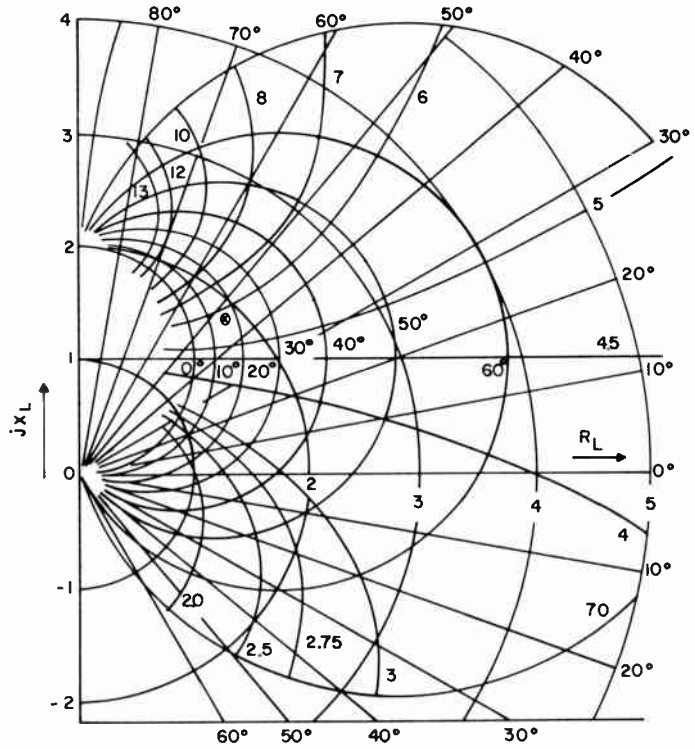


FIGURE 11.3.5 INPUT IMPEDANCE CHART

11.3.3.3 An LC Filter Plus Optimum Pulse Width Selection [7.2]

The requirements of the LC filter can be appreciably reduced by using a narrower pulse width than 180°. Thus a 120° pulse has zero third harmonic distortion. See Figure 11.3.6.

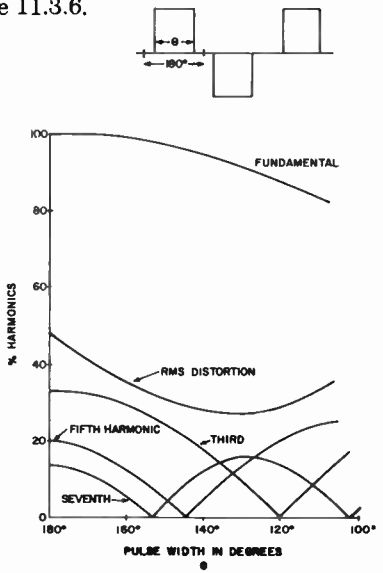


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FIGURE 11.3.6 HARMONIC CONTENT VERSUS PULSE WIDTH WITH RECTANGULAR WAVEFORMS.

11.3.3.4 Synthesis by Means of Output-Voltage Switching [7.1 and 7.6]

The output from an inverter is coupled through a transformer (Figure 11.3.7) to the load via SCR "tap switches". The appropriate SCR is triggered to give the output waveform shown in Figure 11.3.8. The inverter operates, in this case, at five times the output frequency. This waveform is easily filtered to give a good sine wave output.

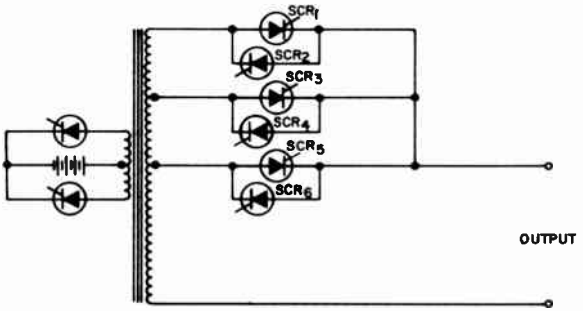

FIGURE 11.3.7 OUTPUT VOLTAGE SWITCHING CIRCUIT

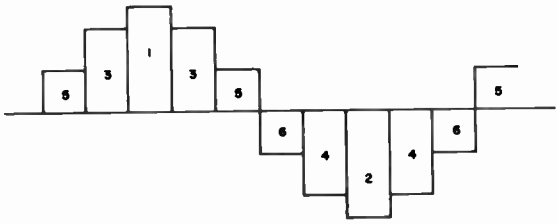

FIGURE 11.3.8 WAVEFORM WITH OUTPUT VOLTAGE SWITCHING

11.3.3.5 Synthesis by Controlling the Phase Relationship of Multiple Inverters [7.1 and 7.5]

The basis of this method of harmonic reduction is to add the outputs of a multiplicity of inverters to form a quasi sine wave which has no low-order harmonic component. The remaining high-order harmonics are easily filtered.

Figure 11.3.9 shows an outline of a three phase bridge inverter circuit. The voltages across outputs a, b and c are shown in Figure 11.3.10 and the line-to-line voltage across the output transformer is shown in Figure 11.3.11. If more phases are used the steps in the waveform become smaller giving an even lower harmonic content.

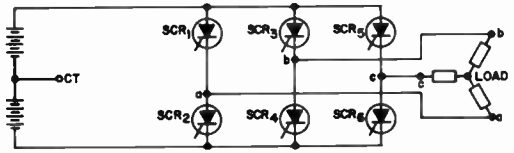

FIGURE 11.3.9 THREE PHASE BRIOGE INVERTER CIRCUIT

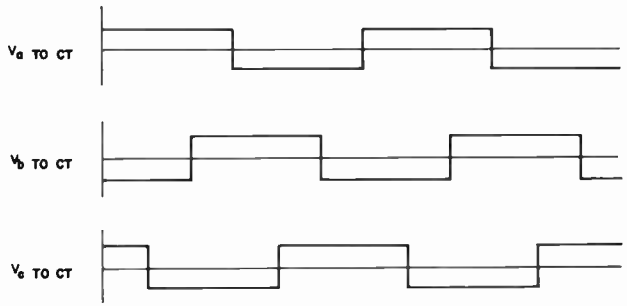

FIGURE 11.3.10 PHASE RELATIONSHIPS IN THREE PHASE INVERTER

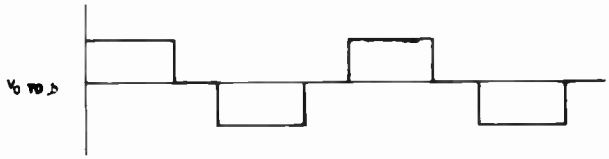

FIGURE 11.3.11 OUTPUT WAVEFORM OF THREE PHASE INVERTER

11.3.3.6 Multiple Pulse Width Control [7.1]

This method of achieving a sine wave output is obvious from Figure 11.3.12. This waveform may be obtained from a bridge circuit (Figure 11.1.4). One pair of SCR's is triggered and turned off with various pulse widths to form the positive half cycle and then the other pair is operated similarly for the negative half cycle.

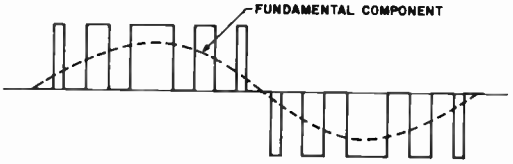

FIGURE 11.3.12 OUTPUT WAVEFORM USING MULTIPLE PULSE WIDTH CONTROL

11.3.3.7 Selected Harmonic Reduction [7.3]

The circuit in Figure 11.1(4) is triggered so as to give a load waveform as shown in Figure 11.3.13. With precise control of the pulse widths the output wave-shape can be made low in 3rd and 5th harmonic content.

The advantages of this method over other methods of synthesis are:

1. The fundamental output may be varied from zero to maximum amplitude without re-introducing the harmonic voltages.
2. A three-phase circuit using only twelve SCR's can eliminate all the harmonics below the eleventh while still being able to control the fundamental frequency from zero to maximum.
3. The triggering circuitry is considerably simplified.

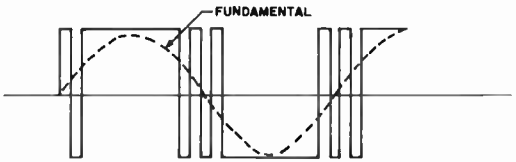

FIGURE 11.3.13 OUTPUT WAVEFORM WITH SELECTED HARMONIC REDUCTION

11.3.3.8 The Cycloinverter

A cycloinverter consists of an inverter, operating at about ten times the desired output frequency, to which is coupled a cycloconverter (see Section 11.4.3) producing the desired output frequency waveform and amplitude.

11.3.4 Regulated Output [8.1]

Most inverter customers specify that the inverter output be regulated both for input voltage and load current variations.

The inverter designer has three choices:

1. To regulate the supply voltage to the inverter
2. To regulate within the inverter
3. To regulate the output of the inverter

11.3.4.1 Supply-Voltage Regulation

If the supply is a battery, fuel cells or some other DC supply, then the pre-regulation takes the form of a regulated DC to DC converter, the logic for the DC to DC converter coming from the output of the inverter, Figure 11.3.14.

The DC to DC regulated supply can take many forms. These are discussed in Chapter 12 and in Reference 8. If the inverter supply is from a rectified AC line, then pre-regulation can be achieved by substituting phase controlled SCR's for the rectifier diodes. The logic for the triggering circuits is again supplied from the output of the inverter, Figure 11.3.15. Phase controlled rectifiers are discussed in Chapter 9.

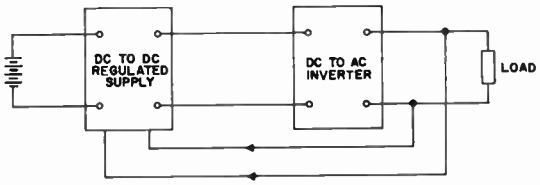

FIGURE 11.3.14 DC SUPPLY VOLTAGE REGULATION

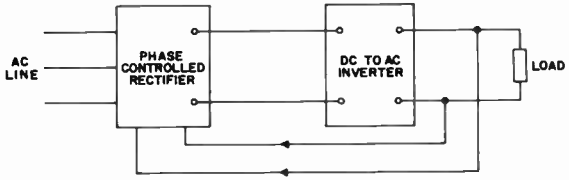

FIGURE 11.3.15 AC SUPPLY VOLTAGE REGULATION

11.3.4.2 Regulation Within the Inverter

By using Class D or Class E inverters pulse-width control is readily achieved. In addition some of the methods of obtaining sine wave output may readily be adapted for output-voltage regulation, the following being the pertinent Sections:

11.3.4.6. Control of the relative phase of multiple inverters
11.3.4.7. Multiple pulse-width control
11.3.4.8. Selected harmonic reduction
11.3.4.9. Cycloinversion

11.3.4.3 Regulation After the Inverter

All the methods commonly used in 60 and 400 Hz. supplies are applicable to the regulation of the AC output of the inverter. These methods include the use of ferroresonant transformers, buck-boost switching of transformers, phase control of SCR's (Chapter 9), and saturating reactors. References 8.2 and 8.3 describe an excellent means whereby the weight of the saturating reactor may be greatly reduced by means of an SCR "amplifier".

11.4 MISCELLANEOUS INVERTER-TYPE CIRCUITS

11.4.1 Sequential Inverters [10]

This is a type of inverter that uses a multiplicity of SCR's in conventional circuits. The SCR's are triggered sequentially giving relatively long rest periods between anode-current pulses during which the junctions can cool down, the turn-off time can be long, and a long period is available to reapply forward blocking voltage. The advantage of this system is that SCR's with fairly poor dynamic characteristics may be used in audio frequency inverters or alternatively, high speed SCR's may be used as VLF and LF power generators.

Figure 11.4.1 shows a circuit[10.1] consisting of five sine-wave inverters (Class A). The gates are triggered sequentially 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 1, 2, etc. The outputs from the five transformers are paralleled and connected to the load. The anode current through any one SCR is shown in Figure 11.4.2 and the voltage across the SCR is shown in Figure 11.4.3. Note the presence in the voltage waveform of the output voltage from pulses in other SCR's. One of the requirements of this circuit is that the resonant circuit Q be high enough so that the voltage to which each capacitor is charged is greater than the peak voltage across the transformer primary

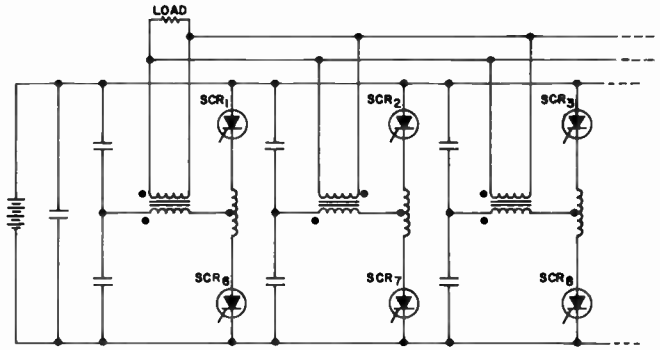

FIGURE 11.4.1 SEQUENTIAL INVERTER CIRCUIT

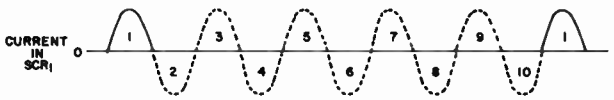

FIGURE 11.4.2 CURRENT WAVEFORM IN SCR_1

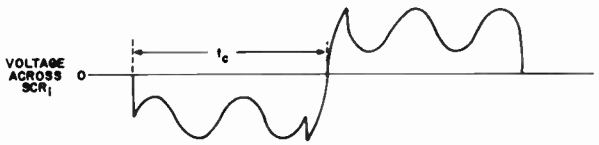

FIGURE 11.4.3 VOLTAGE WAVEFORM ACROSS SCR_1

11.4.2 Pulse Modulator Switches [9]

The conventional pulse modulator circuit using SCR's as switches operates as a Class A inverter. See Figure 11.4.4.

The current pulses through the SCR are narrow, ranging typically from .1 μs to 10μs base width. The repetition rate is from several hundred to several thousand cycles per second.

Turn-off time and dv/dt are usually not critical characteristics of SCR's for this application. The most critical static characteristic is blocking voltage and dynamically, high values of di/dt. The stress of high values of di/dt may be alleviated by using a saturating reactor in series with the SCR.

In order to minimize jitter, and the delay and rise time, the gate of the SCR should be driven as hard as the ratings permit. The rise time of the gate pulse should be much less than 1 microsecond.

High frequency SCR's such as the GE C141 make ideal pulse modulator switches.

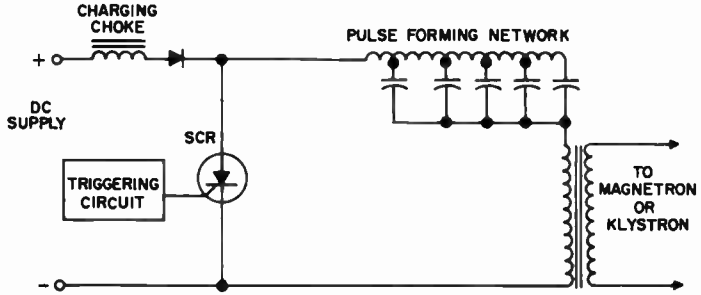

FIGURE 11.4.4 BASIC PULSE MODULATOR CIRCUIT

11.4.3 Cycloconverters [11]

A cycloconverter is a means of changing the frequency of alternating power using controlled rectifiers which are AC line (Class F) commutated. The cycloconverter is thus an alternative to the frequency changing system using a rectifier followed by an inverter.

11.4.3.1 Basic Circuit

The method of operation is readily understood from Figure 11.4.5. A single-phase full-wave rectifier circuit is equipped with two sets of SCR's, which would give opposite output polarities. Thus if SCR_1 and SCR_2 are

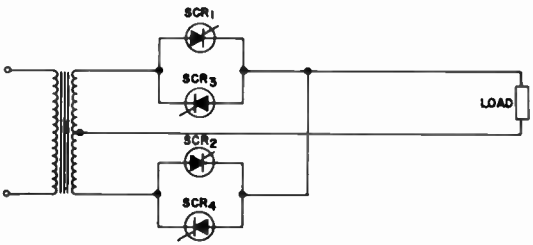

FIGURE 11.4.5 SINGLE PHASE CYCLOCONVERTER

triggered the DC output would be in the polarity shown on the left side of Figure 11.4.5. If SCR_3 and SCR_4 were triggered instead, the output polarity would be reversed as shown. Thus, by alternately triggering the SCR pairs at a frequency lower than the supply frequency a square wave of current would flow in the load resistor. A filter would be needed to eliminate the ripple.

In order to produce a sine wave output, the triggering of the individual SCR's would have to be delayed by varying degrees so as to produce the waveform shown in Figure 11.4.6.

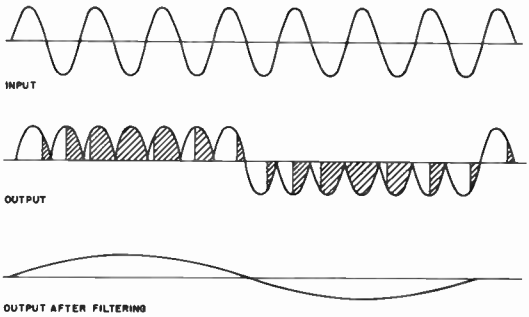

FIGURE 11.4.6 SINGLE PHASE CYCLOCONVERTER WAVEFORMS

11.4.3.2. Polyphase Application

The SCR cycloconverter is important in two applications. In the variable-speed, constant-frequency system an alternator is driven by a variable-speed motor such as an aircraft engine, yet the required output must be at a fixed and precise frequency such as 400 Hz. A second application is where the required output must be variable in both frequency and amplitude for driving an induction or synchronous motor. This makes possible variable speed brushless motors which could for example be used to drive the wheels of vehicles operating in difficult environments.

Due to the advantages in AC motor design, most of the cycloconverter systems are polyphase. Figure 11.4.7 shows a typical schematic (excluding the trigger circuit).

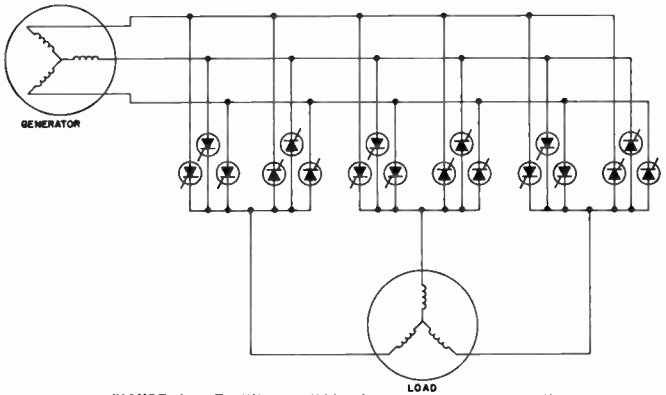

FIGURE 11.4.7 THREE PHASE CYCLOCONVERTER CIRCUIT

11.4.3.3 Discussion

The pro's and con's of cycloconverters versus rectifier-inverters as frequency changers may be summarized as follows:

CYCLOCONVERTER	RECTIFIER-INVERTER
AC line commutation used	Additional commutation circuit necessary
Regeneration from overhauling loads possible	Regeneration in the rectifier stage not possible
Loads of any power factor may be accommodated	Sensitive to load power factor
Frequency range limited to below ⅓ of generator frequency	Wide frequency range
"Shoot through" of an SCR shuts the system down for less than one cycle provided the resulting current surge is non-destructive to the SCR	"Shoot through" of any one SCR shuts down the whole system
	Readily adapted to run from battery emergency supply
In a three-phase system a minimum of 18 load-carrying SCR's are required	In a three-phase system a minimum of 6 rectifier diodes and 6 load-carrying SCR's are required

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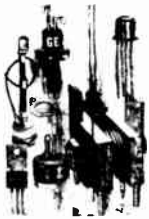
*Refer to Chapter 22 for availability and ordering information.

12 REGULATING SYSTEMS USING THYRISTORS



All regulating systems are closed loop systems. Closed loop systems, consequently regulating systems, are common in our everyday lives. For example, while driving an automobile the driver judges the degree of pressure on the steering wheel by considering such factors as road surface and curvature, speed of the automobile, foreign objects on the road, etc. The driver's eyes monitor these factors and through the human system, control his limbs to allow safe travel. This is a closed loop system. However, if the driver were to close his eyes, the result would be an open loop system. An open loop system is one which does not allow for unpredictable necessary corrections and is not recommended while driving an automobile. This chapter will be concerned with closed loop systems which do not rely on the human for completing the loop.

There are three terms which are used to describe closed loop systems: regulator, servomechanism, and servo. A *regulator* is a closed loop system that holds a steady level or quantity such as voltage, current or temperature, and often it needs no moving parts. A *servomechanism* is a closed loop system that moves or changes the position of the controlled object in accordance with a command signal. It includes some moving parts such as motors, solenoids, etc. The term *servo* has been generally adopted to mean either a regulator or a servomechanism and will be used as such in this chapter.

A well-designed servo has many advantages over an open loop system. It will accept a remote, low-power signal to precisely and quickly control a large amount of power. Because of its self-checking action it decreases the error which could result from external or internal disturbances. Its action is generally smooth. It provides unattended control.

To obtain these advantages, however, servos require precise design to prevent such problems as instability and slow response. Texts are available which necessarily use higher mathematics to explain servo design. A few of these texts are referenced at the end of this chapter and should be consulted. We will be concerned only with presenting the general concept of simple electronic servos and specifically those which use thyristors as the power controlling element. In general, these same principles could apply to hydraulic or mechanical systems.

Many applications are presently being satisfied by servos utilizing thyristors. The major parameters which are being controlled and some of their typical applications are as follows:

Major Parameter Being Controlled	*Application*
Speed	Pumps, fans, blowers, web drives, traction drives, conveyor belts, extrusion machinery, rolling mills, printing, silage unloading, home laundry, hand drills, food blenders and mixers, saber saws, electric knives, reprographics, and ice cream mixers.

Position	Welder position control, antenna drives, gun control.
Temperature	Reprographics, crystal ovens, room temperature, infrared ovens, chemical processing, extrusion head controls, diffusion ovens, cooking ovens, hair dryers, cooking utensils, clothes dryness controls, electric hot water heaters, electric blankets.
Light	Reprographics, room illumination, stage lighting, street light control, photoprojectors, decorative lighting.
Voltage and Current	Regulated battery chargers, DC to AC inverters, DC to DC converters, AC to DC power supplies, AC to AC cycloconverters.

Even though the thyristor servo system is a relatively new concept, there are many more applications presently being satisfied by such systems than those listed above. The list is presented here to give the reader some indication of the existing variety of tasks which are being performed by the thyristor servo system. In the future, these applications will be increased many fold.

Chapter 10 is devoted to some major methods of controlling motor speed using thyristors, the techniques of which are also applicable to motor position controls. The final part of this chapter will give some examples of complete thyristor servo systems which control the other major parameters of temperature, light, voltage and current.

12.1 BASIC MAKEUP OF A SERVO SYSTEM

As shown in the block diagram of Figure 12.1, a closed-loop system contains the following features:

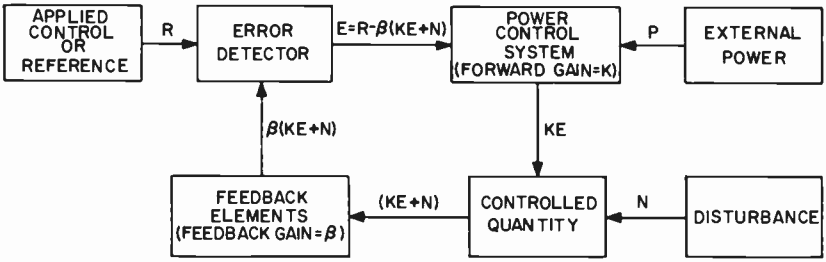


FIGURE 12.1 CLOSED-LOOP SYSTEM BLOCK DIAGRAM

1. Applied Control or Reference

This is a device giving an input signal, R, which sets the level or position the servo is asked to maintain. A potentiometer, or one of the many other well known reference devices, is used here.

2. Controlled Quantity

This is the resulting level or position (temperature, speed, illumination, etc.) which is being controlled by the system. It shall often be referred to as "KE + N" in this chapter.

3. Feedback Elements

This is generally a voltage or current sampler used to obtain an accurate indication of the controlled quantity (KE+N) and to process that quantity, β(KE+N),in a suitable form for comparison with the reference signal R.

4. Error Detector

This may be any device which is capable of comparing the signals R and β(KE+N), which can differ in magnitude and phase, and provide a resulting error, E. An electronic differential amplifier is an example of such a device.

5. Power Control System

This is a device or number of devices that are capable of receiving the error signal E and amplifying it with the result being KE. It can be one or more active elements. This element of the system includes the output device which produces or changes the controlled quantity (e.g., a resistance heating element to produce an oven temperature).

6. External Power

This is the power from a DC or AC source and is controlled proportionally to the error signal E, thus "amplification of signal E."

7. Disturbance

This block represents external disturbances, N, acting upon KE. They can be in the form of a heating load, torque requirements on a motor, etc.

12.1.1 Loop Operation

The closed loop portion of Figure 12.1 operates as follows. The signal E asks for a change in KE+N. E passes through the power control system changing KE, so as to change KE+N. The result is fed through and modified by the feedback elements which report the change to the error detector. It should be noted that many systems have minor loops (i.e., feedback around an active element, etc.) in addition to the major loop (the control of the temperature, light, etc.). We shall be concerned only with the major loop even though the theory applies to the minor loops as well.

The system can be regenerative, known as a positive feedback system and used for oscillators, or it can be degenerative, known as a negative feedback system.

Negative feedback systems, as employed by servo loops, have self-correcting features. For instance, let reference R be constant which ideally would result in a constant controlled quantity, if all other factors were to remain unchanged. Unfortunately, in a practical system, all other factors *do not* remain unchanged. Therefore, let us assume K increases to K_1, where K_1>K. For an initial E, this results in K_1E>KE and K_1E+N>KE+N. Consequently $\beta(K_1E+N)>\beta(KE+N)$ which, when compared to R in the error detector, results in a decrease in E. This causes a decrease in K_1E to a value close to the original KE, thus attempting to hold a constant controlled quantity. As another example let the power P increase. This could result in an increase in KE, β(KE+N) and a decrease in E which would tend to return KE to the level as originally requested by R. Still another example: let N cause an increase in KE+N being fed to the feedback elements. This would increase β(KE+N), decrease E and KE, and return KE+N close to its original level. Therefore we can conclude that a closed loop system with negative feedback suppresses internal and external disturbances and tends to maintain the controlled quantity at a level requested by the reference. It will be shown in the following section that the degree of maintaining the requested controlled quantity becomes a function of β, K and the time lags in the system.

12.2 THE IDEAL SERVO

The output signal of the power control system is KE while its input is E. Therefore we can define its forward gain as +K. Likewise the output of the feedback elements is β(KE+N) while its input is KE+N, therefore we can define the feedback gain as $+\beta$.

Note that we are applying the convention of "+" to β for negative feedback systems, therefore an increase in β results in a decrease in error signal E. For simplicity we shall allow "+K" and "+β" to be represented by "K" and "β."

The product βK is known as *loop gain*. For example if K = 80 and β = 1/4 (a loss through the feedback elements of 4/1 or a "gain" of 1/4), then the loop gain is 80 × 1/4 = 20. This could be measured by disconnecting the output of the feedback elements and terminating it with the representative impedance of the error detector. Then by utilizing suitable meters and increasing R a known amount, say 0.1 volt, and if the β(KE+N) signal changes by 2 volts, the loop gain βK is 2 volts/0.1 volt = 20.

The loop gain determines the overall gain of the system, $\frac{KE+N}{R}$. This can be shown as follows:

Since
$$E = R-\beta(KE+N),$$
$$R = E+\beta(KE+N). \tag{12.1}$$

Therefore, the ratio of controlled quantity to the reference signal is:

$$\frac{KE+N}{R} = \text{overall system gain} = \frac{KE+N}{E+\beta(KE+N)} \tag{12.2}$$

or,
$$\frac{KE+N}{R} = \frac{K+\frac{N}{E}}{1+\beta\left(K+\frac{N}{E}\right)} \tag{12.3}$$

Now if N approaches zero,

$$\text{Overall system gain} = \frac{K}{1+\beta K} \tag{12.4}$$

Note that if $\beta K >> 1$, the overall system gain $= \frac{1}{\beta}$. In other words, in negative feedback systems where $\beta K >> 1$, the overall system gain is determined by the feedback and not the forward gain. The "operational amplifier" functions by this principle. It has a very predictable system gain as dictated by resistive feedback elements.

In most servos, however, a more useful property is $\frac{KE+N}{N}$, which is the system's ability to compensate for disturbances with a constant or zero R.

Letting R approach zero in equation 12.1,

$$N = \frac{E+\beta KE}{-\beta} \tag{12.5}$$

Hence, the ratio of controlled quantity to disturbance is:

$$\frac{KE+N}{N} = \frac{KE + \left(\dfrac{E+\beta KE}{-\beta}\right)}{\dfrac{E+\beta KE}{-\beta}}$$

This simplifies to:

$$\frac{KE+N}{N} = \text{effect of disturbances} = \frac{1}{1+\beta K} \tag{12.6}$$

Note in our example, where $\beta K = 20$, the effect of a disturbance would be $\frac{1}{1+20} = \frac{1}{21}$ of what it would have been without the feedback loop. This is usually referred to as the "stiffness" of the servo. Note that the stiffness improves about ten times with a $\beta K = 200$.

12.3 PRACTICAL SERVO

12.3.1 Phase Shift and Instability

We have been assuming an ideal closed loop system, i.e., a system in which the feedback signal, $\beta(KE+N)$, is produced practically instantaneously with a change in the reference signal R. Unfortunately, in the majority of practical servos this is a bad assumption.

In a practical servo the energy storing elements in the system, such as inductance, capacitance, moving elements, etc., delay the power control system and feedback signals. This can be considered as a phase lag which is aggravated as the rate of change of N or R is increased. Consequently, as the rate of change of N is increased while maintaining a constant R, the ability of the controlled quantity to remain constant is decreased. Likewise, as the frequency of R is increased, the ability of the controlled quantity to follow R is decreased. This is called its dynamic response and can be measured by applying an R signal of increasing frequency and monitoring the controlled quantity for a phase lag. A measure of dynamic response can also be obtained by applying a step function R signal while monitoring the controlled quantity and observing the time required to obtain a steady state level.

The block diagram of Figure 12.1 establishes that the function of the error detector is to *subtract* the feedback signal $\beta(KE+N)$ from the reference signal R to give a resulting error:

$$E = R-\beta(KE+N) \tag{12.7}$$

It is possible, however, when R has a high rate of change, to have sufficient phase lag between R and $\beta(KE+N)$ so that an *addition* will occur in the error detector. Concurrently, if the loop gain is large enough to compensate for the losses in the system, a controlled quantity will be produced by $\beta(KE+N)$, without a reference signal R. This is a positive feedback condition and is the basis of instability and self-oscillation. In oscillators of course this

is a very useful and desirable property. Fortunately, the loop gain decreases with increasing phase lag due to the shunting effects of capacitors, frequency response of active elements, etc. Nevertheless servos, if not properly designed, have a tendency to be unstable when excited at some frequency for which $\beta(KE+N)$ has sufficient phase lag and the concurrent loop gain is large enough to overcome the system losses.

12.3.2 Analysis

12.3.2.1 Nyquist Approach

There are several methods available to the engineer for evaluating a simple* servo system with respect to its freedom from instability and self-oscillation. One method is to disconnect and properly terminate the output of the feedback elements, and to apply an E signal consisting of a changing frequency sine wave of constant unit amplitude. By monitoring E and $\beta(KE+N)$ the phase lag and loop gain are recorded. Then, by using Equation 12.1, $R = E+\beta(KE+N)$, the phase lag, R and loop gain are plotted. It can then be predicted where, if at all, the closed loop system will be unstable or oscillate. This is known as the Nyquist approach with the result being a Nyquist plot as shown in Figure 12.2.

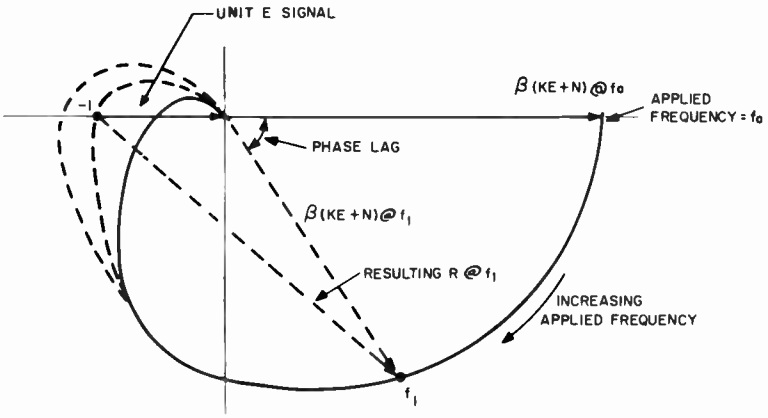


FIGURE 12.2 NYQUIST PLOT OF A TYPICAL SIMPLE SERVO SYSTEM

As indicated on the plot at the frequency of f_1, the R magnitude shown would be necessary to produce the unit E after comparison in the error detector with the $\beta(KE+N)$ shown at f_1. If the plot were to take the path of the solid line, then at a phase lag of 180° (on the negative real axis) R and $\beta(KE+N)$ would be in phase and add to produce a unit E. Note, however,

*In general, level and speed regulators are considered "simple" servos. Although the methods of evaluation and general discussion presented here apply to complex position controls as well, the plots of 12.2, 12.4 and 12.8 are typical for "simple" servos only.

an R signal would be necessary to produce the E. Therefore, according to Nyquist, the gain is not high enough to cause instability even though this is positive feedback. If the plot were to take the path of the dotted line passing through the -1 point, then at a phase lag of 180°, R would be zero and β(KE+N) would be as large as the unit E. This would result in the system self oscillating at whatever frequency caused the 180° phase lag. If now the plot took the path of the dotted line to the left of the -1 point, at a phase lag of 180° β(KE+N) would result in an E larger than unity which would produce a still larger β(KE+N), etc. This could cause a runaway or unstable condition.

Therefore, the "Nyquist criterion" for a simple servo is that, if the plot were to take the path of the dotted line to the left of and so as to surround the -1 point, the system would have a tendency to be unstable or self-oscillate. In practice, however, it is advisable to keep a large stability margin by crossing the axis to the right of the -1 point.

12.3.2.2 Bode Approach

Another method of servo analysis is the Bode approach. Whereas the Nyquist approach required point by point measurement, the Bode requires only that the gain of the servo system be known at one frequency together with the time constants of the main energy storing elements in the system.

To describe the Bode approach it is necessary to briefly review some simple circuits which have one energy storing element.

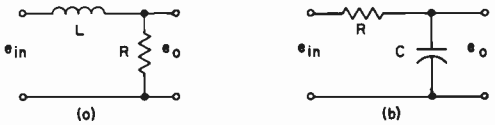


FIGURE 12.3 SIMPLE ENERGY STORING CIRCUITS

In (a) or (b) of Figure 12.3, as the frequency of e_{in} is increased, the ratio of $\frac{e_o}{e_{in}}$ is decreased. At a frequency of:

$$f_1 = \frac{1}{(2\pi)(\text{ time constant})}$$

we find that

$$\frac{e_o}{e_{in}} = 0.707 = 3 \text{ db loss or } -3 \text{ db}$$

In addition, e_o lags e_{in} by 45° at that frequency. As the frequency of e_{in} is further increased, say doubled, the ratio of $\frac{e_o}{e_{in}}$ decreases by approximately 6 db with a corresponding increase in phase lag. It can be shown that each time the frequency is doubled (called an octave) the ratio $\frac{e_o}{e_{in}}$ decreases by an additional 6 db with a corresponding increase in phase lag. In the limit, the phase lag would theoretically reach 90°. Consequently it can be said that

the effect of any energy storing element in a closed loop may be shown as a decreasing slope of 6 db/octave from the f_1 point. Further, this slope will eventually result in a 90° phase lag between R and β(KE+N).

The Bode approach or plot is one in which the f_1 point is calculated for each main energy storing element in the system. These points are then placed on a base line, usually the steady state loop gain of the system, with a −6 db/octave line drawn from each point. The resulting points are then vectorially added. A smooth curve is drawn so as to pass about 3 db inside the corners or breaks. This curve represents the system response. Figure 12.4 shows a Bode plot of a simple servo system with three energy storing elements.

Since a 6 db/octave slope (called a unit slope) will ultimately result in a 90° phase lag between R and β(KE+N), a 12 db/octave line (called a 2-unit slope) will ultimately result in a 180° phase lag, etc. The system may* oscillate where the smooth curve has 2-unit slope or greater and a gain greater than zero db (point of unity gain).

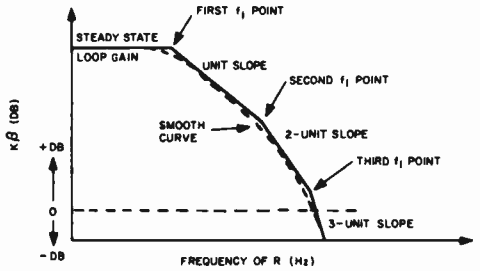


FIGURE 12.4 BODE PLOT OF A SIMPLE SERVO SYSTEM WITH 3 ENERGY STORING ELEMENTS.

The typical system shown may oscillate since it has sufficient gain concurrent with a 2-unit slope.

12.3.3 Corrective Networks

It appears from the Nyquist and Bode plots that it is necessary to reduce loop gain in order to prevent a servo from becoming unstable or from self-oscillating. However, we previously established that a high loop gain may be desirable. Consequently, it is often necessary to install corrective networks in the system, the purpose of which is to allow a high gain, stable system. These corrective networks are usually placed in the low power circuitry where they can be small and have an overall effect on the system.

(a) Phase Lead Network

Since it has been established that instability is caused by phase lag together with sufficient loop gain, it seems appropriate to counteract the lag with a lead network. A typical lead network is shown in Figure 12.5.

*An exact analysis would require a plot of instantaneous phase lag. This can be plotted by knowing the distance from the f_1 points and the magnitude of the slopes.

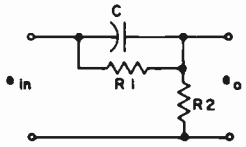


FIGURE 12.5 PHASE LEAD NETWORK

At low e_{in} frequencies, e_o is almost solely dictated by the ratio of R_1 and R_2. As the frequency is increased, C tends to reduce the series impedance and increase e_o.

If this network is strategically placed so that it cancels a portion of the system lags, a stable high gain system will result. This is easily seen on a Bode plot by summing a 6 db/octave increasing slope with a 12 db/octave decreasing slope. This would result in a 6 db/octave decreasing slope with its inherent ultimate phase lag of 90°. The graphical effects of this will be shown in Figure 12.8.

(b) Phase Lag Network

Another method is to properly place a phase lag corrective network in the system. A typical network is shown in Figure 12.6.

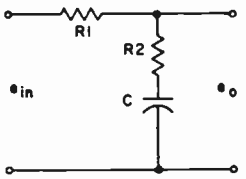


FIGURE 12.6 PHASE LAG NETWORK

At low frequencies e_o nearly equals e_{in}. As the frequency is increased, C reduces the shunting impedance until e_o is determined only by R_1 and R_2. Since e_o does have a lower limit this particular lag network is referred to as a limited lag network.

Essentially, a lag network results in a lower gain at higher frequencies. However, it is important that the total phase lag created does not result in an extended 2-unit slope of the smooth curve prior to crossing the zero db line when represented on a Bode plot. The graphical effects of this will be shown in Figure 12.8.

(c) The Lag-Lead or Notch

The result of combining the previously described lag and lead networks is a "lag-lead" or "notch" network as shown in Figure 12.7.

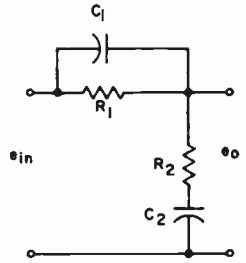


FIGURE 12.7 LAG-LEAD OR NOTCH NETWORK

As in the lag network, at low frequencies e_0 nearly equals e_{in}. As the frequency is increased, e_0 decreases due to the action of C_1 and C_2. The components are chosen so that a reduction in e_0 does occur at some frequency. As the frequency is further increased, e_0 then increases due to the overtaking shunting effect of C_1 on R_1. A network of this type is used where additional response plot shaping is required over that which can be obtained by a lag or lead network.

The results of such a network are shown in Figure 12.8 as applied to Figure 12.4.

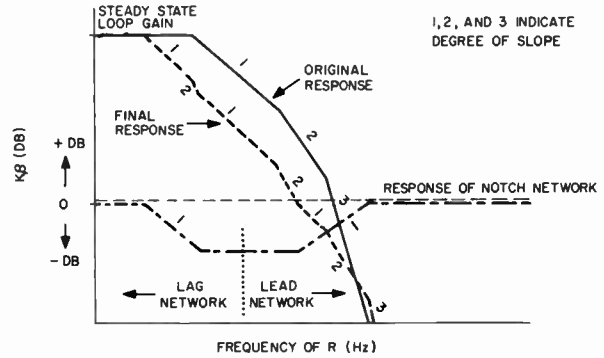


FIGURE 12.8 EFFECT OF A NOTCH NETWORK ON FIGURE 12.4

For simplicity the final smooth curve is not shown. If it were it would show that the system would not oscillate since it does not have an extended 2-unit slope until below zero db gain.

12.3.4 Ease of Stabilizing

Simple servos, in which the controlled quantity is a level or speed, are usually not difficult to stabilize. However, systems in which the controlled quantity is a position, as produced by a motor, are more difficult to stabilize. Due to the inherent 90° lag while the motor is establishing its position, the system starts out with a unit slope and will probably require corrective networks to avoid a 2-unit slope. There is a more difficult case however—systems which utilize one positioning motor to position another. This results in an immediate 2-unit slope during positioning and always requires precise corrective networks and design.

12.3.5 Linearity Domain

The previous discussion showed that, in a practical servo, there is a frequency of R above which the accumulative phase lags may cause instability. It was not mentioned, however, that in some servos there is a lower frequency of R below which KE+N is not regulated. These upper and lower limits specify a frequency range of R for which KE+N will be controlled.

In addition to the frequency range, there is also an amplitude range of R which is shown in Figure 12.9.

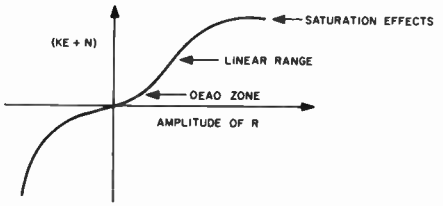


FIGURE 12.9 PRACTICAL SERVO RESPONSE TO AMPLITUDE CHANGES OF R

Due to dead zones and saturation effects, for small and large amplitudes of R respectively, the response of KE+N is not proportional for all values of R.

These two considerations, frequency and amplitude, dictate a range of R for which KE+N changes continually and proportionally. This range is called its linearity domain. A servo which operates within its linearity domain is considered to be "linear." The range of amplitude and frequency values within the domain are functions of each other, i.e., a given amplitude is not included in the domain for all frequencies.

Servos can seldom be boldly classified as linear or non-linear. Usually, a so-called "linear" servo does not have an infinite linearity domain. Likewise a linearity domain can often be found for a non-linear servo—it may be extremely small however. The Nyquist and Bode approaches are designed to analyze systems within their linearity domains, i.e., "linear" systems. Unfortunately, there are no comparable general solutions for systems which operate outside the linearity domain, i.e., "non-linear" systems.

12.4 SERVOS UTILIZING LATCHING ELEMENTS (THYRISTORS) IN THE CONTROL SYSTEM

Severe non-linearity occurs when on-off switching devices are utilized to regulate quickly responding controlled quantities. Further, when a latching switch is utilized (once triggered, it stays on until commutated off), such as an SCR or triac, the system becomes inoperative unless the controlled quantity is made to have a slow response.

12.4.1 SCR's with Quickly Responding Controlled Quantities

As an example, let us attempt to regulate the voltage to a resistive load* utilizing an SCR phase control. (See Chapter 9 for a full discussion on phase control.) Also, assume no delays or averaging elements within the system. The results of this hypothetical system are shown in Figure 12.10.

*It is convenient to refer to the element to which the power is applied as the load, i. e. the heater, lamp, etc. The load may either produce or change the controlled quantity as later examples will illustrate.

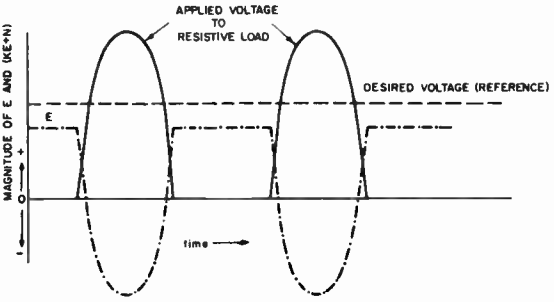


FIGURE 12.10 HYPOTHETICAL UNREGULATED REGULATOR

Note the error signal forces the SCR to turn on at the beginning of each half cycle. Consequently full line voltage will be continuously applied. Therefore, the actual voltage will be the unregulated full one-half cycle average.

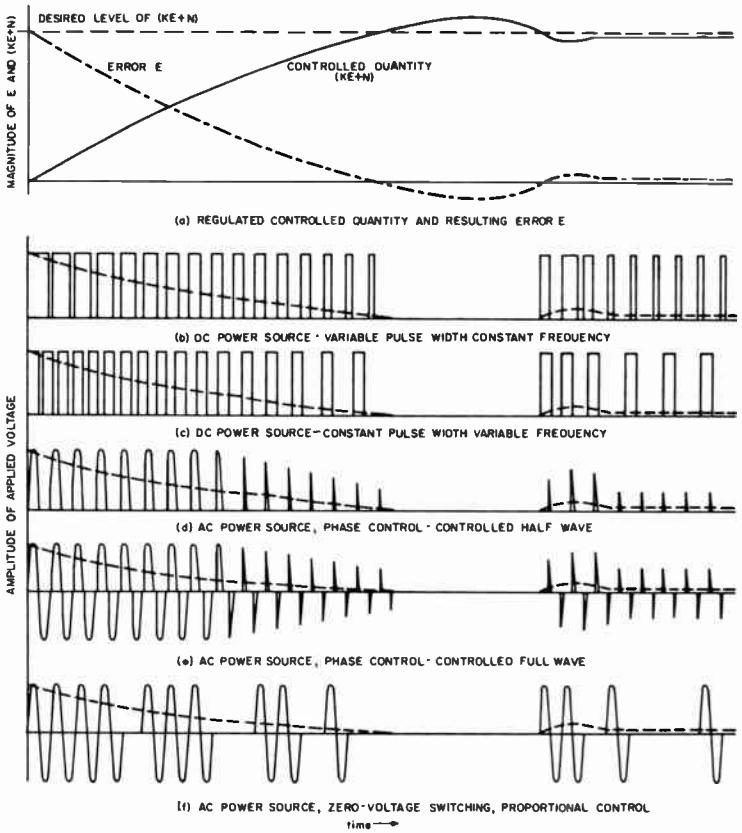


FIGURE 12.11 REGULATING CONTROLLED QUANTITY WITH SCR OR TRIAC-PROPORTIONAL CONTROL.

12.4.2 Thyristors with Slowly Responding Controlled Quantities

Fortunately SCR's and triacs can be used to regulate controlled quantities which have long averaging time constants when compared to their switching frequencies. Temperature, light, and motor speed are such quantities. They allow a linearity domain to be established with the result being the regulation of the controlled quantity.

Figure 12.11(a) shows the regulation of a typical controlled quantity with a long averaging time. Also shown, and in the same time scale, are some of the basic switching methods for SCR's and triacs. The curves are drawn for a resistive load such as a heater or a lamp. The dotted lines in Figures 12.11(b), (c), (d), (e), (f) indicate the average power being delivered to the load. The pulse spacing in some of the illustrations may not be exactly correct for the average power shown but serves to illustrate methods of varying the load power.

12.4.2.1 DC Power Source

Figures 12.11(b) and (c) indicate time ratio control as derived from a DC power source. The techniques involved in switching SCR's from a DC source are discussed in Chapter 5.

12.4.2.2 AC Power Source

Figures 12.11(d), (e), and (f) show power being delivered to the load from an unrectified and unfiltered AC source. These are very popular methods since a source of this type is readily available, simplifies SCR commutation (see Chapter 9), and is compatible with the triac (see Chapter 7).

Figures 12.11(d) and (e) are phase-control methods as discussed in Chapter 9. One other basic phase-control method, which is discussed in Chapter 9 but not shown here, is the controlled-half-plus-fixed-half-wave. This method should be utilized for controlled quantities which require regulation only from one-half to full power. It should be noted that Figures 12.11(d) and (e) were drawn assuming the cosine-modified ramp and pedestal technique as discussed in Chapter 9. Its importance in servo systems requires the following brief discussion.

Phase-control, without the use of the cosine-modified ramp and pedestal, results in a non-linear curve of the voltage delivered to the load for a varying error signal. This is shown in Figure 12.12.

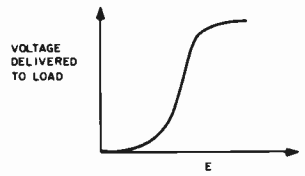


FIGURE 12.12 UNMODIFIED PHASE CONTROL

Note the large dead zones and saturation levels for small and large values of error signal respectively. At these values of E the system gain is low as compared to that of the intermediate region. Consequently, at these levels, the system's ability to compensate for disturbances would be decreased from that of the intermediate region. Unfortunately, in Figure 12.11, the small values of E are most important since this is the area of regulation. To improve this regulation, the overall system gain would have to be increased and the system could become unstable in the intermediate region. However, the cosine-modified ramp and pedestal technique allows the curve of Figure 12.12 to be linearized as shown in Figure 12.13.

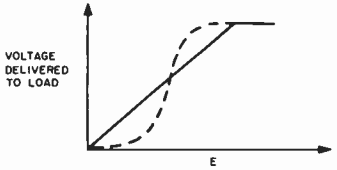


FIGURE 12.13 MODIFIED PHASE CONTROL

The system is shown to have a constant voltage gain over the E range of interest. Consequently at small values of E, disturbances will have the same effect as experienced in the intermediate region. This will result in good regulation without the need for an increase in overall system gain.

Figure 12.11(f) shows the load power being controlled by zero-voltage switching. Zero-voltage switching is a method whereby AC power is applied to the load only when the instantaneous line voltage is zero. This has significant advantages in that it eliminates radio frequency interference (RFI). (Chapter 16 discusses RFI suppression.) It should be noted that, to obtain a "linear" system using this method, the time constant of the controlled quantity must be larger than in the previous methods because of the longer on and off times involved. Consequently this method is not applicable to shorter time constant quantities such as light and motor speed, but has proven to be extremely useful for temperature controls.

12.4.2.3 Proportional and On-Off Control

All of the methods discussed in Figure 12.11 result in proportional control. The nature of a proportional control is to realize the magnitude of the error between the actual and desired levels of KE+N and adjust the power to the load accordingly. Consequently, KE+N approaches its final level at a lower rate than it originally had when the error signal was large. This results in a small overshoot and quick recovery. Note, however, that some steady state error must exist to supply sufficient power to the load in order to maintain KE+N at the desired level. The magnitude of the error is directly related to the gain of the system. If only a very small error is necessary, the system will have high gain with all advantages thereof. However as the gain is increased, a point is ultimately reached where the proportionality feature is eliminated and the system reverts to on-off control. This results in larger overshoots but has the advantage of generally being able to hold KE+N with less error when subjected to internal and external disturbances. Figure 12.14 shows the resulting curves of an on-off system.

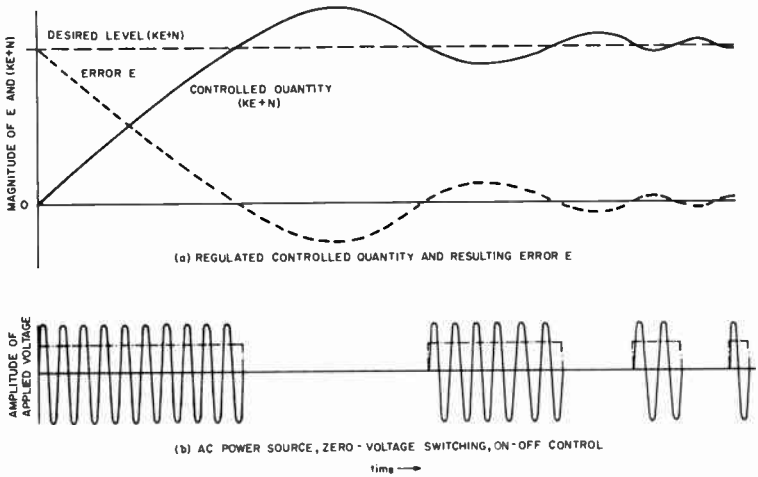


FIGURE 12.14 REGULATING CONTROLLED QUANTITY WITH SCR'S OR TRIAC— ON-OFF CONTROL.

Note the large overshoot and the varying KE+N at "steady state." The system must have a variation, however slight, to regulate KE+N.

Figure 12.14(b) shows AC power utilizing zero-voltage switching being supplied to the load. The dotted lines again show the average power. The comments that were made with reference to proportional zero-voltage switching are applicable to this on-off method as well.

12.4.2.3.1 Selection of Control Considering Hysteresis, Overshoot, Transport Lag

It should *not* be concluded that every on-off control exhibits improved regulation over a given proportional control in all applications.

One reason is that if the curve of Figure 12.14 were explicitly correct, we would find that the load voltage would not be applied until the error signal became slightly positive. Further the voltage would not be removed until the error became slightly negative. The difference in error signal between voltage application and removal is known as hysteresis. Hysteresis reduces the regulation accuracy of an on-off control.

Other obvious considerations as noted in Figures 12.11 and 12.14 are overshoot and speed of response. If large overshoots cannot be tolerated, then a proportional control should be utilized. However, the speed with which KE+N responds will decrease.

Many systems cannot utilize a pure on-off control. This is especially true where a transport lag is present. Transport lag differs from overshoot in that KE+N is not realized until sometime after the initiation of an error signal. This constitutes a time delay as opposed to a phase delay associated with an overshoot. Consequently, if an on-off control were utilized in a system with a transport lag, KE+N could vary between its maximum and mini-

mum limits continuously due to the time lapse. However, a properly designed proportional control will allow the desired intermediate level to be maintained.

Generalization is difficult when recommending proportional or on-off control. Each application must be analyzed individually considering such factors as mentioned above.

12.4.2.4 Phase Lags

Controlled quantities with long averaging time constants will help considerably in reducing instability resulting from the energy storing elements in the system. However, the possibility of instability does exist and is highly probable with the quicker responding controlled quantities. To properly cope with instability, the principles reviewed here should be mastered through the use of the many texts devoted to the subject, some of which are referenced at the end of this chapter.

12.5 ILLUSTRATIONS OF SERVOS USING THYRISTORS

This section is devoted to examples of servo systems utilizing SCR's and triacs for controlling power to the load. They do not exemplify all of the available methods of utilizing these devices in servos, but will suffice to illustrate some of the more popular.

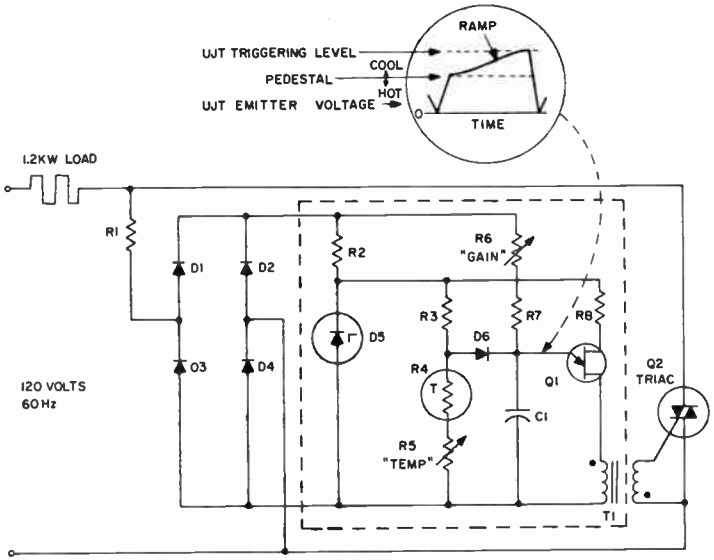
The approach here will be to briefly explain the basic servo loop of these systems and to point out their salient features.

12.5.1 1.2 kw Phase-Controlled Precision Temperature Regulator

Figure 12.15 shows a temperature regulator utilizing cosine-modified ramp and pedestal phase-control. Its method of operation is as follows. The triac supplies controlled full wave, phase-controlled AC power to the heater load. This increases KE+N, which is the temperature in this case, at a rate slower than the switching frequency of the triac. Thus KE+N has a long averaging time constant. The feedback element, thermistor R_4, senses the temperature and when compared by the unijunction error detector with the R_5 reference signal, controls the turn on of the triac so as to regulate KE+N.

It should be noted that the feedback elements, reference signal and error detector are located within the dotted block. The output of this block is the error E, which controls the triac through T_1. The basic configuration of the unijunction and complementary components located within the block is very popular when used with thyristors for obtaining any of the phase-control methods of Chapter 9. Therefore it is important to realize what constitutes the error E in this configuration.

As discussed in Chapter 9 and also shown in Figure 12.11, phase-control methods control the power to a load by controlling the point in time within the half cycle at which the thyristor will turn on. Since the thyristor is a latching device, it will stay on for the remainder of that half cycle.



R1, R2 = 2200 OHMS, 2 WATTS
R3 = 4700 OHMS, 1/2 W
R4 = THERMISTOR, APPROX 5000 OHMS AT OPERATING TEMPERATURE, GE-4H
R5 = 10,000 OHMS W.W. POTENTIOMETER
R6 = 5 MEGOHM POTENTIOMETER
R7 = 100K Ω, 1/2W
R8 = 1000 OHMS, 1/2 W

Q1 = GE 2N2646
Q2 = GE SC468
T1 = SPRAGUE 35ZM923 OR EQUIVALENT
D1-D4 = GE IN1693
D5 = GE Z4XL22
D6 = GE IN1692
C1 = 0.1μfd, 30V

FIGURE 12.15 1.2 KW PHASE-CONTROL PRECISION TEMPERATURE REGULATOR

Therefore, a large error should turn the thyristor on early in the half cycle and conversely a small error should result in a late turn on or possibly none at all.

Consequently, the result of the magnitude of the error E is the *point in time* within the half cycle at which the pulse turns the thyristor on—not the presence of the pulse (assuming it is large enough for turn on). The insert in Figure 12.15 shows how this is accomplished with cosine-modified ramp and pedestal control. When the compound magnitude of the ramp and pedestal rises sufficiently to trigger the unijunction, a pulse will be delivered which will turn the thyristor on. Therefore, the error E is the length of time required for the magnitude of the ramp and pedestal to exceed the unijunction's firing point since it determines the *point in time* which the thyristor will fire.

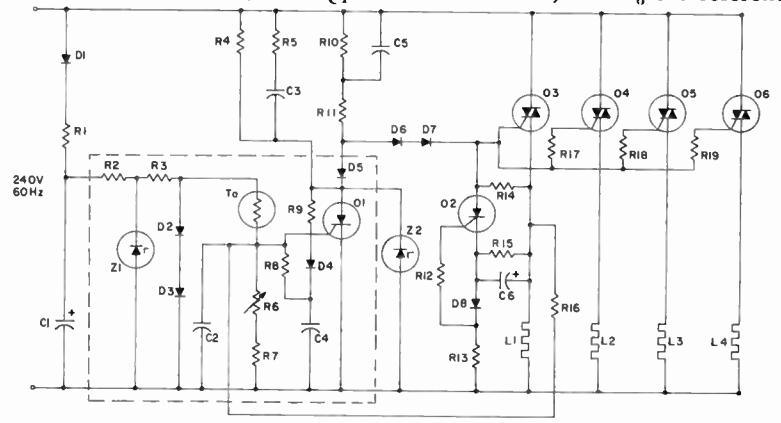
It is important to note that it is necessary for the dotted block to be stable when subjected to variations in line voltage, ambient temperature, etc., i.e., the E of $E = R - \beta(KE+N)$ remains constant for constant R and $\beta(KE+N)$ throughout the variations. If this relationship were to change, the gain of the system probably would not be affected but would result in a steady state error in KE+N. This particular circuit utilizes common voltage points and the stability of the unijunction to maintain the accuracy of the relationship.

As previously mentioned, this circuit utilizes ramp and pedestal phase control. Consequently the circuit gain can be increased through the setting of R_6, with all the advantages (and disadvantages) thereof.

It is difficult to speak of the overall accuracy of a temperature regulator since it is a function of the rate of change and magnitude of the disturbances, and the capacity of the heater when compared to the volume of the controlled chamber. However, it can be said that the dotted block is *capable* of controlling temperature to within a specified limit. Here the dotted block is capable of controlling temperature to within $\pm 2\%$ of the thermistor resistance over a $\pm 10\%$ variation in line voltage.

12.5.2 9.6 kw Zero-Voltage Switching Proportional or On-Off Temperature Regulator

Figure 12.16 shows a temperature regulator which utilizes zero-voltage switching of AC power to supply the load. The system can be made to be proportional or on-off. Its servo loop operates identically to that of Figure 12.15 with heater load L_1 through L_4, temperature as the KE+N, thermistor T_a the feedback element, SCR Q_1 the error detector, and R_6 the reference.



R1 - 22KΩ 2W
R2 - 470Ω
R3 - 5.6 KΩ
R4 - 39KΩ, 2W
R5 - 22KΩ, 7W
R6 - 1KΩ POT, 1/2W
R7 - 220Ω
R8 - 220KΩ
R9 - 220KΩ
R10 - 3K, 10W
R11 - 56Ω
R12 - 10KΩ
R13 - 22K, 2W
R14 - 100Ω
R15 - 2.2KΩ
R16 - 6.8MΩ
R17 - 10Ω
R18 - 10Ω
R19 - 10Ω
C1 - 50 μfd, 25 V
C2 - 001 μfd, 25V
C3 - 0.1μfd, 400V
C4 - 0.47 μfd, 25V
C5 - 0.82 μfd, 400V
C6 - 5 μfd, 15V
Q1, Q2 - GE C106Y1
Q3 THRU Q6 - GE SC46D
D1, D5, D6, D7 - GE A13D
D2, D3, D8 - GEA13A
D4 - GE A13F
Z1 - GE Z4XL16
Z2 - GE Z4XL9.1
To - GE 2D102 1K@25°C THERMISTOR
L1 THRU L4 - 2.4 KW HEATERS
NOTE: ALL RESISTORS 1/2 W, ±10% UNLESS OTHERWISE SPECIFIED

FIGURE 12.16 9.6 KW ZERO-VOLTAGE SWITCHING PROPORTIONAL OR ON-OFF TEMPERATURE REGULATOR.

However, the system does have some additional features. Note that the total load, L_1 through L_4, is divided equally and supplied by a master (Q_3) and 3 slaved triacs (Q_4, Q_5, Q_6). Also note the components around and including SCR Q_2. This group will automatically fire the master triac at the start of the negative half-cycle* provided the master had been turned on at the start of the positive half-cycle through C_5, R_{11}, D_6 and D_7. In addition the 10 ohm resistors in series with the gates of the slaved triacs assure that the slaves will faithfully turn on *after* the master on each half cycle.

Consequently, the result of having a master, slaves, and automatic negative half-cycle is as follows. If the master does turn on at the start of the positive half-cycle, the negative half will follow automatically with the slaves

*In all of these illustrations consider the negative half-cycle to exist when the lower incoming line is positive with respect to the upper line.

following the master on both half cycles. Consequently, the control circuit need only allow or not allow the master triac to turn on at the beginning of the positive half cycle.

The control circuit consists of the feedback element, reference, and error detector located in the dotted block. Depending upon the ratio of T_a, R_6, and R_7, the net result is Q_1 being off or on during the entire positive half cycle. If Q_1 is off, the master triac, and consequently the slaves, will apply load power during both half cycles. If Q_1 is on, the master will not have sufficient gate drive, and power will not be applied to the load during that cycle.

As in the last illustration, we are again concerned with the error signal being a true representation of $R - \beta(KE+N)$ during voltage and temperature variations. The reference diodes Z_1, D_2 and D_3 are included for this purpose.

The addition of components R_9, R_8, D_4 and C_4 change the system from on-off to proportional, but still in the zero-voltage switching mode of operation.

The basic concept of utilizing control SCR (Q_1) to allow or not to allow gate drive to an SCR or triac for the entire half cycle is a very popular method of achieving zero-voltage switching.

The dotted block is capable of regulating temperature with an accuracy of $\pm 0.5\%$ of the thermistor resistance over a $\pm 10\%$ variation in line voltage.

12.5.3 5 kw Half-Wave Zero-Voltage Switched On-Off Temperature Control

Figure 12.17 illustrates a temperature regulator which utilizes half wave zero-voltage switching, on-off control to control a low power hot wire relay. The relay in turn activates a large heater or other load operating directly across the power line.

KE+N is again temperature, T_a the feedback element, SCR's Q_1 and Q_2 the error detector, and R_4 the reference potentiometer.

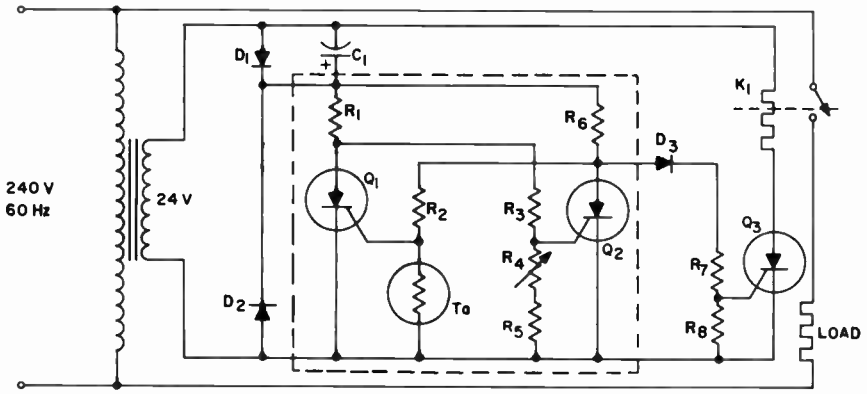
It should be noted that Q_3 operates on the positive half-cycle only. However, the decision to allow or not to allow Q_3 to turn on is made during the previous negative half-cycle. This is made possible by the leading voltage supplied by C_1. If Q_2 is off when the line starts to go positive, Q_3 will turn on through R_6, D_3 and R_7. However, if Q_2 is on, Q_3 cannot turn on for the remainder of the cycle. This is another example of a control SCR (Q_2) being utilized to provide zero-voltage switching of the power controlling element (Q_3).

The decision to allow or not to allow Q_3 to turn on is made by the feedback element, reference, and error detector shown within the dotted block. Q_2 and Q_1 are the major elements of the error detector. They subtract the $\beta(KE+N)$, as derived by T_a, from the reference R_4. This is accomplished by comparing the instantaneous magnitudes of the voltages at each gate. Since Q_2 and Q_1 are cross coupled, one and only one of them will be on during each half-cycle. Therefore, the first one to turn on remains on for the remainder of the negative cycle (made possible by C_1) and entire positive half-cycle. Consequently, if the decision is for Q_2 to turn on, Q_3 cannot turn on during that positive half-cycle and voltage will not be applied to the hot wire relay for that cycle.

The stability of the dotted block against voltage and temperature variations is achieved by symmetry.

The dotted block is capable of regulating with an accuracy of approximately ±0.2% of thermistor resistance over a ±10% variation in line voltage.

The hybrid concept (relay used with thyristors) of Figure 12.17 has the advantage of being able to control a large amount of power with relatively small thyristors. Also, the isolation provided by the relay allows this power to be easily utilized for loads other than heaters. Consequently, by proper choice of feedback elements, the circuit may be easily adapted to a number of high power loads. However, some of these may not allow a closed loop system, e.g., controlling the light level of a lamp load.



R_1, R6 – 560Ω, 1W
R_2, R_3 – 1.8KΩ
R_4 – 1KΩ POT 1/2W
R_5 – 100Ω
R_7, R_8 – 1KΩ

C_1 – 20μfd, 100V
Q_1, Q_2, Q_3 – GE C106F
D_1, D_2, D_3 – GE A13A
T_0 – GE 2D102, 1KΩ 25°C THERMISTOR
K_1 – KING SEELEY 63552 (110Ω COIL)
LOAD – 5KW HEATER

NOTE: ALL RESISTANCES 1/2 W, ±10% UNLESS OTHERWISE SPECIFIED

FIGURE 12.17 5 KW HALF-WAVE ZERO-VOLTAGE SWITCHED ON-OFF TEMPERATURE CONTROL.

12.5.4 3 kw Phase-Controlled Voltage Regulator

Figure 12.18 is shown here because it exemplifies a method of regulating the RMS value of an unfiltered phase-controlled voltage across a resistive load. As mentioned in Section 12.4.1, if β(KE+N) were derived directly from the resistive load, regulation would be impossible. However, Figure 12.18 utilizes a lamp in parallel with the load to provide the long averaging time constant which, in conjunction with a photocell, provides β(KE+N). The lamp can be considered as part of the load or feedback elements. We shall consider it to be the latter. Consequently, this introduces a useful concept of the averaging being done within the feedback element.

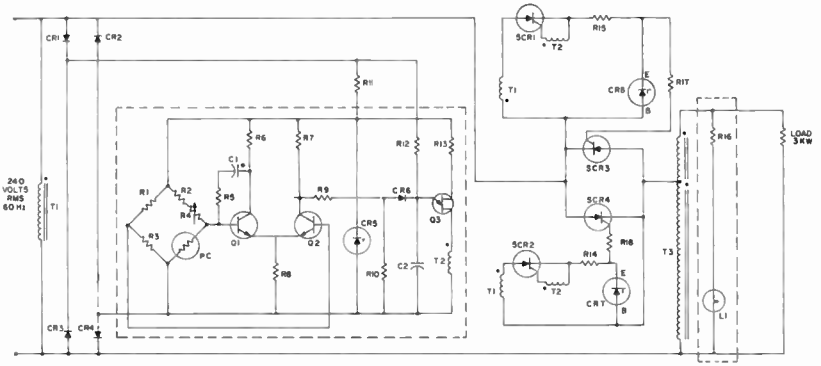
SCR's 3 and 4 supply KE+N which is the RMS voltage impressed across the 3 kw load resistor. The feedback elements, lamp L_1 and photocell P.C., provide a β(KE+N) which when compared by the unijunction error detector to the reference set by R_4, control SCR's 3 and 4 to regulate the RMS output voltage. (Refer to section 12.5.1 for a discussion of error E with phase-control.)

It should be realized that the KE+N of the system is the RMS voltage

and not the *power* being supplied to the load resistor, i.e., if the value of the load resistance were to change slightly so as not to disturb the KE+N, the β(KE+N) would not change and no correction would result.

Included in the dotted blocks are again the feedback element, reference, and error detector. The points of interest here are the stability to voltage and temperature variations through the use of a differential amplifier and unijunction, the ramp and pedestal technique utilized with phase-control, and the unijunction working with SCR's for phase-controlled AC.

The system also has other salient features which should be mentioned. For example, consider Figure 12.19. By placing a low resistance in series with the load and in parallel with the feedback lamp L_1, a current regulator is formed. Again this will not regulate the power to the load but only the current through it.



CR1 THRU CR4 - GE A 30
CR5 - GE Z4XL22
CR6 - GE A13F
CR7, CR8 - GE IN1423
C1 - 10μf, 25 VDC GE 62F204 MINIATURE TUBULAR WET SLUG CAP
C2 - 0.22μf, 50 VDC ±10% GE 75F3R5-244A
Q1,Q2 - GE 2N2925

Q3 - GE 2N2646
SCR1, SCR2 - GE C6U or C10B7
SCR3, SCR4 - GE C35E or C35E
T1 - 220 V RMS PRIMARY 12 V RMS SECONDARY 100 MA RMS RATED SECONDARY CURRENT
T2 - PULSE TRANSFORMER (1:1) ALADDIN PART NO 90-2398

T3 - TURNS RATIO 1:1.82, 4 KVA
R1 - 2.2 KΩ
R2 - 2.2 KΩ
R3 - 18 KΩ
R4 - 10 KΩ MULTI-TURN TRIM POT
R5 - 10 KΩ
R6 - 2.2 KΩ
R7 - 2.2 KΩ
R8 - 2.2 KΩ

R9 - 56 KΩ
R10 - 47 KΩ
R11 - 6.2 KΩ, 10 WATT
R12 - 1.5 MEGΩ
R13 - 1 KΩ
R14, R15 - 22Ω 2 W
R16 - 9K ±5%, 14 WATTS
R17 - 33Ω, 2 W
R18 - 33Ω, 2 W

L1 - INCANDESCENT LAMP OF GE PL58 (LAMP-PHOTOCELL) INTEGRAL HERMETICALLY SEALED UNIT
PC - CADMIUM SULFIDE PHOTOCELL OF GE PL58 (LAMP-PHOTOCELL) INTEGRAL HERMETICALLY SEALED UNIT
ALL RESISTORS 1 10% AND 1/2 WATT EXCEPT WHERE INDICATED

FIGURE 12.18 3 KW PHASE-CONTROLLED VOLTAGE REGULATOR

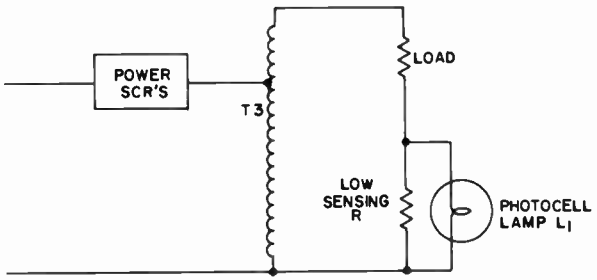


FIGURE 12.19 CIRCUIT CHANGES FOR CURRENT REGULATOR FOR FIGURE 12.18

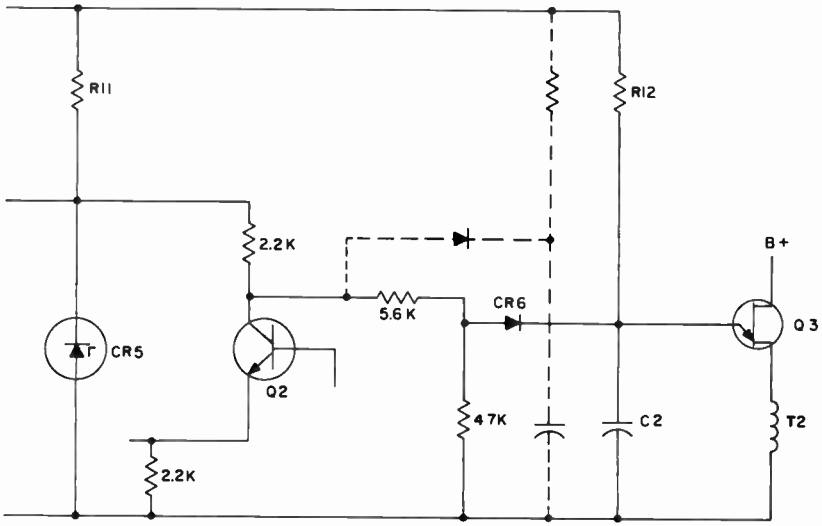


FIGURE 12.20 SOFT-START CIRCUITRY FOR FIGURE 12.18

An additional feature is that the 3 kw load could be a lamp. This would eliminate the need for the feedback lamp L_1. In this case the photocell could monitor, and the system would regulate, the light output of the load. If this were done, the soft-start circuit of Figure 12.20 might be necessary. See Chapter 9 for discussion of soft-start circuits.

Note also C_1 and R_5 in Figure 12.18. These components constitute a "notch" network necessary for stabilization.

Figure 12.21 shows the regulation obtained by the voltage regulator with a 3 kw resistive load for a regulated true RMS load voltage of 300 volts and a nominal input line voltage of 220 volts RMS, 60 Hz.

Input Line Voltage	True RMS Load Voltage	Load Voltage Change	Response Time
220 V RMS (Nom)	300 (Nom)	—	Less Than 100 msec. for step change in input
190 V RMS	Approx. 299.0	$\leq$ (0.33%)	
250 V RMS	Approx. 299.0	$\leq$ (0.33%)	

FIGURE 12.21 TABLE OF REGULATION FOR CIRCUIT OF FIGURE 12.18

12.5.5 860 Watt Limited-Range Low Cost Precision Light Control

The system of Figure 12.22 is designed to regulate an 860 watt lamp load from half to full power. This is achieved by the controlled-half-plus-fixed-half-wave phase control method discussed in Chapter 9. Half power applied to an incandescent lamp results in 30% of the full light output. Consequently the circuit is designed to control the light output of the lamp from 30% to 100% of maximum.

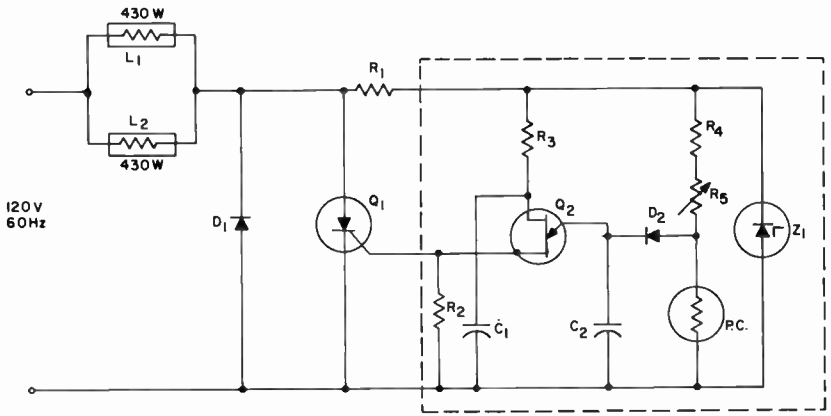
The operation of the closed loop is straightforward with the major features being the load L_1 and L_2, light the KE+N, P.C. the feedback element, Q_2 the error detector, and R_5 the reference.

The method of obtaining the controlled-half-plus-fixed-half-wave is easily seen by realizing that D_1 and Q_1 are in inverse parallel and in series with the load. Also note that Q_1 will turn on during the positive half-cycle at a time dictated by the feedback elements, reference, and error detector located in the dotted block. Consequently, the positive half-cycle is controllable. The function of the dotted block is identical to the ramp and pedestal control of Figure 12.15. Now note that D_1 will conduct during the entire period of every negative half-cycle. Therefore, the negative half-cycle is continually applied to the load. This configuration results in a controllable positive and fixed negative half-cycle applied to the load. It is interesting to note that when D_1 conducts during the negative half-cycle it resets the unijunction firing circuit.

Again temperature and voltage stability of the dotted block is achieved by Z_1, common voltage references, and the stability of the unijunction.

This method of phase-control results in an unsymmetrical wave with a resulting DC component. Therefore, this waveform is not suitable for transformer-fed loads.

The system will regulate the light level to within ±1% for a ±10% change in amplitude of the supply voltage.



R_1 - 6.8KΩ, 2W
R_2 - 47Ω
R_3 - 1KΩ
R_4 - 680Ω
R_5 - 1KΩ, 1/2W POT
P.C. - GE A35

Q_1 - GE C20B
Q_2 - GE 2N2646
D_1 - GE A4IB
D_2 - GE AI3F
Z_1 - GE Z4XLI6
L_1, L_2 - 430W INCANDESCENT LAMP

C_1 - .03μfd, 25V
C_2 - .01μfd, 25V
NOTE: ALL RESISTANCES 1/2w, 10% UNLESS OTHERWISE NOTED.

FIGURE 12.22 860W, LIMITED-RANGE, LOW-COST PRECISION LIGHT CONTROL

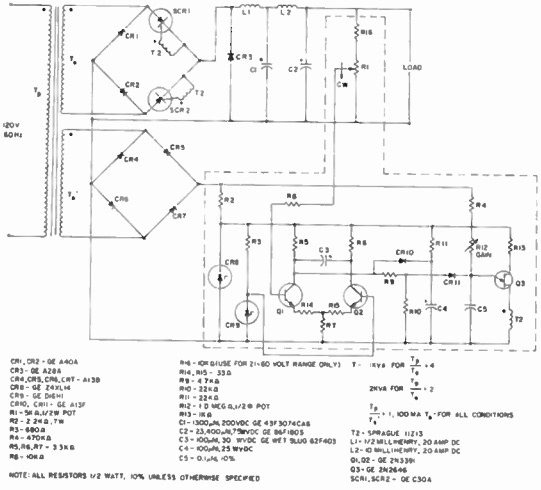
12.5.6 1.2 kw, 60 V Regulated DC Power Supply

Figure 12.23 shows a regulated DC power supply which utilizes cosine-modified ramp and pedestal control. The operation of the servo loop is similar to the previous examples with the load being any suitable external DC component or components, the DC output voltage being the KE+N, R_1 being the feedback element, Q_3 the error detector, and CR_9 the reference.

The group of components operating on the output of SCR_1 and SCR_2 constitute a highly filtered DC supply. If the SCR's were replaced with suitable diodes, the load voltage would be fixed at a DC level dictated by the transformer secondary voltage, T_S. If the number of T_S turns were doubled, the fixed DC level would also double. Therefore, by phase controlling SCR_1 and SCR_2 the DC level can be controlled up to a maximum voltage dictated by the T_S winding and the 120 volt source.

The function of the feedback element, reference, and error detector, all located in the dotted block, is to provide regulation by properly phase-controlling the SCR's. The basic operation of the dotted block is very similar to Figure 12.15. By comparing a portion of the DC output voltage, as sampled by the wiper of R_1, with the stable reference of CR_9, an error is generated by Q_3 (refer to section 12.5.1 for a discussion of error E with phase control). Consequently, by adjusting R_1 clockwise, the regulated output will increase until it reaches its maximum value. At maximum output, of course, the system has no regulating ability. The minimum amplitude is fixed by CR_9. A lower voltage CR_9 could be used which would allow a lower minimum output voltage.

The dotted block incorporates some interesting features. For example, the cosine-modified ramp and pedestal allow the use of the gain pot R_{12}. This should be adjusted for maximum regulation, overshoot, etc. Also note that the combination of CR_{10}, R_{11} and C_4 constitutes a soft-start circuit (see Chapter 9 for a discussion on soft start circuits). This feature protects the supply when starting under heavy loads. In addition, stability of the dotted block is achieved by CR_8, CR_9, the differential amplifier of Q_1 and Q_2, common voltage points and the unijunction Q_3.



CR1, CR2 - GE A40A
CR3 - GE A20A
CR4, CR5, CR6, CR7 - A13B
CR8 - GE Z4XL14
CR9 - GE D6EH
CR10, CR11 - GE A13F
R1 - 5K Ω, 1/2W POT
R2 - 2.2KΩ, 7W
R3 - 680Ω
R4 - 470KΩ
R5, R6, R7 - 3.3KΩ
R8 - 10KΩ
R9 - 10K (USE FOR 21-60 VOLT RANGE ONLY)
R10, R15 - 33Ω
R11 - 47KΩ
R12 - 10KΩ
R13 - 1KΩ
C1 - 1300μF, 200VDC GE 43F3074G6
C2 - 23,400μF, 75VDC GE 86F1805
C3 - 100μF, 30 WVDC GE WET SLUG 62F403
C4 - 100μF, 25 WVDC
C5 - 0.1μF, 10%
T - 1KVA FOR $\frac{T_S}{T_P} = 4$
2KVA FOR $\frac{T_S}{T_P} = 2$
$\frac{T_S}{T_P} = 1$, 100 MA T_S FOR ALL CONDITIONS
T2 - SPRAGUE 11Z13
L1 - 1/2 MILLIHENRY, 20 AMP DC
L2 - 10 MILLIHENRY, 20 AMP DC
Q1, Q2 - GE 2N338
Q3 - GE 2N2646
SCR1, SCR2 - GE C30A
NOTE: ALL RESISTORS 1/2 WATT, 10% UNLESS OTHERWISE SPECIFIED

FIGURE 12.23 1.2KW, 60V REGULATED DC POWER SUPPLY

Load Voltage volts DC	Ripple - 120 Hz millivolts peak-to-peak	Response Time milliseconds	Load Regulation Percentage	T_1 Ratio
10	40 at 2.5 Amps I_L 70 at 20 Amps I_L	100 - 2.5 to 20 Amps 100 - 20 to 2.5 Amps	2% for 2 to 10 Amps I_L .03% for 10 to 20 Amps I_L	4:1
15	60 at 2.5 Amps I_L 360 at 15 Amps I_L	——	——	4:1
20	40 at 2 Amps I_L 880 at 20 Amps I_L	200 - 2 to 8 Amps I_L 150 - 8 to 2 Amps I_L No Check for V_{Line}	1% for 2 to 8 Amps I_L 2% for 8 to 20 Amps I_L $\pm$½% for $\pm$15% Swing in V_{Line} at input to T 10 Amp Load	4:1
25	800 at 20 Amps	——	2% for 2.5 to 10 Amps I_L 1% for 10 to 20 Amps I_L	2:1
40	700 at 20 Amps	200 - 3 to 20 Amp I_L	½% for 3 to 20 Amps I_L ½% for 3 to 8 Amps I_L	2:1
50	200 at 10 Amps	——	$\pm$0.4% for $\pm$15% Swing in V_{Line} at input to T I_L = 10 Amps	2:1
60	500 at 20 Amps 280 at 12 Amps	150 - 2.5 to 12 Amps I_L 75 - 12 to 20 Amps I_L	2% for 2.5 to 12 Amps I_L 1.5% for 12 to 20 Amps I_L	2:1

FIGURE 12.24 PERFORMANCE OF CIRCUIT OF FIGURE 12.23

Figure 12.24 shows the performance of the supply. The output voltage is adjustable between 7 and 21 volts, or 21 and 60 volts by changing the turns ratio of T_S; with a maximum load of 20 amperes in each range. The response time could be reduced, if desired, at the expense of increased ripple.

12.5.7 Fan and Coil, 3 Ampere Blower Speed Control, Temperature Regulator

The system of Figure 12.25 illustrates a concept whereby a blower load is phase-controlled as a means of regulating temperature, the power to create the temperature being derived from an external source not included in the system. This regulator may be used with systems which have a single blower to regulate both room heating and cooling.

Triac Q_1 supplies the power to the blower motor. This in turn changes the room temperature, KE+N, which is monitored by the feedback thermistor T_a. The feedback signal is then compared in the unijunction error detector with reference R_5 and the resulting error fed to triac Q_1.

It should be recognized that the KE+N, being temperature, has again a long averaging time constant compared to the switching frequency of the triac. The actual speed of the motor is of minor importance since it is included within the closed loop.

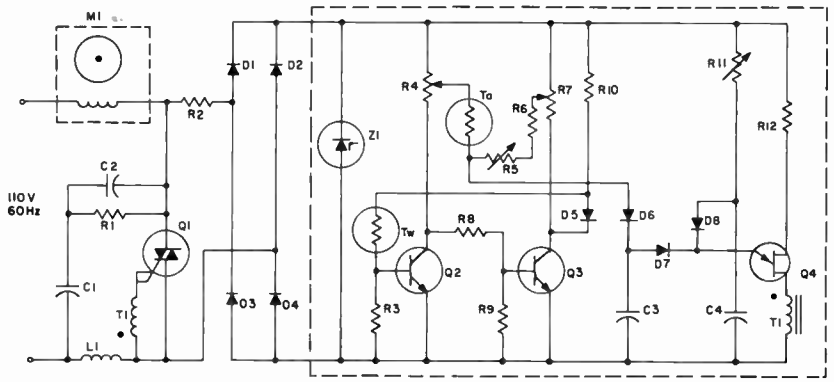
Again the feedback elements, reference, and error detector are located inside the dotted block. Note that this circuit utilizes ramp and pedestal control. Also note that Z_1, common voltage points, and a unijunction are used for stability against voltage and temperature variations. The operation of the dotted block is very similar to Figure 12.15, however it also incorporates some additional features. Note the thermistor T_w and the transistor flip-flop consisting of Q_2 and Q_3. This combination senses the water temperature (when water is used as a medium to both heat and cool a room) to give the proper "sense" to the blower, i.e., to give the blower more or less speed as proves necessary to regulate room temperature under heating or cooling conditions.

Note also R_{11}, D_7, D_8 and C_4. These components provide a minimum speed below which the blower will not be requested to function. This is use-

ful if a gentle circulation of air is required at all times or if the motor bearings will not allow motor operation below a minimum speed.

The combination of L_1, C_1, C_2 and R_1 also provide an interesting feature of this circuit. This combination is used to reduce the rate of rise of voltage and current in the circuit thereby suppressing the possibility of the triac failing to commutate. This combination also suppresses radio frequency interference. These two considerations are discussed in Chapters 9 and 16 respectively.

The dotted block is capable of controlling temperature to ±3% of thermistor resistance throughout a ±10% variation in line voltage.



R1 - 82Ω	R9 - 3.3KΩ	QI THRU Q4 - GE 6RSI6PBILAJI	MI - 3 AMP SHADED POLE MOTOR
R2 - 4.7KΩ, 4W	R10 - 4.7KΩ	D5 THRU D8 - GE AI3F	TI - SPRAGUE 11Z12 PULSE TRANSFORMER
R3 - 1KΩ	R11 - 100Ω, 1/2 W	QI - GE SC41B	
R4 - 5KΩ POT, 1/2W	R12 - 1KΩ	Q2, Q3 - GE 2N2712	NOTE: ALL RESISTANCES 1/2 W, ±10% UNLESS OTHERWISE SPECIFIED.
R5 - 5KΩ POT, 1/2W	C1 - 0.22μfd, 200V	Q4 - GE 2N2646	
R6 - 3.3KΩ	C2 - .05μfd, 200V	ZI - GE Z4XL20	
R7 - 5KΩ POT, 1/2W	C3 - 0.1μfd, 50V	Tw - GE 10103, 5K @ 25°C THERMISTOR	
R8 - 22KΩ	C4 - 0.1μfd, 50V	To - GE 10103, 5K @ 25°C THERMISTOR	

FIGURE 12.25 FAN AND COIL, 3 AMP BLOWER SPEED CONTROL, TEMPERATURE REGULATOR

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2. "Servomechanisms and Regulating System Design," H. Chestnut and R. W. Mayer, John Wiley and Sons, Inc., New York, N. Y., Vol. I, 2nd Ed., 1959, all chapters.
3. "Feedback Control Systems—Analysis, Synthesis and Design," J. C. Gille, M. J. Pelegrin, and P. Decaulne, McGraw-Hill Book Co., Inc., New York, Toronto and London, 1959, all chapters.
4. "AC Voltage or Current Regulator Featuring Closed-Loop Feedback Control," J. L. Brookmire, General Electric Co., Auburn, N. Y., Application Note 200.46.*
5. "Solid State Lighting Control," P. R. Herrick and E. K. Howell, IEEE Convention, March 23, 1965, New York, N. Y. (Copy of paper available from Application Engineering Center, General Electric Co., Auburn, N. Y. 13021.)

*Refer to Chapter 22 for availability and ordering information.

13 LIGHT ACTIVATED THYRISTOR APPLICATIONS

Light and similar forms of radiant energy are increasingly being used in conjunction with solid state devices. The use of light offers a convenient method for sensing the absence or presence of an opaque object and for achieving electrical isolation. These features are useful in the control of power devices and will be discussed in this chapter. Opto-electronic devices also find usage in communications, detection and other applications beyond the scope of this Manual.

13.1 LIGHT ACTIVATED SEMICONDUCTORS

There are many types of devices available for converting radiant energy into electrical information. Such information may be in the form of a variable resistance as in the photo conductors of cadmium sulphide, cadmium selenide and lead sulphide. Other types of devices convert radiant energy into a current and voltage. Devices of this type include selenium, silicon and germanium photovoltaic devices. Junction semiconductor devices are also used as radiant energy sensors. These include photo diodes, phototransistors and light activated PNPN devices.

Radiant energy incident on silicon will create hole-electron pairs. If there is an electric field present, a current will flow. In phototransistors and PNPN devices, this current acts like a base current or gate current to activate the device. This type of light sensor is the only type to be discussed here.

13.1.1 Light Activated SCR (LASCR)

The General Electric Light Activated SCR is similar to the C5 type of SCR except that there is a glass window on top of the can (see Fig. 13.1a). The LASCR may be triggered on by means of a light incident on this window or in the normal manner at the gate. In other respects the operation is the same as the conventional SCR. The construction of the LASCR pellet is similar to that of conventional SCR's (see Fig. 13.1b). The device is capable of handling up to 1.6 amperes of current and of blocking up to 200 volts. The high gain of this PNPN device allows the small amount of power available in the incident light to switch large amounts of power directly.

13.1.2 Light Activated Silicon Controlled Switch (LASCS)

The General Electric Company Light Activated Silicon Controlled Switch is similar to the 3N80 series silicon controlled switch. The principal difference is that the metal can has a lens on top for triggering the LASCS with light. The LASCS performs as a conventional PNPN device. It is constructed, however, using planar transistor technology (see Fig. 13.1c). For greater flexibility in designing circuits, the anode gate lead has been pro-

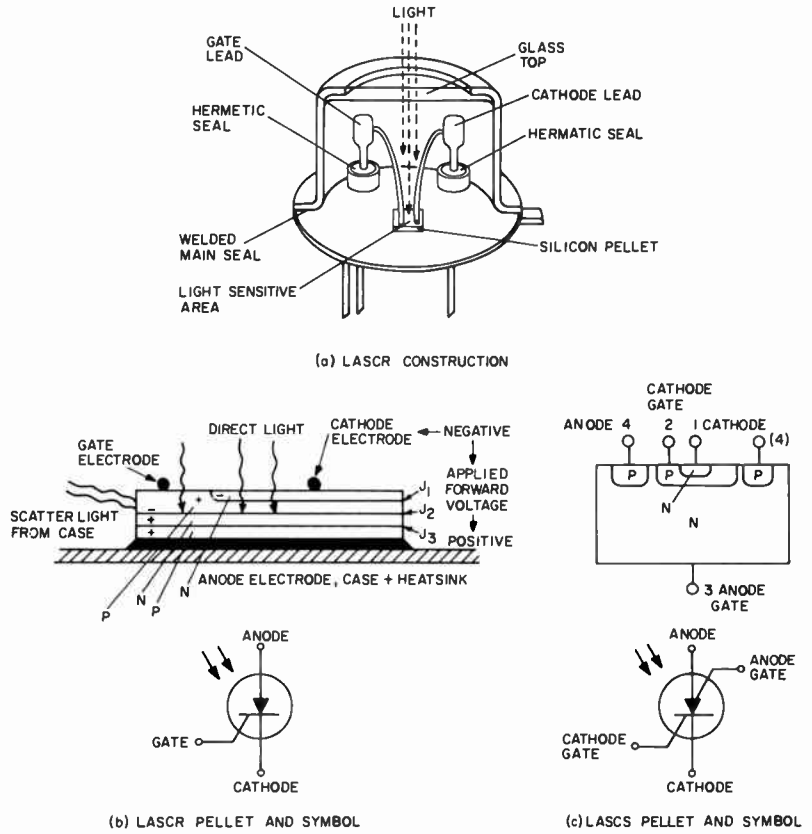


FIGURE 13.1 CONSTRUCTION METHODS

vided, which is not normally available in SCR's. This device offers an economical method for switching up to 175mA and 40 volts with low light levels.

13.1.3 Photo Transistors

The current between the collector and the emitter of a photo transistor can be controlled by the light incident on the device. The effect of the incident light is similar to the effect of base current in the device. The photo transistor differs from an LASCR or an LASCS in that the photo transistor has a proportional response to light whereas the latter two devices operate as switches and can only be triggered completely on with light. The General Electric 14A502 photo transistor is a device similar to the 2N930 transistor with a lens in the top of the transistor can. This device is a high-gain, low-current, planar transistor. It can be used with the base open or with a resistor between base and emitter to adjust the sensitivity of the device.

13.2 SPECIFICATIONS OF LIGHT INTENSITY*

In order to apply these devices, it is necessary to know if a given source at a known distance will cause the desired response in a sensor. This is a function of the characteristics and intensity of the light, the response of sensor to that type of light, and the physical relationship and optical coupling between the source and sensor. The output of most sources is specified in terms of visible light. There is no general relationship between visible light and the effect of the radiation on a sensor.

*See application Note 200.34 for more detailed discussion of this subject and applications of the LASCR.

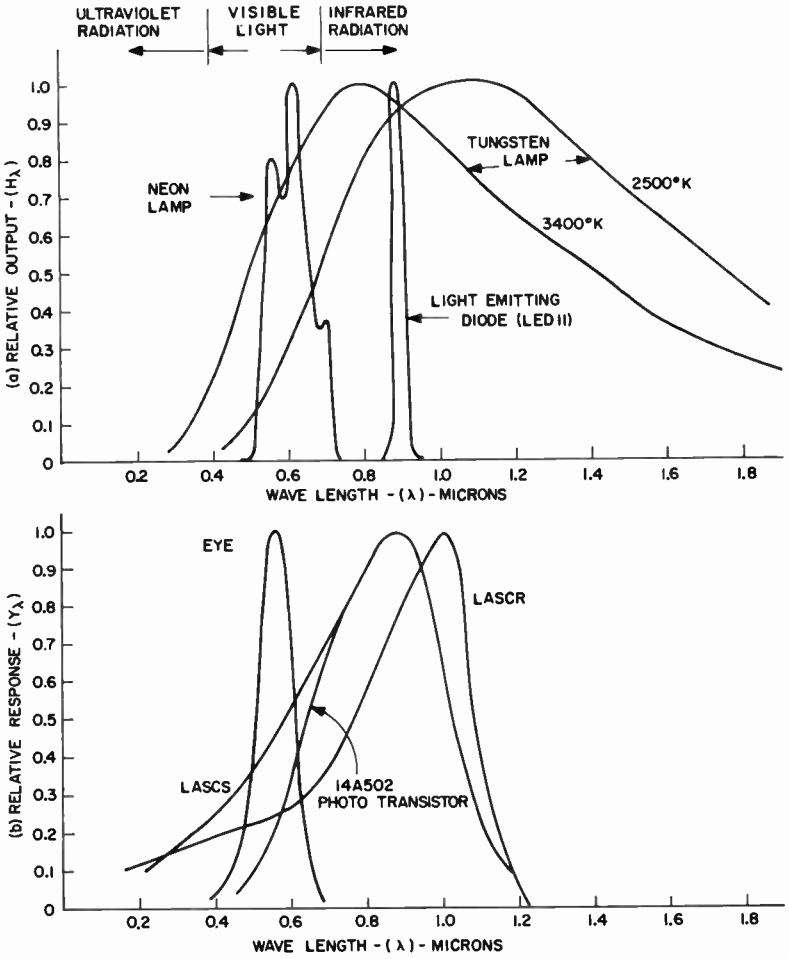


FIGURE 13.2 SPECTRAL DISTRIBUTIONS

13.2.1 Characteristics of Sources and Sensors

Most people learn in high school physics that light is a form of electromagnetic radiation. Electromagnetic radiation is characterized by its frequency (or more commonly in the case of light, wave length), magnitude and direction. Sources vary greatly in the components of frequency in their output. Figure 13.2a shows the spectral distribution of some of the more common types of light sources. The characteristics of the light from a tungsten lamp are a function of the color temperature of that lamp. The color temperature depends upon the type of lamp and upon the applied voltage.

The effect of electromagnetic radiation on a sensor depends upon the wave length of the radiation. The relative effect of radiation of different wave lengths upon the eye and upon several types of silicon semiconductor sensors is shown in Fig. 13.2b. The eye responds to shorter wave lengths than do silicon devices. By comparing Fig. 13.2a and 13.2b, it can be seen that most of the radiation emitted by a tungsten lamp is not visible. Hence, it is important to note that the amount of visible light produced by a source does not reveal how effective this source will be upon a silicon sensor.

13.2.2 Definition of Light Intensity

The intensity of electromagnetic radiation incident on a surface is called irradiance (H). Its dimensions are watts/square centimeter. Since any type of electromagnetic radiation has a spectral distribution, it is also reasonable to define the irradiance per unit of wave length ($H\lambda$). $H\lambda$ is a function of the wave length. By definition then,

$$H = \int H\lambda \, d\lambda$$

$Y\lambda$ is the relative response of a sensor to electromagnetic radiation at any given wave length. The effect of a particular wave length from a light source on a given sensor is the product $H\lambda \, Y\lambda$. The effect of radiation on a sensor is additive so that to determine the total effect of a particular source on a particular sensor, it is necessary to add the $H\lambda \, Y\lambda$ products for all wave lengths of interest. Or,

$$H_E = \int H\lambda \, Y\lambda \, d\lambda$$

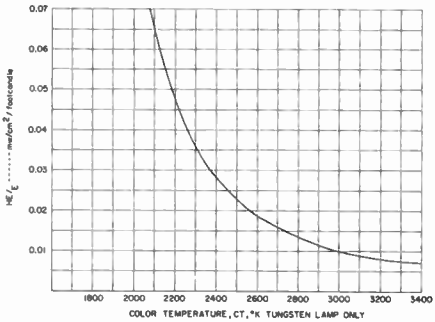


FIGURE 13.3 LASCR EFFECTIVE IRRADIANCE PER FOOTCANDLE FOR A TUNGSTEN LAMP VS COLOR TEMPERATURE

H_E is called effective irradiance.

The definition of light is the effective irradiance on the human eye. The amount of light incident on a surface, or the illuminance (E), is given by the following equation:

$$E = K \int H\lambda \, Y\lambda \, d\lambda$$

$Y\lambda$ in this case is the relative spectral response of the human eye as shown in Fig. 13.2b. K is a proportionality constant depending on the desired units. To get E in the units of foot candles, where H is given in terms of watts per square centimeter, K is equal to 6.35×10^5.

Effective irradiance is used in specifying the LASCR and LASCS. The response of these devices versus wave length is provided on the specification sheet so that effective irradiance can be calculated if the characteristics of the light source is known. The effective irradiance to trigger (H_{ET}) is the minimum amount of effective irradiance that will trigger these devices into conduction.

13.2.3 Design Procedures

For a source with a given spectral distribution, there is a definite relationship between the illuminance (light) and the effective irradiance on a sensor. This ratio has been determined for the combination of a tungsten lamp and an LASCR and is given in Fig. 13.3 as a function of the color temperature of the lamp.

The irradiance on a device varies inversely with the square of the distance between a point source and the device. The devices are most sensitive if the lens in the cap is pointed directly at the source. The relative response for other angles is given on the specification sheets of the devices. As an example, let us calculate the effective irradiance on an LASCR 6 inches from a point source emitting 100 candle power at a 2500°k color temperature. Assume the LASCR is perfectly aligned with the source. At .5 feet the light intensity is

$$E = \frac{100 \text{ candlepower}}{(.5 \text{ ft})^2} = 400 \text{ ft/candles}$$

The conversion factor from E to H_E at 2500°k from Fig. 3 is .023 mW/centimeter squared foot candles. This means that

$$H_E = E \times .023 = 400 \times .023 = 9.2 \text{ mW/cm}^2$$

This amount of light would be adequate to trigger all L9 LASCR's which are specified at a minimum H_{ET} of 4.2mW/centimeter squared.

13.2 4 Effective Irradiance to Trigger

H_{ET} varies depending on how the device is applied in a circuit. Parameters that affect gate trigger current or base current affect H_{ET} in a similar manner. Increases in voltage, temperature or R_{GK} will reduce H_{ET} and also the required irradiance to produce a given current in a phototransistor.

Resistor R_{GK} is almost always used with the LASCR and LASCS. Its purpose is to prevent the devices from being triggered by leakage current and to hold the sensitivity to "rate effect" triggering to a reasonable level. This resistor is particularly important in elevated temperature applications.

Replacing R_{GK} with an inductor (approximately 1 henry) makes the LASCR and LASCS sensitive to rate of rise of light intensity rather than absolute value. After triggering, the holding current of the device will increase as the current in the inductor increases. If the holding current becomes greater than the anode load current, the device turns off. The ringing caused by capacitance in parallel with the inductor will sometimes cause the device to turn back on at a later time. An inductor with a high L/R ratio can reduce turn-off time of the thyristor by maintaining negative gate current during the commutating interval.

Using a capacitor in parallel with R_{GK} makes the device sensitive to the time average of the applied light. This capacitor also causes an increase in turn-off time. A large capacitor (50 mfd) can extend turn-off time to about 10 milliseconds, hence can produce a latching action in 60 Hertz, half-wave circuits.

13.3 APPLICATIONS

13.3.1

The combination of an LASCR or a LASCS with a lamp is close to being the semiconductor analog of an electromechanical relay. This combination offers complete electrical isolation between input and output and an excellent current carrying capability. These are two characteristics that make a relay so useful. In addition, this combination offers the other solid state virtues of long life, microsecond response, freedom from contact bounce and small size. Fig. 13.4 depicts some basic LASCR relay configurations. Fig. 13.4a shows

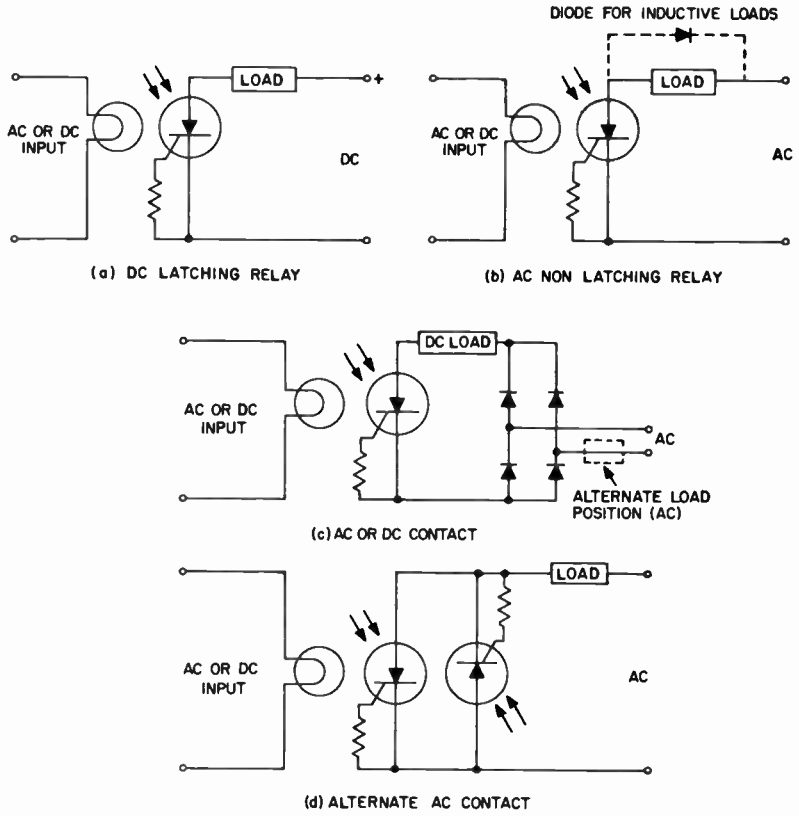


FIGURE 13.4 LASCR RELAY CONFIGURATIONS

the LASCR used with a DC power supply. If the LASCR is off and the lamp is not energized, the load will see what appears to be an open circuit. When the input lamp is energized, the LASCR will switch into conduction so that there is approximately 1 volt drop across it. When the lamp is shut off, the LASCR will remain latched on and must be reset externally.

Fig. 13.4b shows the same circuit with an AC power supply. Since the LASCR will not conduct when its anode is negative with respect to the cathode, the current through the load will be halfwave rectified. The current through the load will flow only when the lamp is energized. The LASCR will reset during the negative half of the AC cycle. The free-wheeling diode shown in this circuit is used with inductive loads, such as relays or solenoids, to provide a smoother load current and reduce chattering.

A nonlatching circuit for driving DC loads is shown in Fig. 13.4c. In this circuit fullwave rectified AC is applied to the LASCR and the load. The LASCR will reset when the voltage applied to the load goes to zero. This circuit is therefore nonlatching. Care should be taken when using this circuit with inductive loads since difficulty in LASCR commutation may be encountered. By placing the load in the alternate position shown, full wave AC power will be applied to it when the lamp is energized. An alternate method of driving an AC load is shown in Fig. 13.4d. The electrical isolation of the optical coupling allows the two LASCR's to be used in the inverse-parallel connection. A possible difficulty with this circuit is that a light level between the sensitivity of the two devices may cause one device to turn on and not the other thereby causing a DC component of current to flow through the load.

13.3.2 Triggering Higher Power SCR's

The power handling ability of any of the preceding circuits may be increased by using the LASCR or LASCS as a gate amplifier to trigger a larger SCR (Fig. 13.5a). Repositioning the light sensitive device with respect to the driven SCR (Fig. 13.5b) converts the circuit into the equivalent of a normally closed relay contact. This is a useful configuration in many monitoring and alarm circuits requiring the load to be energized in the absence of light.

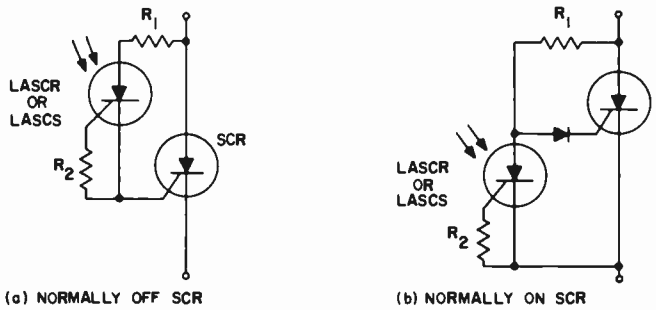


FIGURE 13.5 TRIGGERING HIGH CURRENT SCR'S

If the voltage applied to the load and the LASCR is greater than the voltage rating of the LASCR, an LASCS or an LASCR can be used to trigger a higher voltage SCR. The circuit for doing this is shown in Fig. 13.6. If DC

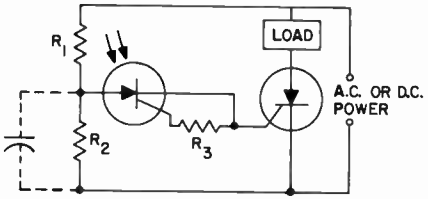


FIGURE 13.6 USE OF LASCR TO TRIGGER HIGHER POWER SCR'S

power is used (or if AC power and a pulsed light), the capacitor indicated will allow larger resistance values to be used for resistors R1 and R2 by furnishing the necessary trigger current pulse for the SCR. If AC power is used, when a steady light is applied to the light sensitive device, a charge cannot build up on the capacitor so that it does not aid triggering. In this case R1 must be small enough to provide adequate trigger current for the SCR and large enough so that the gate current rating of the SCR is not exceeded.

For triggering very high voltage loads, series connections of SCR's are used. The circuit shown in Fig. 13.7 illustrates how the electrical isolation of

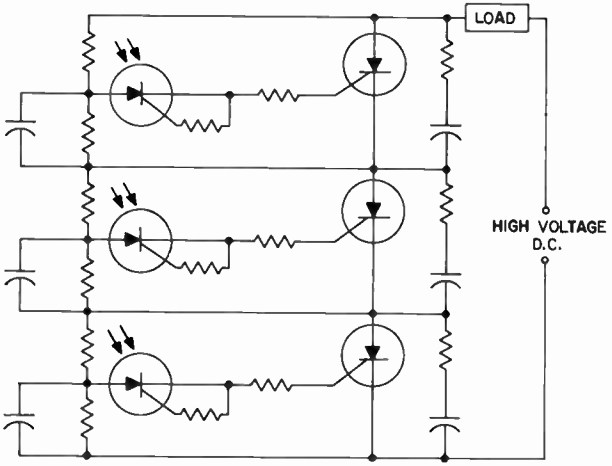
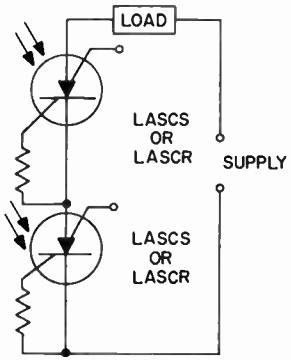


FIGURE 13.7 USE OF LASCR'S TO TRIGGER SERIES CONNECTED SCR'S

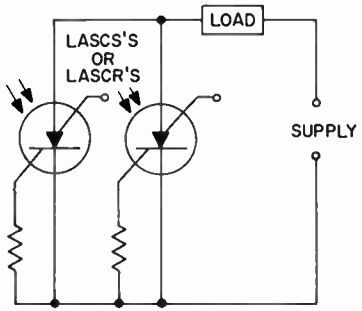
the LASCS or the LASCR can be used to good advantage. This circuit is capable of blocking voltages equal to the sum of the voltage ratings of the three SCR's. See Application Note 200.40 for a detailed explanation.

13.3.3 Logic Circuits

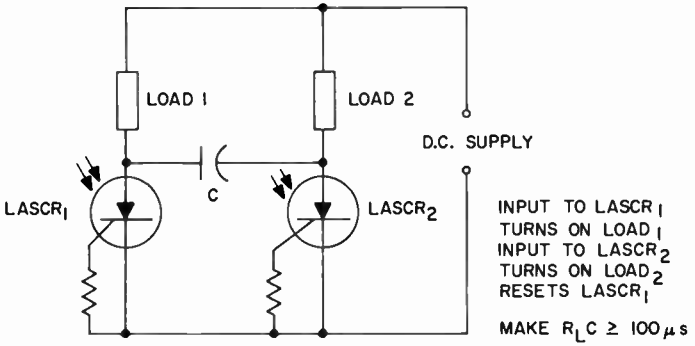
The binary nature of the LASCS and the LASCR makes them ideal elements for use in opto-electronic logic circuitry. Fig. 13.8 illustrates some of the common logic functions that can be implemented with these devices.



(a) "AND" CIRCUIT



(b) "OR" CIRCUIT



(c) FLIP FLOP

FIGURE 13.8 OPTO-ELECTRONIC LOGIC CIRCUITS

13.3.4 Single Shots

The circuits in Fig. 13.9 and 13.10 are light triggered single shots. In Fig. 13.9, the unijunction transistor triggers approximately .6 sec after a pulse of light turns on the LASCR. If the pulse of light has ended, the LASCR will turn off. If the light is still on the unijunction will operate as a relaxation oscillator. It will turn the LASCR off the first time it fires after the light is removed. When the LASCR is off, the high resistance in series with the capacitor prevents the unijunction from oscillating.

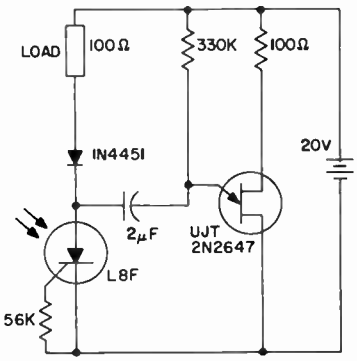


FIGURE 13.9 SELF CLEANING SINGLE SHOT

In the circuit shown in Fig. 13.10, with no light applied to the LASCR, the 3N81 silicon controlled switch is in the conducting state. When a short pulse of light is applied to the LASCR, it is turned on and the SCS is commutated off through the one microfarad capacitor. At the same time, the voltage at the junction of the four microfarad capacitor and the 220k resistor is pulled negative. This voltage gradually goes positive due to the charging action of the 220k resistor. After approximately .6 of a second the SCS is turned on. This in turn commutates off the LASCR.

This circuit is useful for detecting the presence of pulses of light that last longer than some minimum time. If the pulses last longer than 0.6 sec, the LASCR will remain in the conducting state.

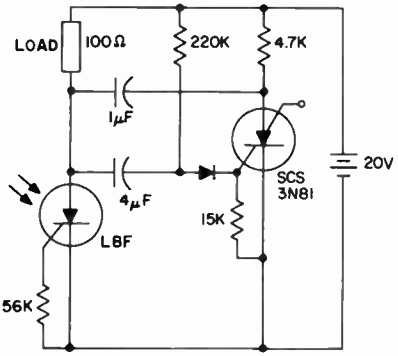


FIGURE 13.10 SINGLE SHOT AND PULSE WIDTH SENSOR

13.3.5 Light Interruption Detector

When the light incident on the LASCS in Fig. 13.11 is interrupted, this allows the voltage at the anode to the 2N4990 unilateral switch to go positive on the next positive cycle of the power and trigger the switch and the C5 SCR when the switching voltage of the unilateral switch is reached. This will cause the load to be energized for as long as light is not incident on the LASCS.

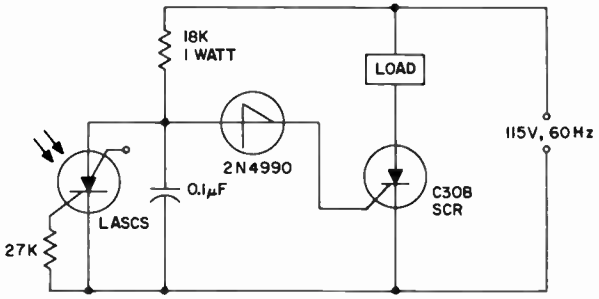
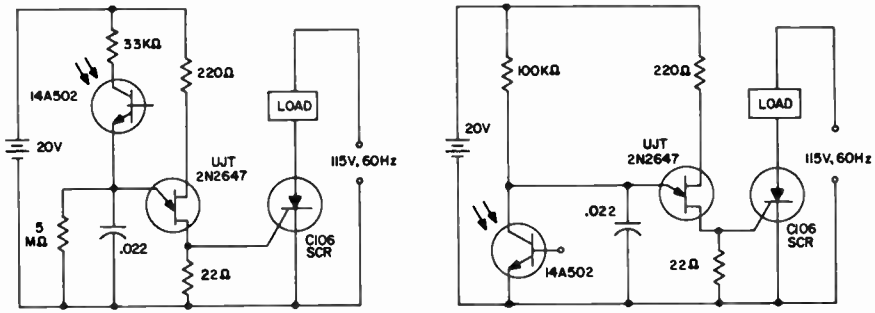


FIGURE 13.11 LIGHT INTERRUPTION DETECTOR

The unilateral switch allows higher power SCR's with their higher gate triggering currents to be used while holding the power in the 18kΩ resistor to a reasonable value. The charge in the capacitor provides a pulse of current adequate to trigger high current SCR's.



(a) LIGHT PRESENCE DETECTOR

(b) LIGHT ABSENCE DETECTOR

FIGURE 13.12 HIGHER SENSITIVITY CIRCUITS

13.3.6 Higher Sensitivity Light Detectors

The 14A502 phototransistor and a unijunction transistor in combination allow much lower levels of light to be detected. Fig. 13.12 shows how this can be done. In Fig. 13.12a when the phototransistor has light incident upon it, the unijunction will oscillate as a relaxation oscillator. Since its frequency is considerably higher than 60 Hz, the C106 SCR is turned on early in the positive half of every cycle. The circuit in Fig. 13.12b energizes the load when light is removed from the phototransistor. In this circuit when the phototransistor is dark, the unijunction operates as a relaxation oscillator and energizes the load on positive half cycles.

13.3.7 "Slave" Electronic Flash

There is a need, in the photographic industry, for a fast photo-sensitive switch capable of triggering the "slave" flash units used extensively in multiple-light-source high speed photography. Fig. 21 shows how an industry-standard flashgun circuit can be modified with an LASCR to serve as a fast acting slave unit. With switch S_1 closed, capacitor C_1 charges to 300 volts through R_1, and capacitor C_2, charges to approximately 200 volts through R_2 and R_3. When the master flashgun fires (triggered by the flash contacts on the camera) its light output triggers $LASCR_1$, which then discharges capacitor C_2 into the primary winding of transformer T_1. Its secondary puts out a high voltage pulse to trigger the flashtube. The flashtube discharges capacitor C_1, while the resonant action between C_2 and T_1 reverse biases $LASCR_1$ for positive turn-off. With the intense instantaneous light energy available from present-day electronic flash units, the speed of response of the LASCR is easily in the low microsecond region, leading to perfect synchronization between master and slave.

High levels of ambient light can also trigger the LASCR when a resistor is used between gate and cathode. Although this resistance could be made

adjustable to compensate for ambient light, the best solution is to use an inductance (at least one henry) which will appear as a low impedance to ambient light and as a very high impedance to a flash.

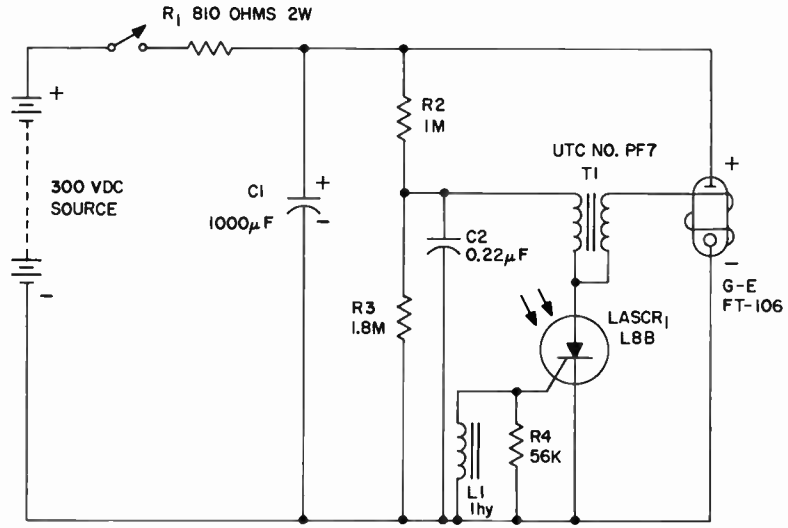
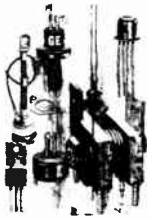


FIGURE 13.13 SLAVE FLASH

14 PROTECTING THE THYRISTOR AGAINST OVERLOADS AND FAULTS



Satisfactory operation of thyristor circuits and the equipment in which they operate often depends heavily on the ability of the system to survive unusual over-current conditions. One obvious answer to this requirement, not usually an economical one, although one that is becoming more reasonable with the decreasing costs of semiconductors, is to design the system to withstand the worst fault currents on a steady-state basis. This requires semiconductors and associated components that are rated many times the normal load requirements. Where this approach is not possible because of economics or other factors, an adequate overcurrent protective system is usually used.

14.1 WHY PROTECTION?

The functions of an overcurrent protective system are any or all of the following:

1. To limit the duration of overloads and the frequency of application of overloads.
2. To limit the duration and magnitude of short circuits.
3. To limit the duration and magnitude of fault currents due to shorted semiconductor cells.[1]

The objective of these functions is to safeguard not only semiconductor components but also the associated electrical devices and buswork in the equipment from excessive heating and magnetic stresses. The trend toward high capacity systems feeding electronic converter equipment often results in extremely high available fault currents. Since both heating and magnetic stresses in linear circuit elements respond to the square of the current, the importance of adequate protection in "stiff" systems is self-evident.

Elaborating on function No. 3 above, thyristors as well as diode rectifiers may fail by shorting rather than by opening. In many circuits such a device fault results in a direct short from line to line through the low forward resistance of the good devices in adjacent legs during at least part of the

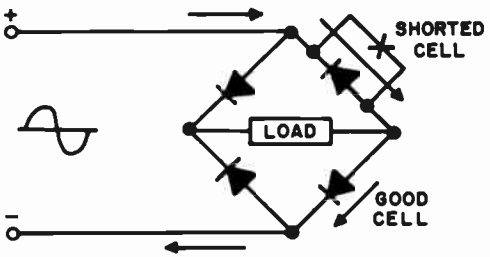


FIGURE 14.1 ARROWS INDICATE FLOW OF FAULT CURRENT THROUGH GOOD DEVICE AFTER ADJACENT LEG HAS SHORTED. LOAD RESISTANCE DOES NOT LIMIT CURRENT.

cycle. See Figure 14.1 where the diode symbol is used to represent both SCR's and diodes for the sake of generalization. Under these circumstances, a protective system functions either to shut the entire supply down, or to isolate the shorted device in order to permit continuity of operation. This will be discussed at greater length later.

It is difficult to make broad recommendations for overcurrent protection since the concept of satisfactory operation means different levels of reliability in different applications. The selection of a protective system should be based on such individual factors as:

1. The degree of system reliability expected
2. The need or lack of need for continuity of operation if a semiconductor fails.
3. Whether or not good semiconductor cells are expendable in the event of a fault.
4. The possibility of load faults.
5. The magnitude and rate of rise of available fault current.

Depending upon the application, these various factors will carry more or less weight. As the investment in semiconductors increases for a specific piece of equipment, or as an increasing number of components in a circuit increases the possibility of a single failure, or as continuity of operation becomes more essential, more elaborate protective systems are justified. On the other hand, in a low-cost circuit where continuity of operation is not absolutely essential, economy type semiconductors may be considered expendable and a branch circuit fuse in the AC line may be all that is needed, or justified, for isolation of the circuit on faults, allowing semiconductor components to fail during the interval until the protection functions. In other designs, the most practical and economical solution may lie in overdesigning the current carrying capability of the semiconductors so that conventional fuses or circuit breakers will protect the semiconductors against such faults.

It is therefore reasonable that each circuit designer rather than the semiconductor component manufacturer decide precisely what level of protection is required for a specified circuit. Once the specific requirements are determined the component manufacturer can recommend means of attaining these specific objectives. This chapter is prepared to assist the circuit designer in determining his protection requirements, and then to select satisfactory means of meeting these requirements.

14.2 OVERCURRENT PROTECTIVE ELEMENTS

The main protective elements can be divided into two general classes. One class consists of those devices which protect by interrupting or preventing current flow, and the other class consists of those elements which limit the magnitude or rate of rise of current flow by virtue of their impedance.

Among the elements in the first class are:

1. The AC circuit breaker or fuse which disconnects the entire circuit from the supply.
2. The cell fuse or breaker which isolates faulted semiconductor cells.
3. Load breakers or fuses which isolate load faults from the equipment or a faulted cell from DC feedback from the load or parallel converter equipments.

4. Current limiting fuses and SCR circuit breakers.
5. Gate blocking of SCR's to interrupt overcurrent.

(The internal fusing characteristics of commercial semiconductors are generally not predictable nor reliable enough to be used as protective elements in practical circuits, even though internal leads may burn open under severe fault currents before regular protective elements function. Long before this however, the associated junction will have been permanently damaged to a shorted condition.)

Among the elements of the second class which limit magnitude or rate-of-rise of current are:

1. Source impedance.
2. Transformer impedance.
3. Inductance and resistance of the load circuit.

Throughout this discussion it is well to bear in mind that circuit interrupting devices that are tripped by magnetic circuits, such as solenoids in fast-acting breakers and interrupting devices that are tripped by thermal means, such as fuses or breakers with thermal overloads, all react to the RMS value of the current. The semiconductor itself reacts essentially to heating, but having a non-linear resistance, it heats proportional to a current value somewhere between the RMS and average value. The considerable difference that may occur between these respective values of current in rectifier circuits is of particular importance in co-ordinating protective elements with one another and with the semiconductors.

14.3 CO-ORDINATION OF PROTECTIVE ELEMENTS

Depending upon their complexity and the degree of protection desired, converter circuits include one or more of the various interrupting devices listed above. Functioning of these devices must be co-ordinated with the semiconductor and with each other so that the over-all protection objectives are met. Fuses or breakers must interrupt fault currents before semiconductor cells are destroyed. In isolating defective semiconductors from the rest of the equipment, only the fuse or breaker in series with a defective semiconductor cell should open. Other fuses and breakers in the circuit should remain unaffected. On the other hand, when a load fault occurs, main breakers or fuses should function before any of the semiconductor cell-isolating fuses or breakers function. This fault discriminating action is often referred to as selectivity. In addition, the voltage surges developed across semiconductors during operation of protective devices should not exceed the transient reverse voltage rating of these devices. More complex protective systems require meeting additional co-ordinating criteria. The example of a protection system and its associated co-ordination chart described later in this discussion illustrates some of the basic principles of co-ordination for both overloads and stiff short circuits.

The magnitude and waveshape of fault and overload currents vary with the circuit configuration, the type of fault, and the size and location of circuit impedances. Fault currents under various conditions can generally be estimated by analytical means. References 1, 2, and 3 show analytical methods for calculating fault currents for generally encountered rectifier circuits.

For overloads on rectifier or inverter circuits where the current is limited to a value which the semiconductors can withstand for roughly 50 milliseconds, conventional circuit interrupting devices like circuit breakers and fuses can usually be used satisfactorily for protection. This type of overload can be expected where a sizeable filter choke in the load or a "weak" line limits the magnitude or rate of rise of current significantly or where semiconductor components are substantially oversized. By placing the circuit breaker or fuse in the line ahead of the semiconductors, the protective device can be designed to isolate the entire circuit from the supply source whenever the line current exceeds a predetermined level which approaches the maximum rating of the semiconductors for that duration of fault.

For time intervals greater than approximately 0.001 second after application of a repetitive overload, the thyristor rating for co-ordination purposes is determined by the methods discussed in Section 3.6. If the overload being considered is of a type that is expected only rarely (no more than 100 times in the life of the equipment), additional semiconductor rating for overload intervals of one second and less can be secured by use of the surge curve and I^2t rating for the specific device being considered.

The surge characteristic is expressed as the peak value of a half-sine wave of current versus the number of cycles that the semiconductor can handle this surge concurrent with its maximum voltage, current, and junction temperature ratings. In circuits that do not impose a half-sine wave of fault current on the semiconductors, the surge curve can be converted into current values that represent the particular waveshape being encountered. The surge curve for the semiconductor can be converted to different waveshapes or different frequencies in an approximate, yet conservative, manner for this time range by maintaining equivalent RMS values of current for a specific time interval. For example, the peak half-sine wave surge current rating of the C35 SCR for 10 cycles on a 60 Hz base is shown on the spec sheet to be 88 amperes. For a half-sine waveshape, the RMS value of current over the complete cycle is one-half the peak value, or 44 amperes. To convert this to average cell current in a three-phase bridge feeding an inductive load (120-degree conduction angle), divide this RMS value by $\sqrt{3}$. ($44 \div \sqrt{3} = 25.4$ amps). To determine the total load current rating for a bridge using this cell, multiply the average cell current by 3. ($25.4 \times 3 = 76.2$ amps).

14.4 PROTECTING CIRCUITS OPERATING ON STIFF POWER SYSTEMS

Conventional circuit breakers and fuses can be designed to provide adequate protection when fault currents are limited by circuit impedance to values within the semiconductor ratings up to the time when these protective devices can function. However, circuits requiring good voltage regulation or high efficiency will usually not tolerate high enough values of series impedance to limit fault currents to such low values unless substantially oversized semiconductors are used. When a fault occurs in a circuit without current limiting impedance, current will develop in a shape similar to the dashed line in Figure 14.2. Its rate of rise is limited by the inductance inherent in even the stiffest practical systems. If the peak available current substantially exceeds the semiconductor ratings, and if it is permitted to

flow in the circuit, the semiconductor would be destroyed before the current reaches this first peak. Conventional circuit breakers and fuses will not function quickly enough. Instead, so-called "current limiting" fuses which melt extremely fast at high levels of current are used. Alternately, "electronic circuit breakers" of the type discussed in Section 8.8 can be designed for this purpose.

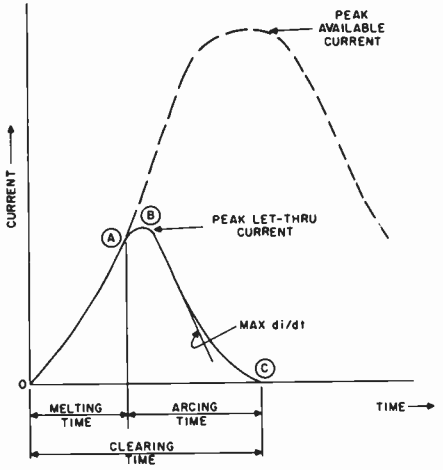


FIGURE 14.2 LIMITING ACTION OF CURRENT LIMITING FUSE

The action of a typical current limiting fuse is indicated in Figure 14.2. Melting of the fuse occurs at point A. Depending on the fuse design and the circuit, the current may continue to rise somewhat further to point B, the peak let-thru current. Beyond this point the impedance of the arcing fuse forces the fault current down to zero at some point C. A satisfactory current limiting fuse will have an arcing time approximately equal to the melting time. If the fuse interrupts fault current too quickly, the high rate of change of current (di/dt) will induce levels of transient voltage in the circuit inductances that can destroy semiconductors. For this same reason, it is not wise to use any higher voltage fuse rating than is required by the supply voltage. Surplus voltage rating of a fuse over the circuit voltage can lead to unnecessarily abrupt arc-quenching with resultant destructive voltage transients. However, the current interrupting rating of the fuse should be ample for the maximum available current to be expected.

Since the buildup of current is so rapid and since the current amplitude is so high in a circuit with low impedance, additional phases and circuit legs usually help very little in increasing the fault current capacity of a circuit because permanent damage may be done before commutation to another leg can occur. For conservative design, all fault current on stiff faults should be considered to flow through only one leg, dividing only between the parallel cells in that particular leg.

Both current limiting fuses[4,5] and semiconductors with uniform current distribution across their junctions[6,7] exhibit ability to withstand essentially constant $\int i^2 dt$ below approximately one cycle (i=instantaneous current, t= time). This fortunate circumstance provides a simple tool for co-ordinating

current limiting fuses and semiconductors in this difficult-to-define area below one cycle. The necessity of calculating fault currents in this region for co-ordination purposes is thereby largely eliminated. If the interrupting or clearing I^2t rating of a fuse is lower than the I^2t rating of the semiconductor in series with it, the fuse will interrupt fault current before the semiconductor fails regardless of current magnitude or rate of rise in the subcycle region.

Several fuse manufacturers now publish maximum clearing I^2t data on their current limiting fuses. However, where manufacturers do not publish I^2t ratings for their current limiting fuses, the clearing I^2t to melting can be approximated from the melting time-current characteristics of the fuse. Figure 14.3 illustrates the characteristics of a line of current limiting fuses manufactured by the Chase-Shawmut Company, Newburyport, Massachusetts. The melting I^2t of the 30-ampere fuse, for example, can be approximated by squaring the current value at 0.01 second and multiplying it by the time ($90^2 \times .01$ second $= 81$ amp^2-seconds). If the fuse co-ordination is critical in a particular application, the manufacturing tolerance should be factored into the current or time values used to determine melting I^2t.

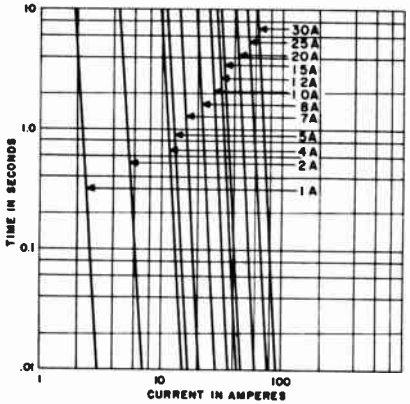


FIGURE 14.3 FORM 101 AMP-TRAP CHARACTERISTIC CURVES, MELTING TIME VS. CURRENT, 1 TO 30 AMPERE CARTRIDGE SIZE, 250 VOLT—TYPE 1.

The arcing I^2t of satisfactory current limiting fuses will not exceed twice the melting I^2t, and total clearing I^2t will therefore not exceed three times the melting I^2t. In the above example, maximum clearing I^2t will not exceed $3 \times 81 = 243$ ampere^2-seconds for the 30-ampere Form 101 Amp-Trap fuse. It is interesting to note that Chase-Shawmut specifies 240 ampere^2-seconds for this fuse. In practice, this type of approximation should only be used when specific I^2t data is not available from the fuse manufacturer.

The minimum I^2t rating of the semiconductor is specified by the semiconductor manufacturer. Depending on the semiconductor design, the I^2t rating may vary with initial junction temperature and may depend on whether or not reverse voltage is impressed on the semiconductor following the current surge.

Several companies manufacture current limiting fuses in various voltage, current and speed ratings. Their literature indicates the following ratings:

FUSE MANUFACTURER	CURRENT LIMITING FUSE RATINGS (RMS VALUES UNLESS OTHERWISE INDICATED)	
General Electric Co. Switchgear Dept. Philadelphia, Pa.	250 Volts DC & AC	6-200 Amps.
	250 Volts AC	300-600 Amps.
	600 Volts DC & AC	6-200 Amps.
	600 Volts AC	3-4000 Amps.
	850 Volts AC	400-500 Amps.
	1000 Volts AC	600 Amps.
	1500 Volts AC	600-800 Amps.
	2000 Volts AC	300 Amps.
	3000 Volts AC	300 Amps.
Bussmann Mfg. Division McGraw-Edison Company St. Louis 7, Mo.	65 Volts	12-30 Amps.
	130 Volts	1-1000 Amps.
	250 Volts	1-800 Amps.
	600 Volts	1-800 Amps.
	850 Volts	100-400 Amps.
Chase-Shawmut Co. 347 Merrimac St. Newburyport, Mass.	AMP-TRAP FUSES, FORM 101	
	130 Volts	1-10,000 Amps.
	250 Volts	1-5,000 Amps.
	300 Volts	1-30 Amps.
	500 Volts	40-400 Amps.
	600 Volts	1-2000 Amps.
	1000 Volts	50-600 Amps.
	1500 Volts	30-600 Amps.
English Electric Corp. One Park Ave. New York, N. Y. 10016	HRC FUSES	
	150 PRVAC-115 VDC	25-700 Amps.
	300 PRVAC-200 VDC	25-600 Amps.
	350 PRVAC-120 VDC	0.25-20 Amps.
	450 PRVAC-200 VDC	25-500 Amps.
	1000 PRVAC-350 VDC	5-500 Amps.
	2000 PRVAC	25-250 Amps.

For data on the melting time-current and I^2t characteristics of these fuses, the designer should refer to the curves and data published by the fuse manufacturer.

When a current limiting fuse in the primary of a transformer must be coordinated with a semiconductor cell in the secondary, their respective I^2t's can be compared by the following equation:

$$I^2t_{fuse} \leqq \left(\frac{V_{sec.}}{V_{pri.}}\right)^2 \times I^2t_{cell}$$

where $V_{sec.}$ = rated secondary voltage of transformer.
$V_{pri.}$ = rated primary voltage of transformer.

In similar manner, the clearing I^2t of a fuse being fed by a group of N parallel semiconductor cells should be no greater than N^2 times the I^2t rating

of the individual cells if all the parallel cells share current equally. If the cells are derated for parallel operation to compensate for inequalities in current sharing, the relationship between clearing I^2t of the fuse and the I^2t rating of the individual cell can be expressed as follows:

$$I^2t_f \leqq I^2t_c\,[N(1 - S) + S]^2$$

where I^2t_f = clearing I^2t of fuse
I^2t_c = I^2t rating of semiconductor cell
N = number of parallel rectifier cells
S = derating factor for parallel cell operation (usually 0.20)

14.5 INTERRUPTED SERVICE TYPE OF PROTECTION

By inserting the protective device in the AC lines feeding a semiconductor AC to DC converter, protection can be provided both against DC faults and semiconductor device faults if there is no possibility of DC feed into faults of the semiconductor devices themselves. DC feed into cell faults will occur in single-way circuits when other power sources feed the same DC bus or when the load consists of CEMF types of loads such as motors, capacitors, or batteries. The following is an example of this type of AC line protection in a circuit without current limiting impedance. Upon functioning of the protective system, the circuit is interrupted and shut down.

14.6 EXAMPLE OF FAULT PROTECTION (NO CURRENT-LIMITING IMPEDANCE)

Application: —120 V RMS AC supply, 60 Hz
—Single-phase bridge employing two C35H SCR's for phase control in two legs and two 1N2156 diode rectifiers in the other two legs. See Figure 14.4.

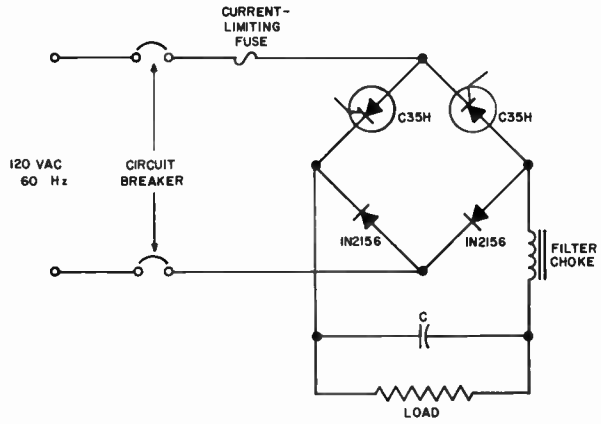


FIGURE 14.4 CIRCUIT FOR EXAMPLE OF FAULT PROTECTION

—Maximum continuous load current = 12 amperes.
—Choke input filter.
—Line impedance negligible. Peak available fault current in excess of 1000 amperes.
—Maximum ambient = 55°C free convection. Each semiconductor mounted to a 4″ x 4″ painted copper fin 1/16″ thick.

Requirements for Protective System:

—Protection system must be capable of protecting SCR's and diodes against overloads, DC shorts, and shorting of individual semiconductors. System can be shut down when any of these faults occurs.

Solution: —Since the current rating of the 1N2156 is higher than the C35 both at steady-state and under overload, the protection, if properly coordinated with C35, will be ample for protecting the 1N2156 also.

Using the data for a C35 on a 4″ x 4″ fin given in Figure 3.4 and the load current rating equation in Figure 3.7 (e) which applies for the continuous square wave of current experienced in a single-phase circuit with inductive load,

$$P_0 = \frac{125 - 55}{\frac{0.0083}{0.0167} \times 5.1 + \left(1 - \frac{0.0083}{0.0167}\right) 0.4 - 0.35 + 0.2}$$

= 27 watts maximum peak heating allowable per SCR on steady-state basis

From the specifications for the C35, this level of heating will be developed by 18 amperes peak or 9 amperes average load current at 180 degree conduction angle with a rectangular current waveshape. Under inductive load conditions, the maximum steady-state RMS rating of the complete circuit is equal to the peak rating of each SCR = 18 amperes.

Assuming that faults and overloads will be superimposed on the steady-state equipment rating of 12 amperes, the semiconductor overload rating can be calculated from Figure 3.7 (f).

$$P_{OL} = \frac{T_J - T_A - P_{(1)}\theta}{\theta_{(t)}} + P_{(1)}$$

For example, for 10 seconds the SCR can dissipate the following power without its junction exceeding 125°C:

$$P_{OL} = \frac{125 - 55 - 8 \times 5.1}{2.2} + 8 = 21.3 \text{ watts/cell}$$

Average current rating per cell =13.3 amps (from specification sheet).

Rated bridge output current = 2 × 13.3 = 26.6 amps RMS.

This point and others calculated by the same means are plotted on the coordination chart of Figure 14.5. Overload ratings achieved by this technique limit junction temperature to 125°C.

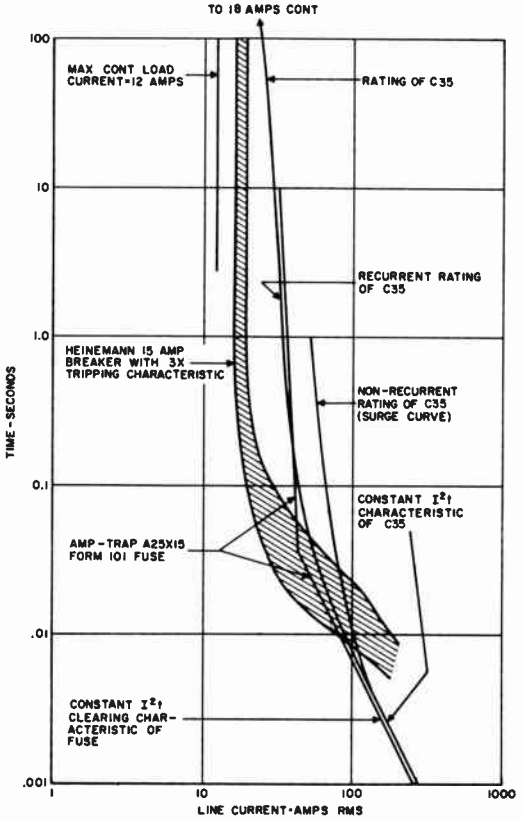


FIGURE 14.5 CO-ORDINATION CURVE FOR EXAMPLE OF FAULT PROTECTION OF SCR's.

For non-recurrent types of overload as typified by accidental short circuits and failure of filter capacitors, the SCR is able to withstand considerably higher overloading as specified in the I^2t and surge current ratings. A typical point of this kind can be calculated as follows. At 0.1 second, a time which is equivalent to 6 cycles on the surge curve, the peak surge current rating of the C35 is 92 amperes. The RMS bridge rating is $92 \div \sqrt{2} = 65$ amperes. This curve blends into ratings determined from the I^2t rating below approximately 50 milliseconds. The I^2t rating of the C35 is 75 amps^2-sec. At .001 second, the current rating of the SCR is

$$\sqrt{75 \text{ amps}^2\text{-sec.}/.001 \text{ sec.}} = 274 \text{ amps.}$$

Below ½ cycle, the rating of a single SCR and the rating of the bridge are identical. Thus, at .001 second, the bridge is rated 274 amps RMS also.

To afford protection against short circuits of the load and shorted semiconductors in this type of circuit, a current limiting fuse is required. The

fuse must carry the steady-state line current without melting. An Amp-Trap A25X15 Form 101 fuse rated at 15 amperes continuous current should handle the 12 amperes RMS steady-state line current satisfactorily. Melting characteristics of this fuse are shown in Figure 14.3, and are plotted directly on the co-ordination curve of Figure 14.5 since both curves are in RMS terms. Below 0.01 second, the fuse clearing characteristic can be determined on the basis of the fuse manufacturer's clearing I^2t data or on approximations from the melting time vs. current curves as explained in Section 14.4. Since the manufacturer of the A25X15 fuse specifies a maximum clearing I^2t of 60 amp^2-seconds for this fuse, the data is translated into clearing current vs time data for the co-ordination curve. For instance, at 0.001 second the maximum RMS current that this fuse will permit to flow is

$$\sqrt{60 \text{ amps}^2\text{-seconds}/.001 \text{ second}} = 245 \text{ amps.}$$

This data for the fuse below 0.01 second is plotted in Figure 14.5 and made very conservative by extending the straight line of the constant I^2t clearing characteristic up to its intersection with the published melting current vs time at a time substantially greater than 0.01 second.

From the co-ordination curve, it can be seen that the current limiting fuse in the line will protect the SCR's for any type of fault of sufficient magnitude to blow the fuse in 0.2 second or less since the fuse rating is to the left of the cell rating.

The curves also indicate that, for times longer than 0.2 second, the SCR's are likely to fail before the fuse blows. In order to provide protection for the SCR's for these lower current faults, a circuit breaker is used. The co-ordination chart shows the tripping characteristic of a Heinemann 15-ampere molded case circuit breaker using the Type 3X time-delay characteristic.

The co-ordination curve reveals that the circuit breaker will trip on any faults under 42 amperes RMS, but above 18 amperes RMS. Between 42 amperes and 85 amperes, the fuse and/or the breaker will function. Above 85 amperes, the fuse only should blow. Under no circumstances should good SCR's fail.

14.7 NON-INTERRUPTED SERVICE UPON FAILURE OF SEMICONDUCTOR

In the foregoing discussion and example, the semiconductors are protected against overloads and short circuits of the output and also against the fault currents that occur if another semiconductor in the circuit should short. Protection is afforded by disconnecting the entire circuit from its supply voltage.

In some types of service such as high reliability military systems and continuous industrial processes, a service interruption due to a semiconductor failure cannot be tolerated regardless of how remote this possibility may be. To maintain service under these conditions requires redundancy of semiconductors and a means of disconnecting faulty cells whenever failure of a semiconductor occurs. It has been observed that, when failures of SCR's have occurred, they could be classified into three main categories:

1. Loss of reverse blocking ability. In rectifier circuits this generally causes a high fault current to flow.
2. Loss of forward blocking ability. In a rectifier circuit, this will gen-

erally result in loss of control of output voltage, the SCR remaining in the forward "on" state.

3. Failure to fire or switch into the forward conduction state. This will also result in loss of control of output voltage since the SCR will remain in the "off" state.

(Conditions 1 and 2 may be combined in a short-circuited device.)

Figures 14.6 and 14.7 suggest two of several possible methods of detecting and isolating defective SCR's from the circuit without interrupting the flow of controlled power to the load. Figure 14.6 illustrates a single-phase centertap phase-controlled power supply in which the SCR's in each leg of the circuit are grouped into pairs of parallel-matched cells. A low value of resistance R is connected in series with each SCR. The value of R is selected to limit fault current through good SCR's if one SCR loses its reverse blocking ability. The contacts of an isolating circuit breaker are connected in series with each pair of SCR's. The trip coil of each breaker or the coil of a pilot relay is connected across the bridge formed by the pair of

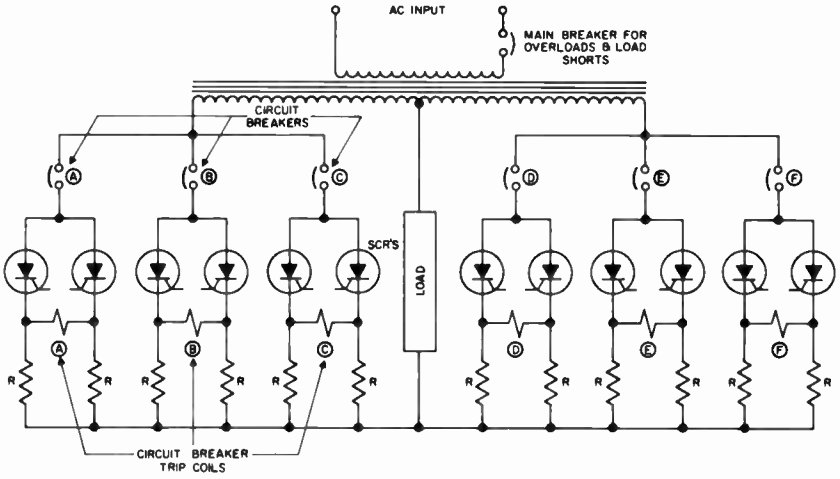


FIGURE 14.6 PARALLEL SCR PAIRS FOR NON-INTERRUPTED SERVICE

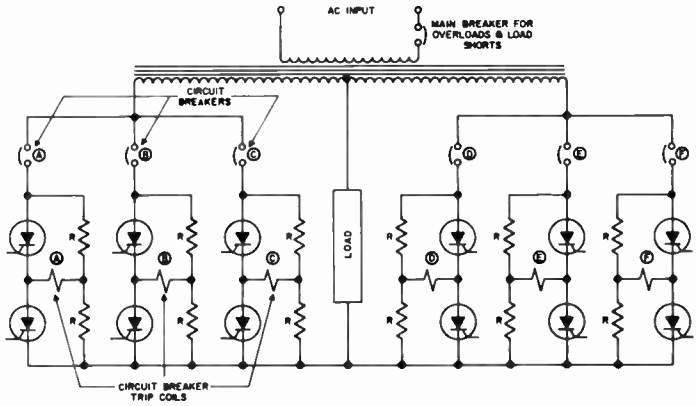


FIGURE 14.7 SERIES SCR PAIRS FOR NON-INTERRUPTED SERVICE

SCR's and their respective series resistors. When both SCR's of a pair are functioning properly and therefore identically, the instantaneous currents through the SCR's and their series resistors are essentially equal and therefore no current flows through the circuit breaker trip coil. If either SCR in a pair fails in any one or more of the three modes enumerated above, unequal currents will flow for at least part of each cycle through the SCR's. Current will flow through the trip coil associated with that SCR pair, tripping the series circuit breaker and isolating the pair from the main circuit. As long as the remaining SCR's in that leg of the circuit are capable of handling the full load current, the circuit will be capable of continuing operation indefinitely. The circuit breakers can be used to actuate an alarm or annunciator scheme to warn the equipment operator of the failure so that he can replace the faulty SCR during a scheduled maintenance shutdown of the equipment.

The circuit shown in Figure 14.7 is more economical than Figure 14.6 for circuits requiring high output voltages rather than high currents. In this circuit the SCR's are grouped in series-connected pairs for the purpose of handling higher voltages. A resistor R is connected in shunt with each SCR to assist in voltage sharing and to provide in conjunction with the pair of SCR's a bridge across which to connect the circuit breaker trip coil. When both SCR's are functioning properly, only the difference in leakage currents between the two SCR's flows through the trip coil. When either SCR in a pair malfunctions for one of the reasons cited earlier, a substantial current will flow for at least part of the cycle through the trip coil, thus opening the circuit breaker and isolating that pair of SCR's from the circuit. In order that the trip coil will reliably discriminate between the normal leakage balancing current of the SCR's and the unbalance current resulting from a faulty SCR, it may be necessary to reduce the value of each resistor R somewhat below the value otherwise adequate for forcing voltage sharing between the SCR's.

Proper functioning of the type of protection shown in Figures 14.6 and 14.7 requires that:

1. None of the circuit breakers in series with the SCR's should trip on DC overloads or faults. Separate protection in the AC or DC lines should disconnect the load from the supply voltage for this type of fault.

2. Adequate SCR and circuit breaker capacity should be provided to handle the maximum load current with one of the parallel paths removed from the circuit by operation of a breaker.
3. In isolating a pair of SCR's, the circuit breaker must cut off the current at a slow enough rate so that induced voltage (L di/dt) does not exceed the transient voltage rating of the SCR's in parallel with that pair. If they occur, excessive transient peaks may be reduced to tolerable levels by means of transient suppression techniques (Chapter 15).

In some applications it may suffice to provide protection only against the possibility of SCR's and rectifier diodes failing by losing their reverse voltage blocking ability (shorting). In this event, the protective scheme can use current limiting fuses in simple parallel paths in a manner identical to that used for protecting diode rectifier circuits.[12] This type of protection presupposes that satisfactory operation can take place at least on a temporary basis with SCR's still in the circuit that have failed either by failure mode 2 or 3 above.

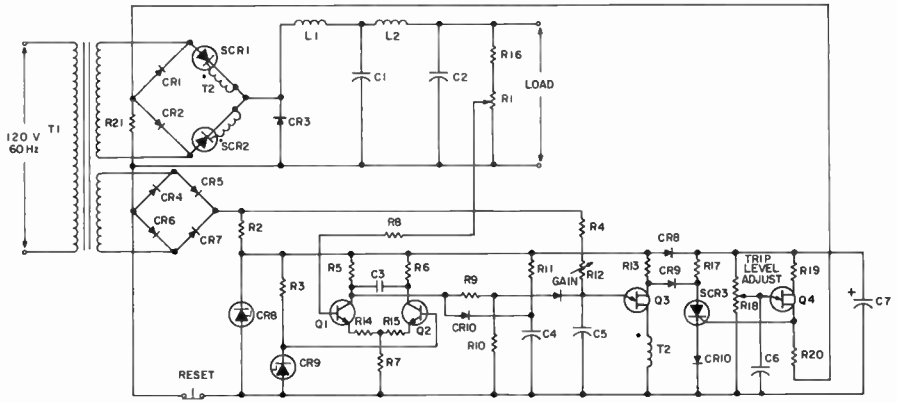
14.8 OVERCURRENT PROTECTION USING GATE BLOCKING

In many phase-controlled and inverter type circuits, SCR's and other circuit components can be protected against overcurrent conditions by removing the gate firing signal from the main power handling SCR's, as soon as excessive current is detected in the circuit. In a phase-controlled system, this will result in fault interruption within one-half cycle after the gate signal has been interrupted since the line voltage reversal will commutate (turn-off) the fault current. In an inverter type of circuit operating from DC without line commutation, the gate signal must be interrupted while the current is still low enough to be commutated by the circuit parameters.

Figure 14.8 illustrates a typical gate blocking circuit as applied to the phase-controlled voltage regulator discussed earlier in Chapter 12. Under normal operation UJT Q3 develops firing pulses which are coupled to the gates of SCR1 and SCR2 through pulse transformer T2. The firing angle and, therefore, the average load voltage are controlled by the feedback action of the differential amplifier Q1 and Q2 on the pedestal height of the voltage waveform on capacitor C5. The UJT Q4, SCR3, a current-sensing resistor R21, and associated components are added to the basic voltage regulator to provide the overcurrent protection feature.

Normally the voltage on the emitter of Q4 is slightly below the peak point triggering level of the UJT, as set by the "Trip Level Adjust" potentiometer. When an overload occurs, the additional voltage drop across R21 drops the voltage on Base 1 of UJT Q4, thus reducing the critical level of voltage required on the emitter to trigger this UJT. If the overload is sufficiently high, Q4 triggers SCR3 and thereby shorts out through CR9 the interbase power supply to UJT Q3. This locks out Q3 from further triggering of the main SCR's in the regulator. SCR3 remains conducting, and the load voltage remains interrupted until the "Reset" button is depressed.

Similar gate blocking circuits for protective purposes can be devised for other types of thyristor applications where the rate-of-rise of fault current is not excessive and where means for commutating this current are available.



CR8, CR9 - GE A13A
CR10 - G-E 1N4009
SCR3 - G-E C106Y
Q4 - G-E 2N2646
R17 - 330 Ω
R18 - 1 MEG POT, 2 W.
R19 - 1K, 1/2 W.
R20 - 22 Ω, 1/2 W.
R21 - 0.007 Ω, 5W.

C6 - 0.04 MFD
C7 - 100 MFD, 30 WVDC
G-E 62F403

FOR OTHER PARTS, SEE FIG. 12.23

FIG. 14.8 PHASE CONTROLLED D.C. POWER SUPPLY WITH OVERCURRENT TRIP

14.9 STATIC SEMICONDUCTOR SWITCHES AND CURRENT-LIMITING CIRCUIT BREAKERS

Static semiconductor switches and circuit breakers may be used for overcurrent protection systems. Several circuits that can be used for this purpose are discussed in Chapter 8. For very high-speed protection of loads against overcurrent, the use of SCR's in electronic crowbar circuits like that shown in Figure 8.16 shunts fault currents away from the load in a few microseconds. Interruption of the fault current is then performed by conventional means such as circuit breakers or fuses.

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15 VOLTAGE TRANSIENTS IN THYRISTOR CIRCUITS

In their early years of development, semiconductor components earned a reputation for being very sensitive to overvoltage conditions in the circuits in which they operated. This shortcoming was accentuated by the relatively limited voltage ratings of semiconductors in comparison with vacuum and gas tubes. More recently, however, significant progress has been made to alleviate the sensitivity of many types of semiconductors to overvoltage situations. High performance power SCR's and diode rectifiers now have voltage capabilities approaching several thousand volts peak. Other semiconductors are now much less prone to damage when subjected to voltage transients that exceed normal operating levels, thanks to improved designs, methods of fabrication, testing, and rating techniques.

With regard to their performance under transient voltage conditions, present-day power semiconductor components can be classified into the following three categories:

1. *Devices that are damaged by low-energy voltage transients above their peak voltage ratings.* This category is typical of the majority of commercial semiconductor components on the market today. Because of their tendency to break down at a microscopic point on the junction periphery, these types of devices usually have little margin between the value of voltage which they can block satisfactorily in the blocking direction on a continuous basis, and the transient overvoltage which will destroy a unit by shorting in a matter of microseconds. Conventional SCR's and diode rectifiers manufactured by General Electric Co. carry a ¼ cycle non-repetitive peak reverse voltage rating that varies between 10 and 50% above the recurrent voltage rating, depending on the type. This additional voltage capacity is a valuable tool in designing reliable circuits with this type of component.
2. *Devices that can harmlessly dissipate high levels of transient energy in their blocking direction.* This category is typified by controlled avalanche rectifier diodes (Section 15.3.4) and voltage regulator (zener) diodes.
3. *Devices that switch harmlessly into conduction when subjected to excess voltage.* Typical semiconductors of this type are triacs, and trigger devices like silicon bilateral switches (SBS) and diacs. As discussed in Chapter 3 the forward blocking characteristic of an SCR is also self-protected by switching into the highly conductive state when the forward breakover voltage is exceeded, except for those SCR's which have a peak forward voltage (PFV) rating. SCR's of this latter type that have very high values of forward breakover voltage may be damaged before anode voltage reaches the breakover voltage.

The last of the three categories, while not plagued by damage to the semiconductor component under transient voltage conditions, may yet be objectionable if a misfire of the semiconductor switch due to a transient causes the circuit or system to malfunction. Such misfires may also occur due to a "first cousin" of voltage transient peaks, namely the dv/dt effect(Section 3.11)

Because of the profound influence of voltage transients on successful and reliable operation of SCR and other thyristor circuits regardless of the particular component type, an understanding of the sources of transient voltages in circuits and the means of reducing them is therefore essential. Thoughtful design practices can then achieve optimum and economical use of the ratings of semiconductor components.

15.1 WHERE TO EXPECT VOLTAGE TRANSIENTS

In the following discussion transients are considered to be those voltage levels which exceed the normal repetitive peak voltage applied to the semiconductor components. In the more common rectifier circuits operating from an AC source, the repetitive peak reverse voltage (V_{RRM}) applied to the semiconductors is equal to the peak line-to-line voltage feeding the circuit. In inverter circuits and other types of DC switches, the repetitive peak voltage applied to SCR's is a function of the particular circuit and must be analyzed on an individual basis. Either or both forward and reverse voltage may change widely in normal circuit operation as load current, conduction angle, load power factor, etc., are varied.

In general, the effect of transient voltages on SCR's and other thyristors is similar to their effect on conventional silicon rectifier diodes, but it should be kept in mind that a thyristor is capable of acting as a high resistance in the forward direction as well as the reverse. In some instances, this blocking action will prevent transient energy from being delivered to and dissipated in the load unless the thyristor first breaks over in the forward direction.

In addition to random line disturbances such as lightning which have been recorded as high as 5600 volts on a 120-volt residential power line, transient voltages across thyristor circuits may be generated by occurrences such as those described in Figures 15.1 through 15.8. The indicated diodes may be conventional rectifiers, SCR's, or other thyristors.

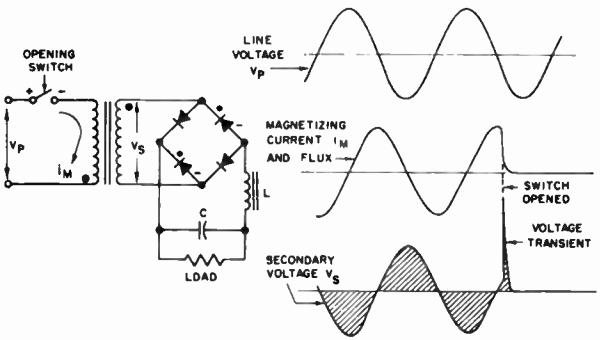

FIGURE 15.1 VOLTAGE TRANSIENT DUE TO INTERRUPTION OF TRANSFORMER MAGNETIZING CURRENT.

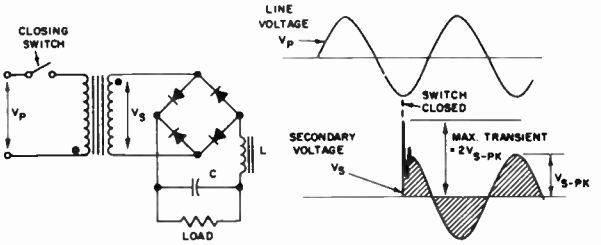

FIGURE 15.2 VOLTAGE TRANSIENT DUE TO ENERGIZING TRANSFORMER PRIMARY

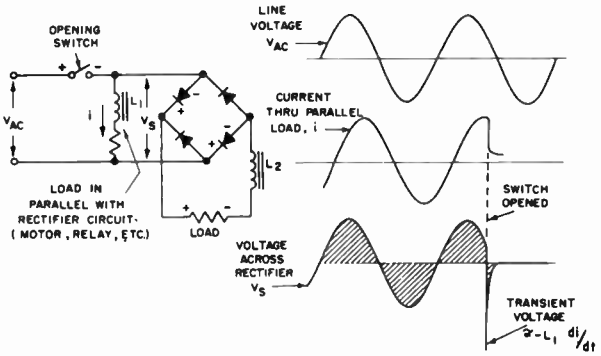

FIGURE 15.3 VOLTAGE TRANSIENT DUE TO SWITCHING CIRCUIT WITH INDUCTIVE LOAD ACROSS INPUT.

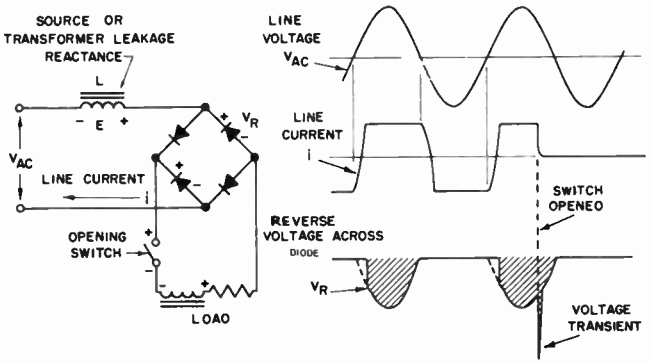

FIGURE 15.4 VOLTAGE TRANSIENT DUE TO LOAD SWITCHING

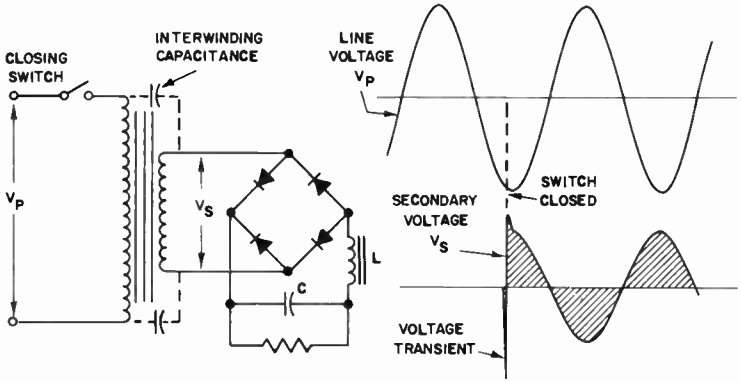

FIGURE 15.5 VOLTAGE TRANSIENT DUE TO ENERGIZING STEP-DOWN TRANSFORMERS.

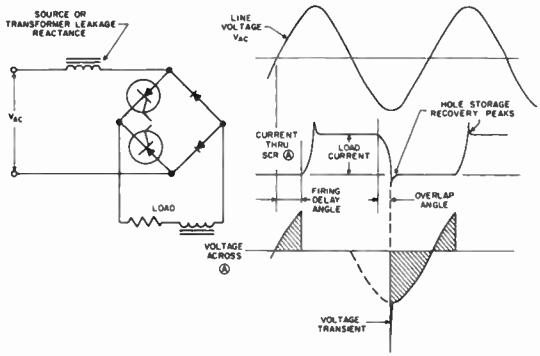

FIGURE 15.6 CYCLICAL VOLTAGE TRANSIENTS DUE TO HOLE STORAGE RECOVERY PHENOMENA. THIS CAN BE PARTICULARLY CRITICAL IN SOME TYPES OF FREE-WHEELING DIODE AND INVERTER CIRCUITS.

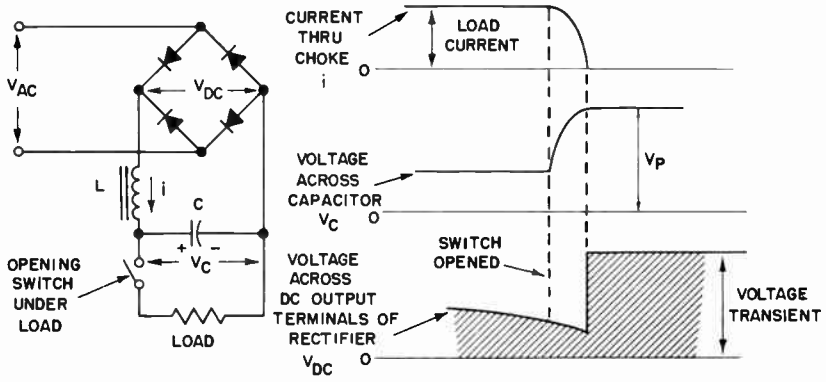

FIGURE 15.7 VOLTAGE TRANSIENT DUE TO DROPPING LOAD FROM EL-TYPE FILTER WITH HIGH L/C RATIO.

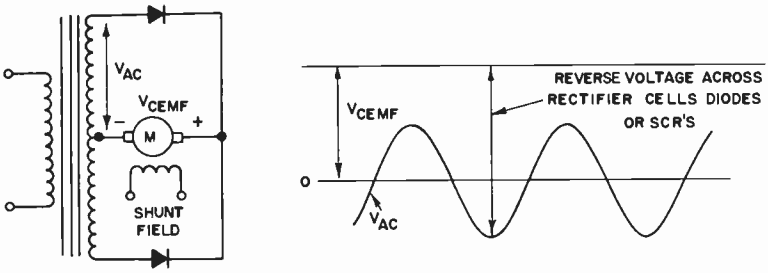

FIGURE 15.8 OVERVOLTAGE DUE TO REGENERATIVE LOAD

Further details on these sources of voltage transients may be found in Reference 7 or in "Rectifier Voltage Transients: Their Generation, Detection and Reduction," Publication 200.11, available on request from the General Electric Company, 1 River Rd., Schenectady, N. Y.

15.2 HOW TO FIND VOLTAGE TRANSIENTS

Only too often the presence of excessive voltage transients in a rectifier circuit is first suspected because of a rash of semiconductor failures in the prototype equipment in the laboratory. Worse yet, these first symptoms sometimes wait until the first equipment is shipped into the field where operating conditions may depart quite radically from the near-ideal conditions that had been successfully passed in the laboratory. When these failures occur at very light loads or immediately following circuit switching, voltage transients should be suspected as the culprit.

Since the search and measurement for possible voltage transients in a circuit may destroy or at least permanently harm semiconductors in the circuit, the anode supply voltage should be reduced to about ¼ or ½ the normal level initially and then gradually increased as measurements indicate the absence or reduction of transients to levels that the semiconductors can withstand.

AC switching transients are usually worst at no load. Therefore, it may be desirable to test the circuit for this type of transient at no load with semiconductors of a lower current rating substituted for the main devices in order to reduce the cost of components that may be destroyed in the course of the test. Also, the higher blocking resistances of lower current components will aggravate voltage transients and thus will generally make measurements and corrective measures conservative.

15.2.1 METERS

Except for very slow high energy transients, instruments with moving coils as their detecting and indicating means are almost useless in measuring transient voltages because of their high inertia and low input impedance. Of the several transient voltage problems discussed earlier, this type of meter may be useful only in measuring the amplitude of regenerative voltage transients such as those generated by a hoist motor being driven by an overhauling load.

15.2.2 OSCILLOSCOPES

A high speed oscilloscope with long persistence screen is probably the most useful single tool for analysis of voltage transients. For significant results in detecting and measuring all the types of transients that may cause rectifier failure, the oscilloscope should have a transient response of at least 0.1 microsecond rise-time and be capable of writing rates in excess of ten million inches per second. Many commercial oscilloscopes meet this specification. A practical screen material is the P11 phosphor. Storage or memory scopes, although handicapped by relatively slow writing speeds and rise-times, are very useful for recording the longer duration types of transients.

For looking at cyclical transients such as those due to recovery from hole storage effects as discussed in Figure 15.6, the use of a scope is straightforward. In this case, the sweep should be repetitive and synchronized with the power system. However, for nonrecurrent types of transients due to switching, more careful precautions are necessary. The scope should be equipped with a hood, and for visual inspection the room should be darkened if possible and the eyes of the operator permitted to become accustomed to a low light level. For checking the amplitude of voltage transients visually, it is sometimes more effective not to use a horizontal sweep, but to use instead only the vertical deflection of the trace. Thus, the eyes can be focused on the precise part of the scope face where the transients will appear, if and when they occur.

When a sweep is employed, it can be triggered by the transient itself or by some external means such as an extra contact or interlock on the circuit switch which initiates the transient. By this latter means, the sweep can be initiated before the transient occurs and any doubt about missing an early part of the transient is eliminated.

The objectiveness of studying and measuring non-cyclical types of transients is enhanced if a photographic record is secured in addition to the fleeting image recorded in the mind by the human eye. In many cases, fast film such as Polaroid Type 42, 44, or 47 (exposure index 200, 400, and 3000, respectively) will catch traces that are not perceptible to the eye.

Circuits should be checked for possible destructive voltage transients by connecting the scope input directly across the semiconductor to be checked.

15.2.3 PEAK RECORDING INSTRUMENTS

Electronic peak recording instruments with a memory can be very useful in checking for transients when their occurrence is random and cannot be predicted. A simple, easy-to-build instrument of this type is described in a General Electric application note, "A Portable Transient Voltage Indicator for Semiconductor Circuits," 200.16, available upon request. This instrument is a "go-no go" type of device for indicating when a transient voltage exceeds the voltage level set on the dial. Accuracy is within 2% maximum setting for voltage pulses down to one microsecond duration. Battery operation increases flexibility of usage and provides continuous operation up to twelve days on one set of batteries. Variations of the basic unijunction-SCR circuitry of this Transient Voltage Indicator permit recording of the frequency of occurrence of voltage transients and the highest transient voltage over an extended inter-

val. Ready-made instruments of this type can be purchased from manufacturers whose names will be furnished on request.

15.2.4 SPARK GAPS

For high voltage systems, calibrated sphere spark gaps can be used to measure the crest values of transient voltages.[4,5] Current through the spark gap after it has broken down should be limited by a non-inductive resistance (at least one ohm per volt of test voltage) in series with the gap on the grounded side. Suitable overcurrent protective devices should be used to interrupt the power follow-through after the voltage surge has passed. In general, the breakdown voltage level for gaps varies significantly with the waveshape of the voltage being measured as well as with many environmental factors.

15.3 WHAT TO DO ABOUT VOLTAGE TRANSIENTS

Given an existing or potential voltage transient problem in a semiconductor circuit, the designer has three main avenues open to him:

1. Use components that are insensitive to the transient voltage or energy conditions.
2. Eliminate or reduce the transients at their source.
3. Provide additional energy storage or dissipation means in the circuit.

The first alternative includes the obvious solution of employing semiconductor components that are less prone to damage by voltage transients. Such devices are typified by triacs which switch on harmlessly when a high voltage transient is applied, and controlled avalanche silicon rectifier diodes and selenium diodes which can dissipate substantial transient energy in their reverse avalanche characteristics. Also, SCR's without PFV limitations switch harmlessly into conduction in the forward direction when subjected to overvoltages. Where the performance of such semiconductors is not adequate for an application, one must consider other alternatives.

When working with more transient-prone semiconductors, a brute force solution is to provide additional voltage capability by using devices with higher voltage ratings or additional devices in series. This alone is usually not the most economical answer. Normally the best solution will lie in a reasonable safety factor of semiconductor voltage rating (1.5-3 times the repetitive circuit peaks) combined with suitable steps to reduce the amplitude of the transients to this semiconductor rating. In circuits using SCR's, economical protection of the SCR reverse characteristic against transients can be achieved by inserting a conventional rectifier diode in series with the SCR. Suitable shunting resistors should be used for voltage equalization. These resistances should be in proportion to the rated voltage of the respective devices across which each is connected. Shunt capacitors may be necessary to equalize the effects of severe commutation.

An example of the second alternative above, eliminating or reducing transients at their source, is to perform switching in the transformer secondary rather than in the primary or load circuits. Since the primary must ulti-

mately be opened, it may be possible to interlock this operation so that the rectifiers are disconnected from the transformer before the primary is opened. Another example of the second alternative is use of a switch or fuse that does not interrupt or chop current too abruptly, thereby limiting transients to lower levels. This type of interrupting device will dissipate the stored circuit energy in its arc. The following list can be used as a guide in selecting switches for low recovery voltage. The list is based on laboratory measurements on samples of each type of switch on a 120-volt 60-Hz circuit. The switches are listed in the order of increasing recovery voltage.

1. Relays (lowest transients)
2. Circuit breakers
3. Snap switches (including microswitches)
4. Mercury switches
5. Vacuum switches (highest transients)

Where the hole storage recovery effect in rectifier diodes causes undesirable voltage transients as described in Figure 15.6, this type of transient can usually be drastically reduced by use of so-called "fast recovery" rectifier diodes (Chapter 21). These components are particularly effective in freewheeling diode and inverter circuits where their roughly 100 to 1 reduction in stored charge practically eliminates the flow of reverse recovery current and the resultant voltage transient that follows it. An additional benefit that stems from the use of fast recovery rectifier diodes is the dramatic reduction in radio frequency interference (RFI) that accompanies the lower level of recovery transients.

The third alternative above entails any number of various schemes for storing and dissipating transient circuit energy. These are treated in the following material.

15.3.1 CAPACITORS

Capacitive filters are one of the more commonly used types of suppressors for low energy transients of the type shown in Figures 15.1 through 15.7. Filters of this type should be placed across the input lines to the semiconductor circuit or across the semiconductor components themselves provided proper precautions are taken to limit the peak discharge current when the semiconductor is triggered.

Figure 15.9 illustrates how the ripple voltage on a filter capacitor in an AC system may be reduced. By connecting the capacitor behind a doubleway rectifier as shown in this illustration, a single capacitor is effective in filtering transients that may occur between any of the lines in a three phase system. What would otherwise be 100% ripple voltage on the capacitor is reduced to approximately 5% and the economical energy storage capabilities of polarized electrolytic capacitors may be used to good advantage.

Filter capacitors may need series resistance to keep them from oscillating with distributed circuit inductance when shocked by a voltage wavefront. When capacitors are connected across the AC line this resistance should be in the order of 5 to 20 times the rated load resistance of the circuit. Final selection of resistance should be based on experimental optimization and the initial di/dt or switching current permitted by the semiconductor rating for the turn-on interval. Series damping resistance is also required in so-called

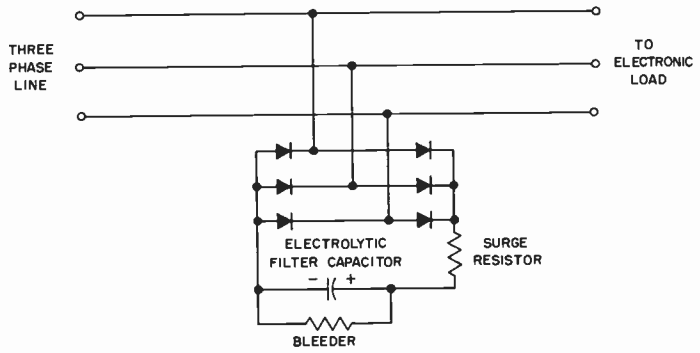

FIGURE 15.9 USE OF ELECTROLYTIC CAPACITORS FOR SURGE SUPPRESSION ON AC SYSTEMS.

"snubbing" circuits across SCR's and diodes for reducing hole storage recovery transients. For capacitors on the DC side of a rectifier, the series resistance should be large enough to protect the semiconductors against the inrush charging current to the capacitor when the circuit is energized initially. The semiconductor manufacturer usually provides surge resistor selection charts for capacitor input filters of this type. The minimum resistance requirement is a function of the capacitance, the supply voltage, and the semiconductor characteristics (I^2t).

Since any inductance in series with the filter capacitor will reduce its effectiveness in suppressing transient voltages, care should be taken in selecting resistors with minimum inductance. Carbon resistors are favored over wire wound types, and capacitors with low self-inductance should be used for the same reason. Since the higher values of electrolytic capacitors may have considerable inductive reactance at high frequencies, it often is helpful to shunt this type with a high frequency type of capacitor (0.1 to 1.0 μfd) to handle these components of the transient.

The size of capacitor required for a particular suppression job is a function of many circuit parameters such as the load current level, the transformer characteristics, and the speed of interruption of switching. Thus it is difficult to predict with any degree of accuracy the optimum size of capacitance. As with the other means of energy storage and dissipation discussed in the following material, actual transient measurements on the prototype equipment will determine the optimum values of filter elements required.

The following equation has proved useful in selecting ample filter capacitance values for one of the most common and severe sources of transient voltages: opening the transformer primary under no load or with inductive load (Figure 15.1):

$$C = \frac{VA}{31\, f\, (V_{pk})^2}$$

where C = filter capacity in farads
VA = volt-ampere rating of transformer
f = supply frequency, Hz
V_{pk} = peak transient voltage rating of each semiconductor leg of the circuit

For evenly distributing the hole storage recovery voltage transient (Figure 15.6) across long series strings of SCR's and diodes, capacitors should be connected across individual cells. The required capacitor size depends on the difference in recovery time between devices. In any event, it need not exceed:

$$C = \frac{10\ I_f}{V}$$

where C = maximum capacitance to limit recovery transient within device voltage rating, microfarads
I_f = amperes flowing through semiconductor immediately preceding commutation
V = maximum continuous peak voltage rating (V_{ROM}) of semiconductor, volts

This value is ultra-conservative and can often be reduced to a few percent of this by experimental optimization.

Capacitors across individual semiconductor components in long series strings are also used to distribute the effects of steep voltage waveforms impressed on the circuit. Because of capacitance between devices and ground, voltage with steep rates of rise would otherwise tend to "crowd" across those devices furthest from ground electrically.[3] Again, resistance in series with the individual capacitors is generally necessary to limit the peak current through a thyristor when it is triggered, as well as to prevent overvoltage "ringing" with source reactance when the circuit is energized.

15.3.2 RESISTANCE

Ample resistive loading across individual legs of a rectifier circuit or across the AC input also provides a means for dissipating stored circuit energy without driving the voltage up to intolerable levels. Care must be taken to keep inductive effects in the resistors to a minimum so that they may dissipate high frequency components as well as lower ones. The disadvantage of the resistance loading approach is the inefficiency that it introduces to the over-all circuit since these resistors dissipate substantial energy at normal voltage levels as well as during transient occurrences.

In circuits where the rise-time of transient overvoltages is not excessive as in some regenerative types of load (Figure 15.8), a voltage sensitive relay may be used to connect a dynamic braking resistor when the DC bus voltage rises to a predetermined level, and to disconnect it when the overvoltage has subsided.

15.3.3 THYRECTOR SURGE VOLTAGE SUPPRESSORS

The introduction of Thyrector surge voltage suppressors by the General Electric Company has greatly reduced the transient voltage protection problem for power semiconductors. These compact non-linear resistances are

essentially selenium "zener" diodes. In many applications they are far more economical and effective than the foregoing techniques of transient voltage suppression.

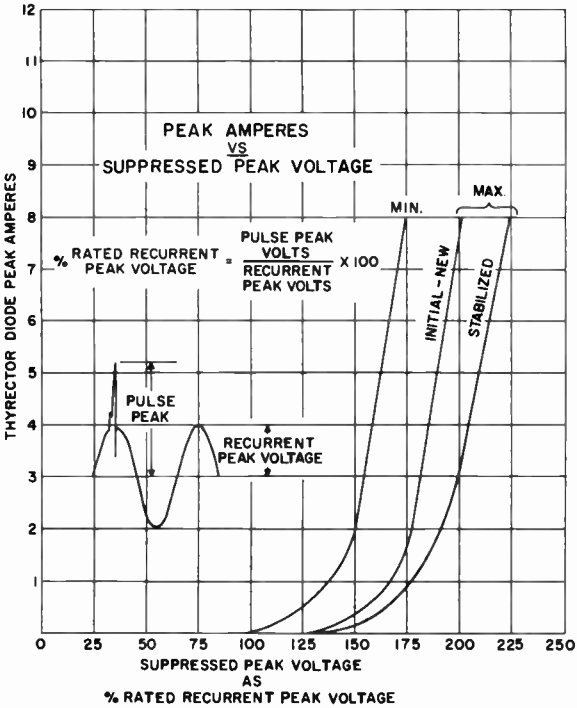

FIGURE 15.10 THYRECTOR DIODE CHARACTERISTICS AT AMBIENT TEMPERATURE OF —20°C TO +100°C (6RS21 CELL).

Figure 15.10 illustrates the voltage-current relationship of the one-inch-square Thyrector diode in an AC circuit. Below rated recurrent peak voltage, the Thyrector surge suppressor draws negligible current. However, as the voltage rises above this point, as would be the case under a transient condition, the Thyrector diode current increases rapidly and dissipates the transient energy. No measurable delay occurs in current flow. When correctly applied, Thyrector suppressors will generally clip transient voltages at 150 to 200% of the recurrent peaks. The one-inch square Thyrector diode is rated 25 volts RMS continuous. Thyrectors are available in compact series assemblies for any multiple of this voltage. Other Thyrector diode sizes are available for suppressing various transient energy levels. Application notes and specifications are available on request.[10]

15.3.4 CONTROLLED AVALANCHE AS A TRANSIENT VOLTAGE SUPPRESSOR

Controlled Avalanche characteristics in silicon rectifier diodes provide a very convenient means of minimizing or eliminating the effects of transient

voltage in thyristor circuits, often without the addition of separate surge suppressor components or substantial voltage safety factors. Introduced by General Electric in 1962, Controlled Avalanche rectifier diodes[9] have avalanche (zener) diode type reverse characteristics that provide built-in transient suppression.

While Controlled Avalanche silicon rectifier diodes have characteristics identical to conventional silicon diodes in the forward load current direction, special design as well as special processing and testing insure reverse characteristics similar to those shown in Figure 15.11 for the A27 twelve ampere Controlled Avalanche rectifier diode. Maximum as well as minimum avalanche breakdown is rigidly specified for each voltage grade. Within its power dissipation capabilities, this type of diode can be operated continuously in the avalanche region, even at avalanche voltages well above 1000 volts. On a transient basis, these rectifier diodes can operate still higher in the avalanche region as defined by the reverse power surge curve of Figure 15.12. For instance, any A27 can dissipate 3900 watts of transient reverse energy for 10 microseconds. An A27 with an avalanche voltage of 1000 volts can therefore conduct over 3 amperes (3900 watts/1000 volts) in its reverse direction for 10 microseconds.

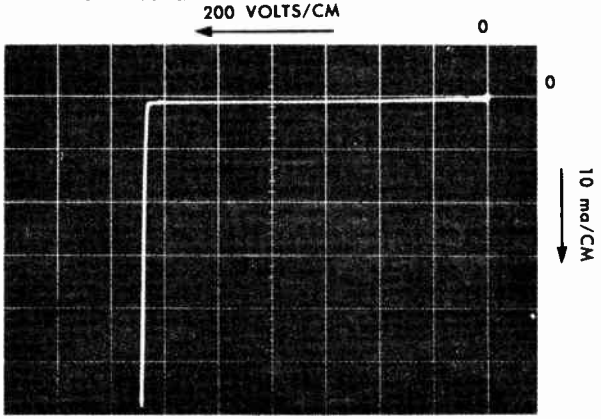

FIG. 15.11 REVERSE CHARACTERISTICS OF TYPICAL A27 CONTROLLED AVALANCHE RECTIFIER DIODE.

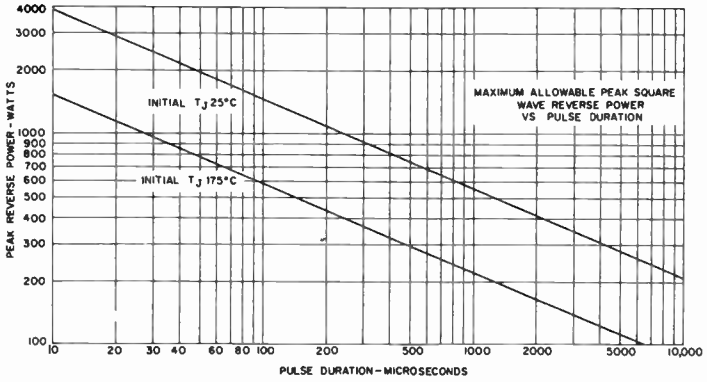

FIG. 15.12 NON-RECURRENT REVERSE POWER SURGE CURVE FOR A27 CONTROLLED AVALANCHE RECTIFIER DIODE.

Controlled Avalanche rectifier diodes are also available in several other forward current ratings extending from ½ ampere to 35 amperes continuous as indicated in Chapter 21. Detailed specifications are available on request.

Besides protecting themselves in the reverse direction against moderate levels of transient energy, Controlled Avalanche diodes can be used to protect other circuit components such as SCR's against overvoltage by virtue of their rigidly specified maximum avalanche characteristics. For instance, the use of Controlled Avalanche diodes to perform the diode functions in the circuit of Figure 15.13 provides inherent suppressing action on voltage transients emanating from either the AC supply or the DC load provided the Controlled Avalanche devices have been properly selected and co-ordinated with the system and the SCR.

Controlled Avalanche rectifier diodes can also be connected directly across individual SCR's as transient suppressors although in many circuits each Controlled Avalanche diode can be used to protect more than one SCR. For example, Figure 15.14 demonstrates the use of two Controlled Avalanche diodes across an AC line to protect four SCR's in a non-freewheeling bridge from line voltage transients. An interesting aspect of this approach is that the Controlled Avalanche diodes will also protect the SCR's against unexpectedly high transient energy levels in excess of the normal energy dissipation rating of the diodes by failing short. In this abnormal case, the Controlled Avalanche rectifiers establish a short circuit across the AC input to the bridge, thereby blowing the line fuse and shutting down the circuit, but protecting the SCR's in the process. Controlled Avalanche rectifier diodes used as expendable overvoltage protective elements in this manner are often an economical means for protecting higher priced semiconductors, particularly where the magnitude, frequency, and energy of transient overvoltages are not known.

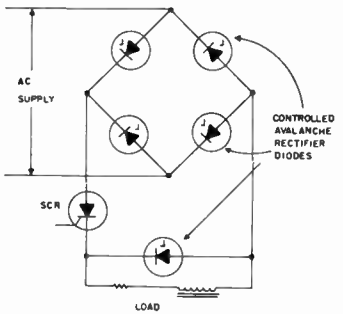

FIGURE 15.13 USE OF CONTROLLED AVALANCHE RECTIFIER DIODES TO LIMIT VOLTAGE TRANSIENTS IN SCR PHASE CONTROL CIRCUIT.

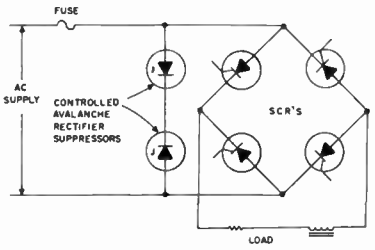

FIGURE 15.14 USE DF CONTROLLED AVALANCHE RECTIFIER DIODES TO PROTECT SCR BRIDGE AGAINST LINE VOLTAGE TRANSIENTS.

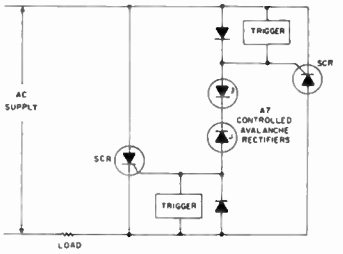

FIGURE 15.15 USE OF LOW POWER CONTROLLED AVALANCHE RECTIFIER DIODES TO TRIGGER SCR'S ON OVERVOLTAGE, THEREBY PROTECTING THE SCR'S AGAINST EXCESSIVE REVERSE VOLTAGE.

Lower power Controlled Avalanche rectifier diodes can also be used as high voltage regulator (zener) diodes in SCR trigger circuits to gate trigger SCR's before overvoltage reaches damaging levels on their anodes. For example, the circuit in Figure 15.15 shows a back-to-back pair of SCR's used to phase control an AC load. Without suitable protection either SCR can be damaged in the reverse direction by excessive transient line voltage spikes if its companion SCR is not triggered in the forward direction. Addition of two Controlled Avalanche diodes selected so that their avalanche voltage occurs below the transient reverse voltage rating of the SCR's insures that neither SCR can be damaged by transient voltage of either polarity.

15.3.5 MISCELLANEOUS METHODS

Several other transient suppression means may be used to good advantage depending on the particular circumstances of the application. Spark gaps may be used in high voltage circuits provided the precautions outlined in Section 15.2.4 are maintained.[6] Silicon diodes can be used as discharge paths for the energy stored in inductive circuit elements such as generator fields and magnetic brakes.

Electronic crowbar circuits of the type shown in Figure 8.16 use the SCR to provide microsecond protection against overvoltage conditions for entire circuits. Properly selected and applied triac and diac components can also be used to shunt transient energy away from sensitive electronic circuitry when voltage tries to rise above the breakover switching level of the particular protective semiconductor component.

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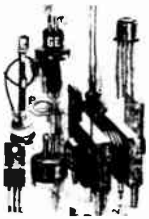
*Refer to Chapter 22 for availability and ordering information.

16 RADIO FREQUENCY INTERFERENCE AND INTERACTION OF THYRISTORS



16.1 INTRODUCTION

Each time a thyristor is triggered in a resistive circuit, the load current goes from zero to the load limited current value in less than a few microseconds. A frequency analysis of such a step function of current would show an infinite spectrum of energy, with an amplitude inversely proportional to frequency. With full wave phase control in a 60 Hz circuit, there is a pulse of this noise 120 times a second. In applications where phase control is used in the home, such as light dimming, this can be extremely annoying, for while the frequencies generated would not generally bother television or FM radio reception, the broadcast band of AM radio would suffer severe interference. In an industrial environment, where several control circuits may be used, these noise pulses cause interaction between one thyristor control and anothanother. The power system can act as a large transmission line and antenna system, propagating these radio frequency disturbances for a considerable distance.

Although thyristor power switches can generate objectionable noise levels in phase control systems, they are in general no worse, and in some cases much better than such things as fluorescent lamp fixtures, electromechanical governers, and series motor brushes. In some areas, notably in static switching of AC circuits, solid state devices can give a decided improvement over mechanical switches, since they have no contact bounce and arcing, and they turn off at current zero, avoiding the interruption of inductive current.

16.2 THE NATURE OF RADIO FREQUENCY INTERFERENCE (RFI)

There are two basic forms of RFI to consider. The first (and most commonly measured) is conducted RFI. In this form, the high frequency energy generated by the thyristor switching transients propagates through the power lines, which act as transmission lines. By using standard methods and equipment, quantitative measurements may be fairly easily obtained on conducted RFI.[1]

The other main form is that of radiated RFI. This is the RF energy which is radiated directly from the equipment. This is a difficult type of RFI to measure since it can never be separated from the problems of location, wiring layout, ground effects, etc.

In most cases, the radiated RFI from a properly designed piece of equipment is insignificant compared to the re-radiation of conducted RFI from the large antenna system we call power lines.

The following military specifications set quantitative interference levels and give test procedures to which an equipment must be qualified if it is to conform to the specification:

MIL-I-6181D
MIL-I-16910C

16.2.1 Filter Design

Since thyristors generate essentially a step function of current when they turn on into a resistive load, the conducted RFI has the frequency distribution of a step function, that is, a continuous spectrum of noise with an amplitude which decreases with frequency at a rate of 20 db per decade. This indicates that even unfiltered thyristor circuits would show very little tendency to interfere with such VHF services as television or FM broadcasting. The AM broadcast band however lies between 550 and 1600 kHz, and would receive severe interference, if the thyristor circuits were not properly filtered.

The simplest type of filter is merely an inductor in series with the load resistance to slow the rate of rise of current. This would give a filter effectiveness of about 20 db/decade. The typical example shown in Figure 16.1 shows that the bottom of the broadcast band requires from 40 to 50 db of suppression to reach a level of interference which could be considered adequate (about 200 quasi-peak μvolts).* To achieve this, the breakpoint frequency, $f_o = R/(2\pi L)$ (where R is the load resistance), would have to be at 5 kHz, or below. This would be a rather large and costly inductor.

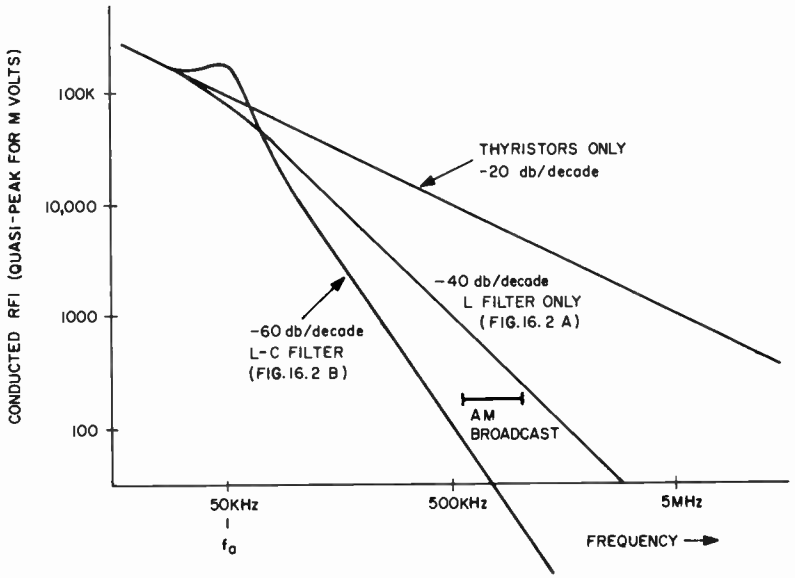


FIGURE 16.1 TYPICAL THYRISTOR CIRCUIT NOISE SPECTRUM WITH AND WITHOUT FILTERING.

*"Quasi-peak Volts" is a unit of measure which is determined by the standard test methods. It is in effect a measure of the "Nuisance Value" conducted RFI.[1]

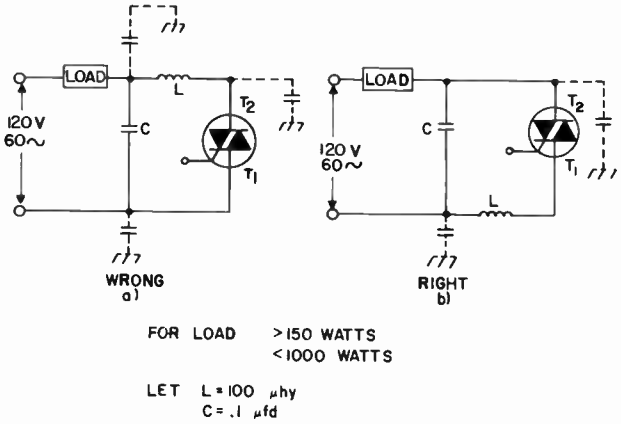


FIGURE 16.2 SIMPLE L-C FILTER

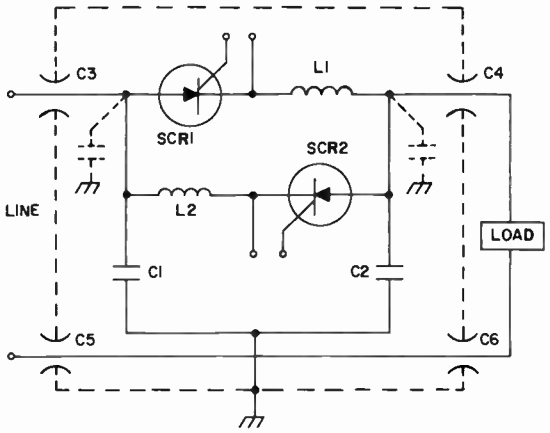


FIGURE 16.3 RFI FILTERING AND SHIELDING FOR BACK-TO-BACK SCR'S

The addition of a shunt capacitance to the filter as shown in Figure 16.2(b) gives a far superior characteristic as can be seen in Figure 16.1. Now the required 40 db of suppression can be obtained in a single decade. As a rule of thumb, the proper values for L and C may be found by making the L-R and L-C breakpoint frequencies equal.

$$f_o = \frac{R_L}{2\pi L} = \frac{1}{2\pi\sqrt{LC}}$$

or in other words

$$2\pi f_o L = \frac{1}{2\pi f_o C} = R_L$$

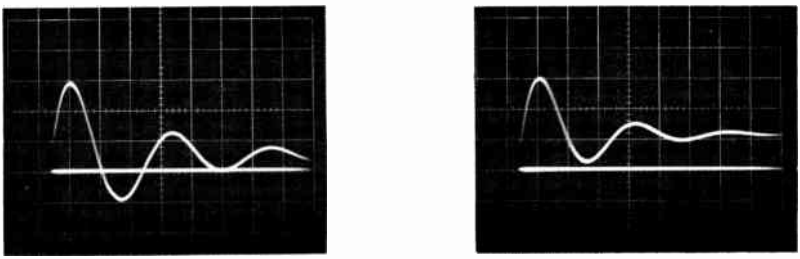
This allows a value of L one tenth that needed for a purely inductive filter.

In a practical thyristor circuit, one side of the device is usually connected to a heat sink, which because of its size or mounting, is capacitively connected to ground. In the case of the triac shown in Figure 16.2 main terminal T_2 is the heat sink side. If the choke L were in series with T_2, as in Figure 16.2(a), the heat sink capacitance in conjunction with stray line capacitance would shunt the choke, thereby reducing its effectiveness as a filter. The proper connection of L in series with T_1 actually puts the stray capacitances in parallel with C, thus enhancing filter effectiveness.

The optimum connection for back-to-back SCR's is shown in Figure 16.3. If a shielded enclosure is not present, C_1 and C_2 should be a single capacitor connected between the anodes of SCR_1 and SCR_2.

It is important to note that any pulse transformers or triggering circuits should put the smallest possible capacitive loading on the cathode of the SCR's, since this capacitance will appear across the chokes.

If you look at the circuits of Figure 16.2, you can see that the L-C and triac form a resonant discharge circuit, which depends on the load impedance for damping. For circuit Q's greater than about 2.5 the current through the triac will reverse, as shown in Figure 16.4, and a specific triac might turn off if it is a relatively fast device. An SCR circuit would of course behave in an identical manner. This condition is worst for light loads, in this case about 100 watts or less, or somewhat inductive loads, which contribute little damping to the circuit. The simple L-C circuit does behave properly however with heavier resistive loads, as shown in Figure 16.4(b). To obtain proper operation under light load conditions, for instance a lamp dimmer with a 60 watt lamp, it is necessary to build the damping required into the filter. This can be done by adding another resistor and capacitor as shown in the circuit of Figure 16.5. The component values are chosen to give about the same filtering effect as the L-C filter of Figure 16.2(b).



(a) 60 WATTS

(b) 150 WATTS

VERT. - 2 AMP/CM
HORIZ. - 5 μSEC/CM

FIGURE 16.4 TRIAC CURRENT FOR THE CIRCUIT OF FIGURE 16.2(B)

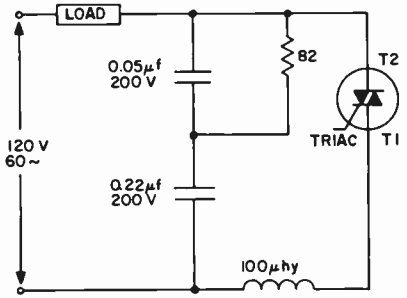


FIGURE 16.5 TYPICAL DAMPED R-F FILTER

16.2.2 Zero Voltage Switching

As we have seen, the RF noise contribution of thyristors is primarily due to a sudden step in current as the thyristor switches. In some applications, particularly in electric heating, satisfactory control may be obtained by turning the thyristors on at line voltage zeros, giving only complete half cycles of current to the load. By eliminating the sudden steps of voltage, the RF noise contribution is brought to an absolute minimum. This eliminates the need for R-F filter components, which, for a large heating load, can become quite large and costly. For details on this type of circuit, see Chapters 4 and 8.

16.2.3 Fast Recovery Rectifiers

In circuits which use rectifier diodes, RF noise may be generated by the reverse recovery performance of the diodes. Due to the minority carrier storage effect, the diode does not immediately block voltage when the circuit causes current reversal. When, after a few μseconds, the charge which had been stored in the diode is "swept-out," the diode can again block the flow of reverse current. At this point, the current can stop quite suddenly, giving a "snap-off" effect. The energy stored in the circuit inductance at this point can be shown to be equal to

$$W_T = Q_R E_C$$

where Q_R is the total charge swept-out
E_C is the circuit commutation voltage.[2]

Figure 16.6 shows the waveform of the recovery current of a conventional as well as a fast recovery diode.

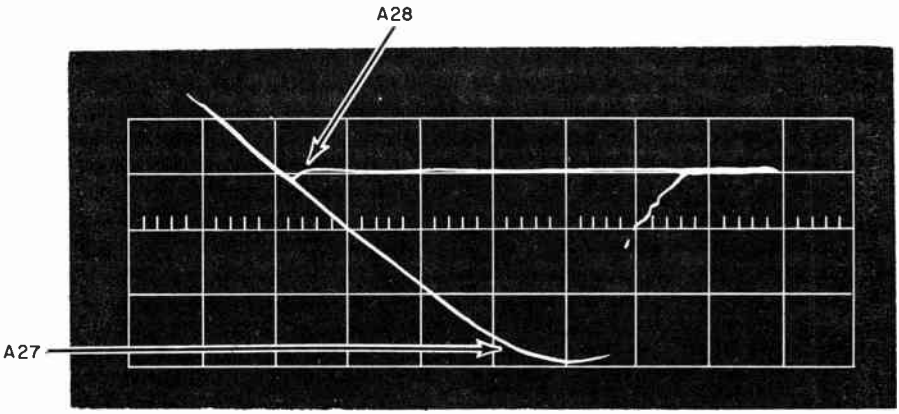


FIGURE 16.6 COMPARISON OF REVERSE RECOVERY PERFORMANCE OF TYPICAL RECTIFIER DIODES. VERTICAL = 8 AMPS. PER CM. HORIZONTAL = .5 μSEC. PER CM.

On each "snap-off" commutation of a diode there is a step of current of height I_{RP}. The RF components of this step are given by

$$S(\omega) = \frac{I_{RP}}{\pi\ \omega}$$

where ω is an RF noise component frequency.
This result is found by Fourier Integral Analysis of a step function.[3]

The RF energy at a given frequency is proportional to the square of this value, or

$$W_{(\omega)} \propto \frac{I_{RP}^2}{\pi^2\ \omega^2}$$

But W_T is proportional to I_{RP}^2, so

$$W_{(\omega)} \propto \frac{W_T}{\omega^2}$$

Since the value of W_T runs better than 100 times less for a fast recovery rectifier than for a conventional rectifier, there is a considerable reduction in RFI problems when using fast recovery devices.

16.2.4 Reduction of Radiated RFI

The minimization of radiated RFI is as much a matter of good construction practice as anything else. Referring to Figure 16.2(b), the current through the loop formed by C, L, and the thyristor contains high frequency components of a much greater magnitude than the line current. (The inner loop has only a single L filter). The wiring of this loop can act as an an-

tenna for direct radiation. Since the radiation efficiency of an antenna of this type is proportional to the area enclosed by the loop, good practice requires that this current loop be constructed with a minimum of enclosed area. It should be pointed out that trigger circuits can also be offenders in direct radiation, and the same techniques apply.

Figure 16.3 illustrates proper shielding techniques. The SCR's with their filter circuitry are enclosed inside their own shielded compartment, with leads from the power line and to the load passing through feedthrough capacitors C_3-C_6. Either the pulse transformer or the gate pulse generation circuitry should be located within the compartment, since locating them remotely forces one to hang leads on the cathodes of the SCR's, thereby providing excellent antennas.

16.3 INTERACTION

In some instances the thyristor system acts as a "receiver" of voltage transients generated elsewhere in the circuit. These transients act either (or both) on the thyristor trigger circuit or directly on the anode of the thyristor in the main power circuit. Interaction will cause the thyristor system acted upon to completely or partially follow, or track, another thyristor system. Also, various types of partial turn on, depending on the nature of the trigger circuit, have been known to arise. Elimination of interaction phenomena must take total system layout into consideration. Section 16.6 gives some general design practices which should be followed to minimize possible sources of interaction. Beyond good design practice in the system as well as in triggering circuits very specific steps for decoupling can be taken as outlined for UJT circuits in Section 16.4.

16.3.1 Interaction Acting on Anode Circuit

When a thyristor circuit is acted upon with its gate circuit disconnected (open gate or terminated per specification bulletin) the nature of the interaction is usually attributable to a rate of rise of forward voltage (dv/dt) phenomenon. When energizing the circuit, such as by a contactor or circuit breaker, applicable dv/dt specifications for the device must be met. This subject is discussed in detail in Chapter 3. Once the circuit is energized the thyristor will sometimes respond to high frequencies superposed on the anode supply voltage. For example, a 1-megacycle oscillation having a peak amplitude of 10 volts has an initial rate of rise in the order of 60 volts per microsecond. Applicable specifications for the thyristor must meet this condition or steps should be taken to attenuate the rate of rise of voltage.

Due to the nature of anode circuit interaction a thyristor will rarely track another circuit over the full control range of phase control. Usually, it will tend to lock in over a very limited range near the top of the applied anode voltage half cycle where the dv/dt is greatest. The best means of suppressing this type of interaction is to select a device with increased dv/dt withstand capability, to increase dv/dt withstand capability by means of negative gate bias, or, conversely, to reduce the rate of rise of positive anode

voltage by suitable circuit means. The effect of negative gate bias on SCR dv/dt withstand capability and dv/dt suppression circuitry is discussed in Section 3.11. Often a combination of these steps yields the desired results. In addition, of course, good circuit layout and system practices should be observed as outlined in Section 16.6.

16.3.2 Interaction Acting on the Trigger Circuit

There are basically two cases to distinguish here:

1. The trigger circuit is acted upon from the supply line directly;
2. The trigger circuit is acted upon from the thyristor gate circuit.

Both of these mechanisms may cause the trigger circuit to fire prematurely, giving rise either to spurious triggering or complete or partial tracking of the thyristors in the circuit. The response of the trigger circuit to incoming transients will determine the degree of interaction, if any. There are no general rules for every type of trigger circuit. However, in the design of a trigger circuit it is well to take the possibility of interaction into account. The designer will be in the best position to assess the transient susceptibility and stability of his circuit.

When using the unijunction transistor trigger circuit there are a few relatively simple steps that can be taken to decouple these circuits against both supply voltage and gate circuit transients. These methods are outlined in the following two sections.

16.4 DECOUPLING THE UJT TRIGGER CIRCUIT AGAINST SUPPLY TRANSIENTS

Depending on the nature of the particular circuit conditions, either one or a combination of the following will give effective decoupling against line voltage transients acting on the unijunction transistor trigger circuit:

1. Use of control (isolation) transformer with an RF filter across its secondary, if necessary;
2. Use of "boot strap" capacitor between base two and the emitter of the unijunction transistor;
3. Use of a Thyrector diode connected across the supply to the unijunction circuit.

The value of the "boot strap" capacitor C_1 should be chosen so that the voltage divider ratio of C_1 and C_2 in Figure 16.7(A) is approximately equal to the intrinsic standoff ratio of the UJT, or:

$$\frac{C_1}{C_1 + C_2} = \eta$$

If this condition is met, positive or negative transients on the unijunction supply voltage will not trigger the UJT.

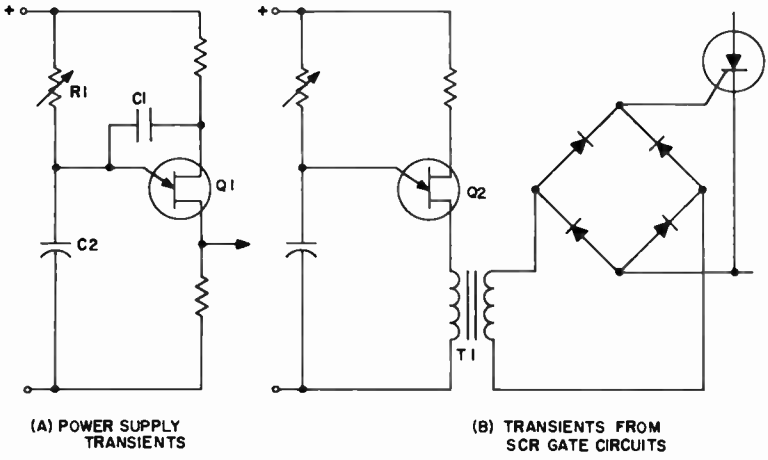


FIGURE 16.7 CIRCUITS FOR ELIMINATION OF ERRATIC FIRING FROM VOLTAGE TRANSIENTS IN UJT CIRCUITS.

16.5 DECOUPLING UJT CIRCUITS AGAINST SCR GATE TRANSIENTS

Negative voltage transients appearing between the gate and cathode of the SCR's when transmitted to the UJT can cause erratic triggering. When transformer coupling is used, these transients can be eliminated by using a diode bridge in the gate circuit of the SCR as shown in Figure 16.7(B). Negative transients often arise in SCR gate circuits in forced-commutated circuits (see Chapter 5) and under certain conditions in AC phase control circuits.

16.6 GOOD DESIGN PRACTICES TO MINIMIZE SOURCES OF SCR INTERACTION

Radio frequency interference and interaction are both total system phenomena and no one step is necessarily the most effective in attaining the desired level of suppression. A combination of good system design practices, good circuit layout, good equipment layout, and, if necessary, a small amount of circuit filtering, as was outlined above, will suppress RFI to acceptable levels and eliminate various types of interaction phenomena.

When the following system considerations are met it is often unnecessary to take additional specific steps to filter trigger or anode circuits (Section 16.2) or use negative gate bias and dv/dt suppression circuitry (Section 3.11):

1. Operate parallel and potentially interacting thyristor circuits from a stiff (low reactance) supply line;
2. If supply line is soft (high reactance), consider using separate transformers to feed the parallel branch circuits; each transformer should be rated no more than the required rating of the branch circuit load;
3. Avoid purely resistive loads operating from stiff lines—they give highest rates of current rise on switching;
4. Keep load moderately inductive—limiting rate of current rise on

switching is in the direction of attenuating RFI and minimizing the possibility of interaction;

5. Keep both leads of a power circuit wiring run together—avoid loops that encircle sensitive control circuitry;
6. Arrange magnetic components so as to avoid interacting stray fields.

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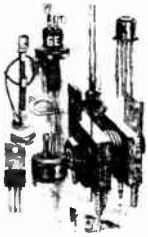
*Refer to Chapter 22 for availability and ordering information.

17 COOLING THE POWER SEMICONDUCTOR



Successful application of SCR's depends to a great extent on adequate cooling of these devices. If junction temperature of an SCR rises high enough, permanent damage may occur in its characteristics and the device may fail by thermal runaway and melting. Circuits may fail before thermal runaway or melting in the SCR occurs since insufficient cooling can reduce the forward breakover voltage, increase SCR turn-off time, moving these and other SCR characteristics outside specifications sufficiently to induce circuit malfunction. For these reasons, all SCR's and rectifier diodes are designed with some type of heat transfer mechanism to dissipate internal heat losses.

17.1 LEAD-MOUNTED SCR'S

For small lead-mounted SCR's like the C3, C5, C6, C7, C8 and C9 series, and some configurations of the C106 (see Fig. 17.1), cooling is maintained by radiation and convection from the surface of the case and by thermal conduction down the leads.

Several good common sense practices for minimizing the SCR temperature should be used whenever possible. Minimum lead length to the terminal board, socket, or printed board permits the mounting points to assist in the cooling of the SCR most efficiently. Other heat dissipating elements such as power resistors should not be connected directly to the SCR leads where avoidable. Also, high temperature devices like tubes, power transformers, and resistors should be shielded from radiating their heat directly on the SCR case. To increase heat dissipation of the standard TO-5 case, clip-on transistor radiators are available from a number of commercial vendors.

Several of the General Electric lead mounted SCR's in the TO-5 case are also available on a power transistor type of base for attachment by screw to a heatsink or chassis. Directions for mounting these devices are given on the specification sheet for that type of SCR.

17.2 TAB-MOUNTED SCR'S

Figure 17.1 shows various configurations of the C106 SCR. Some configurations of the SCR are provided with an anode tab for mounting directly to an appropriate heat exchanger. Because of this unique package design, it can be mounted in a variety of methods, depending upon the heatsink requirements and the circuit packaging methods.

The tab and the leads will bend easily, either perpendicular to the flat or to any angle, and may also be bent, if desired, immediately next to the plastic case. For sharp angle bends (90° or larger), a lead should be bent only

once since repeated bending will fatigue and break the lead. Bending in other directions may be performed as long as the lead is held firmly between the case and the bend, so that the strain on the lead is not transmitted to the plastic case.

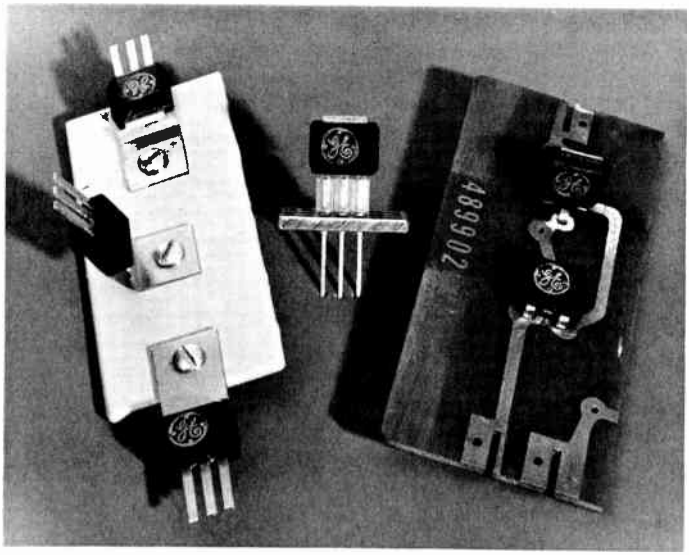


FIGURE 17.1 LEAD OR TAB MOUNTED TYPE C106 SCR

The mounting tab may also be bent or formed into any convenient shape so long as it is held firmly between the plastic case and the area to be formed or bent. Without this precaution, bending may fracture the plastic case and permanently damage the unit.

As a service to its customers, the General Electric Company provides a lead and tab shaping capability. Any of the derived types shown in Figure 17.2 are available directly from the factory to original equipment manufacturers.

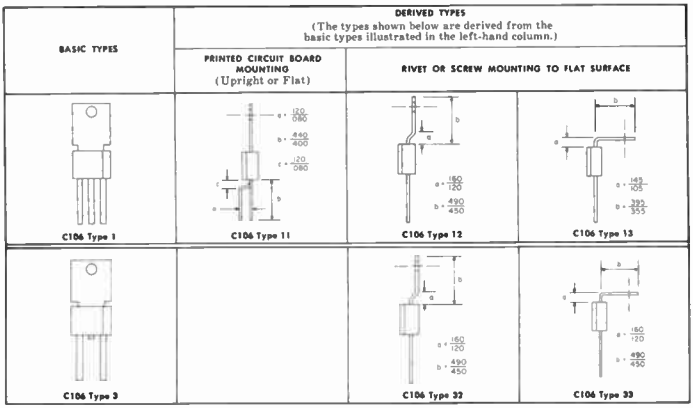


FIGURE 17.2 LEAD/TAB ARRANGEMENTS FOR TYPE C106 SCR

17.3 SCR STACK ASSEMBLIES

For higher rated SCR's, stack assemblies are supplied by General Electric. Figure 17.3 shows typical stack assemblies. Various fin sizes and configurations provide conservative cooling of each SCR type in the General Electric line. These stacks are fully rated in terms of ambient conditions (air velocity, temperature). Literally tens of thousands of pre-wired circuit combinations are available, and associated rectifier diodes can be assembled integrally in the same stack. Detailed specifications are available on these SCR stack assemblies. They explain how these stacks can perform many useful functions in diversified applications.

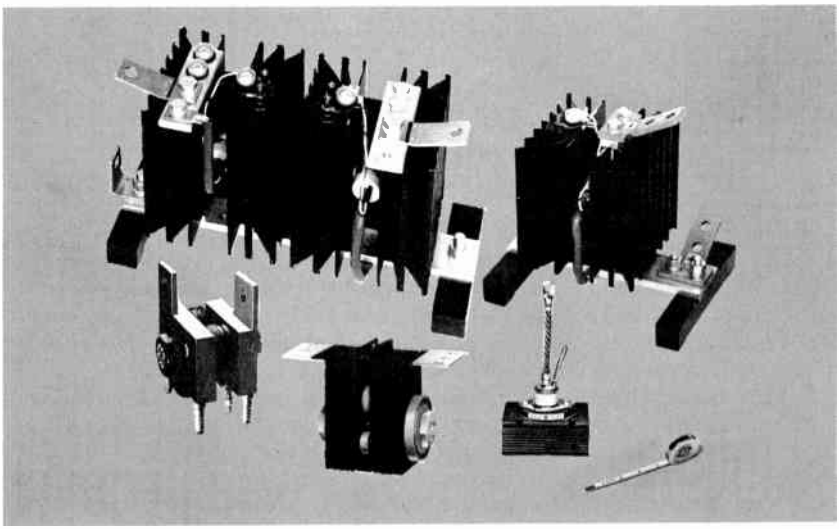


FIGURE 17.3 TYPICAL GENERAL ELECTRIC PRE-WIRED SCR-RECTIFIER STACK ASSEMBLIES.

17.4 MOUNTING SCR'S TO HEATSINKS

Other than the lead or tab mounted SCR types, four different packages are in common use for SCR's. These four types are the stud-mounted, press fit, flat-base, and Press Pak configurations. We will discuss general considerations of mounting first and then cover those situations peculiar to each package type. Usually some form of heatsink or heat exchanger is required with an SCR. The heatsink may consist of a busbar, chassis, liquid cooling system, or a special cooling fin for dissipation of heat to the surrounding air.

If the heatsink is to perform an optimum cooling job, the semiconductor package must be mounted not only in a good location on the heatsink, but also in such a manner as to achieve low thermal resistance to heat flow from the stud to the heatsink. Proper mounting is not always a straightforward simple matter. Several precautions should be considered.

17.4.1 Selection of Heatsink Materials

Maximum cooling effectiveness calls for copper as the heatsink material because of its high thermal conductivity. However, cost considerations may dictate steel instead, and in some cases weight and ease of extrusion may bring aluminum into the picture. Two significant factors should be considered particularly for aluminum heatsinks.

Where moist or corrosive atmospheres are expected, galvanic action between aluminum and the copper SCR case may lead to gradual deterioration of the joint, and an increase in thermal resistance. A good nickel or silver plate over the copper case as provided on General Electric SCR's, combined with use of a corrosion inhibitor, such as Burndy-Penetrox A; Alcoa No. 2, or Penn-Union Cual-Aid, minimizes corrosion at this joint.

17.4.2 Heat Exchanger Surface Preparation

Optimum heat transfer from semiconductor case to heat exchanger surface depends heavily on adequate contact between the two surfaces. Care should be taken to insure a flat surface, free of ridges or high spots.

The surface under the semiconductor contact surface should be flat to within 0.001 inch per inch and have a surface finish of 63 micro-inches or less. Before final assembly, the semiconductor case surface should be checked for removal of all burrs or peened-over corners that may have occurred during shipping and subsequent handling and that would otherwise cause reduced heat transfer across the surfaces.

Most heat exchanger surfaces have some treatment to aid radiation heat transfer and give corrosion protection. Copper fins are plated, painted, or ebnoled. Aluminum fins are generally painted or anodized. The heat exchanger surface under the semiconductor contact surface must be free of paint, anodization, or ebnol to give minimum contact thermal resistance. While plating in this area does not have to be removed, excessive oxides should be removed.

17.4.3 Mounting the Stud Type SCR

The stud-mounted SCR is a particularly flexible component and has wide acceptance. This type of SCR uses a copper stud with a machine thread for making mechanical, electrical and thermal contact to a heatsink of the user's choosing.

If the hole is punched, the fin should be subsequently blanked. If the hole is drilled, the burr should be carefully removed. The hole size should be between 0.005 and 0.015 inch larger than the stud outside diameter. If the stud has a fillet where the thread meets the flat surface of the hex, the fin hole should be chamfered to prevent the stud from hanging up on this fillet.

Mounting straight threaded copper studs into a threaded hole in an aluminum fin is not recommended. Unequal temperature coefficients of expansion of aluminum and copper cause "thermal ratcheting." This tends to unscrew the copper stud from the threaded hole as the temperature cycles. The result is higher stud-fin contact thermal resistance.

Where a copper stud is screwed into a tapped hole in a copper heat exchanger, extreme care must be taken to assure that drilling and tapping are at right angles with the heat exchanger surface.

When mounting copper studs to a fin through a clearance hole by means of a nut on the backside, relaxation and metal creep may cause the mounting to gradually loosen. This condition is accelerated by temperature cycling and is dependent upon the magnitude of the time-temperature relation. As a consequence of this condition, the stud-fin contact thermal resistance will increase with time-at-temperature because of a loss of contact pressure. Tests have shown that after 1000 hours of operation, the stud-fin contact thermal resistance can increase as much as three times the initial value.

To minimize the effect of relaxation, which is common in any fastener under torque, it is recommended that a belleville spring washer be used between the nut and fin. A commercially available nut-belleville washer assembly, made by Shakeproof Corp., Elgin, Illinois, has been found to be satisfactory for maintaining the initial stud-fin contact thermal resistance. Tests using the ⅜, ½ and ¾ inch nut-washer assembly, Shakeproof numbers ND16470, ND16105, and ND16501 respectively, showed a 11 per cent maximum increase in the initial stud-fin contact thermal resistance after 1000 hours at 150°C.

Good thermal contact between the semiconductor stud and the heatsink requires adequate pressure between these two surfaces as applied by torque on the threads of the device. However, torque beyond a certain point no longer improves the thermal contact and may mechanically stress the SCR junction and materials soldered or brazed to the stud inside the housing. Permanent damage to the device characteristics may result. For this reason, precise adherence to the manufacturer's torque recommendations is necessary, and a torque wrench should *always* be used in mounting this type of semiconductor. Table 17.1 lists recommended mounting torques for the General Electric line of stud-mounted SCR's and rectifier diodes.

The recommended torques are for clean, dry threads. Also, on semiconductors with a ⅜-24 stud or larger, the torque is applied on the nut while holding the semiconductor stationary.

Torque wrenches, such as those made by the P. A. Sturtevant Company, should be chosen for the accurate range of torque that is to be used on a given rectifier diode or SCR.

Flat-Base Dia.	Stud Size	Hex Size Across Flats	Typical Max. Recommended Torque (in lb.) (For exact values see spec. sheets)	Effective Hex/Base Diameter (Inches) d	Case Contact Thermal Resistance* (°C/Watt) Metal to Metal			With 0.005" Mica Insulation	
					Dry	With Penetrox‡	With† G623 DC-3 DC-4	Dry	With Penetrox‡
—	10-32 NF	7/16"	15	0.46	0.75	0.60	—	6.5	6.0
—	1/4"-28	9/16"	30	0.59	0.45	0.35	—	4.0	3.5
—	1/4"-28	11/16"	30	0.72	0.30	0.25	—	2.5	2.2
—	3/8"-24	1-1/16"	100	0.91	0.15	0.10	—	—	—
—	1/2"-20	1-1/16"	150	0.91	0.10	0.09	—	—	—
—	3/4"-16	1-1/4"	300	1.20	0.06	0.05	—	—	—
—	3/4"-16	1-5/8"	300	1.50	—	—	0.08	—	—
1 7/8"	—	—	§	1.75	—	—	0.08	—	—

*Values apply for studs tightened down with maximum recommended torque to reasonably smooth flat surfaces by means of nut and clearance hole mounting. Thermal resistance values are stabilized values from studs to point on fin at diameter d. Value for flat-base unit when mounted as per 17.4.4.
†G623—General Electric Co. Silicone Prod. Dept., Waterford, New York.
DC-3 and DC-4—Dow Corning Co., Midland, Michigan
‡Penetrox 'A,' made by the Burndy Corp.
§See Section 17.4.4.

TABLE 17.1 CHARACTERISTICS OF STANDARD POWER SEMICONDUCTOR PACKAGES

17.4.4 Mounting the Press-Fit Semiconductor

Certain sizes of SCR's such as the types C22, C32, C33 and triacs such as the SC41 and SC46 as well as silicon rectifier diodes like the A44 and A45 are available in the so-called "press-fit" package. This package is designed primarily for forced insertion into a slightly undersized hole in the heatsink. When properly mounted this type of SCR has a lower thermal drop to the heatsink than the stud type mounting. Also, in high volume applications the cost of this type of mounting is generally less than that for the stud type of SCR.

The following simple procedures should be followed when press-fitting appropriate SCR's:

1. Heatsink materials may be copper, aluminum, or steel in order of preference. The heatsink thickness should be a minimum of 1/8 inch, the width of the knurl on the housing.
2. The hole dimensions are shown in Figure 17.4. The hole may be punched and reamed in a flat plate or extruded and sized in sheet metal. A slight chamfer on the hole should be used to guide the housing.

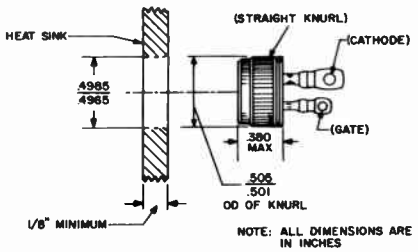
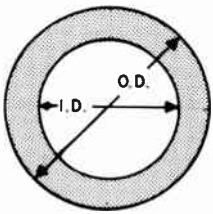


FIGURE 17.4 MOUNTING THE PRESS-FIT POWER SEMICONDUCTOR

3. To insure maximum heat transfer the entire knurl should be in contact with the heatsink. The unit must not be inserted into the heatsink past the knurl. This is to prevent the header from taking pressure off the knurl in a deep hole.
4. The insertion force must be limited to 800 pounds. This is to prevent misalignment with the hole and/or excessive unit-to-hole interference. Pressure must be uniformly applied to the face of the header as shown in Figure 17.5.



I.D.=.390/.370
O.D.= - /.500

→UNIFORM PRESSURE AREA

FIGURE 17.5 AREA OF APPLYING PRESSURE TO PRESS-FIT POWER SEMICONDUCTOR.

If the device is inserted in the above prescribed manner (using a copper heatsink), the thermal resistance, case to heatsink, will be less than 0.5°C/watt. The insertion is generally accomplished by means of an hydraulic ram. Reading the pressure and knowing the piston area, one can pre-set the maximum insertion force. Another possible insertion method which is simple to employ, but which gives no provision for measuring insertion force, is accomplished by the use of two blocks of wood and a bench vise as shown in Figure 17.6.

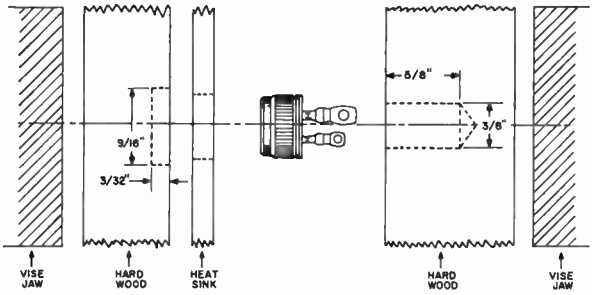


FIGURE 17.6 USE OF VISE TO INSERT PRESS-FIT POWER SEMICONDUCTOR

There are commercially available heatsinks specifically designed to accommodate press-fit devices. One such is a radial fin semiconductor cooler (NC-300-R series) manufactured by Wakefield Engineering Inc. These coolers are available in different sizes with hole accommodation for one or two press-fit units.

Several other mounting methods for press-fit devices are possible. Different types of mountings will demonstrate different thermal characteristics and in a good many cases the characteristics will not be readily predictable from theory. For suggestions on different mounting techniques, see Reference 4.

17.4.5 Mounting the Flat Base Semiconductor

A number of General Electric high current SCR's and rectifier diodes are provided in a flat base package such as shown in Figure 17.7. At present only one package size is available in this flat base configuration and therefore our discussion can be specific. However, the points covered will generally apply to any similar flat-base package.

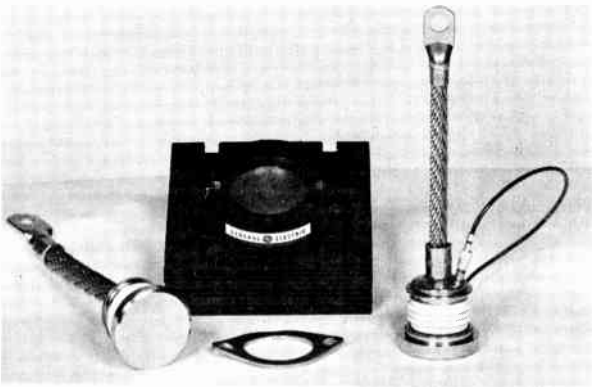


FIGURE 17.7 THE FLAT-BASE POWER SEMICONDUCTOR

The following mounting hardware is supplied with each device:

4 bolts (2 lengths)
2 hex nuts
1 spring clamp
2 spacers

For those mounting situations requiring a second spring clamp (see Figure 17.9a) it should be requested when ordering SCR. The second clamp for this SCR is supplied at no additional cost. Heatsink surface preparation is described in Section 17.4.2.

17.4.5.1 Heatsink Thickness

1. *For all heat sinks over 7/8" in thickness at mounting surface,* two holes are to be drilled and tapped for a 5/16-18 UNC2A bolt to a depth of 7/8". See Figure 17.8.
2. *For all heat sinks 7/8" and under in depth,* two clearance holes are to be drilled for a 5/16" bolt, 2 1/2" ± 1/64" apart, center line to center line.

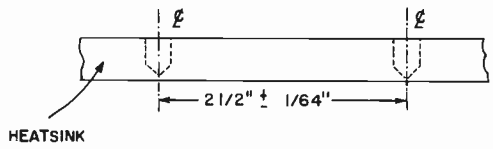


FIGURE 17.8 DRILLING THE HEATSINK FOR THE FLAT-BASE PACKAGE

17.4.5.2 Mounting Procedure

1. See Section 17.5 for proper lubrication of cell-heat exchanger interface.
2. On all heat sinks between 1/4" and 7/8" thick (heat sinks under 1/4" are not used) slide both bolts through the spring clamp, spacers, heatsink and spring clamp (on the opposite side of the heatsink). See Figure 17.9(a).
3. Run the nuts up the bolts finger tight and position the cell so that the cable on the cell can be easily connected to its proper location without a strain on the cell.
4. Tighten the nuts until the spring clamp over the cell bottoms against the spacers. (The spring clamp will then be flattened.)
5. *Be sure that there is no strain on the cable when connecting it to its proper terminal.*
6. For thick heatsinks (over 7/8") the procedure is similar with the exception that only one spring clamp is used. See Figure 17.9(b). For further mounting details see appropriate specification bulletin.

17.4.6 Mounting the Press-Pak

In 1966 General Electric introduced the Press-Pak SCR. This radical change in power semiconductor packaging is shown in Figure 17.10. For package details, see appropriate specification bulletin.

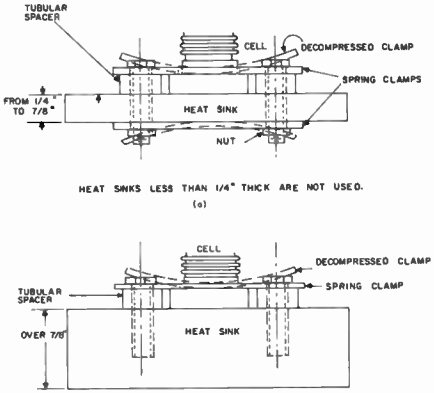


FIGURE 17.9 MOUNTING THE FLAT-BASE PACKAGE

FIGURE17.10 THE C350 AND C380 PRESS-PAK

The Press-Pak is a presure mounted device wherein the pressure is *externally* applied and retained; that is, proper electrical and thermal contact is maintained by presure mounting the Press-Pak between two heat exchangers. Of course, single sided cooling is also feasible with a heat exchanger on one side and a retaining surface on the other side.

The Press-Pak shown in Figure 17.10 must be mounted with 700 to 900 pounds force. The heatsink(s) for this device must be parallel to the face of the device and as smooth as the device surface, which is flat within 0.0003 inches. A swivel mounting clamp is recommended to assure parallelism. For this purpose, a special double-spring mounting clamp assembly kit with a swivel pressure stud is available from the General Electric Company. See Press-Pak specification bulletin for detailed instructions to use kit.

Figure 17.11 shows the Press-Pak installed using one of these kits.

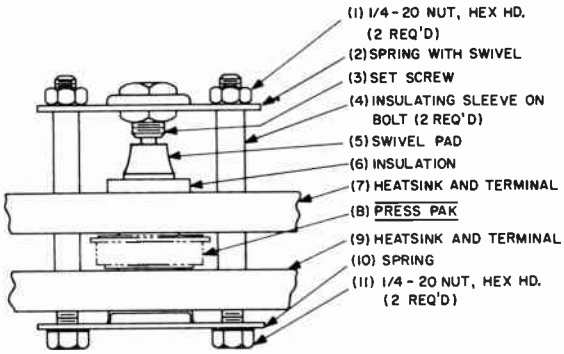


FIGURE 17.11 PROPER MOUNTING OF PRESS-PAK USING G-E MOUNTING KIT

The use of two springs puts the heatsink in compression only, without bending moments. The two nuts are finger tightened against the bolt insulation, with the setscrew free. The setscrew is finger tightened, and then tightened with an Allen wrench the specified number of turns. This provides the necessary force. The swivel pad under the setscrew assures an even distribution of pressure.

The exaggerated sketch of Figure 17.12(a) shows how a flat heat exchanger may bend under the mounting force unless supported with the second spring clamp as shown in Figure 17.11. The exaggerated sketch of Figure 17.12(b) shows that without the recommended self-leveling contact on one side of the mounting, uneven pressure is applied to the contact surface of the Press-Pak. Even a slight difference in the tightening of the two nuts can result in a markedly uneven pressure when the recommended swivel contact is not used.

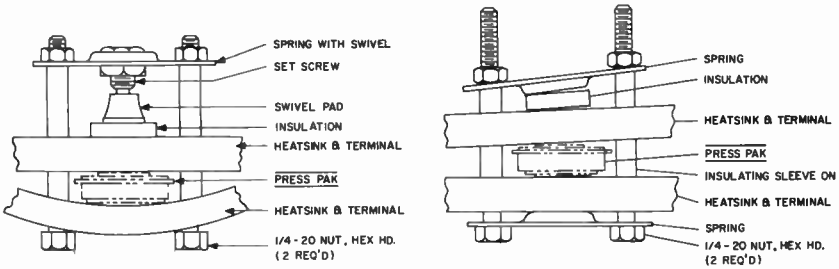


FIGURE 17.12 EXAMPLES OF IMPROPER MOUNTING OF PRESS-PAK

Although the Press-Pak is a rugged component, reasonable care in handling is recommended. Dropping, or other hard jarring, of the device can damage the silicon pellet and destroy electrical characteristics. Dents, nicks, or other distortion of the contact surfaces can also retard the flow of heat through the cooling fin, and cause the junction to overheat.

17.5 LUBRICATION OF JOINT

Any practical thermal joint will have trapped air pockets in the inevitable depressions and voids between the surfaces. Since air is a relatively poor thermal conductor, the thermal transfer can be improved by applying a thin layer of thermal lubricant to the contact interfaces before joining. In the case of stud type packages, care should be taken not to get the joint compound on the stud threads. Also, be sure there are no foreign objects in the compound, such as brush hairs. Wipe excess grease from around base of cell to help prevent dirt accumulation. Table 17.1 indicates the improvement in thermal resistance that can be expected for typical SCR packages by use of a thermal lubricant.

17.6 ELECTRICAL INSULATION OF CASE FROM HEATSINK

In some applications it is desirable to electrically insulate the semiconductor case from the heatsink. Hardware kits for this purpose are available for stud-mounted semiconductors with machine threads in the low and medium power ratings. These kits generally employ a .003 to .005 inch thick piece of mica or bonded fiberglass to electrically isolate the two surfaces, yet provide a thermal path between the surfaces. As evidenced by the data in Table 17.1, the thermal resistance of the joint may be raised as much as ten times by use of this insulation. As in the direct metal-to-metal joint, some improvement in thermal resistance can be made by using lubricant on each side of the mica.

Tests using beryllium oxide (99 per cent) for electrical insulation have shown this material to be excellent in heat transfer. Insulating a semiconductor with a ½-20 stud, using BeO (99 per cent) washers (1.00 inch OD x .52 inch ID x .125 thk) gave a stud-fin contact thermal resistance of 0.14°C/watt. Applying Penetrox 'A' to all contact surfaces decreased that thermal resistance to 0.1°C/watt.

Beryllium oxide discs are also available with one or both sides metalized. With this metallization it is possible to solder the semiconductor case, the heat exchanger, or both to the BeO disc. This technique is particularly useful with the flat-bottom press fit package. Figure 17.13 shows the drastic improvement in case-to-sink thermal impedance using the metallized BeO and solder technique.

Beryllium oxide washers in large, formed sizes and small quantities are basically somewhat expensive items. However, careful consideration should be given to the over-all economics before using any other material when electrical insulation is required. Several standard washer sizes are available from companies such as National Beryllia Corporation, Frenchtown Porcelain, or Brush Beryllium Company.

Another method used for insulating the semiconductor case from the heat exchanger is to directly solder the device to a small metal plate and then insulate that from the heat exchanger. Figure 17.14 shows this approach used with the flat-bottomed press-fit package. The SCR is soldered to a flat metal plate (say 3 or 4 square inches in area). Soldering must be accomplished below 200°C; a 60-40 (Pb-Sn) solder can be employed at about 180°C. A solder which looks quite promising for this application is "Alloy 82" from Alloys Unlimited Inc. This is a lead-tin-indium (37½-37½-25) preform of 468 mils diameter and 9.5 mils thickness. Soldering with this alloy can be accomplished at 150°C.

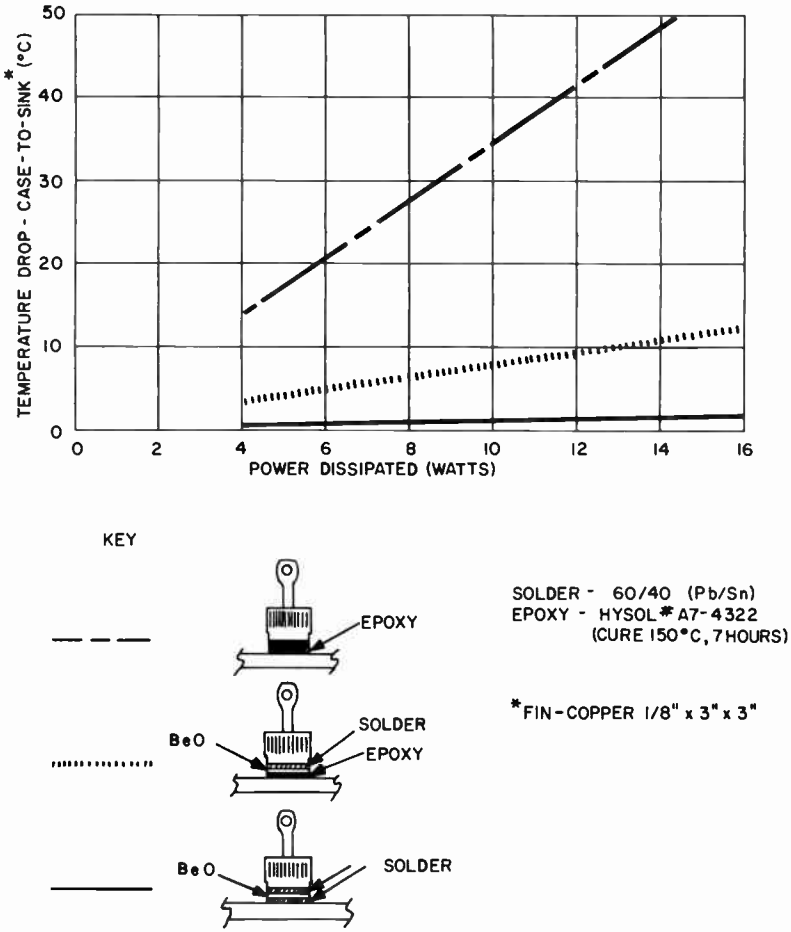


FIGURE 17.13 MOUNTING THE PRESS-FIT PACKAGE WITH BERYLLIUM OXIDE INSULATION.

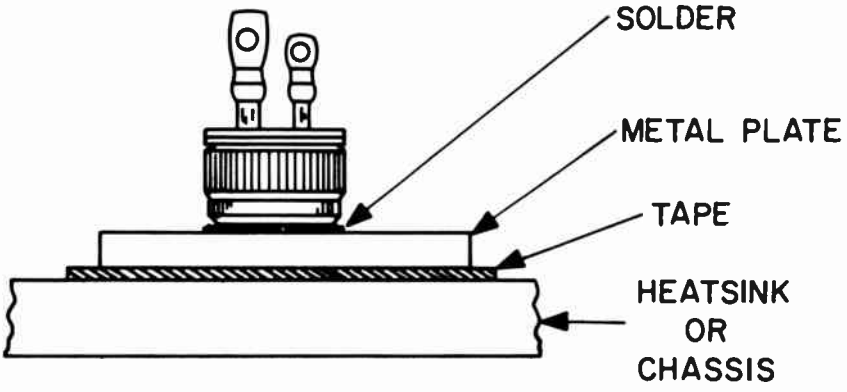


FIGURE 17.14 MOUNTING THE PRESS-FIT PACKAGE WITH TAPE INSULATION

The SCR-flatplate assembly is then mounted to the heat exchanger by means of an epoxy coated, mylar tape. The tape recommended is Scotch Brand #75. This is a one mil mylar tape with about 2 mils of epoxy (when cured) on both sides. The epoxy cures at 121°C in three hours.

The advantage of the above outlined mounting technique is that the operating heat generated at the device junction is first spread out over a large physical area before it tries to traverse the insulating medium. This reduces the total thermal resistance of that insulation.

Other techniques employing the direct use of epoxy adhesives, epoxies with a filler, and the direct use of insulating tape have been successfully employed.[4] Since in most cases a rather high price in current rating is paid in thermal resistance for insulated mounting, such mounting is not recommended for high power SCR's.

17.7 COOLING FIN DESIGN

The most common means of cooling SCR's other than lead or tab types is to mount them to a metallic cooling fin. Heat losses at the junction of the semiconductor will then flow down through the case, into the fin, and will then be dissipated to the ambient air by radiation and either free or forced convection heat transfer.

17.7.1 General

Because the mechanisms of radiation and convection are of distinctly different nature, the so-called heat transfer coefficient (h) for each effect must

Symbol	Definition	Dimensions
A	Surface Area of Fin	$in.^2$
c	Thermal Capacity	watt-sec/lb. °C
h	Heat Transfer Coefficient	watts/$in.^2$°C
k	Thermal Conductivity	watts/°C-inch
L	Length of Fin (in specified direction)	inches
q	Rate of Heat Flow	watts
T	Temperature	°C
ΔT	Temperature Difference	°C
T_S	Surface Temperature of Heatsink	°C
T_A	Ambient Temperature	°C
V	Air Velocity	ft./min.
ϵ	Radiation Surface Emissivity	—
η	Fin Effectiveness	—
θ	Thermal Resistance	°C/watt

TABLE 17.2 BASIC THERMAL UNITS

be calculated separately and combined with the fin effectiveness (η) to determine the over-all heat transfer coefficient if any degree of confidence is to be placed in the analytical design. The rate of heat flow, q, from the fin to the ambient air can be expressed as follows:

$$q = hA\eta\Delta T \tag{17.1}$$

where h = total heat transfer coefficient of the fin
A = surface area of the fin
η = fin effectiveness factor
ΔT = temperature difference between hottest point on fin and ambient

Table 17.2 lists these and other symbols used in the following discussion together with their dimensions.

A short discussion on each of the major factors in Equation 17.1 will reveal the variables on which they depend. The examples cited all apply to the same size fin and temperature conditions so that the reader can compare the relative magnitude of each of the various mechanisms of heat transfer.

It should be emphasized that while the individual equations are quite accurate when the conditions on which they are based are fulfilled in detail, the practical heatsink design will depart from the conditions to some extent because of local turbulence in the air due to mounting hardware and leads, thermal conduction down the electrical leads and the mounting for the fin, nearby radiant heat sources, chimney cooling effects caused by other heated devices above or below the cooling fins, etc. Fortunately most of these additional effects enhance rather than reduce the heat transfer. Therefore, it is common practice to disregard these fringe effects in the paper design stages except where designs are being optimized to a high degree. Even in a highly optimized design, precisely calculated values may be subjected to substantial corrections when the design is actually checked in the prototype. The final measure of the effectiveness of the cooling fin will always be the fin temperature at the case which should never be allowed to exceed the manufacturer's rating for a given load condition.

17.7.2 Radiation

For stacked fins with surface emissivity of 0.9 or more and operating up to 200°C, the radiation coefficient (h_r) can be closely approximated by the following equation:*

$$h_r = 1.47 \times 10^{-10} \epsilon (1 - F) \left(\frac{T_S + T_A}{2} + 273 \right)^3 \frac{\text{watts}}{\text{in.}^2 \text{°C}} \qquad (17.2)$$

where ϵ = surface emissivity (see Table 17.3)
F = shielding factor due to stacking ($F = 0$ for single unstacked fins)
T_S = surface temperature of cooling fin (°C)
T_A = ambient temperature (°C)

Table 17.3 indicates the wide variation in emissivity for various surface finishes. In free convection cooled applications, the radiation component of the total heat transfer is substantial, and it is therefore desirable to maximize radiation heat transfer by painting or anodizing the fin surface.

Note that oil paints regardless of color improve surface emissivity to practically an ideal level (unity).

Figure 17.15 presents Equation 17.2 in the form of a nomogram which considers the detrimental effects of stacking cooling fins. As fin spacing is reduced shielding effects become more marked, and radiation heat transfer is reduced,

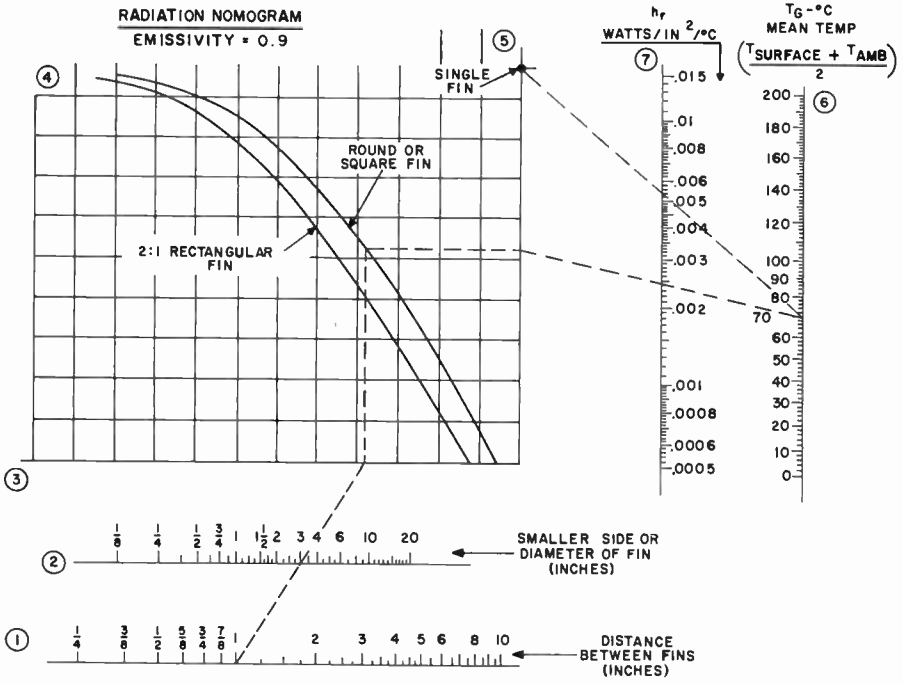


FIGURE 17.15 RADIATION NOMOGRAM (EMISSIVITY = 0.9)

Surface	Emissivity (ϵ)
Anodized Aluminum	0.7–0.9
Commercial Aluminum (Polished)	0.05
Aluminum Paint	0.27–0.67
Commercial Copper (Polished)	0.07
Oxidized Copper	0.70
Rolled Sheet Steel	0.66
Air Drying Enamel (any color)	0.85–0.91
Oil Paints (any color)	0.92–0.96
Lampblack in Shellac	0.95
Varnish	0.89–0.93

TABLE 17.3 EMISSIVITIES OF COMMON SURFACES

Example of Use of Radiation Nomogram

Given: —Stack composed of 3″ x 3″ square cooling fins
—1″ spacing between fins
—ambient temperature = 40°C
—fin surface temperature = 100°C

Problem: Determine coefficient of radiation heat transfer (h_r) and total radiation heat transfer (q_r) assuming fin effectiveness = 1. (See Section 17.7.5)

Solution: $$T_G = \frac{T_S + T_A}{2} = \frac{100 + 40}{2} = 70°C$$

Following the dashed line sequence starting at 1 for the above conditions, $h_r = .0024$ w/in. ^{2}°C.

$q_r = h_r A \Delta T = (.0024$ watts/in. ^{2}°C) (3 x 3 in.^{2}) (2 sides) (100 − 40°C) = 2.6 watts per fin.

For single unstacked fins surrounded by 40°C ambient $h_r = .0054$ watts/in. ^{2}°C by the indicated line on the nomogram.

$q_r = h_r A \Delta T = (.0054)$ (3 x 3 x 2) (100 − 40) = 5.8 watts per fin.

17.7.3 Free or Natural Convection

For vertical fins surrounded by air at sea level and at surface temperatures up to 800°C, the free convection heat transfer coefficient (h_c) can be approximated by the following equation which assumes laminar flow of the cooling medium:[2]

$$h_c = 0.00221 \left(\frac{\Delta T}{L}\right)^{0.25} \frac{\text{watts}}{\text{in.}^2\,°C} \qquad (17.3)$$

where ΔT = temperature difference between surface and ambient air (°C)

L = vertical length of fin (inches)

This equation remains conservative for fin spacing down to approximately $\sqrt[4]{L}$ inch. Figure 17.16 presents Equation 17.3 in the form of a nomogram for convenience.

*This equation can be derived from Equations 31-3 and 31-90 in Reference 1.

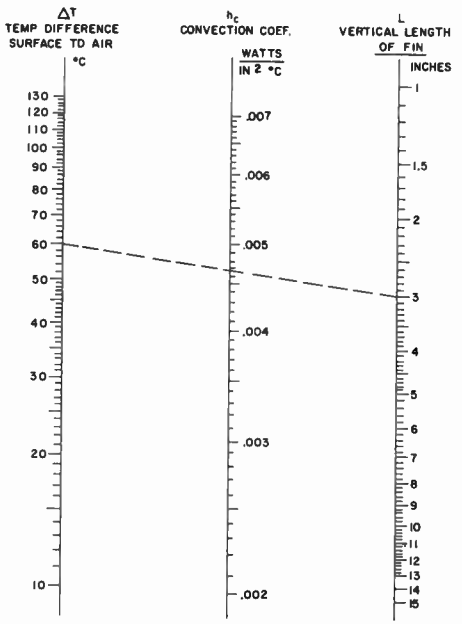


FIGURE 17.16 FREE CONVECTION NOMOGRAM (VERTICAL FINS—SEA LEVEL AIR)

Example of Use of Free Convection Nomogram

Given: —3" x 3" square cooling fin
—ambient temperature = 40°C
—fin surface temperature = 100°C

Problem: Determine free convection coefficient of heat transfer (h_c) and total convection heat transfer (q_c) assuming fin effectiveness = 1. (See Section 17.7.2).

Solution: $\Delta T = T_S - T_A = 100 - 40 = 60°C$
$L = 3$ inches
As shown by dashed line on nomogram, $h_c = .00465$ watts/in. ^{2}°C.
$q_c = h_c A \Delta T = (.00465$ w/in. ^{2}°C) (3 x 3 in.^{2}) (2 sides) (100 − 40°C) = 5.02 watts.

Altitude derating factors for the free convection heat transfer coefficient are shown in Figure 17.17 for fins from ½ inch to 2 feet on a side.

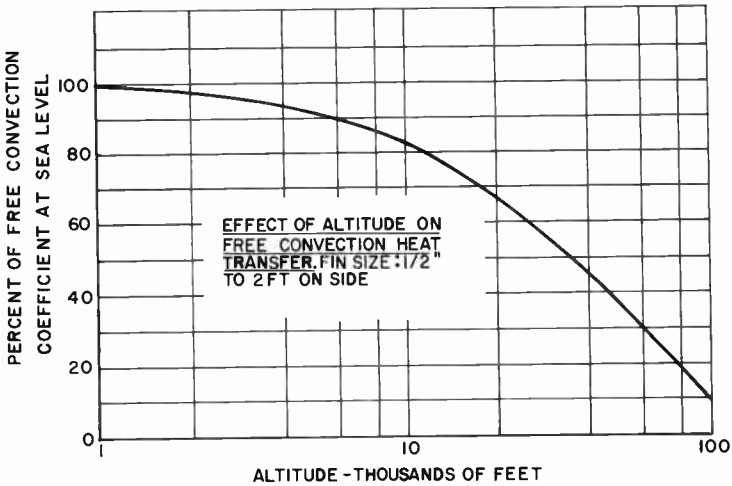


FIGURE 17.17 EFFECT OF ALTITUDE ON FREE CONVECTION HEAT TRANSFER

17.7.4 Forced Convection

When air is moved over cooling fins by external mechanical means such as fans or compressors, heat transfer is improved and the convection heat transfer coefficient can be approximated by the following equation:*

$$h_c = 11.2\sqrt{\frac{V}{L}} \times 10^{-4} \text{ watts/in. } ^2\text{°C} \qquad (17.4)$$

where V = free stream linear cooling air velocity across fin surface (ft./min.)

L = length of fin parallel to air flow (inches)

This equation is based on laminar (non-turbulent) air flow which exists for smooth fin lengths up to $L \cong C/V$, where C is a constant given in Table 17.4 for various air temperatures. For $L > C/V$, air flow becomes turbulent and heat transfer is thereby improved. Turbulent air flow and the resultant impovement in heat transfer may be achieved for shorter L's by physical projections from the fin such as wiring and the rectifier cell itself. However, turbulence increases the power requirements of the main ventilating system. Minimum spacing for the above is $B\sqrt{\frac{L}{V}}$ inches where B is also a constant given in Table 17.4.

Air Temperature	B	C
25°C	3.4	37,000
55°C	3.8	45,000
85°C	4.1	52,000
125°C	4.5	63,000
150°C	4.7	70,000

TABLE 17.4 LAMINAR FLOW LIMITATIONS

*This is accurate within 1% of Equation 7.48, Reference 2, p. 149 for air properties up to 250°C.

Figure 17.18 presents a nomogram for convenience in solving the forced convection equation, Equation 17.4 above.

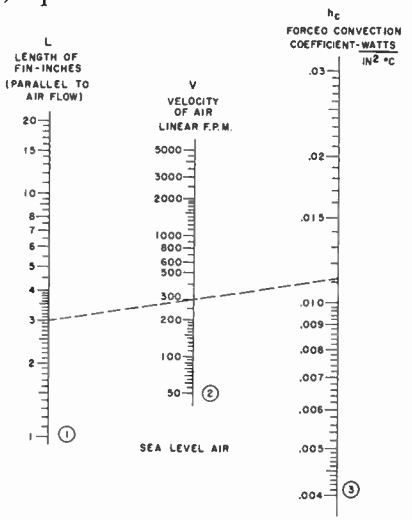


FIGURE 17.18 FORCED CONVECTION NOMOGRAM

Example of Use of Forced Air Convection Nomogram

Given: —3″ x 3″ square cooling fin
—air velocity = 300 linear FPM
—ambient air = 40°C
—fin surface temperature = 100°C

Problem: Determine forced convection heat transfer coefficient (h_c) and total convection heat transfer (q_c) assuming fin effectiveness = 1.

Solution: L = 3 inches, V = 300 LFPM
As shown on dashed line on nomogram, h_c = .011 watt/in. ^{2}°C.
$q_c = h_c A \Delta T$ = (.011 watts/in. ^{2}°C) (3 x 3 in.^{2}) (2 sides) (100 − 40°C) = 11.9 watts.

17.7.5 Fin Effectiveness

For fins of thin material, the temperature of the fin decreases as distance from the heat source (the SCR) increases due to effects of surface cooling. Thus calculations of heat transfer, such as those above, which are based on the assumption that the fin is at a uniformly high temperature are optimistic and should be corrected for the poorer heat transfer which exists at the cooler extremities of the fin. The correction factor which is used is called fin effectiveness (η). η is defined as the ratio of the heat actually transferred by the fin, to the heat that would be transferred if the entire fin were at the temperature of the hottest point on the fin. The hottest spot, of course, is adjacent to the stud of the SCR. The effectiveness depends on the length, thickness, and shape of the fin, on the total surface heat transfer coefficient h,

and on the thermal conductivity k of the fin material. As defined in Equation 17.1, the total actual heat transfer may be calculated by multiplying the fin effectiveness factor by the total surface heat transfer (determined by adding the radiation and convection heat transfer as calculated in the examples above).

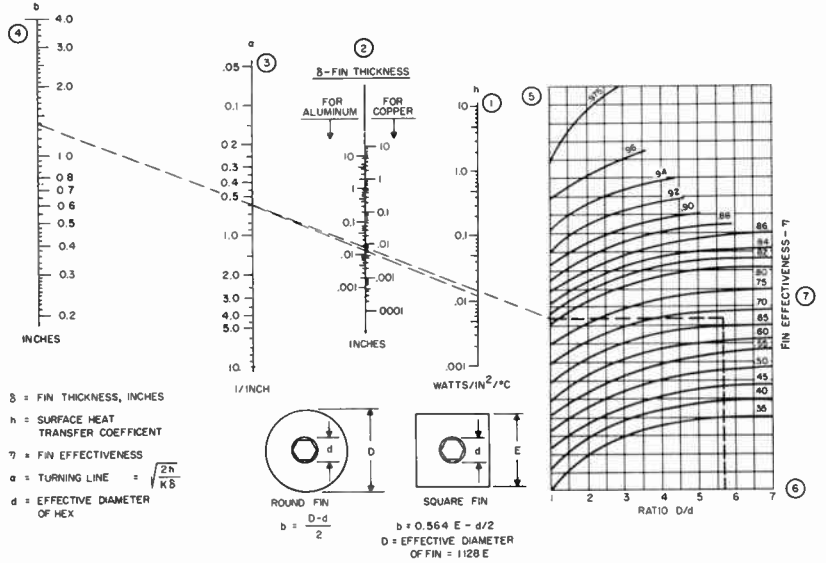


FIGURE 17.19 FIN EFFECTIVENESS NOMOGRAM FOR FLAT, UNIFORM THICKNESS FIN.

Fin effectiveness can be computed by means of the nomogram shown in Figure 17.19. The typical sequence of proceeding through the nomogram is indicated by the encircled numbers adjacent to the scales.

Example of Use of Fin Effectiveness Nomogram

Given: —Stack composed of 3" x 3" square painted aluminum fins, each 1/64 inch thick.
—Effective stud hex diameter d = 0.59 inch.
—1 inch spacing between fins
—300 LFPM air velocity
—Fin temperature at stud = 100°C.
—Ambient air temperature = 40°C.

Problem: Determine total heat transfer of each fin.

Solution:

1st Step: Determine total heat transfer coefficient. Radiation heat transfer coefficient h_r = .0024 w/in. ^{2}°C per example in Section 17.7.2. Convection heat transfer coefficient h_c = .011 w/in. ^{2}°C per example in Section 17.7.4.
Total heat transfer coefficient = $h_r + h_c$ = .0024 + .011, h = .0134 w/in. ^{2}°C.

2nd Step: Determine fin effectiveness factor from nomogram.

$$b = 0.564E - d/2 = (0.564)\,(3) - \frac{0.59}{2} = 1.39''$$

$$D/d = \frac{1.128 \times 3}{0.59} = 5.64$$

For h = .0134 w/in. ^{2}°C and thickness δ = .0155 inch. α = 0.58 as indicated by the dashed line on the nomogram. Through b = 1.39 and α = 0.58, a line is extended to the graph where D/d = 1. Projecting horizontally on this graph to D/d = 5.64, η is found to be 0.67.

3rd Step: Determine total heat transfer.

Total heat transfer $q = hA\eta\Delta T$

$q = (.0134\ w/in.^2°C)\ (18\ in.^2)\ (0.67)\ (100 - 40°C)$

$= 7.2$ watts per fin.

For fin materials other than copper or aluminum, use the "copper" scale on the nomogram by multiplying the actual fin thickness by the ratio of the thermal conductivity of the material being considered to the thermal conductivity of copper. Thus, for a ⅛ inch *steel* fin, enter axis 2 on the *copper* scale at 0.125 inch x 1.16/9.77 = 0.015 inch. Thermal conductivities of several commonly used fin materials are given in Table 17.5.

Material	Density (lbs/in.^{3})	Heat Capacity (c) (watt-sec./lb. °C)	Thermal Conductivity (k) (watts/in. °C)
Aluminum	0.098	407	5.23
Brass (70 Cu, 30 Zn)	0.30	179	2.70
Copper	0.32	175	9.77
Steel	0.28	204	1.16

TABLE 17.5 THERMAL PROPERTIES OF HEATSINK MATERIALS

In general, it will be found that fin thickness should vary approximately as the square of the fin length in order to maintain constant fin effectiveness. Also, a multi-finned assembly will generally have superior fin effectiveness and will make better use of material and weight than a single flat fin.

17.7.6 Typical Example of Complete Fin Design

Given: —Four C35 SCR's with 9/16" hex and 1/4"–28 thread are operated in a single-phase bridge at 10 amperes DC maximum each. The specifications for this rectifier indicate that at this current level each SCR will develop 16 watts of heat losses at its junction and that for satisfactory service at this current level, the stud temperature should be maintained below 92°C. The maximum ambient temperature is 40°C and free convection conditions apply.

Problem: Design a stack of fins to adequately cool the four SCR's in this bridge circuit.

Solution:

1st Step: Determine maximum allowable fin temperature at radius of stud hex. From Table 17.1, the thermal resistance from stud to fin for a joint with lubricant is 0.35°C/watt maximum. The maximum fin temperature therefore must not exceed 92°C − (0.35°C/watt x 16 watts) = 86°C.

2nd Step: Estimate required fin designs based on space available: 6" x 6" painted vertical fins at one inch spacing. Material .08 inch thick steel. Assume all cell losses are dissipated by fin.

3rd Step: Determine surface heat transfer coefficient and fin effectiveness of estimated fin design:

Radiation (from Nomogram in Figure 17.15)

$$T_G = \frac{86 + 40}{2} = 63°C \qquad h_r = .00145 w/in.^2 °C$$

Free Convection (from Nomogram in Figure 17.16)

$$\Delta T = 86 - 40 = 46°C \qquad h_c = .0037 w/in.^2 °C$$

$$h_{total} = .0052 w/in.^2 °C$$

Fin Effectiveness (from Nomogram in Figure 17.19)

$D = 1.128E = 1.128 \times 6 = 6.768$

$d = 0.59$ from Table 17.1

$$b = 0.564E - d/2 = 0.564 \times 6 - \frac{0.59}{2} = 3.089$$

$$D/d = \frac{6.768}{0.59} = 11.5; \quad \delta Cu = (.08)\frac{1.16}{9.77} = .0095 \text{ in.}$$

Using these parameters in the nomogram, $\eta = 55\%$.

4th Step: Determine total heat transfer for estimated fin.

$q = hA\eta\Delta T$

$= (.0052)$ (6 x 6 in.^{2}) (2 sides) (0.55) (86 − 40°C)

$= 9.7$ watts

5th Step: Determine error in approximation. Re-estimate fin requirements, and recalculate total heat transfer. In this example, the capabilities of the initial fin design fell considerably below the requirements of 16 watts. To sufficiently increase the heat transfer, a ¼" thick copper fin would be needed. Alternately a thinner fin of larger area could be used.

17.8 MEASUREMENT OF CASE TEMPERATURE

Heatsink design should be checked in the prototype equipment. A 10 or 12 mil thermocouple wire should be used. A copper-constantan thermocouple junction is suggested. The thermocouple junction should be carefully soldered to the SCR case as indicated in Figure 17.20. The temperature at this point closely approximates the temperature of the case immediately below the junction, which is usually inaccessible once the device is mounted to a fin. The point of measurement on the stud should be shielded from any forced air which might cause localized cooling, and the leads should be kept out of any flow of cooling air since they can provide a heat flow path which will lower the temperature at the thermocouple junction.

Unless carefully calibrated leads and instruments are available, a thermocouple bridge rather than a pyrometer should be employed. Care should be taken to keep the thermocouple leads out of electric fields that might induce error voltages in the leads.

As an alternative to using a thermocouple, temperature indicating waxes and paints bearing such trademarks as "Thermocolors" (manufactured by Curtiss-Wright Research Corporation) and "Tempilaq" (manufactured by Tempil Corporation, New York City) can be used to indicate whether the case exceeds a specific level of temperature. Careful attention should be given to the manufacturer's instructions for using this type of temperature indicator to prevent mis-application and errors. Temperature indicating paints and waxes are particularly useful in high electrical fields where substantial errors may occur in electrical measurement techniques or where the fin is inaccessible for thermocouple leads during the test, such as on the rotor of a rotating machine. Care must be taken in applying paints so their presence does not materially affect the emissivity of the surface.

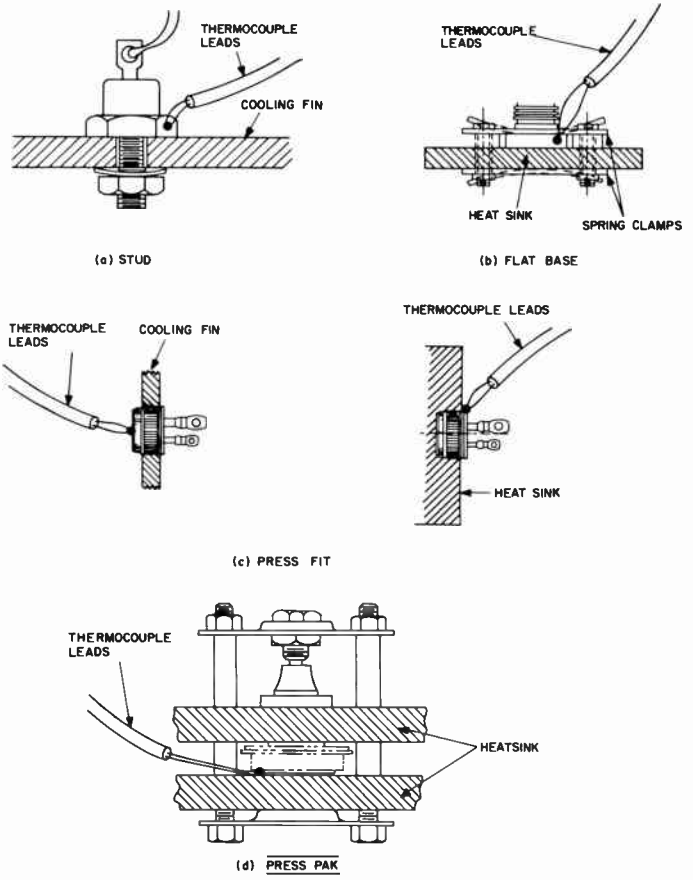


FIGURE 17.20 PREFERREO LOCATION FOR MOUNTING THERMOCOUPLE FOR CASE TEMPERATURE MEASUREMENTS.

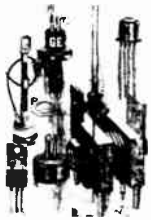
Use of the foregoing procedures to produce a well-engineered cooling fin design for SCR's can pay big dividends in reliable operation, low material costs, and minimum space and weight requirements.

REFERENCES

1. "Heat Transfer," Vol. II, Jakob, John Wiley & Sons, Inc., New York, New York, 1957.
2. "Principles of Engineering Heat Transfer," Giedt, VonNostrand Co., New York, New York, 1957, p. 218.
3. "Heat Transmission," McAdams, McGraw-Hill Book Company, New York, New York, 1942.
4. "A Variety of Mounting Techniques for Press-Fit SCR's and Rectifiers," J. C. Hey, General Electric Company, Auburn, N. Y. Application Note 200.32.*

*Refer to Chapter 22 for availability and ordering information.

18 SCR RELIABILITY



18.1 INTRODUCTION

Reliability is not new as a concept, but the language and techniques relating to its treatment have continued to develop as technology has advanced and become increasingly complex. The need to define reliability as a product characteristic has expanded as the newer technologies have moved from laboratory to space to industry to home. The steel mill calculates the cost of down time in thousands of dollars per minute; the utility is sensitive to the low tolerance level of its customers to interruptions in service; the manufacturer of consumer equipment relies on a low incidence of in-warranty failures to maintain profitability and reputation.

The complexity of equipment, on the one hand, and the development of new components on the other, have forced industry to invest considerable effort in finding means for controlling and predicting reliability. The efforts, in many cases, were accelerated by the desire of the military to evaluate, and improve where necessary, the reliability of new devices, which offered the promise of improvements in size, weight, performance, and reliability in aerospace and weapons systems. One new device so favored was the SCR, the first of the thyristor family of devices to be commercially available.

The first SCR, the General Electric C35, was successfully qualified to the first SCR military specification only two years after it was made commercially available. At approximately that same time, a specification was finalized to which this same device was qualified as part of the highly publicized Minuteman missile high reliability program. These programs, and others that followed, contributed a great deal to the knowledge and understanding of the inherent reliability of semiconductors such as the SCR, and of those factors in design, rating, process control and application that effectively determine the reliability achieved. As a result the General Electric Co. has been able, in a relatively brief span of time, to develop and produce a wide variety of thyristor devices tailored to the particular needs of various fields of application. The variety of thyristor type devices offered by the General Electric Co. at this time includes the SCR, the SCS, the SUS, the SBS, the light-activated SCR and SCS, and the triac. Chapter 21 indicates the broad range of current and voltage available in these devices. Applications thus far are so diverse as to include automobiles, computers, missiles, spacecraft and aircraft, industrial controls, lighting systems, hand tools, and household appliances.

18.2 WHAT IS RELIABILITY?

Reliability may be defined as the probability of performing a specific function under given conditions for a specific period of time. Reliability is a measure of time performance as opposed to quality, which is a measure of conformance to specified standards at a given point in time. Although system reliability is influenced by factors such as the selection and design of circuits,

discussion in this chapter is limited to the effects of component part reliability. In addition, the assumption is made that the parts are properly applied, and that they are not subject to stresses that exceed rated capability.

18.3 MEASUREMENT OF RELIABILITY

In the case of large systems, the common unit of reliability measurement is MTBF, or Mean Time Between Failures. MTBF expresses the average time in hours that the system operates between failures, providing a basis for estimating the cost of system maintenance. The MTBF measurement further contributes in the establishment of preventive maintenance scheduling and in estimating productivity as a function of availability, which is that percentage of time that the system can be expected to be productively operable.

The reliability of a system is based on the summation of the reliabilities of all the parts that make up the system. This process is made complex by factors such as the need for weighting based on the effect on total system performance of the failure of a particular component or circuit, and the assignment of correction factors to compensate for stress levels applied. If these complexities are ignored, and if a further simplification is made in the form of the assumption that the failure rates of the components are constant over time, then Failure Rate is the reciprocal of MTBF, and system MTBF is the reciprocal of the sum of the Failure Rates of the component parts.

18.3.1 Failure Rate

An individual component part, such as a semiconductor, does not lend itself to reliability measurement in the same manner as does a system. For this reason, the statistical approach to estimating device reliability is to relate the observed performance of a sample quantity of devices to the probable performance of an infinite quantity of similar devices operated under the same conditions for a like period of time. The statistical measurement is based on unit hours of operation, using a sampling procedure whose derivation takes into account the resolution with which the sample represents the population from which it was drawn and the general pattern of behaviour of the devices observed with time.

The sampling plan most commonly applied to semiconductors is given as Table C-1 of Mil-S-19500D, and is shown here as Figure 18.1. "Failure Rate" is a commonly used term, generally applied interchangeably with LTPD (Lot Tolerance Percent Defective), which is also called "Lambda" when used in connection with a one thousand hour test period. The table given permits calculation of failure rate at the ninety percent confidence level as a function of the number of devices observed and the number of failures occurring.

According to the sampling plan, satisfactory operation of 231 devices for 1000 hours is indicative that the failure rate is no greater than 1.0% per 1000 hours at a 90% confidence level. If it were desired to demonstrate a maximum failure rate of 0.1% per 1000 hours, the minimum sample would be 2,303 devices with no failures allowed. This could also be demonstrated with a sample of 3,891 samples, allowing one failure. In either case, a successful test would be the equivalent of demonstrating an MTBF of 1,000,000 hours for a system made up solely of the devices under test. Several points become evident in these observations:

(a) It would be extremely difficult to perform an accurate test demonstration to verify failure rate below even 1.0% since the test equipment and instrumentation must have a still greater MTBF in order not to adversely affect the test results. The problem compounds as the failure rate being tested for is lowered. Not only is test equipment complexity increased, but its MTBF must be increased at the same time!

(b) The terminology "Failure Rate" is perhaps a poor choice of words. To the reliability engineer it relates the performance of a limited number of observations to the probable performance of an infinite population. To those not familiar with the statistics used, it unfortunately conveys the impression of actual percent defective.

18.4 SCR FAILURE RATES

Even at the early stages of development and application, it was apparent that the SCR would permit the improvement of equipment reliability. In 1962, Mil-HDBK-217 included the following failure rate estimates for devices operated at rated power:

semiconductor diodes—0.1% per 1000 hours
transistors—0.2% per 1000 hours
single receiving tubes—0.2% to 0.9% per 1000 hours
single power tubes—1.0% to 2.0% per 1000 hours
composition resistors—0.045% per 1000 hours
transformers, magnetic amplifiers, and coils (Class H insulation, 0°C to 90°C hot spot temperature)—0.5% per 1000 hours

For purposes of presentation, SCR's are not treated separately in Mil-HDBK-217, but are included with the semiconductor diodes. Two possible reasons that the SCR could be categorized with the diode rather than the transistor are: (1) the SCR has a geometry that is usually somewhat less susceptible to the degrading effects of surface phenomena than the transistor. (2) The SCR is a bistable rather than a linear device, and is therefore more tolerant of possible parameter degradation.

From 1962 through 1965, a cumulative total of approximately 500 sample C35 SCR's were subjected to full load intermittent operation of 1000 hours in formal lot acceptance testing to Mil-S-19500/108. Of these, none were observed to be failures to the specification end point limits. The calculation of failure rate based on these results indicates the failure rate to be no more than 0.46% per 1000 hours at 90% confidence.

In Mil-HDBK-217, the end point limits used to define failure were: an open; a short; and a radical departure from initial characteristics in a short period of time. The end point limits specified by Mil-S-19500/108 are essentially; an increase of forward or reverse blocking current beyond twice the initial acceptance limit; and an increase of gate current to trigger beyond 110% of the initial acceptance limit. If it is conservatively estimated that as many as 10% of observed failures are catastrophic, then a factor of ten can be applied to the failure rate calculated against the drift limits of Mil-S-19500/108. This allows a more direct comparison with the projection of Mil-HDBK-217. Applying this factor, the above calculated maximum failure rate is reduced to 0.046% per 1000 hours at 90% confidence. Even were the failure rate of semiconductors constant rather than decreasing with time, this would still represent an MTBF of 2,150,000 hours.

Minimum size of sample to be tested to assure, with o 90 percent confidence, o Lot Tolerance Percent Defective or λ no greater than the LTPD specified. The minimum quality (approximate AQL) required to accept (on the average) 19 of 20 lots is shown in parenthesis for information only.

	Maximum Percent Defective (LTPD) or λ (1)	20	15	10	7	5	3	2	1.5	1	0.7	0.5	0.3	0.2	0.1
Rejection Number	Acceptance Number	Minimum Sample Sizes													
1	0	11 (0.46)	15 (0.34)	22 (0.23)	32 (0.16)	45 (0.11)	76 (0.07)	116 (0.04)	153 (0.03)	231 (0.02)	328 (0.02)	461 (0.01)	770 (0.007)	1152 (0.005)	2303 (0.002)
2	1	18 (2.0)	25 (1.4)	38 (.94)	55 (.65)	77 (.46)	129 (.28)	195 (.18)	258 (.14)	390 (.09)	555 (.06)	778 (.045)	1298 (.027)	1946 (.018)	3891 (.009)
3	2	25 (3.4)	34 (2.24)	52 (1.6)	75 (1.1)	105 (.78)	176 (.47)	266 (.31)	354 (.23)	533 (.15)	759 (.11)	1065 (.080)	1777 (.046)	2662 (.031)	5323 (.015)
4	3	32 (4.4)	43 (3.2)	65 (2.1)	94 (1.5)	132 (1.0)	221 (.62)	333 (.41)	444 (.31)	668 (.20)	953 (.14)	1337 (.10)	2228 (.061)	3341 (.041)	6681 (.018)
5	4	38 (5.3)	52 (3.9)	78 (2.6)	113 (1.8)	158 (1.3)	265 (.75)	398 (.50)	531 (.37)	798 (.25)	1140 (.17)	1599 (.12)	2667 (.074)	3997 (.049)	7994 (.025)
6	5	45 (6.0)	60 (4.4)	91 (2.9)	131 (2.0)	184 (1.4)	308 (.85)	462 (.57)	617 (.42)	927 (.28)	1323 (.20)	1855 (.14)	3099 (.084)	4638 (.056)	9275 (.028)
7	6	51 (6.6)	68 (4.9)	104 (3.2)	149 (2.2)	209 (1.6)	349 (.94)	528 (.62)	700 (.47)	1054 (.31)	1503 (.22)	2107 (.155)	3515 (.093)	5267 (.062)	10533 (.031)
8	7	57 (7.2)	77 (5.3)	116 (3.5)	166 (2.4)	234 (1.7)	390 (1.0)	589 (.67)	783 (.51)	1178 (.34)	1680 (.24)	2355 (.17)	3931 (.101)	5886 (.067)	11771 (.034)
9	8	63 (7.7)	85 (5.6)	128 (3.7)	184 (2.6)	258 (1.8)	431 (1.1)	648 (.72)	864 (.54)	1300 (.36)	1854 (.25)	2599 (.18)	4334 (.108)	6498 (.072)	12995 (.036)
10	9	69 (8.1)	93 (6.0)	140 (3.9)	201 (2.7)	282 (1.9)	471 (1.2)	709 (.77)	945 (.58)	1421 (.38)	2027 (.27)	2842 (.19)	4739 (.114)	7103 (.077)	14206 (.038)
11	10	75 (8.4)	100 (6.3)	152 (4.1)	218 (2.9)	306 (2.0)	511 (1.2)	770 (.80)	1025 (.60)	1541 (.40)	2199 (.28)	3082 (.20)	5147 (.120)	7704 (.08)	15407 (.04)

(1) The life test failure rate lambda (λ) shall be defined os the LTPD per 1000 hours.

FIGURE 18.1 LAMBOA SAMPLING PLAN AT 90% CONFIDENCE

The stability of SCR parameters over an extended period was demonstrated by a test, initiated in 1960, that employed some of the first commercially produced devices. The conditions imposed were random, roughly simulating the conditions such devices might be exposed to over a long period of time in a derated application. Temperature cycling, storage at various ambient temperatures, and sporadic short term operation at low current levels essentially constituted the test conditions.

Forty-nine devices were started into the test cycle, of which three became early failures. One of the failures resulted from a mechanical imperfection, the cause for which was subsequently eliminated through design improvement. The other two were analyzed to be the result of leaks in the hermetic seal. Refinements in housing fabrication and final sealing techniques plus the development of improved sensitivity leak detection methods have since provided effective control over the occurrence of this type of defect.

Observations of the forty-six devices that remained on test indicate that the most significant characteristic being monitored was forward blocking current. Though it is difficult to evaluate the degree of instrumentation error present, it is reasonable to assume that some actual change in blocking current was experienced with several of the devices. Figures 18.2a and 18.2b show percentile distributions of forward and reverse blocking currents to twelve thousand, five hundred hours of test time.

Figures 18.2c, 18.2d, 18.2e, 18.2f and 18.2g show percentile distributions of gate trigger current, gate trigger voltage, on voltage, holding current, and forward breakdown voltage of the same devices over the same test interval. Because of the sensitivity of these tests to measurement error, actual variances with time are considered to be below the resolution of available instrumentation.

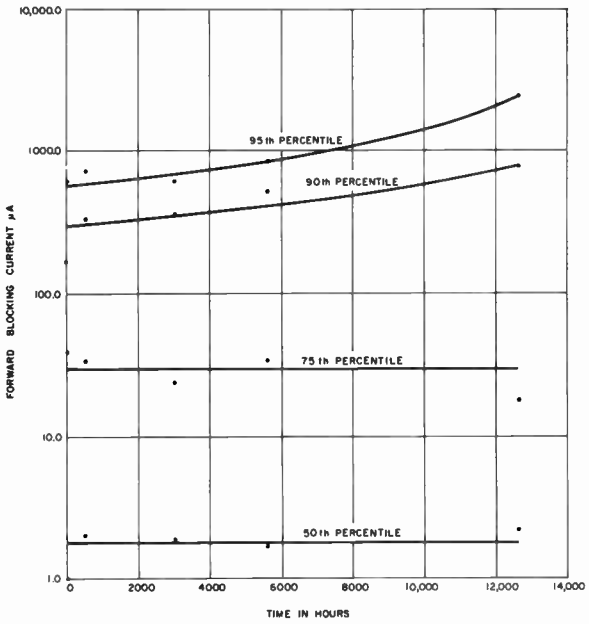


FIGURE 18.2a FORWARD BLOCKING CURRENT (I_{FO}) VERSUS TIME—C35

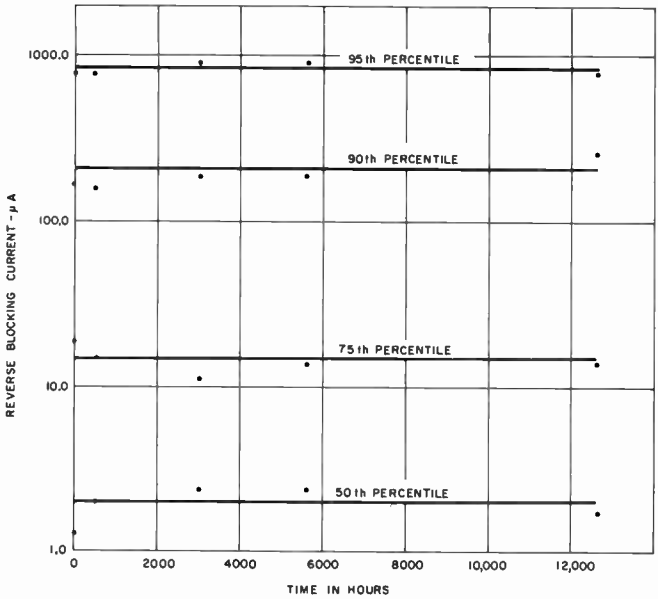


FIGURE 18.2b REVERSE BLOCKING CURRENT (I_{ro}) VERSUS TIME—C35

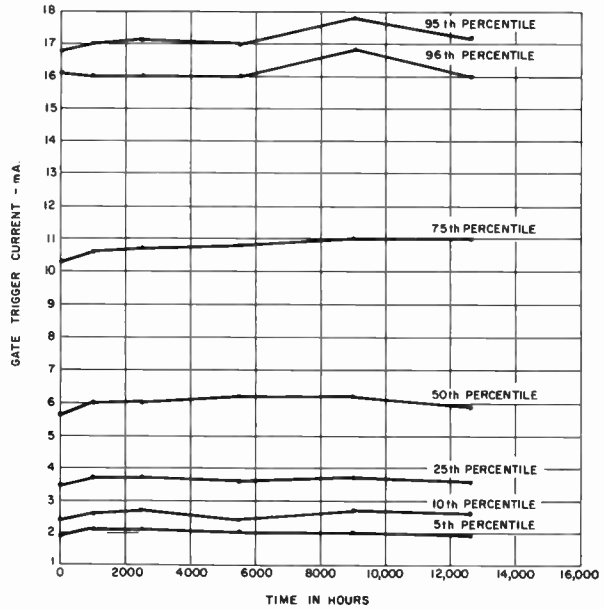


FIGURE 18.2c GATE TRIGGER CURRENT (I_{gt}) VERSUS TIME—C35

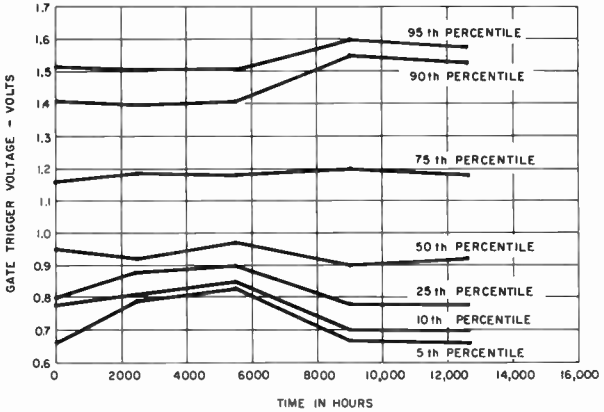


FIGURE 18.2d GATE TRIGGER VOLTAGE (V_{gt}) VERSUS TIME—C35

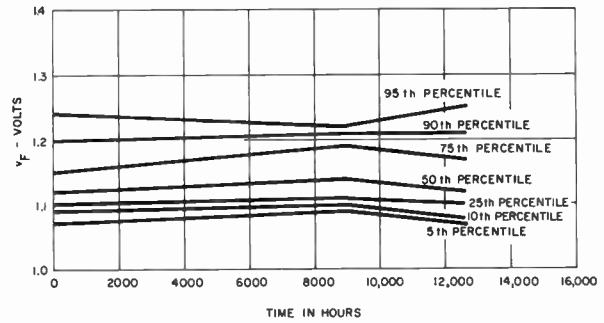


FIGURE 18.2e INSTANTANEOUS ON VOLTAGE VERSUS TIME—C35

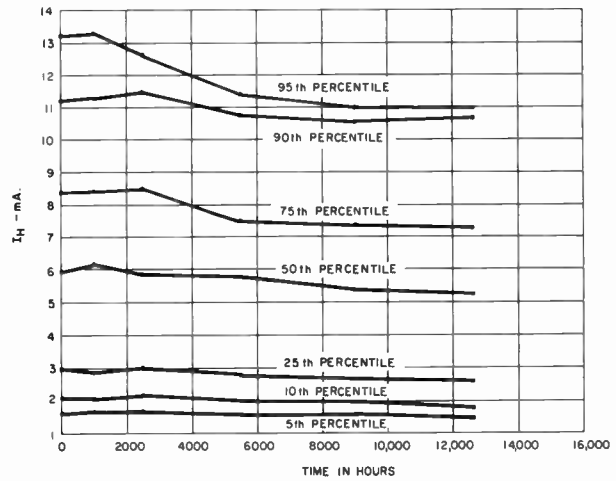


FIGURE 18.2f HOLDING CURRENT (I_h) VERSUS TIME—C35

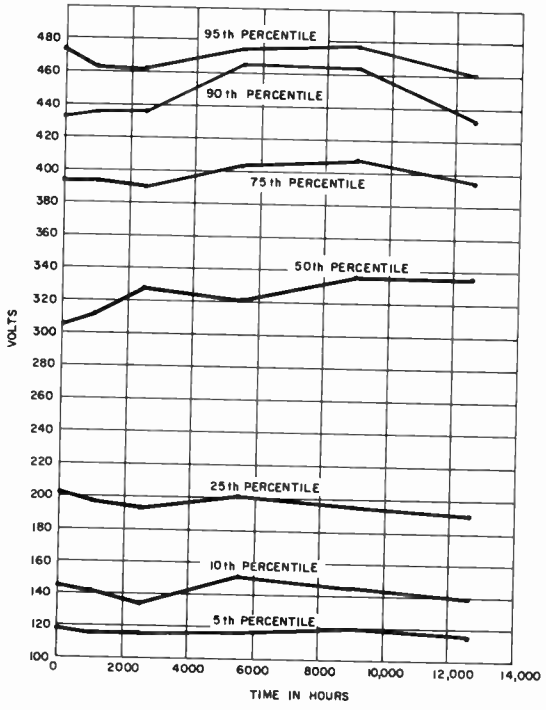


FIGURE 18.2g FORWARD BREAKOVER VOLTAGE (V_{BR})$_{FO}$ VERSUS TIME—COMBINED SAMPLE OF C35F AND C35A

The true measurement of reliability can only be made on the basis of performance in the field. There are, unfortunately, no adequate means for the component manufacturer to gather unit hour data on devices in the field for failure rate analyses. It is, however, significant to note the rapid acceptance of the SCR in such traditionally conservative industries as steel, aluminum, and paper, where devices and systems must be well proven before they are used. This approach is necessary because of the extremely close relationship between product cost and equipment reliability and efficiency. In these industries alone, it is estimated that 500,000 kilowatts of SCR controlled systems were installed or purchased from 1962 through 1965.

18.5 DESIGNING SCR'S FOR RELIABILITY

The design of reliable devices is concerned with the assurance that performance related characteristics remain within specified tolerances over the useful life of the devices. This relates particularly to thermal and mechanical design.

In the case of thermal design, the stability of thermal transfer characteristics are important for the reason that junction temperature is the major application limitation. The deterioration of the thermal path can lead to thermal runaway and device destruction. Interface materials scientifically selected for matched coefficients of expansion compatible with the rated range of temperatures are necessary to reduce the likelihood of metal fatigue.

Mechanical reliability requires the use of rigid assemblies of low mass, low moments of inertia, and the elimination of mechanical resonances in the normal ranges of vibration and shock excitation. Equally critical is the design of the protection of the junction surface, whether it be hermetic seal or passivation. Since degradation failures are mainly manifestations of changes at the junction surface, reliability is closely related to the integrity of the surface protection.

Continuing research and development are constantly expanding technologies that permit the use of lower cost materials and processes in the production of semiconductor devices by limitation of the maximum rating rather than at the expense of reliability. The temperature range of the C30, for example, is limited to −40°C to +100°C. Hence it need only be capable of performing over a maximum temperature range of 140°C. The C35, by contrast, has a storage rating from −65°C to +150°C and must perform reliably over a range of 215°C, placing a greater demand on both the glass to metal seal of the package and the mechanical interfaces in the thermal path.

Lower costs can also be accomplished through new techniques, as exemplified by the C106. Effective passivation and the development of a compatible encapsulant have eliminated the need for glass to metal hermetic seals. This in turn has made possible lower cost high volume processing techniques without the compromise of reliability.

18.6 PRODUCTION FOR RELIABILITY

The complete manufacturing process must be carefully designed and controlled if all design criteria, including reliability, are to be maintained in volume production. Certain aspects of the process allow a greater degree of opportunity than others, to optimize for the achievement of reliability criteria.

MATERIALS—Complete and properly detailed material specifications are an obvious basic necessity. Also important, however, are adequate means for thorough evaluation of the materials both prior to and, as in the case of gases, during their use. The necessary facilities are extensive and often quite sophisticated. They provide the ability to perform electrical, mechanical, physical, chemical, and environmental evaluations.

WORKMANSHIP—Rigid test and inspection standards throughout the process provide an effective means for monitoring controls. The human element is ever present, even in the most automated of processes, and rigid standards of workmanship help to instill a sense of urgency in the operators for the maintenance of the necessary degree of control.

TOOLS—The tooling and equipment used in the processing and fabrication of the semiconductor device can make an increased contribution to reliability of the completed device if their design is optimized for ease of set-up, easy maintainability, repeatability, and simplicity of operation to minimize or eliminate operator judgment.

TEST AND INSPECTION—The design and efficient implementation of in-process inspections and device testing provides for positive monitoring of the effectiveness of controls, with a minimum time lag for the institution of immediate corrective action when the need is indicated. The testing may include electrical tests in both the sub-assembly and completed stages, as well as environmental and electrical stressing of the completed devices.

18.7 FAILURE MECHANISMS

Failure mechanisms are those chemical and physical processes which result in eventual device failure. The kinds of mechanisms that have been observed in the semiconductor classification of component device are shown in the table of Figure 18.3. Also shown in the table are those kinds of stresses to which each mechanism is likely to respond.

If more than a few such failure mechanisms are, to any significant degree prevalent in a given device type from a given process, it would not be reasonable to expect to achieve the degrees of reliability that have been demonstrated by many semiconductors. The dominant mechanisms to which a device type may be susceptible will vary according to the peculiarities of the design and fabrication process of that device.

STRESS / FAILURE MECHANISM	MECHANICAL				TEMPERATURE			ELECTRICAL				MISCELLANEOUS			
	STATIC FORCE	SHOCK	VIBRATION	PRESSURE (FLUID)	STATIC	SHOCK	CYCLING	VOLTAGE	CURRENT	POWER (CONTINUOUS)	POWER (CYCLED)	CORROSION	ABRASION	HUMIDITY	RADIATION
STRUCTURAL FLAWS – WEAK PARTS	●	●	●	●	●	●	●			●	●				
– WEAK CONNECTIONS	●	●	●	●	●	●	●			●	●				
– LOOSE PARTICLES		●	●				●				●				
– THERMAL FATIGUE						●	●				●				
ENCAPSULATION FLAWS				●		●	●			●		●	●	●	
INTERNAL CONTAMINANTS – ENTRAPPED FOREIGN GASES					●		●								
– OUTGASSING					●		●								
– ENTRAPPED IONIZABLE CONTAMINANTS					●			●							
– BASE MINORITY CARRIER TRAPPING					●				●						
– IONIC CONDUCTION					●		●	●	●	●					
– CORROSION					●			●	●	●					
MATERIAL ELECTRICAL FLAWS – JUNCTION IMPERFECTION								●	●	●					
METAL DIFFUSION					●					●					
SUSCEPTABILITY TO RADIATION															●

FIGURE 18.3 FAILURE MECHANISMS AND ASSOCIATED STRESSES

18.7.1 Structural Flaws

Structural flaws are generally considered to be the result of weak parts, discrepancies in fabrication, or inadequate mechanical design. Various in-process tests performed on the device, such as forward voltage drop at high current density levels and thermal resistance measurement, provide effective means for the monitoring of controls against such flaws. These tests also provide a means for the elimination of the occasional possible discrepant device.

The modes of failure generally associated with the mechanical flaw category of failure mechanism for an SCR are excessive on-voltage drop, failure to turn on when properly triggered, and open circuit between the anode and cathode terminals. Because these types of failure mechanism are relatively rare, the incidence of these modes of failure is low.

18.7.2 Encapsulation Flaws

Encapsulation flaws are deficiencies in the hermetic seal that will allow undesirable atmospheric impurities to reach the semiconductor element. Foreign atmospheres, such as oxygen and moisture, can react in such a way as to permanently alter the surface characteristics of the silicon metal.

A change in surface conductivity is evidenced by gradual increase of the forward and reverse blocking current characteristics. Because the SCR is a current actuated device, it will lose its capacity to block rated voltage if blocking current degrades beyond some critical point. This type of mechanism may eventually result in catastrophic failure. The rate of degradation is dependent mostly on the size of the leak and the level of stress, particularly temperature, that is applied.

18.7.3 Internal Contaminants

The inclusion of a source of ionizable material inside the sealed package can result in failure mechanisms similar to those resulting from encapsulation flaws if the inclusion is gross. It can also result in apparently similar mechanisms except that the amount of electrical change that occurs is limited.

The mechanism need not be a permanent change in the surface characteristics of the silicon, but can be an electrical change in base width near the silicon surface due to the formation of inversion layers. This condition is often reversible, with recovery accomplished through the removal of electrical bias and the introduction of elevated temperature.

Because the SCR is a bistable, rather than a linear device, concern for this category of failure mechanism arises only if forward blocking current can increase to the point where forward blocking capability is impaired. The probability of occurrence is extremely low except for the possible case of the small junction area, highly sensitive devices. Even here, the mechanism is often negated through negative gate or resistor biasing in the circuit.

18.7.4 Material Electrical Flaws

This category of failure mechanism involves, basically, imperfections in junction formation. Discrepancies of this nature are not generally experienced with SCR's because of their relatively thick base widths and because the blocking junctions are formed by the diffusion process, which allows consistent control of both depth and uniformity of junction.

18.7.5 Metal Diffusion

Of the possible failure mechanisms observed in semiconductors, metal diffusion is the least significant. Though diffusion will occur over a long period of time when two metals are in intimate contact at very high temperatures, the rate at which it progresses is too slow to have tangible effects during the useful life of the device or the system in which it is applied.

18.7.6 Nuclear Radiation

The only true means for determining the actual tolerance of any device to the effects of nuclear radiation is through actual radiation exposure testing of that device. Approximate levels of SCR tolerance, however, have been determined through various tests performed on the General Electric C35 (2N685 series). Critical levels have been shown to be 10^{14} nvt for fast neutron bombardment and $5x10^5$ R/sec for gamma radiation.

Fast neutron bombardment of the silicon results in permanent damage to the crystal lattice, reducing minority carrier lifetime. Significant effects that appear between 10^{13} nvt and 10^{14} nvt are increased gate current to trigger and, to a lesser degree, increased holding current, on voltage, and forward breakdown voltage.

Although gamma radiation may also produce permanent effects on the SCR, it is expected that failure in the typical radiation environment would result first from fast neutron bombardment. Gamma radiation, however, produces high energy electrons by photoelectric and Compton processes which create a leakage current during irradiation. High pulse levels of irradiation can have the transient effect of triggering the SCR on. At 10^6 R/sec, there is a fifty percent chance that the General Electric C35 SCR will be triggered on.

18.8 EFFECTS OF DERATING

From the above, the most probable failure mechanism is degradation of the blocking capability as a result of either encapsulation flaw (or damage) or internal contaminants. The process can be either chemical or electrochemical, and therefore variable in rate according to the degree of temperature and/or electrical stress applied.

If, by derating, the degradation of a "weak" device is retarded such that failure occurs later in time, MTBF is increased and failure rate is lowered. Suppose, for example, that a sample of 778 devices is tested under rated conditions for 1000 hours with one failure observed. The calculated lambda is 0.5 (see Table 18.1), and the MTBF is 200,000 hours. If the failed device would have remained within limits at the 1000 hour point because of lower applied stress, the calculated lambda becomes 0.3 and MTBF is increased to 333,000 hours.

The failure rate improvement factor, also referred to as acceleration or correction factor, is a function of the nature of the particular device type. It is governed by the kinds of failure mechanisms most likely to exist and the degree to which they are sensitive to the different stresses.

In order to develop approximate acceleration curves for General Electric thyristors, it was necessary to analyze the behaviour of a series of devices subjected to a matrix of test conditions including temperature, voltage, current and combinations thereof. The obvious limitations of such testing include:

1. Inability to perform testing on a unit hour basis high enough to give truly significant statistical value to a large number of test conditions.
2. The low incidence of observed failures. Failures must exist under each of the conditions to permit actual failure rate calculations. As a result, analytical failures were created through use of restrictive failure definitions.

Available commercial data on SCR's were used in conjunction with matrix test data developed by General Electric as part of Signal Corps contract DA-36-039-AMC-03619(E) to produce the failure rate improvement curves in Figure 18.4. Because of the data limitations such as described, the acceleration values shown in Figure 18.4 must be considered somewhat less than would be experienced in actual practice. The acceleration factors shown are considered generally applicable to General Electric's thyristor type devices.

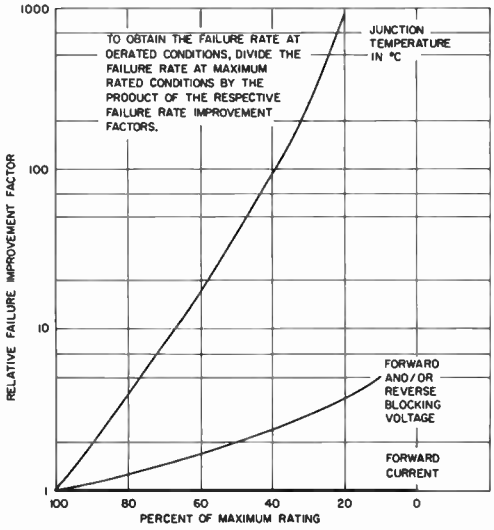


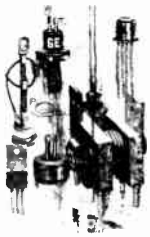
FIGURE 18.4 FAILURE RATE IMPROVEMENT VS. DERATING

From paragraph 18.4, the calculated maximum failure rate of the C35 series was shown to be no greater than 0.46% per 1000 hours. This was reduced to 0.046% by applying a catastrophic definition of failure. Since the testing was performed at rated conditions, a still lower failure rate can be anticipated if the devices are operated at less than rated conditions. From Figure 18.4, improvement factors of two and forty can be used if, in the actual application, the devices are subjected to a maximum of 50% of rated peak voltage and 50% of rated junction temperature on a continuous basis. The maximum failure rate, in this case, is reduced from 0.046% to 0.00058% per 1000 hours, and MTBF is increased from 2,150,000 hours to 1.75×10^8 hours.

The purpose of developing and making available acceleration information is to permit the extrapolation of failure rate predictions, thereby minimizing the cost and opportunity for error inherent in the large scale testing necessary to directly demonstrate the very low failure rates known to be achievable with various semiconductors, including SCR's and other thyristor devices.

Note: Mil-HDBK-217 referenced in this chapter is offered for sale by the Superintendent of Documents, U. S. Government Printing Office, Washington 25, D. C. This publication includes a comprehensive bibliography on the subject of reliability.

19 TEST CIRCUITS FOR THYRISTORS



19.1 INTRODUCTION

The following circuits can be used for a number of purposes; incoming inspection of thyristor components, trouble shooting circuits in which these devices are used, preventive maintenance, comparison of different types and brands of components, and for obtaining a better understanding of thyristor operation. In general the circuits yield test results which can be correlated with max/min values and curves published on a specific device specification sheet.

19.2 INSTRUMENTATION

The current waveform into, and the current and voltage waveforms out of a thyristor circuit may be distorted, due either to the nature of the circuit, e.g., a phase control circuit, or to non-linearities in the semiconductor itself, e.g., its logarithmic forward voltage drop-current relationship. The selection of proper instrumentation for use in thyristor evaluation is therefore of prime importance, if accurate measurement is to be made.

Conventional rectifier diodes and SCR's are rated in terms of *average forward current,* average current being defined as that value of unidirectional current indicated by a DC-reading ammeter placed in series with the diode or SCR. The average value of a waveform should not be confused with its *RMS value,* which is a measure of the heating (I^2R) effect of the waveform in a linear resistance. The ratio of RMS value to average value of any waveform is called its *Form Factor* (F), and F is a function of the ripple content of the wave. For pure (rippleless) DC, $F = 1$, and F increases as the ripple content increases. Thus, the Form Factor of a full wave rectified sine wave is 1.11, but rises to 1.57 for a half wave rectified sine wave.

Triacs, because of their bi-directional nature, are rated in terms of RMS current.

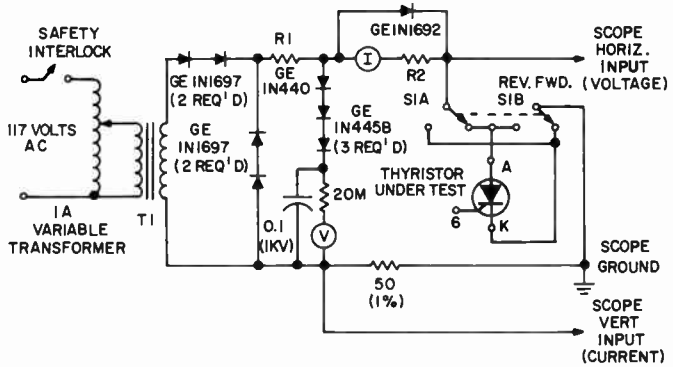
The type of metering used in a particular thyristor circuit will depend on the input voltage to the thyristor. If the input is AC, input voltage should be measured in terms of its RMS value. Note that the commonly available types of "RMS reading" meters (VOM's, most VTVM's) only read RMS correctly when the waveform is a pure undistorted sine wave (rectifier-moving coil instrumets actually *measure* average current, but are *calibrated* to read RMS as long as $F = 1.11$). There are three types of meter that do measure true RMS, independently of waveshape: the iron vane, dynamometer, and thermocouple type instruments. The dynamometer meter is accurate and reasonable in cost, the thermocouple meter is very accurate but delicate, while the iron vane type, although low in cost, has a limited frequency capability. A typical "chopped" sine wave, as produced by SCR phase control, contains a high percentage of harmonics which may be beyond the frequency range

of an iron vane meter: The output "DC" voltage and current of an SCR circuit as well as the current through individual SCR's can be measured with conventional moving-coil instruments. RMS load current must be measured by an RMS ammeter. Ripple voltage is best measured with an oscilloscope, or with an RMS voltmeter in series with a capacitor having low impedance to the ripple compared with the voltmeter. Peak-to-peak voltage is normally read directly from an oscilloscope trace, or with a meter designed to read peak-to-peak values (RCA Senior Voltohmyst WV98C for instance).

19.3 TEST CIRCUITS FOR FORWARD AND REVERSE BLOCKING VOLTAGE AND LEAKAGE CURRENT MEASUREMENTS

19.3.1 Forward and Reverse Blocking Voltage Test for Triacs and All SCR's Above 2 Amperes Rating*

Figure 19.1 illustrates a circuit for testing the forward and reverse blocking characteristics of all G-E low, medium and high current SCR's and triacs, except the very low current types rated at less than 2 amperes. The circuit consists of a variable voltage current-limited power supply that develops a half sine wave of voltage across the thyristor under test to minimize junction heating. Instrumentation consists of suitable meters to indicate blocking voltage and leakage current. An oscilloscope with separate horizontal and vertical amplifiers provides a visual display of the forward and reverse voltage-current characteristics of the test device. Test procedure is as follows:



PEAK BLOCKING VOLTAGE

R1 = 5X MAX. LEAKAGE CURRENT SPEC. OF TEST CELL
R2 = 10 OHMS MINUS RESISTANCE OF METER I
V = 50 μA MOVEMENT CALIBRATED TO 1KV FULL SCALE
I = 50MA FULL SCALE (MEASURES FULL CYCLE AVG.)
T1 = 117/700 VOLT 100 MA TRANSFORMER.

FIGURE 19.1 FORWARD AND REVERSE BLOCKING CHARACTERISTICS TEST SET

*This test set operates at a frequency of 60 Hertz. Stray capacitance charging currents flowing in the equipment are comparable in magnitude to the very low leakage currents of small thyristors. Use the circuit of Figure 19.2 for testing these devices.

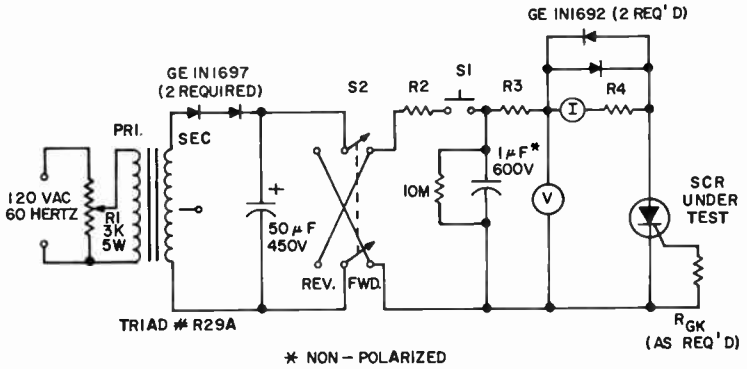


FIGURE 19.2 FORWARD AND REVERSE BLOCKING CHARACTERISTICS TEST SET FOR LOW CURRENT SCR's.

19.3.1.1 $V_{BR(FO)}$, (V_{FOM} for triac), and Forward Leakage Current Measurement

Switch S_1 to "FWD" position. Raise voltage by means of the adjustable transformer T_1 until the meter V reads rated $V_{BR(FO)}$, or V_{FOM}. Read full cycle average leakage current from I, or peak leakage current from the voltage-current trace on the oscilloscope. To measure *actual* forward breakover voltage, increase the applied voltage* by means of T_1 until the scope trace indicates that the test device is breaking over (the current will rise sharply just prior to breakover). Third quadrant blocking voltage measurements on triacs can be made by switching S_1 to "REV" and repeating the test.

*Applied voltage must not exceed peak forward voltage rating (PFV) of a specific device, if the device has a PFV rating—see applicable specification sheet.

19.3.1.2 V_{ROM} (rep) and Reverse Leakage Current Measurement

Switch S_1 to "REV" position. Raise V to the V_{ROM}(rep) rating of the SCR. Read full cycle average reverse leakage current $I_{RO(AV)}$ on I, or peak leakage current on the scope display.

19.3.2 Blocking Voltage and Leakage Current Test for Low Current SCR's (Less Than 2 Amperes Current Rating)

The circuit of Figure 19.2 provides a simple and inexpensive means for checking the instantaneous leakage characteristics and blocking voltage capa-

bilities of low current SCR's. Note that the push button switch S_1 minimizes junction heating and should not be omitted. Tests may be conducted at elevated temperatures by placing the test SCR in an oven. To use, set switch S_1 to "FWD", depress S_1 and turn up the input so that V reads rated blocking voltage. Read off leakage current from I. To measure actual forward breakover voltage, turn up R_1 until I increases sharply and V decreases. Reading of V just prior to this point is the forward breakover voltage of the test device. Reverse blocking voltage and leakage current measurements are made with switch S_2 in the "REV" position.

19.4 GATE TRIGGER VOLTAGE AND CURRENT TESTS

19.4.1 General

These gate tests are used to determine, under stated conditions, the magnitude of the gate trigger voltage and current necessary to switch a thyristor from forward blocking to the on-state. In all circuits, forward voltage is applied to the device under test and the gate voltage is slowly increased in magnitude until the thyristor switches from blocking to the on-state.

19.4.2 Pulse Trigger Test Set for All SCR's and Triacs Above 2 Amperes Rating

The blocking voltage waveform applied to the test thyristor in this circuit (Figure 19.3) consists of a clipped half sine wave of peak magnitude 6 volts or 12 volts, depending on the setting of S_1. The correct setting of S_1 is determined from the specification sheet of the thyristor under test, as is the value of the anode load resistor R_S. Gate source voltage consists of a square wave pulse, whose magnitude can be varied from zero to 6 volts, and whose pulse width is adjustable from about 5 μseconds to greater than 100 μseconds. Gate voltage can be switched either positive or negative for testing triacs. Instrumentation consists of a gate current "looking" resistor R_4, an oscilloscope with separate vertical and horizontal amplifiers, and a DC voltmeter V_1 to monitor when the test device triggers.

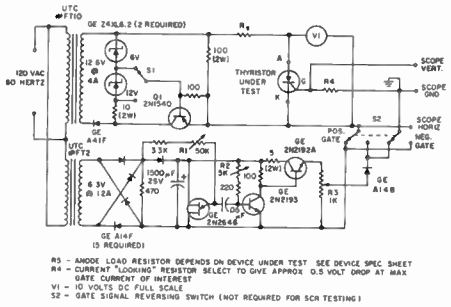
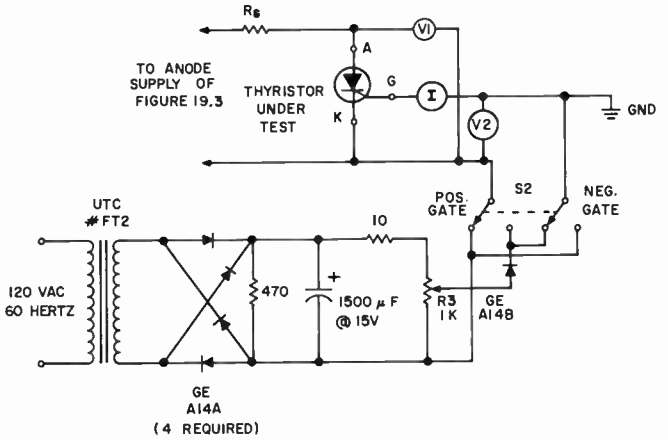


FIGURE 19.3 PULSE TRIGGER TEST (SCR's AND TRIACS)

Test procedure is as follows: R_1 is adjusted so that a gate pulse occurs only *once* during each half cycle of applied anode blocking voltage and the pulse should be timed (by R_1) to occur approximately 4 milliseconds after the start of the half cycle. R_2 is then adjusted to give the desired width of pulse. Note that gate pulse widths in excess of 100 μseconds result in measured values of trigger voltage and current that are equivalent to continuous DC measurements. With R_3 set initially for zero volts output, the applied gate voltage is gradually increased (via R_3) until the test thyristor triggers. Because the gate impedance may change when triggering occurs, the readings of gate voltage and current must be made just prior to triggering. Triggering is indicated by a sudden drop in the reading of V_1, or by a sudden step in the gate E-I trace observed on the oscilloscope.

19.4.3 DC Gate Test for All SCR's and Triacs Above 2 Amperes Rating

The test circuit of Figure 19.4 is essentially a DC version of the pulse test described in 19.4.2. Anode supply circuitry is identical, while the pulse generator is replaced with a simple adjustable DC power source. Instead of monitoring trigger voltage and current with an oscilloscope, DC meters are used. As before, R_3 is turned up until the test thyristor triggers. I and V_2 are read off just prior to the trigger point.



S2 – GATE SIGNAL REVERSING SWITCH (NOT REQUIRED FOR SCR TESTING)
VI – 10 VOLTS D.C. FULL SCALE
V2– 12 VOLTS D.C. FULL SCALE
I – SELECT FULL SCALE TO SUIT GATE CURRENT RANGE OF INTEREST

FIGURE 19.4 DC GATE TRIGGER TEST (SCR's AND TRIACS)

19.4.4 Gate Trigger Test Set for Low Current SCR's (Less Than 2 Amperes Current Rating)

The measurement of low current SCR triggering voltage and current is complicated by the fact that the gate impedance changes *drastically* when

the test device switches on. In addition, the gate trigger voltage and current values are dependent on the source impedance of the test set, and the source impedance must therefore be specified when making tests. The circuit of Figure 19.5A is designed specifically for testing all present G-E low current SCR's. In this circuit a variable half sine wave of voltage is applied to the gate (from a controlled impedance source) and the gate E-I characteristic is monitored with an oscilloscope. The triggering point is detected by the sudden change in gate impedance that occurs when the device switches on.

Figure 19.5B shows a typical scope presentation of a gate E-I characteristic during the gate trigger current and trigger voltage test. The trace is shown dotted beyond the triggering point. In the actual case, the trace suddenly jumps at the triggering point due to the change in gate impedance. The portion of the trace beyond the triggering point becomes somewhat reduced in intensity.

The gate trigger voltage is that value of voltage which will just cause the device to switch to the on-state. As shown in Figure 19.5B it is read just prior to the switching point. Unlike trigger voltage, the gate trigger current value must be read at the point where it is a maximum, although this is not necessarily the actual triggering point. It must be kept in mind that in order to reach the actual triggering point, the trace must first pass through this maximum, and the firing circuit design must take this into account.

Many low current SCR's exhibit triggering with a negative value of gate current. Figure 19.5C shows a typical gate E-I trace for this type of device. Note that the gate trigger voltage is always positive. On this type of unit only the gate trigger voltage is of interest. A negative gate trigger current is meaningless to the circuit designer, and it is not necessary to measure it.

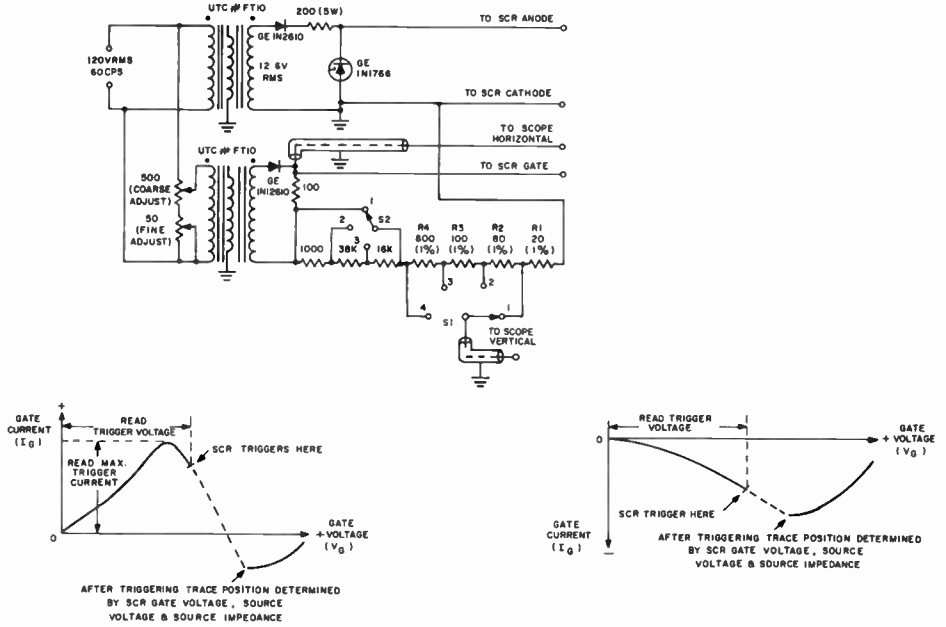
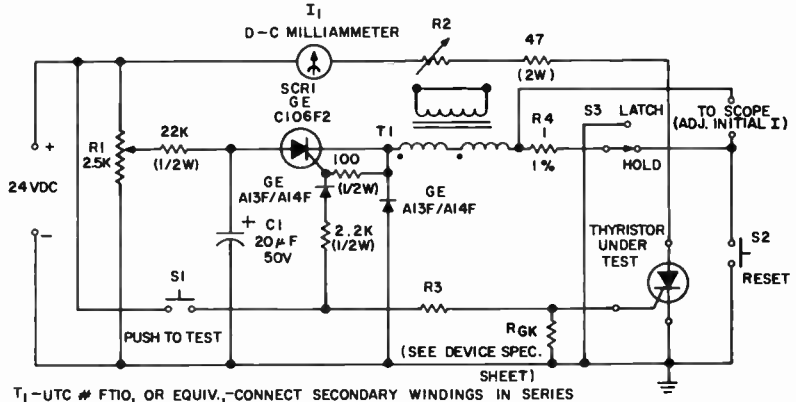


FIGURE 19.5 GATE TRIGGER TEST SET FOR LOW CURRENT SCR's.

19.5 LATCHING AND HOLDING CURRENT TESTS

19.5.1 General

By definition, latching current is the minimum current that must flow through the anode terminal of a thyristor for the device to switch to the "on" state, and *remain in the on state* after removal of the gate trigger pulse. Holding current is defined as the minimum current that can flow through the anode terminal of a conducting thyristor *without the device reverting to the off state.* Because latching and holding current values are dependent on gate conditions and anode supply voltage, these parameters must be specified as test conditions. A thyristor may also exhibit more than one value of on-voltage at a given forward current level, especially if the maximum value of anode current never rises much above holding level. This latter phenomenon can lead to several values of holding current for the same device. To properly perform a holding current test it is therefore necessary to turn the device on initially into a fairly high current pulse, and subsequently reduce the current down to holding level. The test circuit of Figure 19.6 fulfills this requirement; it may also be used for performing latching current tests.



T1 – UTC # FT10, OR EQUIV., – CONNECT SECONDARY WINDINGS IN SERIES & SHORT PRIMARY WINDING.
I1 – 500ma DC MOVEMENT
R2 – 10K POTENTIOMETER (OR 50K FOR TESTING LOW CURRENT SCR'S).
R3 – TO SUIT THYRISTOR UNDER TEST
R_{GK} – AS REQUIRED, e.g. 1K FOR GE LOW CURRENT SCR'S.

FIGURE 19.6 HOLDING AND LATCHING CURRENT TEST SET

19.5.2 Latching Current Measurement

For latching current measurements (S_3 in the LATCH position), the circuit consists essentially of the test thyristor in series with a current adjusting resistor R_2, milliameter I_1, and the 24 VDC power supply. S_1 and R_3 provide trigger signals for the test SCR. R_3 is selected to provide specified trigger current for the thyristor under test. Operating procedure is as follows: R_2 is set initially at its maximum resistance value and is then gradually reduced while switch S_1 is periodically depressed and released. Each time S_1 is depressed I_1 will deflect and then drop back to zero when S_1 is released as long as the anode current flowing through the test thyristor is less than its latching current. When latching finally occurs I_1 will deflect and remain deflected as S_1 is released. The value of current indicated by I_1 at the transition point is the latching current of the test thyristor.

19.5.3 Holding Current Measurement

For holding current measurements, S_3 is moved to the HOLD position and R_2 initially is left at the setting determined during the latching current test. Now each time S_1 is depressed to trigger the test thyristor, SCR_1 also is triggered and SCR_1 sums an additional pulse of current through the test thyristor as it turns on. The magnitude of this initial current pulse is determined by the setting of R_1 and is specified for each thyristor type. Its value is monitored by the 1 ohm "looking" resistor R_4. Pulse width is fixed by C_1 and T_1 and is satisfactory for presently available G-E devices. To measure the holding current of a particular thyristor, S_1 is depressed to trigger the test device and then released. R_2 is then increased in value until I_1 drops suddenly to zero. The reading on I_1 just prior to this point is the holding current of the test thyristor.

19.6 AVERAGE FORWARD VOLTAGE ($V_{F\ AVG}$) TEST SET

The circuit of Figure 19.7 can be used to test the forward voltage drop of a thyristor in the conducting state. In this test, the thyristor is subjected to a DC current as read by meter M_1 and the voltage drop is measured by meter M_2. To make the measurement, close S_1 with T_1 in a position approximately midway between the end positions. Adjust T_1 to the level of current desired on M_1. Read M_2 by depressing S_2. These readings should be less than the maximum values specified on the forward characteristic curves in the specification bulletin for the particular device. A current level somewhere near the continuous duty current rating of the thyristor is recommended. If the thyristor is not attached to a heatsink for this measurement, the readings should be completed within two or three seconds to prevent overheating of the cell. The foregoing tests can be conducted at any ambient temperature within the operating range provided that the ratings at the stud temperature are not exceeded.

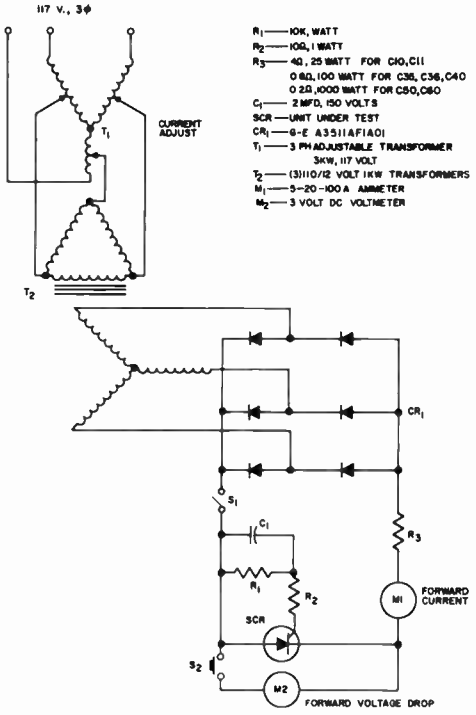


FIGURE 19.7 FORWARD VOLTAGE DROP TEST SET

19.7 TURN-OFF TIME TEST CIRCUIT

As discussed in Chapter V, the turn-off time depends on a number of circuit parameters. Thus, a turn-off time specification inherently must include the precise value of these circuit parameters to be meaningful. Accordingly, specifications for General Electric SCR's with guaranteed turn-off limits list the applicable circuit parameters and show the test circuit which will apply these parameters to the SCR. For this information, the reader is referred to the specification bulletin for the SCR under consideration (e.g., GE C9, C12, C40, C55, C140, etc.).

For general turn-off time test work, the type of circuit shown in Figure 19.8 can be used for low, medium, and high current SCR's by proper manipulation of the circuit constants. Forward load current is adjustable by R_5 from approximately ½ ampere to 70 amperes and the length of time SCR_1 is reverse biased during the turn-off cycle can be adjusted by manipulating R_5 and C_1. The peak reverse current during the recovery period can be adjusted by R_7 and this current can be viewed on a scope by monitoring the voltage across a non-inductive shunt R_8. If one is interested in only one particular load current range, there is of course no necessity in providing the complete range of resistors and capacitors specified in Figure 19.8.

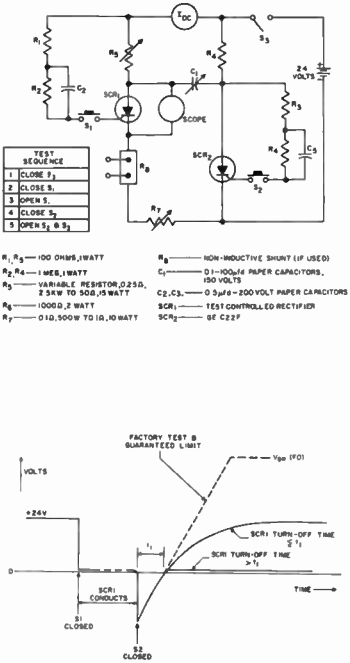


FIGURE 19.8 TURN-OFF TIME TEST

This test circuit subjects the SCR to current and voltage waveforms similar to those found in a parallel inverter circuit. Closing S_1 and S_3 fires SCR_1, the unit under test, so that load current flows through R_5 and the ammeter. In less than a second C_1 charges through R_6 to the voltage being developed across R_5 by load current flow. If S_2 is now closed, SCR_2 turns on. This applies C_1 across SCR_1 so that the current through SCR_1 is reversed. C_1 furnishes a short pulse of reverse recovery current through SCR_1 until this SCR recovers its reverse blocking ability. After this initial pulse of current, C_1 continues its discharge through SCR_2, the battery, and R_5 at the rate dependent on the time constant of R_5C_1. After a time interval, t_1, in Figure 18.7, somewhat less than the R_5C_1 time constant, the anode to cathode voltage of SCR_1 passes through zero and starts building up in the forward direction. If the turn-off time, t_{off}, of the SCR is less than t_1, it will remain turned off and the ammeter reading will return to zero. If not, the SCR will turn back on and current will continue to flow until S_3 is opened.

The turn-off interval t_1 can be measured by observing the anode to cathode voltage across SCR_1 on a high speed oscilloscope such as the Tektronix 545A or equivalent. A waveshape similar to that shown in the figure will be observed.

Satisfactory operation of this circuit requires careful attention to detail. The DC source must have good regulation if C_1 is to develop ample commutation voltage for turning off SCR_1. In order to minimize circuit inductance, power leads should be heavy copper-braid when testing medium and high current SCR's and lead lengths should be held to an absolute minimum.

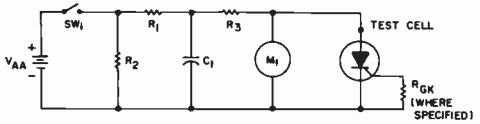
Turn-off time testing in the General Electric factory is performed with a fixed rate of rise of reapplied forward voltage as indicated by the dashed line in Figure 19.8. This is a more severe test on the SCR than the exponential curve and it requires considerably more elaborate test equipment than in Figure 19.8. For those who wish to test under these conditions, information on the factory test circuit will be provided upon request. (Ref. 1)

19.8 DV/DT TEST

The forward blocking capability of a thyristor is sensitive to the rate at which the forward blocking voltage is applied. If the rate of rise exceeds a critical value, switch-on will occur, even though the applied voltage is less than the *static* breakover voltage of the device. For energization of a device from rest with an exponentially rising voltage waveform, the numerical value of dv/dt is computed as follows:

$$dv/dt = \frac{\text{Applied Forward Voltage}}{\text{Exponential Time Constant}} \times .63$$

Where this parameter appears on the device specification sheet, it enables the circuit designer to design filters to prevent false triggering. Figure 19.9 illustrates a simple circuit to check the dv/dt capabilities of p-n-p-n devices.



V_{AA} = ANODE VOLTAGE SUPPLY, VARIABLE
SW_1 = MERCURY WETTED RELAY
R_1 = NON-INDUCTIVE RESISTOR
R_2 = DISCHARGE RESISTOR
R_3 = CURRENT LIMITING RESISTOR
R_{GK} = GATE TO CATHODE RESISTOR (WHERE SPECIFIED e.g. GE C5, C7, L8, L9, C106 E
C_1 = CAPACITOR
M_1 = DC VOLTMETER OR OSCILLOSCOPE

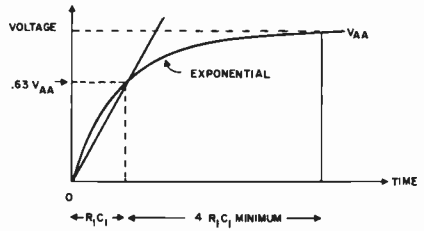


FIGURE 19.9 DV/DT TEST

The switch SW_1, if it is not of the mercury wetted type, must have a closure time (including bounce) of not more than .1 R_1 C_1. R_3 is a current limiting resistor to prevent damage to the device under test in the event of dv/dt triggering.

With the gate open-circuited, or with the specified bias conditions operable, an exponential voltage waveform is applied across the test cell each time SW_1 closes. The test is a GO-NO GO test performed by increasing the supply voltage until the device under test switches on, or until the specified voltage limit value is reached without switching. The exponential waveform may be observed by connecting an oscilloscope directly across the test cell.

19.9 TURN ON VOLTAGE TEST

The circuit of Figure 19.10 may be used to gauge the ability of an SCR to *switch* high current loads satisfactorily. When an SCR is gate triggered, it turns on initially only in the region nearest the gate contact, and the turned-on portion then spreads laterally to encompass the entire pellet area. Until the whole pellet is in conduction, any load current through the SCR concentrates in the turned-on portion, effectively limiting the maximum current-carrying ability of the SCR for the first microsecond or so after triggering. Since the forward voltage drop of an SCR is proportional to current density, it is possible to compare the switching characteristics of a batch of devices by measuring their individual forward voltage drops at a standard current level and time interval subsequent to triggering. In the circuit as shown, the UJT (Q_1) oscillator frequency is set by means of R_1 so that the test SCR triggers sometime after the peak of the 60 Hertz input sine wave. Transformer T_1 is then adjusted until the peak magnitude of the 10 microsecond

wide half sine wave resonant discharge current pulse that ensues is 150 amperes, as measured by the current probe and oscilloscope. By taking measurements at the peak of the current pulse, voltage errors due to stray inductance in the circuit are eliminated. The SCR forward voltage drop at the 150 ampere standard current is a measure of its di/dt capability. Care is needed in the connections of the voltage and current probes to avoid errors due to stray pickup from ground loops.

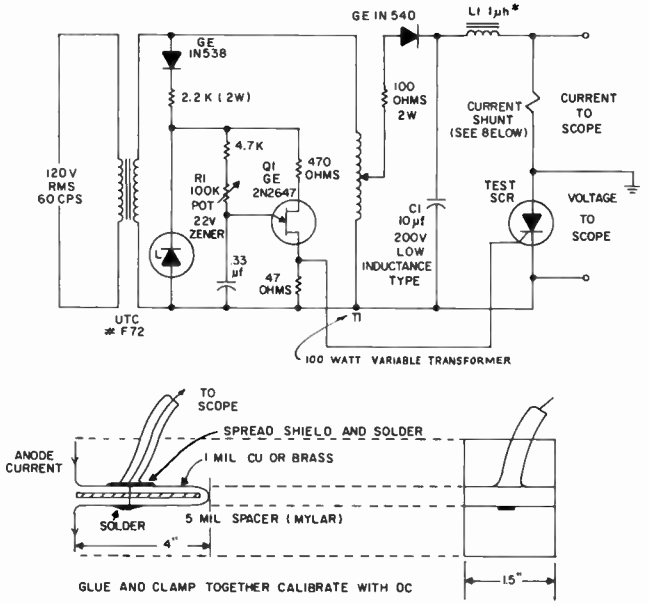


FIGURE 19.10 TURN ON VOLTAGE TEST

19.10 COMMUTATION DV/DT TEST FOR THE TRIAC

19.10.1 General

Operation of the triac into an inductive load may create problems that must be allowed for during circuit design. The most serious of these problems is commutation dv/dt. Commutation dv/dt is that rate of rise of voltage impressed across the triac by a circuit at the cessation of current flow. In an inductive AC circuit (Figure 19.11) current lags voltage by a phase angle ϕ and as a result current goes through zero sometime after the supply voltage has reached a finite value in the opposite direction. Since the triac tries to turn off at zero current, the instantaneous line voltage at that point appears suddenly across the device at a rate limited only by circuit stray capacitance and the capacitance of the triac itself (C_T). For the triac to turn off reliably in an inductive circuit, the rate of voltage rise across the device must be kept within specified limits, and the test circuit of Figure 19.11 is intended to

*L_1 includes stray inductance of main discharge loop (C_1, L_1 and test SCR). The discharge loop leads should be as short and heavy as possible to minimize losses.

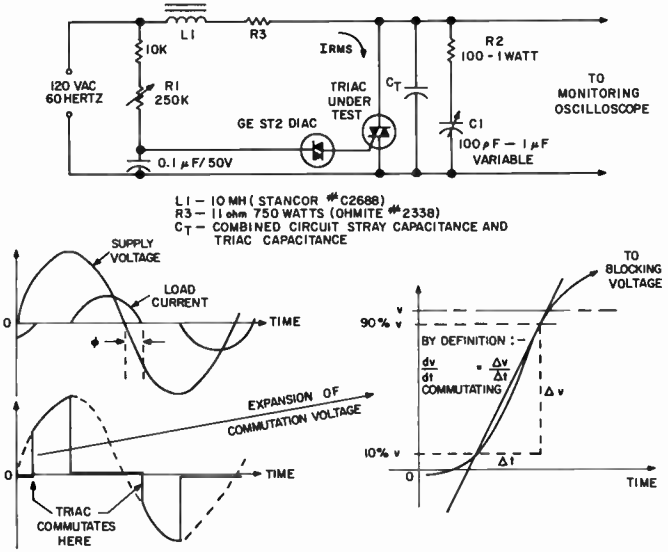


FIGURE 19.11 COMMUTATION DV/DT TEST

check this dv/dt withstand ability. In this circuit, the rate of rise of voltage across the triac is made adjustable (from 10 volts per microsecond down to less than 0.3 volts per μsecond) by deliberately adding capacitance C_1 in shunt with the test device. Resistor R_2 prevents high peak current from flowing through the triac when it turns on and discharges C_1.

19.10.2 Test Procedure

Testing procedure is as follows. Set C_1 initially to 1 μf and R_1 to maximum resistance. With power applied adjust R_1 so that $I_{RMS} = 5$ amps RMS. The easiest way to set $I_{RMS} = 5$ amps is to monitor the voltage across R_3 with a true RMS voltmeter ($V_{R3} = 55$ volts RMS). If testing is to be done at maximum junction temperature, additional heating must be supplied the triac. One method is to screw the triac stud into a 4" x 4" x ½" aluminum block and heat the block with a commercial hot plate or skillet.*
Press-fit type triacs can be laid on the hot plate directly. Case temperature as monitored with a thermocouple placed on the side of the triac (see Chapter 17) is set to 80°C for the SC40 and SC41, or 88°C for the SC45 and SC46. Junction temperature will then be rated 100°C. C_1 is then progressively reduced until the desired rate of voltage rise across the triac is reached, or failure to commutate results as monitored by the test oscilloscope. Numerical rate of voltage rise is defined by the waveforms of Figure 19.11. Note that for triac types SC40, 41, 45, 46 the rate of voltage rise during the first *20 volts only* of reapplied voltage (v = 20 volts) defines the device dv/dt capability.

*It is recommended that the bimetallic temperature controller supplied with the hot plate or skillet be discarded in favor of a more precise electronic control like the circuit of Figure 12.15

19.11 COMMERCIAL SCR TEST EQUIPMENT

There are several manufacturers who offer ready-made SCR test gear for use by OEM's and others. These manufacturers should be contacted directly for details of other respective equipments. A partial listing of such manufacturers follow.

Baird-Atomic Inc.
33 University Road
Cambridge 38, Mass.

Geauga Electronics Co.
7336 Samuel Lord Drive
Chagrin Falls, Ohio

International Electronics Technology
Winthrop, Massachusetts

Modern Design Electronics
Vestal Parkway,
Vestal, New York

Owen Laboratories Inc.
55 Beacon Place
Pasadena, Calif.

Power-Radiation Inc.
Box 616
Suffern, N. Y.

Seco Electronics Inc.
1201 S. Clover Dr.
Minneapolis 20, Minn.

Sensory Systems
P. O. Box 2071
Costa Mesa, California

Solitron Devices, Inc.
Norwood, N. J.

Teltronics Inc.
23 Main Street
Nashua, New Hampshire

Special oscilloscopes, such as the Tektronix 575A Transistor Curve Tracer (Tektronix Inc., Beaverton, Oregon) may also be used for checking SCR characteristics such as forward and reverse blocking voltage, leakage current, gate trigger parameters, holding current, etc.

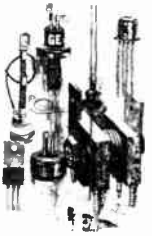
19.12 IEEE TEST STANDARDS

The Semiconductor Components Committee of the IEEE is presently preparing a Standard for Semiconductor Controlled Rectifiers. At this writing no Standard has been issued.

REFERENCE

1. "Turn-Off Time Characterization and Measurement of Silicon Controlled Rectifiers," R. F. Dyer and G. K. Houghton, AIEE CP 61–301.
2. "Portable SCR and Silicon Rectifier Tester," Application Note 201.3, available from General Electric Co.

20 SELECTING THE PROPER THYRISTOR AND CHECKING THE COMPLETED CIRCUIT DESIGN



20.1 SELECTING THE PROPER THYRISTOR

A glance at the device specification section in Chapter 21 shows that the equipment designer has available to him a wide range of thyristor components from which to choose. Basic SCR types are offered with current ratings extending from ½ amp to 850 amps RMS, and with voltage ratings spanning the range 25 volts through 1800 volts peak. Within this range in many instances economy/light industrial SCR's exist side by side with similarly rated industrial/military types. Many *specialized* SCR types also are listed, including high speed inverter SCR's with guaranteed dynamic characteristics, SCR's for use over very wide temperature ranges, SCS's, light-activated SCR's, very high voltage SCR's, and SCR's tested to very rigid quality levels for high reliability applications. Bidirectional thyristors (triacs), intended primarily for use on 120 volt and 240 volt AC power lines, are presently available in 6, 10, and 15 amp sizes. Diacs and UJT's, while not strictly speaking thyristors, are included because of their wide usage as thyristor trigger components. Packaged assemblies ("stacks") of individual thyristors and/or rectifier diodes—both with and without suitable control circuitry—complete the range. For the equipment designer understandably confused by this profusion of types, the following selection criteria are offered.

20.1.1 Semiconductor Design Trade-Offs

Within the present state of the power semiconductor art it is true to say that there is no such thing as a "universal thyristor." An SCR optimized for use in a high speed inverter or chopper circuit for instance may be a bad choice for use in a 60 Hz phase control application. By the same token, a thyristor designed for use in very high voltage applications is by nature unsuited for use in high frequency circuits. These various incompatibilities stem from the fact that most device design approaches leading to good high power handling capabilities (voltage or current) are diametrically opposite to those leading to good high frequency performance. As a result *state of the art* high frequency devices tend to have limited power handling capabilities, while the highest power devices are relatively slow. Between these two extremes there are naturally many general-purpose devices that combine medium speed performance with medium power handling capabilities. Figure 20.1 summarizes some of the design factors that affect practical thyristor electrical performance at this writing.

Design Variable (increase)	EFFECT ON				
	Current Rating	Voltage Rating	Turn Off Time	dv/dt Withstand Ability	Ability to Switch High Currents Rapidly (di/dt)
Pellet Area (emitter)	↑				↓
Base Width	↓	↑	↑	↑	↓
Resistivity	↓	↑			↓
Lifetime	↑	↑	↑	↓	↑
Thermal Resistance	↓	↓	↑	↓	↓
Surface Contouring	↓	↑			
Emitter Shorts		↑		↑	
Optimized Gate Structure (field injection)	↓				↑

Key: Beneficial Effects— Increase ↑ Decrease ↓ Undesirable Effects— Increase ↑ Decrease ↓

FIGURE 20.1 THYRISTOR DESIGN TRADE-OFFS

As discussed in Chapter I, there are also several design compromises that can be made in the *mechanical construction* of a thyristor. For example, when a thyristor is designed specifically for use in the light industrial and consumer markets—environments characterized by limited temperature excursions and absence of wide range cyclical loading—simple low cost fabrication techniques are usually employed in its construction. Such techniques, while completely adequate for their intended purpose, would be completely unacceptable if applied to the design of a 500 amp SCR destined for use in a steel mill drive. Here, a premium thermal-fatigue resistant and high voltage structure would be a "must."

20.1.2 Selection Check List

To select and apply *any* thyristor successfully, none of its published ratings should be exceeded. Equally evident, it would be uneconomical to apply the device too conservatively. To make a proper device selection then, the equipment designer should first of all prepare a check-list outlining all the limiting conditions of his particular application. Since thyristor ratings are usually specified as maximum or minimum values (worst case), the designer subsequently can determine which device best fits the needs of the application. The following is a check list of the steps that should be taken, or considered, in selecting the proper thyristor for a given application.

1. Determine Circuit Requirements on Thyristor

Voltage across and current through the thyristor must be determined in terms of circuit input voltage and output power requirements. Figure 9.4 shows these relationships for some common SCR circuits.

Note. Check voltage transients (Chapter 15).

Check current carrying capability required of the thyristor if the *current waveform* is irregular (Chapter 3).

Determine temperature range over which the circuit must operate. Is a high-reliability or "MIL-Spec" device desirable or mandatory?

2. Select Proper Thyristor

Refer to Section 21.1 and then to the more detailed specifications in Chapter 21. For final check, consider individual device specification sheets with more detailed information.

3. Determine Proper Heatsink

(a) Check maximum allowable ambient temperature if a lead mounted device was selected.

(b) Select proper size heat sink from fin curves given on specification sheet for stud mounted thyristors, OR determine proper size heatsink from Chapter 17 if fin curves are not available for the particular thyristor selected, OR select suitable pre-assembled thyristor stack assembly from the many types available as indicated in Chapter 21.

4. Design Triggering Circuit

See Chapter 4 for thyristor triggering requirements and design criteria. Also, there are commercially available packaged triggering circuits using magnetic and semiconductor components.

5. Design Suitable Overload Protection, if Required

Protect the thyristors and associated semiconductors against short circuit, and other fault conditions. In some applications economic factors and industry practice may preclude or not require protective circuitry coordination. *Do not overlook "normal overloads"* such as cold inrush to incandescent light bulbs, or starting current of induction motors, etc.

Beyond these elementary steps there are often other considerations meriting special attention:

1. Series or parallel operation of individual thyristors—Chapter 6.
2. Radio interference suppression—Chapter 16.
3. Frequency response—Chapter 3 and Chapter 5.

20.2 Checking Circuit Design

The purpose of this section is to aid the designer in diagnosing and curing poor performance in his completed circuit. It also provides a step-by-step procedure for checking the design to ensure long life and reliable operation of the thyristors.

20.2.1 Thyristor Ratings and Characteristics

Thyristors must be operated within their ratings as given in the specification sheet. Do not design around samples; the sample may well be much better than the type number would indicate. If production quantities are later involved, some thyristors may be received which are, for example, of lower voltage capability than the sample. *Use specification sheet values, not sample data.*

Voltage and current measurements must be made on all the thyristors in the prototype. For this purpose an oscilloscope is essential. It should have a rise time of less than 100 nanoseconds in order that the waveforms may be reliably scanned for steep wave fronts.

Measurements should be made under extreme as well as normal load conditions. Include open-circuit operation, momentary overloads, and the first starting cycle.

20.2.2 Voltage Measurement (See also Section 19.2)

Make sure that the probe is adjusted to give a flat response. Make sure too that no ground-current loops are present; the rule is that only one ground lead should run from the circuit to the oscilloscope.

20.2.3 Current Measurement (See also Section 19.2)

Current measurements are more difficult to make accurately than voltage measurements. No universal instrument is available but satisfactory results are obtained using a combination of the following types.

Current Probe. This is a clamp-on type of current transformer with the secondary connected to an oscilloscope. An example is the Tektronix Type P6016 current probe, Figure 20.2. When used with an amplifier this probe can handle 15 amperes peak to peak and has a frequency response extending from 50 Hz to 20 mHz. It is especially useful for measuring gate-current pulses because the readings are free from external pick up.

FIGURE 20.2 CURRENT PROBE AND AMPLIFIER

This type of instrument cannot measure DC and is liable to saturate if the DC component exceeds 0.5 ampere. The current range of the current probe of Figure 20.2 may be extended by winding a current transformer as shown in Figure 20.3.

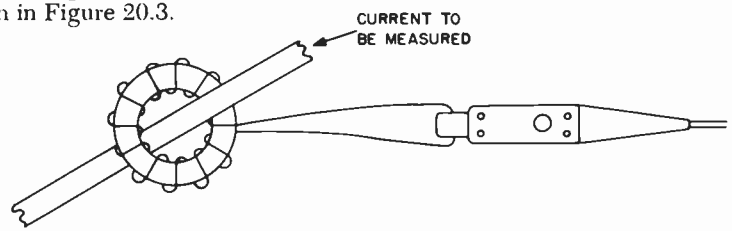


FIGURE 20.3 METHOD FOR EXTENDING CURRENT RANGE OF OSCILLOSCOPE CURRENT PROBE

The core may be of ferrite, powdered iron or powdered molybdenum (typically Arnold Mfg. Co. Cat. #106073-2). The number of turns = current ratio, thus Figure 20.3 shows a 10:1 arrangement.

Current Shunt. The current shunt is a non-inductive resistor which is inserted in the circuit. The voltage across this resistor is then observed on an oscilloscope. An inexpensive form of a current shunt is described in Chapter 19 and construction details are given in Figure 19.10. This shunt can handle about 20 amperes rms and has a usable frequency response from DC to about 1 mHz.

A much more elegant design is shown in Figure 20.4. This shunt, made by T & M Research Products, 1312 Espanola Avenue, N.E., Albuquerque, New Mexico, has a frequency response from DC to 150 mHz and can carry 60 amperes rms continuously. The only limitations of this form of current measurement lie in the practical difficulty of inserting the shunt in the circuit and in avoiding false readings due to stray pick up from ground loops.

FIGURE 20.4 A COMMERCIAL NON-INDUCTIVE CURRENT SHUNT

20.2.4 The Power Circuit

The following anode voltage and current relations should be measured on all thyristors in the circuit:

Peak forward blocking voltage
Peak reverse voltage
dv/dt
Turn-off time (t_q) (if required, as in an inverter or chopper)
Rate of change of turn-on current (initial di/dt)
Forward current before turn-off (if required)
Peak reverse current (if required)

These items are generally specified in the specification sheet. If the thyristor is running outside of specifications, either choose another rating or modify the circuit so as to run the device within ratings.

20.2.5 Modifications to Soften dv/dt

Add a series RC network across the thyristor. Note that this may, with low values of R, increase the di/dt. The effectiveness of the network may be increased by shunting a fast recovery diode across the resistor. This increases softening of the dv/dt without worsening the initial di/dt (see Chapter 6).

20.2.6 Modification to Soften Initial di/dt

The initial di/dt may be limited by means of a reactor or saturating reactor connected in series with the thyristor. The design of the saturating reactor is discussed in Section 3.9.

20.2.7 Gate Circuit

The following gate voltage and current relations should be measured in the prototype:

Gate voltage before triggering
Peak gate triggering voltage
Pulse width of triggering gate voltage
Gate triggering current
Gate current rise time

From the above data check that the following are within the specified limits:

Peak and average gate power
Peak reverse voltage on gate
Peak gate triggering voltage

Note that for short trigger pulses the peak gate voltage that will trigger all thyristors has to be increased as the pulse width decreases (Chapter 4).

Remember that a slowly rising gate pulse that will only just trigger a thyristor is liable to increase local junction heating if fast rising anode currents exist. Always trigger an SCR used in inverters with as steep a rise time as possible (preferably shorter than 500 ns) and with as high an amplitude as is permitted.

Negative gate bias voltage may be applied to an SCR while blocking to improve dv/dt and turn-off time. This also negates random triggering.

Where the anode current of an SCR is liable to oscillate due to resonance in the load, it will be necessary to trigger the SCR with a broad pulse. A gate pulse which did not extend to time t_2 in Figure 20.5 would result in only the shaded part of the anode current flowing. By continuing the gate pulse to time t_2, the SCR will be retriggered when the circuit again causes anode current to flow. Extended gate pulse duration is also necessary when triggering is initiated before current zero in phase control applications with lagging power factor load as discussed in Section 9.6.

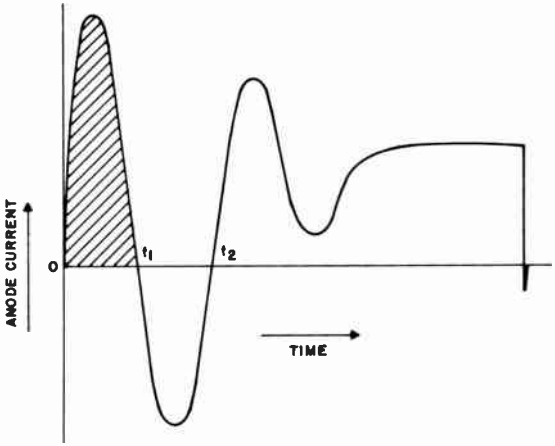


FIGURE 20.5 TYPICAL OSCILLATORY ANODE CURRENT WAVEFORM

Alternatively, the gate may be triggered by a train of pulses such as shown in Figure 20.6.

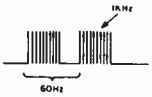


FIGURE 20.6 PULSE TRAIN FOR GATE TRIGGERING

Check the gate current for spurious signals. The clamp-on current probe is ideal for this purpose.

20.2.8 Temperature Measurement

The case and junction temperatures of a thyristor have a strong influence on its characteristics. It is therefore necessary in checking thyristors in a circuit to measure the case temperature of each and, if the specification sheets do not supply adequate data, to estimate the junction temperature. The estimated junction temperature should then be used in prescribing the required thyristor characteristics. Methods of calculating the junction temperature are discussed in Chapter 3.

20.2.9 Magnetic Saturation

Iron core inductors and transformers can saturate and mar the performance of some thyristor circuits. There are two cases where unexpected saturation can commonly be encountered.

1. In phase control circuits with a transformer load. Asymetrical triggering, whether gate or anode type triggering, will cause a DC component of current to flow through the transformer, thus tending to saturate it.

2. When an inverter is initially triggered, the voltage applied to the iron core transformer may be in the same polarity as the half cycle before it was previously turned off. The additional magnetomotive force may cause saturation of the core.

Corrective methods include:

(a) Designing the core for operation at reduced flux density.
(b) Controlling the trigger pulses so that the magnetization polarity is symmetrical and is always automatically reversed.
(c) Starting at a frequency which is momentarily higher than normal.
(d) Introduction of current limiting impedance.

20.2.10 Supply Impedance

Check the power supply impedance. Remember that in an inverter the supply has to carry output-frequency current. Electrolytic capacitors are not always suitable for carrying AC superimposed on DC owing to their relatively high loss factor. Oil impregnated paper capacitors are much better.

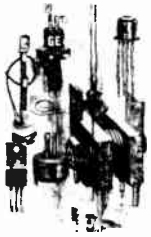
Avoid having mechanical switches in the line from the supply to the thyristor whenever possible. Contact bounce is a common cause of transients and high values of dv/dt.

20.2.11

Measure and check the following against the component specifications.

Max. Load	Min. Load	Starting Load	
☐	☐	☐	Peak forward blocking voltage
☐	☐	☐	Peak reverse voltage
☐	☐	☐	Rate of change of turn-on current at operating frequency
☐	☐	☐	Forward current before turn-off
☐	☐	☐	Average forward current
☐	☐	☐	RMS forward current
☐	☐	☐	Peak reverse current
☐	☐	☐	Maximum gate voltage before triggering
☐	☐	☐	Maximum gate reverse voltage before triggering
☐	☐	☐	Peak gate triggering voltage
☐	☐	☐	Peak gate triggering current
☐	☐	☐	Peak gate power
☐	☐	☐	Average gate power
☐	☐	☐	Gate voltage rise time
☐	☐	☐	No spurious signals on gates
☐	☐	☐	Gate pulse width suitable for the circuit
☐	☐	☐	No undesired saturation in magnetic core reactors
☐	☐	☐	No undesired saturation in magnetic core transformers
☐	☐	☐	Power supply impedance
☐	☐	☐	No contact bounce effects from mechanical switches
☐	☐	☐	Electrolytic capacitors checked for high AC current
☐	☐	☐	Case temperature
☐	☐	☐	Operation satisfactory at maximum ambient temperature
☐	☐	☐	Operation satisfactory at minimum ambient temperature

21 GENERAL ELECTRIC THYRISTOR AND DIODE CONDENSED SPECIFICATIONS



This chapter is primarily devoted to condensed specifications of General Electric's thyristors, thyristor assemblies, trigger devices, and diodes. These specifications are intended for reference only. For full information the designer should rely on the complete specifications indicated for each type.

The selection chart on the following page is included to give the designer an overall look at General Electric's thyristors in addition to serving as a preliminary guide to selecting a device. It should be noted on the chart that the SCR's are classified into ten groups based on their salient features and potential applications. It should also be noted that each SCR family appears once on the chart even though it is applicable to more than one of the eight classifications. Multiple classification was ignored to avoid confusion.

This chapter also includes a handy alpha-numeric index and a list of General Electric's military approved thyristors and diodes.

21.1 THYRISTOR SELECTION CHART

1. LOW CURRENT (UP TO 10A) GENERAL PURPOSE INDUSTRIAL AND MILITARY SCR'S

GE Type	JEDEC No.	Forward Current I_T (RMS) Amp	Peak Voltage Range	Condensed Spec on Page	Complete Spec No	Comments
	2N877-81 2N885-89	.5	30 thru 200	411 412	150.5	I_{GT} = 200 μA I_{GT} = 20 μA
	2N1929-35	1.1	25 thru 300	413	150.12	
C5 C511	2N2322-29 2N2322A-28A	1.6	25 thru 400	415 416 417	150.10	I_{GT} = 200 μA, TO-5 I_{GT} = 20 μA, TO-5 I_{GT} = 200 μA, diamond base
C6 C611		1.6	25 thru 200	418 419	150.8	TO-5 Diamond Base
C7	2N2344-48	1.6	25 thru 200	420	150.11	High Gate Sensitivity
	2N1595-99	1.6	50 thru 400	421	150.15	Low Holding Current
C11	2N1770-78 2N2619	7.4	25 thru 600	425	150.21	High Gate Sensitivity

2. MEDIUM CURRENT (10-50A) GENERAL PURPOSE INDUSTRIAL AND MILITARY SCR'S

	2N681-92	25	25 thru 800	432	160.20	No PFV Limit
C35		35	25 thru 800	434	160.22	

3. HIGH CURRENT (OVER 50A) GENERAL PURPOSE INDUSTRIAL AND MILITARY SCR'S

C45 C46		55	25 thru 900	439	170.17	Flag Type Terminals Flexible Cathode and Gate Leads
C50 C52	2N1909-16 2N1792-98	110	25 thru 900	441	170.20	Flag Type Terminals Flexible Cathode and Gate Leads
C500XI		1200	Up to 1800	453	170.61	Water Cooled

4. GENERAL PURPOSE, IMPROVED DYNAMIC CHARACTERISTIC SCR'S

C135	2N3753-61	35	50 thru 800	437	160.40	Guaranteed dv/dt Guaranteed di/dt
C137		35	500 thru 1200	438	160.45	Guaranteed dv/dt Guaranteed di/dt
C145		55	50 thru 1200	440	170.18	Guaranteed dv/dt Guaranteed di/dt
C150 thru C153		110	500 thru 1300	444 445	170.23	No PFV Limit Guaranteed dv/dt Guaranteed di/dt
C178		200	100 thru 1200	448	170.51	Guaranteed dv/dt Guaranteed di/dt
C280		235	700 thru 1700	450	170.58	Guaranteed di/dt
C290 C291		470	100 thru 1200	452	170.60	Guaranteed dv/dt Guaranteed di/dt
C350		110 avg.	500 thru 1300	447	170.54	New PRESS PAK Guaranteed dv/dt Guaranteed di/dt
C380		235 avg.	500 thru 1300	451	170.56	New PRESS PAK Guaranteed dv/dt Guaranteed di/dt

5. LIGHT INDUSTRIAL AND ECONOMY SCR'S (LIMITED TEMPERATURE)

GE Type	JEDEC No.	Forward Current I_f (RMS) Amp	Peak Voltage Range	Condensed Spec on Page	Complete Spec No	Comments
C106		2	30 thru 200	422	150.9	High Gate Sensitivity
C20/C22		7.4	25 thru 400	424	150.30	
C15		8	25 thru 400	427	150.22	Stud and Press Fit
C36		16	25 thru 400	428	160.21	
C37		25	25 thru 800	431	160.23	
C30, C32 C31, C33		25	25 thru 400	429 430	160.27	Stud and Press Fit Stud and Press Fit
6. HIGH TEMPERATURE SCR'S (150°C)						
C10	2N1770A-77A	7.4	25 thru 400	423	150.20	−65°C to 150°C
C38		35	25 thru 500	435	160.30	−65°C to 150°C
C60 C61	2N2023-29	110	25 thru 300	443	170.26	−65°C to 150°C −40°C to 150°C
7. FAST TURN-OFF SCR'S						
C9		1.1	25 thru 300	414	150.12	$t_{off} = 12$ μsec Max.
C12		7.4	25 thru 400	426	150.25	$t_{off} = 12$ μsec Max.
C40		35	25 thru 400	436	160.25	$t_{off} = 12$ μsec Max.
C55, C56		110	25 thru 600	442	170.21	$t_{off} = 12$ μsec Max.
C154 thru C157		110	100 thru 500	446	170.35	$t_{off} = 10$ μsec No PFV Limit
C180 C181 C185		235	100 thru 1300	449	170.52	I_{fm} Surge = 3500A I_{fm} Surge = 2500A I_{fm} Surge = 3500A
8. HIGH FREQUENCY SCR'S (UP TO 25K Hz)						
C140 C141	2N3549-53 2N3654-58	35	50 thru 400	433	160.35	High dv/dt, di/dt Short t_{off}
9. TRIACS						
SC40B SC41B		6	200	454	175.10	Stud Mount Press Fit
SC40D SC41D		6	400	454	175.15	Stud Mount Press Fit
SC45B SC46B		10	200	454	175.10	Stud Mount Press Fit
SC45D SC46D		10	400	454	175.15	Stud Mount Press Fit
10.LIGHT ACTIVATED SCR'S AND SCS'S						
L8 L811 L9 L911		1.6	25 thru 200	460	190.10	Light Activated SCR
L1V		175 ma Anode Current	40	458	55.41	Light Activated SCS

21.2 ALPHA-NUMERIC INDEX TO GENERAL ELECTRIC'S THYRISTORS

21.3 CONDENSED SPECIFICATIONS

21.3.1 SCR'S

CONDENSED SPECIFICATIONS—FOR COMPLETE SPECIFICATIONS SEE 150.5

.5A RMS SCR UP TO 200V

- Miniature TO-18 Package
- High Gate Sensitivity
- Low Holding Current
- Designed for Military Applications

2N877-2N881

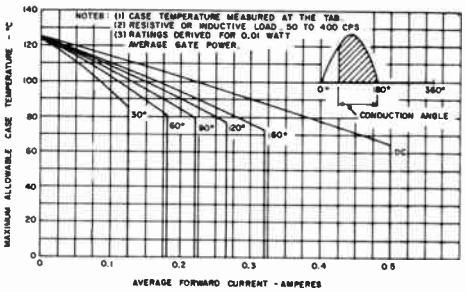
Outline Drawing No. 1

Types	Peak Forward Blocking Voltage, V_{FXM} $T_J = -65°C$ to $+125°C$ $R_{GK} = 1000$ Ohms Maximum	Working and Repetitive Peak Reverse Voltage, V_{ROM} (wkg) and V_{ROM} (rep) $T_J = -65°C$ to $+150°C$	Non-Repetitive Peak Reverse Voltage, V_{ROM} (non-rep) <5 Milliseconds $T_J = -65°C$ to $+125°C$
2N877	30 volts	30 volts	45 volts
2N878	60 volts	60 volts	90 volts
2N879	100 volts	100 volts	130 volts
2N880	150 volts	150 volts	200 volts
2N881	200 volts	200 volts	275 volts

MAXIMUM ALLOWABLE RATINGS AND CHARACTERISTICS

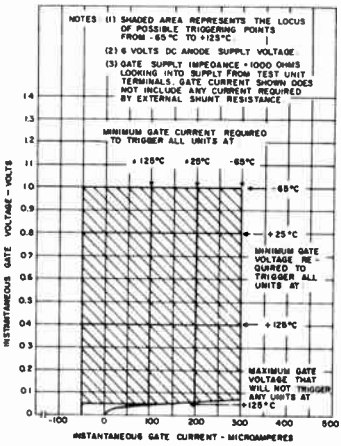
RMS Forward Current, On-state I_F ..... .5 Ampere
Average Forward Current, On-state $I_{F(AV)}$ ..... Depends on conduction angle (see chart)
Peak One Cycle Surge Forward Current (Non-repetitive), I_{FM} (surge) ..... 7 Amperes
Peak Reverse Gate Voltage, V_{GRM} ..... 6 Volts
Operating Temperature T_J ..... $-65°C$ to $+150°C$
Forward and Reverse Blocking Current* ..... I_{FX} I_{RX} Typ. 10/Max. 100 μAdc
Holding Current‡ ..... I_{HX} Typ. 1.7/Max. 5.0 mAdc
Turn-off Time† ..... t_{off} Typ. 15 μsec
dv/dt* ..... 40 Typ. V/μsec

‡$T_J = +25°C$, $R_{GK} = 1000$ ohms
*$T_J = +125°C$, $R_{GK} = 1000$ ohms
†$T_J = +125°C$, $R_{GK} = 100$ ohms



MAXIMUM ALLOWABLE CASE TEMPERATURE

(125°C JUNCTION TEMP.)



GATE TRIGGERING CHARACTERISTICS

CONDENSED SPECIFICATIONS—FOR COMPLETE SPECIFICATIONS SEE 150.5

.5A RMS SCR UP TO 200V

- Miniature TO-18 Package
- Very High Gate Sensitivity
- Low Holding Current
- Designed for Military Applications

2N885-2N889

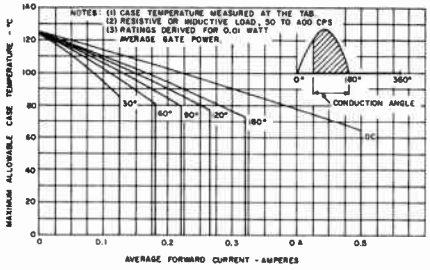
Outline Drawing No. 1

Types	Peak Forward Blocking Voltage, V_{FXM} $T_J = -65°C$ to $+125°C$ $R_{GK} = 1000$ Ohms Maximum	Working and Repetitive Peak Reverse Voltage, V_{ROM} (wkg) and V_{ROM} (rep) $T_J = -65°C$ to $+150°C$	Non-Repetitive Peak Reverse Voltage, V_{ROM} (non-rep) <5 Milliseconds $T_J = -65°C$ to $+125°C$
2N885	30 volts	30 volts	45 volts
2N886	60 volts	60 volts	90 volts
2N887	100 volts	100 volts	130 volts
2N888	150 volts	150 volts	200 volts
2N889	200 volts	200 volts	275 volts

MAXIMUM ALLOWABLE RATINGS AND CHARACTERISTICS

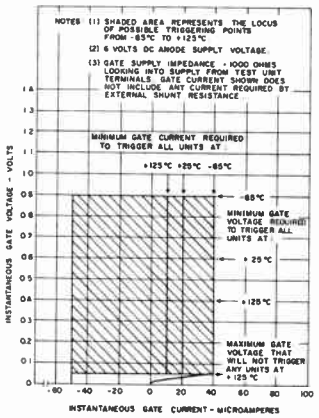
RMS Forward Current, On-state I_F ..... .5 Ampere
Average Forward Current, On-state $I_{F(AV)}$ ..... Depends on conduction angle (see chart)
Peak One Cycle Surge Forward Current (Non-repetitive), I_{FM} (surge) ..... 7 Amperes
Peak Reverse Gate Voltage, V_{GRM} ..... 6 Volts
Operating Temperature T_J ..... −65°C to +150°C
Forward and Reverse Blocking Current* ..... I_{FX} I_{RX} Typ. 10/Max. 20 μAdc
Holding Current‡ ..... I_{HX} Typ. 1.1/Max. 3 mAdc
Turn-off Time† ..... t_{off} Typ. 15 μsec
dv/dt* ..... 40 Typ. V/μsec

‡$T_J = +25°C$, $R_{GK} = 1000$ ohms
*$T_J = +125°C$, $R_{GK} = 1000$ ohms
†$T_J = +125°C$, $R_{GK} = 100$ ohms



MAXIMUM ALLOWABLE CASE TEMPERATURE

(125°C JUNCTION TEMP.)



GATE TRIGGERING CHARACTERISTICS

CONDENSED SPECIFICATIONS—FOR COMPLETE SPECIFICATIONS SEE 150.12

1.1A RMS SCR UP TO 300V

- Permits Point-to-Point Wiring
- Short Turn-off Time

2N1929-35

Outline Drawing No. 3

	2N1929	2N1930	2N1931	2N1932	2N1933	2N1934	2N1935
Repetitive Peak Reverse Voltage (PRV)*	25	50	100	150	200	250	300 volts
Minimum Forward Break-over Voltage (VBO)	25	50	100	150	200	250	300 volts
Transient Peak Reverse Voltage (Non-recurrent <5 millisec.)*	35	75	150	225	300	350	400 volts

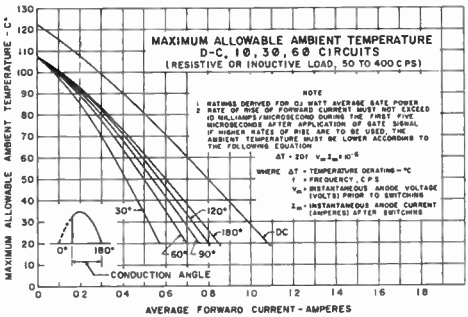
*PRV ratings apply for zero or negative gate voltage only.

MAXIMUM ALLOWABLE RATINGS AND CHARACTERISTICS

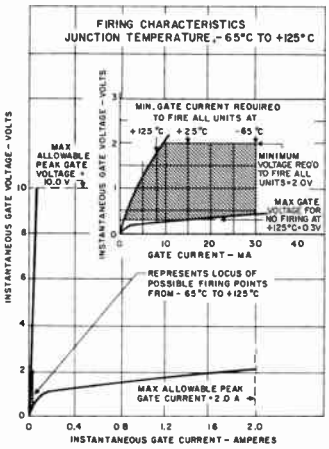
RMS Forward Current, On-state I_F ..... 1.1 Amperes
Average Forward Current, On-state $I_{F(AV)}$ ..... Depends on conduction angle (see chart)
Peak One Cycle Surge Forward Current (Non-repetitive), I_{FM} (surge) ..... 30 Amperes
Peak Reverse Gate Voltage, V_{GRM} ..... 10 Volts
Operating Temperature T_J ..... −65°C to +125°C

Maximum Reverse (I_R) or Forward (I_S) DC Leakage Current T_J = +125°C	2N1929	2N1930	2N1931	2N1932	2N1933	2N1934	2N1935
	4.0	4.0	2.0	1.5	1.1	1.0	0.9 Max. mAdc

Holding Current T_J = +25°C ..... I_{HX} Typ. 8 mAdc
Turn-off Time T_J = +125°C ..... t_{off} Typ. 6 μsec



MAXIMUM FORWARD CURRENT vs. AMBIENT TEMPERATURE



FIRING CHARACTERISTICS

CONDENSED SPECIFICATIONS—FOR COMPLETE SPECIFICATIONS SEE 150.12

1.1A RMS SCR UP TO 300V

- Permits Point-to-Point Wiring
- Guaranteed Turn-off Time Less Than 12 μSec.

C9

Outline Drawing No. 3

	C9U	C9F	C9A	C9G	C9B	C9H	C9C
Repetitive Peak Reverse Voltage (PRV)*	25	50	100	150	200	250	300 volts
Minimum Forward Break-over Voltage (VBO)	25	50	100	150	200	250	300 volts
Transient Peak Reverse Voltage (Non-recurrent <5 millisec.)*	35	75	150	225	300	350	400 volts

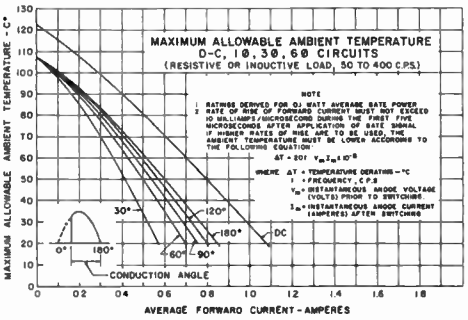
*PRV ratings apply for zero or negative gate voltage only.

MAXIMUM ALLOWABLE RATINGS AND CHARACTERISTICS

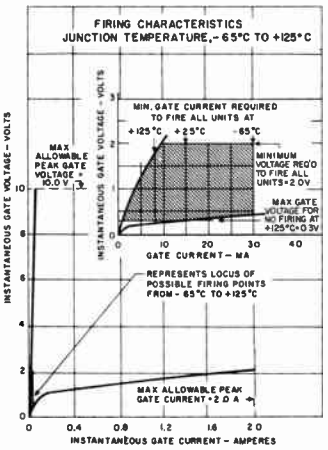
RMS Forward Current, On-state I_F ..... 1.1 Amperes
Average Forward Current, On-state $I_{F(AV)}$ ..... Depends on conduction angle (see chart)
Peak One Cycle Surge Forward Current (Non-repetitive), I_{FM} (surge) ..... 30 Amperes
Peak Reverse Gate Voltage, V_{GRM} ..... 10 Volts
Operating Temperature T_J ..... −65°C to +125°C
Maximum Reverse (I_R) or Forward (I_S) DC Leakage Current

C9U	C9F	C9A	C9G	C9B	C9H	C9C	
4.0	4.0	2.0	1.5	1.1	1.0	0.9	Max. mAdc

Holding Current $T_J = +25°C$ ..... I_{HX} Typ. 8 mAdc
Turn-off Time $T_J = +125°C$ ..... t_{off} Max. 12 μsec



MAXIMUM FORWARD CURRENT vs. AMBIENT TEMPERATURE



FIRING CHARACTERISTICS

CONDENSED SPECIFICATIONS—FOR COMPLETE SPECIFICATIONS SEE 150.10

1.6A RMS SCR UP TO 400V

- High Gate Sensitivity
- Standard TO-5 Package
- Ideal for Printed Circuit Applications
- Low Holding Current
- Designed to Meet Mil-S-19500/276 (Navy)

C5 (2N2322-29)

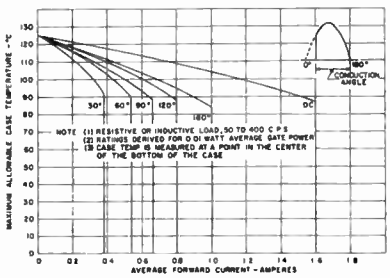
Outline Drawing No. 2

Types	Peak Forward Blocking Voltage, V_{FXM} $T_J = -65°C$ to $+125°C$ $R_{GK} = 1000$ Ohms	Working and Repetitive Peak Reverse Voltage, V_{ROM} (wkg) and V_{ROM} (rep) $T_J = -65°C$ to $+125°C$	Non-Repetitive Peak Reverse Voltage, V_{ROM} (non-rep) $\leq$5 Millisec. $T_J = -65°C$ to $+125°C$
C5U (2N2322)	25 volts	25 volts	40 volts
C5F (2N2323)	50 volts	50 volts	75 volts
C5A (2N2324)	100 volts	100 volts	150 volts
C5G (2N2325)	150 volts	150 volts	225 volts
C5B (2N2326)	200 volts	200 volts	300 volts
C5H (2N2327)	250 volts	250 volts	350 volts
C5C (2N2328)	300 volts	300 volts	400 volts
C5D (2N2329)	400 volts	400 volts	500 volts

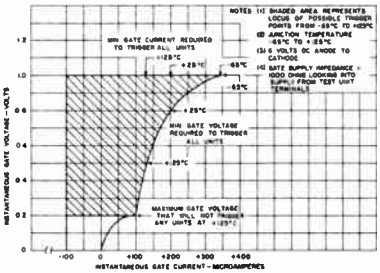
MAXIMUM ALLOWABLE RATINGS AND CHARACTERISTICS

RMS Forward Current, On-state I_F ..... 1.6 Amperes
Average Forward Current, On-state $I_{F(AV)}$ ..... Depends on conduction angle (see chart)
Peak One Cycle Surge Forward Current (Non-repetitive), I_{FM} (surge) ..... 15 Amperes
I^2t (for fusing) ..... .5 Ampere² seconds (for times $\geq$ 1.5 milliseconds)
Peak Reverse Gate Voltage, V_{GRM} ..... 6 Volts
Operating Temperature T_J ..... $-65°C$ to $+125°C$
Forward and Reverse Blocking Current* ..... I_{FX} I_{RX} Typ. 40/Max. 100 μAdc
Holding Current‡ ..... I_{HX} Typ. 1.0/Max. 2.0 mAdc
Turn-off Time† ..... t_{off} Typ. 40 μsec

‡$T_J = +25°C$, $R_{GK} = 1000$ ohms
*$T_J = +125°C$, $R_{GK} = 1000$ ohms
†$T_J = +125°C$, $R_{GK} = 100$ ohms



MAXIMUM ALLOWABLE CASE TEMPERATURE



GATE TRIGGERING CHARACTERISTICS

CONDENSED SPECIFICATIONS—FOR COMPLETE SPECIFICATIONS SEE 150.10

1.6A RMS SCR UP TO 400V

- Very High Gate Sensitivity
- Standard TO-5 Package
- Ideal for Printed Circuit Applications
- Low Holding Current
- Designed to Meet Mil-S-19500/276 (Navy)

2N2322A-28A

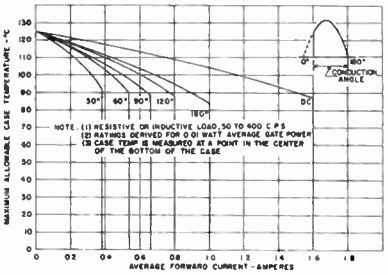
Outline Drawing No. 2

Types	Peak Forward Blocking Voltage, V_{FXM} $T_J = -65°C$ to $+125°C$ $R_{GK} = 2000$ Ohms	Working and Repetitive Peak Reverse Voltage, V_{ROM} (wkg) and V_{ROM} (rep) $T_J = -65°C$ to $+125°C$	Non-Repetitive Peak Reverse Voltage, V_{ROM} (non-rep) <5 Millisec. $T_J = -65°C$ to $+125°C$
2N2322A	25 volts	25 volts	40 volts
2N2323A	50 volts	50 volts	75 volts
2N2324A	100 volts	100 volts	150 volts
2N2325A	150 volts	150 volts	225 volts
2N2326A	200 volts	200 volts	300 volts
2N2327A	250 volts	250 volts	350 volts
2N2328A	300 volts	300 volts	400 volts

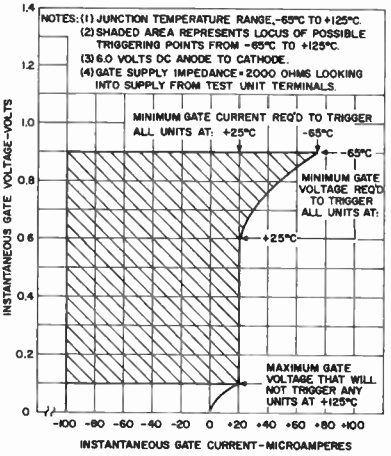
MAXIMUM ALLOWABLE RATINGS AND CHARACTERISTICS

RMS Forward Current, On-state I_F ..... 1.6 Amperes
Average Forward Current, On-state $I_{F(AV)}$ ..... Depends on conduction angle (see chart)
Peak One Cycle Surge Forward Current (Non-repetitive), I_{FM} (surge) ..... 15 Amperes
I^2t (for fusing) ..... .5 Ampere^2 seconds (for times $\geq$ 1.5 milliseconds)
Peak Reverse Gate Voltage, V_{GRM} ..... 6 Volts
Operating Temperature T_J ..... −65°C to +125°C
Forward and Reverse Blocking Current* ..... I_{FX} I_{RX} Typ. 40/Max. 100 μAdc
Holding Current‡ ..... I_{HX} Typ. 1.0/Max. 2.0 mAdc
Turn-off Time† ..... t_{off} Typ. 40 μsec

‡$T_J = +25°C$, $R_{GK} = 2000$ ohms
*$T_J = +125°C$, $R_{GK} = 2000$ ohms
†$T_J = +125°C$, $R_{GK} = 100$ ohms



MAXIMUM ALLOWABLE CASE TEMPERATURE



GATE TRIGGERING CHARACTERISTICS

CONDENSED SPECIFICATIONS—FOR COMPLETE SPECIFICATIONS SEE 150.10

1.6A RMS SCR UP TO 400V

- High Gate Sensitivity
- Diamond Flange Simplifies Heat Dissipation
- Low Holding Current

C511

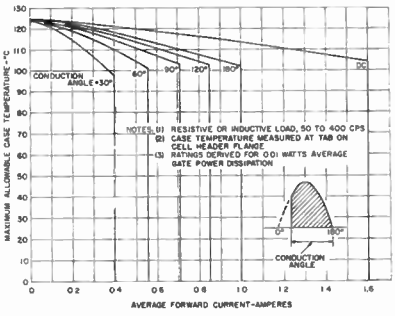
Outline Drawing No. 2

Types	Peak Forward Blocking Voltage, V_{FXM} $T_J = -65°C$ to $+125°C$ $R_{GK} = 1000$ Ohms	Working and Repetitive Peak Reverse Voltage, V_{ROM} (wkg) and V_{ROM} (rep) $T_J = -65°C$ to $+125°C$	Non-Repetitive Peak Reverse Voltage, V_{ROM} (non-rep) <5 Millisec. $T_J = -65°C$ to $+125°C$
C511U	25 volts	25 volts	40 volts
C511F	50 volts	50 volts	75 volts
C511A	100 volts	100 volts	150 volts
C511G	150 volts	150 volts	225 volts
C511B	200 volts	200 volts	300 volts
C511H	250 volts	250 volts	350 volts
C511C	300 volts	300 volts	400 volts
C511D	400 volts	400 volts	500 volts

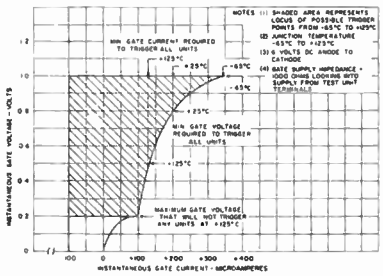
MAXIMUM ALLOWABLE RATINGS AND CHARACTERISTICS

RMS Forward Current, On-state I_F ..... 1.6 Amperes
Average Forward Current, On-state $I_{F(AV)}$ ..... Depends on conduction angle (see chart)
Peak One Cycle Surge Forward Current (Non-repetitive), I_{FM} (surge) ..... 15 Amperes
I^2t (for fusing) ..... .5 Ampere^2 seconds (for times $\geq$ 1.5 milliseconds)
Peak Reverse Gate Voltage, V_{GRM} ..... 6 Volts
Operating Temperature T_J ..... −65°C to +125°C
Forward and Reverse Blocking Current* ..... I_{FX} I_{RX} Typ. 40/Max. 100 μAdc
Holding Current‡ ..... I_{HX} Typ. 1.0/Max. 2.0 mAdc
Turn-off Time† ..... t_{OFF} Typ. 40 μsec

‡T_J = +25°C, R_{GK} = 1000 ohms
*T_J = +125°C, R_{GK} = 1000 ohms
†T_J = +125°C, R_{GK} = 100 ohms



MAXIMUM ALLOWABLE CASE TEMPERATURE



GATE TRIGGERING CHARACTERISTICS

CONDENSED SPECIFICATIONS—FOR COMPLETE SPECIFICATIONS SEE 150.8

1.6A RMS SCR UP TO 200V

- Low Cost
- Sensitive Gate
- Standard TO-5 Package
- Ideal for Printed Circuit Applications

C6

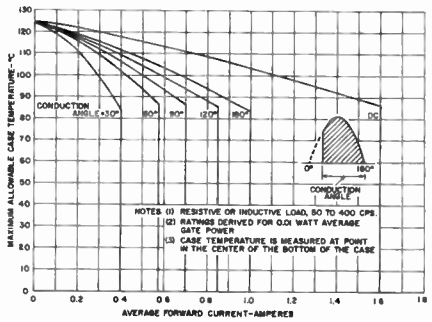
Outline Drawing No. 2

Types	Peak Forward Blocking Voltage, V_{FXM} $T_J = -40°C$ to $+125°C$ $R_{GK} = 1000$ Ohms	Working and Repetitive Peak Reverse Voltage, V_{ROM} (wkg) and V_{ROM} (rep) $T_J = -40°C$ to $+125°C$	Non-Repetitive Peak Reverse Voltage, V_{ROM} (non-rep) <5 Millisec. $T_J = -40°C$ to $+125°C$
C6U	25 volts	25 volts	40 volts
C6F	50 volts	50 volts	75 volts
C6A	100 volts	100 volts	150 volts
C6G	150 volts	150 volts	225 volts
C6B	200 volts	200 volts	300 volts

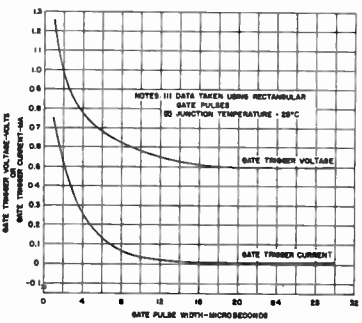
MAXIMUM ALLOWABLE RATINGS AND CHARACTERISTICS

RMS Forward Current, On-state I_F ..... 1.6 Amperes
Average Forward Current, On-state $I_{F(AV)}$ ..... Depends on conduction angle (see chart)
Peak One Cycle Surge Forward Current (Non-repetitive), I_{FM} (surge) ..... 10 Amperes
Peak Reverse Gate Voltage, V_{GRM} ..... 6 Volts
Operating Temperature T_J ..... −40°C to +125°C
Forward and Reverse Blocking Current* ..... I_{FX} I_{RX} Typ. 40/Max. 100 μAdc
Holding Current‡ ..... I_{HX} Typ. 1.0/Max. 5.0 mAdc
Turn-off Time† ..... t_{off} Typ. 40 μsec

‡$T_J = +25°C$, $R_{GK} = 1000$ ohms
*$T_J = +125°C$, $R_{GK} = 1000$ ohms
†$T_J = +125°C$, $R_{GK} = 100$ ohms



MAXIMUM ALLOWABLE CASE TEMPERATURE

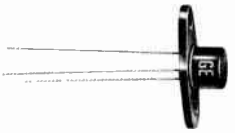


TYPICAL VARIATION OF GATE TRIGGER VOLTAGE AND CURRENT WITH GATE PULSE WIOTH

CONDENSED SPECIFICATIONS—FOR COMPLETE SPECIFICATIONS SEE 150.8

1.6A RMS SCR UP TO 200V

- Low Cost
- Sensitive Gate
- Diamond Flange Simplifies Heat Dissipation



C611

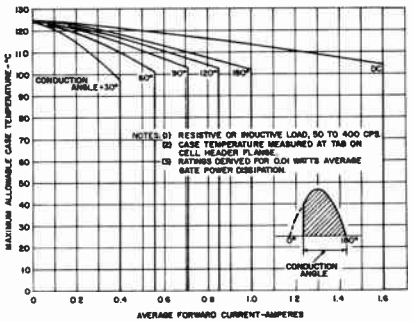
Outline Drawing No. 2

Types	Peak Forward Blocking Voltage, V_{FXM} $T_J = -40°C$ to $+125°C$ $R_{GK} = 1000$ Ohms	Working and Repetitive Peak Reverse Voltage, V_{ROM} (wkg) and V_{ROM} (rep) $T_J = -40°C$ to $+125°C$	Non-Repetitive Peak Reverse Voltage, V_{ROM} (non-rep) <5 Millisec. $T_J = -40°C$ to $+125°C$
C611U	25 volts	25 volts	40 volts
C611F	50 volts	50 volts	75 volts
C611A	100 volts	100 volts	150 volts
C611G	150 volts	150 volts	225 volts
C611B	200 volts	200 volts	300 volts

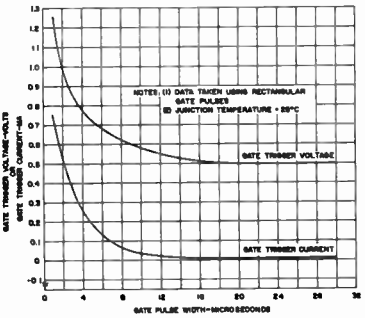
MAXIMUM ALLOWABLE RATINGS AND CHARACTERISTICS

RMS Forward Current, On-state I_F ..... 1.6 Amperes
Average Forward Current, On-state $I_{F(AV)}$ ..... Depends on conduction angle (see chart)
Peak One Cycle Surge Forward Current (Non-repetitive), I_{FM} (surge) ..... 10 Amperes
Peak Reverse Gate Voltage, V_{GRM} ..... 6 Volts
Operating Temperature T_J ..... −40°C to +125°C
Forward and Reverse Blocking Current* ..... I_{FX} I_{RX} Typ. 40/Max. 100 μAdc
Holding Current‡ ..... I_{HX} Typ. 1.0/Max. 5.0 mAdc
Turn-off Time† ..... t_{off} Typ. 40 μsec

‡T_J = +25°C, R_{GK} = 1000 ohms
*T_J = +125°C, R_{GK} = 1000 ohms
†T_J = +125°C, R_{GK} = 100 ohms



MAXIMUM ALLOWABLE CASE TEMPERATURE



TYPICAL VARIATION OF GATE TRIGGER VOLTAGE

CONDENSED SPECIFICATIONS—FOR COMPLETE SPECIFICATIONS SEE 150.11

1.6A RMS SCR UP TO 200V

- Very High Gate Sensitivity
- Standard TO-5 Package
- Ideal for Printed Circuit Applications
- Suitable for High R_{GK}
- Low Holding Current

C7 (2N2344-48)

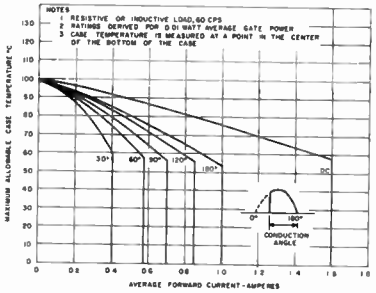
Outline Drawing No. 2

Types	Peak Forward Blocking Voltage, V_{FXM} $T_J = -65°C$ to $+100°C$ $R_{GK} = 40{,}000$ Ohms	Working and Repetitive Peak Reverse Voltage, V_{ROM} (wkg) and V_{ROM} (rep) $T_J = -65°C$ to $+100°C$	Non-Repetitive Peak Reverse Voltage, <5 Millisec. V_{ROM} (non-rep) $T_J = -65°C$ to $+100°C$
C7U (2N2344)	25 volts	25 volts	40 volts
C7F (2N2345)	50 volts	50 volts	75 volts
C7A (2N2346)	100 volts	100 volts	150 volts
C7G (2N2347)	150 volts	150 volts	225 volts
C7B (2N2348)	200 volts	200 volts	300 volts

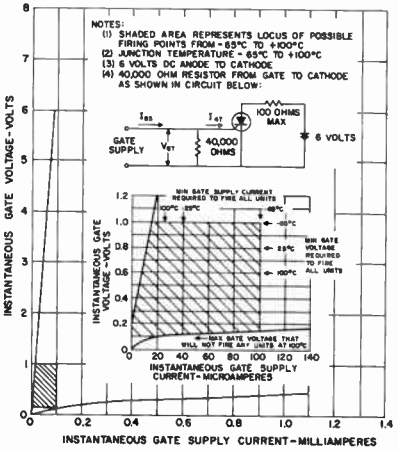
MAXIMUM ALLOWABLE RATINGS AND CHARACTERISTICS

RMS Forward Current, On-state I_F ..... 1.6 Amperes
Average Forward Current, On-state $I_{F(AV)}$ ..... Depends on conduction angle (see chart)
Peak One Cycle Surge Forward Current (Non-repetitive), I_{FM} (surge) ..... 15 Amperes
Peak Reverse Gate Voltage, V_{GRM} ..... 6 Volts
Operating Temperature T_J ..... −65°C to +100°C
Forward and Reverse Blocking Current* ..... I_{FX} I_{RX} Typ. 40/Max. 100 μAdc
Holding Current‡ ..... I_{HX} Typ. 0.2 Max. 1.0 mAdc
Turn-off Time† ..... t_{off} Typ. 20 μsec

‡T_J = +25°C, R_{GK} = 40,000 ohms
*T_J = +100°C, R_{GK} = 40,000 ohms
†T_J = +100°C, R_{GK} = 100 ohms



MAXIMUM ALLOWABLE CASE TEMPERATURE



GATE TRIGGERING CHARACTERISTIC

CONDENSED SPECIFICATIONS—FOR COMPLETE SPECIFICATIONS SEE 150.15

1.6A RMS SCR UP TO 400V

- Low Holding Current
- Standard TO-5 Package
- Ideal for Printed Circuit Application
- For Use in Low Power Switching and Control Applications

2N1595-99

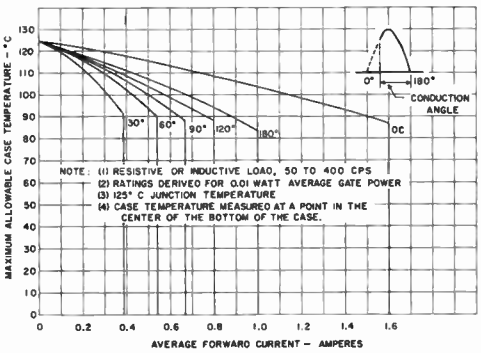
Outline Drawing No. 2

Type	Minimum Forward Breakover Voltage $V_{(BR)FO}$ $T_J = -65°C$ to $+125°C$ $R_{GK} = 1000$ Ohms	Repetitive Peak Reverse Voltage (PRV) $T_J = -65°C$ to $+150°C$
2N1595	50 volts	50 volts
2N1596	100 volts	100 volts
2N1597	200 volts	200 volts
2N1598	300 volts	300 volts
2N1599	400 volts	400 volts

MAXIMUM ALLOWABLE RATINGS AND CHARACTERISTICS

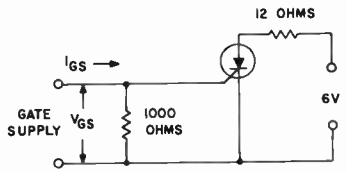
RMS Forward Current, On-state I_F ..... 1.6 Amperes
Average Forward Current, On-state $I_{F(AV)}$ ..... Depends on conduction angle (see chart)
Peak One Cycle Surge Forward Current (Non-repetitive), I_{FM} (surge) ..... 15 Amperes
Peak Reverse Gate Voltage, V_{GRM} ..... 6 Volts
Operating Temperature T_J ..... $-65°C$ to $+150°C$
Forward and Reverse Blocking Current* ..... I_{FX} I_{RX} Typ. 40/Max. 100 μAdc
Holding Current‡ ..... I_{HX} Typ. 0.5 mAdc
Turn-off Time† ..... t_{off} Typ. 20 μsec
Gate Current to Fire‡ ..... I_{GS} Typ. 0.9/Max. 10 mAdc
Gate Voltage to Fire‡ ..... V_{GF} Typ. 0.6/Max. 3.0 Vdc

‡$T_J = +25°C$, $R_{GK} = 1000$ ohms
*$T_J = +125°C$, $R_{GK} = 1000$ ohms
†$T_J = +125°C$, $R_{GK} = 100$ ohms



MAXIMUM ALLOWABLE CASE TEMPERATURE
(125°C Junction Temperature)

I_{GS} is defined in the circuit below:



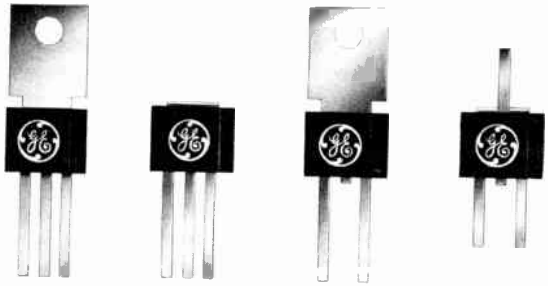
CONDENSED SPECIFICATIONS—FOR COMPLETE SPECIFICATIONS SEE 150.9

2A RMS SCR UP TO 200V

C106

Outline Drawing No. 6

- Very Low Cost
- High Gate Sensitivity
- Versatile Package Configurations
- Plastic Encapsulated
- Reliable



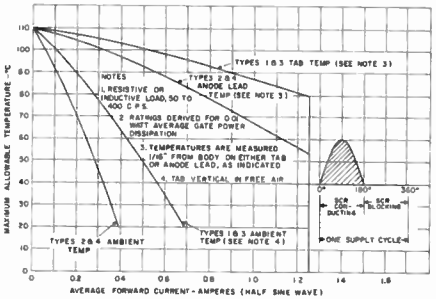
TYPE 1 **TYPE 2** **TYPE 3** **TYPE 4**

Type	Peak Forward Blocking Voltage, V_{FXM} R_{GK} = 1000 Ohms T_J = −40°C to +110°C	Working and Repetitive Peak Reverse Voltage, V_{ROM} (wkg) and V_{ROM} (rep) T_J = −40°C to +110°C
C106Y1, C106Y2, C106Y3, C106Y4	30 volts	30 volts
C106F1, C106F2, C106F3, C106F4	50 volts	50 volts
C106A1, C106A2, C106A3, C106A4	100 volts	100 volts
C106G1, C106G2, C106G3, C106G4	150 volts	150 volts
C106B1, C106B2, C106B3, C106B4	200 volts	200 volts

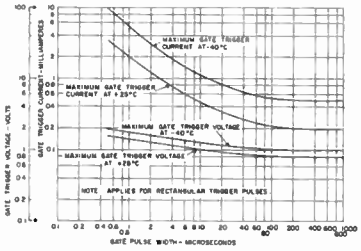
MAXIMUM ALLOWABLE RATINGS AND CHARACTERISTICS

RMS Forward Current, On-state I_F ..... 2.0 Amperes
Average Forward Current, On-state $I_{F(AV)}$ ..... Depends on conduction angle (see chart)
Peak One Cycle Surge Forward Current (Non-repetitive), I_{FM} (surge) ..... 15 Amperes
I^2t (for fusing) ..... 0.5 Ampere² seconds (for times ≧ 1.5 milliseconds)
Peak Reverse Gate Voltage, V_{GRM} ..... 6 Volts
Operating Temperature T_J ..... −40°C to +110°C
Forward and Reverse Blocking Current* ..... I_{FX} I_{RX} Typ. 10.0/Max. 100 μAdc
Holding Current‡ ..... I_{HX} Typ. 0.3/Max. 3 mAdc
Turn-off Time* ..... t_{off} Typ. 40/Max. 100 μsec
dv/dt* ..... Typ. 20V/μsec
di/dt ..... Max. 50 A/μsec

‡T_L = +25°C, R_{GK} = 1000 ohms
*T_L = +110°C, R_{GK} = 1000 ohms



MAXIMUM ALLOWABLE TEMPERATURES



MAXIMUM GATE TRIGGER CURRENT AND VOLTAGE VARIATION WITH TRIGGER PULSE WIDTH

CONDENSED SPECIFICATIONS—FOR COMPLETE SPECIFICATIONS SEE 150.20

7.4A RMS SCR UP TO 400V

- Designed to meet Mil-S-19500/168
- No Gate Bias Required
- Specified Maximum Holding Current
- Full $V_{(BR)F}$ ratings from −65°C to +150°C

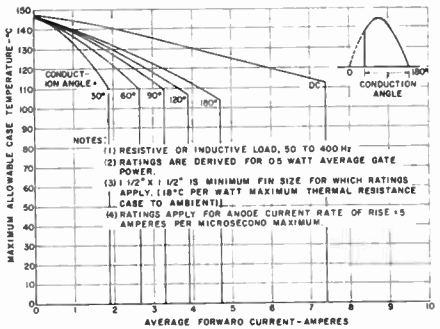
C10 (2N1770A-77A)

Outline Drawing No. 9

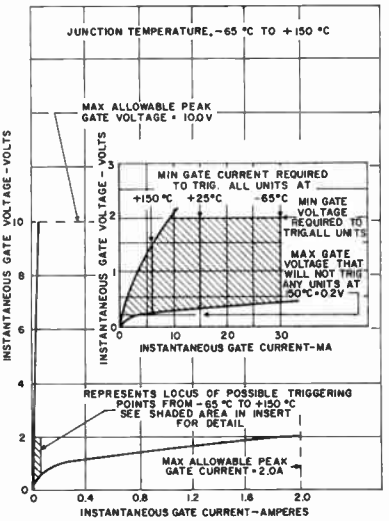
	(C10U) 2N1770A	(C10F) 2N1771A	(C10A) 2N1772A	(C10G) 2N1773A	(C10B) 2N1774A	(C10H) 2N1775A	(C10C) 2N1776A	(C10D) 2N1777A
Transient Peak Reverse Voltage, V_{ROM} (non rep) <5 millisec	35	75	150	225	300	350	400	500 volts
Repetitive Peak Reverse Voltage, V_{ROM} (rep)	25	50	100	150	200	250	300	400 volts
Minimum Forward Breakover Voltage, $V_{(BR)F}$	25	50	100	150	200	250	300	400 volts

MAXIMUM ALLOWABLE RATINGS AND CHARACTERISTICS

RMS Forward Current, On-state I_F ..... 7 Amperes
Average Forward Current, On-state $I_{F(AV)}$ ..... Depends on conduction angle (see chart)
Peak One Cycle Surge Forward Current (Non-repetitive), I_{FM} (surge) ..... 60 Amperes
I^2t (for fusing) ..... 4.9 Ampere² seconds (for times ≧ 1.5 milliseconds)
Peak Reverse Gate Voltage, V_{GRM} ..... 10 Volts
Operating Temperature T_J ..... −65°C to +150°C
Holding Current (T_J = +25°C) ..... I_{HX} Typ. 8/Max. 25 mAdc
Turn-off Time ..... t_{OFF} Typ. 10 μsec
dv/dt ..... not specified
di/dt ..... not specified



MAXIMUM ALLOWABLE STUD TEMPERATURE



TRIGGERING CHARACTERISTICS

CONDENSED SPECIFICATIONS—FOR COMPLETE SPECIFICATIONS SEE 150.22

8A RMS SCR UP TO 400V

- Ideal for Power Switching Applications
- Low Cost

C15

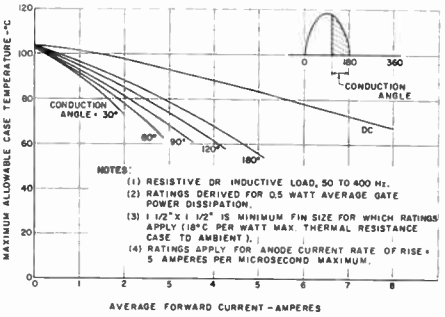
Outline Drawing No. 4

Type	Minimum Forward Breakover Voltage (V_{BO}) T_J = −65°C to +105°C	Repetitive Peak Reverse Voltage (PRV)* T_J = −65°C to +105°C	Transient Peak Reverse Voltage (Non-recurrent) <5 Millisec* T_J = −65°C to +105°C
C15U	25 volts	25 volts	40 volts
C15F	50 volts	50 volts	75 volts
C15A	100 volts	100 volts	150 volts
C15G	150 volts	150 volts	225 volts
C15B	200 volts	200 volts	300 volts
C15C	300 volts	300 volts	400 volts
C15D	400 volts	400 volts	500 volts

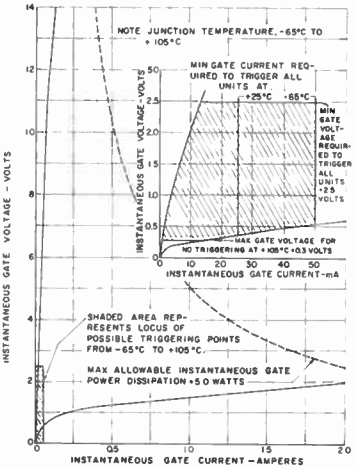
*Values apply for zero or negative gate voltage only. Maximum stud to ambient thermal resistance for which maximum PRV ratings apply equals 18°C/watt.

MAXIMUM ALLOWABLE RATINGS AND CHARACTERISTICS

RMS Forward Current, On-state I_F ..... 8.0 Amperes
Average Forward Current, On-state $I_{F(AV)}$ ..... Depends on conduction angle (see chart)
Peak One Cycle Surge Forward Current (Non-repetitive), I_{FM} (surge) ..... 60 Amperes
I^2t (for fusing) ..... 4.9 Ampere² seconds (for times ≧ 1.5 milliseconds)
Peak Reverse Gate Voltage, V_{GRM} ..... 10 Volts
Operating Temperature T_J ..... −65°C to +105°C
Forward and Reverse Blocking Current (T_J = 105°C) ..... I_{FX} I_{RX}
C15U-C15A/Max. 9.0 mAdc; C15G/Max. 8.0 mAdc; C15B/Max. 6.0 mAdc; C15C/Max. 4.0 mAdc; C15D/Max. 2.0 mAdc.
Holding Current (T_J = +25°C) ..... I_H Max. 30 ma



MAXIMUM ALLOWABLE CASE TEMPERATURE



TRIGGERING CHARACTERISTICS

CONDENSED SPECIFICATIONS—FOR COMPLETE SPECIFICATIONS SEE 150.21

7.4A RMS SCR UP TO 600V

- No Gate Bias Required
- High Gate Sensitivity
- Over 6 Years of Successful Field Experience

C11 (2N1770-78, 2N2619)

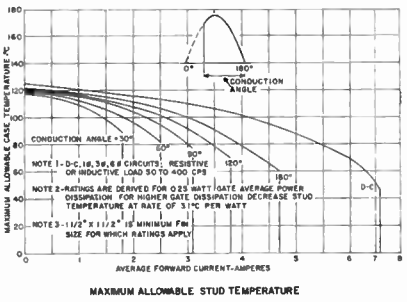
Outline Drawing No. 4

Type	Minimum Forward Breakover Voltage† $V_{(BR)FX}$ $T_J = -65°C$ to $+125°C$	Repetitive Peak Reverse Voltage† V_{ROM} (rep) $T_J = -65°C$ to $+125°C$	Non-Repetitive Peak Reverse Voltage, <5 Millisec† V_{ROM} (non-rep) $T_J = -65°C$ to $+125°C$
C11U (2N1770)	25 volts	25 volts	40 volts
C11F (2N1771)	50 volts	50 volts	75 volts
C11A (2N1772)	100 volts	100 volts	150 volts
C11G (2N1773)	150 volts	150 volts	225 volts
C11B (2N1774)	200 volts	200 volts	300 volts
C11H (2N1775)	250 volts	250 volts	350 volts
C11C (2N1776)	300 volts	300 volts	400 volts
C11D (2N1777)	400 volts	400 volts	500 volts
C11E (2N1778)	500 volts	500 volts	600 volts
C11M (2N2619)	600 volts	600 volts	720 volts

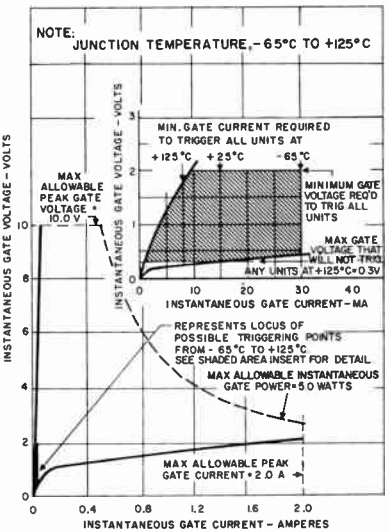
†Values apply for zero or negative gate voltage. Maximum case to ambient thermal resistance for which maximum V_{ROM} (rep) ratings apply = 18°C/watt.

MAXIMUM ALLOWABLE RATINGS AND CHARACTERISTICS

RMS Forward Current, On-state I_F ..... 7.4 Amperes
Average Forward Current, On-state $I_{F(AV)}$ ..... Depends on conduction angle (see chart)
Peak One Cycle Surge Forward Current (Non-repetitive), I_{FM} (surge) ..... 60 Amperes
I^2t (for fusing) ..... 4.9 Ampere² seconds (for times ≧ 1.5 milliseconds)
Peak Reverse Gate Voltage, V_{GRM} ..... 10 Volts
Operating Temperature T_J ..... −65°C to +125°C
Holding Current (T_J = +25°C) ..... I_H Typ. 8.0 mAdc
Turn-off Time (T_J = +125°C) ..... t_{off} Typ. 15 μsec



MAXIMUM ALLOWABLE STUD TEMPERATURE



TRIGGER CHARACTERISTICS

CONDENSED SPECIFICATIONS—FOR COMPLETE SPECIFICATIONS SEE 150.25

7.4A RMS SCR UP TO 400V

- Specially Designed for Inverter, Pulse Modulator, Chopper, Cycloconverter and Other High Frequency Applications.
- Guaranteed Turn-off Time of Less Than 12 μsec

C12

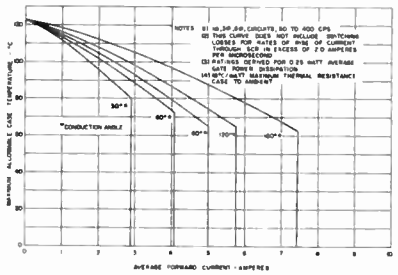
Outline Drawing No. 4

Type	Minimum Forward Breakover Voltage, $V_{(BR)FO}$* T_J = −65°C to +125°C	Repetitive Peak Reverse Voltage, $V_{ROM\ (rep)}$* T_J = −65°C to +125°C	Non-Repetitive Peak Reverse Voltage, <5.0 Millisec, $V_{ROM\ (non\text{-}rep)}$* T_J = −65°C to +125°C
C12U	25 volts	25 volts	40 volts
C12F	50 volts	50 volts	75 volts
C12A	100 volts	100 volts	150 volts
C12G	150 volts	150 volts	225 volts
C12B	200 volts	200 volts	300 volts
C12H	250 volts	250 volts	350 volts
C12C	300 volts	300 volts	400 volts
C12D	400 volts	400 volts	500 volts

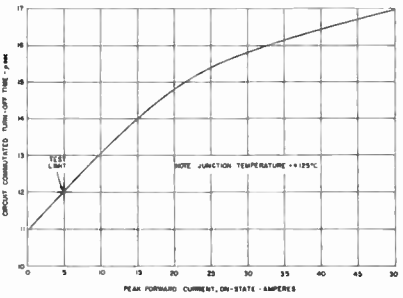
*Values apply for zero or negative gate voltage only. Maximum case to ambient thermal resistance of which maximum V_{ROM} (rep) ratings apply equals 18°C/watt.

MAXIMUM ALLOWABLE RATINGS AND CHARACTERISTICS

RMS Forward Current, On-state I_F ..... 7.4 Amperes
Average Forward Current, On-state $I_{F(AV)}$ ..... Depends on conduction angle (see chart)
Peak One Cycle Surge Forward Current (Non-repetitive), I_{FM} (surge) ..... 60 Amperes
I^2t (for fusing) ..... 40 Ampere² seconds (for times ≧ 1.5 milliseconds)
Peak Reverse Gate Voltage, V_{GRM} ..... 10 Volts
Operating Temperature T_J ..... −65°C to +125°C
Holding Current (T_J = +25°C) ..... I_H Typ. 8.0 mAdc
Turn-off Time (T_J = +125°C) ..... t_{off} Typ. 8.0/Max. 12 μsec



MAXIMUM ALLOWABLE CASE TEMPERATURE FOR RECTANGULAR CURRENT WAVEFORM



MAXIMUM CIRCUIT COMMUTATED TURN-OFF TIME vs. PEAK FORWARD CURRENT, ON-STATE

CONDENSED SPECIFICATIONS—FOR COMPLETE SPECIFICATIONS SEE 150.30

Outline Drawing No. 5

C20

C22

7.4A RMS SCR UP TO 400V

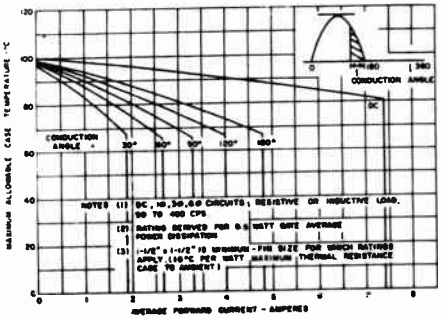
- Low Cost
- Flexibility of Mounting
- One-piece Terminals
- High Surge Current Capabilities
- Low Power Required for Triggering

Type	Minimum Forward Breakover Voltage, $V_{(BR)FO}$† $T_J = -25°C$ to $+100°C$	Repetitive Peak Reverse Voltage, $V_{ROM(rep)}$† $T_J = -25°C$ to $+100°C$	Non-repetitive Peak Reverse Voltage <5.0 millisec $V_{ROM(non\text{-}rep)}$† $T_J = -25°C$ to $+100°C$
C20U, C22U	25 volts	25 volts	35 volts
C20F, C22F	50 volts	50 volts	75 volts
C20A, C22A	100 volts	100 volts	150 volts
C20B, C22B	200 volts	200 volts	300 volts
C20C, C22C	300 volts	300 volts	400 volts
C20D, C22D	400 volts	400 volts	500 volts

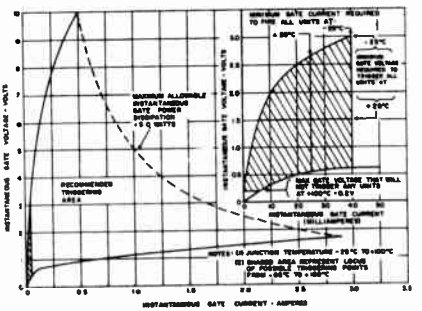
MAXIMUM ALLOWABLE RATINGS AND CHARACTERISTICS

RMS Forward Current, On-state I_F ..... 7.4 Amperes
Average Forward Current, On-state $I_{F(AV)}$ ..... Depends on conduction angle (see chart)
Peak One Cycle Surge Forward Current (Non-repetitive), I_{FM} (surge) ..... 80 Amperes
I^2t (for fusing) ..... 27 Ampere² seconds (for times ≥ 1.5 milliseconds)
Peak Reverse Gate Voltage, V_{GRM} ..... 5 Volts
Operating Temperature T_J ..... −25°C to +100°C
Peak Reverse and Forward Blocking Current (T_J = +100°C) ..... I_{ROM} and I_{FOM}
C20U, C22U Typ. 1.0/Max. 10.0 ma; C20F, C22F Typ. 1.0/Max. 10.0 ma: C20A, C22A Typ. 1.0/Max. 7.0 ma; C20B, C22B Typ. 1.0/Max. 3.5 ma; C20C, C22C Typ. 1.0/Max. 2.3 ma; C20D, C22D Typ. 1.0/Max. 1.7 ma.
Holding Current (T_J = +25°C) ..... I_{HX} Typ. 10/Max. 30 mAdc
Turn-off Time ..... t_{off} Not specified

‡Special selections of Gate Trigger Current down to 4.0 mAdc are available upon request.
†Values apply for zero or negative gate voltage only. Maximum case to ambient thermal resistance for which maximum V_{ROM} (rep) ratings apply equals 18°C/watt.



MAXIMUM ALLOWABLE CASE TEMPERATURE



GATE TRIGGERING CHARACTERISTICS‡

CONDENSED SPECIFICATIONS—FOR COMPLETE SPECIFICATIONS SEE 160.21

16A RMS SCR UP TO 500V

- Good Turn-off Time
- Ideal for Power Switching Applications

C36

Outline Drawing No. 7

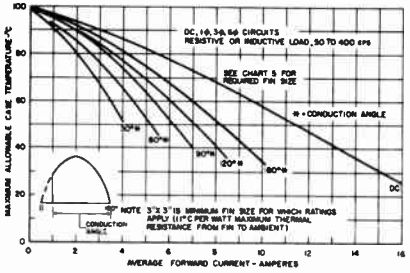
	C36U	C36F	C36A	C36G	C36B	C36H	C36C	C36D	C36E	
Repetitive Peak Reverse Voltage (PRV)*	25	50	100	150	200	250	300	400	500	volts
Minimum Forward Breakover Voltage (V_{BO})	25	50	100	150	200	250	300	400	500	volts
Transient Peak Reverse Voltage (Non-recurrent <5 millisec.)*	35	75	150	225	300	350	400	500	600	volts

MAXIMUM ALLOWABLE RATINGS AND CHARACTERISTICS

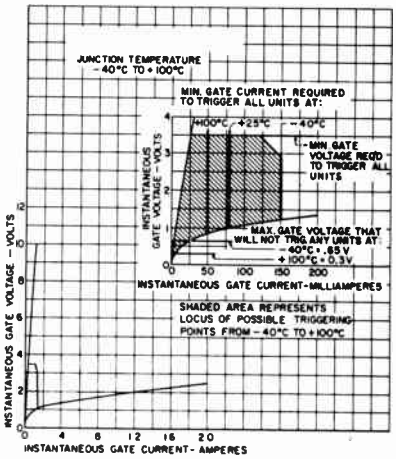
RMS Forward Current, On-state I_F ..... 16 Amperes
Average Forward Current, On-state $I_{F(AV)}$ ..... Depends on conduction angle (see chart)
Peak One Cycle Surge Forward Current (Non-repetitive), I_{FM} (surge) ..... 125 Amperes
I^2t (for fusing) ..... 40 Ampere² seconds (for times ≧ 1.5 milliseconds)
Peak Reverse Gate Voltage, V_{GRM} ..... 5 Volts
Operating Temperature T_J ..... −40°C to +100°C

	C36U	C36F	C36A	C36G	C36B	C36H	C36C	C36D	C36E	
Maximum Reverse (I_R) or Forward (I_S) Leakage Current (Full Cycle Average)*	Typ. 22.5	19.0	12.5	6.5	6.0	5.5	5.0	4.0	3.0	mAdc
Holding Current (T_J = +100°C)										I_{HX} Typ. 20 mAdc
Turn-off Time (T_J = +100°C)										t_{OFF} Typ. 15 μsec
dv/dt										not specified
di/dt										not specified

*PRV ratings apply for zero or negative gate voltage. For positive gate voltage applied simultaneously with PRV, see Application Notes. Maximum heat sink thermal resistance for which maximum PRV ratings apply equals 11.0°C/watt.



MAXIMUM ALLOWABLE STUD TEMPERATURE



FIRING CHARACTERISTICS

CONDENSED SPECIFICATIONS—FOR COMPLETE SPECIFICATIONS SEE 160.27

Outline Drawing No. 5

C30

C32

25A RMS SCR UP TO 400V

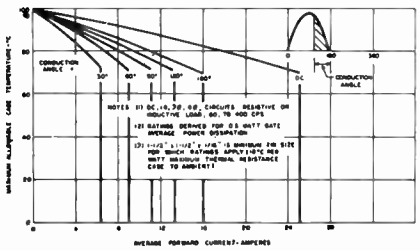
- Low Cost
- Flexibility of Mounting
- One-piece Terminals
- High Surge Current Capabilities
- Low Power Required for Triggering

Type	Peak Forward Blocking Voltage†, V_{FOM} $T_J = -40°C$ to $+100°C$	Repetitive Peak Reverse Voltage†, $V_{ROM(rep)}$ $T_J = -40°C$ to $+100°C$	Non-Repetitive Peak Reverse Voltage†, <5.0 Millisec V_{ROM} (non-rep) $T_J = -40°C$ to $+100°C$
C30U, C32U	25 volts	25 volts	35 volts
C30F, C32F	50 volts	50 volts	75 volts
C30A, C32A	100 volts	100 volts	150 volts
C30B, C32B	200 volts	200 volts	300 volts
C30C, C32C	300 volts	300 volts	400 volts
C30D, C32D	400 volts	400 volts	500 volts

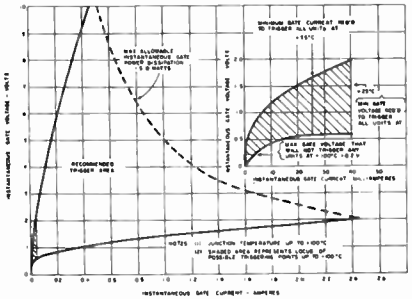
MAXIMUM ALLOWABLE RATINGS AND CHARACTERISTICS

RMS Forward Current, On-state I_F ..... 25 Amperes
Average Forward Current, On-state $I_{F(AV)}$ ..... Depends on conduction angle (see chart)
Peak One Cycle Surge Forward Current (Non-repetitive), I_{FM} (surge) ..... 250 Amperes
I^2t (for fusing) ..... 260 Ampere² seconds (for times ≧ 1.0 millisecond)
Peak Reverse Gate Voltage, V_{GRM} ..... 5.0 Volts
Operating Temperature T_J ..... −40°C to +100°C
Peak Reverse and Forward Blocking Current (T_J = +100°C) ..... I_R and I_F
C30U, C32U Typ. 1.0/Max. 10.0 mA; C30F, C32F Typ. 1.0/Max. 10.0 mA; C30A, C32A Typ. 1.0/Max. 7.0 mA; C30B, C32B Typ. 1.0/Max. 3.5 mA; C30C, C32C Typ. 1.0/Max. 2.3 mA; C30D, C32D Typ. 1.0/Max. 1.7 mA.
Holding Current (T_J = +25°C) ..... I_{HX} Typ. 10/Max. 50 mAdc
Turn-off Time ..... t_{OFF} not specified

†Values apply for zero or negative gate voltage only. Maximum case to ambient thermal resistance for which maximum $V_{ROM(rep)}$ ratings apply equals 18°C/watt.



MAXIMUM ALLOWABLE CASE TEMPERATURE



GATE TRIGGERING CHARACTERISTICS

CONDENSED SPECIFICATIONS—FOR COMPLETE SPECIFICATIONS SEE 160.27

Outline Drawing No. 5

C31

C33

25A RMS SCR UP TO 400V

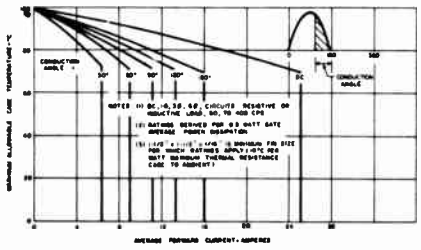
- Low Cost
- Flexibility of Mounting
- One-piece Terminals
- High Surge Current Capabilities
- High Gate Sensitivity

Type	Peak Forward Blocking Voltage†, V_{FOM} $T_J = -40°C$ to $+100°C$	Repetitive Peak Reverse Voltage†, $V_{ROM(rep)}$ $T_J = -40°C$ to $+100°C$	Non-Repetitive Peak Reverse Voltage†, <5.0 Millisec V_{ROM} (non-rep) $T_J = -40°C$ to $+100°C$
C31U, C33U	25 volts	25 volts	35 volts
C31F, C33F	50 volts	50 volts	75 volts
C31A, C33A	100 volts	100 volts	150 volts
C31B, C33B	200 volts	200 volts	300 volts
C31C, C33C	300 volts	300 volts	400 volts
C31D, C33D	400 volts	400 volts	500 volts

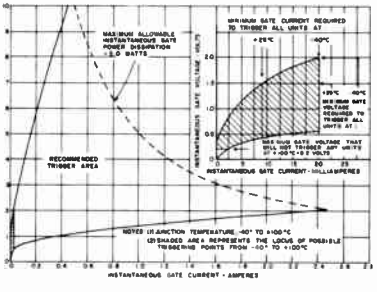
MAXIMUM ALLOWABLE RATINGS AND CHARACTERISTICS

RMS Forward Current, On-state I_F ..... 25 Amperes
Average Forward Current, On-state $I_{F(AV)}$ ..... Depends on conduction angle (see chart)
Peak One Cycle Surge Forward Current (Non-repetitive), I_{FM} (surge) ..... 250 Amperes
I^2t (for fusing) ..... 260 Ampere² seconds (for times $\geqq$ 1.0 millisecond)
Peak Reverse Gate Voltage, V_{GRM} ..... 5.0 Volts
Operating Temperature T_J ..... −40°C to +100°C
Peak Reverse and Forward Blocking Current† ($T_J = +100°C$) ..... I_{ROM} and I_{FOM}
C31U, C33U Typ. 1.0/Max. 10.0 mA; C31F, C33F Typ. 1.0/Max. 10.0 mA; C31A, C33A Typ. 1.0/Max. 7.0 mA; C31B, C33B Typ. 1.0/Max. 3.5 mA; C31C, C33C Typ. 1.0/Max. 2.3 mA: C31D, C33D Typ. 1.0/Max. 1.7 mA.
Holding Current ($T_J = +25°C$) ..... I_{HX} Typ. 10/Max. 50 mAdc
Turn-off Time ..... t_{off} not specified

†Values apply for zero or negative gate voltage only. Maximum case to ambient thermal resistance for which maximum $V_{ROM(rep)}$ ratings apply equals 18°C/watt.
‡Special selections of gate current to trigger available.



MAXIMUM ALLOWABLE CASE TEMPERATURE



GATE TRIGGERING CHARACTERISTICS‡

CONDENSED SPECIFICATIONS—FOR COMPLETE SPECIFICATIONS SEE 160.23

25A RMS SCR UP TO 800V

- Standard TO-48 Package
- Ideal for Power Switching Applications

C37

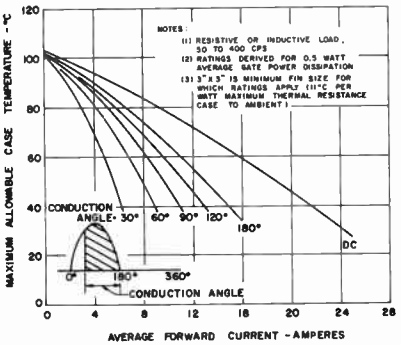
Outline Drawing No. 8

Type	Peak Forward Blocking Voltage, V_{FOM} T_C = −40°C to + 105°C	Peak Forward Voltage, PFV T_C = −40°C to + 105°C	Repetitive Peak Reverse Voltage, $V_{ROM(rep)}$† T_C = −40°C to + 105°C	Non-Repetitive Peak Reverse Voltage, V_{ROM} (non-rep)† T_C = −40°C to + 105°C
C37U	25 volts	480 volts	25 volts	40 volts
C37F	50 volts	480 volts	50 volts	75 volts
C37A	100 volts	480 volts	100 volts	150 volts
C37B	200 volts	480 volts	200 volts	300 volts
C37C	300 volts	480 volts	300 volts	400 volts
C37D	400 volts	500 volts	400 volts	500 volts
C37E	500 volts	600 volts	500 volts	600 volts
C37M	600 volts	720 volts	600 volts	720 volts
C37S	700 volts	840 volts	700 volts	840 volts
C37N	800 volts	960 volts	800 volts	960 volts

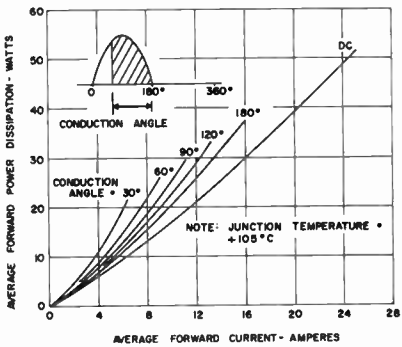
†Values apply for zero or negative gate voltage only. Maximum case to ambient thermal resistance for which maximum V_{FOM} and V_{ROM} ratings apply equals 11°C/watt.

MAXIMUM ALLOWABLE RATINGS AND CHARACTERISTICS

RMS Forward Current, On-state I_F ..... 25 Amperes
Average Forward Current, On-state $I_{F(AV)}$ ..... Depends on conduction angle (see chart)
Peak One Cycle Surge Forward Current (Non-repetitive), I_{FM} (surge) ..... 125 Amperes
I^2t (for fusing) ..... 40 Ampere² seconds (for times ≧ 1.5 milliseconds)
Operating Temperature T_J ..... −40°C to +105°C
Turn-off Time ..... t_{off} not specified
dv/dt ..... not specified
di/dt ..... not specified



MAXIMUM ALLOWABLE CASE TEMPERATURE



MAXIMUM POWER DISSIPATION

CONDENSED SPECIFICATIONS—FOR COMPLETE SPECIFICATIONS SEE 160.22

25A RMS SCR UP TO 800V

- Standard TO-48 Package
- 9 Years of Design and Field Experience

2N681-92

Outline Drawing No. 8

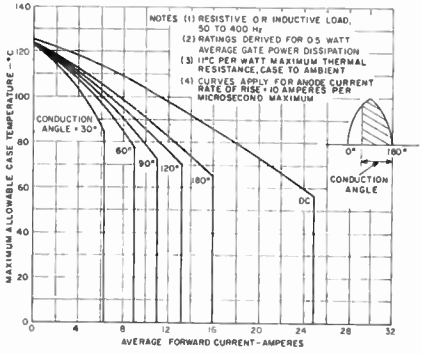
Type	Peak Forward Blocking Voltage, V_{FOM} $T_C = -65°C$ to $+125°C$	Peak Forward Voltage, PFV† $T_C = -65°C$ to $+125°C$	Repetitive Peak Reverse Voltage, $V_{ROM(rep)}$* $T_C = -65°C$ to $+125°C$	Non-Repetitive Peak Reverse Voltage, <5 Millisec. $V_{ROM(non\text{-}rep)}$* $T_C = -65°C$ to $+125°C$
2N681	25 volts	35 volts	25 volts	35 volts
2N682	50 volts	75 volts	50 volts	75 volts
2N683	100 volts	150 volts	100 volts	150 volts
2N684	150 volts	225 volts	150 volts	225 volts
2N685	200 volts	300 volts	200 volts	300 volts
2N686	250 volts	350 volts	250 volts	350 volts
2N687	300 volts	400 volts	300 volts	400 volts
2N688	400 volts	500 volts	400 volts	500 volts
2N689	500 volts	600 volts	500 volts	600 volts
2N690	600 volts	720 volts	600 volts	720 volts
2N691	700 volts	840 volts	700 volts	840 volts
2N692	800 volts	960 volts	800 volts	960 volts

*Values apply for zero or negative gate voltage only. Maximum case to ambient thermal resistance for which maximum V_{FOM} and V_{ROM} ratings apply equals 11°C/watt.

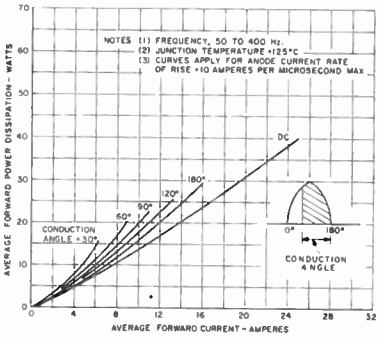
†Cells with higher PFV ratings are available upon request.

MAXIMUM ALLOWABLE RATINGS AND CHARACTERISTICS

RMS Forward Current, On-state I_F ..... 25 Amperes
Average Forward Current, On-state $I_{F(AV)}$ ..... Depends on conduction angle (see chart)
Peak One Cycle Surge Forward Current (Non-repetitive), I_{FM} (surge) ..... 150 Amperes
I^2t (for fusing) ..... 75 Ampere² seconds (for times ≥ 1.5 milliseconds)
Operating Temperature T_J ..... −65°C to +125°C
Turn-off Time ..... t_{off} Not specified
dv/dt ..... not specified
di/dt ..... not specified



MAXIMUM ALLOWABLE CASE TEMPERATURE



FORWARD POWER DISSIPATION

CONDENSED SPECIFICATIONS—FOR COMPLETE SPECIFICATIONS SEE 160.35

35A RMS SCR UP TO 400V

- Ideal for High Frequency Power Switching
- Up to 25KHz
- Guaranteed dv/dt
- Guaranteed di/dt
- Short Turn-off Time

C140 (2N3649-43)
C141 (2N3654-58)

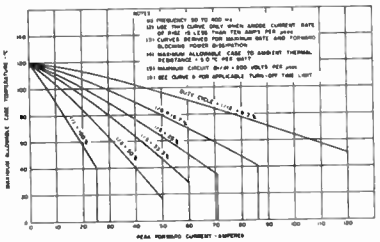
Outline Drawing No. 8

Type	DC Forward Blocking Voltage, V_{FO}† $T_C = -65°C$ to $+120°C$	Peak Forward Voltage, PFV† $T_C = -65°C$ to $+120°C$	DC Peak Reverse Voltage, V_{RO}† $T_C = -65°C$ to $+120°C$	Non-Repetitive Peak Reverse Voltage, (Half Sine Wave) V_{ROM}(non-rep)† $T_C = -65°C$ to $+120°C$
C140F (2N3649) C141F (2N3654)	50 volts	50 volts	50 volts	75 volts
C140A (2N3650) C141A (2N3655)	100 volts	100 volts	100 volts	150 volts
C140B (2N3651) C141B (2N3656)	200 volts	200 volts	200 volts	300 volts
C140C (2N3652) C141C (2N3657)	300 volts	300 volts	300 volts	400 volts
C140D (2N3653) C141D (2N3658)	400 volts	400 volts	400 volts	500 volts

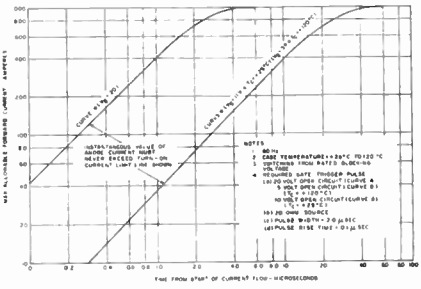
†Maximum case to ambient thermal resistance for which maximum V_{FO}, V_{RO} ratings apply equals 5°C/watt.

MAXIMUM ALLOWABLE RATINGS AND CHARACTERISTICS

RMS Forward Current, On-state I_F ..... 35 Amperes
Peak One Cycle Surge Forward Current (Non-repetitive), I_{FM} (surge) ..... 180 Amperes
I^2t (for fusing) ..... 165 Ampere² seconds (for times $\geq$ 1.0 millisecond)
Operating Temperature T_C ..... −65°C to +120°C
Turn-off Time ($T_C = +120°C$) ..... t_{off} C140 Max. 15 μsec; C141 Max. 10 μsec
dv/dt ($T_C = +120°C$) ..... Min. 200V/μsec



MAXIMUM ALLOWABLE CASE TEMPERATURE FOR RECTANGULAR CURRENT WAVEFORM



TURN-ON CURRENT LIMIT

CONDENSED SPECIFICATIONS—FOR COMPLETE SPECIFICATIONS SEE 160.20

35A RMS SCR UP TO 800V

- Compatible with 2N681-92
- Thermal Fatigue Free
- No Peak Forward Voltage Limitation
- Designed to Meet Mil-S-19500/108B
- 9 Years of Design and Field Experience
- Standard TO-48 Outline

C35

Outline Drawing No. 8

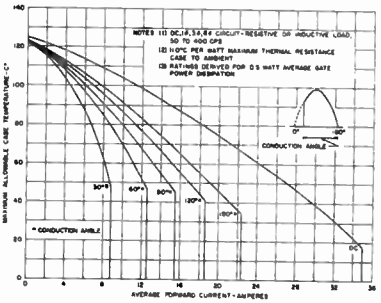
Type	Peak Forward Blocking Voltage, V_{FOM} $T_C = -65°C$ to $+125°C$	Repetitive Peak Reverse Voltage, V_{ROM}(rep)* $T_C = -65°C$ to $+125°C$	Non-Repetitive Peak Reverse Voltage, <5.0 Millisec V_{ROM}(non-rep)* $T_C = -65°C$ to $+125°C$
C35U	25 volts	25 volts	35 volts
C35F	50 volts	50 volts	75 volts
C35A	100 volts	100 volts	150 volts
C35G	150 volts	150 volts	225 volts
C35B	200 volts	200 volts	300 volts
C35H	250 volts	250 volts	350 volts
C35C	300 volts	300 volts	400 volts
C35D	400 volts	400 volts	500 volts
C35E	500 volts	500 volts	600 volts
C35M	600 volts	600 volts	720 volts
C35S	700 volts	700 volts	840 volts
C35N	800 volts	800 volts	960 volts

*Values apply for zero or negative gate voltage only. Maximum case to ambient thermal resistance for which maximum V_{FOM} and V_{ROM} ratings apply equals 11°C/watt.

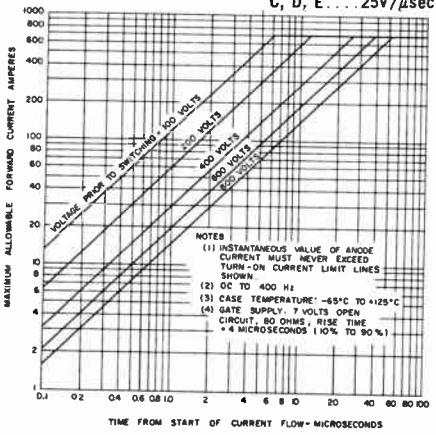
MAXIMUM ALLOWABLE RATINGS AND CHARACTERISTICS

RMS Forward Current, On-state I_F ..... 35 Amperes
Average Forward Current, On-state $I_{F(AV)}$ ..... Depends on conduction angle (see chart)
Peak One Cycle Surge Forward Current (Non-repetitive), I_{FM} (surge) ..... 150 Amperes
I^2t (for fusing) ..... 75 Ampere² seconds (for times ≥ 1.5 milliseconds)
Operating Temperature T_J ..... −65°C to +125°C
Turn-off Time† ..... t_{off} Max. 75 μsec
dv/dt (T_J = +125°C) ..... U, F, M, S, N....10V/μsec
A, G, B, H....20V/μsec
C, D, E....25V/μsec

†T_J = +125°C, R_{GK} = 100 ohms



MAXIMUM ALLOWABLE CASE TEMPERATURE



TURN-ON CURRENT LIMIT

CONDENSED SPECIFICATIONS—FOR COMPLETE SPECIFICATIONS SEE 160.30

35A RMS SCR UP TO 500V

- No Peak Forward Voltage Limitation
- Thermal Fatigue Free
- High Junction Temperature
- Low Thermal Resistance

C38

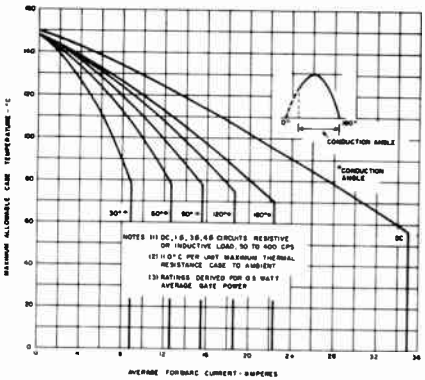
Outline Drawing No. 8

Type	Minimum Forward Breakover Voltage, $V_{(BR)FO}$* $T_J = -65°C$ to $+150°C$	Repetitive Peak Reverse Voltage, $V_{ROM(rep)}$* $T_J = -65°C$ to $+150°C$	Transient Peak Reverse Voltage, (Non-recurrent) <5.0 Millisec.* $T_J = -65°C$ to $+150°C$
C38U	25 volts	25 volts	35 volts
C38F	50 volts	50 volts	75 volts
C38A	100 volts	100 volts	150 volts
C38G	150 volts	150 volts	225 volts
C38B	200 volts	200 volts	300 volts
C38H	250 volts	250 volts	350 volts
C38C	300 volts	300 volts	400 volts
C38D	400 volts	400 volts	500 volts
C38E	500 volts	500 volts	600 volts

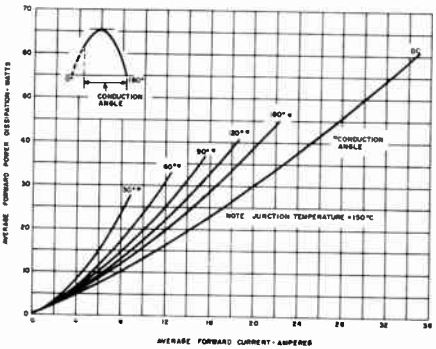
*Values apply for zero or negative gate voltage only. Maximum case to ambient thermal resistance for which maximum V_{ROM} ratings apply equals 11°C/watt.

MAXIMUM ALLOWABLE RATINGS AND CHARACTERISTICS

RMS Forward Current, On-state I_F ..... 35 Amperes
Average Forward Current, On-state $I_{F(AV)}$ ..... Depends on conduction angle (see chart)
Peak One Cycle Surge Forward Current (Non-repetitive), I_{FM} (surge) ..... 150 Amperes
I^2t (for fusing) ..... 75 Ampere² seconds (for times ≧ 1.5 milliseconds)
Operating Temperature T_J ..... −65°C to +150°C
Turn-off Time ($T_J = +150°C$) ..... t_{off} Typ. 24 μsec
dv/dt ($T_J = +150°C$) ..... Min. 20V/μsec
di/dt ..... not specified



MAXIMUM ALLOWABLE CASE TEMPERATURE



FORWARD POWER DISSIPATION

CONDENSED SPECIFICATIONS—FOR COMPLETE SPECIFICATIONS SEE 160.25

35A RMS SCR UP TO 400V

- Guaranteed Turn-off Time Less Than 12 μsec
- Specially Designed for Inverter and Chopper Applications

C40

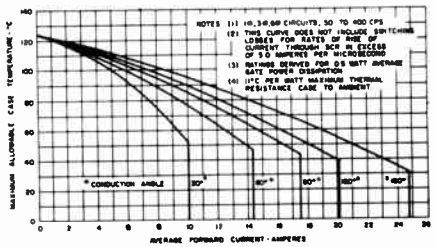
Outline Drawing No. 8

Type	Minimum Forward Breakover Voltage, $V_{(BR)FO}$* $T_C = -65°C$ to $+125°C$	Repetitive Peak Reverse Voltage, V_{ROM}(rep)* $T_C = -65°C$ to $+125°C$	Non-Repetitive Peak Reverse Voltage, <5.0 Millisec. V_{ROM}(non-rep)* $T_C = -65°C$ to $+125°C$
C40U	25 volts	25 volts	35 volts
C40F	50 volts	50 volts	75 volts
C40A	100 volts	100 volts	150 volts
C40G	150 volts	150 volts	225 volts
C40B	200 volts	200 volts	300 volts
C40H	250 volts	250 volts	350 volts
C40C	300 volts	300 volts	400 volts
C40D	400 volts	400 volts	500 volts

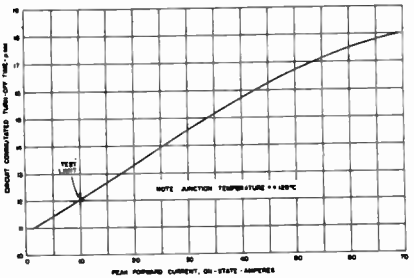
*Values apply for zero or negative gate voltage only. Maximum case to ambient thermal resistance for which maximum V_{ROM} (rep) ratings apply equals 11°C/watt.

MAXIMUM ALLOWABLE RATINGS AND CHARACTERISTICS

RMS Forward Current, On-state I_F ..... 35 Amperes
Average Forward Current, On-state $I_{F(AV)}$ ..... Depends on conduction angle (see chart)
Peak One Cycle Surge Forward Current (Non-repetitive), I_{FM} (surge) ..... 150 Amperes
I^2t (for fusing) ..... 75 Ampere² seconds (for times ≥ 1.5 milliseconds)
Operating Temperature T_C ..... −65°C to +125°C
Turn-off Time (T_C = +125°C) ..... t_{off} Max. 12 μsec
dv/dt (T_C = +125°C) ..... U, F, M, S, N Min. 10V/μsec
A, G, B, H Min. 20V/μsec
C, D, E Min. 25V/μsec
di/dt ..... same as C35



MAXIMUM ALLOWABLE CASE TEMPERATURE FOR RECTANGULAR CURRENT WAVEFORM



MAXIMUM CIRCUIT COMMUTATED TURN-OFF TIME vs. PEAK FORWARD CURRENT, ON-STATE

CONDENSED SPECIFICATIONS—FOR COMPLETE SPECIFICATIONS SEE 160.40

35A RMS SCR UP TO 800V

- Guaranteed dv/dt (200V/μsec)
- Guaranteed di/dt (200A/μsec)

C135 (2N3753-61)

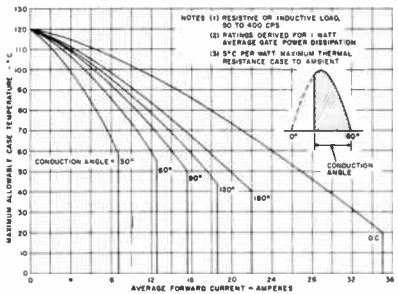
Outline Drawing No. 8

Type	Peak Forward Blocking Voltage, V_{FOM} $T_C = -40°C$ to $+120°C$	Peak Forward Voltage, PFV $T_C = -40°C$ to $+120°C$	Repetitive Peak Reverse Voltage, $V_{ROM(rep)}$*. $T_C = -40°C$ to $+120°C$	Non-Repetitive Peak Reverse Voltage, <5 Millisec. $V_{ROM(non\text{-}rep)}$* $T_C = -40°C$ to $+120°C$
C135F (2N3753)	50 volts	75 volts	50 volts	75 volts
C135A (2N3754)	100 volts	150 volts	100 volts	150 volts
C135B (2N3755)	200 volts	300 volts	200 volts	300 volts
C135C (2N3756)	300 volts	400 volts	300 volts	400 volts
C135D (2N3757)	400 volts	500 volts	400 volts	500 volts
C135E (2N3758)	500 volts	600 volts	500 volts	600 volts
C135M (2N3759)	600 volts	720 volts	600 volts	720 volts
C135S (2N3760)	700 volts	840 volts	700 volts	840 volts
C135N (2N3761)	800 volts	960 volts	800 volts	960 volts

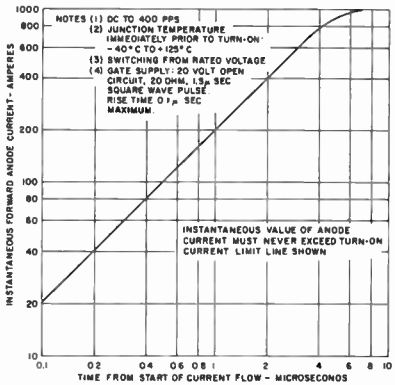
*Values apply for zero or negative gate voltage only. Maximum case to ambient thermal resistance for which maximum V_{FOM} and V_{ROM} ratings apply equals 5°C/watt.

MAXIMUM ALLOWABLE RATINGS AND CHARACTERISTICS

RMS Forward Current, On-state I_F ..... 35 Amperes
Average Forward Current, On-state $I_{F(AV)}$ ..... Depends on conduction angle (see chart)
Peak One Cycle Surge Forward Current (Non-repetitive), I_{FM} (surge) ..... 250 Amperes
I^2t (for fusing) ..... 100 Ampere² seconds (for times ≧ 1.0 millisecond)
Operating Temperature T_J ..... −40°C to +125°C
Turn-off Time (T_J = +120°C) ..... t_{off} Max. 75 μsec
dv/dt (T_J = +120°C) ..... Min. 200V/μsec



MAXIMUM ALLOWABLE CASE TEMPERATURE



TURN-ON CURRENT LIMIT

CONDENSED SPECIFICATIONS—FOR COMPLETE SPECIFICATIONS SEE 160.45

35A RMS SCR UP TO 1200V

- Guaranteed di/dt (150A/μsec)
- Guaranteed dv/dt (100V/μsec)
- No Peak Forward Voltage Limitation

C137

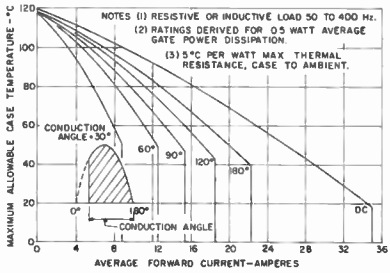
Outline Drawing No. 8

Type	Peak Forward Blocking Voltage, V_{FOM} $T_C = -40°C$ to $+120°C$	Repetitive Peak Reverse Voltage, $V_{ROM(rep)}$* $T_C = -40°C$ to $+120°C$	Non-Repetitive Peak Reverse Voltage, <5.0 Millisec. $V_{ROM(non\text{-}rep)}$* $T_C = -40°C$ to $+120°C$
C137E	500 volts	500 volts	600 volts
C137M	600 volts	600 volts	720 volts
C137N	800 volts	800 volts	960 volts
C137P	1000 volts	1000 volts	1200 volts
C137PB	1200 volts	1200 volts	1440 volts

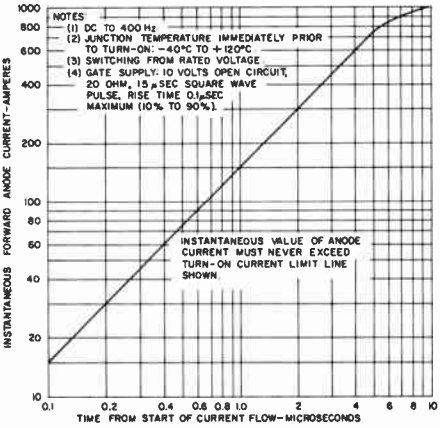
MAXIMUM ALLOWABLE RATINGS AND CHARACTERISTICS

RMS Forward Current, On-state I_F ..... 35 Amperes
Average Forward Current, On-state $I_{F(AV)}$ ..... Depends on conduction angle (see chart)
Peak One Cycle Surge Forward Current (Non-repetitive), I_{FM} (surge) ..... 360 Amperes
I^2t (for fusing) ..... 300 Ampere² seconds (for times $\geqq$ 1.0 millisecond)
Operating Temperature T_J ..... −40°C to +120°C
Turn-off Time ($T_C = +120°C$) ..... t_{off} Max. 75 μsec
dv/dt ($T_C = +120°C$) ..... Min. 100V/μsec

*Values apply for zero or negative gate voltage only. Maximum case to ambient thermal resistance for which maximum V_{FOM} and V_{ROM} ratings apply equals 5.0°C/watt.



MAXIMUM ALLOWABLE CASE TEMPERATURE



TURN-ON CURRENT LIMIT

CONDENSED SPECIFICATIONS—FOR COMPLETE SPECIFICATIONS SEE 170.17

C45

Outline Drawing No. 10

C46

Outline Drawing No. 11

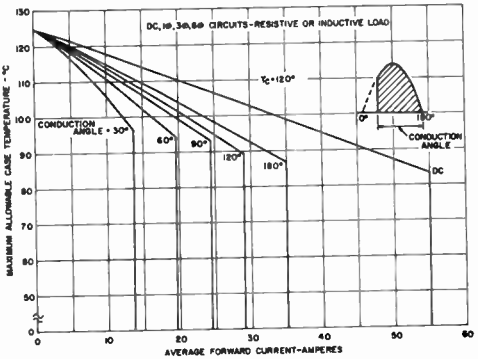
55A RMS SCR UP TO 900V

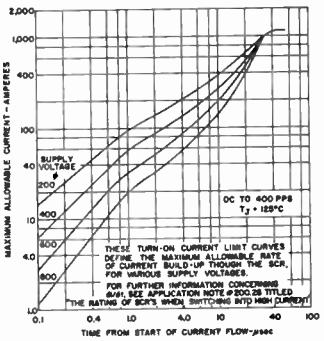
- Choice of Flag or Flexible Cathode and Gate Terminals
- Thermal Fatigue Resistant
- No Peak Forward Voltage Limitation on Units Rated 500 Volts and Above

Type	Minimum Forward Breakover Voltage, $V_{(BR)FO}$ $T_J = -40°C$ to $+125°C$	Repetitive Peak Reverse Voltage, V_{ROM}(rep) $T_J = -40°C$ to $+125°C$	Non-Repetitive Peak Reverse Voltage, <5.0 Millisec. V_{ROM} (non-rep) $T_J = -40°C$ to $+125°C$	Peak Forward Voltage, PFV
C45U, C46U	25 volts	25 volts	35 volts	500 volts
C45F, C46F	50 volts	50 volts	75 volts	500 volts
C45A, C46A	100 volts	100 volts	150 volts	500 volts
C45G, C46G	150 volts	150 volts	225 volts	500 volts
C45B, C46B	200 volts	200 volts	300 volts	500 volts
C45H, C46H	250 volts	250 volts	350 volts	500 volts
C45C, C46C	300 volts	300 volts	400 volts	500 volts
C45D, C46D	400 volts	400 volts	500 volts	500 volts
C45E, C46E	500 volts	500 volts	650 volts	No Limitation
C45M, C46M	600 volts	600 volts	720 volts	No Limitation
C45S, C46S	700 volts	700 volts	840 volts	No Limitation
C45N, C46N	800 volts	800 volts	960 volts	No Limitation
C45T, C46T	900 volts	900 volts	1040 volts	No Limitation

MAXIMUM ALLOWABLE RATINGS AND CHARACTERISTICS

RMS Forward Current, On-state I_F ..... 55 Amperes
Average Forward Current, On-state $I_{F(AV)}$ ..... Depends on conduction angle (see chart)
Peak One Cycle Surge Forward Current (Non-repetitive), I_{FM} (surge) ..... 700 Amperes
I^2t (for fusing) ..... 2000 Ampere² seconds (for times ≧ 1.5 milliseconds)
Operating Temperature T_J ..... −40°C to +125°C
Turn-off Time (T_J = +125°C) ..... t_{off} Typ. 30 μsec
dv/dt (T_J = +120°C) ..... U, F, A, G, B, H Typ. 30V/μsec
C, D, E, M Typ. 20V/μsec
S, N, T Typ. 15V/μsec





MAXIMUM ALLOWABLE CASE TEMPERATURE **CURRENT LIMIT FOR STEEP WAVEFORM OPERATION**

CONDENSED SPECIFICATIONS—FOR COMPLETE SPECIFICATIONS SEE 170.18

55A RMS SCR UP TO 1200V

- Guaranteed di/dt rating of 50 amps/μsec
- Guaranteed dv/dt rating of 200 volts/μsec
- Reduced Package Size, Mounted on a $\frac{5}{16}$ Inch Stud

C145

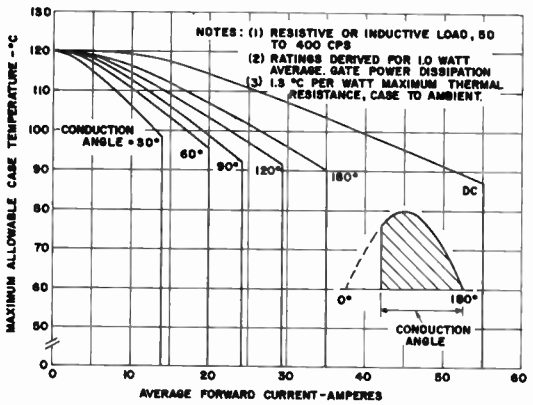
Outline Drawing No. 12

Type	Peak Forward Blocking Voltage, V_{FOM} $T_C = -40°C$ to $+120°C$	Peak Forward Voltage, PFV $T_C = -40°C$ to $+120°C$	Repetitive Peak Reverse Voltage, $V_{ROM(rep)}$* $T_C = -40°C$ to $+120°C$	Non-Repetitive Peak Reverse Voltage, <5 Millisec $V_{ROM(non\text{-}rep)}$* $T_C = -40°C$ to $+120°C$
C145F	50 volts	75 volts	50 volts	75 volts
C145A	100 volts	150 volts	100 volts	150 volts
C145B	200 volts	300 volts	200 volts	300 volts
C145C	300 volts	400 volts	300 volts	400 volts
C145D	400 volts	500 volts	400 volts	500 volts
C145E	500 volts	600 volts	500 volts	600 volts
C145M	600 volts	720 volts	600 volts	720 volts
C145S	700 volts	840 volts	700 volts	840 volts
C145N	800 volts	960 volts	800 volts	960 volts
C145T	900 volts	1080 volts	900 volts	1080 volts
C145P	1000 volts	1200 volts	1000 volts	1200 volts
C145PA	1100 volts	1320 volts	1100 volts	1320 volts
C145PB	1200 volts	1440 volts	1200 volts	1440 volts

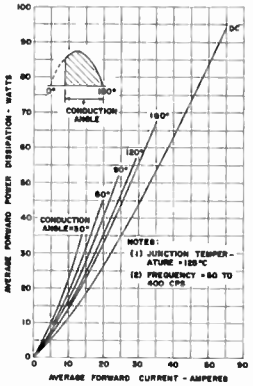
*Values apply for zero or negative gate voltage only. Maximum case to ambient thermal resistance for which maxium V_{FOM} and V_{ROM} ratings apply equals 1.3°C/watt.

MAXIMUM ALLOWABLE RATINGS AND CHARACTERISTICS

RMS Forward Current, On-state I_F ..... 55 Amperes
Average Forward Current, On-state $I_{F(AV)}$ ..... Depends on conduction angle (see chart)
Peak One Cycle Surge Forward Current (Non-repetitive), I_{FM} (surge) ..... 700 Amperes
I^2t (for fusing) ..... 2000 Ampere² seconds (for times $\geq$ 1.5 milliseconds)
Operating Temperature T_J ..... −40°C to +125°C
Turn-off Time ..... not specified
dv/dt (T_J = +120°C) ..... Min. 200V/μsec



MAXIMUM ALLOWABLE CASE TEMPERATURE



MAXIMUM FORWARD POWER DISSIPATION

CONDENSED SPECIFICATIONS—FOR COMPLETE SPECIFICATIONS SEE 170.20

C50 (2N1909-16)
Outline Drawing No. 11

C52 (2N1792-98)
Outline Drawing No. 10

110A RMS SCR UP TO 900V

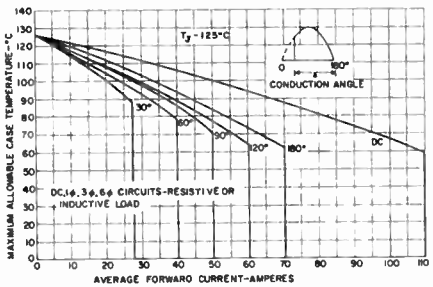
- Designed to Meet MIL-S-19500/204A
- Backed by 6 Years of Design and Field Experience
- Thermal Fatigue Resistant
- Immunity to Forward Voltage Destruction
- Choice of Flag or Flexible Cathode and Gate Terminals

Type				Minimum Forward Breakover Voltage, $V_{(BR)FO}$ $T_J = -40°C$ to $+125°C$	Repetitive Peak Reverse Voltage, $V_{ROM(rep)}$ $T_J = -40°C$ to $+125°C$	Non-Repetitive Peak Reverse Voltage, <5.0 millisec. V_{ROM} (non-rep) $T_J = -40°C$ to $+125°C$	Peak Forward Voltage, PFV*
C50U	(2N1909)	C52U		25 volts	25 volts	35 volts	500 volts
C50F	(2N1910)	C52F	(2N1792)	50 volts	50 volts	75 volts	500 volts
C50A	(2N1911)	C52A	(2N1793)	100 volts	100 volts	150 volts	500 volts
C50G	(2N1912)	C52G	(2N1794)	150 volts	150 volts	225 volts	500 volts
C50B	(2N1913)	C52B	(2N1795)	200 volts	200 volts	300 volts	500 volts
C50H	(2N1914)	C52H	(2N1796)	250 volts	250 volts	350 volts	500 volts
C50C	(2N1915)	C52C	(2N1797)	300 volts	300 volts	400 volts	500 volts
C50D	(2N1916)	C52D	(2N1798)	400 volts	400 volts	500 volts	500 volts
C50E		C52E		500 volts	500 volts	650 volts	No Limitation
C50M		C52M		600 volts	600 volts	720 volts	No Limitation
C50S		C52S		700 volts	700 volts	840 volts	No Limitation
C50N		C52N		800 volts	800 volts	960 volts	No Limitation
C50T		C52T		900 volts	900 volts	1040 volts	No Limitation

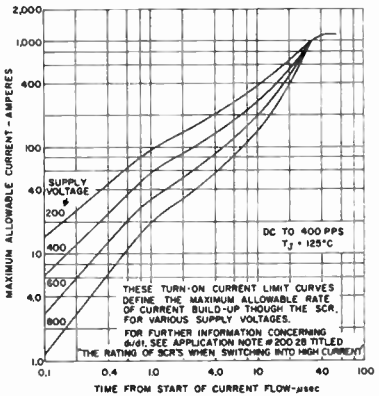
*Device may be safely switched into the forward conducting state by anode voltage.

MAXIMUM ALLOWABLE RATINGS AND CHARACTERISTICS

RMS Forward Current, On-state I_F ..... 110 Amperes
Average Forward Current, On-state $I_{F(AV)}$ ..... Depends on conduction angle (see chart)
Peak One Cycle Surge Forward Current (Non-repetitive), I_{FM} (surge) ..... 1000 Amperes
I^2t (for fusing) ..... 4000 Ampere² seconds (for times ≧ 1.5 milliseconds)
Operating Temperature T_J ..... $-40°C$ to $+125°C$
Turn-off Time ($T_C = +120°C$) ..... t_{off} Typ. 30 μsec
dv/dt ($T_C = +120°C$) ..... U, F, A, G, B, H Typ. 30V/μsec
C, D, E, M Typ. 20V/μsec
S, N, T Typ. 15V/μsec



MAXIMUM ALLOWABLE CASE TEMPERATURE



CURRENT LIMIT FOR STEEP WAVEFORM OPERATION

CONDENSED SPECIFICATIONS—FOR COMPLETE SPECIFICATIONS SEE 170.21

C55

Outline Drawing No. 11

C56

Outline Drawing No. 10

110A RMS SCR UP TO 600V

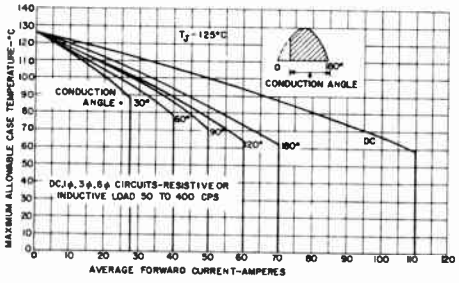
- Thermal Fatigue Resistant
- Choice of Flag or Flexible Cathode and Gate Terminals
- No Peak Forward Voltage Limitation on Units Rated 500 Volts and Above
- Specially Designed for Inverter and Chopper Applications
- Insured Turn-off Time of Less than 20 μsec

Type	Peak Forward Blocking Voltage, V_{FOM}* $T_C = -40°C$ to $+120°C$	Repetitive Peak Reverse Voltage, $V_{ROM(rep)}$* $T_C = -40°C$ to $+120°C$	Non-Repetitive Peak Reverse Voltage, <5 Millisec $V_{ROM(non\text{-}rep)}$* $T_C = -40°C$ to $+120°C$
C55, C56U	25 volts	25 volts	35 volts
C55, C56F	50 volts	50 volts	75 volts
C55, C56A	100 volts	100 volts	150 volts
C55, C56G	150 volts	150 volts	225 volts
C55, C56B	200 volts	200 volts	300 volts
C55, C56H	250 volts	250 volts	350 volts
C55, C56C	300 volts	300 volts	400 volts
C55, C56D	400 volts	400 volts	500 volts
C55, C56E	500 volts	500 volts	650 volts
C55, C56M	600 volts	600 volts	720 volts

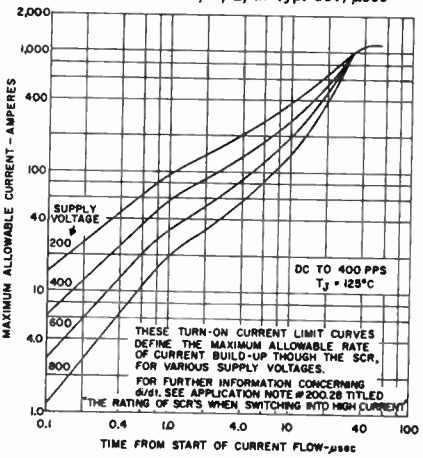
*Values apply for zero or negative gate voltage only. Maximum case to ambient thermal resistance for which maximum V_{FOM} and V_{ROM} ratings apply equals 3.5°C/watt.

MAXIMUM ALLOWABLE RATINGS AND CHARACTERISTICS

RMS Forward Current, On-state I_F ..... 110 Amperes
Average Forward Current, On-state $I_{F(AV)}$ ..... Depends on conduction angle (see chart)
Peak One Cycle Surge Forward Current (Non-repetitive), I_{FM} (surge) ..... 1000 Amperes
I^2t (for fusing) ..... 4000 Ampere² seconds (for times $\geq$ 1.5 milliseconds)
Operating Temperature T_J ..... −40°C to +125°C
Turn-off Time (T_J = +120°C) ..... t_{OFF} Typ. 15/Max. 20 μsec
dv/dt (T_C = +120°C) ..... U, F, A, G, B, H Typ. 30V/μsec
C, D, E, M Typ. 15V/μsec



MAXIMUM ALLOWABLE CASE TEMPERATURE



CURRENT LIMIT FOR STEEP WAVEFORM OPERATION

CONDENSED SPECIFICATIONS—FOR COMPLETE SPECIFICATIONS SEE 170.26

110A RMS SCR UP TO 300V

- Freedom from Thermal Fatigue
- Welded Seals
- High Junction Temperature

C60 (2N2023-29)

C61

Outline Drawing No. 11

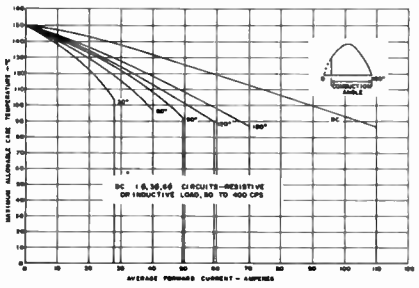
NOTE: The 2N2023-2029 has a guaranteed low temperature limit of —65°C; the C61 series is guaranteed to —40°C. In all other respects they are identical.

	2N2023 (C60U) C61U	2N2024 (C60F) C61F	2N2025 (C60A) C61A	2N2026 (C60G) C61G	2N2027 (C60B) C61B	2N2028 (C60H) C61H	2N2029 (C60C) C61C	
Transient Peak Reverse Voltage (Nonrecurrent <5 millisecond)*	35	75	150	225	300	350	400	volts
Repetitive Peak Reverse Voltage, V_{ROM}(rep)*	25	50	100	150	200	250	300	volts
Minimum Forward Breakover Voltage, $V_{(BR)FO}$	25	50	100	150	200	250	300	volts

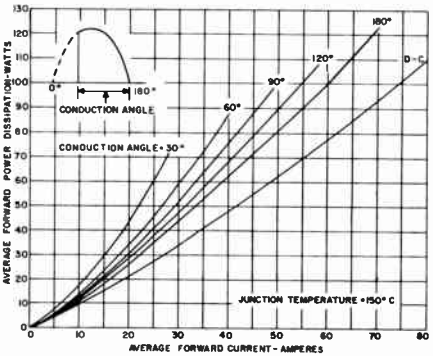
MAXIMUM ALLOWABLE RATINGS AND CHARACTERISTICS

RMS Forward Current, On-state I_F ..... 110 Amperes
Average Forward Current, On-state $I_{F(AV)}$ ..... Depends on conduction angle (see chart)
Peak One Cycle Surge Forward Current (Non-repetitive), I_{FM} (surge) ..... 1000 Amperes
I^2t (for fusing) ..... 4000 Ampere² seconds (for times ≧ 1.5 milliseconds)
Operating Temperature T_J ..... C60 —65°C to +150°C
C61 —40°C to +150°C
Turn-off Time (T_J = +150°C) ..... t_{off} Typ. 30 μsec
dv/dt ..... not specified
di/dt ..... not specified

*V_{ROM} ratings apply for zero or negative gate voltage. Maximum heatsink thermal resistance for which maximum V_{ROM} ratings apply equals 3.5°C/watt.



MAXIMUM ALLOWABLE STUD TEMPERATURE



FORWARD POWER DISSIPATION

CONDENSED SPECIFICATIONS—FOR COMPLETE SPECIFICATIONS SEE 170.23

C150

C150 Outline Drawing No. 11

C152

C152 Outline Drawing No. 10

110A RMS SCR UP TO 1300V

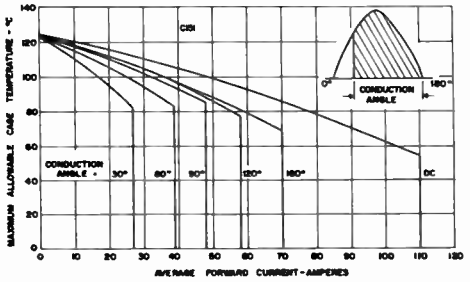
- Guaranteed dv/dt (200 V/μsec)
- Guaranteed Value of di/dt
- No PFV Limit

Type	Peak Forward Blocking Voltage, V_{FOM}* T_C = −40°C to +120°C	Repetitive Peak Reverse Voltage, $V_{ROM(rep)}$* T_C = −40°C to +120°C	Transient Peak Reverse Voltage, (Non-recurrent <5.0 Millisec.) V_{ROM} (non-rep) T_C = −40°C to +120°C
C150, C152E	500 volts	500 volts	600 volts
C150, C152M	600 volts	600 volts	720 volts
C150, C152S	700 volts	700 volts	850 volts
C150, C152N	800 volts	800 volts	950 volts
C150, C152T	900 volts	900 volts	1075 volts
C150, C152P	1000 volts	1000 volts	1200 volts
C150, C152PA	1100 volts	1100 volts	1325 volts
C150, C152PB	1200 volts	1200 volts	1450 volts
C150, C152PC	1300 volts	1300 volts	1550 volts

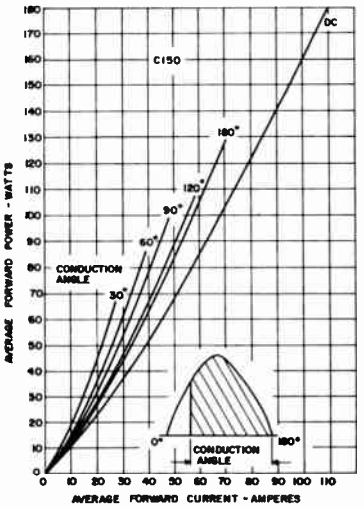
*Ratings apply for zero or negative gate voltage. Maximum heatsink thermal resistance for which maximum PRV ratings apply equal 1.1°C/watt.

MAXIMUM ALLOWABLE RATINGS AND CHARACTERISTICS

RMS Forward Current, On-state I_F ..... 110 Amperes
Average Forward Current, On-state $I_{F(AV)}$ ..... Depends on conduction angle (see chart)
Peak One Cycle Surge Forward Current (Non-repetitive), I_{FM} (surge) ..... 1500 Amperes
I^2t (for fusing) ..... 7000 Ampere^2 seconds (for times ≥ 1.5 milliseconds)
Operating Temperature T_J ..... −40°C to +125°C
Turn-off Time (T_J = +120°C) ..... t_{off} Typ. 100 μsec
di/dt ..... Switching from 1000V or Less, Max. 75A/μsec
Switching from 1300V to 1000V, Max. 50A/μsec
dv/dt (T_J = +120°C) ..... Min. 200V/μsec



MAXIMUM ALLOWABLE CASE TEMPERATURE



AVERAGE FORWARD POWER DISSIPATION

CONDENSED SPECIFICATIONS—FOR COMPLETE SPECIFICATIONS SEE 170.23

C151

C151 Outline Drawing No. 11

C153

C153 Outline Drawing No. 10

110A RMS SCR UP TO 1100V

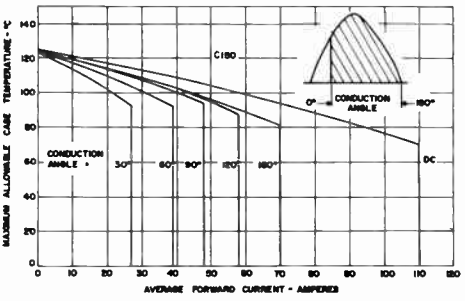
- Guaranteed dv/dt (200 V/μsec)
- Guaranteed Value of di/dt
- Guaranteed Value of t_{off}
- No PFV Limit

Type	Peak Forward Blocking Voltage, V_{FOM}* $T_C = -40°C$ to $+120°C$	Repetitive Peak Reverse Voltage, $V_{ROM(rep)}$* $T_C = -40°C$ to $+120°C$	Transient Peak Reverse Voltage, Non-recurrent <5.0 Millisec $V_{ROM(non\text{-}rep)}$ $T_C = -40°C$ to $+120°C$
C151, C153E	500 volts	500 volts	600 volts
C151, C153M	600 volts	600 volts	720 volts
C151, C153S	700 volts	700 volts	850 volts
C151, C153N	800 volts	800 volts	950 volts
C151, C153T	900 volts	900 volts	1075 volts
C151, C153P	1000 volts	1000 volts	1200 volts
C151, C153PA	1100 volts	1100 volts	1325 volts

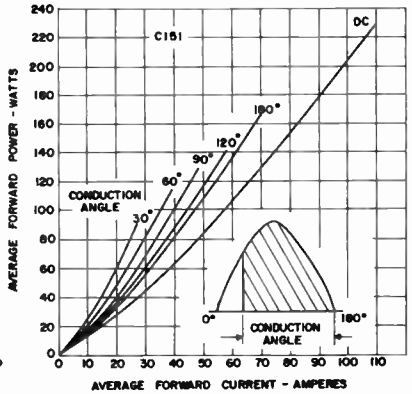
*Ratings apply for zero or negative gate voltage. Maximum heatsink thermal resistance for which maximum PRV ratings apply equal 1.1°C/watt.

MAXIMUM ALLOWABLE RATINGS AND CHARACTERISTICS

RMS Forward Current, On-state I_F ..... 110 Amperes
Average Forward Current, On-state $I_{F(AV)}$ ..... Depends on conduction angle (see chart)
Peak One Cycle Surge Forward Current (Non-repetitive), I_{FM} (surge) ..... 1000 Amperes
I^2t (for fusing) ..... 4000 Ampere^2 seconds (for times $\geqq$ 1.5 milliseconds)
Operating Temperature T_J ..... −40°C to +125°C
Turn-off Time (T_J = +120°C) ..... t_{off} Typ. 30/Max. 50 μsec
di/dt ..... Switching from 1000V or less, Max. 75A/μsec
Switching from 1100V to 1000V, Max. 50A/μsec
dv/dt (T_J = +120°C) ..... Min. 200V/μsec



MAXIMUM ALLOWABLE CASE TEMPERATURE



AVERAGE FORWARD POWER DISSIPATION

CONDENSED SPECIFICATIONS—FOR COMPLETE SPECIFICATIONS SEE 170.35

C154
C155
Outline Drawing No. 11

C156
C157
Outline Drawing No. 10

110A RMS SCR UP TO 500V

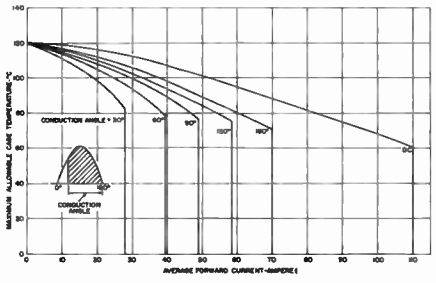
- Short Turn-off Times
- No PFV Limit
- Guaranteed dv/dt (200 V/μsec)
- Guaranteed di/dt (100 A/μsec)
- Choice of Flag or Flexible Cathode and Gate Terminals

Type	Peak Forward Blocking Voltage, V_{FOM}* $T_C = -40°C$ to $+125°C$	Repetitive Peak Reverse Voltage, $V_{ROM(rep)}$* $T_C = -40°C$ to $+125°C$	Transient Peak Reverse Voltage, (Non-recurrent <5 Millisec.) $V_{ROM(non\text{-}rep)}$ $T_C = -40°C$ to $+125°C$
C154, C155, C156, C157A	100 volts	100 volts	200 volts
C154, C155, C156, C157B	200 volts	200 volts	300 volts
C154, C155, C156, C157C	300 volts	300 volts	400 volts
C154, C155, C156, C157D	400 volts	400 volts	500 volts
C154, C155, C156, C157E	500 volts	500 volts	600 volts

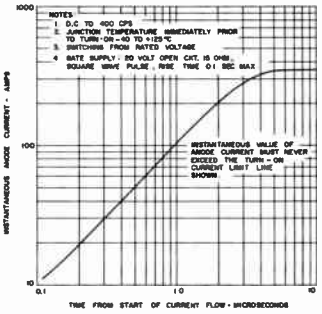
*Ratings apply for zero or negative gate voltage. Maximum heatsink thermal resistance for which maximum PRV ratings apply equal 1.1°C/watt.

MAXIMUM ALLOWABLE RATINGS AND CHARACTERISTICS

RMS Forward Current, On-state I_F ..... 110 Amperes
Average Forward Current, On-state $I_{F(AV)}$ ..... Depends on conduction angle (see chart)
Peak One Cycle Surge Forward Current (Non-repetitive), I_{FM} (surge) ..... 1000 Amperes
I^2t (for fusing) ..... 4000 Ampere^2 seconds (for times $\geq$ 1.5 milliseconds)
Operating Temperature T_J ..... $-40°C$ to $+125°C$
Turn-off Time ($T_C = +120°C$) ..... t_{off} C154, 156 Max. 10 μsec
C155, 157 Max. 20 μsec
dv/dt ($T_C = +120°C$) ..... C154, 156 Min. 200V/μsec
C155, 157 Min. 100V/μsec



MAXIMUM ALLOWABLE CASE TEMPERATURE



TURN-ON CURRENT LIMIT

CONDENSED SPECIFICATIONS—FOR COMPLETE SPECIFICATIONS SEE 170.54

110A AVG SCR UP TO 1300V

- Increased Current Capability When Double Sided Cooling is Used
- Reversibility Eliminates Need for Special Reverse Polarity Units
- Smaller Size and Lighter Weight
- Guaranteed dv/dt (200V/μsec)
- Guaranteed di/dt

C350

Outline Drawing No. 17

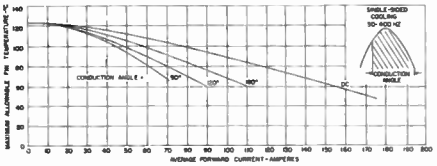
Type	Peak Forward Blocking Voltage, V_{FOM}* $T_C = -40°C$ to $+120°C$	Repetitive Peak Reverse Voltage, V_{ROM}(rep)* $T_C = -40°C$ to $+120°C$	Transient Peak Reverse Voltage, (Non-recurrent <5 Millisec.) V_{ROM}(non-rep) $T_C = -40°C$ to $+120°C$
C350E	500 volts	500 volts	600 volts
C350M	600 volts	600 volts	720 volts
C350S	700 volts	700 volts	850 volts
C350N	800 volts	800 volts	950 volts
C350T	900 volts	900 volts	1075 volts
C350P	1000 volts	1000 volts	1200 volts
C350PA	1100 volts	1100 volts	1325 volts
C350PB	1200 volts	1200 volts	1450 volts
C350PC	1300 volts	1300 volts	1550 volts

*Ratings apply for zero or negative gate voltage. Maximum heatsink thermal resistance for which maximum PRV ratings apply equal 1.1°C/watt.

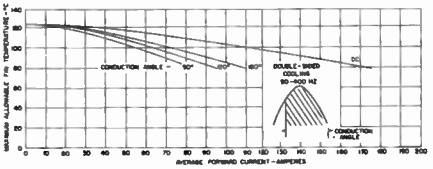
MAXIMUM ALLOWABLE RATINGS AND CHARACTERISTICS

Average Forward Current, On-state $I_{F(AV)}$ ..... Depends on conduction angle (see chart)
Peak One Cycle Surge Forward Current (Non-repetitive), I_{FM} (surge) ..... 1300 Amperes
I^2t (for fusing) ..... 7000 Ampere² seconds (for times $\geq$ 1.5 milliseconds)
Operating Temperature T_C ..... −40°C to +120°C
Turn-off Time† ..... t_{off} Typ. 100 μsec
dv/dt† ..... Min. 200V/μsec
di/dt ..... Switching from 1000V or less, Max. 75A/μsec
Switching from 1300V to 1000V, Max. 50A/μsec

†$T_C = +120°C$



MAXIMUM ALLOWABLE FIN TEMPERATURE SINGLE-SIDED COOLING



MAXIMUM ALLOWABLE FIN TEMPERATURE DOUBLE-SIDED COOLING

CONDENSED SPECIFICATIONS—FOR COMPLETE SPECIFICATIONS SEE 170.51

200A RMS SCR UP TO 1200V

- Guaranteed dv/dt of 200V/μsec
- Guaranteed di/dt
- Immunity to Forward Voltage Destruction

C178

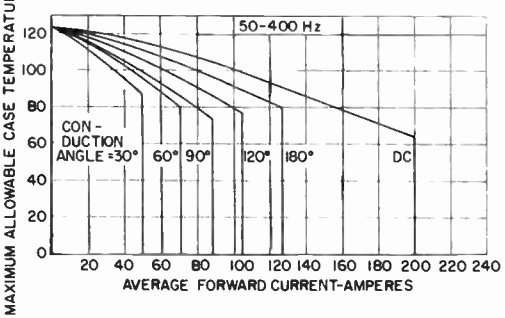
Outline Drawing No. 14

Type	Peak Forward Blocking Voltage, V_{FOM}* T_J = −40°C to +125°C	Repetitive Peak Reverse Voltage, $V_{ROM(rep)}$* T_J = −40°C to +125°C	Non-Repetitive Peak Reverse Voltage, <5.0 Millisec. $V_{ROM(non\text{-}rep)}$ T_J = −40°C to +125°C
C178A	100 volts	100 volts	200 volts
C178B	200 volts	200 volts	300 volts
C178C	300 volts	300 volts	400 volts
C178D	400 volts	400 volts	500 volts
C178E	500 volts	500 volts	600 volts
C178M	600 volts	600 volts	720 volts
C178S	700 volts	700 volts	840 volts
C178N	800 volts	800 volts	950 volts
C178T	900 volts	900 volts	1075 volts
C178P	1000 volts	1000 volts	1200 volts
C178PA	1100 volts	1100 volts	1325 volts
C178PB	1200 volts	1200 volts	1450 volts

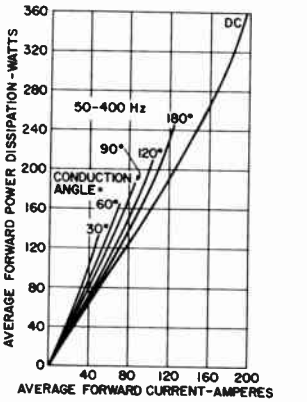
*Ratings apply for zero or negative gate voltage. Maximum heatsink thermal resistance for which maximum PRV ratings apply equal 1.5°C/watt.

MAXIMUM ALLOWABLE RATINGS AND CHARACTERISTICS

RMS Forward Current, On-state I_F ..... 200 Amperes
Average Forward Current, On-state $I_{F(AV)}$ ..... Depends on conduction angle (see chart)
Peak One Cycle Surge Forward Current (Non-repetitive), I_{FM} (surge) ..... 2500 Amperes
I^2t (for fusing) ..... 25,000 Ampere² seconds (for times ≧ 1.5 milliseconds)
Operating Temperature T_J ..... −40°C to +125°C
Turn-off Time (T_J = +125°C) ..... t_{off} Typ. 150 μsec
di/dt (T_J = + 25°C) ..... Switching from 500V or less, Max. 100A/μsec
Switching from 1000V to 500V, Max. 75A/μsec
Switching from 1200V to 1000V, Max. 50A/μsec
dv/dt (T_J = +125°C) ..... Min. 200V/μsec



MAXIMUM ALLOWABLE CASE TEMPERATURE



AVERAGE FORWARD POWER DISSIPATION

CONDENSED SPECIFICATIONS—FOR COMPLETE SPECIFICATIONS SEE 170.52

235A RMS SCR UP TO 1300V

- Range of Turn-off Times
- Guaranteed dv/dt (200V/μsec)
- Immunity to Forward Voltage Destruction

C180, C181, C185

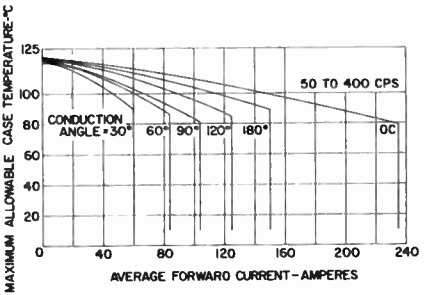
Outline Drawing No. 14

Type	Peak Forward Blocking Voltage, V_{FOM}* $T_C = -40°C$ to $+120°C$	Repetitive Peak Reverse Voltage, $V_{ROM(rep)}$* $T_C = -40°C$ to $+120°C$	Non-Repetitive Peak Reverse Voltage, <5.0 Millisec. $V_{ROM(Non\text{-}rep)}$ $T_C = -40°C$ to $+120°C$
C180, C181, C185A	100 volts	100 volts	200 volts
C180, C181, C185B	200 volts	200 volts	300 volts
C180, C181, C185C	300 volts	300 volts	400 volts
C180, C181, C185D	400 volts	400 volts	500 volts
C180, C181, C185E	500 volts	500 volts	600 volts
C180, C181M	600 volts	600 volts	720 volts
C180, C181S	700 volts	700 volts	840 volts
C180, C181N	800 volts	800 volts	950 volts
C180, C181T	900 volts	900 volts	1075 volts
C180, C181P	1000 volts	1000 volts	1200 volts
C180, C181PA	1100 volts	1100 volts	1325 volts
C180, C181PB	1200 volts	1200 volts	1450 volts
C180RC	1300 volts	1300 volts	1550 volts

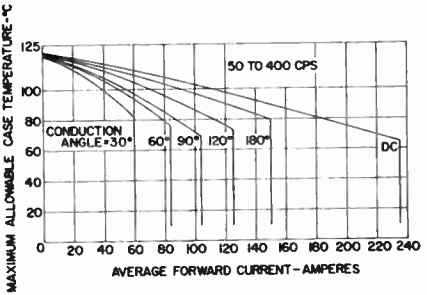
*Ratings apply for zero or negative gate voltage. Maximum heatsink thermal resistance for which maximum PRV ratings apply equal 1.5°/watt.

MAXIMUM ALLOWABLE RATINGS AND CHARACTERISTICS

RMS Forward Current, On-state I_F ..... 235 Amperes
Average Forward Current, On-state $I_{F(AV)}$ ..... Depends on conduction angle (see chart)
Peak One Cycle Surge Forward Current (Non-repetitive), I_{FM} (surge) ..... C180, 185 3500 Amperes
C181 2500 Amperes
I^2t (for fusing) ..... C180, 185 32,000 Ampere² seconds (for times $\geq$ 1.5 milliseconds)
C181 25,000 Ampere² seconds (for times $\geq$ 1.5 milliseconds)
Operating Temperature T_J ..... $-40°C$ to $+125°C$
dv/dt ($T_J = +120°C$) ..... Min. 200V/μsec
di/dt ..... Switching from 500V or less, Max. 100A/μsec
Switching from 1000V to 500V, Max. 75A/μsec
Switching from 1300V to 1000V, Max. 50A/μsec
Turn-Off Time ($T_C = 120°C$), t_{off} ..... C185 ..... 20 μsec. Max.
C180 ..... 30-125 μsec. Typ.
C181 ..... 25-75 μsec. Typ.



MAXIMUM ALLOWABLE CASE TEMPERATURE (C180, C185)



MAXIMUM ALLDWABLE CASE TEMPERATURE (C181)

CONDENSED SPECIFICATIONS—FOR COMPLETE SPECIFICATIONS SEE 170.58

235A RMS SCR UP TO 1700V

- Extremely High Voltage Capability
- Guaranteed di/dt (50A/μsec)

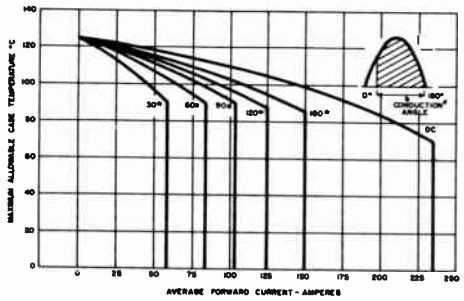
C280

Outline Drawing No. 15

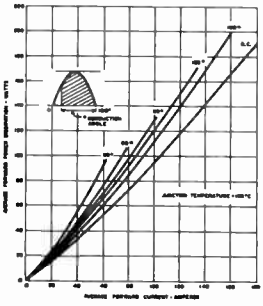
Type	Minimum Forward Breakover Voltage or Rep. Peak Rev. Voltage T_J = −40°C to +125°C	Transient Peak Reverse Voltage (Non-recurrent <5 millisec) T_J = 25°C to +125°C	Peak Forward Voltage (Non-Destructive) T_J = 25°C to +125°C
C280S	700 volts	800 volts	1000 volts
C280N	800 volts	900 volts	1000 volts
C280T	900 volts	1000 volts	1200 volts
C280P	1000 volts	1100 volts	1200 volts
C280PA	1100 volts	1200 volts	1300 volts
C280PB	1200 volts	1300 volts	1300 volts
C280PC	1300 volts	1400 volts	1400 volts
C280PD	1400 volts	1500 volts	1500 volts
C280PE	1500 volts	1600 volts	1600 volts
C280PM	1600 volts	1700 volts	1700 volts
C280PS	1700 volts	1800 volts	1800 volts

MAXIMUM ALLOWABLE RATINGS AND CHARACTERISTICS

RMS Forward Current, On-state I_F ..... 235 Amperes
Average Forward Current, On-state $I_{F(AV)}$ ..... Depends on conduction angle (see chart)
Peak One Cycle Surge Forward Current (Non-repetitive), I_{FM} (surge) ..... 3500 Amperes
I^2t (for fusing) ..... 32,000 Ampere^2 seconds (for times ≧ 1.5 milliseconds)
Operating Temperature T_J ..... −40°C to +125°C
Turn-off Time ..... Consult Factory
dv/dt (T_J = +125°C) ..... Typ. 100V/μsec
di/dt (T_J = +125°C) ..... Max. 50A/μsec



MAXIMUM ALLOWABLE CASE TEMPERATURE



AVERAGE FORWARD POWER DISSIPATION

CONDENSED SPECIFICATIONS—FOR COMPLETE SPECIFICATIONS SEE 170.56

230A AVG SCR UP TO 1300V

- Increased Current Capability When Double-Sided Cooling is Used
- Reversibility Eliminates Need for Special Reverse Polarity Units
- Smaller Size and Lighter Weight
- Guaranteed dv/dt (200V/μsec)
- Guaranteed di/dt

C380

Outline Drawing No. 17

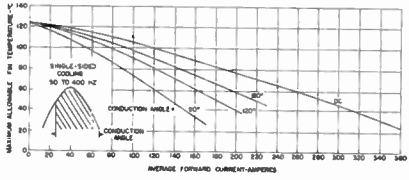
Type	Peak Forward Blocking Voltage, V_{FOM}* T_C = −40°C to +120°C	Repetitive Peak Reverse Voltage, $V_{ROM(rep)}$* T_C = −40°C to +120°C	Transient Peak Reverse Voltage (Non-recurrent <5 Millisec. $V_{ROM(non\text{-}rep)}$ T_C = −40°C to +120°C
C380A	100 volts	100 volts	200 volts
C380B	200 volts	200 volts	300 volts
C380C	300 volts	300 volts	400 volts
C380D	400 volts	400 volts	500 volts
C380E	500 volts	500 volts	600 volts
C380M	600 volts	600 volts	720 volts
C380S	700 volts	700 volts	840 volts
C380N	800 volts	800 volts	950 volts
C380T	900 volts	900 volts	1075 volts
C380P	1000 volts	1000 volts	1200 volts
C380PA	1100 volts	1100 volts	1325 volts
C380PB	1200 volts	1200 volts	1450 volts
C380PC	1300 volts	1300 volts	1550 volts

*Ratings apply for zero or negative gate voltage. Maximum heatsink thermal resistance for which maximum PRV ratings apply equal 1.5°C/watt.

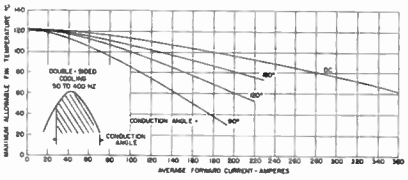
MAXIMUM ALLOWABLE RATINGS AND CHARACTERISTICS

Average Forward Current, On-state $I_{F(AV)}$ ..... Depends on conduction angle (see chart)
Peak One Cycle Surge Forward Current (Non-repetitive), I_{FM} (surge) ..... 3500 Amperes
I^2t (for fusing) ..... 32,000 Ampere^2 seconds (for times ≧ 1.5 milliseconds)
Operating Temperature T_C ..... −40°C to +120°C
Turn-off Time† ..... t_{off} A, B, C, D, E Typ. 30 μsec
M, S, N, T, P, Typ. 75 μsec
PA, PB, PC Typ. 125 μsec
dv/dt† ..... Min. 200V/μsec
di/dt ..... Switching from 500V or less, Max. 100A/μsec
Switching from 1000V to 500V, Max. 75A/μsec
Switching from 1300V to 1000V, Max. 50A/μsec

†T_C = +120°C



MAXIMUM ALLOWABLE FIN TEMPERATURE SINGLE-SIDED COOLING

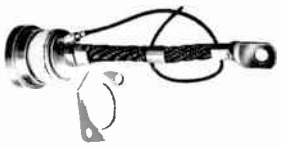


MAXIMUM ALLOWABLE FIN TEMPERATURE DOUBLE-SIDED COOLING

CONDENSED SPECIFICATIONS—FOR COMPLETE SPECIFICATIONS SEE 170.60

C290

Outline Drawing No. 15



C291

Outline Drawing No. 16

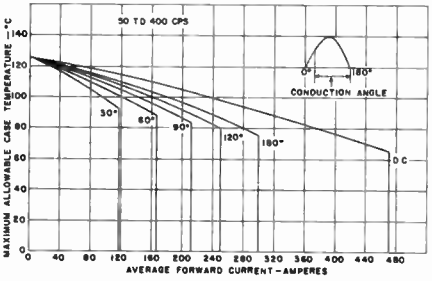
470A RMS SCR UP TO 1200V

- High Current
- Available in Two Configurations
- Guaranteed dv/dt (100V/μsec)
- Guaranteed di/dt (50A/μsec)

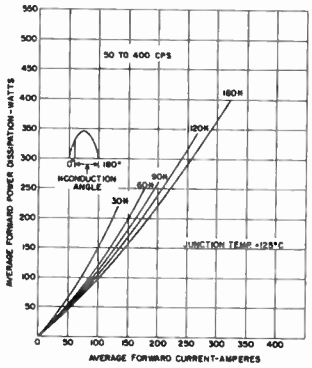
Type	Minimum Forward Blocking Voltage or Repetitive Peak Reverse Voltage T_J = —40°C to +125°C	Transient Peak Reverse Voltage, (Non-recurrent <5 msec. duration) T_J = +25°C to +125°C	Peak Forward Voltage (Non-destructive) T_J = +25°C to +125°C
C290F	50 volts	100 volts	400 volts
C290A	100 volts	200 volts	400 volts
C290B	200 volts	300 volts	400 volts
C290C	300 volts	400 volts	400 volts
C290D	400 volts	500 volts	500 volts
C290E, C291E	500 volts	600 volts	600 volts
C290M, C291M	600 volts	700 volts	700 volts
C290S, C291S	700 volts	800 volts	800 volts
C290N, C291N	800 volts	900 volts	900 volts
C290T, C291T	900 volts	1000 volts	1000 volts
C290P, C291P	1000 volts	1100 volts	1100 volts
C290PA, C291PA	1100 volts	1200 volts	1200 volts
C290PB, C291PB	1200 volts	1300 volts	1300 volts

MAXIMUM ALLOWABLE RATINGS AND CHARACTERISTICS

RMS Forward Current, On-state I_F ..... 470 Amperes
Average Forward Current, On-state $I_{F(AV)}$ ..... Depends on conduction angle (see chart)
Peak One Cycle Surge Forward Current (Non-repetitive), I_{FM} (surge) ..... 5500 Amperes
I^2t (for fusing) ..... 120,000 Ampere² seconds (for times ≧ 8.3 milliseconds)
Operating Temperature T_J ..... —40°C to +125°C
Turn-off Time ..... Consult Factory
dv/dt (T_J = +125°C) ..... Min. 100V/μsec
di/dt (T_J = +125°C) ..... Max. 50A/μsec



MAXIMUM ALLOWABLE CASE TEMPERATURE



AVERAGE FORWARD POWER DISSIPATION

CONDENSED SPECIFICATIONS—FOR COMPLETE SPECIFICATIONS SEE 170.61

The C500X1* water-cooled AC switch consists of two silicon controlled rectifiers inverse-parallel mounted between water-cooled heat exchangers.

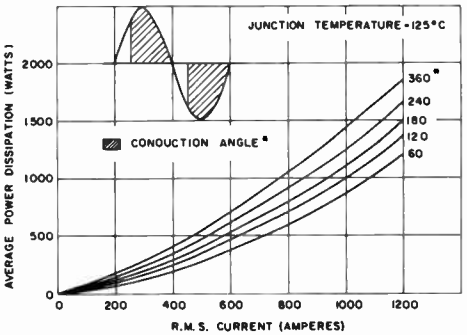
C500X1

Outline Drawing No. 13

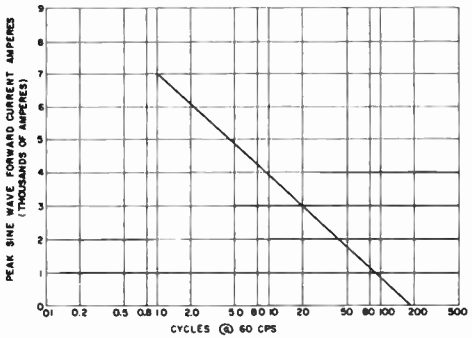
RATINGS

RMS Continuous Current	1200 amperes
Peak One-Cycle Surge Current	7000 amperes
Peak Ten-Cycle Surge Current	4000 amperes
Continuous Blocking Voltage	1800 volts
Maximum Average Power Dissipation (1200A RMS and 360° conduction angle)	1850 watts
Thermal Resistance (Junction to Water @ 1 gpm)	0.12°C/watt/cell
Water Flow Required for Max. Rating	1 gallon/minute at a Max. of 40°C
Weight	15 pounds

*Also available in the C500 series are AC and half-wave (Single SCR) air cooled switches.



AVERAGE FORWARD POWER DISSIPATION



PEAK SURGE FORWARD CURRENT AT RATED LOAD CURRENT

21.3.2 Triac

CONDENSED SPECIFICATIONS—FOR COMPLETE SPECIFICATIONS SEE 175.10,15

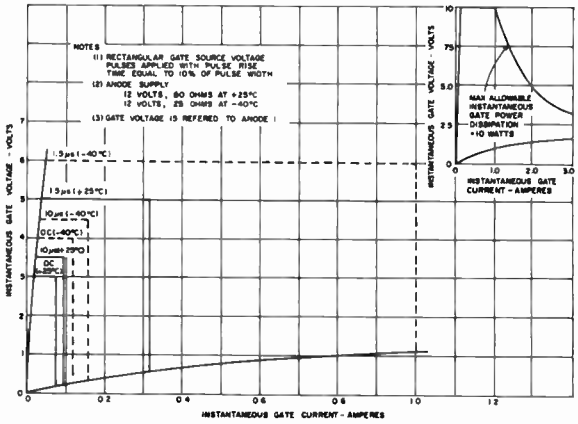
Outline Drawing No. 5

SC40 SC41
SC45 SC46

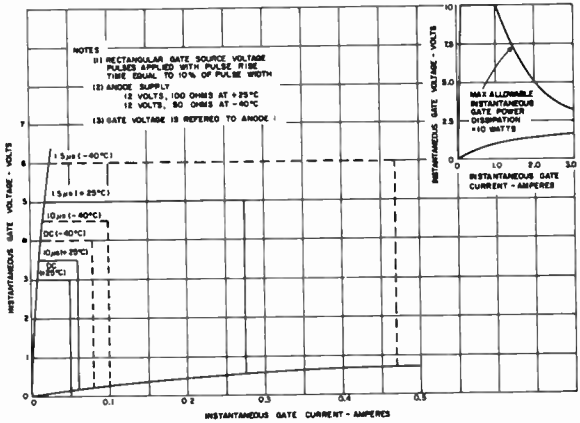
6A AND 10A RMS 200V AND 400V TRIAC (GATE CONTROLLED AC SWITCH)

- Comparable to Two Inverse Parallel SCR's
- One Gate Lead
- Ideal for Lamp Dimming and Temperature Controlling

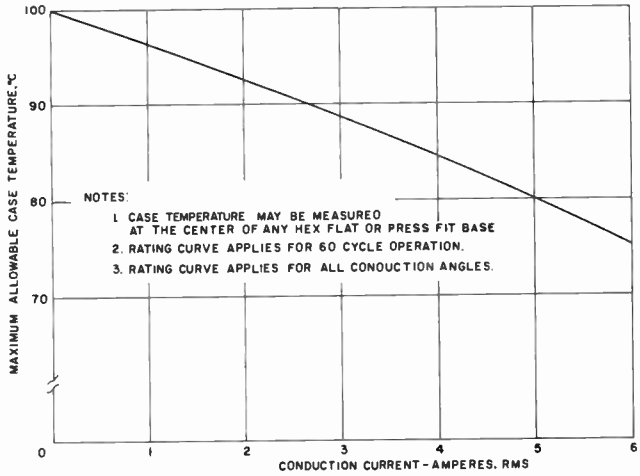
MAXIMUM ALLOWABLE RATINGS AND CHARACTERISTICS	SC40B, SC41B	SC40D, SC41D	SC45B, SC46B	SC45D, SC46D	
Minimum Breakover Voltage either direction; $V_{(BR)}$	±200	±400	±200	±400	volts
RMS Conduction Current Rating; T_{case} = 75°C (see Curves 3 and 4)	6	6	10	10	amperes
Peak One Cycle Surge, T_J = 100°C	50	50	80	80	amperes
Operating Junction Temperature T_J	−40°C to +100°C		−25°C to +100°C		
Peak Blocking Current either direction, T_J = 100°C	2	5	2	5	ma



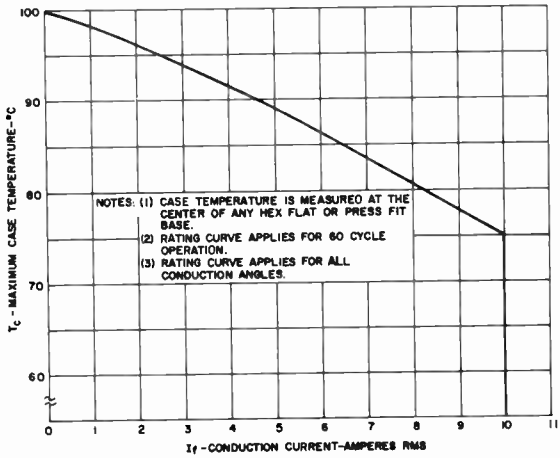
1. MAXIMUM PULSE AND DC GATE TRIGGER CHARACTERISTICS (ALL TYPES) (A_2+ Gate−)



2. MAXIMUM PULSE AND DC GATE TRIGGER CHARACTERISTICS (ALL TYPES) (A_2+ GATE+; A_2— GATE—)



3. MAXIMUM CONDUCTION CURRENT RATING AS A FUNCTION OF MAXIMUM CASE TEMPERATURE (SC40, SC41)



4. MAXIMUM CONDUCTION CURRENT RATING AS A FUNCTION OF MAXIMUM CASE TEMPERATURE (SC45, SC46)

21.3.3 Special Devices Condensed Specifications

CONDENSED SPECIFICATIONS—FOR COMPLETE SPECIFICATIONS SEE 60.62

UNIJUNCTION TRANSISTORS

2N2646 & 2N2647

Outline Drawing No. 18

The General Electric 2N2646 and 2N2647 Silicon Unijunction Transistors have an entirely new structure resulting in lower saturation voltage, peak-point current and valley current as well as a much higher base-one peak pulse voltage. In addition, these devices are much faster switches. The 2N2646 is intended for general purpose industrial applications where circuit economy is of primary importance, and is ideal for use in triggering circuits for Silicon Controlled Rectifiers and other applications where a guaranteed minimum pulse amplitude is required. The 2N2647 is intended for applications where a low emitter leakage current and a low peak point emitter current (trigger current) are required (i.e. long timing applications), and also for triggering high power SCR's and triacs. Consult your nearest Electronic Component Sales Office for GE's full line of unijunction transistors.

ABSOLUTE MAXIMUM RATINGS: (25°C)

Power Dissipation (Note 1)	300 mw
RMS Emitter Current	50 ma
Peak Emitter Current (Note 2)	2 amperes
Emitter Reverse Voltage	30 volts
Interbase Voltage	35 volts
Operating Temperature Range	−65°C to +125°C
Storage Temperature Range	−65°C to +150°C

ELECTRICAL CHARACTERISTICS: (25°C)

PARAMETER		2N2646			2N2647			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Intrinsic Standoff Ratio (V_{BB} = 10V) (Note 4)	η	0.56	0.65	0.75	0.68	0.75	0.82	
Interbase Resistance (V_{BB} = 3V, I_E = 0)	R_{BBO}	4.7	7	9.1	4.7	7	9.1	KΩ
Emitter Saturation Voltage (V_{BB} = 10V, I_E = 50 ma)	$V_{E(SAT)}$		2			2		volts
Modulated Interbase Current (V_{BB} = 10V, I_E = 50 ma)	$I_{B2(MOD)}$		12			12		ma
Emitter Reverse Current (V_{B2E} = 30V, I_{B1} = 0)	I_{EO}		0.05	12		0.01	0.2	μa
Peak Point Emitter Current (V_{BB} = 25V)	I_P		0.4	5		0.4	2	μa
Valley Point Current (V_{BB} = 20V, R_{B2} = 100Ω)	I_V	4	6		8	11	18	ma
Base-One Peak Pulse Voltage (Note 3)	V_{OB1}	3.0	6.5		6.0	7.5		volts

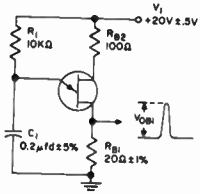


FIGURE 1

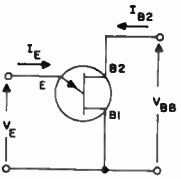


FIGURE 2
Unijunction Transistor Symbol with Nomenclature used for voltage and currents.

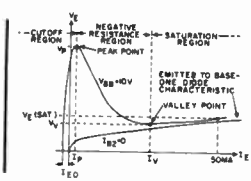


FIGURE 3
Static Emitter Characteristics curves showing important parameters and measurement points (exaggerated to show details).

NOTES:

1. Derate 3.0 MW/°C increase in ambient temperature. The total power dissipation (available power to Emitter and Base-Two) must be limited by the external circuitry.
2. Capacitor discharge—10 μfd or less, 30 volts or less.
3. The Base-One Peak Pulse Voltage is measured in Figure 1. This specification on the 2N2646 and 2N2647 is used to ensure a minimum pulse amplitude for applications in SCR triggering circuits and other types of pulse circuits.
4. The intrinsic standoff ratio, η, is essentially constant with temperature and interbase voltage. η is defined by the equation:
   $V_P = \eta V_{BB} + V_D$
   Where V_P = Peak Point Emitter Voltage
   V_{BB} = Interbase Voltage
   V_D = Junction Diode Drop (Approx. 0.5V)

SCR TRIGGER CIRCUIT DESIGN CURVES

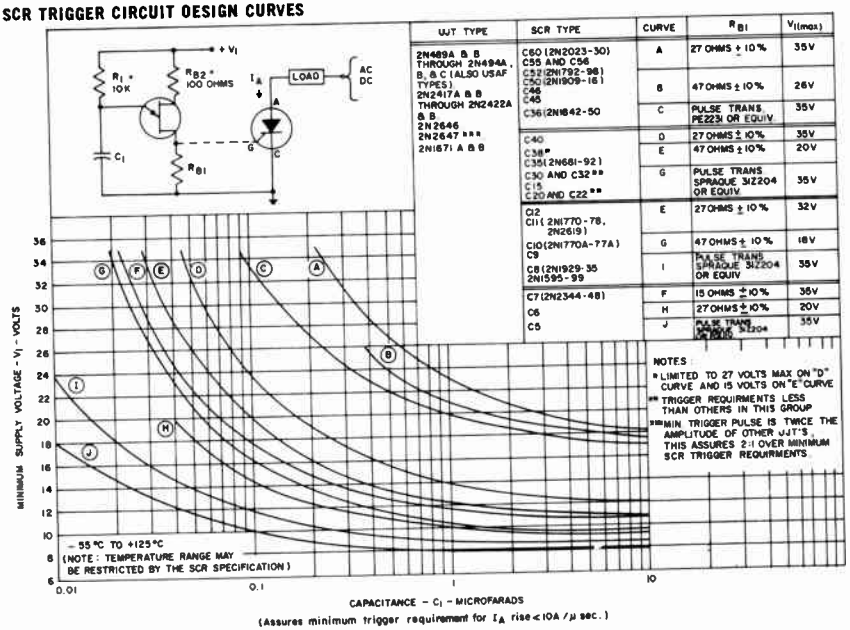


FIGURE 4—BOTH TYPES—LO AND MED. SCR's

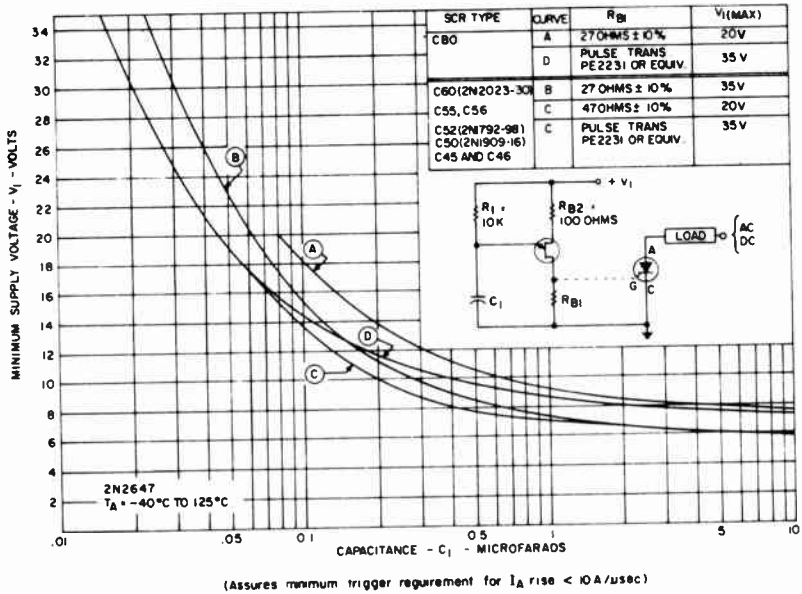


FIGURE 5—2N2647—HI CURRENT SCR's

CONDENSED SPECIFICATIONS—FOR COMPLETE SPECIFICATIONS SEE 55.41

175 MA RMS UP TO 40V LIGHT ACTIVATED SILICON CONTROLLED SWITCH

LASCS

Outline Drawing No. 21

Ideal for Such Applications as:

- Optical Logic Control
- Counting
- Sorting
- Meter Relays
- Precision Indexing
- Explosion Proof Isolated Switches
- Static Relays

ABSOLUTE MAXIMUM RATINGS AND CHARACTERISTICS: (25°C unless otherwise specified)

	Symbol	Min.	Max.	
Voltages				
Anode to Cathode forward and reverse			40	volts
Anode to Anode Gate			40	volts
Cathode to Cathode Gate			5	volts
Currents				
Anode (steady state)*			175	mA
Peak recurrent Anode (T_A = 100°C, 100 μsec 1% Duty Cycle)			.5	amps
Peak non recurrent Anode (10 μsec)			2.0	amps
Anode Gate (steady state)*			100	mA
Peak recurrent Anode Gate (T_A = 100°C, 100 μsec 1% Duty Cycle)			200	mA
Cathode Gate (steady state)			10	mA
Peak recurrent Cathode Gate (T_A = 100°C, 100 μsec 1% Duty Cycle)			100	mA
Dissipation				
Total power*			400	mW
Temperature				
Storage	T_{STG}	−65°C	+200	°C
Operating Junction	T_J	−55°C	+125	°C
CUTOFF CHARACTERISTICS (DARK)				
Forward Blocking Current				
(R_{GC} = 27 KΩ, V_{AC} = 40V)	I_B		1	μA
(R_{GC} = 27 KΩ, V_{AC} = 40V, T_A = 100°C)	I_B		20	μA
Reverse Blocking Current				
(R_{GC} = 27 KΩ, V_{AC} = 40V)	I_R		1	μA
(R_{GC} = 27 KΩ, V_{AC} = 40V, T_A = 100°C)	I_R		20	μA
Cathode Gate Reverse Cutoff Current (V_{GC} = 5V)	I_{GC}		20	μA
Anode Gate Reverse Cutoff Current (V_{GA} = 40V)	I_{GA}		1	μA
CONDUCTING CHARACTERISTICS				
Forward Voltage				
(I_A = 175 mA, R_{GC} = 27 KΩ)	V_F		2.0	volts
(I_A = 175 mA, R_{GC} = 27 KΩ, T_A = −55°C)	V_F		2.5	volts
Holding Current				
(R_{GC} = 27 KΩ)	I_H		2	mA
(R_{GC} = 27 KΩ, T_A = −55°C)	I_H		10	mA
TRIGGERING CHARACTERISTICS				
Effective Irradiance to Trigger**				
(V_{AC} = 40V, R_A = 800 Ω, R_{GC} = 27 KΩ)	H_{ET}	1.0	10	mW/cm²
(V_{AC} = 40V, R_A = 800 Ω, R_{GC} = 27 KΩ, T_A = −55°C)	H_{ET}		50	mW/cm²
(V_{AC} = 40V, R_A = 800 Ω, R_{GC} = 27 KΩ, T_A = 100°C)	H_{ET}	.3		mW/cm²
Cathode Gate Current to Trigger				
(R_{GC} = 1 megΩ, V_{AC} = 40V, R_A = 800 Ω)	I_{GTC}		10	μA
(R_{GC} = 1 megΩ, V_{AC} = 40V, R_A = 800 Ω, T_A = −55°C)	I_{GTC}		100	μA
Cathode Gate Voltage to Trigger				
(R_{GC} = 27 KΩ, V_{AC} = 40V, R_A = 800 Ω)	V_{GTC}	.4	.65	volts
(R_{GC} = 27 KΩ, V_{AC} = 40V, R_A = 800 Ω, T_A = −55°C)	V_{GTC}		1.0	volts
(R_{GC} = 27 KΩ, V_{AC} = 40V, R_A = 800 Ω, T_A = 100°C)	V_{GTC}	.2		volts
TRANSIENT CHARACTERISTICS				
Turn on time (Fig. 1)	t_{on}		15	μs
Recovery time (Fig. 2)	t_{rec}		25	μs

*Derate 3.2 mW/°C increase in ambient above 25°C.

**The effective irradiance (H_E) is the product of the spectral distribution of the light energy (Y_λ) and the spectral distribution of the device sensitivity (H_λ) integrated with respect to wavelength. ($H_E = \int H_\lambda Y_\lambda d\lambda$). Effective irradiance to trigger (H_{ET}) is the effective irradiance necessary to just trigger the device. See Application Note 200.34 for a discussion of these parameters.

CONDENSED SPECIFICATIONS—FOR COMPLETE SPECIFICATIONS SEE 175.30

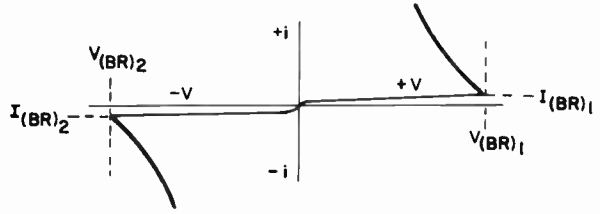
• DIODE AC SWITCH (DIAC)

ST2

Outline Drawing No. 20

The DIAC is a diffused silicon bi-directional trigger diode which may be used to trigger the GE TRIAC or Silicon Controlled Rectifiers. This device has a three-layer structure having negative resistance switching characteristics for both directions of applied voltage.

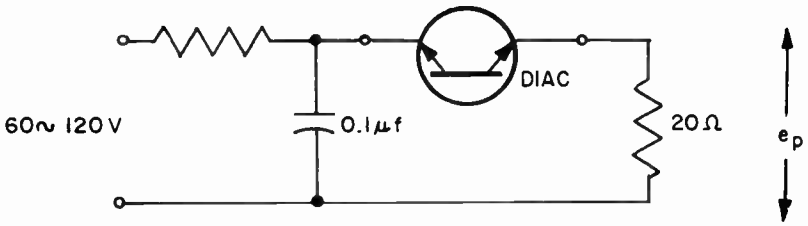
VOLT-AMPERE CHARACTERISTICS



RATINGS AT 50°C AMBIENT

Peak Current (10 μsec duration, 120 cycle repetition rate)	I_p	±2	Amperes Max.
Peak Output Voltage*	e_p	±3	Volts Min.

*CIRCUIT FOR PEAK OUTPUT VOLTAGE TEST



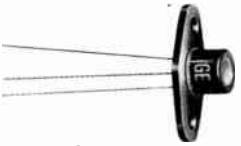
CHARACTERISTICS AT 25°C AMBIENT

Test	Symbols	Min.	Typ.	Max.	Units
Breakover Voltage	$V_{(BR)_1}$ and $V_{(BR)_2}$	28	32	36	volts
Breakover Voltage Temp. Coefficient		—	0.1	—	%/°C
Breakover Currents	$I_{(BR)_1}$ and $I_{(BR)_2}$	—	—	200	μ amp
Breakover Voltage Symmetry	$< V_{(BR)_1} = V_{(BR)_2} \pm 10\% V_{(BR)_2} >$				

It should be recognized that the General Electric ST2 is a developmental device and that Ratings and Characteristics listed above are typical of the device at the time this specification sheet was issued. The General Electric Company reserves the right to make any changes in specifications which in the Company's opinion are required to improve the device or make it more adaptable.

CONDENSED SPECIFICATIONS—FOR COMPLETE SPECIFICATIONS SEE 190.10

Outline Drawing No. 2



L8 **L811**
L9 **L911**

1.6A RMS UP TO 200V LIGHT ACTIVATED SCR

Ideal for Such Applications as:

- Optical Logic Control
- Counting
- Sorting
- Meter Relays
- Precision Indexing
- Explosion Proof Isolated Switches
- Static Relays

The L811 and L911 series are identical to the L8 and L9 respectively except that they are soldered to a diamond base heat sink.

Types[1]	Peak Forward Blocking[2] Voltage, V_{FXM} $T_J = -65°C$ to $+100°C$ $R_{GK} = 56{,}000$ Ohms Maximum	Working and Repetitive Peak Reverse Voltage, V_{ROM} (wkg) and V_{ROM} (rep) $T_J = -65°C$ to $+100°C$	Non-Repetitive Peak Reverse Voltage, V_{ROM} (non-rep) <5 Millisec. $T_J = -65°C$ to $+100°C$
L8U, L9U	25 volts	25 volts	40 volts
L8F, L9F	50 volts	50 volts	75 volts
L8A, L9A	100 volts	100 volts	150 volts
L8G, L9G	150 volts	150 volts	225 volts
L8B, L9B	200 volts	200 volts	300 volts

[1]The diamond base versions are L811U, L911U, L811F, etc.
[2]H_e<0.08 mw/cm² for L8 types and H_e<0.02 mw/cm² for L9 types.

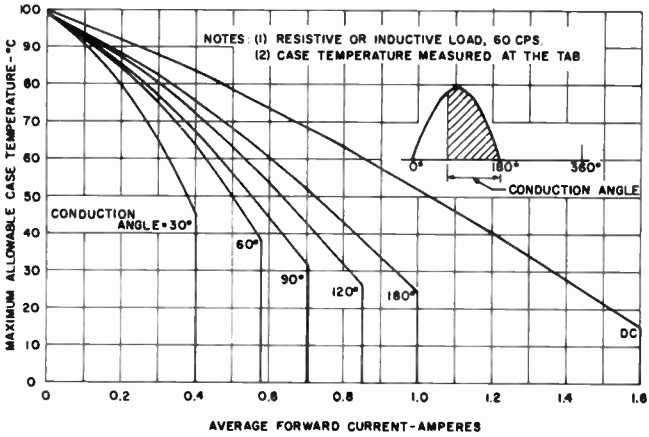
MAXIMUM ALLOWABLE RATINGS AND CHARACTERISTICS

RMS Forward Current, On-state I_F ..... 1.6 Amperes
Average Forward Current, On-state $I_{F(AV)}$ ..... Depends on conduction angle (see charts)
Peak One Cycle Surge Forward Current (Non-repetitive), I_{FM} (surge) ..... 15 Amperes
I^2t (for fusing) ..... 0.5 Ampere² seconds (for times ≧ 1.5 milliseconds)
Peak Reverse Gate Voltage, V_{GRM} ..... 6 Volts
Operating Temperature T_J ..... −65°C to +100°C
Forward and Reverse Blocking Current* ..... I_{FX} I_{RX} Typ. 40/Max. 100 μAdc
Holding Current‡ ..... I_{HX} Typ. 75/Max. 560 μAdc
Turn-off Time† ..... t_{off} Typ. 40 μsec

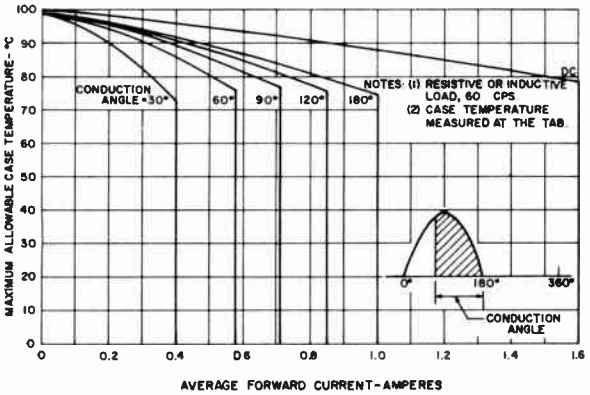
*$T_J = +100°C$, $R_{GK} = 56{,}000$ ohms
‡$T_J = +25°C$, $R_{GK} = 56{,}000$ ohms
†$T_J = 100°C$, $R_{GK} = 100$ ohms

			Min.	Typ.	Max.			
Effective Irradiance to Trigger	L8	H_{ET}	0.68	5.0	10.0	milliwatts/Cm²	$T_J = +25°C$	V_{FX} = 6 vdc, R_L = 100 ohms, R_{GK} = 56,000 ohms
	L9		0.68	2.0	4.2			
	L8		0.15	2.0	6.0		$T_J = +100°C$	
	L9		0.15	0.7	2.5			
	L8		0.9	15.0	50.0		$T_J = -65°C$	
	L9		0.9	4.0	20.0			
	L8		0.02	—	—		$T_J = +100°C$, R_{GK} = 56,000 ohms	
	L9		0.02	—	—		V_{FX} = Rated V_{FXM}, R_L = 500 ohms	

Light Actuated SCR, con't.



MAXIMUM ALLOWABLE CASE TEMPERATURE



MAXIMUM ALLOWABLE CASE TEMPERATURE (DIAMOND BASE)

CONDENSED SPECIFICATIONS—FOR COMPLETE SPECIFICATIONS SEE 65.26

D13P1

Outline Drawing No. 19

• SILICON UNILATERAL SWITCH (SUS)

The General Electric D13D1 is a diode thyristor with electrical characteristics that closely approximate those of an "ideal" four layer diode. The device uses a silicon monolithic integrated structure to achieve an 8 volt switching voltage, an on voltage of 1.75 volts at 200ma and temperature coefficient of switching voltage of less than 0.05%/°C. A gate lead is provided to give access to the circuit between the top of the zener and the base of the PNP.

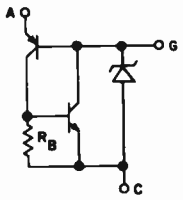
Silicon Unilateral Switches are specifically designed and characterized for use in monostable and bistable applications where stability of the switching voltage is required over wide temperature variations. They are ideally suited for telephone switching, SCR and triac triggering and for a variety of logic and memory applications.

Absolute Maximum Ratings and Characteristics: 25°C (unless otherwise specified)

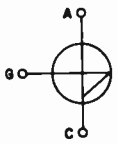
	Max.	
Peak Reverse Voltage	−30	volts
DC Forward Current*	200	ma
Peak Recurrent Forward Current (1% duty cycle, 10 μsec pulse width, T_A = 100°C)	1.0	amp
Peak Non-Recurrent Forward Current (10 μsec pulse width, T_A = 25°C)	5.0	amps
Operating Temperature T_J	−55°C to +150	°C
Forward Switching Voltage, V_S	10	volts
Forward Switching Current, I_S	500	μa
Holding Current, I_H	1.5	ma

*Derate linearly to zero at 150°C.

EQUIVALENT CIRCUIT



CIRCUIT SYMBOL



CONDENSED SPECIFICATIONS—FOR COMPLETE SPECIFICATIONS SEE 65.31

D13Q1

Outline Drawing No. 19

• SILICON BILATERAL SWITCH (SBS)

The General Electric D13E1 is a silicon planar multijunction device having a symmetrical negative resistance characteristic. The device uses a silicon monolithic structure to achieve a typical switching voltage of 8 volts and excellently matched characteristics in both directions. The temperature coefficient of switching voltage is less than .05%/°C. A gate lead is provided to give access to the zener and PNP base node.

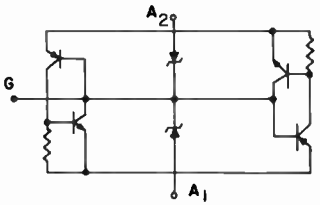
Silicon Bilateral Switches are specifically designed and characterized for applications where stability of switching voltage over a wide temperature range and well matched bilateral characteristics are an asset. They are ideally suited for half wave and full wave triggering in low voltage SCR and triac phase control circuits.

Absolute Maximum Ratings and Characteristics:* 25°C (unless otherwise specified)

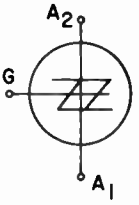
	Max.	
DC Forward Current	200	ma
Peak Recurrent Forward Current (1% duty cycle, 10 μsec pulse width, $T_A = 100°C$)	1.0	amp
Peak Non-Recurrent Forward Current (10 μsec pulse width, $T_A = 25°C$)	5.0	amps
Operating Temperatures	−55°C to +150	°C
Switching Voltage, V_S	10	volts
Switching Current, I_S	500	μA
Holding Current, I_H	1.5	mA

*This device is a symmetrical negative resistance diode. All electrical limits shown apply in either direction of current flow.

EQUIVALENT CIRCUIT



CIRCUIT SYMBOL



21.3.4 Rectifier Diodes

CONDENSED SPECIFICATIONS—COMPLETE SPECIFICATION NUMBERS LISTED IN TABLES

Silicon Subminiature Glass Rectifier Diodes

Up to 600 ma
Up to 600 volts

- Designed for Maximum Thermal Conductance
- Rugged Design to Meet Military Requirements
- Insulated Housing

JEDEC or GE Type Number	$V_{RM(rep)}$ and $V_{RM(wkg)}$ Volts	V_{RM} (non-rep)	Max. $I_{F(AV)}$		Max. Rev. Current I_{RM}	Max. Oper. Temp. T_A in °C	Out-line No.	Comp. Spec. No.
			T_A25°C	150°C	$T_A = 100°C$			
1N645	225	275	400 ma	150 ma	15 μa	175	22	125.5
1N646	300	360	400 ma	150 ma	15 μa	175	22	125.5
1N647	400	480	400 ma	150 ma	20 μa	175	22	125.5
1N648	500	600	400 ma	150 ma	20 μa	175	22	125.5
1N649	600	720	400 ma	150 ma	25 μa	175	22	125.5
Meets MIL-E-1/1143 and 19500/240A Specifications								
					$T_A = 150°C$			
1N676	100	120	200 ma	75 ma	.2 ma	175	22	125.15
1N677	100	120	400 ma	150 ma	.2 ma	175	22	125.20
1N678	200	240	200 ma	75 ma	.2 ma	175	22	125.15
1N679	200	240	400 ma	150 ma	.2 ma	175	22	125.20
1N681	300	360	200 ma	75 ma	.2 ma	175	22	125.15
1N682	300	360	400 ma	150 ma	.2 ma	175	22	125.20
1N683	400	480	200 ma	75 ma	.2 ma	175	22	125.15
1N684	400	480	400 ma	150 ma	.2 ma	175	22	125.20
1N685	500	600	200 ma	75 ma	.2 ma	175	22	125.15
1N686	500	600	400 ma	150 ma	.2 ma	175	22	125.20
1N687	600	720	200 ma	75 ma	.2 ma	175	22	125.15
1N689	600	720	400 ma	150 ma	.2 ma	175	22	125.20
					$T_A = 175°C$			
1N3544	100	120	600 ma	250 ma	75 μa	200	22	125.10
1N3545	200	240	600 ma	250 ma	75 μa	200	22	125.10
1N3546	300	360	600 ma	250 ma	75 μa	200	22	125.10
1N3547	400	480	600 ma	250 ma	75 μa	200	22	125.10
1N3548	500	600	600 ma	250 ma	75 μa	200	22	125.10
1N3549	600	720	600 ma	250 ma	75 μa	200	22	125.10
Low leakage at high temperature								

Germanium Low Current Rectifier Diodes

Up to 1200 ma
Up to 400 volts

- Extremely Low Forward Resistance, High Back Resistance
- Industry Standard for High Reliability Units

JEDEC or GE Type Number	$V_{RM(rep)}$ and $V_{RM(wkg)}$ Volts	Max. $I_{F(AV)}$ @ T_A	I_{FM} (Surge)	Max. Rev. Current $I_{R(AV)}$ @ T_A	Max. Full Load Voltage Drop	Max. Oper. T_A	Out-line No.	Comp. Spec. No.
		@ 55°C						
1N93	300	75 ma	25A	.6 ma	.18V	95°C	23	120.5
USN 1N93	300	75 ma	25A	.6 ma	.18V	95°C	23	120.5
1N315	300	75 ma	25A	Min. Fwd./Rev. Ratio 700 @ 55°C		85°C	23	120.10
USAF 1N315	300	75 ma	25A	Min. Fwd./Rev. Ratio 700 @ 55°C .3 ma @ 150 VDC		85°C	23	120.10
1N368	200	100 ma	25A		.48V	55°C	23	120.10
1N92	200	100 ma	25A	.95 ma	.19V	95°C	23	120.5
1N91	100	150 ma	25A	1.35 ma	.22V	95°C	23	120.5
1N153	300	750 ma	25A			95°C	24	120.20
1N158	400	1000 ma	25A			95°C	25	120.20
1N152	200	1000 ma	25A			95°C	24	120.20
1N151	100	1200 ma	25A			95°C	24	120.20
			Very Low Forward Voltage Drop					

Silicon Low Current Top Hat Rectifier Diodes

Up to 750 ma
Up to 1000 volts

These low current top hat alloy junction silicon rectifiers are designed for maximum forward conductance at high operating temperatures. A prime feature of these devices is that high current loads are carried without the use of any external heatsink whatsoever. The reverse current at maximum junction temperature is maintained at an extremely low level, making the devices ideal for magnetic amplifiers and other low leakage applications.

JEDEC or GE Type Number	$V_{RM(rep)}$ and $V_{RM(wkg)}$ Volts	Max. $I_{F(AV)}$ @ T_A	I_{FM} (Surge)	Max. Rev. Current $I_{R(AV)}$ @ T_A	Max. Full Load Voltage Drop @ T_A	Max. Oper. T_A	Out-line No.	Comp. Spec. No.
		@ 50°C		@ 25°C	@ 25°C			
1N440	100	300 ma	15A	.3 μa	1.5V peak	150°C	23	130.16
1N441	200	300 ma	15A	.75 μa	1.5V	150°C	23	130.16
1N442	300	300 ma	15A	1.0 μa	1.5V	150°C	23	130.16
1N443	400	300 ma	15A	1.5 μa	1.5V	150°C	23	130.16
1N444	500	300 ma	15A	1.75 μa	1.5V	150°C	23	130.16
1N445	600	300 ma	15A	2.0 μa	1.5V	150°C	23	130.16
1N440B	100	750 ma	15A	0.3 μa	1.5V	165°C	23	130.16
1N441B	200	750 ma	15A	0.75 μa	1.5V	165°C	23	130.16
1N442B	300	750 ma	15A	1.0 μa	1.5V	165°C	23	130.16
1N443B	400	750 ma	15A	1.5 μa	1.5V	165°C	23	130.16
1N444B	500	650 ma	15A	1.75 μa	1.5V	150°C	23	130.16
1N445B	600	650 ma	15A	2.0 μa	1.5V	150°C	23	130.16
		Low Leakage—Transient Voltage Ratings Up to 800V						

Silicon Low Current Top Hat Rectifier Diodes, Cont.

JEDEC or GE Type Number	$V_{RM(rep)}$ and $V_{RM(wkg)}$ Volts	Max. $I_{F(AV)}$ @ T_A	I_{FM} (Surge)	Max. Rev. Current $I_{R(AV)}$ @ T_A	Max. Full Load Voltage Drop @ T_A	Max. Oper. T_A	Out-line No.	Comp. Spec. No.
		@ 25°C			@ 200 ma			
1N599	50	600 ma	10A	1.0 μa	1.5V peak	150°C	23	130.35
1N599A	50	600 ma	10A	1.0 μa	1.5V	150°C	23	130.35
1N600	100	600 ma	10A	1.0 μa	1.5V	150°C	23	130.35
1N600A	100	600 ma	10A	1.0 μa	1.5V	150°C	23	130.35
1N601	150	600 ma	10A	1.0 μa	1.5V	150°C	23	130.35
1N601A	150	600 ma	10A	1.0 μa	1.5V	150°C	23	130.35
1N602	200	600 ma	10A	1.0 μa	1.5V	150°C	23	130.35
1N602A	200	600 ma	10A	1.0 μa	1.5V	150°C	23	130.35
1N603	300	600 ma	10A	1.0 μa	1.5V	150°C	23	130.35
1N603A	300	600 ma	10A	1.0 μa	1.5V	150°C	23	130.35
1N604	400	600 ma	10A	1.5 μa	1.5V	150°C	23	130.35
1N604A	400	600 ma	10A	1.5 μa	1.5V	150°C	23	130.35
1N605	500	600 ma	10A	2.0 μa	1.5V	150°C	23	130.35
1N605A	500	600 ma	10A	2.0 μa	1.5V	150°C	23	130.35
1N606	600	600 ma	10A	2.5 μa	1.5V	150°C	23	130.35
1N606A	600	600 ma	10A	2.5 μa	1.5V	150°C	23	130.35
		@ 30°C		@ 150°C	@ 150°C			
1N560	800	600 ma	15A	.3 ma	0.5V	150°C	23	130.10
1N561	1000	600 ma	15A	.3 ma	0.5V	150°C	23	130.10
		Transient PRV Ratings Up to 1200V						
		@ 50°C		@ 100°C	@ 100°C			
1N1692	100	600 ma	20A	.5 ma	0.6V	115°C	23	130.30
1N1693	200	600 ma	20A	.5 ma	0.6V	115°C	23	130.30
1N1694	300	600 ma	20A	.5 ma	0.6V	115°C	23	130.30
1N1695	400	600 ma	20A	.5 ma	0.6V	115°C	23	130.30
1N1696	500	600 ma	20A	.5 ma	0.6V	115°C	23	130.30
1N1697	600	600 ma	20A	.5 ma	0.6V	115°C	23	130.30
		Lowest Price Series, Lower Temperature and Current than 1N536-47 Series						
		@ 50°C		@ 150°C				
1N1100	100	750 ma	15A	.3 ma	1.5V peak	165°C	23	130.32
1N1101	200	750 ma	15A	.3 ma	1.5V	165°C	23	130.32
1N1102	300	750 ma	15A	.3 ma	1.5V	165°C	23	130.32
1N1103	400	750 ma	15A	.3 ma	1.5V	165°C	23	130.32
		Very Low Leakage. Ideal for Magnetic-amplifier Applications.						
		@ 25°C		@ 125°C	@ 125°C			
1N1487	100	750 ma	15A	.4 ma	.55V	140°C	23	130.22
1N1488	200	750 ma	15A	.3 ma	.55V	140°C	23	130.22
1N1489	300	750 ma	15A	.3 ma	.55V	140°C	23	130.22
1N1490	400	750 ma	15A	.3 ma	.55V	140°C	23	130.22
1N1491	500	750 ma	15A	.3 ma	.55V	125°C	23	130.22
1N1492	600	750 ma	15A	.3 ma	.55V	120°C	23	130.22
		Similar to 1N536-47 Series. Intermediate Temperature Operation.						
		@ 50°C		@ 150°C	@ 150°C			
1N536	50	750 ma	15A	.4 ma	.5V	165°C	23	130.10
1N537	100	750 ma	15A	.4 ma	.5V	165°C	23	130.10
1N538*	200	750 ma	15A	.3 ma	.5V	165°C	23	130.10
1N539	300	750 ma	15A	.3 ma	.5V	165°C	23	130.10
1N540*	400	750 ma	15A	.3 ma	.5V	165°C	23	130.10
1N1095	500	750 ma	15A	.3 ma	.5V	150°C	23	130.10
1N1096	600	750 ma	15A	.3 ma	.5V	150°C	23	130.10
1N547*	600	750 ma	15A	.3 ma	.5V	165°C	23	130.10
		A Popular Line. Transient Voltage Ratings Up to 800V.						
*Military Approved Units Also Available.								
		@ 85°C			@ 150°C			
A10A	100	.9A	45A	.4 ma	.5V	165°C	23	130.41
A10B	200	.9A	45A	.4 ma	.5V	165°C	23	130.41
A10C	300	.9A	45A	.4 ma	.5V	165°C	23	130.41
A10D	400	.9A	45A	.4 ma	.5V	165°C	23	130.41
A10E	500	.9A	45A	.4 ma	.5V	165°C	23	130.41
A10M	600	.9A	45A	.4 ma	.5V	165°C	23	130.41
A10N	800	.9A	45A	.4 ma	.5V	150°C	23	130.41
A10P	1000	.9A	45A	.4 ma	.5V	150°C	23	130.41
		High Surge Ratings in Dimmer Circuits and Television and Radio Voltage Doublers.						

Silicon Low Current Rectifier Diodes

Stud Mounted
Up to 1.5 amps
Up to 1000 volts

JEDEC or GE Type Number	$V_{RM(rep)}$ and $V_{RM(wkg)}$ Volts	Max. $I_{F(AV)}$ @ T_A	I_{FM} (Surge)	Max. Rev. Current $I_{R(AV)}$ @ T_A	Max. Full Load Voltage Drop	Max. Oper. T_A	Outline No.	Comp. Spec. No.
		@ 150°C Case		@ 150°C				
1N340	100	200 ma	10A	1 ma	2V @ 400 ma	170°C	27	130.80
1N349	100	200 ma	10A	1 ma	2V @ 400 ma	170°C	27	130.80
1N337	200	200 ma	10A	1 ma	2V @ 400 ma	170°C	27	130.80
1N346	200	200 ma	10A	5 ma	2V @ 400 ma	170°C	27	130.80
1N335	300	200 ma	10A	2 ma	2V @ 400 ma	170°C	27	130.80
1N344	300	200 ma	10A	5 ma	2V @ 400 ma	170°C	27	130.80
1N333	400	200 ma	10A	2 ma	2V @ 400 ma	170°C	27	130.80
1N342	400	200 ma	10A	5 ma	2V @ 400 ma	170°C	27	130.80
1N339	100	400 ma	15A	1 ma	2V @ 800 ma	170°C	27	130.80
1N348	100	400 ma	15A	5 ma	2V @ 800 ma	170°C	27	130.80
1N336	200	400 ma	15A	1 ma	2V @ 800 ma	170°C	27	130.80
1N345	200	400 ma	15A	5 ma	2V @ 800 ma	170°C	27	130.80
1N334	300	400 ma	15A	2 ma	2V @ 800 ma	170°C	27	130.80
1N343	300	400 ma	15A	5 ma	2V @ 800 ma	170°C	27	130.80
1N332	400	400 ma	15A	2 ma	2V @ 800 ma	170°C	27	130.80
1N341	400	400 ma	15A	5 ma	2V @ 800 ma	170°C	27	130.80
				Popular Series.				
		@ 100°C Case						
1N562	800	400 ma	15A	3 ma	.65V @ 150°C	150°C	27	130.62
1N563	1000	400 ma	15A	3 ma	.65V @ 150°C	150°C	27	130.62

JEDEC or GE Type Number	$V_{RM(rep)}$ and $V_{RM(wkg)}$ Volts	Max. $I_{F(AV)}$ @ T_A	I_{FM} (Surge)	Max. Rev. Current $I_{R(AV)}$	Max. Full Load Voltage Drop	Max. Oper. T_A	Outline No.	Comp. Spec. No.
		@ 100°C Amb.		@ 25°C	@ T_c = 25°C			
1N550	100	500 ma	4A, 3 ms	.5 μa	1.5V	150°C	27	130.70
1N551	200	500 ma	4A, 3 ms	1.0 μa	1.5V	150°C	27	130.70
1N552	300	500 ma	4A, 3 ms	1.5 μa	1.5V	150°C	27	130.70
1N553	400	500 ma	4A, 3 ms	2.5 μa	1.5V	150°C	27	130.70
1N554	500	500 ma	4A, 3 ms	3.5 μa	1.5V	150°C	27	130.70
1N555	600	500 ma	4A, 3 ms	5.0 μa	1.5V	150°C	27	130.70
			Very low leakage for magnetic amplifier applications.					
		@ 135°C Case		@ 135°C				
1N253*	95	1000 ma	15A	.1 ma	1.2V @ 1A	170°C	27	130.5
1N254*	190	800 ma	15A	.1 ma	1.2V @ 1A	170°C	27	130.5
1N255*	380	800 ma	15A	.15 ma	1.2V @ 1A	170°C	27	130.5
1N256*	570	600 ma	15A	.25 ma	1.2V @ 1A	155°C	27	130.5
*Military Approved units also available—Mil-S-19500/194A.								
		@ 100°C Amb.		@ 25°C	@ 25°C			
1N607	50	1A	2A, .1 sec	.025 ma	1.5V @ 200 ma	150°C	27	130.57
1N607A	50	1A	2A, .1 sec	.001 ma	1.5V @ 200 ma	150°C	27	130.57
1N608	100	1A	2A, .1 sec	.025 ma	1.5V @ 200 ma	150°C	27	130.57
1N608A	100	1A	2A, .1 sec	.001 ma	1.5V @ 200 ma	150°C	27	130.57
1N609	150	1A	2A. .1 sec	.025 ma	1.5V @ 200 ma	150°C	27	130.57
1N609A	150	1A	2A, .1 sec	.001 ma	1.5V @ 200 ma	150°C	27	130.57
1N610	200	1A	2A, .1 sec	.025 ma	1.5V @ 200 ma	150°C	27	130.57
1N610A	200	1A	2A, .1 sec	.001 ma	1.5V @ 200 ma	150°C	27	130.57
1N611	300	1A	2A, .1 sec	.025 ma	1.5V @ 200 ma	150°C	27	130.57
1N611A	300	1A	2A, .1 sec	.001 ma	1.5V @ 200 ma	150°C	27	130.57
1N612	400	1A	2A, .1 sec	.025 ma	1.5V @ 200 ma	150°C	27	130.57
1N612A	400	1A	2A, .1 sec	.0015 ma	1.5V @ 200 ma	150°C	27	130.57
1N613	500	1A	2A, .1 sec	.025 ma	1.5V @ 200 ma	150°C	27	130.57
1N613A	500	1A	2A, .1 sec	.002 ma	1.5V @ 200 ma	150°C	27	130.57
1N614	600	1A	2A, .1 sec	.025 ma	1.5V @ 200 ma	150°C	27	130.57
1N614A	600	1A	2A, .1 sec	.0025 ma	1.5V @ 200 ma	150°C	27	130.57
		@ 85°C Case		@ 150°C				
1N1115	100	1.5A	15A	.4 ma	.65V @ 150°C	170°C	27	130.60
1N1116	200	1.5A	15A	.3 ma	.65V @ 150°C	170°C	27	130.60
1N1117	300	1.5A	15A	.3 ma	.65V @ 150°C	170°C	27	130.60
1N1118	400	1.5A	15A	.3 ma	.65V @ 150°C	170°C	27	130.60
1N1119	500	1.3A	15A	.3 ma	.65V @ 150°C	155°C	27	130.60
1N1120	600	1.3A	15A	.3 ma	.65V @ 150°C	155°C	27	130.60
				A popular line				

Silicon Low Current Flangeless Rectifier Diodes

Up to 1 Amp
Up to 800 volts

The most desirable features of the top hat, such as long life, reliability and unit stability have been incorporated into this smaller package. These devices feature:

- High Surge Capability
- Thermal Fatigue Free Operation
- Transient Reverse Voltage Ratings
- Hermetically Sealed
- Small, Easy to Mount Package
- Strong Welded Tube Seal

JEDEC or GE Type Number	$V_{RM(rep)}$ and $V_{RM(wkg)}$ Volts	Max. $I_{F(AV)}$ @ T_A	I_{FM} (Surge)	Max. Rev. Current $I_{R(AV)}$ @ T_A	Max. Full Load Voltage Drop @ T_A	Max. Oper. T_A	Outline No.	Comp. Spec. No.
		@ 50°C		@ 150°C	@ 150°C			
1N2610	100	750 ma	30A	.3 ma	.5V	175°C	26	130.40
1N2611	200	750 ma	30A	.3 ma	.5V	175°C	26	130.40
1N2612	300	750 ma	30A	.3 ma	.5V	175°C	26	130.40
1N2613	400	750 ma	30A	.3 ma	.5V	175°C	26	130.40
1N2614	500	750 ma	30A	.3 ma	.5V	175°C	26	130.40
1N2615	600	750 ma	30A	.3 ma	.5V	175°C	26	130.40
		@ 75°C		@ 25°C	@ 25°C			
1N3639	200	750 ma	40A	10 μa	1.2V	100°C	26	130.44
1N3640	400	750 ma	40A	10 μa	1.2V	100°C	26	130.44
1N3641	600	750 ma	40A	10 μa	1.2V	100°C	26	130.44
1N3642	800	500 ma	40A	10 μa	1.2V	100°C	26	130.44
		@ 100°C		@ 150°C				
1N3189	200	1A	30A	.5 ma	1.0V	175°C	26	130.46
1N3190	400	1A	30A	.5 ma	1.0V	175°C	26	130.46
1N3191	600	1A	30A	.5 ma	1.0V	175°C	26	130.46

A new line of silicon low current diffused rectifiers in the flangeless package designed to meet the stringent requirements of Mil-S-19500.

Passivated Silicon Diffused Rectifier Diodes

1 Amp
Up to 600 volts

This is a small, insulated glass package featuring a passivated junction to enhance a high degree of reliability. Other features include:

- All Diffused Structure
- High Surge Capabilities
- High Output Rating
- Hermetic Seal
- Small Easy-to-Mount Package

JEDEC or GE Type Number	PRV	$I_{F(AV)}$ T_A = 50°C	Max. Peak 1 Cycle Surge	Max. Rev. Current $I_{R(AV)}$ T_J = 25°C	Oper. Temp.	Outline No.	Comp. Spec. No.
A13F	50	1.0A	30A	10 μA	175°C	30	130.50
A13A	100	1.0A	30A	10 μA	175°C	30	130.50
A13B	200	1.0A	30A	10 μA	175°C	30	130.50
A13C	300	1.0A	30A	10 μA	175°C	30	130.50
A13D	400	1.0A	30A	10 μA	175°C	30	130.50
A13E	500	1.0A	30A	10 μA	175°C	30	130.50
A13M	600	1.0A	30A	10 μA	175°C	30	130.50

Silicon Medium Current Rectifier Diodes

Up to 35 amperes
Up to 1000 volts

- High Junction Temperatures
- Hard-Solder, Thermal Fatigue Free
- Solid One-piece Terminal
- Low Thermal Impedance
- Transient PRV Ratings

These rectifiers may be mounted directly to a chassis or fin or may be insulated by using the insulating kit provided. Most units are also available with negative polarity (stud is anode).

JEDEC or GE Type Number	$V_{RM(rep)}$ and $V_{RM(wkg)}$ Volts	Max. $I_{F(AV)}$ @ T_C	I_{FM} (Surge)	Max. Rev. Current $I_{R(AV)}$ @ T_C	Max. T_J in °C	Out-line No.	Comp. Spec. No.
		50°C Amb.		@ 150°C			
1N1124	200	3.0A	25A	.3 ma	150	36	140.42
1N1124A	200	3.3A	25A	.3 ma	150	36	140.42
1N1125	300	3.0A	25A	.3 ma	150	36	140.42
1N1126	400	3.0A	25A	.3 ma	150	36	140.42
1N1126A	400	3.3A	25A	.3 ma	150	36	140.42
1N1127	500	3.0A	25A	.3 ma	150	36	140.42
1N1128	600	3.0A	25A	.3 ma	150	36	140.42
1N1128A	600	3.3A	25A	.3 ma	150	36	140.42
		@ 85°C		T_A = 150°C			
1N3569	100	3.5A	35A	.4 ma	165	27	140.43
1N3570	200	3.5A	35A	.4 ma	165	27	140.43
1N3571	300	3.5A	35A	.4 ma	165	27	140.43
1N3572	400	3.5A	35A	.4 ma	165	27	140.43
1N3573	500	3.5A	35A	.4 ma	165	27	140.43
1N3574	600	3.5A	35A	.4 ma	165	27	140.43
		@ 150°C		@ 150°C			
1N1612	50	5A	150A	1 ma	190	27	140.15
1N1613	100	5A	150A	1 ma	190	27	140.15
1N1614*	200	5A	150A	1 ma	190	27	140.15
1N1615*	400	5A	150A	1 ma	190	27	140.15
1N1616*	600	5A	150A	1 ma	190	27	140.15
*Meets MIL-S-19500/162A U.S. Army Spec.—also in reverse polarity 1N1612R-1616R.							
		@ 145°C		@ 150°C			
1N1341A	50	6A	150A	3 ma	200	27	140.10
1N1342A	100	6A	150A	2.5 ma	200	27	140.10
1N1343A	150	6A	150A	2.25 ma	200	27	140.10
1N1344A	200	6A	150A	2.0 ma	200	27	140.10
1N1345A	300	6A	150A	1.75 ma	200	27	140.10
1N1346A	400	6A	150A	1.5 ma	200	27	140.10
1N1347A	500	6A	150A	1.25 ma	200	27	140.10
1N1348A	600	6A	150A	1.0 ma	200	27	140.10
Reverse units 1N1341RA-1348RA available.							
		@ 145°C		@ 150°C			
1N1199A	50	12A	240A	3.0 ma	200	27	140.20
1N1200A	100	12A	240A	2.5 ma	200	27	140.20
1N1201A	150	12A	240A	2.25 ma	200	27	140.20
1N1202A	200	12A	240A	2.0 ma	200	27	140.20
1N1203A	300	12A	240A	1.75 ma	200	27	140.20
1N1204A	400	12A	240A	1.5 ma	200	27	140.20
1N1205A	500	12A	240A	1.25 ma	200	27	140.20
1N1206A	600	12A	240A	1.0 ma	200	27	140.20
Designed to meet Mil-E-1/1108 USAF Spec. Reverse Polarity 1N1199RA-1206RA.							
		@ 150°C		@ 150°C			
1N3670A	700	12A	240A	.9 ma	200	27	140.21
1N3671A	800	12A	240A	.8 ma	200	27	140.21
1N3672A	900	12A	240A	.7 ma	200	27	140.21
1N3673A	1000	12A	240A	.6 ma	200	27	140.21
New High Voltage—Diffused Junction.							
		@ 150°C		@ 150°C			
1N248	50	10A	200A	5 ma	175	28	140.28
1N249	100	10A	200A	5 ma	175	28	140.28
1N250	200	10A	200A	5 ma	175	28	140.28
1N248A	50	20A	350A	5 ma	175	28	140.28
1N249A	100	20A	350A	5 ma	175	28	140.28
1N250A	200	20A	350A	5 ma	175	28	140.28
1N248B	55	20A	350A	5 ma	175	28	140.28
1N249B*	110	20A	350A	5 ma	175	28	140.28
1N250B*	220	20A	350A	5 ma	175	28	140.28
1N2135*	400	20A	250A	40 ma	150	28	140.28
*Available as military units to Mil-S-19500/134.							

Silicon Medium Current Rectifier Diodes, Cont.

JEDEC or GE Type Number	$V_{RM(rep)}$ and $V_{RM(wkg)}$ Volts	Max. $I_{F(AV)}$ @ T_C	I_{FM} (Surge)	Max. Rev. Current $I_{R(AV)}$ @ T_C	Max. T_J in °C	Out-line No.	Comp. Spec. No.
		@ 150°C		@ 150°C			
1N248C	55	20A	350A	3.8 ma	175	28	140.30
1N249C	110	20A	350A	3.6 ma	175	28	140.30
1N250C	220	20A	350A	3.4 ma	175	28	140.30
1N1195A	300	20A	350A	3.2 ma	175	28	140.30
1N1196A	400	20A	350A	2.5 ma	175	28	140.30
1N1197A	500	20A	350A	2.2 ma	175	28	140.30
1N1198A	600	20A	350A	1.5 ma	175	28	140.30
		@ 145°C		@ 145°C			
1N2154	50	25A	400A	5 ma	200	28	140.40
1N2155	100	25A	400A	4.5 ma	200	28	140.40
1N2156	200	25A	400A	4.0 ma	200	28	140.40
1N2157	300	25A	400A	3.5 ma	200	28	140.40
1N2158	400	25A	400A	3.0 ma	200	28	140.40
1N2159	500	25A	400A	2.5 ma	200	28	140.40
1N2160	600	25A	400A	2.0 ma	200	28	140.40
Available with negative polarity (stud is anode) 1N2154R-2160R.							
		@ 140°C		@ 140°C			
1N1183	50	35A	500A	10 ma	200	32	140.50
1N1184	100	35A	500A	10 ma	200	32	140.50
1N1185	150	35A	500A	10 ma	200	32	140.50
1N1186	200	35A	500A	10 ma	200	32	140.50
1N1187	300	35A	500A	10 ma	200	32	140.50
1N1188	400	35A	500A	10 ma	200	32	140.50
1N1189	500	35A	500A	10 ma	200	32	140.50
1N1190	600	35A	500A	10 ma	200	32	140.50
		@ 140°C		@ 140°C			
1N3765	700	35A	500A	10 ma	200	32	140.50
1N3766	800	35A	500A	10 ma	200	32	140.50
1N3767	900	35A	500A	10 ma	200	32	140.50
1N3768	1000	35A	500A	10 ma	200	32	140.50
New High Voltage.							

General Purpose Types

Up to 20 amperes
Up to 600 volts

General Electric has designed these 20 Ampere rectifiers specifically for the normal industrial and consumer low ambient temperature applications. The design utilizes the smallest practical size for the rating with particular attention to rigidity and rugged construction. The solid one-piece terminal and the case-to-hex solder mounting technique provides good mechanical strength, minimizes breakage problems, and promotes stability of heat transfer characteristics from the diffused junction to the stud.

JEDEC or GE Type Number	$V_{RM(rep)}$ and $V_{RM(wkg)}$ Volts	Max. $I_{F(AV)}$ @ T_C		I_{FM} (Surge)	Max. Rev. Current $I_{R(AV)}$	Max. T_J in °C	Dut-line No.	Comp. Spec. No.
		@ 110°C	@ 150°C					
A40F, A41F	50	20A	15A	300A	10 ma	175	29	140.32
A40A, A41A	100	20A	15A	300A	9 ma	175	29	140.32
A40B, A41B	200	20A	15A	300A	8 ma	175	29	140.32
A40C, A41C	300	20A	15A	300A	6 ma	175	20	140.32
A40D, A41D	400	20A	15A	300A	5 ma	175	29	140.32
A40E, A41E	500	20A	15A	300A	4.5 ma	175	29	140.32
A40M, A41M	600	20A	15A	300A	4 ma	175	29	140.32
		A41F-M is reverse polarity (stud is Anode)						
		@ 110°C	@ 150°C		T_J = 150°C			
A44F, A45F	50	20A	15A	300A	10 ma	175	31	140.33
A44A, A45A	100	20A	15A	300A	9 ma	175	31	140.33
A44B, A45B	200	20A	15A	300A	8 ma	175	31	140.33
A44C, A45C	300	20A	15A	300A	6 ma	175	31	140.33
A44D, A45D	400	20A	15A	300A	5 ma	175	31	140.33
A44E, A45E	500	20A	15A	300A	4.5 ma	175	31	140.33
A44M, A45M	600	20A	15A	300A	4 ma	175	31	140.33
		A45F-M is reverse polarity (case is Anode)						

Silicon High Current Rectifier Diodes

Up to 500 amperes
Up to 1200 volts

These large area junction rectifiers are the ultimate in today's High Current Silicon Rectifier field. By taking full advantage of the most advanced semiconductor component manufacturing techniques, General Electric now offers the industry's first **double diffused, all hard solder** 100 and 250 ampere rectifiers in $V_{RM(rep)}$ ratings up to 1200 volts—also available is a 500 amp rectifier up to 800 volts. As a result, circuit designers now receive:

- Freedom from Thermal Fatigue Failure
- Higher Surge Current Capabilities
- NEMA Overload Ratings
- Forward and Reverse Polarities

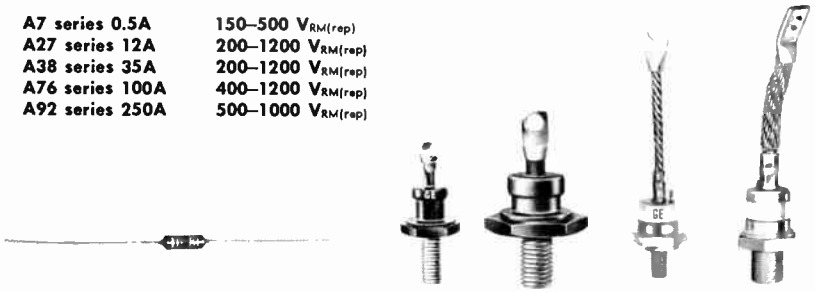
GE Type Number	JEDEC Type Number	$V_{RM(rep)}$ and $V_{RM(wkg)}$ Volts	V_{RM} (non-rep)	Max. $I_{F(AV)}$	I_{FM} (Surge) 1~@ 60 Hz	Max. Rev. Current $I_{R(AV)}$	Max. Oper. Temp. T_J in °C	Out-line No.	Comp. Spec. No.
				T_C = 130°C		T_C = 130°C			
A70B	1N3289	200	300	100A	1600A	9.5 ma	200	33	145.15
A70C	1N3290	300	400	100A	1600A	9.0 ma	200	33	145.15
A70D	1N3291	400	525	100A	1600A	9.0 ma	200	33	145.15
A70E	1N3292	500	650	100A	1600A	8.0 ma	200	33	145.15
A70M	1N3293	600	800	100A	1600A	6.5 ma	200	33	145.15
A70N	1N3294	800	1050	100A	1600A	5.5 ma	200	33	145.15
A70P	1N3295	1000	1300	100A	1600A	4.5 ma	200	33	145.15
A70PB	1N3296	1200	1500	100A	1600A	3.5 ma	200	33	145.15
A71B thru PB (1N3289R-3296R) reverse polarity units available 1N3289M-3295M Military Types per Mil-S-19500/246A									
A90B	1N3736	200	300	250A	4500A	16 ma	200	34	145.30
A90C	1N3737	300	400	250A	4500A	16 ma	200	34	145.30
A90D	1N3738	400	525	250A	4500A	16 ma	200	34	145.30
A90E	1N3739	500	650	250A	4500A	15 ma	200	34	145.30
A90M	1N3740	600	800	250A	4500A	12.5 ma	200	34	145.30
A90N	1N3741	800	1050	250A	4500A	10 ma	200	34	145.30
A90P	1N3742	1000	1300	250A	4500A	8 ma	200	34	145.30
A91B thru A91P (1N3736R-3742R) reverse polarity units (stud is Anode)									
——	1N3260	50	——	160A	2000A	12 ma	175	34	145.28
——	1N3261	100	——	160A	2000A	12 ma	175	34	145.28
——	1N3262	150	——	160A	2000A	12 ma	175	34	145.28
——	1N3263	200	——	160A	2000A	12 ma	175	34	145.28
——	1N3264	250	——	160A	2000A	12 ma	175	34	145.28
——	1N3265	300	——	160A	2000A	12 ma	175	34	145.28
——	1N3266	350	——	160A	2000A	12 ma	175	34	145.28
——	1N3267	400	——	160A	2000A	12 ma	175	34	145.28
——	1N3268	500	——	160A	2000A	12 ma	175	34	145.28
——	1N3269	600	——	160A	2000A	12 ma	175	34	145.28
——	1N3270	700	——	160A	2000A	12 ma	175	34	145.28
——	1N3271	800	——	160A	2000A	12 ma	175	34	145.28
——	1N3272	900	——	160A	2000A	12 ma	175	34	145.28
——	1N3273	1000	——	160A	2000A	12 ma	175	34	145.28

Silicon High Current Rectifier Diodes, con't.

GE Type Number	JEDEC Type Number	$V_{RM(rep)}$ and $V_{RM(wkg)}$ Volts	V_{RM} (non-rep)	Max. $I_{F(AV)}$	I_{FM} (Surge) 1~@ 60 Hz	Max. Rev. Current $I_{R(AV)}$	Max. Oper. Temp. T_J in °C	Out-line No.	Comp. Spec. No.
——	1N4044	50	——	275A	5000A	15 ma	190	34	145.32
——	1N4045	100	——	275A	5000A	15 ma	190	34	145.32
——	1N4046	150	——	275A	5000A	15 ma	190	34	145.32
——	1N4047	200	——	275A	5000A	15 ma	190	34	145.32
——	1N4048	250	——	275A	5000A	15 ma	190	34	145.32
——	1N4049	300	——	275A	5000A	15 ma	190	34	145.32
——	1N4050	400	——	275A	5000A	15 ma	190	34	145.32
——	1N4051	500	——	275A	5000A	15 ma	190	34	145.32
——	1N4052	600	——	275A	5000A	15 ma	190	34	145.32
——	1N4053	700	——	275A	5000A	15 ma	190	34	145.32
——	1N4054	800	——	275A	5000A	15 ma	190	34	145.32
——	1N4055	900	——	275A	5000A	15 ma	190	34	145.32
——	1N4056	1000	——	275A	5000A	15 ma	190	34	145.32
A291PC, 292PC	——	1300	1500	250A	4500A	8 ma	200	35	145.58
A291PD, 292PD	——	1400	1600	250A	4500A	8 ma	200	35	145.58
A291PE, 292PE	——	1500	1700	250A	4500A	8 ma	200	35	145.58
A291PM, 292PM	——	1600	1800	250A	4500A	8 ma	200	35	145.58
A291PS, 292PS	——	1700	1900	250A	4500A	8 ma	200	35	145.58
A291PN, 292PN	——	1800	2000	250A	4500A	8 ma	200	35	145.58
A295B, 296B	——	200	400	500A	7000A	15 ma	200	35	145.60
A295C, 296C	——	300	500	500A	7000A	15 ma	200	35	145.60
A295D, 296D	——	400	600	500A	7000A	15 ma	200	35	145.60
A295E, 296E	——	500	700	500A	7000A	15 ma	200	35	145.60
A295M, 296M	——	600	800	500A	7000A	15 ma	200	35	145.60
A295S, 296S	——	700	900	500A	7000A	15 ma	200	35	145.60
A295N, 296N	——	800	1000	500A	7000A	15 ma	200	35	145.60
A295T, 296T	——	900	1100	500A	7000A	15 ma	200	35	145.60
A295P, 296P	——	1000	1200	500A	7000A	15 ma	200	35	145.60
A295PA, 296PA	——	1100	1300	500A	7000A	15 ma	200	35	145.60
A295PB, 296PB	——	1200	1400	500A	7000A	15 ma	200	35	145.60
A295PC, 296PC	——	1300	1500	500A	7000A	15 ma	200	35	145.60
A295PD, 296PD	——	1400	1600	500A	7000A	15 ma	200	35	145.60
A295PE, 296PE	——	1500	1700	500A	7000A	15 ma	200	35	145.60
A295PM, 296PM	——	1600	1800	500A	7000A	15 ma	200	35	145.60
A295PS, 296PS	——	1700	1900	500A	7000A	15 ma	200	35	145.60
A295PN, 296PN	——	1800	2000	500A	7000A	15 ma	200	35	145.60

Controlled Avalanche Rectifier Diodes

A7 series 0.5A 150–500 $V_{RM(rep)}$
A27 series 12A 200–1200 $V_{RM(rep)}$
A38 series 35A 200–1200 $V_{RM(rep)}$
A76 series 100A 400–1200 $V_{RM(rep)}$
A92 series 250A 500–1000 $V_{RM(rep)}$



Featuring these outstanding advances in silicon rectifier applications:

- Self-protection against normal voltage transient. Dissipates many watts of peak power in reverse direction. Permits decreased peak reverse voltage safety factors in equipment due to greatly reduced transient voltage vulnerability.
- New standards of reliability at peak reverse voltages.
- Protection of other circuit components against overvoltage through rigidly specified maximum/minimum avalanche characteristics.
- Makes ideal voltage equalizing elements for series connected SCR's and conventional silicon rectifiers, also for anode triggering SCR's to prevent damage from voltage transients in forward direction.
- Simplified series operation of rectifiers in high voltage applications—no shunting resistors necessary for Controlled Avalanche Rectifiers. Makes possible compact high voltage assemblies.
- Can operate in Avalanche breakdown region at high voltages—unharmed by hi-pot and megger tests.

For information on application of Controlled Avalanche Rectifiers, see Section 15.3.4 and Application Note 200.27, "An Introduction to the Controlled Avalanche Silicon Rectifier."

JEDEC or GE Type Number	$V_{RM(rep)}$ and $V_{RM(wkg)}$ Volts	Avalanche Voltage T_J = 25°C Min.	Avalanche Voltage T_J = 25°C Max.	Max. Rev. Power Surge P_{RM} (non-rep)	Max. $I_{F(AV)}$	I_{FM} (Surge)	Max. Rev. Current $I_{R(AV)}$ @ $V_{RM(wkg)}$	Max. T_J in °C	Outline No.	Comp. Spec. No.
				T_J = 50°C	T_A = 50°C		T_A = 150°C			
A7G	150	200	450	310W	500 ma	10A	100 μa	175	22	125.8
A7B	200	300	550	310W	500 ma	10A	100 μa	175	22	125.8
A7C	300	400	650	310W	500 ma	10A	100 μa	175	22	125.8
A7D	400	500	750	310W	500 ma	10A	100 μa	175	22	125.8
A7E	500	600	850	310W	500 ma	10A	100 μa	175	22	125.8
Units also available in Potted Assemblies up to 10kv and 820 ma.										
				T_J = 25°C	T_C = 135°C		T_C = 135°C			
A27B	200	250	515	3.9Kw	12A	240A	2.5 ma	175	27	140.24
A27C	400	500	770	3.9Kw	12A	240A	2.5 ma	175	27	140.24
A27M	600	750	1030	3.9Kw	12A	240A	2.5 ma	175	27	140.24
A27N	800	1000	1290	3.9Kw	12A	240A	2.0 ma	175	27	140.24
A27P	1000	1250	1550	3.9Kw	12A	240A	1.75 ma	175	27	140.24
A27PB	1200	1500	1930	3.9Kw	12A	240A	1.5 ma	175	27	140.24
					T_C = 115°C		T_C = 115°C			
A38B	200	250	515	12Kw	35A	500A	3.5 ma	175	32	140.37
A38D	400	500	770	12Kw	35A	500A	3.5 ma	175	32	140.37
A38M	600	750	1030	12Kw	35A	500A	3.5 ma	175	32	140.37
A38N	800	1000	1290	12Kw	35A	500A	3.0 ma	175	32	140.37
A38P	1000	1250	1550	12Kw	35A	500A	2.5 ma	175	32	140.37
A38PB	1200	1500	1930	12Kw	35A	500A	2.0 ma	175	32	140.37

Fast Recovery Rectifier Diodes

FEATURES:

- Fast Recovery Time
- For Use in:
  - —Inverters
  - —Choppers
  - —Low RF Interference Applications
  - —Free-Wheeling Rectifier Applications
  - —Sonar Power Supplies
  - —Ultrasonic Systems
  - —DC-DC Power Supplies

JEDEC or GE Type Number	Repetitive PRV	Max. I_{DC} Single Phase	Max. Peak 1 Cycle Surge	Max. Rev. Current $I_{R(AV)}$	Max. Oper. °C	Outline No.	Max. Recovery Time (n Sec.)	Comp. Spec. No.
1N3958	100	3.5A	35A	.4 ma	165	27	3000	140.44
1N3959	200	3.5A	35A	.4 ma	165	27	3000	140.44
1N3960	300	3.5A	35A	.4 ma	165	27	3000	140.44
1N3961	400	3.5A	35A	.4 ma	165	27	3000	140.44
1N3962	500	3.5A	35A	.4 ma	165	27	3000	140.44
1N3963	600	3.5A	35A	.4 ma	165	27	3000	140.44
		Case @ 100°C		Case @ 100°C				
1N3879, R	50	6A	75A	1.0 ma	150	27	200	140.12
1N3880, R	100	6A	75A	1.0 ma	150	27	200	140.12
1N3881, R	200	6A	75A	1.0 ma	150	27	200	140.12
1N3882, R	300	6A	75A	1.0 ma	150	27	200	140.12
1N3883, R	400	6A	75A	1.0 ma	150	27	200	140.12
		Case @ 135°C		Case @ 135°C				
A28A	100	12A	240A	8.0 ma	175	27	100	140.23
A28B	200	12A	240A	8.0 ma	175	27	100	140.23
A28C	300	12A	240A	8.0 ma	175	27	100	140.23
A28D	400	12A	240A	8.0 ma	175	27	100	140.23
A28F	50	12A	240A	8.0 ma	175	27	100	140.23
		Case @ 100°C		Case @ 100°C				
1N3889, R	50	12A	150A	3.0 ma	150	27	200	140.22
1N3890, R	100	12A	150A	3.0 ma	150	27	200	140.22
1N3891, R	200	12A	150A	3.0 ma	150	27	200	140.22
1N3892, R	300	12A	150A	3.0 ma	150	27	200	140.22
1N3893, R	400	12A	150A	3.0 ma	150	27	200	140.22
		Case @ 100°C		Case @ 100°C				
1N3899, R	50	20A	225A	10 ma	150	28	200	140.47
1N3900, R	100	20A	225A	10 ma	150	28	200	140.47
1N3901, R	200	20A	225A	10 ma	150	28	200	140.47
1N3902, R	300	20A	225A	10 ma	150	28	200	140.47
1N3903, R	400	20A	225A	10 ma	150	28	200	140.47
1N3909, R	50	30A	300A	15 ma	150	28	200	140.48
1N3910, R	100	30A	300A	15 ma	150	28	200	140.48
1N3911, R	200	30A	300A	15 ma	150	28	200	140.48
1N3912, R	300	30A	300A	15 ma	150	28	200	140.48
1N3913, R	400	30A	300A	15 ma	150	28	200	140.48

21.3.5 Silicon Zener Diodes

CONDENSED SPECIFICATIONS—COMPLETE SPECIFICATION NUMBERS LISTED IN TABLES

1 Watt Axial Lead
Zener voltages from 5.1 to 22 volts

These 1 watt Zener Diodes utilize the all welded flangeless package for ease in mounting. This small package is a tried and proved design with an exceptional reliability history over the past several years. The design incorporates know-how which promotes very good voltage regulation and voltage stability over a long period of time under the severest environmental conditions.

RATING TABLES

JEDEC or GE Type Number	V_{ZT} @ I_{ZT} Nominal Zener Voltage @ 25°C Volts	Test Current I_{ZT} mA	Maximum Dynamic Impedance Z_{ZT} @ I_{ZT} @ 25°C Ohms	Typical Voltage Regulation $\triangle V_Z$ Volts	Maximum Zener Current I_{ZM} $T_A = 50°C$ Maximum	Outline No.	Max. T_J in °C	Comp. Spec. No.
Z4X5.1B	8.2	100	7.0	0.11	160 ma	15	175	185.50
1N1765	9.1	100	1.2	0.14	150 ma	15	175	185.50
1N1766	10.0	100	1.5	0.16	130 ma	15	175	185.50
1N1767	11.0	100	1.7	0.20	120 ma	15	175	185.50
1N1768	12.0	100	2.1	0.24	109 ma	15	175	185.50
1N1769	13.0	100	2.4	0.28	100 ma	15	175	185.50
1N1770	14.0	50	3.0	0.34	90 ma	15	175	185.50
1N1771	15.0	50	3.5	0.41	82 ma	15	175	185.50
1N1772	16.0	50	4.2	0.48	74 ma	15	175	185.50
1N1773	12.0	50	5.0	0.57	68 ma	15	175	185.50
1N1774	13.0	50	5.8	0.66	63 ma	15	175	185.50
Z4X14B	14.0	50	6.6	0.75	58 ma	15	175	185.50
1N1775	15.0	50	7.6	0.86	54 ma	15	175	185.50
1N1776	16.0	50	8.6	0.97	51 ma	15	175	185.50

Standard types are supplied to the ±10% of voltage values listed. For 5% tolerance, change B suffix to A suffix in GE Type Number (i.e., Z4X5.-1A), add A suffix in 1N number (i.e., 1N1776A).
The Z4X6.2 to XL22, 1 watt zener diodes are intended for consumer and low cost industrial applications. While designed and produced for economy, this design features low thermal resistance, good voltage regulation and stability.

Z4XL6.2	6.2	20	9.0	——	123 ma	15	165	185.40
Z4XL7.5	7.5	20	12.0	——	101 ma	15	165	185.40
Z4XL9.1	9.1	20	15.0	——	83 ma	15	165	185.40
Z4XL12	12.0	20	24.0	——	63 ma	15	165	185.40
Z4XL14	14.0	20	30.0	——	54 ma	15	165	185.40
Z4XL16	16.0	20	40.0	——	47 ma	15	165	185.40
Z4XL18	18.0	20	50.0	——	43 ma	15	165	185.40
Z4XL20	20.0	20	60.0	——	38 ma	15	165	185.40
Z4XL22	22.0	20	72.0	——	34 ma	15	165	185.40

Standard types are supplied to ±20% of nominal voltage values listed.
For ±10% tolerance, add suffix B to GE type number (i.e., Z4XL6.2B).

21.3.6 Triac and SCR Assemblies Condensed Specifications

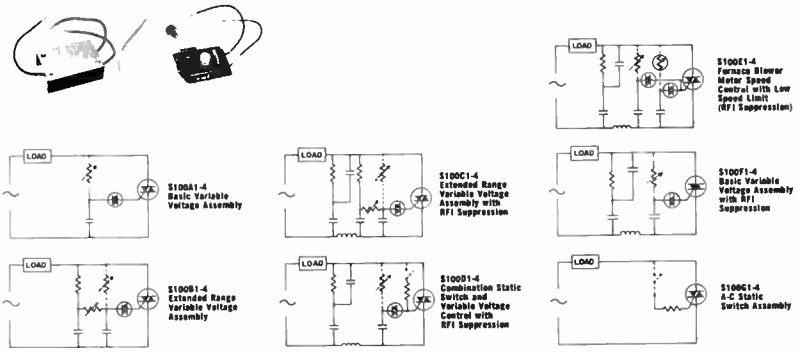
CONDENSED SPECIFICATIONS—FOR COMPLETE SPECIFICATIONS SEE 155.20 THROUGH 155.26

S100 LINE—STANDARD TRIAC CIRCUIT ASSEMBLIES

Available with either 6 amp or 10 amp TRIAC's, these seven circuit configurations can be obtained for use on either 115 or 230V (RMS) power lines.

All of these assemblies feature an electrically isolated heatsink allowing it to be mounted directly to the metal frame of the equipment.

As the titles imply, these circuit variations allow a wide variety of uses, including simple voltage control, shaded-pole or permanent split capacitor type motor speed control, resistance heating control and many others.



Suffix numbers (e.g. 1, 2, 3 or 4). Refer to the rating of the TRIAC used in the circuit as follows:

"1"— 6 amp 200V TRIAC (for use on 115V line)
"2"— 6 amp 400V TRIAC (for use on 230V line)
"3"—10 amp 200V TRIAC (for use on 115V line)
"4"—10 amp 400V TRIAC (for use on 230V line)

For complete rating and descriptive information, refer to the specification sheets for the particular circuit configuration desired. These specifications are available upon request.

21.3.7 Rectifier Stacks

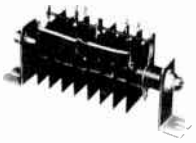
Germanium Low Current

Up to 630 PRV. or 6 amps. @ 55°C amb.

4JA211 Stacks: The industry's most widely used semiconductor rectifier series. Hundreds of thousands in use. May be arranged in stacks up to 12 fins to produce more than 160 various circuit configurations. Small, lightweight, excellent regulation.

Silicon Low Current

Up to 3360 PRV. or 18 amps. @ 25°C amb.



4JA411 Stacks: Combine high temperature operation (up to 150°C) with increased ratings (up to 18 amps DC). Hundreds of stack combinations to meet a variety of circuit conditions. High efficiency plus excellent regulation.

4JA1011 Stacks: Available in same mechanical and circuit configurations and featuring 45 amp, one cycle surge rating.

Silicon Medium Current

Up to 65 amps @ 55°C amb. Up to 1800 PRV.

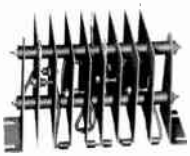
4JA2011 Stacks: Provides a wide range of power applications with DC outputs up to 32 amps.

4JA2511 Stacks: Provide a wide range of power applications with DC outputs up to 50 amps.

4JA3511 Stacks: Provide a wide range of power applications with DC outputs up to 65 amps.

Silicon Medium Current (5" Fin)

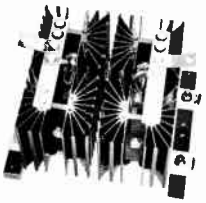
Up to 108 amps @ 55°C amb. Up to 1800 PRV.



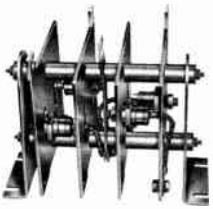
4JA3512 Stacks: This 5" square fin assembly makes optimum use of the 1N2154 series 25 ampere cell. This stack provides a wide range of power applications with DC outputs up to 108 amperes.

Silicon High Current

Up to 690 amps @ 40°C amb. Up to 1,000 PRV.

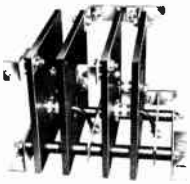


4JA7014
4JA9015



4JA7012
4JA9016

4JA7011



4JA7013
4JA9013

4JA7011 3½" x 3½" x 2" Aluminum Extrusion Stacks: Particularly suitable for free convection applications. Plated copper terminals for all connections.

4JA7012, 4JA7013 Stacks: Available with a choice of two heatsink sizes; the 5" x 5" x ⅛" flat copper fin (7012) and the 7" x 7" x ⅜" flat aluminum fin (7013). Lightweight units with outputs up to 165 amps DC.

4JA7014 Stacks: The 4JA7014 stack line has been designed especially for free convection cooled applications where a maximum amount of current is required in a relatively small space. Fin size is 4" x 4" x 5" anodized aluminum. DC outputs up to 240 amps, free convection cooled in 40°C ambient.

4JA9013 Stacks: DC outputs up to 250 amps, per fin, forced air cooled, in 40°C ambient. Utilizes lightweight 7" x 7 "x ⅜" aluminum fin. Heat dissipation abilities equal to 7" x 7" x ¼" nickel-plated copper, yet less than half the weight of copper fin stacks.

4JA9015 Aluminum Extrusion Stacks: Designed for maximum heat dissipation in free convection cooled applications. Plated copper terminals for all purchaser connections.

4JA9016 Stacks: Different rectifier configurations available on 5" x 5" nickel-plated copper flat fins. Fin thickness ⅛".

NOTE: Series and parallel configurations available in all High Current Stacks.

Potted Rectifier Circuits

4JA220, 4JA420-421-422 Series: Mounted in standard eight pin tube base (4JA220-420 Series) or in rectangular design with solder lug connections (4JA221-421-422 Series). Available in a large number of circuit configurations. One to 20 cells may be potted in a single circuit. Individual cell specifications determine ratings. 4JA220 Series utilize germanium 1N91-93 cells. 4JA420-421-422 Series utilize silicon 1N536-540, 1N1095 cells. (See BASIC RECTIFIER CELL LISTING.)

	Up to:	Up to:
4JA220	.4 amp @ 55°C amb.	1,800 PRV.
4JA420	2.0 amps @ 50°C amb.	3,000 PRV.
4JA421	.65 amp @ 25°C amb.	10,000 PRV.
4JA422	1.50 amps @ 25°C amb.	2,000 PRV.

Controlled Avalanche Rectifiers in Potted Assemblies

1N1730, 1N2382 and A725 Series: Controlled Avalanche rectifiers potted in axial lead cartridge type assemblies.

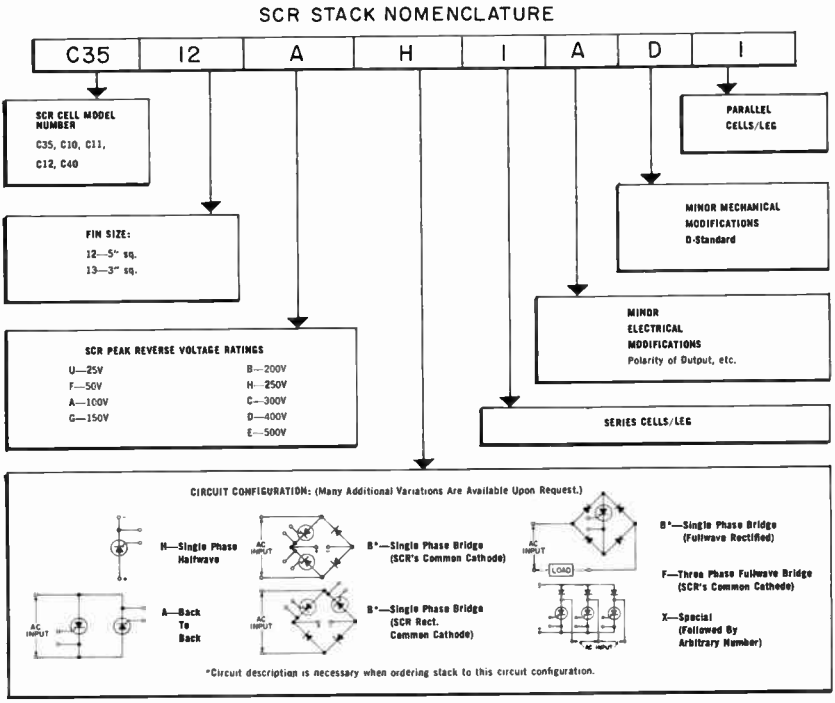
A723 Series: Potted block assemblies utilizing A7 Controlled avalanche cells. Available in half wave, center tap, voltage doublers, full-wave bridge, single phase or three phase.

	Up to:	Up to:
1N1730	.1 amp @ 100°C amb.	5,000 PRV.
1N2382	.075 amp @ 100°C amb.	10,000 PRV.
A725	.150 amp @ 100°C amb.	10,000 PRV.
A723	.820 amp @ 50°C amb.	6,000 PRV.

21.3.8 SCR Combination Stacks

General Electric's broad line of SCR's and rectifiers permits the offering of packaged SCR building blocks. Low, medium and high current packaged SCR blocks, complete with SCR's, compatible rectifiers, inter-connections, heatsinks, and all required hardware in one package are available from your authorized General Electric semiconductor distributor or electronic components district sales.

The SCR stack nomenclature below summarizes the significance of the letters and numerals used when ordering SCR stacks. Complete specification sheets on the various low, medium and high current stacks can be obtained by writing to General Electric Company, Distribution Services, Bldg. 6—Room 208, 1 River Road, Schenectady, N. Y. 12305, for bulletins 170.40, 195.10, 195.10.1 and 195.40.



SCR Combination Stacks, con't.

SERIES:
C3512, 13
C4012, 13
C1012, 13
C1112, 13
C1212, 13

Up to 13.65A per fin free convection rating in 25°C ambient.

Up to 23.5A per fin forced cooling in 25°C ambient.

Two fin sizes (3" x 3", 5" x 5") and 5 SCR types permit an optimum designed assembly for each application. Stacks can be mounted in either vertical or horizontal plane. An almost limitless number of circuit configurations available. Will operate from −65°C up to +150°C.

SERIES:
C5014, C15014, C18015
C5514, C15114, C18115
C6014, C15414, C18515
C8015, C15514

Up to 102 amps per fin free convection rating in 30°C ambient. Aluminum extrusions designed specifically for maximum heat dissipation when used with any GE high current SCR. Hundreds of configurations available.

SERIES:
C28120
C29120
A29620

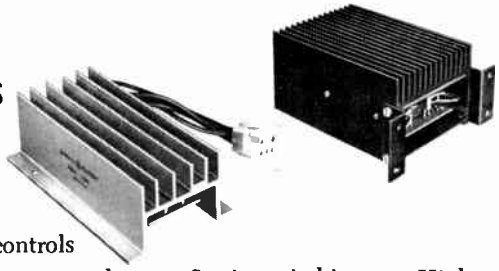
High power semiconductors, mounted on heatsink designed for high velocity forced cooling, permit operation at or near nameplate ratings at industrial ambient temperatures.

SERIES:
14040-46
14140-46

The new General Electric Power Thyristors are designed primarily to provide high frequency, high current power switching up to 25 kHz. The GE High Frequency Power Thyristor is a uniquely packaged arrangement of selected integral devices with common anode and cathode terminations. These parallel units, mounted on a common heatsink, provide a convenient, economical means of attaining higher frequency performance at current levels up to 120 amps average.

For complete specifications, see 160.38.

21.4 CUSTOMIZED ASSEMBLIES



Typical Applications Include:

• SCR and TRIAC motor speed controls • Solid state replacements for thyratron tubes • Static switching • High voltage rectifier stacks • Molded multiple diode modules for computer logic circuits • Molded SCR and transistor modules for computer and other uses • Temperature controllers • Automatic exposure lamp controls for copying machines, etc. • Light activated controls

Complete semiconductor circuit assemblies using discrete components are available in a variety of mechanical configurations, including printed circuit boards, potted modules, standard tube shells and many special packages to meet individual customer needs.

SOLID STATE THYRATRONS

G-E Type Number	Peak Annode Voltage	Cathode Current	Max. Temp. T_A	May Replace
S-26	200 V	1.0 A RMS @ 30° C	125° C	2D21
S-27	200 V	1.0 A RMS @ 30° C	125° C	2050

21.5 GENERAL ELECTRIC SILICON CONTROLLED RECTIFIERS AND DIODES WHICH MEET MILITARY SPECIFICATIONS

Silicon Controlled Rectifiers

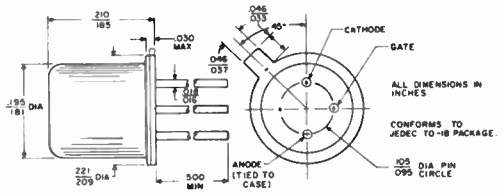
Type	MIL Specification	$V_{RM(rep)}$ and $V_{(BR)FO}$	Max. I_F	Comp. Spec. No.
USN 2N2323, A	MIL-S-19500/276	50	1.6A	150.10
USN 2N2324, A	MIL-S-19500/276	100	1.6A	150.10
USN 2N2326, A	MIL-S-19500/276	200	1.6A	150.10
JAN 2N1771A	MIL-S-19500/168B	50	7A	150.20
JAN 2N1772A	MIL-S-19500/168B	100	7A	150.20
JAN 2N1774A	MIL-S-19500/168B	200	7A	150.20
JAN 2N1776A	MIL-S-19500/168B	300	7A	150.20
JAN 2N1777A	MIL-S-19500/168B	400	7A	150.20
	For low power switching and control applications.			
JAN 2N682	MIL-S-19500/108B	50	35A	160.20
JAN 2N683	MIL-S-19500/108B	100	35A	160.20
JAN 2N685	MIL-S-19500/108B	200	35A	160.20
JAN 2N686	MIL-S-19500/108B	250	35A	160.20
JAN 2N687	MIL-S-19500/108B	300	35A	160.20
JAN 2N688	MIL-S-19500/108B	400	35A	160.20
JAN 2N689	MIL-S-19500/108B	500	35A	160.20
	For medium power switching and control applications.			
USN 2N1910W	MIL-S-19500/204A	50	110A	170.20
USN 2N1911W	MIL-S-19500/204A	100	110A	170.20
USN 2N1912W	MIL-S-19500/204A	200	110A	170.20
USN 2N1913W	MIL-S-19500/204A	300	110A	170.20
USN 2N1914W	MIL-S-19500/204A	400	110A	170.20
USN 2N2031W	MIL-S-19500/204A	50	110A	170.26
	For high power switching and control applications.			

Diodes

Type	MIL Specification	$V_{RM(rep)}$	Max. $I_{F(AV)}$	Spec. No.
		GERMANIUM		
USN 1N93A	MIL-S-19500/293A	300 volts	75 ma @ 55°C Amb.	120.5
		SILICON SUBMINIATURE		
JAN 1N645, 647, 649	MIL-S-19500/240B	225 to 600 volts	150 ma @ 150°C Amb.	125.5
JAN 1N914	MIL-S-19500/116B	75 volts	150 ma @ 25°C Amb.	75.28
USN 1N3064	MIL-S-19500/144C	75 volts	150 ma @ 25°C Amb.	75.25
JAN 1N4148	MIL-S-19550/116B	75 volts	150 ma @ 25°C Amb.	75.28
USN 1N4454	MIL-S-19500/144C	50 volts	150 ma @ 25°C Amb.	75.25
		SILICON LOW CURRENT		
JAN 1N538, 40, 47	MIL-S-19500/202A	200 to 600 volts	250 ma @ 150°C Amb.	130.10
USN 1N3189, 90, 91	MIL-S-19500/155C	200 to 600 volts	1A @ 100°C Amb.	130.46
		SILICON MEDIUM CURRENT		
JAN 1N249B, 50B	MIL-S-19500/134A	100 to 200 volts	20A @ 150°C Case	140.28, 30
JAN 1N1202, 4, 6 2R, 4R	MIL-S-19500/260	200 to 600 volts	12A @ 150°C Case	140.20
JAN 1N1614, 15, 16 and R	MIL-S-19500/162B	200 to 400 volts	5A @ 150°C Case	140.15
		SILICON HIGH CURRENT		
JAN 1N1184, 86, 88, 84R, 86R, 88R	MIL-S-19500/297	100 to 400 volts	35A @ 140°C Case	140.50
JAN 1N3289, 91, 93, 94, 95 and R's	MIL-S-19500/246C	200 to 1000 volts	100A @ 130°C Case	145.15

21.6 OUTLINE DRAWINGS

1



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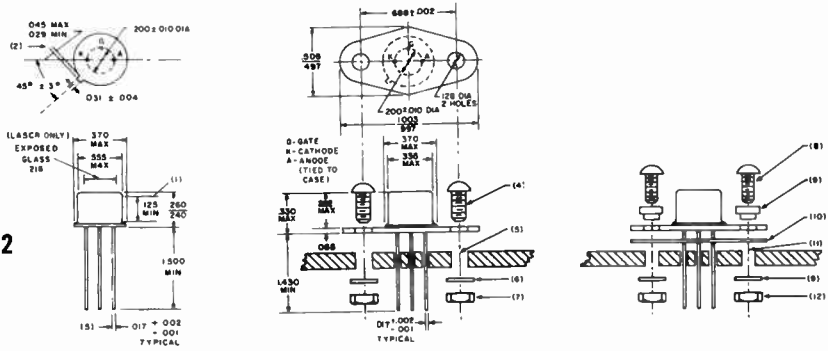


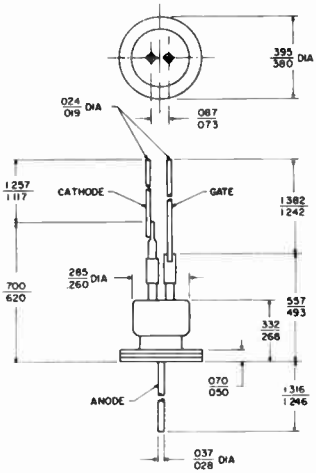
CONFORMS TO JEDEC TO-5 OUTLINE

DIAMOND BASE STANDARD MOUNTING

DIAMOND BASE INSULATED MOUNTING

(1) This zone is controlled for automatic handling. The variation in actual diameter within this zone shall not exceed .010.
(2) Measured from max. diameter of the actual device.
(3) The specified lead diameter applies in the zone between .050 and .250 from the base seat. Between .250 and 1.5 maximum of .021 diameter is held. Outside of these the lead diameter is not controlled. Leads may be inserted without damage in .031 holes while device enters .371 hole concentric with lead hole circle.
(4) #4-40 screw, stainless steel 3/16" long
(5) .120 hole (#31 drill)
(6) Int. tooth lockwasher, stainless steel
(7) #4-40 nut, stainless steel
(8) #2-56 screw, stainless steel 3/16" long
(9) Shoulder washer, vulcanized fiber
(10) Mica insulator, .003 thick
(11) .0935 hole (#42 drill)
(12) #2-56 nut, stainless steel
All dimensions in inches

3



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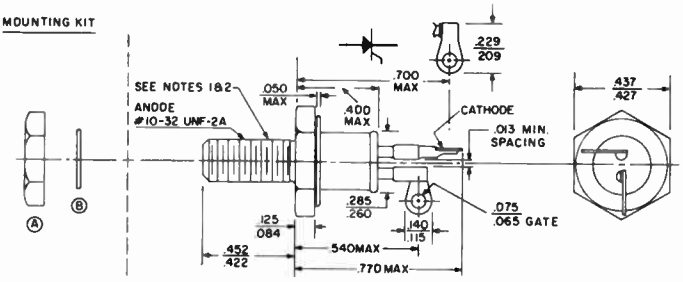
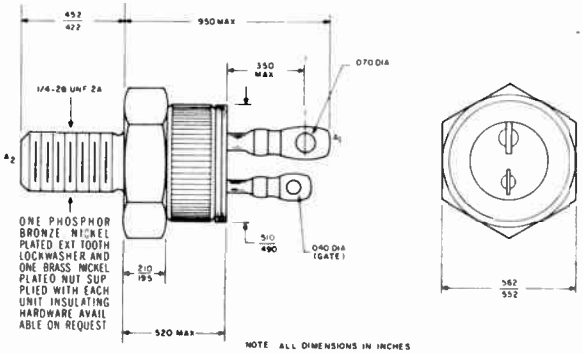


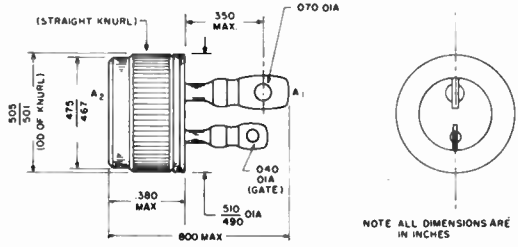
Ⓐ 10-32 BRASS NUT, Ni PLATED, .117 MIN. THK.

Ⓑ EXT. TOOTH LOCK-WASHER, PHOS. BRONZE, NI PLATED, .020 MIN. THK.

NOTES:
1. COMPLETE THREAD TO EXTEND TO WITHIN 2-1/2 THREADS OF HEAD.
2. DIAMETER OF UNTHREADED PORTION .190 MAX.
3. ANGULAR ORIENTATION OF THESE TERMINALS IS UNDEFINED.
4. CASE IS ANODE CONNECTION.
5. ALL DIMENSIONS IN INCHES

5





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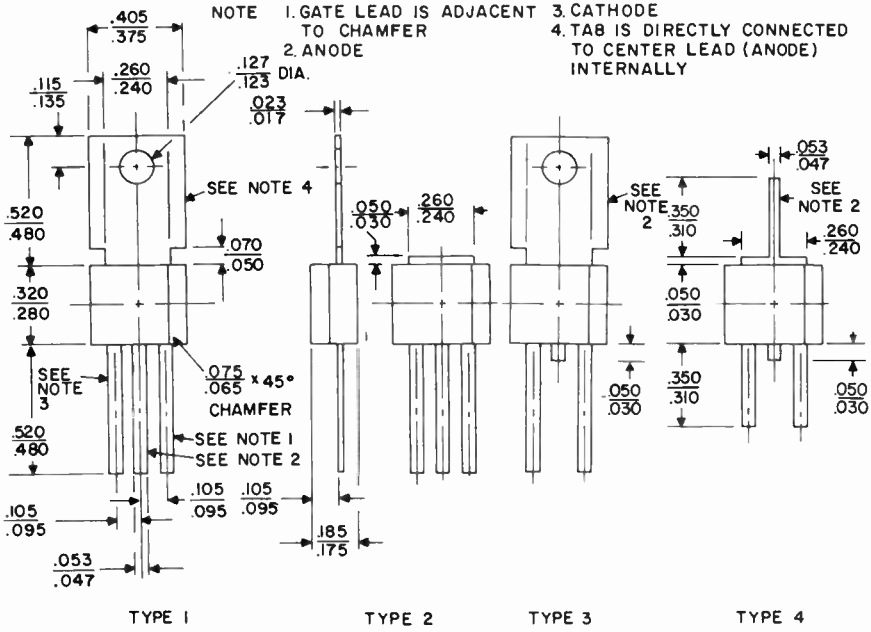
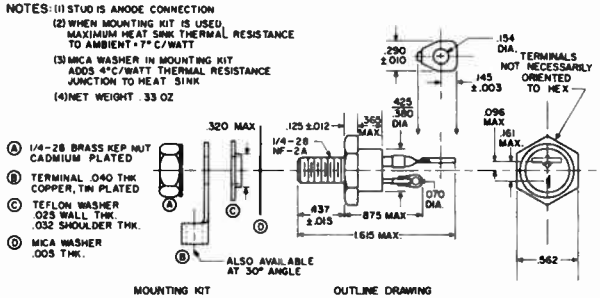
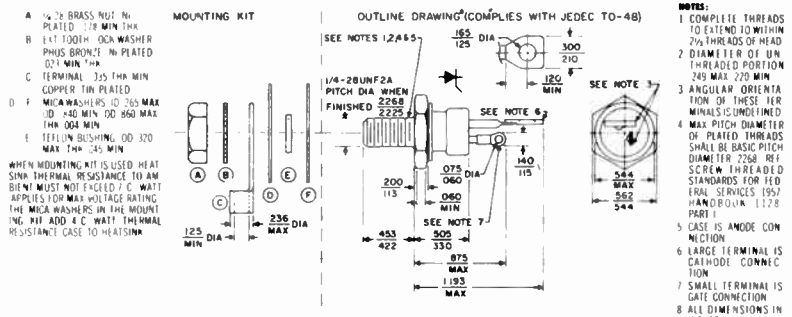

NOTE 1. GATE LEAD IS ADJACENT TO CHAMFER
2. ANODE
3. CATHODE
4. TAB IS DIRECTLY CONNECTED TO CENTER LEAD (ANODE) INTERNALLY
.405 .375
.260 .240
.115 .135
.127 .123 DIA.
.023 .017
SEE NOTE 4
.520 .480
.070 .050
.320 .280
SEE NOTE 3
.075 .065 x 45° CHAMFER
SEE NOTE 1
SEE NOTE 2
.520 .480
.105 .095
.105 .095
.105 .095
.053 .047
.185 .175
.050 .030
.260 .240
SEE NOTE 2
.050 .030
.053 .047
SEE NOTE 2
.350 .310
.260 .240
.050 .030
.350 .310
.050 .030
TYPE 1
TYPE 2
TYPE 3
TYPE 4

7

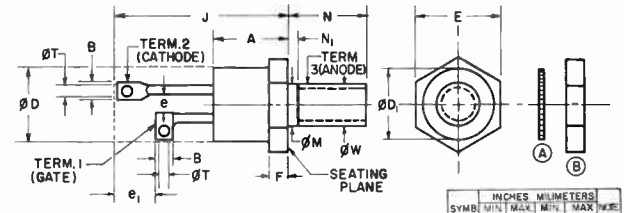

NOTES: (1) STUD IS ANODE CONNECTION
(2) WHEN MOUNTING KIT IS USED, MAXIMUM HEAT SINK THERMAL RESISTANCE TO AMBIENT = 7° C/WATT
(3) MICA WASHER IN MOUNTING KIT ADDS 4°C/WATT THERMAL RESISTANCE JUNCTION TO HEAT SINK
(4) NET WEIGHT .33 OZ
Ⓐ 1/4-28 BRASS KEP NUT CADMIUM PLATED
Ⓑ TERMINAL .040 THK COPPER, TIN PLATED
Ⓒ TEFLON WASHER .025 WALL THK. .032 SHOULDER THK.
Ⓓ MICA WASHER .005 THK.
320 MAX
.125 ±.012
1/4-28 NF-2A
.360 MAX.
.290 ±.010
.154 DIA.
TERMINALS NOT NECESSARILY ORIENTED TO HEX
.145 ±.003
.425 .380 DIA
.096 MAX
.161 MAX.
.070 DIA.
.437 ±.015
.875 MAX
1.615 MAX.
.562
ALSO AVAILABLE AT 30° ANGLE
MOUNTING KIT
OUTLINE DRAWING

8


A 4-28 BRASS NUT Ni PLATED .128 MIN THK
B EXT TOOTH LOCK WASHER PHOS BRONZE Ni PLATED .021 MIN THK
C TERMINAL .035 THK MIN COPPER TIN PLATED
D MICA WASHERS ID .265 MAX OD .480 MIN OD .860 MAX THK .004 MIN
E TEFLON BUSHING OD .320 MAX THK .045 MIN
WHEN MOUNTING KIT IS USED HEAT SINK THERMAL RESISTANCE TO AMBIENT MUST NOT EXCEED 7° C/WATT APPLIES FOR MAX VOLTAGE RATING THE MICA WASHERS IN THE MOUNTING KIT ADD 4° C/WATT THERMAL RESISTANCE CASE TO HEATSINK
MOUNTING KIT
OUTLINE DRAWING (COMPLIES WITH JEDEC TO-48)
SEE NOTES 1,2,&5
.165 .125 DIA
.300 .210
.120 MIN
SEE NOTE 3
1/4-28UNF2A PITCH DIA WHEN FINISHED .2268 .2225
SEE NOTE 6
.140 .115
.200 .113
.075 .060 DIA
.060 MIN
SEE NOTE 7
.544 MAX .562 .544
.125 MIN DIA
.236 DIA MAX
.453 .422
.505 .330
.875 MAX
1.193 MAX
NOTES:
1 COMPLETE THREADS TO EXTEND TO WITHIN 2½ THREADS OF HEAD
2 DIAMETER OF UNTHREADED PORTION .249 MAX .220 MIN
3 ANGULAR ORIENTATION OF THESE TERMINALS IS UNDEFINED
4 MAX PITCH DIAMETER OF PLATED THREADS SHALL BE BASIC PITCH DIAMETER .2268 REF SCREW THREADED STANDARDS FOR FED ERAL SERVICES 1957 HANDBOOK H28 PART I
5 CASE IS ANODE CONNECTION
6 LARGE TERMINAL IS CATHODE CONNECTION
7 SMALL TERMINAL IS GATE CONNECTION
8 ALL DIMENSIONS IN INCHES

9

(Complies with JEDEC registered TO-64 outline)

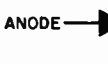


NOTES:
(1) Contour and orientation of fixed terminal lugs are optional
(2) The outlined contour (with exception of hexagon) is optional within zone defined by øD and J
(3) Maximum diameter of seating plane
(4) A chamfer (or undercut) on one or both ends of hexagonal portion is optional
(5) Minimum difference in terminal lengths to establish datum line for numbering terminals
(6) Pitch diameter—thread 10-32 NF 2A (Coated) Reference (Screw Thread Standards for Federal Services 1957) Handbook 1957 H28
(7) Minimum spacing between terminals
(8) Insulating kit available upon request

Ⓐ STEEL LOCKWASHER NI-PLATED

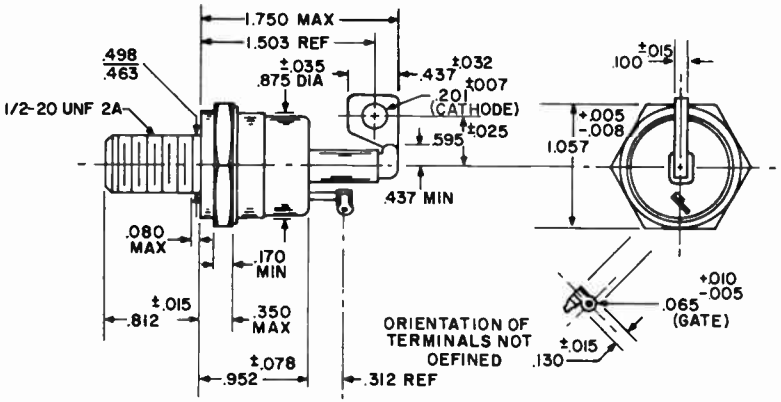
Ⓑ 10-32 BRASS HEX NUT, NI PLATED

SYMB	INCHES MIN.	INCHES MAX.	MILIMETERS MIN.	MILIMETERS MAX.	NOTE
ø	.300	.400	7.62	10.16	
B	.080	.139	2.03	3.45	3
øD		.498		12.77	2
øD1	.400		10.16		3, 6
E	.424	.437	10.77	11.10	
e	.213		5.32		7
e1	.060		1.52		5
F	.060	.175	1.52	4.45	4
J	.700	.875	17.78	21.72	2
øM	.163	.189	4.14	4.80	
N	.400	.453	10.16	11.51	
N1		.378		1.98	
øT	.088	.093	2.02	2.41	
øW	.1618	.1697	4.212	4.310	8

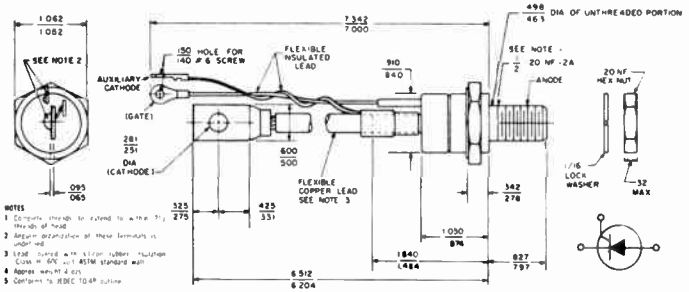


NOTE:
One 1/2-20 brass Ni plated nut and one silicon bronze spring lockwasher supplied with each unit.

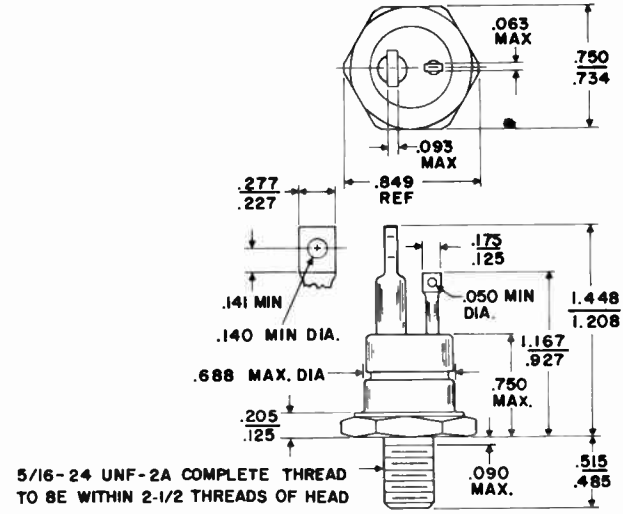
10



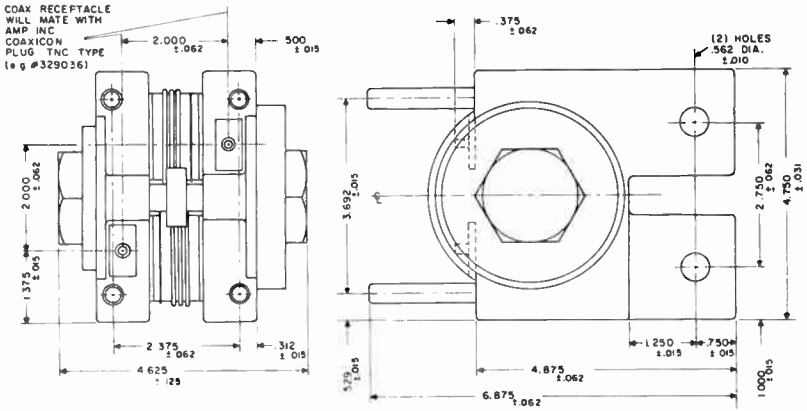
11



12

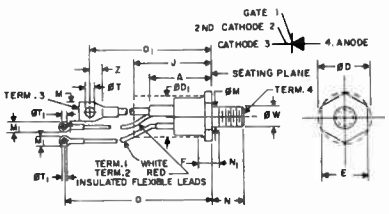


13



*DIMENSIONS SUBJECT TO CHANGE CONTACT FACTORY BEFORE COMPLETING FINAL MOUNTING DESIGNS.

14



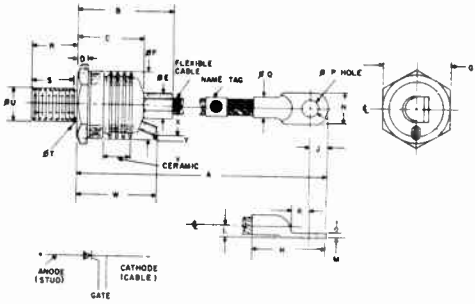
NOTES.
1. The device with exception of the hexagon thread and flexible leads lies within the cylinder diameter ØD and length J.
2. Angular orientation of these terminals with respect to hex portion is undefined. Square or radius on end of terminals is optional.
3. Length of incomplete or undercut threads.
4. Pitch diameter of ¼-16 UNF-2A (coated) threads (ASA B1.1).
5. A chamfer (or undercut) on one or both ends of hex portion is optional.
6. Maximum flat.
7. Diameter of seating surface.
8. Sealant height with lead bent 90°.
9. Dimensions should be used for estimating only.

SYMBOL	MILLIMETERS		INCHES		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	39.75	57.15	1.565	2.250	
ØD		36.65		1.443	7
$ØD_1$		30.94		1.218	1
E	30.94	31.75	1.218	1.250	
F	5.84	10.16	.230	.400	5
J		82.55		3.250	1,8
M	13.46	19.18	.530	.755	2
ØM	17.78	19.02	.700	.749	
M_1	5.46	7.62	.215	.300	2
N	26.59	27.36	1.047	1.077	1,4
N_1		3.96		.156	3
O	186.69	205.74	7.350	8.100	
O_1	186.69	205.74	7.350	8.100	
ØT	7.87	8.74	.310	.344	
$ØT_1$	3.56	3.94	.140	.155	
ØW	17.853	18.018	.7029	.7094	4
Z	8.64		.340		6

15

SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	.960	1.000	24.38	25.40	
B		2.375		60.32	
C		1.625		41.28	
D	.235	.265	5.97	6.73	
øE		.750		19.05	
øF		1.625		41.28	
G	1.605	1.640	40.77	41.66	
H	1.625	2.000	41.28	50.80	
J	.375	.438	9.52	11.12	
K	.375		9.52		
L	.250	.297	6.35	7.54	
M	.094	.125	2.39	3.18	
N		.744		18.90	
øP	.391	.422	9.93	10.72	
øQ		.562		14.27	
R	1.037	1.087	26.34	27.61	
S	.912	1.099	23.16	29.63	
øT	.660	.670	16.76	17.02	
øU					2
V					1
W		2.000		50.80	
X		.750		19.05	
Y					3

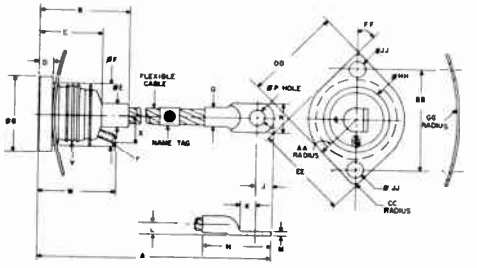
NOTES:
1. 1.000" (25.40 mm) max insulation surface creep
2. No. 16 UNF 2A
   Pitch Dia — 0.7029" (17.85 mm) min
   0.7094 (18.02 mm) max
3. Case receptacle will mate with Amp Incorporated Coaxicon plug TNC type (e.g. #329036)



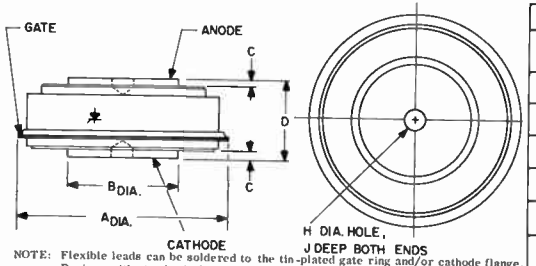
16

SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	.875	1.125	22.23	28.58	
B		2.500		63.50	
C		1.750		44.45	
D	.375	.406	8.25	9.86	
øE		.750		19.05	
øF		1.625		41.28	
G	1.865	1.885	47.37	47.88	
H	1.625	2.000	41.28	50.80	
J	.375	.438	9.52	11.12	
K	.375		9.52		
L	.250	.297	6.35	7.54	
M	.094	.125	2.39	3.18	
N		.744		18.90	
øP	.391	.422	9.93	10.72	
øQ		.562		14.27	
R					1
W		2.000		50.80	
X		.750		19.05	
Y					3
AA	1.178	1.188	29.92	30.43	4
BB	2.484	2.546	63.09	64.91	3
CC	.172	.203	4.37	5.16	3
DD	2.356	2.391	59.82	60.81	3
EE	2.356	2.391	59.82	60.81	3
FF					2,3
GG	5.500	6.500	139.70	165.10	3
øHH	1.640	1.650	41.66	41.91	3
øJJ	.370	.380	9.40	9.65	3

NOTES:
1. 1.000" (25.40 mm) max insulation surface creep
2. 45° max, 45° max.
3. Dimensions at clamp before forming to 4.000" (101.6 mm) radius
4. Case receptacle will mate with Amp Incorporated Coaxicon plug TNC type (e.g. #329036)



17



	DIMENSIONS	
	DECIMAL (INCHES)	METRIC (MM)
A	1.500 / 1.430	38.10 / 36.32
B	.752 / .744	19.101 / 18.897
C	.075 / .020	1.905 / .507
D	.625 / .500	15.875 / 12.699
H	.135 / .145	3.429 / 3.683
J	.067 / .083	1.702 / 2.108

NOTE: Flexible leads can be soldered to the tin-plated gate ring and/or cathode flange. Devices with standard, 5-inch flexible leads are available as an option.

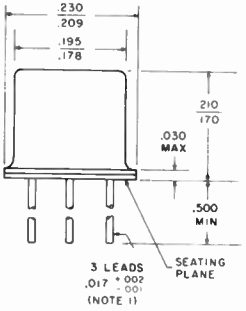
18

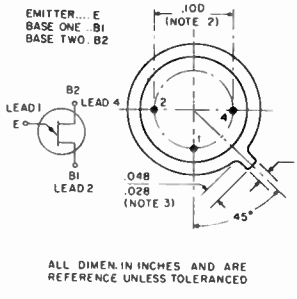
DIMENSIONS WITHIN JEDEC OUTLINE TO-18 EXCEPT FOR LEAD CONFIGURATION

NOTE 1: Lead diameter is controlled in the zone between .050 and .250 from the seating plane. Between .250 and end of lead a max of .021 is held

NOTE 2: Leads having maximum diameter (.019) measured in gaging plane .054 .001 .000 below the seating plane of the device shall be within .007 of true position relative to a maximum width tab

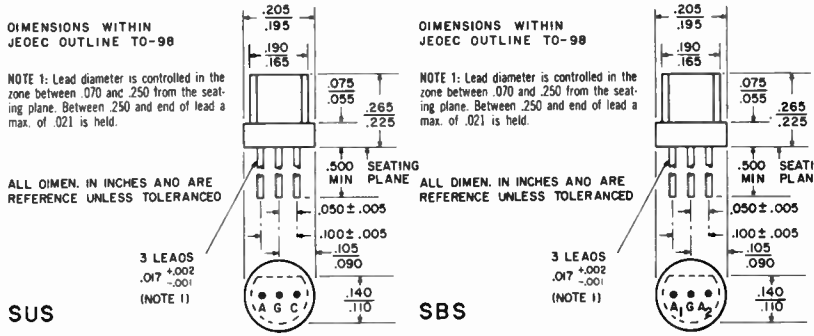
NOTE 3: Measured from max diameter of the actual device



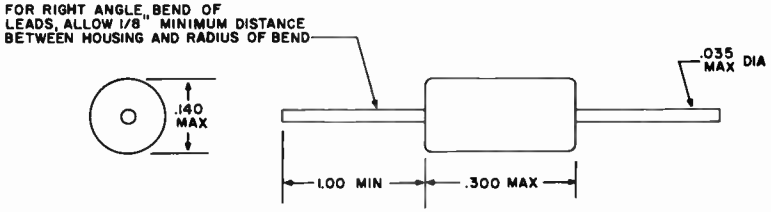


ALL DIMEN. IN INCHES AND ARE REFERENCE UNLESS TOLERANCED

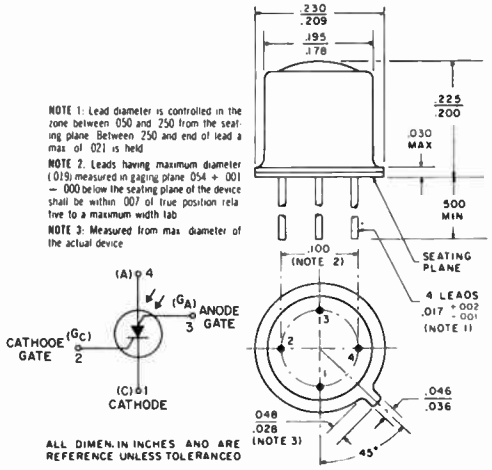
19


DIMENSIONS WITHIN JEDEC OUTLINE TO-98
NOTE 1: Lead diameter is controlled in the zone between .070 and .250 from the seating plane. Between .250 and end of lead a max. of .021 is held.
ALL DIMEN. IN INCHES AND ARE REFERENCE UNLESS TOLERANCED
3 LEADS .017 +.002 -.001 (NOTE 1)
SUS
.205 .195
.190 .165
.075 .055
.265 .225
.500 MIN
SEATING PLANE
.050 ± .005
.100 ± .005
.105
.090
.140 .110
A G C
DIMENSIONS WITHIN JEDEC OUTLINE TO-98
NOTE 1: Lead diameter is controlled in the zone between .070 and .250 from the seating plane. Between .250 and end of lead a max. of .021 is held.
ALL DIMEN. IN INCHES AND ARE REFERENCE UNLESS TOLERANCED
3 LEADS .017 +.002 -.001 (NOTE 1)
SBS
A1 G A2

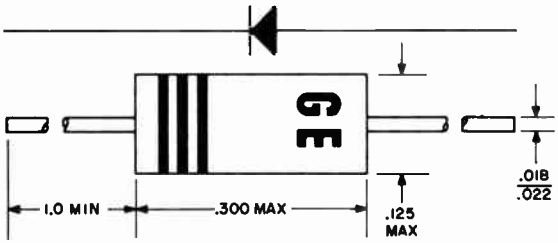
20


FOR RIGHT ANGLE BEND OF LEADS, ALLOW 1/8" MINIMUM DISTANCE BETWEEN HOUSING AND RADIUS OF BEND
.140 MAX
.035 MAX DIA
1.00 MIN
.300 MAX

21

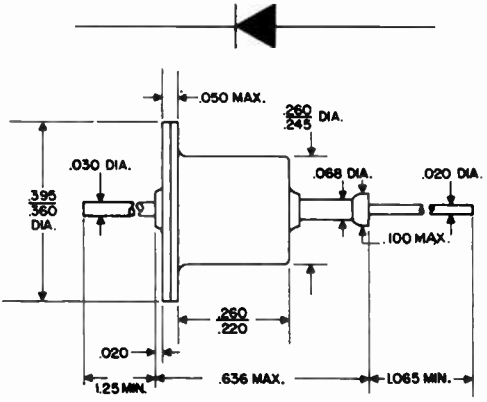

NOTE 1: Lead diameter is controlled in the zone between .050 and .250 from the seating plane. Between .250 and end of lead a max. of .021 is held
NOTE 2: Leads having maximum diameter (.019) measured in gaging plane .054 + .001 − .000 below the seating plane of the device shall be within .007 of true position relative to a maximum width tab
NOTE 3: Measured from max. diameter of the actual device
(A) 4
(GA) ANODE GATE
3
CATHODE GATE (GC)
2
(C) 1 CATHODE
ALL DIMEN. IN INCHES AND ARE REFERENCE UNLESS TOLERANCED
.230 .209
.195 .178
.225 .200
.030 MAX
.500 MIN
.100 (NOTE 2)
SEATING PLANE
4 LEADS .017 +.002 -.001 (NOTE 1)
.046 .036
.048 .028 (NOTE 3)
45°

22



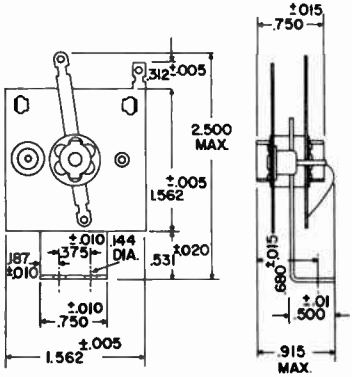
NOTES: 1. JEDEC COLOR CODED BANDS DENOTE CATHODE END
2. UNIT WEIGHT – .25 GMS

23

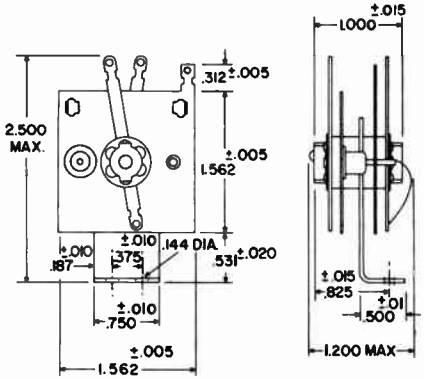


COMPLIES WITH EIA REGISTERED OUTLINE DO-3
APPROX. WEIGHT = .05 OZ.

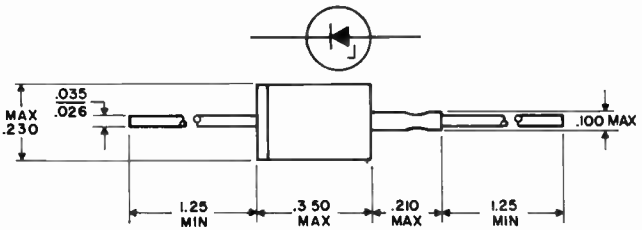
24



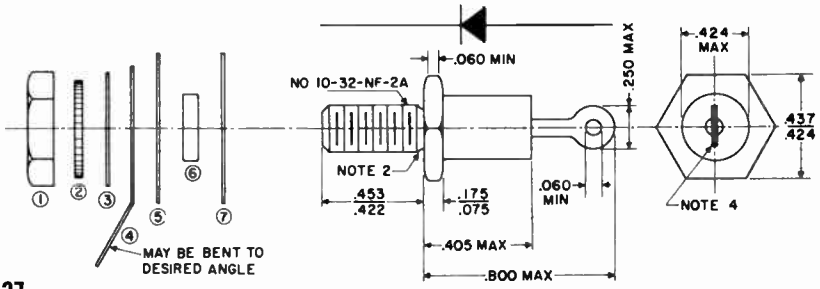
25



26



27



① 10-32 BRASS NI. PL. HEX. NUT

② LOCK WASHER (EXT.) STEEL NI. PL.

③ FLAT WASHER 7/16" O.D. .004 THK.

④ TERMINAL: .010 THK. COPPER TIN PL.

⑤ MICA WASHER .005 THK.

⑥ TEFLON WASHER .032 WALL THK.

⑦ MICA WASHER .005 THK.

NOTES:

1. UNIT MUST NOT BE DAMAGED BY TORQUE OF 15 IN. LB. APPLIED TO 10-32-NF-2B NUT ASSEMBLED ON THREAD.
2. DIA OF UNTHREADED PORTION .189 MAX. AND .169 MIN.
3. COMPLETE THREADS TO EXTEND TO WITHIN 2 1/2 THREADS OF HEAD.
4. ANGULAR ORIENTATION OF THIS TERMINAL IS UNDEFINED.
5. MAXIMUM PITCH DIAMETER OF PLATED THREADS SHALL BE BASIC PITCH DIAMETER (.1697) REFERENCE SCREW THREAD STANDARD FOR FEDERAL SERVICES 1957 HANDBOOK H2B 1957 PI.

COMPLIES WITH EIA REGISTERED OUTLINE DO-4

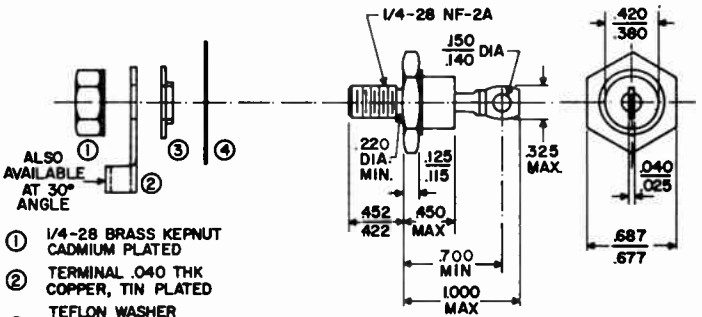
APPROX WEIGHT = .15 OZ

28

NOTE: MICA WASHER IN MOUNTING KIT MAY ADD UP TO 2.5° C/WATT THERMAL RESISTANCE STUD TO AMBIENT
UNIT WEIGHT .5 OZ.

DIRECTION OF EASY CONVENTIONAL CURRENT FLOW
IN2154–IN2160; IN248A–IN250A; IN248B–IN250B

DIRECTION OF EASY CONVENTIONAL CURRENT FLOW
IN2154R–IN2160R; IN248R–IN250R
IN248RA–IN250RA; IN248RB–IN250RB



① 1/4-28 BRASS KEPNUT CADMIUM PLATED

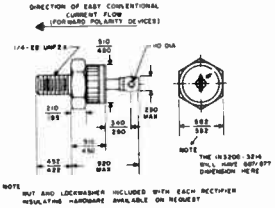
② TERMINAL .040 THK COPPER, TIN PLATED

③ TEFLON WASHER .025 WALL THK. .032 SHOULDER THK.

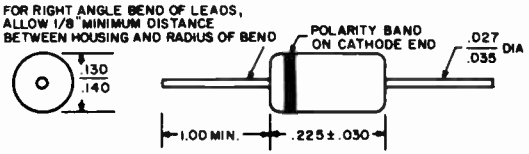
④ MICA WASHER .005 THK.

COMPLIES WITH EIA REGISTERED OUTLINE DO-5

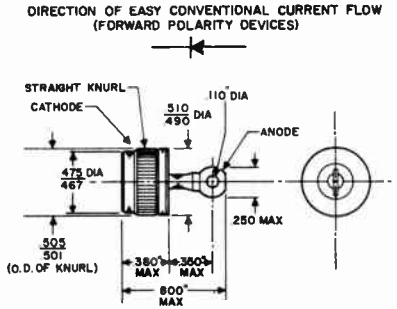
29


DIRECTION OF EASY CONVENTIONAL CURRENT FLOW (FORWARD POLARITY DEVICES)
NOTE
NUT AND LOCKWASHER INCLUDED WITH EACH RECTIFIER
INSULATING HARDWARE AVAILABLE ON REQUEST

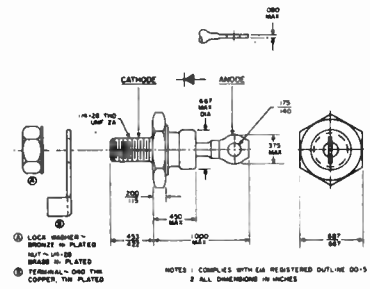
30


FOR RIGHT ANGLE BEND OF LEADS, ALLOW 1/8" MINIMUM DISTANCE BETWEEN HOUSING AND RADIUS OF BEND
POLARITY BAND ON CATHODE END
.027 / .035 DIA
.130 / .140
1.00 MIN.
.225 ± .030

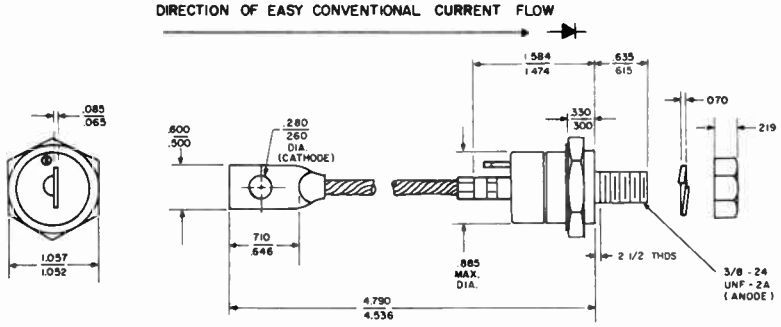
31


DIRECTION OF EASY CONVENTIONAL CURRENT FLOW (FORWARD POLARITY DEVICES)
STRAIGHT KNURL
CATHODE
.110" DIA
.510 / .490 DIA
ANODE
.475 DIA / .467
.250 MAX
.505 / .501 (O.D. OF KNURL)
.380" MAX
.380" MAX
.800" MAX

32

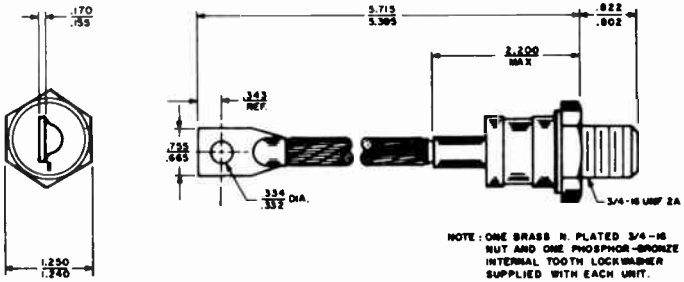

CATHODE
ANODE
NOTES : 1 COMPLIES WITH EIA REGISTERED OUTLINE DO-5
2 ALL DIMENSIONS IN INCHES

33



CONFORMS TO JEDEC OUTLINE DO-8

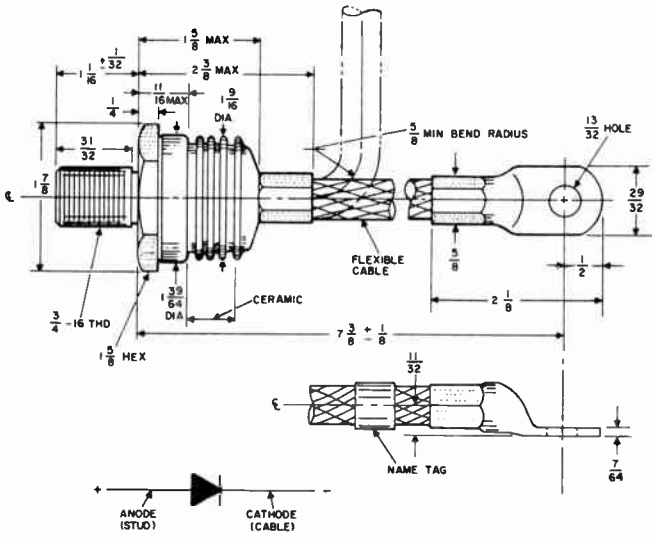
34



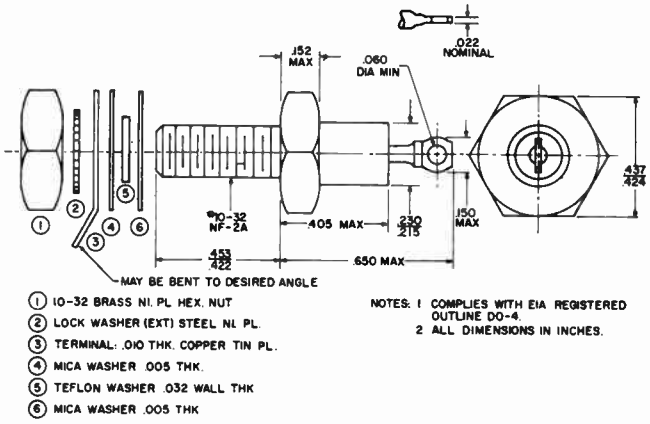
A90, IN3736 SERIES STUD CATHODE

A91, IN3736R SERIES STUD ANODE

35



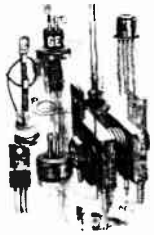
36



(1) 10-32 BRASS NI. PL HEX. NUT
(2) LOCK WASHER (EXT) STEEL NI PL.
(3) TERMINAL: .010 THK. COPPER TIN PL.
(4) MICA WASHER .005 THK.
(5) TEFLON WASHER .032 WALL THK
(6) MICA WASHER .005 THK

NOTES: 1 COMPLIES WITH EIA REGISTERED OUTLINE DO-4.
2 ALL DIMENSIONS IN INCHES.

22 APPLICATION AND SPECIFICATION LITERATURE; SALES OFFICES



General Electric silicon controlled rectifier and rectifier diode Application Notes and Specification Sheets provide greater detail on the application data and condensed device specifications in this Manual. Copies of the literature listed in Section 22.1 and as indicated in Section 22.2 may be ordered by Publication Number from:

General Electric Company
Distribution Services
Bldg. 6, Room 208
1 River Road,
Schenectady, New York 12305

However, those Manuals listed as ETR 3296, ETR 3875A or ETR 3960 must be ordered from:

General Electric Company
Department B
3800 North Milwaukee Avenue,
Chicago, Illinois 60641

Section 22.3 lists other General Electric Departments furnishing related electrical and electronic components.

22.1 APPLICATION NOTES

Publication Number 200.0, "Semiconductor Applications," contains abstracts of application notes, article reprints, technical papers and application manuals listed in the following sub-sections.

22.1.1 General Applications for Power Semiconductors

Publication Number	*Title*
90.16	Silicon Controlled Switches
90.21	How to Suppress Rate Effect in PNPN Devices
90.55	Semiconductor Strain Sensors
90.57	Using the Silicon Bilateral/Unilateral Switch
90.58	Reversible Ring Counter Utilizing the Silicon Controlled Switch
200.1	Characteristics of Common Rectifier Circuits

Publication Number	*Title*
200.5	General Electric Selenium Thyrector Diodes
200.8	Accommodating Inrush Currents With Silicon Controlled Rectifiers
200.9	Power Semiconductor Ratings Under Transient and Intermittent Loads
200.10	Overcurrent Protection of Semiconductor Rectifiers
200.15	Turn-Off Time Characterization and Measurement of Silicon Controlled Rectifiers
200.19	Using Low Current SCR's
200.27	An Introduction to the Controlled Avalanche Silicon Rectifier
200.28	The Rating of SCR's When Switching Into High Currents
200.30	Capacitor Input Filter Design With Silicon Rectifier Diodes
200.32	A Variety of Mounting Techniques for Press-Fit SCR's and Rectifiers
200.34	The Light Activated SCR
200.35	Triac Control for AC Power
200.36	The Solid State Thyratron
200.37	Increasing Power and Frequency with GE's New Line of High-Speed SCR's and Power Diodes
200.38	Application of Fast Recovery Rectifiers
200.39	The Series Connection of Rectifier Diodes
200.42	Commutation Behavior of Diffused High-Current Rectifier Diodes
201.19	RF Filter Considerations for Triac and SCR Circuits
450.37	Transistor Manual, 7th Edition (ETR 3296, $2.00)
ETR 3875A	Silicon Controlled Rectifier Manual, 4th Edition ($3.00)
660.1	Silicon Controlled Rectifier—Interview With E. E. VonZastrow
660.10	SCR's Break the Frequency Barrier
660.12	Better Utilization of SCR Capability with AC Inductive Loads
660.13	The Rating and Application of SCR's Designed for Power Switching at High Frequencies
660.14	Basic Magnetic Functions in Converters and Inverters Including New Soft Commutation
671.1	Economy Power Semiconductor Applications
CP65-937	A Program Report on Solid State Appliance Controls GE
——	Electronic Components Hobby Manual (ETR 3960, $1.50)

22.1.2 Silicon Controlled Rectifier and Other Thyristor Circuits

200.14	The Silicon Controlled Rectifier in Lamp Dimming and Heating Control Service
200.18	Fluorescent Lamp Dimming With SCR's and Associated Semiconductors

Publication Number	*Title*
200.21	Three-Phase SCR Firing Circuits For DC Power Supplies
200.31	Phase Control of SCR's With Transformer and Other Inductive AC Loads
200.33	Regulated Battery Chargers Using the Silicon Controlled Rectifier
200.40	Series Operation of SCR's
200.41	Simple Circuits for Triggering SCR's Into Fast-Rising Load Currents
200.43	Solid State Control for DC Motors Provides Variable Speed With Synchronous-Motor Performance
200.44	Speed Control for Shunt-Wound Motors
200.45	Temperature Controls Incorporating Zero-Voltage Switching
200.46	AC Voltage or Current Regulator Featuring Closed-Loop Feedback Control
200.47	Speed Control for Universal Motors
200.48	Flashers, Ring Counters and Chasers
200.49	A Low-Cost, Ultrasonic-Frequency Inverter Using A Single SCR
201.1	A Plug-In Speed Control For Standard Portable Tools and Appliances
201.5	A High-Frequency Inverter Circuit
201.6	Touch Switch or Proximity Detector
201.9	Precision Temperature Controller
201.10	Auto, Boat or Barricade Flasher
201.11	Time-Delayed Relay
201.12	500 Watt AC Line Voltage and Power Regulator
201.13	Universal Motor Control With Built-In Self-Timer
201.14	Automatic Liquid-Level Control
201.15	Solid-State Control for Electric Blankets
201.16	Fan Motor Speed Control—"Hi-Intensity" Lamp Dimmer
201.17	Sequential Turn Signal System for Automobiles
201.18	High-Voltage Power Supply for Low-Current Applications
201.20	Proportional Zero-Voltage Switching Temperature Control
201.21	On-Off Zero-Voltage Switching Temperature Control
660.7	RFI-Less Switching with SCR's

22.1.3 Unijunction Applications

90.10	The Unijunction Transistor Characteristics and Applications
90.12	Unijunction Temperature Compensation
90.19	Unijunction Frequency Divider

22.1.4 Test Circuits

201.3	Portable SCR and Silicon Rectifier Tester

22.2 SPECIFICATION SHEETS

The device specification sheets referred to on the condensed specifications of Chapter 21, and others that may be mentioned in this Manual, may be ordered by Publication Number from:

General Electric Company
Distribution Services
Bldg. 6, Room 208
1 River Road,
Schenectady, New York 12305

22.3 RELATED GENERAL ELECTRIC DEPARTMENTS

The Semiconductor Products Department would like to remind its readers of the great variety of parts and services that our sister departments in General Electric can furnish to meet your SCR circuit needs. Among them are:

—SCR Capacitors for phase control and inverter commutation duty (GE Capacitor Dept., Hudson Falls, N.Y.)

—Transformers and chokes for inverters and power supply needs (GE Specialty Transformer Dept., Fort Wayne, Ind.)

—A complete family of GE Sensors and control elements:

- Cadmium sulfide cells and magnetic reed switches (GE Tube Dept., Owensboro, Ky.)
- Thermistors and magnetic materials (GE Metallurgical Products Dept., Edmore, Mich.)

—A complete family of high-reliability lamps for activation of light-activated SCR's (GE Miniature Lamp Dept., Cleveland, Ohio)

—Silicone potting and joint compounds (GE Silicone Products Dept., Waterford, N.Y.)

—And, of course, the industry's most complete line of motors and other related electrical and electronic equipment

22.4 GENERAL ELECTRIC SALES OFFICES

All products of the Capacitor, Metallurgical Products, Miniature Lamp, Semiconductor Products, Specialty Transformer and Tube Departments are sold through General Electric's Electronic Components Sales Operation (ECSO) to original equipment manufacturers (OEM's) and distributors of electrical/electronic equipment and components. ECSO's OEM Sales Offices are listed below:

Alabama: Huntsville 35801
3322 Memorial Parkway S.
Suite 13, Area Code: 205
881-3131

Arizona:	Phoenix 85012 Suite 712 Guaranty Bank Bldg. 3550 N. Central Ave. Area Code: 602 264-1751
California:	Los Angeles 90064 11840 W. Olympic Blvd. Area Code: 213 479-7763 272-8566
	Redwood City 94063 555 Veterans Blvd. Area Code: 415 369-7151
Colorado:	Denver 80201 201 University Blvd. P.O. Box 2331 Area Code: 303 388-5771
Connecticut:	Bridgeport 06602 1285 Boston Ave. Bldg. 21-ES Area Code: 203 334-1012
District of Columbia:	Washington 20005 777-14th St., NW Area Code: 202 393-3600
Florida:	Orlando 32806 14 W. Gore St. Area Code: 305 425-8634
	Tampa 33609 2106 S. Lois Ave. Area Code: 813 877-8311

Illinois:	Chicago 60641 3800 N. Milwaukee Ave. Area Code: 312 777-1600
Indiana:	Ft. Wayne 46806 3606 S. Calhoun St. Area Code: 219 744-2346
	Indianapolis 46208 3750 N. Meridian St. Area Code: 317 923-7221
Iowa:	Cedar Rapids 52403 210 Second St., SE Area Code: 319 364-9149
Massachusetts:	Wellesley 02181 1 Washington St. Area Code: 617 237-2050
Michigan:	Southfield (Detroit) 48076 17220 W. Eight Mile Rd. Area Code: 313 444-4340 (Detroit) 356-1075 (Southfield)
Minnesota:	Minneapolis 55442 4900 Viking Dr. Area Code: 612 927-5458
Missouri:	Kansas City 64199 911 Main St. Area Code: 816 221-4033
New Jersey:	Clifton 07014 200 Main Ave. Area Code: 201 472-8100

New York:	Buffalo 14240 P.O. Box 1087 625 Delaware Ave. Area Code: 716 883-9210
	Great Neck, L.I. 11021 425 Northern Blvd. Area Code: 516 HN 6-8800
	Syracuse 13201 Bldg. 7, Electronics Park Area Code: 315 456-3063 (Gov't Programs)
	North Syracuse 13212 Northern Concourse Off. Bldg. Area Code: 315 456-3412
North Carolina:	Charlotte 28201 129 W. Trade St. P.O. Box 1969 Area Code: 704 375-5571
Ohio:	Cleveland 44117 25000 Euclid Ave. Area Code: 216 266-2900
	Dayton 45429 P.O. Box 2143 Kettering Branch Area Code: 513 298-0311
Oklahoma:	Okahoma City 73112 3022 Northwest Expressway May-Ex Bldg., Rm. 412 Area Code: 405 943-9015
Pennsylvania:	Philadelphia 19102 3 Penn Center Plaza Area Code: 215 568-1800

	Pittsburgh 15220 875 Greentree Rd. 3 Parkway Center Area Code: 412 921-4134
Tennessee:	Memphis 38104 1420 Union Ave. Area Code: 901 272-9641
Texas:	Dallas 75205 4447 N. Central Expressway Area Code: 214 521-1931
Virginia:	Lynchburg 24501 P.O. Box 4217 (Carroll Ave. Plant) Area Code: 703 846-7311
Washington:	Seattle 98188 P.O. Box 6100 112 Andover Park East Tukwila Area Code: 206 CH 4-7750
Wisconsin:	Milwaukee 53202 615 E. Michigan St. Area Code: 414 271-5000

In Canada, address inquiries to:

Canadian General Electric Co.
189 Dufferin St.
Toronto, Ontario, Canada
Area Code: 416
534-6311

Inquiries from outside continental United States, excluding Hawaii and Alaska, should be sent to:

Electronic Component Sales
IGE Export Division
159 Madison Ave.
New York, N.Y. 10016
Area Code: 212
PLaza 1-1311

Also, your authorized full-line General Electric Semiconductor Distributor is generally listed in the classified section of local telephone directories.

APPLICATION INDEX

The circuits referred to in the following figure numbers are intended as a starting point for the equipment designer in achieving the detailed requirements of his application. Since these circuits are not necessarily "ultimate" for every application, it is hoped the imaginative designer will use them simply as a jumping-off point for his own development. Likewise, many of these circuits can be used for other functions besides those mentioned in the text. As a guide to some of the various thyristor circuits for accomplishing specific tasks, here is a tabulation of figures in this manual classified by possible application (please note that these are *Figure* numbers and not section or paragraph numbers):

Applications	For Basic Circuit Possibilities See Figure Number
AC Regulated Supplies	8.9, 9.16, 9.25, 9.27, 9.30, 9.31, 9.32, 9.39, 10.11, 10.12, 11.3.7, 12.15, 12.18, 12.22, 12.25
AC Static Switches	4.18, 4.24, 7.5, 7.6, 7.10, 8.1, 8.2, 8.3, 8.4, 8.5, 8.6, 8.7, 8.8, 8.11, 8.21, 8.30, 10.15, 10.16, 12.16, 12.17, 13.4, 13.11
Appliance Controls	4.20, 7.5, 7.6, 7.9, 7.10, 8.1, 8.4, 8.5, 8.11, 8.24, 8.26, 8.30, 9.10, 9.24, 9.30, 9.31, 10.1, 10.3, 10.4, 10.6, 10.11, 10.14, 10.15, 10.16, 12.15, 12.16, 12.25
Battery Chargers	4.22, 8.12, 9.35, 9.38, 11.2.12, 12.23, 14.8
Circuit Breakers	5.9, 8.1, 8.17, 8.18, 8.19
Current Regulators	8.18, 8.27, 9.25, 9.30, 9.35, 11.3.3, 11.3.4, 12.18, 12.22, 14.8
DC Static Switches	5.8, 5.9, 5.14, 8.13, 8.14, 8.17, 8.19, 8.20, 8.22, 8.24, 8.25, 8.26, 8.27, 8.30, 13.4
DC to AC Inverters	4.39, 4.40, 5.5, 5.6, 11.2.1, 11.2.5, 11.2.7, 11.4.1
DC to DC Converters	5.5, 5.6, 5.7, 5.9, 5.10, 5.12, 5.14, 11.2.9, 11.2.12
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Decade Counters	8.22, 8.23
Electric Vehicle Drives	5.10, 5.12, 5.14, 11.2.7, 11.2.9, 11.2.12
Electronic Crowbars	8.16, 8.19
Exciters for Motors and Generators	4.20, 4.22, 8.15, 9.10, 9.25, 9.26, 9.35, 9.38, 10.8, 10.14, 12.23
Flashers	5.12, 7.8, 8.7, 8.11, 8.13, 8.20, 8.21, 8.22, 13.9
Firing Circuits	(see Trigger Circuits)
Flip Flops	4.39, 4.40, 5.8, 7.8, 8.14, 8.20, 8.21, 8.22, 13.8
Frequency Changers	4.40, 7.8, 9.27, 11.2.1, 11.2.7, 11.3.7, 11.4.1, 11.4.5, 11.4.7
Ignitron Firing	8.11, 11.4.4
Indicator Circuits	8.4, 8.22, 8.23, 8.32, 8.33
Lamp Dimmers	4.20, 4.21, 4.23, 4.38, 7.9, 7.10, 9.10, 9.12, 9.13, 9.14, 9.15, 9.17, 9.26, 9.27, 9.29, 12.22
Latching Relays	8.4, 8.14, 8.25, 8.26
Logic Circuits	8.22, 8.23, 13.8, 13.9, 13.10
Motor Controls and Drives—DC	4.22, 5.10, 5.12, 5.14, 8.11, 8.13, 9.10, 9.25, 9.26, 9.29, 9.35, 9.38, 10.1, 10.3, 10.4, 10.5, 10.6, 10.8, 10.9, 10.14, 11.2.9, 12.23

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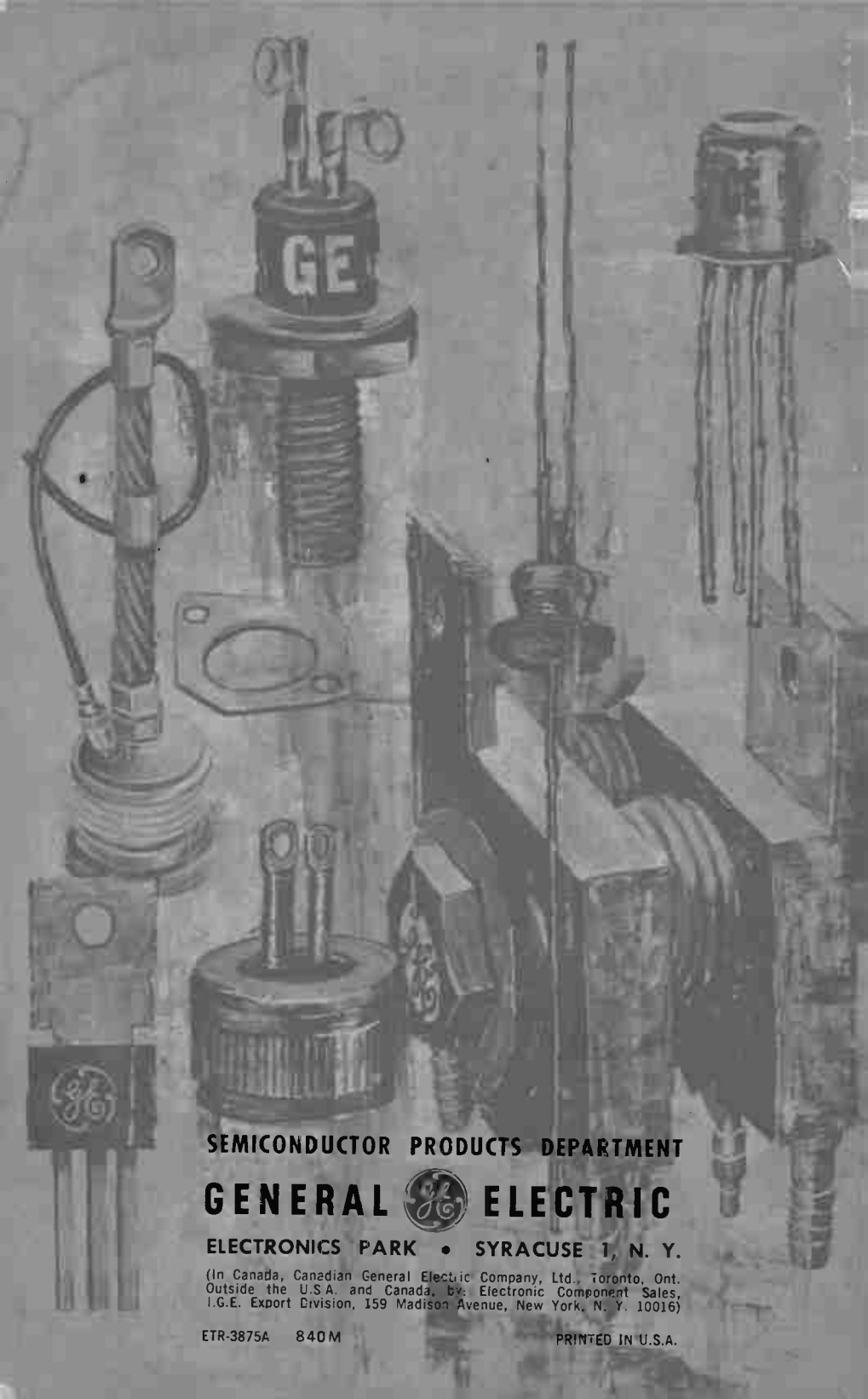

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I.G.E. Export Division, 159 Madison Avenue, New York, N. Y. 10016)

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