

100W Dual USB-C PFC+QR Charger Reference Design

Technical Manual



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Table of Contents

1. Scope and Purpose	3
2. Introduction.....	3
2.1 System Block Diagram.....	3
2.2 System Specifications.....	5
2.3 Reference Design Board	6
3. System Design Considerations.....	6
3.1 PFC Stage Design	6
3.2 QR Flyback Stage Design	9
4. GaN Transistor Value Propositions.....	11
5. Test Results.....	14
5.1 Test Equipment.....	14
5.2 Efficiency	14
5.3 Standby Power	16
5.4 Electromagnetic Interference (EMI).....	16
5.5 Thermal.....	18
5.6 Electrical Waveforms	20
6. Conclusion.....	23
Appendix – How to take out PCBA from the Case	24
References	25

1. Scope and Purpose

This document provides a comprehensive functional description and guide to designing with the 100W dual USB-C AC/DC PD charger reference design (part number: GS-EVM-CHG-100WPFCQR-GS1) based on the 650V Gallium Nitride (GaN) transistor from GaN Systems. It describes the system operation and covers technical aspects essential to the design process, including calculation of key components as well as additional design documents (schematics, layout, and BOM). Test results and waveforms are also included in this document.

2. Introduction

The 100W dual USB-C PD GaN-based charger reference design provides a cased turn-key solution with the following key features:

- High power density up to 16.3W/in³ (100cc) and high efficiency above 92.5%
- Dual USB-C ports with smart power distribution
- Cost effective topologies with PFC+QR Flyback
- Passes EN55023 Class B with >6dB margin for conduction and radiation EMI
- Meets IEC 62368-1 touch temperature requirement
- Meets IEC 61000-3-2 THD requirement with high power factor
- Supports most PD protocols including PD3.0/PD2.0, PPS, QC4.0+/QC4.0/QC3.0/QC2.0, AFC, FCP, SCP, PE2.0/PE1.1, SFCP, low voltage direct charging, and BC1.2 DCP
- Comprehensive system protections such as OVP, OCP, SCP, and open loop
- Exceeds CoC Ver5 2019/1782 efficiency standard requirement
- Folding Prong

2.1 System Block Diagram

As shown in Figure 1, the reference design includes three main power conversion stages: Power Factor Correction (PFC), Quasi-Resonant (QR) Flyback, and Buck DC/DC. The primary side and secondary side include:

1. On the primary side, there is a front-end Critical Mode (CrM) PFC stage to achieve high power factor and meet the IEC61000-3-2 THD standard. A galvanic isolation synchronous rectification (SR) QR Flyback is used to achieve 22V DC Vbus output.

- Both PFC and QR Flyback stages use one 650V, 150mΩ GaN transistor (part number: **GS-065-011-1-L**) for efficiency and power density improvements.
2. On the secondary output side, two independent synchronous buck converters realize dual USB-C ports outputs. A dedicated microcontroller unit is used for smart power distribution on each USB-Cx and operation mode management.

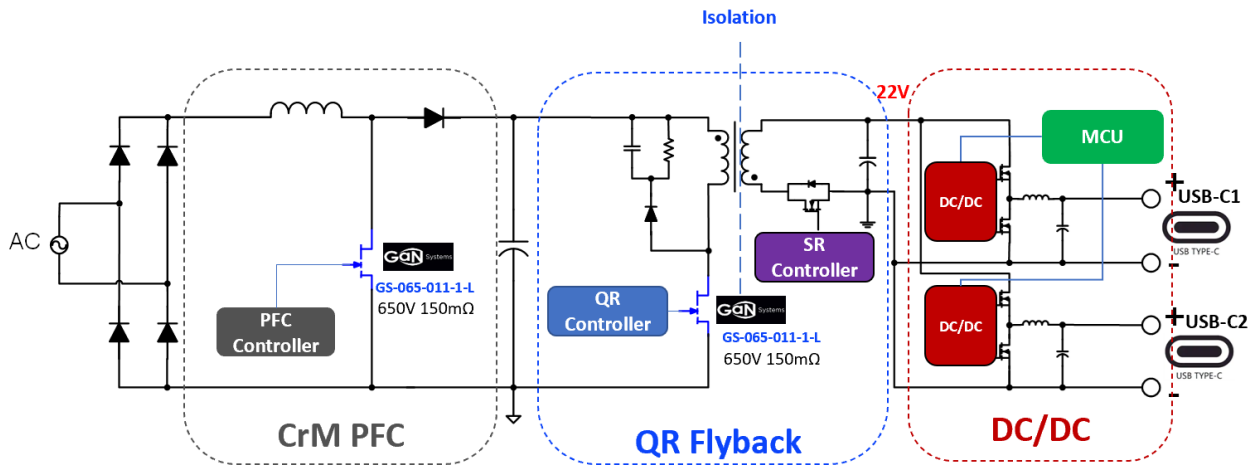


Figure 1. Simplified system block diagram for GS-EVM-CHG-100WPFCQR-GS1 reference design

Figure 2 shows the output power distribution configurations for USB-Cx. By sensing the output current and voltage, the power of the dual USB-C can be distributed according to the plug-in end devices (e.g., laptop or cell phone) and its related protocols. The descriptions are as follows:

- **Signal USB-C output:** the USB-C1 or USB-C2 can support maximum power up to the 100W (20V/5A) maximum output.
- **Dual USB-C outputs:** USB-Cx ports have the flexibility to support dual laptops with 45W maximum power each, dual cell phones with 30W maximum power each, or one laptop with 65W maximum power and one cell phone with 35W maximum power.

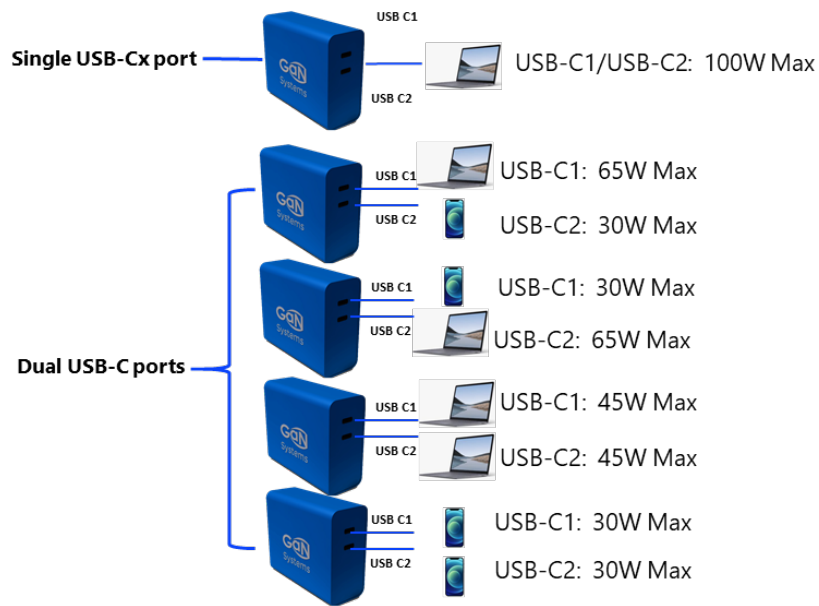


Figure 2. Power distribution configuration for the USB-Cx

2.2 System Specifications

Table 1 summarizes the key specification and performance for this 100W GaN-based charger reference design.

Table 1. Key parameters and performance of GS-EVM-CHG-100WPFCQR-GS1 reference design

Parameter	Value
Input AC Voltage (V_{in})	90-264 V_{rms}
Input Frequency Range	50/60 Hz
Max. Output Power	100W
Output Voltage and Current	5V3A, 9V3A, 12V3A, 15V3A, 20V5A
Max. Output Current	5A
PD Protocols	PD3.0, PPS, QC4.0+, BC1.2 etc.
Performance	Specification
Cased Power Density	16.3 W/in ³ (100cc)
Board Dimension with Case	60mmX60mmX28mm (2.4inchX2.4inchX1.1inch)
Peak Efficiency	>92.5%
Average Efficiency	CoC V5 2019/1782
Standby Power	<200mW
Touch Temperature @20V/5A	IEC 62368-1
EMI Standard	EN55032 Class B
System Protections	OVP, OCP, SCP, Open Loop

2.3 Reference Design Board

Figure 3 shows the PCBA photo of this reference design which uses a generic 2-layer 2Oz FR4 PCB with common industrial components. Two motherboards are included: Figure 3a shows a primary side motherboard which includes an input EMI filter, bridge diode, PFC stage, and QR Flyback's primary side. Figure 3b shows a secondary side motherboard which includes QR Flyback's secondary side, Buck DC/DC, and two-piece USB-C PD daughter boards.

The reference design board also includes a plastic case, copper shielding, and thermal interface material (TIM) for heat spread and EMI purposes.

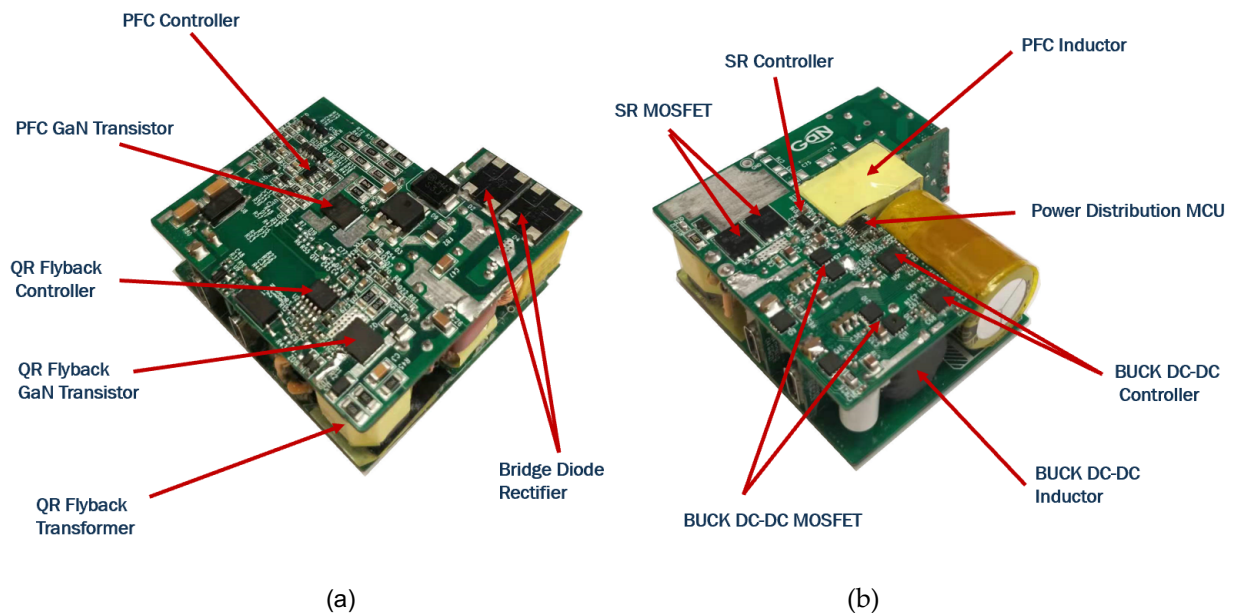


Figure 3. PCBA photos for GS-EVM-CHG-100WPFCQR-GS1 reference design

3. System Design Considerations

3.1 PFC Stage Design

The PFC circuit shapes the input current of the power supply to maximize the real power available from the mains. In addition, it is important to have the PFC circuit comply with low total harmonic distortion (THD) regulatory requirements such as IEC61000-3-2. The ON Semiconductor NCP1622 is used as the PFC controller which is based on a Valley Synchronized Frequency Fold-back (VSFF) methodology with valley switching.

The traditional PFC pre-regulator topology has a fixed output DC voltage (typical 390V), which is higher than the maximum peak AC line voltage. With a fixed DC voltage, the efficiency could be dropped at low line AC input (e.g., 90V~115Vac) due to the larger input and output voltage difference and that the PFC stage must boost DC voltage up to 390V. To improve the efficiency especially at low line AC input, a Boost follower circuit is used so that the DC voltage is linearly following with the input AC peak voltage.

Table 2 lists the design parameters for a PFC stage design. These parameters are used in further calculations of the main components.

Table 2. Key specification of PFC stage for GS-EVM-CHG-100WPFCQR-GS1 reference design

Parameter	MIN	TYP	MAX	UNITS
Low line AC Voltage, V_{rms_LL}	90			V
High line AC Voltage, V_{rms_HL}			264	V
Input AC Frequency, f_{line}	47	60	63	Hz
Maximum on-time at low line 90Vac, $T_{on_max, LL}$		5.6		μs
Output DC voltage at low Line 90Vac $V_{pfc_out_LL}$		250		VDC
Output DC voltage at high Line 264Vac $V_{pfc_out_HL}$		390		VDC
Output PFC Power, P_{pfc_out}		110		W
Target Efficiency, η_{pfc}		97.5		%
Minimum switching frequency	65			kHz

At low line 90V AC input, the peak current value of inductance $I_{pfc_pk_LL}$ is:

$$I_{pfc_pk_LL} := 2\sqrt{2} \cdot \frac{P_{pfc_out}}{\eta_{pfc} \cdot V_{rms_LL}} = 3.546A$$

The PFC inductance L_{pfc} is calculated based on the maximum on-time at low line 90V input:

$$L_{pfc} := \frac{\sqrt{2} V_{rms_LL} \cdot T_{on_max_LL}}{I_{pfc_pk_LL}} = 2.01 \times 10^{-4} H$$

Hence, the inductance $L_{pfc}=200\mu\text{H}$ is chosen in the PFC inductor design. The off-time at low line ($T_{pfc_off_LL}$) and variable switching frequency (F_{pfc_LL}) can be calculated as the below equation, and the C_{pfc_oss} is the equivalent parasitic capacitance of the PFC inductor and transistor, here C_{pfc_oss} is equal to 20pF:

$$T_{pfc_off_LL}(\varphi) := L_{pfc} \cdot \frac{I_{pfc_pk_LL} \cdot \cos(\varphi)}{V_{pfc_out_LL} - \sqrt{2} \cdot V_{rms_LL} \cdot \cos(\varphi)}$$

$$F_{pfc_LL}(\varphi) := \frac{1}{T_{pfc_on_LL} + T_{pfc_off_LL}(\varphi) + \pi \cdot \sqrt{L_{pfc} \cdot C_{pfc_oss}}}$$

The current and switching frequency at 90V AC input within a half line frequency cycle is plotted in Figure 4. The minimum switching frequency happens at peak voltage with around 88kHz.

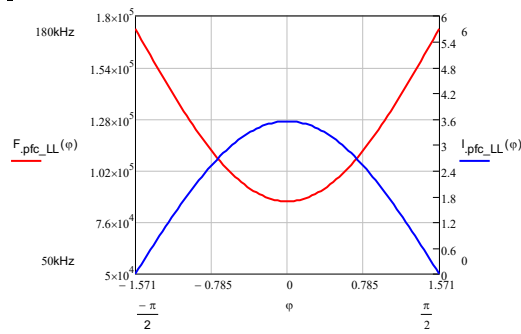


Figure 4. PFC current and switching frequency at 90V AC input

At high line 264V AC input, the peak current value of inductance $I_{pfc_pk_HL}$ is:

$$I_{pfc_pk_HL} := 2\sqrt{2} \cdot \frac{P_{pfc_out}}{\eta_{pfc} \cdot V_{rms_HL}} = 1.209\text{A}$$

The off-time at high line ($T_{pfc_off_HL}$) and variable switching frequency (F_{pfc_HL}) at half line frequency cycle can be calculated as below:

$$T_{pfc_off_HL}(\varphi) := L_{pfc} \cdot \frac{I_{pfc_pk_HL} \cdot \cos(\varphi)}{V_{pfc_out_HL} - \sqrt{2} \cdot V_{rms_HL} \cdot \cos(\varphi)}$$

$$F_{pfc_HL}(\varphi) := \frac{1}{T_{pfc_on_HL} + T_{pfc_off_HL}(\varphi) + \pi \cdot \sqrt{L_{pfc} \cdot C_{pfc_oss}}}$$

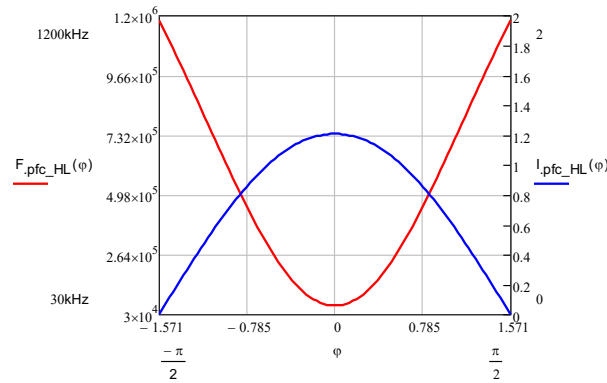


Figure 5. PFC current and switching frequency at 264V AC input

The current and switching frequency at 264V AC input within a half line frequency cycle is plotted in Figure 5. The minimum switching frequency happens at peak voltage with 65kHz.

For the PFC inductor calculation, the turns of inductor can be calculated according to peak current at low line 90V AC input. The maximum flux density ΔB is set at 0.3T for the core loss consideration.

The EQ20 3C95 Core is chosen with effective area $A_e=60\text{mm}^2$. Based on the below calculation, the turns $N_{pfc}=40$ is selected with $25 \times 0.1\text{mm}$ Litz wire.

$$N_{pfc} := \frac{L_{pfc} \cdot I_{pfc_pk_LL}}{\Delta B \cdot A_e} = 39.794$$

3.2 QR Flyback Stage Design

The ON Semiconductor NCP1343 is used as a Quasi-Resonant Flyback Controller with Power Excursion Mode (PEM). With this PEM, the flyback operates at CCM mode for load transient from light load to full load before PFC start up. It can support 2x power load transient and avoids transformer saturation with a small bulk capacitor, thus minimizing the size of the transformer and bulk capacitor.

Table 3 lists the design goal parameters for a QR Flyback stage. These parameters are used in further calculations of the main components.

Table 3. Key specification of QR Flyback stage for GS-EVM-CHG-100WPFCQR-GS1 reference design

Parameter	MIN	TYP	MAX	UNITS
Low Input DC Voltage, V_{in_min}	210			V
High Input DC Voltage, V_{in_max}			390	V
Output Power, P_{out}		110		W
Output voltage, V_{out}		22		V
Frequency at low DC input and full load, F_{sw_LV}		140		kHz
Output synchronous rectification forward voltage, V_f		0.5		V
RCD Clamping coefficient, k_c		1.1		
Drain to source Max voltage, V_{DSmax}		580		V
Efficiency, η		94%		

The QR Flyback transformer turns ratio N_{ps} is calculated:

$$N_{ps} := \frac{k_c \cdot (V_{out} + V_f)}{[(V_{DSmax}) - V_{os} - V_{in_max}]} = 0.14$$

The peak current I_{pk_LV} at low input DC voltage can be calculated as the below and the equivalent parasitic capacitor C_{oss} is equal to 80pF:

$$I_{pk_LV} := \frac{2 \cdot P_{out}}{\eta} \cdot \left(\frac{1}{V_{in_min}} + \frac{N_{ps}}{V_{out} + V_f} \right) + \pi \sqrt{\frac{2 \cdot P_{out} \cdot C_{oss} \cdot F_{sw_LV}}{\eta}} = 2.742A$$

The QR Flyback transformer inductance L_p can be calculated as the following equation and the transformer $L_p=220\mu H$ is chosen according to the below equation:

$$L_p := \frac{2P_{out}}{I_{pk_LV}^2 \cdot \eta \cdot F_{sw_LV}} = 2.256 \times 10^{-4} H$$

Choosing the transformer core with RM8 3C95 ferrite core material with the effective area $A_e=63mm^2$, the primary turns N_p can be calculated assuming maximum flux density $\Delta B=0.26T$:

$$N_p := \frac{L_p \cdot I_{pk_LV}}{\Delta B \cdot A_e} = 36.269$$

So, choosing $N_p=36Ts$ and secondary turns $N_s=N_p \cdot N_{ps} \approx 5$, the auxiliary winding N_{aux} is 5Ts per the below equation at $V_{cc}=21V$:

$$N_{aux} := \frac{N_s \cdot (V_{CC} + 0.7V)}{V_{out} + V_f} = 4.93$$

At high input voltage, the switching frequency at full load F_{sw_HV} and peak current I_{pk_HV} can be deduced by the two equations below:

$$L_p := \frac{2P_{out}}{I_{pk_HV}^2 \cdot \eta \cdot F_{sw_HV}}$$

$$I_{pk_HV} := \frac{2 \cdot P_{out}}{\eta} \cdot \left(\frac{1}{V_{in_max}} + \frac{N_{ps}}{V_{out} + V_f} \right) + \pi \sqrt{\frac{2 \cdot P_{out} \cdot C_{OSS} \cdot F_{sw_HV}}{\eta}}$$

The switching frequency and peak current at high input voltage can be obtained $F_{sw_HV}=190\text{KHz}$ and $I_{pk_HV}=2.4\text{A}$.

4. GaN's Value Propositions

Figure 6 shows a typical one switching cycle steady state V_{ds} and I_{ds} waveforms for CrM PFC and QR Flyback. Although both PFC and QR Flyback achieve a valley switching turn-on to minimize the switching turn-on loss, there are two types of switching frequency related losses that need to be considered:

- **Switching turn-off loss.** During the turn-off period, the I_{ds} current reaches peak current, and the transistor is turned off with hard switching at this peak primary current, which will result in a switching crossover turn-off loss. The loss depends on the turn-off energy (E_{off}) of the transistor and can be evaluated by the parameters of gate charge, $Q_{g,}$ and Q_{gd} .
- **Capacitor discharge loss.** During the turn-on period, because of the close zero drain current at turn-on, the turn-on crossover loss can be ignored. However, for PFC stage, if the instant sinusoid AC voltage $V_{in}(t)$ is larger than half of V_{dc} voltage ($V_{dc}/2$), the valley switching voltage is non-zero. There is a capacitor discharge loss due to the parasitic capacitance of the transistor. Similarly, for QR Flyback at high input, the turn-on valley voltage is also non-zero. For this reference design at high $V_{dc}=390\text{V}$, the transformer turns ratio is 7.2 and the output voltage is 22V. The valley switching voltage is equal to $V_{valley_turnon} = V_{dc} - \frac{N_p}{N_s} \cdot V_{out} = 232\text{V}$. The capacitance discharging loss can be evaluated by the transistor's stored energy E_{oss} at around 200V.

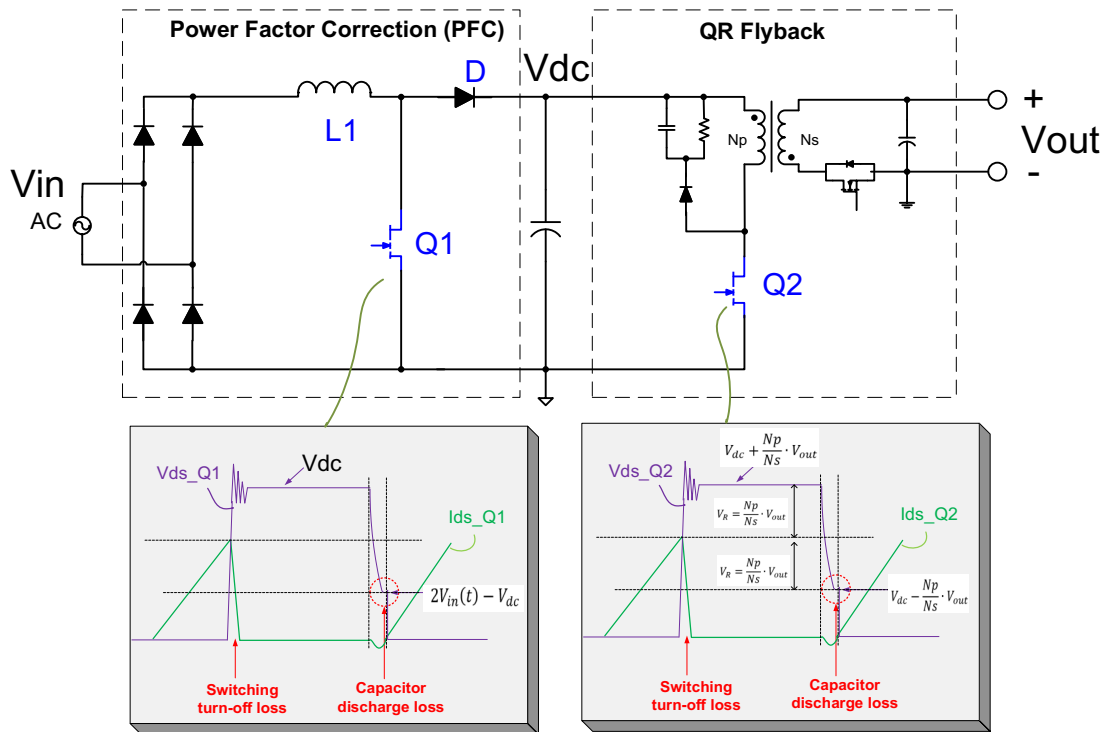


Figure 6. Q1 and Q2 steady state waveforms for Vds and Ids

The combined advantages of GaN transistors: low gate charge, low parasitic capacitor, and low on-state resistance in the converter leads to a more efficient system. Meanwhile, with low gate charge and E_{oss} , the GaN transistor offers the fastest switching speed and high switching frequency for both CrM PFC and QR Flyback to achieve high power density without sacrificing the efficiency and thermal performance.

Table 4 summarizes two key Figures of Merit (FOM) between the GaN transistor and Si Super Junction (SJ) MOSFET. The Input FOM indicates the voltage and current crossover loss during the switching turn-off of the device under the same on-state resistance. The second FOM is PFC+QR Flyback FOM. It indicates the capacitor discharge loss caused by the parasitic capacitance of the transistor at 200V under the same on-state resistance. As can be seen, a GaN transistor has much lower FOMs (both Input FOM and PFC+QR Flyback FOM) compared to Si SJ MOSFETs. The Input FOM of the GaN transistor has only 10% of Si MOSFET's Input FOM while PFC+QR Flyback FOM is more than 25% lower than the Si MOSFET's QR Flyback FOM.

Figure 7 compares the output capacitance stored energy E_{oss} (@200V) between GaN and a best-in-class Si SJ MOSFET at different levels of on-state resistance. It confirms GaN has about 50% lower E_{oss} at the same R_{dson} with $T_j=125^\circ\text{C}$ and 200V V_{ds} . In summary, the low switching turn-off loss and low capacitor discharge loss for a GaN transistor provides the key value propositions for this high density and high efficiency charger.

Table 4. GaN vs Si MOSFET parameters for QR Flyback

Manufacturer	GaN Systems	Si SJ MOSFET		
Part Number	GS-065-011-1-L	#1	#2	#3
Technology	GaN	Si Super Junction MOSFET		
$V_{dss}(V)$	650	600	600	700
R_{dson} (mohm) Typ. $T_j=25^\circ\text{C}$	150	159	300	300
Q_g (nC)	2	24	13	16.4
Q_{gd} (nC)	0.6	8	4	6
Q_{rr} (nC)	0	2900	740	1000
Package type	PDFN5X6	PDFN8X8	DPAK	TO220-FP
Input FOM = $R_{dson} \text{ Hot} * Q_g$	660	7440	7800	9512
PFC+QR Flyback FOM = $R_{dson} \text{ Hot} * E_{oss@200V}$	363	496	480	667

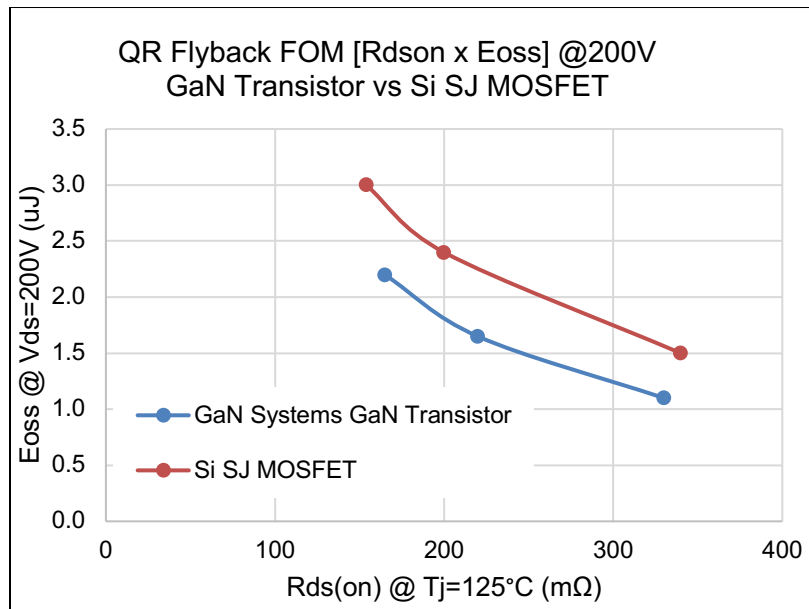


Figure 7. Output energy E_{oss} at 200V with different $R_{ds(on)}$ (GaN vs Si SJ MOS)

5. Test Results

The section illustrates the performance test results of the charger reference design.

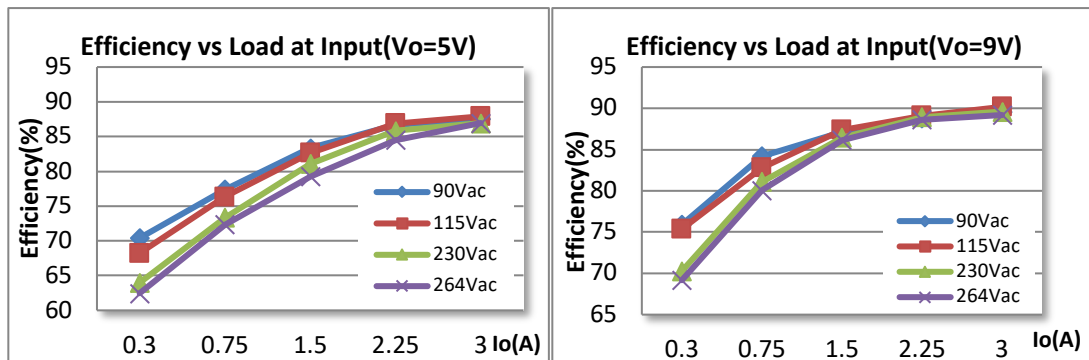
5.1 Test Equipment

- Oscilloscope: Tektronix MDO3054
- AC power source: Chroma 61504
- Electronic load: Chroma 6312A
- Digital power meter: Keysight 34401A
- Power analyzer: Yokogawa WT210

5.2 Efficiency

For the efficiency test, a PD emulator is used to simulate the Type C PD protocol. The Output voltage is directly measured by the multi-meter 34401A from USB-C port on the PCBA board and the output current is measured via the E-load 63115A. The input power is measured with the WT210.

Please note in order to have accurate input power, the input voltage is directly measured on the multi-meter 34401A from AC input on the PCBA when the output voltage is 15V and 20V from half load to full load.



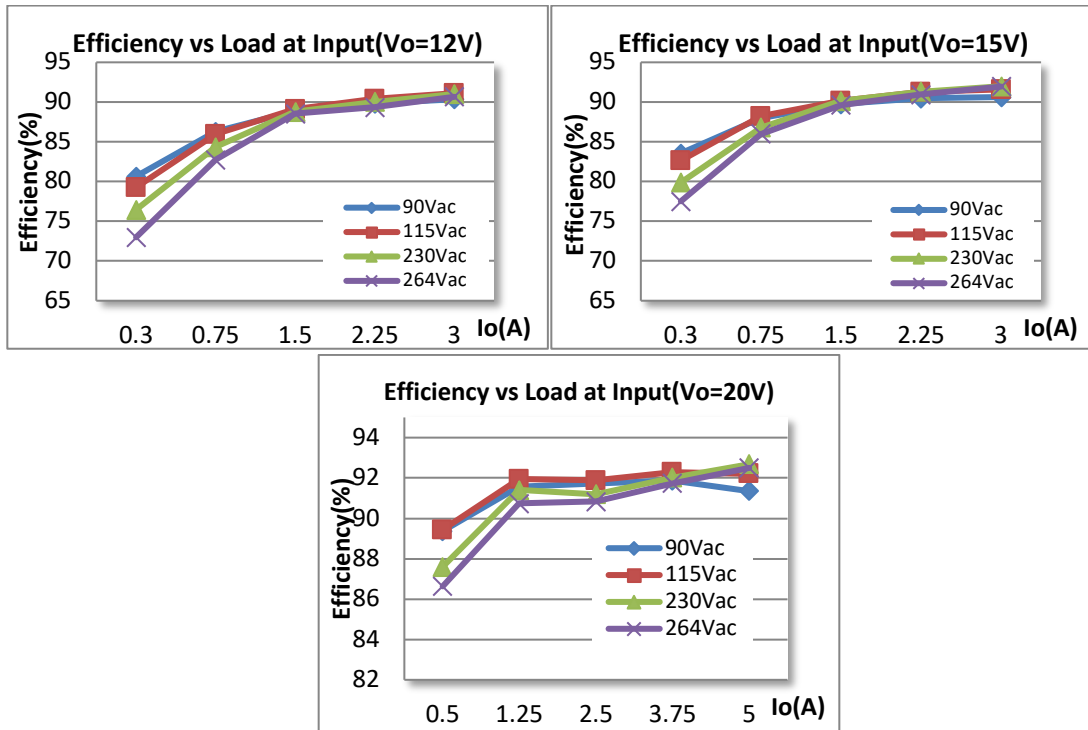


Figure 8. The single USB-C port efficiency curve at 5V, 9V, 12V, 15V, and 20V

The efficiency curve in Figure 8 shows the peak efficiency is above 92.5%. The average efficiency curve in Figure 9 shows this reference design exceeds the CoC V5 2019/1782 efficiency requirement with more than 3% higher average efficiency over the universal input AC voltage.

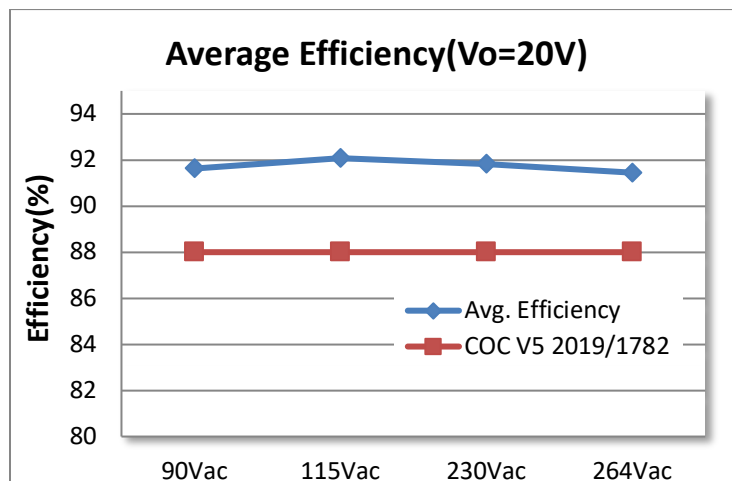


Figure 9. The average efficiency curve at 90V, 115V, 230V, and 264V

5.3 Standby Power

In Figure 10, the no-load standby power is measured from 90V to 264V and the maximum standby power of 190mW occurs at the 264V input which meets the CoC V5 2019/1782 standard requirement with standby power less than 200mW.

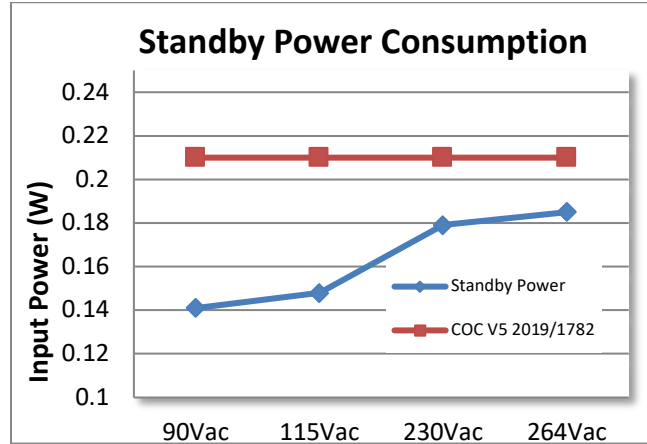
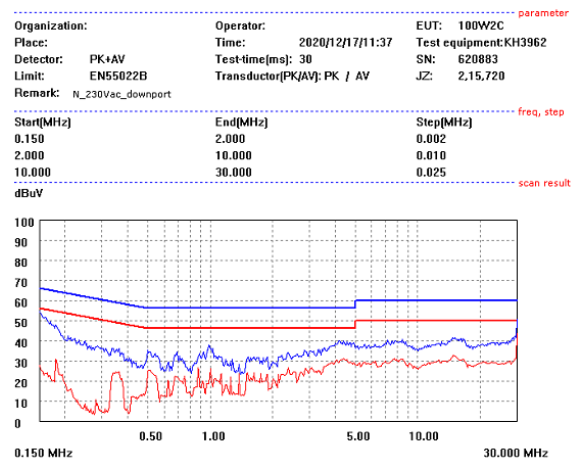
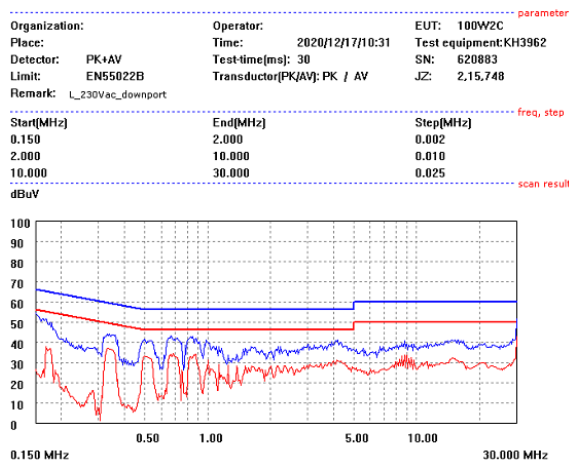


Figure 10. No load standby power from 90V to 264V

5.4 Electromagnetic Interference (EMI)

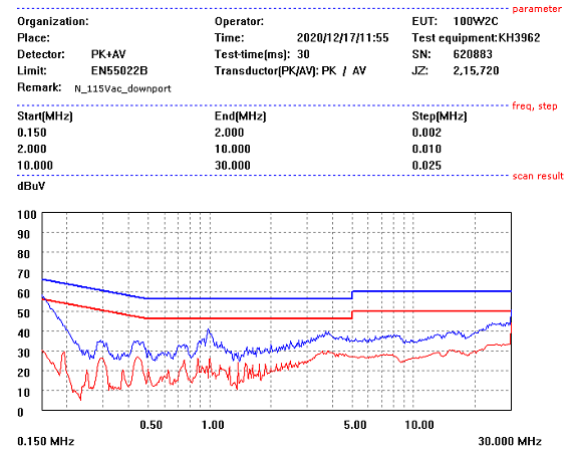
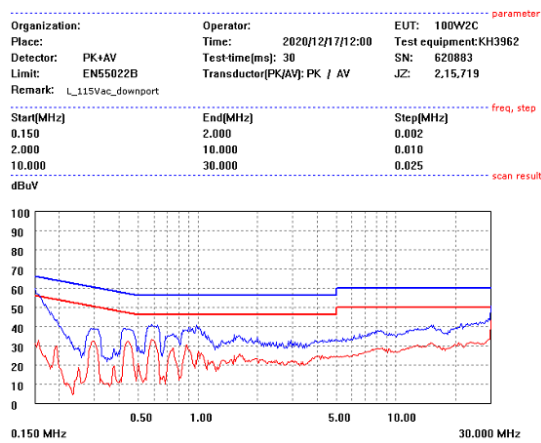
The charger reference design board is measured based on EMI EN55032 class B standard. The test results pass the EMI test with 10dB margin for conduction EMI and 6dB margin for radiation EMI. Figure 11 to Figure 14 give the EMI results at 230V and 115V and full load (20V/5A) conditions.



(a) Line

(b) Neutral

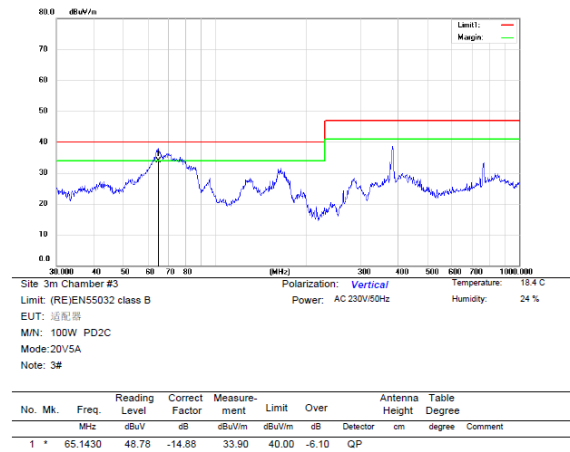
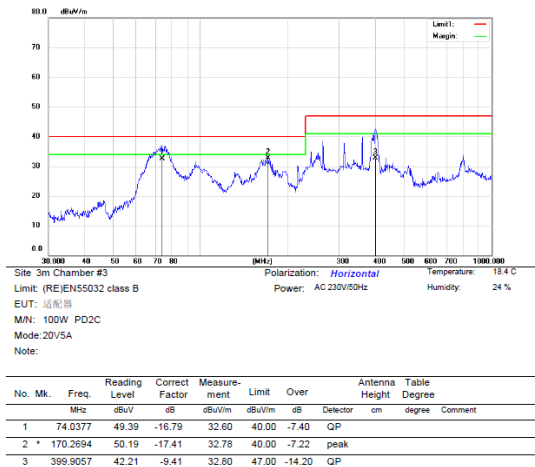
Figure 11. Conduction EMI with 230V input and 20V/5A output



(a) Line

(b) Neutral

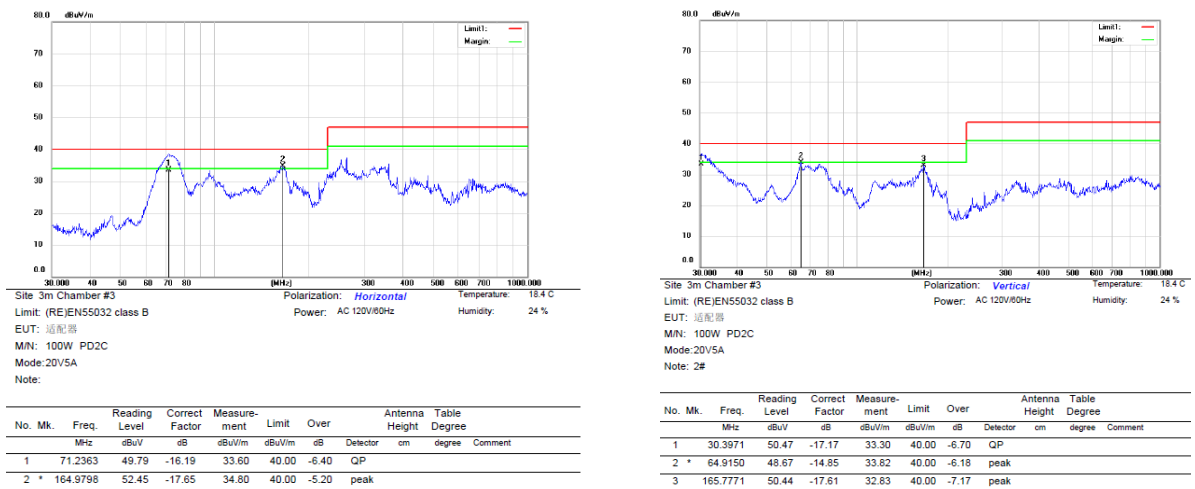
Figure 12. Conduction EMI with 115V input and 20V/5A output



(a) Horizontal

(b) Vertical

Figure 13. Radiation EMI with 230V input and 20V/5A output



(a) Horizontal

(b) Vertical

Figure 14. Radiation EMI with 115V input and 20V/5A output

5.5 Thermal

The surface temperature is measured at 90W and 100W output power as shown in Figure 15 and Figure 16. A plastic case with a 1.5mm thermal conductive silicone pad and 0.5mm copper foil are used to spread the heat on the internal hot spots. The ambient temperature is approximately 25°C with the charger in operation for more than one hour before the thermal is measured.

The temperature results show 70°C maximum temperature for 90W and 75°C maximum temperature for 100W output at 25°C ambient temperature. The results meet the IEC 62368-1 requirement for touch temperature.

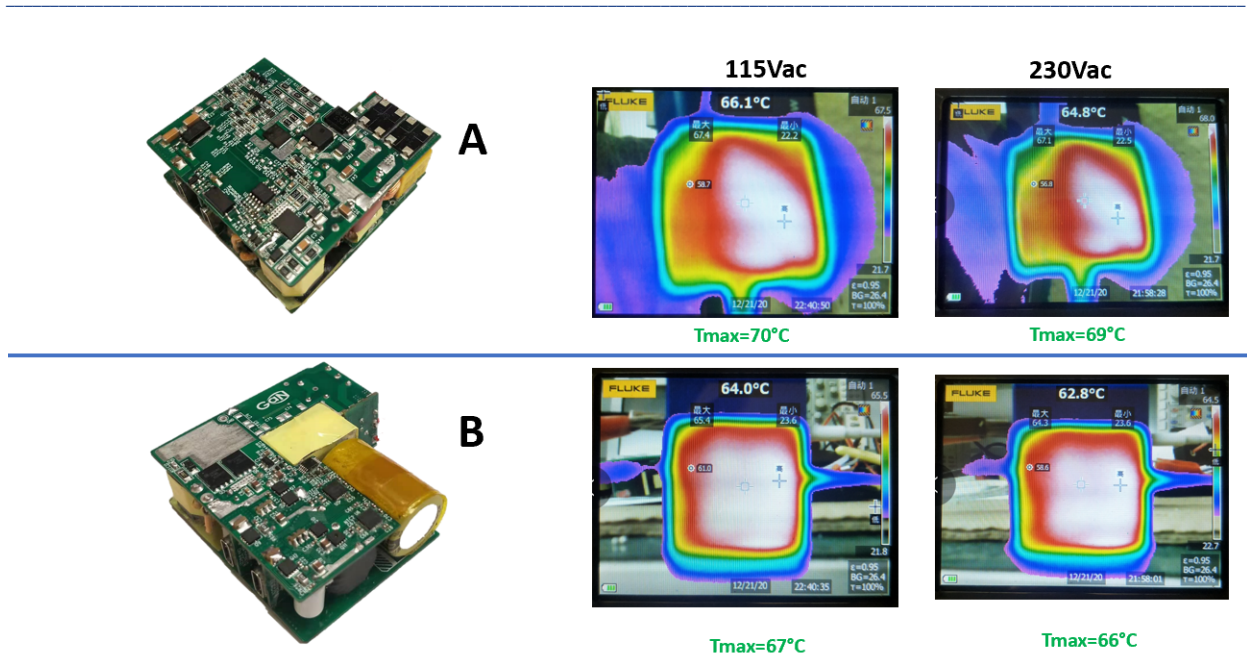


Figure 15. Surface temperature data with 20V/4.5A (90W) output

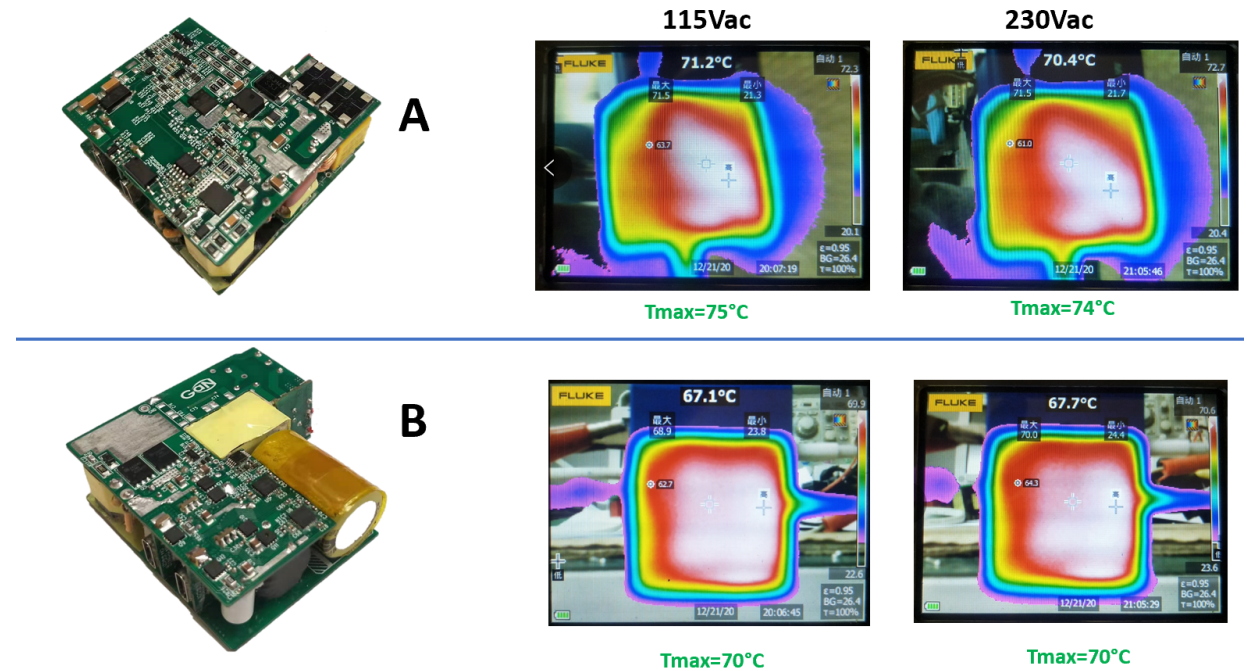


Figure 16. Surface temperature data with 20V/5A (100W) output

5.6 Electrical Waveforms

Figure 17 shows the PFC stage full load steady state waveforms at different input AC voltage.

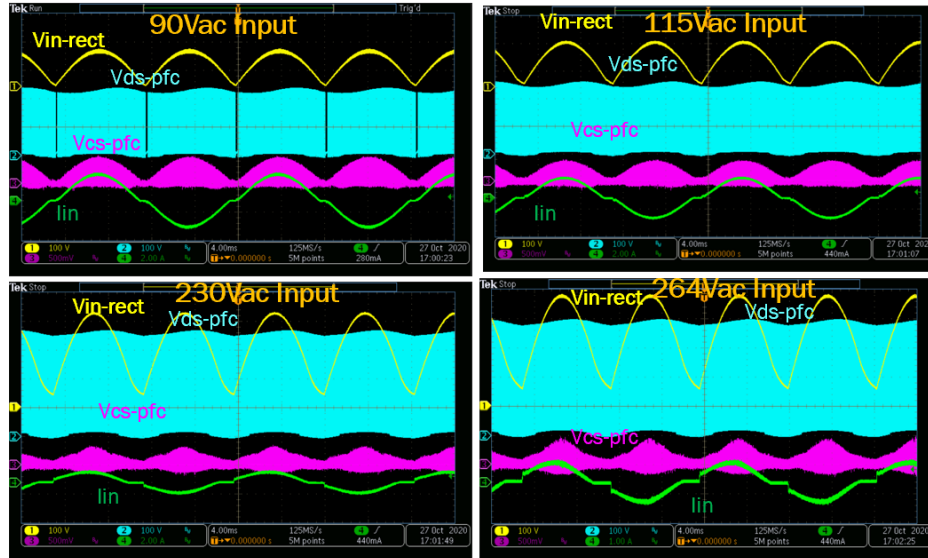


Figure 17. PFC steady state waveforms at 20V/5A (*Vin-rect*: Input voltage after bridge diode; *Vds-pfc*: Vds on PFC's GaN; *Vcs-pfc*: PFC current sense voltage; *Iin*: Input current)

Figure 18 shows the QR flyback steady state waveforms at 20V/5A full load. The maximum frequency at full load is approximately 190KHz at high line 264V input.

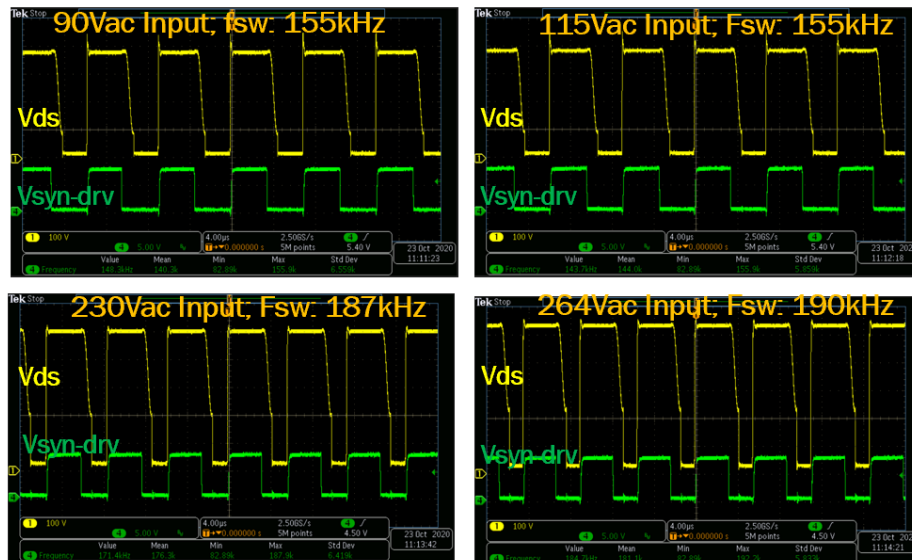


Figure 18. QR steady state waveforms at 20V/5A (V_{ds} : V_{ds} on QR's GaN; $V_{syn-drv}$: V_{gs} on SR FET)

Figure 19 verifies the V_{ds} stress voltage waveforms at steady states and OCP transient condition. The V_{ds} stress voltage “worse case scenario” happens at 264V AC input voltage. The maximum primary QR's GaN stress voltage is below 580V and the maximum secondary SR MOSFET's stress voltage is below 100V. It confirms the stress voltage is lower than the breakdown voltage of transistors with sufficient design margin for both primary 650V QR transistor and secondary 120V SR MOSFET.

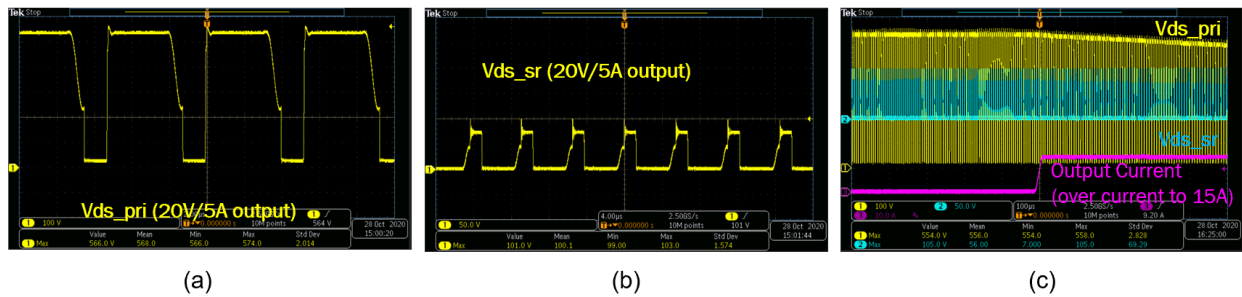


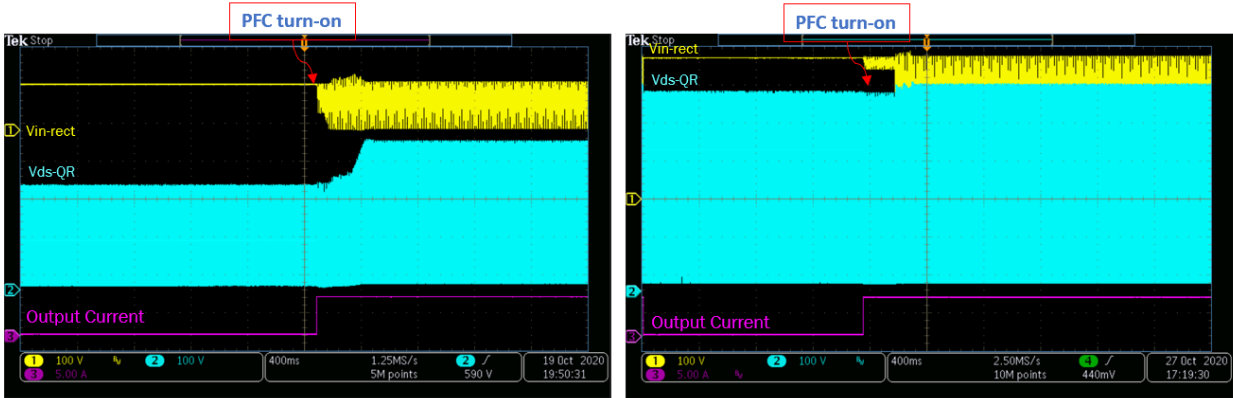
Figure 19. Voltage stress waveforms at 264V AC input, (a): QR GaN Transistor V_{ds} ; (b) Secondary SR MOSFET V_{ds} ; (c) no load to 15A OCP V_{ds} for QR GaN transistor and secondary SR MOSFET (V_{ds_pri} : V_{ds} voltage for QR's GaN; V_{ds_sr} : V_{ds} on QR's SR MOSFET)

Figure 20 shows the load transient waveforms from 0A to 5A. The QR's GaN V_{ds} is smooth below the breakdown voltage during the load transient. Meanwhile, the PFC is turned on when the output power is above 50W after output current increases to 5A.

Figure 21 shows the QR Flyback waveforms 22V DC V_{bus} short circuit protection. Before a short circuit event, the QR Flyback operates at light load burst mode and the charger safely goes to hiccup-mode with an auto-recovery time for 2.6 seconds after V_{bus} short.

Figures 22 shows the output voltage is adjusted by the PD simulator; the V_{ds} waveform is smooth when PD voltage is changed. When output PD voltage is changed from 15V to 20V at 3A, the PFC is turned on with the output power beyond 50W.

Figure 23 gives the output ripple voltage waveform with different output PD voltage. The output ripple voltage is below 100mV at different output PD voltages of 5V, 9V, 15V, and 20V.



(a) 90Vac and 20V output with 0A to 5A

(b) 264Vac and 20V output with 0A to 5A

Figure 20. Load transient waveforms from no load 0A to full load 5A (*Vin-rect*: Input voltage after bridge diode; *Vds-QR*: *Vds* on QR's GaN)

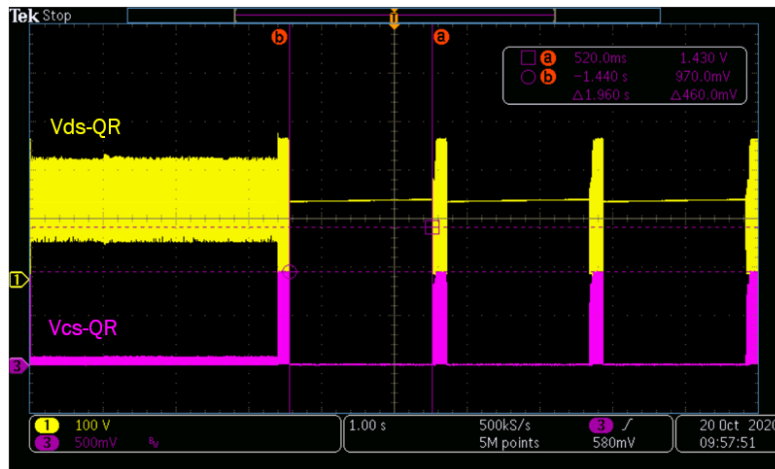


Figure 21. 22V DC Vbus short circuit protection waveforms at 115V input (*Vds-QR*: *Vds* on QR's GaN; *Vcs-QR*: voltage on current sensing resistor for QR Flyback)

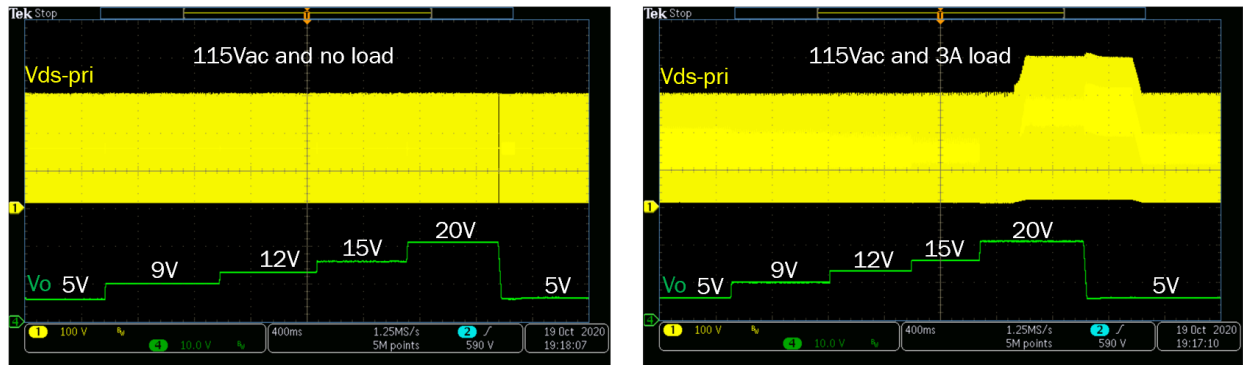


Figure 22. The output voltage is adjusted by the PD simulator with different PD output voltage (V_{ds_pri} : V_{ds} voltage for QR; V_o : USB-C output voltage)

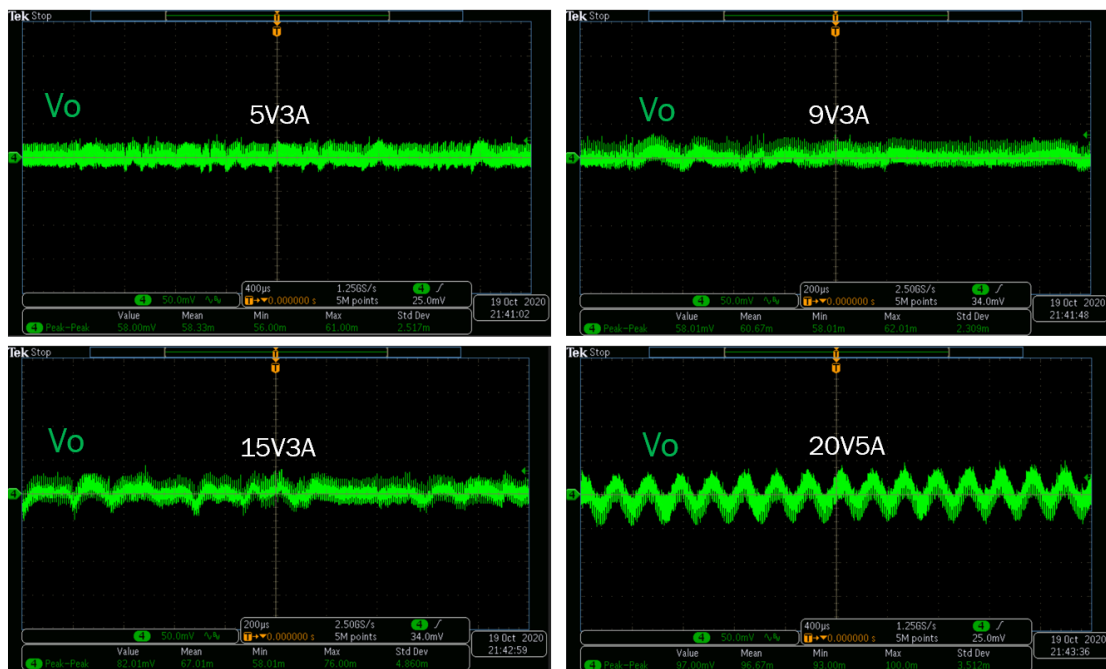


Figure 23. Output ripple voltage with different output voltage and full load (V_o : USB-C output voltage)

6. Conclusion

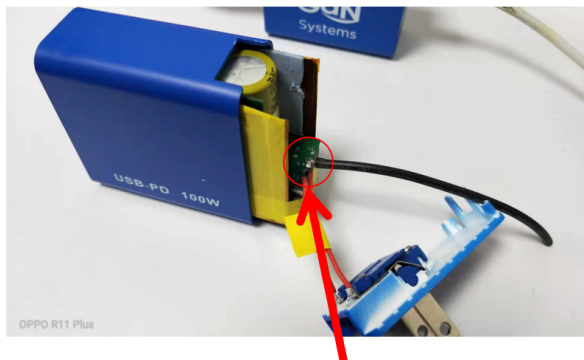
The GaN-based 100W Dual USB-C PD charger reference design is introduced in this technical manual. The reference design achieves the following best-in-class features and performance:

- Topology: Low cost CrM PFC & QR Sync-Flyback
- Cased Power density: 16.3W/in³ (100cc)
- Efficiency: >92.5%
- Standby power: Exceeds standards with <200mW
- Waveforms: Clean with full protections (SCP, OCP, OVP etc.)
- Thermal: ≤ 75°C (meet IEC 62368-1 touch temperature)
- EMI: Pass EN55032 Class B with >6dB margin

Appendix – How to remove the PCBA from the Case

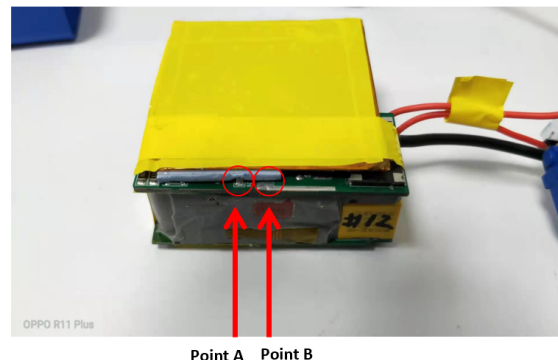
When measuring the board performance such as electrical waveforms, the PCBA has to be taken out from the charger case. The below manual steps are recommended for safety.

Step 1:



1. Solder a thicker wire (black) on the point and take out the whole PCBA from the case by pulling the thicker wire

Step 2:



2. Discharge the stored energy from point A to point B and make sure the voltage between A and B are close to zero

Figure 24. How to take out PCBA from the case

References

- [1] GaN Systems Application Note GN010, EZDrive™ Solution for GaN Systems E-HEMTs, 2020, [Online]. Available: https://gansystems.com/wp-content/uploads/2020/07/GN010_EZDrive-Solution-for-GaN-Systems-GaN-Transistors-20200715.pdf
- [2] GaN Systems Reference Design, GS-EVM-CHG-65WQR-GS1, 65W Type-C PD QR Charger Reference Design [Online]. Available: <https://gansystems.com/evaluation-boards/gs-evm-chg-65wqr-gs1/>

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