

RS OEMax

NX70 Plus 시스템 (NX70-CPU70p1, NX70-CPUp2)

사용 설명서

Catalog Number(s): NX70-CPU70p1,
NX70-CPU70p2)

일러두기

이 문서에서 설명하는 제품은 다양한 애플리케이션에 사용될 수 있습니다. 본 제품의 적용 애플리케이션이 다양하므로 본 제품의 모든 사용자와 관리자는 사용하고자 하는 애플리케이션과 관련된 운전 및 안전상의 제 법령 및 규정과 준수사항을 반드시 확인하고 지켜야 합니다.

사용자가 본 제품을 사용 및 응용함에 따른 직접 또는 간접적인 손상에 대해서 알에스오토메이션(주)는 그 책임을 면합니다.

이 문서에 사용된 예제, 삽화, 도표, 데이터 등은 설명을 위한 예시적인 자료일 뿐입니다. 제품이 설치 및 사용되는 구체적인 상황에 따라 많은 변수와 충족되어야 할 전제 조건들이 있습니다. 이러한 사유로 이 문서에서 제시된 예시, 도표 및 데이터의 사용 및 이에 따른 직간접적 결과에 대해 알에스오토메이션(주)는 그 책임을 면합니다.

알에스오토메이션(주)는 본 매뉴얼에 포함된 소프트웨어, 장비, 회로 또는 정보 사용에 대해 특허 책임을 면합니다.

알에스오토메이션(주)의 서면 승인 없이 본 매뉴얼의 내용 전부 또는 일부를 복제하는 것은 금지됩니다.

사용자의 안전 및 효과적인 정보 전달을 위해 이 문서는 다음 기호들을 사용하고 있습니다

경고



주어진 정보 또는 절차를 잘못 취급할 경우, 사망, 중상 또는 재산상의 손실을 야기할 수 있음을 나타냅니다.

중요

주어진 정보가 제품을 이해하고 활용함에 있어 중요한 정보임을 나타냅니다.

주의



주어진 정보 또는 절차를 잘못 취급할 경우, 경상 또는 재산상의 손실을 야기할 수 있음을 나타냅니다. 그렇지만, 상황에 따라서 심각한 결과를 가져올 수도 있습니다.

1.

1-1. CPU70plus(NX70) PLC	
(1)	10
(2) CPU70plus(NX70) PLC	10
(3) I/O	11
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(1)	12
(2)	14
(3) 가	15
(4)	16
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NX70 PLC



주의

...

1. 가 0~55
- 2.
3. 가 30~85%
- 4.
5. ,
6. , , 가
7. ,



주의

.....

가 가 ,



주의

.....

(PCB)



주의

.....

1. PLC , , 가 .
(, PROG. , RUN .)
2. PLC , PLC OFF .
3. PLC 가 ON/ OFF PLC가
가 .



주의

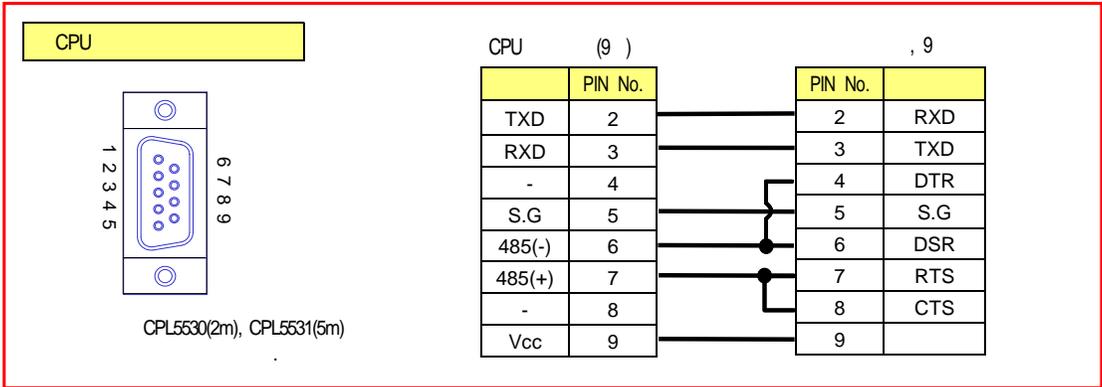
.....

1. , 가 .
2. , 가 .
3. , .
4. PROG. .

NX70(NX70-CPU70p1, NX70-CPU70p2) CPU

- NX70-CPU70p1 가 1 . (RS232C/ RS485 x 1)
- NX70-CPU70p2 가 2 . (RS232C/ RS485 x 2)
- PLC Nplus- (SPC10, N70plus, N700plus, NX7, NX70(CPU70p1, CPU70p2), NX700(CPU700p) PLC)
WinGPC S/W

CPU



NX70 PLC CPU

CPU				SW
NX70-CPU70p1	<ul style="list-style-type: none"> • 9K Words (), 0.2μs/ STEP, RS232C/485 1 , • FLASH ROM • 2K Data Register 		NX70 (NX70-CPU70p1, p2)	WinGPC SW
NX70-CPU70p2	<ul style="list-style-type: none"> • 20K Words (), 0.2μs/ STEP, RS232C/485 2 , • , FLASH ROM , PID , • 4K Data Register 			

CPU	가	
NX70-CPU70p1	ROM 2.0 : CCU, W-Link, MW-Link, HSC 4Ch, Pulse4, 가.	
NX70-CPU70p2	ROM 2.0 : CCU 가.	
NX70-CPU70p2	CCU ,	ROM 2.0

* CPU ROM

* CCU NX , NX plus CCU+ .

NX70 PLC N70 PLC



N70 PLC NX70 PLC CPU , POWER

ex1) N70plus CPU(CPL9215) NX70 PLC (NX70-BASE02 NX70-BASE12)

ex2) N70 POWER (CPL9631) NX70 PLC (NX70-BASE02 NX70-BASE12)

ex3) N70 (CPL9502 CPL9508) Version-Up Analog 가

ex4) NX70 PLC (NX70-BASE02 NX70-BASE12) N70 I/O



PLC N- N-plus 가 . (S/W가)
 , N70 , N700 , NX70 , NX700 CPU (POWER, I/O, ...)

		CPU	
N-plus, NX-plus	SPC	SPC10, SPC24S, SPC120S, SPC100, SPC300, A200	WinGPC S/W
	N70	CPL9215A, CPL9216A	
	N700	CPL7215A	
	NX7	NX7-28ADR, NX7-28ADT, NX7-48ADR, NX7-48ADR.....	
	NX70	NX70-CPU70p1, NX70-CPU70p2	
	NX700	NX-CPU700p	

N- NX-	N7	CPL02323, CPL02343C, CPL02543C.....	WinFPST S/W
	N70	CPL9210A, CPL9211A	
	N700	CPL7210A, CPL7211A, CPL6210A, CPL6210B, CPL6215A	
	NX70	NX70-CPU70, NX70-CPU750	
	NX700	NX-CPU750A, NX-CPU750B, NX-CPU750C, NX-CPU750D, NX-CPU700	

1

1-1. CPU70plus(NX70) PLC	
(1)	10
(2) CPU70plus(NX70) PLC	10
(3) I/O	11
1-2 ()	
(1)	12
(2)	14
(3) 가	15
(4)	16
1-3.	
(1)	17

1-1. CPU70plus(NX70) PLC

(1)



(2) CPU70plus(NX70) PLC

1. IC 가 0.2μ sec/STEP 가 가 .
2. RUN CPU
3. Clock(RTC : Real Time Clock) function (NX70-CPU70p2)
4. / 20k (NX70-CPU70p2), 9.6k (NX70-CPU70p1) 가 , FLASH (EEPROM)
- 5.
6. 384 가
7. DC24V (16/32), AC110V , AC220V , TR (16 /32), SSR , A/D(4CH), D/A(2CH, 4CH), RTD(4CH), TC(4CH), SCU(), MW-Link, .
8. WinGPC CPU S/W , CPU WinGPC / .
9. (12) 2 , 3 , 5 , 6 , 8 , 10 , 12 .
10. RS232C/ RS485, 2 (NX70-CPU70p2) 2 TOUCH PANEL DATA 가 , COM2 , (가) ,

(3) I/O

2  (NX70-BASE02) 32 : 16 I/O 64 : 32 I/O	3  (NX70-BASE03) 48 : 16 I/O 96 : 32 I/O	5  (NX70-BASE05) 80 : 16 I/O 160 : 32 I/O	6  (NX70-BASE06) 96 : 16 I/O 192 : 32 I/O
8  (NX70-BASE08) 128 : 16 I/O 256 : 32 I/O	10  (NX70-BASE10) 160 : 16 I/O 320 : 32 I/O		
12  (NX70-BASE12)			192 : 16 I/O 384 : 32 I/O

- NX70 PLC 7 가 , (2 , 3 , 5 , 6 , 8 , 10 , 12)
- I/O , , CPU
- I/O 384
- NX70 PLC 12 , 384 (192)
- NX70 PLC . (.)

NX70 PLC N70 PLC

N70 PLC NX70 PLC CPU , , POWER

ex1) N70plus CPU(CPL9215) NX70 PLC (NX70-BASE02 NX70-BASE12)

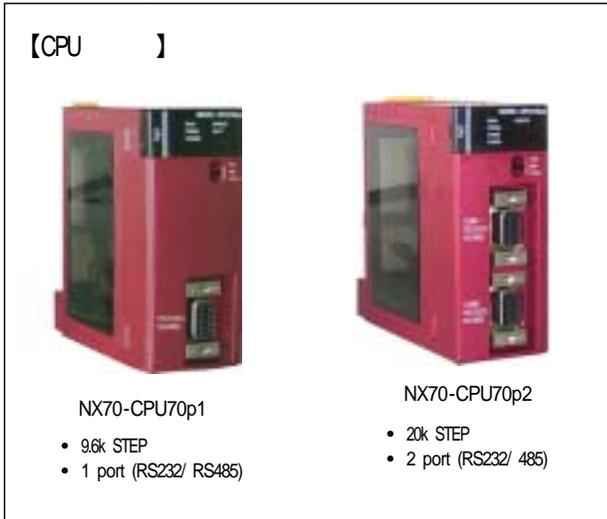
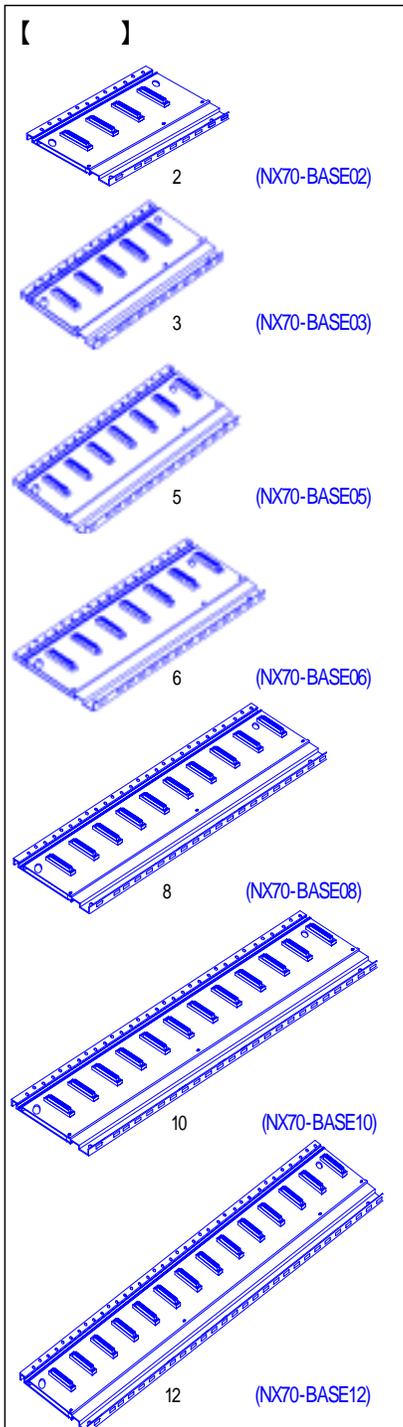
ex2) N70 POWER (CPL9631) NX70 PLC (NX70-BASE02 NX70-BASE12)

ex3) N70 (CPL9502 CPL9508) Version-Up Analog 가

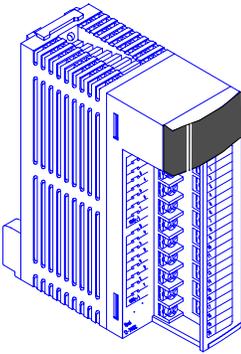
ex4) NX70 PLC (NX70-BASE02 NX70-BASE12) N70 I/O

1-2. ()

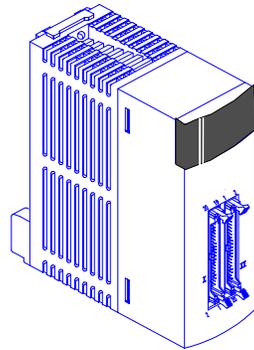
(1)



[/]

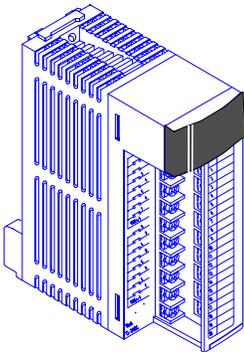


- | | |
|--|--|
| <p>16</p> <ul style="list-style-type: none"> • 24V DC IN (NX70-X16D) (NX70-X16D1) • 110V AC IN (NX70-X16A110) • 220V AC IN (NX70-X16A220) <p>8</p> <ul style="list-style-type: none"> • Relay OUT (NX70-Y8R) | <p>16</p> <ul style="list-style-type: none"> • Relay OUT (NX70-Y16R) (NX70-Y16RV) • TR OUT (NX70-Y16T) • SSR OUT (NX70-Y16SSR) <p>16</p> <ul style="list-style-type: none"> • DC 8IN/Ry 8out (NX70-XY16) |
|--|--|

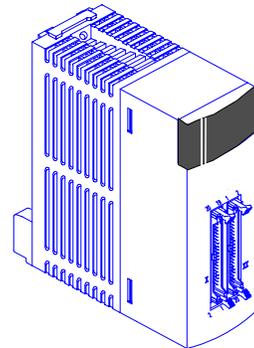


- | |
|--|
| <p>32</p> <ul style="list-style-type: none"> • 24V DC IN (NX70-X32D) (NX70-X32D1) <p>32</p> <ul style="list-style-type: none"> • TR OUT (NX70-Y32T) (NX70-Y32P) <p>32</p> <ul style="list-style-type: none"> • DC 16IN/TR 16out (NX70-XY32) |
|--|

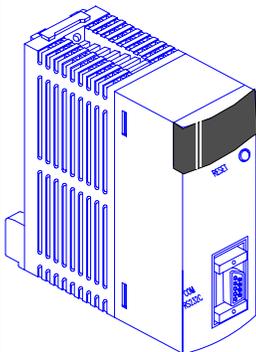
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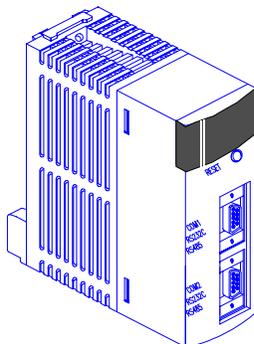
- | | |
|---|--|
| <p>Analog</p> <ul style="list-style-type: none"> • 8CH, (NX70-AI8C) • 8CH, (NX70-AI8V) • 4CH, (NX70-AI4C) • 4CH, (NX70-AI4V) <p>Analog</p> <ul style="list-style-type: none"> • 4CH, (NX70-AO4C) • 4CH, (NX70-AO4V) • 2CH, (NX70-AO2C) • 2CH, (NX70-AO2V) | <p>RTD</p> <ul style="list-style-type: none"> • 4CH, RTD (NX70-RTD4) <p>TC</p> <ul style="list-style-type: none"> • 4CH, TC (NX70-TC4) <p>1</p> <ul style="list-style-type: none"> • 2CH, HSC (NX70-HSC2) • 1CH, HSC (NX70-HSC1) |
|---|--|



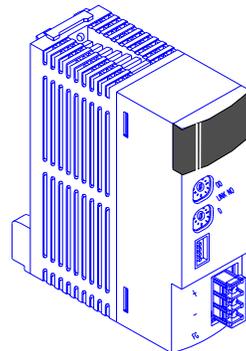
- | |
|---|
| <p>2</p> <ul style="list-style-type: none"> • 4CH, HSC (NX70-HSC4) • 4CH, Pulse (NX70-PULSE4) • 2CH, 4Ch (NX70-POS12) (NX70-POS14) |
|---|



CCU+ (NX70-CCU+)



SCU (NX70-SCU)

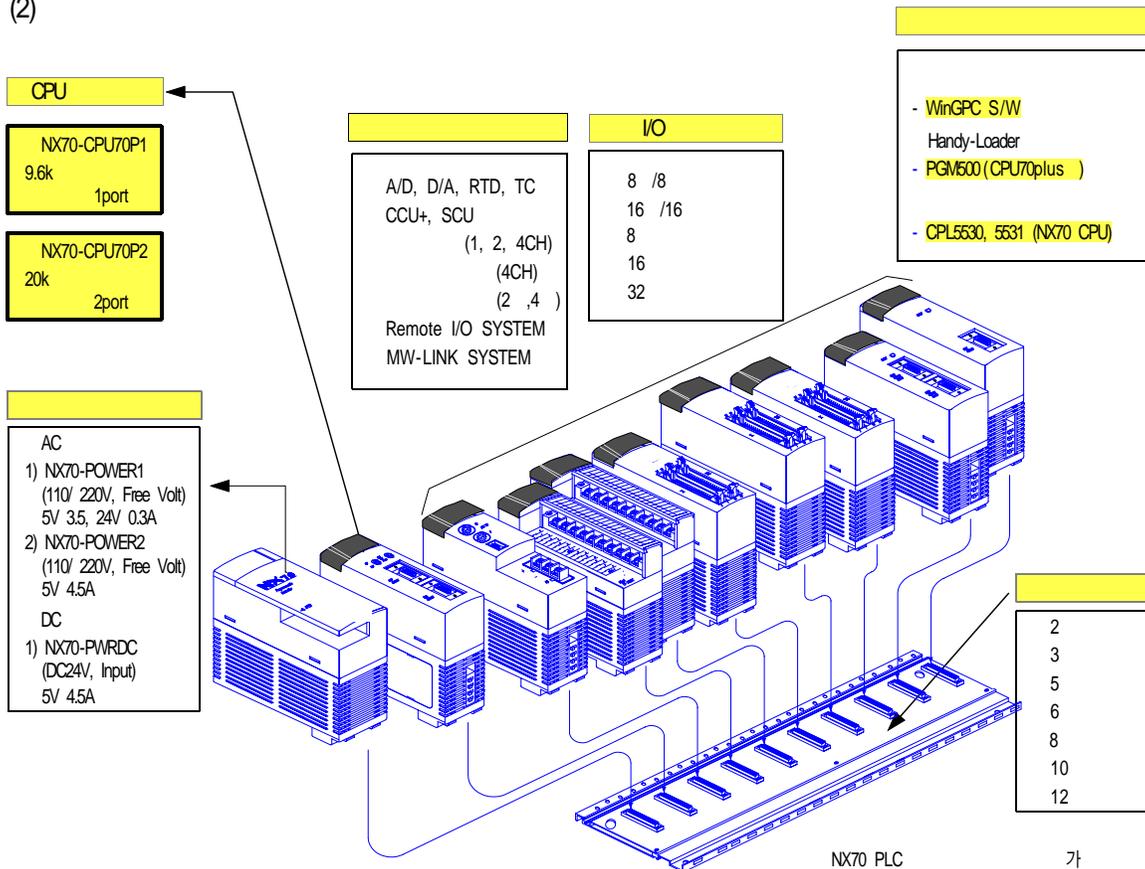


W-LINK (NX70-MWLINK)

- MW-LINK (NX70-MWLINK)
Multi W-Link (MW-Link)
• W - Link

Slave (NX70-SLAVE)

(2)



CPU	AC		DC		AD, D/A, RTD, TC		CCU+		SCU		W-Link		MW-Link		Remote Slave	
	(NX70-POWER1, NX70-POWER2)		(NX70-PWRDC)		(1CH / 2CH)		(1CH)		(2, 4)		(W-)		(W- , W2-)			
	(2, 3, 5, 6, 8, 10, 12)															
CPU	NX70-CPU70p1															
CPU	NX70-CPU70p2															

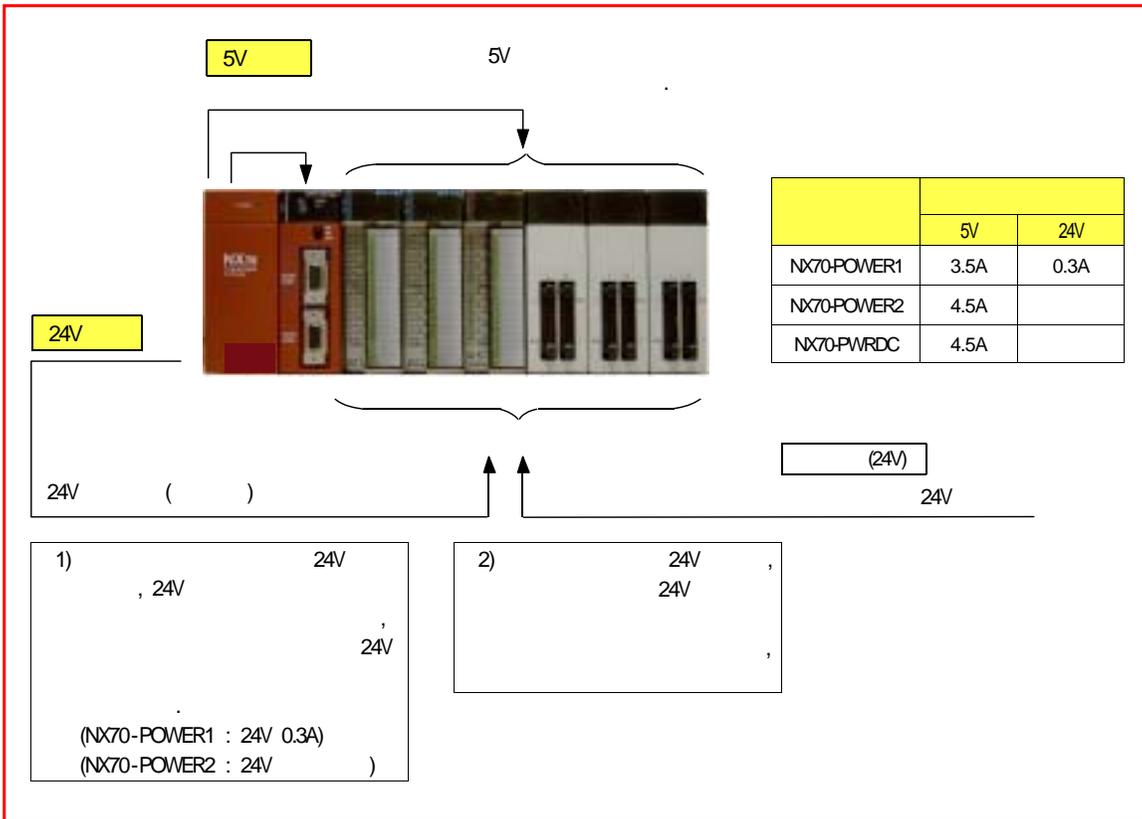
ROM 2.0

(3) 가

1.

	NX70-CPU70p1, NX70-CPU70p2	
CCU+	ROM 2.0 1 가	
W-Link	2 가	
MW-Link (W-)	가	

(4)



(5V) , 5V, 24V
5V ,
()

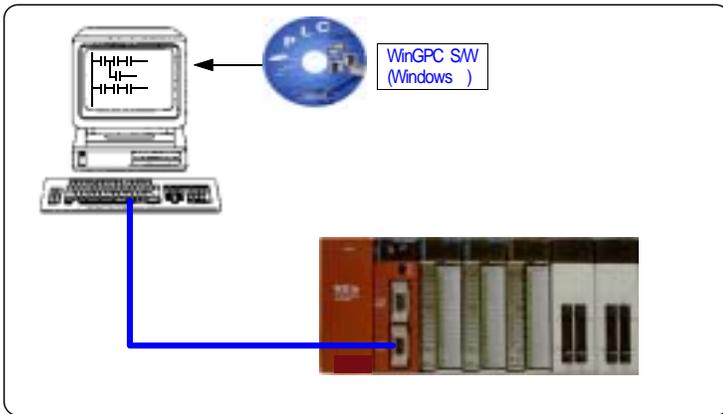
- (24V)
- 24V ,
 - ()
 - , NX70-POWER2 NX70-PWRDC 24V
(5V 가)

1-3. Tool

(1) (Tool)

WinGPC S/W

가



WinGPC S/W (Windows)

PLC Nplus-

WinGPC S/W Windows

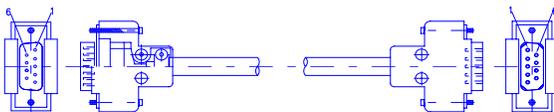
(WinGPC S/W Ver 3.**)

PLC Nplus- , SPC10, N70plus, N700plus, NX7, NX70(CPU70p1, CPU70p2), NX700(CPU700p) PLC CPU

CPU70plus(NX70) CPU

(CPL5530, CPL5531)

가



CPU (9) -

, 9 -

	PIN No.		PIN No.	
TXD	2	—	2	RXD
RXD	3	—	3	TXD
-	4	—	4	DTR
S.GND	5	—	5	GND
485(-)	6	—	6	DSR
485(+)	7	—	7	RTS
-	8	—	8	CTS
Vcc	9	—	9	

2

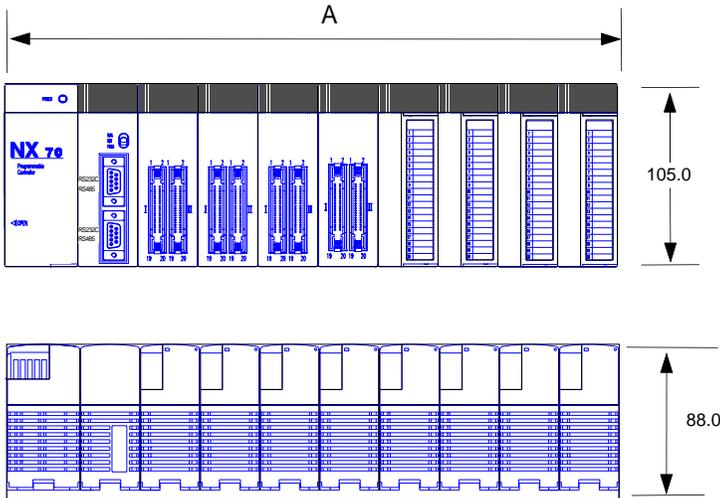
2-1.	20
(1)	20
(2)	20
(3)	21
2-2.	22
2-3. CPU	23
(1-1) CPU (NX70-CPU70p1)	23
(1-2) CPU (NX70-CPU70p2)	25
2-4.	27
2-5. ,	29
(1)	29
(2)	30
(3)	33

2-1.

(1)

		0 55
		-25 70
		30 85% RH (,)
		30 85% RH (,)
AC <-> , AC 1500V 1		
DC <-> , AC 500V 1		
		<-> , 100M (DC 500V 가)
		10 55Hz 1掃引/ 1 , 0.75mm, X, Y, Z 10
		98 m/s ² , X, Y, Z 4
		1500 Vp-p 50ns, 1μs ()
		IP20 (가 가 , 가)

(2) (mm)



(mm)

	2	3	5	6	8	10	12
	NX70-BASE02	NX70-BASE03	NX70-BASE05	NX70-BASE06	NX70-BASE08	NX70-BASE10	NX70-BASE12
A(mm)	149.5	185.0	256.0	291.5	362.5	398.0	433.5

(3)

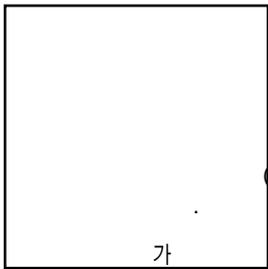
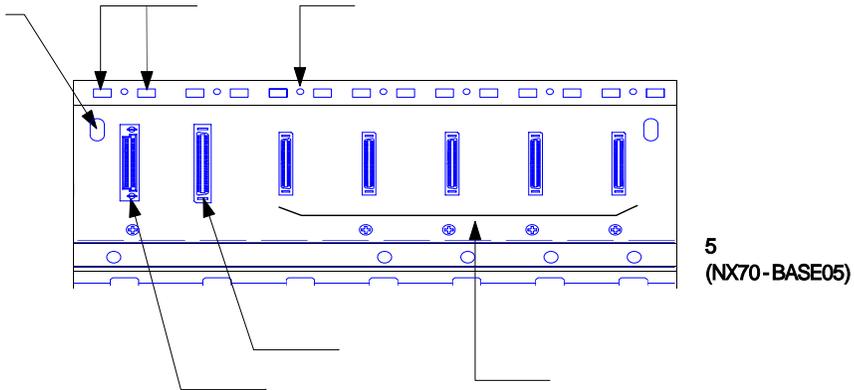
CPU		NX70-CPU70p1	NX70-CPU70p2
		384 (32 / 12 Slots)	
		48 (4 / 12 Slots)	
		30	
		147	
		0.2 μs/step	
		1.0 ~ μs/step	
		9.6K	20K
	(R)	2,048 (R0.0 ~ R127.15)	
	(L)	1,024 (L0.0 ~ L63.15)	
	(M)	2,048 (M0.0 ~ M127.15), (, NX70-CPU70p2 가 , 64)	
	(K)	2,048 (K0.0 ~ M127.15)	
	(F)	256 (F0.0 ~ F15.15)	
	(TC / TIM)	256 (+), : 0 ~65535 : 0.01 : CH000~CH063 (64) , 0.1 : CH064~CH255 (192) : CH000 ~ CH255 (256)	
	(W)	2,048 (W0000 ~ W2047)	4,096 (W0000~ W2047), (W3072~ W5119)
	(W, SR)	512 W2560(=SR000) ~ W3071(=SR511)	
	(RTC)		
	Port 1	RS232C/ RS485 , 4800/ 9600/ 19200/ 38400bps	
	Port 2	RS232C/ RS485 , 4800 38400bps 가	
FLASH ROM	(BACK-UP)	(CPU)	

K, W, Counter PV Register

CPU Battery가 Super Capacitor 48 Register
Back-Up

2-2.

(NX70-BASE02, NX70-BASE03, NX70-BASE05, NX70-BASE06, NX70-BASE08, NX70-BASE10, X70-BASE12)



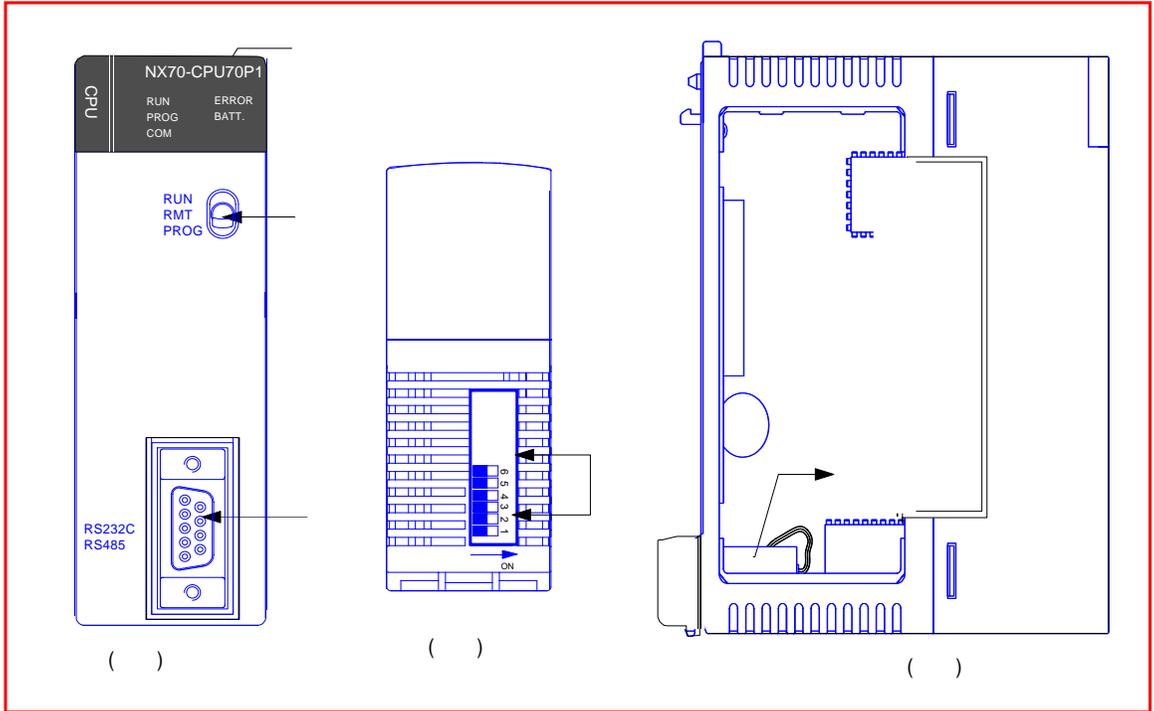
), CPU, I/O()

2	NX70-BASE02	
3	NX70-BASE03	
5	NX70-BASE05	
6	NX70-BASE06	
8	NX70-BASE08	
10	NX70-BASE10	
12	NX70-BASE12	

CPU
 CPU . CPU
 I/O ()
 I/O()

2-3. CPU

(1-1) CPU (NX70-CPU70p1)



LED
 PLC / , /
 .
 PLC
 COM (RS232C/ RS485), 9
 (WinGPC SW) T/P
 가
 DIP SW (6 ,)
 (RAM)
 가

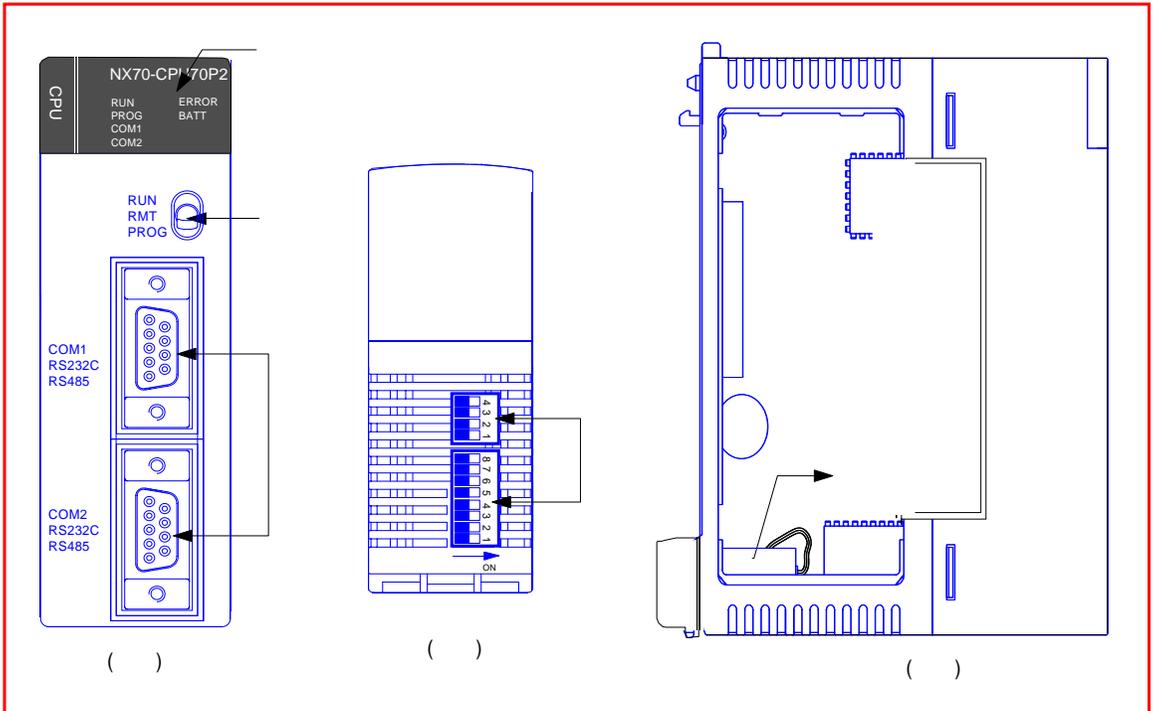
LED	
LED	
LED	
RUN	CPU가 RUN
PROG.	Program 가
COMM.	CPU가
ERROR	CPU가 Error
BATT.	Battery

RUN	CPU RUN Mode
REMOTE	CPU RUN PROG Mode
PROG.	CPU Stop, Program



PIN						Dip Switch	
6	5	OFF	OFF	9600 bps			/
		ON	OFF	19200 bps			
		OFF	ON	38400 bps			
		ON	ON	4800 bps			
4	OFF		RS-232C				
	ON		RS-485				
3	OFF		RAM				
	ON		FLASH ROM				
2, 1	ON	ON	RS-485 : ,)				
	OFF	OFF	RS-485 : ,)				

(1-2) CPU (NX70-CPU70p2)



LED
 PLC / , /
 PLC
 COM1, COM2 (RS232C/ RS485), 9
 (WinGPC SW) T/P MMI,
 (COM2) 가

DIP SW 1(4 ,),
 DIP SW 2(8 ,)
 (RAM) 가

LED

LED		
RUN		CPU가 RUN
PROG.		Program 가
COM1		CPU가 COM1
COM2		CPU가 COM2
ERROR		CPU가 Error
BATT		

RUN	CPU	RUN Mode
REMOTE	CPU	RUN PROG Mode
PROG.	CPU	Stop, Program



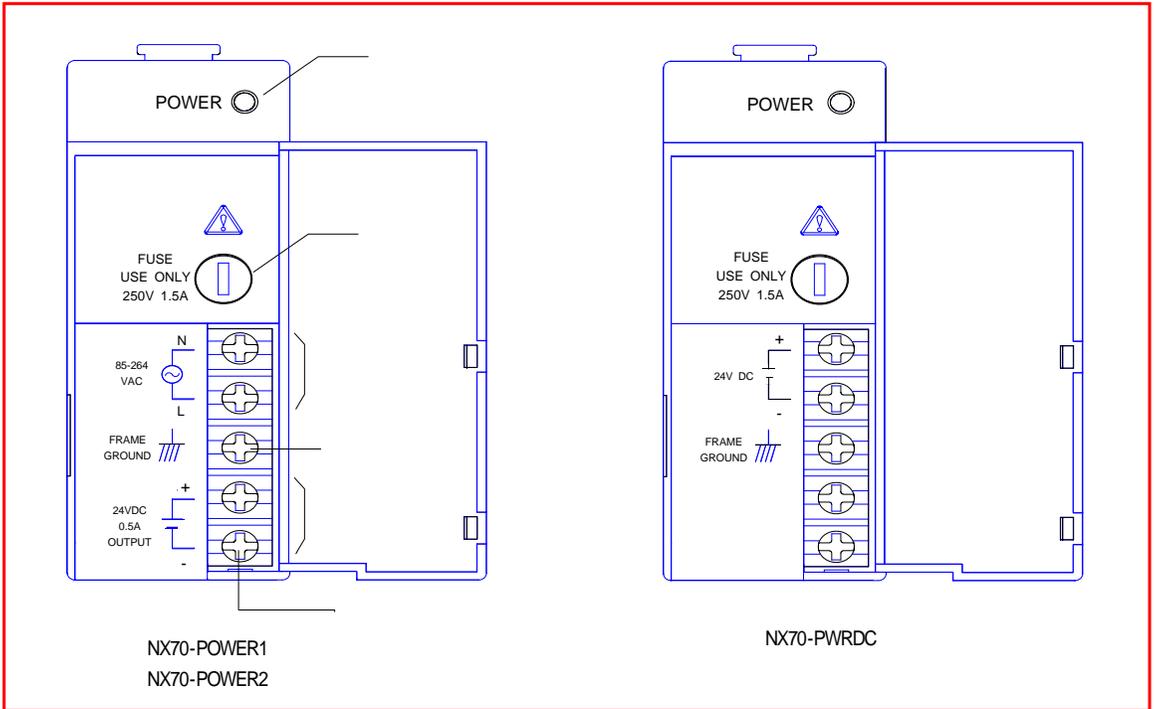
("DIP 1")

PIN						Dip Switch1
3, 4	ON	ON	RS-485	:	(COM1)	
	OFF	OFF	RS-485	:	(COM1)	
1, 2	ON	ON	RS-485	:	(COM2)	
	OFF	OFF	RS-485	:	(COM2)	

/ ("DIP 2")

PIN						Dip Switch2
8,7	OFF	OFF	COM2	9600 bps		
	ON	OFF	COM2	19200 bps		
	OFF	ON	COM2	38400 bps		
	ON	ON	COM2	4800 bps		
6,5	OFF	OFF	COM1	9600 bps		
	ON	OFF	COM1	19200 bps		
	OFF	ON	COM1	38400 bps		
	ON	ON	COM1	4800 bps		
4	ON		COM1	RS-485		
	OFF		COM1	RS-232C		
3	ON		COM2	RS-485		
	OFF		COM2	RS-232C		
2	OFF		OFF	()		
1	ON		ON	EEPROM (Flash ROM) Load.		
	OFF		ON	RAM		

2-4.



POWER LED

M3.5

AC110-240V Free Voltage
(, NX70-PWRDC DC24V)

Frame Ground (FG)

3

(DC24V)
DC

	NX70-POWER1	NX70-POWER2
	AC 110 220V, Free Voltage	
	AC 85 264V	
	47 63Hz	47 63Hz
	20A	20A
(5V)	5V 3.5A	5V 4.5A
(24V)	24V 0.3A	

	NX70-PWRDC	
	DC 24V	
	DC 21.6 26.4V	
(5V)	5V 4.5A	

주의 NX70-POWER1, NX70-POWER2 , AC110V

주의

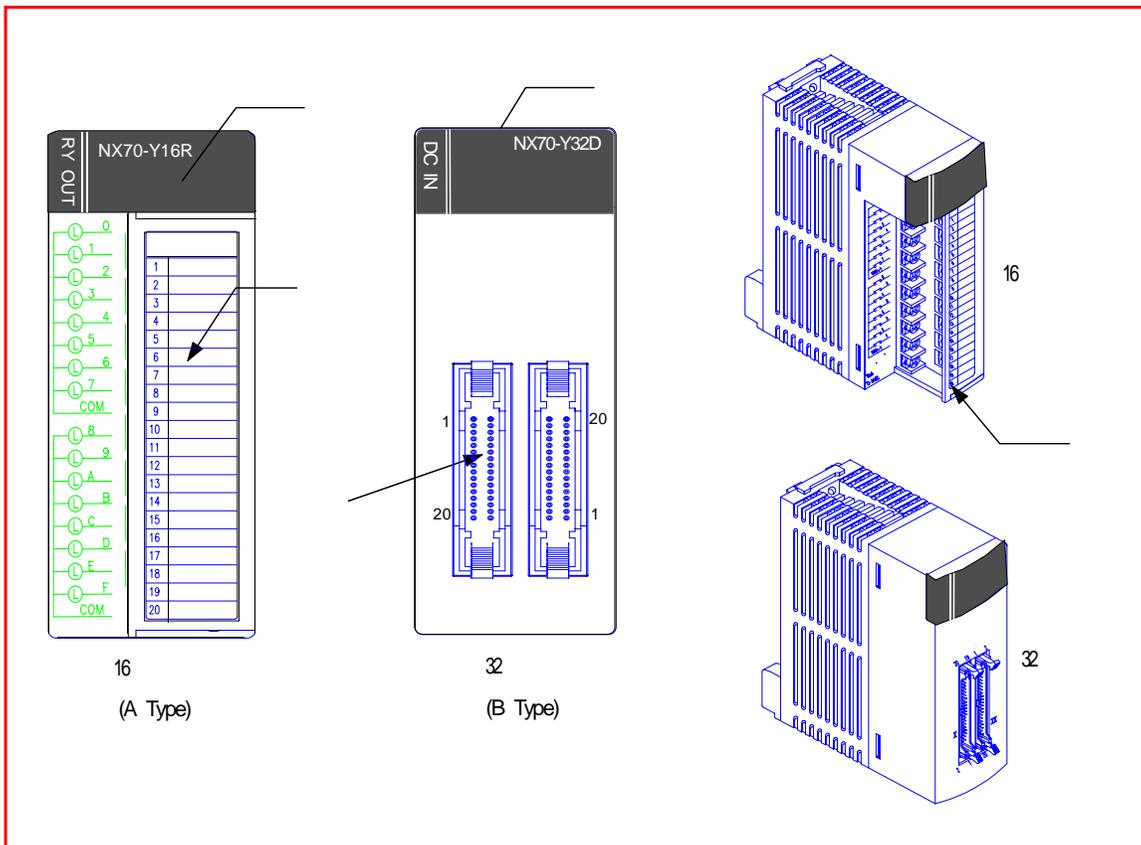
(5V) 24V 5V



- (1) 가
- (2) 5V 가
- (3) 24V DC
24V
- (4) AC FUSE 250V 1A FUSE ()
- (5) 24V
()
- (6) NX70-POWRER1, NX70-POWER2 , AC110V

2-5. ,

(1)



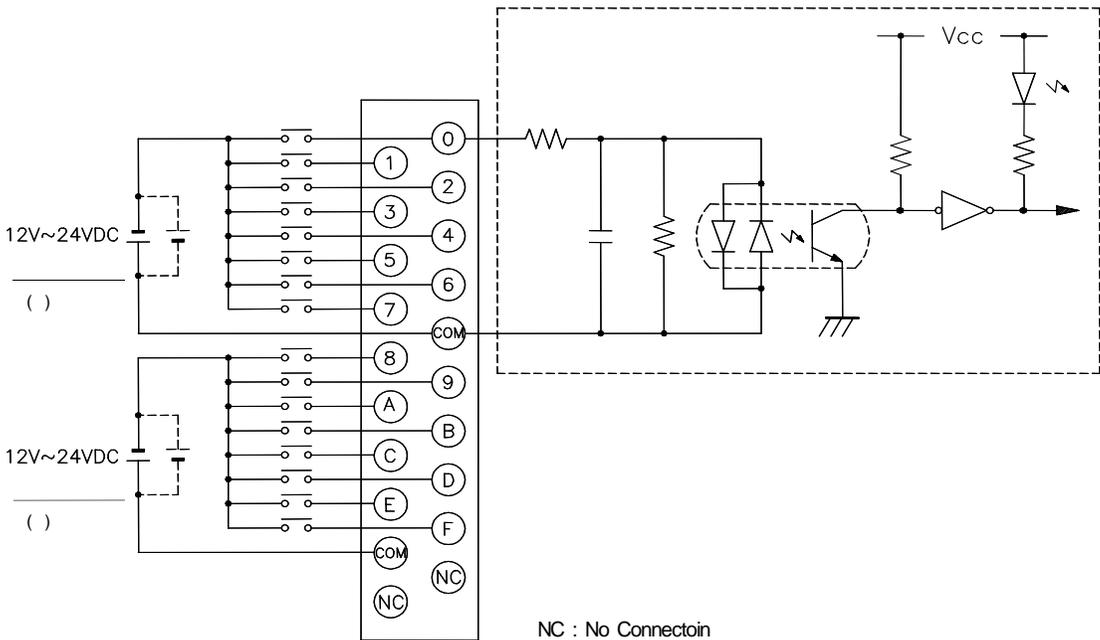
LED
ON/ OFF
(20P)

M3.5
「4-4. TYPE」
32 (20 x 2)

PIN
「4-5. TYPE」
(COVER)

(2)

		DC	
		NX70-X16D (CPL93023)	NX70-X16D1 (CPL93033)
		16	
		12 ~ 24V DC	24V DC
		10.2 ~ 26.4V DC	21.6V ~ 26.4V DC
		10mA	
ON		9.6V	20V
OFF		2.5V	7V
		3K	
	OFF ON	2ms	
	ON OFF	2ms	
(5V)		50mA	
COMMON		8 / 1COM (+, -)	
		LED	
		(M3.0)	
		0.5 1.25 mm ²	
		160g	
		(A) Type	



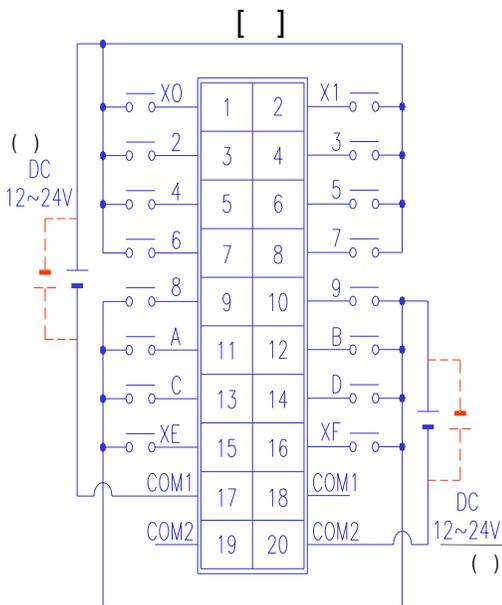
NC : No Connectoin

() NX70-X16D1

24V DC

		DC	
		NX70-X32D (CPL93024)	NX70-X32D1 (CPL93034)
		32	
		12 ~ 24V DC	24V DC
		10.2 ~ 26.4V DC	21.6V ~ 26.4V DC
		10mA	
ON / ON		9.6V	20V
OFF / OFF		2.5V	7 V
		3K	
	OFF ON	2ms	
	ON OFF	2ms	
(5V)		90mA	
COMMON		8 / 1COM (+, -)	
		LED	
		(20 x 2)	
		0.2 mm ²	
		130g	
		(B) Type	

(1 20)



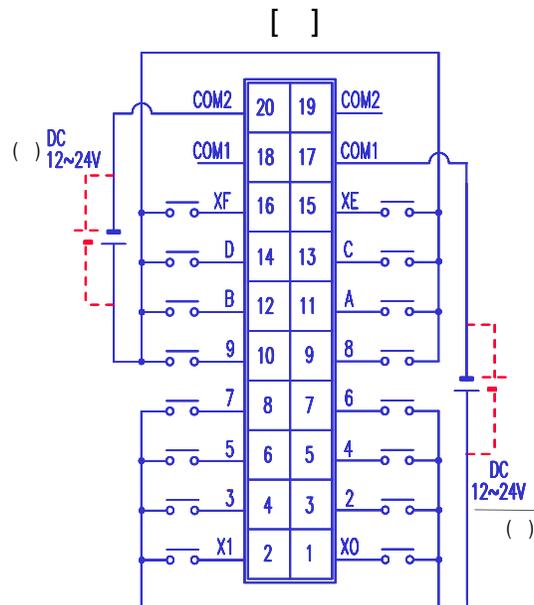
() NX70-X32D1 24V DC

NX70-X16D

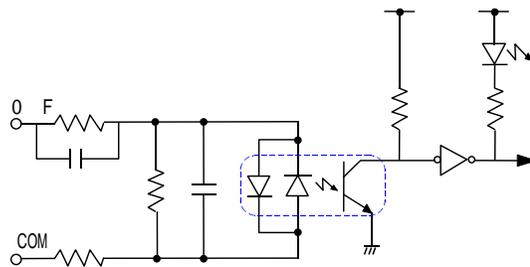
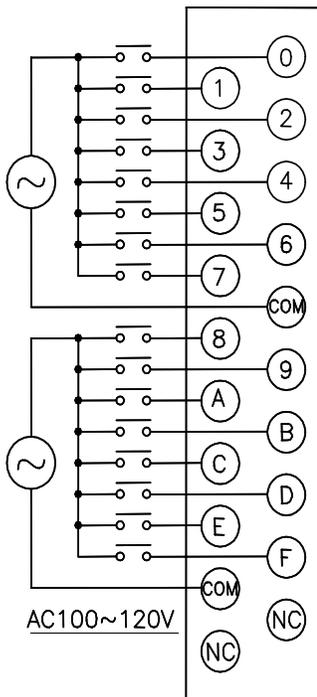
[], []

(CPL8800) Pin Type Ass'y (CPL8880)

(, 「4-5. 」)



		AC	
		NX70-X16A110 (CPL93043)	NX70-X16A220 (CPL93053)
		16	
		AC 100 ~120V	AC 200 ~240V
		AC 85 ~ 132V	AC 170 ~ 264V
		20mA	
ON / ON		80V / 6mA	160V / 6mA
OFF / OFF		30V / 3mA	50V / 3mA
		15K	20K
	OFF ON	15ms	
	ON OFF	15ms	
(5V)		80mA	
COMMON		8 / 1COM	
		LED	
		(M3.0)	
		0.5 1.25 mm ²	
		160g	
		(A) Type	



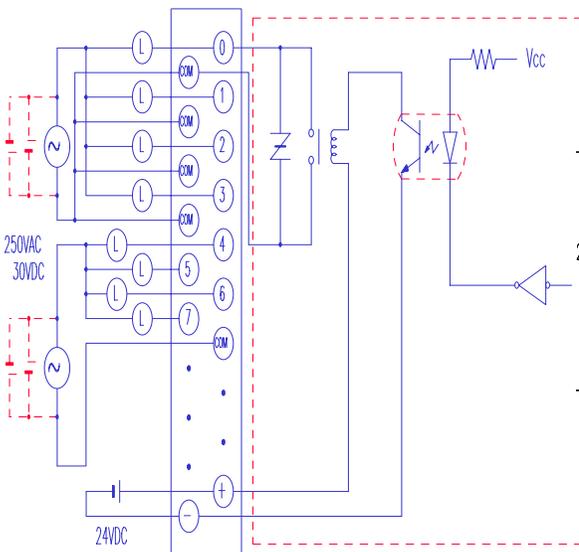
NC : No Connectoin

() NX70-X16A220 : AC 200-240V

(3)

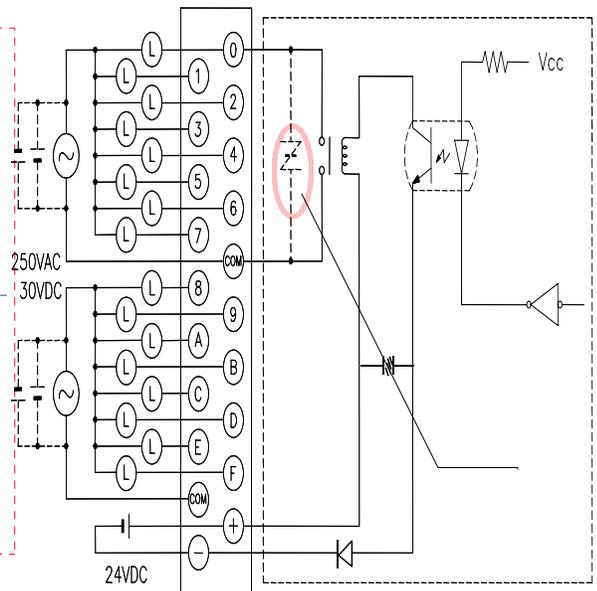
		RELAY		
		NX70-Y8R (CPL93202)	NX70-Y16R (CPL93103)	NX70-Y16RV (CPL93203)
		8	16	
		250V AC, 30V DC		
		85 V ~ 264V AC		
		3A /	1A /	
	OFF ON	10ms		
	ON OFF	10ms		
		24V 150mA	24V 150mA	
(5V)		60mA	100mA	
COMMON		4 /COM, 1 /COM x 4	8 /1COM	
		LED		
		(M3.0)		
		0.5 1.25 mm ²		
		200g	300g	
		(A) Type		

NX70-Y8R

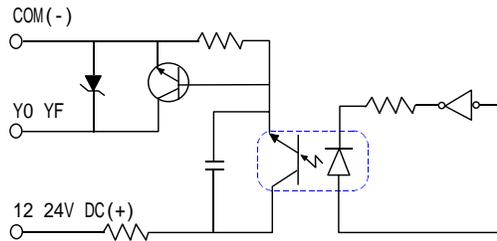
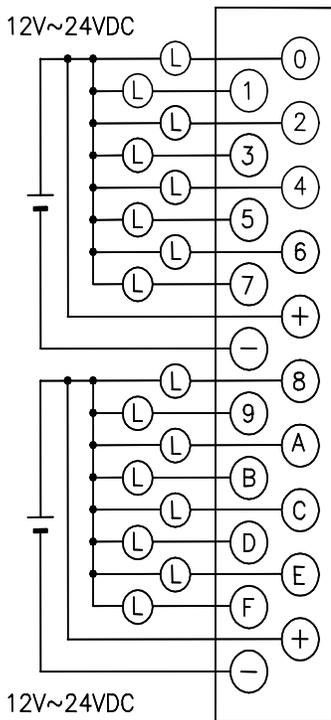


NX70-Y16R :

NX70-Y16RV :



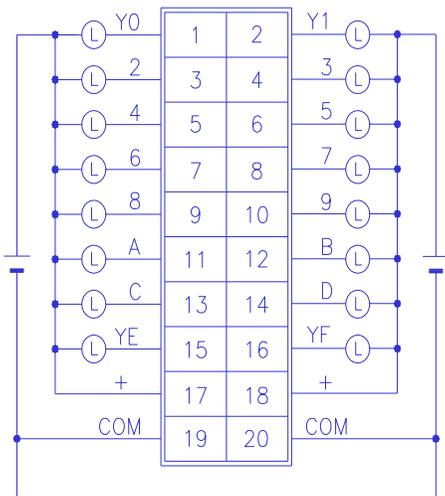
		TR (NPN)
		NX70-Y16T (CPL93483)
		16
		12 ~ 24V DC
		10 ~ 30V AC
		0.6A /
	OFF	100µA
	OFF ON	1ms
	ON OFF	1ms
	(5V)	80mA
	COMMON	8 /1COM(-)
		LED
		(M3.0)
		0.5 1.25 mm ²
		160g
		(A) Ttype



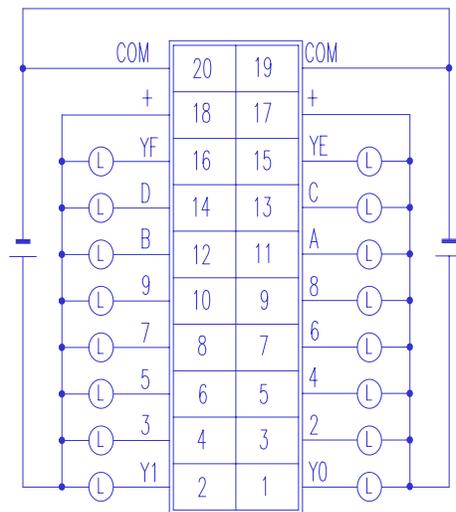
		TR
		NX70-Y32T (NPN) (CPL93484)
		32
		12 ~ 24V DC
		10 ~ 30V AC
		0.4A /
OFF		100µA
	OFF ON	1ms
	ON OFF	1ms
(5V)		140mA
COMMON		16 / 1COM (-)
		LED
		(20 x 2)
		0.2 mm ²
		120g
		(B) Type

(1 20)

[]



[]



[], []

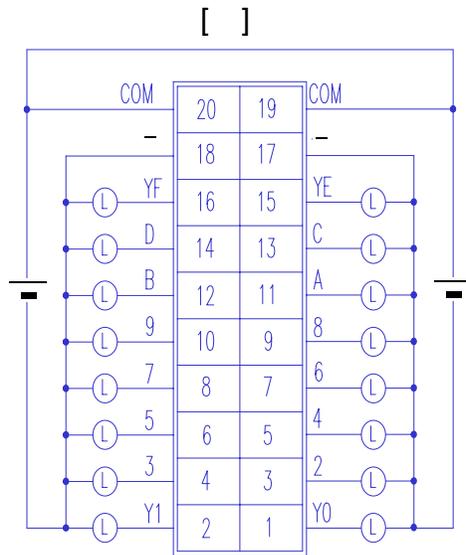
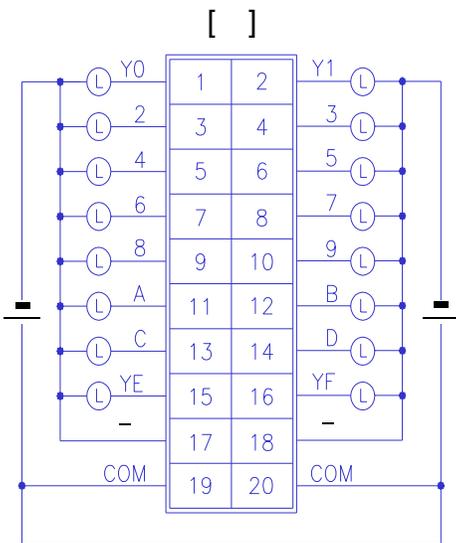
(CPL8810)
, 「4-5.

Pin Type Ass'y (CPL8880)

.)

		TR
		NX70-Y32P (PNP) (CPL93584)
		32
		12 ~ 24V DC
		10 ~ 30V AC
		0.4A /
OFF		100μA
	OFF ON	1ms
	ON OFF	1ms
(5V)		140mA
COMMON		16 / 1COM (+)
		LED
		(20 x 2)
		0.2 mm ²
		120g
		(B) Type

(1 20)



[], []

(CPL8810) Pin Type Ass'y (CPL8880)

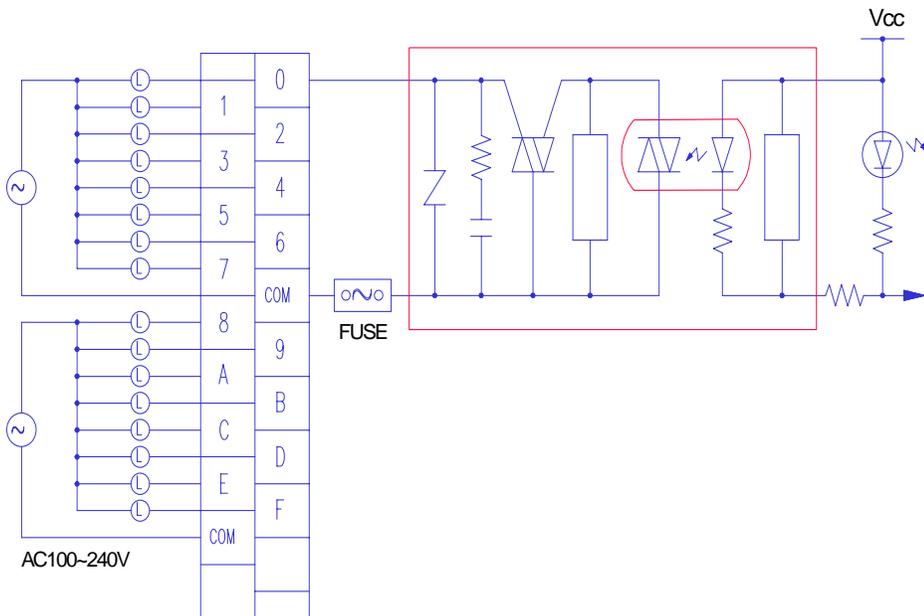
, 「4-5. 」)

NPN (NX70-Y32T)

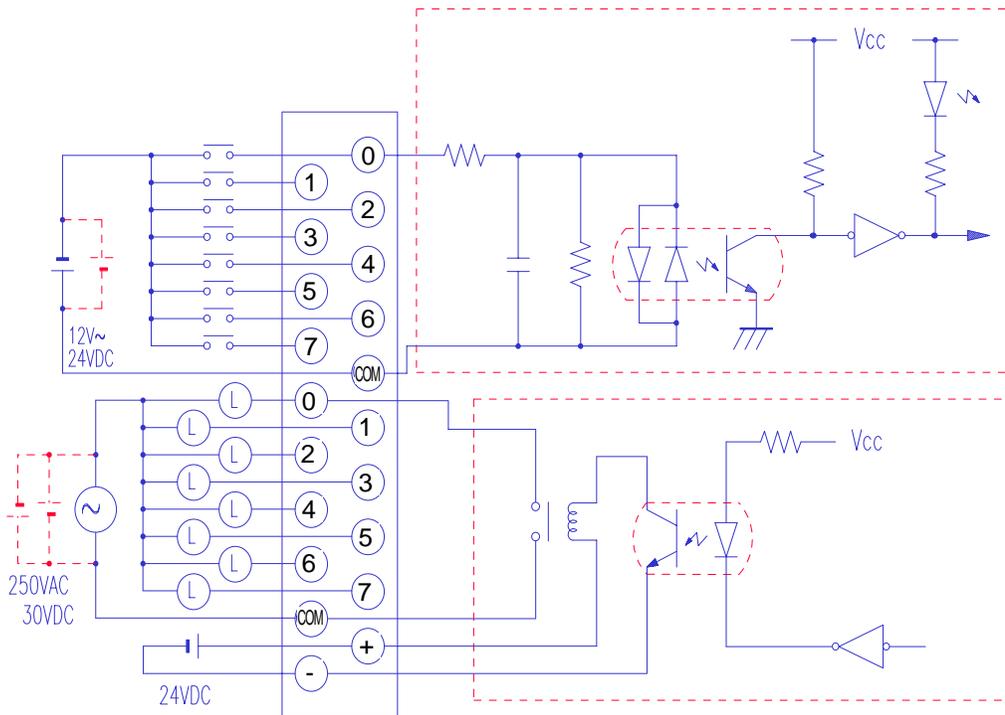
17, 18 : - (VDC-)

19, 20 : COM (VDC+)

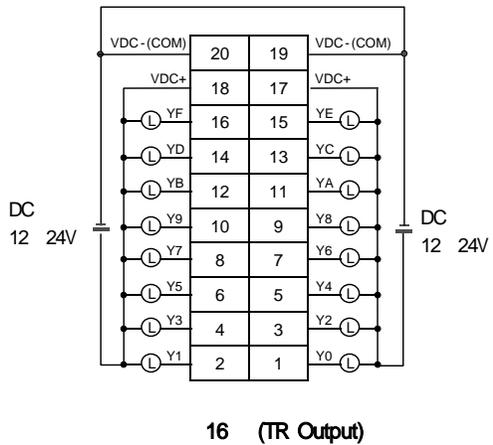
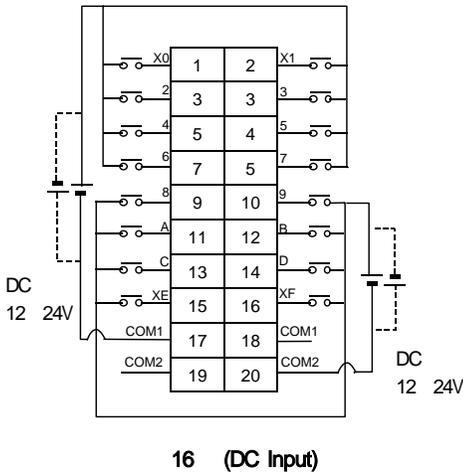
		SSR
		NX70-Y16SSR (CPL93703)
		16
		S S R
		100 ~ 240V AC
		85 ~ 264V AC
		0.5A /
	OFF	100μA
	OFF ON	1ms
	ON OFF	0.5 CYCLE + 1ms
	(5V)	250mA
		3A
	COMMON	8 / 1COM
		LED
		(M 3.0)
		0.5 1.25 mm ²
		300g
		(A) Type



		DC / RELAY	
		NX70-XY16 (CPL93088)	
(16)		8 (DC Input)	8 (Relay Output)
		12 ~ 24V DC	
		10.2 ~ 26.4V DC	
		10mA	
/			250V AC, 30V DC, 1A /
ON / ON		9.6V / 4mA	
OFF / OFF		2.5V / 1.5mA	
		3K	
			24V 150mA
	OFF ON	10ms	
	ON OFF	10ms	
(5V)		80mA	
COMMON		8 / 1COM (+, -)	8 /1COM
		LED	
		(M3.0)	
		0.5 1.25 mm ²	
		220g	
		(A) Type	



		DC / TR	
		NX70-XY32	
(32)		16 (DC Input)	16 (TR Output, NPN)
		12 ~ 24V DC	
		10.2 ~ 26.4V DC	
		10mA	
/			12 ~ 24V DC, 0.4A /
ON / ON		9.6V / 4mA	
OFF / OFF		2.5V / 1.5mA	
		3K	
	OFF ON	10ms	1ms
	ON OFF	10ms	1ms
(5V)		120mA	
COMMON		8 / 1COM (+, -)	16 / 1COM (-)
		LED	
		(20 x 2)	
		0.2 mm ²	
		120g	
		(B) Type	



(CPL8880) (DC Input : CPL8800, TR Output :CPL8810) Pin Type Ass'y

3

■

3-1.	42
3-2.	44
3-3.	45
3-4.	46
3-5.	48
3-6.	/	55
3-7.	CPU (Mode)	59
3-8.	CPU	60

3-1.

(Address) Data가

R, L, M, K, F, TC, W

(R)	R0.0 ~ R127.15	- 가 (Local) - 2048 , 128
(L)	L0.0 ~ L63.15	- ,1024 , Loop 0 - 가
	M0.0 ~ M63.15	- , 1024 , Loop 1
(M)	M0.0 ~ M127.15	- - 2048 , 128
(K)	K0.0 ~ K127.15	- 가 - 2048 , 128 - CPU Clear
(F)	F0.0 ~ F15.15	- - 256 , 16
/ (TC)	TC0 ~ TC255 : W2048 (=SV0) ~W2303 (=SV255) : W2304 (=PV0) ~W2559 (=PV255)	- 256 (,) - TC - SV , () PV - SV 0 ~ 65535 가
(W) 1	W0000 ~ W2047 W0~W255	- - Bit 가 - CPU Clear -) W000 ~ W255 가
(W) 2	W3072 W5119	- (CPU Ver2.0) - - Bit 가 - NX70_CPU70p2
(SR)	SR000 ~ SR511	- CPU , RTC

R, L, M, K, F, TC Bit, Word 가 가
W Word 가
L() 가
K,W, Timer/Counter PV Register Data가

3-2.

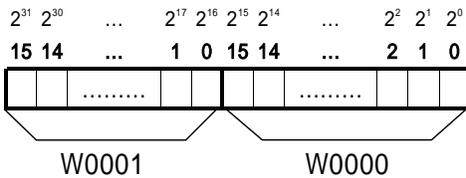
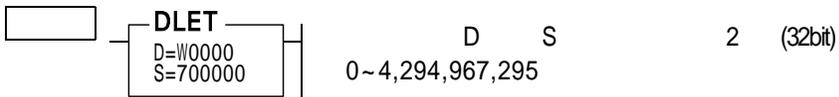
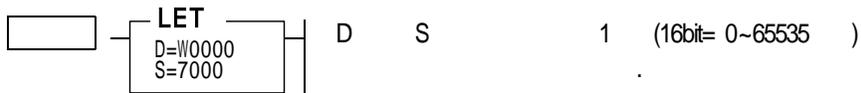
가 32bit

GPC5
'Double'

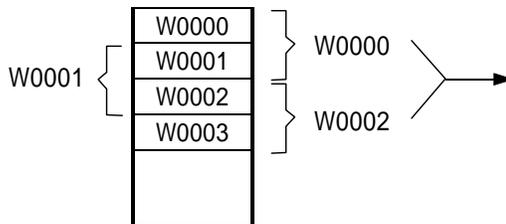
'Ctrl+T'

'D' 가

1)

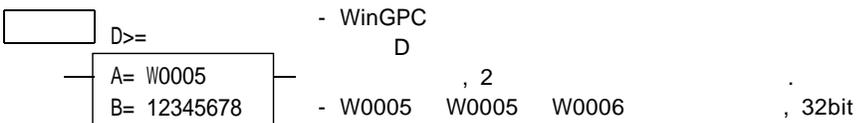
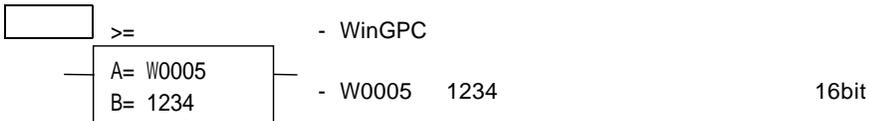


, W0 W0 W1 W0 LSB , W1 MSB
, W1 W1 W2가 가

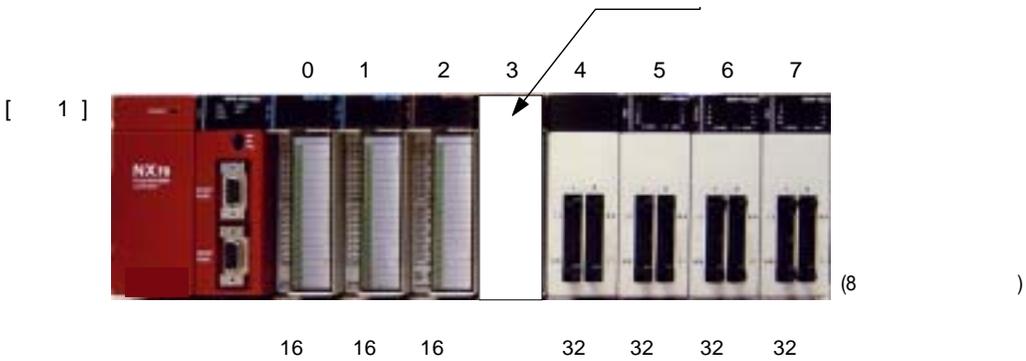


2)

(WinGPC)

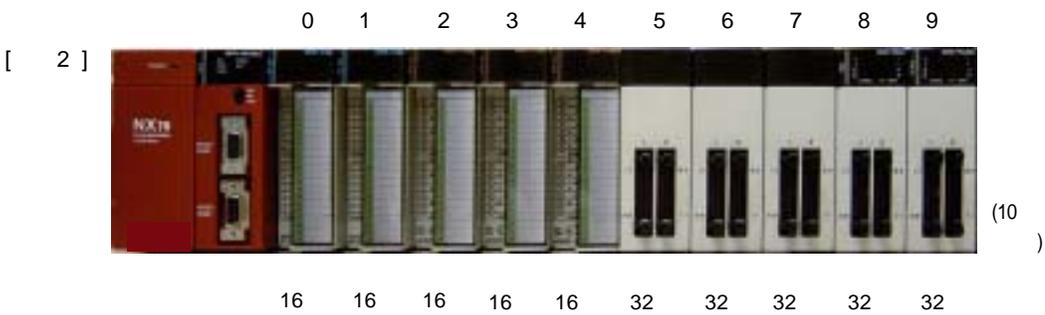


3-4.



()

		00	01	02	03	04	05	06	07
	CPU	R0	R1	R2		R3 R4	R5 R6	R7 R8	R9 R10
		R0.0	R1.0	R2.0		R3.0	R5.0	R7.0	R9.0
		R0.1	R1.1	R2.1		R3.1	R5.1	R7.1	R9.1
		R0.2	R1.2	R2.2		R3.2	R5.2	R7.2	R9.2
		⋮	⋮	⋮		⋮	⋮	⋮	⋮
		R0.15	R1.15	R2.15		R4.15	R6.15	R8.15	R10.15



()

		00	01	02	03	04	05	06	07	08	09
	CPU	R0	R1	R2	R3	R4	R5 R6	R7 R8	R9 R10	R11 R12	R13 R14
		R0.0	R1.0	R2.0	R3.0	R4.0	R5.0	R7.0	R9.0	R11.0	R13.0
		R0.1	R1.1	R2.1	R3.1	R4.1	R5.1	R7.1	R9.1	R11.1	R13.1
		R0.2	R1.2	R2.2	R3.2	R4.2	R5.2	R7.2	R9.2	R11.2	R13.2
		⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
		R0.15	R1.15	R2.15	R3.15	R4.15	R6.15	R8.15	R10.15	R12.15	R14.15

CPU
 16 1 , 1 1
 16 8bit(0~7) 가
 CPU 가 ()
 (NX-DUMMY)
 (CPU) 가
 (, NX-CPU70p)

	NX70-X16D	1	1	
	NX70-X16D1	1	1	
	NX70-X16A110	1	1	
	NX70-X16A220	1	1	
	NX70-X32D	2	2	
	NX70-X32D1	2	2	
	NX70-Y8R	1		1
	NX70-Y16R	1		1
	NX70-Y16RV	1		1
	NX70-Y16T	1		1
	NX70-Y16SSR	1		1
	NX70-Y32T	2		2
	NX70-Y32P	2		2
	NX70-XY16	2	1	1
	NX70-XY32	2	1	1

A/I	NX70-AI8C	8 (1)	8 (1)	
	NX70-AI8V	8 (1)	8 (1)	
	NX70-AI4C	4 (1)	4 (1)	
	NX70-AI4V	4 (1)	4 (1)	
	NX70-RTD4	4 (1)	4 (1)	
	NX70-TC4	4 (1)	4 (1)	
A/O	NX70-AO4C	4 (1)	(1)	4
	NX70-AO4V	4 (1)	(1)	4
	NX70-AO2C	2 (1)	(1)	2
	NX70-AO2V	2 (1)	(1)	2
	NX70-HSC1	2	1	1
	NX70-HSC2	2	1	1
	NX70-HSC4	4	2	2
	NX70-PULSE4	4	2	2
	NX70-POS12	4	2	2
	NX70-POS14	8	4	4
		NX70-CCU+	0	-
NX70-SCU		2	1	1
NX70-MWLink		0	-	-
NX70-DNS		0	-	-

) - ()

NX70 PLC N70 PLC



- N70 PLC NX70 PLC CPU, POWER
- ex1) NX70 (NX70-BASE02 NX70-BASE12) N70 CPU(CPL9215..) POWER (CPL9631..)
- ex2) NX70 (NX70-BASE02 NX70-BASE12) N70 I/O
- ex3) N70 (CPL9502 CPL9508) NX70 CPU POWER

3-5.

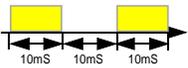
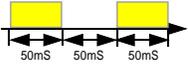
1. F000 F015

F000	/	/ ,
F001	/Clock	, ,Carry Flag
F002~F007	Link	Link , ,
F008~F010	Remote	Remote Flag,
F011~F013		, RTC ,
F014	PID	PID (0~3)
F015	PID	PID (4~7)

2. F000 (F0.0 F0.15)

F0.00		ON
F0.01	CPU ROM (ROM CheckSum)	Error 가 ROM ON ,
F0.02	CPU RAM	ON RAM ON .
F0.03		가 ON , Error ON,
F0.04		CPU가 (RUN) Error ON,
F0.05	I/O	R64 ON
F0.06		Remote CPU RUN 가 ON 가 RUN
F0.07	()	CPU ON , Error 가 (RUN)
F0.08		CPU OFF (Input Update No)
F0.09		CPU OFF 가 OFF(Output Update No) ,
F0.10	OFF	CPU OFF(Output Enable No)
F0.11		ON
F0.12		1 ON
F0.13		ON
F0.14	(RUN)	(RUN) ON , 가
F0.15	CPU가 ON	CPU가 (RUN) ON OFF , (Stop) (Pause) OFF .

3. F001 (F001.0 F001.15)

F1.0	1 ON	STOP RUN 1 ON	
F1.1		ON/OFF (1SCAN ON, 1SCAN OFF)	
F1.2	0.02	10ms : ON, 10ms : OFF 	
F1.3	0.1	50ms : ON, 50ms : OFF 	
F1.4	1	500ms : ON, 500ms : OFF 	
F1.5		20ms OFF ON	
F1.6	CPU	CPU 가 RUN (RUN) ON) CPU 가 Remote RUN F0.15 .	
F1.7	K	K 가 , ON	
F1.8	()	가 ON	
F1.9		가 0 ON	
F1.10		ON	
F1.11	Reserved()		
F1.12	W		
F1.13	Reserved()		
F1.14	Reserved()		
F1.15	Reserved()		

F001 16 CPU
, (, F001.05 가 OFF () .)

4. F011 : COM2 (CPU70p2)

F11.00		1:
F11.01		1:
F11.02	ASCII	1:
F11.03	ASCII	1:
F11.04		1:
F11.05	(Read '1' SET)	1:
F11.06		1:
F11.07		1:
F11.08	ASCII ASCII	1: ASCII
F11.09		1:
F11.10		1:
F11.11	ODD/EVEN	0: ODD, 1: EVEN
F11.12	7 8 Bit	0: 8 , 1: 7
F11.13	Port 2	0: ASCII, 1: HEX , 2)
F11.14	COM2 Modbus	MODBUS ON (V2.30)
F11.15	Reserved()	

5. F012 :

F12.00	RTC	RTC ON .
F12.01	REMOTE MAP	REMOTE I/O MAP ON .
F12.02	COM1 Modbus	COM1 Port Modbus RTU Set (V2.0)
F12.03	FLASH ,	FLASH 가 ON .
F12.05	Battery	가 , Backup Error LED 가 .
F12.07		ON .
F12.08		COM2
F12.09	COM2 Modbus	COM2 Modbus
F12.10	RTC	RTC ON (OFF .)
F12.11	FLASH	F12.15 ON FLASH OFF .
F12.12	EEPROM	EEPROM RAM ON
F12.13	RTC 1	/ / / ON .
F12.14	RTC 2	/ / ON . OFF
F12.15	FLASH	FLASH , ON . : OFF .

6. F014 F015 : PID

F14.00	PID Loop0	Loop 0 1=PID , 0=PID
F14.01		1= , 0=
F14.02		PID 1= , 0=
F14.03		PID 1= , 0=
F14.04~ F14.07	PID Loop1	Loop 1 PID (Loop0)
F14.08~ F14.11	PID Loop2	Loop 2 PID (Loop0)
F14.12~ F14.15	PID Loop3	Loop 3 PID (Loop0)
F15.00~ F15.03	PID Loop4	Loop 4 PID (Loop0)
F15.04~ F15.07	PID Loop5	Loop 5 PID (Loop0)
F15.08~ F15.11	PID Loop6	Loop 6 PID (Loop0)
F15.12~ F15.15	PID Loop7	Loop 7 PID (Loop0)

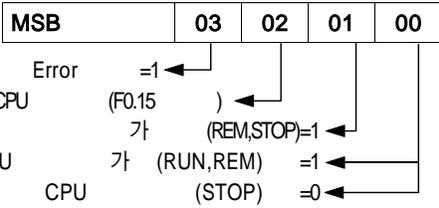
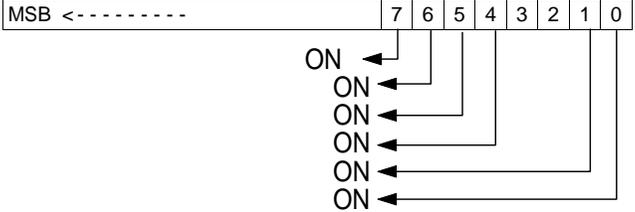
7. SR

SR SR000(\$0C00) ~ SR511(\$0DFF) ,
가

1) SR000 SR511

SR000 SR004	W2560 W2564	CPU	CPU
SR005 SR007	W2565 W2567	Reserved()	
SR008	W2568	PID	PID
SR009 SR016	W2569 W2576	Reserved()	
SR017 SR048	W2577 W2608		
SR049 SR288	W2609 W2848	Reserved()	
SR289 SR297	W2849 W2857		
SR298 SR373	W2858 W2933		COM2 Protocol
SR374 SR511	W2934 W3071	Reserved()	

2) SR000(W2560) SR029(W2589) :
 (CPU, ,)

SR000	W2560	CPU ID	CPU (CPU ID Number) 8bit 0~223 , 255 Default 가
SR001	W2561	CPU	CPU가  , Stop=010, REM/Pause=011, REM/RUN=111, RUN/RUN=101
SR002	W2562		가 (: mSec)
SR003	W2563		, (mSec)
SR004	W2564		
SR005~SR007	W2565~W2567	Reserved ()	
SR008	W2568	PID	PID
SR009~SR016	W2569~W2576	Remote I/O	Remote Master , Complement ()
SR017	W2577		F0.0 ON , 
SR018	W2578		
SR019	W2579	Reserved	
SR020	W2580		
SR021	W2581		
SR022	W2582		
SR023	W2583		
SR024~SR029	W2584~W2589	Reserved ()	

3) SR30(W2590) SR48(W2608) :

SR030	W2590		Bit 0 = 가 ON. Bit 1 = 가 255 Bit 2 = 가 ON Bit 3 = INPR/ OOUTR 가 ON Bit 4 = ON Bit 5 = ON Bit 6 = ON Bit 7 = ON Bit 8 = 가 ON Bit 9 = JMP CALL 가 63 CALL (SBR~RET) JMP/ CALL LBL/ SBR ON. Bit10 = LBL 가 63 ON Bit11 = JMPS/ JMPE ON Bit12 = FOR/ NEXT 4 Loop ON Bit13 = SBR/ RET 가 63 ON Bit14 = INT/ RETI ON Bit15 = END ON
SR031	W2591	-	
SR032	W2592	CPU	Error
SR033	W2593		T/C Error
SR034	W2594		Error
SR035	W2595		I/O Error
SR036	W2596		Error
SR037	W2597		
SR038	W2598		
SR039	W2599		
SR040	W2600		
SR041	W2601		JMP/Call Error
SR042	W2602		LBL Error
SR043	W2603		JMPS/JMPE Error
SR044	W2604		FOR/NEXT Error
SR045	W2605		SBR/RET Error
SR046	W2606		INT/RETI Error
SR047	W2607		END Error
SR048	W2608		

4) SR49(W2609) SR251(W2811) :

SR049~ SR288	W2609~ W2848	Reserved()	
-----------------	-----------------	-------------	--

5) SR289 SR297(W2849 W2857)

(RTC) / BCD ,

			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SR289	W2849	(4 BCD)			x	x	x	x	x	x	x	x	x	x	x	x	x	
SR290	W2850	(日):			x	x	x	x	x	x					x	x	x	
SR291	W2851	(年): (月)		x	x	x	x	x	x	x				x	x	x	x	
SR292	W2852	(秒):00			x	x	x	x	x	x								
SR293	W2853	(時): (分)			x	x	x	x	x	x		x	x	x	x	x	x	
SR294	W2854	(日):			x	x	x	x	x	x					x	x	x	
SR295	W2855	(年): (月)		x	x	x	x	x	x	x				x	x	x	x	
SR296	W2856	(秒):00			x	x	x	x	x	x								
SR297	W2857	(時): (分)			x	x	x	x	x	x		x	x	x	x	x	x	

) 'x' Data가 F12.13 ON , , , F12.14 ON

6) SR298 SR373(W2858 W2933)

가 COM2 (Modular Jack) PLC

SR298~ SR333	W2858 ~ W2893		36 , 3370
SR334~ SR369	W2894 ~ W2929		36 , 3406
SR370	W2930		Byte
SR371	W2931		Byte
SR372	W2932		ASCII
SR373	W2933		(Byte)

7) SR

SR 가

3-6. / (TC0-255)

1. / ,

	(SV)	(PV)
0	W2048	W2304
1	W2049	W2305
2	W2050	W2306
3	W2051	W2307
4	W2052	W2308
5	W2053	W2309
6	W2054	W2310
7	W2055	W2311
8	W2056	W2312
9	W2057	W2313
10	W2058	W2314
11	W2059	W2315
12	W2060	W2316
13	W2061	W2317
14	W2062	W2318
15	W2063	W2319
16	W2064	W2320
17	W2065	W2321
18	W2066	W2322
19	W2067	W2323
20	W2068	W2324
21	W2069	W2325
22	W2070	W2326
23	W2071	W2327
24	W2072	W2328
25	W2073	W2329
26	W2074	W2330
27	W2075	W2331
28	W2076	W2332
29	W2077	W2333
30	W2078	W2334
31	W2079	W2335
32	W2080	W2336
33	W2081	W2337
34	W2082	W2338
35	W2083	W2339
36	W2084	W2340
37	W2085	W2341
38	W2086	W2342
39	W2087	W2343

	(SV)	(PV)
40	W2088	W2344
41	W2089	W2345
42	W2090	W2346
43	W2091	W2347
44	W2092	W2348
45	W2093	W2349
46	W2094	W2350
47	W2095	W2351
48	W2096	W2352
49	W2097	W2353
50	W2098	W2354
51	W2099	W2355
52	W2100	W2356
53	W2101	W2357
54	W2102	W2358
55	W2103	W2359
56	W2104	W2360
57	W2105	W2361
58	W2106	W2362
59	W2107	W2363
60	W2108	W2364
61	W2109	W2365
62	W2110	W2366
63	W2111	W2367
64	W2112	W2368
65	W2113	W2369
66	W2114	W2370
67	W2115	W2371
68	W2116	W2372
69	W2117	W2373
70	W2118	W2374
71	W2119	W2375
72	W2120	W2376
73	W2121	W2377
74	W2122	W2378
75	W2123	W2379
76	W2124	W2380
77	W2125	W2381
78	W2126	W2382
79	W2127	W2383

	(SV)	(PV)
80	W2128	W2384
81	W2129	W2385
82	W2130	W2386
83	W2131	W2387
84	W2132	W2388
85	W2133	W2389
86	W2134	W2390
87	W2135	W2391
88	W2136	W2392
89	W2137	W2393
90	W2138	W2394
91	W2139	W2395
92	W2140	W2396
93	W2141	W2397
94	W2142	W2398
95	W2143	W2399
96	W2144	W2400
97	W2145	W2401
98	W2146	W2402
99	W2147	W2403
100	W2148	W2404
101	W2149	W2405
102	W2150	W2406
103	W2151	W2407
104	W2152	W2408
105	W2153	W2409
106	W2154	W2410
107	W2155	W2411
108	W2156	W2412
109	W2157	W2413
110	W2158	W2414
111	W2159	W2415
112	W2160	W2416
113	W2161	W2417
114	W2162	W2418
115	W2163	W2419
116	W2164	W2420
117	W2165	W2421
118	W2166	W2422
119	W2167	W2423

GPC5, WinGPC

W

	(SV)		(PV)		(TC)	
	PGM	WinGPC	PGM	WinGPC	PGM	WinGPC
0	W2048	SV000	W2304	PV000	TIM000	TC000
.....
255	W2303	SV255	W2559	PV255	TIM255	TC255

/ ()

	(SV)	(PV)
120	W2168	W2424
121	W2169	W2425
122	W2170	W2426
123	W2171	W2427
124	W2172	W2428
125	W2173	W2429
126	W2174	W2430
127	W2175	W2431
128	W2176	W2432
129	W2177	W2433
130	W2178	W2434
131	W2179	W2435
132	W2180	W2436
133	W2181	W2437
134	W2182	W2438
135	W2183	W2439
136	W2184	W2440
137	W2185	W2441
138	W2186	W2442
139	W2187	W2443
140	W2188	W2444
141	W2189	W2445
142	W2190	W2446
143	W2191	W2447
144	W2192	W2448
145	W2193	W2449
146	W2194	W2450
147	W2195	W2451
148	W2196	W2452
149	W2197	W2453
150	W2198	W2454
151	W2199	W2455
152	W2200	W2456
153	W2201	W2457
154	W2202	W2458
155	W2203	W2459
156	W2204	W2460
157	W2205	W2461
158	W2206	W2462
159	W2207	W2463
160	W2208	W2464
161	W2209	W2465
162	W2210	W2466
163	W2211	W2467
164	W2212	W2468
165	W2213	W2469

	(SV)	(PV)
166	W2214	W2470
167	W2215	W2471
168	W2216	W2472
169	W2217	W2473
170	W2218	W2474
171	W2219	W2475
172	W2220	W2476
173	W2221	W2477
174	W2222	W2478
175	W2223	W2479
176	W2224	W2480
177	W2225	W2481
178	W2226	W2482
179	W2227	W2483
180	W2228	W2484
181	W2229	W2485
182	W2230	W2486
183	W2231	W2487
184	W2232	W2488
185	W2233	W2489
186	W2234	W2490
187	W2235	W2491
188	W2236	W2492
189	W2237	W2493
190	W2238	W2494
191	W2239	W2495
192	W2240	W2496
193	W2241	W2497
194	W2242	W2498
195	W2243	W2499
196	W2244	W2500
197	W2245	W2501
198	W2246	W2502
199	W2247	W2503
200	W2248	W2504
201	W2249	W2505
202	W2250	W2506
203	W2251	W2507
204	W2252	W2508
205	W2253	W2509
206	W2254	W2510
207	W2255	W2511
208	W2256	W2512
209	W2257	W2513
210	W2258	W2514
211	W2259	W2515

	(SV)	(PV)
212	W2260	W2516
213	W2261	W2517
214	W2262	W2518
215	W2263	W2519
216	W2264	W2520
217	W2265	W2521
218	W2266	W2522
219	W2267	W2523
220	W2268	W2524
221	W2269	W2525
222	W2270	W2526
223	W2271	W2527
224	W2272	W2528
225	W2273	W2529
226	W2274	W2530
227	W2275	W2531
228	W2276	W2532
229	W2277	W2533
230	W2278	W2534
231	W2279	W2535
232	W2280	W2536
233	W2281	W2537
234	W2282	W2538
235	W2283	W2539
236	W2284	W2540
237	W2285	W2541
238	W2286	W2542
239	W2287	W2543
240	W2288	W2544
241	W2289	W2545
242	W2290	W2546
243	W2291	W2747
244	W2292	W2548
245	W2293	W2549
246	W2294	W2550
247	W2295	W2551
248	W2296	W2552
249	W2297	W2553
250	W2298	W2554
251	W2299	W2555
252	W2300	W2556
253	W2301	W2557
254	W2302	W2558
255	W2303	W2559

3

1. (=)

1 16 (=) 32 (=)

2. (Bit)

. 1 0

3. (Byte)

8 0~255(16 :0 FF)

4. (Word)

16 0 65,535 (16 : 0 FFFF)

plus PLC R, M, K, F, W

가

5. (Double Word)

32 0 4,294,967,295 (16 : 0 FFFFFFFF)

" " = " " + " "

) W003

W003() = W003() + W004()

6. (Scan Time)

CPU RUN

1

1

ON/OFF

7. (Edge)

/ , 1 ON

OFF ON

ON

가

ON OFF

OFF

가

8. BCD(Binary Coded Decimal)

1 (Digit) 4

0-9

BCD 16

) 59(BCD)=59(HEX), 32(BCD)=(32HEX)

9. FLASH ROM

ROM(EEPROM)

PLC

1. R(Relay) ... (/ / 가)

2. M(Memory) ... (/ / 가)

PLC CPU가
STOP(PROG.)

3. W(Word) ... (/ / 가)

M 가 , OFF
:()

4. K(Keep) ... (/ / 가)

OFF

5. F(Flag) ... ()

PLC RUN / STOP(PROG.)

6. 65,535(FFFFh) ...

65,535 ()
4,294,967,295(2³²)
0 65,535 K, M, R, W

7. ...

K, W K, W W

8. A+B=C, 34x45=D, A1>C1, ...

R, M, W, K , R

9. ...

M, K, R : W

10. / ...

W2048 W2303 SV0 SV255 /

11. / ...

1) W2304 W2559 , PV0 PV255 /
STOP(PROG.)

2) (PV) OFF

3-7. CPU (mode)

CPU ?
 CPU가 RUN /REMOTE/ PROG 가 PLC

RUN ()

R UN plus CPU RAM (FLASH ROM)

STOP ()

S TOP STOP / / OFF
 (FLASH)

PAUSE ()

P AUSE 1 . STOP Data

ERROR ()

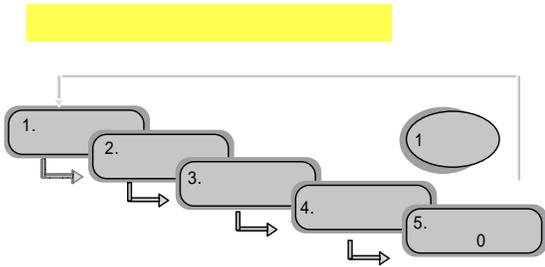
E RROR Plus ("p"가 CPU) CPU 가
 가 CPU
 OFF 가
 OFF ON , PROG. INITIALIZE KEY Error

CPU :

		LED				INITIALIZE	OFF ON
		RUN LED	PROG LED				
RUN	RUN			가	가	0	RUN
	STOP			가	가	0	
REMOTE	RUN			가	가	0	RUN
	PAUSE			가	가	0	PAUSE
PROG.	STOP			가	가	0	STOP

PROG. LED가 가
 PROG. , INITIALIZE ERROR CLEAR
 가 REMOTE OFF ON 가
 REMOTE

3-8. CPU



PLC
CPU 1 5
1 "1"

1.

(Working RAM)

2.

3.

가 ON/ OFF

4.

ON/OFF

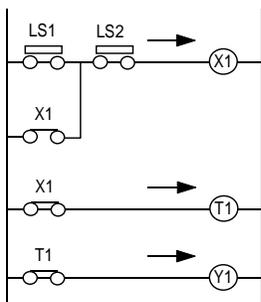
(1)

5.

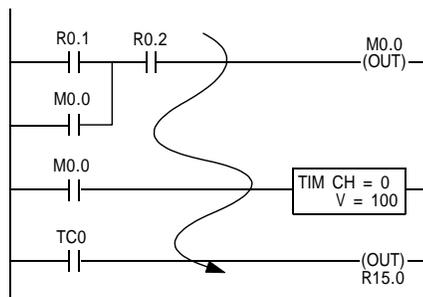
0 ()

PLC
, PLC

가



()



PLC
()

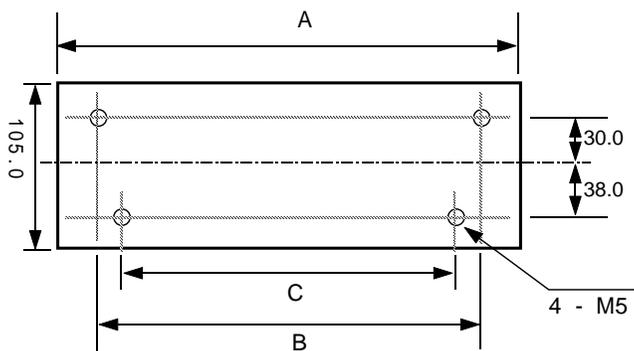
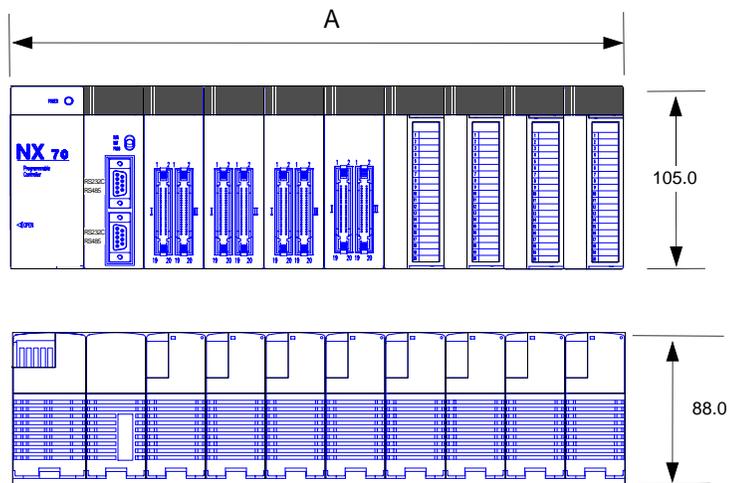
4

4-1.	62
(1)	62
4-2.	64
(1)	64
(2)	65
4-3.	66
(1)	66
(2)	69
(3)	70
4-4.	Type	70
4-5.	Type	71
(1)	71
(2)	73
4-6.	74
4-7. N-plus CPU	75
4-8. EEPROM	76
(1) EEPROM Backup	?	76
(2)	76
(3)	76

4-1.

(1)

(: mm)



(mm)

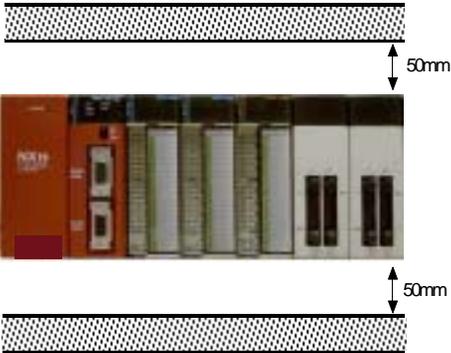
		(A)	(B)	(C)
2	NX70-BASE02	157.2	128.6	114.6
3	NX70-BASE03	192.4	163.8	149.8
5	NX70-BASE05	262.8	234.2	220.2
6	NX70-BASE06	298.0	269.4	255.4
8	NX70-BASE08	368.4	339.8	325.8
10	NX70-BASE10	438.8	410.2	396.2
12	NX70-BASE12	508.6	480.6	466.6

(Control Box)

-
-
-
- ()

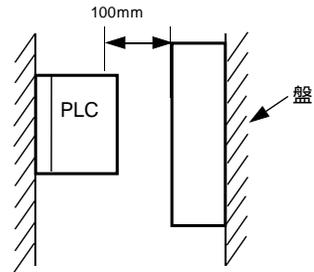
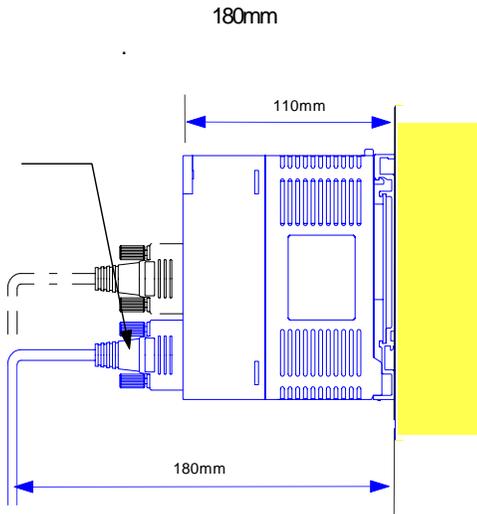
PLC

100mm



(TOOL)

CPU

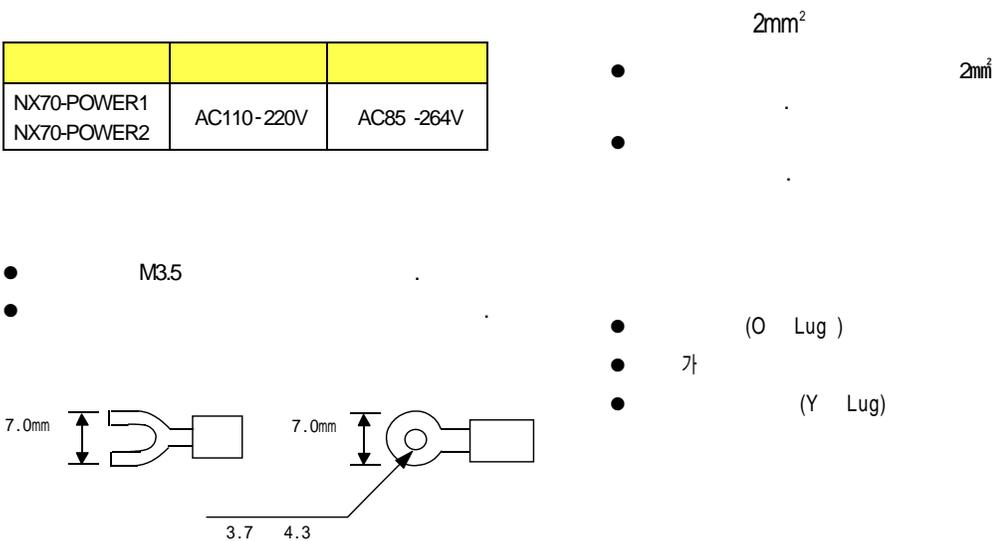
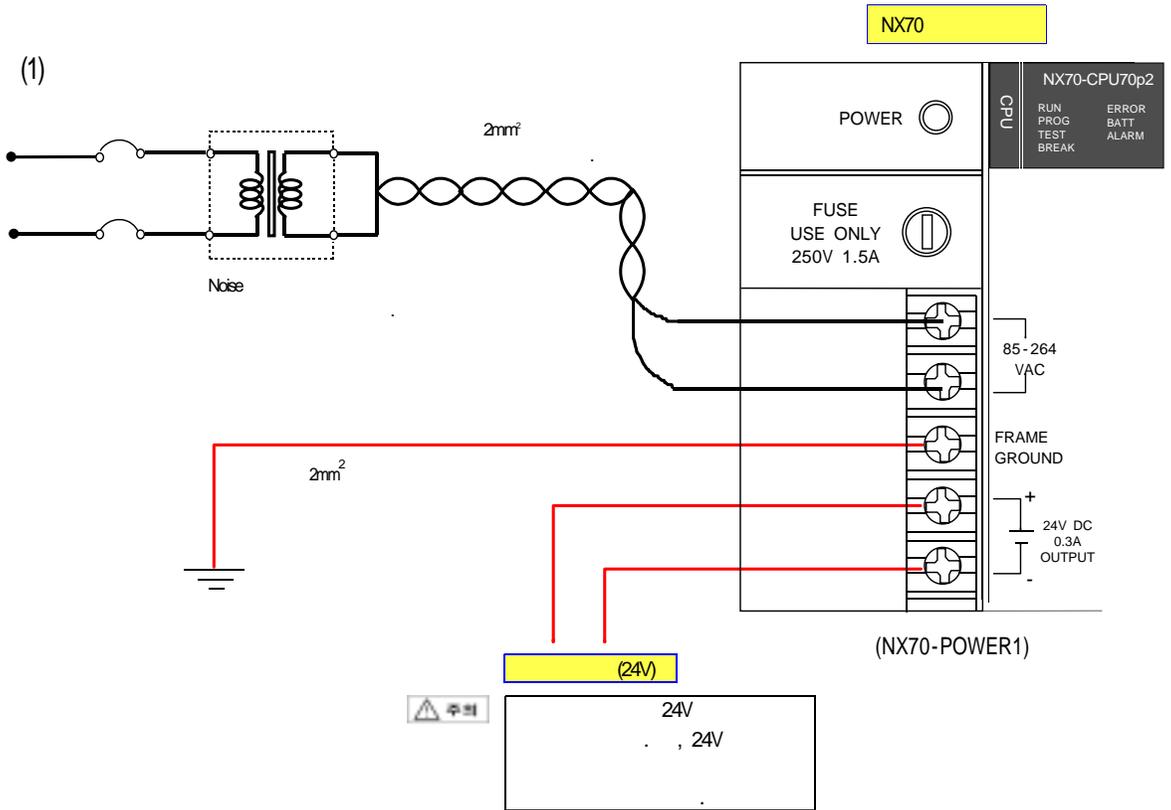


가 0 55
 가 30 85%RH
 가
 가 , 가 가
 가 ,
 가 ,
 가 ,
 가

가

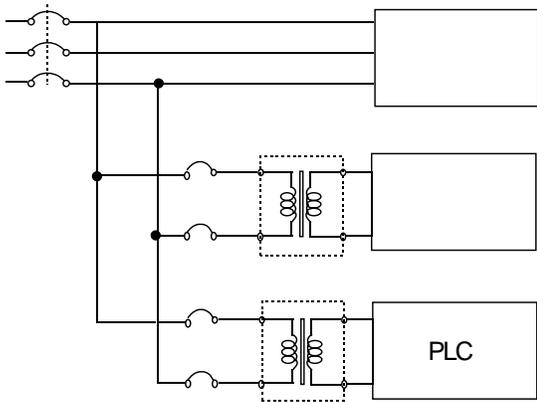
(100mm)

4-2.



(2)

● PLC,



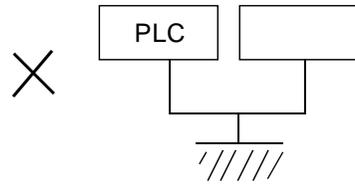
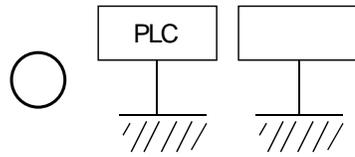
● Frame Ground (FG) , 大地

● 2mm² 3 100

● 接地点 가 PLC

● 가 가

- 가
- 가

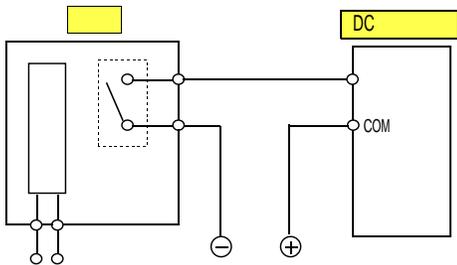


4-3.

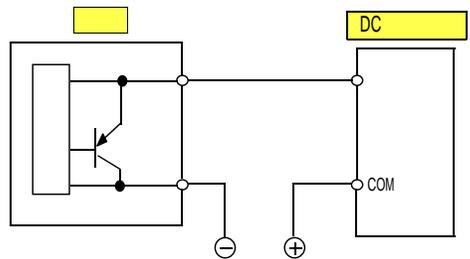
(1)

1. ON , 가 .
2. ,

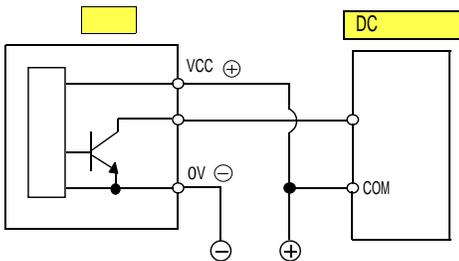
1)



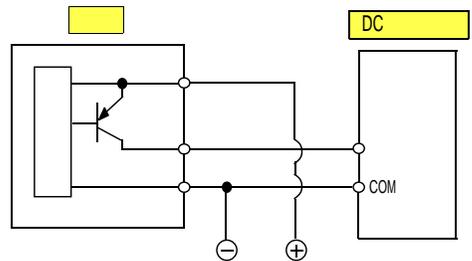
4) 2



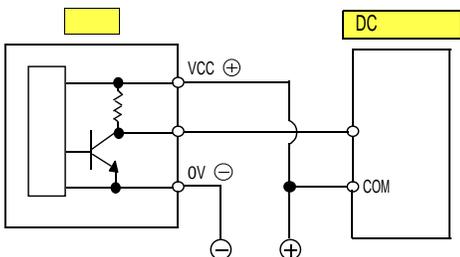
2) NPN



5) PNP

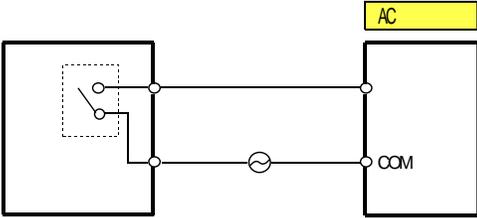


3)

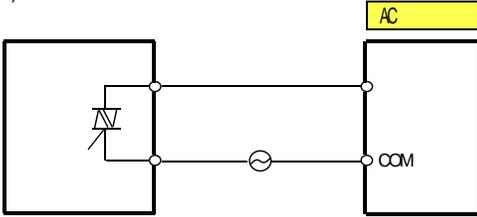


AC

1)



2)



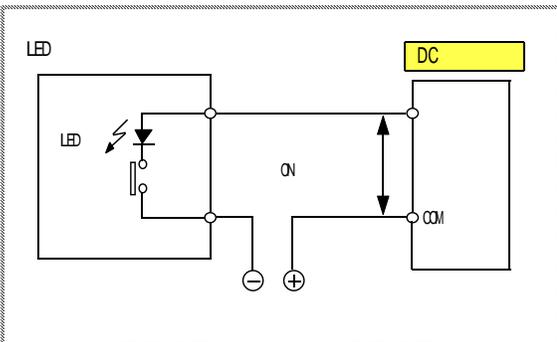
LED가

LED가

PLC

ON

LED가



2

2

PLC

OFF가

DC 12-24V
(OFF 2.5V, 3k)

2

DC

R

COM

⊖ ⊕

I : (mA)
R : (k)

OFF 2.5V COM
2.5V 가 R
3k

$$I \times \frac{3R}{3 + R} = 2.5 \quad R = \frac{7.5}{3I - 2.5} (k)$$

W

$$W = \frac{(\quad)^2}{R}$$

3 5

LED가

LED가

LED가

PLC

OFF

DC 12-24V
(OFF 25V, 3k)

LED

DC

COM

r : (k)

R : (k)

OFF 2.5V 24V ,

$$I = \frac{24 - 2.5}{r}$$

R . I 2

$$R = \frac{7.5}{31-2.5} \text{ (k) } \quad W = \frac{(\quad)^2}{R} \times (3 \ 5 \)$$

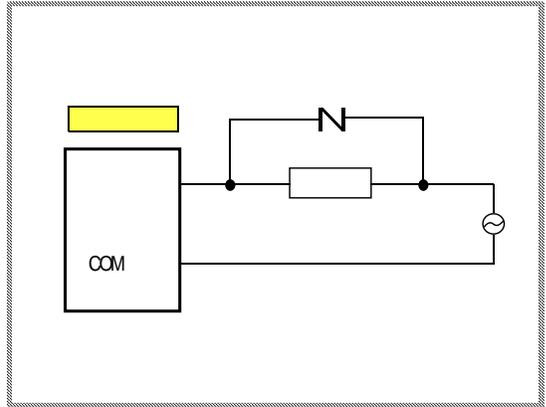
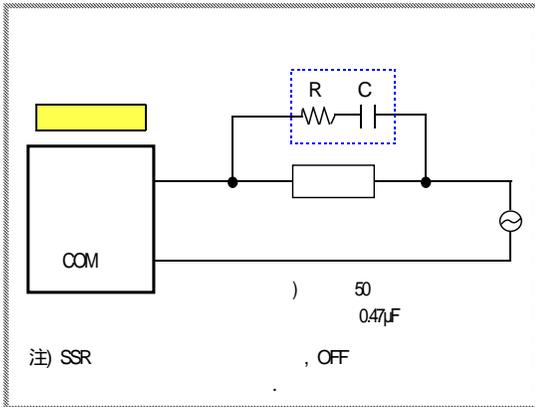
(2)

1. 가 ON
2. ,
3. Common

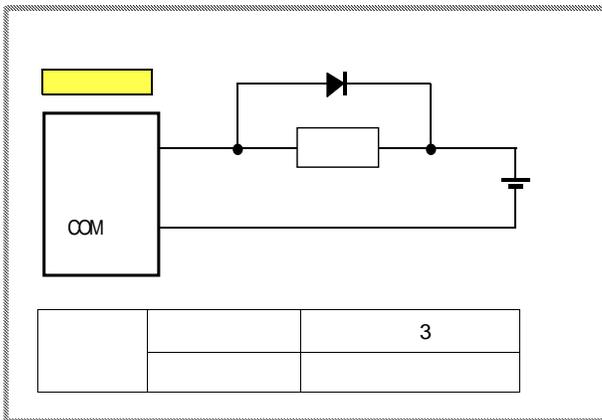
DC

가

1) AC ()



2) DC

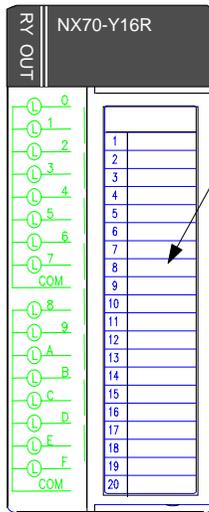
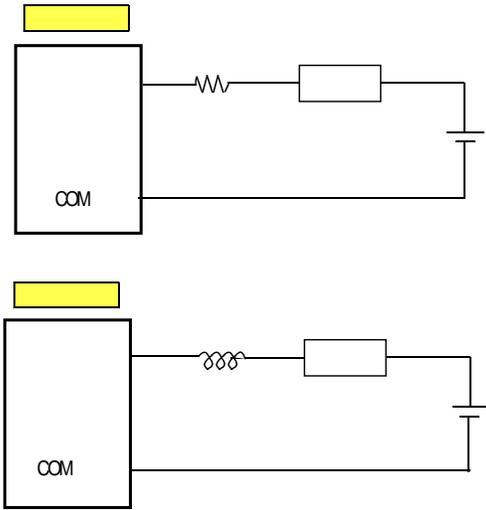


(3)

가

가

100mm



- 가
- 가
- , 가

1

4-4.

SSR

가 OFF

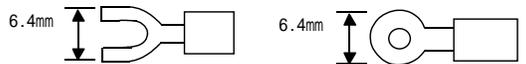
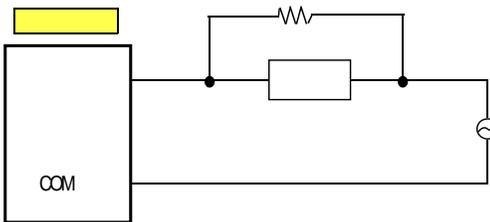
가

가

M3.0

NX70 PLC
M3.0

()



4

4-5.

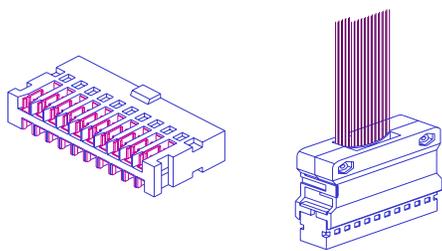
(1)

NX70 PLC 32 (NX70-X32D, NX70-X32D1)
 32 (NX70-Y32T, NX70-Y32P) , 20 MIL
 Type

- 1) _____ Pin _____
 - 2) _____
- 2가 가 . ()

1) PIN

PIN



I/O (Pin)	ASSY ()	CPL8880	· 20 1) PIN 20 2) 3)
-----------	----------	---------	-------------------------------

32	NX70-X32D (DC IN 32 , 12-24V) NX70-X32D1(DC IN 32), 24V)
32	NX70-Y32T (TR OUT 32 , NPN) NX70-Y32P (TR OUT 32 , PNP)

2)

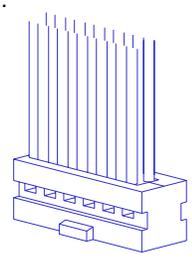
()

20

가 20가

가

1.5m



ASSY	CPL8800	DC IN 32 ,	1.5m
	CPL8810	TR OUT 32	1.5m

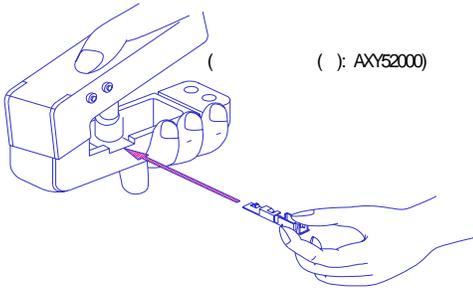
32	NX70-X32D (DC IN 32 , 12-24V) NX70-X32D1(DC IN 32), 24V)
32	NX70-Y32T (TR OUT 32 , NPN) NX70-Y32P (TR OUT 32 , PNP)

()

		()
	NX70-X16D NX70-X16D1 NX70-X32D NX70-X32D1 NX70-X16A110 NX70-X16A220	(CPL93023) (CPL93033) (CPL93024) (CPL93034) (CPL93043) (CPL93053)
	NX70-Y8R NX70-Y16R NX70-Y16RV NX70-Y16T NX70-Y32T NX70-Y32P NX70-Y16SSR	(CPL93202) (CPL93103) (CPL93203) (CPL93483) (CPL93484) (CPL93584) (CPL93703)
	NX70-XY16 NX70-XY32	(CPL93088) -

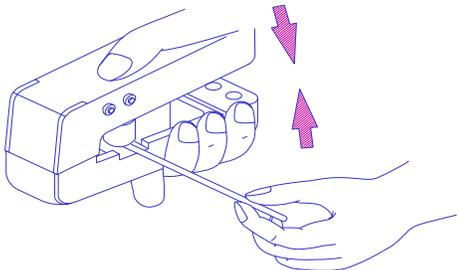
PIN

(1)

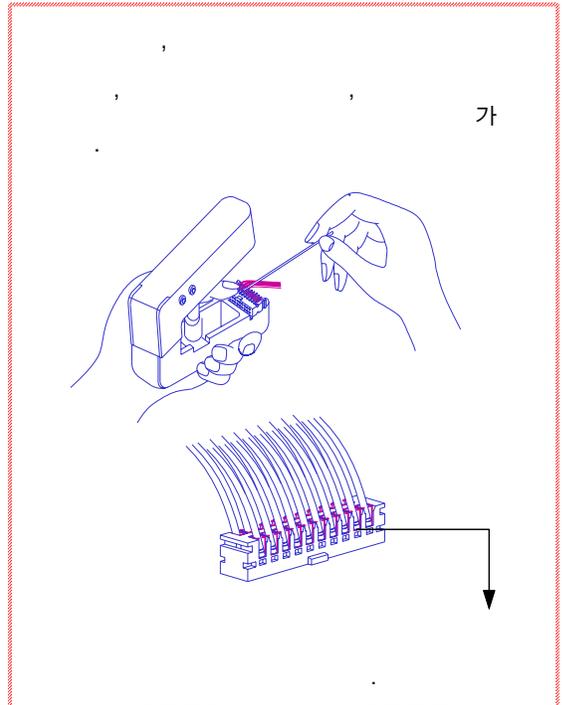
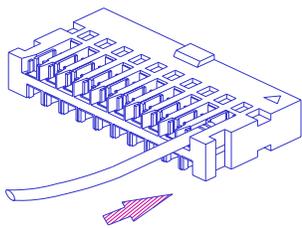


(2)

가



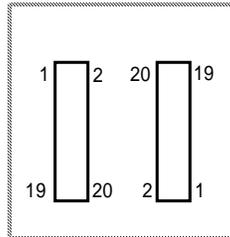
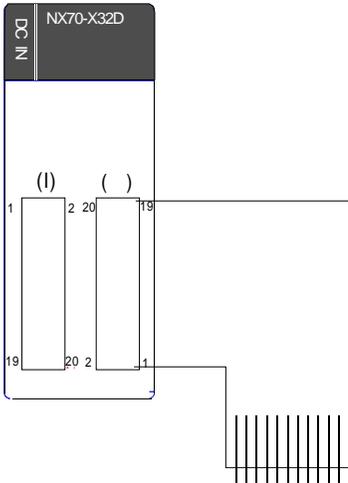
(3)



(2)

No. I/O

32



(1.5m)	CPL8800	DC IN 32 (NX70-X32D) (NX70-X32D1)
	CPL8810	TR OUT 32 (NX70-YX32T) (NX70-YX32P)

No. I/O (32)

(I)

()

	NX70-X32D NX70-X32D1	NX70-Y32T NX70-Y32P
1	X 0	Y 0
2	X 1	Y 1
3	X 2	Y 2
4	X 3	Y 3
5	X 4	Y 4
6	X 5	Y 5
7	X 6	Y 6
8	X 7	Y 7
9	X 8	Y 8
10	X 9	Y 9
11	X A	Y A
12	X B	Y B
13	X C	Y C
14	X D	Y D
15	X E	Y E
16	X F	Y F
17	COM1	+
18	COM1	+
19	COM2	COM
20	COM2	COM

	NX70-X32D NX70-X32D1	NX70-Y32T NX70-Y32P
20	COM2	COM
19	COM2	COM
18	COM1	+
17	COM1	+
16	X1F	Y1F
15	X1E	Y1E
14	X1D	Y1D
13	X1C	Y1C
12	X1B	Y1B
11	X1A	Y1A
10	X19	Y19
9	X18	Y18
8	X17	Y17
7	X16	Y16
6	X15	Y15
5	X14	Y14
4	X13	Y13
3	X12	Y12
2	X11	Y11
1	X10	Y10

(I) (II)

4-6.

PLC

가

PLC

PLC

PLC

PLC

PLC

PLC

PLC

()

PLC

가

- PLC RUN

- PLC

- ON , 640ms

- 가 ALARM LED가 ON ,
ALARM OFF 가 가 .
(가)

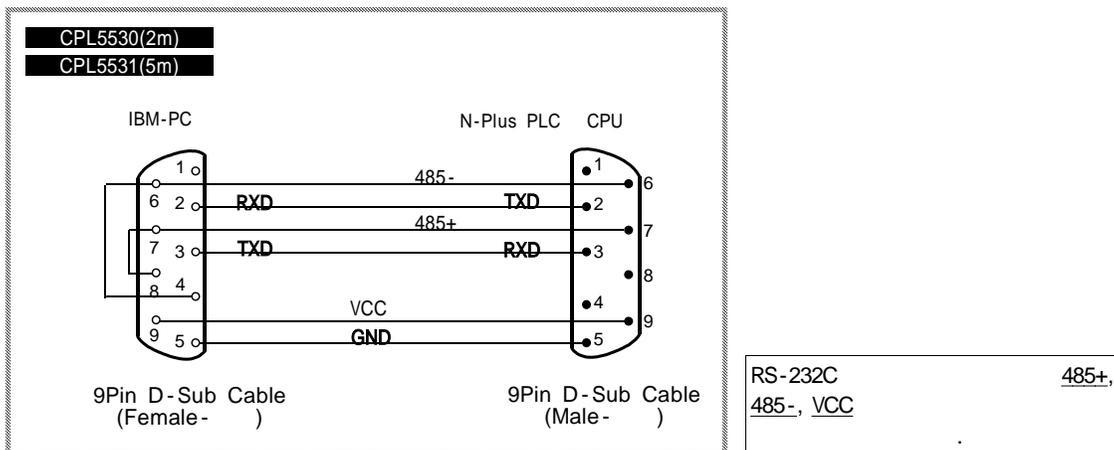
4-7. N-plus CPU

* PGM-500 RS232C, RS485

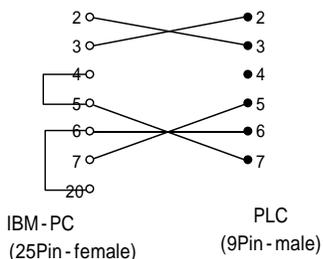
	RS485	RS232C	
(max)	1.2km	15m	
	38,400, 19,200, 9,600, 4,800 bps		Dip
	Half Duplex Asynchronous/ Polling		
	NO Parity		
Stop	1 Stop bit		
	Twisted Pair Cable		Shield Cable
	*PGM-500	IBM-PC (RS-232C) *PGM-500	

*1. N-plus CPU , SPC10, N70plus, N700plus, NX7, NX70(CPU70p1, CPU70p2), NX700(CPU700p) PLC . (WinGPC S/W)

N-plus CPU SPC Protocol
 RS232C/ RS485 : CPL5530(2m), CPL5531(5m)



(25Pin-9Pin)



4-8. EEPROM (NX70-CPU70p1, NX70-CPU70p2, NX-CPU700p, N70plus, N700plus CPU)

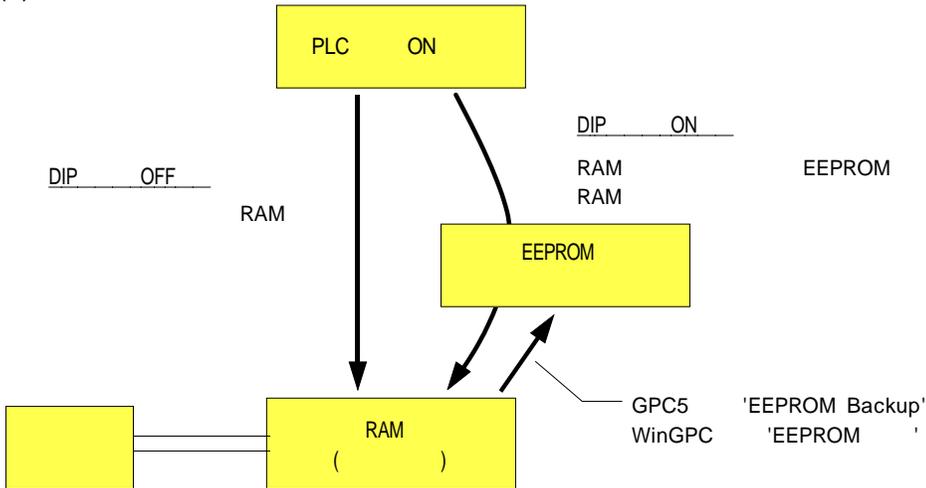
(1) EEPROM Backup ?

EEPROM(Electric Erase Programmable Read Only Memory) () 가 ,
 가 PLC ,
 가

(2)

EEPROM
 PLC NX70(NX70-CPU70p1 NX70-CPU70p2) PLC, NX700(NX-CPU700p) PLC N70plus,
 N700 plus CPU (Flash Memory)
 , NX700 (NX-CPU700p)
 , N700plus
 NX70 PLC (NX70-CPU70p2), N70plus(CPL9216)
 CPL7203
 EEPROM 29EE512 , (Write) 가 (3000)가 ,

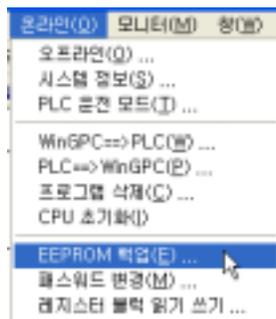
(3)



WinGPC, PGM-500

1) WinGPC 3.xx

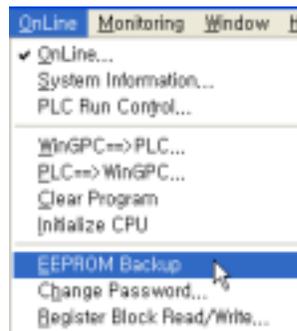
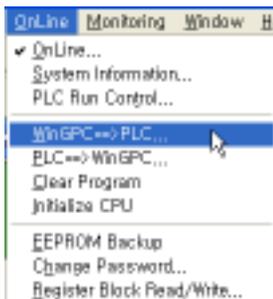
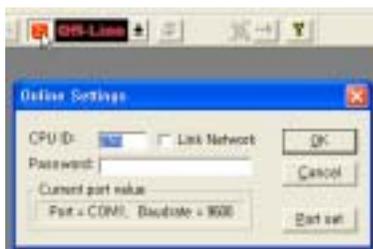
- PLC Online
- PLC (Download : WinGPC => PLC)
- 'EEPROM (E)'



2) WinGPC 4.xx

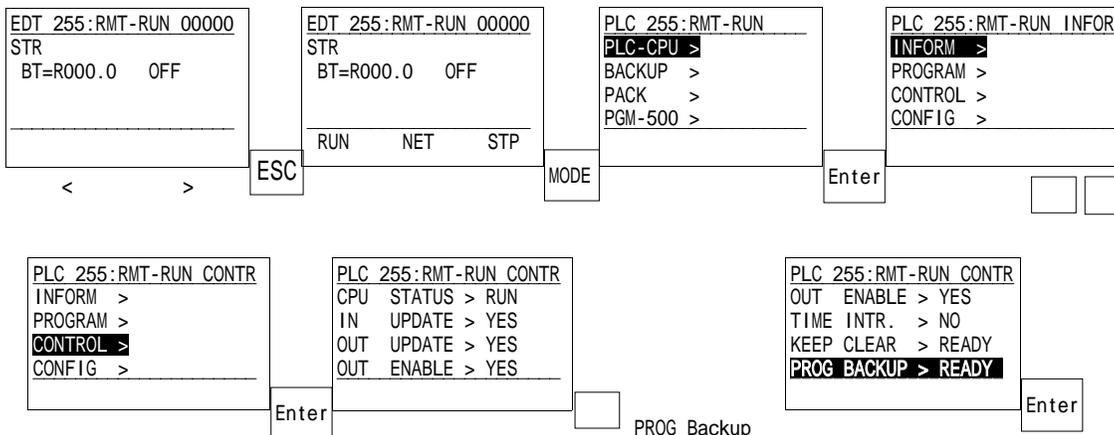
(4.xx WinGPC3 .)

- OnLine
- PLC (Download : WinGPC => PLC)
- 'EEPROM (E)'



3) PGM-500

- PLC , PROG Backup

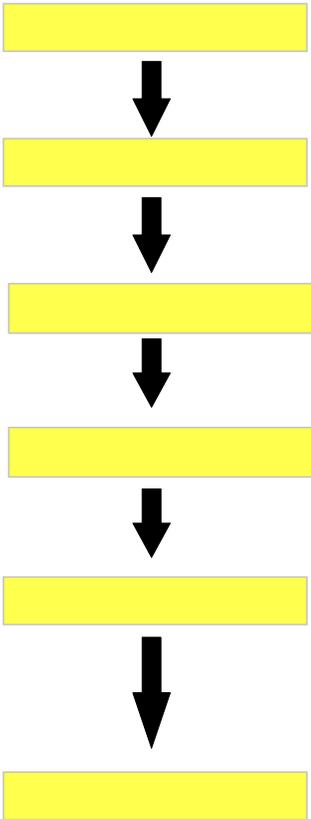


5

5-1.	80
5-2.	81
5-3.	82
5-4.	88
(1)	88
(2)	88
(3)	89
(4)	90

5-1.

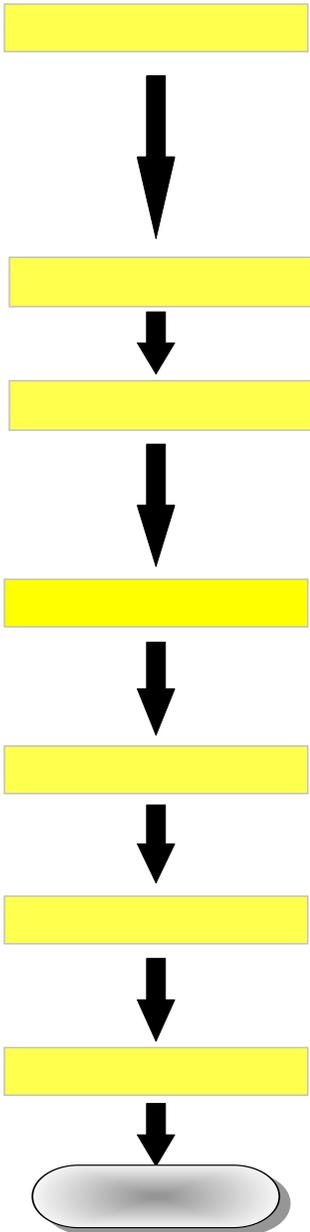
PLC



	<ol style="list-style-type: none"> 1. 가? 2. 가? 3. 가? 4. 가? 5. 가? 6. 가?
	1. (3) 가?
	<ol style="list-style-type: none"> 1. CPU 가? 2. 가 CPU 가?
	1. PLC 가 (PLC)
	<ol style="list-style-type: none"> 1. 가? AC110V (AC90~132V) AC220V (AC180~264V) 2. AC 가?

5-2.

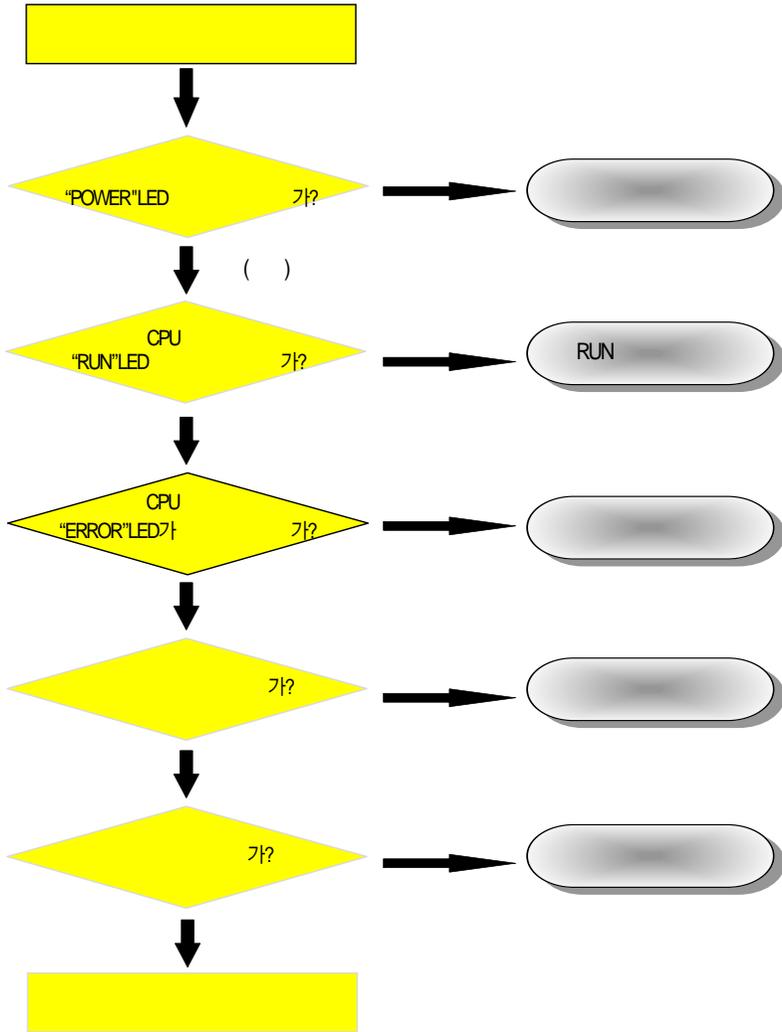
PLC



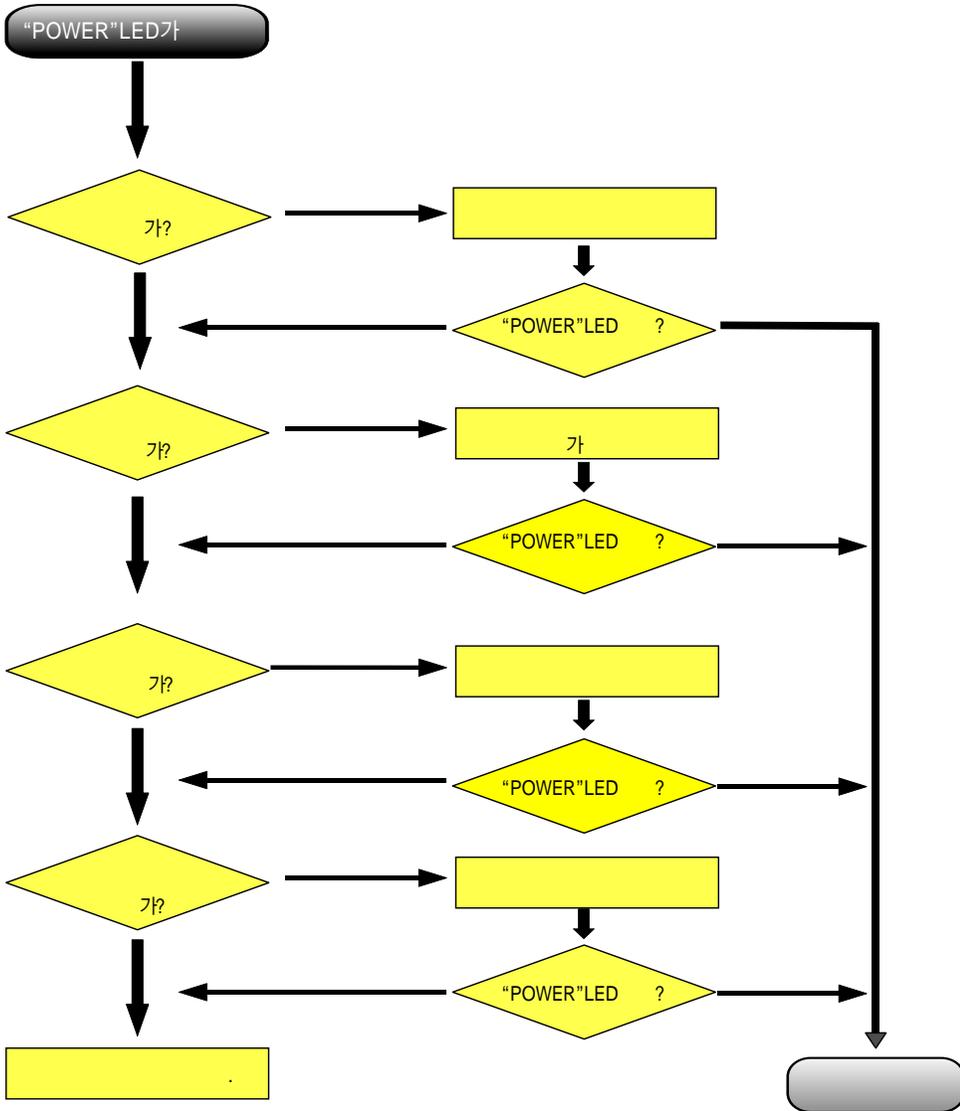
	<ol style="list-style-type: none"> 1. 2. 3. WinGPC (PGM-500) CPU 4. (CPU PROG) 5. LED
	<ol style="list-style-type: none"> 1. WinGPC PLC
	<ol style="list-style-type: none"> 1. LED WinGPC 2. WinGPC ON/OFF <p>가 (CPU RUN)</p>
	<ol style="list-style-type: none"> 1. WinGPC 2. WinGPC CPU
	<ol style="list-style-type: none"> 1. CPU RUN 2. RUN LED 3.
	<ol style="list-style-type: none"> 1. 가
	<ol style="list-style-type: none"> 1. HDD 2. (,)
)	PLC , , ,

5-3.

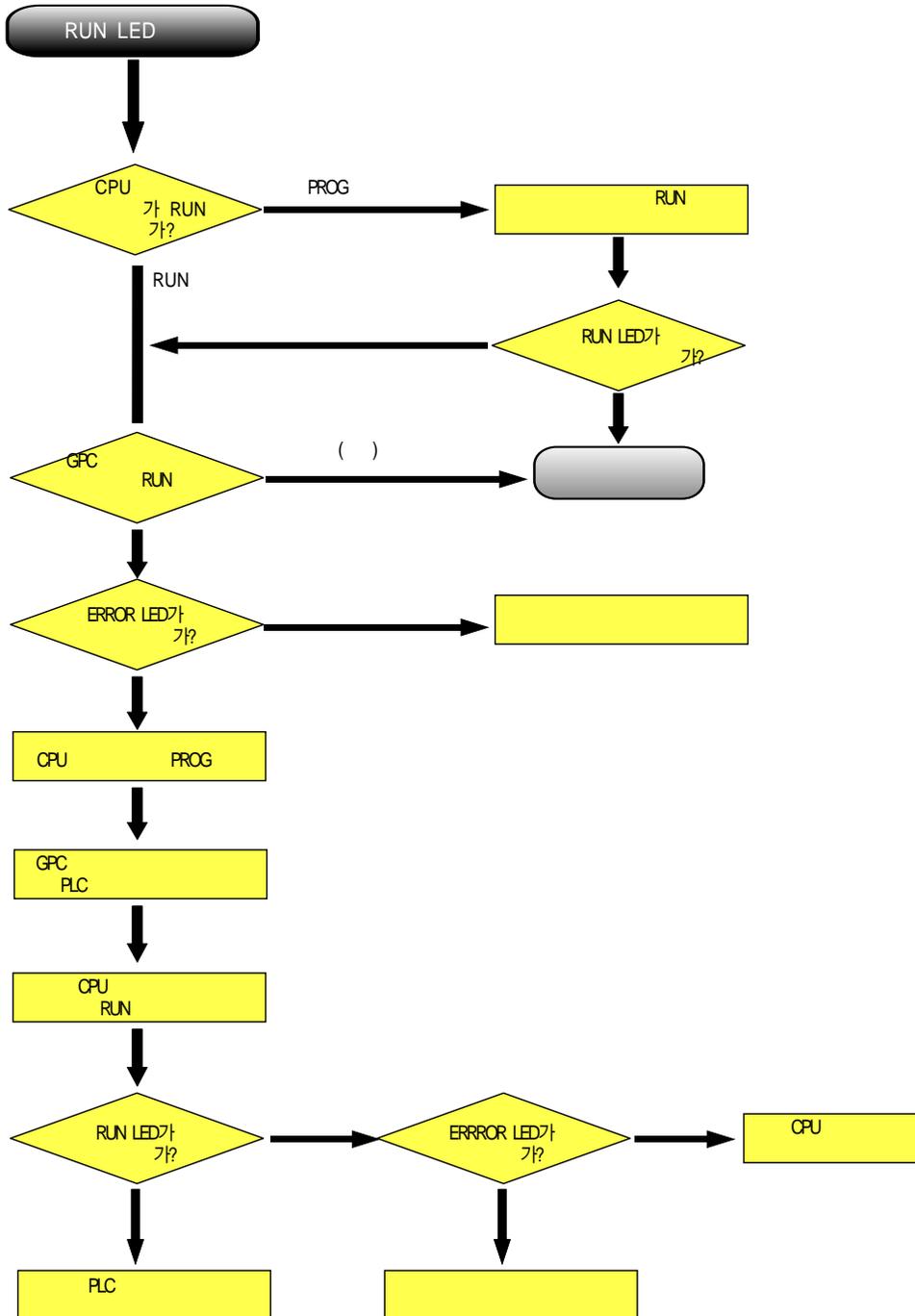
(1)



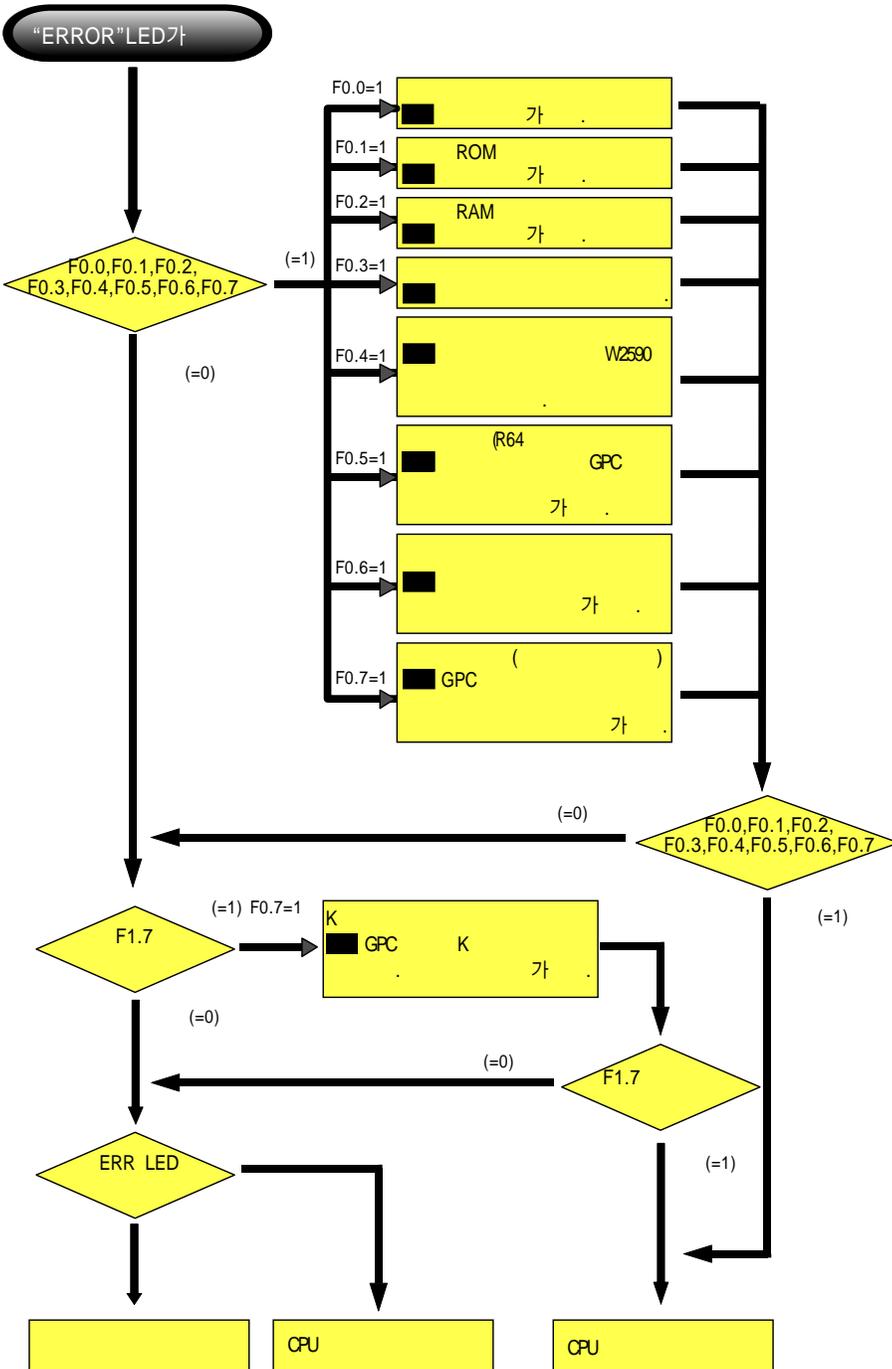
(2)



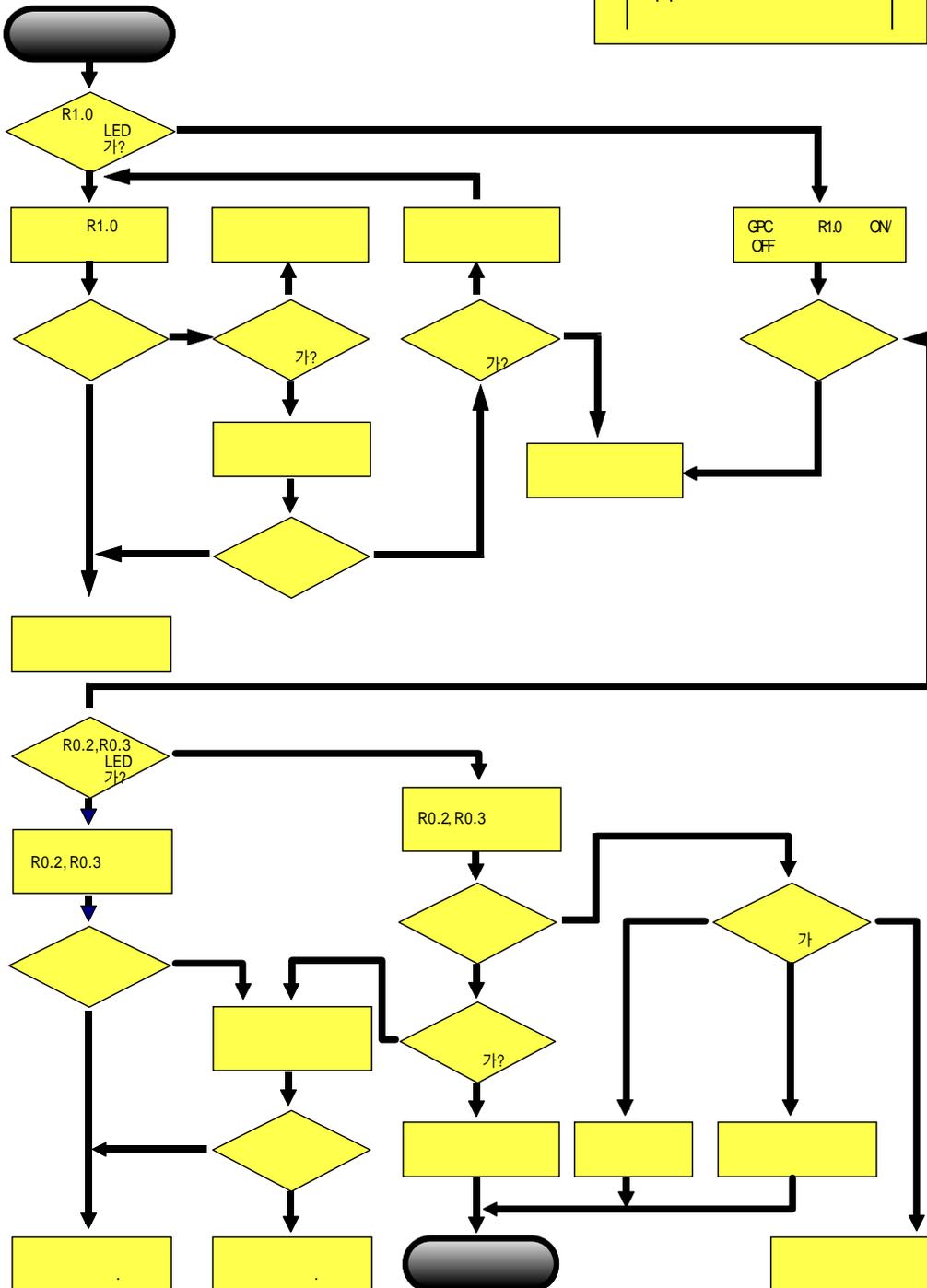
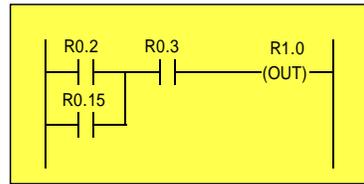
(3) RUN



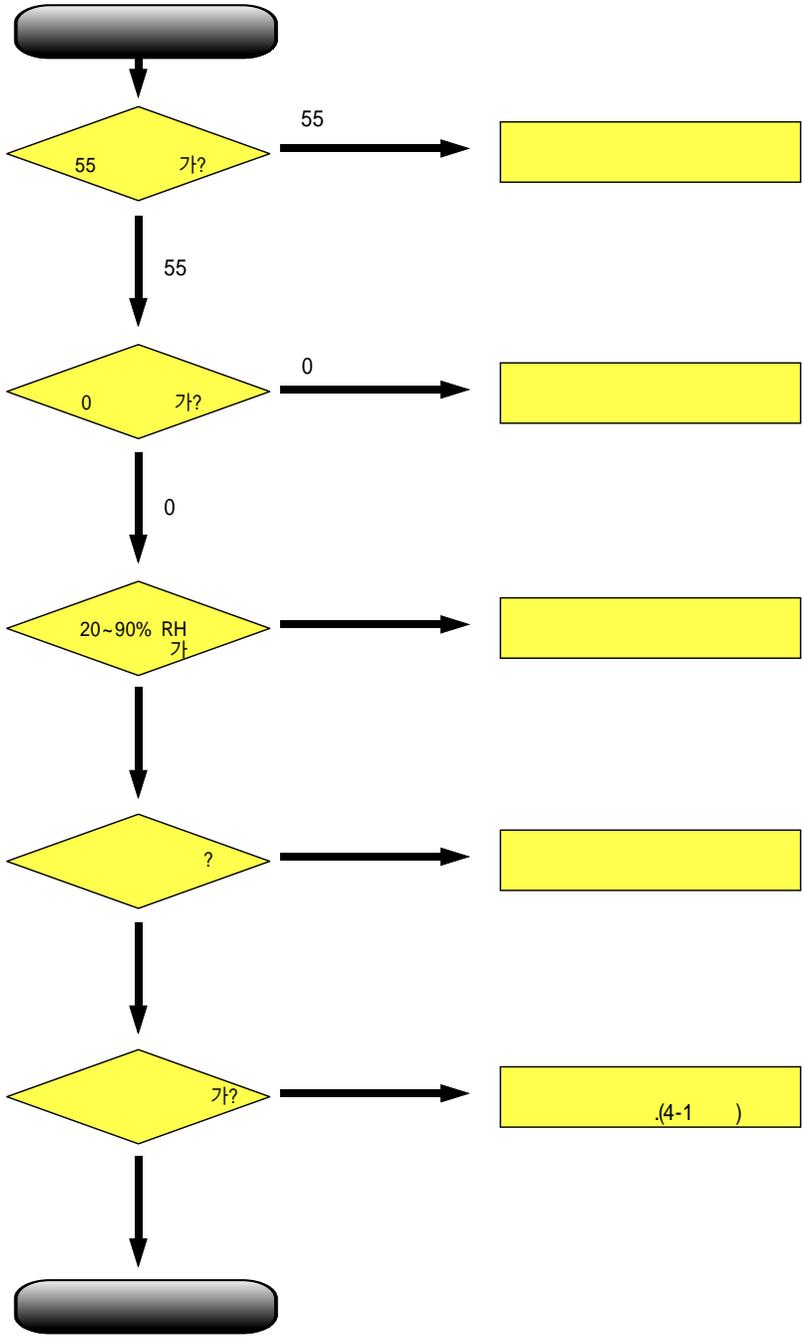
(4)



(5)



(6)



5-4.

(1)

POWER LED가	가	
가		CPU
RUN LED가		CPU
RUN ON		CPU
가	I/O	
ON	I/O	
	I/O	

(2)

ON (LED)	가 /	
ON (LED)		
OFF		
ON	ON 가 /	
OFF		
ON / OFF	가 /	
LED가 ()	LED	

(3)

ON		
	가 /	
	I/O	
OFF		
ON (LED)	ON	
ON (LED)		
	가 /	
OFF (LED)		
OFF (LED)		
ON / OFF		
	가 /	
가 8	가	
	CPU	CPU
LED가	LED	

(4)

PLC

6 1

	가?		
	() 가?	0~55	
	() 가?	35~85%RH	
	가?		
	가?		
	가?		
	가?		
	가?		
		10~30	
		3 (25)	

- | | |
|----|-----|
| 1. | OFF |
| 2. | |
| 3. | |
| 4. | |
| 5. | |

6

6-1.	92
6-2.	/ /SR	93
6-3.	94
6-4.	, 가/	94
6-5.	95
6-6.	96
6-7.	96
6-8.	97
6-9.	98
6-10.	99
6-11.	100
6-12.	100
6-13.	101
6-14.	102

6-1.

STR	Start		a
STN	Start Not		b
AND	And		a
ANN	And Not		b
OR	Or		a
ORN	Or Not		b
OUT	Out		
SET	Set		SET(ON)
RST	Reset		RESET(OFF)
NOT	Not		
STR DIF	Start Differential		()
STR DFN	Start Dif. Not		()
AND DIF	And Dif.		()
AND DFN	And Dif. Not		()
OR DIF	Or Dif		()
OR DFN	Or Dif. Not		()
ANB	And Block		
ORB	Or Block		
MS	Master block Set		(CPU ROM V2.0)
MR	Master block Reset		(CPU ROM V2.0)
MCS	MCS		
MCR	MCR		
-	(Extension)		(AND (WinGPC3, GPC5))

6-2. / /SR

TIM	On Delay Timer			Time Base: Ch 0~63= 0.01s Ch 64~255= 0.1s : SV = 0~65535 : TC +
TOF	Off Delay Timer			Time Base: Ch 0~63= 0.01s Ch 64~255= 0.1s : SV = 0~65535 : TC +
SST	Single Shot Timer			Time Base: Ch 0~63= 0.01s Ch 64~255= 0.1s : SV = 0~65535 : TC +
UC	Up Counter			: Ch 0~255 () : SV = 0~65535 : TC +
DC	Down Counter			: Ch 0~255 () : SV = 0~65535 : TC +
RCT	Ring Counter			: Ch 0~255 () : SV = 0~65535 : TC +
UDC	Up-Down Counter			: Ch 0~255 () : SV = 0~65535 : TC +
SR	Shift Register			(Sb, Eb): M, K (M, K) 1Bit I Sb : 256

6-3.

STR == AND == OR ==	START == AND == OR ==			A B / ON. A B / Data
STR <> AND <> OR <>	START <> AND <> OR <>			A B / ON. <> ≠ , A B / Data
STR > AND > OR >	START > AND > OR >			A B / ON.
STR >= AND >= OR >=	START >= AND >= OR >=			A B / ON.
STR <= AND <= OR <=	START <= AND <= OR <=			A B / ON.
STR < AND < OR <	START < AND < OR <			A B / ON.

)

'D'

6-4. 가/

LET (DLET)	Let ()			S D ()
INC (DINC)	Increment (Binary 가)			ON D 1 가
INCB (DINCB)	BCD increment (BCD 가)			ON 가 BCD D 1
DEC (DDEC)	Decrement (Binary)			ON D 1
DECB (DDECB)	BCD decrement (BCD)			ON BCD D 1

6-5.

ADD (DADD)	Decimal addition (10)	ADD D = S1= S2=	DADD D = S1= S2=	$D = S1 + S2$ (10)
ADDB (DADDB)	BCD addition (BCD)	ADDB D = S1= S2=	DADDB D = S1= S2=	$D = S1 + S2$ (BCD)
SUB (DSUB)	Decimal subtraction (10)	SUB D = S1= S2=	DSUB D = S1= S2=	$D = S1 - S2$ (10)
SUBB (DSUBB)	BCD subtraction (BCD)	SUBB D = S1= S2=	DSUBB D = S1= S2=	$D = S1 - S2$ (BCD)
MUL (DMUL)	Decimal multiplication (10)	MUL D = S1= S2=	DMUL D = S1= S2=	$D = S1 \times S2$ (10)
MULB (DMULB)	BCD multiplication (BCD)	MULB D = S1= S2=	DMULB D = S1= S2=	$D = S1 \times S2$ (BCD)
DIV (DDIV)	Decimal division (10)	DIV D = S1= S2=	DDIV D = S1= S2=	$D = S1 \div S2$ (10), S2 0
DIVB (DDIVB)	BCD division (BCD)	DIVB D = S1= S2=	DDIVB D = S1= S2=	$D = S1 \div S2$ (BCD) S2 0
ADC (DADC)	Decimal addition w/carry (10)	ADC D = S1= S2=	DADC D = S1= S2=	$D = S1 + S2 + CY$ (10 ,)
ADCB (DADCB)	BCD addition w/carry (BCD)	ADCB D = S1= S2=	DADCB D = S1= S2=	$D = S1 + S2 + CY$ (BCD ,)
SBC (DSBC)	Decimal subtraction w/carry (10)	SBC D = S1= S2=	DSBC D = S1= S2=	$D = S1 - S2 - CY$ (10 ,)
SBCB (DSBCB)	BCD subtraction w/carry (BCD)	SBCB D = S1= S2=	DSBCB D = S1= S2=	$D = S1 - S2 - CY$ (BCD ,)
ABS (DABS)	Absolute value ()	ABS D =	DABS D =	$D = D $ ()
WNOT (DNOT)	NOT (, 1)	WNOT D =	DNOT D =	$D = 1 - D$
NEG (DNEG)	Negative (2)	NEG D =	DNEG D =	$D = 2 - D$ (1 +1)(-)

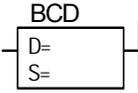
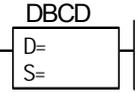
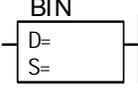
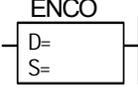
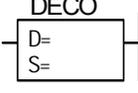
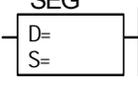
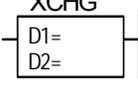
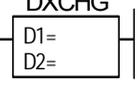
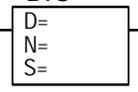
6-6.

WAND (DAND)	AND ()			<table border="1"> <tr> <td>S1</td> <td>S2</td> <td>D</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> </tr> </table>	S1	S2	D	0	0	1	0	1	0	1	0	0	1	1	1
S1	S2	D																	
0	0	1																	
0	1	0																	
1	0	0																	
1	1	1																	
WOR (DOR)	OR ()			<table border="1"> <tr> <td>S1</td> <td>S2</td> <td>D</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> </tr> </table>	S1	S2	D	0	0	1	0	1	0	1	0	1	1	1	1
S1	S2	D																	
0	0	1																	
0	1	0																	
1	0	1																	
1	1	1																	
WXOR (DXOR)	Exclusive OR ()			<table border="1"> <tr> <td>S1</td> <td>S2</td> <td>D</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> </tr> </table>	S1	S2	D	0	0	1	0	1	0	1	0	1	1	1	0
S1	S2	D																	
0	0	1																	
0	1	0																	
1	0	1																	
1	1	0																	
WXNR (DXNR)	Exclusive OR NOT ()			<table border="1"> <tr> <td>S1</td> <td>S2</td> <td>D</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> </tr> </table>	S1	S2	D	0	0	1	0	1	0	1	0	0	1	1	1
S1	S2	D																	
0	0	1																	
0	1	0																	
1	0	0																	
1	1	1																	

6-7.

RLC (DRLC)	Rotate left (,)			<p>N (-)</p>
RRC (DRRC)	Rotate right (,)			<p>N (-)</p>
ROL (DROL)	Rotate left (,)			<p>N (->) ()</p> <p>(F1.8)</p>
ROR (DROR)	Rotate right (,)			<p>N (-) ()</p> <p>(F1.8)</p>
SHL (DSHL)	Shift left ()			<p>N (0)</p>
SHR (DSHR)	Shift right ()			<p>N (0)</p>

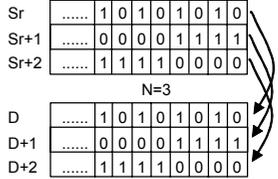
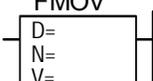
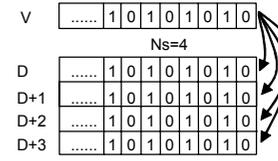
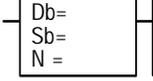
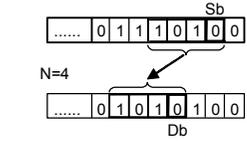
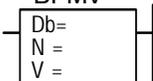
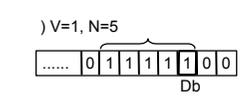
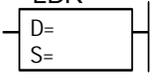
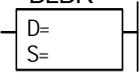
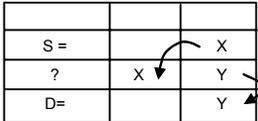
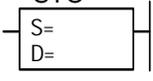
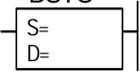
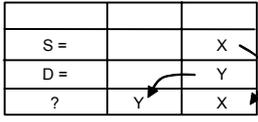
6-8.

BCD (DBCD)	BCD			<p>S 2 BCD D</p> <p>S $\dots 00111111 = 63(10)$</p> <p>D $\dots 01110001 = \\$63$ (BCD)</p>
BIN (DBIN)	Binary			<p>S BCD 2 D</p> <p>S $\dots 011011001 = \\$39$ (BCD)</p> <p>D $\dots 001100111 = 39(10)$</p>
ENCO	Encode			<p>1</p> <p>$(2^n - n) D$ 8bit</p> <p>S $\overset{15.8}{0} \overset{7}{0} \overset{6}{0} \overset{5}{1} \overset{4}{1} \overset{3}{1} \overset{2}{1} \overset{1}{0} \overset{0}{0} = 2^6$</p> <p>D $\dots 00000110 = 6$</p> <p>) SPC $(2^n + 1)$</p>
DECO	Decode			<p>S 4 2^n</p> <p>D</p> <p>S $\dots x x x x 0 1 0 1 = 5$</p> <p>D $\overset{15.8}{0} \overset{7}{0} \overset{6}{0} \overset{5}{0} \overset{4}{1} \overset{3}{0} \overset{2}{0} \overset{1}{0} \overset{0}{0}$</p>
SEG	7- 7-Segment			<p>S 4 7-Segment</p> <p>D</p> <p>S $\dots 00000101 = 5$</p> <p>D $\dots 01101101$</p> <p>f a b e d c g</p>
XCHG (DXCHG)	(Exchange)			<p>D1 D2</p> <p>D1 $\dots 0101$ D1 $\dots 0011$</p> <p>D2 $\dots 0011$ D2 $\dots 0101$</p>
DIS	Dissemble			<p>S 4 N+1</p> <p>D D+N 4</p> <p>S=\$7325 011110011001001011</p> <p>N=3</p> <p>D $0 \dots 0011011 = 5$</p> <p>D+1 $0 \dots 000110 = 2$</p> <p>D+2 $0 \dots 000011 = 3$</p> <p>D+3 $0 \dots 001111 = 7$</p>
UNI	Unify			<p>S S+N 4 D</p> <p>(N= 0~3)</p> <p>N=3</p> <p>S $0 \dots 0011011 = 5$</p> <p>S+1 $0 \dots 000110 = 2$</p> <p>S+2 $0 \dots 000011 = 3$</p> <p>S+3 $0 \dots 001111 = 7$</p> <p>D=\$7325 011110011001001011</p>

6-9.

BSET	(SET) Bit Set			D N 1 SET D 0 0 1 1 0 0 1 0 0 N=5 ↑ 1 (N=0~15)
BRST	Bit Reset			D N 0 D 0 1 0 1 1 0 1 0 0 N=3 ↑ 0
BNOT	Bit Not			D N D 0 1 1 1 1 0 1 0 0 N=4 ↓ D 0 1 1 1 0 0 1 0 0
BTST	Bit Test			D N F1.8 D 0 1 1 1 1 0 1 0 0 N=6 → F1.8
SUM	1 Sum			S 1 D S 0 0 0 1 1 0 1 0 0 1 1 0 1 0 0 1 1 1 =7 D 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 D=7
SC	(SET) Set Carry			(F1.8) 1 SET 1 → F1.8
RC	Reset Carry			(F1.8) 0 RESET 0 → F1.8
CC	Complement Carry			(F1.8) F1.8 F1.8 1 → 0 0 → 1

6-10.

<p>MOV</p>	<p>Move</p>	<p>MOV</p> 		<p>S N (S)</p> <p>D N</p> <p>Sr 1 0 1 0 1 0 1 0</p> <p>Sr+1 0 0 0 0 1 1 1 1</p> <p>Sr+2 1 1 1 1 0 0 0 0</p> <p>N=3</p> <p>D 1 0 1 0 1 0 1 0</p> <p>D+1 0 0 0 0 1 1 1 1</p> <p>D+2 1 1 1 1 0 0 0 0</p> 									
<p>FMOV</p>	<p>Fill Move</p>	<p>FMOV</p> 		<p>V D N</p> <p>v 1 0 1 0 1 0 1 0</p> <p>Ns=4</p> <p>D 1 0 1 0 1 0 1 0</p> <p>D+1 1 0 1 0 1 0 1 0</p> <p>D+2 1 0 1 0 1 0 1 0</p> <p>D+3 1 0 1 0 1 0 1 0</p> 									
<p>BMOV</p>	<p>Bit Move</p>	<p>BMOV</p> 		<p>Sb N</p> <p>Db N</p> <p>(Sb, Db 가)</p> <p>..... 0 1 1 1 1 0 1 1 0 0</p> <p>N=4</p> <p>..... 0 1 1 0 1 0 1 1 0 0</p> <p>Db</p> 									
<p>BFMV</p>	<p>Bit Fill Move</p>	<p>BFMV</p> 		<p>V Db N</p> <p>(V=0 1)(N=1...256,)</p> <p>(Db)</p> <p>) V=1, N=5</p> <p>..... 0 1 1 1 1 1 1 0 0</p> <p>Db</p> 									
<p>LDR (DLDR)</p>	<p>Load D←(S)</p>	<p>LDR</p> 	<p>DLDR</p> 	<p>S</p> <p>D</p> <p>()</p> <table border="1" data-bbox="854 1329 1112 1450"> <tr> <td>S =</td> <td></td> <td>X</td> </tr> <tr> <td>?</td> <td>X</td> <td>Y</td> </tr> <tr> <td>D =</td> <td></td> <td>Y</td> </tr> </table> 	S =		X	?	X	Y	D =		Y
S =		X											
?	X	Y											
D =		Y											
<p>STO (DSTO)</p>	<p>S Store (D)←S</p>	<p>STO</p> 	<p>DSTO</p> 	<p>S</p> <p>D</p> <p>()</p> <table border="1" data-bbox="854 1580 1112 1702"> <tr> <td>S =</td> <td></td> <td>X</td> </tr> <tr> <td>D =</td> <td></td> <td>Y</td> </tr> <tr> <td>?</td> <td>Y</td> <td>X</td> </tr> </table> 	S =		X	D =		Y	?	Y	X
S =		X											
D =		Y											
?	Y	X											

6-11.

FOR (DFOR)	FOR For Loop	FOR D=	DFOR D=	D 1 NEXT D (D가 0)
NEXT	FOR Next	NEXT		FOR
JMP	LBL Lb	JMP Lb=		LBL L L=0~63(가)
LBL	JMP	LBL Lb=		JMP L=0~63(가)
JMPS	JMPE Jump Start	JMPS		JMPE
JMPE	JMPS Jump End	JMPE		(JMPS) (JMPS)
CALL	Call Subroutine	CALL Sb=		
SBR	Subroutine Start	SBR Sb=		Sb=0~63(64 , 가)
RET	Subroutine Return	SBR		

6-12.

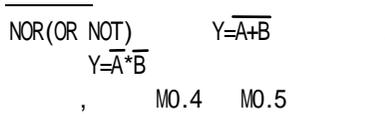
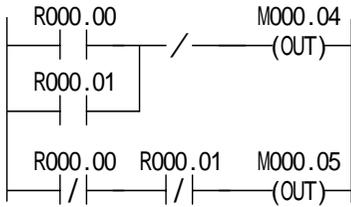
INT	Interrupt	INT V=		(1 가) N:=1~999(20msec 10sec) =(Ni+1)×0.01
RETI	Return Interrupt	RETI		
INPR	Input Refresh	INPR Ch=		() CH
OUTR	Output Refresh	OUTR Ch=		() CH
WAT	Watchdog Timer	WAT		
END	END	END		(CPU)

6-13.

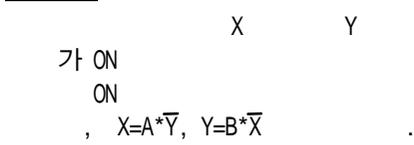
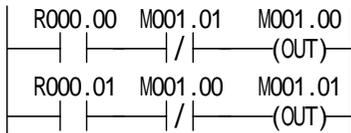
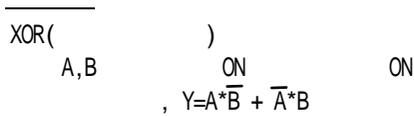
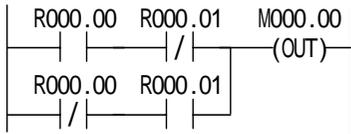
READ	(UNIT)	READ TO=RR1 SZ=NR3 FR=NN5:NR6	Slot(NN5) (NR3) (NN6) (RR1)
WRITE	(UNIT)	WRITE TO=NN1:NR2 SZ=NR3 FR=NN5	/ (NR5) (NR3) Slot(NN1) (NR2)
RMRD	(UNIT)	RMRD TO=NR1:RR2 NT=NN3:NN4 FR=NN5:NR6	Remote Network Loop(NN3) Station(NN4) Slot(NN5) (NR6) (NR1) (RR2)
RMWR	(UNIT)	RMWR NT=NN1:NN2 TO=NN3:NR4 FR=NR5:NR6	/ (NR6) (NR5) Remote Network Loop(NN1) Station(NN2) Slot(NN3) (NR4)
RECV		RECV TO=NR1:RR2 NT=NN3:NN4 FR=NN5:NR6	Link Network Loop(NN3) Station(NN4) (NN5) (NR6) (NR1) (RR2)
SEND		SEND NT=NN1:NN2 TO=NN3:NR4 FR=NN5:NR6	/ (NR6) (NR5) Link Network Loop(NN1) Station(NN2) (NN3) (NR4)
RECVB		RECVB TO=BR1 NT=NN3:NN4 FR=NN5:NR6	Link Network Loop(NN3) Station(NN4) (NN5) Bit (NR6) Bit (BR1)
SENDB		SENDB NT=NN1:NN2 TO=NN3:NR4 FR=NB5	Bit (NB5) Link Network Loop(NN1) Station(NN2) (NN3) Bit (NR4)

1

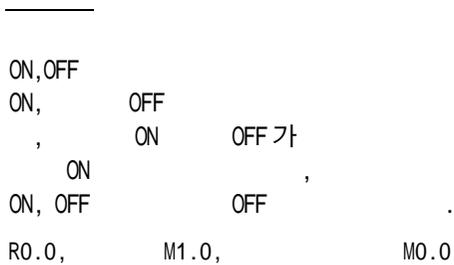
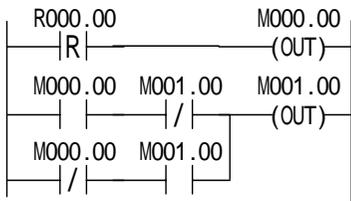
NOR(OR NOT)



XOR(Exclusive OR)



2



1)

2)

OFF ON
DIF



1Scan

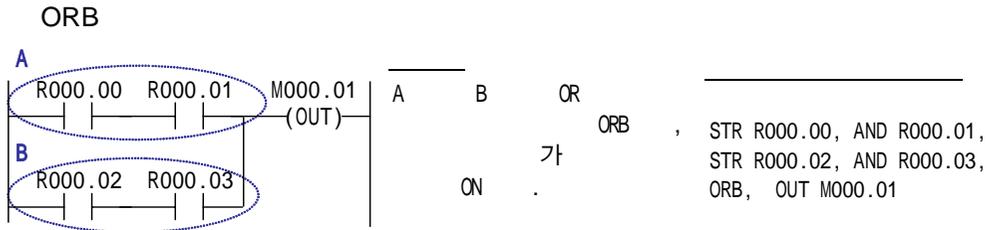
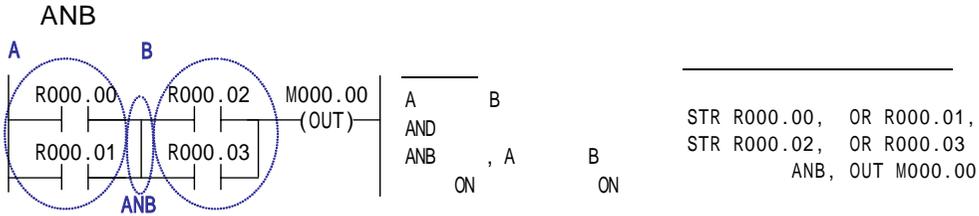
ANB			1	
ORB			1	
NOT		()	1	

1. ANB(AND Block)
ORB(OR Block)

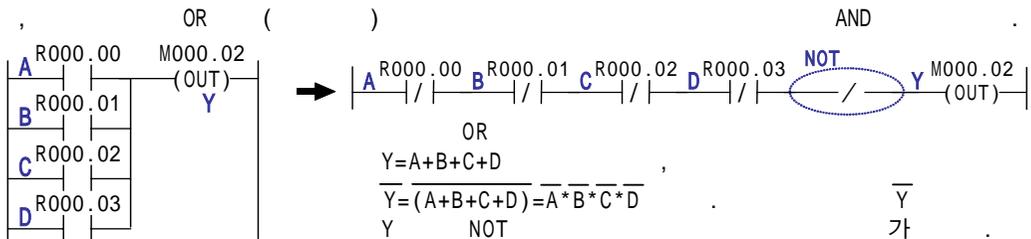
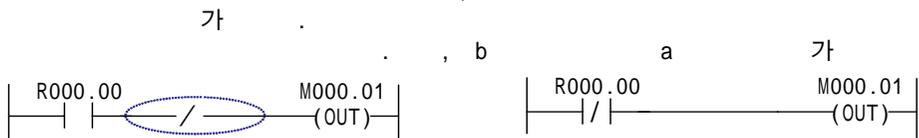
2. NOT NOT

3. 3

4. (Stack) 16 가 , CPU



NOT
NOT

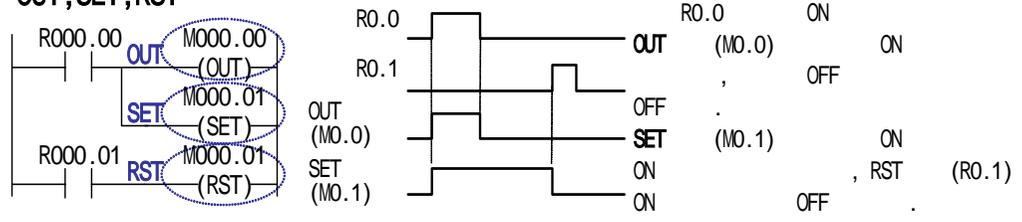


AND OR

OUT			1	
SET		ON SET	2	
RST		OFF RESET	2	

1. OUT
2. OUT, SET, RST R, L, M, K 가 , F 가
3. R
4. OUT R 가 , OUT L, M, K, F
5. SET RST , 가 , SET RST RESET 가
6. K SET RST OFF
7. OUT, SET, RST ROOT ON F0.15 a

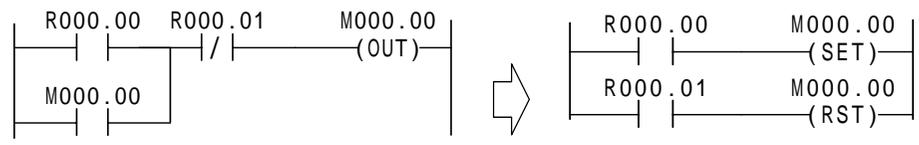
OUT, SET, RST



```
STR R000.00, OUT M000.00, SET M000.01, STR R000.01, RST M000.01
```

1

SET, RST



STR DIF			1	
AND DIF			1	
OR DIF			1	
STR DFN			1	
AND DFN			1	
OR DFN			1	

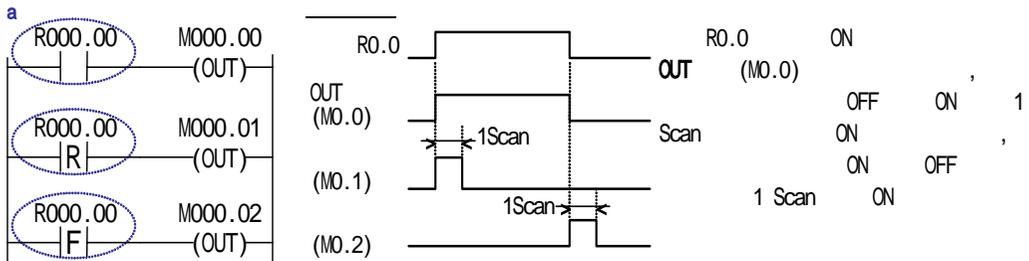
1. () 1SCAN ON
2. (DIF) OFF ON 1Scan ON
(DFN) ON OFF 1Scan ON

3.
 - NX-CPU700P, NX70-CPU70p2, NX70-CPU70p1(Ver2.0), CPL9216A, CPL7215A = => R, L, M, K, F, TC 가
 - NX70-CPU70p1 (V1.x), CPL9215A = R , M0.0 M63.15, F, TC 가

주의 : CPU70p1, 9215A M64.0 M127.15 , K
S/W CPU Download

(RUN)
주의 : SPC (SPC-10, SPC-100/24S/120S/300) 1 1

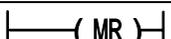
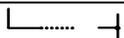
- 4.
- 5.



a b

가

STR R00.00, OUT M00.00, STR DIF R00.00, OUT M00.01, STR DFN R00.00, OUT M00.02

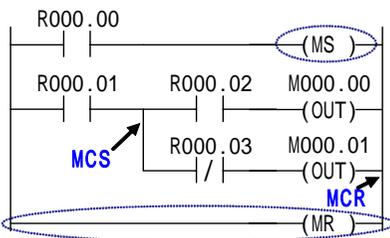
MS		()	1	1)
MR		()	1	1)
MCS			1	, 2)
MCR		()	1	, 2)

1) - MS, MR CPU F/W 2.0 WinGPC 3.70
 - WinGPC V3.70 , PLC V2.0 MCS, MCR (Upgrade)

2) - WinGPC
 - WinGPC 3.70 MS, MR , WinGPC 3.6
 , 2.xx

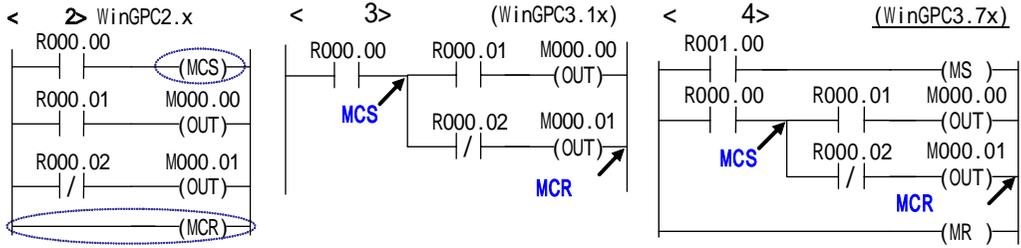
1. MS MR , ,
2. MS, MR (MS OverFlow)
 16 , CPU 가 (SPC 8).
3. CPU MCS, MCR WinGPC3.0 , WinGPC V2.xx MCS, MCR
4. MS 가 , ROOT , MR
5. MCS, MCR WinGPC3.70 가 ,

1
 < 1>(CPU V1.3 , WinGPC 3.5)



MS R0.0 ON MS/MR
 ON ON
 , R0.0, R0.1, R0.2 가 ON MO.0 ON
 R0.0= ON, R0.1= ON, R0.3= OFF MO.1 ON,
 R0.0 OFF OFF

2 : MS/MR, MCS/MCR (WinGPC3.x)

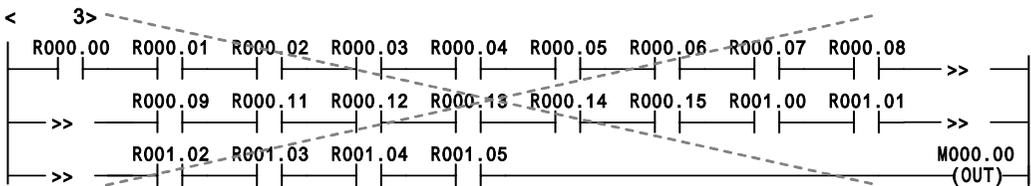
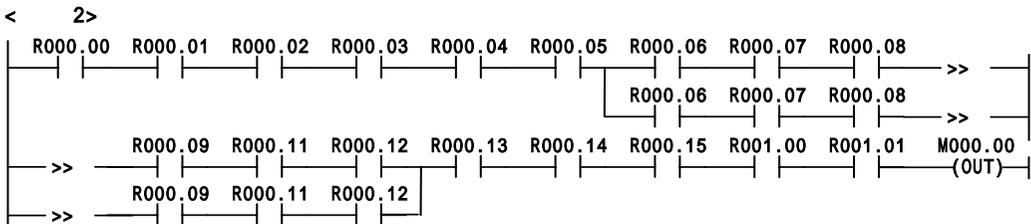
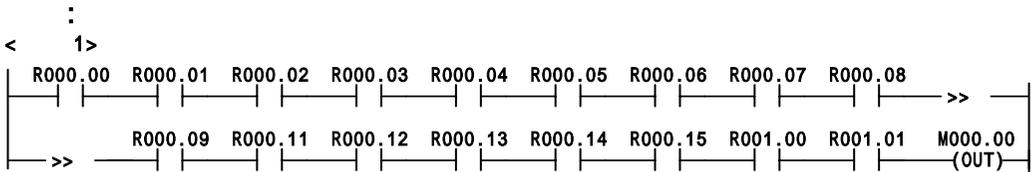


1. WinGPC 2.x MCS, MCR < 1, 2> ,
 < 3> WinGPC3.0, 3.1 , < 4> WinGPC3.7x
 가 , MS, MR 3.7 .
2. MCS/MCR ,
 CPU MCS, MCR ,
 CPU Upload .
3. PC (Compile) PLC
 , PLC Upload (Decompile) WinGPC
 2,3,4 .
 , WinGPC V3.1x < 2> PLC , WinGPC
 V3.x Upload < 3> , WinGPC2.x Upload
 < 2> .
4. WinGPC V3.7x < 1> , CPU V1.2x
 , PLC V2.0 . (PLC
 V1.2x) 3 .
5. WinGPC 3.7 CPU ROM MCS/MCR, MS/MR .

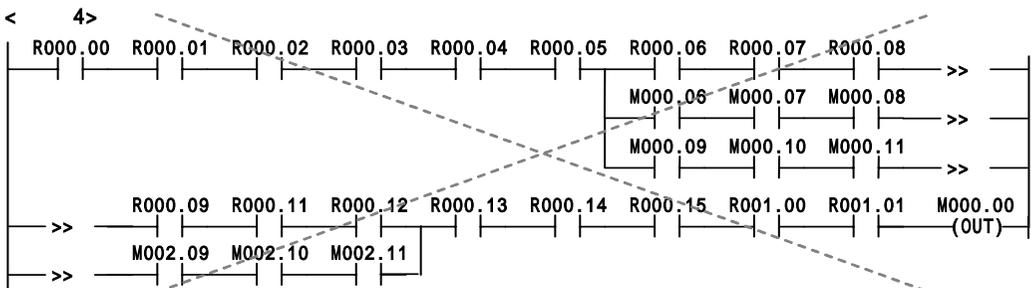
1. , < 2, 3 >
 WinGPC STR R0.0, MCS, STR R0.1, OUT M0.0, STN R0.2, OUT M0.1, MCR
 , WINGPC V3.5x CPU 2.0x MS, MR 가
 , .

-		(Extension) (AND (WinGPC3, GPC5))	-	
---	--	-------------------------------------	---	--

1. 가 ,
2. (RUNG) RUNG , RUNG
3. 가 , CPU WinGPC



→ , R001.01



→

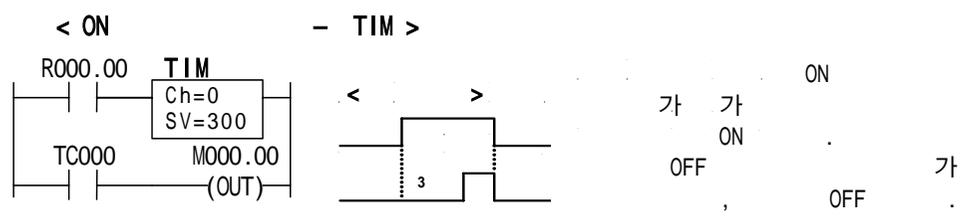
- / / SR

TIM		ON ()	3	
TOF		OFF ()	3	1)
SST		(/)	3	

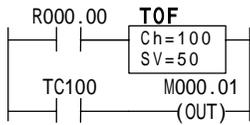
1) (TOF)

	SPC-10	SPC100 24S/120S	SPC300	A200	N70 plus 9215A, 9216A	NX70 plus CPU70p1/V2, CPU70p2/V2	N/NX700plus 7215A, CPU700p	NX700plus CPU700p/V2
	X	X	X					

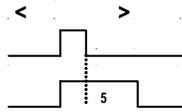
1. 가 , 256
2. 0 255
3. 0 63 , Time Base 가 10mSec
(0.01) , 64 255 Time Base 가
100mSec(0.1)
4. (SV) 16 0 65,535
5. " TC + "
6. 가 ,
7. 가 가 (TIM, SST) ON
가 (65535) , OFF 가
8. 가 (TOF) 가 가 , 가
9. ' 0 ' ON 가 ON
10. TIM ON 가 ON
TOF OFF 가 OFF
11. SST ON 가 ,
OFF



< OFF

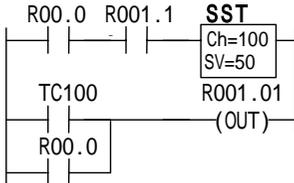


- TOF >

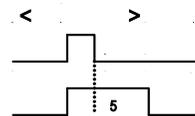


ON 가 OFF 가 '0' 가 OFF

< : SST

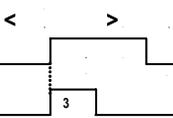
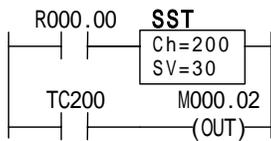


OFF



ON 가 OFF 가 SST 가 OFF 가

< - SST >

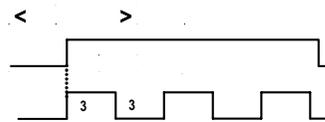
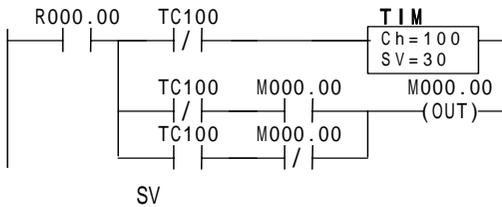


ON 가 OFF 가 ON 가 OFF 가

1

1

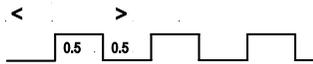
→ ON 3 ON, 3 OFF 가 ()



SV

1

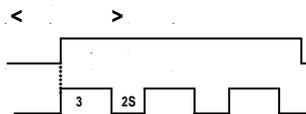
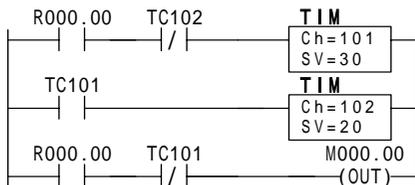
→ PLC (F) 1

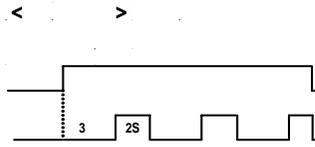
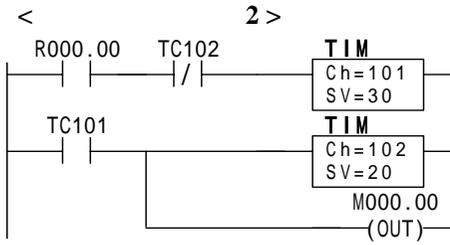


2

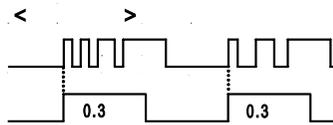
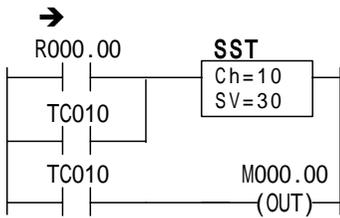
2

→ ON 3 ON, 2 OFF 가

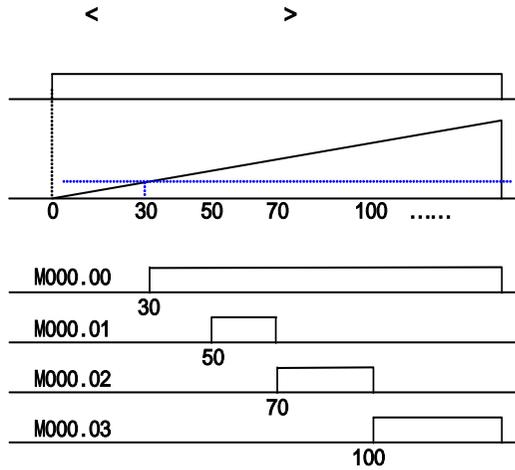
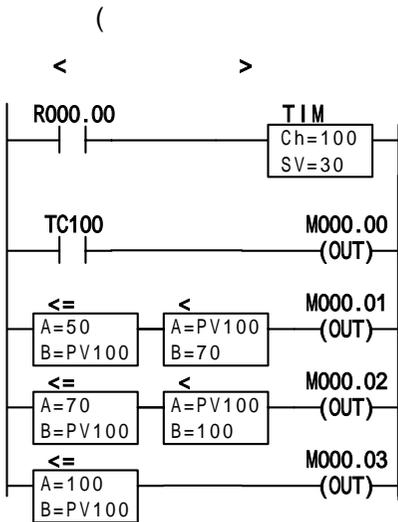




2



→ (PV)



1. (PV) 가 가

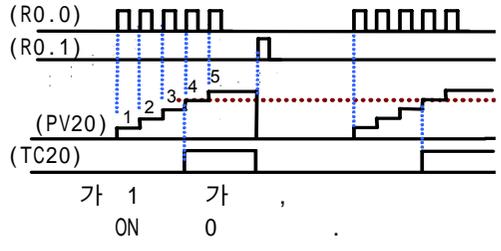
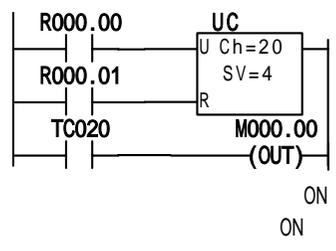
2.

- / / SR

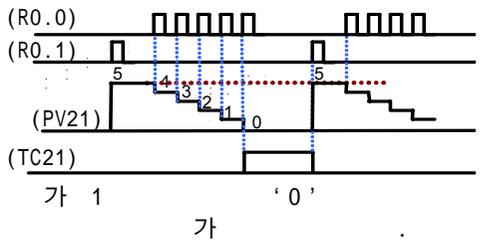
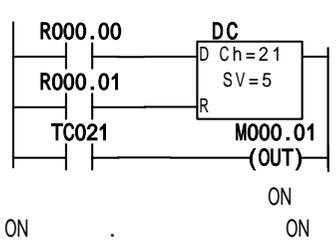
UC			3
DC			3

1. 4 (UC, DC, RCT, UDC)가 , 256
2. , 0 255
3. (SV) 16 (0 65,535)
4. " TC + "
5. 가
6. UC() OFF ON 가 1 ,
0 (65,535) 가 ,
7. DC() ON 가 , OFF
ON 가 1 '0' ON ,
가 Reset ON , OFF
OFF
8. ON

< UP Counter >



< Down Counter >



- / / SR

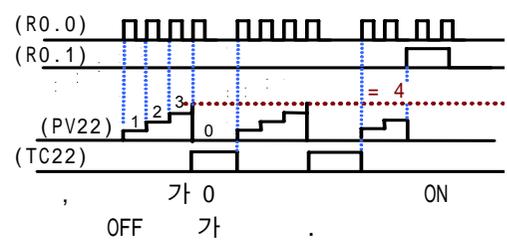
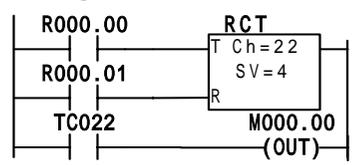
RCT			3	1)
UDC			3	

1)

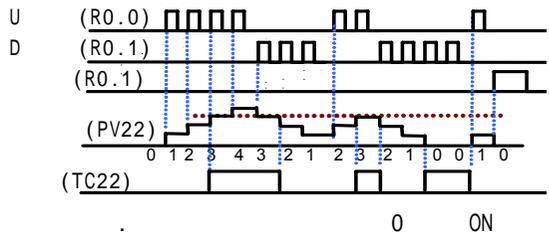
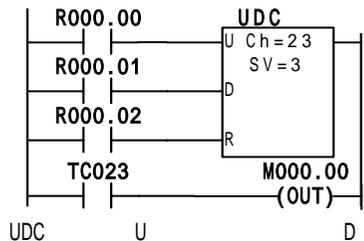
SPC-10	SPC100 24S/120S	SPC300	A200	N70 plus 9215A, 9216A	NX70 plus CPU70p1/V2, CPU70p2/V2	N/NX700plus 7215A, CPU700p	NX700plus CPU700p/V2
×	×	×					

1. 가 , 256
2. , 0 255
3. (SV) 16 (0 65,535) "TC + "
4. 가
5. RCT() OFF ON '0' 1
가 가 0 ON
6. UDC(/) (U) OFF ON 가 1 가 1
가 , (D) OFF ON 가 '0'
0 ON , ON OFF , '0'
(, SPC 가 0 (-)
7. ON

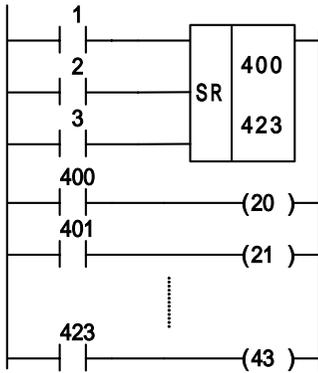
< Ring Counter >



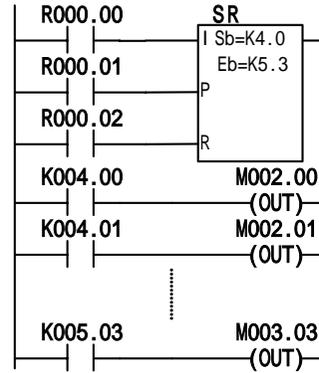
< UP-Down Counter >



: SPC-120, SPC24 SR



<SPC120/24 >



<NX-p, Nplus >

1) SPC-120/24 8 , NX plus 16

2) ,

SPC-120/24	NX-p,Nplus
400	K4.00
401	K4.01
402	K4.02
403	K4.03
404	K4.04
405	K4.05
406	K4.06
407	K4.07
410	K4.08
411	K4.09

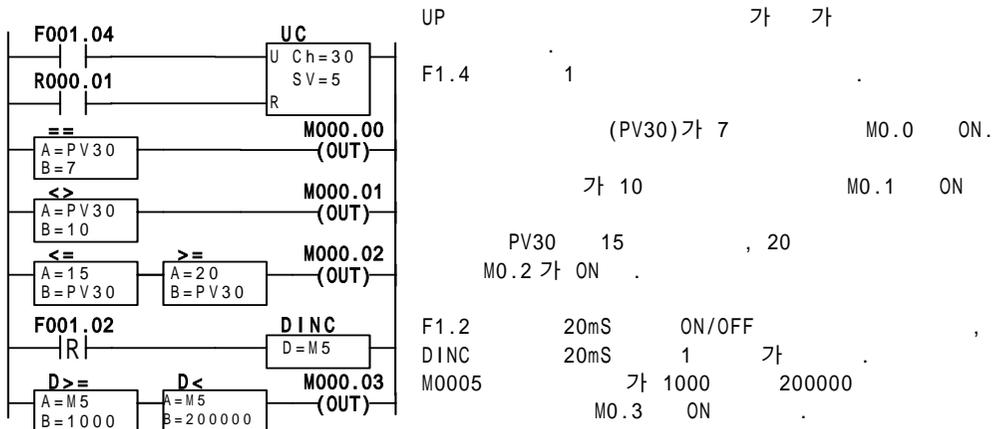
SPC-120/24	NX-p,Nplus
412	K4.10
413	K4.11
414	K4.12
415	K4.13
416	K4.14
417	K4.15
420	K5.00
421	K5.01
422	K5.02
423	K5.03

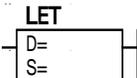
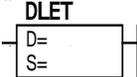
SPC-120/24	NX-p,Nplus
20	M2.00
21	M2.01
22	M2.02
23	M2.03
24	M2.04
25	M2.05
26	M2.06
27	M2.07
30	M2.08
31	M2.09

SPC-120/24	NX-p,Nplus
32	M2.10
33	M2.11
34	M2.12
35	M2.13
36	M2.14
37	M2.15
40	M3.00
41	M3.01
42	M3.02
43	M3.03

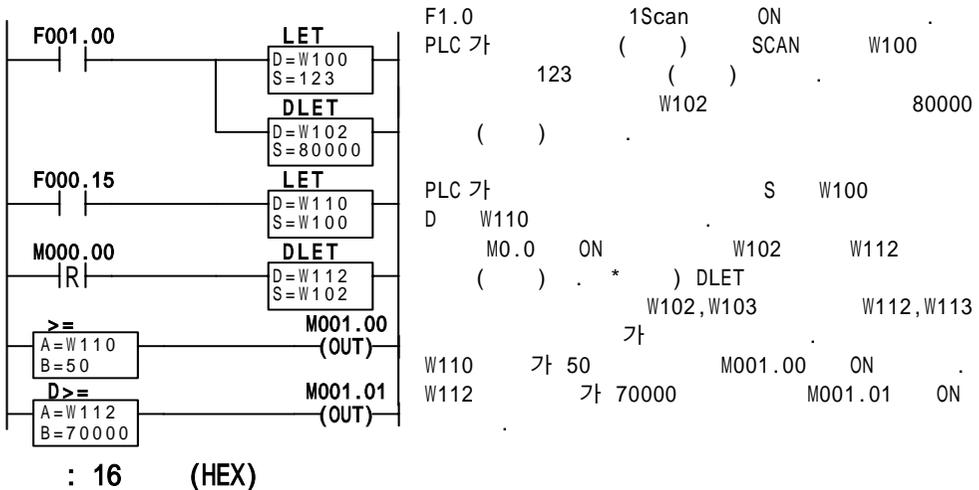
STR == AND == OR ==	3		A = B	A B ON. A,B
STR D== AND D== OR D==	4		A = B	A B ON. A,B
STR <> AND <> OR <>	3		A B	A B ON. <> A,B
STR D<> AND D<> OR D<>	4		A B	A B ON. <> A,B
STR > AND > OR >	3		A > B	A B ON. A,B
STR D> AND D> OR D>	4		A > B	A B ON. A,B
STR >= AND >= OR >=	3		A B	A B ON. A,B
STR D>= AND D>= OR D>=	4		A B	A B ON. A,B
STR <= AND <= OR <=	3		A B	A B ON. A,B
STR D<= AND D<= OR D<=	4		A B	A B ON. A,B
STR < AND < OR <	3		A < B	A B ON. A,B
STR D< AND D< OR D<	4		A < B	A B ON. A,B

1. A B R, L, M, K, W, SV, PV, SR ()
2. 16 (65,535) , 32 (4,294,967,295)
3. STR, AND, OR
4. ON , A B

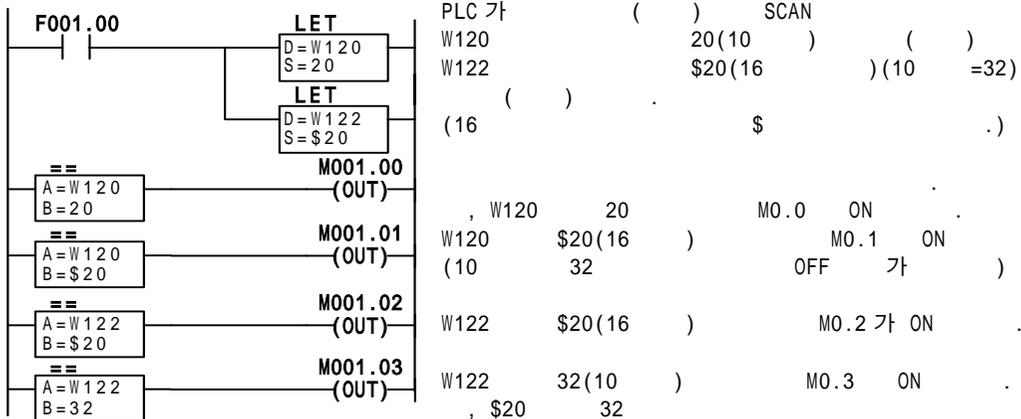


LET	3		(D= () , S= ()) (S=Source, D=Destination)
DLET	4		(D= (S D) , S= ())

1. D S ()
2. () 가
D R, L, M, K, W, SV, PV, SR ()
S LET 16 (65,535) , DLET
32 (4,294,967,295)
3. , Root
F0.15 (ON) ' a '



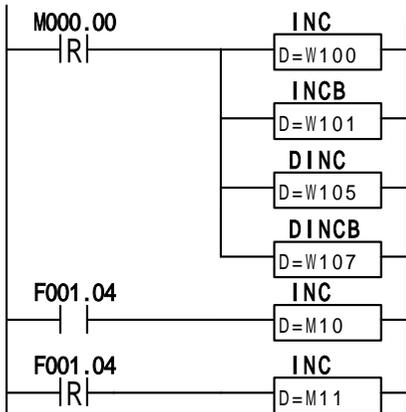
F1.0 1Scan ON
PLC 가 () SCAN W100
123 ()
W102 80000
PLC 가 S W100
D W110
MO.0 ON W102 W112
() *) DLET
W102, W103 W112, W113
가
W110 가 50 M001.00 ON
W112 가 70000 M001.01 ON



- 가

INC	2		2 가 (10 가) - 1 (Binary Increment)
DINC	2		2 가 (10 가) -
INCB	2		BCD 가 - 1 (BCD Increment)
DINCB	2		BCD 가 -

1. 가 D 가 1 가 가 , Binary 가 BCD 가 가
2. Binary 가 가 , BCD 가 BCD 가 4 가 , 16 A F
3. D R,L,M,K,W,SV,PV,SR () 가 16 (65,535) , 32 (4,294,967,295) 가
4. 가 Overflow 가 0 ,
5. 가 , Root , 가



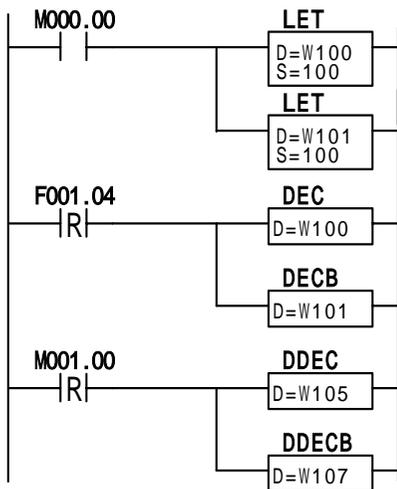
M1.0 ON 1Scan () 가 가 , INC Binary(10) 1 , INCB BCD 1 가, DINC Binary(10) 2 , DINCB BCD 2 가 M10 M11 , F1.4 0.5 ON, 0.5 OFF 'a' M10 ON SCAN 1 가 , M11 1 1 가

) BCD ?

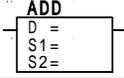
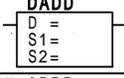
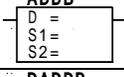
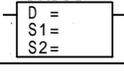
BCD ' Binary Coded Decimal' ' 2 10 ' , 4 10 10 2 . , 10 10 23 BCD 0010 0011 , 16 \$23 10 57 BCD 0101 0111 , 16 \$57 ,10 87 BCD 0 \$99999999 (10 2,576,980,377)

DEC	2		2 (10) - 1 (Binary Decrement)	
DDEC	2		2 (10) -	
DECB	2		BCD - 1 (BCD Decrement)	
DDECB	2		BCD -	

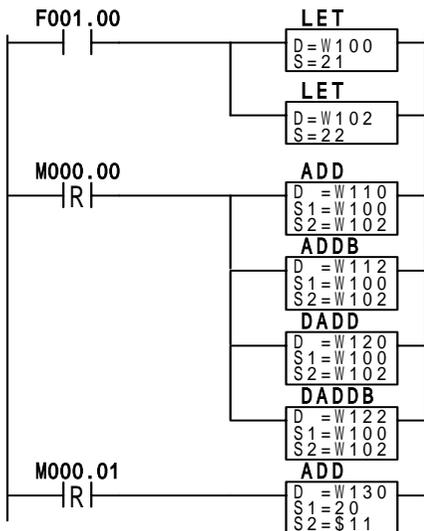
1. D 가 1 가 , Binary BCD 가 .
2. Binary , BCD BCD 4 , 16 A F ().
3. D R, L, M, K, W, SV, PV, SR () , 16 (65,535) , 32 (4,294,967,295) .
4. 0 가 Overflow 가 , 1 .
5. , Root ,



MO.0 ON W100, W101 100
 F1.4 1 ON 가
 가 , .
 , DEC Binary 1 ,
 DECB BCD 1
 DDEC DDECB W105, W107
 '0' 1
 DDEC Binary 2 ,
 DDECB BCD 2

ADD	4		2 (10) - 1 (Binary addition)	
DADD	5		2 (10) -	
ADDB	4		BCD - 1 (BCD addition)	
DADDB	5		BCD -	

1. S1 S2 D 가 , Binary
2. BCD Binary , BCD BCD 4
3. S1, S2 () (R, L, M, K, W, SV, PV, SR)
4. BCD (ADDB, DADDB) S1 S2 () BCD
5. Binary 16 (65,535) , 32 (4,294,967,295)
6. BCD 0 \$99999999 (10 2,576,980,377) 가
7. 65530 + 10 F1.8 ON , 65536



CPU 가 F1.0 SCAN ON

W100 10 21(16 \$15)

W102 10 22(16 \$16)

M000.00 4 가

ADD 10 21+22=43

ADDB BCD 21+22=49 가

BCD

\$15 + \$16 = \$31 , \$31=49(10)

DADD DADDB 16

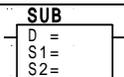
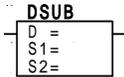
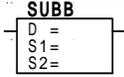
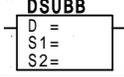
W122 , W120 43

\$31(10 49)

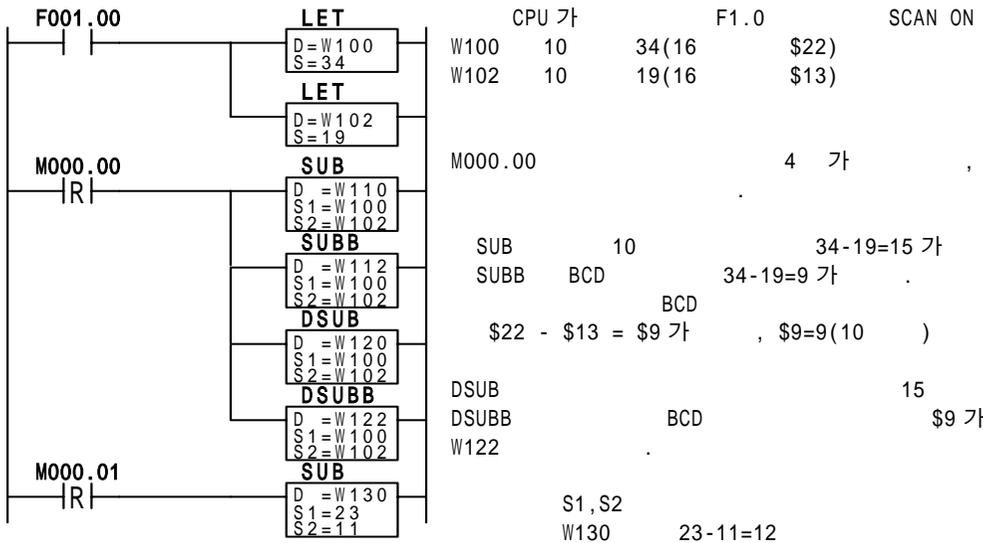
S1, S2

D 22+17(\$11)=42

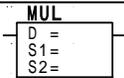
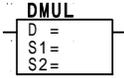
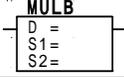
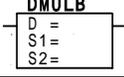
()

SUB	4		2 (10) - 1 (Binary subtraction)	
DSUB	5		2 (10) -	
SUBB	4		BCD - 1 (BCD subtraction)	
DSUBB	5		BCD -	

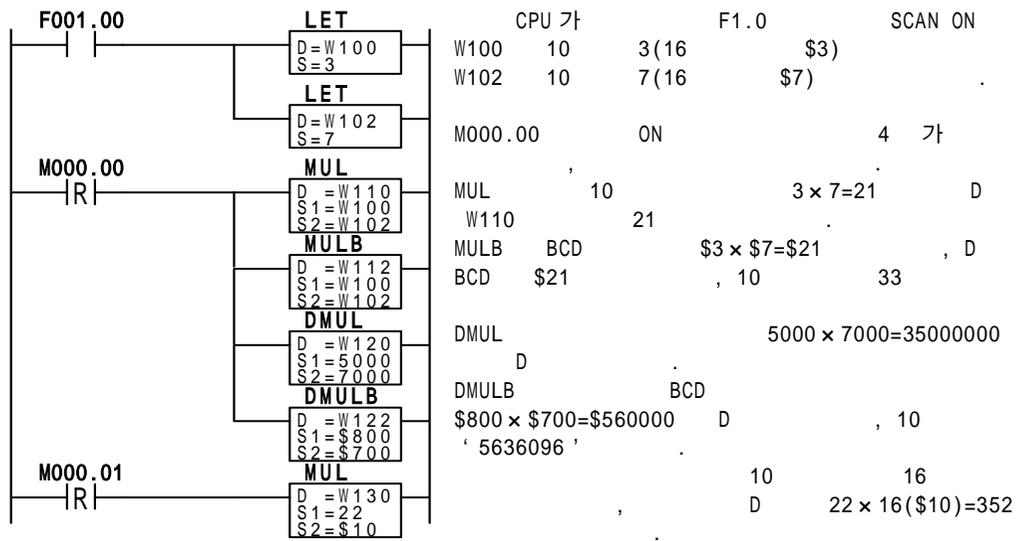
1. S1 S2 D 가 , Binary BCD
2. Binary , BCD BCD 4 , HEX ()
3. S1, S2 () (R, L, M, K, W, SV, PV, SR) , D ()
4. BCD (SUBB, DSUBB) S1 S2 () BCD \$ (, \$10, \$30)
5. Binary 16 (65,535) , 32 (4,294,967,295) , BCD 0 \$9999(10 39,321) , BCD 0 \$99999999(10 2,576,980,377)
6. ()가 ON () 10 10-20 -10 F1.8 ON , 65536 10 65526 -10
7. , Root



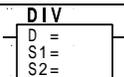
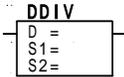
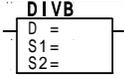
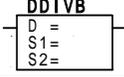
- ()

MUL	4		2 (10) - 1 (Binary multiplication)
DMUL	5		2 (10) -
MULB	4		BCD - 1 (BCD multiplication)
DMULB	5		BCD -

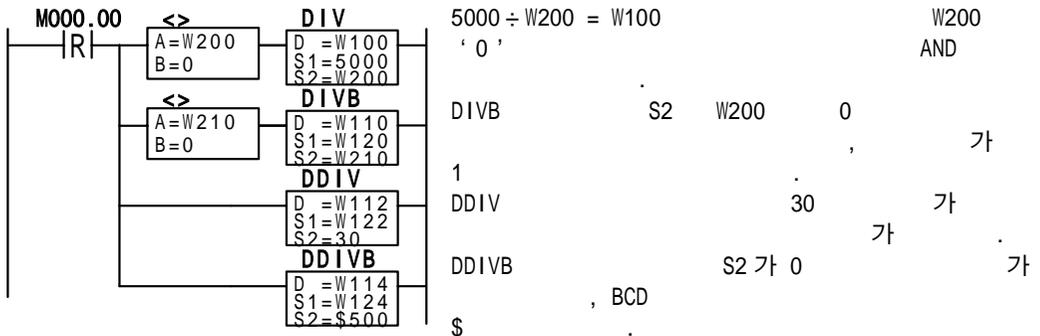
1. S1 S2 D 가 , Binary
BCD
2. Binary , BCD BCD , HEX
()
3. S1, S2 () (R, L, M, K, W, SV, PV, SR)
4. BCD (MULB, DMULB) S1 S2 () BCD
\$ (, \$100, \$300)
5. Binary 16 (65,535) , 32 (4,294,967,295)
BCD 0 \$9999(10 39,321)
BCD 0 \$99999999(10 2,576,980,377)
6. SR20
ON D
MUL 20*3500 70000 SR20 1(65536)
F1.8 ON , 4464 D
7. , Root



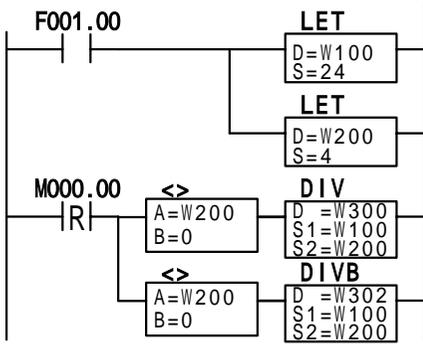
()

DIV	4		2 (10) - 1 (Binary division)	
DDIV	5		2 (10) -	
DIVB	4		BCD - 1 (BCD division)	
DDIVB	5		BCD -	

1. S1 S2 (D = S1 ÷ S2) D 가
, Binary BCD
2. () (SR22)
SR23
3. (S2) '0' 가 ()가 CPU
(F1.9)(가 0) ON ,
LED
'0'
4. Binary , BCD BCD , HEX
()
5. S1, S2 () (R, L, M, K, W, SV, PV, SR)
6. BCD (DIVB, DDIVB) S1 S2 () BCD
\$ (, \$100, \$300)
7. Binary 16 (65,535) , 32 (4,294,967,295)
, BCD 0 \$9999(10 39,321)
BCD 0 \$99999999 (10 2,576,980,377) 가
8. , Root

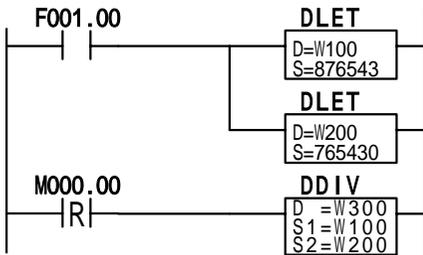


1 ()



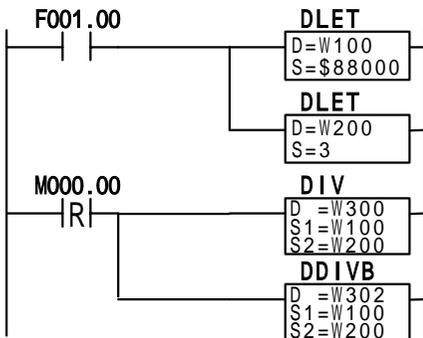
Scan W100 24, W200 4 Data
 MO.0 ON W200 0
 $W100 \div W200 = W300$
 $24 \div 4 = 6$
 BCD W100 BCD \$18(24)
 $\$18 \div \$4 = 4$, 가 2
 W302 \$4 가 , 2 SR022

2 ()



Scan W100 876543, W200 765430
 Data
 MO.0 ON , 876543 ÷ 765430= 1 ,
 111113 (\$1B209)
 SR22 , (SR23)
 \$0001 , (SR22)
 45577(\$B209)가

3



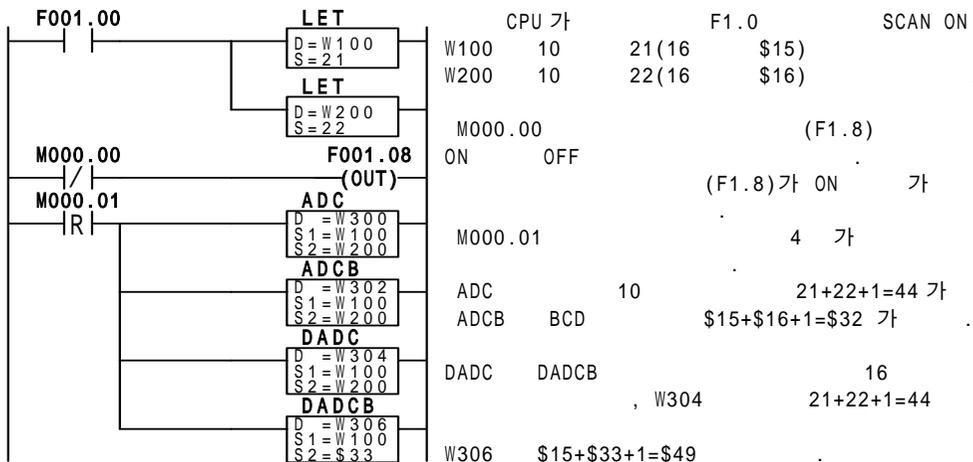
Scan W100 \$88000(10
 557056) , W200 3
 MO.0 ON , DIV
 W100 1 , W100 \$8000 ,
 $32768(\$8000) \div 3 = 10922$, 가 2
 , W300 10922 가 ,
 SR22 2 가 .
 BCD DDIVB
 $\$88000 \div \$99000 = 0$, \$88000
 W302 0 , SR22=
 \$88000 , SR22 \$8000, SR23 \$0008

		()	
ADC	4		$D = S1 + S2 + CY$, () 2 (Decimal addition with carry) 1)
DADC	5		$D = S1 + S2 + CY$, () 2 (Decimal addition with carry) 1)
ADCB	4		$D = S1 + S2 + CY$, () BCD (BCD addition with carry) 1)
DADCB	5		$D = S1 + S2 + CY$, () BCD (BCD addition with carry) 1)

1)

SPC-10	SPC100 24S/120S	SPC300	A200	N70 plus 9215A, 9216A	NX70 plus CPU70p1/V2, CPU70p2/V2	N/NX700plus 7215A, CPU700p	NX700plus CPU700p/V2
x	x						

- ADC() S1 S2, (F1.8) D
가 , Binary BCD
- Binary , BCD BCD 4
, HEX ()
- S1, S2 () (R, L, M, K, W, SV, PV, SR)
- BCD (ADCB, DADCB) S1 S2 () BCD
, \$ (, \$100, \$300)
- Binary 16 (65,535) , 32 (4,294,967,295)
, BCD 0 \$9999(10 39,321)
BCD 0 \$99999999 (10 2,576,980,377) 가
- ON ()
65530 + 10 F1.8 ON , 4
- , Root

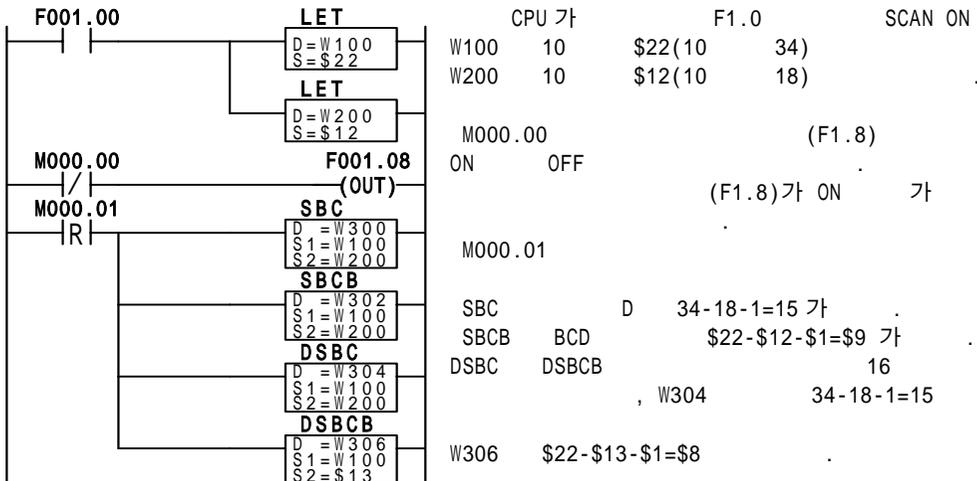


SBC	4		$D = S1 - S2 - CY, ()$ 2 (Binary subtraction W/Carry)	1)
DSBC	5		$D = S1 - S2 - CY, ()$ 2 (Binary subtraction W/Carry)	1)
SBCB	4		$D = S1 - S2 - CY, ()$ BCD (BCD subtraction W/Carry)	1)
DSBCB	5		$D = S1 - S2 - CY, ()$ BCD (BCD subtraction W/Carry)	1)

1)

SPC-10	SPC100 24S/120S	SPC300	A200	N70 plus 9215A, 9216A	NX70 plus CPU70p1/V2, CPU70p2/V2	N/NX700plus 7215A, CPU700p	NX700plus CPU700p/V2
x	x						

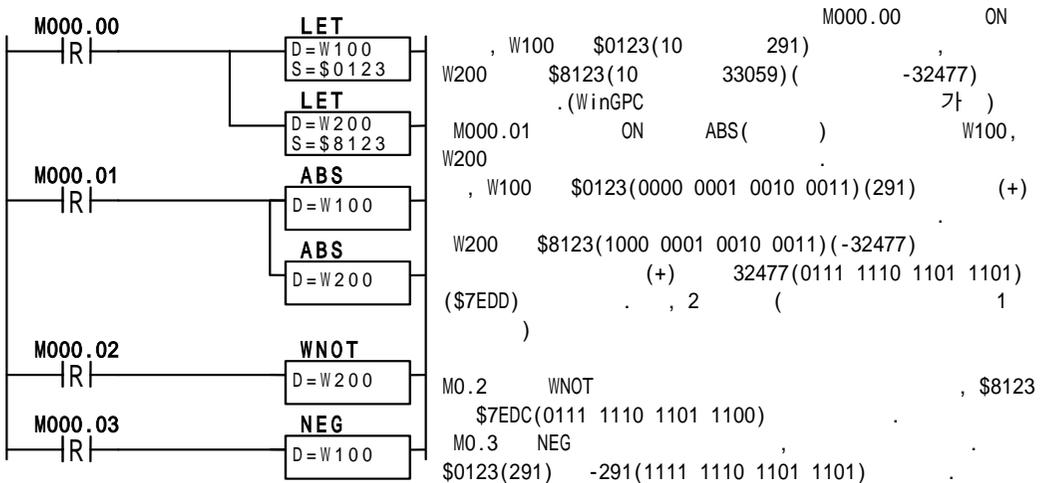
- SBC() S1 S2 (F1.8) D
가 , Binary BCD , HEX
- Binary , BCD BCD , HEX
- S1, S2 () (R, L, M, K, W, SV, PV, SR)
- BCD (SBC, DSBC) S1 S2 () BCD
\$ (, \$10, \$30)
- Binary 16 (65,535) 32 (4,294,967,295)
BCD 0 \$9999(10 0 \$9999(10 39,321)
0 \$99999999 (10 2,576,980,377) 가
- 10 ()가 ON ()
10-20 -10
F1.8 ON 65536 10 65526
-10
- Root



(,)

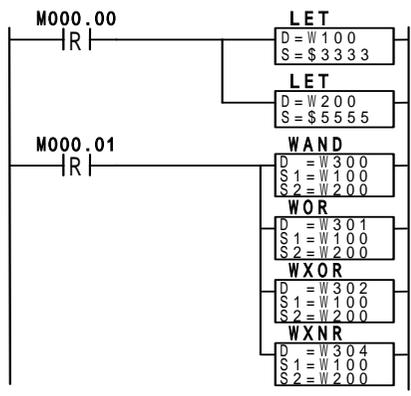
ABS	2		Absolute value (, D = D) ()
DABS	2		Absolute value (, D = D) ()
WNOT	2		NOT (, 1) ()
DNOT	2		NOT (, 1) ()
NEG	2		2 D (1 +1 =) Negative ()
DNEG	2		2 D (1 +1 =) Negative ()

- ABS() (MSB)가 1 2 , 0 , 10 + , + .
- ABS() DABS()
- WNOT(1) ()
- WNOT() DNOT()
- NEG(2 , , Negative) ()
- NEG() DNEG()
- D () (R,L,M,K,W,SV,PV,SR)
- 16 (65,535) , 32 (4,294,967,295)
- Root



WAND	4		(Word AND :)	S1 S2 D	S1 0 0 1 1 S2 0 1 0 1 D 0 0 0 1
DAND	5		(D-Word AND :)	S1 S2 D	S1 0 0 1 1 S2 0 1 0 1 D 0 0 0 1
WOR	4		(Word OR :)	S1 S2 D	S1 0 0 1 1 S2 0 1 0 1 D 0 1 1 1
DOR	5		(D-Word OR :)	S1 S2 D	S1 0 0 1 1 S2 0 1 0 1 D 0 1 1 1
WXOR	4		(Word Exclusive OR)	S1 S2 D	S1 0 0 1 1 S2 0 1 0 1 D 0 1 1 0
DXOR	5		(Exclusive OR :)	S1 S2 D	S1 0 0 1 1 S2 0 1 0 1 D 0 1 1 0
WXNR	4		(Word Exclusive OR NOT)	S1, S2 D ()	S1 0 0 1 1 S2 0 1 0 1 D 1 0 0 1
DXNR	5		(Exclusive OR Not :)	S1, S2 D ()	S1 0 0 1 1 S2 0 1 0 1 D 1 0 0 1

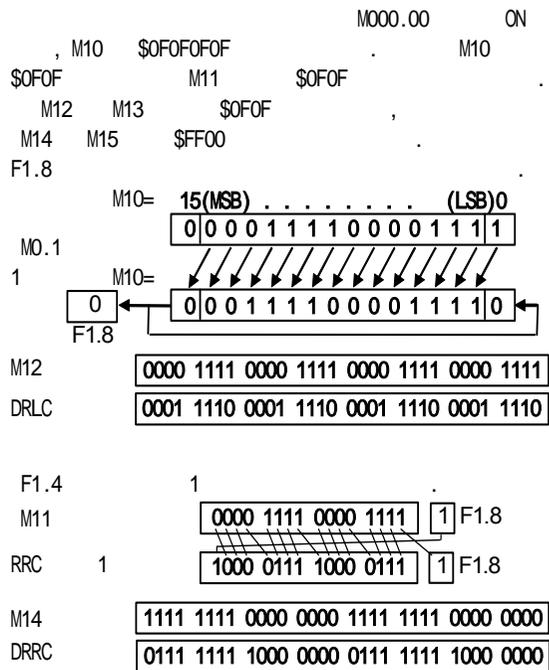
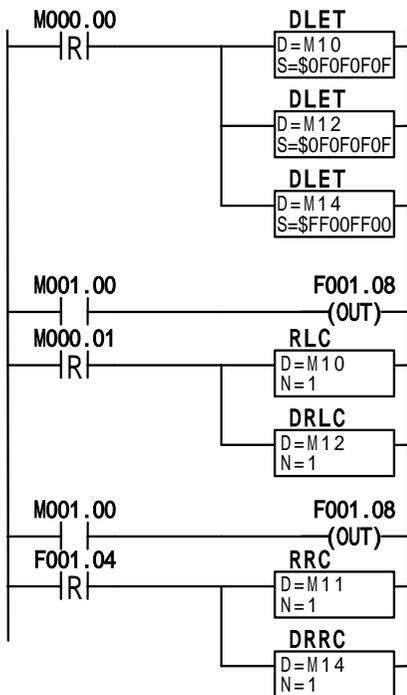
1. WAND(DAND) S1 S2 (S1 S2 가 1 1) D
2. WOR(DOR) S1, S2 (S1, S2 가 1 1 가 1) D
3. WXOR(DXOR) S1, S2 1 1 가 1 D
4. WXNR(DXNR) () S1, S2 가 1 D
5. S1, S2 () (R, L, M, K, W, SV, PV, SR) D ()



M000.00 ON
 , W100 \$3333(0011 0011 0011 0011)
 W200 \$5555(0101 0101 0101 0101)
 M000.01 ON
 가 D
 , WAND W300 \$1111(0001 0001 0001 0001)
 WOR W301 \$7777(0111 0111 0111 0111),
 WXOR W302 \$6666(0110 0110 0110 0110),
 WXNR W304 \$9999(1001 1001 1001 1001)가

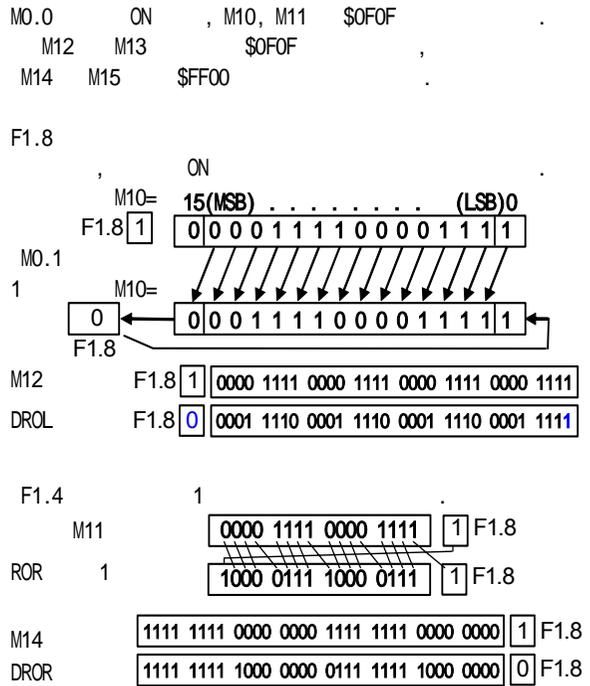
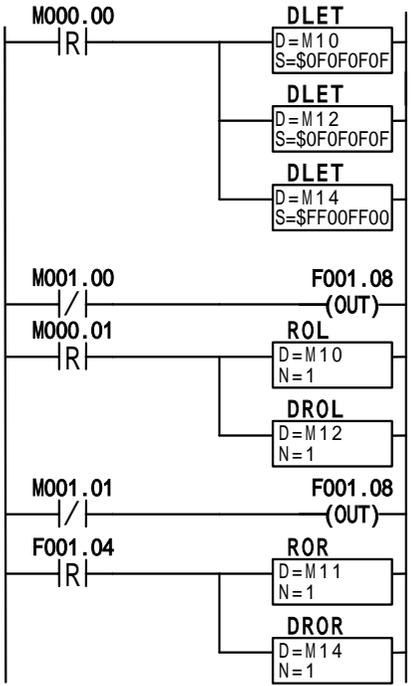
RLC	3		(Rotate left) ()
DRLC	4		(Rotate left) ()
RRC	3		(Rotate Right) ()
DRRC	4		(Rotate Right) ()

1. RLC(DRLC) D (MSB) N (F1.8) () ,
2. RRC(DRRC) D (LSB) N (F1.8) () ,
3. D () (R, L, M, K, W, SR) , N 0 15()
4. 0 31() , Root



ROL	3		(Rotate left) ()
DROL	4		(Rotate left) ()
ROR	3		(Rotate Right) ()
DROR	4		(Rotate Right) ()

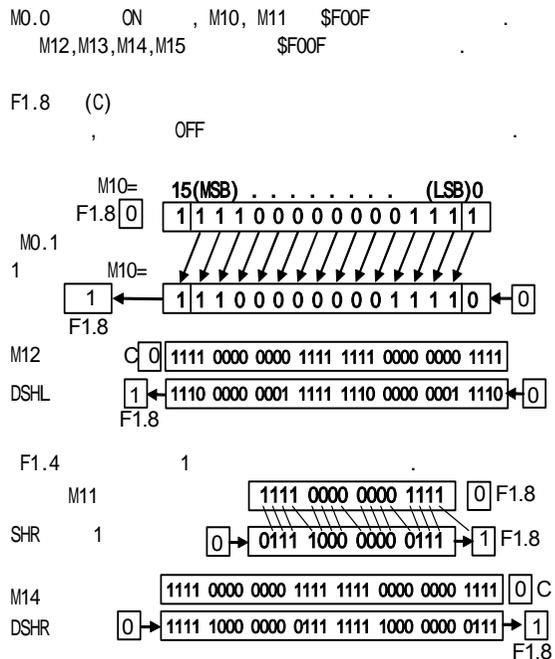
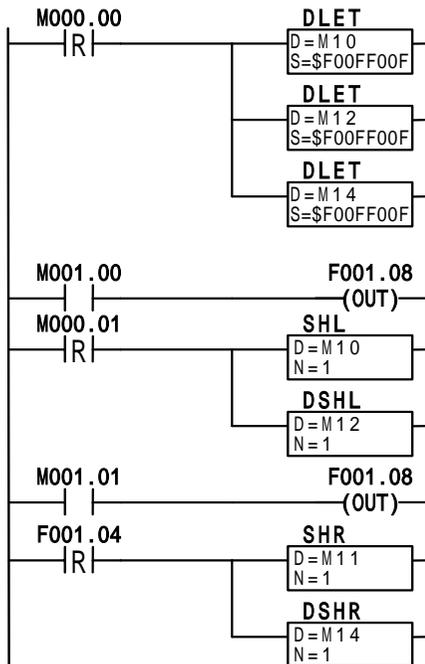
1. ROL(DROL) D (MSB) (F1.8) N (LSB) ,
2. ROR(DROR) D (LSB) (F1.8) N (MSB) ,
3. D () (R,L,M,K,W,SR) , N 0 15()
4. , Root



- (/)

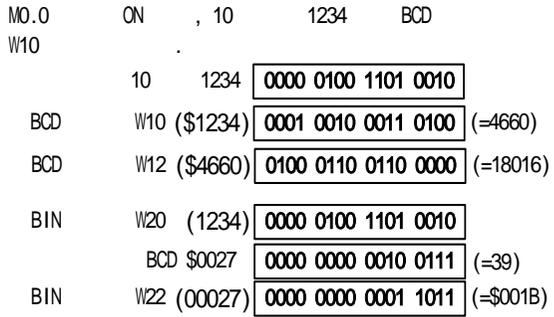
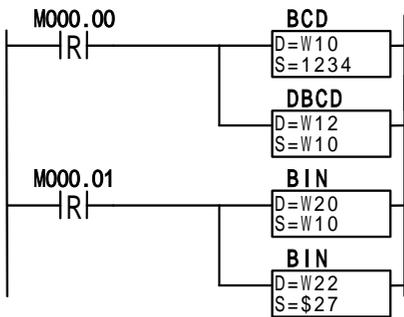
SHL	3		(Shift left) (, 0)
DSHL	4		(Shift left) (, 0)
SHR	3		(Shift Right) (, 0)
DSHR	4		(Shift Right) (, 0)

- SHL(DSHL) D N () , (MSB) (F1.8) , 0 (LSB) .
- SHR(DSHR) D N () , (LSB) (F1.8) , 0 (MSB) .
- D () (R,L,M,K,W,SR) , N 0 15() 0 31()
- Root



BCD	3		S 2 BCD D ()) S= 00063 (10) → D= \$0063(BCD) 000000000001111111 000000000011000111
DBCD	3		S 2 BCD D ()
BIN	3		S BCD 2 D ()) S= \$0039 (BCD) → D= 00039(10 , Binary) 000000000001110001 000000000001001111
DBIN	3		S BCD 2 D ()

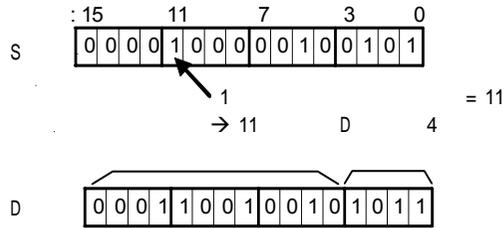
1. BCD(DBCD) S Binary BCD D , S BCD
2. BIN(DBIN) S BCD binary D , S BCD
3. (BCD, BIN) 0 9999(10) (16 \$270F) ,
(DBCD,DBIN) 0 99999999 (16 \$05F5E0FF)
4. D () (R,L,M,K,W,SR) , S
5. , Root



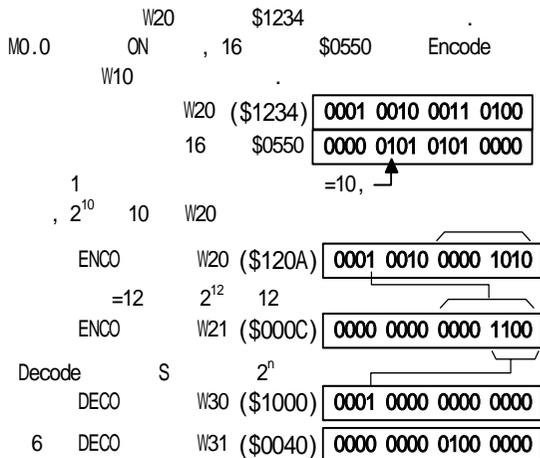
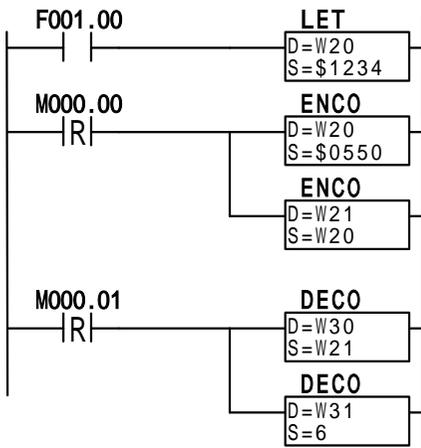
) BCD ?
 BCD ' Binary Coded Decimal'
 4 10
 , 10 10
 10 23(0001 0111) BCD
 10 57 BCD 0101 0111 , 16 \$57 , 10 87
 WinGPC
 10 /16 /2
 BCD 0 \$9999(10 39,321 , BCD
 0 \$99999999 (10 2,576,980,377)

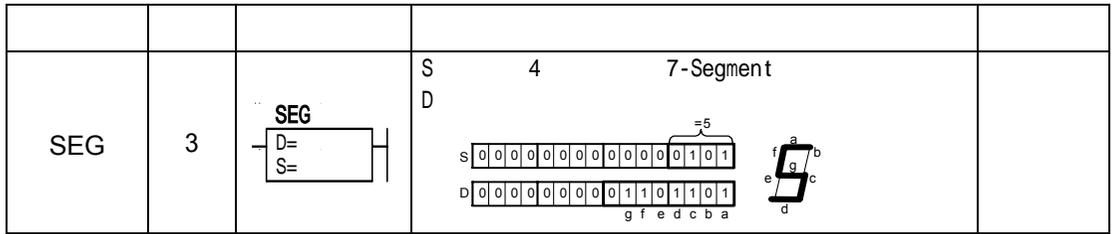
ENCO	3		S D	8421 Encode	
DECO	3		S	8421 Decode	D

- ENCO S 1 (2ⁿ n)
D 8 , D
- (, SPC 2ⁿ n+1 D)

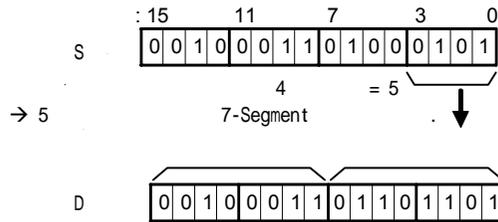


- DECO S 4 (2ⁿ) D
- D (R, L, M, K, W, SR) , S
- Root

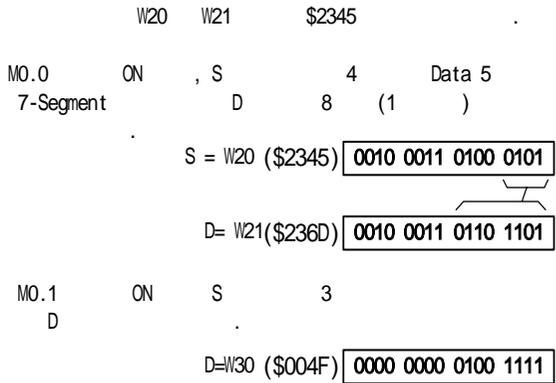
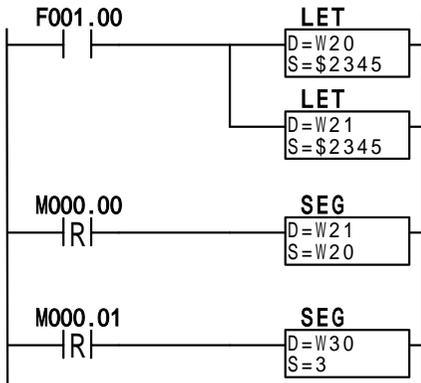




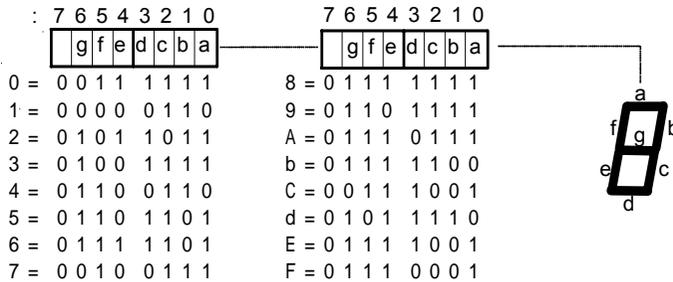
1. SEG S 4 7- D 8



2. SEG D
3. D (R, L, M, K, W) , S
4. , Root



) 7-Segment

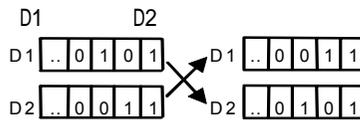


XCHG	3		D1 D2 ()	1)
DXCHG	3		D1 D2 ()	1)

1)

SPC-10	SPC100 24S/120S	SPC300	A200	N70 plus 9215A, 9216A	NX70 plus CPU70p1/V2, CPU70p2/V2	N/NX700plus 7215A, CPU700p	NX700plus CPU700p/V2
x	x						

1. XCHG (DXCHG)

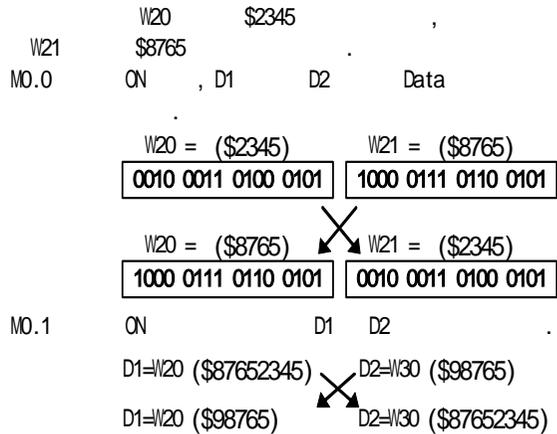
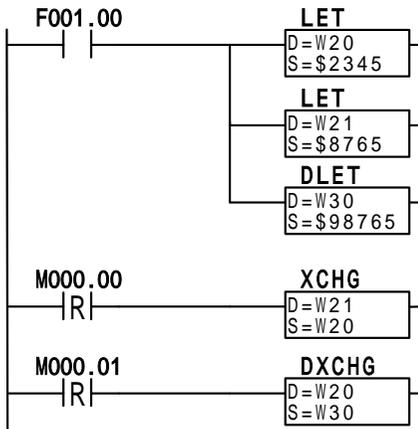


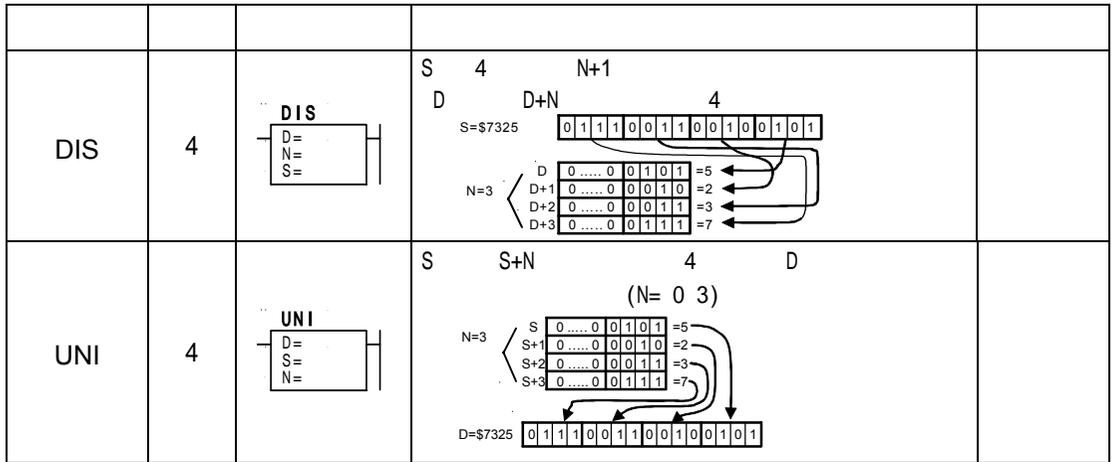
2. D1, D2

(R, L, M, K, W)

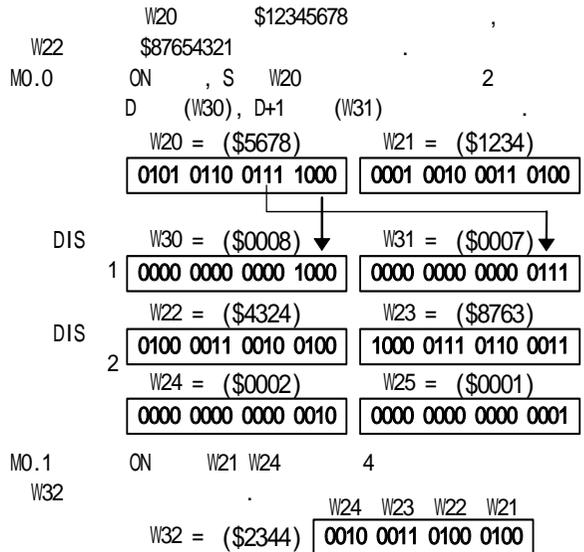
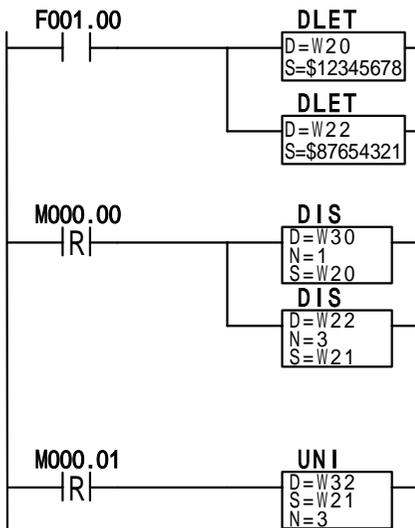
3.

, Root



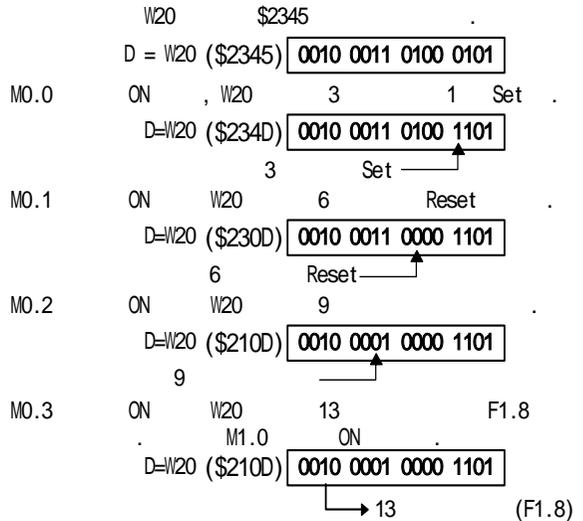
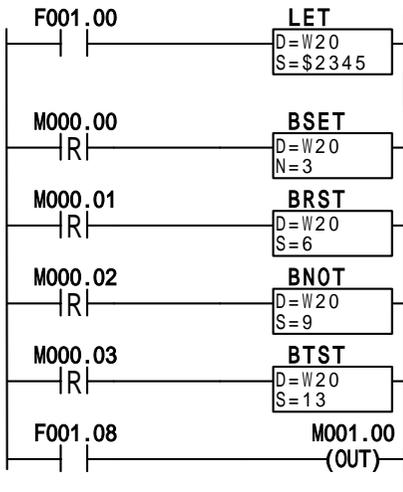


1. DIS 4 (1)
2. UNI 4 1
3. D, S (R,L,M,K,W) , N () 0 3
4. , Root



BSET	3		D N 1 SET D 0 0 1 0 0 1 0 0 N=5 (N=0~15)
BRST	3		D N 0 () D 0 1 0 1 0 1 0 0 N=3 0
BNOT	3		D N . (0 → 1, 1 → 0) D 0 1 1 1 0 1 0 0 N=4 D 0 1 1 0 0 1 0 0
BTST	3		D N F1.8() D 0 1 1 1 0 1 0 0 N=6 F1.8

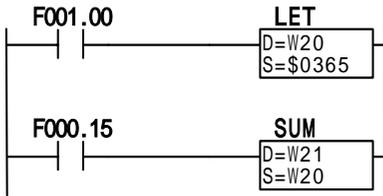
- 1.
2. N
3. D (R, L, M, K, W, SR) , N 0 15
4. , Root



SUM	3		S 1 D S 0001101001101001 1 =7 D 000000000000000111 D=7
-----	---	--	--

1. SUM S ON(=1) Set D
2. D S (R,L,M,K,W, SR)
3. , Root

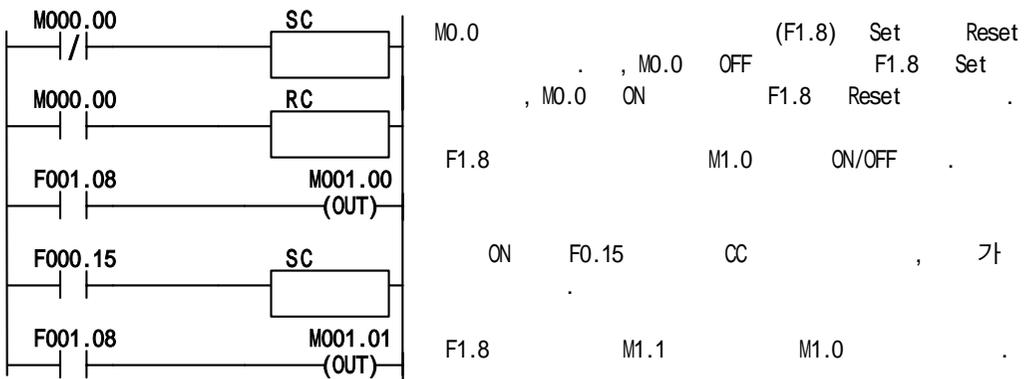
1.



W20 \$0365
 S = W20 (\$0365) 0000 0011 0110 0101
 ON F0.15 S
 D Data
 D=W21 (\$0006) 0000 0000 0000 0110

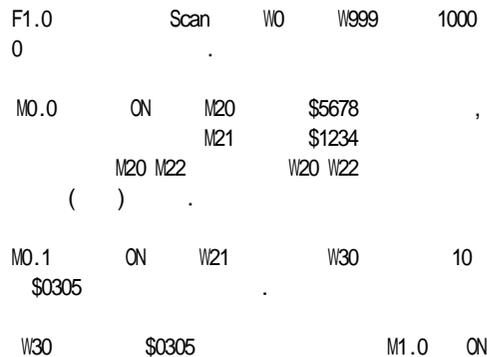
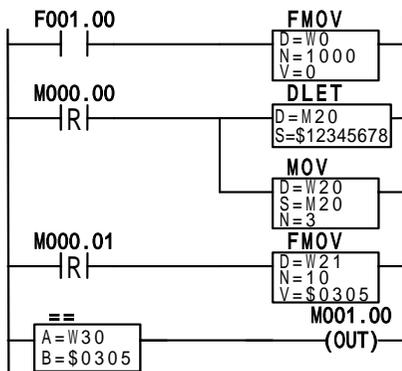
SC	1		(F1.8) 1 SET 1 → [F1.8]	
RC	1		(F1.8) 0 RESET 0 → [F1.8]	
CC	1		(F1.8) [F1.8] 1 → 0 [F1.8] 0 → 1	

1. (F1.8) Set Reset
2. (F1.8) SC, RC, CC
- 3.
4. (F1.8)
5. , Root

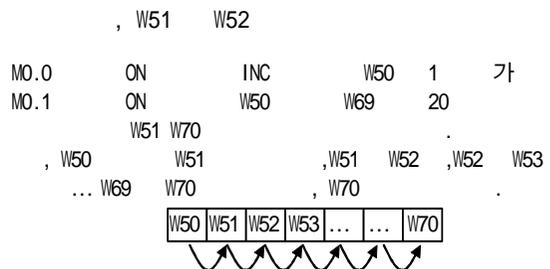
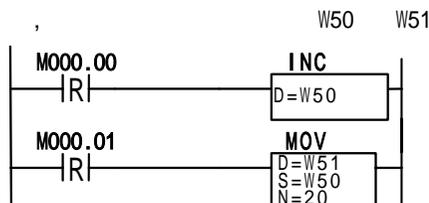


MOV	4		<p>S N (S)</p> <p>D N</p> <p>S 1 0 1 0 1 0 1 0</p> <p>S+1 0 0 0 0 1 1 1 1</p> <p>S+2 1 1 1 1 0 0 0 0</p> <p>→</p> <p>D 1 0 1 0 1 0 1 0</p> <p>D+1 0 0 0 0 1 1 1 1</p> <p>D+2 1 1 1 1 0 0 0 0</p>
FMOV	4		<p>V D N</p> <p>V 1 0 1 0 1 0 1 0</p> <p>N=4</p> <p>→</p> <p>D 1 0 1 0 1 0 1 0</p> <p>D+1 1 0 1 0 1 0 1 0</p> <p>D+2 1 0 1 0 1 0 1 0</p> <p>D+3 1 0 1 0 1 0 1 0</p>

1. () MOV ,
2. MOV D S (R,L,M,K,W, SR) , N
3. FMOV D (R,L,M,K,W, SR) , N
4. , V 16 , Root
- 5.

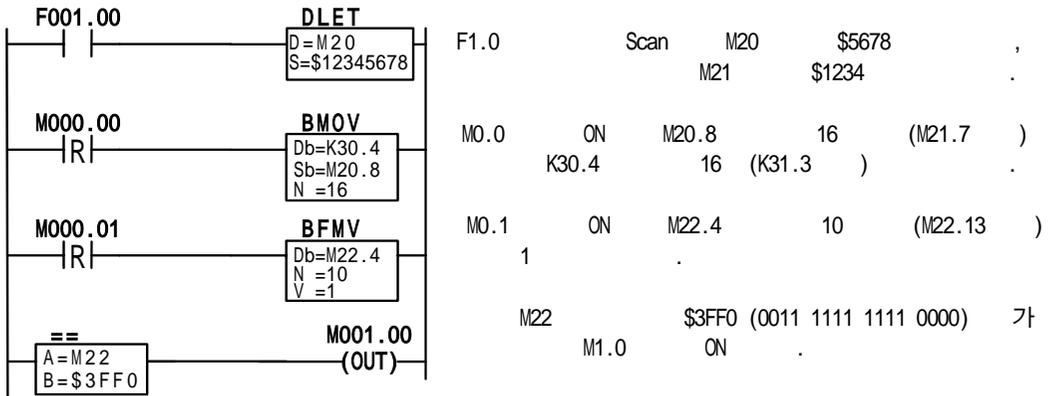


1. Data



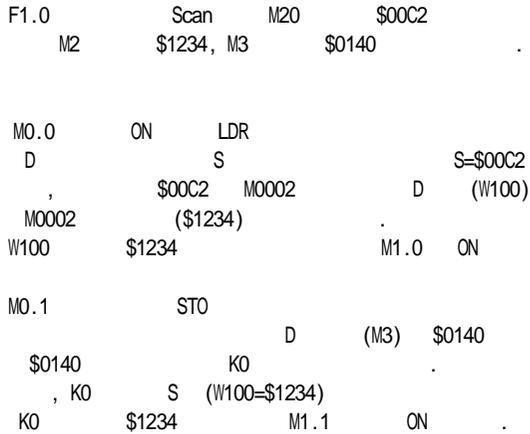
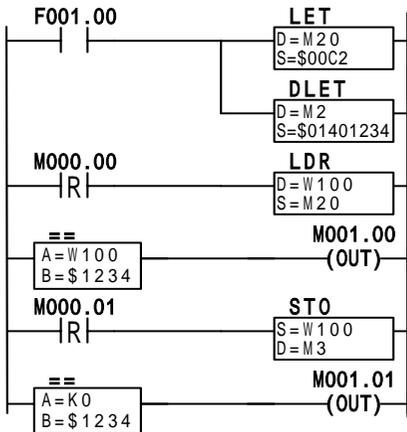
BMOV	4		<p>Sb N Db N</p> <p>(Sb, Db 가)</p>	
BFMV	4		<p>V Db N</p> <p>(V=0 1) (N=1...256,) (Db)</p> <p>) V=1, N=5</p>	

1. () BMOV , .
2. BMOV Db Sb (R, L, M, K) , N 1 256
3. BFMV Db (R, L, M, K) , N 1 256
4. V 0 1 , Root , .



LDR	3		(S		D)
DLDR	3					
STO	3		(D		S)
DSTO	3					

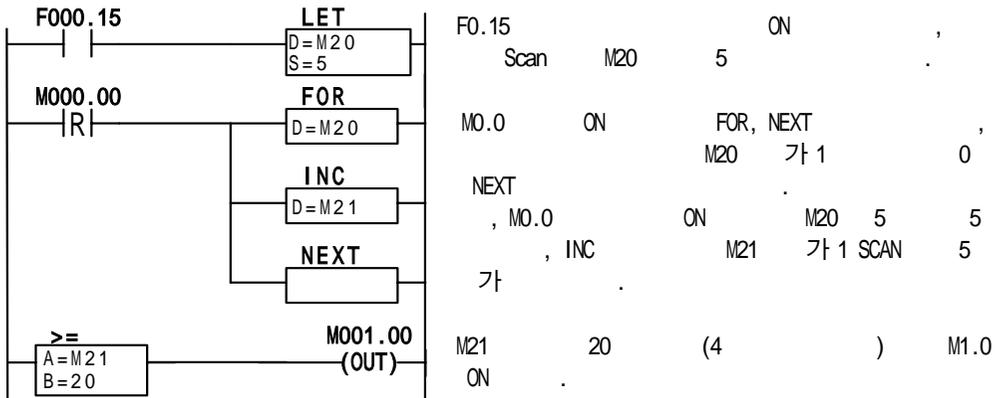
1. () ,
2. (R, M, K, W) CPU 16
3. LDR, DLDR S D 가
4. STO, DSTO D , Root



R000	\$0000	L000	\$0080	M000	\$01C0	K0000	\$0140	W000	\$0200
R001	\$0001	L001	\$0081	M001	\$01C1	K0001	\$0141	W001	\$0201
R002	\$0002	L002	\$0082	M002	\$01C2	K0002	\$0142	W002	\$0202
.....		
R0126	\$007E	L0062	\$00BE	M0126	\$013E	K0126	\$01BE	W2046	\$09FE
R0127	\$007F	L0063	\$00BF	M0127	\$013F	K0127	\$01BF	W2047	\$09FF

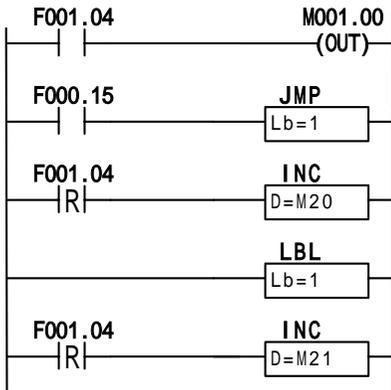
FOR	3	FOR D=	D () 1 D (D가 0)	NEXT (FOR Loop)
DFOR	3	DFOR D=	D () 1 D (D가 0)	NEXT (FOR Loop)
NEXT	2	NEXT	FOR	(FOR Loop)

- FOR(DFOR) D 0 NEXT (JMP, CALL)
- FOR D 0 NEXT 가
- FOR(DFOR) NEXT , NEXT 가
- NEXT OFF FOR(DFOR) 가
- D ON (R,L,M,K,W) ,FOR , DFOR
- FOR(DFOR) D ,
- FOR, DFOR , Root



JMP	3		LBL Lb () Lb=0~63 (가)	
LBL	2		JMP (가) Lb=0~63 (가)	

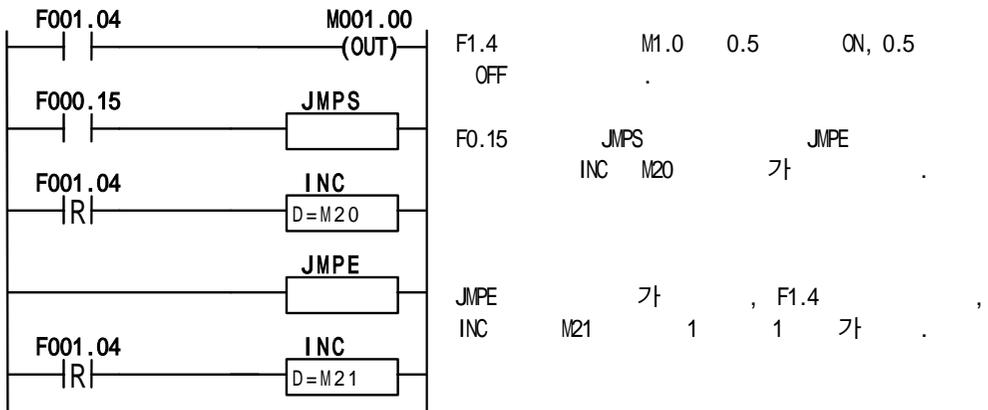
1. JMP , Lb 가 0 63 64 가 .
2. JMP LBL , Lb .
3. (JMP) (LBL) .
4. JMP LBL JMP .
5. JMP , Root , .
6. LBL Root , .



F1.4 1 ON/OFF
M1.0 0.5 ON, 0.5 OFF
F0.15 JMP
F1.4 INC(M20)
LBL Lb 1
LBL 가 , F1.4
INC M21 1 1 가

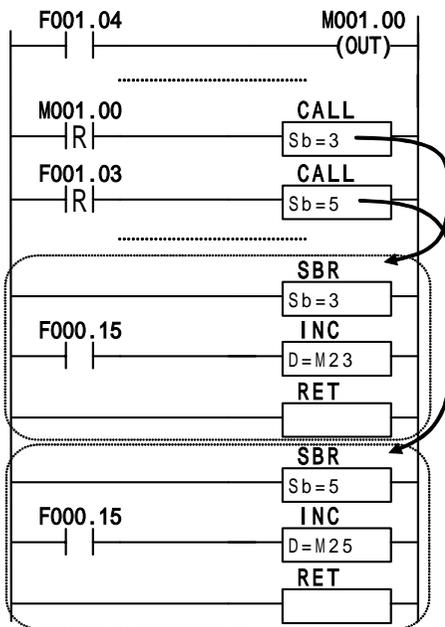
JMPS	2		JMPE ()	
JMPE	1		(JMPS) (JMPS)	

1. JMPS , 가 JMPE
2. JMPS JMPE , JMPS LBL
3. JMPS , Root
4. JMPE Root



CALL	3		
SBR	2		Sb=0 63(64 가)
RET	1		(Subroutine Return)

- CALL (Sb)
- RET CALL
- CALL SBR Sb 0 63 64 , CALL
- CALL SBR/RET Sb 가 , SBR RET
- CALL , Root
- SBR RET Root
- SBR RET SBR



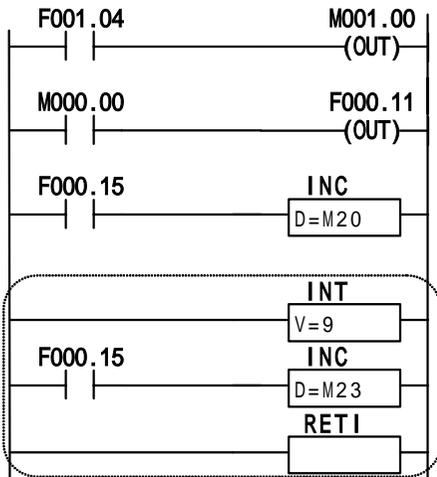
F1.4 M1.0 0.5 ON, 0.5
 OFF
 M1.0 CALL 3 1 3
 F0.15 INC
 1 가 M23 1 1
 가
 F1.3 0.2 , 0.1 ON,
 0.1 OFF
 , CALL 5 0.2 5
 M25 0.2 1 가 INC

INT	2		$V=1 \text{ 999}$ $= (V+1) \times 0.01$	(1 가) 가 , = F0.11 (20msec 10sec)	1)
RETI	1				1)

1)

SPC-10	SPC100 24S/120S	SPC300	A200	N70 plus 9215A, 9216A	NX70 plus CPU70p1/V2, CPU70p2/V2	N/NX700plus 7215A, CPU700p	NX700plus CPU700p/V2
x	x						

1. (INT RETI)
2. , 0.02 10
3. 10mSec V +1
4. = (V+1)*0.01 , V 3 , (3+1)*0.01=40mSec
5. F0.11 ON
6. INT RETI Root ,



F1.4 OFF M1.0 0.5 ON, 0.5

M0.0 ON INT , OFF

INT RETI

F0.15 M20 1 가

V 9 (9+1)*10mS=100mSec

, M23 100mSec 1 가

, M0.0 ON F0.11 ON

INPR	2		Ch	()	1)
OUTR	2		Ch	()	1)

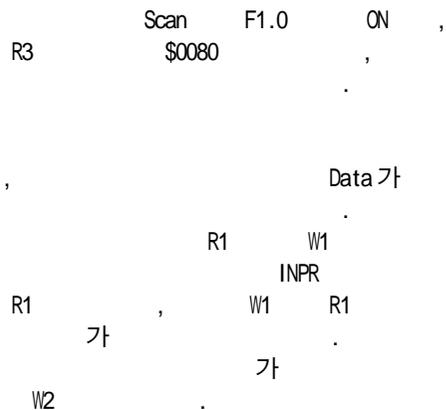
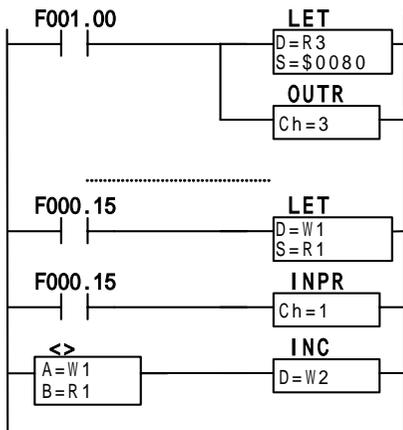
1)

SPC-10	SPC100 24S/120S	SPC300	A200	N70 plus 9215A, 9216A	NX70 plus CPU70p1/V2, CPU70p2/V2	N/NX700plus 7215A, CPU700p	NX700plus CPU700p/V2
x	x						

1. PLC CPU () () ()
2. INPR OUTR
3. INPR Update
4. OUTR Update
5. Ch 0 63 , Local ()

가 R0, R1, (R2, R3)

POWER	CPU	IN	IN	HSC	OUT	OUT	→
		16	16	(32)	16	16	→
		R0	R1	R2,3	R4	R5	→ ()



WAT	1		(0)	1)
END	1		(CPU)	

1)

SPC-10	SPC100 24S/120S	SPC300	A200	N70 plus 9215A,9216A	NX70 plus CPU70p1/V2,CPU70p2/V2	N/NX700plus 7215A,CPU700p	NX700plus CPU700p/V2
×	×						

1. WAT

2. CPU

(1 Scan Time)

3.

가

CPU

, Error

4.

가

, 가

3000mSec(3)

5.

가

WAT

6. WAT

, Root

7. END

CPU

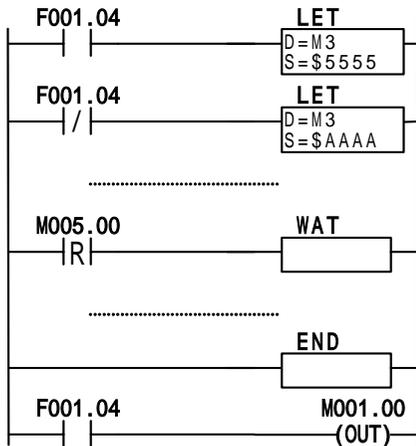
8.

9. END

Root

10. WAT, END

가



F1.4 M3 0.5 \$5555

0.5 \$AAAA

→

M5.0 ON 가

END

F1.4

M1.0

READ	5	READ TO=RR1 SZ=NR3 FR=NN5:NR6	Slot(NN5) (NN6) (NR3)	(RR1)	1)
------	---	---	-----------------------	-------	----

1)

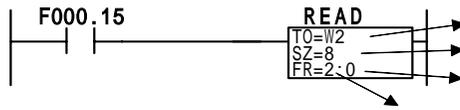
SPC-10	SPC100 24S/120S	SPC300	A200	N70 plus 9215A, CPU70p1, V2	NX70 plus 9216A, CPU70p2, V2	N/NX700plus 7215A, CPU700p	NX700plus CPU700p/V2
×	×	×	×	×			

) : NN= , NR= , RR=

1.

PLC CPU
 SCU , DeviceNet, 가 , , ,
 2. READ () PLC CPU 가
 3. RR1= (PLC CPU),
 NR3= ,
 NN5= (0 , ,)
 NR6= (/)
 4. READ , Root ,

POWER	CPU	IN 16	IN 32	A/I 8Ch	OUT 16	OUT 32	→
		RO	R1,2	R3	R4	R5,6	→
		0	1	2	3	4	→



()
 ()
 (8 =8)
 (A/D)
 (0 52)
 W2 0 7 W9 8

PLC CPU

0 0	5 0 0
0 1	1 0 0 0
0 2	1 5 0 0
0 3	2 0 0 0
0 4	2 5 0 0
0 5	3 0 0 0
0 6	3 5 0 0
0 7	4 0 0 0
...	...
5 2	...

CPU	
W 0 0 0 0	...
W 0 0 0 1	...
W 0 0 0 2	5 0 0
W 0 0 0 3	1 0 0 0
W 0 0 0 4	1 5 0 0
W 0 0 0 5	2 0 0 0
W 0 0 0 6	2 5 0 0
W 0 0 0 7	3 0 0 0
W 0 0 0 8	3 5 0 0
W 0 0 0 9	4 0 0 0
W 0 0 1 0	...

WRITE	5	<table border="1"> <tr> <td>WRITE</td> </tr> <tr> <td>TO=NN1:NR2</td> </tr> <tr> <td>SZ=NR3</td> </tr> <tr> <td>FR=NR5</td> </tr> </table>	WRITE	TO=NN1:NR2	SZ=NR3	FR=NR5	PLC / (NR5) (NR3) (NN1) (RR2)	1)
WRITE								
TO=NN1:NR2								
SZ=NR3								
FR=NR5								

1)

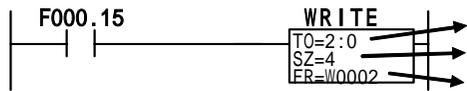
SPC-10	SPC100 24S/120S	SPC300	A200	N70 plus 9215A, CPU70p1, V2	NX70 plus 9216A, CPU70p2, V2	N/NX700plus 7215A, CPU700p	NX700plus CPU700p/V2
×	×	×	×	×			

) : NN= , NR= , RR=

1.

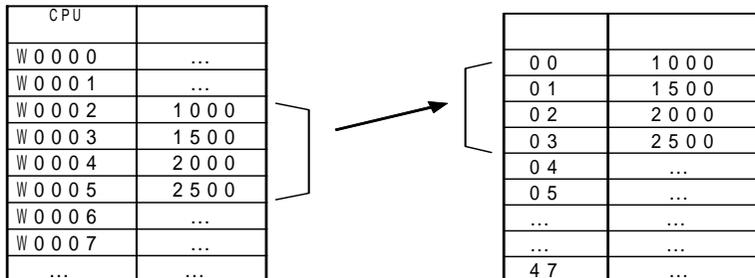
가 , PLC CPU
 SCU , DeviceNet ,
 2. WRITE PLC CPU
 () ()
 3. NN1= (0)
 NR2= (/)
 NR3=
 NR5= PLC CPU (/)
 4. WRITE , Root ,

POWER	CPU	IN 16 R0	IN 32 R1,2 1	A/O 4Ch R3	OUT 16 R4	OUT 32 R5,6 4	→
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CPU W2 W5 4

PLC CPU



RMWR	7	<div style="border: 1px solid black; padding: 2px; display: inline-block;"> RMWR NT=NN1:NN2 TO=NN3:NR4 FR=NR5:NR6 </div>	CPU / (NR6) (NR5) Loop(NN1) Station(NN2) Slot (NN3) (NR4)	1)

1)

SPC-10	SPC100 24S/120S	SPC300	A200	N70 plus 9215A, CPU70p1, V2	NX70 plus 9216A, CPU70p2, V2	N/NX700plus 7215A, CPU700p	NX700plus CPU700p/V2
x	x	x	x	x			

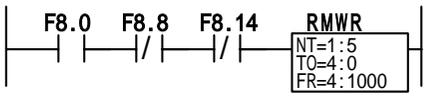
) : NN= , NR= , RR=

1. PLC CPU
2. RMWR
3. NN1= (1, 2 3 = Master 가 1 1)
 NN2= Slave Station
 NN3=
 NR4= (/)
 NR5=
 RR6= 가 CPU (PLC CPU),
4. RMWR SCAN 1Scan
5. RMWR , Root

Master 가 Slave ID 5 4

POWER	CPU	REM	IN	IN	OUT	OUT
		Master	32	32	16	32
		0	R0,1	R2,3	R4	R5,6
			1	2	3	4

POWER	REM	IN	IN	OUT	OUT	A/O
	Slave	32	32	16	32	4Ch
	#5	R0,1	R2,3	R4	R5,6	R7
		0	1	2	3	4



< PLC CPU

>

<

>

1000

0 0	1 0 0 0
0 1	1 0 0 0
0 2	1 0 0 0
0 3	1 0 0 0
0 4	...
0 5	...
...	...
...	...
4 7	...

(RECV)

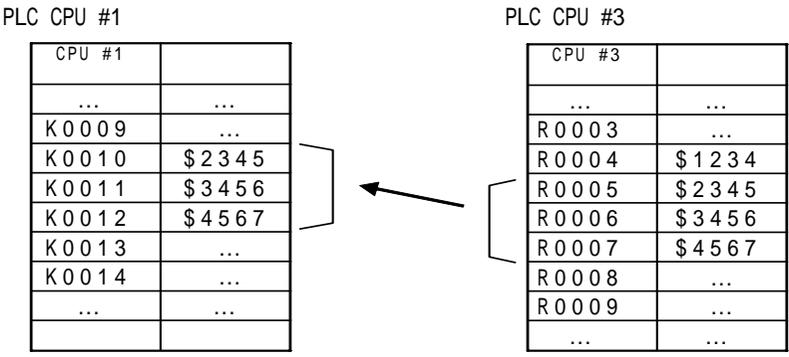
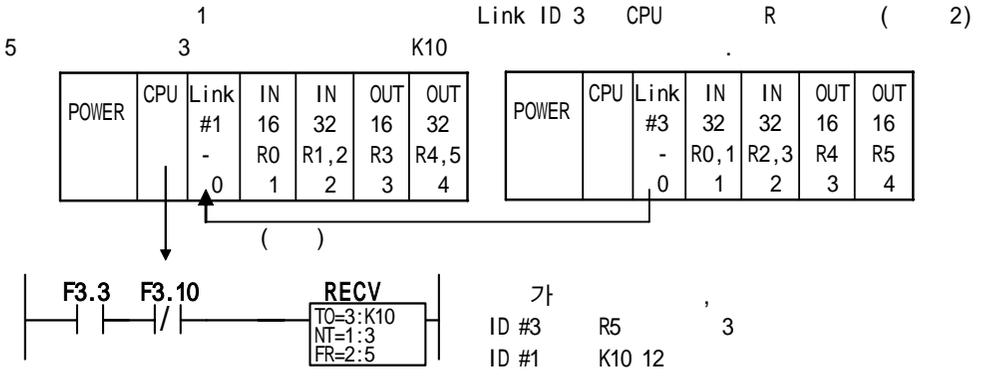
RECV	7	<div style="border: 1px solid black; padding: 2px;"> TO=NR1:RR2 NT=NN3:NN4 FR=NN5:NR6 </div>	(NN5)	(NN3) Station(NN4) (NR6)	(NR1)	1)
------	---	--	-------	-----------------------------	-------	----

1)

SPC-10	SPC100 24S/120S	SPC300	A200	N70 plus 9215A, CPU70p1, V2	NX70 plus 9216A, CPU70p2, V2	N/NX700plus 7215A, CPU700p	NX700plus CPU700p/V2
×	×	×	×	×			

) : NN= , NR= , RR=

1. RECV ID 가 CPU
2. NR1= ()
 RR2= () (PLC CPU),
 NN3= Loop (1, 2 3 = 가 CPU 1)
 NN4= Station (ID)
 NN5= (0= L , 1=M, 2=R, 3=K, 4=SV, 5=PV,6=W,7=F)
 NR6= (/) - CPU
3. RECV SCAN 1Scan
4. RECV , Root



(SEND)

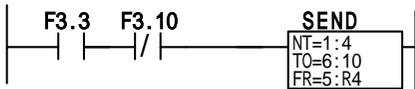
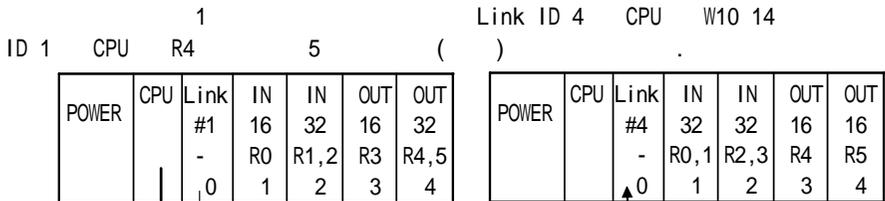
SEND	7	SEND NT=NN1:NN2 TO=NN3:NR4 FR=NN5:NR6	/ (NR6) (NR5) (NN1) Station(NN2) (NN3) (NR4)	1)
------	---	--	--	----

1)

SPC-10	SPC100 24S/120S	SPC300	A200	N70 plus 9215A,CPU70p1,V2	NX70 plus 9216A,CPU70p2,V2	N/NX700plus 7215A,CPU700p	NX700plus CPU700p/V2
x	x	x	x	x			

) : NN= , NR= , RR=

- SEND CPU ID 가 CPU
- NN1= Loop (1, 2 3 = 가 CPU 1 1)
 NN2= Station (ID)
 NN3= (0= L , 1=M, 2=R, 3=K, 4=SV, 5=PV,6=W,7=F)
 NR4= (/) - CPU.
 NR5=
 NR6=
- SEND SCAN 1Scan
- SEND , Root



= 1, Station (ID) = 4
 W=6, = 10
 = 5, = R4

PLC CPU #1

CPU #1	
...	...
R0003	...
R0004	\$ 1234
R0005	\$ 2345
R0006	\$ 3456
R0007	\$ 4567
R0008	\$ 5678
R0009	...
...	...

PLC CPU #4

CPU #4	
...	...
W0009	...
W0010	\$ 1234
W0011	\$ 2345
W0012	\$ 3456
W0013	\$ 4567
W0014	\$ 5678
...	...



(RECVB)

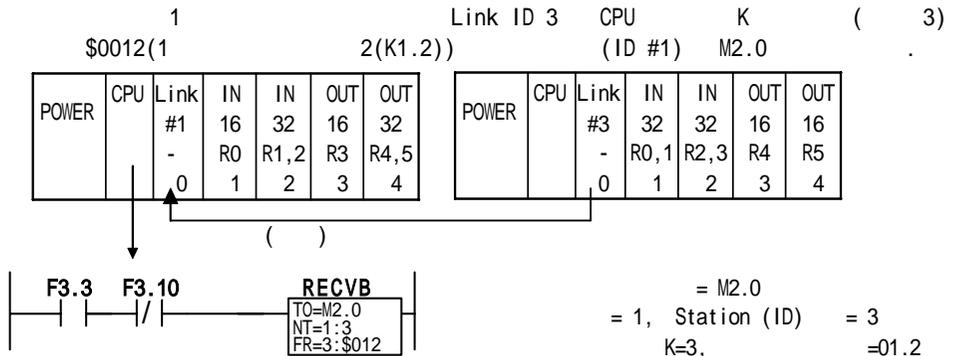
RECVB	6	RECVB TO=BR1 NT=NN3:NN4 FR=NN5:NR6	(NN3) Station(NN4) (NN5) (NR6) (BR1)	1)
-------	---	--	--	----

1)

SPC-10	SPC100 24S/120S	SPC300	A200	N70 plus 9215A,CPU70p1,V2	NX70 plus 9216A,CPU70p2,V2	N/NX700plus 7215A,CPU700p	NX700plus CPU700p/V2
x	x	x	x	x			

) : BR= , NN= , NR= , RR=

- RECVB ID 가 CPU
- BR1= ()
 NN3= Loop (1, 2 3 = 가 CPU 1)
 NN4= Station (ID)
 NN5= (0= L , 1=M, 2=R, 3=K, 4=SV, 5=PV,6=W,7=F)
 NR6= () (/) - CPU, 16
) 3) 5 : NR6=\$0035
- RECVB SCAN 1Scan
- RECVB , Root



PLC CPU #1	PLC CPU #3
CPU #1 ()	CPU #3 ()
M 0 0 0 0 ...	K 0 0 0 0 ...
M 0 0 0 1 ...	K 0 0 0 1 0 0 0 0 1 0 0 0 1 0 0
M 0 0 0 2 0 0 0 0 0 0 0 0 0 0 0 0 0 1	K 0 0 0 2 0 0 0 0 0 0 0 0 0 0 0 0 0 0
M 0 0 0 3 0 0 0 0 0 0 0 0 0 0 0 0 0 0	K 0 0 0 3 0 0 0 0 0 0 0 0 0 0 0 0 0 0
M 0 0 0 4 0 0 0 0 0 0 0 0 0 0 0 0 0 0	K 0 0 0 4 0 0 0 0 0 0 0 0 0 0 0 0 0 0
M 0 0 0 5 ...	K 0 0 0 5 ...
M 0 0 0 6 ...	K 0 0 0 6 ...
...	...

(SENDB)

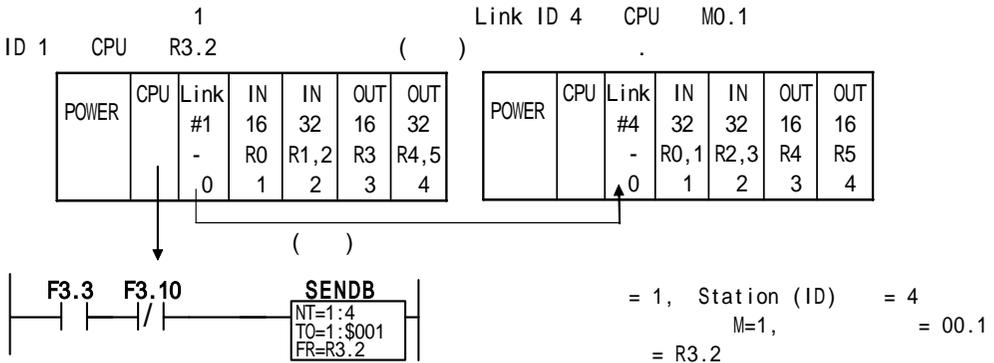
SENDB	6	SENDB NT=NN1:NN2 TO=NN3:NR4 FR=NB5	/ (NB5) (NN1) Station(NN2) (NN3) (NR4)	1)
-------	---	---	--	----

1)

SPC-10	SPC100 24S/120S	SPC300	A200	N70 plus 9215A, CPU70p1, V2	NX70 plus 9216A, CPU70p2, V2	N/NX700plus 7215A, CPU700p	NX700plus CPU700p/V2
x	x	x	x	x			

) : BR= , NN= , NR= , RR=

- SENDB CPU ID 가
CPU
- NN1= Loop (1, 2 3 = 가 CPU 1 1)
NN2= Station (ID)
NN3= (0= L , 1=M, 2=R, 3=K, 4=SV, 5=PV,6=W,7=F)
NR4= (/) - CPU, 16
) 3 5 : NR6=\$0035
NB5=
- SENDB SCAN 1Scan
- SENDB , Root



PLC CPU #1

CPU #1	()
R0000	...
R0001	...
R0002	00000000 10000001
R0003	00000000 01000100
R0004	00000000 00000000
R0005	...
R0006	...
...	...

PLC CPU #4

CPU #3	()
M0000	00000000 00000100
M0001	00001000 01000100
M0002	00000000 00000000
M0003	00000000 00000000
M0004	00000000 00000000
M0005	...
M0006	...
...	...

7

-1.	160
7-2	165

7-1. NX70 PLC

CPU (plus-)

WinGPC SW

CPU	NX70-CPU70p1	<ul style="list-style-type: none"> • 9K Words (), 0.2μs/ STEP, RS232C/485 1 , • FLASH ROM • 2K Data Register 	
	NX70-CPU70p2	<ul style="list-style-type: none"> • 20K Words (), 0.2μs/ STEP, RS232C/485 2 , • , FLASH ROM , PID , • 4K Data Register 	

CPU

CPU	CPL5530	2m	NX70, NX700 CPU
	CPL5531	5m	

	NX70-BASE02	2	NX70 PLC
	NX70-BASE03	3	
	NX70-BASE05	5	
	NX70-BASE06	6	
	NX70-BASE08	8	
	NX70-BASE10	10	
	NX70-BASE12	12	

	NX70-POWER1	AC 110/ 220V Free Voltage, 5V 3.5A, 24V 0.3A	AC Type
	NX70-POWER2	AC 110/ 220V Free Voltage, 5V 4.5A	
	NX70-PWRDC	DC 24V Input, 5V 4.5A	DC Type

		()			
	16	NX70-X16D	CPL93023	DC 12~24V, 20, 8 / COM, (+, -)	
		NX70-X16D1	CPL93033	DC 24V, 20, 8 / COM, (+, -)	
		NX70-X16A110	CPL93043	AC 100~120V, 20, 8 / COM	
		NX70-X16A220	CPL93053	AC 200~240V, 20, 8 / COM	
	32	NX70-X32D	CPL93024	DC 12~24V, 20 x 2, 8 / COM, (+, -)	
		NX70-X32D1	CPL93034	DC 24V, 20 x 2, 8 / COM, (+, -)	
	8	NX70-Y8R	CPL93202	RELAY, 20, 250V 3A, (4 / COM x 1, 1 / COM x 4)	
		16	NX70-Y16R	CPL93103	
	NX70-Y16RV		CPL93203	RELAY, 20, 250V 1A, 8 / COM,	
	NX70-Y16T		CPL93483	TR (NPN), 20, 12~24V 0.6A, 8 / COM	
	NX70-Y16SSR		CPL93703	SSR, 20, 100~220V, 0.5A, 8 / COM	
	32	NX70-Y32T	CPL93484	TR (NPN), 20 x 2, 12~24V 0.4A, 16 / COM(-)	
		NX70-Y32P	CPL93584	TR (PNP), 20 x 2, 12~24V 0.4A, 16 / COM(+)	
	16	NX70-XY16	CPL93088	<ul style="list-style-type: none"> DC12~24V, 8, 8 / COM, (+, -), RELAY, 8, 250V 1A, 8 / COM, 20 	
32		NX70-XY32	<ul style="list-style-type: none"> DC12~24V 16, 16 / COM (+, -), 20 TR (NPN) 16, DC12~24V 0.4A, 16 / COM 	16, 16 ()	
		NX70-DUMMY	CPL93000	Dummy()	

(A/D)	NX70-AI8C	8CH Current Input, 16Bit A/D Converter, ±20mA, 0 20mA, 4 20mA (0.519uA 2.0uA) 1.25ms/Ch		
	NX70-AI8V	8CH Voltage Input, 16Bit A/D Converter, ±5V, ±10V, 0 5V, 0 10V (0.153mV 1.0mV), 1.25ms/Ch		
	NX70-AI4C	4CH Current Input, 16Bit A/D Converter, ±20mA, 0 20mA, 4 20mA (0.519uA 2.0uA) 1.25ms/Ch		
	NX70-AI4V	4CH Voltage Input, 16Bit A/D Converter, ±5V, ±10V, 0 5V, 0 10V (0.153mV 1.0mV), 1.25ms/Ch		
(D/A)	NX70-AO4V	4CH Voltage Output, 14bit D/A Converter, ±10V, ±5V, 0 10V, 0 5V (0.305mV 1.0mV), 2.5ms/ Ch	20 (Ver 2.0)	
	NX70-AO4C	4CH Current Output, 14bit D/A Converter, 0 20mA, 4 20mA (0.037uA 2.0uA) 4uA, 2.5ms/ Ch		
	NX70-AO2V	2CH Voltage Output, 14bit D/A Converter, ±10V, ±5V, 0 10V, 0 5V (0.305mV 1.0mV), 2.5ms/ Ch		
	NX70-AO2C	2CH Current Output, 14bit D/A Converter, 0 20mA, 4 20mA (0.037uA 2.0uA) 4uA, 2.5ms/ Ch		
(RTD)	NX70-RTD4	4CH 3-Wire, Pt100, Pt200, Pt500, Pt1000, JPt100, JPt200, JPt500, JPt1000, NI100, NI120, CU50, 300, 600, 2000 0.1, 0.1, 10m, 20m, 60ms/Ch		
(ThermoCouple)	NX70-TC4	4CH Type : B/ R/ S/ N/ K/ E/ J/ T(가) ±30mV (1uV /Bit), ±60mV (2uV /Bit) 0.1 / 0.1 / 1uV/ 2uV, 60ms/Ch		

(CCU+)	NX70-CCU+	NX Protocol RS232C/ RS485 x 1 (1 가) (CPU Version 2.0)	ROM V2.0
(SCU)	NX70-SCU	RS232C/ RS485 x 2 () • RS232C/ RS485 Master 가 (Binary/ ASCII)	

/

	NX70-HSC1	1CH (100Kcps) 24Bit Up/Down	
	NX70-HSC2	2CH (100Kcps) 24Bit Up/Down	
	NX70-HSC4	4CH (200Kcps), 8 , 8 32Bit Up/Down	
	NX70-PULSE4	4Ch, 4Ch , 8 , 8 100KHz, CW/CCW, HSC 200Kcps, 32Bit, PWM 30KHz, Duty 0~100%(1%)	CPU70p2 ROM V2.0

PLC (CPU)

W-Link MW-Link	NX70-WLINK NX70-MWLINK	W-Link (W-) • • CCU 3 • : PLC (16 , L : 1,024 , W : 128) , , (16 / 1) , • : 0.5Mbps, : 800m, 2Line 가 : NX70-CPU70p2	Twisted - Pair

REMOTE I/O

REMOTE I/O SLAVE	NX70-SLAVE	CPU : N700 PLC (CPL7740) NX700 PLC (NX-MASTER)	
I/O Link (SLAVE)	NX-IOLINK	• (Stand Alone Type) • Slave + 1 • NX70 (1)	NX700, N700 Master Slave

Handy-Loader	PGM-500	<ul style="list-style-type: none"> · , , , BACK LIGHT · BACK-UP 가 · LCD · RS-232C/ 485 	<ul style="list-style-type: none"> · SPC10 PLC · N70plus (CPL9215A) (CPL9216A) 	
SW	WinGPC S/W (Window)	<ul style="list-style-type: none"> · PLC · FILE / / ON-LINE / · PLC · / / I/O MAP / · TIME CHART · S/W · WinGPC(Window) Ver 3.xx 	<ul style="list-style-type: none"> · N700plus (CPL7215A) · NX7 PLC · NX70 PLC (NX70-CPU70p1) (NX70-CPU70p2) · NX700 PLC (NX-CPU700p) 	Windows 98

CPU

CPU	NX-CBLCPU2 (CPL5530)	2m	WinFPST S/W()	
	NX-CBLCPU5 (CPL5531)	5m		

I/O ASSY	NX70 I/O ()	CPL8800	DC IN 32 / 64	: 20 1.5m
		CPL8810	TR OUT 32 / 64	
		CPL8820	RELAY OUT 32	
I/O ASSY	NX70 I/O ()	CPL8880	20 (PIN 20 ,)	NX70, N70, N700 I/O



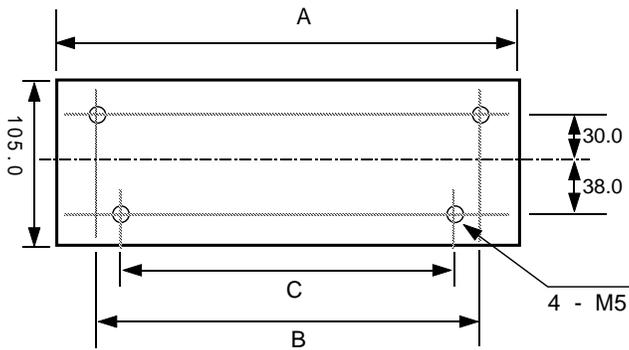
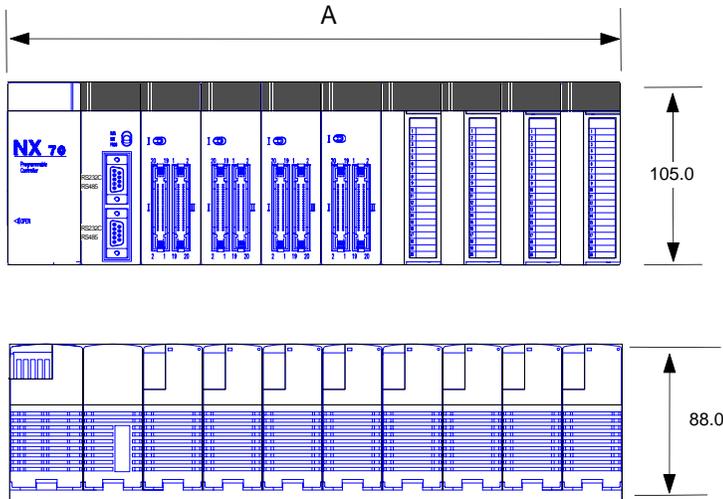
PLC N- N-plus 가 . (S/W가)
 , N70 , N700 , NX70 , NX700 CPU (POWER, I/O, , ...)

		CPU	
N-plus	SPC10	SPC-28ADR, SPC-28ADT, SPC-10ADR, SPC-10ADT, SPC-10DR.....	WinGPC S/W
	NX7	NX7-28ADR, NX7-28ADT, NX7-48ADR, NX7-48ADT.....	
	N70	CPL9215A, CPL9216A	
	N700	CPL7215A	
	NX70	NX70-CPU70p1, NX70-CPU70p2	
	NX700	NX-CPU700p	
N-	N7	CPL02323, CPL02343C, CPL02543C.....	WinFPST S/W
	N70	CPL9210A, CPL9211A	
	N700	CPL7210A, CPL7211A, CPL6210A, CPL6210B, CPL6215A	
	NX70	NX70-CPU70, NX70-CPU750	
	NX700	NX-CPU750A, NX-CPU750B, NX-CPU750C, NX-CPU750D, NX-CPU700	

7-2. NX70 PLC

1) (mm)

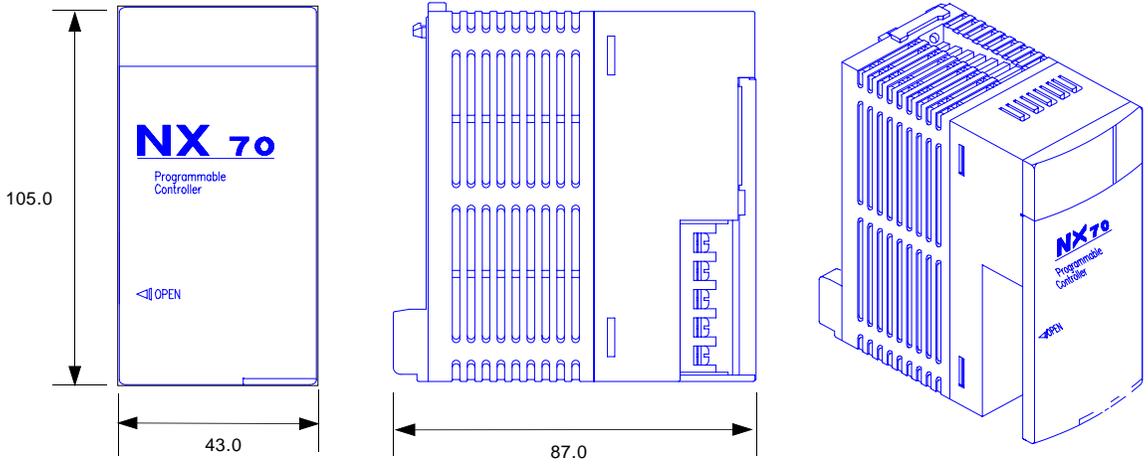
(: mm)



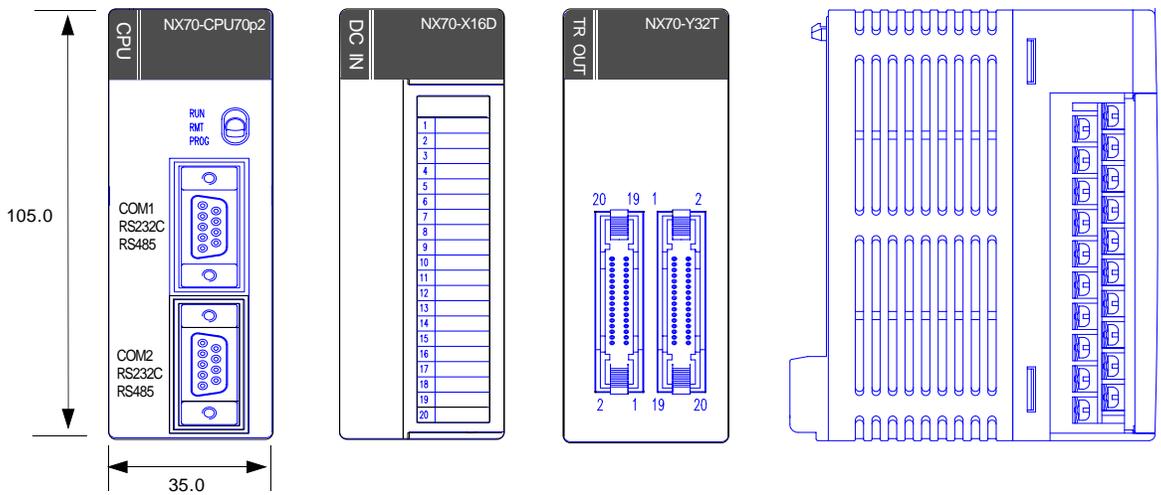
(mm)

		(A)	(B)	(C)
2	NX70-BASE02	157.2	128.6	114.6
3	NX70-BASE03	192.4	163.8	149.8
5	NX70-BASE05	262.8	234.2	220.2
6	NX70-BASE06	298.0	269.4	255.4
8	NX70-BASE08	368.4	339.8	325.8
10	NX70-BASE10	438.8	410.2	396.2
12	NX70-BASE12	508.6	480.6	466.6

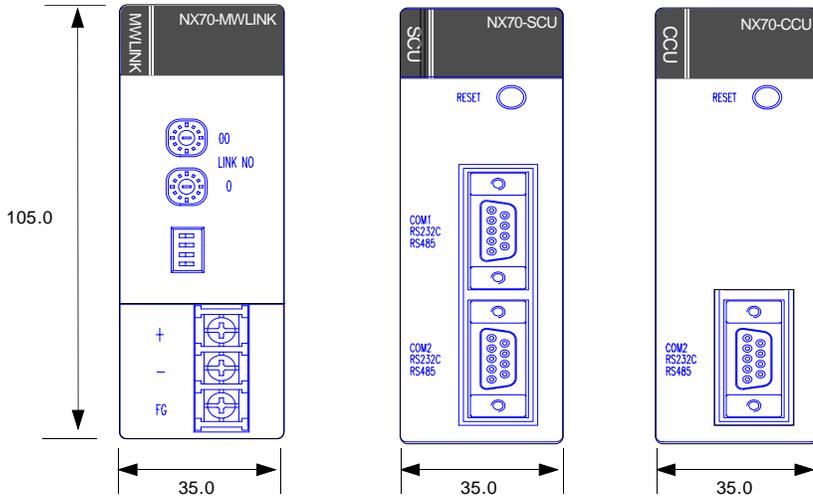
2) (mm)



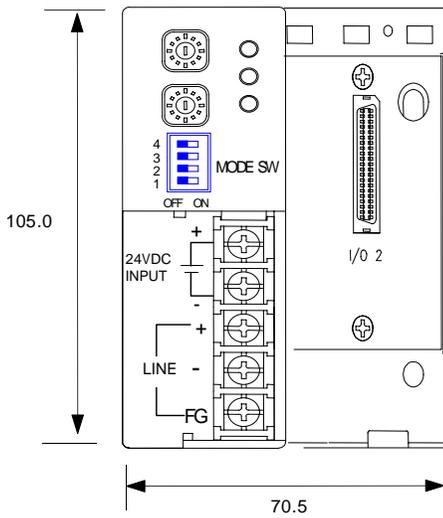
3) CPU, I/O (mm)



4) (mm)



5) NX-IOLINK (mm)





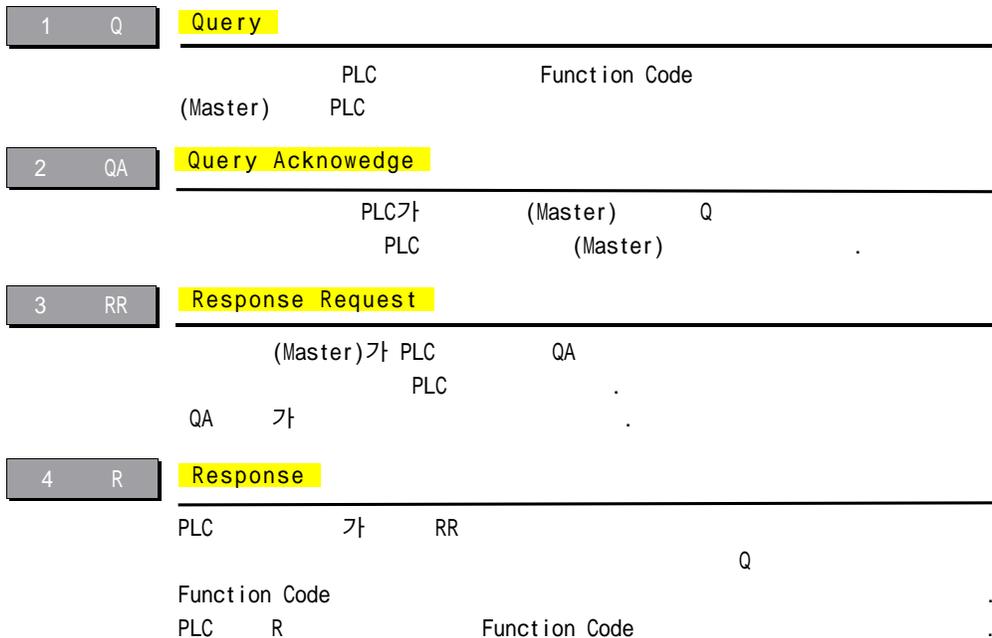
1-1. NX-plus CPU	169
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1-1. NX-plus CPU

	RS-232C/RS-485
	4800/ 9600/ 19200/38400 bps
	2 (Half DUPLEX Asynchronous)
	Polling
	Binary (HEX)
	: 8bit
	STOP BIT : 1bit
	Parity : (NO Parity)
	CRC-16
	Byte
	Twisted Pair Cable

1-2. NX-plus CPU (Protocol)

N plus CPU Protocol 2가
 Master(PC) Q(Query), QA(Query Acknowledge), RR(Response Request),
 R(Response) 4 , Master Q R
 2



CPU

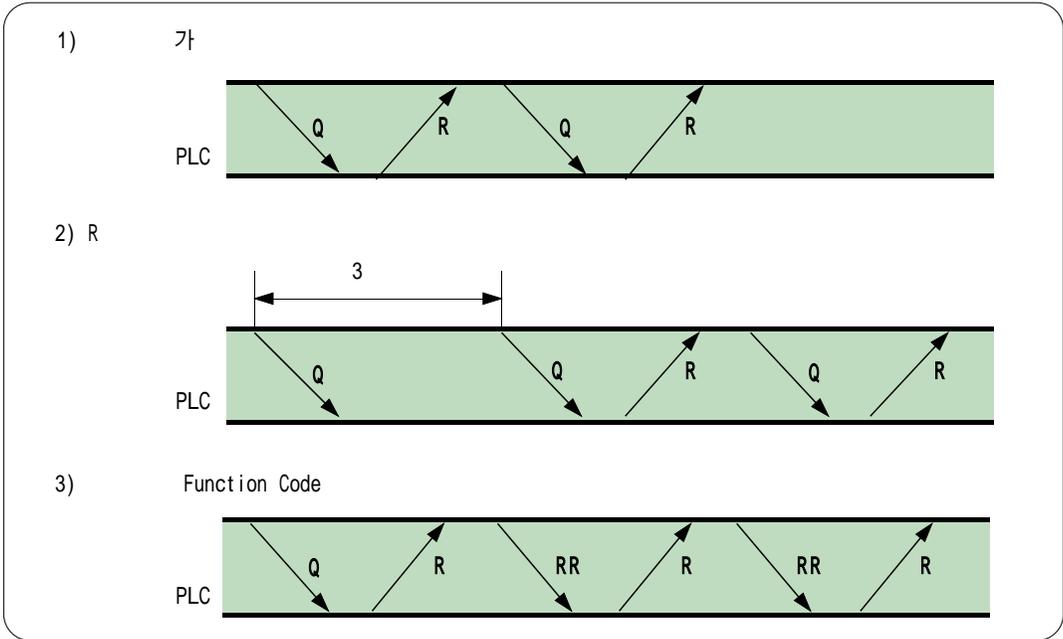
PLC Q RR
 , CRC ,
 PLC가 가
 Q RR 가 3
 Q RR

CPU (CPU ID)

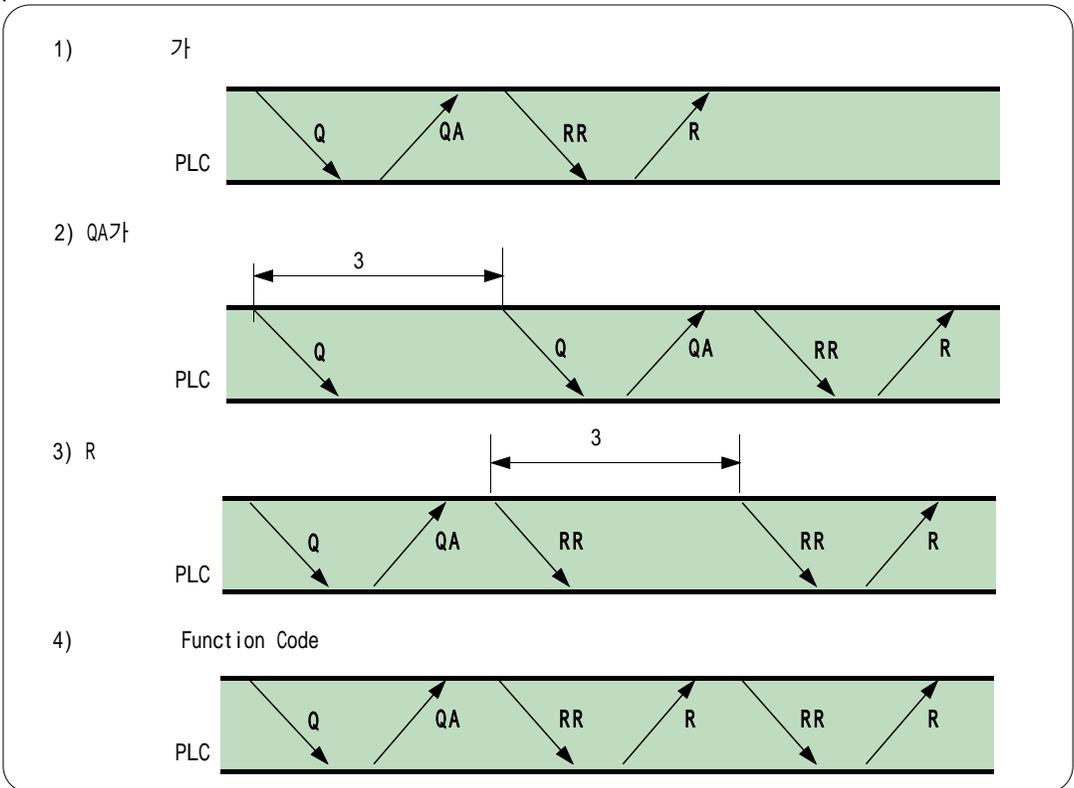
NX-plus PLC CPU 가 CPU가 RS-485
 가
 N plus Series 0 191 가
 CPU
 CPU 0, 1 255
 ID
 , 255 CPU 가 , ID
 CPU CPU , N-plus
 Series CPU ID CPU 255 ID
 CPU ID 가 CPU
 S/W(GPC5,WingPC)
 , Link Link ID

N plus CPU 2 4 , 2 4 Q(Query)
 Frame (Function Code) 2
 4 Query 2 RR
 4
 2
 2 N plus CPU , SPC
 Q R
 , 2 : Q(1) R(2)
 : Q(1) R(2) RR(1) R(2) ..
 , CPU , Q 가 가
 4
 4 N plus CPU SPC Protocol , Q QA RR R 4
 RR 2
 , 4 : Q(1) QA(2) RR(3) R(4)
 : Q(1) QA(2) RR(3) R(4) RR(1) R(2)..

(1) 2



(2) 4



(3) (Query)

(Function Code)

1 PLC (Q) , R
 \$80(Hex) , PLC
 FC() \$23 Q , R \$A3 (\$80) FC
 2 4
 Response 가 \$20(Hex) 가
 PLC가 R Q Function
 Code

) \$ Hex(16)

	(Q) Function Code		Response(R) Function Code		
	2	4	2	4	
	\$21	\$01	\$A1	\$81	
	\$22	\$02	\$A2	\$82	"
	\$23	\$03	\$A3	\$83	"
	\$24	\$04	\$A4	\$84	"
/	\$25	\$05	\$A5	\$85	"
/	\$26	\$06	\$A6	\$86	"
	\$27	\$07	\$A7	\$87	
	\$28	\$08	\$A8	\$88	
	\$29	\$09	\$A9	\$89	
	\$2A	\$0A	\$AA	\$8A	
	\$2B	\$0B	\$AB	\$8B	
	\$2C	\$0C	\$AC	\$8C	
	\$2D	\$0D	\$AD	\$8D	
	\$2E	\$0E	\$AE	\$8E	
	\$2F	\$0F	\$AF	\$8F	
/	\$20	\$10	\$A0	\$90	
NO SERVICE	\$00	\$00	\$00(Hex)	\$00(Hex)	

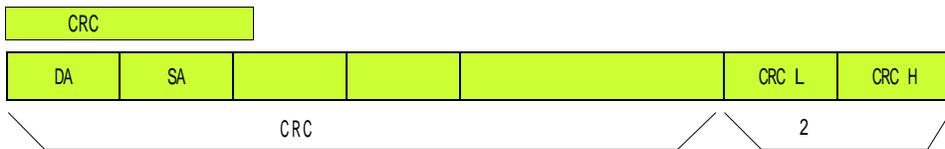
Query ?

(4) (CRC-16, Cycle Redundancy Checking :)

CPU CRC-16 (Cyclic Redundancy Checking,)
 2Byte
 CRC (Frame)
 (Check Sum Code) 2
 / 1 / CRC
 CRC

CRC-16

CRC-16 (DA)
 17 2 (1 1000 000 000 0101) 2Byte



C++ CRC-16 1

```

/*-----*/
// CRC-16 Routine with traditional method
// method 1. No need CRC table
/*-----*/
void CRC16_Test(int count)
{
  int i;

  Crc = 0xffff;
  for(i=0; i<count; i++)
  {
    CrcOld = Crc;
    Crc = Crc ^ (Data[i] & 0x00FF);
    for(int bit=0; bit<8; bit++)
    {
      if((Crc & 0x0001) == 0x0001)
        Crc = (Crc>>1) ^ 0xA001;
      else
        Crc = Crc>>1;
    }
    PRINT_CRC_JOBPROCESS(i, Data[i]);
  }
}

```

C++

CRC-16

2 (Table)

```

/*-----*/
// CRC-16 Routine with CrcTable
// method 2. Need CRC table
/*-----*/
void CRC16_TestFast(int count)
{
    int i;
    unsigned int Temp;

    Crc = 0xffff;
    for(i=0; i<count; i++)
    {
        CrcOld = Crc;
        Temp = Crc ^ Data[i];
        Crc = (Crc>>8) ^ Crc16Table[Temp&0x00ff];
        PRINT_CRC_JOBPROCESS(i, Data[i]);
    }
}

```

Table (CrcTest.h)

```

unsigned int Crc, CrcOld;

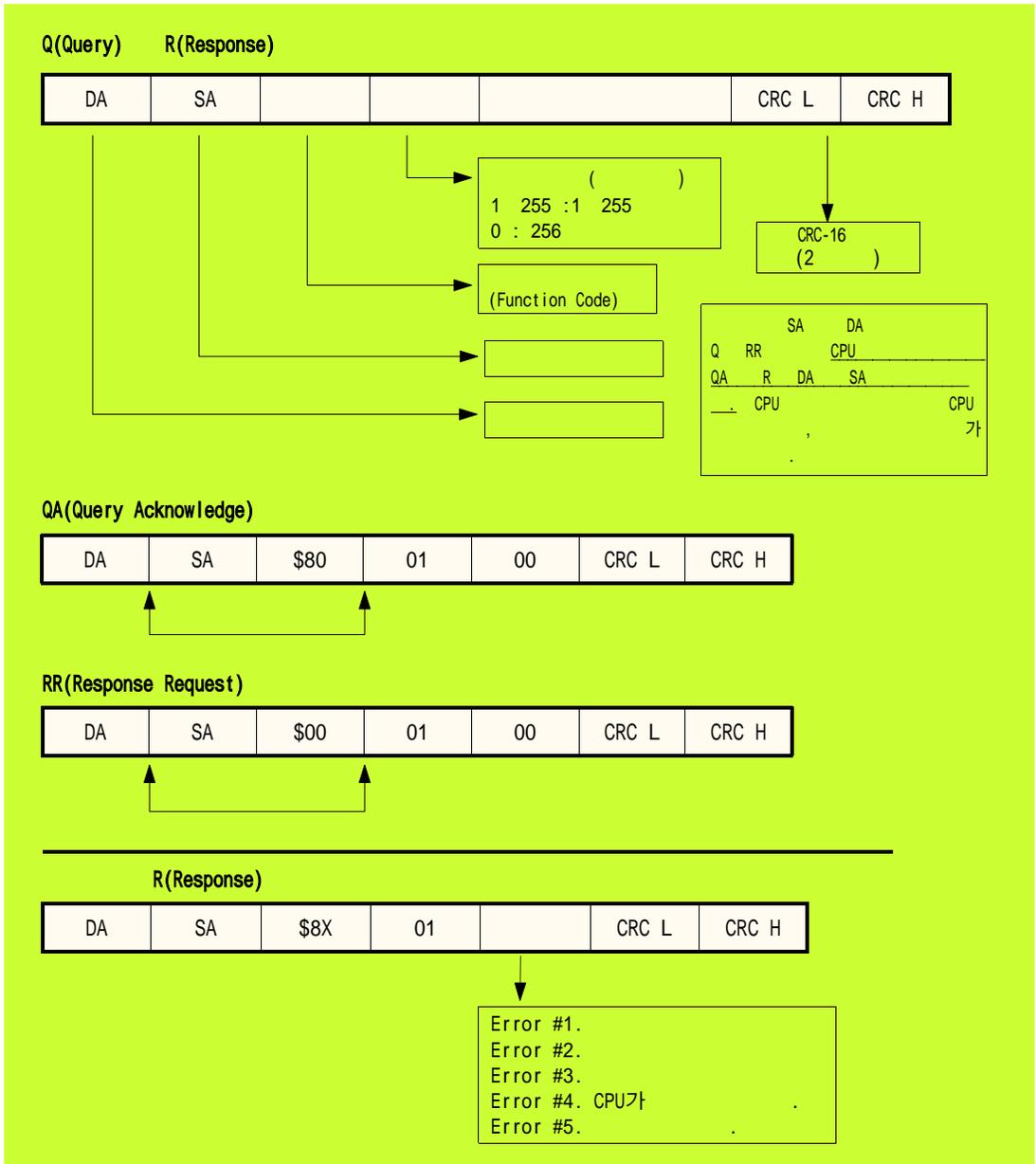
const unsigned int Crc16Table[256] =
{
    0x0000,0xc0c1,0xc181,0x0140,0xc301,0x03c0,0x0280,0xc241,
    0xc601,0x06c0,0x0780,0xc741,0x0500,0xc5c1,0xc481,0x0440,
    0xcc01,0x0cc0,0x0d80,0xcd41,0x0f00,0xcf c1,0xce81,0x0e40,
    0x0a00,0xcac1,0xcb81,0x0b40,0xc901,0x09c0,0x0880,0xc841,
    0xd801,0x18c0,0x1980,0xd941,0x1b00,0xdb c1,0xda81,0x1a40,
    0x1e00,0xdec1,0xdf81,0x1f40,0xdd01,0x1dc0,0x1c80,0xdc41,
    0x1400,0xd4c1,0xd581,0x1540,0xd701,0x17c0,0x1680,0xd641,
    0xd201,0x12c0,0x1380,0xd341,0x1100,0xd1c1,0xd081,0x1040,
    0xf001,0x30c0,0x3180,0xf141,0x3300,0xf3c1,0xf281,0x3240,
    0x3600,0xf6c1,0xf781,0x3740,0xf501,0x35c0,0x3480,0xf441,
    0x3c00,0xfcc1,0xfd81,0x3d40,0xff01,0x3fc0,0x3e80,0xfe41,
    0xfa01,0x3ac0,0x3b80,0xfb41,0x3900,0xf9c1,0xf881,0x3840,
    0x2800,0xe8c1,0xe981,0x2940,0xeb01,0x2bc0,0x2a80,0xea41,
    0xee01,0x2ec0,0x2f80,0xef41,0x2d00,0xedc1,0xec81,0x2c40,
    0xe401,0x24c0,0x2580,0xe541,0x2700,0xe7c1,0xe681,0x2640,
    0x2200,0xe2c1,0xe381,0x2340,0xe101,0x21c0,0x2080,0xe041,
    0xa001,0x60c0,0x6180,0xa141,0x6300,0xa3c1,0xa281,0x6240,
    0x6600,0xa6c1,0xa781,0x6740,0xa501,0xa5c0,0xa480,0xa441,
    0x6c00,0xacc1,0xad81,0x6d40,0xaf01,0x6fc0,0x6e80,0xae41,
    0xaa01,0x6ac0,0x6b80,0xab41,0x6900,0xa9c1,0xa881,0x6840,
    0x7800,0xb8c1,0xb981,0x7940,0xbb01,0x7bc0,0x7a80,0xba41,
    0xbe01,0x7ec0,0x7f80,0xbf41,0x7d00,0xbdc1,0xbc81,0x7c40,
    0xb401,0x74c0,0x7580,0xb541,0x7700,0xb7c1,0xb681,0x7640,
    0x7200,0xb2c1,0xb381,0x7340,0xb101,0x71c0,0x7080,0xb041,
    0x5000,0x90c1,0x9181,0x5140,0x9301,0x53c0,0x5280,0x9241,
    0x9601,0x56c0,0x5780,0x9741,0x5500,0x55c1,0x5481,0x5440,
    0x9c01,0x5cc0,0x5d80,0x9d41,0x5f00,0x5fc1,0x5e81,0x5e40,
    0x5a00,0x9ac1,0x9b81,0x5b40,0x9901,0x59c0,0x5880,0x9841,
    0x8801,0x48c0,0x4980,0x8941,0x4b00,0x4bc1,0x4a81,0x4a40,
    0x4e00,0x8ec1,0x8f81,0x4f40,0x8d01,0x4dc0,0x4c80,0x8c41,
    0x4400,0x84c1,0x8581,0x4540,0x8701,0x47c0,0x4680,0x8641,
    0x8201,0x42c0,0x4380,0x8341,0x4100,0x81c1,0x8081,0x4040
};

```

1-3

2,4

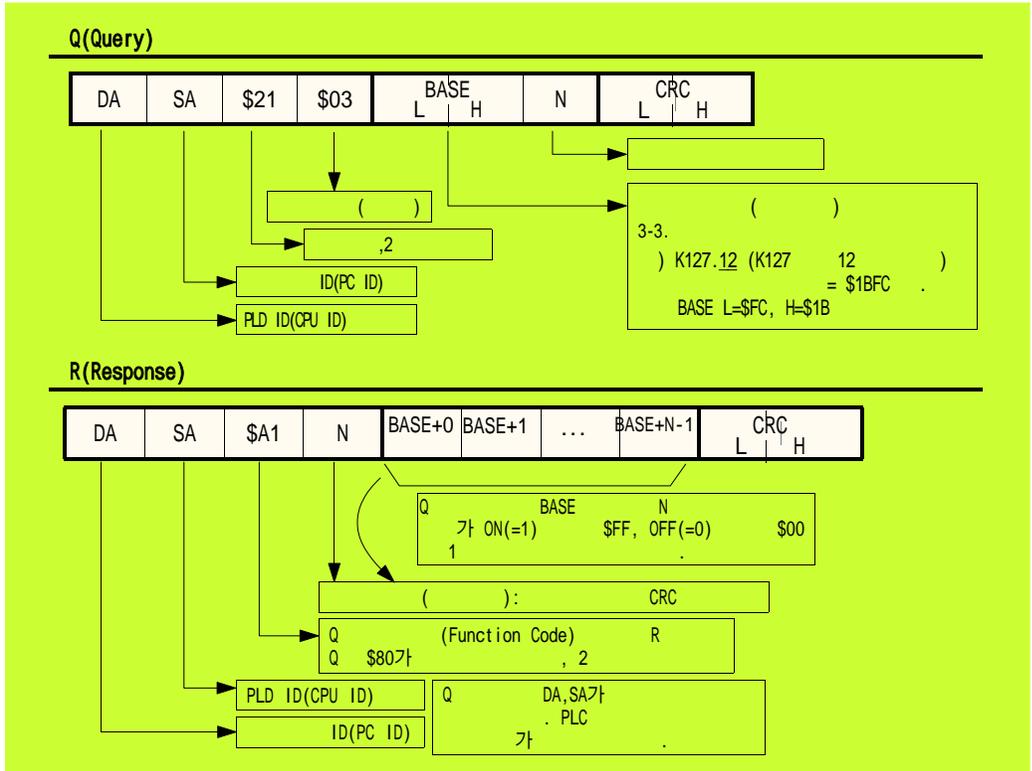
Query Response Frame



DA PLC ID , SA PC ID , DA가 PC ,
 PLC SA가 . PLC ID QA DA가 PC ,
 가 1 (2 Digits) ,
 , 00 FF ,
 256 .

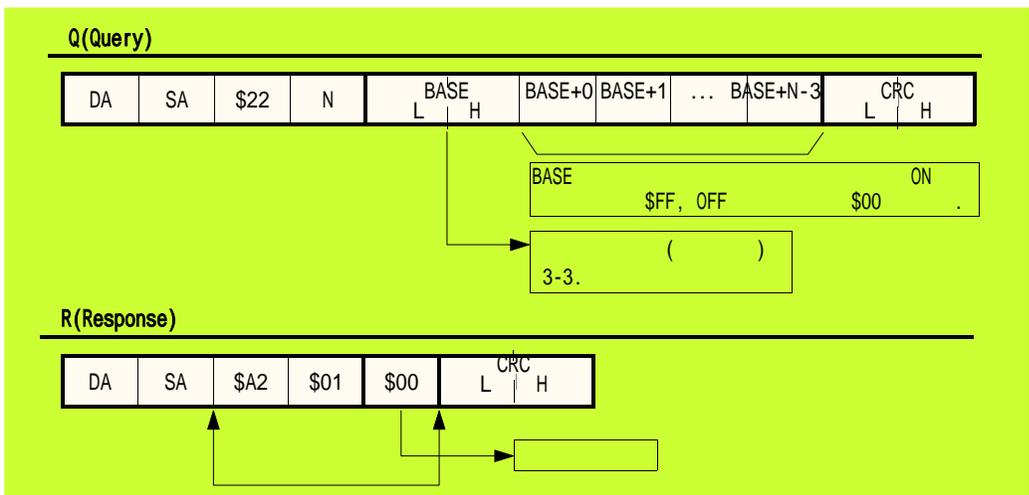
(1)

(R, L, M, K, F, TC)
 N
 (ON/ OFF)



(2)

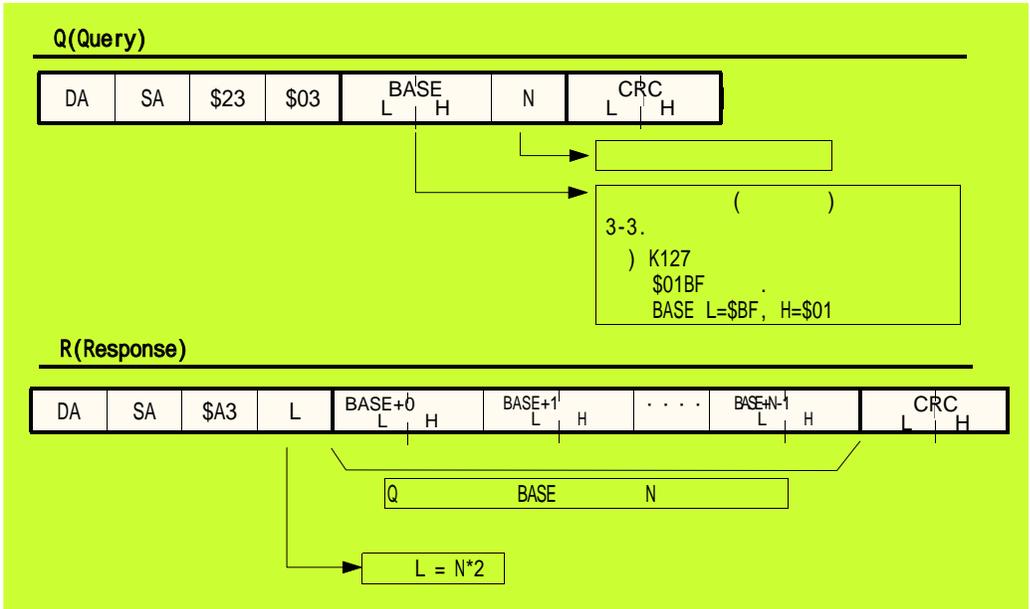
(R, L, M, K, F, TC) . ON/ OFF .



(3)

(R, L, M, K, F, W)

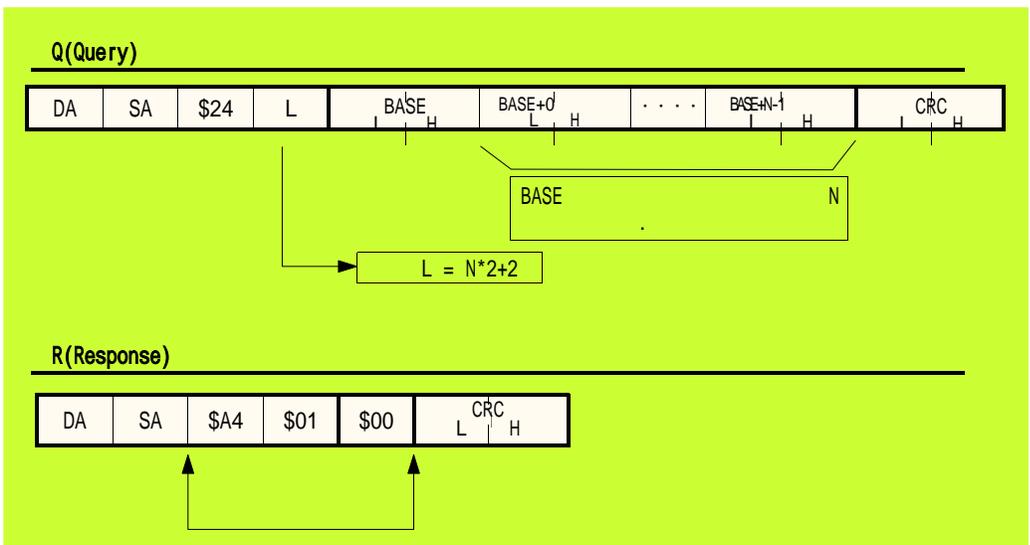
N



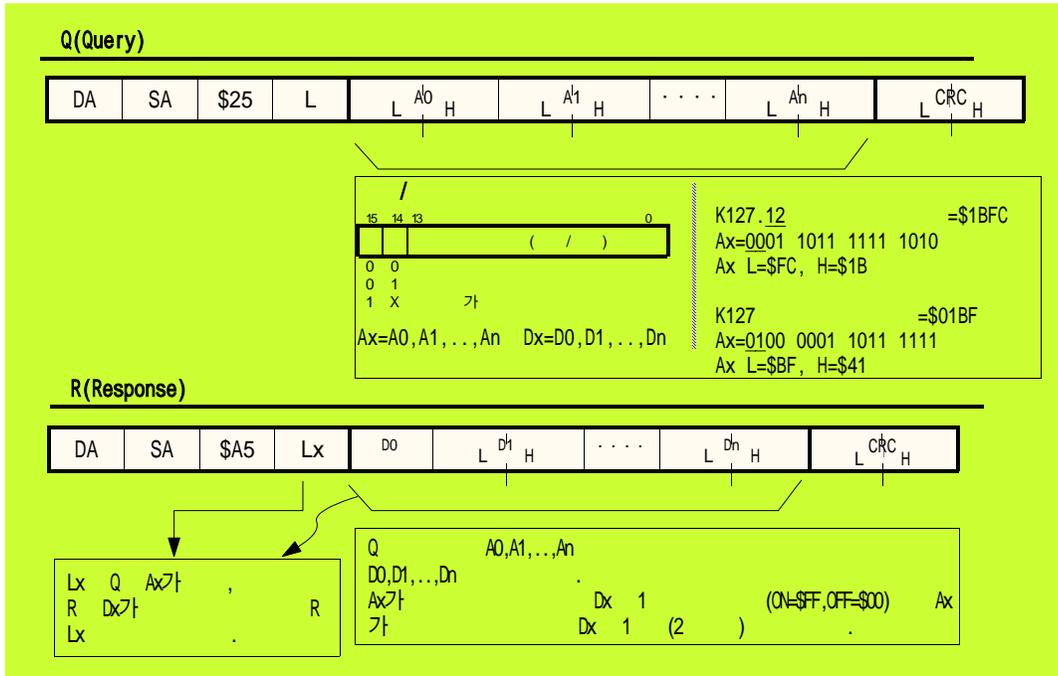
(4)

(R, L, M, K, F, W)

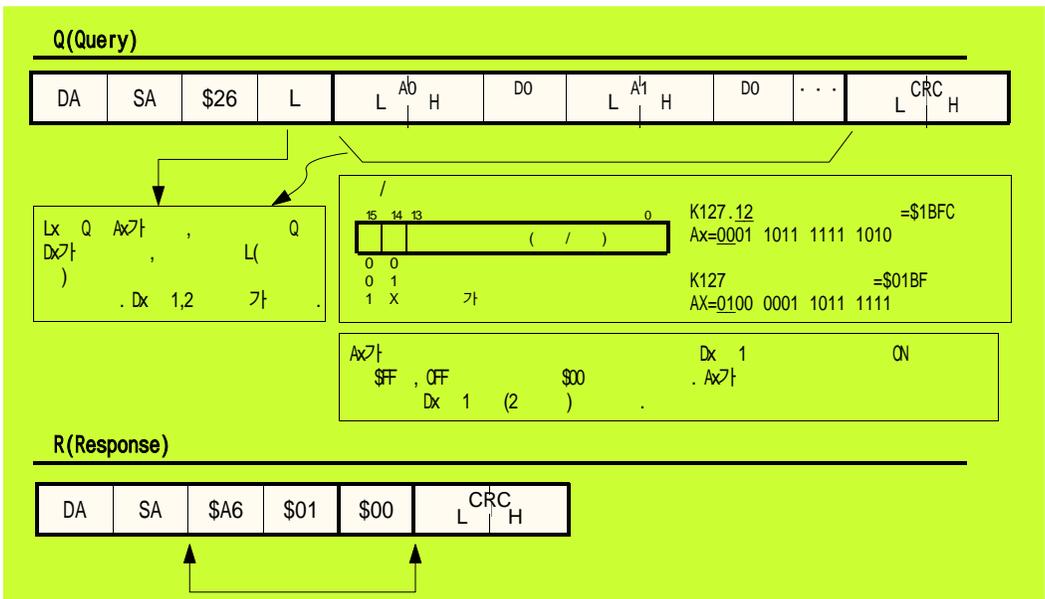
N



(5) /



(6) /



1-4.

C++ , Visual Basic

<pre> 1 // 2 // NpDemo.cpp : Defines the entry point for the console application. 3 // 7 // 8 #include "NpDemo.h" 9 #include <stdio.h> 10 #include <conio.h> 11 12 int main(int argc, char* argv[]) 13 { 14 printf("*****\n"); 16 printf("N-plus series PLC Communication Test Program *\n"); 18 printf("*****\n"); 19 20 //----Serial port initialization 21 printf("\nReady serial port init... "); 22 if(OnlineConnection(1)) 23 { 24 printf("Port open success!\n"); 25 } 26 else 27 { 28 CloseHandle(hPort); 29 printf("Port open error!\n"); 30 } 31 32 //----COMMUNICATION TEST 33 if(Test_Read()!=CS_END) 34 printf("Test_Read() failed!\n"); 35 DsplPacket(); 36 37 if(Test_Write()!=CS_END) 38 printf("Test_Write() failed!\n"); 39 DsplPacket(); 40 41 //----End process 42 if(hPort!=NULL) 43 { 44 if(CloseHandle(hPort)) 45 printf("\nPort close success!\n"); 46 else 47 printf("\nPort close failed!\n"); 48 } 49 50 return 0; 51 } 52 53 54 /*-----*/ 55 // N-plus READ_WORD TEST 56 // R0 : 1 word read 57 /*-----*/ 58 BYTE Test_Read() 59 { 60 int i=0; 61 62 Tx_Data.Data[i++] = 0xFF; 63 Tx_Data.Data[i++] = 0xE1; 64 Tx_Data.Data[i++] = FC_READ_WORD_2STEP; 65 Tx_Data.Data[i++] = 0x03; 66 Tx_Data.Data[i++] = 0x00; 67 Tx_Data.Data[i++] = 0x00; 68 Tx_Data.Data[i++] = 0x01; 69 CRC16(Tx_Data.Data, i++); 70 i--; 71 Tx_Data.Data[i++] = LOBYTE(Crc); 72 Tx_Data.Data[i++] = HIBYTE(Crc); 73 Tx_Data.Size = i; 74 75 RRA_LengthCalc(FC_READ_WORD_2STEP); 76 printf("\nREAD_WORD Function Code Test\n"); 77 return StateMachine(); 78 } 79 80 /*-----*/ 81 // N-plus READ_WORD TEST 82 // MO M4 : 5 word write 83 /*-----*/ </pre>	<p>COM1</p> <p>2</p> <p>(PLC) ID (PC) ID</p> <p>L. H</p> <p>CRC-16</p> <p>CRC L CRC H</p> <p>PLC</p>
---	--

<pre> 84 BYTE Test_Write() 85 { 86 int i=0, j, WordNumber=5; 87 88 Tx_Data.Data[i++] = 0xFF; 89 Tx_Data.Data[i++] = 0xE1; 90 Tx_Data.Data[i++] = FC_WRITE_WORD_2STEP; 91 Tx_Data.Data[i++] = WordNumber*2+2; 92 Tx_Data.Data[i++] = LOBYTE(0xc0); //0xc0 is M0 address 93 Tx_Data.Data[i++] = HIBYTE(0xc0); 94 95 for(j=0; j<WordNumber; j++) 96 { 97 Tx_Data.Data[i+j*2+0] = rand(); 98 Tx_Data.Data[i+j*2+1] = rand(); 99 } 100 i += WordNumber*2; 101 CRC16(Tx_Data.Data, i++); 102 i--; 103 Tx_Data.Data[i++] = LOBYTE(Crc); 104 Tx_Data.Data[i++] = HIBYTE(Crc); 105 Tx_Data.Size = i; 106 107 RRA_LengthCalc(FC_WRITE_WORD_2STEP); 108 printf("\nWRITE_WORD Function Code Test\n"); 109 return StateMachine(); 110 } 111 112 /*-----*/ 113 // Query Acknowledgement 114 /*-----*/ 115 bool Q_Process() 116 { 117 BOOL bRet; 118 DWORD dwWritten, dwErr; 119 COMSTAT CommState; 120 121 printf("Q : "); 122 ClearCommError(hPort, &dwErr, &CommState); 123 PurgeComm(hPort, MY_PURGE_EVENT); 124 bRet = WriteFile(hPort, 125 Tx_Data.Data, 126 Tx_Data.Size, 127 &dwWritten, 128 NULL); 129 130 if(!bRet) return false; 131 132 while(dwWritten!=Tx_Data.Size); 133 134 return true; 135 } 136 137 /*-----*/ 138 // Request Response Acknowledgement 139 /*-----*/ 140 bool RRA_Process() 141 { 142 BOOL bRet; 143 DWORD dwReaded=0, dwRdTotal=0, dwErr, StartTime; 144 COMSTAT CommState; 145 146 printf("RRA: "); 147 ClearCommError(hPort, &dwErr, &CommState); 148 PurgeComm(hPort, MY_PURGE_EVENT); 149 StartTime = GetTickCount(); 150 151 while((StartTime+1000)>GetTickCount()) 152 { 153 bRet = ReadFile(hPort, 154 (Rx_Data.Data+dwRdTotal), 155 Rx_Data.Size-dwRdTotal, 156 &dwReaded, 157 NULL); 158 159 if(!bRet) return false; 160 if(dwReaded!=0) 161 { 162 dwRdTotal+=dwReaded; 163 if(dwRdTotal==Rx_Data.Size) 164 return true; 165 } 166 } 167 168 return false; 169 } </pre>	<pre> 2 (PLC) ID (PC) ID L H L H CRC-16 CRC L CRC H PLC 가 가 WriteFile 가 dwWritten 가 PLC (Q) 1000ms PLC PC Rx_Data.Size= 1000ms </pre>
--	---

<pre> 171 /*-----*/ 172 // Win32 Serial Communication Port Open 173 // method 1. No need CRC table 174 /*-----*/ 175 bool OnlineConnection(int PortNumber) 176 { 177 char cpName[256]; 178 DCB CommDCB; 179 BOOL fRet; 180 181 hPort = NULL; 182 sprintf(cpName, "COM%d", PortNumber); 183 hPort = CreateFile(cpName, 184 GENERIC_READ GENERIC_WRITE, 185 0, 186 NULL, 187 OPEN_EXISTING, 188 FILE_ATTRIBUTE_NORMAL, 189 NULL); 190 191 if(hPort == INVALID_HANDLE_VALUE) return FALSE; 192 193 // set buffer size 194 fRet = SetupComm(hPort, MAX_FRAME_LEN, MAX_FRAME_LEN); 195 if(!fRet) return FALSE; 196 197 // device clear 198 PurgeComm(hPort, MY_PURGE_EVENT); 199 if(!fRet) return FALSE; 200 201 // Comm timeout set 202 COMMTIMEOUTS CommTimeOuts; 203 CommTimeOuts.ReadIntervalTimeout = 1; 204 CommTimeOuts.ReadTotalTimeoutMultiplier = 5; 205 CommTimeOuts.ReadTotalTimeoutConstant = 100; 206 CommTimeOuts.WriteTotalTimeoutMultiplier = 5; 207 CommTimeOuts.WriteTotalTimeoutConstant = 100; 208 fRet = SetCommTimeouts(hPort, &CommTimeOuts); 209 if(!fRet) return FALSE; 210 211 // DCB Block Set 212 CommDCB.DCBlength = sizeof(DCB) ; 213 fRet = GetCommState(hPort, &CommDCB) ; 214 if(!fRet) return FALSE; 215 CommDCB.BaudRate = CBR_9600; 216 CommDCB.Parity = NOPARITY; // Parity Setting 217 CommDCB.ByteSize = 8; // Data Size Setting 218 CommDCB.StopBits = ONESTOPBIT; // Stop Bit Setting 219 fRet = SetCommState(hPort, &CommDCB); 220 if(!fRet) return FALSE; 221 222 return TRUE; 223 } 224 225 226 /*-----*/ 227 // CRC-16 Routine with traditional method 228 // method 1. No need CRC table 229 /*-----*/ 230 void CRC16(BYTE *src, int count) 231 { 232 int i; 233 234 Crc = 0xffff; 235 for(i=0; i<count; i++) 236 { 237 CrcOld = Crc; 238 Crc = Crc ^ (*(src+i) & 0x00FF); 239 for(int bit=0; bit<8; bit++) 240 { 241 if((Crc & 0x0001) == 0x0001) 242 Crc = (Crc>>1) ^ 0xA001; 243 else 244 Crc = Crc>>1; 245 } 246 } 247 } 248 249 250 /*-----*/ 251 // Recieve length calculation 252 /*-----*/ 253 void RRA_LengthCalc(BYTE fc) 254 { 255 switch(fc) 256 { </pre>	<p>(95/98 NT/2000/XP API</p> <p>)</p> <p>NON_OVERRAPPED</p> <p>가</p> <p>API</p> <p>가 가 .</p> <p>: Plus : Plus : Plus</p> <p>CRC</p> <p>CRC-16</p> <p>Q PLC</p>
--	--

<pre> 257 case FC_READ_WORD_2STEP: 258 Rx_Data.Size = 6+Tx_Data.Data[6]*2; //6=4(header)+2(Crc) 259 break; 260 261 case FC_WRITE_WORD_2STEP: 262 Rx_Data.Size = 7; //7=4(header)+1(info)+2(Crc) 263 break; 264 265 default: 266 break; 267 } 268 } 269 } 270 271 /*-----*/ 272 // N-plus protocol establish 273 /*-----*/ 274 BYTE StateMachine() 275 { 276 bool bRet; 277 278 //----Q 279 bRet = Q_Process(); 280 if(!bRet) { printf("TX error!\n"); 281 return CS_ERR; 282 } 283 printf("%d bytes transmit success!\n", Tx_Data.Size); 284 285 //----RRA 286 bRet = RRA_Process(); 287 if(!bRet) { printf("%d bytes received error!\n", Rx_Data.Size); 288 return CS_ERR; 289 } 290 printf("%d bytes received success!\n", Rx_Data.Size); 291 292 //----packet verify 293 bRet = VerifyFrame(); 294 if(!bRet) { printf("Received packet informaton invalid!\n"); 295 return CS_ERR; 296 } 297 printf("Received packet informaton success!\n"); 298 299 return CS_END; 300 } 301 302 /*-----*/ 303 // Packet verify 304 /*-----*/ 305 bool VerifyFrame() 306 { 307 DWORD rxCrc; 308 309 310 rxCrc = (DWORD)(Rx_Data.Data[Rx_Data.Size-2] + 311 Rx_Data.Data[Rx_Data.Size-1]*0x100); 312 CRC16(Rx_Data.Data, Rx_Data.Size-2); 313 314 if((Tx_Data.Data[0]==Rx_Data.Data[1]) && 315 ((Tx_Data.Data[2]+0x80)==Rx_Data.Data[2]) && 316 (Crc==rxCrc)) 317 return true; 318 else 319 return false; 320 } 321 322 323 /*-----*/ 324 // Sent and Received packet data display 325 /*-----*/ 326 void DsplPacket() 327 { 328 int i; 329 330 printf("TxPacket:"); 331 for(i=0; i<Tx_Data.Size; i++) 332 printf("%02X ", Tx_Data.Data[i]); 333 printf("\nRxPacket:"); 334 335 for(i=0; i<Rx_Data.Size; i++) 336 printf("%02X ", Rx_Data.Data[i]); 337 printf("\n"); 338 } </pre>	<p>PLC 가</p> <p>PLC 가</p> <p>Q</p> <p>RRA</p> <p>2 CRC16 가</p> <p>CRC 가</p> <p>가 Q RRA</p> <p>(RS-485</p> <p>PLC</p> <p>PLC가</p> <p>ID</p> <p>)</p>
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(Header File)

<pre>1 // 2 // NpDemo.h : NpDemo source Header file 3 // 7 // 8 9 #include <windows.h> 10 11 //-----DEFINITION PART----- 12 const unsigned int MAX_FRAME_LEN = 262; 13 const unsigned int MY_PURGE_EVENT = PURGE_TXABORT PURGE_RXABORT 14 PURGE_TXCLEAR PURGE_RXCLEAR; 15 const BYTE CS_RDY = 0; 16 const BYTE CS_ING = 1; 17 const BYTE CS_END = 2; 18 const BYTE CS_ERR = 3; 19 20 const BYTE FC_READ_BIT_2STEP = 0x21; 21 const BYTE FC_WRITE_BIT_2STEP = 0x22; 22 const BYTE FC_READ_WORD_2STEP = 0x23; 23 const BYTE FC_WRITE_WORD_2STEP = 0x24; 24 const BYTE FC_READ_BITWORD_2STEP = 0x25; 25 const BYTE FC_WRITE_BITWORD_2STEP = 0x26; 26 27 struct Tx_RxData 28 { 29 public: 30 BYTE Data[MAX_FRAME_LEN]; 31 WORD Size; 32 }; 33 34 35 //-----VARIABLE PART----- 36 unsigned int Crc, CrcOld; 37 HANDLE hPort; 38 Tx_RxData Tx_Data, Rx_Data; 39 40 //-----FUNCTION PART----- 41 bool OnlineConnection(int PortNumber); 42 void CRC16(BYTE *src, int count); 43 bool Q_Process(); 44 bool RRA_Process(); 45 void RRA_LengthCalc(BYTE fc); 46 BYTE Statemachine(); 47 BYTE Test_Read(); 48 BYTE Test_Write(); 49 bool VerifyFrame(); 50 void DspIPacket();</pre>	<pre>262: N-plus . 2 2 2 2 2 2 / /</pre>
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1-5. 10 /BIN /HEX /BCD /Gray

10 (Decimal)	16 (Hecadecimal)	BIN 2 (Binary)	BCD 2 10 (4) (Binary Coded Decimal)	Gray
0	0000	00000000 00000000	0000 0000 0000 0000	0000 0000 0000 0000
1	0001	00000000 00000001	0000 0000 0000 0001	0000 0000 0000 0001
2	0002	00000000 00000010	0000 0000 0000 0010	0000 0000 0000 0011
3	0003	00000000 00000011	0000 0000 0000 0011	0000 0000 0000 0010
4	0004	00000000 00000100	0000 0000 0000 0100	0000 0000 0000 0110
5	0005	00000000 00000101	0000 0000 0000 0101	0000 0000 0000 0111
6	0006	00000000 00000110	0000 0000 0000 0110	0000 0000 0000 0101
7	0007	00000000 00000111	0000 0000 0000 0111	0000 0000 0000 0100
8	0008	00000000 00001000	0000 0000 0000 1000	0000 0000 0000 1100
9	0009	00000000 00001001	0000 0000 0000 1001	0000 0000 0000 1101
10	000A	00000000 00001010	0000 0000 0001 0000	0000 0000 0000 1111
11	000B	00000000 00001011	0000 0000 0001 0001	0000 0000 0000 1110
12	000C	00000000 00001100	0000 0000 0001 0010	0000 0000 0000 1010
13	000D	00000000 00001101	0000 0000 0001 0011	0000 0000 0000 1011
14	000E	00000000 00001110	0000 0000 0001 0100	0000 0000 0000 1001
15	000F	00000000 00001111	0000 0000 0001 0101	0000 0000 0000 1000
16	0010	00000000 00010000	0000 0000 0001 0110	0000 0000 0001 1000
17	0011	00000000 00010001	0000 0000 0001 0111	0000 0000 0001 1001
18	0012	00000000 00010010	0000 0000 0001 1000	0000 0000 0001 1011
19	0013	00000000 00010011	0000 0000 0001 1001	0000 0000 0001 1010
20	0014	00000000 00010100	0000 0000 0010 0000	0000 0000 0001 1110
21	0015	00000000 00010101	0000 0000 0010 0001	0000 0000 0001 1111
22	0016	00000000 00010110	0000 0000 0010 0010	0000 0000 0001 1101
23	0017	00000000 00010111	0000 0000 0010 0011	0000 0000 0001 1100
24	0018	00000000 00011000	0000 0000 0010 0100	0000 0000 0001 0100
25	0019	00000000 00011001	0000 0000 0010 0101	0000 0000 0001 0101
26	001A	00000000 00011010	0000 0000 0010 0110	0000 0000 0001 0111
27	001B	00000000 00011011	0000 0000 0010 0111	0000 0000 0001 0110
28	001C	00000000 00011100	0000 0000 0010 1000	0000 0000 0001 0010
29	001D	00000000 00011101	0000 0000 0010 1001	0000 0000 0001 0011
30	001E	00000000 00011110	0000 0000 0011 0000	0000 0000 0001 0001
31	001F	00000000 00011111	0000 0000 0011 0001	0000 0000 0001 0000
32	0020	00000000 00100000	0000 0000 0011 0010	0000 0000 0011 0000
63	003F	00000000 00111111	0000 0000 0110 0011	0000 0000 0010 0000
64	0040	00000000 01000000	0000 0000 0110 0011	0000 0000 0110 0000
255	00FF	00000000 11111111	0000 0010 0101 0101	0000 0000 0110 0000

1.6 ASCII

b8	b7	b6	b5	b4	b3	b2	b1	R	C	0	1	2	3	4	5	6	7
0	0	0	0	0	0	0	0	0	NUL	DEL	SPACE	0	@	P	`	p	
0	0	0	1					1	SOH	DC ₁	!	1	A	Q	a	q	
0	0	1	0					2	STX	DC ₂	"	2	B	R	b	r	
0	0	1	1					3	ETX	DC ₃	#	3	C	S	c	s	
0	1	0	0					4	EOT	DC ₄	\$	4	D	T	d	t	
0	1	0	1					5	ENQ	NAK	%	5	E	U	e	u	
0	1	1	0					6	ACK	SYN	&	6	F	V	f	v	
0	1	1	1					7	BEL	ETB	'	7	G	W	g	w	
1	0	0	0					8	BS	CAN	(8	H	X	h	x	
1	0	0	1					9	HT	EM)	9	I	Y	i	y	
1	0	1	0					A	LF	SUB	*	:	J	Z	j	z	
1	0	1	1					B	VT	ESC	+	;	K	[k	{	
1	1	0	0					C	FF	FS	'	<	L	\	l		
1	1	0	1					D	CR	GS	-	=	M]	m	}	
1	1	1	0					E	SO	RS	.	>	N		n	~	
1	1	1	1					F	SI	US	/	?	O	_	o	DEL	

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