SH7216 Group

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Data Flash Reprogramming Using Background Operation (BGO)

Introduction

This application note describes the use of background operation (BGO) on the SH7216. BGO allows the CPU to perform other operations while the on-chip data flash (FLD) of the SH7216 is being programmed or erased.

A standard application programming interface (API)* supplied by Renesas Electronics is used to reprogram the on-chip flash.

Note: * This application note does not include a detailed description of the standard API.

Target Device

SH7216

Contents

1. Introduction

1.1 Overview of BGO

In the sample application, the SH7216 is activated in single chip mode and 32 KB of data is programmed to and erased from the on-chip data storage flash memory (FLD).

The SH7216 has a dedicated sequencer (FCU) for the on-chip flash, and the FCU can perform programming and erasing operations independently of the operation of the CPU. In addition, programs can be executed from the on-chip flash while the FLD is performing programming and erasing operations.

Figure 1.1 shows an outline of reprogramming of the FLD by the FCU.

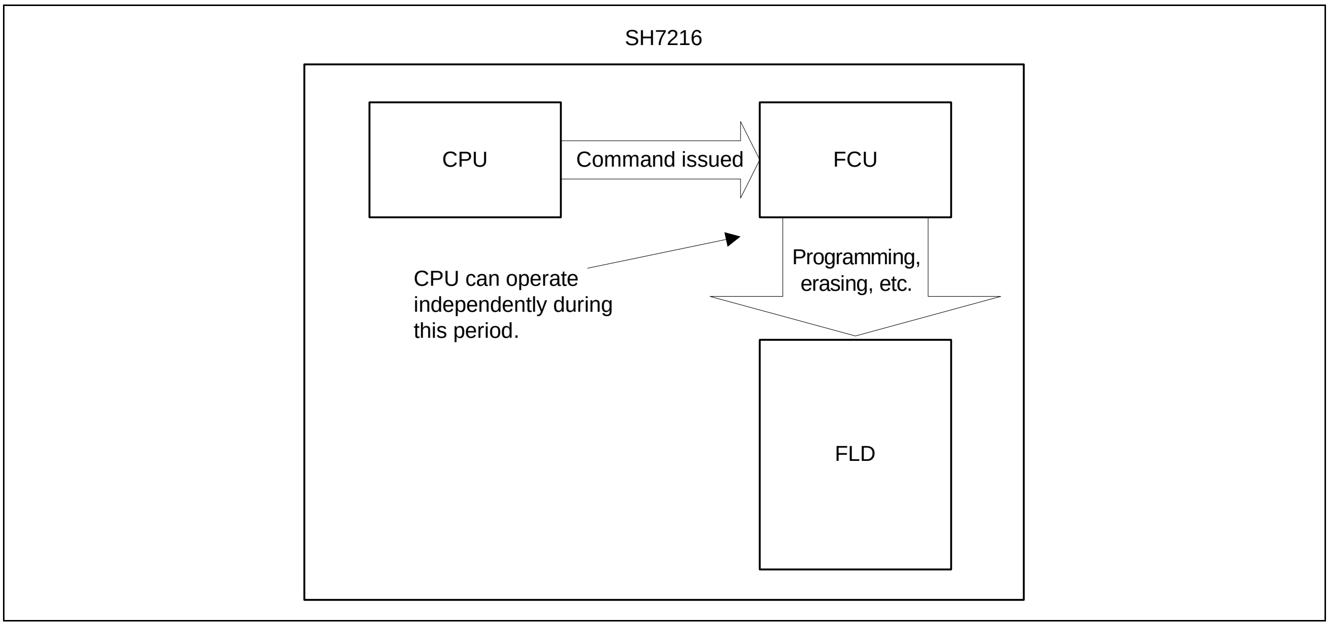


Figure 1.1 FLD Reprogramming Outline

In the sample application, a compare-match timer interrupt is used by the CPU to continuously toggle the output from a general port while the FLD is being programmed and erased. A standard API supplied by Renesas Electronics is used to program and erase the FLD.

Table 1.1 SH7216 Mode Pin Settings for Sample Program

	Pin Settings		
Mode	**FWE**	**MD1**	**MD0**
Single-chip mode	0	1	1

1.2 Functions Used

- Dedicated sequencer for on-chip flash (FCU)
- Compare-match timer (CMT)
- Pin function controller (PFC)
- Interrupt controller (INTC)
- Clock pulse generator (CPG)

1.3 Applicable Conditions

MCU	SH7216
Operating frequency	Internal clock: 200 MHz Bus clock: 50 MHz Peripheral clock: 50 MHz MTU2S clock: 100 MHz AD clock: 50 MHz
Integrated development environment	Renesas Electronics High-performance Embedded Workshop, Ver. 4.07.00
C compiler	Renesas Electronics SuperH RISC engine Family C/C++ Compiler Package, Ver. 9.03, Release 02
Compile options	High-performance Embedded Workshop default settings (-cpu=sh2afpu -pic=1 –object=”$(CONFIGDIR)\$(FILELEAF).obg” -debug –gbr=auto –chgincpath –errorpath –global_volatile=0 -opt_range=all –infinite_loop=0 –del_vacant_loop=0 -struct_alloc=1 –nologo)

1.4 Related Application Notes

The following application note is related to this application note. Refer to it as necessary in conjunction with this application note.

SH Family: Simple Flash API for SH-2 and SH-2A

2. Description of Functions Used

In the sample application, the FCU performs all blank checking, erasing, and programming operations on the FLD. While the FCU is operating, the CPU performs different processing using the CMT interrupt.

2.1 FLD Functions

The FLD is on-chip flash memory for storing data. It has a total capacity of 32 KB, configured as four 8 KB blocks.

Figure 2.1 is a block diagram of the FLD, and figure 2.2 shows the division of the constituent blocks of memory.

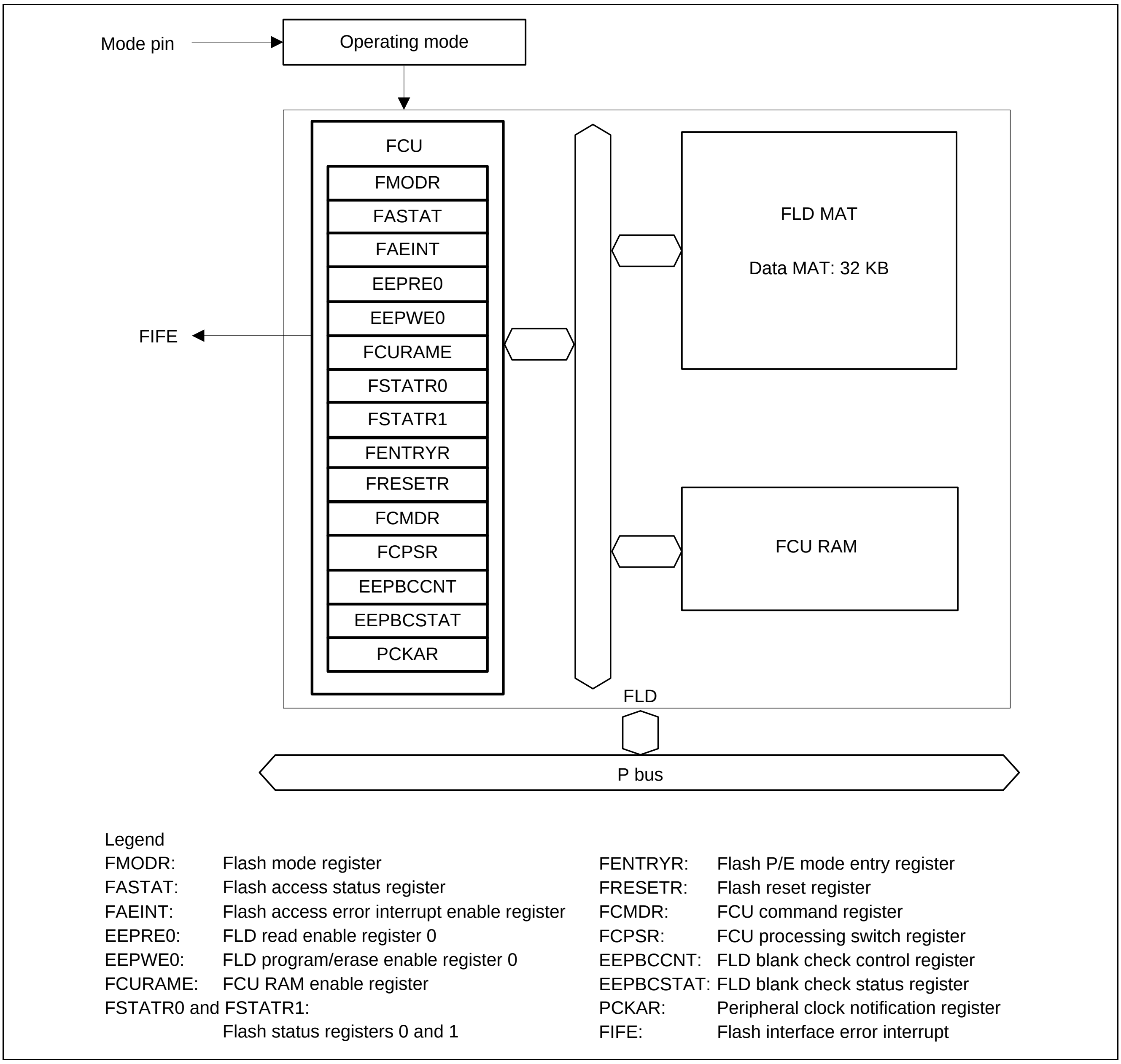


Figure 2.1 FLD Block Diagram

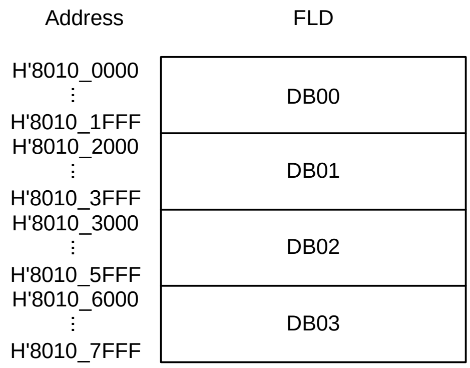


Figure 2.2 FLD Block Divisions

2.1.1 Blank Checking

The FLD uses a complementary memory configuration and when read in the erased state returns an undefined value. It is therefore necessary to perform blank checking to confirm that the FLD has been programmed.

Blank checking is performed by issuing a blank check command to the FCU, after which the FLD blank check status register (EEPBCSTAT) is updated to indicate the result. The unit of data on which blank checking is performed is selectable between 8 bytes and 8 KB (1 block) according to the command issue sequence.

For details of the command issue sequence and operations, see *SH7216 Hardware Manual*.

2.1.2 Erasing

Erasing of the FLD is performed in block (8 KB) units.

When the FCU receives an erase command, is clears to 0 the FRDY bit in flash status register 0 (FSTATR0) and erases the FLD. After erasure completes, the FCU sets the FRDY bit in FSTATR0 to 1. The CPU can determine the operation status of the FCU by checking the FRDY bit in FSTATR0 after a command is issued.

For details of the command issue sequence and operations, see *SH7216 Hardware Manual*.

2.1.3 Programming

In user mode, user program mode, and user boot mode, programming can be performed in 8-byte or 128-byte units. Programming is performed in 256-byte units in boot mode.

As with erasing, the FCU operation status can be determined by checking the FRDY bit in FSTATR0 after a command is issued.

For details of the command issue sequence and operations, see *SH7216 Hardware Manual*.

2.2 CMT Functions

The CMT is a timer with a 16-bit counter and comprises two channels. The sample program uses channel 0 and generates an interrupt every 2 ms (Pϕ = 50 MHz).

Figure 2.3 is a block diagram of the CMT.

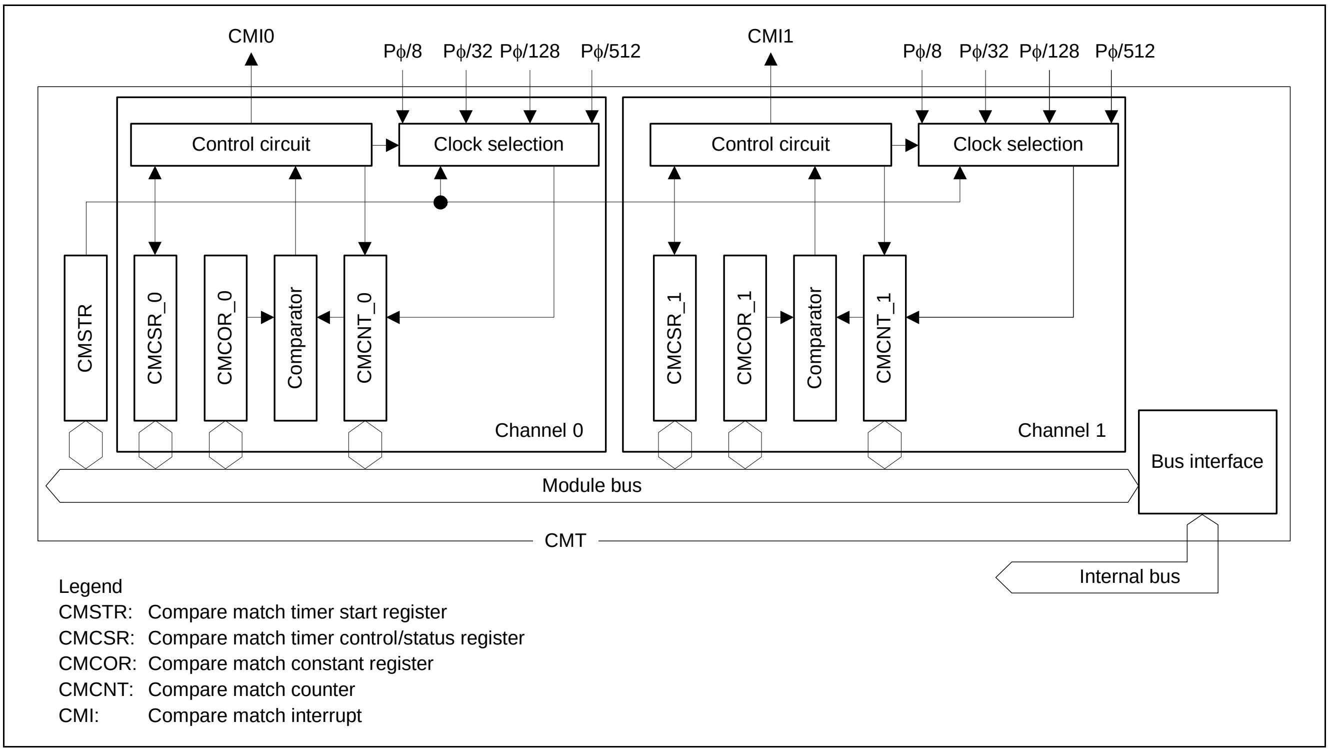
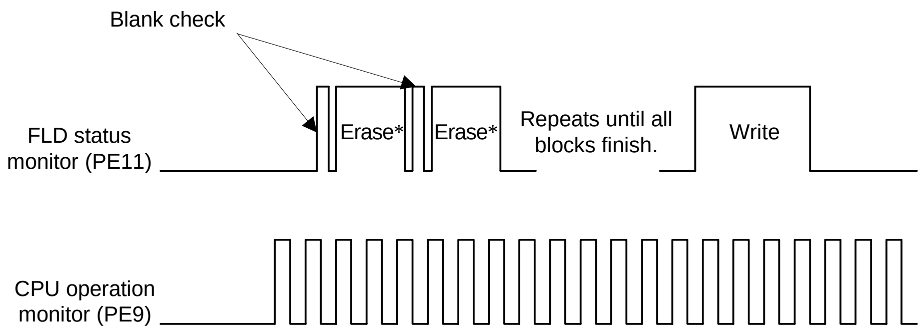


Figure 2.3 Block Diagram of CMT

3. Operation of Sample Program

Figure 3.1 shows an overview of the operation of the sample application.



Note: * No erase operation is performed when the FLD is blank. The CPU operation monitor signal is toggled by the CMT interrupt.

Figure 3.1 Operation Overview

In the sample application, PE9 and PE11 are used to check on BGO. The FLD status monitor pin output is toggled before and after standard API routines are called. In addition, because the return from the standard API routine occurs after operations on the FLD complete, toggling of the CPU operation monitor pin output continues based on the every CMT interrupt.

3.1 Basic Specifications of Sample Program

3.1.1 Sample Program Settings

Table 3.1 lists the settings used in the sample application.

Table 3.1 SH7216 Settings

Function	Item	Setting
All	Frequency (input: 12.5 MHz)	Iϕ = 200 MHz, Bϕ = Pϕ = 50 MHz, Mϕ = 100 MHz, Aϕ = 50 MHz
	Register bank usage	Enables for all interrupt levels
	Interrupt mask level	0
CMT	Count clock division ratio	Pϕ/8
	Compare-match interrupt	Enabled
	Compare-match generation interval	2 ms

3.1.2 Variables Used by Sample Program

Table 3.2 lists the variable used in the sample application.

Table 3.2 Variables Used by Sample Program

Variable	Function	Type Declaration	Remarks
passfail	Stores the return value from the standard API.	unsigned char	
fld_wr_addr	Write destination address in FLD	unsigned long	
fld_wr_source	Storage address of data to be written to FLD	unsigned long	

3.1.3 Functions Used by Sample Program

Table 3.3 lists the functions used in the sample application.

Table 3.3 Functions Used by Sample Program

Variable	Function	File Name	Remarks
main	Main function Makes general port settings for operating checking and calls functions.	main.c	
init_CMT	CMT settings		
init_INTC	INTC settings		
init_CPG	CPG settings Transfers the FRQCR setting program to RAM and executes it.	cpg_init.c	
set_FRQCR	FRQCR settings		Executed in RAM
INT_CMT_CMI0	Inverts the state of the CMT ch0 compare-match interrupt operation confirmation pin.	intprg.c	
R_FlashDataAreaAccess	FLD program/erase enable settings	Flash_API_SH7216.c	
R_FlashDataBlankCheck	FLD blank check		
R_FlashErase	ROM/FLD block erase		
R_FlashWrite	ROM/FLD write		

3.1.4 Standard API

Table 3.4 lists the functions provided by the standard API.

Table 3.4 Standard API Functions

Function Name	Function	Argument	Return Value
R_FlashDataAreaAccess(x,y)	FLD access enable setting (read and write enable)	x: Read enabled setting y: Write enabled setting	None
R_FlashDataBlankCheck(x,y)	FLD blank check	x: Target address y: Target size	0: Blank 1: Not Blank 2: Fail
R_FlashErase(x)	Flash erase (common to ROM and FLD)	x: Target block	0: Succeed 1: Fail
R_FlashWrite(x,y,z)	Flash write (common to ROM and FLD)	x: Write destination address y: Storage address of write data z: Write size	0: Succeed 1: Fail 2-5: Argument error

3.2 Register Settings of Sample Program

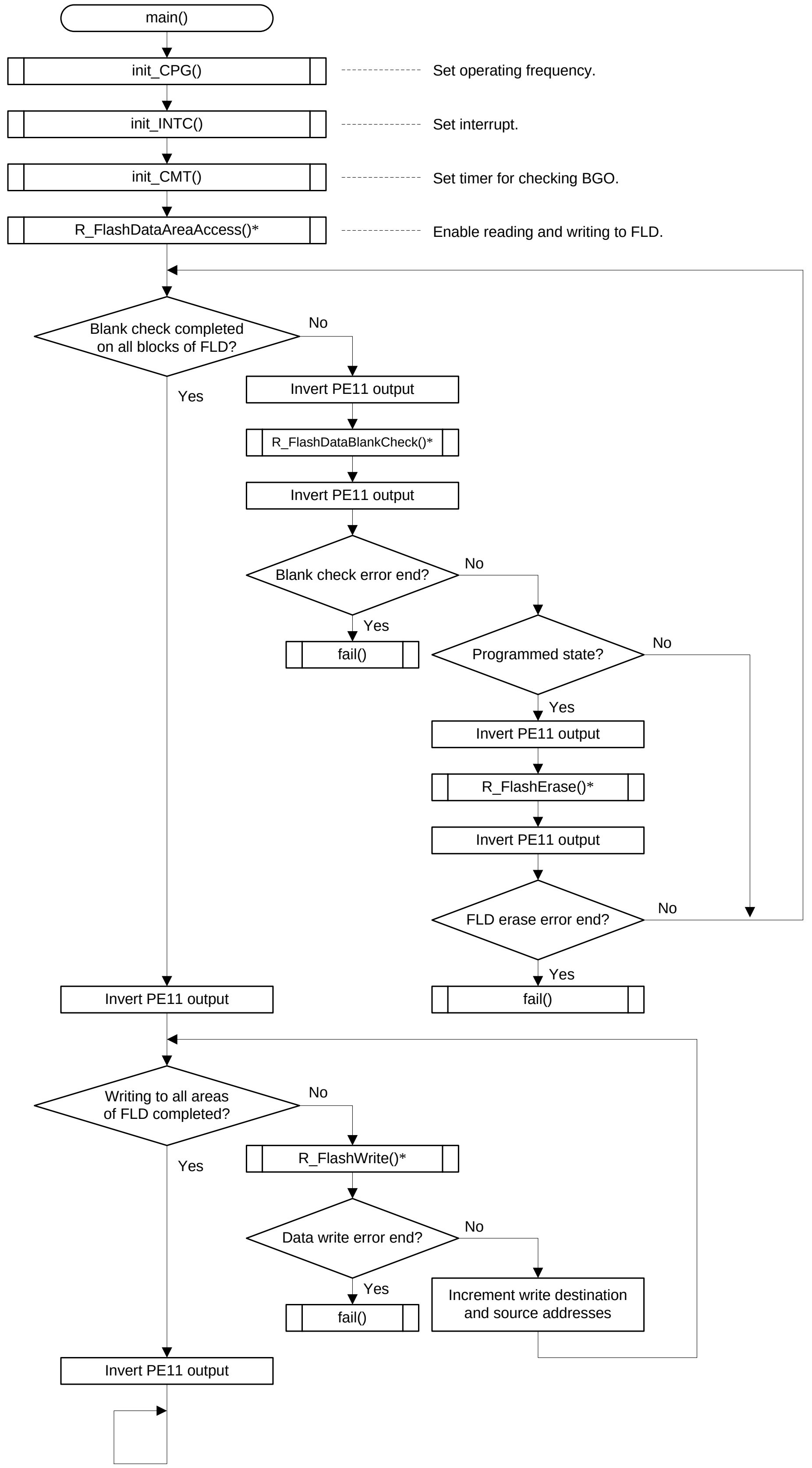
Table 3.5 lists the register settings used in the sample program.

Table 3.5 Register Settings of Sample Program

Module	Register Name	Address	Setting Value	Description
Clock pulse generator (CPG)	Frequency control register (FRQCR)	H'FFFE0010	H'0303	STC[2:0] = B'011: × 1/8 IFC[2:0] = B'000: × 1/4 PFC[2:0] = B'011: × 1/8
	MTU2S clock frequency control register (MCLKCR)	H'FFFE0410	H'41	MSDIVS[1:0] = B'01: × 1/2
	AD clock frequency control register (ACLKCR)	H'FFFE0414	H'43	ASDIVS[1:0] = B'11: × 1/4
Interrupt controller (INTC)	Interrupt priority register 08 (IPR08)	H'FFFE0C04	H'A000	Set interrupt level to 10.
	Bank number register (IBNR)	H'FFFE080E	H'C000	BE[1:0] = B'11: Usage of register banks is according to setting of IBCR.
	Bank control register (IBCR)	H'FFFE080C	H'FFFE	Enable register bank usage for all interrupt levels.
Standby control	Standby control register 4 (STBCR4)	H'FFFE040C	H'F3	MSTP42 = 0: CMT operates
Pin function controller (PFC)	Port E IO register L (PEIORL)	H'FFFE3A06	H'0A00	PE11IOR = B'1: PE11 output PE9IOR = B'1: PE9 output
	Port E data register L (PEDRL)	H'FFFE3A02	H'0000	PE11: Toggled at every FLD operation PE9: Toggled at every CMT interrupt
Compare-match timer (CMT)	Compare match timer start register (CMSTR)	H'FFFEC000	H'0001	
	Compare match timer control/status register 0 (CMCSR0)	H'FFFEC002	H'0040	
	Compare match constant register 0 (CMCOR0)	H'FFFEC006	H'30D4	Compare-match every 2 ms

Note: Flash-related registers are not listed in the table because their settings are made by the standard API.

3.3 Flowcharts of Sample Program



Note: * Standard API function

Figure 3.2 Main Routine

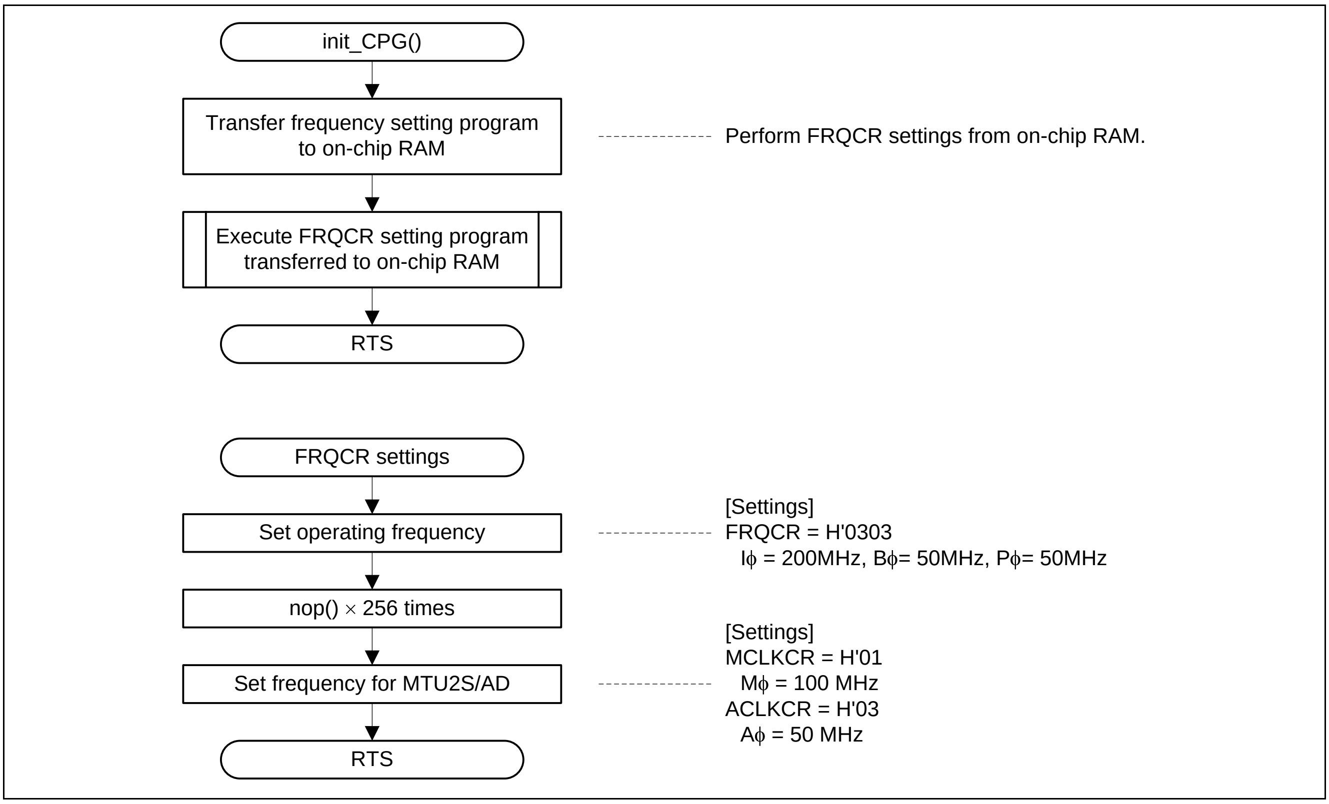


Figure 3.3 Frequency Setting Routine

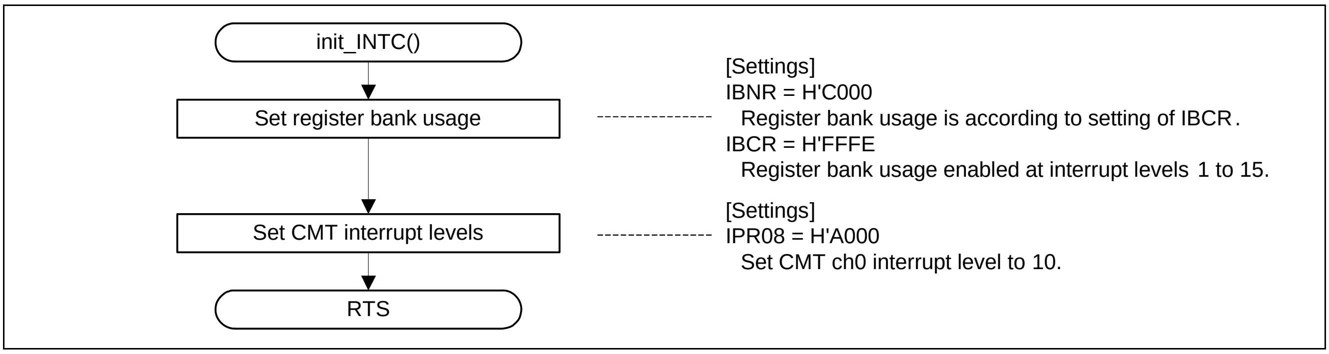


Figure 3.4 INTC Setting Routine

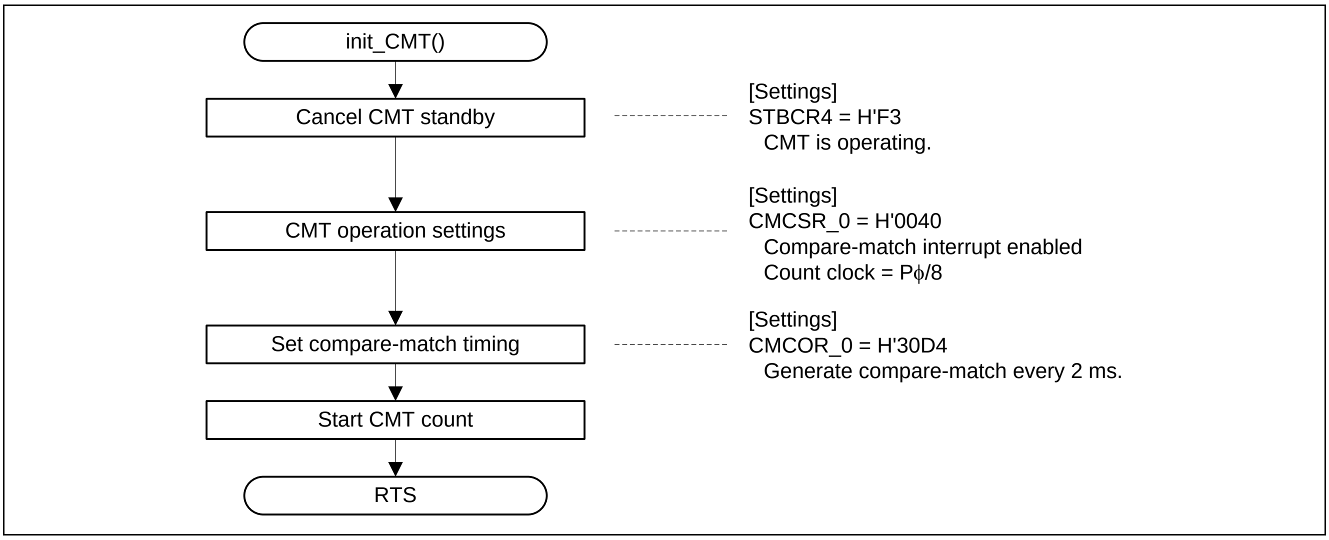


Figure 3.5 CMT Setting Routine

Website and Support

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http://www.renesas.com

Inquiries
http://www.renesas.com/contact/

Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Mar.02.10	—	First edition issued
2.00	Dec.14.10	—	Simple Flash API for SH-2 and SH-2A used to reprogram FLD
2.10	Feb.28.11	—	Added read after FRQCR settings
2.20	Jun.11.12	—	Sample code (simple flash API) revised Sample code for SH7231 Group added

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.
   — The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different type numbers, implement a system-evaluation test for each of the products.

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