An Overview of the QorIQ Qonverge B4860 Base Station-on-a-Chip

EUF-NET-T0645

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Agenda

- The baseband market trends and requirements
- QorIQ Qonverge B4860 block diagram overview
- e6500 and SC3900 cores
- Memory system and interconnect
- CPRI
- MAPLE B3
- Data Path Architecture (DPAA)
- Power Management
- Q&A

Need for Capacity, Speed and QoS

Higher Capacities and Data Rates

Smartphone Density
- 32x increase per km^2 by 2015

Internet over Mobile
- 70% of mobile data by 2014

(Source: Bell Labs, Apr-11)

Wireless Standards & Topologies Evolution

- Multi-standard support required (LTE, LTE-Advanced, 3G-HSPA, TD-SCDMA, GSM)
- Move to heterogeneous networks; Macro, RRH, Metrocell, Picocell & Cloud RAN architectures

Rapidly Evolving Macro Infrastructure

- Drive for increased processing & performance
- Need to leverage spectrum availability
- Desire for efficient energy consumption
- Continual strive for increased efficiency and lower costs

Global LTE Macro Base Station Deployments to Reach 1.5 Million by 2015 (In-Stat, Sep-11)

Global Capital Expenditures by Wireless Carriers for 4G LTE Infrastructure Gear will Reach $36.1 Billion by 2015 (iSuppli Research, Jan-12)
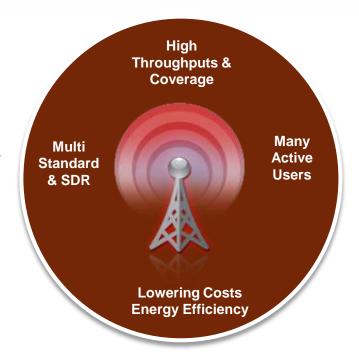
Macro Base Station Challenges

Connectivity

- **Coverage:** Urban, highways and rural
- **Spectral efficiency:** Radio and network performance
- **Multi-standard:** Supports variety of users
- **Reliability:** Zero down time

Capacity

- **Users:** Hundreds of active users
- **Throughputs:** Over 1Gbps data rate
- **Scalable/Modular:** Sectors, antennas, users…
- **Active Antenna, MIMO:** Improved QoS

Cost

- **Space:** Miniaturization and consolidation of equipment
- **Low Impact:** Power & Cost
- **Future Proof:** Easy upgrades, SDR
- **Complete solutions:** Ease of development, faster time to market

High Throughputs & Coverage

Multi Standard & SDR

Many Active Users

Lowering Costs Energy Efficiency

QorIQ Qonverge B4860 – Block Diagram & Benefits

- Next generation, e6500 Dual-Thread Power Architecture® cores offer highest CoreMark/Watt with AltiVec technology for dramatic L2 scheduling acceleration

- Next generation, SC3900 StarCore™ provides 2x DS performance compared to competitive offerings

- 20GHz of Programmable Performance

- Smart hardware acceleration for Layer 1, 2, Control and Transport allows for best in class performance, power and cost

- Large scale SoC integration allows for simpler programming models and easier load balancing

- Integrated, Rich I/O including backhaul & antenna interfaces provides flexibility, interoperability and reduces overall system cost

StarCore™ SC3900 FVP · StarCore™ SC3900 FVP · 32KB D-Cache · 32KB I-Cache · 2MB Banked L2

Power™ e6500 (T1, T2) · Power™ e6500 (T1, T2) · Power™ e6500 (T1, T2) · Power™ e6500 (T1, T2) · 32KB D-Cache · 32KB I-Cache · 2MB Banked L2

64-bit DDR3 Memory Controller · 64-bit DDR3 Memory Controller · 512KB CoreNet Platform Cache · 512KB CoreNet Platform Cache

CoreNet™ Coherency Fabric

MAPLE-B3: 12x RISCs · 2x DEPE · 2x ULF2 · 2x eTVPE · 2x PUPE2 · 1x TCPE · 8x eFTPE · 2x PDPE2 · 1x CRPE · 2x EQPE2 · 2x ULB2 · 3x CRCPE

8x AIF CPRI/9.8G

Security Engine 5.3 · Queue Mgr. · RMAN · Buffer Mgr.

FMAN: Parse, Classify, Distribute IEEE1588v2 · 16xDMA ch.
10G/2.5G/1G · 10G/2.5G/1G · 2.5G/1G · 2.5G/1G · 2.5G/1G · 2.5G/1G · PCIe x4 5G · sRIO x4 5G · sRIO x4 5G

Real Time Debug: Watchpoint Cross Trigger · Perf. Monitor · Corenet Trace · Aurora xB

USB 2.0 · Security Monitor · IFC · 2x DUART · 4x I2C · SD/MMC · eSPI · GPIOs

16-Lane 10G SERDES
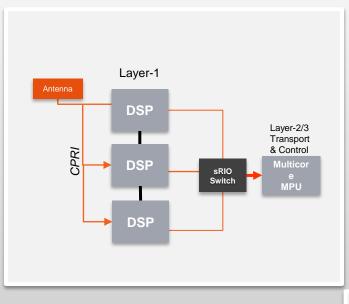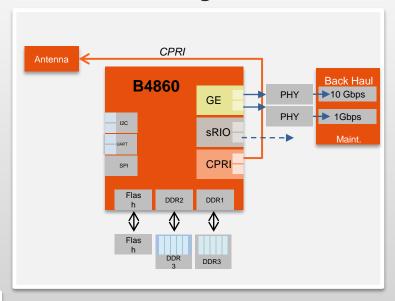
Benefit of Intelligent Integration

3 sector, 20 MHz LTE with 5 major components

Layer-1

Antenna

CPRI

DSP

DSP

DSP

sRIO Switch

Layer-2/3 Transport & Control

Multicore MPU

3 sector, 20 MHz LTE on a single SoC

CPRI

Antenna

B4860

GE

I2C

sRIO

UART

SPI

CPRI

Flash

DDR2

DDR1

Flash

DDR3

DDR3

PHY — 10 Gbps

PHY — 1Gbps

Back Haul

Maint.

COST **POWER**

4X | 3X

B4860 SoC

4X Cost Reduction
3X Power Reduction

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Industry's Highest Capacity

High Density Baseband Solution

LTE/LTE-A SOLUTION
Base station on a chip
20 MHz, 3-sector, 24x24 Ant.
1.4 Gbps Aggregated Throughput

**Supports
Large cells**

**Supports multiple
Radio Access
Technologies**

LTE-Advanced SOLUTION
60 MHz sector on a chip
16 Ant.
1.8Gbps Aggregated Throughput

WCDMA SOLUTION
Base station on a chip
5 MHz, up to 6 cells, 12x12 ant.
318 Mbps Aggregated Throughput

**Supports LTE,
LTE-A, WCDMA,
TD-SCDMA, GSM**

**Multi-mode
Support**

TD-SCDMA SOLUTION
Base station on a chip
32 carriers with a single device

- Industry leading performance solution for base stations
- Based on advanced Power Architecture, StarCore, CoreNet and MAPLE technologies
- First SoC in 28nm technology node for Wireless Infrastructure
- Supports the most advanced mobile wireless standards

B4860

'All New' e6500 Core & Clusters

High Performance

- 64-bit Power Architecture core
- Dual threads provide 1.7 times the performance of a single thread
- Clustered L2 cache allowing strict allocation or full sharing
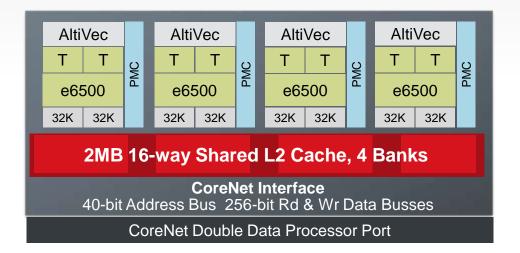- 128b AltiVec SIMD unit

Large Memory Space

- 40-bit real address
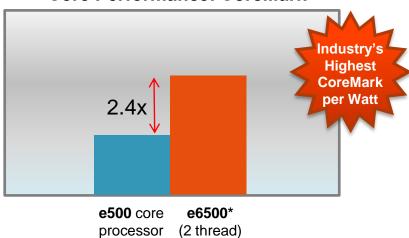- Terabyte physical address

Increase Productivity

- Core Virtualization
  - Hypervisor
  - Logical to Real Address Translation

Energy Efficiency

- Drowsy: core, cluster, AltiVec

AltiVec		PMC	AltiVec		PMC	AltiVec		PMC	AltiVec		PMC
T	T		T	T		T	T		T	T	
e6500			e6500			e6500			e6500		
32K	32K		32K	32K		32K	32K		32K	32K	

2MB 16-way Shared L2 Cache, 4 Banks

CoreNet Interface
40-bit Address Bus 256-bit Rd & Wr Data Busses

CoreNet Double Data Processor Port

Core Performance: CoreMark™

2.4x

Industry's Highest CoreMark per Watt

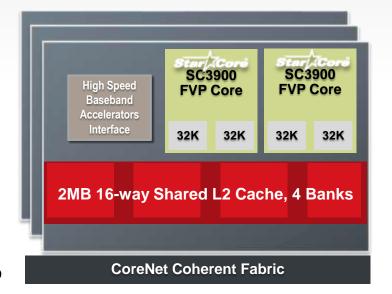**e500** core processor   **e6500*** (2 thread)

*Based on simulation

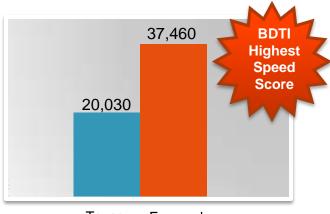# 'All New' SC3900 Core & Clusters

StarCore SC3900 Flexible Vector Processor

- High DSP performance without compromising flexibility
- Step function in performance over previous generation
    - 8 instructions per cycle
        - Up to 8 data lanes vector in a single instruction (SIMD8)
    - 38.4 GMACS per core @1.2 GHz & 1.2 Tbps memory bandwidth per core
- State-of-the-art support for control code with Branch Prediction
- Fully featured Memory Management Unit and Logical to Real Address Translation

High Speed Baseband Accelerators Interface	SC3900 FVP Core		SC3900 FVP Core	
	32K	32K	32K	32K

2MB 16-way Shared L2 Cache, 4 Banks

CoreNet Coherent Fabric

StarCore SC3900 FVP Clusters

- Six SC3900 Cores
- Clustering two SC3900 under a 2MB, multi-banked L2 cache
- High bandwidth accelerator ports (up to 1Tbps per cluster)
- Hardware support for memory coherency between L1, L2 caches and the main memory
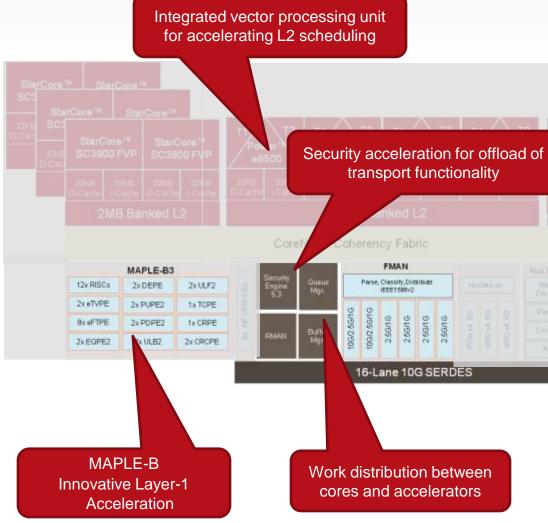
BDTI Highest Speed Score

37,460

20,030

Texas Instruments C66x 1.5GHz	Freescale SC3900 1.2GHz

- BDTIsimMark2000™
- BDTImark2000™

BDTi CERTIFIED
DSP Kernel Benchmarks

Smart Acceleration for Optimal Performance

Integrated vector processing unit for accelerating L2 scheduling

Security acceleration for offload of transport functionality

MAPLE-B Innovative Layer-1 Acceleration

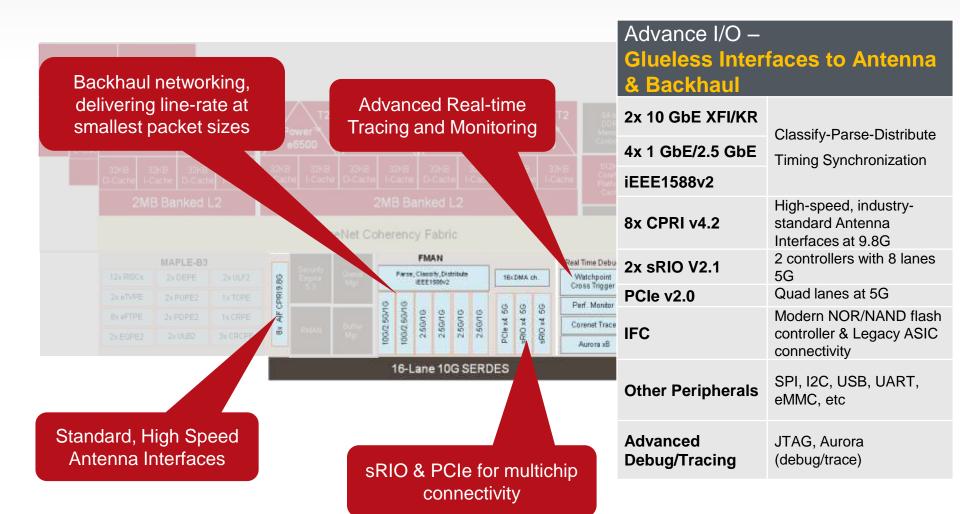Work distribution between cores and accelerators

DPAA Control/Transport Hardware Accelerators	
FMAN Frame Manager	>20 Gbps aggregate throughput, Parse, Classify, Distribute
BMAN Buffer Manager	Manages buffer pools for accelerators and network interfaces
QMAN Queue Manager	Simplified sharing of network interfaces and hardware accelerators by multiple cores
RMAN Rapid IO Manager	Seamless mapping sRIO to DPAA
SEC Security	SNOW-3G, Kasumi, ZUC, IPSec, AES, DES, MD5, SHA-1/2….
Saving CPU Cycles for higher value work	

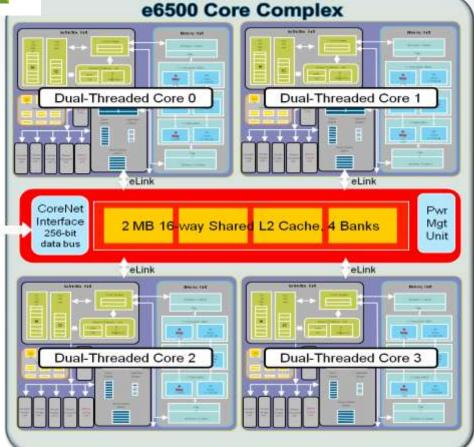| MAPLE-B Layer-1 Hardware Accelerators	
Standards support	LTE, WCDMA, WiMAX, GSM and LTE-Advanced
Throughputs	Very high throughputs enabling low processing latencies
Programming	Simple API
Multimode operations	LTE, LTE-A, WCDMA
Advanced MiMO	Innovative MiMO Equalizer for improved spectral efficiency and reduce processing latencies compared to conventional techniques
Streaming	Direct streaming to/from antenna without core intervention
Internal Embedded Flows	Internal embedded flows for PUSCH/PDSCH Uplink/Downlink processing without core intervention
Completely offloads extensive Baseband algorithms	

Advanced Interfaces for Macro Deployments

Backhaul networking, delivering line-rate at smallest packet sizes

Advanced Real-time Tracing and Monitoring

Standard, High Speed Antenna Interfaces

sRIO & PCIe for multichip connectivity

Advance I/O – Glueless Interfaces to Antenna & Backhaul	
2x 10 GbE XFI/KR	Classify-Parse-Distribute Timing Synchronization
4x 1 GbE/2.5 GbE	
iEEE1588v2	
8x CPRI v4.2	High-speed, industry-standard Antenna Interfaces at 9.8G
2x sRIO V2.1	2 controllers with 8 lanes 5G
PCIe v2.0	Quad lanes at 5G
IFC	Modern NOR/NAND flash controller & Legacy ASIC connectivity
Other Peripherals	SPI, I2C, USB, UART, eMMC, etc
Advanced Debug/Tracing	JTAG, Aurora (debug/trace)

e6500 and sc3900 Clusters and Cores

e6500 Cluster

e6500 Core Complex

- Dual-Threaded Core 0
- Dual-Threaded Core 1
- CoreNet Interface 256-bit data bus
- 2 MB 16-way Shared L2 Cache, 4 Banks
- Pwr Mgt Unit
- Dual-Threaded Core 2
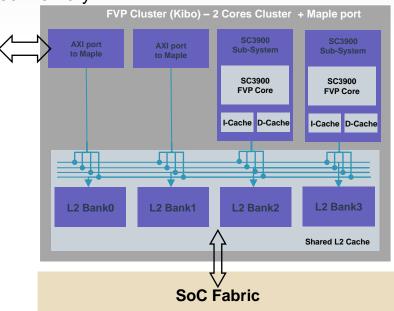- Dual-Threaded Core 3
- eLink

- 64-bit Power Architecture
- e5500 core features plus:
  - Two threads per core (SMT)
  - Dual load/store units, one per thread
- Shared L2 in cluster of 4 cores (8 threads per cluster)
  - 2048KB 16-way, 4 Banks
  - High-performance eLink bus between coreLd/St and instruction fetch units
- Power
  - Drowsy core
  - Power Mgt Unit
  - Wait-on-reservation instruction
- Enhanced MPPerformance
  - Accelerated Atomic Operations
  - Optimized Barrier Instructions
  - Fast intra-cluster sharing
- AltiVec SIMD Unit
- CoreNet BIU
  - 256-bit Din and Dout data busses
- 36-bit Real Address
  - 256 GByte physical addr. space
- Hardware Table Walk
- LRAT
  - Logical to Real Addr. translation mechanism for improved hypervisor performance

- Each thread: Superscalar , seven-issue, out-of-order execution/in-order completion, Branch units with a 512-entry, 4-way set associative Branch Target/History
- Execution units: 1 Load/Store Unit per thread, 2 Simple integer per thread,
  1 Complex for integer Multiply & Divide, 1 Floating-point Unit, Altivec
- 64 TLB SuperPages, 1024-entry 4K Pages, 36-bit Physical Address
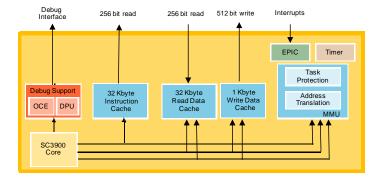
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SC3900 DSP Cluster

- Cluster consists of 2x SC3900 under large and fast shared memory
  - Multibank Cache of 2 MB
  - AXI based accelerators coupling port (45-90 GBps)
- Advanced bus architecture
  - Out of order transaction completion
  - Deep pipeline
  - **Full MESI+L HW Coherency**
- Advanced L1 memory subsystem architecture
  - 36bit address towards memory (64GB space)
  - 32 Kbyte L1 Instruction cache
  - Streaming data paths for read and write
    - 32 Kbyte read only Data Cache
      - 8 way, 128B line, streaming PLRU
    - 1 Kbyte Store/Gather Buffer
- Advanced debug and profiling support
  - Rich event monitoring
  - Multi-core tracing
- Improved core peripherals
  - All core peripherals are SoC accessible
  - Low latency interrupt support

SC3900 Memory Allocation Options
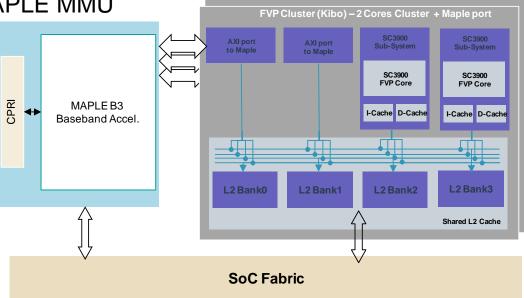
- SC3900 has a fully cache based memory:

  - No constraints due to internal memory sizes and rigid allocations

  - No DMA management and scheduling overheads

  - Smaller internal memories required as only used code/data is allocated

- In addition, the SC3900 supports:

  - Lock/Unlock of DDR space on the L2 Cache – M2 behavior

  - Partition of the L2 Cache to several orthogonal L2 caches

  - Cache equivalent, DMA operations

    - Tightly coupled accelerator port - Ultra High bandwidth and low latency

    - I/O Stashing and Intervention support

    - Cache Management Engine per core

Direct MAPLE/CPRI Access to SC3900 Clusters L2 Caches

- MAPLE/CPRI read/write coherent accesses to clusters L2 caches

    - Provides tight coupling of MAPLE/CPRI to the DSP cores

    - Provides high BW (>76GBps per cluster) and low latency

    - Significantly reduces DDR bus load and coherency traffic

    - Parallel access to multiple SC3900 clusters

- MAPLE/CPRI accesses to DDRs directly via CoreNet fabric
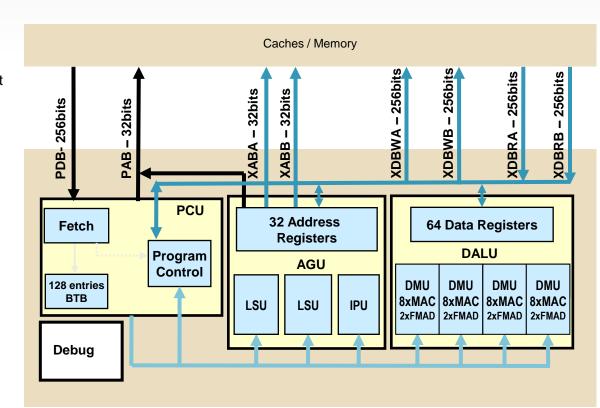
- Target selection is based on MAPLE MMU

SC3900 FVP Core Block Diagram

SC3900 Main Features:

- 4 symmetric DMUs in the DALU
    - **32xMACs** per cycle
    - **16 FLOPs/cycle** Floating Point support
    - **4xSIMD8/vector** support
- High memory bandwidth
    - Program bus – 256 bit/cycle
    - Data bus – up to 1024 bit/cycle
- Address & integer unit
    - 2 Load/Store units
    - General Integer Processing Unit (IPU)
    - Support multiply and shift
- **Large register files**
    - For both AGU and DALU
- Enhanced compiler support
    - Improved predication
    - Enhanced prediction mechanisms
- **Enriched Instruction Set**
    - New binary & syntax
- Improved Multi-core Debug and trace features

SC3900 Optimized for Baseband L1 Processing

- SC3900 is optimized to efficiently handle Baseband PHY Layer processing

- PHY layer processing can be divided into three categories:
  - **Computation intensive DSP** code (mainly MAC intensive)
  - **Data manipulation and less intensive DSP code**
  - **Control code**

- Each one of the categories is non-negligible in processing requirements

- There is no clear boundary separation

- SC3900 accelerates all types of Baseband L1 processing

Computation Intensive DSP Code Acceleration

- SC3900 provides Vector processor capability by increasing the execution units and the whole data-path accordingly

  - Up to 32 MACs per cycles

  - 64 dedicated data registers of 40bit each)

  - Up to 1024bit (128B) core-to-L1 Data Cache throughput per cycle

    - Strong and flexible cache based data streaming abilities

- SC3900 optimized datapath lead to high MAC utilization

- Performance:

  - SC3900 is **3.5x-4x** better than SC3850 in intensive DSP code

L1 Processing - Data Manipulation Acceleration

- "Data manipulation" stands for many different functions existing in Baseband Layer 1 - For examples:
  - Data preparation before/after intensive kernels
    - Ex: data re-ordering, matrix transpose, pack/unpack
  - Less regular kernels or serial/cyclic kernels with low parallelism
    - Ex: QR Decomposition, IIR, Interleaver, encoder.

- SC3900 architecture addresses "Data manipulation" by different means:
  - Data-path flexibility: This is the "Flexible Vector Processor" essence
    - Register file flexibility: Each unit can read/write any registers
    - Execution unit flexibility: Each unit can run different and independent instructions
  - Rich and flexible Instructions set
    - Efficient instruction set which large support of different data type and size
    - New powerful data manipulation specific instructions

- Performance:
  - SC3900 is **2x-3x** better than SC3850 in "Data Manipulation"

L1 Processing - Control Code Efficiency

- SC3900 control code efficiency
  - L1 control functions are tightly integrated with the Arithmetic intensive SW
  - Useful for running scheduling functions that are control intensive

- Control code performance is affected by two main aspects:
  - Core and Compiler efficiency in typical control code constructs
  - Memory system efficiency

- Both have been addressed on the SC3900 – few examples:
  - Ability to flatten decision trees using multiple predicates
  - Third AGU unit with multiply and shift for address calculation and boost control code performance
  - Full support for non-aligned memory access without penalty
  - Larger, clustered 2MB L2 cache to keep the program close to the core

SC3900 Instruction Set

- Robust and flexible Instruction set
  - Significant improvement over previous generations
  - Instructions are highly flexible and fit wide range of DSP operations
  - For example, MAC instruction is defined to support:
    - Single precision 16bx16b, mixed-precision 16bx32b and double precision 32bx32b
    - Saturated and non-saturated arithmetic
    - SIMD and dot-product
    - Real x Real, Real x Complex, Complex x Complex, Complex x Conjugate

- Uniform and consistent Instruction set
  - All instructions can use every register, support all data type, and all addressing modes
  - Remove grouping restrictions
    - All instructions can be grouped together

Baseband Optimized Instruction Set

- The Instruction set definition is based on deep analysis of baseband requirements and MAPLE™ offloaded functionality

- Powerful application specific instructions are introduced in SC3900 (patents pending) – few examples:

  - Maximum/Peak search
    - Find maximum value and index between 4 words and previous results
    - Up to 4 Maxsearch (total of 20 elements) per cycle

  - Filter and correlation dedicated instructions
    - Support for both complex and real filters

  - FFT/DFT highly optimized kernel and instructions

  - Specialized load/store instructions
    - Support matrix transposed & manipulation (2x2, 2x4, 4x4, 2x8, 4x8, 8x8)

  - Bit manipulation
    - Dedicated instruction for scrambling, puncturing, interleaver

  - Reciprocal (1/x), 1/Square Root and Log approximation instructions

Memory System and Interconnect

CoreNet Platform Cache (CPC)

- Instead of using a conventional L3 cache, the B4860 has a CoreNet Platform Cache (CPC) — 512KB for each of the two DRAM controllers.

- The platform cache can function as:

  - L3 cache, or

  - Scratchpad memory, optimizing traffic to main memory and providing transient storage for sharing data among the DSPs and CPUs.

- Fully coherent with the other caches in the SoC

Why Clustering?

- Data and code sharing between cores on the same cluster
  - Low L2-cache access latency
  - Increased cores utilization
  - Reduce DDR traffic
  - Lower power

- Simplified SoC interconnect
  - Reduced area
  - Lower power
  - Higher performance

- Full hardware coherency
  - Within the cluster
  - SoC level

SoC Interconnect

- B4860 has two main fabrics
  - Corenet fabric
  - AXI fabric

- CoreNet fabric is the major fabric
  - Connect between CPU cluster, DSP clusters, OCeaN world, FM and other to CPC/DDR memories.
  - 42.5GB/s of raw bandwidth per cluster.

- AXI fabric
  - Connect between Maple units, CPRI to SC3900 clusters and to CoreNet fabric
  - Allows for high throughput, low latency transfers in Layer 1 sub-system
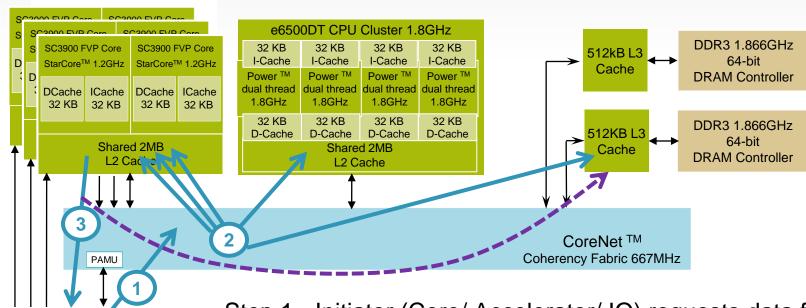
CoreNet Overview

- Coherent fabric
    - Maintains coherence among all the CPU and DSP caches and memories.
    - Reduces multicore software development effort
    - Easier software partitioning and upgrade
- High data bandwidth buses: 256-bit at 667 MHz
    - 42.5 GB/s of raw bandwidth per cluster
- Performance features
    - Parallel accesses
    - Deep pipeline
    - Out-of-order completion
    - Inter-processor communication
- Stashing
- PAMU - Peripheral Access Management Unit

CoreNet Flow Example - Intervention

e6500DT CPU Cluster 1.8GHz			
32 KB I-Cache	32 KB I-Cache	32 KB I-Cache	32 KB I-Cache
Power ™ dual thread 1.8GHz	Power ™ dual thread 1.8GHz	Power ™ dual thread 1.8GHz	Power ™ dual thread 1.8GHz
32 KB D-Cache	32 KB D-Cache	32 KB D-Cache	32 KB D-Cache
Shared 2MB L2 Cache			

SC3900 FVP Core StarCore™ 1.2GHz

SC3900 FVP Core StarCore™ 1.2GHz

DCache 32 KB / ICache 32 KB

DCache 32 KB / ICache 32 KB

Shared 2MB L2 Cache

512kB L3 Cache

512KB L3 Cache

DDR3 1.866GHz 64-bit DRAM Controller

DDR3 1.866GHz 64-bit DRAM Controller

CoreNet ™ Coherency Fabric 667MHz

PAMU

MAPLE B3 Baseband Accel.

- Step 1 - Initiator (Core/ Accelerator/ IO) requests data from CoreNet fabric

- Step 2 – CoreNet broadcasts the request to relevant initiators/target that might have the data

- Step 3 – An initiator/Target which has the latest data responds and the data reaches the requestor (and optionally from memory) without a need for SW intervention

CoreNet Flow Example - Invalidation
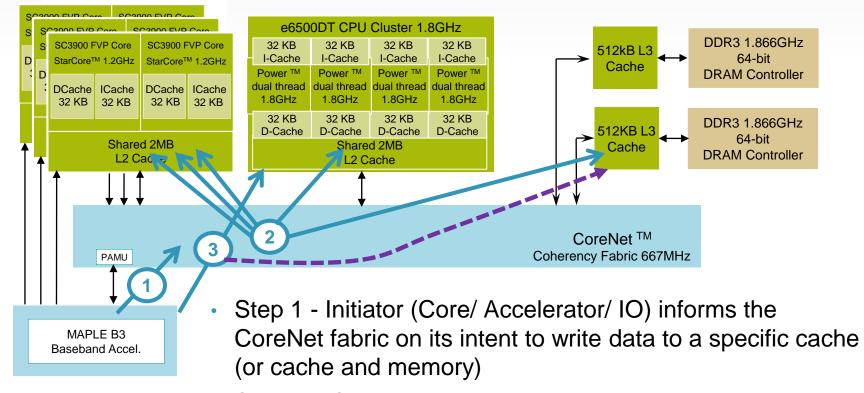
- Step 1 - Initiator (Core/ Accelerator/ IO) informs the CoreNet fabric on its intention to update the memory
- Step 2 – CoreNet broadcasts the request to find the relevant caches that might hold old copies of the data
- Step 3 – Initiators which hold an old version of the data invalidate it and the write data is written by the requestor

CoreNet Flow Example - Stashing

- Step 1 - Initiator (Core/ Accelerator/ IO) informs the CoreNet fabric on its intent to write data to a specific cache (or cache and memory)

- Step 2 – CoreNet broadcasts the request to find the relevant caches that might hold old copies of the data

- Step 3 – The data is written only to the designated target(s)

DMAs

- B4860 instantiates two OceAN DMAs
  - Transfer data between PCI/SRIO to/from the device memories
  - Transfer data between two locations in the memory

- Each DMA includes the following features
  - Eight channels
  - Advanced chaining and strides capabilities
  - Priority support
  - Can be activated using external signal

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CPRI
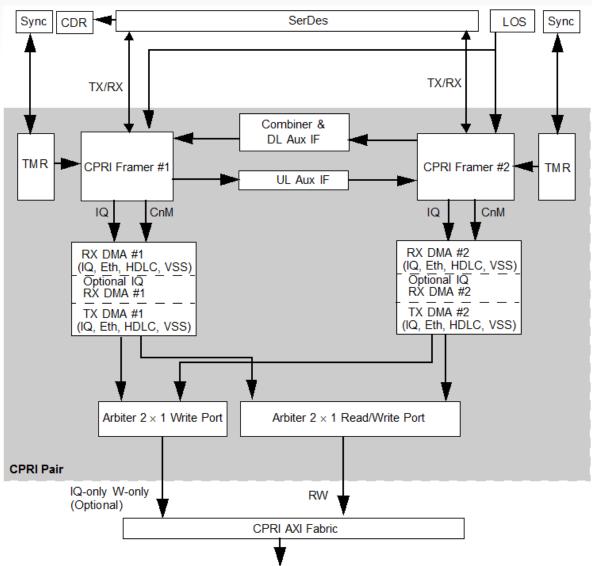
CPRI Antenna Interface in B4860

- The CPRI complex enables communication among radio devices over a CPRI bus.

- The CPRI complex is designed to support the CPRI V4.2 specification and can be configured to support several air interface standards, including WiMAX, LTE, and WCDMA.

- The complex supports up to 8 CPRI links (4 pairs) with each link configurable as a master or slave port.

- Up to 9.8Gbps per lane

- Each CPRI link supports three types of service access points (SAPs):

    - IQ samples for antenna transferred through the SAP IQ Interface

    - CPRI frames synchronized by the SAP synchronization interface

    - CPRI link control and management (C&M) data transferred between SAPs in both CPRI master and slave ports.

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CPRI – Block Diagram
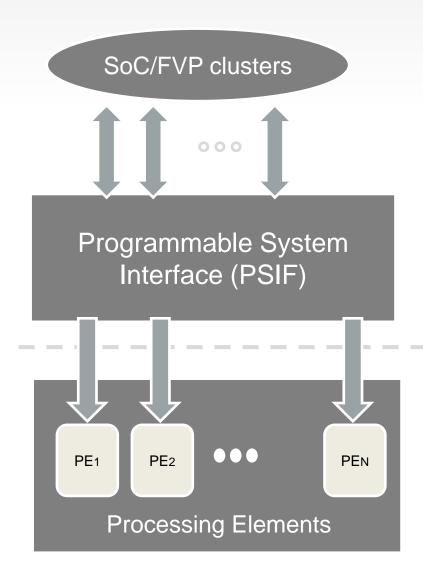
MAPLE-B3

MAPLE Modular Concept

SoC/FVP clusters

Programmable System Interface (PSIF)

PE1   PE2   ● ● ●   PEN

Processing Elements

<u>PSIF</u>

Central programmable control for:

- Tasks Scheduling

- Efficient DMAing from/to SoC and internally

- Flexible processing flow allow multiple

  standards support

- BD parsing and job configurations

- Interrupts handling

- Internal Embedded Data Flows

<u>PE-s</u>

- Highly efficient HW implementation of baseband

  computational extensive algorithms
- Lego like concept allowing:
  - Fast solution derivation (Macro to Femto)
  - Use of algorithms commonality between technologies (LTE, WCDMA, CDMA, WiMAX)

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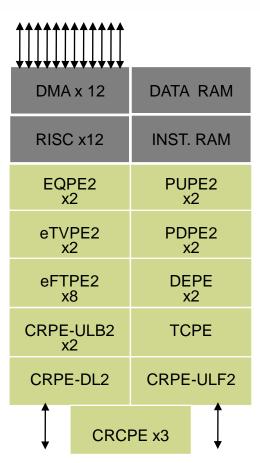
B4860 Baseband Accelerator Platform - Highlights

- LTE/LTE-Advanced, HSPA/WCDMA, WiMAX and Multi-Mode acceleration solution.

- **LTE/LTE-A** acceleration R.10/R.11 compliant:
  - PUSCH acceleration including Cancelation, Flexible MIMO Equalization, iDFT, De-Modulator, De-Scrambler, DINTLV, UCI decoding, HARQ, FEC decoding.
  - PDSCH acceleration including full PDSCH/PMCH from FEC to IFFT, internal RS generation, multiplexing of PBCH, PSS, SSS at RE mapping.
  - FFT/DFT and vector multiplication acceleration for PUSCH, PCFICH, PHICH, PDCCH, PRACH, Sounding and general purpose use

- **WCDMA/HSPA** acceleration R.10/R.11 compliant:
  - HSDPA FEC encoding
  - HSUPA, WCDMA FEC decoding
  - Downlink Chip Rate acceleration
  - Uplink Chip Rate acceleration with flexible scheme addressing:
    - Low latency control channels processing
    - Flexible Interference Cancelation, Grouping, Pre-Despreading data channels processing
    - Flexible Path Searcher and RACH correlations

MAPLE-B3

DMA x 12	DATA RAM
RISC x12	INST. RAM
EQPE2 x2	PUPE2 x2
eTVPE2 x2	PDPE2 x2
eFTPE2 x8	DEPE x2
CRPE-ULB2 x2	TCPE
CRPE-DL2	CRPE-ULF2
CRCPE x3	
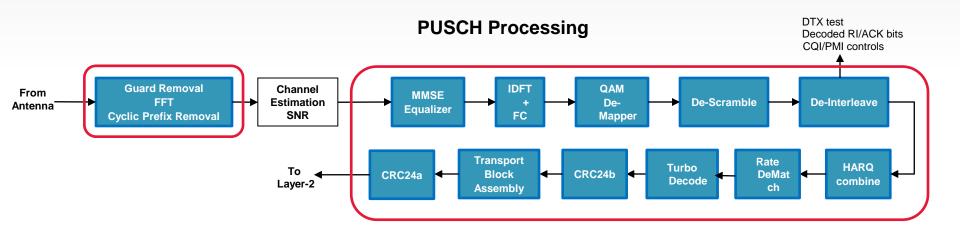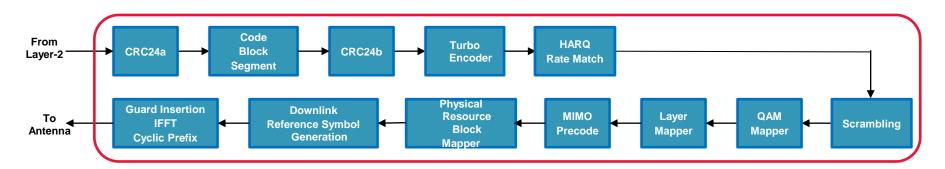
MAPLE-B3 Layer-1 Processing Accel. (LTE/LTE-A)

PUSCH Processing

DTX test
Decoded RI/ACK bits
CQI/PMI controls

From Antenna → **Guard Removal FFT Cyclic Prefix Removal** → **Channel Estimation SNR** → **MMSE Equalizer** → **IDFT + FC** → **QAM De-Mapper** → **De-Scramble** → **De-Interleave**

CRC24a ← **Transport Block Assembly** ← **CRC24b** ← **Turbo Decode** ← **Rate DeMatch** ← **HARQ combine**

To Layer-2 ← **CRC24a**

PDSCH Processing

From Layer-2 → **CRC24a** → **Code Block Segment** → **CRC24b** → **Turbo Encoder** → **HARQ Rate Match**

Guard Insertion IFFT Cyclic Prefix ← **Downlink Reference Symbol Generation** ← **Physical Resource Block Mapper** ← **MIMO Precode** ← **Layer Mapper** ← **QAM Mapper** ← **Scrambling**

To Antenna ← **Guard Insertion IFFT Cyclic Prefix**

Legend:
- MAPLE-PE
- MAPLE Embedded Flow
- SC3900 Core

3GPP TS36.211/212/213

freescale™

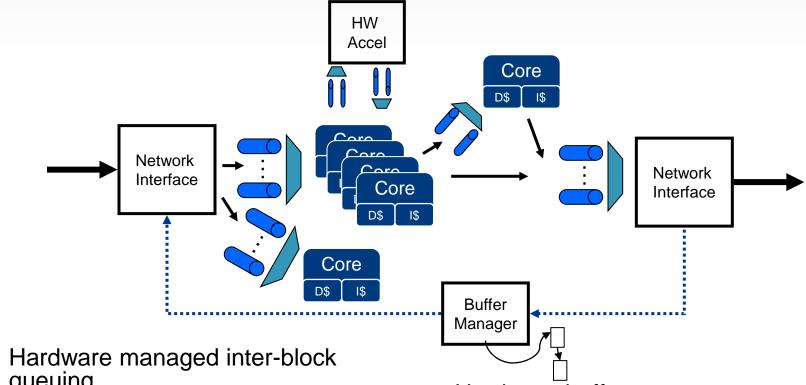# Data Path Architecture (DPAA)

DPAA Purposes

- Acceleration of frame/packet processing
  - Network protocols (Layer-1 to 4)
  - Standard algorithmics (security and content processing)
- Classification and Distribution of data flows among cores and software partitions
  - Load balancing through parse/classify/distribute
  - Load spreading through queues shared among multiple consumers
- Abstract and manage efficiently Intercore communications and the access to shared resources (NW interfaces, HW-Accelerators, Buffers, Queues)
  - More sophisticated approach compared to basic BD/buffer list
- Scalability and Portability
  - Across 'any' mix of cores, accelerators and device boundaries
  - Across device generations

Basic Hardware Infrastructure

- Hardware managed inter-block queuing
  - Class based prioritization
  - Large number of queues
  - Universal: between all blocks
- Lock free, low software overhead queuing

- Hardware buffer management
  - Hardware blocks acquire and release buffers without software intervention
- Lock free, low software overhead buffer pool management for hardware use

Frame manager

Frame Manager is responsible for preprocessing and moving Ethernet packets into and out of the datapath

- **Parsing**
  - Packet Parsing at wire speed
  - Supports standard protocols parsing and identification by HW (VLAN/IP/UDP/TCP/SCTP/PPPoE/PPP/MPLS/GRE/IPSec …)
  - Supports non-standard UDF header parsing for custom protocols

- **Classification / Distribution**
  - Coarse classification based on Key generation Hash and exact match lookup
  - Supports aggregated speed of 20Gbps, 30Mpps@667MHz
  - Lookups configured by user, can be chained
  - Classification result is frame queue ID, storage profile and policing profile.
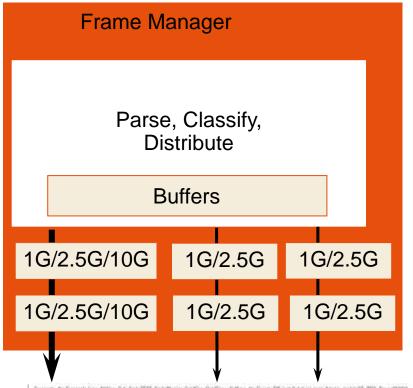
- **Ingress Policing**
  - Two rate – three colour marking algorithm (rfc 2968 & 4115)
  - Up to 256 internal profiles

- **General**
  - Supports offline PCD on frames extracted from QMan
  - Supports "Independent" mode (no work with BMan & QMan, BD ring model)
  - Per port egress rate limiting
  - Statistics & Multicast support
  - Support for IEEE1588 thru HW-Timestamping

Frame Manager

Parse, Classify, Distribute

Buffers

| 1G/2.5G/10G | 1G/2.5G | 1G/2.5G |
| 1G/2.5G/10G | 1G/2.5G | 1G/2.5G |

B4860QDS Development Platform

- Dual-AMC form factor

- Standalone operation or pluggable into open-top standard MicroTCA chassis

- 2x DDR3
    - 4GB Dual rank 64b/72b, 1.867GHz w/ ECC
    - 2GB 64b/72b, 1.866GHz w/ ECC

- Ethernet –
    - Up to 6x 1G/2.5G SGMII
    - Up to 2x 10G XFI/XAUI

- CPRI v4.2 – up to 8 ports at 9.8G

- sRIO v2.1 – up to 2 four lanes ports at 5G su

- PCIe v2.0 – one port four lanes at 5G suppo

- AMC connector for HSSI expansions

- SFP+ - Two optical transceivers

- NOR, NAND, I2C & SPI FLASH memories

- USB, UART

- JTAG & Aurora interfaces