MICROCHIP

AN3770

ATA8352 Module Application Note

Introduction

This application note describes the ATA8352 module, which provides hardware setup guidance for the ATA8352 Ultra-Wide Band (UWB) device. The ATA8352 module is available in two versions:

1. A Demo version with a 48 MHz crystal used in the Demo kit
2. A TDoA version with an external clock and sync signal used in the TDoA kit

Additionally, this document provides the following:

- Current consumption data with the current profile operating in the Prover or the Verifier mode
- Bill of Material (BOM) for the module

Note: The schematic, layout and BOM are provided in a zip folder.

Table of Contents

1. Quick References

1.1 Reference Documentation

For further details, refer to the following:

1. ATA8352 User Guide V1.0
2. ATA8352 Datasheet V1.0

1.2 Acronyms and Abbreviations

Table 1-1. Acronyms and Abbreviations

Acronyms	Abbreviations
ADC	Analog-to-Digital Converter
ETSI	European Telecommunications Standards Institute
FCC	Federal Communications Commission
FLL	Frequency Lock Loop
MCU	Microcontroller Unit
PR	Prover
RF	Radio Frequency
SMA	Sub Miniature version A
SSID	Secure Session Identifier
SWD	Serial Wire Debugger
TDoA	Time Difference of Arrival
USB	Universal Serial Bus
UWB	Ultra-Wide Band
VR	Verifier
XTAL	External Crystal

2. ATA8352 Module

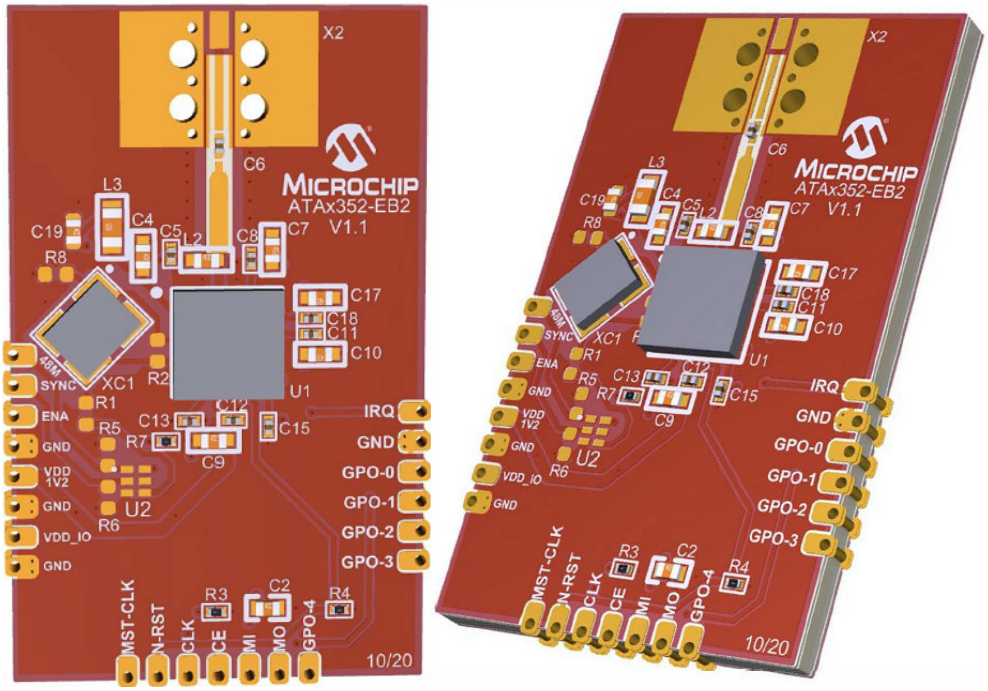
The ATA8352 Module includes the following components to set up a UWB system, controlled by an external MCU host using an SPI connection (see the following figure):

- ATA8352 Module UWB transceiver device
- 48 MHz crystal for Demo version or external clock supply for TDoA version
- SMA connector for a UWB antenna

The version V1.1 of the module does not include the following:

- UWB prefilter for the 6 GHz to 8.2 GHz band
- Integrated UWB antenna for the 6 GHz to 8.2 GHz band (Replacing the SMA connector)

Figure 2-1. ATA8352 Module (without SMA Connector)

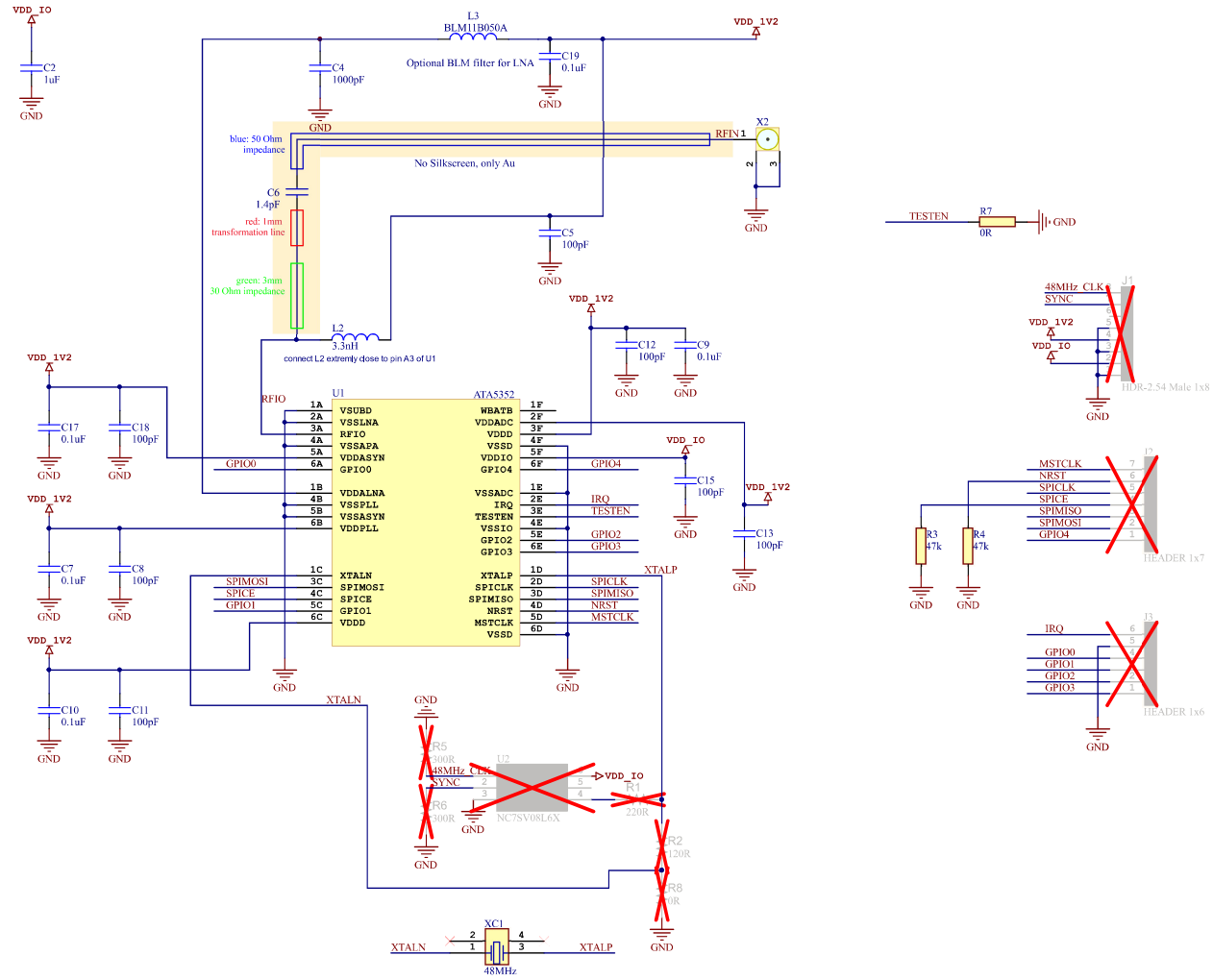


2.1 Schematic

The following figure shows the overview of a schematic for the ATA8352 module. This module includes the following components:

1. ATA8352 UWB device with BGA 33-pin package
2. SMA connector
3. 48 MHz crystal for Demo version or external clock circuitry for TDoA version
4. A 30 to 50Ω microstrip transformation line for the RFIO pin
   Some components are marked as not mounted as they are not necessary for application use.

Figure 2-2. ATA8352 Module Overview Schematic

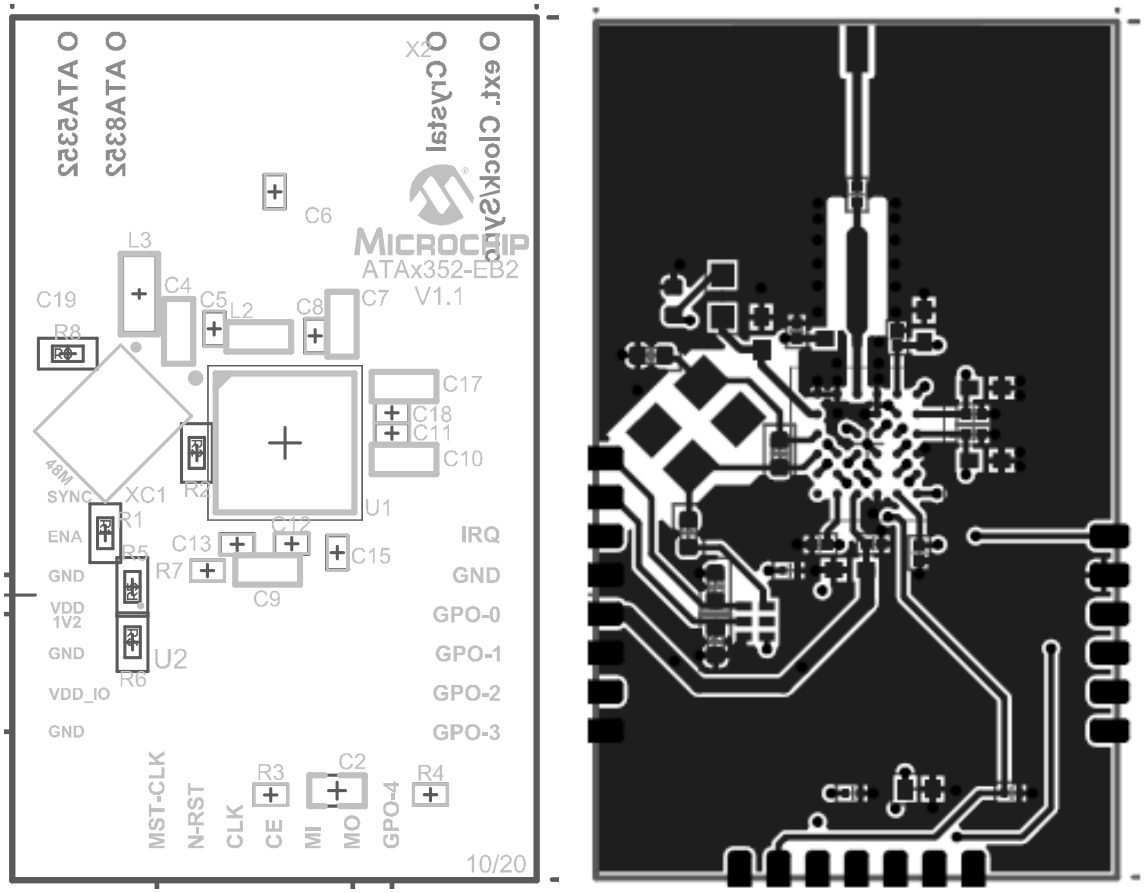


2.2 Layout

The following figure shows the top layer of the ATA8352 module with the routing of the RF path and GND routing of the ATA8352 device with the blocking capacitors. The structure connection between the PCB and SMA connector contains a 30 to 50Ω convertor. The recommended guidelines are:

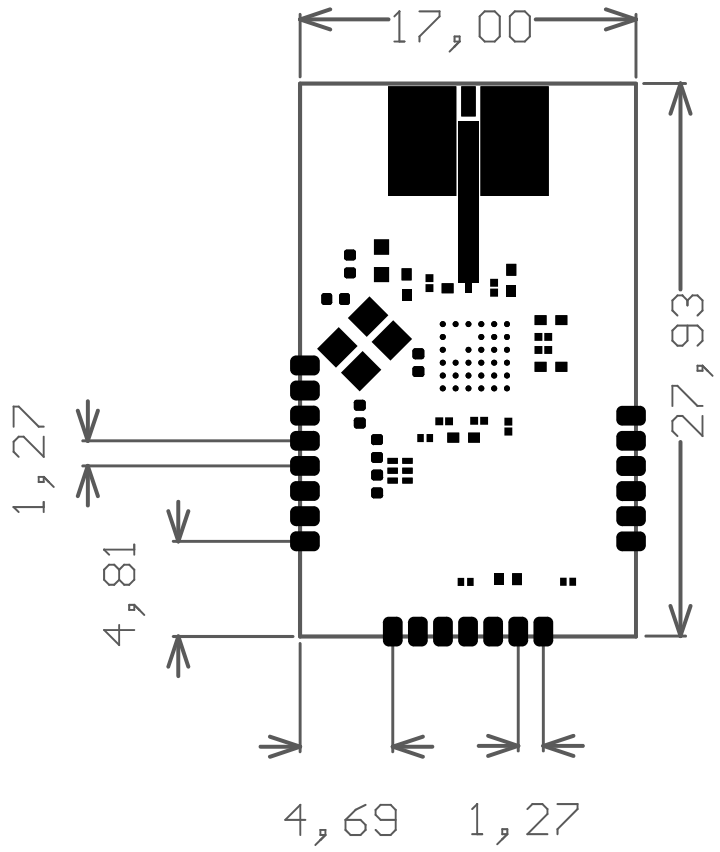
1. Use the same structure and follow the GND connection, as shown in the ATA8352 device layout and the capacitors to achieve the required sensitivity level. The layout shown in the following figure is designed in such a way to avoid loop connections for the power and ground supplies.

Figure 2-3. ATA8352 – Top Layer and Components



2. Place three vias below the ATA8352 device for the GND connection.
3. Place a short and straight connection for the RF path to the SMA connector and copy the 30 to 50Ω conversion.
   The following figure illustrates the module footprint.

Figure 2-4. ATA8352 Module Footprint (dimension in mm)



2.3 Pin Details

The following table describes the ATA8352 module pin details. Refer to Figure 2-1 for the signal names.

Table 2-1. ATA8352 Module Pin Details

Name	Description
ENA	(Optional) Active high input to enable the DC/DC converter for 1.25V supply
GND	GND connection
VDD_1V2	1.25V supply connection (use either external 1.25V supply or the on-module DCDC converter if mounted. Do not use both supplies.)
GND	GND connection
VDD_IO	3.3V IO supply connection
GND	GND connection
MST-CLK	4 MHz master clock output from the ATA8352
N-RST	Active low reset input signal for the ATA8352
SPI-CLK	SPI clock input signal for the ATA8352
SPI-CE	Active high SPI chip enable signal for the ATA8352
SPI-MISO	SPI MISO input signal for the ATA8352

.....continued	
Name	**Description**
SPI-MOSI	SPI MOSI output signal from the ATA8352
GPO-4	GPO4 signal from the ATA8352
GPO-3	GPO3 signal from the ATA8352
GPO-2	GPO2 signal from the ATA8352
GPO-1	GPO1 signal from the ATA8352
GPO-0	GPO0 signal from the ATA8352
GND	GND connection
IRQ	Active high interrupt output from the ATA8352
48M	48 MHz input clock
RF	SMA 50Ω antenna connector footprint
SYNC	Synchronization input signal

2.4 Bill of Material

The following table provides the Bill of Material (BOM) for the ATA8352 module.

Table 2-2. ATA8352 Module BOM

Designator	Description	Quantity	Value
C2	Ceramic capacitor, SMD 0402, X5R, 10V, 10%	1	1 µF
C4	Ceramic capacitor, SMD 0402, X7R, 16V, +/-10% (de19761)	1	1000 pF
C5	Ceramic capacitor, SMD 0201, C0G, 25V, +/-0.25pF	1	100 pF
C6	Ceramic Capacitor, KEMET CBR02C149B5GAC, HF-Capacitor C0G / NP0, 1.4 pF, 50 V, HiQ-CBR, ± 0.1pF, 125 °C, SMD 0201	1	1.4 pF
C6 (Alternative)	Murata GCM0335C1E1R5CA16, AEC-Q200, HF-Capacitor C0G / NP0, 1.5 pF, 50 V, HiQ-CBR, ± 0.25pF, 125 °C, SMD 0201	1	1.5 pF
C7	Ceramic capacitor, SMD 0402, X7R, 16V, +/-10% (de19761)	1	0.1 µF
C8	Ceramic capacitor, SMD 0201, C0G, 25V, +/-0.25pF	1	100 pF
C9	Ceramic capacitor, SMD 0402, X7R, 16V, +/-10% (de19761)	1	0.1 µF
C10	Ceramic capacitor, SMD 0402, X7R, 16V, +/-10% (de19761)	1	0.1 µF
C11	Ceramic capacitor, SMD 0201, C0G, 25V, +/-0.25pF	1	100 pF
C12	Ceramic capacitor, SMD 0201, C0G, 25V, +/-0.25pF	1	100 pF
C13	Ceramic capacitor, SMD 0201, C0G, 25V, +/-0.25pF	1	100 pF
C15	Ceramic capacitor, SMD 0201, C0G, 25V, +/-0.25pF	1	100 pF
C17	Ceramic capacitor, SMD 0402, X7R, 16V, +/-10% (de19761)	1	0.1 µF
C18	Ceramic capacitor, SMD 0201, C0G, 25V, +/-0.25pF	1	100 pF
C19	Ceramic capacitor, SMD 0402, X7R, 16V, +/-10% (de19761)	1	0.1 µF

.....continued

Designator	Description	Quantity	Value
L2	Chip inductor, SMD 0402, Murata LQW15AN3N3B80D, Fixed Inductors Rdc = 30 mOhms , 3.3nH, Ir = 2000mA +/-0.1nH	1	3.3 nH
L3	(Optional) Johanson Technology L-14C56NJV4T Inductor RF, 0603, 56NH, 5%	1	BLM11B050A
R3	RES 2.2 KΩ, 1/20W, 5%, 0201 SMD	1	47k
R4	RES 2.2 KΩ, 1/20W, 5%, 0201 SMD	1	47k
R7	Thick film resistor, SMD 0201, 1/20W, 5%	1	0R
U1	UWB TRX	1	ATA8352
X2	CONN SMA Jack R/A 500 Ω Edge MNT high frequency 26.5 GHz	1	901-10512-3
XC1	SMD crystal ECX-2236 series, 48 MHz Refer to crystal specification in ATA8352 datasheet.	1	48 MHz

3. Current Consumption Profile

This chapter provides the ATA8352 module's current consumption profiles of the Prover and Verifier modes. The measurement conditions are:

- $t_{ambient}$ = 25°C
- VDDIO = 3.0V

Note: The data sheet defines the electrical characteristics of the ATA8352 module's RF and IO pins. The 3.3V IO supply provides voltage to the DC/DC converter on the module.

3.1 Supply Current Profile

The supply current profile for a complete Verifier operation including power-up, initialization, calibration of the Verifier offset mode with Prover response and power-down is shown in Figure 3-1, Figure 3-2 and Figure 3-3. The figures show the analog signals, VDD_CORE (supply voltage for the core), IDD_CORE (supply current for the core) at 1.25V and IDD_SUP at 3.3V (supply domain), and the digital signals, N_RST, 1V2_ENA, SPI_CE, IRQ and Controller state signals. The complete sequence of operations requires ~7.6 ms. The measurement was performed with the evaluation kit using a SAMC21 MCU with 48 MHz clock and an SPI communication with an 8 MHz clock frequency. The supply current (IDD_SUP) includes the current for the VDD_IO domain and the current for a DC/DC converter to supply the VDD_CORE domain (the DC/DC converter used for the measurement is TPS62244-Q1 with a 1.25V output voltage).

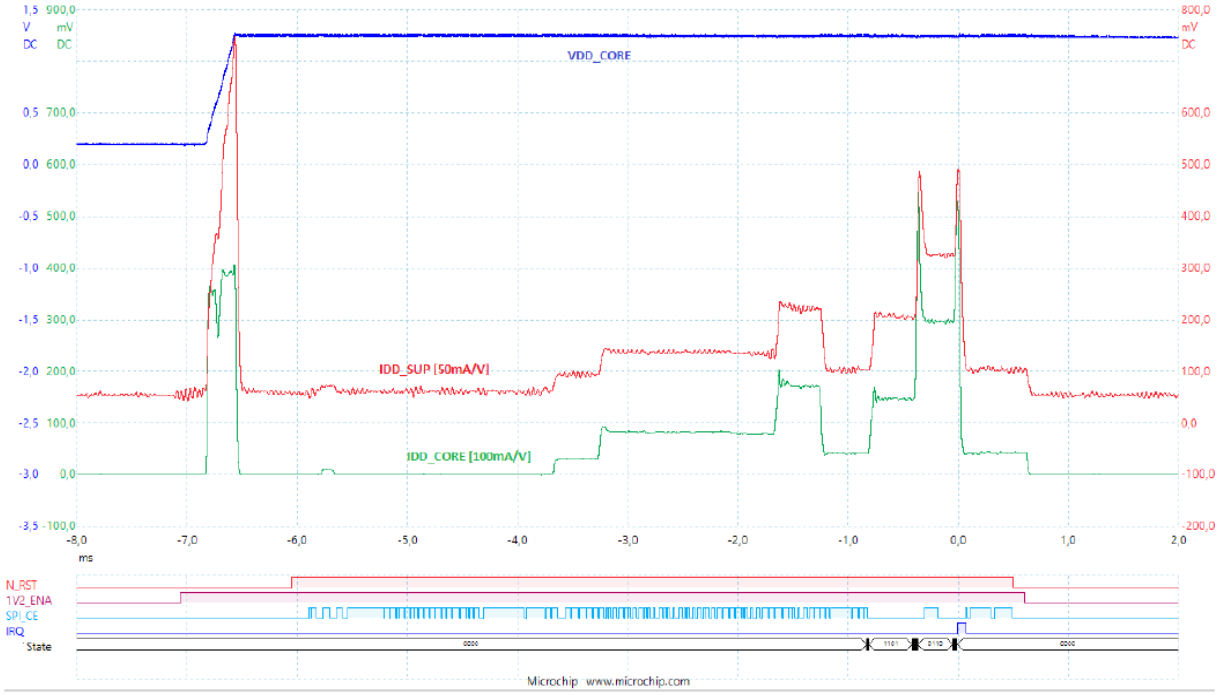
Following is the sequence operation:

1. The DC/DC is switched On at -7.1 ms when the signal, 1V2_ENA, is set to high and, after 1 ms, release the N_RST signal.
2. Switch On the crystal oscillator at -5.8 ms.
3. Load the device registers.
4. Initialize the PLL at -3.7 ms and the calibration of the FLL RX at -3.2 ms.
5. Set the RF RX and TX frequencies at -1.7 ms, and enter the READY mode at -1.0 ms.

3.2 Verifier Mode Current Consumption

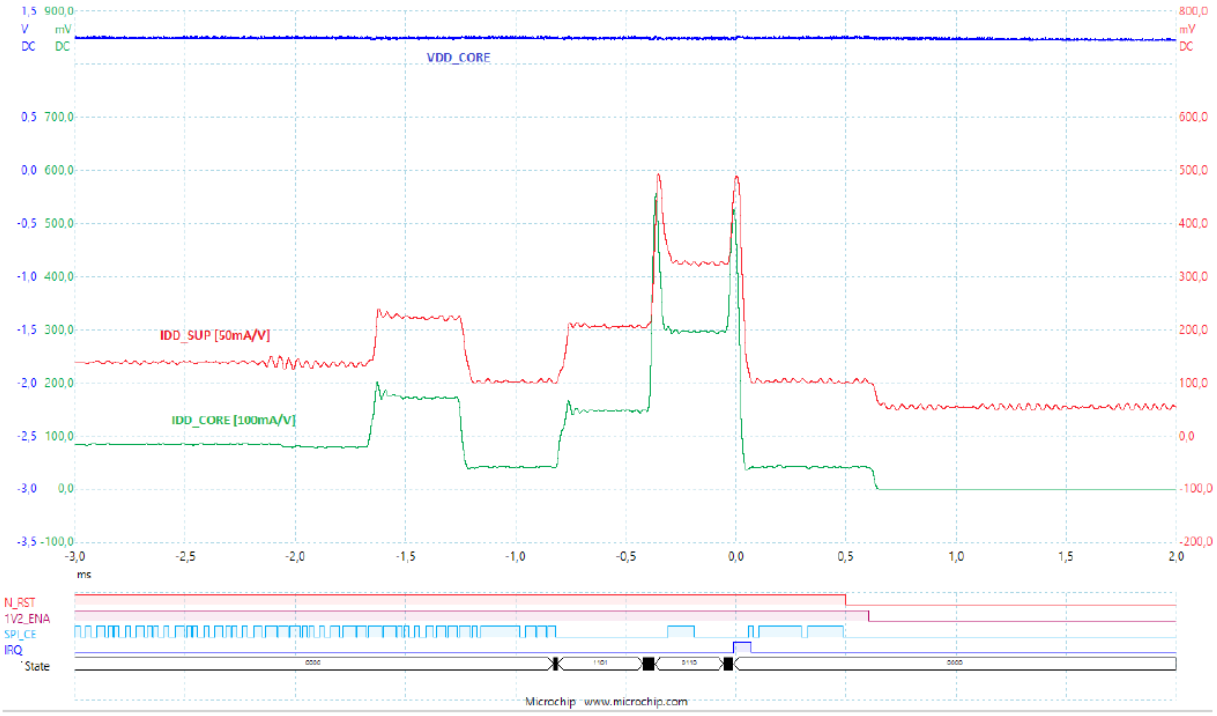
The Verifier mode, VRo, is started with the transmission state and the controller state at 1101 (for details, refer to the ATA8352 User Manual). See the following figure. The turnaround phases follow this and receive a locked state at 0110. The IRQ signal is activated when the receive is complete and the registers are read. Enable the reset signal (N_RST) to start the power-down sequence and disable the DC/DC converter.

Figure 3-1. Current Profile for Verifier Operation



The following figure (zoomed in from -2.0 to 2.0 ms) shows the Verifier operation in VRo mode.

Figure 3-2. Current Profile for the Verifier Mode VRo



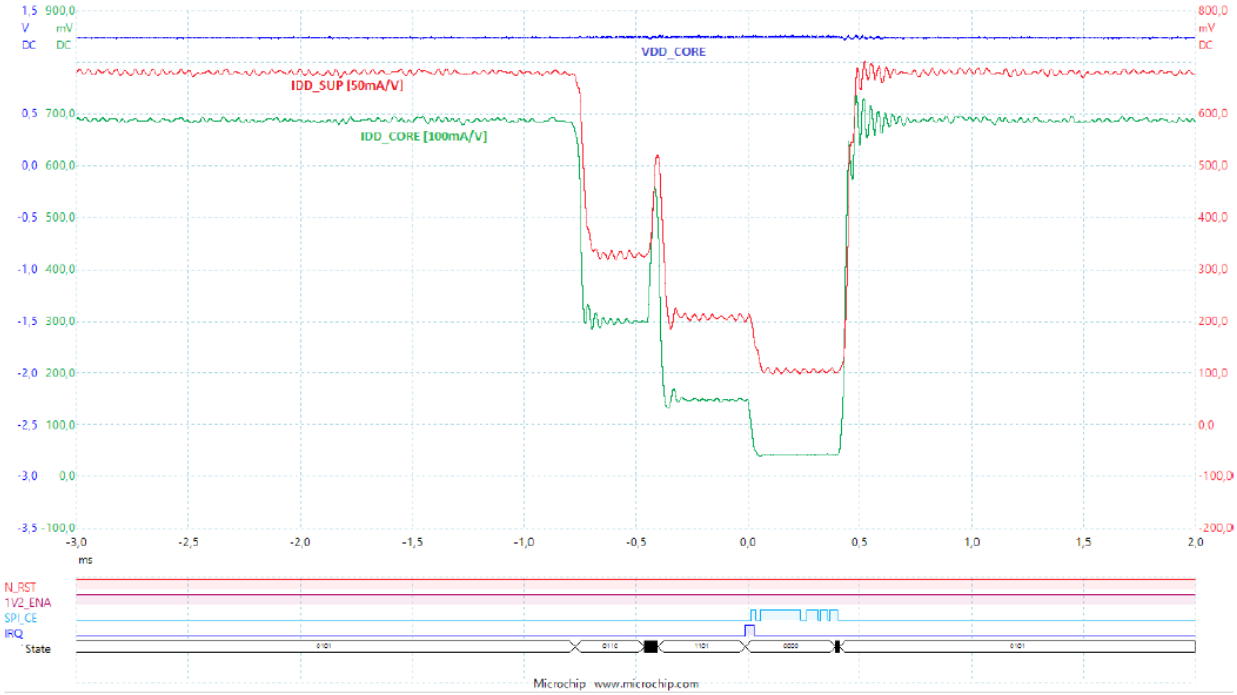
3.3 Prover Mode Current Consumption

When starting the Prover mode, the device switches to the RX mode to search for a preamble.

The following figure shows the Prover mode, PRo, where the initialization occurs similarly to the sequence in Figure 3-2. The Prover is operating in the Receiver Search mode as the controller state at 0101 indicates. When a valid preamble and sync word are received, the Receiver Locked mode is entered as the controller state at 0110 shows.

When the data telegram is received, the turnaround sequence is executed and the Prover transmits the telegram, as the controller state at 1101 shows. This sequence is completed with an IRQ and the activation of the Prover mode, PRo, for the next data telegram.

Figure 3-3. Current Profile for the Prover Mode PRo

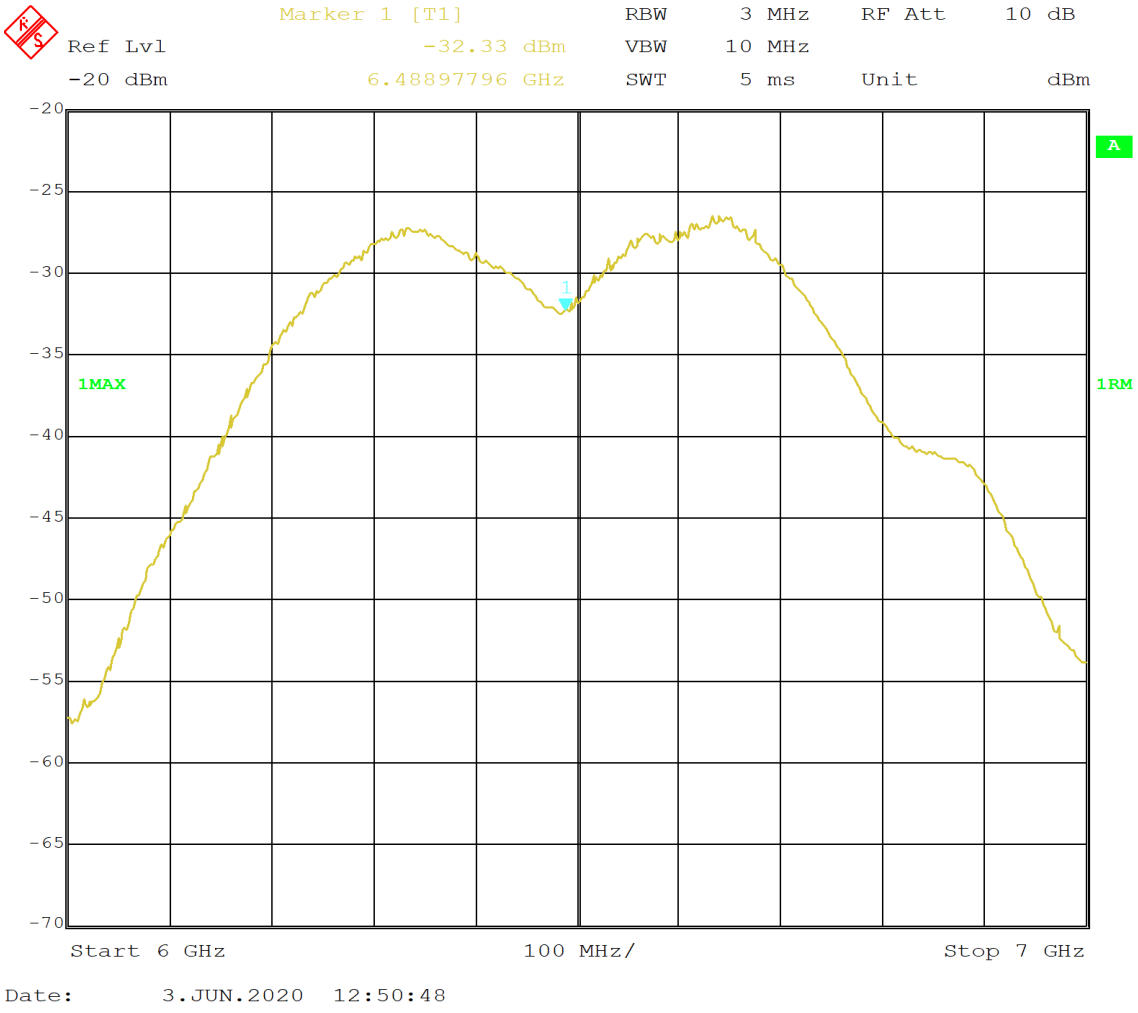


4. RF Spectrum

The following figure shows the RF spectrum for the ATA8352 module for the composite signal (with low and high modulation switched on).

Note: The RF filter is not used in the current version of the module, that is, the spectrum shown is the RF output signal of the device with the default settings, f_{TX} at 6.52 GHz.

Figure 4-1. RF Spectrum for Composite Signal



5. Document Revision History

Revision	Date	Section	Description
A	01/2021	Document	Initial Revision

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