AURIX™ TC27x variants

Data Sheet Addendum

TC277 / TC275 / TC270

AURIX™

32-bit microcontroller

Addendum

v1.10, 2021-04-15

Microcontrollers

Table of Contents

About this document

Scope and purpose

This document is an addendum to the TC27x data sheet listing all intended product variants, key parameters such as memory size, and optional features..

Naming Conventions

Prefix

- SAK: $T_{ambient}$ Temperature Range from -40 °C up to +125 °C
- SAL: $T_{ambient}$ Temperature Range from -40 °C up to +150 °C (packaged device)

Feature Package

- T – Standard type without HSM
- TP – Standard type with HSM enabled
- TC – customer specific feature set

1. Variants BC Step

Derivative	Production Status	Package Type	Temp. Range	Chip ID	Freq. (MHz)	Flash (MB) 1)	EEPROM (KB) 2)	Total SRAM (KB)	Core 1&2 TC16P 1)		Core 0 TC16E 1)		LMU (KB)	ADC Chan.	FlexRay (#/ch.)	ETH	HSM	CAN FD
									DSPR (KB)	PSPR (KB)	DSPR (KB)	PSPR (KB)						
SAK-TC277TP-64F200S BC	on request	PG-LFBGA-292	-40°C – +125°C	4740 7153$_H$ 4746 7153$_H$ 3)	200	4	64 @ 500k	472	120	32	112	24	32	60	1 / 2	Yes	Yes	No

1) The address range starts at the lowest address defined in the User's Manual (See the Memory Maps chapter).
2) Based on an EEPROM emulation algorithm with a wear levelling factor of 6 (size scales with number of program/erase cycles, for more details see User Manual).
3) Featuring flash firmware (µCode) version 23$_H$

2. Variants CA Step

Derivative	Production Status 1)	Package Type	Temp. Range	Chip ID	Freq. (MHz)	PFlash (MB) 2)	EEPROM (KB) 3)	Total SRAM (KB)	Core 1&2 TC16P 2)		Core 0 TC16E 2)		LMU (KB)	ADC Chan.	FlexRay (#/ch.)	ETH	HSM	CAN FD	CAN FD ISO frame
									DSPR (KB)	PSPR (KB)	DSPR (KB)	PSPR (KB)							
SAK-TC277TP-64F200S CA	on request	PG-LFBGA-292	-40°C – +125°C	4742 7160H 4746 7160H 4)	200	4	64 @ 500k	472	120	32	112	24	32	60	1 / 2	Yes	Yes	Yes	No
SAK-TC277TC-64F200S CA	on request	PG-LFBGA-292	-40°C – +125°C	4742 7560H 4746 7560H 4)	200	4	24 @ 500k	424	120	24	112	24	-	60	1 / 2	No	Yes	No	No
SAK-TC277T-64F200S CA	on request	PG-LFBGA-292	-40°C – +125°C	0742 7160H 0746 7160H 4)	200	4	64 @ 500k	472	120	32	112	24	32	60	1 / 2	Yes	No	Yes	No
SAK-TC275TP-64F200W CA	on request	PG-LQFP-176	-40°C – +125°C	4742 7060H 4746 7060H 4)	200	4	64 @ 500k	472	120	32	112	24	32	48	1 / 2	Yes	Yes	Yes	No
SAK-TC275TC-64F200W CA	on request	PG-LQFP-176	-40°C – +125°C	4742 7460H 4746 7460H 4)	200	4	24 @ 500k	424	120	24	112	24	-	48	1 / 2	No	Yes	No	No
SAK-TC275T-64F200W CA	on request	PG-LQFP-176	-40°C – +125°C	0742 7060H 0746 7060H 4)	200	4	64 @ 500k	472	120	32	112	24	32	48	1 / 2	Yes	No	Yes	No
SAL-TC275T-64F200W CA	on request	PG-LQFP-176	-40°C – +150°C	0742 7060H 0746 7060H 4)	200	4	64 @ 500k	472	120	32	112	24	32	48	1 / 2	Yes	No	Yes	No
SAL-TC275TP-64F200W CA	on request	PG-LQFP-176	-40°C – +150°C	4742 7060H 4746 7060H 4)	200	4	64 @ 500k	472	120	32	112	24	32	48	1 / 2	Yes	Yes	Yes	No
SAL-TC277T-64F200S CA	on request	PG-LFBGA-292	-40°C – +150°C	0742 7160H 0746 7160H 4)	200	4	64 @ 500k	472	120	32	112	24	32	60	1 / 2	Yes	No	Yes	No

1) STANDARD = serial production planned.
2) The address range starts at the lowest address defined in the User's Manual (See the Memory Maps chapter).
3) Based on an EEPROM emulation algorithm with a wear levelling factor of 6 (size scales with number of program/erase cycles, for more details see User Manual).
4) Featuring flash firmware (µCode) version 23H

3. Variants DB Step

Derivative	Production Status 1)	Package Type	Temp. Range	Chip ID	Freq. (MHz)	Flash (MB) 2)	EEPROM (KB) 3)	Total SRAM (KB)	Core 1&2 TC16P 2)		Core 0 TC16E 2)		LMU (KB)	ADC Chan.	FlexRay (#/ch.)	ETH	HSM	CAN FD	CAN FD ISO frame
									DSPR (KB)	PSPR (KB)	DSPR (KB)	PSPR (KB)							
SAK-TC277TP-64F200S DB	on request	PG-LFBGA-292	-40°C – +125°C	4744 7171H 4746 7171H 4)	200	4	64 @ 500k	472	120	32	112	24	32	60	1 / 2	Yes	Yes	Yes	No
SAK-TC277T-64F200S DB	on request	PG-LFBGA-292	-40°C – +125°C	0744 7171H 0746 7171H 4)	200	4	64 @ 500k	472	120	32	112	24	32	60	1 / 2	Yes	No	Yes	No
SAK-TC277TC-64F200S DB	on request	PG-LFBGA-292	-40°C – +125°C	4744 7571 H 4746 7571H 4)	200	4	24 @ 500k	424	120	24	112	24	-	60	1 / 2	No	Yes	No	No
SAK-TC275TP-64F200W DB	on request	PG-LQFP-176	-40°C – +125°C	4744 7071 H 4746 7071H 4)	200	4	64 @ 500k	472	120	32	112	24	32	48	1 / 2	Yes	Yes	Yes	No
SAK-TC275T-64F200W DB	on request	PG-LQFP-176	-40°C – +125°C	4744 7071 H 4746 7071H 4)	200	4	64 @ 500k	472	120	32	112	24	32	48	1 / 2	Yes	Yes	No	No
SAK-TC275TC-64F200W DB	on request	PG-LQFP-176	-40°C – +125°C	4744 7471 H 4746 7471H 4)	200	4	24 @ 500k	424	120	24	112	24	-	48	1 / 2	No	Yes	No	No
SAL-TC270TP-64F200 DB	on request	Bare Die	-40°C – +170°C	4744 7F71 H4746	200	4	64 @ 500k	472	120	32	112	24	32	60	1 / 2	Yes	Yes	Yes	No
SAL-TC277TP-64F200S DB	on request	PG-LFBGA-292	-40°C – +150°C	4) 4744 7171H 4746 7171H 4)	200	4	64 @ 500k	472	120	32	112	24	32	60	1 / 2	Yes	Yes	Yes	No
SAL-TC277T-64F200S DB	on request	PG-LFBGA-292	-40°C – +150°C	0744 7171H 0746 7171H 4)	200	4	64 @ 500k	472	120	32	112	24	32	60	1 / 2	Yes	No	Yes	No
SAL-TC275TP-64F200W DB	on request	PG-LQFP-176	-40°C – +150°C	4744 7071 H 4746 7071H 4)	200	4	64 @ 500k	472	120	32	112	24	32	48	1 / 2	Yes	Yes	Yes	No
SAL-TC275T-64F200W DB	on request	PG-LQFP-176	-40°C – +150°C	4744 7071 H 4746 7071H 4)	200	4	64 @ 500k	472	120	32	112	24	32	48	1 / 2	Yes	Yes	No	No

1) STANDARD = serial production planned.
2) The address range starts at the lowest address defined in the User's Manual (See the Memory Maps chapter).
3) Based on an EEPROM emulation algorithm with a wear levelling factor of 6 (size scales with number of program/erase cycles, for more details see User Manual).
4) Featuring flash firmware (µCode) version 23H

4. Variants DC Step

Derivative	Production Status 1)	Package Type	Temp. Range	Chip ID	Freq. (MHz)	Flash (MB) 2)	EEPROM (KB) 3)	Total SRAM (KB)	Core 1&2 TC16P 2)		Core 0 TC16E 2)		LMU (KB)	ADC Chan.	FlexRay (#/ch.)	ETH	HSM	CAN FD	CAN FD ISO frame
									DSPR (KB)	PSPR (KB)	DSPR (KB)	PSPR (KB)							
SAK-TC277TP-64F200N DC	STANDARD	PG-LFBGA-292	-40°C – +125°C	4746 7172H	200	4	64 @ 500k	472	120	32	112	24	32	60	1 / 2	Yes	Yes	Yes	Yes
SAK-TC277TP-64F200S DC	STANDARD	PG-LFBGA-292	-40°C – +125°C	4746 7172H	200	4	64 @ 500k	472	120	32	112	24	32	60	1 / 2	Yes	Yes	Yes	No
SAK-TC277TC-64F200N DC	on request	PG-LFBGA-292	-40°C – +125°C	4746 7572H	200	4	24 @ 500k	424	120	24	112	24	-	60	1 / 2	No	Yes	Yes	Yes
SAK-TC277TC-64F200S DC	on request	PG-LFBGA-292	-40°C – +125°C	4746 7572H	200	4	24 @ 500k	424	120	24	112	24	-	60	1 / 2	No	Yes	No	No
SAK-TC277T-64F200N DC	on request	PG-LFBGA-292	-40°C – +125°C	0746 7172H	200	4	64 @ 500k	472	120	32	112	24	32	60	1 / 2	Yes	No	Yes	Yes
SAK-TC277T-64F200S DC	on request	PG-LFBGA-292	-40°C – +125°C	0746 7172H	200	4	64 @ 500k	472	120	32	112	24	32	60	1 / 2	Yes	No	Yes	No
SAK-TC275TP-64F200N DC	STANDARD	PG-LQFP-176	-40°C – +125°C	4746 7072H	200	4	64 @ 500k	472	120	32	112	24	32	48	1 / 2	Yes	Yes	Yes	Yes
SAK-TC275TP-64F200W DC	on request	PG-LQFP-176	-40°C – +125°C	4746 7072H	200	4	64 @ 500k	472	120	32	112	24	32	48	1 / 2	Yes	Yes	Yes	No
SAK-TC275T-64F200N DC	on request	PG-LQFP-176	-40°C – +125°C	0746 7072H	200	4	64 @ 500k	472	120	32	112	24	32	48	1 / 2	Yes	No	Yes	Yes
SAK-TC275TC-64F200N DC	on request	PG-LQFP-176	-40°C – +125°C	4746 7472H	200	4	24 @ 500k	424	120	24	112	24	-	48	1 / 2	No	Yes	Yes	Yes
SAK-TC275TC-64F200W DC	on request	PG-LQFP-176	-40°C – +125°C	4746 7472H	200	4	24 @ 500k	424	120	24	112	24	-	48	1 / 2	No	Yes	No	No
SAK-TC275T-64F200W DC	on request	PG-LQFP-176	-40°C – +125°C	0746 7072H	200	4	64 @ 500k	472	120	32	112	24	32	48	1 / 2	Yes	No	Yes	No
SAL-TC277TP-64F200N DC	on request	PG-LFBGA-292	-40°C – +150°C	4746 7172H	200	4	64 @ 500k	472	120	32	112	24	32	60	1 / 2	Yes	Yes	Yes	Yes
SAL-TC277T-64F200S DC	on request	PG-LFBGA-292	-40°C – +150°C	0746 7172H	200	4	64 @ 500k	472	120	32	112	24	32	60	1 / 2	Yes	No	Yes	No
SAL-TC275TP-64F200N DC	on request	PG-LQFP-176	-40°C – +150°C	4746 7072H	200	4	64 @ 500k	472	120	32	112	24	32	48	1 / 2	Yes	Yes	Yes	Yes
SAL-TC275TP-64F200W DC	on request	PG-LQFP-176	-40°C – +150°C	4746 7072H	200	4	64 @ 500k	472	120	32	112	24	32	48	1 / 2	Yes	Yes	Yes	No
SAL-TC270TP-64F200N DC	on request	Bare Die	-40°C – +170°C	4746 7F72H	200	4	64 @ 500k	472	120	32	112	24	32	60	1 / 2	Yes	Yes	Yes	Yes

1) STANDARD = serial production planned.
2) The address range starts at the lowest address defined in the User's Manual (See Memory Maps chapter).
3) Based on an EEPROM emulation algorithm with a wear levelling factor of 6 (size scales with number of program/erase cycles, for more details see User Manual).

Memory Maps of Variants

This section shows the influence of above feature variants on the memory map.

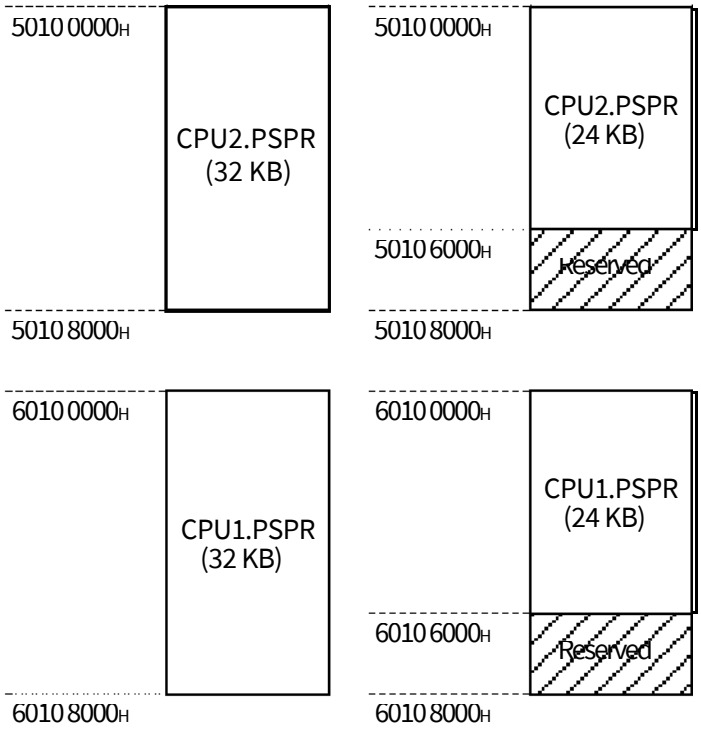
DF_EEPROM Variants: **384 KB**
Exemplary EEPROM size: 64 KB @ 500k

	Logical Sector	Size	Offset Address
AF00 0000H	EEPROM0	8 KB	00 0000H
	EEPROM1	8 KB	00 2000H
	EEPROM2	8 KB	00 4000H
	...	...	...
	EEPROM47	8 KB	05 E000H
AF06 0000H			

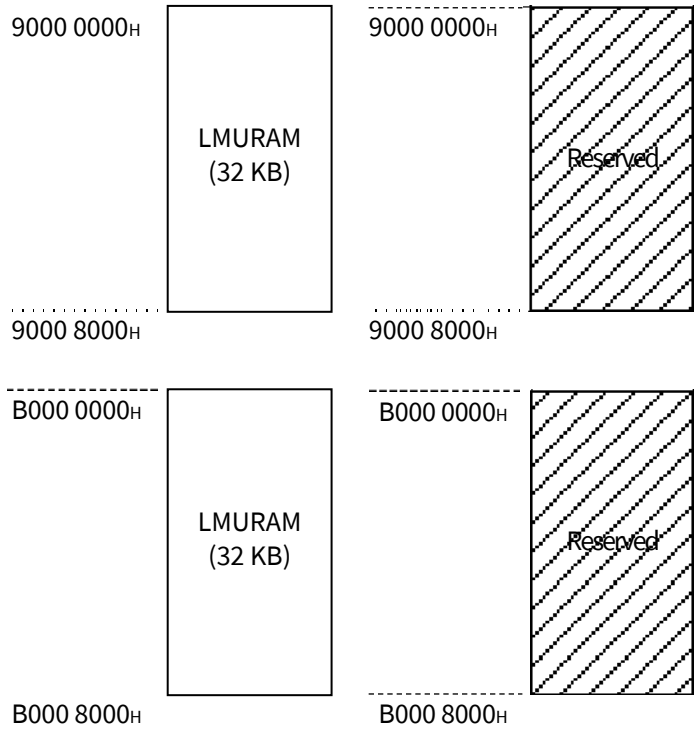
144 KB
24 KB @ 500k

	Logical Sector	Size	Offset Address
AF00 0000H	EEPROM0	8 KB	00 0000H
	EEPROM1	8 KB	00 2000H
	EEPROM2	8 KB	00 4000H
	...	...	...
	EEPROM17	8 KB	02 2000H
AF02 4000H	Reserved		
AF06 0000H			

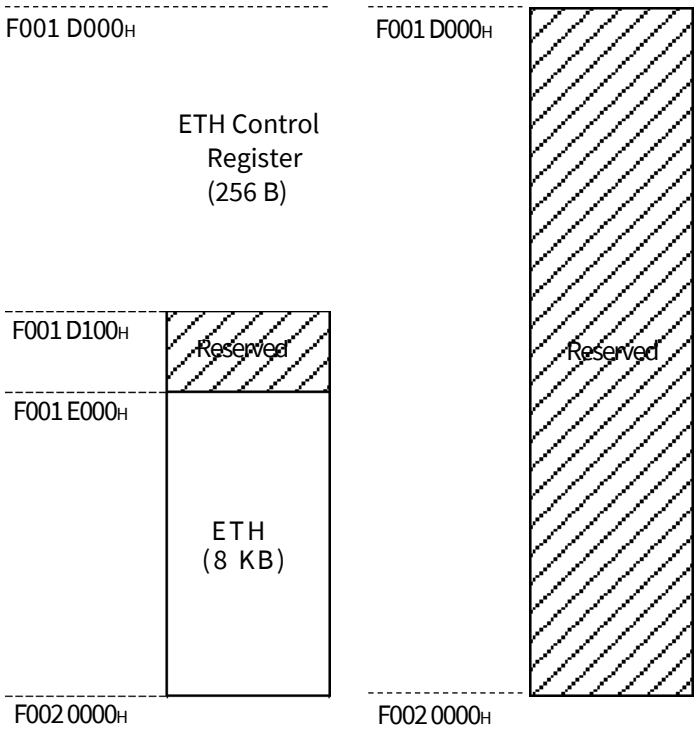
Core1/2 PSPR Variants: 32 KB **24 KB**



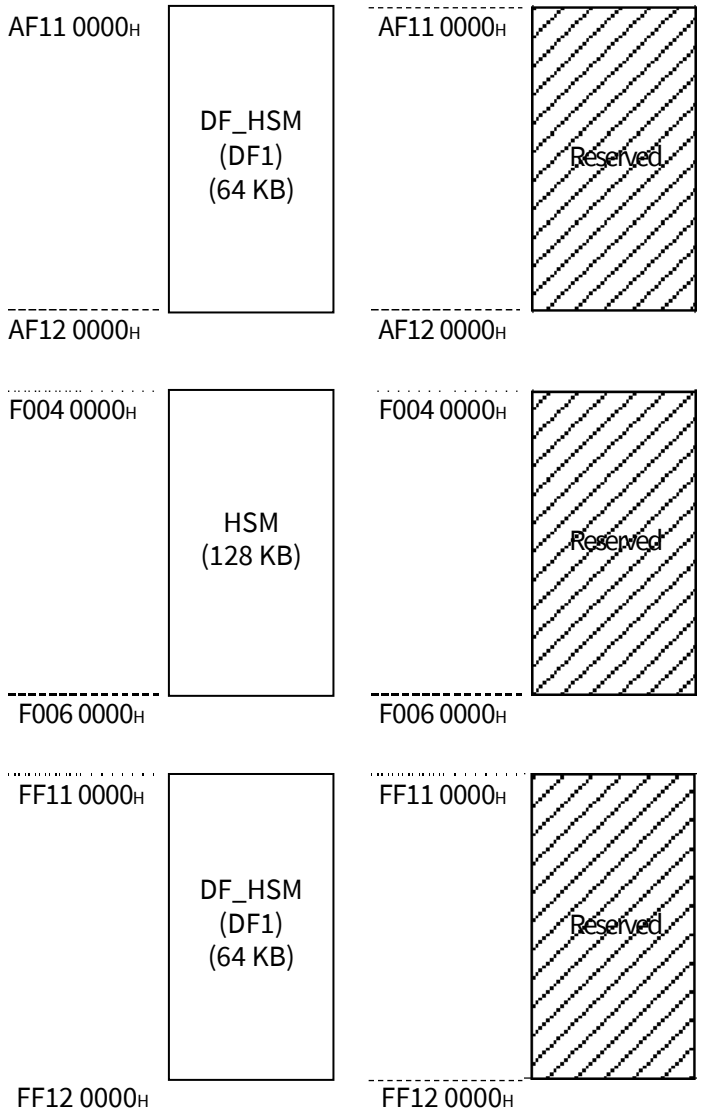
LMU Variants: **32 KB** **0 KB**



ETH Variants: **Yes** **Nc**



HSM Variants: **Yes** **No**



CAN FD Variants:

No influence on Memory Map.

CAN FD = “No” variants: all CAN register fields NCRx.FDEN have to be kept 0_B.

Revision History

Major changes since the last revision

Page or Reference	Description of change
V1.1	
5, 6	Chip IDs for CA & DC steps corrected Bugs in HSM (Y/N) and CAN FD (Y/N) corrected
V1.2	
	Memory maps added CAN FD DIS2015 markings added µCode 23_H ChipIDs added
V1.3	Memory maps corrections
V1.4	CAN FD Chip ID added Variant cleanup on older steps
V1.5	New CAN FD marking options added
V1.6	Navigation pane added to improve Ease of Use
V1.7	Alignment with Safety Documentation
V1.8	Corrections to the CA step table
V1.9	Package information updated
V1.10	Chip ID for SAK-TC277T-64F200S DB and SAL-TC277T-64F200S DB corrected

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Do you have a question about any aspect of this document?

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Document reference

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