DS90UR910QEVM User's Guide

User's Guide



Literature Number: SNLU143 September 2013

User's Guide SNLU143 – September 2013



The DS90UR910QEVM converts FPD-Link II to MIPI CSI-2. This kit will demonstrate the functionality and operation of the DS90UR910Q. The DS90UR910Q is an interface bridge chip that recovers data from the FPD-Link II serial bit stream and converts into a Camera Serial Interface (CSI-2) format compatible with Mobile Industry Processor Interface (MIPI) specifications. It recovers the 24- or 18-bit RGB data and 3 video sync-signals from the serial bit stream compatible to FPD-Link II serializers.

The recovered data is packetized and serialized over two data lanes strobed by a half-rate serial clock compliant with the MIPI DPHY / CSI-2 specifications, each running up to 900 Mbps. The FPD-Link II receiver supports pixel clocks of up to 75 MHz. The CSI-2 output serial bus greatly reduces the interconnect and signal count to a graphic processing unit (GPU) and eases system designs for video streams from multiple automotive driver assist cameras.

NOTE:	The demo board is not intended for EMI testing. The demo board was designed for
	easy accessibility to device pins with tap points for monitoring or applying signals,
	additional pads for termination, and multiple connector options.

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1 DS90UR910QEVM

The Texas Instruments DS90UR910QEVM evaluation module (EVM) helps system designers evaluate the operation and performance of the DS90UR910Q 10 - 75 MHz 24-bit Color FPD-Link II to CSI-2 Converter.

1.1 Features

- 10 75 MHz PCLK support (280 Mbps 2.10 Gbps FPD-Link II linerate)
- Compatible to DC balanced, AC coupled for FPD-Link II serial bit stream
- Capable to recover data up to 10 meters STP cable
- MIPI D-PHY modules conform to v1.00.00
- Compatible with MIPI CSI-2 Version 1.01
- Supports data rate up to 900Mbps per data lane, with two lanes
- Video stream packet formats: RGB888
- Continuous and Non-Continuous Clocking Mode
- Ultra low power, escape, high speed, and control modes support
- Integrated input terminations and adjustable receive equalization
- Fast random lock; no reference clock required
- CCI/I²C compatible control bus
- @Speed BIST and reporting pin
- Single +1.8V power supply
- 1.8V or 3.3V compatible LVCMOS I/O interface
- Automotive grade product: AEC-Q100 Grade 2 qualified
- 8 kV ISO 10605 ESD Rating

1.2 Ordering Information

Reference	DEVICE ID	DEVICE PACKAGE
U1	DS90UR910SQE	WQFN40

1.3 System Requirements

In order to demonstrate, the following is required:

- 1. FPD-Link II compatible Serializer
 - DS90UR905Q, DS90UR241Q, DS90C241Q, DS90UR907Q, DS99R421Q
 - DS90UH/UB/925/927Q FPD-Link III serializers in backward compatibility mode
- 2. Video source
- 3. Optional I²C controller
- 4. Power supply for 1.8V (required) and 3.3V (optional)

1.4 Contents of the Demo Evaluation Kit

• One EVM board with the DS90UR910Q

1.5 Applications Diagram

Figure 1 and Figure 2 below illustrate the use of the chipset in a display application.

DS90UR910QEVM



DS90UR910QEVM

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Figure 1. Applications Diagram

1.6 Typical Configuration





2 Quick Start Guide

- 1. Connect header JP3 to I²C host controller for register programming (optional)
- 2. Configure switches S1, S2 and S3 to set device's operating modes
- 3. Connect J1, J2 (RIN+, RIN-) to FPD-Link serial bit stream from an external DS90UR905, DS90Ux925, or compatible FPD-Link II serializer.
- 4. Connect CSI-2 output signals (J4-8, J10) to GPU
- 5. Provide power to board on VDD (1.8V), GND (Ground), and VDDIO (1.8V or 3.3V)
 - Optional +5VDC power supply on J11
- 6. Look for the LED D1 to light up on the board. If the LED is lit and stable, then the DS90UR910Q is LOCKED to the FPD-Link II serial stream. LED D2 will be lit when a valid display timing is detected.
- 7. For details of pin-names and pin-functions, please refer to the DS90UR910 datasheet



Figure 3. Evaluation Board Connections

2.1 Demo Board Connections

Table 1. Power Supply Connection

Reference	Signal	Description	
P4	VDDIO	1.8V ±5% OR 3.3V ±10%	
P5	GND	Ground	
P6	VDD	1.8V ±5%	
J11 (Optional) +5V		Single main +5V (0.5A) power connector that supplies power to the entire board. Short jumpers JP7 and JP6 for 1.8V and 3.3V on board regulator power supplies respectively.	

Table 2. CSI-2 Output Signals

Reference	Signal	Description	
J4	DATA1+	Non-inverting data output of DPHY Lane 1	
J5	DATA1-	Inverting data output of DPHY Lane 1	
J6	DATA0+	Non-inverting data output of DPHY Lane 0	
J7	DATA0-	Inverting data output of DPHY Lane 0	
J8	CLK+	Non-inverting half-rate DPHY clock lane	
J10	CLK-	Inverting half-rate DPHY clock lane	

Table 3. FPD-Link II Input Signal

Reference	Signal	Description
J1	RIN+	SMA connector
J2	RIN-	SMA connector
P1 (Optional) RIN+/-		HSD connector Populate C17 and C18 to use P1 connector.

Table 4. I²C/CCI Interface Header

Reference	Signal	Description
JP3.1	VDDI2C	I ² C/CCI VDDIO
JP3.2	SCL	I ² C/CCI SCL
JP3.3	SDA	I ² C/CCI SDA
JP3.4	GND	Ground

Table 5. Control Status

Reference	Signal	Description
JP4.1	LOCK	LOCK = 1, PLL acquired lock to the reference clock input LOCK = 0, PLL is unlocked
JP4.3	PASS	PASS = 1: No fault detected on input display timing. PASS = 0: Indicates an error condition or corruption in display video timing.
JP4.5	GPIO	General Purpose I/O

Table 6. CMLOUT Output Signals

Reference	Signal	Description
J3	CMLOUT+	SMA connector
J9	CMLOUT-	SMA connector



Reference	Signal	Description		
		Receive	r Equalization Configuration	
SO 1	EQ1		EQ[3:1]	EQ Boost
32.1	EQT		001	~3 dB
			010	~4.5 dB
	EQ2		011	~6 dB
\$2.2			100	~7.5 dB
			101	~9 dB
	2.3 EQ3		110	~10.5 dB
S2.3			111	~12 dB
			000	OFF* (Default)

Table 7. EQ Setting SW-DIP3 – S2

Table 8. Config/ID Setting SW-DIP4 - S1

Reference	Signal	Description				
		Config	Configuration Modes			
S1.1	CONFIG0		CONFIG1	CONFIG0	MODE	
			L (Default)	L (Default)	DS90UR905Q/907Q, DS90Ux925Q	
			L	Н	DS90UR905Q/907Q, DS90Ux925Q	
S1.2	1.2 CONFIG1		Н	L	DS90UR241Q, DS99R421Q	
			Н	Н	DS90C241Q	
		CCI/I	2C Slave Address S	elect		
S1.3	ID0		ID1	ID0	SLAVE ADDRESS	
			L (Default)	L (Default)	0x3C'h (0x78'h<<1)	
			L	н	0x3D'h (0x7A'h<<1)	
S1.4	ID1		Н	L	0x36'h (0x6C'h<<1)	
			Н	Н	0x37'h (0x6E'h<<1)	

Table 9. BISTEN/PDN Setting SW-DIP2 - S3

Reference	Signal	Input = L	Input = H	Description
S3.1	BISTEN	Normal operating mode. BIST is disabled (Default)	BIST Mode is enabled.	BIST Enable Input
\$3.2	PDN	Power Down (Disabled)	Operational (Default)	Power Down Mode Input



2.2 Typical Connection and Test Equipment

The following is a list of typical test equipment that may be used to generate signals for the Serializer inputs or video data/controls:

- 1. Digital Video Source for generation of specific display timing such as Digital Video Processor or Graphics Controller (GPU) with digital RGB (1.8V/3.3V LVCMOS) output.
- Any other signal generator / video source This video generator may be used for video signal sources for 6/8-bit Digital 1.8V/3.3V LVCMOS/RGB
- 3. Any other signal / video generator that generates the correct input levels as specified in the datasheet.
- 4. Programming the DS90Ux925Q to use the internal pattern generation feature. For detailed information, refer to SNLA132.

The following is a list of typical test equipment that may be used to monitor the MIPI CSI-2 signals from the DS90UR910Q:

- 1. Logic Analyzer
 - Agilent Protocol Analyzer and Exerciser for MIPI D-PHY Interfaces
 - Agilent Logic Analyzer with MIPI CSI2 software loaded
 - Agilent N4851A/B MIPI Analyzer
 - Agilent E5381A Differential Flying Lead Set Probe
- Any SCOPE with a bandwidth of at least 75MHz for 1.8V/3.3V LVCMOS and/or 1.5GHz for observing differential signals.
- 3. UNH-IOL MIPI D-PHY Reference Termination Board (RTB)
- 4. UNH-IOL MIPI D-PHY/CSI/DSI Probing Board
- 5. UNH-IOL CSIGUI Tool

Figure 4 below shows a typical test set up using a Graphics Controller and display.



Video Processor Board



Figure 5 below shows a typical test set up using a video generator and logic analyzer.



Figure 5. Typical Test Setup for Evaluation



2.3 CSI-2 Interface

The DS90UR910Q (in default mode) takes the RGB data bits R[7:0], G[7:0] and B[7:0] defined in the 24bit serializer pinout and directly maps to the RGB888 color space in the data frame. The DS90UR910Q follows the General Frame Format as described in the CSI-2 standard.

Valid video signals and display timing (DE, VS, and HS) is required in order for the DS90UR910Q CSI-2 interface to operate. Upon the end of the vertical sync pulse (VS), the DS90UR910Q generates the Frame End and Frame Start synchronization packets within the vertical blanking period. The timing of the Frame Start will not reflect the timing of the VS signal. Upon the rising edge of the DE signal, each active line is output in a long data packet with the RGB888 data format. At the end of each packet, the data lanes DATA0± and DATA1± return to the LP-11 state, while the clock lane CLK± continue outputting the high speed clock.

2.4 Terminal Device

A termination device is required in order to properly monitor and measure the transmission of the CSI-2 signals. The termination device should support the change of signals as it switches between LP and HS modes. This can be provided by either a CSI-2 receiver or a dedicated dynamic termination board. The recommended termination board is the UNH-IOL MIPI D-PHY Reference Termination Board (RTB).

2.5 CMLOUT Outputs for Eye Monitor

Connector J3 connects to CMLOUT+ and J9 connects to CMLOUT-, which are present on left side of DS90UR910Q Evaluation board. CMLOUT+/- must be enabled by register, 0x04[7] = 1, to be able to monitor the FPD-Link II serial stream.

3 References

Note: Please note that the following references are supplied only as a courtesy to our valued customers. It is not intended to be an endorsement of any particular equipment or supplier.

3.1 Equipment References

Digital Video Pattern Generator:

Astrodesign - www.astro-americas.com

Logic Analyzer:

Agilent Technologies Inc - www.agilent.com

MIPI Test Fixtures:

University of New Hampshire InterOperability Laboratory (UNH-IOL) – *www.iol.unh.edu/services/testing/mipi/fixtures.php*

I²C Adapters:

Corelis CAS-1000-I2C/E I2C Bus Analyzer and Exerciser - www.corelis.com/products/I2C-Analyzer.htm

Aardvark I2C/SPI Host Adapter Part Number: TP240141 - www.totalphase.com/products/aardvark_i2cspi

3.2 Cable References

For optimal performance, we recommend Shielded Twisted Pair (STP) 100ohm differential impedance and 24 AWG (or larger diameter) cable for high-speed data applications.

Leoni Dacar 538 series cable – www.leoni-automotive-cables.com

Rosenberger HSD connector - www.rosenberger.de/en/Products/35_Automotive_HSD.php

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References

4 Bill of Materials for DS90UR910QEVM:

ltem	Qty	Reference	Value	Manufacture PN	Vendor	Description
1	22	C1,C2,C5,C6, C9,C11,C12,C 15,C19,C20,C 21,C23,C24,C 25,C26,C27,C 28,C29,C30,C 31,C39,C41	0.1UF	GRM155R71C104K A88D	Murata	CAP CER 0.1UF 16V 10% X7R 0402
2	5	C3,C4,C16,C3 2,C40	10UF	LMK107BJ106MAL TD	Taiyo Yuden	CAP CER 10UF 10V 20% X5R 0603
3	6	C7,C8,C10,C1 3,C14,C42	2.2UF	JMK105BJ225MV-F	Taiyo Yuden	CAP CER 2.2UF 6.3V 20% X5R 0402
4	0	C17,C18	NO STUFF	GRM155R71C104K A88D	Murata	CAP CER 0.1UF 16V 10% X7R 0402
5	1	C22	4.7UF	CGB3B1X5R1A475 M055AC	TDK	CAP CER 4.7UF 10V 20% X5R 0603
6	2	C33,C36	C_X7R_22UF_1 210	C3225X7R1A226K2 30AC	TDK	CAP CER 22UF 10V 10% X7R 1210
7	2	C34,C37	10UF	EMK212BJ106KG-T	Taiyo Yuden	CAP CER 10UF 16V 10% X5R 0805
8	2	C35,C38	10UF	EMK107BBJ106MA- T	Taiyo Yuden	CAP CER 10UF 16V 20% X5R 0603
9	2	D1,D2	LED	LTST-C191KGKT	Lite-On Inc	LED GREEN CLEAR THIN 0603 SMD.
10	1	JP3	HEADER 4	68001-204HLF	FCI	CONN HEADER 4POS .100"
11	1	JP4	HDR_3X2	68602-206HLF	FCI	CONN HEADER 6POS .100"
12	2	JP6,JP7	HDR_2	68001-202HLF	FCI	BERGSTIK II .100
13	10	J1,J2,J3,J4,J5, J6,J7,J8,J9,J1 0	SMA_142_0701 _851	142-0701-851	Emerson	CONN JACK END LAUNCH PC GOLD SMA
14	1	J11	CONN JACK PWR	RAPC712X	Switchcraft Inc.	CONN POWERJACK MINI R/A PCMT
15	1	P1	ROSENBERGE R_HSD_CON	D4S20D-40ML5-Y	Rosenberger	Male Right angle SMD
16	3	P4,P5,P6	TERMINAL-PS	108-0740-001	Emerson	CONN JACK BANANA UNINS PANEL MOU
17	7	R1,R2,R3,R4, R5,R9,R24	0	RC0402JR-070RL	Yageo	RES 0.0 OHM 1/16W 0402 SMD
18	2	R6,R7	49.9	ERJ-2RKF49R9X	Panasonic	RES 49.9 OHM 1/10W 1% 0402 SMD
19	1	R8	0	RC0402JR-070RL	Yageo	RES 0.0 OHM 1/16W 0402 SMD
20	9	R11,R26,R27, R28,R29,R30, R31,R32,R33	10K	ERJ-3EKF1002V	Panasonic	RES 10.0K OHM 1/10W 1% 0603 SMD
21	1	R12	150	ERJ-2RKF1500X	Panasonic	RES 150 OHM 1/10W 1% 0402 SMD
22	1	R13	150	ERJ-2RKF1500X	Panasonic	RES 150 OHM 1/10W 1% 0402 SMD
23	2	R14,R15	4.7K	ERJ-2RKF4701X	Panasonic	RES 4.70K OHM 1/10W 1% 0402 SMD
24	3	R16,R18,R22	10K	ERJ-3EKF1002V	Panasonic	RES 10.0K OHM 1/10W 1% 0603 SMD
25	0	R17,R21	NOSTUFF			
26	1	R19	16.5K	ERJ-3EKF1652V	Panasonic	RES 16.5K OHM 1/10W 1% 0603 SMD

Table 10. DS90UR910QEVM BOM

					•	•
ltem	Qty	Reference	Value	Manufacture PN	Vendor	Description
27	1	R20	10K	ERJ-3EKF1002V	Panasonic	RES 10.0K OHM 1/10W 1% 0603 SMD
28	1	R23	4.52K	ERJ-3EKF4531V	Panasonic	RES 4.53K OHM 1/10W 1% 0603 SMD
29	1	R25	100	ERJ-2RKF1000X	Panasonic	RES 100 OHM 1/10W 1% 0402 SMD
30	0	R34,R35,R36, R37,R38,R39	0_DNL	RC0201FR-070RL	Yageo	RES 0.0 OHM 1/20W 0201 SMD
31	1	S1	SW DIP-4	78B04ST	Grayhill	SWITCH DIP EXTENDED SEALED 4POS
32	1	S2	SW DIP-3	78B03ST	Grayhill	SWITCH DIP EXTENDED SEALED 3POS
33	1	S3	78B02ST	78B02ST	Grayhill Inc	SWITCH DIP EXTENDED SEALED 2POS
34	1	U1	DS90UR910Q	DS90UR910QSQE/ NOPB	ТІ	IC SERIALIZER FPD-CSI2 48WQFN
35	2	U2,U3	LP38693MP- ADJ	LP38693MP- ADJ/NOPB	ТІ	IC REG LDO ADJ .5A SOT223-4
36	1	DS90UR910Q EVM PCB	SV600551-001	PCB board		

Table 10. DS90UR910QEVM BOM (continued)



Schematic for DS90UR910QEVM:

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5 Schematic for DS90UR910QEVM:









6 EVM Layout



П

TEXAS INSTRUMENTS				
NAME:DS90UR910Q EVM				
DATE:JULY 2013	JOB: 305-PD-12-0905	Rev.2		
LAYER: TOP				



TEXAS INSTRUMENTS				
NAME:DS90UR910Q EVM				
DATE:JULY 2013	JOB: 305-PD-12-0905	Rev.2		
LAYER : BOTTOM				



TEXAS INSTRUMEN	ſS	
NAME:DS90UR910Q	EVM	
DATE:JULY 2013	JOB:305-PD-12-0905	Rev.2
LAYER : GND		

TEXAS INSTRUMENTS				
NAME:DS90UR910Q	NAME:DS90UR910Q EVM			
DATE:JULY 2013	JOB: 305-PD-12-0905	Rev.2		
LAYER: PWR				





	14 DATA1+ 22 - - - - - - - - - - - - - - - - - -
יי ערגאנאשבאנג גוא+ יי גנא גדיי גוא- גוא- וא- גוא- סוגסטד+	J45 DATA0+ 200 200 DATA0- J7 J8 CLK+
101 H 102 T 101 101 H 102 H 102 101 102 H 102 102 101 102 102 102 102 101 102 102 102 102 101 102 102 102 102 101 102 102 102 102 101 102 102 102 102 101 102 102 102 102 101 102 102 102 102	е - - - - - - - - - - - - - - - - - - -

TEXAS INSTRUMENTS				
NAME:DS90UR910Q EVM				
DATE:JULY 2013	JOB:305-PD-12-0905	Rev.2		
LAYER: TOP_ASY				



TEXAS INSTRUMENTS					
NAME:DS90UR910Q EVM					
DATE:JULY 2013	JOB: 305-PD-12-0905	R e v . 2			
LAYER: BOTTOM_ASSY					

TEXAS INSTRUMENTS					
NAME:DS90UR910Q EVM					
DATE:JULY 2013	JOB:305-PD-12-0905	Rev.2			
AYER: TOP SILK					



TEXAS INSTRUMENTS					
NAME:DS90UR910Q EVM					
DATE: JULY 2013 JOB: 305-PD-12-0905 Rev.2					
LAYER: BOTTOM SILK					

EVM Layout

7 EVM PCB Stackup



Figure 6. Board Stackup

STANDARD TERMS AND CONDITIONS FOR EVALUATION MODULES

- 1. Delivery: TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, or documentation (collectively, an "EVM" or "EVMs") to the User ("User") in accordance with the terms and conditions set forth herein. Acceptance of the EVM is expressly subject to the following terms and conditions.
 - 1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM ("Software") shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms and conditions that accompany such Software
 - 1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.
- 2 Limited Warranty and Related Remedies/Disclaimers:
 - 2.1 These terms and conditions do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.
 - 2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for any defects that are caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI. Moreover, TI shall not be liable for any defects that result from User's design, specifications or instructions for such EVMs. Testing and other quality control techniques are used to the extent TI deems necessary or as mandated by government requirements. TI does not test all parameters of each EVM.
 - 2.3 If any EVM fails to conform to the warranty set forth above, TI's sole liability shall be at its option to repair or replace such EVM, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.
- 3 Regulatory Notices:
 - 3.1 United States
 - 3.1.1 Notice applicable to EVMs not FCC-Approved:

This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

3.2 Canada

3.2.1 For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 Japan

- 3.3.1 Notice for EVMs delivered in Japan: Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に 輸入される評価用キット、ボードについては、次のところをご覧ください。 http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page
- 3.3.2 Notice for Users of EVMs Considered "Radio Frequency Products" in Japan: EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required by Radio Law of Japan to follow the instructions below with respect to EVMs:

- 1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
- 2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
- 3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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- 3.3.3 Notice for EVMs for Power Line Communication: Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page 電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page
- 4 EVM Use Restrictions and Warnings:
 - 4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.
 - 4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.
 - 4.3 Safety-Related Warnings and Restrictions:
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 - 4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.
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