Design Guide: TIDA-010054

Bi-Directional, Dual Active Bridge Reference Design for Level 3 Electric Vehicle Charging Stations

Description

This reference design provides an overview on the implementation of a single-phase Dual Active Bridge (DAB) DC-DC converter. DAB topology offers advantages like soft-switching commutations, a decreased number of devices and high efficiency. The design is beneficial where power density, cost, weight, galvanic isolation, high voltage conversion ratio and reliability are critical factors, making it ideal for EV charging stations and energy storage applications. Modularity and symmetrical structure in DAB allow for stacking converters to achieve high power throughput and facilitate a bidirectional mode of operation to support battery charging and discharging applications.

Resources

TIDA-010054	Design Folder
UCC21530, AMC1311	Product Folder
AMC1302, AMC1306M05	Product Folder
TPS82130, ISO7721	Product Folder
TPS763, TPS7B69	Product Folder
OPA320, REF2033	Product Folder
SN6501, SN6505B	Product Folder
TL431, SN74LVC2G34	Product Folder
TMS320F280049	Product Folder

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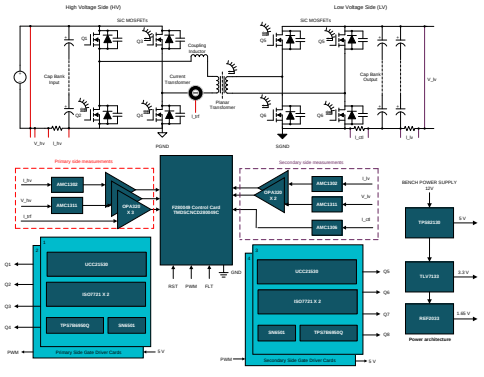
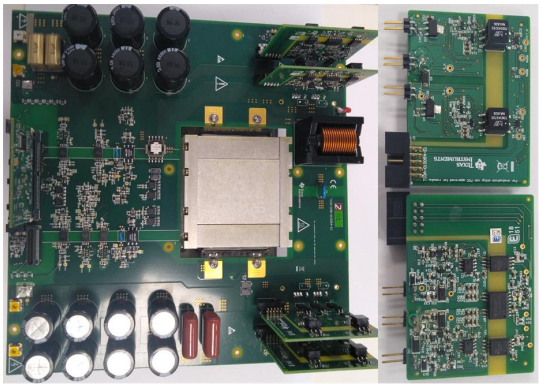
Features

- Single-phase-shift, DAB
- Dual-channel UCC21530 with reinforced isolation used for driving SiC MOSFETs in the half-bridge configuration
- TMS320F280049 controller for implementation of digital control
- Isolated voltage and current sensing
- Maximum power output of 10 kW
- Full load efficiency of 97.6% and a peak efficiency of 98.2% at 6 KW
- High-power density of 1.92 KW/L
- Primary voltage of 700-800-V DC, secondary voltage of 380-500-V DC
- Two-level turnoff for short-circuit protection with adjustable current limit and delay (blanking) time
- PWM switching frequency of 100 kHz and reduced transformer size enabled by planar magnetics
- Soft switching without auxiliary components

Applications

- DC charging (pile) station
- EV charging station power module
- Energy storage power conversion system (PCS)
- On-board (OBC) & wireless charger





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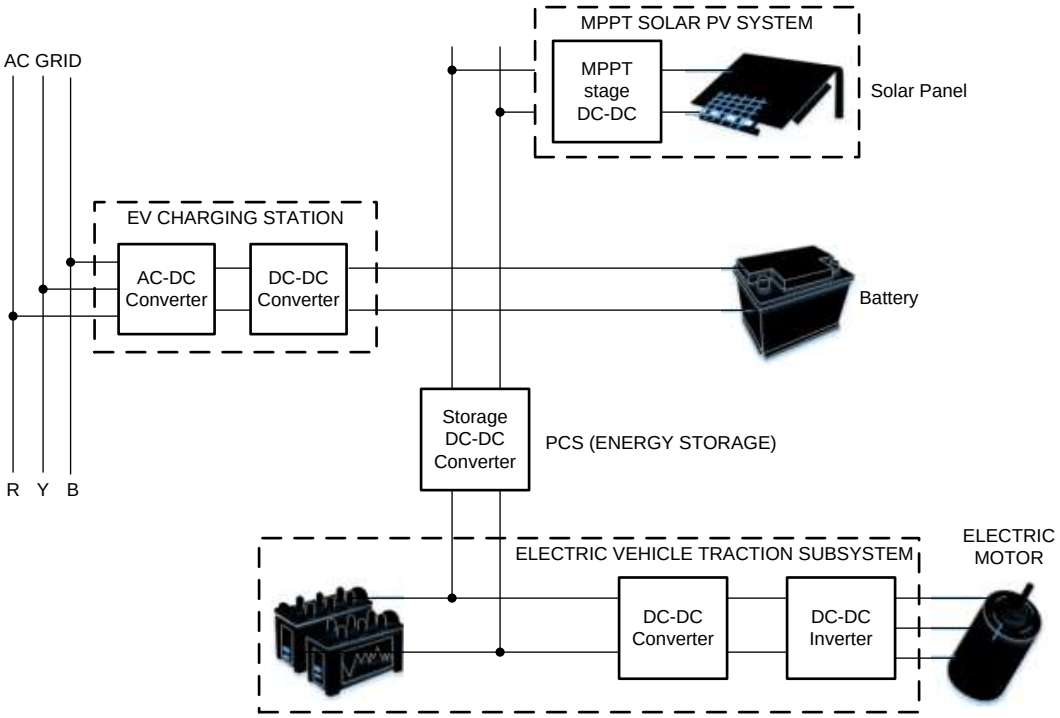
1 System Description

The electric vehicle charging standards governed by the Combined Charging System (CCS) and CHAdeMO® are constantly changing and are pushing for faster battery charging rates requiring typically less than 30 minutes spent at a charging station for one full charge of an electric vehicle. The DC charging station is typically a Level 3 charger which can cater to a very high power level between 120-240 KW. These DC charging stations are standalone units which house AC/DC and DC/DC power conversion stages. A number of power conversion modules are stacked together inside of a charging station to increase the power levels and enable fast charging. DC fast-charging stations provide a high power DC current to an electric vehicle's battery without passing through any onboard AC/DC converter, which means the current is connected directly to the battery. Most cars on the road today can handle only up to 50 KW. Newer cars will have the ability to charge at greater rates of power. As EVs come with higher range and batteries get bigger, DC charging solutions are being developed to support long-range EV batteries through fast charging stations up to 120 kW or more.

The DC/DC converter in a charging station must be capable of interfacing with the rectified bus voltage (700-800 V) from a three-phase Vienna rectifier at its input and connect with the battery of an electric vehicle at its output, delivering rated power. The DC/DC converter finds important application in a number of end equipment. Figure 1 shows its use in charging stations, solar photovoltaic systems, energy storage systems, and electric vehicle traction applications.

Figure 1. Role of DC/DC Converter



The DC/DC converter must be capable of handling high power levels. In addition to this, the converter must be modular, which enables single power stage converter units to be paralleled, whereby the output power throughput can be scaled to higher levels as required by DC charging station standards. Current trends in the charging station are moving toward converters that can handle bidirectional power flow. New practices, such as Vehicle-to-Grid (V2G), involve power transfer between the battery of an electric vehicle and the AC grid. Bidirectional DC/DC converters enable charging of the battery in the forward mode of operation and facilitate flow of power back to the grid from the battery during reverse mode of operation, which can be used to stabilize the grid during peak load periods.

Power density and system efficiency are two important requirements of a converter in a DC charging station. Operating at high switching frequencies enables reduced size of magnetics. By moving to higher bus voltage to facilitate fast charging, more power can be transferred at the same current level. This helps to reduce the amount of copper, thereby improving power density of the converter. The converter must also be highly efficient as it results in significant cost savings and reduced thermal solution. This reduced thermal solution directly translates into reduced and compact heat sink size, which in turn increases the power density of the converter. It must also be capable of inherent soft switching like ZVS (Zero Voltage Switching) and ZCS (Zero Current Switching) without the addition any bulky passive components which might hamper power density.

The DC/DC converter must be capable of interfacing seamlessly with Lithium ion or a lead acid battery, which are predominantly used in EV charging stations. It must also be capable of providing the required voltage conversion between the high-voltage and low-voltage side and provide galvanic isolation between them.

Traditional switching devices have a limit on how quickly they can switch high voltages, or more appropriately, the dV/dt ability of the device. This slow ramping process increases switching loss because the device spends more time in switching transition. This increased switch time also increases the amount of dead time required in the control system to prevent shoot-through and shorts. The solution to this has been developed in newer switching semiconductor technology such as SiC and GaN devices with high electron mobility. This reference design uses SiC MOSFETs alongside TI's SiC gate driver technology to demonstrate the potential benefits it translates when it comes to efficiency and power density.

The following four popular topologies were considered for analysis.

- LLC resonant converter
- Phase-shifted, full bridge
- Single-phase, dual-active bridge
- Dual-active bridge in CLLC mode

Based on this study, the dual-active bridge was chosen for implementation in this reference design, owing to its ease of bidirectional operation, modular structure, competitive efficiency, and power density numbers with respect to other competing topologies. This reference design focuses on addressing the challenges when designing a high-power, dual-active-bridge DC/DC converter for the EV charging station.

1.1 Key System Specifications

Table 1 lists some of the critical design specifications of the dual-active-bridge (DAB) DC/DC converter. The system has a full load efficiency of 97.6% at an output power of 10 KW.

Table 1. Key System Specifications

PARAMETER	SPECIFICATIONS	DETAILS
Input voltage range	700-800-V DC	Section 3.1
Output voltage range	380-500-V DC	Section 3.1
Output power rating	10-KW maximum	Section 2.3.5
Output current	26-A maximum	Section 2.3.5
Efficiency	Peak 98.2% (at 6.6 KW) full load 97.6% (at 10 KW)	Section 4.2.2
PWM switching frequency	100 kHz	Section 2.3.4.6
Power density	>1 KW/L	Section 4.2.2
Voltage ripple	<5 %	Section 2.3.4.4

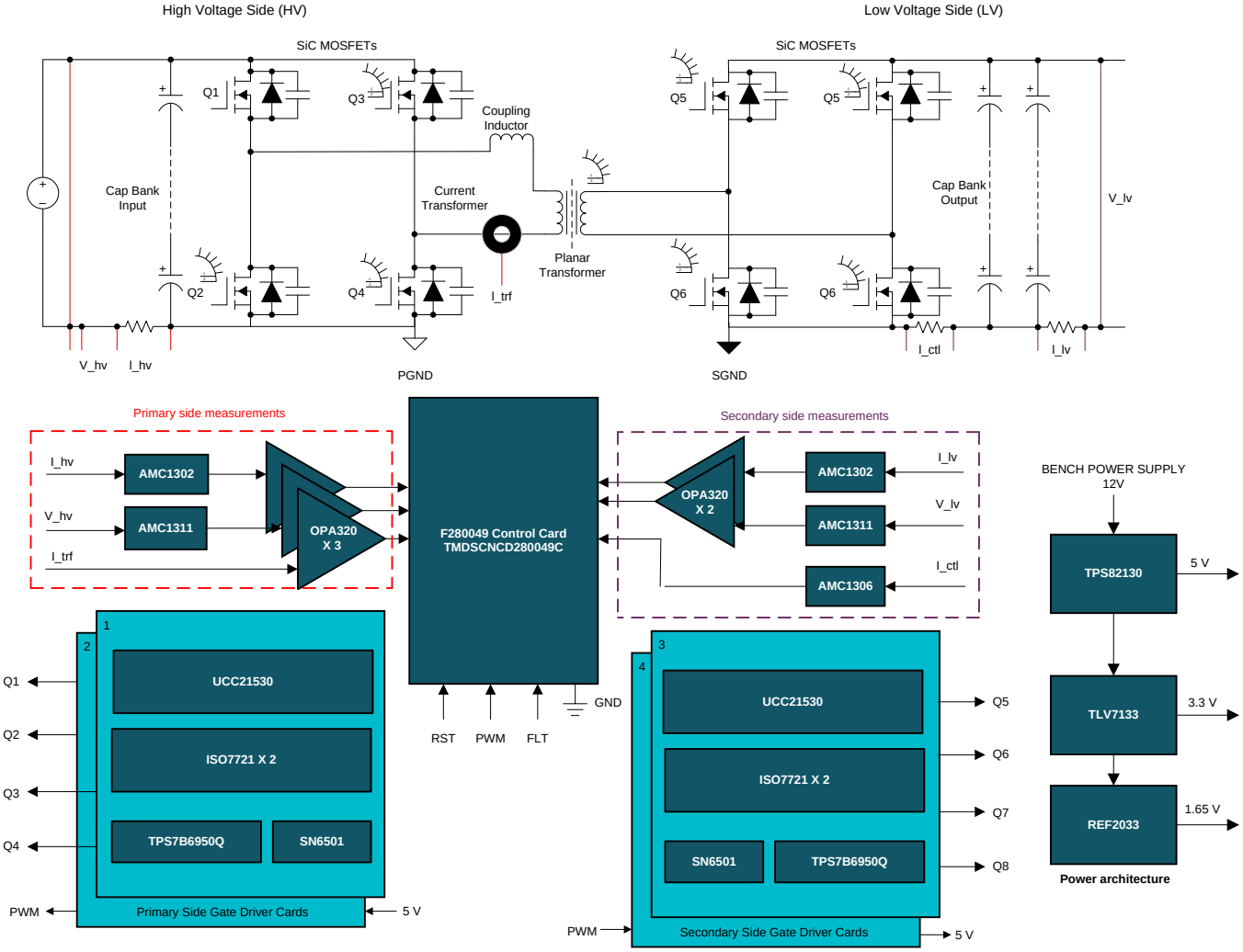
Table 1 shows that the input voltage range is between 700 V and 800 V. This range was considered because the DC/DC converter must interface with the front-end Vienna rectifier and the three-phase power factor correction (PFC), which has an output that is within this range. This converter can also be used in conjunction with single-phase PFC systems with an output that is in the range of 400 V, which must interface with 48- and 72-V batteries.

2 System Overview

This section shows the block diagram of the dual-active-bridge DC/DC converter.

2.1 Block Diagram

Figure 2. TIDA-010054 Block Diagram



This reference design consists of three main sections that intercommunicate:

- A power board comprising the power stage SiC MOSFETs, a high frequency transformer, current and voltage sensing electronics, and the system power tree
- A TMDSCNCD280049C control card to support digital control
- Four gate driver cards, each having a UCC21530 to drive the four legs of the DC/DC converter

2.2 Highlighted Products

This section highlights the critical components of the design which include the gate driver, F280049 controller, isolated amplifiers for current and voltage sensing, and generating voltage references.

2.2.1 UCC21530

The UCC21530 is used for driving the SiC MOSFETs of the power stage. It is an isolated dual-channel gate driver with 4-A source and 6-A sink peak current. It is designed to drive IGBTs and SiC MOSFETs up to 5-MHz with best-in-class propagation delay of 19-ns and pulse-width distortion of 5-ns. The input side is isolated from the two output drivers by a 5.7-kVRMS reinforced isolation barrier, with a minimum of 100-V/ns common-mode transient immunity (CMTI). Internal functional isolation between the two secondary-side drivers allows a working voltage of up to 1850 V. The device accepts VDD supply voltages up to 25 V. A wide input VCCI range from 3 V to 18 V makes the driver suitable for interfacing with both analog and digital controllers.

For more details on this device, see the UCC21530 product page.

2.2.2 AMC1311

The AMC1311 is used for DC voltage sensing at the input and output terminals. It is a precision, isolated amplifier with an output separated from the input circuitry by an isolation barrier that is highly resistant to magnetic interference. This barrier is certified to provide reinforced galvanic isolation of up to 7 kV peak according to VDE V 0884-1 and UL1577. The high-impedance input of the AMC1311 is optimized for connection to high-voltage resistive dividers or other voltage signal sources with high output resistance. The excellent performance of the device supports accurate, low temperature drift voltage or temperature sensing and control in closed-loop systems.

For more details on this device, see the AMC1311 product page.

2.2.3 AMC1302

The AMC1302 is used in the signal chain path for measuring the current in the input and output terminals. It is a precision isolated amplifier with a capacitive isolation barrier that has high immunity to magnetic interference. This barrier provides reinforced isolation of 5 kVRMS (maximum) with a very long lifetime and low power dissipation. When used with isolated power supplies, this device isolates components that operate on different common-mode voltage levels. The input of the AMC1302 is optimized for direct connection to shunt resistors or other low voltage-level signal sources. The ±50-mV input voltage range allows significant reduction of the power dissipation through the shunt. Additionally, the low high-side supply current and voltage of the AMC1302 allow use of low-cost isolated power-supply solutions. The performance of the device supports accurate current control resulting in system-level power savings and in low torque ripple that is particularly important in motor control applications.

For more details on this device, see the AMC1302 product page.

2.2.4 AMC1306M05

The AMC1306 is a precision, delta-sigma ($\Delta\Sigma$) modulator with the output separated from the input circuitry by a capacitive double isolation barrier that is highly resistant to magnetic interference. This barrier is certified to provide reinforced isolation of up to 7000 VPEAK according to the UL1577 standards. The input of the AMC1306 is optimized for direct connection to shunt resistors and the unique low input voltage range of the ±50-mV device allows significant reduction of the power dissipation through the shunt and supports excellent ac and dc performance. The output bit stream of the AMC1306 is Manchester coded (AMC1306Ex) or uncoded (AMC1306Mx), depending on the derivate. By using an integrated digital filter (such as those in the TMS320F2807x orTMS320F2837x microcontroller families) to decimate the bit stream, the device can achieve 16 bits of resolution with a dynamic range of 85 dB at a data rate of 78 kSPS.

For more details on this device, refer the AMC1306M05 product page.

2.2.5 TPS82130

The TPS82130 is a 17-V input 3-A step-down converter power module optimized for small solution size and high efficiency. The module integrates a synchronous step-down converter and an inductor to simplify design, reduce external components and save PCB area. To maximize efficiency, the converter operates in PWM mode with a nominal switching frequency of 2 MHz and automatically enters power save mode operation at light load currents. Using the DCS-Control™ topology, the device achieves excellent load transient performance and accurate output voltage regulation.

For more details on this device, refer the TPS82130 product page.

2.2.6 OPA320

The OPA320 (single) and OPA2320 (dual) are a new generation of precision, low-voltage CMOS operational amplifiers optimized for very low noise and wide bandwidth while operating on a low quiescent current of only 1.45 mA. The OPA320 series is ideal for low-power, single- supply applications. Low-noise (7 nV/√Hz) and high- speed operation also make them well-suited for driving sampling analog-to-digital converters (ADCs). Other applications include signal conditioning and sensor amplification. The OPA320 features a linear input stage with zero- crossover distortion that delivers excellent common- mode rejection ratio (CMRR) of typically 114 dB over the full input range.

For more details on this device, refer the OPA320 product page.

2.2.7 ISO7721

The ISO772x devices are high-performance, dual-channel digital isolators with 5000 Vrms (DW and DWV packages) and 3000 Vrms(D package) isolation ratings per UL 1577. The ISO772x devices provide high electromagnetic immunity and low emissions at low power consumption, while isolating CMOS or LVCMOS digital I/Os. Each isolation channel has a logic input and output buffer separated by a double capacitive silicon dioxide (SiO2) insulation barrier. They support up to 100 Mbps data rate and have low propagation delay 11-ns.

For more details on this device, refer the ISO7721 product page.

2.2.8 SN6501

The SN6501 is a monolithic oscillator/power-driver, specifically designed for small form factor, isolated power supplies in isolated interface applications. The device drives a low-profile, center-tapped transformer primary from a 3.3-V or 5-V DC power supply. The secondary can be wound to provide any isolated voltage based on transformer turns ratio. The SN6501 consists of an oscillator followed by a gate drive circuit that provides the complementary output signals to drive the ground referenced N-channel power switches. The internal logic ensures break-before-make action between the two switches.

For more details on this device, refer the SN6501 product page.

2.2.9 SN6505B

The SN6505x is a low-noise, low-EMI push-pull transformer driver, specifically designed for small form factor, isolated power supplies. It drives low-profile, center-tapped transformers from a 2.25 V to 5 V DC power supply. Ultra-low noise and EMI are achieved by slew rate control of the output switch voltage and through Spread Spectrum Clocking (SSC). The SN6505x consists of an oscillator followed by a gate drive circuit that provides the complementary output signals to drive ground-referenced N-channel power switches. The device includes two 1-A Power-MOSFET switches to ensure start-up under heavy loads. The switching clock can also be provided externally for accurate placement of switcher harmonics, or when operating with multiple transformer drivers. The internal protection features include a 1.7 A current limiting, under-voltage lockout, thermal shutdown, and break-before-make circuitry. SN6505x includes a soft-start feature that prevents high inrush current during power up with large load capacitors.

For more details on this device, refer the SN6505B product page.

2.2.10 TMP235

The TMP23x devices are a family of precision CMOS integrated-circuit linear analog temperature sensors with an output voltage proportional to temperature engineers can use in multiple analog temperature-sensing applications. These temperature sensors are more accurate than similar pin-compatible devices on the market, featuring typical accuracy from 0°C to +70°C of ±0.5°C and ±1°C. The increased accuracy of the series is designed for many analog temperature-sensing applications. The TMP235 device provides a positive slope output of 10 mV/°C over the full –40°C to +150°C temperature range and a supply range from 2.3 V to 5.5 V. The 9-µA typical quiescent current and 800-µs typical power-on time enable effective power-cycling architectures to minimize power consumption for battery-powered devices.

For more details on this device, refer the TMP235 product page.

2.2.11 LMT87

The LMT87 device is a precision CMOS temperature sensor with ±0.4°C typical accuracy (±2.7°C maximum) and a linear analog output voltage that is inversely proportional to temperature. The 2.7-V supply voltage operation, 5.4-µA quiescent current, and 0.7-ms power-on time enable effective power-cycling architectures to minimize power consumption for battery-powered applications such as drones and sensor nodes. The LMT87LPG through-hole TO-92S package fast thermal time constant supports off-board time-temperature sensitive applications such as smoke and heat detectors. The accuracy over the wide operating range and other features make the LMT87 an excellent alternative to thermistors.

For more details on this device, refer the LMT87 product page.

2.2.12 TL431

The TL431 is three-terminal adjustable shunt regulators, with specified thermal stability over applicable automotive, commercial, and military temperature ranges. The output voltage can be set to any value between Vref (approximately 2.5 V) and 36 V, with two external resistors. These devices have a typical output impedance of 0.2 Ω. Active output circuitry provides a very sharp turn-on characteristic, making these devices excellent replacements for Zener diodes in many applications, such as onboard regulation, adjustable power supplies, and switching power supplies.

For more details on this device, refer the TL431 product page.

2.2.13 LMV762

The LMV76x devices are precision comparators intended for applications requiring low noise and low input offset voltage. The LMV761 single has a shutdown pin that can be used to disable the device and reduce the supply current. These devices feature a CMOS input and push-pull output stage. The push-pull output stage eliminates the need for an external pullup resistor. The LMV76x are designed to meet the demands of small size, low power and high performance required by portable and battery-operated electronics. The input offset voltage has a typical value of 200 µV at room temperature and a 1-mV limit over temperature.

For more details on this device, refer the LMV762 product page.

2.2.14 TVS1400

The TVS1400 robustly shunts up to 43 A of IEC 61000-4-5 fault current to protect systems from high power transients or lightning strikes. The device offers a solution to the common industrial signal line EMC requirement to survive up to ±2 kV IEC 61000-4-5 open circuit voltage coupled through 42 Ω impedance. The TVS1400 uses a unique feedback mechanism to ensure precise flat clamping during a fault, assuring system exposure below 20 V. The tight voltage regulation allows designers to confidently select system components with a lower voltage tolerance, lowering system costs and complexity without sacrificing robustness.

For more details on this device, refer the TVS1400 product page.

2.2.15 TMS320F280049 C2000 MCU

The Piccolo™ TMS320F28004x (F28004x) is a powerful 32-bit floating-point microcontroller unit (MCU) that lets designers incorporate crucial control peripherals, differentiated analog, and nonvolatile memory on a single device. The real-time control subsystem is based on TI's 32-bit C28x CPU, which provides 100 MHz of signal processing performance. The C28x CPU is further boosted by the new TMU extended instruction set, which enables fast execution of algorithms with trigonometric operations commonly found in transforms and torque loop calculations; and the VCU-I extended instruction set, which reduces the latency for complex math operations commonly found in encoded applications. The CLA allows significant offloading of common tasks from the main C28x CPU. The CLA is an independent 32-bit floating-point math accelerator that executes in parallel with the CPU. Additionally, the CLA has its own dedicated memory resources and it can directly access the key peripherals that are required in a typical control system. Support of a subset of ANSI C is standard, as are key features like hardware breakpoints and hardware task-switching. The F28004x supports up to 256KB (128KW) of flash memory divided into two 128KB (64KW) banks, which enables programming and execution in parallel. Up to 100KB (50KW) of on-chip SRAM is also available in blocks of 4KB (2KW) and 16KB (8KW) for efficient system partitioning. Flash ECC, SRAM ECC/parity, and dual-zone security are also supported. High-performance analog blocks are integrated on the F28004x MCU to further enable system consolidation. Three separate 12-bit ADCs provide precise and efficient management of multiple analog signals, which ultimately boosts system throughput. Seven PGAs on the analog front end enable on-chip voltage scaling before conversion. Seven analog comparator modules provide continuous monitoring of input voltage levels for trip conditions. The TMS320C2000™ devices contain industry-leading control peripherals with frequency-independent ePWM/HRPWM and eCAP allow for a best-in-class level of control to the system. The built-in 4-channel SDFM allows for seamless integration of an oversampling sigma-delta modulator across an isolation barrier.

For more details on the product, refer the TMS320F280049 product page.

2.2.16 TMDSCNCD280049C

TMDSCNCD280049C is an HSEC180 controlCARD based evaluation and development tool for the C2000™ Piccolo F28004x series of microcontroller products. controlCARDs are ideal to use for initial evaluation and system prototyping.

For more details on the product, refer the TMDSCND280049C product page.

2.3 System Design Theory

The following sections give an extensive overview of the operating principles of the dual-active bridge.

2.3.1 Dual Active Bridge Analogy With Power Systems

Power transfer between the two bridges in a dual-active bridge is analogous to the power flow between two voltage buses in a power system. Consider two voltage sources connected by a line reactance as shown in Figure 3.

Figure 3. Power Transfer Between Voltage Bus

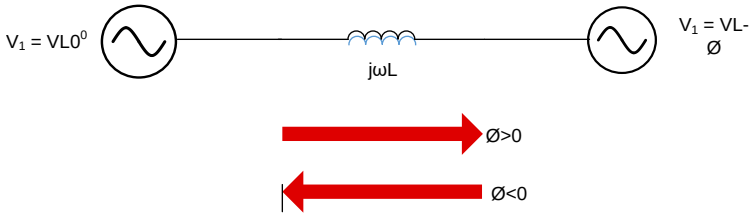
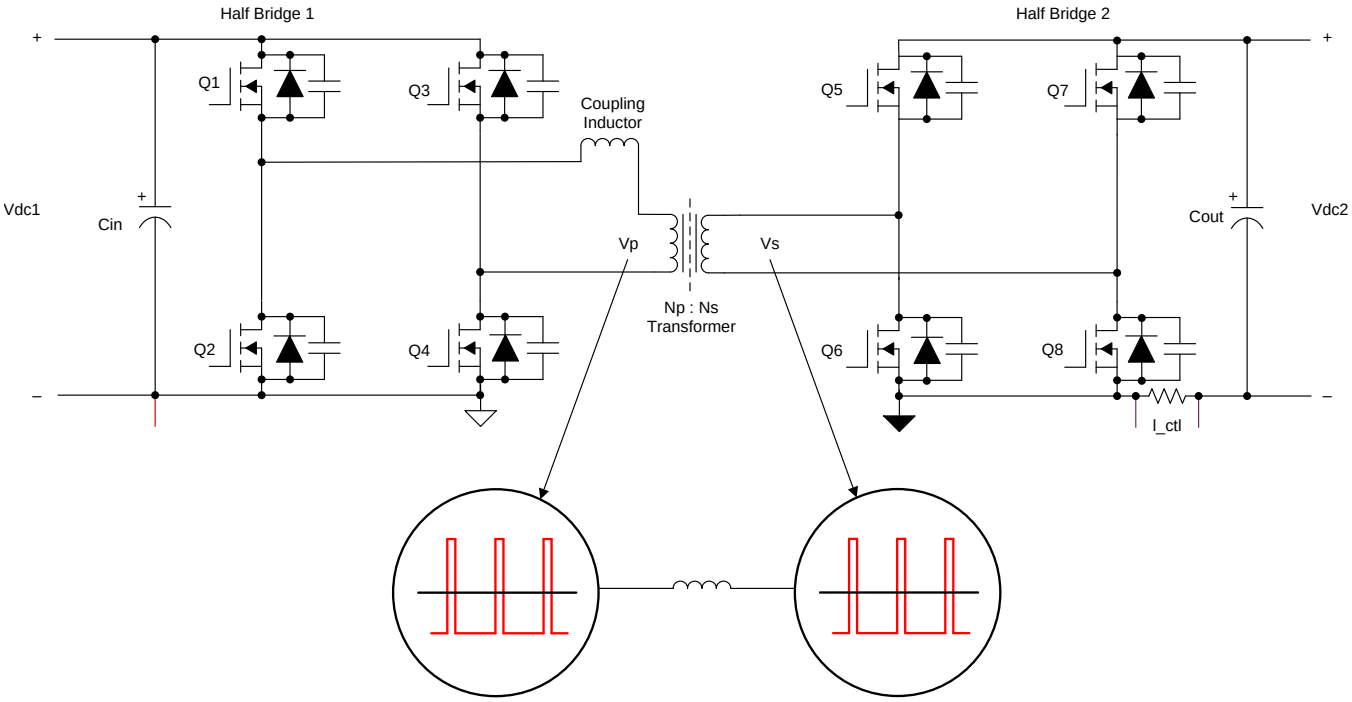


Figure 3 shows that the voltage source on the right is lagging with respect to the voltage source on the left. Hence, the power transfer takes place from the left towards the right as per Equation 1.

$$P = \frac{V1 \times V2 \times \sin Ø}{\omega \times L} \quad (1)$$

Similarly, power transfer happens in a dual-active bridge where two high-frequency square waves are created in the primary and secondary side of the transformer by the switching action of MOSFETs. These high-frequency square waves are phase shifted with respect to each other. Power transfer takes place from the leading bridge to the lagging bridge, and this power flow direction can be easily changed by reversing the phase shift between the two bridges. Hence, it is possible to obtain bidirectional power transfer with ease in a dual-active bridge as shown in Figure 4.

Figure 4. Dual-Active Bridge



2.3.2 Dual-Active Bridge - Switching Sequence

In a single-phase, dual-active bridge, primary and secondary bridges are controlled simultaneously. All switches operate at 50% duty ratio. The diagonal switches turn on and turn off together so that the output of each bridge is a square wave. The switching sequence of the converter is elaborated in detail in this section.

The switching sequence is divided into four intervals based on the inductor current waveform and phase shift between the voltages at the primary and secondary of the transformer. The voltage and the current waveforms are depicted in Figure 11. During interval one, the inductor current waveform is both positive and negative, and hence, the current commutation follows the scheme shown in Figure 5 and Figure 6. During this interval, switches Q1 and Q4 in the primary and switches Q6 and Q7 in the secondary conduct current.

Figure 5. Interval 1: Negative Inductor Current

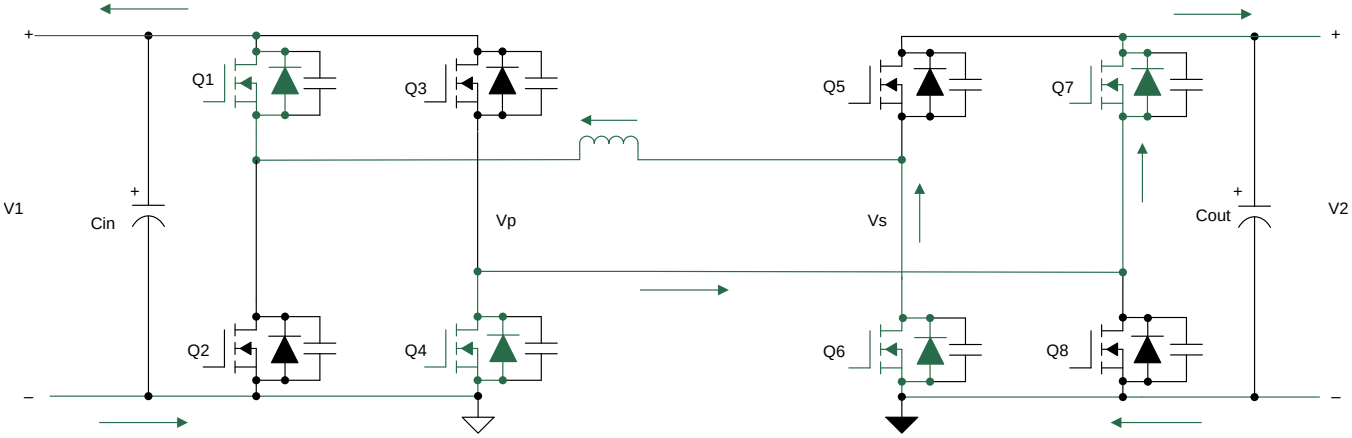
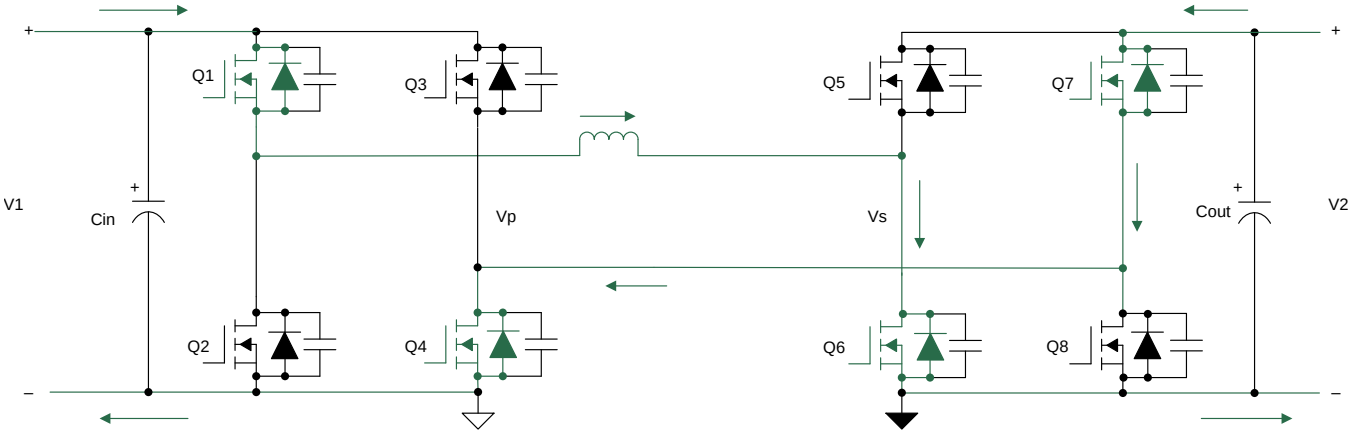


Figure 6. Interval 1: Positive Inductor Current



During this interval, the voltage across the primary, Vp, is equal to V1, and the voltage across the secondary, Vs, is equal to V2. The difference between these voltages appears across the leakage inductor, and the slope of the current during this interval can be approximated by Equation 2.

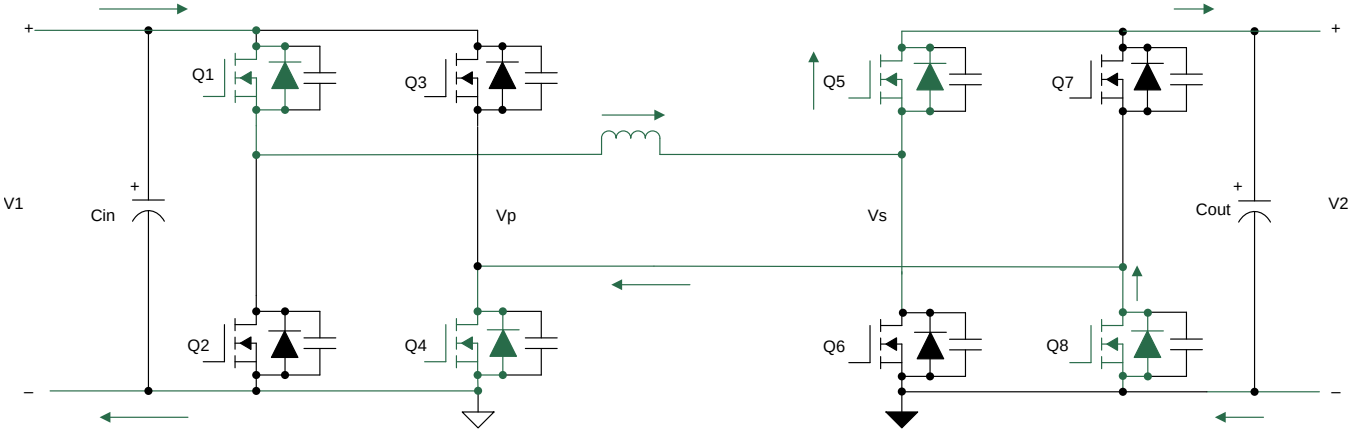
$$\frac{di}{dt} = \frac{V1 + V2}{L} \tag{2}$$

During interval two, the inductor current is positive. The voltage across the transformer primary is positive and is equal to V1, and the voltage across the secondary winding is positive and is equal to V2. Hence, the difference of these two voltages appears across the leakage inductor, and the slope of the rising current during this interval can be calculated by Equation 3.

$$\frac{di}{dt} = \frac{V1 - V2}{L} \tag{3}$$

During this interval, switches Q1 and Q4 remain turned on, but as the voltage across the secondary is now V2 with the inductor current positive, switches Q5 and Q8 turn on to conduct current. There is a small dead time period between the turn off of Q6 and Q7 and the turn on of Q5 and Q8. During this dead time, the phenomenon of zero voltage switching (ZVS) occurs, which is explained in detail in the following section. The commutation sequence for the second interval is shown in Figure 7.

Figure 7. Interval 2



During interval three, the inductor current starts ramping down from its positive peak to a negative value as shown in Figure 11. In this interval, the voltage across the primary is –V1, and the voltage across the secondary is V2. The difference of these voltages, which is (-V1-V2), appears across the inductor. Hence, the current ramps down with a negative slope as shown in Equation 4.

$$\frac{di}{dt} = -\frac{V1+V2}{L} \tag{4}$$

During this interval, switches Q5 and Q8 continue to remain turned on, but as the voltage across the primary is now –V1, switches Q2 and Q3 turn on to conduct current. The conduction for both directions of inductor current IL > 0 and IL < 0 is shown in Figure 8 and Figure 9 respectively.

Figure 8. Interval 3: Positive Inductor Current

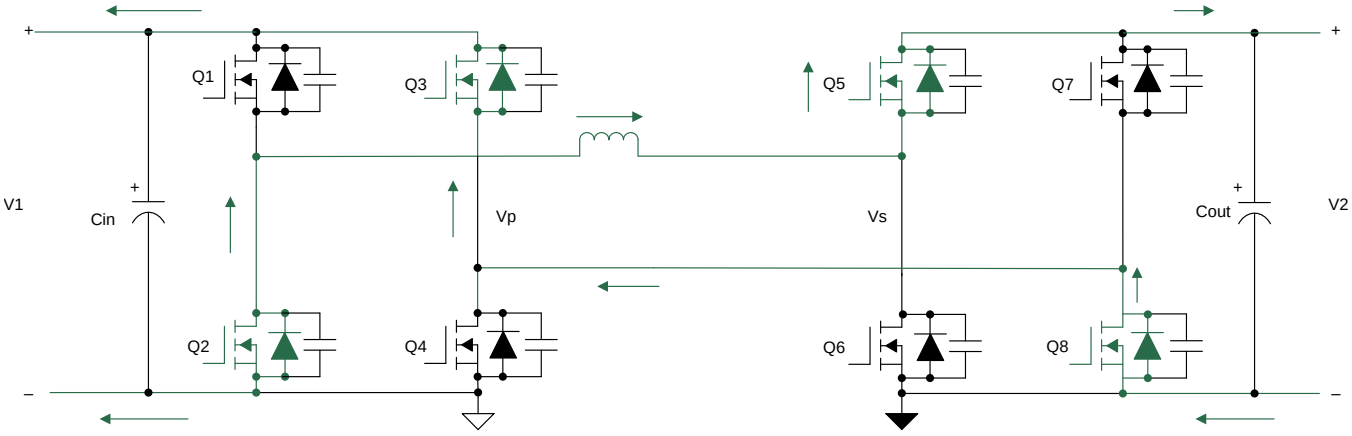
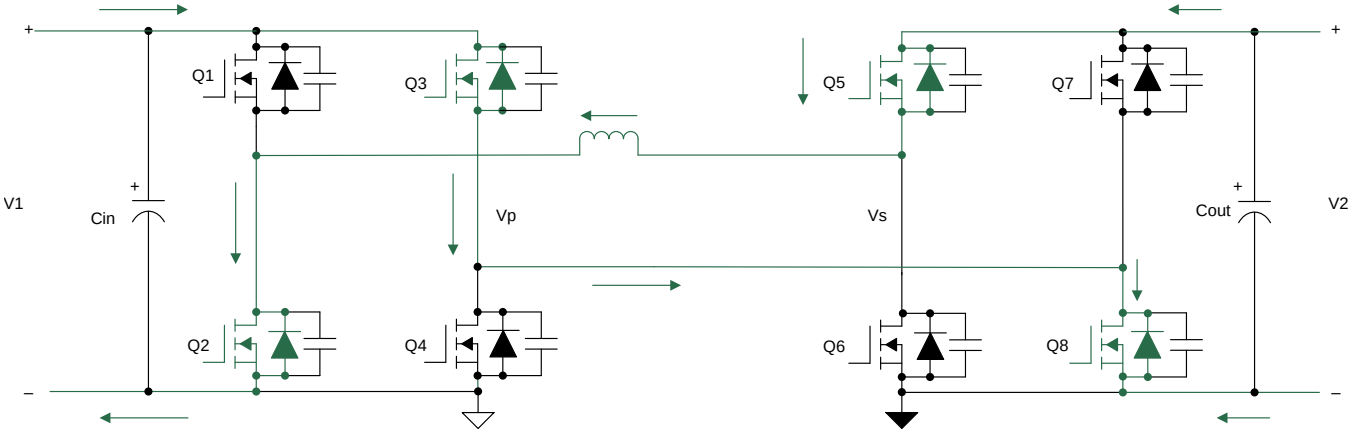


Figure 9. Interval 3: Negative Inductor Current



During interval four, the inductor current continues to be negative. During this interval, the voltage across the primary is –V1 and, and the voltage across the secondary is -V2. The difference in these voltages, which is (-V1+V2), appears across the inductor. Hence, the current ramps down with a negative slope as shown in Equation 5.

$$\frac{di}{dt} = -\frac{V1 - V2}{L} \quad (5)$$

During this interval, switches Q2 and Q3 continue to remain turned on, but as the voltage across the secondary are now –V2, switches Q6 and Q7 turn on to conduct current as shown in Figure 10.

Figure 10. Interval 4

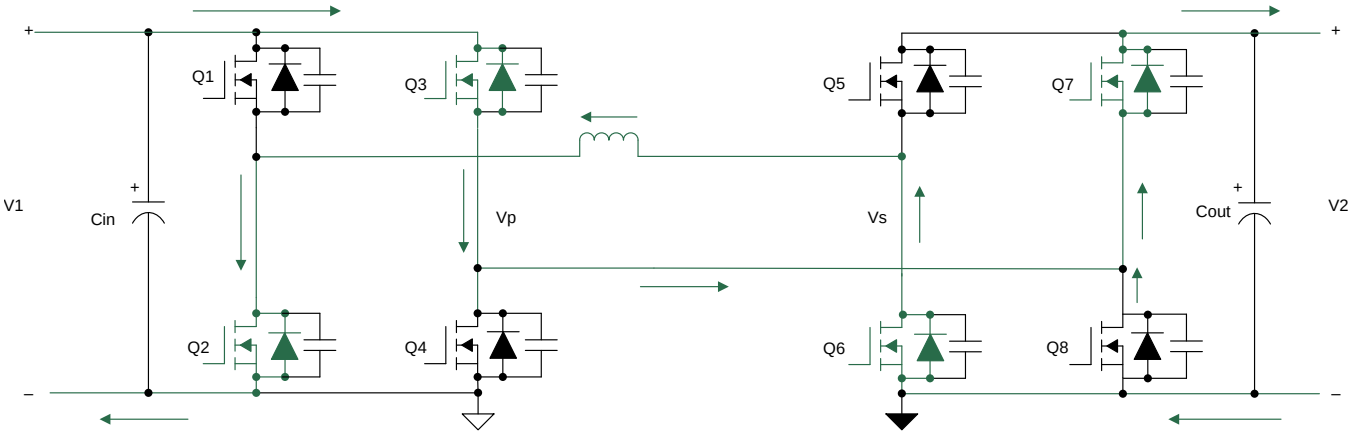
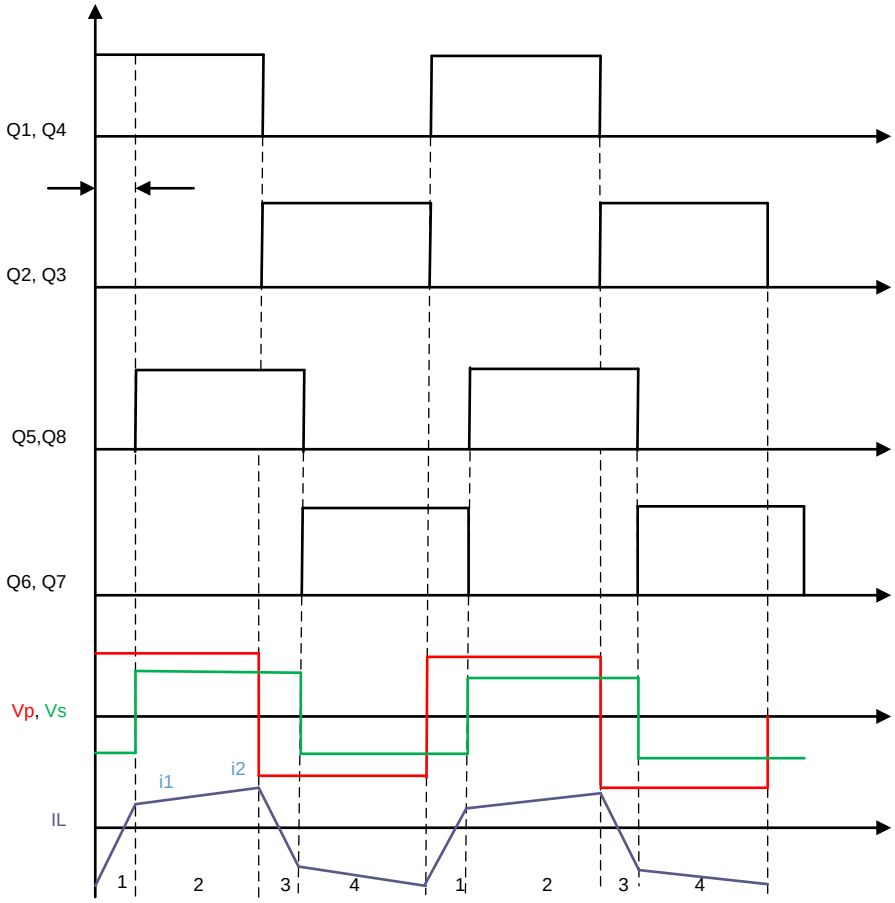


Figure 11 shows the gating pulses of the switches on the primary and secondary side. The variable Ø represents the phase shift between the PWM pulses of the primary and secondary side. Vp and Vs represent the voltage on the primary and secondary winding of the transformer. IL represents the transformer current.

Figure 11. Gate Signals, Transformer Primary and Secondary Voltages, and Inductor Current

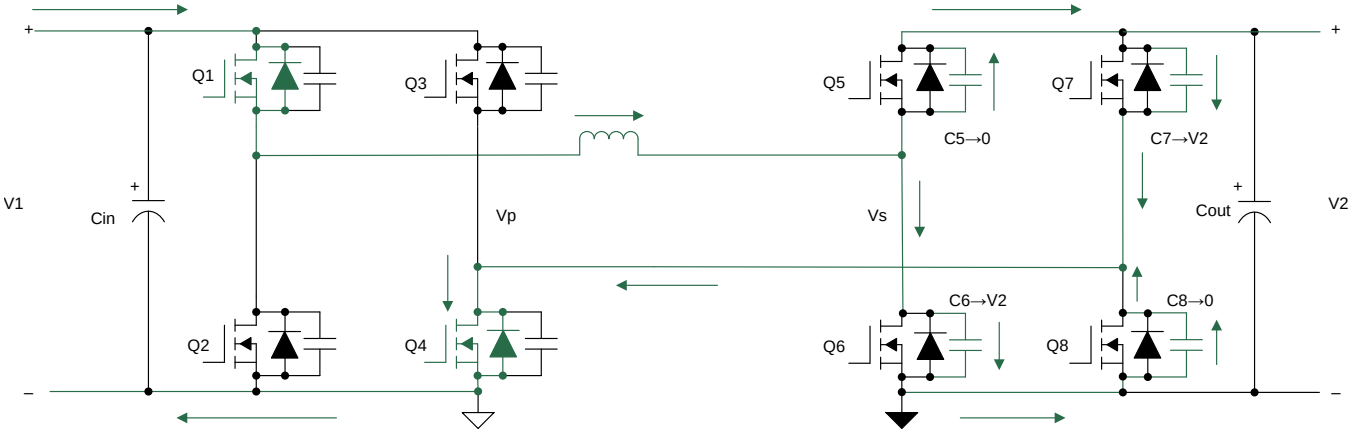


2.3.3 Dual-Active Bridge - Zero Voltage Switching (ZVS)

During the transition from interval one to two, there exists a small dead time where the inductor-stored energy discharges the output capacitances of the MOSFETs and holds them close to zero voltage before they are turned on. This phenomenon, where the voltage across the MOSFET is close to zero at turn on, is referred to as zero voltage switching (ZVS). This is a major advantage with this topology, where due to the natural lagging current in one of the bridges, the inductive stored energy causes ZVS of all of the lagging bridge switches and some of the switches of the leading bridge. This depends on the stored inductive energy ($E_L = 0.5LI^2$) available to charge and discharge the output capacitances of MOSFETs ($E_C = 0.5CV^2$).

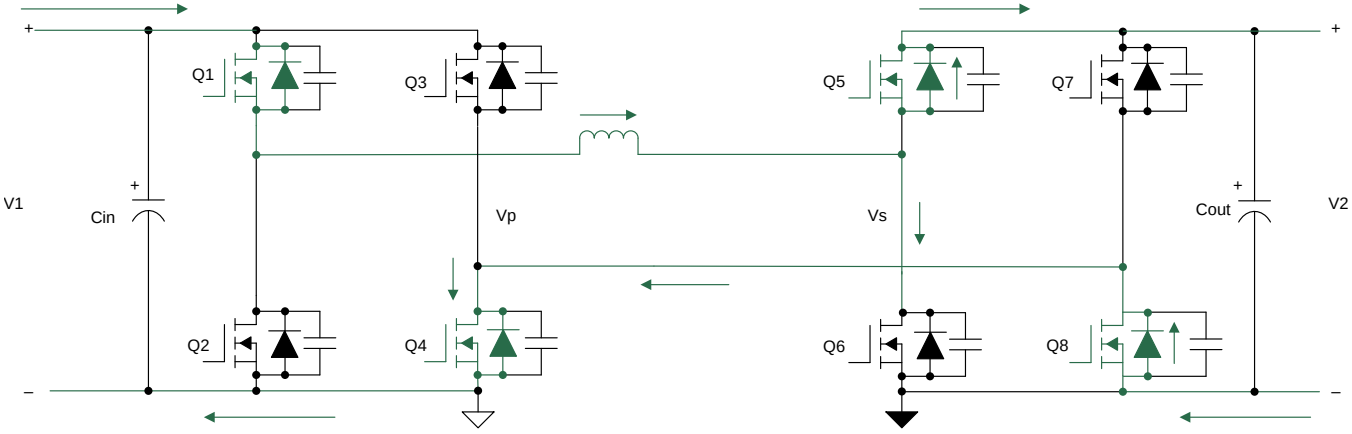
When transition happens from interval one to two, the primary side switches Q_1 and Q_5 continue conduction, whereas in the secondary, Q_6 and Q_7 turn off and Q_5 and Q_8 turn on. Initially the voltage across Q_6 and Q_7 is zero when they are conducting, and Q_5 and Q_8 block the entire secondary voltage. During dead time, when all of the switches in the secondary are off, the inductor-stored energy circulates current which discharges the capacitor across MOSFETs Q_5 and Q_8 to zero and charges the capacitor across MOSFETs Q_6 and Q_7 to the full secondary voltage. The current commutation is shown in Figure 12.

Figure 12. ZVS Transition in Secondary Side - Capacitor



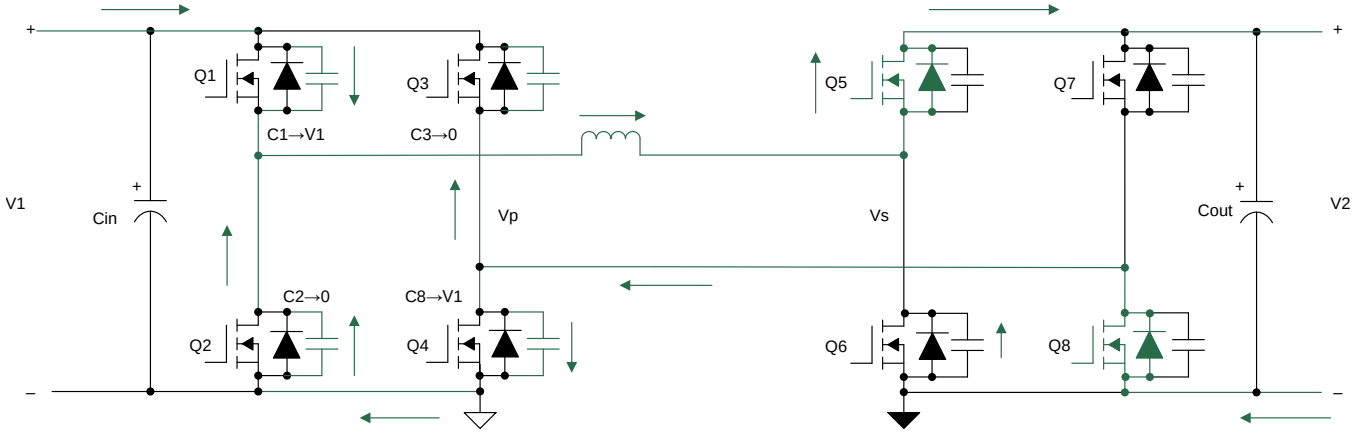
Once the capacitors have been charged and discharged, the current must continue to flow. The current will flow through the diodes D_5 and D_8, thereby clamping the voltage across MOSFETs Q_5 and Q8 to zero as shown in Figure 13. During the next interval, MOSFETs Q_5 and Q_8 are turned on at zero voltage, thereby reducing turn on losses completely. The arrow close to the diode indicates that the diode is conducting and the MOSFET is off.

Figure 13. ZVS Transition in Secondary Side - Diode



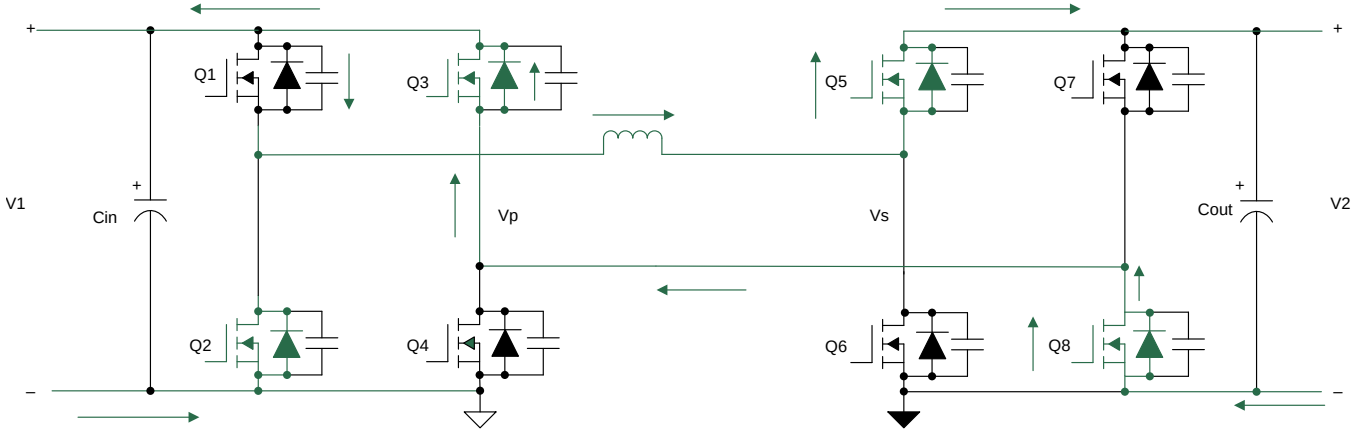
Similarly, zero voltage switching across the switches of the primary during the transition from interval 2 to 3 is explained in the following section. When transition happens from interval two to three, the secondary side switches Q_5 and Q_8 continue conduction, whereas in the primary, Q_1 and Q_4 turn off and Q_2 and Q_3 turn on. Initially, the voltage across Q_1 and Q_4 is zero when they are conducting, and Q_2 and Q_3 block the entire secondary voltage. During dead time when all of the switches in the primary are off, the inductor stored energy circulates current, which discharges the capacitor across MOSFETs Q_2 and Q_3 to zero and charges the capacitor across MOSFETs Q_1 and Q_4 to the full primary voltage. The current commutation is shown in Figure 14.

Figure 14. ZVS Transition in Primary Side - Capacitor



Once the capacitors have been charged and discharged, the current must continue to flow. The current will flow through diodes D2 and D3, thereby clamping the voltage across MOSFETs Q2 and Q3 to zero as shown in Figure 15. During the next interval, MOSFETs Q2 and Q3 are turned on at zero voltage, thereby reducing turn on losses completely. The arrow close to the diode indicates that the diode is conducting and the MOSFET is off.

Figure 15. ZVS Transition in Primary Side - Diode



2.3.4 Dual-Active Bridge - Design Considerations

A number of factors are critical in the design of the power stage of a dual-active bridge. The most important factors are the selection of leakage inductor, desired phase shift of operation, output capacitor rating, switching frequency of operation, selection of SiC MOSFETs, transformer, and intended ZVS range of operation. Many of these design parameters are interrelated, and selection of any one of them has a direct impact on the others. For example, the selection of leakage inductor has a direct effect on the maximum power transferred, which in turn affects the phase shift of operation of the converter at the intended power level. Each of these factors are discussed in detail in the following sections.

2.3.4.1 Leakage Inductor

The most important design parameter is the selection of leakage inductor. The power transfer relation of the dual-active bridge is given by Equation 6.

$$P = \frac{nV_1V_2\emptyset\left(1-\frac{\emptyset}{\pi}\right)}{\left(2\pi^2 F_S L\right)} \tag{6}$$

Equation 6 shows that a low value of inductance will lead to high power transfer capability. The maximum value of power transfer for a given switching frequency, leakage inductor, and input and output voltage will occur at Ø = π/2. Figure 16 shows the inductor current waveform. From this waveform, the value of current at points i_1 and i_2 can be derived.

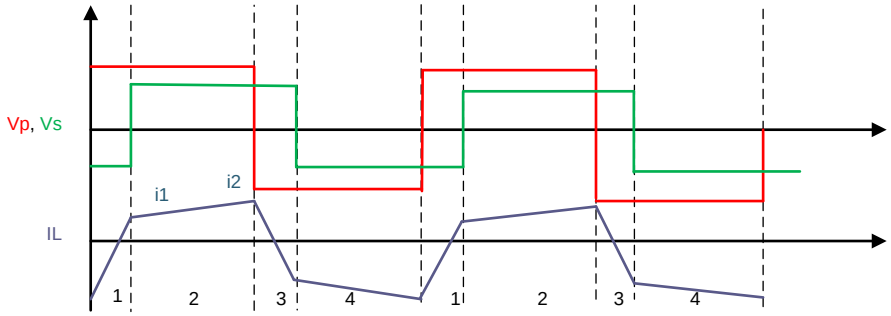
$$i_1 = 0.5\left(2d\text{Ø} + (1-d)\pi\right)I_{nom} \quad (7)$$

$$i_2 = 0.5\left(2\text{Ø} - (1-d)\pi\right)I_{nom} \quad (8)$$

Where d is the voltage transfer ratio of the converter given in Equation 9 and I_{nom} is the nominal base current of the converter.

$$d = \frac{V_2}{NV_1} \quad (9)$$

Figure 16. Inductor Current Waveform



From Equation 7 and Equation 8, the conditions for zero voltage switching for leading and lagging bridge of the converter can be obtained.

From the following conditions, the conditions for ZVS are obtained in terms of phase and voltage gain of the converter, summarized in Equation 10 and Equation 11 for the primary bridge and secondary bridges respectively.

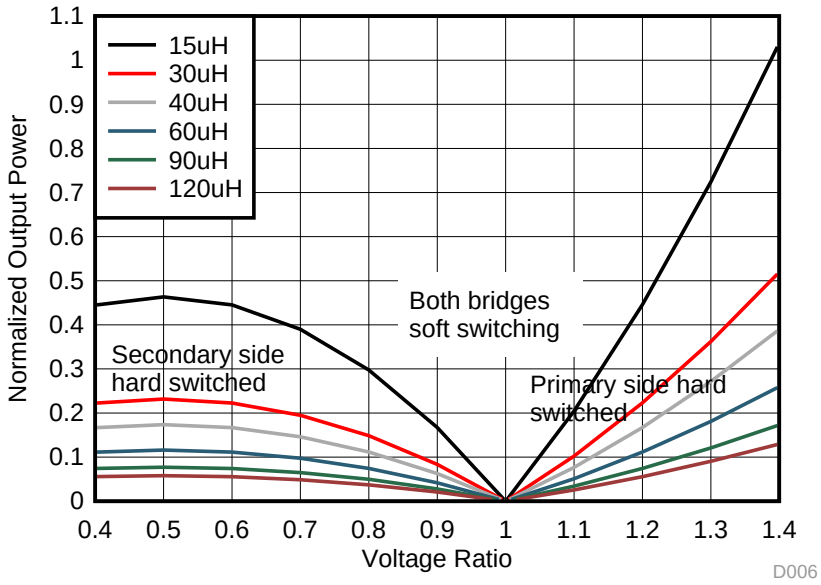
- $i_1 > 0$ for the secondary side bridge
- $i_2 > 0$ for the primary side bridge

$$\text{Ø} > \left(1 - \frac{1}{d}\right)\pi / 2 \quad (10)$$

$$\text{Ø} > (1-d)\pi / 2 \quad (11)$$

By combining Equation 7, Equation 8, Equation 10, and Equation 11, the relationship between output power and voltage ratio for different values of the inductor is obtained. A MATLAB® script used to plot this relationship is depicted in Figure 17. The figure shows that for a particular value of inductance, when the voltage transfer ratio changes from unity, the converter switches experience hard switching. As long as the voltage transfer ratio is kept at unity, soft switching across both the primary and secondary leg switches is obtained. The most important point to note is that the soft switching region (zero voltage switching) depends on the value of leakage inductance. As the value of inductance increases, the ability for soft switching of the converter extends up to very low power levels (light loads).

Figure 17. ZVS Range and Output Power Versus Voltage Transfer Ratio



2.3.4.2 Effect of Inductance on Current

In the previous section, it is noted that a high value of leakage inductance can contribute to soft switching up to a very low power level and hence leads to better switching performance. Alternatively, increasing the leakage inductance leads to increased RMS currents in the primary and secondary of transformer, switch currents, and ripple currents in the capacitor as described in the following sections. Equation 12 and Equation 13 show the RMS currents across the primary and secondary side.

$$I_{P\_rms}^2 = i_1^2 + i_2^2 + i_1 i_2 \frac{1 - 2\frac{\emptyset}{\pi}}{3} \tag{12}$$

$$I_{S\_rms} = \frac{Np}{Ns} I_{P_{rms}} \tag{13}$$

Using these equations and the equation for power transfer, the variation in current across the primary and secondary side with inductance is plotted in Figure 18.

Figure 18. Variation of RMS Currents With Leakage Inductance

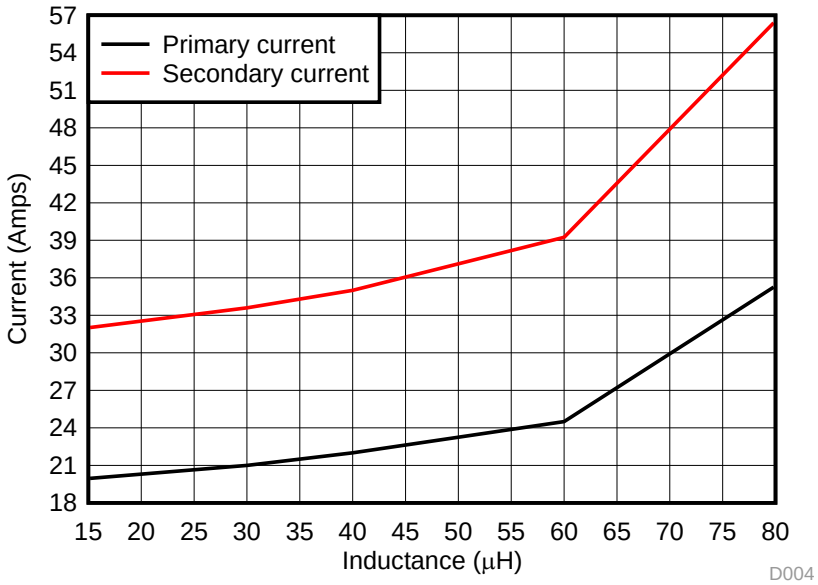


Figure 18 shows that as the value of leakage inductance increases, the RMS currents in the transformer and switches increase, leading to more conduction losses. Thus, there exists a tradeoff between an optimal value of leakage inductance to affect ZVS and minimizing conduction losses.

2.3.4.3 Phase Shift

The phase shift of the converter is dependent on the value leakage inductor. The phase shift for required power transfer is given by Equation 14.

$$Ø = \frac{\pi}{2} \times \left(1 - \sqrt{1 - \frac{8 \times F_s \times L \times P_{out}}{n \times V_1 \times V_2}}\right) \quad (14)$$

Figure 19. Variation of Phase Shift With Leakage Inductance

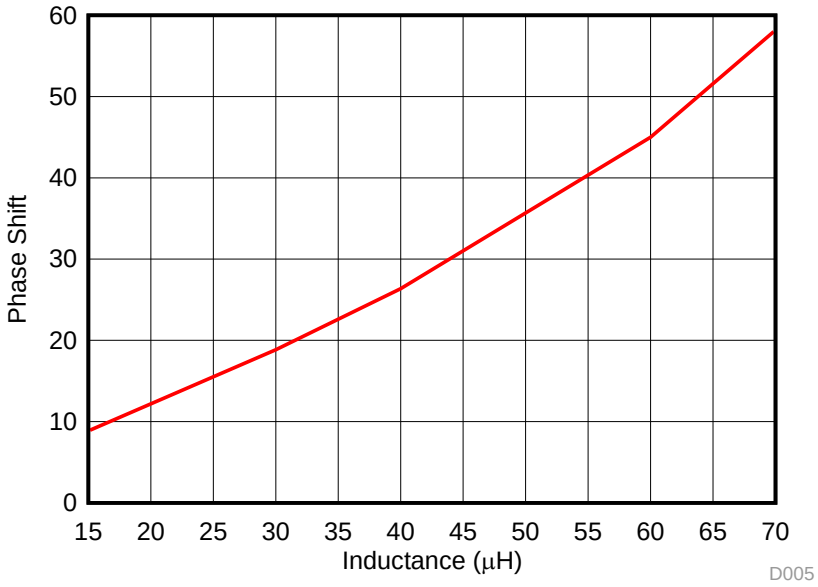


Figure 19 shows that for a small value of inductance, a maximum power transfer at a small value of phase shift is obtained. To have fine control over power transferred, fine high resolution steps in which the phase can be varied must be obtained. Alternatively, a larger inductor can obtain maximum power transfer at a high value of phase shift for better control.

2.3.4.4 Capacitor Selection

The output capacitor in the dual-active bridge must be designed to handle the ripple. This value impacts the output voltage specification. From Figure 20, Equation 15 and Equation 16 are obtained.

$$I_{cap} = I_{hb2} - I_{load} \tag{15}$$

$$C\frac{dV_2}{dt} = \frac{V_1}{X_L}\text{Ø}\left(1 - \frac{\text{Ø}}{\pi}\right) - \frac{V_2}{R} \tag{16}$$

Figure 20. Output Current in Dual-Active Bridge

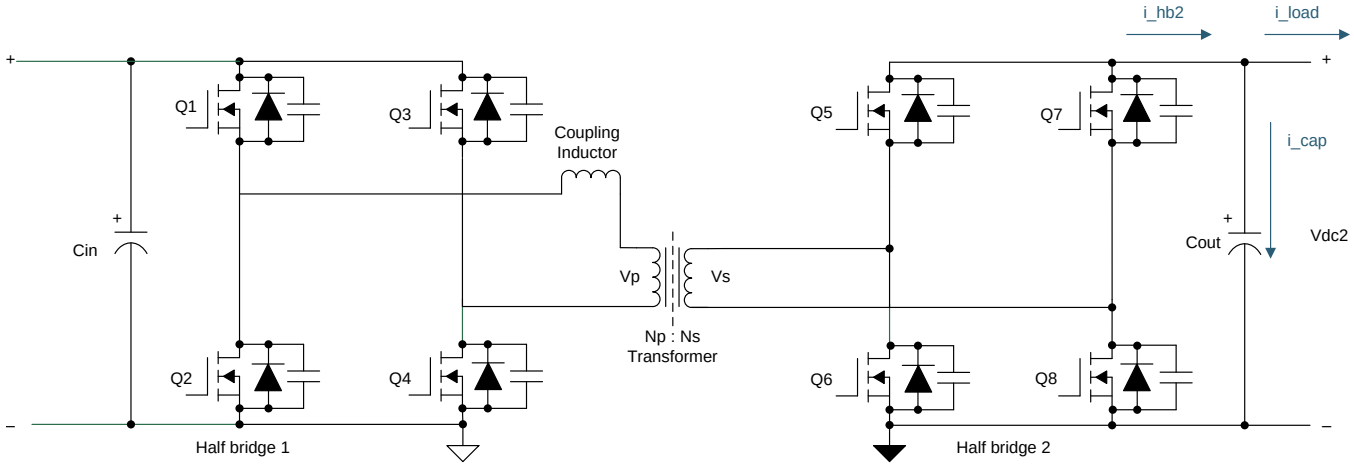
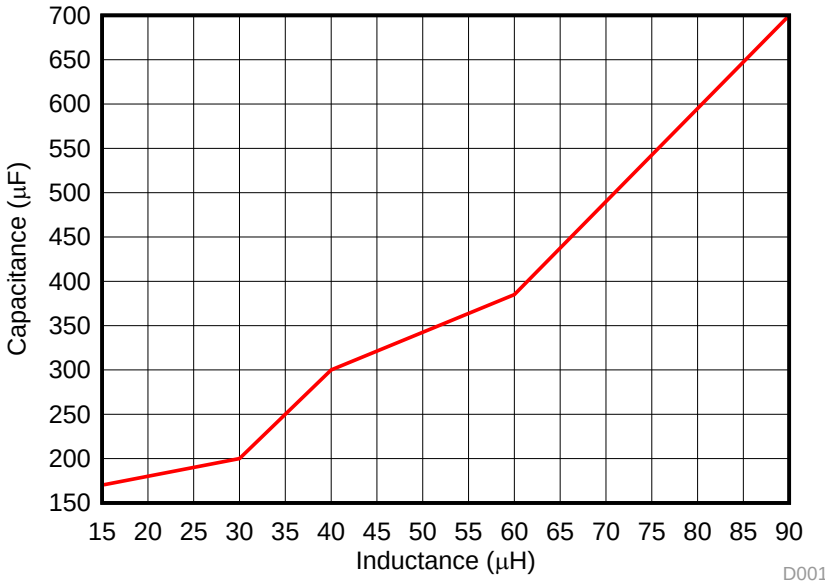


Figure 21 shows the effect of the leakage inductor on the selection of the output capacitance. For a particular value of phase shift and inductance, capacitance required for containing the voltage ripple to a specified limit, as per the system specification, increases as the leakage inductor increases. This also means that more capacitance is needed to handle the voltage ripple. As the RMS value of capacitor current increases, more is the loss dissipated across the equivalent series resistance (ESR) of capacitance. Considering these factors, the output capacitor was chosen to keep the output voltage under 5% ripple.

Figure 21. Desired Output Capacitance Versus Leakage Inductance



2.3.4.5 Soft Switching Range

Figure 17 shows that the soft switching range of the converter is maximized when the turns ratio is chosen such that the primary voltage is equal to the reflected secondary voltage. In this condition, the voltage transfer ratio is equal to unity, and all of the switches of the primary and secondary side experience soft switching under all conditions. In practice, the total capacitance of the switching node must be discharged by currents i1 and i2 as given by Equation 7 and Equation 8 within the specified dead time so that switches turn on at zero voltage. For light load conditions where there is not sufficient inductive stored energy to discharge the capacitive energy of the MOSFETs, the dead time could be increased in accordance with current so as to affect ZVS.

2.3.4.6 Switching Frequency

Switching frequency is another important design parameter which affects the efficiency and power density of power converter. The input and the output voltage levels primarily determine the type of switches used in the power stage. Usage of SiC MOSFETs in the power stage drives the switching frequencies to very high levels. Operating at higher switching frequencies enables reduced size of magnetics which help in improved thermal solution, thereby improving power density of the converter. Therefore, selection of switching frequency is primarily a tradeoff between the allowable heat sink solution and transformer size for a given efficiency target. Secondly, if the output capacitance (Ecoss) of MOSFET is very high, selection of high switching frequency leads to high switching losses at light load and hampers efficiency. Selection of switching frequency also affects the control loop bandwidth implementation. Considering all of these parameters, 100 Khz was used as the switching frequency for this application.

2.3.4.7 Transformer Selection

In a power supply design, transformers and inductors are major contributors to size. Increasing the operating frequency reduces their size, but increasing the switching frequency beyond a particular value affects the efficiency of the power module. This is because the skin effect becomes very high at that frequency where the current flows through the surface of the conductor. Similar to the skin effect, there is a proximity effect, which causes current to only flow on surfaces closest to each other. Furthermore, from a proximity standpoint in high-frequency designs, conductor size and the number of layers must be optimized. With a planar transformer, more interleaving to reduce the proximity effect can be achieved. This interleaving can be tailored to produce a specific amount of leakage so as to aid in power transfer and to contribute to ZVS.

Planar transformers offer the following advantages over conventional transformers and hence were used in this reference design:

- Planar magnetics have very high power density. They are more compact and consume less space when compared to a conventional transformer of the same power rating.
- They have the ability to do more interleaving to reduce AC conductor losses.
- They have consistent spacing between turns and layers which translate into consistent parasitics. Both leakage inductance and intrawinding capacitances can be maintained to very predictable and tight values.
- Tight control over the leakage inductance is possible with planar magnetics.
- The transformer's compact size can support integration of the additional shim inductor with the transformer itself without the need for a separate component on board.

focuses on the actual planar transformer chosen for this application with details on the loss numbers.

The leakage inductor alone cannot ensure soft switching up to light loads. As seen previously, increasing the soft switching range by increasing inductor value increases the RMS currents. In practice, leakage inductor is chosen to provide soft switching only up to ½ or 1/3 of rated load. Beyond this point, the transformer magnetizing inductance is used for ensuring soft switching near light loads. The magnetizing inductance is chosen generally ten times the value of leakage inductance as a starting point for this optimization.

2.3.4.8 SiC MOSFET Selection

As shown in Figure 2, the main power stage switching devices of the primary and secondary must block the full input and output DC voltages. SiC switches were chosen for the following reasons:

- The switching speed of the SiC MOSFET is faster than a traditional Si device, thereby reducing switching losses.
- The reverse recovery charge is significantly smaller in the SiC MOSFET for DAB application, resulting in reduced voltage and current overshoot.
- Lower state resistance will significantly reduce conduction losses during on time of the device.
- The switches have the ability to block higher voltages without breaking down.

For this design, 1200-V Cree® devices with on state resistance of 16 mΩ were used on the primary side, and a 900-V, voltage-blocking Cree device with on state resistance of 30 mΩ was used in the secondary. Both are four-pin devices with a kelvin connection for better switching performance. The actual conduction and switching loss calculations are shown in the following sections.

2.3.5 Loss Analysis

In this section, the theoretical efficiency numbers obtained in the dual-active bridge are reviewed. To arrive at the losses in different elements, the average and the RMS currents across the primary and secondary side are calculated. Details on the actual derivation of equations are out of scope for this design but are listed as references in . The maximum power transfer in a dual-active bridge occurs at a phase shift of 90°. However, a high phase shift requires a high leakage inductance for power transfer. Using a high inductor leads to increased RMS currents in the primary and secondary side, which affects the efficiency of the converter.

Figure 19 shows the relationship between phase shift and the required inductance obtained from MATLAB simulations. The system specifications are tabulated in Table 2.

Table 2. DC/DC Converter Electrical Parameters

Phase shift	-0.44 < Ø < 0.44 (rad)
Total Leakage Inductance	35 uH
Turns Ratio	1: 0.625
Load resistance	26Ω
Input Voltage	800V
Output voltage	500V
Input current	12.5A
Output current	20A
Output Power	10KW

2.3.5.1 Design Equations

The voltage transfer ratio, m, for a dual-active bridge is given by Equation 17, where N is the primary-to-secondary turns ratio.

$$m = \frac{V_o}{NV_{in}} \tag{17}$$

The required leakage inductor for phase shift is calculated from Equation 18.

$$L_{lk} = Ø\left(1 - Ø\right) NV_{in} \frac{V_{out}}{2F_{sw}P_{out}} = 36\ \mu h \tag{18}$$

For the required phase shift of 23°, the required leakage inductance calculated from this equation is approximately 36 uH. The total transformer leakage inductance is around 23 uH when referred to the output side. Hence, an additional shim inductance of between 13 uH to 15 uH is needed to achieve the required power transfer at this value of phase shift. This approximately matches the simulation results for required phase shift against inductance.

2.3.5.2 SiC MOSFET and Diode losses

As SiC is used in the power stage, the body diodes conduct only during the dead time, causing ZVS. In all other instances, the channel of SiC is turned on to conduct current. The peak current in the primary is calculated using Equation 19. In this equation,

- Leakage inductance is 32 uH
- Phase shift is 23 degrees
- N is the primary-to-secondary turns ratio, which is 1.6
- n is secondary to primary turns ratio, which is 0.625

$$I_p = \frac{T_s}{2L_k}\left(nV_{in} + V_{out}\left(2Ø - 1\right)\right) = 22\ A \tag{19}$$

The RMS and average values of currents through current through the switches and diodes of the primary side are calculated using Equation 20 and Equation 21. In these equations, I_l is equal to I_p because duty cycle is operating at 0.5.

$$I_{switch\_prim\_rms} = \sqrt{\frac{1}{3T_S}\left(I_p^2\left(t_{zero}\right) + I_p^2\left(Ø\frac{T_s}{2} - t_{zero}\right) + \left(\frac{T_s}{2} - Ø\frac{T_s}{2}\right) \times \left(I_p^2 + I_l^2 + I_l I_p\right)\right)} = 15.65\ A \tag{20}$$

The RMS value of switch current is calculated from Figure 22 over a switching cycle. The diode conducts for only a small fraction of time during the switching period, as in, the dead time causing ZVS. The dead time chosen for this application is 200 ns.

$$I_{diode\_prim\_avg} = t_{dead\_time} \frac{I_p}{T_s} = 0.44\,A \quad (21)$$

From the data sheet of the SiC MOSFETs, the value of drain source resistance corresponding to the applied gate voltage waveform is obtained. This value is approximately 20 mΩ. The forward voltage drop across the body diode is 4.2 V. The conduction losses across the four primary side FETs is calculated using Equation 22:

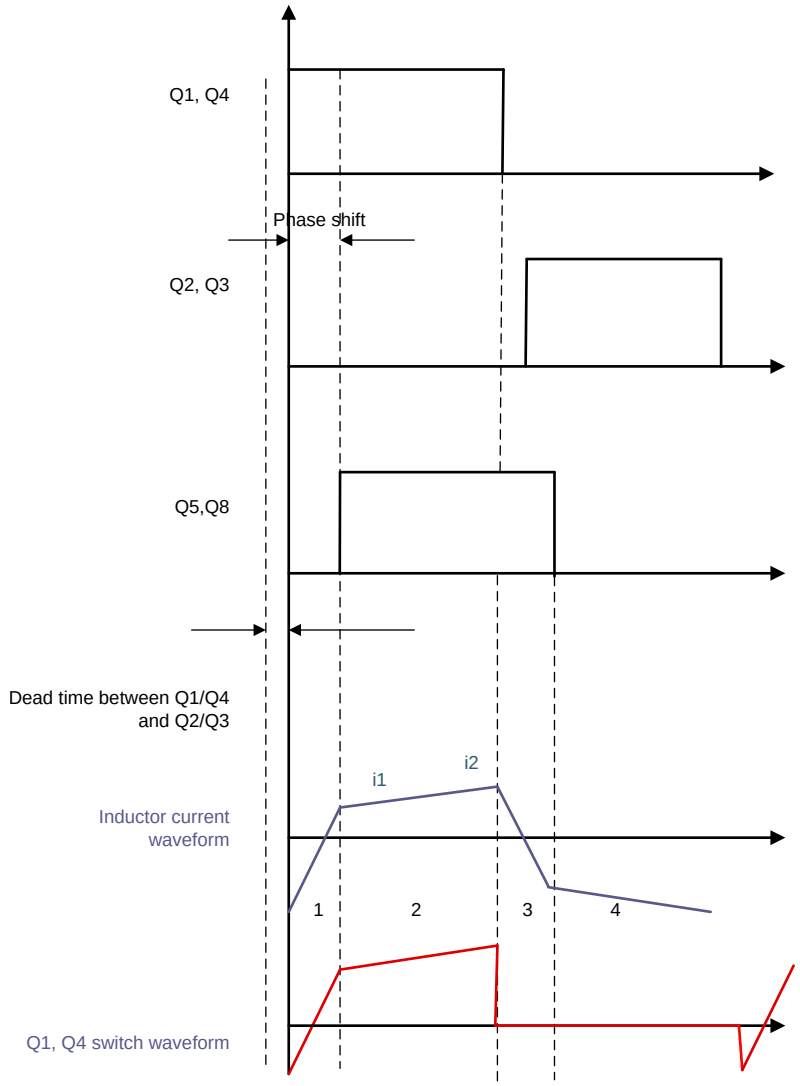
$$P_{cond\_prim} = 4\left(I^2_{switch\_prim\_rms} R_{ds\_on\_prim} + I_{diode\_prim\_avg} V_{fd_{prim}}\right) = 27\ W \quad (22)$$

Similarly, the conduction losses are calculated across the secondary side FETs by scaling the primary side RMS currents with transformer turns ratio using Equation 23 and Equation 24. The on state resistance of the secondary side MOSFET is approximately 33 mΩ.

$$I_{switch\_sec\_rms} = N \times I_{switch\_prim\_rms} = 25\ A \quad (23)$$

$$P_{cond\_sec} = 4\left(I^2_{switch\_sec\_rms} R_{ds\_on\_sec} + I_{diode\_avg\_sec} V_{fd\_sec}\right) = 95\ W \quad (24)$$

Figure 22. Switch Current Waveforms for Calculating RMS Value of Current



To calculate switching losses, the switching loss curves from the manufacturer are used. Shown in Figure 23 and Figure 24 are the switching loss curves from manufacturer for the primary and secondary side FETs.

Figure 23. C3M0030090K Loss Curves

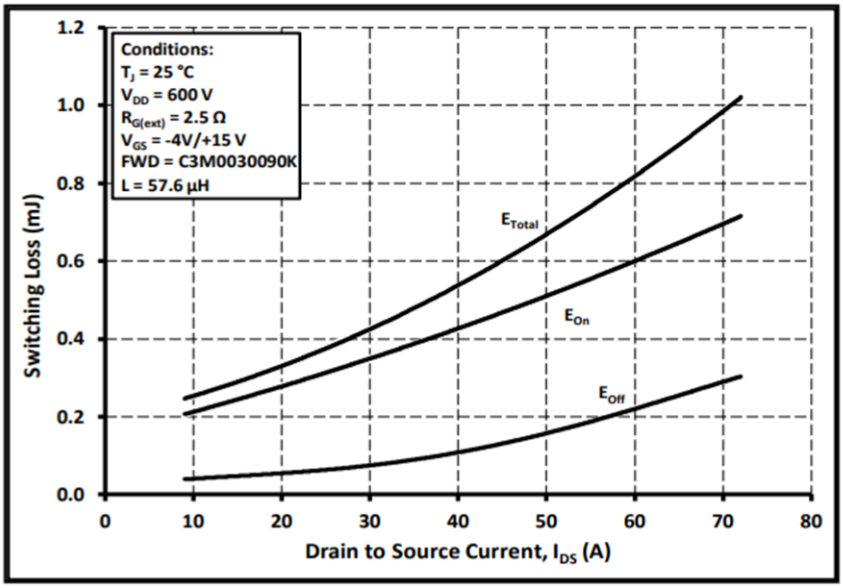
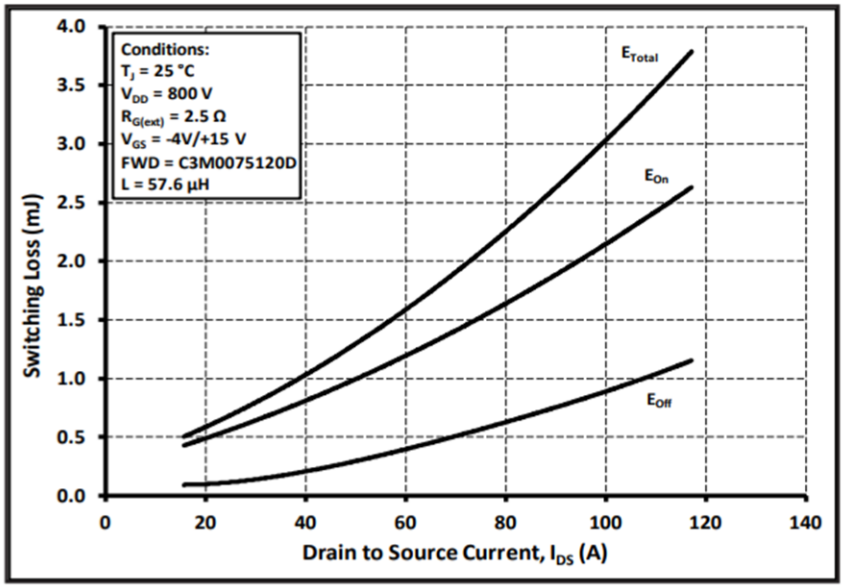


Figure 24. C3M0016120K Switching Curves



Because the FETs turn on at zero voltage, only the turn off loss coefficients are used for calculating the switching losses. Consider the secondary side MOSFETs for illustrating the calculation of switching losses. The curves are characterized during the double pulse test for a voltage of 600 V. From the graph, it can be inferred that at 50 A, the turn off energy is around 0.18 mJ. Using this information in Equation 25, the values of switching loss is obtained.

$$P_{sw\_turnoff\_sec} = \frac{F_s E_{off\_sec} I_{pk\_sec} V_{out}}{V_{nom} I_{nom} \pi} = 3.34 \text{ W} \quad (25)$$

In Equation 25, V_{out} is the maximum secondary voltage at 500 V, I_{pk_sec} is the maximum current in the secondary at approximately 35 A, F_s is the switching frequency, E_{off_sec} is the turn off loss coefficient, and V_{nom} and I_{nom} are obtained from the data sheet. Similarly, the turn off loss across the primary is calculated in Equation 26.

$$P_{sw\_turnoff\_prim} = \frac{F_s E_{off\_prim} I_{pk\_sec} V_{in}}{V_{nom} I_{nom} \pi} = 3.85\ W \quad (26)$$

Total turn off switching losses in the primary and secondary side across all eight switches comes to 36 W. In addition to these losses, two switches of the primary turn on at non-zero voltage, leading to switching losses during turn. This is because the inductor stored energy (0.5 Li^2) at this point is not fully sufficient to discharge the capacitive energy (0.5 CV^2) at the output of the MOSFETs. These losses are calculated in the same way as calculated previously, but the turn on loss coefficients are taken. These losses come to approximately 24 W across both of the switches.

$$P_{sw\_turnon\_prim\_nonZVS} = \frac{F_S E_{on\_prim} I_{pk\_prim} V_{in}}{V_{non} I_{nom} \pi} = 6.13\ W \quad (27)$$

2.3.5.3 Transformer Losses

The purpose of this section is to give an estimate of the different components of transformer loss. Transformer for this design was done with the help of Payton Planar Magnetics. This reference design focuses only on the loss of numbers and not the actual design process of the transformer. To select the core for this transformer, the area product approach is considered. The area product of the transformer is calculated by Equation 28.

$$A_p = \frac{P_o \left(1 + \frac{1}{n}\right) 10^4}{K_f K_u B_m J F_{sw}} = 17.57\ cm^4 \quad (28)$$

Where,

- Kf is the waveform factor
- Ku is the utilization factor
- Bm is the maximum flux density
- Fsw is the switching frequency
- Po is the power output of the converter
- n is the efficiency
- J is the current density

Substitute the values for flux density as 0.2 T, switching frequency as 100 Khz, and utilization factor as 0.3 as this is a planar design. With a waveform factor of 4, current density as 400 A/cm^2 we get the area product as 18 cm^4. Choosing a core with area product greater than the calculated value, E64/18/50 ferrite DMR44 core was chosen.

Next, the number of turns required for the primary and secondary side is calculated. The number of primary turns is calculated using Equation 29.

$$N_p = \frac{V_{in} 10^4}{K_f B_m A_e F_{sw}} = 22 \quad (29)$$

From the data sheet for the core, the effective core area, A_e, is 516 mm^2. By substituting this value, the number of turns is approximately 22. In a practical implementation, the number of turns selected in the primary was 24. By using the required conversion ratio of 1.6 between the primary and secondary, the number of secondary turns, N_s, is 15 turns.

Figure 25 shows the parameters of the core obtained from the data sheet. The core loss per unit of volume, P_v, at 100°C is approximately 300 mW/cm^3. The core volume, A_e, is 81.9 cm^2. Therefore, the total core loss at 100 kHz is given by Equation 30.

$$P_{Core\_loss} = P_v A_e = 24\,W \quad (30)$$

Figure 25. Transformer Core Data

DMR44材料特性・DMR44 Material Characteristics

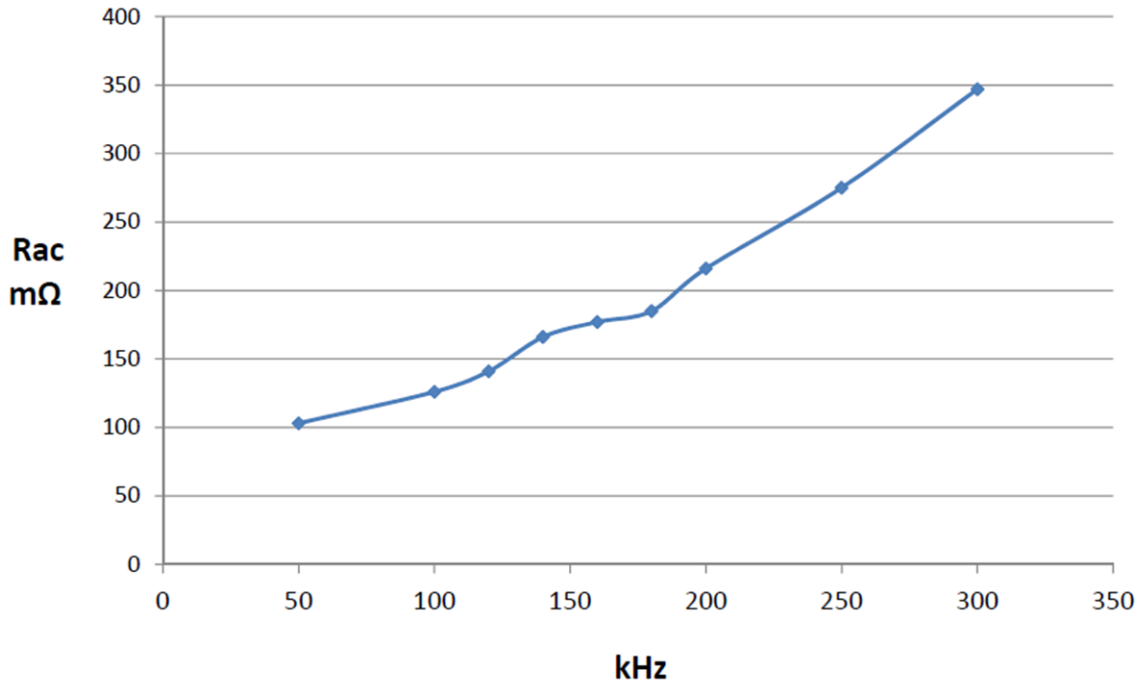
特性 SYMBOL	测试条件 CONDITIONS		典型值 VALUE
初始磁导率 μi Initial permeability	10kHz,B<0.25mT	25℃	2400 ± 25%
饱和磁通密度Bs (mT) Saturation flux density	50Hz, 1194A/m	25℃	510
		100℃	400
剩磁 Br(mT) Residual magnetic flux density		25℃	110
		100℃	60
矫顽力Hc(A/m) Coercive force		25℃	15
		100℃	6
功耗Pv(mW/cm³) Power loss	100kHz, 200mT	25℃	600
		60℃	400
		100℃	300
		120℃	380
居里温度Tc (℃) Curie temperature	10kHz,B<0.25mT		> 215
电阻率 ρ (Ω・m) Resistivity		25℃	2.0
密度d(g/cm³) Density		25℃	4.8

From the manufacturer's data sheet, the primary and secondary winding DC resistances were 43 mΩ and 16 mΩ respectively. The copper losses in the windings were calculated as per Equation 31.

$$P_{Copper} = I^2_{prim\_rms} R_{dc\_prim} + I^2_{sec\_rms} R_{dc\_sec} = 20.5\ W \quad (31)$$

Losses due to the AC resistance at high frequencies are also arising as a result of the skin effect. At 100 kHz, Figure 26 shows that the AC resistance is approximately 12.5 mΩ. These contribute 8 W of loss due to currents flowing in the primary and secondary windings.

Figure 26. AC Resistance



$$P_{ac\_loss} = I^2_{prim\_rms} R_{ac\_prim} + I^2_{sec\_rms} R_{ac\_sec} = 10\ W \quad (32)$$

The core loss, copper losses, and skin effect losses together contribute 50 W of transformer loss. The 10-KW planar transformer designed with Payton is summarized in Table 3:

Table 3. Transformer Specifications

Functional specifications	Ratings
Total output power	10 KW (500 V/20 Adc)
Operating frequency	100-200 Khz
Input voltage of transformer	800 V (Vout = 500 V), Bipolar Square waveform;
Volt-second product	8000 V-μsec -- for Vout = 500 V, 100 kHz;
Primary-to-secondary ratio	24:15
Primary current maximum	15 Arms (20 A peak) -- for Vout = 500 V;
Secondary current maximum	22 Arms (30 A peak) -- for Vout = 500 V;
Estimated power losses	50 W -- for Vout = 500 V, 100 kHz;
Primary winding DC resistance	43- mΩ
Secondary winding DC resistance	16- mΩ
Leakage inductance	17 uH
Magnetizing inductance	720 uH

More details of this transformer can be requested from Payton.

2.3.5.4 Inductor Losses

The inductor used for this design is a custom inductor. The required inductance for this application is an additional 15 uH as the leakage inductance provides 18 uH of inductance. To design the inductor, use the same area product approach as done in the case of the transformer.

$$A_p = \frac{LI_p^2}{B_m K_w K_c J} = 1.85\ cm^4 \quad (33)$$

The calculated value is approximately 1.85 cm^4, shown in Equation 33, where J is the current density, which is approximately 3 A/mm^2, K_c is the crest factor of the waveform, which is approximately 1.414, and K_w is the window utilization factor. Using the Magnetics Inc® data sheet, select a toroidal core with an area product higher than this value. A 0_43615TC toroidal core with an R-type material was selected for this purpose. Using Equation 34, check that the A_L value chosen from the data sheet satisfies the following inequality.

$$A_L < \frac{B_m^2 A_c^2}{I_p^2 L} \quad (34)$$

By substituting the values of the core area from the data sheet, this inequality does not hold, and hence, the number of turns must be evaluated by another approach given in Equation 35.

$$N = \frac{LI_p}{B_m A_e} = 20 \quad (35)$$

The value of N is 20 turns. For wire sizing, a number of strands of litz wire were connected in parallel to carry the required current. The required diameter of the litz wire and the number of conductors in parallel needed are shown in Equation 36 and Equation 37.

$$d = \frac{66}{\sqrt{f}} = 0.2\ mm \quad (36)$$

$$N_p = \frac{I_p}{K_c J a_w} = 188 \quad (37)$$

Value d is the penetration depth at 0.2 mm, a_w is the area of a single strand of wire, and N_p refers to the number of conductors that must be connected in parallel to conduct current. From the litz wire recommendations, a 38 AWG wire with a 0.12-mm diameter for winding the core was chosen. In substituting these numbers, the value of N_p is 188. To check if the calculations fit into the window, use Equation 38 with window utilization K_w as 0.6 and a window area, W_a, of 2.85 cm^2.

$$K_w W_a > a_w N N_p \quad (38)$$

There must be a small air gap of 3.2 mm, which is evaluated with Equation 39.

$$l_g = \frac{\mu N^2 A_c}{L} = 3.2mm \quad (39)$$

From the curves for core loss for R-type material taken from the data sheet, the approximate value of core loss can be calculated. The core volume, V_c, is 8596 mm^3, and core loss is 400 mT/cm^3, which gives core loss approximately 3.4 W. To compute the AC and DC resistances of the litz wire, the following recommendations were used. For convenience, take the number of parallel conductors, N_s, to be 200. These are bunched together in two operations and one cabling operation. The DC resistance is calculated with Equation 40.

$$R_{dc} = \frac{R_{max} 1.015^b 1.025^c}{N_s} \quad (40)$$

Where R_{max} is the maximum DC resistance of individual strands, b is the number of bunching operations, and c is the number of cabling operations. By substituting the value of R_{max} as 681.9 Ω/ft, b as 2, and c as 1, the result is R_{dc} as 3.6 Ω/1000ft. Next, calculate the ratio of AC to DC resistance from Equation 41.

$$\frac{R_{ac}}{R_{dc}} = H + K\left(\frac{N^2 D_i^2}{D_o^2}\right) G \quad (41)$$

H is the ratio of individual strands when isolated as 1, G is the eddy current factor given by Equation 42, N is the number of strands in the cable, D_i is the diameter of individual strands, and D_o is the diameter of finished cable.

$$G = \left(\frac{Di\sqrt{F}}{10.44} \right)^4 \quad (42)$$

$$\frac{R_{ac}}{R_{dc}} = 1 + 2\left(\frac{200^2\, 0.004^2}{0.094^2} \right) 2.155 \times 10^{-4} = 1.0312 \quad (43)$$

The AC resistance is therefore 3.71 Ω/1000ft or 12.2 mΩ/m. Therefore, the total AC resistance for the given length of wire around the core for 20 turns is 16 mΩ. The total AC and DC resistance loss is 15 W.

2.3.5.5 Gate Driver Losses

The power loss in the gate driver circuit includes the losses in the UCC21530 and losses in the peripheral circuitry like the gate resistors. The power losses consist of the static power loss, which includes quiescent power loss on the driver as well as driver self-power consumption when operating with a certain switching frequency. Values of the static current flowing into the V_{cc1} pin (I_{vcc1}) , V_{DDA} pin (I_{DDA}) , and V_{DDB} pin (I_{DDB}) are extracted from the data sheet.

$$P_{static} = V_{Vcc1} I_{ICC1} + V_{DDA} I_{DDA} + V_{DDB} I_{DDB} = 70 \text{ mW} \quad (44)$$

By substituting the values from the data sheet in Equation 44, the result is P_{static} losses of the gate driver around 70 mW. The other component of gate driver loss is the switching operation loss.

$$P_{sw} = 2(V_{DD} - V_{ss}) Q_G F_{SW} = 0.8 \text{ W} \quad (45)$$

By substituting the value of VDD = 15 V, VSS = -4 V, FSW = 100 KHz, QG = 211 nC in Equation 45, the switching loss comes to 0.8 W. The gate charge for C3M0016120K (primary side MOSFET) is extracted from data sheet. Similarly, for the secondary side, the switching losses are calculated to be approximately 0.33 W. Gate charge, QG, for the C3M0030090K MOSFET is 87 nC and is obtained from the data sheet. Also during turn on and turn off of the MOSFETs, losses occur in the gate resistors. The turn on and turn off gate resistors are 5.11 Ω and 1 Ω. These resistors are chosen to dampen out the oscillations at the gate. The gate driver IC can source 4 A and sink 6-A peak current during the switching process. Taking an average value of this current pulse over a switching cycle, the turn on and turn off losses occurring in the gate resistors is given by Equation 46.

$$P_{cond} = I_{on}^2 R_{on} + I_{off}^2 R_{off} = 0.5 \text{ W} \quad (46)$$

This value comes to 0.5 W across one switch. Thus, the total losses occurring in the four gate driver cards is 10 W.

2.3.5.6 Efficiency

Table 4 summarizes the loss numbers from the previous sections and computes the theoretical efficiency at 10 KW.

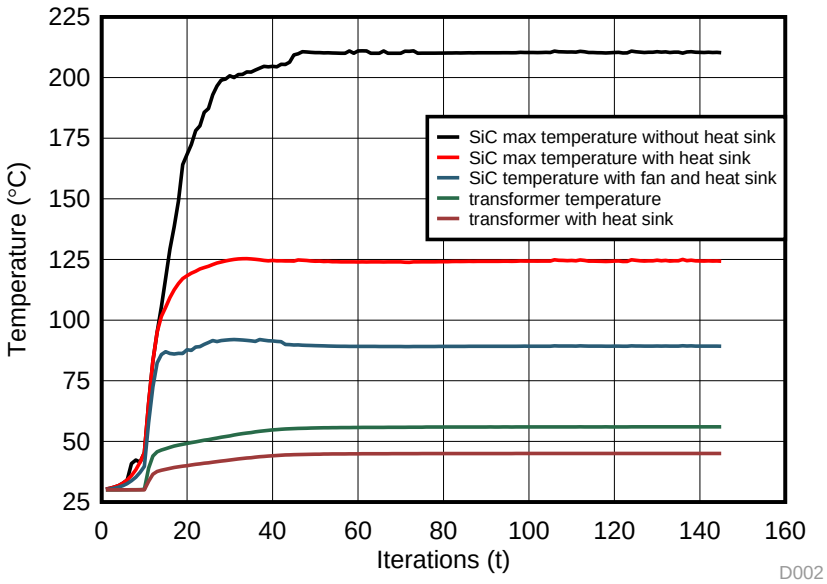
Table 4. Loss Analysis

TYPE OF LOSS	LOSS (Watts)
SiC conduction loss in primary and secondary side	112
SiC turn off switching loss	36
SiC non-ZVS turn on loss	24
Transformer loss	50
Gate driver loss + shunt resistor losses	12
Inductor loss	15
Efficiency	97.5%

2.3.5.7 Thermal Considerations

The loss estimations also allow the heat output of the design to be characterized. Any electrical loss in the system is converted to waste heat. Thermal simulations were performed using the physical layout of the design by exporting a step 3D from Altium, as well as the expected energy losses. An off-the-shelf heat sink from Wakefield-Vette (OMNI-UNI-18-75) was selected to simplify the design process and provide a starting reference point for understanding the thermal performance. This data should be used as a starting point for a thermal solution and not a fully validated solution. The system was simulated using a worse-than-calculated thermal output of 25 W per switching device. This meant that 200 W of total power dissipation across all of the switches and an additional 75 W across the capacitor, transformer, and leakage inductor. Figure 27 shows the thermal simulation results.

Figure 27. Simulated Temperature Versus Time



This simulation shows that the maximum junction temperature of the SiC MOSFETs, when run without heat sink close to the rated load of 10 KW, is approximately 210°C. When the heat sink is mounted to the FETs, the temperature rise is limited to 125°C. On using active airflow, the maximum temperature of the MOSFETs is contained to 90°C. Similarly, the transformer temperature is approximately 55°C without heat sink and around 45°C with heat sink.

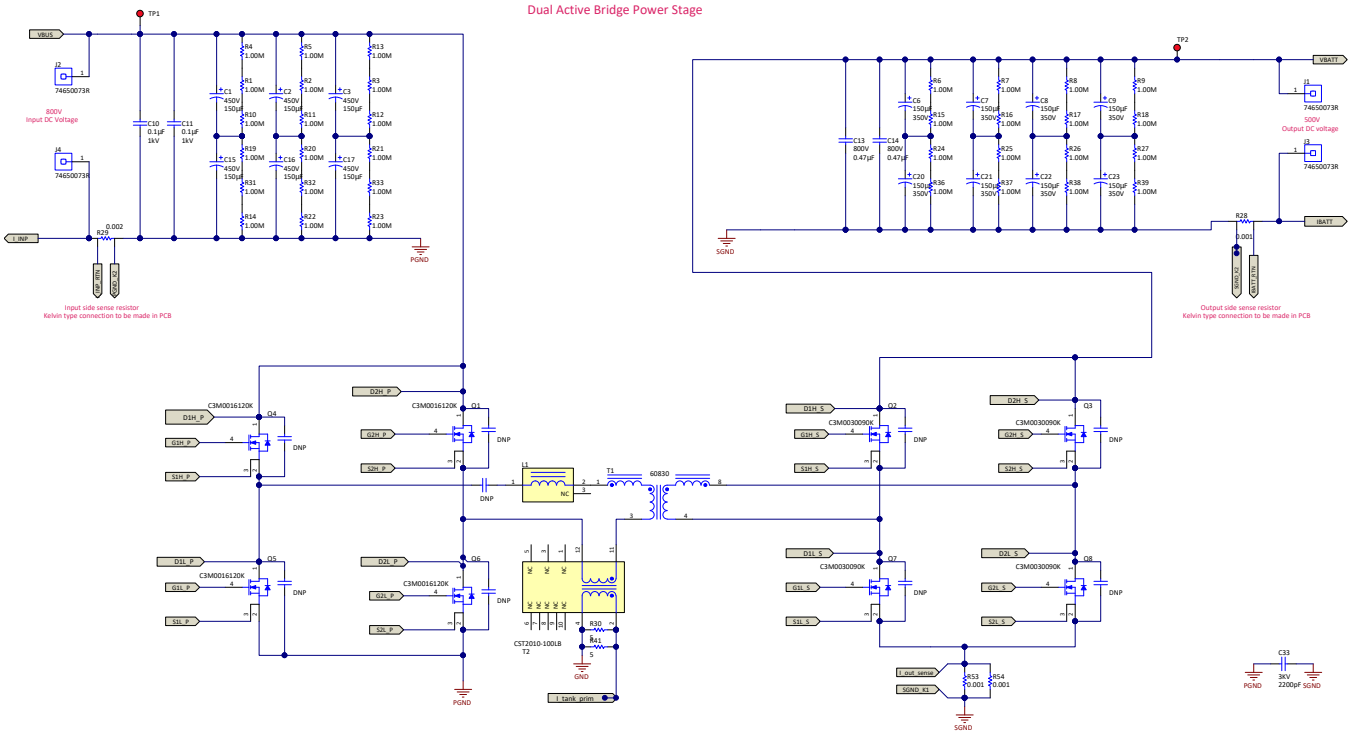
In tests conducted at 10 KW, the maximum temperature recorded in the hard switching SiC MOSFET of the primary side was approximately 55°C, and the temperature on the secondary side SiC MOSFETs were approximately 35°C because of ZVS turn across all of them. The transformer temperature was approximately 40°C with heat sink. The measurements were taken using thermal imager under forced air cooling for the SiC MOSFETs alone.

3 Circuit Description

3.1 Power Stage

Figure 28 shows the power stage of a single-phase, dual-active bridge. The primary side consists of 1200-V, 16-mΩ silicon carbide FETs (C3M0016120K) to block a DC voltage of 800 V, and the secondary side consists of 900-V, 30-mΩ silicon carbide FETs (C3M0030090K) to block DC voltage of 500 V. The full bridges are connected with a high frequency switching transformer (T1) and a power transfer inductor (L1). The components struck out in red are not populated on the board. These are output capacitances for the MOSFETs, and they can be used optionally to reduce the turn off switching losses.

Figure 28. DAB Power Stage



3.2 DC Voltage Sensing

3.2.1 Primary DC Voltage Sensing

The design implements overvoltage protection by measuring the primary and secondary DC voltages. These voltages are scaled down using a resistive divider network and fed to the MCU using the AMC1311 reinforced isolation amplifier and the OPA320. The output of the OPA320 can directly drive the ADC input or can be further filtered before processed by the ADC.

The primary voltage sensing circuit is shown in Figure 29. The maximum primary input voltage to be sensed is 800 V and is scaled down by a resistor divider network to 1.72 V, which is compatible to the 2-V input of the AMC1311. The figure shows six 1-MΩ resistors and one 13-kΩ resistor used to drop the primary voltage signal. It is then processed by the OPA320, which converts the signal in the range of 0-3.3 V as required by the ADC.

Figure 29. Primary Side DC Voltage Sense

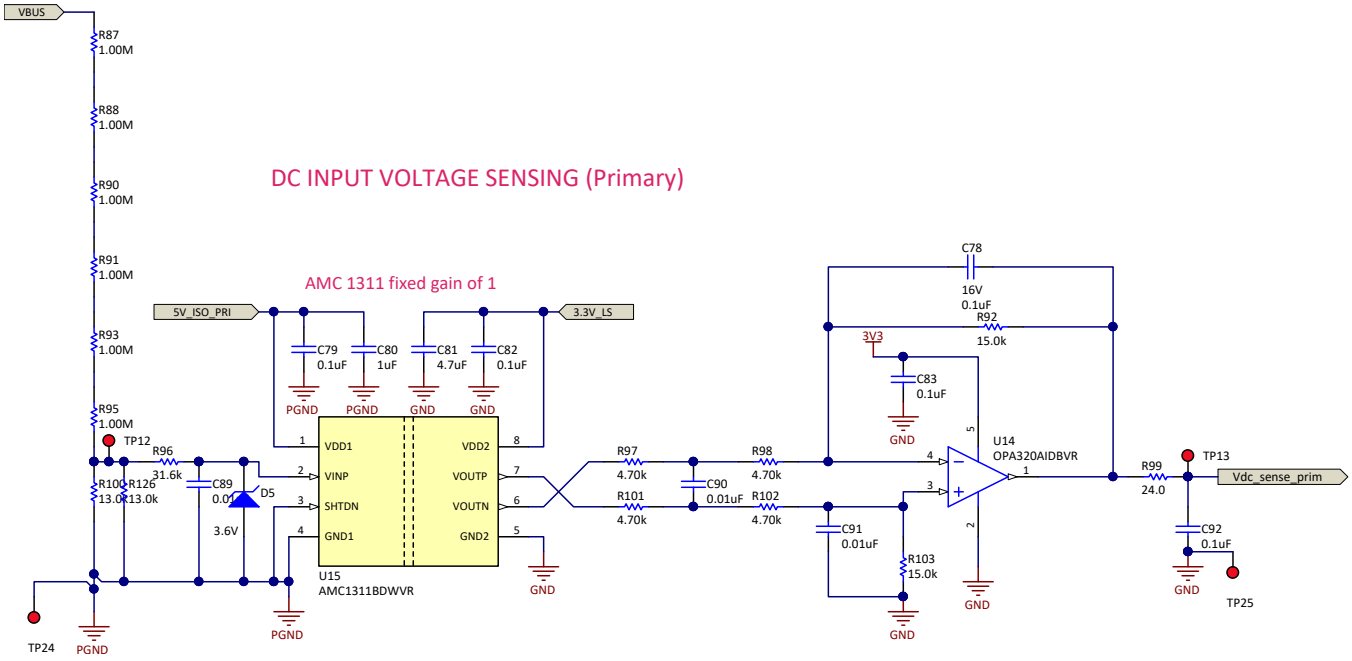
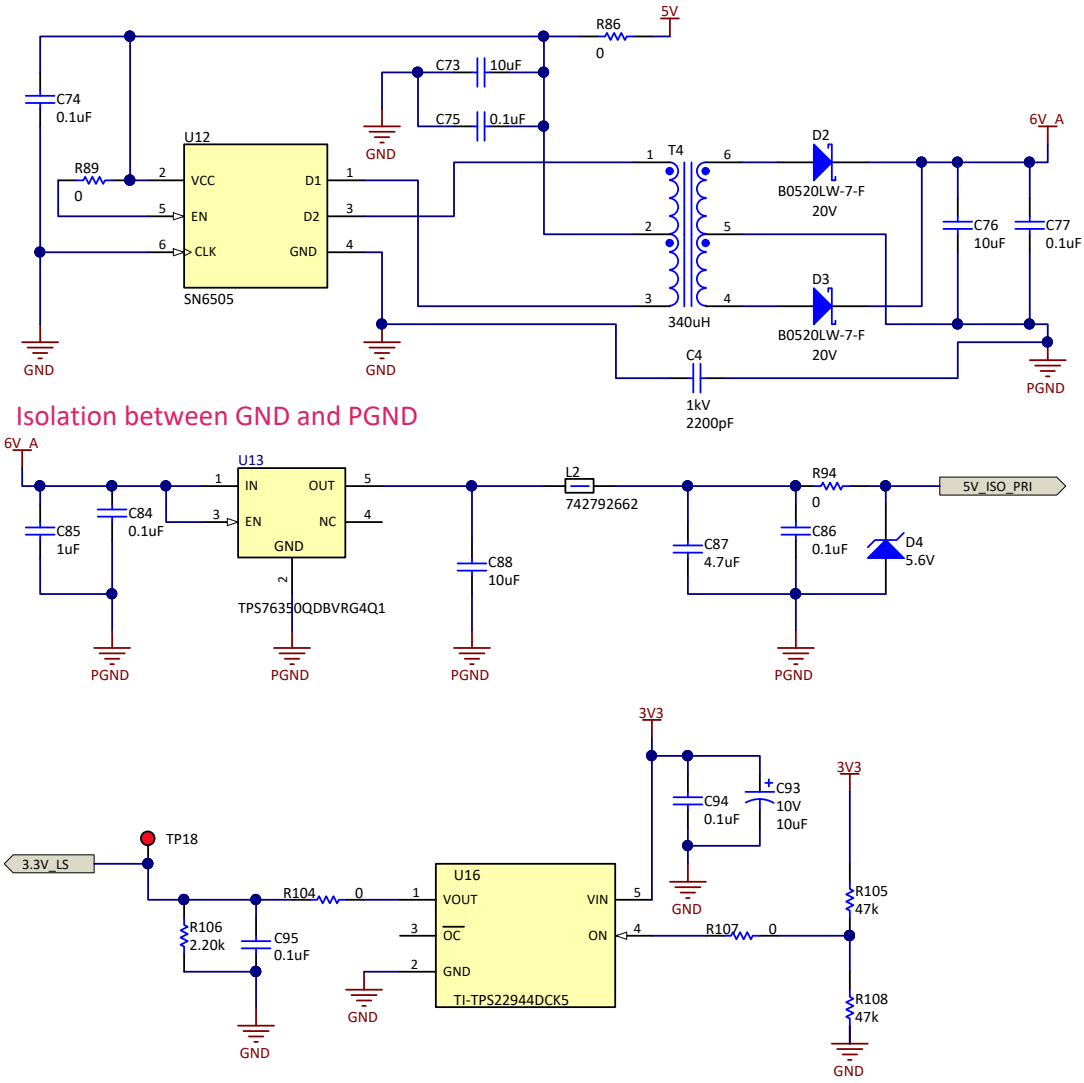


Figure 30 shows the isolated power supply circuit for powering the AMC1311. An isolated 5-V supply is needed to power the primary side of the AMC1311. This is accomplished through an SN6505 driving a push-pull transformer, which creates an isolated reference for the primary side. This isolated voltage is then regulated to 5 V using the TPS7635. The secondary side of the AMC1311 is powered with 3.3 V directly from the system power tree and is referenced to the controller GND.

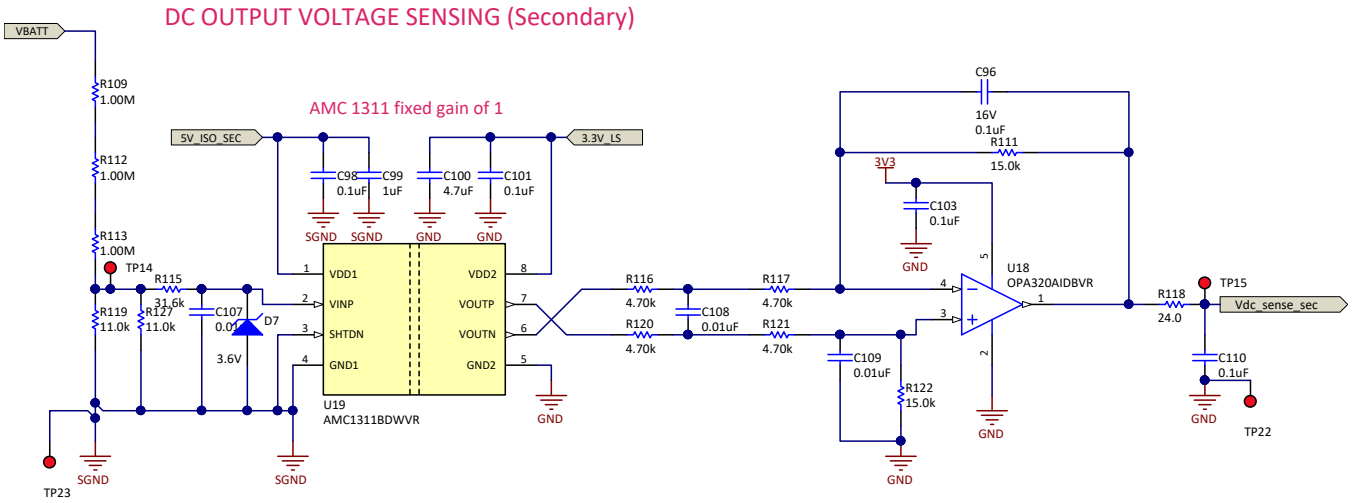
Figure 30. Isolated Power Supply for Primary



3.2.2 Secondary DC Voltage Sensing

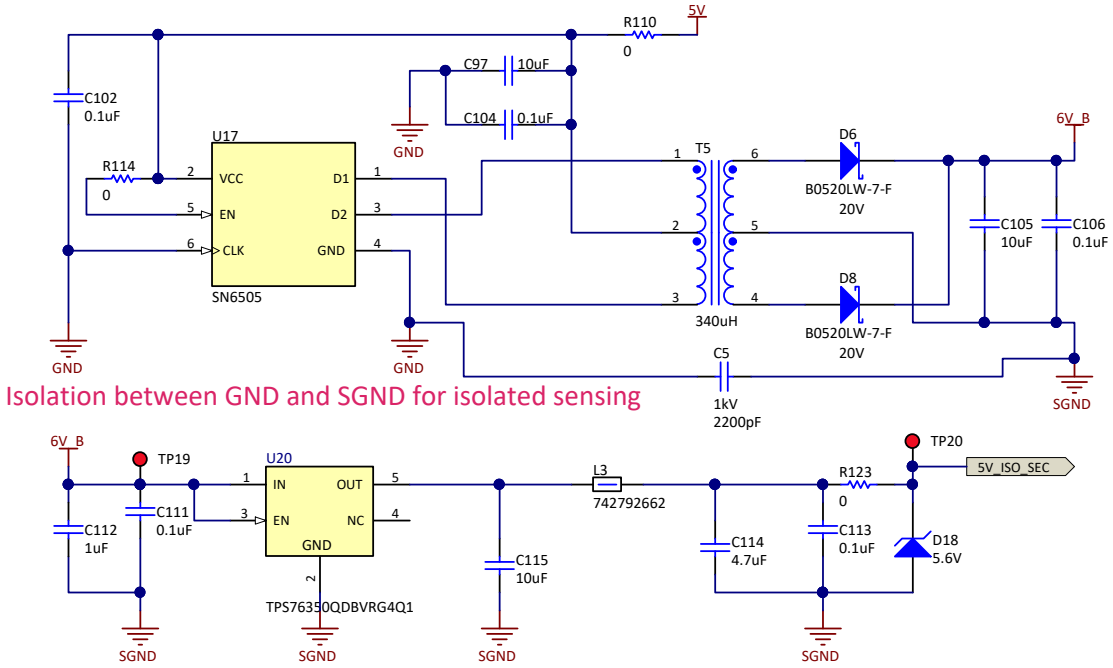
Similar to the primary side voltage sensing, the maximum secondary input voltage to be sensed is 500 V and is scaled down by a resistor divider network to 1.83 V, which is compatible to the 2-V input of the AMC1311. Figure 31 shows three 1-MΩ resistors and one 11-kΩ resistor used to drop the secondary voltage signal. It is then processed by the OPA320, which converts the signal in the range of 0-3.3 V as required by the ADC.

Figure 31. Secondary Side DC Voltage Sense



The isolated power for the AMC1311, which is used for secondary voltage sensing, is shown in Figure 32 and is the same as primary side voltage sensing.

Figure 32. Isolated Power Supply for Secondary



3.3 Current Sensing

Current sensing is important for sensing overcurrent and getting a closed loop system to work accurately. In this design, current sensing is done at multiple locations with different sensing methods. The first is on the input and output side DC terminals using current sense resistors. The measured voltage across the sense resistor is given to the input of the AMC1302. The AMC1302, with a +/- 50-mV input and a fixed gain of 41, minimizes the power loss across the shunt. The positive and negative voltages are considered for bidirectional operation of the converter. A 1-mΩ and 2-mΩ four-pin shunt resistors with kelvin sense connections are used for accurate measurement of current. The +/- 50-mV input is scaled by a gain factor of 41 to produce +/- 2.05 V. This is then scaled and level shifted (by a 1.65-V reference) by the OPA320 to match the 0-3.3 V of ADC.

Sizing the shunt resistor for this design is a tradeoff between sensing accuracy and power dissipation. A 1-mΩ shunt at the input provides a voltage drop of +/- 125 mV at 12.5 Amp, and a 2-mΩ shunt at the output provides a voltage drop of +/-40 mV at 20 Amp. Figure 33 and Figure 34 show isolated current sensing using the AMC1302. Schottky diodes are used in the input of the AMC1302 to protect the input of the devices against current overshoots. The isolated power supply to the input side of the AMC1302 is the same seen for voltage sensing in Figure 30 and Figure 32.

Figure 33. Isolated Sensing With AMC1302 in Primary

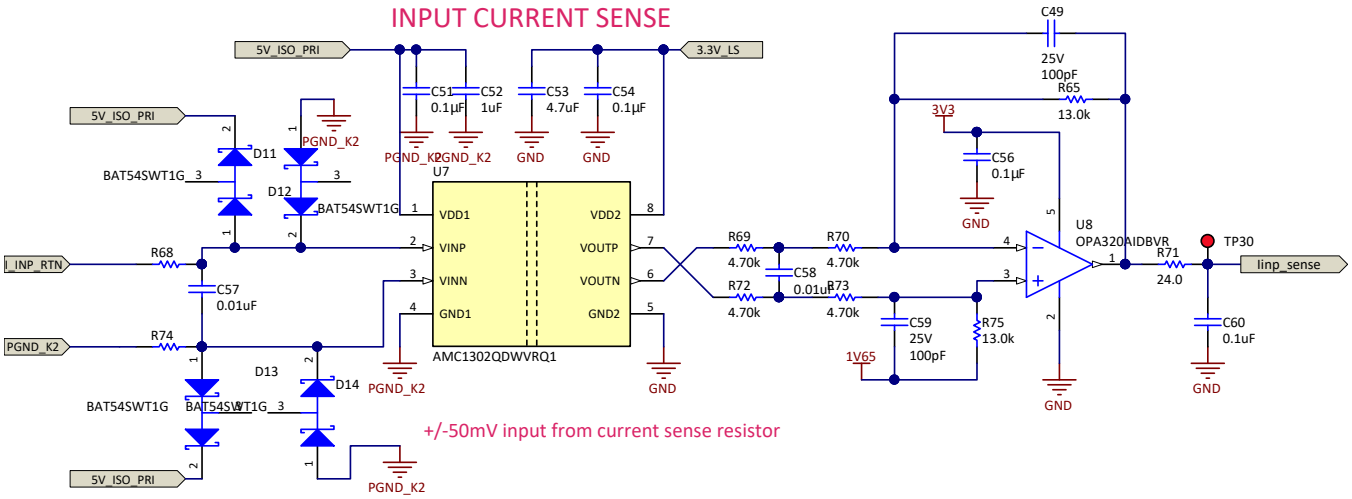
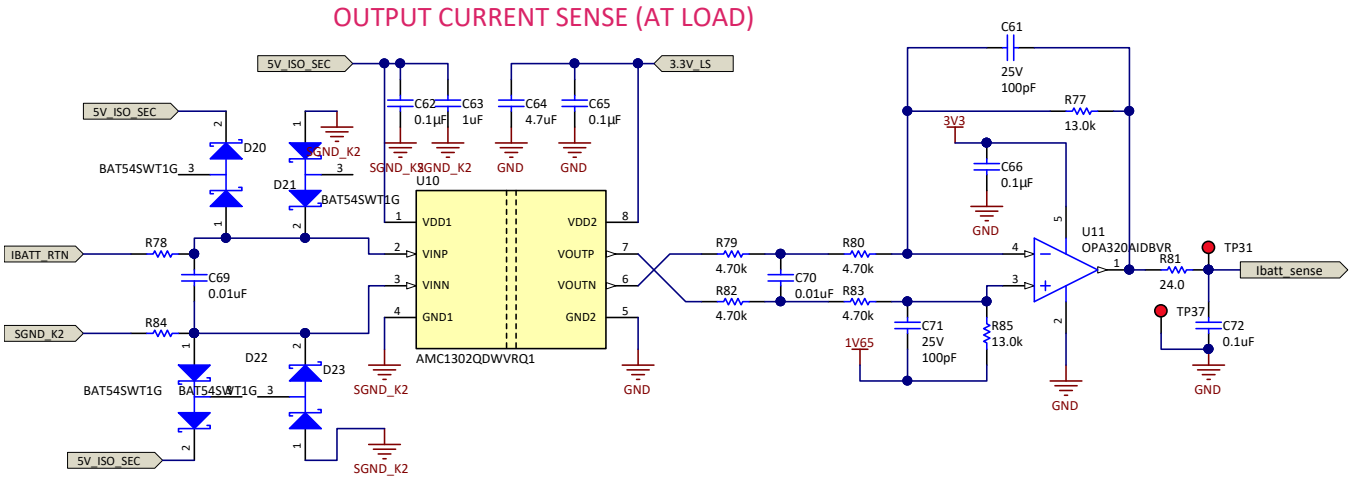
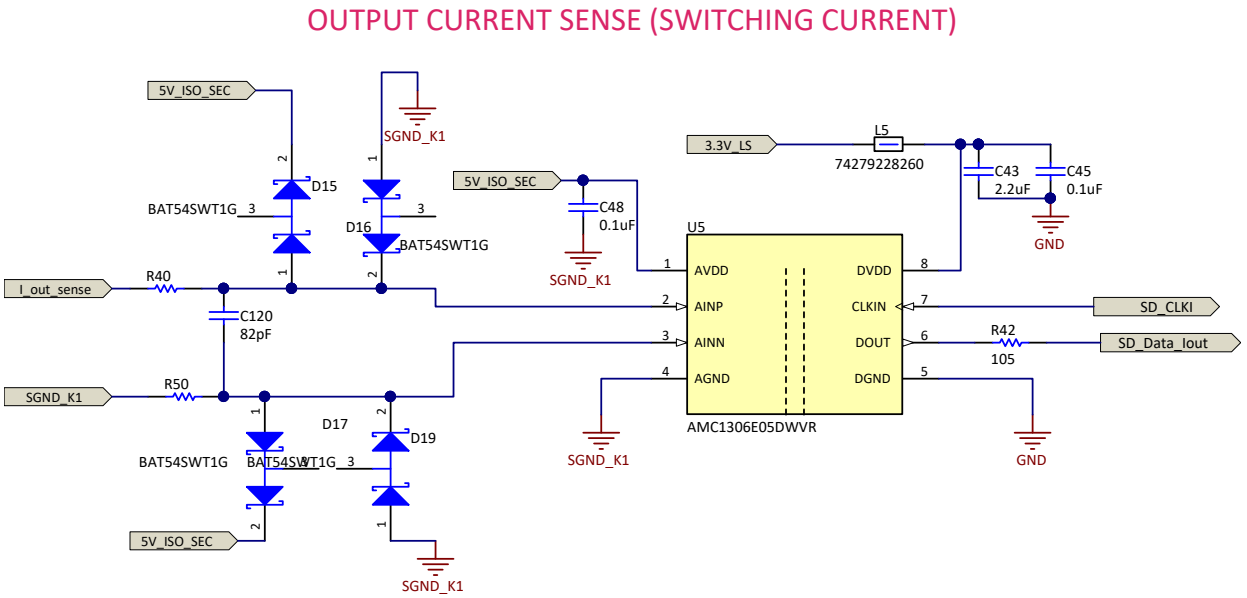


Figure 34. Isolated Sensing With AMC1302 in Secondary



To measure the switching currents across the secondary before the capacitor, the AMC1306M05 isolated reinforced modulator with a high bandwidth of 800 kHz is used. The AMC1306 has a +/- 50-mV input range, and hence, the shunt resistor can be sized with a smaller resistance value to keep the power losses low. The voltage across the shunt resistor is fed into the AMC1306M05 sigma-delta modulator, which generates the sigma-delta stream that is decoded by the SDFM demodulator present on the C2000™ MCU. Figure 35 shows isolated current sensing with the AMC1306. The clock for the modulator is generated from the ECAP/e-PWM peripheral on the C2000 MCU, and the AMC1306M05 data is decoded using the built-in SDFM modulator.

Figure 35. Isolated Current Sensing With AMC1306



There is a provision to measure primary tank current with a current transformer and the OPA320. The current transformer has a turns ratio of N = 1:100. The burden resistor across CT is chosen to produce a voltage drop of 1.4 V. In the schematic, two 5-Ω resistors are put in parallel for the purpose of redundancy. One of the resistors can be removed. The CT burden resistor is chosen according to Equation 47:

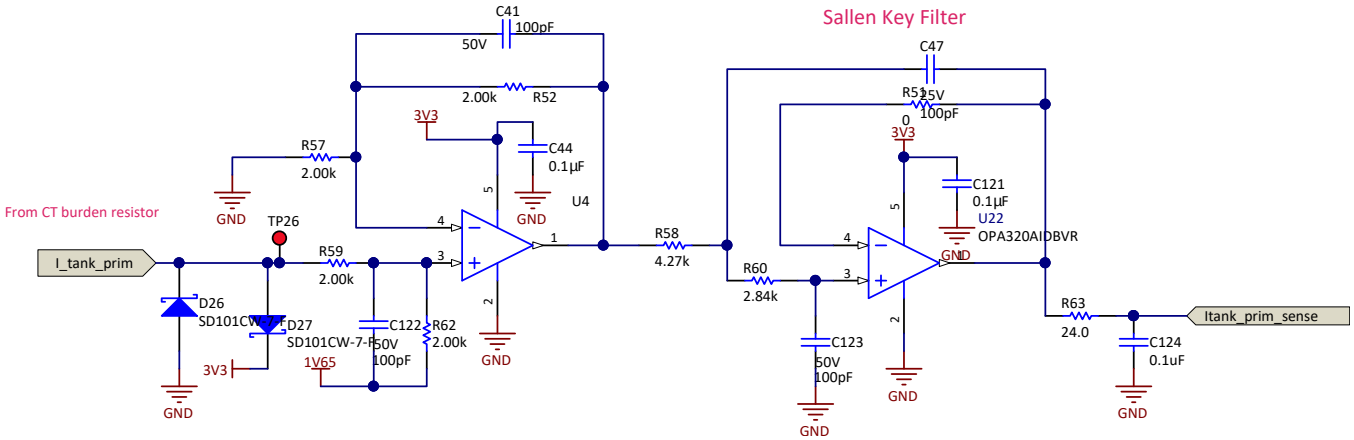
$$R = \frac{V}{NI} \tag{47}$$

Where N is the CT turns ratio, V is the allowable voltage drop across burden resistor, and I is the current in the primary winding. This bipolar voltage of +/-1.4 V is level shifted across a 1.65-V reference using the OPA320 to 0.25 V - 3.05 V, which is then fed to the ADC of the MCU through an optional filter. The signal conditioning is shown in Figure 36. The optional filter has a cut off frequency of 460 kHz given by Equation 48.

$$F_{cutoff} = \frac{1}{2\pi\sqrt{C_{47}C_{123}R_{58}R_{60}}} \tag{48}$$

This is not being used for this design, but it could be helfpful to detect peak currents.

Figure 36. Current Sense Using CT

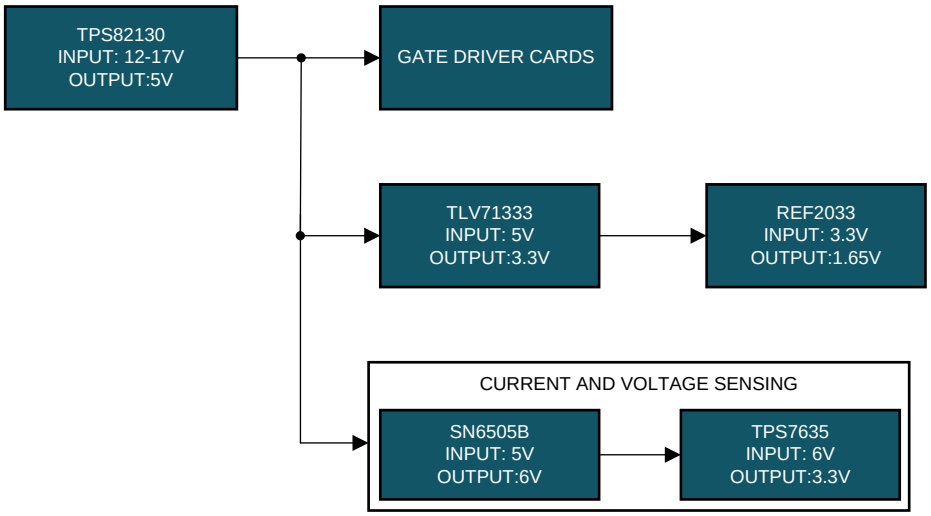


3.4 Power Architecture

Figure 37 shows the system power tree used for multiple voltage domains across the system for powering discrete components.

- A primary voltage of 17 V (bench supply) to power up the auxiliary power tree components
- 5 V to drive the gate driver cards
- Isolated 5 V to drive current and voltage sensing circuits
- Non-isolated 3.3 V for driving the current and voltage sensing circuits
- 1.65-V reference for current sense circuits

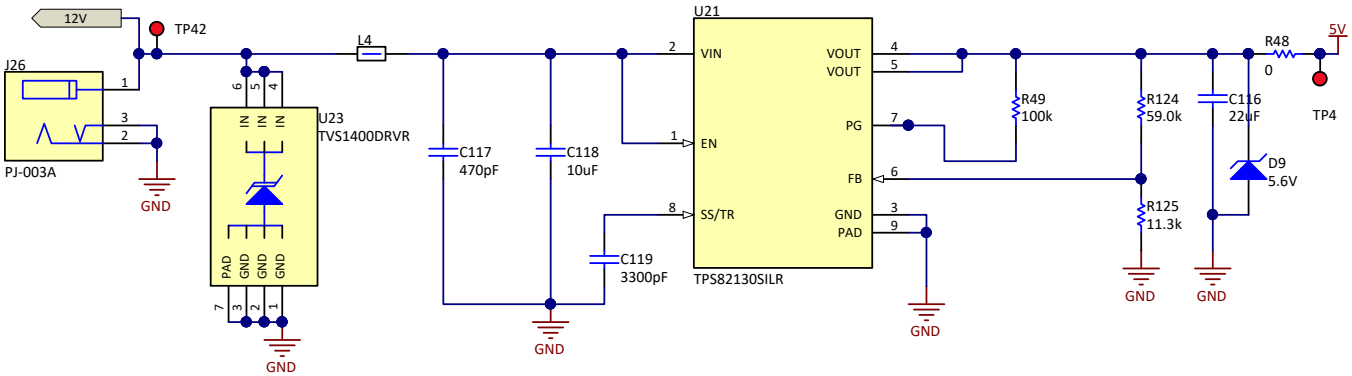
Figure 37. Power Architecture



3.4.1 Auxiliary Power Supply

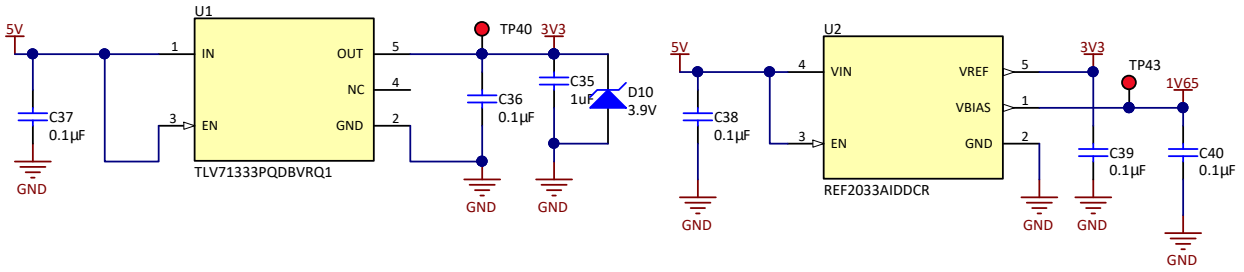
The primary voltage for powering the auxiliary circuits is up to 17 V, which is given as input to the TPS82130. The feedback resistors R124 and R125 are configured to provide an output voltage of 5 V. This 5-V rail is used to power the gate driver cards and current and voltage sensing circuits. The circuit is shown in Figure 38.

Figure 38. TPS82130 Circuit



The other rail voltages of 3.3 V and 1.65 V used to power the amplifiers and level shift the current signal are produced using the TLV71333 and REF2033 shown in Figure 39.

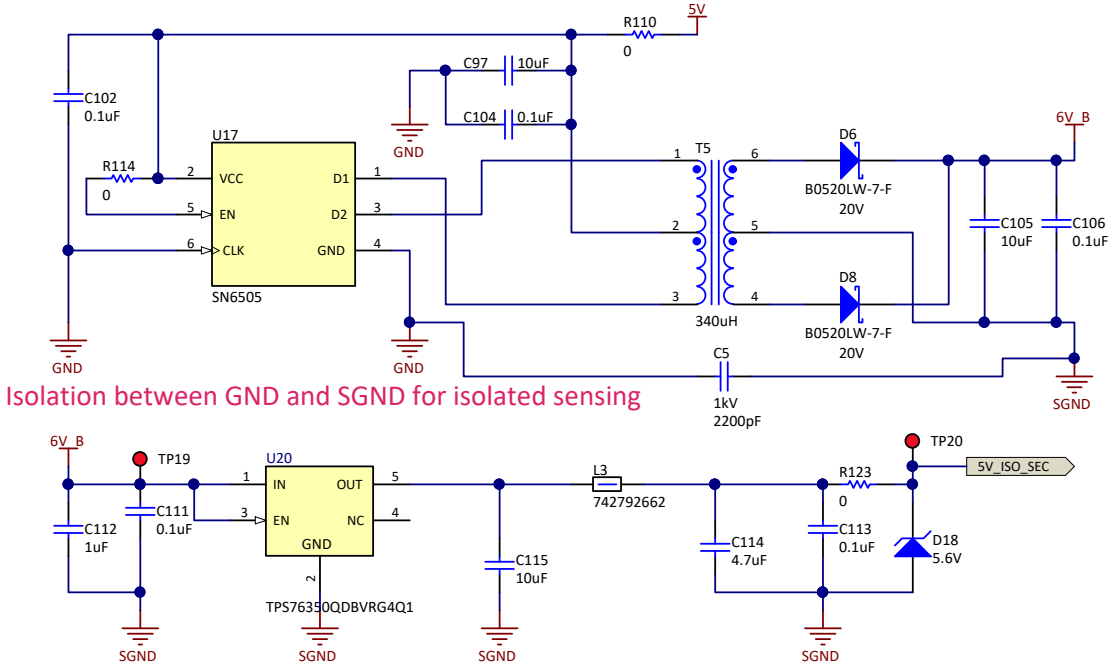
Figure 39. 3.3-V and 1.65-V References



3.4.2 Isolated Power Supply for Sense Circuits

To generate bias voltages for the AMC1311, AMC1302 and AMC1306 isolated amplifiers, the SN6505B transformer driver is used to drive a Wurth 750313638 transformer in a push-pull configuration. The output of the push-pull stage produces a voltage of 6 V. The 6-V output is fed to a TPS7635 LDO to generate an isolated 5 V for driving the isolated amplifiers as shown in Figure 40.

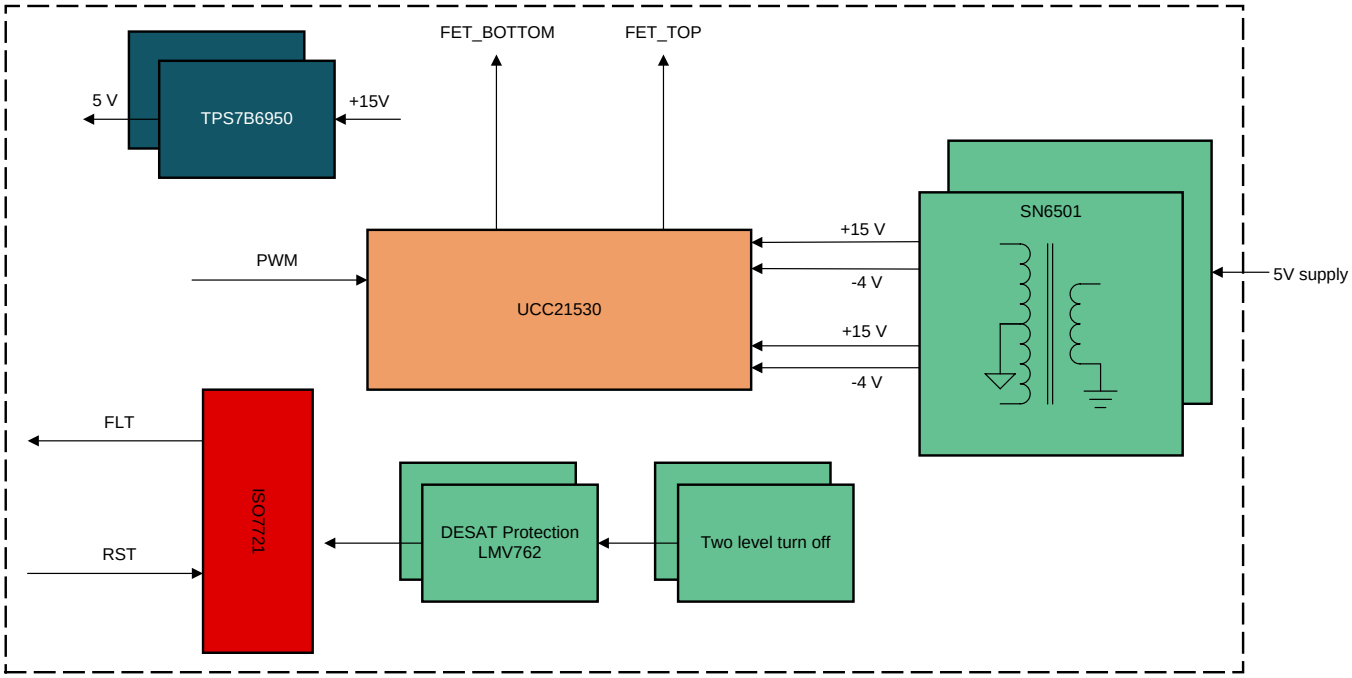
Figure 40. SN6505 Isolated Power Supply



3.5 Gate Driver

Figure 41 shows the block diagram of the gate driver daughter card inserted onto the main power board. The UCC21530 is the main gate driver driving the SiC MOSFETs of the power stage. Each block will be elaborated in detail in the following sections. For a detailed explanation on the selection of components and functionality of the UCC21530, see the Automotive Dual Channel SiC MOSFET Gate Driver Reference Design with Two Level Turn-off Protection.

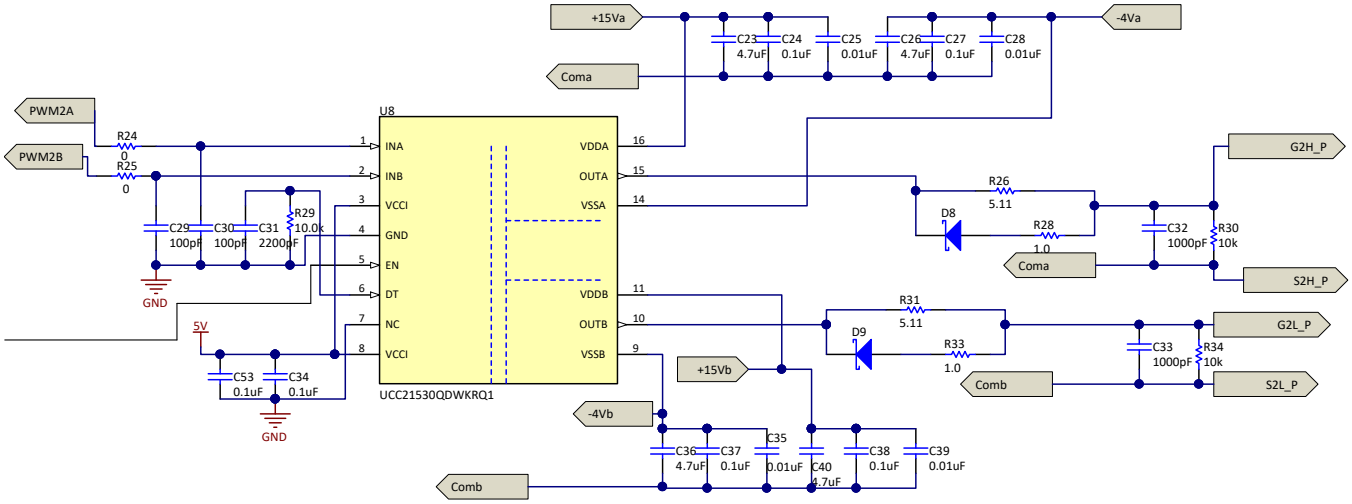
Figure 41. Gate Driver Card Block Diagram



3.5.1 Gate Driver Circuit

Figure 42 shows the schematic diagram of the isolated SiC MOSFET gate driver UCC21530. It has 5.7-KV_{rms} isolation capability between the controller side and power side switch. The UCC21530 can be configured as either two low-side gate drivers or one single-half-bridge driver. The 3.3-mm, driver-to-driver spacing enables higher DC bus voltages.

Figure 42. Gate Driver Circuit



The resistors R26 and R28 are the gate turn on and gate turn off resistors for the top SiC MOSFET, and R31 and R33 are the gate turn on and turn off resistors for the bottom SiC MOSFET. The PWM signals from the controller interface with pins INA and INB. There is also a hardware-configurable dead time provision available. The isolated bias voltages of 15 V and -4 V for driving the power stage of the gate driver is explained in the following section.

3.5.2 Gate Driver Bias Power Supply

Figure 43 shows the bias power supply voltage architecture, which enables to drive the gates across the isolation barrier. There are a total of 4 gate driver cards driving the primary and secondary side FETs. Each gate driver card consists of two bias voltage generators: one for driving the top-side FET and the other for driving the bottom-side FET. Overall, there are 8 bias supplies across the 4-gate driver boards used for this reference design. Figure 44 shows the implementation of the gate drive bias power supply.

Figure 43. Gate Driver Bias Supply Architecture

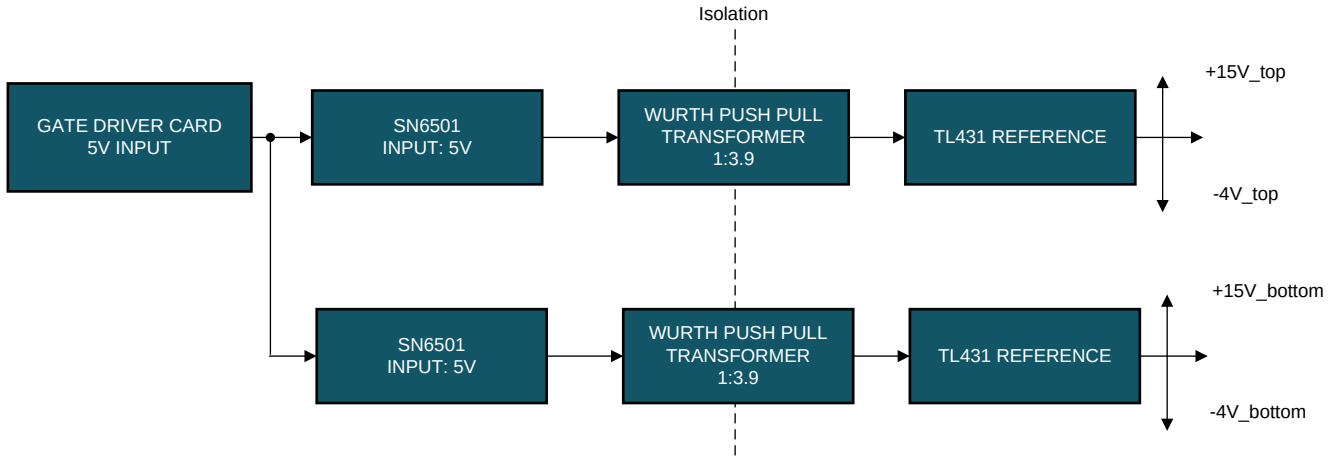
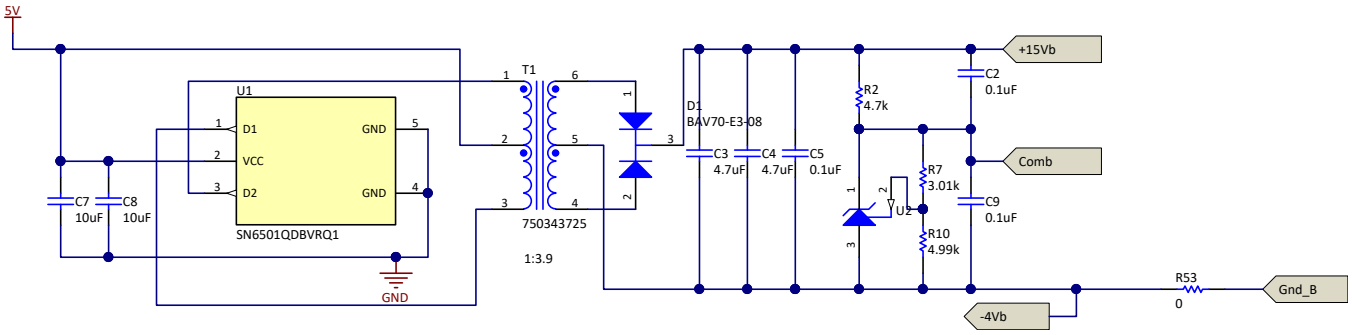


Figure 44. Gate Driver Bias Supply Circuit



The 5 V across the primary is translated to approximately 19 V in the secondary with a transformer turns ratio of 1:3.9. This is then separated into a positive rail of 15 V and negative rail of -4 V using the TL431 shunt regulator. The resistors R7 and R10 create a voltage reference of 4 V according to Equation 49.

$$V_{ref} = \left(1 + \frac{R_7}{R_{10}}\right) V_{shunt} \quad (49)$$

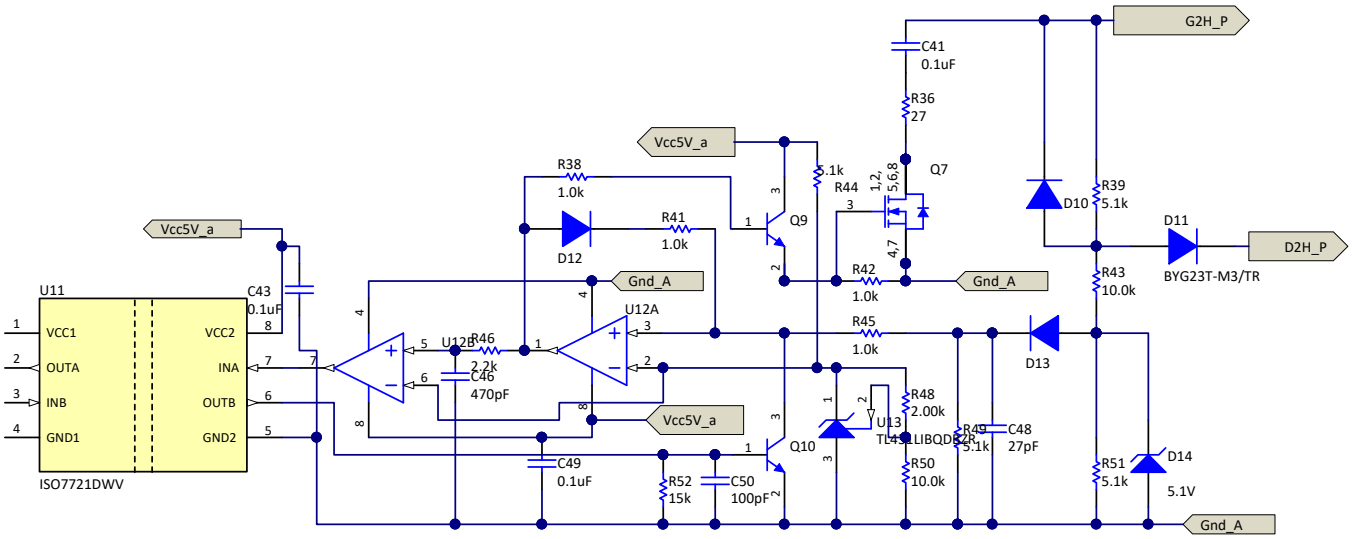
The shunt regulator reference voltage is 2.5 V.

3.5.3 Gate Driver Discrete Circuits - Short Circuit Detection and Two Level Turn Off

SiC MOSFETs work in the linear region during normal operation. Unlike IGBTs, which have a sharp transition from saturation to active region, SiC MOSFETs have a large linear region and do not have a sharp saturation behavior under conditions with excessive currents. The transition to saturation region happens at significantly high drain source voltage (V_{ds}) and the drain current (I_d) reaches significantly high value, which can be as high as 15 times the normal current and can blow out the device. A DESAT detection circuit is necessary to detect this condition and protect the SiC MOSFET.

Figure 45 shows the circuitry for detecting short circuits. The diode, D6, interacts with the high-voltage drain pin of the MOSFET. At the start of the short circuit, the current flowing in the MOSFET channel increases dramatically until saturation, and the voltage from drain-to-source also increases and can reach up to the DC bus voltage. The voltage built up across C14 is compared with a voltage reference (3 V) set by the shunt regulator TL431 using the LMV762, which triggers the protection stage to shut down gate driver IC. See the Automotive Dual Channel SiC MOSFET Gate Driver Reference Design with Two Level Turn-off Protection for details on working with this circuit.

Figure 45. Short Circuit Detection of SiC



In the event the SiC experiences a short circuit, it is detected and turned off. During the turn off process, the voltage overshoot can exceed the breakdown down voltage of the device and can destroy the switch completely. To avoid this, a two-level turn off process is initiated where the SiC MOSFET, instead of completely turning off in one shot, is made to turn off at two levels. This helps in preventing overshoot across the switch and keeps it within the safe operating area. Figure 51 shows the circuit for the two-level turn off process where a dual comparator, LMV762 (U4A and U4B), is used to initiate turn off by discharging the capacitors of the gate at two voltage levels. The capacitor C1 and R1 form an RC circuit which discharges the gate to a lower voltage level during turn off. The resistor R14 and C11 are used to set the delay time between the turn off transitions.

4 Hardware, Software, Testing Requirements, and Test Results

4.1 Required Hardware and Software

4.1.1 Hardware

The hardware for this reference design is composed of the following boards:

- One TIDA-010054 power board
- Four TIDA-010054 gate driver cards
- One TMDSCNCD280049C control card
- Mini USB cable
- Laptop

The following test equipment is needed to power and evaluate the DUT:

- 10-KW DC source capable of delivering voltage between 700 – 800 V at required current
- 10-KW resistive load bank
- Power analyzer
- Dual channel +15-V / 4-A auxiliary bench power supply
- Oscilloscope
- Isolated voltage probes and current probes

4.1.2 Software

Code Composer Studio™ 8.x with C2000 powerSUITE and digital power SDK are used in this design.

NOTE: The software will be available at a later date following the release of this design.

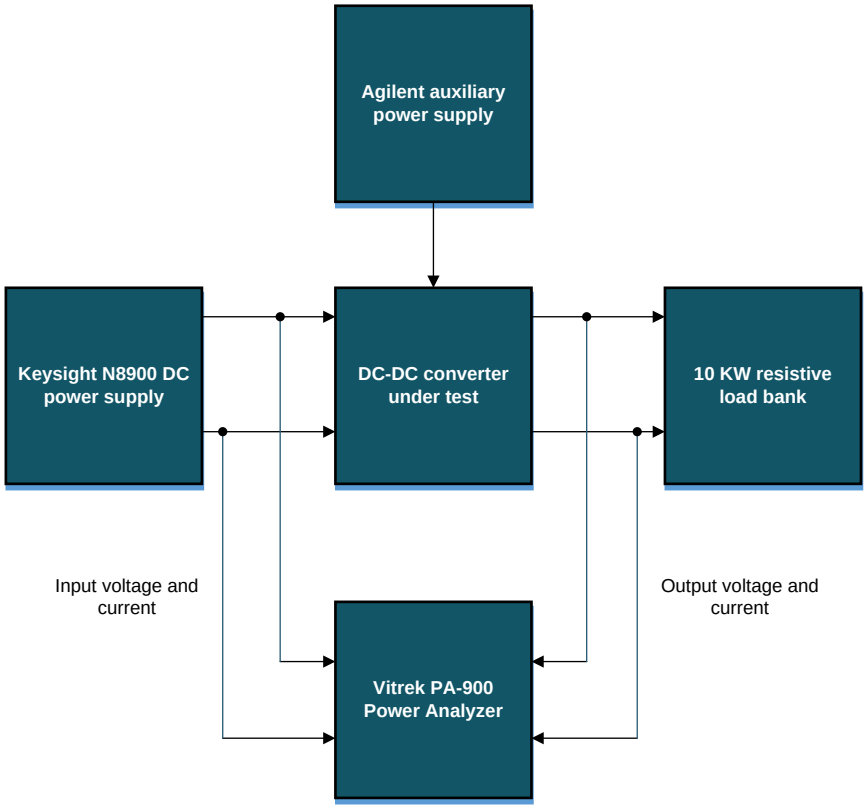
4.2 Testing and Results

4.2.1 Test Setup

To test the efficiency of this reference design, use the set up shown in Figure 46.

- Keysight® N8900 DC power supply
- Vitrek PA-900 power quality analyzer

Figure 46. Test Setup



Before powering the board to perform open-loop testing, use the following steps to set up the board.

1. Insert the four TIDA-010054 gate driver boards and the control card carefully into their respective slots.
2. Connect the terminals J2 and J4 to the input power supply and terminals J1 and J3 to the output load bank. Use a 4-mm^2 wire to make these connections so that they can handle high currents without getting heated quickly.
3. Connect the auxiliary power supply to terminal J26 using a PJ-003 female connector to power the controller, gate driver, and sense circuits.

There is a cut-out area provided at the center of the board to mount the transformer. The transformer is directly connected to the board using M3 screws. Take care while mounting the transformer so that the primary and secondary sides are not interchanged.

The control card is programmed using a USB connection from the laptop to generate PWM pulses at 100 kHz. Once programmed, the auxiliary power supply is set to 12 V. No voltage should be applied across terminals J2 and J4. When the auxiliary power supply is turned on, it should take current of approximately 550 mA.

Once the auxiliary power supply is verified, voltage is applied across terminals J2 and J4. Initially, start with a voltage of 100 V and then slowly increase the voltage in steps of 50 V until 800 V is reached. See Section 4.2.2 for the required values of phase shift to be applied for a particular load condition.

The inductor, L1, listed in the BOM is only designed to handle power up to 6 KW above which it starts getting heated. To test at 10 KW, custom inductors were used. There is a current effort to integrate the required leakage within the transformer itself, or the BOM will be updated with the custom inductor at a later date following the release of this design.

Forced air cooling using SAN ACE 40GA20 were used to remove heat from MOSFET heat sink. The capacitor C28 should be removed and should be shorted with a wire while testing. Also, capacitors C24, C25, C26, C27, C28, C29, C30, C31, and C32 are not populated on the board. These are placeholders for adding external snubbers capacitors to help to reduce turn off losses. The current design does not have these capacitors populated on board.

Table 5. Connection Details

CONNECTOR TERMINALS	FUNCTION	COMMENTS
J2 - J4	Input high voltage power supply	800-V DC power supply capable of sourcing 10-KW power
J1 - J3	Output load terminals	10-KW resistive load bank is connected here
J26	Auxiliary power supply for gate driver, control card and sense circuits	12-V DC power supply current limited to 700 mA
J5	TMDSCNCD280049C Control card	Insert the control card here
J20, J23, J29, J18	Primary side gate driver card (Leg 1)	Insert the 4 gate driver cards here
J19, J22, J15, J27	Primary side gate driver card (Leg 2)	
J12, J13, J10, J11	Secondary side gate driver card (Leg 1)	
J16, J21, J28, J17	Secondary side gate driver card (Leg 2)	

4.2.2 Test Results

Testing and implementation of the DC/DC converter is carried out in two stages:

- Open-loop testing: In this phase, the PWM waveforms were configured at a fixed frequency of 100 kHz, and the phase between the input and output bridges were varied to get the desired output voltage and power levels. The performance of the converter is quantified by measuring the efficiency at different power levels.
- Closed-loop testing: In this phase, the converter is tested for its stability and its ability to track a reference voltage with good transient performance.

4.2.2.1 Open-Loop Performance

Table 6 shows the system efficiency as a function of output power. The converter output power was varied by changing the load and the phase angle between the input and output bridge to reach 10 KW. The table shows that the converter achieves a peak efficiency of 98.2% at approximately 6 KW and has a full load efficiency of 97.6% at 10 KW. Figure 47 shows the measured efficiency of the converter at different power levels.

Table 6. Converter Efficiency Results

TESTING CONDITIONS	INPUT VOLTAGE Vin: 800 V, Switching frequency: 100 kHz, Phase shift: Between 10° to 15°, Load resistance: Decreased from 128 Ω to 34 Ω						INPUT VOLTAGE Vin: 800 V, Switching frequency: 100 kHz, Load resistance: 26 Ω, Phase shift: Increased from 16° to 23°				
Load in Watts	500	1000	2000	3000	4000	5000	6000	7000	8000	9000	10000
Efficiency	91%	94%	97.50%	97.70%	97.90%	98%	98.16%	97.90%	97.80%	97.75%	97.60%

Figure 47. Efficiency Versus Output Power

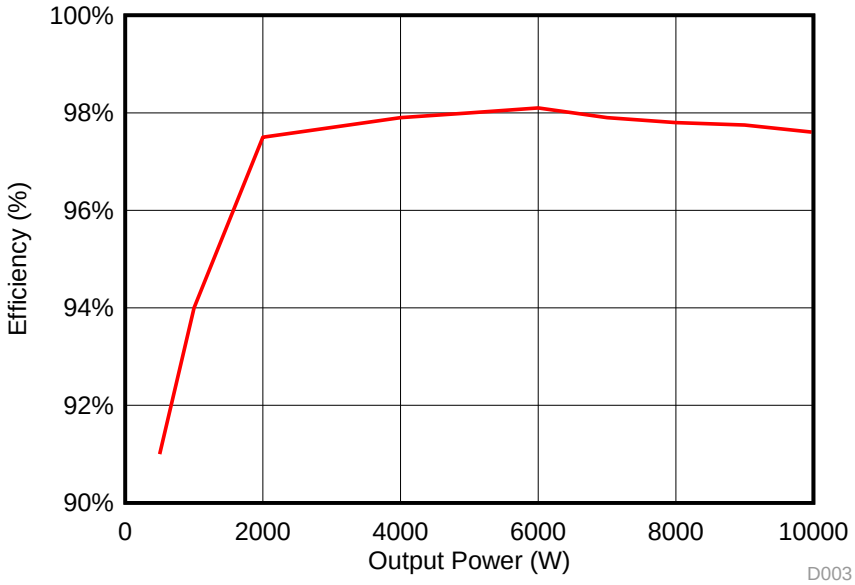


Table 7 shows the resistive loads that were used to vary the output power from light load to full load. The input voltage is kept constant at 800 V. As seen from the table, to achieve power transfer of 10 KW, the phase angle is varied by keeping the load resistance fixed at 26 Ω. For a particular power output, input voltage, output voltage, switching frequency, turns ratio, and leakage inductance, the phase angle is calculated using Equation 14.

Table 7. Results Summary

INPUT CURRENT (A)	INPUT POWER (W)	OUTPUT CURRENT (A)	OUTPUT VOLTAGE (V)	OUTPUT POWER (W)	EFFICIENCY	LOAD RESISTANCE (Ω)	OBSERVED PHASE SHIFT (deg)	ACTUAL CALCULATED PHASE SHIFT (deg)
2.47	1976	3.875	496	1922	97.3%	128	10	7
4.37	3496	7.07	483.4	3416	97.7%	68	10	7
5.51	4408	9.06	473	4286	97.2%	52	10	8.5
7.79	6232	13.42	455.6	6114	98.1%	34	15	13
8.86	7088	16.49	419.4	6916	97.6%	26	16.2	16.32
11.56	9248	18.85	479.4	9036	97.7%	26	21.6	18.9
12.62	10096	19.68	500.5	9855	97.6%	26	23	20

Table 7 shows that the observed phase shift (calculated from the PWM settings) and the actual phase shift calculated from formula varies slightly. The theoretical formula gives a good starting point to set the phase shift, but depending on the load applied to the converter, there is a requirement for fine adjustment of phase to deliver the required power. At a phase shift of 23 degrees, full power transfer of 10 KW and an output voltage of 500 V for an input voltage of 800 V at a switching frequency of 100 Khz are obtained. The closed-loop regulation of output voltage to the desired value by controlling phase is being implemented and will be available following the release of this design.

Figure 48 shows the drain voltage (dark blue), gate voltage (cyan), and inductor current (purple) waveforms of the primary side SiC MOSFET at a 10-KW power level. The drain voltage switches between zero and 800 V, the gate voltage waveform switches from +15 / -4 V, and the inductor current has a trapezoidal signature with peak current of approximately 20 A.

Figure 48. Waveforms at 10 KW

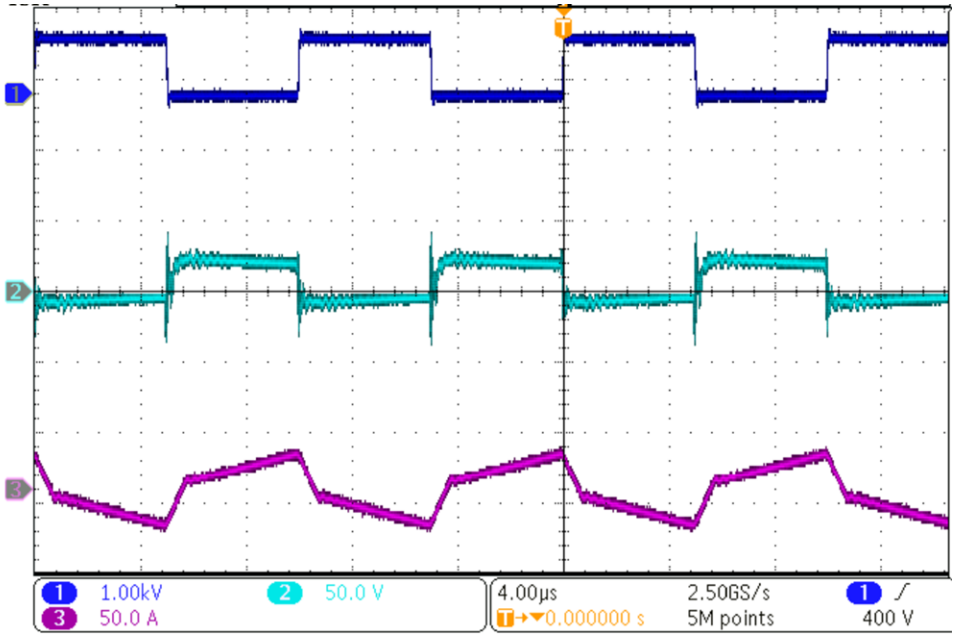


Figure 49 shows the waveforms at the instant of turn on. Gating pulses (dark blue) are applied to turn on the MOSFET once the drain voltage (cyan) falls to zero. This results in ZVS turn on of the MOSFET. Figure 50 shows the switch turn off waveform. The turn off process results in switching losses. This can be minimized by placing output capacitors across MOSFETs.

Figure 49. Switch Turn on Waveforms

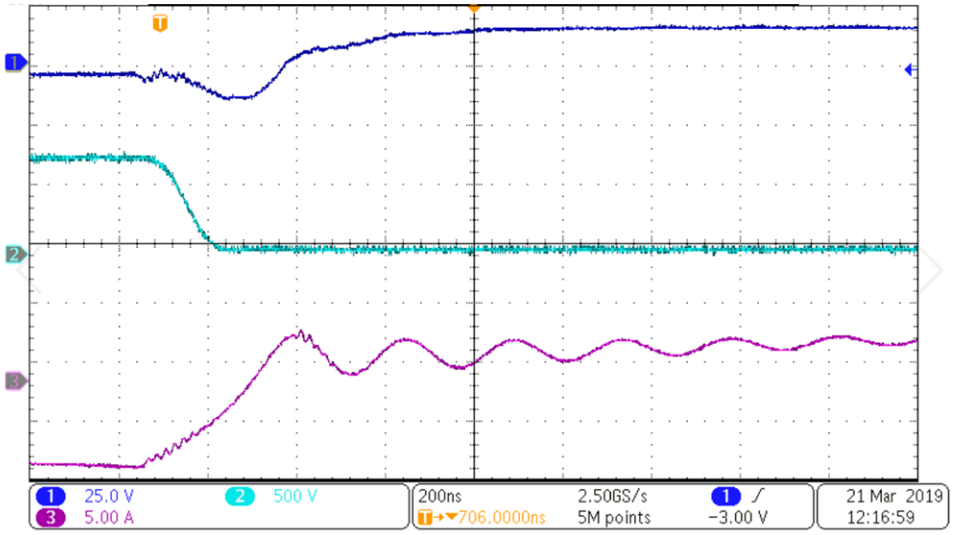


Figure 50. Switch Turn Off Waveforms

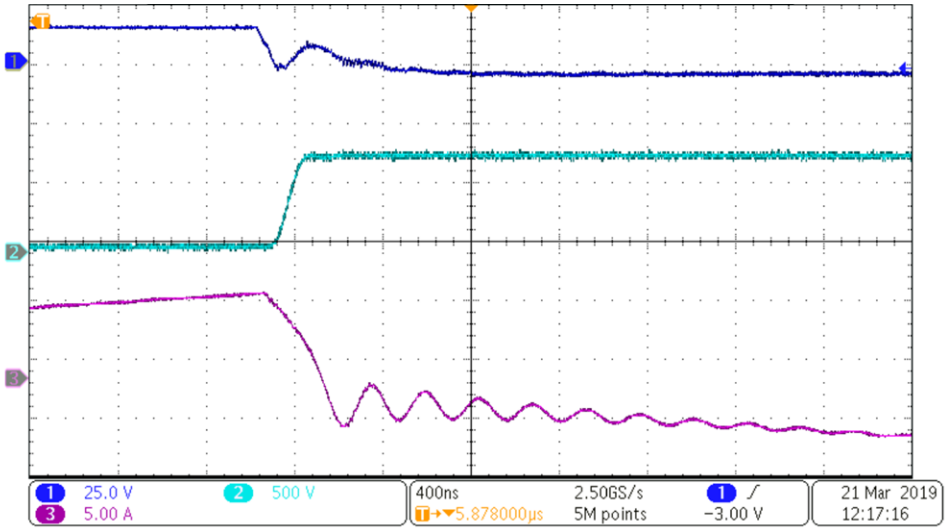


Table 8 shows the dimensions of the converter. The calculated total power density of the converter is 1.92 KW/L, which is more than our targeted specification of 1 KW/L.

Table 8. Board Dimensions

AXIS	DIMENSIONS
X	275 mm
Y	270 mm
Z	70 mm
Volume	5.2 litre

4.2.2.2 Closed-Loop Performance

To quantify the closed-loop performance, the following functional blocks have been implemented in the current design:

- Sensing of primary and secondary voltages with the AMC1311
- Current sensing with the AMC1302 and AMC1306
- Temperature sensing with the TMP235 and LMT87 for protection purposes

These functional blocks are interfaced with the F280049 MCU, where the signals can be processed to implement voltage mode or current mode control. Currently, digital control has not been implemented in this reference design. This section will be updated following the release of this reference design with test results on calibration of signal chain, stability, and closed-loop performance of the converter.

5 Design Files

5.1 Schematics

To download the schematics, see the design files at TIDA-010054.

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-010054.

5.3 PCB Layout Recommendations

5.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-010054.

5.4 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-010054.

5.5 Gerber Files

To download the Gerber files, see the design files at TIDA-010054.

5.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-010054.

6 Related Documentation

1. Texas Instruments, *Performance characterization of a high power dual active bridge dc to dc converter*
2. Texas Instruments, *Performance of a 25kW 700V Galvanically Isolated Bidirectional DC-DC Converter Using 1.2kV Silicon Carbide MOSFETs and Schottky Diodes*
3. Texas Instruments, *Modeling and Optimization of Bidirectional Dual Active Bridge DC–DC Converter Topologies*

6.1 Trademarks

6.2 Third-Party Products Disclaimer

7 Terminology

- SiC - Silicon Carbide
- DAB - Dual-Active Bridge
- ZVS - Zero Voltage Switching
- EV - Electric Vehicle
- CCS - Code Composer Studio
- V2G - Vehicle-to-Grid

8 About the Author

HARISH RAMAKRISHNAN is a systems engineer at Texas Instruments India, where he is responsible for developing reference design solutions for Grid Infrastructure.

9 Acknowledgement

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