

HD66790R

720-channel Source Driver for 262,144-color, 64-grayscale Display on Amorphous Silicon, Low-temperature Poly-silicon TFT Panel

REJxxxxxxx-xxxxZ

Rev.1.0

October.22.2004

Description	4
Features	5
Block Diagram	6
Block Function	7
(1) External Display Interface (RGB interface).....	7
(2) Control circuit.....	7
(3) Grayscale Voltage Generating Circuit.....	7
(4) Timing Generator.....	7
(5) LCD Driver Circuit.....	8
(6) VCOM amplitude generator	8
(7) Level shifter.....	8
(8) System interface clock synchronizing serial circuit	8
(9) Vci internal reference voltage generating circuit	8
(10) VciOUT output circuit	8
(11) Step-up circuit 1 (DCDC1).....	8
(12) Step-up circuit 2 (DCDC2).....	8
(13) VREG1 regulator	9
Pin Arrangement	10
PAD Coordinate.....	11
BUMP Arrangement	15
Wiring example.....	16
Pin function.....	17
Instruction	23
Index: IR	23
Power Color 1: R01h.....	23
Voltage setup 1 : R01h.....	27

<i>Voltage setup 2: R02h</i>	29
<i>Driver output control: R03h</i>	32
<i>LCD driving waveform control, Source output control: R04h</i>	34
<i>Gate output control: R05h</i>	35
<i>Display signal select control, frame control 1: R06h</i>	37
<i>γ Control – positive polarity gradient adjustment: R07h</i>	41
<i>γ Control – negative polarity gradient adjustment: R08h</i>	41
<i>γ Control – positive polarity amplitude adjustment: R09h</i>	41
<i>γ Control – negative polarity amplitude adjustment: R0Ah</i>	41
<i>γ Control – Positive polarity fine adjustment 1: R0Bh</i>	42
<i>γ Control – Positive polarity fine adjustment 2: R0Ch</i>	42
<i>γ Control – Positive polarity fine adjustment 3: R0Dh</i>	42
<i>γ Control – Negative polarity fine adjustment 1: R0Eh</i>	42
<i>γ Control – Negative polarity fine adjustment 2: R0Fh</i>	42
<i>γ Control – Negative polarity fine adjustment 3: R10h</i>	42
<i>Low Power Mode: R26h</i>	43
Instruction List	45
Reset Function	46
LCD Signal Output Timing Control Function	47
Power Control Function	48
POC, VCOMG, LSENRL output control	49
RGB Interface timing	50
<i>RGB interface timing 1 (18-bit transfer mode)</i>	50
<i>RGB interface timing 2 (6-bit x 3 transfers)</i>	51
LCD panel interface timing	52
Serial Interface	53
Data Shift Direction	54
Liquid Crystal AC Drive	55
LCD Display Signal Control	56
Grayscale Amplifier Unit Configuration	57
<i>Configuration of grayscale level generating unit</i>	58
<i>Reference voltage generating block (ladder resistor units and 8-to-1 selectors)</i>	59
<i>γ-Correction Register</i>	60
<i>Ladder resistors and 8-to-1 selector</i>	61
<i>Variable resistors</i>	61
<i>Grayscale voltage calculating formulae (Positive polarity)</i>	63

<i>Grayscale voltage calculating formulae (Positive polarity)</i>	64
<i>Grayscale voltage calculating formulae (Negative polarity)</i>	65
<i>Grayscale voltage calculating formulae (Negative polarity)</i>	66
Input/Output level relationship	67
System configuration example.....	68
Voltage Setting Pattern Diagram	69
Power Supply Setting.....	70
Sleep mode sequence	71
Internal state transition of the HD66790R	72
Absolute Maximum Ratings	73
Capacitance	73
DC Operating Condition	74
Electrical characteristics	75
<i>DC characteristics</i>	75
<i>Step-up circuit output characteristics</i>	76
<i>AC characteristics</i>	77
<i>Reset Timing Characteristics</i>	77
<i>LCD driver output characteristics</i>	79
<i>Timing diagram</i>	80
<i>Notes to Electrical Characteristics</i>	82
<i>Example of test circuits</i>	84
<i>Power supply startup, display ON sequence (reference)</i>	85
<i>Display OFF, power supply OFF sequence (reference)</i>	86
<i>Sleep sequence (reference)</i>	87
<i>Reference data</i>	88

Description

The HD66790R is a source driver LSI for 262,144-TFT-color, 720-channel graphics display, incorporating a timing controller to adjust the timing of LCD signals.

The HD66790R supports 18-bit RGB interface (via VSYNC, HSYNC, DOTCLK, ENABLE, and PD17-0) and 6-bit RGB interface (via VSYNC, HSYNC, DOTCLK, ENABLE, and PD17-12) for moving picture display. As a system interface to a microcomputer, the HD66790R supports a serial interface to manage high quality display and low power consumption drive by setting instruction.

The HD66790R allows for precise power management by software, which makes this LSI an ideal for medium or small-sized portable products supporting WWW browsers, such as digital cellular phones or PDAs, where long battery life is a major concern.

Features

- 720-channel LCD source driver circuit
- Data bits: 6-bit (grayscale) x RGB dots
- Moving picture display interface: 18-bit RGB Interface (via VSYNC, HSYNC, DOTCLK, ENABLE, PD17-0), 6-bit RGB Interface (via VSYNC, HSYNC, DOTCLK, ENABLE, PD17-12)
- Multicolor display: 262,144 colors simultaneously available
- Internal timing controller for adjusting LCD signal output timing
- System interface: Serial Interface
- Reversible source driver shift direction
- Level shifter for LCD signals
- High-speed operation: fDOTCLK = 25MHz (Max.)
- TFT display storage capacitance: Cst (C storage on Common)
- Power supply to the TFT display's common electrode
- Vcom AC drive function
- Operating power supply voltage range

Input supply voltage levels

- Logic power supply: $V_{cc} = 2.5V \sim 3.6V$
- Analog power supply: $V_{ci} = 2.5V \sim 3.6V$
- Interface power supply: $IOV_{cc} = 1.65V \sim 3.6V$

LCD drive power supply voltage levels

- Source driver power supply: $DDVDH = 4.0V \sim 5.5V$
- Gate driver power supplies: $VGH-VGL = 22.0V \sim 37.5V$
 $VGH-AGND = 12.0V \sim 20.0V$
 $VGL-AGND = -10.0V \sim -17.5V$
 $VcomH-VcomL = 4.0V \sim 5.5V$
 $VCL-AGND = 0.0V \sim -3.3V$

Output supply voltage levels

- LCD panel output level: $SOUT1-4R/L = VGL \sim VGH$
- Source output level: $S1 \sim S720 = AGND + 0.3V \sim DDVDH - 0.3V$
- Internal step-up circuit output levels: $DDVDH: VLOUT1 = V_{ci1} \times 2$
 $VGH: VLOUT2 = V_{ci1} \times 6, 7, 8$
 $VGL: VLOUT3 = V_{ci1} \times -5, -6, -7$
 $VCL: VLOUT4 = V_{ci1} \times -1$

Table 1 Product lineup

Type No.	Organization	Package
HCD667B90RBP	Laced bump arrangement	Die with BUMP

Block Diagram

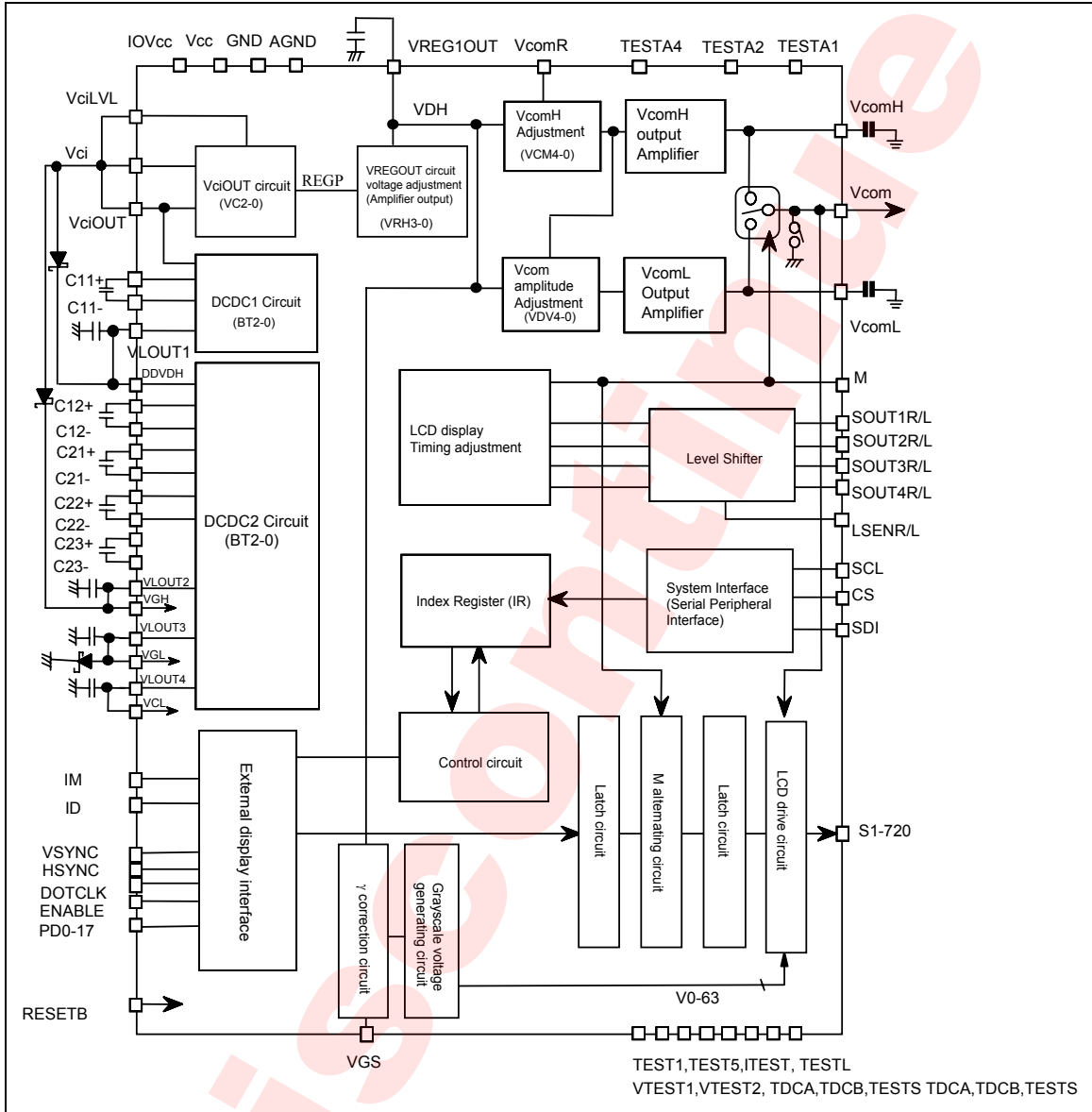


Figure 1

Block Function

(1) External Display Interface (RGB interface)

The HD66790R supports RGB interface as an external display interface. In RGB-I/F mode, the HD66790R operates in synchronization with externally supplied signals (VSYNC, HSYNC, and DOTCLK), and takes in data according to data enable signal (ENABLE). See “RGB interface timing” for details.

The correspondence between input and output data is as follows.

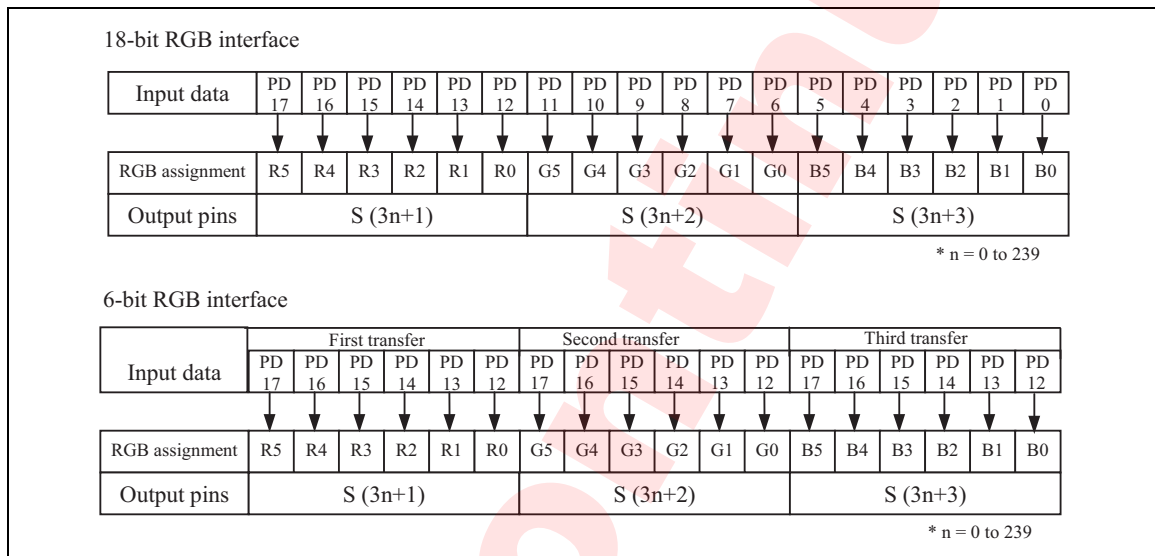


Figure 2

(2) Control circuit

The control circuit generates internal control signals from various signals.

(3) Grayscale Voltage Generating Circuit

The grayscale voltage generating circuit generates 64 grayscale voltage levels each for positive and negative polarities by dividing externally input voltages with resistors and enabling display in 262,144 colors. See “Grayscale Amplifier” for details.

(4) Timing Generator

The timing generator generates timing signals for LCD operation.

(5) LCD Driver Circuit

The LCD driver circuit consists of a 720 source-output (S1~S720) driver, latching display pattern data in units of lines and generating drive waveforms. The shift direction of source outputs can be switched between either from (S1, S2, S3) to (S718, S719, S720) or from (S718, S719, S720) to (S1, S2, S3), whichever suitable for the module.

(6) VCOM amplitude generator

The VCOM amplitude generator generates an amplitude signal VcomS to generate Vcom, which is supplied to the TFT LCD panel's common electrode. The AC voltage Vcom alternates between arbitrarily set two levels (VcomR and GND) in sync with alternating cycle signal.

(7) Level shifter

The level shifter generates gate line drive supply voltages from logic supply voltages by changing the amplitude from Vcc-GND to VGH-VGL.

(8) System interface clock synchronizing serial circuit

The system interface clock synchronizing serial circuit provides an interface to a microcomputer, enabling the HD66790R's mode setting with registers.

(9) Vci internal reference voltage generating circuit

The Vci internal reference voltage generating circuit generates an internal reference voltage REGP from Vci for generating VciOUT and VREG1OUT levels. See "Instruction" for details.

(10) VciOUT output circuit

The VciOUT output circuit outputs the VciOUT level, which is input to the step-up circuit 1 (DCDC1) from Vci1 pin. See "Instruction" for details.

(11) Step-up circuit 1 (DCDC1)

The step-up circuit 1 steps up the VciOUT level twice to output as VLOUT1. VLOUT1 then generates the supply voltage DDVDH. See "Instruction" for details.

(12) Step-up circuit 2 (DCDC2)

The step-up circuit 2 generates VLOUT2, 3, 4 from VciOUT and VDDVH. VLOUT2 and VLOUT3 are connected to VGH and VGL pins, respectively. See "Instruction" for details.

(13) VREG1 regulator

The VREG1 regulator multiplies REGP by a constant-number factor and then output into VREG1. See “Instruction” for details.

(14) Level sift circuit

The level sifter changes the amplitude of input signal Vcc-GND. See “Electrical characteristics” for details.

Discontinued

Pin Arrangement

Chip size: 18.90 mm x 2.30 mm
 Chip thickness: 550µm(typ.)
 Pad coordinates: PAD center
 Coordinates origin: Chip center

Au bump size
 (1) 54µm x 100µm
 Input side: No.1~No.198
 (2) 26µm x 90µm
 Staggered output side: No.251~No.886

(3) 90µm x 26µm
 Staggered output side: No.205~No.246,
 No.891~No.932

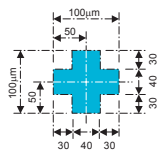
(4) 100µm x 100µm
 DUMMY pins: No.199, No.938

(5) 90µm x 26µm
 DUMMY pins: No.200~No.204, No.247, No.248
 DUMMY pins: No.889, No.890, No.933~No.937


(6) 26µm x 90µm
 DUMMY pins: No.249, No.250, No.887, No.888

Au bump pitch: See PAD coordinates
 Au bump height: 15µm(typ.)
 No. in the figure corresponds No. in the PAD coordinates


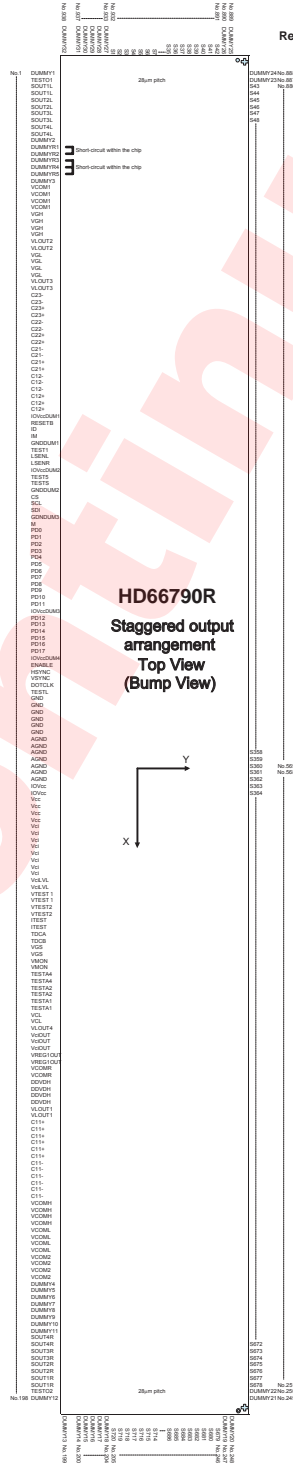
Alignment mark
 (1) arrangement: 2 places
 Coordinates (X, Y) = (± 9244.5, 944.4)



(2-a) Coordinates (X, Y) = (-9294.4, 802.5)



(2-b) Coordinates (X, Y) = (9294.4, 802.5)

PAD Coordinate

HD66790R PAD Coordinates (input)				Rev.1.0 2004.06.04			
No.	pad name	X	Y	No.	pad name	X	Y
1	DUMMY1	-9037.6	-990.7	100	AGND	-422.5	-990.7
2	TESTO1	-8952.0	-990.7	101	AGND	-336.9	-990.7
3	SOUT1L	-8853.6	-990.7	102	AGND	-251.3	-990.7
4	SOUT1L	-8768.0	-990.7	103	AGND	-165.6	-990.7
5	SOUT2L	-8682.4	-990.7	104	AGND	-80.0	-990.7
6	SOUT2L	-8596.8	-990.7	105	AGND	5.6	-990.7
7	SOUT3L	-8511.2	-990.7	106	AGND	91.2	-990.7
8	SOUT3L	-8425.5	-990.7	107	IOVCC	210.0	-990.7
9	SOUT4L	-8339.9	-990.7	108	IOVCC	295.6	-990.7
10	SOUT4L	-8254.3	-990.7	109	VCC	422.4	-990.7
11	DUMMY2	-8155.9	-990.7	110	VCC	508.0	-990.7
12	DUMMYR1	-8070.3	-990.7	111	VCC	634.8	-990.7
13	DUMMYR2	-7984.7	-990.7	112	VCC	720.4	-990.7
14	DUMMYR3	-7899.1	-990.7	113	VCI	848.5	-990.7
15	DUMMYR4	-7813.5	-990.7	114	VCI	934.1	-990.7
16	DUMMYR5	-7727.9	-990.7	115	VCI	1019.8	-990.7
17	DUMMY3	-7642.3	-990.7	116	VCI	1105.4	-990.7
18	VCOM1	-7543.8	-990.7	117	VCI	1225.8	-990.7
19	VCOM1	-7458.2	-990.7	118	VCI	1311.4	-990.7
20	VCOM1	-7372.6	-990.7	119	VCI	1397.0	-990.7
21	VCOM1	-7287.0	-990.7	120	VCI	1482.6	-990.7
22	VGH	-7162.2	-990.7	121	VCILVL	1626.4	-990.7
23	VGH	-7076.6	-990.7	122	VCILVL	1712.0	-990.7
24	VGH	-6991.0	-990.7	123	VTEST1	1838.8	-990.7
25	VGH	-6905.4	-990.7	124	VTEST1	1924.4	-990.7
26	VLOUT2	-6803.2	-990.7	125	VTEST2	2010.0	-990.7
27	VLOUT2	-6717.6	-990.7	126	VTEST2	2095.7	-990.7
28	VGL	-6592.7	-990.7	127	ITES T	2181.3	-990.7
29	VGL	-6507.1	-990.7	128	ITES T	2266.9	-990.7
30	VGL	-6421.5	-990.7	129	TDCA	2353.7	-990.7
31	VGL	-6335.9	-990.7	130	TDCB	2439.3	-990.7
32	VLOUT3	-6224.7	-990.7	131	VGS	2606.1	-990.7
33	VLOUT3	-6139.1	-990.7	132	VGS	2691.7	-990.7
34	C23-	-6027.8	-990.7	133	VMON	2777.3	-990.7
35	C23-	-5942.2	-990.7	134	VMON	2862.9	-990.7
36	C23+	-5856.6	-990.7	135	TESTA4	2981.9	-990.7
37	C23+	-5771.0	-990.7	136	TESTA4	3102.3	-990.7
38	C22-	-5685.4	-990.7	137	TESTA2	3230.5	-990.7
39	C22-	-5599.8	-990.7	138	TESTA2	3316.1	-990.7
40	C22+	-5514.2	-990.7	139	TESTA1	3401.7	-990.7
41	C22+	-5428.6	-990.7	140	TESTA1	3487.3	-990.7
42	C21-	-5343.0	-990.7	141	VCL	3606.3	-990.7
43	C21-	-5257.4	-990.7	142	VCL	3691.9	-990.7
44	C21+	-5171.7	-990.7	143	VLOUT4	3803.2	-990.7
45	C21+	-5086.1	-990.7	144	VCIOUT	3947.0	-990.7
46	C12-	-5000.5	-990.7	145	VCIOUT	4032.6	-990.7
47	C12-	-4914.9	-990.7	146	VCIOUT	4118.2	-990.7
48	C12-	-4829.3	-990.7	147	VREG1OUT	4245.0	-990.7
49	C12+	-4710.3	-990.7	148	VREG1OUT	4330.6	-990.7
50	C12+	-4624.7	-990.7	149	VCOMR	4416.2	-990.7
51	C12+	-4539.1	-990.7	150	VCOMR	4501.8	-990.7
52	IOVCCDUM	-4336.2	-990.7	151	DDVDH	4630.0	-990.7
53	RESETB	-4218.6	-990.7	152	DDVDH	4715.6	-990.7
54	ID	-4159.8	-850.7	153	DDVDH	4836.0	-990.7
55	IM	-4100.9	-990.7	154	DDVDH	4921.6	-990.7
56	GNDDUM1	-3983.3	-990.7	155	VLOUT1	5040.7	-990.7
57	TEST1	-3865.7	-990.7	156	VLOUT1	5159.4	-990.7
58	LSENL	-3806.9	-850.7	157	C11+	5278.2	-990.7
59	LSENR	-3748.1	-990.7	158	C11+	5363.8	-990.7
60	IOVCCDUM	-3630.5	-990.7	159	C11+	5449.4	-990.7
61	TEST5	-3512.8	-990.7	160	C11+	5535.1	-990.7
62	TEST5	-3454.0	-850.7	161	C11+	5620.7	-990.7
63	GNDDUM2	-3336.4	-990.7	162	C11+	5706.3	-990.7
64	CS	-3218.8	-990.7	163	C11-	5791.9	-990.7
65	SCL	-3160.0	-850.7	164	C11-	5877.5	-990.7
66	SDI	-3101.1	-990.7	165	C11-	5963.1	-990.7
67	GNDDUM3	-2983.5	-990.7	166	C11-	6048.7	-990.7
68	M	-2865.9	-990.7	167	C11-	6134.3	-990.7
69	PD0	-2807.1	-850.7	168	C11-	6219.9	-990.7
70	PD1	-2748.3	-990.7	169	VCOMH	6363.8	-990.7
71	PD2	-2689.5	-850.7	170	VCOMH	6449.4	-990.7
72	PD3	-2630.6	-990.7	171	VCOMH	6535.0	-990.7
73	PD4	-2571.8	-850.7	172	VCOMH	6654.4	-990.7
74	PD5	-2513.0	-990.7	173	VCOML	6775.8	-990.7
75	PD6	-2454.2	-850.7	174	VCOML	6861.4	-990.7
76	PD7	-2395.4	-990.7	175	VCOML	6947.0	-990.7
77	PD8	-2336.6	-850.7	176	VCOML	7067.4	-990.7
78	PD9	-2277.8	-990.7	177	VCOM2	7187.8	-990.7
79	PD10	-2219.0	-850.7	178	VCOM2	7273.4	-990.7
80	PD11	-2160.2	-990.7	179	VCOM2	7359.0	-990.7
81	IOVCCDUM	-2042.5	-990.7	180	VCOM2	7444.6	-990.7
82	PD12	-1924.9	-990.7	181	DUMMY4	7543.1	-990.7
83	PD13	-1866.1	-850.7	182	DUMMY5	7628.7	-990.7
84	PD14	-1807.3	-990.7	183	DUMMY6	7714.3	-990.7
85	PD15	-1748.5	-850.7	184	DUMMY7	7799.9	-990.7
86	PD16	-1689.7	-990.7	185	DUMMY8	7885.5	-990.7
87	PD17	-1630.8	-850.7	186	DUMMY9	7971.1	-990.7
88	IOVCCDUM	-1513.2	-990.7	187	DUMMY10	8056.7	-990.7
89	ENABLE	-1395.6	-990.7	188	DUMMY11	8142.3	-990.7
90	HSYNC	-1336.8	-850.7	189	SOUT4R	8240.8	-990.7
91	VSYNC	-1278.0	-990.7	190	SOUT4R	8326.4	-990.7
92	DOTCLK	-1219.2	-850.7	191	SOUT3R	8412.0	-990.7
93	TESTL	-1160.3	-990.7	192	SOUT3R	8497.6	-990.7
94	GND	-986.7	-990.7	193	SOUT2R	8583.2	-990.7
95	GND	-901.1	-990.7	194	SOUT2R	8668.8	-990.7
96	GND	-815.5	-990.7	195	SOUT1R	8754.4	-990.7
97	GND	-704.5	-990.7	196	SOUT1R	8840.0	-990.7
98	GND	-618.9	-990.7	197	TESTO2	8938.4	-990.7
99	GND	-533.3	-990.7	198	DUMMY12	9024.0	-990.7

HD66790R PAD Coordinates (Staggered output side 3) Rev1.0 2004.06.04

No.	pad name	X	Y	No.	pad name	X	Y
799	S130	-6468.0	995.7	899	S34	-9295.8	361.8
800	S129	-6496.0	860.7	900	S33	-9160.8	333.8
801	S128	-6524.0	995.7	901	S32	-9295.8	305.8
802	S127	-6552.0	860.7	902	S31	-9160.8	277.8
803	S126	-6580.0	995.7	903	S30	-9295.8	249.8
804	S125	-6608.0	860.7	904	S29	-9160.8	221.8
805	S124	-6636.0	995.7	905	S28	-9295.8	193.8
806	S123	-6664.0	860.7	906	S27	-9160.8	165.8
807	S122	-6692.0	995.7	907	S26	-9295.8	137.8
808	S121	-6720.0	860.7	908	S25	-9160.8	109.8
809	S120	-6748.0	995.7	909	S24	-9295.8	81.8
810	S119	-6776.0	860.7	910	S23	-9160.8	53.8
811	S118	-6804.0	995.7	911	S22	-9295.8	25.8
812	S117	-6832.0	860.7	912	S21	-9160.8	-2.2
813	S116	-6860.0	995.7	913	S20	-9295.8	-30.2
814	S115	-6888.0	860.7	914	S19	-9160.8	-58.2
815	S114	-6916.0	995.7	915	S18	-9295.8	-86.2
816	S113	-6944.0	860.7	916	S17	-9160.8	-114.2
817	S112	-6972.0	995.7	917	S16	-9295.8	-142.2
818	S111	-7000.0	860.7	918	S15	-9160.8	-170.2
819	S110	-7028.0	995.7	919	S14	-9295.8	-198.2
820	S109	-7056.0	860.7	920	S13	-9160.8	-226.2
821	S108	-7084.0	995.7	921	S12	-9295.8	-254.2
822	S107	-7112.0	860.7	922	S11	-9160.8	-282.2
823	S106	-7140.0	995.7	923	S10	-9295.8	-310.2
824	S105	-7168.0	860.7	924	S9	-9160.8	-338.2
825	S104	-7196.0	995.7	925	S8	-9295.8	-366.2
826	S103	-7224.0	860.7	926	S7	-9160.8	-394.2
827	S102	-7252.0	995.7	927	S6	-9295.8	-422.2
828	S101	-7280.0	860.7	928	S5	-9160.8	-450.2
829	S100	-7308.0	995.7	929	S4	-9295.8	-478.2
830	S99	-7336.0	860.7	930	S3	-9160.8	-506.2
831	S98	-7364.0	995.7	931	S2	-9295.8	-534.2
832	S97	-7392.0	860.7	932	S1	-9160.8	-562.2
833	S96	-7420.0	995.7	933	DUMMY2	-9295.8	-590.2
834	S95	-7448.0	860.7	934	DUMMY2	-9160.8	-618.2
835	S94	-7476.0	995.7	935	DUMMY2	-9295.8	-646.2
836	S93	-7504.0	860.7	936	DUMMY3	-9295.8	-702.2
837	S92	-7532.0	995.7	937	DUMMY3	-9295.8	-758.2
838	S91	-7560.0	860.7	938	DUMMY3	-9290.8	-990.7
839	S90	-7588.0	995.7				
840	S89	-7616.0	860.7				
841	S88	-7644.0	995.7				
842	S87	-7672.0	860.7				
843	S86	-7700.0	995.7				
844	S85	-7728.0	860.7				
845	S84	-7756.0	995.7				
846	S83	-7784.0	860.7				
847	S82	-7812.0	995.7				
848	S81	-7840.0	860.7				
849	S80	-7868.0	995.7				
850	S79	-7896.0	860.7				
851	S78	-7924.0	995.7				
852	S77	-7952.0	860.7				
853	S76	-7980.0	995.7				
854	S75	-8008.0	860.7				
855	S74	-8036.0	995.7				
856	S73	-8064.0	860.7				
857	S72	-8092.0	995.7				
858	S71	-8120.0	860.7				
859	S70	-8148.0	995.7				
860	S69	-8176.0	860.7				
861	S68	-8204.0	995.7				
862	S67	-8232.0	860.7				
863	S66	-8260.0	995.7				
864	S65	-8288.0	860.7				
865	S64	-8316.0	995.7				
866	S63	-8344.0	860.7				
867	S62	-8372.0	995.7				
868	S61	-8400.0	860.7				
869	S60	-8428.0	995.7				
870	S59	-8456.0	860.7				
871	S58	-8484.0	995.7				
872	S57	-8512.0	860.7				
873	S56	-8540.0	995.7				
874	S55	-8568.0	860.7				
875	S54	-8596.0	995.7				
876	S53	-8624.0	860.7				
877	S52	-8652.0	995.7				
878	S51	-8680.0	860.7				
879	S50	-8708.0	995.7				
880	S49	-8736.0	860.7				
881	S48	-8764.0	995.7				
882	S47	-8792.0	860.7				
883	S46	-8820.0	995.7				
884	S45	-8848.0	860.7				
885	S44	-8876.0	995.7				
886	S43	-8904.0	860.7				
887	DUMMY2	-8932.0	995.7				
888	DUMMY2	-8960.0	860.7				
889	DUMMY2	-9295.8	641.8				
890	DUMMY2	-9160.8	613.8				
891	S42	-9295.8	585.8				
892	S41	-9160.8	557.8				
893	S40	-9295.8	529.8				
894	S39	-9160.8	501.8				
895	S38	-9295.8	473.8				
896	S37	-9160.8	445.8				
897	S36	-9295.8	417.8				
898	S35	-9160.8	389.8				

BUMP Arrangement

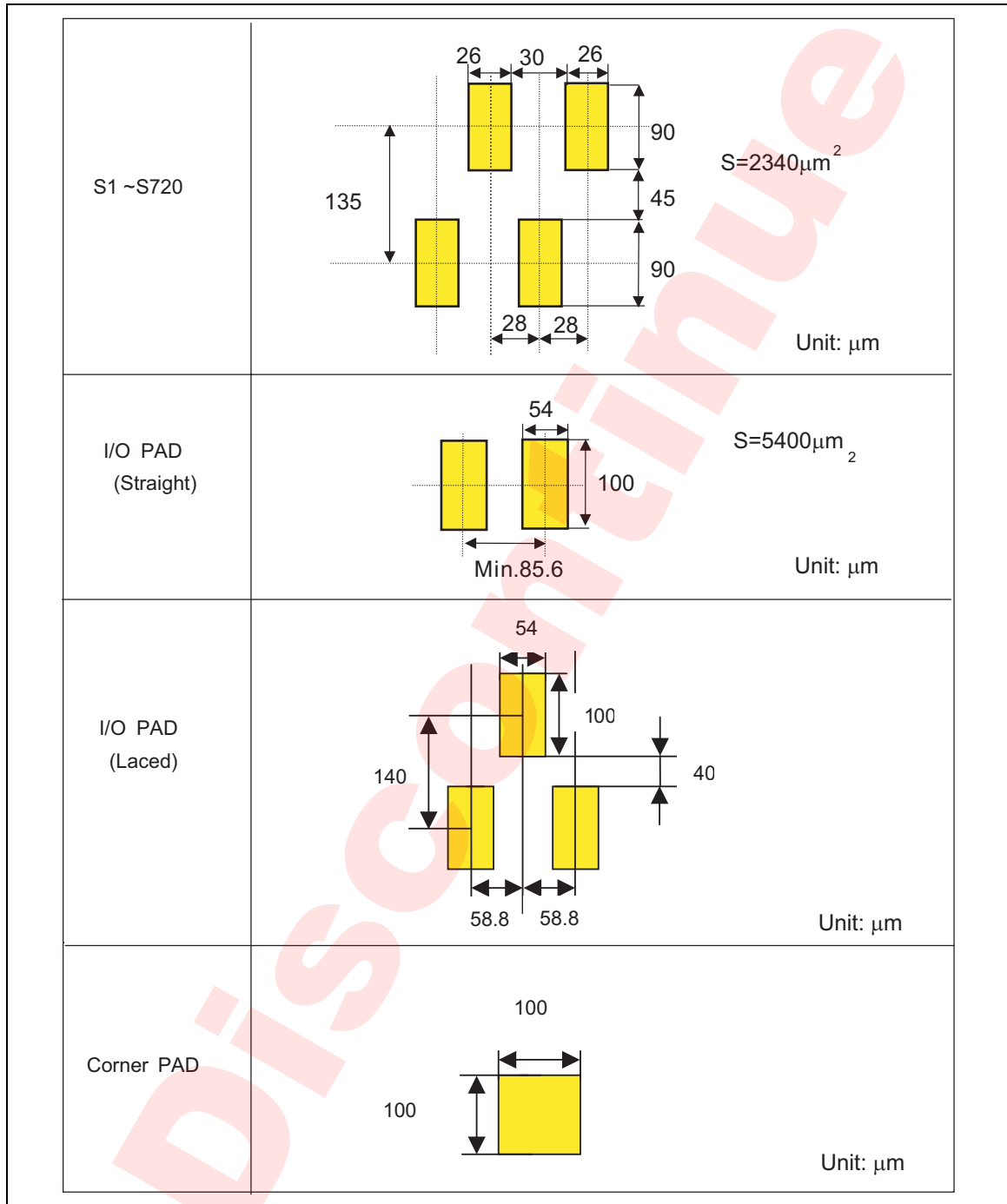
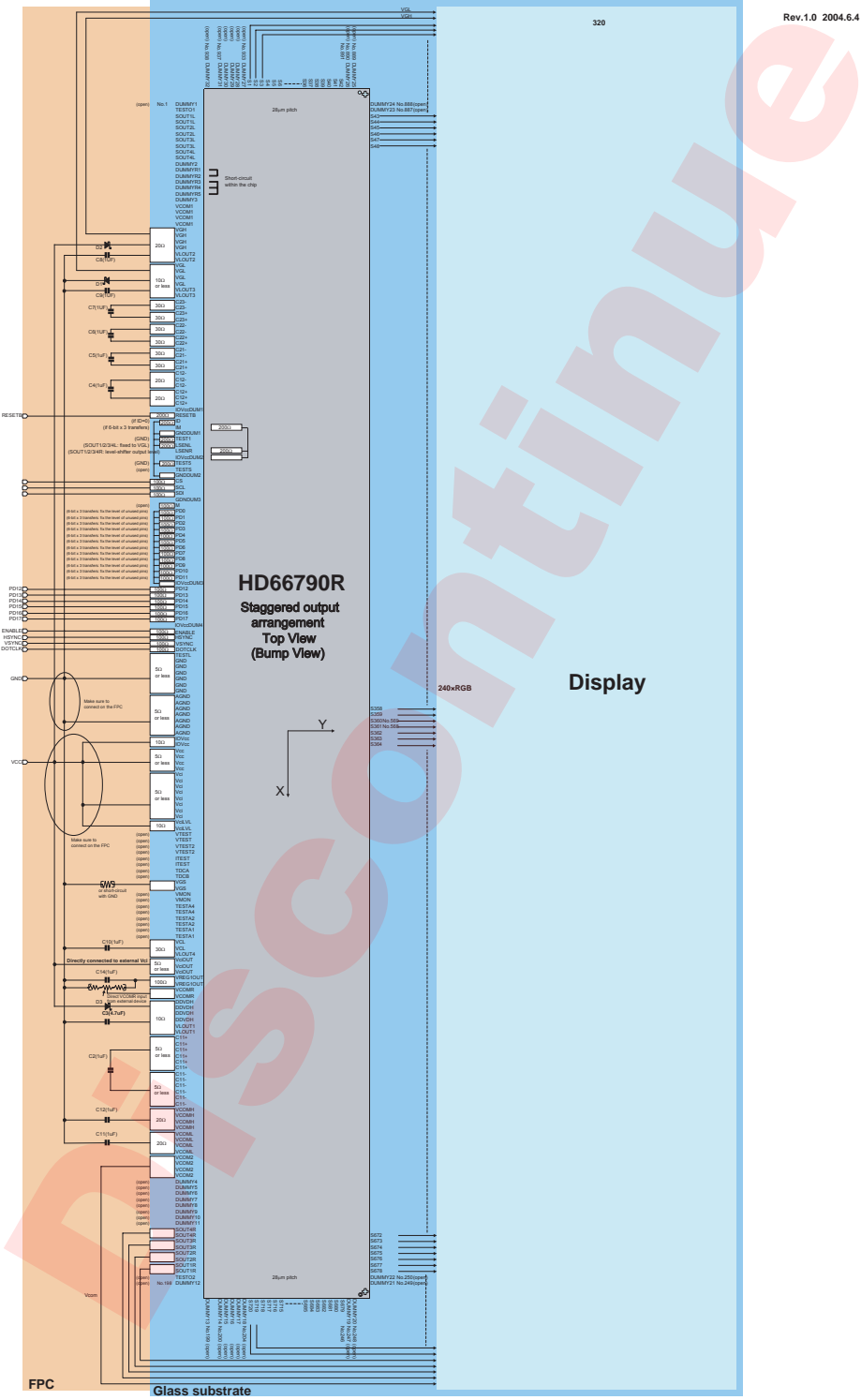


Figure 3

Wiring example



Pin function**Table 2 Power supply pins**

Signals	I/O	Connected to	Function	Unused pins
Vcc	S	Power supply	Logic supply voltage	
IOVcc	S	Power supply	Interface supply voltage	
GND	S	Power supply	Logic ground	
Vci	S	Power supply	Analog supply voltage	
AGND	S	Power supply	Analog ground	

Table 3 DCDC converter pins

Signals	I/O	Connected to	Function	Unused pins
VciOUT	O	Vci1 or Vci	A reference voltage for the step-up circuits, generated from Vci-GND as a reference level. The voltage level is set according to VC[2:0]. Connect a stabilizing capacitor when using. When not in use, leave it open.	
VciLVL	I	Power supply (Vci)	A reference supply voltage setting the maximum electrical potential of ladder resistor for generating reference supply voltage. Set at the Vci level in normal operation.	
VLOUT1	O	DDVDH	A supply voltage having twice the VciOUT level. An output from the step-up circuit 1. Connect a stabilizing capacitor when in use.	
DDVDH	I	VLOUT1 or power supply	A supply voltage for source driver and Vcom drive. Connect to VLOUT1 when using the internal step-up circuit. When not using the internal step-up circuit, connect to an external power supply.	
VLOUT2	O	Stabilizing capacitor	A supply voltage having either 6, 7, or 8 times the VciOUT level. An output from the step-up circuit 2, when DDVDH=VciOUT x 2. The step-up factor is set according to BT[2:0]. Connect a stabilizing capacitor when using VGH.	
VGH	I	VLOUT2 or power supply	A supply voltage to drive the gate driver circuit incorporated in the TFT LCD panel.	
VLOUT3	O	Stabilizing capacitor	A supply voltage of either -5, -6, or -7 times the VciOUT level, output from the step-up circuit 2, when DDVDH=VciOUT x 2. The step-up factor is set according to BT[2:0]. Connect a stabilizing capacitor when using VGL.	
VGL	I	VLOUT3 or power supply	A supply voltage to drive the gate driver circuit incorporated in the TFT LCD panel.	
VLOUT4	O	Stabilizing capacitor	A supply voltage having -1 times the VciOUT level. An output from the step-up circuit 2. Connect a stabilizing capacitor when in use.	
VCL	I	VLOUT4 or power supply	VcomL drive supply voltage.	
C11+, C11-	I/O	Step-up capacitor	Connect a stabilizing capacitor when using the step-up circuit 1.	Open
C12+, C12-	I/O	Step-up capacitor	Connect a stabilizing capacitor when using the step-up circuit 2.	Open
C21+, C21-	I/O	Step-up capacitor	Connect a stabilizing capacitor when using the step-up circuit 2.	Open
C22+, C22-	I/O	Step-up capacitor	Connect a stabilizing capacitor when using the step-up circuit 2.	Open
C23+, C23-	I/O	Step-up capacitor	Connect a stabilizing capacitor when using the step-up circuit 2.	Open

Table 4 Common electrode output and control pins

Signals	I/O	Connected to	Function	Unused pins
VREG1OUT	O	Stabilizing capacitor	A voltage level generated by multiplying the internal reference voltage REGP, having the same electrical potential as VciOUT, by a factor 1.27 ~ 1.92. The REGP is generated internally from the Vci-GND level. The step-up factor for REGP is set by instruction (VRH[3:0]). VREG1OUT serves as (1) source driver grayscale reference level VDH, (2) VcomH reference level, (3) Vcom width reference level. Connect a stabilizing capacitor in use. When not in use, leave it open.	Open
VCOM1, VCOM2	O	TFT panel common electrode	Output the Vcom level to the TFT panel's common electrode. Both VCOM1 and VCOM2 output the same signal. VCOM1 and VCOM2 are arranged on the left and right sides of the chip respectively for convenience of arrangement. Use either one of them.	
VcomH	O	Stabilizing capacitor	Vcom High. The output level is adjusted by instruction (VCM[4:0]).	
VcomL	O	Stabilizing capacitor or open	Vcom Low. See "Voltage Setting Pattern Diagram" for reference. The Vcom Low level is set by instruction (VDV[4:0]), which sets the amplitude VcomH-VcomL using the VcomH level as a reference. When VCOMG=0, the VcomL output is halted. In this case, a capacitor connection is not required.	
VcomR	I	Variable resistor	Use the VcomR pin when adjusting the VcomH level using a variable resistor. When using VcomR, halt the VcomH internal adjusting circuit by instruction (VCM[4:0]) and connect a variable resistor between VREG1OUT and GND. When not using VcomR (not adjusting VcomH with a resistor externally), leave the VcomR pin open, and adjust the Vcom level by instruction (VCM[4:0]).	Open

Table 5 Source driver output and control pins

Signals	I/O	Connected to	Function	Unused pins
S1~ S720	O	LCD	Source signal lines, which output LCD applied voltages. The shift direction of source output is changeable by setting the SHL pin.	

Table 6 Source driver power supply pin

Signals	I/O	Connected to	Function	Unused pins
VGS	S	GND or resistor	Source driver power supply Low.	

Table 7 Grayscale level monitor pins

Signals	I/O	Connected to	Function	Unused pins
VMON	I/O	OPEN	A grayscale level monitor pin. Do not use this pin. Disconnect it.	
RESETB	I	MPU or external RC circuits	A reset pin. The HD66790R is initialized during RESETB Low. Be sure to execute a power-on reset after turning on the power supply.	
VSYNC	I	LCTC	A frame synchronous signal. The effective polarity of the signal is changeable by setting the VPL pin.	
HSYNC	I	LCTC	A line synchronous signal. The effective polarity of the signal is changeable by setting the HPL pin.	
DOTCLK	I	LCTC	A DOTCLK signal. The effective polarity of the signal is changeable by setting the DPL pin.	
ENABLE	I	LCTC	A data ENABLE signal. The effective polarity of the signal (data input timing edge) is set by the EPL bit.	
PD17-0	I	LCTC	A data bus to input display data in units of 18 bits (6 bits (grayscale) x 3 dots (RGB)).	GND or Vcc
IM	I	GND or Vcc	RGB interface mode switching pin. If IM = "L": input RGB dot data at a time via 18-bit RGB interface. If IM = "H": input one dot data (6 bits) at a time via 6-bit interface (input RGB dot data by 3 transmissions).	

Table 8 Register control interface pins

Signals	I/O	Connected to	Function	Unused pins
ID	I	GND or Vcc	Chip ID setting pin for serial interface.	
CS	I	MPU	Chip select signal for serial interface. If CS = "L": select the HD66790R (accessible). If CS = "H": not select the HD66790R (inaccessible)	Fix to Vcc
SCL	I	MPU	Synchronous clock signal for serial interface.	Fix to Vcc
SDI	I	MPU	Data input pin for serial interface. Input data on the rising edge of SCL signal.	Fix to Vcc

Table 9 Gate driver control signal function setting pins

Signals	I/O	Connected to	Function	Unused pins
LSENR	I	GND or Vcc	Level shifter output ENABLE signal. If LSENR = "H": enable level-shifter output levels from SOUTxR pins (x: 1~4) If LSENR = "L": output the VGL level from SOUTxR pins. In consideration of current consumption increase and voltage drop, set LSENL = "L" if LSENR = "H".	-
LSENL	I	GND or Vcc	Level shifter output ENABLE signal. If LSENL = "H": enable level-shifter output levels from SOUTxL pins (x: 1~4) If LSENL = "L": output the VGL level from SOUTxL pins. In consideration of current consumption increase and voltage drop, set LSENR = "L" if LSENL = "H".	-

Table 10 Gate driver control signal within level shifter

Signals	I/O	Connected to	Function	Unused pins
SOUT1R SOUT1L	O		A frame pulse signal for LCD (a level-shifter output having an operating amplitude VGH-VGL).	Open
SOUT2R SOUT2L	O		A line cycle clock signal for LCD (a level-shifter output having an operating amplitude VGH-VGL).	Open
SOUT3R SOUT3L	O		A signal for LCD (a level-shifter output having an operating amplitude VGH-VGL).	Open
SOUT4R SOUT4L	O		A signal for LCD (a level-shifter output having an operating amplitude VGH-VGL).	Open

Table 11 Gate driver control signal for logic level

Signals	I/O	Connected to	Function	Unused pins
M	O		Alternating cycle clock signal (logic level output).	Open

Table 12 TEST pins

Signals	I/O	Connected to	Function	Unused pins
TESTO1	O	Open	A monitor pin for S1.	
TESTO2	O	Open	A monitor pin for S720.	
TEST1	I	GND	A logic test pin.	
TEST5	I	GND	A logic test pin.	
TESTS	O	Open	A logic test pin.	
VTEST1	O	Open	An analog test pin.	
VTEST2	O	Open	An analog test pin.	
ITEST	O	Open	An analog test pin.	
TDCA	O	Open	An analog test pin.	
TDCB	O	Open	An analog test pin.	
TESTA1	O	Open	An analog test pin.	
TESTA2	O	Open	An analog test pin.	
TESTA4	O	Stabilizing capacitor	An analog test pin.	
TESTL	I	GND	An analog test pin.	

Table 13 Dummy pins

Signals	I/O	Connected to	Function	Unused pins
DUMMY 1 ~ 15	-	Open	Disconnect these pins.	
DUMMYR	I/O		Dummy pads. DUMMYR can also be used for measuring COG contact resistance.	
VccDUM 1 ~ 4	O		Pins to fix High level. Use them to fix the levels of mode pins.	
GNDDUM 1 ~ 3	O		Pins to fix Low level. Use them to fix the levels of mode pins.	

Patents of dummy pin which is used to fix pin to VCC or GND are pending and granted.

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PATENT PENDING: Japanese Application No. 10-514484

Korean Application No. 19997002322

Taiwanese Application No.086103756

(PCT/JP96/02728(W098/12597))

Instruction

The HD66790R supports an interface to a microcomputer to manage high-quality display and low power consumption drive by setting instruction. See “Serial Interface” for reference to setting and timing chart and so on.

Index: IR

RS1	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	0	0	ID4	ID3	ID2	ID1	ID0
Default	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0

Specifies the index of the register to access. When changing the setting in a register, make sure to specify its index in this register.

Power Color 1: R01h

RS1	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	DC 12	DC 11	DC 10	GON	0	BT2	BT1	BT0	DC 02	DC 01	DC 00	AP2	AP1	AP0	SLP
Default	-	0	0	0	0	-	1	1	1	0	0	0	0	0	0	0

SLP: Sets sleep mode. Upon setting SLP = “1”, the HD66790R’s internal state becomes the same as when AP[2:0] = “000”, in which the power circuit operation (DCDC step-up circuits) is halted but the source amplifiers and other circuits are operating normally. This does not mean the AP[2:0] bits are overwritten to “000” upon setting sleep mode. This register setting is enabled from the next VSYNC assert timing.

AP[2:0]: Adjusts the constant current in the constant current source in internal operational amplifier circuit. The operational amplifier circuit is stabilized with the higher constant current. Adjust the constant current taking the trade-off between grayscale level stability and current consumption into account. In cases like sleep and standby modes when there is no display on the screen, set AP[2:0] = “000” to halt the operational amplifiers to reduce power consumption. If AP[2:0] is set to other than “000”, the step-up circuits 1, 2 output VLOUT1 and VLOUT2 respectively.

Table 14

AP2	AP1	AP0	Constant current in operational amplifiers
0	0	0	Halt operations of operational amplifier and step-up circuits (Default)
0	0	1	0.5
0	1	0	0.75
0	1	1	1
1	0	0	1.25
1	0	1	1.5
1	1	0	Setting disabled
1	1	1	Setting disabled

Note: The values in this table are the ratios of constant currents when AP[2:0] is set to "011".

DC0[2:0]: Sets the operating cycle of step-up circuit 1. Current consumption will increase as setting the higher step-up cycle. Set the optimum cycle taking display quality, power consumption, and power supply startup characteristics in high temperatures into consideration. The load fluctuation of DDVDH becomes smaller by setting the higher step-up cycle. The operating cycle of the step-up circuit 2 is set separately with DC1[2:0].

Table 15

DC02	DC01	DC00	Step-up circuit 1: Step-up cycle
0	0	0	DOTCLK / 32 (Default)
0	0	1	DOTCLK / 64
0	1	0	DOTCLK / 128
0	1	1	DOTCLK / 256
1	0	0	DOTCLK / 512
1	0	1	Setting disabled
1	1	0	DOTCLK / 16
1	1	1	Setting disabled

BT[2:0]: Sets the step-up factor for the internal step-up circuits. Change the step-up factor according to the power supply voltages in use.

Table 16

VLOUT1 output: Vci1 x 2 (fixed whatever the setting of BT[2:0])

BT2	BT1	BT0	VLOUT1 output	Capacitor connection pins	
*	*	*	Vci1 x 2	VLOUT1, C11±	
VLOUT2, VLOUT3 outputs:					
BT2	BT1	BT0	VLOUT2	VLOUT3	Capacitor connection pins
0	0	0		$-(V_{ciOUT} + DDVDH \times 3)$ [x -7]	VLOUT2, VLOUT3, C12±, C21±, C22±
0	0	1	DDVDH x 4 [x 8]	$-(DDVDH \times 3)$ [x -6]	VLOUT2, VLOUT3, C21±, C22±
0	1	0		$-(V_{ciOUT} + DDVDH \times 2)$ [x -5]	VLOUT2, VLOUT3, C12±, C21±, C22±
0	1	1		$-(V_{ciOUT} + DDVDH \times 3)$ [x -7]	VLOUT2, VLOUT3, C12±, C21±, C22±
1	0	0	VciOUT+DDV DHx3 [x 7]	$-(DDVDH \times 3)$ [x -6]	VLOUT2, VLOUT3, C21±, C22±
1	0	1		$-(V_{ciOUT} + DDVDH \times 2)$ [x -5]	VLOUT2, VLOUT3, C12±, C21±, C22±
1	1	0	DDVDH x 3 [x 6]	$-(DDVDH \times 3)$ [x -6]	VLOUT2, VLOUT3, C21±, C22±
1	1	1		$-(V_{ciOUT} + DDVDH \times 2)$ [x -5]	VLOUT2, VLOUT3, C12±, C21± (Default)

Notes: 1. The step-up factors in the brackets are the factors against VciOUT, when short-circuiting VLOUT1 and DDVDH.

2. When using VLOUT1/2/3/4 pins, connect capacitors as required.

GON: Controls Vcom output. When GON = "0", the Vcom output level becomes GND.

DC1[2:0]: Sets the operating cycle of step-up circuit 2. Current consumption will increase as setting the higher step-up cycle. Set the optimum cycle taking display quality, power consumption, and power supply startup characteristics in high temperatures into consideration. The load fluctuation of DDVDH becomes smaller by setting the higher step-up cycle. The operating cycle of the step-up circuit 1 is set separately with DC0[2:0].

Table 17

DC 12	DC 11	DC 10	Step-up circuit 2: Step-up cycle
0	0	0	DOTCLK / 64 (Default)
0	0	1	DOTCLK / 128
0	1	0	DOTCLK / 256
0	1	1	DOTCLK / 512
1	0	0	DOTCLK / 1024
1	0	1	DOTCLK / 2048
1	1	0	DOTCLK / 4096
1	1	1	Setting disabled

The HD66790R adopts a charge pump method (DCDC) to generate supply voltages to the LSI. The DDVDH output voltage level fluctuation (ripple) is likely to occur with higher power supply load in synchronization with the cycle of the division ratio set with DC0[2:0]. Also, with larger DDVDH voltage fluctuation, source output voltage fluctuation is likely to occur in synchronization with this and this phenomenon sometime becomes visible as differences in shade on the display in gate line direction. The DDVDH ripple is also likely to occur in synchronization with Vcom operation when the Vcom load on the panel is large. This again will result in source output voltage fluctuation.

To mitigate the DDVDH voltage fluctuation, connect multiple stabilizing capacitors of 1uF to DDVDH in parallel so that enough capacitance will be secured. Also, use the smallest possible electrical load on the panel. The following functions are effective to reduce current consumption and power supply load: halt source amplifiers (EQE, SDC, SDT); use source-Vcom equalize function (EQE, SDT); adjust source amplifier bias current (TMB). Optimize the settings using these registers according to the characteristics of the panel.

The HD66790R's step-up operation is synchronized with DOTCLK, the frequency of which is multiplied with the division ratio set with DC0[2:0] or DC1[2:0]. Set the appropriate division ratios to optimize the DOTCLK frequencies for step-up cycles DCDC1, DCDC2. Set DC0[2:0] and DC1[2:0] so that the frequencies of step-up cycles DCDC1, DCDC2 are set from 25KHz to 100KHz and from 5KHz to 25KHz, respectively with the smaller division ratio for DCDC1 than that for DCDC2. The HD66790R can operate with step-up cycle frequencies not within the recommended ranges. However, current consumption will increase with higher step-up clock frequency, which results in output voltage drop. It is important to check the quality of display in setting. When operating with a frequency not within the recommended range, it demands special attention in generating supply voltage levels according to the power supply setting sequence (page 70). In this case, it will take longer to generate the VGH and VGL levels after setting AP[2:0] at the power supply setting instruction 1 stage in the sequence. Upon setting DK = 0 to generate the DDVDH level at the power supply setting instruction 2 stage in the sequence, the relationship of electrical potentials between DDVDH and VGH is likely to be reversed, which results in failed power supply generation. For this reason, spread between the two setting stages in the sequence.

In general, the DDVDH ripple synchronized with the DCDC frequency can be mitigated by raising the step-up clock frequency by setting a smaller division ratio because the electrical potential fluctuation synchronized with the higher DCDC frequency will be smaller. In this case, the visible effects from DDVDH ripple will become smaller. However, the DDVDH output voltage is likely to drop at high frequencies because of compromised efficiency. When $f_{\text{DOTCLK}} = 5\text{MHz}$, setting the division ratio between 1/128 and 1/256 can minimize the output impedance.

There are cases that lines are seen moving in gate line direction (horizontally) on the screen with some division ratio setting. This phenomenon has something to do with the step-up cycles DCDC1, DCDC2, which are the same with the cycles of respective division ratios. For example, when setting the division ratio to 1/64, the charge pump cycle occurs every 64 DOTCLKs and the DDVDH ripple occurs in a cycle of 64 DOTCLKs. The DDVDH ripple causes source output voltage fluctuation and it appears as differences in shade on the screen in gate line direction. This phenomenon can be explained by the following reason. When the total duration of horizontal back porch period (HBP) and horizontal front porch (HFP) period lasts for 320 DOTCLKs, and not 160 DOTCLKs, the number of DOTCLK in 1H (horizontal) period becomes 272. In this case, since the number of DOTCLK in 1H period is not a multiple of 64, i.e. the number of DOTCLK in one charge pump cycle, the DDVDH ripple occurs at different lines and it appears as a visible phenomenon that the differences in shade are seen moving in gate line direction. Accordingly, this problem will overcome by setting the total duration of HBP and HFP periods to 256

DOTCLK (the least common multiple of 32, 64, 128, and 256) when the division ratio of DCDC1 is 1/16, or 1/256. When the division ratio of DCDC1 is 1/512, set 1H period to 256 DOTCLKs and the total number of horizontal line (the number of valid lines+HBP+HFP) to an odd number. This is because one charge pump cycle lasts for 2 line periods. If the total number of horizontal line is set to an even number, the DDVDH ripple is fixed at the same lines, which appears as the differences in shade in gate line direction every 2 lines. However, by setting the total number of horizontal line to an odd number, the DDVDH ripple, which occurs every other lines, occurs every 2 frame periods with regard to each line. Accordingly, the voltage fluctuations are offset during 2 frame periods, and the differences in shade occurring every two lines will disappear.

The following are examples of setting. In 18-bit interface mode, set the division ratios of DCDC1 and DCDC2 to 1/128, 1/512, respectively when DOTCLK = 5MHz. The number of DOTCLK in 1H period should be 256 DOTCLKs. In 6-bit interface mode, the frequency of DOTCLK becomes three times higher than otherwise for the same frame frequency. In this case, DOTCLK = 15MHz, and the recommended combination of division ratios of DCDC1 and DCDC2 is either 1/512, 1/2048 or 1/256, 1/1024, respectively. Even when the division ratio of DCDC1 is set to 1/32 for fair quality of display, it is recommended to set as high a division ratio as possible (lower step-up clock frequency) for DCDC2.

Voltage setup 1 : R01h

RS1	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	DK	0	POC	0	PON	VRH 3	VRH 2	VRH 1	VRH 0	VC2	VC1	VC0
Default	-	-	-	-	1	-	0	-	0	0	0	0	0	0	0	0

VC[2:0]: Generates the VciOUT output and the VREG1OUT input levels using VciLVL as a reference. The step-up factors set with VC[2:0] are follows. Set VC[2:0] to "000" when the Vci level externally.

Table 18

VC2	VC1	VC0	VciOUT voltage (REGP)
0	0	0	VciLVL (Default)
0	0	1	0.92 x VciLVL
0	1	0	0.90 x VciLVL
0	1	1	0.87 x VciLVL
1	0	0	0.85 x VciLVL
1	0	1	0.83 x VciLVL
1	1	0	0.73 x VciLVL
1	1	1	Setting disabled

VRH[3:0]: Sets the amplifying factor of REGP from 1.27 to 1.92 to output VREG1OUT level. REGP is the VciOUT input level set with VC[2:0].

Table 19

VRH3	VRH2	VRH1	VRH0	VREG1OUT voltage
0	0	0	0	1.27 x REGP (Default)
0	0	0	1	1.32 x REGP
0	0	1	0	1.37 x REGP
0	0	1	1	1.42 x REGP
0	1	0	0	1.47 x REGP
0	1	0	1	1.52 x REGP
0	1	1	0	1.57 x REGP
0	1	1	1	Halt
1	0	0	0	1.62 x REGP
1	0	0	1	1.67 x REGP
1	0	1	0	1.72 x REGP
1	0	1	1	1.77 x REGP
1	1	0	0	1.82 x REGP
1	1	0	1	1.87 x REGP
1	1	1	0	1.92 x REGP
1	1	1	1	Halt

PON: Controls ON/OFF of VLOUT3 output.

Table 20

PON	VLOUT3
0	OFF (Default)
1	ON

POC: Controls the power control mode.

Table 21

POC	Power control mode
0	Power control mode. All white display on the screen (Default)
1	Normal operation mode. All I/O interfaces are operable.

- Notes
1. See "Power control" for details.
 2. The setting is enabled from the next VSYNC assert timing.

DK: Controls DDVDH.

Table 22

DK	Function
0	Generates DDVDH simultaneously with VGH. Startup the step-up circuit 1 (VLOUT1 output) according to the step-up factor set with AP[2:0].
1	Halt step-up circuit 1 (VLOUT1). (Default)

Voltage setup 2: R02h

RS1	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	VCOMG	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	VCM4	VCM3	VCM2	VCM1	VCM0
Default	-	-	0	0	0	0	0	0	-	-	-	0	0	0	0	0

VCOMG: When VCOMG = “1”, the VcomL output level is set by instruction VDV[4:0]. VCOMG = “1” is enabled when PON = “1”. When VCOMG = “0”, the VcomL output level is fixed to the GND level and the register setting VDV[4:0] is disenabled. In this case, the supply voltage for VcomL (VLOUT4) is halted. Since the register setting VCOMG affects the power supply startup sequence, set VCOMG according to the power supply startup sequence.

VCM[4:0]: Sets the amplifying factor from 0.41 to 1.00 of VREG1OUT to generate VcomH (Vcom High). The VcomH level adjustment using internal volume is halted by setting VCM[4:0] = “11111” and the VcomH level can be adjusted using an external resistor connected to the VcomR.

Table 23

VCM4	VCM3	VCM2	VCM1	VCM0	VcomH voltage	
0	0	0	0	0	VREG1 x 0.41	24/60R (Default)
0	0	0	0	1	VREG1 x 0.43	26/60R
0	0	0	1	0	VREG1 x 0.45	27/60R
0	0	0	1	1	VREG1 x 0.47	28/60R
0	0	1	0	0	VREG1 x 0.49	29/60R
0	0	1	0	1	VREG1 x 0.51	30/60R
0	0	1	1	0	VREG1 x 0.53	32/60R
0	0	1	1	1	VREG1 x 0.55	33/60R
0	1	0	0	0	VREG1 x 0.57	34/60R
0	1	0	0	1	VREG1 x 0.59	35/60R
0	1	0	1	0	VREG1 x 0.61	36/60R
0	1	0	1	1	VREG1 x 0.63	38/60R
0	1	1	0	0	VREG1 x 0.65	39/60R
0	1	1	0	1	VREG1 x 0.67	40/60R
0	1	1	1	0	VREG1 x 0.69	41/60R
0	1	1	1	1	Setting disabled	
1	0	0	0	0	VREG1 x 0.71	42/60R
1	0	0	0	1	VREG1 x 0.73	43/40R
1	0	0	1	0	VREG1 x 0.75	44/60R
1	0	0	1	1	VREG1 x 0.77	45/60R
1	0	1	0	0	VREG1 x 0.79	47/60R
1	0	1	0	1	VREG1 x 0.81	48/60R
1	0	1	1	0	VREG1 x 0.83	50/60R
1	0	1	1	1	VREG1 x 0.85	51/60R
1	1	0	0	0	VREG1 x 0.87	52/60R
1	1	0	0	1	VREG1 x 0.89	54/60R
1	1	0	1	0	VREG1 x 0.91	55/60R
1	1	0	1	1	VREG1 x 0.93	56/60R
1	1	1	0	0	VREG1 x 0.95	57/60R
1	1	1	0	1	VREG1 x 0.97	58/60R
1	1	1	1	0	VREG1 x 1.00	60/60R
1	1	1	1	1	Disenables internal volume adjustment and enables adjustment with an external resistor.	

VDV[4:0]: Sets the amplifying factor of VREG1OUT from 0.6 to 1.48 to change the amplitude of Vcom, when it is defined between VcomH and VcomL. When VCOMG = "0", the register setting VDV[4:0] is disabled.

Table 24

VDV4	VDV3	VDV2	VDV1	VDV0	Vcom amplitude	
0	0	0	0	0	VREG1OUT x 0.60	36/60R (Default)
0	0	0	0	1	VREG1OUT x 0.63	38/60R
0	0	0	1	0	VREG1OUT x 0.66	40/60R
0	0	0	1	1	VREG1OUT x 0.70	42/60R
0	0	1	0	0	VREG1OUT x 0.73	44/60R
0	0	1	0	1	VREG1OUT x 0.77	46/60R
0	0	1	1	0	VREG1OUT x 0.80	48/60R
0	0	1	1	1	VREG1OUT x 0.83	50/60R
0	1	0	0	0	VREG1OUT x 0.87	52/60R
0	1	0	0	1	VREG1OUT x 0.90	54/60R
0	1	0	1	0	VREG1OUT x 0.93	56/60R
0	1	0	1	1	VREG1OUT x 0.97	58/60R
0	1	1	0	0	VREG1OUT x 1.00	60/60R
0	1	1	0	1	VREG1OUT x 1.03	62/60R
0	1	1	1	0	Setting disabled	
0	1	1	1	1	Setting disabled	
1	0	0	0	0	VREG1OUT x 1.05	63/60R
1	0	0	0	1	VREG1OUT x 1.08	65/40R
1	0	0	1	0	VREG1OUT x 1.12	67/60R
1	0	0	1	1	VREG1OUT x 1.15	69/60R
1	0	1	0	0	VREG1OUT x 1.18	71/60R
1	0	1	0	1	VREG1OUT x 1.22	73/60R
1	0	1	1	0	VREG1OUT x 1.25	75/60R
1	0	1	1	1	VREG1OUT x 1.28	77/60R
1	1	0	0	0	VREG1OUT x 1.32	79/60R
1	1	0	0	1	VREG1OUT x 1.35	81/60R
1	1	0	1	0	VREG1OUT x 1.38	83/60R
1	1	0	1	1	VREG1OUT x 1.42	85/60R
1	1	1	0	0	VREG1OUT x 1.45	87/60R
1	1	1	0	1	VREG1OUT x 1.48	89/60R
1	1	1	1	0	Setting disabled	
1	1	1	1	1	Setting disabled	

Driver output control: R03h

RS1	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	VPL	HPL	DPL	EPL	0	0	SHL	0	0	0	0	SDT 1	SDT 0	0	0
Default	-	0	0	0	0	-	-	0	-	-	-	-	0	0	-	-

SDT[1:0]: Sets the source output delay time. Set an optimum delay time for the characteristics of the panel when using source-Vcom equalizing function and source amplifier halt function.

Table 25

SDT1	SDT0	Delay	Source output delay time	
			18-bit RGB I/F (5MHz)	6-bit RGB I/F (16MHz)
0	0	10 DOTCLKs	2.0 μ S	1.8750 μ S (Default)
0	1	40 DOTCLKs	8.0 μ S	7.5 μ S
1	0	80 DOTCLKs	16.0 μ S	15.0 μ S
1	1	120 DOTCLKs	524 μ S	22.5 μ S

Note: The delay time changes according to the DOTCLK frequency.

SHL: Sets the shift direction of source output.

Table 26

SHL	Shift direction
0	(S1, S2, S3) \rightarrow (S718, S719, S720) (Default)
1	(S718, S719, S720) \rightarrow (S1, S2, S3)

EPL: Sets the signal polarity of ENABLE pin to input data.

Table 27

EPL	Porality
0	If ENABLE = "L", enables data write operation. (Default) If ENABLE = "H", disables data write operation.
1	If ENABLE = "H", enables data write operation. If ENABLE = "L", disables data write operation.

DPL: Sets the signal polarity of DOTCLK pin.

Table 28

DPL	Porality
0	Take in data on the falling edge of DOTCLK. (Default)
1	Take in data on the rising edge of DOTCLK.

HPL: Sets the signal polarity of HSYNC pin.

Table 29

HPL	Porality
0	Low active. (Default)
1	High active

VPL: Sets the signal polarity of VSYNC pin.

Table 30

VPL	Porality
0	Low active. (Default)
1	High active

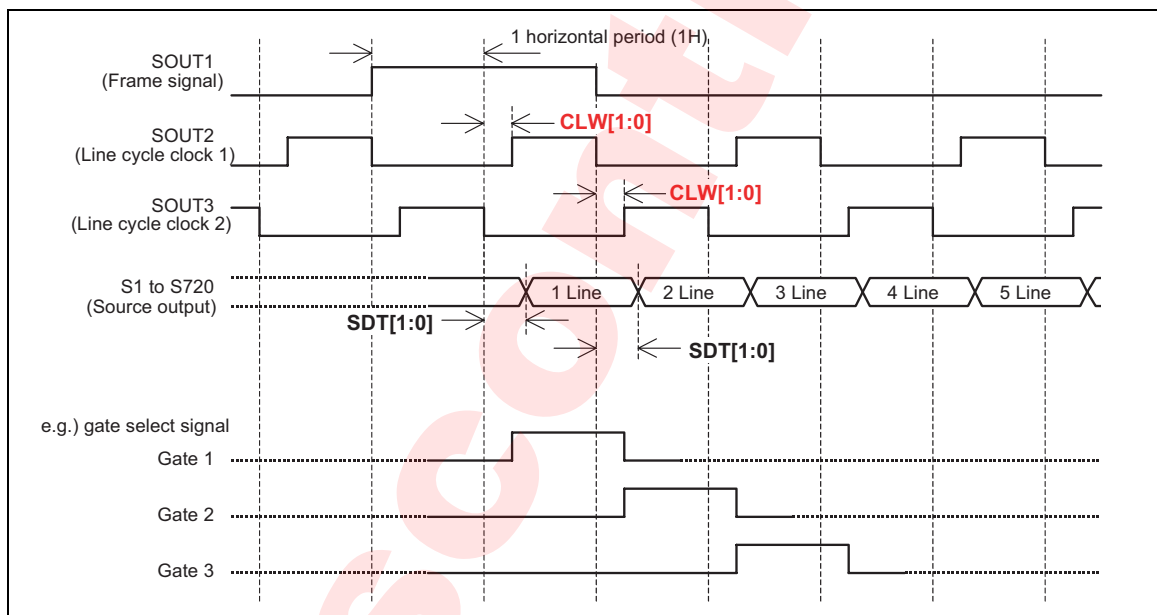


Figure 4

LCD driving waveform control, Source output control: R04h

RS1	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	0	NW 1	NW 0	0	0	0	0	BP3	BP2	BP1	BP0
Default	-	-	-	-	-	-	0	1	-	-	-	-	0	0	1	0

NW[1:0]: Selects the alternating cycle between VcomH and VcomL. For details, see “LCD AC drive”. The register setting is enabled from the next VSYNC assert timing.

Table 31

NW1	NW0	alternating cycle
0	0	Every frame
0	1	Every line (Default)
1	0	Every 2 lines
1	1	Setting disabled

BP[3:0]: Sets the blank period (back porch) in the following figure by line periods. The back porch period should be 14 line periods \geq back porch period \geq 2line periods. The front porch period starts after the end of transfer of display data and lasts until the next VSYNC assert timing. The setting is enabled from the next assert timing

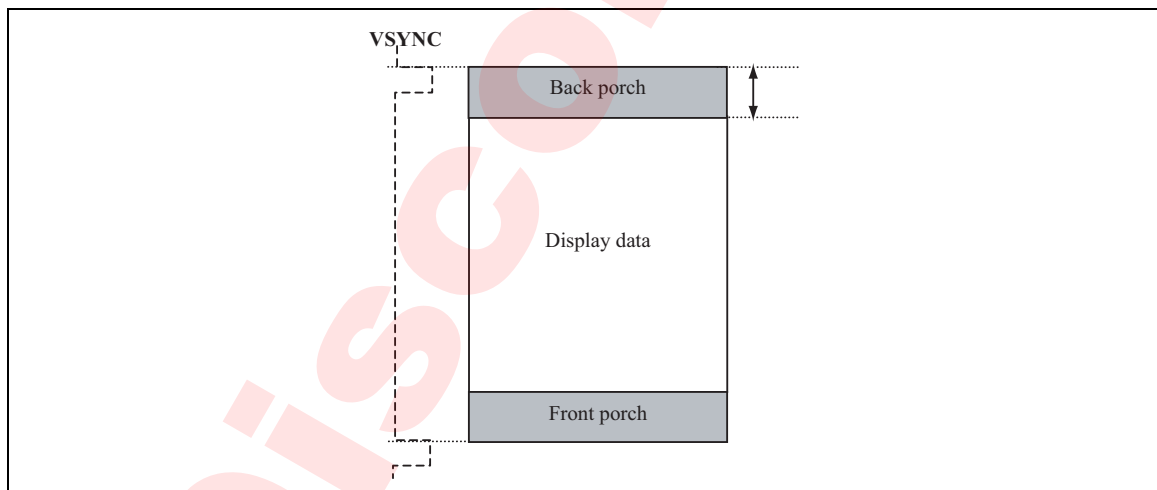


Figure 5

Table 32

BP3	BP2	BP1	BP0	Back porch line period
0	0	0	0	Setting disabled
0	0	0	1	Setting disabled
0	0	1	0	2 line period (Default)
0	0	1	1	3 line period
0	1	0	0	4 line period
0	1	0	0	5 line period
0	1	1	1	6 line period
0	1	1	0	7 line period
1	0	0	0	8 line period
1	0	0	1	9 line period
1	0	1	0	10 line period
1	0	1	1	11 line period
1	1	0	0	12 line period
1	1	0	1	13 line period
1	1	1	0	14 line period
1	1	1	1	Setting disabled

Gate output control: R05h

RS1	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	CLW 1	CLW 0	0	0	NO 1	NO 0	0	0	GA ON	DTE	0	RE V	0	0
Default	-	-	0	0	-	-	0	0	-	-	0	0	-	0	-	-

REV: The relationship between grayscales and output levels can be reversed with REV as follows. The register setting is enabled from the next VSYNC assert timing.

Table 33

REV	Grayscale level	Source output grayscale voltage	
		Positive porality	Negative porality
0	000000b[0]	V0	V63
	111111b[63]	V63	V0
1	000000b[0]	V63	V0
	111111b[63]	V0	V63

DTE: Outputs gate off signal. The register setting is enabled from the next VSYNC assert timing.

Table 34

DTE	Gate off signal	
0	Halt	(Default)
1	Output	

GAON: Sets the level of gate all ON signal. See “LCD display signal control” for details with regard to the selection of output pins. The setting is enabled from the next VSYNC assert timing.

Table 35

GAON	Gate off signal	
0	Gate output signal: SOUT3, SOUT4="0"	(Default)
1	Gate output signal: SOUT3, SOUT4="1"	

NO[1:0]: Sets the non-overlap period of gate off signals. The non-overlap time depends on the DOTCLK frequency.

Table 36

NO1	NO0	Delay	non-overlap period: Delay period when 5MHz	
			18-bit RGB I/F (5MHz)	6-bit RGB I/F (16MHz)
0	0	0 DOTCLK	0.0 μ s	0.0000 μ s (Default)
0	1	20 DOTCLK	4.0 μ s	3.7500 μ s
1	0	30 DOTCLK	6.0 μ s	5.6250 μ s
1	1	40 DOTCLK	8.0 μ s	7.5000 μ s

CLW[1:0]: Sets the output timings of display line cycle clocks (SOUT2, 3). The delay periods change according to the DOTCLK frequency.

Table 37

CLW 1	CLW 0	Delay	non-overlap period: Delay period when 5MHz	
			18-bit RGB I/F (5MHz)	6-bit RGB I/F (16MHz)
0	0	0 DOTCLK	0.0 μ s	0.0000 μ s (Default)
0	1	10 DOTCLK	2.0 μ s	1.8750 μ s
1	0	20 DOTCLK	4.0 μ s	3.6250 μ s
1	1	30 DOTCLK	6.0 μ s	4.6875 μ s

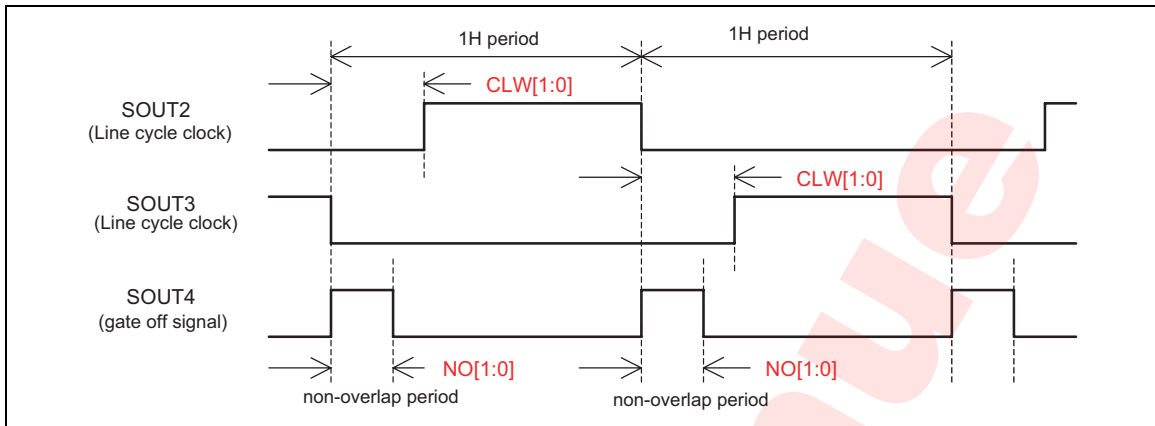


Figure 6

Display signal select control, frame control 1: R06h

RS1	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	IFS	DS C	0	0	GIF 1	GIF 0	FH N	0	FIT 1	FIT 0	0	0	FWI 1	FWI 0
Default	-	-	0	1	-	-	0	0	1	-	1	0	-	-	1	1

IFS: Halt the operation of display circuit by fixing the input level of RGB interface signals (HSYNC, VSYNC, ENABLE, PD17-0, DOTCLK) within the LSI. In this case, the first input level to the interface circuit is active.

When setting IFS = "1" after executing display off and power supply off according to the sleep mode sequence (p.71), the HD66790R enters the sleep mode. In sleep mode, current consumption is in proportion to the input clock frequency. To make the current consumption in sleep mode equal to that in the standby mode, halt all input signals by fixing the level at input stage. The register setting is enabled from the next VSYNC assert timing.

Table 38

IFS	RGB interface input
0	Input (Default)
1	Halt

DSC: Controls ON/OFF of LCD display signals. The register setting is enabled from the next VSYNC assert timing. When DSC = 0, the level shifter outputs signals having amplitude between VGH and VGL from the SOUT1/2/3/4 pins. Be sure to set DSC = "0" before power supply startup. See "Power Supply Setting"(p.70) for details.

Table 39

DSC	SOUT1/2/3/4 output
0	OFF (fix all the output at the VGL level)
1	ON (Default)

Note: SOUT 1/2/3/4 are outputs from the level shifter (voltage: VGH-VGL).

FWI[1:0]: Sets the high width of SOUT1 (frame timing signal). The duration of high width period depends on the DOTCLK frequency. The register setting is enabled from the next VSYNC assert timing.

Table 40

FW11	FW10	High width period	Time for the high width period when 5MHz	
			18-bit RGB I/F (5MHz)	6-bit RGB I/F (16MHz)
0	0	10 DOTCLK	2.0 μ s	1.8750 μ s
0	1	40 DOTCLK	8.0 μ s	7.5000 μ s
1	0	80 DOTCLK	17.0 μ s	15.000 μ s
1	1	Until the end of 1H period	-	- (Default)

FTI1-0: Sets the assert timing of SOUT1 (frame timing signal) in 1H period. The time lag before SOUT1 is asserted depends on the DOTCLK frequency. The register setting is enabled from the next VSYNC assert timing.

Table 41

FT11	FT10	Assert timing delay	Time lag before assert timing when 5MHz	
			18-bit RGB I/F (5MHz)	6-bit RGB I/F (16MHz)
0	0	0.0 DOTCLK	0.0 μ s	0.00000 μ s
0	1	7.5 DOTCLK	1.5 μ s	1.40625 μ s
1	0	17.5 DOTCLK	3.5 μ s	3.28125 μ s
1	1	37.5 DOTCLK	7.5 μ s	7.03125 μ s (Default)

FHN: Sets the assert period of SOUT1 (frame timing signal). The setting is enabled from the next VSYNC assert timing.

Table 42

FHN	Assert period
0	Lasts for up to 1H period. The register setting (FWI[1:0]) is enabled.
1	Lasts for up to 2H periods. (The assert period starts after the delay set with FTI[1:0] and it lasts to the end of next H period irrespective of register setting (FW[1:0])).

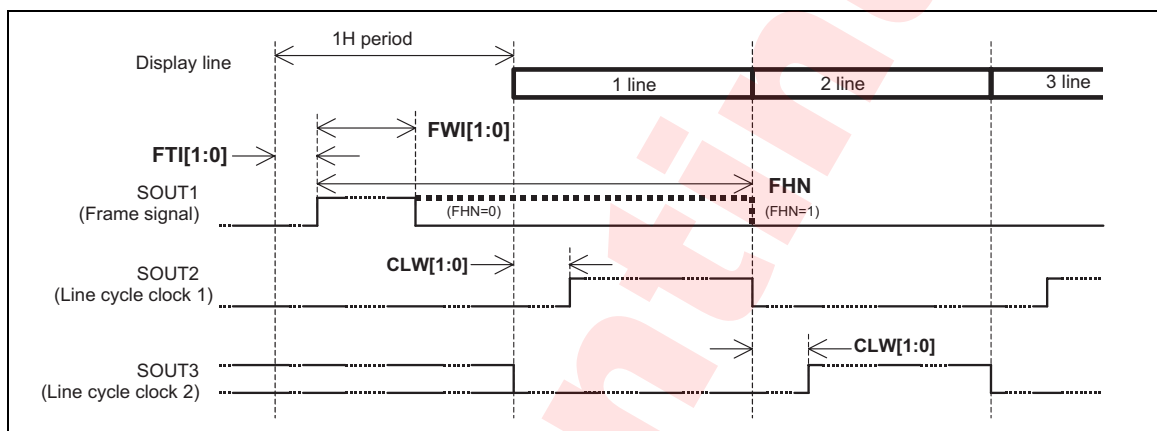


Figure 7

GIF[1:0]: Selects the combination of LCD display signals as follows. The register setting is enabled from the next VSYNC assert timing. When GIF[1:0] = “11”, the assert period always lasts for 1H period whatever the setting of FHN.

Table 43

GIF1	GIF0	SOUT2	SOUT3	SOUT4
0	0	Line cycle clock 1	Line cycle clock 2	Output VGL (Default)
0	1	Line cycle clock 1	Line cycle clock 2	Gate OFF signal
1	0	Line cycle clock 1	Line cycle clock 2	Gate All ON
1	1	Line cycle clock 3	Gate All On	Gate OFF signal

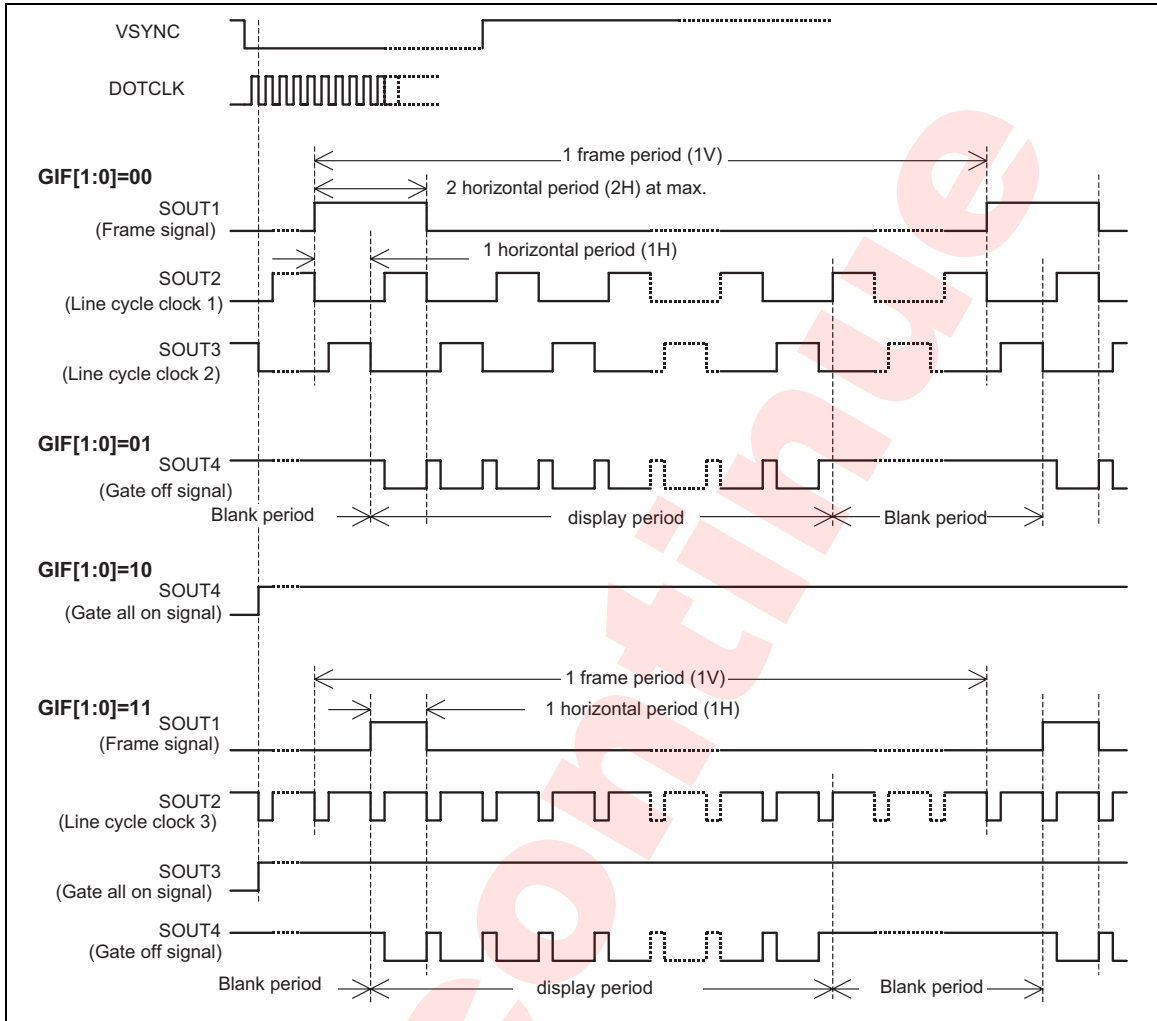


Figure 8

γ Control – positive polarity gradient adjustment: R07h

RS1	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	PRP 12	PRP 11	PRP 10	0	0	0	0	0	PRP 02	PRP 01	PRP 00
Default	-	-	-	-	-	0	0	0	-	-	-	-	0	0	0	0

 γ Control – negative polarity gradient adjustment: R08h

RS1	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	PRN 12	PRN 11	PRN 10	0	0	0	0	0	PRN 02	PRN 01	PRN 00
Default	-	-	-	-	-	0	0	0	-	-	-	-	0	0	0	0

 γ Control – positive polarity amplitude adjustment: R09h

RS1	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	VRP 14	VRP 13	VRP 12	VRP 11	VRP 10	0	0	0	0	VRP 03	VRP 02	VRP 01	VRP 00
Default	-	-	-	0	0	0	0	0	-	-	-	-	0	0	0	0

 γ Control – negative polarity amplitude adjustment: R0Ah

RS1	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	VRN 14	VRN 13	VRN 12	VRN 11	VRN 10	0	0	0	0	VRN 03	VRN 02	VRN 01	VRN 00
Default	-	-	-	0	0	0	0	0	-	-	-	-	0	0	0	0

γ Control – Positive polarity fine adjustment 1: R0Bh

RS1	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	PKP 12	PKP 11	PKP 10	0	0	0	0	0	PKP 02	PKP 01	PKP 00
Default	-	-	-	-	-	0	0	0	-	-	-	-		0	0	0

γ Control – Positive polarity fine adjustment 2: R0Ch

RS1	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	PKP 32	PKP 31	PKP 30	0	0	0	0	0	PKP 22	PKP 21	PKP 20
Default	-	-	-	-	-	0	0	0	-	-	-	-		0	0	0

γ Control – Positive polarity fine adjustment 3: R0Dh

RS1	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	PKP 52	PKP 51	PKP 50	0	0	0	0	0	PKP 42	PKP 41	PKP 40
Default	-	-	-	-	-	0	0	0	-	-	-	-		0	0	0

γ Control – Negative polarity fine adjustment 1: R0Eh

RS1	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	PKN 12	PKN 11	PKN 10	0	0	0	0	0	PKN 02	PKN 01	PKN 00
Default	-	-	-	-	-	0	0	0	-	-	-	-		0	0	0

γ Control – Negative polarity fine adjustment 2: R0Fh

RS1	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	PKN 32	PKN 31	PKN 30	0	0	0	0	0	PKN 22	PKN 21	PKN 20
Default	-	-	-	-	-	0	0	0	-	-	-	-		0	0	0

γ Control – Negative polarity fine adjustment 3: R10h

RS1	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	PKN 52	PKN 51	PKN 50	0	0	0	0	0	PKN 42	PKN 41	PKN 40
Default	-	-	-	-	-	0	0	0	-	-	-	-		0	0	0

Low Power Mode: R26h

RS1	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	0	0	0	0	0	EQ E	SD C	0	TMB 2	TMB 1	TMB 0
Default	-	-	-	-	-	-	-	-	-	-	0	0	-	0	0	0

EQE: Enables source-Vcom equalize function. In equalize period, the Vcom drive operation and source amplifier operation are halted and all source output levels and the Vcom output levels are short-circuited. The equalize period lasts for the delay time set with SDT[1:0] minus 10 DOTCLK periods in 18-bit interface mode. In case of 6-bit interface mode, the equalize period lasts for three times longer than in 18-bit interface mode, i.e. (the delay time set with SDT[1:0] minus (10 DOTCLK periods x 3)).

Table 44

EQE	Function
0	Disenables the source-Vcom equalize function (Default)
1	Enables the source-Vcom equalize function

SDC: The source amplifier operation is halted temporarily when EQE = "0" by setting SDC = "1". The source amplifier halt period lasts for the delay time set with SDT[1:0] minus 10 DOTCLK periods in 18-bit interface mode. In case of 6-bit interface mode, the equalize period lasts for three times longer than in 18-bit interface mode, i.e. (the delay time set with SDT[1:0] minus (10 DOTCLK periods x 3)). When EQE = "1", the source-Vcom equalize function has precedence over this function.

Table 45

SDC	Function
0	Disenables the source amplifier halt function (Default)
1	Enables the source amplifier halt function

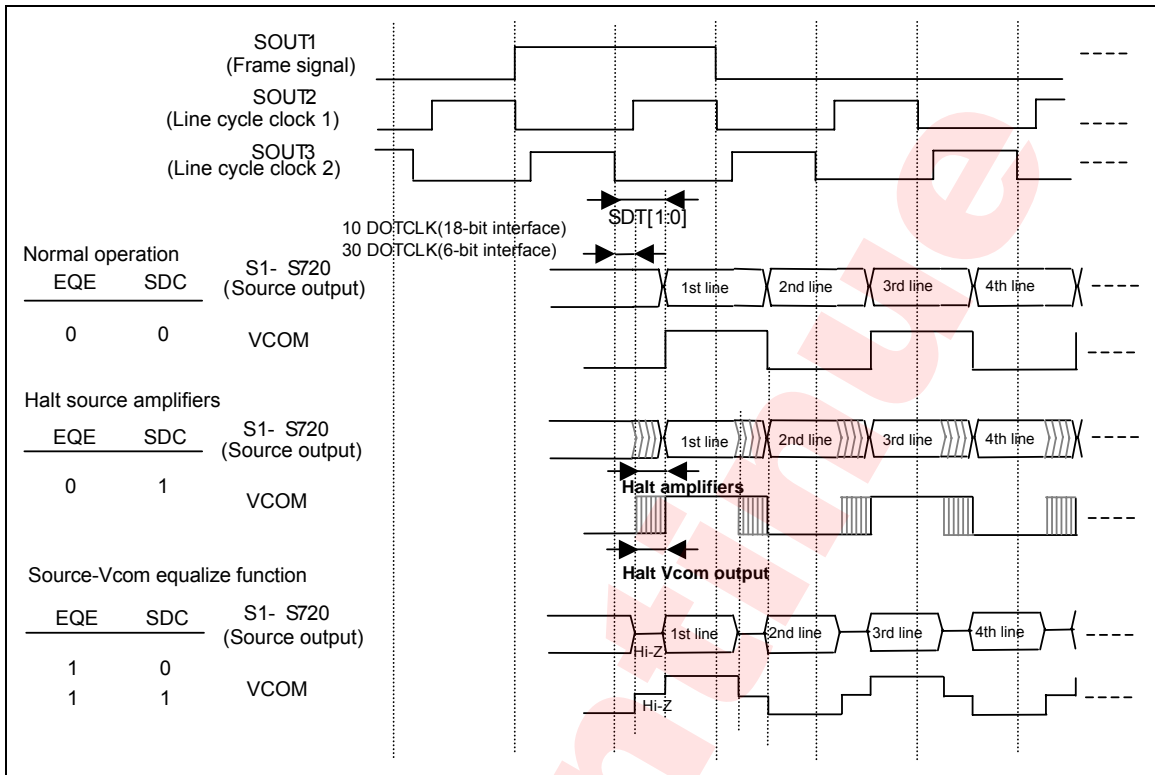


Figure 9

TMB[1:0]: Changes the bias current in source amplifiers according to the drivability and load capacity of the panel. When saving power, set TMB[1:0] = "11" (x 0.8).

Table 46

TMB1	TMB0	Function
0	0	Constant current in source amplifier: x 1 (Default)
0	1	Constant current in source amplifier: x 1.15
1	0	Setting disabled
1	1	Constant current in source amplifier: x 0.8

TMB2: Halts the source amplifier operation when TMB2 = "0". The register setting is enabled from the next VSYNC assert timing.

Table 47

TMB2	Function
0	Halt source amplifiers (Default)
1	Source amplifiers in operation

Instruction List

	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Index	0	0	0	0	0	0	0	0	0	0	0	0	ID4	ID3	ID21	ID1	ID0
R00h	1	0	DC12	DC11	DC10	GON	0	BT2	BT1	BT0	DC02	DC01	DC00	AP2	AP1	AP0	SLP
R01h	1	0	0	0	0	DK	0	POC	0	PON	VRH3	VRH2	VRH1	VRH0	VC2	VC1	VC0
R02h	1	0	0	VCOMG	DVD4	DVD3	DVD2	DVD1	DVD0	0	0	0	VCM4	VCM3	VCM2	VCM1	VCM0
R03h	1	0	VPL	HPL	DPL	EPL	0	0	SHL	0	0	0	0	STD1	STD0	0	0
R04h	1	0	0	0	0	0	0	NW1	NW0	0	0	0	0	BP3	BP2	BP1	BP0
R05h	1	0	0	CLW1	CLW0	0	0	NO1	NO0	0	0	GAON	DTE	0	REV	0	0
R06h	1	0	0	IFS	DSC	0	0	GIF1	GIF0	FHN	0	FT11	FTI0	0	0	FWI1	FWI0
R07h	1	0	0	0	0	0	PRP12	PRP11	PRP10	0	0	0	0	0	PRP02	PRP01	PRP00
R08h	1	0	0	0	0	0	PRN12	PRN11	PRN10	0	0	0	0	0	PRN02	PRN01	PRN00
R09h	1	0	0	0	VRP14	VRP13	VRP12	VRP11	VRP10	0	0	0	0	VRP03	VRP02	VRP01	VRP00
R0Ah	1	0	0	0	VRN14	VRN13	VRN12	VRN11	VRN10	0	0	0	0	VRN03	VRN02	VRN01	VRN00
R0Bh	1	0	0	0	0	0	PKP12	PKP11	PKP10	0	0	0	0	0	PKP02	PKP01	PKP00
R0Ch	1	0	0	0	0	0	PKP32	PKP31	PKP30	0	0	0	0	0	PKP22	PKP21	PKP20
R0Dh	1	0	0	0	0	0	PKP52	PKP51	PKP50	0	0	0	0	0	PKP42	PKP41	PKP40
R0Eh	1	0	0	0	0	0	PKN12	PKN11	PKN10	0	0	0	0	0	PKN02	PKN01	PKN00
R0Fh	1	0	0	0	0	0	PKN32	PKN31	PKN30	0	0	0	0	0	PKN22	PKN21	PKN20
R10h	1	0	0	0	0	0	PKN52	PKN51	PKN50	0	0	0	0	0	PKN42	PKN41	PKN40
R26h	1	0	0	0	0	0	0	0	0	0	0	EQE	SDC	0	TMB2	TMB1	TMB0

Reset Function

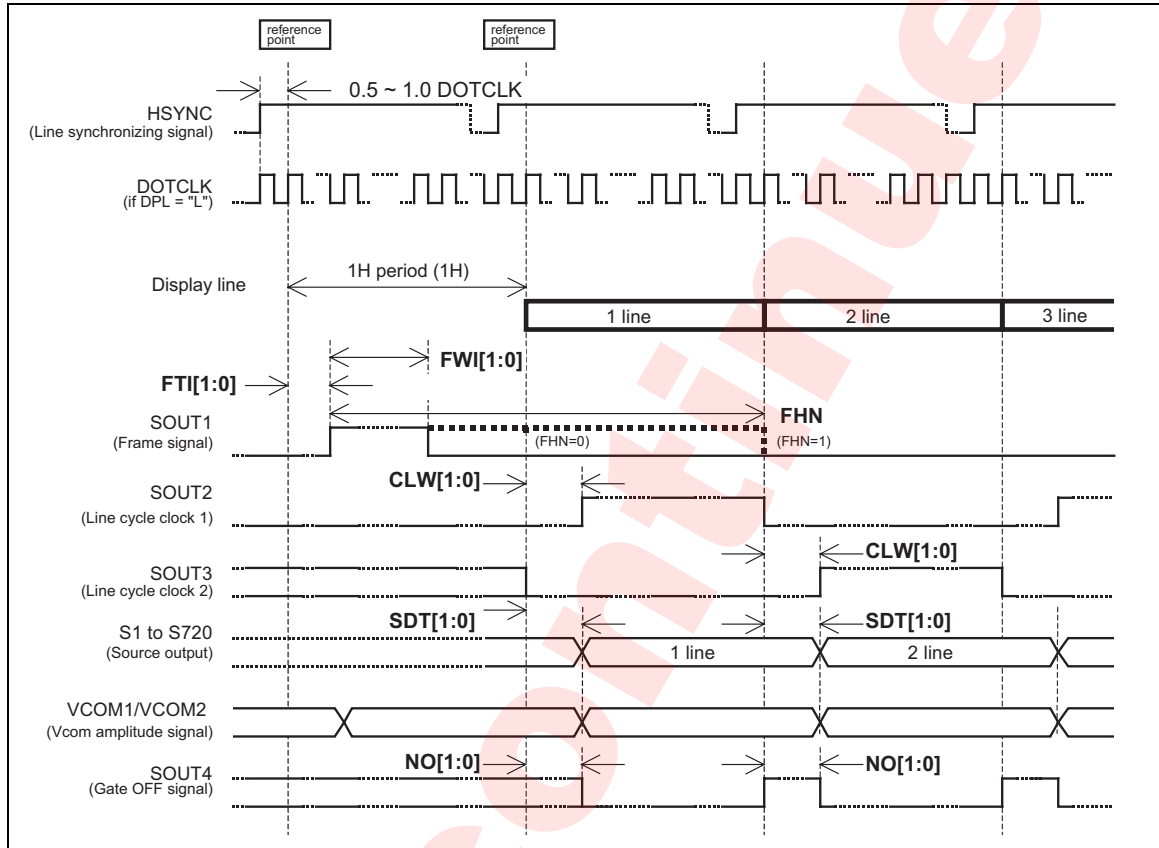
The HD66790R is internally initialized with a RESET input. During the reset period, the internal state of the HD66790R is busy and no access from external devices is accepted. At least 1 ms must be secured for the reset period. In case of power-on reset, any data transfer and initial instruction setting are prohibited.

1. Instruction bits initial state: See the descriptions of each register in the "Instruction" section.
2. Output pin initial state:

LCD display output:	SOUT1-4R/L	Output the "GND" level.
Source output:	S1-S720	Output the "GND" level.
AC drive amplitude signal:	VCOM	Output the "GND" level.

LCD Signal Output Timing Control Function

The following is a timing chart of control signals of the HD66790R.



Note: When GIF[1:0] = "11", the assert period always lasts for 1H period whatever the setting of FHN.

Figure 10

Power Control Function

When POC = “L”, all-white display is on the screen.

- Notes: 1. The panel display signals from the SOUT1/2/3/4 pins are output normally.
- 2. The changes in register setting POC is enabled in synchronization with the VSYNC signal and the source output level as a result of the change in setting is output from the next assert timing.

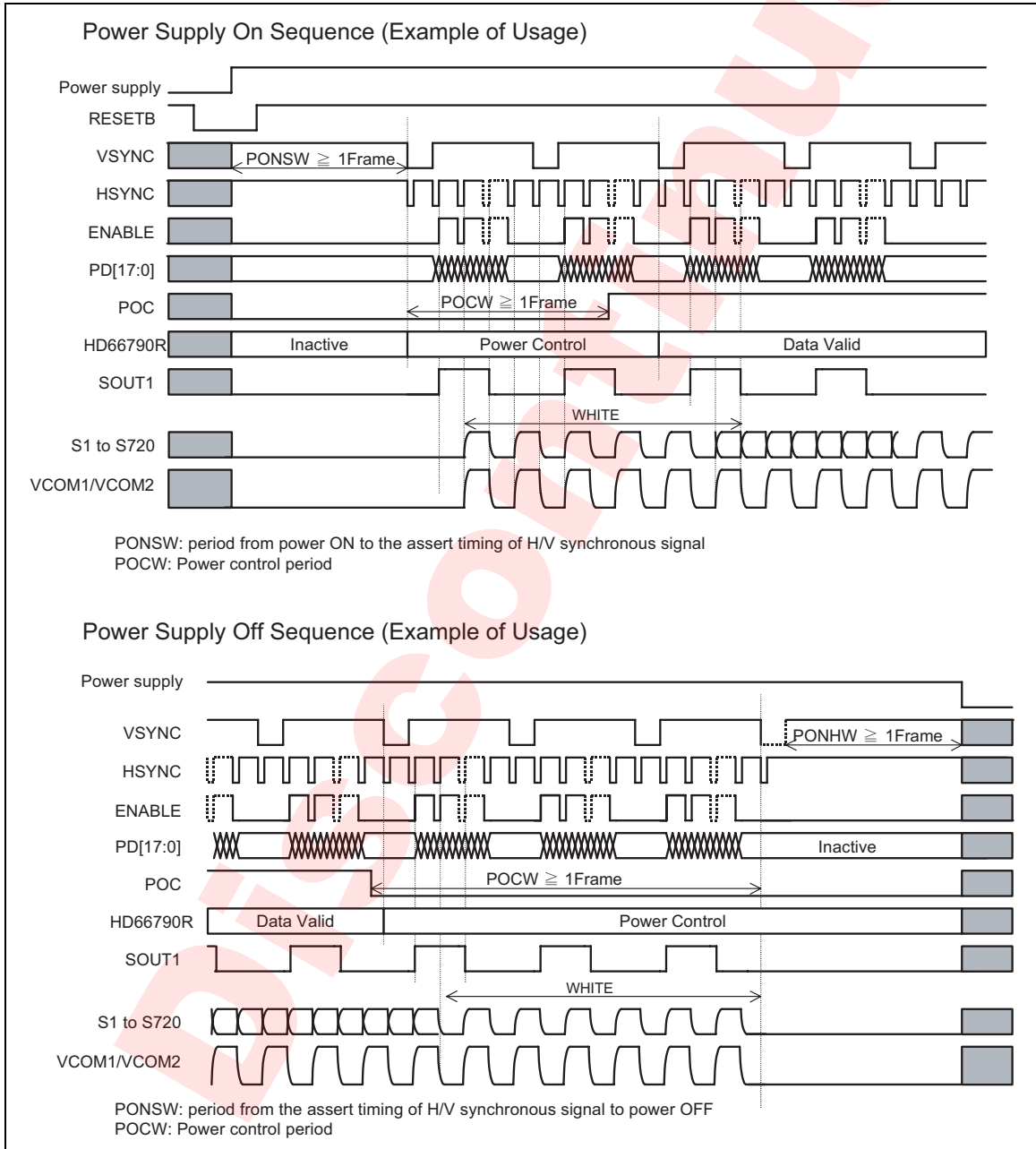


Figure 11

POC, VCOMG, LSENRL output control

The register setting of the three bits and respective output control functions are as follows.

Source output (Sn) control with POC**Table 48**

POC	Operation mode	Source output (Sn)
0	Power control mode	WHITE level
1	Normal operation mode	Input data

Panel display signals (SOUT*) control with LSENRL/LSNR**Table 49**

LSENL	LSNR	Level shifter output level	
		SOUT1/2/3/4L	SOUT1/2/3/4R
0	0	Fixed to VGL	Fixed to VGL
0	1	Fixed to VGL	VGH – VGL
1	0	VGH – VGL	Fixed to VGL
1	1	VGH – VGL	VGH – VGL

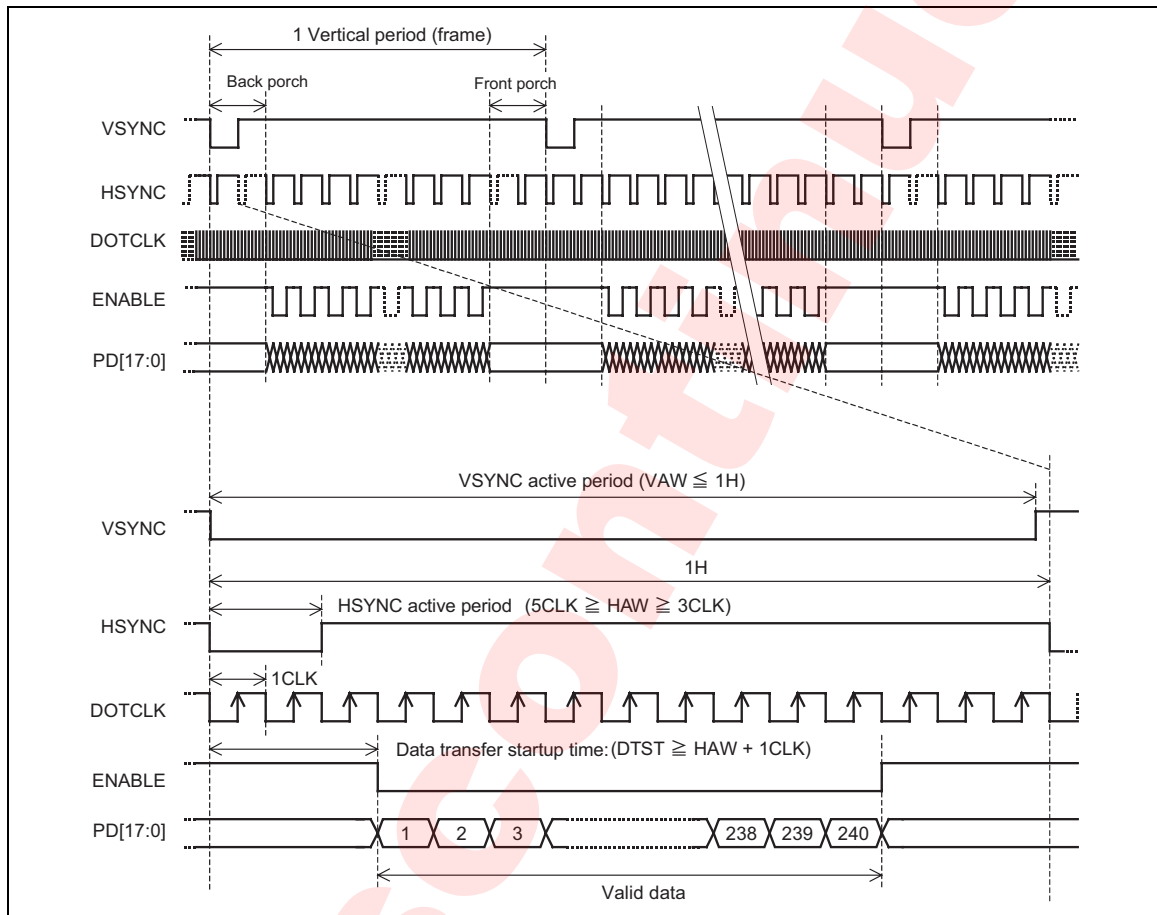
VCOM control with VCOMG**Table 50**

VCOMG	VCOM output
0	GND
1	Vcom output

RGB Interface timing

The following are timing charts of RGB interface signals.

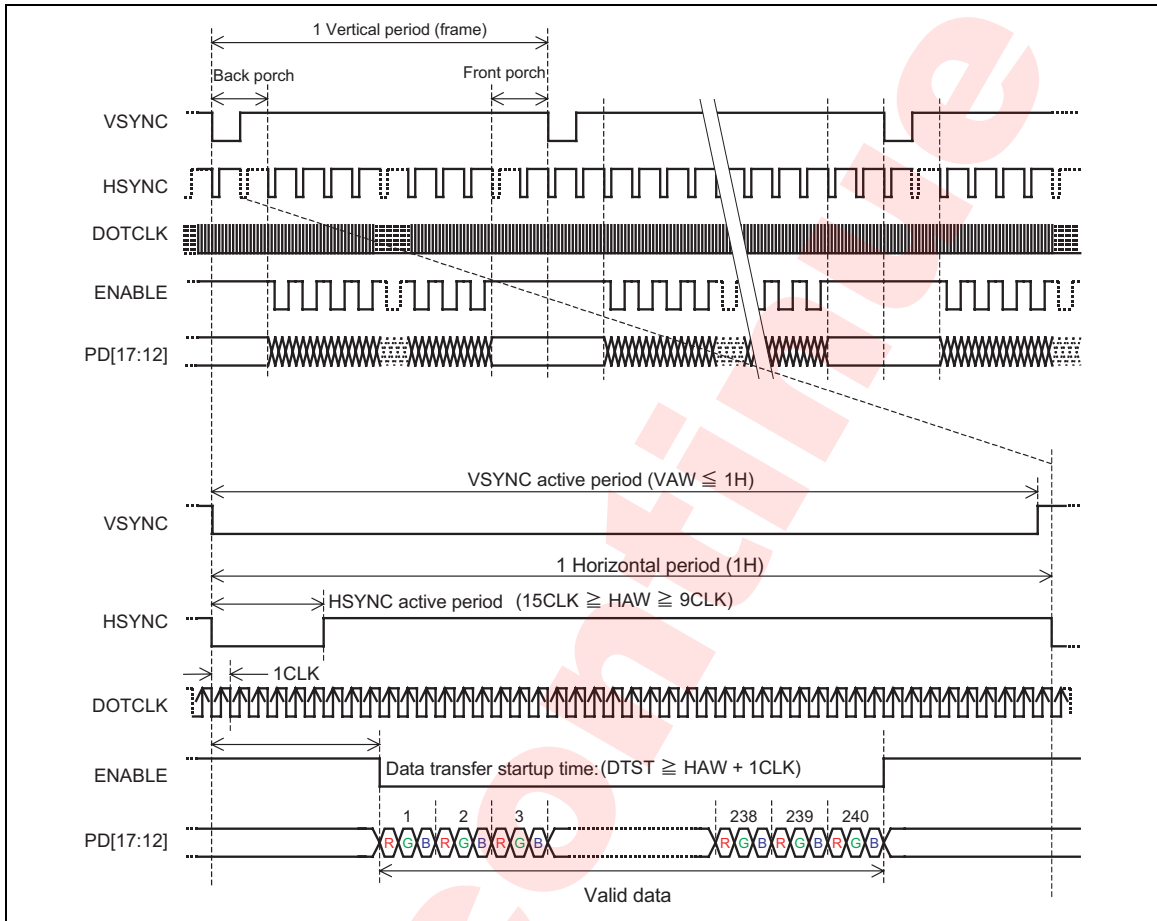
RGB interface timing 1 (18-bit transfer mode)



VAW: VSYNC active period
 HAW: HSYNC active period
 DTST: data transfer startup time

Figure 12

RGB interface timing 2 (6-bit x 3 transfers)



VAW: VSYNC active period
 HAW: HSYNC active period
 DTST: data transfer startup time

Figure 13

LCD panel interface timing

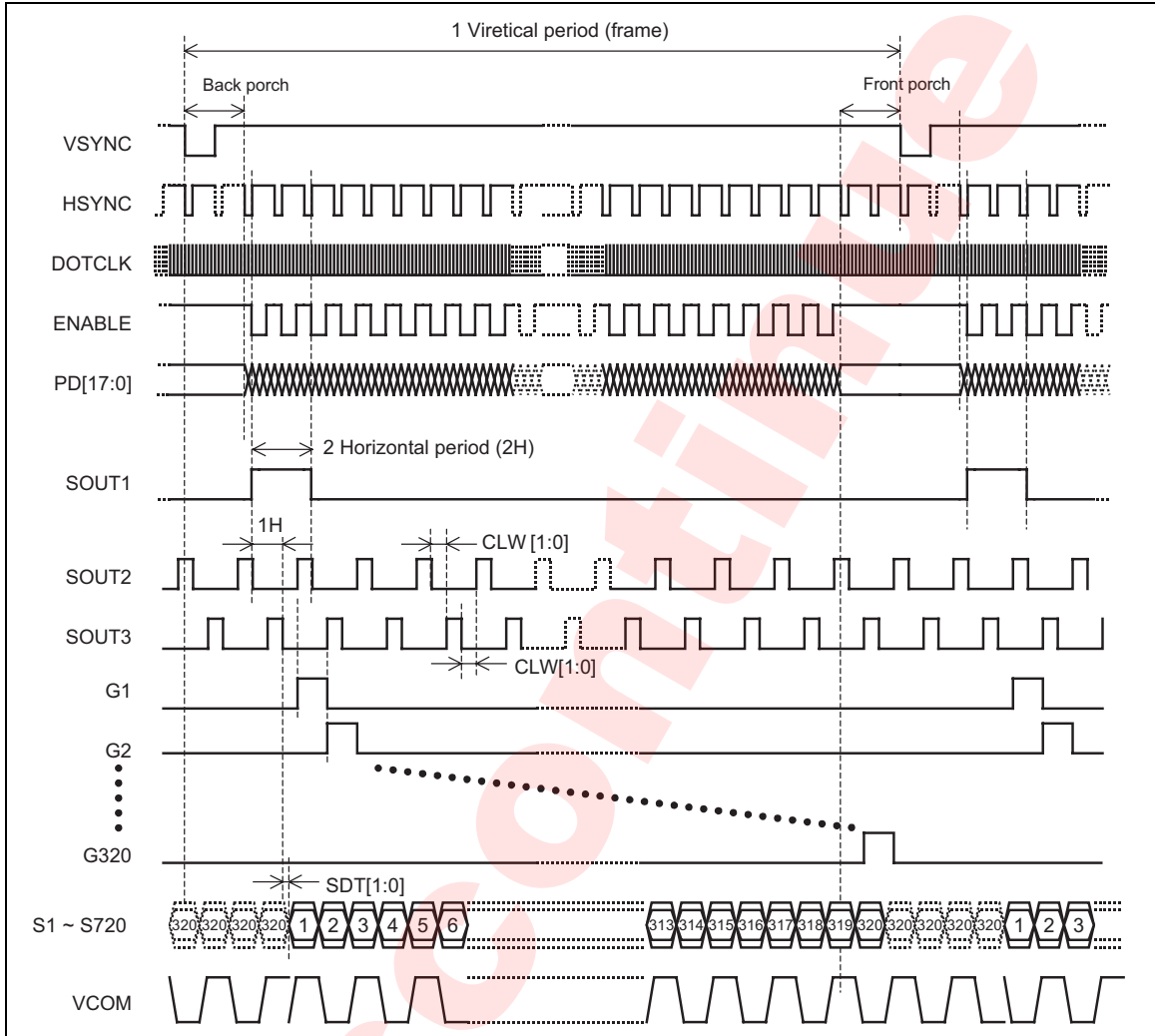


Figure 14

Serial Interface

The HD66790R allows changes in register setting via serial interface using 3 ports: chip select (CS); serial clock (SCL); and serial data input (SDI).

The HD66790R recognizes the start of data transfer on a falling edge of CS and starts taking in data. The HD66790R recognizes the end of data transfer on a rising edge of CS and stops transferring data. The data are transferred in units of 16 bits from the MSB.

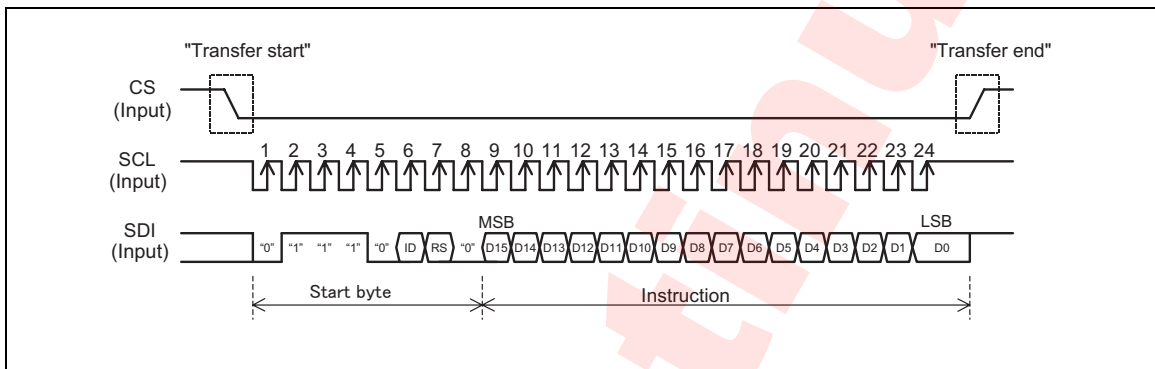


Figure 15

Data Shift Direction

The HD66790R allows changing the shift direction of data output from source pins by setting the register R03h: D8 (SHL bit). Select either direction according to the LC module.

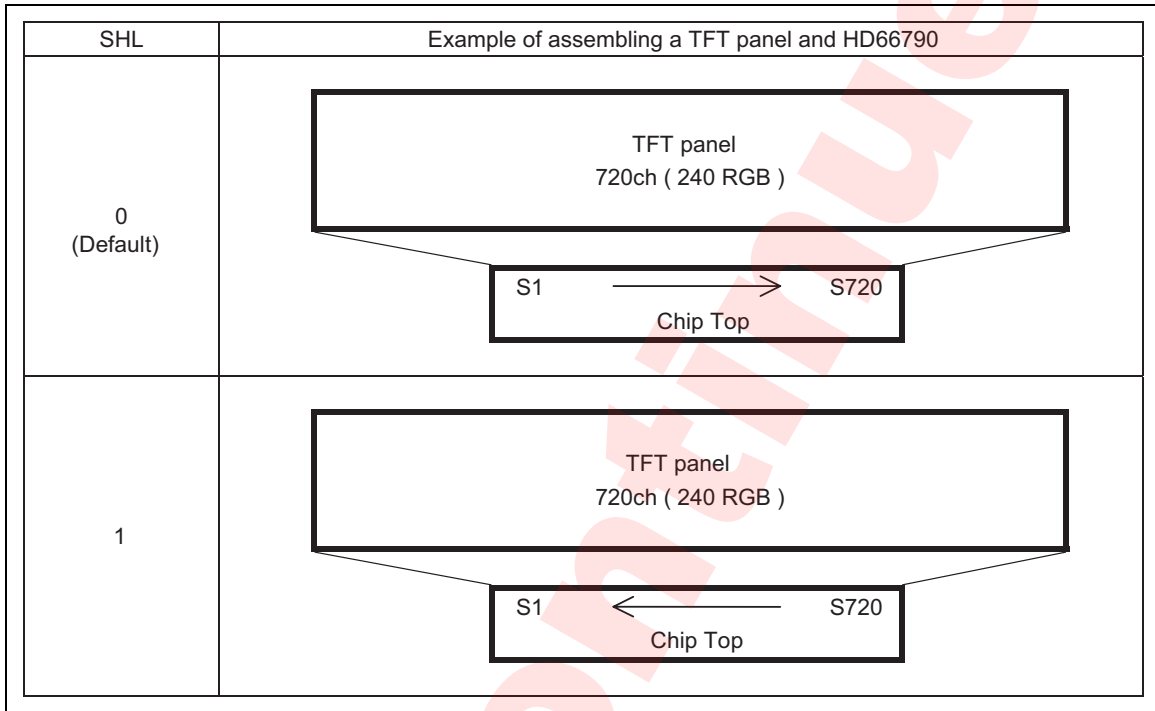


Figure 16

Liquid Crystal AC Drive

The HD66790R supports line-inversion and 2-line inversion AC drive in addition to frame-inversion AC drive. The alternating cycle is selected by setting the register R04h:D[9:8](NW[1:0] bits). Check the quality of display on the panel in selecting the alternating cycle. Note that the shorter alternating interval increases charging/discharging current on liquid crystal cells because of increase in liquid crystal alternating frequency.

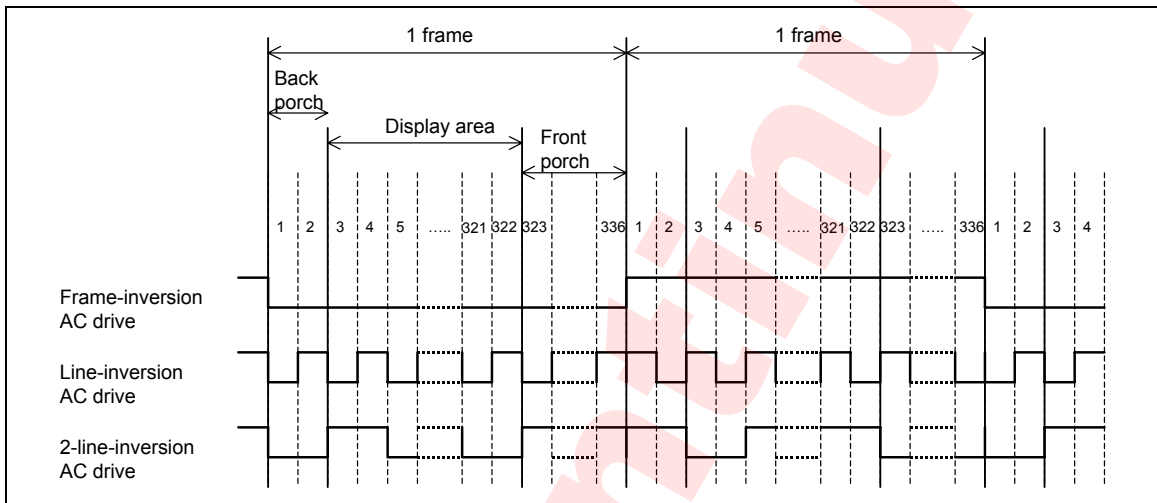


Figure 17

LCD Display Signal Control

The HD66790R allows selecting the optimal combination of LCD signals according to the structure of the system. Also, see the description of “Display signal select control: R06h” in the “Instruction” section for details on the timing relationship of these signals.

Register setting

Table 51

DSC	GIF1	GIF0	Voltage amplitude of outputs from the Level shifter: VGH-VGL (unless specified otherwise)		
			SOUT2	SOUT3	SOUT4
0	0	0			
	0	1			
	1	0		Output the VGL level	
	1	1			
1	0	0			Output the VGL level
	0	1	Line cycle clock 1	Line cycle clock 2	Gate off signal
	1	0			Gate-all-on signal
	1	1	Line cycle clock 3	Gate-all-on signal	Gate off signal

Grayscale Amplifier Unit Configuration

The following figure shows the configuration of grayscale amplifier unit of the HD66790R. The power supply input levels VREF0P ~ VREF4P, VREF0N ~ VREF4N are divided internally with internal resistors to generate 64 voltage levels for grayscales V0 ~ V63.

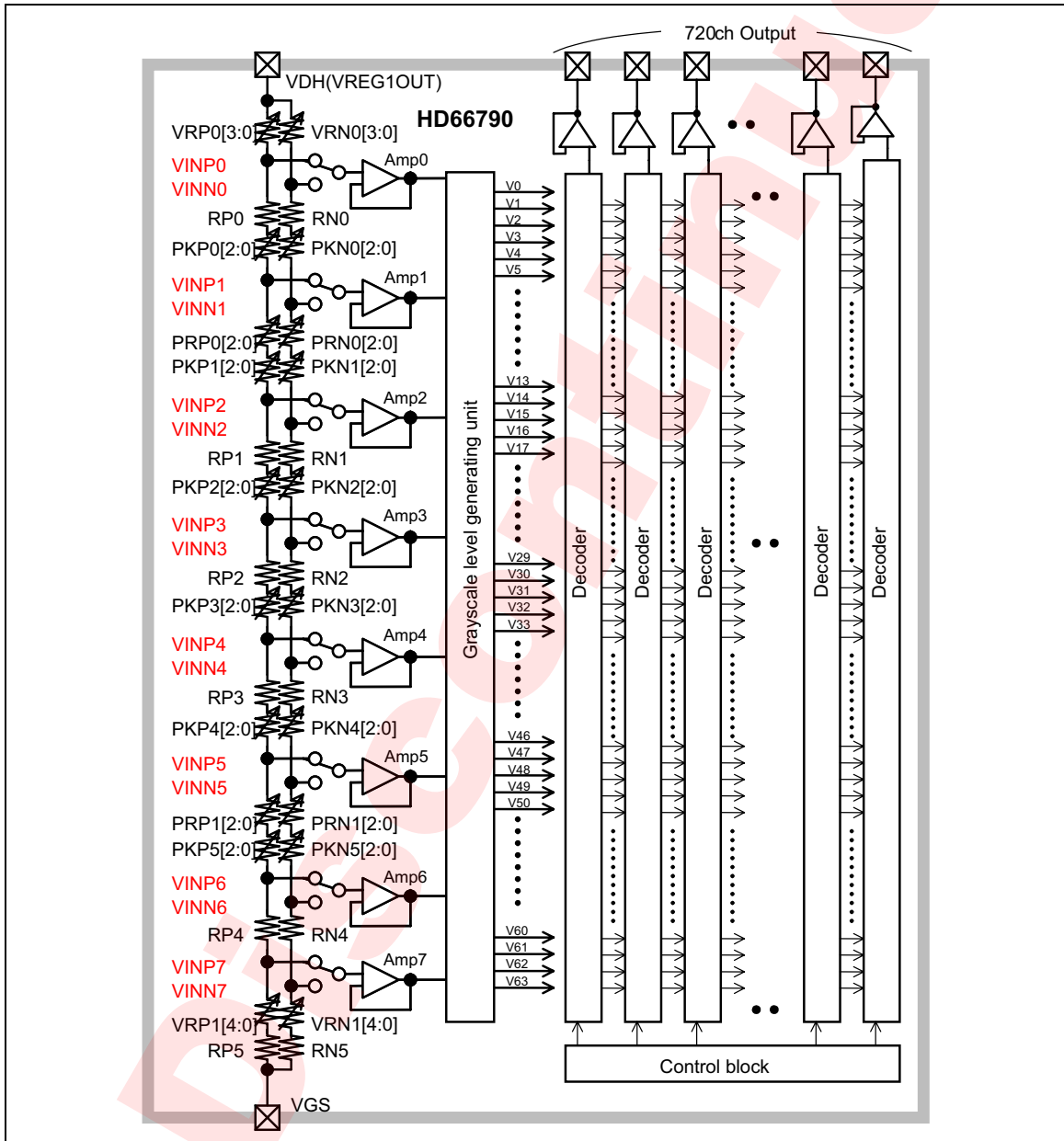


Figure 18

Configuration of grayscale level generating unit

The following is the configuration of grayscale level generating unit. To generate 64 grayscale voltage levels (V0~V63), the HD66790R first generates eight reference grayscale levels (VINP0-7/VINN0-7) according to the gradient and fine adjustment registers, which are then divided with the ladder resistors in the grayscale amplifier unit.

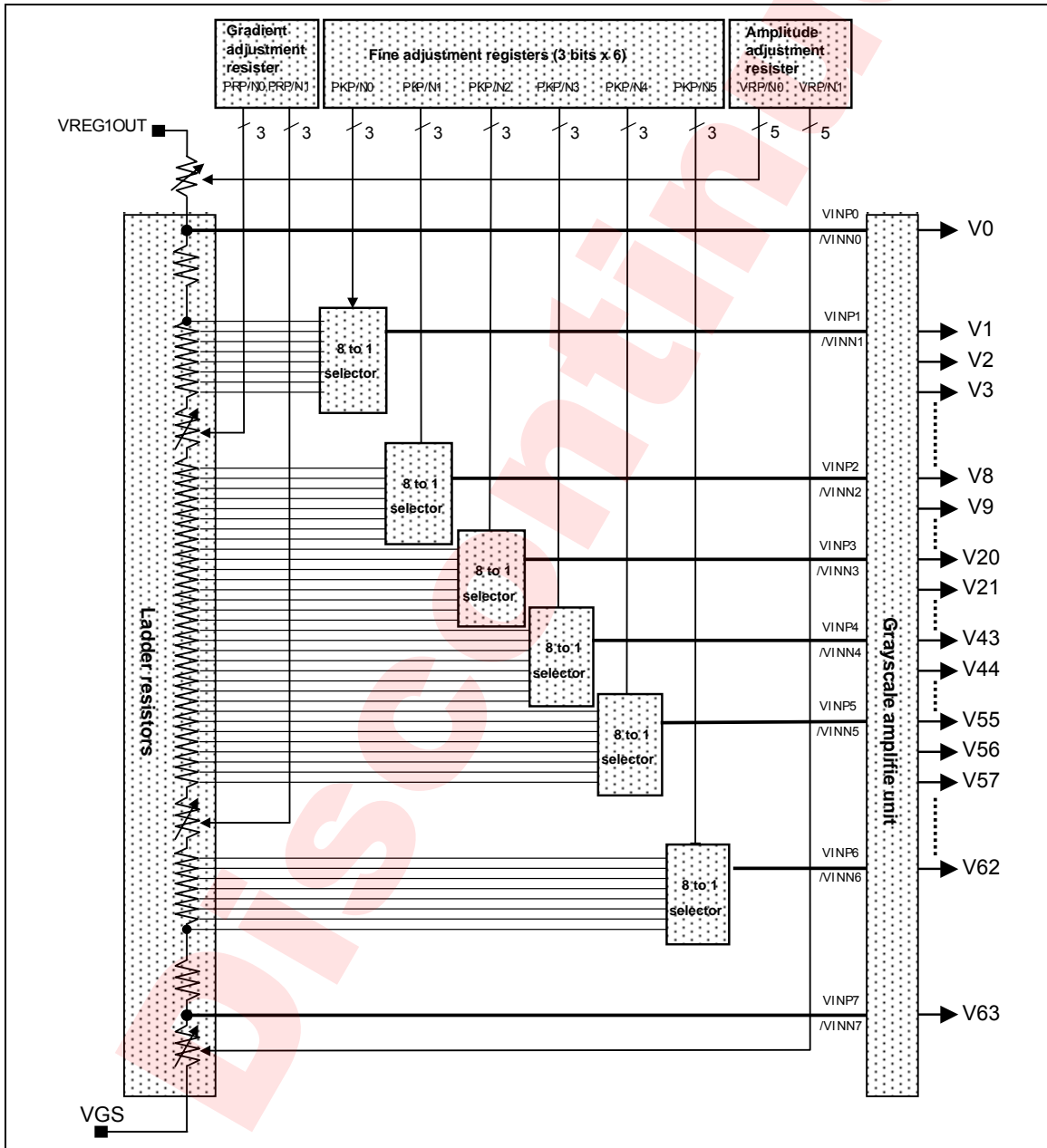


Figure 19

Reference voltage generating block (ladder resistor units and 8-to-1 selectors)

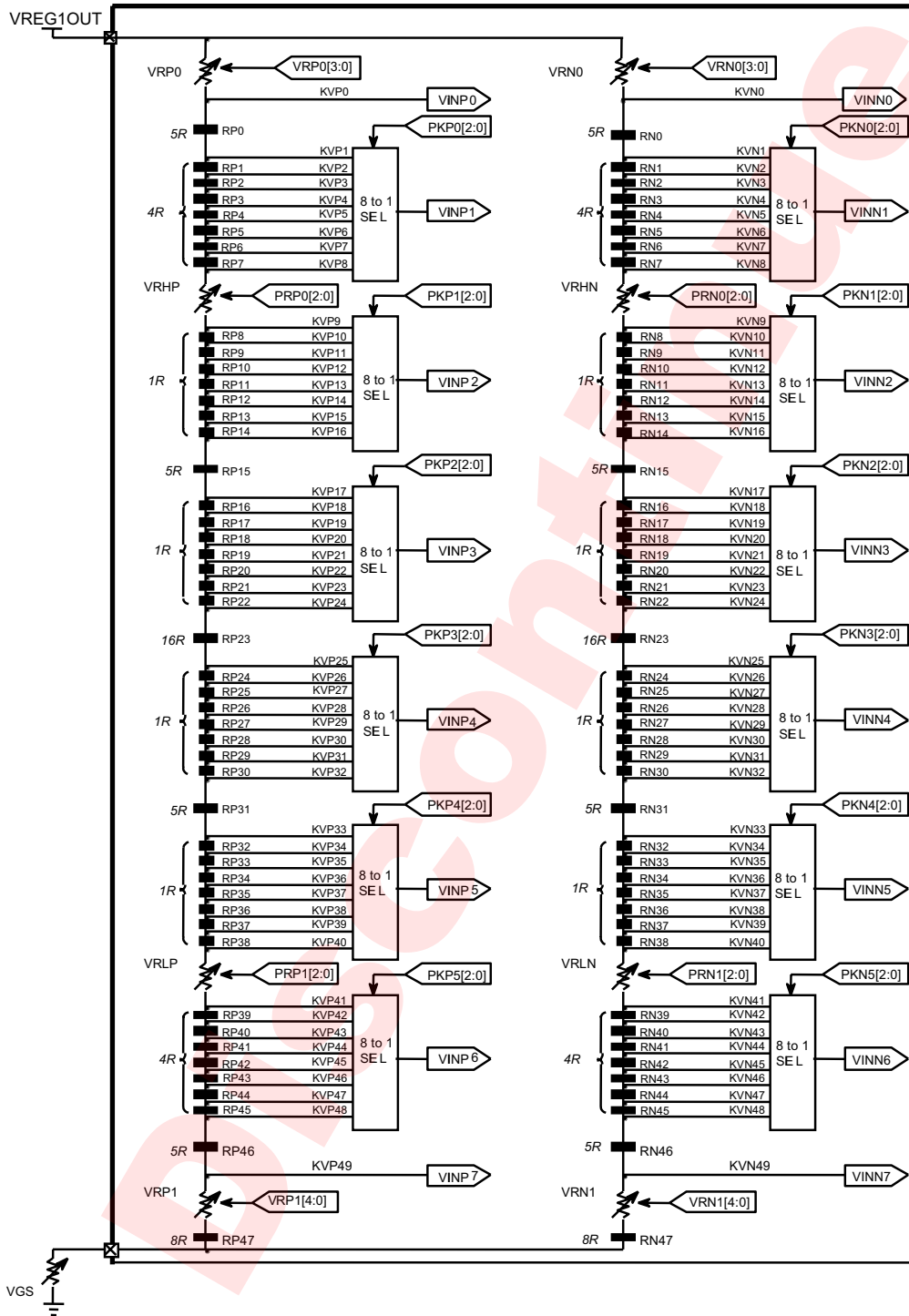


Figure 20 Reference voltage generating block (ladder resistor units and 8-to-1 selectors)

γ -Correction Register

The γ -correction registers of the HD66790R consist of gradient adjustment, amplitude adjustment, and fine-adjustment registers, each consists of registers of positive and negative polarities. Each register can be set independently, enabling optimal adjustment of grayscale voltage levels in relation to grayscales for the γ -characteristics of the liquid crystal panel. These settings in the γ -correction registers and the reference levels for the 64 grayscales, to which these three kinds of adjustments are made, are common to all RGB dots.

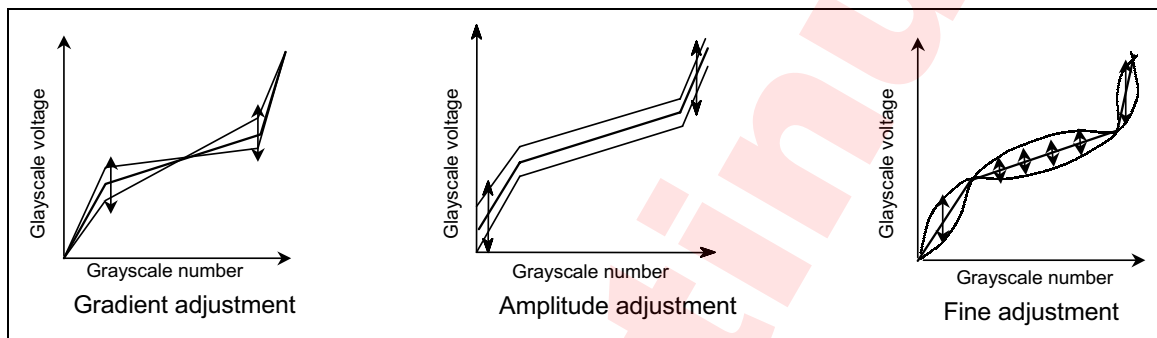


Figure 21

1. Gradient adjustment registers

The gradient adjustment registers are used to adjust the gradient representing the grayscale-voltage relationship for the middle grayscale numbers without changing the dynamic range by changing the resistance values of the resistors (VRHP(N)/VRLP(N)) in the middle of the ladder resistor unit. The gradient adjustment registers consist of positive and negative polarity registers to allow for asymmetric drive.

2. Amplitude adjustment registers

The amplitude adjustment registers are used to adjust the amplitude of the grayscale voltage by changing the resistance values of the resistors (VRP(N)1/0) at both ends of the ladder resistor unit. Same with the gradient registers, the amplitude adjustment registers consist of positive and negative polarity registers.

3. Fine adjustment registers

The fine adjustment registers are used for minute adjustment of grayscale voltage levels. The fine adjustment register represent one voltage level to be selected in the 8-to-1 selector among 8 levels generated from the ladder resistor unit. Same with other registers, the fine adjustment registers consist of positive and negative polarity registers.

Table 52

Register Groups	Positive Polarity	Negative Polarity	Description
Gradient adjustment	PRP0 [2:0]	PRN0 [2:0]	Variable resistor VRHP (N)
	PRP1 [2:0]	PRN1 [2:0]	Variable resistor VRLP (N)
Amplitude adjustment	VRP0 [3:0]	VRN0 [3:0]	Variable resistor VRP (N)0
	VRP1 [4:0]	VRN1 [4:0]	Variable resistor VRP (N)1
Fine adjustment	PKP0 [2:0]	PKN0 [2:0]	8-to-1 selector (voltage level of grayscale 1)
	PKP1 [2:0]	PKN1 [2:0]	8-to-1 selector (voltage level of grayscale 8)
	PKP2 [2:0]	PKN2 [2:0]	8-to-1 selector (voltage level of grayscale 20)
	PKP3 [2:0]	PKN3 [2:0]	8-to-1 selector (voltage level of grayscale 43)
	PKP4 [2:0]	PKN4 [2:0]	8-to-1 selector (voltage level of grayscale 55)
	PKP5 [2:0]	PKN5 [2:0]	8-to-1 selector (voltage level of grayscale 62)

Ladder resistors and 8-to-1 selector

Block configuration

The reference voltage generating unit as illustrated in page 59 consists of two ladder resistor unit including variable resistors and 8-to-1 selectors. In this unit, one voltage level is selected in each 8-to-1 selector among 8 levels generated by ladder resistors and it is output as the reference voltage for generating 64 grayscale voltage levels. The γ correction registers represent the resistance values of these resistors in the ladder resistor unit and the reference levels selected in the 8-to-1 selectors (Table 52). This unit has a pin to connect a volume resistor for adjusting the characteristics of the panel.

Variable resistors

The HD6690R uses variable resistors for the following three purposes: gradient adjustment (VRHP(N)/VRLP(N)); amplitude adjustment (1) (VRP(N)0); and amplitude adjustment (2) (VRP(N)1). The resistance values are determined by gradient adjustment and amplitude adjustment registers as below.

Table 53

Gradient adjustment

Contents of Register PRP(N) 0/1[2:0]	Resistance VRHP(N) VRLP(N)
000	0R
001	4R
010	8R
011	12R
100	16R
101	20R
110	24R
111	28R

Table 54

Amplitude adjustment (1)

Contents of Register VRP(N)0[3:0]	Resistance VRP(N)0
0000	0R
0001	2R
0010	4R
:	:
:	:
1101	26R
1111	28R
1111	30R

Table 55

Amplitude adjustment (2)

Contents of Register VRP(N)1[4:0]	Resistance VRP(N)1
00000	0R
00001	1R
00010	2R
:	:
:	:
11101	29R
11110	30R
11111	31R

8-to-1 selectors

The 8-to-1 selector selects one voltage level according to the bits in the fine adjustment register among eight voltage levels generated by ladder resistors, and output the selected level as the reference voltage (VINP(N)1~6). The following table shows the correspondence between the selected voltage levels and the values represented by the fine adjustment registers for respective reference voltage levels (VINP(N)1~6).

Table 56 Fine adjustment registers and selected voltage

The value of Register PKP(N)[2:0]	Selected Voltage					
	VINP(N)1	VINP(N)2	VINP(N)3	VINP(N)4	VINP(N)5	VINP(N)6
000	KVP(N)1	KVP(N)9	KVP(N)17	KVP(N)25	KVP(N)33	KVP(N)41
001	KVP(N)2	KVP(N)10	KVP(N)18	KVP(N)26	KVP(N)34	KVP(N)42
010	KVP(N)3	KVP(N)11	KVP(N)19	KVP(N)27	KVP(N)35	KVP(N)43
011	KVP(N)4	KVP(N)12	KVP(N)20	KVP(N)28	KVP(N)36	KVP(N)44
100	KVP(N)5	KVP(N)13	KVP(N)21	KVP(N)29	KVP(N)37	KVP(N)45
101	KVP(N)6	KVP(N)14	KVP(N)22	KVP(N)30	KVP(N)38	KVP(N)46
110	KVP(N)7	KVP(N)15	KVP(N)23	KVP(N)31	KVP(N)39	KVP(N)47
111	KVP(N)8	KVP(N)16	KVP(N)24	KVP(N)32	KVP(N)40	KVP(N)48

Grayscale voltage calculating formulae (Positive polarity)

Table 57

Pin	Equation	Fine adjustment register setting	Reference Voltage
KVP0	$VREG1OUT - \Delta V * VRP0 / SUMRP$	-	VINP0
KVP1	$VREG1OUT - \Delta V * (VRP0 + 5R) / SUMRP$	PKP02-00 = "000"	VINP1
KVP2	$VREG1OUT - \Delta V * (VRP0 + 9R) / SUMRP$	PKP02-00 = "001"	
KVP3	$VREG1OUT - \Delta V * (VRP0 + 13R) / SUMRP$	PKP02-00 = "010"	
KVP4	$VREG1OUT - \Delta V * (VRP0 + 17R) / SUMRP$	PKP02-00 = "011"	
KVP5	$VREG1OUT - \Delta V * (VRP0 + 21R) / SUMRP$	PKP02-00 = "100"	
KVP6	$VREG1OUT - \Delta V * (VRP0 + 25R) / SUMRP$	PKP02-00 = "101"	
KVP7	$VREG1OUT - \Delta V * (VRP0 + 29R) / SUMRP$	PKP02-00 = "110"	
KVP8	$VREG1OUT - \Delta V * (VRP0 + 33R) / SUMRP$	PKP02-00 = "111"	
KVP9	$VREG1OUT - \Delta V * (VRP0 + 33R + VRHP) / SUMRP$	PKP12-10 = "000"	VINP2
KVP10	$VREG1OUT - \Delta V * (VRP0 + 34R + VRHP) / SUMRP$	PKP12-10 = "001"	
KVP11	$VREG1OUT - \Delta V * (VRP0 + 35R + VRHP) / SUMRP$	PKP12-10 = "010"	
KVP12	$VREG1OUT - \Delta V * (VRP0 + 36R + VRHP) / SUMRP$	PKP12-10 = "011"	
KVP13	$VREG1OUT - \Delta V * (VRP0 + 37R + VRHP) / SUMRP$	PKP12-10 = "100"	
KVP14	$VREG1OUT - \Delta V * (VRP0 + 38R + VRHP) / SUMRP$	PKP12-10 = "101"	
KVP15	$VREG1OUT - \Delta V * (VRP0 + 39R + VRHP) / SUMRP$	PKP12-10 = "110"	
KVP16	$VREG1OUT - \Delta V * (VRP0 + 40R + VRHP) / SUMRP$	PKP12-10 = "111"	
KVP17	$VREG1OUT - \Delta V * (VRP0 + 45R + VRHP) / SUMRP$	PKP22-20 = "000"	VINP3
KVP18	$VREG1OUT - \Delta V * (VRP0 + 46R + VRHP) / SUMRP$	PKP22-20 = "001"	
KVP19	$VREG1OUT - \Delta V * (VRP0 + 47R + VRHP) / SUMRP$	PKP22-20 = "010"	
KVP20	$VREG1OUT - \Delta V * (VRP0 + 48R + VRHP) / SUMRP$	PKP22-20 = "011"	
KVP21	$VREG1OUT - \Delta V * (VRP0 + 49R + VRHP) / SUMRP$	PKP22-20 = "100"	
KVP22	$VREG1OUT - \Delta V * (VRP0 + 50R + VRHP) / SUMRP$	PKP22-20 = "101"	
KVP23	$VREG1OUT - \Delta V * (VRP0 + 51R + VRHP) / SUMRP$	PKP22-20 = "110"	
KVP24	$VREG1OUT - \Delta V * (VRP0 + 52R + VRHP) / SUMRP$	PKP22-20 = "111"	
KVP25	$VREG1OUT - \Delta V * (VRP0 + 68R + VRHP) / SUMRP$	PKP32-30 = "000"	VINP4
KVP26	$VREG1OUT - \Delta V * (VRP0 + 69R + VRHP) / SUMRP$	PKP32-30 = "001"	
KVP27	$VREG1OUT - \Delta V * (VRP0 + 70R + VRHP) / SUMRP$	PKP32-30 = "010"	
KVP28	$VREG1OUT - \Delta V * (VRP0 + 71R + VRHP) / SUMRP$	PKP32-30 = "011"	
KVP29	$VREG1OUT - \Delta V * (VRP0 + 72R + VRHP) / SUMRP$	PKP32-30 = "100"	
KVP30	$VREG1OUT - \Delta V * (VRP0 + 73R + VRHP) / SUMRP$	PKP32-30 = "101"	
KVP31	$VREG1OUT - \Delta V * (VRP0 + 74R + VRHP) / SUMRP$	PKP32-30 = "110"	
KVP32	$VREG1OUT - \Delta V * (VRP0 + 75R + VRHP) / SUMRP$	PKP32-30 = "111"	
KVP33	$VREG1OUT - \Delta V * (VRP0 + 80R + VRHP) / SUMRP$	PKP42-40 = "000"	VINP5
KVP34	$VREG1OUT - \Delta V * (VRP0 + 81R + VRHP) / SUMRP$	PKP42-40 = "001"	
KVP35	$VREG1OUT - \Delta V * (VRP0 + 82R + VRHP) / SUMRP$	PKP42-40 = "010"	
KVP36	$VREG1OUT - \Delta V * (VRP0 + 83R + VRHP) / SUMRP$	PKP42-40 = "011"	
KVP37	$VREG1OUT - \Delta V * (VRP0 + 84R + VRHP) / SUMRP$	PKP42-40 = "100"	
KVP38	$VREG1OUT - \Delta V * (VRP0 + 85R + VRHP) / SUMRP$	PKP42-40 = "101"	
KVP39	$VREG1OUT - \Delta V * (VRP0 + 86R + VRHP) / SUMRP$	PKP42-40 = "110"	
KVP40	$VREG1OUT - \Delta V * (VRP0 + 87R + VRHP) / SUMRP$	PKP42-40 = "111"	
KVP41	$VREG1OUT - \Delta V * (VRP0 + 87R + VRHP + VRLP) / SUMRP$	PKP52-50 = "000"	VINP6
KVP42	$VREG1OUT - \Delta V * (VRP0 + 91R + VRHP + VRLP) / SUMRP$	PKP52-50 = "001"	
KVP43	$VREG1OUT - \Delta V * (VRP0 + 95R + VRHP + VRLP) / SUMRP$	PKP52-50 = "010"	
KVP44	$VREG1OUT - \Delta V * (VRP0 + 99R + VRHP + VRLP) / SUMRP$	PKP52-50 = "011"	
KVP45	$VREG1OUT - \Delta V * (VRP0 + 103R + VRHP + VRLP) / SUMRP$	PKP52-50 = "100"	
KVP46	$VREG1OUT - \Delta V * (VRP0 + 107R + VRHP + VRLP) / SUMRP$	PKP52-50 = "101"	
KVP47	$VREG1OUT - \Delta V * (VRP0 + 111R + VRHP + VRLP) / SUMRP$	PKP52-50 = "110"	
KVP48	$VREG1OUT - \Delta V * (VRP0 + 115R + VRHP + VRLP) / SUMRP$	PKP52-50 = "111"	
KVP49	$VREG1OUT - \Delta V * (VRP0 + 120R + VRHP + VRLP) / SUMRP$	-	VINP7

SUMRP : Sum of positive ladder resistors = 128R+VRHP+VRLP+VRP0+VRP1
 SUMRN : Sum of negative ladder resistors = 128R+VRHN+VRLN+VRN0+VRN1
 ΔV : Voltage difference between VREG1OUT and VGS.

Grayscale voltage calculating formulae (Positive polarity)

Table 58

Grayscale	Equation	Grayscale	Equation
V0	VINP0	V32	$V43 + (V20 - V43) \times (11/23)$
V1	VINP1	V33	$V43 + (V20 - V43) \times (10/23)$
V2	$V8 + (V1 - V8) \times (30/48)$	V34	$V43 + (V20 - V43) \times (9/23)$
V3	$V8 + (V1 - V8) \times (23/48)$	V35	$V43 + (V20 - V43) \times (8/23)$
V4	$V8 + (V1 - V8) \times (16/48)$	V36	$V43 + (V20 - V43) \times (7/23)$
V5	$V8 + (V1 - V8) \times (12/48)$	V37	$V43 + (V20 - V43) \times (6/23)$
V6	$V8 + (V1 - V8) \times (8/48)$	V38	$V43 + (V20 - V43) \times (5/23)$
V7	$V8 + (V1 - V8) \times (4/48)$	V39	$V43 + (V20 - V43) \times (4/23)$
V8	VINP2	V40	$V43 + (V20 - V43) \times (3/23)$
V9	$V20 + (V8 - V20) \times (22/24)$	V41	$V43 + (V20 - V43) \times (2/23)$
V10	$V20 + (V8 - V20) \times (20/24)$	V42	$V43 + (V20 - V43) \times (1/23)$
V11	$V20 + (V8 - V20) \times (18/24)$	V43	VINP4
V12	$V20 + (V8 - V20) \times (16/24)$	V44	$V55 + (V43 - V55) \times (22/24)$
V13	$V20 + (V8 - V20) \times (14/24)$	V45	$V55 + (V43 - V55) \times (20/24)$
V14	$V20 + (V8 - V20) \times (12/24)$	V46	$V55 + (V43 - V55) \times (18/24)$
V15	$V20 + (V8 - V20) \times (10/24)$	V47	$V55 + (V43 - V55) \times (16/24)$
V16	$V20 + (V8 - V20) \times (8/24)$	V48	$V55 + (V43 - V55) \times (14/24)$
V17	$V20 + (V8 - V20) \times (6/24)$	V49	$V55 + (V43 - V55) \times (12/24)$
V18	$V20 + (V8 - V20) \times (4/24)$	V50	$V55 + (V43 - V55) \times (10/24)$
V19	$V20 + (V8 - V20) \times (2/24)$	V51	$V55 + (V43 - V55) \times (8/24)$
V20	VINP3	V52	$V55 + (V43 - V55) \times (6/24)$
V21	$V43 + (V20 - V43) \times (22/23)$	V53	$V55 + (V43 - V55) \times (4/24)$
V22	$V43 + (V20 - V43) \times (21/23)$	V54	$V55 + (V43 - V55) \times (2/24)$
V23	$V43 + (V20 - V43) \times (20/23)$	V55	VINP5
V24	$V43 + (V20 - V43) \times (19/23)$	V56	$V62 + (V55 - V62) \times (44/48)$
V25	$V43 + (V20 - V43) \times (18/23)$	V57	$V62 + (V55 - V62) \times (40/48)$
V26	$V43 + (V20 - V43) \times (17/23)$	V58	$V62 + (V55 - V62) \times (36/48)$
V27	$V43 + (V20 - V43) \times (16/23)$	V59	$V62 + (V55 - V62) \times (32/48)$
V28	$V43 + (V20 - V43) \times (15/23)$	V60	$V62 + (V55 - V62) \times (25/48)$
V29	$V43 + (V20 - V43) \times (14/23)$	V61	$V62 + (V55 - V62) \times (18/48)$
V30	$V43 + (V20 - V43) \times (13/23)$	V62	VINP6
V31	$V43 + (V20 - V43) \times (12/23)$	V63	VINP7

Note: DDVDH - V0 > 0.5V
DDVDH - V8 > 1.1V

Grayscale voltage calculating formulae (Negative polarity)

Table 59

Pin	Equation	Fine adjustment register setting	Reference Voltage
KVP0	$VREG1OUT - \Delta V * VRN0 / SUMRN$	-	VINN0
KVN1	$VREG1OUT - \Delta V * (VRN0+5R) / SUMRN$	PKN 02-00 = "000"	VINN1
KVN2	$VREG1OUT - \Delta V * (VRN0+9R) / SUMRN$	PKN 02-00 = "001"	
KVN3	$VREG1OUT - \Delta V * (VRN0+13R) / SUMRN$	PKN 02-00 = "010"	
KVN4	$VREG1OUT - \Delta V * (VRN0+17R) / SUMRN$	PKN 02-00 = "011"	
KVN5	$VREG1OUT - \Delta V * (VRN0+21R) / SUMRN$	PKN 02-00 = "100"	
KVN6	$VREG1OUT - \Delta V * (VRN0+25R) / SUMRN$	PKN 02-00 = "101"	
KVN7	$VREG1OUT - \Delta V * (VRN0+29R) / SUMRN$	PKN 02-00 = "110"	
KVN8	$VREG1OUT - \Delta V * (VRN0+33R) / SUMRN$	PKN 02-00 = "111"	
KVN9	$VREG1OUT - \Delta V * (VRN0+33R+VRHN) / SUMRN$	PKN 12-10 = "000"	VINN2
KVN10	$VREG1OUT - \Delta V * (VRN0+34R+VRHN) / SUMRN$	PKN 12-10 = "001"	
KVN11	$VREG1OUT - \Delta V * (VRN0+35R+VRHN) / SUMRN$	PKN 12-10 = "010"	
KVN12	$VREG1OUT - \Delta V * (VRN0+36R+VRHN) / SUMRN$	PKN 12-10 = "011"	
KVN13	$VREG1OUT - \Delta V * (VRN0+37R+VRHN) / SUMRN$	PKN 12-10 = "100"	
KVN14	$VREG1OUT - \Delta V * (VRN0+38R+VRHN) / SUMRN$	PKN 12-10 = "101"	
KVN15	$VREG1OUT - \Delta V * (VRN0+39R+VRHN) / SUMRN$	PKN 12-10 = "110"	
KVN16	$VREG1OUT - \Delta V * (VRN0+40R+VRHN) / SUMRN$	PKN 12-10 = "111"	
KVN17	$VREG1OUT - \Delta V * (VRN0+45R+VRHN) / SUMRN$	PKN 22-20 = "000"	VINN3
KVN18	$VREG1OUT - \Delta V * (VRN0+46R+VRHN) / SUMRN$	PKN 22-20 = "001"	
KVN19	$VREG1OUT - \Delta V * (VRN0+47R+VRHN) / SUMRN$	PKN 22-20 = "010"	
KVN20	$VREG1OUT - \Delta V * (VRN0+48R+VRHN) / SUMRN$	PKN 22-20 = "011"	
KVN21	$VREG1OUT - \Delta V * (VRN0+49R+VRHN) / SUMRN$	PKN 22-20 = "100"	
KVN22	$VREG1OUT - \Delta V * (VRN0+50R+VRHN) / SUMRN$	PKN 22-20 = "101"	
KVN23	$VREG1OUT - \Delta V * (VRN0+51R+VRHN) / SUMRN$	PKN 22-20 = "110"	
KVN24	$VREG1OUT - \Delta V * (VRN0+52R+VRHN) / SUMRN$	PKN 22-20 = "111"	
KVN25	$VREG1OUT - \Delta V * (VRN0+68R+VRHN) / SUMRN$	PKN 32-30 = "000"	VINN4
KVN26	$VREG1OUT - \Delta V * (VRN0+69R+VRHN) / SUMRN$	PKN 32-30 = "001"	
KVN27	$VREG1OUT - \Delta V * (VRN0+70R+VRHN) / SUMRN$	PKN 32-30 = "010"	
KVN28	$VREG1OUT - \Delta V * (VRN0+71R+VRHN) / SUMRN$	PKN 32-30 = "011"	
KVN29	$VREG1OUT - \Delta V * (VRN0+72R+VRHN) / SUMRN$	PKN 32-30 = "100"	
KVN30	$VREG1OUT - \Delta V * (VRN0+73R+VRHN) / SUMRN$	PKN 32-30 = "101"	
KVN31	$VREG1OUT - \Delta V * (VRN0+74R+VRHN) / SUMRN$	PKN 32-30 = "110"	
KVN32	$VREG1OUT - \Delta V * (VRN0+75R+VRHN) / SUMRN$	PKN 32-30 = "111"	
KVN33	$VREG1OUT - \Delta V * (VRN0+80R+VRHN) / SUMRN$	PKN 42-40 = "000"	VINN5
KVN34	$VREG1OUT - \Delta V * (VRN0+81R+VRHN) / SUMRN$	PKN 42-40 = "001"	
KVN35	$VREG1OUT - \Delta V * (VRN0+82R+VRHN) / SUMRN$	PKN 42-40 = "010"	
KVN36	$VREG1OUT - \Delta V * (VRN0+83R+VRHN) / SUMRN$	PKN 42-40 = "011"	
KVN37	$VREG1OUT - \Delta V * (VRN0+84R+VRHN) / SUMRN$	PKN 42-40 = "100"	
KVN38	$VREG1OUT - \Delta V * (VRN0+85R+VRHN) / SUMRN$	PKN 42-40 = "101"	
KVN39	$VREG1OUT - \Delta V * (VRN0+86R+VRHN) / SUMRN$	PKN 42-40 = "110"	
KVN40	$VREG1OUT - \Delta V * (VRN0+87R+VRHN) / SUMRN$	PKN 42-40 = "111"	
KVN41	$VREG1OUT - \Delta V * (VRN0+87R+VRHN+VRLN) / SUMRN$	PKN 52-50 = "000"	VINN6
KVN42	$VREG1OUT - \Delta V * (VRN0+91R+VRHN+VRLN) / SUMRN$	PKN 52-50 = "001"	
KVN43	$VREG1OUT - \Delta V * (VRN0+95R+VRHN+VRLN) / SUMRN$	PKN 52-50 = "010"	
KVN44	$VREG1OUT - \Delta V * (VRN0+99R+VRHN+VRLN) / SUMRN$	PKN 52-50 = "011"	
KVN45	$VREG1OUT - \Delta V * (VRN0+103R+VRHN+VRLN) / SUMRN$	PKN 52-50 = "100"	
KVN46	$VREG1OUT - \Delta V * (VRN0+107R+VRHN+VRLN) / SUMRN$	PKN 52-50 = "101"	
KVN47	$VREG1OUT - \Delta V * (VRN0+111R+VRHN+VRLN) / SUMRN$	PKN 52-50 = "110"	
KVN48	$VREG1OUT - \Delta V * (VRN0+115R+VRHN+VRLN) / SUMRN$	PKN 52-50 = "111"	
KVN49	$VREG1OUT - \Delta V * (VRN0+120R+VRHN+VRLN) / SUMRN$	-	VINN7

SUMRP : Sum of positive ladder resistors = 128R+VRHP+VRLP+VRP0+VRP1

SUMRN : Sum of negative ladder resistors = 128R+VRHN+VRLN+VRN0+VRN1

 ΔV : Voltage difference between VREG1OUT and VGS

Grayscale voltage calculating formulae (Negative polarity)

Table 60

Grayscale	Equation	Grayscale	Equation
V0	VINN0	V32	$V43 + (V20 - V43) \times (11/23)$
V1	VINN1	V33	$V43 + (V20 - V43) \times (10/23)$
V2	$V8 + (V1 - V8) \times (30/48)$	V34	$V43 + (V20 - V43) \times (9/23)$
V3	$V8 + (V1 - V8) \times (23/48)$	V35	$V43 + (V20 - V43) \times (8/23)$
V4	$V8 + (V1 - V8) \times (16/48)$	V36	$V43 + (V20 - V43) \times (7/23)$
V5	$V8 + (V1 - V8) \times (12/48)$	V37	$V43 + (V20 - V43) \times (6/23)$
V6	$V8 + (V1 - V8) \times (8/48)$	V38	$V43 + (V20 - V43) \times (5/23)$
V7	$V8 + (V1 - V8) \times (4/48)$	V39	$V43 + (V20 - V43) \times (4/23)$
V8	VINN2	V40	$V43 + (V20 - V43) \times (3/23)$
V9	$V20 + (V8 - V20) \times (22/24)$	V41	$V43 + (V20 - V43) \times (2/23)$
V10	$V20 + (V8 - V20) \times (20/24)$	V42	$V43 + (V20 - V43) \times (1/23)$
V11	$V20 + (V8 - V20) \times (18/24)$	V43	VINN4
V12	$V20 + (V8 - V20) \times (16/24)$	V44	$V55 + (V43 - V55) \times (22/24)$
V13	$V20 + (V8 - V20) \times (14/24)$	V45	$V55 + (V43 - V55) \times (20/24)$
V14	$V20 + (V8 - V20) \times (12/24)$	V46	$V55 + (V43 - V55) \times (18/24)$
V15	$V20 + (V8 - V20) \times (10/24)$	V47	$V55 + (V43 - V55) \times (16/24)$
V16	$V20 + (V8 - V20) \times (8/24)$	V48	$V55 + (V43 - V55) \times (14/24)$
V17	$V20 + (V8 - V20) \times (6/24)$	V49	$V55 + (V43 - V55) \times (12/24)$
V18	$V20 + (V8 - V20) \times (4/24)$	V50	$V55 + (V43 - V55) \times (10/24)$
V19	$V20 + (V8 - V20) \times (2/24)$	V51	$V55 + (V43 - V55) \times (8/24)$
V20	VINN3	V52	$V55 + (V43 - V55) \times (6/24)$
V21	$V43 + (V20 - V43) \times (22/23)$	V53	$V55 + (V43 - V55) \times (4/24)$
V22	$V43 + (V20 - V43) \times (21/23)$	V54	$V55 + (V43 - V55) \times (2/24)$
V23	$V43 + (V20 - V43) \times (20/23)$	V55	VINN5
V24	$V43 + (V20 - V43) \times (19/23)$	V56	$V62 + (V55 - V62) \times (44/48)$
V25	$V43 + (V20 - V43) \times (18/23)$	V57	$V62 + (V55 - V62) \times (40/48)$
V26	$V43 + (V20 - V43) \times (17/23)$	V58	$V62 + (V55 - V62) \times (36/48)$
V27	$V43 + (V20 - V43) \times (16/23)$	V59	$V62 + (V55 - V62) \times (32/48)$
V28	$V43 + (V20 - V43) \times (15/23)$	V60	$V62 + (V55 - V62) \times (25/48)$
V29	$V43 + (V20 - V43) \times (14/23)$	V61	$V62 + (V55 - V62) \times (18/48)$
V30	$V43 + (V20 - V43) \times (13/23)$	V62	VINN6
V31	$V43 + (V20 - V43) \times (12/23)$	V63	VINN7

Note: DDVDH - V0 > 0.5V
DDVDH - V8 > 1.1V

Input/Output level relationship

The relationship between the data for each grayscale and its output level is as follows.

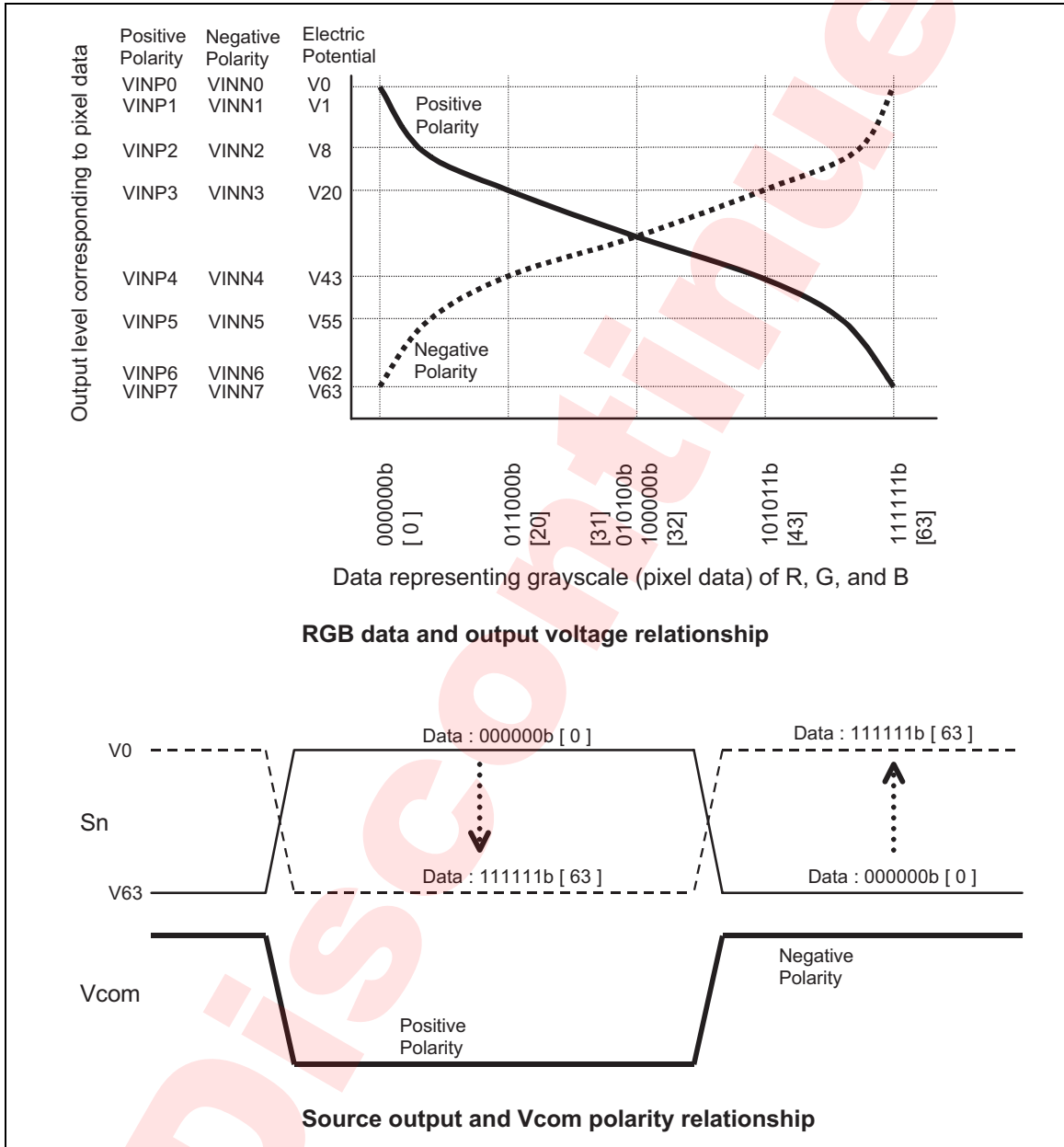


Figure 22

System configuration example

The following is an example of a module using a TFT LCD panel incorporating a gate driver with the HD66790R.

System example: 240(horizontal) x 320(vertical) pixels, using serial interface

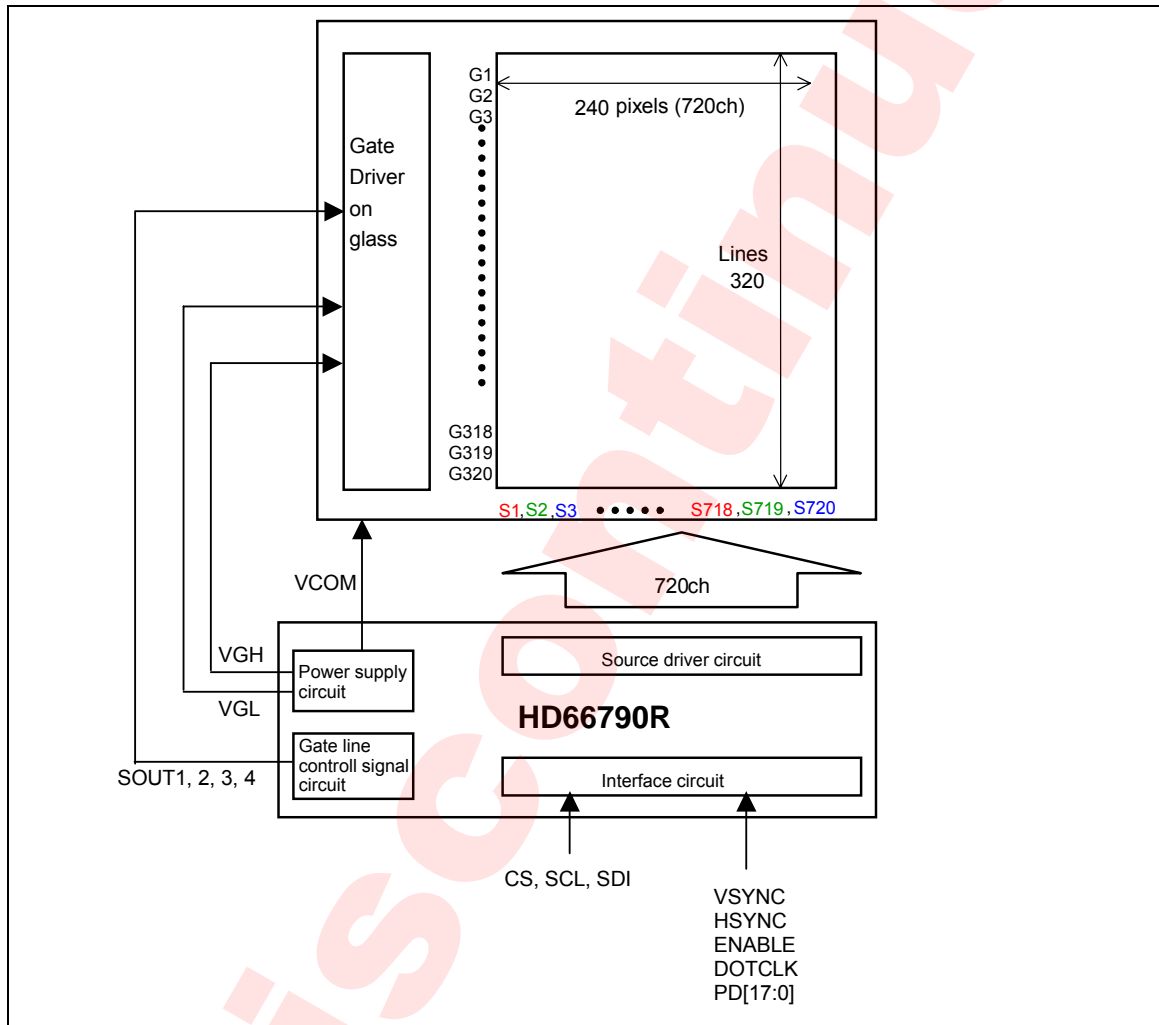


Figure 23

Voltage Setting Pattern Diagram

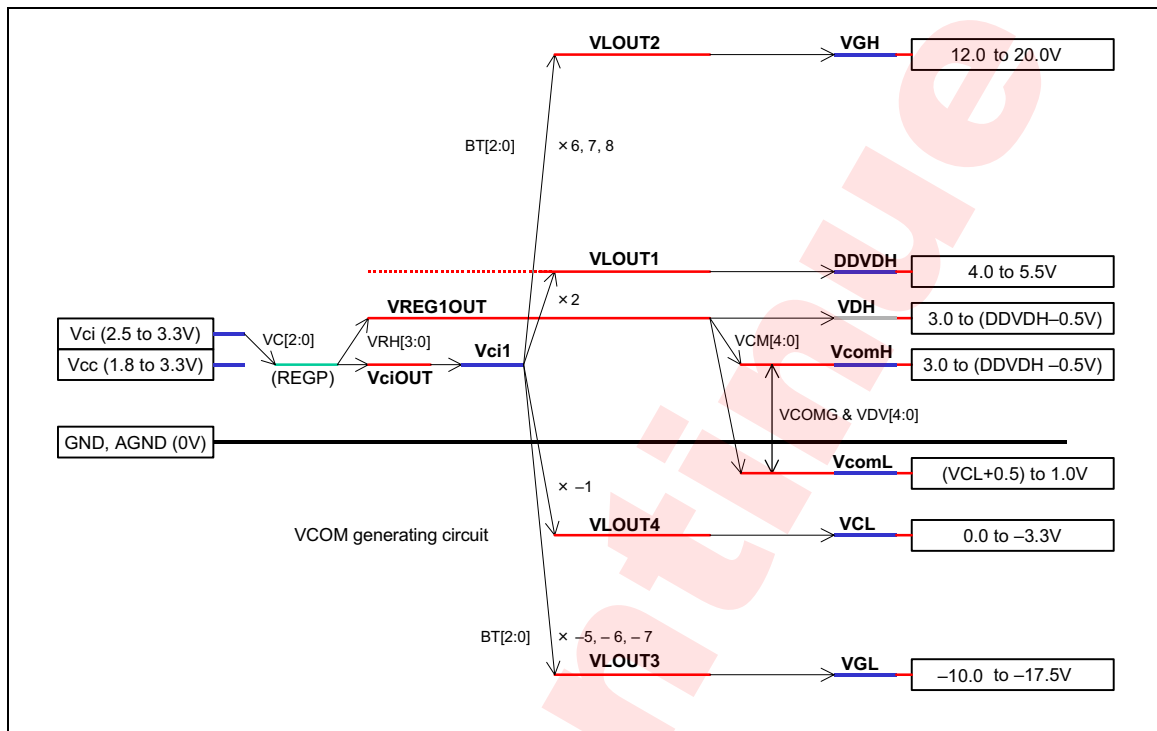


Figure 24

Note: When using the HD66790R, make sure $GND \leq VcomL \leq 1.0V$. If $VcomL < GND$, the HD66790R's equalize MOS structure will conduct a through current. When using the HD66790R with $VcomL < GND$ for display adjustment is inevitable, use the equalize function. Adjust the $VcomL$ level taking a trade-off between the quality of display and the current consumption. In case of using the HD66790R with $VcomL < GND$, a power supply for VCL is necessary.

Power Supply Setting

When supplying and cutting off the power, follow the sequences below. The stabilizing time for step-up circuits and operational amplifiers depends on the external resistance and capacitance.

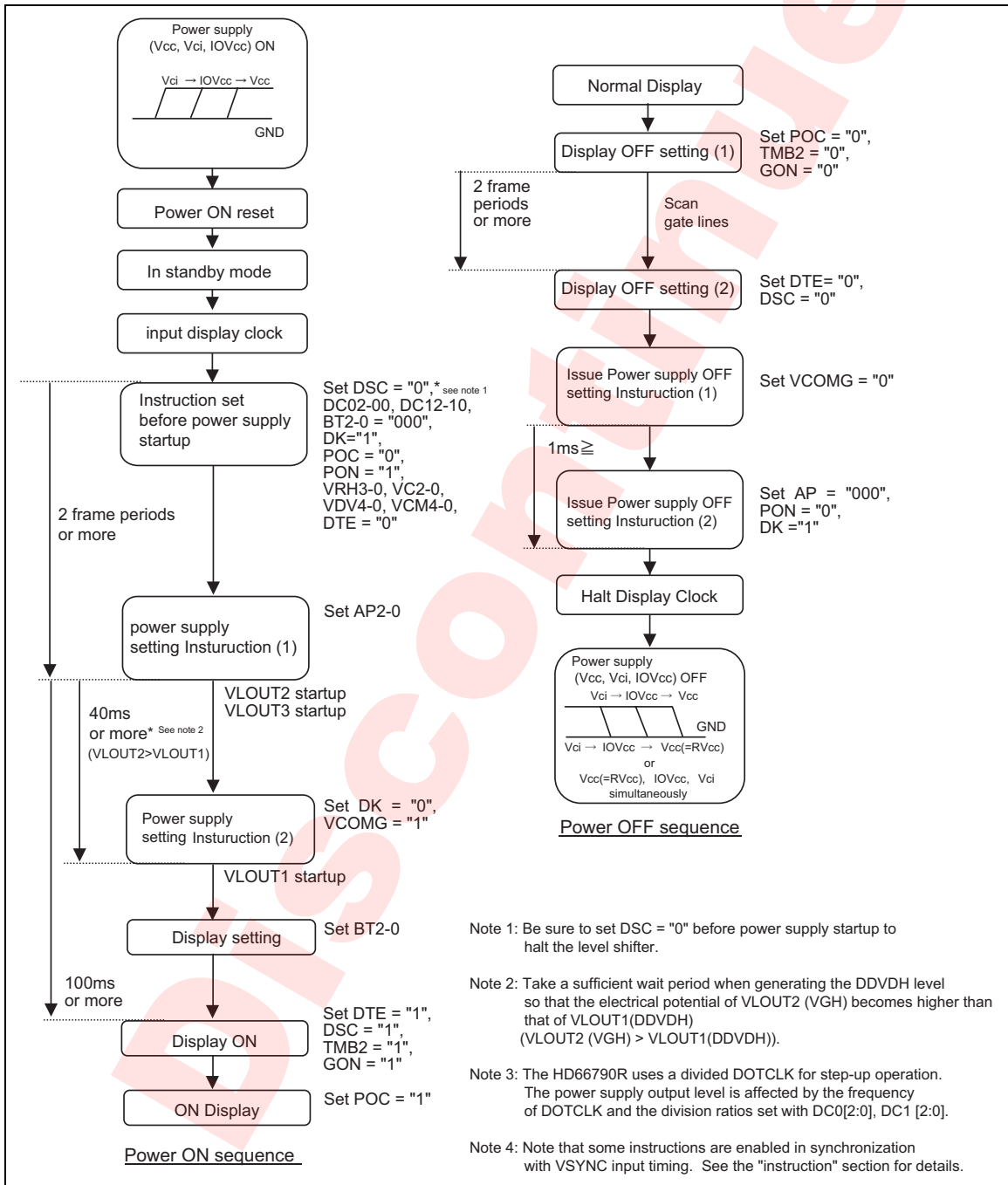


Figure 25

Sleep mode sequence

To enter the sleep mode, follow the sequence below.

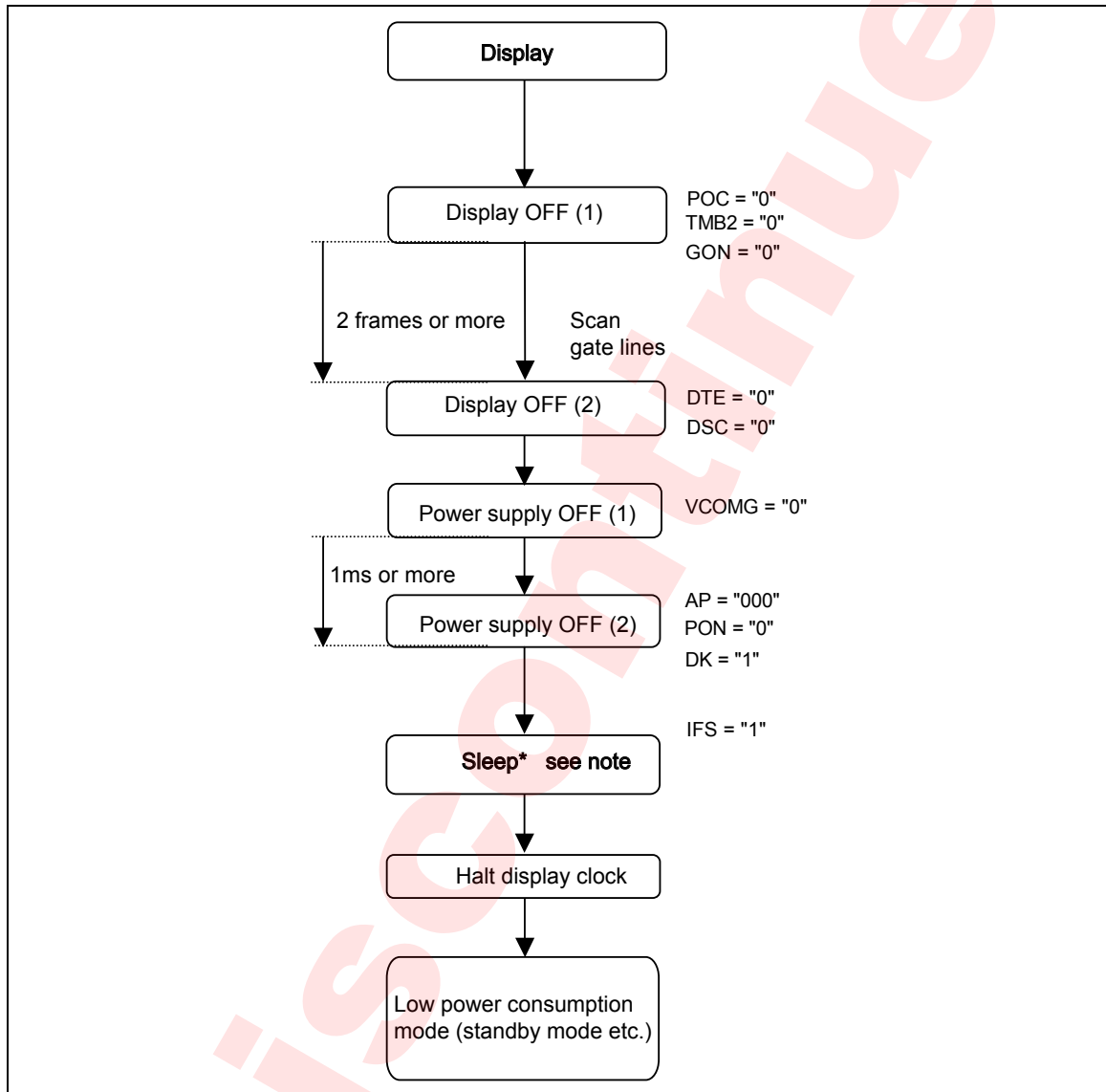


Figure 26

Note: In sleep mode, the current consumption becomes in proportion to the input display clock frequency. To make the current consumption in sleep mode equal to that in the standby mode, stop the display clock input.

Internal state transition of the HD66790R

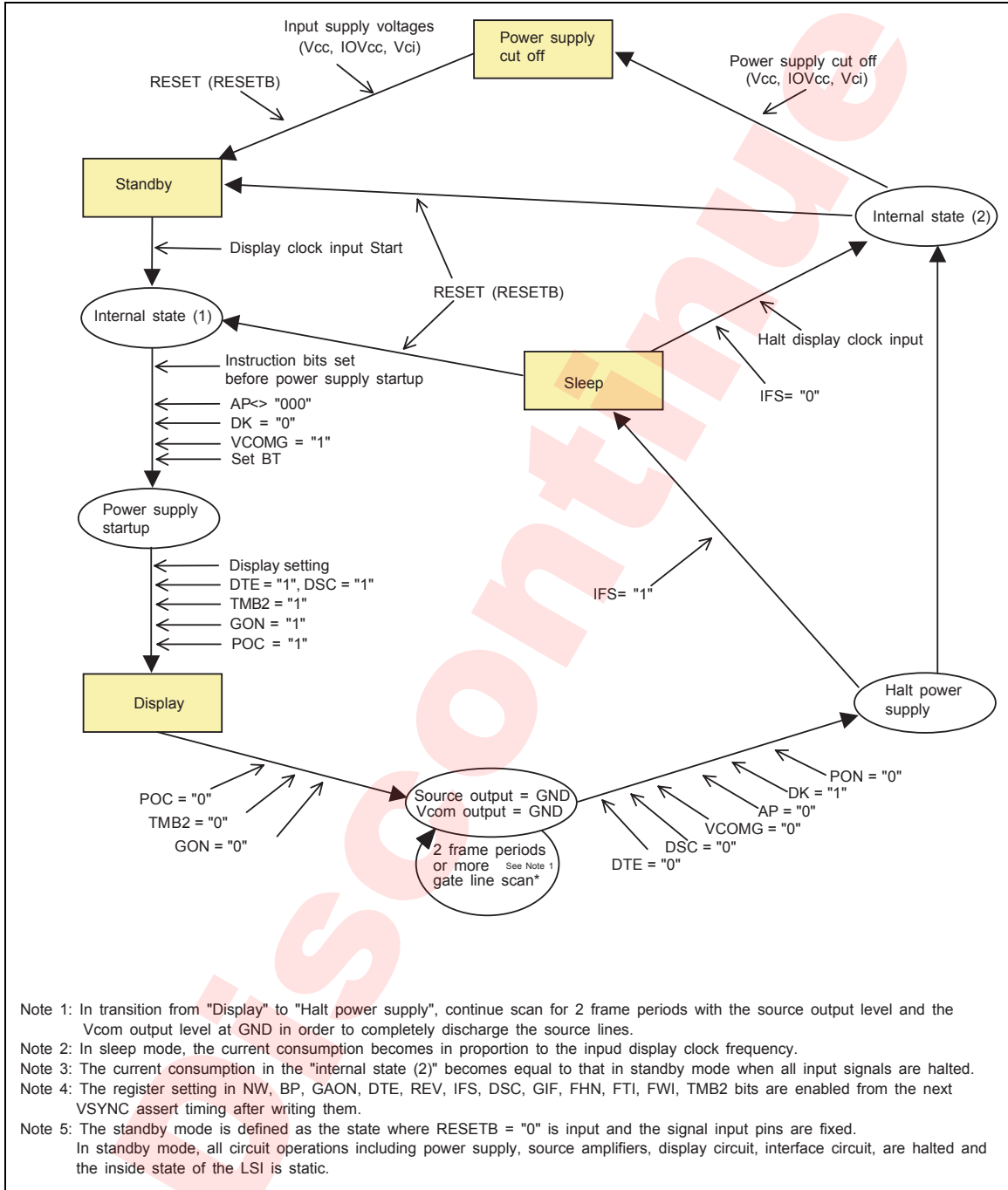


Figure 27

Absolute Maximum Ratings

Table 61

Item	Symbol	Unit	Rated value	Notes
Power supply voltage (1)	Vcc-GND	V	- 0.3 ~ + 4.3	(1), (2)
Power supply voltage (2)	IOVcc-GND	V	- 0.3 ~ + 4.3	(1), (3)
Power supply voltage (3)	Vci-AGND	V	- 0.3 ~ + 4.3	(1), (4)
Power supply voltage (4)	DDVDH-AGND	V	- 0.3 ~ + 6.0	(1), (5)
Power supply voltage (5)	AGND-VCL	V	- 0.3 ~ + 4.3	(1)
Power supply voltage (6)	DDVDH-VCL	V	- 0.3 ~ + 9.0	(1), (6)
Power supply voltage (7)	VGH-AGND	V	- 0.3 ~ + 22.0	(1), (7)
Power supply voltage (8)	AGND-VGL	V	- 0.3 ~ - 18.5	(1), (8)
Input/output voltage	V _t	V	- 0.3 ~ Vcc + 0.3	(1)
Operating temperature	Topr	°C	- 40 ~ + 85	(1), (9)
Storage temperature	Tstg	°C	- 55 ~ + 110	(1)

Notes: 1. If used beyond the absolute maximum ratings, the LSI may permanently be damaged.
It is strongly recommended to use the LSI at a condition within the electrical characteristics in normal operation. Exposure to a condition not within the electrical characteristics may affect device reliability.

2. Make sure Vcc (High) ≥ GND (Low).
3. Make sure IOVcc (High) ≥ GND (Low).
4. Make sure Vci (High) ≥ AGND (Low).
5. Make sure DDVDH (High) ≥ AGND (Low).
6. Make sure DDVDH (High) ≥ VCL (Low).
7. Make sure VGH (High) ≥ AGND (Low).
8. Make sure AGND (High) ≥ VGL (Low).
9. The DC/AC characteristics of die and wafer products is guaranteed at 85 °C.

Capacitance

Ta = - 25°C, Vcc = 3.3V ± 0.3V

Table 62

Parameter	Symbol	Typ.	Max.	Unit	Notes
Input capacitance	C ₁₁	-	20	pF	1
Input capacitance	C ₁₂	-	20	pF	1

Note: Measurement using a Booton Meter or other equivalent methods and when CAS = V_{IH} for not selecting Dout.

DC Operating Condition

Table 63

Parameter	Symbol	Min	Typ	Max	Unit	Note
Logic supply voltage	V _{CC}	2.5	3.0	3.6	V	1, 2
Analog supply voltage	V _{CI}	2.5	3.0	3.6	V	1
Interface supply voltage	IOV _{CC}	1.65	3.0	3.6	V	1
Source driver supply voltage	V _{DDVDH}	4.0	-	5.5	V	1, 2
Supply voltage for level shifter output "high" level	V _{GH}	8.0	-	20.0	V	1, 2
Supply voltage for level shifter output "low" level	V _{GL}	-17.5	-	-4.0	V	1
Supply voltage for V _{com} amplitude	V _{COMR}	0.0	-	V _{DDVDH} -0.3	V	1, 2

Notes: 1. All above voltages are measured with either GND or AGND level as the reference level.

2. Make sure $V_{GH} > V_{DDVDH} > V_{CC}$.

Electrical characteristics

DC characteristics

Ta = -40°C ~ +85°C, IOVcc = 1.65V ~ 3.6 V, Vcc = Vci = 2.5 ~ 3.6V* see Note 1

Table 64

Items	Symbol	Min.	typ.	Max.	Unit	Test Condition	Notes
Input "High" level voltage	V _{IH}	0.7 IOVcc		IOVcc	V		2, 3
Input "Low" level voltage	V _{IL}	0		0.3 IOVcc	V		2, 3
Output "High" level voltage	V _{OH}	0.7 IOVcc			V	I _{OH} = -0.1mA	2
Output "Low" level voltage	V _{OL}			0.15 IOVcc	V	I _{OL} = 0.1mA	2
Input/output leak current	I _{LO}	-5		5	μA	V _{IN} = 0 ~ IOVcc	4
Current Consumption (Normal operation mode)	Vcc-GND	I _{Vcc}	0.45	0.6	mA	Vcc=Vci=IOVcc= 2.8V, BT; x7, x-5, DC0: 1/256, DC1: 1/1024 fDOTCLK = 5MHz, 18-bit interface, Ta = 25°C, AP = "001", LSENL="0", LSENR="1"	5, 6
	Vci-GND	I _{Vci}	4.7	6	mA		
Current Consumption (Standby mode)	Vcc-GND +Vci-GND	I _{stb}	2	10	μA	Vcc=Vci=IOVcc= 2.8V, Ta = 25°C	5
Current Consumption (Sleep mode)	Vcc-GND +IOVcc-GND	I _{slp}	20			Vcc=Vci=IOVcc= 2.8V, fDOTCLK = 1.5MHz Ta = 25°C	5
Output voltage difference	ΔV _O		±15	±25	mV		7
Average output voltage variance	ΔV _Δ		±15		mV		8
Level Shifter ON resistance	R _{ON}			250	Ohm	VGH-VGL I _{load} =±500μA	9

- Notes
1. Refer to the corresponding numbers in "Note to electrical characteristics" for notes.
 2. The standby mode is defined as the state where the signal input pins are fixed after input of RESETB = "0". In standby mode, the internal state of the HD66790R is static, where all circuit operation, including power supply, source amplifiers, display, interface circuits, are halted.

Step-up circuit output characteristics

Ta = -40°C ~ +85°C, IOVcc = 1.65V ~ 3.6V, Vcc=Vci= 2.5V ~ 3.6 V* see Note 1

Table 65

Items	Symbol	Min.	typ.	Max.	Unit	Test Condition	Notes
Step-up output voltage1	VLOUT1	4.85	4.9		V	IOVcc=Vcc=Vci=3.0V, fDOTCLK=5MHz, Ta=25°C, Vci=VciOUT (directly input Vci externally), DC0="010", DC1="011", BT="101", AP="001", TMB="11", C11=C12=C21=C22=1uF/B, VLOUT1=VLOUT2=VLOUT3=VLOUT4=1uF/B, No load, Iload = -5mA	11
Step-up output voltage2	VLOUT2	15.5	16.2		V	IOVcc=Vcc=Vci=3.0V, fDOTCLK=5MHz, Ta=25°C, Vci=VciOUT(directly input Vci externally), DC0="010", DC1="011", BT="101", AP="001", TMB="11", C11=C12=C21=C22=1uF/B, VLOUT1=VLOUT2=VLOUT3=VLOUT4=1uF/B, No load, Iload = -500 μA	11
Step-up output voltage3	VLOUT3	-11.2	-11.9		V	IOVcc=Vcc=Vci=3.0V, fDOTCLK=5MHz, Ta=25°C, Vci=VciOUT(directly input Vci externally), DC0="010", DC1="011", BT="101", AP="001", TMB="11", C11=C12=C21=C22=1uF/B, VLOUT1=VLOUT2=VLOUT3=VLOUT4=1uF/B, No load, Iload = +500 μA	11
Step-up output voltage4	VLOUT4	-2.4	-2.6		V	IOVcc=Vcc=Vci=3.0V, fDOTCLK=5MHz, Ta=25°C, Vci=VciOUT(directly input Vci externally), DC0="010", DC1="011", BT="101", AP="001", TMB="11", C11=C12=C21=C22=1uF/B, VLOUT1=VLOUT2=VLOUT3=VLOUT4=1uF/B, No load, Iload = +500μA	11
Input voltage	Vci	2.5		3.6	V		11

Note: Refer to the corresponding numbers in "Note to electrical characteristics" for notes.

AC characteristics

Serial Peripheral Interface Timing Characteristics

Ta = -40°C ~ +85°C, IOVcc = 1.65V ~ 3.6 V, Vcc = 2.5V ~ 3.6V* see Note 1

Table 66

Item	Symbol	Min	Typ	Max	Unit	Timing diagram
Serial clock cycle time	t _{SCYC}	0.2	—	40	μs	Figure 28
Serial clock "High" level pulse width	t _{SCH}	80	—	—	nS	Figure 28
Serial clock "Low" level pulse width	t _{SCL}	80	—	—	nS	Figure 28
Serial clock rising time	t _{scr}	—	—	40	nS	Figure 28
Serial clock falling time	t _{scf}	—	—	40	nS	Figure 28
Chip select setup time	t _{CSU}	40	—	—	nS	Figure 28
Chip select hold time	t _{CSH}	120	—	—	nS	Figure 28
Serial input data setup time	t _{SISU}	60	—	—	nS	Figure 28
Serial input data hold time	t _{SIH}	60	—	—	nS	Figure 28

- Notes 1. Refer to the corresponding number in "Note to electrical characteristics" for notes.
2. Refer to the corresponding Figure in "Note to electrical characteristics" for timing diagram.

Reset Timing Characteristics

Ta = -40°C ~ +85°C, IOVcc = 1.65V ~ 3.6 V, Vcc = 2.5V ~ 3.6V* see Note 1

Table 67

Item	Symbol	Min	Typ	Max	Unit	Timing diagram
Reset "Low" level width	t _{RES}	1	—	—	ms	Figure 29
Reset startup time	t _{rRES}	—	—	10	μs	Figure 29
Reset exit delay time	t _{DRES}	—	—	500	μs	Figure 29

- Notes 1. Refer to the corresponding number in "Note to electrical characteristics" for notes.
2. Refer to the corresponding Figure in "Note to electrical characteristics" for timing diagram.

18-bit RGB interface timing characteristics

Ta = -40°C ~ +85°C, IOVcc = 1.65V ~ 3.6 V, Vcc = 2.5V ~ 3.6V* see Note 1

Table 68

Item	Symbol	min.	typ.	max.	Unit	Timing diagram
VSYNC/HSYNC Setup time	t _{SYNCS}	20	—	—	nS	Figure 30
ENABLE Setup time	t _{ENS}	30	—	—	nS	Figure 30
ENABLE Hold time	t _{ENH}	30	—	—	nS	Figure 30
DOTCLK "Low" level pulse width	P _{WDL}	40	—	—	nS	Figure 30
DOTCLK "High" level pulse width	P _{WDH}	40	—	—	nS	Figure 30
DOTCLK cycle time	t _{CYCD}	100	—	—	nS	Figure 30
Data Setup time	t _{PDS}	30	—	—	nS	Figure 30
Data Hold time	t _{PDH}	30	—	—	nS	Figure 30
DOTCLK, VSYNC, HSYNC rise/fall time	t _{rgbr} , t _{rgbf}	—	—	25	nS	Figure 30

- Notes 1. Refer to the corresponding number in "Note to electrical characteristics" for notes.
 2. Refer to the corresponding Figure in "Note to electrical characteristics" for timing diagram.

16-bit RGB interface timing characteristics

Ta = -40°C ~ +85°C, IOVcc = 1.65V ~ less than 2.5V, Vcc = 2.5V ~ 3.6V* see Note 1

Table 69

Item	Symbol	min.	typ.	max.	Unit	Timing diagram
VSYNC/HSYNC Setup time	t _{SYNCS}	15	—	—	nS	Figure 30
ENABLE Setup time	t _{ENS}	18	—	—	nS	Figure 30
ENABLE Hold time	t _{ENH}	20	—	—	nS	Figure 30
DOTCLK "Low" level pulse width	P _{WDL}	24	—	—	nS	Figure 30
DOTCLK "High" level pulse width	P _{WDH}	24	—	—	nS	Figure 30
DOTCLK cycle time	t _{CYCD}	60	—	—	nS	Figure 30
Data Setup time	t _{PDS}	15	—	—	nS	Figure 30
Data Hold time	t _{PDH}	20	—	—	nS	Figure 30
DOTCLK, VSYNC, HSYNC rise/fall time	t _{rgbr} , t _{rgbf}	—	—	10	nS	Figure 30

- Notes 1. Refer to the corresponding number in "Note to electrical characteristics" for notes.
 2. Refer to the corresponding Figure in "Note to electrical characteristics" for timing diagram.

6-bit RGB interface timing characteristics

Ta = -40°C ~ +85°C, IOVcc = 2.5V ~ 3.6V, Vcc = 2.5V ~ 3.6V* see Note 1

Table 70

Item	Symbol	min.	typ.	max.	Unit	Timing diagram
VSYNC/HSYNC Setup time	t _{SYNCS}	15	—	—	nS	Figure 30
ENABLE Setup time	t _{ENS}	18	—	—	nS	Figure 30
ENABLE Hold time	t _{ENH}	20	—	—	nS	Figure 30
DOTCLK "Low" level pulse width	P _{WDL}	16	—	—	nS	Figure 30
DOTCLK "High" level pulse width	P _{WDH}	16	—	—	nS	Figure 30
DOTCLK cycle time	t _{CYCD}	40	—	—	nS	Figure 30
Data Setup time	t _{PDS}	15	—	—	nS	Figure 30
Data Hold time	t _{PDH}	20	—	—	nS	Figure 30
DOTCLK, VSYNC, HSYNC rise/fall time	t _{rgbr} , t _{rgbf}	—	—	10	nS	Figure 30

- Notes 1. Refer to the corresponding number in "Note to electrical characteristics" for notes.
 2. Refer to the corresponding Figure in "Note to electrical characteristics" for timing diagram.

LCD driver output characteristics

Table 71

Item	Symbol	min.	typ.	max.	Unit	Test Condition	Timing diagram	Note
Driver output delay time	t _{DD}	—	20	35	μS	Vcc = 3.0V, V _{DDVDH} = 5.0V, VGH = 8.0V, VGL = 0V, Ta = 25°C, DOTCLK = 8MHz, Time to reach the target voltage level ±25mV from Vcom polarity inversion timing When changing from a same grayscale level at all source pins Load resistance R = 10kΩ, Load capacity 50pF	Figure 31	10

- Notes 1. Refer to the corresponding number in "Note to electrical characteristics" for notes.
 2. Refer to the corresponding Figure in "Note to electrical characteristics" for timing diagram.

Timing diagram

Serial Peripheral Interface Operation

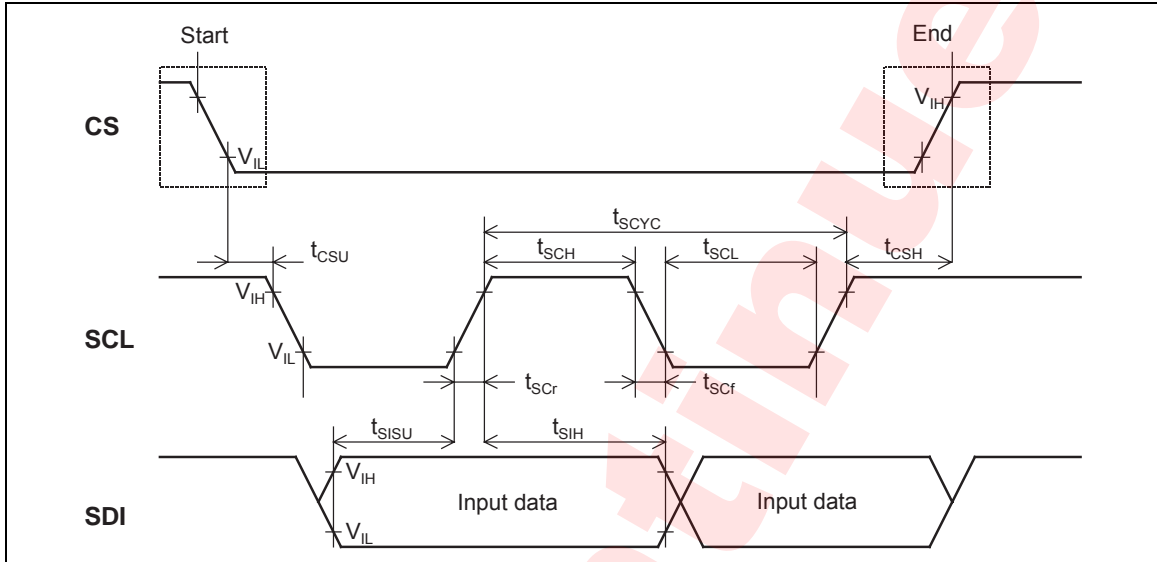


Figure 28

Reset Operation

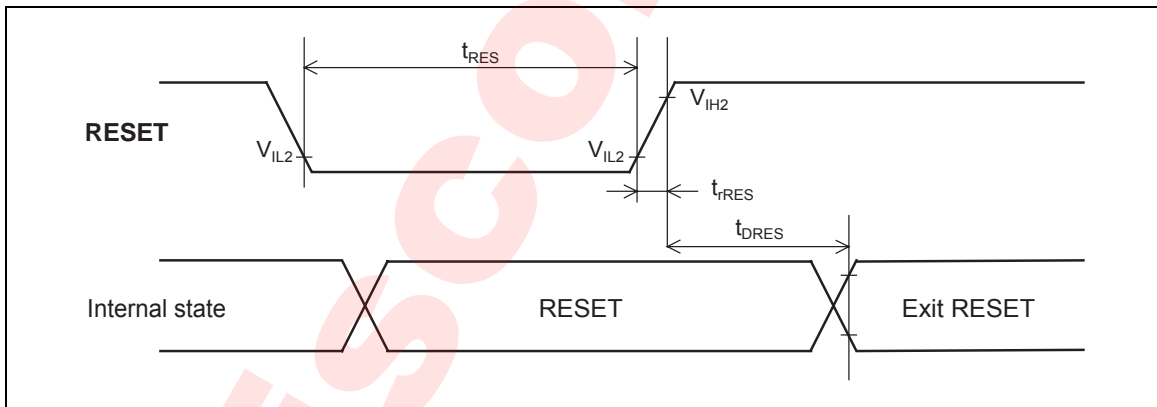


Figure 29

Interfacing Operation

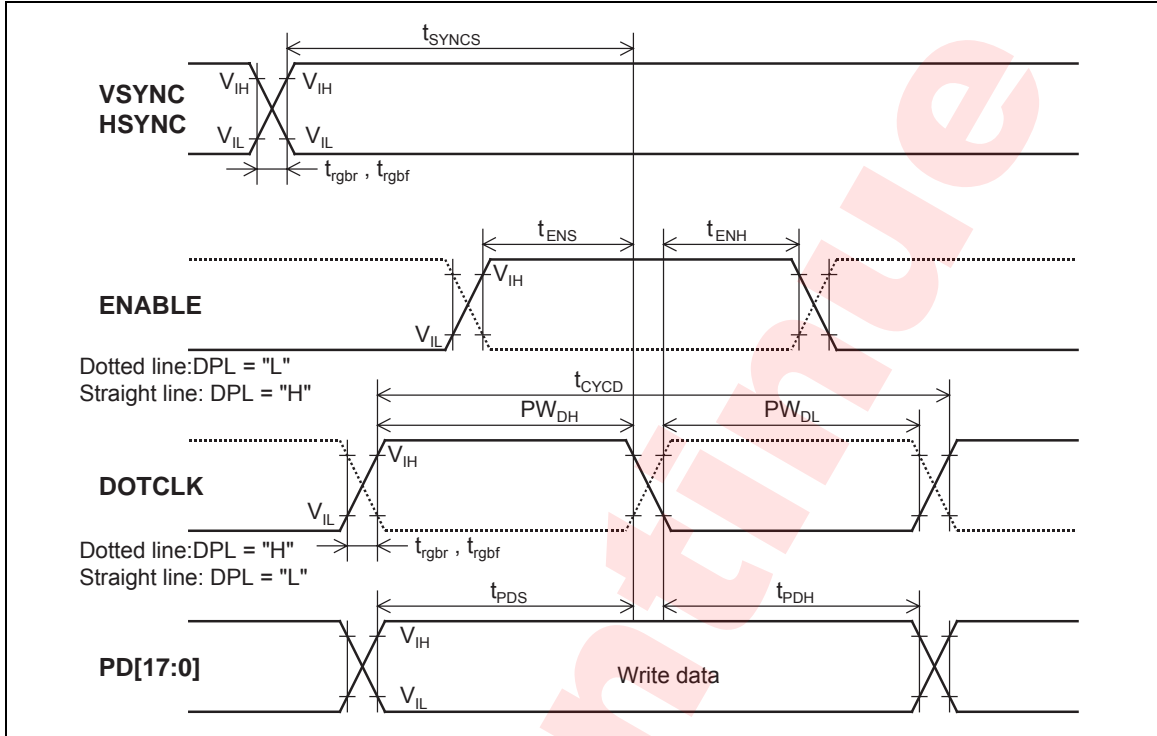


Figure 30

Switching Operation

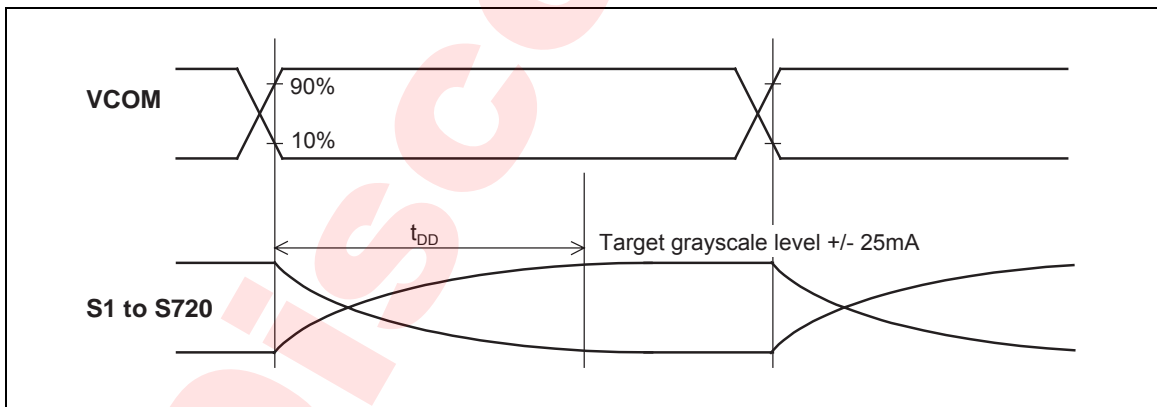


Figure 31

Notes to Electrical Characteristics

1. The DC/AC electrical characteristics of bare die and wafer products are guaranteed at 85°C.
2. The following are the structures of input, input/output, and output pins.

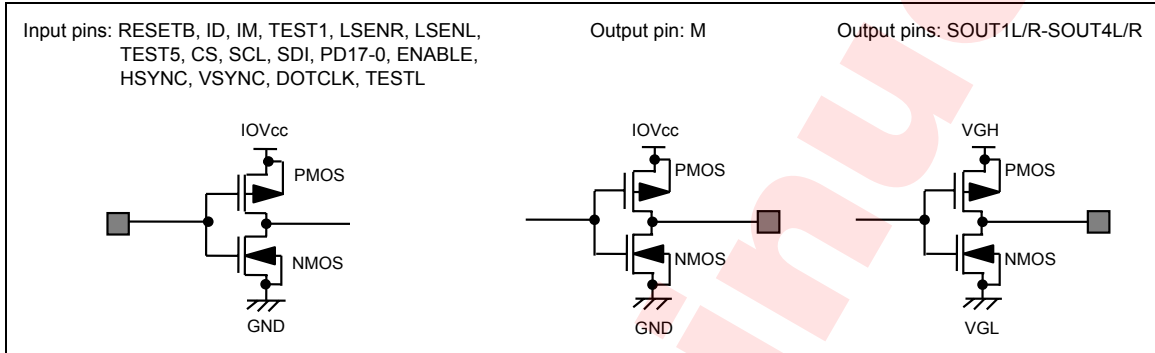


Figure 32

3. The TEST1, TEST5 and TESTL pins must be grounded (GND). The LSENR, LSENL, ID, IM pins must be fixed at either GND or the Vcc level.
4. This excludes currents through the output drive MOS.
5. This excludes currents through input and output units. Make sure that input levels are fixed to prevent through current in input units when the CMOS input level takes medium range. While not accessing the HD66790R via interface pins, current consumption will not change whether the CS* pin is set to “High” or “Low”.
6. The relationships between the voltages and current consumption are as follows (reference data).

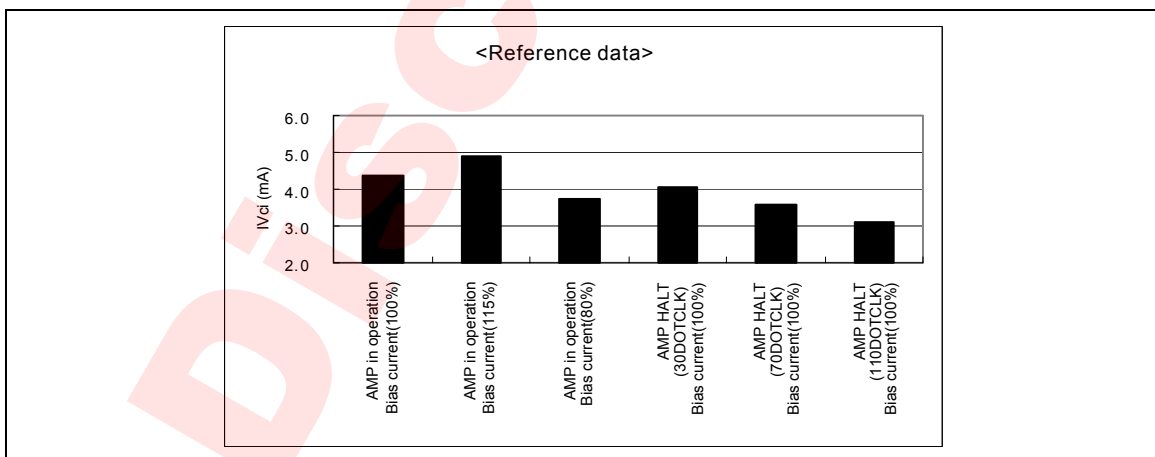


Figure 33

7. The output voltage difference is the difference in voltage levels from adjacent source pins for a same grayscale. In offset cancel operation, this difference becomes within +/-10mV.
8. The average output voltage variance is the difference in average source output voltages within the same product. The average source output voltage is measured for each chip of the same product when the same data are written for the entire display. This value is just for reference.
9. In this test, the input level having amplitude between $V_{GH} = 16.5V$ and $V_{GL} = -16.5$ is applied externally. The voltage drop on each SOUT pin from externally input levels minus load current $500 \mu A$ is defined as ΔV , and $\Delta V/500(\mu A)$ is defined as the ON resistance of the most outside buffer in the level shifter. The following are reference data under the TYP. condition.

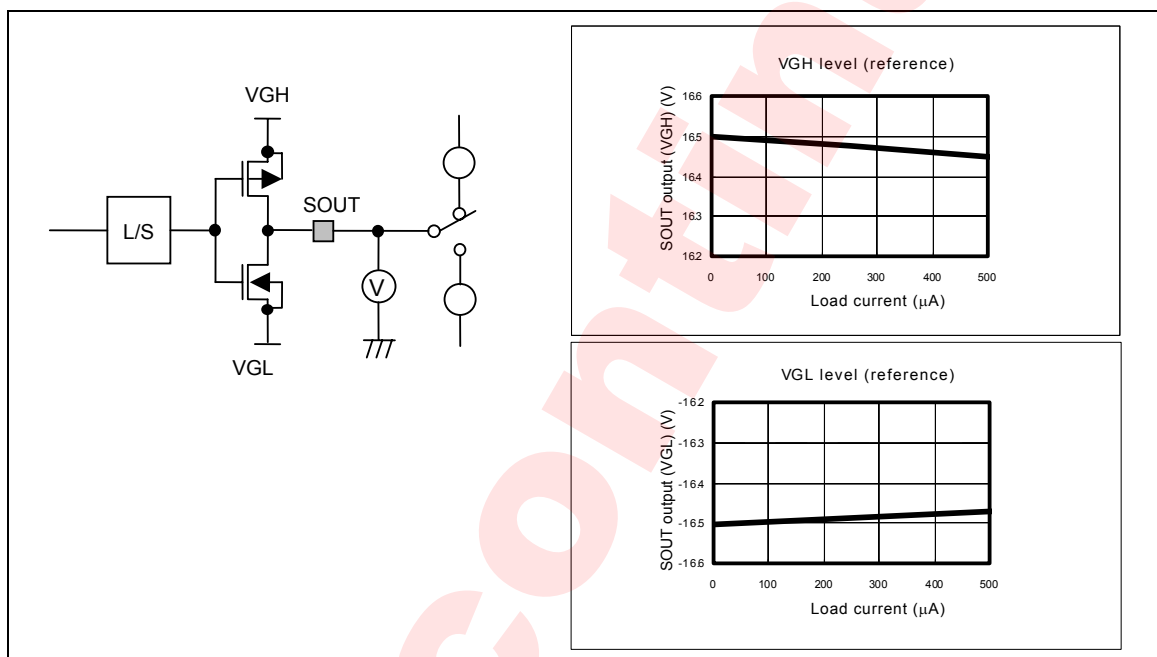


Figure 34

10. The LCD driver output delay time depends on the load capacitance of the LCD panel. Check the quality of display on the panel when setting a frame frequency and a cycle per line.

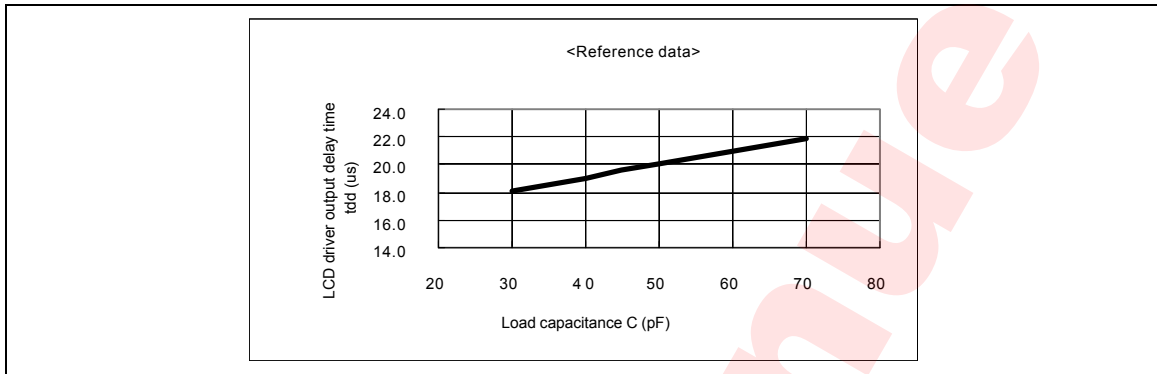


Figure 35

11. This does not include the wiring resistance when an LSI chip is mounted on glass, i.e. COG. No load element is added to pins except those being tested.

Example of test circuits

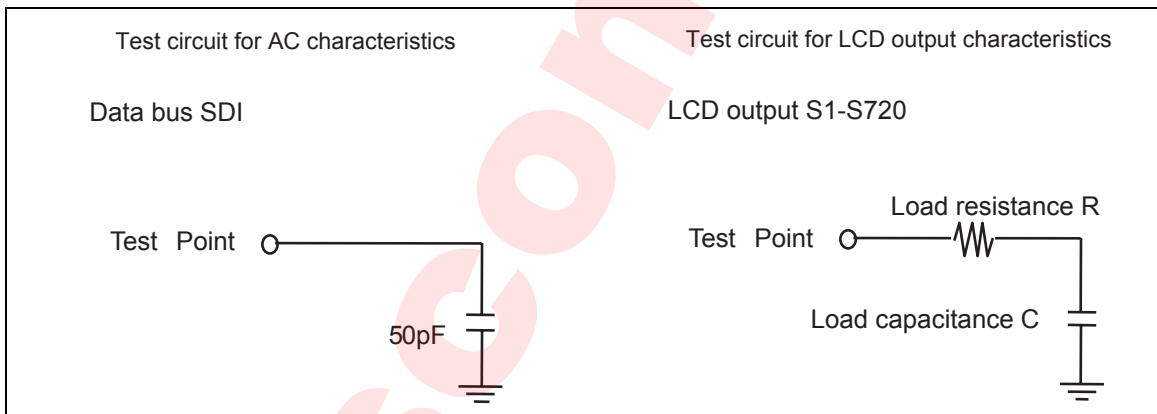
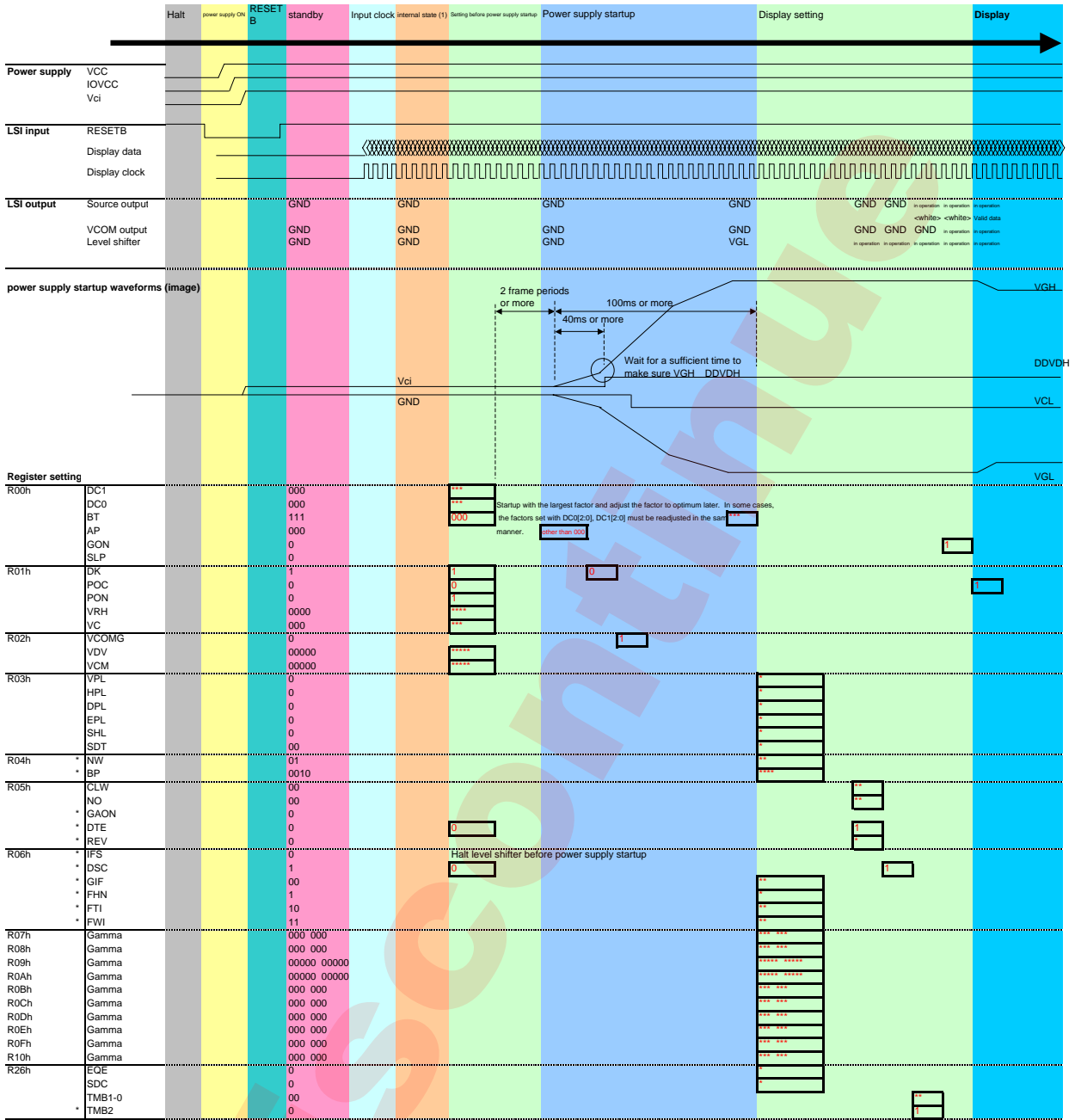


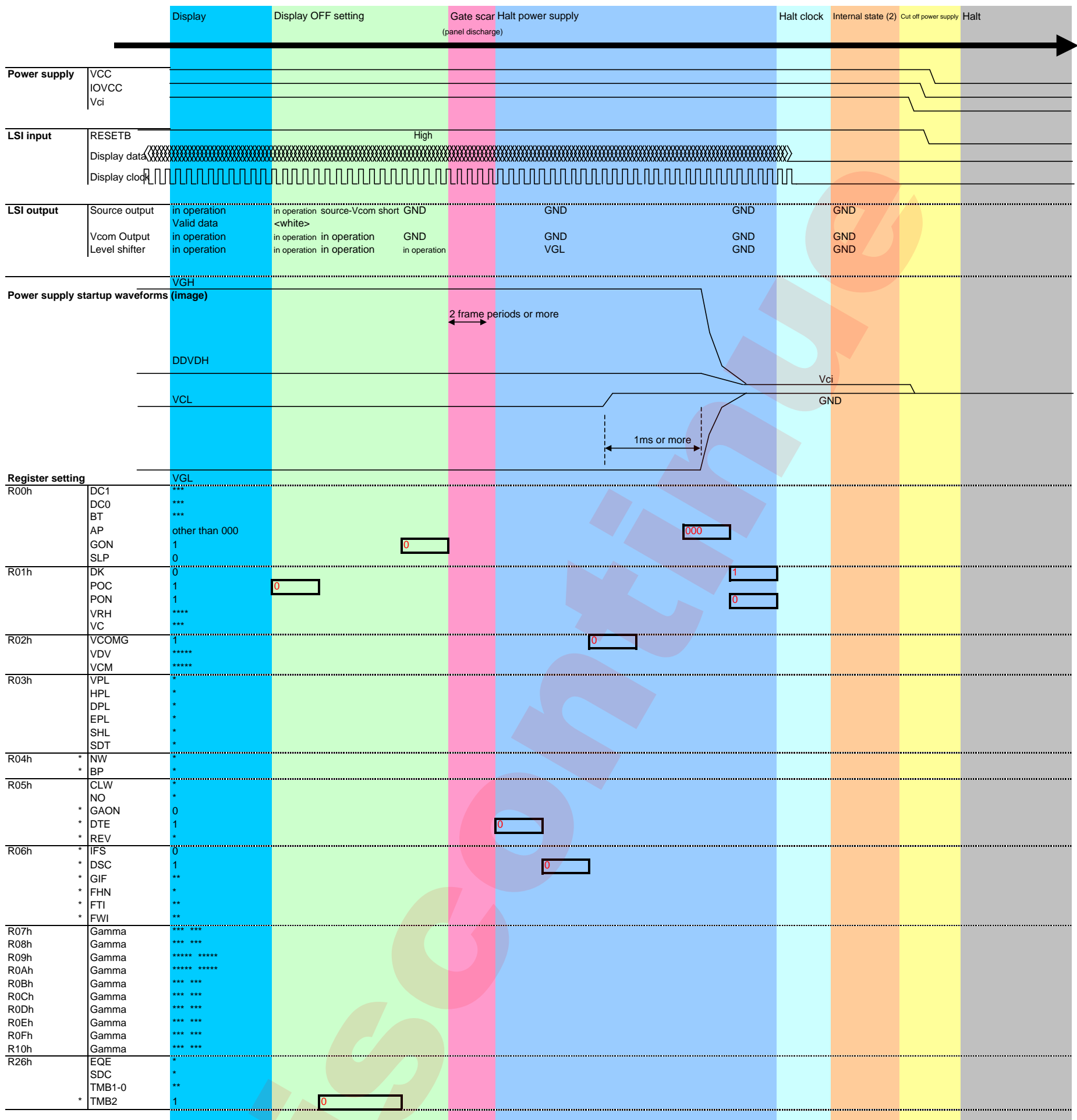
Figure 36

Power supply startup, Display ON sequence (reference)



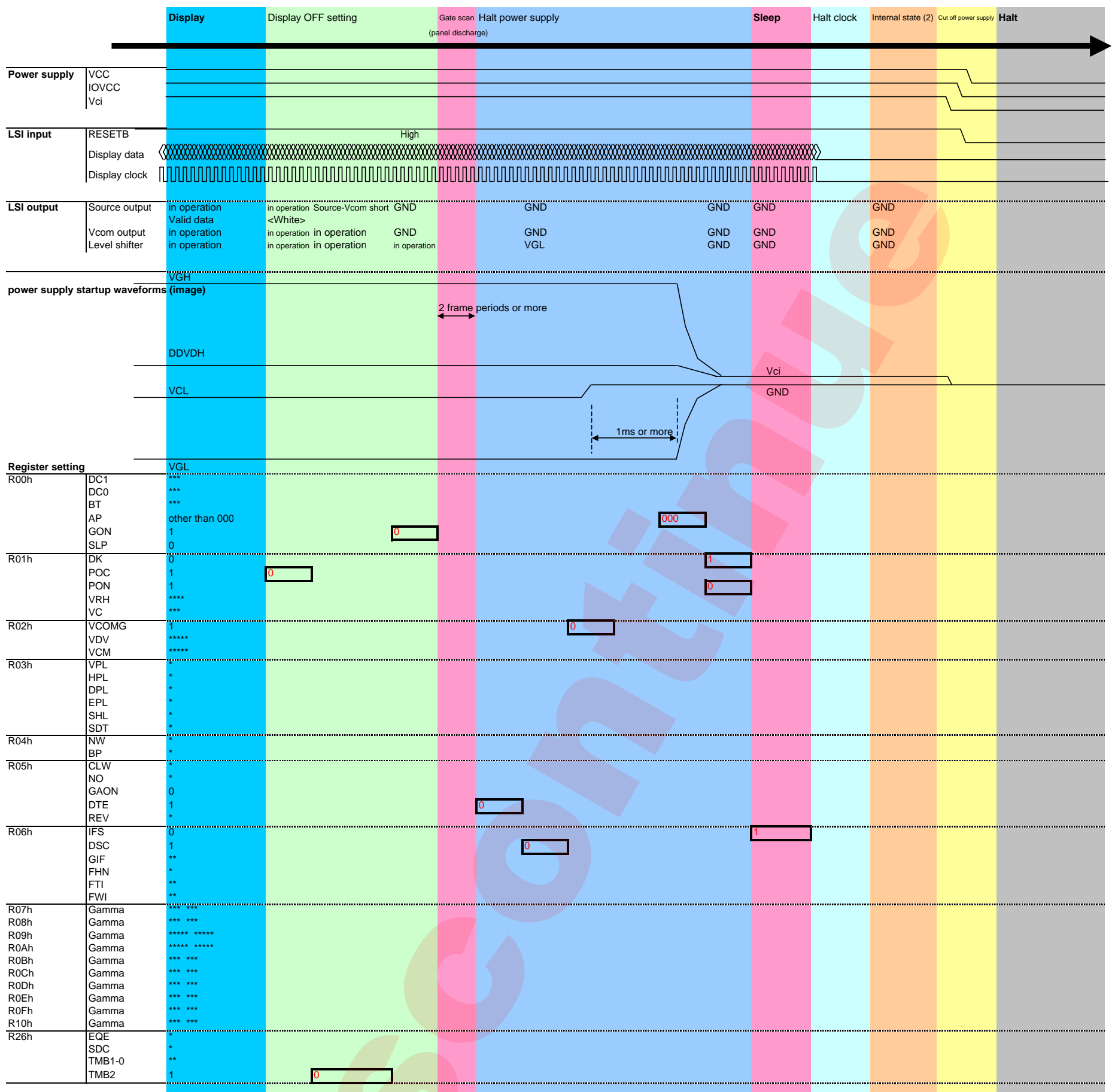
Notes: 1. Instruction bits with * are set arbitrarily by user.
 2. Instruction bits with * are enabled inside the LSI in synchronizaion with VSYNC. Secure at least 2 frame periods after writing these bi

Display OFF, Power supply OFF sequence (reference)



Notes: 1. Instruction bits with * are set arbitrarily by users
 2. Instruction bits with * are enabled inside the LSI in synchronizaion with VSYNC. Secure at least 2 frame periods after writing these bits

Sleep sequence (reference)

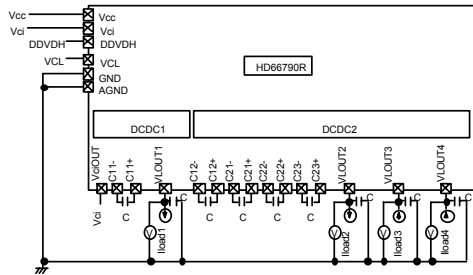


Notes: 1. Instruction bits with * are set arbitrarily by users
 2. Instruction bits with * are enabled inside the LSI in synchronization with VSYNC. Secure at least 2 frame periods after writing these bit.
 3. Clock and data input via RGB interface circuit may get some of the circuits started even when IFS=1

Reference data

1. VLOUT1

(1) Test circuit



(2) Test Condition

25 TYP sample		external capacitance	
Vcc	Applied voltage	C	1[μF]/B
Vci	2.8V		
VciOUT	Connect to Vci		Clock cycle
DDVDH	5.6V	fDOTCLK	5MHz

(3) Test description

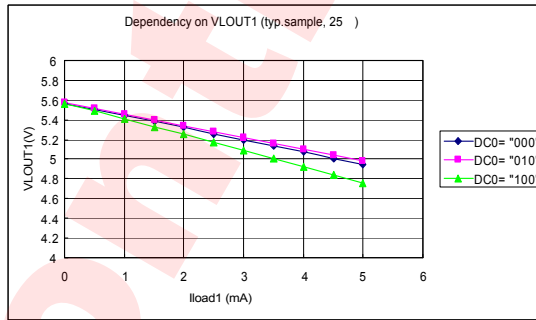
Measure the dependency of VLOUT1 on the load current (Iload1) using the step-up clock cycle of VLOUT1 as a parameter. (No load is applied to pins other than those being tested.)

(4) Test Results

(a) VLOUT1 load current characteristics 1
parameter: step-up cycle

Setting in the register

- VC2-0 = "000"
- AP2-0 = "001"
- BT2-0 = "101"
- DC02-0 = "000" (1/32)
- DC02-0 = "010" (1/128)
- DC02-0 = "100" (1/512)
- DC12-0 = "011" (1/512)

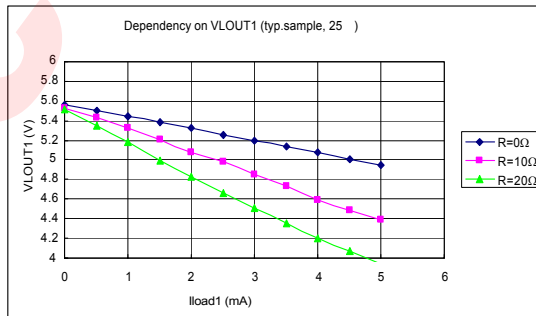
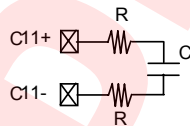


(b) VLOUT1 load current characteristics 1
parameter: Resistance with step-up capacitance (see below)

Setting in the register

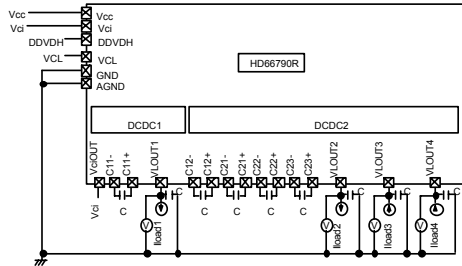
- VC2-0 = "000"
- AP2-0 = "001"
- BT2-0 = "101"
- DC02-0 = "000" (1/32)
- DC12-0 = "011" (1/512)

Circuit



2. VLOUT2

(1) Test circuit



(2) Test Condition

25 TYP sample

Applied voltage		external capacitance	
Vcc	2.8V	C	1[μF]/B
Vci	2.8V		
VciOUT	Connect to Vci	Clock cycle	
DDVDH	5.6V	fDOTCLK	5MHz

(3) Test description

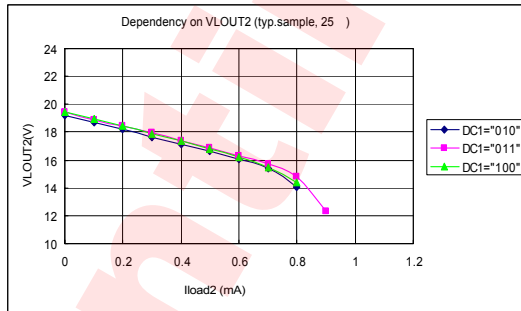
- (a) Measure the dependency of VLOUT2 on the load current (Iload2) using the step-up clock cycle of VLOUT2 as a parameter (No load is applied to pins other than those being tested.)
- (b) Measure the dependency of VLOUT2 on the load current (Iload2) using the step-up factor of VLOUT2 as a parameter (No load is applied to pins other than those being tested.)

(4) Test Results

(a) VLOUT2 load current characteristics 1
parameter: step-up cycle

Setting in the register

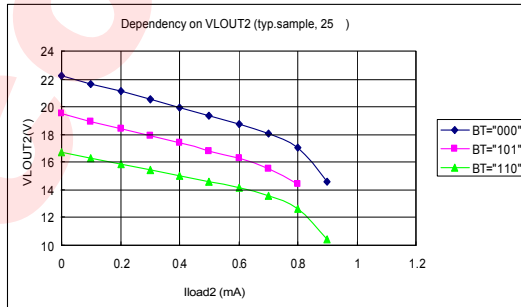
- VC2-0 = "000"
- AP2-0 = "001"
- BT2-0 = "101"
- DC02-0 = "010" (1/128)
- DC12-0 = "001" (1/128)
- DC12-0 = "011" (1/512)
- DC12-0 = "100" (1/1024)



(b) VLOUT2 load current characteristics 2
parameter: step-up factor

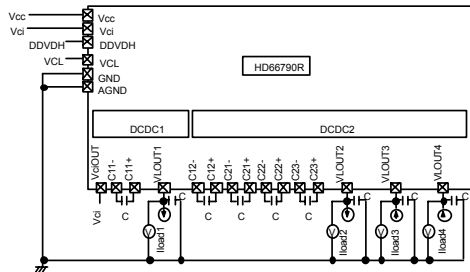
Setting in the register

- VC2-0 = "000"
- AP2-0 = "001"
- BT2-0 = "000" (x8, x-7)
- BT2-0 = "101" (x7, x-5)
- BT2-0 = "110" (x6, x-6)
- DC02-0 = "010" (1/128)
- DC12-0 = "100" (1/1024)



3. VLOUT3

(1) Test circuit



(2) Test Condition

25 TYP sample

	Applied voltage
Vcc	2.8V
Vci	2.8V
VciOUT	Connect to Vci
DDVDH	5.6V

	external capacitance
C	1[μF]/B

	Clock cycle
fDOTCLK	5MHz

(3) Test description

(a) Measure the dependency of VLOUT3 the load current (Iload3) using the step-up clock cycle of VLOUT3 as a parameter (No load is applied to pins other than those being tested.)

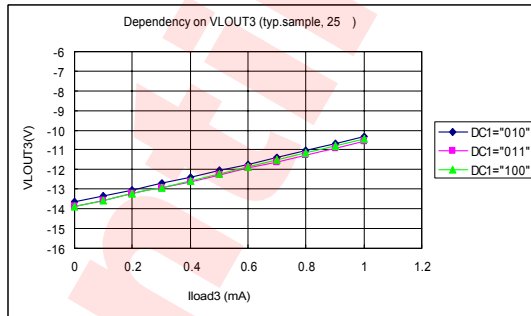
(b) Measure the dependency of VLOUT3 the load current (Iload3) using the step-up factor of VLOUT3 as a parameter (No load is applied to pins other than those being tested.)

(4) Test Results

(a) VLOUT3 load current characteristics 1
parameter: step-up cycle

Setting in the register

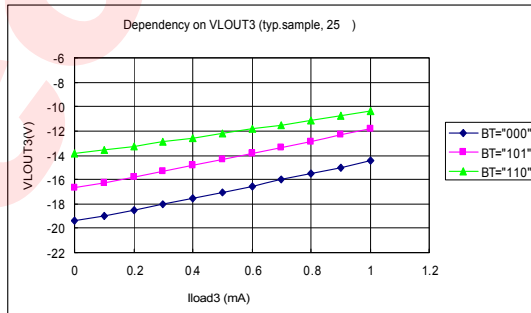
- VC2-0 = "000"
- AP2-0 = "001"
- BT2-0 = "101"
- DC02-0 = "010" (1/128)
- DC12-0 = "001" (1/128)
- DC12-0 = "011" (1/512)
- DC12-0 = "100" (1/1024)



(b) VLOUT3 load current characteristics 2
parameter: step-up factor

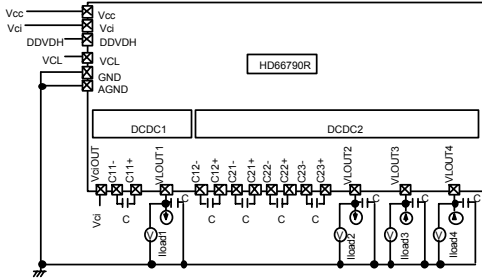
Setting in the register

- VC2-0 = "000"
- AP2-0 = "001"
- BT2-0 = "000" (x8, x-7)
- BT2-0 = "101" (x7, x-5)
- BT2-0 = "110" (x6, x-6)
- DC02-0 = "010" (1/128)
- DC12-0 = "100" (1/1024)



4. VLOUT4

(1) Test circuit



(2) Test Condition

25 TYP sample

	Applied voltage
Vcc	2.8V
Vci	2.8V
VciOUT	Connect to Vci
DDVDH	5.6V

	external capacitance
C	1[μF]/B
Clock cycle	
fDOTCLK	5MHz

(3) Test description

Measure the dependency of VLOUT4 the load current (Iload4) using the step-up clock cycle of VLOUT4 as a parameter (No load is applied to pins other than those being tested).

(4) Test Results

(a) VLOUT4 load current characteristics 1 parameter: step-up cycle

Setting in the register

VC2-0 = "000"

AP2-0 = "001"

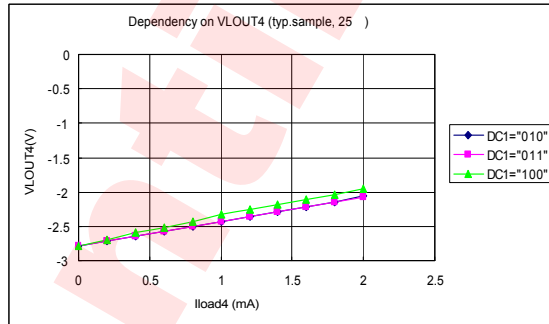
BT2-0 = "101"

DC02-0 = "010" (1/128)

DC12-0 = "001" (1/128)

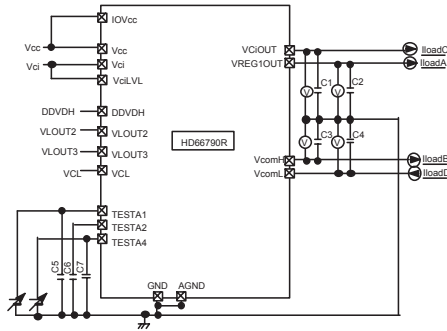
DC12-0 = "011" (1/512)

DC12-0 = "100" (1/1024)



5. VciOUT amplifier

(1) Test circuit



(2) Test Condition

25 TYP sample

Applied voltage		External capacitance	
Vcc	2.9V	C1	1[μF]/B
Vci	2.9V	C2	1[μF]/B
DDVDH	5.8V	C3	1[μF]/B
VLOUT2	VciOUT x6	C4	1[μF]/B
VLOUT3	VciOUT x-5	C5	0.1 [μF]/B
VCL	VciOUT x-1	C6	0.1 [μF]/B
		C7	0.1 [μF]/B

(3) Test description

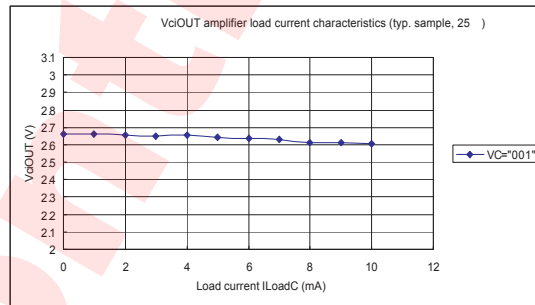
Measure the dependency of VciOUT on the load current (IloadC) with different factors for the VciOUT level (VC[2:0]) (No load is applied to pins other than those being tested).

Note: Test(n) pins are arranged for in-house test purposes. Do not use them as output open.

(4) Test Results

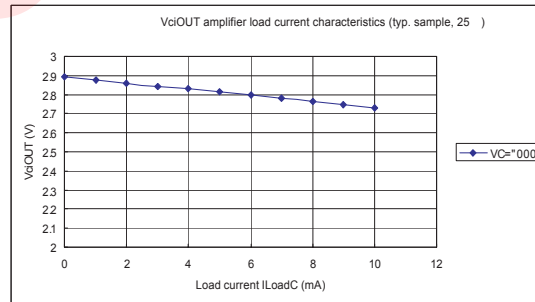
(a) VciOUT load current characteristics 1
(VciOUT = Vci x 0.92)

Setting in the register
VC2-0 = "001" (x 0.92)
AP2-0 = "011"



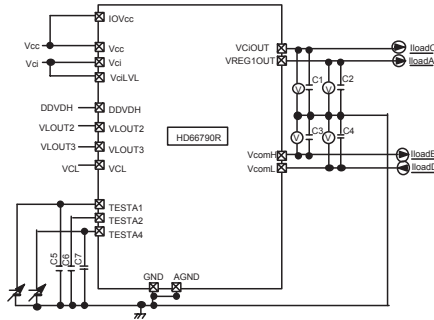
(b) VciOUT load current characteristics 2
(VciOUT = Vci x 1.00)

Setting in the register
VC2-0 = "000" (x 1.00)
AP2-0 = "011"



6. VREG1OUT amplifier

(1) Test circuit



(2) Test Condition

25 TYP sample

Applied voltage		External capacitance	
Vcc	2.9V	C1	1[μF]/B
Vci	2.9V	C2	1[μF]/B
DDVDH	5.8V	C3	1[μF]/B
VLOUT2	VciOUT x6	C4	1[μF]/B
VLOUT3	VciOUT x-5	C5	0.1 [μF]/B
VCL	VciOUT x-1	C6	0.1 [μF]/B
		C7	0.1 [μF]/B

(3) Test description

Measure the dependency of VREG1OUT on the load current (IloadA) with different factors for the VREG1OUT level (VRH[3:0]) (No load is applied to pins other than those being tested).

Note: Test(n) pins are arranged for in-house test purposes. Do not use them as output open.

(4) Test Results

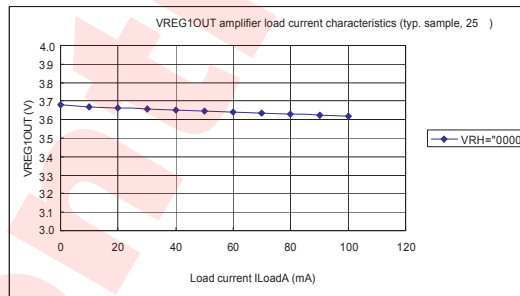
(a) VREG1OUT load current characteristics 1 (VREG1OUT = REGP x 1.27)

Setting in the register

VC2-0 = "000" (x 1.00)

AP2-0 = "011"

VRH3-0 = "0000" (x 1.27)



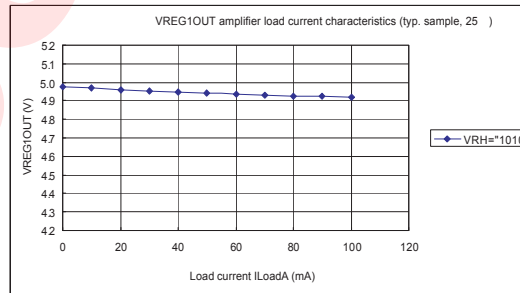
(b) VREG1OUT load current characteristics 2 (VREG1OUT = REGP x 1.72)

Setting in the register

VC2-0 = "000" (x 1.00)

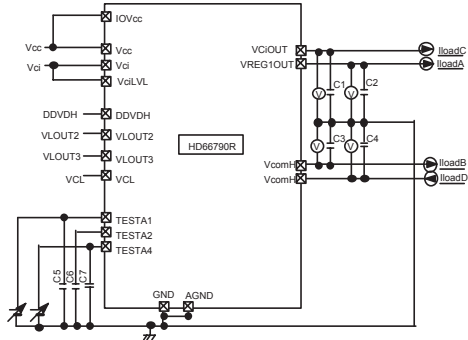
AP2-0 = "011"

VRH3-0 = "1010" (x 1.72)



7. VcomH amplifier

(1) Test circuit



(2) Test Condition
25 TYP sample

Applied voltage		External capacitance	
Vcc	2.9V	C1	1[μF]/B
Vci	2.9V	C2	1[μF]/B
DDVDH	5.8V	C3	1[μF]/B
VLOUT2	VciOUT x6	C4	1[μF]/B
VLOUT3	VciOUT x-5	C5	0.1 [μF]/B
VCL	VciOUT x-1	C6	0.1 [μF]/B
		C7	0.1 [μF]/B

(3) Test description

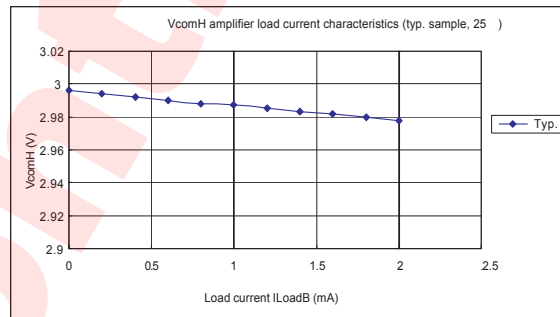
Measure the dependency of VcomH on the load current (IloadB) with different VcomH output level (No load is applied to pins other than those being tested).

Note: Test(n) pins are arranged for in-house test purposes. Do not use them as output open.

(4) Test Results

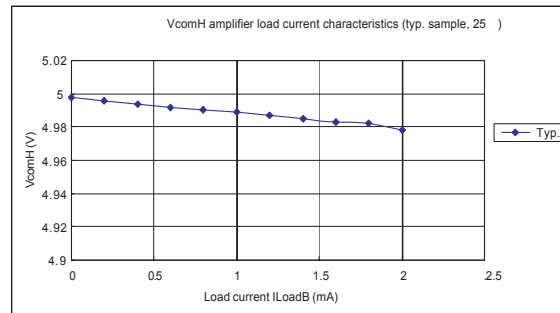
(a) VcomH load current characteristics 1
(VcomH = 3V)

Setting in the register
VC2-0 = "000" (x 1.00)
AP2-0 = "011"



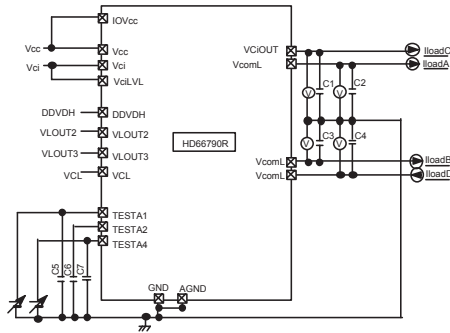
(b) VcomH load current characteristics 2
(VcomH = 5V)

Setting in the register
VC2-0 = "000" (x 1.00)
AP2-0 = "011"



8. VcomL amplifier

(1) Test circuit



(2) Test Condition

25 TYP sample

Applied voltage		External capacitance	
Vcc	2.9V	C1	1[μF]/B
Vci	2.9V	C2	1[μF]/B
DDVDH	5.8V	C3	1[μF]/B
VLOUT2	VciOUT x6	C4	1[μF]/B
VLOUT3	VciOUT x-5	C5	0.1 [μF]/B
VCL	-2.9V	C6	0.1 [μF]/B
		C7	0.1 [μF]/B

(3) Test description

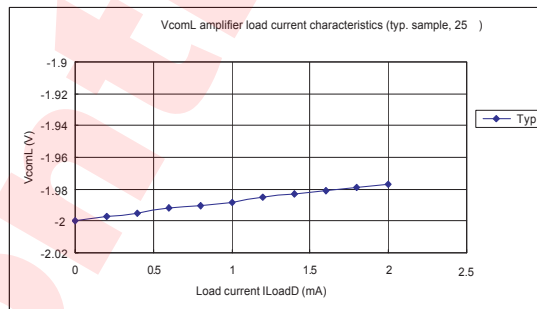
Measure the dependency of VcomL on the load current (IloadD) with different VcomL output level (No load is applied to pins other than those being tested).

Note: Test(n) pins are arranged for in-house test purposes. Do not use them as output open.

(4) Test Results

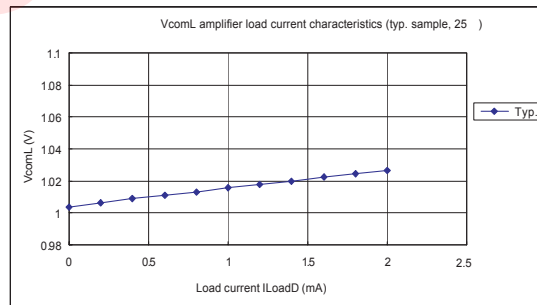
(a) VcomL load current characteristics 1 (VcomL = -2V)

Setting in the register
 VC2-0 = "000" (x 1.00)
 AP2-0 = "011"



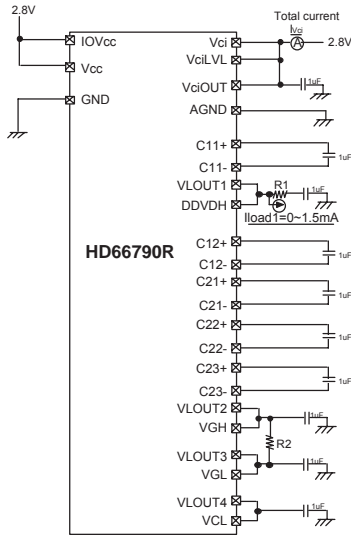
(b) VcomL load current characteristics 2 (VcomL = 1V)

Setting in the register
 VC2-0 = "000" (x 1.00)
 AP2-0 = "011"



9. Step-up load characteristics (when connected to external power supply Vci)

(1) Test circuit



(2) Test Condition

Test circuit	see Left
fFLM	60(Hz)

Instruction bits	
AP	"001"
BT	"101" (x7, x-5)
VC	"000" (x1.0)
VRH	"0110" (REGP x 1.57)
VCM	"10011" (VREG1 x 0.77)
GON	"1"
VCOMG	"0"

Pin setting	
LSENL	"H" operate level shifter
LSENR	"L" halt level shifter

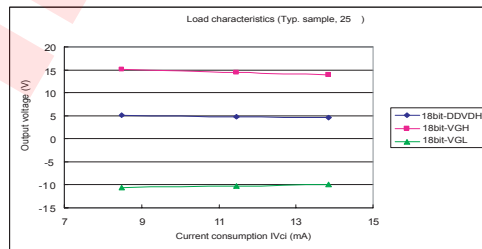
Load	
R1	0Ω~3KΩ (Iload1 = 0 ~1.5mA)
R2	82KΩ

(3) Test Results

(a) 18-bit 3 dots (RGB) /transfer mode

Setting in the register

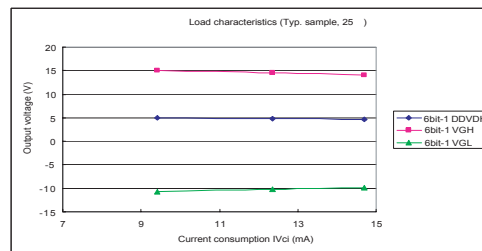
DC02-0 = "000" (1/32)
 DC12-0 = "000" (1/64)
 fDOTCLK = 5MHz



(b) 6-bit one dot (RGB) /transfer mode

Setting in the register

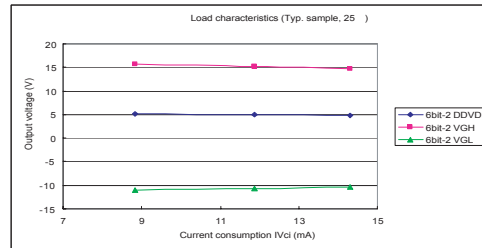
DC02-0 = "001" (1/64)
 DC12-0 = "001" (1/128)
 fDOTCLK = 15MHz



(c) 6-bit one dot (RGB) /transfer mode

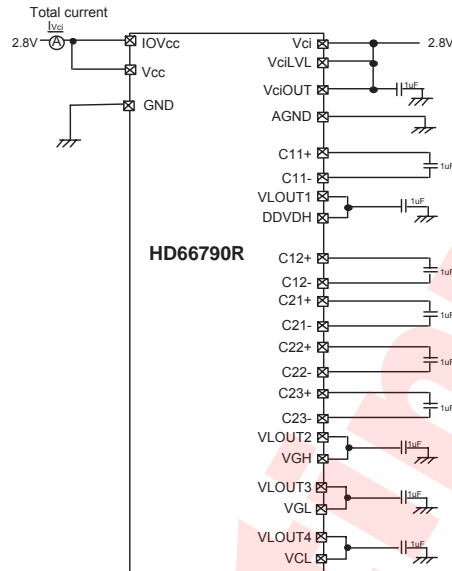
Setting in the register

DC02-0 = "010" (1/128)
 DC12-0 = "010" (1/256)
 fDOTCLK = 15MHz



10. Sleep current

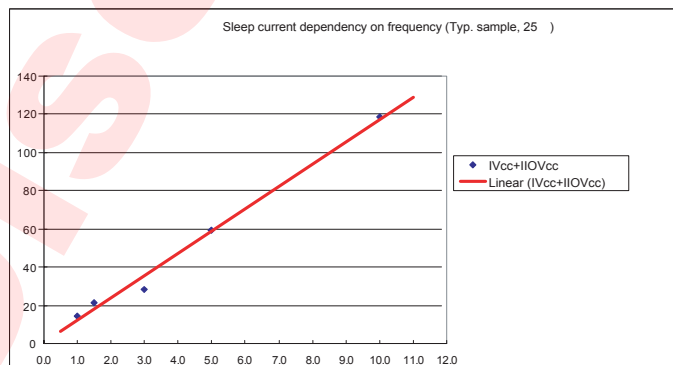
(1) Test circuit



(2) Test Condition

Instruction bits	
SLP	"1" (Halt step-up circuits)
TMB2	"1" (Halt source amplifiers)
IFS	"1" (Halt RGB interface)
fDOTCLK	1~10 (MHz)
fFLM	60Hz @ 1.5 MHz
PD[17:0]	01 alternation input

(3) Test Results



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Revision Record

Rev.	Date	Page	Contents of Modification	Approved by
1.0	2004.10.22		First issue	

Discontinue