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Semiconductor Group

The Bipolar Microcomputer Components Data Book

for

Design Engineers

Second Edition

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UNITED KINGDOM, Texas Instruments Ltd: Manton Lane, Bedford, England MK417PU, 0234-67466. D

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THE BIPOLAR MICROCOMPUTER COMPONENTS DATA BOOK

Second Edition

This data book describes a series of high-complexity bipolar digital building blocks designed specifically for implementing high-performance computer or controller systems. The series offers the system designer maximum flexibility for achieving cost-effective hardware designs from dedicated, highly specialized unique systems with tailored instructions to general-purpose computers capable of emulating existing machine instructions, or programs, without loss of software investment.

In addition to a choice between the high-performance Schottky-clamped† TTL 4-bit-slice processor element and a 16-bit computer central processing unit (CPU), the system designer can pick from a new expanded family of Schottky TTL memories (RAMs, PROMs and ROMs), and state-of-the art support functions needed to meet all control and interface requirements.

The SN54S481 and the SN74S481, with typical clock cycle times of 90 ns, are the industry's highest-complexity Schottky TTL processor elements and are the only bipolar micro/macroprogrammable elements featuring automatically sequenced iterative multiply, divide, and cyclical-redundancy algorithms. System control is simplified to a very low package count with the expandable SN54S482/SN74S482 4-bit-slice controller performing next-address generation functions.

The SBP 9900A microprocessor, a ruggedized, monolithic, 16-bit-parallel I^2L central processing unit (CPU), combines an advanced memory-to-memory architecture and a powerful minicomputer instruction set with the simplicity of a single power supply and static logic with a single-phase clock to thrust its capabilities beyond those of existing microprocessors.

The new SN74LS462/SN74LS463 fiber-optics interface functions provide a simplified, low-cost solution to interfacing requirements for optical source and detector components. This transmitter/receiver pair is designed to provide the appropriate encoding, synchronizing, and decoding logic necessary to control the transmission of digital data through a wide variety of fiber-optic data-link assemblies.

The family of high-performance Schottky TTL memories offers a wide variety of organizations providing efficient solutions for virtually any size microcontrol or program memory. A new expanded family of bipolar PROM (including standard, low-power, power-down and registered types) has dictated a new numbering system to encompass new device types. A number of advanced high-complexity I/O and interface circuits have been added to the peripheral product family. Most of these I/O and interface functions, as well as a number of the other processor support functions, are offered in space-saving 20-pin packages, which reduce package count and enhance system density.

The SBP 9708 8-bit by 8-bit parallel byte multiplier provides a 16-bit signed or unsigned 8-bit bytes. The SBP 9708 is designed to achieve the cost-effectiveness needed for microprocessor based systems.

Although this volume offers design and specification data only for bipolar computer components, complete technical data for any TI semiconductor-component product is available from your nearest TI field sales office, local authorized TI distributor, or by writing direct to: Marketing and Information Services, Texas Instruments Incorporated, P. O. Box 225012, MS 308, Dallas, Texas 75265.

We sincerely hope you will find *The Bipolar Microcomputer Components Data Book* a meaningful addition to your technical library.

†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U. S. Patent Number 3,463,975.

GENERAL INFORMATION

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ALPHANUMERIC INDEX

INTRODUCTION

This glossary consists of two parts: (1) general concepts for digital circuits including types of bipolar memories and (2) operating conditions and characteristics (including letter symbols). Some of the terms, symbols, abbreviations, and definitions used with memory integrated circuits have not, as yet, been standardized. These are currently under consideration by the EIA/JEDEC (Electronic Industries Association) and the IEC (International Electrotechnical Commission). The following are as consistent with the past and future work of these organizations as is possible to anticipate at this time.

PART I – GENERAL CONCEPTS INCLUDING TYPES OF BIPOLAR MEMORIES

Chip-Enable Input

A control input that when active permits operation of the integrated circuit for input, internal transfer, manipulation, refreshing, and/or output of data and when inactive causes the integrated circuit to be in a reduced-power standby mode.
NOTE: See "chip-select input".

Chip-Select Input

A gating input that when inactive prevents input or output of data to or from an integrated circuit.
NOTE: See "chip-enable input".

Dynamic (Read/Write) Memory

A read/write memory in which the cells require the repetitive application of control signals in order to retain stored data.
NOTES: 1. The words "read/write" may be omitted from the term when no misunderstanding will result.
2. Such repetitive application of the control signals is normally called a refresh operation.
3. A dynamic memory may use static addressing or sensing circuits.
4. This definition applies whether the control signals are generated inside or outside the integrated circuit.

First-In First-Out (FIFO) Memory

A memory from which data bytes or words can be read in the same order, but not necessarily at the same rate, as that of the data entry.

Gate Equivalent Circuit

A basic unit-of-measure of relative digital-circuit complexity. The number of gate equivalent circuits is that number of individual logic gates that would have to be interconnected to perform the same function.

Large-Scale Integration, LSI

A concept whereby a complete major subsystem or system function is fabricated as a single microcircuit. In this context a major subsystem or system, whether digital or linear, is considered to be one that contains 100 or more equivalent gates or circuitry of similar complexity.

Mask-Programmed Read-Only Memory

A read-only memory in which the data content of each cell is determined during manufacture by the use of a mask, the data content thereafter being unalterable.

Medium-Scale Integration, MSI

A concept whereby a complete subsystem or system function is fabricated as a single microcircuit. The subsystem or system is smaller than for LSI, but whether digital or linear, is considered to be one that contains 12 or more equivalent gates or circuitry of similar complexity.

Memory Cell

The smallest subdivision of a memory into which a unit of data has been or can be entered, in which it is or can be stored, and from which it can be retrieved.

Memory Integrated Circuit

An integrated circuit consisting of memory cells and usually including associated circuits such as those for address selection, amplifiers, etc.

Output-Enable Input

A gating input that when active permits the integrated circuit to output data and when inactive causes the integrated circuit output(s) to be at a high impedance (off).

Programmable Read-Only Memory (PROM)

A read-only memory that after being manufactured can have the data content of each memory cell altered once only.

Random-Access Memory (RAM)

A memory that permits access to any of its address locations in any desired sequence with similar access time for each location.
NOTE: The term RAM, as commonly used, denotes a read/write memory.

Read-Only Memory (ROM)

A memory in which the contents are not intended to be altered during normal operation.
NOTE: Unless otherwise qualified, the term "read-only memory" implies that the content is unalterable and defined by construction.

Read/Write Memory

A memory in which each cell may be selected by applying appropriate electronic input signals and the stored data may be either (a) sensed at appropriate output terminals, or (b) changed in response to other similar electronic input signals.

Small-Scale Integration, SSI

Integrated circuits of less complexity than medium-scale integration (MSI).

Very-Large-Scale Integration, VLSI

A concept whereby a complete system function is fabricated as a single microcircuit. In this context, a system, whether digital or linear, is considered to be one that contains 1000 or more gates or circuitry of similar complexity.

Volatile Memory

A memory the data content of which is lost when power is removed.

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PART II – OPERATING CONDITIONS AND CHARACTERISTICS (INCLUDING LETTER SYMBOLS)

The symbols for quantities involving time use upper and lower case letters according to the following historically evolved principles:

a. Time itself, is always represented by a lower case t.

b. Subscripts are lower case when one or more letters represent single words, e.g., d for delay, su for setup, rd for read, wr for write.

c. Multiple subscripts are upper case when each letter stands for a different word, e.g., SR for sense recovery and PLH for propagation delay from low to high.

Access Time (of a memory)

The time between the application of a specified input pulse during a read cycle and the availability of valid data signals at an output.

Example symbology:

$t_{a(ad)}$	Access time from address
$t_{a(E)}$	Access time from chip enable
$t_{a(S)}$	Access time from chip select

Clock Frequency

Maximum clock frequency, f_{max}
The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transistions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification.

Current

High-level input current, I_{IH}
The current into* an input when a high-level voltage is applied to that input.

High-level output current, I_{OH}
The current into* an output with input conditions applied that according to the product specification will establish a high level at the output.

Low-level input current, I_{IL}
The current into* an input when a low-level voltage is applied to that input.

Low-level output current, I_{OL}
The current into* an output with input conditions applied that according to the product specification will establish a low level at the output.

Off-state output current, $I_{O(off)}$
The current flowing into* an output with input conditions applied that according to the product specification will cause the output switching element to be in the off state.
Note: This parameter is usually specified for open-collector outputs intended to drive devices other than logic circuits.

*Current out of a terminal is given as a negative value.

Off-state (high-impedance-state) output current (of a three-state output), I_{OZ}
The current into* an output having three-state capability with input conditions applied that according to the product specification will establish the high-impedance state at the output.

Short-circuit output current, I_{OS}
The current into* an output when that output is short-circuited to ground (or other specified potential) with input conditions applied to establish the output logic level farthest from ground potential (or other specified potential).

Supply current, I_{CC}
The current into* the V_{CC} supply terminal of an integrated circuit.

Cycle Time

Read cycle time, $t_{c(rd)}$ (see note)
The time interval between the start and end of a read cycle.

Read-write cycle time, $t_{c(rd,wr)}$ (see note)
The time interval between the start of a cycle in which the memory is read and new data are entered, and the end of that cycle.

Write cycle time, $t_{c(wr)}$ (see note)
The time interval between the start and end of a write cycle.
NOTE: The read, read-write, or write cycle time is the actual interval between two impulses and may be insufficient for the completion of operations within the memory. A minimum value is specified that is the shortest time in which the memory will perform its read and/or write function correctly.

Hold Time

Hold time, t_h
The interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.
NOTES: 1. The hold time is the actual time between two events and may be insufficient to accomplish the intended result. A minimum value is specified that is the shortest interval for which correct operation of the logic element is guaranteed.
2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of data and the active transition) for which correct operation of the logic element is guaranteed.

Output Enable and Disable Time

Output enable time (of a three-state output) to high level, t_{PZH} (or low level, t_{PZL})
The propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined high (or low) level.

Output enable time (of a three-state output) to high or low level, t_{PZX}
The propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to either of the defined active levels (high or low).

Output disable time (of a three-state output) from high level, t_{PHZ} (or low level, t_{PLZ})
The propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined high (or low) level to a high-impedance (off) state.

*Current out of a terminal is given as a negative value.

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Output disable time (of a three-state output) from high or low level, t_{PXZ}
The propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from either of the defined active levels (high or low) to a high-impedance (off) state.

Propagation Time

Propagation delay time, t_{PD}
The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level.

Propagation delay time, low-to-high-level output, t_{PLH}
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.

Propagation delay time, high-to-low-level output, t_{PHL}
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.

Pulse Width

Pulse width, t_w
The time interval between specified reference points on the leading and trailing edges of the pulse waveform.

Example symbology:

$t_{w(cl)}$	Clear pulse width
$t_{w(wr)}$	Write pulse width

Recovery Time

Sense Recovery time, t_{SR}
The time interval needed to switch a memory from a write mode to a read mode and to obtain valid data signals at the output.

Release Time

Release time, $t_{release}$
The time interval between the release from a specified input terminal of data intended to be recognized and the occurrence of an active transition at another specified input terminal.
Note: When specified, the interval designated "release time" falls within the setup interval and constitutes, in effect, a negative hold time.

Setup Time

Setup time, t_{su}
The time interval between the application of a signal that is maintained at a specified input terminal and a consecutive active transition at another specified input terminal.
NOTES: 1. The setup time is the actual time between two events and may be insufficient to accomplish the setup. A minimum value is specified that is the shortest interval for which correct operation of the logic element is guaranteed.
2. The setup time may have a negative value in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the logic element is guaranteed.

Transition Time

Transition time, low-to-high-level, t_{TLH}
The time between a specified low-level voltage and a specified high-level voltage on a waveform that is changing from the defined low level to the defined high level.

Transition time, high-to-low-level, t_{THL}
The time between a specified high-level voltage and a specified low-level voltage on a waveform that is changing from the defined high level to the defined low level.

Voltage

High-level input voltage, V_{IH}
An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables.
NOTE: A minimum is specified that is the least positive value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.

High-level output voltage, V_{OH}
The voltage at an output terminal with input conditions applied that according to the product specification will establish a high level at the output.

Input clamp voltage, V_{IK}
An input voltage in a region of relatively low differential resistance that serves to limit the input voltage swing.

Low-level input voltage, V_{IL}
An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables.
NOTE: A maximum is specified that is the most positive value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.

Low-level output voltage, V_{OL}
The voltage at an output terminal with input conditions applied that according to the product specification will establish a low level at the output.

Negative-going threshold voltage, V_{T-}
The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage falls from a level above the positive-going threshold voltage, V_{T+}.

Off-state output voltage, $V_{O(off)}$
The voltage at an output terminal with input conditions applied that according to the product specification will cause the output switching element to be in the off state.
Note: This characteristic is usually specified only for outputs not having internal pull-up elements.

On-state output voltage, $V_{O(on)}$
The voltage at an output terminal with input conditions applied that according to the product specification will cause the output switching element to be in the on state.
Note: This characteristic is usually specified only for outputs not having internal pull-up elements.

Positive-going threshold voltage, V_{T+}
The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage rises from a level below the negative-going threshold voltage, V_{T-}.

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ACRONYMS AND MNEMONICS

AG	arithmetically greater than
AI	address input port
ALU	arithmetic logic unit
AO	address output port
BLWP	branch and load workspace pointer
CCO	counter-carry output
C	clock input (PROMs)
CE	chip enable
CIN	carry in
CL	clock
CLK	clock
CLA	carry look-ahead
CLR	clear
COUT	carry out
CPU	central processing unit
CRC	cyclic redundancy check
CRU	communications register unit
CRUIN	data input to CPU for CRU input operations
CRUOUT	data output from CPU for CRU output operations
CRUCLK	CRU-enable signal from CPU for CRU output operations
DBIN	data bus input
DO	data output port
DMA	direct memory access
DP	double precision
E	asynchronous chip enable
EQ	equal to
FPLA	field-programmable logic array
G	asynchronous output enable
INCMC	increment memory counter
INCPC	increment program counter
INT	interrupt
I/O	input or output
IP	intermediate position
INTREQ	interrupt request
LG	logically greater than
LCIR	left circulate
LD	load
LDCR	load CRU
LSA	left-shift arithmetic
LSB	least-significant bit
LSL	left-shift logical
LSP	least-significant position

MC	memory counter
MEMEN	memory enable
MSB	most-significant bit
MPX	multiplex
MSP	most-significant position
MUX	multiplexer
NC	not connected
OE	output enable
OV	overflow
PC	program counter
PLA	programmable logic array
POS	relative position control (MPS, IP, or LSP)
RCIR	right circulate
RSA	right-shift arithmetic
RSL	right-shift logical
RTWP	return workspace pointer instruction
S	asyncronous chip select
SBZ	set bit to zero
SBO	set bit to one
SP	single precision
ST	status register
STCR	store CRU
TB	test bit
WR	working register
WE	write enable
XOP	extended operation instruction
XWR	extended working register

Additional mnemonics or acronyms specifically relating to SBP 9900A instructions are found on pages 3–24 and 3–26.

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The following symbols are used in function tables on TI data sheets:

H	=	high level (steady state)
L	=	low level (steady state)
↑	=	transition from low to high level
↓	=	transition from high to low level
→	=	value/level or resulting value/level is routed to indicated destination
↶	=	value/level is re-entered
X	=	irrelevant (any input, including transitions)
Z	=	off (high-impedance) state of a 3-state-output
a . . h	=	the level of steady-state inputs at inputs A through H respectively
Q_0	=	level of Q before the indicated steady-state input conditions were established
$\bar{Q}_0$	=	complement of Q_0 or level of $\bar{Q}$ before the indicated steady-state input conditions were established
Q_n	=	level of Q before the most recent active transition indicated by ↓ or ↑
⎍	=	one high-level pulse
⎴	=	one low-level pulse
TOGGLE	=	each output changes to the complement of its previous level on each active transition indicated by ↓ or ↑.

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

If, in the input columns, a row contains H, L, and/or X together with ↑ and/or ↓, this means the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady-state levels. If the output is shown as a level (H, L, Q_0, or $\bar{Q}_0$), it persists so long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output. (If the output is shown as a pulse, ⎍ or ⎴, the pulse follows the indicated input transition and persists for an interval dependent on the circuit.)

TEXAS INSTRUMENTS
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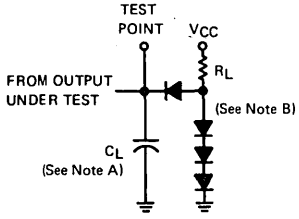
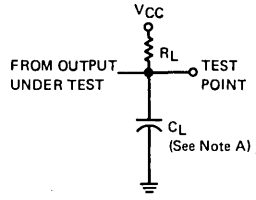
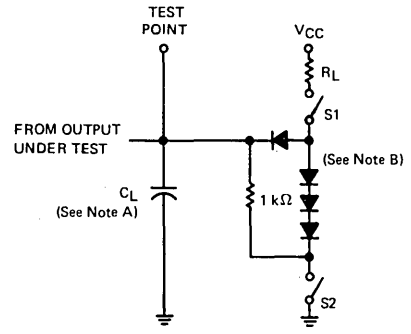
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR BI-STATE TOTEM-POLE OUTPUTS

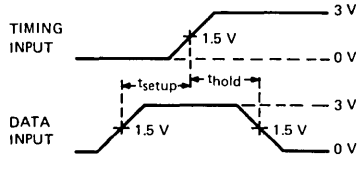


LOAD CIRCUIT FOR OPEN-COLLECTOR OUTPUTS

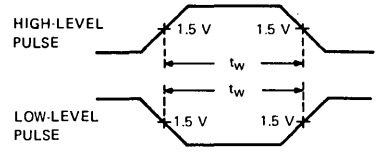


LOAD CIRCUIT FOR THREE-STATE OUTPUTS

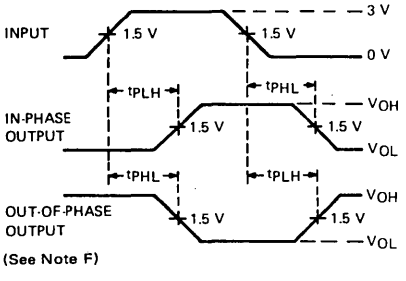
NOTES. A. C_L includes probe and jig capacitance.
B. All diodes are 1N916 or 1N3064.



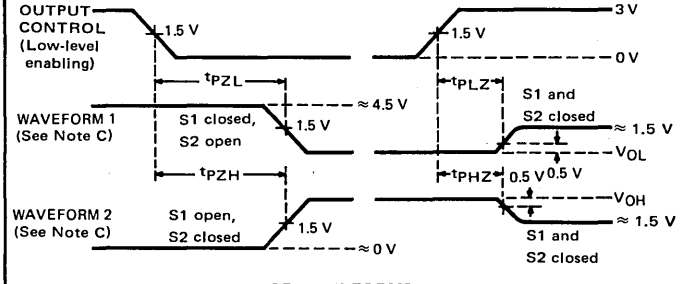
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE WIDTHS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
E. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_{out} \approx 50\ \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
F. When measuring propagation delay times of 3-state outputs, switches S1 and S2 are closed.

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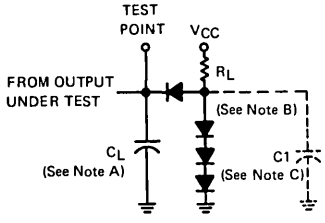
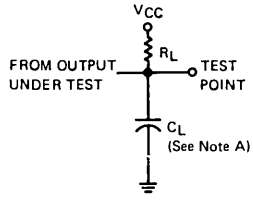
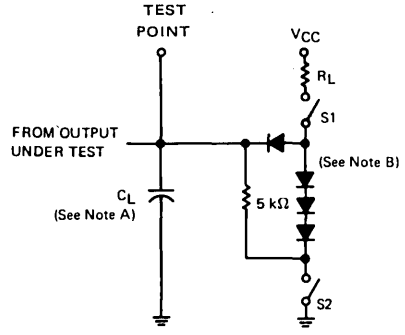
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR BI-STATE TOTEM-POLE OUTPUTS

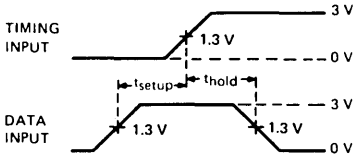


LOAD CIRCUIT FOR OPEN-COLLECTOR OUTPUTS

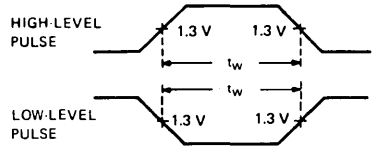


LOAD CIRCUIT FOR THREE-STATE OUTPUTS

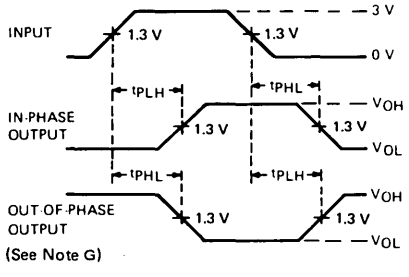
NOTES A. C_L includes probe and jig capacitance.
B. All diodes are 1N916 or 1N3064.
C. C1 (30 pF) is used for testing Series 54/74L devices only.



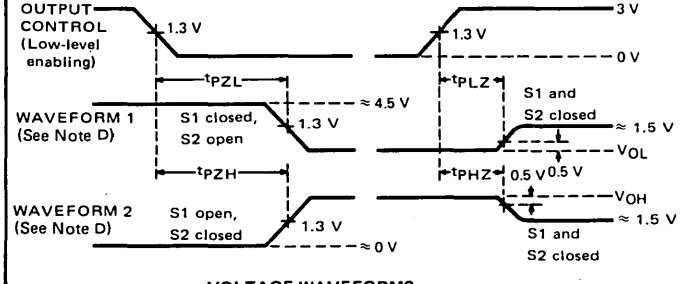
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE WIDTHS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
E. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
F. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_{out} \approx 50\ \Omega$, $t_r \leq 15$ ns, $t_f \leq 6$ ns.
G. When measuring propagation delay times of 3-state outputs, switches S1 and S2 are closed.

4-Bit-Slice Schottky Processor Components

4-BIT-SLICE PROCESSOR COMPONENTS

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LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Continued)

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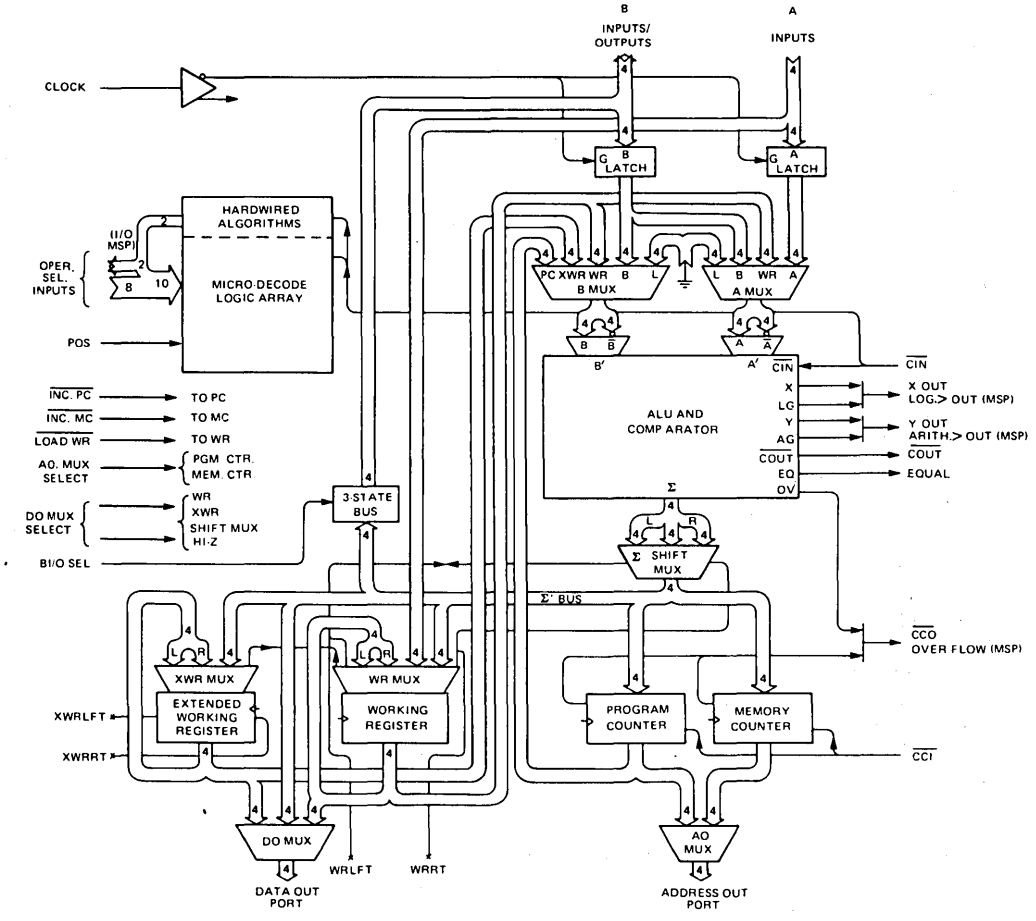


FUNCTIONAL BLOCK DIAGRAM FOR 'S481

1 INTRODUCTION

These Schottky TTL 4-bit expandable parallel binary micro/macroprogrammable processor element building blocks are designed specifically for implementing high-performance digital computer/controllers. With the ability to efficiently emulate existing systems, they can be used to upgrade hardware performance with full compatibility to protect software investments.

The SN54S/74S481, Schottky TTL performs typically at a clock cycle time of 90 nanoseconds at 345 milliamperes of supply current.

1.1 ARCHITECTURAL FEATURES

Designed with full parallel dual input/output ports, the memory-to-memory architecture provides a new dimension in interrupt processing or program context switching flexibilities. Static bipolar logic performs each microinstruction within a single clock cycle.

Primary among the architectural features are:

- Microprogrammable, bit-slice design is expandable in 4-bit multiples
- Full parallel dual input/output ports for use in advanced memory-to-memory architecture
- Full-function ALU with carry look-ahead, magnitude, and overflow decision capabilities
- Double-length accumulator with full shifting capability and sign-bit handling
- Dual memory address generators on-chip.

1.2 OPERATIONAL FEATURES

The functional capabilities, characterized by the 24,780 unique operations, coupled with the macroprogrammable multiply and divide algorithms, make these processor elements particularly attractive for implementing advanced high performance computers and controllers.

In addition to the full parallel data bus structure, the 'S481 architecture also features asynchronous access to data routing and counter updating controls which, when combined with the most versatile instruction set available (see operational description) maximizes flexibility, efficiency, and performance. Simultaneous compound operations in the form of an ALU function with shift, plus destination selection with address/iteration updating, plus address *and* present data to memory can be accomplished in a single microcyle. Some other operational features are:

- Simultaneous one-clock compound operations, with status, can reduce microcycles and improve throughput
- Pre-programmed CRG and double-precision multiply/divide algorithms
- Double length accumulator with full bidirectional single/double precision arithmetic/logical/circulate shift capabilities include sign protection
- Full micro-operational control is provided for programming: address updating, data and address source selection, and direct transfer of data to working register or working memory
- Relative position control defines bit-slice rank and sign handling in N-bit applications.

1.3 MECHANICAL FEATURES

These processor elements are supplied in either a high-density quad-in-line ceramic package or a plastic dual-in-line package. The high-density 48-pin ceramic package has quad pin rows formed on 600- and 800-mil centers. Within each of the four rows, the pin spacing is 100 mils, center-to-center. The plastic dual-in-line package has standard 100-mil spacing on 600-mil centers. Outline drawings are provided in Section 6 of this data book.

TABLE 1
FUNCTIONAL DESCRIPTIONS

PIN NUMBER	PIN NAME	PIN FUNCTION	INPUT, OUTPUT, OR INPUT/OUTPUT
46, 47 1, 2	BI/O0, BI/O1 BI/O2, BI/O3	4-bit parallel data input port to the B latch, or 4-bit parallel data output for the Σ-bus when not being used as an input.	Inputs/Outputs
6, 5 4, 3	AI0, AI1 AI2, AI3	4-bit parallel data input port to the A latch and WR.	Inputs
7, 8 9, 10 17, 14 13, 11 15, 16	OP0, OP1 OP2, OP3 OP4, OP5 OP6, OP7 OP8, OP9	OP0 through OP9 serve as a 10-bit parallel operation-select input to the micro-decode logic array. In the most-significant position, OP8 and OP9 additionally serve as open-collector outputs during multiply and divide algorithms. In the least-significant position, OP9 serves as an open-collector output during the CRC algorithm.	Inputs
12	V_{CC}	Single 5-volt power-supply terminal.	Supply Voltage Pin
18	$\overline{CIN}$	Receives low-active ripple carry input data.	Input
19	POS	Directs internal and input/output end-conditions required to define the relative position of each bit-slice when N-SN74S481's are cascaded to implement Nx4-bit word lengths. When biased at 2.4 volts, the package operates as the least-significant (LSP) slice; when grounded, it functions as an intermediate (IP) slice; and when high, 5 volts, it functions as the most-significant (MSP) slice.	Input
20	Y/AG	In least-significant and intermediate positions outputs arithmetic carry generate (Y) for use with look-ahead. In most-significant position outputs true arithmetically-greater-than signal.	Output
21	X/LG	In least-significant and intermediate positions outputs arithmetic carry propagate (X) for use with look-ahead. In most-significant position outputs true logically-greater-than signal.	Output
22	$\overline{COUT}$	Outputs low-active ripple carry data.	Output
23	EQ	Outputs true (active-high) equality of Σ' bus equals zero for each 4-bit slice. The open-collector output permits wire-AND to achieve Nx4-bit equality output.	Open-Collector Output
24	$\overline{LD\,WR}$	When low, data applied at the AI port coincident with the ↑ clock transition is loaded into the WR.	Input
26 25	WRRT, WRLFT	Working register and Σ-bus shift interconnectivity pins. WRRT receives left-shift and outputs right-shift (true) data. WRLFT receives right-shift and outputs left-shift (true) data. Shift can be single-precision, double-precision, signed or unsigned.	Bidirectional I/O
28 27	XWRRT, XWRLFT	Extended working register shift interconnectivity pins. XWRRT receives left-shift and outputs right-shift (true) data. XWRLFT receives right-shift and outputs left-shift (true) data. Shift can be single-precision, double-precision, signed or unsigned.	Bidirectional I/O
29 30	D0 D1	Selects one of three DOP sources (WR, XWR, or Σ-bus) or places the DOP outputs in a high-impedance state.	Inputs
34 33 32 31	DOP0 DOP1 DOP2 DOP3	4-bit parallel, data-out port. DOP0 is LSB.	3-state outputs
35	$\overline{INCMC}$	When low, enables the MC to increment as directed by $\overline{CCI}$ on the next ↑ clock transition. When high, inhibits MC to hold mode. As $\overline{CCO}$ is common to MC and PC, the MC should be inhibited when PC is enabled.	Input
36	GND	Common or ground terminal for the supply voltage.	
37	$\overline{CCO}$/OV	In least-significant and intermediate positions a low-level output indicates that either the PC or MC is at maximum count. As $\overline{CCO}$ is common for both PC and MC ambiguous carry can be avoided if one or both counters is/are disabled by the $\overline{INCPC}$ and/or $\overline{INCMC}$ inputs. In the most-significant position, a high-level output, depending on the operation selected, indicates that the WR, XWR, or ALU will overflow (OV) on the next clock.	Output

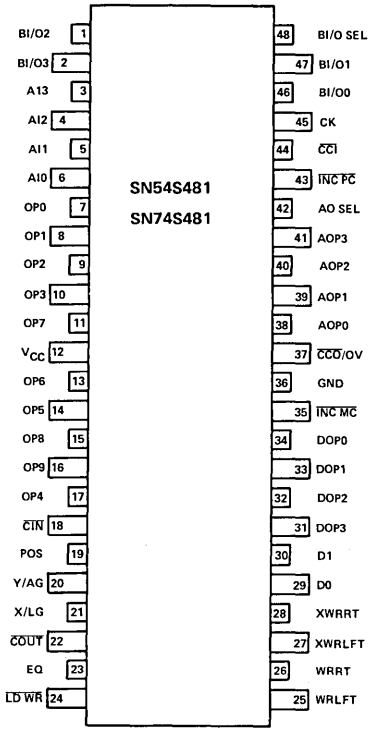


FIGURE 1–PIN ASSIGNMENTS

TABLE 1 (Continued)

PIN NUMBER	PIN NAME	PIN FUNCTION	INPUT, OUTPUT, OR INPUT/OUTPUT
38, 39 40, 41	AOP0, AOP1 AOP2, AOP3	4-bit parallel address-out port.	Outputs
42	A0	Selects one of two AOP sources (PC or MC).	Input
43	$\overline{\text{INCPC}}$	When low, enables the PC to increment as directed by $\overline{\text{CCI}}$ on the next ↑ clock transition. When high, inhibits PC to hold mode. As $\overline{\text{CCO}}$ is common to PC and MC, the PC should be inhibited when MC is enabled.	Input
44	$\overline{\text{CCI}}$	In least-significant position, a low input directs enabled PC or enabled MC to increment by one on next ↑ clock transition. In the LSP, a high directs enabled PC or enabled MC to increment by 2. In other positions, a low is a carry input and a high inhibits the counter.	Input
45	CK	When high, enables the transparency of A and B input latches. When low, latches A and B input data. Clocks synchronous registers and counters on the positive transition.	Input
48	BI/O SEL	When low, enables BI/O to output Σ-bus data. When high, the BI/O output drivers are placed in a high-impedance state permitting BI/O to be used as data inputs.	Input

2. DETAILED FUNCTIONAL DESCRIPTIONS

2.1 MICRO-DECODING LOGIC ARRAY

The micro-decoding logic array is a dedicated 11-input PLA decoding 73 product terms to generate 24 control lines needed to implement the 14 operation forms. The eleven inputs consist of the ten operation select lines (OP0 through OP9) and the ALU carry input. The carry input, utilized as an additional operation select line during operation forms not performing arithmetic functions, maximizes system pin efficiency and functional density.

In an expanded word length system (two or more 'S481's), operation select inputs 8 (OP8) and 9 (OP9) assume an input/output capability in the most-significant or least-significant package as a result of the position control and the type of operation being performed. During microprogrammable operation forms I through IX, OP8 and OP9 function simply as another input; but, during the macroprogrammable operations of forms X through XIV one or both become an output during iterations. Table 2 summarizes by operation form the control (output) package and the operation lines which are used as an output.

TABLE 2
MSP OP8 and OP9 ITERATIVE FUNCTION SUMMARY

OP. FORM	ALGORITHM	CONTROL PACKAGE	OPERATION SELECT I/O	
			OP8	OP9
I thru IX	All	None	INPUT	INPUT
X	CRC ACCUMULATION	LSP	INPUT	OUTPUT
XI	SIGNED DIVIDE	MSP	OUTPUT	OUTPUT
XII	UNSIGNED DIVIDE	MSP	INPUT	OUTPUT
XIII	UNSIGNED MULTIPLY	MSP	INPUT	OUTPUT
XIV	SIGNED MULTIPLY	MSP	OUTPUT	OUTPUT

If the macroinstructions are to be used in an expanded word length, OP8 and OP9 select lines of the MSP and the OP9 line of the LSP should be driven from either a 3-state output (which can be placed in high-impedance state) or an open-collector output (which can be wire-OR'ed with the OP select I/O lines). During an iterative function for which the OP line is designated as an open-collector output, the OP line driver should be placed in a high-impedance or off state permitting the output function to drive similar OP lines in the remaining packages.

The output state of OP8 or OP9 is a function of on-chip status decoder as enumerated in the flow diagrams illustrating the five algorithms.

2.2 RELATIVE POSITION CONTROL (POS)

The single line position control, with the ability of decoding one of three input logic states, provides each 'S481 in an expanded word length system with the capability of identifying its relative position. The relative positions, with the corresponding input logic levels are enumerated in Table 3.

TABLE 3
POSITION CONTROL FUNCTIONS

POS INPUT LOGIC LEVEL	RELATIVE POSITION
$\geq$ 3.6 V	MOST-SIGNIFICANT POSITION (MSP)
1.8 V to 3 V	LEAST-SIGNIFICANT POSITION (LSP)
$\leq$ 0.8 V	INTERMEDIATE POSITION (IP)

This relative position identification dictates how each 'S481 in the system handles the multi-purpose I/O accommodations and ALU sign and magnitude functions. See Table 4. Shift/Circulate interconnectivity bit transfers are explained in detail under shift/circulate transfer multiplexers.

TABLE 4
DUAL-FUNCTION LOGIC I/O PINS

PIN	MSP	IP	LSP
X/LG	LG (OUT)	X (IN)	X (IN)
Y/LG	AG (OUT)	Y (IN)	Y (IN)
$\overline{CCO}$/OV	OVERFLOW (OUT)	$\overline{CCO}$ (OUT)	$\overline{CCO}$ (OUT)

X AND Y ARE CARRY LOOK-AHEAD FUNCTIONS

2.3 CLOCK

The clock synchronizes the entry or change of data in the 'S481 registers and counters, and it controls the status of the A and B input latches. A typical clock cycle is illustrated in Figure 2. The low-to-high transition of the clock input is the clocking edge for any combination of either the working register, extended working register, flag flip-flops, and the program counter or the memory counter activated by the resident operation. During the low-level portion of the clock input, both input latches are latched ensuring data stability at the positive clock transition. After the clock has gone to a high level, the input latches are placed in a transparent mode to accept the next set of input data.

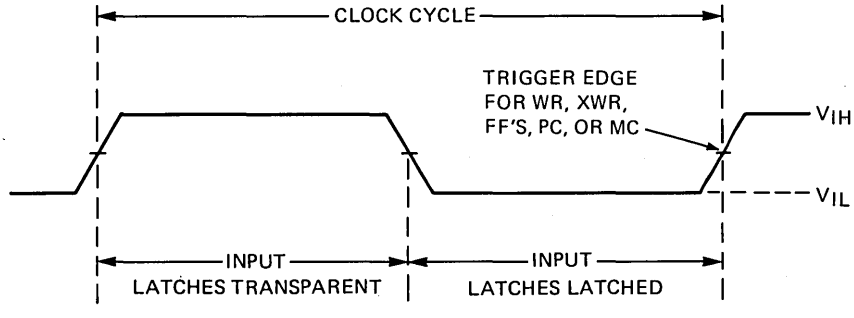


FIGURE 2 – CLOCK CYCLE

2.4 LATCHED DATA INPUT PORTS

The SN54S/74S481 features dual input ports combined with data flow paths which are designed specifically to reduce the number of system clock cycles needed to enter operands and/or data. Both the A and B input ports are latched, eliminating the need for external registers, to simplify interfacing directly with system data bus paths.

The A input port data is made available to both the input latch and the working register which allows A data to be loaded into the working register directly.

The B port is configured to serve as an input/output data path providing the capability to:

a. Input data to the B latch
b. Output sum-bus data.

This I/O port is designed specifically to simplify implementation of data transfers to the external working memory.

Both the A and B latches are transparent when the 'S481 clock input is high. Data applied at the A and B inputs should be stable anytime prior to or at least coincident with the falling edge of the clock input (see Figure 3). After the clock falling edge, the data inputs should be held steady for $t_{hold(data)}$ or longer to facilitate the on-chip clock buffers to latch the data.

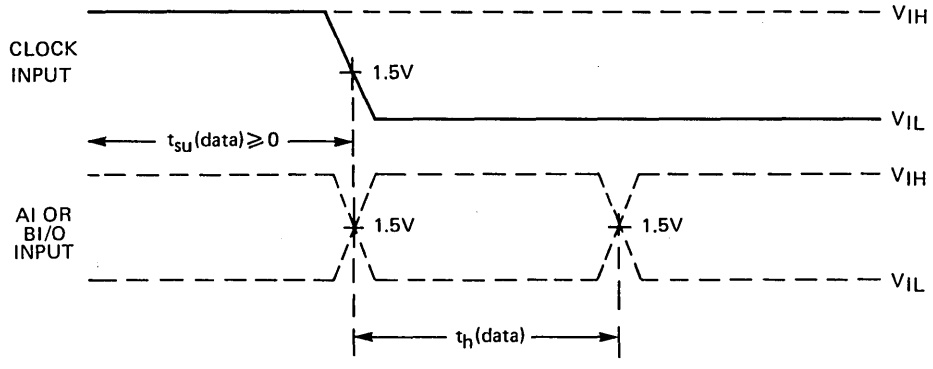


FIGURE 3 – INPUT LATCHES SETUP/HOLD TIMES

The A input port latch data is routed to the A input multiplexers, and the B input port latch data is sourced to both the A and B input multiplexers.

2.5 A AND B OPERAND SOURCES

The A and B input multiplexers source the ALU A' and B' ports through true/complement conditional inverter circuits. Data routing for each, illustrated and listed in Figure 4, provides the ALU with access to the true or complement of:

ALU A' PORT

1. A input latch
2. B input latch
3. Working Register
4. Low logic level inputs (force zeros)

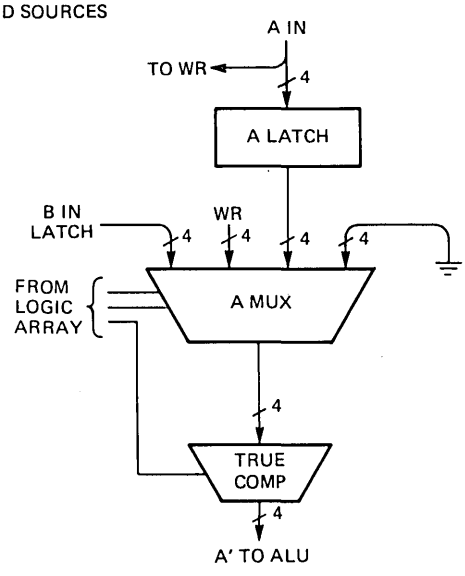
ALU B' PORT

1. B input latch
2. Sum bus
3. Working register
4. Extended working register
5. Program counter
6. Low logic level inputs (force zeros)

The A and B multiplexers and true complement circuits, under control of the resident operation code, are selectable at the microprogram level. The number of A or B multiplexer sources available depend upon the specific operation being performed by the 'S481. Operation form descriptions contain detailed microprogramming.

The A and B input multiplexers, with selectable true and complement operand sources, maximizes the processing power of the 'S481 by minimizing the active components needed to achieve both the simple but highly flexible data routing tasks and full ALU capabilities.

A OPERAND SOURCES

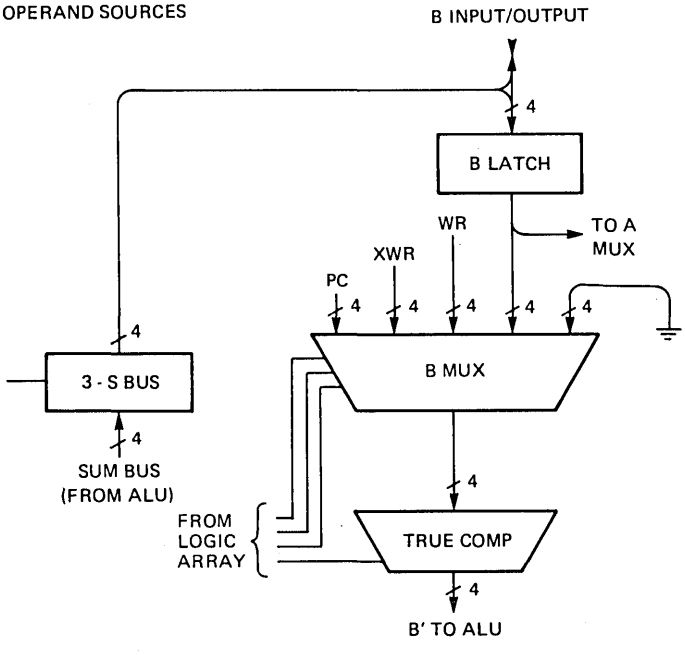


A INPUT SELECTIONS

A IN → A'
$\overline{\text{A IN}}$ → A'
LOGIC ONE'S → A'
LOGIC ZERO'S → A'
B IN → A'
$\overline{\text{B IN}}$ → A'
WR → A'
$\overline{\text{WR}}$ → A'

2

B OPERAND SOURCES



B INPUT/OUTPUT SELECTIONS

B IN → B'
$\overline{\text{B IN}}$ → B'
LOGIC ONE'S → B'
LOGIC ZERO'S → B'
(B IN) • (WR) → B'
$\overline{\text{(B IN) • (WR)}}$ → B'
WR → B'
$\overline{\text{WR}}$ → B'
(B IN) • (XWR) → B'
$\overline{\text{(B IN) • (XWR)}}$ → B'
XWR → B'
$\overline{\text{XWR}}$ → B'
(B IN) • (PC) → B'
$\overline{\text{(B IN) • (PC)}}$ → B'
PC → B'
$\overline{\text{PC}}$ → B'

FIGURE 4 – ALU OPERAND SOURCES

2.6 ARITHMETIC/LOGIC UNIT (ALU)

The 4-bit, parallel, binary arithmetic/logic unit provides the arithmetic/Boolean operand combination/modification mechanism including magnitude and overflow status. The ALU performs, as directed by the resident operation form, one of four basic functions which, when combined with the operand selections at the A and B multiplexers, extends the arithmetic/logic capabilities to that of a full 16-function ALU.

When compared to other bit-slice processor elements, unique to the 'S481 arithmetic architecture are the parallel input ports and fully microprogrammable symmetry for all ALU functions within the selections of the A and B input multiplexers.

Logical and arithmetic operation forms for the 'S481 are shown in Table 5. The full functional power of the 'S481 can be visualized only if it is understood that although both ALU's have parallel A and B input ports, the 'S481 architecture not only provides access to multiple sources but has the capability to route true or complement of any source to the A and B ALU port. This means that for a subtract operation, the subtrahend may be either an A or B input. In addition to maximizing data routing capabilities of the 'S481 at minimum logic/gate levels, this architecture permits fully symmetrical operations to be performed on the A or B sources within the selections offered by these 'S481 arithmetic/logical operation forms.

TABLE 5
'S481 ALU AND LOGIC FUNCTIONS

DATA INPUT		TWO'S COMPLEMENT INTEGER ARITHMETIC OP'S		LOGICAL OP'S (FORM VIII) $\overline{CIN}$ = H OR L		
A PORT	B PORT	$\overline{CIN}$ = L	$\overline{CIN}$ = H	OR	NOR	EX-NOR
ZEROS	ZEROS	1	0	ZEROS	ONES	ONES
ZEROS	ONES	0	MINUS 1	ONES	ZEROS	ZEROS
ONES	ZEROS	0	MINUS 1	ONES	ZEROS	ZEROS
ONES	ONES	MINUS 1	MINUS 2	ONES	ZEROS	ONES
A	ZEROS	A PLUS 1	A	A	$\overline{A}$	$\overline{A}$
A	ONES	A	A MINUS 1	ONES	ZEROS	A
$\overline{A}$	ZEROS	MINUS A	MINUS A MINUS 1	$\overline{A}$	A	A
$\overline{A}$	ONES	MINUS A MINUS 1	MINUS A MINUS 2	ONES	ZEROS	$\overline{A}$
ZEROS	B	B PLUS 1	B	B	$\overline{B}$	$\overline{B}$
ONES	B	B	B MINUS 1	ONES	ZEROS	B
ZEROS	$\overline{B}$	MINUS B	MINUS B MINUS 1	$\overline{B}$	B	B
ONES	$\overline{B}$	MINUS B MINUS 1	MINUS B MINUS 2	ONES	ZEROS	$\overline{B}$
A	B	A PLUS B PLUS 1	A PLUS B	A + B	$\overline{A} \cdot \overline{B}$	$\overline{A \oplus B}$
A	$\overline{B}$	A MINUS B	A MINUS B MINUS 1	A + $\overline{B}$	$\overline{A} \cdot B$	A ⊕ B
$\overline{A}$	B	B MINUS A	B MINUS A MINUS 1	$\overline{A}$ + B	A · $\overline{B}$	A ⊕ B
$\overline{A}$	$\overline{B}$	MINUS A MINUS B MINUS 1	MINUS A MINUS B MINUS 2	$\overline{A}$ + B	A · B	$\overline{A \oplus B}$

Some unique one-clock arithmetic/iterative capabilities of the 'S481 are listed in Table 6.

TABLE 6
EXTENDED ALU FUNCTIONS OF 'S481

FORM NO.	FUNCTION
I	A (ALU) B · WR A (ALU) B · XWR A (ALU) B · PC
II	A (ALU) B DOUBLE-PRECISION SHIFTED LOGICAL LEFT OR RIGHT
III	A (ALU) B SINGLE-PRECISION SHIFTED LOGICAL OR ARITHMETIC LEFT OR RIGHT

Table 5 also indicates the 16 logical combinations of two Boolean variables which are selectable for the OR, NOR, and exclusive-NOR functions. Full symmetry of the ALU and the ability to select the complement of input data extends the logic functions for performance of:

a. NAND
b. AND
c. Exclusive-OR
d. Mixed combinations of each
e. Transfer functions for true or inverted data
f. All ones or all zeros.

2.7 ALU MAGNITUDE AND CARRY FUNCTIONS

The 'S481 ALU is fully decoded on chip to generate three magnitude outputs (status lines) and both ripple and look-ahead carry functions. The magnitude outputs and their status indications are as follows:

2.7.1 Equal (EQ, See Figure 5)

The results of the resident ALU operation are compared at the sum-bus for all bits high during subtract and left-shift arithmetic operations, or for all bits low during other operations.

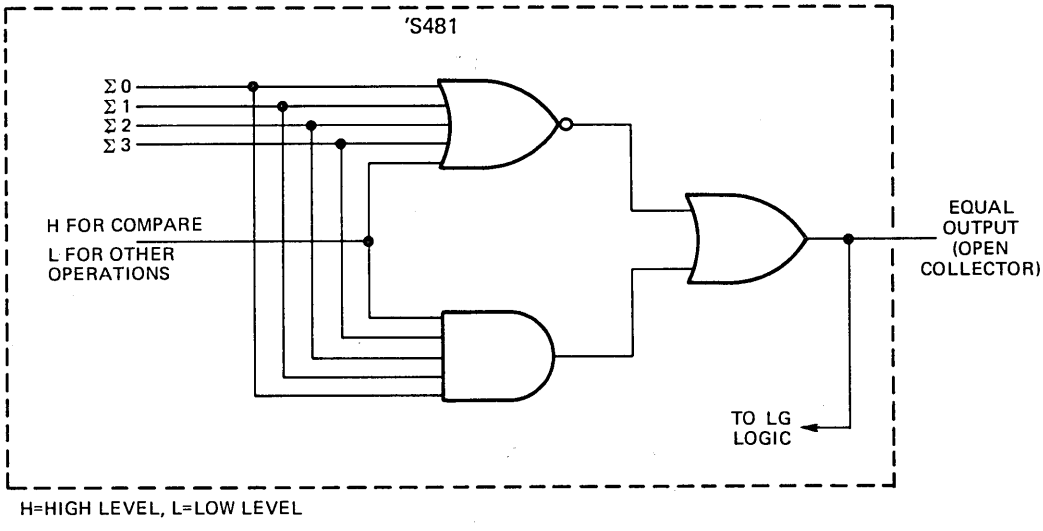


FIGURE 5 – EQUAL OUTPUT

2.7.2 Logically-Greater Than (LG, See Figure 6)

In the most-significant package (MSP) the X look-ahead function from the ALU is inhibited and the logically-greater-than (LG) output is enabled. See Figure 6. The MSP LG output is active during arithmetic and shift operation forms to provide a status indication that can be used when it is desirable to compare two unsigned integer numbers. The specific status for each operation form is listed in Table 7.

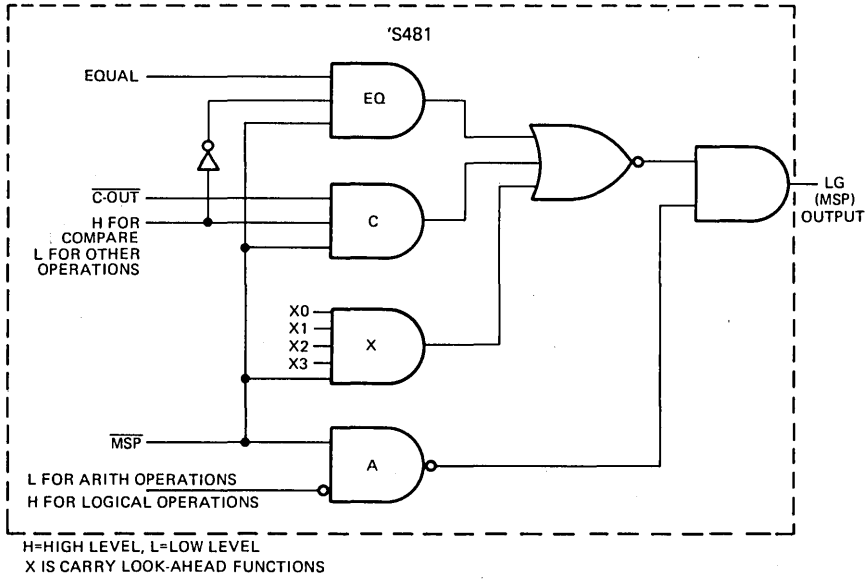


FIGURE 6 – MSP LOGICALLY-GREATER-THAN (LG) OUTPUT

TABLE 7
MSP LOGICALLY-GREATER-THAN (LG) OUTPUT

OP FORM	TYPE OF OP	LG = H INDICATES
I or II (ARITH)	ALL	Σ-BUS $\neq$ ZERO (EQ = L)
III (ARITH WITH SHIFT)	LSL, RSL	Σ-BUS $\neq$ ZERO (EQ = L)
	LSA or RSA	ADDER C-OUT
IV, V, or VI (SHIFTS)	ALL	AI $\neq$ ZERO (EQ = L)
VII (COMPARE)	A : B	A IS LG THAN B
	B : A	B IS LG THAN A
VIII (LOGICAL)	ALL	Σ-BUS $\neq$ ZERO (EQ = L)
IX (NO OP)	ZERO Σ-BUS	LG = L (EQ = H)
X THRU XIV	HARDWIRED ALGORITHMS	SEE OPERATION FORM DESCRIPTION

2.7.3 Arithmetically-Greater Than (AG, See Figure 7)

In the most-significant package (MSP) the Y look-ahead function from the ALU is inhibited and the arithmetically-greater-than (AG) output is enabled. The MSP AG output is active during arithmetic and shift operation forms to provide a status indication that can be used when it is desirable to compare two signed integer numbers. The specific status for each operation form is listed in Table 8.

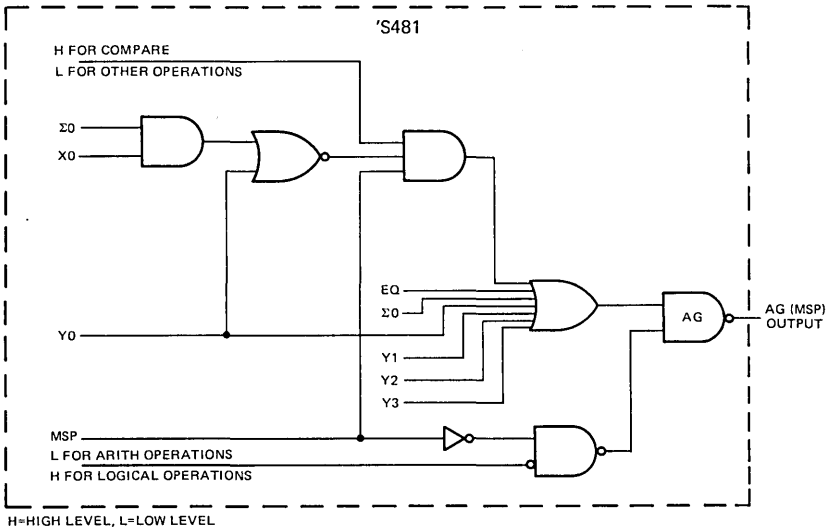


FIGURE 7 – MSP ARITHMETICALLY-GREATER-THAN (AG) OUTPUT

TABLE 8
ALU CARRY AND MSP ARITHMETICALLY-GREATER-THAN (AG) OUTPUTS

OPERATION FORM	LSP AND IP				MSP			
	X	Y	EQ	$\overline{C\text{-}OUT}$	LG	AG	EQ	$\overline{C\text{-}OUT}$
LOGICAL OPERATIONS	L	H	Σ-BUS = 0	$\overline{C\text{-}IN}$	Σ-BUS ≠ 0	Σ-BUS > 0	Σ-BUS = 0	$\overline{C\text{-}IN}$
ARITHMETIC OPERATIONS:								
COMPARE	X	Y	A=B	$\overline{C\text{-}OUT}$	A LG B or B LG A	A AG B or B AG A	A = B	$\overline{C\text{-}OUT}$
ALL OTHER ARITHMETIC	X	Y	Σ-BUS = 0	$\overline{C\text{-}OUT}$	Σ-BUS ≠ 0	Σ-BUS AG 0	Σ-BUS AG 0	$\overline{C\text{-}OUT}$

X and Y are carry look-ahead functions.

2.8 OPERAND OVERFLOW

In the most-significant package (MSP) the counter-carry output ($\overline{CCO}$) function from the program/memory counter is inhibited and the overflow (OV) output is enabled. The MSP OV output is active during arithmetic and shift operation forms to provide a status indication that the result of the operation cannot be correctly represented with the number of bit positions available. When the OV output goes high, it indicates that the next clock will:

a. During arithmetic operations, cause the ALU to overflow.
b. During left-shift arithmetic operations, cause the shifted register to overflow.

Table 9 enumerates the specific indicators generated.

TABLE 9
MSP OVERFLOW (OV) OUTPUT

OP FORM	TYPE OF OP	OV = H INDICATES
I or II (ARITH)	ADD or SUB	ALU OVERFLOW
III (ARITH WITH SHIFT)	LSL, RSL	ALU OVERFLOW
	RSA	OV = L
	LSA	NEXT CLOCK WILL CAUSE SHIFT OVERFLOW
IV, V, or VI (SHIFTS)	LSA	NEXT CLOCK WILL CAUSE SHIFT OVERFLOW
	ALL OTHERS	OV ≡ L
VII (COMPARE)	A : B	UNDEFINED
	B : A	UNDEFINED
VIII (LOGICAL)	ALL	OV ≡ L
IX (NO OP)	ZERO Σ-BUS	OV ≡ L
X THRU XIV	HARDWIRED ALGORITHMS	SEE OPERATION FORM DESCRIPTIONS

H = high level, L = low level

2.9 SUM' BUS MULTIPLEXER

The sum'-bus multiplexer, sourced by the ALU, provides a means for accomplishing a shift operation on the ALU operand without affecting the contents of WR, XWR, PC or MC (See Figure 8). Functionally, this multiplexer can be used to:

a. Shift the operand left or right (one bit position) arithmetic, logical, or circulate
b. Pass the operand without shift to the Σ' bus.

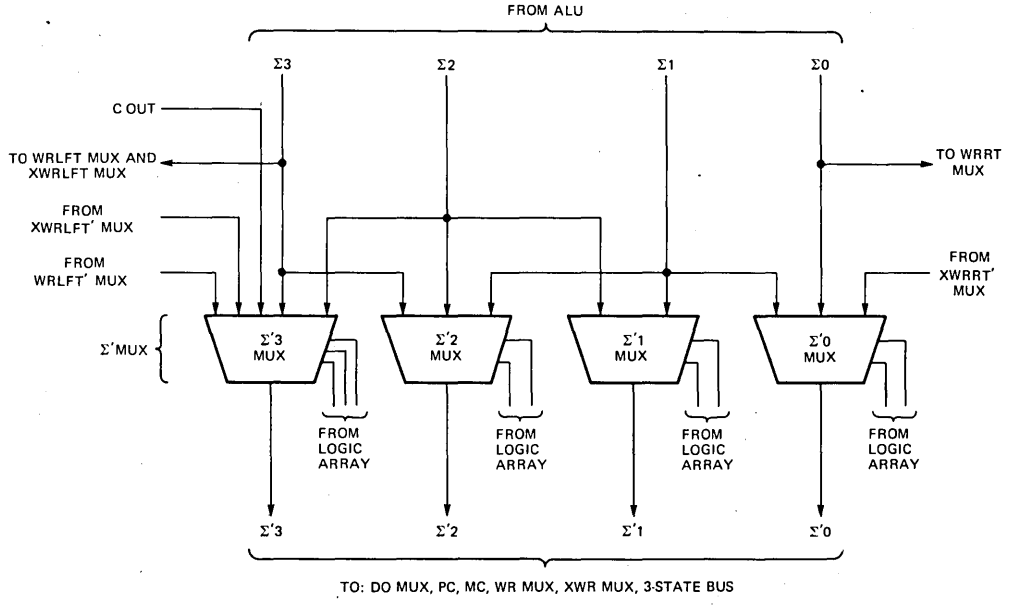


FIGURE 8 – SUM BUS MULTIPLEXER

Full sign protection and fill-in is provided in the MSP and LSP under control of the relative position inputs.

Information on the Σ' bus can be accessed during some operations through the 3-state Σ' bus control buffer at the B input/output port.

The parallel data input ports and the I/O capability of the B port, combined with the Σ-bus access, provides considerable flexibility for performing simple shifts or combinations of operation-and-shift on data or operands resident in the external working memory locations.

2.10 B-INPUT/OUTPUT CONTROL

The B-input/output port is isolated from the sum' bus by a 3-state control buffer when the buffer outputs are at a high-impedance. Enabling the buffer routes the sum' bus data to the B-port. The low-current inputs of the B port latch minimizes loading effects, and the buffers can source 6.5 mA or sink 10 mA of drive current in the output mode. During the output mode, the 'bus data can be latched in the B input latch. Enabling or disabling is accomplished by the I/O control input. See Table 10 and Figure 9.

TABLE 10
B-INPUT/OUTPUT CONTROL

I/O CONTROL	I/O BUFFER OUTPUT
L	SUM' BUS DATA
H	HIGH-IMPEDANCE

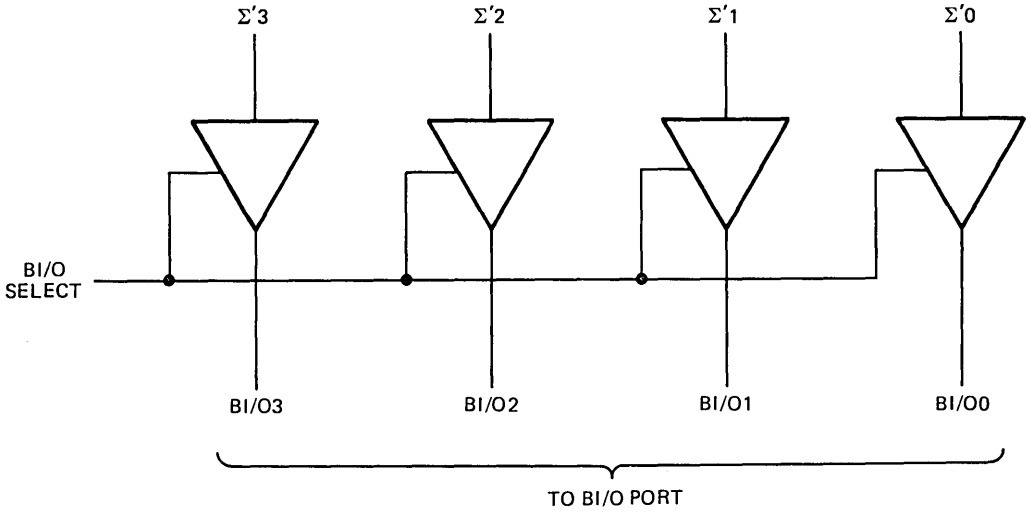


FIGURE 9 – B-INPUT/OUTPUT CONTROL

2.11 WORKING REGISTER

The working register (WR) is a 4-bit D-type register which functions as an accumulator during iterative arithmetic operations or as a temporary holding register for intermediate operands (see Figure 10). It is sourced by the WR multiplexer. Storage of setup data, under control of the resident operation forms which permit the WR to be a destination, occurs on the positive transition of the clock. WR shifting capabilities are implemented in the WR multiplexer. The working register can be selected to source the data-out port multiplexer (DO MUX), A-input multiplexer (A MUX), or B-input multiplexer (B MUX). The MSB of the WR is sourced to the WRLFT MUX, and the LSB of the WR is sourced to the WRRT MUX to facilitate expansion.

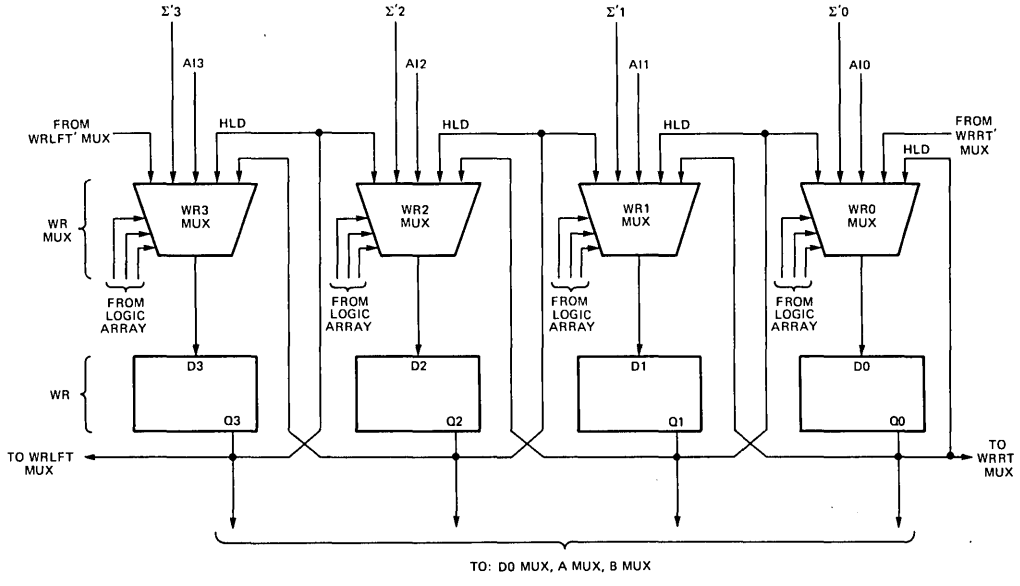


FIGURE 10 – WORKING REGISTER (WR) AND WR MULTIPLEXER

An asynchronous control line, $\overline{\text{LDWR}}$, is available to facilitate loading the working register directly from the A input port in combination with the resident micro-operation.

2.12 WORKING REGISTER MULTIPLEXER (WR MUX)

The working register multiplexer provides source selection, including the bidirectional shifting capability, for the working register. See Figure 10. Under direction of the resident operation, the WR MUX asynchronously selects either:

a. A input port for direct loading
b. Σ' bus for ALU operand results

c. Hold mode for no change
d. Shift left
e. Shift right

End conditions for both shift left and shift right operations are routed to or from WR MSB (WR3) or WRLSB (WR0) to the WRLFT/WRLFT' multiplexers or to the WRRT/WRRT' multiplexers respectively.

2.13 EXTENDED WORKING REGISTER

The extended working register (XWR) is a 4-bit D-type register which functions primarily as an extension of the working register to provide the double-precision operation capabilities needed for iterative multiply and divide routines (see Figure 11). Additionally, the storage capabilities of the XWR are available for use as another temporary holding register for intermediate operands during a number of the single-precision operation forms. It is sourced by the XWR multiplexer. Storage of setup data, under control of resident operation forms which permit the XWR to be a destination, occurs on the positive transition of the clock. XWR shifting capabilities are implemented in the XWR multiplexer. The XWR can be selected to source the data-out port multiplexer (DO MUX), B-input multiplexer (B MUX), or the XWR multiplexer (XWR MUX). The MSB of the XWR is sourced to the XWRLFT' MUX, and the LSB of the XWR is sourced to the XWRRT' MUX to facilitate expansion.

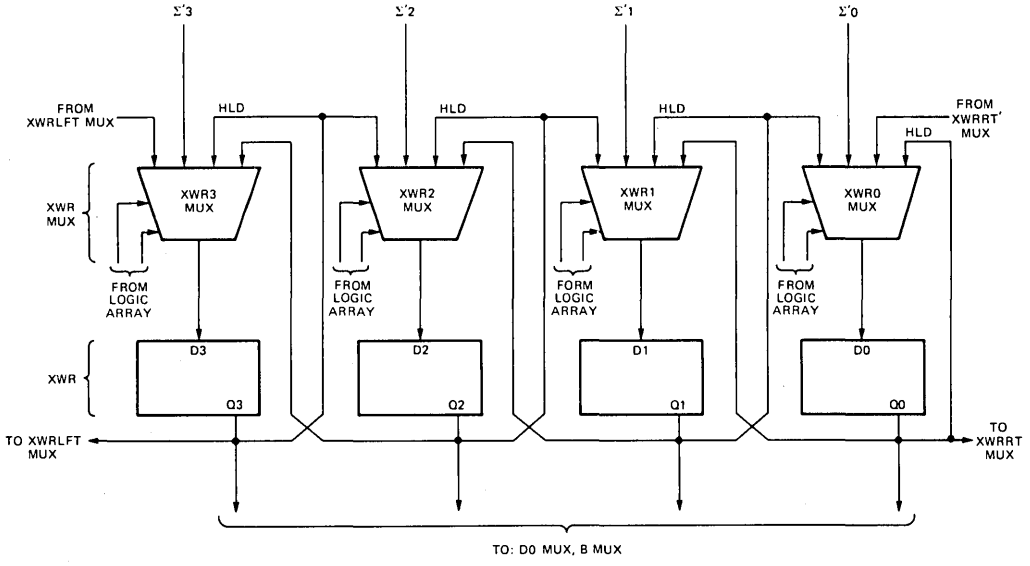


FIGURE 11 – EXTENDED WORKING REGISTER (XWR) AND XWR MULTIPLEXER

2.14 EXTENDED WORKING REGISTER MULTIPLEXER (XWR MUX)

The extended working register multiplexer provides source selection, including the bidirectional shifting capability, for the extended working register (see Figure 11). Under direction of the resident operation, the XWR MUX asynchronously selects either:

a. Σ' bus for ALU operand results
b. Hold mode for no change

c. Shift left
d. Shift right.

End conditions for both shift left and shift right operations are routed to or from XWR MSB (XWR3) or XWR LSB (XWR0) to the XWRLFT/XWRLFT' multiplexers or to the XWRRT/XWRRT' multiplexers respectively.

2.14.1 Σ-Bus, WR, XWR MSB Shift Transfer Multiplexers

The MSB shift transfers are accomplished by the WRLFT, XWRLFT input/output multiplexers and the WRLFT', XWRLFT' sum-bus/register MSB input multiplexers. All four multiplexers, and the impedance of the 3-state I/O lines of the WRLFT and XWRLFT multiplexer outputs are under control of the resident operation code and the relative position control (POS). Data paths of the multiplexers are illustrated in Figure 12, and bit transfers with respect to each of the shift operations are enumerated in Tables 11 through 14.

2.14.2 WRLFT, XWRLFT Multiplexers

The WRLFT, XWRLFT input/output multiplexers facilitate routing of the working register, extended working register, or sum bus MSB out the WRLFT, XWRLFT I/O's during output modes. In an input mode, the three-state output is at a high impedance permitting the WRLFT and/or the XWRLFT pins to be used as inputs.

2.14.3 WRLFT', XWRLFT' Multiplexers

The WRLFT' multiplexer selects the source for either the sum bus or working register MSB. Sign bit protection and right-shift bit-fill functions are all handled on-chip by these multiplexers under control of the operation code and relative position. The WRLFT' sources are:

a. WRLFT (input)
b. ALU carry out (for sign-fill)
c. Low level (for zero-fill)
d. XWRLFT input
e. XWR MSB
f. WR MSB (sign-fill in for RSA)
g. Sign fill in for RSA (see Figure 12)

The XWRLFT multiplexer selects the source for XWR MSB and provides sign-bit protection and right-shift-fill functions for the XWR. The XWRLFT sources are:

a. XWRLFT (input)
b. WRLFT
c. XWR MSB (sign-fill in for RSA)

2.14.4 WR, XWR LSB Shift Transfer Multiplexers

The LSB shift transfers are accomplished by the WRRT, XWRRT input/output multiplexers and the WRRT', XWRRT' sum-bus/register LSB input multiplexers. All four multiplexers, and the impedance of the 3-state I/O lines of the WRRT and XWRRT multiplexer outputs, are under control of the resident operation code and the relative position control (POS). Data paths of the multiplexers are illustrated in Figure 13.

2.14.5 WRRT Multiplexer, XWRRT Buffer

The WRRT input/output multiplexer facilitates routing of sum-bus or working register LSB out the WRRT I/O during output modes. The XWRRT I/O buffer can access and source the XWR LSB. In an input mode, the three-state output is at a high impedance permitting the WRRT and/or XWRRT pins to be used as inputs.

2.14.6 WRRT', XWRRT' Multiplexers

The WRRT' multiplexer selects either the WRRT input or a low logic level (fill) input as the LSB source for either the working register or the sum-bus. The XWRRT' multiplexer selects between the XWRRT input and low logic level (fill) input as the XWR LSB source.

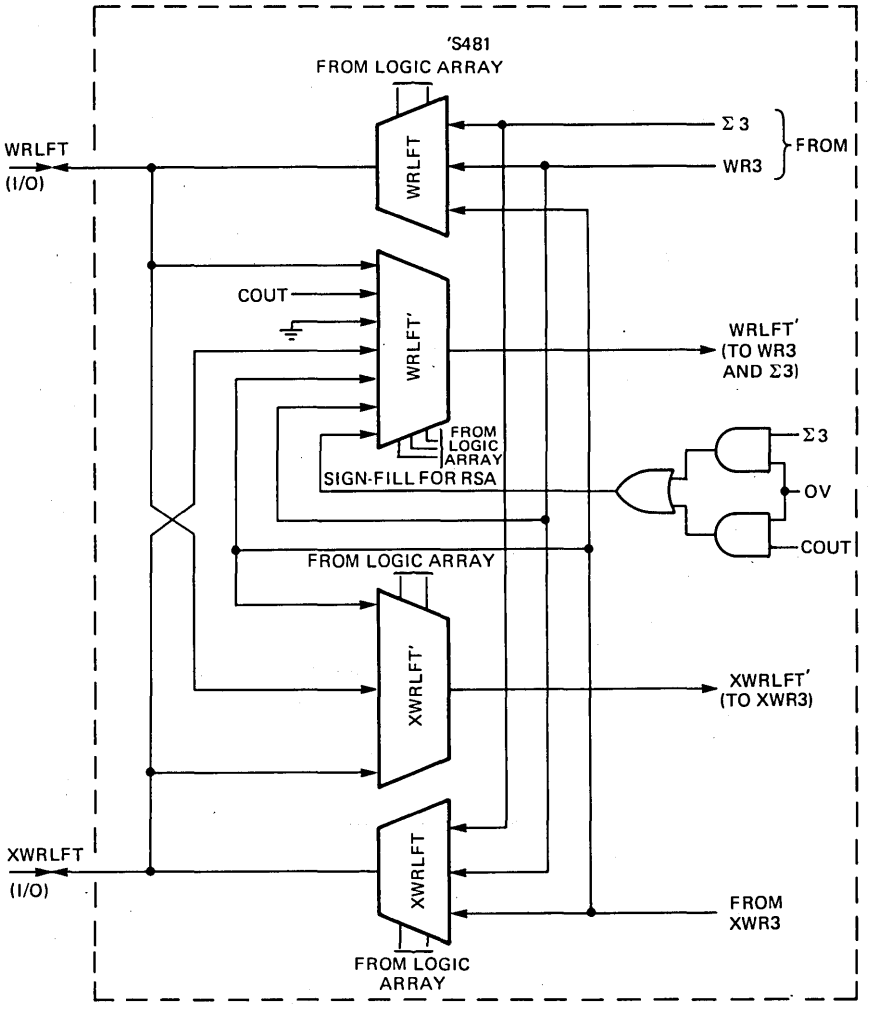


FIGURE 12 – SUM-BUS, WR, XWR MSB SHIFT TRANSFER MULTIPLEXERS

TABLE 11
WORKING REGISTER BIT TRANSFERS TO WRLFT/WRRT

SHIFT MODE	MOST-SIGNIFICANT POSITION				INTERMEDIATE POSITION				LEAST-SIGNIFICANT POSITION			
	WRLFT	WRLFT'	WRRT'	WRRT	WRLFT	WRLFT'	WRRT'	WRRT	WRLFT	WRLFT'	WRRT'	WRRT
LSL (SP)	Z	X	WRRT	Z	WR3	X	WRRT	Z	WR3	X	WRRT	Z
LSL (DP)	XWR3	X	WRRT	Z	WR3	X	WRRT	Z	WR3	X	WRRT	Z
LSA (SP)	WR3	X	WRRT	Z	WR3	X	WRRT	Z	WR3	X	L	Z
LSA (DP)	XWR3	X	WRRT	Z	WR3	X	WRRT	Z	WR3	X	WRRT	Z
LCIR (SP)	WR3	X	WRRT	Z	WR3	X	WRRT	Z	WR3	X	WRRT	Z
LCIR (DP)	XWR3	X	WRRT	Z	WR3	X	WRRT	Z	WR3	X	WRRT	Z
RSL (SP)	Z	WRLFT	X	WR0	Z	WRLFT	X	WR0	Z	WRLFT	X	Z
RSL (DP)	Z	L	X	WR0	Z	WRLFT	X	WR0	Z	WRLFT	X	WR0
RSA (SP)	Z	WR3	X	WR0	Z	WRLFT	X	WR0	Z	WRLFT	X	WR0
RSA (DP)	Z	WR3	X	WR0	Z	WRLFT	X	WR0	Z	WRLFT	X	WR0
RCIR (SP)	Z	WRLFT	X	WR0	Z	WRLFT	X	WR0	Z	WRLFT	X	WR0
RCIR (DP)	Z	WRLFT	X	WR0	Z	WRLFT	X	WR0	Z	WRLFT	X	WR0

TABLE 12
SUM-BUS BIT TRANSFERS TO WRLFT/WRRT

SHIFT MODE	MOST-SIGNIFICANT POSITION				INTERMEDIATE POSITION				LEAST-SIGNIFICANT POSITION			
	WRLFT	WRLFT'	WRRT'	WRRT	WRLFT	WRLFT'	WRRT'	WRRT	WRLFT	WRLFT'	WRRT'	WRRT
LSL (SP)	Z	X	WRRT	Z	Σ3	X	WRRT	Z	Σ3	X	WRRT	Z
LSL (DP)	XWR3	X	WRRT	Z	Σ3	X	WRRT	Z	Σ3	X	WRRT	Z
LSA (SP)	Σ3	X	WRRT	Z	Σ3	X	WRRT	Z	Σ3	X	L	Z
LSA (DP)	XWR3	X	WRRT	Z	Σ3	X	WRRT	Z	Σ3	X	WRRT	Z
LCIR (SP)	Σ3	X	WRRT	Z	Σ3	X	WRRT	Z	Σ3	X	WRRT	Z
LCIR (DP)	XWR3	X	WRRT	Z	Σ3	X	WRRT	Z	Σ3	X	WRRT	Z
RSL (SP)	Z	WRLFT	X	Σ0	Z	WRLFT	X	Σ0	Z	WRLFT	X	Σ0
RSL (DP)	Z	C-OUT	X	Σ0	Z	WRLFT	X	Σ0	Z	WRLFT	X	Σ0
RSA (SP)	Z	*	X	Σ0	Z	WRLFT	X	Σ0	Z	WRLFT	X	Σ0
RSA (DP)	Z	*	X	Σ0	Z	WRLFT	X	Σ0	Z	WRLFT	X	Σ0
RCIR (SP)	Z	WRLFT	X	Σ0	Z	WRLFT	X	Σ0	Z	WRLFT	X	Σ0
RCIR (DP)	Z	XWRLFT	X	Σ0	Z	WRLFT	X	Σ0	Z	WRLFT	X	Σ0

*VARIABLE = (Σ3 • ALU OVERFLOW) + (C-OUT • ALU OVERFLOW)

TABLE 13
EXTENDED WORKING REGISTER BIT TRANSFERS TO XWRLFT/XWRRT

SHIFT MODE	MOST-SIGNIFICANT POSITION				INTERMEDIATE POSITION				LEAST-SIGNIFICANT POSITION			
	XWRLFT	XWRLFT'	XWRRT'	XWRRT	XWRLFT	XWRLFT'	XWRRT'	XWRRT	XWRLFT	XWRLFT'	XWRRT'	XWRRT
LSL (SP)	Z	X	XWRRT	Z	XWR3	X	XWRRT	Z	XWR3	X	XWRRT	Z
LSL (DP)	Z	X	XWRRT	Z	XWR3	X	XWRRT	Z	XWR3	X	XWRRT	Z
LSA (SP)	XWR3	X	XWRRT	Z	XWR3	X	XWRRT	Z	XWR3	X	L	Z
LSA (DP)	WR3	X	XWRRT	Z	XWR3	X	XWRRT	Z	XWR3	X	L	Z
LCIR (SP)	XWR3	X	XWRRT	Z	XWR3	X	XWRRT	Z	XWR3	X	XWRRT	Z
LCIR (DP)	WR3	X	XWRRT	Z	XWR3	X	XWRRT	Z	XWR3	X	XWRRT	Z
RSL (SP)	Z	XWRLFT	X	XWR0	Z	XWRLFT	X	XWR0	Z	XWRLFT	X	Z
RSL (DP)	Z	WRLFT	X	XWR0	Z	XWRLFT	X	XWR0	Z	XWRLFT	X	XWR0
RSA (SP)	Z	XWR3	X	XWR0	Z	XWRLFT	X	XWR0	Z	XWRLFT	X	XWR0
RSA (DP)	Z	WRLFT	X	XWR0	Z	XWRLFT	X	XWR0	Z	XWRLFT	X	XWR0
RCIR (SP)	Z	XWRLFT	X	XWR0	Z	XWRLFT	X	XWR0	Z	XWRLFT	X	XWR0
RCIR (DP)	Z	WRLFT	X	XWR0	Z	XWRLFT	X	XWR0	Z	XWRLFT	X	XWR0

TABLE 14
SUM-BUS BIT TRANSFERS TO XWRLFT (MSP)

SHIFT MODE	MOST-SIGNIFICANT POSITION XWRLFT	XWRLFT'	XWRRT'	XWRRT
LSL (SP)	Z	X	XWRRT	Z
LSL (DP)	Z	X	XWRRT	Z
LSA (SP)	XWR3	X	XWRRT	Z
LSA (DP)	Σ3	X	XWRRT	Z
LCIR (SP)	XWR3	X	XWRRT	Z
LCIR (DP)	Σ3	X	XWRRT	Z
RSL (SP)	Z	XWRLFT	X	XWR0
RSL (DP)	Z	WRLFT	X	XWR0
RSA (SP)	Z	XWR3	X	XWR0
RSA (DP)	Z	WRLFT	X	XWR0
RCIR (SP)	Z	XWRLFT	X	XWR0
RCIR (DP)	Z	WRLFT	X	XWR0

NOTE: Intermediate and Least-Significant Positions are the same as shown in Table 13.

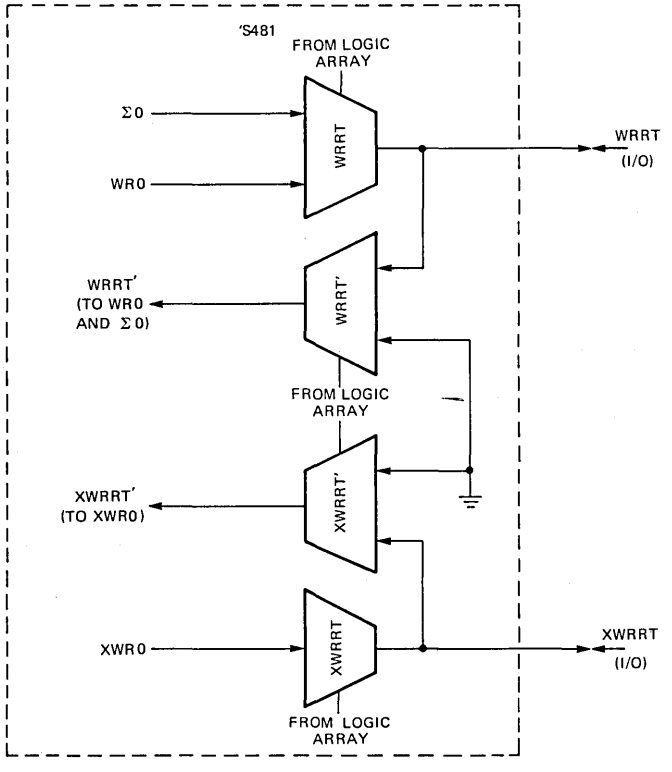


FIGURE 13 – SUM-BUS, WR, XWR LSB SHIFT TRANSFER MULTIPLEXERS

2.15 SHIFT FUNCTIONS

The 'S481 contains the necessary controls and data paths to perform single or double length logical, arithmetic, or circulate bidirectional shift functions in a single clock cycle. Each of the six shift functions implemented are selectable by a single microinstruction; and, additionally two single clock operation forms are included which provide the capability of performing an add/subtract in conjunction with a shift. The six shift functions and the basic operation forms offering them are enumerated in Table 15.

TABLE 15
MICROPROGRAMMABLE SHIFT FUNCTIONS

FUNCTION	OPERATION FORMS			
	SIMPLE SHIFT		ADD/SUBTRACT WITH SHIFT	
	SINGLE LENGTH	DOUBLE LENGTH	SINGLE LENGTH	DOUBLE LENGTH
LEFT CIRCULATE (LCIR)	IV, V	VI		
LEFT SHIFT ARITHMETIC (LSA)	IV, V	VI	III	
LEFT SHIFT LOGICAL (LSL)	IV, V	VI	III	II
RIGHT CIRCULATE (RCIR)	IV, V	VI		
RIGHT SHIFT ARITHMETIC (RSA)	IV, V	VI	III	
RIGHT SHIFT LOGICAL (RSL)	IV, V	VI	III	II

2.15.1 CIRCULATE (SHIFT) FUNCTIONS (MICROPROGRAMMABLE)

Operation forms IV and V provide the system designer with the capability of programming a single precision circulate (or rotate) of the Σ' bus, working register, or extended working register and operation form VI provides the capability of circulating or rotating a double-length word resident in the WR/XWR. A single-bit-position left or right circulate is accomplished on each clock without the loss of any bits as the shift transfer multiplexers, under control of the resident operation and position input, interconnect the bus or register as illustrated in Figure 14.

The remaining end conditions are handled on chip by the shift transfer multiplexers to interconnect the bit transfer mechanisms for MSB → LSB for single precision circulates and for transfers to or from the Σ' bus or working register and the extended working register during double-precision circulates. Data flow between packages in an expanded word-length system is via the interconnected WRRT/WRLFT and XWRRT/XWRLFT terminals.

2.15.2 ARITHMETIC SHIFT FUNCTIONS (MICROPROGRAMMABLE)

Operation forms III, IV, V and VI provide the system designer with the capability of programming the following arithmetic shifts.

Form III – A single-precision arithmetic left or sign-protected right shift of the sum or difference of the A and B operands destined for either the WR or XWR.

Form IV – A single-precision arithmetic left or sign-protected right shift of the A operand destined for the Σ' bus.

Form V – A single-precision arithmetic left or sign-protected right shift of the WR or XWR contents.

Form VI – A double-precision arithmetic left or sign-protected right shift of the WR and XWR contents.

SN74S481 4-BIT-SLICE SCHOTTKY PROCESSOR ELEMENT

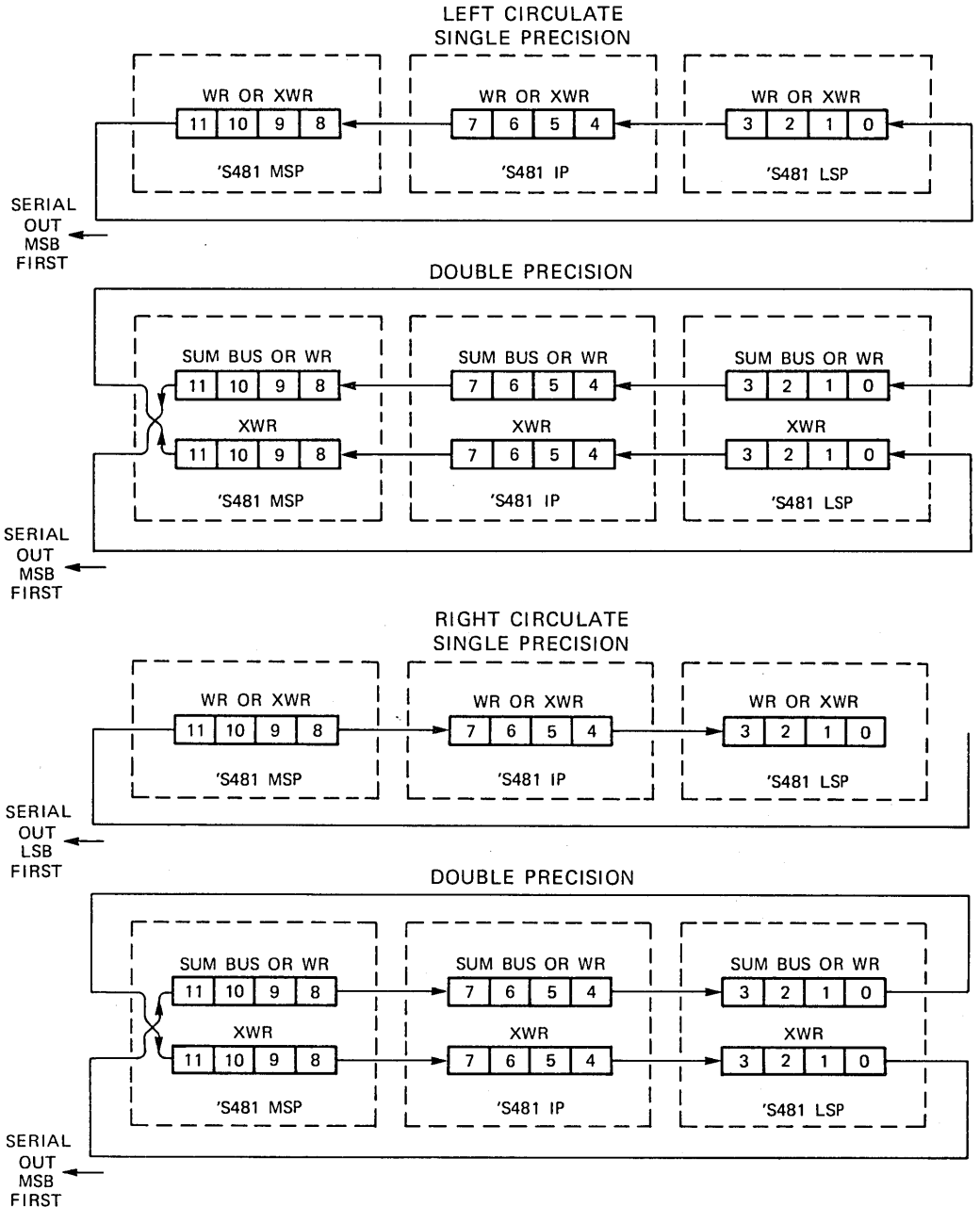


FIGURE 14 – CIRCULATE FUNCTIONS

A single-bit-position shift is accomplished on each clock with right-shift sign-protection and left shift LSB zero-fill operations controlled by the shift transfer multiplexers under direction of the resident operation and the position input. See Figure 15.

The remaining end conditions are handled on chip by the shift transfer multiplexers to interconnect the bit transfer mechanisms for transfers to or from the Σ' bus or working register and the extended working register during double-precision arithmetic shifts. Data flow between packages in an expanded word-length system is via the interconnected WRRT/WRLFT and XWRRT/XWRLFT terminals.

2.15.3 LOGICAL SHIFT FUNCTIONS (MICROPROGRAMMABLE)

Operation Forms II, III, IV, V and VI provide the system designer with the capability of programming the following logical shifts:

Form II – A double-precision left or right shift of the sum or difference of the A and B operands destined for the WR in conjunction with the XWR.

Form III – A single-precision left or right logical shift of the sum or difference of the A and B operands destined for the WR or the XWR.

Form IV – A single-precision left or right logical shift of the A operand destined for the Σ' bus.

Form V – A single-precision left or right logical shift of the WR or XWR contents.

Form VI – A double-precision left or right logical shift of the WR and XWR contents.

A single-bit-position shift is accomplished on each clock with MSB and LSB fill operations controlled by the shift transfer multiplexers under direction of the resident operation and the position input. See Figure 16.

The remaining end conditions are handled on chip by the shift transfer multiplexers to interconnect the bit transfer mechanisms for transfers to and from the Σ' bus or working register and the extended working register during double-precision logical shifts. Data flow between packages in an expanded word length system is via the interconnected WRRT/WRLFT and XWRRT/XWRLFT terminals.

2.16 DATA-OUT PORT MULTIPLEXER (DO MUX)

The data-out port multiplexer, Figure 17, provides selection for routing the contents of either the sum'-bus, working register, or extended working register to the parallel output port. Additionally, the multiplexer is equipped with 3-state outputs providing the capability to isolate the 'S481 from the system data bus. Source selections and high-impedance controls are detailed in Table 16.

Each data output is capable of sourcing 6.5 and sinking 10 milliamperes of drive current.

2.17 MEMORY AND PROGRAM COUNTERS

Dual counters provide the system designer with a processor element containing both an iteration counter and the capability of generating and/or storing locations of operands/data.

Either counter can be loaded or preset to any value or result from the sum bus in operations forms as follows:

	SELECTABLE AS DESTINATION	
OP FORM	PC	MC
I	Yes	Yes
III	No	Yes
VIII	Yes	No

SN54S481/SN74S481 4-BIT-SLICE SCHOTTKY PROCESSOR ELEMENT

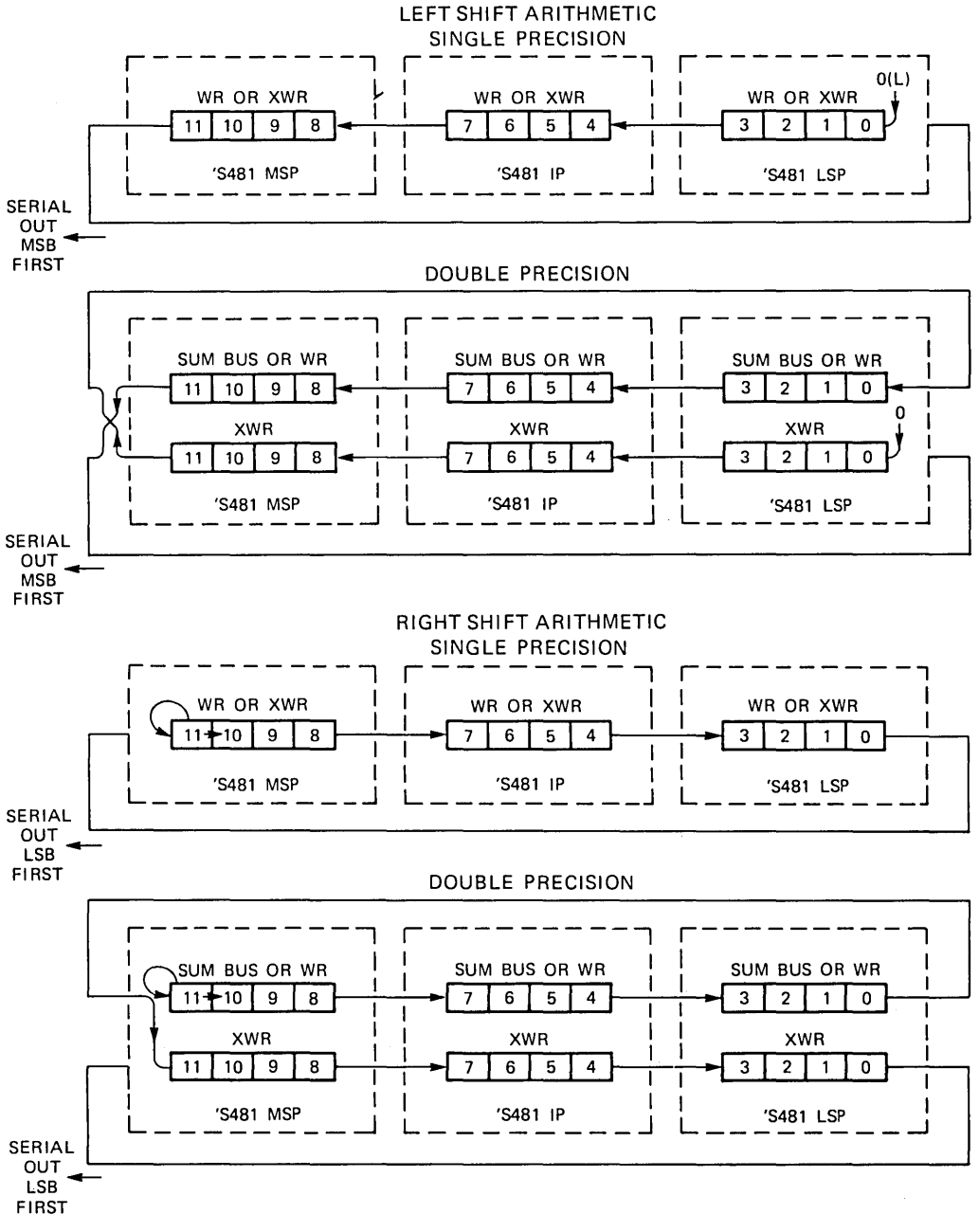


FIGURE 15 – ARITHMETIC SHIFT FUNCTIONS

SN54S481/SN74S481 4-BIT-SLICE SCHOTTKY PROCESSOR ELEMENT

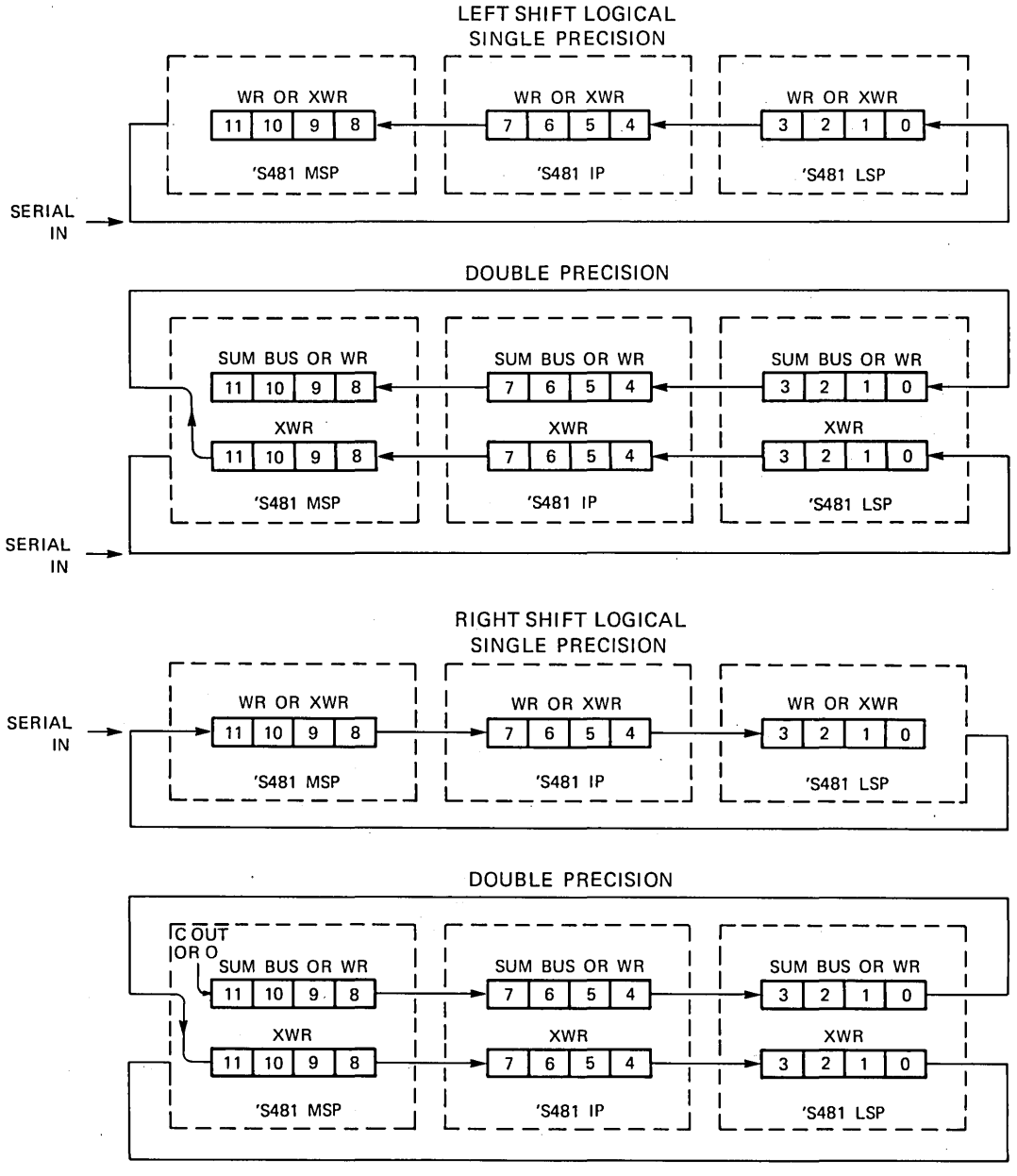


FIGURE 16 – LOGICAL SHIFT FUNCTIONS

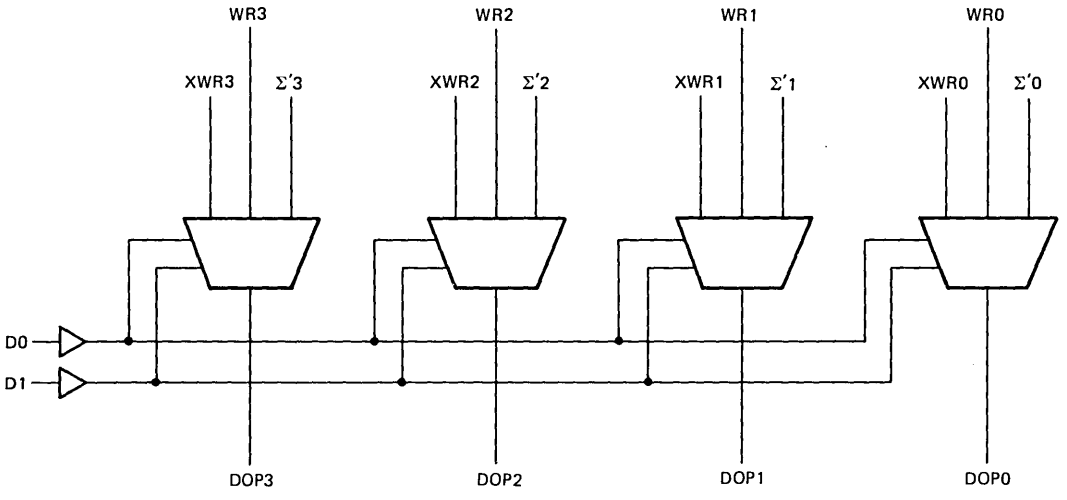


FIGURE 17 – DATA-OUT PORT MULTIPLEXER (DO MUX)

Under control of the position (POS) input and the resident operation code, the $\overline{CCO}$/OV output facilitates cascading the program and memory counters. In the least-significant and intermediate positions, the $\overline{CCO}$ pins of lesser significant packages are connected to the $\overline{CCI}$ pins of more significant packages to complete the counter interconnections to the bit-size of the processor element.

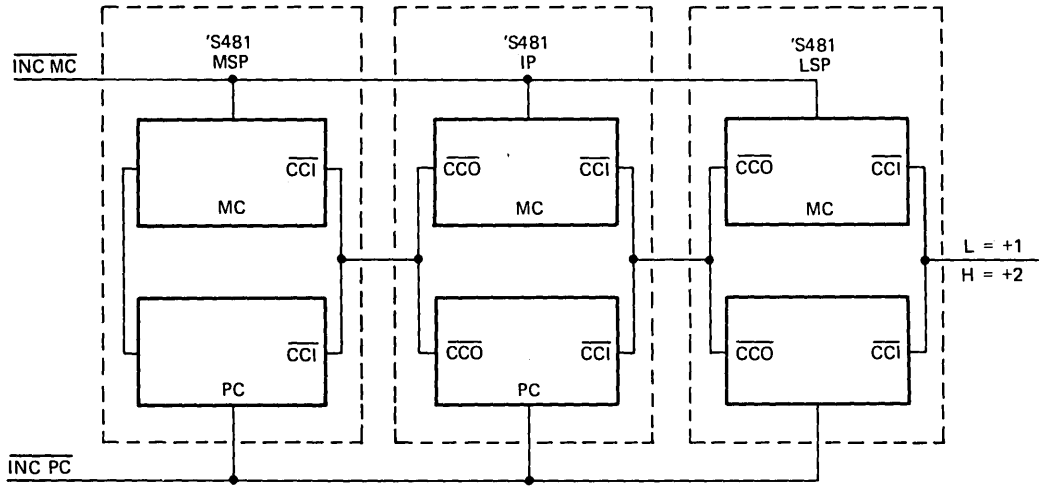
TABLE 16
DATA-OUT PORT CONTROL

CONTROL INPUTS		SOURCE OR FUNCTION
D1	D0	
L	L	Σ'-BUS
L	H	EXTENDED WORKING REGISTER
H	L	WORKING REGISTER
H	H	HIGH-IMPEDANCE

The functionally identical program and memory counters, sharing a common counter carry input ($\overline{CCI}$) control pin and a common counter carry output ($\overline{CCO}$) pin, feature individual control lines ($\overline{INC\ PC}$, $\overline{INC\ MC}$) which can be used to instruct either (but normally not both) or neither counter to increment on the next clock transition in any of the 14 operation forms. Additionally, the counter in the LSP, under command of the POS input, has the capability of incrementing its value by one or by two to facilitate the generation of even or odd address locations in a single clock cycle. Contents of the counters can be read out from the address out port asynchronously under control of the address output multiplexer (AO MUX) select input.

Typical counter functions with respect to package relative positions are shown in Figure 18.

In the MSP, the $\overline{CCO}$/OV output, as a result of the position (POS) control, becomes the ALU/shift overflow (OV) status output.



INPUTS			CK	COUNTER VALUE			
INC PC	INC MC	CCI		LSP MC	LSP PC	MSP, IP MC	MSP, IP PC
H	H	X	↑	NO CHG	NO CHG	NO CHG	NO CHG
L	H	L	↑	NO CHG	+1	NO CHG	+1
L	H	H	↑	NO CHG	+2	NO CHG	NO CHG
H	L	L	↑	+1	NO CHG	+1	NO CHG
H	L	H	↑	+2	NO CHG	NO CHG	NO CHG
X	X	X	L	NO CHG	NO CHG	NO CHG	NO CHG
X	X	X	H	NO CHG	NO CHG	NO CHG	NO CHG

H=HIGH LEVEL, L=LOW LEVEL, X=IRRELEVANT, ↑=LOW-TO-HIGH TRANSITION

FIGURE 18 – PROGRAM AND MEMORY COUNTER FUNCTIONS

2.18 ADDRESS-OUT PORT MULTIPLEXER (AO MUX)

The address-out port multiplexer, Figure 19, provides for direct parallel access to the contents of either the program or memory counter contents. A single line controls selection as shown in Table 17.

TABLE 17
ADDRESS-OUT PORT CONTROL

CONTROL INPUT A0	COUNTER SELECTED
L	MEMORY
H	PROGRAM

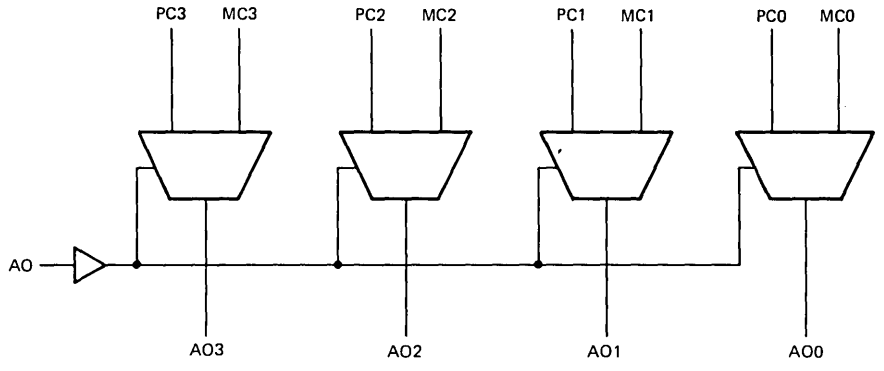


FIGURE 19 – ADDRESS-OUT PORT MULTIPLEXER (AO MUX)

2.19 EXPANDING THE WORD LENGTH

The 'S481 processor element contains on-chip personality circuitry designed specifically to minimize the external discrete components required to cascade 4-bit slices to form larger word lengths. At the processor-element level, three external resistors are all that is required: one to pull-up the open-collector outputs and two to establish the position control input voltage at the LSP. Figure 20 shows a typical 16-bit processor element and illustrates the parallel bus arrangements for I/O and control with an SN74S182 performing ALU look-ahead across the 16-bit word. Interconnectivity for the shift, arithmetic, and counter functions is accomplished by hardwiring the functions as shown.

At the system level, standard techniques commonly employed for power-supply bypass, termination of unused pins, and system grounding of high-performance Schottky TTL systems are recommended.

3. OPERATIONAL DESCRIPTIONS

3.1 MICRO/MACRO-OPERATIONS

The micro/macro-operations resident in the micro-decode logic array can be accessed with an eleven-bit operation-select word. Operational flexibility is maximized by the fact that the op-select word format has been defined individually for each of the 14 different operation forms.

Operation Forms I, II, and III are primarily ALU functions. Forms II and III combine logical or arithmetic shifting functions with the ALU result. Form II can be used for double-precision shifting. Sources, specific ALU function, shift format, and destinations are detailed for each op-select word format.

Forms IV, V, and VI perform either logical or arithmetic, bidirectional shifting of the single- and double-precision buses and registers.

Form VII can be used to compare the magnitude of A source to B source, or B source to A source.

Form VIII provides the capability to logically combine the values of the A and B sources.

Form IX zeros the Σ' bus with the effect of providing no operation.

Forms X through XIV are macroprogrammable operations which provide:

a. CRC partial sum update (normally $\frac{N}{2}$ clocks)
b. Signed Divide (N + 3 clocks)
c. Unsigned Divide (N + 1 clocks)
d. N-bit-by-N-bit double-precision unsigned multiply (N clocks)
e. N-bit-by-N-bit double-precision signed multiply (N clocks)

The 14 operation forms, symbols, and number of unique operations are detailed in Table 18.

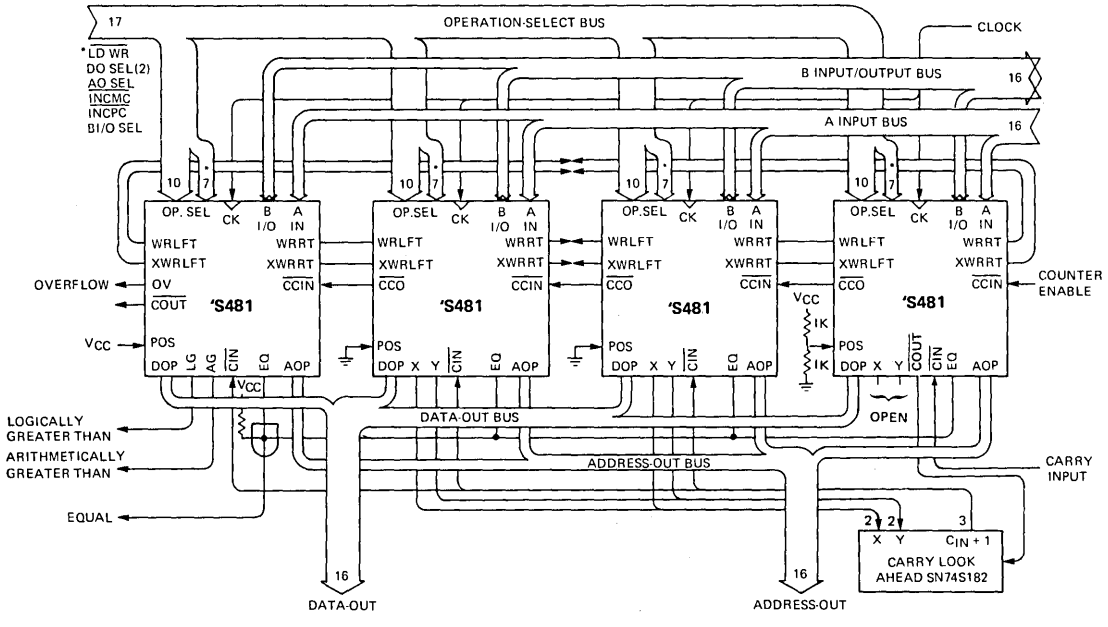


FIGURE 20—TYPICAL 16-BIT PROCESSOR

TABLE 18 – OPERATION FORM, COMMAND FORMAT, AND TEST OUTPUTS

OPERATION FORM		COMMAND FORMAT											TEST OUTPUTS							
													MSP		ALL		$\overline{MSP}$		MSP	$\overline{MSP}$
NO.	OPERATION	OP0 (7)[1]	OP1 (8)	OP2 (9)	OP3 (10)	OP4 (17)	OP5 (14)	OP6 (13)	OP7 (11)	OP8 (15)	OP9 (16)	LSP $\overline{CIN}$ (18)	LG (21)	AG (20)	EQ (23)	$\overline{C\text{-}OUT}$ (22)	X (21)	Y (20)	OVFL (37)	$\overline{CCO}$ (37)
IA	(±A ±B + $\overline{CIN}$) → Σ' BUS ONLY[2]	H	L	L	A SOURCE		B SOURCE			A' FNCT	B' FNCT	L = CARRY H = NO CARRY	Σ'≠ZERO	Σ'>ZERO	Σ'=ZERO	$\overline{C\text{-}OUT}$	X[4]	Y[4]	OVFL	$\overline{CCO}$
IB	(±A ±B + $\overline{CIN}$) → REGISTER	L	REGISTER LL = Σ' → WR LH = Σ' → XWR HL = Σ' → PC HH = Σ' → MC		LL = AI → A LH = H'S → A HL = BI → A HH = WR → A		LLL = BI → B LLH = H'S → B LHL = BI + WR → B LHH = WR → B HLL = BI • XWR → B HLH = XWR → B HHL = BI • PC → B HHH = PC → B			L = A → A' H = $\overline{A}$ → A'	L = B → B' H = $\overline{B}$ → B'									
IIA	(A + B + $\overline{CIN}$) ↠ WR, XWR[2]	H	H	H	L	H	L	FUNCT L = A → A' H = $\overline{A}$ → A'	B' SRC L=BI→B' H=WR→B'	A' SRC L = AI → A' H = BI → A'	SHIFT L = LFT H = RT	L = SUB H = ADD	Σ'≠ZERO	Σ'>ZERO	Σ'=ZERO	$\overline{C\text{-}OUT}$	X	Y	OVFL	$\overline{CCO}$
IIB	(B − A − 1) ↠ WR, XWR	H	H	H	L	H	L													
III	(A + B + $\overline{CIN}$) ↠ REGISTER	H	H	L	H	A' SRC L = AI → A' H = BI → A'	REGISTER L = Σ' → MC H = Σ' → XWR	B' SOURCE LL = BI → B' LH = WR → B' HL = XWR → B' HH* = L'S → B'		SHIFT L = LOG H = *ARITH	TYPE L = LFT H = RT	L = CARRY H = NO CARRY	Σ'≠ −1	Σ'> −1	Σ' = −1	$\overline{C\text{-}OUT}$	X	Y	OVFL SHIFT OVFL	$\overline{CCO}$
IV	AI ↠ Σ' BUS	H	H	H	L	H	H	REG OR AI LL = AI ↠ Σ'		SHIFT LL = LOG LH = ARITH HL = ROTATE HH (NOT DEFINED)		TYPE L = LFT H = RT	AI≠ZERO	AI>ZERO	AI=ZERO	$\overline{CIN}$	X	Y	L (FOR LSA OVFL)	$\overline{CCO}$
VA	WR ↠ WR	H	H	H	L	H	H	LH = WR ↠ WR												
VB	XWR ↠ XWR	H	H	H	L	H	H	HL = XWR ↠ XWR												
VI	WR, XWR ↠ WR, XWR	H	H	H	L	H	H	HH=WR,XWR→WR,XWR												
VIIA	A:B (N1:N2)	H	H	H	L	L	B' SOURCE (SAME AS FORM I ABOVE)			A' SRC L = AI→A' H = WR→A'	OPER L = A:B H = B:A	H	N1>N2	N1>N2	N1=N2	=LG	X	Y	–	$\overline{CCO}$
VIIB	B:A (N1:N2)	H	H	H	L	L														
VIIIA	NOR/AND LOGICAL OPERATIONS	H	FUNCTION LHL = NOR			A' SRC L=AI→A H=WR→A	REG[3] LL = WR	B SOURCE LL = BI → B		A' FNCT L = A → A' H = $\overline{A}$ → A'	B' FNCT L=B→B' H= $\overline{B}$ → B'	REG[3] (SEE UNDER OP5 COLUMN)	Σ'≠ZERO	Σ'>ZERO	Σ'=ZERO	=$\overline{CIN}$	X	Y	L	$\overline{CCO}$
VIIIB	OR/NAND LOGICAL OPERATIONS	H	LHH = OR				LH = XWR	LH = WR → B												
VIIIC	EX OR/EX NOR LOGICAL OPERATIONS	H	HLL = XOR				HL = PC	HL = XWR → B												
							HH = Σ'	HH = PC → B												
IX	NO OPERATION (ZERO → Σ' BUS)	H	H	H	H	H	H or L	H or L	H or L	H or L	H or L	H or L	L	L	H	=$\overline{CIN}$	X	Y	L	$\overline{CCO}$
X	CRC ACCUMULATION	H	H	H	H	L	L	L	L	L	O/I[5]	H	–	–	–	–	X	Y	L	$\overline{CCO}$
XI	SIGNED INTEGER DIVIDE A. START	H	H	H	H	L	L	H	L	H	H	H	–	–	DIV=ZERO	–	–	–	–	–
	B. ITERATE (N-1 CLKS)	H	H	H	H	L	H	L	H	O/I[6]	O/I[6]	H	–	–	–	–	–	–	–	–
	C. ITERATE FINISH	H	H	H	H	L	H	H	L	O/I[6]	O/I[6]	H	–	–	–	–	–	–	–	–
	D. FIX REMAINDER	H	H	H	H	L	H	L	L	O/I[6]	O/I[6]	H	–	–	–	–	–	–	–	–
	E. ADJUST QUOTIENT	H	H	H	H	L	L	H	H	O/I[6]	O/I[6]	H	–	–	–	–	–	–	–	–
XII	UNSIGNED DIVIDE A. START	H	H	H	H	L	L	L	L	H	H	L	–	DIV OVFL	–	–	–	–	–	–
	B. ITERATE (N-1 CLKS)	H	H	H	H	L	L	L	H	H	O/I[6]	L	–	–	–	–	–	–	–	–
	C. FINISH	H	H	H	H	L	L	L	H	L	O/I[6]	L	–	–	–	–	–	–	–	–
XIII	UNSIGNED MULTIPLY	H	H	H	H	L	L	H	L	L	O/I[6]	H	–	–	–	–	–	–	–	–
XIV	SIGNED INTEGER MULTIPLY	H	H	H	H	L	H	H	H	O/I[6]	O/I[6]	H	–	–	–	–	–	–	–	–

AO SEL (42)
- L MC
- H PC

DO1 SEL (29)
DO2 SEL (30)
- LL Σ' BUS
- LH WR
- HL XWR
- HH HI-Z

BI/O SEL (29)
- L OUTPUT
- H INPUT

$\overline{LD\ WR}$ (24)
- L AI → WR
- H NO LOAD

$\overline{INC\ MC}$ (35)
- L INC
- H HOLD

$\overline{INC\ PC}$ (43)
- L INC
- H HOLD

$\overline{CCI}$ (44)
- LSP L: x 1
- LSP H: x 2

MID OR MSP
- L CARRY
- H NO CARRY

POS (19)
- 0 V = MID
- 2.4 V = LSP
- 5 V = MSP

PIN NUMBER	DATA PORTS AI	BI/O	DOP	AOP	BIT (2^n)
	(6)	(46)	(34)	(38)	0 (LSB)
	(5)	(47)	(33)	(39)	1
	(4)	(1)	(32)	(40)	2
	(3)	(2)	(31)	(41)	3 (MSB)

PIN ASSIGNMENTS

WRRT (26)	CK (45)
WRLFT (25)	V_{CC} (12)
XWRRT (28)	GND (36)
XWRLFT (27)	

NOTES:
1. NUMERALS IN PARENTHESIS ARE PIN NUMBERS
2. → DESTINED FOR ↠ SHIFTED AND DESTINED FOR
3. H = HIGH VOLTAGE LEVEL, L = LOW VOLTAGE LEVEL
4. X AND Y ARE CARRY LOOK-AHEAD FUNCTIONS
5. O IS OUTPUT ON LSP, I IS INPUT ON $\overline{LSP}$
6. O IS OUTPUT ON MSP, I IS INPUT ON $\overline{MSP}$
7. VOLTAGE VALUES ARE NOMINAL

3.2 OPERATION FORM I – ADD/SUBTRACT → REGISTER

Operation Form I is designed specifically to perform the addition or symmetrial subtraction of two operands. The operation form shown in Figure 21, is composed of two distinct capabilities:

	OP0	OP3	OP4	OP8	OP5	OP6	OP7	OP9	$\overline{CIN}$	OP1	OP2
FORM IA	H	A2	A1	A0	B3	B2	B1	B0	C	L	L
FORM IB	L	A2	A1	A0	B3	B2	B1	B0	C	S1	S0

FORM IA: A PLUS B PLUS ALUCIN → Σ' BUS ONLY

FORM IB: A PLUS B PLUS ALUCIN → REGISTER

A-SOURCE SEL

A2	A1	A0	SEL
L	L	L	AI → A
L	L	H	$\overline{AI}$ → A
L	H	L	H → A
L	H	H	L → A
H	L	L	BI → A
H	L	H	$\overline{BI}$ → A
H	H	L	WR → A
H	H	H	$\overline{WR}$ → A

B-SOURCE SEL

B3	B2	B1	B0	SEL
L	L	L	L	BI → B
L	L	L	H	$\overline{BI}$ → B
L	L	H	L	H → B*
L	L	H	H	L → B*
L	H	L	L	BI · WR → B
L	H	L	H	$\overline{BI \cdot WR}$ → B
L	H	H	L	WR → B*
L	H	H	H	$\overline{WR}$ → B*
H	L	L	L	BI · XWR → B
H	L	L	H	$\overline{BI \cdot XWR}$ → B
H	L	H	L	XWR → B*
H	L	H	H	$\overline{XWR}$ → B*
H	H	L	L	BI · PC → B
H	H	L	H	$\overline{BI \cdot PC}$ → B
H	H	H	L	PC → B*
H	H	H	H	$\overline{PC}$ → B*

ACTIVE CARRY

$\overline{CIN}$ = H:
NO CARRY

$\overline{CIN}$ = L:
CARRY INPUT

REG. DESTINATION SEL

S1	S0	SEL
L	L	Σ' → WR
L	H	Σ' → XWR
H	L	Σ' → PC
H	H	Σ' → MC

ASYNCHRONOUS CONTROLS:

SEL B INPUT/OUTPUT*
SEL DOP SOURCE
SEL AOP SOURCE
INCREMENT PC OR MC
INHIBIT PC AND/OR MC
LOAD WR

H=HIGH LEVEL, L=LOW LEVEL

*BI/O CAN BE USED AS OUTPUT

1. OVFL (MSP) = H
   Indicates that operation in process will cause ALU to overflow.

2. MAGNITUDE: The Σ Bus is compared to ZERO. Resultant outputs are:
   AG = H (Σ Bus Arithmetically > ZERO)
   LG = H (Σ Bus ≠ ZERO)
   EQ = H (Σ BUS = ZERO)

3. $\overline{C\text{-}OUT}$ (MSP) = L
   Indicates ALU Carry Out.

FIGURE 21 – FORM I–ARITHMETIC OPERATIONS: A PLUS B PLUS ALUCIN → { Σ' BUS / REGISTER }

a. Form IA provides the capability of adding or subtracting two operands and routing the results to the Σ' bus. Symbolically, this operation can be expressed as:

$$A \left\{\begin{matrix}\text{PLUS}\\ \text{MINUS}\end{matrix}\right\} B \text{ PLUS ALUCIN} \rightarrow \Sigma' \text{ BUS}$$

This form provides the capability of choosing from any one of the A and any one of the B sources listed in Figure 21 as the operands to accomplish the add/subtract. The example illustrated in Figure 22 utilizes the I/O capability of the B input/output port. Input data at the AI or B I/O is setup and then latched into the 'S481 A or B input latch on the negative transition of the 'S481 clock.

During Form IA operations, the contents of the extended working register are not changed and the working register may be saved or loaded directly. The program or memory counters under control of the asynchronous increment, inhibit, and LSP $\overline{CCI}$ can be saved or either may be incremented by one or two. Sources for the DOP and AOP are also selectable.

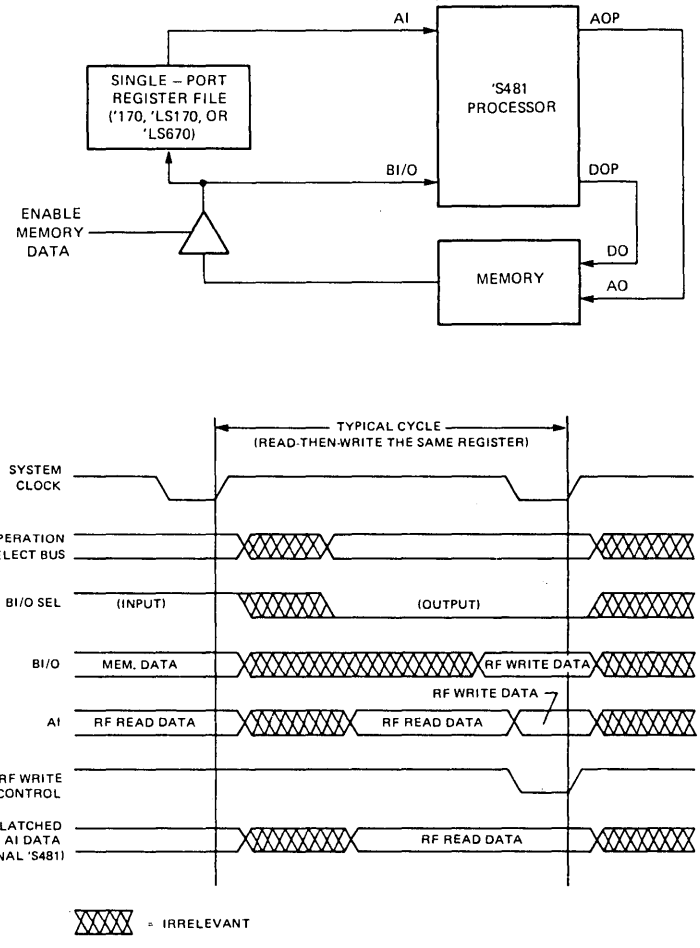


FIGURE 22 – 'S481 OPERATION WITH SINGLE-PORT REGISTER FILE

The overflow and magnitude status lines are active as enumerated in Figure 21.

b. Form IB provides the capability of adding or subtracting two operands and routing the results to one of the four 'S481 storage destinations: the working register (WR), the extended working register (XWR), the program counter (PC), or the memory counter (MC). Symbolically, this operation can be expressed as:

$$A \left\{ \begin{matrix} \text{PLUS} \\ \text{MINUS} \end{matrix} \right\} \text{B PLUS ALUCIN} \rightarrow \text{REGISTER}$$

This form provides the capability of choosing from any one of the A and any one of the B sources listed in Figure 21 as the operands to accomplish the add/subtract.

3.3 OPERATION FORM II – ADD/SUBTRACT WITH DOUBLE-PRECISION SHIFT

Operation Form II is designed specifically to perform one of two classical iterations used frequently to implement microprogrammed multiply and divide algorithms. This form provides the system designer with the capability of selecting a single microinstruction which will complete both the add-and-shift or subtract-and-shift functions in a single clock cycle. Available microinstructions are illustrated in Figure 23. Symbolically, Form II operations can be represented as:

(A PLUS B PLUS ALUCIN)	SHIFTED → WR, XWR
(B MINUS A MINUS 1)	SHIFTED → WR, XWR

Hardwired algorithms for double-precision multiply and divide routines can be selected in operation forms XI, XII, XIII, or XIV.

During Form II operations the status, overflow, and asynchronous controls are the same as described for Form I.

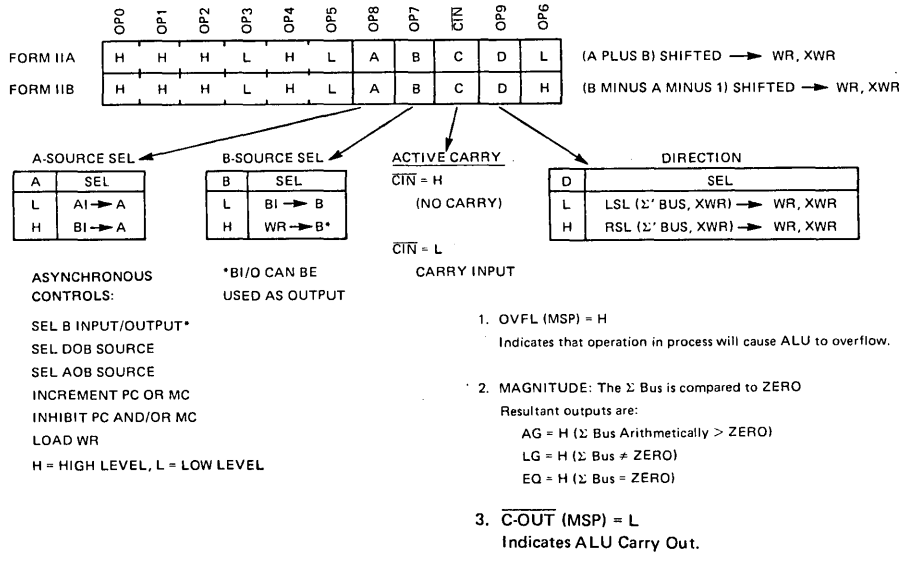


FIGURE 23 – FORM II–ARITHMETIC WITH DOUBLE-PRECISION SHIFT

$$\left\{\begin{matrix}A\\B\end{matrix}\right\} \text{ PLUS } \left\{\begin{matrix}B\\A\end{matrix}\right\} \text{ PLUS CARRY SHIFTED} \rightarrow \text{WR, XWR}$$

(MULTIPLY AND DIVIDE SHIFT OPERATIONS WITHOUT AUTOMATIC CONTROL)

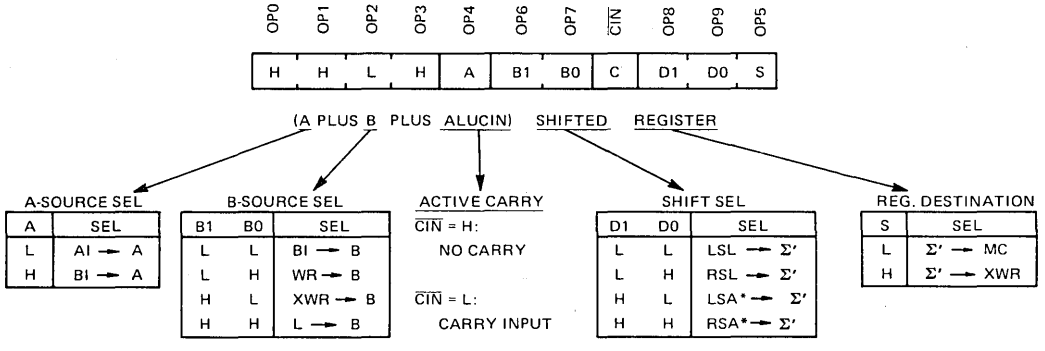
3.4 OPERATION FORM III – ADD WITH SINGLE-PRECISION SHIFT

Operation Form III is a universal microinstruction providing the designers with the capability of performing an add-and-shift function in a single clock cycle. Sources and destinations are shown in Figure 24. Also enumerated are the shift functions which are selectable as part of the microinstruction.

Magnitude and overflow status indicators are active as enumerated in Figure 24. Form III can be represented symbolically as:

(A PLUS B PLUS ALUCIN) SHIFTED → XWR, OR MC

During Form III operation the contents of the working register are not changed unless an asynchronous load is selected. If not selected as the destination, the extended working register will be saved. The memory counter can be the operand destination, or it and the program counter can be saved, or one can be incremented by one or two on selection. Sources for the DOP and AOP are also selectable.



ASYNCHRONOUS CONTROLS:

- SEL B INPUT/OUTPUT
- SEL DOB SOURCE
- SEL AOB SOURCE
- INCREMENT PC OR MC
- INHIBIT PC AND/OR MC
- LOAD WR

H = HIGH LEVEL, L = LOW LEVEL

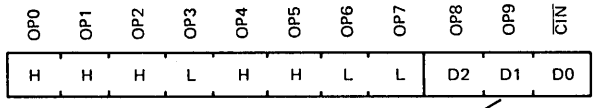
1. OVFL (MSP) = H Indicates that the shift operation in process will cause the selected register to overflow.
2. *MAGNITUDE: During LSA or RSA, A plus C (N1) is compared to $\overline{B}$ (N2); during the remaining operations, the Σ Bus is compared to ZERO. Resultant outputs are:
   AG = H (N1 ARITHMETICALLY > N2) or (Σ BUS ARITHMETICALLY > ZERO)
   LG = H (N1 > N2) or (Σ BUS ≠ ZERO)
   EQ = H (N1 = N2) or (Σ BUS = ZERO)
3. $\overline{COUT}$ (MSP) = L Indicates ALU Carry Out.

FIGURE 24 – FORM III–ARITHMETIC WITH SINGLE-PRECISION SHIFT (A PLUS B PLUS ALUCIN) SHIFTED → XWR OR MC

3.5 OPERATION FORM IV – AI SHIFTED → Σ' BUS

Operation Form IV is designed specifically for performing a single bit-position logical, arithmetic, or circular shift of the data applied at the A input port. This single clock operation can be used to shift information residing in any of the external working memory register locations simply by enabling the output capability of the BI/O port and writing the shifted word back into the same (or any other selected) memory location.

Asynchronous controls are the same as described for Operation Form IA, and the magnitude status lines are active and overflow is active during left-shift arithmetic (LSA) operation as enumerated in Figure 25.



SHIFT SEL

D2	D1	D0	SEL
L	L	L	LSL
L	L	H	RSL
L	H	L	LSA
L	H	H	RSA
H	L	L	LCIR
H	L	H	RCIR
H	H	L	NOT DEFINED
H	H	H	NOT DEFINED

ASYNCHRONOUS CONTROLS:

SEL B INPUT/OUTPUT
SEL DOB SOURCE
SEL AOB SOURCE
INCREMENT PC OR MC
INHIBIT PC AND/OR MC
LOAD WR

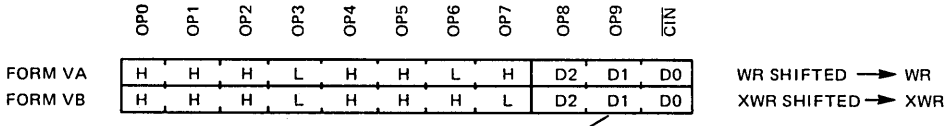
H = HIGH LEVEL, L = LOW LEVEL

1. $\overline{COUT} = \overline{CIN}$
2. OVFL (MSP = H)
   Indicates that LSA operation in process will cause shift overflow. For all other operations, OVFL = L.
3. MAGNITUDE: AI is compared to ZERO. Resultant outputs are:
   AG = H (AI > ZERO)
   LG = H (AI ≠ ZERO)
   EQ = H (AI = ZERO)

FIGURE 25 – FORM IV–AI SHIFTED → Σ* BUS

3.6 OPERATION FORM V – SINGLE-LENGTH SHIFT

Operation Form V performs a single-bit position, logical, arithmetic, or circular shift of either the working register or extended working register. Magnitude status indicators are active and overflow is active during left-shift arithmetic (LSA) operations as enumerated in Figure 26. Asynchronous controls are the same as described for Operation Form IA.



SHIFT SEL

D2	D1	D0	SEL
L	L	L	LSL
L	L	H	RSL
L	H	L	LSA
L	H	H	RSA
H	L	L	LCIR
H	L	H	RCIR
H	H	L	NOT DEFINED
H	H	H	NOT DEFINED

ASYNCHRONOUS CONTROLS:

SEL B INPUT/OUTPUT
SEL DOB SOURCE
SEL AOB SOURCE
INCREMENT PC OR MC
INHIBIT PC AND/OR MC
LOAD WR

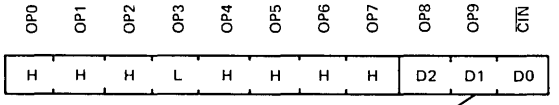
H = HIGH LEVEL, L = LOW LEVEL

1. $\overline{COUT} = \overline{CIN}$
2. OVFL (MSP - H)
   Indicates that LSA operation in process will cause shift overflow. For all other operations, OVFL ≡ L.
3. MAGNITUDE: AI is compared to ZERO. Resultant outputs are:
   AG = H (AI > ZERO)
   LG = H (AI ≠ ZERO)
   EQ = H (AI = ZERO)

FIGURE 26 – FORM V: {WR / XWR} SHIFTED → {WR / XWR}

3.7 OPERATION FORM VI – DOUBLE-PRECISION SHIFTS

Operation Form VI performs a double-precision logical, arithmetic, or circular shift of a double-length word residing in the working register and extended working register. Magnitude status indicators are active and overflow is active during left-shift arithmetic (LSA) operations as enumerated in Figure 27. Asynchronous controls are the same as described for operation form IA.



SHIFT SEL

D2	D1	D0	SEL
L	L	L	LSL
L	L	H	RSL
L	H	L	LSA
L	H	H	RSA
H	L	L	LCIR
H	L	H	RCIR
H	H	L	NOT DEFINED
H	H	H	NOT DEFINED

ASYNCHRONOUS CONTROLS:

SEL B INPUT/OUTPUT
SEL DOB SOURCE
SEL AOB SOURCE
INCREMENT PC OR MC
INHIBIT PC AND/OR MC
LOAD WR
H = HIGH LEVEL, L = LOW LEVEL

1. $\overline{COUT} = \overline{CIN}$
2. OVFL (MSP = H)
   Indicates that LSA operation in process will cause shift overflow. For all other operations, OVFL = L.
3. MAGNITUDE: AI is compared to ZERO. Resultant outputs are:

   AG = H (AI > ZERO)
   LG = H (AI ≠ ZERO)
   EQ = H (AI = ZERO)

FIGURE 27 – FORM VI–DOUBLE-PRECISION SHIFTS: (WR, XWR)SHIFTED →(WR, XWR)

3.8 OPERATION FORM VII – COMPARE (A:B OR B:A)

Operation Form VII is designed specifically to provide the system designer with the capability of symmetrically comparing either operands A-to-B or operands B-to-A. The operands selectable are enumerated in Figure 28 as the A source select or B source select. The carry output, overflow, and magnitude status lines decode and indicate the logical and arithmetic relationship of the operands being compared as shown in Figure 28. Asynchronous controls are the same as described for Operation Form IA.

3.9 OPERATION FORM VIII – LOGICAL FUNCTIONS

The ALU with its carry circuit functionally inactivated in Form VIII operations can be microprogrammed in conjunction with the source operands to perform any of the possible combinatorial Boolean functions on two binary variables. See Figure 29. Simple transfer functions are performed with the arithmetic operations in Form I, and combinatorial transfer and shift operations are available in Form III.

As with the arithmetic operations, a highly flexible source selection extends performance of single clock combinatorial logical operations between two (external) operands applied at the A and B input ports, or combinations of resident data in 'S481 registers or counters can be combined logically with another register or external source. The specific combinations selectable are enumerated in the following paragraphs.

	OP0	OP1	OP2	OP3	OP4	OP8	OP5	OP6	OP7	OP9	$\overline{CIN}$	N1:N2
FORM VIIA	H	H	H	L	L	A	B2	B1	B0	L	H	A : B
FORM VIIB	H	H	H	L	L	A	B2	B1	B0	H	H	B : A

A-SOURCE SEL

A	SEL
L	AI
H	WR

B-SOURCE SEL

B2	B1	B0	SEL
L	L	L	BI
L	L	H	H*
L	H	L	BI · WR
L	H	H	WR*
H	L	L	BI · XWR
H	L	H	XWR*
H	H	L	BI · PC
H	H	H	PC*

ASYNCHRONOUS CONTROLS:
- SEL B INPUT/OUTPUT*
- SEL DOB SOURCE
- SEL AOB SOURCE
- INCREMENT PC OR MC
- INHIBIT PC AND/OR MC
- LOAD WR

*BI/O CAN BE USED AS OUTPUT (Σ BUS = N1–N2–1)

1. $\overline{COUT}$ = LG
2. MAGNITUDE: A or B (N1) is compared to B or A (N2), respectively. The resultant outputs are:
   - AG = H (N1 arithmetically > N2)
   - LG = H (N1 logically > N2)
   - EQ = H (N1 = N2)
3. OVFL (MSP) IS NOT DEFINED.

H = HIGH LEVEL, L = LOW LEVEL

FIGURE 28 – FORM VII–COMPARE: {A : B / B : A}

	OP0	OP1	OP2	OP3	OP4	OP8	OP6	OP7	OP9	OP5	$\overline{CIN}$	
FORM VIIA	H	L	H	L	A1	A0	B2	B1	B0	S1	S0	NOR
FORM VIIB	H	L	H	H	A1	A0	B2	B1	B0	S1	S0	OR
FORM VIIC	H	H	L	L	A1	A0	B2	B1	B0	S1	S0	EX-OR

A {NOR / OR / X-OR} B → REG

A-SOURCE SEL

A1	A0	SEL
L	L	AI → A
L	H	$\overline{AI}$ → A
H	L	WR → A
H	H	$\overline{WR}$ → A

B-SOURCE SEL

B2	B1	B0	SEL
L	L	L	BI → B
L	L	H	$\overline{BI}$ → B
L	H	L	WR → B*
L	H	H	$\overline{WR}$ → B*
H	L	L	XWR → B*
H	L	H	$\overline{XWR}$ → B*
H	H	L	PC → B*
H	H	H	$\overline{PC}$ → B*

REG DESTINATION SEL

S1	S0	SEL
L	L	Σ' → WR
L	H	Σ' → XWR
H	L	Σ' → PC
H	H	Σ' ONLY

*BI/O CAN BE USED AS OUTPUT.

ASYNCHRONOUS CONTROLS:
- SEL B INPUT/OUTPUT*
- SEL DOB SOURCE
- SEL AOB SOURCE
- INCREMENT PC OR MC
- INHIBIT PC AND/OR MC
- LOAD WR

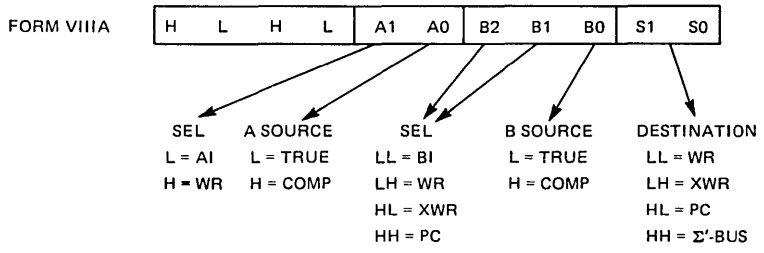
H = HIGH LEVEL, L = LOW LEVEL

1. OVFL = LOW
2. $\overline{COUT}$ = $\overline{CIN}$
3. MAGNITUDE: The Σ Bus is compared to ZERO. Resultant outputs are:
   - AG = H (Σ Bus Arithmetically > ZERO)
   - LG = H (Σ Bus ≠ ZERO)
   - EQ = H (Σ Bus = ZERO)

FIGURE 29 – FORM VIII–LOGICAL OPERATIONS: A {NOR / OR / X-OR} B → REGISTER

3.9.1 NOR/AND Logical Operations

Operation Form VIIIA can be used to perform the NOR or AND logical combination of two selectable operands and route the results to one of four destinations. The operation microcode is:



H=HIGH LEVEL, L=LOW LEVEL

As shown above, the A and B sources are selectable by the A1, B1, and B2 bits in their true or complementary form (bits A0, B0) to facilitate performing the NOR, mixed NOR/AND, and the AND functions. As implemented, see Figure 30, the NOR function is performed when the sources are both true, mixed NOR/AND functions are performed with one source complemented, and the AND function is performed when both sources are selected in their complement form. Both implementation and other/equal logic symbols are shown in Figure 30. Also provided are the function tables and Boolean equations.

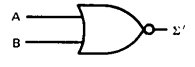
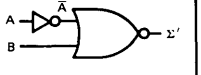
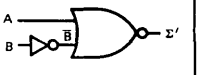
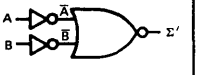
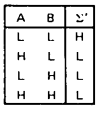
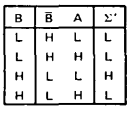
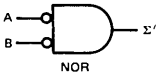
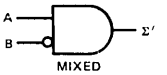
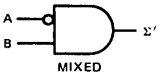
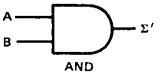
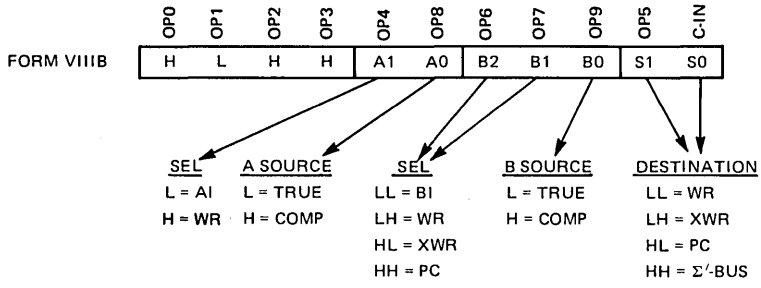
	SELECTIONS AVAILABLE			
	TRUE	A = COMP	B = COMP	A and B = COMP
IMPLEMENTATION				
FUNCTION TABLES (H = HIGH LEVEL, L = LOW LEVEL)	 OP8 = OP9 = L	 OP8 = H, OP9 = L	 OP8 = L, OP9 = H	 OP8 = OP9 = H
OTHER OR EQUAL SYMBOLS	 NOR	 MIXED	 MIXED	 AND
BOOLEAN FUNCTIONS	$\Sigma' = \overline{A + B}$	$\Sigma' = A\overline{B}$	$\Sigma' = \overline{A}B$	$\Sigma' = AB$

FIGURE 30 – FORM VIIIA NOR/AND LOGICAL OPERATIONS

3.9.2 OR/NAND Logical Operations

Operation Form VIIIB can be used to perform the OR or NAND logical combination of two selectable operands and route the results to one of four destinations. The operation microcode is:



H=HIGH LEVEL, L=LOW LEVEL

As shown above, the A and B sources are selectable by the A1, B1, and B2 bits in their true or complementary form (bits A0, B0) to facilitate performing the OR, mixed OR/NAND, and the NAND functions. As implemented, see Figure 31, the OR function is performed when the sources are both true, mixed OR/NAND functions are performed with one source complemented, and the NAND function is performed when both sources are selected in their complement form. Both implementation and other/equal logic symbols are shown in Figure 31. Also provided are the function tables and Boolean equations.

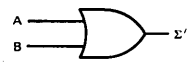
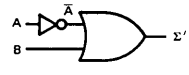
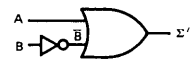
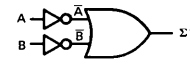
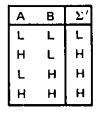
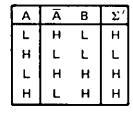
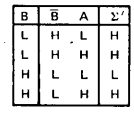
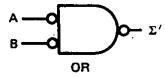
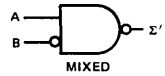
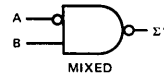
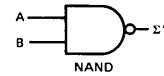
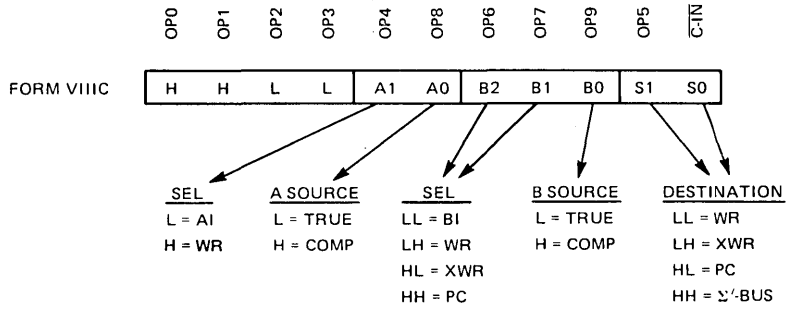
	SELECTIONS AVAILABLE			
	TRUE	A = COMP	B = COMP	A and B = COMP
IMPLEMENTATION				
FUNCTION TABLES (H = HIGH LEVEL, L = LOW LEVEL)	 OP8 = OP9 = L	 OP8 = H, OP9 = L	 OP8 = L, OP9 = H	 OP8 = OP9 = H
OTHER OR EQUAL SYMBOLS	 OR	 MIXED	 MIXED	 NAND
BOOLEAN FUNCTIONS	$\Sigma' = A + B$	$\Sigma' = \overline{A} + B$	$\Sigma' = A + \overline{B}$	$\Sigma' = \overline{AB}$

FIGURE 31 – FORM VIIIB OR/NAND LOGICAL OPERATIONS

3.9.3 Exclusive-OR/Exclusive-NOR Logical Operations

Operation Form VIIIC can be used to perform the exclusive-OR/exclusive-NOR logical combination of two selectable operands and route the results to one of four destinations. The operation microcode is:



H = HIGH LEVEL, L = LOW LEVEL

As shown above, the A and B sources are selectable by the A1, B1, and B2 bits in their true or complementary form (bits A0, B0) to facilitate both exclusive-OR and exclusive-NOR operations. As implemented, see Figure 32, the exclusive-NOR function is performed when the sources are both true or both complemented. When either the A or the B source (not both) are complemented, the exclusive-OR function is performed. Both implementation and other/equal logic symbols are shown in Figure 32. Also provided are the function tables and Boolean equations.

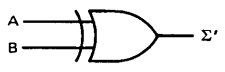
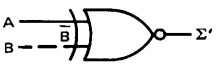
	ALL TRUE OR ALL COMPLEMENT SOURCES	ONE SOURCE COMPLEMENTED	
IMPLEMENTATION	 EX–OR		
FUNCTION TABLES (H = HIGH LEVEL, L = LOW LEVEL)	A B Σ' L L H H L L L H L H H H	A Ā B Σ' L H L L H L L H L H H H H L H L	B B̄ A Σ' L H L L L H H H H L L H H L H L
	OP8 = OP9 = L	OP8 = H, OP9 = L	OP8 = L, OP9 = H
BOOLEAN FUNCTIONS	$\Sigma' = A \oplus B$	$\Sigma' = \bar{A} \oplus B$	$\Sigma' = A \oplus \bar{B}$

FIGURE 32–FORM VIIIC EXCLUSIVE-OR/EXCLUSIVE-NOR OPERATIONS

3.10 OPERATION FORM IX – NO OP

Operation Form IX is designed specifically to clear the Σ' bus force AG and LG low, and force EQ high; and, during this operation form data in the 'S481 registers, counters and latches remain unchanged unless directed to do otherwise by the asynchronous control inputs as shown in Figure 33.

The memory or program counter can be incremented (by one or two) on each clock transition, or the working register can be loaded on each clock. Additionally, the B input/output can be specified, as well as sources for the address or data out ports. States of the carry and overflow outputs are not interrupted.

OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	OP8	OP9	$\overline{CIN}$
H	H	H	H	H	X	X	X	X	X	X

H = HIGH LEVEL, L = LOW LEVEL, X = IRRELEVANT

ASYNCHRONOUS CONTROLS:

SEL B INPUT/OUTPUT
SEL DOB SOURCE
SEL AOB SOURCE
INCREMENT PC OR MC
INHIBIT PC AND/OR MC
LOAD WR

AG = ZERO
LG = ZERO
EQ = HIGH

FIGURE 33 – FORM IX–NO OPERATION: ZERO → Σ' BUS

3.11 OPERATION FORM X – CYCLIC REDUNDANCY CHARACTER ACCUMULATION

Operation Form X is a macroinstruction which can be used to update a 16-bit cyclic redundancy character (CRC) partial sum in eight clock cycles, assuming 8-bit data characters. The updated CRC partial sum resides in the working register. The flow diagram of this algorithm is illustrated in Figure 34.

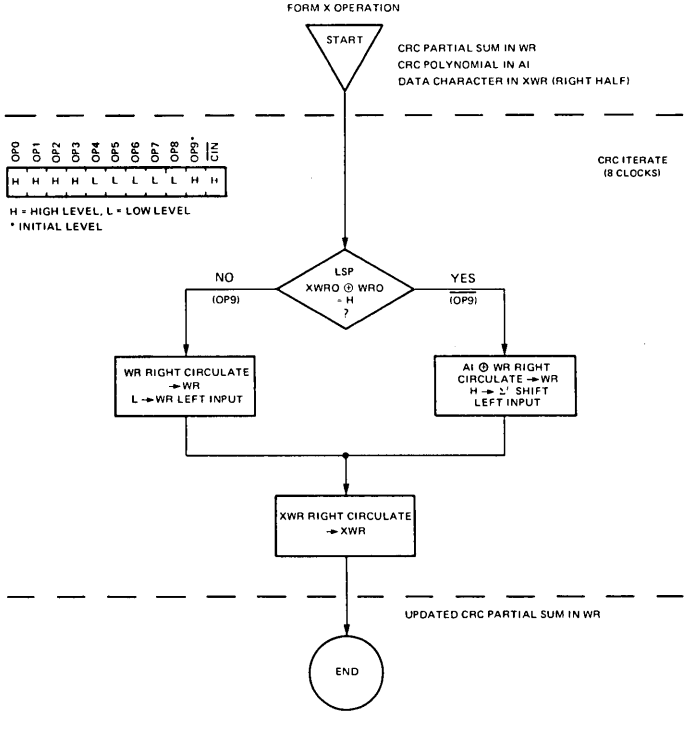


FIGURE 34 – CYCLIC REDUNDANCY CHARACTER ACCUMULATION

Setup conditions include the existence or placement of the previous CRC partial sum in the working register, the CRC polynomial at the A input port, and the data character in the eight least significant bits of the extended working register. All decisions after setup are decoded on chip for each of the eight iterations. Microcontrol open-collector output OP9 of the LSP assumes control during the iterations to generate one of two microinstructions requires to accomplish the CRC update.

3.12 OPERATION FORM XI – SIGNED INTEGER DIVIDE

Operation Form XI consists of the micro/macroinstructions needed to perform the signed division of a double length dividend by an N-bit divisor in N + 3 clock times. After the division routine the quotient will reside in the extended working register (XWR) and the remainder will be in the working register (WR). Negative results are in two's complement. The flow diagram of this algorithm is illustrated in Figure 35.

Setup conditions include the existence or placement of the double length dividend in the WR, XWR and application of the divisor at the A input port. To obtain a legitimate result, the divisor must not be arithmetically zero as indicated during the start command by the EQ output being low. The dividend must be of a nature that it could be generated by a signed multiply and add operation on the divisor. Status outputs LG, AG, C OUT and OV are undefined, as is EQ after the start command.

After setup, all decisions are decoded on chip for start, iterate, iteration finish, fix remainder, and adjust quotient. The iterate macroinstruction (Form XIB) internally decodes the status of the stored signs, carry out, and working register and the OP8 and OP9 microcontrol open-collector outputs of the MSP assume control generating one of four microinstructions required to accomplish the signed divide.

3.13 OPERATION FORM XII – UNSIGNED DIVIDE

Operation Form XII consists of micro/macroinstructions needed to perform the unsigned division of a double length dividend by an N-bit divisor in N + 1 clock times. After the division routine the binary magnitude quotient will reside in the extended working register (XWR) and the binary magnitude remainder will be in the working register (WR). The flow diagram of this algorithm is illustrated in Figure 36.

Setup conditions include the existence or placement of the double length dividend in the WR, XWR; application of the divisor at the A input port and that the last operation was not a divide command. To obtain a legitimate result, the N-bit divisor must be logically greater than the most-significant N-bits resident in the working register. A-input data compared to working register (AI:WR) prior to the unsigned divide can be used to obtain validity to start by asserting LG true.

After setup, all decisions are decoded on chip for start, iterate and finish. The iterate macroinstruction (Form XIIB) internally decodes the status of C OUT or FORCE LOAD FLAG and the OP9 microcontrol open-collector output of the MSP assumes control generating one of two microinstructions required to accomplish the unsigned divide.

3.14 OPERATION FORM XIII – UNSIGNED MULTIPLY

Operation Form XIII consists of a macroinstruction which performs the unsigned multiplication of two N-bit words in N clock times. After the multiply routine the double length product is residing in the working register (most-significant N-bits) and the extended working register (least-significant N-bits). The flow diagram of this algorithm is illustrated in Figure 37.

Setup conditions include clearing the working register to all zeros, loading (not shifting) the multiplier into the extended working register, and applying the multiplicand at the A input port. Arithmetic shift commands must not occur between multiplier load and the first iteration. Status outputs (EQ, AG, LG, C OUT and OV) are undefined during this algorithm.

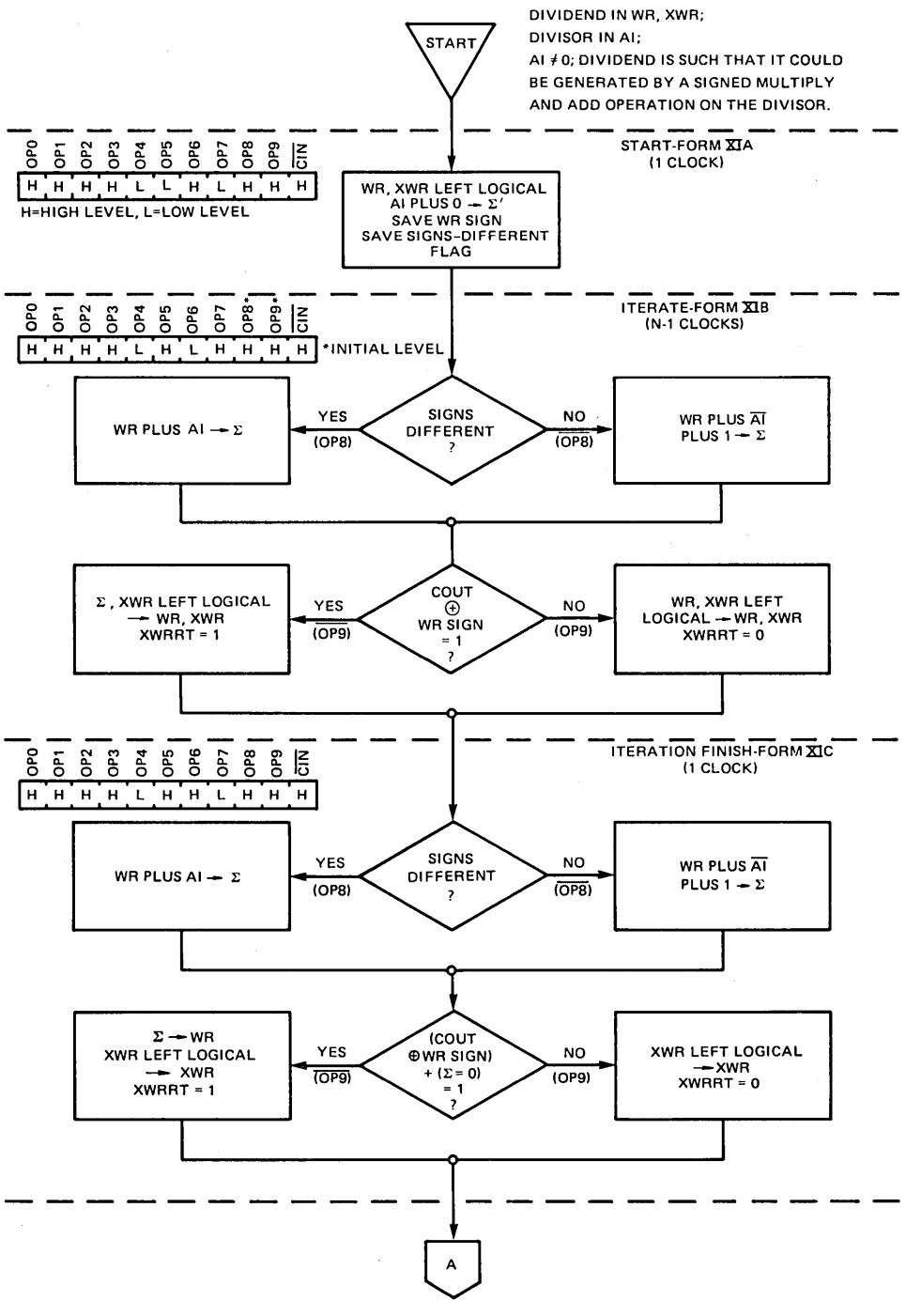


FIGURE 35 – FORM XI–SIGNED INTEGER DIVIDE (SHEET 1 OF 2)

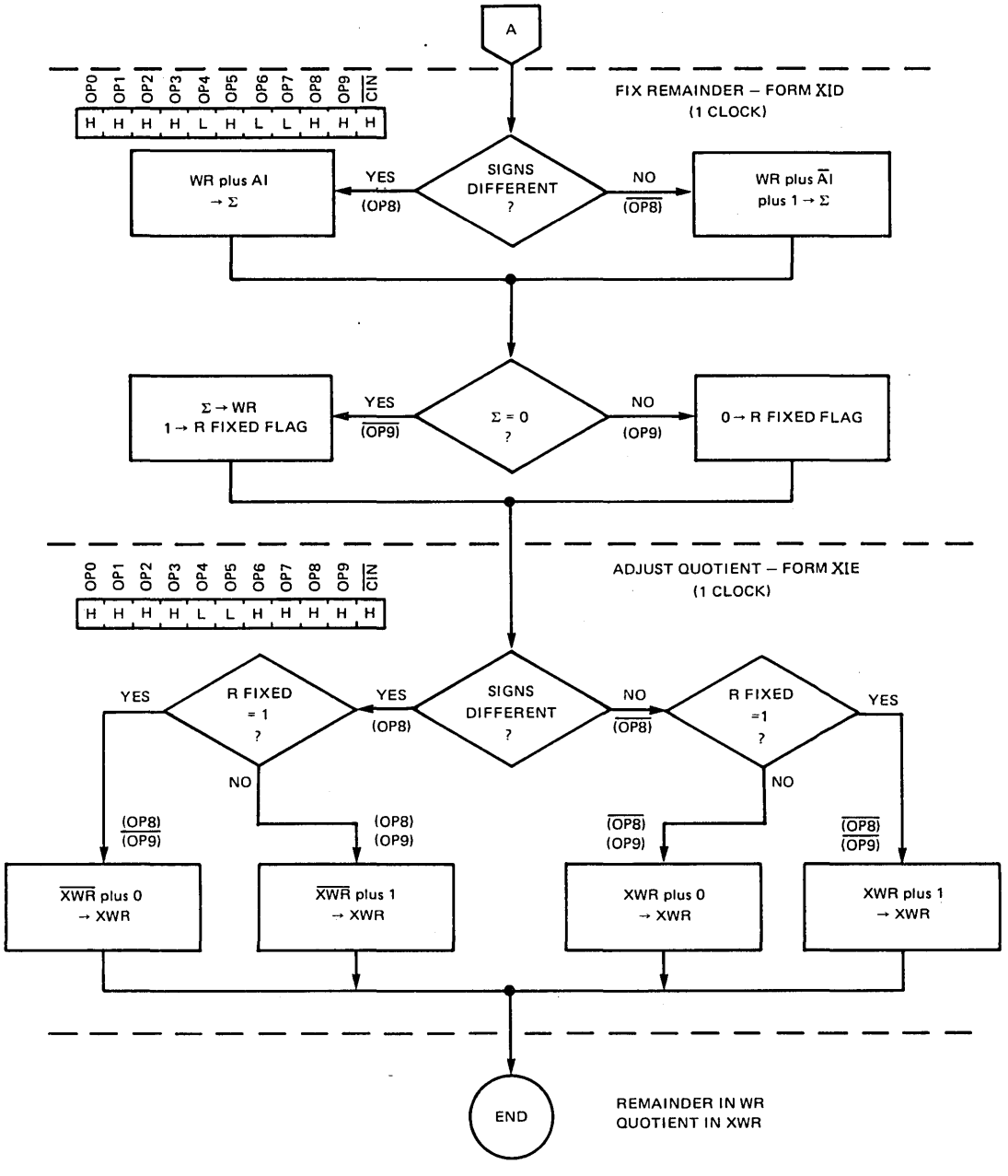


FIGURE 35 – FORM XI–SIGNED INTEGER DIVIDE (SHEET 2 OF 2)

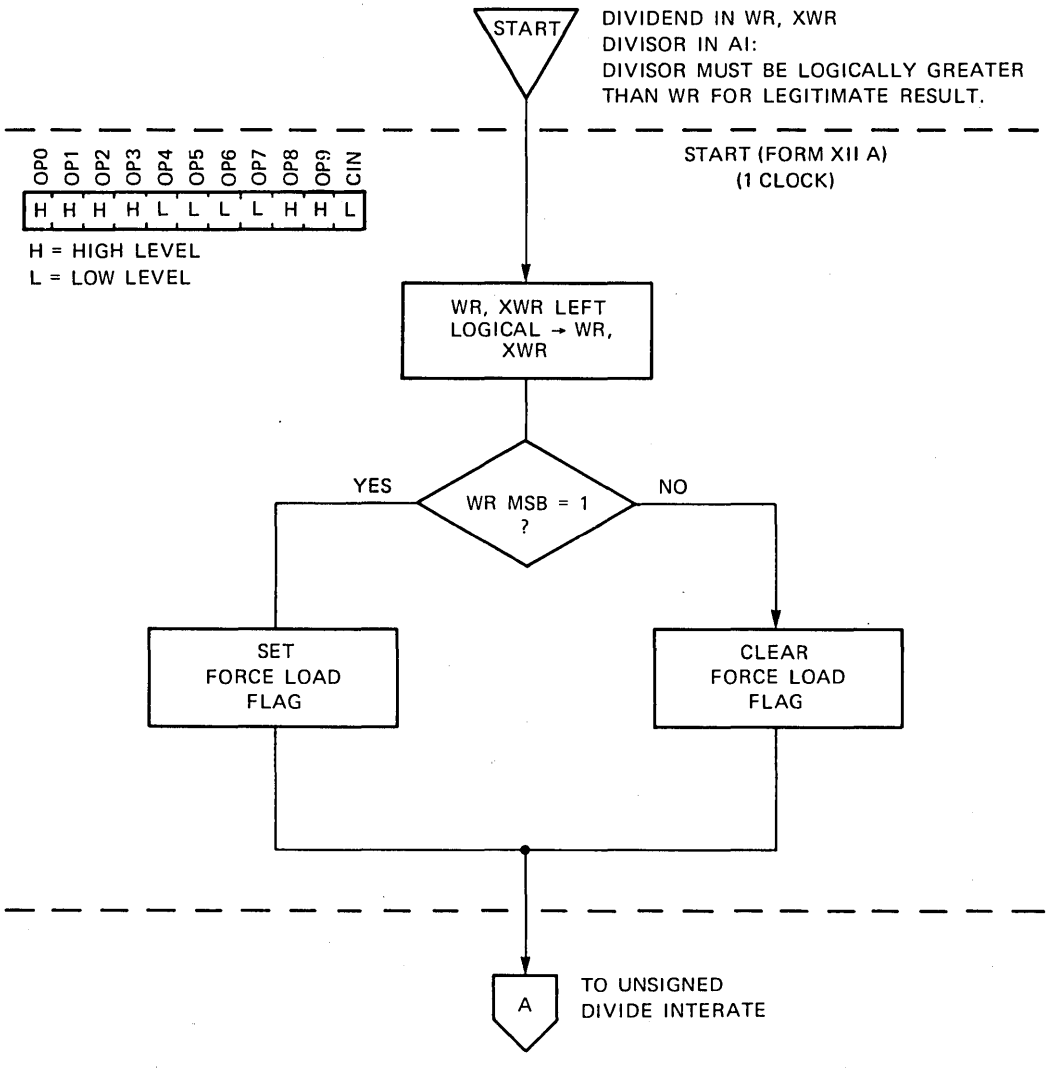


FIGURE 36 – FORM XII–UNSIGNED DIVIDE (SHEET 1 OF 2)

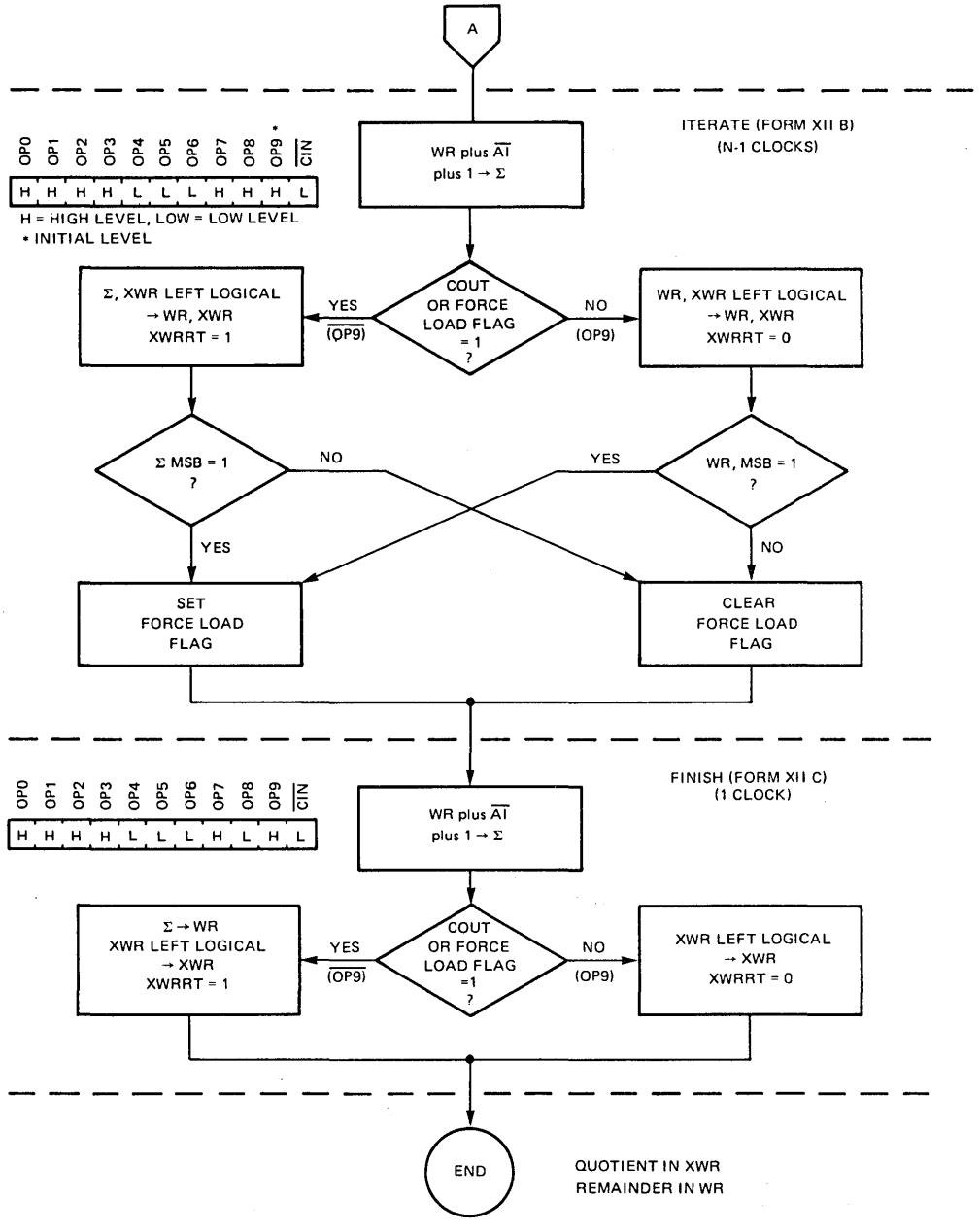


FIGURE 36 – FORM XII–UNSIGNED DIVIDE (SHEET 2 OF 2)

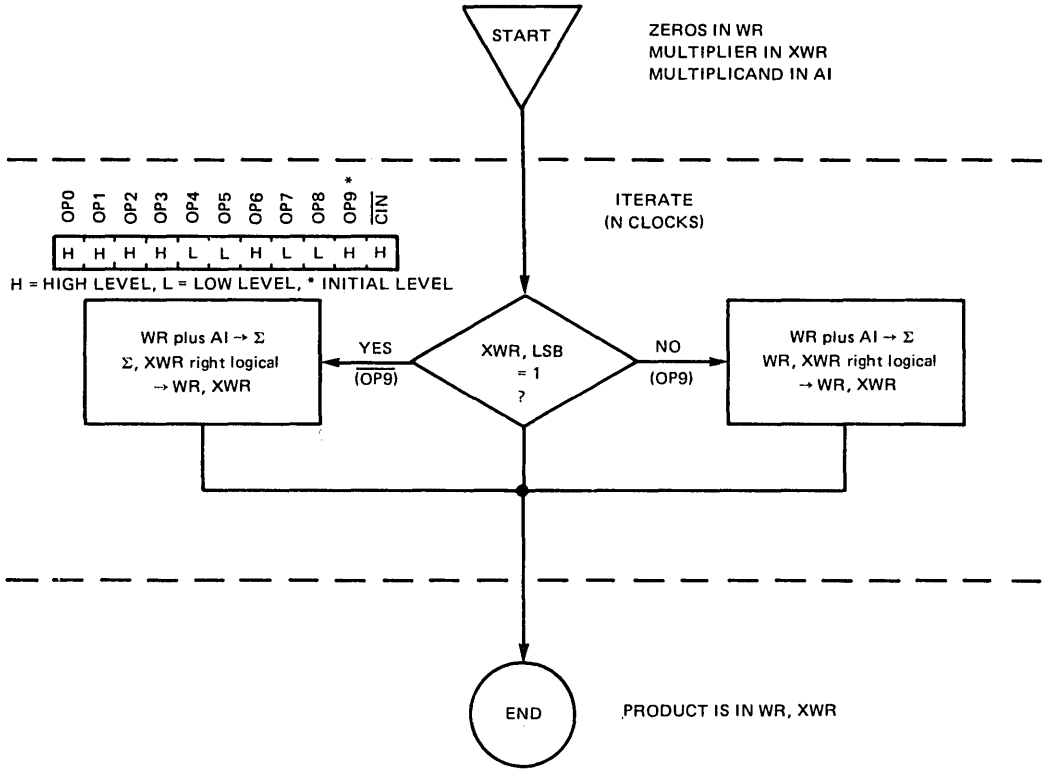


FIGURE 37 – FORM XIII–UNSIGNED MULTIPLY

The iterate macroinstruction internally decodes the status of the XWR LSB and the OP9 microcontrol open-collector output of the MSP assumes control generating one of two microinstructions required to accomplish the unsigned multiply.

3.15 OPERATION FORM XIV – SIGNED INTEGER MULTIPLY

Operation Form XIV consists of a macroinstruction which performs the signed multiplication of two N-bit signed integers in N clock times. After the multiply routine, the double precision signed product resides in the working register (most-significant N-bits) and the extended working register (least-significant N-bits). Negative products are in two's complement. The flow diagram of this algorithm is illustrated in Figure 38.

Setup conditions include clearing the working register to all zeros, loading (not shifting) the multiplier into the extended working register, and applying the multiplicand at the A input port. Arithmetic shifts must not occur between multiplier load and the first iteration. Status outputs (EO, AG, LG, C-OUT, and OV) are undefined during this algorithm.

The iterate macroinstruction internally decodes the status of the multiplier (XWR) sign-bit flag, the multiplier LSB, and the multiplier LSB flag and the OP8 and OP9 microcontrol open-collector outputs of the MSP assume control generating one of four microinstructions required to accomplish the signed multiply.

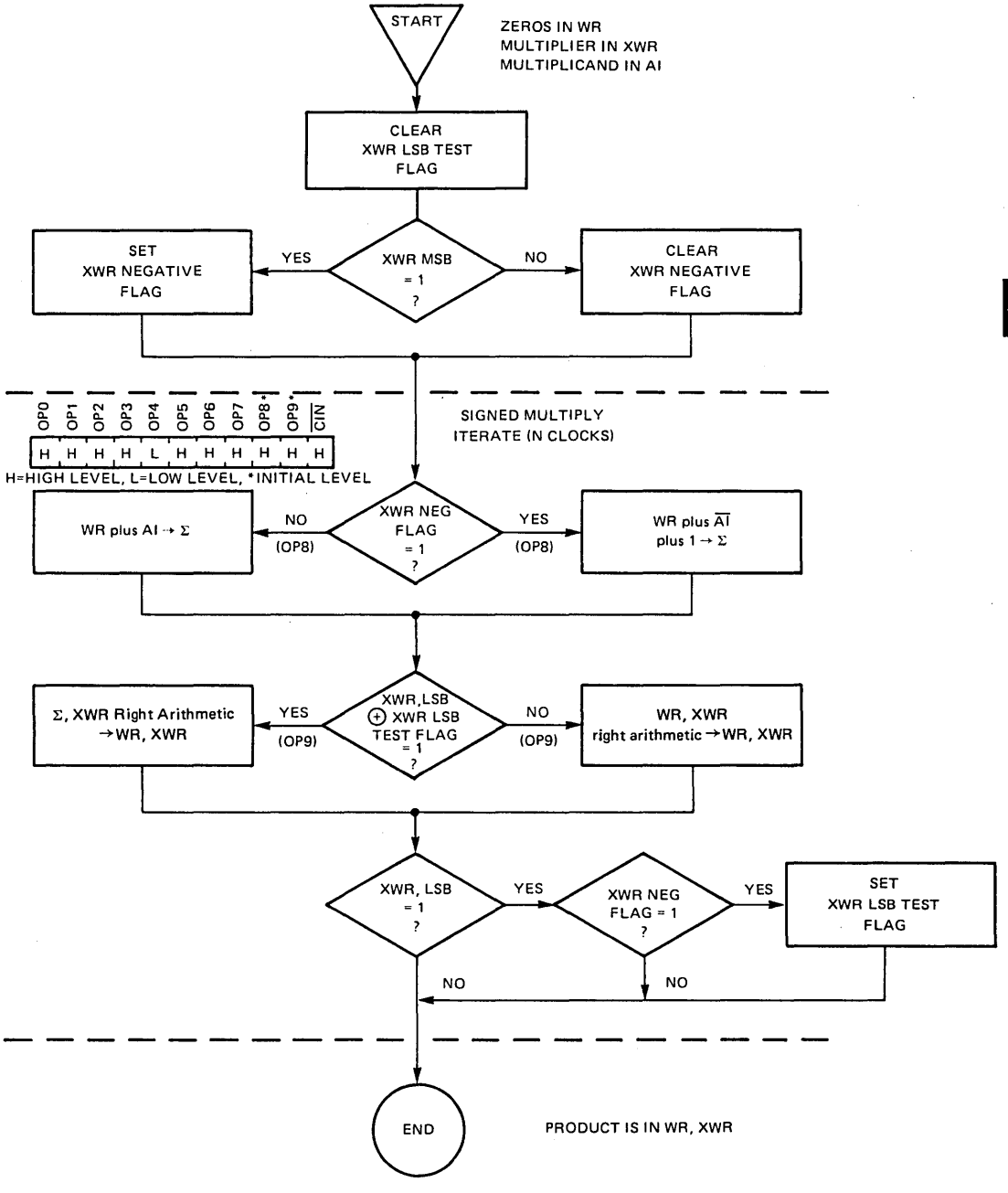


FIGURE 38 – FORM XIV–SIGNED INTEGER MULTIPLY

4. SPECIFICATIONS

TABLE 19

SN54S481 AND SN74S481 RECOMMENDED OPERATING CONDITIONS

PARAMETER		SN54S481			SN74S481			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output voltage at EQ, OP8, OP9; V_O				5.5			5.5	V
Low-level output current, I_{OL}	AOP, BI/O, DOP, $\overline{CCO}$/OV, $\overline{COUT}$			10			10	mA
	EQ, OP8, OP9			8			8	
	WRLFT, WRRT, XWRLFT, XWRRT			6			6	
	X/LG, Y/AG			16			16	
High-level output current, I_{OH}	BI/O, DOP			2			6.5	mA
	All other outputs or I/O except EQ, OP8, OP9			1			1	
Width of clock pulse, t_w	High logic level	35			35			ns
	Low logic level	25			25			
Clock frequency				9			10	MHz
Setup time, t_{su}	AI, BI/O Latch	15↓			15↓			ns
	AI → WR	15↑			15↑			
	AI, BI/O → ALU → MC, PC, WR, XWR	70↑			60↑			
	$\overline{CCI}$, $\overline{INCMC}$, $\overline{INCPC}$, $\overline{LDWR}$	35↑			30↑			
	OP0 thru OP9	120↑	90		100↑	60		
	$\overline{CIN}$	55↑			40↑			
	WRLFT, WRRT, XWRLFT, XWRRT	30↑			25↑			
Hold time, t_h	AI, BI/O → Latch	10↓			10↓			ns
	AI → WR	10↑			10↑			
	AI, BI/O → ALU → MC, PC, WR, XWR			−20↑			−20↑	
	$\overline{CCI}$, $\overline{INCMC}$, $\overline{INCPC}$, $\overline{LDWR}$	0↑			10↑			
	OP0 thru OP9			5↑			5↑	
	$\overline{CIN}$	0↑			0↑			
	WRLFT, WRRT, XWRLFT, XWRRT	5↑			5↑			
Operating free-air temperature range, T_A		55	25	125	0	25	70	°C

↑↓The arrow indicates the transistion of the clock input used for reference; ↑for the low-to-high transition, ↓ for the high-to-low transistion.

TABLE 20

SN54S481 AND SN74S481 ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage	see Note 1			2			V
V_{IL}	Low-level input voltage	see Note 1					0.8	V
V_{IK}	Input clamp voltage		V_{CC}=MIN, I_I=−18 mA				−1.2	V
V_{OH}	High-level output voltage	Any I/O or output except EQ, OP8, OP9	V_{CC}=MIN, V_{IH}=2 V, V_{IL}=0.8 V, I_{OH}=MAX	54S'	2.5			V
				74S'	2.7	3.4		
V_{OL}	Low-level output voltage		V_{CC}=MIN, V_{IH}=2 V, V_{IL}=0.8 V, I_{OL}=MAX				0.5	V
I_{OH}	High-level output current	EQ, OP8, OP9	V_{CC}=MAX, V_O=5.5 V				100	μA
I_I	Input current at maximum input voltage	POS	V_{CC}=MAX, V_I=V_{CC}				1	mA
		Any other input	V_{CC}=MAX, V_I=5.5 V				1	
I_{IH}	High-level input current	OP0, OP1, OP2, OP3, $\overline{CIN}$	V_{CC}=MAX, V_I=2.7 V				200	μA
		Any other (see Note 1)					100	μA
I_{IL}	Low-level input current	OP0 thru OP3, $\overline{CIN}$, POS, $\overline{CCI}$	V_{CC}=MAX, V_I=0.5 V				−8	mA
		WRRT, WRLFT, XWRRT, XWRLFT, CLOCK					−6	
		Any other input					−2	
I_{OS}	Short-circuit output current§	Any output or I/O except EQ, OP8, OP9	V_{CC}=MAX		−30		−100	mA
I_{CC}	Supply current		V_{CC}=MAX			380	425	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time.

NOTE 1. For POS input value see Table 3 on page 1-10

DESIGN GOAL
This document provides tentative information on a product in the developmental stage. Texas Instruments reserves the right to change or discontinue this product without notice.

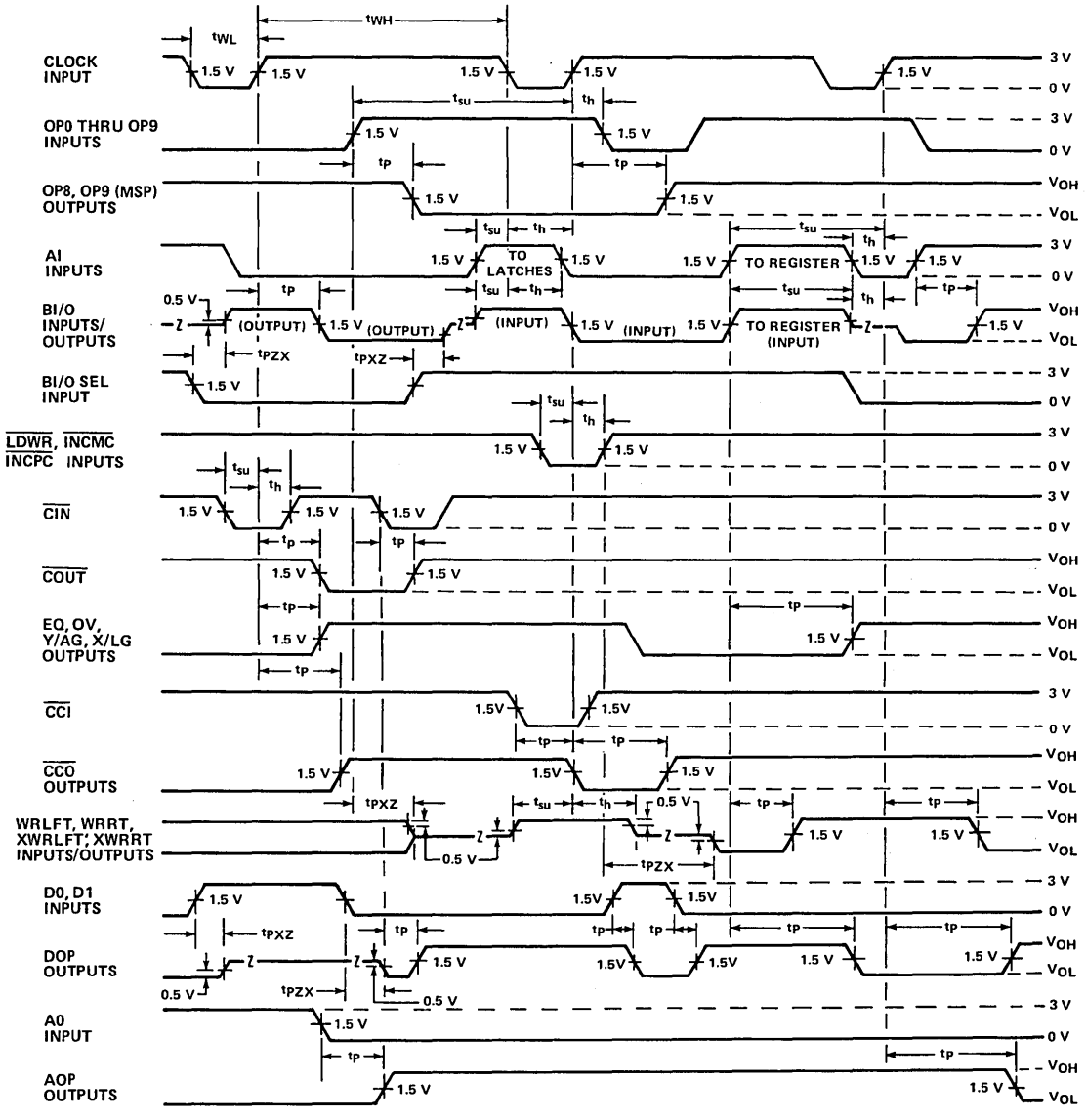
TABLE 21
SN54S481 AND SN74S481 SWITCHING CHARACTERISTICS (OVER OPERATING RANGE OF V_{CC} AND T_A)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OPERATION ROUTING	SN54S481 TYP	SN54S481 MAX	SN74S481 TYP	SN74S481 MAX	UNIT
t_{PD}	AL, BI/O	DOP	LATCH → ALU, DOP	42	75	42	65	ns
		X, Y	LATCH → ALU	32	60	32	50	
		$\overline{COUT}$	LATCH → ALU	30	50	30	45	
		EQ	LATCH → ALU	45	75	45	65	
		OV	LATCH → ALU	35	60	35	45	
		AG, LG	LATCH → ALU	60	100	60	80	
		WRLFT, WRRT, XWRLFT, XWRRT	LATCH → ALU	45	75	45	65	
t_{PD}	OP0 thru OP9	WRLFT, WRRT, XWRLFT, XWRRT		65	115		95	ns
		$\overline{COUT}$		55	95	55	80	
		X, Y		60	105	60	85	
		EQ		55	105	55	75	
		OV		60	105	60	90	
		AG, LG		75	125	75	110	
		DOP		70	115	70	95	
t_{PD}	AI, BI/O	BI/O	LATCH → ALU	35	65	50	55	ns
t_{PD}	$\overline{CIN}$	$\overline{COUT}$		30	50	30	45	ns
t_{PD}	$\overline{CCI}$	$\overline{CCO}$		37	75	37	60	ns
t_{PD}	A0	AOP		20	30	15	30	ns
t_{PD}	D0, D1	DOP		15	35	15	30	ns
t_{PXZ}	BI/O SEL or D0, D1	BI/O or DOP		15	35	15	30	ns
t_{PXZ}	OP0 thru OP9	WRLFT, WRRT, XWRLFT, XWRRT		45	90	45	80	ns
t_{PZX}	BI/O SEL or D0, D1	BI/O or DOP		15	35	15	30	ns
t_{PZX}	OP0 thru OP9	WRLFT, WRRT, XWRLFT, XWRRT		45	90	45	80	ns
t_{PD}	CLOCK	AOP, DOP	NO SHIFT	26	50	26	40	ns
		WRLFT, WRRT, XWRLFT, XWRRT	[WR, XWR, ΣBUS]	40	75	40	60	
		AOP, DOP	→ SHIFTED	30	50	35	40	
		OV		50	90	50	70	
		$\overline{CCO}$		25	45	25	40	
		$\overline{COUT}$		47	85	47	65	
		OP8, OP9		45	90	45	75	
		X, Y		48	85	48	75	
t_{PD}	$\overline{CIN}$	DOP		42	80	42	60	ns

t_{PD} ≡ Propogation delay
t_{PXZ} ≡ Disable time to Hi-Z
t_{PZX} ≡ Enable time (Hi-Z-To-Enable)

2

DESIGN GOAL
This document provides tentative information on a product in the developmental stage. Texas Instruments reserves the right to change or discontinue this product without notice.



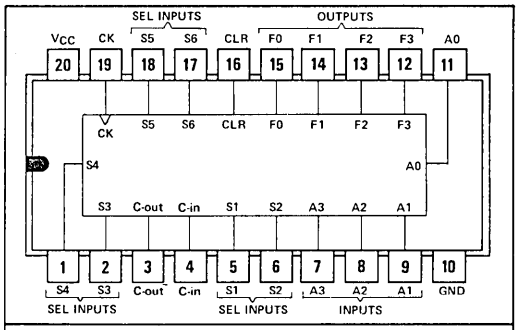
NOTE: Input pulses are supplied by a generator having the following characteristics:
$t_r \leq 5$ ns, tp ≤ 5 ns, PRR ≥ 1 MHz, ZOUT $\approx 50\ \Omega$

A0001385

FIGURE 39 – SWITCHING-TIME VOLTAGE WAVEFORMS

- 4-Bit Slice is Cascadable to N-Bits
- Designed Specifically for Microcontroller/ Next-Address Generator Functions
- Increment/Decrement by One (Immediate or Direct Symbolic Addressing Modes)
- Offset, Vector, or Branch (Indexed or Relative Addressing Modes)
- Store Up to Four Returns or Links (Program Return Address from Subroutine)
- Program Start or Initialize (Return to Zero or Clear Mode)
- On-Chip Edge-Triggered Output Register (Provides Steady-State Micro-Address/ Instruction)
- High-Density 20-Pin Dual-in-Line Package with 300-Mil Row Pin Spacing

SN54S482 . . . J PACKAGE
SN74S482 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: See function table.

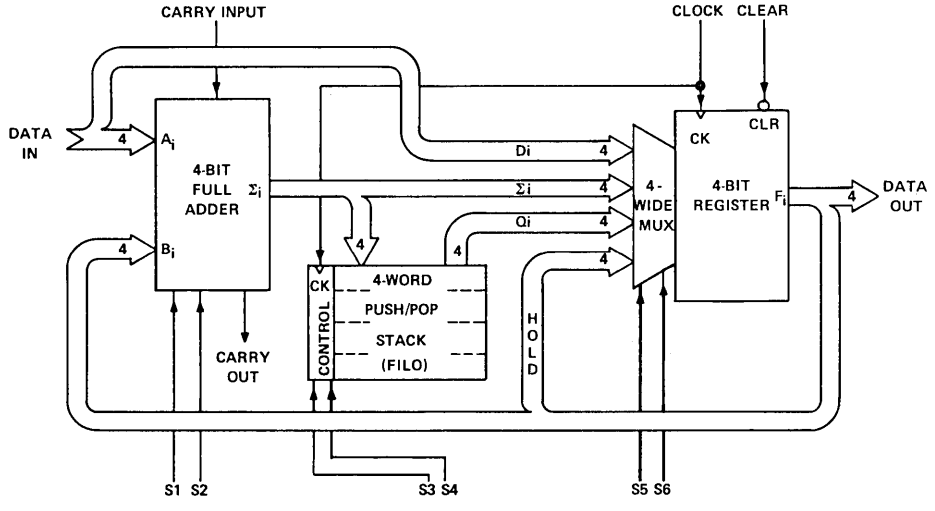
2

description

The 'S482 is a high-performance Schottky TTL 4-bit-slice control element for use in any computer/control application requiring the coupling of high-performance bipolar speeds with the flexibility of microprogram control and bit-slice expandability. When used as a next-address generator, two 'S482 elements can address up to 256 words of microprogram; three elements can address up to 4096 words of microprogram; or a number of 'S482 elements can generate N words in multiples of four lines.

Comprised of an output register, push-pop stack, and a full adder, the 'S482 provides the capability to implement multiway testing needed to generate or to determine and select the source of the next function of microprogram address.

functional block diagram



TENTATIVE DATA SHEET

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output register and source functions

The 4-bit edge-triggered register provides a steady-state output throughout each system clock cycle. An asynchronous clear extends the multiway testing to directly implement system initialization at ROM address zero.

Two source-select lines (S5, S6) provide the output register with access to either the current instruction (no change), an operand or address stored in the push-pop stack, the output of a four-function full adder, or a direct data-in address port. The sources and functions are summarized in Tables I and II.

TABLE I. REGISTER-SOURCE FUNCTIONS

SELECT		REGISTER INPUT SOURCE
S5	S6	
L	L	DATA-IN PORT (Di)
L	H	FULL ADDER OUTPUTS (Σi)
H	L	PUSH-POP STACK OUTPUTS (Qi)
H	H	REGISTER OUTPUTS (HOLD)

H ≡ high level, L ≡ low level

TABLE II. PUSH-POP STACK CONTROL AND REGISTER-SOURCE FUNCTIONS

	INPUTS						INTERNAL	OUTPUTS
	S3	S4	S5	S6	CLOCK	CLEAR	QiA	Fi
HOLD	X	X	X	X	L	H	QiA0	Fi0
CLEAR	X	X	X	X	X	L	QiA0	L
PUSH-POP STACK "HOLD"	L	L	L	L	↑	H	QiA0*	Di
	L	L	L	H	↑	H	QiA0*	Σi
	L	L	H	L	↑	H	QiA0*	QiA0
	L	L	H	H	↑	H	QiA0*	Fi0
PUSH-POP STACK "LOAD"	L	H	L	L	↑	H	Σi*	Di
	L	H	L	H	↑	H	Σi*	Σi
	L	H	H	L	↑	H	Σi*	QiA0
	L	H	H	H	↑	H	Σi*	Fi0
PUSH-POP STACK "POP"	H	L	L	L	↑	H	QiB0†	Di
	H	L	L	H	↑	H	QiB0†	Σi
	H	L	H	L	↑	H	QiB0†	QiA0
	H	L	H	H	↑	H	QiB0†	Fi0
PUSH-POP STACK "PUSH"	H	H	L	L	↑	H	Σi‡	Di
	H	H	L	H	↑	H	Σi‡	Σi
	H	H	H	L	↑	H	Σi‡	QiA0
	H	H	H	H	↑	H	Σi‡	Fi0

MSB LSB
i ≡ 3, 2, 1, 0
Ai ≡ Data inputs
QiA ≡ Push-pop stack word A output (internal)
QiA0 ≡ the level of Qi before the indicated inputs conditions were established.

Fi ≡ Device outputs
Fi0 ≡ the level of Fi before the indicated input conditions were established.
Σi ≡ Adder outputs (internal)
*QiB, QiC, QiD do not change
†QiD0 → QiD, QiD0 → QiC, QiC0 → QiB, QiB0 → QiA
‡QiA0 → QiB, QiB0 → QiC, QiC0 → QiD

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push-pop stack control

The 4-word push-pop stack can be used for nesting up to four levels of program or return (link) addresses. In the load mode, the first (top) word is filled with new data from the output of the full adder, and no push occurs meaning that previous data at that location is lost. However, all other word locations in the push-pop stack remain unchanged. In the push mode, the new word is again entered in the first (top) location; however, previous data residing in the top three words are pushed down one word location and retained at their new locations. The bottom word is written over and lost.

In the pop mode, words in the push-pop stack move up one location on each clock transition. A unique function is provided by the bottom (fourth) register as its content is retained during the pop mode, and after 3 clock transitions, all words in the stack are filled with the operand/address that occupied the bottom register.

The operand/address will remain available indefinitely if stack functions are limited to the pop or hold modes.

The push-pop stack functions are shown in Tables II and III.

TABLE III. PUSH-POP STACK FUNCTIONS

	FUNCTION	SEL. S3	SEL. S4	REG. D	REG. C	REG. B	REG. A	INPUT/ OUTPUT
BIT 0	LOAD	L	H	QiD0	QiC0	QiB0	← Σi	Σi IN
BIT 1	PUSH	H	H	← QiC0	← QiB0	← QiA0	← Σi	Σi IN
BIT 2	POP	H	L	↶ → QiD0	→ QiD0	→ QiC0	→ QiB0	QiA OUT
BIT 3	HOLD	L	L	QiD0	QiC0	QiB0	QiA0	QiA OUT

μlink operations show previous data location after clock transition.

full adder

The four-function full adder is controllable from select inputs S1 and S2 to perform:

A or B incrementation, or decrementation of B

Unconditional jumps or relative offsets

No change

Return to zero or one

Incrementation can be implemented by forcing a carry (high) into the ALU. In this mode either of the following options are possible:

1. Increment (A plus zero plus carry)
2. Increment B (zero plus B plus carry), or decrement B (all highs at A then A plus B with carry input low and disregard, don't use, carry out)
3. Increment the jump or offset (A plus B plus carry)

full adder (continued)

4. Start at zero or one and increment on each clock (select zero plus zero plus carry, then select zero plus B plus carry), or set register to N and decrement B (see 2 above).
5. No change (carry input is always active and removal of carry combined with either the ALU or register hold mode will retain the current address).

Unconditional jumps can be implemented by applying and selecting the jump directly from the data inputs to the output register. Offset can be accomplished by summing the output register with the offset magnitude (A plus B) with carry low.

The ALU functions are shown in Table IV.

TABLE IV. ADDRESS CONTROL FUNCTIONS

INPUTS		INTERNAL
S1	S2	Σi
H	H	0 PLUS 0 PLUS C-in
H	L	0 PLUS Bi PLUS C-in
L	H	Ai PLUS 0 PLUS C-in
L	L	Ai PLUS Bi PLUS C-in

compound generator functions

As the function-select lines of the register sources, push-pop stack, and adder are independent, compound functions can be selected to occur on the next clock transition.

Subroutine branches and returns can be simplified by saving the return or link addresses in the push-pop stack. This branch-and-save function can be accomplished on the same clock time as follows:

DATA-IN	ADDER	PUSH-POP STACK	REGISTER SOURCE
Branch address	Zero plus B plus one (S1 = H, S2 = L)	Push (S3 = S4 = H)	Data-in (S5 = S6 = L)

Up to four branches can be made with the return stored in the 4-word push-pop stack.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54S482 . . . . . −55°C to 125°C
SN74S482 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1. All voltage values are with respect to network ground terminal.

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recommended operating conditions

		SN54S482			SN74S482			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	Carry output			−1			−1	mA
	Any F output			−2			−2	
Low-level output current, I_{OL}	Carry output			10			10	mA
	Any F output			16			16	
Setup time, t_{su}	Data-in, S5, S6	0↑			0↑			ns
	Data-in via adder	20↑			15↑			
	S1, S2	40↑			30↑			
	S3, S4	20↑			15↑			
	Clear-inactive state	0↑			0↑			
Pulse width, t_w	Clock (high or low)	50			30			ns
	Clear (low)	15			15			
Clock input rise time, t_r		20			25			ns
Hold time, t_h	Data-in, S5, S6	30↑			25↑			ns
	Data-in via adder	15↑			10↑			
	S1, S2	15↑			10↑			
	S3, S4	25↑			20↑			
Operating free-air temperature, T_A		−55		125	0	25	70	°C

↑The arrow indicates that the rising edge of the clock pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54S482			SN74S482			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = MAX	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = MAX			0.5			0.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	S1, S2, Cin	V_{CC} = MAX,	V_I = 2.7 V			50			50	μA
		S3, S4, S5, S6, clock					100			100	
		Clear					250			250	
		Any A					150			150	
I_{IL}	Low-level input current	S1, S2	V_{CC} = MAX,	V_I = 0.5 V			−1			−1	mA
		C-in					−0.8			−0.8	
		S3, S4					−1.2			−1.2	
		Any A, S5, S6, CK					−2			−2	
		Clear					−4			−4	
		Clock					−2.8			−2.8	
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−40		−110	−40		−110	mA
I_{CC}	Supply current		V_{CC} = MAX			90	130		90	140	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

switching characteristics over recommended operating ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	SN54S482			SN74S482			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	CLOCK	DATA OUT	C_L = 15 pF, R_L = 280 Ω		12	30		12	25	ns
t_{PHL}					15	30		15	25	
t_{PHL}	CLEAR	DATA OUT			12	25		12	20	ns
t_{PLH}	CARRY IN	CARRY OUT			12	22		12	18	ns
t_{PHL}					10	22		10	18	
t_{PLH}	DATA IN	CARRY OUT			17	30		17	25	ns
t_{PHL}					12	30		12	25	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

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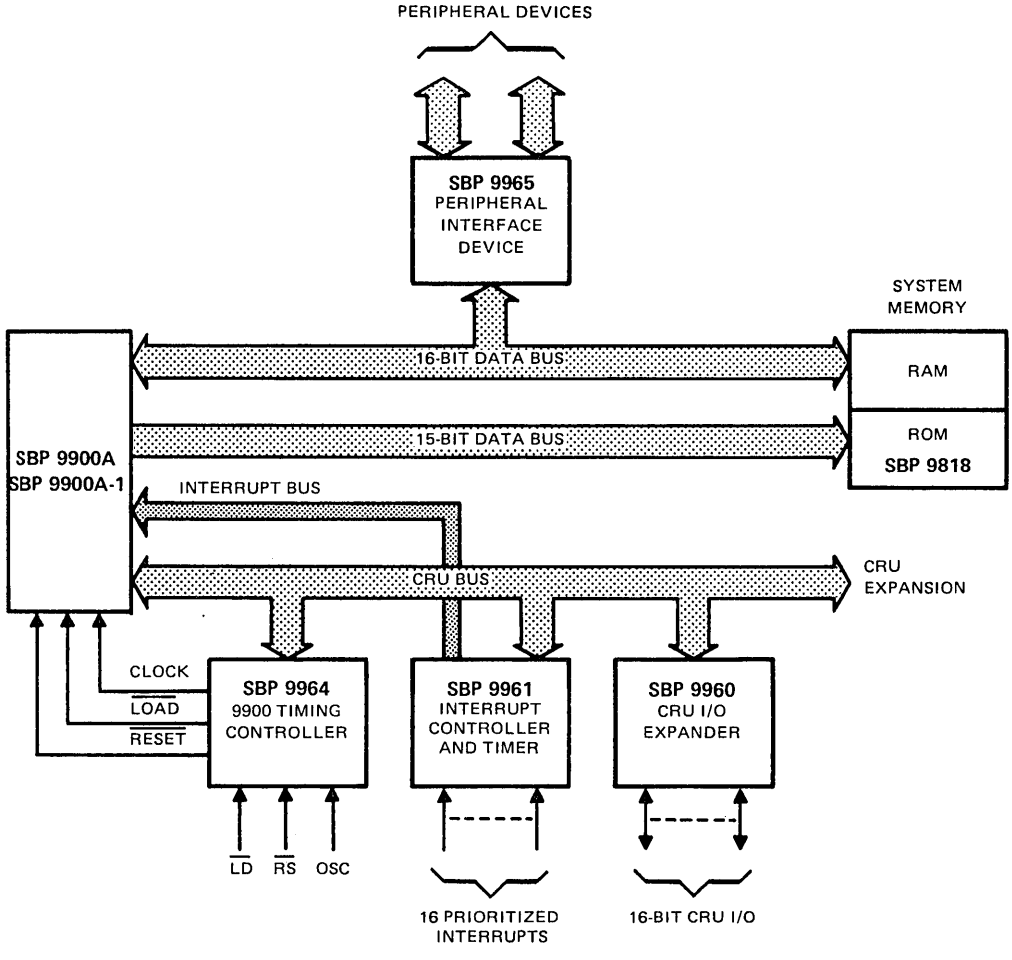
I^2L Microcomputer Components



I^2L MICROPROCESSOR SYSTEM

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SBP 9900A
SBP 9900A-1
Microprocessors

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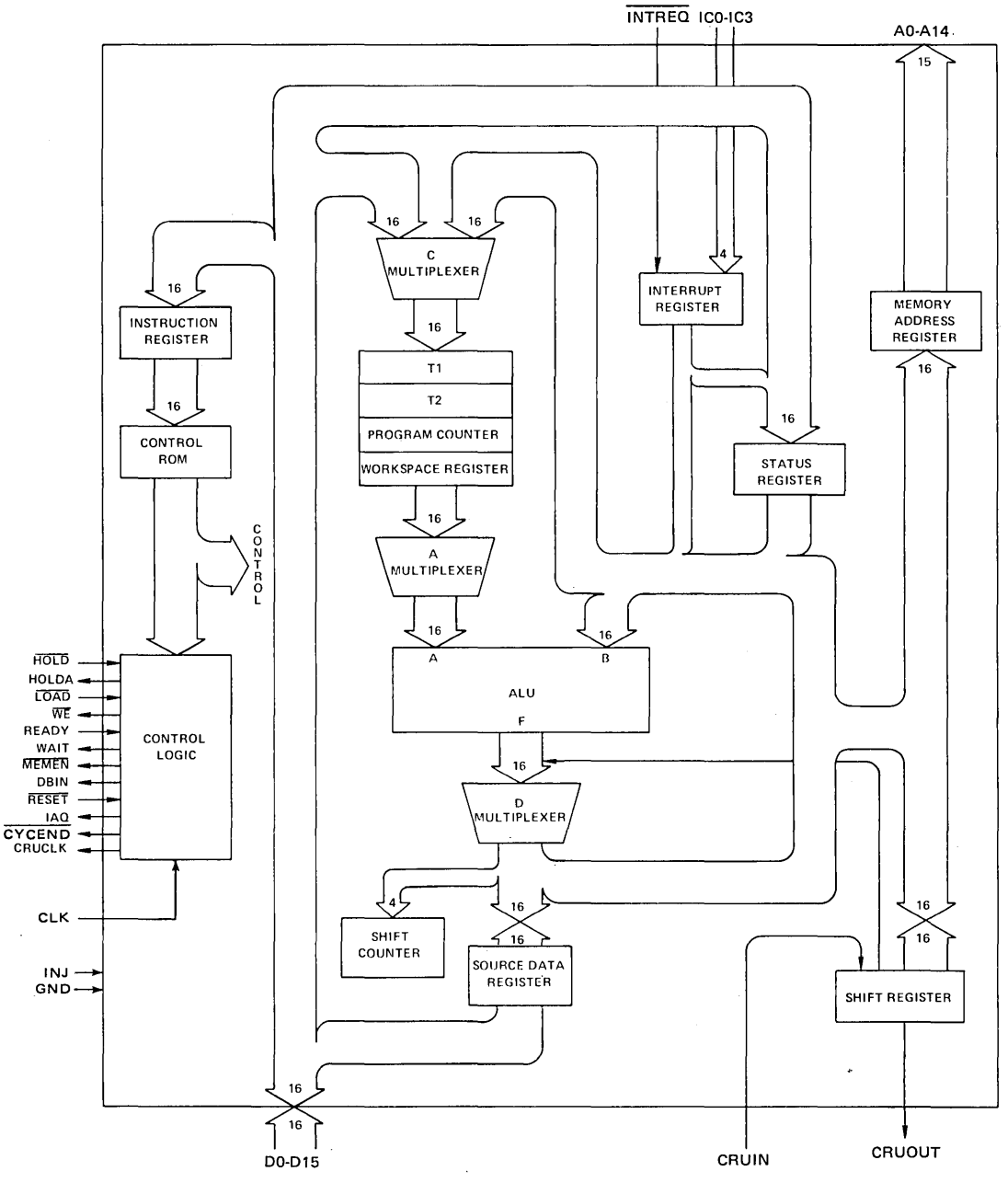


*References to SBP 9900A apply equally to the SBP 9900A-1 throughout this document except in 6.3 Switching Characteristics. SBP 9900A-1 complies with JAN specification MIL-M-38510/46001 and MIL-STD-883 processing.

FIGURE 1 – SBP 9900A AND SBP 9900A-1* ARCHITECTURE

1. INTRODUCTION

1.1 DESCRIPTION

The SBP 9900A microprocessor is a ruggedized monolithic Central Processing Unit (CPU) fabricated with Integrated Injection Logic (I^2L) technology. The SBP 9900A combines the properties of I^2L technology with a 16-bit word length, an advanced memory-to-memory architecture, and a full minicomputer instruction set to extend the end application reach of Texas Instruments 9900 microprocessor family into those applications requiring efficient, stable, reliable performance in severe operating environments. I^2L technology enables the SBP 9900A to operate over a very wide ambient temperature range from a dc power source. Static Logic is used throughout with directly TTL compatible I/O permitting use with standard logic and memory devices and thereby eliminating the need for special clock and interface functions. The SBP 9900A is software compatible with other 9900 microprocessor family members and shares a common body of hardware/software with Texas Instruments 990 minicomputer family. The SBP 9900A-1 continues all the advantages of the SBP 9900A with MIL-M-38512/46001 JAN qualification and MIL-STD-883 processing. In the following discussion all references to the SBP 9900A apply equally to the SBP 9900A-1 except in 6.3 Switching Characteristics.

1.2 KEY FEATURES

- Parallel 16-Bit Word Length
- Full Minicomputer Instruction Set Includes Multiply and Divide
- Directly Addresses Up to 65,536 Bytes/32,768 Words of Memory
- Advanced Memory-To-Memory Architecture
- Multiple 16-Word Register Files (Work Spaces) Reside in Memory
- Separate I/O, Memory and Interrupt Bus Structures
- 16 Prioritized Hardware Interrupts
- 16 Software Interrupts (XOPS)
- Programmed and DMA I/O Capability
- Serial I/O Via Communications-Register-Unit (CRU)
- 64-Pin Package
- Software Compatible with TI 9900 Microprocessor/9900 Minicomputer Family
- I^2L Technology:
  - 2.6 MHz Nominal Clock at 500 mW
  - Single dc Power Supply
  - Fully Static Operation
  - Single Phase Clock
  - Directly TTL Compatible I/O (Including Clock)
  - Operates Over Wide Temperature Range:
    - $-55^{\circ}C$ to $125^{\circ}C$ for SBP 9900AM, SBP 9900AN (883 B)
    - $-40^{\circ}C$ to $85^{\circ}C$ for SBP 9900AE
- SBP 9900A-1 Provided With MIL-M-38510 Qualification and MIL-STD-883 Processing

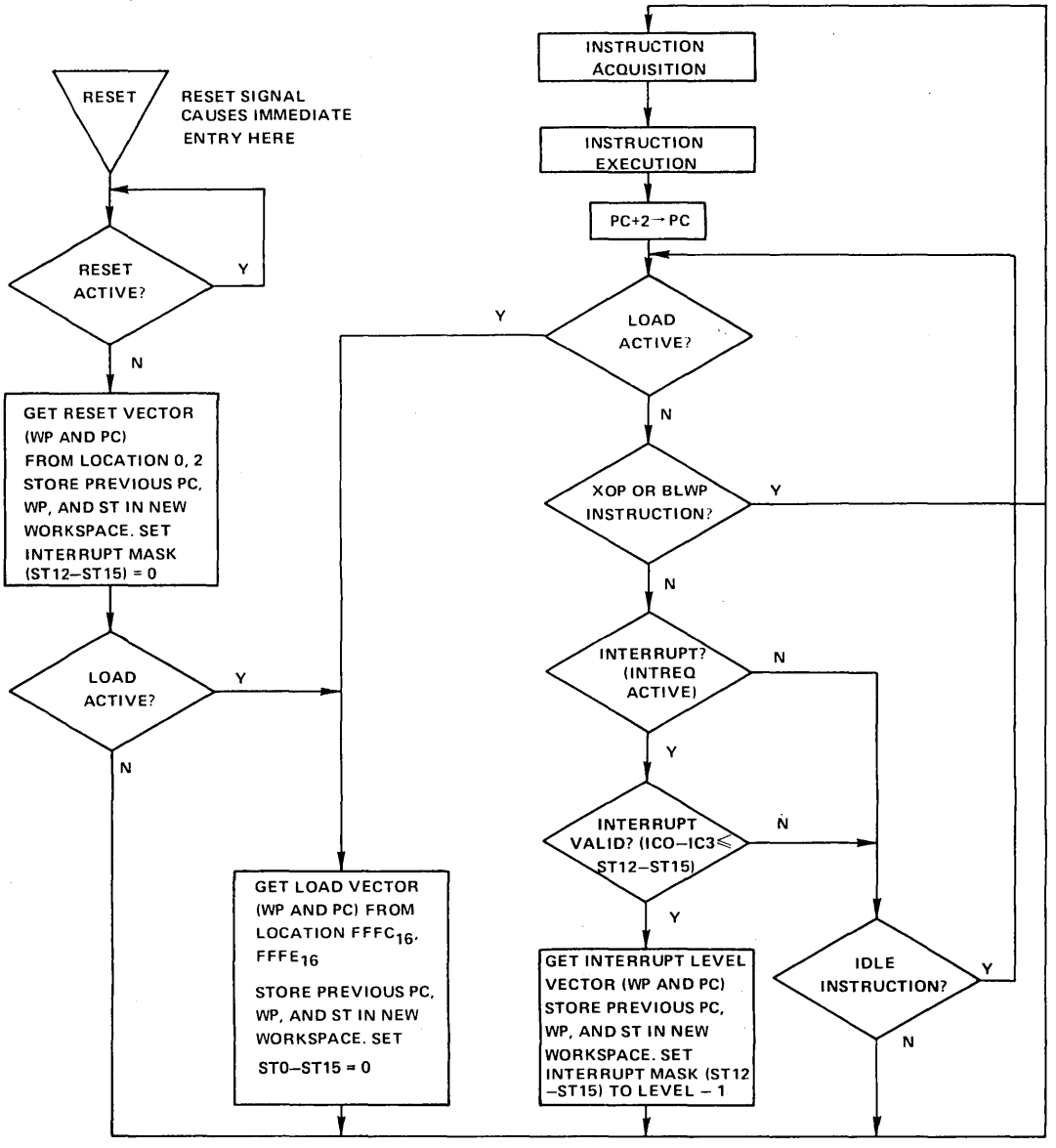


FIGURE 2 – 9900 CPU FLOW CHART

The SBP 9900A is a 16-bit processor with 69 instructions including byte and bit addressing. The 16-bit word is used to address 32K words or 65K bytes of memory. Processing power comes not only from the 16-bit word length, but also from eight powerful addressing modes and the use of memory as working registers. It is, in fact, this concept called the "Workspace Register" concept that is the most outstanding architectural feature of the SBP 9900A. In contrast to the pushdown stack found in many minicomputers and microprocessors, the workspace register file is a contiguous block of 16 words in memory used as working registers. Storage of intermediate results and subroutine return addresses, as well as index register functions, is accomplished in the workspace.

Most important of all is that each small routine, program or subroutine may have its own 16-word workspace. A workspace pointer (a 16-bit register within the arithmetic unit) points to the first word of the appropriate workspace for any given program. This is especially significant in systems where interrupt processing is used, or where multifunction applications require frequent changes of program context. When an interrupt occurs, for example, there is no need to save register contents and a return address in a stack or other block of memory, because they are all in the workspace. The Program Counter, Status Register, and Workspace Pointer (PC, ST, WP) are saved in three words of the workspace, the WP is set to a new value, pointing to the appropriate service routine, and processing resumes around a new set of workspace registers.

The primary impact of the workspace is to give the program designer 16 "working registers" for *every routine and subroutine;* and because the "registers" are actually memory words, there is no need to save and restore register contents when jumping from one routine to another.

Other important features of the SBP 9900A are vectored interrupts (16 levels), an asynchronous I/O bus, and a Communications Register Unit (CRU) to accommodate I/O circuit cards for a wide variety of peripherals and general interface requirements.

2. ARCHITECTURE

The memory word of the 9900 is 16 bits long. Each word is also defined as 2 bytes of 8 bits. The instruction set of the 9900 allows both word and byte operands. Thus, all memory locations are on even address boundaries and byte instructions can address either the even or odd byte. The memory space is 65,536 bytes or 32,768 words. The word and byte formats are shown in Figure 3.

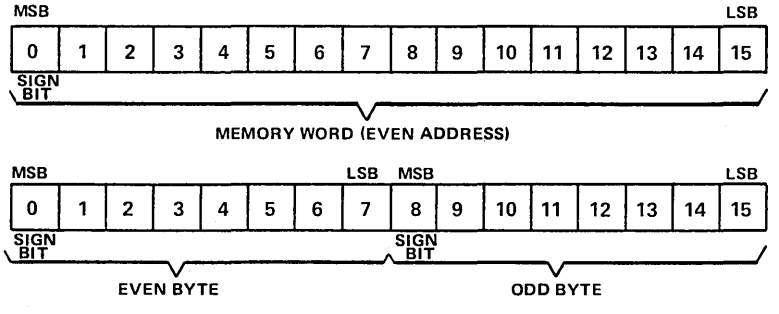


FIGURE 3 – WORD AND BYTE FORMATS

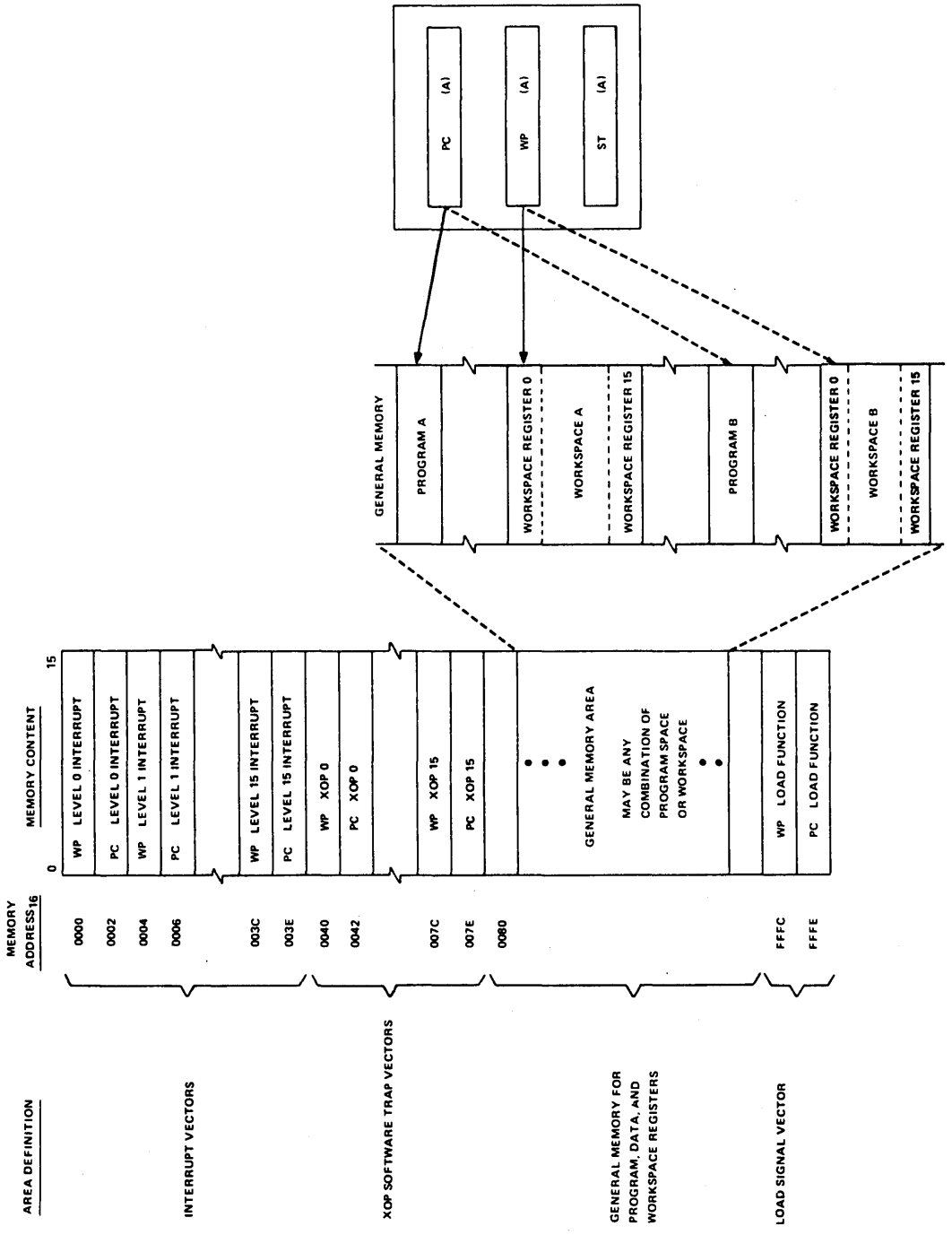


FIGURE 4 – MEMORY MAP AND WORKSPACE CONCEPT

2.1 REGISTERS AND MEMORY

The 9900 employs an advanced memory-to-memory architecture. The 9900 memory map is shown in Figure 4.

The first 32 words are used for interrupt trap vectors. The next contiguous block of 32 memory words is used by the extended operation (XOP) instruction for trap vectors. The last two memory words, $FFFC_{16}$ and $FFFE_{16}$, are used for the trap vector of the LOAD signal. The remaining memory is then available for programs, data, and workspace registers. If desired, any of the special areas may also be used as general memory.

Three internal registers are accessible to the user. The program counter (PC) contains the address of the instruction following the current instruction being executed. This address is referenced by the processor to fetch the next instruction from memory and is then automatically incremented. The status register (ST) contains the present state of the processor and will be further defined in Section 3.4. The workspace pointer (WP) contains the address of the first word in the currently active set of workspace registers.

A workspace-register file occupies 16 contiguous memory words in the general memory area (see Figure 4). Each workspace register may hold data or addresses and function as operand registers, accumulators, address registers, or index registers. During instruction execution, the processor addresses any register in the workspace by adding the register number to the contents of the workspace pointer and initiating a memory request for the word. The relationship between the workspace pointer and its corresponding workspace is shown in Figure 4.

The workspace concept is particularly valuable during operations that require a context switch which is a change from one program environment to another (as in the case of an interrupt) or to a subroutine. Such an operation, using a conventional multi-register arrangement, requires that at least part of the contents of the register file be stored and reloaded. A memory cycle is required to store or fetch each word. By exchanging the program counter, status register, and workspace pointer in the 9900 concept accomplishes a complete context switch withonly three store cycles and three fetch cycles. See Figure 4. After the switch the workspace pointer contains the starting address of a new 16-word workspace in memory for use in the new routine. A corresponding time saving occurs when the original context is restored. Instructions in the 9900 that result in a context switch include:

1. Branch and Load Workspace Pointer (BLWP)
2. Return from Subroutine (RTWP)
3. Extended Operation (XOP).

Device interrupts, $\overline{\text{RESET}}$, and $\overline{\text{LOAD}}$ also cause a context switch by forcing the processor to trap to a service subroutine.

2.2 INTERRUPTS

The 9900 employs 16 interrupt levels with the highest priority level 0 and lowest level 15. Level 0 is reserved for the $\overline{\text{RESET}}$ function and all other levels may be used for external devices. The external levels may also be shared by several device interrupts, depending upon system requirements.

The 9900 continuously compares the interrupt code (IC0 through IC3) with the interrupt mask contained in status-register bits 12 through 15. When the level of the pending interrupt is less than or equal to the enabling mask level (higher or equal priority interrupt), the processor recognizes the interrupt and initiates a context switch following completion of the currently executing instruction. The processor fetches the new context WP and PC from the interrupt vector locations. Then, the previous context WP, PC, and ST are stored in workspace registers 13, 14, and 15, respectively, of the new workspace. The 9900 then forces the interrupt mask to a value that is one less than

the level of the interrupt being serviced. This allows only interrupts of higher priority to interrupt a service routine. The processor also inhibits interrupts until the first instruction of the service routine has been executed. All interrupt requests should remain active until recognized by the processor in the device-service routine. The individual service routines must reset the interrupt requests before the routine is complete.

If a higher priority interrupt occurs, a second context switch occurs to service the higher priority interrupt. When that routine is complete, a return instruction (RTWP) restores the first service routine parameters to the processor to complete processing of the lower-priority interrupt. All interrupt subroutines should terminate with the return instruction to restore original program parameters. The interrupt-vector locations, device assignment, enabling-mask value, and the interrupt code are shown in Table 1.

TABLE 1
INTERRUPT LEVEL DATA

Interrupt Level	Vector Location (Memory Address In Hex)	Device Assignment	Interrupt Mask Values To Enable Respective Interrupts (ST12 thru ST15)	Interrupt Codes IC0 thru IC3
(Highest priority) 0	00	Reset	0 through F*	0000
1	04	External device	1 through F	0001
2	08	↓	2 through F	0010
3	0C	↓	3 through F	0011
4	10	↓	4 through F	0100
5	14	↓	5 through F	0101
6	18	↓	6 through F	0110
7	1C	↓	7 through F	0111
8	20	↓	8 through F	1000
9	24	↓	9 through F	1001
10	28	↓	A through F	1010
11	2C	↓	B through F	1011
12	30	↓	C through F	1100
13	34	↓	D through F	1101
14	38	↓	E and F	1110
(Lowest priority) 15	3C	External device	F only	1111

*Level 0 can not be disabled.

The 9900 interrupt interface utilizes standard TTL components as shown in Figure 5. Note that for eight or less external interrupts a single SN54/74148 is required and for one external interrupt $\overline{\text{INTREQ}}$ is used as the interrupt signal with a hard-wired code IC0 through IC3.

2.3 I/O INTERFACE COMMUNICATIONS-REGISTER-UNIT (CRU)

The SBP 9900A communications-register-unit (CRU) is a versatile, direct command-driven serial I/O interface. The CRU may directly address, in bit-fields of one to sixteen, up to 4096 peripheral input bits and up to 4096 peripheral output bits. The SBP 9900A executes three single-bit and two multiple-bit CRU instructions. The single-bit instructions include TEST BIT (TB), SET BIT TO ONE (SBO), and SET BIT TO ZERO (SBZ); the multiple-bit instructions include LOAD CRU (LDCR) and STORE CRU (STCR).

The SBP 9900A employs three dedicated I/O signals CRUIN, CRUOUT, CRUCLK, and the least significant twelve bits of the address but to support the CRU interface. CRU interface timing is shown in Section 2.9.

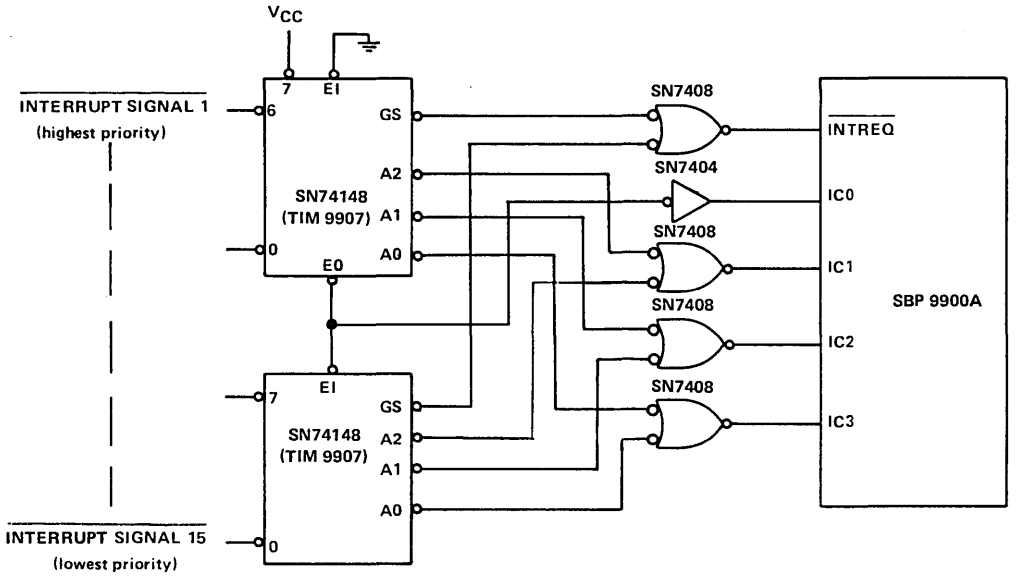


FIGURE 5 – SBP 9900A INTERRUPT INTERFACE

2.4 SINGLE-BIT CRU OPERATIONS

The 9900 performs three single-bit CRU functions: test bit (TB), set bit to one (SBO), and set bit to zero (SBZ). To identify the bit to be operated upon, the 9900 develops a CRU-bit address and places it on the address bus, A3 to A14.

For the two output operations (SBO and SBZ), the processor also generates a CRUCLK pulse, indicating an output operation to the CRU device, and places bit 7 of the instruction word on the CRUOUT line to accomplish the specified operation (bit 7 is a one for SBO and a zero for SBZ). A test-bit instruction transfers the addressed CRU bit from the CRUIN input line to bit 2 of the status register (EQUAL).

The 9900 develops a CRU-bit address for the single-bit operations from the CRU-base address contained in workspace register 12 and the signed displacement count contained in bits 8 through 15 of the instruction. The displacement allows two's complement addressing from base minus 128 bits through base plus 127 bits. The base address from W12 is added to the signed displacement specified in the instruction and the result is loaded onto the address bus. Figure 6 illustrates the development of a single-bit CRU address.

2.5 MULTIPLE-BIT CRU OPERATIONS

The 9900 performs two multiple-bit CRU operations: store communications register (STCR) and load communications register (LDCR). Both operations perform a data transfer from the CRU-to-memory or from memory-to-CRU as illustrated in Figure 8. Although the figure illustrates a full 16-bit transfer operation, any number of bits from 1 through 16 may be involved. The LDCR instruction fetches a word from memory and right-shifts it to serially transfer it to CRU output bits. If the LDCR involves eight or fewer bits, those bits come from the right-justified field within the addressed byte of the memory word. If the LDCR involves nine or more bits, those bits come from the right-justified field within the whole memory word. When transferred to the CRU interface, each successive bit receives an address that is sequentially greater than the address for the previous bit. This addressing mechanism results

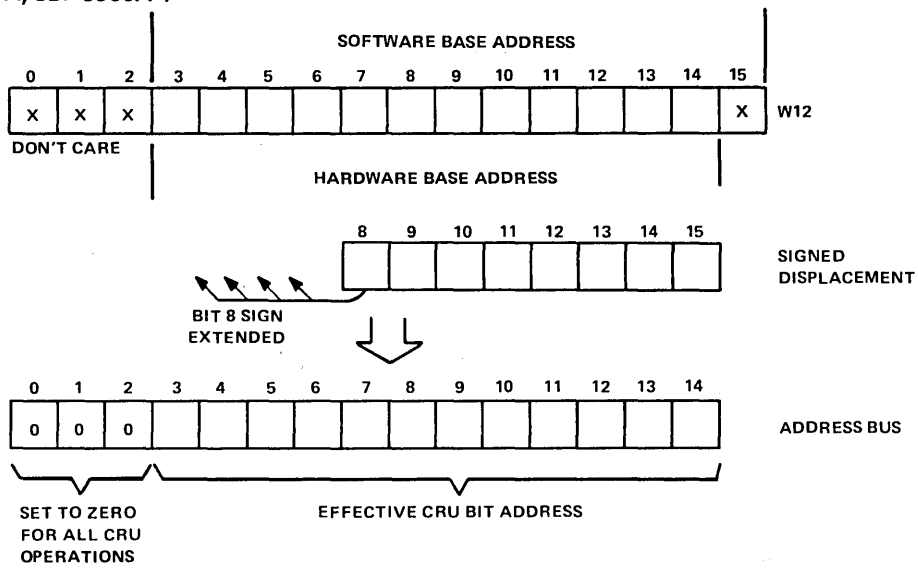


FIGURE 6 – 9900 SINGLE-BIT CRU ADDRESS DEVELOPMENT

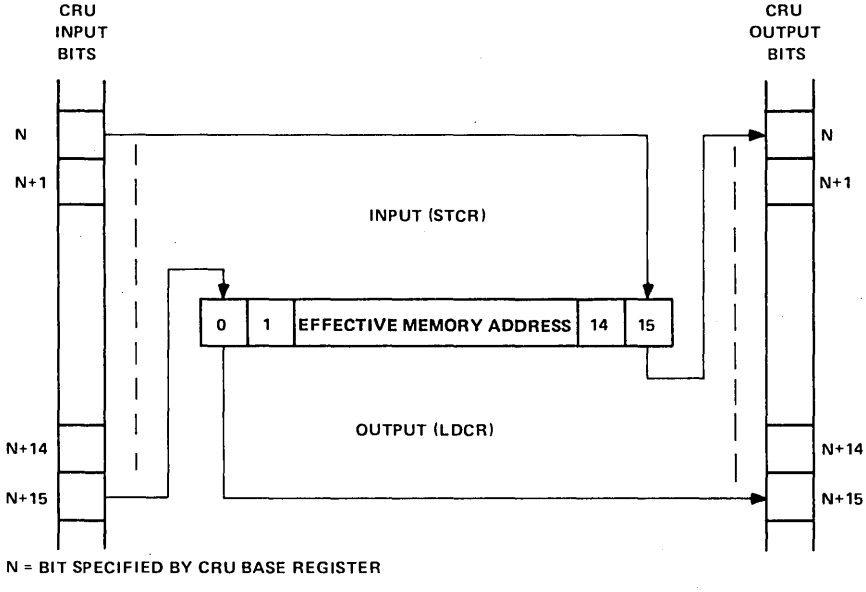


FIGURE 7 – 9900 LDCR/STCR DATA TRANSFERS

in an order reversal of the bits; that is, bit 15 of the memory word (or bit 7) becomes the lowest addressed bit in the CRU and bit 0 becomes the highest addressed bit in the CRU field.

An STCR instruction transfers data from the CRU to memory. If the operation involves a byte or less transfer, the transferred data will be stored right-justified in the memory byte with leading bits set to zero. If the operation involves from nine to 16 bits, the transferred data is stored right-justified in the memory word with leading bits set to

zero. When the input from the CRU device is complete, the first bit from the CRU is the least-significant-bit position in the memory word or byte.

Figure 8 illustrates how to implement a 16-bit input and a 16-bit output register in the CRU interface. CRU addresses are decoded as needed to implement up to 256 such 16-bit interface registers. In system application, however, only the exact number of interface bits needed to interface specific peripheral devices are implemented. It is not necessary to have a 16-bit interface register to interface an 8-bit device.

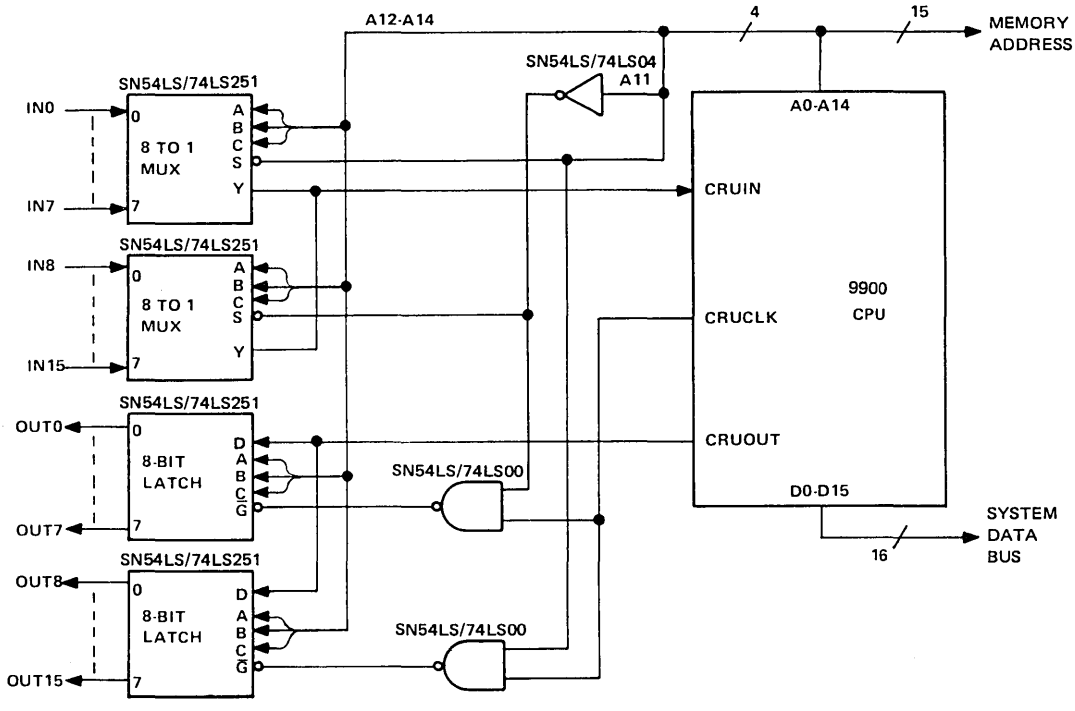


FIGURE 8 – 9900 16-BIT INPUT/OUTPUT INTERFACE

2.6 EXTERNAL INSTRUCTIONS

The 9900 has five external instructions that allow user-defined external functions to be initiated under program control. These instructions are CKON, CKOF, RSET, IDLE, and LREX. These mnemonics, except for IDLE, relate to functions implemented in the 990 minicomputer and do not restrict use of the instructions to initiate various user-defined functions. IDLE also causes the 9900 to enter the idle state and remain until an interrupt, $\overline{\text{RESET}}$, or $\overline{\text{LOAD}}$ occurs. When any of these five instructions are executed by the 9900, a unique 3-bit code appears on the most-significant 3 bits of the address bus (A0 through A2) along with a CRUCLK pulse. When the 9900 is in an idle state, the 3-bit code and CRUCLK pulses occur repeatedly until the idle state is terminated. The codes are shown in Table 2.

Figure 9 illustrates typical external decode logic to implement these instructions. Note that a signal is generated to inhibit CRU decodes during external instructions.

TABLE 2
EXTERNAL INSTRUCTIONS

EXTERNAL INSTRUCTION	A0	A1	A2
LREX	H	H	H
CKOF	H	H	L
CKON	H	L	H
RSET	L	H	H
IDLE	L	H	L

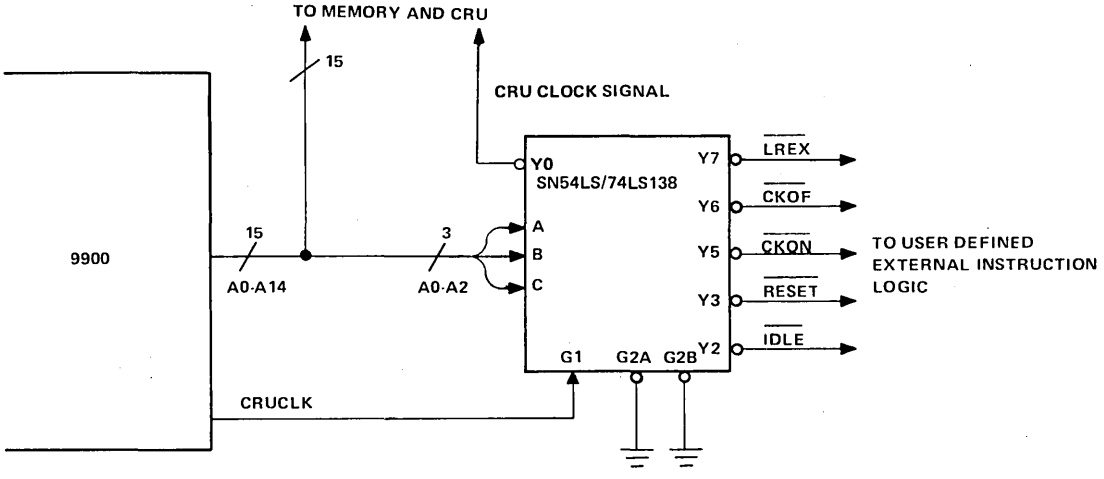


FIGURE 9 – EXTERNAL INSTRUCTION DECODE LOGIC

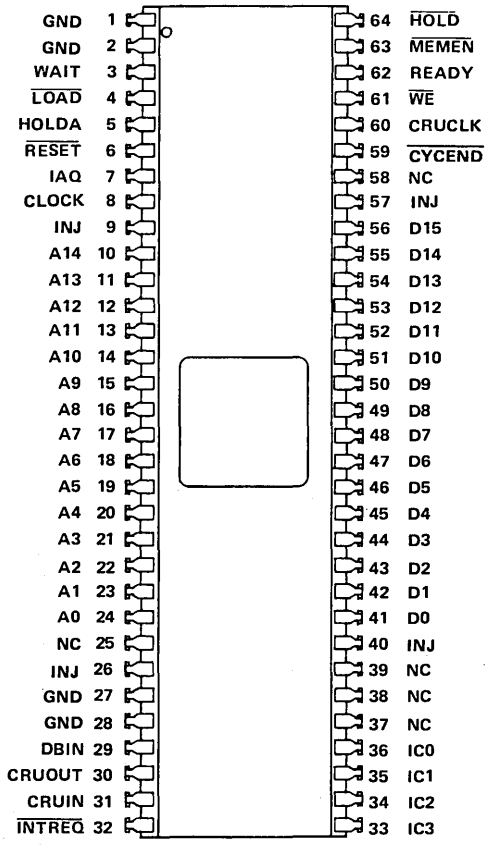
2.7 LOAD FUNCTION

The $\overline{\text{LOAD}}$ signal allows cold-start ROM loaders and front panels to be implemented for the 9900. When active, $\overline{\text{LOAD}}$ causes the 9900 to initiate an interrupt sequence immediately following the instruction being executed. Memory location FFFC is used to obtain the vector (WP and PC). The old PC, WP and ST are loaded into the new workspace and the interrupt mask is set to 0000. Then, program execution resumes using the new PC and WP.

2.8 SBP 9900A PIN DESCRIPTION

TABLE 3
9900 PIN ASSIGNMENTS AND FUNCTIONS

SIGNATURE	PIN	I/O	DESCRIPTION
			ADDRESS BUS
A0 (MSB)	24	OUT	A0 (MSB) through A14 (LSB) comprise the address bus. This open-collector bus provides the memory-address vector to the external-memory system when $\overline{\text{MEMEN}}$ is active, and I/O-bit addresses to the I/O system when $\overline{\text{MEMEN}}$ is inactive. When HOLDA is active, the address bus is pulled to the logic level HIGH state by the individual pull-up resistors tied to each respective open-collector output.
A14 (LSB)	10	OUT	
			DATA BUS
D0 (MSB)	41	I/O	D0 (MSB) through D15 (LSB) comprise the bidirectional open-collector data bus. This bus transfers memory data to (when writing) and from (when reading) the external-memory system when $\overline{\text{MEMEN}}$ is active. When HOLDA is active, the data bus is pulled to the logic level HIGH state by the individual pull-up resistors tied to each respective open-collector output.
D15 (LSB)	56	I/O	
			POWER SUPPLY
INJ	9		Injector-Supply-Current
INJ	26		Injector-Supply-Current
INJ	40		Injector-Supply-Current
INJ	57		Injector-Supply-Current
GND	1		Ground Reference
GND	2		Ground Reference
GND	27		Ground Reference
GND	28		Ground Reference
			CLOCK
CLOCK	8	IN	CLOCK
			BUS CONTROL
DBIN	29	OUT	DATA BUS IN. When active (pulled to logic level HIGH), DBIN indicates that the SBP 9900 has disabled its output buffers to allow the memory to place memory-read data on the data bus during $\overline{\text{MEMEN}}$. DBIN remains at logic level LOW in all other cases except when HOLDA is active (pulled to logic level HIGH).
$\overline{\text{MEMEN}}$	63	OUT	MEMORY ENABLE. When active (logic level LOW), $\overline{\text{MEMEN}}$ indicates that the address bus contains a memory address.
$\overline{\text{WE}}$	61	OUT	WRITE ENABLE. When active (logic level LOW), $\overline{\text{WE}}$ indicates that the SBP 9900A data bus is outputting data to be written into memory.



NC—No internal connection

TABLE 3 (CONTINUED)

SIGNATURE	PIN	I/O	DESCRIPTION
CRUCLK	60	OUT	COMMUNICATIONS-REGISTER-UNIT (CRU) CLOCK. When active (pulled to logic level HIGH), CRUCLK indicates to the external interface logic the presence of output data on CRUOUT, or the presence of an encoded external instruction on A0 through A2.
CRUIN	31	IN	CRU DATA IN. CRUIN, normally driven by 3-state or open-collector devices, receives input data from the external interface logic. When the SBP 9900A executes a STCR or TB instruction, it samples CRUIN for the level of the CRU input bit specified by the address bus (A3 through A14).
CRUOUT	30	OUT	CRU DATA OUT. CRUOUT ouputs serial data when the SBP 9900A executes a LDCR, SBZ, SBO instruction. The data on CRUOUT should be sampled by the external interface logic when CRUCLK goes active (pulled to logic level HIGH).
			INTERRUPT CONTROL
$\overline{\text{INTREQ}}$	32	IN	INTERRUPT REQUEST. When active (logic level LOW), $\overline{\text{INTREQ}}$ indicates that an external interrupt is requesting service. If $\overline{\text{INTREQ}}$ is active, the SBP 9900A loads the data on the interrupt-code input lines IC0 through IC3 into the internal interrupt-code storage register. The code is then compared to the interrupt mask bits of the status register. If equal or higher priority than the enabled interrupt level (interrupt code equal or less than status register bits 12 through 15), the SBP 9900A initiates the interrupt sequence. If the comparison fails, the SBP 9900A ignores the interrupt request. In that case, $\overline{\text{INTREQ}}$ should be held active. The SBP 9900A will continue to sample IC0 through IC3 until the program enables a sufficiently low interrupt level to accept the requesting interrupt.
IC0 (MSB)	36	IN	INTERRUPT CODES. IC0 (MSB) through IC3 (LSB), receiving an interrupt identity code, are sampled by the SBP 9900A when $\overline{\text{INTREQ}}$ is active (logic level LOW). When IC0 through IC3 are LLLH, the highest priority *external* interrupt is requesting service; when HHHH, the lowest priority external interrupt is requesting service.
IC3 (LSB)	33	IN	
			MEMORY CONTROL
$\overline{\text{HOLD}}$	64	IN	When active (logic level LOW), $\overline{\text{HOLD}}$ indicates to the SBP 9900A that an external controller (e.g., DMA device) desires to use both the address bus and data bus to transfer data to or from memory. In response, the SBP 9900A enters the hold state after completion of its present memory cycle. The SBP 9900A then allows its address bus, data bus, $\overline{\text{WE}}$, $\overline{\text{MEMEN}}$, DBIN, and HOLDA facilities to be pulled to the logic level HIGH state. When $\overline{\text{HOLD}}$ is deactivated, the SBP 9900A returns to normal operation from the point at which it was stopped.
HOLDA	5	OUT	HOLD ACKNOWLEDGE. When active (pulled to logic level HIGH), HOLDA indicates that the SBP 9900A is in the hold state and that its address bus, data bus, $\overline{\text{WE}}$, $\overline{\text{MEMEN}}$, and DBIN facilities are pulled to the logic level HIGH state.
READY	62	IN	When active (logic level HIGH), READY indicates that the memory will be ready to read or write during the next clock cycle. When not-ready is indicated during a memory operation, the SBP 9900A enters a wait state and suspends internal operation until the memory systems activate READY.
WAIT	3	OUT	When active (pulled to logic level HIGH), WAIT indicates that the SBP 9900A has entered a wait state in response to a not-ready condition from memory.
			TIMING AND CONTROL
IAQ	7	OUT	INSTRUCTION ACQUISITION. IAQ is active (pulled to logic level HIGH) during any SBP 9900A initiated instruction acquisition memory cycle. Consequently, IAQ may be used to facilitate detection of illegal op codes.
$\overline{\text{CYCEND}}$	59	OUT	CYCLE END. When active (logic level LOW), $\overline{\text{CYCEND}}$ indicates that the SBP 9900A will initiate a new machine cycle on the low-to-high transition of the next CLOCK.
$\overline{\text{LOAD}}$	4	IN	When active (logic level LOW), $\overline{\text{LOAD}}$ causes the SBP 9900A to execute a nonmaskable interrupt with memory addresses $FFFC_{16}$ and $FFFE_{16}$ containing the associated trap vectors (WP and PC). The load sequence is initiated after the instruction being executed is completed. $\overline{\text{LOAD}}$ will also terminate an idle state. If $\overline{\text{LOAD}}$ is active during the time $\overline{\text{RESET}}$ is active, the $\overline{\text{LOAD}}$ trap will occur after the $\overline{\text{RESET}}$ function is completed. $\overline{\text{LOAD}}$ should remain active for one instruction execution period (IAQ may be

TABLE 3 (CONCLUDED)

SIGNATURE	PIN	I/O	DESCRIPTION
$\overline{\text{LOAD}}$ (Cont.)			used to monitor instruction boundaries). $\overline{\text{LOAD}}$ may be used to implement cold-start ROM loaders. Additionally, front-panel routines may be implemented using CRU bits as front-panel-interface signals, and software-control routines to direct the panel operations.
$\overline{\text{RESET}}$	6	IN	When active (logic level LOW), $\overline{\text{RESET}}$ causes the SBP 9900A to reset itself and inhibit $\overline{\text{WE}}$ and CRUCLK. When $\overline{\text{RESET}}$ is released, the SBP 9900A initiates a level-zero interrupt sequence acquiring the WP and PC trap vectors from memory locations 0000_{16} and 0002_{16}, sets all status register bits to logic level LOW, and then fetches the first instruction of the reset program environment. $\overline{\text{RESET}}$ must be held active for a minimum of three CLOCK cycles.

2.9 SBP 9900A TIMING

2.9.1 SBP 9900A MEMORY

The SBP 9900A basic memory timing for a memory-read cycle with no wait states and for a memory-write cycle with one wait state is as shown in Figure 10. During each memory-read or memory-write, $\overline{\text{MEMEN}}$ becomes active (logic level LOW) along with valid memory-address data appearing on the address bus (A0 through A14).

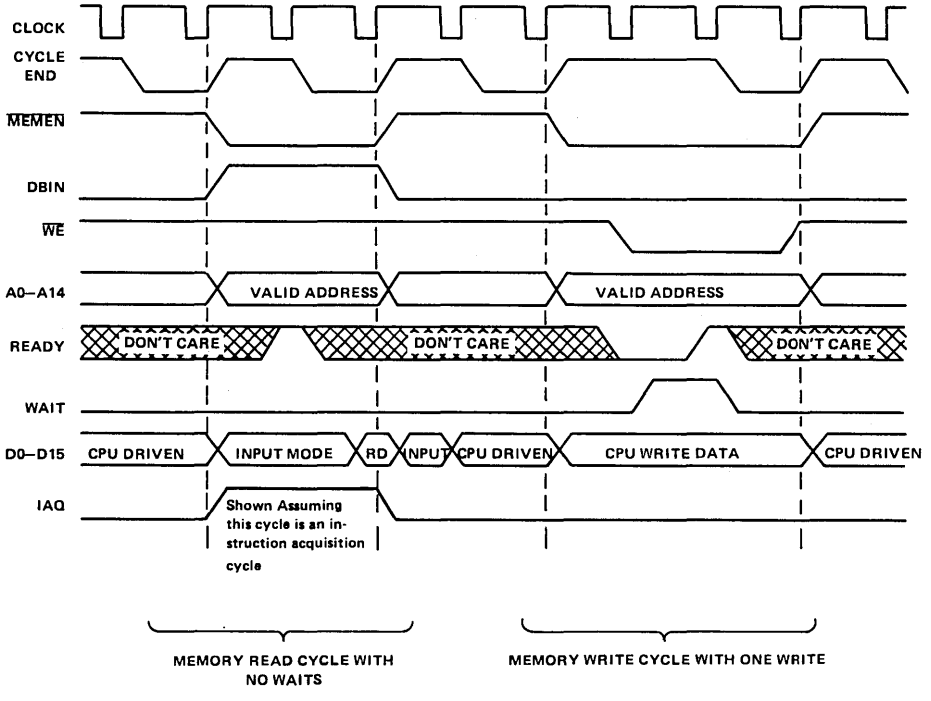


FIGURE 10 – SBP 9900A MEMORY BUS TIMING

In the case of a memory-read cycle, DBIN becomes active (pulled to logic level HIGH) at the same time memory-address data becomes valid; the memory write strobe $\overline{WE}$ remains inactive (pulled to logic level HIGH). If the memory-read cycle is initiated for acquisition of an instruction, IAQ becomes active (pulled to logic level HIGH) at the same time $\overline{MEMEN}$ becomes active. At the end of a memory-read cycle, $\overline{MEMEN}$ and DBIN together become inactive. At that time, though the address may change, the data bus remains in the input mode until terminated by the next high-to-low transition of the clock.

In the case of a memory-write cycle, $\overline{WE}$ becomes active (logic level LOW) with the first high-to-low transition of the clock after $\overline{MEMEN}$ becomes active; DBIN remains inactive. At the end of a memory-write cycle, $\overline{WE}$ and $\overline{MEMEN}$ together become inactive.

During either a memory-read or a memory-write operation, READY may be used to extend the duration of the associated memory cycle such that the speed of the memory system may be coordinated with the speed of the SBP 9900. If READY is inactive (logic level LOW) during the first low-to-high transition of the clock after $\overline{MEMEN}$ becomes active, the SBP 9900A will enter a wait state suspending further progress of the memory cycle. The first low-to-high transistion of the clock after READY becomes active terminates the wait state and allows normal completion of the memory cycle.

2.9.2 SBP 9900A HOLD

The hold facilities allow both the SBP 9900A and external devices to share a common memory. To gain memory-bus control, an external device requiring direct memory access (DMA) sends a hold request ($\overline{HOLD}$) to the SBP 9900A. When the next available non-memory cycle occurs, the SBP 9900A enters a hold state and signals its surrender of the memory-bus to the external device via a hold acknowledge (HOLDA). Receiving the hold acknowledgement, the external device proceeds to utilize the common memory. After its memory requirements have been satisfied, the external device returns memory-bus control to the SBP 9900A by releasing $\overline{HOLD}$.

When $\overline{HOLD}$ becomes active (logic level LOW), the SBP 9900A enters a hold state at the beginning of the next available non-memory cycle as shown below. Upon entering a hold state, HOLDA becomes active (pulled to logic level HIGH) with the following signals pulled to a HIGH logic level by the individual pull-up resistors tied to each respective open-collector output: DBIN, $\overline{MEMEN}$, $\overline{WE}$, A0 through A14, and D0 through D15. When $\overline{HOLD}$ becomes inactive, the SBP 9900A exits the hold state and regains memory-bus control. If $\overline{HOLD}$ becomes active during a CRU operation, the SBP 9900A uses an extra clock cycle after the deactivation of $\overline{HOLD}$ to reassert the CRU address thereby providing the normal setup time for the CRU-bit transfer.

2.9.3 SBP 9900A CRU

The transfer of two data-bits from memory to a peripheral CRU device and the transfer of one data-bit from a peripheral CRU device memory are shown in Figure 12. To transfer a data-bit to a peripheral CRU device, the SBP 9900A outputs the corresponding CRU-bit-address on address bus bits A3 through A14 and the respective data-bit on CRUOUT. During the second clock cycle of the operation, the SBP 9900A outputs a pulse, on CRUCLK, indicating to the peripheral CRU device the presence of a data-bit. This process is repeated until transfer of the entire field of data-bits specified by the CRU instruction has been accomplished. To transfer a data-bit from a peripheral CRU device, the SBP 9900A outputs the corresponding CRU-bit-address on address bus bits A3 through A14 and receives the respective data-bit on CRUIN. No CRUCLK pulses occur during a CRU input operation.

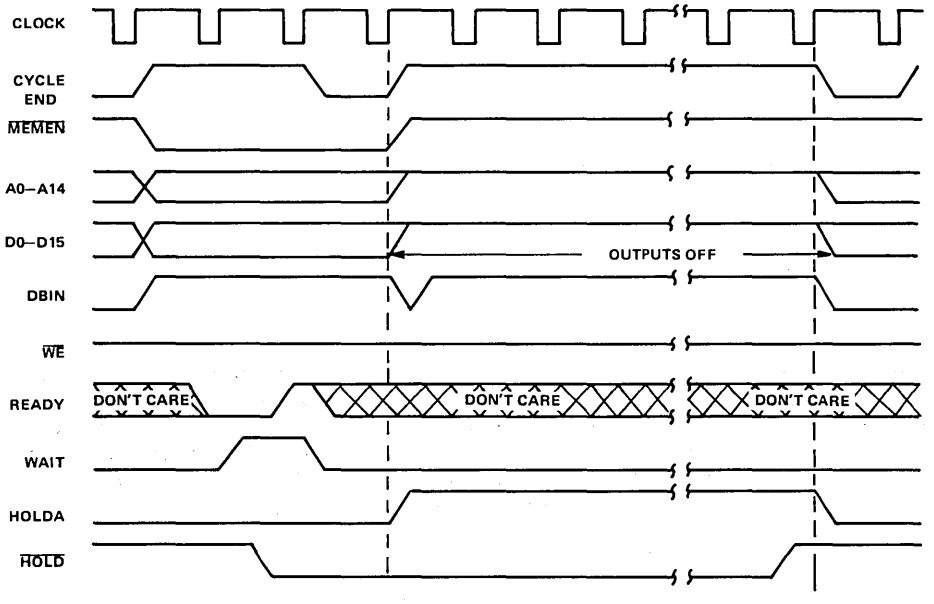


FIGURE 11 – SBP 9900A HOLD TIMING

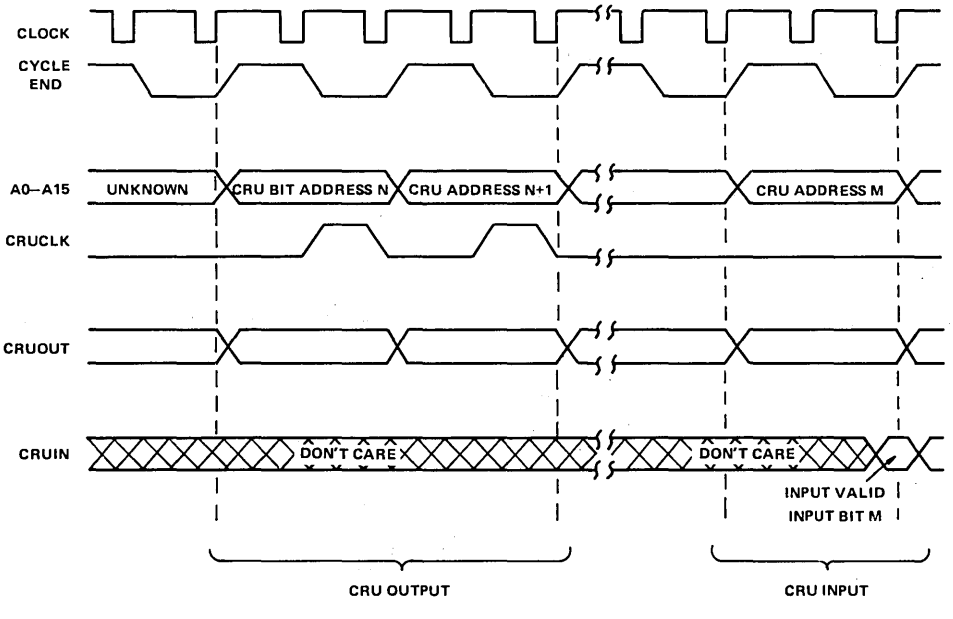


FIGURE 12 – SBP 9900A CRU INTERFACE TIMING

3. 9900 INSTRUCTION SET

3.1 DEFINITION

Each 9900 instruction performs one of the following operations:

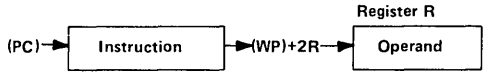
- Arithmetic, logical, comparison, or manipulation operations on data
- Loading or storage of internal registers (program counter, workspace pointer, or status)
- Data transfer between memory and external devices via the CRU
- Control functions.

3.2 ADDRESSING MODES

The 9900 instructions contain a variety of available modes for addressing random-memory data (e.g., program parameters and flags), or formatted memory data (character strings, data lists, etc.). The following figures graphically describe the derivation of the effective address for each addressing mode. The applicability of addressing modes to particular instructions is described in Section 3.5 along with the description of the operations performed by the instruction. The symbols following the names of the addressing modes [R, *R, *R+, @ LABEL, or @ TABLE (R)] are the general forms used by 9900 assemblers to select the addressing mode for register R.

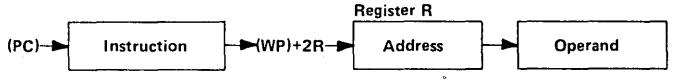
3.2.1 WORKSPACE REGISTER ADDRESSING R

Workspace Register R contains the operand.



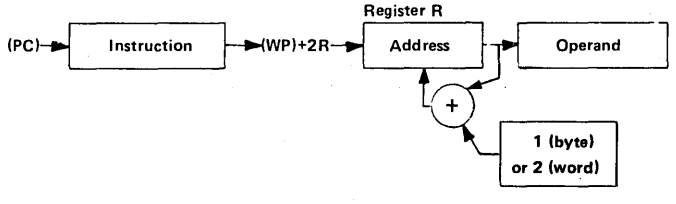
3.2.2 WORKSPACE REGISTER INDIRECT ADDRESSING *R

Workspace Register R contains the address of the operand.



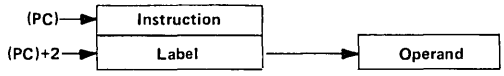
3.2.3 WORKSPACE REGISTER INDIRECT AUTO INCREMENT ADDRESSING *R+

Workspace Register R contains the address of the operand. After acquiring the operand, the contents of workspace register R are incremented.



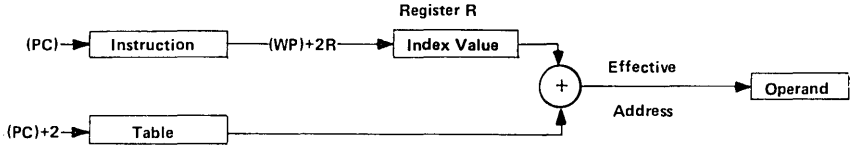
3.2.4 SYMBOLIC (DIRECT) ADDRESSING @ LABEL

The word following the instruction contains the address of the operand.



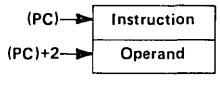
3.2.5 INDEXED ADDRESSING @ TABLE (R)

The word following the instruction contains the base address. Workspace register R contains the index value. The sum of the base address and the index value results in the effective address of the operand.



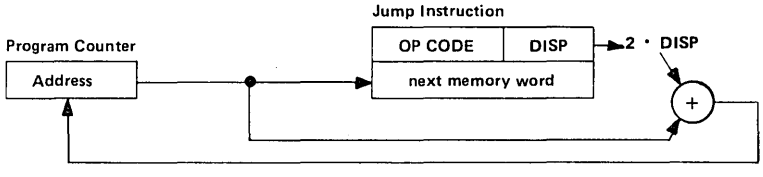
3.2.6 IMMEDIATE ADDRESSING

The word following the instruction contains the operand.



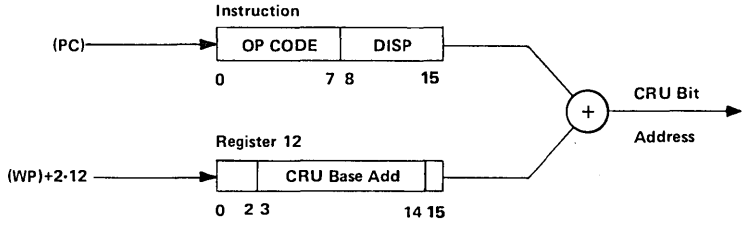
3.2.7 PROGRAM COUNTER RELATIVE ADDRESSING

The 8-bit signed displacement in the right byte (bits 8 through 15) of the instruction is multiplied by 2 and added to the updated contents of the program counter. The result is placed in the PC.



3.2.8 CRU RELATIVE ADDRESSING

The 8-bit signed displacement in the right byte of the instruction is added to the CRU base address (bits 3 through 14 of the workspace register 12). The result is the CRU address of the selected CRU bit.



3.3 TERMS AND DEFINITIONS

The terms used in describing the instructions of the 9900 are defined in Table 4.

TABLE 4
TERM DEFINITIONS

TERM	DEFINITION
B	Byte indicator (1=byte, 0 = word)
C	Bit count
D	Destination address register
DA	Destination address
IOP	Immediate operand
LSB(n)	Least significant (right most) bit of (n)
MSB(n)	Most significant (left most) bit of (n)
N	Don't care
PC	Program counter
Result	Result of operation performed by instruction
S	Source address register
SA	Source address
ST	Status register
STn	Bit n of status register
T_D	Destination address modifier
T_S	Source address modifier
WR	Workspace register (working register)
WRn	Workspace register n
(n)	Contents of n
a → b	a is transferred to b
|n|	Absolute value of n
+	Arithmetic addition
–	Arithmetic subtraction
AND	Logical AND
OR	Logical OR
⊕	Logical exclusive OR
$\overline{n}$	Logical complement of n

3.4 STATUS REGISTER

The status register contains the interrupt mask level and information pertaining to the instruction operation. Table 5 explains the bit indications.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
ST0	ST1	ST2	ST3	ST4	ST5	ST6	not used (=0)					ST12	ST13	ST14	ST15
L>	A>	=	C	O	P	X						Interrupt Mask			

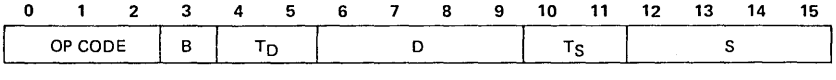
TABLE 5
STATUS REGISTER BIT DEFINITIONS

BIT	NAME	INSTRUCTION	CONDITION TO SET BIT TO 1
ST0	LOGICAL GREATER THAN	C,CB	If MSB(SA) = 1 and MSB(DA) = 0, or if MSB(SA) = MSB(DA) and MSB of [(DA)-(SA)] = 1
		CI	If MSB(WR) = 1 and MSB of IOP = 0, or if MSB(WR) = MSB of IOP and MSB of [IOP-(WR)] = 1
		ABS	If (SA) ≠ 0
		All Others	If result ≠ 0
ST1	ARITHMETIC GREATER THAN	C,CB	If MSB(SA) = 0 and MSB(DA) = 1, or if MSB(SA) = MSB(DA) and MSB of [(DA)-(SA)] = 1
		CI	If MSB(WR) = 0 and MSB of IOP = 1, or if MSB(WR) = MSB of IOP and MSB of [IOP-(WR)] = 1
		ABS	If MSB(SA) = 0 and (SA) ≠ 0
		All Others	If MSB of result = 0 and result ≠ 0
ST2	EQUAL	C, CB	If (SA) = (DA)
		C1	If (WR) = IOP
		COC	If (SA) and $\overline{(DA)}$ = 0
		CZC	If (SA) and (DA) = 0
		TB	If CRUIN = 1
		ABS	If (SA) = 0
		All Others	If result = 0
ST3	CARRY	A, AB, ABS, AI, DEC, DECT, INC, INCT, NEG, S, SB	If CARRY OUT = 1
		SLA, SRA, SRC, SRL	If last bit shifted out = 1
ST4	OVERFLOW	A, AB	If MSB(SA) = MSB(DA) and MSB of result ≠ MSB(DA)
		AI	If MSB(WR) = MSB of IOP and MSB of result ≠ MSB(WR)
		S, SB	If MSB(SA) ≠ MSB(DA) and MSB of result ≠ MSB(DA)
		DEC, DECT	If MSB(SA) = 1 and MSB of result = 0
		INC, INCT	If MSB(SA) = 0 and MSB of result = 1
		SLA	If MSB changes during shift
		DIV	If MSB(SA) = 0 and MSB(DA) = 1, or if MSB(SA) = MSB(DA) and MSB of [(DA)-(SA)] = 0
		ABS, NEG	If (SA) = 8000_{16}
ST5	PARITY	CB, MOVB	If (SA) has odd number of 1's
		LDCR, STCR	If 1 ≤ C ≤ 8 and (SA) has odd number of 1's
		AB, SB, SOCB, SZCB	If result has odd number of 1's
ST6	XOP	XOP	If XOP instruction is executed
ST12–ST15	INTERRUPT MASK	LIMI	If corresponding bit of IOP is 1
		RTWP	If corresponding bit of WR15 is 1

3.5 INSTRUCTIONS

3.5.1 Dual Operand Instructions with Multiple Addressing Modes for Source and Destination Operand

General format:



If B = 1 the operands are bytes and the operand addresses are byte addresses. If B = 0 the operands are words and the operand addresses are word addresses.

The addressing mode for each operand is determined by the T field of that operand.

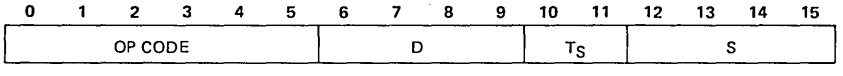
T_S OR T_D	S OR D	ADDRESSING MODE	NOTES
00	0, 1, . . . 15	Workspace register	1
01	0, 1, . . . 15	Workspace register indirect	
10	0	Symbolic	4
10	1, 2, . . . 15	Indexed	2,4
11	0, 1, . . . 15	Workspace register indirect auto-increment	3

NOTES: 1. When a workspace register is the operand of a byte instruction (bit 3 = 1), the left byte (bits 0 through 7) is the operand and the right byte (bits 8 through 15) is unchanged.
2. Workspace register 0 may not be used for indexing.
3. The workspace register is incremented by 1 for byte instructions (bit 3 = 1) and is incremented by 2 for word instructions (bit 3 = 0).
4. When $T_S = T_D = 10$, two words are required in addition to the instruction word. The first word is the source operand base address and the second word is the destination operand base address.

MNEMONIC	OP CODE 0 1 2	B 3	MEANING	RESULT COMPARED TO 0	STATUS BITS AFFECTED	DESCRIPTION
A	1 0 1	0	Add	Yes	0-4	(SA)+(DA) → (DA)
AB	1 0 1	1	Add bytes	Yes	0-5	(SA)+(DA) → (DA)
C	1 0 0	0	Compare	No	0-2	Compare (SA) to (DA) and set appropriate status bits
CB	1 0 0	1	Compare bytes	No	0-2,5	Compare (SA) to (DA) and set appropriate status bits
S	0 1 1	0	Subtract	Yes	0-4	(DA) – (SA) → (DA)
SB	0 1 1	1	Subtract bytes	Yes	0-5	(DA) – (SA) → (DA)
SOC	1 1 1	0	Set ones corresponding	Yes	0-2	(DA) OR (SA) → (DA)
SOCB	1 1 1	1	Set ones corresponding bytes	Yes	0-2,5	(DA) OR (SA) → (DA)
SZC	0 1 0	0	Set zeroes corresponding	Yes	0-2	(DA) AND ($\overline{SA}$) → (DA)
SZCB	0 1 0	1	Set zeroes corresponding bytes	Yes	0-2,5	(DA) AND ($\overline{SA}$) → (DA)
MOV	1 1 0	0	Move	Yes	0-2	(SA) → (DA)
MOVB	1 1 0	1	Move bytes	Yes	0-2,5	(SA) → (DA)

3.5.2 Dual Operand Instructions with Multiple Addressing Modes for the Source Operand and Workspace Register Addressing for the Destination

General format:



The addressing mode for the source operand is determined by the T_S field.

T_S	S	ADDRESSING MODE	NOTES
00	0, 1, . . . 15	Workspace register	
01	0, 1, . . . 15	Workspace register indirect	
10	0	Symbolic	
10	1, 2, . . . 15	Indexed	1
11	0, 1, . . . 15	Workspace register indirect auto increment	2

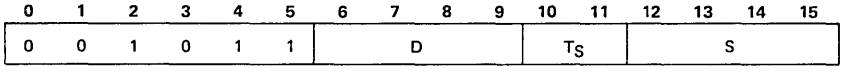
NOTES: 1. Workspace register 0 may not be used for indexing.
2. The workspace register is incremented by 2.

MNEMONIC	OP CODE 0 1 2 3 4 5	MEANING	RESULT COMPARED TO 0	STATUS BITS AFFECTED	DESCRIPTION
COC	0 0 1 0 0 0	Compare ones corresponding	No	2	Test (D) to determine if 1's are in each bit position where 1's are in (SA). If so, set ST2.
CZC	0 0 1 0 0 1	Compare zeros corresponding	No	2	Test (D) to determine if 0's are in each bit position where 1's are in (SA). If so, set ST2.
XOR	0 0 1 0 1 0	Exclusive OR	Yes	0-2	(D) ⊕ (SA) → (D)
MPY	0 0 1 1 1 0	Multiply	No		Multiply unsigned (D) by unsigned (SA) and place unsigned 32-bit product in D (most significant) and D+1 (least significant). If WR15 is D, the next word in memory after WR15 will be used for the least significant half of the product.
DIV	0 0 1 1 1 1	Divide	No	4	If unsigned (SA) is less than or equal to unsigned (D), perform no operation and set ST4. Otherwise, divide unsigned (D) and (D+1) by unsigned (SA). Quotient → (D), remainder → (D+1). If D = 15, the next word in memory after WR 15 will be used for the remainder.

3

3.5.3 Extended Operation (XOP) Instruction

General format:



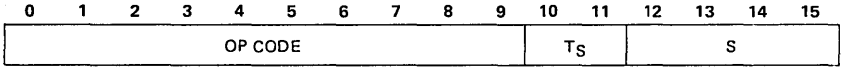
The T_S and S fields provide multiple mode addressing capability for the source operand. When the XOP is executed, ST6 is set and the following transfers occur:

$(40_{16} + 4D) \rightarrow$ (WP)
$(42_{16} + 4D) \rightarrow$ (PC)
SA → (new WR11)
(old WP) → (new WR13)
(old PC) → (new WR14)
(old ST) → (new WR15)

The 9900 does not test interrupt requests ($\overline{\text{INTREQ}}$) upon completion of the XOP instruction.

3.5.4 Single Operand Instructions

General format:



The T_S and S fields provide multiple mode addressing capability for the source operand.

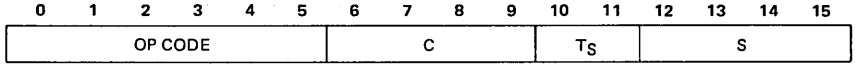
MNEMONIC	OP CODE 0 1 2 3 4 5 6 7 8 9	MEANING	RESULT COMPARED TO 0	STATUS BITS AFFECTED	DESCRIPTION
B	0 0 0 0 0 1 0 0 0 1	Branch	No	–	SA → (PC)
BL	0 0 0 0 0 1 1 0 1 0	Branch and link	No	–	(PC) → (WR11); SA → (PC)
BLWP	0 0 0 0 0 1 0 0 0 0	Branch and load workspace pointer	No	–	(SA) → (WP); (SA+2) → (PC); (old WP) → (new WR13); (old PC) → (new WR14); (old ST) → (new WR15); the interrupt input ($\overline{\text{INTREQ}}$) is not tested upon completion of the BLWP instruction.
CLR	0 0 0 0 0 1 0 0 1 1	Clear operand	No	–	0 → (SA)
SETO	0 0 0 0 0 1 1 1 0 0	Set to ones	No	–	$FFFF_{16}$ → (SA)
INV	0 0 0 0 0 1 0 1 0 1	Invert	Yes	0-2	$\overline{(SA)}$ → (SA)
NEG	0 0 0 0 0 1 0 1 0 0	Negate	Yes	0-4	–(SA) → (SA)
ABS	0 0 0 0 0 1 1 1 0 1	Absolute value*	No	0-4	|(SA)| → (SA)
SWPB	0 0 0 0 0 1 1 0 1 1	Swap bytes	No	–	(SA), bits 0 thru 7 → (SA), bits 8 thru 15; (SA), bits 8 thru 15 → (SA), bits 0 thru 7.
INC	0 0 0 0 0 1 0 1 1 0	Increment	Yes	0-4	(SA) + 1 → (SA)
INCT	0 0 0 0 0 1 0 1 1 1	Increment by two	Yes	0-4	(SA) + 2 → (SA)
DEC	0 0 0 0 0 1 1 0 0 0	Decrement	Yes	0-4	(SA) – 1 → (SA)
DECT	0 0 0 0 0 1 1 0 0 1	Decrement by two	Yes	0-4	(SA) – 2 → (SA)
X†	0 0 0 0 0 1 0 0 1 0	Execute	No	–	Execute the instruction at SA.

*Operand is compared to zero for status bit.

†If additional memory words for the execute instruction are required to define the operands of the instruction located at SA, these words will be accessed from PC and the PC will be updated accordingly. The instruction acquisition signal (IAQ) will not be true when the 9900 accesses the instruction at SA. Status bits are affected in the normal manner for the instruction executed.

3.5.5 CRU Multiple-Bit Instructions

General format:

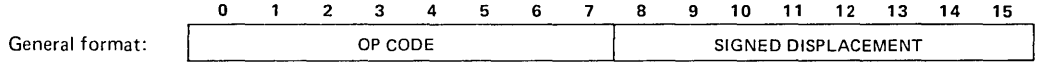


The C field specifies the number of bits to be transferred. If C = 0, 16 bits will be transferred. The CRU base register (WR12, bits 3 through 14) defines the starting CRU bit address. The bits are transferred serially and the CRU address is incremented with each bit transfer, although the contents of WR12 is not affected. T_S and S provide multiple mode addressing capability for the source operand. If 8 or fewer bits are transferred (C = 1 through 8), the source address is a byte address. If 9 or more bits are transferred (C = 0, 9 through 15), the source address is a word address. If the source is addressed in the workspace register indirect auto increment mode, the workspace register is incremented by 1 if C = 1 through 8, and is incremented by 2 otherwise.

MNEMONIC	OP CODE 0 1 2 3 4 5	MEANING	RESULT COMPARED TO 0	STATUS BITS AFFECTED	DESCRIPTION
LDCR	0 0 1 1 0 0	Load communcation register	Yes	0-2,5†	Beginning with LSB of (SA), transfer the specified number of bits from (SA) to the CRU.
STCR	0 0 1 1 0 1	Store communcation register	Yes	0-2,5†	Beginning with LSB of (SA), transfer the specified number of bits from the CRU to (SA). Load unfilled bit positions with 0.

†ST5 is affected only if $1 \leq C \leq 8$.

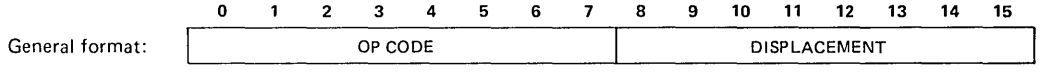
3.5.6 CRU Single-Bit Instructions



CRU relative addressing is used to address the selected CRU bit.

MNEMONIC	OP CODE 0 1 2 3 4 5 6 7	MEANING	STATUS BITS AFFECTED	DESCRIPTION
SBO	0 0 0 1 1 1 0 1	Set bit to one	–	Set the selected CRU output bit to 1.
SBZ	0 0 0 1 1 1 1 0	Set bit to zero	–	Set the selected CRU output bit to 0.
TB	0 0 0 1 1 1 1 1	Test bit	2	If the selected CRU input bit = 1, set ST2.

3.5.7 Jump Instructions

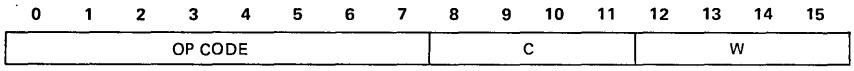


Jump instructions cause the PC to be loaded with the value selected by PC relative addressing if the bits of ST are at specified values. Otherwise, no operation occurs and the next instruction is executed since PC points to the next instruction. The displacement field is a word count to be added to PC. Thus, the jump instruction has a range of –128 to 127 words from memory-word address following the jump instruction. No ST bits are affected by jump instruction.

MNEMONIC	OP CODE 0 1 2 3 4 5 6 7	MEANING	ST CONDITION TO LOAD PC
JEQ	0 0 0 1 0 0 1 1	Jump equal	ST2 = 1
JGT	0 0 0 1 0 1 0 1	Jump greater than	ST1 = 1
JH	0 0 0 1 1 0 1 1	Jump high	ST0 = 1 and ST2 = 0
JHE	0 0 0 1 0 1 0 0	Jump high or equal	ST0 = 1 or ST2 = 1
JL	0 0 0 1 1 0 1 0	Jump low	ST0 = 0 and ST2 = 0
JLE	0 0 0 1 0 0 1 0	Jump low or equal	ST0 = 0 or ST2 = 1
JLT	0 0 0 1 0 0 0 1	Jump less than	ST1 = 0 and ST2 = 0
JMP	0 0 0 1 0 0 0 0	Jump unconditional	unconditional
JNC	0 0 0 1 0 1 1 1	Jump no carry	ST3 = 0
JNE	0 0 0 1 0 1 1 0	Jump not equal	ST2 = 0
JNO	0 0 0 1 1 0 0 1	Jump no overflow	ST4 = 0
JOC	0 0 0 1 1 0 0 0	Jump on carry	ST3 = 1
JOP	0 0 0 1 1 1 0 0	Jump odd parity	ST5 = 1

3.5.8 Shift Instructions

General format:

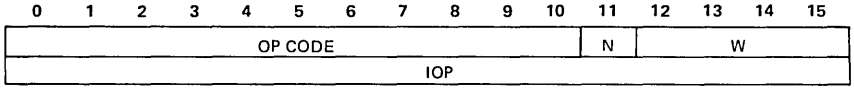


If C = 0, bits 12 through 15 of WR0 contain the shift count. If C = 0 and bits 12 through 15 of WR0 = 0, the shift count is 16.

MNEMONIC	OP CODE 0 1 2 3 4 5 6 7	MEANING	RESULT COMPARED TO 0	STATUS BITS AFFECTED	DESCRIPTION
SLA	0 0 0 0 1 0 1 0	Shift left arithmetic	Yes	0-4	Shift (WR) left. Fill vacated bit positions with 0.
SRA	0 0 0 0 1 0 0 0	Shift right arithmetic	Yes	0-3	Shift (WR) right. Fill vacated bit positions with original MSB of (WR).
SRC	0 0 0 0 1 0 1 1	Shift right circular	Yes	0-3	Shift (WR) right. Shift previous LSB into MSB.
SRL	0 0 0 0 1 0 0 1	Shift right logical	Yes	0-3	Shift (WR) right. Fill vacated bit positions with 0's.

3.5.9 Immediate Register Instructions

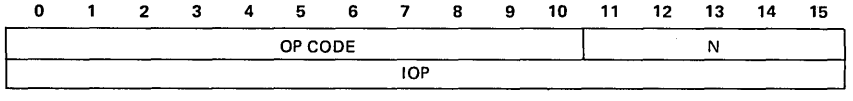
General format:



MNEMONIC	OP CODE 0 1 2 3 4 5 6 7 8 9 10	MEANING	RESULT COMPARED TO 0	STATUS BITS AFFECTED	DESCRIPTION
AI	0 0 0 0 0 0 1 0 0 0 1	Add immediate	Yes	0-4	(WR) + IOP → (WR)
ANDI	0 0 0 0 0 0 1 0 0 1 0	AND immediate	Yes	0-2	(WR) AND IOP → (WR)
CI	0 0 0 0 0 0 1 0 1 0 0	Compare immediate	Yes	0-2	Compare (W) to IOP and set appropriate status bits
LI	0 0 0 0 0 0 1 0 0 0 0	Load immediate	Yes	0-2	IOP → (WR)
ORI	0 0 0 0 0 0 1 0 0 1 1	OR immediate	Yes	0-2	(WR) OR IOP → (WR)

3.5.10 Internal Register Load Immediate Instructions

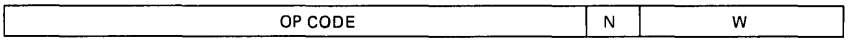
General format:



MNEMONIC	OP CODE 0 1 2 3 4 5 6 7 8 9 10	MEANING	DESCRIPTION
LWPI	0 0 0 0 0 0 1 0 1 1 1	Load workspace pointer immediate	IOP → (WP), no ST bits affected
LIMI	0 0 0 0 0 0 1 1 0 0 0	Load interrupt mask	IOP, bits 12 thru 15 → ST12 thru ST15

3.5.11 Internal Register Store Instructions

General format:

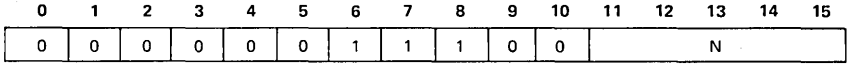


No ST bits are affected.

MNEMONIC	OP CODE 0 1 2 3 4 5 6 7 8 9 10	MEANING	DESCRIPTION
STST	0 0 0 0 0 0 1 0 1 1 0	Store status register	(ST) → (WR)
STWP	0 0 0 0 0 0 1 0 1 0 1	Store workspace pointer	(WP) → (WR)

3.5.12 Return Workspace Pointer (RTWP) Instruction

General format:

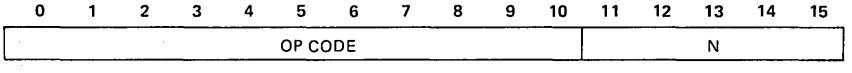


The RTWP instruction causes the following transfers to occur:

(WR15) → (ST)
(WR14) → (PC)
(WR13) → (WP)

3.5.13 External Instructions

General format:



External instructions cause the three most-significant address lines (A0 through A2) to be set to the below-described levels and the CRUCLK line to be pulsed, allowing external control functions to be initiated.

MNEMONIC	OP CODE 0 1 2 3 4 5 6 7 8 9 10	MEANING	STATUS BITS AFFECTED	DESCRIPTION	ADDRESS BUS A0	A1	A2
IDLE	0 0 0 0 0 0 1 1 0 1 0	Idle	–	Suspend SBP 9900A instruction execution until an interrupt, $\overline{\text{LOAD}}$, or $\overline{\text{RESET}}$ occurs	L	H	L
RSET	0 0 0 0 0 0 1 1 0 1 1	Reset	12–15	0 → ST12 thru ST15	L	H	H
CKOF	0 0 0 0 0 0 1 1 1 1 0	User defined		---	H	H	L
CKON	0 0 0 0 0 0 1 1 1 0 1	User defined		---	H	L	H
LREX	0 0 0 0 0 0 1 1 1 1 1	User defined		---	H	H	H

3.6 MICROINSTRUCTION CYCLE

The SBP 9900A includes circuitry which will indicate the completion of a microinstruction cycle. Designated as the $\overline{\text{CYCEND}}$ function, it provides CPU status that can simplify system design. The $\overline{\text{CYCEND}}$ output will go to a low logic level as a result of the low-to-high transistion of each clock pulse which initiates the last clock of a microinstruction.

3.7 SBP 9900A INSTRUCTION EXECUTION TIMES

Instruction execution times for the SBP 9900A are a function of:

1) Clock cycle time, t_c

2) Addressing mode used where operands have multiple addressing mode capability

3) Number of wait states required per memory access.

The following Table 6 lists the number of clock cycles and memory accesses required to execute each SBP 9900A instruction. For instructions with multiple addressing modes for either or both operands, the table lists the number of clock cycles and memory accesses with all operands addressed in the workspace-register mode. To determine the additional number of clock cycles and memory accesses required for modified addressing, add the appropriate values from the referenced tables. The total instruction-execution time for an instruction is:

$$T = t_c (C + W \cdot M)$$

where:

T = total instruction execution time;
t_c = clock cycle time;
C = number of clock cycles for instruction execution plus address modification;
W = number of required wait states per memory access for instruction execution plus address modification;
M = number of memory accesses.

As an example, the instruction MOVB is used in a system with $t_c = 0.5\ \mu s$ and no wait states are required to access memory. Both operands are addressed in the workspace register mode:

$$T = t_c (C + W \cdot M) = 0.5\ (14 + 0 \cdot 4)\ \mu s = 7\ \mu s.$$

If two wait states per memory access were required, the execution time is:

$$T = 0.5\ (14 + 2 \cdot 4)\ \mu s = 11\ \mu s.$$

If the source operand was addressed in the symbolic mode and two wait states were required:

$$T = t_c (C + W \cdot M)$$
$$C = 14 + 8 = 22$$
$$M = 4 + 1 = 5$$
$$T = 0.5\ (22 + 2 \cdot 5)\ \mu s = 16\ \mu s.$$

TABLE 6
INSTRUCTION EXECUTION TIMES

INSTRUCTION	CLOCK CYCLES C	MEMORY ACCESS M	ADDRESS MODIFICATION† SOURCE	ADDRESS MODIFICATION† DEST	INSTRUCTION	CLOCK CYCLES C	MEMORY ACCESS M	ADDRESS MODIFICATION† SOURCE	ADDRESS MODIFICATION† DEST
A	14	4	A	A	LWPI	10	2	–	–
AB	14	4	B	B	MOV	14	4	A	A
ABS (MSB = 0)	12	2	A	–	MOVB	14	4	B	B
(MSB = 1)	14	3	A	–	MPY	52	5	A	–
AI	14	4	–	–	NEG	12	3	A	–
ANDI	14	4	–	–	ORI	14	4	–	–
B	8	2	A	–	RSET	12	1	–	–
BL	12	3	A	–	RTWP	14	4	–	–
BLWP	26	6	A	–	S	14	4	A	A
C	14	3	A	A	SB	14	4	B	B
CB	14	3	B	B	SBO	12	2	–	–
CI	14	3	–	–	SBZ	12		–	–
CKOF	12	1	–	–	SETO	10	3	A	–
CKON	12	1	–	–	Shift (C ≠ 0)	12+2C	3	–	–
CLR	10	3	A	–	(C = 0, Bits 12–15				
COC	14	3	A	–	of WRO = 0)	52	4	–	–
CZC	14	3	A	–	(C = 0, Bits 12–15)				
DEC	10	3	A	–	of WRP = N ≠ 0)	20+2N	4	–	–
DECT	10	3	A	–	SOC	14	4	A	A
DIV (ST4 is set)	16	3	A	–	SOCB	14	4	B	B
DIV (ST4 is reset)*	92-124	6	A	–	STCR (C = 0)	60	4	A	–
IDLE	12	1	–	–	(1≤C≤7)	42	4	B	–
INC	10	3	A	–	(C = 8)	44	4	B	–
INCT	10	3	A	–	(9≤C≤15)	58	4	A	–
INV	10	3	A	–	STST	8	2	–	–
Jump (PC is changed)	10	1	–	–	STWP	8	2	–	–
(PC is not changed)	8	1	–	–	SWPB	10	3	A	–
LDCR (C = 0)	52	3	A	–	SZC	14	4	A	A
(1≤C≤8)	20+2C	3	B	–	SZCB	14	4	B	B
(9≤C≤15)	20+2C	3	A	–	TB	12	2	–	–
LI	12	3	–	–	X**	8	2	A	–
LIMI	14	2	–	–	XOP	36	8	A	–
LREX	12	1	–	–	XOR	14	4	A	–
$\overline{\text{RESET}}$ function	26	5	–	–	Undefined op codes:				
$\overline{\text{LOAD}}$ function	22	5	–	–	0000-01FF,0320-033F,0C00-0FFF,	6	1	–	–
Interrupt context switch	22	5	–	–	0780-07FF				

*Execution time is dependent upon the partial quotient after each clock cycle during execution.

**Execution time is added to the execution time of the instruction located at the source address minus 4 clock cycles and 1 memory access time.

†The letters A and B refer to the respective columns in the Address Modification Table.

ADDRESS MODIFICATION

ADDRESSING MODE	COLUMN A CLOCK CYCLES C	COLUMN A MEMORY ACCESSES M	COLUMN B CLOCK CYCLES C	COLUMN B MEMORY ACCESSES M
WR (T_S or T_D = 00)	0	0	0	0
WR indirect (T_S or T_D = 01)	4	1	4	1
WR indirect auto-increment (T_S or T_D = 11)	8	2	6	2
Symbolic (T_S or T_D = 10, S or D = 0)	8	1	8	1
Indexed (T_S or T_D = 10, S or D ≠ 0)	8	2	8	2

4. INTERFACING

The input/output (I/O) accommodations have been designed for TTL compatibility. Direct interfacing, supportable by the entire families of catalog devices, is shown in Figure 13.

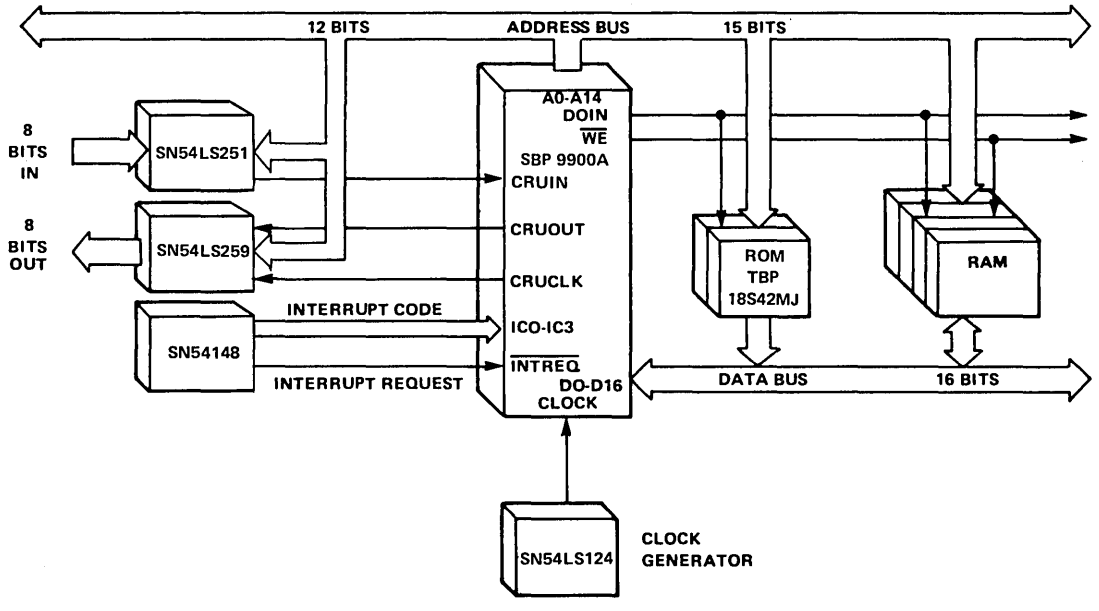


FIGURE 13 – MINIMUM SBP 9900A SYSTEM

4.1 INPUT CIRCUIT

The input circuit used on the SBP 9900A is basically an RTL configuration which has been modified for TTL compatibility as shown in Figure 14. An input-clamping diode is incorporated to limit negative excursions (ringing) when the SBP 9900A is on the receiving end of a transmission line; and input switching threshold of nominally +1.5 volts has been specified for improved noise immunity. This threshold is achieved via two resistors which function as a voltage divider to increase the one V_{BE} threshold of the I^2L input transistor to +1.5 volts.

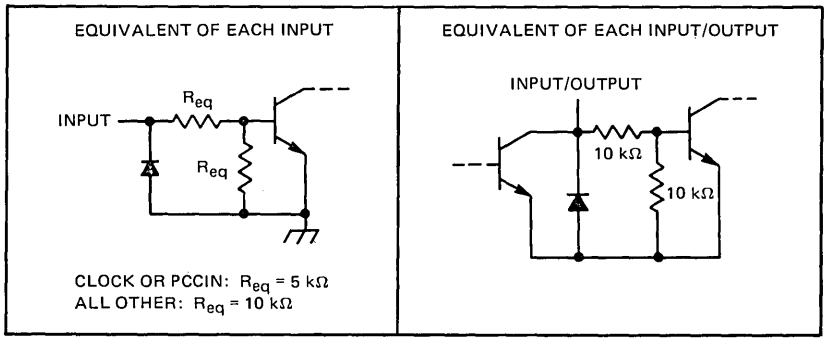


FIGURE 14 – SCHEMATICS OF INPUTS AND INPUT/OUTPUTS

The input circuit characteristics for input current versus input voltage are shown in Figure 15. The 10-kΩ and 20-kΩ load lines and threshold knee at +1.5 volts provide a high-impedance characteristic to reduce input loading and improve the low-logic-level input noise immunity over some standard TTL inputs. Full compatibility is maintained with virtually all 5-volt-logic families even when the SBP 9900A is powered down (injector current reduced).

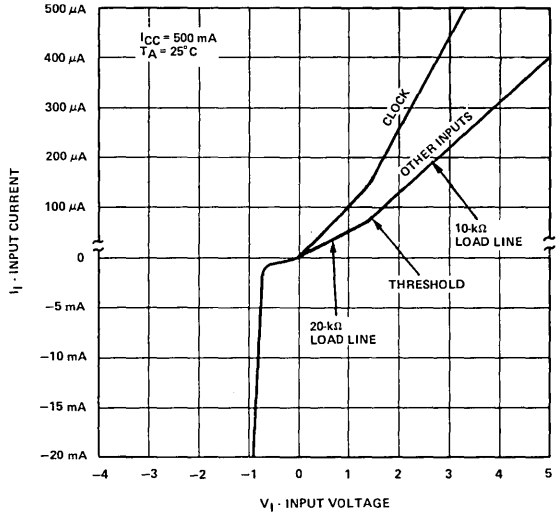


FIGURE 15 – TYPICAL INPUT CHARACTERISTICS

4.1.1 Sourcing Inputs

The inputs may be driven directly by most 5-volt-logic families. Functions that feature internal pull-up resistors at their outputs usually require no external interface components. Functions that feature open-collector outputs generally require external pull-up resistors.

4.1.2 Terminating Unused Inputs

Inputs that are selected to be hardwired to a logic-level low may be connected directly to ground. Inputs that are selected to be hardwired to a logic-level high must be tied, via a current limiting (pull-up) resistor, to a logic-level-high low-impedance voltage source such as V_{CC}. A single resistor common to all (N) inputs may be used for transient protection.

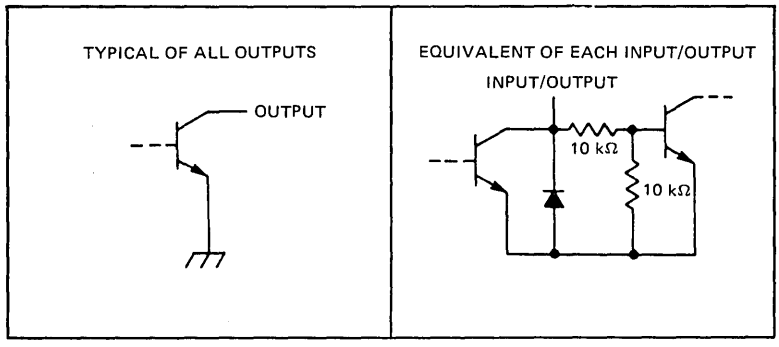


FIGURE 16 – SCHEMATICS OF OUTPUTS AND INPUT/OUTPUTS

4.2 OUTPUT CIRCUIT

The output circuit selected for the SBP 9900A is a current-injected, open-collector transistor shown in Figure 16. Since this transistor is current-injected, output sourcing capability is directly related to injector current. In other words, the number of loads that may be driven by an SBP 9900A output is directly reduced as injector current is reduced.

The output circuit characteristic for low-level output voltage (V_{OL}) versus low-level output current (I_{OL}) is shown in Figure 17. At rated injector current, the SBP 9900A output circuit offers a low-level output voltage of typically 220 mV.

The output circuit characteristics for 1) high-level output voltage (V_{OH}) and current (I_{OH}), 2) rise times, and 3) next stage input noise immunity, are a function of the load circuit being driven. The load circuit may be either:

A) the direct input of a five-volt-logic family if no source current is required

or, for greater noise immunity and improved rise times,

B) the direct input of a five-volt-logic family in conjunction with a discrete pull-up resistor.

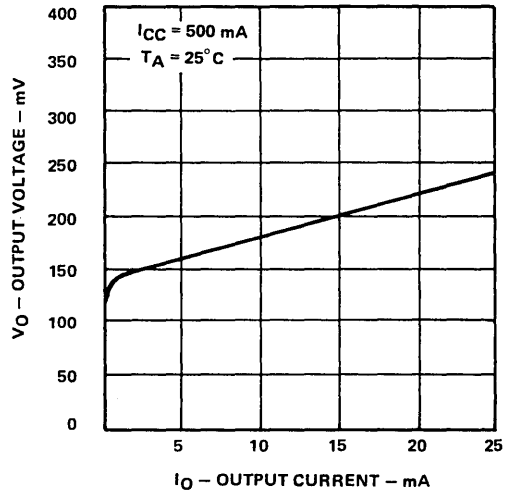


FIGURE 17 – TYPICAL OUTPUT CHARACTERISTICS

4.2.1 OUTPUT LOAD RESISTOR

When a discrete pull-up resistor R_L is utilized, the fanout requirements will restrict both its maximum and minimum values. The maximum load resistor value $R_{L(max)}$ will maintain the high-level output voltage minimum (2.4 V) while conducting $I_{OH} + N \cdot I_{IH(load)}$. $R_{L(max)}$ may be calculated as shown in Figure 18.

The minimum load resistor $R_{L(min)}$ should insure that the arithmetic sum of the current through R_L and the sink currents of the loads is less than I_{OL}. $R_{L(min)}$ may be calculated as shown in Figure 18.

Table 7 shows, for convenience, $R_{L(Min)}$ and $R_{L(Max)}$ values for several fanout values.

HIGH-LEVEL (OFF-STATE) CIRCUIT CALCULATIONS

The allowable voltage drop across the load resistor (V_{RL}) is the difference between the pull-up source and the V_{OH} level required at the load:

$$V_{RL} = V_{source} - V_{OH\ min}$$

The total current through the load resistor (I_{RL}) is the sum of the load current and the high-level output current (I_{OH}):

I_{RL} = Load Current (into the load inputs) + I_{OH}
where: I_{OH} = 400 μA max

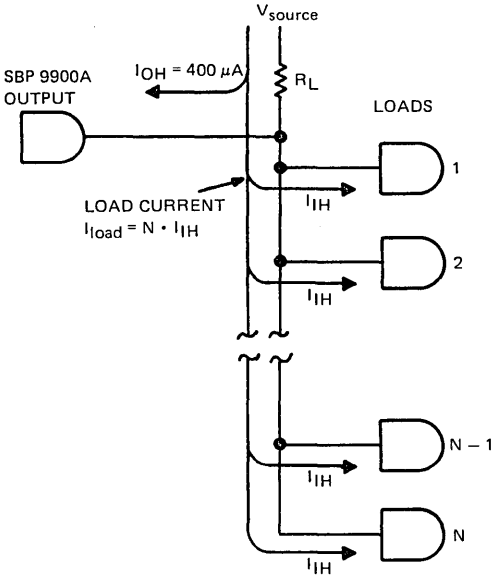
Therefore, calculations for the maximum value of R_L would be:

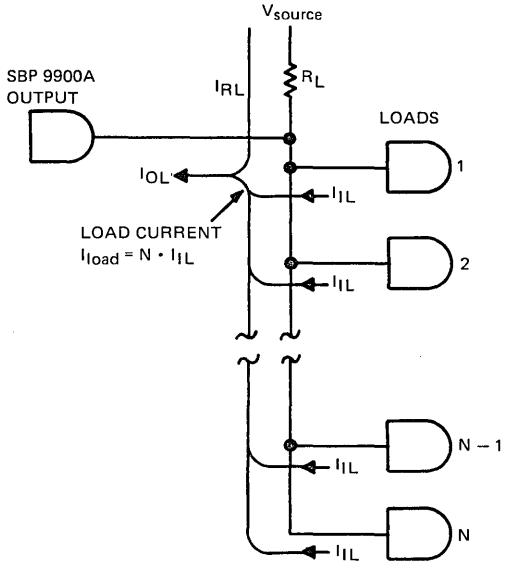
$$R_{L(max)} \text{ in ohms} = \frac{V_{source} - V_{OH\ min}}{\text{Load Current} + 400\ \mu A}$$

LOW-LEVEL (ON-STATE) CIRCUIT CALCULATIONS

The maximum current through the load resistor when the output is on, plus the amount of current from the low-level input load, must be limited to the I_{OL} capability of the output. Therefore, the equation is:

$$R_{L(min)} = \frac{V_{source} - V_{OL\ max}}{I_{OL} - I_{load}}$$





Assume: V_{source} = 5 V, $V_{OH(min)}$ = 2.4 V, N = 5, I_{IH} = 50 μA

$$R_{L(max)} = \frac{V_{source} - V_{OH}}{I_{load} + I_{OH}}$$

$$R_{L(max)} = \frac{5\ V - 2.4\ V}{250\ \mu A + 400\ \mu A} = \frac{2.6}{0.00065}\ \Omega = 4000\ \Omega$$

A. R_L MAXIMUM CALCULATIONS

Assume: V_{source} = 5 V, V_{OL} = 0.4 V, I_{IL} = 2 mA, N = 5, I_{OL} capability = 20 mA

$$R_{L(min)} = \frac{V_{source} - V_{OL}}{I_{OL} - I_{load}}$$

$$R_{L(min)} = \frac{5\ V - 0.4\ V}{20\ mA - 10\ mA} = \frac{4.6}{0.01}\ \Omega = 460\ \Omega$$

B. R_L MINIMUM CALCULATIONS

FIGURE 18 – OUTPUT LOAD RESISTOR CALCULATIONS

TABLE 7
OUTPUT LOAD RESISTOR VALUES (R_L)

TYPE OF LOGIC	DRIVING 1 LOAD		DRIVING 5 LOADS		DRIVING 10 LOADS	
	$R_{L(min)}$	$R_{L(max)}$	$R_{L(min)}$	$R_{L(max)}$	$R_{L(min)}$	$R_{L(max)}$
54LS/74LS	234 Ω	6190 Ω	252 Ω	5200 Ω	280 Ω	4333 Ω
54/74	250 Ω	5909 Ω	383 Ω	4333 Ω	1150 Ω	3250 Ω
54S/74S	256 Ω	5777 Ω	460 Ω	4160 Ω	2300 Ω	2888 Ω
MOS	230 Ω	6341 Ω	230 Ω	5777 Ω	231 Ω	5200 Ω
C-MOS	230 Ω	6500 Ω	230 Ω	6500 Ω	231 Ω	6498 Ω

CONDITIONS:	And unit loads of:	I_{IL}	I_{IH}
V_{source} = 5 V,	54LS/74LS	0.36 mA	10 μA
V_{OH} = 2.4 V (Satisfies most 5-V logic),	54/74	1.6 mA	40 μA
V_{OL} = 0.4 V,	54S/74S	2 mA	50 μA
I_{OH} = 400 μA (Maximum leakage),	N-MOS	10 μA	10 μA
I_{OL} = 20 mA	C-MOS	10 pA	10 pA

5. POWER SOURCE

I^2L is a current-injected logic. When the injector and ground pins are placed across a curve tracer, the processor V-I characteristic will resemble that of a silicon switching diode. Any voltage or current source capable of supplying the desired current at the injector node voltage required will suffice. A dry-cell battery, a 5-volt TTL power supply, a programmable current supply (See Figure 19) — literally whatever power source is convenient can be used for most cases. For example, if a 5-volt TTL power supply is to be used, a series dropping resistor should be connected between the 5-volt supply and the injector pins of the I^2L device, as illustrated in Figure 20, to select the desired operating current.

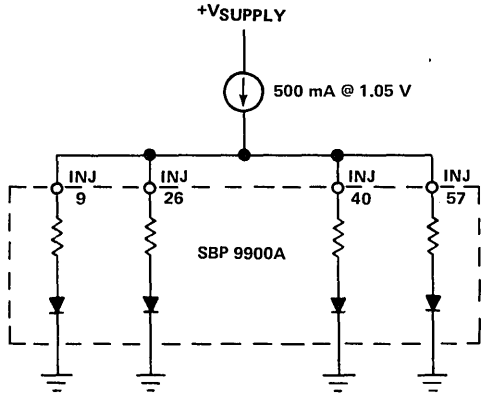
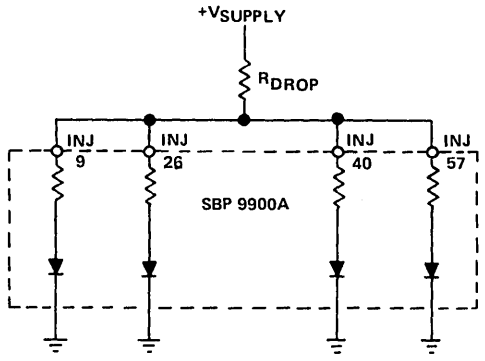


FIGURE 19 — INJECTOR CURRENT SOURCE



GENERAL FORMULA (OHM'S LAW)

$$R_{DROP} = \frac{V_{SUPPLY} - V_{CC}}{I_{CC}}$$

EXAMPLE FOR V_{SUPPLY} = 5V, AND I_{CC} = 500 mA:

$$R_{DROP} = \frac{5 - 1.05}{0.5} = \frac{3.95}{0,5} = 7.9 \text{ OHMS}$$

FIGURE 20 – INJECTOR CURRENT CALCULATIONS

Figures 21 and 22 show the typical injector node voltages that occur across the temperature and injector current ranges.

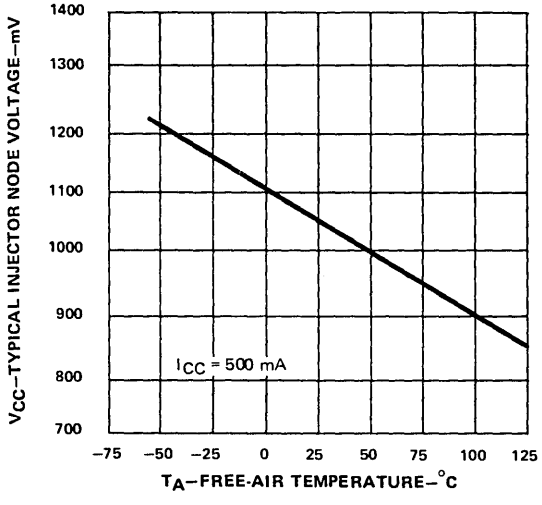


FIGURE 21 – INJECTOR-NODE VOLTAGE vs FREE-AIR TEMPERATURE

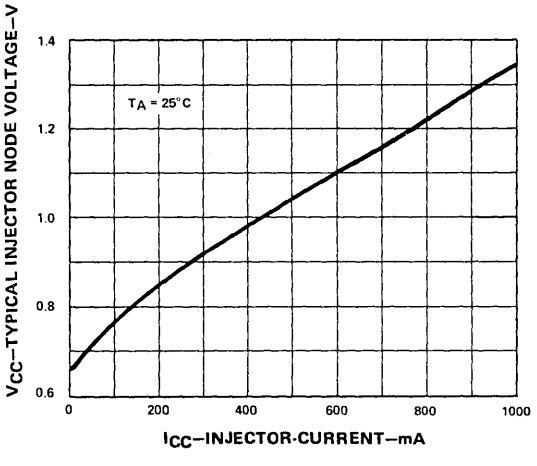


FIGURE 22 – INJECTOR-NODE VOLTAGE vs INJECTOR CURRENT

6. ELECTRICAL AND MECHANICAL SPECIFICATIONS

6.1 SBP 9900A AND SBP 9900A-1* RECOMMENDED OPERATING CONDITIONS AT I_{CC} = MAX † (UNLESS OTHERWISE NOTED)

PARAMETER		MIN	NOM	MAX	UNIT
Supply current, I_{CC}	SBP 9900A MJ/NJ/EJ	450	500	550	mA
	SBP 9900ACJ				
High-level output voltage, V_{OH}				5.5	V
Low-level output current, I_{OL}				20	mA
Clock frequency, f_{clock}		0		3	MHz
Width of clock pulse, t_w	High (67%)	222			ns
	Low (33%)	111			
Clock rise time, t_r				20	ns
Clock fall time, t_f				20	ns
Setup time, t_{su} (see Figure 23)	HOLD	110†			ns
	READY	70†			
	D0 thru D15	65†			
	CRUIN	50†			
	INTREQ	25†			
	IC0 thru IC3	25†			
Hold time, t_h (see Figure 23)	HOLD	25†			ns
	READY	50†			
	D0 thru D15	40†			
	CRUIN	40†			
	INTREQ	55†			
	IC0 thru IC3	55†			
Operating free-air temperature, T_A	SBP 9900AMJ, SBP 9900ANJ	−55		125	°C
	SBP 9900AEJ	−40		85	
	SBP 9900ACJ	0		70	

* References to SBP 9900A apply equally to the SBP 9900A-1 throughout this document except in 6.3 Switching Characteristics. SBP 9900A-1 complies with JAN specification MIL-M-38510/46001 and MIL-STD-883 processing.

† For conditions shown as MIN, NOM, MAX, use the appropriate value specified under recommended operating conditions.

DESIGN GOAL

This page provides tentative information on a product in the developmental stage. Texas Instruments reserves the right to change or discontinue this product without notice.

6.2 SBP 9900A AND SBP 9900A-1* CHARACTERISTICS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage		I_{CC} = MIN,	I_I = –12 mA			–1.5	V
I_{OH}	High-level output current	I/O Pins	I_{CC} = NOM,	V_{IH} = 2 V,			350	μA
		Other outputs	V_{IL} = 0.8 V,	V_{OH} = 2.4 V			50	μA
		I/O Pins	I_{CC} = NOM,	V_{IH} = 2 V			1	mA
		Other outputs	V_{IL} = 0.8 V,	V_{OH} = 5.5 V			250	μA
V_{OL}	Low-level output voltage		I_{CC} = NOM, V_{IL} = 0.8 V,	V_{IH} = 2 V I_{OL} = 20 mA			0.4	V
I_I	Input current	Clock	I_{CC} = NOM,	V_I = 2.4 V		0.6	1	mA
		All other inputs				200	300	μA

6.3 SBP 9900A AND SBP 9900A-1* SWITCHING CHARACTERISTICS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED), I_{CC} = MAX, SEE FIGURES 23 AND 24

PARAMETER	FROM	TO	TEST CONDITIONS†	SBP 9900A			SBP 9900A-1*			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH} or t_{PHL}	CLOCK	ADDRESS BUS (A0 – A14)	C_L = 150 pF		90	130		90	140	ns
t_{PLH} or t_{PHL}	CLOCK	DATA BUS (D0 – D15)			105	145		105	155	ns
t_{PLH} or t_{PHL}	CLOCK	WRITE ENABLE (WE)			100	155		100	185	ns
t_{PLH} or t_{PHL}	CLOCK	CYCLE END (CYCEND)			90	135		90	145	ns
t_{PLH} or t_{PHL}	CLOCK	DATA BUS IN (DBIN)			115	160		115	160	ns
t_{PLH} or t_{PHL}	CLOCK	MEMORY ENABLE (MEMEN)			90	130		90	140	ns
t_{PLH} or t_{PHL}	CLOCK	CRU CLOCK (CRUCK)			95	145		95	155	ns
t_{PLH} or t_{PHL}	CLOCK	CRU DATA OUT (CRUOUT)			110	175		110	185	ns
t_{PLH} or t_{PHL}	CLOCK	HOLD ACKNOWLEDGE (HLDA)			190	290		190	290	ns
t_{PLH} or t_{PHL}	CLOCK	WAIT			90	130		90	130	ns
t_{PLH} or t_{PHL}	CLOCK	INSTRUCTION ACQUISITION (IAQ)			90	130		90	130	ns

† For conditions shown MIN, NOM, or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at I_{CC} = NOM, T_A = 25°C.

* References to SBP 9900A apply equally to the SBP 9900A-1 throughout this document except in 6.3 Switching Characteristics. SBP 9900A-1 complies with JAN specification MIL-M-38510/46001 and MIL-STD-883 processing.

DESIGN GOAL

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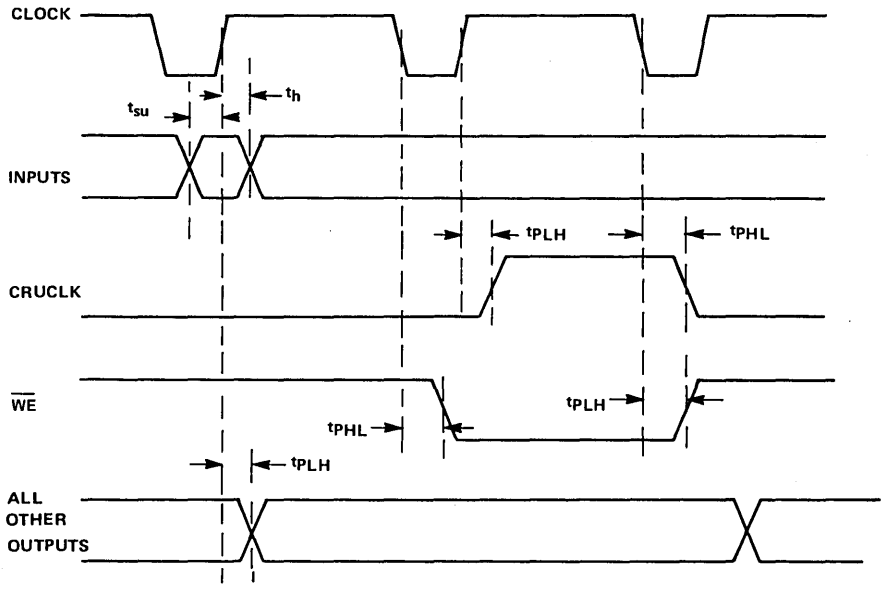


FIGURE 23 – SWITCHING-TIME VOLTAGE WAVEFORMS

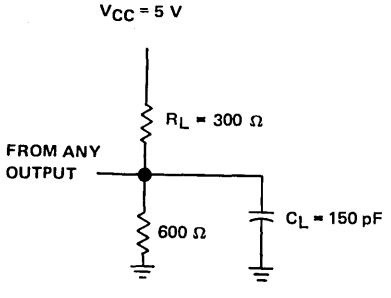


FIGURE 24 – SWITCHING-TIME LOAD-CIRCUITS

6.4 CLOCK FREQUENCY VS. TEMPERATURE

Stability of the operational frequency over the full temperature range of −55°C to 125°C is illustrated in Figure 25. The effects of temperature on clock frequency are nil above 0°C. Below 0°C the effects are typically less than −5% with respect to the typical performance.

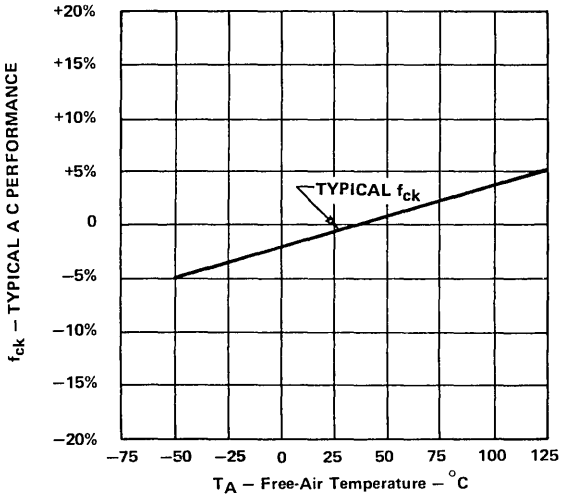
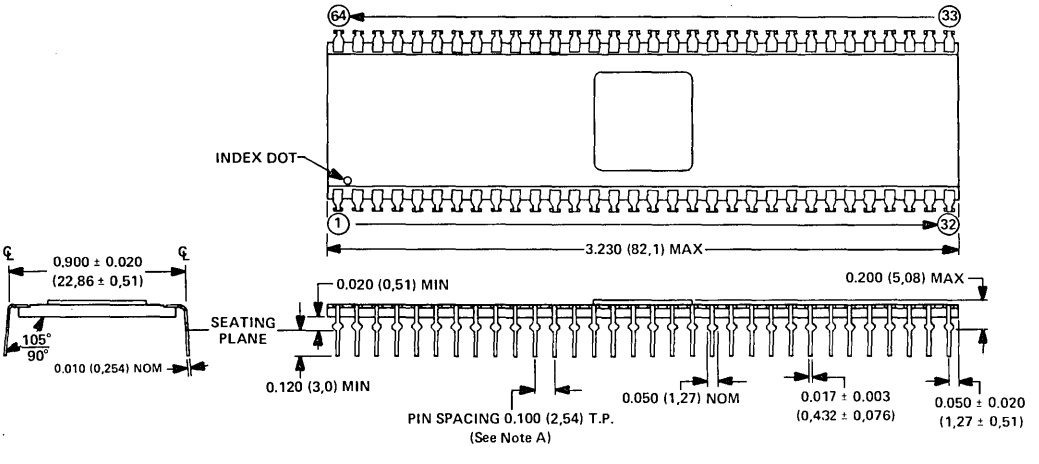


FIGURE 25 – AC PERFORMANCE FREE-AIR TEMPERATURE

7. MECHANICAL DATA



NOTES: A. Each pin centerline is located within 0.010 (2,54) of its true longitudinal position.
B. All linear dimensions are in inches and parenthetically in millimeters. Inch dimensions govern.

SBP 9960 Programmable CRU I/O Expander

SBP 9960
PROGRAMMABLE CRU I/O EXPANDER

1.0 INTRODUCTION

1.1 GENERAL DESCRIPTION

The SBP 9960 Programmable CRU I/O Expander is a ruggedized monolithic software-configurable input/output device fabricated with oxide separated Integrated Injection Logic (I^2L) technology. The SBP 9960 provides a flexible and efficient Communications Register Unit (CRU) based interface between the SBP/TMS 9900 series Family of microprocessors and auxiliary systems functions ranging from bit-oriented sensors and actuators to byte/word/n-bit-field oriented peripherals.

Under software control, each of the SBP 9960's sixteen single-bit I/O ports may be individually configured to either the input or output mode. I^2L technology enables the SBP 9960's static logic, and TTL compatible I/O, to operate over a very wide ambient temperature range from a single d-c power source with output current sink capability up to 40 mA. When the SBP 9960 is used in conjunction with the SBP 9961 I^2L Interrupt-Controller/Timer, the SBP 9960/SBP 9961 pair form an I^2L systems alternate to the N-channel MOS TMS 9901 Programmable Systems Interface device while maintaining strict compatibility with existing software handlers developed in support of the TMS 9901.

1.2 KEY FEATURES

- SBP/TMS 9900 Series Microprocessor Family Peripheral
- 16 Individual, Single Bit, Software Configurable I/O Ports
- 20/40 mA current Sinking Outputs
- Software Compatibility with TMS 9901 when used in Conjunction with SBP 9961
- TTL Compatible I/O
- Wide Ambient Temperature Operation
  - —SBP 9960CJ: 0°C to +70°C
  - —SBP 9960EJ: −40°C to +85°C
  - —SBP 9960MJ: −55°C to +125°C
  - —SBP 9960NJ: −55°C to +125°C (with high-reliability processing)
- I^2L Technology
  - —Constant Current Power Source
  - —Fully Static Operation
  - —Single Phase Edge-Triggering Clock
  - —Wide Temperature Stability

DESIGN GOAL
This document provides tentative information on a product in the developmental stage. Texas Instruments reserves the right to change or discontinue this product without notice.

2.0 FUNCTIONAL DESCRIPTION

2.1 SBP 9960/CPU INTERFACE

The SBP 9960 communicates with the CPU through the commumications Register Unit (CRU) interface as shown in Figures 1 and 3. The SBP 9960's CRU interface consists of: a) five CRU address select lines (S0-S4), B) a single chip enable ($\overline{CE}$), c) a 9960 to CPU serial data-bit line (CRUIN), d) a CPU to 9960 serial data-bit line (CRUOUT), and e) a CPU to 9960 serial data-bit clock (CRUCLK). When $\overline{CE}$ is activated (logic-level low), S0-S4 select a specific single-bit I/O port as indicated in Table 1. In the case of an SBP 9960 write operation, the datum is transferred from the CPU to the SBP 9960 via the CRUOUT line. The CRUOUT datum is strobed into the selected single-bit port by CRUCLK. In the case of a SBP 9960 read operation, the selected single-bit port is sampled by the CPU via the CRUIN line.

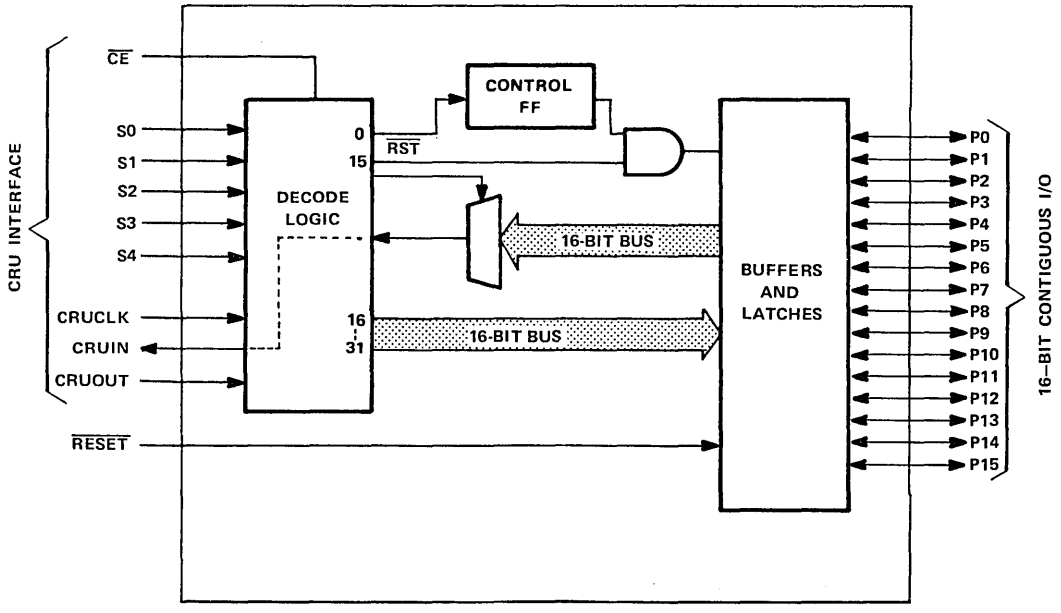


FIGURE 1. SBP9960 FUNCTIONAL BLOCK DIAGRAM

2.2 CRU BIT ASSIGNMENTS

Table 1 describes the SBP 9960's CRU bit assignments. Note that CRU bits 1-14 have been reserved for the SBP 9961 thereby insuring software compatibility between the SBP 9960/SBP9961 pair and the TMS 9901.

2.3 INPUT/OUTPUT

One of sixteen SBP 9960, single-bit, combination open-collector-output/resistor-divider-input I/O ports is conversationally represented in figure 2. As a direct result of the open-collector output structure, the data flow direction through the port is determined by the stored logic-level of the associated output-register bit in combination with the data flow direction of the external device serviced by the port. When

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the output-register bit (Q) is at logic-level high, the corresponding package pin (P) is essentially floating and therefore free to be externally pulled to either the high or low logic-level. In other words, when Q is at logic-level high, the ports data flow direction can be either inward, where an external device pulls P to the high or low logic-level; or the data flow direction can be outward, where an external resistor (R) both pulls P to logic-level high and sources current drive into the inputs of external devices. When Q is at logic-level low, the ports unconditional data flow direction is outward, where P has the capacity to sink 20/40*mA of current from external devices. Q can be reset to logic-level low through CPU execution of a SET BIT TO ZERO (SBZ) instruction; Q can be set to logic-level high through: 1) a hardware initiated reset ($\overline{\text{RESET}}$), 2) a software initiated reset ($\overline{\text{RST}}$: CRU BIT 15) preceded by setting the control bit (CRU BIT 0) to logic-level high, or 3) CPU execution of a SET BIT TO ONE (SBO) instruction. Note that both $\overline{\text{RESET}}$ and $\overline{\text{RST}}$ affect all sixteen single-bit I/O ports while CPU execution of either an SBO or SBZ instruction can be targeted at an individual single-bit port independent of uninvolved ports. Once the data flow direction has been established for each single-bit port, CPU communication with the external devices driven or sensed by each individual port is effected through execution of the CRU instructions: LDCR, STCR, SBO, SBZ, and TB.

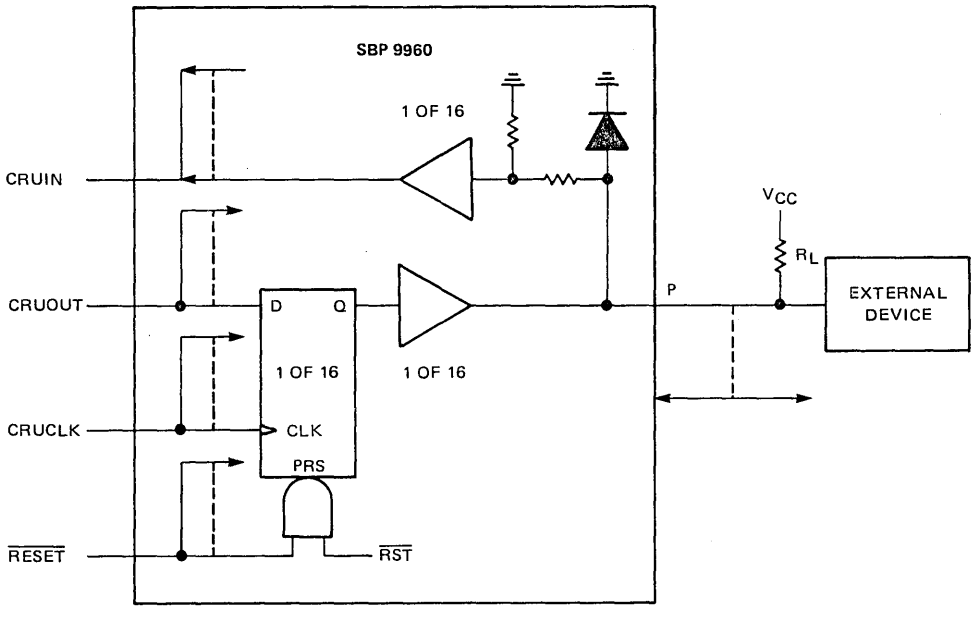

FIGURE 2. 1 OF 16 SINGLE-BIT I/O PORTS

*Outputs P0, P1, P2, and P3 have extended current sink capability to 40 mA.

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TABLE 1 – SBP 9960 CRU BIT ASSIGNMENTS

CRU BIT	S0	S1	S2	S3	S4	CRU READ DATA	CRU WRITE DATA
0	0	0	0	0	0	Control Bit	Control Bit
1-14						Note 1	Note 1
15	0	1	1	1	1	"1"	No Operation/ $\overline{RST}$ (2)
16	1	0	0	0	0	P0 Input(3)	P0 Output(4) (5)
17	1	0	0	0	1	P1	P1 (5)
18	1	0	0	1	0	P2	P2 (5)
19	1	0	0	1	1	P3	P3 (5)
20	1	0	1	0	0	P4	P4
21	1	0	1	0	1	P5	P5
22	1	0	1	1	0	P6	P6
23	1	0	1	1	1	P7	P7
24	1	1	0	0	0	P8	P8
25	1	1	0	0	1	P9	P9
26	1	1	0	1	0	P10	P10
27	1	1	0	1	1	P11	P11
28	1	1	1	0	0	P12	P12
29	1	1	1	0	1	P13	P13
30	1	1	1	1	0	P14	P14
31	1	1	1	1	1	P15 Input(3)	P15 Output(4)

NOTES: (1) Bits 1-14 reserved for SBP 9961 Interval Timer/Interrupt Controller
(2) Writing a zero to bit 15 while CONTROL = 1 executes a software reset of the I/O ports.
(3) Data present on the port will be read without affecting the data.
(4) Writing data to the port will both program the port to the output mode and output the data.
(5) These outputs are provided with extended sink-current capability to 40 mA.

2.4 SYSTEM OPERATION

During a typical power-up sequence of a SBP 9960-based system, $\overline{RESET}$ should be activated (logic-level low) to force the SBP 9960 to the state where each of the sixteen individual single-bit I/O ports is in the input mode. System software should then configure each single-bit port as required. If a given port must be reconfigured from the input to output mode after power-up, the associated output-register bit must be set to logic-level high through CPU execution of an SBO instruction.

2.5 SBP 9960/SBP 9961 EMULATION OF THE TMS 9901

Figure 3 shows the system configuration of a SBP 9960 functioning in conjunction with a SBP 9961 in emulation of a TMS 9901. Note the common connection of: a) the individual chip enables, and b) the CRU interface lines. For a complete description of the SBP 9961 and the TMS 9901 refer respectively to the *SBP 9961 Interrupt-Controller/Timer Data Manual* and the *TMS 9901 Programmable Systems Interface Data Manual.*

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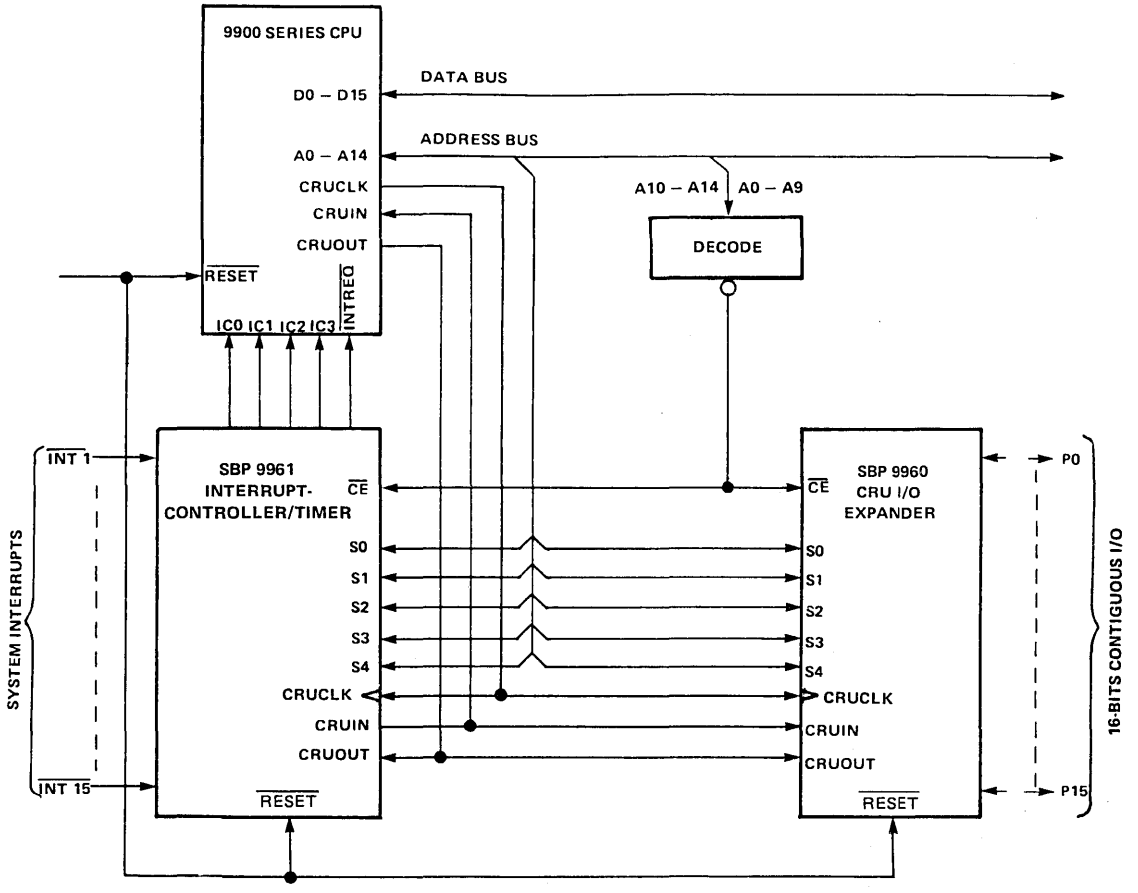

FIGURE 3 – SYSTEM CONFIGURATION USING SBP 9960 AND SBP 9961

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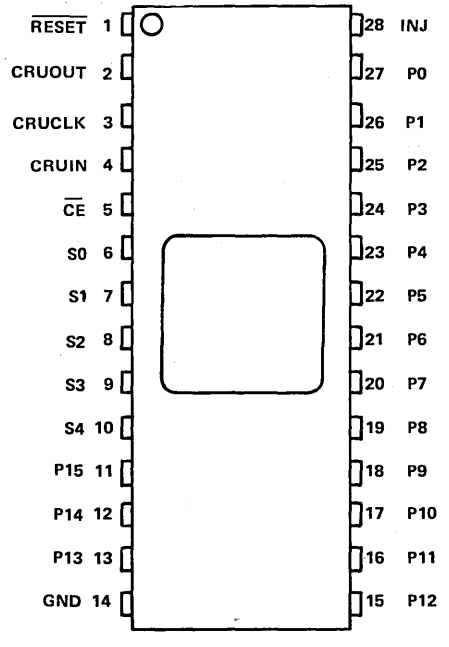
2.6 SBP 9960 PIN ASSIGNMENTS AND FUNCTIONS

SIGNATURE	PIN	I/O	DESCRIPTION
S0	6	IN	ADDRESS SELECT LINES. The data bit being accessed by the CRU
S1	7	IN	interface is specified by the 5-bit code appearing on S0-S4.
S2	8	IN	
S3	9	IN	
S4	10	IN	
CRUIN	4	OUT	CRU DATA IN (to CPU). Data specified by S0-S4 is transmitted to the CPU by CRUIN. When $\overline{CE}$ is not active, CRUIN is pulled to logic-leve high.
CRUOUT	2	IN	CRU DATA OUT (from CPU). When $\overline{CE}$ is active data present on the CRUOUT input will be strobed by CRUCLK and written into the CRU bit specified by S0-S4.
CRUCLK	3	IN	CRU CLOCK (from CPU). CRUCLK specifies that valid data is present on the CRUOUT line.
$\overline{RESET}$	1	IN	POWER-UP RESET. When active (low), $\overline{RESET}$ forces all I/O's (P0-P15) to input mode.
$\overline{CE}$	5	IN	CHIP ENABLE. When active (low), data may be bidirectionally transferred between the SBP 9960 and the CPU.
INJ	28		Supply Current
GND	14		Ground Reference
P0	27	I/O	I/O pins
P1	26	I/O	
P2	25	I/O	
P3	24	I/O	
P4	23	I/O	
P5	22	I/O	
P6	21	I/O	
P7	20	I/O	
P8	19	I/O	
P9	18	I/O	
P10	17	I/O	
P11	16	I/O	
P12	15	I/O	
P13	13	I/O	
P14	12	I/O	
P15	11	I/O	



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3.0 ELECTRICAL SPECIFICATIONS

3.1 RECOMMENDED OPERATING CONDITIONS UNLESS OTHERWISE NOTED, I_{CC} = 70 mA

PARAMETER		MIN	NOM	MAX	UNIT
Supply current, I_{CC}		63	70	77	mA
High-level output voltage, V_{OH}				5.5	V
Low-level output current, I_{OL}				20†	mA
Operating free-air temperature, T_A	SBP 9960MJ, SBP 9960NJ	−55		125	°C
	SBP 9960EJ	−40		85	
	SBP 9960CJ	0		70	

†40 mA on extended drive outputs P0, P1, P2, and P3

3.2 ELECTRICAL CHARACTERISTICS (OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE, UNLESS OTHERWISE NOTED)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	I_{CC} = MIN,	I_I = −12 mA			−1.5	V
I_{OH}	High-level output current	I_{CC} = 70 mA, V_{IL} = 0.8 V,	V_{IH} = 2 V, V_{OH} = 5.5 V			400	μA
V_{OL}	Low-level output voltage	I_{CC} = 70 mA, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 20 mA (40 mA§)			0.5	V
I_I	Input current	I_{CC} = 70 mA,	V_I = 2.4 V		225		μA

†For conditions shown as MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at I_{CC} = 70 mA, T_A = 25°C.
§Extended drive outputs only.

3.3 TIMING REQUIREMENTS OVER FULL RANGE OF OPERATING CONDITIONS

PARAMETER		MIN	NOM	MAX	UNIT
t_{su}	Setup time for S0-S4, $\overline{CE}$, or CRUOUT before CRUCLK		200		ns
t_{su}	Setup time, input before valid CRUIN		200		ns
$t_{w(CRUCLK)}$	CRU clock pulse width		100		ns
t_h	Hold time for Address or Data		0		ns

3.4 SWITCHING CHARACTERISTICS OVER FULL RANGE OF RECOMMENDED OPERATING CONDITIONS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PD}	Propagation delay, S0-S4 or $\overline{CE}$ to valid CRUIN	C_L = 100 pF, R_L = 300 Ω		300		ns

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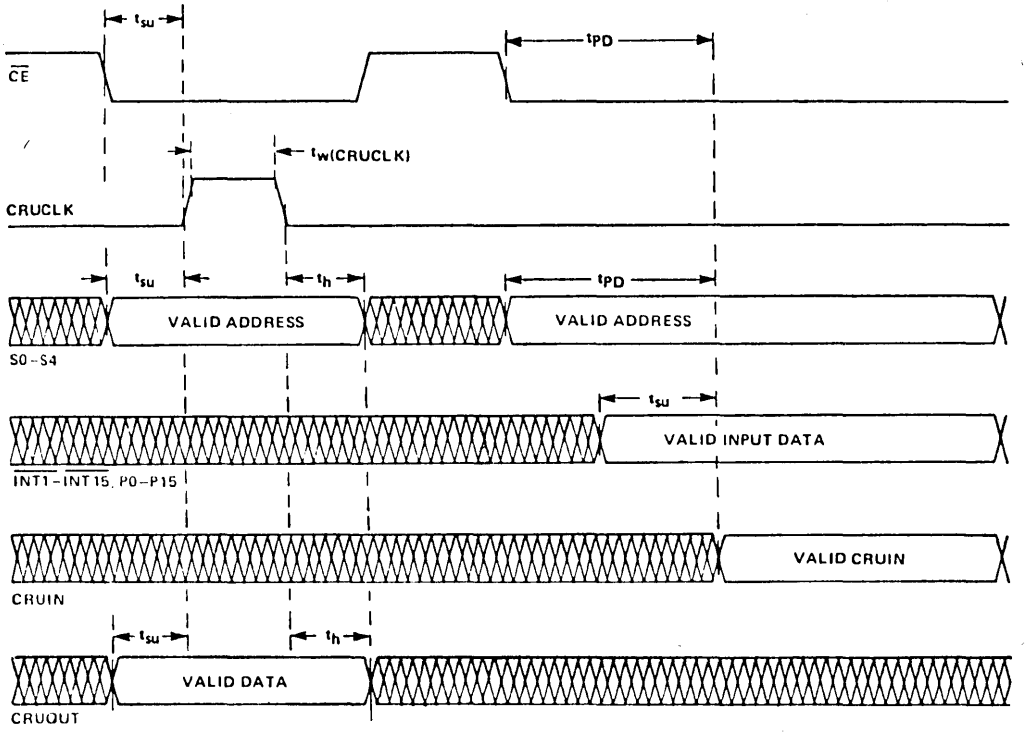
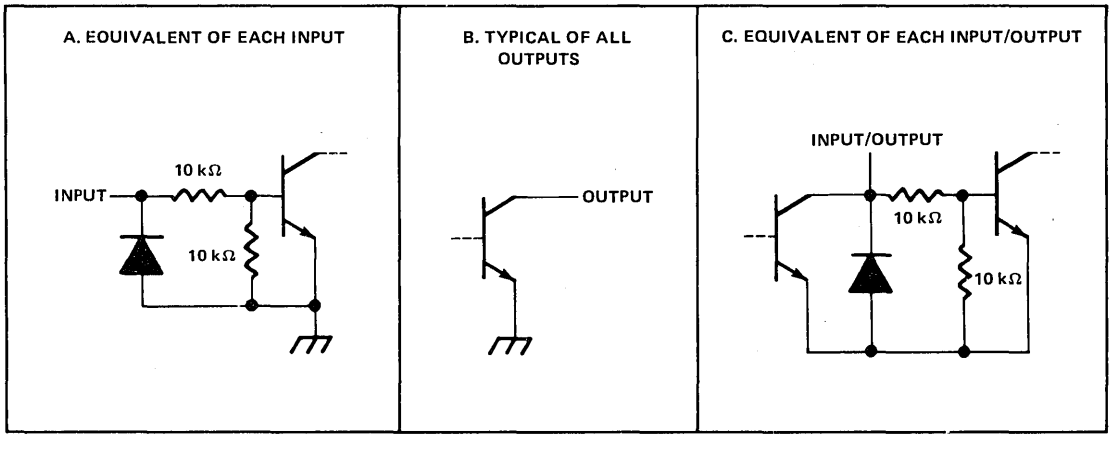


NOTE 1: ALL TIMING MEASUREMENTS ARE FROM 10% and 90% POINTS

SWITCHING CHARACTERISTICS

4.0 INPUT, OUTPUT, AND INPUT/OUTPUT STRUCTURES



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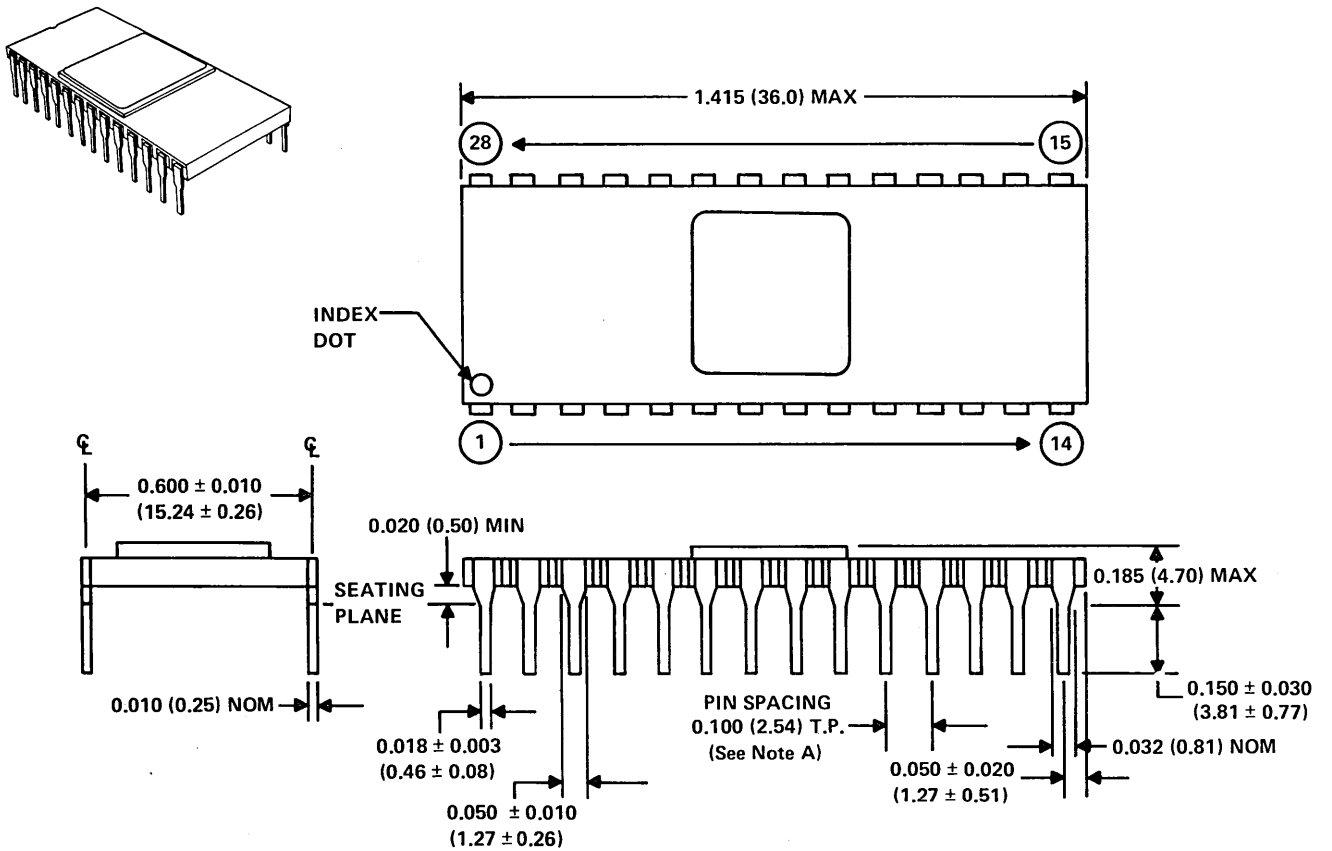

NOTES: A. EACH PIN CENTERLINE IS LOCATED WITHIN 0.100 OF ITS TRUE LONGITUDINAL POSITION.

B. ALL LINEAR DIMENSIONS ARE IN INCHES (AND PARENTHETICALLY IN MILLIMETERS FOR REFERENCE ONLY). INCH DIMENSIONS GOVERN.

SBP 9961
Interrupt Controller and Timer

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1.0 INTRODUCTION

1.1 GENERAL DESCRIPTION

The SBP 9961 Interrupt Controller and Timer is a ruggedized, monolithic, Communications Register Unit (CRU) programmable, multifunction systems support device fabricated with oxide separated Integrated Injection Logic (I^2L) technology. The SBP 9961 provides the SBP/TMS 9900 series Family of Microprocessors with a flexible independently clocked interval/event timer plus maskable prioritized interrupt encoding capability. I^2L technology enables the SBP 9961s static logic, and TTL compatible I/O, to operate over a very wide ambient temperature range from a single d-c power source. When the SBP 9961 is used in conjunction with the I^2L SBP 9960 CRU I/O Expander, the SBP 9961/SBP 9960 pair form an I^2L systems alternate to the N-channel MOS TMS 9901 Programmable Systems Interface device while maintaining strict compatibility with existing software handlers developed in support of the TMS 9901.

1.2 KEY FEATURES

- SBP/TMS 9900 Series Microprocessor Family Peripheral
- 15 Dedicated, Maskable, Prioritized, Encoded Interrupts
- 20 mA Current Sinking Outputs
- 40-Pin Package
- Independently Clocked 14-Bit Interval/Event Timer
- Software Compatible with TMS 9901 when used in conjunction with SBP 9960
- TTL Compatible I/O
- Wide Ambient Temperature Operation
  - SBP 9961CJ: 0°C to +70°C
  - SBP 9961EJ: -40°C to +85°C
  - SBP 9961MJ: -55°C to +125°C
  - SBP 9961NJ: -55°C to +125°C (with high-reliability processing)
- I^2L Technology
  - Constant Current Power Source
  - Fully Static Operation
  - Single Phase Edge-Triggering Clock
  - Wide Temperature Stability

2.0 FUNCTIONAL DESCRIPTION

2.1 SBP 9961/CPU INTERFACE

The SBP 9961 communicates with the CPU through the Communications Register Unit (CRU) interface as shown in Figures 1 and 4. The SBP 9961s CRU interface consists of: a) five CRU address select lines (S0-S4), b) a single chip enable ($\overline{CE}$), c) a 9961 to CPU serial data-bit line (CRUIN), d) a CPU to 9961 serial data-bit line (CRUOUT), and e) a CPU to 9961 serial data-bit clock (CRUCLK). When $\overline{CE}$ is activated (logic-level low), S0-S4 selects a specific CRU-bit function as indicated in Table 1. In the case of a SBP 9961 write operation, the datum is transferred from the CPU to the SBP 9961 via the CRUOUT line. The CRUOUT datum is strobed into the selected 9961 CRU-bit function by CRUCLK. In the case of a SBP 9961 read operation, the selected CRU-bit function is sampled by the CPU via the CRUIN line.

TABLE 1 – CRU BIT ASSIGNMENTS

CRU BIT	S0	S1	S2	S3	S4	CRU READ DATA	CRU WRITE DATA
0	0(4)	0	0	0	0	Control Bit	Control Bit(1)
1	0	0	0	0	1	$\overline{INT1}$/TIM1(2)	Mask1/TIM1(3)
2	0	0	0	1	0	$\overline{INT2}$/TIM2	Mask2/TIM2
3	0	0	0	1	1	$\overline{INT3}$/TIM3	Mask3/TIM3
4	0	0	1	0	0	$\overline{INT4}$/TIM4	Mask4/TIM4
5	0	0	1	0	1	$\overline{INT5}$/TIM5	Mask5/TIM5
6	0	0	1	1	0	$\overline{INT6}$/TIM6	Mask6/TIM6
7	0	0	1	1	1	$\overline{INT7}$/TIM7	Mask7/TIM7
8	0	1	0	0	0	$\overline{INT8}$/TIM8	Mask8/TIM8
9	0	1	0	0	1	$\overline{INT9}$/TIM9	Mask9/TIM9
10	0	1	0	1	0	$\overline{INT10}$/TIM10	Mask10/TIM10
11	0	1	0	1	1	$\overline{INT11}$/TIM11	Mask11/TIM11
12	0	1	1	0	0	$\overline{INT12}$/TIM12	Mask12/TIM12
13	0	1	1	0	1	$\overline{INT13}$/TIM13	Mask13/TIM13
14	0	1	1	1	1	$\overline{INT14}$/TIM14	Mask14/TIM14
15	0	1	1	1	1	$\overline{INT15}$/$\overline{INTREQ}$	Mask 15

NOTES: (1) 0 = Interrupt Mode; 1 = TIMCK Mode.
(2) Data present on $\overline{INT}$ input (or timer value) will be read regardless of mask value.
(3) While in the Interrupt Mode (Control Bit = 0), writing a "1" into a mask will enable interrupt, "0" will disable.
(4) When the SBP 9961/SBP 9960 pair are used in emulation of the TMS 9901, S0 is used to distinguish between activation of the 9961 (S0 = 0) v.s. the 9960 (S0 = 1).

2.2 INTERRUPT CONTROL

A block diagram of the SBP 9961 interrupt control section is shown in Figure 2. The interrupt inputs are sampled on the positive-going edge of CLOCK and are ANDed with their respective mask bits. If an interrupt input is active (low) and enabled (MASK = 1), the signal is passed through the priority encoder where the highest priority signal is encoded into a 4-bit binary word as shown in Table 2. This word, along with an interrupt request, is then output to the CPU on the positive-going edge of the next CLOCK.

The output signals will remain valid until either the corresponding interrupt input is removed, the interrupt is disabled (MASK = 0), or a higher priority enabled interrupt becomes active. When the highest priority enabled interrupt is removed, the code corresponding to the next highest priority enabled interrupt is output. If no enabled interrupt is active, $\overline{INTREQ}$ will be pulled to logic-level high with IC0–IC3 retaining the last asserted interrupt code. $\overline{RESET}$ (power-up reset) will force the interrupt code IC0–IC3 to (0,0,0,0) with $\overline{INTREQ}$ pulled high, and will reset all mask bits low (interrupts disabled). Individual interrupts can be subsequently enabled (disabled) by programming the appropriate mask bits. Unused interrupt inputs may be used as data inputs by disabling the interrupt (MASK = 0).

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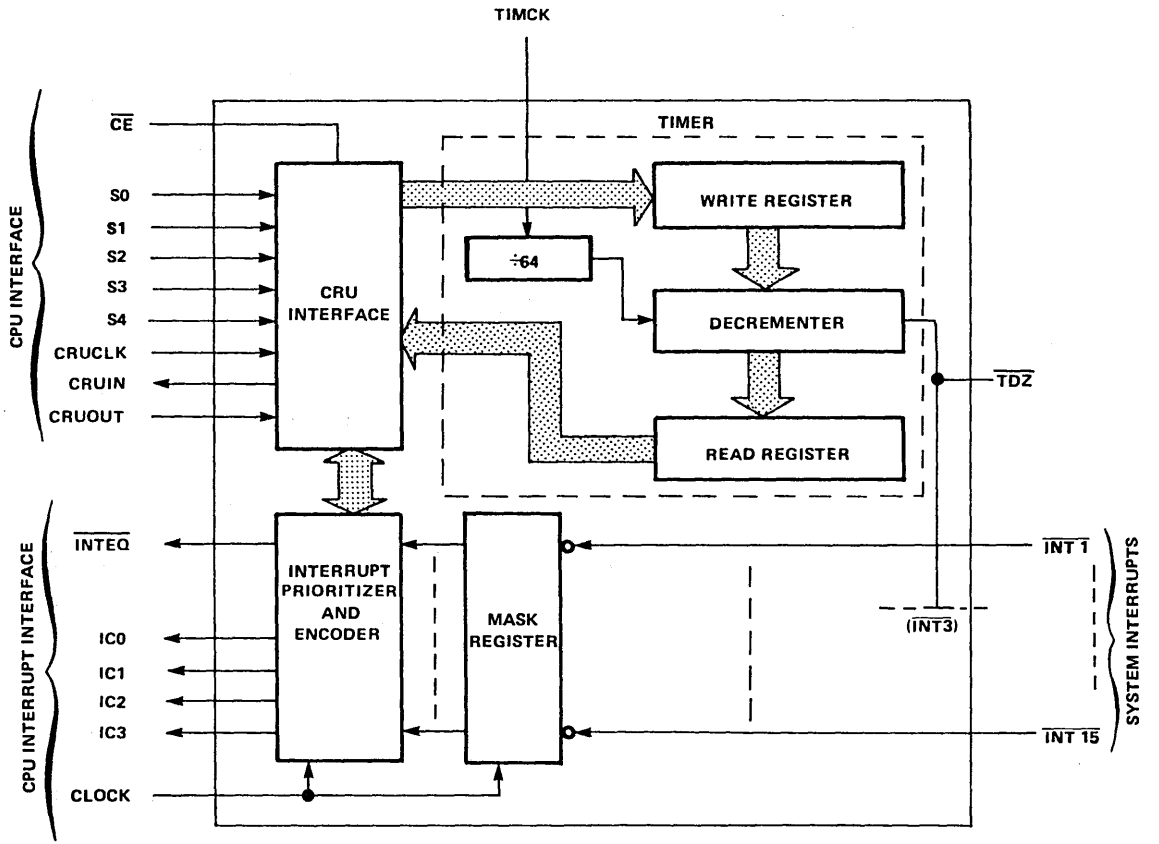

FIGURE 1 – SBP 9961 BLOCK DIAGRAM

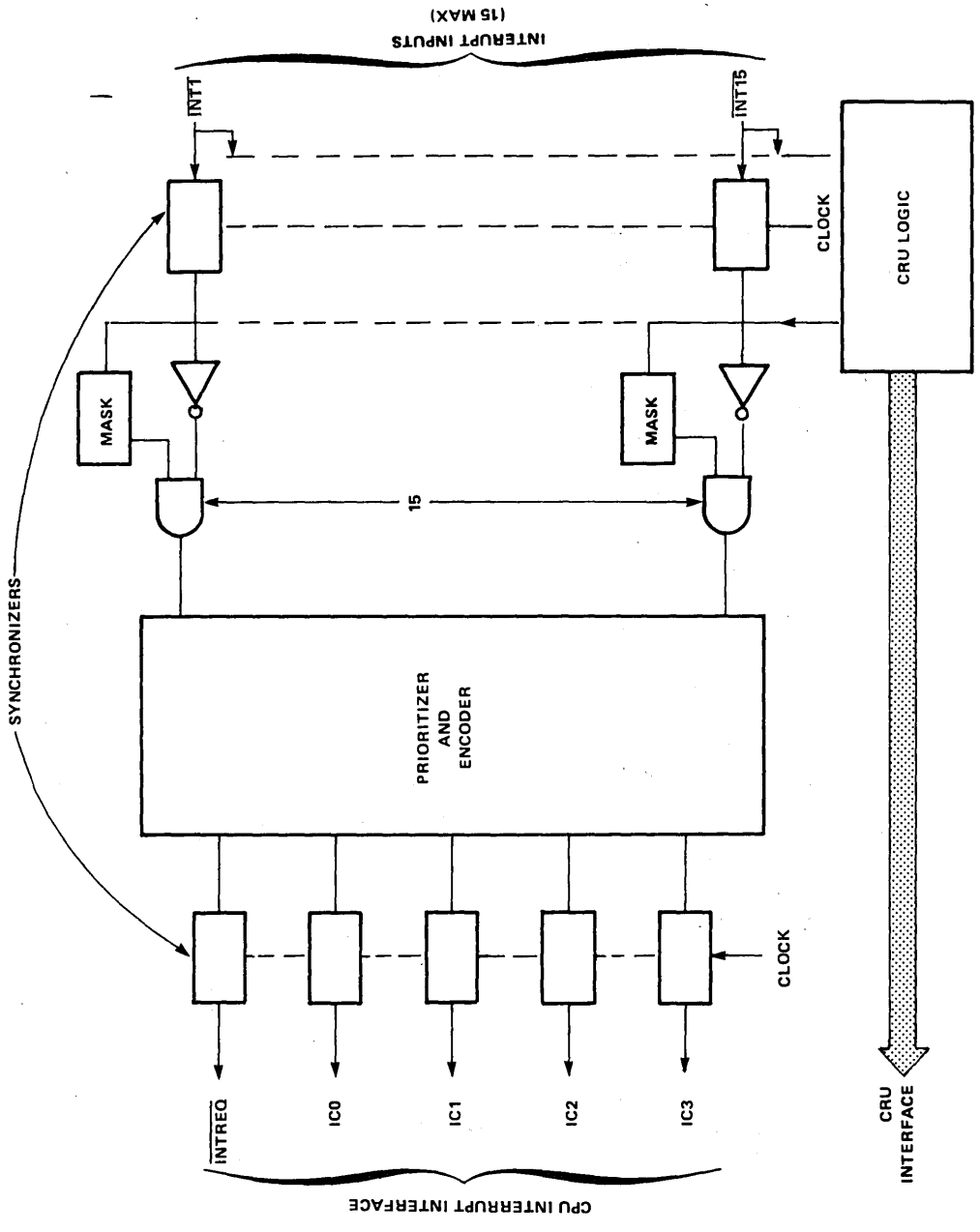

FIGURE 2 – INTERRUPT CONTROL LOGIC

TABLE 2
INTERRUPT CODE GENERATION

INTERRUPT/STATE	PRIORITY	I_{C0}	I_{C1}	I_{C2}	I_{C3}	$\overline{INTREQ}$
$\overline{INT}$ 1	1 (HIGHEST)	0	0	0	1	0
$\overline{INT}$ 2	2	0	0	1	0	0
$\overline{INT}$ 3/TIMER	3	0	0	1	1	0
$\overline{INT}$ 4	4	0	1	0	0	0
$\overline{INT}$ 5	5	0	1	0	1	0
$\overline{INT}$ 6	6	0	1	1	0	0
$\overline{INT}$ 7	7	0	1	1	1	0
$\overline{INT}$ 8	8	1	0	0	0	0
$\overline{INT}$ 9	9	1	0	0	1	0
$\overline{INT}$ 10	10	1	0	1	0	0
$\overline{INT}$ 11	11	1	0	1	1	0
$\overline{INT}$ 12	12	1	1	0	0	0
$\overline{INT}$ 13	13	1	1	0	1	0
$\overline{INT}$ 14	14	1	1	1	0	0
$\overline{INT}$ 15	15 (LOWEST)	1	1	1	1	0
NO INTERRUPT	–	Note 1	Note 1	Note 1	Note 1	1

(1) IC0-IC3 hold the level code of the previous interrupt.

3

2.3 INTERVAL TIMER

The SBP 9961's interval/event timer, shown in Figure 3, has the following operational features:

a) Independent clock input TIMCK

b) Programmable 14-bit decrementer

c) Timer-reaches-zero level-3 interrupt

d) Timer reaches zero output pulse $\overline{TDZ}$

e) Able to read the current decremented value and therefore function as an event timer

f) Able to determine the SBP 9961's operating mode and value of $\overline{INTREQ}$.

The SBP 9961 has an independent timer clock input, TIMCK, which allows the user to define an interval timer clock frequency other than that of the CPU. This, however, does not preclude the user option of connecting TIMCK to the CPU's CLOCK input and therefore running the interval timer at the CPU's clock frequency. The typical operating range of TIMCK is 0-5 MHz.

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The timer's CRU control bits are shown in Table 1. The SBP 9961 is placed into the timer-access mode by writing a logic-level high to the control bit located at CRU address zero. CRU bits 1-14 are then used to initiate the write-register with the desired start count. Writing a non-zero value to the write-register a) enables the decrementer, b) programs the third priority interrupt ($\overline{INT3}$) as the timer interrupt, and c) disables the influence of external interrupts on the $\overline{INT3}$ input pin. A single LDCR instruction can be used to accomplish the above initialization operation. After the write-register has been initialized with the desired start count, the timer begins decrementing toward zero. Upon reaching zero, the timer issues the level-3 interrupt, outputs the timer-zero pulse $\overline{TDZ}$, and restarts itself with the write-register value. Since the timer interrupt is latched, clearing that interrupt is accomplished by writing either a logic-level low or high to the respective interrupt mask bit at CRU address three. The CRUCLK that accompanies that write operation is the stimulus which resets the timers interrupt latch. However, in order to retain the current mask value, the appropriate SBZ or SBO CRU-write instruction must be executed unless the mask value itself is to be changed. At any point in the timer's decrement sequence, a timer restart can be accomplished by either reinitiating the entire write-register with an LDCR instruction, or by writing to any individual write-register bit with an SBZ or SBO instruction.

If the control bit is at logic-level low, the timer's read-register is updated with the current decrementer value after each decrement operation (once every 64 TIMCK clocks); if the control bit is at logic-level high (timer-access mode), the read-register retains its current value thereby ensuring that the read-register is not changed in the event a CRU read operation is executing during a decrement operation. Consequently, the current value of the timer's decrementer can be interrogated by 1) placing the SBP 9961 into the timer-access mode, and 2) performing a CRU-read operation on the timer's read-register through execution of an STCR instruction. The timer, then, can function as an event timer by reading the elapsed time between software events as shown in Table 3. Note that when accessing the timer, all interrupts should be disabled. The timer is disabled by either $\overline{RESET}$ (power-up reset) or by writing all zeroes to the write-register.

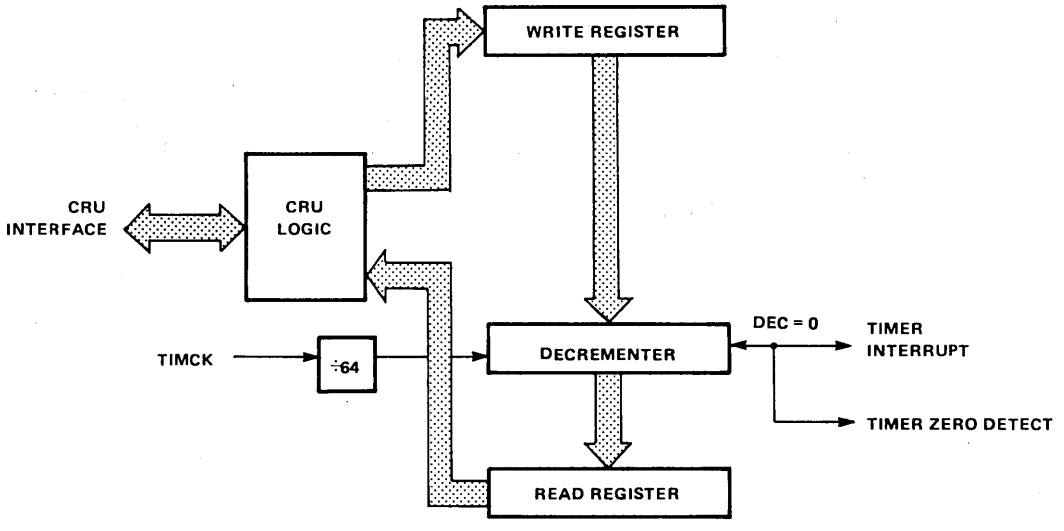

FIGURE 3 – INTERVAL/EVENT TIMER

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2.4 SBP 9961 STATUS

The SBP 9961s status can be determined by reading the value of the control bit located at CRU address zero. If the control bit has a logic-level low value, then the interrupt masks may be changed and data on the interrupt inputs may be read. However, access to the interval timer is inhibited. If the control bit has a logic-level high value, then the timer may be initiated, restarted, or read. Also, reading CRU address fifteen gives the status of $\overline{\text{INTREQ}}$ where logic-level low indicates activation.

TABLE 3 – SOFTWARE EXAMPLES

ASSUMPTIONS:
- Total of 6 interrupts are used
- RESET has been applied
- System uses timer at maximum interval

```
                LI      R12, CRUBAS     Setup CRU Base Address to point to 9961
                LDCR    @X,0            Program Timer with maximum interval
SYSTEM          LDCR    @Y,7            Re-enter interrupt mode and enable top 6 interrupts
SETUP           (X)-------------->FFFF
                (Y)-------------->7FXX
                .
                .
                .
                .
                BLWP    CLKVCT          Save Interrupt Mask
                .
                .
                .
CLKPC           LIMI    0               Disable Interrupts
                LI      R12, CRUBASE+1  Set up CRU base
                SBO     -1              Set 9961 into timer-access mode
                STCR    R4,14           Store read register into R4
                .
                .                       Process Timer Value
                .
                .
                SBZ     -1              Re-enter Interrupt Mode (i.e., Exit Timer-Access Mode)
                RTWP                    Restore Interrupt Mask
                .
                .
                .
CLKUCT          DATA    CLKWP,CLKPC
```

DESIGN GOAL
This document provides tentative information on a product in the developmental stage. Texas Instruments reserves the right to change or discontinue this product without notice.

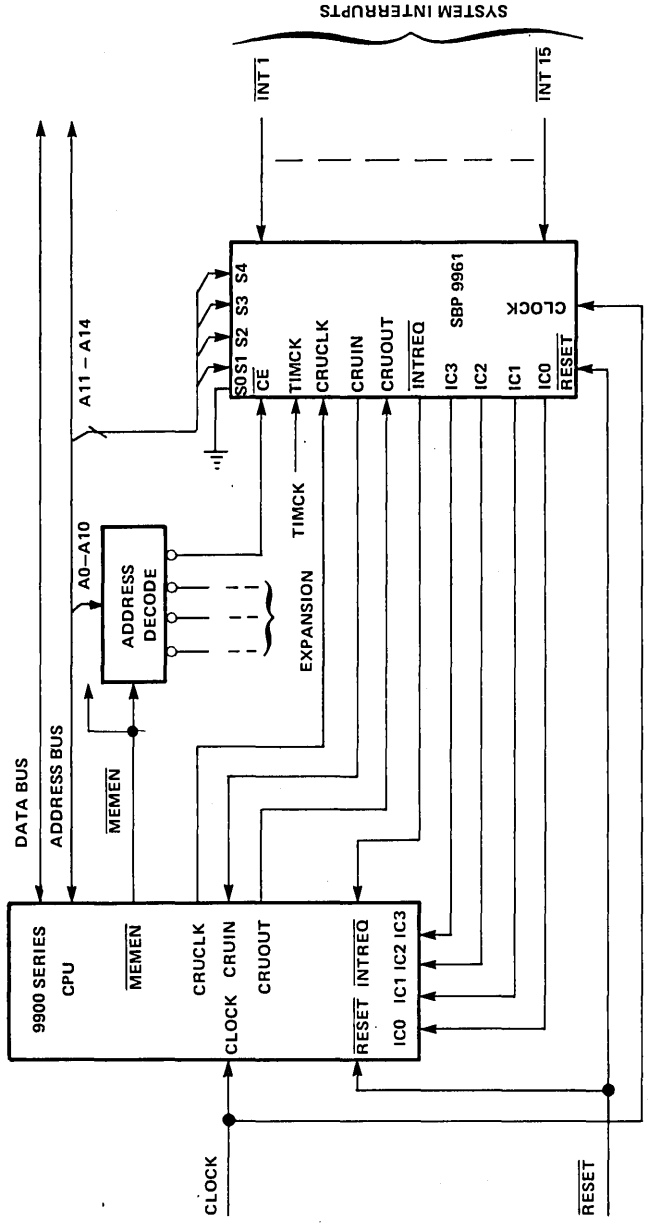

FIGURE 4 – SBP 9961 SYSTEM CONFIGURATION

DESIGN GOAL

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2.5 SYSTEM OPERATION

During power-up, $\overline{\text{RESET}}$ should be activated (low) to force the SBP 9961 into a known state. $\overline{\text{RESET}}$ will disable all interrupts, disable the timer, and force IC0-IC3 to (0,0,0,0) with $\overline{\text{INTREQ}}$ pulled high. System software should then enable the proper interrupts and program the timer (if used). See Table 3 for an example. After initial power up, the SBP 9961 is accessed only as needed to service the timer and enable or disable interrupts.

Figure 4 shows SBP 9961s system configuration. Figure 5 shows the use of a SBP 9961 with a SBP 9960 CRU I/O expander in emulation of the TMS 9901. (See *TMS 9901 Systems Interface Data Manual.*)

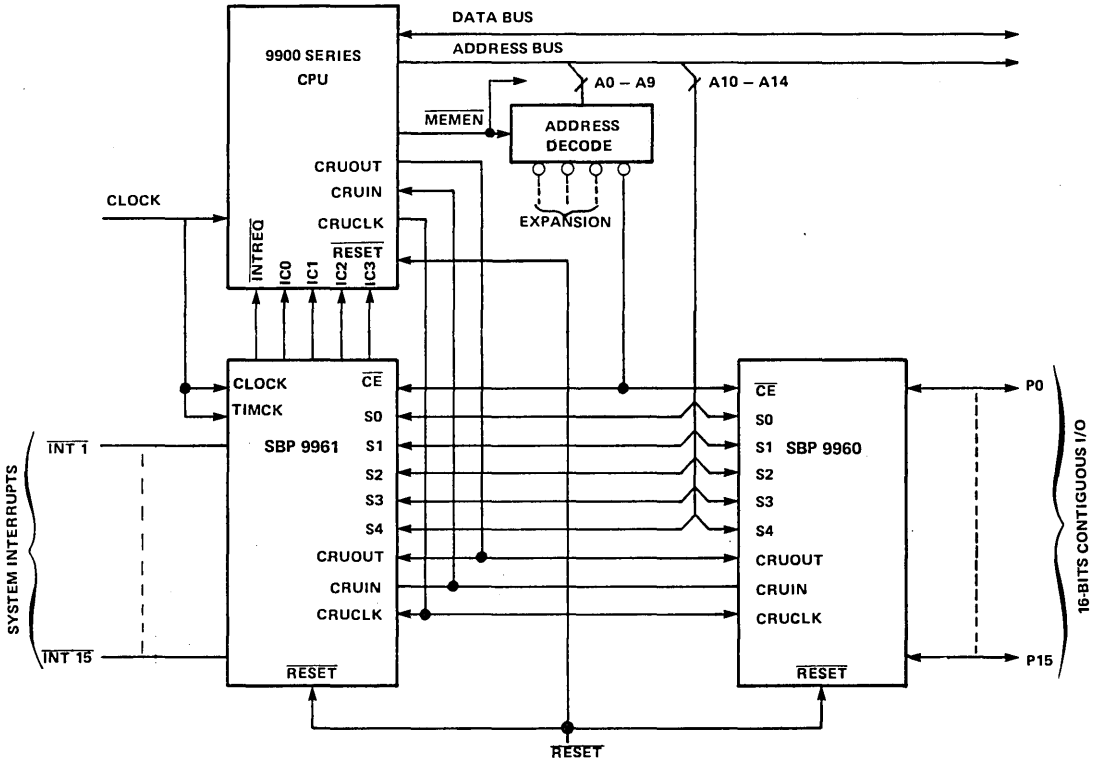

FIGURE 5 – SYSTEM CONFIGURATION USING SBP 9960 AND SBP 9961

DESIGN GOAL

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2.6 SBP 9961 PIN ASSIGNMENTS AND FUNCTIONS

SIGNATURE	PIN	I/O	DESCRIPTION
S0	33	IN	ADDRESS SELECT LINES. The data bit being accessed by the CRU interface is specified by the 4-bit code appearing on S1–S4. S0 is used as the high order select line when the SBP 9961 is used with the SBP 9960 in emulation of the TMS 9901. Otherwise, tie S0 to logic-level low.
S1	35	IN	
S2	31	IN	
S3	34	IN	
S4	32	IN	
CRUIN	28	OUT	CRU DATA IN (to CPU). Data specified by S0-S4 is transmitted to the CPU by CRUIN. When $\overline{CE}$ is not active, CRUIN is logic-level high.
CRUOUT	17	IN	CRU DATA OUT (from CPU). When $\overline{CE}$ is active, data present on the CRUOUT input will be sampled during CRUCLK and written into the CRU bit specified by S0-S4.
CRUCLK	1	IN	CRU CLOCK (from CPU). CRUCLK specifies that valid data is present on the CRUOUT line.
$\overline{RESET}$	38	IN	POWER-UP RESET. When active (low), $\overline{RESET}$ forces all interrupt masks to "0", and disables the clock.
$\overline{CE}$	2	IN	CHIP ENABLE. When active (low), data transfers may occur between the CPU and the SBP 9961.
TIMCK	11	IN	TIMER CLOCK IN. External clock used for the timer decrementer. May be externally tied to the CLOCK input pin.
$\overline{TDZ}$	30	OUT	TIMER DECREMENTER EQUALS ZERO. Low active pulse indicating that the timers decrementer contains a value of zero (all logic-level lows).
IC0	3	OUT	INTERRUPT CODE LINES (to CPU). IC0 (MSB) through IC3 output the binary code corresponding to the highest priority enabled interrupt most recently asserted.
IC1	4	OUT	
IC2	5	OUT	
IC3	6	OUT	
$\overline{INTREQ}$	7	OUT	INTERRUPT REQUEST (to CPU). When active (low) $\overline{INTREQ}$ indicates to the CPU that an enabled interrupt has been asserted, prioritized, and encoded.
CLOCK	9	IN	CPU SYSTEM CLOCK. Used by the SBP 9961 to synchronize the interrupt interface ($\overline{INTREQ}$, IC0-IC3) to the CPU.
INJ	40		Supply Current
GND	19, 20		Ground Reference
V_{CC}	37		Common voltage return/reference for all I/O pull-up resistors.
$\overline{INT1}$	12	IN	INTERRUPT INPUTS. When active (low), the signal is ANDed with its corresponding mask bit and if enabled sent to the interrupt control section. $\overline{INT1}$ has highest priority.
$\overline{INT2}$	13	IN	
$\overline{INT3}$	21	IN	
$\overline{INT4}$	14	IN	
$\overline{INT5}$	15	IN	
$\overline{INT6}$	16	IN	
$\overline{INT7}$	18	IN	
$\overline{INT8}$	8	IN	
$\overline{INT9}$	10	IN	
$\overline{INT10}$	22	IN	
$\overline{INT11}$	23	IN	
$\overline{INT12}$	25	IN	
$\overline{INT13}$	26	IN	
$\overline{INT14}$	27	IN	
$\overline{INT15}$	29	IN	

DESIGN GOAL

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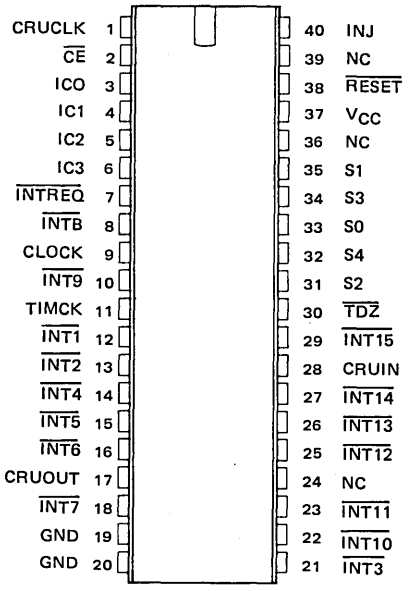

3.0 ELECTRICAL SPECIFICATIONS

3.1 RECOMMENDED OPERATING CONDITIONS, UNLESS OTHERWISE NOTED I_{CC}= 130 mA

PARAMETER		MIN	NOM	MAX	UNIT
Supply current, I_{CC}		115	130	145	mA
High-level output voltage, V_{OH}				5.5	V
Low-level output current, I_{OL}				20	mA
Operating free-air temperature, T_A	SBP 9961MJ, SBP 9961NJ	−55		125	°C
	SBP 9961EJ	−40		85	
	SBP 9961CJ	0		70	

3.2 ELECTRICAL CHARACTERISTICS (OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE, UNLESS OTHERWISE NOTED)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	I_{CC} = MIN,	I_I = −12 mA			−1.5	V
I_{OH}	High-level output current	I_{CC} = 130 mA, V_{IL} = 0.8 V,	V_{IH} = 2 V, V_{OH} = 5.5 V			−400	μA
V_{OL}	Low-level output voltage	I_{CC} = 130 mA, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 20 mA			0.5	V
I_I	Input current	I_{CC} = 130 mA,	V_I = 2.4 V		180		μA

†For conditions shown as MAX, use the appropriate value specified under recommended operating conditions

‡All typical values are at I_{CC} = 130 mA, T_A = 25°C.

DESIGN GOAL

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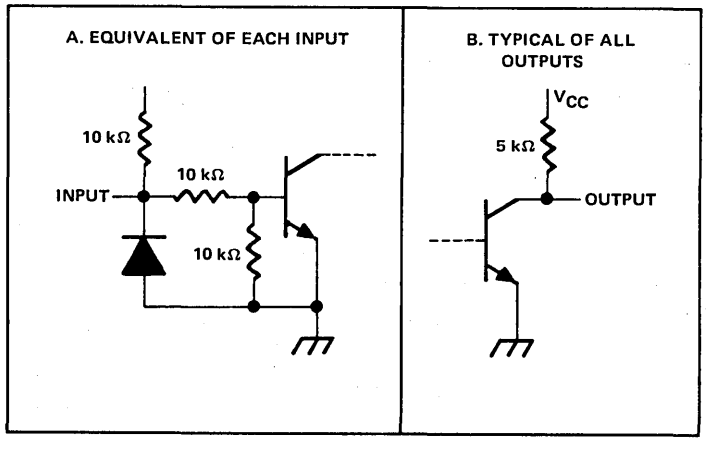
3.3 TIMING REQUIREMENTS OVER FULL RANGE OF OPERATING CONDITIONS

PARAMETER		MIN	NOM	MAX	UNIT
t_c	Clock cycle time	333			ns
t_r	Clock rise time		10	20	ns
t_f	Clock fall time		10	20	ns
t_{wL}	Clock pulse low width	111			ns
t_{wH}	Clock pulse high width	222			ns
t_{su}	Setup time for S0-S4, $\overline{CE}$, or CRUOUT before CRUCLK		200		ns
t_{su}	Setup time, input before valid CRUIN		200		ns
t_{su}	Setup time, interrupt before clock high		60		ns
$t_{w(CRUCLK)}$	CRU clock pulse width		100		ns
t_h	Address hold time		80		ns
t_{TC}	TIMCK cycle time		200		ns

3.4 SWITCHING CHARACTERISITICS OVER FULL RANGE OF RECOMMENDED OPERATING CONDITIONS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PD}	Propagation delay, ↑ CLOCK to valid $\overline{INTREQ}$, IC0-IC3	C_L = 25 pF, R_L = 5 kΩ		150		ns
t_{PD}	Propagation delay, S0-S4 or $\overline{CE}$ to valid CRUIN	C_L = 25 pF, R_L = 5 kΩ		330		ns

4.0 INPUT, OUTPUT, AND INPUT/OUTPUT STRUCTURES



DESIGN GOAL

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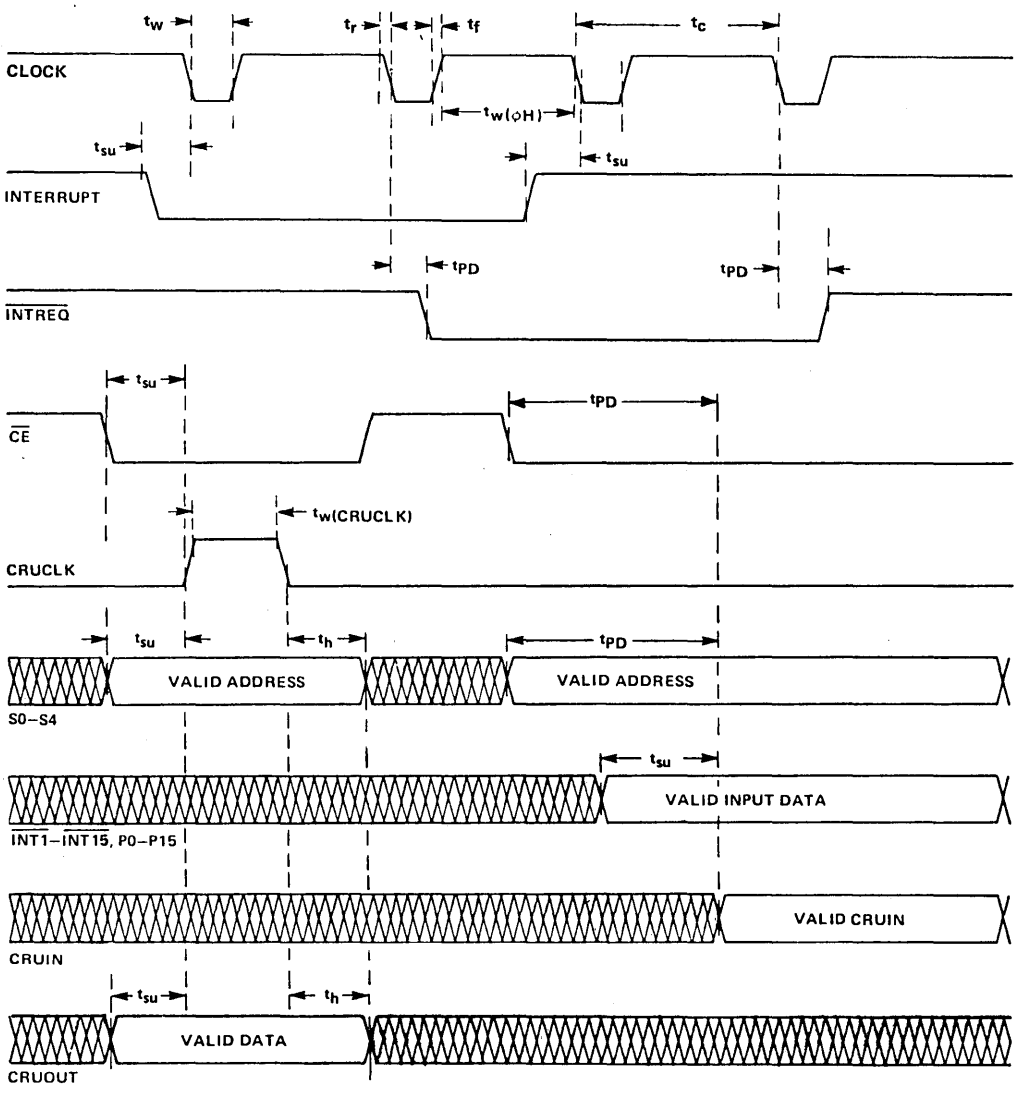

NOTE 1: ALL TIMING MEASUREMENTS ARE FROM 10% and 90% POINTS

SWITCHING CHARACTERISTICS

3

DESIGN GOAL

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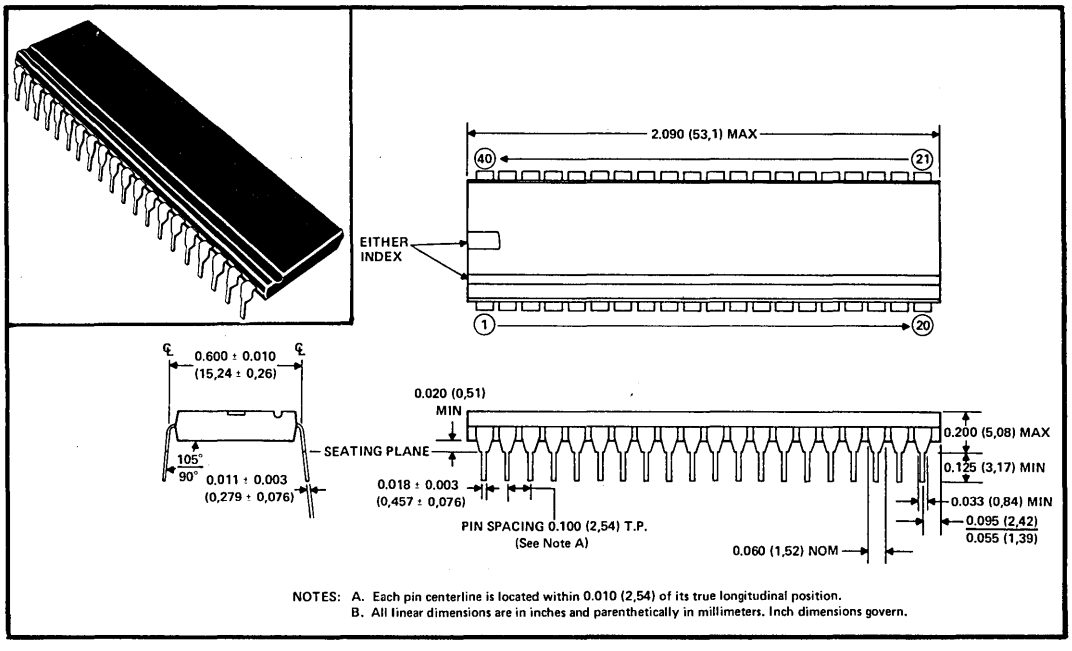
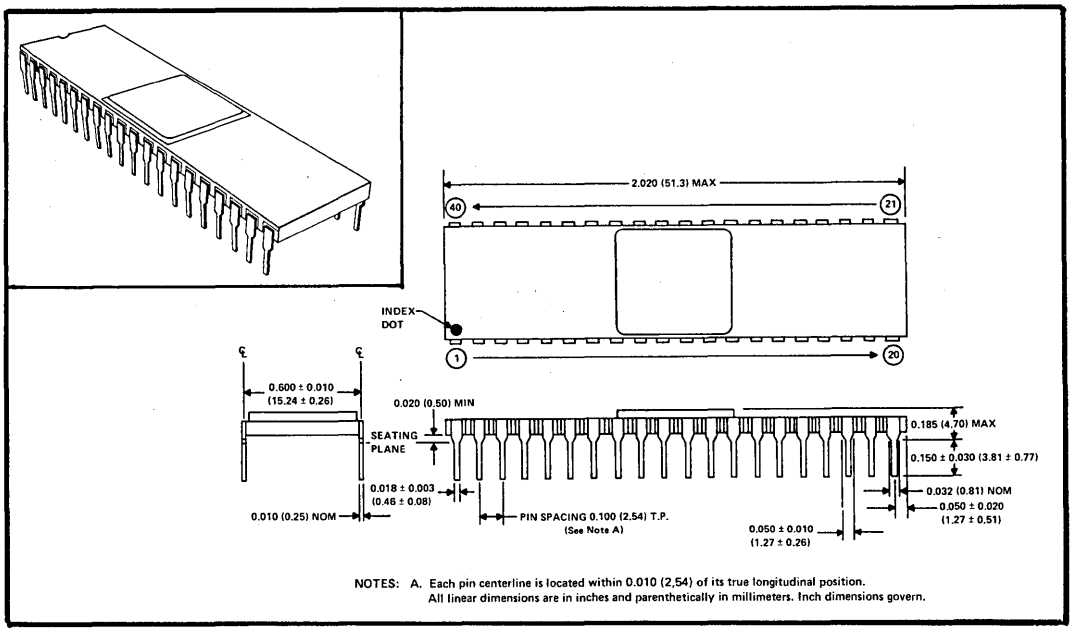
5.0 MECHANICAL DATA

5.1 40-PIN PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. Each pin centerline is located within 0.010 (2,54) of its true longitudinal position.
B. All linear dimensions are in inches and parenthetically in millimeters. Inch dimensions govern.

5.2 40-PIN CERAMIC DUAL-IN-LINE PACKAGE



NOTES: A. Each pin centerline is located within 0.010 (2,54) of its true longitudinal position.
All linear dimensions are in inches and parenthetically in millimeters. Inch dimensions govern.

Miscellaneous 9900 Family Products

TIMING CONTROLLER FOR THE SBP 9900A

- 14-Bit Interval Timer-Event Counter
- RESET and LOAD Synchronization
- SBP 9900A Clock Generation
- 20-Pin Package
- TTL Compatible Open-Collector I/O

DESCRIPTION

The SBP 9964 is a 14-bit interval timer-event counter, an SBP 9900A clock generator and an SBP 9900A RESET and LOAD signal synchronizer. The interval timer-event counter communicates with the SBP 9900A through the SBP 9900A's Communication Register Unit (CRU) I/O interface. The interval timer-event counter may be efficiently applied to a variety of applications in which the interval between external events, the number of external events, or the initiation of periodic events is desired. RESET and LOAD synchronizers provide for SBP 9900A compatible synchronization of these signals from asynchronously applied external signals.

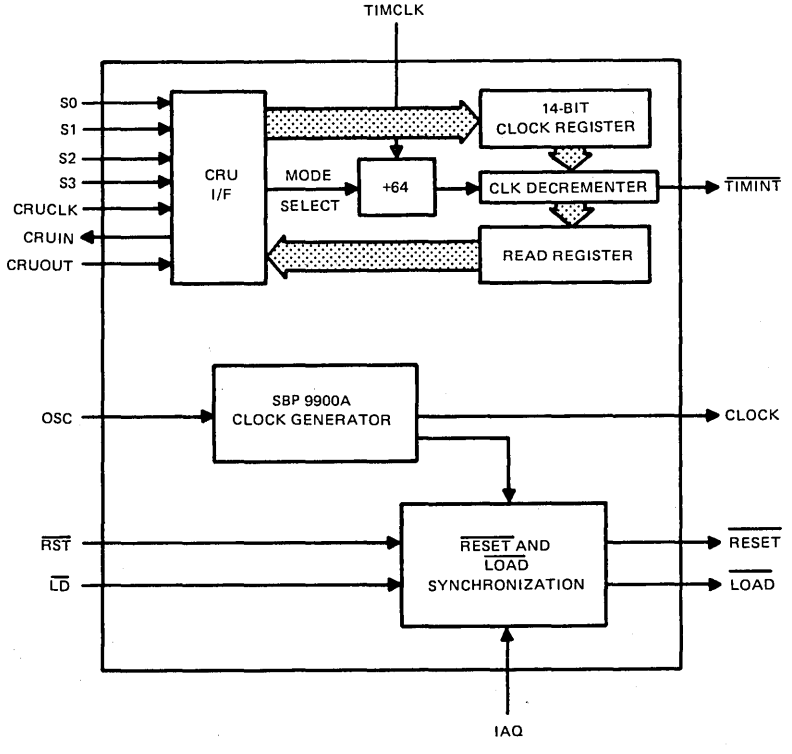


FIGURE 1 – FUNCTION BLOCK DIAGRAM

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

PERIPHERAL INTERFACE ADAPTER

- Microprocessor Memory-Mapped I/O Peripheral Interface
- Dual 8-Bit Input/Output Peripheral Ports
- Internal Mask Registers and Associated Compare Logic for Character/Data Recognition
- TTL Compatible Open-Collector I/O
- 40-Pin Package

DESCRIPTION

The SBP 9965 Peripheral Interface Adapter is a byte oriented, parallel memory-mapped, input/output interface which interfaces to microprocessor CPU's through the memory bus. Two 8-bit I/O ports with independent handshake lines are provided which allow a variety of byte oriented peripheral devices to be efficiently interfaced to the CPU. High data rates are effected through parallel transfers of data between the CPU and the peripheral device.

Two internal mask registers, one associated with each I/O port, may compare logic which flags the CPU whenever an equal condition exists between I/O and mask register data. This feature is useful for byte string searches or control character recognition.

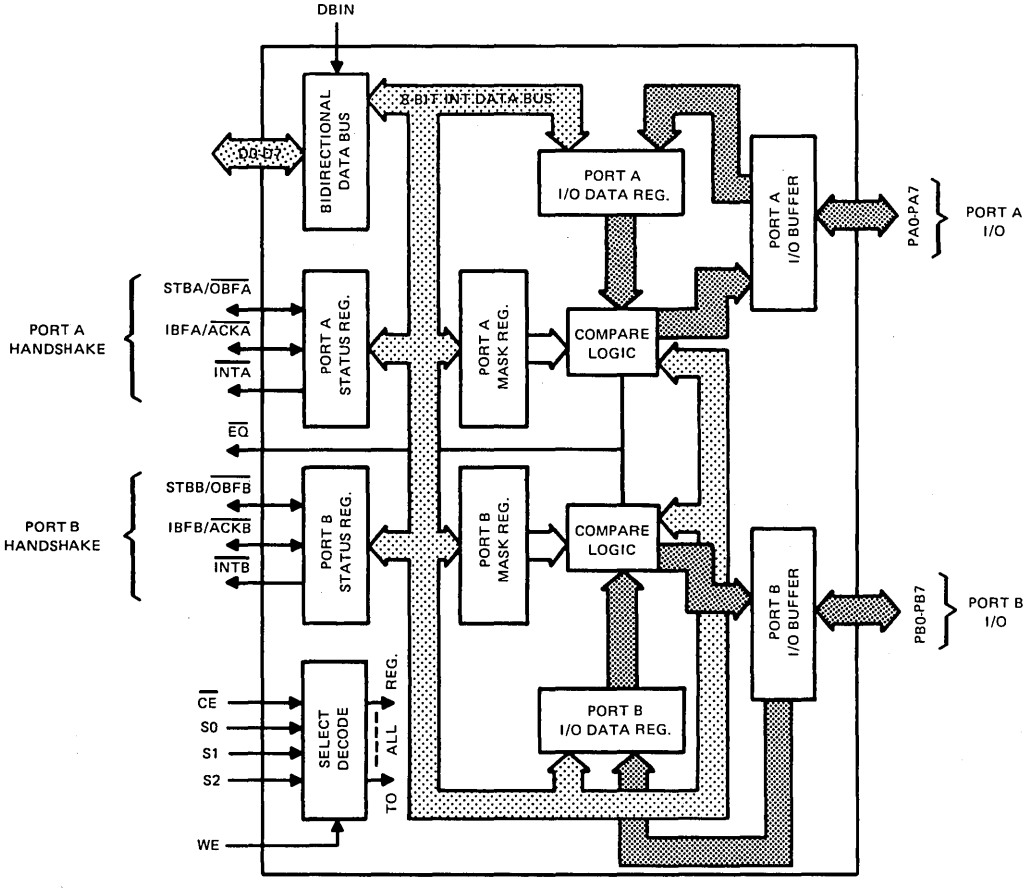


FIGURE 1 – FUNCTIONAL BLOCK DIAGRAM

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

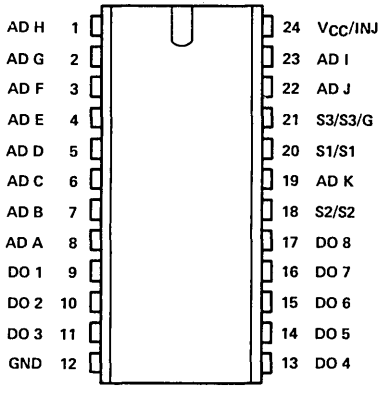
TYPES SBP 9818C, SBP 9818M
2048-WORD BY 8-BIT READ-ONLY MEMORIES

JUNE 1979

I^2L MASK-PROGRAMMABLE READ-ONLY MEMORIES

- TTL-Compatible Inputs and Outputs
- Industry Standard Pin Assignments in 24-Pin Plastic and Ceramic Dual-In-Line Packages
- Open-Collector Outputs

SBP 9818M . . . J PACKAGE
SBP 9818C . . . J OR N PACKAGE
(TOP VIEW)



description

These mask-programmed read-only memories offer the designer a wide range of options such as active-high or active-low memory-enable pins and strobe control for latched or transparent output flip flops (see Programmable Options Table). These flexible, high-density ROMs can provide the basis for cost-effective solutions to many design problems including those in large, fixed program memories with capability for code converters, constants, character generators, and look-up tables.

The SBP 9818M is characterized for operation over the full military temperature range of −55°C to 125°C. The SBP 9818C is designed for operation from 0°C to 70°C.

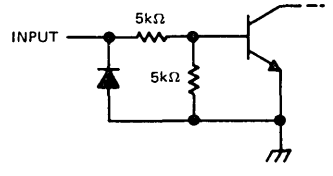
PROGRAMMABLE OPTIONS TABLE

PINS	MEMORY ENABLE		OUTPUTS
18	S2	S2	
20	S1	S1	
21	S3 No Output Latches	S3 No Output Latches	Strobe Controlled* Output Latches

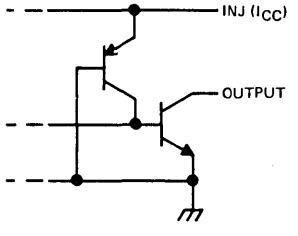
*A TTL high level at pin 21 will make the output flip flops transparent, a low TTL level latches the outputs.

schematics of inputs and outputs

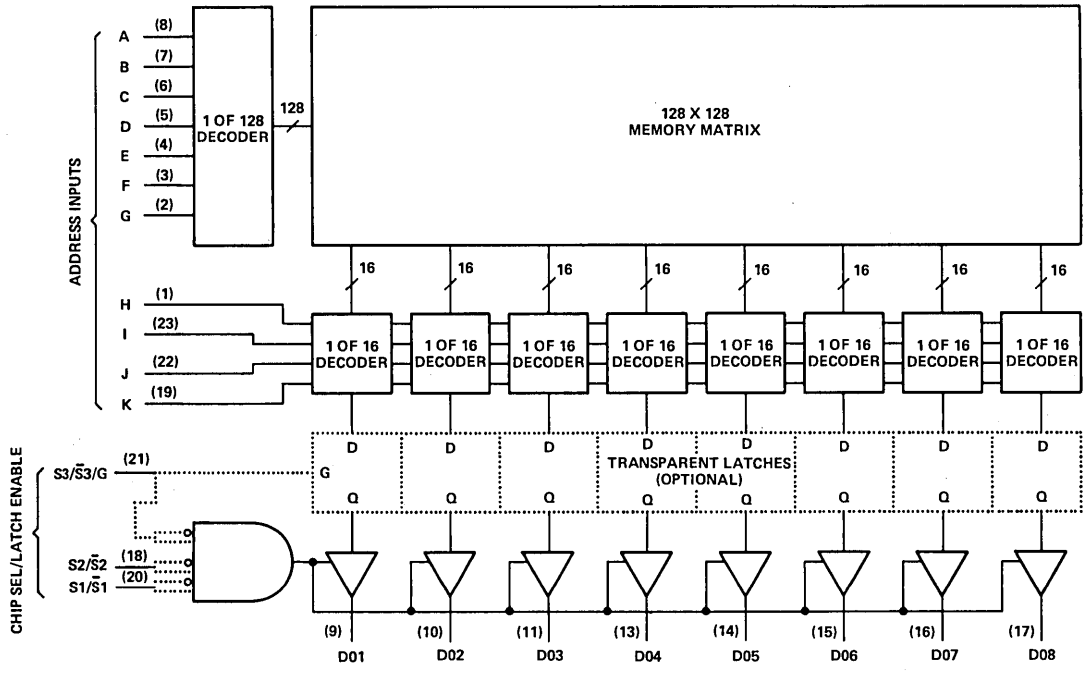
EQUIVALENT OF EACH INPUT



CURRENT INJECTED OPTION
TYPICAL OF EACH OUTPUT



functional block diagram



NOTE: ..... Indicates Programmable Options

recommended operating conditions

	SBP 9818C			SBP 9818M			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply current, I_{CC}	300		500	300		500	mA
Strobe pulse width, $t_{W(G)}$	100			100			ns
Address setup time, $t_{su(ad)}$	250↓			250↓			ns
Address hold time, $t_{h(ad)}$	50↓			50↓			ns
Operating free-air temperature, T_A	0		70	−55		125	°C

↓The arrow indicates that the high-to-low transition of the strobe input is used for reference.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	I_{CC} = 3 mA or V_{CC} = 5 V, I_I = −12 mA				−1.5	V
I_{OH}	High-level output current	I_{CC} = 300 to 500 mA	V_O = 2.4 V		100	200	μA
			V_O = 5.5 V		200	400	
V_{OL}	Low-level output voltage	V_{IH} = 2 V, I_{CC} = 300 mA,	V_{IL} = 0.8 V, I_{OL} = 16 mA		0.25	0.4	
I_I	Input current	V_I = 2.4 V			340		μA
		V_I = 0.4 V			25		

switching characterisitics, T_A = 25°C, C_L = 50 pF

PARAMETER		TEST CONDITIONS	TYP
$t_{a(ad)}$	Access time from address	I_{CC} = 300 mA	250 ns
$t_{a(S)}$	Access time from chip select		150 ns
$t_{a(G)}$	Access time from strobe		150 ns

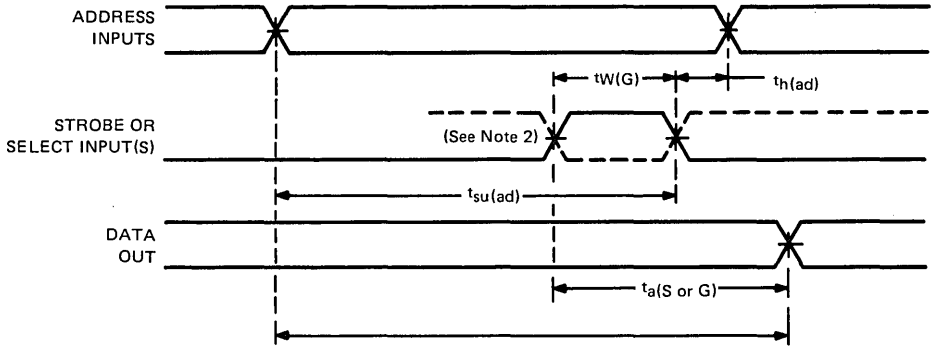

FIGURE 1 – TIMING DIAGRAM

NOTE 2: A typical strobe pulse is indicated by the solid waveform. Select inputs may be active high or active low (as indicated by the dashed reference line) and enable or disable the outputs for the duration of their steady active or inactive conditions respectively.

ORDERING INSTRUCTIONS

TO BE COMPLETED BY REQUESTOR

COMPANY: _____

ADDRESS: _____

_____

POSTAL ZIP CODE: _____

CONTACT (NAME): _____

PHONE: (Area Code)_____(NO.)_____

CUSTOMER PURCHASE ORDER NO: _____

CUSTOMER PRINT OR I.D. NO: _____

CUSTOMER PART NO: _____

SYMBOLIZE AS PART NO: _____

ROM MEMORY-ENABLE OPTIONS
(Choose one option for each pin):

A. PIN 18 (Check one) ☐ H = true enable ☐ L = true enable

B. PIN 20 (Choose one) ☐ H = true enable ☐ L = true enable

NOTES: 1. L = True enable pins will be logically true if left open.
2. All memory enable pins must be true to enable the outputs.

ROM LATCH/ENABLE OPTIONS
(Choose one option):

A. ☐ TRANSPARENT LATCH FOR EACH OUTPUT
(Pin 21 = H for transparency, L for storing)

B. ☐ NO LATCHES (Choose memory enable option for pin 21):

B1. PIN 21 (Choose one) ☐ H = true enable ☐ L = true enable

BIT PROGRAMMING INSTRUCTIONS

Programming instructions for each bit location of these read-only memories are solicited in the form of a sequenced deck of standard 80-column data cards providing the information requested below, and accompanied by a properly sequenced listing of these cards. Upon receipt of these items, a computer run will be made from the deck of cards which will produce a complete function table for the requested part. This function table, showing output conditions for each of the words, will be forwarded to the purchaser as verification of the input data as interpreted by the computer-automated design (CAD) program. This single run also generates mask and test program data; therefore, verification of the function table should be completed promptly.

Each card in the deck prepared by the purchaser identifies the words specified and describes the levels at the outputs for each of those words. All addresses must have all outputs defined and columns designated as "blank" must not be punched. The 512 cards should be punched according to the following data card format:

Column	
1-3	Punch a right-justified integer representing the binary input address (000-2044) for the first set of outputs described on the card.
4	Punch a "–" (Minus sign)
5-7	Punch a right-justified integer representing the binary input address (003-2047) for the last set of outputs described on the card.
8-9	Blank
10-17	Punch "H", "L", or "X" for bits eight, seven, six, five, four, three, two, and one (outputs DO 8, DO 7, DO 6, DO 5, DO 4, DO 3, DO 2, and DO 1 in that order) for the first set of outputs specified on the card. (See note 1.)
18	Blank
19-26	Punch "H", "L", or "X" for the second set of outputs.
27	Blank
28-35	Punch "H", "L", or "X" for the third set of outputs.
36	Blank
37-44	Punch "H", "L", or "X" for the fourth set of outputs.
45-49	Blank
50-80	Same as the '187 data card format, page 15.

TO BE COMPLETED BY TI

SPECIAL DEVICE NO: _____

SALES ORDER NO: _____

CONTACT (NAME): _____

LOCATION: _____

PHONE EXT: _____

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SBP/TMS 9900 TRANSPORTABLE CROSS-SUPPORT SOFTWARE PRODUCT DESCRIPTION

• PACKAGING

The SBP/TMS 9900 transportable cross-support package, which is now available for sales and distribution, is composed of three distinct products: 9900 Cross Assembler, Simulator, and ROM Utility. The part number for the package is *SYS9900/16F.X.* The *Product Name* is *TMS 9900 Transportable Cross-Support Software.* Initially, the package will be manufactured only on *½ inch, 9 track PE encoded* (IBM compatible) magnetic tape recorded at *1600 BPI.* The tape will be *un-labeled, un-blocked,* with *80 ASCII bytes per data record* and will contain *131 files.* The first file on the tape is a data file which contains:

a) A one-time descriptor for each file on the tape

b) A bill of materials (to verify that the complete package has been received), and

c) An errata list of problems and known solutions for the software version on that tape.

Each file on the tape is terminated by an EOF mark except for the last file which is terminated with a double EOF to indicate *end-of-logical tape.*

Included in the shipping package is a *User Manual* for each of the three programs and an *Installation Manual* covering each of the three programs (4 manuals, total).

• OPERATING ENVIRONMENT

The programs are written to conform to ANSI STANDARD X3.0 (1966) 16-BIT FORTRAN and are designed to execute on any minicomputer with the following minimum characteristics.

1) ANSI STANDARD X3.0 (1966) 16-BIT FORTRAN COMPILER

2) Two's complement arithmetic

3) Disc capacity for up to 7 simultaneously active sequential files.

4) A 20K-word user program-memory partition.

To date, the package has been extensively tested on the TI 990/10 under DX10V2.2, DEC PDP11/10 under RSX-11M (FIN IV PLUS), and System 370/160 under MVS.

• 9900 CROSS ASSEMBLER DESCRIPTION

The SBP/TMS 9900 Assembly Language source is translated by the 9900 Cross Assembler into relocatable linkable SBP/TMS 9900 Object module format. Both the source input and the object output are fully compatible with the FS 990 Prototype Development System and TMS time-sharing services (GE TERMINET, NCSS, and TYMSHARE).

• SBP/TMS 9900 SIMULATOR DESCRIPTION

The Simulator is patterned after and affords extensions to the SBP/TMS 9900 Simulator on GE TERMINET, NCSS and TYMSHARE. Object modules generated by the Cross Assembler along with "link-control" statements are input to the first stage of the simulator. The output from this stage, an *absolute,* non-relocatable load module, plus simulation/debug control statements to the second stage of simulation. This stage may be operated in "batchmode" or interactively (e.g., the simulation/debug control stream is entered to the Simulator from a Keyboard/Display device). In this second phase of Simulation the user's program logic is verified and the program's performance characteristics are ascertained. Performance parameterization is supported for considerations such as target system clock speed, memory characteristics, and I/O part descriptions. Debug features include multiple breakpoints, full instruction trace and snapshots, plus the normal inspect/modify for CPU registers. All program references may be made symbolically, using symbols defined in the user's source program.

• ROM UTILITY DESCRIPTION

When the application program has been satisfactorily verified, the object module may be input to the ROM Utility Program for translation into a format acceptable for production of a gate placement program (preparatory to mass production). Alternatively, the utility may be used to generate a BNPF formatted file which may be input to a PROM Programmer (DATA I/O) to produce a PROM version of the program. In all, there are 12 acceptable input formats and 12 output formats in support of the TMS 1000 and the SBP/TMS 9900 microprocessors.

AMPL . . . A COMPLETE MICROPROCESSOR PROTOTYPING LAB

The AMPL* Microprocessor Prototyping Lab combines the high performance 990 computer with the low-cost flexibility of the floppy disk to provide a complete microprocessor prototyping lab. The AMPL lab provides in-circuit emulation support, logic-state trace and analysis, read-only memory implementation aids, and SBP 9900A software development support. This microprocessor lab provides the user a dedicated design center where 9900-based systems can be developed in an integrated software-hardware design and debug sequence. Substantial savings in design cost and design time in each phase of new product development is ensured with this system.

The microprocessor lab is structured around the FS9900 system, a fellow member of TI's 990 computer family. The FS990 system includes the Model 911 Video Display Terminal dual floppy-disk drive and TX990/TXDS system software license, all packaged in a self-contained single-bay desk. The Texas Instruments Model 810 Printer option for the FS990 system provides the user a fast throughput for software listings, trace data, and other hard-copy output requirements.

In-Circuit Emulation Support

The SBP 9900A in-circuit emulation feature includes the SBP 9900A emulator, SBP 9900A buffer, and SBP 9900A target connector. This feature allows the SBP 9900A microprocessor-based system design engineer to simulate his target system by utilizing the dedicated 4096 words of emulator memory and the SBP 9900A microprocessor emulator. All functions of the proposed system can be simulated except input/output, and benchmark data can be tabulated.

SBP 9900A emulation is designed to aid the design engineer through each stage of his prototype implementation. Emulation control provided by the FS9900 system allows the design engineer to step through the developed code, setting breakpoints and instruction traces to start/stop tests at desired points within his code.

Two significant advantages included in the emulation feature are the use of dedicated emulator memory and the ability under interactive software control to switch back and forth between target system memory and emulator memory. The dedicated 4096 16-bit words of emulator memory provides a significant speed advantage over systems which utilize host system memory on a cycle-stealing basis. The faster, dedicated emulator is designed so that this dedicated memory can have precedence over target system memory so that even after target system memory is implemented, 9900 code changes can be quickly evaluated and tested before implementing this change in target system ROM/PROM.

Logic-State Trace

The logic-state trace feature adds a dramatic new dimension to the integration and checkout of the target system.

The FS9900 system trace/emulation features interactive on-line control and analysis to provide fast data reduction and programmable emulation control based on the results of this analysis.

The trace feature can be interconnected with the emulator module or it can utilize the general-purpose Trace Data Probe. When interconnected to the emulator, the design engineer can trace 256 events of both address and 16-bit data. The Trace Data Probe provides 20 individual logic-line trace probes.

These probes can be used by the design engineer to trace any TTL logic lines desired in his target system. The sampling rate can be controlled by a 10-megahertz internal clock or by an external clock up to 10 megahertz. Of the 20 trace probes, 4 have a special glitch latch feature and can detect noise pulses down to 10 nanoseconds in width.

In addition to the 20 trace data probes, 4 general-purpose trace clock qualifier probes are provided to allow the user to pre-qualify trace conditions based on logic-state conditions within his target system. By using the interactive programming features within the host FS990 system, the design engineer can define procedures and functions to automatically process incoming trace data from these events, perform data reduction looking for defined conditions, display or print only the desired results, or branch into other emulation/trace procedures. Thus, for example the design engineer can set qualifying conditions and start trace and emulation in a continuous cycle while looking for those random troublesome noise glitches. Upon detecting a glitch, the trace/emulation cycle can be programmed to pause momentarily, analyze and print conditions, and then continue the trace/emulation sequence looking for the next glitch. This feature can mean tremendous savings in manpower and design checkout time since the full speed and power of the 990 computer is processing the problem.

SBP 9900A-BASED

TM 990/110M MICROCOMPUTER

The TM 990/110M is an assembled, tested microcomputer module utilizing as its CPU the powerful, ruggedized, I^2L 16-bit SBP 9900A microprocessor. With RAM and ROM/EPROM included on board as well as programmable serial and parallel I/O, the TM 990/100M is a powerful single-board microcomputer. Since all address, data, and control lines are brought to the board connectors, the board can be expanded to use the entire capabilities of the SBP 9900A in larger systems. The TM 990/110M is also being reformatted to meet the form factor/ruggedness requirements of the U.S. Navy's standard electronic module (SEM) program.

Features

- SBP 9900A 16-bit CPU
- 1024 words of 4045 Static RAM
- 1K words of 2708 EPROM, expandable to 4K words using 2716 EPROMs
- SBP 9960/SBP 9961 programmable system interface
- TMS 9902 asynchronous communications controller
- EIA or TTY terminal interface option
- Fully expandable bus structure
- Designed to fit the 990/510 chassis
- TIBUG operating monitor.

Operation

The TM 990/110M microcomputer is a software compatible member of the SBP 9900A/990 family. The SBP 9900A is used as a CPU to provide 16 bits of processing power with a minicomputer instruction set which includes multiply and divide. The TM 990/110M module is designed for 3-MHz operation, utilizing the full 16 levels of prioritized interrupts and the advanced memory-to-memory architecture of the SBP 9900A. Additionally, the bus structures are set up to take advantage of the full 64K-byte memory-addressing capability of the SBP 9900A and the nonmultiplexed memory, I/O and interrupt buses.

Memory

The on-board memory includes both an EPROM/ROM section and a static RAM section. Four sockets are available for TMS 2708, TMS 2716 EPROM or TMS 4700, TMS 4732 ROM operation. Using the available jumper option, all four sockets can be populated with TMS 2716's, providing a maximum on-board EPROM capability of 4K words. The static RAM area consists of 1024 words of memory. Four TMS 4045's are included. The cycle time of this memory is 0.667 microseconds. The minimum area of EPROM/RAM area may not be used for off-board expansion. DMA control lines are also accessible on the bus.

Interrupts and Timers

Fifteen maskable interrupts plus the reset and load trap vectors are implemented. The SBP 9961 handles all 15 external interrupts which can be generated from either the bus connector or the SBP 9961 I/O bus. The SBP 9961 enables each level to be individually maskable under program control. Additionally, level 3 can be programmed to use the interval timer in the SBP 9961. Level 4 can be generated from the TMS 9902 as an interval timer or for three other serial interface conditions (see the *TMS 9902 Data Manual*). Two programmable timers, therefore, are available on board.

I/O

The serial I/O and the parallel I/O are handled over the dedicated I/O bus of the SBP 9900A, the communications register unit (CRU). The TMS 9902 acts as the controller for this asynchronous serial interface. The character length, baud rate (75 to 38,400), and parity and stop bits are programmable. Three optional types of interface are supported:

- EIA
- 20 mA neutral current loop TTY
- Private wire differential line driver/receiver.

The TM 990/110M board is delivered complete with a 25-pin RS-232 type female connector, and is jumper selectable to support EIA or TTY operation. The differential line driver is normally unpopulated (see *Options*). Also, the TMS 9903 synchronous communications controller can be utilized since the TMS 9902/9903 are socket compatible.

The parallel I/O is handled by the SBP 9900/SBP 9961 pair; 16 parallel lines are all interfaced to the top edge connector which as 40 pins on 0.100 inch centers. Additionally, eight parallel lines are interfaced to the bus connectors. All I/O lines are equipped with pullup resistors.

TIBUG

The TIBUG monitor TM 990/401-1 is normally supplied preprogrammed in the populated TMS 2708 EPROMs (see *Options*). Its operation is described in the *User's Manual* or the TM 990 Series literature.

Options

The TM 990/110M-1 board is equipped with two TMS 2708's preprogrammed with the TIBUG monitor, and the serial I/O is jumper selectable as EIA port or a TTY interface. The TM 990/110M-2 board is populated with two blank EPROMs, and a private wire differential line driver interface is populated instead of the TTY interface. Other software or accessories, such as the line by line assembler and the microterminal, may be ordered under separate part numbers.

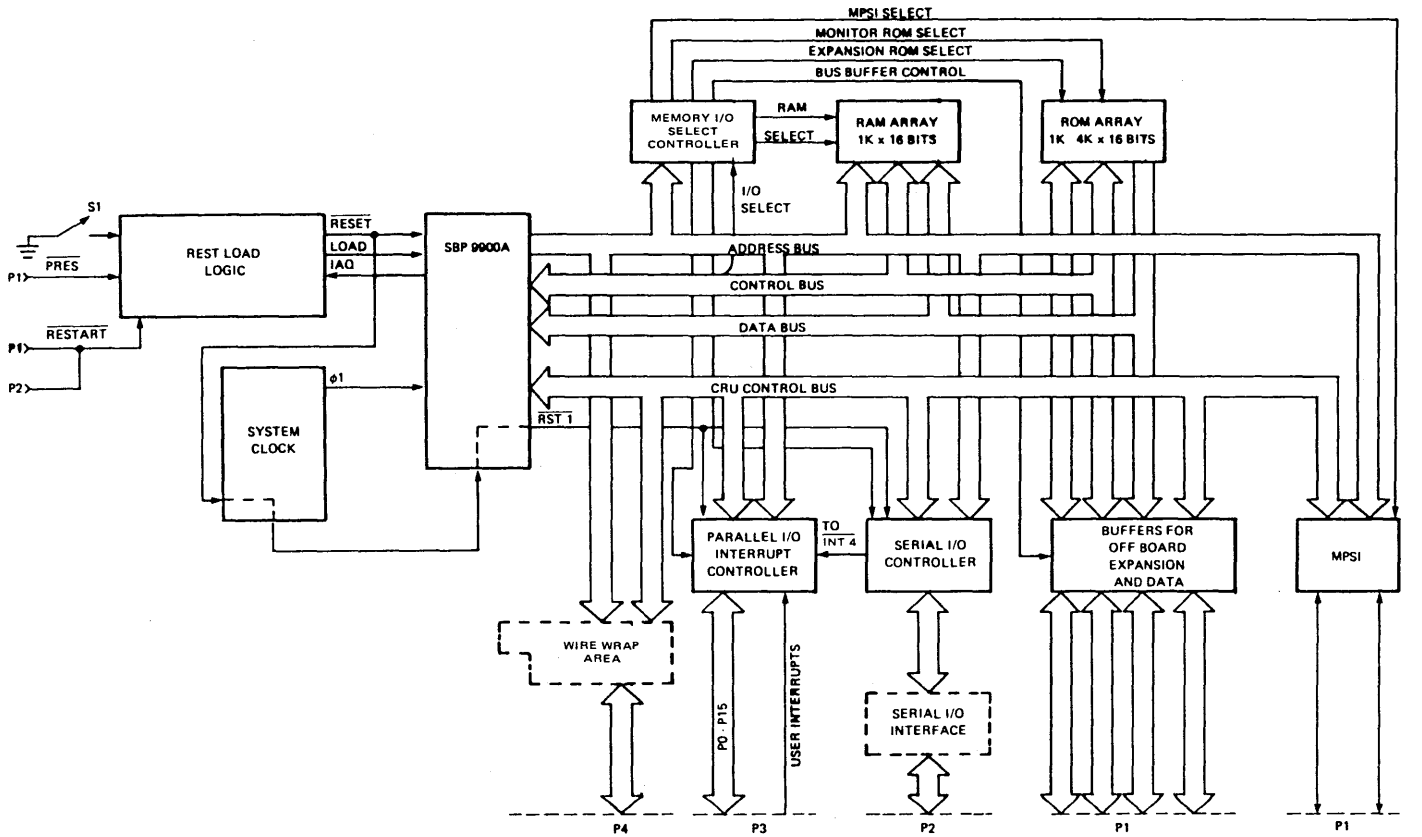


Figure F-1. TM 990/110 FUNCTIONAL DIAGRAM

Specifications

CPU: SBP 9900A

Instruction Set – 69 instructions
8, 16, or 32-bit operation
3 MHz System Clock

Interrupts: 16 levels – 15 may be external

Interval Timers: Two (in SBP 9961 and TMS 9902)

	Resolution	Maximum Interval
SBP 9961	21.3 μsec	349 msec
TMS 9902	64 μsec	16.32 msec

Memory: 16-bit word configuration

On-board EPROM/ROM, 1K words, expandable to 4K
On-board RAM, 1024 words
Off-board expansion to full 32K words

I/O

Parallel: 16 lines (expandable to 4K total I/O using CPU)

Serial: Asynchronous Controller TMS 9902
5–8 bit character
Programmable data rate, stop bits, parity

Baud Rates (bps):

75	2400
110	4800
150	9600
300	19,200
600	38,400
1200	

Interfaces

Bus:	Data and Address	Three-state TTL compatible buffered output
	Control	TTL compatible
Parallel I/O and Interrupts:		TTL compatible
Serial I/O:		RS-232, 20 mA current loop or differential line driver

Software

TIBUG monitor self-contained in EPROM

Mating Connectors

Bus	100 pin, 0.125 in.	TI	H321150 (wire wrap)
		TI	H322150 (solder tail)
Parallel I/O	40 pin, 0.100 in.	TI	H311120 (wire wrap)
		3M	3464-0001 (no ears)

FIBER-OPTIC COMPONENTS

TYPES SN74LS462, SN74LS463
FIBER-OPTIC DATA-LINK CONTROLLERS

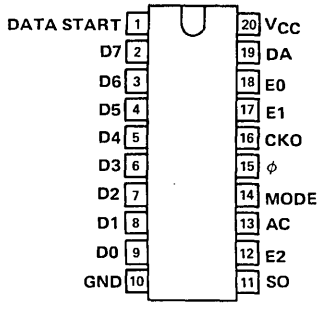
AUGUST 1979

- Inexpensive, Reliable Alternative to Conventional Copper-Wire Systems
- Single 5-Volt Supply
- Inputs and Outputs Compatible with TTL and Low-Level MOS
- Data Rate of 1 Megabit/Second
- Byte-Oriented Expansion Capability for 16-Bit Applications
- Interfaces With a Wide Range of Optical-Link Components
- Space-Saving 20-Pin 300-Mil Package

SN74LS462 TRANSMITTER

- Drive Current Up To 200 mA
- Three Operational Modes:
  Continuous Data Stream
  DC Sync (8-Bit or 16-Bit Bursts)
  AC Sync (8-Bit or 16-Bit Bursts)
- Automatic Start-Up

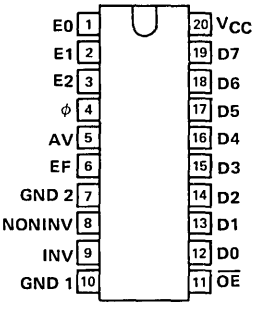
SN74LS462
J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



SN74LS463 RECEIVER

- Input Sensitivity of 1 μA
- Error Indication
- 3-State Parallel Data Outputs
- Isolated Comparator Ground For Improved Common-Mode Noise Rejection

SN74LS463
J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

The SN74LS462 transmitter and SN74LS463 receiver are designed for use in optical-wave data-transmission systems. Fabricated with oxide-isolated Integrated Injection Logic (I^2L) and low-power Schottky† TTL technology, these devices are operated from a single 5-volt dc power source and are completely TTL-compatible on all inputs and outputs. The SN74LS462/SN74LS463 transmitter/receiver pair are designed to provide the appropriate encoding, synchronizing, and decoding logic necessary control the transmission of digital data through a wide variety of serial fiber-optic data-link assemblies.

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†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U.S. Patent Number 3,463,975.

description (continued)

The basic fiber-optic data link shown in Figure 1 consists of five stages; encoding logic, which converts parallel data to be transmitted into a modulated serial data stream; a transducer (source) to convert the electrical serial data stream into optical logic levels (LED on or off); an optical waveguide (fiber) for transmission of the optical data stream; a transducer (detector), which converts the optical levels back into electrical logic levels; and lastly, decoding logic to convert the modulated serial data stream back into parallel output data.

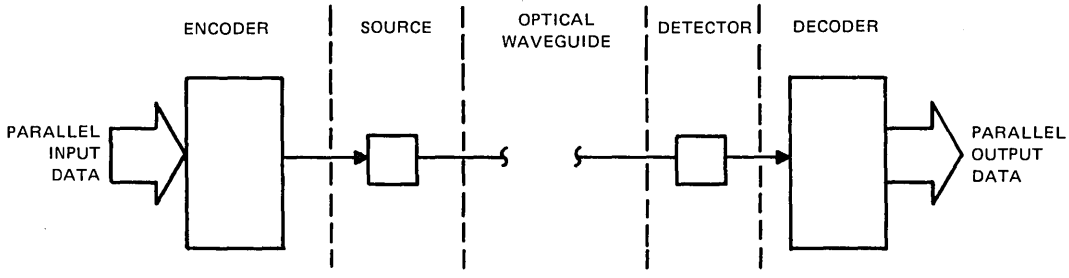


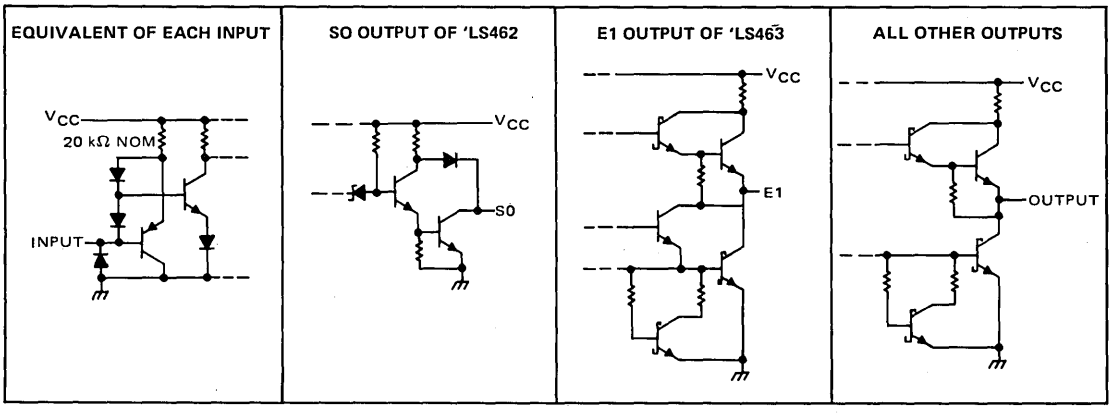
FIGURE 1 – TYPICAL SIMPLEX FIBER-OPTIC DATA LINK

The functions of encoding and decoding are efficiently provided by the SN74LS462 transmitter and SN74LS463 receiver, respectively, by incorporating all of the necessary logic in space-saving, 20-pin, 300-mil packaging. Transducer functions and transmission fibers can be selected from a wide variety of plastic, glass, or silica assemblies now available including Texas Instruments TXE series of low-cost, all plastic, source, detector, and fiber-cable assemblies.

The SN74LS462 transmitter accepts eight-bit parallel data inputs, encodes this data into frequency-shift coding (FSC), and transmits this information in the user-selected operating mode out of the serial output. (For an explanation of frequency-shift coding, see the "Operation" section of this data sheet). The serial output is capable of driving directly an infrared-emitting diode (IRED), which is coupled through a fiber-optic cable to a PIN detector diode. The SN74LS463 receiver then accepts very low-level currents from the PIN detector into an internal transimpedance amplifier, which amplifies this signal to the level required by the logic. The receiver then decodes the serial data stream and reconstructs the eight bits of parallel data originally transmitted. The parallel data word may be expanded to 16-bits through the addition of four standard low-power Schottky components interfaced to the transmitter's and receiver's expand pins. Both transmitter and receiver require either a crystal or TTL-level clock connected to the ϕ input.

More detailed information on the functions of these controllers is included elsewhere in this data sheet in the section entitled "Operation".

schematics of inputs and outputs



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SN74LS462

PIN	SIGNATURE	FUNCTION
1	DS	Data start input loads data into the buffer register on the low-to-high-level transition provided that the data acknowledge output is high.
2	D7	Parallel data inputs.
3	D6	
4	D5	
5	D4	
6	D3	
7	D2	
8	D1	
9	D0	
10	GND	Ground.
11	SO	Serial output provides a signal capable of driving an infrared-emitting diode (200 mA maximum). SO is connected to the cathode of the diode, and the anode is connected to five volts through a 33-ohm resistor.
12	E2	Expand-2 input accepts inverted data from an external eight-bit shift register for 16-bit operation.
13	AC	AC sync input, which, if mode input is high, selects the AC mode of operation when high and the DC mode when low.
14	MODE	Mode input when high allows the AC input to select either AC sync mode or DC sync mode. When low (and AC is low), it selects the continuous mode of operation.
15	ϕ	Clock input for crystal or TTL clock. (Clock frequency = 8X data rate).
16	CKO	Clock output provides clock frequency to the receiver at the same location when bidirectional operation is required.
17	E1	Expand-1 output shifts data out of the external shift register for 16-bit operation. For eight-bit operation this is an input and it must be high.
18	E0	Expand-0 output loads external serial shift register for 16-bit operation.
19	DA	Data-acknowledge output provides a signal that, when high, indicates that the buffer register is ready to accept data. It goes low approximately 250 ns after a low-to-high-level transition of data start thereby acknowledging the input of data.
20	V_{CC}	+5V Supply.

SN74LS463

PIN	SIGNATURE	FUNCTION
1	E0	Expand-0 output supplies serial data to an external shift register for 16-bit operation.
2	E1	Expand-1 output supplies a clock signal to an external serial shift register for 16-bit operation. For eight-bit operation this is an input and should be shorted to V_{CC}.
3	E2	Expand-2 output provides a signal to load data from the external serial register to the external parallel-output buffer register for 16-bit operation.
4	ϕ	Clock input for crystal or TTL clock. (Clock frequency = 8X data rate).
5	AV	Data-available output goes high when a demodulated word is transferred from the serial shift register to the parallel-output buffer register. This output is self-clearing: it goes inactive (low) typically 800 nanoseconds after going high.
6	EF	Error-flag output goes high if a data bit times out during the transmission of 8 or 16 bits of data; that is, if an FSC transition has not occurred in 10 clock periods. It will then remain high (and AV will be inhibited [low]) until 8 bits (or 16 bits for 16-bit operation) have been received without a time-out error occurring on any bit.
7	GND2	Comparator ground.
8	NONINV	Noninverting comparator input from the infrared-detecting diode.
9	INV	Inverting comparator input from the infrared-detecting diode.
10	GND1	Digital ground.
11	$\overline{OE}$	Output enable input, which, when low, enables the buffer register outputs and when high, forces the buffer register outputs into the high-impedance state.
12	D0	Buffer register data outputs.
13	D1	
14	D2	
15	D3	
16	D4	
17	D5	
18	D6	
19	D7	
20	V_{CC}	+5 V Supply.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, any logic input . . . . . 7 V
Off-state output voltage, SN74LS463 data outputs . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

recommended operating conditions

		SN74LS462			SN74LS463			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.75	5	5.25	4.75	5	5.25	V
Off-state output voltage, SN74LS463 data outputs							5.5	V
High-level output voltage, SO output				5.5				V
High-level output current, I_{OH}				−400			−400	μA
Low-level output current, I_{OL}	SO output			200				mA
	E1 output						3	
	other outputs			8			8	
Operating free-air temperature, T_A		0		70	0		70	°C

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN74LS462			SN74LS463			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level logic input voltage				2			2			V
V_{IL}	Low-level logic input voltage						0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_T	Comparator input threshold voltage		V_{CC} = MAX						1.2		V
	Comparator input current		V_{CC} = MAX					1		100	μA
V_{OH}	High-level output voltage (any output except SO)		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = 0.4 mA	2.4			2.4			V
V_{OL}	Low-level output voltage	SO output	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = MAX			0.5				V
		E1 output				0.35	0.5		0.35	0.5	
		other outputs				0.35	0.5		0.35	0.5	
I_{OH}	High-level output current, (SO output)		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, V_{OH} = 5.5 V			4				mA
I_{OZH}	Off-state output current, high-level voltage applied (D0-D7 outputs)		V_{CC} = MAX, V_O = 2.7 V	V_{IH} = 2 V,						50	μA
I_{OZL}	Off-state output current, low-level voltage applied (D0-D7 outputs)		V_{CC} = MAX, V_O = 0.4 V	V_{IH} = 2 V,						−50	μA
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V						1	mA
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.4 V			20			20	μA
I_{IL}	Low-level input current		V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC}	Supply current		V_{CC} = MAX				100			100	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

4

timing requirements over recommended ranges of T_A and V_{CC}

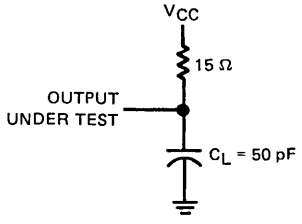
PARAMETER		SN74LS462			SN74LS463			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$t_{c(\phi)}$	Clock cycle time	100			100			ns
$t_{r(\phi)}$	Clock rise time						18	ns
$t_{f(\phi)}$	Clock fall time		9				18	ns
$t_{w(\phi)}$	Clock pulse width	50			50			ns
t_{su}	Setup time, data in before data start	15						ns
t_h	Hold time, data in after data start	30						ns

switching characteristics over recommended ranges of T_A and V_{CC}

PARAMETER		TEST CONDITIONS	SN74LS462			SN74LS463			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_d	Delay time, data start high to data acknowledge low	See Figures 2 and 3		450					ns
t_d	Delay time, data in to serial out			250					ns
t_d	Delay time, output enable to data out						35		ns
t_d	Delay time, data in to data available							400	ns
t_d	Delay time, invalid data to error flag							300	ns
t_d	Delay time, clock (ϕ) input to clock output			30					ns
t_w	Pulse width, data available high							800	ns

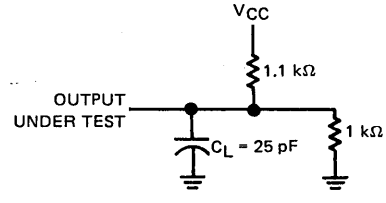
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION



C_L includes probe and jig capacitance

SN74LS462 LOAD CIRCUIT



C_L includes probe and jig capacitance

SN74LS463 LOAD CIRCUIT

FIGURE 2 – LOAD CIRCUITS

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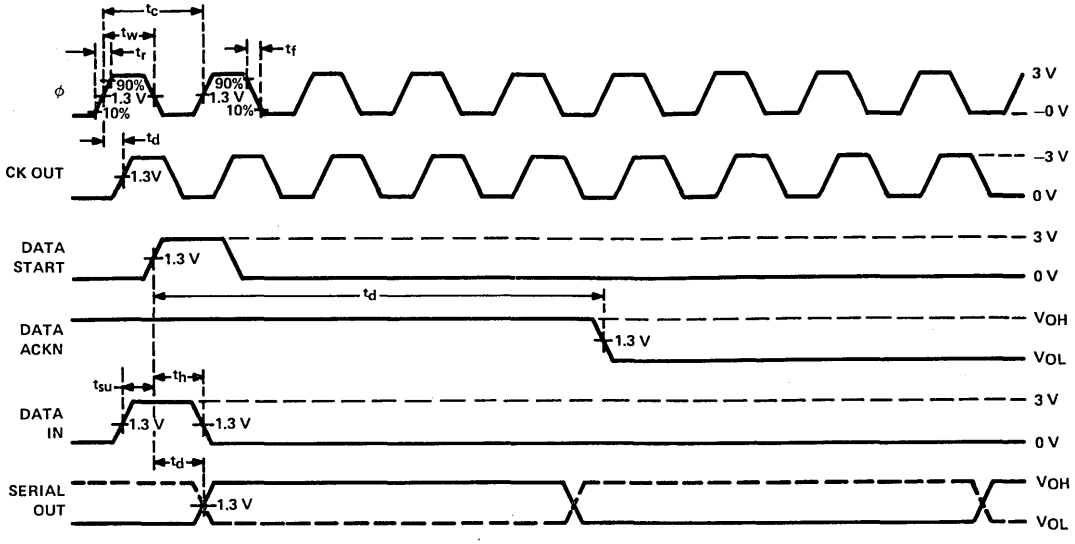
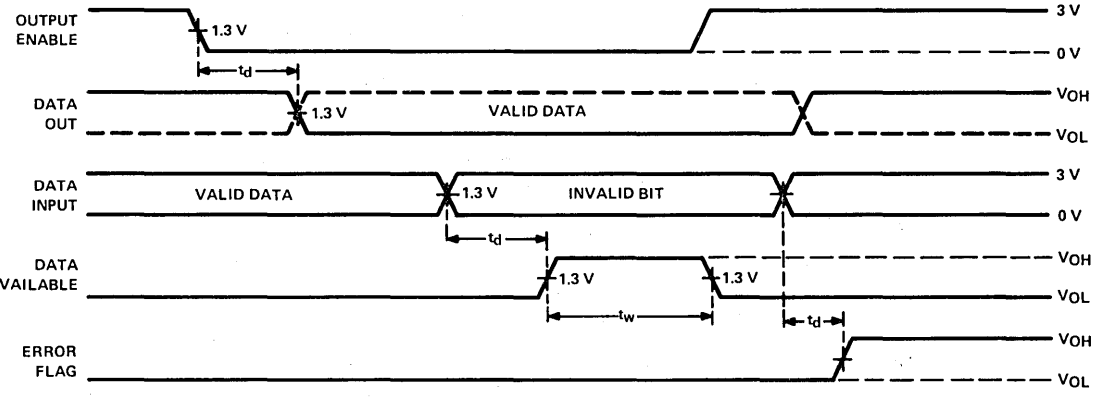
PARAMETER MEASUREMENT INFORMATION



SN74LS462 VOLTAGE WAVEFORMS



SN74LS463 VOLTAGE WAVEFORMS

FIGURE 3 – SWITCHING CHARACTERISTICS

OPERATION

serial data coding and synchronization

frequency-shift coded (FSC) data

Frequency-shift coding, or FSC, is a term for a data transmission code in which each bit period begins with a transition. A space ('0') has no transition during the bit period, however, a mark ('1') has one transition during the bit period (See Figure 4). FSC formatting provides the advantage that it is self-clocking and therefore precludes the necessity of transmitting a clock signal to the receiving end to define the point in time in which data is valid. The SN74LS462 transmitter and SN74LS463 receiver incorporate FSC data to provide a data rate of one megabit per second.

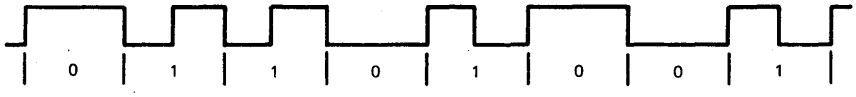


FIGURE 4–FSC SERIAL DATA

continuous-data-stream mode

Continuous-data-stream mode refers to a mode of serial data transmission in which the word boundaries between consecutive transmissions are not defined by any type of synchronization periods. (See Figure 5A). That is, the next consecutive word is transmitted immediately following the previous word. When no further data is to be transmitted, the serial data line goes to a logic high (LED off) state until a new word is to be transmitted. Continuous data stream offers the advantage of a higher data rate than synchronized transmission schemes.

dc-synchronization mode

In the dc-synchronization mode, word boundaries are separated by two bit times at a high logic level (LED off). When no data is to succeed the previous transmission, the serial data line goes to a logic high state until a new word is to be transmitted (See Figure 5B). When new data is to be transmitted after an extended (greater than two bit times) idle period, the current synchronization period will be completed prior to transmission. (i.e., idle periods are always a multiple of two bit time sync periods). Dc synchronization offers the advantage over continuous data stream in that word boundaries are defined by the synchronization period.

ac-synchronization mode

Ac synchronization refers to a three-bit time synchronization period wherein the signal is low for one half of the synchronization period (one and a half bit times) and is high for the other half of the synchronization period. The initial state of the synchronization period is dependent upon the status of the serial data line when the synchronization period is entered. If the serial line is low, the first half of the synchronization period is high and the second half is low. Likewise, if the serial line is high, the first half of the synchronization period is low and the second half is high. When no further data is to succeed the previous transmission, the alternating synchronization period is repeated until the next word is to be transmitted. The current synchronization period will be completed prior to data transmission. (See Figure 5C). Ac synchronization provides the advantage that the receiving end remains in constant synchronization with the transmitting end, even during extended idle periods.

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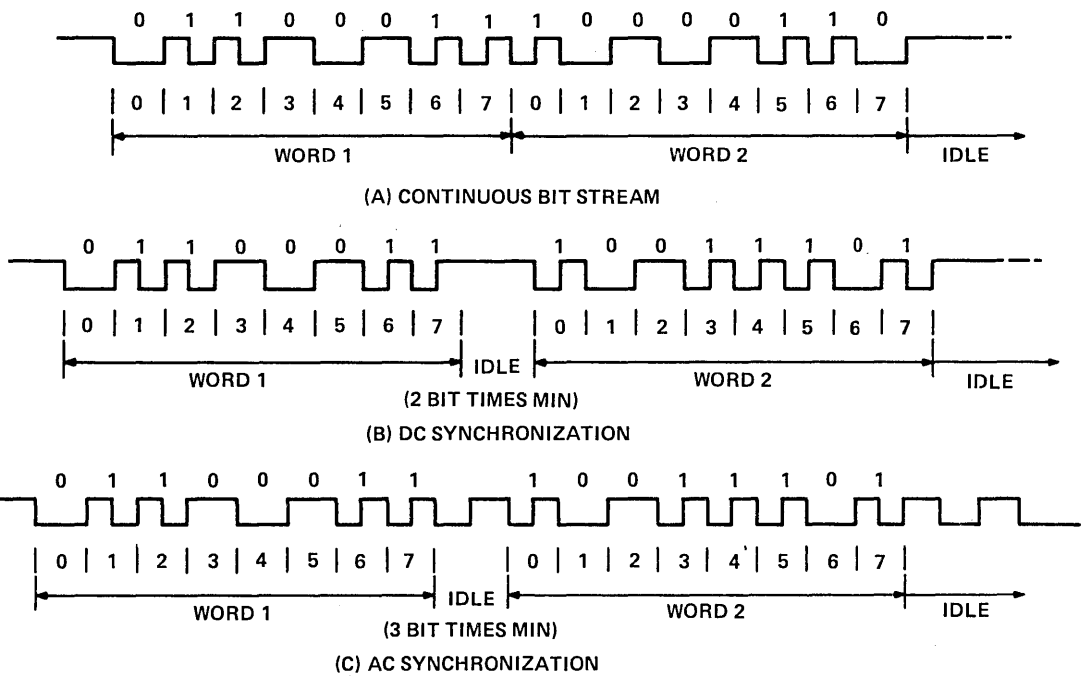

FIGURE 5 – SN74LS462 TRANSMITTER MODES OF OPERATION

SN74LS462 transmitter functional description

SN74LS462 operational description

When power is first applied to the transmitter, power-up circuitry causes the data acknowledge (DA) output to go active (high) indicating that the buffer register is empty and ready to accept data. (See Figure 6). Parallel loading of the data present on the D0-D7 input pins is accomplished by taking the data start (DS) input high when the data acknowledge is high. Loading will then occur on the rising edge of data start. The parallel data loaded into the buffer register appears at the inputs of the shift register. Approximately 250 nanoseconds after the rising edge of data start, data acknowledge (DA) goes inactive (low). Simultaneously, control logic sends out a pulse to the shift register, and the shift register loads the data from the buffer register. After this operation is complete, data acknowledge once again goes active (high) to indicate that the buffer register is ready to accept new data. The new data now present on the D0-D7 data lines will be entered into the buffer register upon the occurance of the next low-to-high transition of data start. The shift register begins shifting data, one bit at a time, into the modulator where it is encoded into FSC format and output on the serial output (SO) pin. After the eighth bit has been transmitted, further operation depends upon the mode of operation selected by the MODE and ac-sync (AC) inputs. (See Table 1). If the continuous-data-stream mode is selected, the next eight bits are loaded into the shift register from the buffer register and shifting of the data continues without interruption. In the dc-sync mode, the two-bit synchronization period will be inserted between consecutive transmissions. In the

OPERATION

ac-sync mode, the three-bit synchronization period will be inserted between consecutive transmissions. (See ac-synchronization mode.) In all modes, the output of the modulator is amplified so that the serial output (SO) is capable of directly driving an external infrared-emitting diode (source).

In all modes, if the buffer and shift registers are empty, data acknowledge will be high and the transmitter will enter the wait mode. In the wait mode, if dc-sync or continuous (bit stream) operation is selected, the SO output will remain high (transmit diode off). In the ac-sync mode, the SO output will repeat the three-bit synchronization period. The wait mode is ended by the rising edge of a data start pulse. When exiting an extended wait period, the transmitter will complete the current synchronization period (two bit times for dc-sync, three bit times for ac-sync) prior to beginning serial output from SO.

The transmitter has a clock input (ϕ) for connection of crystal or TTL-level clock. The bit time is defined as eight cycles of the clock input so that for one-megabit-per-second operation, the clock (ϕ) frequency must be 8 megahertz. The clock output (CKO) may be used to source the SN74LS463 receiver clock input when full-duplex (bidirectional) systems are configured. The two expander outputs, E0 and E1, and the expander input E2 are used to control external devices when the transmitter is configured for 16-bit operation (see Figure 7). However, for 8-bit operation E1 must be tied directly to V_{CC} (+5 volts).

FUNCTION TABLE

INPUTS		SYNC SELECTED
MODE (PIN 14)	AC (PIN 13)	
L	L	Continuous (no sync)
L	H	Undefined
H	L	DC sync
H	H	AC sync

H = high level, L = low level

TABLE 1 – MODE-SELECT FUNCTION TABLE

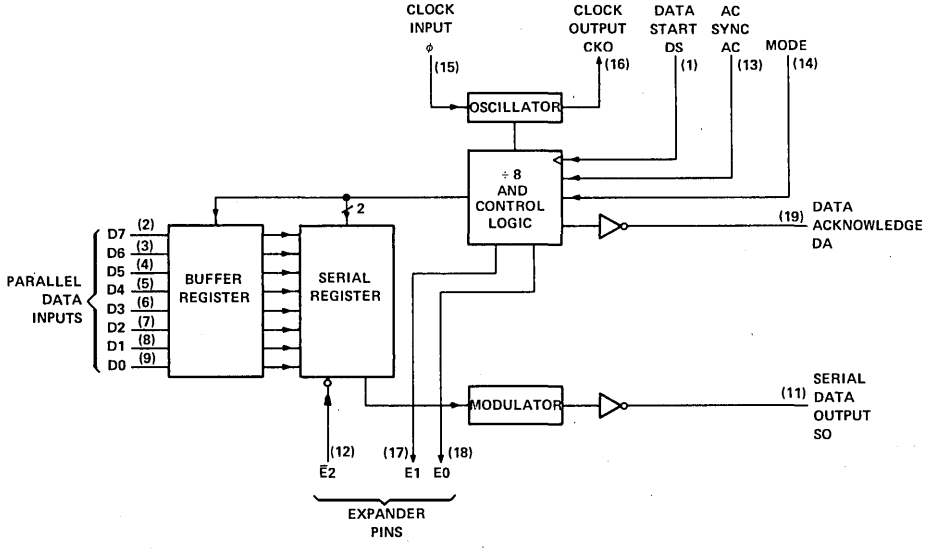

FIGURE 6–SN74LS462 FUNCTIONAL BLOCK DIAGRAM

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SN74LS462 transmitter 16-bit expansion

Sixteen-bit expansion of the transmitter is effected through connection of an SN74LS377 octal D-type flip-flop and an SN74LS165 octal shift register to the expander pins of the transmitter (E0, E1, and E2). (See Figure 7). Addition of these two standard low-power Schottky devices effectively expands the buffer and shift registers of the transmitter to 16 bits. Input E2 is the serial data output of the 'LS165. Outputs E0 and E1 control the shift/load and clock functions, respectively, of the 'LS165. Note that the data start (DS) input is also used to clock data into the 'LS377 external buffer register. Operation in 16-bit mode is identical to 8-bit operation except that the transmitted word length is now 16-bits long.

source interface to SN74LS462 transmitter

The serial output (SO) of the transmitter utilizes extremely large output buffer circuitry to provide 200 milliamperes of low-level sink current. This allows the SN74LS462 transmitter to be interfaced to a wide variety of infrared emitting diode (IRED) source assemblies.

The source assembly is connected in the manner illustrated in Figure 8. Note that for a forward diode current of 100 milliamperes, resistor R is shown to be 32 ohms.

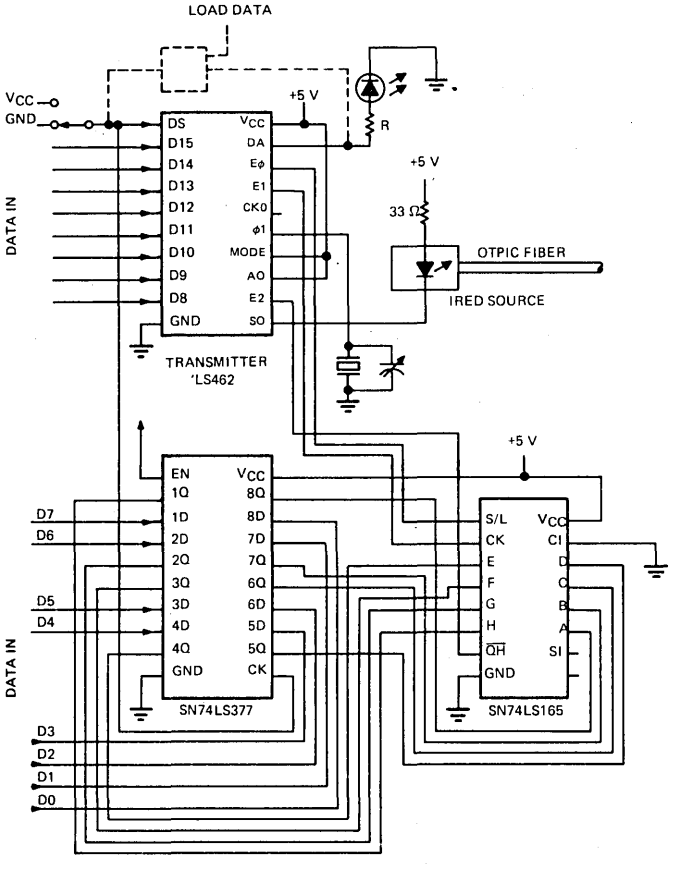

FIGURE 7 – SN74LS462 16-BIT CONFIGURATION

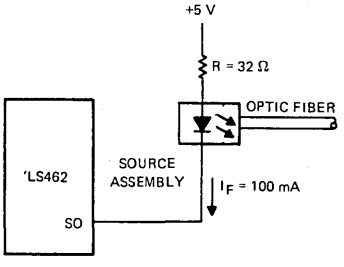

FIGURE 8 – SOURCE ASSEMBLY CONNECTION TO SN74LS462

OPERATION

SN74LS463 receiver functional description

SN74LS463 operation description

The SN74LS463 receiver receives very-low-level currents generated by the external photodiode detector, amplifies this signal, and decodes it into eight (or optionally 16) parallel data outputs. A block diagram of the SN74LS463 is shown in Figure 9.

The SN74LS463 has amplifier/comparator inputs, NONINV and INV, which receive the signal from the photodetector. The clock input (ϕ) provides the synchronization for the circuit. The error flag (EF) output indicates a long-bit error has occurred during the transmission of the eight (or 16) bits of data. The data available output (AV) indicates when the data is available at the output buffer register (D0-D7). The AV output will remain active (high) until the occurrence of an appropriate edge is received by the receiver. For the ac-sync mode, AV will clear typically 800 nanoseconds after it becomes active. For the continuous and dc-sync modes, the time at which AV is cleared inactive (low) is dependent upon the state of the input when the last bit of a bit stream is received. If the bit stream is concluded with a high logic level, the next input transition that clears AV will not occur until the first transition of the first bit of the next eight (or 16) bits to be received. However, if the bit stream is concluded with a low logic level, AV will be cleared when the transition to the high logic level of idle is entered. Because the actual point when AV becomes inactive (low) is dependent upon the subsequent data transmitted system designers are urged to utilize the rising edge of AV to set flags, control logic, etc. in their systems. The output enable ($\overline{OE}$) input either enables the eight parallel three-state outputs or forces them into the high-impedance state. The expander outputs, E0, E1, and E2, are used to expand receiver operation to 16 bits. For eight-bit operation, E1 must be connected to V_{CC}.

The first stage of the SN74LS463 is a low-noise front-end amplifier optimized for use with a PIN detector diode. When the photodiode detects the infrared signal transmitted through the fiber-optic cable, it produces an output current proportional to the received infrared intensity. This current is converted to a voltage by the comparator transimpedance amplifier and amplified to the levels required for internal logic. The FSC information synchronizes with the timer-counter logic in the demodulator where it is demodulated into non-return-to-zero (NRZ) format and fed to a serial shift register. The internal shift register accepts eight-bit serial data and transfers it in parallel to the buffer register. The data outputs from the buffer register are controlled by the output enable ($\overline{OE}$) input; a low at this input enables the outputs, a high forces the outputs to the high-impedance state. If 16-bit operation is selected, serial data will shift out through output E0 to the serial input of an external shift register and data from the external shift register is loaded

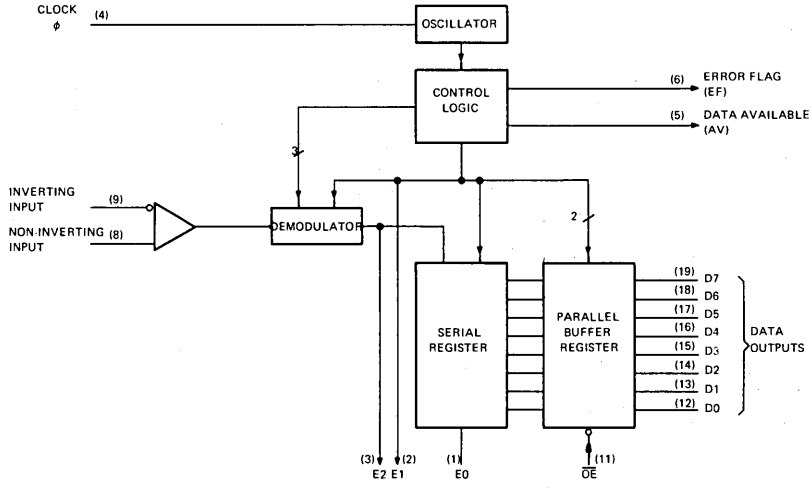

FIGURE 9 – SN74LS463 FUNCTIONAL BLOCK DIAGRAM

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into an external buffer register with a pulse from output E2. A clock signal is supplied to the external shift register through output E1, but for eight-bit operation E1 acts as an input and must be tied to V_{CC}.

The receiver counts eight clock pulses for each data bit. If an FSC transition has not occurred within ten clock periods, the bit will time-out. If less than eight bits (or 16 bits for 16-bit operation) have been received when a time-out error occurs, data available will be inhibited (low) and error flag will go high until eight bits (or 16 bits for 16-bit operation) have been received without a time-out error occurring on any bit. After eight bits (or 16 bits for 16-bit operation) have been received without a time-out error, error flag will go low and data available will operate normally. At the end of each eight bits (or 16 bits), a two-bit or longer synchronization pulse (idle period) may occur. This will be recognized as such by the internal circuitry, and error flag will remain low. If synchronization pulses do not occur after eight bits (or 16 bits for 16-bit operation), the continuous bit-stream mode will be assumed.

SN74LS463 receiver 16-bit expansion

Sixteen-bit expansion of the receiver is effected through connection of an SN74LS164 8-bit serial shift register and an SN74LS374 octal D-type flip-flop to the expander pins of the receiver (E0, E1, and E2). Figure 10 illustrates the connection of these devices to the receiver.

detector interface to the SN74LS463 receiver

The detector assembly is connected to the receiver in the manner illustrated in Figure 11. The PIN detector diode is connected to the NONINV comparator input, and the second diode is a compensating diode connected to the INV comparator input to offset the effects of temperature on the PIN diode characteristics and to establish a PIN "dark" low-level current level.

4

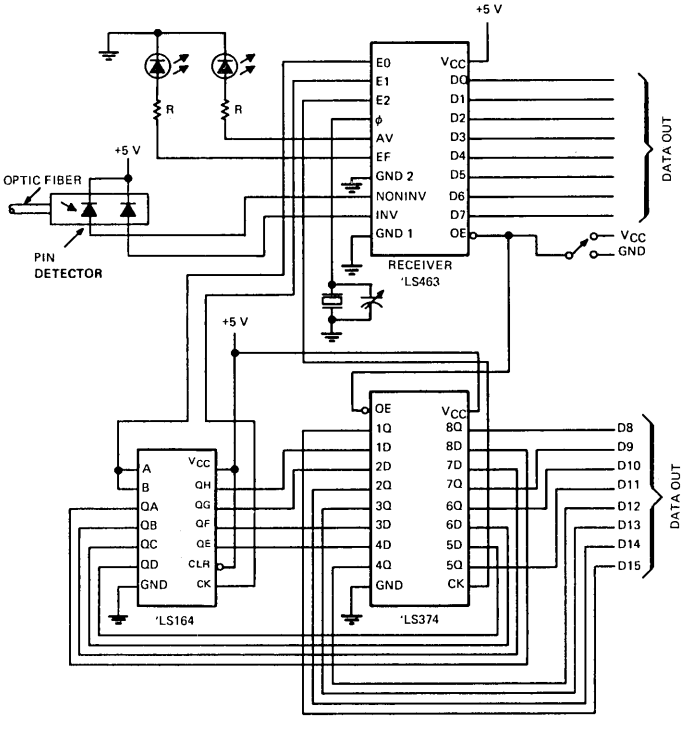

FIGURE 10 – SN74LS463 16-BIT CONFIGURATION

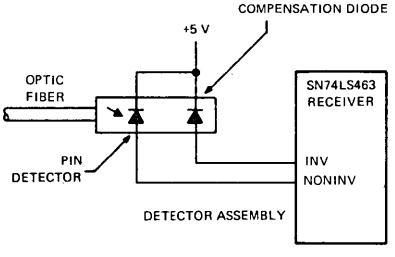

FIGURE 11 – DETECTOR ASSEMBLY CONNECTION TO SN74LS462

OPERATION

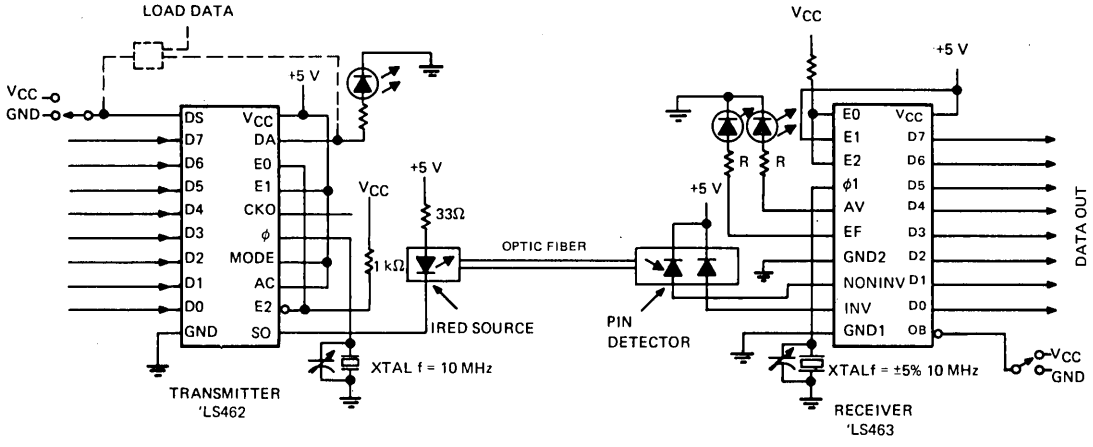

FIGURE 12 – WIRING DIAGRAM 8-BIT AC SYNC MODE

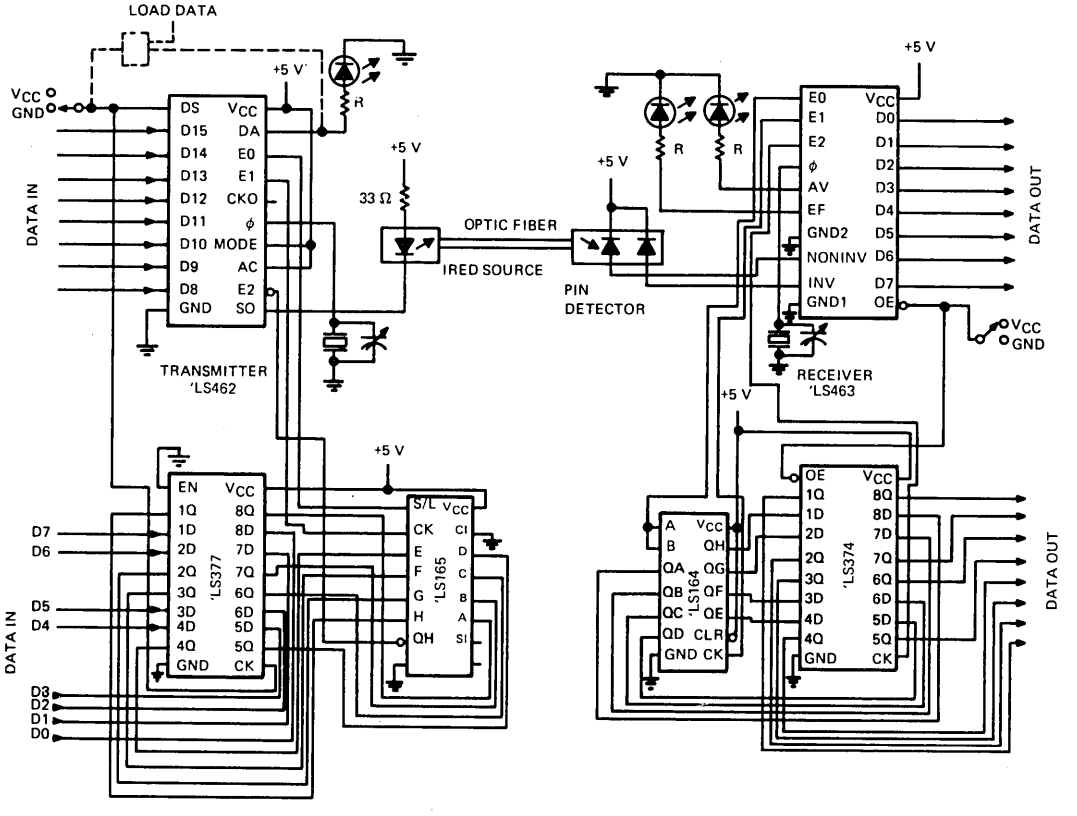

FIGURE 13 – WIRING DIAGRAM 16-BIT AC SYNC MODE

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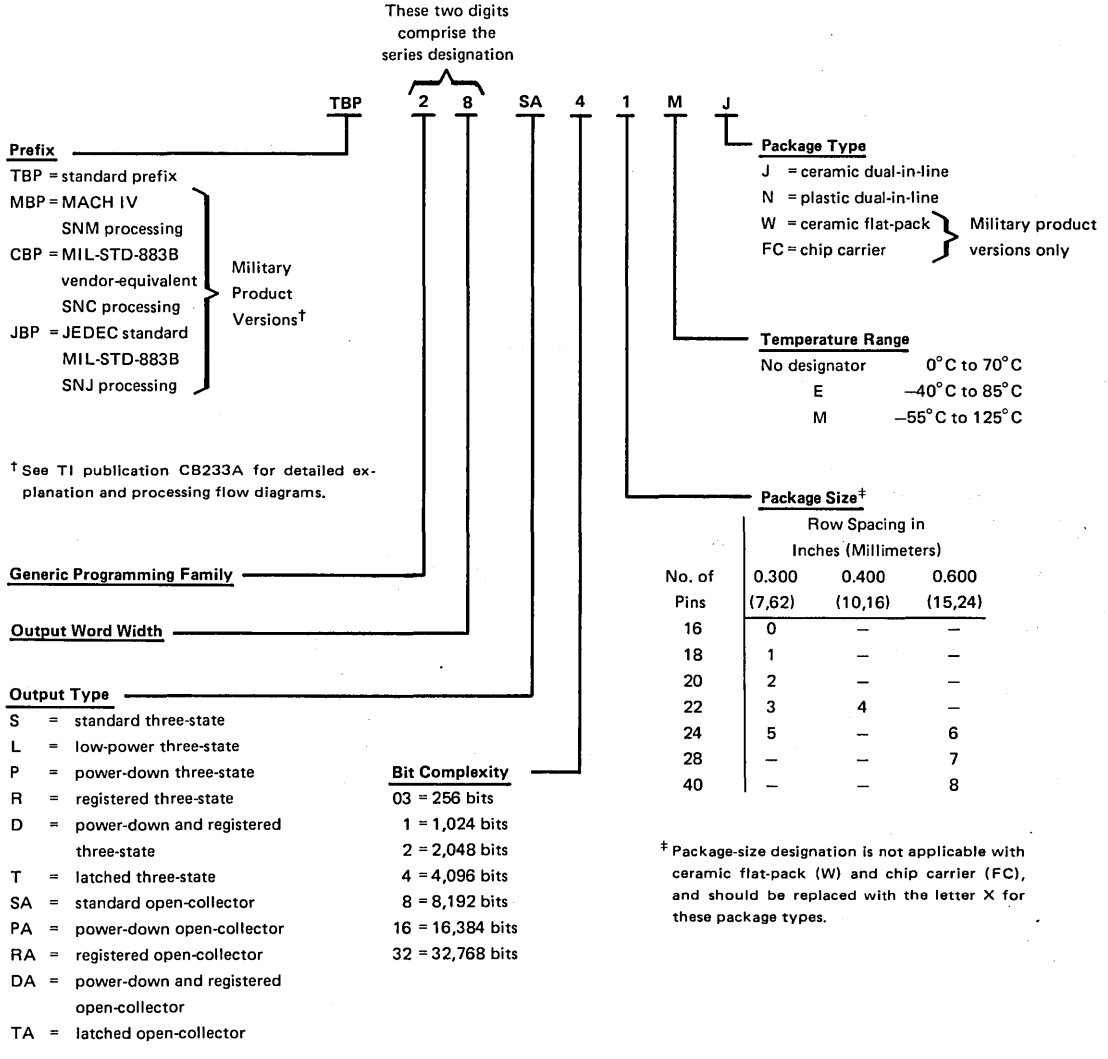
Bipolar Memories

PROM NUMBERING SYSTEM AND ORDERING INSTRUCTIONS

To complement Texas Instruments continually expanding line of bipolar PROMs, a new numbering system is being implemented. This system provides the user with information regarding the generic programming family, bit density, organization, temperature range, and the size and type of package without the necessity of looking up this information in tables. Below is a guide for use of this new numbering system.

Factory orders for PROMs described in this book should include a type number as explained in the following example.



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USER-PROGRAMMABLE READ-ONLY MEMORY (PROM) LINE SUMMARIES

STANDARD PROMS

NEW TYPE NUMBER	OLD TYPE NUMBER	OUTPUT TYPE†	BIT SIZE (ORGANIZATION)	TYPICAL PERFORMANCE		SEE PAGE
				ADDRESS ACCESS TIME	POWER DISSIPATION	
TBP18SA030	SN74S188	◇	256 Bits (32W X 8B)	25 ns	400 mW	5-7
TBP18S030	SN74S288	▽				
TBP14S10	SN74S287	▽	1024 Bits (256W X 4B)	42 ns	500 mW	
TBP14SA10	SN74S387	◇				
TBP24S10		▽		35 ns	375 mW	5-13
TBP24SA10		◇				
TBP18SA22	SN74S470	◇	2048 Bits (256W X 8B)	50 ns	550 mW	5-7
TBP18S22	SN74S471	▽				
TBP18S42	SN74S472	▽	4096 Bits (512W X 8B)	55 ns	600 mW	
TBP18SA42	SN74S473	◇				
TBP18S46	SN74S474	▽				
TBP18SA46	SN74S475	◇				
TBP28S42		▽		35 ns	500 mW	5-13
TBP28S45		▽				
TBP24S41	SN74S476	▽	4096 Bits (1024W X 4B)	40 ns	475 mW	
TBP24SA41	SN74S477	◇				
TBP24S81	SN74S454	▽	8192 Bits (2048W X 4B)	45 ns	625 mW	
TBP24SA81	SN74S455	◇				
TBP28S86	SN74S478	▽	8192 Bits (1024W X 8B)	45 ns	625 mW	
TBP28SA86	SN74S479	◇				
TBP28S2708	SN74S2708	▽				
TBP28S85		▽		35 ns	550 mW	
TBP28S166		▽	16,384 Bits (2048W X 8B)	35 ns	500 mW	

LOW-POWER PROMS

NEW TYPE NUMBER	OLD TYPE NUMBER	OUTPUT TYPE†	BIT SIZE (ORGANIZATION)	TYPICAL PERFORMANCE		SEE PAGE
				ADDRESS ACCESS TIME	POWER DISSIPATION	
TBP28L22		▽	2048 Bits (256W X 8B)	45 ns	300 mW	5-13
TBP28L42		▽	4096 Bits (512W X 8B)	60 ns	250 mW	
TBP28L45		▽				
TBP28L86	SN74LS478	▽	8192 Bits (1024W X 8B)	80 ns	350 mW	
TBP28L85		▽		65 ns	275 mW	
TBP28L166		▽	16,384 Bits (2048W X 8B)	65 ns	250 mW	

† ◇ = open collector, ▽ = three state.

POWER-DOWN PROMS

NEW TYPE NUMBER	OLD TYPE NUMBER	OUTPUT TYPE†	BIT SIZE (ORGANIZATION)	TYPICAL PERFORMANCE		SEE PAGE
				ADDRESS ACCESS TIME	POWER DISSIPATION	
TBP28P42		▽	4096 Bits (512W X 8B)	35 ns	550/60 mW	5-13
TBP28P45		▽				
TBP28P85		▽	8192 Bits (1024W X 8B)	35 ns	550/60 mW	
TBP28P166		▽	16,384 Bits (2048W X 8B)	35 ns	550/75 mW	

REGISTERED PROMS

NEW TYPE NUMBER	OLD TYPE NUMBER	OUTPUT TYPE†	BIT SIZE (ORGANIZATION)	TYPICAL PERFORMANCE		SEE PAGE
				CLOCK TO OUTPUT	POWER DISSIPATION	
TBP28R45		▽	4096 Bits (512W X 8B)	20 ns	550 mW	5-13
TBP28R85		▽	8192 Bits (1024W X 8B)		600 mW	
TBP28R166		▽	16,384 Bits (2048W X 8B)		550 mW	

READ/WRITE MEMORY (RAM) LINE SUMMARY

TYPE NUMBER	BIT SIZE (ORGANIZATION)	OUTPUT CONFIGURATION†	TYPICAL PERFORMANCE		SEE PAGE
			ADDRESS ACCESS TIME	POWER DISSIPATION	
SN54S189/SN74S189	64 Bits (16W X 4B)	▽	25 ns	375 mW	5-29
SN54S289/SN74S289		◇			
SN74S201	256 Bits (256W X 1B)	▽	42 ns	500 mW	5-33
SN74S301		◇	42 ns	500 mW	

FIRST-IN/FIRST-OUT (FIFO) MEMORY WITH 3-STATE OUTPUTS

TYPE NUMBER	BIT SIZE (ORGANIZATION)	TYPICAL PERFORMANCE				SEE PAGE
		DATA RATES		FALL THROUGH	POWER DISSIPATION	
		INPUT	OUTPUT			
SN74S225	80 Bits (16W X 5B)	d-c to 10 MHz	d-c to 10 MHz	190 ns	400 mW	5-37

† ◇ = open collector, ▽ = three state.

BULLETIN NO. DL-S 12727, SEPTEMBER 1979

- Titanium-Tungsten (Ti-W) Fuse Link For Reliable Low-Voltage Full Family Compatible Programming
- Full Decoding And Fast Chip Select Simplify System Design
- P-N-P Inputs For Reduced Loading On System Buffers/Drivers
- Each PROM Supplied With a High Logic Level Stored At Each Bit Location
- Applications Include:
  Microprogramming/Firmware Loaders
  Code Converters/Character Generators
  Translators/Emulators
  Address Mapping/Look-Up Tables

NEW TYPE NUMBER	OLD TYPE NUMBER	BIT SIZE (ORGANIZATION)	OUTPUT CONFIGURATION†	TYPICAL PERFORMANCE	
0°C to 70°C	0°C to 70°C			ADDRESS ACCESS TIME	POWER DISSIPATION
TBP18SA030 (J, N)▲	SN74S188 (J, N)	256 Bits (32W X 8B)	◇	25 ns	400 mW
TBP18S030 (J, N)▲	SN74S288 (J, N)		▽		
TBP14S10 (J, N)▲	SN74S287 (J, N)	1024 Bits (256W X 4B)	▽	42 ns	500 mW
TBP14SA10 (J, N)▲	SN74S387 (J, N)		◇		
TBP18SA22 (J, N)▲	SN74S470 (J, N)	2048 Bits (256W X 8B)	◇	50 ns	550 mW
TBP18S22 (J, N)▲	SN74S471 (J, N)		▽		
TBP18S42 (J, N)▲	SN74S472 (J, N)	4096 Bits (512W X 8B)	▽	55 ns	600 mW
TBP18SA42 (J, N)▲	SN74S473 (J, N)		◇		
TBP18S46 (J, N)▲	SN74S474 (J, N)	4096 Bits (512W X 8B)	▽	55 ns	600 mW
TBP18SA46 (J, N)▲	SN74S475 (J, N)		◇		

▲ For full temperature parts (−55°C to +125°C) use suffix MJ. For devices with MIL-STD 883B processing (−55°C to +125°C) see page 5-2.
† ◇ = open collector, ▽ = three state.

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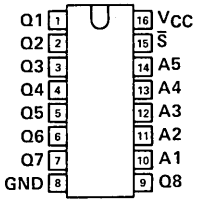
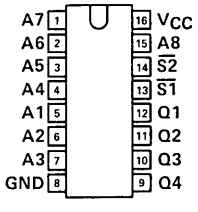
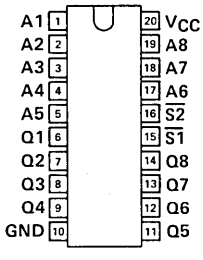
TBP18SA030, TBP18S030
256 BITS
(32 WORDS BY 8 BITS)
(TOP VIEW)



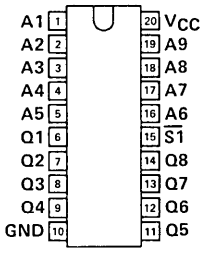
TBP14S10, TBP14SA10
1024 BITS
(256 WORDS BY 4 BITS)
(TOP VIEW)



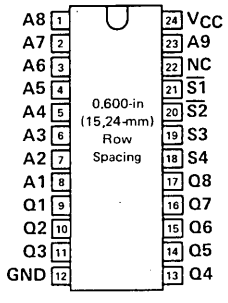
TBP18SA22, TBP18S22
2048 BITS
(256 WORDS BY 8 BITS)
(TOP VIEW)



TBP18S42, TBP18SA22
4096 BITS
(512 WORDS BY 8 BITS)
(TOP VIEW)



TBP18S46, TBP18SA46
4096 BITS
(512 WORDS BY 8 BITS)
(TOP VIEW)



Pin assignments for all of these memories are the same for all packages.

description

These monolithic TTL programmable read-only memories (PROMs) feature titanium-tungsten (Ti-W) fuse links with each link designed to program in 100 microseconds. The Schottky-clamped versions of these PROMs offer considerable flexibility for upgrading existing designs or improving new designs as they feature full Schottky clamping for improved performance, low-current MOS-compatible p-n-p inputs, choice of bus-driving three-state or open-collector outputs, and improved chip-select access times.

The high-complexity 2048- and 4096-bit PROMs can be used to significantly improve system density for fixed memories as all are offered in the 20-pin dual-in-line package having pin-row spacings of 0.300 inch (7,62 mm).

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† Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U.S. Patent Number 3,463,975.

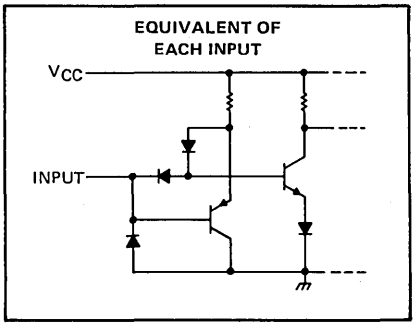
description (continued)

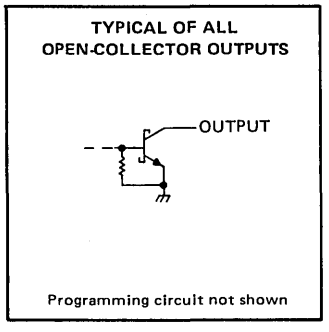
Data can be electronically programmed, as desired, at any bit location in accordance with the programming procedure specified. All PROMs, except the TBP14S10 and TBP14SA10 are supplied with a low-logic-level output condition stored at each bit location. The programming procedure open-circuits Ti-W metal links, which reverses the stored logic level at selected locations. The procedure is irreversible; once altered, the output for that bit location is permanently programmed. Outputs that have never been altered may later be programmed to supply the opposite output level. Operation of the unit within the recommended operating conditions will not alter the memory content.

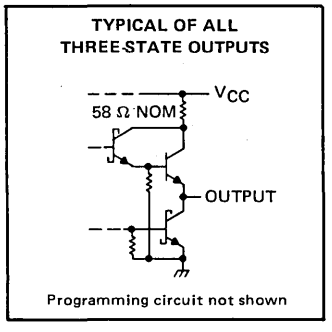
A low level at the chip-select input(s) enables each PROM. The opposite level at any chip-select input causes the outputs to be off.

The three-state output offers the convenience of an open-collector output with the speed of a totem-pole output; it can be bus-connected to other similar outputs yet it retains the fast rise time characteristic of the TTL totem-pole output. The open-collector output offers the capability of direct interface with a data line having a passive pull-up.

schematics of inputs and outputs







absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage (see Note 1) 7V
Input voltage 5.5V
Off-state output voltage 5.5V
Operating free-air temperature range: Full-temperature-range circuits . . . . . −55°C to 125°C
Commercial-temperature-range circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended conditions for programming the TBP18S', TBP18SA', TBP14S', and TBP14SA' PROMs

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC} (see Note 1)	Steady state	4.75	5	5.25	V
	Program pulse	10	10.5	11†	
Input voltage	High level, V_{IH}	2.4		5	V
	Low level, V_{IL}	0		0.5	
Termination of all outputs except the one to be programmed		See load circuit (Figure 1)			
Voltage applied to output to be programmed, $V_{O(pr)}$ (see Note 2)		0	0.25	0.3	V
Duration of V_{CC} programming pulse X (see Figure 2 and Note 3)		98	100	1000	μs
Programming duty cycle for Y pulse			25	35	%
Free-air temperature		0		55	°C

† Absolute maximum ratings.

NOTES: 1. Voltage values are with respect to network ground terminal. The supply voltage rating does not apply during programming.
2. The TBP18S030, TBP18SA030, TBP18SA22, TBP18S22, TBP18S42, TBP18SA42, TBP18S46 and TBP18SA46 are supplied with all bit locations containing a low logic level, and programming a bit changes the output of the bit to high logic level. The TBP14S10, TBP14SA10 are supplied with all bit outputs at a high logic level, and programming a bit changes it to a low logic level.
3. Programming is guaranteed if the pulse applied as 98 μs in duration.

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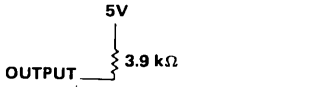
step-by-step programming procedure for the TBP18SA030, TBP18S030, TBP14S10, TBP14SA10, TBP18SA22, TBP18S22, TBP18SA42, TBP18S42, TBP18S46, TBP18SA46

1. Apply steady-state supply voltage (V_{CC} = 5 V) and address the word to be programmed.
2. Verify that the bit location needs to be programmed. If not, proceed to the next bit.
3. If the bit requires programming, disable the outputs by applying a high-logic-level voltage to the chip-select input(s).
4. Only one bit location is programmed at a time. Connect each output not being programmed to 5 V through 3.9 kΩ and apply the voltage specified in the table to the output to be programmed. Maximum current into the programmer output is 150 mA.
5. Step V_{CC} to 10.5 V nominal. Maximum supply current required during programming is 750 mA.
6. Apply a low-logic-level voltage to the chip-select input(s). This should occur between 1 μs and 1 ms after V_{CC} has reached its 10.5-V level. See programming sequence of Figure 2.
7. After the X pulse time is reached, a high logic level is applied to the chip-select inputs to disable the outputs.
8. Within the range of 1 μs to 1 ms after the chip-select input(s) reach a high logic level, V_{CC} should be stepped down to 5 V at which level verification can be accomplished.
9. The chip-select input(s) may be taken to a low logic level (to permit program verification) 1 μs or more after V_{CC} reaches its steady-state value of 5 V.
10. At a Y pulse duty cycle of 35% or less, repeat steps 1 through 8 for each output where it is desired to program a bit.
11. Verify accurate programming of every word after all words have been programmed using V_{CC} values of 4.5 and 5.5 volts.

NOTE: Only one programming attempt per bit is recommended.

5



LOAD CIRCUIT FOR EACH OUTPUT NOT BEING PROGRAMMED OR FOR PROGRAM VERIFICATION

FIGURE 1 – LOAD CIRCUIT

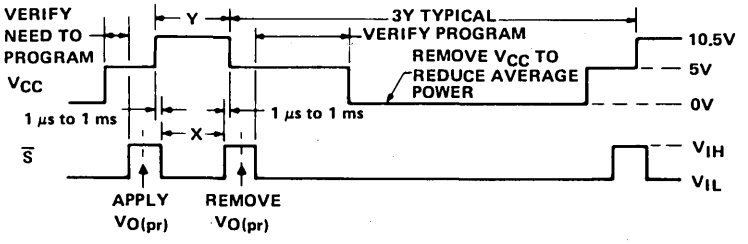


FIGURE 2 – VOLTAGE WAVEFORMS FOR PROGRAMMING

recommended operating conditions

PARAMETER		TBP14S10, TBP18S22			TBP18S030			TBP18S42, TBP18S46			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	MJ	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	J, N	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}	MJ			−2			−2			−2	mA
	J, N			−6.5			−6.5			−6.5	
Low-level output current, I_{OL}				16			20			12	mA
Operating free-air temperature, T_A	MJ	−55		125♦	−55		125	−55		125	°C
	J, N	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		FULL TEMP (MJ)			COMM. TEMP (J, N)			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = MAX	2.4	3.4		2.4	3.2		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = MAX			0.5			0.5	V
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_O = 2.4 V	V_{IH} = 2 V,			50			50	μA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX, V_O = 0.5 V	V_{IH} = 2 V,			−50			−50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V			25			25	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.5 V			−250			−250	μA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−30		−100	−30		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, Chip select(s) at 0 V, Outputs open, See Note 4	TBP14S10		100	135		100	135	mA
			TBP18S030		80	110		80	110	
			TBP18S22		110	155		110	155	
			TBP18S42, TBP18S46		120	155		120	155	

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

TYPE	TEST CONDITIONS	$t_{a(A)}$ (ns) Access time from address			$t_{a(S)}$ (ns) Access time from chip select (enable time)			t_{PXZ} (ns) Disable time from high or low level			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
TBP14S10MJ	C_L = 30 pF for $t_{a(A)}$ and $t_{a(S)}$, 5 pF for t_{PXZ}, R_L = 300 Ω, See Page 1-14		42	75		15	40		12	40	ns
TBP14S10			42	65		15	35		12	35	ns
TBP18S030MJ			25	50		12	30		8	30	ns
TBP18S030			25	40		12	25		8	20	ns
TBP18S22MJ			50	80		20	40		15	35	ns
TBP18S22			50	70		20	35		15	30	ns
TBP18S42MJ, TBP18S46MJ			55	85		20	45		15	40	ns
TBP18S42, TBP18S46			55	75		20	40		15	35	ns

NOTE: MJ designates full-temperature-range circuits (formerly 54 Family), J and N designate commercial-temperature-range circuits (formerly 74 Family).

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

♦ The military product versions of the '14S10 in the W package operating at free-air temperatures above 108°C requires a heat sink that provides a thermal resistance from case-to-free-air, $R_{\theta CA}$, of not more than 42°C/W.

NOTE 4: The typical values of I_{CC} are with all outputs low.

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recommended operating conditions

PARAMETER		TBP14SA10, TBP18SA22			TBP18SA030			TBP18SA42, TBP18SA46			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	MJ	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	J, N	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output voltage, V_{OH}				5.5			5.5			5.5	V
Low-level output current, I_{OL}				16			20			16	mA
Operating free-air temperature, T_A	MJ	−55		125♦	−55		125	−55		125	°C
	J, N	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.2	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	V_{OH} = 2.4 V			50	µA
			V_{OH} = 5.5 V			100	
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = MAX			0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V			25	µA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.5 V			−250	µA
I_{CC}	Supply current	V_{CC} = MAX, Chip select(s) at 0 V, Outputs open, See Note 4	TBP18SA030		80	110	mA
			TBP14SA10		100	135	
			TBP18SA22		110	155	
			TBP18SA42, TBP18SA46		120	155	

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

TYPE	TEST CONDITIONS	$t_{a(A)}$ Access time from address			$t_{a(S)}$ Access time from chip select (enable time)			t_{PLH} Propagation delay time, low-to-high-level output from chip select (disable time)			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
TBP18SA030MJ	C_L = 30 pF, R_{L1} = 300 Ω, R_{L2} = 600 Ω, See Page 1-14		25	50		12	30		12	30	ns
TBP18SA030			25	40		12	25		12	25	ns
TBP14SA10MJ			42	75		15	40		15	40	ns
TBP14SA10			42	65		15	35		15	35	ns
TBP18SA22MJ			50	80		20	40		15	35	ns
TBPSA22			50	70		20	35		15	30	ns
TBP18SA42MJ, TBP18SA46MJ			55	85		20	45		15	40	ns
TBP18SA42, TBP18SA46			55	75		20	40		15	35	ns

NOTE: MJ designates full-temperature-range circuits (formerly 54 Family), J and N designate commercial-temperature-range circuits (formerly 74 Family).

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

♦ The military product versions of the '14SA10 in the W package operating at free-air temperatures above 108°C requires a heat sink that provides a thermal resistance from case-to-free-air, $R_{\theta CA}$, of not more than 42°C/W.

NOTE 4: The typical values of I_{CC} are with all output low.

SERIES 24 AND 28 STANDARD, LOW-POWER, POWER-DOWN, REGISTERED PROGRAMMABLE READ-ONLY MEMORIES

BULLETIN NO. DL-S 12728, SEPTEMBER 1979

- New, Expanded Family of Standard, Low Power, Power Down, And Registered PROMs
- Titanium-Tungsten (Ti-W) Fuse Links for Reliable Low-Voltage Full-Family-Compatible Programming
- Full Decoding And Fast Chip Select Simplify System Design
- P-N-P Inputs for Reduced Loading On System Buffers/Drivers
- Each PROM Supplied With a High Logic Level Stored At Each Bit Location
- Applications Include:
  Microprogramming/Firm Ware Loaders
  Code Converters/Character Generators
  Translators/Emulators
  Address Mapping/Look-Up Tables

STANDARD PROMS

TYPE NUMBER		OUTPUT CONFIGURATION‡	BIT SIZE (ORGANIZATION)	TYPICAL PERFORMANCE		
				ACCESS TIMES		POWER
NEW TYPE NUMBER	OLD TYPE NUMBER			ADDRESS	SELECT	DISSIPATION
TBP24S10 (J, N)†		▽	1024 Bits (256W X 4B)	35 ns	20 ns	375 mW
TBP24SA10 (J, N)†		◇				
TBP28S42 (J, N)†		▽	4096 Bits (512W X 8B)	35 ns	15 ns	500 mW
TBP28S45 (J, N)†		▽				
TBP24S41 (J, N)▲	SN74S476 (J, N)	▽	4096 Bits (1024W X 4B)	40 ns	20 ns	475 mW
TBP24SA41 (J, N)▲	SN74S477 (J, N)	◇				
TBP24S81 (J, N)	SN74S454 (J, N)	▽	8192 Bits (2048W X 4B)	45 ns	20 ns	625 mW
TBP24SA81 (J, N)	SN74S455 (J, N)	◇				
TBP28S86 (J, N)	SN74S478 (J, N)	▽	8192 Bits (1024W X 8B)	45 ns	20 ns	625 mW
TBP28SA86 (J, N)	SN74S479 (J, N)	◇				
TBP28S2708 (J, N)	SN74S2708 (J, N)	▽				
TBP28S85 (J, N)†		▽		35 ns	15 ns	550 mW
TBP28S166 (J, N)†		▽	16,384 Bits (2048W X 8B)	35 ns	15 ns	500 mW

LOW POWER PROMS

TYPE NUMBER		OUTPUT CONFIGURATION‡	BIT SIZE (ORGANIZATION)	TYPICAL PERFORMANCE		
				ACCESS TIMES		POWER
NEW TYPE NUMBER	OLD TYPE NUMBER			ADDRESS	SELECT	DISSIPATION
TBP28L22 (J, N)†		▽	2048 Bits (256W X 8B)	45 ns	35 ns	300 mW
TBP28L42 (J, N)†		▽	4096 Bits (512W X 8B)	60 ns	30 ns	250 mW
TBP28L45 (J, N)†		▽				
TBP28L86 (J, N)▲	SN74LS478 (J, N)	▽	8192 Bits (1024W X 8B)	80 ns	35 ns	350 mW
TBP28L85 (J, N)†		▽		65 ns	30 ns	275 mW
TBP28L166 (J, N)†		▽	16,384 Bits (2048W X 8B)	65 ns	30 ns	250 mW

† NOTE — Electrical parameters for these devices are design goals only.
▲ NOTE — These devices available as full-temperature-range and as high-rel processed devices (use suffix MJ or NJ).
‡ ◇ = open collector, ▽ = three state.

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†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U.S. Patent Number 3,463,975.

SERIES 24 AND 28
STANDARD, LOW-POWER, POWER-DOWN, REGISTERED PROGRAMMABLE READ-ONLY MEMORIES

POWER DOWN PROMS

TYPE NUMBER		OUTPUT CONFIGURATION‡	BIT SIZE (ORGANIZATION)	TYPICAL PERFORMANCE		
				ACCESS TIMES		POWER
NEW TYPE NUMBER	OLD TYPE NUMBER			ADDRESS	SELECT	DISSIPATION
TBP28P42 (J, N)†		▽	4096 Bits (5RW X 8B)	35 ns	35 ns	500/60 mW
TBP28P45 (J, N)†		▽				
TBP28P85 (J, N)†		▽	8291 Bits (1024W X 8B)	35 ns	35 ns	550/60 mW
TBP28P166 (J, N)†		▽	16,384 Bits (2048W X 8B)	35 ns	35 ns	500/75 mW

REGISTERED PROMS

TYPE NUMBER		OUTPUT CONFIGURATION‡	BIT SIZE (ORGANIZATION)	TYPICAL PERFORMANCE		
				CLOCK TO OUTPUT	ADDRESS SET UP TIME	POWER DISSIPATION
NEW TYPE NUMBER	OLD TYPE NUMBER					
TBP 28R45 (J, N)†		▽	4096 Bits (512W X 8B)	20 ns	20 ns	550 mW
TBP28R85 (J, N)†		▽	8192 Bits (1024W X 8B)			600 mW
TBP28R166 (J, N)†		▽	16,384 Bits (2048W X 8B)			550 mW

† Electrical parameters for these devices are design goals only.
‡ ▽ = three state.

description

The new 24 and 28 Series of monolithic TTL programmable read-only memories (PROMs) feature an expanded selection of standard, low-power, power-down, and registered PROMs. This expanded PROM family provides the system designer with considerable flexibility in upgrading existing designs or optimizing new designs. Featuring proven titanium-tungsten (Ti-W) fuse links with low-current MOS-compatible p-n-p inputs, all family members utilize a common programming technique designed to program each link with a 100-microsecond pulse.

The new 4096-bit and 8192-bit PROMs are offered in 24-pin 300-mil-wide packages, greatly improving system density for large PROM arrays. For systems requiring even higher levels of complexity and density, the 16,384-bit PROMs provide twice the bit density of the 8192-bit PROMs in 24-pin 600-mil-wide packages. All PROMs are supplied with a logic-high output level stored at each bit location. The programming procedure open-circuits Ti-W metal links, which reverses the stored logic level at selected locations. The procedure is irreversible; once altered, the output for that bit location is permanently programmed. Outputs that have never been altered may later be programmed to supply the opposite output level. Operation of the unit within the recommended operating conditions will not alter the memory content.

Active level(s) at the chip-select input(s) (S or $\overline{S}$) enables all of the outputs. An inactive level at any chip-select input causes all outputs to be off. On power-down PROMs, active level(s) at the chip-enable input(s) (E or $\overline{E}$) power up the device and enables all of the outputs. An inactive level at any chip-enable input causes all the outputs to be off and the PROM to be in a reduced-power standby mode.

The three-state output offers the convenience of an open-collector output with the speed of a totem-pole output; it can be bus connected to other similar outputs, yet it retains the fast rise time characteristics of the TTL totem-pole output. The open-collector output offers the capability of direct interface with a data line having a passive pull-up.

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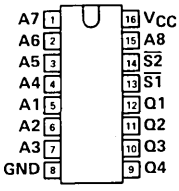
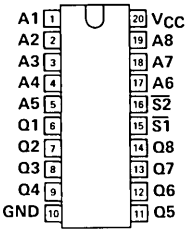
PIN ASSIGNMENTS (TOP VIEWS)

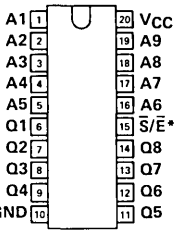
TBP24S10, TBP24SA10
1024 BITS
(256 WORDS BY 4 BITS)



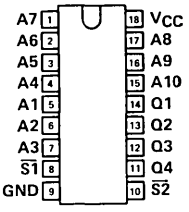
TBP28L22
2048 BITS
(256 WORDS BY 8 BITS)



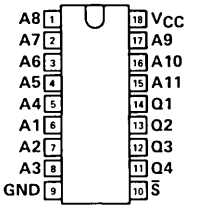
TBP28S42*, TBP28L42,
TBP28P42 4096 BITS
(512 WORDS BY 8 BITS)



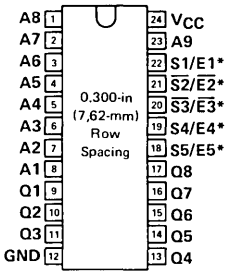
TBP34S41, TBP24SA41
4096 BITS
(1024 WORDS BY 4 BITS)



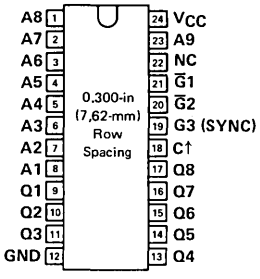
TBP24S81, TBP24SA81
8192 BITS
(2048 WORDS BY 4 BITS)



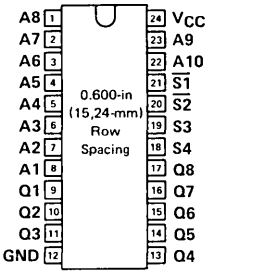
TBP28S45, TBP28L45, TBP28P45*
4096 BITS
(512 WORDS BY 8 BITS)



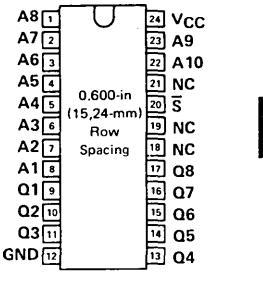
TBP28R45
4096 BITS
(512 WORDS BY 8 BITS)



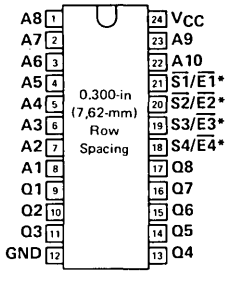
TBP28S86, TBP28SA86, TBP28L86
8192 BITS
(1024 WORDS BY 8 BITS)



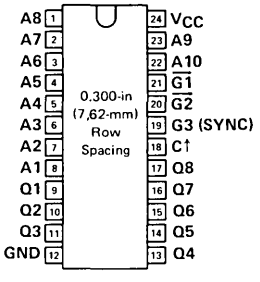
TBP28S2708
8192 BITS
(1024 WORDS BY 8 BITS)



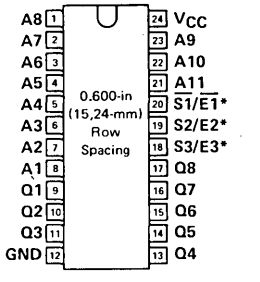
TBP28S85, TBP28L85, TBP28P85*
8192 BITS
(1024 WORDS BY 8 BITS)



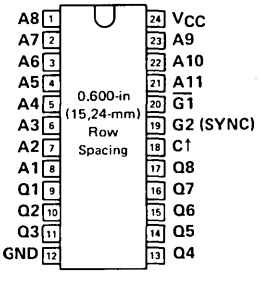
TBP28R85
8192 BITS
(1024 WORDS BY 8 BITS)



TBP28S166, TBP28L166, TBP28P166*
16,384 BITS
(2048 WORDS BY 8 BITS)



TBP28R166
16,384 BITS
(2048 WORDS BY 8 BITS)



NC = No internal connection

* For those pins having dual designations, the designation to the right of the virgule (/) applies only to the type number(s) immediately followed by an asterisk (*) above the pinout drawing.

standard PROMs

The standard PROM members of Series 24 and 28 offer the highest performance for applications requiring the uncompromised speed of Schottky technology. The fast chip-select access times allow additional decoding delays to occur without degrading speed performance.

low-power PROMs

To upgrade systems utilizing MOS EPROMs or MOS PROMs, the low-power PROM family offers the increased output drive and speed performance of bipolar technology and the reduced power dissipation necessary to implement effective upgrades. Additionally, low-power PROMs offer substantially reduced power dissipation over standard PROMs with minimal speed penalty.

power-down PROMs

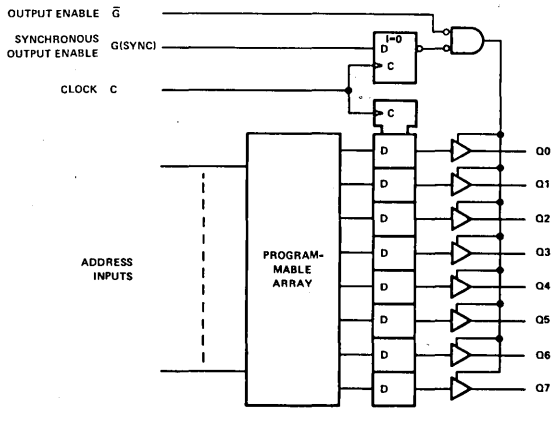
For power-sensitive systems requiring the speed performance of the standard PROM members as well as reduced system power dissipation, the power-down PROM members allow a 75% or better reduction in power dissipation when disabled while providing standard PROM speed performance when enabled. The power-down and power-up functions are sequenced to occur with the outputs at a high-impedance state. The enable (power-up) function provides adequate performance to allow power-up to occur during the normal read access time precluding any degradation in memory speed performance.

registered PROMs

For microprogrammed pipelined systems the Series 24 and 28 registered PROM members offer the system designer reduced package count and improved system performance by incorporating the pipeline register onto the PROM chip. Available in 4096-bit, 8192-bit and 16,384-bit densities, all registered PROMs are provided with synchronous and asynchronous output controls (G and $\overline{G}$) allowing maximum flexibility in data bus control.

When power is first applied, the edge-triggered latch for the synchronous output control is cleared, and the Q outputs are placed in a high-impedance state. To read data, the address is set up, the synchronous output enable, G(SYNC), is taken high, and a low-to-high transition on the clock (C) input causes the selected data to be stored in the registers. That same transition causes the outputs to be enabled if asynchronous output enable $\overline{G}$ is low. At this time the address may be changed and a new word addressed without affecting the register contents. If the synchronous output enable is low at the time of a low-to-high clock transition, the outputs will be disabled to the high-impedance state. They may be disabled at any time by taking output enable G high.

block diagram (positive logic)



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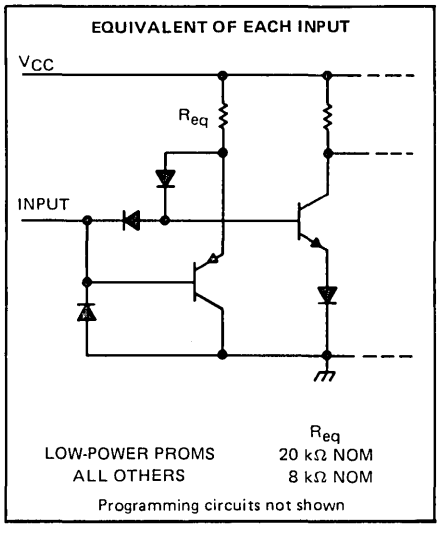
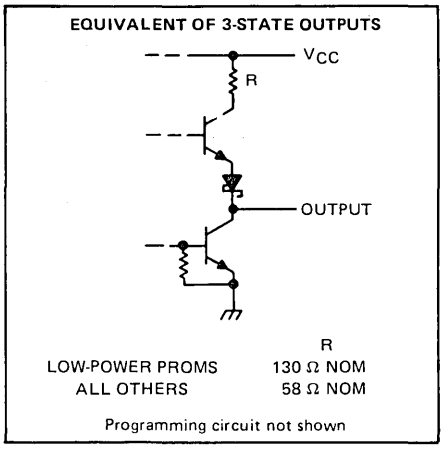
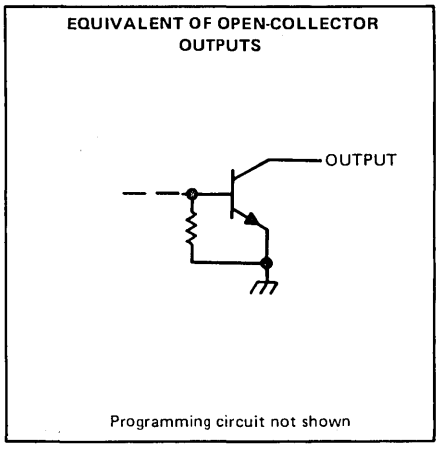
schematics of inputs and outputs







5

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage (see Note 1)	7 V
Input voltage	5.5 V
Chip-select peak input voltage (S, S1, S2) (see Note 2)	11 V
Off-state output voltage	5.5 V
Off-state peak output voltage (see Note 2)	17.25 V
Operating free-air temperature range: Full-temperature-range circuits (MJ)	−55°C to 125°C
Commercial-temperature-range circuits (J, N)	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. These ratings apply only under the conditions described in the programming procedure.

recommended operating conditions

PARAMETER		TBP28SA86			TBP24SA81, TBP24SA41			TBP24SA10*			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	MJ	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	J, N	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output voltage, V_{OH}				5.5			5.5			5.5	V
Low-level output current, I_{OL}	MJ			12			16			16	mA
	J, N			12			16			16	
Operating free-air temperature range	MJ	−55		125	−55		125	−55		125	°C
	J, N	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TBP24SA81 TBP28SA86			TBP24SA41			TBP24SA10*			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.2			−1.2			−1.2	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	V_O = 2.4 V			50			50			50	μA
			V_O = 5.5 V			100			100			100	
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = MAX	MJ			0.5			0.5			0.5	V
			J, N			0.5			0.5			0.45	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				25			25			25	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V				−250			−250			−250	μA
I_{CC}	Supply current	V_{CC} = MAX	MJ		125			95	140		75		mA
			J, N		125	175		95	140		75		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

TYPE		TEST CONDITIONS	$t_{a(A)}$ Access time from address			$t_{a(S)}$ Access time from chip select (enable time)			t_{PLH} Propagation delay time, low-to-high-level output from chip select			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TBP24SA10*	MJ	C_L = 30 pF, See Page 1-14		35			20	40		15	40	ns
	J, N			35			20	30		15	30	
TBP24SA81				45	70		20	40		20	40	ns
TBP24SA41	MJ			40	75		20	40		20	40	ns
	J, N			40	60		20	30		20	30	
TBP24SA86				45	70		20	40		20	40	ns

* Electrical parameters for these devices are design goals only.
NOTE: MJ designates full-temperature-range circuits (formerly 54 Family), J and N designate commercial-temperature-range circuits (formerly 74 Family).

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recommended operating conditions

PARAMETER		TBP24S10*			TBP28S86, TBP28S2708			TBP24S81, TBP24S41			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	MJ	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	J, N	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}	MJ			−2			−2			−2	mA
	J, N			−3.2			−3.2			−3.2	
Low-level output current, I_{OL}	MJ			16			12			16	mA
	J, N			16			12			16	
Operating free-air temperature range	MJ	−55		125	−55		125	−55		125	°C
	J, N	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TBP24S10*			TBP24S81, TBP24S86, TBP28S2708			TBP24S41			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.2			−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = MAX		2.4	3.1		2.4	3.1		2.4	3.1		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = MAX				0.5			0.5			0.5	V
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_O = 2.4 V				50			50			50	μA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_O = 0.5 V				−50			−50			−50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				25			25			25	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V				−250			−250			−250	μA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	MJ	−15		−100	−15		−100	−15		−100	mA
			J, N	−20		−100	−20		−100	−20		−100	
I_{CC}	Supply current	V_{CC} = MAX	MJ					125	175		95	140	mA
			J, N		75			125	175		95	140	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

TYPE		TEST CONDITIONS		$t_{a(A)}$ Access time from address			$t_{a(S)}$ Access time from chip select (enable time)			t_{PXZ} Disable time			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TBP24S10*	MJ	C_L = 30 pF for $t_{a(A)}$ and $t_{a(S)}$, C_L = 5 pF for t_{PXZ}	R_L = 300 Ω, See Page 1-14		35			20	35		15	35	ns
	J, N				35			20	40		15	30	ns
TBP24S81					45	70		20	40		20	40	ns
TBP24S41	MJ				40	75		20	40		20	40	ns
	J, N				40	60		20	30		20	30	ns
TBP28S86					45	70		20	40		20	40	ns
TBP28S2708													

* Electrical parameters for these devices are design goals only.

NOTE: MJ designates full-temperature-range circuits (formerly 54 Family), J and N designate commercial-temperature-range circuits (formerly 74 Family).

recommended operating conditions

PARAMETER		TBP28S42*, TBP28S45*			TBP28S85*			TBP28S166*			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	MJ	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	J, N	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}	MJ			−2			−2			−2	mA
	J, N			−3.2			−3.2			−3.2	
Low-level output current, I_{OL}	MJ			16			16			16	mA
	J, N			16			16			16	
Operating free-air temperature range	MJ	−55		125	−55		125	−55		125	°C
	J, N	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TBP28S42*, TBP28S45*			TBP28S85*			TBP28S166*			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.2			−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = MAX		2.4	3.1		2.4	3.1		2.4	3.1		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = MAX				0.5			0.5			0.5	V
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_O = 2.4 V				50			50			50	μA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_O = 0.5 V				−50			−50			−50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				25			25			25	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V				−250			−250			−250	μA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	MJ	−15		−100	−15		−100	−15		−100	mA
			J, N	−20		−100	−20		−100	−20		−100	
I_{CC}	Supply current	V_{CC} = MAX	MJ		105			110			100		mA
			J, N		105			110			100		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

TYPE	TEST CONDITIONS		$t_{a(A)}$ Access time from address			$t_{a(S)}$ Access time from chip select (enable time)			t_{PXZ} Disable time			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TBP28S42* TBP28S45*	C_L = 30 pF for $t_{a(A)}$ and $t_{a(S)}$, C_L = 5 pF for t_{PXZ}	R_L = 300 Ω, See Page 1-14		35			15			12		ns
TBP28S85*				35			15			12		ns
TBP28S166*				35			15			12		ns

*Electrical parameters for these devices are design goals only.

NOTE: MJ designates full-temperature-range circuits (formerly 54 Family), J and N designate commercial-temperature-range circuits (formerly 74 Family).

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recommended operating conditions

PARAMETER		TBP28L22*			TBP28L42*, TBP28L45*			TBP28L86			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	MJ	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	J, N	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}	MJ			−1			−1			−1	mA
	J, N			−1.6			−1.6			−1.6	
Low-level output current, I_{OL}	MJ			8			8			4	mA
	J, N			8			8			8	
Operating free-air temperature range	MJ	−55		125	−55		125	−55		125	°C
	J, N	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TBP28L22*			TBP28L42* TBP28L42*			TBP28L86			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.2			−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = MAX		2.4	3.1		2.4	3.1		2.4	3.1		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = MAX				0.5			0.5			0.5	V
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_O = 2.4 V				50			50			50	μA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_O = 0.5 V				−50			−50			−50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				25			25			25	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V				−250			−250			−250	μA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	MJ	−10		−100	−10		−100	−10		−100	mA
			J, N	−10		−100	−10		−100	−10		−100	
I_{CC}	Supply current	V_{CC} = MAX	MJ								60	100	mA
			J, N		60	85		50			60	100	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

TYPE		TEST CONDITIONS		$t_{a(A)}$ Access time from address			$t_{a(S)}$ Access time from chip select (enable time)			t_{PXZ} Disable time			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TBP28L22*	MJ	C_L = 30 pF for $t_{a(A)}$ and $t_{a(S)}$, C_L = 5 pF for t_{PXZ}	R_L = 600 Ω, See Page 1-15		45			20			15		ns
	J, N				45			20			15		ns
TBP28L42* TBP28L45*					60			30			25		ns
TBP28L86	MJ				85	175		55	135		50	90	ns
	J, N				85	130		55	90		50	75	

* Electrical parameters for these devices are design goals only.
NOTE: MJ designates full-temperature-range circuits (formerly 54 Family), J and N designate commercial-temperature-range circuits (formerly 74 Family).

recommended operating conditions

PARAMETER		TBP28L85*			TBP28L166*			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	MJ	4.5	5	5.5	4.5	5	5.5	V
	J, N	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}	MJ			−1			−1	mA
	J, N			−1.6			−1.2	
Low-level output current, I_{OL}	MJ			8			8	mA
	J, N			8			8	
Operating free-air temperature range	MJ	−55		125	−55		125	°C
	J, N	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TBP28L85*			TBP28L166*			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = MAX		2.4	3.1		2.4	3.1		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = MAX				0.5			0.5	V
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_O = 2.4 V				50			50	μA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_O = 0.5 V				−50			−50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				25			25	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V				−250			−250	μA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	MJ	−10		−100	−10		−100	mA
			J, N	−10		−100	−10		−100	
I_{CC}	Supply current	V_{CC} = MAX	MJ		55			50		mA
			J, N		55			50		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

TYPE	TEST CONDITIONS		$t_{a(A)}$ Access time from address			$t_{a(S)}$ Access time from chip select (enable time)			t_{PXZ} Disable time			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TBP28L85*	C_L = 30 pF for $t_{a(A)}$ and $t_{a(S)}$, C_L = 5 pF for t_{PXZ}	R_L = 600 Ω, See Page 1-15		65			30			25		ns
TBP28L166*				65			30			25		ns

* Electrical parameters for these devices are design goals only.
NOTE: MJ designates full-temperature-range circuits (formerly 54 Family), J and N designate commercial-temperature-range circuits (formerly 74 Family).

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recommended operating conditions

PARAMETER		TBP28P42*, TBP28P45*			TBP28P85*			TBP28P166*			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	MJ	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	J, N	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}	MJ			−2			−2			−2	mA
	J, N			−3.2			−3.2			−3.2	
Low-level output current, I_{OL}	MJ			16			16			16	mA
	J, N			16			16			16	
Operating free-air temperature range	MJ	−55		125	−55		125	−55		125	°C
	J, N	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TBP28P42*, TBP28P45*			TBP28P85*			TBP28P166*			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.2			−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = MAX		2.4	3.1		2.4	3.1		2.4	3.1		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = MAX				0.5			0.5			0.5	V
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_O = 2.4 V				50			50			50	μA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_O = 0.5 V				−50			−50			−50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				25			25			25	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V				−250			−250			−250	μA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	MJ	−15		−100	−15		−100	−15		−100	mA
			J, N	−20		−100	−20		−100	−20		−100	
I_{CC}	Supply current, Power Up	V_{CC} = MAX			100			110			100		mA
	Supply current, Power Down				12			12			15		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

TYPE	TEST CONDITIONS		$t_{a(A)}$ Access time from address			$t_{a(E)}$ Access time from chip enable (enable time)			t_{PXZ} Disable time			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TBP28P42* TBP28P45*	C_L = 30 pF for $t_{a(A)}$ and $t_{a(E)}$, C_L = 5 pF for t_{PXZ}	R_L = 300 Ω, See Page 1-14		35			35			12		ns
TBP28P85*				35			35			12		ns
TBP28P166*				35			35			12		ns

*Electrical parameters for these devices are design goals only.

NOTE: MJ designates full-temperature-range circuits (formerly 54 Family), J and N designate commercial-temperature-range circuits (formerly 74 Family).

recommended operating conditions

PARAMETER		TBP28R45*			TBP28R85*			TBP28R166*			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	MJ	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	J, N	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}	MJ			−2			−2			−2	mA
	J, N			−3.2			−3.2			−3.2	
Low-level output current, I_{OL}	MJ			16			16			16	mA
	J, N			16			16			16	
Clock pulse width high, $t_{w(CH)}$		20			20			20			ns
Clock pulse width low, $t_{w(CL)}$		20			20			20			ns
Address setup time, $t_{su(A)}$		20			20			20			ns
Chip select setup time, $t_{su(S)}$		0			0			0			ns
Address hold time, $t_{h(A)}$		0			0			0			ns
Chip select hold time, $t_{h(S)}$		5			5			5			ns
Operating free-air temperature range	MJ	−55		125	−55		125	−55		125	°C
	J, N	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TBP28R45*			TBP28R85*			TBP28R166*			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.2			−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = MAX		2.4	3.1		2.4	3.1		2.4	3.1		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = MAX	MJ			0.5			0.5			0.5	V
			J, N			0.5			0.5			0.5	
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_O = 2.4 V				50			50			50	μA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_O = 0.5 V				−50			−50			−50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				25			25			25	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V				−250			−250			−250	μA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	MJ	−15		−100	−15		−100	−15		−100	mA
			J, N	−20		−100	−20		−100	−20		−100	
I_{CC}	Supply current	V_{CC} = MAX	MJ		110			120			110		mA
			J, N		110			120			110		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.
* Electrical and switching parameters for these devices are design goals only.
NOTE: MJ designates full-temperature-range circuits (formerly 54 Family), J and N designate commercial-temperature-range circuits (formerly 74 Family).

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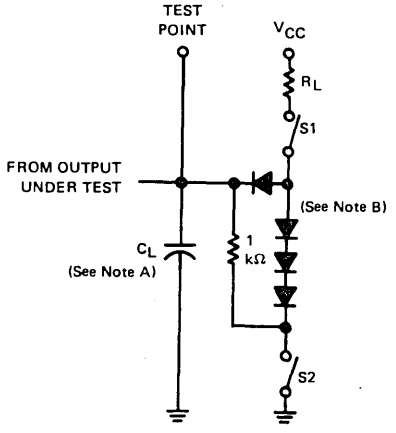
switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

types TBP28R45*, TBP28R85*, TBP28R166*

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{a(C)}$	Access time from clock	R_L = 300 Ω, C_L = 30 pF, See Figure 1		20		ns
$t_{PXZ(C)}$	Output disable time from clock			20		ns
$t_{PZX(C)}$	Output enable time from clock			20		ns
$t_{PXZ(G)}$	Output disable time from $\overline{G}$			12		ns
$t_{PZX(G)}$	Output enable time from $\overline{G}$			15		ns

* Electrical and switching parameters for these devices are design goals only.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N916 or 1N3064.

LOAD CIRCUIT

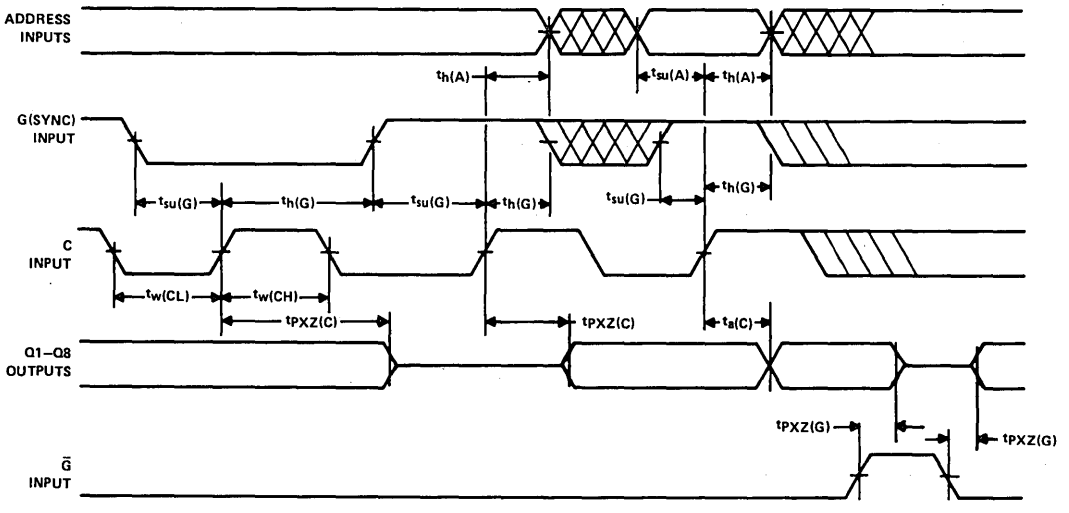


FIGURE 1 – SWITCHING WAVEFORMS FOR TYPES TBP28R45, TBP28R85, AND TBP28R166

5

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recommended conditions for programming

PARAMETER		MIN	TYP	MAX	UNIT
Steady-state supply voltage, V_{CC}		4.5	5	5.5	V
Address input voltage	V_{IH}	2.4		5	V
	V_{IL}	0		0.5	
E3 and E4 input voltage (where appropriate)	V_{IH}	2.4		5	V
Voltage at all outputs except the one to be programmed		0		0.5	V
Supply voltage programming pulse (see Figure 2)	Voltage, $V_{CC(pr)}$	5.75	6	6.25	V
	Pulse width, t_w	1000		2000	μs
	Duty cycle		25	35	%
Select or enable programming pulse (see Figure 2)	Voltage, $V_{S(pr)}$	9.75	10	11	V
	V_{IL}				
Output programming pulse (see Figure 2)	Voltage, $V_{O(pr)}$	16.75	17	17.25	V
	Rise time, t_r	10		50	μs
	Pulse width, t_w	98	100	1000	μs
	V_{IL}	0		0.5	
Registered PROM verify clock pulse width	$t_{w(CH)}$		20		ns
Free-air temperature, T_A		0		55	°C

step-by-step programming instructions (see Figure 2)

1. Address the word to be programmed, apply 5V ± 10% to V_{CC} and active levels to all chip select (S and $\overline{S}$) or chip enable (E and $\overline{E}$) inputs.
2. Verify the status of a bit location by checking the output level. For registered PROMs a clock must be applied to the clock pin to verify the output level.
3. Increase V_{CC} to $V_{CC(pr)}$ with a minimum current capability of 200 milliamperes.
4. Apply $V_{S(pr)}$ to all the $\overline{S}$, $\overline{E}$ or $\overline{G}$ inputs. $I_I \leqslant 15$ mA.
5. Connect all outputs, except the one to be programmed, to a logic low level ($0 \leqslant V_{IL} \leqslant 0.5$ V). Only one bit is programmed at a time.
6. Apply the output programming pulse for at least 98 microseconds. Minimum current capability of the programming supply should be 200 milliamperes.
7. After terminating the output pulse, disconnect all outputs from V_{IL} conditions.
8. Reduce the voltage at $\overline{S}$, $\overline{E}$ or $\overline{G}$ inputs to V_{IL}.
9. Reduce V_{CC} to steady-state voltage and verify output status. Note that for registered PROMs, a clock must be applied to the clock input pin to verify output status.
10. Repeat steps 3 through 9 for each bit location that requires programming.
11. Verify accurate programming of every word after all words have been programmed using V_{CC} values of 4.5 and 5.5 volts. Note that registered PROMs must be clocked to verify the output condition.

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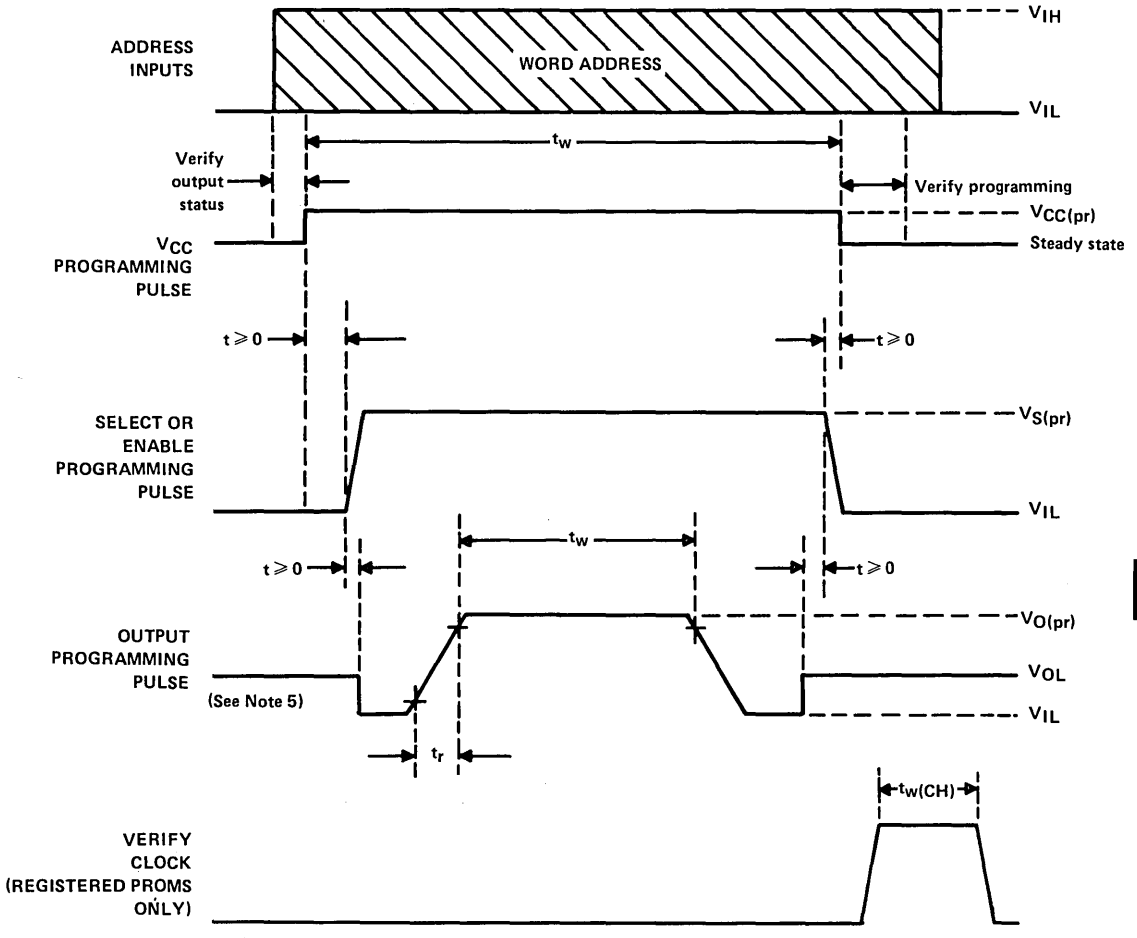


FIGURE 2 – TIMING DIAGRAM AND VOLTAGE WAVEFORMS FOR PROGRAMMING SEQUENCE

NOTE: The output to be programmed may be forced to zero volts after the transition to $V_{O(pr)}$ at the E input has begun.

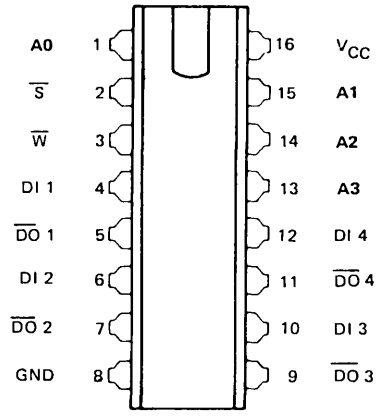
TYPES SN54S189A, SN54S289A, SN74S189A, SN74S289A 64-BIT HIGH-PERFORMANCE RANDOM-ACCESS MEMORIES

SEPTEMBER 1976—REVISED JUNE 1979

STATIC RANDOM-ACCESS MEMORIES

- Fully Decoded RAM's Organized as 16 Words of Four Bits Each
- Schottky-Clamped for High Speed:
  - Read Cycle Time . . . 25 ns Typical
  - Write Cycle Time . . . 25 ns Typical
- Choice of Three-State or Open-Collector Outputs
- Compatible with Most TTL and I^2L Circuits
- Chip-Select Input Simplifies External Decoding

SN54S189A, SN54S289A . . . . J OR W PACKAGE
SN74S189A, SN74S289A . . . . J OR N PACKAGE
(TOP VIEW)



Pin assignments are same for all packages.

description

These 64-bit active-element memories are monolithic Schottky-clamped transistor-transistor logic (TTL) arrays organized as 16 words of four bits each. They are fully decoded and feature a chip-select input to simplify decoding required to achieve expanded system organization. The memories feature p-n-p input transistors that reduce the low-level input current requirement to a maximum of −0.25 milliamperes, only one-eighth that of a Series 54S/74S standard load factor. The chip-select circuitry is implemented with minimal delay times to compensate for added system decoding.

5

write cycle

The information applied at the data input is written into the selected location when the chip-select input and the write-enable input are low. While the write-enable input is low, the 'S189A output is in the high-impedance state and the 'S289A output is off. When a number of outputs are bus-connected, this high-impedance or off state will neither load nor drive the bus line, but it will allow the bus line to be driven by another active output or a passive pull-up.

read cycle

The stored information (complement of information applied at the data input during the write cycle) is available at the output when the write-enable input is high and the chip-select input is low. When the chip-select input is high, the 'S189A output will be in the high-impedance state and the 'S289A output will be off.

FUNCTION TABLE

FUNCTION	INPUTS		'S189A OUTPUT	'S289A OUTPUT
	CHIP SELECT	WRITE ENABLE		
Write	L	L	High Impedance	Off
Read	L	H	Complement of Data Entered	Complement of Data Entered
Inhibit	H	X	High Impedance	Off

H = high level, L = low level, X = irrelevant

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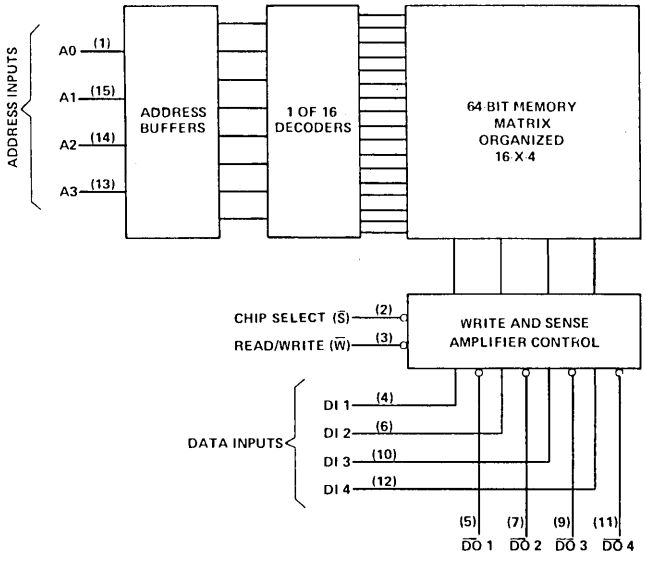
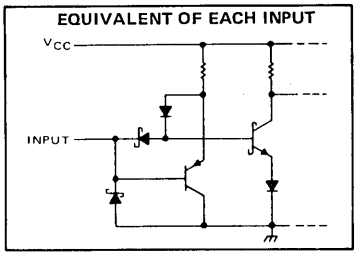
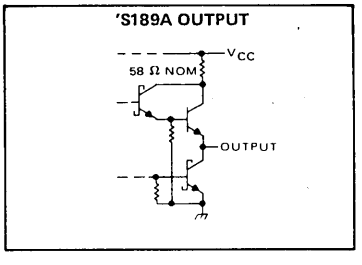
†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U. S. Patent Number 3,463,975.

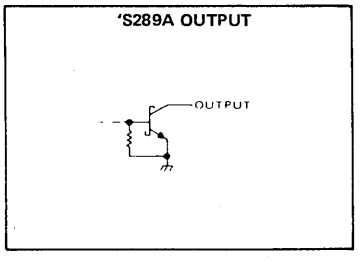
functional block diagram



schematics of inputs and outputs







absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Off-State output voltage	5.5 V
Operating free-air temperature range: SN54S' Circuits	−55°C to 125°C
SN74S' Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

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recommended operating conditions

		SN54S189A			SN74S189A			SN74S289A			SN54S289A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	4.75	5	5.25	4.75	5	5.25	V
High-level output voltage, V_{OH}							5.5						5.5	V
High-level output current, I_{OH}				−2						−6.5				mA
Low-level output current, I_{OL}				16			16			16			16	mA
Width of write pulse (write enable low), $t_{w(wr)}$		25			25			25			25			ns
Setup time	Address before write pulse, $t_{su(da)}$	0↓			0↓			0↓			0↓			ns
	Data before end of write pulse, $t_{su(da)}$	25↑			25↑			25↑			25↑			
	Chip-select before end of write pulse, $t_{su(\overline{S})}$	25↑			25↑			25↑			25↑			
Hold time	Address after write pulse, $t_{h(ad)}$	3↑			3↑			0↑			0↑			ns
	Data after write pulse, $t_{h(da)}$	0↑			0↑			0↑			0↑			
	Chip-select after write pulse, $t_{h(\overline{S})}$	0↑			0↑			0↑			0↑			
Operating free-air temperature, T_A		−55		125	−55		125	0		70	0		70	°C

↑↓The arrow indicates the transition of the write-enable input used for reference: ↑ for the low-to-high transition, ↓ for the high-to-low transition.

electrical characteristics over recommended operating free-air temperature range (otherwise noted)

PARAMETER		TEST CONDITIONS†			'S189A			'S289A			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18mA					−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = MAX		SN54S'	2.4	3.4					V
				SN74S'	2.4	3.2					
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V		V_O=2.4 V						40	μA
				V_O=5.5 V						100	
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		SN54S'		0.35	0.5		0.35	0.5	V
				SN74S'		0.35	0.45		0.35	0.45	
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = 0.8 V, V_{OH} = 2.4 V					50				μA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = 0.8 V, V_{OL} = 0.4 V					−50				μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V					1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V					25			25	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V					−250			−250	μA
I_{OS}	Short-circuit output current§	V_{CC} = MAX			−30		−100				mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2				75	110		75	105	mA

† For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Duration of the short circuit should not exceed one second.

NOTE 2: I_{CC} is measured with the read/write and chip-select inputs grounded. All other inputs at 4.5V, and the outputs open.

'S189A switching characteristics over recommended operating ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER			TEST CONDITIONS	SN54S189A		SN74S189A		UNIT
				TYP‡	MAX	TYP‡	MAX	
$t_{a(ad)}$	Access time from address		C_L = 30 pF, R_L = 300 Ω See Note 3	25	50	25	35	ns
$t_{a(S)}$	Access time from chip select (enable time)			18	25	18	22	ns
t_{SR}	Sense recovery time			22	40	22	35	ns
t_{PXZ}	Disable time from high or low level	from $\overline{S}$	C_L = 5 pF, R_L = 300 Ω, See Note 3	12	25	12	17	ns
		from $\overline{W}$		12	30	12	25	

'S289A switching characteristics over recommended operating ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER			TEST CONDITIONS	SN54S289A		SN74S289A		UNIT
				TYP‡	MAX	TYP‡	MAX	
$t_{a(ad)}$	Access time from address		C_L = 30 pF, R_{L1} = 300 Ω, R_{L2} = 600 Ω, See Note 3	25	50	25	35	ns
$t_{a(S)}$	Access time from chip select (enable time)			18	25	18	22	ns
t_{SR}	Sense recovery time			22	40	22	35	ns
t_{PLH}	Propagation delay time, low-to-high-level output (disable time)	from $\overline{S}$		12	25	12	17	ns
		from $\overline{W}$		12	30	12	25	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C

NOTE: 3. Load circuit and voltage waveforms are shown on page 1-14.

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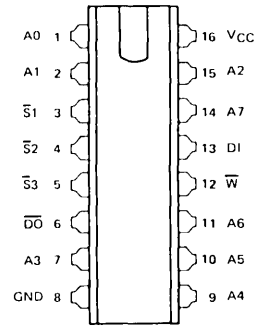
TYPES SN74S201, SN74S301
256-BIT HIGH-PERFORMANCE RANDOM-ACCESS MEMORIES

SEPTEMBER 1977—REVISED JUNE 1979

STATIC RANDOM-ACCESS MEMORIES

- Static Fully Decoded RAM's Organized as 256 Words of One Bit Each
- Schottky-Clamped for High Performance
- Choice of Three-State or Open-Collector Outputs
- Compatible with Most TTL and I^2L Circuits
- Chip-Select Inputs Simplify External Decoding
- Typical Performance:
  - Read Access Time ..... 42 ns
  - Power Dissipation ..... 500 mW

SN74S201, SN74S301 . . J OR N PACKAGE
(TOP VIEW)



description

These 256-bit active-element memories are monolithic transistor-transistor logic (TTL) arrays organized as 256 words of one bit. They are fully decoded and have three chip-select inputs to simplify decoding required to achieve expanded system organizations.

write cycle

The information applied at the data input is written into the selected location when the three chip-select inputs and the write-enable input are low. While the write-enable input is low, the 'S201 outputs are in the high-impedance state and the 'S301 outputs are off. When a number of outputs are bus-connected, this high-impedance or off state will neither load nor drive the bus line, but it will allow the bus line to be driven by another active output or a passive pull-up.

read cycle

The stored information (complement of information applied at the data input during the write cycle) is available at the output when the write-enable input is high and the three chip-select inputs are low. When any one of the chip-select inputs are high, the 'S201 outputs will be in the high-impedance state and the 'S301 outputs will be off.

FUNCTION TABLE

FUNCTION	INPUTS		'S201 OUTPUT ($\overline{DO}$)	'S301 OUTPUT ($\overline{DO}$)
	CHIP SELECT ($\overline{S}$)	WRITE ENABLE ($\overline{W}$)		
Write	L	L	High Impedance	Off
Read	L	H	Complement of Data Entered	Complement of Data Entered
Inhibit	H	X	High Impedance	Off

H ≡ high level, L ≡ low level, X ≡ irrelevant

‡For chip-select: L ≡ all $\overline{Si}$ inputs low, H ≡ one or more $\overline{Si}$ inputs high

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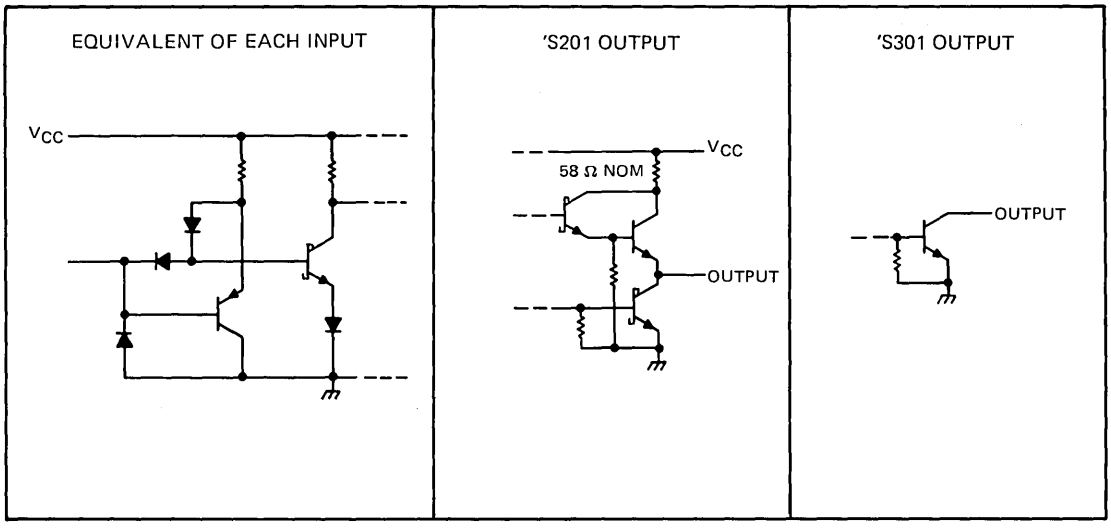
†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U. S. Patent Number 3,463,975.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Off-State output voltage . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN74S201			SN74S301			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage, V_{CC} (see Note 1)		4.75	5	5.25	4.75	5	5.25	V
High-level output voltage, V_{OH}							5.5	V
High-level output current, I_{OH}				−10.3				mA
Low-level output current, I_{OL}				16			16	mA
Width of write pulse (write enable low), $t_{w(wr)}$		65			65			ns
Setup time	Address before write pulse, $t_{su(ad)}$	0↓			0↓			ns
	Data before end of write pulse, $t_{su(da)}$	65↑			65↑			
	Chip-select before end of write pulse, $t_{su(\overline{S})}$	65↑			65↑			
Hold time	Address after write pulse, $t_{h(ad)}$	0↑			0↑			ns
	Data after write pulse, $t_{h(da)}$	0↑			0↑			
	Chip-select after write pulse, $t_{h(\overline{S})}$	0↑			0↑			
Operating free-air temperature, T_A		0		70	0		70	°C

↑↓ The arrow indicates the transition of the write input used for references: ↑ for the low to high transistion, ↓ for the high to low transistion.

NOTE 1: Voltage values are with respect to network ground terminal.

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electrical characteristics over recommended operating free-air temperature range (otherwise noted)

PARAMETER		TEST CONDITIONS†		'S201			'S301			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18mA				1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 08 V, I_{OH} = MAX		2.4						V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V,				0.45			0.45	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	V_O=2.4 V						40	μA
			V_O=5.5 V						100	
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = 0.8 V, V_{OH} = 2.4 V				40				μA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = 0.8 V, V_{OL} = 0.5 V				−40				μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				25			25	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V				−250			−250	μA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−30		−100				mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2			100	140		100	140	mA

†For conditions shown as MIN or MAX use the appropriate value specified under recommended operation conditions.
‡These typical values are at V_{CC} = 5 V, T_A = 25°C.
§Duration of the short circuit should not exceed one second.
NOTE: 2. I_{CC} is measured with all chip-select inputs grounded, all other inputs at 4.5 V, and the output open

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'S201 switching characteristics over recommended operating ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
$t_{a(ad)}$	Access time from address		C_L = 30 pF, R_L = 300 Ω, See Note 3		42	65	ns
$t_{a(S)}$	Access time from chip select (select time)				13	30	ns
t_{SR}	Sense recovery time				20	40	ns
t_{PXZ}	Disable time from high or low level	From $\overline{S}$	C_L = 5 pF, R_L = 300 Ω, See Note 3		9	20	ns
		From $\overline{W}$					

'S301 switching characteristics over recommended operating ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
$t_{a(ad)}$	Access time from address		C_L = 30 pF, R_{L1} = 300 Ω, R_{L2} = 600 Ω		42	65	ns
$t_{a(S)}$	Access time from chip enable (enable time)				13	30	ns
t_{SR}	Sense recovery time				20	40	ns
t_{PLH}	Propagation delay time, low-to-high-level output (disable time)	From $\overline{S}$	See Note 3		8	20	ns
		From $\overline{W}$			15	35	

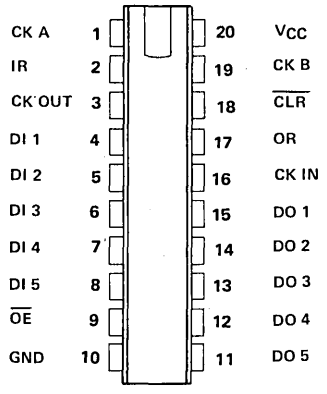
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE: 3. Load circuit and voltage waveforms are shown on page 1-14.

TYPE SN74S225
16 x 5 ASYNCHRONOUS FIRST-IN/FIRST-OUT MEMORY

SEPTEMBER 1976—REVISED JUNE 1979

- Independent Synchronous Inputs and Outputs
- Organized as 16-Words of 5 Bits
- DC to 10-MHz Data Rate
- 3-State Data Outputs
- 20-Pin, 300-mil, High-Density Package

SN74S225 . . . J OR N PACKAGE
(TOP VIEW)



Pin assignments are same for all packages

description

This 80-bit active-element memory is a monolithic Schottky-clamped transistor-transistor logic (STTL) array organized as 16 words of five-bits each. A memory system using the SN74S225 can easily be expanded in multiples of 16 words or of 5 bits as shown in Figure 2. The three-state outputs controlled by a single enable, OE, make bus connection and multiplexing easy.

operation

A FIFO is a memory storage device which allows data to be written into and/or read from its array at independent data rates. The 'S225 is a FIFO which will process data at any desired clock rate from DC to 10 MHz. The data is processed in a parallel format, word by word.

Reading or writing is done independently utilizing separate synchronous data clocks. Data may be written into the array on the low-to-high transition of either load clock input. Data may be read out of the array on the low-to-high transition of the unload clock input (normally high). When writing data into the FIFO one of the load clock inputs must be held high while the other strobes in the data. This arrangement allows either load clock to function as an inhibit for the other.

Status of the 'S225 is provided by three outputs. Input ready monitors the status of the last word location and signifies when the memory is full. This output is high whenever the memory is available to accept any data. The unload clock output also monitors the last word location. This output generates a low-logic-level pulse (synchronized to the internal clock pulse) when the location is vacant. The third status output, output ready, is high when the first word location contains valid data and unload clock input is high. When unload clock input is low, output ready will be low. The first word location is defined as the location from which data is provided to the outputs.

The data outputs are noninverted with respect to the data inputs and are three-state with a common control input, output enable. When output enable is low, the data outputs are enabled to function as totem-pole outputs. A high-logic-level forces each data output to a high-impedance state while all other inputs and outputs remain active.

The clear input invalidates all data stored in the memory array by clearing the control logic and setting output ready to a low-logic-level on the high-to-low transition of a low-active pulse. The data outputs do not change as a result of the clear input; however, the output ready at a low-logic-level signifies invalid data.

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†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U. S. Patent Number 3,463,975.

FUNCTION TABLES

Table 1 – Input Functions

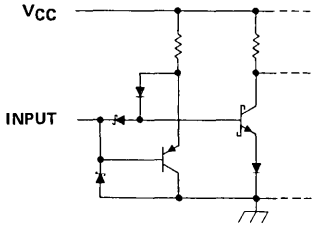
Input	Pin	Description
CK A	1	Load Clock A
DI 1 - DI 5	4-8	Data Inputs
$\overline{OE}$	9	Output Enable
CK IN	16	Unload Clock Input
$\overline{CLR}$	18	Clear
CK B	19	Load Clock B
GND	10	Ground pin
V_{CC}	20	Supply Voltage

Table 2 – Output Functions

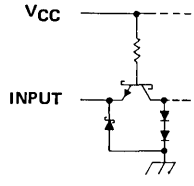
Output	Pin	Description
IR	2	Input Ready
CK OUT	3	Unload Clock Output
DO 5 - DO 1	11 - 15	Data Outputs
OR	17	Output Ready

schematics of inputs and outputs

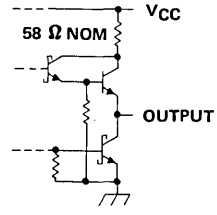
EQUIVALENT OF ALL INPUTS EXCEPT DATA INPUTS



EQUIVALENT OF DATA INPUTS



TYPICAL OF ALL OUTPUTS



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltage, V_{CC} (see Note 1) 7V
Input Voltage 5.5V
Off-State Output Voltage 5.5V
Operating Free-Air Temperature Range . . . . . 0°C to 70°C
Storage Temperature Range . . . . . −65°C to 150°C

NOTE 1: All voltage values are with respect to network ground terminal.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply Voltage, V_{CC}		4.75	5	5.25	V
High-level output current, I_{OH}	All Outputs Except Data			−3.2	mA
	Data Outputs			−6.5	
Low-level output current, I_{OL}	All Outputs Except Data			8	mA
	Data Outputs			16	
Pulse Width	Load Clock A or B, t_w (high)	25			ns
	Unload Clock Input, t_w (low)	7			
	Clear, t_w (low)	40			
Setup Time	Data to Load Clock, t_{su} (DIi) See Note 2	−20↑			ns
	Clear Release to Load Clock, t_{su}	25↑			
Hold Time, Data from Load Clock, t_h(DIi)		70↑			ns
Operating free-air temperature, T_A		0		70	°C

NOTE 2: Data must be setup within 15 ns after the load clock positive transition.

↑ ≡ The arrow indicates that the low-to-high transition of the load clock is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.2	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = MAX	2.4	2.9		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = MAX		0.35	0.50	V
I_{OZH}	Off-state output current, high-level voltage applied		V_{CC} = MAX, V_{IL} = 0.8 V,	V_{IH} = 2 V, V_O = 2.4 V			50	μA
I_{OZL}	Off-state output current, low-level voltage applied		V_{CC} = MAX, V_{IL} = 0.8 V,	V_{IH} = 2 V, V_O = 0.5 V			-50	μA
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	Data In	V_{CC} = MAX,	V_I = 2.7 V			40	μA
		All Inputs Except Data In					25	
I_{IL}	Low-level input current	Data In	V_{CC} = MAX,	V_I = 0.5 V			−1	mA
		All Inputs Except Data In					−250	μA
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−30		−100	mA
I_{CC}	Supply Current		V_{CC} = MAX,	See Note 3		80	120	mA

†For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Duration of the short circuit should not exceed one second.
NOTE 3: I_{CC} is measured with all inputs grounded and the output open.

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switching characteristics over recommended operating ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETERS¶	FROM	TO	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
f_{max}	CK A		C_L = 30 pF, R_L = 300 Ω, See Note 4	10	20		MHz
f_{max}	CK B			10	20		MHz
f_{max}	CK IN			10	20		MHz
t_w	CK OUT			7	14		ns
t_{PXZ}	$\overline{OE}$	DOi	C_L = 5 pF		10	25	ns
t_{PZX}			C_L = 30 pF, R_L = 300 Ω, See Note 4		25	40	
t_{PLH}	CK IN	DOi			50	75	ns
t_{PHL}					50	75	
t_{PLH}	CK A or CK B	OR			190	300	ns
t_{PLH}	CK IN	OR			40	60	ns
t_{PHL}					30	45	
t_{PHL}	$\overline{CLR}$	OR			35	60	ns
t_{PHL}	CK A or CK B	CK OUT			25	50	ns
t_{PHL}	CK IN	CK OUT			270	400	ns
t_{PHL}	CK A or CK B	IR			55	75	ns
t_{PLH}	CK IN	IR			255	400	ns
t_{PLH}	$\overline{CLR}$	IR			16	35	ns
t_{PLH}	OR↑	DOi			10	20	ns

¶ f_{max} ≡ maximum clock frequency.
t_w ≡ pulse width (output)
↑↓ ≡ The arrow indicates that the low-to-high (↑) or high-to-low (↓) transition of the output ready (OR) output is used for reference.
t_{PLH} ≡ propagation delay time, low-to-high level output.
t_{PHL} ≡ propagation delay time, high-to-low-level output.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 4: Load circuit and voltage waveforms are shown on page 1-14.

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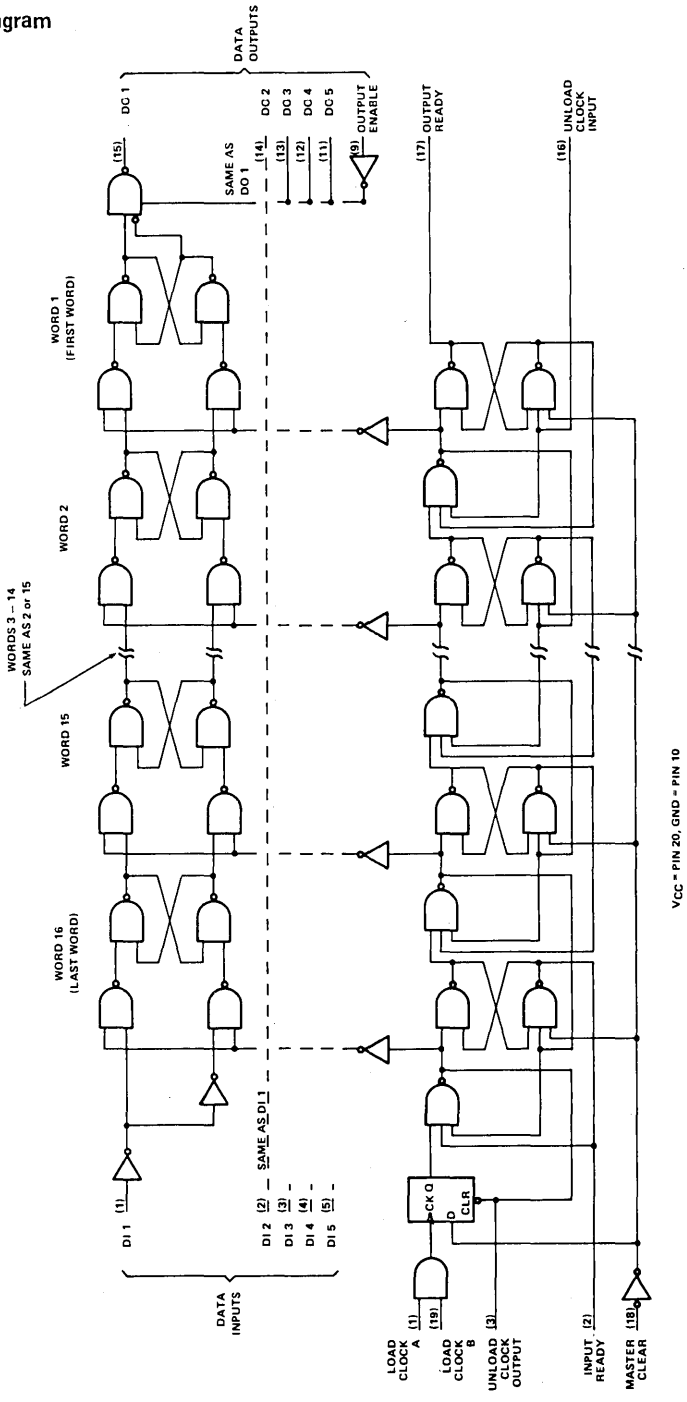
functional block diagram



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TYPICAL WAVEFORMS FOR A 16-WORD FIFO

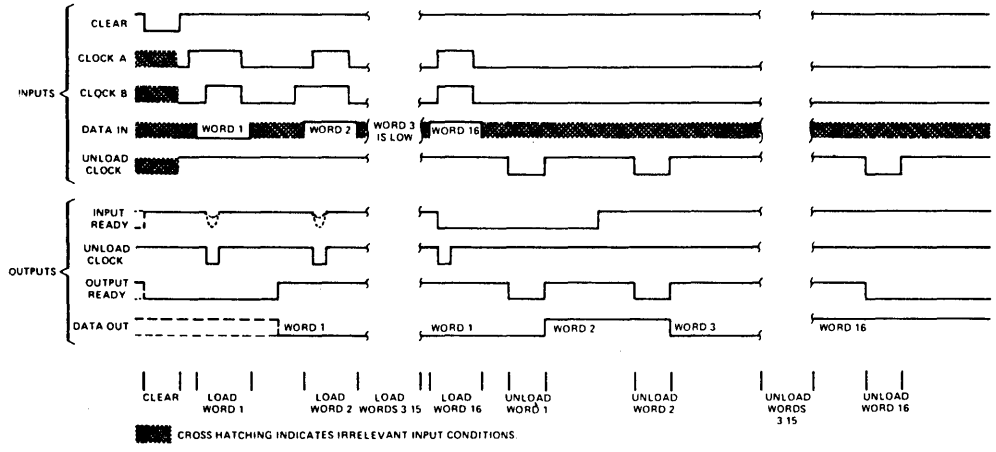

FIGURE 1 – TYPICAL WAVEFORMS FOR A 16-WORD FIFO

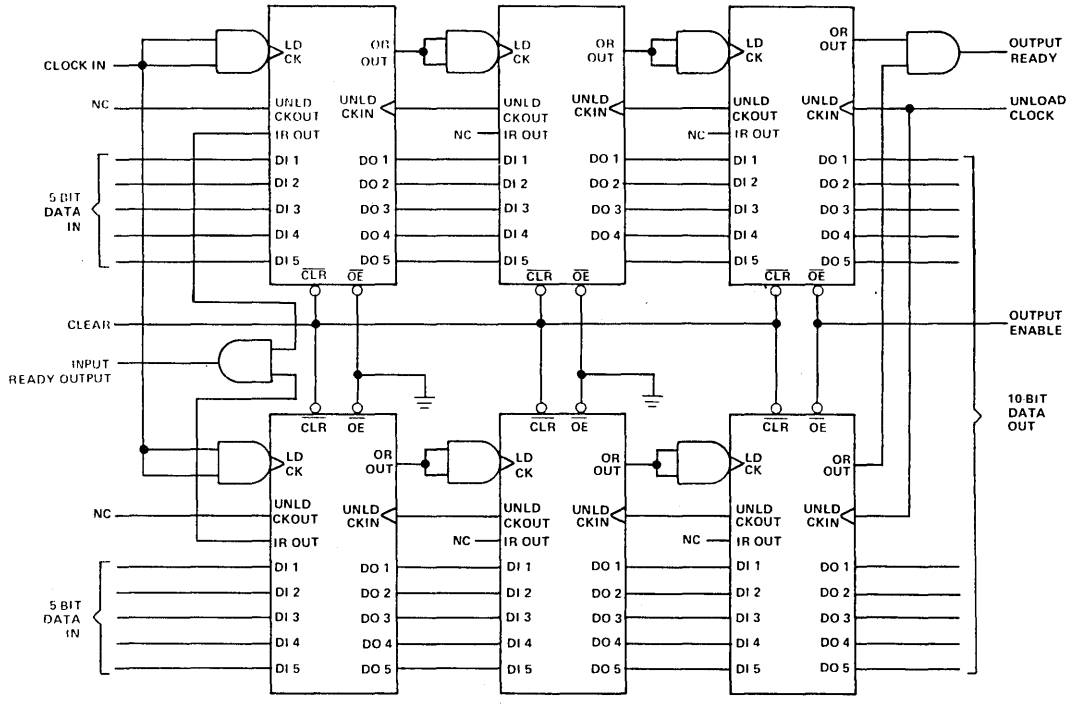

FIGURE 2 – EXPANDING THE 'S225 FIFO (48 WORDS OF 10 BITS SHOWN)

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Support Functions

INDEX TO SUPPORT FUNCTIONS

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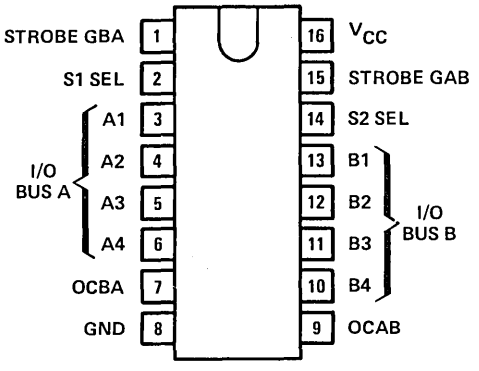
TYPES SN54S226, SN74S226
4-BIT PARALLEL LATCHED BUS TRANSCEIVERS

BULLETIN NO. DL-S 12477, OCTOBER 1976—REVISED AUGUST 1979

- Universal Transceivers for Implementing System Bus Controllers
- Dual-Rank 4-Bit Transparent Latches Provide:
  - Exchange of Data Between 2 Buses In One Clock Pulse
  - Bus-to-Bus Isolation
  - Rapid Data Transfer
  - Full Storage Capability
- Hysteresis at Data Inputs Enhances Noise Rejection
- Separate Output-Control Inputs Provide Independent Enable/Disable for Either Bus Output
- 3-State Outputs Drive Bus Lines Directly

SN54S226 . . . J PACKAGE
SN74S226 . . . J OR N PACKAGE
(TOP VIEW)



description

These high-performance Schottky† TTL quadruple bus transceivers employ dual-rank bidirectional four-bit transparent latches and feature three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The bus-management functions implemented and the high-impedance controls offered provide the designer with a controller/transceiver that interfaces and drives system bus-organized lines directly. They are particularly attractive for implementing:

Bidirectional bus transceivers
Data-bus controllers

The bus-management functions, under control of the function-select (S1, S2) inputs, provide complete data integrity for each of the four modes described in the function table. Directional transparency provides for routing data from or to either bus, and the dual store and dual readout capabilities can be used to perform the exchange of data between the two bus lines in the equivalent of a single clock pulse. Storage of data is accomplished by selecting the latch function, setting up the data, and taking the appropriate strobe input low. As long as the strobe is held high, the data is latched for the selected function. Further control is offered through the availability of independent output controls that can be used to enable or disable the outputs as shown in the output-control function table, regardless of the latch function in process. Store operations can be performed with the outputs disabled to a high impedance (Hi-Z). In the Hi-Z state the inputs/outputs neither load nor drive the bus lines significantly. The p-n-p inputs feature typically 400 millivolts of hysteresis to enhance noise rejection.

BUS-MANAGEMENT FUNCTION TABLE

MODE CONTROLS S2	S1	STROBES GAB	GBA	A-TO-B LATCHES 1	2	B-TO-A LATCHES 1	2	OPERATION
L	L	X	L	Latch	Trans	Trans	Trans	Pass B to A
			H			Latch	Trans	Read out stored data
L	H	X	X	Latch	Trans	Latch	Trans	Read out stored data
H	L	L	X	Trans	Trans	Latch	Trans	Pass A to B
		H		Latch	Trans			Read out stored data
H	H	L	L	Trans	Latch	Trans	Latch	Read in both buses
		H	H	Latch	Latch	Latch	Latch	Store bus data

H = high level L = low level X = irrelevant Latch = latched Trans = transparent

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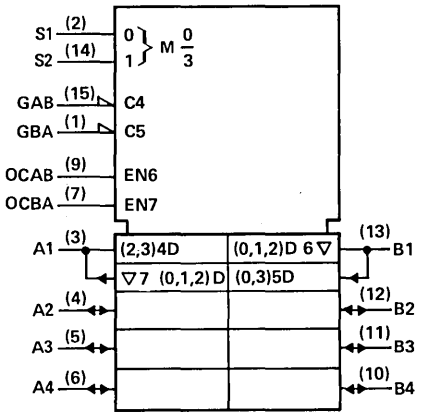
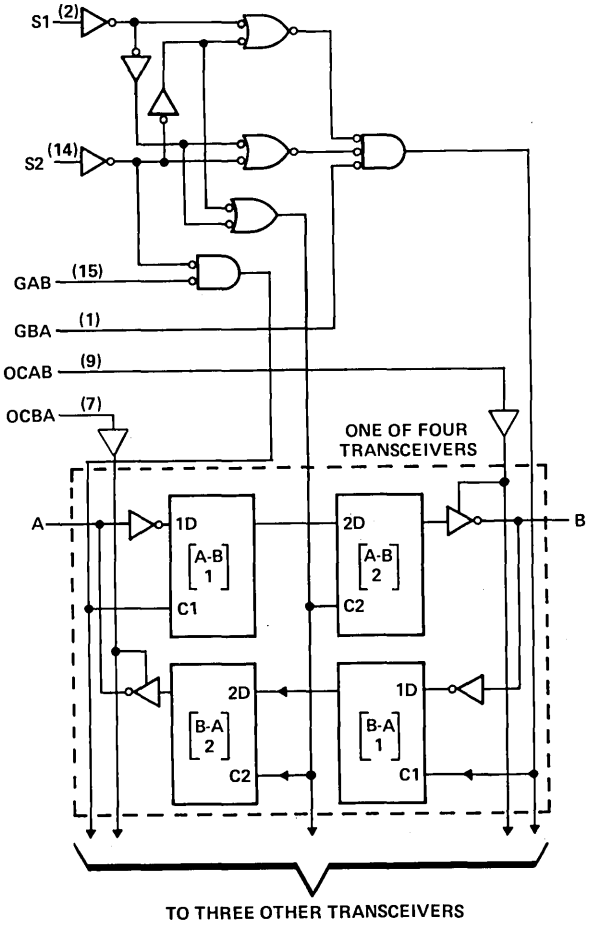
†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U.S. Patent Number 3,463,975.

logic symbol†



†This symbol is in accordance with IEEE Std 91/ANSI Y32.14 and current discussions in IEC and IEEE.

functional block diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)		7 V
Input voltage		5.5 V
Off-state output voltage		5.5 V
Operating free-air temperature range:	SN54S226 (see Note 2)	−55°C to 125°C
	SN74S226	0°C to 70°C
Storage temperature range		−65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. An SN54S226 in the J package operating at temperatures above 113°C requires a heat-sink that provides a thermal resistance from case to free air, $R_{\theta CA}$, of not more than 48°C/W.

recommended operating conditions

		SN54S226			SN74S226			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}				5.5			5.5	V
High-level output current, I_{OH}				−6.5			−10.3	mA
Width of strobe pulse		30			20			ns
Setup time, t_{su}	To Strobe	30↑			20↑			ns
	To Select	30			20			
Hold time, t_h	To Strobe	0↑			0↑			ns
	To Select	0			0			
Operating free-air temperature, T_A (see Note 2)		−55		125	0		70	°C

↑ The arrow indicates that the low-to-high transition of the strobe input is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA			−1.2	V
V_{OH}	High-level output voltage	SN54S226	V_{CC} = MIN, V_{IH} = 2 V,	2.4	3.3		V
		SN74S226	V_{IL} = 0.8 V, I_{OH} = MAX	2.4	2.9		
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 15 mA			0.5	V
I_{OZH}	Off-state output current, high-level voltage applied		V_{CC} = MAX, V_{IH} = 2 V, V_O = 2.4 V			100	μA
I_{OZL}	Off-state output current, low-level voltage applied		V_{CC} = MAX, V_{IH} = 2 V, V_O = 0.5 V			−100	μA
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7 V			100	μA
I_{IL}	Low-level input current	OCAB, OCBA	V_{CC} = MAX, V_I = 0.5 V			−0.38	mA
		All other inputs				−1.6	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	−50		−180	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 3		125	185	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

NOTES: 2. An SN54S226 in the J package operating at temperatures above 113°C requires a heat-sink that provides a thermal resistance from case to free air, $R_{\theta CA}$, of not more than 48°C/W.
3. I_{CC} is measured with all inputs (and outputs) grounded.

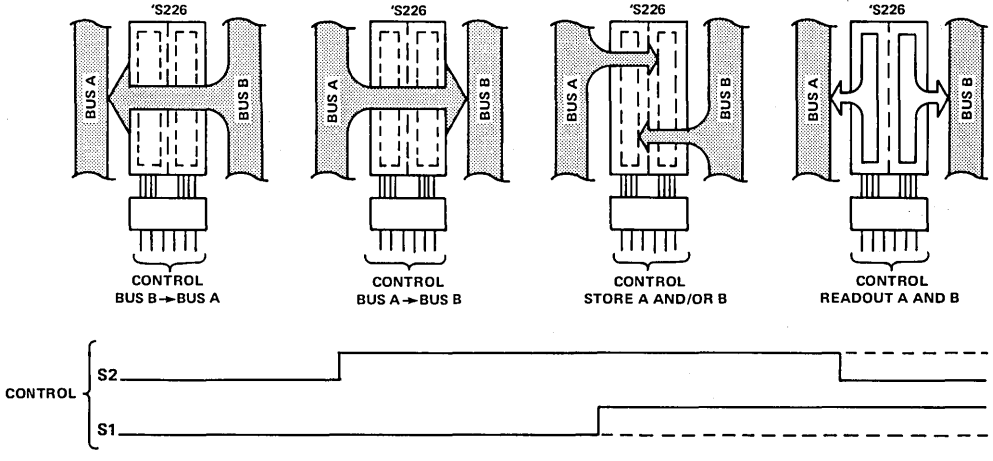
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	B or A	C_L = 50 pF, R_L = 280 Ω, See Note 4		20	30	ns
t_{PHL}					15	30	
t_{PLH}	Select	Any			25	37	ns
t_{PHL}					19	30	
t_{PLH}	Strobe GBA or GAB	A or B			25	37	ns
t_{PHL}					19	30	
t_{PZH}	Output Control OCBA or OCAB	A or B			12	20	ns
t_{PZL}					12	20	
t_{PHZ}	Output Control OCBA or OCAB	A or B	C_L = 5 pF, R_L = 280 Ω, See Note 4		10	15	ns
t_{PLZ}					10	15	

t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, low-to-high-level output
t_{ZH} ≡ output enable time to high level
t_{ZL} ≡ output enable time to low level
t_{HZ} ≡ output disable time from high level
t_{LZ} ≡ output disable time from low level
NOTE 4: Load circuits and voltage waveforms are shown on page 1-14.

applications

The following examples demonstrate four fundamental bus-management functions that can be performed with the 'S226. Exchange of data on the two bus lines can be accomplished with a single high-to-low transition at S2 when S1 is high.



TYPES SN54LS240,SN54LS241,SN54LS244,SN54S240,SN54S241, SN74LS240,SN74LS241,SN74LS244,SN74S240,SN74S241
OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

AUGUST 1979

	Typical I_{OL} (Sink Current)	Typical I_{OH} (Source Current)	Typical Propagation Delay Times		Typical Enable/ Disable Times	Typical Power Dissipation (Enabled)	
			Inverting	Noninverting		Inverting	Noninverting
SN54LS'	12 mA	−12 mA	10.5 ns	12 ns	18 ns	130 mW	135 mW
SN74LS'	24 mA	−15 mA	10.5 ns	12 ns	18 ns	130 mW	135 mW
SN54S'	48 mA	−12 mA	4.5 ns	6 ns	9 ns	450 mW	538 mW
SN74S'	64 mA	−15 mA	4.5 ns	6 ns	9 ns	450 mW	538 mW

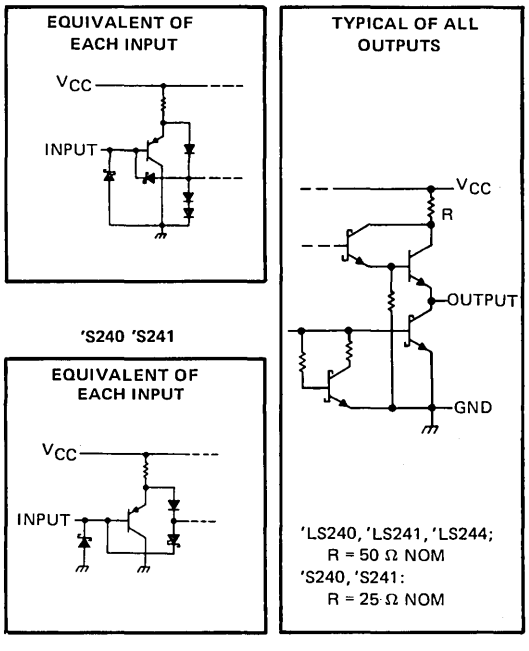
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- P-N-P Inputs Reduce D-C Loading
- Hysteresis at Inputs Improves Noise Margins

description

These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{G}$ (active-low output control) inputs, and complementary G and $\overline{G}$ inputs. These devices feature high fan-out, improved fan-in, and 400-mV noise-margin. The SN74LS' and SN74S' can be used to drive terminated lines down to 133 ohms.

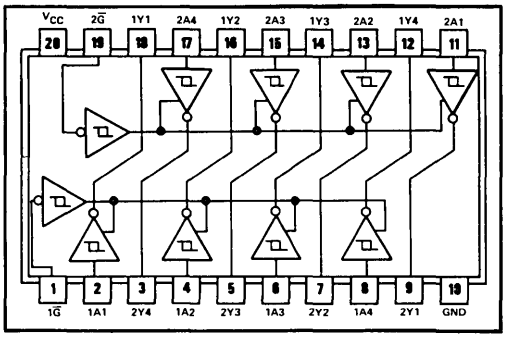
schematics of inputs and outputs

'LS240, 'LS241, 'LS244

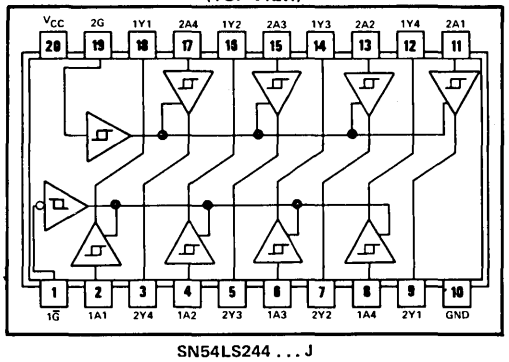


'S240 'S241

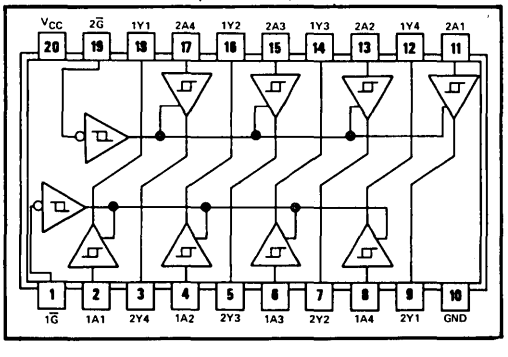
SN54LS240, SN54S240 . . . J
SN74LS240, SN74S240 . . . J OR N
(TOP VIEW)



SN54LS241, SN54S241 . . . J
SN74LS241, SN74S241 . . . J OR N
(TOP VIEW)



SN54LS244 . . . J
SN74LS244 . . . J OR N
(TOP VIEW)



6

877

absolute maximum ratings

Same as SN54LS245 and SN74LS245 on page 6-13.

recommended operating conditions

PARAMETER	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−12			−15	mA
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

NOTE 1: Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
	Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = MIN		0.2	0.4		0.2	0.4		V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, I_{OH} = −3 mA	2.4	3.4		2.4	3.4		V
		V_{CC} = MIN, V_{IL} = 0.5 V,	V_{IH} = 2 V, I_{OH} = MAX	2			2			
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max	I_{OL} = 12 mA			0.4			0.4	V
			I_{OL} = 24 mA						0.5	
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = V_{IL}max	V_O = 2.7 V			20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied		V_O = 0.4 V			−20			−20	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 7 V			0.1			0.1	mA
I_{IH}	High-level input current, any input	V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_{IL} = 0.4 V			−0.2			−0.2	mA
I_{OS}	Short-circuit output current♦	V_{CC} = MAX		−40		−225	−40		−225	mA
I_{CC}	Supply current, Outputs high	V_{CC} = MAX, Outputs open	All		17	27		17	27	mA
	Outputs low		'LS240		26	44		26	44	
			'LS241, 'LS244		27	46		27	46	
	All outputs disabled		'LS240		29	50		29	50	
			'LS241, 'LS244		32	54		32	54	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
♦Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		'LS240			'LS241, 'LS244			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 45 pF, See Note 2	R_L = 667 Ω,		9	14		12	18	ns
t_{PHL}	Propagation delay time, high-to-low-level output				12	18		12	18	ns
t_{PZL}	Output enable time to low level				20	30		20	30	ns
t_{PZH}	Output enable time to high level				15	23		15	23	ns
t_{PLZ}	Output disable time from low level	C_L = 5 pF, See Note 2	R_L = 667 Ω,		15	25		15	25	ns
t_{PHZ}	Output disable time from high level				10	18		10	18	ns

NOTE 2: Load circuit and voltage waveforms are shown on page 1-15.

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absolute maximum ratings

Same as the SN54S740 and SN74S740 maximum ratings on page 6-106.

recommended operating conditions

PARAMETER	SN54S'			SN74S'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−12			−15	mA
Low-level output current, I_{OL}			48			64	mA
External resistance between any input or V_{CC} and ground			40			40	kΩ
Operating free-air temperature, T_A (see Note 3)	−55		125	0		70	°C

NOTES: 1. Voltage values are with respect to network ground terminal.
3. An SN54S241J operating at free-air temperature above 116°C requires a heat sink that provides a thermal resistance from case to free-air, $R_{\theta CA}$, of not more than 40°C/W.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

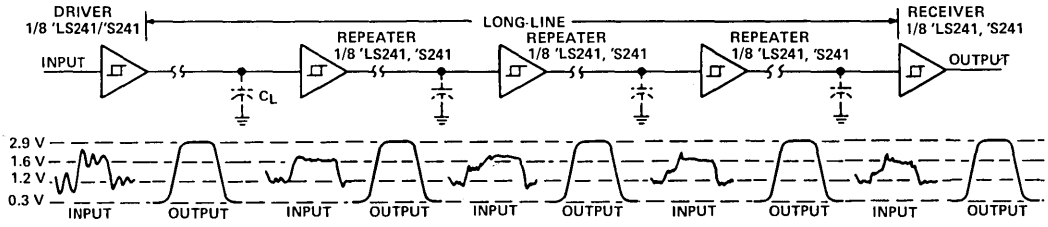
PARAMETER			TEST CONDITIONS†		'S240			'S241			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
	Hysteresis ($V_{T+} - V_{T-}$)		V_{CC} = MIN		0.2	0.4		0.2	0.4		V
V_{OH}	High-level output voltage	SN74S'	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V,	I_{OH} = −1 mA	2.7			2.7			V
		SN54S' and SN74S'	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V,	I_{OH} = −3 mA	2.4	3.4		2.4	3.4		V
		SN54S' and SN74S'	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.5 V,	I_{OH} = MAX	2			2			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V,	I_{OL} = MAX			0.55			0.55	V
I_{OZH}	Off-state output current, high-level voltage applied		V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = 0.8 V	V_O = 2.4 V			50			50	μA
I_{OZL}	Off-state output current, low-level voltage applied			V_O = 0.5 V			−50			−50	μA
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current, any input		V_{CC} = MAX,	V_I = 2.7 V			50			50	μA
I_{IL}	Low-level input current	Any A	V_{CC} = MAX,	V_I = 0.5 V			−400			−400	μA
		Any G					−2			−2	mA
I_{OS}	Short-circuit output current♦		V_{CC} = MAX		−50		−225	−50		−225	mA
I_{CC}	Supply current	Outputs high	V_{CC} = MAX, Outputs open	SN54S'		80	123		95	147	mA
				SN74S'		80	135		95	160	
		Outputs low		SN54S'		100	145		120	170	
				SN74S'		100	150		120	180	
		Outputs disabled		SN54S'		100	145		120	170	
				SN74S'		100	150		120	180	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
♦Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

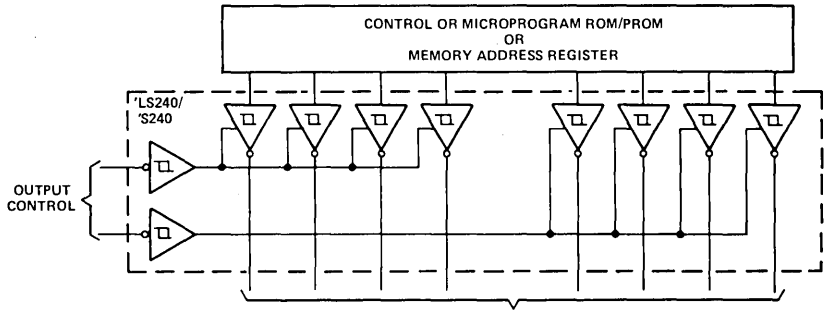
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		'S240			'S241			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF, See Note 4	R_L = 90 Ω,		4.5	7		6	9	ns
t_{PHL}	Propagation delay time, high-to-low-level output				4.5	7		6	9	ns
t_{PZL}	Output enable time to low level				10	15		10	15	ns
t_{PZH}	Output enable time to high level				6.5	10		8	12	ns
t_{PLZ}	Output disable time from low level	C_L = 5 pF, See Note 4	R_L = 90 Ω,		10	15		10	15	ns
t_{PHZ}	Output disable time from high level				6	9		6	9	ns

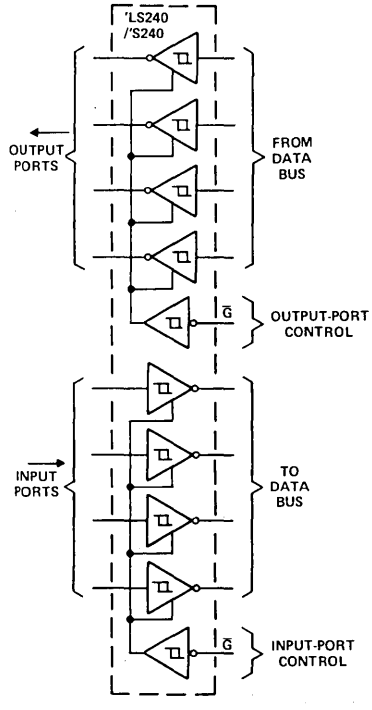
NOTE 4: Load circuit and voltage waveforms are shown on page 1-14.



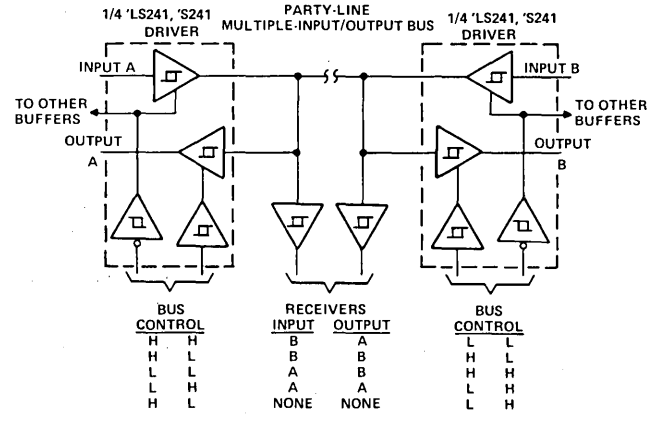
'LS241, 'S241 USED AS REPEATER/LEVEL RESTORER



'LS241, 'S240 USED AS SYSTEM AND/OR MEMORY BUS DRIVER—4-BIT ORGANIZATION CAN BE APPLIED TO HANDLE BINARY OR BCD



INDEPENDENT 4-BIT BUS DRIVERS/RECEIVERS IN A SINGLE PACKAGE



PARTY-LINE BUS SYSTEM WITH MULTIPLE INPUTS, OUTPUTS, AND RECEIVERS

External resistance between any input of the 'S240 or 'S241 and ground or V_{CC} must not exceed 40 kΩ.

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AUGUST 1979

- Two-Way Asynchronous Communication Between Data Buses
- P-N-P Inputs Reduce D-C Loading
- Hysteresis (Typically 400 mV) at Inputs Improves Noise Margin

description

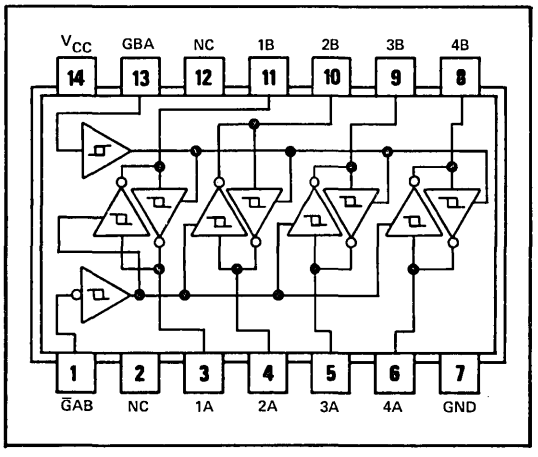
These four-data-line transceivers are designed for asynchronous two-way communications between data buses. The SN74LS' can be used to drive terminated lines down to 133 ohms.

FUNCTION TABLE (EACH TRANSCEIVER)

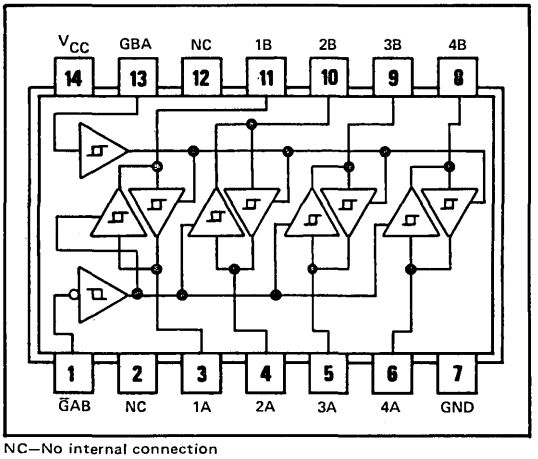
CONTROL INPUTS		'LS242 DATA PORT STATUS		'LS243 DATA PORT STATUS	
$\overline{G}AB$	GBA	A	B	A	B
H	H	$\overline{O}$	I	O	I
L	H	*	*	*	*
H	L	ISOLATED		ISOLATED	
L	L	I	$\overline{O}$	I	O

*Possibly destructive oscillation may occur if the transceivers are enabled in both directions at once.
I = Input, O = Output, $\overline{O}$ = Inverting Output.

SN54LS242 . . . J OR W
SN74LS242 . . . J OR N
(TOP VIEW)

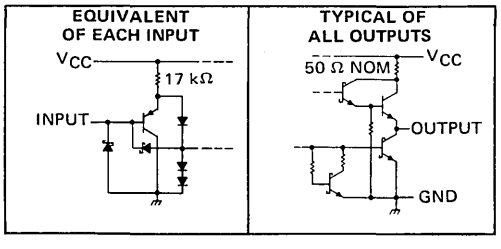


SN54LS243 . . . J OR W
SN74LS243 . . . J OR N
(TOP VIEW)



NC—No internal connection

schematics of inputs and outputs



absolute maximum ratings

Same as SN54LS245 and SN74LS245 maximum ratings on page 6-13.

recommended operating conditions

	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−12			−15	mA
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

NOTE 1: Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS' MIN	SN54LS' TYP‡	SN54LS' MAX	SN74LS' MIN	SN74LS' TYP‡	SN74LS' MAX	UNIT
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
	Hysteresis ($V_{T+} - V_{T-}$)		V_{CC} = MIN		0.2	0.4		0.2	0.4		V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, I_{OH} = −3 mA	2.4	3.1		2.4	3.1		V
			V_{CC} = MIN, V_{IL} = 0.5 V,	V_{IH} = 2 V, I_{OH} = MAX	2			2			
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied		V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = V_{IL} max	V_O = 2.7 V			40			40	μA
I_{OZL}	Off-state output current, low-level voltage applied			V_O = 0.4 V			−200			−200	μA
I_I	Input current at maximum input voltage	A or B	V_{CC} = MAX,	V_I = 5.5 V			0.1			0.1	mA
		$\overline{G}$AB or GBA		V_I = 7 V			0.1			0.1	
I_{IH}	High-level input current, any input		V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current	A inputs	V_{CC} = MAX, $\overline{G}$AB and GBA at V_{IL} max	V_I = 0.4 V,			−0.2			−0.2	mA
		B inputs	V_{CC} = MAX, $\overline{G}$AB and GBA at 2 V	V_I = 0.4 V,			−0.2			−0.2	
		$\overline{G}$AB or GBA	V_{CC} = MAX,	V_I = 0.4 V			−0.2			−0.2	
I_{OS}	Short-circuit output current♦		V_{CC} = MAX		−40		−225	−40		−225	mA
I_{CC}	Supply current	Outputs high	V_{CC} = MAX, Outputs open, See Note 2	'LS242, 'LS243		22	38		22	38	mA
		Outputs low		'LS242, 'LS243		29	50		29	50	
		All outputs disabled		'LS242		29	50		29	50	
				'LS243		32	54		32	54	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
♦Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 2: I_{CC} is measured with transceivers enabled in one direction only, or with all transceivers disabled.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	'LS242 MIN	'LS242 TYP	'LS242 MAX	'LS243 MIN	'LS243 TYP	'LS243 MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 45 pF, R_L = 667 Ω, See Note 3		9	14		12	18	ns
t_{PHL}	Propagation delay time, high-to-low-level output			12	18		12	18	ns
t_{PZL}	Output enable time to low level			20	30		20	30	ns
t_{PZH}	Output enable time to high level			15	23		15	23	ns
t_{PLZ}	Output disable time from low level	C_L = 5 pF, R_L = 667 Ω, See Note 3		15	25		15	25	ns
t_{PHZ}	Output disable time from high level			10	18		10	18	ns

NOTE 3: Load circuit and waveforms are shown on page 1-15.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

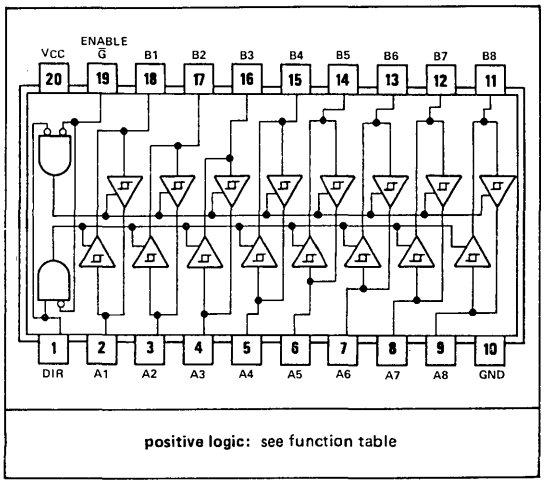
TYPES SN54LS245, SN74LS245
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

BULLETIN NO. DL-S 12471, OCTOBER 1976—REVISED FEBRUARY 1979

- Bi-directional Bus Transceiver in a High-Density 20-Pin Package
- 3-State Outputs Drive Bus Lines Directly
- P-N-P Inputs Reduce D-C Loading on Bus Lines
- Hysteresis at Bus Inputs Improve Noise Margins
- Typical Propagation Delay Times, Port-to-Port . . . 8 ns
- Typical Enable/Disable Times . . . 17 ns

TYPE	I_{OL} (SINK CURRENT)	I_{OH} (SOURCE CURRENT)
SN54LS245	12 mA	−12 mA
SN74LS245	24 mA	−15 mA

SN54LS245 . . . J PACKAGE
SN74LS245 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

description

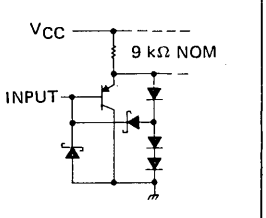
These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

The device allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so that the buses are effectively isolated.

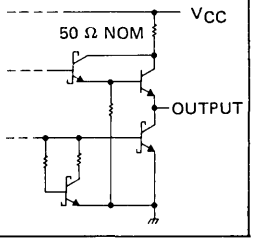
The SN54LS245 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LS245 is characterized for operation from 0°C to 70°C.

schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



TYPICAL OF ALL OUTPUTS



FUNCTION TABLE

ENABLE $\overline{G}$	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

H = high level, L = low level, X = irrelevant

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54LS' . . . . . −55°C to 125°C
SN74LS' . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

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recommended operating conditions

PARAMETER	SN54LS245			SN74LS245			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−12			−15	mA
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS245			SN74LS245			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
	Hysteresis ($V_{T+} - V_{T-}$) A or B input		V_{CC} = MIN		0.2	0.4		0.2	0.4		V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OH} = −3 mA	2.4	3.4		2.4	3.4		V
				I_{OH} = MAX	2			2			
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 12 mA			0.4			0.4	V
				I_{OL} = 24 mA						0.5	
I_{OZH}	Off-state output current, high-level voltage applied		V_{CC} = MAX, $\overline{G}$ at 2 V	V_O = 2.7 V			20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied			V_O = 0.4 V			−200			−200	
I_I	Input current at maximum input voltage	A or B	V_{CC} = MAX,	V_I = 5.5 V			0.1			0.1	mA
		DIR or $\overline{G}$		V_I = 7 V			0.1			0.1	
I_{IH}	High-level input current		V_{CC} = MAX,	V_{IH} = 2.7 V			20			20	μA
I_{IL}	Low-level input current		V_{CC} = MAX,	V_{IL} = 0.4 V			−0.2			−0.2	mA
I_{OS}	Short-circuit output current¶		V_{CC} = MAX		−40		−225	−40		−225	mA
I_{CC}	Supply current	Total, outputs high	V_{CC} = MAX,	Outputs open		48	70		48	70	mA
		Total, outputs low				62	90		62	90	
		Outputs at Hi-Z				64	95		64	95	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
¶Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 45 pF,	R_L = 667 Ω,	See Note 2		8	12	ns
t_{PHL}	Propagation delay time, high-to-low-level output					8	12	ns
t_{PZL}	Output enable time to low level					27	40	ns
t_{PZH}	Output enable time to high level					25	40	ns
t_{PLZ}	Output disable time from low level	C_L = 5 pF,	R_L = 667 Ω,	See Note 2		15	25	ns
t_{PHZ}	Output disable time from high level					15	25	ns

NOTE 2: Load circuit and waveforms are shown on page 1-15.

TEXAS INSTRUMENTS
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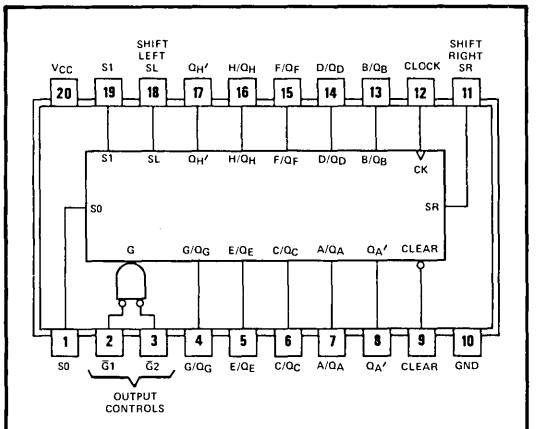
TYPES SN54LS299, SN54S299, SN74LS299, SN74S299
8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS

BULLETIN NO. DL-S 12115, MARCH 1974—REVISED FEBRUARY 1979

- Multiplexed Inputs/Outputs Provide Improved Bit Density
- Four Modes of Operation:
  Hold (Store) Shift Left
  Shift Right Load Data
- Operates with Outputs Enabled or at High Z
- 3-State Outputs Drive Bus Lines Directly
- Can Be Cascaded for N-Bit Word Lengths
- SN54LS323 and SN74LS323 Are Similar But Have Synchronous Clear
- Applications:
  Stacked or Push-Down Registers.
  Buffer Storage, and
  Accumulator Registers

TYPE	GUARANTEED SHIFT (CLOCK) FREQUENCY	TYPICAL POWER DISSIPATION
'LS299	35 MHz	175 mW
'S299	50 MHz	700 mW

SN54LS299, SN54S299 . . . J PACKAGE
SN74LS299, SN74S299 . . . J OR N PACKAGE
(TOP VIEW)



logic: see description and function table

description

These Schottky† TTL eight-bit universal registers feature multiplexed inputs/outputs to achieve full eight-bit data handling in a single 20-pin package. Two function-select inputs and two output-control inputs can be used to choose the modes of operation listed in the function table.

Synchronous parallel loading is accomplished by taking both function-select lines, S0 and S1, high. This places the three-state outputs in a high-impedance state, which permits data that is applied on the input/output lines to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. A direct overriding input is provided to clear the register whether the outputs are enabled or off.

6

FUNCTION TABLE

MODE	INPUTS								INPUTS/OUTPUTS								OUTPUTS	
	CLEAR	FUNCTION SELECT		OUTPUT CONTROL		CLOCK	SERIAL		A/Q_A	B/Q_B	C/Q_C	D/Q_D	E/Q_E	F/Q_F	G/Q_G	H/Q_H	$Q_{A'}$	$Q_{H'}$
		S1	S0	$\overline{G1}$†	$\overline{G2}$†		SL	SR										
Clear	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
Hold	H	L	L	L	L	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
	H	X	X	L	L	L	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
Shift Right	H	L	H	L	L	↑	X	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	H	Q_{Gn}
	H	L	H	L	L	↑	X	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	L	Q_{Gn}
Shift Left	H	H	L	L	L	↑	H	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	H	Q_{Bn}	H
	H	H	L	L	L	↑	L	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	L	Q_{Bn}	L
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h

†When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

a . . . h = the level of the steady-state input at inputs A through H, respectively. These data are loaded into the flip-flops while the flip-flop outputs are isolated from the input/output terminals. See explanation of function tables on page 1-13.

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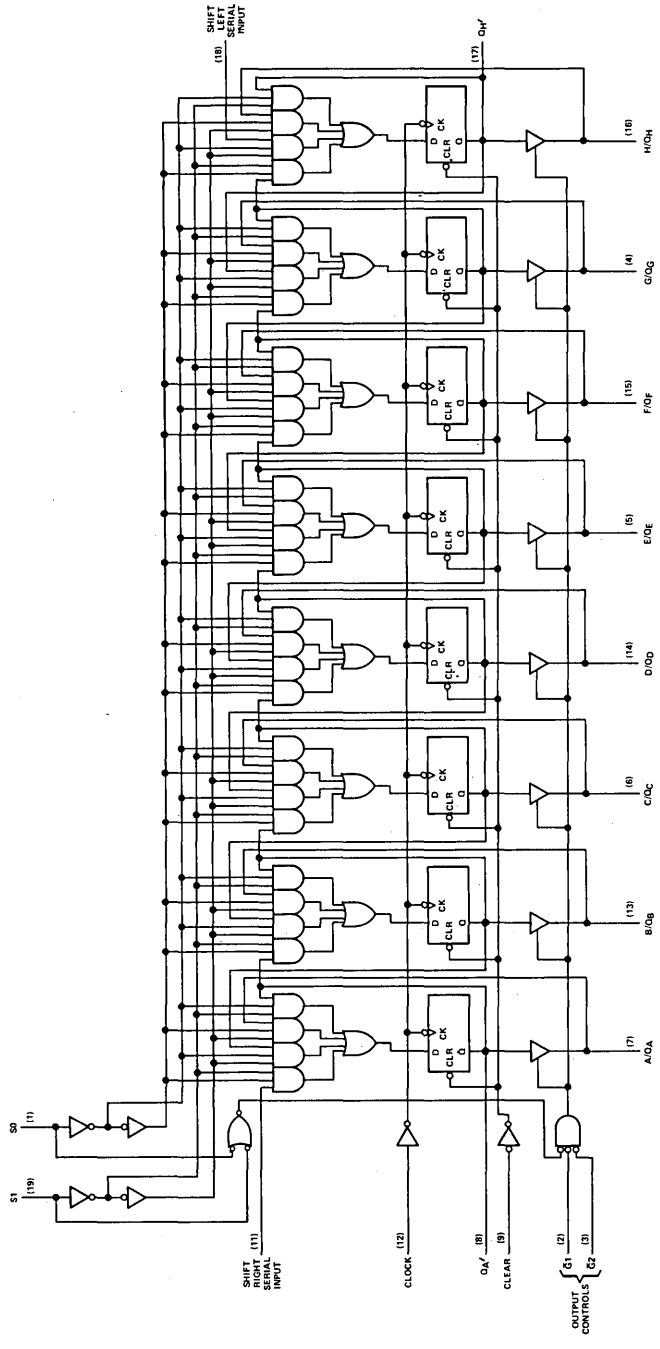
†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U.S. Patent Number 3,463,975.

functional block diagram



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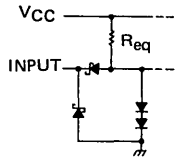
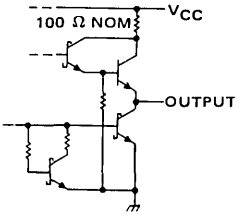
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT

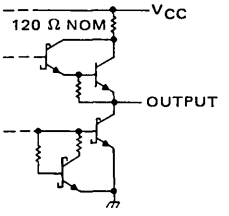


S0, S1: R_{eq} = 9 kΩ NOM
All other inputs: R_{eq} = 18 kΩ NOM

TYPICAL OF OUTPUTS
Q_A THRU Q_H



TYPICAL OF OUTPUTS
$Q_{A'}$ THRU $Q_{H'}$



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54LS299 . . . . . −55°C to 125°C
SN74LS299 . . . . . 0°C to 70°C
Storage temperature . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS299			SN74LS299			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	Q_A thru Q_H			−1			−2.6	mA
	$Q_{A'}$ or $Q_{H'}$			−0.4			−0.4	
Low-level output current, I_{OL}	Q_A thru Q_H			12			24	mA
	$Q_{A'}$ or $Q_{H'}$			4			8	
Clock frequency, f_{clock}		0		30	0		30	MHz
Width of clock pulse, $t_{w(clock)}$	Clock high	20			20			ns
	Clock low	20			20			
Width of clear pulse, $t_{w(clear)}$	Clear low	20			20			ns
Setup time, t_{su}	Select	30↑			30↑			ns
	High-level data◇	20↑			20↑			
	Low-level data◇	20↑			20↑			
	Clear inactive-state	20↑			20↑			
Hold time, t_h	Select	10↑			10↑			ns
	Data◇	0↑			0↑			
Operating free-air temperature, T_A		−55		125	0		70	°C

◇Data includes the two serial inputs and the eight input/output data lines.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS299 MIN	SN54LS299 TYP‡	SN54LS299 MAX	SN74LS299 MIN	SN74LS299 TYP‡	SN74LS299 MAX	UNIT
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	Q_A thru Q_H	V_{CC} = MIN,	V_{IH} = 2 V,	2.4	3.2		2.4	3.1		V
		Q_A' or Q_H'	V_{IL} = V_{IL}max,	I_{OH} = MAX	2.5	3.4		2.7	3.4		
V_{OL}	Low-level output voltage	Q_A thru Q_H	V_{CC} = MIN,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
			V_{IH} = 2 V,	I_{OL} = 24 mA					0.35	0.5	
		Q_A' or Q_H'	V_{IL} = V_{IL}max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	
				I_{OL} = 8 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	Q_A thru Q_H	V_{CC} = MAX, V_O = 2.7 V	V_{IH} = 2 V,			40			40	μA
I_{OZL}	Off-state output current, low-level voltage applied	Q_A thru Q_H	V_{CC} = MAX, V_O = 0.4 V	V_{IH} = 2 V,			−400			−400	μA
I_I	Input current at maximum input voltage	S0, S1	V_{CC} = MAX	V_I = 7 V			200			200	μA
		A thru H		V_I = 5.5 V			100			100	
		Any other		V_I = 7 V			100			100	
I_{IH}	High-level input current	A thru H, S0, S1	V_{CC} = MAX,	V_I = 2.7 V			40			40	μA
		Any other					20			20	
I_{IL}	Low-level input current	S0, S1	V_{CC} = MAX,	V_I = 0.4 V			−0.8			−0.8	mA
		Any other					−0.4			−0.4	
I_{OS}	Short-circuit output current§	Q_A thru Q_H	V_{CC} = MAX		−30		−130	−30		−130	mA
		Q_A' or Q_H'			−20		−100	−20		−100	
I_{CC}	Supply current		V_{CC} = MAX			33	53		33	53	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			See Note 2	30	35		MHz
t_{PLH}	Clock	Q_A' or Q_H'	C_L = 15 pF, R_L = 2 kΩ, See Note 2		22	33	ns
t_{PHL}					26	39	
t_{PHL}	Clear	Q_A' or Q_H'			27	40	ns
t_{PLH}	Clock	Q_A thru Q_H	C_L = 45 pF, R_L = 665 Ω, See Note 2		17	25	ns
t_{PHL}					26	39	
t_{PHL}	Clear	Q_A thru Q_H			26	40	ns
t_{PZH}	$\overline{G}1$, $\overline{G}2$	Q_A thru Q_H			13	21	ns
t_{PZL}					19	30	
t_{PHZ}	$\overline{G}1$, $\overline{G}2$	Q_A thru Q_H	C_L = 5 pF, R_L = 665 Ω, See Note 2		10	15	ns
t_{PLZ}					10	15	

¶ f_{max} ≡ maximum clock frequency
t_{PLH} ≡ propagation delay time, low-to-high-level output.
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
t_{PHZ} ≡ output disable time from high level
t_{PLZ} ≡ output disable time from low level

NOTE 2: For testing f_{max}, all outputs are loaded simultaneously, each with C_L and R_L as specified for the propagation times. See load circuits and waveforms on page 1-15.

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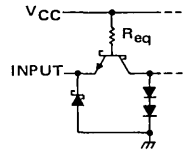
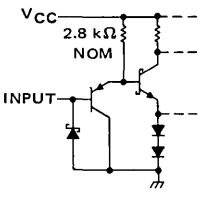
schematics of inputs and outputs

EQUIVALENT OF CLOCK AND CLEAR INPUTS

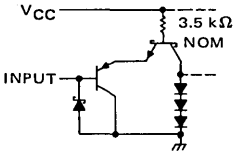


Clock: R_{eq} = 2.8 kΩ NOM
Clear: R_{eq} = 3.5 kΩ NOM

EQUIVALENT OF $\overline{G1}$ AND $\overline{G2}$ INPUTS

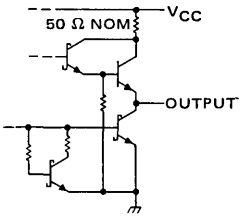


EQUIVALENT OF A THRU H†, S0, S1, SHIFT RIGHT, AND SHIFT LEFT INPUTS

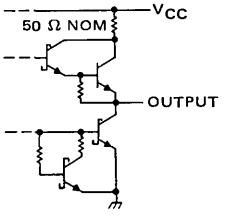


†When 3-state outputs are disabled.

TYPICAL OF OUTPUTS Q_A THRU Q_H



TYPICAL OF OUTPUTS $Q_{A'}$ AND $Q_{H'}$



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54S299 (see Note 2) . . . . . −55°C to 125°C
SN74S299 . . . . . 0°C to 70°C
Storage temperature . . . . . −65°C to 150°C

NOTES 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54S299			SN74S299			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	Q_A thru Q_H			−2			−6.5	mA
	$Q_{A'}$ or $Q_{H'}$			−0.5			−0.5	
Low-level output current, I_{OL}	Q_A thru Q_H			20			20	mA
	$Q_{A'}$ or $Q_{H'}$			6			6	
Clock frequency, f_{clock}		0		50	0		50	MHz
Width of clock pulse, $t_{w(clock)}$	Clock high	10			10			ns
	Clock low	10			10			
Width of clear pulse, $t_{w(clear)}$	Clear low	10			10			ns
Setup time, t_{su}	Select	15†			15†			ns
	High-level data◇	7†			7†			
	Low-level data◇	5†			5†			
	Clear inactive-state	10†			10†			
Hold time, t_h	Select	5†			5†			ns
	Data◇	5†			5†			
Operating free-air temperature, T_A		−55		125	0		70	°C

◇Data includes the two serial inputs and the eight input/output data lines.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA			−1.2	V
V_{OH}	High-level output voltage	Q_A thru Q_H	V_{CC} = MIN, V_{IH} = 2 V,	2.4	3.2		V
		$Q_{A'}$ or $Q_{H'}$	V_{IL} = 0.8 V, I_{OH} = MAX	2.7	3.4		
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = MAX			0.5	V
I_{OZH}	Off-state output current, high-level voltage applied	Q_A thru Q_H	V_{CC} = MAX, V_{IH} = 2 V, V_O = 2.4 V			100	μA
I_{OZL}	Off-state output current, low-level voltage applied	Q_A thru Q_H	V_{CC} = MAX, V_{IH} = 2 V, V_O = 0.5 V			−250	μA
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	A thru H, S0, S1	V_{CC} = MAX, V_I = 2.7 V			100	μA
		Any other				50	
I_{IL}	Low-level input current	Clock or clear	V_{CC} = MAX, V_I = 0.5 V			−2	mA
		Any other				−250	μA
I_{OS}	Short-circuit output current§	Q_A thru Q_H	V_{CC} = MAX	−40		−100	mA
		$Q_{A'}$ or $Q_{H'}$		−20		−100	
I_{CC}	Supply current		V_{CC} = MAX		140	225	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			See Note 2	50	70		MHz
t_{PLH}	Clock	$Q_{A'}$ or $Q_{H'}$	C_L = 15 pF, R_L = 1 kΩ, See Note 2		12	20	ns
t_{PHL}					13	20	
t_{PHL}	Clear	$Q_{A'}$ or $Q_{H'}$			14	21	ns
t_{PLH}	Clock	Q_A thru Q_H	C_L = 45 pF, R_L = 280 Ω, See Note 2		15	21	ns
t_{PHL}					15	21	
t_{PHL}	Clear	Q_A thru Q_H			16	24	ns
t_{PZH}	$\overline{G}1$, $\overline{G}2$	Q_A thru Q_H			10	18	ns
t_{PZL}					12	18	
t_{PHZ}	$\overline{G}1$, $\overline{G}2$	Q_A thru Q_H	C_L = 5 pF, R_L = 280 Ω, See Note 3		7	12	ns
t_{PLZ}					7	12	

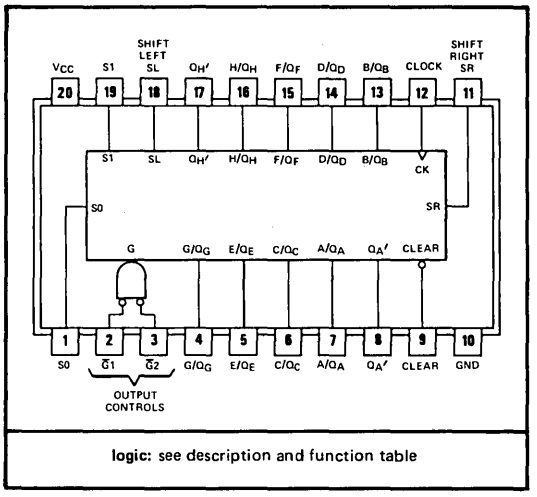
¶ f_{max} ≡ maximum clock frequency
t_{PLH} ≡ propagation delay time, low-to-high-level output.
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
t_{PHZ} ≡ output disable time from high level
t_{PLZ} ≡ output disable time from low level
NOTE 3: For testing f_{max}, all outputs are loaded simultaneously, each with C_L and R_L as specified for the propagation times. See load circuits and waveforms on page 1-14.

TYPES SN54LS323, SN74LS323
8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS

BULLETIN NO. DL-S 12462, OCTOBER 1976—REVISED AUGUST 1979

- Multiplexed Inputs/Outputs Provide Improved Bit Density
- Four Modes of Operation:
  Hold (Store) Shift Left
  Shift Right Load Data
- Operates with Outputs Enabled or at High Z
- 3-State Outputs Drive Bus Lines Directly
- Can Be Cascaded for N-Bit Word Lengths
- Typical Power Dissipation . . . 175 mW
- Guaranteed Shift (Clock) Frequency . . . 30 MHz
- Applications:
  Stacked or Push-Down Registers,
  Buffer Storage, and
  Accumulator Registers
- SN54LS299 and SN74LS299 Are Similar But Have Direct Overriding Clear

SN54LS323 . . . J PACKAGE
SN74LS323 . . . J OR N PACKAGE
(TOP VIEW)



logic: see description and function table

description

These Low-Power Schottky† eight-bit universal registers feature multiplexed inputs/outputs to achieve full eight-bit data handling in a single 20-pin package. Two function-select inputs and two output-control inputs can be used to choose the modes of operation listed in the function table. Synchronous parallel loading is accomplished by taking both function-select lines, S0 and S1, high. This places the three-state outputs in a high-impedance state, which permits data that is applied on the input/output lines to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. The clear function is synchronous, and a low level at the clear input clears the register on the next low-to-high transition of the clock.

FUNCTION TABLE

MODE	INPUTS								INPUTS/OUTPUTS								OUTPUTS	
	CLEAR	FUNCTION SELECT		OUTPUT CONTROL		CLOCK	SERIAL		A/Q_A	B/Q_B	C/Q_C	D/Q_D	E/Q_E	F/Q_F	G/Q_G	H/Q_H	$Q_{A'}$	$Q_{H'}$
		S1	S0	$\overline{G1}$†	$\overline{G2}$†		SL	SR										
Clear	L	X	L	L	L	↑	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	↑	X	X	L	L	L	L	L	L	L	L	L	L
Hold	H	L	L	L	L	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
	H	X	X	L	L	L	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
Shift Right	H	L	H	L	L	↑	X	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	H	Q_{Gn}
	H	L	H	L	L	↑	X	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	L	Q_{Gn}
Shift Left	H	H	L	L	L	↑	H	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	H	Q_{Bn}	H
	H	H	L	L	L	↑	L	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	L	Q_{Bn}	L
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h

†When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

a . . . h = the level of the steady-state input at inputs A through H, respectively. These data are loaded into the flip-flops while the flip-flop outputs are isolated from the input/output terminals. See explanation of function tables on page 1-19.

schematics of inputs and outputs, absolute maximum ratings, recommended operating conditions, and electrical characteristics

Same as SN54LS299 and SN74LS299, see page 6-17.

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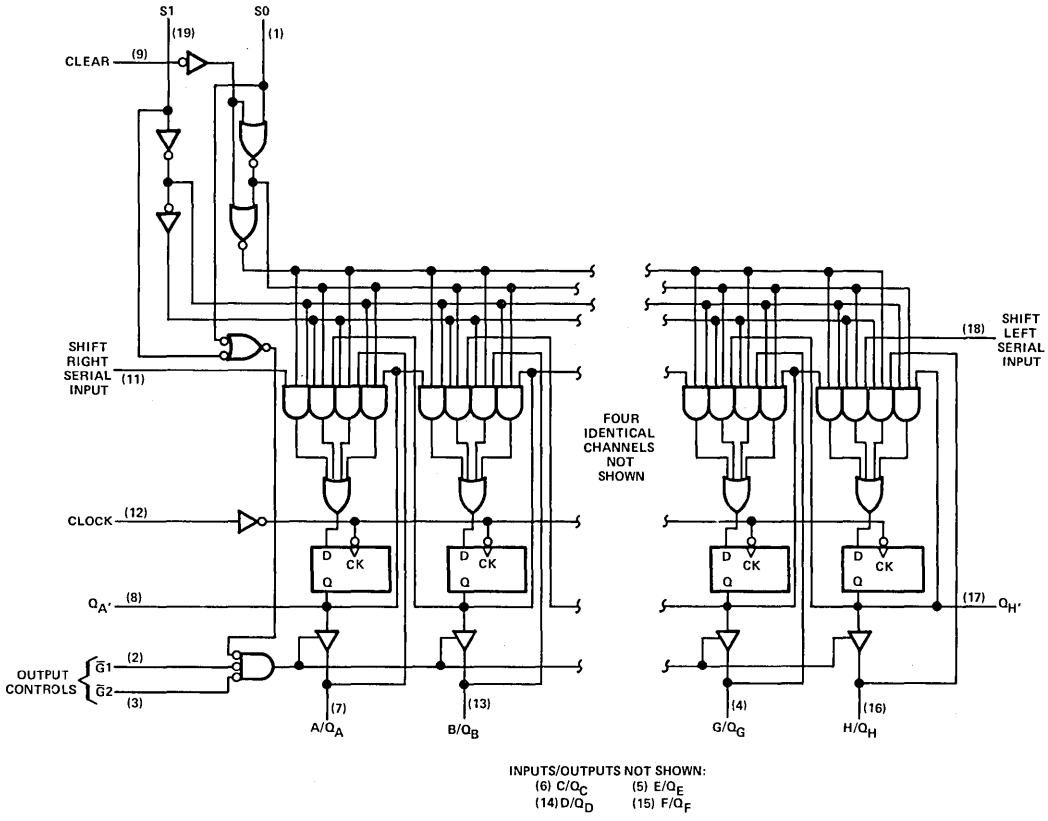
†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U.S. Patent Number 3,463,975.

functional block diagram



switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			See Note 1	30	35		MHz
t_{PLH}	Clock	$Q_{A'}$ or $Q_{H'}$	C_L = 15 pF, R_L = 2 kΩ, See Note 1		22	33	ns
t_{PHL}					26	39	
t_{PLH}	Clock	Q_A thru Q_H	C_L = 45 pF, R_L = 665 Ω, See Note 1		17	25	ns
t_{PHL}					25	39	
t_{PZH}	$\overline{G}1$, $\overline{G}2$	Q_A thru Q_H			14	21	ns
t_{PZL}					20	30	
t_{PHZ}	$\overline{G}1$, $\overline{G}2$	Q_A thru Q_H	C_L = 5 pF, R_L = 665 Ω, See Note 1		10	15	ns
t_{PLZ}					10	15	

¶ f_{max} ≡ maximum clock frequency
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
t_{PHZ} ≡ output disable time from high level
t_{PLZ} ≡ output disable time from low level

NOTE 1: For testing f_{max}, all outputs are loaded simultaneously, each with C_L and R_L as specified for the propagation times. See load circuits and waveforms on page 1–15.

TYPES SN74S340, SN74S341, SN74S344
OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

BULLETIN NO. DL-S 12710, JUNE 1979 – REVISED AUGUST 1979

	I_{OL} Typical (Sink Current)	I_{OH} Typical (Source Current)	Typical Propagation Delay Times	Typical Enable Times	Typical Disable Times
'S340	64 mA	15 mA	8 ns	17 ns	11 ns
'S341	64 mA	15 mA	9 ns	14 ns	16 ns
'S344	64 mA	15 mA	9 ns	14 ns	14 ns

- Pin-for-Pin Compatible With SN74S240 Series
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- Typical Input and Output Capacitances, $\leqslant$10 pF
- 300 mV Guaranteed Hysteresis at Inputs Improves Noise Margins

description

These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{G}$ (active-low output control) inputs, and complementary G and $\overline{G}$ inputs. These devices feature high fan-out, improved fan-in, 700–mV typical noise margin, and the capability of driving lines with terminations as low as 133 ohms.

SN74S340 FUNCTION TABLE

$1\overline{G}$	$2\overline{G}$	1Y OUTPUTS	2Y OUTPUTS
H	H	Z	Z
H	L	Z	Enabled (Inverting)
L	H	Enabled (Inverting)	Z
L	L	Enabled (Inverting)	Enabled (Inverting)

SN74S341 FUNCTION TABLE

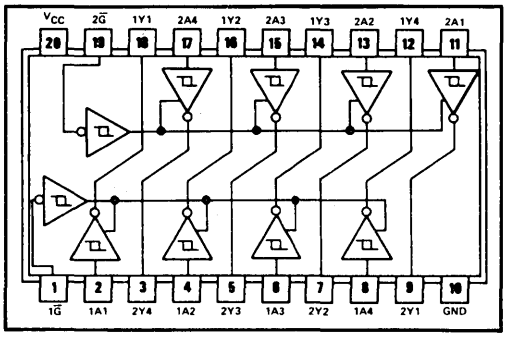
$1\overline{G}$	2G	1Y OUTPUTS	2Y OUTPUTS
H	H	Z	Enabled
H	L	Z	Z
L	H	Enabled	Enabled
L	L	Enabled	Z

SN74S344 FUNCTION TABLE

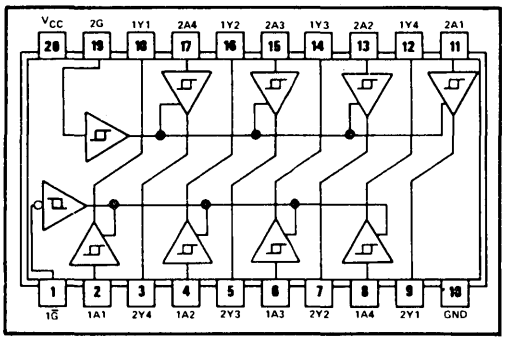
$1\overline{G}$	$2\overline{G}$	1Y OUTPUTS	2Y OUTPUTS
H	H	Z	Z
H	L	Z	Enabled
L	H	Enabled	Z
L	L	Enabled	Enabled

Z = high impedance (output off)

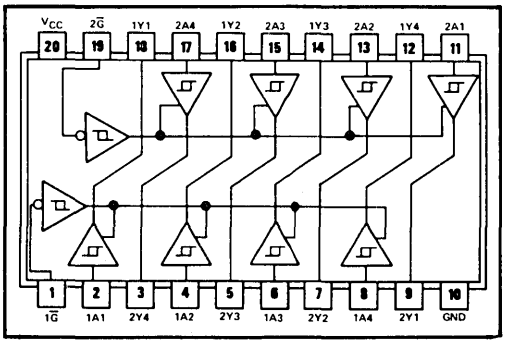
SN74S340 . . . J OR N PACKAGE
(TOP VIEW)



SN74S341 . . . J OR N PACKAGE
(TOP VIEW)



SN74S344 . . . J OR N PACKAGE
(TOP VIEW)



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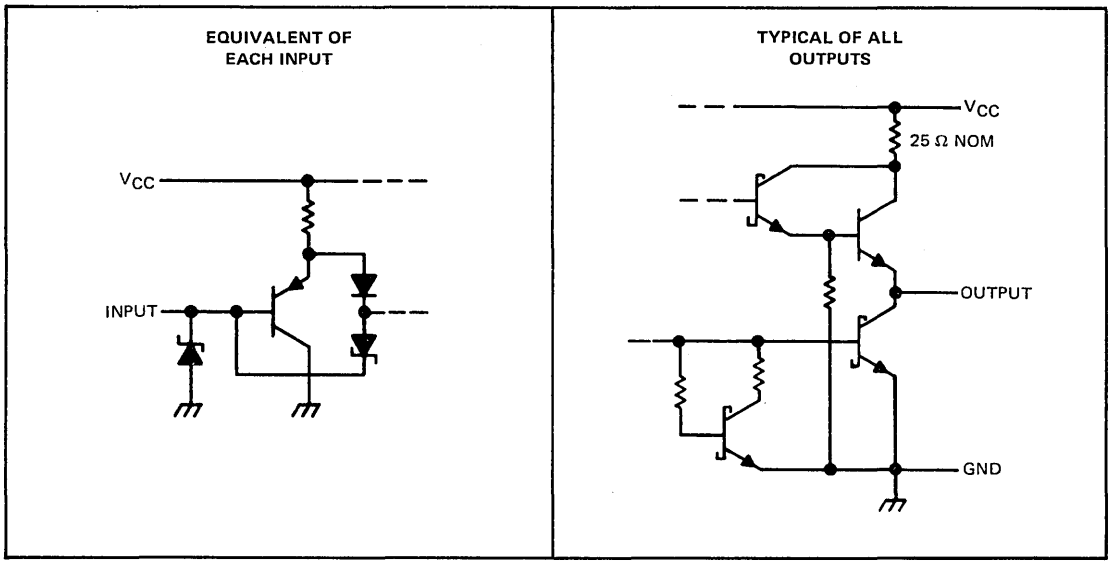
schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC} (see Note 1)	4.75	5	5.25	V
High-level output current, I_{OH}			−15	mA
Low-level output current, I_{OL}			64	mA
Operating free-air temperature, T_A	0		70	°C

NOTE 1: Voltage values are with respect to network ground terminal.

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electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN74S340			SN74S341, SN74S344			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{T+}	Positive-going threshold voltage			1.3	1.5	1.9	1.3	1.5	1.9	V
V_{T-}	Negative-going threshold voltage			0.6	0.85	1.05	0.6	0.85	1.05	V
	Hysteresis ($V_{T+} - V_{T-}$)			0.3	0.65		0.3	0.65		V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.5 V,	V_{IH} = 2 V, I_{OH} = −1 mA	2.4			2.4			V
		V_{CC} = MIN, V_{IL} = 0.5 V,	V_{IH} = 2 V, I_{OH} = −3 mA	2.4	3.4		2.4	3.4		
		V_{CC} = MIN, V_{IL} = 0.5 V,	V_{IH} = 2 V, I_{OH} = MAX	2			2			
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.5 V,	V_{IH} = 2 V, I_{OL} = MAX			0.55			0.55	V
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = 0 V	V_O = 2.4 V			50			50	μA
I_{OZL}	Off-state output current, low-level voltage applied		V_O = 0.5 V			−50			−50	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current, any input	V_{CC} = MAX,	V_I = 2.7 V			50			50	μA
I_{IL}	Low-level input current, Any A	V_{CC} = MAX,	V_I = 0.5 V			−250			−250	μA
	Low-level input current, Any G or $\overline{G}$					−250			−250	μA
I_{OS}	Short-circuit output current♦	V_{CC} = MAX		−50		−225	−50		−225	mA
I_{CC}	Supply current	V_{CC} = MAX, Outputs open	Outputs high			75			135	mA
			Outputs low			170			180	
			Outputs disabled			110			145	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
♦Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

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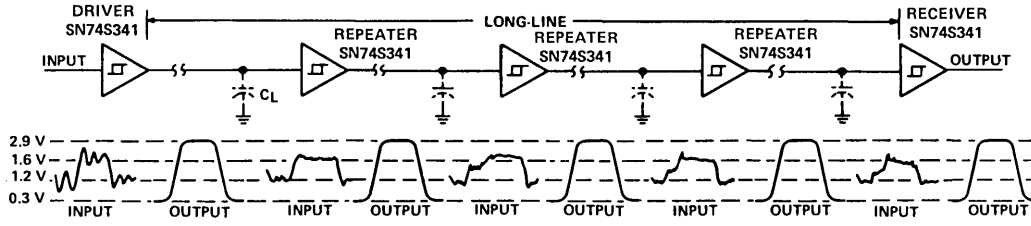
switching characteristics, V_{CC} = 5 V, T_A = 25°C

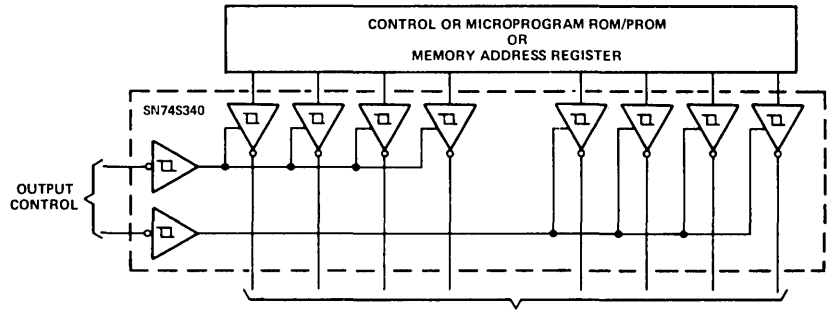
PARAMETER	TEST CONDITIONS		SN74S340			SN74S341			SN74S344			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	C_L = 50 pF, See Note 2	R_L = 90 Ω,		7	11		10	15		10	15	ns
t_{PHL}				8	12		8	12		8	12	ns
t_{PZL}				17	25		14	21		14	21	ns
t_{PZH}				11	16		11	17		11	17	ns
t_{PLZ}	C_L = 5 pF, See Note 2	R_L = 90 Ω,		11	17		16	25		14	23	ns
t_{PHZ}				5	9		8	13		5	9	ns

NOTE 2: Load circuit and voltage waveforms are shown on page 1-14.
t_{PLH} ≡ Propagation delay time, low-to-high-level input
t_{PHL} ≡ Propagation delay time, high-to-low-level input
t_{PZL} ≡ Output enable time to low level
t_{PZH} ≡ Output enable time to high level
t_{PLZ} ≡ Output disable time from low level
t_{PHZ} ≡ Output disable time from high level

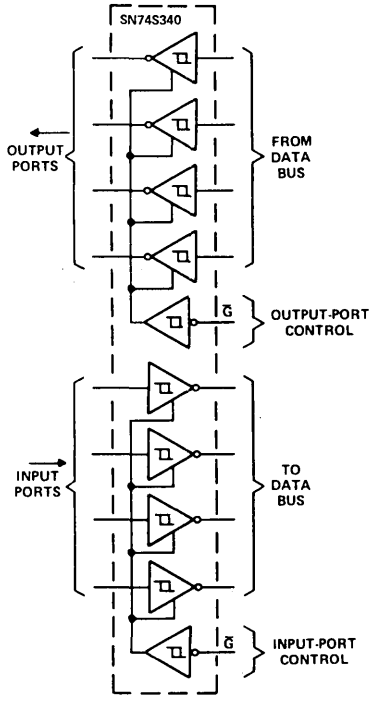
TYPICAL APPLICATION DATA



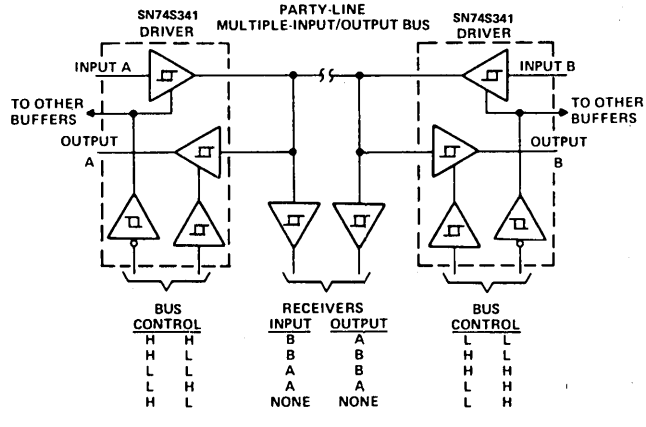
SN74S341 USED AS REPEATER/LEVEL RESTORER



SN74S340 USED AS SYSTEM AND/OR MEMORY BUS DRIVER—4-BIT ORGANIZATION CAN BE APPLIED TO HANDLE BINARY OR BCD



INDEPENDENT 4-BIT BUS DRIVERS/RECEIVERS IN A SINGLE PACKAGE



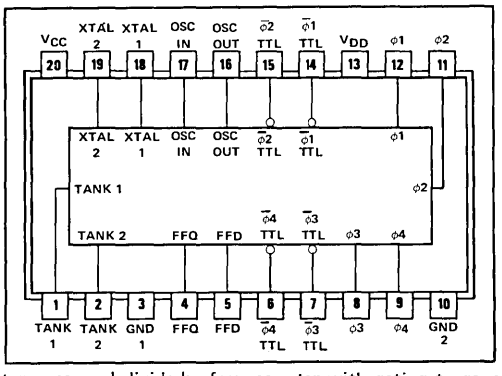
PARTY-LINE BUS SYSTEM WITH MULTIPLE INPUTS, OUTPUTS, AND RECEIVERS

TYPE SN74LS362 (TIM9904)
FOUR-PHASE CLOCK GENERATOR/DRIVER

BULLETIN NO. DL-S 12476, OCTOBER 1976–REVISED FEBRUARY 1979

- Clock Generator/Driver for The TMS 9900 or Other Microprocessors
- High-Level 4-Phase Outputs
- Complementary TTL 4-Phase Outputs
- Self-Contained Oscillator Can be Crystal or Capacitor Controlled
- External Oscillator Can Be Used
- Clocked D-Type Flip-Flop With Schmitt-Trigger Input For Reset Signal Synchronization

SN74LS362 . . . J OR N PACKAGE
(TOP VIEW)



description

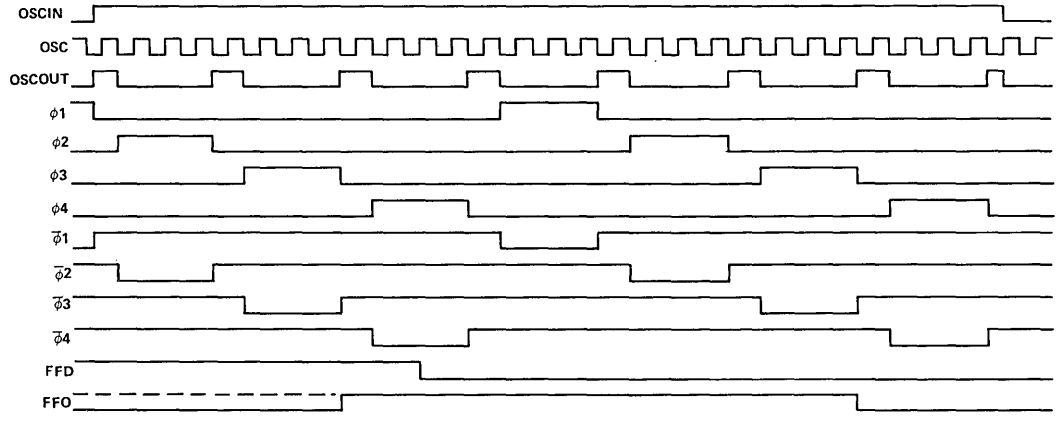
The 'LS362 consists of an oscillator, divide-by-four counter, a second divide-by-four counter with gating to generate four clock phases, high-level (12-volt) output drivers, low-level (5-volt) complementary output drivers, and a D-type flip-flop controlled by an external signal and the $\phi 3$ clock. The four high-level clock phases provide clock inputs to a TMS 9900 microprocessor. The four complementary TTL-level clocks can be used to time memory or other logic functions in a TMS 9900 computer system. The D-type flip-flop can be used to provide (for example) a reset signal to a TMS 9900, timed by $\phi 3$, on receipt of an input to the FFD input from power turn-on or a manual switch closure. Other applications are possible. A safety feature has been incorporated in the ϕ outputs such that if an open occurs in the V_{CC} supply common to 'LS362 and TMS 9900, the ϕ outputs will go low thus protecting the TMS 9900.

The frequency of the internal oscillator can be established by a quartz crystal or capacitor and LC circuit. Either a fundamental or overtone crystal may be used. The LC circuit connected to the tank inputs selects the desired crystal overtone or establishes the internal oscillator frequency when a capacitor is used instead of a crystal. An LC circuit must always be used at the tank inputs when using the internal oscillator. An external oscillator can be used, if desired, see "Applications Information" for details.

CAUTION: Power dissipation at 3 MHz requires the use of a heat sink that provides a thermal resistance from case to free air, $R_{\theta CA}$, of not more than 32°C/W.

6

typical phase relationships of inputs and outputs (OSC is internal)



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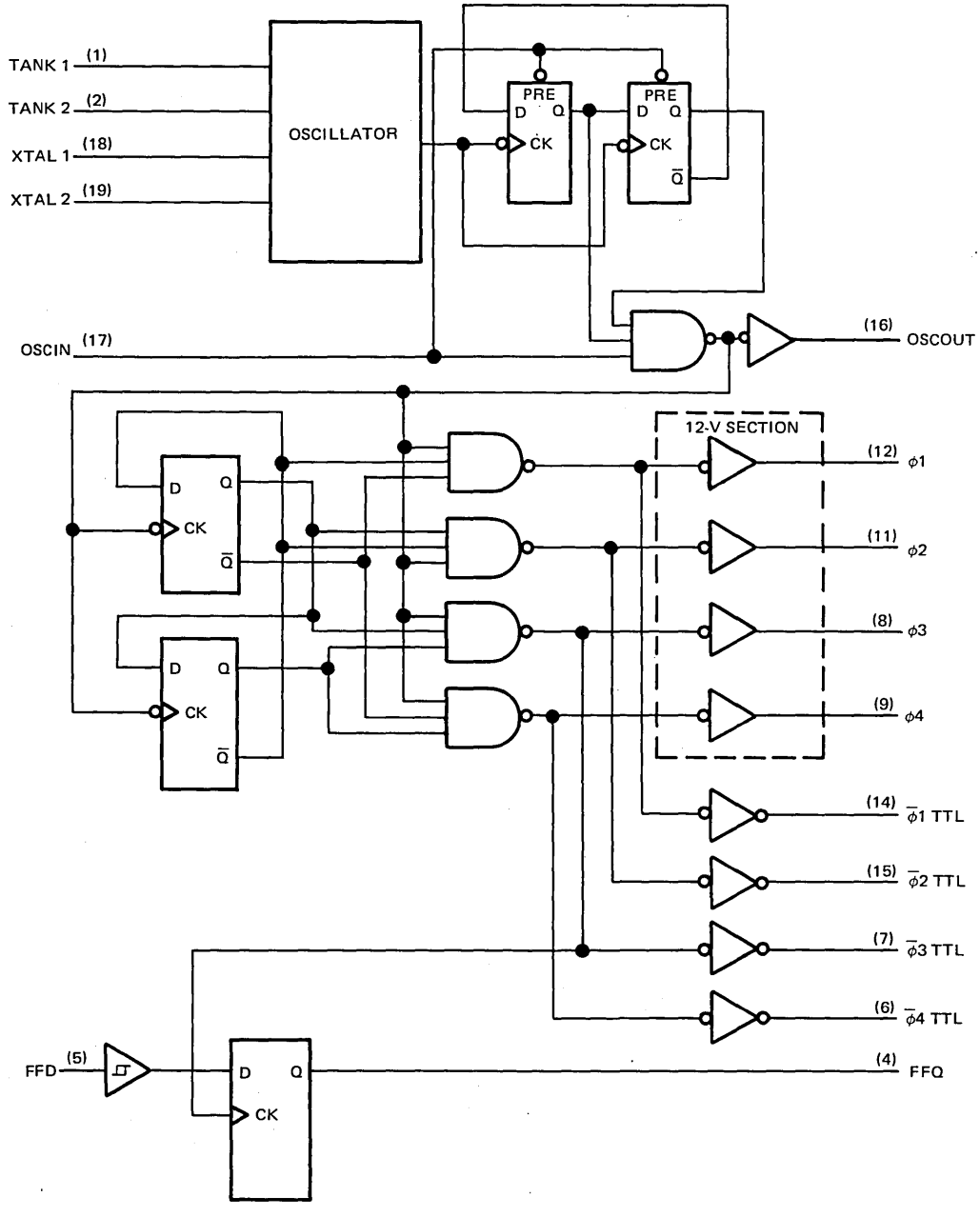
functional block diagram



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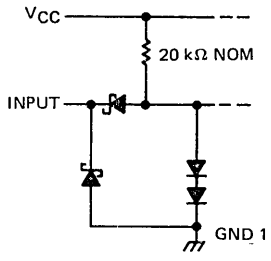
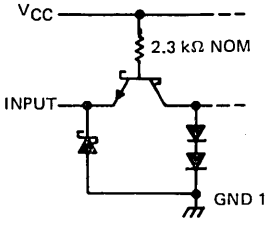
schematics of inputs and outputs

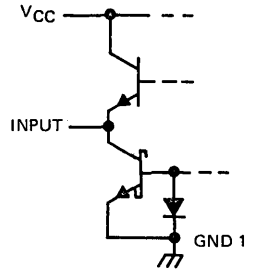
EQUIVALENT OF D INPUT



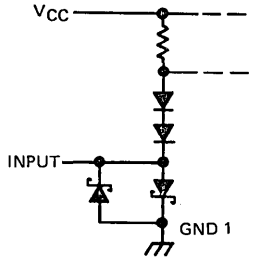
EQUIVALENT OF OSCIN INPUT



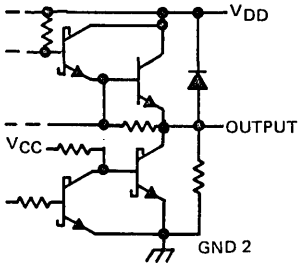
EQUIVALENT OF XTAL 1 AND XTAL 2 INPUTS



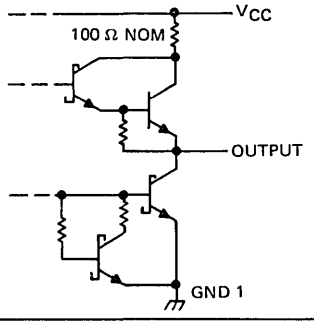
EQUIVALENT OF TANK INPUTS



TYPICAL OF $\phi1, \phi2, \phi3$ AND $\phi4$ OUTPUTS



TYPICAL OF OSCOUT, Q, AND ALL $\overline{\phi}$ TTL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage: V_{CC} (see Note 1) . . . . . 7 V
V_{DD} (see Note 1) . . . . . 13 V
Input voltage: OSCIN . . . . . 5.5 V
FFD . . . . . −0.5 V to 7 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminals connected together.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltages	V_{CC}	4.75	5	5.25	V
	V_{DD}	11.4	12	12.6	V
High-level output current, I_{OH}	$\phi1, \phi2, \phi3, \phi4$			−100	μA
	All others			−400	μA
Low-level output current, I_{OL}	$\phi1, \phi2, \phi3, \phi4$			4	mA
	All others			8	mA
Internal oscillator frequency, f_{osc}			48	54	MHz
External oscillator pulse width, $t_{w(osc)}$		25			ns
Setup time, FFD input (with respect to falling edge of $\phi3$), t_{su}		50			ns
Hold time, FFD input (with respect to falling edge of $\phi3$), t_h		−30¶			ns
Operating free-air temperature, T_A		0		70	°C

¶The algebraic convention where the more negative limit is designated minimum is used in this data sheet for time intervals only.

TYPE SN74LS362 (TIM9904)
FOUR-PHASE CLOCK GENERATOR/DRIVER

REVISED FEBRUARY 1979

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage	FFD					0.5	V
		OSCIN					0.8	
$V_{T+} - V_{T-}$	Hysteresis	FFD			0.4	0.8		V
V_{IK}	Input clamp voltage		V_{CC} = 4.75 V, V_{DD} = 11.4 V, I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	$\phi1, \phi2, \phi3, \phi4$	V_{CC} = 4.75 V,	I_{OH} = −100 μA	V_{DD}−2	V_{DD}−1.5	V_{DD}	V
		Other outputs	V_{DD} = 11.4 V to 12.6 V	I_{OH} = −400 μA	2.7	3.4		
V_{OL}	Low-level output voltage	$\phi1, \phi2, \phi3, \phi4$	V_{CC} = 4.75 V, V_{DD} = 11.4 V	I_{OL} = 4 mA		0.25	0.4	mA
		Other outputs		I_{OL} = 4 mA		0.25	0.4	
				I_{OL} = 8 mA		0.35	0.5	
I_I	Input current at maximum input voltage	FFD	V_{CC} = 5.25 V, V_{DD} = 12.6 V	V_I = 7 V			0.1	mA
		OSCIN		V_I = 5.5 V			0.3	
I_{IH}	High-level input current	FFD	V_{CC} = 5.25 V, V_{DD} = 12.6 V, V_I = 2.7 V				20	μA
		OSCIN					60	
I_{IL}	Low-level input current	FFD	V_{CC} = 5.25 V, V_{DD} = 12.6 V, V_I = 0.4 V				−0.4	mA
		OSCIN					−3.2	
I_{OS}	Short-circuit output current‡	All except $\phi1, \phi2, \phi3, \phi4$	V_{CC} = 5.25 V		−20		−100	mA
I_{CC}	Supply current from V_{CC}		V_{CC} = 5.25 V, FFD and OSCIN at GND, Outputs open			105	175	mA
I_{DD}	Supply current from V_{DD}		V_{CC} = 5.25 V, V_{DD} = 12.6 V, FFD and OSCIN at GND, Outputs open			12	20	mA

†All typical values are at V_{CC} = 5 V, V_{DD} = 12 V, T_A = 25°C.

‡Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second. Outputs $\phi1$, $\phi2$, $\phi3$, and $\phi4$ do not have short-circuit protection.

switching characteristics, T_A = 25°C, V_{CC} = 5 V, V_{DD} = 12 V, f_{osc} = 48 MHz, see figure 1

PARAMETER		TEST CONDITIONS	MIN¶	TYP	MAX	UNIT
f_{out}	Output frequency, any ϕ or $\overline{\phi}$ TTL			3		MHz
f_{out}	Output frequency, OSCOUT			12		MHz
$t_{c(\phi)}$	Cycle time, any ϕ output		330	333	340	ns
$t_{r(\phi)}$	Rise time, any ϕ output		5	9	20	ns
$t_{f(\phi)}$	Fall time, any ϕ output		10	14	20	ns
$t_{w(\phi)}$	Pulse width, any ϕ output high		40	55	70	ns
$t_{\phi1L, \phi2H}$	Delay time, $\phi1$ low to $\phi2$ high		0	5	15	ns
$t_{\phi2L, \phi3H}$	Delay time, $\phi2$ low to $\phi3$ high		0	5	15	ns
$t_{\phi3L, \phi4H}$	Delay time, $\phi3$ low to $\phi4$ high		0	5	15	ns
$t_{\phi4L, \phi1H}$	Delay time, $\phi4$ low to $\phi1$ high	Output loads:	0	5	15	ns
$t_{\phi1H, \phi2H}$	Delay time, $\phi1$ high to $\phi2$ high	$\phi1, \phi3, \phi4$: 100 pF to GND	73	83	96	ns
$t_{\phi2H, \phi3H}$	Delay time, $\phi2$ high to $\phi3$ high	$\phi2$: 200 pF to GND	73	83	96	ns
$t_{\phi3H, \phi4H}$	Delay time, $\phi3$ high to $\phi4$ high	Others: R_L = 2 kΩ,	73	83	96	ns
$t_{\phi4H, \phi1H}$	Delay time, $\phi4$ high to $\phi1$ high	C_L = 15 pF	73	83	96	ns
$t_{\phi H, \phi TL}$	Delay time, ϕ_n high to $\overline{\phi}_n$ TTL low	See Note 2	−14	−4	6	ns
$t_{\phi L, \phi TH}$	Delay time, ϕ_n low to $\overline{\phi}_n$ TTL high		−29	−19	−9	ns
$t_{\phi3L, QH}$	Delay time, $\phi3$ low to FFQ output high		−18	−8	2	ns
$t_{\phi3L, QL}$	Delay time, $\phi3$ low to FFQ output low		−19	−9	1	ns
$t_{\phi L, OSOH}$	Delay time, ϕ low to OSCOUT high		−30	−20	−10	ns
$t_{\phi H, OSOL}$	Delay time, ϕ high to OSCOUT low		−27	−17	−7	ns

NOTE 2: Use load circuit for bi-state totem-pole outputs, page 1-15.

¶The algebraic convention where the more negative limit is designated minimum is used in this data sheet for time intervals only.

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PARAMETER MEASUREMENT INFORMATION

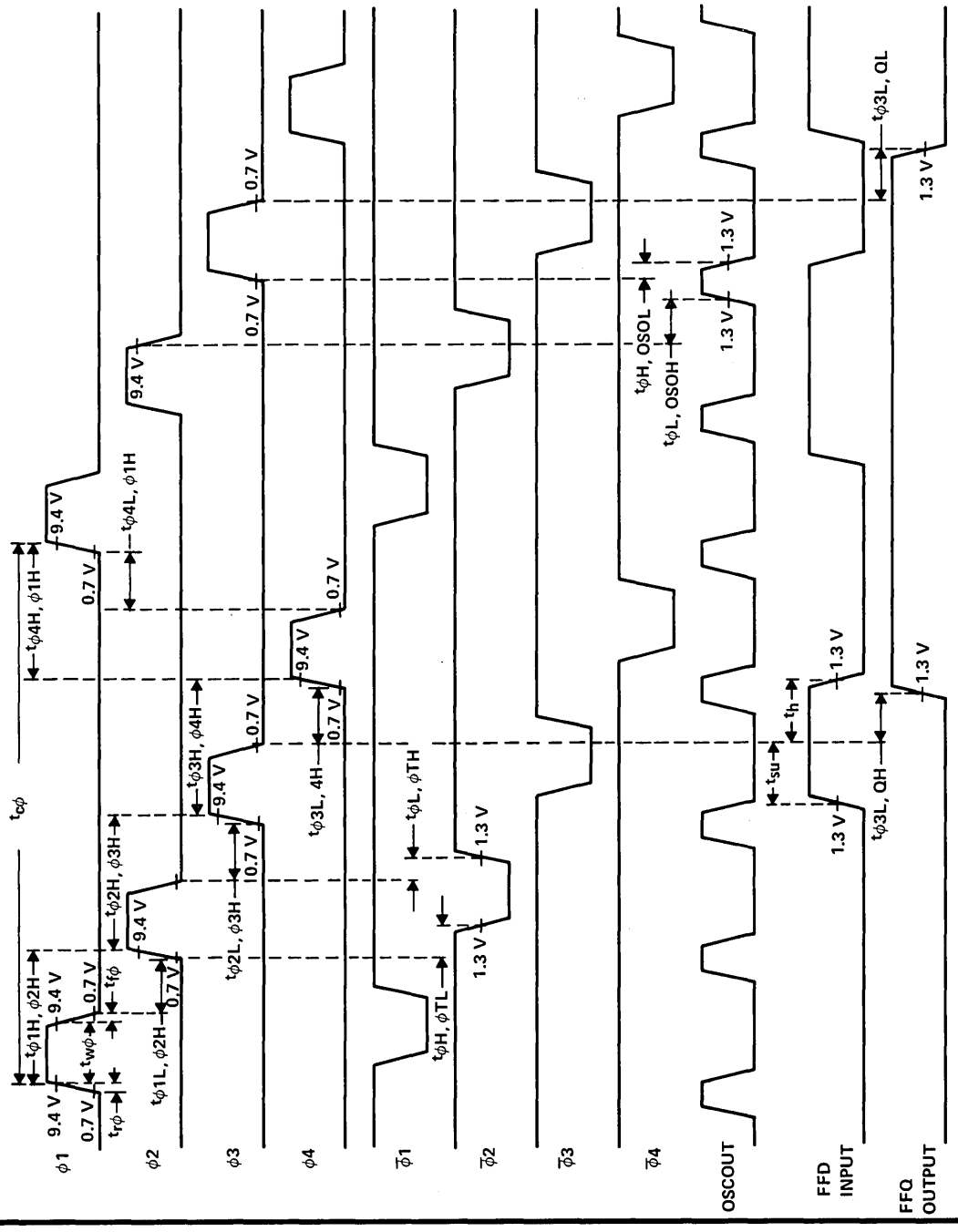

FIGURE 1–SWITCHING CHARACTERISTICS, VOLTAGE WAVEFORMS

6

APPLICATION INFORMATION

Figure 2 shows the 'LS362 connected to a TMS9900. The oscillator is shown operating with a quartz crystal and an LC circuit connected to the tank terminals.

For operation of the TMS 9900 microprocessor at 3 MHz, the frequency reference will need a resonant frequency of 48 MHz (16 x 3 MHz). A quartz crystal used as a frequency reference should be made for series-mode operation with a resistance in the 20- to 75-ohm range and be capable of a minimum of 2 mW power dissipation. Typical frequency tolerance is ±0.005%. For 48-MHz operation a third-overtone crystal is used. The inductance L connected across the tank terminals should be 0.47 μH ± 10%, and the capacitance C (including board capacity) should be 22 pF ± 5%. The LC circuit should be tuned to the third-overtone crystal frequency for best results. A 0.1-μF capacitor can be substituted for the quartz crystal. With a capacitor rather than a crystal, the LC tuned circuit establishes the operating frequencies. LC component values for operation at any frequency can be computed from $f_{osc} = 1/(2\pi\sqrt{LC})$ where f_{osc} is the oscillator frequency, L is the inductance value in henries, and C is the capacitance value in farads.

When the internal oscillator is being used, OSCIN should be connected to V_{CC} through a resistor (1 kΩ nominal) and an LC tank circuit must be connected to the tank inputs. An external oscillator can be used by connecting it to OSCIN and disabling the internal oscillator by connecting the crystal terminals to V_{CC} and leaving the tank inputs open. An external oscillator must have a frequency four times the desired output clock frequency and a 25% duty cycle. See Figure 3.

The first low-level external clock pulse will preset the divide-by-four counter, allowing the external oscillator signal to directly drive the phase generator. Figure 3 is a timing diagram illustrating operation with an external oscillator.

Resistors between $\phi1$, $\phi2$, $\phi3$, and $\phi4$ outputs of the 'LS362 and the corresponding clock input terminals of the TMS 9900 should be in the 10- to 20-ohm range (See Figure 2). Their purpose is to minimize overshoot and undershoot. The required resistance value is dependent on circuit layout. Clock signal interconnections should be as short as possible.

The D-type flip-flop associated with pins FFD and FFQ can be used to provide a power-on reset and a manual reset to the TMS 9900 as shown in Figure 4. A Schmitt-trigger circuit driving the D input generates a fast-rising waveform when the input voltage rises to a specific value. At power turn-on, voltage across the 0.1 μF capacitor in Figure 4 will rise towards V_{CC}. This circuit provides a delay that resets the TMS 9900 after V_{CC} has stabilized. An optional manual reset switch can be connected to the delay circuit for resetting the TMS 9900 at any time. The TMS 9900 HOLD signal could alternately be actuated by FFD.

The ground terminals GND1 and GND2 should be connected together and to system ground.

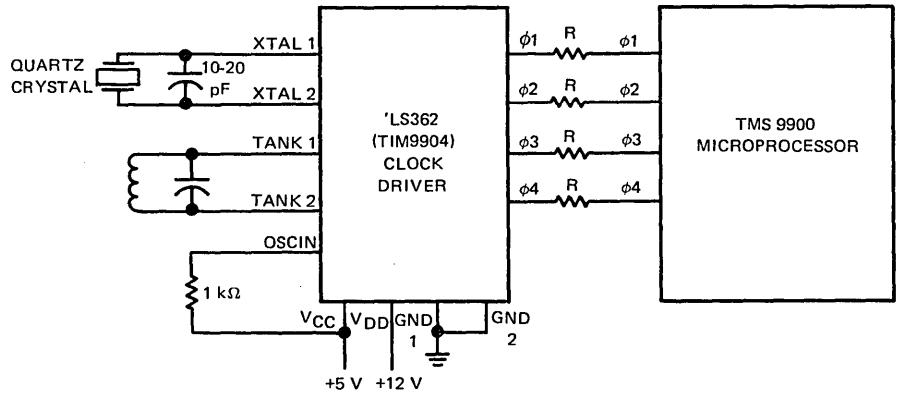

FIGURE 2–'LS362 CRYSTAL-CONTROLLED OPERATION

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APPLICATION INFORMATION

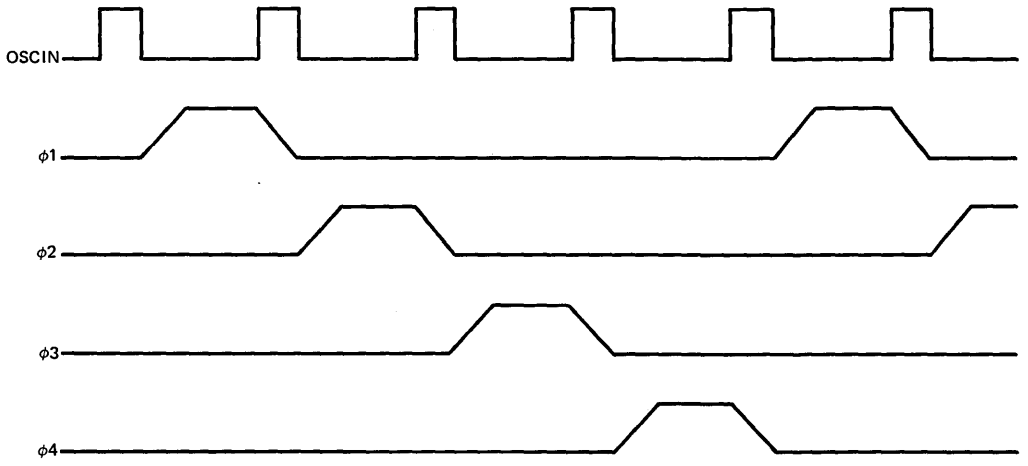


FIGURE 3–EXTERNAL OSCILLATOR TIMING

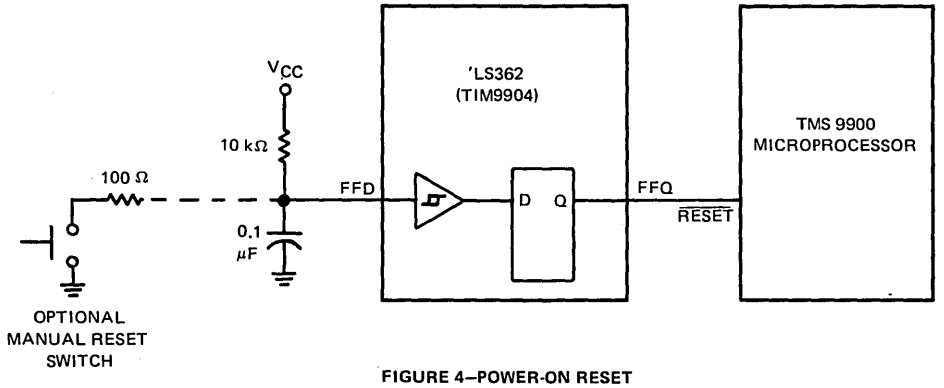


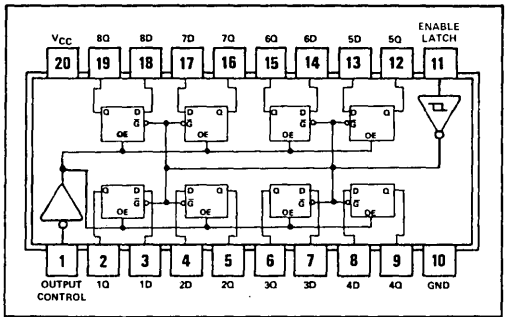
FIGURE 4–POWER-ON RESET

TYPES SN54LS373, SN54LS374, SN54S373, SN54S374, SN74LS373, SN74LS374, SN74S373, SN74S374 OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS

BULLETIN NO. DL-S 12350, OCTOBER 1975 – REVISED JUNE 1979

- Choice of 8 Latches or 8 D-Type Flip-Flops In a Single Package
- 3-State Bus-Driving Outputs
- Full Parallel-Access for Loading
- Buffered Control Inputs
- Clock/Enable Input Has Hysteresis to Improve Noise Rejection
- P-N-P Inputs Reduce D-C Loading on Data Lines ('S373 and 'S374)
- SN54LS363 and SN74LS364 Are Similar But Have Higher V_{OH} For MOS Interface

SN54LS373, SN54S373 . . . J PACKAGE
SN74LS373, SN74S373 . . . J OR N PACKAGE
(TOP VIEW)

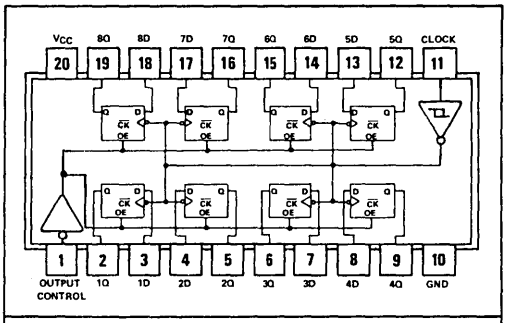


logic: see function table

'LS373, 'S373
FUNCTION TABLE

OUTPUT ENABLE	ENABLE LATCH	D	OUTPUT
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

SN54LS374, SN54S374 . . . J PACKAGE
SN74LS374, SN74S374 . . . J OR N PACKAGE
(TOP VIEW)



logic: see function table

'LS374, 'S374
FUNCTION TABLE

OUTPUT ENABLE	CLOCK	D	OUTPUT
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

See explanation of function tables on page 1-13.

6

description

These 8-bit registers feature totem-pole three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the 'LS373 and 'S373 are transparent D-type latches meaning that while the enable (G) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data that was set up.

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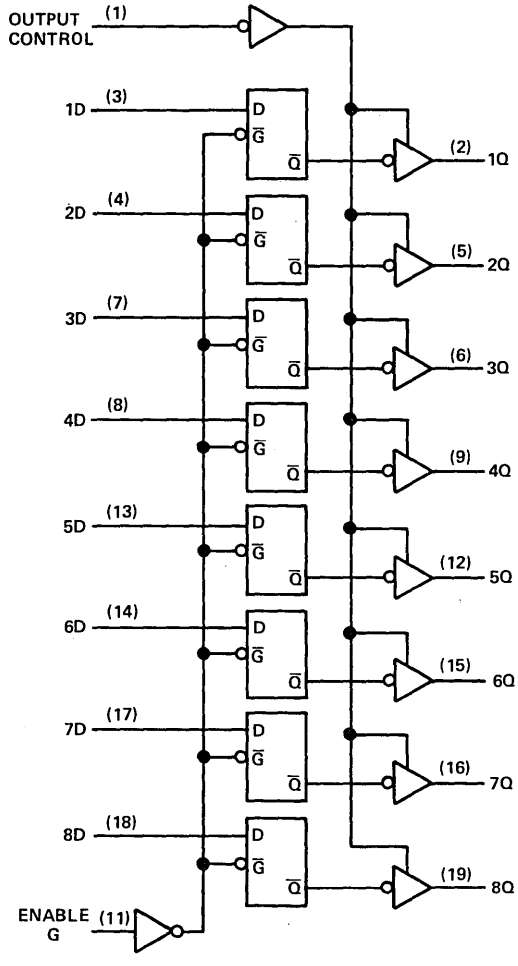
description (continued)

The eight flip-flops of the 'LS374 and 'S374 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the logic states that were setup at the D inputs.

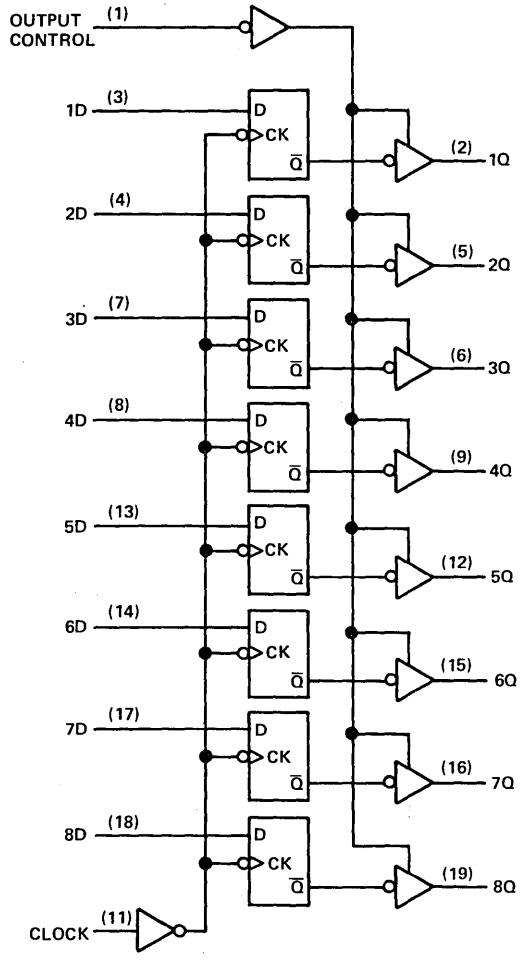
Schmitt-trigger buffered inputs at the enable/clock lines simplify system design as ac and dc noise rejection is improved by typically 400 mV due to the input hysteresis. A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the latches or flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

'LS373, 'S373
TRANSPARENT LATCHES



'LS374, 'S374
POSITIVE-EDGE-TRIGGERED FLIP-FLOPS



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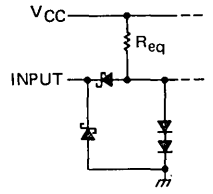
schematic of inputs and outputs

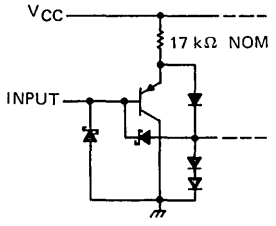
'LS373

EQUIVALENT OF DATA AND OUTPUT CONTROL INPUTS

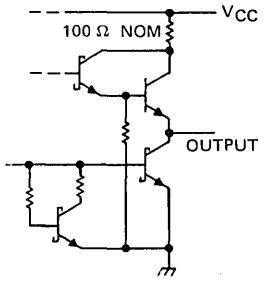


Data: R_{eq} = 20 kΩ NOM
Output control: R_{eq} = 18 kΩ NOM

EQUIVALENT OF ENABLE INPUT

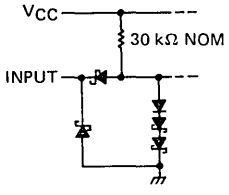


TYPICAL OF ALL OUTPUTS

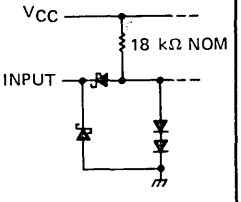


'LS374

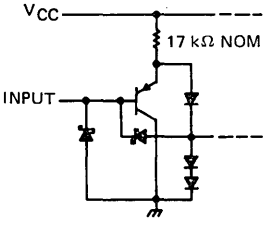
EQUIVALENT OF DATA INPUTS



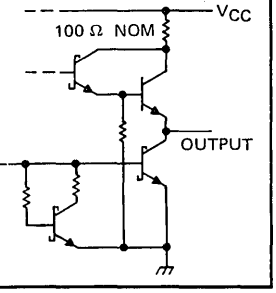
EQUIVALENT OF OUTPUT CONTROL INPUT



EQUIVALENT OF CLOCK INPUT



TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54LS' . . . . . −55°C to 125°C
SN74LS' . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}				5.5			5.5	V
High-level output current, I_{OH}				−1			−2.6	mA
Width of clock/enable pulse, t_w	High	15			15			ns
	Low	15			15			
Data setup time, t_{su}	'LS373	0↓			0↓			ns
	'LS374	20↑			20↑			
Data hold time, t_h	'LS373	10↓			10↓			ns
	'LS374	0↑			0↑			
Operating free-air temperature, T_A		−55		125	0		70	°C

↑↓ The arrow indicates the transition of the clock/enable input used for reference: ↑ for the low-to-high transition, ↓ for the high-to-low transition.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS' MIN	SN54LS' TYP‡	SN54LS' MAX	SN74LS' MIN	SN74LS' TYP‡	SN74LS' MAX	UNIT
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max, I_{OH} = MAX		2.4	3.4		2.4	3.1		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_O = 2.7 V				20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_O = 0.4 V				−20			−20	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−30		−130	−30		−130	mA
I_{CC}	Supply current	V_{CC} = MAX, Output control at 4.5 V	'LS373		24	40		24	40	mA
			'LS374		27	40		27	40	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS373 MIN	'LS373 TYP	'LS373 MAX	'LS374 MIN	'LS374 TYP	'LS374 MAX	UNIT
f_{max}			C_L = 45 pF, R_L = 667 Ω, See Notes 2 and 3				35	50		MHz
t_{PLH}	Data	Any Q			12	18				ns
t_{PHL}					12	18				
t_{PLH}	Clock or enable	Any Q			20	30		15	28	ns
t_{PHL}					18	30		19	28	
t_{PZH}	Output Control	Any Q			15	28		20	28	ns
t_{PZL}					25	36		21	28	
t_{PHZ}	Output Control	Any Q	C_L = 5 pF, R_L = 667 Ω, See Note 3		12	20		12	20	ns
t_{PLZ}					15	25		14	25	

NOTES: 2. Maximum clock frequency is tested with all outputs loaded.
3. See load circuits and waveforms on page 1-15.

f_{max} ≡ maximum clock frequency
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
t_{PHZ} ≡ output disable time from high level
t_{PLZ} ≡ output disable time from low level

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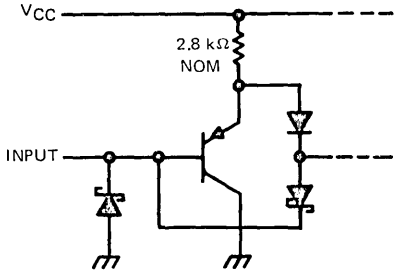
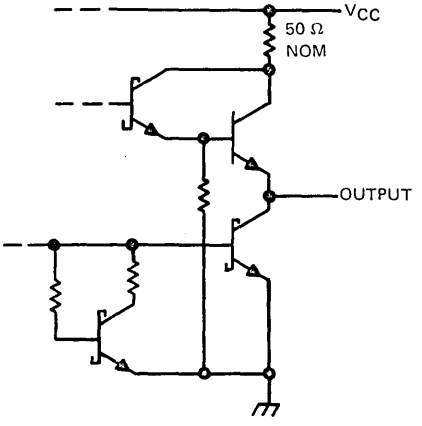
schematic of inputs and outputs

EQUIVALENT OF EACH INPUT



TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54S' . . . . . −55°C to 125°C
SN74S' . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54S'			SN74S'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}				5.5			5.5	V
High-level output current, I_{OH}				−2			−6.5	mA
Width of clock/enable pulse, t_w	High	6			6			ns
	Low	7.3			7.3			
Data setup time, t_{su}	'S373	0↓			0↓			ns
	'S374	5↑			5↑			
Data hold time, t_h	'S373	10↓			10↓			ns
	'S374	2↑			2↑			
Operating free-air temperature, T_A		−55		125	0		70	°C

↑↓ The arrow indicates the transition of the clock/enable input used for reference: ↑ for the low-to-high transition, ↓ for the high-to-low transition.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.2	V
V_{OH}	High-level output voltage	SN54S'	V_{CC} = MIN,	V_{IH} = 2 V,	2.4	3.4		V
		SN74S'	V_{IL} = 0.8 V,	I_{OH} = MAX	2.4	3.1		
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 20 mA			0.5	V
I_{OZH}	Off-state output current, high-level voltage applied		V_{CC} = MAX, V_O = 2.4 V	V_{IH} = 2 V,			50	μA
I_{OZL}	Off-state output current, low-level voltage applied		V_{CC} = MAX, V_O = 0.5 V	V_{IH} = 2 V,			−50	μA
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7 V			50	μA
I_{IL}	Low-level input current		V_{CC} = MAX,	V_I = 0.5 V			−250	μA
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−40		−100	mA
I_{CC}	Supply current		V_{CC} = MAX	'S373		105	160	mA
				'S374		90	140	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'S373			'S374			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}			C_L = 15 pF, R_L = 280 Ω, See Notes 2 and 4				75	100		MHz
t_{PLH}	Data	Any Q			7	12				ns
t_{PHL}					7	12				
t_{PLH}	Clock or enable	Any Q			7	14		8	15	ns
t_{PHL}					12	18		11	17	
t_{PZH}	Output Control	Any Q			8	15		8	15	ns
t_{PZL}					11	18		11	18	
t_{PHZ}	Output Control	Any Q	C_L = 5 pF, R_L = 280 Ω, See Note 3		6	9		5	9	ns
t_{PLZ}					8	12		7	12	

NOTES: 2. Maximum clock frequency is tested with all outputs loaded.
4. See load circuits and waveforms on page 1-14.

f_{max} ≡ maximum clock frequency
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
t_{PHZ} ≡ output disable time from high level
t_{PLZ} ≡ output disable time from low level

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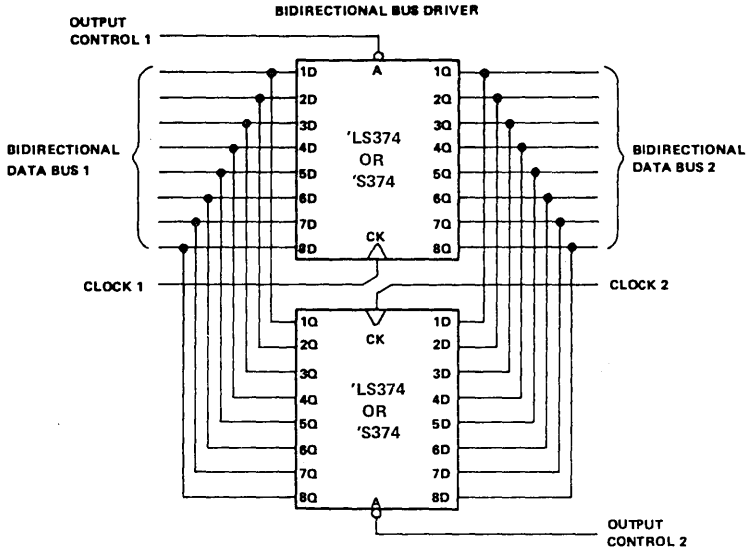
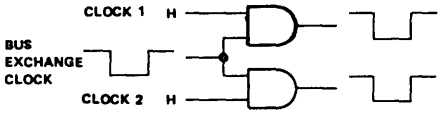
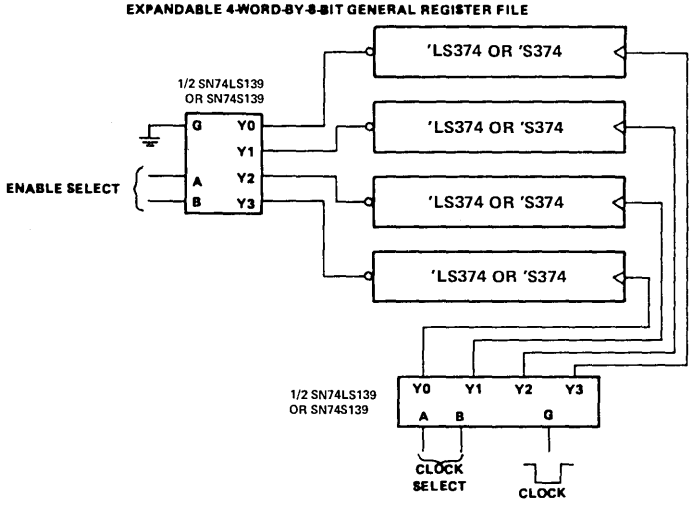
TYPICAL APPLICATION DATA





CLOCK CIRCUIT FOR BUS EXCHANGE



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TEXAS INSTRUMENTS
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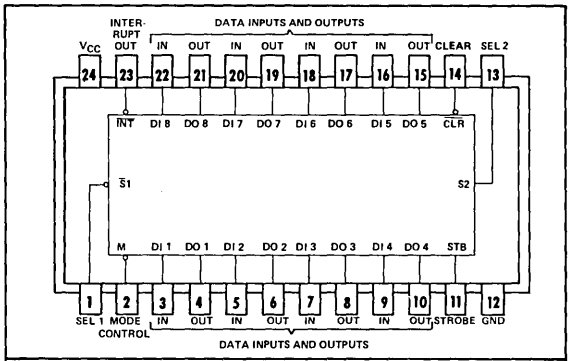
TYPES SN54S412, SN74S412 (TIM8212)
MULTI-MODE BUFFERED LATCHES

BULLETIN NO. DL-S 12351, OCTOBER 1975

- P-N-P Inputs and 3-State Outputs Maximize I/O and Data Bus Capabilities
- Data Latch Transparency Permits Asynchronous or Latched Receiver Modes
- Mode and Select Inputs Permit Storing With Outputs Enabled or Disabled
- Strobe-Controlled Flag Flip-Flop Indicates Status or Interrupt
- Asynchronous Clear Sets All Eight Data Lines Low and Initializes Status Flag
- High-Level Output Voltage, Typically 4 V, Drives Most MOS Functions Directly
- Direct Replacement for Intel 3212 or 8212

SN54S412 . . . J PACKAGE
SN74S412 . . . J OR N PACKAGE
(TOP VIEW)



logic: see function table

description

This high-performance eight-bit parallel expandable buffer register incorporates package and mode selection inputs and an edge-triggered status flip-flop designed specifically for implementing bus-organized input/output ports. The three-state data outputs can be connected to a common data bus and controlled from the appropriate select inputs to receive or transmit data. An integral status flip-flop provides package busy or request interrupt commands. The outputs, with a 4-volt typical high-level voltage, are compatible for driving low-threshold MOS directly.

DATA LATCHES

The eight data latches are fully transparent when the internal gate enable, G, input is high and the outputs are enabled (OE = H). Latch transparency is selected by the mode control (M), select ($\overline{S1}$ and S2), and the strobe (STB) inputs and during transparency each data output (DO_i) follows its respective data input (DI_i). This mode of operation can be terminated by clearing, de-selecting, or holding the data latches. See data latches function table.

MODE SELECTION

An input mode or an output mode is selectable from this single input line. In the input mode, MD = L, the eight data latch inputs are enabled when the strobe is high regardless of device selection. If selected during an input mode, the outputs will follow the data inputs. When the strobe input is taken low, the latches will store the most-recently setup data.

In the output mode, M = H, the output buffers are enabled regardless of any other control input. During the output mode the content of the register is under control of the select ($\overline{S1}$ and S2) inputs. See data latches function table.

STATUS FLIP-FLOP

The status flip-flop provides a low-level output signal when:

a. the package is selected

b. a strobe input is received.

This status signal can be used to indicate that the register is busy or to initiate an interrupt type command.

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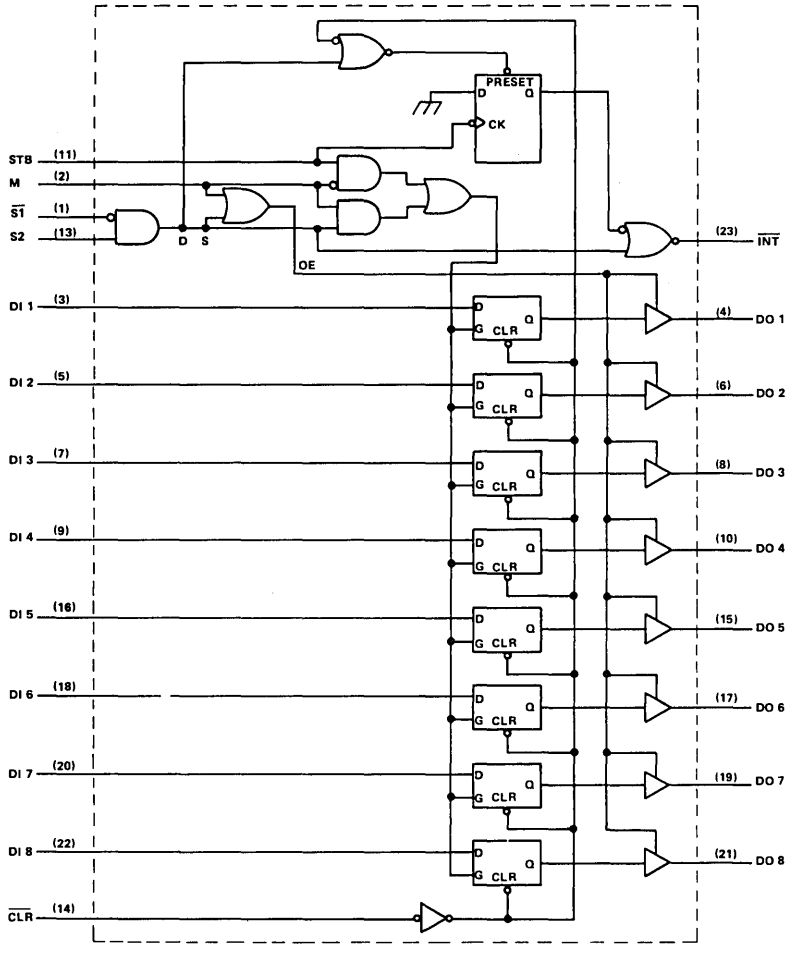
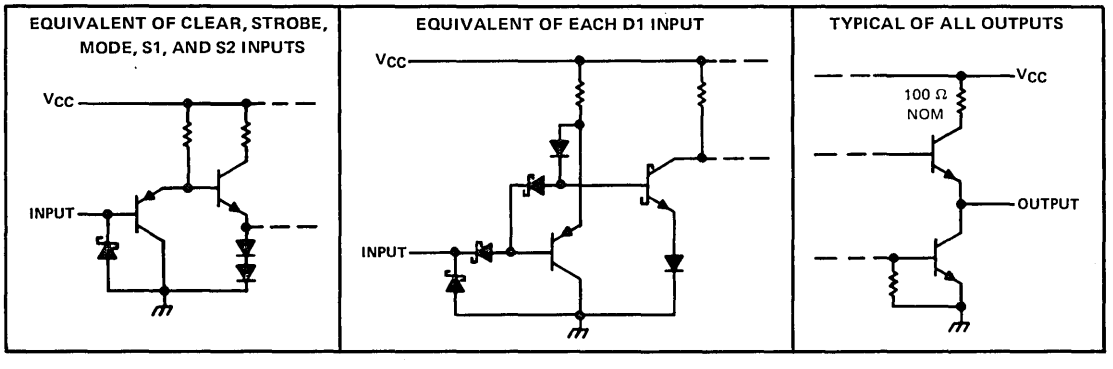
functional block diagram



schematics of inputs and outputs



DATA LATCHES FUNCTION TABLE

FUNCTION	CLEAR	M	$\overline{S1}$	S2	STB	DATA IN	DATA OUT
Clear	L	H	H	X	X	X	L
	L	L	L	H	L	X	L
De-select	X	L	X	L	X	X	Z
	X	L	H	X	X	X	Z
Hold	H	H	H	L	X	X	Q_O
	H	L	L	H	L	X	Q_O
Data Bus	H	H	L	H	X	L	L
	H	H	L	H	X	H	H
Data Bus	H	L	L	H	H	L	L
	H	L	L	H	H	H	H

STATUS FLIP-FLOP FUNCTION TABLE

CLEAR	$\overline{S1}$	S2	STB	$\overline{INT}$
L	H	X	X	H
L	X	L	X	H
H	X	X	↓	L
H	L	H	X	L

H ≡ high level (steady state)
L ≡ low level (steady state)
X ≡ irrelevant (any input, including transitions)
Z ≡ high impedance (off)
↓ ≡ transition from low to high level

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54S412 . . . . . −55°C to 125°C
SN74S412 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54S412			SN74S412			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Pulse width, t_w (see Figures 1, 2, and 4)	STB or $\overline{S1} \cdot S2$	25			25			ns
	Clear low	25			25			
Setup time, t_{su} (see Figure 3)		15↓			15↓			ns
Hold time, t_h (see Figures 1 and 3)		20↓			20↓			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

↓ The arrow indicates that the falling edge of the clock pulse is used for reference.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54S412 MIN	SN54S412 TYP‡	SN54S412 MAX	SN74S412 MIN	SN74S412 TYP‡	SN74S412 MAX	UNIT
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.85			0.85	V
V_{IK}	Input clamp voltage		V_{CC} = MIN;	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = −1 mA	3.4	4		3.65	4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	I_{OL} = 15 mA			0.45			0.45	V
				I_{OL} = 20 mA			0.5			0.5	
I_{OZH}	Off-state output current, high-level voltage applied	DO 1 thru DO 8	V_{CC} = MAX,	V_O = 2.4 V			50			50	μA
I_{OZL}	Off-state output current, low-level voltage applied	DO 1 thru DO 8	V_{CC} = MAX,	V_O = 0.5 V			−50			−50	μA
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 5.25 V			20			10	μA
I_{IL}	Low-level input current	$\overline{S1}$	V_{CC} = MAX,	V_I = 0.4 V			−1			−1	mA
		M					−0.75			−0.75	
		All others					−0.25			−0.25	
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−20		−65	−20		−65	mA
I_{CC}	Supply current		V_{CC} = MAX,	see Note 2		82			82	130	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

NOTE 2: I_{CC} is measured with all outputs open, clear input at 4.5 V, and all other inputs grounded.

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switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM	TO	FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	STB, $\overline{S1}$, or S2	Any DO	1	C_L = 30 pF, See Note 3		18	27	ns
t_{PHL}						15	25	
t_{PHL}	$\overline{CLR}$	Any DO	2			18	27	ns
t_{PLH}	DI_i	DO_i	3			12	20	ns
t_{PHL}						10	20	
t_{PLH}	$\overline{S1}$ or S2	$\overline{INT}$	4	C_L = 30 pF, See Note 3		12	20	ns
t_{PHL}	STB	$\overline{INT}$	4			16	25	
t_{PZH}	$\overline{S1}$, S2, or M	Any DO	5	C_L = 30 pF, See Note 3		21	35	ns
t_{PZL}						25	40	
t_{PHZ}	$\overline{S1}$, S2, or M	Any DO	5	C_L = 5 pF, See Note 3		9	20	ns
t_{PLZ}						12	20	

t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
t_{PHZ} ≡ output disable time from high level
t_{PLZ} ≡ output disable time from low level
NOTE 3: Load circuit and voltage waveforms are shown on page 1-14.

PARAMETER MEASUREMENT INFORMATION

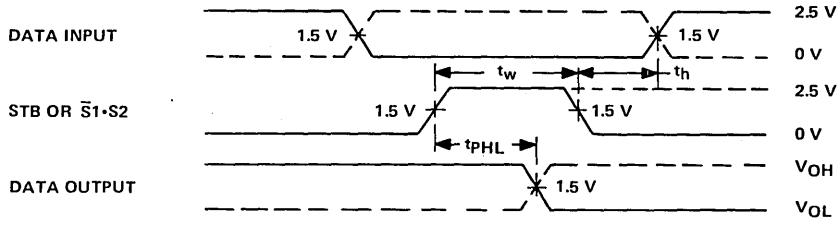

FIGURE 1 – STROBE OR SELECT TO DATA OUTPUT

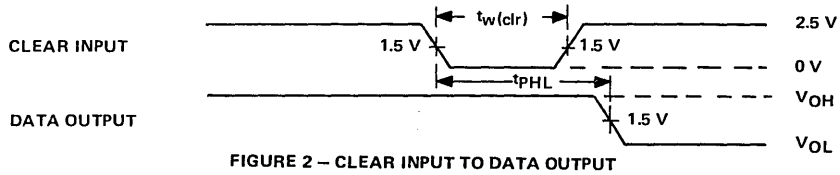

FIGURE 2 – CLEAR INPUT TO DATA OUTPUT

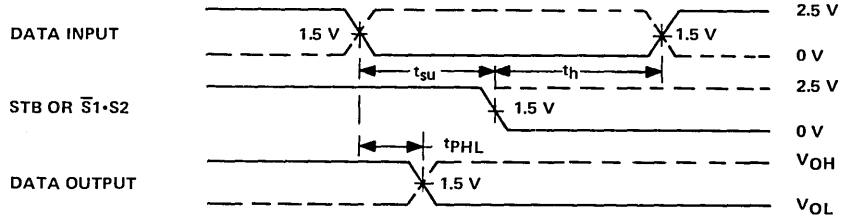

FIGURE 3 – DATA INPUT TO DATA OUTPUT

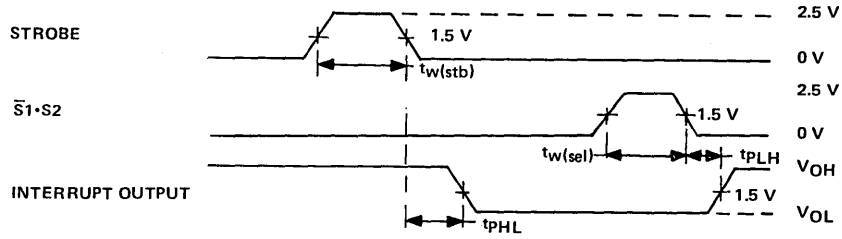

FIGURE 4 – STROBE OR SELECT TO INTERRUPT OUTPUT

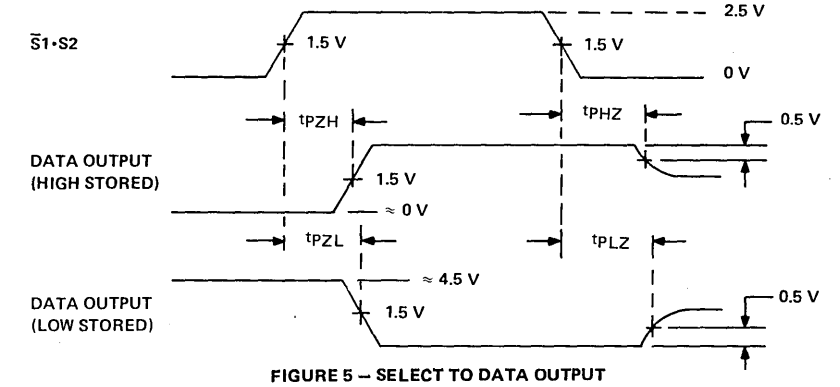

FIGURE 5 – SELECT TO DATA OUTPUT

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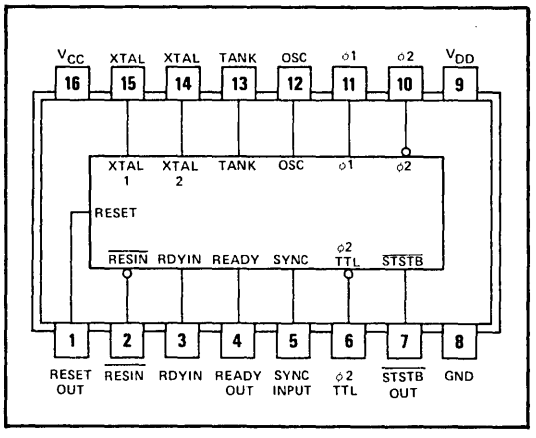
TYPE SN74LS424 (TIM8224)
TWO-PHASE CLOCK GENERATOR/DRIVER

BULLETIN NO. DL-S 12475, OCTOBER 1976–REVISED AUGUST 1977

- Designed to be Interchangeable With Intel 8224
- Single-Chip Clock Driver With Self-Contained Oscillator
- Specifically Designed to Drive All 8080A Microprocessors

J OR N PACKAGE
(TOP VIEW)



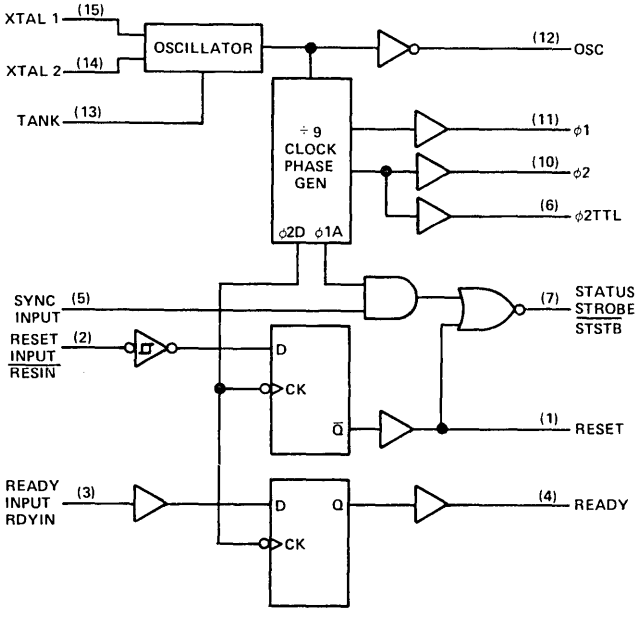
description

This clock generator is capable of driving 12-volt lines. It contains a crystal-controlled oscillator, a divide-by-nine clock phase generator, two high-level drivers, and auxiliary circuitry.

The internal oscillator is designed to operate with fundamental-mode crystals, or with overtone-mode crystals when using a parallel-tuned circuit connected to the tank terminal, pin 13. The oscillator output appears on pin 12 and drives the divide-by-nine counter. The ÷9 clock phase generator output consists of phases $\phi 2$ for driving MOS inputs and $\phi 2$ TTL for driving TTL. Three other TTL outputs, status strobe, reset, and ready, are coupled to the divide-by-nine counter. A sync input from the 8080A is AND'ed with $\phi 1A$ to produce the status strobe. The power-on reset also generates the status strobe signal through an output NOR gate. The reset input works on a voltage-level basis by use of a Schmitt trigger. A rising voltage waveform is triggered at a particular voltage. A synchronized ready output is obtained by clocking with a $\phi 2$ signal.

The SN74LS424 is characterized for operation over the temperature range of 0°C to 70°C.

functional block diagram



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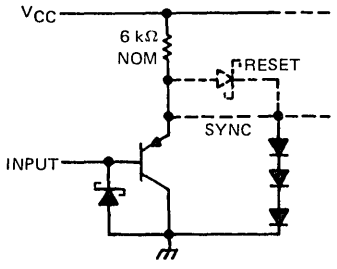
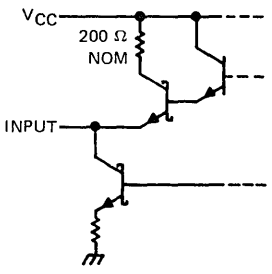
schematics of inputs and outputs

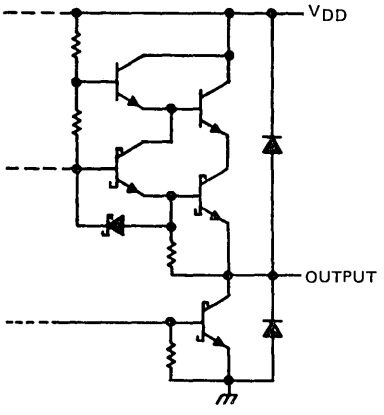
EQUIVALENT OF RESET AND SYNC INPUTS



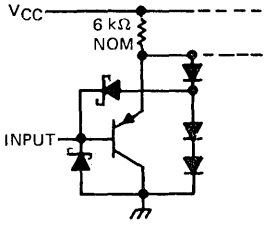
EQUIVALENT OF XTAL 1 AND XTAL 2 NODES



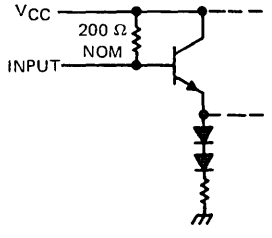
TYPICAL OF $\phi1$, $\phi2$ OUTPUTS



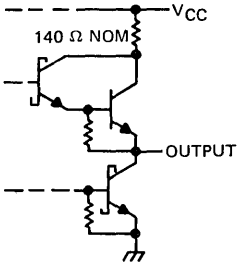
EQUIVALENT OF READY INPUT



EQUIVALENT OF TANK INPUT



TYPICAL OF ALL OUTPUTS EXCEPT $\phi1$, $\phi2$



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Supply voltage, V_{DD}	17 V
Input voltages (sync, reset, ready)	7 V
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

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recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Supply voltage, V_{DD}	11.4	12	12.6	V
Ready input setup time, $t_{su(RDYIN)}$	$50 - \frac{4t_c}{9}$			ns
Ready input hold time, $t_{h(RDYIN)}$	$\frac{4t_c}{9}$			ns
Operating free-air temperature range, T_A	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage	Reset input			2.6			V
		All others			2			
V_{IL}	Low-level input voltage						0.8	V
$V_{T+} - V_{T-}$	Hysteresis	Reset input			0.25			V
V_{IK}	Input clamp voltage		V_{CC} = 4.75 V, V_{DD} = 11.4 V	I_I = −5 mA			−1	V
				I_I = −18 mA			−1.5	
V_{OH}	High-level output voltage	$\phi1, \phi2$	V_{CC} = 4.75 V, V_{DD} = 11.6 V	I_{OH} = −100 μA	9.4	10.4		V
		Ready, reset			3.6	3.9		
		Others		I_{OH} = −1 mA	2.4	3.1		
V_{OL}	Low-level output voltage	$\phi1, \phi2$, reset, status strobe	V_{CC} = 4.75 V, V_{DD} = 11.4 V	I_{OL} = 2.5 mA		0.2	0.45	V
		$\phi2$ TTL, osc		I_{OL} = 15 mA		0.25	0.45	
I_I	Input current at maximum input voltage		V_{CC} = 5.25 V, V_{DD} = 12.6 V, V_I = 7 V				100	μA
I_{IH}	High-level input current		V_{CC} = 5.25 V, V_{DD} = 12.6 V, V_I = 5.25 V				10	μA
I_{IL}	Low-level input current		V_{CC} = 5.25 V, V_{DD} = 12.6 V, V_I = 0.4 V				−0.25	mA
I_{OS}	Short-circuit circuit current§	All except $\phi1, \phi2$	V_{CC} = 5 V, V_{DD} = 12 V		−10		−60	mA
I_{CC}	Supply current from V_{CC}		V_{CC} = 5.25 V, V_{DD} = 12 V			70	115	mA
I_{DD}	Supply current from V_{DD}		V_{DD} = 12.6 V, V_{CC} = 5 V,	See Note 2		6	12	mA
C_i	Input capacitance		V_{CC} = 5 V, V_{DD} = 12 V, V_I = 2.5 V, f = 1 MHz,	See Note 2			8	pF

‡All typical values are at V_{CC} = 5 V, V_{DD} = 12 V, T_A = 25°C.
§Not more than one output should be shorted at a time. $\phi1$ and $\phi2$ do not have short-circuit protection.
NOTE 2: I_{CC} and I_{DD} are measured with outputs disabled and open.

switching characteristics, V_{CC} = 5 V, V_{DD} = 12 V, T_A = 25°C, see figure 1

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum oscillator frequency		27			MHz
$t_{c(osc)}$	Oscillator cycle time			$\frac{t_c}{9}$ †		ns
$t_{w(\phi1)}$	Pulse width, $\phi1$ high	$\phi1$ and $\phi2$: C_L = 20 pF to 110 pF, See Figure 2	$\frac{2t_c}{9} - 20$			ns
$t_{w(\phi2)}$	Pulse width, $\phi2$ high		$\frac{5t_c}{9} - 35$			ns
$t_{w(SS)}$	Pulse width, status strobe low		$\frac{t_c}{9} - 15$			ns
$t_{r(\phi)}$	Rise time, clock outputs	$\phi2$ TTL: C_L = 30 pF, $R1$ = 300 Ω, $R2$ = 600 Ω, See Figure 3			20	ns
$t_{f(\phi)}$	Fall time, clock outputs				20	ns
$t_{\phi1L,\phi2H}$	Delay time, $\phi1$ low to $\phi2$ high		0			ns
$t_{\phi2L,\phi1H}$	Delay time, $\phi2$ low to $\phi1$ high	Status Strobe: C_L = 15 pF, $R1$ = 2 kΩ, $R2$ = 4 kΩ, See Figure 3	$\frac{2t_c}{9} - 30$			ns
$t_{\phi1H,\phi2H}$	Delay time, $\phi1$ high to $\phi2$ high		$\frac{2t_c}{9}$		$\frac{2t_c}{9} + 20$	ns
$t_{\phi2,\phi2T}$	Delay time, $\phi2$ to $\phi2$ TTL	OSC, Ready, Reset: C_L = 10 pF, $R1$ = 2 kΩ, $R2$ = 4 kΩ, See Figure 3	−5		15	ns
$t_{\phi2H,SSL}$	Delay time, $\phi2$ high to status strobe low		$\frac{6t_c}{9} - 50$		$\frac{6t_c}{9}$	ns
$t_{RV,\phi2L}$	Delay time, ready or reset output valid to phase 2 low		$\frac{4t_c}{9} - 25$			ns

† $t_c \equiv t_{c(\phi1)} = t_{c(\phi2)}$

EXAMPLE: switching times for f_{osc} = 20 MHz ($t_{c(\phi1)} = t_{c(\phi2)}$ = 450 ns)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{osc}	Oscillator frequency	Same as above		20		MHz
$t_{c(osc)}$	Oscillator cycle time			50		ns
$t_{w(\phi1)}$	Pulse width, $\phi1$ high		80			ns
$t_{w(\phi2)}$	Pulse width, $\phi2$ high		215			ns
$t_{w(SS)}$	Pulse width, status strobe		35			ns
$t_{\phi1L,\phi2H}$	Delay time, $\phi1$ low to $\phi2$ high		0			ns
$t_{\phi2L,\phi1H}$	Delay time, $\phi2$ low to $\phi1$ high		70			ns
$t_{\phi1H,\phi2H}$	Delay time, $\phi1$ high to $\phi2$ high		100		120	ns
$t_{\phi2H,SSL}$	Delay time, $\phi2$ high to status strobe low		250		300	ns
$t_{RV,\phi2L}$	Delay time, ready or reset output valid to $\phi2$ low		175			ns

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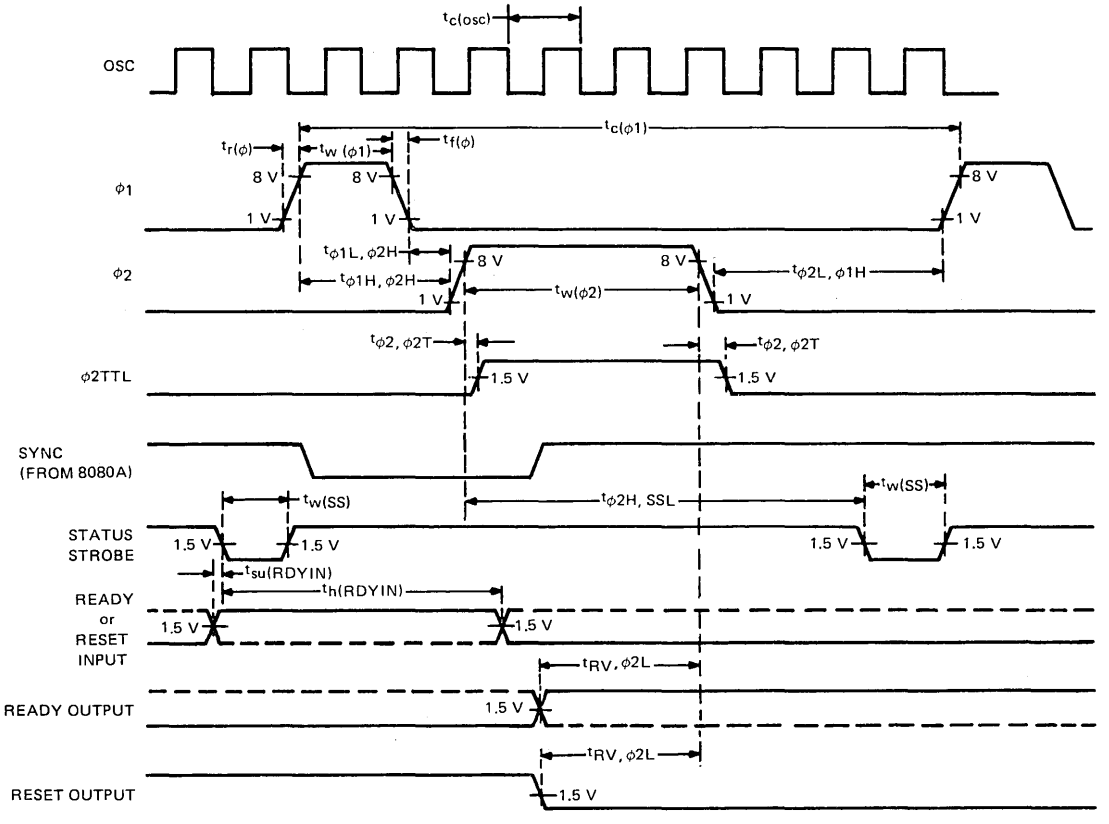
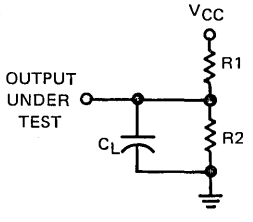
PARAMETER MEASUREMENT INFORMATION



NOTE: Transistion times, pulse widths, and interpulse relationships are distorted in this diagram in order to define various intervals, See Figure 5 for correct relative relationships.

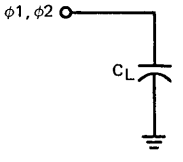
VOLTAGE WAVEFORMS

FIGURE 1



LOAD CIRCUIT

FIGURE 2



LOAD CIRCUIT

FIGURE 3

TYPICAL APPLICATION DATA

The 'LS424 is a single-chip clock generator/driver for 8080A CPU's, furnishing three clocks ($\phi1$, $\phi2$ and $\phi2$ TTL), status strobe, reset, and ready signals. The 'LS424 contains a crystal-controlled oscillator, a divide-by-nine counter, two high-level drivers, and several auxiliary logic functions. Figure 4 is a functional block diagram of the SN74LS424. Figure 5 shows the relationship between $\phi1$, $\phi2$, and the oscillator frequency period.

oscillator

A high order of clock frequency stability is provided by use of an external quartz crystal to set the oscillator frequency which is nine times the operating frequency of the 8080A. The quartz crystal is operated in a series-resonant mode. A fundamental-mode crystal requires no auxiliary circuitry, but an overtone-mode crystal requires an ac-coupled parallel-resonant circuit to be connected to the tank connection (pin 13). The parallel-resonant circuit, tuned to the oscillator frequency, compensates for the lower Q of the overtone-mode crystal. The required size of the circuit components can be calculated from $f = 1/2\pi\sqrt{LC}$ where f is the oscillator frequency, L is inductance value, and C is capacitance value. Figure 6 shows an ac-coupled parallel-tuned circuit used with the SN74LS424.

clock phase generator

The divide-by-nine clock phase generator contains a divide-by-nine counter, logic required to shape the clock pulses as shown under parameter measurement information, gates and flip-flops to generate auxiliary signals, and output drivers. The divide-by-nine counter waveforms are combined with gates to form a $\phi1$ pulse with a width of two periods of the oscillator frequency, repeating at intervals of nine oscillator periods. Similarly, the $\phi2$ pulse, having a width of five oscillator frequency periods, is formed lagging the $\phi1$ pulse by two oscillator periods.

$\phi1$ and $\phi2$ outputs are provided by high-level drivers for direct connection to the 8080A CPU. $\phi2$ TTL is derived in a manner similar to $\phi1$ and $\phi2$, but the output driver output is at TTL voltage levels. The $\phi2$ TTL pulse width is the same as $\phi2$. A $\phi2$ TTL application is clocking in direct memory access activities. Figure shows the 'LS424 connected to an 8080A, quartz crystal, and LC circuits.

status strobe

The 8080A CPU puts status information on its data bus at the beginning of each machine cycle that defines the nature of the machine operation for that cycle. A sync signal from the 8080A is gated by an internal timing signal ($\phi1A$) and becomes a status strobe to notify system components that the status data is present on 8080A status output lines. The status strobe signal connects directly to the 'S428 system controller.

The status strobe signal is alternatively generated by the reset input. An external RC series network connected to V_{CC} and the reset input will provide a rising voltage waveform when V_{CC} is turned on. An internal Schmitt trigger circuit generates a sharp, fast-rising waveform when the reset input reaches a particular voltage value. The Schmitt trigger is connected to the D input of a flip-flop clocked by $\phi2D$. When power is turned on, the combination of internal and external circuitry will produce a status strobe signal. A manual reset switch can be connected as in figure 6 to the RC network to produce reset and status strobe signals for the 8080A.

The ready signal indicates to the 8080A that an external device has completed transfer of data to or from the data bus. A ready signal input to the 'LS424 drives the D input of a flip-flop clocked by an internal $\phi2D$ signal. Timing requirements of the 8080A machine cycle are met by the synchronization with the system clocks provided by the flip-flop. This implementation saves about 200 ns of system time during memory cycles (as contrasted with generating a "wait request" within the 8080A's MOS logic) since the bipolar logic of the 'LS424 has much less delay.

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TYPICAL APPLICATION DATA

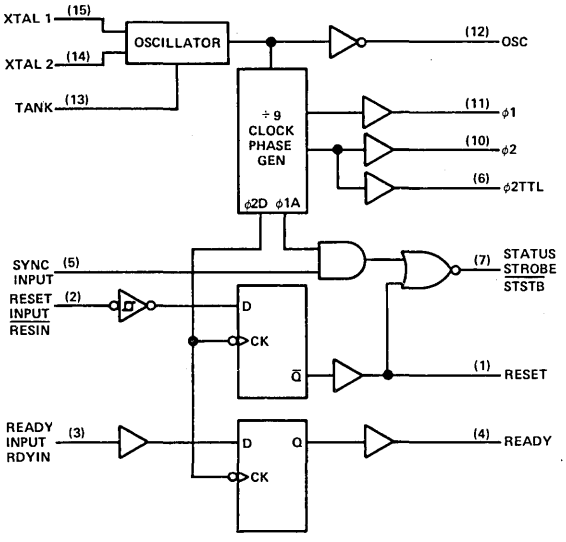
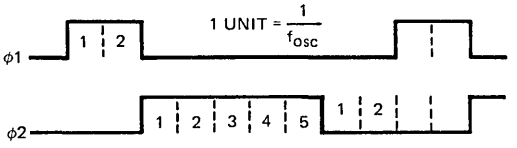


FIGURE 4



Example: 8080A cycle = 450 ns

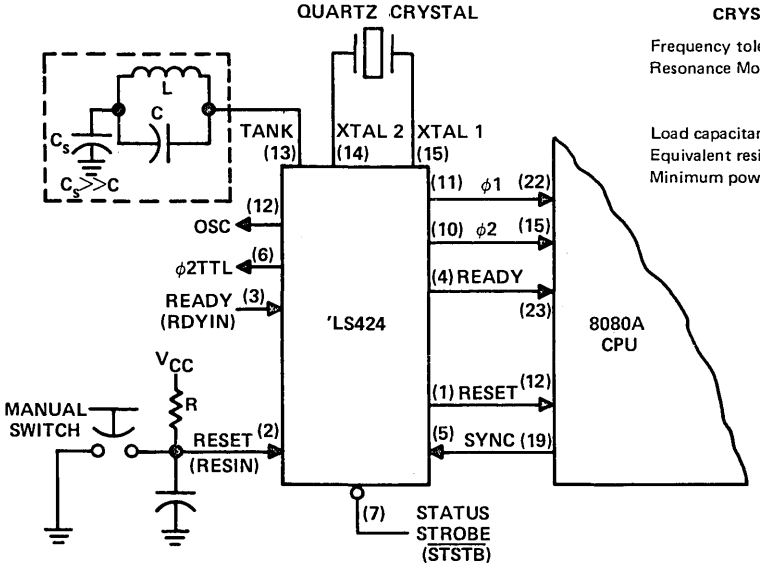
f_{osc}: 20 MHz (unit = 50 ns)

$t_{w(\phi1)}$ = 100 ns (2 X 50 ns)

$t_{w(\phi2)}$ = 250 ns (5 X 50 ns)

$t_{\phi2L,\phi1H}$ = 100 ns (2 X 50 ns)

FIGURE 5



CRYSTAL REQUIREMENTS

Frequency tolerance: ±0.005% for 0°C to 70°C
Resonance Mode: series, fundamental (use 3rd overtone mode with tank circuit)
Load capacitance: 20 pF to 35 pF
Equivalent resistance: 20 Ω to 75 Ω
Minimum power dissipation: 4 mW

FIGURE 6

TYPES SN74S428(TIM8228), SN74S438(TIM8238) CONTROLLER AND BUS DRIVER FOR 8080A SYSTEMS

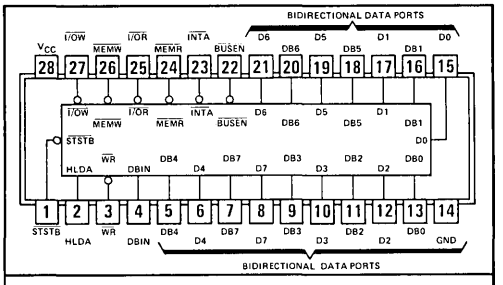
BULLETIN NO. DL-S 12468, OCTOBER 1976

- Designed to Be Interchangeable with Intel 8228 and 8238

PIN DESIGNATIONS

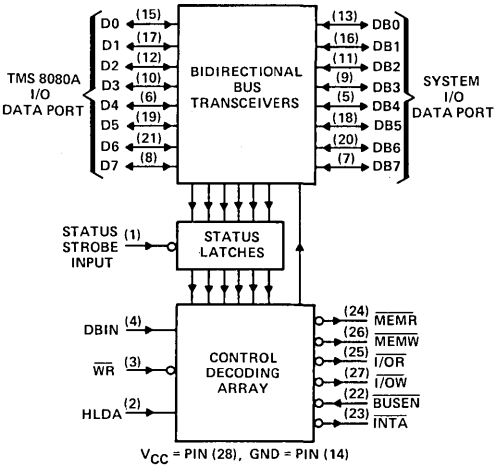
DESIGNATION	PIN NOS.	FUNCTION
D0 thru D7	15, 17, 12, 10, 6, 19, 21, 8	BIDIRECTIONAL DATA PORT (TO TMS 8080A)
DB0 thru DB7	13, 16, 11, 9, 5, 18, 20, 7	BIDIRECTIONAL DATA PORT (TO SYSTEM BUS)
$\overline{I/OR}$	25	READ OUTPUT TO I/O (ACTIVE LOW)
$\overline{IO/W}$	27	WRITE OUTPUT TO I/O (ACTIVE LOW)
$\overline{MEMR}$	24	READ OUTPUT TO MEMORY (ACTIVE LOW)
$\overline{MEMW}$	26	WRITE OUTPUT TO MEMORY (ACTIVE LOW)
DBIN	4	INPUT TO INDICATE TMS 8080A IS IN INPUT MODE (ACTIVE HIGH)
$\overline{INTA}$	23	INTERRUPT ACKNOWLEDGE OUTPUT (ACTIVE LOW)
HLDA	2	HOLD ACKNOWLEDGE INPUT (ACTIVE HIGH) FROM TMS 8080A
$\overline{WR}$	3	INPUT TO INDICATE TMS 8080A IS IN WRITE MODE (ACTIVE LOW)
$\overline{BUSEN}$	22	SYSTEM DATA PORT ENABLE INPUT (ACTIVE LOW)
$\overline{STSTB}$	1	SYNCHRONIZING STATUS STROBE INPUT FROM SN74LS424 (TIM8224)
V_{CC}	28	SUPPLY VOLTAGE (5 V)
GND	14	GROUND

N PACKAGE
(TOP VIEW)



logic: see description

functional block diagram



description

These monolithic Schottky-clamped †TTL system controllers are designed specifically to provide bus-driving and peripheral-control capabilities for interfacing memory and I/O devices with the 8080A in small to medium-large microcomputer systems.

A bidirectional eight-bit parallel bus driver is provided that isolates the 8080A bus from the memory and I/O data bus allowing the system designed to utilize cost-effective memory and peripheral devices while obtaining the maximum efficiency from the microprocessor. The TTL system drivers also provide increased fan-out with a lower impedance that enhances noise margins on the system bus.

Implementation of the status latches and control decoding array of the SN74S428/SN74S438 provides for using either a single-level interrupt vector RST7 for small systems, or multiple-byte call instructions for systems needing unlimited interrupt levels.

†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U.S. Patent Number 3,463,975.

description (continued)

With respect to the system clocks, the SN74S438 is configured to generate an advanced response for I/O or memory write output signals to further simplify peripheral control implementation of complex systems. See Figure 3.

8-bit parallel bus transceiver

The 8-bit parallel bus transceiver buffers the 8080A data bus from the memory and I/O system bus by providing one port (DO through D7) to interface with the 8080A and another port (DBO through DB7) to interface with the system devices. The 8080A side of the transceiver is designed specifically to interface with the microprocessor data bus ensuring not only that the processor output drive capabilities are adequate, but also that the inputs are driven with enhanced noise margins. The system bus side features high fan-out buffers designed to drive a number of system devices simultaneously and directly. The system port is rated to sink ten milliamperes of current and to source one milliampere of current at standard low-threshold voltage levels.

Status lines from the 8080A instruction-status decoder and the system bus enable input (BUSEN) provide complete transceiver directional and enable control to ensure integrity of both the processor data and the system bus data.

status latches

During the beginning of each machine cycle, the six status latches receive status information from the 8080A data bus indicating the type of operation that will be performed. When the $\overline{\text{STSTB}}$ input goes low, the latches store the status data and generate the signals needed to enable and sequence the memory and I/O control outputs. The status words and types of machine cycles are enumerated in Table A.

TABLE A – STATUS WORDS

STATUS WORD	8080A STATUS OUTPUT								TYPE OF MACHINE CYCLE	'S428/'S438 COMMAND GENERATED
	D0	D1	D2	D3	D4	D5	D6	D7		
1	L	H	L	L	L	H	L	H	Instruction fetch	$\overline{\text{MEMR}}$
2	L	H	L	L	L	L	L	H	Memory read	$\overline{\text{MEMR}}$
3	L	L	L	L	L	L	L	L	Memory write	$\overline{\text{MEMW}}$
4	L	H	H	L	L	L	L	H	Stack read	$\overline{\text{MEMR}}$
5	L	L	H	L	L	L	L	L	Stack write	$\overline{\text{MEMW}}$
6	L	H	L	L	L	L	H	L	Input read	$\overline{\text{I/OR}}$
7	L	L	L	L	H	L	L	L	Output write	$\overline{\text{I/OW}}$
8	H	H	L	L	L	H	L	L	Interrupt acknowledge	$\overline{\text{INTA}}$
9	L	H	L	H	L	L	L	H	Halt acknowledge	NONE
10	H	H	L	H	L	H	L	L	Interrupt acknowledge at halt	$\overline{\text{INTA}}$
	INTA	$\overline{\text{WO}}$	STACK	HLTA	OUT	M1	INP	MEMR		
	STATUS INFORMATION									

decoding array

The decoding array receives enabling commands from the status latches and sequencing commands from the 8080A and generates memory and I/O read/write commands and an interrupt acknowledgement.

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description (continued)

The read commands ($\overline{\text{MEMR}}$, $\overline{\text{I/OR}}$) and the interrupt acknowledgement ($\overline{\text{INTA}}$) are derived from the status bit(s) and the data bus input mode (DBIN) signal. The write commands ($\overline{\text{MEMW}}$, $\overline{\text{I/OW}}$) are derived from the status bit(s) and the write mode ($\overline{\text{WR}}$) signal. (See Table A.) All control commands are active low to simplify interfacing with memory and I/O controllers.

The interrupt acknowledgement ($\overline{\text{INTA}}$) command output is actually a dual function pin. As an output, its function is to provide the $\overline{\text{INTA}}$ command to the memory and I/O peripherals as decoded from the status inputs and latches. When CALL is used as an interrupt instruction, the SN74S428/SN74S428 generates the proper sequence of control signals. Additionally, the terminal includes high-threshold decoding logic that permits it to be biased through a one-kilohm series resistor to the 12-volt supply to implement an interrupt structure that automatically inserts an RST7 instruction on the bus when the DBIN input is active and an interrupt is acknowledged. This capability provides a single-level interrupt vector with minimal hardware.

The asynchronous bus enable ($\overline{\text{BUSEN}}$) input to the decoding array is a control signal that protects the system bus. The system bus can be accessed and driven from the SN74S428/SN74S428 controller only when the $\overline{\text{BUSEN}}$ input is at a low voltage level.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level output current, I_{OH}	D0 thru D7			−10	μA
	All others			−1	mA
Low-level output current, I_{OL}	D0 thru D7			2	mA
	All others			10	
Status strobe pulse width, $t_{w(STSTB)}$ (see Figure 3)		22			ns
Setup time, t_{su} (see Figure 3)	Status inputs D0 thru D7	8			ns
	System bus inputs to HLDA	10			
Hold time, t_h (see Figure 3)	Status inputs D0 thru D7	5			ns
	System bus inputs to HLDA	20			
Operating free-air temperature, T_A		0		70	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −5 mA			−1	V
V_{OH}	High-level output voltage	D0 thru D7	V_{CC} = MIN,	V_{IH} = 2 V,	3.6	4		V
		All other outputs	V_{IL} = 0.8 V,	I_{OH} = MAX	2.4			
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = MAX			0.45	V
I_{OZH}	Off-state output current, high-level voltage applied		V_{CC} = MAX,	V_O = 5.25 V			100	μA
I_{OZL}	Off-state output current, low-level voltage applied		V_{CC} = MAX,	V_O = 0.45 V			−100	μA
I_{IH}	High-level input current	$\overline{INTA}$	V_{CC} = MIN,	See Figure 1			5	mA
		D0 thru D7	V_{CC} = MAX,	V_I = 5.25 V			20	μA
		All other inputs					100	
I_{IL}	Low-level input current	D2 or D6	V_{CC} = MAX,	V_I = 0.45 V			−750	μA
		$\overline{STSTB}$					−500	
		All other inputs					−250	
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−15		−90	mA
I_{CC}	Supply current		V_{CC} = MAX			140	190	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, see figure 3

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PD}	D0 thru D7	DB0 thru DB7	C_L = 100 pF,	See Figure 2	5		40	ns
t_{PD}	DB0 thru DB7	D0 thru D7	C_L = 25 pF,	See Figure 2			30	ns
t_{PHL}	$\overline{STSTB}$	$\overline{INTA}$, $\overline{I/OR}$, $\overline{MEMR}$, $\overline{I/OW}$, $\overline{MEMW}$	C_L = 100 pF,	See Figure 2	20		60	ns
t_{PD}	$\overline{WR}$	$\overline{I/OW}$, $\overline{MEMW}$			5		45	ns
t_{PLH}	DBIN	$\overline{INTA}$, $\overline{I/OR}$, $\overline{MEMR}$					30	ns
t_{PLH}	HLDA	$\overline{INTA}$, $\overline{I/OR}$, $\overline{MEMR}$					25	ns
t_{PZX}	DBIN	D0 thru D7	C_L = 25 pF,	See Figure 2			45	ns
t_{PXZ}	DBIN	D0 thru D7					45	ns
t_{PZX}	$\overline{STSTB}$, $\overline{BUSEN}$	DB0 thru DB7	C_L = 100 pF,	See Figure 2			30	ns
t_{PXZ}	$\overline{BUSEN}$	DB0 thru DB7					30	ns

¶ t_{PD} ≡ propagation delay time
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PZX} ≡ output enable time from high-impedance state
t_{PXZ} ≡ output disable time to high-impedance state

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PARAMETER MEASUREMENT INFORMATION

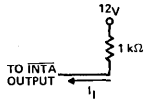


FIGURE 1–$\overline{\text{INTA}}$ INPUT CURRENT TEST CIRCUIT

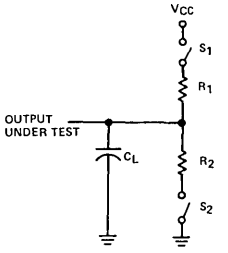
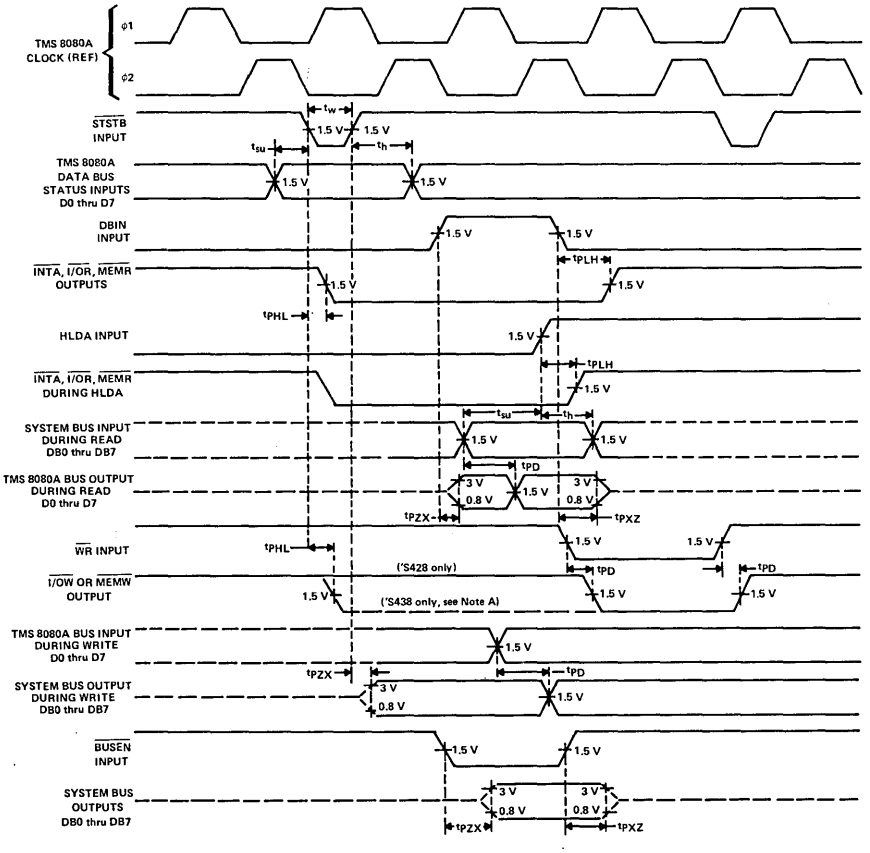


FIGURE 2–SWITCHING CHARACTERISTICS LOAD CIRCUIT



NOTE A: Advanced response of $\overline{\text{I/OW}}$ or $\overline{\text{MEMW}}$ for the SN74S438 is indicated by the dashed line.

FIGURE 3–VOLTAGE WAVEFORMS

TYPICAL APPLICATION DATA

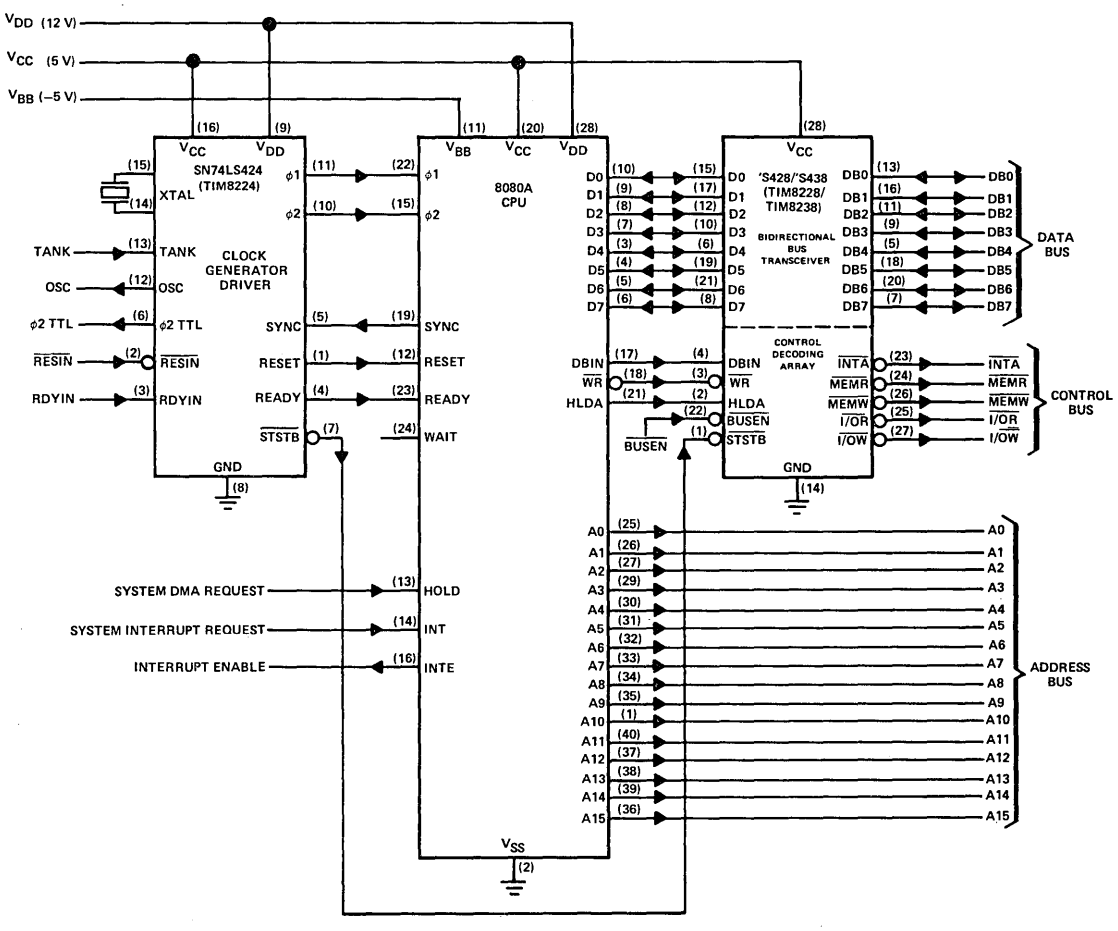


FIGURE 4–SYSTEM INTERFACING WITH CENTRAL PROCESSING UNIT

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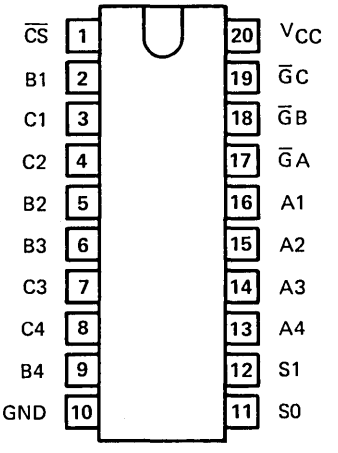
TYPES SN54LS440 THRU SN54LS444, SN54LS448, SN74LS440 THRU SN74LS444, SN74LS448 QUADRUPLE TRIDIRECTIONAL BUS TRANSCEIVERS

BULLETIN NO. DL-S 12709, AUGUST 1979

- 3-Way Asynchronous Communication
- On-Chip Bus Selection Decoding
- Input Hysteresis Improves Noise Margin
- Choice of Open-Collector or 3-State Outputs

SN54LS' . . . . . J PACKAGE
SN74LS' . . . . . J OR N PACKAGE
(TOP VIEW)



description

These bus transceivers are designed for asynchronous three-way communication between four-line data buses. They give the designer a choice of selecting inverting, noninverting, or a combination of inverting and noninverting data paths with either 3-state or open-collector outputs.

The S0 and S1 inputs select the bus from which data are to be transferred. The $\overline{G}$ inputs enable the bus or buses to which data are to be transferred. The port for any bus selected for input and any other bus not enabled for output will be at high impedance including those of the open-collector devices.

The SN54LS440 through SN54LS444 and SN54LS448 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LS440 through SN74LS444 and SN74LS448 are characterized for operation from 0°C to 70°C.

DEVICE	OUTPUT	LOGIC
'LS440	Open-Collector	True
'LS441	Open-Collector	Inverting
'LS442	3-State	True
'LS443	3-State	Inverting
'LS444	3-State	True/Inverting
'LS448	Open-Collector	True/Inverting

6

FUNCTION TABLE

INPUTS						TRANSFERS BETWEEN BUSES		
$\overline{CS}$	S1	S0	$\overline{G}A$	$\overline{G}B$	$\overline{G}C$	'LS440 'LS442	'LS441 'LS443	'LS444 'LS448
H	X	X	X	X	X	None	None	None
X	H	H	X	X	X	None	None	None
X	X	X	H	H	H	None	None	None
X	L	L	X	H	H	None	None	None
X	L	H	H	X	H	None	None	None
X	H	L	H	H	X	None	None	None
L	L	L	X	L	L	A → B, A → C	$\overline{A}$ → B, $\overline{A}$ → C	$\overline{A}$ → B, $\overline{A}$ → C
L	L	H	L	X	L	B → C, B → A	$\overline{B}$ → C, $\overline{B}$ → A	B → C, $\overline{B}$ → A
L	H	L	L	L	X	C → A, C → B	$\overline{C}$ → A, $\overline{C}$ → B	$\overline{C}$ → A, C → B
L	L	L	X	L	H	A → B	$\overline{A}$ → B	$\overline{A}$ → B
L	L	H	H	X	L	B → C	$\overline{B}$ → C	B → C
L	H	L	L	H	X	C → A	$\overline{C}$ → A	$\overline{C}$ → A
L	L	L	X	H	L	A → C	$\overline{A}$ → C	$\overline{A}$ → C
L	L	H	L	X	H	B → A	$\overline{B}$ → A	$\overline{B}$ → A
L	H	L	H	L	X	C → B	$\overline{C}$ → B	C → B

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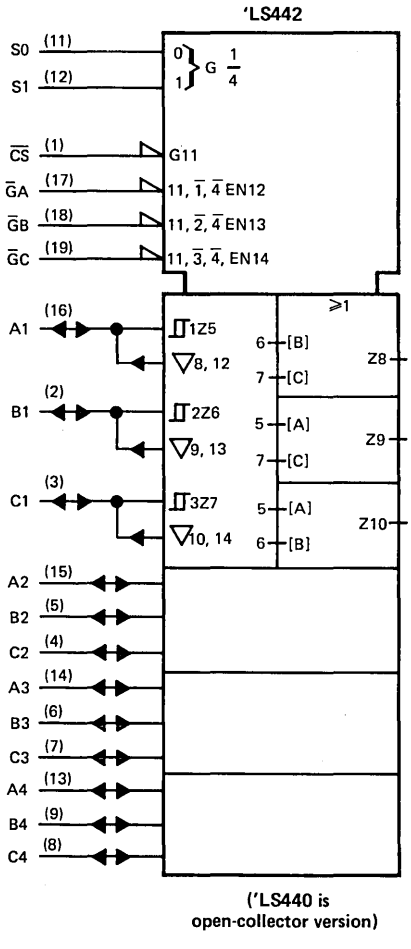
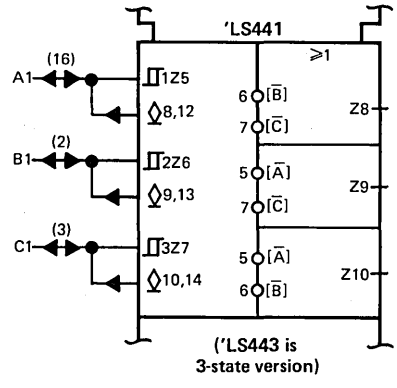
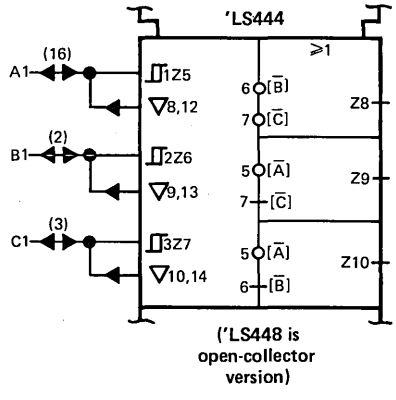
logic symbols†



('LS440 is open-collector version)



('LS443 is 3-state version)



('LS448 is open-collector version)

†These symbols are in accordance with IEEE Std 91/ANSI Y32.14 and current discussions in IEC and IEEE.

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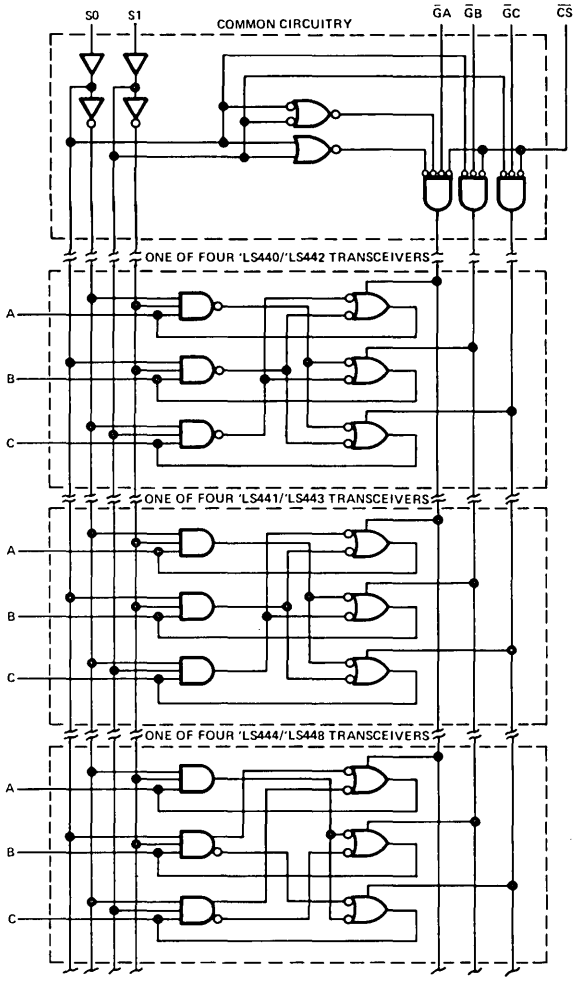
functional block diagram (composite showing one of four transceivers from each type, positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)		7 V
Input voltage		7 V
Off-state output voltage		5.5 V
Operating free-air temperature range:	SN54LS'	−55°C to 125°C
	SN74LS'	0°C to 70°C
Storage temperature range		−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS440 SN54LS441 SN54LS448			SN74LS440 SN74LS441 SN74LS448			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	−55		125	0		70	C

NOTE 1: Voltage values are with respect to the network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.5			0.6	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
	Hysteresis ($V_{T+} - V_{T-}$)	A,B,C input	V_{CC} = MIN		0.1	0.4		0.2	0.4		V
I_{OH}	High-level output current		V_{CC} = MIN, V_{IH} = 2 V,	V_{OH} = 5.5 V, V_{IL} = V_{IL}max			100			100	μA
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	V
I_I	Input current at maximum input voltage	A,B,C input	V_{CC} = MAX	V_I = 5.5 V			0.1			0.1	mA
		All others		V_I = 7 V			0.1			0.1	
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current		V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
I_{CC}	Supply current	Outputs low	V_{CC} = MAX,	Outputs open		62	90		62	90	mA
		Outputs disabled				64	95		64	95	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics at V_{CC} = 5 V, R_L = 667 Ω, C_L = 45 pF, T_A = 25°C (see Note 2)

PARAMETER		INPUT	OUTPUT	'LS440			'LS441			'LS448			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high level output	A	B		24	35		21	30		21	30	ns
		A	C		24	35		21	30		21	30	
		B	A		24	35		21	30		21	30	
		B	C		24	35		21	30		24	35	
		C	A		24	35		21	30		21	30	
		C	B		24	35		21	30		24	35	
t_{PHL}	Propagation delay time, high-to-low level output	A	B		20	30		9	15		9	15	ns
		A	C		20	30		9	15		9	15	
		B	A		20	30		9	15		9	15	
		B	C		20	30		9	15		20	30	
		C	A		20	30		9	15		9	15	
		C	B		20	30		9	15		20	30	
t_{PLH}	Propagation delay time, low-to-high level output	any $\overline{G}$	A, B, C		29	45		23	35		25	40	ns
		S0, S1	A, B, C		33	50		27	40		26	40	
		$\overline{CS}$	A, B, C		31	45		26	40		25	40	
t_{PHL}	Propagation delay time, high-to-low level output	any $\overline{G}$	A, B, C		27	40		20	30		22	35	ns
		S0, S1	A, B, C		32	50		26	40		27	40	
		$\overline{CS}$	A, B, C		28	45		21	30		22	35	

NOTE 2: Load circuits and voltage waveforms are shown on page 1-15.

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recommended operating conditions

	SN54LS442 SN54LS443 SN54LS444			SN74LS442 SN74LS443 SN74LS444			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−12			−15	mA
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

NOTE 1: Voltage values are with respect to the network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2						V
V_{IL}	Low-level input voltage						0.5			0.6	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
	Hysteresis ($V_{T+} - V_{T-}$)	A,B,C input	V_{CC} = MIN		0.1	0.4		0.2	0.4		V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max	I_{OH} = −3 mA	2.4	3.4		2.4	3.4		V
				I_{OH} = MAX	2			2			
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied		V_{CC} = MAX, $\overline{CS}$ at 2 V	V_O = 2.7 V			20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied			V_O = 0.4 V			−400			−400	
I_I	Input current at maximum input voltage	A,B,&C	V_{CC} = MAX	V_I = 5.5 V			0.1			0.1	mA
		Others		V_I = 7 V			0.1			0.1	
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current		V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
I_{OS}	Short circuit output current¶		V_{CC} = MAX		−40		−225	−40		−225	mA
I_{CC}	Supply current	Total outputs low	V_{CC} = MAX,	Outputs open		62	90		62	90	mA
		Outputs at Hi-Z				64	95		64	95	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
¶Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

6

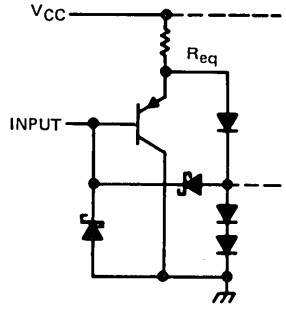
switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Note 2)

PARAMETER		INPUT	OUTPUT	TEST CONDITIONS	'LS442			'LS443			'LS444			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high level output	A	B	C_L = 45 pF, R_L = 667 Ω		10	14		9	14		9	14	ns
		A	C			10	14		9	14		9	14	
		B	A			10	14		9	14		9	14	
		B	C			10	14		9	14		10	14	
		C	A			10	14		9	14		9	14	
		C	B			10	14		9	14		10	14	
t_{PHL}	Propagation delay time, high-to-low level output	A	B			13	20		7	13		7	13	ns
		A	C			13	20		7	13		7	13	
		B	A			13	20		7	13		7	13	
		B	C			13	20		7	13		13	20	
		C	A			13	20		7	13		7	13	
		C	B			13	20		7	13		13	20	
t_{PZL}	Output enable time to low level	Any $\overline{G}$	A, B, C			22	33		22	33		22	33	ns
		S0 or S1	A, B, C			28	42		28	42		28	42	
		$\overline{CS}$	A, B, C			23	36		24	36		23	36	
t_{PZH}	Output enable time to high level	$\overline{G}$, S, $\overline{CS}$	A, B, C			21	32		20	32		24	32	ns
t_{PLZ}	Output disable time from low level	$\overline{G}$, S, GS	A, B, C	C_L = 5 pF, R_L = 667 Ω		14	25		15	25		14	25	ns
t_{PHZ}	Output disable time from high level	$\overline{G}$, S, $\overline{CS}$	A, B, C			14	25		15	25		14	25	ns

NOTE 2: Load circuits and voltage waveforms are shown on page 1-15.

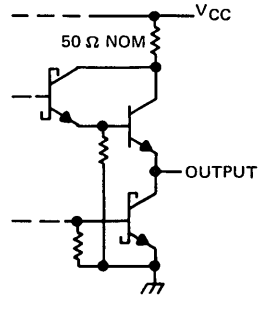
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT

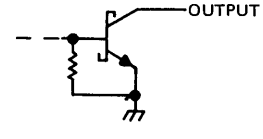


R_{eq}: $\overline{G}A$, $\overline{G}B$, $\overline{G}C$ = 9 kΩ NOM
All others = 5 kΩ NOM

TYPICAL OF 3-STATE OUTPUTS



TYPICAL OF OPEN-COLLECTOR OUTPUT



TEXAS INSTRUMENTS
INCORPORATED
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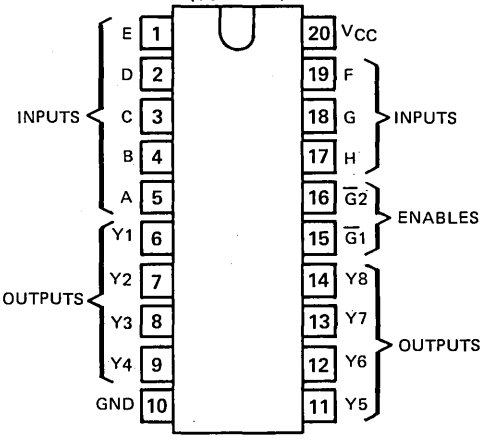
TYPES SN54S484, SN54S485, SN74S484, SN74S485
BCD-TO-BINARY AND BINARY-TO-BCD CONVERTERS

BULLETIN NO. DL-S 12700, JUNE 1979

SN54S484, SN74S484 BCD-TO-BINARY CONVERTERS
SN54S485, SN74S485 BINARY-TO-BCD CONVERTERS

- Significant Savings in Package Count Compared with SN54184, SN54185A, SN74184, or SN74185A (Over Half in Many Applications)
- Three-State Outputs

SN54S484, SN54S485 . . . J PACKAGE
SN54S484, SN54S485 . . . J OR N PACKAGE
(TOP VIEW)



description

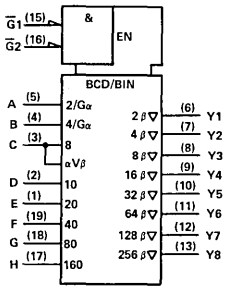
These monolithic converters are derived from the SN54S371/SN74S371 custom-programmed read-only memories. Both of these converters comprehend that the least-significant bits (LSB) of the binary and BCD are logically equal, and in each case the LSB bypasses the converter as shown in the typical applications. This means that a nine-bit converter is produced in each case. The devices are cascadable to N bits.

The three-state outputs offer the convenience of open-collector outputs with the speed of totem-pole outputs: they can be bus-connected to other similar outputs yet they retain the fast rise-time characteristic of totem-pole outputs. A high logic level at either enable ($\overline{G}$) input causes the outputs to be in a high-impedance state.

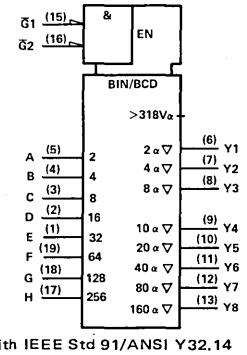
These converters, by including three more bits of conversion than their SN54184/SN74184 or SN54185/SN74185 counterparts, result in a reduction in package count by more than half in most applications, and a significant savings in power consumption in many applications as shown in the tables at right.

logic symbols†

SN54S484
SN74S484



SN54S485,
SN74S485



†These symbols are in accordance with IEEE Std 91/ANSI Y32.14 and current discussions in IEC and IEEE.

SN54S484/SN74S484 vs SN54184/SN74184

DECADES	PACKAGE COUNT		MAXIMUM SUPPLY CURRENT (A)		TYPICAL ACCESS TIME @ T_A = 25°C (ns)	
	'S484	'184	'S484	'184	'S484	'184
3	3	6	0.41	0.59	117	135
4	5	11	0.72	1.09	180	189
5	8	18	1.18	1.78	270	270
6	12	27	1.75	2.67	342	351
7	16	38	2.37	3.76	405	405
8	21	49	3.14	4.85	495	485
9	27	62	4.02	6.14	567	540

SN54S485/SN74S485 vs SN54185/SN74185

BINARY BITS	PACKAGE COUNT		MAXIMUM SUPPLY CURRENT (A)		TYPICAL ACCESS TIME @ T_A = 25°C (ns)	
	'S485	'185	'S485	'185	'S485	'185
8	2	3	0.35	0.30	72	81
16	8	16	1.44	1.58	252	216
24	19	40	3.44	3.96	459	351
32	33	74	4.78	5.45	612	486

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SN54S484, SN74S484
BCD-TO-BINARY CONVERTER
FUNCTION TABLE

INPUTS								OUTPUTS							
H	G	F	E	D	C	B	A	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1
160	80	40	20	10	8	4	2	256	128	64	32	16	8	4	2
L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	H
L	L	L	L	L	L	H	L	L	L	L	L	L	L	H	L
L	L	L	L	L	L	H	H	L	L	L	L	L	L	H	H
L	L	L	L	L	H	L	L	L	L	L	L	L	H	L	L
L	L	L	L	L	H	L	H	Invalid BCD code (All outputs are high)							
L	L	L	L	L	H	H	L								
L	L	L	L	L	H	H	H								
L	L	L	L	H	L	L	L	L	L	L	L	L	H	L	H
L	L	L	L	H	L	L	H	L	L	L	L	L	H	H	L
L	L	L	L	H	L	H	L	L	L	L	L	L	H	H	H
H	H	H	H	L	L	H	L	H	L	L	H	H	L	L	L
H	H	H	H	L	L	H	H	H	L	L	H	H	L	L	H
H	H	H	H	L	H	L	L	H	L	L	H	H	L	H	L
H	H	H	H	L	H	L	H								
H	H	H	H	L	H	H	L								
H	H	H	H	L	H	H	H								
H	H	H	H	H	L	L	L	H	L	L	H	H	L	L	H
H	H	H	H	H	L	L	H	H	L	L	H	H	H	L	L
H	H	H	H	H	L	H	L	H	L	L	H	H	H	L	H
H	H	H	H	H	L	H	H	H	L	L	H	H	H	H	L
H	H	H	H	H	H	L	L								
H	H	H	H	H	H	L	H								
H	H	H	H	H	H	H	L								
H	H	H	H	H	H	H	H								
X	X	X	X	X	H	X	H	H	H	H	H	H	H	H	H
X	X	X	X	X	H	H	X	H	H	H	H	H	H	H	H

H = high level L = low level X = irrelevant

SN54S485, SN74S485
BINARY-TO-BCD CONVERTER
FUNCTION TABLE

INPUTS								OUTPUTS							
H	G	F	E	D	C	B	A	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1
256	128	64	32	16	8	4	2	160	80	40	20	10	8	4	2
L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	H
L	L	L	L	L	L	H	L	L	L	L	L	L	L	H	L
L	L	L	L	L	L	H	H	L	L	L	L	L	L	H	H
L	L	L	L	L	H	L	L	L	L	L	L	L	H	L	L
L	L	L	L	L	H	L	H	L	L	L	L	H	L	L	L
L	L	L	L	L	H	H	L	L	L	L	L	H	L	L	H
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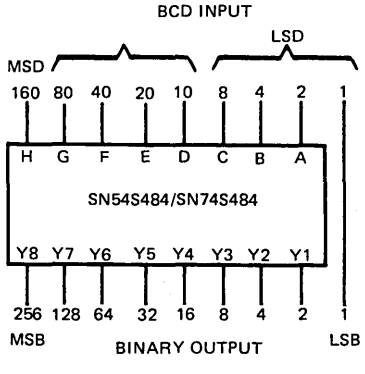
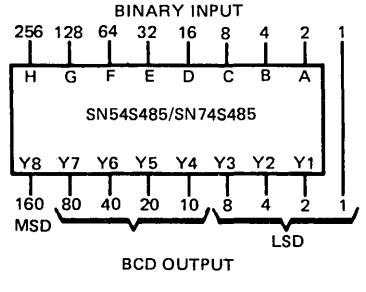
L	L	L	H	H	H	H	H	H	L	L	H	H	H	H	L
L	L	H	L	L	L	L	L	H	H	H	H	H	H	H	H
thru															
H	H	H	H	H	H	H	H								





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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) 7V
Input voltage 5.5V
Off-state output voltage 5.5V
Operating free-air temperature range: SN54S484, SN54S485 . . . . . −55°C to 125°C
SN74S484, SN74S485 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

	SN54S'			SN74S'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Off-state output voltage			5.5			5.5	V
High-level output current, I_{OH}			−2			−6.5	mA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

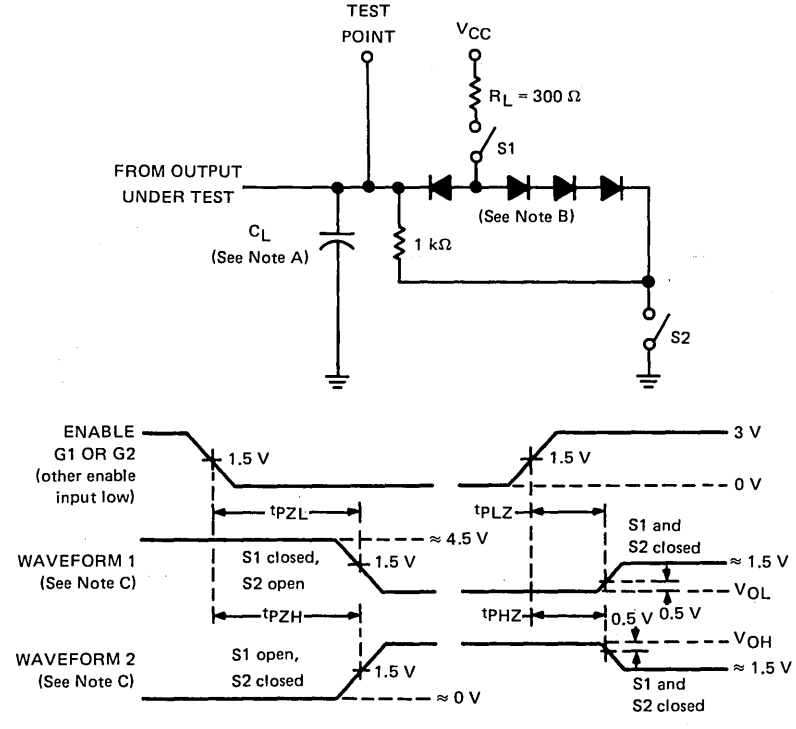
PARAMETER		TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = -18 mA				−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, I_{OH} = MAX	V_{IH} = 2 V,	V_{IL} = 0.8 V,	2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = MAX	V_{IH} = 2 V,	V_{IL} = 0.8 V,			0.5	V
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX,	V_{IH} = 2 V,	V_O = 2.7 V			50	μA
I_{OZL}	Off-state output current low-level voltage applied	V_{CC} = MAX,	V_{IH} = 2 V,	V_O = 0.4 V			−50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V				25	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.5 V				−0.25	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX,			−30		−100	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 2			105	155	mA
C_O	Off-state output capacitance	V_{CC} = 5 V,	V_O = 5 V,	f = 1 MHz		6.5		pF

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54S'			SN74S'			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$t_{a(ad)}$	Access time from address	C_L = 30 pF,	See Figure 1		45	95		45	70	ns
t_{PZX}	Output enable time				15	45		15	30	ns
t_{PXZ}	Output disable time	C_L = 5 pF,	See Figure 1		10	40		10	25	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
NOTES: 1. Voltage values are with respect to network ground terminal.
2. With outputs open and enable ($\overline{G}$) inputs grounded, I_{CC} is measured first by selecting a word that contains the maximum number of high-level outputs, then be selecting a word that contains the maximum number of low-level inputs.

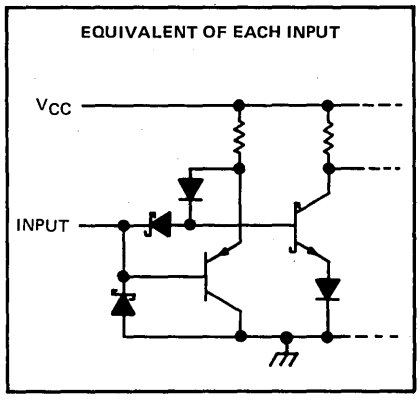
PARAMETER MEASUREMENT INFORMATION

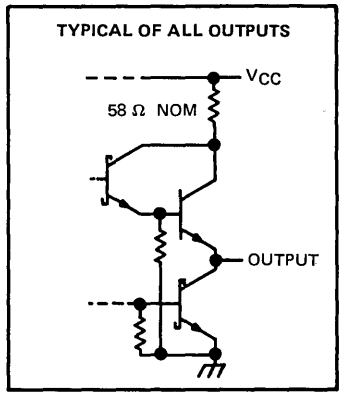


NOTES: A. C_L includes probe and capacitance.
B. All diodes are IN916 or IN3064.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

FIGURE 1

schematics of inputs and outputs





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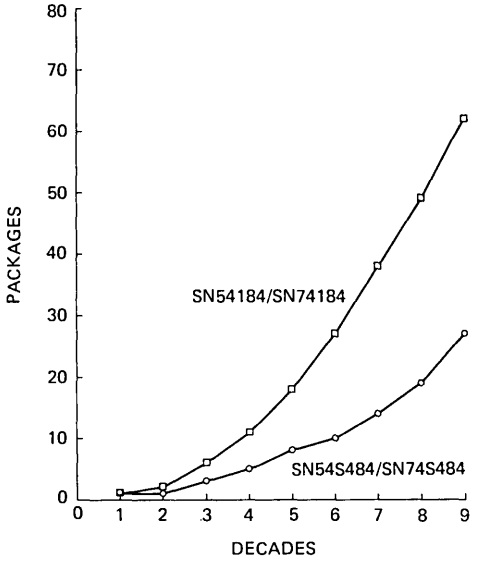
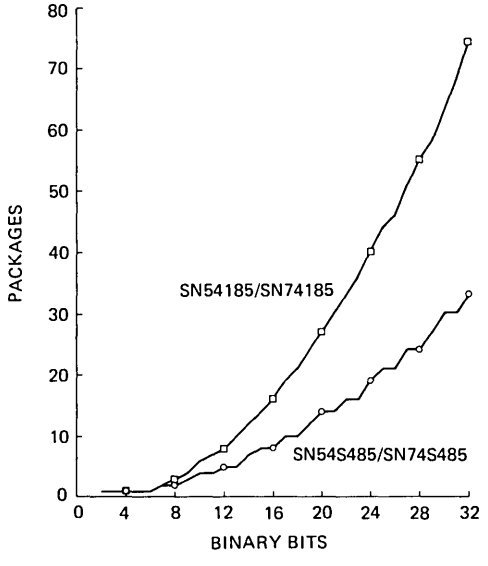
TYPICAL APPLICATION DATA

PACKAGES REQUIRED
vs
DECADES OF CONVERSION

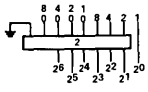


PACKAGES REQUIRED
vs
BINARY BITS OF CONVERSION

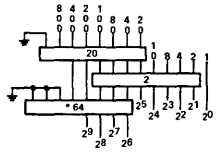


6

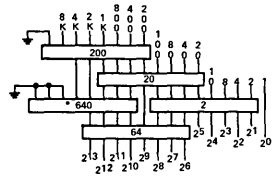
TYPICAL APPLICATION DATA
SN54S484, SN74S484



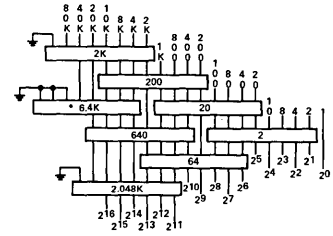
2-DECADE-BCD-TO-BINARY CONVERTER



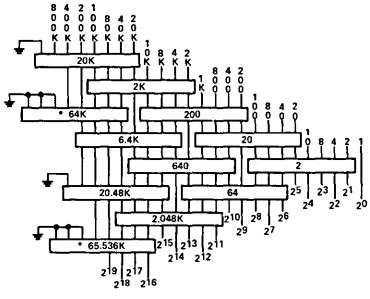
3-DECADE-BCD-TO-BINARY CONVERTER



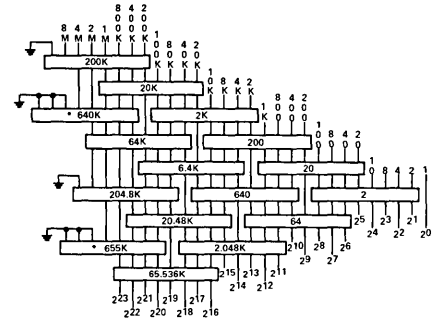
4-DECADE-BCD-TO-BINARY CONVERTER



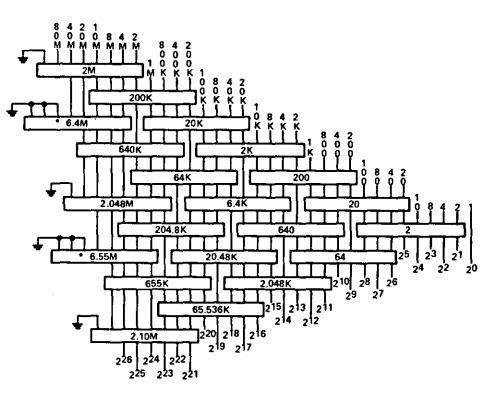
5-DECADE-BCD-TO-BINARY CONVERTER



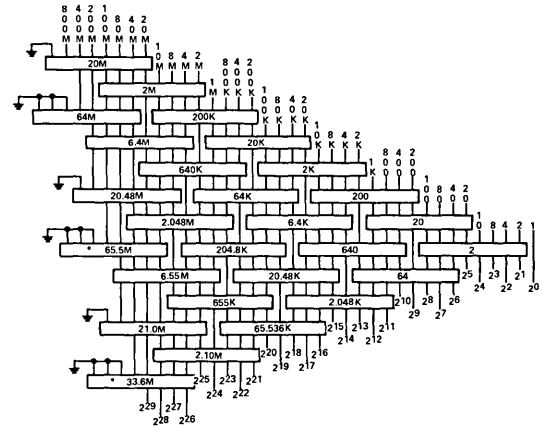
6-DECADE-BCD-TO-BINARY CONVERTER



7-DECADE-BCD-TO-BINARY CONVERTER



8-DECADE-BCD-TO-BINARY CONVERTER



9-DECADE-BCD-TO-BINARY CONVERTER

*SN54184/SN74184 can be used.

K = 10^3, M = 10^6

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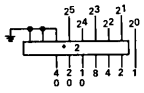
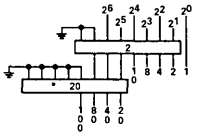
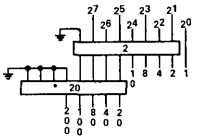
TYPICAL APPLICATION DATA
SN54S485, SN74S485



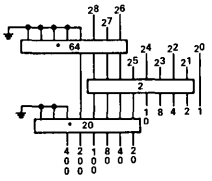
6-BIT-BINARY-TO-BCD CONVERTER



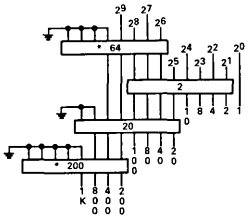
7-BIT-BINARY-TO-BCD CONVERTER



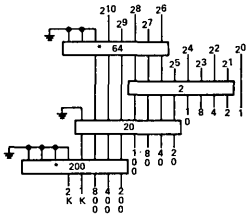
8-BIT-BINARY-TO-BCD CONVERTER



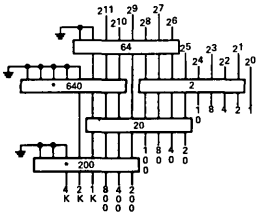
9-BIT-BINARY-TO-BCD CONVERTER



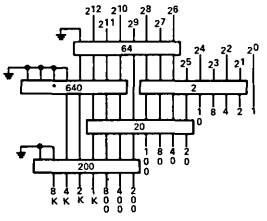
10-BIT-BINARY-TO-BCD CONVERTER



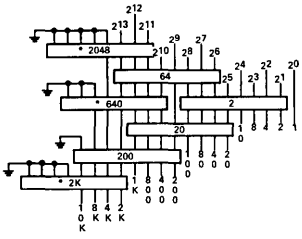
11-BIT-BINARY-TO-BCD CONVERTER



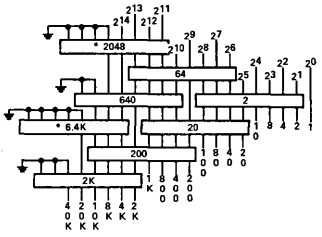
12-BIT-BINARY-TO-BCD CONVERTER



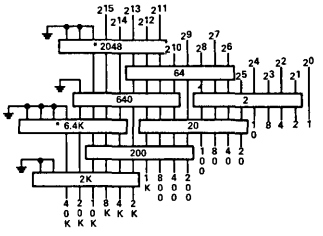
13-BIT-BINARY-TO-BCD CONVERTER



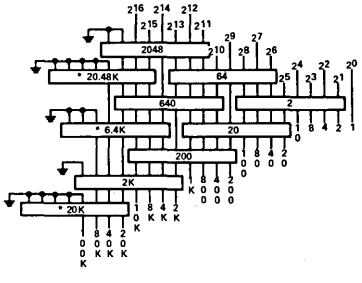
14-BIT-BINARY-TO-BCD CONVERTER



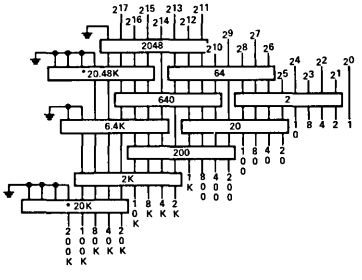
15-BIT-BINARY-TO-BCD CONVERTER



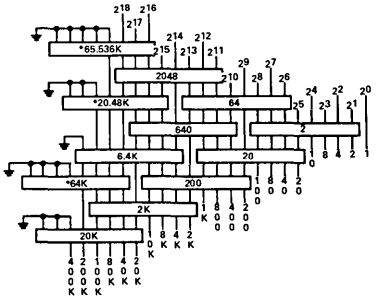
16-BIT-BINARY-TO-BCD CONVERTER



17-BIT-BINARY-TO-BCD CONVERTER



18-BIT-BINARY-TO-BCD CONVERTER



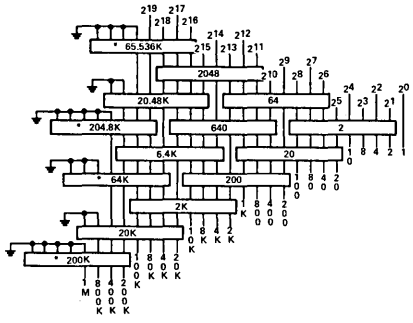
19-BIT-BINARY-TO-BCD CONVERTER

*SN54185/SN74185 can be used.

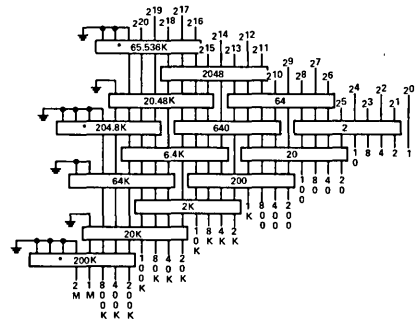
$K = 10^3$, $M = 10^6$

6

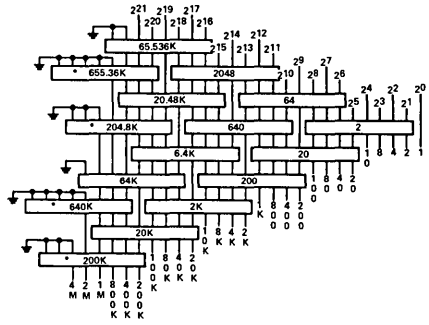
TYPICAL APPLICATION DATA
SN54S485/SN74S485



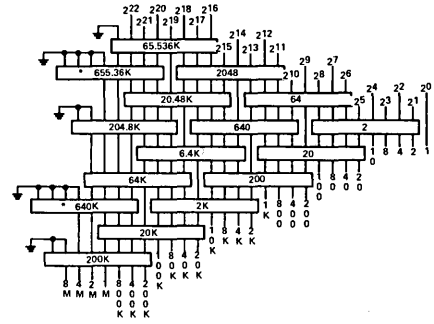
20-BIT-BINARY-TO-BCD CONVERTER



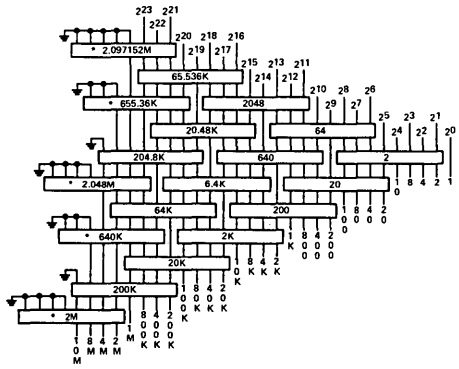
21-BIT-BINARY-TO-BCD CONVERTER



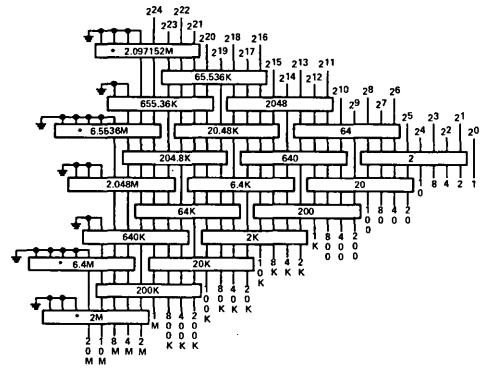
22-BIT-BINARY-TO-BCD CONVERTER



23-BIT-BINARY-TO-BCD CONVERTER



24-BIT-BINARY-TO-BCD CONVERTER



25-BIT-BINARY-TO-BCD CONVERTER

*SN54185/SN74185 can be used.

K = 10^3, M = 10^6

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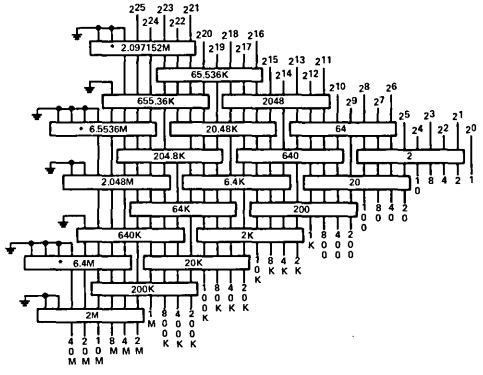
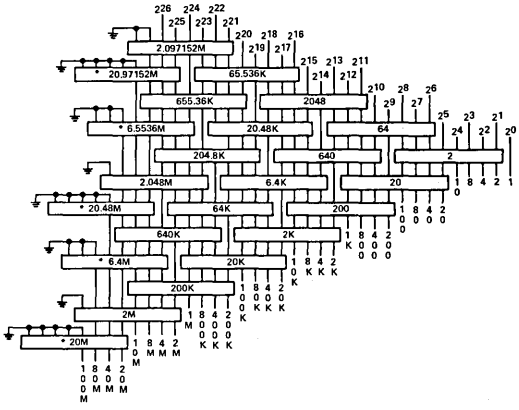
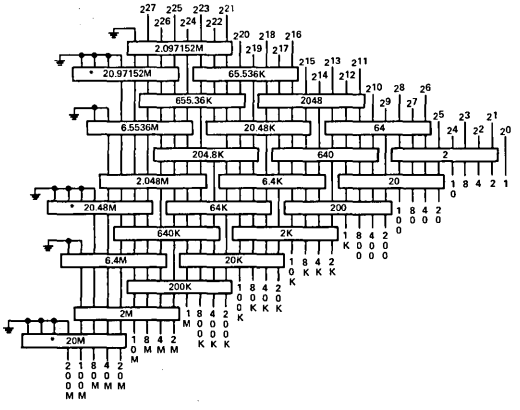
TYPICAL APPLICATION DATA
SN54S485, SN74S485



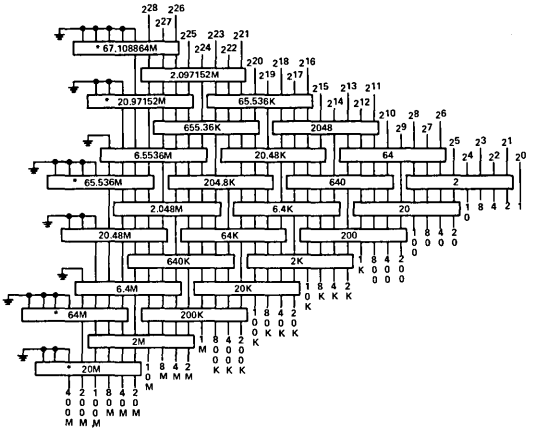
26-BIT-BINARY-TO-BCD CONVERTER



27-BIT-BINARY-TO-BCD CONVERTER



28-BIT-BINARY-TO-BCD CONVERTER

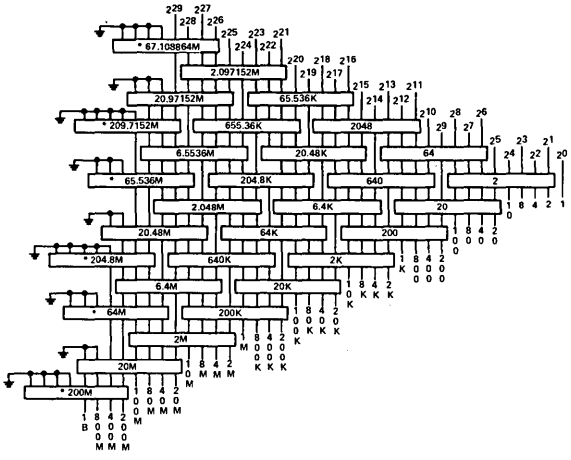


29-BIT-BINARY-TO-BCD CONVERTER

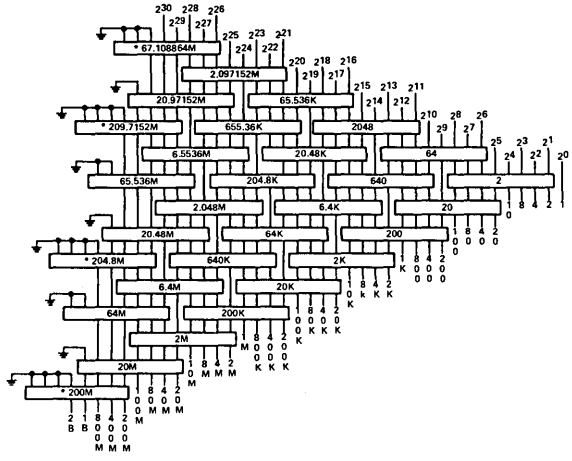
*SN54185/SN74185 can be used.

$K = 10^3$, $M = 10^6$

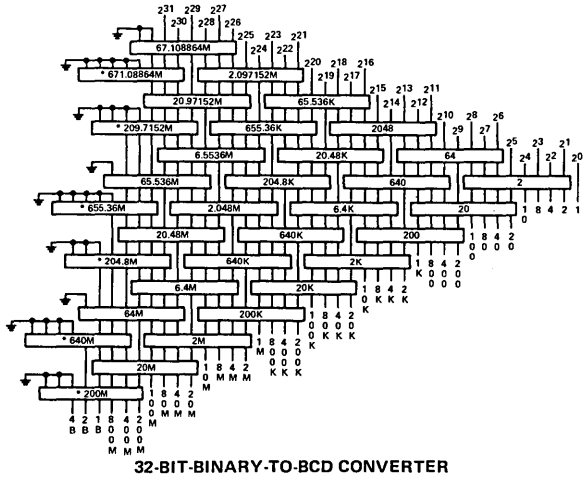
TYPICAL APPLICATION DATA
SN54S485, SN74S485



30-BIT-BINARY-TO-BCD CONVERTER



31-BIT-BINARY-TO-BCD CONVERTER



32-BIT-BINARY-TO-BCD CONVERTER

*SN54185/SN74185 can be used.

$K = 10^3$, $M = 10^6$

TEXAS INSTRUMENTS
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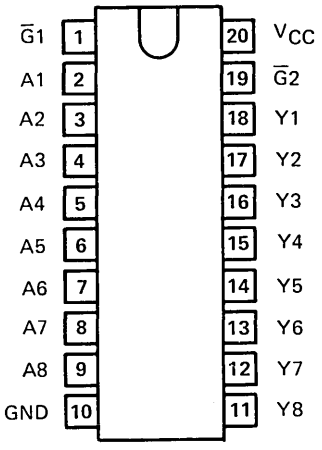
TYPES SN54LS540, SN54LS541, SN74LS540, SN74LS541
OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

BULLETIN NO. DL-S 12722, AUGUST 1979

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- P-N-P Inputs Reduce D-C Loading
- Hysteresis at Inputs Improves Noise Margins
- Data Flow-thru Pinout (All Inputs on Opposite Side from Outputs)

SN54LS' . . . J PACKAGE
SN74LS' . . . J OR N PACKAGE
(TOP VIEW)



description

These octal buffers and line drivers are designed to have the performance of the popular SN54LS240/SN74LS240 series and, at the same time, offer a pinout having the inputs and outputs on opposite sides of the package. This arrangement greatly enhances printed circuit board layout.

The three-state control gate is a 2-input NOR such that if either $\overline{G1}$ or $\overline{G2}$ are high, all eight outputs are in the high-impedance state.

The 'LS540 offers inverting data and the 'LS541 offers true data at the outputs.

The SN54LS540 and SN54LS541 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LS540 and SN74LS541 are characterized for operation from 0°C to 70°C.

	Rated I_{OL} (Sink Current)	Rated I_{OH} (Source Current)	Typical Power Dissipation (Enabled) Inverting	Noninverting
SN54LS'	12 mA	−12 mA	92.5 mW	117.5 mW
SN74LS'	24 mA	−15 mA	92.5 mW	117.5 mW

6

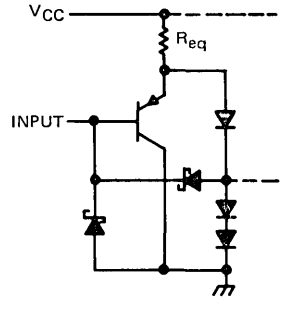
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS540, SN54LS541 . . . . . −55°C to 125°C
SN74LS540, SN74LS541 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

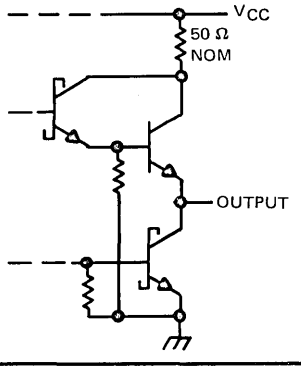
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



Enable Inputs: R_{eq} = 9 kΩ NOM
All Other Inputs: R_{eq} = 10 kΩ NOM

TYPICAL OF ALL OUTPUTS



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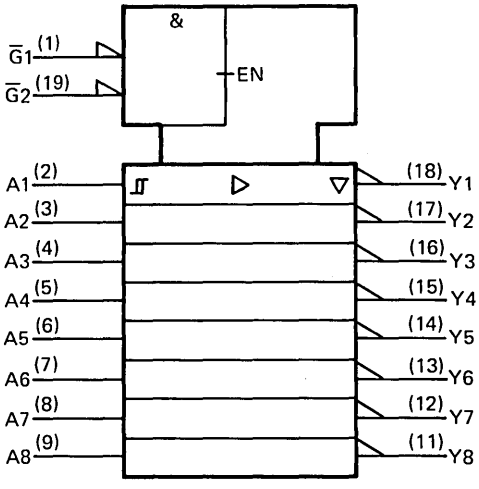
ADVANCE INFORMATION

This document contains information on a new product. Specifications are subject to change without notice.

logic symbols†

'LS540

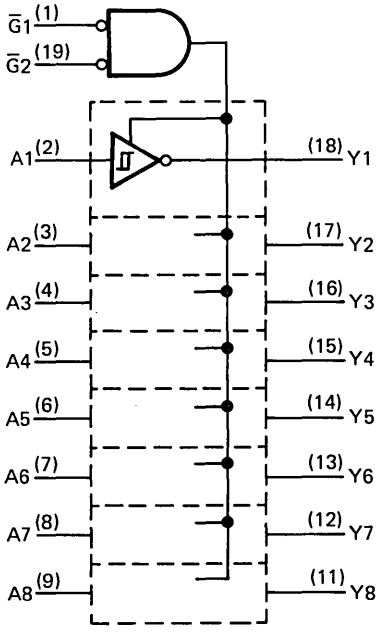


'LS541

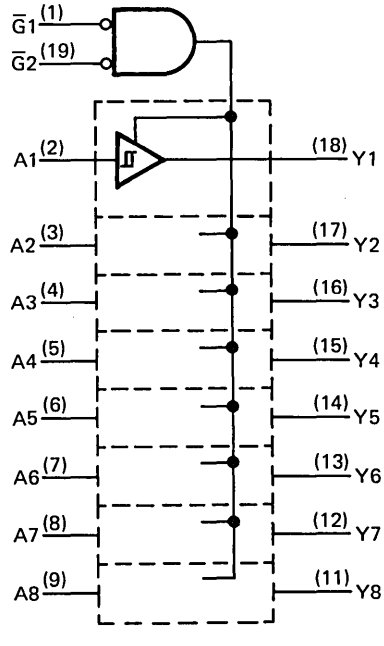
†These symbols are in accordance with IEEE Std 91/ANSI Y32.14 and current discussions in IEC and IEEE.

functional block diagram (positive logic)

'LS540



'LS541



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recommended operating conditions

PARAMETER	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−12			−15	mA
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

NOTE 1: Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
	Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = MIN		0.2	0.4		0.2	0.4		V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, I_{OH} = −3 mA	2.4	3.4		2.4	3.4		V
		V_{CC} = MIN, V_{IL} = 0.5 V,	V_{IH} = 2 V, I_{OH} = MAX	2			2			
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = V_{IL}max	V_O = 2.7 V			20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied		V_O = 0.4 V			−20			−20	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 7 V			0.1			0.1	mA
I_{IH}	High-level input current, any input	V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−0.2			−0.2	mA
I_{OS}	Short-circuit output current♦	V_{CC} = MAX		−40		−225	−40		−225	mA
I_{CC}	Supply current, Outputs high	V_{CC} = MAX, Outputs open	'LS540		13			13		mA
			'LS541		18			18		
	Outputs low		'LS540		24			24		
			'LS541		29			29		
	All outputs disabled		'LS540		30			30		
			'LS541		31			31		

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
♦Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		'LS540			'LS541			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 45 pF, See Note 2	R_L = 667 Ω,		9			12		ns
t_{PHL}	Propagation delay time, high-to-low-level output				12			12		ns
t_{PZL}	Output enable time to low level				20			20		ns
t_{PZH}	Output enable time to high level				15			25		ns
t_{PLZ}	Output disable time from low level	C_L = 5 pF, See Note 2	R_L = 667 Ω,		15			15		ns
t_{PHZ}	Output disable time from high level				10			10		ns

NOTE 2: Load circuit and voltage waveforms are shown on page 1-15.

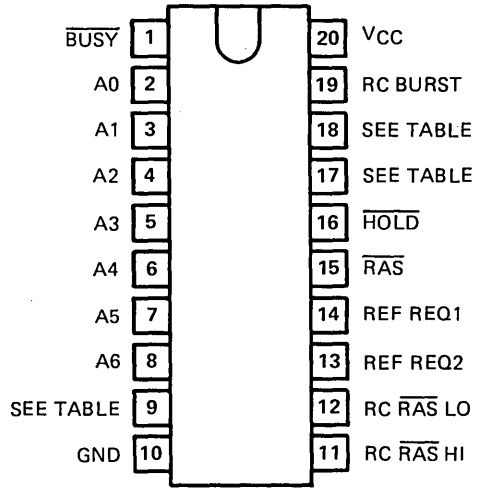
TYPES SN54LS600 THRU SN54LS603, SN74LS600 THRU SN74LS603 MEMORY REFRESH CONTROLLERS

AUGUST 1979

(TIM99600 THRU TIM99603)

- Controls Refresh Cycle of 4K, 16K, and 64K Dynamic RAMs
- Creates Static RAM Appearance
- Choice of Transparent, Cycle Steal, or Burst Refresh Modes
- 3-State Outputs Drive Bus Lines Directly
- Critical Times Are User RC-Programmable to Optimize System Performance

SN54LS' . . . J PACKAGE
SN74LS' . . . J OR N PACKAGE
(TOP VIEW)



SELECTION TABLE

DEVICE	REFRESH MODES	MEMORY SIZE	PIN ASSIGNMENTS		
			PIN 9	PIN 17	PIN 18
'LS600	Transparent, Burst	4K or 16K	4K/16K	NC	NC
'LS601	Transparent, Burst	64K	A7	NC	NC
'LS602	Cycle Steal, Burst	4K or 16K	4K/16K	READY	RC CYCLE STEAL
'LS603	Cycle Steal, Burst	64K	A7	READY	RC CYCLE STEAL

NC = No internal connection.

description

The 'LS600 thru 'LS603 memory refresh controllers contain one 8-bit synchronous counter, nine 3-state buffer drivers, four RC-controlled multivibrators, and other control circuitry on a monolithic chip. They are intended for use with RAS-only-refresh dynamic RAMs. These controllers have 3-state RAS and address outputs that are in the high-impedance state when no refresh is in progress. They become active approximately 30 nanoseconds after the REF REQ pins are taken high and remain active until about 30 nanoseconds after the refresh is complete.

operating modes

In the transparent refresh mode, row refresh cycles occur during inactive CPU-memory times so that, in most cases, the entire memory refresh sequence can be done "transparently" (without interrupting CPU operations). When the REF REQ pins are taken high to indicate an idle CPU/memory period, as many rows as possible are refreshed. A low level on BUSY signals the CPU to wait until the end of the current row refresh cycle before reinstating operations. When the RC time constant programmed at RC BURST indicates that the safe refresh time of the memory has been exceeded, the memory refresh controller will automatically signal the CPU for an emergency burst-mode refresh by taking HOLD low. The CPU must then take the REF REQ pins high and keep them at the level until HOLD goes high after all rows have been refreshed. The automatic burst refresh will be initiated by the refresh controller even when transparent or cycle-steal refresh operations are already in progress.

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PRODUCT PREVIEW

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Cycle-steal refresh is implemented by dividing the safe refresh time into equal segments and refreshing one row in each of those segments. The safe refresh time is programmed by the time constant at RC BURST and the segment time by the time constant at RC CYCLE STEAL. A low level at $\overline{\text{READY}}$ on the 'LS602 and 'LS603 indicates to the CPU to suspend operations for one memory cycle for a row refresh. In effect it "steals" one memory cycle from the CPU.

In all operating modes, the latch on the automatic burst mode circuit is reset at the end of every complete memory refresh cycle.

PIN FUNCTION TABLE

PIN	PIN NAME	FUNCTIONAL DESCRIPTION
1	$\overline{\text{BUSY}}$	Active output indicates to the CPU that a refresh cycle is in progress.
16	$\overline{\text{HOLD}}$	Active output should be a priority interrupt to the CPU for emergency burst refresh.
15	$\overline{\text{RAS}}$	3 state output row address strobe.
11	RC $\overline{\text{RAS}}$ HI	Timing node for high-level portion of $\overline{\text{RAS}}$. See Note 1.
12	RC $\overline{\text{RAS}}$ LO	Timing node for low-level portion of $\overline{\text{RAS}}$. See Note 1.
2–8	A0 thru A6	3 state output row address lines.
9	A7	MSB row address line for 'LS600 and 'LS603 (64K-bit memory controllers).
9	4K/$\overline{\text{16K}}$	A high input level disables the A6 row address line for 'LS600 and 'LS602. (The high level input makes the count chain 6 bits long while the low level makes the count chain 5 bits long.)
17	$\overline{\text{READY}}$	Interrupt to CPU for cycle steal refresh ('LS602 and 'LS603). No internal connection on 'LS600 and 'LS601.
18	RC CYCLE STEAL	Timing node that controls the $\overline{\text{READY}}$ output. See Note 1.
19	RC BURST	Timing node for burst refresh. See Note 1.
13, 14	REF REQ1, REF REQ2	High level on both pins starts and continues row refresh. Low on either pin inhibits refresh.
20, 10	V_{CC}, GND	5-V power supply and network ground pins.

NOTE 1: All timing nodes require a resistor to V_{CC} and a capacitor to GND. Programmed time is approximately equal to 0.24 RC.

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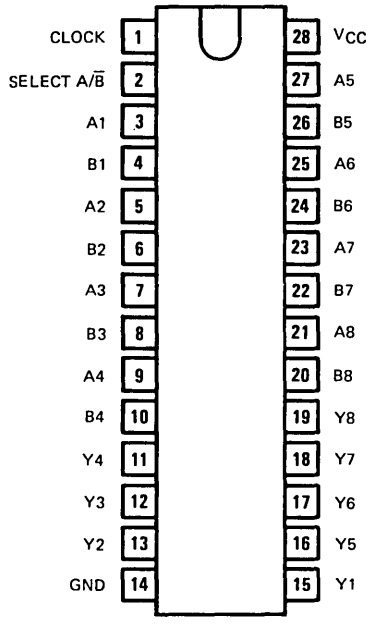
TYPES SN54LS604 THRU SN54LS607, SN74LS604 THRU SN74LS607 OCTAL 2-INPUT MULTIPLEXED LATCHES

BULLETIN NO. DL-S 12699, JULY 1979

(TIM99604 THRU TIM99607)

- Choice of Outputs:
  Three-State ('LS604, 'LS606)
  Open-Collector ('LS605, 'LS607)
- 16 D-Type Registers, One for each Data Input
- Multiplexer Selects Stored Data from Either A Bus or B Bus
- Application Oriented:
  Maximum Speed ('LS604, 'LS605)
  Giltch-Free Operation ('LS606, 'LS607)

SN54LS604 thru SN54LS607 . . . J PACKAGE
SN74LS604 thru SN74LS607 . . . J OR N PACKAGE
(TOP VIEW)



description

The 'LS604 through 'LS607 multiplexed latches are ideal for storing data from two input buses, A and B, and providing the output bus with stored data from either the A or B register.

The clock loads data on the positive-going (low-level to high-level) transition. The clock pin also controls the active and high-impedance states of the outputs. When the clock pin is low, the outputs are in the high-impedance or off state. When the clock pin is high, the outputs are enabled.

The 'LS604 and 'LS605 are optimized for high-speed operation. The 'LS606 and 'LS607 are especially designed to eliminate decoding voltage spikes.

These functions are ideal for interface from a 16-bit microprocessor to a 64K RAM board. The row and column addresses can be loaded as one word from the microprocessor and then multiplexed sequentially to the RAM during the time that RAS and CAS are active.

The SN54LS604 through SN54LS607 are characterized for operation over the full military temperature range of −55°C to 125°C; the SN74LS604 through SN74LS607 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS				OUTPUTS
A1-A8	B1-B8	SELECT A/B̄	CLOCK	Y1-Y8
A data	B data	L	↑	B data
A data	B data	H	↑	A data
X	X	X	L	Z or Off
X	X	L	H	B register stored data
X	X	H	H	A register stored data

H = high level (steady state)
L = low level (steady state)
X = irrelevant
Z = high-impedance state
Off = H if pull-up resistor is connected to open-collector output
↑ = transistion from low to high level

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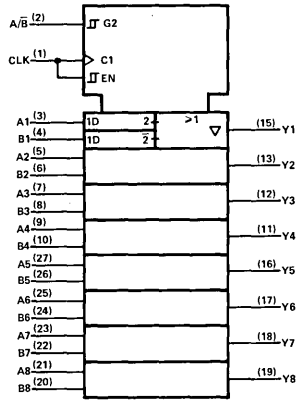
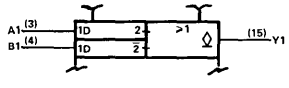
logic symbols†

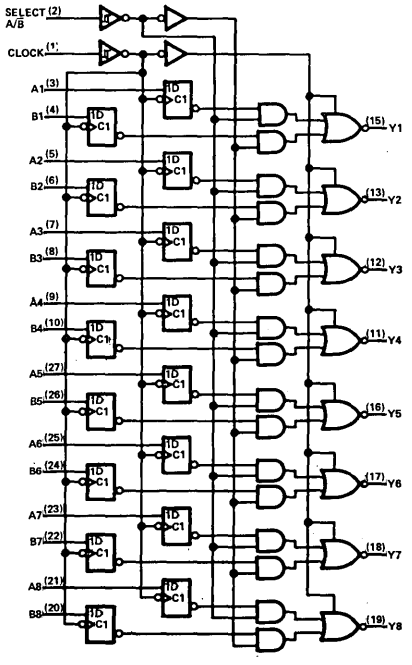
'LS604
'LS606



'LS605
'LS607



functional block diagram (positive logic)

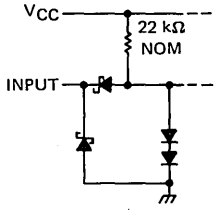


†These symbols are in accordance with IEEE Std 91/ANSI Y32.14 and current discussions in IEC and IEEE.

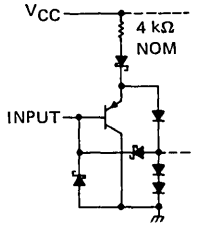
6

schematics of inputs and outputs

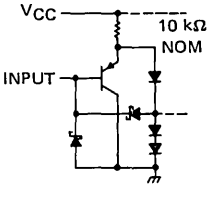
EQUIVALENT OF A AND B INPUTS



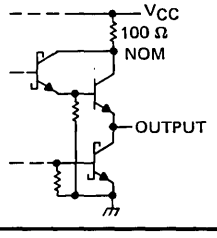
EQUIVALENT OF CLOCK INPUTS



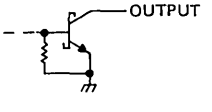
EQUIVALENT OF SELECT INPUTS



TYPICAL OF ALL OUTPUTS
('LS604, 'LS606)



TYPICAL OF ALL OUTPUTS
('LS605, 'LS607)



recommended operating conditions

	SN54LS604 SN54LS606			SN74LS604 SN74LS606			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−1			−2.6	mA
Low-level output current, I_{OL}			12			24	mA
Width of clock pulse, t_w	20			20			ns
Setup time, t_{su}	20↑			20↑			ns
Hold time, t_h	0↑			0↑			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

NOTE 1: Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			SN54LS604 SN54LS606			SN74LS604 SN74LS606			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, I_{OH} = MAX		2.4	3.1		2.4	3.1		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_{IL} = V_{IL} max,	V_{IH} = 2 V, V_O = 2.7 V				20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX, V_{IL} = V_{IL} max,	V_{IH} = 2 V, V_O = 0.4				−20			−20	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 7 V	A, B			0.1			0.1	mA
				CLK, SELECT			0.1			0.1	
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V	A, B			20			20	μA
				CLK, SELECT			20			20	
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V	A, B			−0.4			−0.4	mA
				CLK, SELECT			−0.2			−0.2	
I_{OS}	Short-circuit output current§	V_{CC} = MAX			−30		−130	−30		−130	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 2			55	70		55	70	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Note more than one output should be shorted at a time.
NOTE 2: I_{CC} is tested with all inputs grounded and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TEST CONDITIONS	'LS604			'LS606			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Select $A/\overline{B}$ (Data: A = H, B = L)	C_L = 45 pF, R_L = 667 Ω, See Note 3		15	25		36	50	ns
t_{PHL}				23	35		16	30	
t_{PLH}	Select $A/\overline{B}$ (Data: A = L, B = H)			31	45		22	35	ns
t_{PHL}				19	30		22	35	
t_{PZH}	Clock			19	30		27	40	ns
t_{PZL}				28	40		35	50	
t_{PHZ}	Clock	C_L = 5 pF, R_L = 667 Ω, See Note 3		20	30		20	30	ns
t_{PLZ}				15	25		15	25	

t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, low-to-high-level output
t_{ZH} ≡ output enable time to high level
t_{ZL} ≡ output enable time to low level
t_{HZ} ≡ output disable time from high level
t_{LZ} ≡ output disable time from low level
NOTE 3: Load circuits and voltage waveforms are shown on page 1-14.

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recommended operating conditions

	SN54LS605 SN54LS607			SN74LS605 SN74LS607			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			12			24	mA
Width of clock pulse, t_w	20			20			ns
Setup time, t_{su}	20↑			20↑			ns
Hold time, t_h	0↑			0↑			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

NOTE 1: Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			SN54LS605 SN54LS607			SN74LS605 SN74LS607			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, V_{OH} = 5.5 V				250			250	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL} max	V_{IH} = 2 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 7 V	A, B			0.1			0.1	mA
				CLK, SELECT			0.1			0.1	
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V	A, B			20			20	μA
				CLK, SELECT			20			20	
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V	A, B			−0.4			−0.4	mA
				CLK, SELECT			−0.2			−0.2	
I_{CC}	Supply current	V_{CC} = MAX,	See Note 2			40	60		40	60	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: I_{CC} is tested with all inputs grounded and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TEST CONDITIONS	'LS605			'LS607			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Select $A/\overline{B}$ (Data: A = H, B = L)	C_L = 45 pF, R_L = 667 Ω, See Note 3		28	40		51	70	ns
t_{PHL}				28	40		21	30	
t_{PLH}	Select $A/\overline{B}$ (Data: A = L, B = H)			39	60		28	40	ns
t_{PHL}				25	40		28	40	
t_{PLH}	Clock			27	40		30	45	ns
t_{PHL}				25	40		32	45	

t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, low-to-high-level output
NOTE 3: Load circuits and voltage waveforms are shown on page 1-14.

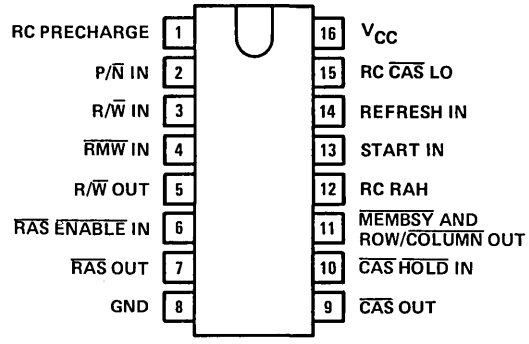
TYPES SN54LS608, SN74LS608
MEMORY CYCLE CONTROLLERS

AUGUST 1979

(TIM99608)

- Provides Correct Timing for Memory Cycles
  - Read Cycle
  - Write Cycle
  - Read-Modify-Write Cycle
  - RAS-Only Refresh Cycle
- Page or Normal Modes
- Stand-Alone Controller for CPU-to-Memory Interface
- Also Designed to be Part of a Three-Chip Set Consisting of 'LS600 thru 'LS603, 'LS604 thru 'LS607, and 'LS608
- $\overline{RAS}$ Output is 3-State to Share Bus With 'LS600 thru 'LS603
- Critical Times Are User RC-Programmable to Optimize System Performance

SN54LS608 . . . J PACKAGE
SN74LS608 . . . J OR N PACKAGE
(TOP VIEW)



description

The 'LS608 memory cycle controller is designed to interface between a microprocessor and dynamic RAM memories. It contains six RS latches, five D-type flip-flops, and more than 50 miscellaneous gates on a single chip. The 'LS608 combines maximum flexibility and ease of programming via RC nodes to allow optimum memory cycle performance.

The 'LS608 can operate as a stand-alone interface but is also designed to be part of a three-chip memory controller set. The user must select one of the 'LS600 thru 'LS603 refresh controllers and one of the 'LS604 thru 'LS607 multiplexers to use along with the 'LS608 memory cycle controller for complete dynamic RAM control.

After the user has selected and attached RC networks to pins 1, 12, and 15, the 'LS608 will deliver proper $\overline{RAS}$, $\overline{CAS}$, and READ/$\overline{WRITE}$ output signals to execute one memory cycle as the start input is switched from low to high. The actual cycle executed will depend upon steady-state input conditions of the 'LS608 as indicated in the table below.

MEMORY CYCLE	MODE	INPUT CONDITIONS						
		P/$\overline{N}$ IN	R/$\overline{W}$ IN	$\overline{RMW}$ IN	$\overline{RAS}$ $\overline{ENABLE}$ IN	$\overline{CAS}$ $\overline{HOLD}$ IN	START IN	REFRESH IN
READ	PAGE	H	H	H	L	H	↑	L
WRITE		H	L	H	L	H	↑	L
READ-MODIFY-WRITE		H	H	L	L	H	↑	L
READ	NORMAL	L	H	H	L	H	↑	L
WRITE		L	L	H	L	H	↑	L
READ-MODIFY-WRITE		L	H	L	L	H	↑	L
REFRESH	REFRESH	x	x	x	L	H	↑	H
EXTERNAL REFRESH		x	x	x	H	H	x	L

H = High, L= Low, x = Irrelevant, ↑ = low-to-high transition

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

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PIN FUNCTION TABLE

PIN	PIN NAME	FUNCTIONAL DESCRIPTION
1	RC PRECHARGE	User-programmable timing node* for precharge (CAS high and RAS high).
2	P/$\overline{N}$ IN	When high, enables page mode; when low, enables normal mode. The page mode read or write cycle holds $\overline{RAS}$ continuously low while $\overline{CAS}$ and column addresses are sequenced.
3	R/$\overline{W}$ IN	When high, initiates a read cycle (holds R/$\overline{W}$ OUT high). When low, initiates a write cycle (holds R/$\overline{W}$ OUT low). Pin 4 must be high.
4	$\overline{RMW}$ IN	When low, enables read-modify-write cycle. R/$\overline{W}$ IN must be high at the start of the RMW cycle.
5	R/$\overline{W}$ OUT	When high, indicates a read cycle is in progress. When low, indicates a write cycle is in progress. Normally ties to a $\overline{W}$ memory input in a system.
6	$\overline{RAS}$ $\overline{ENABLE}$ IN	When low, enables $\overline{RAS}$ output. When high, $\overline{RAS}$ is in the high-impedance or third state.
7	$\overline{RAS}$ OUT	3-state row-address-strobe output controlled by $\overline{RAS}$ $\overline{ENABLE}$ IN. In the three-chip controller set, the $\overline{RAS}$ output of the 'LS608 ties to the $\overline{RAS}$ output of the refresh controller ('LS600 thru 'LS603).
8	GND	Device and substrate ground.
9	$\overline{CAS}$ OUT	Column-address-strobe output.
10	$\overline{CAS}$ $\overline{HOLD}$ IN	When low, allows $\overline{CAS}$ to latch in low state. When high, latch is removed. Can be used to improve data retrieval during read cycle.
11	$\overline{MEMBSY}$ and ROW/$\overline{COLUMN}$ OUT	In a system where the 'LS608 is a stand-alone controller, this output indicates a memory busy condition to the microprocessor. When the 'LS608 is used as a part of a three-chip controller set, this pin ties to the SELECT A/$\overline{B}$ input of the multiplexer ('LS604 thru 'LS607) in addition to indicating a memory busy condition to the microprocessor.
12	RC RAH	User-programmable timing node* for row address hold time. (high level at $\overline{MEMBSY}$ and ROW/$\overline{COLUMN}$ OUT).
13	START IN	When changed from low to high, initiates a memory cycle.
14	REFRESH IN	When high, enables $\overline{RAS}$-only refresh cycle.
15	RC $\overline{CAS}$ LO	User-programmable timing node* for column-address-strobe low time.
16	V_{CC}	5-volt power supply terminal.

*All timing nodes require a resistor to V_{CC} and a capacitor to ground. Programmed time is approximately 0.24 RC.

TYPES SN54LS610 THRU SN54LS613, SN74LS610 THRU SN74LS613 MEMORY MAPPERS

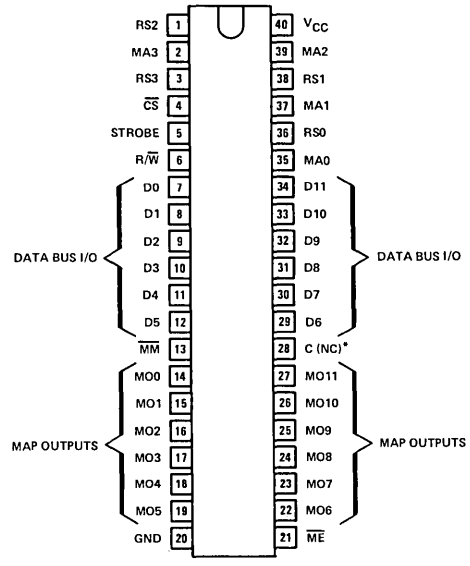
AUGUST 1979

(TIM99610 THRU TIM99613)

- Expands 4 Address Lines to 12 Address Lines
- Designed for Paged Memory Mapping
- Output Latches Provided on 'LS610 and 'LS611
- Choice of 3-State or Open-Collector Map Outputs
- Compatible with TMS 9900 and Other Microprocessors

DEVICE	OUTPUTS LATCHED	MAP OUTPUT TYPE
'LS610	Yes	3-State
'LS611	Yes	Open-Collector
'LS612	No	3-State
'LS613	No	Open-Collector

SN54LS' . . . J PACKAGE
SN74LS' . . . J OR N PACKAGE
(TOP VIEW)



*NOTE: Pin 28 has no internal connection on 'LS612 and 'LS613

description

These memory-mapper integrated circuits contain a 4-line to 16-line decoder, a 16-word by 12-bit RAM, 16 channels of 2-line to 1-line multiplexers, and other miscellaneous circuitry on a monolithic chip. The 'LS610 and 'LS611 also contain 12 latches with an enable control.

The memory mappers are designed to expand a microprocessor's memory address capability by eight bits. The four most-significant bits of the memory address bus (see Figure 1) can be used to select one of 16 map registers that contain 12 bits each. These 12 bits are presented to the system memory address bus through the map output buffers along with the unused memory address bits from the CPU. However, addressable memory space without reloading the map registers is the same as would be available with the memory mapper left out. The addressable memory space is increased only by periodically reloading the map registers from the data bus.

This configuration lends itself to memory utilization of 16 pages of $2^{(n-4)}$ registers each without reloading (n = number of address bits available from CPU).

These devices have four modes of operation (read, write, map, and pass). Data may be read from or loaded into the map register selected by the register select inputs (RS0 thru RS3) under control of R/$\overline{W}$ whenever chip select ($\overline{CS}$) is low. The data I/O takes place on the data bus D0 thru D7. The map operation will output the contents of the map register selected by the map address inputs (MA0 thru MA3) when $\overline{CS}$ is high and $\overline{MM}$ (map mode control) is low. The 'LS612 and 'LS613 output stages are transparent in this mode, while the 'LS610 and 'LS611 outputs may be transparent or latched. When $\overline{CS}$ and $\overline{MM}$ are both high (pass mode), the address bits on MA0 thru MA3 appear as the most significant bits at the map outputs (assuming appropriate latch enable) with low levels in the other bit positions.

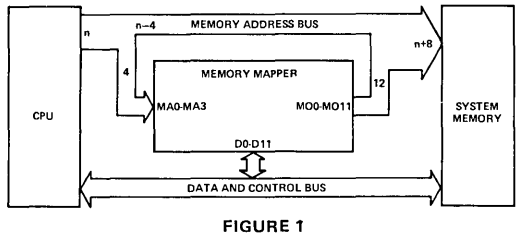


FIGURE 1

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PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TEXAS INSTRUMENTS
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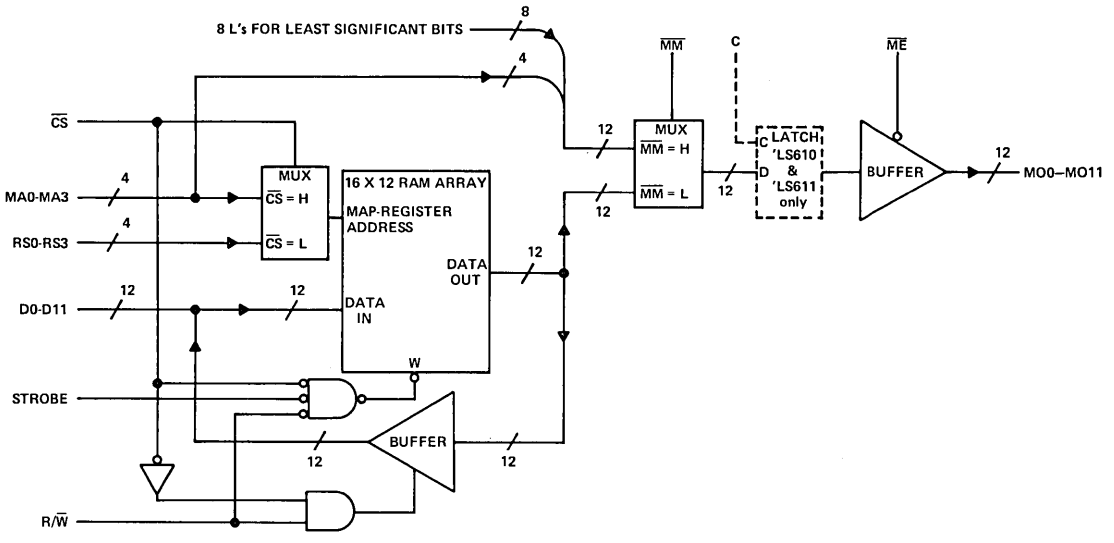
functional block diagram (positive logic)



PIN FUNCTION TABLE

PIN	PIN NAME	FUNCTIONAL DESCRIPTION
7–12, 29–34	D0 thru D11	I/O connections to data and control bus used for reading from and writing to the map register selected by RS0–RS3 when $\overline{CS}$ is low. Mode controlled by R/$\overline{W}$.
36, 38, 1, 3	RS0 thru RS3	Register select inputs for I/O operations.
6	R/$\overline{W}$	Read or write control used in I/O operations to select the condition of the data bus. When high, the data bus outputs are active for reading the map register. When low, the data bus is used to write into the register.
5	STROBE	Strobe input used to enter data into the selected map register during I/O operations.
4	$\overline{CS}$	Chip select input. A low input level selects the memory mapper (assuming more than one used) for an I/O operation.
35, 37, 39, 2	MA0 thru MA3	Map address inputs to select one of 16 map registers when in map mode ($\overline{MM}$ low and $\overline{CS}$ high).
14–19, 22–27	MO0 thru MO11	Map outputs. Present the map register contents to the system memory address bus in the map mode. In the pass mode, these outputs provide the map address data on MO8–MO11 and low levels on MO0–MO7.
13	$\overline{MM}$	Map mode input. When low, 12 bits of data are transferred from the selected map register to the map outputs. When high (pass mode), the 4 bits present on the map address inputs are passed to the map outputs.
21	$\overline{ME}$	Map enable for the map outputs. A low level allows the outputs to be active while a high input level puts the outputs at high impedance.
28	C	Latch enable input for the 'LS610 and 'LS611 (no internal connection for 'LS612 and 'LS613). A high level will transparently pass data to the map outputs. A low level will latch the outputs.
40, 20	V_{CC}, GND	5-V power supply and network ground (substrate) pins.

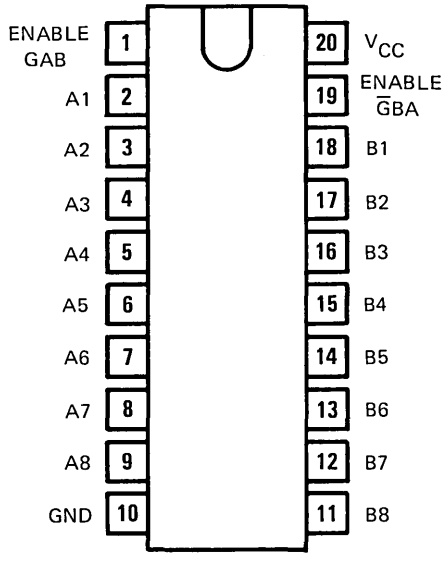
TYPES SN54LS620 THRU SN54LS623, SN74LS620 THRU SN74LS623 OCTAL BUS TRANSCEIVERS

BULLETIN NO. DL-S 12708, AUGUST 1979

- Bidirectional Bus Transceivers in High-Density 20-Pin Packages
- Local Bus-Latch Capability
- Hysteresis at Bus Inputs Improves Noise Margins
- Choice of True or Inverting Logic
- Choice of 3-State or Open-Collector Outputs

DEVICE	OUTPUT	LOGIC
'LS620	3-State	Inverting
'LS621	Open-Collector	True
'LS622	Open-Collector	Inverting
'LS623	3-State	True

SN54LS' . . . J PACKAGE
SN74LS' . . . J OR N PACKAGE
(TOP VIEW)



description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the enable inputs ($\overline{G}$BA and GAB).

The enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives the 'LS620 thru 'LS623 the capability to store data by simultaneous enabling of $\overline{G}$BA and GAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states. The 8-bit codes appearing on the two sets of buses will be identical for the 'LS621 and 'LS623 devices or complementary for the 'LS620 and 'LS622.

FUNCTION TABLE

ENABLE INPUTS		OPERATION	
$\overline{G}$BA	GAB	'LS620, 'LS622	'LS621, 'LS623
L	L	$\overline{B}$ data to A bus	B data to A bus
H	H	$\overline{A}$ data to B bus	A data to B bus
H	L	Isolation	Isolation
L	H	$\overline{B}$ data to A bus, $\overline{A}$ data to B bus	B data to A bus, A data to B bus

H = high level, L = low level, X = irrelevant

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54LS' . . . . . −55°C to 125°C
SN74LS' . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

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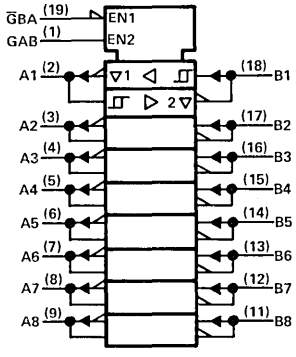
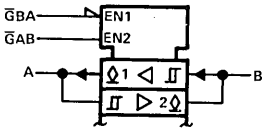
logic symbols†

'LS620



'LS621 (PARTIAL)



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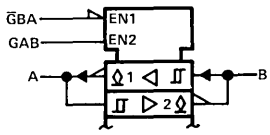

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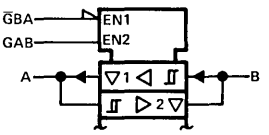
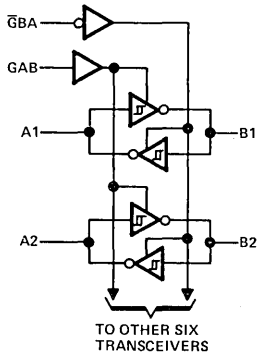


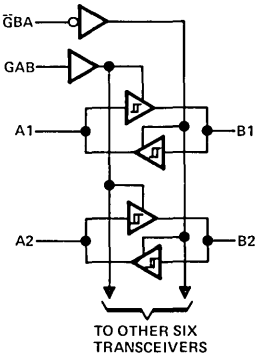
†These symbols are in accordance with IEEE Std 91/ANSI Y32.14 and current discussions in IEC and IEEE.

functional block diagrams (positive logic)

¼ 'LS620, ¼ 'LS622

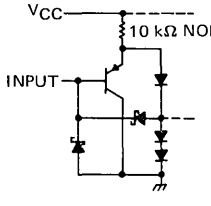


¼ 'LS621, ¼ 'LS623

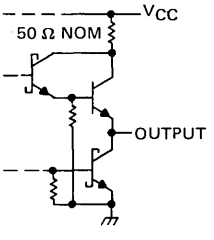


schematics of inputs and outputs

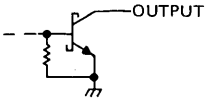
EQUIVALENT OF EACH INPUT



TYPICAL OF OUTPUTS OF 'LS620, 'LS623



TYPICAL OF OUTPUTS OF 'LS621, 'LS622



TEXAS INSTRUMENTS
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recommended operating conditions

PARAMETER	SN54LS620 SN54LS623			SN74LS620 SN74LS623			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−12			−15	mA
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

NOTE 1: Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS620 SN54LS623			SN74LS620 SN74LS623			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.5			0.6	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
	Hysteresis ($V_{T+} - V_{T-}$) A or B input		V_{CC} = MIN		0.1	0.4		0.2	0.4		V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OH} = −3 mA	2.4	3.4		2.4	3.4		V
				I_{OH} = MAX	2			2			
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied		V_{CC} = MAX, V_O = 2.7 V	$\overline{G}$ at 2 V,			20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied		V_{CC} = MAX, V_O = 0.4 V	$\overline{G}$ at 2 V,			−400			−400	μA
I_I	Input current at maximum input voltage	A or B	V_{CC} = MAX,	V_I = 5.5 V			0.1			0.1	mA
		$\overline{G}$BA or GAB		V_I = 7 V			0.1			0.1	
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current		V_{CC} = MAX,	V_I = 0.4 V			−400			−400	μA
I_{OS}	Short-circuit output current¶		V_{CC} = MAX		−40		−225	−40		−225	mA
I_{CC}	Total supply current	Outputs high	V_{CC} = MAX,	Outputs open		48	70		48	70	mA
		Outputs low				62	90		62	90	
		Outputs at Hi-Z				64	95		64	95	

†For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
¶Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics at V_{CC} = 5 V, T_A = 25°C

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS620			'LS623			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	A	B	C_L = 45 pF, R_L = 667 Ω, See Note 2		6	10		8	15	ns
		B	A			6	10		8	15	
t_{PHL}	Propagation delay time, high-to-low-level output	A	B			8	15		11	15	ns
		B	A			8	15		11	15	
t_{PZL}	Output enable time to low level	$\overline{G}$BA	A			31	40		31	40	ns
		GAB	B			31	40		31	40	
t_{PZH}	Output enable time to high level	$\overline{G}$BA	A			23	40		26	40	ns
		GAB	B			23	40		26	40	
t_{PLZ}	Output disable time from low level	$\overline{G}$BA	A	C_L = 5 pF, R_L = 667 Ω, See Note 2		15	25		15	25	ns
		GAB	B			15	25		15	25	
t_{PHZ}	Output disable time from high level	$\overline{G}$BA	A			15	25		15	25	ns
		GAB	B			15	25		15	25	

NOTE 2: For load circuits and voltage waveforms, see page 1-15.

recommended operating conditions

PARAMETER	SN54LS621 SN54LS622			SN74LS621 SN74LS622			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

NOTE 1: Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS621 SN54LS622			SN74LS621 SN74LS622			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.5			0.6	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
	Hysteresis ($V_{T+} - V_{T-}$) A or B input		V_{CC} = MIN		0.1	0.4		0.2	0.4		V
I_{OH}	High-level output current		V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, V_{OH} = 5.5 V			100			100	μA
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 7 V			0.1			0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current		V_{CC} = MAX,	V_I = 0.4 V			−400			−400	μA
I_{CC}	Total supply current	Outputs high	V_{CC} = MAX,	Outputs open		48	70		48	70	mA
		Outputs low				62	90		62	90	

†For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics at V_{CC} = 5 V, T_A = 25°C

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS621			'LS622			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	A	B	C_L = 45 pF, R_L = 667 Ω, See Note 2		17	25		19	25	ns
		B	A			17	25		19	25	
t_{PHL}	Propagation delay time, high-to-low-level output	A	B			16	25		14	25	ns
		B	A			16	25		14	25	
t_{PLH}	Output disable time from low level	$\overline{G}$BA	A			23	40		26	40	ns
		GAB	B			25	40		28	40	
t_{PHL}	Output disable time from high level	$\overline{G}$BA	A			34	50		43	60	ns
		GAB	B			37	50		39	60	

NOTE 2: For load circuits and voltage waveforms, see page 1-15.

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INCORPORATED
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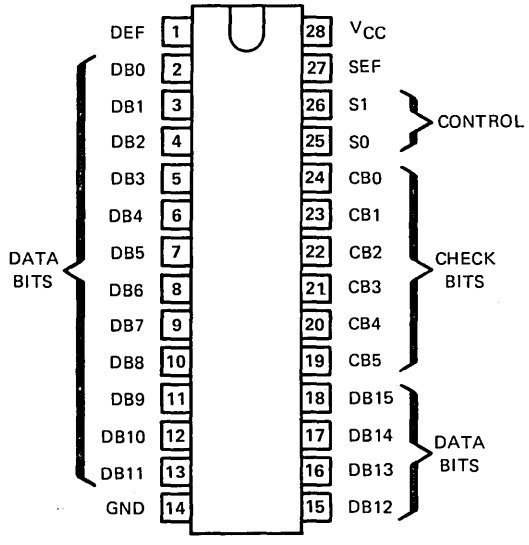
TYPES SN54LS630,SN54LS631,SN74LS630,SN74LS631
16-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

AUGUST 1979

(TIM99630, TIM99631)

- Detects and Corrects Single-Bit Errors
- Detects and Flags Dual-Bit Errors
- Fast Processing Times:
  - Write Cycle: Generates Checkword in 35 ns Typical
  - Read Cycle: Flags Errors in 40 ns Typical
- Power Dissipation 600 mW Typical
- Choice of Output Configurations:
  - 'LS630 . . . 3-State
  - 'LS631 . . . Open-Collector

SN54LS' . . . J PACKAGE
SN74LS' . . . J OR N PACKAGE
(TOP VIEW)



description

The 'LS630 and 'LS631 devices are 16-bit parallel error detection and correction circuits (EDACs) in 28-pin, 600-mil packages. They use a modified Hamming code to generate a 6-bit checkword from a 16-bit data word. This checkword is stored along with the data word during the memory write cycle. During the memory read cycle, the 22-bit words from memory are processed by the EDACs to determine if errors have occurred in memory.

Single-bit errors in the 16-bit data word are flagged and corrected.

Single-bit errors in the 6-bit checkword are flagged, and the CPU sends the EDAC through the correction cycle even though the 16-bit word is not in error. The correction cycle will simply pass along the original 16-bit word in this case and produce error syndrome bits to pinpoint the error-generating location.

Dual-bit errors are flagged but not corrected. These dual errors may occur in any two bits of the 22-bit word from memory (two errors in the 16-bit data word, two errors in the 6-bit checkword, or one error in each word).

The gross-error condition of all lows or all highs from memory will be detected. Otherwise, errors in three or more bits of the 22-bit word are beyond the capabilities of these devices to detect.

CONTROL FUNCTION TABLE

Memory Cycle	Control S1	Control S0	EDAC Function	Data I/O	Checkword I/O	Error Flags SEF	Error Flags DEF
WRITE	L	L	Generate Checkword	Input Data	Output Checkword	L	L
READ	L	H	Read Data & Checkword	Input Data	Input Checkword	L	L
READ	H	H	Latch & Flag Errors	Latch Data	Latch Checkword	Enabled	
READ	H	L	Correct Data Word & Generate Syndrome Bits	Output Corrected Data	Output Syndrome Bits	Enabled	

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PRODUCT PREVIEW

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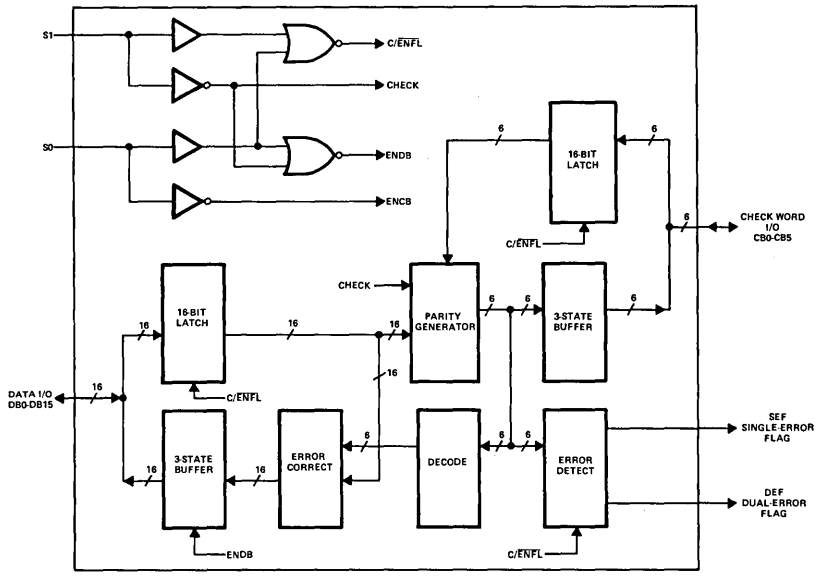
functional block diagram



ERROR FUNCTION TABLE

Total Number of Errors		Error Flags		Data Correction
16-Bit Data	6-Bit Checkword	SEF	DEF	
0	0	L	L	Not Applicable
1	0	H	L	Correction
0	1	H	L	Correction
1	1	H	H	Interrupt
2	0	H	H	Interrupt
0	2	H	H	Interrupt

In order to be able to determine whether the data from the memory is acceptable to use as presented to the bus, the EDAC must be strobed to enable the error flags and the flags will have to be tested for the zero condition.

The first case in the error function table represents the normal, no-error condition. The CPU sees lows on both flags. The next two cases of single-bit errors require data correction. Although the EDAC can discern the single checkbit error and ignore it, the error flags are identical to the single error in the 16-bit data word. The CPU will ask for data correction in both cases. An interrupt condition to the CPU results in each of the last three cases, where dual errors occur.

error detection and correction details

During a memory write cycle, six check bits (CB0-CB5) are generated by eight-input parity generators using the data bits as defined below. During a memory read cycle, the 6-bit checkword is retrieved along with the actual data.

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CHECKWORD	16-BIT DATA WORD															
BIT	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CB0	x	x		x	x				x	x	x			x		
CB1	x		x	x		x	x		x			x			x	
CB2		x	x		x	x		x		x			x			x
CB3	x	x	x				x	x			x	x	x			
CB4				x	x	x	x	x						x	x	x
CB5									x	x	x	x	x	x	x	x

The six check bits are parity bits derived from the matrix of data bits as indicated by "x" for each bit.

Error detection is accomplished as the 6-bit checkword and the 16-bit data word from memory are applied to internal parity generators/checkers. If the parity of all six groupings of data and check bits are correct, it is assumed that no error has occurred and both error flags will be low. (It should be noted that the sense of two of the check bits, bits CB0 and CB1, is inverted to ensure that the gross-error condition of all lows and all highs is detected.)

If the parity of one or more of the check groups is incorrect, an error has occurred and the proper error flag or flags will be set high. Any single error in the 16-bit data word will change the sense of exactly three bits of the 6-bit checkword. Any single error in the 6-bit checkword changes the sense of only that one bit. In either case, the single error flag will be set high while the dual error flag will remain low.

Any two-bit error will change the sense of an even number of check bits. The two-bit error is not correctable since the parity tree can only identify single-bit errors. Both error flags are set high when any two-bit error is detected.

Three or more simultaneous bit errors can fool the EDAC into believing that no error, a correctable error, or an uncorrectable error has occurred and produce erroneous results in all three cases.

Error correction is accomplished by identifying the bad bit and inverting it. Identification of the erroneous bit is achieved by comparing the 16-bit data word and 6-bit checkword from memory with the new checkword with one (checkword error) or three (data word error) inverted bits.

As the corrected word is made available on the data word I/O port, the checkword I/O port presents a 6-bit syndrome error code. This syndrome code can be used to identify the bad memory chip.

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ERROR SYNDROME TABLE

ERROR LOCATION	SYNDROME ERROR CODE					
	CB0	CB1	CB2	CB3	CB4	CB5
DB0	L	L	H	L	H	H
DB1	L	H	L	L	H	H
DB2	H	L	L	L	H	H
DB3	L	L	H	H	L	H
DB4	L	H	L	H	L	H
DB5	H	L	L	H	L	H
DB6	H	L	H	L	L	H
DB7	H	H	L	L	L	H
DB8	L	L	H	H	H	L
DB9	L	H	L	H	H	L
DB10	L	H	H	L	H	L
DB11	H	L	H	L	H	L
DB12	H	H	L	L	H	L
DB13	L	H	H	H	L	L
DB14	H	L	H	H	L	L
DB15	H	H	L	H	L	L
CB0	L	H	H	H	H	H
CB1	H	L	H	H	H	H
CB2	H	H	L	H	H	H
CB3	H	H	H	L	H	H
CB4	H	H	H	H	L	H
CB5	H	H	H	H	H	L
NO ERROR	H	H	H	H	H	H

applications

It is possible to design the error detection and correction function using a single EDAC. Even though most semiconductor memories have separate inputs and outputs, the EDAC's data and checkbit pins are I/O combinations. But wired-AND logic becomes mandatory, and a fairly complex system timing is required for both bus logic and controlling the EDAC. This scheme becomes difficult to implement both in terms of board layout and timing. System performance is also adversely affected. See Figure 1.

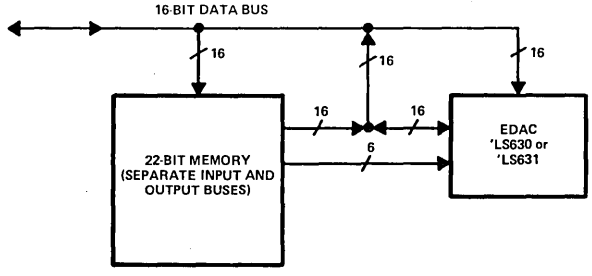
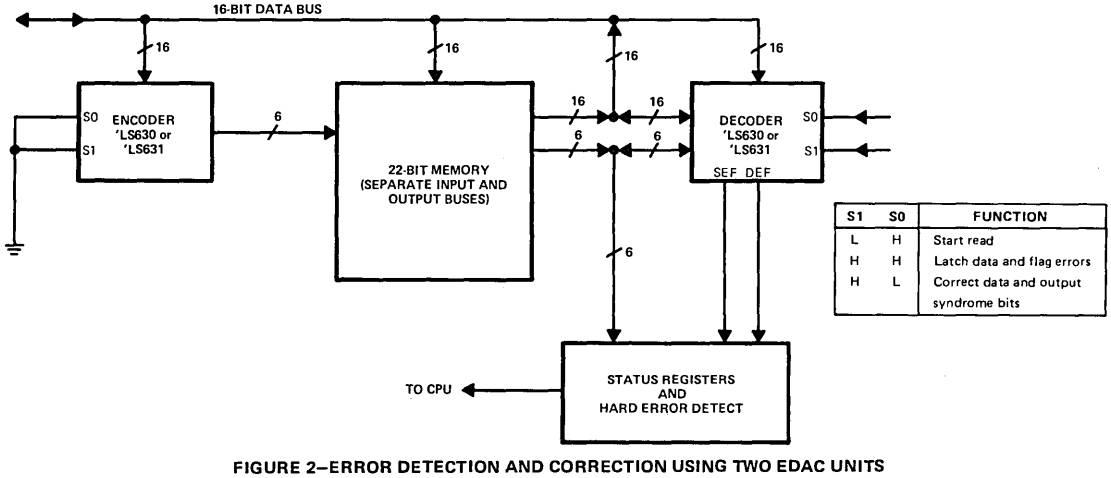


FIGURE 1–ERROR DETECTION AND CORRECTION USING A SINGLE EDAC UNIT

Optimized systems can be implemented using two EDACs in parallel. One of the units is used strictly as an encoder during the memory write cycle. Both controls S0 and S1 are grounded. This encoder chip will generate the 6-bit check-word for memory storage along with the 16-bit data.

The second of the two EDACs will be used as a decoder during the memory read cycle. This decoder chip does require timing pulses for proper operation. Control S0 is set low and S1 high as the memory read cycle begins. After the memory output data is valid, the control S0 input is moved from the low to a high. This low-to-high transition latches the 22-bit word from memory into internal registers of this second EDAC and enables the two error flags. If no error occurs, the CPU can accept the 16-bit word directly from memory. If a single error has occurred, the CPU must move the control S1 input from the high to a low to output corrected data and the error syndrome bits. Any dual error should be an interrupt condition.

In most applications, status registers will be used to keep tabs on error flags and error syndrome bits. If repeated patterns of error flags and syndrome bits occur, the CPU will be able to recognize these symptoms as a "hard" error. The syndrome bits can be used to pinpoint the faulty memory chip. See Figure 2.



S1	S0	FUNCTION
L	H	Start read
H	H	Latch data and flag errors
H	L	Correct data and output syndrome bits

FIGURE 2–ERROR DETECTION AND CORRECTION USING TWO EDAC UNITS

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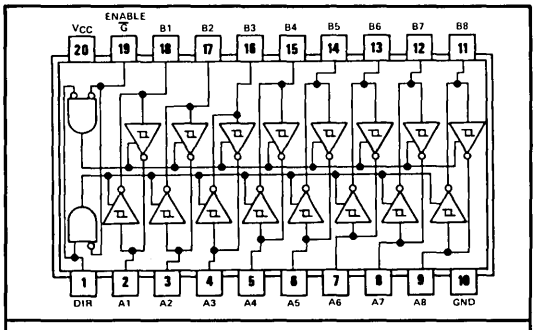
TYPES SN54LS640 THRU SN54LS645, SN74LS640 THRU SN74LS645 OCTAL BUS TRANSCEIVERS

BULLETIN NO. DL-S 12674, APRIL 1979

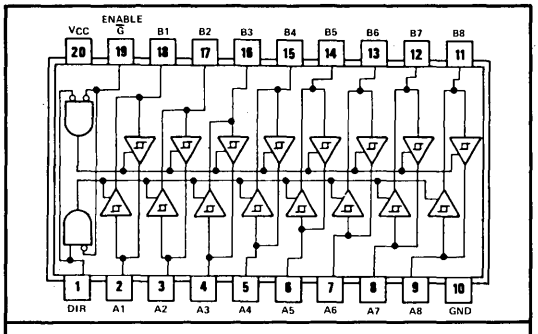
- SN74LS64X-1 Versions Rated at I_{OL} of 48 mA
- Bi-directional Bus Transceivers in High-Density 20-Pin Packages
- Hysteresis at Bus Inputs Improves Noise Margins
- Choice of True or Inverting Logic
- Choice of 3-State or Open-Collector Outputs

SN54LS640, SN54LS642 . . . J PACKAGE
SN74LS640, SN74LS642 . . . J OR N PACKAGE
(TOP VIEW)



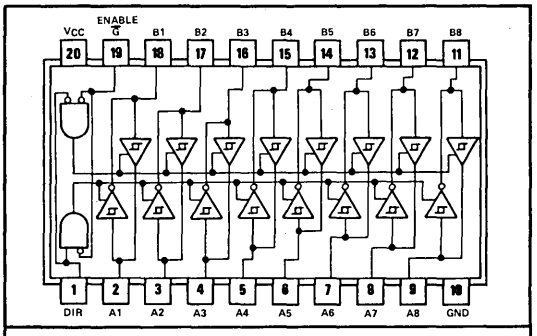
positive logic: see function table

SN54LS641, SN54LS645 . . . J PACKAGE
SN74LS641, SN74LS645 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

SN54LS643, SN54LS644 . . . J PACKAGE
SN74LS643, SN74LS644 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so that the buses are effectively isolated.

DEVICE	OUTPUT	LOGIC
'LS640	3-State	Inverting
'LS641	Open-Collector	True
'LS642	Open-Collector	Inverting
'LS643	3-State	True and inverting
'LS644	Open-Collector	True and inverting
'LS645	3-State	True

FUNCTION TABLE

CONTROL INPUTS		OPERATION		
$\overline{G}$	DIR	'LS640 'LS642	'LS641 'LS645	'LS643 'LS644
L	L	$\overline{B}$ data to A bus	B data to A bus	B data to A bus
L	H	$\overline{A}$ data to B bus	A data to B bus	$\overline{A}$ data to B bus
H	X	Isolation	Isolation	Isolation

H = high level, L = low level, X = irrelevant

absolute maximum ratings

Same as SN54LS245 and SN74LS245 maximum ratings on page 6-13.

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recommended operating conditions

PARAMETER	SN54LS640 SN54LS643 SN54LS645			SN74LS640 SN74LS643 SN74LS645			SN74LS640–1 SN74LS643–1 SN74LS645–1			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	4.75	5	5.25	V
High-level output current, I_{OH}			−12			−15			−15	mA
Low-level output current, I_{OL}			12			24			48	mA
Operating free-air temperature, T_A	−55		125	0		70	0		70	°C

NOTE 1: Voltage values are with respect to the network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS640 SN54LS643 SN54LS645			SN74LS640 SN74LS643 SN74LS645			SN74LS640–1 SN74LS643–1 SN74LS645–1			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			2			V
V_{IL}	Low-level input voltage						0.5			0.6			0.6	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5			−1.5	V
	Hysteresis ($V_{T+} - V_{T-}$) A or B input		V_{CC} = MIN		0.1	0.4		0.2	0.4		0.2	0.4		V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OH} = −3 mA	2.4	3.4		2.4	3.4		2.4	3.4		V
				I_{OH} = MAX	2			2			2			
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5		0.35	0.5	
				I_{OL} = 48 mA								0.4	0.5	
I_{OZH}	Off-state output current, high-level voltage applied		V_{CC} = MAX, V_O = 2.7 V	$\overline{G}$ at 2 V,			20			20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied		V_{CC} = MAX, V_O = 0.4 V	$\overline{G}$ at 2 V,			−400			−400			−400	μA
I_I	Input current at maximum input voltage	A or B	V_{CC} = MAX	V_I = 5.5 V			0.1			0.1			0.1	mA
		DIR or $\overline{G}$		V_I = 7 V			0.1			0.1			0.1	
I_{IH}	High-level input current		V_{CC} = MAX,	V_{IH} = 2.7 V			20			20			20	μA
I_{IL}	Low-level input current		V_{CC} = MAX,	V_{IL} = 0.4 V			−400			−400			−400	μA
I_{OS}	Short-circuit output current¶		V_{CC} = MAX		−40		−225	−40		−225	−40		−225	mA
I_{CC}	Total supply current	Outputs high	V_{CC} = MAX,	Outputs open		48	70		48	70		48	70	mA
		Outputs low				62	90		62	90		62	90	
		Outputs at Hi-Z				64	95		64	95		64	95	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
¶Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

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switching characteristics at V_{CC} = 5 V, T_A = 25°C

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS640, 'LS640–1			'LS643, 'LS643–1			'LS645, 'LS645–1			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	A	B	C_L = 45 pF, R_L = 667 Ω, See Note 2		6	10		6	10		8	15	ns
		B	A			6	10		8	15		8	15	
t_{PHL}	Propagation delay time, high-to-low-level output	A	B			8	15		9	15		11	15	ns
		B	A			8	15		11	15		11	15	
t_{PZL}	Output enable time to low level	$\overline{G}$, DIR	A			31	40		32	45		31	40	ns
		$\overline{G}$, DIR	B			31	40		32	45		31	40	
t_{PZH}	Output enable time to high level	$\overline{G}$, DIR	A			23	40		27	40		26	40	ns
		$\overline{G}$, DIR	B			23	40		23	40		26	40	
t_{PLZ}	Output disable time from low level	$\overline{G}$, DIR	A	C_L = 5 pF, R_L = 667 Ω, See Note 2		15	25		15	25		15	25	ns
		$\overline{G}$, DIR	B			15	25		15	25		15	25	
t_{PHZ}	Output disable time from high level	$\overline{G}$, DIR	A			15	25		15	25		15	25	ns
		$\overline{G}$, DIR	B			15	25		15	25		15	25	

NOTE 2: For load circuits and voltage waveforms, see page 1-15.

schematics of inputs and outputs

EQUIVALENT OF EACH INPUT

TYPICAL OF OUTPUTS

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TYPICAL CHARACTERISTICS

SN54LS'
INVERTING OUTPUT VOLTAGE
vs
INPUT VOLTAGE

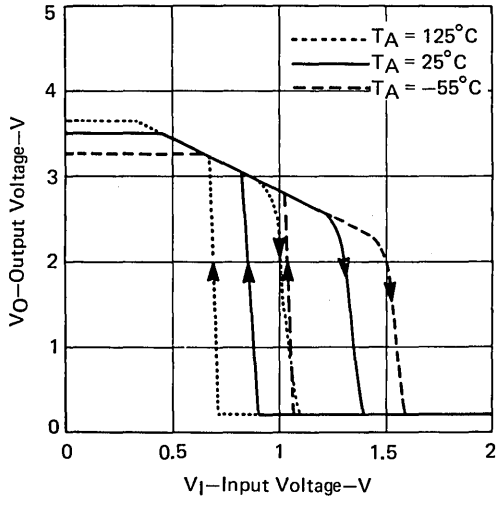

FIGURE 1

SN74LS'
INVERTING OUTPUT VOLTAGE
vs
INPUT VOLTAGE

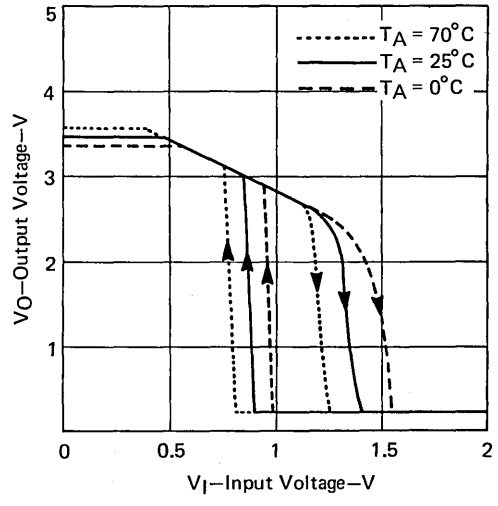

FIGURE 2

SN54LS'
NONINVERTING OUTPUT VOLTAGE
vs
INPUT VOLTAGE

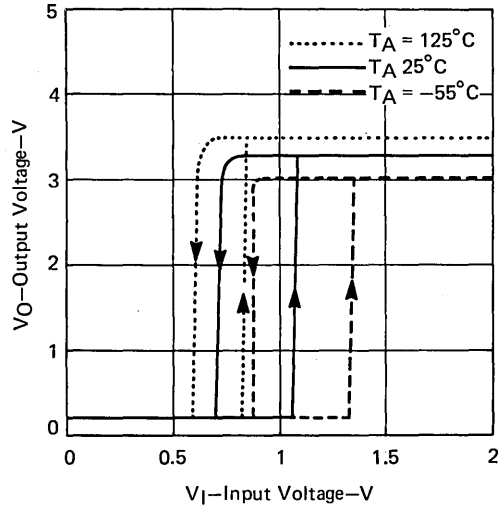

FIGURE 3

SN74LS'
NONINVERTING OUTPUT VOLTAGE
vs
INPUT VOLTAGE

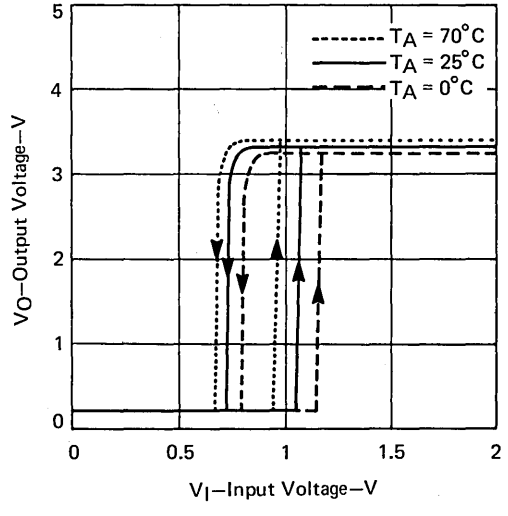

FIGURE 4

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recommended operating conditions

PARAMETER	SN54LS641 SN54LS642 SN54LS644			SN74LS641 SN74LS642 SN74LS644			SN74LS641–1 SN74LS642–1 SN74LS644–1			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5			5.5	V
Low-level output current, I_{OL}			12			24			48	mA
Operating free-air temperature, T_A	−55		125	0		70	0		70	°C

NOTE 1 : Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS641 SN54LS642 SN54LS644			SN74LS641 SN74LS642 SN74LS644			SN74LS641–1 SN74LS642–1 SN74LS644–1			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			2			V
V_{IL}	Low-level input voltage					0.5			0.6			0.6	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5			−1.5	V
	Hysteresis ($V_{T+} - V_{T-}$) A or B input	V_{CC} = MIN		0.1	0.4		0.2	0.4		0.2	0.4		V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, V_{OH} = 5.5 V			100			100			100	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4		0.25	0.4	V
			I_{OL} = 24 mA					0.35	0.5		0.35	0.5	
			I_{OL} = 48 mA								0.4	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 7 V			0.1			0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V			20			20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−400			−400			−400	μA
I_{CC}	Total Supply Current, Outputs high	V_{CC} = MAX,	Outputs open		48	70		48	70		48	70	mA
	Total Supply Current, Outputs low				62	90		62	90		62	90	
	Total Supply Current, Outputs at Hi-Z				64	95		64	95		64	95	

†For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions.
‡All Typical values are at V_{CC} = 5 V, T_A = 25°C.

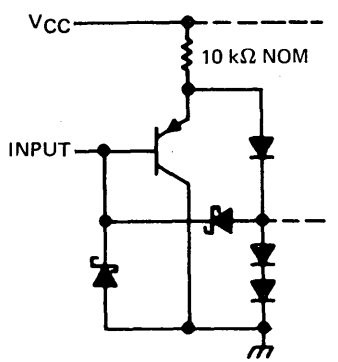
switching characteristics at V_{CC} = 5 V, T_A = 25°C

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS641, 'LS641–1			'LS642, 'LS642–1			'LS644, 'LS644–1			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	A	B	C_L = 45 pF, R_L = 667 Ω, See Note 2		17	25		19	25		17	25	ns
		B	A			17	25		19	25		19	25	
t_{PHL}	Propagation delay time, high-to-low-level output	A	B			16	25		14	25		14	25	ns
		B	A			16	25		14	25		16	25	
t_{PLH}	Output disable time from low level	$\overline{G}$, DIR	A			23	40		26	40		26	40	ns
		$\overline{G}$, DIR	B			25	40		28	40		25	40	
t_{PHL}	Output disable time from high level	$\overline{G}$, DIR	A			34	50		43	60		43	60	ns
		$\overline{G}$, DIR	B			37	50		39	60		37	50	

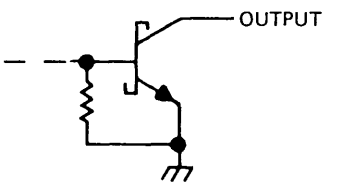
NOTE 2: For load circuits and voltage waveforms, see page 1-15.

schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



TYPICAL OF OUTPUTS



TEXAS INSTRUMENTS
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TYPES SN54S740, SN54S741, SN54S744, SN74S740, SN74S741, SN74S744 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

BULLETIN NO. DL-S 12711, JUNE 1979 – REVISED AUGUST 1979

	I_{OH} Typical (Source Current)	I_{OL} Typical (Sink Current)		Typical Propagation Delay Times	Typical Enable Times	Typical Disable Times
SN54S'	−12 mA	48 mA	'S740	4 ns	10 ns	6 ns
			'S741	6 ns	10 ns	11 ns
SN74S'	−15 mA	64 mA	'S744	6 ns	10 ns	10 ns

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- P-N-P Inputs Reduce D-C Loading
- Typical Input and Output Capacitances ⩽ 10 pF

description

These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{G}$ (active-low output control) inputs, and complementary G and $\overline{G}$ inputs. These devices feature high fan-out, improved fan-in, and less than 10-picofarad capacitance at inputs and outputs.

'S740 FUNCTION TABLE

$1\overline{G}$	$2\overline{G}$	1Y OUTPUTS	2Y OUTPUTS
H	H	Z	Z
H	L	Z	Enabled (Inverting)
L	H	Enabled (Inverting)	Z
L	L	Enabled (Inverting)	Enabled (Inverting)

'S741 FUNCTION TABLE

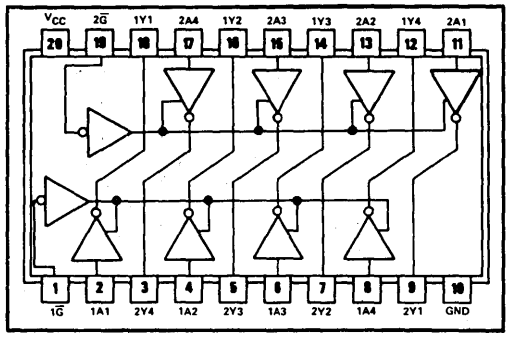
$1\overline{G}$	2G	1Y OUTPUTS	2Y OUTPUTS
H	H	Z	Enabled
H	L	Z	Z
L	H	Enabled	Enabled
L	L	Enabled	Z

'S744 FUNCTION TABLE

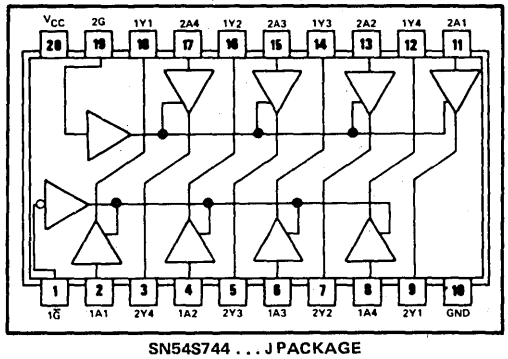
$1\overline{G}$	$2\overline{G}$	1Y OUTPUTS	2Y OUTPUTS
H	H	Z	Z
H	L	Z	Enabled
L	H	Enabled	Z
L	L	Enabled	Enabled

Z ≡ high impedance (output off)

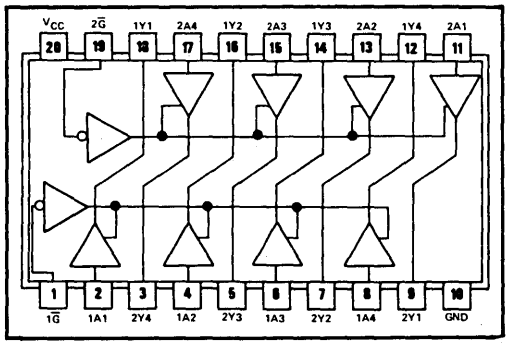
SN54S740 . . . J PACKAGE
SN74S740 . . . J OR N PACKAGE
(TOP VIEW)



SN54S741 . . . J PACKAGE
SN74S741 . . . J OR N PACKAGE
(TOP VIEW)



SN54S744 . . . J PACKAGE
SN54S744 . . . J OR N PACKAGE
(TOP VIEW)



6

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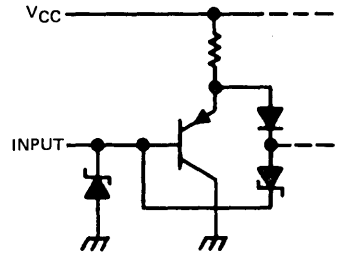
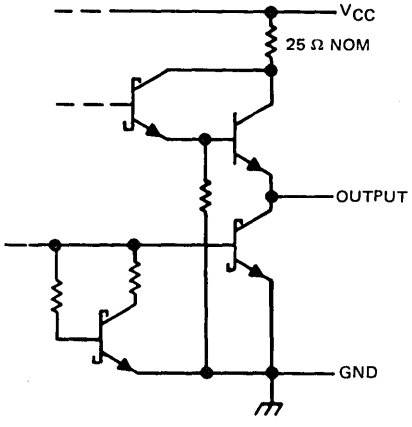
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54LS' . . . . . −55°C to 125°C
SN74LS' . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

PARAMETER	SN54S'			SN74S'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−12			−15	mA
Low-level output current, I_{OL}			48			64	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

NOTE 1: Voltage values are with respect to network ground terminal.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		'S740			'S741, 'S744			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = −1 mA	2.4			2.4			V
			V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = −3 mA	2.4	3.4		2.4	3.4		
			V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = MAX	2.4			2.4			
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = MAX			0.55			0.55	V
I_{OZH}	Off-state output current, high-level voltage applied		V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = 0.8 V	V_O = 2.4 V			50			50	μA
I_{OZL}	Off-state output current, low-level voltage applied			V_O = 0.5 V			−50			−50	
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current, any input		V_{CC} = MAX,	V_I = 2.7 V			50			50	μA
I_{IL}	Low-level input current	Any A	V_{CC} = MAX,	V_I = 0.5 V			−250			−250	μA
		Any G or $\overline{G}$					−250			−250	μA
I_{OS}	Short-circuit output current♦		V_{CC} = MAX		−50		−225	−50		−225	mA
I_{CC}	Supply current	Outputs high	V_{CC} = MAX, Outputs open	SN54S'		25	60		60	90	mA
				SN74S'		23	60		55	90	
		Outputs low		SN54S'		100	145		118	160	
				SN74S'		97	140		111	155	
		Outputs disabled		SN54S'		69	110		72	110	
				SN74S'		64	100		68	100	

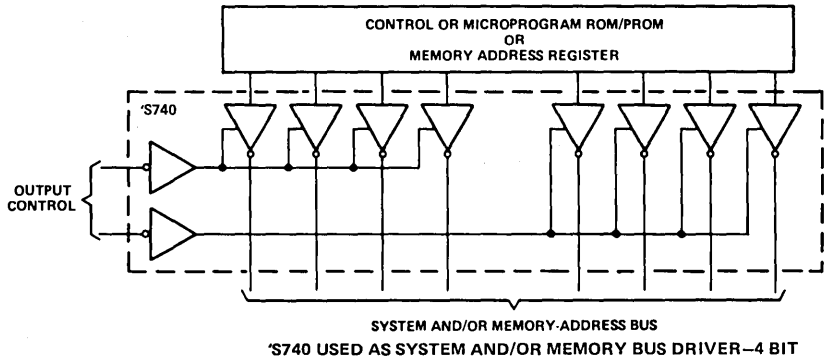
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
♦Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characterisitics, V_{CC} = 5 V, T_A = 25°C

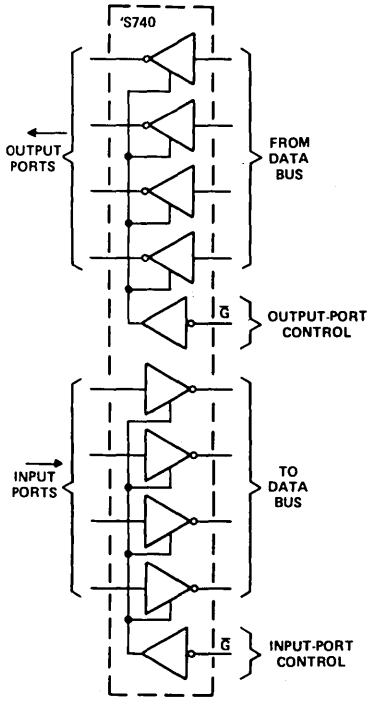
PARAMETER	TEST CONDITIONS		'S740			'S741			'S744			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	C_L = 50 pF, See Note 2	R_L = 90 Ω,		4	7		6	9		6	9	ns
t_{PHL}				4	7		5	8		5	8	ns
t_{PZL}				10	15		10	16		10	15	ns
t_{PZH}				7	11		8	13		7	11	ns
t_{PLZ}	C_L = 5 pF, See Note 2	R_L = 90 Ω,		6	11		11	18		10	16	ns
t_{PHZ}				3	6		5	9		3	6	ns

NOTE 2: Load circuit and voltage waveforms are shown on page 1-14.
t_{PLH} ≡ Propagation delay time, low-to-high-level input
t_{PHL} ≡ Propagation delay time, high-to-low-level input
t_{PZL} ≡ Output enable time to low level
t_{PZH} ≡ Output enable time to high level
t_{PLZ} ≡ Output disable time from low level
t_{PHZ} ≡ Output disable time from high level

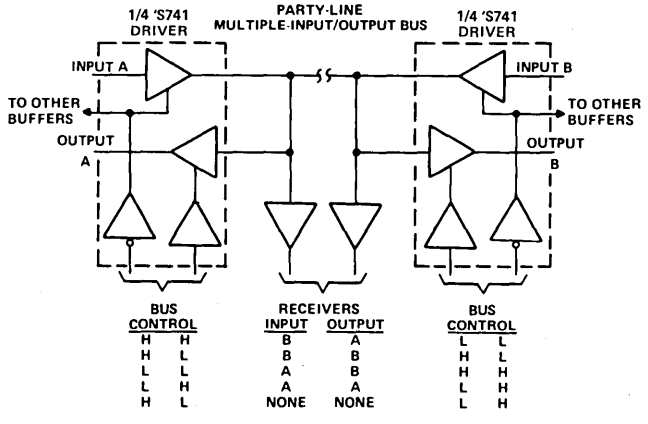
TYPICAL APPLICATION DATA



'S740 USED AS SYSTEM AND/OR MEMORY BUS DRIVER—4 BIT ORGANIZATION CAN BE APPLIED TO HANDLE BINARY OR BCD



INDEPENDENT 4-BIT BUS DRIVERS/RECEIVERS IN A SINGLE PACKAGE



PARTY-LINE BUS SYSTEM WITH MULTIPLE INPUTS, OUTPUTS, AND RECEIVERS

External resistance between any input and ground or V_{CC} must not exceed 40 kΩ.

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SBP 9708
Parallel-Byte
Multiplier

SBP 9708 8-BIT-BY-8-BIT PARALLEL BYTE MULTIPLIER

FEATURES

- Signed or Unsigned 8-Bit Multiplier Produces 16-Bit Product
- On-Chip Latches Simplify System Design
- Transparent or Latched (Pipelined) Operating Modes
- Bus Compatible With Popular 8-Bit Microprocessors
- Supports Systems With Bus Data Rates Up to 4 MHz
- Standard 16-Pin Packaging Maximizes Boards Density
- Compatible With TTL and Low-Threshold MOS
- Choice of Ambient Temperature Performance Ranges:

  SBP 9708M . . . –55°C to 125°C
  SBP 9708E . . . –40°C to 85°C
  SBP 9708C . . . 0°C to 70°C

DESCRIPTION

This 8-bit by 8-bit I^2L parallel multiplier provides a 16-bit signed or unsigned product resulting from two signed 2's complement or unsigned 8-bit bytes. Designed specifically to achieve the cost-effectiveness needed for microprocessor based systems, the SBP 9708 combines the static logic of I^2L with a pin-efficient organization to make available a low-cost byte-oriented peripheral multiplier that can improve CPU throughput rates and reduce software overhead significantly over iterative algorithms.

Sequential byte-parallel operations can be performed in either a transparent or latched (pipelined) multiply mode. In the transparent mode, the multiplier/multiplicand latches accept the two operators, the 16-bit product bypasses the output latches and is available in two of the multiplier array bytes directly from the 8-bit 4-to-1 multiplexer. This mode is best-suited when the need is for fast, isolated multiply occurrences. In the latched mode, during the first write cycle, the multiplier latch accepts new data and the previous array result is strobed into the two product latches. On the next write cycle, the multiplicand is latched. In this mode, designed for multiply-intensive systems, pipelining allows sequential multiplication operations carried out at a rate 50% faster than in the transparent mode.

In addition to single line controls for operating mode (MODE) and sign-bit handling (S/$\overline{U}$), active-low chip-select ($\overline{CS}$) and read-write (R/$\overline{W}$) inputs are configured to make the multiplier addressable from hardware and software as either a memory-mapped, or an I/O-mapped peripheral. Sequential parallel byte loading (write) and result output (reading) are steered to or from the storage latches by a single most-significant byte/least-significant byte (M/$\overline{L}$) control input.

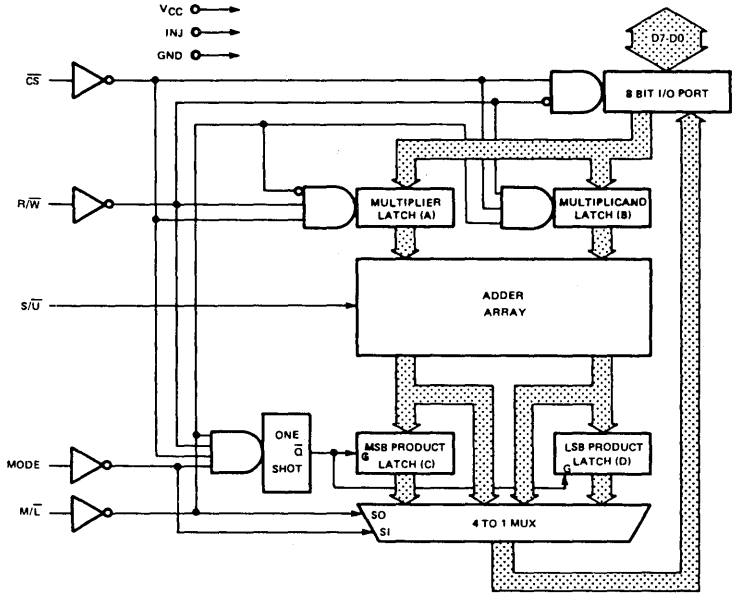
All versions are TTL and low-threshold MOS compatible. Output pullup resistors are provided on chip to minimize external components.

CONTROL FUNCTION TABLE

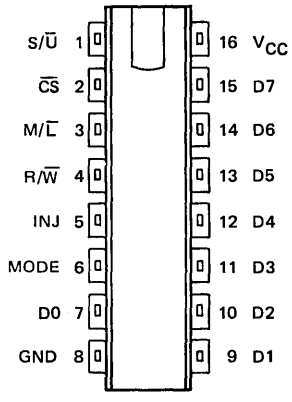
MODE	INPUT				FUNCTION
	$\overline{CS}$	R/$\overline{W}$	M/$\overline{L}$	MODE	
Transparent Multiply	H	X	X	X	I/O Disabled
	L	L	L	H	Load Multiplier Latch
	L	L	H	H	Load Multiplicand Latch
	L	H	L	H	Read LSB Product From Adder Array
	L	H	H	H	Read MSB Product From Adder Array
Latched Multiply	L	L	L	L	Load Multiplier, Latch, Strobe Adder Array Data into Product Latches
	L	L	H	L	Load Multiplicand Latch
	L	H	L	L	Read LSB Product Latch
	L	H	H	L	Read MSB Product Latch

SIGN-BIT SELECTION FUNCTION TABLE

S/$\overline{U}$	I/O SIGNIFICANCE
L	Unsigned Byte Multiply
H	Signed Byte Multiply



16-PIN DIP
SBP 9708C . . . J OR N PACKAGE
SBP 9708 E,M . . . J PACKAGE



PIN DESCRIPTION

SIGNATURE	PIN	DESCRIPTION
V_{CC}	16	Provides +5 V connection to resistive pullups on outputs and voltage dividers on inputs.
GND	8	Ground
INJ *	5	Injector current input
D0-D7	7, 9 thru 15	Data input/output port
$\overline{CS}$, R/$\overline{W}$	2,4	Chip select low causes product latch data to be transferred onto the external data bus if read-write is high or causes multiplier/multiplicand data to be input to one of the input latches from the external bus if R/$\overline{W}$ is low. Chip select high causes D0-D7 to be at a logic high level.
M/$\overline{L}$	3	Most/Least byte select determines which multiplier latch is loaded on input, which byte of the product is read on output. Byte 1 latch and LSB product latch are accessed on M/$\overline{L}$ low.
MODE	6	MODE high causes adder array outputs to be passed directly to the 2 to 1 multiplexer. MODE low causes adder array outputs to be strobed into the product latches as the multiplier latch is loaded. Previous product data is then available after new multipliers are loaded. The multiplier latch must be loaded first.
S/$\overline{U}$	1	Signed multiply when high, unsigned multiply when low.

*Nominal current may be supplied by connection of a 24 Ω±5% (2 watt) resistor from V_{CC} to INJ input.

SBP 9708

recommended operating conditions

PARAMETER			MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}			4.5	5	5.5	V
Injector current, I_{INJ}			155	165	175	mA
High-level output voltage, V_{OH}					5.5	V
Low-level output current, I_{OL} (SBP 9708C only*)					8	mA
Width of load pulse (chip select low), $t_{w(\overline{CS})}$			100			ns
Setup time	$M/\overline{L}$ before load pulse, t_{su}		35↓			ns
	Data before end of load pulse, $t_{su(da)}$		60↓			
	$R/\overline{W}$ before load pulse, $t_{su(RW)}$		40↓			
Hold time	$M/\overline{L}$ after load pulse, $t_{h(ML)}$		0↑			ns
	Data after load pulse, $t_{h(da)}$		10↑			
	$R/\overline{W}$ after chip select, $t_{h(WR)}$		0↑			
Operating free-air temperature, T_A		SBP 9708M	−55		125	°C
		SBP 9708E	−40		85	
		SBP 9708C	0		70	

* Values for SBP 9708M and SBP 9708E will be announced at a later date.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

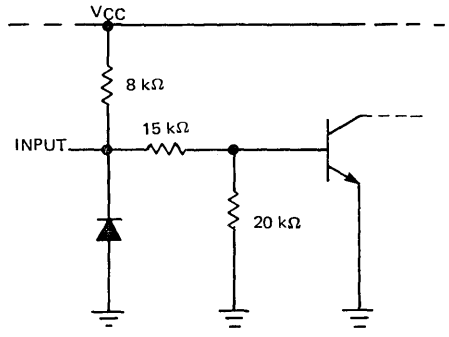
PARAMETER		TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN,	V_{IH} = 2.4 V, No Load	V_{IL} = 0.8V,	2.5	3.5		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2 V, I_{OL} = 8 mA	I_{INJ} = 130 mA,			0.5	V
I_{OS}	Short-circuit output current	V_{CC} = 5.5V			−0.3	−0.8	−1.2	mA
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			0.4	1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V			−0.3	−0.7	mA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.5 V			−0.7	−1.1	mA
I_{CC}	Supply current	V_{CC} = MAX				8	15	mA

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5V, I_{INJ} = 165 mA

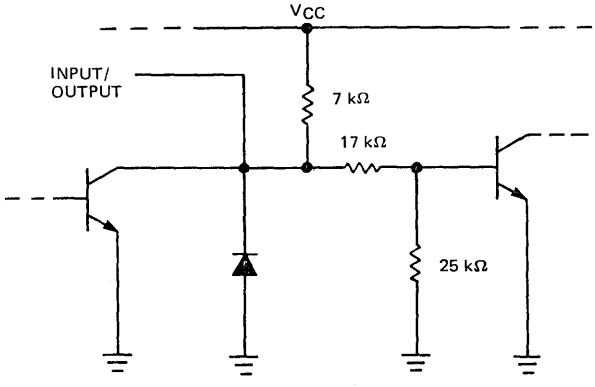
PARAMETER	FROM	TO	TEST CONDITIONS	NO EXTERNAL PULLUP			SEE LOAD CIRCUIT			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$t_{PD(CS)}$	$\overline{CS}$	OUTPUT (D7-D0)			240			150	200	ns
$t_{PD(S/U)}$	S/U	OUTPUT (D7-D0)	C_L = 80 pF		340			250	325	ns
$t_{PD(M/L)}$	M/L	OUTPUT (D7-D0)			250			160	200	ns
$t_{PD(MPY)}$	$\overline{CS}$ ↑	PROD OUT (D7-D0)	C_L = 80 pF, $V_{I(mode)}$ = 2 V		365			275	400	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡ All typical values are at V_{CC} = 5V, T_A = 25°C.
↓ ↑ The arrow indicates the transition of the chip-select input used for reference: ↑ for the low-to-high transition, ↓ for the high-to-low transition.

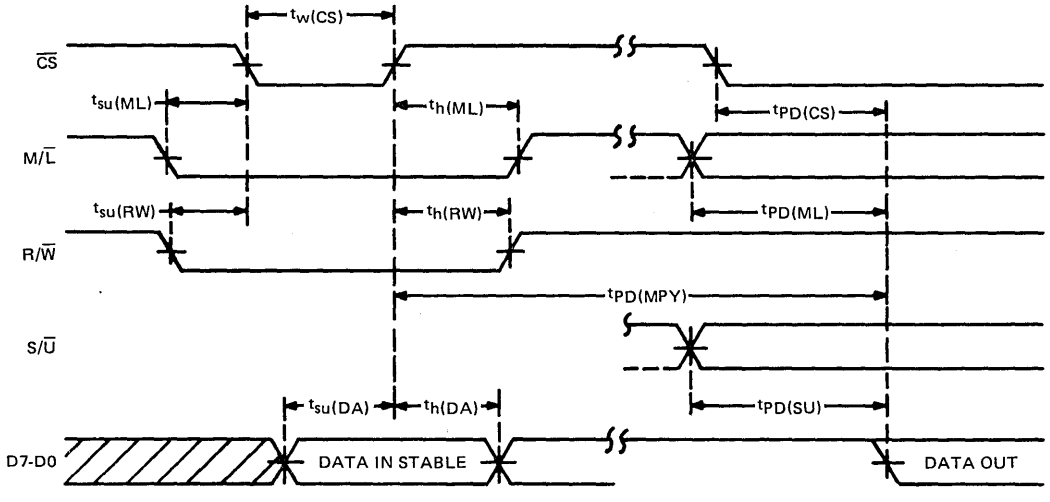
EQVIVALENT OF EACH INPUT



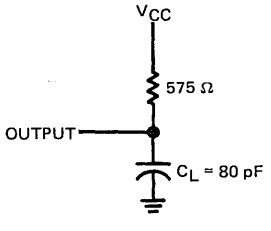
EQUIVALENT OF EACH INPUT/OUTPUT



SCHEMATICS OF INPUTS AND INPUT/OUTPUTS



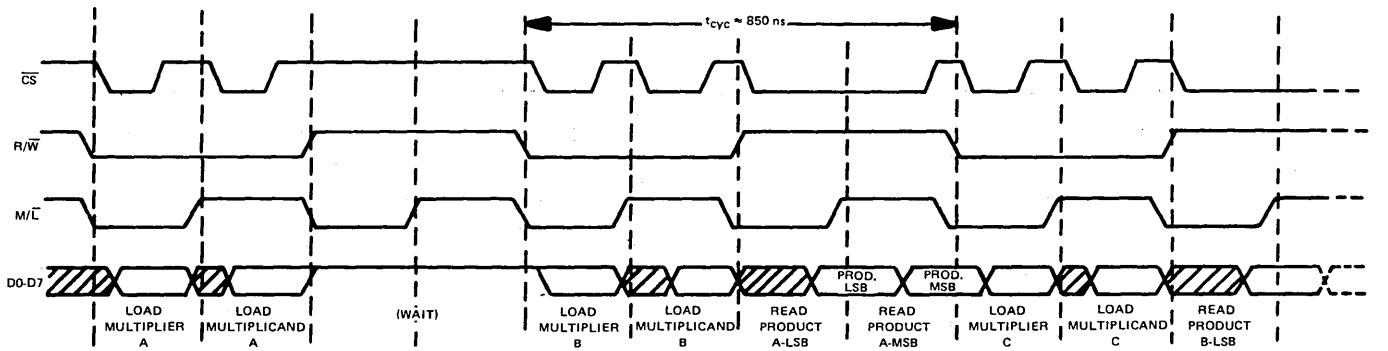
VOLTAGE WAVEFORMS



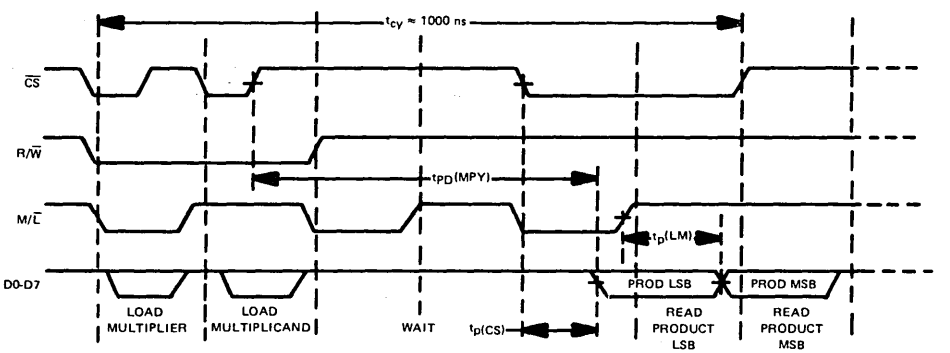
C_L includes probe and jig capacitance.

LOAD CIRCUIT

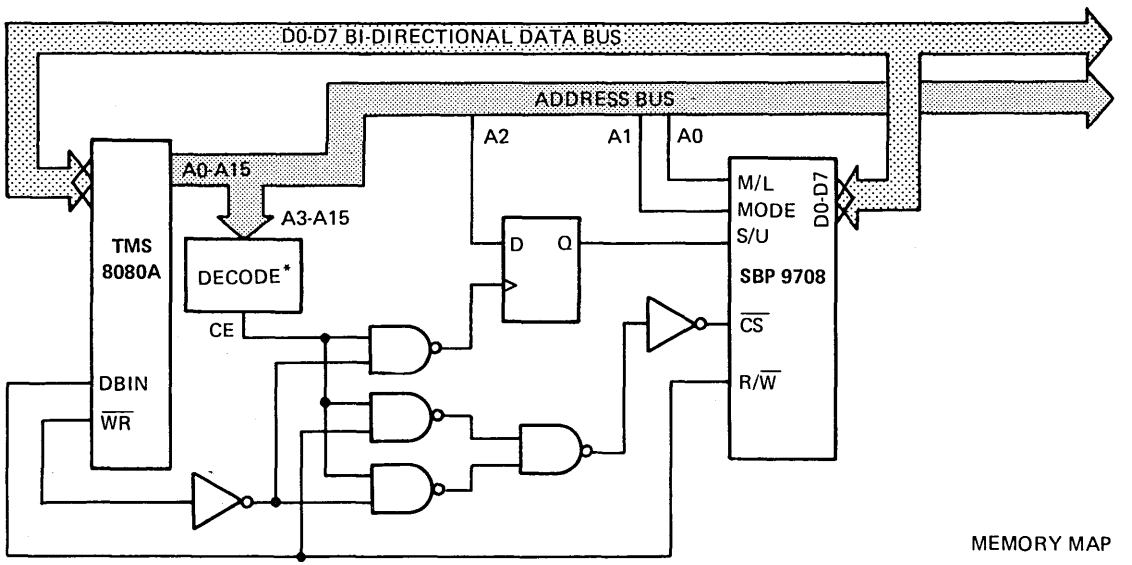
7



TIMING DIAGRAM—TYPICAL PIPELINED MODE SEQUENCE OF MULTIPLIES



TIMING DIAGRAM—TYPICAL TRANSPARENT MODE CYCLE

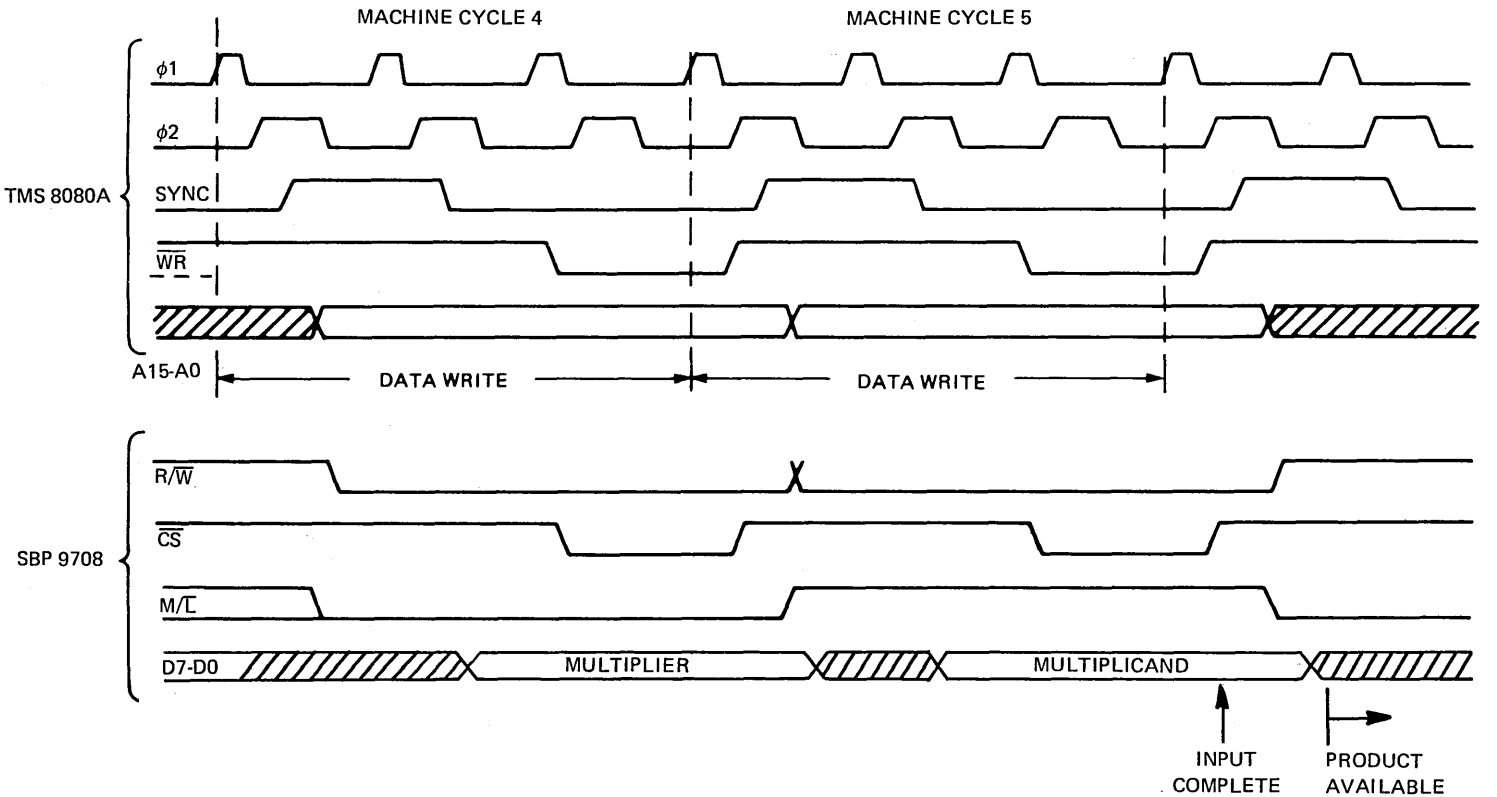


*CE becomes active (high) on a unique decode of address lines A3-A15

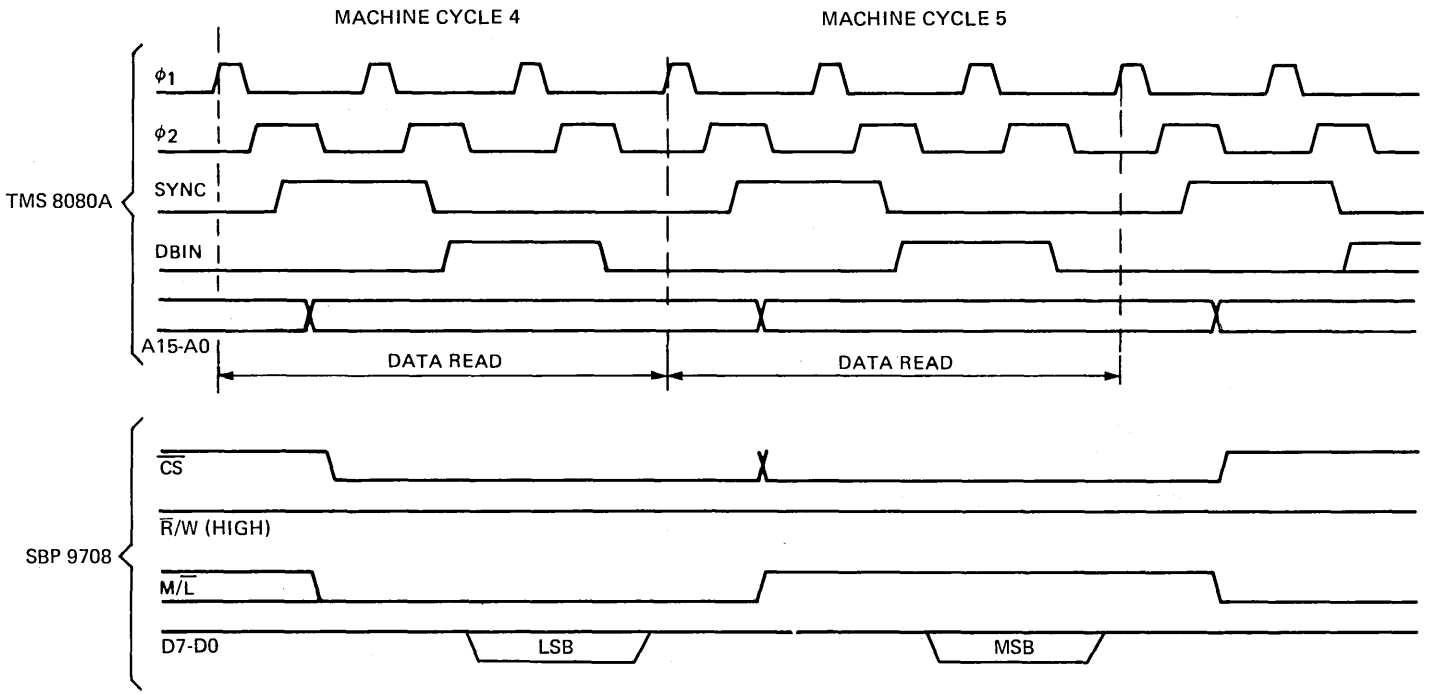
MEMORY MAP

(A_1)	(A_2)	$A_0 = 0$	$A_0 = 1$	
LATCHED, UNSIGNED				ADR
TRANSPARENT, UNSIGNED				ADR + 2
LATCHED, SIGNED				ADR + 4
TRANSPARENT, SIGNED				ADR + 6
		LSB	MSB	

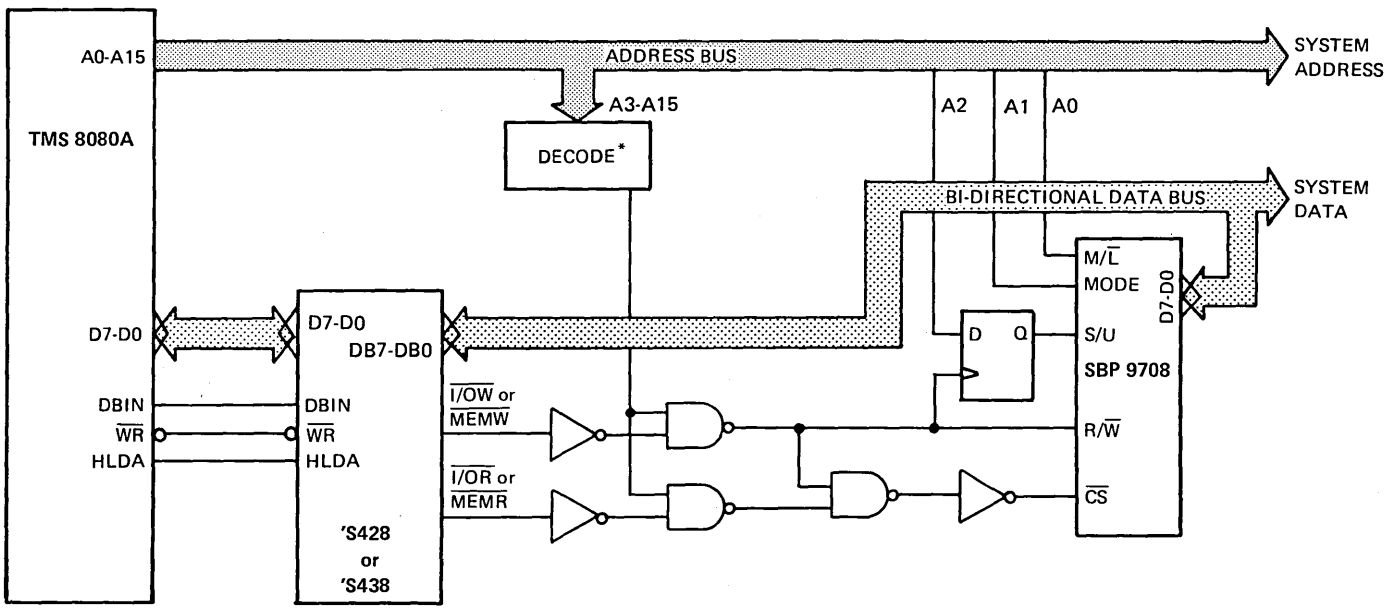
SBP 9708 TYPICAL MEMORY-MAPPED APPLICATION (8080A SYSTEM)



8080A SYSTEM MULTIPLIER LOAD CYCLE USING SN74LS245 (MEMORY-MAPPED)

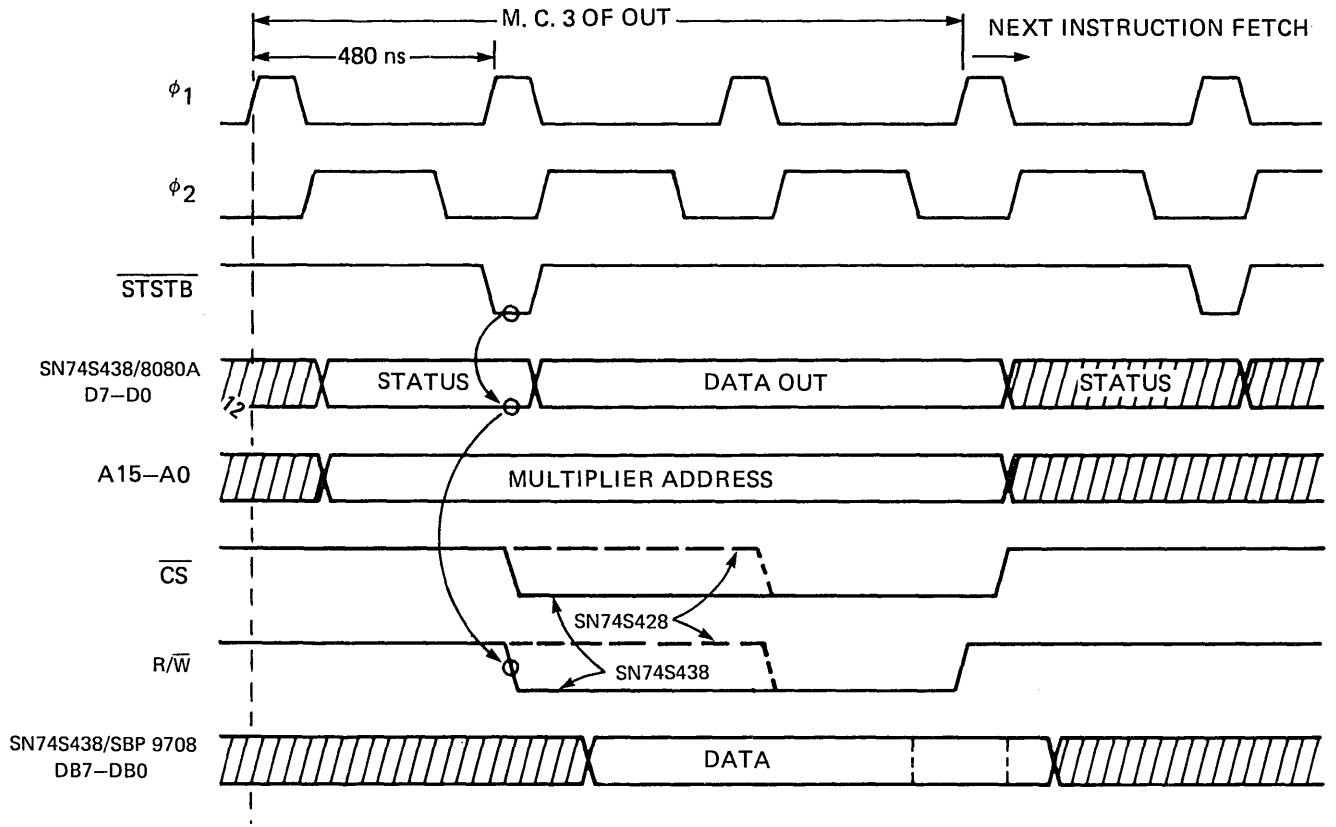


8080A SYSTEM PRODUCT READ CYCLE (MEMORY-MAPPED)

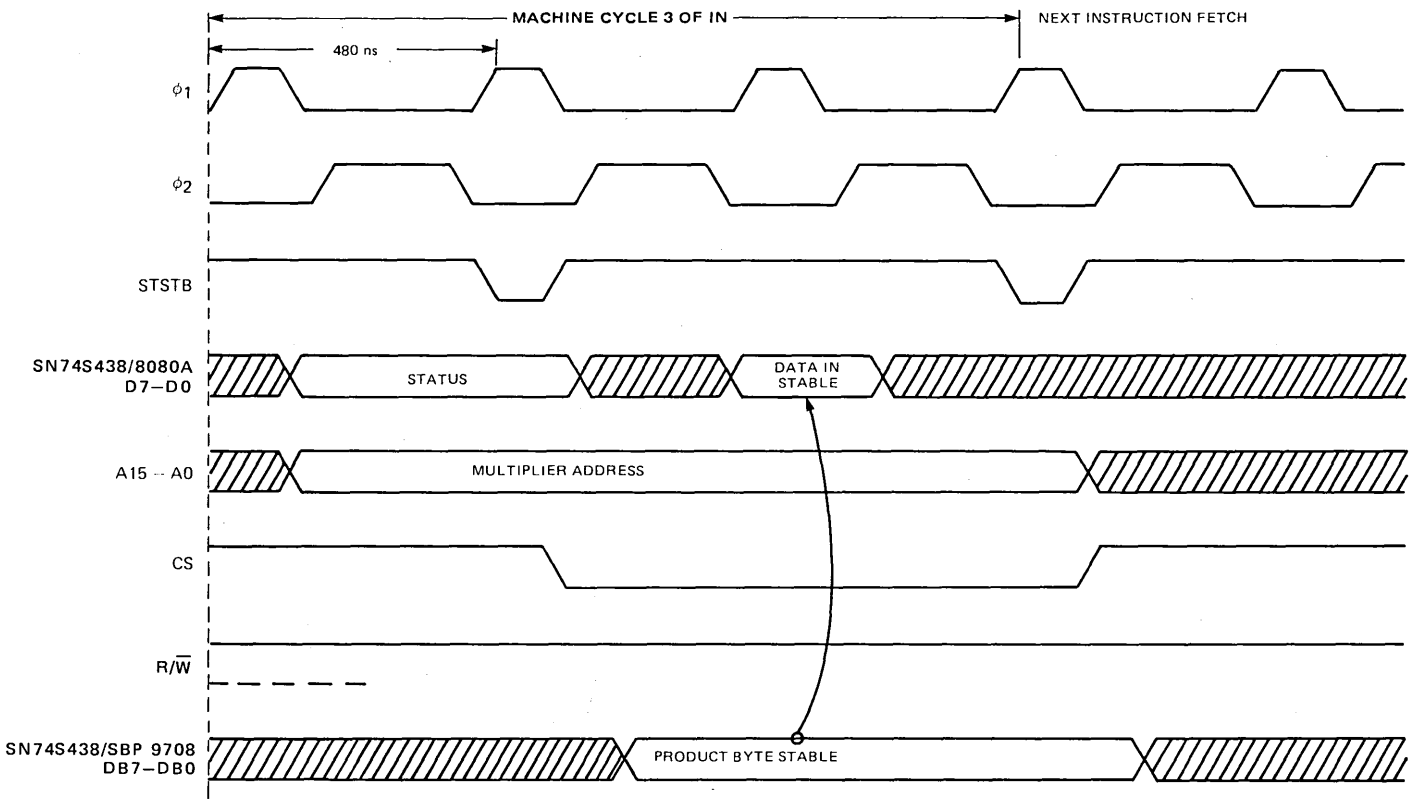


*DECODER OUTPUT GOES ACTIVE (HIGH)
ON A UNIQUE DECODE OF ADDRESS LINES A3-A15

SBP 9708 TYPICAL I/O MAPPED APPLICATION (8080A SYSTEM)



8080A SYSTEM MULTIPLIER LOAD CYCLE USING SN74S428 OR SN74S438



8080A SYSTEM MULTIPLIER READ CYCLE USING SN74S428 OR SN74S438

MECHANICAL DATA

ORDERING INSTRUCTIONS

Orders for devices from this book should include the package outline letter(s) at the end of the type number.

Examples: SN54S482J, SN74S740N

It is necessary to use only the first letter of the package type (J or N) unless the device is available in more than one type of J (dual-in-line ceramic) package, or in more than one type of N (dual-in-line plastic) package.

Special ordering instructions for programmable read-only memories (PROMs) are found on page 5-2.

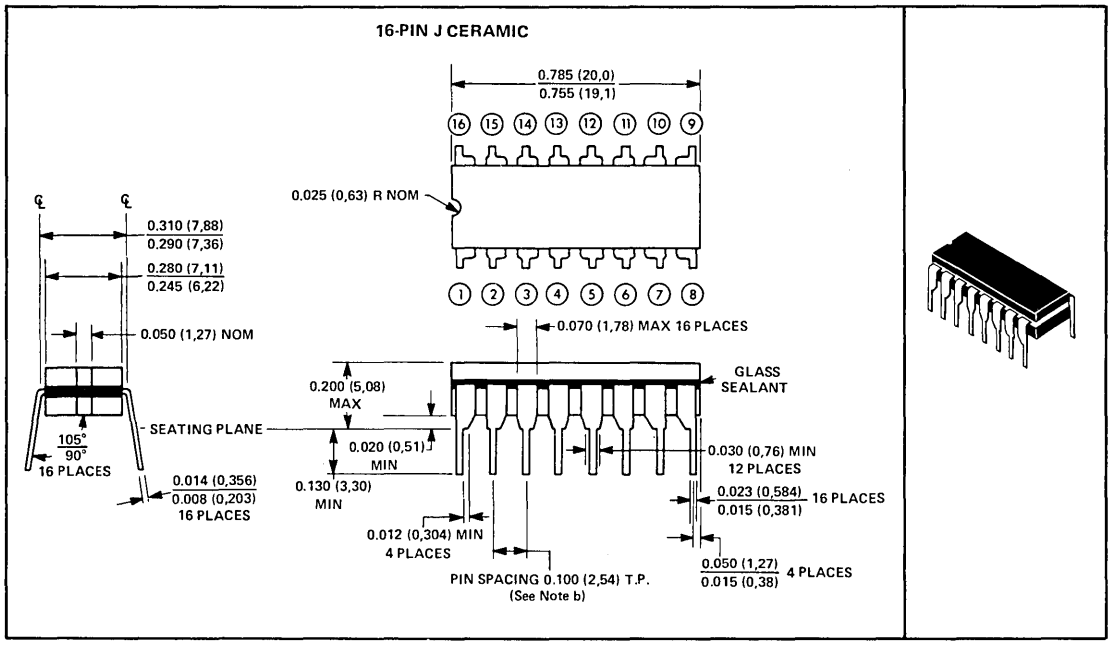
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

J ceramic packages (including JT and JW dual-in-line and JQ quad-in-line packages)

These hermetically sealed dual-in-line packages consist of a ceramic base, ceramic cap, and a 16-, 18-, 20-, 24-, 28-, or 48-lead frame. Hermetic sealing is accomplished with glass. The JT packages are intended for insertion in mounting-hole rows on 0.300 (7,62) centers, JW packages for mounting-hole rows on 0.600 (15,24) centers, and the JQ quad-in-line package for mounting-hole rows on 0.600 (15,24) and 0.800 (20,32) centers. Once the leads are compressed and inserted sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.

NOTE: For the 16-, 28-, and 20-pin packages, the letter J is used by itself since these packages are available only in the 0.300 (7,62) row spacing. For the 24-pin packages, if no second letter nor row spacing is specified, the package is assumed to have 0.600 (15,24) row spacing.

16-PIN J CERAMIC



NOTES: a. All dimensions are shown in inches (and parenthetically in millimeters for reference only). Inch dimensions govern.
b. Each pin centerline is located within 0.010 (0,26) of its true longitudinal position.

TEXAS INSTRUMENTS
INCORPORATED
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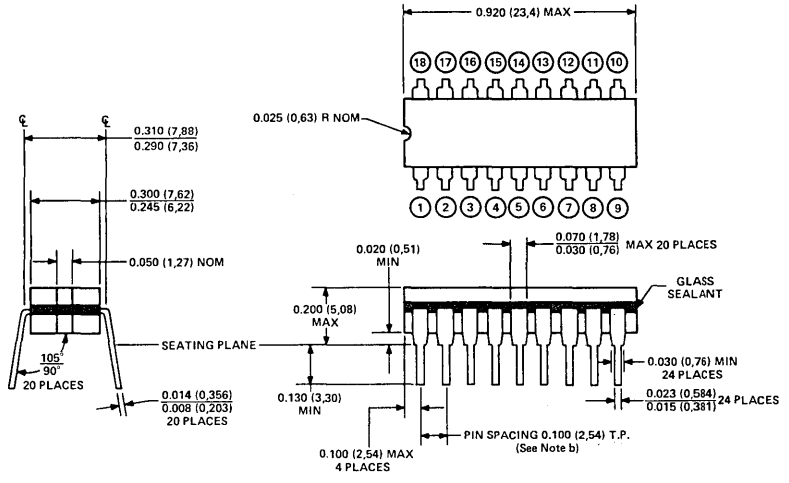
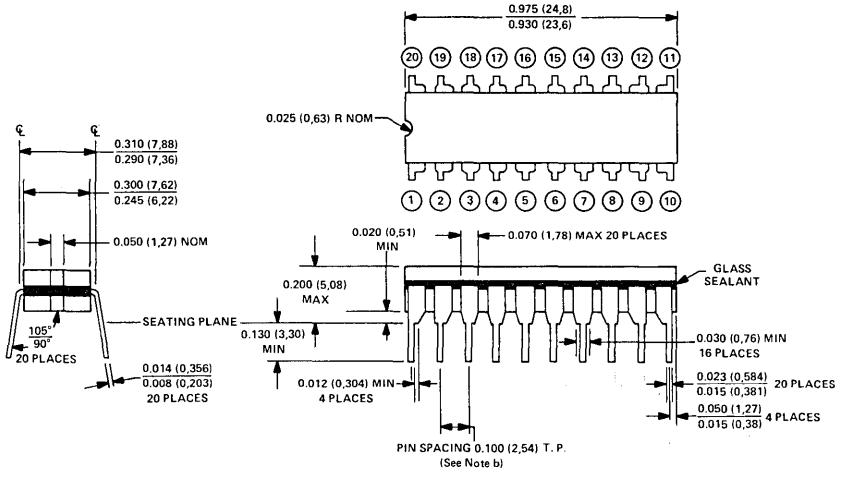
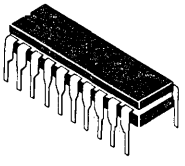
J ceramic packages (continued)

18-PIN J CERAMIC



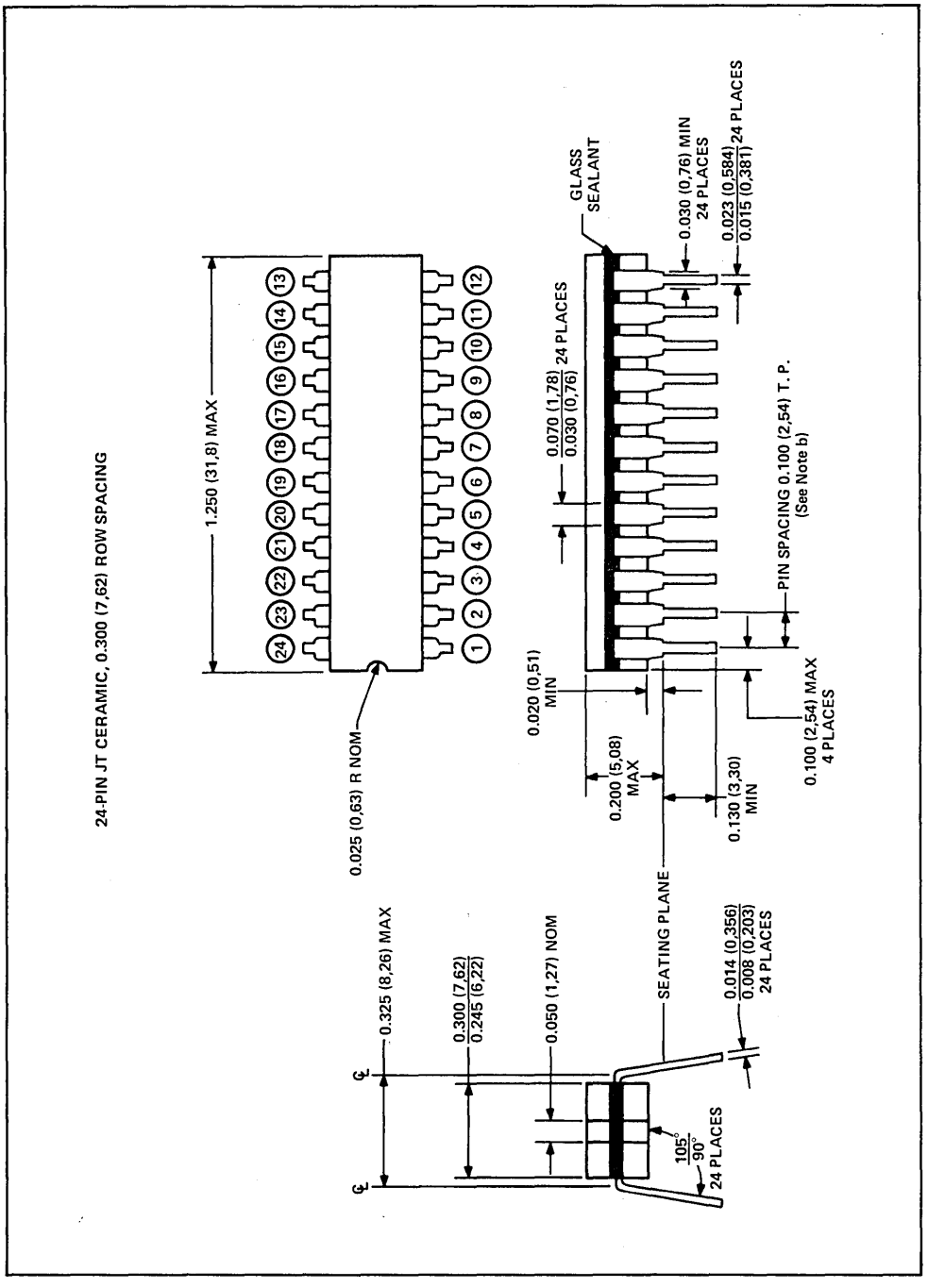
20-PIN J CERAMIC





NOTES: a. All dimensions are shown in inches (and parenthetically in millimeters for reference only). Inch dimensions govern.
b. Each pin centerline is located within 0.010 (0,26) of its true longitudinal position.

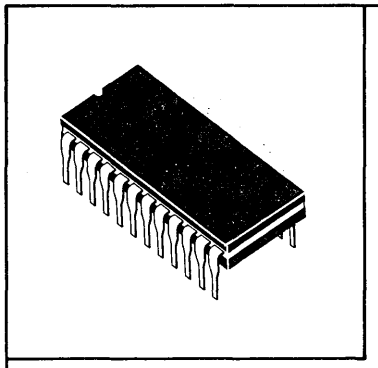
J ceramic packages (continued)



NOTES: a. All dimensions are shown in inches (and parenthetically in millimeters for reference only). Inch dimensions govern.
b. Each pin centerline is located within 0.010 (0,26) of its true longitudinal position.

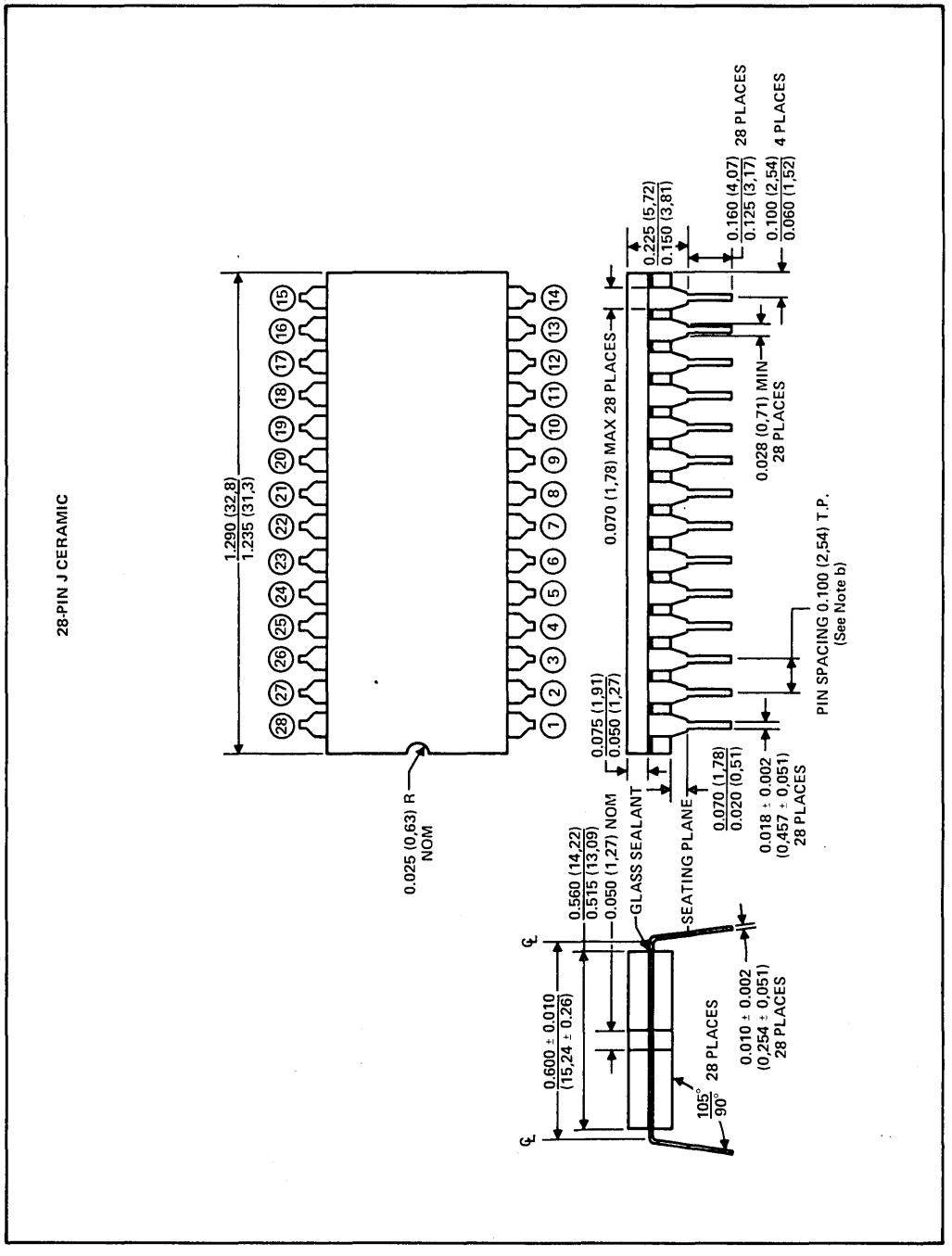
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

J ceramic packages (continued)



NOTES: a. All dimensions are shown in inches (and parenthetically in millimeters for reference only). Inch dimensions govern.
b. Each pin centerline is located within 0.010 (0,26) of its true longitudinal position.

J ceramic packages (continued)



NOTES: a. All dimensions are shown in inches (and parenthetically in millimeters for reference only). Inch dimensions govern.
b. Each pin centerline is located within 0.010 (0,26) of its true longitudinal position.

TEXAS INSTRUMENTS
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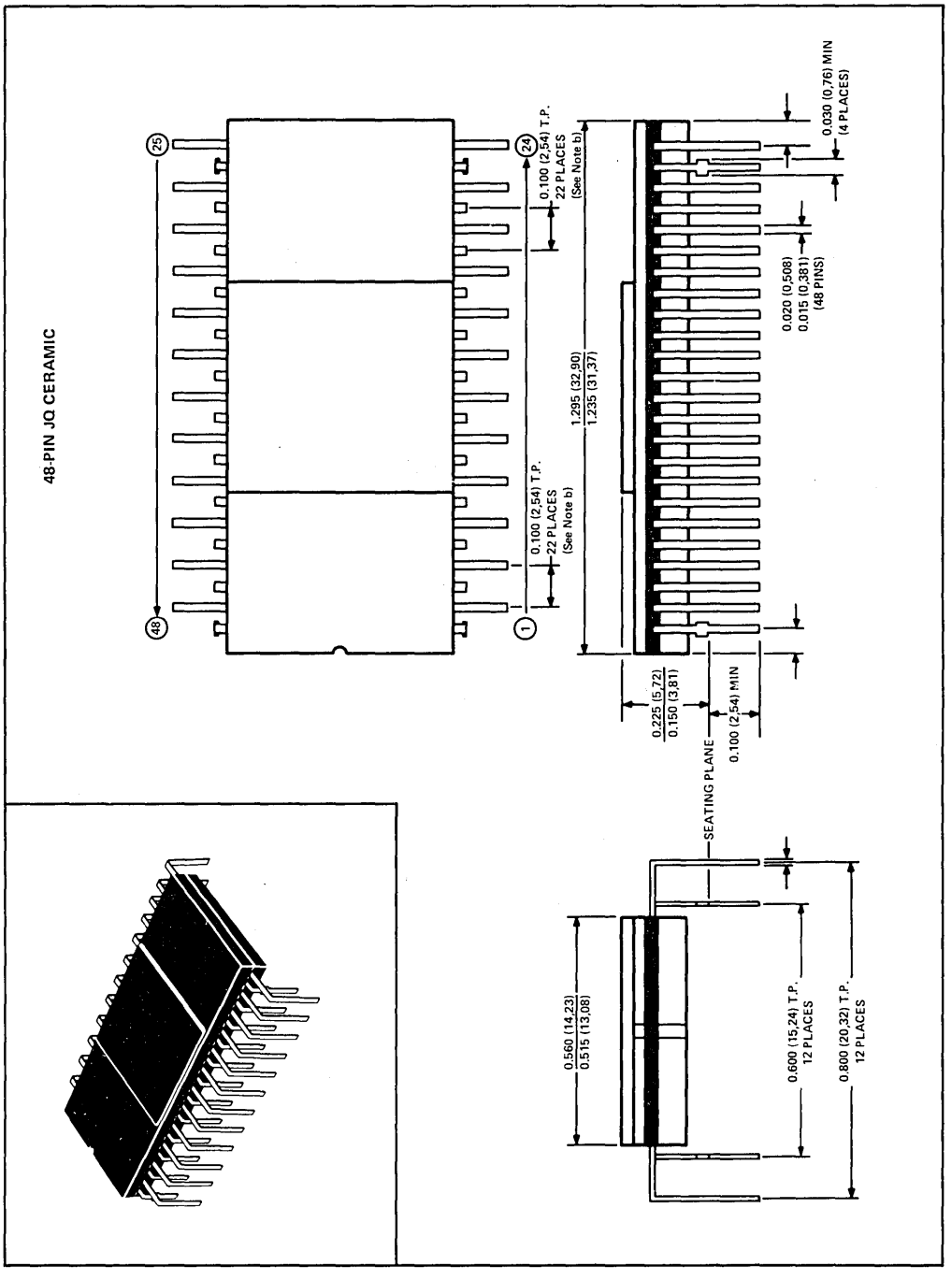
J ceramic packages (continued)

48-PIN JQ CERAMIC



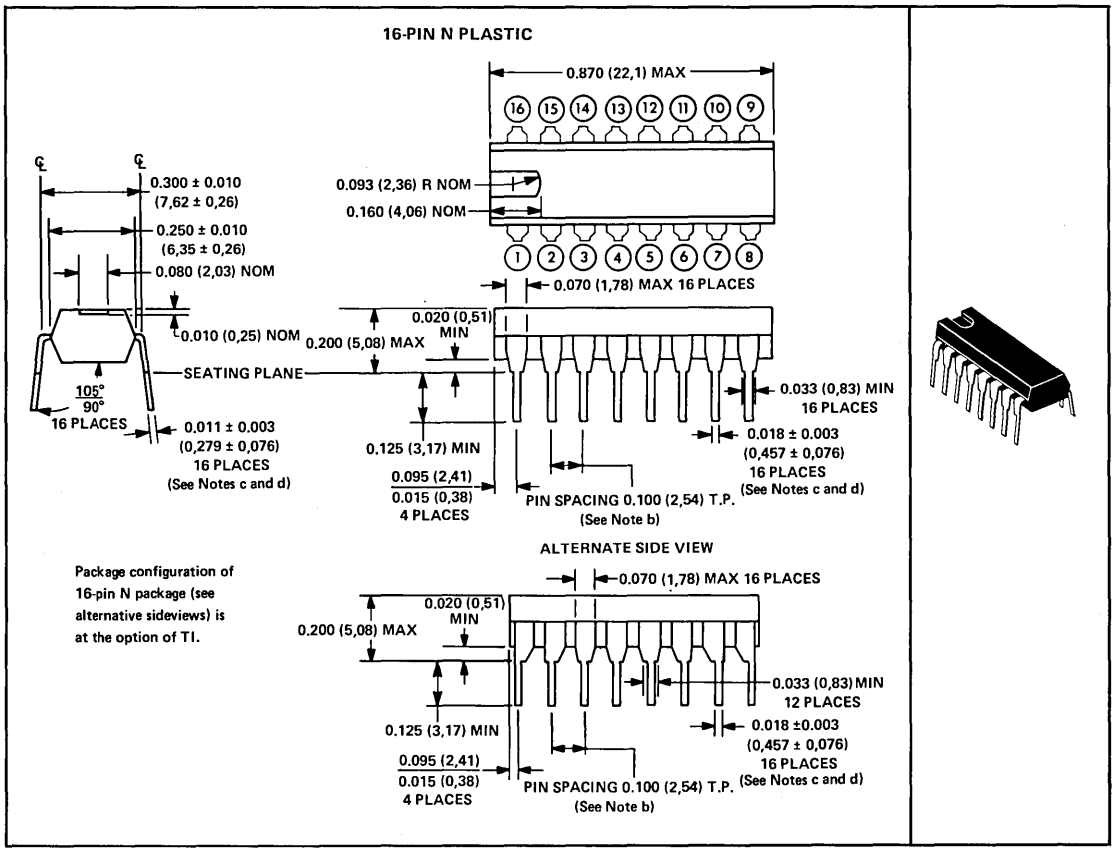
NOTES: a. All dimensions are shown in inches (and parenthetically in millimeters for reference only). Inch dimensions govern.
b. Each pin centerline is located within 0.010 (0,26) of its true longitudinal position.

8

N plastic packages (including NT and NW dual-in-line packages)

These dual-in-line packages consist of a circuit mounted on a 16-, 18-, 20-, 24-, or 28-pin lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. The packages are intended for insertion in mounting-hole rows on 0.300 (7,62) centers for the NT packages and on 0.600 (15,24) centers for the NW packages. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

NOTE: For the 16-, 18-, 20-, and 28-pin packages, the letter N is used by itself since these packages are available in only one row-spacing width — 0.300 (7,62) for the 16-, 18-, and 20-pin packages and 0.600 (15,24) for the 28-pin package. For the 24-pin package, if no second letter nor row spacing is specified, the package is assumed to have 0.600 (15,24) row spacing.



NOTES: a. All dimensions are shown in inches (and parenthetically in millimeters for reference only). Inch dimensions govern.
b. Each pin centerline is located within 0.010 (0,26) of its true longitudinal position.

TEXAS INSTRUMENTS
INCORPORATED
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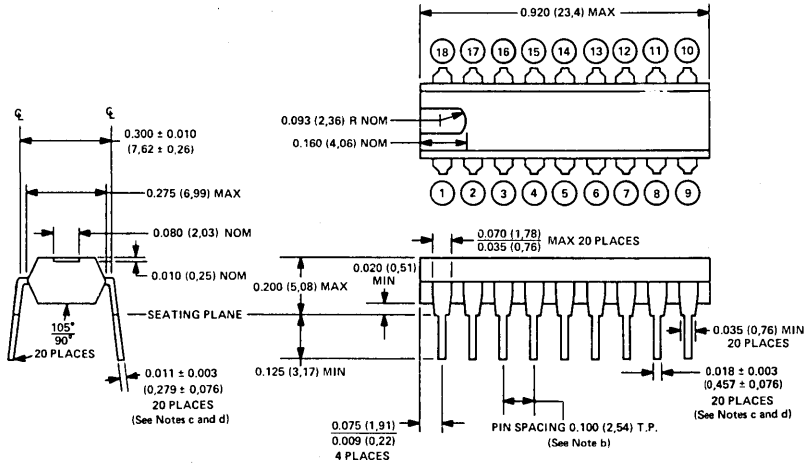
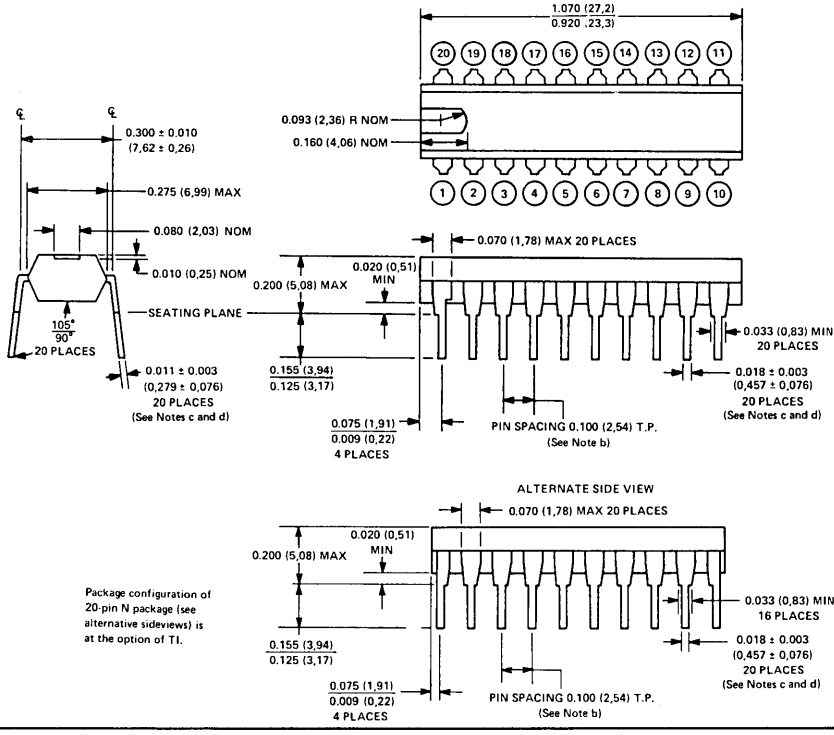
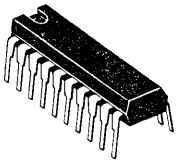
N plastic packages (continued)

18-PIN N PLASTIC



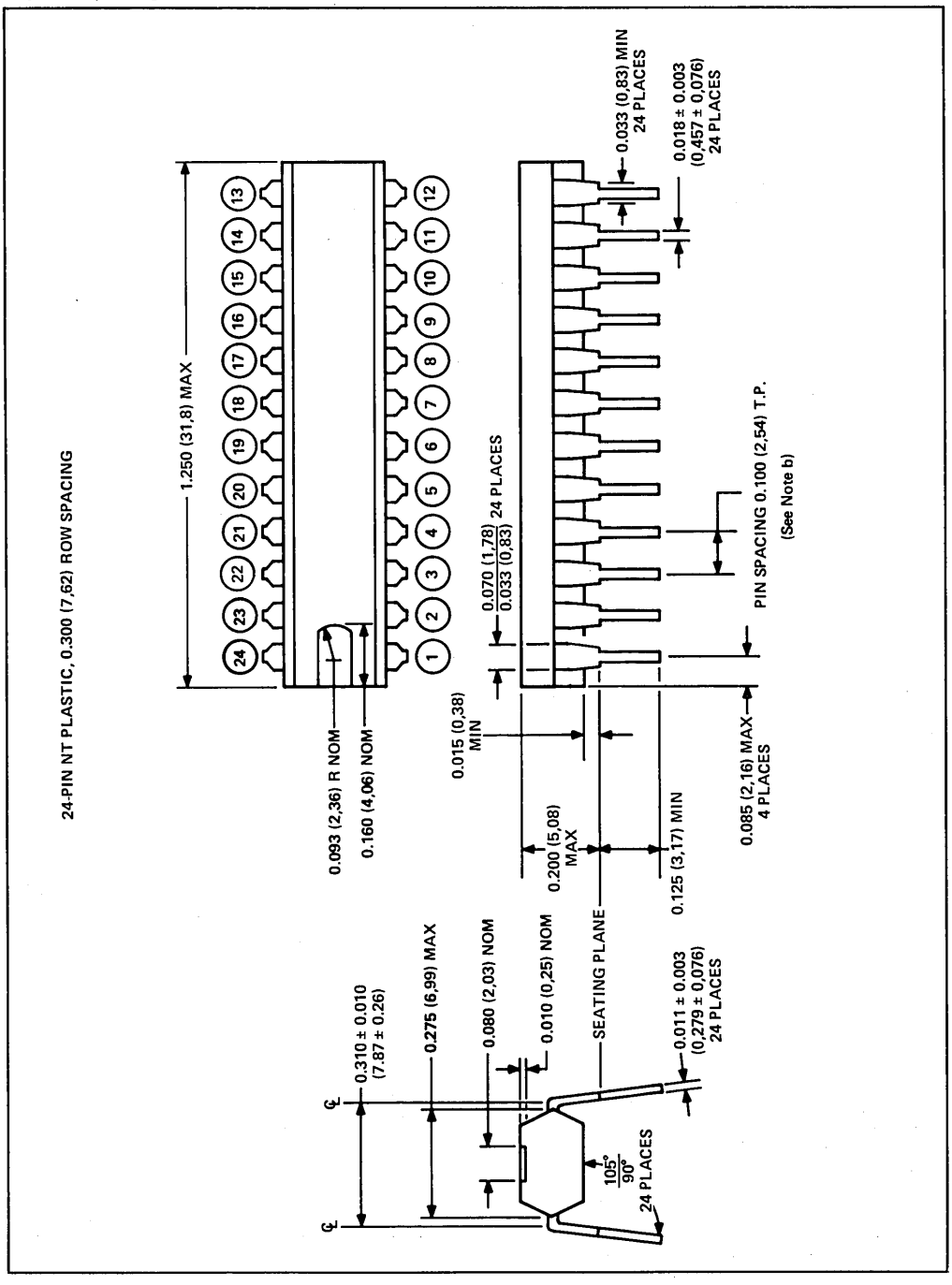
20-PIN N PLASTIC





NOTES: a. All dimensions are shown in inches (and parenthetically in millimeters for reference only). Inch dimensions govern.
b. Each pin centerline is located within 0.010 (0,26) of its true longitudinal position.

N plastic packages (continued)



NOTES: a. All dimensions are shown in inches (and parenthetically in millimeters for reference only). Inch dimensions govern.
b. Each pin centerline is located within 0.010 (0,26) of its true longitudinal position.

TEXAS INSTRUMENTS
INCORPORATED
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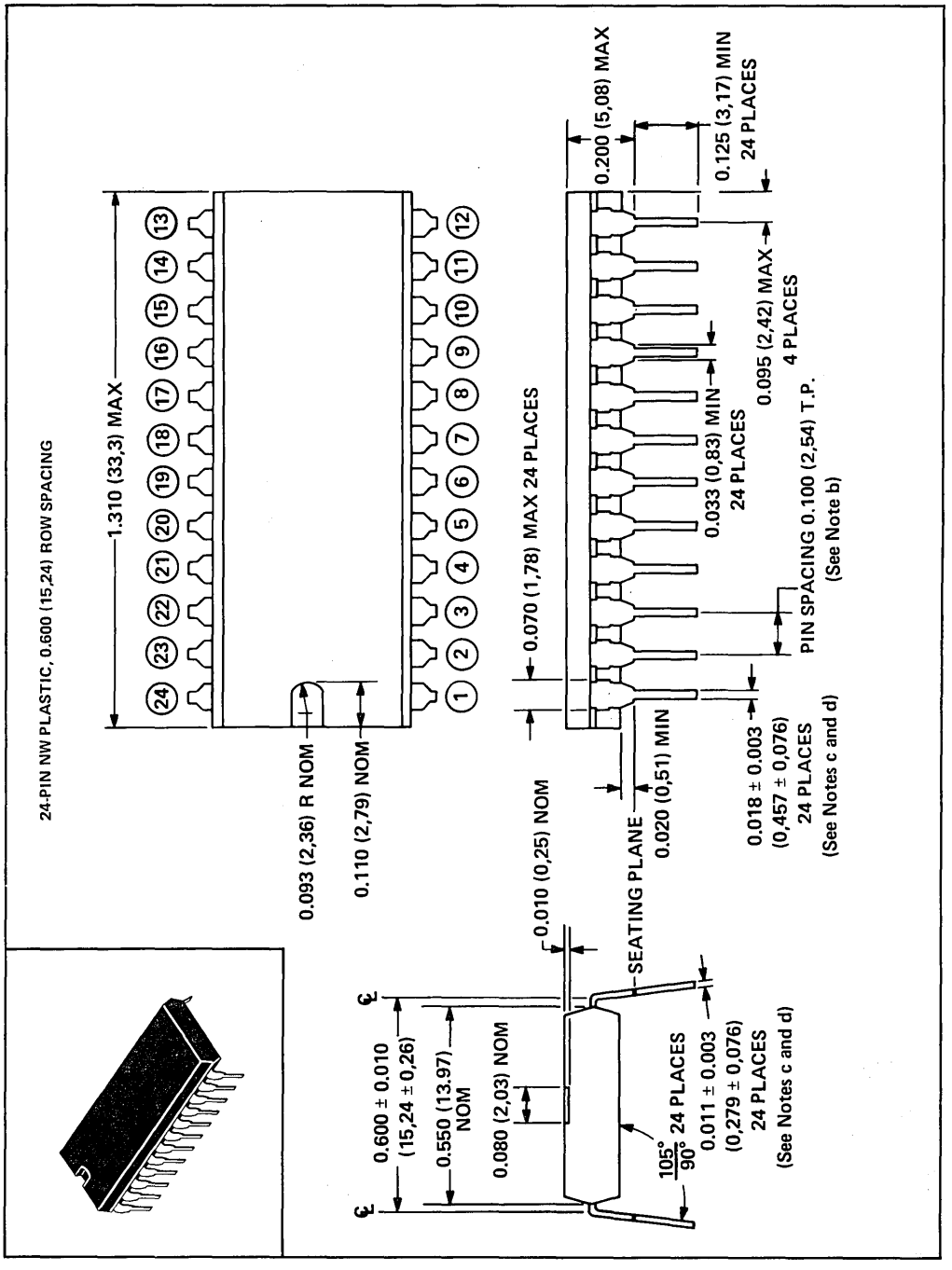
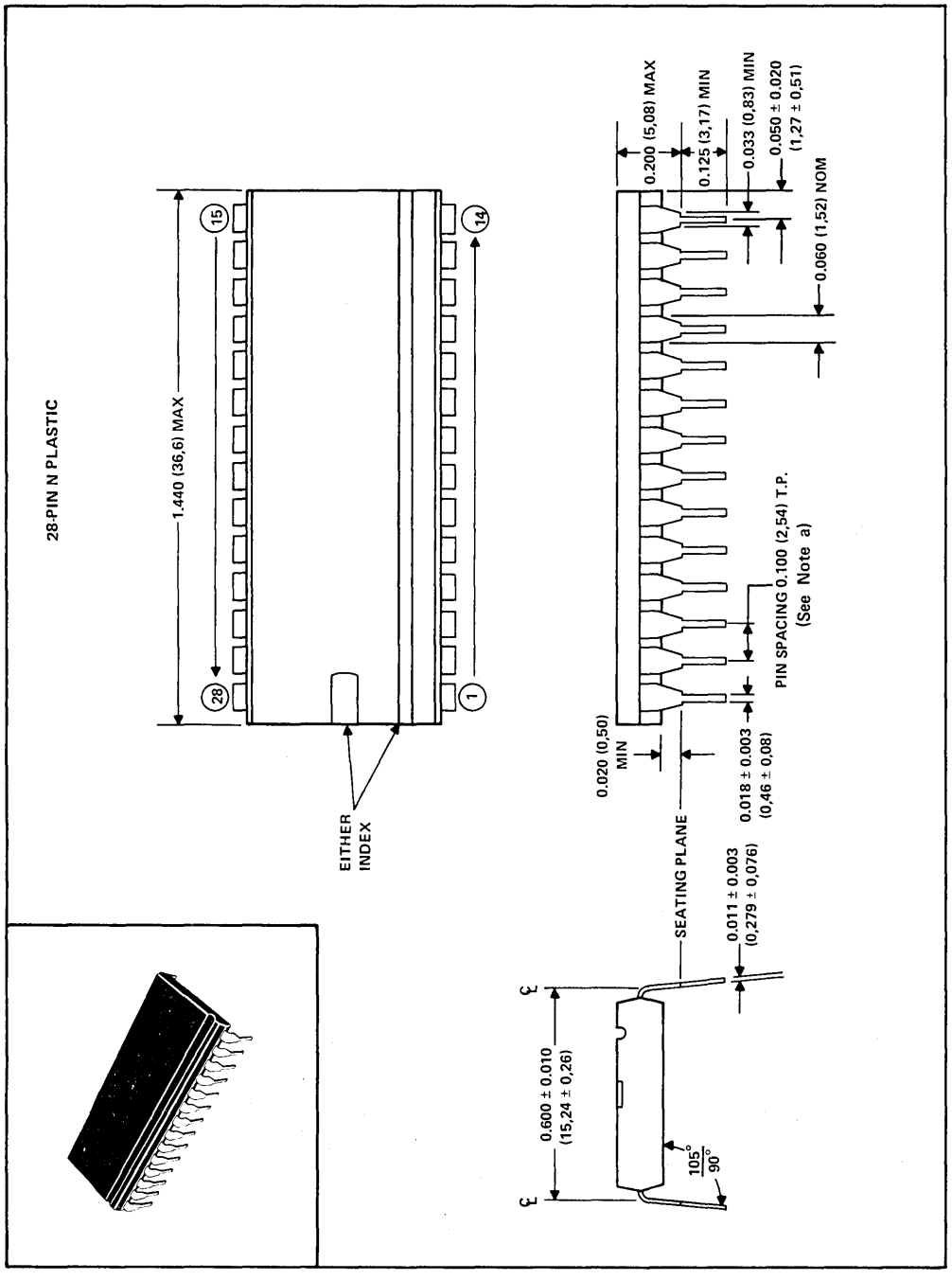
N plastic packages (continued)



NOTES: a. All dimensions are shown in inches (and parenthetically in millimeters for reference only). Inch dimensions govern.
b. Each pin centerline is located within 0.010 (0,26) of its true longitudinal position.

8

N plastic packages (continued)



NOTES: a. All dimensions are shown in inches (and parenthetically in millimeters for reference only). Inch dimensions govern.
b. Each pin centerline is located within 0.010 (0,26) of its true longitudinal position.

TEXAS INSTRUMENTS
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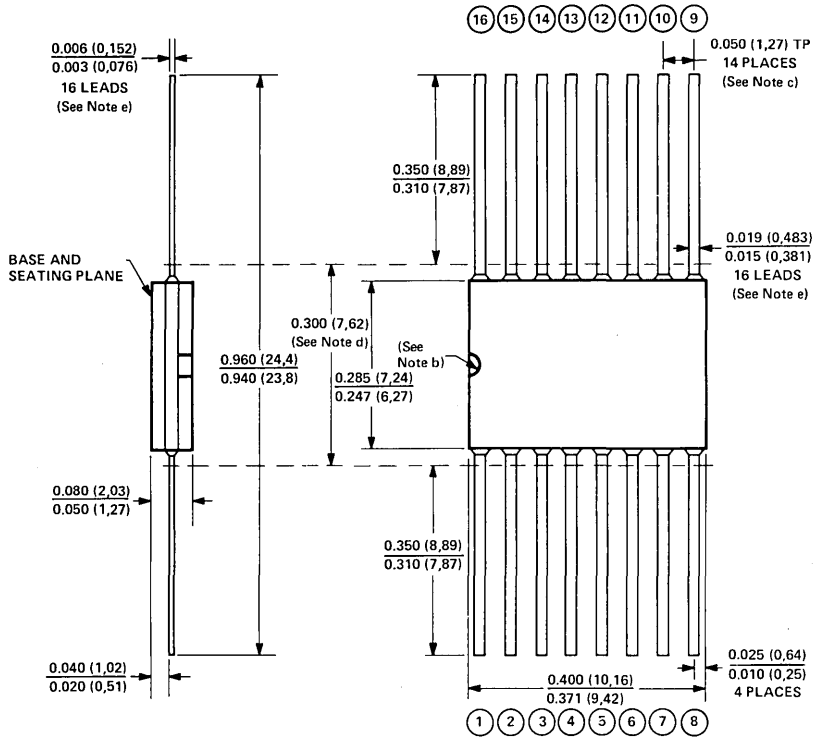
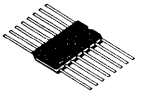
W ceramic flat package

These hermetically sealed flat packages consist of an electrically nonconductive ceramic base and cap, and a 16- or 24-lead frame. Hermetic sealing is accomplished with glass. Tin-plated ("bright-dipped") leads (–00) require no additional cleaning or processing when used in soldered assembly.

16-PIN W CERAMIC



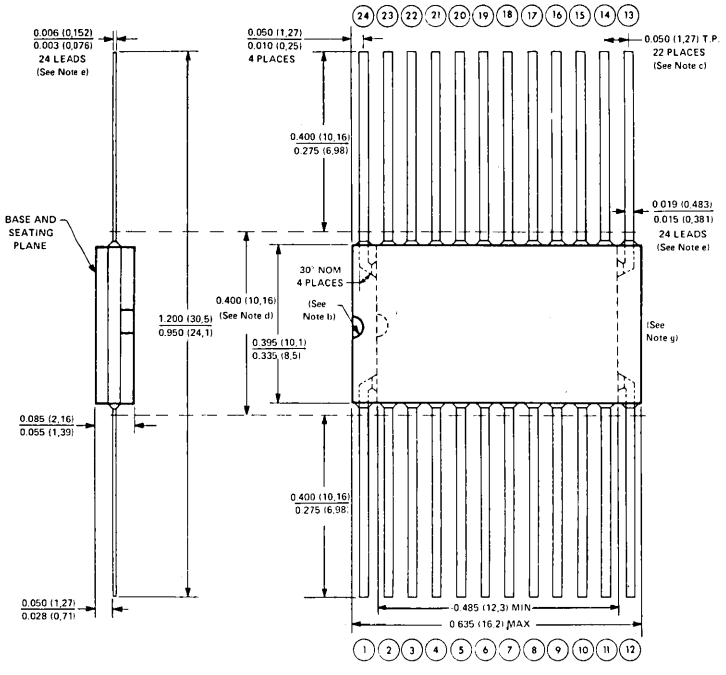


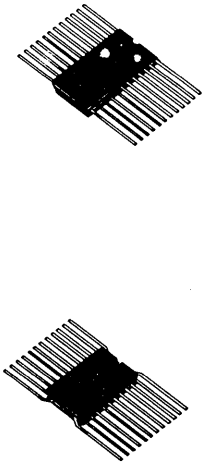
Falls within JEDEC MO-004AG Dimensions

NOTES: a. All dimensions are shown in inches (and parenthetically in millimeters for reference only). Inch dimensions govern.
b. Index point is provided on cap for terminal identification only.
c. Leads are within 0.005 (0,13) radius of true position (T.P.) at maximum material condition.
d. This dimension determines a zone within which all body and lead irregularities lie.
e. Not applicable for solder-dipped leads.
f. When solder-dipped leads are specified, dipped area extends from lead tip to within 0.050 (1,27) of package body.

W ceramic flat package (continued)

24-PIN W CERAMIC





NOTES: a. All dimensions are shown in inches (and parenthetically in millimeters for reference only). Inch dimensions govern.
b. Index point is provided on cap for terminal identification only.
c. Leads are within 0.005 (0,13) radius of true position (T.P.) at maximum material condition.
d. This dimension determines a zone within which all body and lead irregularities lie.
e. Not applicable for solder-dipped leads.
f. When solder-dipped leads are specified, dipped area extends from lead tip to within 0.050 (1,27) of package body.
g. End configuration of 24-pin package is at the option of TI.

TEXAS INSTRUMENTS
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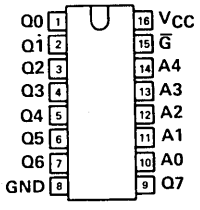
ERRATA

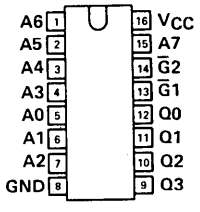
This page and the one that follows correct pages 5-7 and 5-15. In addition to showing pins 18 and 19 of TBP28S85, TBP28L85, and TBP28P85 to be active high (E, not $\overline{E}$), the rank numbers of all A, E, G, and Q pins have been changed to correspond with the numbering in the standard pin-outs currently under consideration by the JEDEC Committee on Bipolar Memories, JC42.1. For the same reason, S pins (chip select) have been redesignated G (output enable), these functions being interchangeable in unregistered PROMs. With the exception of the E to $\overline{E}$ corrections, these changes strictly involve nomenclature, not functional changes.

SERIES 14 AND 18 PROGRAMMABLE READ-ONLY MEMORIES

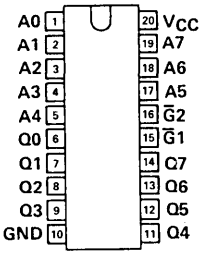
TBP18SA030, TBP18S030
256 BITS
(32 WORDS BY 8 BITS)
(TOP VIEW)



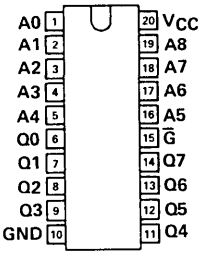
TBP14S10, TBP14SA10
1024 BITS
(256 WORDS BY 4 BITS)
(TOP VIEW)



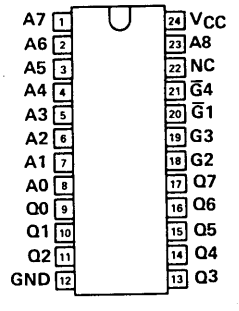
TBP18SA22, TBP18S22
2048 BITS
(256 WORDS BY 8 BITS)
(TOP VIEW)



TBP18S42, TBP18SA22
4096 BITS
(512 WORDS BY 8 BITS)
(TOP VIEW)



TBP18S46, TBP18SA46
4096 BITS
(512 WORDS BY 8 BITS)
(TOP VIEW)



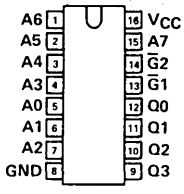
Pin assignments for all of these memories are the same for all packages.

8

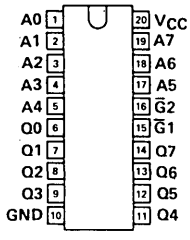
ERRATA

SERIES 24 AND 28 PROGRAMMABLE READ-ONLY MEMORIES

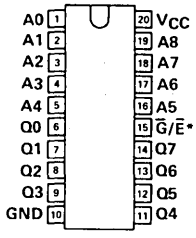
TBP24S10, TBP24SA10
1024 BITS
(256 WORDS BY 4 BITS)



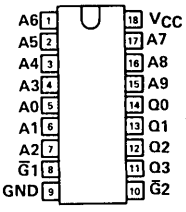
TBP28L22
2048 BITS
(256 WORDS BY 8 BITS)



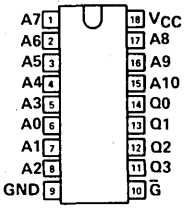
TBP28S42, TBP28L42,
TBP28P42* 4096 BITS
(512 WORDS BY 8 BITS)



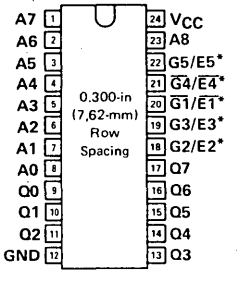
TBP24S41, TBP24SA41
4096 BITS
(1024 WORDS BY 4 BITS)



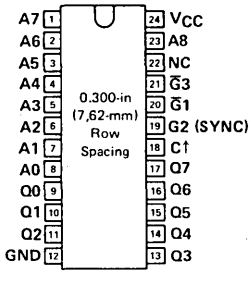
TBP24S81, TBP24SA81
8192 BITS
(2048 WORDS BY 4 BITS)



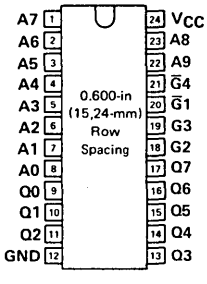
TBP28S45, TBP28L45, TBP28P45*
4096 BITS
(512 WORDS BY 8 BITS)



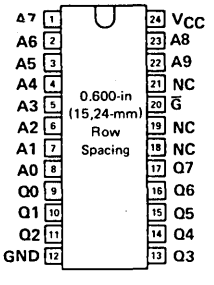
TBP28R45
4096 BITS
(512 WORDS BY 8 BITS)



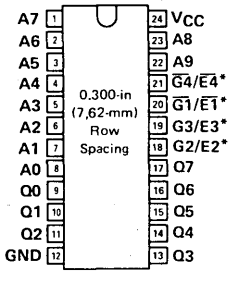
TBP28S86, TBP28SA86, TBP28L86
8192 BITS
(1024 WORDS BY 8 BITS)



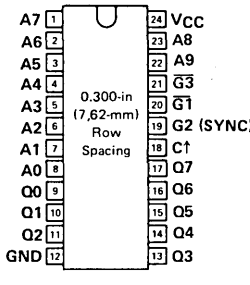
TBP28S2708
8192 BITS
(1024 WORDS BY 8 BITS)



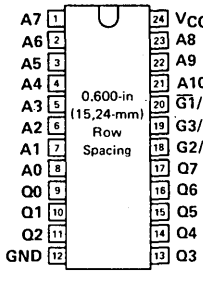
TBP28S85, TBP28L85, TBP28P85*
8192 BITS
(1024 WORDS BY 8 BITS)



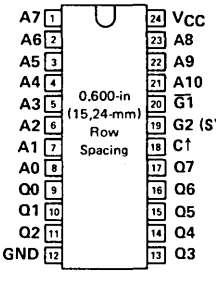
TBP28R85
8192 BITS
(1024 WORDS BY 8 BITS)



TBP28S166, TBP28L166, TBP28P166*
16,384 BITS
(2048 WORDS BY 8 BITS)



TBP28R166
16,384 BITS
(2048 WORDS BY 8 BITS)



* For those pins having dual designations, the designation to the right of the virgule (/) applies only to the type number(s) immediately followed by an asterisk (*) above the pinout drawing.

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