The Benefits of Microcontoller and Analog Integration: S12 MagniV Mixed-Signal MCUs

AMF-AUT-T0801

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Designing with Freescale
Toronto November 7&8

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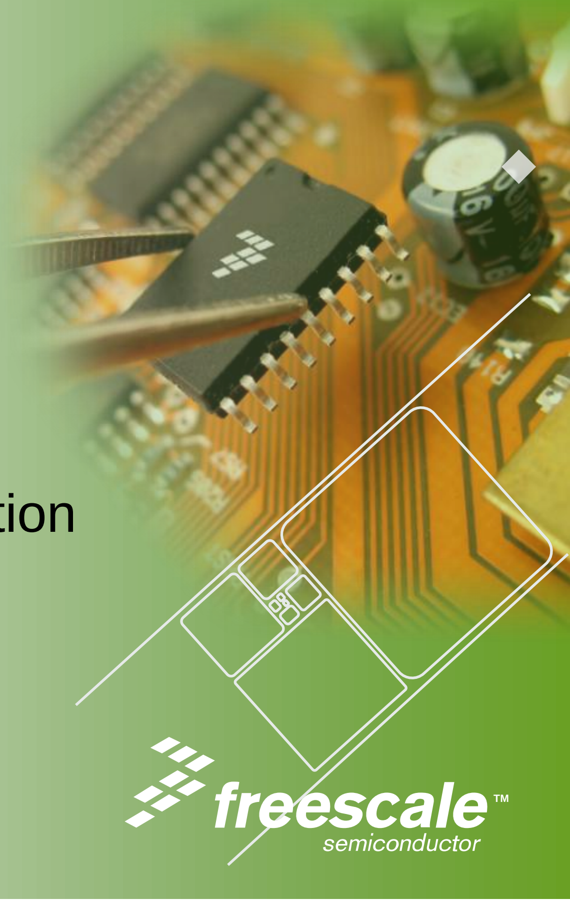
Agenda

- MagniV Roadmap
- S12VM
  - Overview
  - CPU12Z
  - Motor Control
    - Digital
    - Analog
- Development Tools
- BLDC Sensorless Motor Control Implementation
- Position Sensing with Zero Cross Detection
- Speed Control
- Dynamic Current Limitation



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Automotive Market Trends

- **Reduction of power consumption** is critical for creating “greener” vehicles
  - Reduce **cable weight**
  - **Smarter** control techniques
- **Higher reliability** to achieve Zero Defect goal
- Increase convenience and comfort
  - Find **space** for new features
  - Make them **affordable** to the user.

LOCAL INTERCONNECT NETWORK

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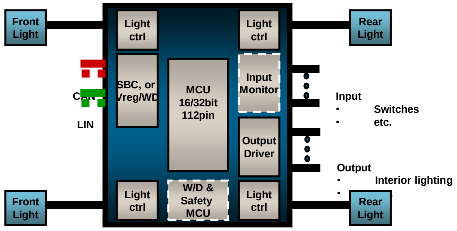
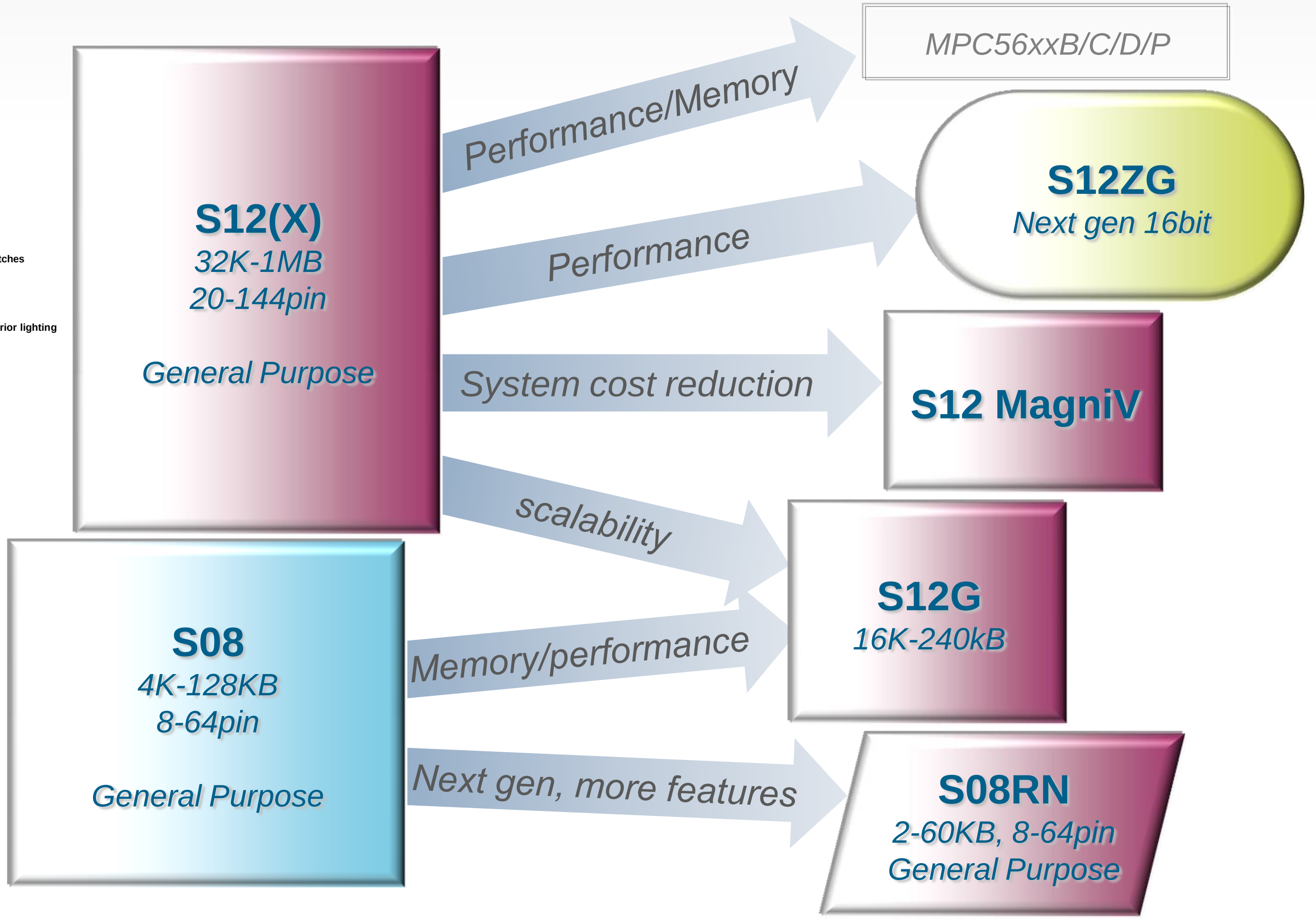
Highlevel 8 & 16-bit Body MCU Roadmap

PERFORMANCE



Low End BCM

Single CAN node BCMs
Door/Seat/Window/Etc



MPC56xxB/C/D/P

S12(X)
32K-1MB
20-144pin

General Purpose

Performance/Memory

Performance

S12ZG
Next gen 16bit

System cost reduction

S12 MagniV

scalability

S12G
16K-240kB

S08
4K-128KB
8-64pin

General Purpose

Memory/performance

Next gen, more features

S08RN
2-60KB, 8-64pin
General Purpose

▨	250nm
▨	180 nm
▨	55nm

Production | Execution | Planning | Proposal

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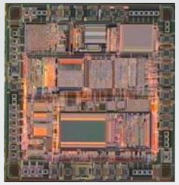
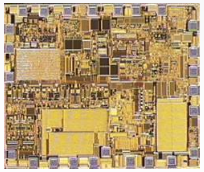
What‘s System in Package (SiP)?

Semi-Discrete Solution

- Standard MCU

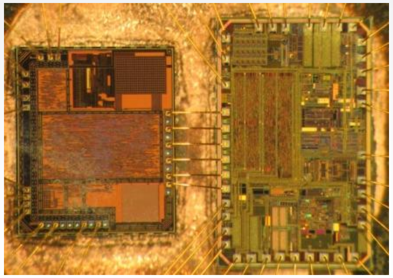


- Application Specific Analog IC (ASIC)



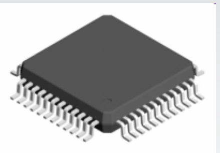
Multi-die SiP

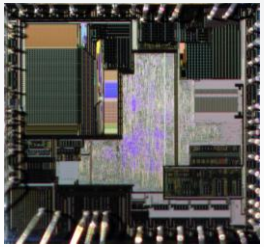
- Single package
- Die-to-die bonding



Monolithic SiP

- MCU and Analog on the same die





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15 Years of System in Package (SiP) Experience

Products

908E622/1
- 8-bit HC08 + SMOS5 Mirror Driver

HC05PV8
- 8-bit HC05 Hyper-integrated Relay Driver

908E624
- 8-bit HC08 + SMOS5 Relay Driver

908E630
- 8-bit HC08 (SOG) + SMOS8 Relay Driver

912F634
- 16-bit S12I32 + SMOS8 Relay & Switch Driver

S12**V**R64
First S12 MagniV product:

S12**ZV**M
S12**ZV**H

908E626
- HC08 + SMOS5 AFS Stepper Driver

Troll - MUX3
- 8-bit HC05 Hyper-integrated Climate Stepper Driver

1997	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015

Technologies

SMOS8 (0.25um)

QFN Package

LL18UHV technology
Monolithic SiP

Monolithic Architecture

SiP Architecture

HC05 Microcontroller with
EEPROM (IDR60% -1.2um)

HC08 Microcontroller with
flash (0.5um)

S12Z Core

Mechatronics
Package

SMOS5 (0.8um)

S12 Core (0.25um)

Start of SiP R&D

54ld SOIC Package

Architecture
Repartitioning

1st Gen

2nd Gen

3rd Gen

4th Gen

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2012 Designing with Freescale
Toronto November 7&8

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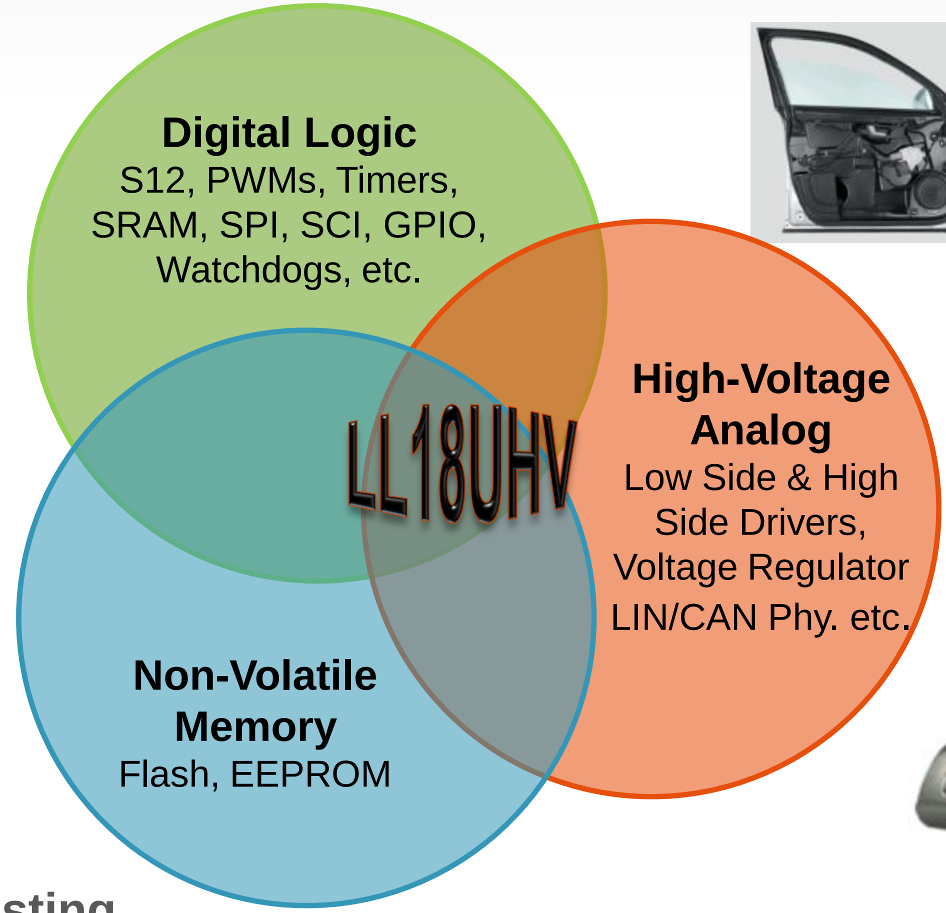
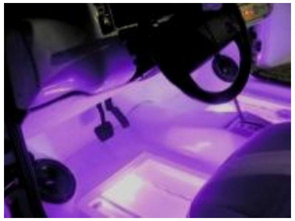
LL18UHV Technology Summary for S12 MagniV



Digital Logic
S12, PWMs, Timers, SRAM, SPI, SCI, GPIO, Watchdogs, etc.

High-Voltage Analog
Low Side & High Side Drivers, Voltage Regulator
LIN/CAN Phy. etc.

Non-Volatile Memory
Flash, EEPROM



Existing
Low Leakage 180nm CMOS+NVM

40V UHV Devices

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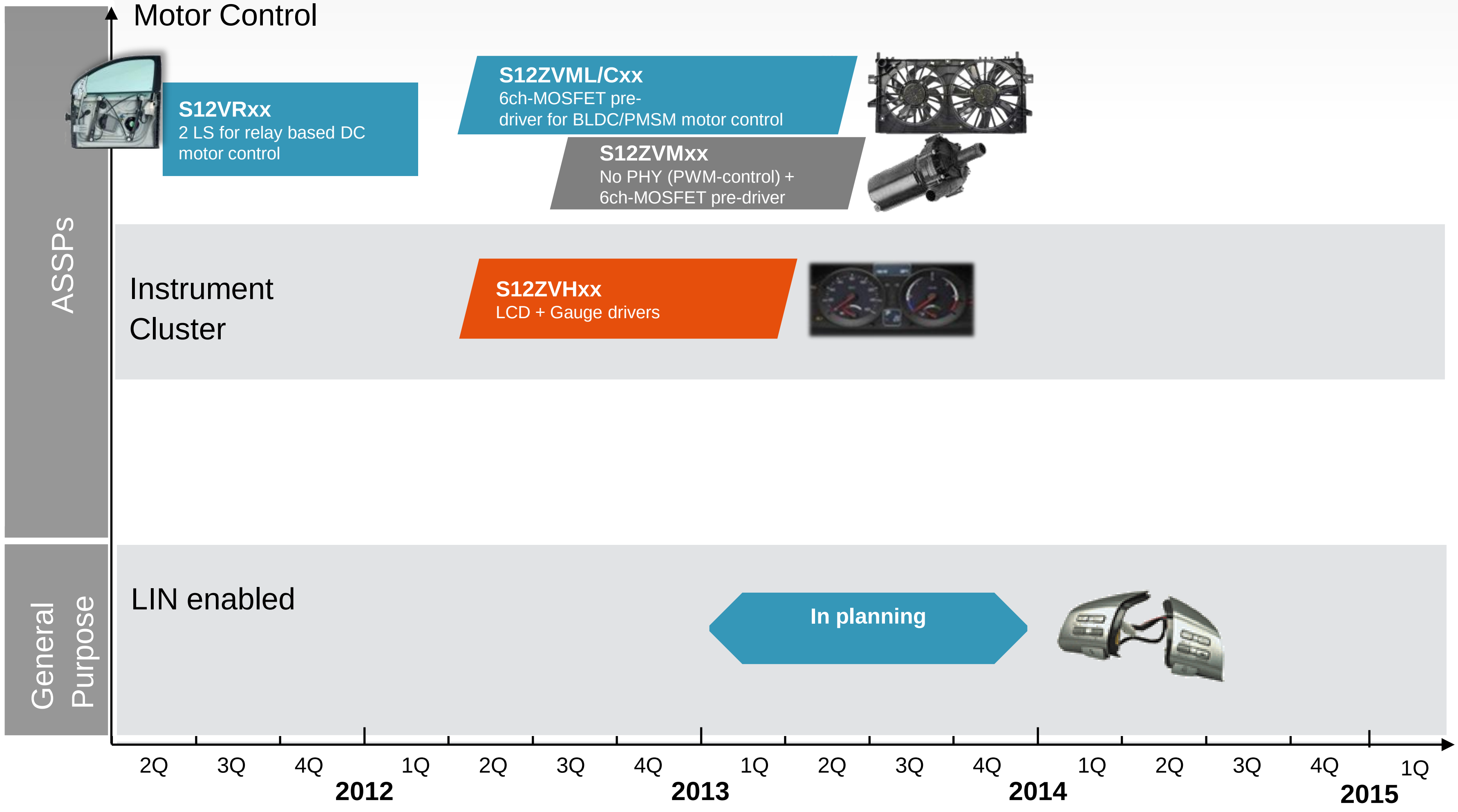
S12 MagniV Roadmap



ASSPs

Motor Control

S12VRxx
2 LS for relay based DC motor control

S12ZVML/Cxx
6ch-MOSFET pre-driver for BLDC/PMSM motor control

S12ZVMxx
No PHY (PWM-control) +
6ch-MOSFET pre-driver

Instrument Cluster

S12ZVHxx
LCD + Gauge drivers

General Purpose

LIN enabled

In planning

🟦 With LIN-PHY

🟧 With CAN-PHY

⬛ No comms (PWM-control)

Production **Execution** **Planning**

First Sample Date (left edge)

Product Qualification (right edge)

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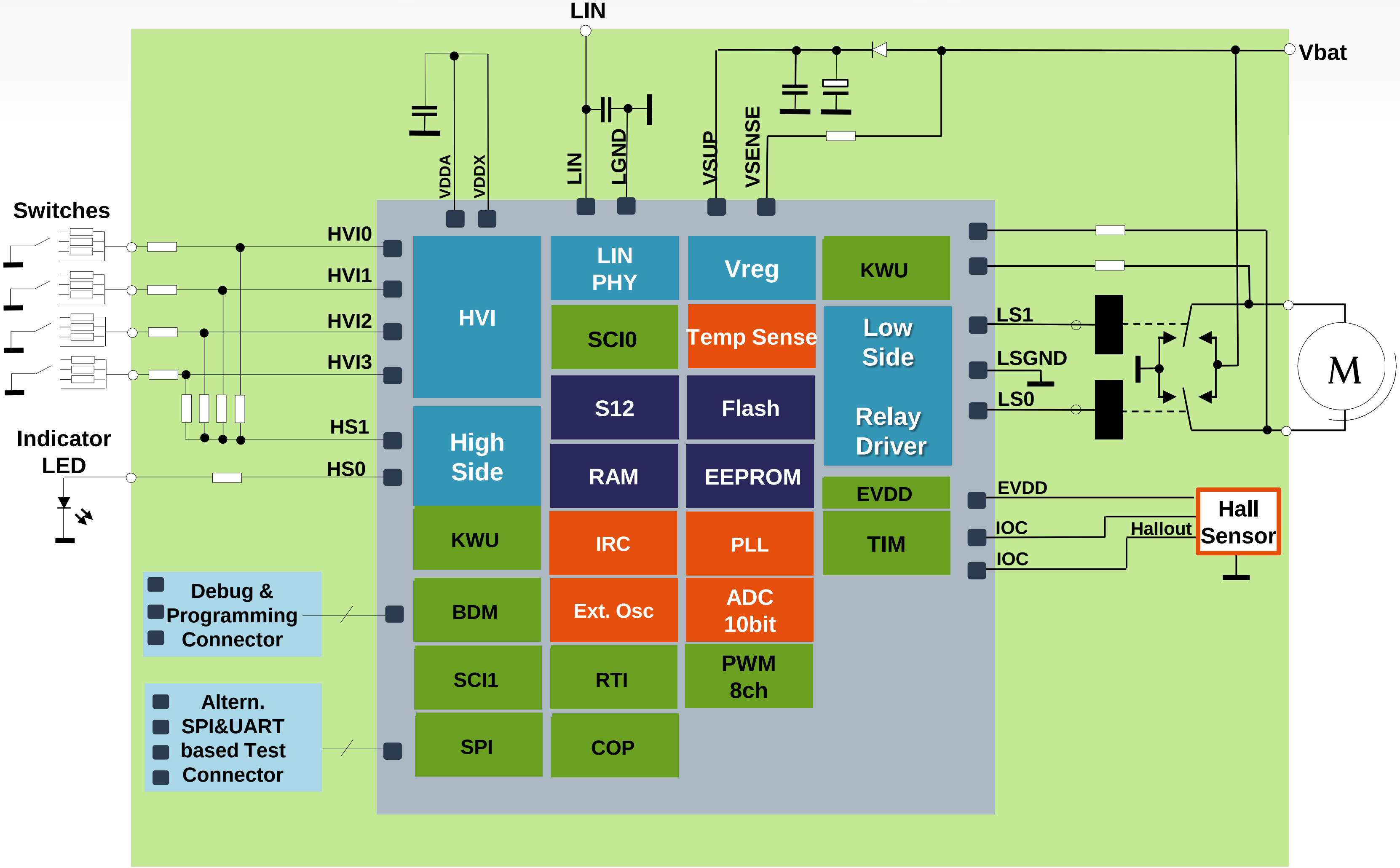
S12VR for Relay Based DC Motor Applications



Pinout representing functionality,
Physical pins location is not correct

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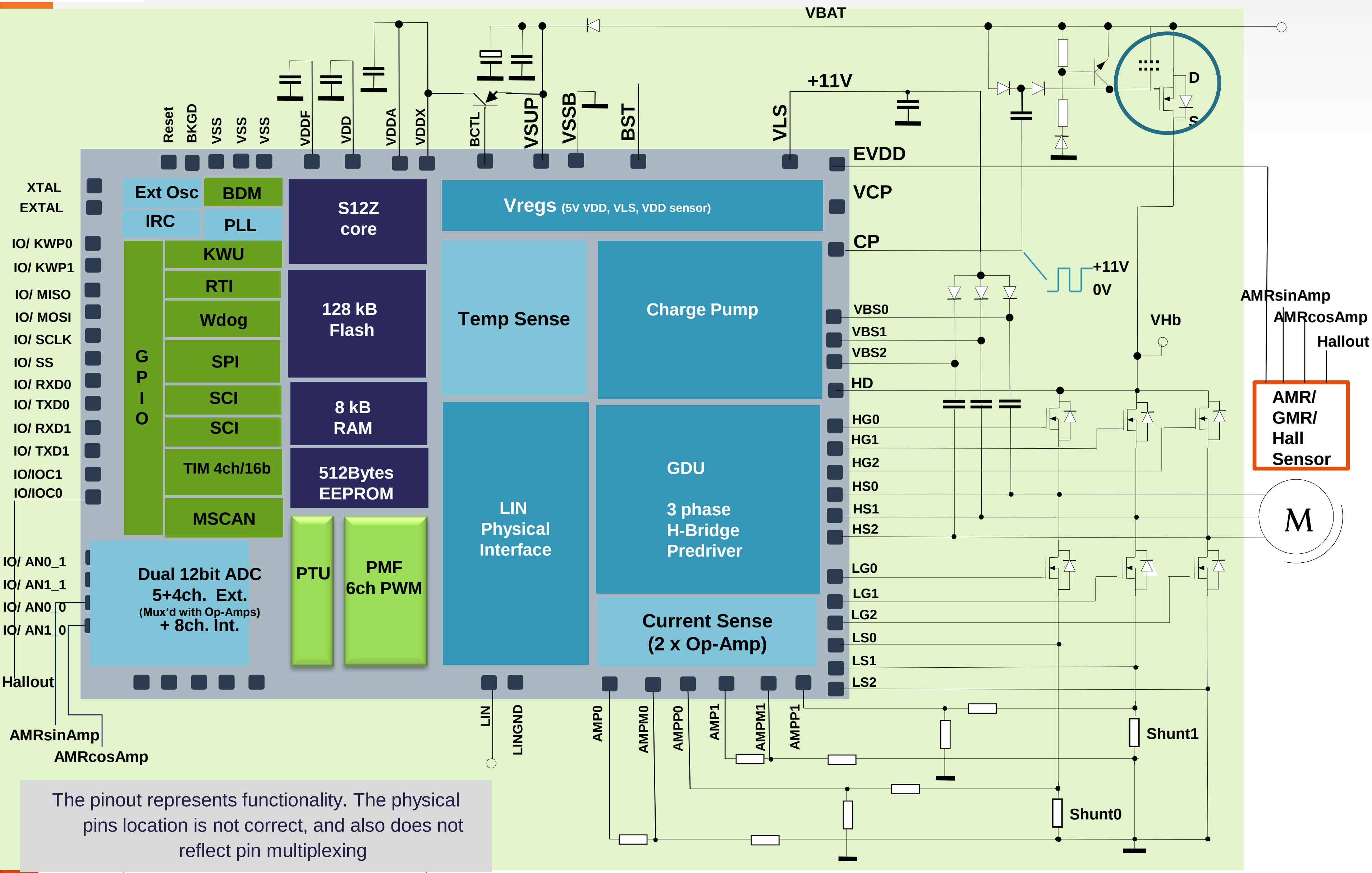
S12ZVM for MOSFET driven BLDC/DC Motor Control



The pinout represents functionality. The physical pins location is not correct, and also does not reflect pin multiplexing

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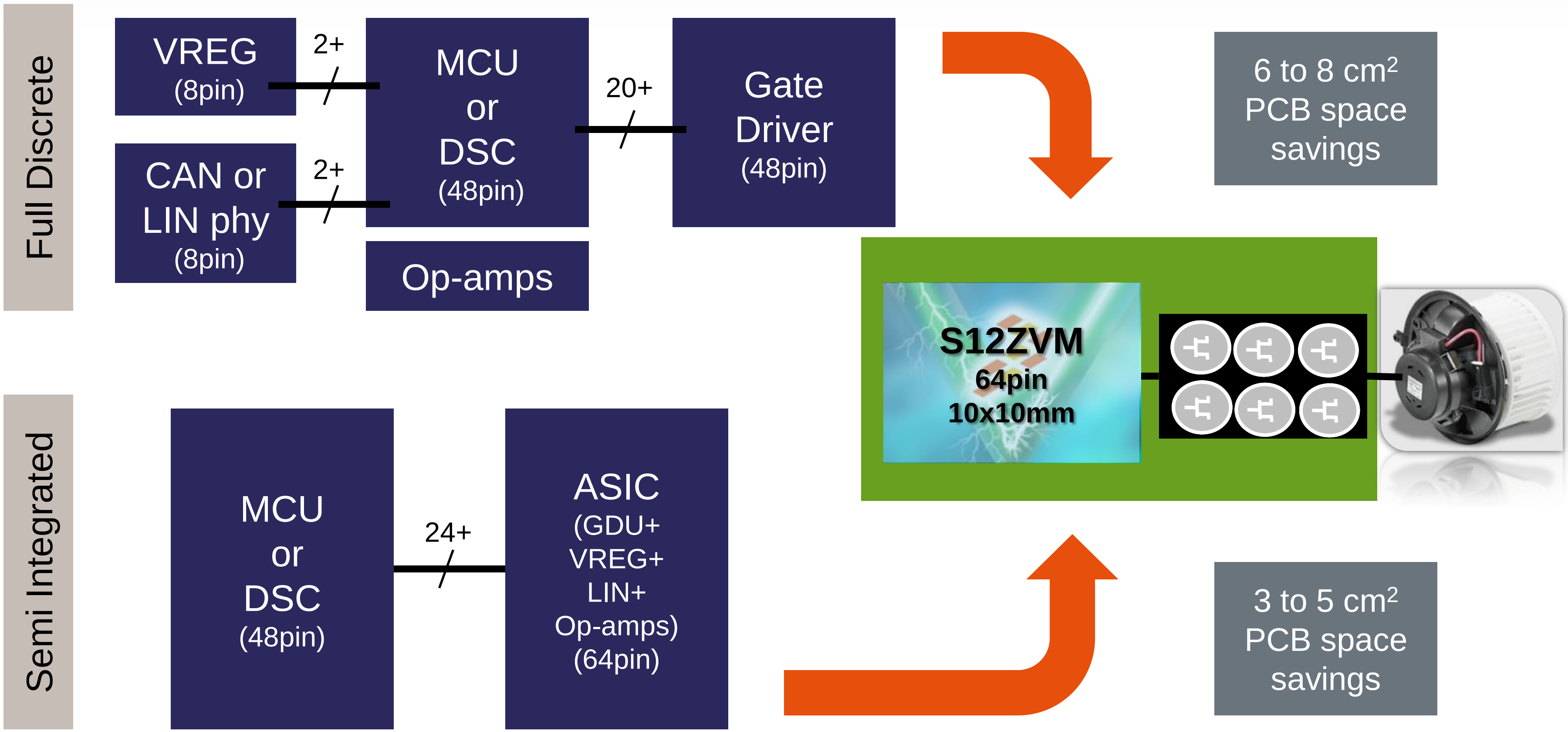
Space Savings with S12ZVM



Full Discrete

VREG
(8pin)

2+

CAN or
LIN phy
(8pin)

2+

MCU
or
DSC
(48pin)

Op-amps

20+

Gate
Driver
(48pin)

6 to 8 cm^2
PCB space
savings

S12ZVM
64pin
10x10mm

Semi Integrated

MCU
or
DSC
(48pin)

24+

ASIC
(GDU+
VREG+
LIN+
Op-amps)
(64pin)

3 to 5 cm^2
PCB space
savings

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Products Benefits

		S12VR	S12ZVML
Product specific benefits	Bill of material reduction	LIN phy VREG + Vsense 2xLS for relays 2xHS	LIN phy VREG + Vsense Gate Driver Op-ampsx2
	PCB Space/Cost	2-4cm^2	3-8cm^2
General benefits	Manufacturing cost	- Fewer components to mount (pick & place) - Less testing required for individual ICs	
	Quality	- Fewer solder joints → fewer points of failure - Pre-tested “sub-system”	
	Logistics	Fewer parts to qualify, source, store, track, etc…	

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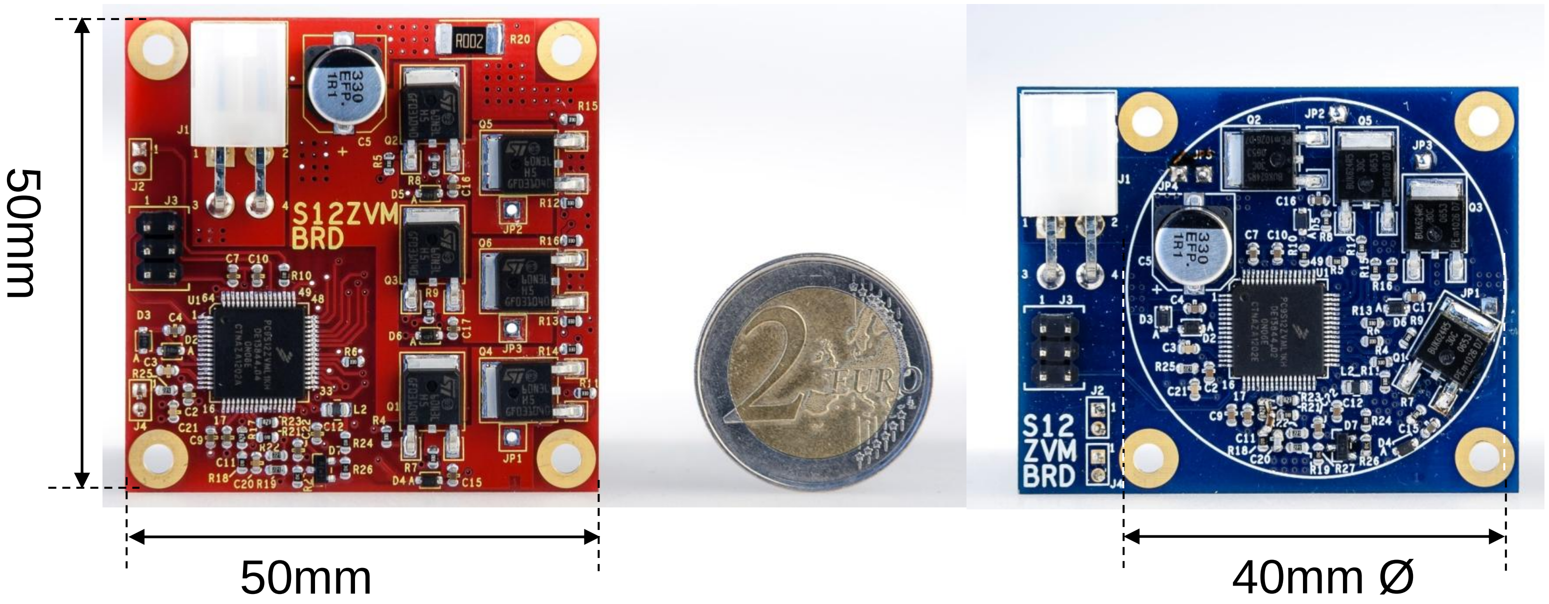
Highest level of Integration

Of your BLDC system:



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Agenda

MagniV Roadmap

S12VM

- Overview
- CPU12Z
- Motor Control
  - Digital
  - Analog

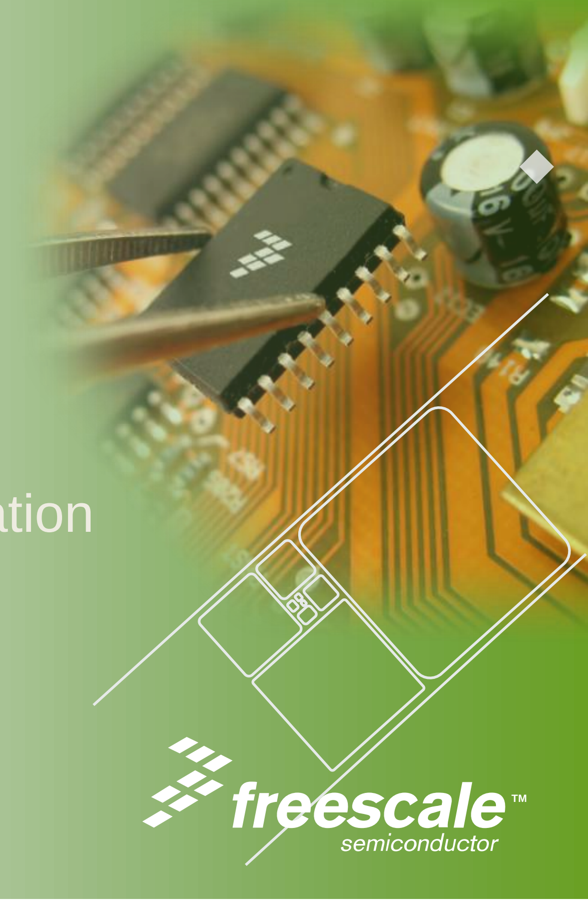
Development Tools

BLDC Sensorless Motor Control Implementation

Position Sensing with Zero Cross Detection

Speed Control

Dynamic Current Limitation



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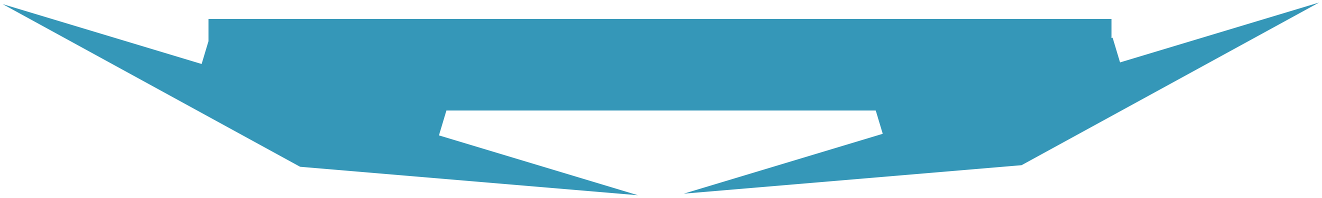
S12ZVM Family Concept

- **Multiple variants to support different multiplexing and motor types**

LIN bus based applications

CAN bus based applications

PWM input based applications



BLDC / PMSM Motors

3-phase pre-driver

DC Motors

2-phase pre-driver

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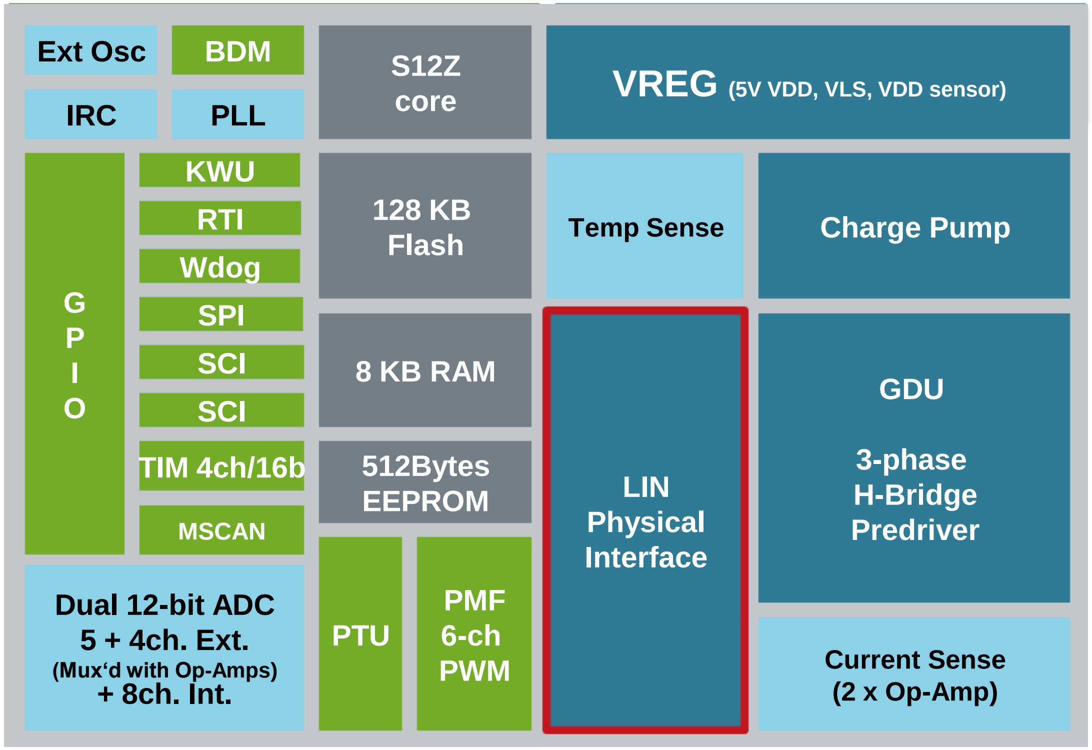
S12ZVM Family Concept – LIN

LIN bus based

- Integrated LIN physical layer
- 48-pin (2-phase) or 64-pin (3-phase) package
- 64KB or 128KB FLASH



S12ZVM**L**128

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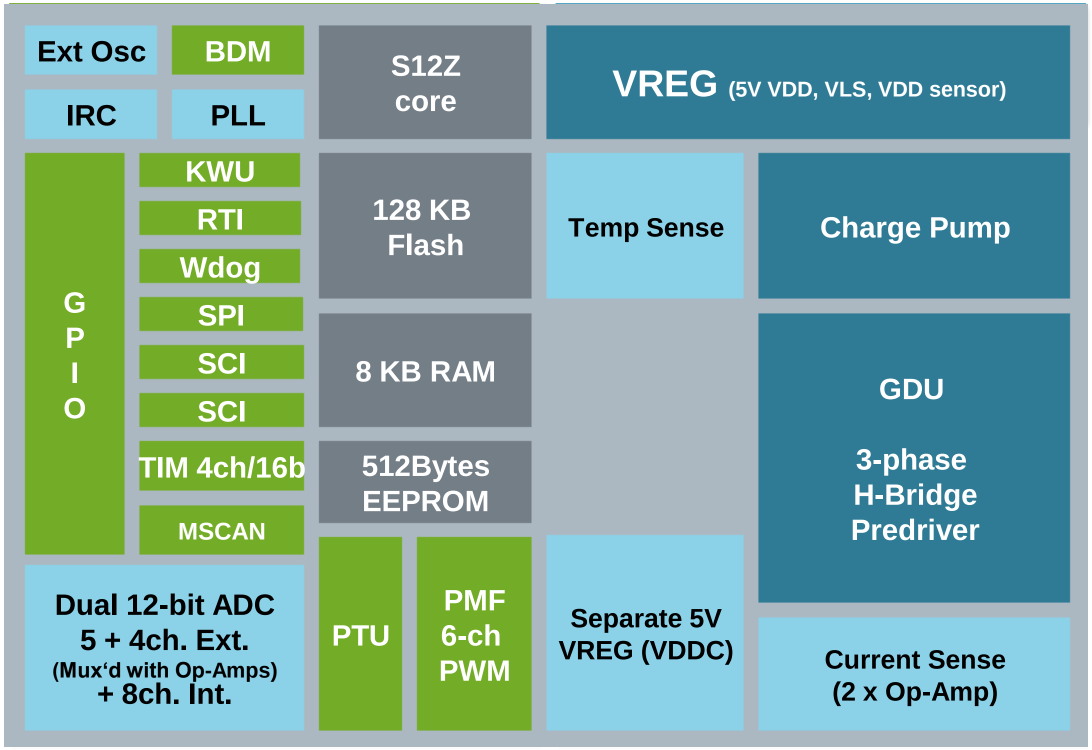
S12ZVM Family Concept – CAN

CAN bus based

- 2^{nd} 5V regulator controller to support an external CAN transceiver
- 48-pin (2-phase) or 64-pin (3-phase) package
- 64KB or 128KB FLASH



Ext Osc

BDM

IRC

PLL

S12Z core

VREG (5V VDD, VLS, VDD sensor)

G P I O

KWU

RTI

Wdog

SPI

SCI

SCI

TIM 4ch/16b

MSCAN

128 KB Flash

8 KB RAM

512Bytes EEPROM

Temp Sense

Charge Pump

GDU

3-phase H-Bridge Predriver

Dual 12-bit ADC
5 + 4ch. Ext.
(Mux'd with Op-Amps)
+ 8ch. Int.

PTU

PMF 6-ch PWM

Separate 5V VREG (VDDC)

Current Sense (2 x Op-Amp)

S12ZVMC128

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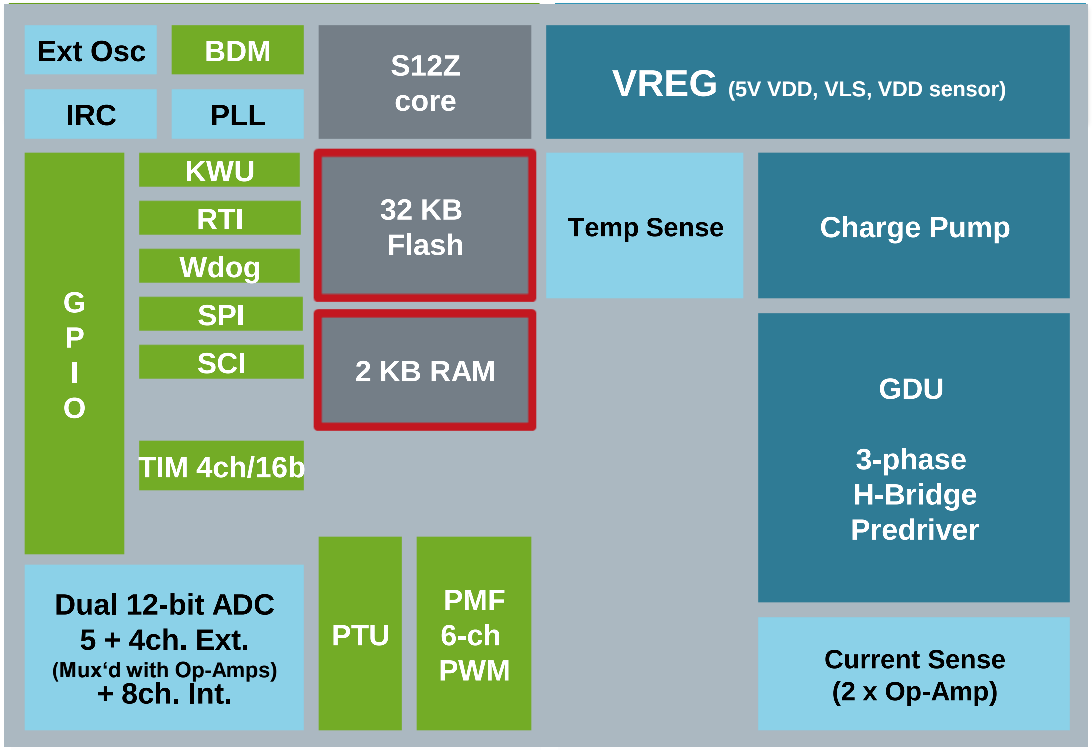
S12ZVM Family Concept – PWM

- No MSCAN controller / no LIN physical layer
- 48-pin (2-phase) or 64-pin (3-phase) package
- 32KB FLASH


Ext Osc
BDM
IRC
PLL
S12Z core
VREG (5V VDD, VLS, VDD sensor)
G P I O
KWU
RTI
Wdog
SPI
SCI
TIM 4ch/16b
32 KB Flash
2 KB RAM
Temp Sense
Charge Pump
GDU
3-phase H-Bridge Predriver
Dual 12-bit ADC 5 + 4ch. Ext. (Mux'd with Op-Amps) + 8ch. Int.
PTU
PMF 6-ch PWM
Current Sense (2 x Op-Amp)

S12ZVM32

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S12ZVM Family Feature Summary

Flash /RAM Size	128 KB / 8 KB				64 KB / 4 KB				32 KB / 2 KB	
Connectivity	LIN		CAN		LIN		CAN		PWM	
Product Name	S12ZVML128		S12ZVMC128		S12ZVML64		S12ZVML64		S12ZVM32	
Motor Type	BLDC/ PMSM	DC	BLDC/ PMSM	DC *	BLDC/ PMSM	DC	BLDC/ PMSM	DC *	BLDC/ PMSM	DC *
Pin count	64	48	64	48	64	48	64	48	64	48
EEPROM (bytes)	512	512	512	512	512	512	512	512	-	-
LIN PHY	1	1	0	0	1	1	0	0	0	0
2nd VREG	0	0	1	1	0	0	1	1	0	0
GDU (HS / LS)	3 / 3	2 / 2	3 / 3	2 / 2	3 / 3	2 / 2	3 / 3	2 / 2	3 / 3	2 / 2
PWM channels	6	4	6	4	6	4	6	4	6	4
ADC (ext. channels)	4 + 5	3 + 3	4 + 5	3 + 3	4 + 5	3 + 3	4 + 5	3 + 3	4 + 5	3 + 3
MSCAN	1	1	1	1	1	1	1	1	0	0
SCI	2	2	2	2	2	2	2	2	1	1
SPI	1	1	1	1	1	1	1	1	1	1
TIM	4	3	4	3	4	3	4	3	4	3

*Upon Request

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Overview of S12ZVM Feature Set

Internal RC osc.
- +/-1.3% over tmp

Sensor Supply
- 20mA I/O for sensor

Window Watchdog
- independent RC osc

2 UARTs
- one linked to LIN Phy
- 2nd as test interface

Multiple timers
- IOC/periodic wakeup

CAN Option
- CAN controller

Two 12bit ADC

•List Based Architecture allows flexible definition of order and number of conversions
- 2.5µs conv. time

New S12Z CPU
- Up to 100MHz
- 32-bit ALU & 32bit MAC unit,
- Optimized 32-bit math. operations

Safe RAM

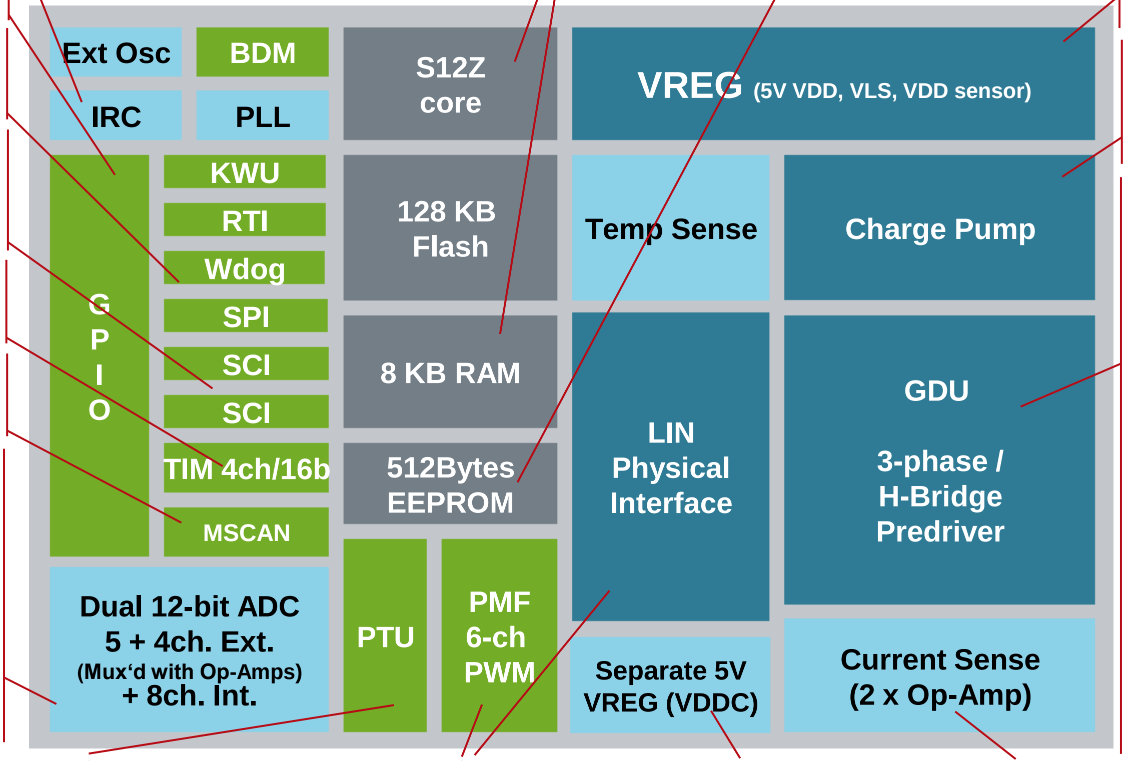
ECC

Flash& EEPROM
- ECC
- Memory Protection
- Margin Read

Voltage Regulator
- Boost Option
- Support for external ballast transistor
- Vbat sense

Charge Pump
- Optional to support 100% duty cycle

Gate Drive Unit
- Operational from 3.5V to 26V
- Bootstrap circuit based
- 11V Vreg
- Phase comparators
- Desaturation comp. for HS/LS protection
- Under-/Over-voltage detection
- DC-link and phase voltage internally accessible on ADC
- Selectable HS/LS slew rate



Programmable Trigger Unit
- synchronize ADC to PWM
- Trigger Command list with up to 32 triggers per cycle

PWM Module
- Complementary mode with deadtime ctrl.
- Fault protection
- Double-Switching

LIN Phys. Interface
- 250kb/s fast mode
- +/-6kV

CAN Support
- 5V Vreg controller for external transceiver

Current Sense Amplifiers
- 2-shunt system supported with additional selectable over-current protection comparator

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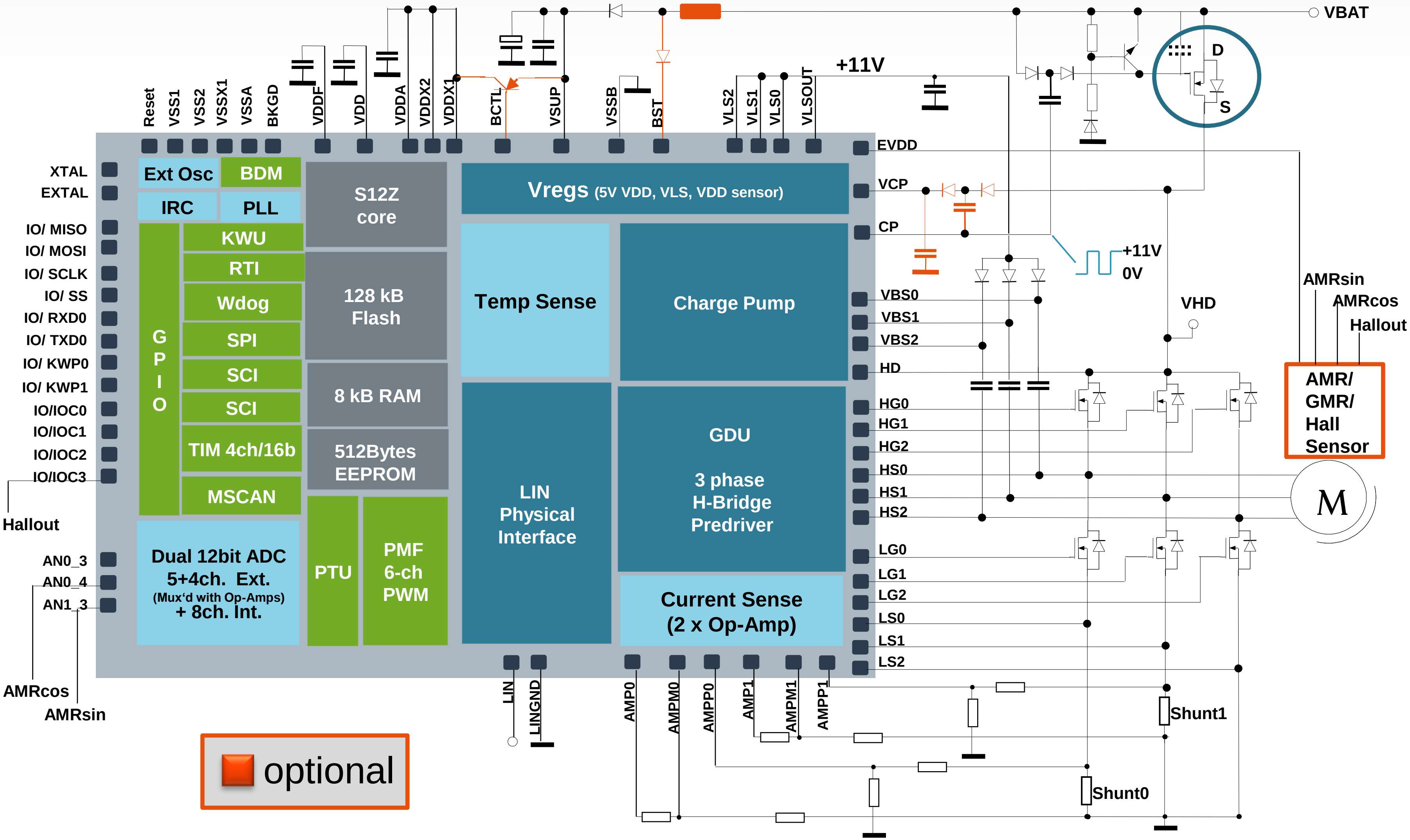
S12ZVML Application Schematic



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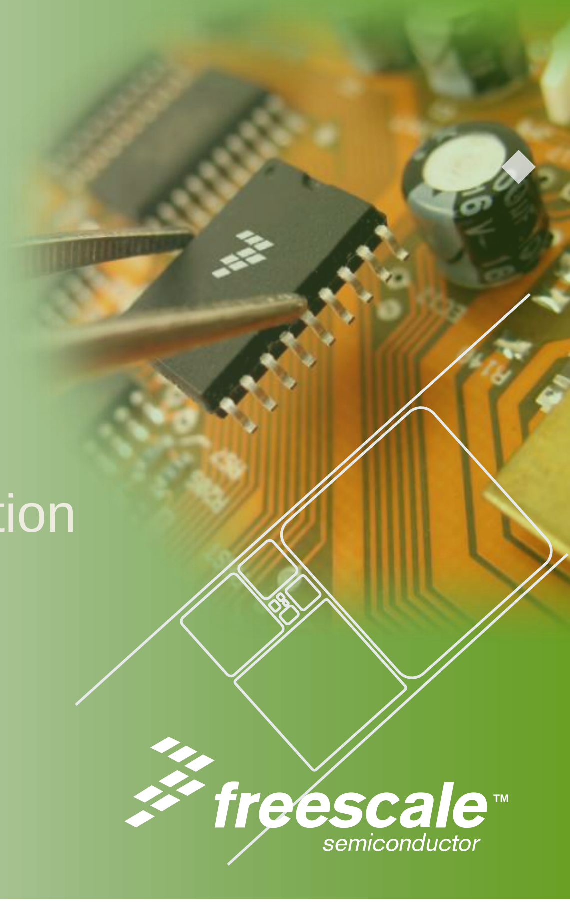
Agenda

- MagniV Roadmap
- S12VM
  - Overview
  - CPU12Z
  - Motor Control
    - Digital
    - Analog
- Development Tools
- BLDC Sensorless Motor Control Implementation
- Position Sensing with Zero Cross Detection
- Speed Control
- Dynamic Current Limitation



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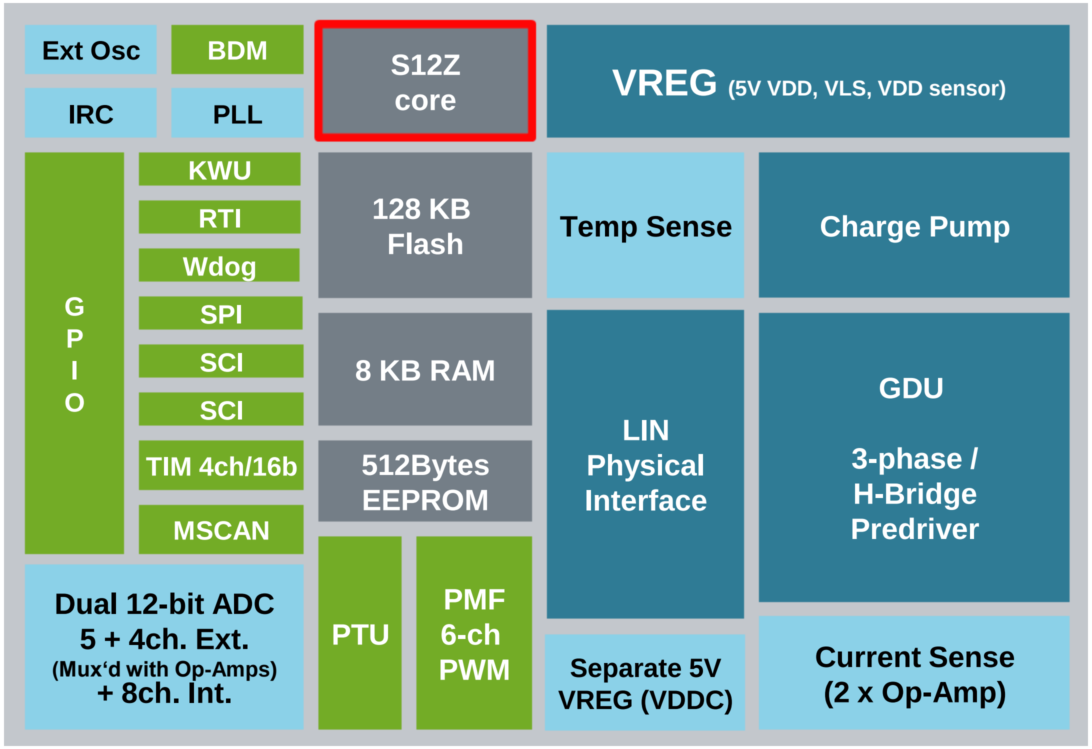
S12Z Core



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S12Z Core Overview

- The S12Z CPU is the next generation of CPU in the CPU12 line.
  - High-speed 16-bit processor with an expanded programmers model
  - Improved addressing modes support efficient use of the 16MB (24-bit) linear address space.
  - Improved support for C code-size efficiency and overall performance

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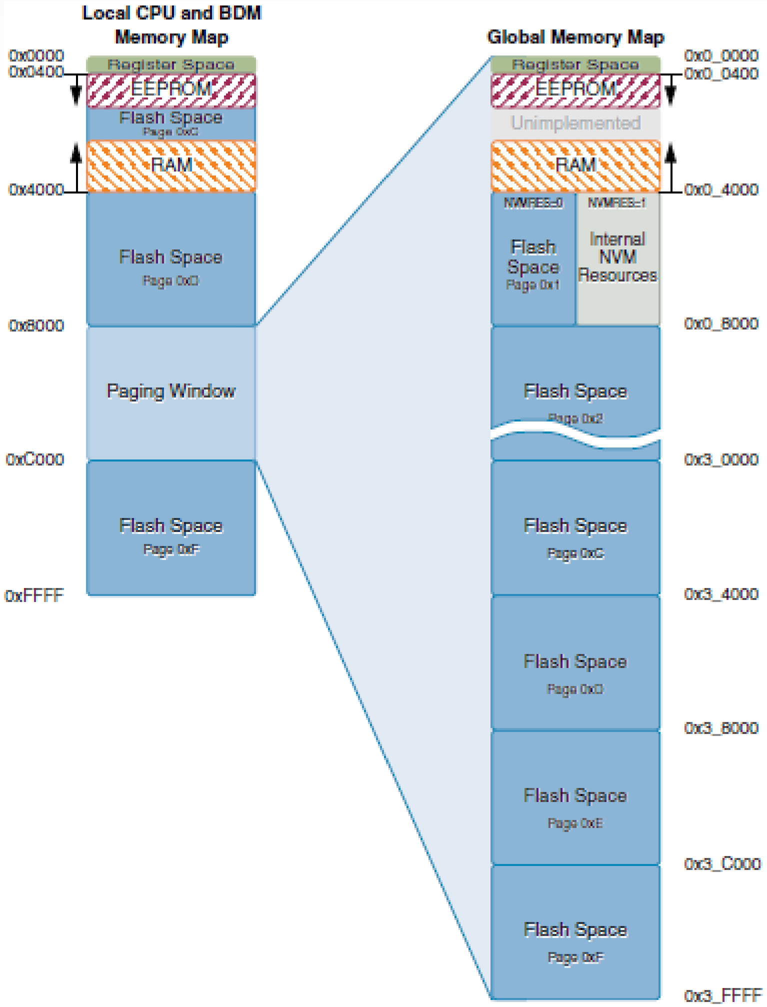
Linear vs. Paged Addressing Mode

- S12 MCUs typical architecture provides 64KB memory space
  - To achieve extended memory sizes, a paging mechanism is needed
    - 256 pages of 16kB each = 4MB maximum
  - Paging is one of the biggest dissatisfiers from the customers' perspective



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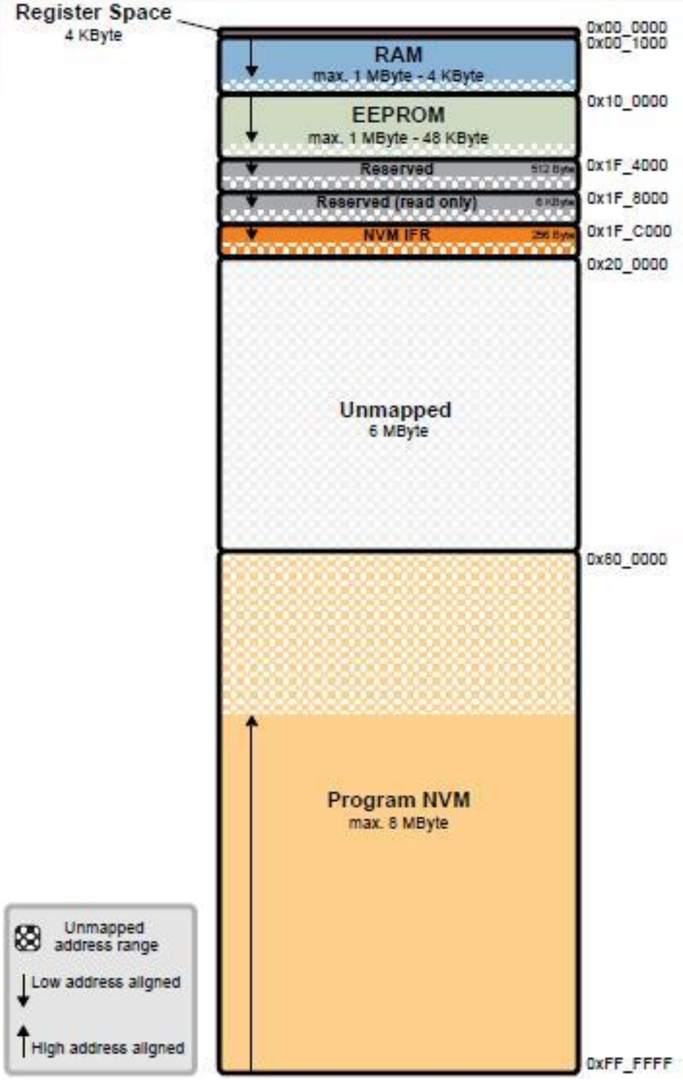
Linear vs. Paged Addressing Mode

- The S12Z CPU includes a 24-bit address bus, which provides up to 16MB memory space
- Linear addressing simplifies memory accesses



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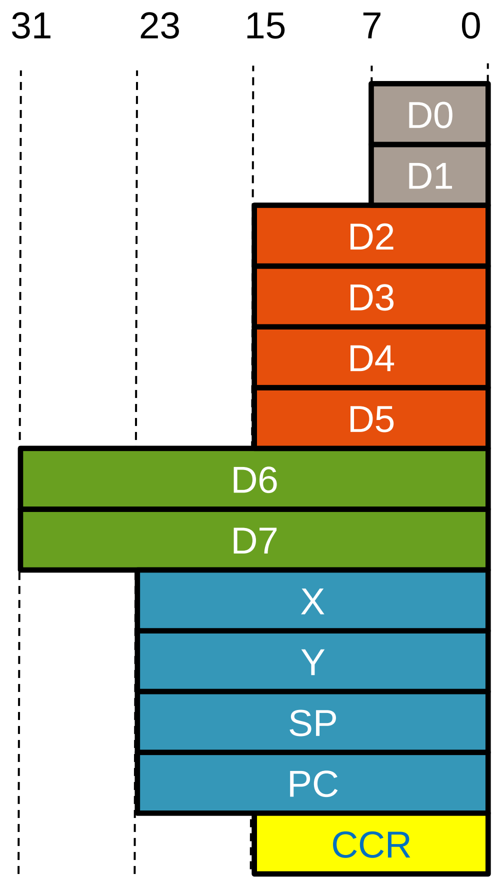
S12Z Core Architecture … a 16-bit MCU?

- It uses 32-Bit data paths, ALU, Data registers
  - Single-cycle 16x16 multiply (2.5 cycles 32x32)
  - MAC unit 32bit += 32bit*32bit (3.5 cycles)
  - Hardware divider 32bit = 32bit/32bit (18.5 cycles)
  - Single cycle multi-bit shifts (Barrel shifter)
  - Fractional Math support
- It uses a 24-bit address bus, Stack Pointer, Program Counter and Index registers
- Its native "int" data type is 16-bit, with 16-bit I/O data path
- It can handle 8-Bit data and indexes better than S12X
- CPU operates at 100MHz
  - Optimized bus architecture with 100MHz load and store to RAM
  - NVM works with 1 Wait-state => effective 20ns accesses
- Harvard Architecture => parallel code and data access
  - Instructions and addressing modes optimized for C programming and compiler

Expanded programmer's model



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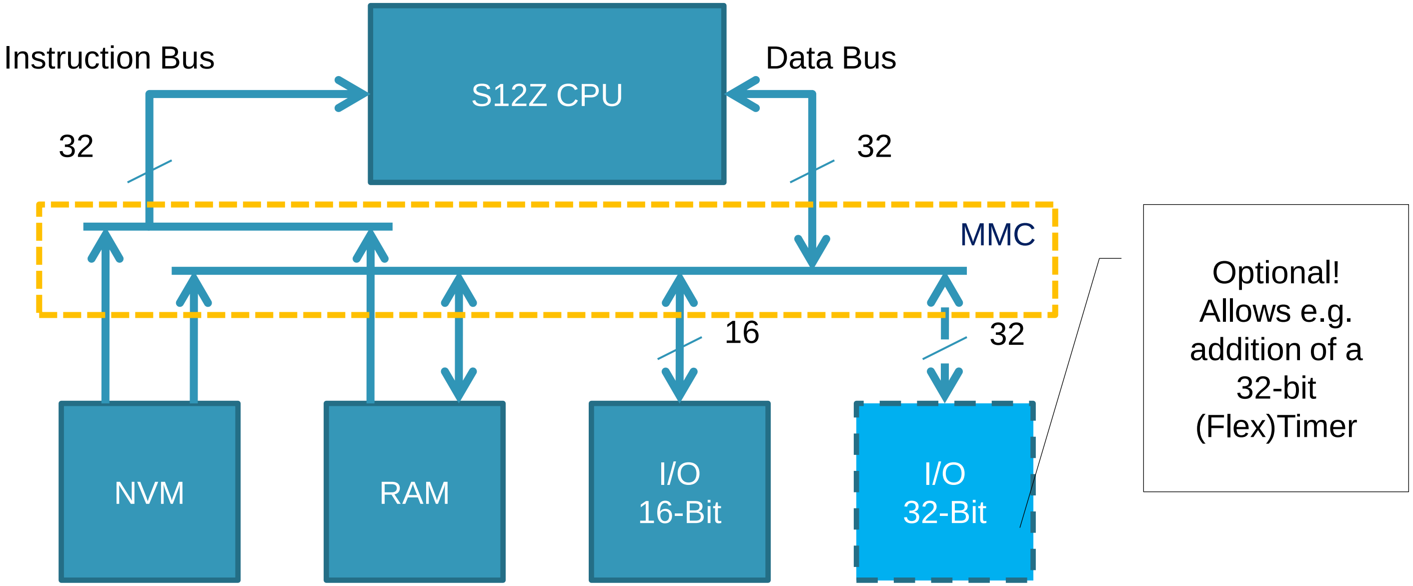
S12Z Platform Architecture

- Harvard Architecture (Parallel Data and Code access)



Optional! Allows e.g. addition of a 32-bit (Flex)Timer

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S12Z vs. S12X – Features

Attribute	S12Z	S12XE
Architecture	Harvard	Von Neumann
Address space	16MByte Linear	64KByte Linear (up to 4MByte Paged)
Data Bus Width	32-Bit RAM & Flash, 16-Bit I/O	16-Bit
ALU Width	32-Bit	16-Bit
Data Registers	2 x 8-Bit, 4 x 16-Bit, 2 x 32-Bit	2 x 8-Bit (can be used as a single 16-Bit accumulator)
Pointers	2 x 24-Bit	2 x 16-Bit

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S12Z vs. S12X – Performance

Attribute	S12Z	S12XE
Bit Shifter	32-bit multi-bit 1 cycle	16-bit single-bit 2cycles
Multiplier	32*32 2.5cycles 16*16 1cycle	16*16 1cycle
Divider	32 = 32/32 18.5cycles	32 = 32/16 11cycles
MAC	32 += 32*32 3.5cycles	32 += 16*16 13cycles
Fractional math support	Yes	No
Bus speed	50MHz	50MHz

- CPU operates at up to 100MHz, bus at 50 MHz
  - RAM bus can load and store w/ 100MHz
  - I/O buses @50MHz to reduce power consumption and die area

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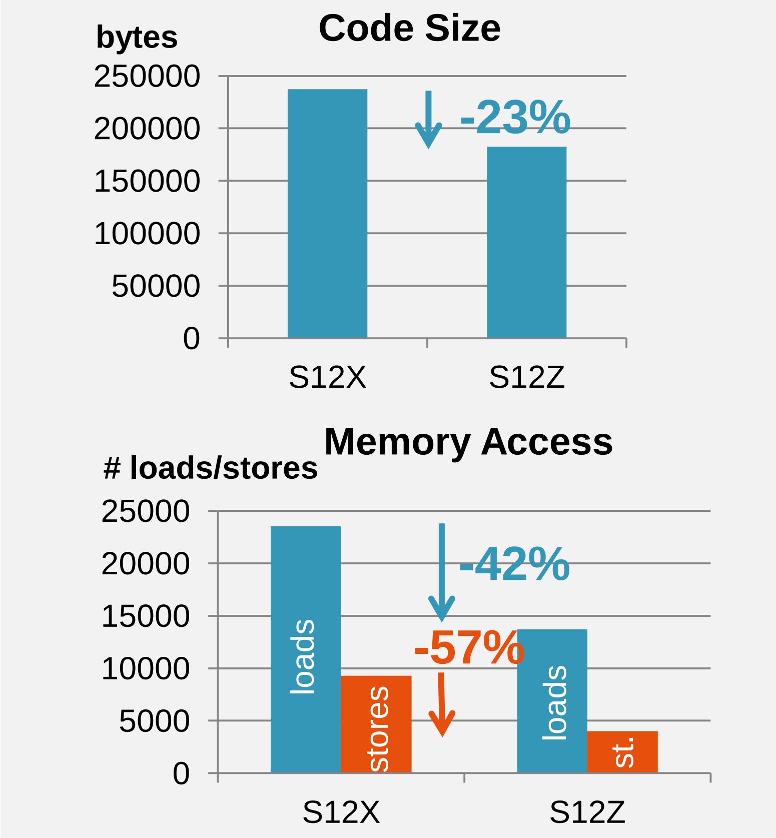
S12Z Benchmarks Results

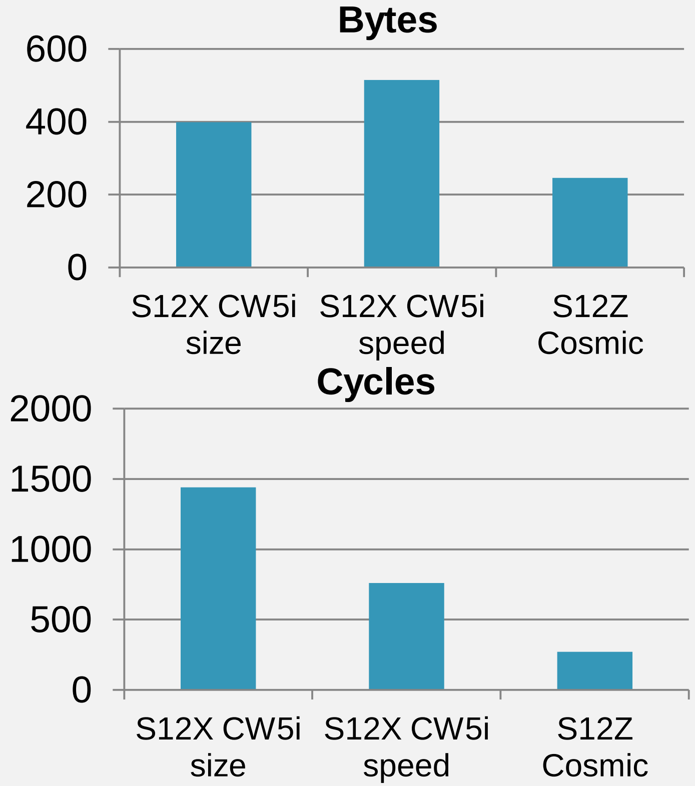
- **S12Z typically saves 20% code size versus S12X**
- **S12Z typically uses 30% less memory accesses than S12X which saves power**

Large Application Code Example:



Digital Filter:

S12Z is faster and denser than any optimization option of S12X



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In Depth Code Size Analysis

Feature	S12X	S12Z	Comment
Code Size	237277	182362	-23%
pg1	86.3%	96.9%	Shows well chosen pg1 instructions
Loads	23550	13725	-42%
Stores	9280	4015	-57%
Moves	4347	4332	About equal

- Code is about 200k byte large Body Application
  - Significant code size savings
  - Large reduction of memory instructions (not accesses!)
    - => Power Savings expected

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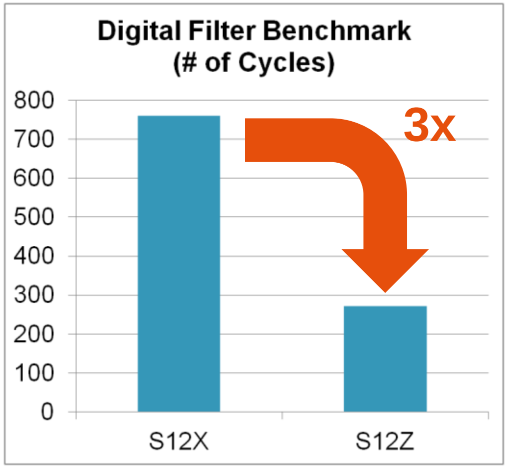
S12Z Performance Benefits

Improved Performance for Motor Control

- 100 MHz CPU @ 50 MHz bus speed
- Harvard architecture accelerates data handling



- Fractional math instructions added

Improved Software Friendliness

- 24-bit linear address map to ease software development and porting
- Added 8- and 32-bit registers to allow further compiler code size optimization

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Agenda

MagniV Roadmap

S12VM

- Overview
- CPU12Z
- Motor Control
  - Digital
  - Analog

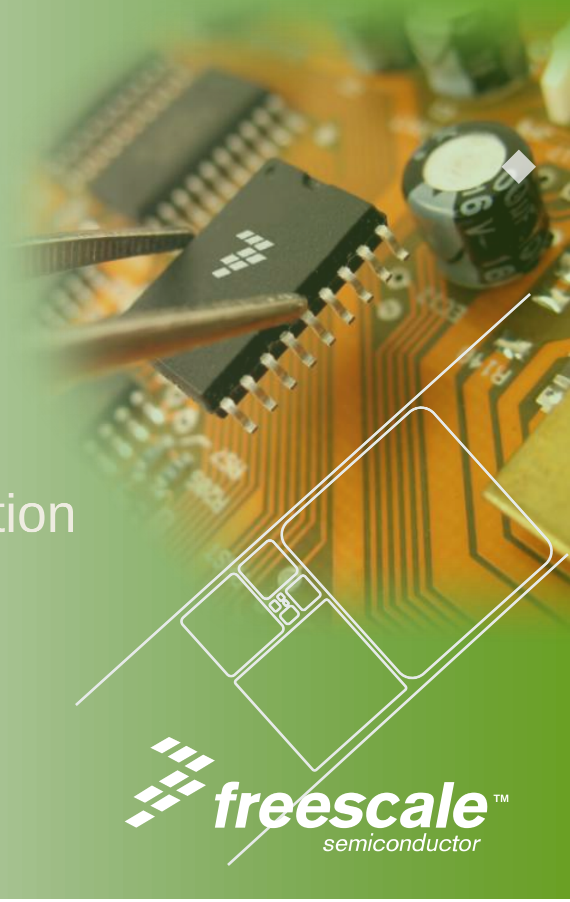
Development Tools

BLDC Sensorless Motor Control Implementation

Position Sensing with Zero Cross Detection

Speed Control

Dynamic Current Limitation



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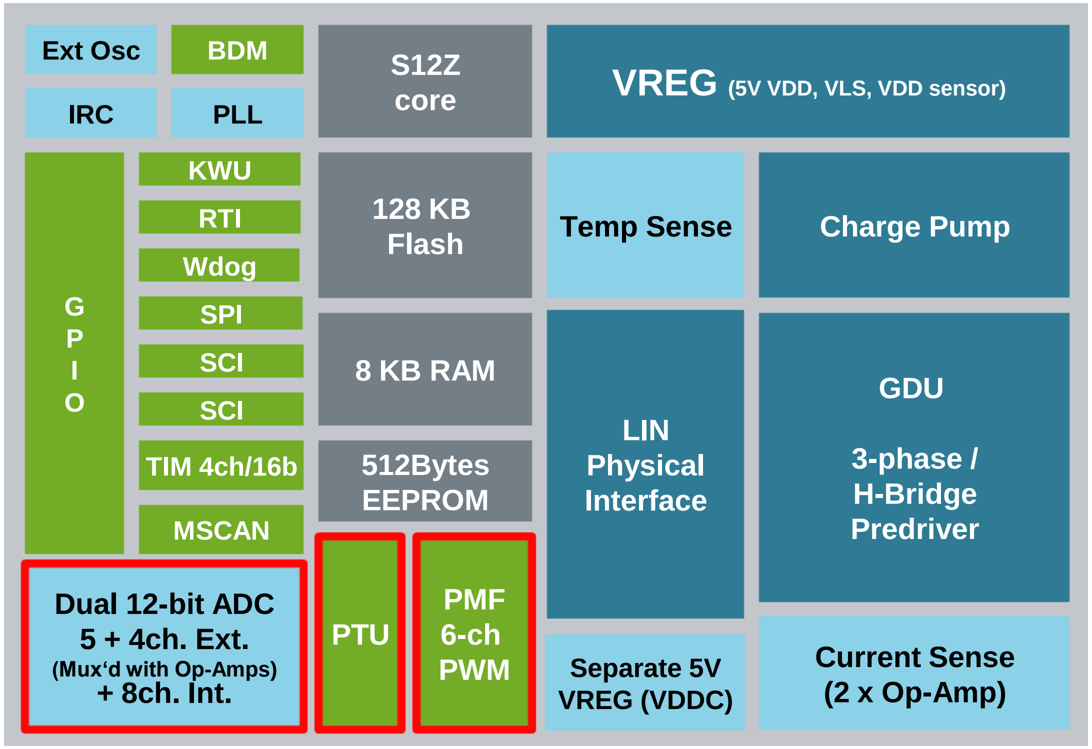
Motor Control Loop Related Modules



Ext Osc

BDM

IRC

PLL

S12Z core

VREG (5V VDD, VLS, VDD sensor)

GPIO

KWU

RTI

Wdog

SPI

SCI

SCI

TIM 4ch/16b

MSCAN

128 KB Flash

8 KB RAM

512Bytes EEPROM

Temp Sense

Charge Pump

LIN Physical Interface

GDU

3-phase / H-Bridge Predriver

Dual 12-bit ADC
5 + 4ch. Ext.
(Mux'd with Op-Amps)
+ 8ch. Int.

PTU

PMF 6-ch PWM

Separate 5V VREG (VDDC)

Current Sense (2 x Op-Amp)

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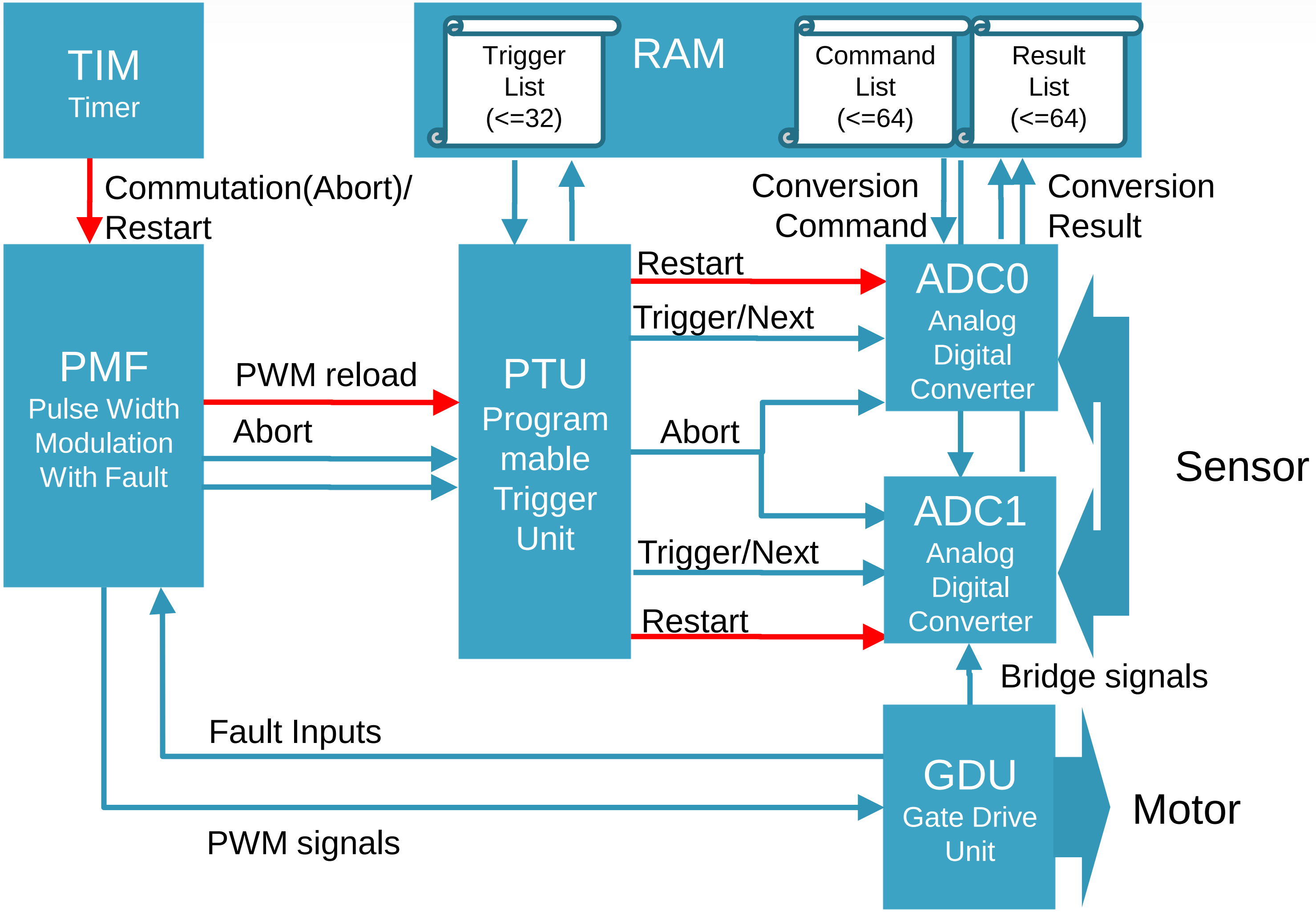
Motor Control Control Loop Implementation

- **One control cycle can be a PWM cycle or a number of PWM cycles.**



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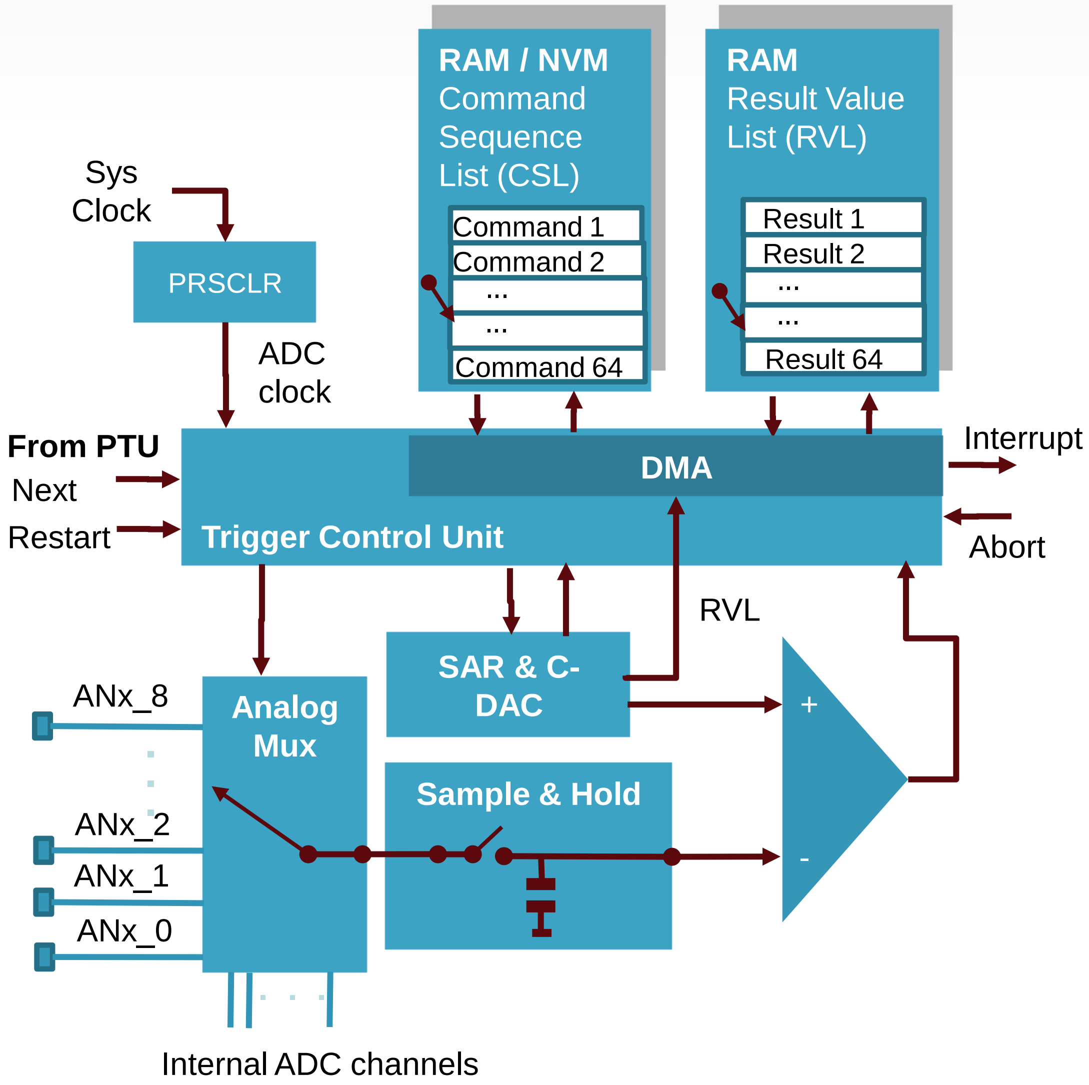
12-bit SAR ADC

- **2 independent converters:**
  - ADC0 (5 ext ch. + 5 int. ch.)
  - ADC1 (4 ext ch. + 4 int. ch.)
- **2.5µsec conversion time**
- **List Based Architecture**
  - Double buffered Command and Results list, so that CPU can load new values in the background
  - Provides flexible conversion sequence definition and oversampling.
- **Can be triggered by PTU, for accurate synch with PWM**
- **DMA taking commands from SRAM /NVM and storing results back into SRAM**



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ADC – Internal Channels

- **Internal Channels give access to following internal signals**

	Channel Select						ADC Channel	Signal
ADC0	0	0	1	0	0	0	Internal_0	ADC0 temperature sensor
	0	0	1	0	0	1	Internal_1	VREG temperature sensor or Bandgap voltage
	0	0	1	0	1	0	Internal_2	GDU phase multiplexer voltage
	0	0	1	0	1	1	Internal_3	GDU DC link voltage monitor
	0	0	1	1	0	0	Internal_4	BATS VSUP sense voltage

	Channel Select						ADC Channel	Signal
ADC1	0	0	1	0	0	0	Internal_0	ADC1 temperature sensor
	0	0	1	0	0	1	Internal_1	VREG temperature sensor or Bandgap voltage
	0	0	1	0	1	0	Internal_2	GDU phase multiplexer voltage
	0	0	1	0	1	1	Internal_3	GDU DC link voltage monitor

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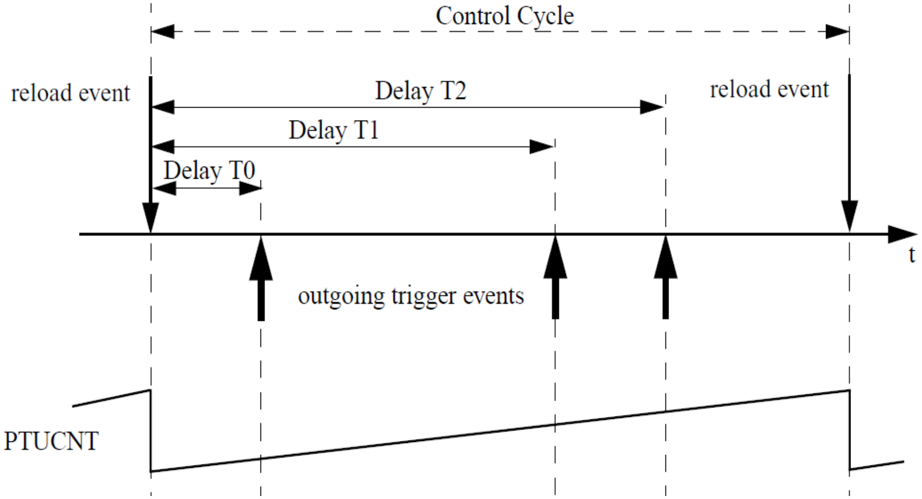
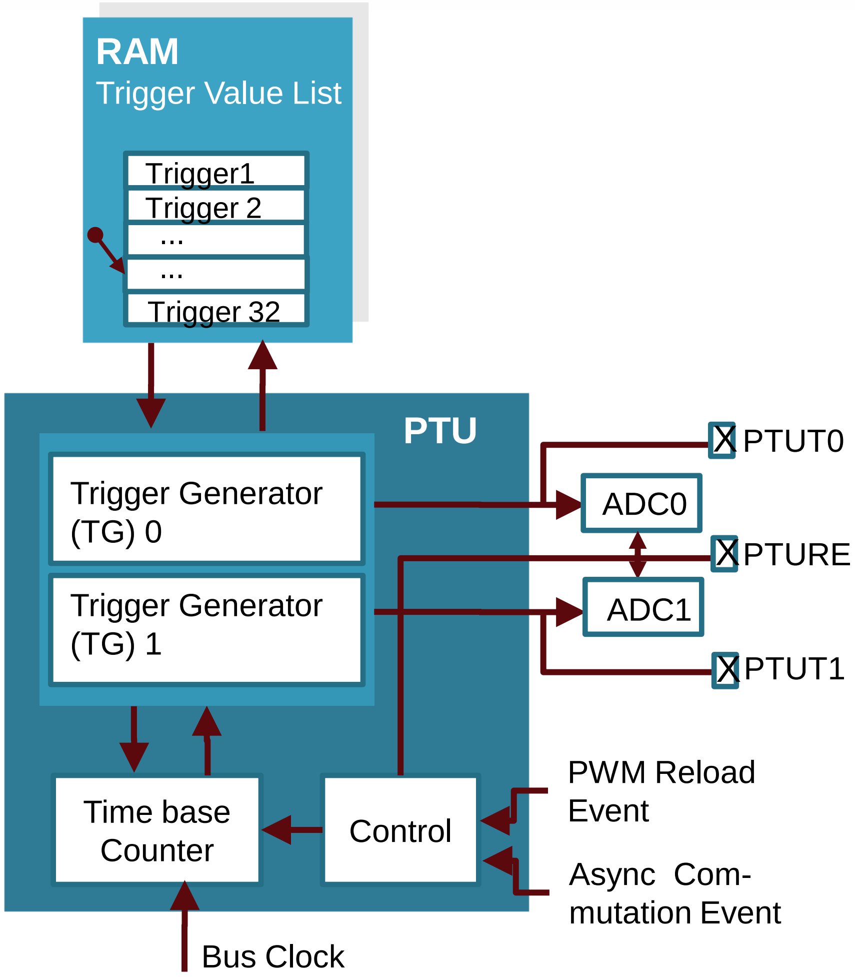
Programmable Trigger Unit (PTU)

Completely avoids CPU involvement to trigger ADC during the control cycle

- One 16-bit counter as time base for all trigger events
- Two independent trigger generators (TG)
- Up to 32 trigger events per trigger generator
- Trigger Value List stored in system memory
- Double buffered list, so that CPU can load new values in the background
- Software generated “Reload” event
- Software generated trigger event
- Global Load OK support, to guarantee coherent update of all control loop modules





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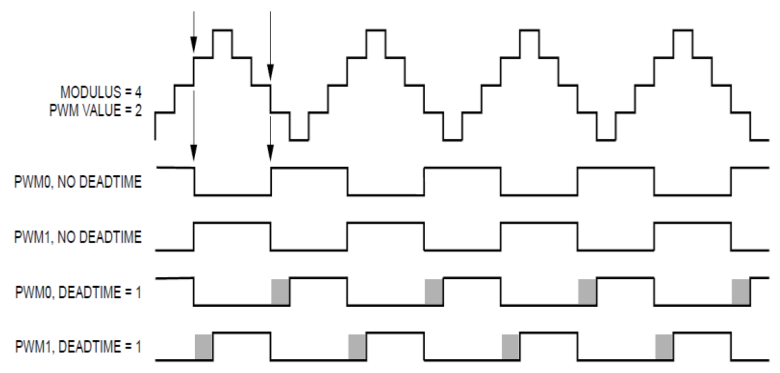
Pulse Width Modulator Module (PMF)

- **Up to 6 independent PWM channels or up to 3 complementary pairs**
- **Three 15-bit counters based on core clock (max. 100MHz)**
- **Complementary channel operation with**
  - Dead time insertion
  - Separate top and bottom pulse width correction
  - Asymmetric PWM output within center-aligned mode (phase shift)
  - Double switching
  - Separate top and bottom polarity control
- **Edge-aligned or center-aligned PWM signals**
- **Half-cycle reload capability**
- **Integral reload rates from 1 to 16**
- **Optional counter restart from Timer output compare for 6-step BLDC commutation support**
- **Reload overrun interrupt**
- **Individual software-controlled PWM output**
- **Programmable fault protection**
- **PWM compare output polarity control**
- **PWM output polarity control**

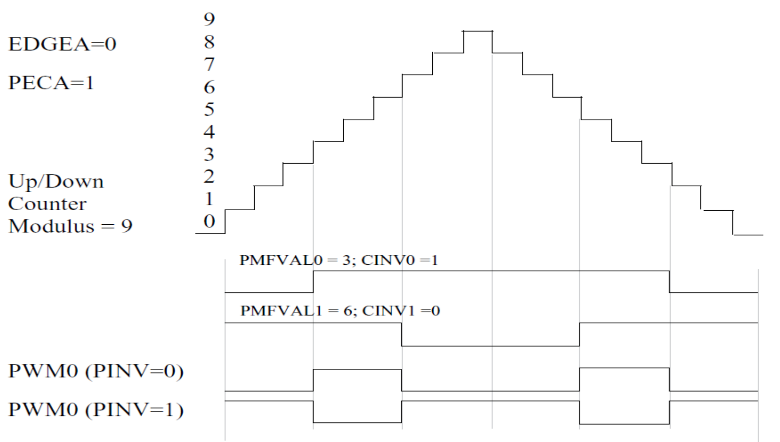
Complementary Mode

with / without dead time insertion



Double-Switching Mode

for single shunt system



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Agenda

MagniV Roadmap

S12VM

- Overview
- CPU12Z
- Motor Control
  - Digital
  - Analog

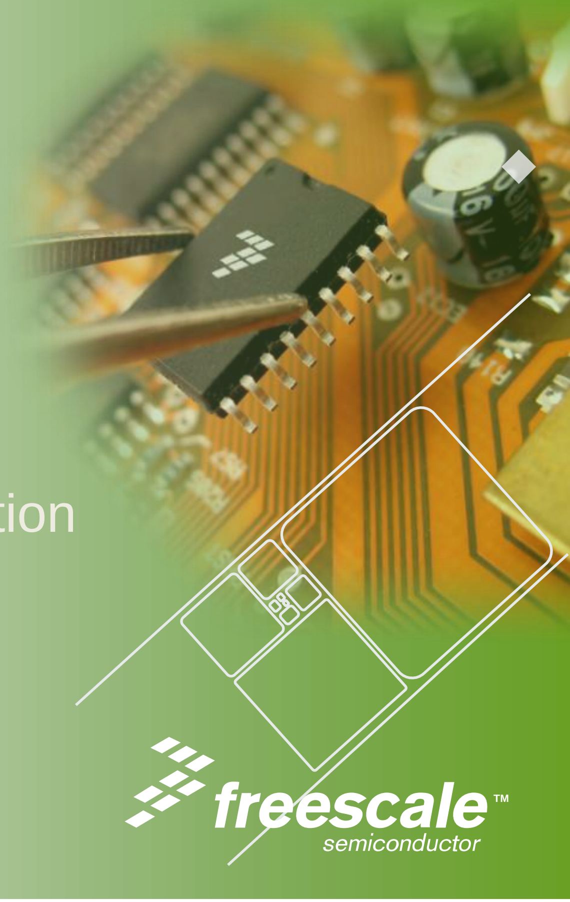
Development Tools

BLDC Sensorless Motor Control Implementation

Position Sensing with Zero Cross Detection

Speed Control

Dynamic Current Limitation



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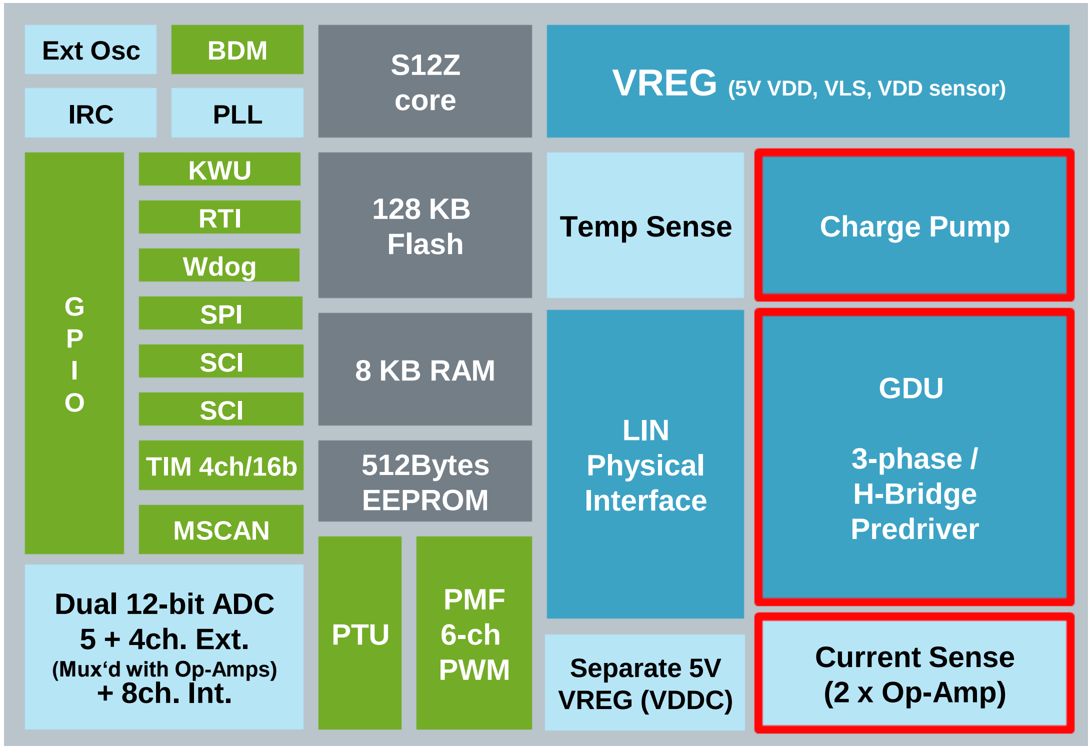
Motor Control Loop Related Modules



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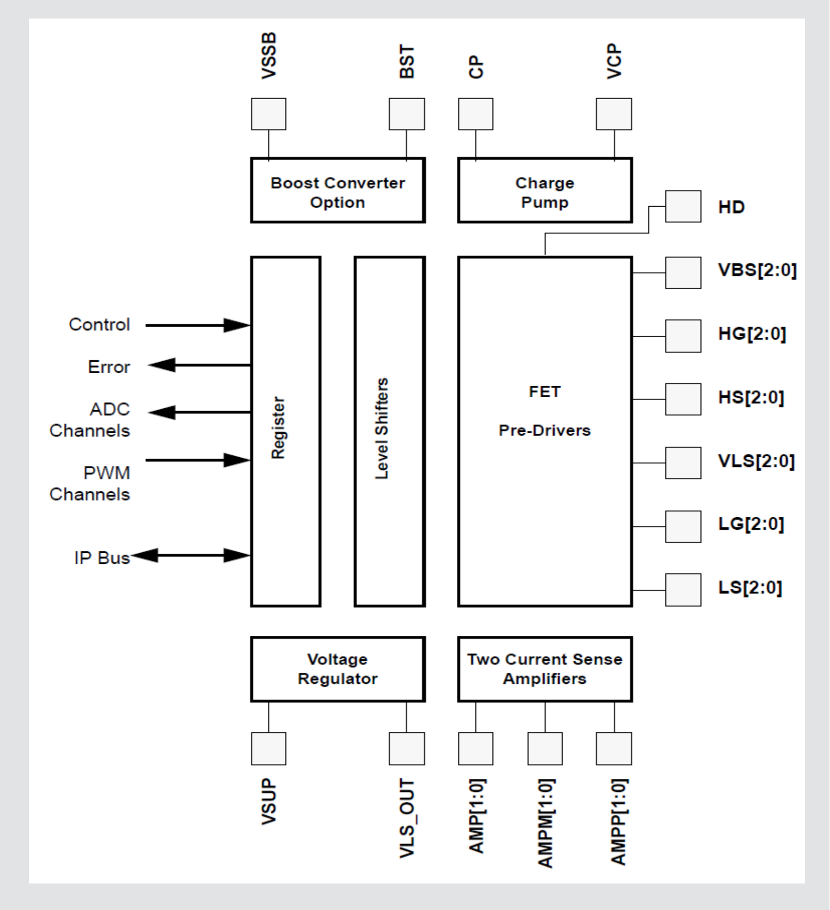
Gate Drive Unit (GDU) – Overview

FET pre-driver for 6 N-ch power MOSFETs (3 high-side, 3 low-side)

- 11V LDO to drive external FETs VGS
- Bootstrap circuit for high-side drivers
- Phase comparators to signal BEMF zero crossing
- Over- /under- voltage monitoring
- Short circuit protection by monitoring VDS for both LS and HS
- Step-up (boost) converter option for low supply voltage operation
- Option to route DC Link (HD) or Phase voltage measurement to ADC
- Two current sense amplifiers feeding ADC
- Optional charge pump to support static high-side driver operation



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Operating Voltage Ranges

Without Boost

Vsup	MCU	GDU
26V…40V	Full	Disabled
7V...26V	Full	Enabled Vgs> Vsup – 2*Vbe (5V min)
6V .. 7V	Full	Disabled
3.5V .. 6V	Full Iddx = 25mA max if no external PNP	Disabled
<3.5V	Reset	Disabled

With Boost

Vsup	MCU	GDU
26V... 40V	Full	Disabled
9.5V..26V	Full	Boost OFF for Vsup > 11V Vgs = 9.6V
6V…9.5V	Full	Boost ON Vgs >9V
3.5V .. 6V	Full Iddx = 25mA max if no external PNP	Boost ON Vgs >9V
<3.5V	Reset	Disabled

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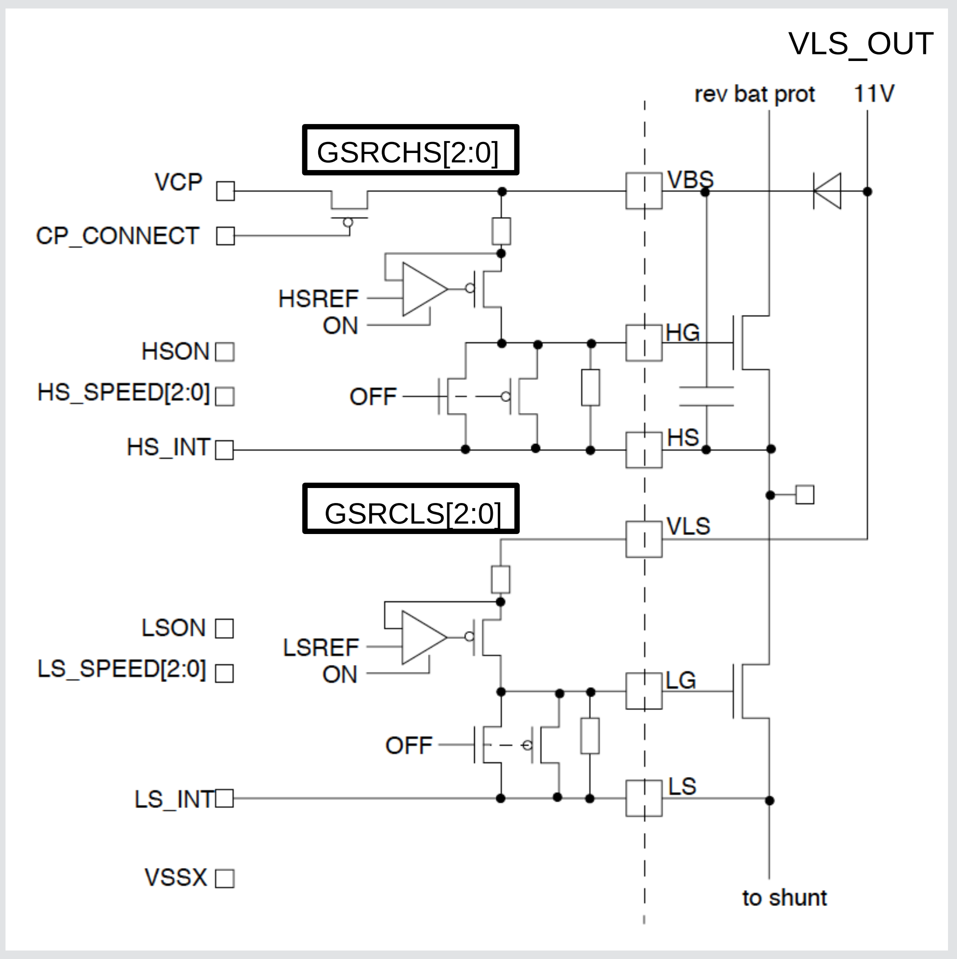
“Half-Bridge” Driver Topology

- Turn on slope is controlled by current shaping, 8 steps programmable.
- Drives power MOS transistors up to ~100nC total gate charge.
- Charge pump assisted Bootstrap circuit for high side drive.
- VLS_OUT directly supplies the LS drivers, while it charges the bootstrap cap for the HS drivers.
- VLS_OUT is monitored.

  If < 7V all drivers are turned off.



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HS& LS Protection – Vds Monitoring

- 6 Desaturation Comparators for HS and LS protection

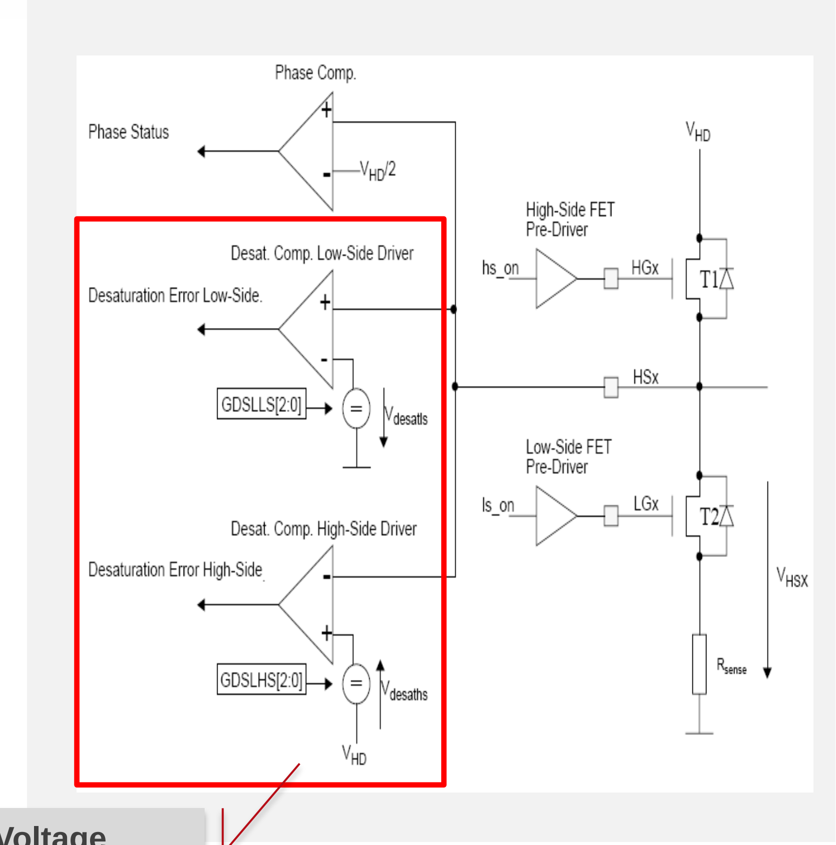
- After turning on (any) high side or low side transistor the HSx voltage is monitored

- In case of Desaturation error

  → LS/HS switched off

  → optional interrupt

- Programmable blanking time = delay between driver turn-on and the evaluation of the comparator (~60ns..5us @ 50MHz) .



Saturation Voltage programmable from 0.3V to 1.35V in 8 steps (150mV steps)

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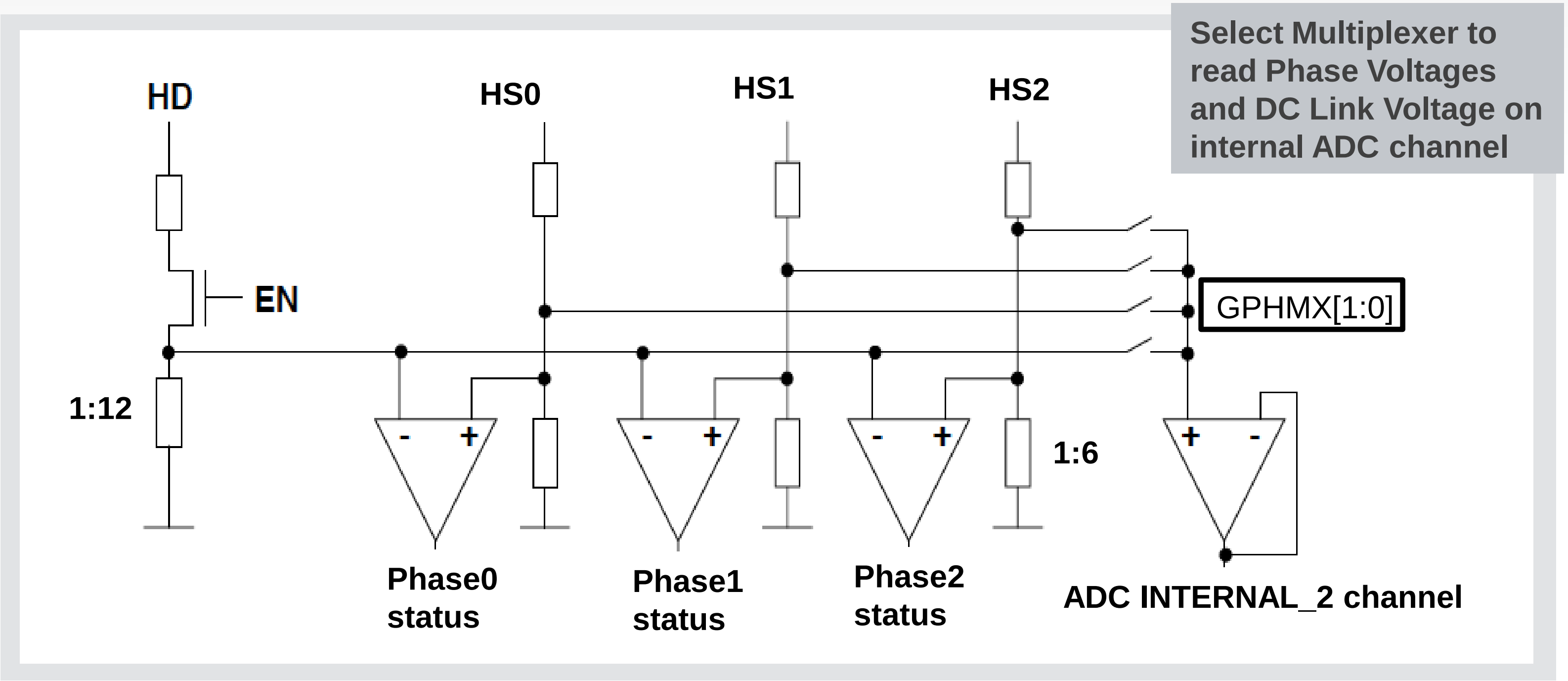
Phase Comparators



Select Multiplexer to read Phase Voltages and DC Link Voltage on internal ADC channel

- The phase comparators indicate if phase voltage V_{HSx} is greater than $0.5*V_{HD}$
- This can be used for BEMF detection in un-driven phases.
- A multiplexer selects if the supply voltage HD or any of the phase voltages is routed to an ADC internal channel.

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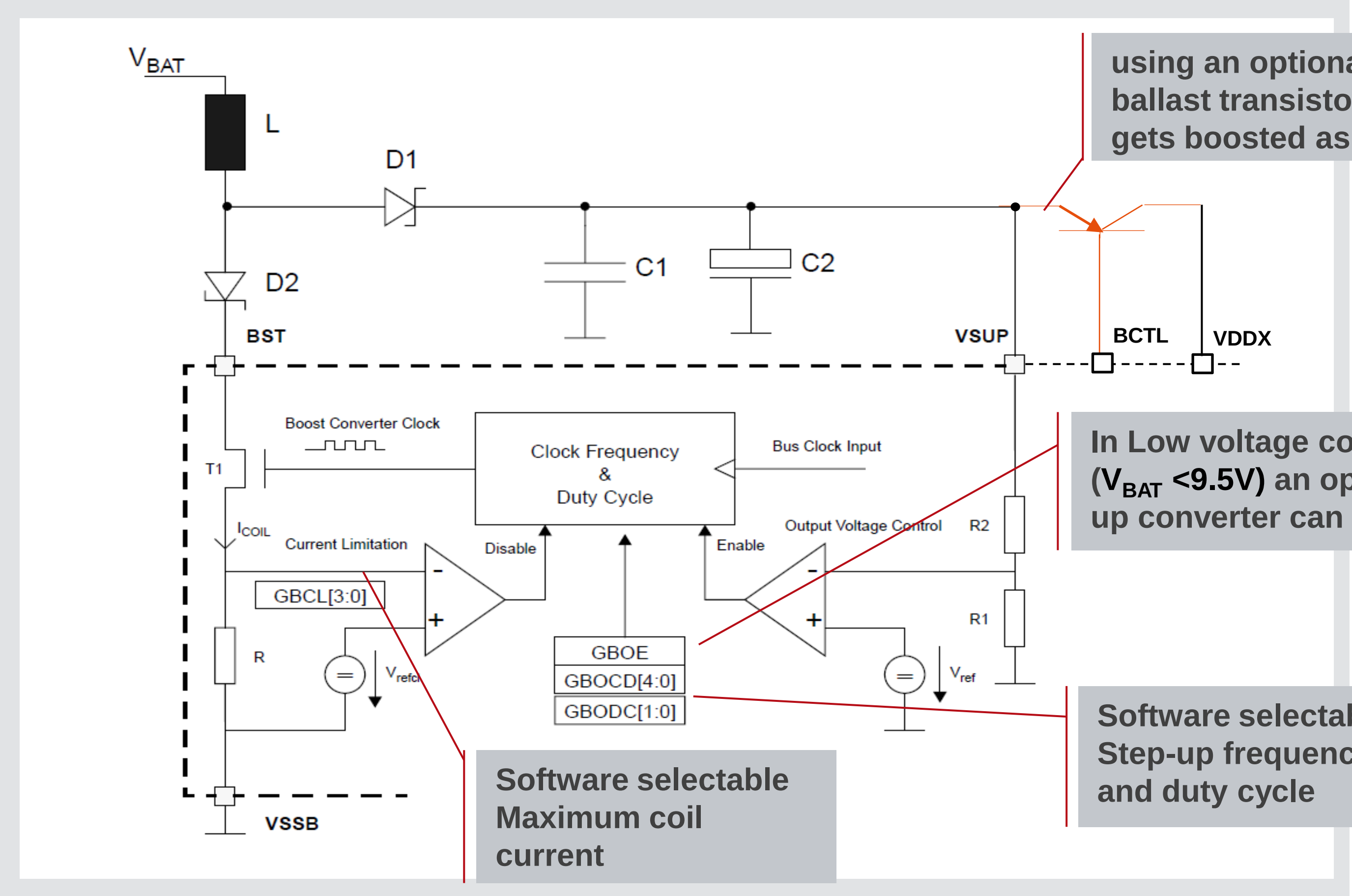
Boost (Step-Up) Converter

- This option can be used to guarantee a V_{GS} > 9V at low V_{BAT} conditions



using an optional external ballast transistor the core gets boosted as well or not.

In Low voltage condition (V_{BAT} <9.5V) an optional step up converter can be enabled

Software selectable Maximum coil current

Software selectable Step-up frequency and duty cycle

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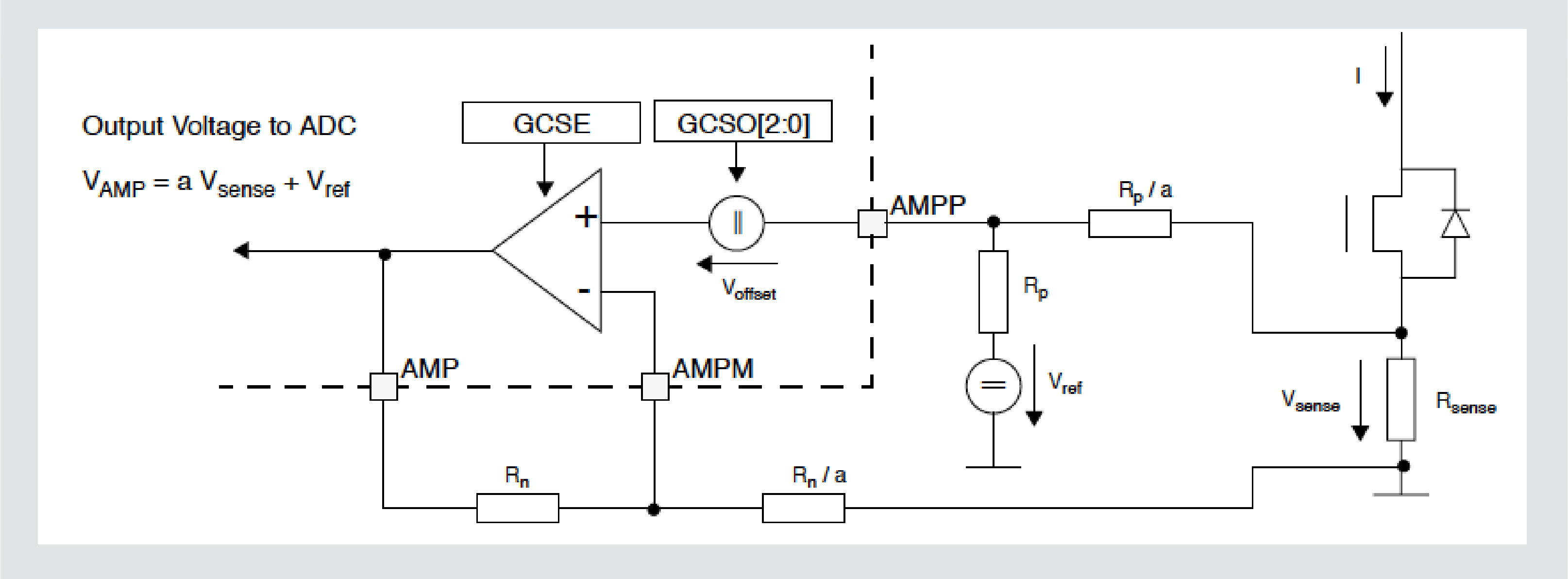
Current Sense Amplifier



- Two linear operational amplifiers are provided to amplify voltage across two separate current sense shunt resistors
- Each amplifier drives an ADC channel
- The amplifier closed-loop gain (Av) can be selected by choosing resistor values populated on the PCB
- The amplifier features offset compensation in 8 steps in order to avoid low signal “hiding” near to ground level.
- By applying an offset level (by resistor network), bidirectional current sense can be accomplished.

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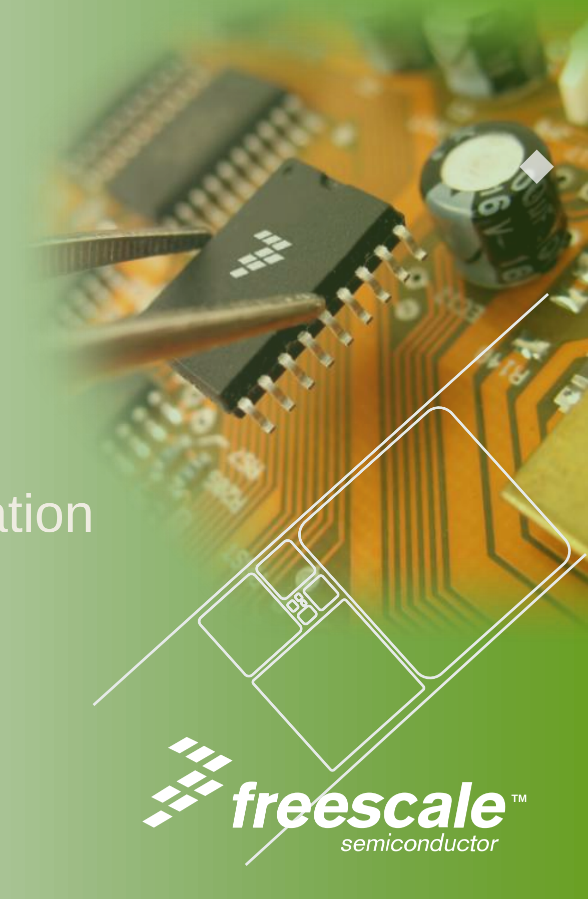
- Dynamic Current Limitation



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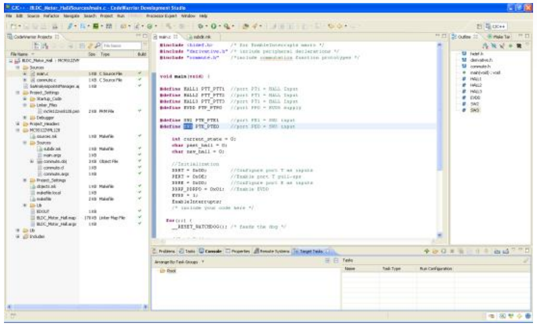
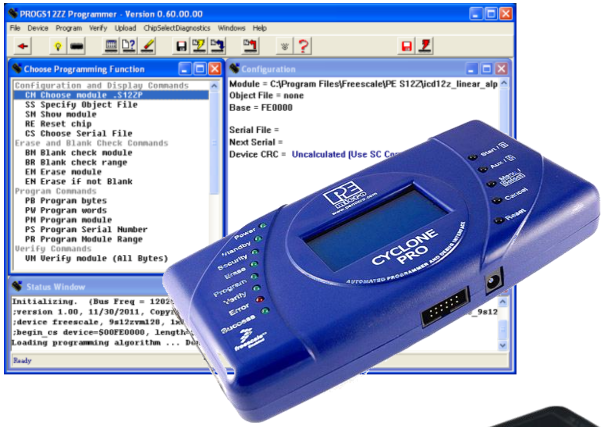
Available Development Tools

- **IDE**
  - Codewarrior 10.2 (eclipse based)
  - Cosmic Win IDEA
  - eclipse
- **Compilers**
  - Codewarrior S12Z
  - Cosmic
- **Programmers**
  - P&E PROGS12Z
  - Cyclone Pro Programmer
- **Debugger**
  - CW & P&E S12Z Debugger
  - Cosmic Zap Debugger
- **Freemaster Run time debugger**
- **Debug Interface**
  - P&E USB Multilink Debug Interface
  - 3rd Party Debug Interfaces (isystem, Lauterbach)
- **EVB board available now**





```
Configuration and Display Commands
  CM Choose module .S12ZP
  SS Specify Object File
  SM Show module
  RE Reset chip
  CS Choose Serial File
Erase and Blank Check Commands
  BM Blank check module
  BR Blank check range
  EM Erase module
  EN Erase if not Blank
Program Commands
  PB Program bytes
  PW Program words
  PM Program module
  PS Program Serial Number
  PR Program Module Range
Verify Commands
  VM Verify module (All Bytes)
```

```
Module = C:\Program Files\Freescale\PE S12Z\icd12z_linear_alp
Object File = none
Base = FE0000

Serial File =
Next Serial =
Device CRC = Uncalculated [Use SC Co
```

```
Initializing.  (Bus Freq = 1202
;version 1.00, 11/30/2011, Copy
;device freescale, 9s12zvm128, 1x
;begin_cs device=$00FE0000, length
Loading programming algorithm ... Do
_9s12
```

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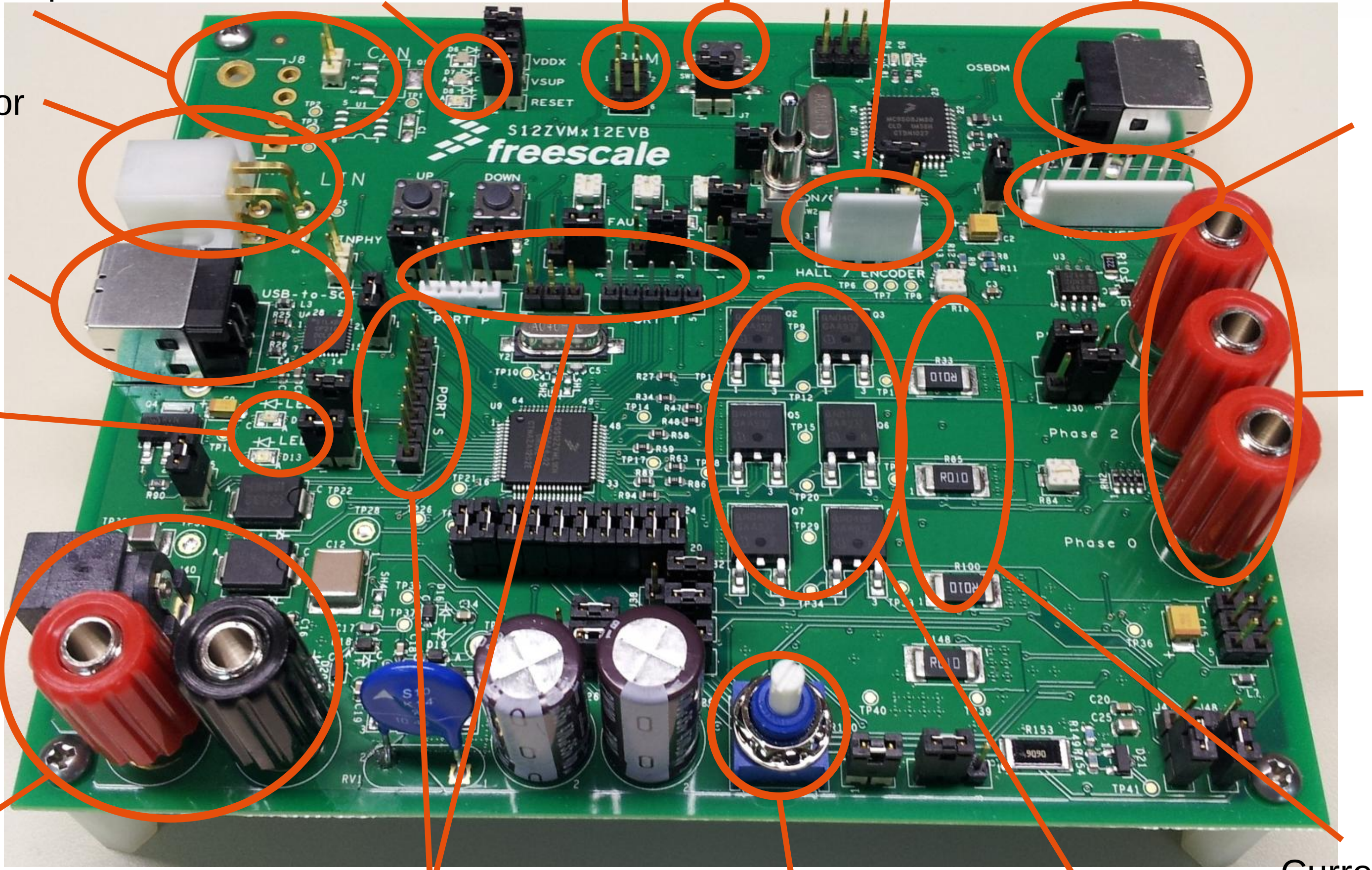
XS12ZVMx12EVB



CAN option

Power indicator LEDs

BDM interface

Reset

Hall/Encoder interface

OSBDM

LIN connector

Resolver interface

Freemaster USB-to-SCI interface

User LEDs

Motor connectors

VDDX external ballast

12V supply

I/O Port access (for example PWM / ECLK)

ATD inputs

GDU / 3phase bridge access

Current Sense Resistors

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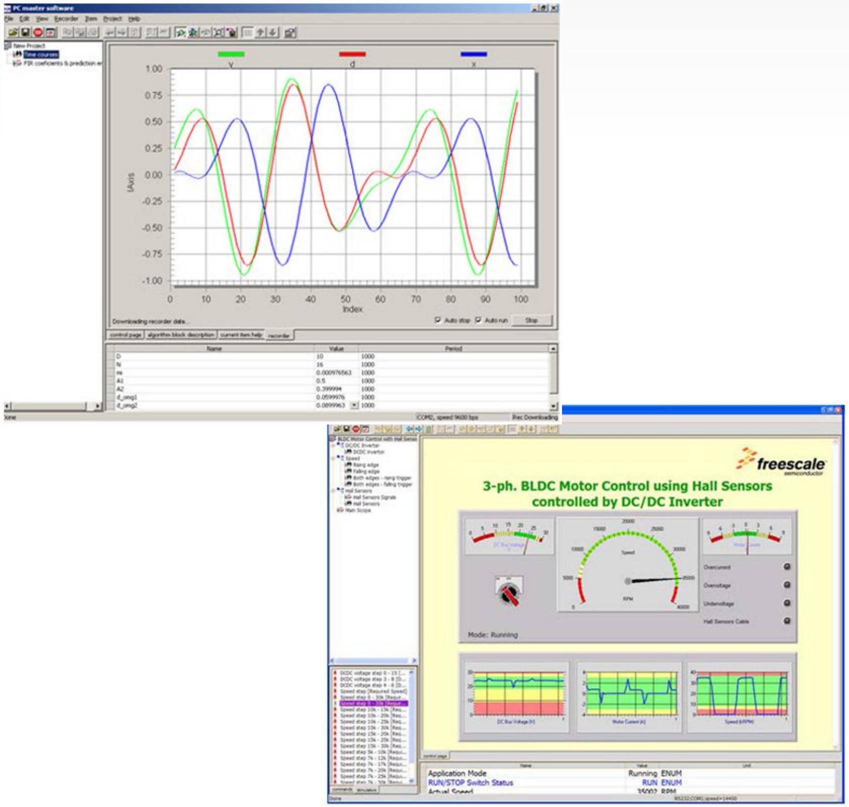
FreeMASTER – Run Time Debugging Tool

- A user-friendly **real-time** debug monitor and data visualization tool
- It supports completely **non-intrusive** monitoring of variables on a running system
- Display multiple variables changing over time on an **oscilloscope-like display**, or view the data in text form
- It communicates with an on-target driver **via USB, BDM, CAN, UART**, for transmitting data from the target to the host computer
- The user can **provide Active-X** based instrumentation gauges, dials, knobs, and sliders to create custom visual dashboards



USB
BDM
CAN
UART
JTAG
Ethernet

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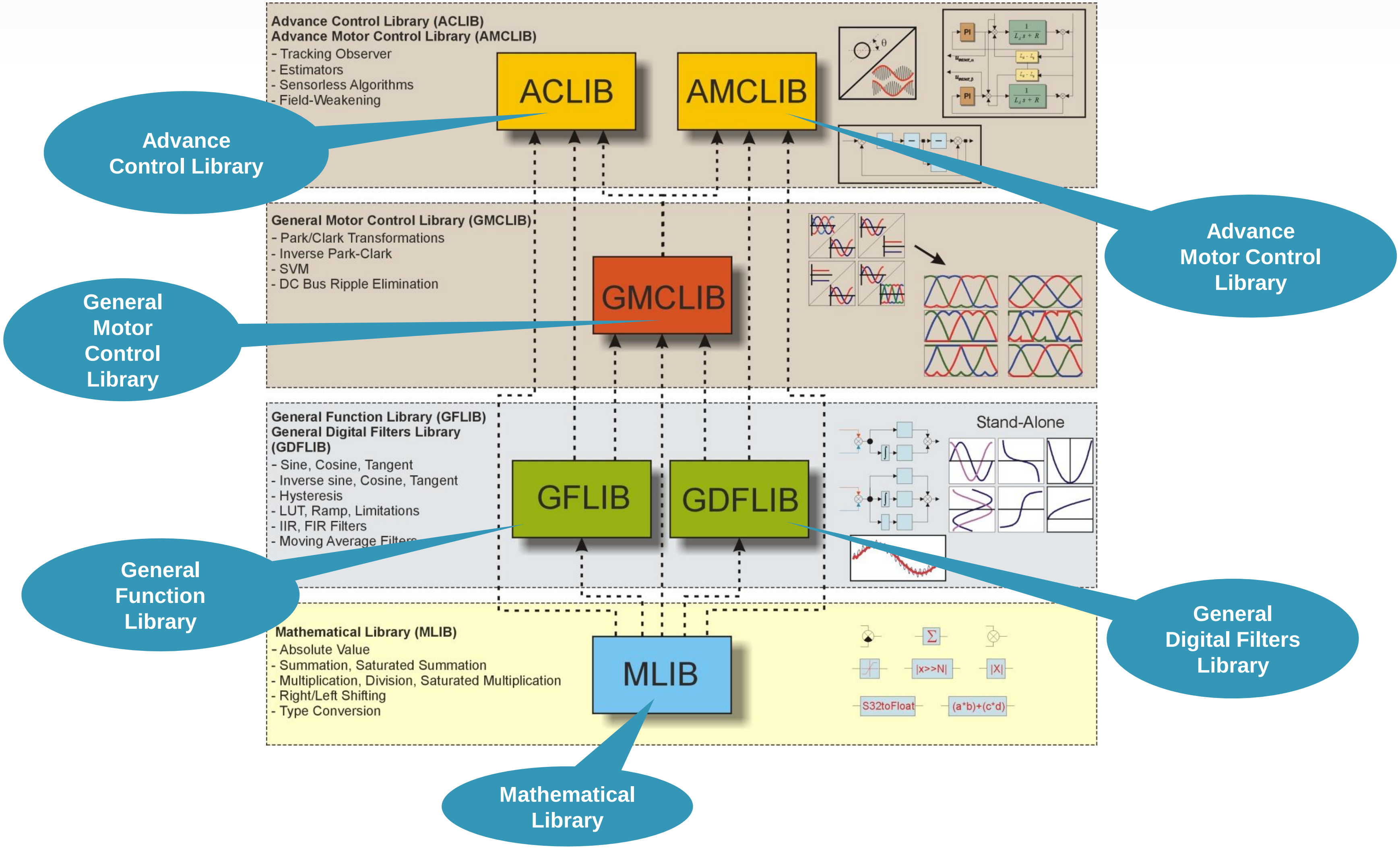
Automotive Math and Motor Control Library Set



Advance Control Library (ACLIB)
Advance Motor Control Library (AMCLIB)
- Tracking Observer
- Estimators
- Sensorless Algorithms
- Field-Weakening

ACLIB

AMCLIB

General Motor Control Library (GMCLIB)
- Park/Clark Transformations
- Inverse Park-Clark
- SVM
- DC Bus Ripple Elimination

GMCLIB

General Function Library (GFLIB)
General Digital Filters Library (GDFLIB)
- Sine, Cosine, Tangent
- Inverse sine, Cosine, Tangent
- Hysteresis
- LUT, Ramp, Limitations
- IIR, FIR Filters
- Moving Average Filters

GFLIB

GDFLIB

Stand-Alone

Mathematical Library (MLIB)
- Absolute Value
- Summation, Saturated Summation
- Multiplication, Division, Saturated Multiplication
- Right/Left Shifting
- Type Conversion

MLIB

Advance Control Library

Advance Motor Control Library

General Motor Control Library

General Function Library

General Digital Filters Library

Mathematical Library

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Auto Math and Motor Control Library Set – Contents

MLIB

- **Absolute Value, Negative Value**
  - MLIB_Abs, MLIB_AbsSat
  - MLIB_Neg, MLIB_NegSat
- **Add/Subtract Functions**
  - MLIB_Add, MLIB_AddSat
  - MLIB_Sub, MLIB_SubSat
- **Multiply/Divide/Add-multiply Functions**
  - MLIB_Mul, MLIB_MulSat
  - MLIB_Div, MLIB_DivSat
  - MLIB_Mac, MLIB_MacSat
  - MLIB_VMac
- **Shifting**
  - MLIB_ShL, MLIB_ShLSat
  - MLIB_ShR
  - MLIB_ShBi, MLIB_ShBiSat
- **Normalisation, Round Functions**
  - MLIB_Norm, MLIB_Round
- **Conversion Functions**
  - MLIB_ConvertPU, MLIB_Convert

GFLIB

- **Trigonometric Functions**
  - GFLIB_Sin, GFLIB_Cos, GFLIB_Tan
  - GFLIB_Asin, GFLIB_Acos, GFLIB_Atan, GFLIB_AtanYX
- **Limitation Functions**
  - GFLIB_Limit, GFLIB_VectorLimit
  - GFLIB_LowerLimit, GFLIB_UpperLimit
- **PI Controller Functions**
  - GFLIB_ControllerPIr, GFLIB_ControllerPIrAW
  - GFLIB_ControllerPIp, GFLIB_ControllerPIpAW
- **Interpolation**
  - GFLIB_Lut1D, GFLIB_Lut2D
- **Hysteresis Function**
  - GFLIB_Hyst
- **Signal Integration Function**
  - GFLIB_IntegratorTR
- **Sign Function**
  - GFLIB_Sign
- **Signal Ramp Function**
  - GFLIB_Ramp
- **Square Root Function**
  - GFLIB_Sqrt

GDFLIB

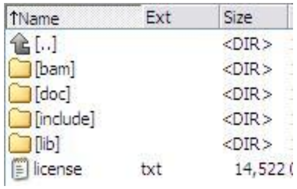
- **Finite Impulse Filter**
  - GDFLIB_FilterFIR
- **Moving Average Filter**
  - GDFLIB_FilterMA
- **1st Order Infinite Impulse Filter**
  - GDFLIB_FilterIIR1init
  - GDFLIB_FilterIIR1
- **2nd Order Infinite Impulse Filter**
  - GDFLIB_FilterIIR2init
  - GDFLIB_FilterIIR2

GMCLIB

- **Clark Transformation**
  - GMCLIB_Clark
  - GMCLIB_ClarkInv
- **Park Transformation**
  - GMCLIB_Park
  - GMCLIB_ParkInv
- **Duty Cycle Calculation**
  - GMCLIB_SvmStd
- **Elimination of DC Ripples**
  - GMCLIB_ElimDcBusRip
- **Decoupling of PMSM Motors**
  - GMCLIB_DecouplingPMSM

ACLIB/AMCLIB

- **Angle Tracking Observer**
- **Tracking Observer**
- **PMSM BEMF Observer in Alpha/Beta**
- **PMSM BEMF Observer in D/Q**
- **Content To Be Defined**



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Delivery Content

→ Matlab/Simulink Bit Accurate Models
→ User Manuals
→ Header files
→ Compiled Library File
→ License File (to be accepted at install time)

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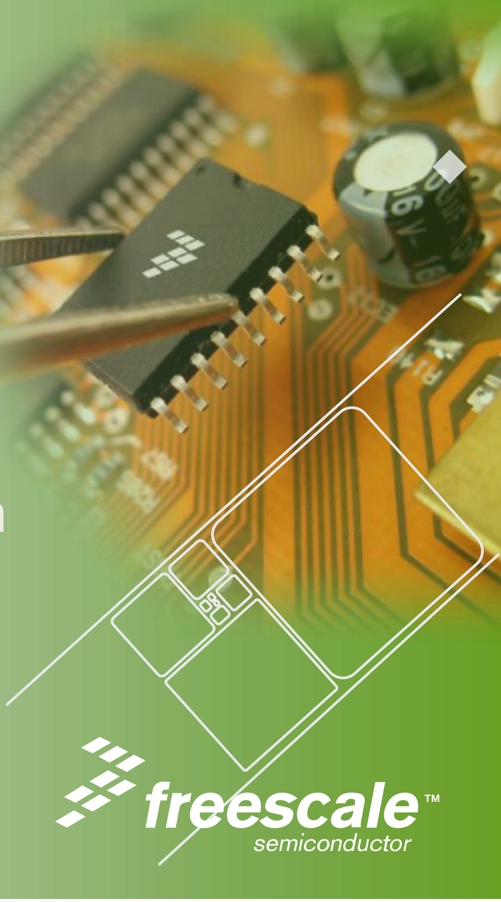
Agenda

- MagniV Roadmap
- S12VM
  - Overview
  - CPU12Z
  - Motor Control
    - Digital
    - Analog
- Development Tools
- BLDC Sensorless Motor Control Implementation
- Position Sensing with Zero Cross Detection
- Speed Control
- Dynamic Current Limitation



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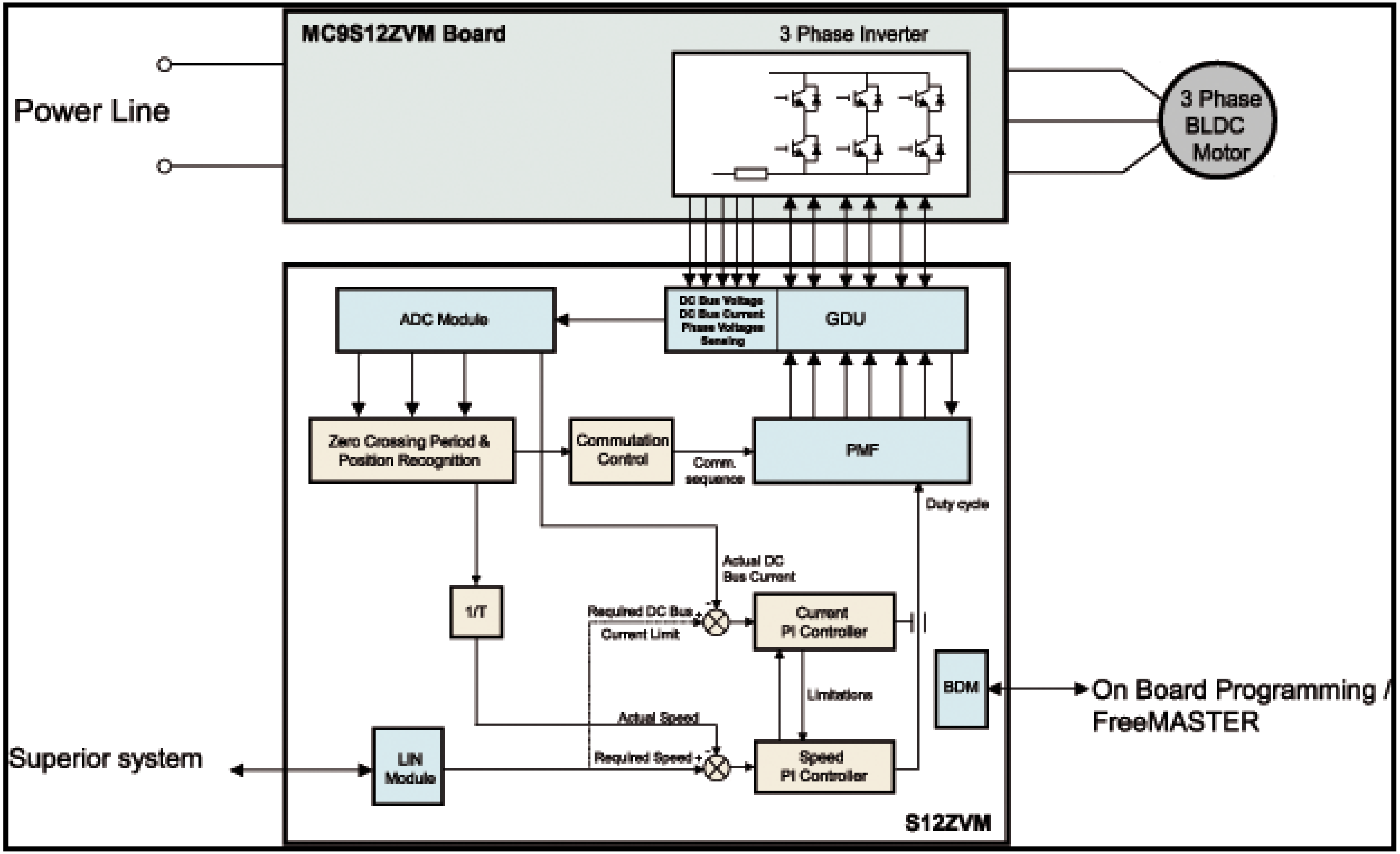
Example Control Block diagram



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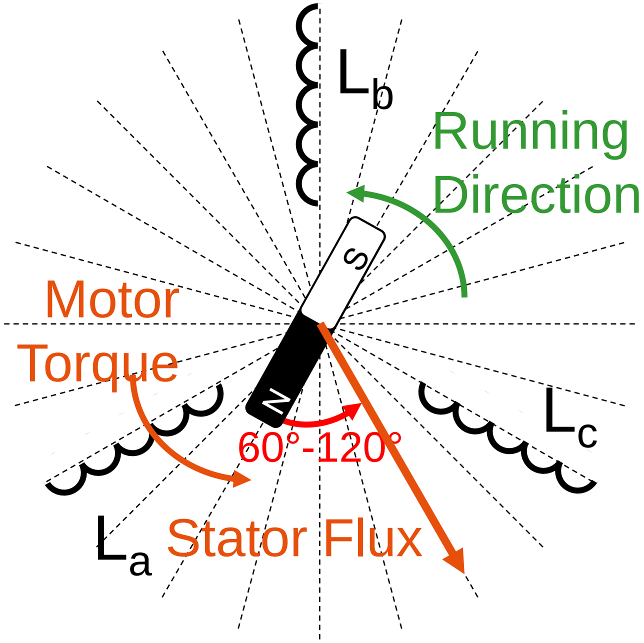
BLDC 6-Step Commutation Principle



- Stator Field is generated between 60° to 120° to rotor field to get maximal torque and energy efficiency
- Six Flux Vectors defined to create rotation

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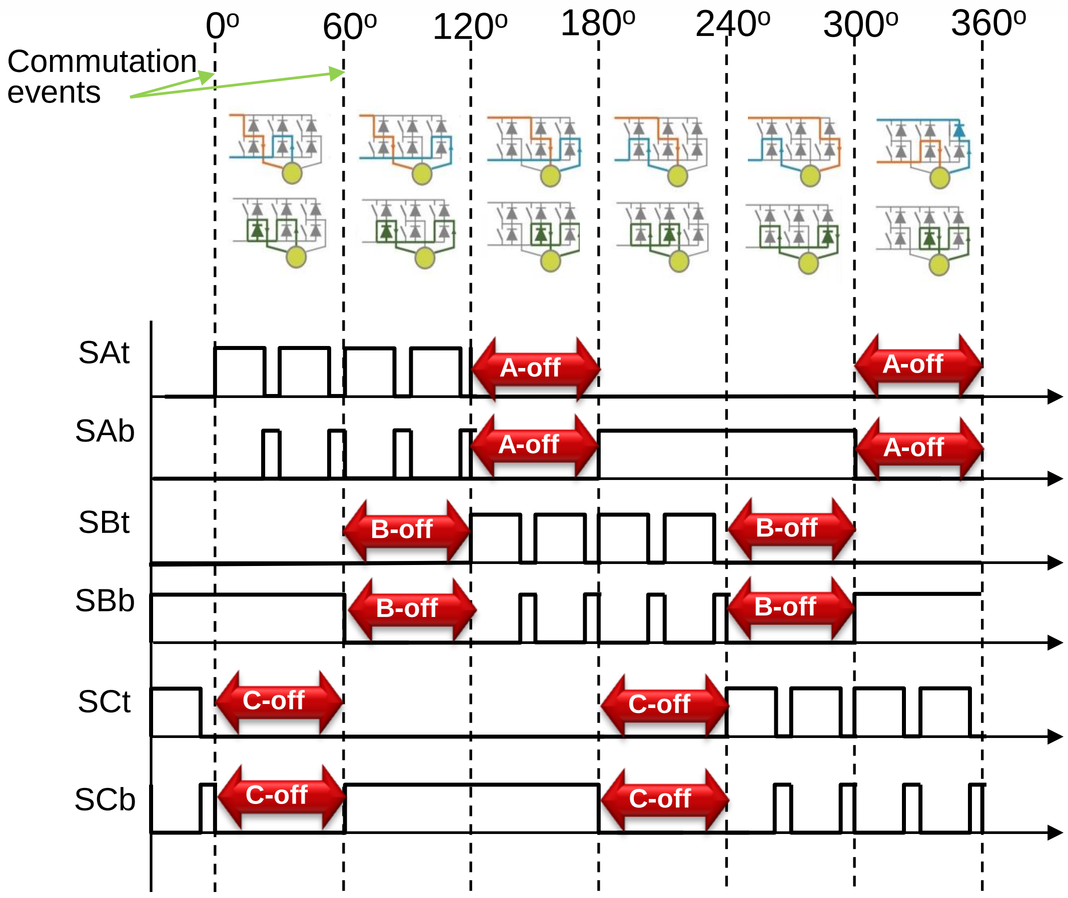
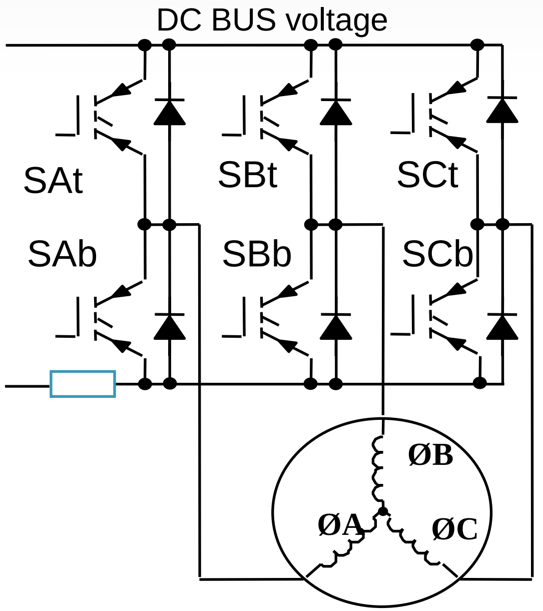
Complementary/Independent Unipolar PWM Switching





One phase powered by complementary PWM signal,
second phase grounded:

- Low MOSFET switching losses
- Low EMC noise

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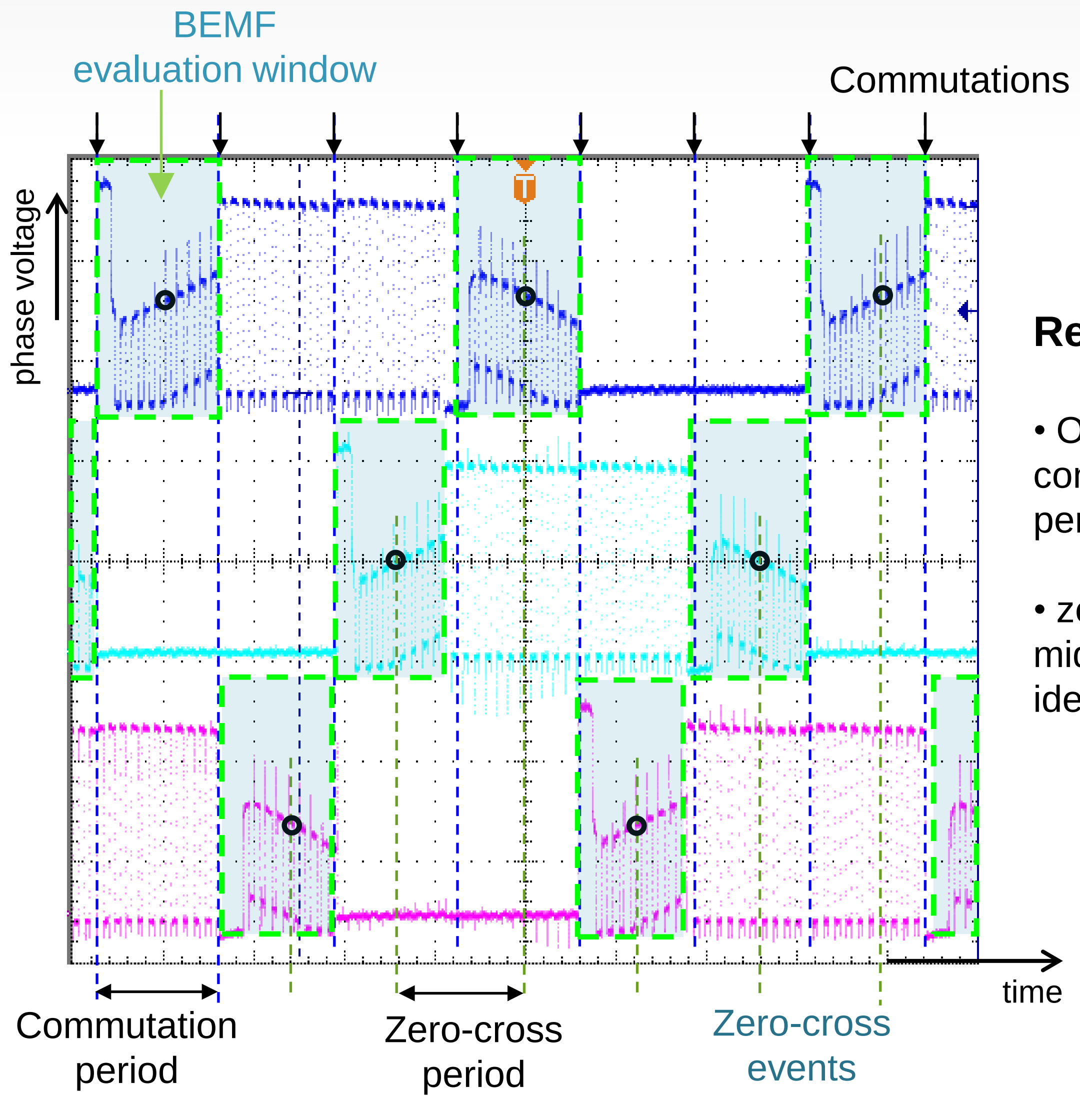
Back-EMF Zero-Cross Events and Commutations



Relationships:

- On constant rotor speed: commutation period = zero-cross period
- zero-cross event occurs in the middle of two commutations (on ideal motor)

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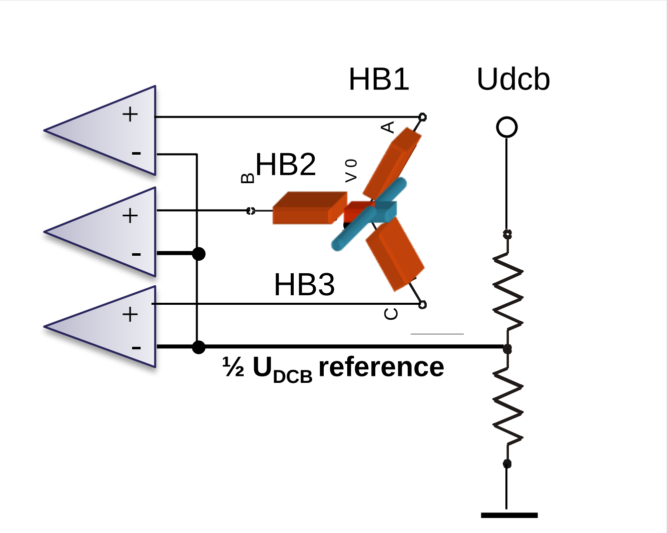
Zero Crossing topologies

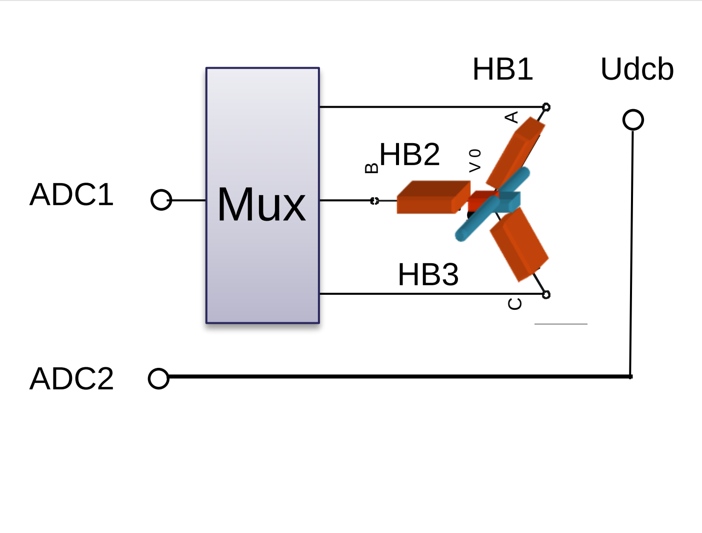
Both supported by S12ZVM

Using Phase comparators



- Implemented on S12ZVM
- little less CPU load

Using SW ATD sensing



- More flexible
- more accurate zero cross approximation

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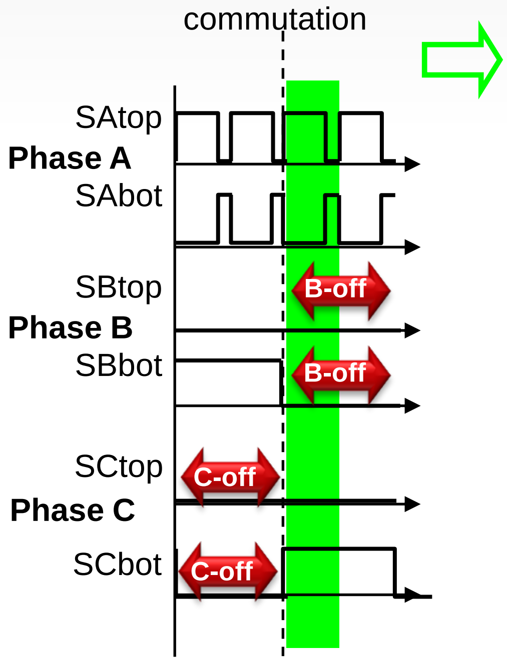
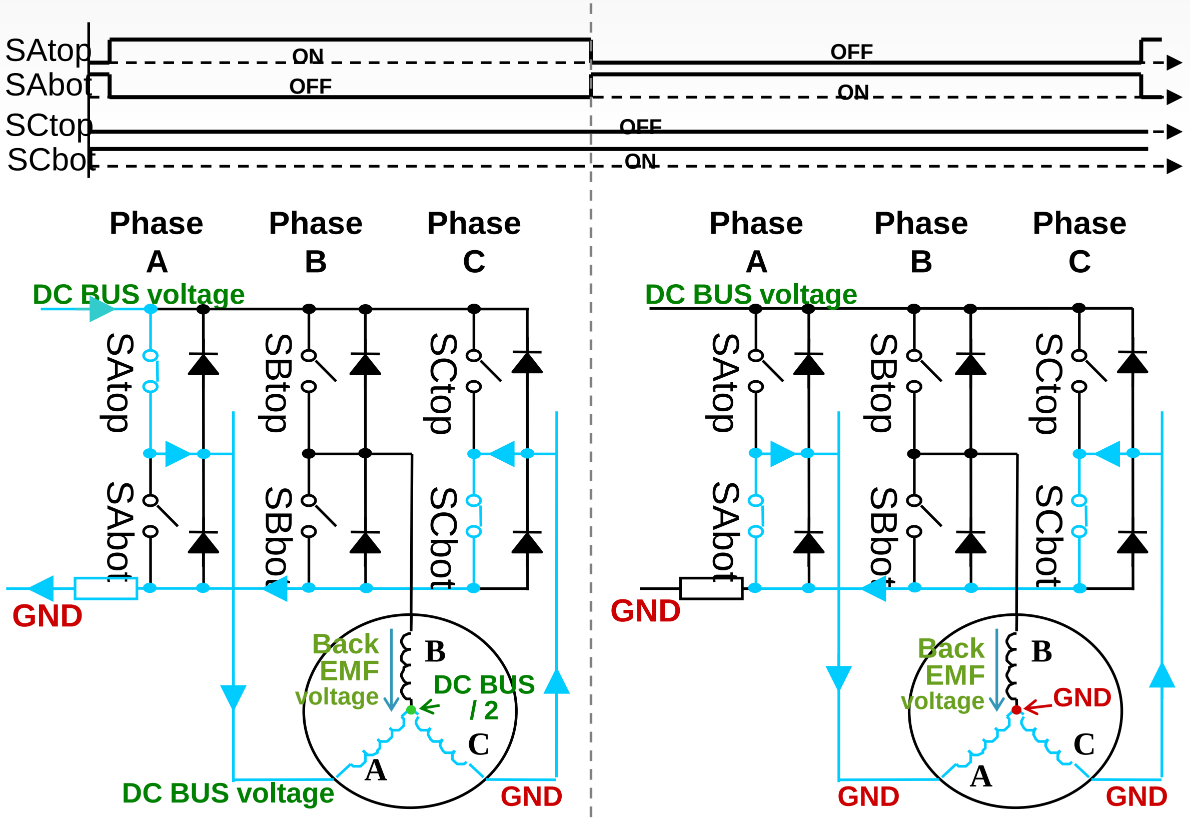
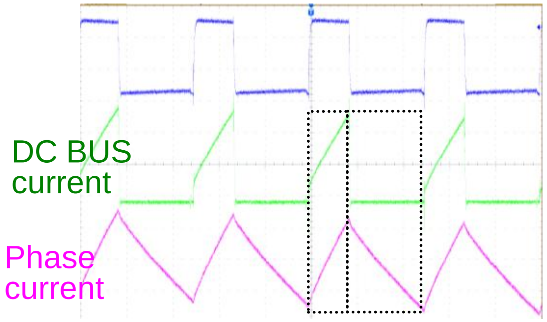
Measurement during PWM Switching







Top MOSFET is ON:

+ Phase current can be measured by DC BUS shunt resistor

+ Back-EMF voltage can be measured both positive and negative

Top MOSFET is OFF:

– Phase current can **NOT** be measured by DC BUS shunt resistor

– **Only positive** Back-EMF voltage can be measured (**zero-cross can not be precisely measured**)

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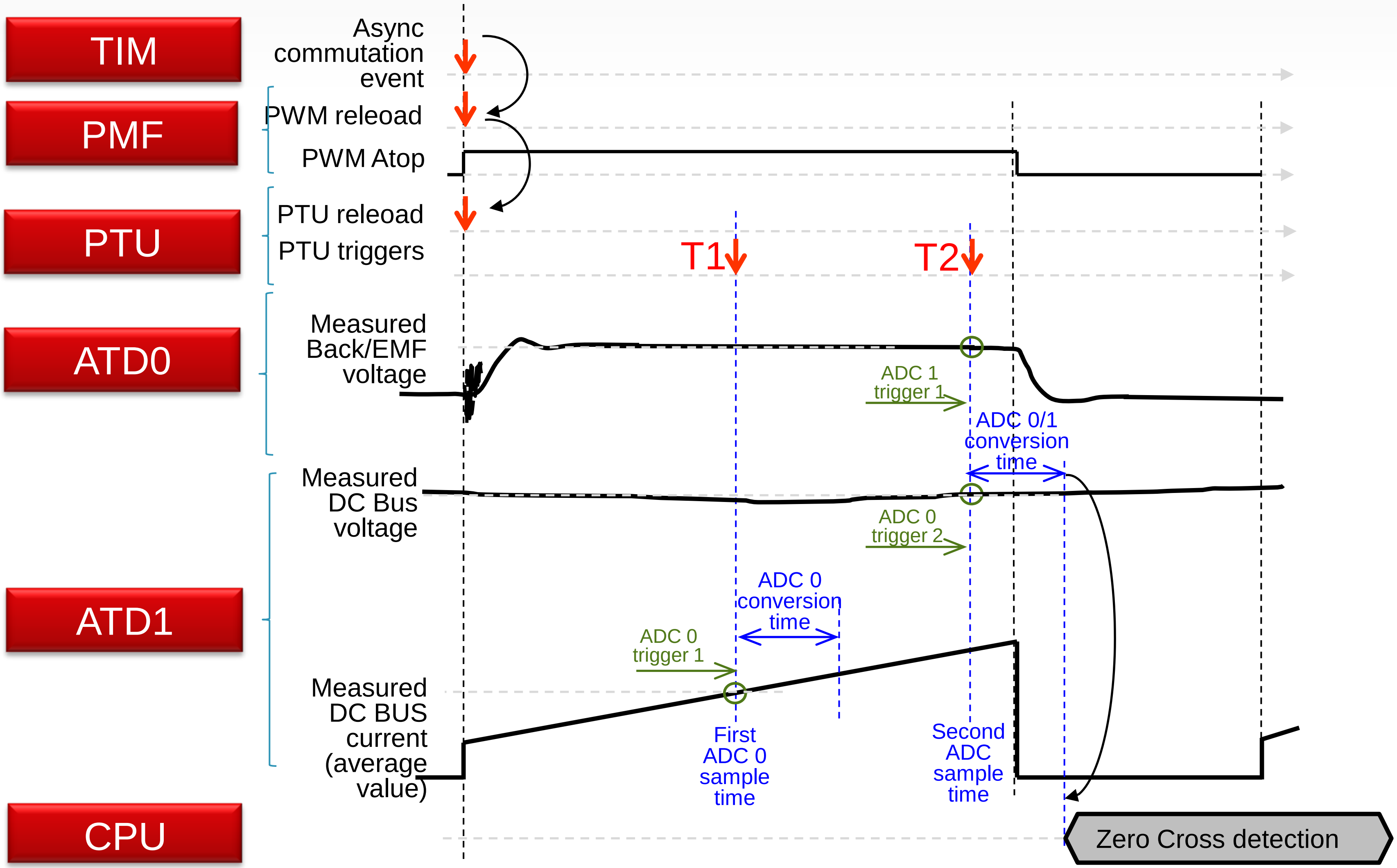
Module involvement in BLDC SW control loop



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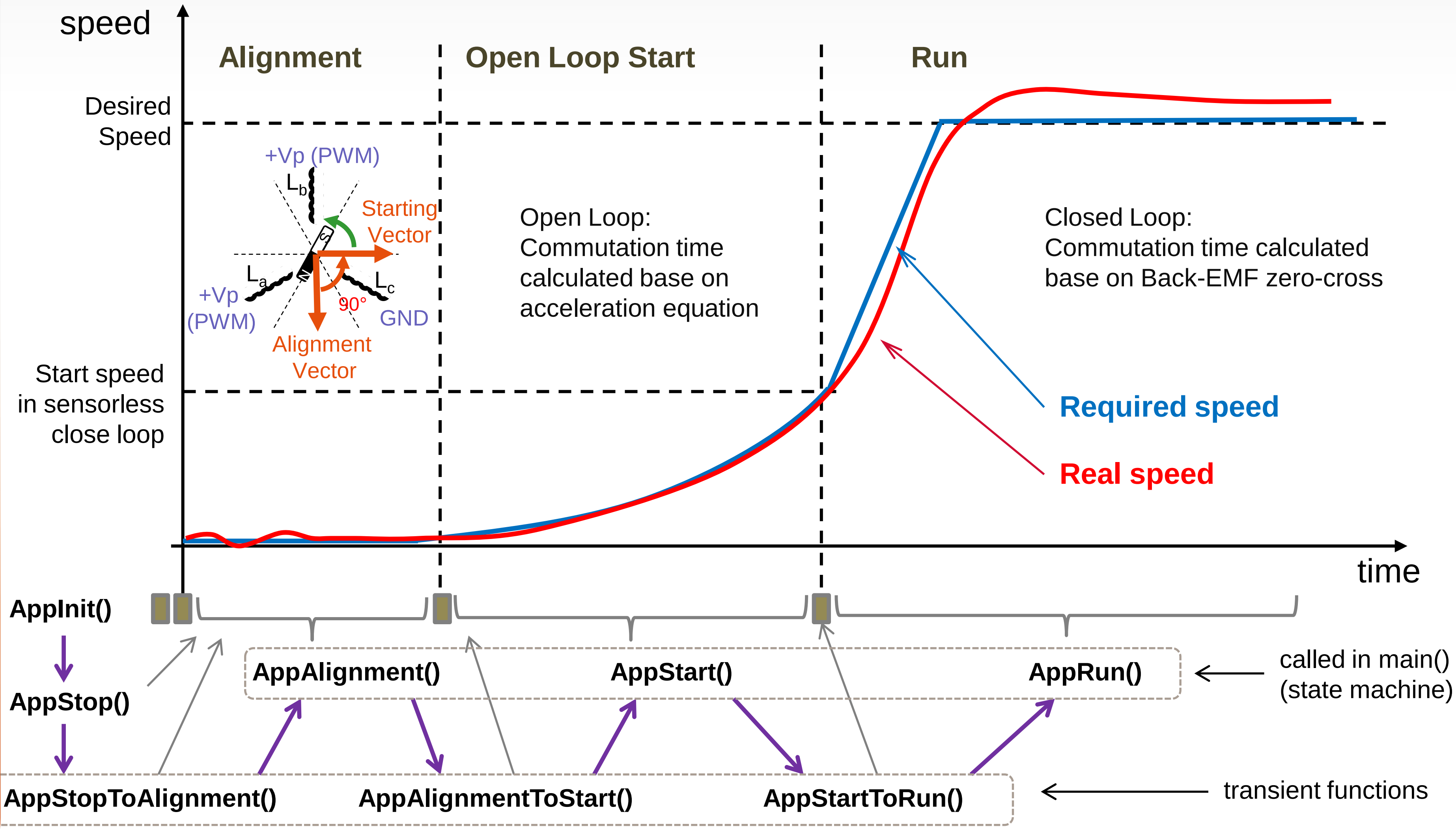
Application State Flow



Open Loop:
Commutation time calculated base on acceleration equation

Closed Loop:
Commutation time calculated base on Back-EMF zero-cross

AppInit()

AppStop()

AppAlignment() AppStart() AppRun() ← called in main() (state machine)

AppStopToAlignment() AppAlignmentToStart() AppStartToRun() ← transient functions

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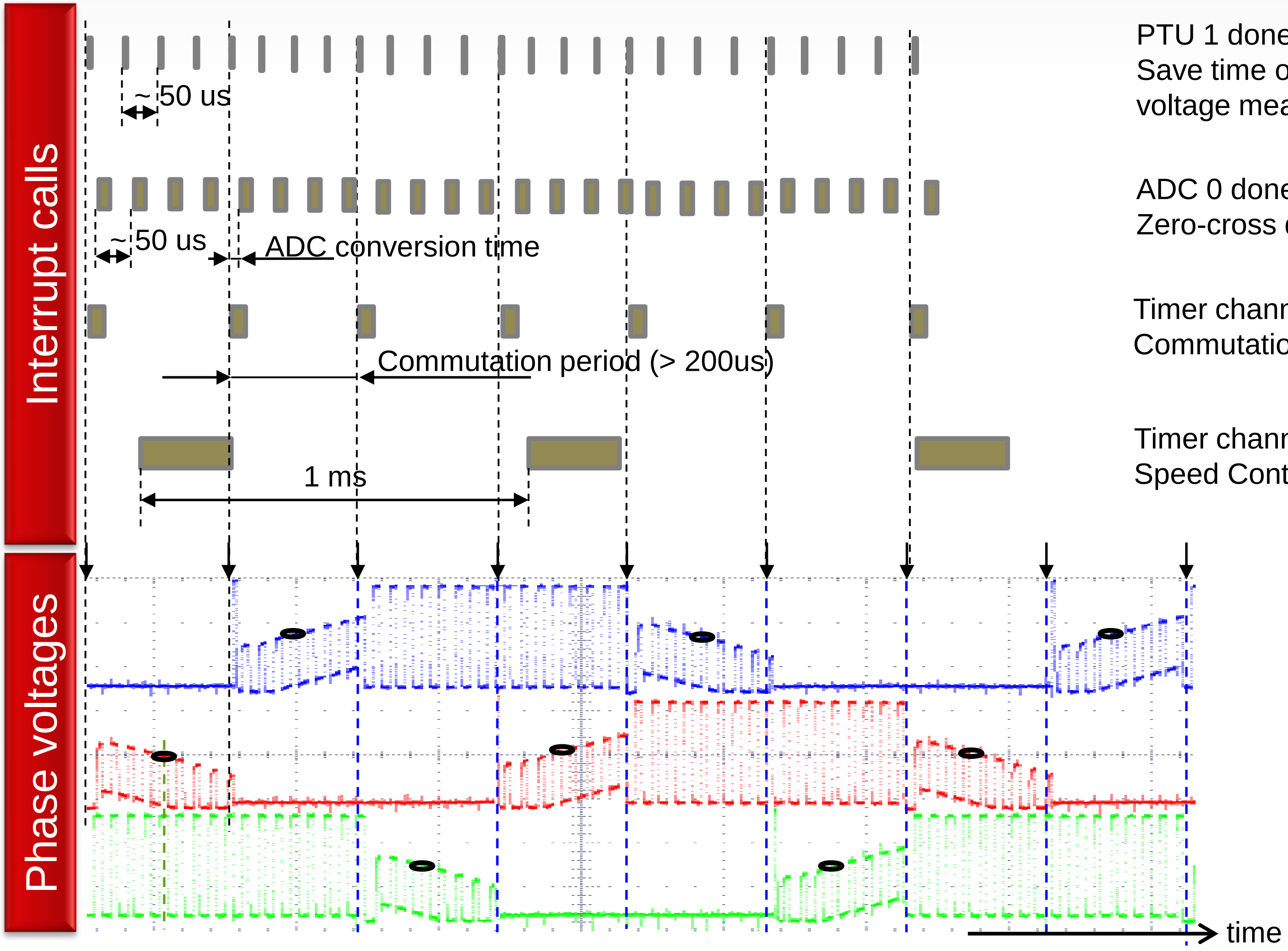
Control loop timing and interrupts



PTU 1 done ISR
Save time of Back-EMF voltage measurement

ADC 0 done ISR
Zero-cross detection

Timer channel 0
Commutation event

Timer channel 3
Speed Control Loop

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Agenda

MagniV Roadmap

S12VM

- Overview
- CPU12Z
- Motor Control
  - Digital
  - Analog

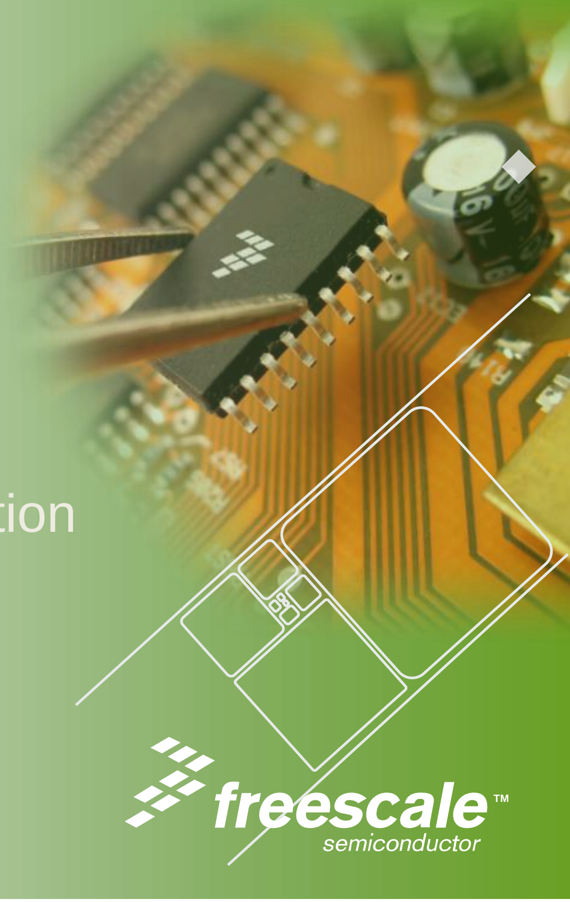
Development Tools

BLDC Sensorless Motor Control Implementation

Position Sensing with Zero Cross Detection

Speed Control

Dynamic Current Limitation



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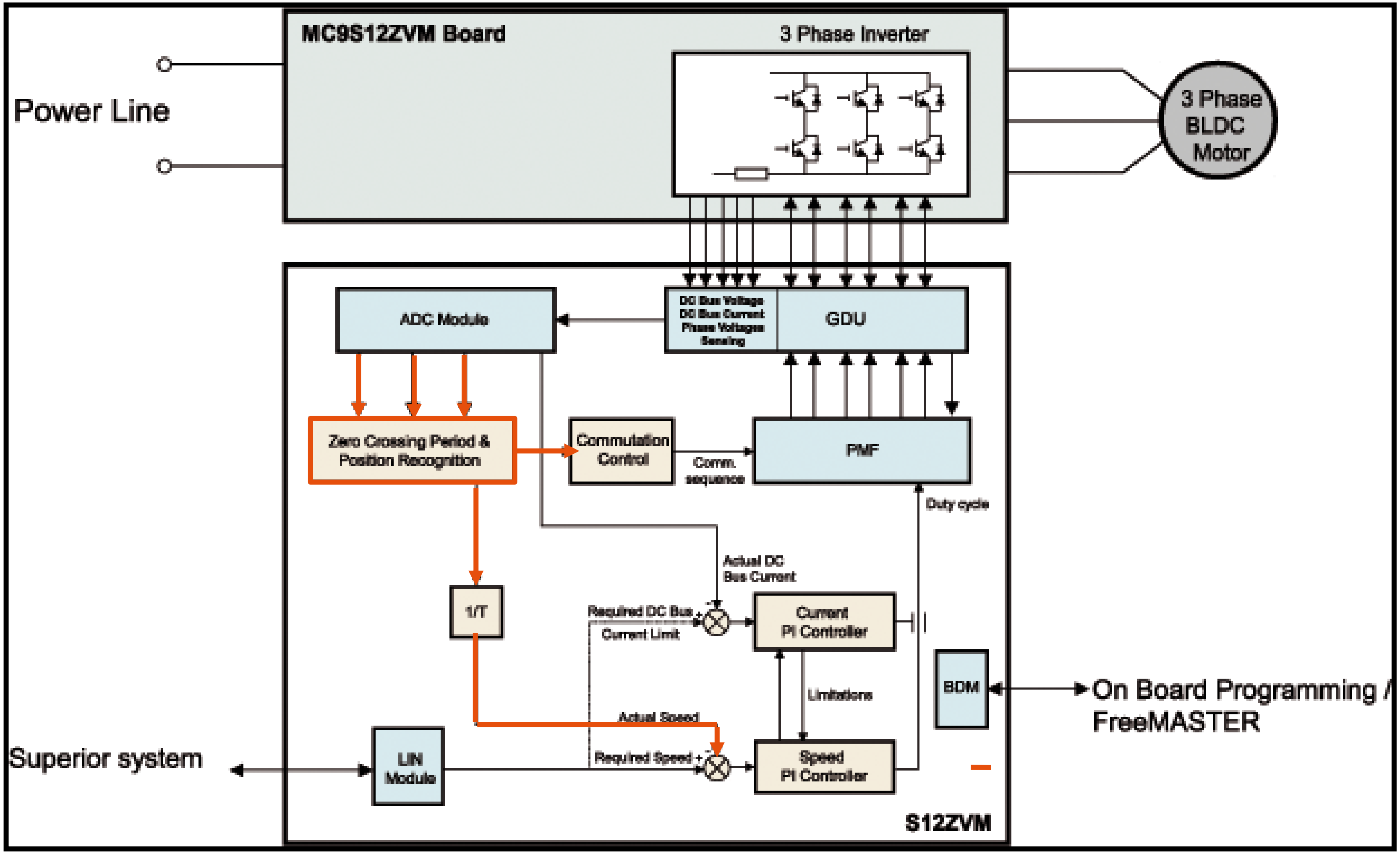
Example Control Block diagram



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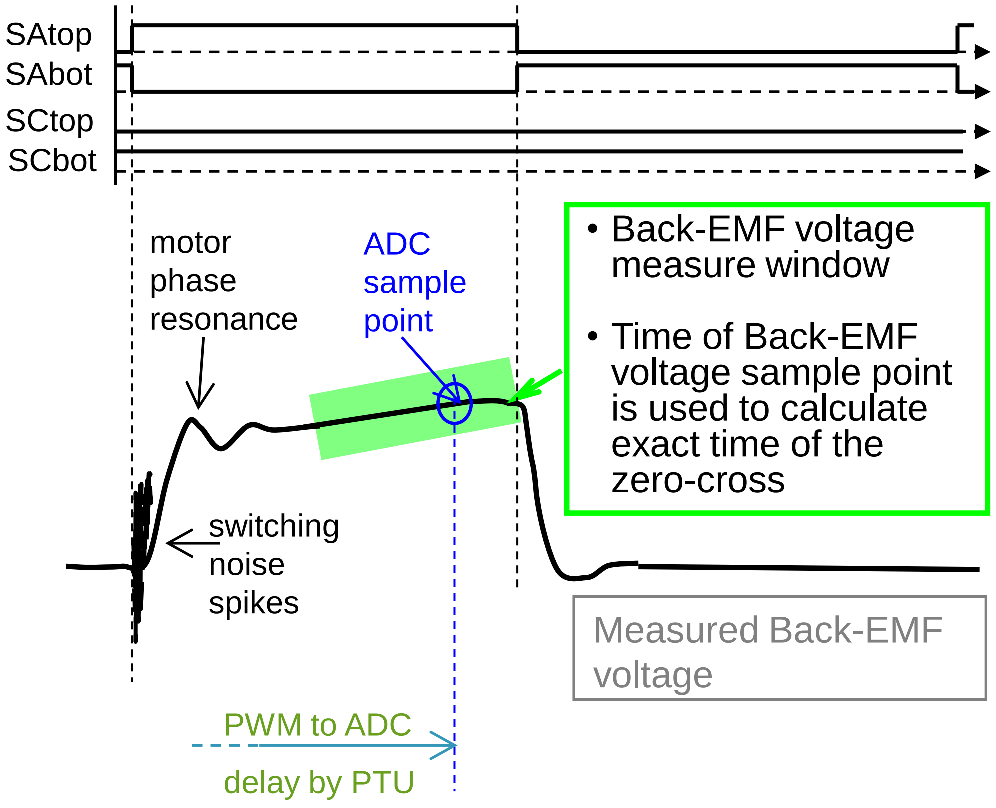
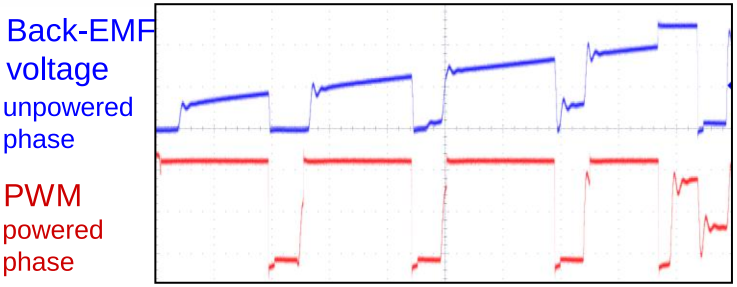
Back-EMF Voltage Measurement

Back-EMF voltage can not be measured within all the active PWM pulse as there is switching noise and resonance transient at the beginning of the PWM pulse

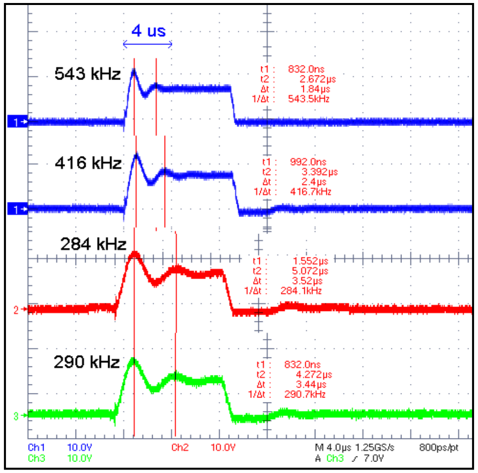


- Back-EMF voltage measure window
- Time of Back-EMF voltage sample point is used to calculate exact time of the zero-cross

Measured Back-EMF voltage



Resonance transient on Back-EMF voltage depends on motor and power stage parameters



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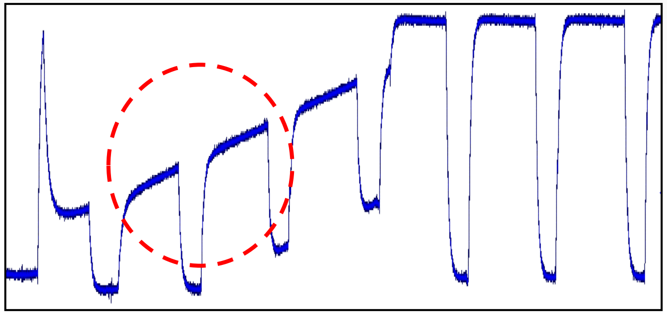
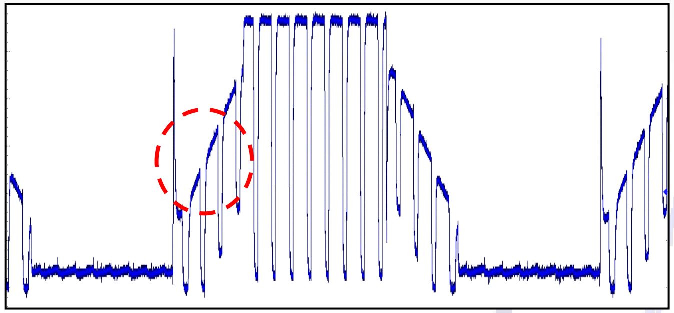
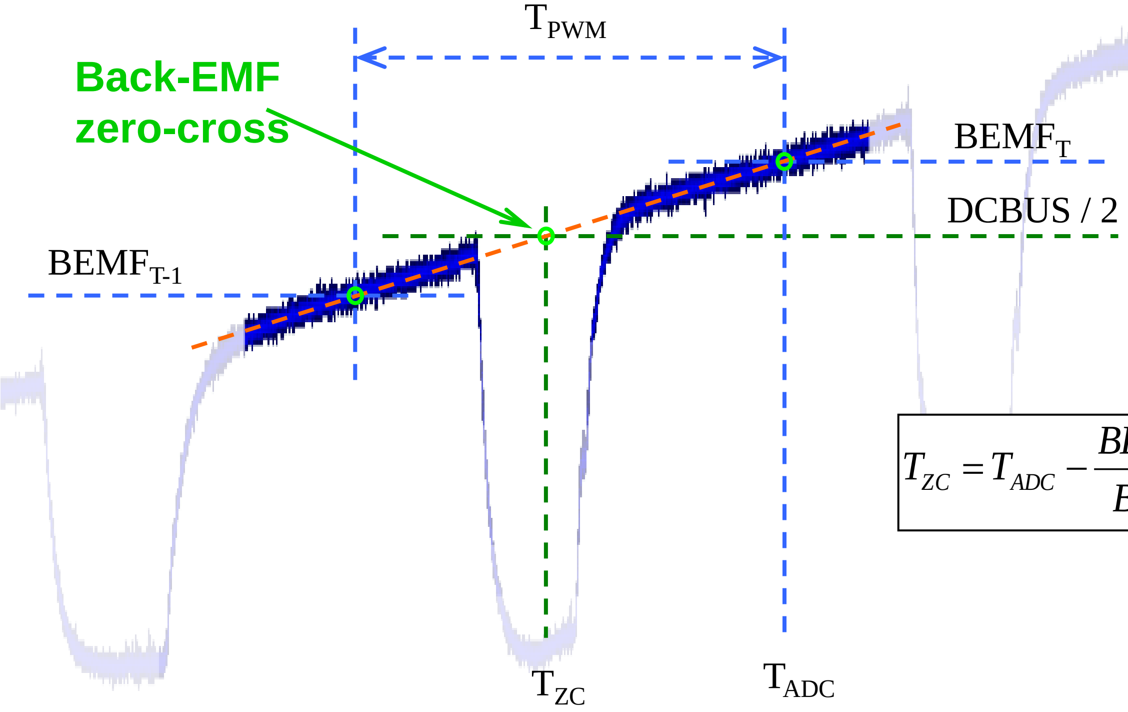
Zero Cross Approximation







$$T_{ZC} = T_{ADC} - \frac{BEMF_T - DCBUS/2}{BEMF_T - BEMF_{T-1}} \cdot T_{PWM}$$

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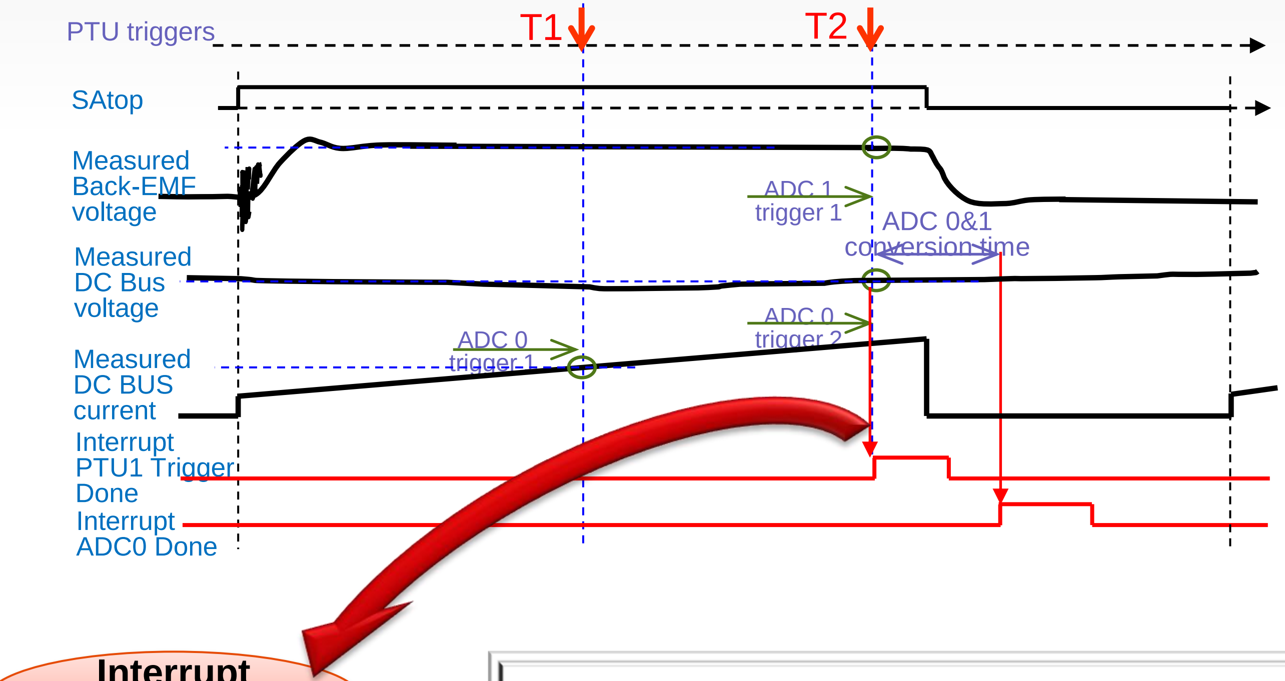
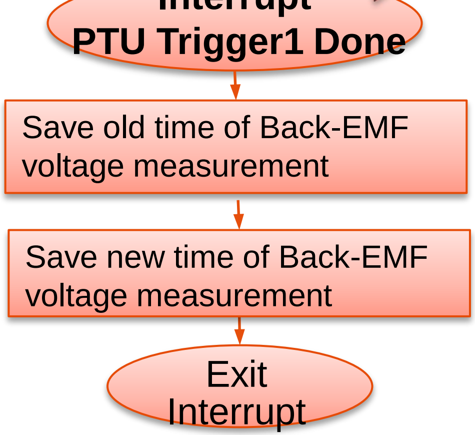
Zero-Cross detection preparation – 1/3




Interrupt PTU Trigger1 Done

Save old time of Back-EMF voltage measurement

Save new time of Back-EMF voltage measurement

Exit Interrupt

```
@interrupt void PTUTrigger1Done_ISR(void)
{
  timeOldBEMF = timeBEMF;
  timeBEMF = TIM_DEF.TCNT.R;

  PTU_DEF.PTUIFL.R = (1 << 4);
}
```

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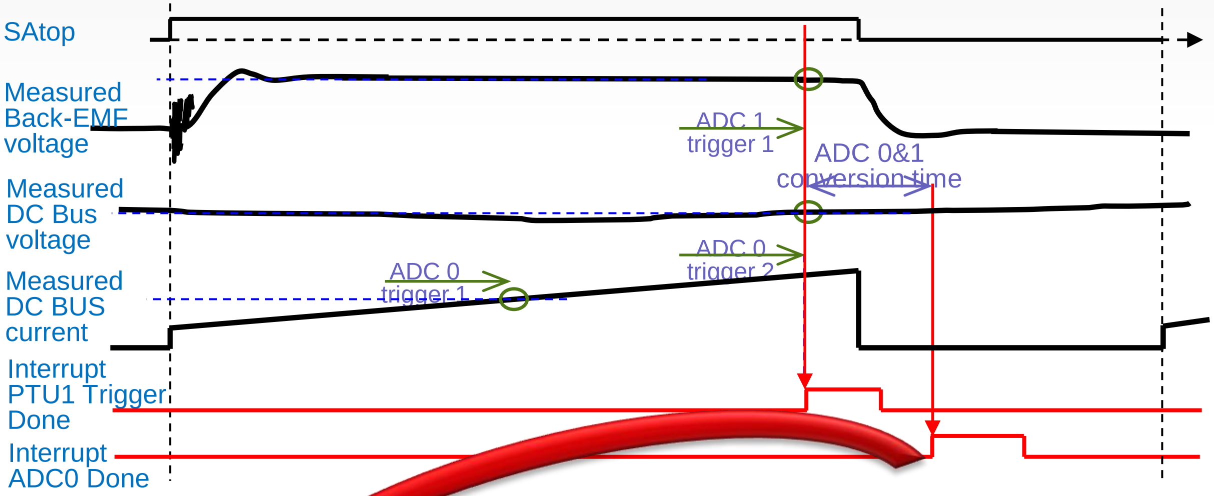
Zero-Cross detection preparation – 2/3



Interrupt ADC0 Done

Save ADC results of
DC Bus Current / Voltage
Phase voltage measurements

Scale phase and DC Bus voltages according to their resistor divider ratio

Calculate Back-EMF voltage

Check T_{OFF} period

```
@interrupt void ADC0done_ISR(void)
{
  DCBusCurrent      = (ADC0ResultList[0]>>1) - DCBusCurrentOffset;
  // DC Bus Voltage * 5/6/2
  DCBusVoltageHalf = MLIB_Mul(ADC0ResultList[1]>>1, 13653 ,F16);
  // Phase Voltage
  phaseVoltage       = ADC1ResultList[0]>>1;

  bemfVoltage = phaseVoltage - DCBusVoltageHalf;

  if (driveStatus.bit.AfterCMT == 1) {
    if ((timeBEMF - timeCommutation) > timeZCToff) {
      driveStatus.bit.AfterCMT = 0;
    }
  }
…
```

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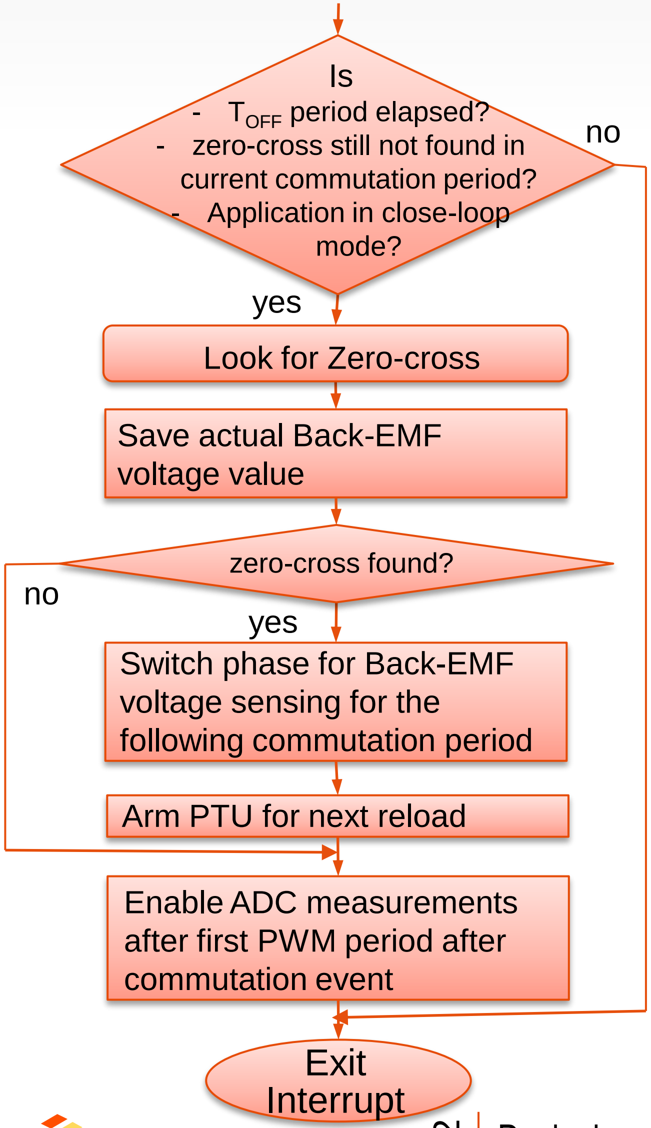
Zero-Cross detection preparation – 3/3



Is
- T_{OFF} period elapsed?
- zero-cross still not found in current commutation period?
- Application in close-loop mode?

no

yes

Look for Zero-cross

Save actual Back-EMF voltage value

zero-cross found?

no

yes

Switch phase for Back-EMF voltage sensing for the following commutation period

Arm PTU for next reload

Enable ADC measurements after first PWM period after commutation event

Exit Interrupt

```
…
  if ((driveStatus.bit.AfterCMT == 0) &&
      (driveStatus.bit.NewZC == 0) &&
      (driveStatus.bit.Sensorless == 1)) {



     ZCdetectionAdc[ActualCmtSector]();
     // save previous Back-EMF voltage (for ADC samples approximation)
     bemfVoltageOld = bemfVoltage;
     driveStatus.bit.AdcSaved = 1;

     if (driveStatus.bit.NewZC) {
        // will be applied at the next PMF Reload
        GDU_DEF.GDUPHMUX.B.GPHMX = BemfPhase[NextCmtSector];
        PTU_DEF.PTUC.B.PTULDOK = 1;
        DCBusCurrentZC = DCBusCurrent;
     }
  }

  if (driveStatus.bit.DisableAdc == 1) {
     driveStatus.bit.DisableAdc = 0;
     driveStatus.bit.NewZC = 0;
  }

  ADC0_DEF.ADCCONIF.R = 1;      // Clear Interrupt flag
}
```

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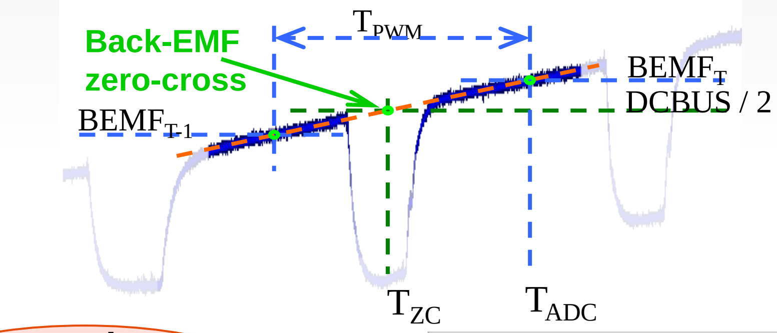
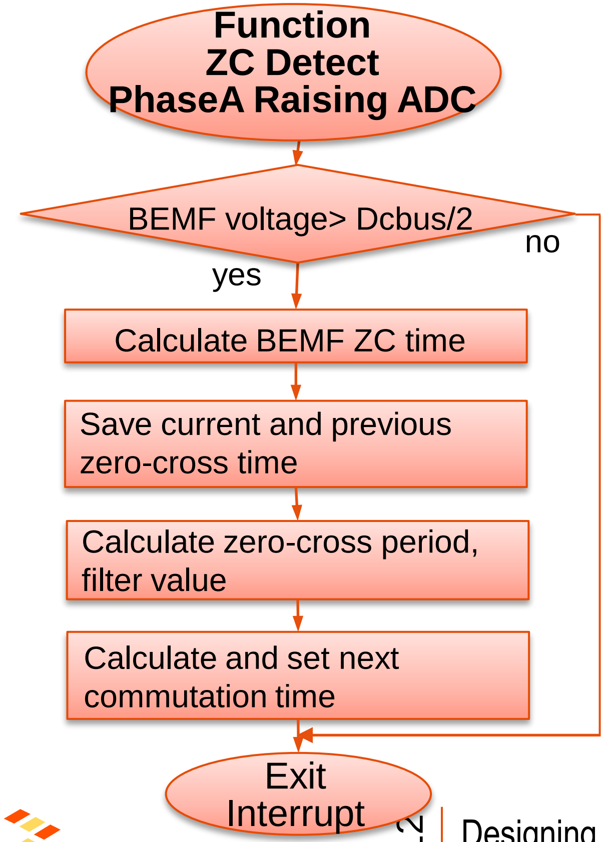
Zero-Cross detection



$$T_{ZC} = T_{ADC} - \frac{BEMF_T - DCBUS/2}{BEMF_T - BEMF_{T-1}} \cdot T_{PWM}$$



Function
ZC Detect
PhaseA Raising ADC
BEMF voltage> Dcbus/2
no
yes
Calculate BEMF ZC time
Save current and previous zero-cross time
Calculate zero-cross period, filter value
Calculate and set next commutation time
Exit
Interrupt

```
void ZCdetectPhAraisingAdc(void)
{
tFrac16 delta;
   if (bemfVoltage > 0)
   {        // In  Raising approximation bemF Voltage after ZC >0
      delta = bemfVoltage - bemfVoltageOld;    // > 0 for raising BEMF
      if ((driveStatus.bit.AdcSaved == 1) && (delta > bemfVoltage))
      {      // if delta > bemfVoltage then also delta > 0
         timeBEMF -= MLIB_Mul(MLIB_Div(bemfVoltage, delta, F16),
                             timeBEMF - timeOldBEMF, F16);
      }
     else      //  middle of previous ADC sensing events
     {  timeBEMF -= ((timeBEMF - timeOldBEMF) >> 1);
     }
      lastTimeZC = timeZC;
      timeZC = timeBEMF;
      periodZC_R_PhA = timeZC - lastTimeZC;
      actualPeriodZC = (actualPeriodZC + periodZC_R_PhA) >> 1;

      NextCmtPeriod = MLIB_Mul(actualPeriodZC, advanceAngle, F16);
      TIM_DEF.TC0.R = timeZC + NextCmtPeriod;

      driveStatus.bit.NewZC = 1;
..
```

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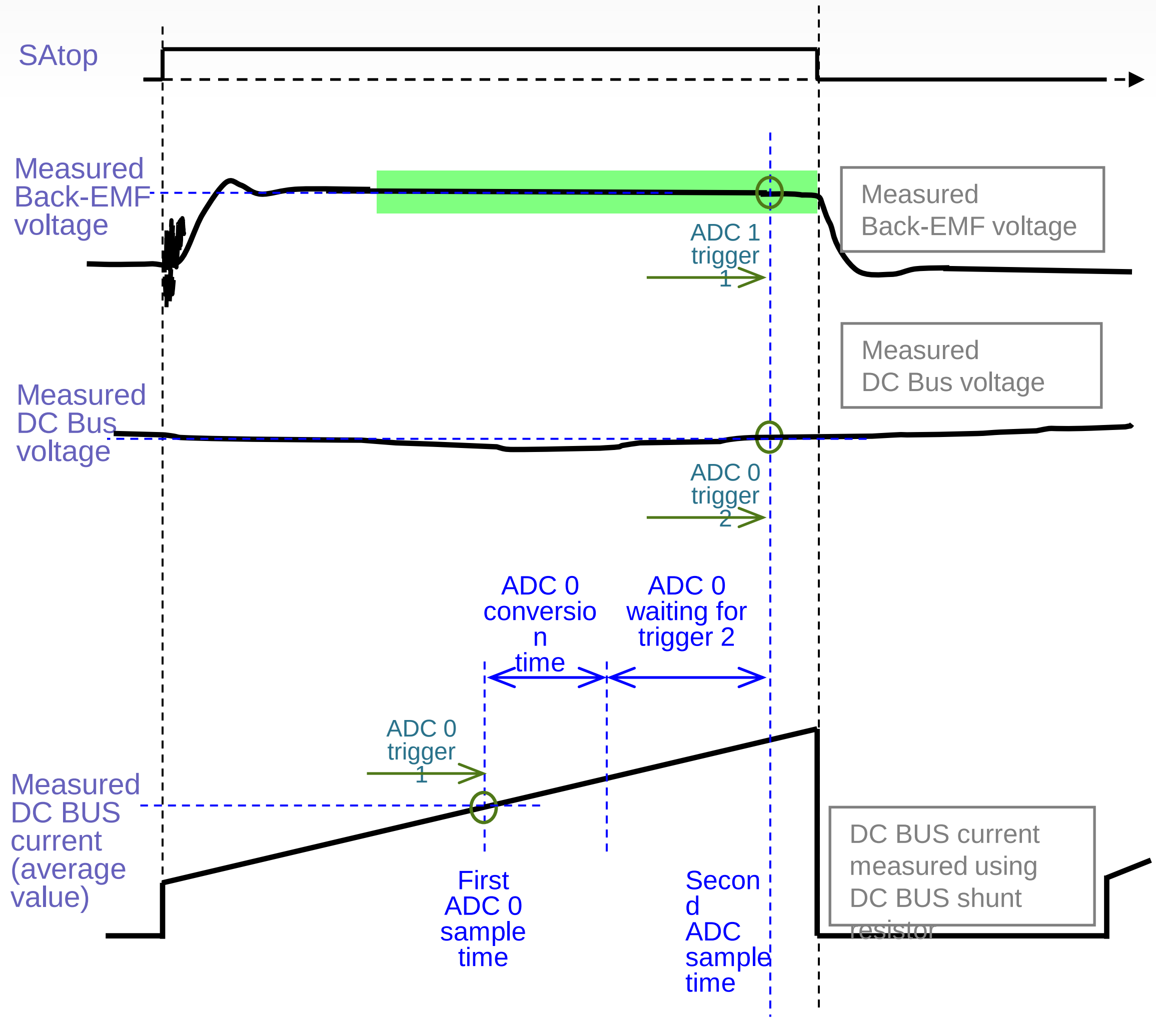
Measurement at low to high

Low to High PWM duty cycle:

- Back-EMF voltage measured close to the end of the PWM pulse

- DC Bus voltage measured at the same time as Back-EMF => precise Back-EMF ZC finding

- DC Bus current measured at the middle of PWM pulse => average current value measured


SAtop
Measured Back-EMF voltage
ADC 1 trigger 1
Measured Back-EMF voltage
Measured DC Bus voltage
ADC 0 trigger 2
Measured DC Bus voltage
ADC 0 conversio n time
ADC 0 waiting for trigger 2
ADC 0 trigger 1
Measured DC BUS current (average value)
First ADC 0 sample time
Secon d ADC sample time
DC BUS current measured using DC BUS shunt resistor

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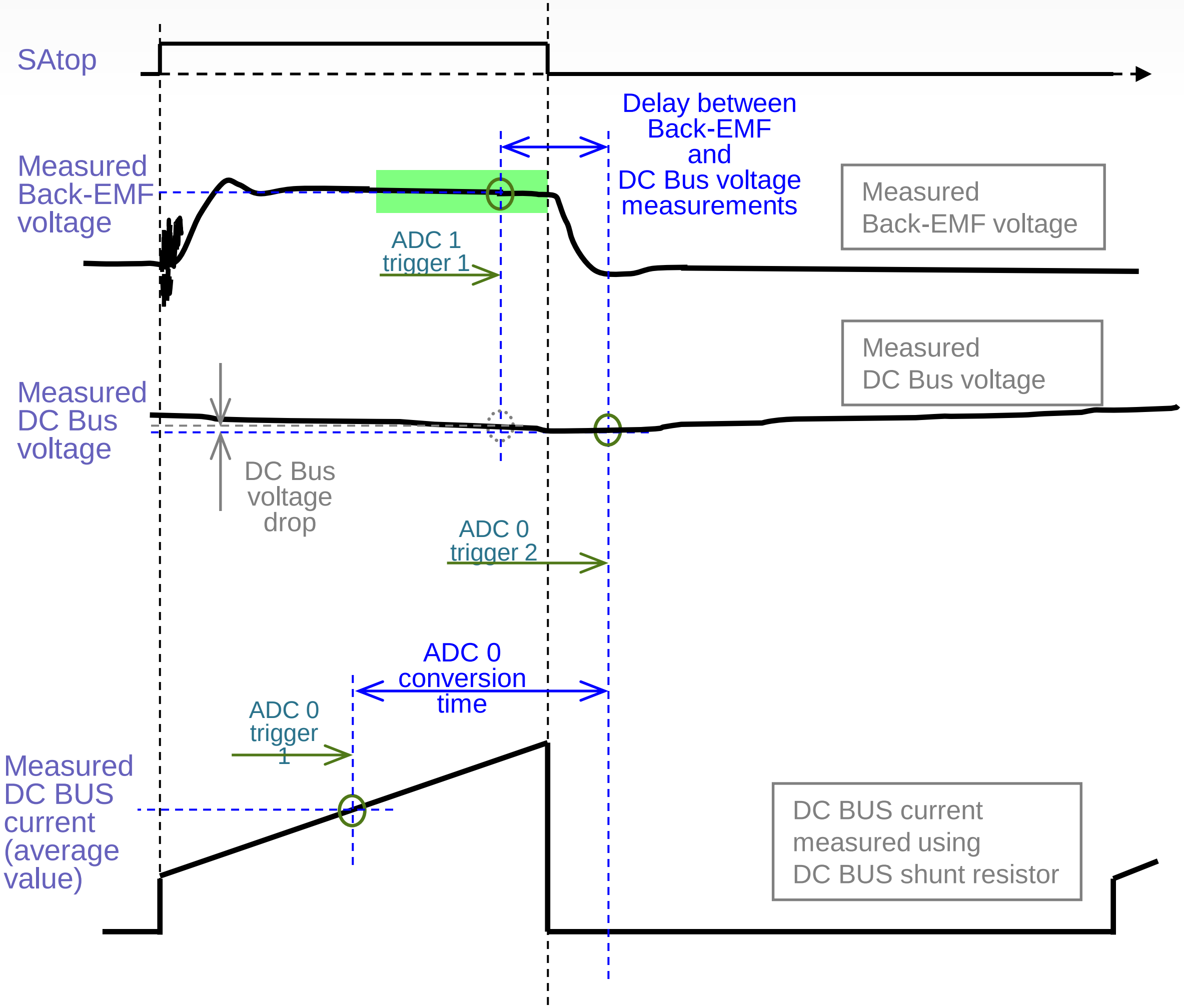
Measurement at very low duty cycle

Very Low PWM duty cycle:

- Back-EMF voltage measured close to the end of the PWM pulse

- DC Bus voltage measured at the different time than Back-EMF => less accuracy of Back-EMF ZC finding

- DC Bus current measured at the middle of PWM pulse => average current value measured


SAtop
Measured Back-EMF voltage
Delay between Back-EMF and DC Bus voltage measurements
Measured Back-EMF voltage
ADC 1 trigger 1
Measured DC Bus voltage
Measured DC Bus voltage
DC Bus voltage drop
ADC 0 trigger 2
ADC 0 conversion time
ADC 0 trigger 1
Measured DC BUS current (average value)
DC BUS current measured using DC BUS shunt resistor

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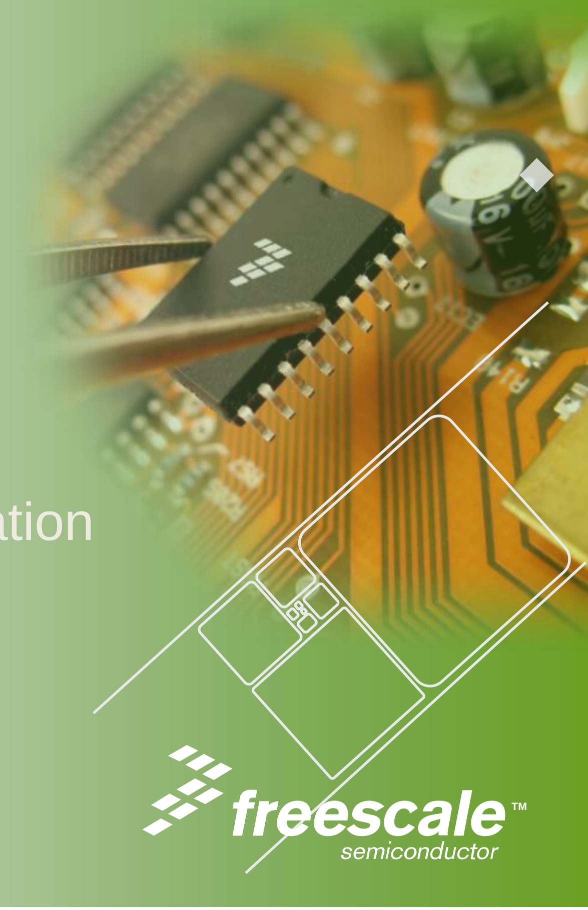

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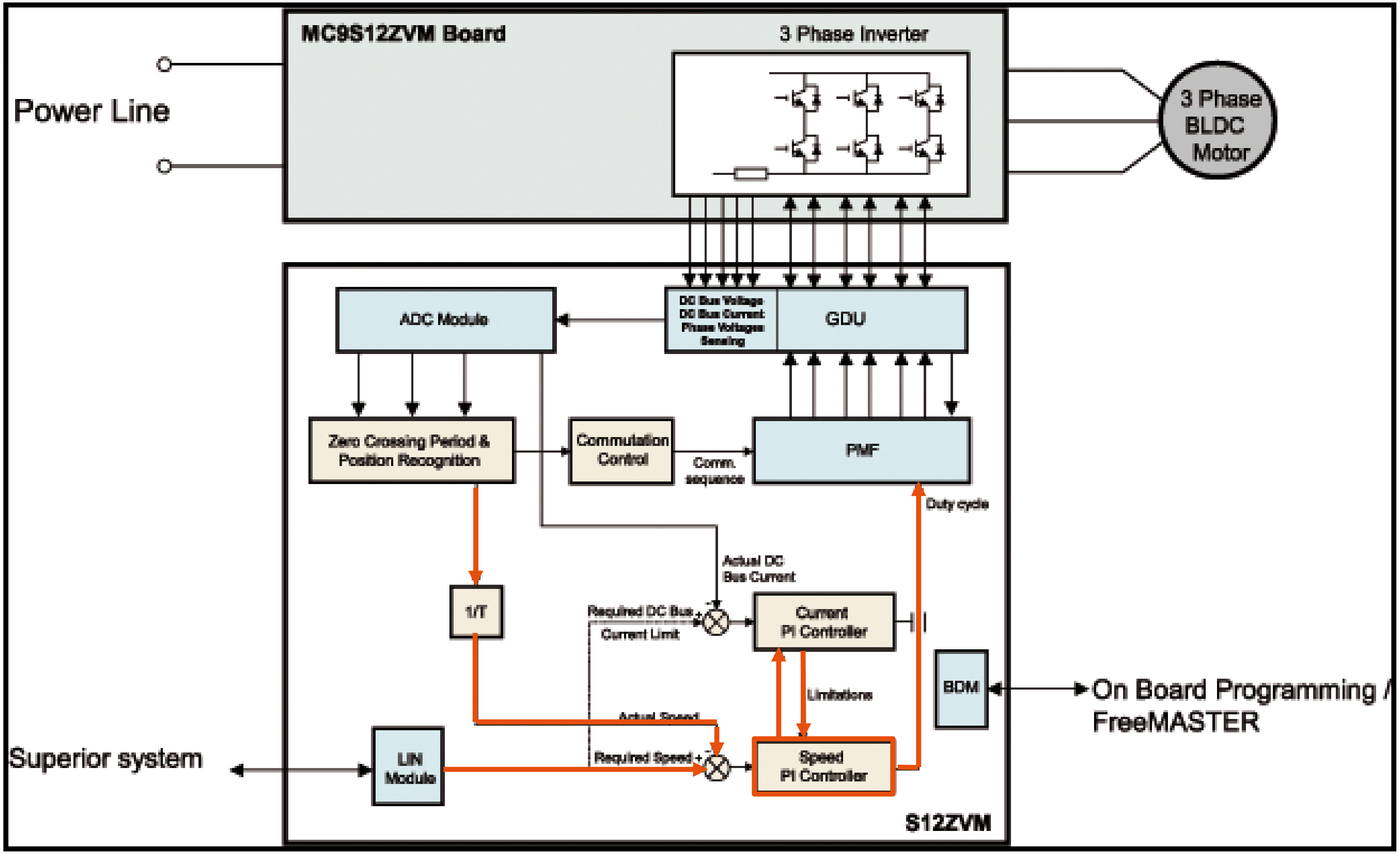
Example Control Block diagram



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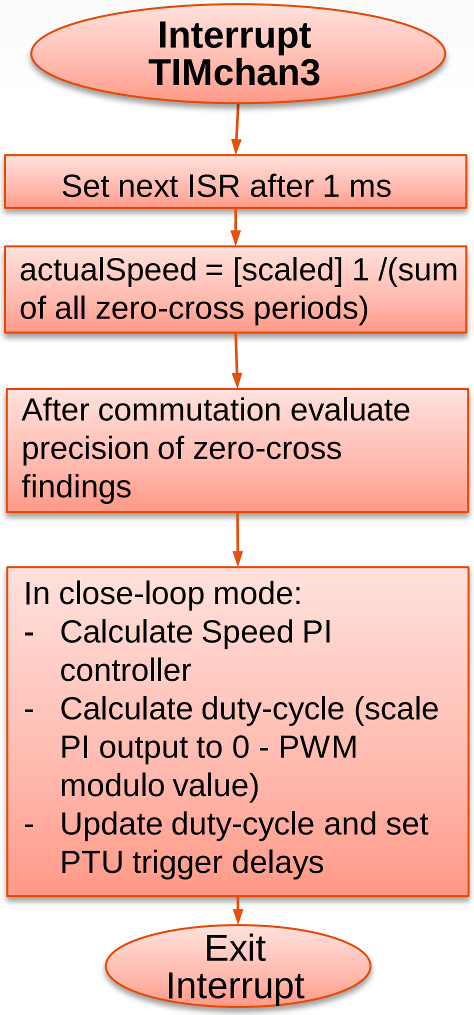
Speed Control Loop


Interrupt TIMchan3
Set next ISR after 1 ms
actualSpeed = [scaled] 1 /(sum of all zero-cross periods)
After commutation evaluate precision of zero-cross findings
In close-loop mode:
- Calculate Speed PI controller
- Calculate duty-cycle (scale PI output to 0 - PWM modulo value)
- Update duty-cycle and set PTU trigger delays
Exit Interrupt

```
@interrupt void TIMchan3_ISR(void)
{
  EnableInterrupts;

  TIM_DEF.TC3.R = TIM_DEF.TC3.R + 750;

  period6ZC = periodZC_F_PhA + periodZC_R_PhA +
              periodZC_F_PhB + periodZC_R_PhB +
              periodZC_F_PhC + periodZC_R_PhC;
  actualSpeed = SPEED_CALC_NUMERATOR / period6ZC;

  if (driveStatus.bit.StallCheckReq == 1) {
    driveStatus.bit.StallCheckReq = 0;
    StallError = StallCheck();
  }

  if (driveStatus.bit.Sensorless == 1)
  {
    speedErr = requiredSpeed - (tFrac16) actualSpeed;
    speedPIOut = GFLIB_ControllerPIrAW(speedErr, &speedPIPrms, F16);
    // duty cycle 0-1 -> 0-PWM_MODULO
    duty_cycle = MLIB_Mul(speedPIOut, PWM_MODULO, F16);
    UpdateDutycycle();
  }
  TIM_DEF.TFLG1.R = (1 << 3);
}
```

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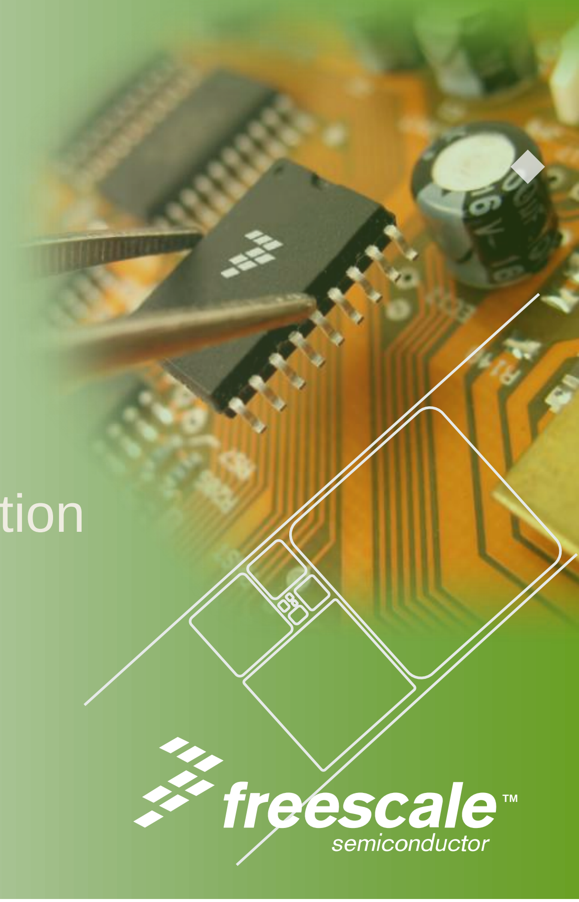

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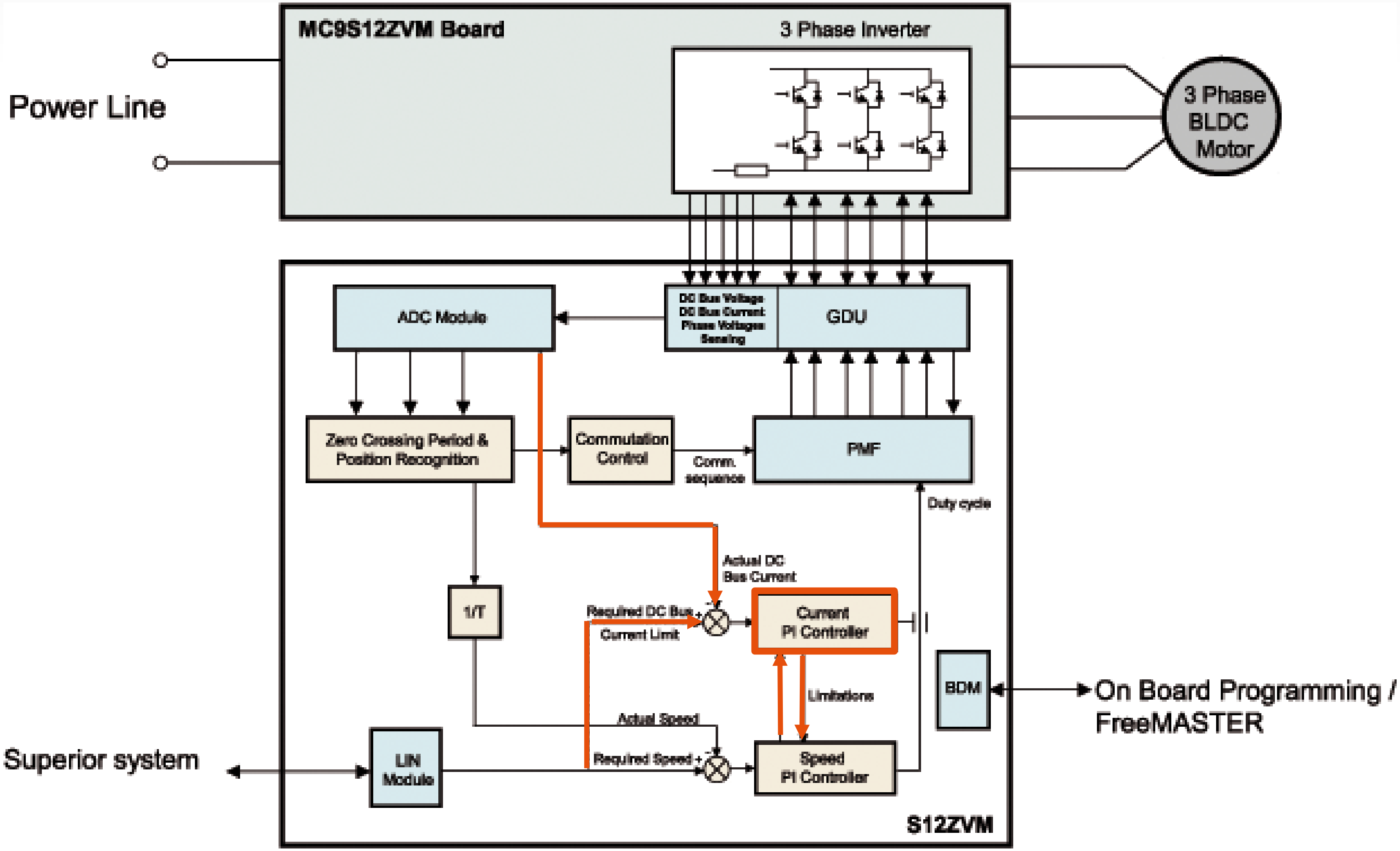

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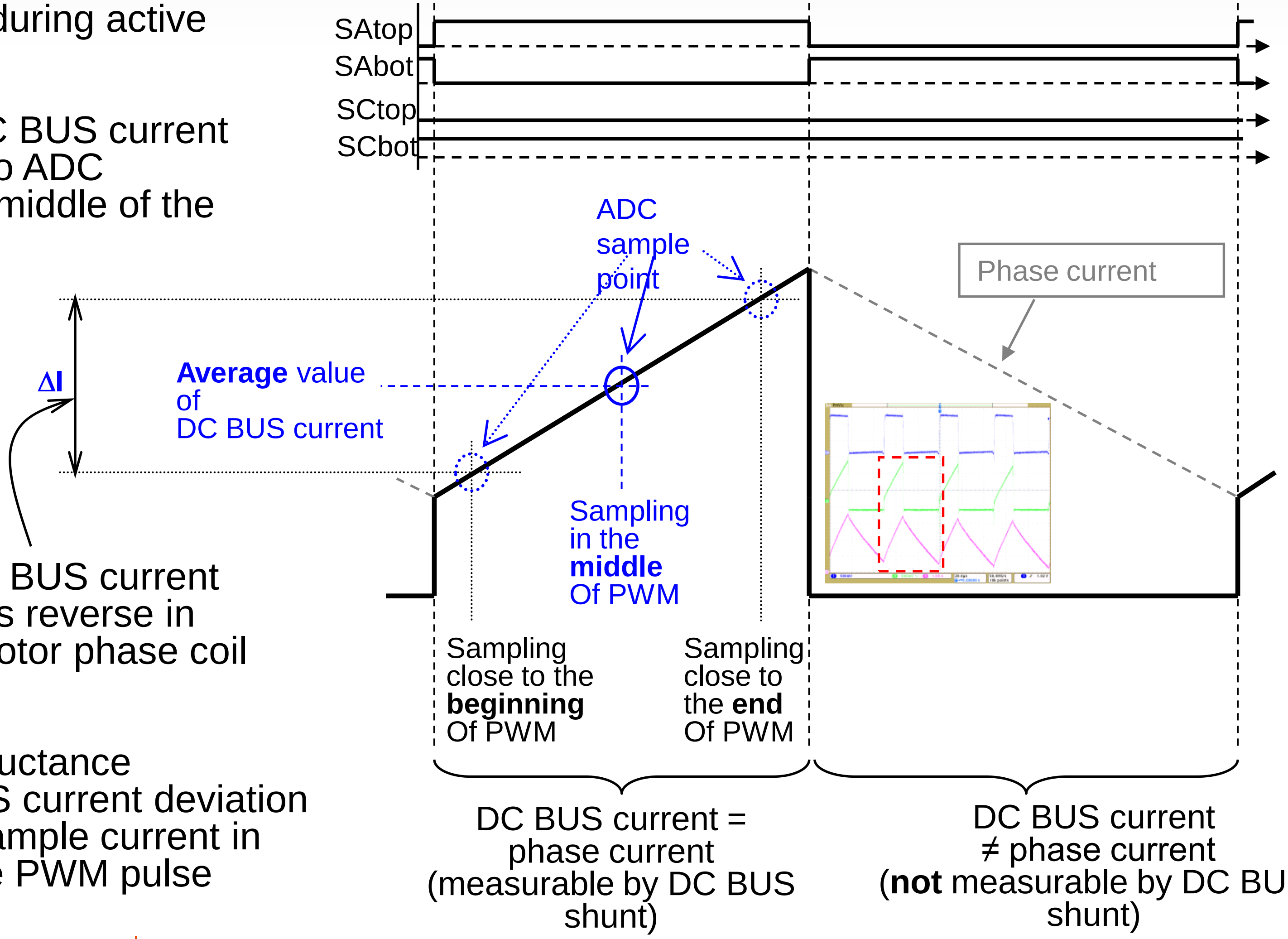
DC BUS Current Measurement

- DC BUS current can be measured only during active PWM pulse

- For precise DC BUS current measurement do ADC sampling in the middle of the PWM pulse



ADC sample point

Phase current

Average value of DC BUS current

Sampling in the **middle** Of PWM

Sampling close to the **beginning** Of PWM

Sampling close to the **end** Of PWM

DC BUS current = phase current (measurable by DC BUS shunt)

DC BUS current ≠ phase current (**not** measurable by DC BUS shunt)

- Measured DC BUS current difference (**ΔI**) is reverse in proportion to motor phase coil inductance:

- low phase inductance
-> high DC BUS current deviation
-> needed to sample current in middle of active PWM pulse

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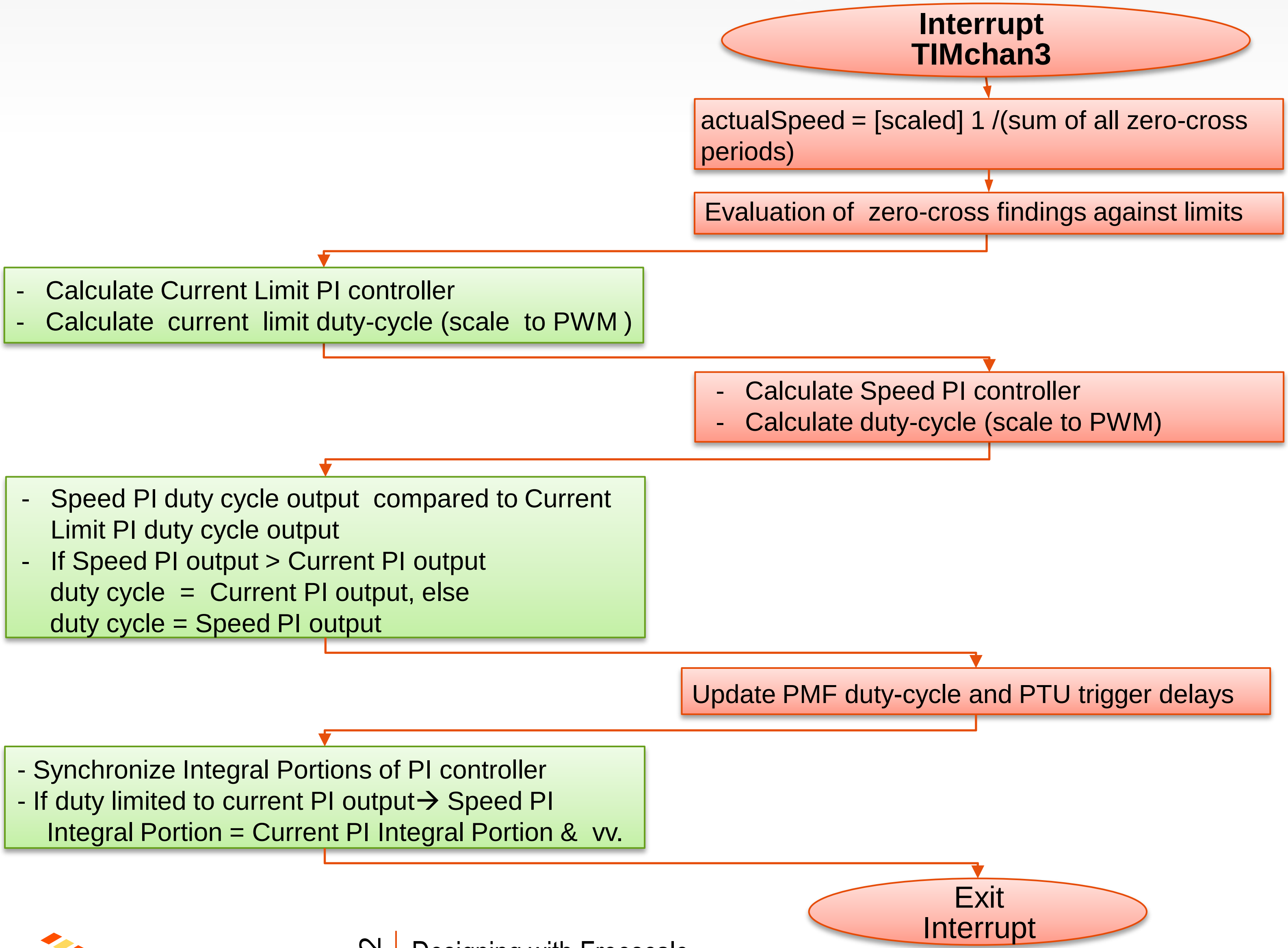
Current Limit Outer Control loop



Interrupt TIMchan3

actualSpeed = [scaled] 1 /(sum of all zero-cross periods)

Evaluation of zero-cross findings against limits

- Calculate Current Limit PI controller
- Calculate current limit duty-cycle (scale to PWM)

- Calculate Speed PI controller
- Calculate duty-cycle (scale to PWM)

- Speed PI duty cycle output compared to Current Limit PI duty cycle output
- If Speed PI output > Current PI output
  duty cycle = Current PI output, else
  duty cycle = Speed PI output

Update PMF duty-cycle and PTU trigger delays

- Synchronize Integral Portions of PI controller
- If duty limited to current PI output→ Speed PI Integral Portion = Current PI Integral Portion & vv.

Exit Interrupt

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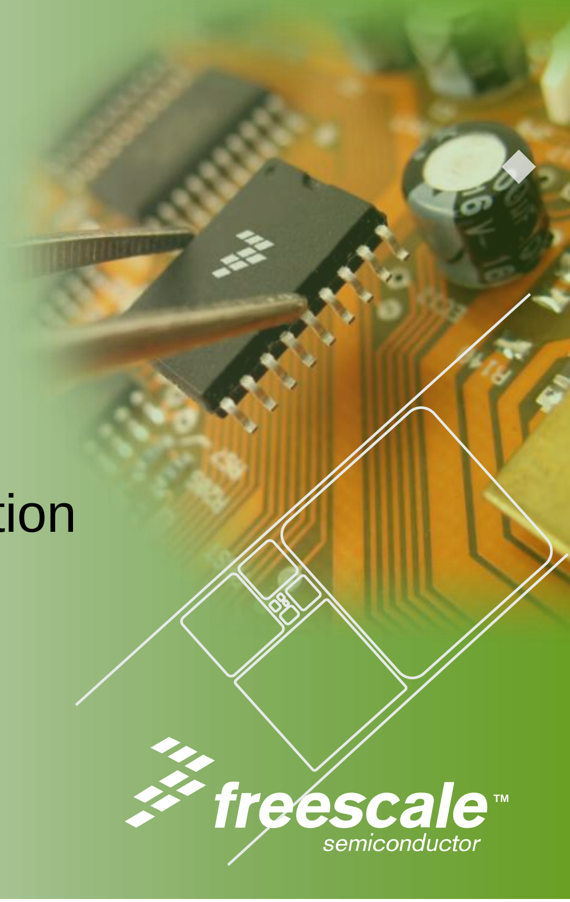

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Advantages with S12ZVM

Board Level Advantages

- Highest **level of Integration**
- less components lead to **smaller placement cost**
- smaller PCB size lead to **smaller PCB cost**
- motor control platform can be covered with one layout due to **family concept**
- optional external bypass transistor **improves thermal board management**
- boost option can **cover different operating range** requirements with one layout
- high speed Boost frequency supported to **minimize size of external components**
- Two-Shunt systems supported **without the need for external Amplifier**
- selectable slope in **gate driver for optimized EMC** performance
- **more robust against EMC** due to integrated connections between GDU and µC
- **no external resonator** might be required, due to trimmed RC oscillator, +/- 1.3%

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Advantages with S12ZVM

Software Level Advantages

- **High performance core** with 32bit ALU and MAC unit up to 100MHz fcore
- High **code density** with ~ 20% improvement versus 16bit S12 core
- **Mature tool chain** of S12 family
- Supports **different sensorless position sensing strategies** (integrated zero crossing comparators & phase voltage multiplexers)
- Fully **autonomous motor control loop** with very small CPU load due to auto-triggering of ATD synchronous to PWM
- **Double buffered** ATD and Trigger command list and ATD result list allows easy SW handling
- Available **Motor control SW library** reduces time to market
- **Double switching** feature of PMF module easily supports Single-Shunt systems
- Easy debugging:: Very fast Single wire debugging interface, flexible watchdog

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Advantages with S12ZVM

System Level Advantages

- Improved **Accuracy of Position sensing** due to integration level
- dual ATD converter concept supports high accuracy of position sensing
- Flexible **Operation range down to 3.5V Vsup** with selectable boost option
- integrated charge pump supports **100% duty cycle**
- high **PMF resolution** & speed up to **50kHz** covers large range of motor applications
- **high safety level**
    - integrated desaturation and overcurrent comparators
    - Protection against unintended clock and gate drive unit register access
    - Flash/EEPROM margin read for run time cell status check

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Advantages with S12ZVM

System Level Advantages

- High grade **of system testability**
  - High grade of failure status reporting and reset status flagging
  - Sophisticated temperature and voltage monitoring capabilities
  - High speed SPI or 250kbaud LIN usable as test interface
- Continuous **Automotive Quality improvement**
  - Reduction of BOM and soldering points in system
  - Robust 180nm technology with zero defect strategy
  - NVM and RAM ECC & protection

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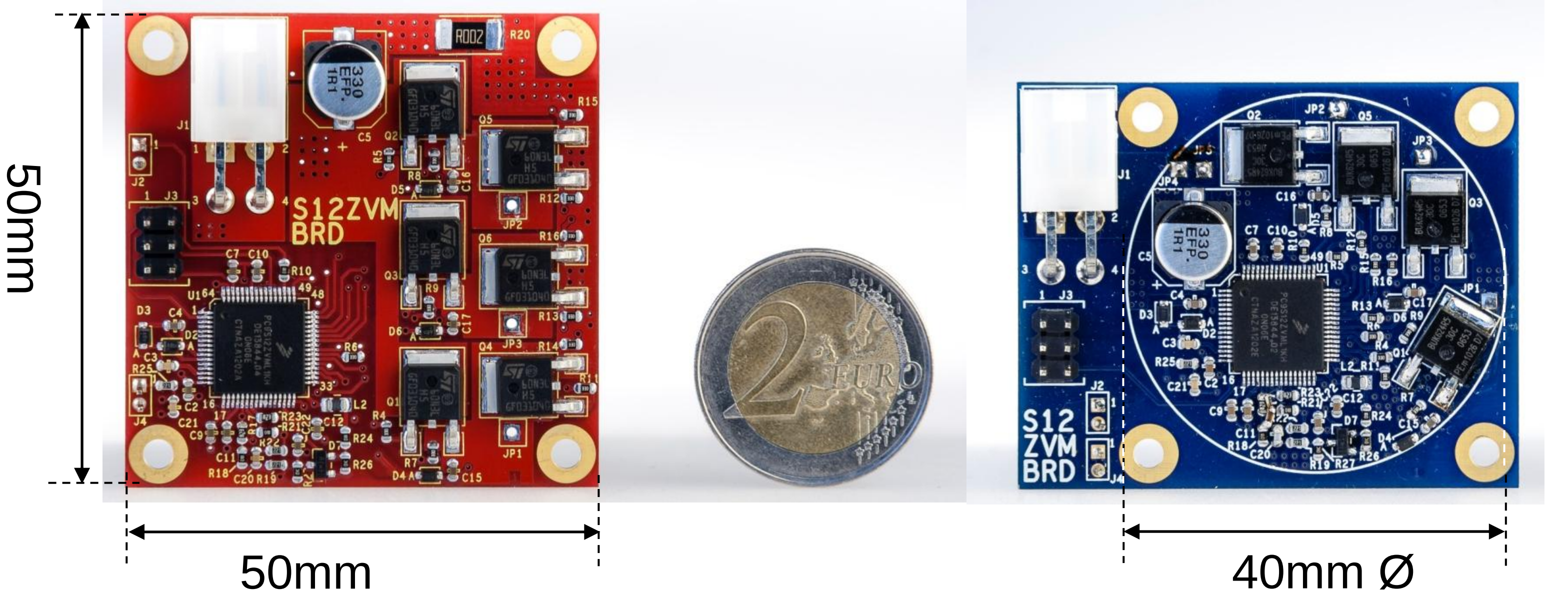
Highest level of Integration

Of your BLDC system:



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