TWR-MPC8309 Schematic

SCHEMATIC PAGE DESCRIPTION:

01: Cover
02: Reset, Clock and Switch
03: DDR2 and NOR Flash Memory
04: eLBC, Latch, Buffer and Logics
05: Display, SD Card and CAN
06: Ethernet Interface and Clock
07: Ethernet PHYs and RJ45
08: USB Interface and USB PHY
09: RS485, RS232 and RS232 MUX
10: PCI Interface and Mini PCI Connector
11: Primary and Secondary Elevators
12: ColdFire MCU, IEEE1588, JTAG and I2C Device
13: Audio CODEC
14: MPC Decoupling
15: Power Supplies

MAJOR REVISION HISTORY:

PCB REV.	SCM REV.	DESCRIPTION	DATE
30	A	Initial Version	4/12/2011
31	B	Production Version	9/14/2011
32	C	Modify Audio	10/26/2011

PCB MECHANICAL DETAILS:

1: PCB SIZE: 90mm x 70mm
2: PCB MATERIAL: FR4
3: NUMBER OF LAYERS: 08
4: IMPEDENCE CONTROL: YES

VOLTAGE RAIL NOTATION

PWR RAIL	DESCRIPTION
+5V	5.0V Input voltage from sources
+5V_ELEV	5.0V Input/output voltage to/from tower system
+3.3V	3.3V MPC & Other I/O Voltage
+3.3V_ELEV	3.3V Output to Tower system
+1.8V	1.8V MPC & DDR I/O voltage
+1.0V	1.0V MPC Core Voltage

NOTES, UNLESS OTHERWISE SPECIFIED:

1. RESISTANCE TOLERENCE IS 5% IF NOT SPECIFIED
2. PARTS NOT INSTALLED ARE INDICATED WITH 'NP'.
3. SIGNAL NET NAMES WITH "#" SUFFIX, ARE ACTIVE LOW SIGNALS.
4. PACKAGE SIZE FOR DESCRETES IS "0402" IF NOT SPECIFIED

I2C2 ADRESS DETAILS

1. Audio CODEC, SGTL5000 = 0x0A
2. Digital Accelerometer, MMA8541 = 0x1C
3. MPR121 on Display Module = 0x5B (ADDR pin = VDD)

COMPONENT MOUNT / UNMOUNT NOTATIONS:

NOTATION (IN "MOUNTING" PROPERTY FIELD)	MOUNTING INSTRUCTIONS
BLANK	COMPONENT TO BE POPULATED
NP	NOT POPULATE

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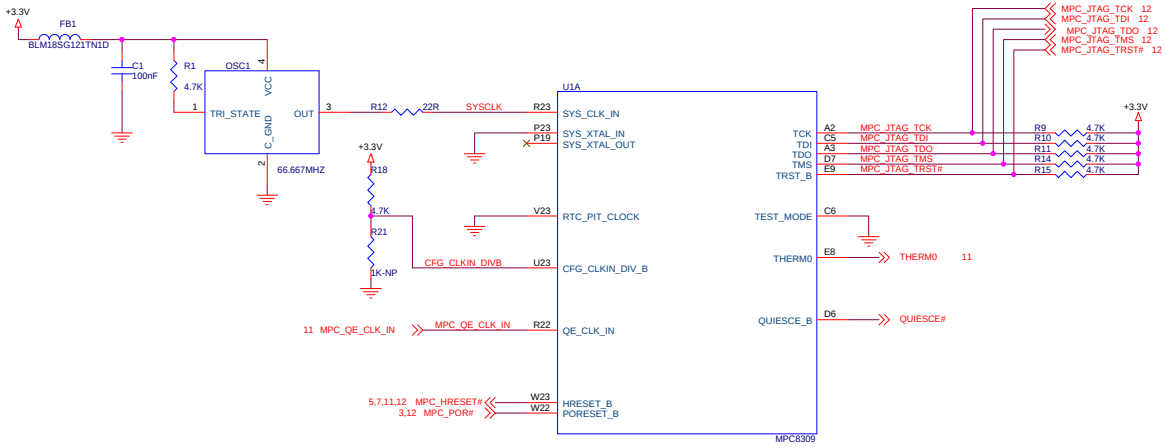
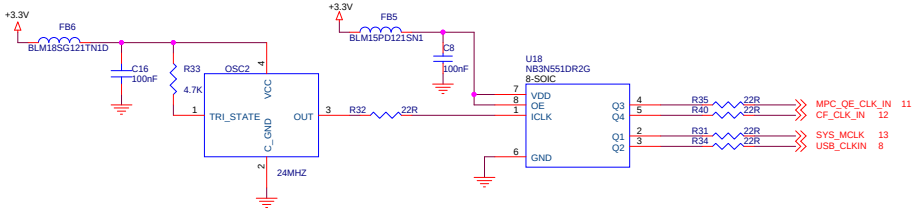
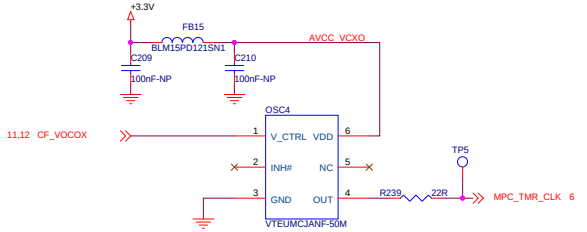
MPC RESET, CLOCK & Switch

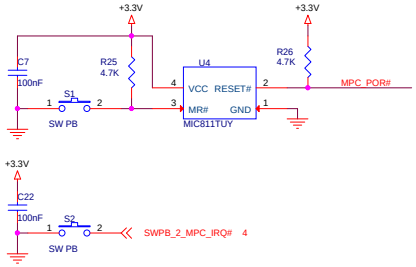


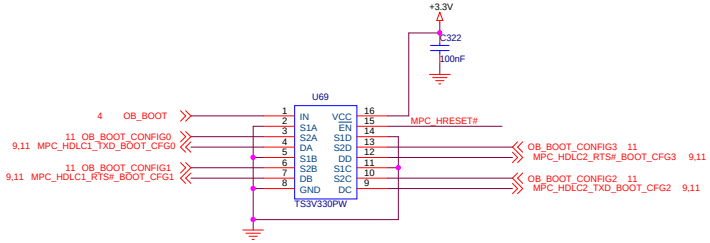


IEEE1588 Clock Generation

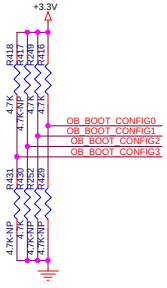


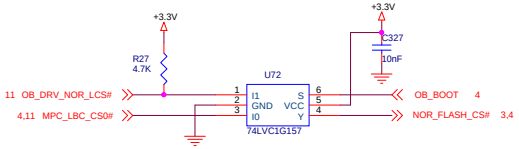
MPC Boot MUX





When IN=0, D=S1
Boot from on board NOR flash
When IN=1, D=S2
Boot from SD card





When S=0,
CS0# = ON BOARD FLASH CS
When S=1
CS0# = OFF BOARD CS

Reset Configuration Words Source

CFG_RESET SOURCE[0:3]	DESCRIPTION
0000	RCW from eLBC NOR (Default)
0001	RCW from eLBC NAND (small page 8-bit)
0010	Reserved
0011	Reserved
0100	RCW from I2C
0101	RCW from eLBC NAND (large page 8-bit)
0110	Reserved
0111	Reserved
1000	RCW hard-coded, boot from eLBC
1001	RCW hard-coded, boot from eLBC
1010	RCW hard-coded, boot from eLBC
1011	RCW from eLBC NOR
1100	RCW hard-coded, boot from eLBC
1101	RCW hard-coded, boot from eSDHC (OB_BOOT default)
1110	RCW hard-coded, boot from eSDHC
1111	RCW hard-coded, boot from SPI

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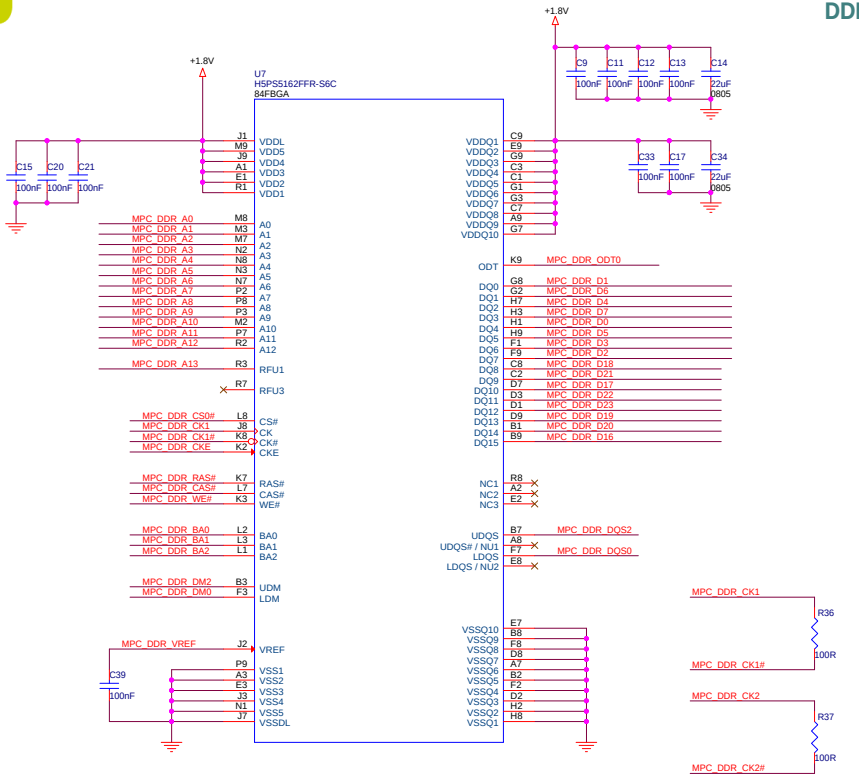
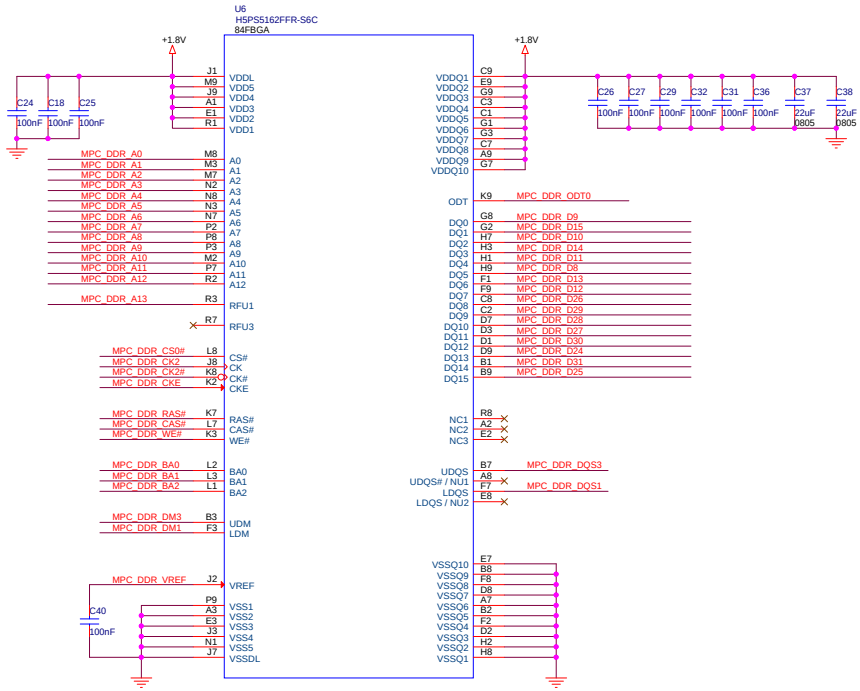
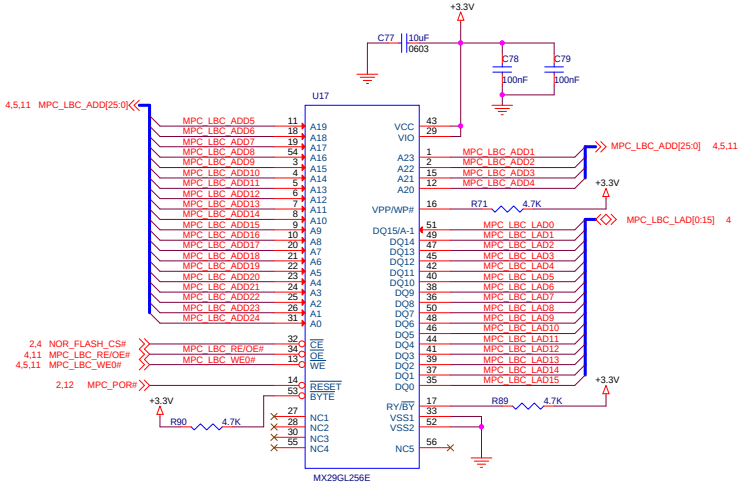
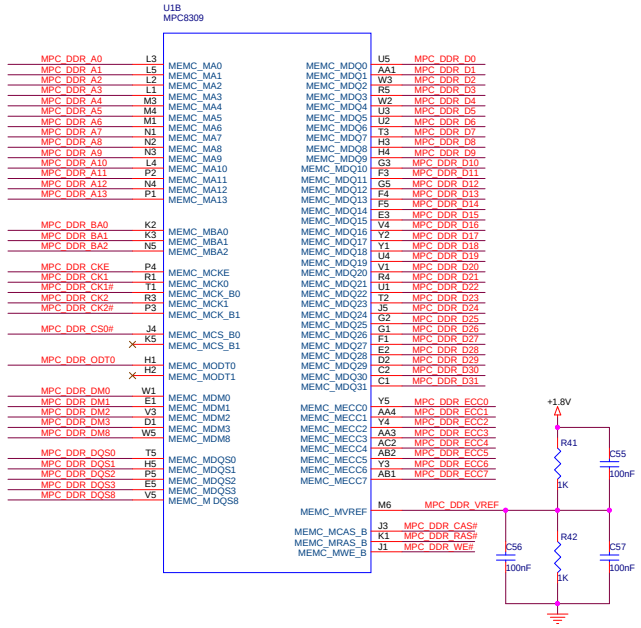
DDR2 Memory





NOR FLASH





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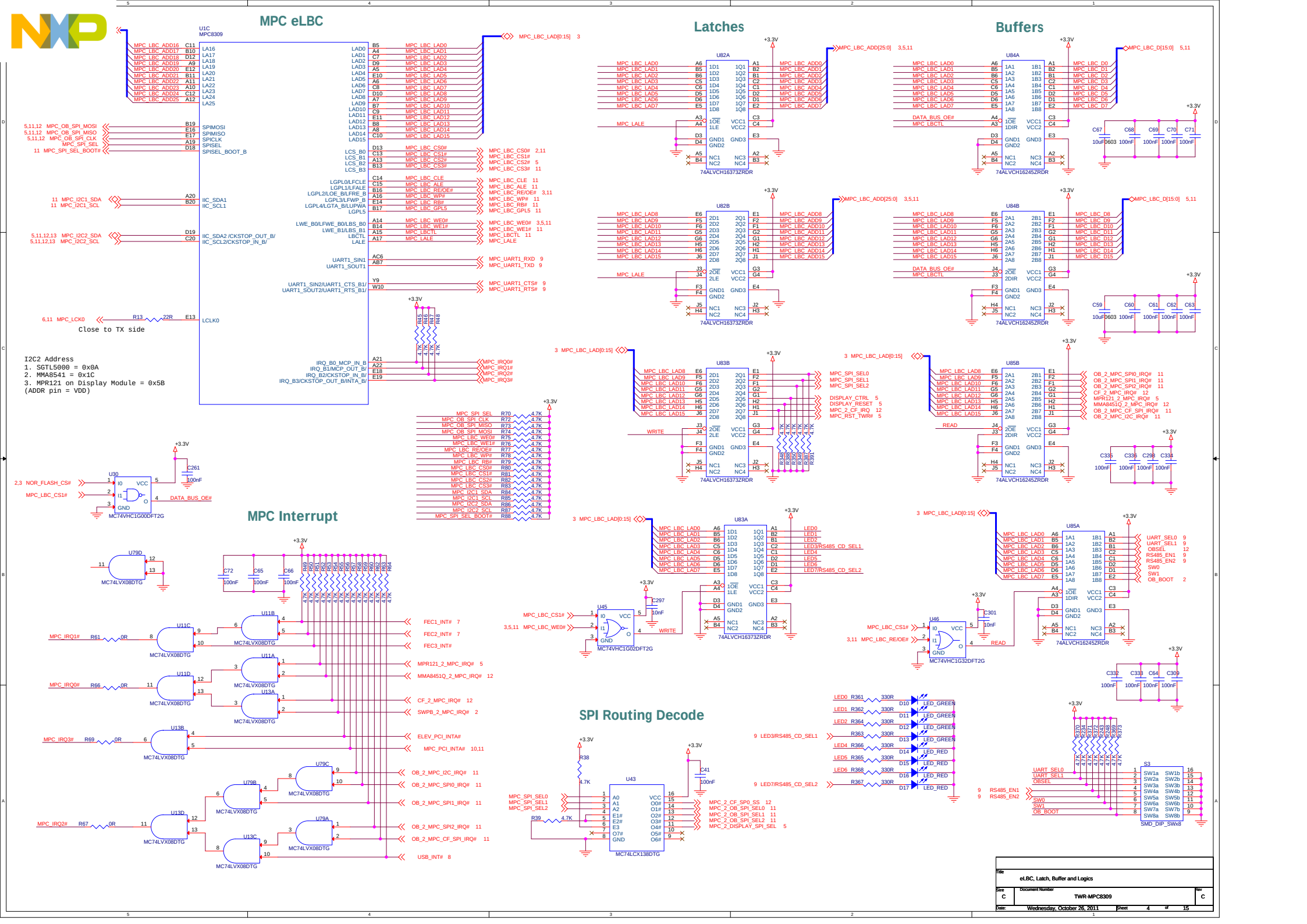
MPC eLBC
Latches
Buffers
MPC Interrupt
SPI Routing Decode
Close to TX side
I2C2 Address
1. SGTL5000 = 0x0A
2. MMA8541 = 0x1C
3. MPR121 on Display Module = 0x5B
(ADDR pin = VDD)
U1C
MPC8309
U82A
U82B
U84A
U84B
U83B
U83A
U85B
U85A
U30
U45
U46
U43
74ALVCH16373ZRDR
74ALVCH16245ZRDR
MC74VHC1G00DFT2G
MC74VHC1G02DFT2G
MC74VHC1G32DFT2G
MC74LVX08DTG
MC74LCX138DTG
eLBC, Latch, Buffer and Logics
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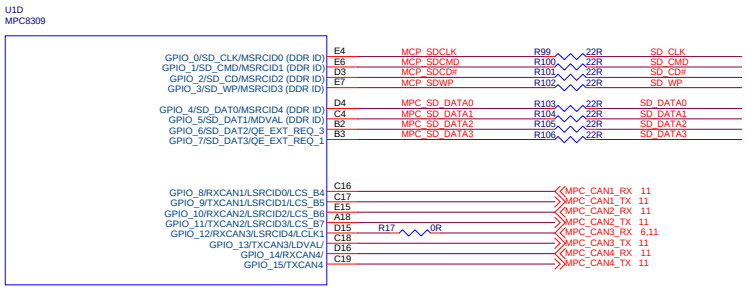
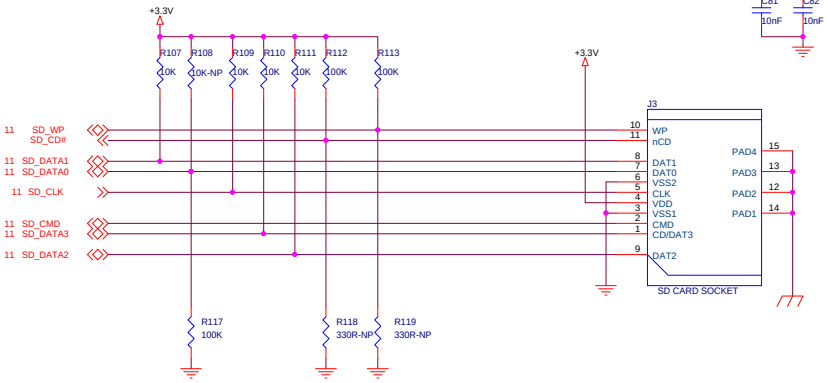
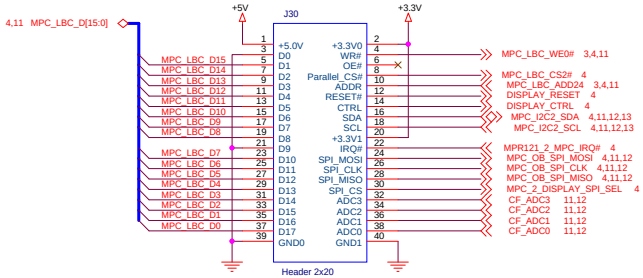
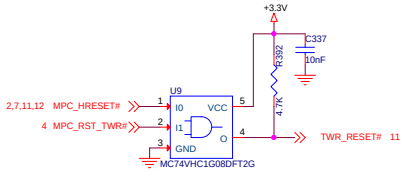
Display, SD Card and CAN Signals





Display Connector





I2C2 Address = 0x5B
Assume MPR121 on Display Module with ADDR pin = VDD

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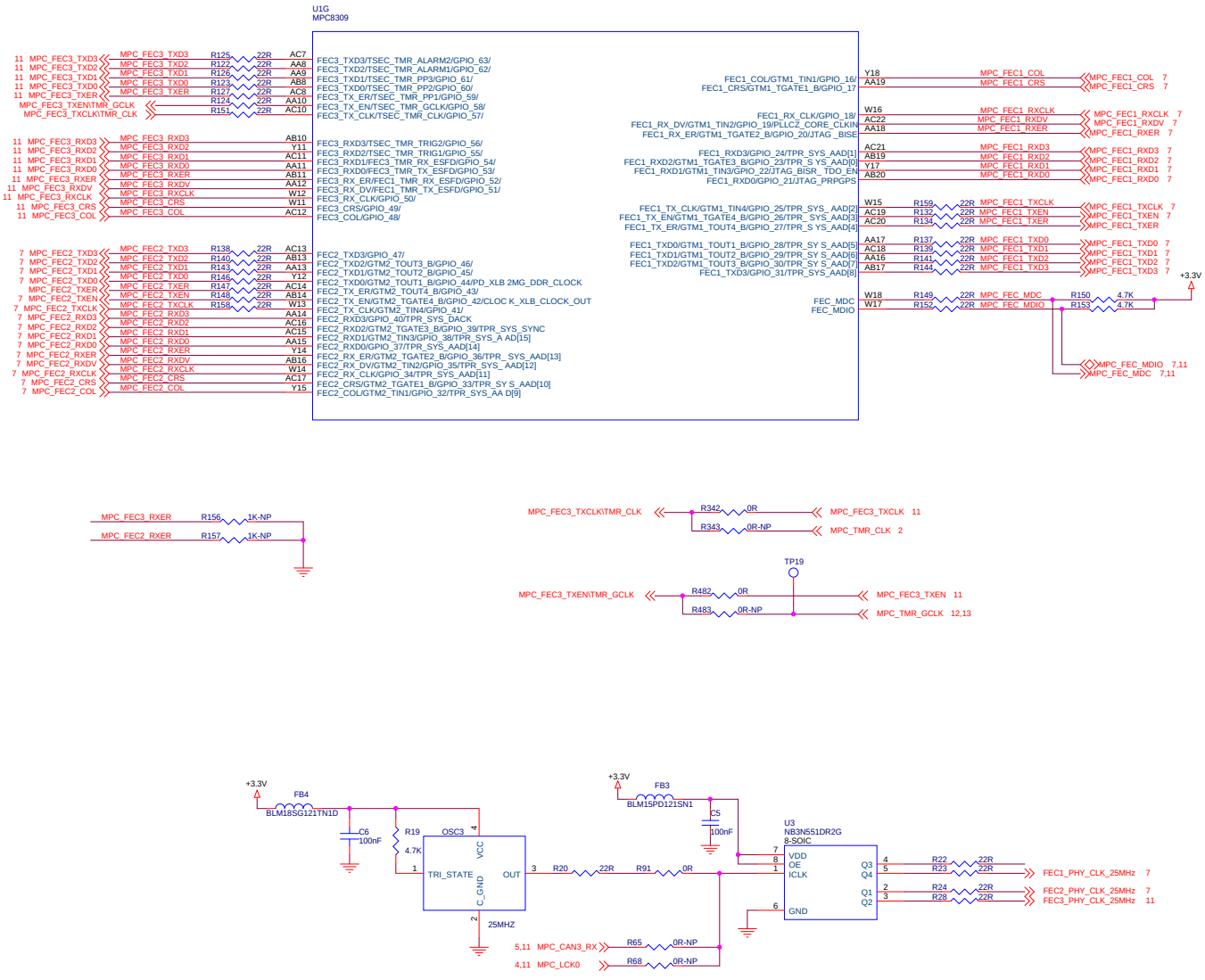
MPC FEC1,FEC2 & FEC3



Title	Ethernet Interface and Clock		
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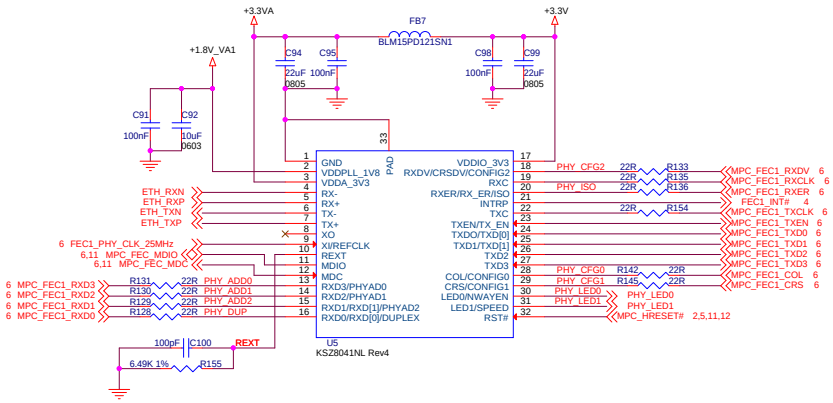
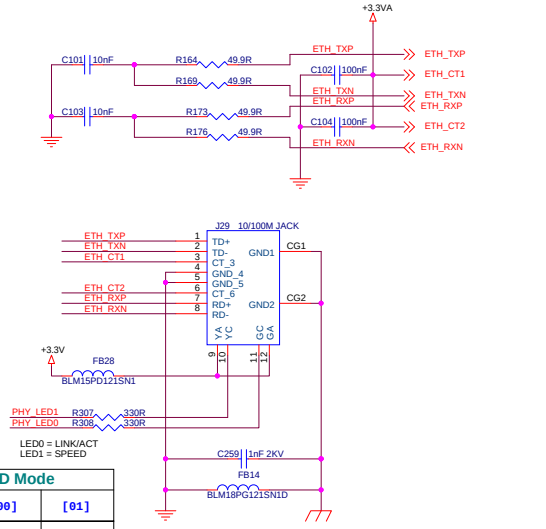
10/100 ETHERNET PHY



10/100 RJ45 with Magnetics

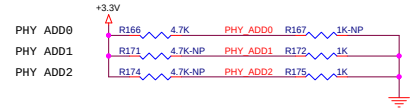


LED Mode		
LED #	[00]	[01]
LED0	LINK/ACT	LINK
LED1	SPEED	SPEED

Note:
Software: Configure LED mode for [00] setting

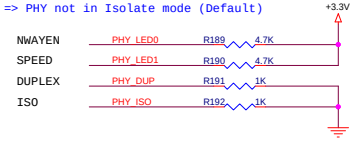
PHY BOOT STRAPS

PHY ADDRESS[4:0]=>0X00001

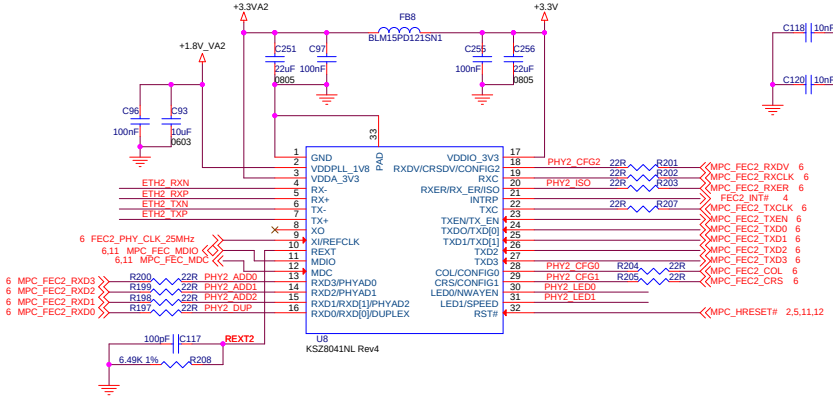


CONFIG[0:2]=>000 MII

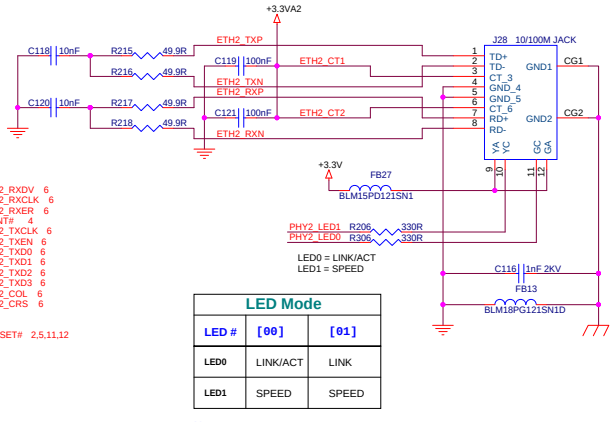
NWAYEN=>Auto Nego Enable(default)
SPEED=>100Mbps(default)
DUPLEX=>FULL DUPLEX
ISO => PHY not in Isolate mode (Default)



10/100 ETHERNET PHY



10/100 RJ45 with Magnetics

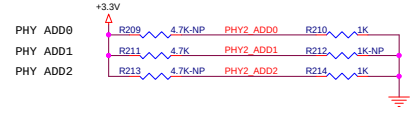


LED Mode		
LED #	[00]	[01]
LED0	LINK/ACT	LINK
LED1	SPEED	SPEED

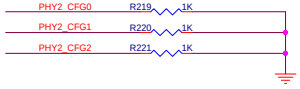
Note:
Software: Configure LED mode for [00] setting

PHY BOOT STRAPS

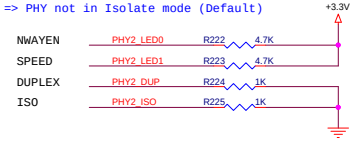
PHY ADDRESS[4:0]=>0X00010



CONFIG[0:2]=>000 MII



NWAYEN=>Auto Nego Enable(default)
SPEED=>100Mbps(default)
DUPLEX=>FULL DUPLEX
ISO => PHY not in Isolate mode (Default)



Title	ETH PHYs & RJ45		
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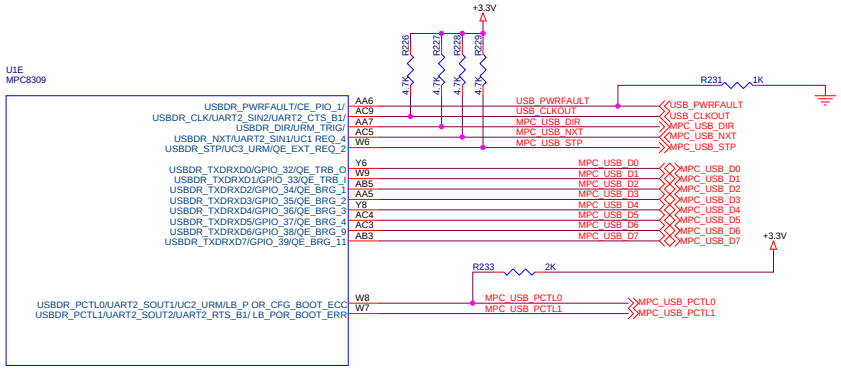
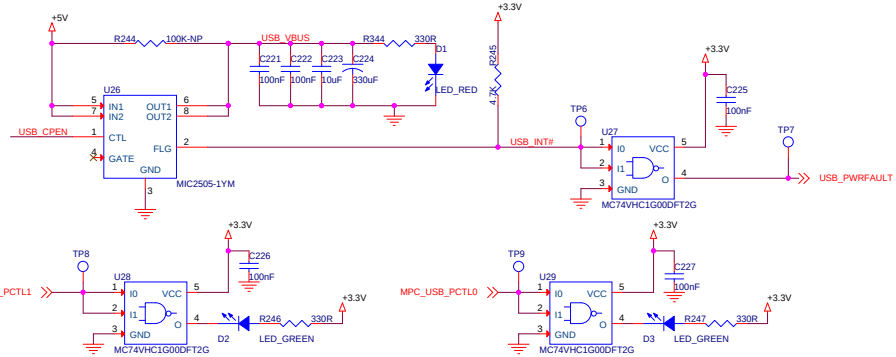
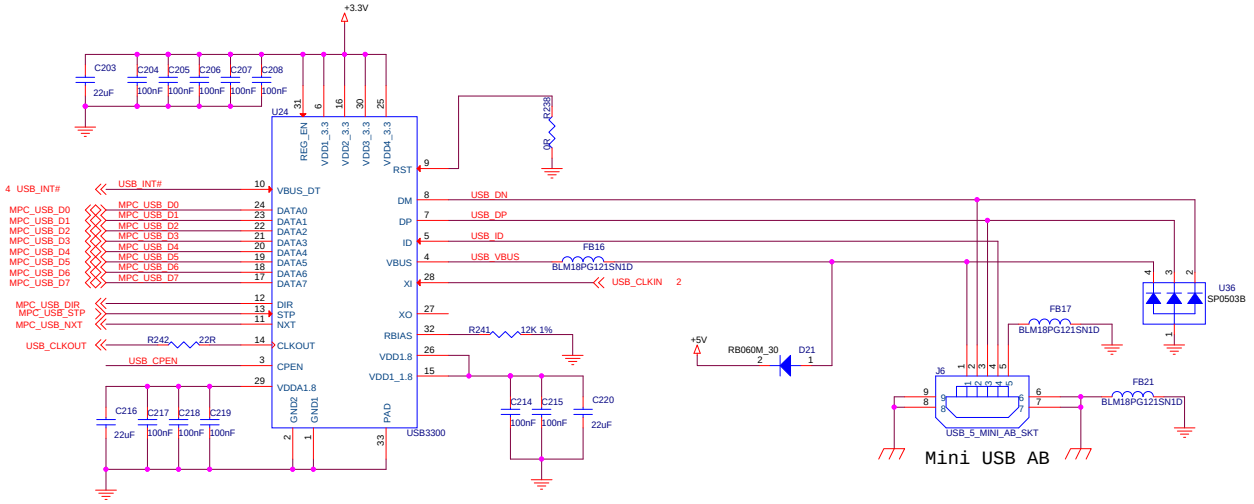
USB Interface





USB PHY



Title	USB Interface and USB PHY		
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MPC - HDLC

U1H
MPC8309

HDLC1_TXCLK/GPIO_0/QE_BRG_5/TDM1_TCK
HDLC1_TXD/GPIO_2/TDM1_TD/CFG_RESET_S OURCE[0]
HDLC1_CD_B/GPIO_4/TDM1_TFS/
HDLC1_RXCLK/GPIO_1/TDM1_RCK/
HDLC1_RXD/GPIO_3/TDM1_RD/
HDLC1_CTS_B/GPIO_5/TDM1_RFS/
HDLC1_RTS_B/GPIO_6/TDM1_STROBE_B/CFG _RESET_SOURCE[1]

AA20 MPC_HDLC1_TCK → MPC_HDLC1_TCK 11
AB22 MPC_HDLC1_TXD_BOOT_CFG0 → MPC_HDLC1_TXD_BOOT_CFG0 2,11
W19 MPC_HDLC1_CD# → MPC_HDLC1_CD# 11
AA21 MPC_HDLC1_RCK → MPC_HDLC1_RCK 11
AB23 MPC_HDLC1_RXD → MPC_HDLC1_RXD 11
V19 MPC_HDLC1_CTS# → MPC_HDLC1_CTS# 11
AA23 MPC_HDLC1_RTS#_BOOT_CFG1 → MPC_HDLC1_RTS#_BOOT_CFG1 2,11

HDLC2_TXCLK/GPIO_16/QE_BRG_7/TDM2_TCK
HDLC2_TXD/GPIO_18/TDM2_TD/CFG_RESET_ SOURCE[2]
HDLC2_CD_B/GPIO_20/TDM2_TFS/
HDLC2_RXCLK/GPIO_17/TDM2_RCK/QE_BRG_ 6
HDLC2_RXD/GPIO_19/TDM2_RD/
HDLC2_CTS_B/GPIO_21/TDM2_RFS/
HDLC2_RTS_B/GPIO_22/TDM2_STROBE_B/CF G_RESET_SOURCE[3]

Y20 MPC_HDLC2_TCK → MPC_HDLC2_TCK 11
W20 MPC_HDLC2_TXD_BOOT_CFG2 → MPC_HDLC2_TXD_BOOT_CFG2 2,11
V20 MPC_HDLC2_CD# → MPC_HDLC2_CD# 11
Y22 MPC_HDLC2_RCK → MPC_HDLC2_RCK 11
W21 MPC_HDLC2_RXD → MPC_HDLC2_RXD 11
Y23 MPC_HDLC2_CTS# → MPC_HDLC2_CTS# 11
U20 MPC_HDLC2_RTS#_BOOT_CFG3 → MPC_HDLC2_RTS#_BOOT_CFG3 2,11

RS232 PHY

U53 MAX3232CUE
C1+ C1- C2+ C2- V+ V- T1-IN T2-IN T1-OUT T2-OUT R1-OUT R2-OUT R1-IN R2-IN GND VCC
UART-C1+ UART-C1- UART-C2+ UART-C2- UART-V+ UART-V-
C305 C307 C310 C311 C312 100nF
PHY_UART_TXD PHY_UART_RTS# PHY_UART_RXD PHY_UART_CTS#
RS232_TXD RS232_RTS RS232_RXD RS232_CTS
R352 4.7K R353 4.7K
+3.3V

J7 RA Header 2x3 2.54mm
R355 R459 0R-NP 0R
RS232_TXD RS232_RTS RS232_RXD RS232_CTS

Quad 4:1 mux

U80 TS3A5017PW
U81 TS3A5017PW
1EN# 1N2 1S4 1S3 1S2 1S1 1D GND V+ 2EN# 2N1 2S4 2S3 2S2 2S1 2D
C320 C354 100nF
4 UART_SEL0
12 CF_UART1_TXD
11 TEP_UART1_TXD
PHY_UART_RXD
4 MPC_UART1_RXD
UART_SEL1 4
CF_UART1_RXD 12
CF_UART1_RXD 12
TEP_UART1_RXD 11
PHY_UART_TXD
MPC_UART1_TXD 4
11,12 CF_UART1_RTS#
11 TEP_UART1_CTS#
PHY_UART_CTS#
4 MPC_UART1_CTS#
TEP_UART1_RTS# 11
CF_UART1_CTS# 12
TEP_UART1_RTS# 11
PHY_UART_RTS#
MPC_UART1_RTS# 4
R354 4.7K

EN#	IN2	IN1	D to S
0	0	0	D=S1
0	0	1	D=S2
0	1	0	D=S3
0	1	1	D=S4
1	X	X	OFF

UCC5 & UCC7 - RS485

11 MPC_HDLC1_TCK
2,11 MPC_HDLC1_TXD_BOOT_CFG0
11 MPC_HDLC1_CD#
11 MPC_HDLC1_RXD
11 MPC_HDLC1_CTS#
2,11 MPC_HDLC1_RTS#_BOOT_CFG1
RS485_1_DTR 11
RS485_1_TXD 2,11
RS485_1_CD 11
RS485_1_RXD 11
RS485_1_CTS 11
RS485_1_RTS# 2,11
R254 4.7K

U16 M74VHC1G125DFT1G
RS485_1_RE# 11 RS485_1_RXD RS485_1_DTR 11
C300 100nF

U70 MC74VHC1G02DFT2G
4 LED3/RS485_CD_SEL1
2,11 RS485_1_RTS#
C257 100nF
U14 M74VHC1G125DFT1G
RS485_1_RE#
C262 100nF R114 10K
RS485_1_CD 11

VISO1
R358 2K C303 10nF
U50 MC74VHC1G00DFT2G
U49 PS2801-1 Emitter Anode Cathode Collector GND1
R380 760
BUS1_RTS
11 RS485_1_RXD
RS485_1_RE#
RS485_1_DE
RS485_1_TXD
2,11 RS485_1_TXD
RS485_1_RTS#
U47 MC74VHC1G00DFT2G
U54 MC74VHC1G08DFT2G
U55 MC74VHC1G00DFT2G
4 RS485_EN1
RS485_1_DE
RS485_1_RE#
C306 100nF C308 100nF C313 100nF

+3.3V
C228 C229 C230 C213 100nF 100nF 10nF 10uF0603
C288 C289 C233 C292 100nF 100nF 10nF 10uF0603
GND1
R356 2K
R357 1K
U31 ADM2582E
DGND1 VDD1 DGND2 RXD RE# DE TXD VDD2 DGND3 DGND4 GND1 VISO_IN A B GND2 Z GND3 Y VISO_OUT GND4
BUS1+ BUS1-
J21 RA Header 2x3 2.54mm
BUS1+ GND1 BUS1_RTS BUS1-

11 MPC_HDLC2_TCK
2,11 MPC_HDLC2_TXD_BOOT_CFG2
11 MPC_HDLC2_CD#
11 MPC_HDLC2_RXD
11 MPC_HDLC2_CTS#
2,11 MPC_HDLC2_RTS#_BOOT_CFG3
RS485_2_DTR 11
RS485_2_TXD 2,11
RS485_2_CD 11
RS485_2_RXD 11
RS485_2_CTS 11
RS485_2_RTS# 2,11
R253 4.7K

U20 M74VHC1G125DFT1G
RS485_2_RE# 11 RS485_2_RXD RS485_2_DTR 11
C302 100nF

U71 MC74VHC1G02DFT2G
4 LED7/RS485_CD_SEL2
2,11 RS485_2_RTS#
C258 100nF
U15 M74VHC1G125DFT1G
RS485_2_RE#
C299 100nF R115 10K
RS485_2_CD 11

VISO2
R374 2K C304 10nF
U51 MC74VHC1G00DFT2G
U52 PS2801-1 Emitter Anode Cathode Collector GND2
R381 760
BUS2_RTS
11 RS485_2_RXD
RS485_2_RE#
RS485_2_DE
RS485_2_TXD
2,11 RS485_2_TXD
RS485_2_RTS#
U48 MC74VHC1G00DFT2G
U57 MC74VHC1G08DFT2G
U56 MC74VHC1G00DFT2G
4 RS485_EN2
RS485_2_DE
RS485_2_RE#
C323 100nF C319 100nF C321 100nF

+3.3V
C231 C232 C290 C291 100nF 100nF 10nF 10uF0603
C294 C295 C293 C296 100nF 100nF 10nF 10uF0603
GND2
R359 2K
R360 1K
U33 ADM2582E
DGND1 VDD1 DGND2 RXD RE# DE TXD VDD2 DGND3 DGND4 GND1 VISO_IN A B GND2 Z GND3 Y VISO_OUT GND4
BUS2+ BUS2-
J20 RA Header 2x3 2.54mm
BUS2+ GND2 BUS2_RTS BUS2-

Title	RS485, RS232 and RS232 MUX
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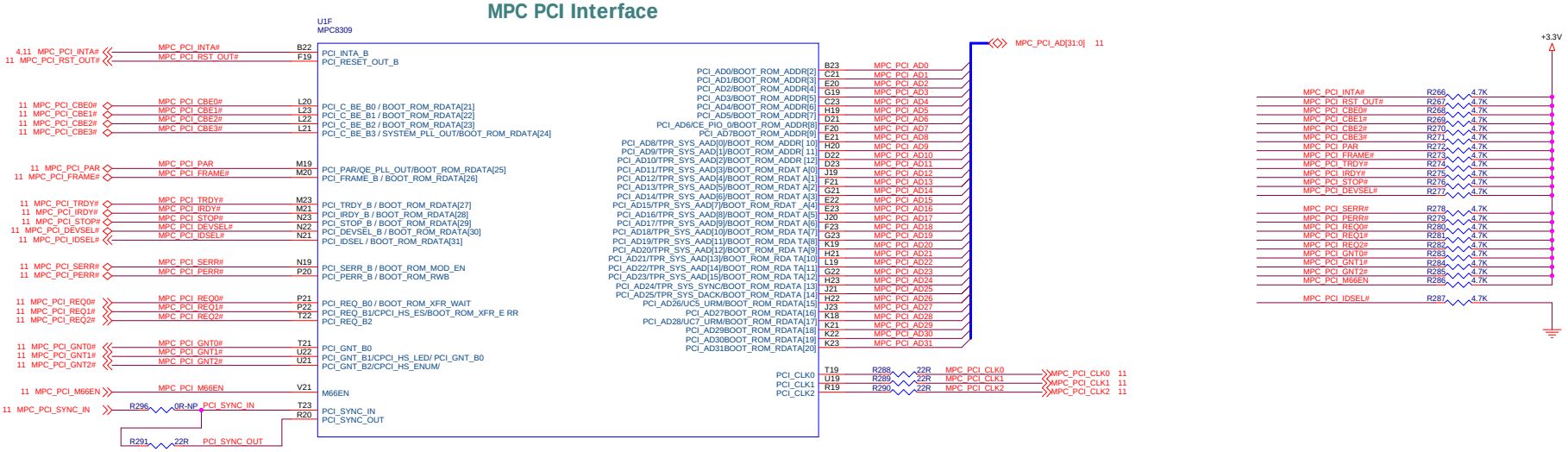
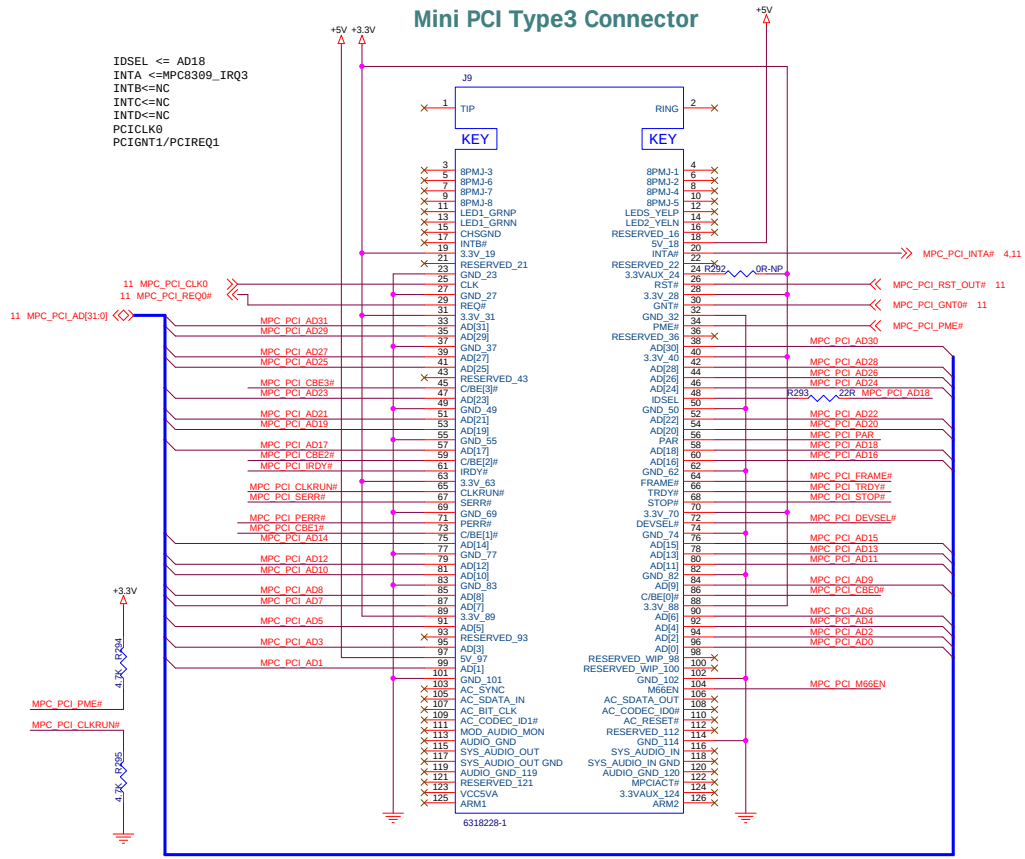
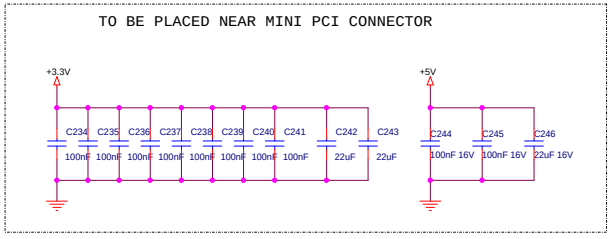
MPC PCI Interface



Mini PCI Type3 Connector





Title	PCI Interface and Mini PCI Connector		
Size	Document Number		Rev
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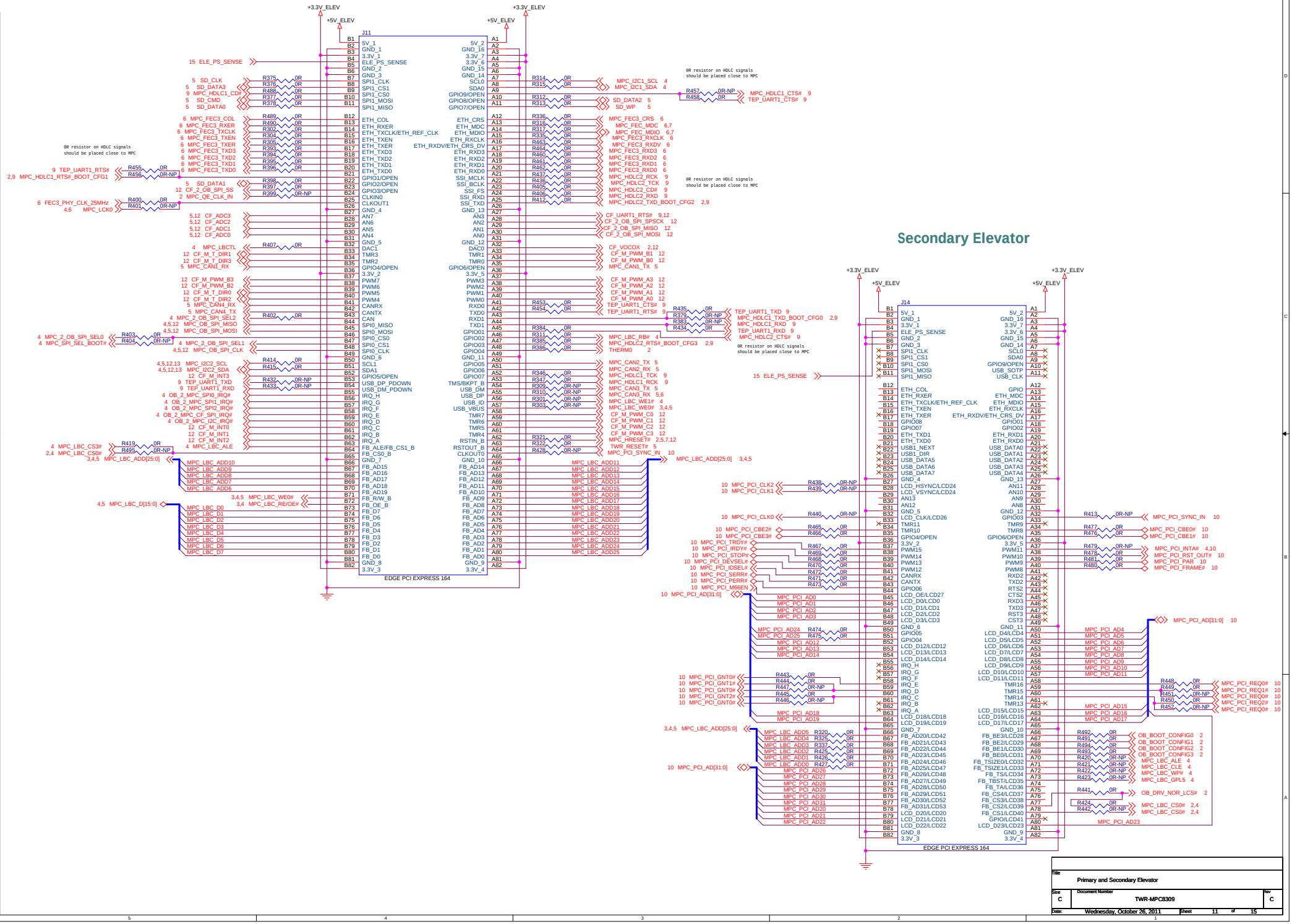
Primary Elevator
Secondary Elevator
+3.3V_ELEV
+5V_ELEV
J11
J14
EDGE PCI EXPRESS 164
0R resistor on HDLC signals should be placed close to MPC
15 ELE_PS_SENSE
MPC_LBC_ADD[25:0] 3,4,5
MPC_PCI_AD[31:0] 10
Title
Primary and Secondary Elevator
Size C
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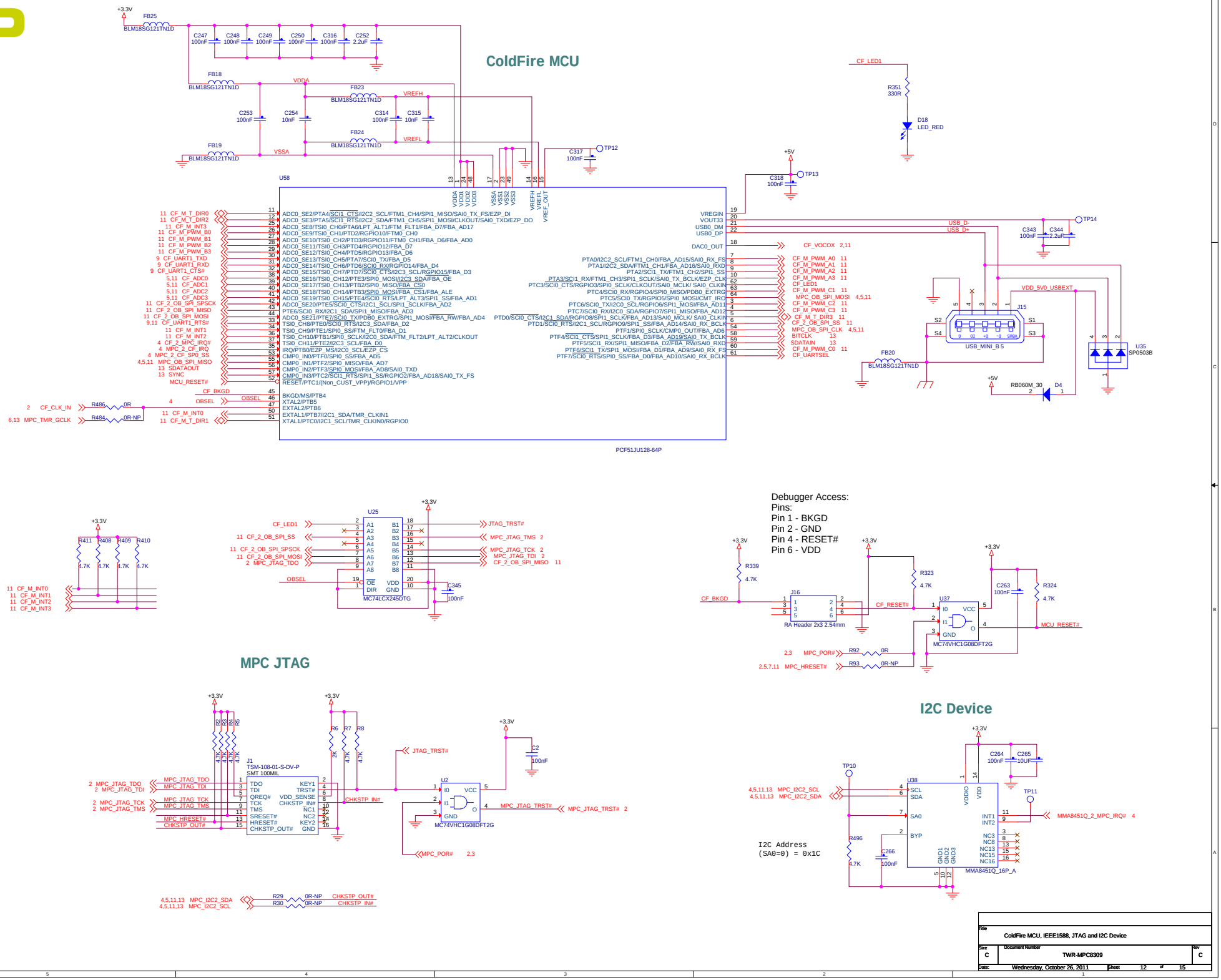
ColdFire MCU
U58
PCF51JU128-64P
MPC JTAG
I2C Device
Debugger Access:
Pins:
Pin 1 - BKGD
Pin 2 - GND
Pin 4 - RESET#
Pin 6 - VDD
I2C Address
(SA0=0) = 0x1C
ColdFire MCU, IEEE1588, JTAG and I2C Device
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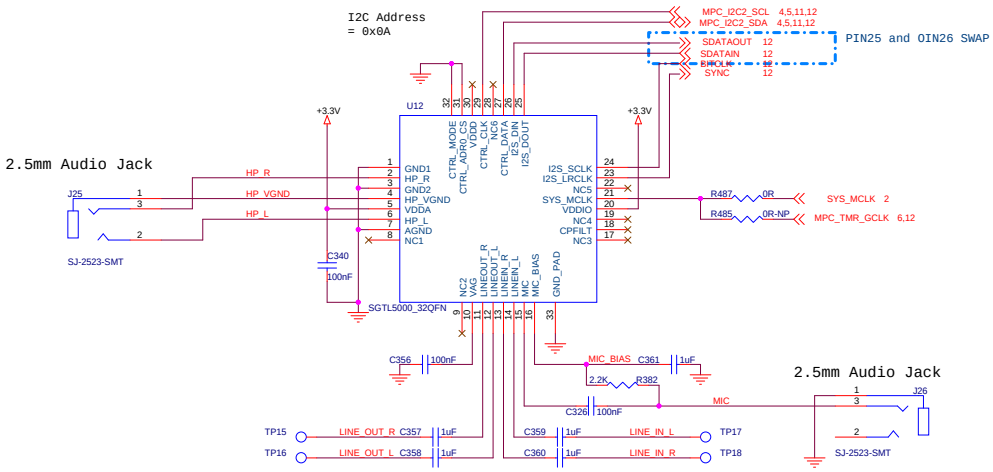
Audio CODEC



Title: Audio CODEC			
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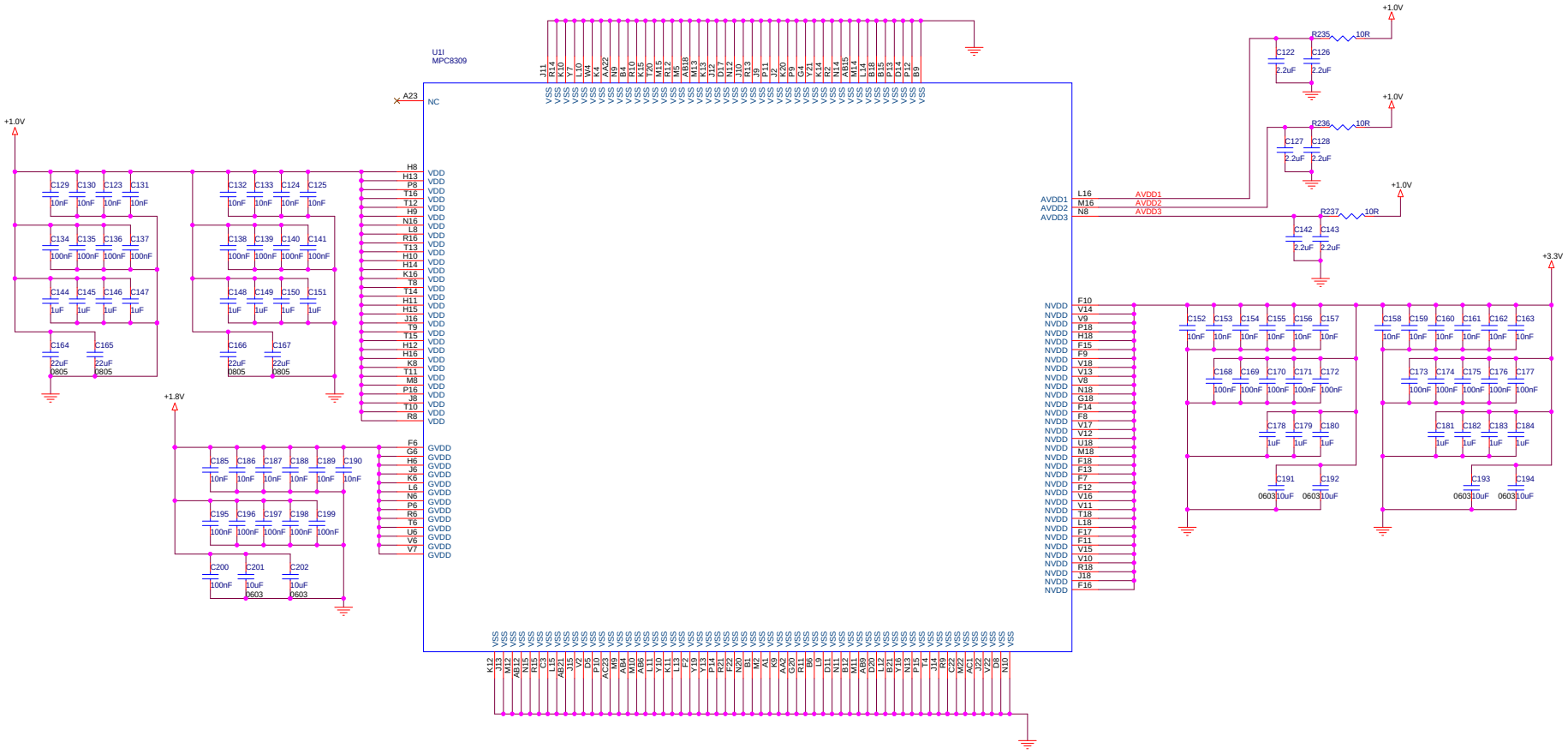
MPC Decoupling



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Size C	Document Number TWR-MPC8309		Rev C
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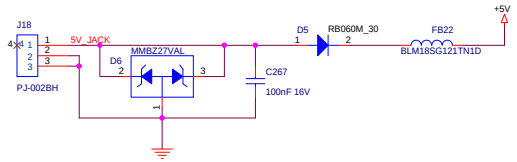
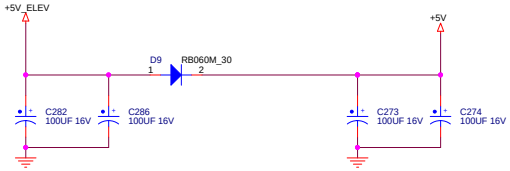
Power Supplies

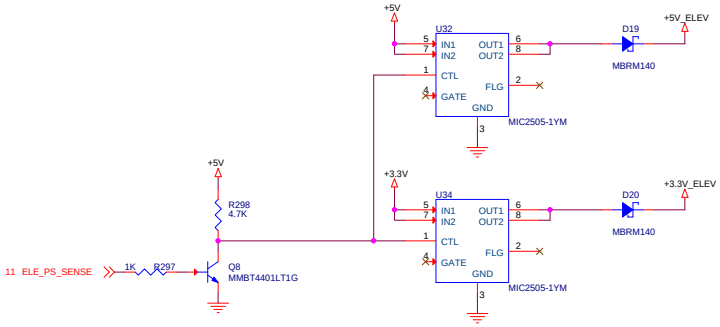
External Power Input



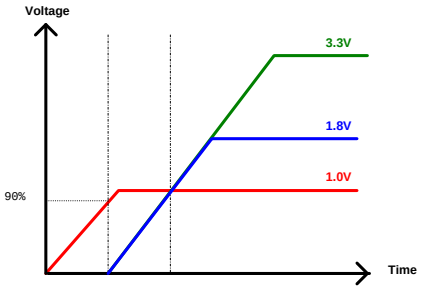
Tower Power Input



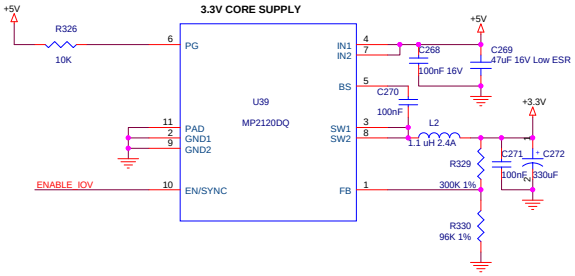

```
When ELE_PS_SENSE = 0,
Drive on board +3.3V to +3.3V_ELEV and +5V to +5V_ELEV
When ELE_PS_SENSE = 1,
Disconnect +3.3V_ELEV from on board +3.3V and +5V_ELEV from +5V
```

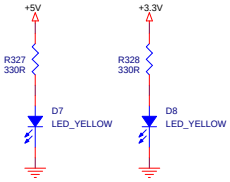


Power-up Sequence

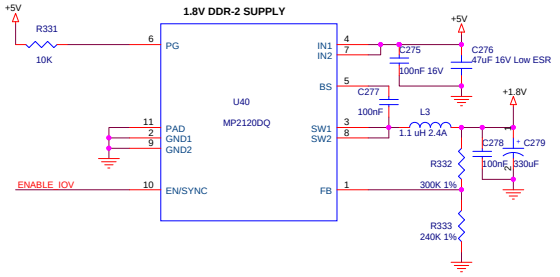


3.3V @ 2.5A POWER SUPPLY

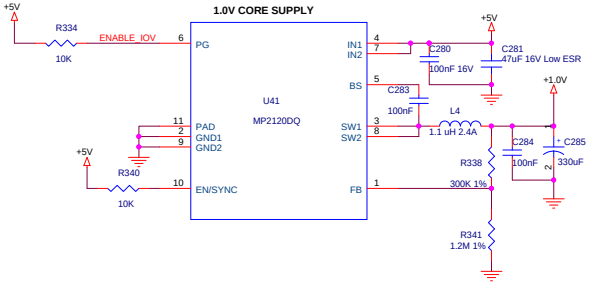




1.8V @ 2.5A POWER SUPPLY



1.0V @ 2.5A POWER SUPPLY



Title: Power Supplies			
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