Application Report
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Synchronizing DC/DC Converters in a Power Tree

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ABSTRACT

Many applications use different supply voltages for powering different functional blocks of the system. For example, state of the art microcontrollers use at least two supply rails: one to power the I/O ports, and a lower voltage to power the processor core. Those voltages are usually generated by voltage regulators, either linear regulators or DC/DC converters. If DC/DC converters are used for generating the different supply rails, the application needs to be designed in a way to minimize the switching noise distributed in the power distribution network of the system. This noise usually is minimized by adding suitable decoupling capacitors at the input of the converters. Different switching frequencies of the converters can introduce additional challenges to the system design. In this application note, five different configurations of a power tree example generating two output voltages are explained. All five circuits use the same inductors for the DC/DC converters and the same input and output capacitor configuration. In all examples, the converters are also configured to operate at the same nominal frequency of 2.25 MHz and use the same resistance value for the RCF resistors. Measurement data of supply current and supply voltage of the configurations are shown and discussed. The power tree example uses two converters of the TPS62810 family. Both converters are connected to the same supply voltage, a regulated 5-V rail. The output voltages are set to 3.3 V on converter 1, and 1.8 V on converter 2. During all measurements, a 2-A load is connected at the output of each of the converters.

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Trademarks

1 Different Strategies for Synchronization

The TPS62810 devices support multiple features to control the switching frequency. The switching frequency can be defined by connecting a suitable resistor between COMP/FSET and GND. With the signal connected to MODE/SYNC, the devices are configured for how to use this preset switching frequency. Schematics shown in the following sections only show what is relevant for the specific configuration. See the *TPS6281x-Q1 2.75-V to 6-V Adjustable-Frequency Step-Down Converter Data Sheet*, or the *TPS62810EVM-015 Evaluation Module User's Guide* for more details.

1.1 No Synchronization

The first example shows the most common method of configuring DC/DC converters in a power tree. The MODE/SYNC pin is tied to GND which sets the TPS62810 device in the most flexible and autonomous mode of operation. At high-load currents, the converters operate at the switching frequency defined by the resistors connected to the COMP/FSET pins. In this example, RCF1 and RCF2 have the same value, setting the two converters to the same nominal switching frequency. At light load, this MODE/SYNC setting allows the converters to reduce the switching frequency for maintaining high-power conversion efficiency. Figure 1 shows a simplified schematic of this configuration.

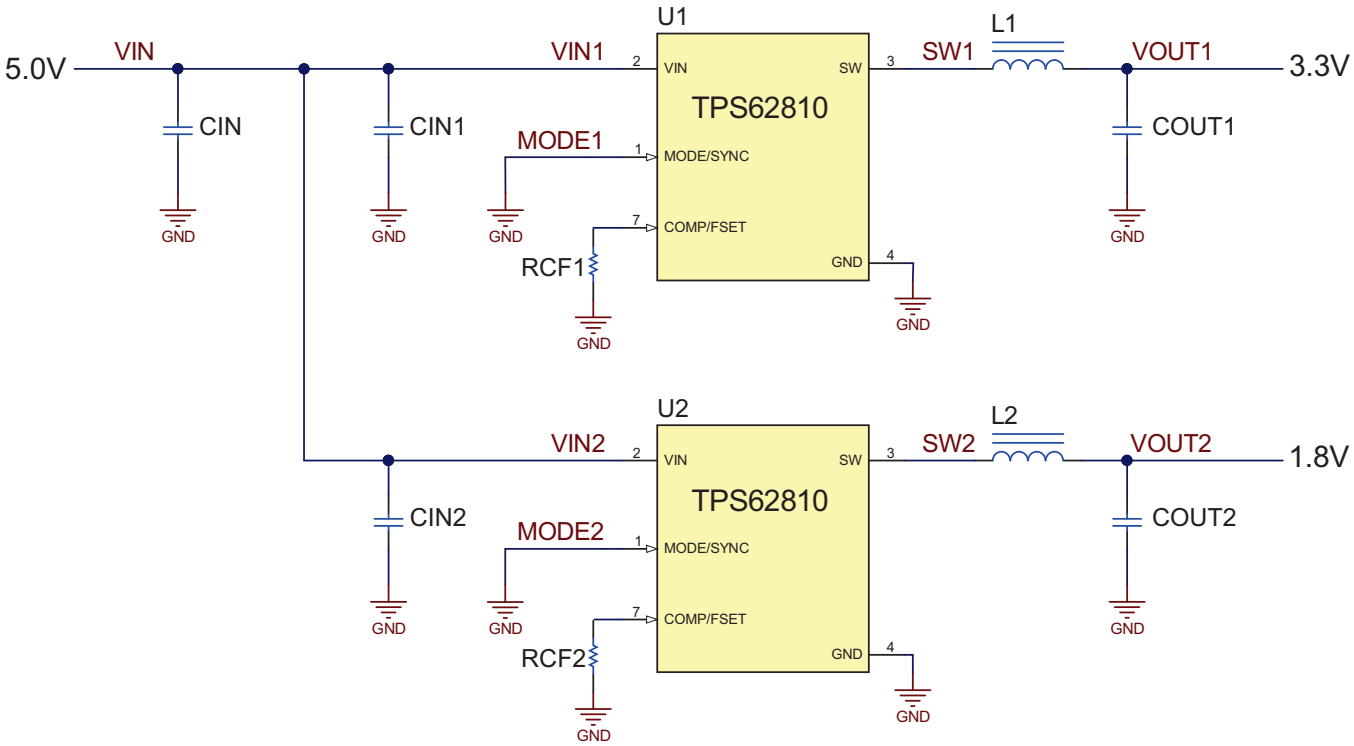

Figure 1. Simplified Schematic — No Synchronization

Figure 2 shows the measured switch-node voltages for this configuration. The measurement is done with limited bandwidth to better show the relation between the operating frequencies of the different converters. This makes the switching edges appear much slower than they really are. Since the trigger is set to the switch-node voltage of converter 1, the waveform of this switch-node voltage is clearly shown. The persistence setting makes the waveform of switch-node 2 appear blurry, indicating that the switching frequency is not the same as the switching frequency of converter 1. Due to the different output voltage setting, the on time of the high-side switches is different.

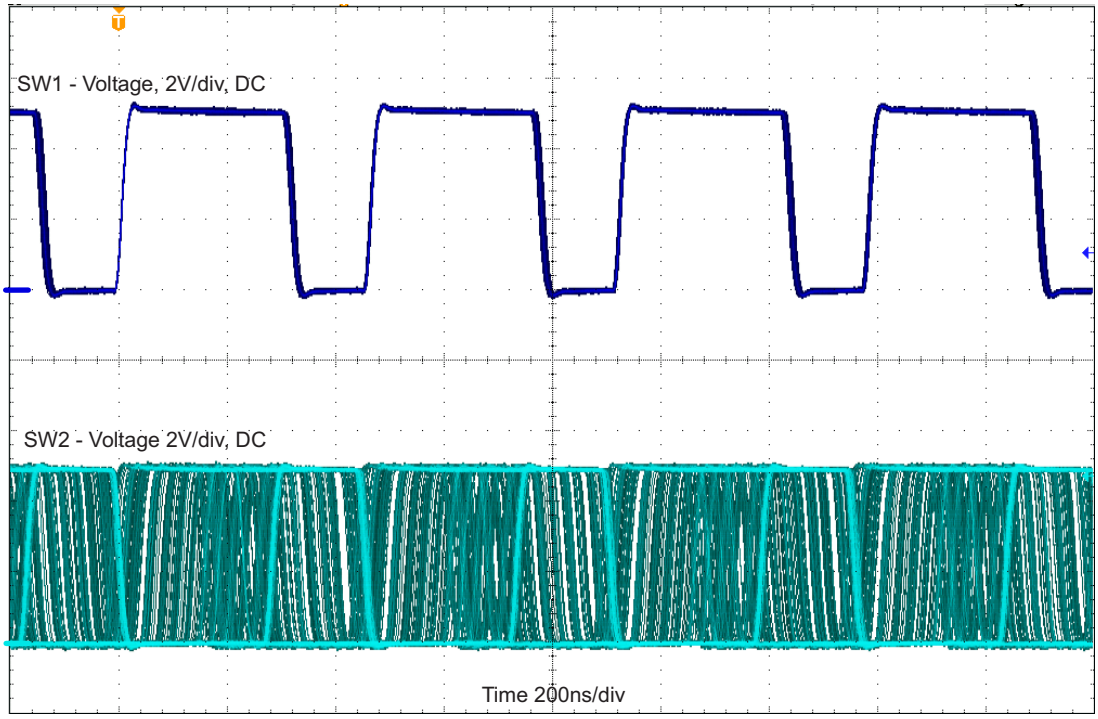

Figure 2. Switch-Node Voltages — No Synchronization

Figure 3 shows the current waveforms. The inductor current waveforms for L1 and L2 show the similar switching frequency. Due to the different output voltages, the inductor current ripple is different. At the input current waveform, a lower frequency is superimposed to the high-frequency ripple caused by the operating frequency of both converters. It basically shows the beat frequency, which is the difference between the switching frequency of converter 1 and converter 2, in the range of 40 kHz in this case.

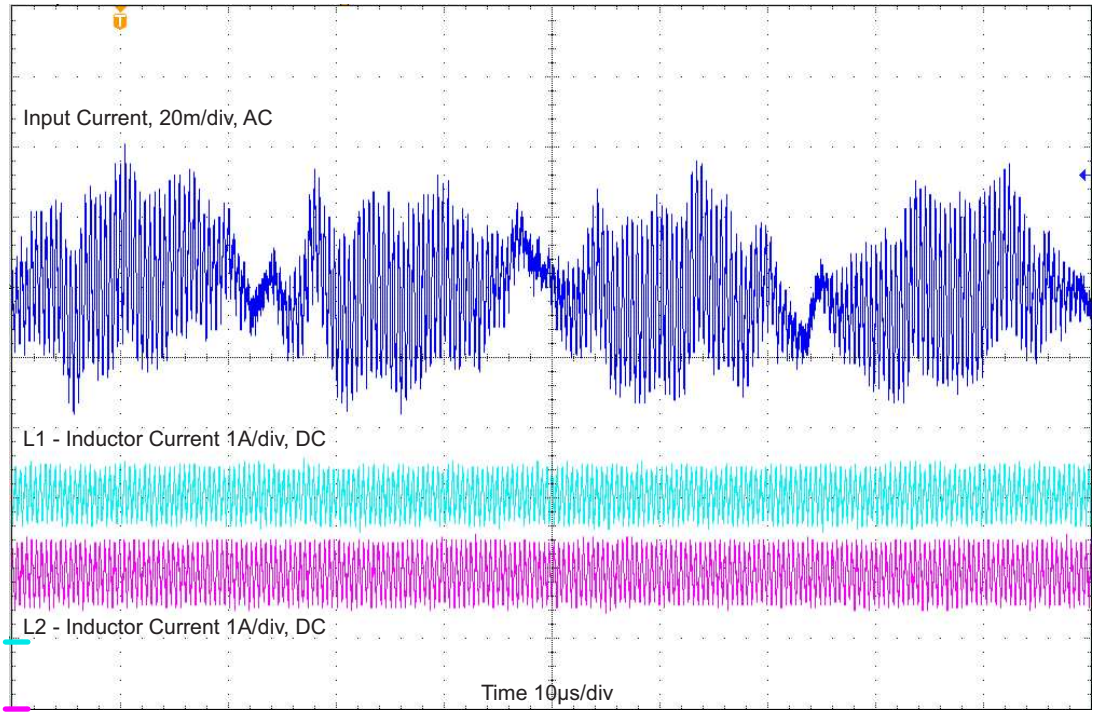

Figure 3. Current Waveforms — No Synchronization

In the spectrum of the input voltage shown in Figure 4, the switching frequency is dominant. Since the 40-kHz difference of the switching frequencies of the two converters is less than the resolution bandwidth of 50 kHz, the converters cannot be distinguished at the base frequency. The frequency difference of the harmonics of the switching frequency of the different converters is higher than the resolution bandwidth, so it is visible in this measurement. The measurement with a wider resolution bandwidth shows higher peak values compared to the narrower resolution bandwidth measurement. This indicates that there is varying ripple on the input voltage, which is not properly captured in the narrow bandwidth measurement.

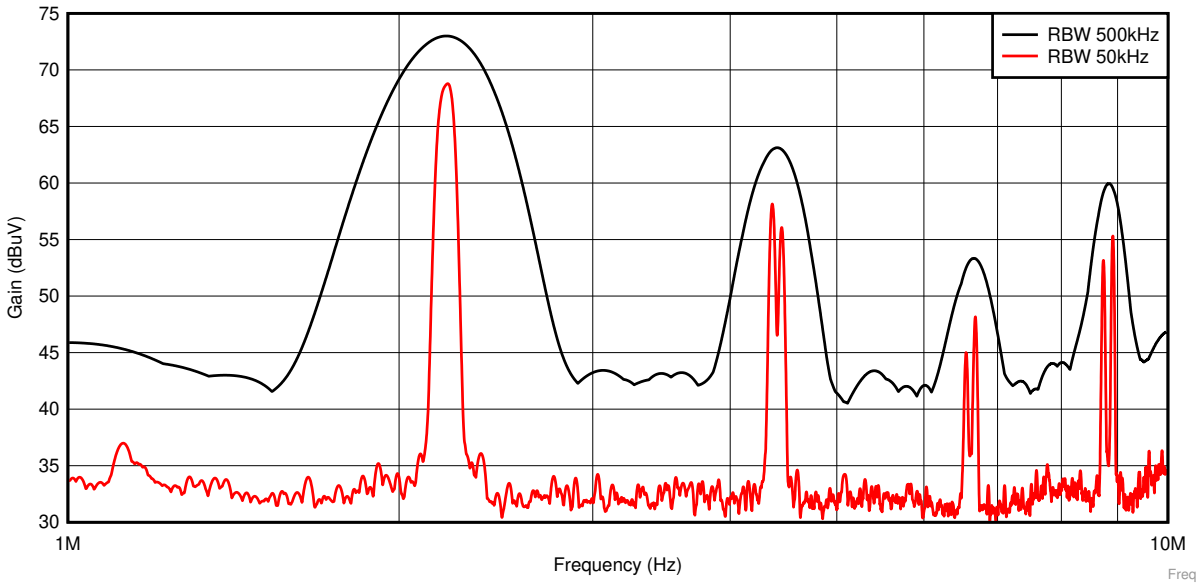

Figure 4. Input Voltage Spectrum — No Synchronization

1.2 Synchronization to an External Clock

The second example shows a simple way of synchronizing DC/DC converters in a power tree to an external clock. The clock signal is directly connected to the MODE/SYNC pin. In this configuration, the switching frequency of the converters is always synchronous to the frequency of the external clock if the clock signal is in the allowed range. This does not change at light load conditions. This means power conversion efficiency at light load operation becomes worse than without synchronization. Figure 5 shows a simplified schematic of this configuration.

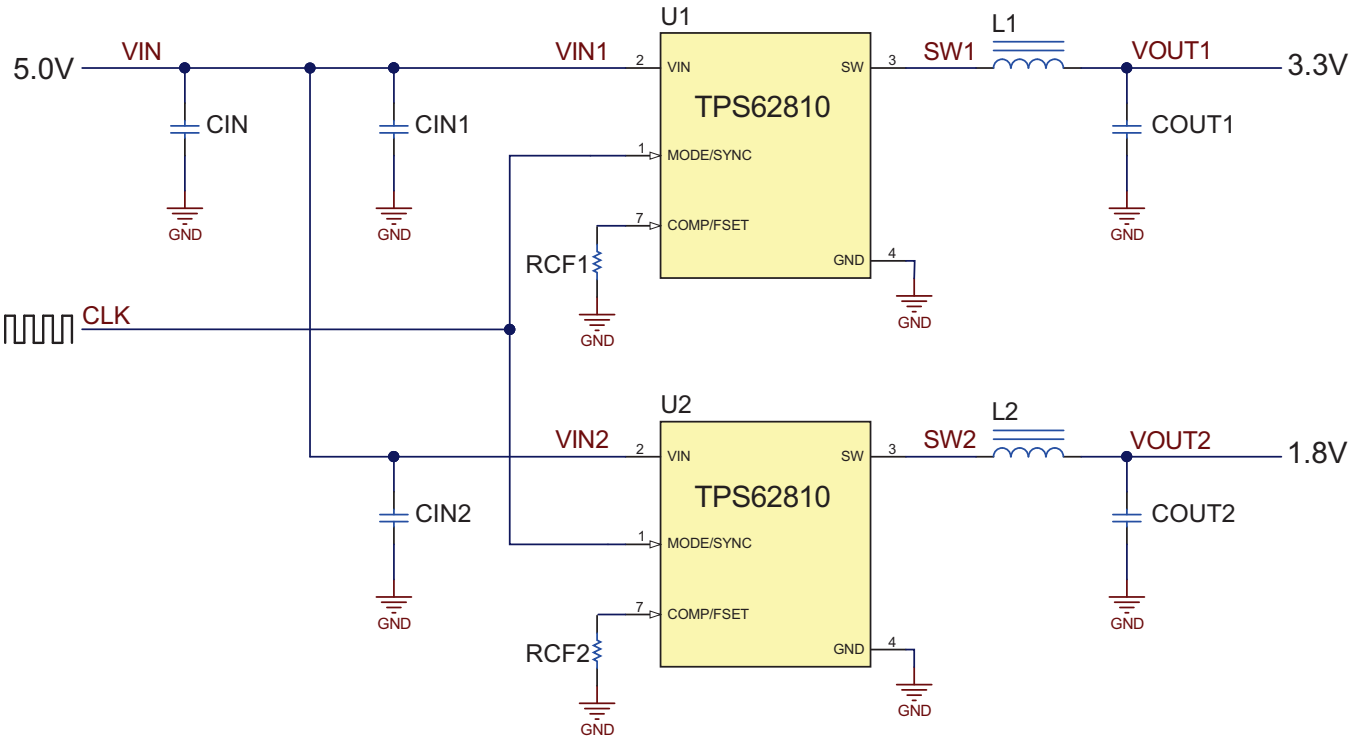

Figure 5. Simplified Schematic — Synchronization to an External Clock

Figure 6 shows the measured switch-node voltages for this configuration. The measurement has been done with limited bandwidth to better show the relation between the operating frequencies of the different converters. This makes the switching edges appear much slower than they really are. Since the trigger is set to the switch-node voltage of converter 1, the waveform of this switch-node voltage is clearly shown. Due to the synchronization, the switch-node voltage of converter 2 is clearly shown as well. No persistence setting is needed to show the complete information. Both converters operate at the same frequency, turning on their high-side switches at the same time. Due to the different output voltage, setting the on time of the high-side switches is different.

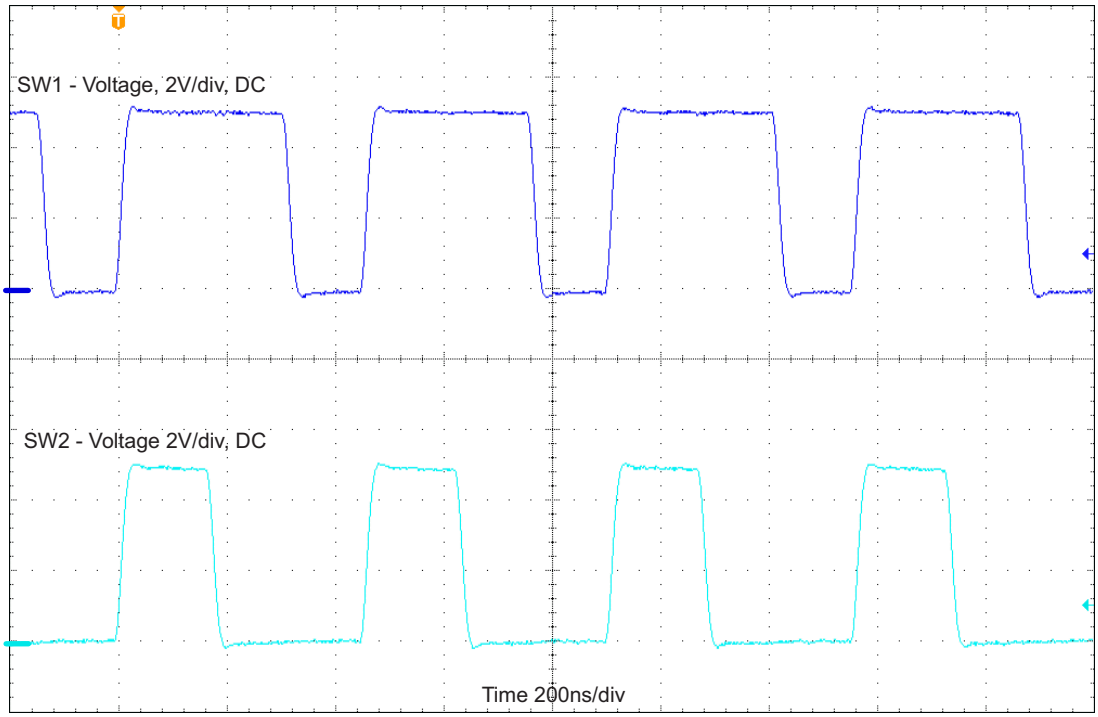

Figure 6. Switch-Node Voltages — Synchronization to an External Clock

Figure 7 shows the current waveforms measured in this configuration. The inductor current waveforms are basically not different compared to the previous example. The frequency is forced to be the same though. This is also clearly visible on the input current waveform. The dominant frequency is the switching frequency. Since the chosen method for synchronizing the converters forces the high-side switches to turn on at the same time, both converters pull current from the input at the same time, which causes higher input current and input voltage ripple at the switching frequency.

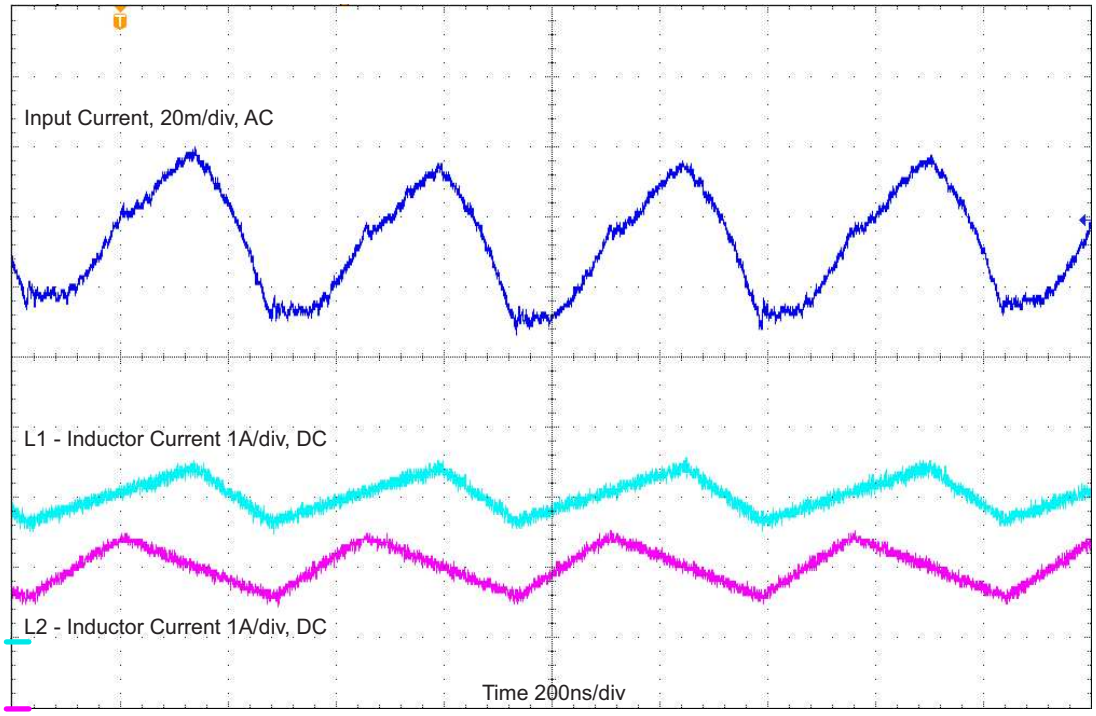

Figure 7. Current Waveforms — Synchronization to an External Clock

The spectrum of the input voltage shown in Figure 8 shows the synchronization. There is no different frequency visible in the base frequency and in the harmonics. Wide and narrow bandwidth settings show very similar peak values, so the ripple is properly captured with both settings.

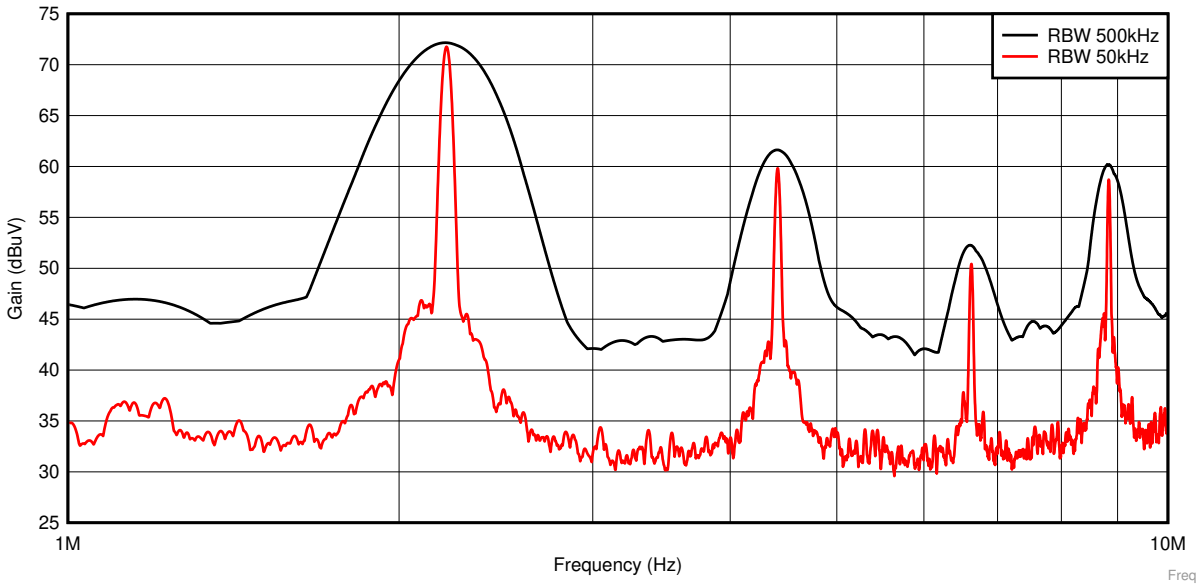

Figure 8. Input Voltage Spectrum — Synchronization to an External Clock

1.3 Phase Shifted Synchronization

The third example shows a more complex way of synchronizing DC/DC converters in a power tree to an external clock. Both converters get a separate clock signal having the same frequency. The separate clock signals are 180° out of phase or inverted to each other. The clock signals are directly connected to the respective MODE/SYNC pin. In this configuration, the converters always work as well at the switching frequency defined by the frequency of the external clock, so there is no change at light-load conditions. This means power conversion efficiency at light-load operation is also worse than without synchronization. Figure 9 shows a simplified schematic of this configuration.

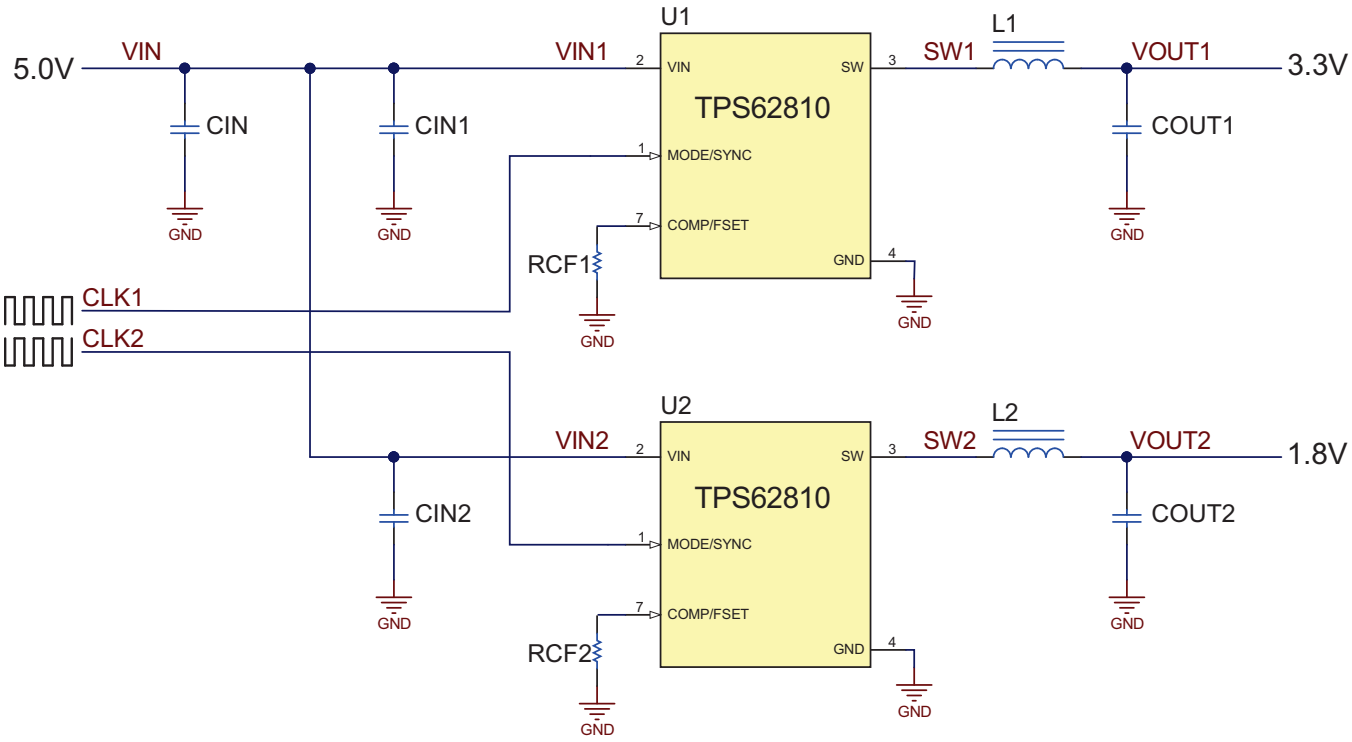

Figure 9. Simplified Schematic — Phase-Shifted Synchronization

Figure 10 shows the measured switch-node voltages for this configuration. The measurement is done with limited bandwidth to better show the relation between the operating frequencies of the different converters. This makes the switching edges appear much slower than they really are. The trigger is set to the switch-node voltage of converter 1, so the waveform of this switch-node voltage is clearly shown. Due to the synchronization, the switch-node voltage of converter 2 is clearly shown as well. No persistence setting is needed to show the complete information. Both converters operate at the same frequency. The 180° phase shift of the clock signal for converter 2 causes converter 2 to turn on the high-side switch with a delay of about 200 ns compared to converter 1. Due to the different output voltage, setting the on time of the high-side switches is different.

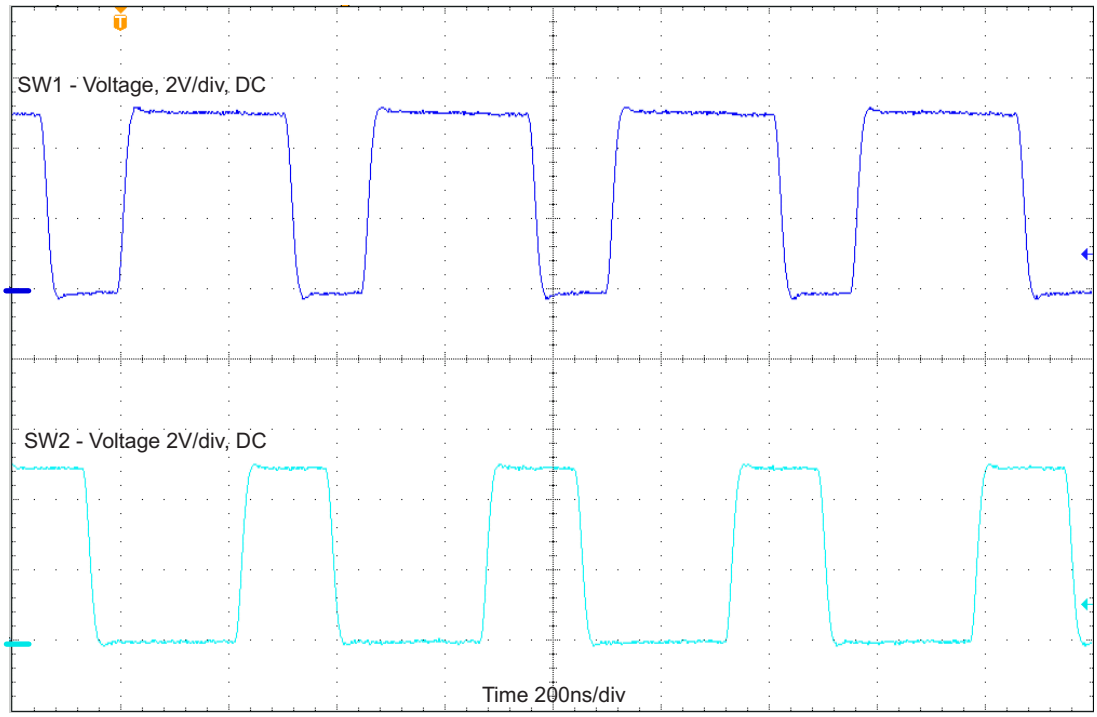

Figure 10. Switch-Node Voltages — Phase-Shifted Synchronization

Figure 11 shows the current waveforms. The inductor current waveforms show the same ripple as in the previous examples. Due to the synchronization, the switching frequency is the same. Compared to the previous example, the inductor current waveforms are phase shifted by 180°. This causes the input current ripple to get lower. Due to the high duty cycle of converter 1 and the low duty cycle of converter 2, the switching frequency is still dominant at the input current waveform.

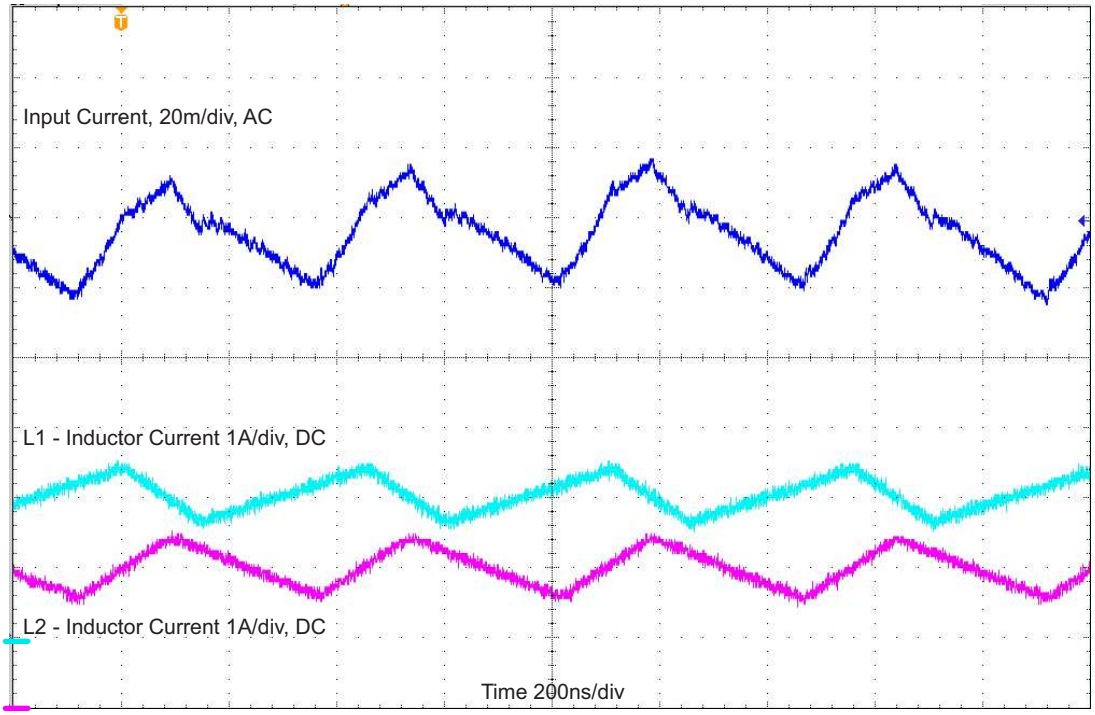

Figure 11. Current Waveforms — Phase-Shifted Synchronization

The spectrum of the input voltage shown in Figure 12 shows the synchronization. There is no different frequency visible in the base frequency, and in the harmonics. Wide and narrow bandwidth settings show very similar peak values, so the ripple is properly captured with both settings. Since input current ripple is lower, the input voltage ripple gets lower as well.

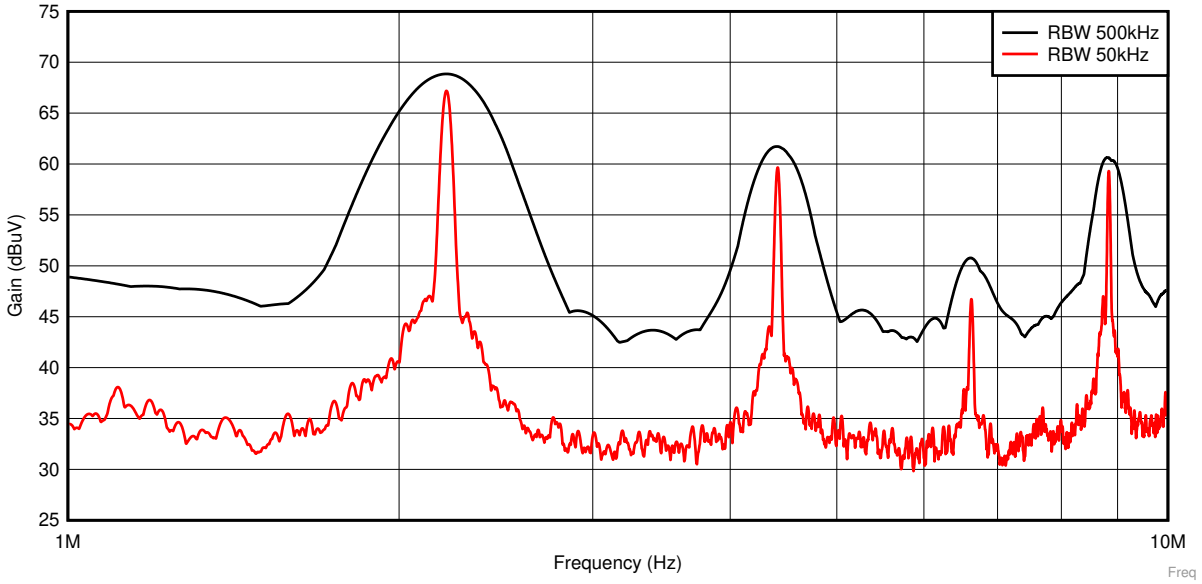

Figure 12. Input Voltage Spectrum — Phase-Shifted Synchronization

1.4 Synchronization to the Other DC/DC Converter

The fourth example shows a method of synchronizing DC/DC converters in a power tree without using an external clock. Converter 2 gets the synchronization clock signal directly from converter 1. The switch node voltage is a rectangular waveform, which can be used as a clock signal. TPS62810 synchronization is designed in a way that the switching is out of phase. This means when the high-side switch of converter 1 (which provides the clock signal) is turned off, the high-side switch of converter 2 is turned on. The switch node voltage of converter 1 is filtered by a simple R-C filter and directly connected to the MODE/SYNC pin of converter 2. If converter 1 operates at light load, it reduces switching frequency. To avoid that, the clock reference for converter 2 moves below the specified synchronization range. Converter 1 must always have enough load current, or it must be operated in forced PWM mode, connecting MODE1 to VIN1. Figure 13 shows a simplified schematic of this configuration.

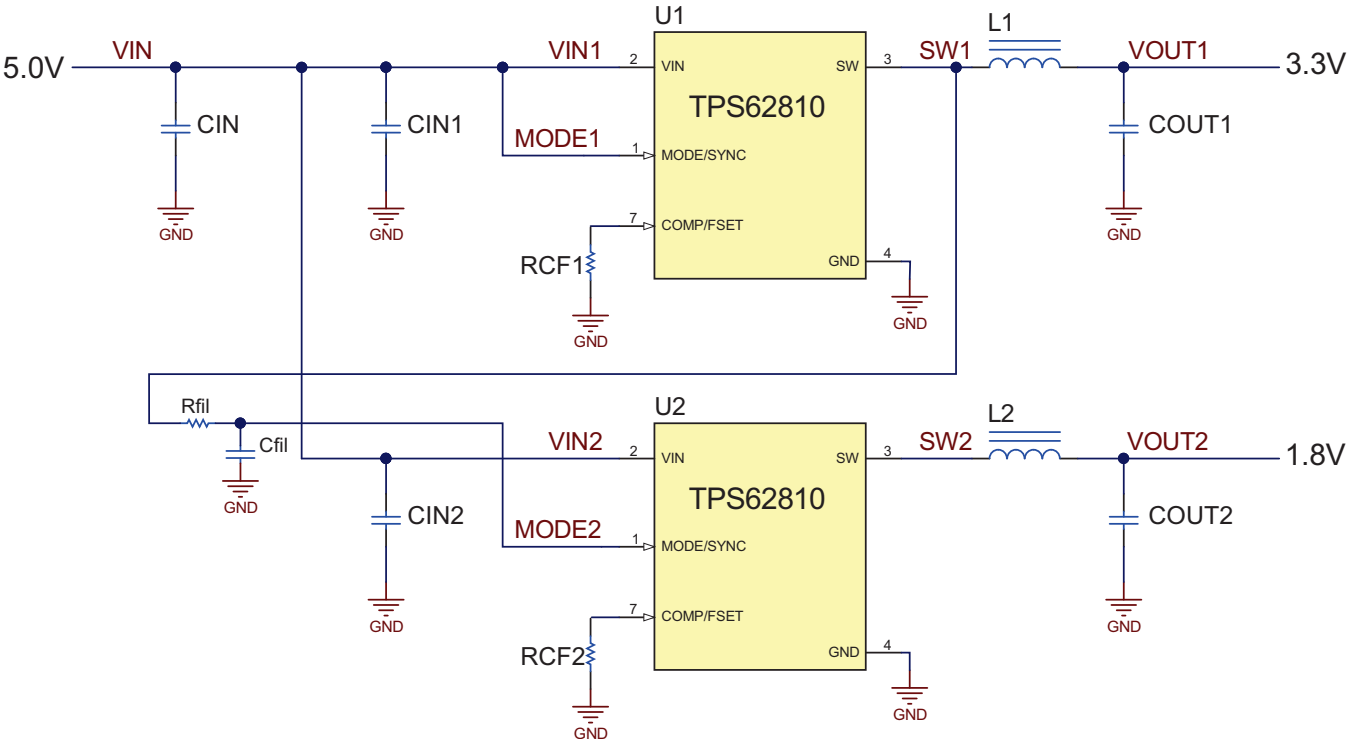

Figure 13. Simplified Schematic — Synchronization to the Other DC/DC Converter

Figure 14 shows the measured switch-node voltages for this configuration. The measurement is done with limited bandwidth to better show the relation between the operating frequencies of the different converters. This makes the switching edges appear much slower than they really are. The trigger is set to the switch-node voltage of converter 1, so the waveform of this switch-node voltage is clearly shown. Due to the synchronization, the switch-node voltage of converter 2 is clearly shown as well. No persistence setting is needed to show the complete information. Both converters operate at the same frequency. The synchronization of converter 2 to converter 1 causes converter 2 to turn on the high-side switch at the time converter 1 turns off the high-side switch. Due to the different output voltage, setting the on time of the high side switches is different.

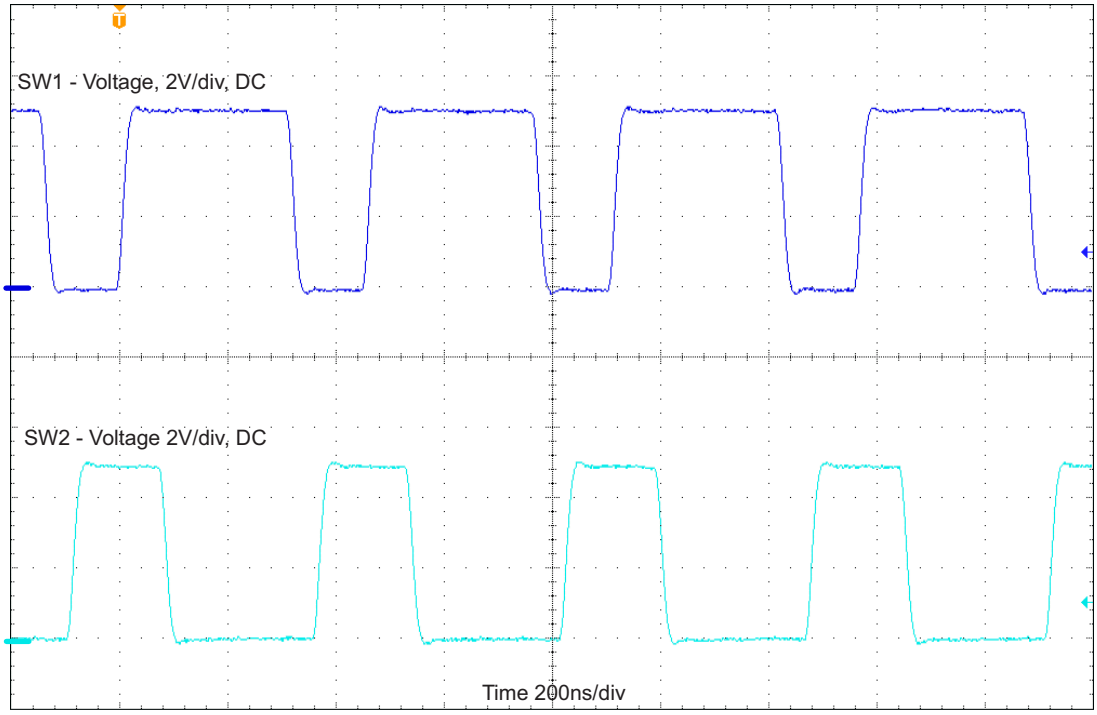

Figure 14. Switch-Node Voltages — Synchronization to the Other DC/DC Converter

Figure 15 shows the current waveforms. The inductor current waveforms show the synchronization. Since the turn on of the high-side switch of converter 2 is synchronized to the turn off of the high-side switch of converter 1, the peak current drawn from the input is minimized causing the lowest input current ripple.

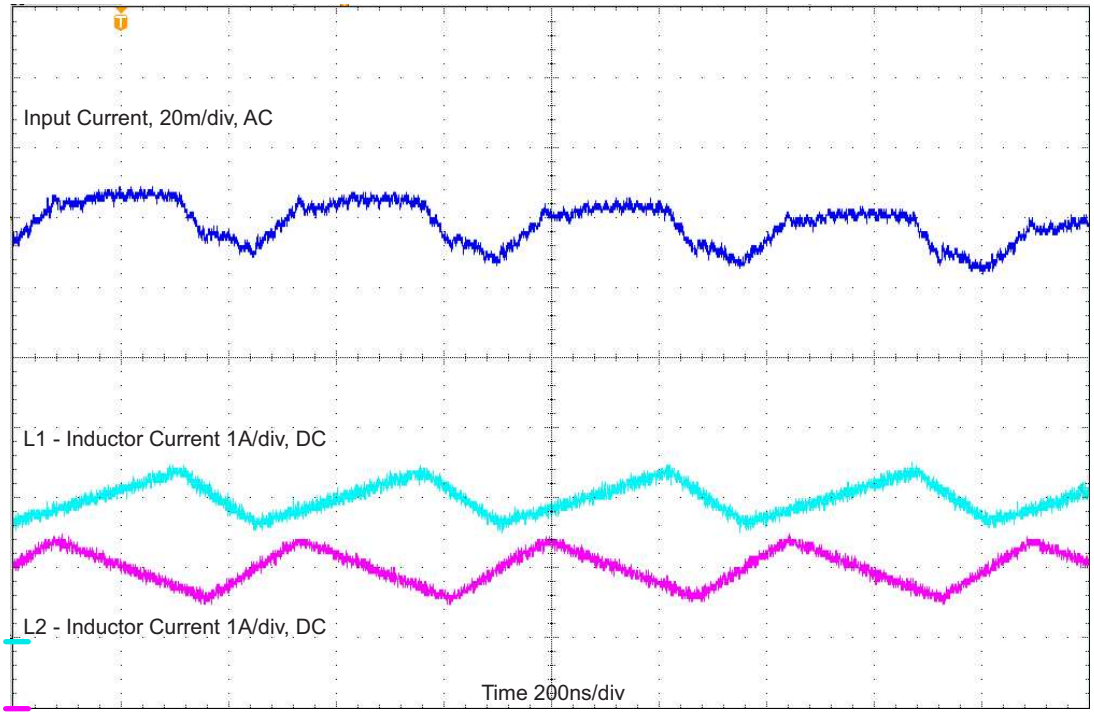

Figure 15. Current Waveforms — Synchronization to the Other DC/DC Converter

The spectrum of the input voltage shown in Figure 16 shows the synchronization. There is no different frequency visible in the base frequency and in the harmonics. Wide and narrow bandwidth settings show very similar peak values, so the ripple is properly captured with both settings. The input current ripple is lowest in this configuration, so the peak at the switching frequency is lowest as well. The synchronization to the other converter is causing slightly higher current ripple at twice the switching frequency, so the peak value at the second harmonic is increasing.

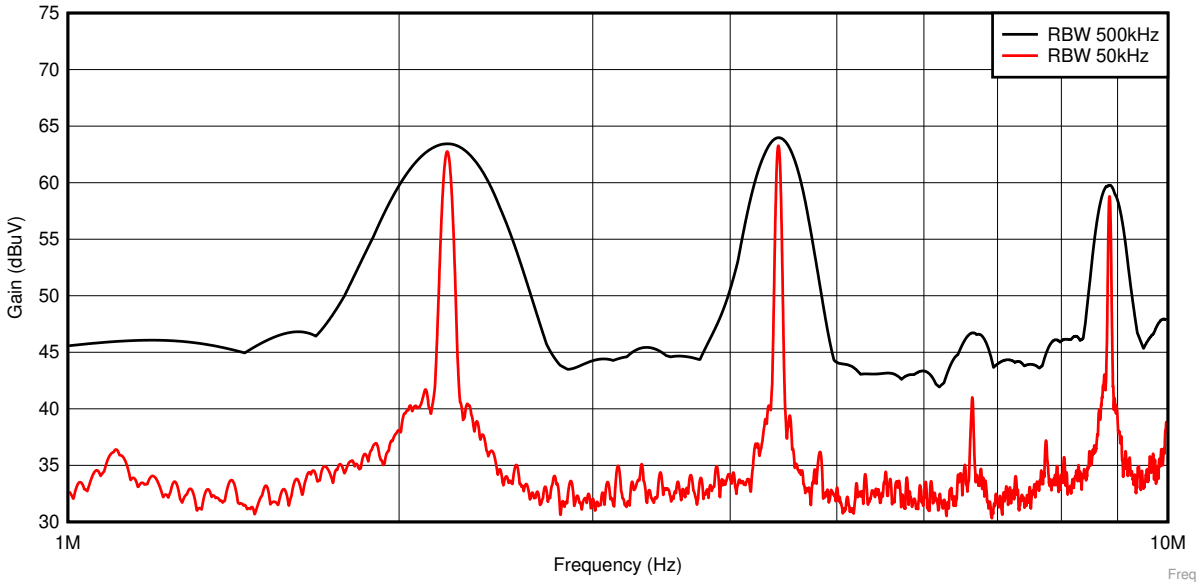

Figure 16. Input Voltage Spectrum — Synchronization to the Other DC/DC Converter

1.5 Spread Spectrum Operation

The fifth example is similar to the first example. It just uses TPS62810 versions with a spread spectrum oscillator. This means there is a significant variation of the switching frequency of both converters, and the difference of the frequencies varies as well. Both converters operate autonomously as they do in the first example. At light load, the MODE/SYNC setting allows the converters to reduce the switching frequency for maintaining high-power conversion efficiency. Figure 17 shows a simplified schematic of this configuration.

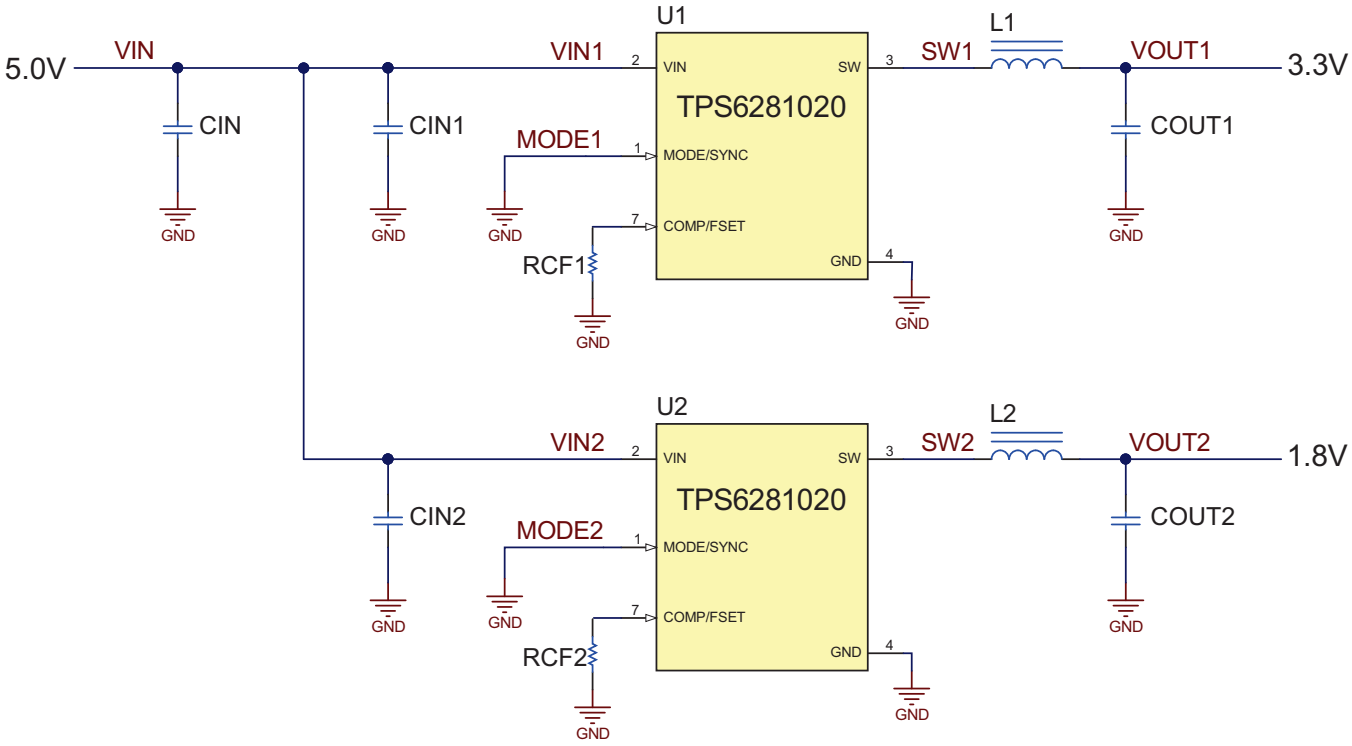

Figure 17. Simplified Schematic — Spread Spectrum Operation

Figure 17 shows the measured switch-node voltages for this configuration. The measurement is done with limited bandwidth to better show the relation between the operating frequencies of the different converters. This makes the switching edges appear much slower than they really are. The trigger is set to the switch-node voltage of converter 1. The persistence setting helps to show the change in frequency. Compared to the configuration shown in Section 1.1, the waveform of this switch-node voltage is getting blurry due to spread-spectrum operation. The persistence setting makes the waveform of switch-node 2 appear blurry as well. Its frequency is different from the frequency of the switch-node voltage of converter 1 and it is changing as well due to spread-spectrum operation. Due to the different output voltage setting the on time of the high-side switches is different.

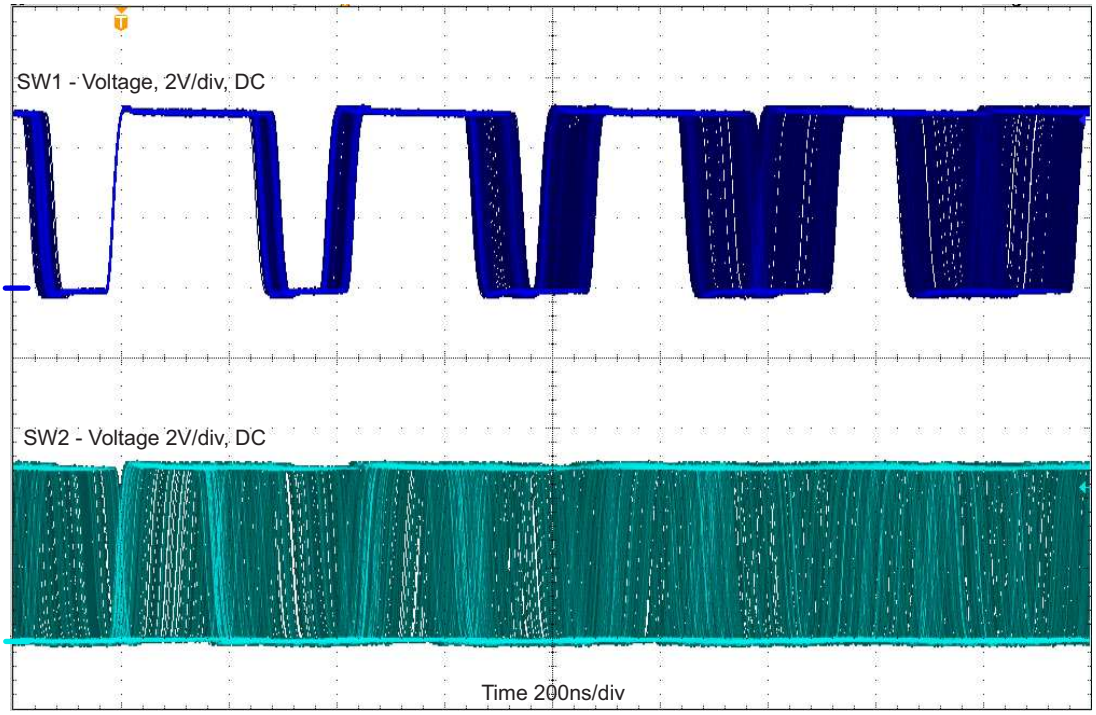

Figure 18. Switch-Node Voltages — Spread-Spectrum Operation

The current waveforms of the spread-spectrum configuration shown in Figure 19 look similar to the current waveforms of the no synchronization configuration. The difference is mainly visible in the input current waveform. There is no beat frequency but peak currents are at a similar magnitude.

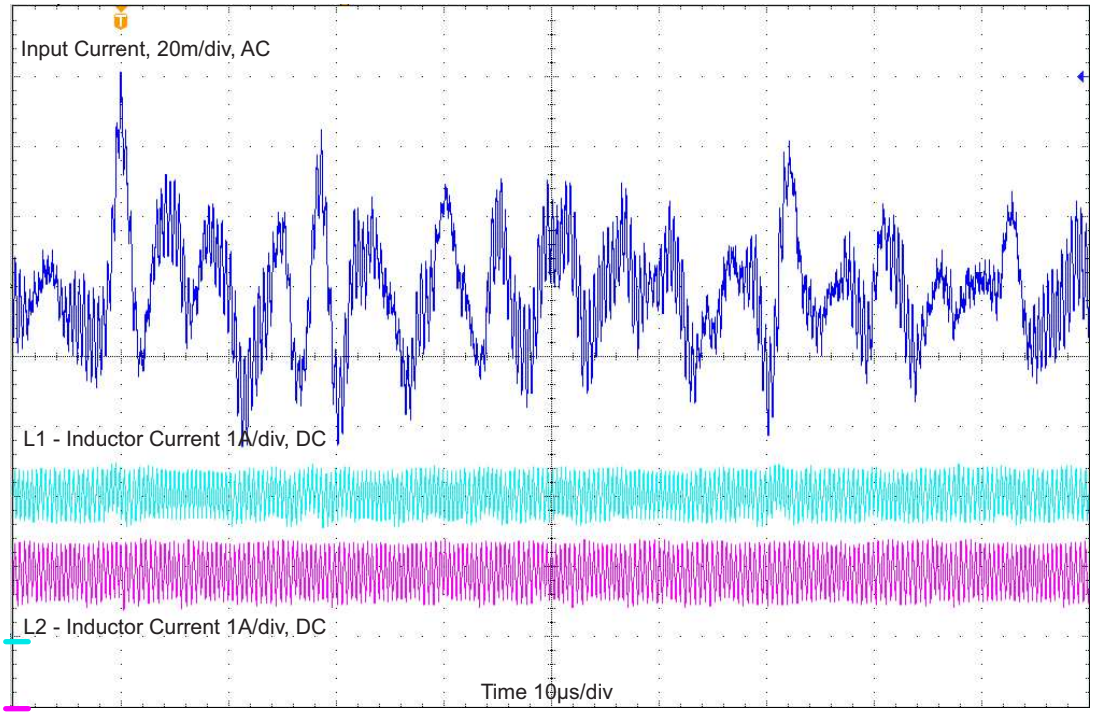

Figure 19. Current Waveforms — Spread-Spectrum Operation

Although both converters operate with spread spectrum in the spectrum of the input voltage shown in Figure 20 the region of the switching frequency is still dominant. The difference of the switching frequencies cannot be distinguished anymore. The peak hold measurement with a wider resolution bandwidth shows higher peak values compared to the narrower resolution bandwidth measurement. This indicates that there is varying ripple on the input voltage which is not properly captured in the narrow bandwidth measurement.

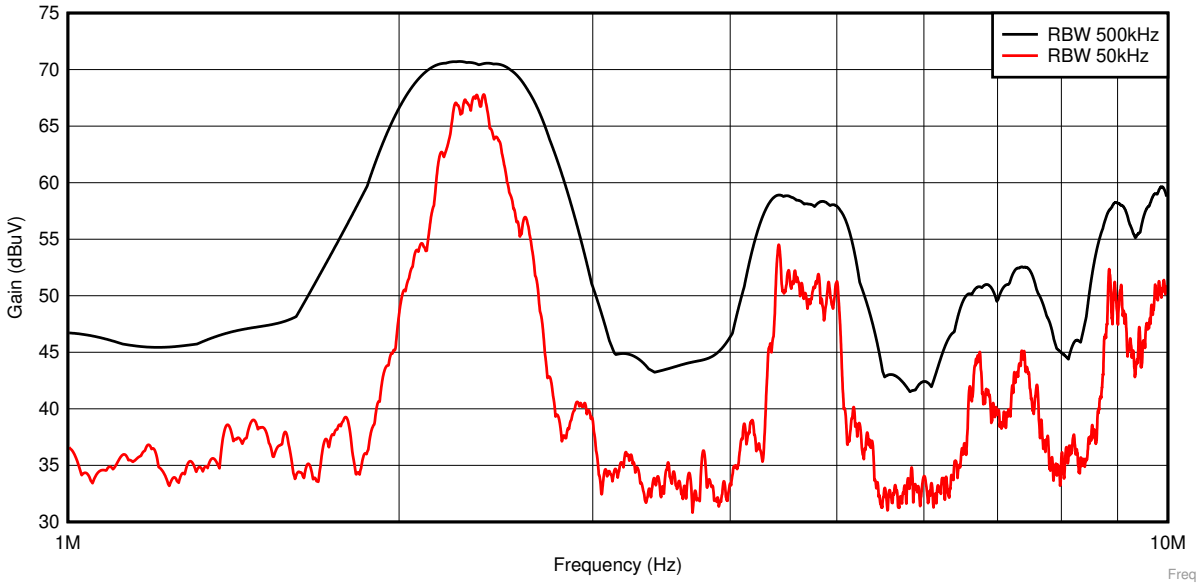

Figure 20. Input Voltage Spectrum — Spread-Spectrum Operation

2 Summary

Different concepts of controlling the switching frequency of two converters in a power tree are shown in this report. They can be implemented with different effort. No synchronization, either with constant frequency operation or spread spectrum obviously is the simplest implementation and allows the highest power conversion efficiency at light load since automatic transition in power save mode can be enabled. To avoid beat frequencies in an audible range when using converters with constant frequency operation, the nominal frequencies can be set wider apart to make sure the beat frequency is always above the audible range. Synchronization in any implementation can lower the input current and voltage ripple or at least control it at a defined frequency. This can reduce the effort for noise filtering. It may even allow lowering the total capacitance at the input of the converters. A simple method for implementing synchronization is using one of the DC/DC converters as a clock reference. Depending on the input and output voltage ratio the switching waveform can be used directly as a clock reference for the other converter. To get a stable solution the DC/DC converter providing the clock signal should be operated in forced PWM operation to avoid disruptions caused by low-frequency operation in power save mode. All experiments have been done at constant load current. Any changes in the load current of one of the converters will have an impact on its input current with an impact on the total input current of the system. It changes waveform and ripple of the total input current which may reduce the benefits of synchronization.

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