Freescale Semiconductor
Application Note

Document Number:A N4505
Rev. 0, 7/2012

Safety Considerations S12G-Family

by: Joachim Krücken
AISG MCU Design
Munich

Contents

1 Introduction

This application note describes top level features and connections to better understand the dependencies when analyzing failure modes and ways to detect faults.

The document splits the chip into the key building blocks and gives hints about fault detection mechanisms.

It should be noted, that in many cases only general hints are given, as the end application is owned by the customer.

2 Power Supply

The S12G-Family features an internal voltage regulator that generates the logic supply VDD = 1.8 V, and the Flash Supply VDDF = 2.8 V (typical) from the input of the VDDR and ranging from 3.13 V to 5.5 V. No external load capacitors are required. A key element of the voltage supply is the reference voltage created by a bandgap circuit.

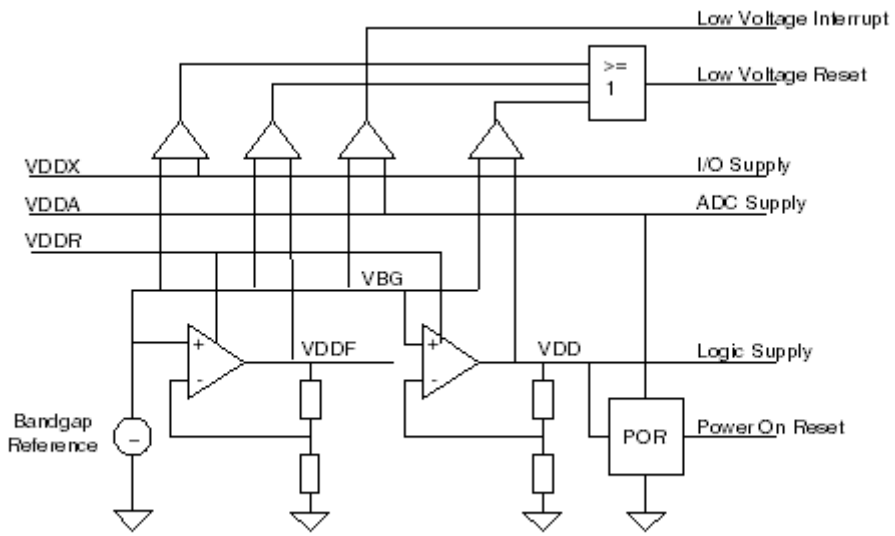

Figure 1. Power supply overview

The external voltage supply inputs are tied to the following circuits:

VDDR — Provides only the input to the internal voltage regulator.

VDDA — Supplies the bandgap, POR, the Low voltage reset and interrupt circuitry and the Input and Output pins (I/O) located located on the right hand side of the chip if pin 1 is in the top left corner.

VDDX — Supplies the I/O pins which are not supplied by VDDA.

In most S12G applications VDDR, VDDX, and VDDA are tied together at board level. On the smaller packages they are tied internally.

The three Low Voltage Reset (LVR) monitors supervise the VDD, VDDF, and VDDX supplies and asserts a reset if any of these drop below a minimum value.

The S12G features a Low Voltage Interrupt (LVI) at typical 4.2 V of the VDDA supply, which can be used in a 5 V system to indicate a drop of the supply.

The Power-On-Reset (POR) circuit independent from the bandgap reference and will assert the reset if the voltage drops below ca. 1.8 V ensuring a proper shutdown and initialization of the circuit at low voltages. The circuit is built by stacked MOS transistors in diode configuration, so that the actual voltage level tracks with the process deviations. For example, if the silicon process provides MOS transistors with lower Vt and therefore faster, the trip voltage of the POR is lower.

The VDDF can be measured by the ADC via an internal channel.

The following are possible failure modes in the power supply (assuming that VDDA, VDDX, and VDDR are not tied together as it is the case in the larger packages).

- **VDDR too low**

  If this voltage is too low, then VDDF or VDD will also be too low, therefore LVR is asserted.

- **VDDX too low**

  The LVR will assert a reset.

- **VDDA too low**

  As long as the bandgap is operating, the LVR will assert a reset.

- **VDD or VDDF too low**

Both voltages are separately monitored by the LVR circuit and a reset will be asserted.

- **Bandgap reference voltage too low**

  If the reference voltage is too low, then VDD and VDDF will also be too low. If VDD is low enough, then POR is asserted.

  Overall the bandgap is a well tested small circuit which is not stressed over its lifetime. The likelihood of a failure resulting in parametric shifts in this circuit is low.

- **VDDR, VDDX, or VDDA too high**

  There is no general protection against voltages that are too high. However in case the VREFH tracks with VDDA as in most systems, the ADC can read back the VDDF which is stabilized and compare it to its nominal value. In case the resulting ADC conversion count is too low, it is an indication for voltages that are too high.

- **VDD or VDDF too high**

  There are no provisions to detect this situation. VDDF can be monitored by the ADC. Assuming the VREFH is in the right range, then the value can be compared to its nominal value.

- **Bandgap voltage too high**

  If the reference voltage is too high, then VDD and VDDF will also be too high. The bandgap is a well tested small circuit, which is not stressed over its lifetime. The likelihood of a failure resulting in parametric shifts in this circuit is low.

3 Clock System

The S12G-Family features three independent time bases;
- Crystal/resonator oscillator (OSC),
- Internal RC 1MHz oscillator (IRC),
- Asynchronous periodic interrupt (API).

The IRC is trimmed such that it allows operation of a LIN bus without an external crystal or resonator.

The system clock can be generated from either the OSC directly or via the PLL which can be driven by the IRC or the OSC.

All peripherals, the CPU, and memories are clocked by the system clock.

Failures in the crystal or resonator cannot be distinguished from failures in the OSC circuit itself. Therefore they are captured here in the same section.

3.1 Crystal, resonator, or oscillator

The following are possible failure modes on the clock system crystal, resonator, or oscillator:

- **Crystal, resonator, or oscillator does not start**

  The system starts on the IRC. To switch to the external oscillator by software the oscillator must pass a clock quality check. This is indicated to the system by the UPOSC bit.

- **Crystal, resonator, or oscillator stop operation**

The Clock Monitor Unit (CMU) monitors the output of the oscillator. In case there are no clock edges for more than the typical 2.2 us (maximum of 5 us), the application can configure the circuit to create either a reset or switch into the Self-Clock-Mode (SCM). In the later case, the system continues to run on a slow clock. A change into or out of SCM is indicated by a change of state flag. A change can assert an interrupt if enabled.

- **Glitches on the oscillator output**

  The system clock is provided by either the PLL which is driven by the IRC or the external crystal. The PLL has the inherent property to act as a low pass filter efficiently suppressing disturbances at the oscillator output. If the disturbances get too big, the PLL unlocks. In this case the change of lock is indicated by a flag, which can assert an interrupt if enabled. The bus clock also divides the PLL clock by four and sets the system in a safe operating state. The fastest VCO output frequency divided by four is lower than the maximum allowed system clock frequency.

3.2 IRC

Compared to the oscillator, the IRC has no external connections and is less vulnerable to external noise injections.

The following are possible failure modes on the IRC:

- **IRC does not start**

  The system does not exit the reset state, which from the system point of view is a safe state.

- **IRC stops operation**

  It is unlikely this could happen, but two cases can be considered:

  - The system clock is generated by the external oscillator. The IRC in this case can only drive the Real Time Interrupt (RTI) or the COP. A missing RTI can be detected by software checking the RTI frequency using other timers driven from the system clock or the API.
  - The system clock is generated by the IRC. The PLL, if used would indicate this by loosing its lock state. The customer can configure the API timer to drive the COP.

3.3 PLL

The PLL is comprised of a Voltage Controlled Oscillator (VCO), a phase comparator, and a lock detector. Basic function of the PLL is to multiply a reference frequency which is either derived from the oscillator or the IRC to generate the system clock frequency. The VCO is an analog hardmacro while the rest is implemented in a standard cell approach. An important detection mechanism is the loss of the lock detector. This detector compares every 128 reference clock cycles the value of the feedback divider. In case there is a deviation of > 2 cycles a loss of lock status is asserted and an interrupt can be raised if enabled.

The following are possible failure modes on the PLL:

- **Configuration register corrupted**

  In case the most critical divider registers are corrupted the loss of lock indicator will trigger. Deviations of the system clock frequency generated by the PLL can be detected by the RTI, API, and most important the watchdog driven from different frequency generators. See Section 7.2.2 COP for details on clocking options.

- **Clock Select register corrupted**

  A frequency comparison using API, RTI, and Timer can detect this case.

- **PLL not starting**

  A software time out function that will detect this situation until the lock bit is set.

- **PLL loss of lock**

  Interrupt will be generated.

4 Core (CPU, Interrupt, Debug)

There are no special provisions in the S12G- CPU like dual core or comparison circuits. For critical mathematical operations, they could be calculated using a different code sequence and compared to each other. This covers most transient faults and if the algorithm is changed also for permanent defects.

- **Illegal Address**

  The S12G family provides an Illegal Address Reset (ILLADR) which can capture code runaways. This can be caused by an out of range supply voltage, noise in the lock system, and so on.

4.1 Interrupt module (INT)

The interrupt module collects the interrupt request signals from the peripherals and asserts a single interrupt request to the CPU. The CPU then changes the instruction flow at the next instruction boundary and requests an interrupt vector from the INT module. The INT module returns the interrupt vector with the highest priority, the CPU continues its operation from there. The interrupt priorities on S12G are fixed. All signals from to the INT module as well as from the INT module to the CPU are level sensitive (even if the peripheral itself reacts on an edge).

The following are possible failure modes on the Interrupt module:

- **Interrupt request stuck active**

  The CPU would constantly execute the interrupt service routine. In case the watchdog is not serviced, a reset is asserted.

- **Interrupt request stuck inactive**

  For interrupts that are expected at a certain rate, a potential timeout can be checked. For interrupts which are rare events, a check-software could periodically read the status registers associated with the interrupt and check if they are active.

- **Transient missing interrupt**

  This is a very unlikely event as the interrupt lines inside the MCU are level sensitive. Only a few events associated with the external inputs are edge sensitive. Those can be covered by routinely reading the input status.

- **Transient spurious interrupt**

  In this context a spurious interrupt is an interrupt which changes the flow of operation in the CPU, but when the vector fetch occurs no interrupt line is asserted. The S12G provides a special vector for such spurious interrupts.

  Hint — In most cases those spurious interrupts are associated with a software bug disabling an incoming interrupt in a race condition shortly after the interrupt was asserted and before the associated vector is fetched.

- **Wrong interrupt**

By bridging faults between two interrupt lines or other signals a wrong interrupt processing could start. It is advisable that each interrupt service routine checks the interrupt flags associated with the module causing the interrupt.

4.2 Debug module

The mode entry, serial communication, and the breakpoint module are summarized under the Debug module.

4.2.1 Mode entry

There are many ways to enter the debugging capabilities of the chip. Those ways require complex procedures to make the CPU enter the debug mode. At least a double fault is required to enter the debug mode.

The following are possible failure modes on the mode entry for the debug module:

- **Special single chip mode**

  The special single chip mode is entered by applying a logic low level to the MODC/BGND pin during reset. This will hold the CPU in a state waiting for communication via the single pin serial interface. No code has been executed, which means all peripherals and I/O ports are in their reset state.

- **Background debug command**

  In case a Background debug command (a distinct pattern of 16 0/1 symbols) is sent via the BKGD wire to the chip enters the debug modes and waits for further commands.

- **BGND instruction**

  In case the BGND instruction is executed by the CPU, the CPU enters the debug firmware and checks for the enable Background debug Mode bit (ENBDM). In case the ENBDM-bit is clear the CPU leaves the firmware again, causing a several cycle delay in the program execution. In case the ENBDM-bit is set, the CPU is idle waiting for a command via the BGND wire.

- **Hardware breakpoint**

  In case a hardware breakpoint is enabled and the CPU hits this breakpoint, the CPU enters firmware, executing a BGND instruction.

4.2.2 Serial interface communication

This serial interface uses pulse width modulated symbols for 0s and 1s and a dedicated stream of 0s and 1s to make the module enter the debug mode.

4.2.3 Breakpoint module

The breakpoint module can also be used to setup a software code check. By setting breakpoints to forbidden regions, data write, or reads, the CPU can be sent to debug mode in case of erroneous operation. Then the watchdog could reset the device if the ENBDM bit in the firmware is set. This may also help to prevent code run-away.

5 Input / Output Circuits

This section covers the main aspects for of the I/O circuits.

5.1 Port integration module (PIM)

The routing from the peripheral modules to the I/O pins is handled by the Port Integration Module (PIM). The configuration is mainly handled by the Package Code Register (PKGCR) and a smaller part by additional routing register bits. The basic philosophy of the S12 PIM is that an enabled peripheral module requests access to the pin and depending on the fixed priority the access is granted. Also invalid conditions like making the CAN RX pin an output are blocked by the combinatorial logic of the PIM. This method requires only a minimum of configuration registers and no sequential logic, which makes it robust against disturbances of any kind.

5.1.1 Package code register (PKGCR)

This register holds only three bits reflecting the package the chip is assembled in. This register is loaded during the startup phase from an internal NVM location, which is factory programmed.

The PKGCR content should be compared with the intended content and overwritten to block a potential corruption as it is a write once register.

5.2 General purpose I/O function and pin Logic

All I/Os have the same circuitry. The pins can be configured to either output or input. In case of output some I/Os provided can emulate an open drain port. In case of input they may also have a pull-up or pull-down device and provide an optional edge sensitive interrupt, which can be used for wakeup from STOP purposes as well.

The following are possible failure modes on the I/O function and pin logic:

The failure modes apply to any register. Details are given under their respective register functions.

- **Configuration corrupted**

  The content of the registers can be periodically read back and checked.

- **Input circuit defect**

  In case the port supports data in the register the value of the pin can be read back.

- **Output driver defect**

  In case the port supports data in the register the value of the pin can be read back.

- **Data Direction Register (DDR)**

  In case a peripheral is routed to the associated pin the content of this register is not relevant.

- **Data I/O Register**

Writing to the address of the Data I/O register defines the status of the pin in case it is configured as output and no peripheral module controls the pin. The content of the register is read back in case the DDR = 1, in case of DDR = 0 the actual value at the pin is read in all cases.

- **Data In Register**

  Some I/O ports provide a special read-only register which reads back the actual pin status independently of the DDR content or any peripheral controlling the pin. So the pin status can be observed at any time via software.

- **Pull Enable and Select Registers**

  The content of those registers can be periodically checked by the software. If it is important that there is a pull-device on a pin, an external device can be used in addition to the internal one.

- **Interrupt Flag and Enable Register**

  The content of those registers can be periodically checked by the software. Depending on the external hardware those bits can also be self tested by setting the port to output and creating the edge causing an interrupt.

- **Wired-or-Mode Register**

  The content of those registers can be periodically checked by software.

6 Memories

This section covers the non-volatile memories (NVM), the Program Flash and the EEPROM, and the Static RAM (SRAM).

6.1 Program Flash and EEPROM

The program and data flash share the charge pump and the high voltage regulator which are used only for programming and erasing. Bias circuit and sense-amplifiers are also shared and used during read. The main difference is the width of the data path which is 32 bits + 7 bits parity for the program flash and 16 bits + 6 bits for the EEPROM.

The following are possible failure modes on the program flash and EEPROM:

- **Erase or Programming Errors**

  The erase and program quality is ensured by verifying the status of the bit cells versus a more stringent margin then in normal reads. This prevents insufficient programmed or erased bit cells.

- **Incorrect Address decoder**

  Permanent defects in the address decoder can be detected by a Software CRC across a block of data in the NVM. This check must be done once per process safety time.

- **Single Bit Error**

  Single bit errors in the data path (39-Bits / 22-Bits) get corrected. The occurrence of the error correction is flagged and an interrupt is asserted if enabled.

- **Double Bit Error**
  Double bit errors in the data path (39-Bits / 22-Bits) are detected but not corrected. The occurrence of the error detection is flagged by a different flag bit than the error correction and an interrupt is asserted if enabled.

- 2 bit error

  More than 2 bit errors cannot be detected reliable. There are cases when 3 bit errors are detected as one bit errors and corrected.

- **ECC Logic not working**
  The ECC can be self-tested by programming phrases (a phrase is the combination of the dataword plus the parity bits) into the NVM. The S12G memory interface does not support as a user function the programming of a complete phrase. When programming the NVM the parity bits are automatically calculated by the state machine. The following procedure is a workaround making use of the property that during programming only 1 to 0 transitions are possible, while attempts to transition a 0 to a 1 are ignored. Carefully selecting two words can mimic a single, double bit, or any other error.
  a. 0xFFF4–0x20 — First word + ECC programmed to an erased memory location
  b. 0xFFFB–0x29 — Second word programmed at the same address as first word. Programming will however yield a verified error.
  c. 0xFFF0–0x20 — Resulting phrase; as only 1–>0 transitions can happen, bit 2 is now considered as a single bit error and corrected, data read will then result in 0xFFF4 with a single bit error. This can be tested at any time by reading out the word.

If there is some interest a set of data pairs for various bit error combinations can be provided.

- **Overall Non Volatile Memory (NVM) Content corrupted**

  For the Program-Flash a flash block wide CRC calculated at program start up can be used to detect this situation.

6.2 RAM

The RAM is a single hard macro 16-bit wide. There are no hardware measures to protect the RAM from corruption.

The Single Event Rate (SER) is the susceptibility of a RAM cell being flipped by either radiation from alpha particles or neutrons. The Freescale 9S12XEP100 180 nm device was measured according to the JDES89A standard. This device has a large RAM of 64 kBytes or 1 MBits, therefore better to measure. The S12G has the same RAM bit cell, wordline drives, and sense-amplifiers so that it is valid to scale the FIT rate to the 4Kbyte System RAM.

Composite n-SER and α-SER data are shown in Table 1 and are in line with industry benchmark.

Table 1. 180 nm n-SER and α-SER data compared to a benchmark foundry

180 nm SRAM	FIT / Mbit	–90% / +90% conf.	Benchmark FIT / Mbit
n-SER, sea level NYC	602	–125 / + 100	1000
α -SER, (0.001 α/cm^2/hr)	530	–38 / 34	450

The results of Table 1 were scaled to a product with 4 kByte of SRAM for two mold compounds, and the results are shown in Table 2. The rightmost column shows the FIT rate for a 4 KByte SRAM.

Table 2. 180 nm SRAM n-SER and a-SER data scaled to a 4 kByte SRAM product.

180 nm SRAM	FIT / Mbit	Mbits / 4 kByte	FIT/ Part
n-SER, sea level NYC	602	0.0328	20
α-SER, ULA mold compound (0.001 α/cm^2/hr)	530	0.0328	17
α-SER, std. mold compound (0.001 α/cm^2/hr)	10600	0.0328	347

Table 3 shows the mold compound used in the S12-Family, non-low alpha.

Table 3. Oneway analysis of alpha ray count (Count/cm2.hr) by type

Type	Alpha Ray Count Statistics		
	Median	Minimum	Maximum
Non-low alpha	0.0107	0.002	0.0265
Low alpha	All measured values below 0.001		

7 Peripherals

This section covers the main peripherals available on the S12G-family.

7.1 ADC

The ADC is a SAR type converter based on an array of scaled capacitances. Next to the external input channels it provides a selection of internal signals that can be used to self test the ADC. Those are VRH, high reference, (VRH+VRL)/2 midpoint, and VRL. VRL is tied to ground on all S12G devices. The VDDF of ca. 2.8 V can be converted. All inputs use the same converter and sampling circuit.

The following are possible failure modes on the ADC module:

- **Configuration corrupted**

  The configuration registers can be monitored periodically.

- **Reference voltage is wrong**

  The internal stable VDDF voltage of 2.8 V can be measured and an erroneous value can be identified. A deviation of the expected result can then be managed.

- **Signal path from the external source to the ADC is defect**

  The ADC offers a discharge feature that discharges the sample and hold capacitor before each conversion. If there is no driving signal source the conversion yields a result close to 0. If the useful range of the external signal starts at 0.5 V, this open connection can be detected. It is also possible to configure the ADC pins as outputs and drive them low or high. By converting those signals, the basic connection can be tested.

7.2 Timers

The S12G family provides three timers. Each timer can be driven by a different independent clock. This allows the checking of the correct frequency of operation for each of the timers using one of the others.

7.2.1 RTI

The Real Time Interrupt (RTI) can be driven by the OSC or the IRC. Its main purpose is to generate a periodic interrupt for task scheduling.

7.2.2 COP

The watchdog timer (COP) can be driven by the OSC, IRC, or API. Even if the OSC is not used there is an independent frequency source to drive the COP.

7.2.3 16-bit Timer

The 16-bit timer provides up to 8 channels (output compare or input capture) driven by a free running 16-bit counter. The 16-bit counter value can be read at any time and can also provide a periodic interrupt that can be used to monitor the function.

The following are possible failure modes on the 16-bit timer:

- **Output compare is not working**

  On each valid compare an interrupt can be generated, which can be checked by the task scheduler. Also on a successful compare an output pin can be set, cleared, or toggled. Its function can be self tested by reading the pin's output value.

- **Input Capture not working**

  On each active input edge (falling, rising, both) the actual value of the free running counter is captured in the input capture register. If enabled an interrupt is generated. It is possible to self test the input capture function depending on the external hardware, by setting the associated pin to output and generating an active edge.

7.2.4 API

The API has an independent time base (10 kHz), which can be used to drive the COP and create a periodic interrupt.

7.3 PWM

The PWM provides per channel an up counter, double buffered period, and duty cycle registers. Those counters are driven by a selectable pre-scaled bus clock.

The following are possible failure modes on the PWM module:

- **Configuration is corrupted**

  All configuration registers can be periodically monitored by the CPU.

- **Counter does not work**

  The actual counter value can be read by the CPU and progress being monitored

- **PWM output does not toggle**

In case the PWM is routed to an output pin the value of the output can be monitored by reading the actual pin value. In case the PWM is routed to a pin having a wake-up interrupt functionality an interrupt can be generated and monitored. In this case higher interrupt loading needs to be considered.

7.4 SPI

The SPI provides a serial synchronous interface to external devices. If the SPI is used in master mode the shift clock is derived from the system clock. In case of slave mode, the SPI is clocked by an external input.

The following are possible failure modes on the SPI module:

- **Configuration is corrupted**

  All configuration registers can be periodically monitored by the CPU.

- **Protocol Engine corrupted**

  In case of master mode this is easy to detect because for each transmission a byte or word is received and the associated flags are set.

  In case of slave mode any transmission is initiated by an external master device. Missing communication can be detected by a time-out.

- **Interrupts or completion flag missing**

  In case of master mode this is easy to detect because for each transmission a byte or word is received and the associated flags are set.

  In case of slave mode any transmission is initiated by an external master device. Missing communication can be detected by a time-out.

- **Baud Rate incorrect**

  The SPI is a synchronous protocol, this makes it non-detectable as data is correctly received or transmitted unless electrical characteristics are violated. The SPI protocol, because of its synchronous nature can be disturbed by noise on the clock. It is advisable to add parity bits to any communication.

7.5 SCI/LIN

The Serial Communication Interface (SCI) provides an asynchronous serial interface. Often it is associated with a single wire Local Interconnect Network (LIN) interface.

The following are possible failure modes on the SCI/LIN module:

- **Configuration is corrupted**

  All configuration registers can be periodically monitored by the CPU.

- **Protocol Engine corrupted**

  This is a asynchronous interface with several detection mechanisms that identifies wrong communication.

  Framing Error – Flags a missing STOP bit.

  Parity error – In case the protocol adds a parity bit to each byte, errors can be detected at byte level.

Noise error – The SCI provides a 3 sample per bit option, in case those 3 bits differ a noise flag is set.

In case of transmission, the transmit completion flag or the transmit buffer empty flag gets set. Via a timeout this can be monitored.

In case of LIN (single wire, half duplex) the transmitted bytes are received and can be verified.

In case of a full duplex two-wire interface, missing incoming data is difficult to identify. In case the SCI-RX receive is shared with an interrupt capable I/O port, the CPU can be notified of in-bound traffic and consequently checks if the SCI has received it.

- **Baud Rate incorrect**

  In a SCI system this leads to several errors like frame error, parity, and noise.

7.6 msCAN

The msCAN is comprised of a 64x16-bit dual ported RAM with logic synthesized in standard cells. The msCAN provides a loopback mode that can be used to self test the msCAN module.

The following are possible failure modes on the msCAN module:

- **Configuration is corrupted**

  All configuration registers can be periodically monitored by the CPU.

- **Protocol engine corrupted**

  There are several detection mechanisms available:
  Error bits (transmit and receive error active, passive and bus off)
  Error counters are read by the MCU
  Transmit buffer empty flag indicates a message has been successfully transmitted.
  Receiver buffer full flag indicates a message has been successfully received.

- **Baud rate incorrect**

  The CAN protocol ensures in this case that the node is taken off the CAN bus. Inside the msCAN module the situation can be detected by the BUSOFF Bit.

- **Dual ported RAM is corrupted**

  The content of the transmit buffer can be read back after its filled.

  The loopback mode allows a self-test test of the RAM.

7.7 System wide detection methods

In this section several detection methods are described, which are not directly related to a specific function.

7.7.1 Illegal Address

The S12G family provides an Illegal Address Reset (ILLADR), which can capture code runaways, potentially caused by supply voltage out of specified range, noise in the lock system, and so on.

7.7.2 Temperature Sensor

The ADC features a temperature sensor that returns a voltage proportional to the die temperature. In case of major short circuits this can be used to shutdown the MCU.

How to Reach Us:

Home Page:
www.freescale.com

Web Support:
http://www.freescale.com/support

USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
+1-800-521-6274 or +1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

Document Number: A N4505
Rev. 0, 7/2012