# PowerQUICC™ Integrated Communications Processors

freescale.com/powerarchitecture

freescale semiconductor

# Table of Contents

# MPC8572 PowerQUICC™ III Processor

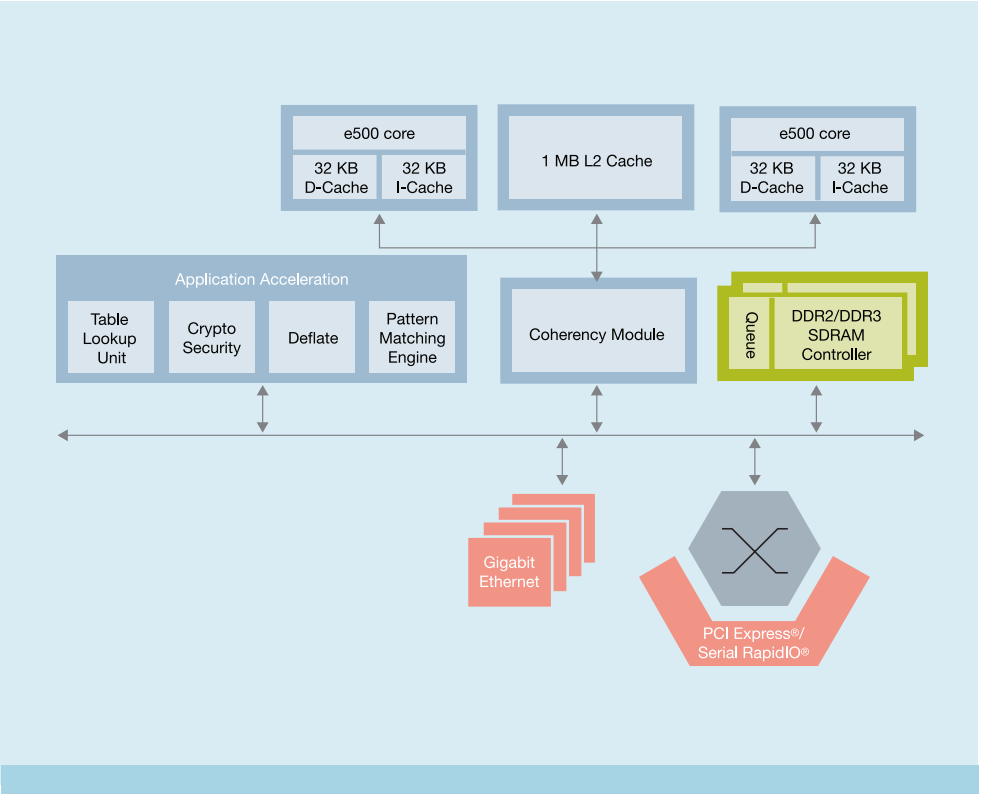
**Revolutionary and Evolutionary**

Freescale's next-generation PowerQUICC™ III integrated communications processors are designed to provide solutions for symmetrical and asymmetrical multi-core systems. Based on the scalable e500 system-on-chip (SoC) platform built on Power Architecture™ technology, they deliver dual-core gigahertz-plus communications processing performance with advanced content processing and security features.

The MPC8572 family of processors is designed to offer clock speeds from 1.2 GHz up to 1.5 GHz, combining two powerful processor cores, enhanced peripherals and high-speed interconnect technology to balance processor performance with I/O system throughput. These processors also contain an application acceleration block that integrates four powerful engines: a table lookup unit (TLU) that offloads complex table searches and header inspections, a pattern-matching engine to handle regular expression matching, a deflate engine to manage file decompression, and a security engine that accelerates crypto operations in IPSec and SSL/TLS for virtual private networks.

Based on Freescale's 90 nm silicon-on-insulator (SOI) copper interconnect process technology, the MPC8572 is designed to deliver higher performance with lower power dissipation. The MPC8572 processors provide a significant performance increase and represent the next step in continuous innovation from the popular PowerQUICC family. With uncompromising integration, the MPC8572 platform builds on the embedded core performance of Power Architecture technology and adds new features to enhance traffic management and security acceleration.

MPC8572 Block Diagram




Support for high-speed interfaces on the MPC8572 enables scalable connectivity to network processors and/or ASICs in the data plane while the MPC8572 platform handles complex, computationally demanding control plane processing tasks. These processors also include a next-generation double data rate (DDR2/DDR3) memory controller, enhanced Gigabit Ethernet support, double precision floating point and an integrated security engine that features updated Advanced Encryption Standard (AES) functionality.

**Key Features**

- Dual integrated DDR2/DDR3 memory controllers
- Single 10/100 Fast Ethernet controller (FEC) with MII (muxed)
- Four integrated Ethernet controllers (enhanced TSEC) with IEEE® 1588 support and lossless flow control
- Flexible high-speed interconnect interfaces Serial RapidIO® interconnect technology PCI Express®

freescale semiconductor

## Wide Range of Features for Multiple Target Applications

The robust feature set and advanced integration found on the MPC8572 family of processors provides an optimal communications processing solution for applications requiring Ethernet-only or RapidIO® interworking, such as multi-service routing and switching, firewall/VPN, unified threat management, intrusion detection and prevention, anti-virus, load balancing, content switching and application-aware networking equipment. The next-generation architecture also addresses the computationally demanding processing requirements of wireless infrastructure equipment, such as radio node controllers and WiMAX base stations.

The high-performance and cost-effective MPC8572 family of processors targets a wide range of imaging and general-purpose embedded control applications, such as robotics, discrete manufacturing and process manufacturing control.

On-chip support for the RapidIO serial fabric interface is ideal for connecting MPC8572 processors and peripherals in high-performance distributed systems. Examples include control plane processing, protocol processing and other compute-intensive applications requiring high-speed, peer-level communications with a low pin count, such as those found in AdvancedTCA® platforms. The RapidIO ecosystem is more than 50 members strong and includes industry-leading embedded vendors who provide host processors, DSPs, communications processors, backplane interfaces, switches, systems, tools, operating systems and services.

## Key Advantages

- High level of integration and performance
- Flexible SoC platform for fast time to market
- Consistent programming model across the PowerQUICC III family
- Simplified board design

## MPC8572/E Technical Specifications

- Dual embedded e500 core, scaling up to 1.5 GHz
  - 6897 MIPS at 1500 MHz (estimated Dhrystone 2.1)
- 36-bit physical addressing
- Enhanced hardware and software debug support
- Double-precision floating point unit
- Memory management unit
- Integrated L1/L2 cache
  - L1 cache—32 KB data and 32 KB instruction cache with line-locking support
  - Shared L2 cache—1 MB with ECC
  - L1 and L2 hardware coherency
  - L2 configurable as SRAM, cache and I/O transactions can be stashed into L2 cache regions
- Integrated DDR memory controller with full ECC support, supporting:
  - 333 MHz clock rate (667 MHz data rate), 64-bit, 1.8V SSTL, DDR2 SDRAM
  - 400 MHz clock rate (up to 800 MHz data rate), 64-bit, 1.5V SSTL, DDR3 SDRAM
- Application acceleration platform
  - Advanced TLU
  - Integrated security engine supporting DES, 3DES, MD-5, SHA-1/2, AES, RSA, RNG, Kasumi F8/F9 and ARC-4 encryption algorithms
  - Integrated pattern matching engine (Regular Expression)
  - Packet deflate engine
  - Integrated security engine with XOR
- Four on-chip, triple-speed Ethernet controllers supporting 10 and 100 Mbps, and 1 Gbps Ethernet/IEEE 802.3 networks with MII, RMII, GMII, SGMII, RGMII, RTBI and TBI physical interfaces and IEEE 1588
  - TCP/IP checksum acceleration and advanced QoS features
  - Lossless flow control
- General-purpose I/O
- Serial RapidIO and PCI Express high-speed interconnect interfaces
- On-chip network (OCeaN) switch fabric
- 133 MHz, 32-bit, 3.3V I/O, local bus with memory controller
- Dual Integrated DMA controller
- Dual $I^2C$ and DUARTS
- Programmable interrupt controller
- IEEE 1149.1 JTAG test access port
- 1.1V core voltage with 3.3V/2.5V/1.8V I/O
- 1023-pin FC-PBGA package

**Learn More:** For current information about Freescale products and documentation, please visit **www.freescale.com**.



Document Number: MPC8572FS
REV 2

freescale semiconductor

# MPC8568E PowerQUICC™ III Processor

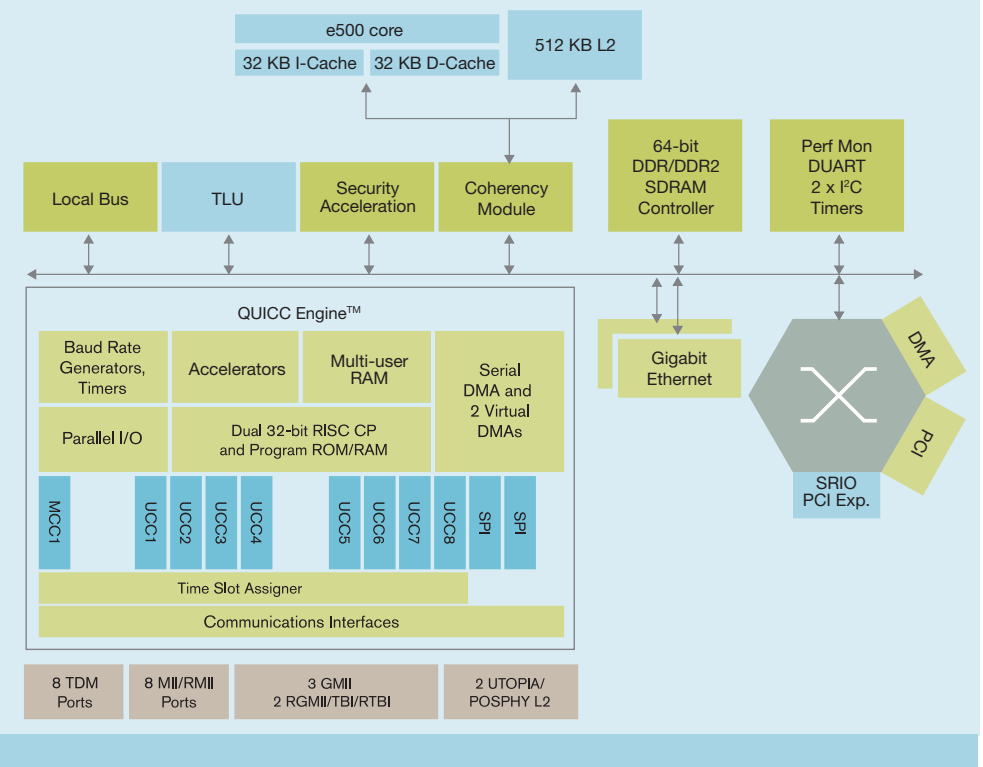
## Overview

The MPC8568E PowerQUICC™ III family is designed to address the increasing performance requirements for broadband access equipment including 3G/WiMAX/LTE base stations, RNC's, gateways and ATM/TDM/IP equipment. The MPC8568E enables both IP and multi-protocol solutions, combining a high-performance e500 processor core, built on Power Architecture™ technology, scaling up to 1.33 GHz with a flexible communications engine and high-speed system interfaces, enabling customers to handle many functions in a single chip solution that otherwise would require multiple devices. Ultimately this high level of integration provides savings in cost, power and board space. The MPC8568E provides multi-protocol support for both protocol termination and interworking for a wide range of communication protocols, including ATM, POS, Ethernet, PPP, HDLC and TDM—allowing the flexibility necessary for broadband access devices. Two enhanced Gigabit Ethernet ports, PCI Express® and Serial RapidIO® interconnect technology enables high-speed links to industry-wide switches, field-programmable gate arrays (FPGAs), application-specific integrated circuits (ASICs) and digital signal processors (DSPs). An integrated security engine supports common encryption algorithms, including the Kasumi algorithm needed for 3G wireless security.

## MPC8568E Family of Processors

The MPC8568E family consists of the MPC8568E and the MPC8567E. Both are offered in a 1023-pin FC-BGA package for pin compatibility.

MPC8568E Family Block Diagram integrated Control and Data Path for Network Interface Cards

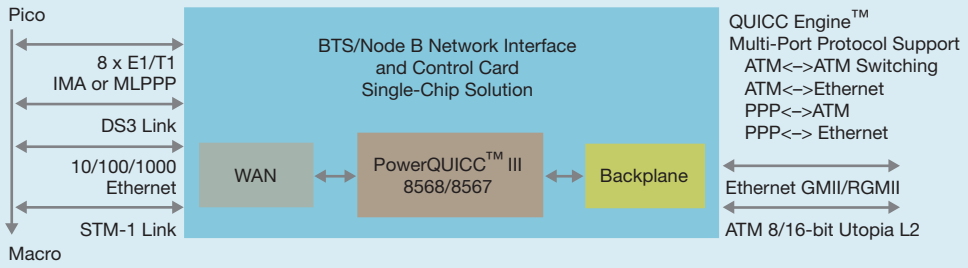



## Key Features

- High level of integration and performance, simplifying board design
- Consistent programming model across the PowerQUICC III family of processors
- Flexible system-on-chip (SoC) platform can help improve time to market
- 90 nm silicon-on-insulator (SOI) technology
- Enhanced high-performance e500 core
- 512 KB L2 cache
- High internal processing bandwidth
- Integrated DDR/DDR2 memory controller
- Two integrated Triple Speed Ethernet Controllers (enhanced TSEC)
- Advanced QUICC Engine™ technology supports a wide range of protocols and associated interworking
- TLU provides off-load for table search functions associated with IP forwarding, firewall and Access Control List (ACL) applications
- Flexible high-speed interconnect interfaces
- Serial RapidIO interconnect technology
- PCI Express support
- PCI and local bus interface support
- Integrated security engine

freescale semiconductor

## Wireless Node B Network Interface Cards (NIC) Block Diagram




## MPC8568E Processor Highlights

| | MPC8568E | MPC8567E |
|---|---|---|
| Core | e500 | e500 |
| CPU Speed | 1.0, 1.2, 1.33 GHz | 800 MHz, 1.0, 1.2, 1.33 GHz |
| L1 I/D Cache | 32 KB | 32 KB |
| L2 Cache | 512 KB | 512 KB |
| Memory Controller | 64-bit DDR/DDR2 | 64-bit DDR/DDR2 |
| Local Bus | 32-bit | 32-bit |
| System Interfaces | sRIO, PCI, PCI Express® (x8) | sRIO, PCI, PCI Express (x4) |
| Stand-Alone 10/100/1000 Ethernet | 2 (eTSEC) | - |
| Table Lookup Unit (TLU) | Yes | No |
| QUICC Engine™ | Up to 533 MHz | Up to 533 MHz |
| Ethernet | 3 x Gigabit, 8 x 10/100 | 3 x Gigabit, 8 x 10/100 |
| ATM (AAL0,1,2,5) | 2 x UTOPIA-L2, 124 M-PHY | 2 x UTOPIA-L2, 124 M-PHY |
| Packet over SONET (POS) | 2 x POSPHY-L2, 31 M-PHY | 2 x POSPHY-L2, 31 M-PHY |
| 8 TDMs (256 channels of HDLC) | 8 x T1/E1, 8 x T3/E3 | 8 x T1/E1, 8 x T3/E3 |
| Protocol Interworking | Yes | Yes |
| Security Engine | SEC 2.4 | SEC 2.4 |
| Additional Interfaces | DUART, 2 x I²C, 2 x SPI | DUART, 2 x I²C, 2 x SPI |
| Interrupt Controller | Yes | Yes |
| Package | 1023 FC-BGA | 1023 FC-BGA |

## Technical Specifications

- Embedded e500 core, scaling up to 1.33 GHz
  - 3199 MIPS at 1.33 GHz (estimated Dhrystone 2.1)
  - 36-bit physical addressing
  - Double-precision embedded floating point
  - Memory management unit (MMU)
- Integrated L1/L2 cache
  - L1 cache—32 KB data and 32 KB instruction
  - L2 cache—512 KB (8-way set associative)
- Integrated DDR memory controller with full ECC support
- Integrated security engine supporting DES, 3DES, MD-5, SHA-1/2, AES, RSA, RNG, Kasumi F8/F9 and ARC-4
- Two on-chip, triple-speed Ethernet controllers supporting 10 Mbps, 100 Mbps and 1 Gbps Ethernet/IEEE® 802.3 networks with MII, RMII, GMII, RGMII, RTBI and TBI physical interfaces
- QUICC Engine technology
  - Protocol Support:
    - ATM SAR up to 622 Mbps (OC-12) full duplex
    - PPP, multi-link (ML-PPP), multi-class (MC-PPP) and PPPmux
    - IP termination support for IPv4
    - L2 Ethernet interworking
    - ATM (AAL2/AAL5) to Ethernet (IP) interworking
    - Extensive support for Ethernet RMON/MIB statistics
    - 256 channels of HDLC/Transparent or 128 channels of SS#7
  - Serial Interfaces:
    - Two UL2/POS-PHY interfaces
    - Three 1 Gbps Ethernet interfaces using GMII. Two 1 Gbps Ethernet interfaces using RGMII, TBI and RTBI
    - Up to eight 10/100 Mbps Ethernet interfaces using MII or RMII
    - Up to eight T1/E1/J1 interfaces or eight T3/E3 interfaces
    - Dual SPI interfaces
- Serial RapidIO and PCI Express high-speed interconnect interfaces
- Table lookup unit
- On-chip network (OCeaN) switch fabric
- 32-bit PCI 2.2 bus controller (up to 66 MHz, 3.3V I/O)
- 166 MHz, 32-bit, 3.3V I/O, local bus with memory controller
- Integrated four-channel DMA controller
- Dual I²C and Dual Universal Asynchronous Receiver/Transmitter (DUART) support
- Programmable interrupt controller (PIC)
- IEEE 1149.1 JTAG test access port
- 1.1V core voltage with 3.3V, 2.5V and 1.8V I/O
- 1023-pin FC-BGA package

**Learn More:** For current information about Freescale products and documentation, please visit **www.freescale.com**.



Document Number: MPC8568FS
REV 2

# MPC8560/E PowerQUICC™ III Processor

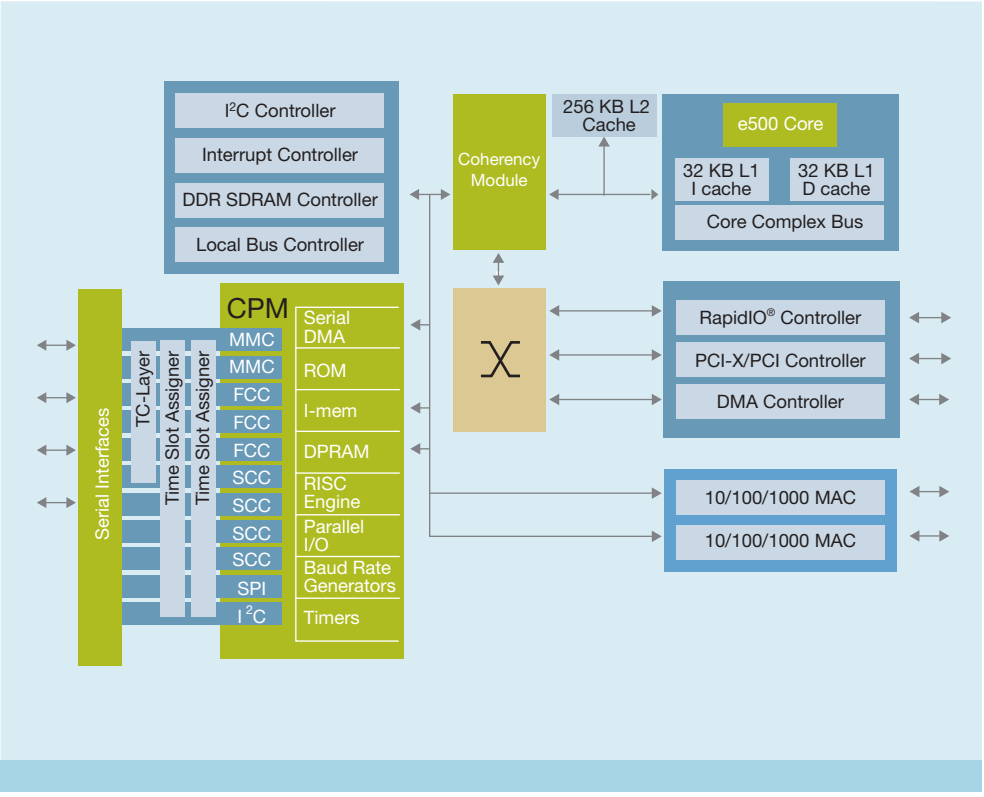
## Overview

The PowerQUICC™ III is a versatile integrated communications processor designed for a variety of compute-intensive applications, excelling particularly in communications and networking products. Freescale's PowerQUICC III processor family is the next generation of Freescale's industry-leading PowerQUICC line of integrated communications processors. PowerQUICC III processors provide higher performance in all areas of device operation, including greater flexibility, extended capabilities and higher integration.

## Product Highlights

Freescale's leading PowerQUICC III architecture integrates two processing blocks. One block is a high-performance embedded e500 core. With 256 KB of Level 2 cache, the e500 core built on Power Architecture™ technology provides unprecedented levels of hardware and software debugging support. The second block is the Communications Processor Module (CPM). The CPM of the PowerQUICC III can support three fast serial communications controllers (FCCs), two multi-channel controllers (MCCs), four serial communications controllers (SCCs), one serial peripheral interface (SPI) and one I²C interface. The PowerQUICC III also offers two integrated 10/100/1000 Ethernet controllers, a DDR SDRAM memory controller, a 64-bit PCI-X/PCI controller and a RapidIO® interconnect. This high level of integration helps simplify board design and offers significant bandwidth and performance for high-end control plane and data plane applications.

MPC8560 Block Diagram




## RapidIO Interconnect Technology

As a founding member of the RapidIO Trade Association, Freescale has been driving the industry's adoption of this high-performance switch fabric control plane interconnect. RapidIO technology offers significantly greater bandwidth, scalability and reliability than other interconnects in use today, yet is compatible with existing PCI and CPU architectures. It has a flexible architecture that can easily adapt to changing industry needs without affecting existing infrastructure. RapidIO technology is an open standard governed by an industry body, designed specifically for embedded, networking and communications applications.

RapidIO MEMBER

freescale semiconductor

| PowerQUICC™ III Processor Family | MPC8541E | MPC8540 | MPC8555E | MPC8560 |
|---|---|---|---|---|
| **Core** | e500 | e500 | e500 | e500 |
| **Frequency** | 533 MHz–1 GHz | 667 MHz–1 GHz | 533 MHz–1 GHz | 667 MHz–1 GHz |
| **I-Cache/D-Cache (KB)** | 32/32 | 32/32 | 32/32 | 32/32 |
| **Integrated L2 Cache (KB)** | 256 | 256 | 256 | 256 |
| **Integrated Security Engine** | Yes | - | Yes | - |
| **Fast Communications Controllers** | - | - | 2 | 3 |
| **Serial Communications Controllers** | - | - | 3 | 4 |
| **Ethernet (10/100 only)** | 2 | 1 | Up to 2 | Up to 3 |
| **Ethernet (10/100/1000)** | 2 | 2 | 2 | 2 |
| **I²C Controller** | 2 | 1 | 2 | 2 |
| **UTOPIA Level II Ports** | - | - | 2 | 2 |
| **Multi-Channel HDLC** | - | - | Up to 64 (QMC) | Up to 256 |
| **PCI Interface** | 2x 32-bit or 1x 64-bit | 1x 32/64-bit | 2x 32-bit or 1x 64-bit | 1x 32/64-bit |
| **PCI-X Interface** | - | Yes | - | Yes |
| **RapidIO® Interface** | - | Yes | - | Yes |

## Typical Applications

- Remote access concentrators/servers
- Regional office routers
- Wireless infrastructure equipment
- Telecommunications switching and transmission equipment
- Ethernet switches
- T1/E1 and T3/E3 line cards
- OC-3 line card
- LAN-to-WAN router
- DSLAMs
- Multi-service access platforms
- Optical networking
- IP networking
- SONET transmission controller
- Media gateways
- IP Virtual Private Networks (VPN)

## Technical Specifications

- High-performance embedded e500 core available from 667 MHz to 1 GHz
  - 32-bit, dual-issue, superscalar, seven-stage pipeline
  - 2310 MIPS at 1 GHz (estimated Dhrystone 2.1)
  - 32 KB L1 data and 32 KB L1 instruction cache with line locking support
  - 256 KB on-chip L2 cache with direct mapped capability
  - Enhanced hardware and software debug support
  - Memory management unit (MMU)
  - SIMD extension with single precision floating point
- Two TSECs supporting 10/100/1000 Mbps Ethernet with two GMII/TBI/RGMII interfaces
- High-performance CPM
  - 32-bit RISC architecture running up to 333 MHz
  - One instruction per clock
  - Software compatible with other CPM-based offerings
  - 32 KB dual-port RAM
  - Three full-duplex FCCs supporting:
    - ATM at up to 155 Mbps
      - Support for two UTOPIA interfaces
      - AAL0, AAL1, AAL2, AAL3/4, AAL5
    - 10/100 Mbps Ethernet
      - Support for up to three MII/RMII interfaces
    - HDLC/transparent up to 45 Mbps
  - ATM transmission convergence layer capabilities (eight channels)
  - Integrated inverse multiplexing for ATM (IMA) functionality
  - Two MCCs
    - Up to 256 HDLC/transparent channels at 64 Kbps each
    - Eight TDM interfaces
  - Four full-duplex SCCs that support the following protocols:
    - High level/synchronous data link control (HDLC/SDLC)
    - LocalTalk (HDLC-based local area network protocol)
    - Universal asynchronous receiver transmitter (UART)
    - Synchronous UART (1x clock mode)
    - Binary synchronous communication
    - Totally transparent operation
  - Serial peripheral interface support for master or slave
  - I²C bus controller
  - Time-slot assigner (TSA) supports multiplexing of data from any of the SCCs and FCCs onto eight time-division multiplexed (TDM) interfaces
- DDR SDRAM memory controller
  - 166 MHz, 64-bit, 2.5V I/O
  - Full ECC support
- RapidIO controller—500 MHz, 8-bit, LVDS I/O
  - PCI, PCI-X controller
  - PCI 2.2 and PCI-X 1.0 compatible
  - 64- or 32-bit PCI from 16 to 66 MHz
- 64-bit PCI-X support up to 133 MHz
- Host and agent mode support
- Integrated 4-channel DMA controller
- Local bus with memory controller—166 MHz, 32-bit, 3.3V I/O
- Interrupt controller
- IEEE® 1149.1 JTAG test access port
- 1.2V core power supply (1.3V for 1 GHz operation) with 3.3V and 2.5V I/O
- 783-pin FC-BGA package

**Learn More:** For current information about Freescale products and documentation, please visit **www.freescale.com**.



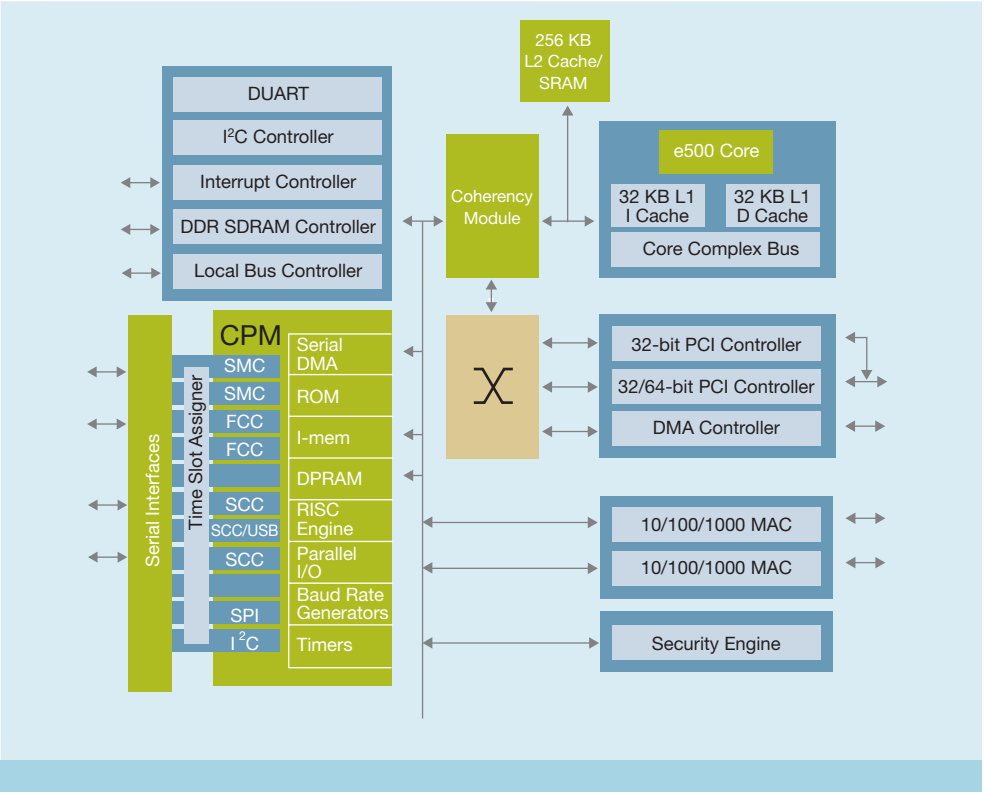
Document Number: MPC8560FACT
REV 9

freescale semiconductor

# MPC8555/E PowerQUICC™ III Processor

Freescale's MPC8555E PowerQUICC™ III integrated communications processor integrates a wide range of advanced Freescale technologies, modular cores and peripherals. Leveraging Freescale's system-on-chip (SoC) PowerQUICC III platform achitecture, the MPC8555E combines the powerful Book E e500 core, built on Power Architecture™ technology, and communications peripheral technology to balance processor performance with I/O system throughput. Freescale's MPC8555E device integrates two processing blocks: a high-performance e500 core that implements the enhanced Power Architecture Book E instruction-set architecture and a RISC-based Communications Processor Module (CPM) that supports a wide range of communications peripherals. This innovative architecture is designed to reduce power consumption and offer a more balanced approach to processing than traditional processor architectures. The CPM offloads low-level peripheral communications tasks, enabling the embedded e500 core to manage high-level processing tasks. The MPC8555E device's high level of integration helps simplify board design and enhances system-level bandwidth and performance. In addition to the e500 core and CPM, the MPC8555E features an integrated security engine, a double data rate SDRAM (DDR SDRAM) memory controller, dual Gigabit Ethernet controllers, a four-channel DMA controller, dual asynchronous receiver/ transmitters (DUART) and a 64-bit PCI controller that can also serve as two 32-bit PCI ports. Dual on-chip PCI support provides a cost-effective alternative to separate, discrete PCI bridges and chipsets for I/O intensive applications that require multiple PCI interfaces. In addition to these features, the MPC8555E provides a local bus controller and I²C support.

## MPC8555/E Block Diagram




### Integrated Security

The MPC8555E processor features a security engine that supports DES, 3DES, MD-5, SHA-1, AES and ARC-4 encryption algorithms, as well as offering a public key accelerator and on-chip random number generator. This embedded security core is derived from Freescale's security coprocessor product line and offers the same direct-memory access (DMA) and parallel processing capabilities, as well as the ability to perform single-pass encryption and authentication as required by widely used security protocols, such as IPsec and 802.11i. Integrated security makes the MPC8555E an optimal communications processor solution for applications that require security features in concert with high performance and low system-level cost.

### Wide Range of Applications

With its high-performance core, communications processor module and integrated security engine, the MPC8555E processor offers a powerful control element for networking, communications and general-purpose embedded applications. The MPC8555E serves as an optimal host-processing solution for a multitude of compute-intensive applications, such as telecommunications, integrated access devices and metro area networks.

freescale semiconductor

| PowerQUICC™ III Processor Family | MPC8541E | MPC8540 | MPC8555E | MPC8560 |
|---|---|---|---|---|
| **Core** | e500 | e500 | e500 | e500 |
| **Available Frequencies** | 533 MHz–1 GHz | 667 MHz–1 GHz | 533 MHz–1 GHz | 667 MHz–1 GHz |
| **I-Cache/D-Cache (KB)** | 32/32 | 32/32 | 32/32 | 32/32 |
| **Integrated L2 Cache (KB)** | 256 | 256 | 256 | 256 |
| **Integrated Security Engine** | Yes | - | Yes | - |
| **Fast Communications Controllers** | - | - | 2 | 3 |
| **Serial Communications Controllers** | - | - | 3 | 4 |
| **Ethernet (10/100 Only)** | 2 | 1 | Up to 2 | Up to 3 |
| **Ethernet (10/100/1000)** | 2 | 2 | 2 | 2 |
| **I²C Controller** | 2 | 1 | 2 | 2 |
| **UTOPIA Level II Ports** | - | - | 2 | 2 |
| **Multi-Channel HDLC** | - | - | Up to 64 (QMC) | Up to 256 |
| **PCI Interface** | 2 x 32-bit or 1 x 64-bit | 1 x 32/64-bit | 2 x 32-bit or 1 x 64-bit | 1 x 32/64-bit |
| **PCI-X Interface** | - | Yes | - | Yes |
| **RapidIO® Interface** | - | Yes | - | Yes |

## Key Advantages

- High level of integration and performance
- CPM for peripheral processing tasks
- Integrated security engine
- Multiple-PCI interface support
- High-performance Book E core
- Lower power consumption
- Flexible SoC platform for fast time-to-market
- Simplified board design

## Typical Applications

- Telecommunications switching equipment
- Integrated access devices
- Metro area networks
- VPN and firewall routers
- Branch office and enterprise routers

## Technical Specifications

- Embedded e500 Book E core available from 533 MHz up to 1 GHz
  - 32-bit, dual-issue, superscalar, seven-stage pipeline
  - 2300 MIPS at 1 GHz (estimated Dhrystone 2.1)
  - 32 KB L1 data and 32 KB L1 instruction cache with line-locking support
  - 256 KB on-chip L2 cache with direct mapped capability
  - Enhanced hardware and software debug support
  - Memory management unit (MMU)
- Two TSECs supporting 10/100/1000 Mbps Ethernet (IEEE® 802.3, 802.3u, 802.3x, 802.3z and 802.3 ac-compliant) with two MII/GMII/TBI/RGMII/RTBI interfaces
- 166 MHz, 64-bit, 2.5V I/O, DDR SDRAM memory controller with full ECC support
- Integrated security engine supporting DES, 3DES, MD-5, SHA-1, AES, PKEU, RNG and RC-4 encryption algorithms
- CPM to handle communications tasks
  - e500 core and CPM may run at different frequencies
  - 32-bit scalar RISC controller
  - General-purpose I/O
  - Parallel I/O registers
  - Onboard 16K of dual-port RAM
  - Two fast communications controllers (FCCs) supporting:
    - Two 10/100 Base-T Ethernet MACs with MII/RMII interfaces
    - Two 8-bit UTOPIA interfaces for ATM
    - ATM AAL 0,1,2,5
    - Multi-PHY support for 31 x 2 or 62 PHYs
    - HDLC
  - Three serial communications controllers (SCCs)
  - Support for multi-channel HDLC (up to 64 channels two T1/E1)
  - Two serial management controllers (SMCs)
  - One I²C port (in addition to another I²C port in the platform)
  - One serial peripheral interface (SPI)
  - USB host/device interface (USB 2.0 full/low-speed compatible)
- Multiple PCI interface support
  - 64-bit PCI 2.2 bus controller (up to 66 MHz, 3.3V I/O)
  - Flexibility to configure two 32-bit PCI controllers
- 166 MHz, 32-bit, 3.3V I/O, local bus with memory controller
- Integrated four-channel DMA controller
- Dual I²C and DUART support
- Interrupt controller
- IEEE 1149.1 JTAG test access port
- 1.2V core power supply (1.3V for 1 GHz operation) with 3.3V and 2.5V I/O
- 783-pin FC-BGA package

## Learn More

With more than 5,000 design wins and greater than 82 percent market share in communications processors, Freescale's PowerQUICC processors are the ideal choice for your embedded networking and communication system needs.

To learn more about Freescale's communications and networking embedded solutions, visit us on the Web: **www.freescale.com/powerquicc.**

**Learn More:** For current information about Freescale products and documentation, please visit **www.freescale.com**.



Document Number: MPC8555EFS
REV 7

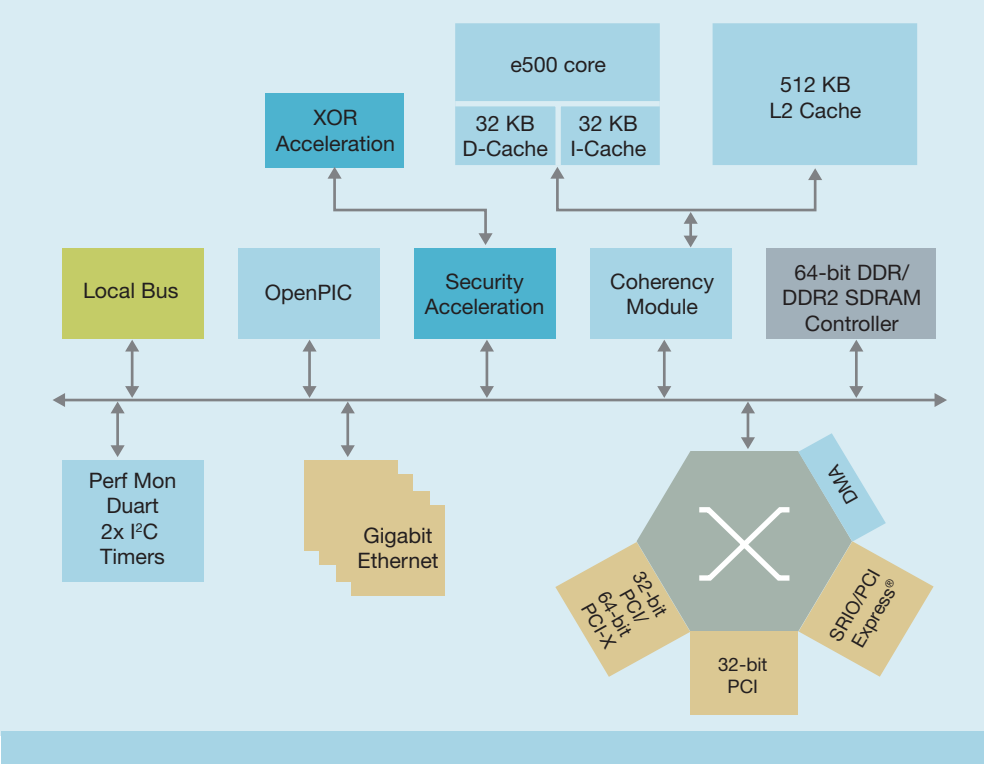
# MPC8548E PowerQUICC™ III Processor Family

## Key Features

The MPC8548E networking/telecom processor features an embedded e500 core, targeting up to a 1.5 GHz core operation, an integrated security engine, 64-bit DDR/ DDR2 controller scaling up to 667 MHz data rate, dual 32-bit PCI or 64-bit PCI-X, 4-bit serial RapidIO® fabric technology and 4-bit PCI Express® (or single 8-bit PCI Express 1.0a), local bus I/O interfaces and four Gigabit Ethernet interfaces. The combination of these features makes this device an optimal communications processing solution for Ethernet-only or RapidIO interworking applications, such as enterprise networking, telecom transmission and switching and 3G wireless base stations. The security engine includes Kasumi algorithm acceleration, making the MPC8548E an ideal choice for enhancing security protocol processing in 2.5G and 3G wireless network infrastructure. This device's integrated security also includes XOR acceleration, which enhances system performance by offloading the compute-intensive parity check in small-medium business enterprise and redundant array of inexpensive disk storage applications.

The MPC8548E device is the first integrated communications processor to comply with the Serial RapidIO interconnect specification, Revision 1.2, from the RapidIO Trade Association. The RapidIO serial fabric interface is ideal for connecting MPC8548 processors and peripherals in high-performance distributed systems. Examples include control plane processing, protocol processing and other compute-intensive applications requiring high-speed, peer-level communications with a low pin count, such as those found in AdvancedTCA® platforms.

MPC8548/E Block Diagram




The PowerQUICC™ III RapidIO ecosystem is more than 50 members strong and includes industry-leading embedded vendors who provide host processors, DSPs, communications processors, backplane interfaces, switches, systems, tools, operating systems and services. The 90 nm PowerQUICC III family includes the MPC8548E, MPC8547E, MPC8545E and MPC8543E.

The MPC8547 is targeted toward storage markets, the MPC8545 includes features for printing and imaging markets and the MPC8543 is targeted at general purpose data plane processing requirements—rounding out the product family.

### High-Speed Connectivity

Freescale's MPC8548E processor offers a wide range of high-speed connectivity options, including enhanced Triple Speed Ethernet, serial RapidIO interconnect technology and PCI Express. Support for these high-speed interfaces enables scalable connectivity to network processors and/or ASICs in the data plane while the PowerQUICC III handles complex, computationally demanding control plane processing tasks. These processors also feature next-generation double data rate (DDR2) memory controllers, enhanced Gigabit Ethernet support, double precision floating point and integrated security engines that support the Kasumi algorithm needed for 3G wireless security. In addition, support is provided for exclusive OR (XOR) acceleration needed for parity in storage applications.

### MPC8548E Technical Specifications

- Embedded e500 core, initial offerings up to 1.33 GHz, targeting up to 1.5 GHz
  - Dual dispatch superscalar, seven-stage pipeline design with out-of-order issue and execution
  - 3065 MIPS at 1333 MHz (estimated Dhrystone 2.1)
    - 36-bit physical addressing
- Enhanced hardware and software debug support
- Double-precision embedded scalar and vector floating-point APUs
- Memory management unit (MMU)
- Integrated L1/L2 cache
  - L1 cache—32 KB data and 32 KB instruction cache with line-locking support
  - L2 cache—512 KB (8-way set associative); 512 KB/256 KB/128 KB/64 KB can be used as SRAM
  - L1 and L2 hardware coherency
  - L2 configurable as SRAM, cache and I/O transactions can be stashed into L2 cache regions
- Integrated DDR memory controller with full ECC support, supporting:
  - 200 MHz clock rate (400 MHz data rate), 64-bit, 2.5V/2.6V I/O, DDR SDRAM
  - 333 MHz clock rate (up to 667 MHz data rate) DDR2 SDRAM
- Integrated security engine supporting DES, 3DES, MD-5, SHA-1/2, AES, RSA, RNG, Kasumi F8/F9 and ARC-4 encryption algorithms
- Four on-chip triple-speed Ethernet controllers (GMACs) supporting 10 and 100 Mbps, and 1 Gbps Ethernet/ IEEE® 802.3 networks with MII, RMII, GMII, RGMII, RTBI and TBI physical interfaces
  - TCP/IP checksum acceleration
  - Advanced QoS features
- General-purpose I/O (GPIO)
- Serial RapidIO and PCI Express high-speed interconnect interfaces, supporting:
  - Single x8 PCI Express, or
  - Single x4 PCI Express and single 4x serial RapidIO
- On-chip network (OCeaN) switch fabric
- Multiple PCI interface support
  - 64-bit PCI 2.2 bus controller (up to 66 MHz, 3.3V I/O)
  - 64-bit PCI-X bus controller (up to 133 MHz, 3.3V I/O), or
  - Flexibility to configure two 32-bit PCI controllers
- 166 MHz, 32-bit, 3.3V I/O, local bus with memory controller
- Integrated four-channel DMA controller
- Dual $I^2C$ and Dual Universal Asynchronous Receiver/Transmitter (DUART) support
- Programmable interrupt controller (PIC)
- IEEE 1149.1 JTAG test access port
- 1.2V core voltage with 3.3V and 2.5V I/O
- 783-pin FC-BGA package

**MPC854X Product Comparison**

| | MPC8548E | MPC8547E | MPC8545E | MPC8543E |
|---|---|---|---|---|
| L2 cache | 512 KB | 512 KB | 512 KB | 256 KB |
| 64-bit DDR2 support | Yes | Yes | Yes | Yes |
| Support for battery-backed DDR | Yes | Yes | - | - |
| PCI/PCI-X | Single 64-bit PCI/PCI-X or dual 32-bit PCI | 64-bit PCI/PCI-X | Single 64-bit PCI/PCI-X or dual 32-bit PCI | 32-bit PCI |
| Enhanced three-speed Ethernet Controller (eTSECs) | 4 | 4 | 2 | 2 |
| High-speed interconnects | x8/x4/x2/x1 PCI Express®<br>4x/1x serial RapidIO® and x4/x2/x1 PCI Express | x4/x2/x1 PCI Express | x4/x2/x1 PCI Express | 4x/1x Serial RapidIO<br>x4/x2/x1 PCI Express |
| Double-precision floating-point APU | Yes | Yes | Yes | Yes |
| Integrated security engine | Yes | Yes | Yes | Yes |
| XOR acceleration | Yes | Yes | - | - |

**Learn More:** For current information about Freescale products and documentation, please visit **www.freescale.com**.



Document Number: MPC8548PQIIIFS
REV 1

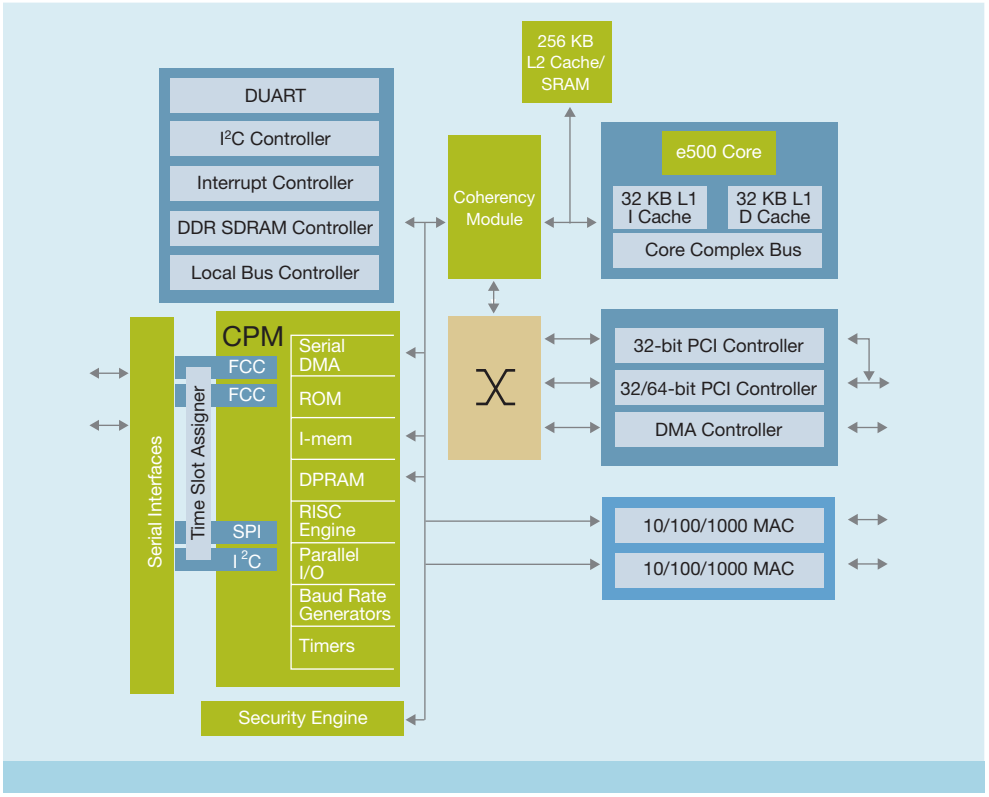
# MPC8541E PowerQUICC™ III Processor

## Key Features

Freescale's MPC8541E PowerQUICC™ III integrated communications processor incorporates a wide range of advanced Freescale technologies, modular cores and peripherals. Leveraging Freescale's system-on-chip (SoC) PowerQUICC III platform architecture, the MPC8541E combines the powerful e500 core, built on Power Architecture™ technology, and peripheral technology to balance processor performance with I/O system throughput.

The MPC8541E device's high level of integration helps simplify board design and enhances overall system-level bandwidth and performance. In addition to the e500 core and 256 KB of Level 2 (L2) cache memory, the MPC8541E features an integrated security engine, a double data rate (DDR) SDRAM memory controller, dual Gigabit Ethernet controllers, a four-channel DMA controller, dual asynchronous receiver/transmitters (DUART), local bus controller and a 64-bit PCI controller that can also serve as two 32-bit PCI ports. Dual on-chip PCI support provides a cost-effective alternative to separate, discrete PCI bridges and chipsets for I/O-intensive applications that require multiple PCI interfaces. The MPC8541E also supports Communications Processor Module (CPM) capabilities, such as dual 10/100 Fast Ethernet controllers, I²C controller and a serial peripheral interface (SPI).

MPC8541E Block Diagram




## Integrated Security

The MPC8541E processor features a security engine that supports DES, 3DES, MD-5, SHA-1, AES and ARC-4 encryption algorithms and offers a public key accelerator and on-chip random number generator. This embedded security core is derived from Freescale's security coprocessor product line and offers the same direct memory access (DMA) and parallel processing capabilities, as well as the ability to perform single-pass encryption and authentication as required by widely used security protocols, such as IPsec and 802.11i. Integrated security makes the MPC8541E an optimal communications processor solution for applications that require security features in concert with high performance and low system-level cost.

## Wide Range of Applications

With its high-performance core, I/O peripherals and integrated security engine, the MPC8541E processor offers a powerful control element for networking, communications and general-purpose embedded applications. The MPC8541E serves as an optimal host-processing solution for a multitude of compute-intensive applications, such as VPN and firewall routers, enterprise-class storage systems, Ethernet switching equipment, SOHO, enterprise router, business-class imaging equipment and general-purpose embedded applications.

freescale semiconductor

| PowerQUICC™ III Processor Family | MPC8541E | MPC8540 | MPC8555E | MPC8560 |
|---|---|---|---|---|
| Core | e500 | e500 | e500 | e500 |
| Available Frequencies | 533 MHz–1 GHz | 667 MHz–1 GHz | 533 MHz–1 GHz | 667 MHz–1 GHz |
| I-Cache/D-Cache (KB) | 32/32 | 32/32 | 32/32 | 32/32 |
| Integrated L2 Cache (KB) | 256 | 256 | 256 | 256 |
| Integrated Security Engine | Yes | - | Yes | - |
| Fast Communications Controllers | 2 | - | 2 | 3 |
| Serial Communications Controllers | - | - | 3 | 4 |
| Ethernet (10/100 only) | 2 | 1 | Up to 2 | Up to 3 |
| Ethernet (10/100/1000) | 2 | 2 | 2 | 2 |
| I²C Controller | 2 | 1 | 2 | 2 |
| UTOPIA Level II Ports | - | - | 2 | 2 |
| Multi-Channel HDLC | - | - | Up to 64 (QMC) | Up to 256 |
| PCI Interface | 2x 32-bit or 1x 64-bit | 1x 32/64-bit | 2x 32-bit or 1x 64-bit | 1x 32/64-bit |
| PCI-X Interface | - | Yes | - | Yes |
| RapidIO® Interface | - | Yes | - | Yes |

**Technical Specifications**

- Embedded e500 core available from 533 MHz up to 1 GHz
  - 32-bit, dual-issue, superscalar, seven-stage pipeline
  - 2300 MIPS at 1 GHz (estimated Dhrystone 2.1)
  - 32 KB L1 data and 32 KB L1 instruction cache with line-locking support
  - 256 KB on-chip L2 cache with direct mapped capability
  - Enhanced hardware and software debug support
  - Memory management unit (MMU)
- Two TSECs supporting 10/100/1000 Mbps Ethernet (IEEE 802.3, 802.3u, 802.3x, 802.3z and 802.3ac-compliant) with two GMII/TBI/RGMII interfaces
- 166 MHz, 64-bit, 2.5V I/O, DDR SDRAM memory controller with full ECC support
- Integrated security engine supporting DES, 3DES, MD-5, SHA-1, AES, PKEU, RNG and RC-4 encryption algorithms
- Multiple PCI interface support
  - 64-bit PCI 2.2 bus controller (up to 66 MHz, 3.3V I/O)
  - Flexibility to configure two 32-bit PCI controllers
- 166 MHz, 32-bit, 3.3V I/O, local bus with memory controller
- Integrated four-channel DMA controller
- Dual I²C, DUART, SPI
- Two 10/100 Ethernet controllers
- Interrupt controller
- IEEE 1149.1 JTAG test access port
- 1.2V core power supply (1.3V for 1 GHz operation) with 3.3V and 2.5V I/O
- 783-pin FC-BGA package

**Typical Applications**

- VPN and firewall routers
- Branch office and enterprise routers
- Enterprise-class storage
- Ethernet switching equipment
- General purpose embedded applications
- Business-class imaging equipment

**PowerQUICC Processors**

With more than 5,500 design wins in communications processors, Freescale's PowerQUICC processors are the ideal choice for your embedded networking and communication system needs.

To learn more about Freescale's communications and networking embedded solutions, visit us on the web: **www.freescale.com/powerquicc**

**Learn More:** For current information about Freescale products and documentation, please visit **www.freescale.com**



Document Number: MPC8541EFS
REV 7

# MPC8540 PowerQUICC™ III Processor

## Overview

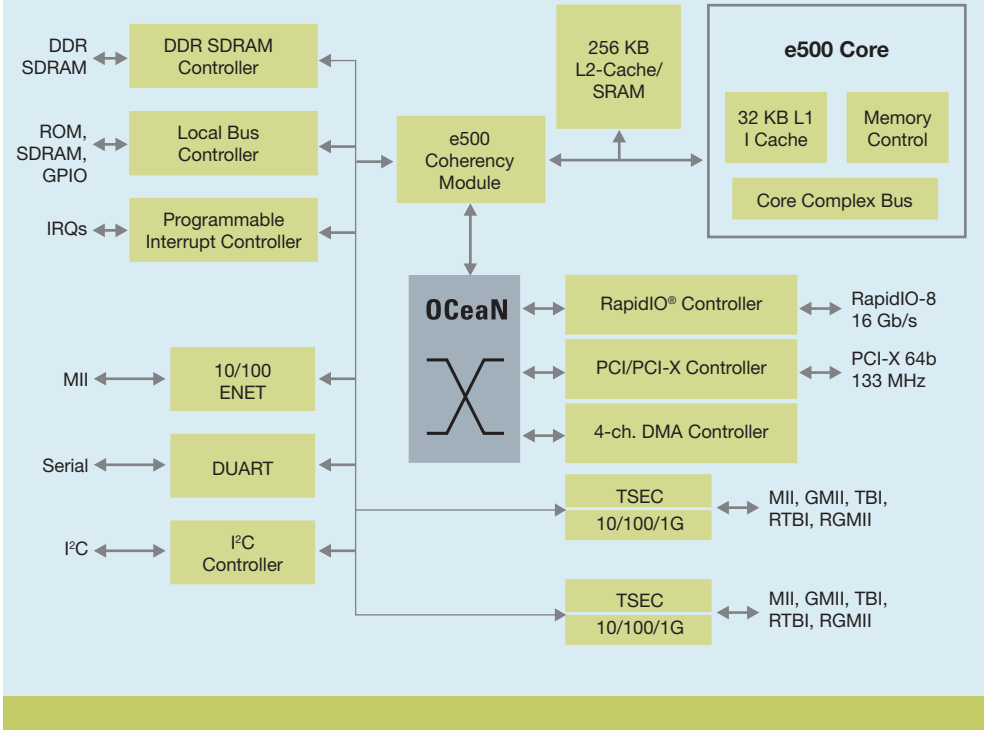
Addressing the need for higher compute density and lower system cost, the Freescale MPC8540 PowerQUICC™ III integrated communications processor, built on Power Architecture™ technology, is designed to provide an exceptionally high level of performance and integration. Balancing processor performance with I/O system throughput, the MPC8540 is a powerful control element for network routers and switches, storage subsystems, telecommunications systems and imaging devices.

## Innovative Technology

The MPC8540 processor integrates two 10/100/1000 Ethernet controllers (with support for jumbo frames), a 10/100 Ethernet controller, a 64-bit PCI/PCI-X controller operating at up to 133 MHz, an 8-bit 500 MHz parallel RapidIO® controller, a DDR memory controller, a four-channel DMA, a multi-channel interrupt controller and a DUART serial interface. Its high level of integration means simplified board design, low power consumption and a fast time to market solution for customers.

The MPC8540 integrates the e500 core, 256 KB of on-chip L2 cache and the revolutionary on-chip, non-blocking, crossbar switch fabric on-chip network (OCeaN), allowing for full duplex port connections and independent per-port transaction queuing and flow control.

MPC8540 Block Diagram




## Platform Architecture

Using a system-on-chip (SoC) platform that balances MIPS, watts, packet performance and cost, Freescale has created a flexible platform architecture enabling multiple products to be derived from an easily integrated IP.

The high-performance e500 core, built on Power Architecture technology, provides unprecedented levels of hardware and software debug support. The e500 core spans Freescale's processor families of ASSPs for networking, communications, automotive and consumer applications.

| PowerQUICC™ III Processor Family | MPC8541E | MPC8540 | MPC8555E | MPC8560 |
|---|---|---|---|---|
| Core | e500 | e500 | e500 | e500 |
| I-Cache/D-Cache (KB) | 32/32 | 32/32 | 32/32 | 32/32 |
| Integrated L2 Cache (KB) | 256 | 256 | 256 | 256 |
| Integrated Security Engine | Yes | - | Yes | - |
| Fast Communications Controllers | - | - | 3 | 3 |
| Serial Communications Controllers | - | - | 3 | 4 |
| Ethernet (10/100 only) | 2 | 1 | Up to 2 | Up to 3 |
| Ethernet (10/100/1000) | 2 | 2 | 2 | 2 |
| $I^2C$ Controller | 2 | 1 | 2 | 2 |
| UTOPIA Level II Ports | - | - | 2 | 2 |
| Multi-Channel HDLC | - | - | Up to 64 (QMC) | Up to 256 |
| PCI Interface | 2x 32-bit or 1x 64-bit | 1x 32/64-bit | 2x 32-bit or 1x 64-bit | 1x 32/64-bit |
| PCI-X Interface | - | Yes | - | Yes |
| RapidIO® Interface | - | Yes | - | Yes |

## RapidIO Interconnect Technology

As a founding member of the RapidIO Trade Association, Freescale has been driving the industry's adoption of this new high-performance switch fabric control plane interconnect. RapidIO technology offers significantly greater bandwidth, scalability and reliability than other interconnects used today, yet is compatible with existing PCI and CPU architectures. It has a flexible architecture that can easily adapt to changing industry needs without affecting existing infrastructure. RapidIO technology is an open standard governed by an industry body, designed specifically for embedded, networking and communications applications.

## Key Advantages

- High level of integration and performance
- Lower power consumption
- Fast time to market solution
- Enabled by RapidIO interconnect technology
- Flexible SoC platform
- Simplified board design compatibility
- Designed to integrate seamlessly with Freescale's networking, security and communications processors
- Compatible with a rich set of operating systems, compilers and development tools

## Technical Specifications

- High-performance embedded e500 core available from 667 MHz to 1 GHz
  - 32-bit, dual-issue, superscalar, seven-stage pipeline
  - 2310 MIPS at 1 GHz (estimate Dhrystone 2.1)
  - 32 KB L1 data and 32 KB L1 instruction cache with line locking support
  - 256 KB on-chip L2 cache with direct mapped capability
  - Enhanced hardware and software debug support
  - Memory management unit (MMU)
  - SIMD extension with single precision floating point
- Two TSECs supporting 10/100/1000 Mbps Ethernet with two GMII/TBI/RGMII interfaces
- DDR SDRAM memory controller
  - 166 MHz, 64-bit, 2.5V I/O
  - Full ECC support
- RapidIO controller—500 MHz, 8-bit, LVDS I/O
- PCI, PCI-X controller
  - PCI 2.2 and PCI-X 1.0 compatible
  - 64- or 32-bit PCI from 16 to 66 MHz
  - 64-bit PCI-X support up to 133 MHz
  - Host and agent mode support
- Integrated 4-channel DMA controller
- Local bus with memory controller—166 MHz, 32-bit, 3.3V I/O
- Interrupt controller
- IEEE® 1149.1 JTAG test access port
- 1.2V core power supply (1.3V for 1 GHz operation) with 3.3V and 2.5V I/O
- 783-pin FC-BGA package

**Learn More:** For current information about Freescale products and documentation, please visit **www.freescale.com**.



Document Number: MPC8540FACT
REV 8

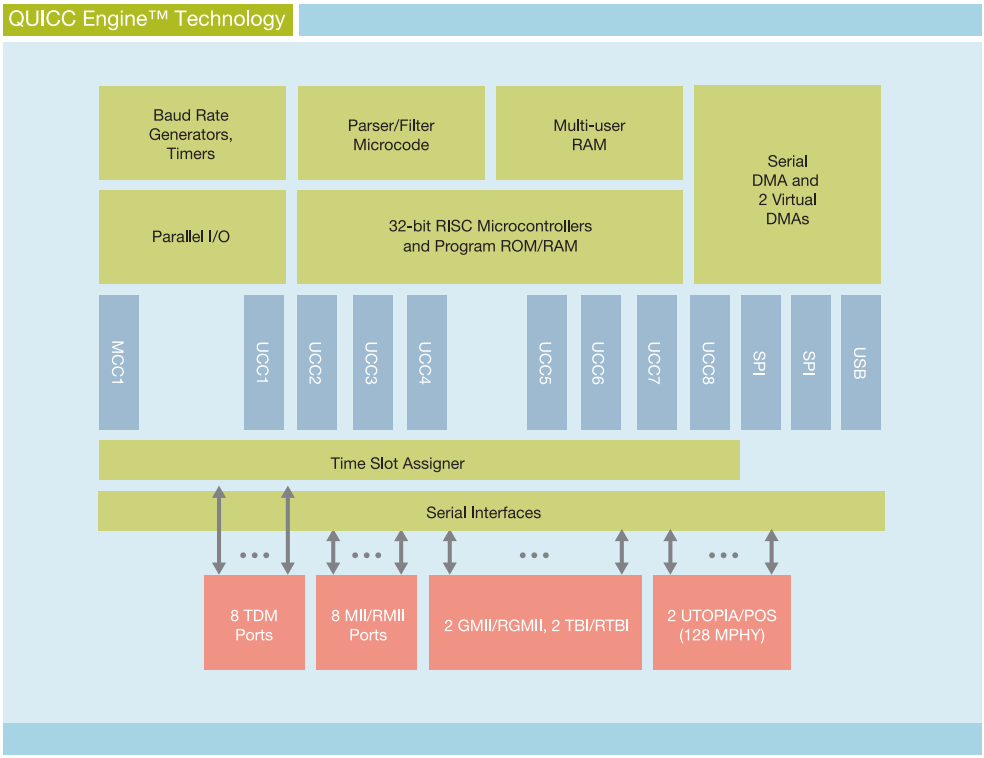
# Introducing Freescale's QUICC Engine™ Technology

## Overview

The QUICC Engine™ technology is an evolutionary step forward for Freescale Semiconductor's Communications Processor Module (CPM), a hallmark of the PowerQUICC™ family of communications processors built on Power Architecture™ technology. The QUICC Engine features a scalable number of embedded RISC engines that provide a range of performance points that cover customer premises equipment to the edge of the network, and in some instances, to the core of the network.

The initial QUICC Engine includes two optimized RISC processors, each initially scaling up to 500 MHz and supporting a wide range of protocols, while providing high data aggregate throughput of 1.2 Gbps interworking. In addition, Freescale plans to expand its shrink-wrapped protocol software support with further enhancements that include interworking, switching, parsing and IP forwarding, as well as improvements in Freescale's existing termination suite of protocol support. The QUICC Engine supports OC-12 to Gigabit Ethernet interworking throughput of 1.2 Gbps (2.34 Mpps), or in excess of 2 Gbps Layer 2 termination (3.9 Mpps) based on 64 byte packets.

Eight unified communications controllers (UCCs) provide support for Fast Ethernet, Gigabit Ethernet, high-level data link control (HDLC) and asynchronous transfer mode (ATM)/Packet over Sonet (POS) at up to OC-12 speeds. Eight time-division multiplexers (TDMs) enable connection to eight T1/E1 or eight clear channel T3/E3 lines. In addition to the UCCs, the QUICC Engine can support multiple multi-channel communications controllers (MCCs), although only one is offered today. The QUICC Engine allows for exceptional flexibility and includes an integrated Ethernet L2 switch, as well as a host of advanced protocol support.




To simplify the transition from current PowerQUICC designs, the advanced QUICC Engine technology maintains a high degree of software compatibility with previous-generation PowerQUICC designs. This backward compatibility helps to ease migration issues, reduce development costs and speed time to market.

The QUICC Engine technology also supports direct memory access via low latency serial direct memory access controllers, which allows it to connect to SDRAM and DDR memory support. This provides quick access to low-latency memory for parameters, buffer descriptors and data.

QUICC Engine technology is designed to handle a wide range of communications interfaces supporting a combination of ATM, POS, Ethernet, HDLC and transparent communications protocols, such as MII, RMII, GMII, RGMII, TBI, RTBI, NMSI, UTOPIA, UTOPIA MPHY, POS-PHY, TDM, UART, BISYNC, serial peripheral interface (SPI) and Universal Serial Bus (USB) interface (USB 2.0 full-/low-speed compatible).

QUICC Engine technology incorporates many advanced features that make it suitable for today's and tomorrow's broadband wired and wireless access equipment, as well as small and medium enterprise networking equipment. Target applications include multi-tenant units (MTUs), digital subscriber line access multiplexers (DSLAMs), wireless base stations, multi and fixed subscriber access nodes, multi-service provisioning platforms and routers.

freescale semiconductor

## Typical Applications

- DSL infrastructure
  - DSLAMs
  - MTUs
- Wireless infrastructure
  - Base transceiver station (BTS)
  - Base station controller (BSC)
  - Radio network controller (RNC)
  - NodeB
- Small and medium enterprise (SME) routers
  - Intrusion detection/protection system (IDS/IPS)
  - Secure VPN
  - Firewall
- Add/drop multiplexers and digital cross connects
- Integrated voice routers and digital IP-based private automatic branch exchange (PABX)
- Multi-service access nodes (MSAN)
- Passive optical networks (PON)
- IEEE® 802.16 WiMAX Super Access points and base stations
- Industrial and general purpose networking

## Technical Specifications

- QUICC Engine operating at 200 MHz to 500 MHz
- Two 32-bit RISC controllers for flexible support of the communications peripherals
  - Enhancements in the RISC microarchitecture
  - Improved instruction set
  - Multiple hardware accelerators
  - Pipelined packet processing
  - High level of tolerance to maximum latency accesses to memory
  - Deep programmable first in, first outs (FIFOs)
  - QUICC Engine frequency is independent of the system bus frequency
  - Arbitration mechanism is fully optimized for communications protocols and interfaces
- Serial DMA channel for receive and transmit on all serial channels
- QUICC Engine peripheral request interface for Integrated Security, PCI, IEEE Std 1588™
- Eight unified communications controllers supporting the following protocols and interfaces (Also see Table 1 for protocol comparison.):
  - 10/100/1000 Mbps Ethernet
  - Support for IEEE Std 1588 protocol
  - ATM SAR supporting up to 622 Mbps per second AAL5, AAL2, AAL1, AAL0, TM 4.0 CBR, VBR, UBR traffic types, up to 64 KB external connections
  - Inverse multiplexing for ATM (IMA)
  - POS up to 622 Mbps
  - Transparent
  - HDLC
  - Multi-link, multi-class PPP
  - HDLC bus
  - UART
  - BISYNC
  - User programmable FIFO size
  - One multi-channel communications controller (MCC), supporting:
    - 256 TDM channels
    - Transparent and HDLC mode per channel
    - Almost any combination of subgroups can be multiplexed to single or multiple TDM interfaces
  - Two UTOPIA/POS interfaces supporting up to 128 MPHY each
  - Eight TDM interfaces supporting
    - Aggregate bandwidth of 64 kbps per channel and 256 channels total
    - Maximum of 16 Mbps and 256 channels on a single TDM link
    - 2,048 bytes of SI RAM (1,024 entries)
    - Eight programmable strobes
    - Bit or byte resolution
    - Independent transmit and receive routing, frame synchronization
    - T1, CEPT, T1/E1, T3/E3, pulse-code modulation highway, ISDN primary/basic rate, Freescale interchip digital link (IDL) and user-defined TDM serial interfaces
  - Sixteen independent baud rate generators and 30 clock pins for supplying clocks to UCC, MCC serial channels
  - Four independent 16-bit timers that can be interconnected as two 32-bit timers
  - Two serial peripheral interface (SPI) ports can be configured as an Ethernet management port for management data input/output (MDIO), while the other can be configured for low-cost serial peripherals; the SPI also has a CPU mode that can be configured by the CPU and not through the QUICC Engine
  - Two SPIs—SPI2 is dedicated to Ethernet PHY management
  - USB interface (USB 2.0 full-/low-speed compatible)

| QUICC Engine™ and CPM Technical Comparison | | |
|---|---|---|
| **Feature/Capability** | **CPM** | **QUICC Engine** |
| Number of RISC Engines | 1 | 2 in 8360E family (scalable SoC methodology: 1, 2 and 4-core designs possible) |
| Asynchronous Clocking | No | Yes |
| Clock Frequency | Up to 333 MHz | Scales from 200 MHz to 500 MHz |
| DDR Memory Support | No | Yes |
| Layer 2 Support | Yes | Yes |
| Layer 3 Support | No | Yes |
| Major Interfaces/Protocols | 2 UTOPIA: OC-3 ATM, 31 MPHY each<br>3 MII/RMII: 10/100 Ethernet<br>8 TDMs | 2 UTOPIA: OC-12 ATM/POS, 128 MPHY each<br>8 MII/RMII: 10/100 Ethernet, 2 GMII: 10/100/1000 Ethernet<br>8 TDMs |
| Interworking | No | Yes, including forwarding, switching and parsing; offloads these tasks from CPU |
| Communication Peripheral Architecture | 2 MCCs: 128 channels of HDLC each<br>3 FCCs: ATM, Fast Ethernet, Transparent<br>4 SCCs: 10 Base-T, UART and other slow-speed serial interfaces | 1 MCC: 256 channels of HDLC<br>8 unified communications controllers (UCCs): ATM, Fast Ethernet, Gigabit Ethernet, Transparent and the slower SCC based protocols |
| Performance | Up to 700 Mbps Layer 2 termination | Up to 1.2 Gbps interworking (2.34 Mpps)<br>Up to 2 Gbps termination (3.9 Mpps) |
| User Configurability and Programmability | Not supported | Software configuration tools and drivers available **www.freescale.com/quiccengine** for Open QUICC Engine program overview |

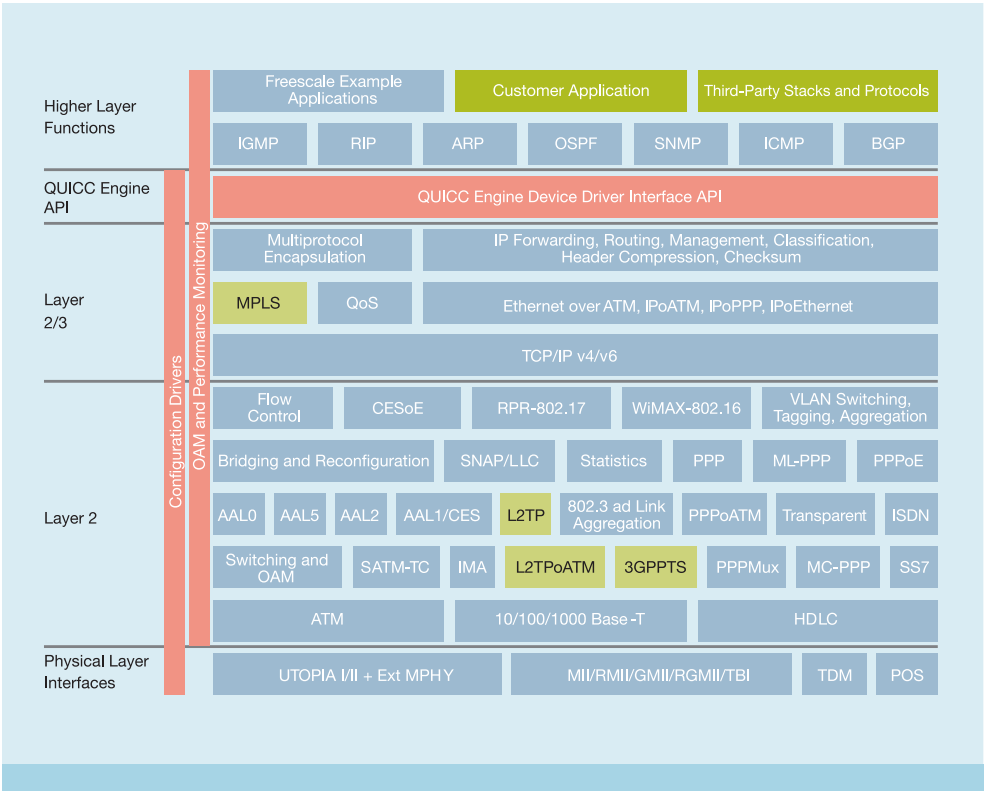
### Architectural Scalability through System-on-Chip Design Methodology

The QUICC Engine uses Freescale's scalable system-on-chip (SoC) design methodology, enabling a portable piece of technology that may be used in a variety of products in a variety of configurations. QUICC Engine technology performance scales by using a multi-RISC core-scaling factor that is able to run multiple tasks concurrently. In addition, it scales in terms of frequency and technology that also enables varying levels of performance.

For more cost-sensitive applications aimed at retail and customer premises equipment, the QUICC Engine can be configured as a single RISC or dual RISC communications engine. For higher performance access, infrastructure and edge applications, it can be configured as a dual RISC communications engine and has the capacity to scale to a multi-RISC core architecture. The initial QUICC Engine is designed to support dual RISC cores implemented on the MPC8360 PowerQUICC II Pro integrated communications processor.

Scalability also is available in terms of the number of UCCs and MCCs. The initial implementation offers eight UCCs and one MCC. However, with the flexibility of the SoC design methodology used for the QUICC Engine, these numbers can be scaled in both directions to support optimized mix and match of communications channels to give the right balance of price/performance, depending on the targeted application.

Software for Product Implementations of the QUICC Engine™ Technology



## Software Support

The QUICC Engine technology will build upon Freescale's shrink-wrapped software protocol support for PowerQUICC processors and provide enhancements for interworking, parsing, switching and forwarding. The QUICC Engine will also be supported by a full set of configurable driver software and initialization support.

Freescale also simplifies development and speeds time to market with the CodeWarrior® QUICC Engine Utility—a GUI tool that speeds and simplifies initialization and configuration of drivers and communications protocols managed by QUICC Engine technology. The tool provides an easy-to-use environment for handling common QUICC Engine initialization tasks. Key features include:

- Automatic protocol conflict notification
- Common default values
- Point-and-click protocol selection and implementation
- Immediate access to pertinent documentation via mouse-over functionality and drop-down menus

The QUICC Engine also has a wealth of third-party software support from Freescale's Design Alliance Program, including third-party protocol and signaling stack suppliers, real-time operating systems support and a variety of applications software support. All of this builds upon the existing industry-standard PowerQUICC family support program.

## Key Advantages

- High-performance, low-power and cost-effective communications processor solution
  - Convergence for packet-based networks
  - Compatibility with current PowerQUICC offerings
  - Cost-effective solution at the chip and system level
- Advanced QUICC Engine technology supporting a wide range of functionality
  - Interworking
  - Forwarding
  - Parsing
  - Switching
- DDR memory support interfaces
- Low risk of transitioning from legacy to IP-based systems
- Quick time to market enabled by software compatibility with current PowerQUICC offerings
- Low bill of material (BOM) cost

## Interworking

With the potential to offer three revenue streams from a single IP packet network, the triple play of voice, video and data is the goal of every telecom operator. IP is the key enabler, and in time, it will be universal. Until then, equipment has to interoperate between circuit- and packet-switched networks and between many standards and protocols. The interoperability between standard protocols is referred to as interworking.

The QUICC Engine technology supports ATM to Ethernet interworking, without CPU intervention in support of the industry standard RFC2684 specification. In addition, the QUICC Engine can support MC/MLPPP to Ethernet interworking. It is able to perform powerful table lookup functions including multiple fields from Layers 2 to 4 without CPU intervention.

In terms of performance, the dual-RISC QUICC Engine is designed to support a throughput of up to 1.2 Gbps interworking, or 2.34 Mpps based on 64 byte packets.

**Learn More:** For more information about QUICC Engine and products that incorporate it or other Freescale communications processor products, please visit **www.freescale.com/QUICCEngine**.



Document Number: BRQUICCENGINE
REV 5

freescale semiconductor

# MPC8360E PowerQUICC™ II Pro Family

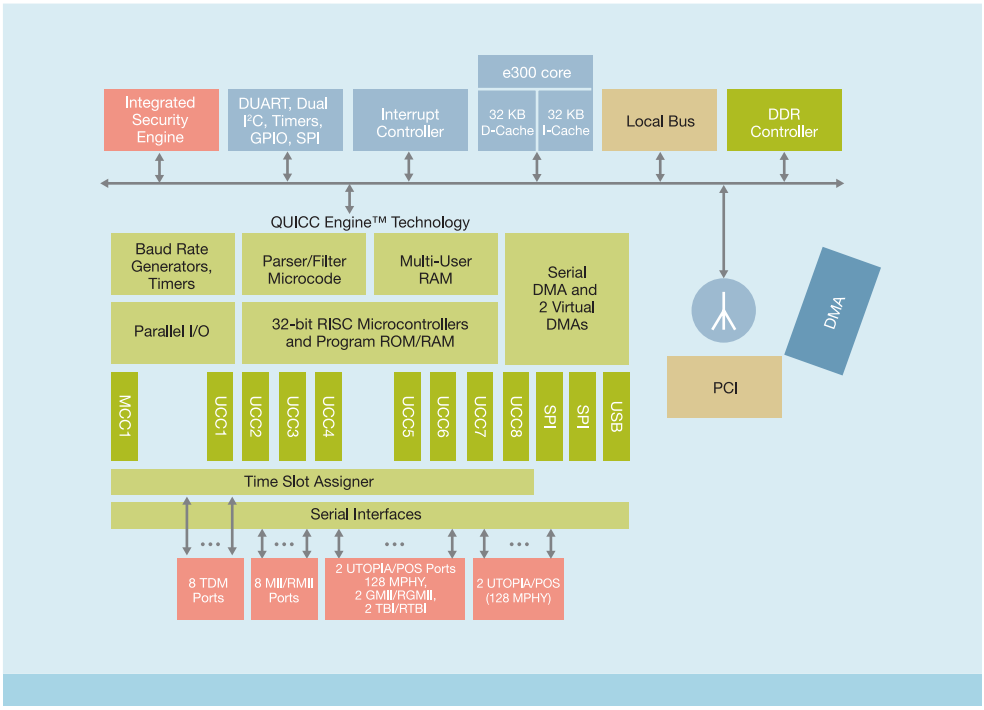
## Overview

Freescale Semiconductor's MPC8360E PowerQUICC™ II Pro family of integrated communications processors is a next-generation extension of the popular PowerQUICC II line containing Power Architecture™ technology. The MPC8360E family incorporates a next-generation communications engine, the QUICC Engine™, supporting a wide range of protocols, including Gigabit Ethernet, OC-12 asynchronous transfer mode (ATM)/ Packet over Sonet (POS), and IEEE® 1588 clock synchronization protocol. Additional enhancements include the e300 core, built on Power Architecture technology (an enhanced version of the 603e core with larger caches), scaling up to 667 MHz, up to two DDR memory controllers and the integrated security engine.

The MPC8360E PowerQUICC II Pro communications processor's advanced features make it suitable for today's and tomorrow's wired and wireless access equipment, as well as small and medium enterprise networking equipment. Target applications include multi-tenant units (MTUs), digital subscriber line access multiplexers (DSLAMs), wireless base stations, multi and fixed subscriber access nodes, add/drop multiplexers and routers.

The MPC8358E processor, a member of the MPC8360E PowerQUICC II Pro family, is pin-compatible with the MPC8360E. The MPC8358E offers a cost-effective, low-power processing solution that meets the performance requirements for broadband access applications such as small-to-medium enterprise (SME) routers, low-end DSLAMs, IP private automatic branch exchange (PABX) systems and industrial network equipment.

MPC8360E




## e300 System-on-a-Chip Platform

The MPC8360E PowerQUICC II Pro family is based on the e300 system-on-a-chip (SoC) platform. This makes it easy and fast to add or remove functional blocks and develop additional SoC-based family members for emerging markets. At the heart of the e300 SoC platform is Freescale's e300 core, built on Power Architecture technology. The e300 core is an enhanced version of the 603e core used in previous-generation PowerQUICC II processors. Enhancements include twice as much L1 cache (32 KB data cache and 32 KB instruction cache) with integrated parity checking and other performance-enhancing features. The e300 core is software-compatible with existing 603e core-based products.

freescale semiconductor

## Connectivity

The MPC8360E processor is designed to support a wide range of communications interfaces, such as MII, RMII, GMII, TBI, RTBI, NMSI, UTOPIA, POS and TDM. The dual 32-bit DDR memory controllers help to ensure high-speed memory access and a local system bus operating up to 133 MHz. Additional system connectivity is supplied by dual UART, dual inter-integrated circuit ($I^2C$), dual serial peripheral interface (SPI), PCI interfaces and Universal Serial Bus (USB) interface (USB 2.0 full/low speed compatible).

## Integrated Security

The MPC8360E and MPC8358E processors integrate the powerful security hardware block developed for Freescale's security coprocessor products. This on-chip security hardware block supports DES, 3DES, MD-5, SHA-1, AES and ARC-4 encryption algorithms, as well as a public key accelerator and an on-chip random number generator. It also supports single-pass encryption and authentication, as defined by IPsec, the IEEE® 802.11i standard and other security protocols.

## Typical Applications

- DSL infrastructure
  - DSLAMs
  - MTUs
- Wireless infrastructure
  - Base transceiver station (BTS)
  - Base station controller (BSC)
  - Radio network controller (RNC)
  - Node B
- Small and medium enterprise (SME) routers
  - Intrusion detection/protection system (IDS/IPS)
  - Secure VPN
  - Firewall
- Add/drop multiplexers and digital cross connects
- Integrated voice routers and digital IP-based private automatic branch exchange (PABX)
- Multi-service access nodes (MSAN)
- Industrial and general-purpose networking

## QUICC Engine

Freescale's QUICC Engine technology includes two optimized RISC processors supporting a wide range of protocols while providing high data throughput of up to 1.2 Gbps. Flexibility is provided by the eight unified communications controllers (UCCs) providing support for Fast Ethernet, Gigabit Ethernet, high-level data link control (HDLC) and ATM/POS at up to OC-12 speeds. The MPC8360E and MPC8358E support connectivity up to eight T1/E1s. The MPC8360E supports eight TDMs and the MPC8358E supports four TDMs, with each TDM capable of supporting a clear channel T3/E3. One multi-channel communications controller (MCC) on the MPC8360E supports up to 256 x 64 kbps HDLC or transparent channels.

To simplify the transition from current PowerQUICC designs, the advanced QUICC Engine technology maintains a high degree of software compatibility with previous-generation PowerQUICC processor-based designs. This helps ease migration issues, reduce development costs and speed time to market.

The QUICC Engine technology builds upon the PowerQUICC shrink-wrapped software protocol support and provides enhancements in terms of interworking, parsing, switching and forwarding. A full set of configurable driver software and initialization support will also be available.

## Interworking

With the potential to offer three revenue streams from a single IP packet network, the triple play of voice, video and data is the goal of every telecom operator. IP is the key enabler, and in time, it will be universal. Until then, equipment has to interoperate between circuit- and packet-switched networks and between many standards and protocols. The interoperability between standard protocols is referred to as interworking.

The QUICC Engine block supports ATM-to-Ethernet interworking without CPU intervention in support of the industry-standard RFC2684 specification. In addition, it can support MC/MLPPP to Ethernet interworking.

It is able to perform powerful table lookup functions including multiple fields from Layers 2 to 4 without CPU intervention.

## Key Advantages

- High-performance, low-power and cost-effective communications processor solution
  - Convergence for packet-based networks
  - Compatibility with current PowerQUICC offerings
  - Cost-effective solution at the chip and system level
- Advanced QUICC Engine technology supporting a wide range of protocols and associated interworking
- DDR memory support—one 64-bit or 2 x 32-bit interfaces
- Low risk when transitioning from legacy to IP-based systems
- Quick to market enabled by software compatibility
- Low bill of material (BOM) cost

## Product Family Highlights

- e300 core, built on Power Architecture technology (enhanced version of the 603e core with larger caches)
- DDR memory controller, 1 x 32/64-bit or 2 x 32-bit, up to 333 MHz
- QUICC Engine technology with eight communications interfaces supporting Fast Ethernet, Gigabit Ethernet, ATM, POS, HDLC, asynchronous HDLC, UART and Transparent protocols
- 32-bit PCI interface
- 32-bit local bus interface
- Optional integrated security

## Technical Specifications

- e300 Power Architecture core operating from 266 MHz to 667 MHz
  - 32-bit, high-performance superscalar core
  - 1,261 MIPS at 667 MHz; 503 MIPS at 266 MHz
  - Double-precision floating point, integer, load/store, system register and branch processor units
  - 32 KB data and 32 KB instruction cache with line-locking support
- QUICC Engine technology initially operating up to 500 MHz
  - Two 32-bit RISC controllers for flexible support of the communications peripherals
  - Serial DMA channel for receive and transmit on all serial channels
  - QUICC Engine peripheral request interface for Integrated Security, PCI, IEEE® 1588 clock synchronization
  - Eight UCCs supporting the following protocols and interfaces:
    - 10/100/1000 Mbps Ethernet
    - IEEE 1588 hardware timestamping
    - ATM SAR supporting AAL5, AAL2, AAL1, AAL0, TM 4.0 CBR, VBR, UBR traffic types, up to 64 KB external connections
    - Inverse multiplexing for ATM (IMA)
    - POS up to 622 Mbps
    - Transparent
    - HDLC
    - Multi-link, multi-class PPP
    - HDLC bus
    - UART
    - BISYNC
  - One multi-channel communications controller (MCC), supporting:
    - 256 TDM channels
    - Transparent and HDLC mode per channel
    - Support for Signaling System Number 7 (SS7)
    - Almost any combination of subgroups can be multiplexed to single or multiple TDM interfaces
  - Two UTOPIA/POS interfaces supporting up to 128 multi-PHY each
  - Two serial peripheral interfaces (SPIs)
  - Eight TDM interfaces, supporting:
    - Aggregate bandwidth of 64 kbps and 256 channels
    - Maximum of 16 Mbps and 256 channels on a single TDM link
    - 2,048 bytes of SI RAM (1,024 entries)
    - Eight programmable strobes
    - Bit or byte resolution
    - Independent transmit and receive routing, frame synchronization
    - T1, CEPT, T1/E1, T3/E3, pulse-code modulation highway, ISDN primary/basic rate, Freescale interchip digital link (IDL) and user-defined TDM serial interfaces
  - 16 independent baud rate generators
  - Four independent 16-bit timers that can be interconnected as two 32-bit timers
  - Two SPI ports that can be configured as an Ethernet management port for management data input/output (MDIO), while the other can be configured for cost-effective serial peripherals; the SPI also has a CPU mode that can be configured by the CPU and not through the QUICC Engine
- USB interface (USB 2.0 full/low speed compatible)
- DDR memory controller
  - Programmable timing supporting DDR-1/2 SDRAM
  - 2 x 32-bit (MPC8360E only) or 1 x 32/64-bit data interface; up to 333 MHz data rate
  - Four banks of memory, each up to 1 GB
  - Full ECC support
- PCI interface
  - One 32-bit PCI 2.3 bus controller (3.3V I/O; up to 66 MHz)
- Integrated security (MPC8360E and MPC8358E only)
  - Public key execution (RSA and Diffie-Hellman)
  - Data encryption standard execution (DES and 3DES)
  - Advanced encryption standard (AES) execution
  - ARC-4 execution (RC4-compatible algorithm)
  - Message digest execution (SHA, MD5, HMAC)
  - Random number generation (RNG)
- Local bus controller
  - Multiplexed 32-bit address and data operating up to 133 MHz
  - 32-, 16- and 8-bit port sizes controlled by on-chip memory controller
- Dual UART (DUART)
- Dual $I^2C$ interfaces (master or slave mode)
- Four-channel DMA controller
- General-purpose parallel I/O
- IEEE 1149.1 JTAG test access port
- Package option: 37.5 mm X 37.5 mm 740 TBGA (MPC8360E, MPC8358E); 29 mm x 29 mm 668 PBGA (MPC8358 only)
- Process technology: 130 nm CMOS
- Voltage: 1.2V core voltage with 3.3V, 2.5V and 1.8V I/O

| MPC8360E Family Features Comparison | MPC8358E | MPC8360E |
|---|---|---|
| CPU | e300 | e300 |
| • I-Cache/D-Cache (KB) | 32/32 | 32/32 |
| • Available clock frequencies | Up to 400 MHz | Up to 667 MHz |
| QUICC Engine™ | 2 x RISC core | 2 x RISC core |
| • Available clock frequencies | Up to 400 MHz | Up to 500 MHz |
| • Ethernet (Supports IEEE® 1588 hardware timestamping) | Up to 2 x 10/100/1000<br>Up to 6 x 10/100 | Up to 2 x 10/100/1000<br>Up to 8 x 10/100 |
| • ATM | 1 x UTOPIA L2 | 2 x UTOPIA L2 |
| ○ MPHY | Single 31/128 port | 128 per UTOPIA port |
| • POS** | Yes | Yes |
| • TDM | Up to 4 TDM interfaces<br>Up to 256 channels at<br>16 Mbps on a single interface<br>Up to 4 clear channel T3/E3 | Up to 8 TDM interfaces<br>Up to 256 channels at<br>16 Mbps on a single interface<br>Up to 8 clear channel T3/E3 |
| Memory controller | 1 x 32/64-bit DDR-1/2 with ECC<br>Up to 266 Mbps data rate | 1 x 32/64-bit or 2 x 32-bit DDR-1/2 with ECC<br>Up to 333 Mbps data rate |
| Local bus | Yes | Yes |
| PCI | One 32-bit (up to 66 MHz) | One 32-bit (up to 66 MHz) |
| Integrated security engine* | Yes | Yes |
| DUART | Yes | Yes |
| $I^2C$ controller | 2 | 2 |
| SPI | 2 | 2 |
| USB | Yes | Yes |
| Interrupt controller | Yes | Yes |
| Package options | 740 TBGA<br>668 PBGA | 740 TBGA |

*"E" in the product name designates encryption acceleration through an integrated security engine. MPC8360 and MPC8358 processor versions without integrated security engines are available.

**The microcode for POS will be made available in Q1 2008. Consult your Freescale Representative for more information.

**Learn More:** For more information about the MPC8360E Family and other Freescale communications processor products, please visit **www.freescale.com/powerquicc**.



Document Number: MPC8360EFS
REV 5

# MPC8349E PowerQUICC™ II Pro

## Overview

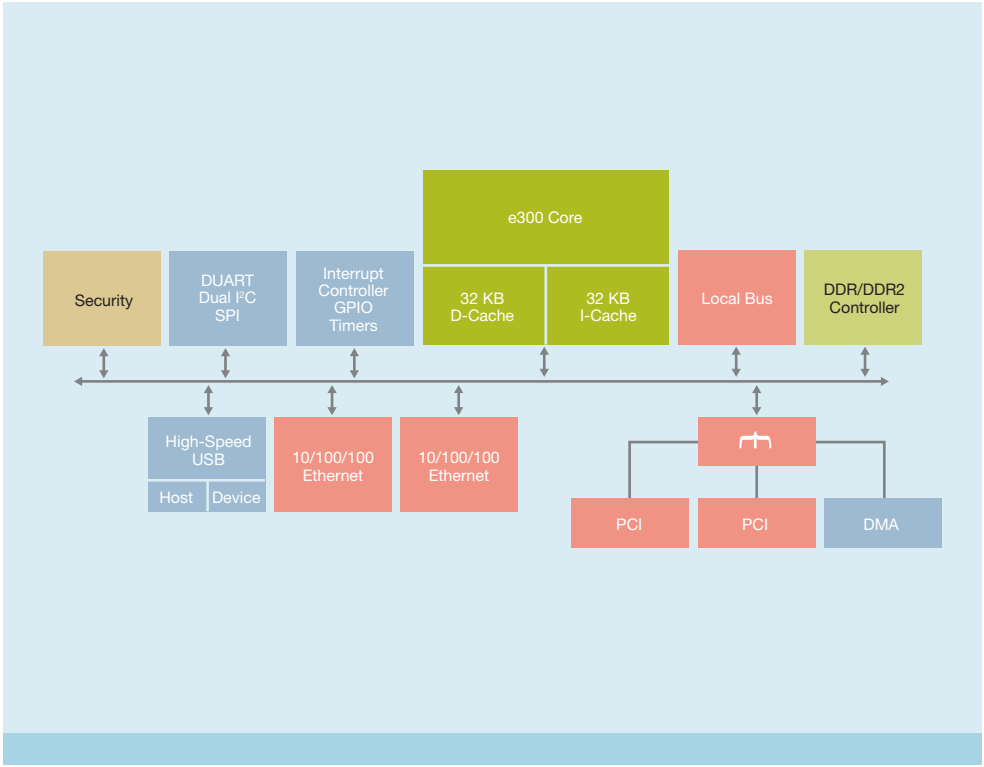
Freescale Semiconductor's MPC8349E PowerQUICC™ II Pro family of integrated communications processors is a next-generation extension of the popular PowerQUICC II line. Based on a system-on-chip (SoC) architecture, the MPC8349E PowerQUICC II Pro family integrates the enhanced e300 core, built on Power Architecture™ technology, and advanced features, such as DDR/DDR2 memory, Dual Gigabit Ethernet, Dual PCI and High-Speed USB controllers. With clock speeds scaling to 667 MHz, the MPC8349E family of processors offers the highest performing PowerQUICC II Pro devices available.

The MPC8349E PowerQUICC II Pro family is designed to provide a cost-effective, highly integrated control processing solution that addresses the emerging needs of networking, communications and pervasive computing applications. MPC8349E processors can be used in applications such as Ethernet routers and switches, wireless LAN (WLAN) equipment, network storage, home network appliances, industrial control equipment, copiers, printers and other imaging systems.

## e300 SoC Platform

The MPC8349E PowerQUICC II Pro family is based on the e300 SoC platform—making it easy and fast to add or remove functional blocks and develop additional SoC-based family members targeting emerging market requirements. The e300 core, built on Power Architecture technology, is an enhanced version of the 603e core used in previous generations. Enhancements include twice as much L1 cache (32 KB data cache and 32 KB instruction cache) with integrated parity checking, and other performance-enhancing features. The e300 core is completely software-compatible with existing 603e core-based products.

MPC8349E Block Diagram



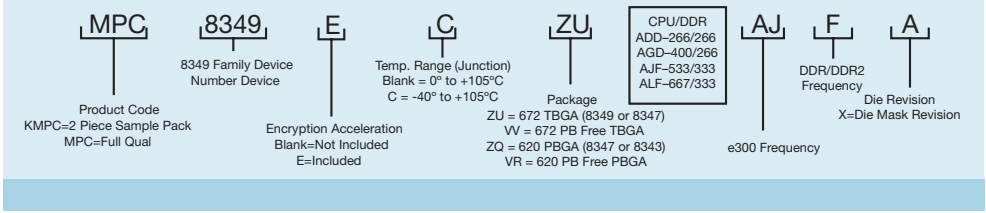

## Integrated Security

The MPC8349E family features a powerful integrated security engine derived from Freescale's security coprocessor product line. The MPC8349E family's security engine supports DES, 3DES, MD-5, SHA-1, AES and ARC-4 encryption algorithms, as well as a public key accelerator and an on-chip random number generator. The security engine is capable of single-pass encryption and authentication, as required by IPsec, IEEE® 802.11i standard and other security protocols.

## Key Advantages

- Exceptional price/performance for highly integrated, cost-sensitive applications
- Processor speeds up to 667 MHz
- High level of integration enabling simplified board design
- Flexible SoC platform for market-optimized designs and fast time to market
- Dual Gigabit Ethernet and Dual PCI interfaces

freescale semiconductor




| MPC8349E* PowerQUICC™ II Pro Family | MPC8349E* | MPC8347E* | MPC8343E* |
|---|---|---|---|
| Core | e300 | e300 | e300 |
| I-Cache/D-Cache (KB) | 32/32 | 32/32 | 32/32 |
| Frequencies | Up to 667 MHz | Up to 667 MHz | Up to 400 MHz |
| Memory controller | 64-/32-bit DDR/DDR2 | 64-/32-bit DDR/DDR2 | 64-/32-bit DDR/DDR2 |
| Local bus | Yes | Yes | Yes |
| PCI interface | Two 32-bit (up to 66 MHz) or one 64-bit | One 32-bit (up to 66 MHz) | One 32-bit (up to 66 MHz) |
| Ethernet | Dual 10/100/1000 | Dual 10/100/1000 | Dual 10/100/1000 |
| High-Speed USB | Dual: host and device/OTG | Dual: host and device/OTG | Dual: host and device/OTG |
| Integrated security | Available | Available | Available |
| DUART | Yes | Yes | Yes |
| I²C controller | Dual | Dual | Dual |
| SPI | Yes | Yes | Yes |
| Interrupt controller | Yes | Yes | Yes |
| Package options | 35 mm x 35 mm TBGA | 35 mm x 35 mm TBGA<br>29 mm x 29 mm PBGA | 29 mm x 29 mm PBGA |

*Note: E in the product name designates encryption acceleration through an integrated security engine. MPC8349, MPC8347 and MPC8343 processor versions without integrated security engines are available.

### Product Family Highlights

- e300 core, built on Power Architecture technology (enhanced version of 603e core with larger caches)
- DDR/DDR2 memory controller, up to 333 MHz
- Dual 10/100/1000 Ethernet channels
- Dual 32-bit PCI interfaces (configurable as one 64-bit PCI interface)
- Dual High-Speed USB controllers
- Optional integrated security engine

### Typical Applications

- Ethernet routers and switches
- Wireless LAN
- Copier/printer/imaging
- Home gateways/media gateways
- Network-attached storage (NAS)
- Industrial control
- Line cards

### Technical Specifications

- e300 core, built on Power Architecture technology, operating from 266 MHz to 667 MHz
  - 32-bit, high-performance superscalar core
  - 1260 MIPS @ 667 MHz; 504 MIPS @ 266 MHz
  - Double-precision floating point, integer, load/store, system register and branch processor units
  - 32 KB data and 32 KB instruction cache with line locking support
- DDR/DDR2 memory controller
  - Programmable timing supporting DDR/DDR2 SDRAM
  - 32- or 64-bit data interface; up to 333 MHz data rate
  - Four banks of memory, each up to 1 GB
  - Full ECC support
- Dual PCI interfaces
  - Two 32-bit PCI 2.2 bus controllers (3.3V I/O; each controller can operate up to 66 MHz)
  - Flexibility to configure the two PCI controllers as a single 64-bit PCI controller
- Dual 10/100/1000 Ethernet controllers
  - 1000 Mbps IEEE 802.3 GMII/RGMII, 802.3z TBI/RTBI, full-duplex
  - 10/100 Mbps IEEE 802.3 MII full and half-duplex
  - Station management interface for control and status
  - Jumbo frame support up to 9.6 KB
- Embedded security engine
  - Public key execution (RSA and Diffie-Hellman)
  - Data encryption standard execution (DES and 3DES)
  - Advanced encryption standard (AES) execution
  - ARC Four execution (RC4-compatible algorithm)
  - Message digest execution (SHA, MD5, HMAC)
  - Random number generation (RNG)
- Dual High-Speed USB 2.0 controllers
  - Support for device, host and On-the-Go (OTG) functionality
  - High-speed (480 Mbps), full-speed (12 Mbps) and low-speed (1.5 Mbps) operation
- Local bus controller
  - Multiplexed 32-bit address and data operating up to 133 MHz
  - 32-, 16- and 8-bit port sizes controlled by on-chip memory controller
- Dual UART (DUART)
- Dual I²C interfaces (master or slave mode)
- Four-channel direct memory access (DMA) controller
- Serial peripheral interface
- General-purpose parallel input/output
- IEEE 1149.1 JTAG test access port
- Package options: 35 mm x 35 mm TBGA and 29 mm x 29 mm PBGA (both with 1 mm pitch)
- Process technology: 130 nm CMOS
- Voltage: 1.3V core voltage for 667 MHz

**Learn More:** For current information about Freescale products and documentation, please visit **www.freescale.com**.

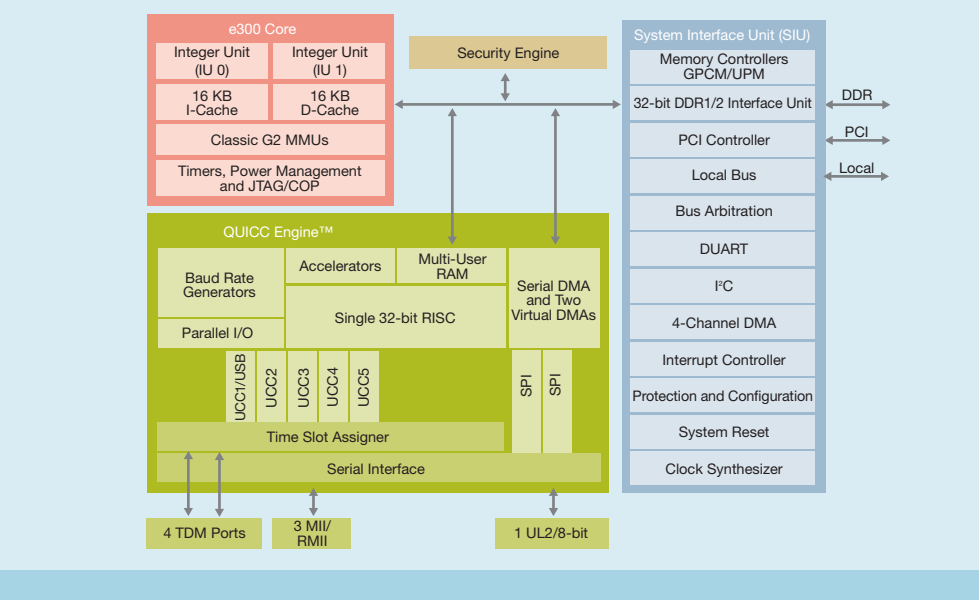


Document Number: MPC8349FS
REV 5

# MPC8323E Family PowerQUICC™ II Pro

The cost-effective MPC8323E communications processor family that includes the MPC8323E, MPC8323, MPC8321E and MPC8321 meets the requirements of several small office/home office (SOHO), access, IP services and industrial control applications. It provides better CPU performance, additional functionality and faster interfaces than current PowerQUICC™ II processors while addressing important time to market, price, power consumption and board space requirements.

## MPC8323E Block Diagram




### Core Complex

The MPC8323E family incorporates a unique configuration of the e300 (MPC603e-based) core. This configuration has been designed to include dual integer units as well as a modified multiply instruction. These architectural enhancements enable more efficient operations to be executed in parallel, resulting in a significant performance improvement. The e300 core complex also includes 16 KB of L1 instruction and data caches and on-chip memory management units (MMUs).

### QUICC Engine™ Technology

A new single-RISC version of the QUICC Engine subsystem communications engine forms the heart of the networking capability of the MPC8323E. The QUICC Engine subsystem contains several peripheral controllers and a single 32-bit reduced instruction set computing (RISC) controller. Unique microcode packages provide support for NAT, Firewall, IPSec and Advanced Quality of Service (QoS). Protocol support is provided by the main workhorses of the device—the unified communication controllers (UCCs).

Each of the five UCCs can support a variety of communication protocols:

- 10/100 Mbps Ethernet
- Asynchronous transfer mode (ATM) support up to OC-3 speeds
- Serial ATM
- Multi-physical layer (PHY) ATM
- Time division multiplexing (TDM)

In addition, the QUICC Engine subsystem can also support a Universal Test and Operations PHY Interface for ATM (UTOPIA) level 2 for up to 31 multi-PHY. UCC can also support USB 2.0 (full/low speed).

### Hardware Security Engine

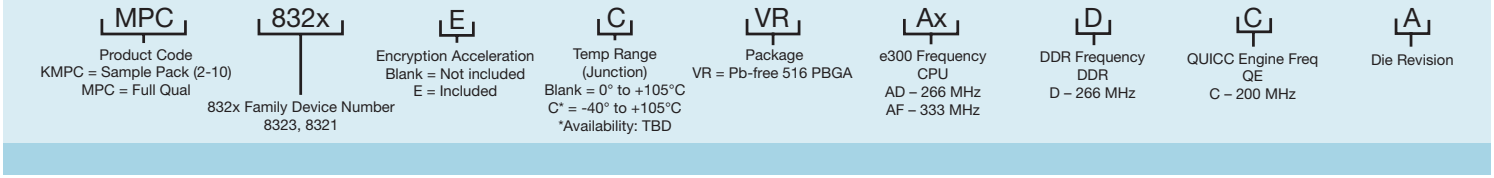
The security engine on the MPC8323E and MPC8321E allows CPU-intensive cryptographic operations to be off-loaded from the main CPU core. The security-processing accelerator provides hardware acceleration for the DES, 3DES, Advanced Encryption Standard (AES), Secure Hash Algorithm (SHA)-1 and MD-5 algorithms.

### System Interface Unit

The MPC8323E family also includes a 32-bit double data rate (DDR1/DDR2) memory controller, a 32-bit peripheral component interconnect (PCI) controller, a 16-bit local bus and four direct memory access (DMA) channels.

In summary, the MPC8323E family provides users with a highly integrated, fully programmable communications processor for use in many SOHO, access, IP services and industrial control applications. This helps ensure that a cost-effective system solution can be quickly developed and will offer flexibility to acommodate new standards and evolving system requirements.

freescale semiconductor




| MPC8323E PowerQUICC™ II Pro Family | MPC8323E | MPC8323 | MPC8321E | MPC8321 |
|---|---|---|---|---|
| Core | e300 | e300 | e300 | e300 |
| I-Cache/D-Cache | 16/16 | 16/16 | 16/16 | 16/16 |
| Floating Point Unit | No | No | No | No |
| Core Frequency | 266/333 | 266/333 | 266/333 | 266/333 |
| QUICC Engine™ Subsystem | Single RISC | Single RISC | Single RISC | Single RISC |
| Memory Controller | 32-bit DDR1/DDR2 | 32-bit DDR1/DDR2 | 32-bit DDR1/DDR2 | 32-bit DDR1/DDR2 |
| Local Bus | 16-bit; up to 66 MHz | 16-bit; up to 66 MHz | 16-bit; up to 66 MHz | 16-bit; up to 66 MHz |
| PCI Interface | 32-bit; up to 66 MHz | 32-bit; up to 66 MHz | 32-bit; up to 66 MHz | 32-bit; up to 66 MHz |
| Ethernet | (3) 10/100; MII/RMII | (3) 10/100; MII/RMII | (3) 10/100; MII/RMII | (3) 10/100; MII/RMII |
| USB 2.0 | Full/low speed | Full/low speed | Full/low speed | Full/low speed |
| Integrated Security | Yes | No | Yes | No |
| DUART | Yes | Yes | Yes | Yes |
| $I^2C$ Controller | Yes | Yes | Yes | Yes |
| SPI | Dual | Dual | Dual | Dual |
| Interrupt Controller | Yes | Yes | Yes | Yes |
| ATM | Yes | Yes | No | No |
| Package | 516-PBGA | 516-PBGA | 516-PBGA | 516-PBGA |

## Typical Application

- Residential gateways
- SOHO networking
- VPN routers
- Access points
- DSLAM line cards
- Industrial control
- Test and measurement equipment

## MPC8323E Features

- High-performance, low power and cost-effective communications processor
- The e300 core built on Power Architecture™ technology with dual integer units enables more efficient operations to be conducted in parallel, resulting in significant performance improvement
- The single-RISC QUICC Engine communications module offers a future-proof solution for next-generation designs by supporting programmable protocol termination and network interface termination to meet evolving protocol standards
- Single platform architecture supports the convergence of IP packet networks and ATM networks
- DDR1/DDR2 memory controller—one 32-bit interface at up to 266 MHz
- Peripheral interfaces such as 32-bit, 66 MHz PCI, 16-bit, 66 MHz local bus interface and USB 2.0 (full/low speed)
- Security engine provides acceleration for control and data plane security protocols
- High degree of software compatibility with previous-generation PowerQUICC processor-based designs for backward compatibility and easier software migration

## QUICC Engine Technology

- Single 32-bit RISC controller for flexible support of communications peripherals
- Serial DMA channel for receive and transmit on all serial channels
- Five UCCs supporting the following interfaces (not all of them simultaneously):
  - ATM protocol through UTOPIA interface supporting 31 multi PHYs
  - HDLC/transparent up to 70 Mbps full duplex
  - QUICC multi-channel controller (QMC) for 64 time division multiplexing (TDM) channels

The UCCs are similar to the PowerQUICC II peripherals: serial communications controller (SCC) (BISYNC, UART and HDLC bus) and fast serial communications controller (FCC) (fast Ethernet, HDLC, transparent and ATM).

**Learn More:** For current information about Freescale products and documentation, please visit **www.freescale.com**.



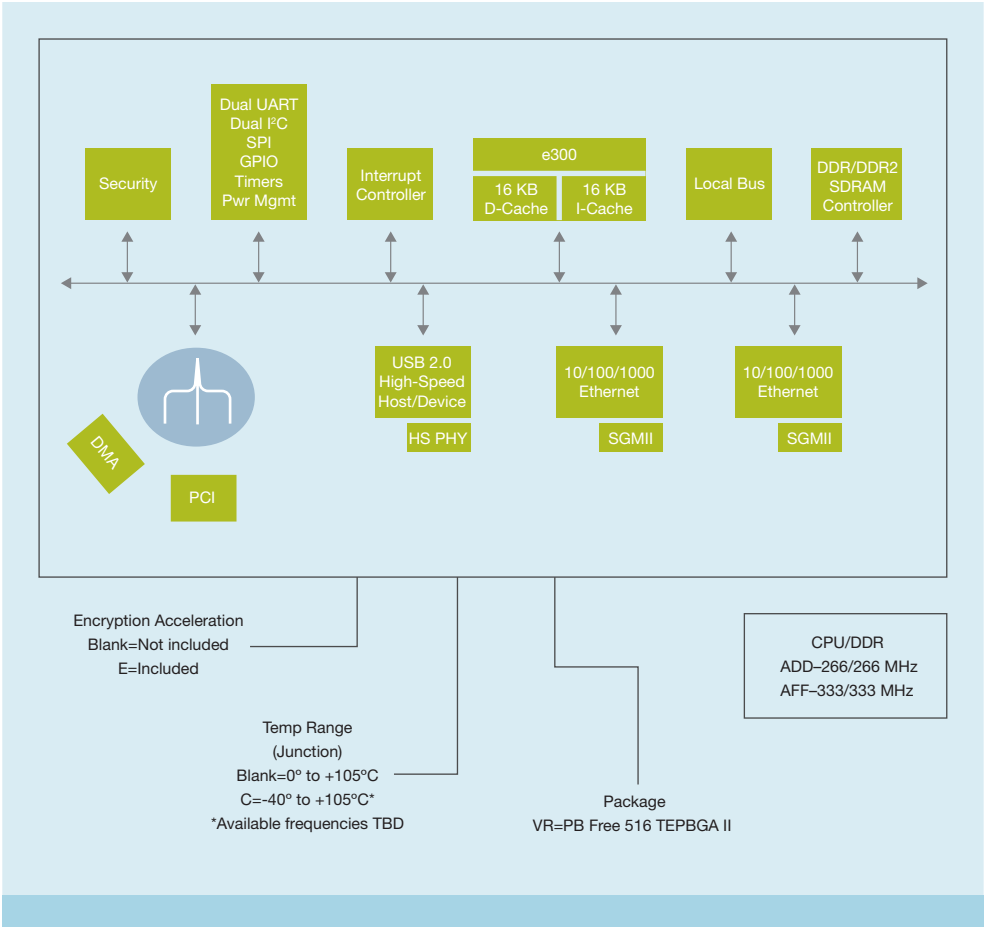
Document Number: MPC8323EPQIIFS
REV 4

# MPC8313E PowerQUICC™ II Pro Processor

## Overview

Rapid growth of personal and premium content has created a need for deploying more interactive multimedia services inside the home. The MPC8313E processor family enables feature rich applications that enhance the digital home experience. The cost-effective MPC8313E communications processor family meets the requirements of several small office/home office (SOHO), printing, IP services and industrial control applications. It provides more CPU performance, additional functionality and faster interfaces while addressing important time to market, price, power consumption and board real estate requirements. The introduction of Gigabit Ethernet (SGMII), High-Speed USB 2.0, and low-power management makes it unique in the marketplace. For extremely precise clock synchronization for applications such as time-sensitive telecommunications services, industrial network switches, powerline networks and test/measurement devices, the MPC8313E features integrated IEEE® 1588 time synchronization, the leading-edge standard.

MPC8313E Block Diagram




## Core Complex

The MPC8313E family incorporates a unique configuration of the e300 (MPC603E based) core. This configuration has been designed to include dual integer units as well as a modified multiply instruction. These architectural enhancements enable more efficient operations to be executed in parallel, resulting in a significant performance improvement. The e300 core complex also includes 16 KB of L1 instruction and data caches and on-chip memory management units (MMUs).

## Peripheral Interfaces

The MPC8313E family also includes a 32-bit double data rate (DDR1/DDR2) memory controller, a 32-bit peripheral component interconnect (PCI) controller, a 16-bit local bus and four direct memory access (DMA) channels.

## Hardware Security Engine

The security engine (SEC 2.2) on the MPC8313E allows CPU-intensive cryptographic operations to be off-loaded from the main CPU core. The security processing accelerator provides hardware acceleration for the DES, 3DES, Advanced Encryption Standard (AES), Secure Hash Algorithm (SHA)-1 and MD-5 algorithms.

freescale semiconductor

| | MPC8313E | MPC8313 |
|---|---|---|
| Core | e300c3, 2-IU, w/FPU, up to 333 MHz | e300c3, 2-IU, w/FPU, up to 333 MHz |
| L1 I/D Cache | 16 KI/16 KD | 16 KI/16 KD |
| Memory Controller | 16/32-bit DDR2-333 | 16/32-bit DDR2-333 |
| Local Bus Controller | 25b/8b dedicated or 25b/16b mux add/data, up to 66 MHz | 25b/8b dedicated or 25b/16b mux add/data, up to 66 MHz |
| PCI | 1 32-bit up to 66 MHz wake-on-PME | 1 32-bit up to 66 MHz wake-on-PME |
| Ethernet | 2 10/100/1000 MACs, SGMII, 98145.452 | 2 10/100/1000 MACs, SGMII, 98145.452 |
| 98145.452 | 1 High-Speed USB 2.0 host/device+HS PHY, wake-on-USB | 1 High-Speed USB 2.0 host/device+HS PHY, wake-on-USB |
| Security | SEC 2.2 | NONE |
| UART | Dual | Dual |
| I²C | Dual | Dual |
| SPI | 1 | 1 |
| Boot options | NOR, NAND, CF, MMC | NOR, NAND, CF, MMC |
| Int. Controller | PIC | PIC |
| Mux/Dedicated GPIO | 10/16 | 10/16 |
| DMA | 4 channels | 4 channels |
| Est. Core Power | ~ 2.4W | ~ 2.4W |
| Power Management | Standby power <300 mW | Standby power <300 mW |

**MPC8313E Family Derivative Optimized for Printing Markets**

Freescale also introduces an MPC8313E derivative optimized for printing and imaging markets. The SC8311 is a cost-effective SoC for printing customers only that helps manufacturers offer highly advanced, full-featured laser printers at low price points. The SC8311 features advanced low-power capabilities that help manufacturers meet emerging power regulations in European and Japanese markets.

**Cost-Effective Evaluation Board**

MPC8313E-RDB (Evaluation Board) is available to customers for US$299*. The kit includes Linux® 2.6 BSP with optimized drivers to support all peripherals, and a six-month CodeWarrior® development tools evaluation license.

*Manufacturer Suggested Resale Price

**Learn More:** For current information about Freescale products and documentation, please visit **www.freescale.com**.



Document Number: MPC8313PRPREFS
REV 1

# MPC8280 PowerQUICC™ II Processor Family

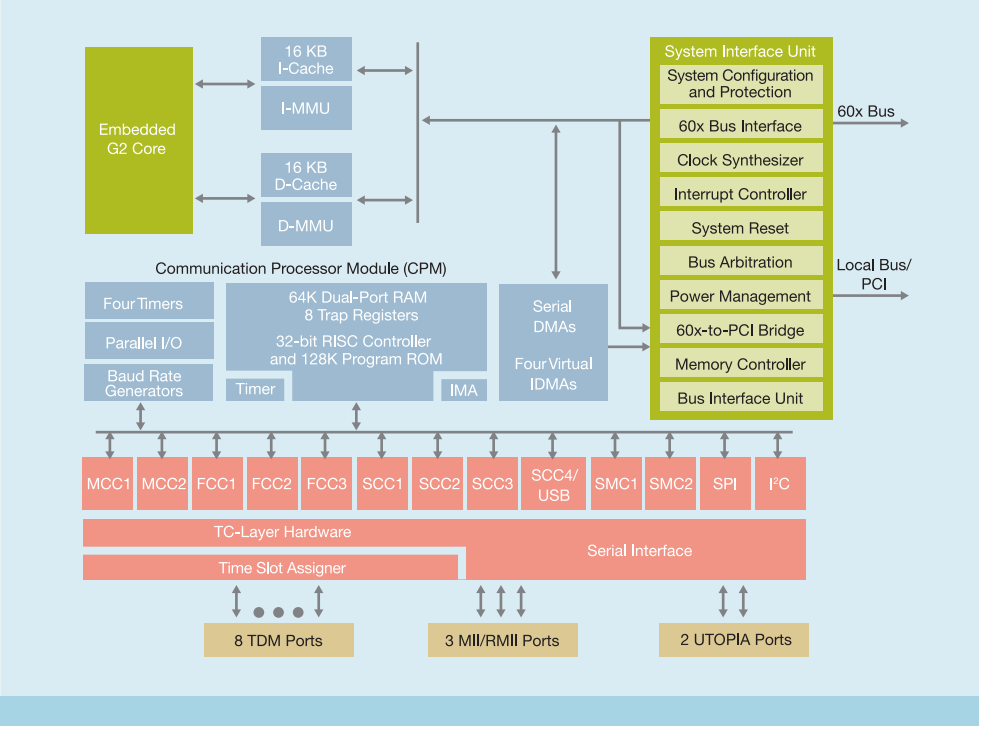
## Join the Revolution

Demand for greater performance and higher integration in telecommunications equipment is driving a revolution in communications processors. In this time to market race, networking equipment makers know to turn to Freescale's family of PowerQUICC™ integrated communications processors which are built on Power Architecture™ technology

Utilizing Freescale's HiPerMOS7 0.13-micron process technology, the MPC8280 PowerQUICC II family offers a range of performance, feature enhancements and package options with lower power consumption. Ideal for wired and wireless infrastructure communications processing tasks, enhancements to the PowerQUICC II family offer system designers a high degree of integrated features and functionality and a compelling, proven architecture. The MPC8280 PowerQUICC II processor family is an optimum solution for integrated control and data path processing in high-end communications and networking equipment—such as routers, DSLAMs, remote access concentrators, telecom switching equipment and cellular base stations.

Combining extensive Layer 2 functionality with control plane processing, Freescale's PowerQUICC II processors combine a high-performance embedded 603e™ core, built on Power Architecture technology, and a powerful RISC-based core to provide support for multiple communications protocols, including 10/100 Mbps Ethernet, 155 Mbps ATM and 256 HDLC channels. The MPC8280 PowerQUICC II devices retain full software compatibility with other members of the PowerQUICC II family.

MPC8280 Block Diagram




## A Range of Performance and Package Options

Taking advantage of the 0.13-micron process, the next-generation of PowerQUICC II devices offers significant performance increases and power efficiencies over previous generation PowerQUICC II devices, with speeds of up to 450 MHz and 300 MHz in the core and CPM respectively operating at less than 2 watts. These processors continue to enhance the PowerQUICC architecture's industry-leading ATM support, offering up to two UTOPIA ports with support for up to 31 PHYs per interface–ideal for high-density DSLAM line cards. The next generation of PowerQUICC II solutions also delivers support for USB (full/low speed), targeting high performance small office/home office (SOHO) and customer premise networking equipment.

Unlike other integrated communications processors in the market, the PowerQUICC architecture integrates two processing cores to handle specific tasks: the Power Architecture core and the RISC-based CPM—enabling a balanced approach for systems by handling both high-level tasks and low-level communications all in one integrated device.

freescale semiconductor

| PowerQUICC™ II Derivative Features—0.13 micron | 8270 | 8270 | 8275 | 8280 |
|---|---|---|---|---|
| **Performance** | | | | |
| CPU | 266 | 333/450 | 266 | 333/450 |
| CPM | 166 | 250/300 | 166 | 250/300 |
| 60x/Memory Bus | 66 | 83/100 | 66 | 83/100 |
| Local Bus | – | 83/100 | – | 83/100 |
| I/D Cache | 16/16 | 16/16 | 16/16 | 16/16 |
| **CPM Interfaces** | | | | |
| PCI | Yes | Yes | Yes | Yes |
| FCCs | 3 | 3 | 3 | 3 |
| • MII/RMII (Fast Ethernet) | 3 | 3 | 3 | 3 |
| • UTOPIA (ATM) | 0 | 0 | 2 | 2 |
| Multi-Channel HDLC | 128 | 128 | 128 | 256 |
| SCCs | 4 | 4 | 4 | 4 |
| USB 1.1 | 1 | 1 | 1 | 1 |
| SMCs | 2 | 2 | 2 | 2 |
| I²C/SPI | 1 | 1 | 1 | 1 |
| IMA/TC Functionality | No | No | No | Yes |
| • Package | 516 PBGA | 480 TBGA | 516 PBGA | 480 TBGA |

Freescale's Design Alliance Program delivers innovative software and hardware solutions that speed time to market and free network equipment providers to focus on value-added functionality.

Freescale works closely with members of the Design Alliance program to ensure that PowerQUICC developers are supported by a wide range of industry-standard operating systems, development tools, instrumentation support and software. These tools enable developers to get the most out of Freescale processors in all phases of the design process.

**PowerQUICC II Processor Family**

With more than 5,000 design wins, Freescale's PowerQUICC family of integrated communications processors is the ideal choice for your embedded networking and communications systems needs.

Explore Freescale's networking and communications embedded solutions on the web at **www.freescale.com/powerquicc**.

**Learn More:** For current information about Freescale products and documentation, please visit **www.freescale.com**.



Document Number: MPC8280FACT
REV 8

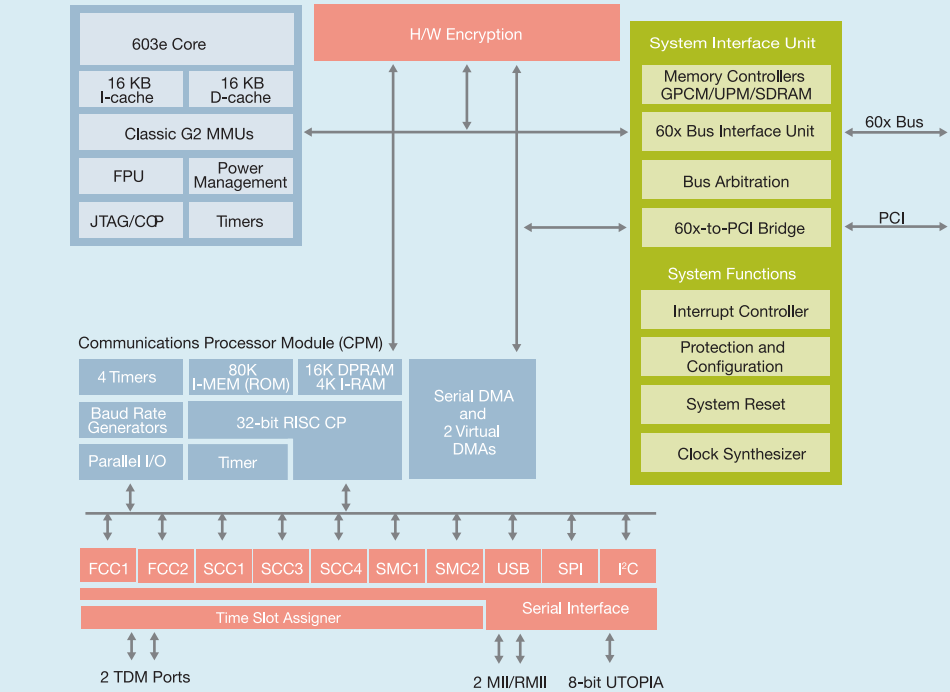
# MPC8272 PowerQUICC™ II Processor Family

The high-performance MPC8272 PowerQUICC™ II processor family, built on Power Architecture™ technology, addresses the cost-sensitive needs of a wide variety of networking and communications applications. By offering integrated hardware security, the MPC8272 family is well suited for networking equipment requiring encryption capabilities, such as small and medium enterprise (SME) routers, virtual private network (VPN) and firewall routers, wireless access points, residential gateways and xDSL equipment, as well as imaging, industrial control and test and measurement equipment.

Delivering an ideal combination of price, performance and low-power operation, the MPC8272 family supports CPU frequencies ranging from 266 MHz to 400 MHz while offering the benefits of low power consumption (0.8 watts at 266 MHz). The family's high level of on-chip integration and small footprint enable developers to reduce board space.

The MPC8272 family includes the MPC8247, MPC8248, MPC8271 and MPC8272 processors. Each device integrates two processing blocks: an embedded 603e™ core, built on Power Architecture technology, and a RISC-based Communications Processor Module (CPM). This dual-core architecture is designed to reduce power consumption and offer a more balanced approach to processing than traditional processor architectures. The CPM offloads low-level peripheral communications tasks, enabling the embedded Power Architecture core to manage high-level processing tasks. The MPC8272 family supports a variety of protocols and interfaces, including dual fast Ethernet MACs, ATM, HDLC, a 32-bit 33/66 MHz PCI interface and a USB host/device interface.

MPC8272 Block Diagram




The MPC8248 and MPC8272 processors feature a security engine that supports DES, 3DES, MD-5, SHA-1, AES and ARC-4 encryption algorithms. The processors also offer a public key accelerator and on-chip random number generator. This embedded security core is derived from Freescale's security coprocessor product line. The core offers the same direct-memory access (DMA) and parallel processing capabilities as Freescale's security coprocessor product line as well as the ability to perform single-pass encryption and authentication as required by widely used security protocols such as IPsec and 802.11i.

On-chip security makes the MPC8272 family an optimal solution for applications that require security features in concert with high performance and low system-level cost.

freescale semiconductor

| MPC8272 Family Features Checklist Chart | MPC8247 | MPC8248 | MPC8271 | MPC8272 |
|---|---|---|---|---|
| Fast Communications Controllers | 2 | 2 | 2 | 2 |
| Serial Communications Controllers | 3 | 3 | 3 | 3 |
| ATM/UTOPIA support | No | No | Yes | Yes |
| Hardware Security | No | Yes | No | Yes |
| 10/100 Base-T MAC | 2 | 2 | 2 | 2 |
| USB (low- and full-speed) | Yes | Yes | Yes | Yes |
| 32-bit 33/66 MHz PCI | Yes | Yes | Yes | Yes |

## Product Highlights

- Efficient, dual-core architecture that combines the 603e core with a separate RISC-based Communications Processor Module
- High-performance operation with CPU frequencies scaling to 400 MHz, CPM frequencies at up to 200 MHz and bus speeds up to 133 MHz
- Superior integration with features optimized for cost-sensitive designs and security-oriented networking applications
- Economical, powerful integrated security engine that supports industry-standard encryption algorithms
- Smooth migration path for PowerQUICC and PowerQUICC II processor-based designs
- Strong third-party tools support through Freescale's Design Alliance Program members

## Typical Applications

- Residential gateways
- SOHO/ROBO and enterprise routers
- Security applications, including VPN routers
- Integrated access devices (IADs)
- Voice-over-Internet Protocol (VoIP) systems
- xDSL equipment
- Wireless access points
- Industrial control

## Technical Specifications

- Embedded 603e core, based on Power Architecture technology, available in speeds of 266 MHz
  - 760 MIPS at 400 MHz (Dhrystone 2.1)
  - High-performance, superscalar processor architecture
  - 16 KB instruction cache and 16 KB data cache
  - Floating point unit
  - Memory management units with 32 TLBs and fully associative instruction and data TLBs
- Advanced on-chip emulation debug mode
- Data bus dynamic bus sizing for 8-, 16- and 32-bit buses
- Embedded security engine that supports AES, DES/3DES, SHA/MD-5 with HMAC, ARC-4, Public Key and on-chip Random Number Generator (security engine available on the MPC8272 and MPC8248 devices)
- Communications Processor Module (CPM) to handle communications tasks
  - 32-bit scalar RISC controller
  - General-purpose I/O; parallel I/O registers
  - Onboard 16K of dual-port RAM
  - Serial I/F unit supporting up to two TDM streams
  - Two fast communications controllers (FCCs) supporting:
    - Two 10/100 Base-T Ethernet MACs with MII/RMII interfaces
    - One 8-bit UTOPIA interface for ATM (AAL 0, 1, 2, 5)


    - Multi-PHY support for 31 PHYs
    - Transparent; HDLC—up to T3 rates (clear channel)
    - Three serial communications controllers (SCCs)
    - 10-Base-T, HDLC/SDLC, UART, BiSync, Transparent, Multi-channel HDLC supporting up to 64 channels
    - Two serial management controllers (SMCs)
    - One I²C port; one serial peripheral interface (SPI)
    - USB host/device interface (USB 2.0 full/low-speed compatible)
- System interface unit
  - 32-bit 3/66 MHz PCI interface
  - Memory controller built from SDRAM, UPM and GPCM machines
  - System functions
- Available in a 516-pin PBGA package (27 mm x 27 mm)
- 0.13µ process technology
- 1.5V core, 3.3V I/O, 1.2 watts of power dissipation at 400 MHz

## PowerQUICC™ II Processor Family

With more than 5,700 design wins, Freescale's PowerQUICC processors are the ideal choice for your embedded networking and communications system needs.

Explore Freescale's embedded solutions, on the web: **www.freescale.com/powerquicc**.

**Learn More:** For current information about Freescale products and documentation, please visit **www.freescale.com**.



Document Number: MPC8272FAMFS
REV 5

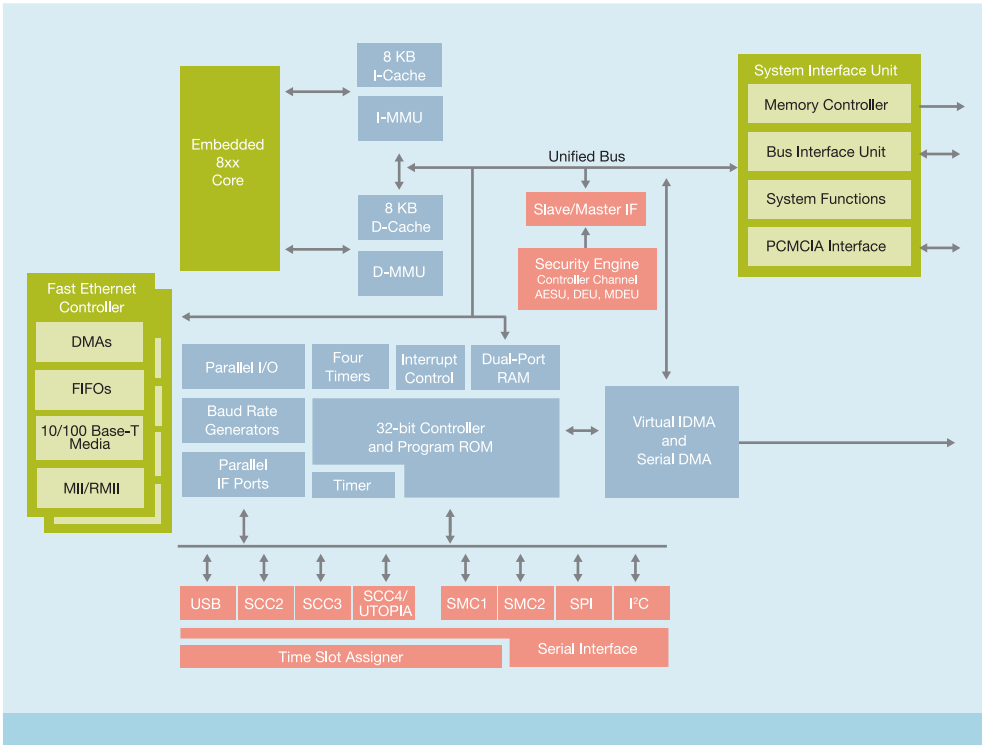
# MPC885 PowerQUICC™ Processor Family

## Overview

Freescale's PowerQUICC™ processor family, built on Power Architecture™ technology, provides an exceptional combination of price, performance and functionality for networking and communications applications. The Freescale MPC885 family takes the price/performance benefits, features and functionality of PowerQUICC communications processors to the next level. The most advanced and feature-rich PowerQUICC devices available, the MPC885 family of processors are engineered to deliver on-chip security, dual Fast Ethernet (MII and RMII) ports, USB and bus speeds scaling to 80 MHz for higher system throughput.

The MPC885 family includes the MPC885, MPC880, MPC875 and MPC870 processors. These highly integrated PowerQUICC devices are designed to deliver a versatile, single-chip communications processor and peripheral solution that can be used in a variety of controller applications, excelling particularly in communications and networking products. Ideal applications include low-end routers, VPN routers with integrated security features, home networking equipment, cost-effective WLAN access points and xDSL gateway boxes.

MPC885 Communications Processor




## Product Highlights

- Dual processor architecture that integrates an embedded 8xx core and RISC-based Communications Processor Module (CPM)
- Available in CPU frequencies of 66 MHz, 80 MHz and 133 MHz
- 8 KB instruction cache and 8 KB data cache
- Powerful memory controller and system functions
- On-chip security engine to help support AES, DES/3DES, SHA/MD5/HMAC (available on the MPC875 and MPC885 devices)
- Support for PCMCIA (for connecting to wireless modules, e.g 802.11 a/b/g)
- Support for dual Fast Ethernet (10/100 Mbps), UART, HDLC, ATM and more, depending on MPC885 family device
- USB host/device (USB 2.0 full/low-speed compatible)
- Up to three SCCs and up to two SMCs available, depending on MPC885 family device
- Many other features: timers, baud rate generators, etc.
- MPC885/880 available in a 357-pin RoHS-compliant PBGA package; MPC870/875 available in a 256-pin RoHS-compliant PBGA package
- Strong third-party tools support through Freescale's Design Alliance Program
- 0.18µ process technology
- 1.8V core, 3.3V I/O, with power consumption below 1W

freescale semiconductor

| | MPC870 | MPC875 | MPC880 | MPC885 |
|---|---|---|---|---|
| I-Cache/D-Cache (KB) | 8/8 | 8/8 | 8/8 | 8/8 |
| Fast Ethernet (10/100) Ports | 2 | 2 | 2 | 2 |
| USB 2.0 Full/Low-speed | Yes | Yes | Yes | Yes |
| Serial Communications Controllers (SCCs) | - | 1 | Up to 2 | Up to 3 |
| Serial Management Controllers (SMCs) | 1 | 1 | 2 | 2 |
| I²C/SPI | Yes | Yes | Yes | Yes |
| ATM Support | - | - | Yes | Yes |
| Multi-Channel HDLC Support | - | 32-ch. | 64-ch. | 64-ch. |
| On-Chip Security | - | Yes | - | Yes |


### Typical Applications

- Low-end routers, including VPN routers
- SOHO and enterprise routers
- Home networking equipment
- Wireless LAN, including cost-effective WLAN access points
- ADSL gateway boxes
- xDSL equipment
- Telecom switching and transmission devices
- Integrated access devices (IADs)
- T1/E1 termination equipment
- General-purpose controller
- Factory automation
- Industrial control
- Embedded control

### MPC885 Full Feature List

- Power Architecture technology
  - Embedded 8xx core designed to provide 158 MIPS (using Dhrystone 2.1) at 120 MHz
  - Single-issue, 32-bit version of the embedded 8xx core with 32-bit x 32-bit fixed point registers
  - Memory management units with 32 TLBs and fully associative instruction and data TLBs
- Advanced on-chip emulation debug mode
- Data bus dynamic bus sizing for 8-, 16- and 32-bit buses
- On-chip security engine
- Communications Processor Module
  - 8 KB dual-port RAM
  - 32-bit scalar RISC controller
  - 16 serial DMA (SDMA) channels
  - One I²C port
  - One serial peripheral interface (SPI)
  - Four general-purpose timers
  - Time slot assigner
  - Interrupts
  - Four baud rate generators
  - Enhanced ATM functionality
    - Simultaneous Fast Ethernet and UTOPIA operation
    - UTOPIA II Multi-PHY
    - AAL2 and VBR microcode in ROM
    - ATM port-to-port switching
  - Protocols supported
    - Ethernet (802.3)
    - Asynchronous Transfer Mode (ATM)
    - HDLC
    - Asynchronous HDLC
    - Channelized HDLC
    - Multi-channel HDLC (T1/E1)
    - AppleTalk® network system
    - UART
    - IrDA
    - Basic Rate ISDN (BRI) and Primary Rate ISDN (PRI)
  - Totally transparent mode with/without CRC
- System interface unit (SIU)
  - Memory controller
  - PCMCIA interface
  - System functions

### PowerQUICC II Processor Family

PowerQUICC, Freescale's PowerQUICC family of integrated communications processors is the ideal choice for your embedded networking and communication system needs.

**Learn More:** For current information about Freescale products and documentation, please visit **www.freescale.com**.



Document Number: MPC885FAMFS
REV 7

# MPC8641D Host Processor

## Built on Power Architecture™ Technology

Freescale's MPC8641D dual-core processor is engineered to deliver breakthrough performance, connectivity and integration for embedded networking, telecom, military, storage and pervasive computing applications.

The MPC8641D's strength is its integration—the high-performance e600 core, built on Power Architecture™ technology, combined with the PowerQUICC™ system-on-chip (SoC) platform. With dual-core performance and integrated northbridge and southbridge functionality, this single chip can replace what could take up to four chips using other solutions. This translates into smaller boards or higher processing density. Additionally, all core-to-peripheral connections are internal in an integrated device, so the board designer is not exposed to the difficulties of laying out high-speed parallel busses.

The MPC8641D features two e600 cores operating at up to 1.5 GHz. Each has its own ECC-protected 1 MB backside L2 caches for avoidance of "cache thrashing." The per-core AltiVec™ 128-bit vector processing engines commonly achieve a 3x to 10x performance increase as shown by EEMBC benchmarks. The peripherals are derived from the field-proven PowerQUICC family, allowing for significant software reuse across Freescale product lines.

One of the significant advantages of the MPC8641D is the fully integrated MPX bus that can run three times faster than an external MPX bus. With MPX bus speed proportional to memory bandwidth and inversely related to memory latency, this integrated bus relieves system bottlenecks for applications limited by either condition. In addition, the MPC8641D features dual integrated memory controllers that provide support for both DDR and DDRII memories, increasing bandwidth and capacity and reducing latency. The memory controllers support error correction codes to ensure data integrity, a basic requirement for any application that needs reliability.

In addition to its performance enhancements, the highly integrated MPC8641D can replace multiple devices, resulting in huge savings in board cost and space. With its on-chip, high-speed interfaces, including the standard RapidIO® fabric interface, PCI Express® interfaces and Gigabit Ethernet interfaces, the MPC8641D does not require system controllers or northbridges and southbridges.

The two cores can run in symmetric multiprocessing mode (SMP) where one operating system assigns tasks to each core, or asymmetric multiprocessing mode, where each core can run an entirely separate OS.

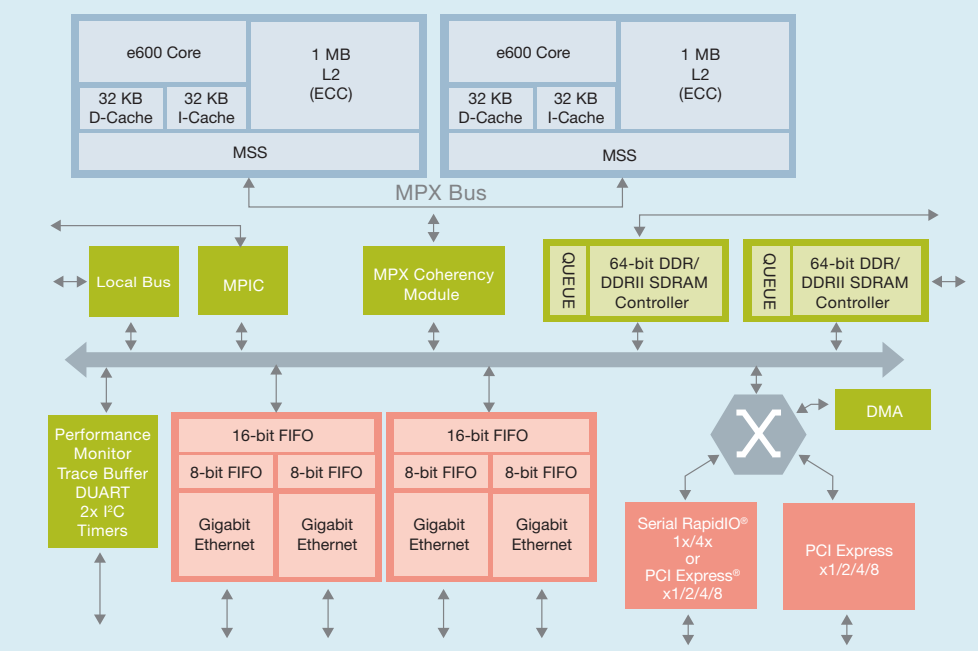
The MPC8641D processor provides extensive application flexibility for developers, offering various options for assigning distinct processing resources to tasks that need guaranteed performance.

**Example 1:** A **high-end line card** uses an ASIC or ASSP for the data path and MPC8641D for the control plane. The two cores can operate in SMP mode for straightforward performance scaling. Two separate operating systems may be used for separate control plane functions, such as off loading security, classification and quality-of-service (QoS) tasks from the core running the main OS.

**Example 2:** A **mid-range line card** uses the MPC8641D to implement both the control and data plane and can be organized in a variety of ways, including splitting functionality directionally (one core per direction) or splitting functionality vertically (one core for handling data plane, one for control plane).

**Example 3:** A **services card**, leveraging the MPC8641D, supports a new feature set in a centralized manner, receiving traffic from all line cards. The RapidIO port connects to the fabric and the Gigabit Ethernet ports implement a management interface.

MPC8641D SoC Diagram



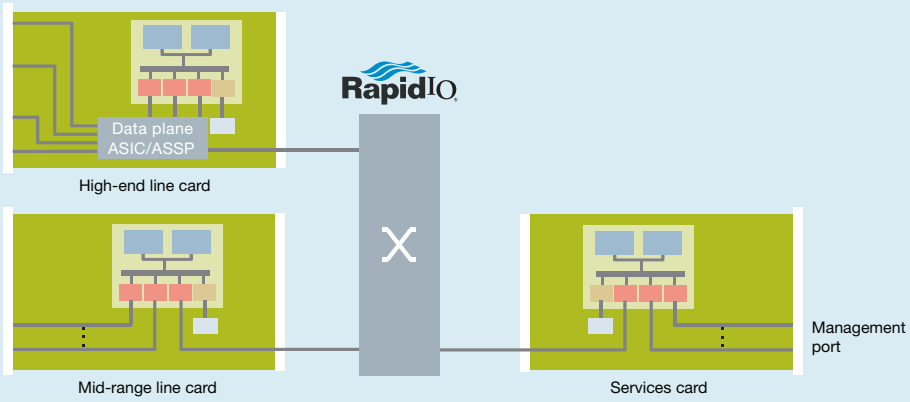

Note: The MPC8641, a pin-for-pin compatible, single-core implementation of the dual-core device is also available. This device offers the same level of bus and interface integration, but it includes only one e600 core built on Power Architecture™ technology.

freescale semiconductor

## MPC8641D Processor Highlights

| | |
|---|---|
| CPU Speeds (internal) | • 1.33 GHz (1.05V), 1.5 GHz (1.1V) |
| Typical Power | • 23.9 watts (1.05V); 32.1 watts (1.1V) |
| MPX Bus (integrated) | • Up to 600 MHz, 64-bit |
| L1 Cache (integrated) | • 32 KB instruction, 32 KB data per core with parity protection |
| L2 Cache (integrated) | • 1 MB per core with optional ECC |
| Package | • 33 x 33 mm, 1023-pin, high-thermal coefficient of expansion (HCTE) ceramic package |
| Process Technology | • 90 nm silicon-on-insulator (SOI) |
| Execution Units | • Integer (4), floating-point, AltiVec™ (4), branch, load/store per core |
| RapidIO® Interface | • 1x/4x serial at Gbaud/lane intervals of 1.25, 2.5 and 3.125<br>• DMA and message-based programming models<br>• Message unit supports SARing up to 4 KB messages into 256-byte packets<br>• Hardware-based error recovery |
| PCI Express® Interface | • One or two 1x/4x/8x serial at 2.5 Gbaud/lane<br>• Configurable as root complex or endpoint<br>• Maximum supported packet payload size is 256 bytes |
| Ethernet Interface | • Four 10/100/1000 Ethernet controllers<br>• Supports MII, RMII, GMII, RGMII, TBI and RTBI<br>• Accelerates TCP and UPD checksum operations<br>• 64 receive queues and eight transmit queues per Ethernet controller with QoS features<br>• Classification and filtering capabilities<br>• High-efficiency FIFO mode for ASIC/FPGA connectivity |
| Memory Controller | • Supports dual 64-bit DDR and DDRII with up to 600 MHz data rate with ECC |
| DMA Controller | • Four independent channels with bandwidth control per channel |
| Multiprocessor Interrupt Controller | • Four inter-core messaging interrupts<br>• Steering of interrupts to either core |
| Local Bus | • 32-bit multiplexed address/data |
| Availability | • Samples: now<br>• Production: mid-2007 |

## System Example Using the MPC8641D Processor




**Learn More:** For current information about Freescale products and documentation, please visit **www.freescale.com**.



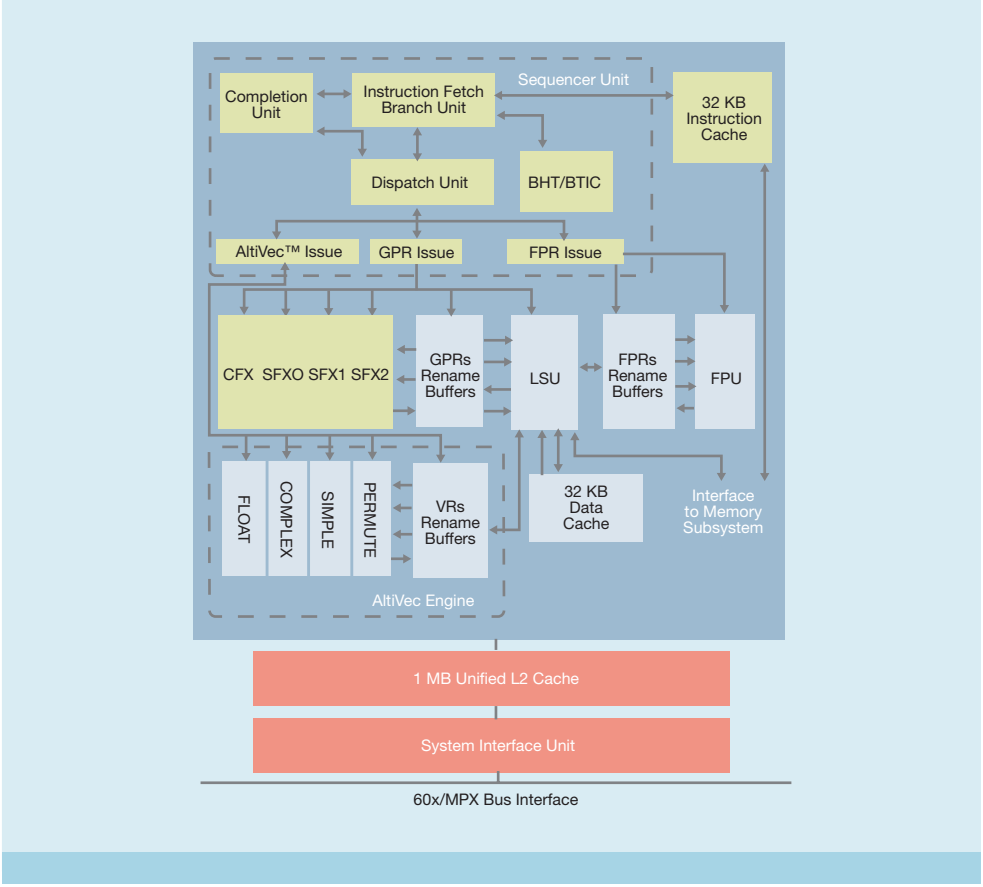
Document Number: MPC8641DDLCRFS
REV 4

# MPC7448 Host Processor Built on Power Architecture™ Technology

The MPC7448 is the first discrete high-performance processor, built on Power Architecture™ technology, manufactured on 90 nanometer silicon-on-insulator (SOI) process technology and continues Freescale Semiconductor's strong legacy of providing products with significant processing performance at very low power. The MPC7448 is designed to exceed 1.7 GHz processing performance and offers enhanced power management capabilities. Running at 1.4 GHz, the MPC7448 uses less then 11 watts of power. MPC7448 processors are ideal for leading-edge computing, embedded network control and signal processing applications.

Key architectural features include a MPX bus that scales to 200 MHz, 1 MB of on-chip L2 cache with support for error correcting codes (ECC), and full 128-bit implementation of Freescale's AltiVec™ technology with the added feature of supporting out-of-order transactions. The MPC7448 is pin-compatible with Freescale's MPC7447 and MPC7447A Power Architecture products, offering an easy upgrade path to better system performance.

MPC7448 Block Diagram




## Caching In

L2 cache helps keep the processor pipeline full, enabling faster and more efficient processing—and the increase in the MPC7448's L2 cache to 1 MB provides an even greater opportunity for performance gains. The L2 cache is fully pipelined for two-cycle throughput in the MPC7448. It responds with an 11-cycle load latency for an L1 miss that hits in L2 with ECC disabled and 12 cycles when ECC is enabled. In the MPC7448, as many as six outstanding cache misses are allowed between the L1 data cache and L2 bus. In addition, the MPC7448 supports a second cacheable store miss. The processors also provide cache locking to the L1 caches so that key performance algorithms and code can be locked in the L1 cache.

freescale semiconductor

| MPC7448 Processor Highlights | |
|---|---|
| CPU Speeds (internal) | Up to 1.7 GHz |
| Instructions per Clock | 4 (3 + Branch) |
| L1 Cache (integrated) | 32 KB instruction, 32 KB data |
| L2 Cache (integrated) | 1 MB with optional ECC |
| Typical Power Consumption | 21 watts @ 1700 MHz, 11 watts @ 1400 MHz, 8.4 watts @ 1267 MHz |
| Execution Units | Integer(4), Floating Point Unit, AltiVec™(4), Branch, Load/Store |
| Performance (est.) | 2.3 MIPS per MHz (using Dhrystone 2.1 method) |
| Bus Protocol | MPX/60x |
| Bus Frequency | 200 MHz |
| Bus Interface | 64-bit |
| Package | 360 HiCTE BGA LGA |
| Process Technology | 90 nm SOI, Multi-Vt, Triple Gate Oxide, Low-K Dielectric, 10 Year Reliability at 105°C |

*Note: The e600 core is identical to the G4 core in previous 7xxx products.

## Power Management

Continuing to pursue lower power consumption is a keen focus with the Freescale family of processors, and the MPC7448 is no exception. Power management features include:

- Expanded Dynamic Frequency Switching (DFS) capability enabling improved power savings (divide-by-two and divide-by-four modes are provided)
- Voltage scales down to 1.0V
- Added benefits of 90 nanometer technology include:
  - Multi-Vt and triple gate oxide integrated transistors for low standby power
  - Low-K dielectric for high performance with reduced power and noise
- Temperature sensing diodes included to monitor die temperature

## Superscalar Core

The MPC7448 processor features a high-frequency superscalar e600 core, built on Power Architecture technology, capable of issuing four instructions per clock cycle (three instructions plus one branch) into 11 independent execution units:

- Four integer units (three simple plus one complex)
- Double-precision floating point unit
- Four AltiVec technology units (simple, complex, floating and permute)
- Load/store unit
- Branch processing unit

## AltiVec Acceleration

The MPC7448 includes the same powerful 128-bit AltiVec vector execution unit as found in previous MPC7xxx devices. AltiVec technology may dramatically enhance the performance of applications such as voice-over-Internet Protocol (VoIP), speech recognition, multi-channel modems, virtual private network servers, high-resolution 3-D graphics, motion video (MPEG-2, MPEG-4) and high fidelity audio (3-D audio, AC-3). AltiVec computational instructions are executed in the four independent, pipelined AltiVec execution units. A maximum of two AltiVec instructions can be issued in order to any combination of AltiVec execution units per clock cycle. In the MPC7448, a maximum of two AltiVec instructions can be issued out-of-order to any combination of AltiVec execution units per clock cycle from the bottom two AltiVec instruction queue entries. For example, an instruction in queue one destined for AltiVec integer unit one does not have to wait for an instruction in queue zero that is stalled behind an instruction waiting for operand availability.

## Compatibility and Support

The MPC7448 can be a drop-in upgrade for MPC7447 and MPC7447A processors because it is pin-for-pin compatible. In addition, as with all processors, the MPC7448 is fully software compatible with the MPC7xxx family of processors. The Freescale family of processors, built on Power Architecture technology, continues to enjoy the support of a broad set of operating systems, compilers and development tools from third-party vendors.

To learn more, please visit **www.freescale.com/powerarchitecture**.

**Learn More:** For current information about Freescale products and documentation, please visit **www.freescale.com**.



Document Number: MPC7448FS
REV 2

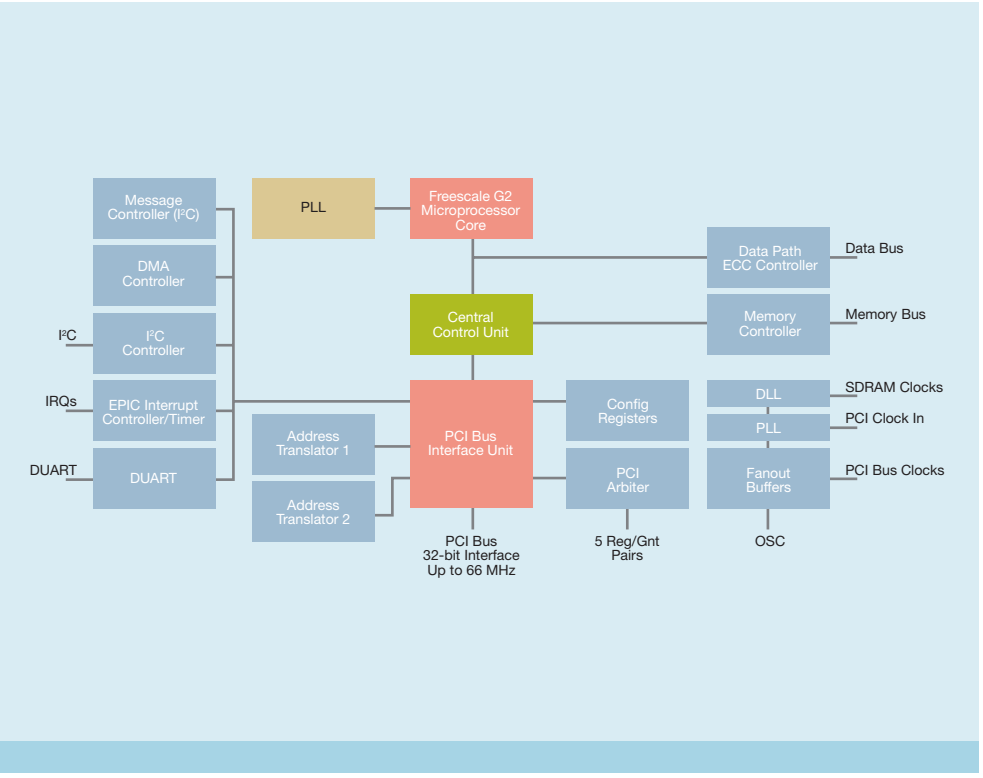
freescale semiconductor

# MPC8245 Host Processor Built on Power Architecture™ Technology

## Overview

The MPC8245 integrated host processor built on Power Architecture™ technology fits applications where cost, space, power consumption and performance are critical requirements. This device is designed to provide a high level of integration, which reduces the chip count from five discrete chips to one and can significantly lower system component costs. High integration results in a simplified board design, low power consumption and a faster time to market solution. This cost-effective, general-purpose integrated processor targets systems using Peripheral Component Interconnect (PCI) interfaces in networking infrastructure, telecommunications and other embedded markets. It can be used for control processing in applications such as routers, switches, network storage applications and image display systems.

## MPC8245 Block Diagram




## Product Highlights

- 266 MHz–400 MHz processor core
- 32-bit PCI interface operating at up to 66 MHz
- Memory controller offering SDRAM support up to 133 MHz operation, support up to 2 GB
- General-purpose I/O and ROM interface support
- Two-channel DMA controller that supports chaining
- Messaging unit with intelligent input/output ($I_2O$) messaging support capability
- Industry-standard inter-integrated circuit ($I^2C$) interface
- Programmable interrupt controller with multiple timers and counters
- 16550 compatible dual universal asynchronous receiver/transmitter (DUART)

## Typical Applications

- Wireless LAN
- Routers/switches
- Embedded computing
- Multi-channel modems
- Network storage
- Image display systems
- Enterprise I/O processor
- Internet access device (IAD)
- Disk controller for RAID systems
- Copier/printer board control

freescale semiconductor

| MPC8245 Integrated Host Processor | |
|---|---|
| CPU Speeds—Internal | 266 MHz–400 MHz |
| CPU Bus Dividers | 2.0, 2.5, 3.0, 3.5, 4.0, 4.5, 5.0, 5.5, 6.0 |
| Memory Bus Dividers | 1.0, 1.5, 2.0, 2.5, 3.0 |
| PCI Interface | 32-bit (up to 66 MHz) |
| Memory Interface | 64-bit (up to 133 MHz) + 8-bit parity |
| Instructions Per Clock | 3 (2 + branch) |
| L1 Cache | 16 KB instruction<br>16 KB data |
| Typical Power Dissipation (est.) | 1.3W @ 266 MHz (with FPU on and @ 1.8V)<br>2.8W @ 400 MHZ (with FPU on and @ 2.0V) |
| Package | 352 TBGA |
| Process | 0.25µ 5LM CMOS |
| Voltage | 3.3V I/O, (1.8V–2.0V internal) |
| Dhrystone (2.1) MIPS | 760 @ 400 MHz |
| 603e Processor Core Functional Units | Integer, floating-point, branch processing, load/store, PCI, DMA, memory control |
| Peripheral Logic Functional Units | $I_2O$, $I^2C$, EPIC, ATU, PCI and memory clocks, ECC controller x2 DUART |

## Technical Specifications

### G2 Processor Core

- High-performance, superscalar processor core
- Floating-point unit, integer, load/store, system register and branch processing unit
- 16 KB instruction cache, 16 KB data cache
- Lockable portion of L1 cache
- Dynamic power management
- Software-compatible with the Freescale processor families built on Power Architecture technology

### On-Chip Peripheral Logic

- Memory interface
- 133 MHz memory bus capability
- Programmable timing supporting SDRAM
- High-bandwidth bus (32-bit/64-bit data bus) to DRAM
- Supports one to eight banks of 16-, 64-, 128-, 256- or 512-bit SDRAM
- Supports 1 MB to 2 GB DRAM memory
- Contiguous memory mapping
- 272 MB of ROM space
- 8-, 16-, 32- or 64-bit ROM
- Supports bus-width writes to flash
- Read-modify-write parity support (selectable)
- ECC support (selectable)
- SDRAM, DRAM buffer data-path
- Error injection/capture on data-path
- Low voltage transistor transistor logic (LVTTL) compatible
- PortX: 8-, 16-, 32- or 64-bit general-purpose I/O port uses ROM controller interface with address strobe

### 32-bit PCI Interface Operating up to 66 MHz

- PCI 2.2V compatible
- PCI 5.0V tolerant
- Support for PCI-locked accesses to memory
- Support for accesses to all PCI address spaces
- Selectable big- or little-endian operation
- Store gathering of processor-to-PCI writes and PCI-to-memory writes
- Memory prefetching of PCI read accesses
- Parity support (selectable)
- Selectable hardware-enforced coherency
- PCI bus arbitration unit (five request/grant pairs)

### PCI Agent Mode Capability

- Dual address translation unit (ATU)
- Run-time register access
- PCI configuration register access

### Two-Channel Integrated DMA Controller

- Supports direct or chaining modes
- Scatter gather
- Interrupt on completed segment, chain and error
- Local to local memory
- PCI to PCI memory
- PCI to local memory
- Local to PCI memory
- Message unit
- $I_2O$ message controller
  - Two door-bell registers
  - Inbound and outbound messaging registers
- $I^2C$ controller
  - Full master/slave support
- Embedded programmable interrupt controller (EPIC)
- Five hardware interrupts (IRQs) or 16 serial interrupts
- Four programmable timers

### Integrated PCI Bus and SDRAM Clock Generation Programmable Memory and PCI Bus Drivers Debug Features

- Watchpoint monitor
- Memory attribute and PCI attribute signals
- JTAG/COP (common on-board processor) for in-circuit hardware debugging

### Dual UART

### Contact Information

Freescale offers user's manuals, application notes and sample code for all of its communications processors. Local support for these products is also provided. Information can be found at **www.freescale.com/powerarchitecture**.

**Learn More:** For current information about Freescale products and documentation, please visit **www.freescale.com**.



Document Number: MPC8245FACT
REV 5

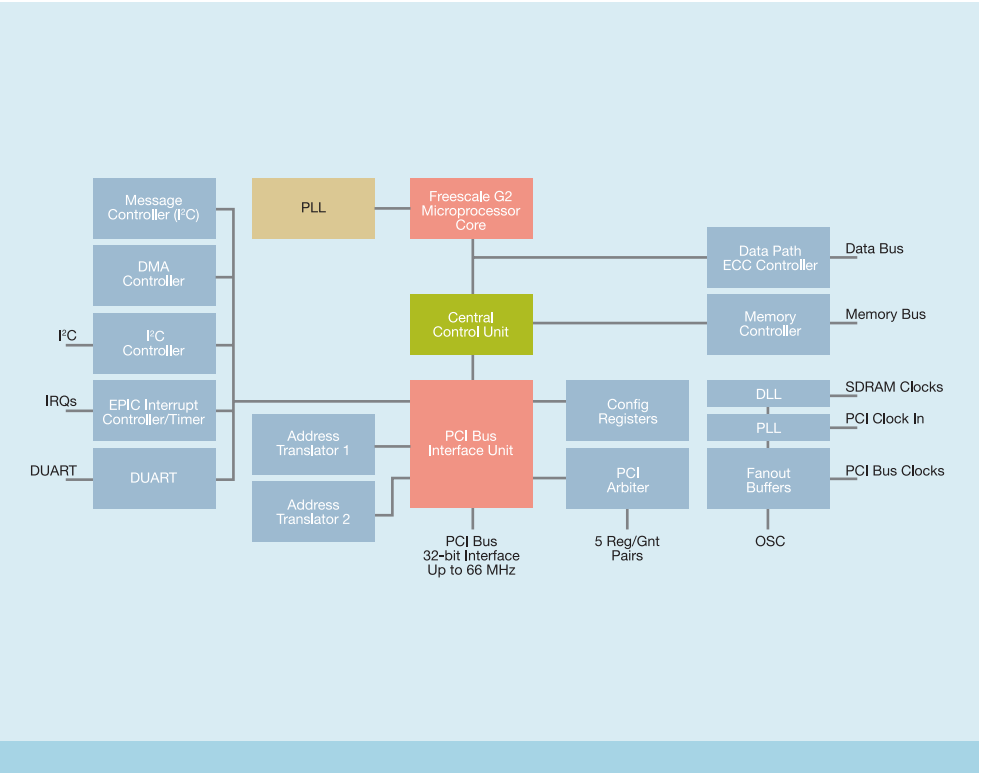
Integrated Host Processors

# MPC8241 Host Processor Built on Power Architecture™ Technology

## Overview

The MPC8241 integrated host processor implementing a core based on Power Architecture™ technology fits applications where cost, space, power consumption and performance are critical requirements. This device is designed to provide a high level of integration, reducing chip count from five discrete chips to one, thereby significantly reducing system component cost. High integration results in a simplified board design, low power consumption and a faster time to market solution. This cost-effective, general-purpose integrated processor targets systems using Peripheral Component Interconnect (PCI) interfaces in networking infrastructure, telecommunications and other embedded markets. It can be used for control processing in applications such as routers, switches, network storage applications and image display systems.

## MPC8241 Block Diagram




## Product Highlights

- 166 MHz–266 MHz processor core
- 32-bit PCI interface operating at up to 66 MHz
- Memory controller offering SDRAM support up to 133 MHz operation, support up to 2 GB
- General-purpose I/O and ROM interface support
- Two-channel DMA controller that supports chaining
- Messaging unit with $I_2O$ messaging support capability
- Industry-standard $I^2C$ interface
- Programmable interrupt controller with multiple timers and counters
- 16550 compatible dual universal asynchronous receiver/transmitter (DUART)

## Typical Applications

- Wireless LAN
- Routers/switches
- Embedded computing
- Multi-channel modems
- Network storage
- Image display systems
- Enterprise I/O processor
- Internet access device (IAD)
- Disk controller for RAID systems
- Copier/printer board control

freescale semiconductor

| MPC8241 Integrated Host Processor | |
|---|---|
| CPU Speeds—Internal | 166 MHz–266 MHz |
| CPU Bus Dividers | 2.0, 2.5, 3.0, 4.0, 4.5 |
| Memory Bus Dividers | 1.0, 1.5, 2.0, 3.0 |
| PCI Interface | 32-bit (up to 66 MHz) |
| Memory Interface | 64-bit (up to 100 MHz) + 8-bit parity |
| Instructions Per Clock | 3 (2 + branch) |
| L1 Cache | 16 KB instruction<br>16 KB data |
| Typical Power Dissipation (est.) | 1.8 watts @ 266 MHz (with FPU on and @ 1.8V) |
| Package | 357 PBGA |
| Process | 0.25µ 5LM CMOS |
| Voltage | 3.3V I/O, 1.8V internal |
| Dhrystone (2.1) MIPS | 488 @ 266 MHz |
| 603e Processor Core Functional Units | Integer, floating point unit, branch processing, load/store, PCI, DMA, memory control |
| Peripheral Logic Functional Units | $I_2O$, $I^2C$, EPIC, ATU, PCI and memory clocks, ECC controller x2 DUART |

## Technical Specifications

### G2 Processor Core

- High-performance, superscalar processor core
- Floating point unit, integer, load/store, system register and branch processing unit
- 16 KB instruction cache, 16 KB data cache
- Lockable portion of L1 cache
- Dynamic power management
- Software-compatible with the Freescale processor families implementing Power Architecture technology

### Power Architecture On-Chip Peripheral Logic/Memory Interface

- 133 MHz memory bus capability
- Programmable timing supporting SDRAM
- High-bandwidth bus (32-bit/64-bit data bus) to DRAM
- Supports one to eight banks of 16-, 64-, 128-, 256- or 512-bit SDRAM
- Supports 1 MB to 2 GB DRAM memory
- Contiguous memory mapping
- 272 MB of ROM space
- 8-, 16-, 32- or 64-bit ROM
- Supports bus-width writes to flash
- Read-modify-write parity support (selectable)
- ECC support (selectable)
- SDRAM, DRAM buffer data path
- Error injection/capture on data path
- Low voltage transistor transistor logic (LVTTL) compatible
- PortX: 8-, 16-, 32- or 64-bit general-purpose I/O port uses ROM controller interface with address strobe

### 32-bit PCI Interface Operating Up to 66 MHz

- PCI 2.2V compatible
- PCI 5.0V tolerant
- Support for PCI-locked accesses to memory
- Support for accesses to all PCI address spaces
- Selectable big- or little-endian operation
- Store gathering of processor-to-PCI writes and PCI-to-memory writes
- Memory prefetching of PCI read accesses
- Parity support (selectable)
- Selectable hardware-enforced coherency
- PCI bus arbitration unit (five request/grant pairs)

### PCI Agent Mode Capability

- Dual address translation unit (ATU)
- Run time register access
- PCI configuration register access

### Two-Channel Integrated DMA Controller

- Supports direct or chaining modes
- Scatter gather
- Interrupt on completed segment, chain and error
- Local to local memory
- PCI to PCI memory
- PCI to local memory
- Local to PCI memory
- Message unit
- Intelligent input/output message controller ($I_2O$)
  - Two door-bell registers
  - Inbound and outbound messaging registers
- Inter-integrated circuit controller ($I^2C$)
  - Full master/slave support
- Embedded programmable interrupt controller (EPIC)
- Five hardware interrupts (IRQs) or 16 serial interupts
- Four programmable timers

### Integrated PCI Bus and SDRAM Clock Generation Programmable Memory and PCI Bus Drivers Debug Features

- Watchpoint monitor
- Memory attribute and PCI attribute signals
- JTAG/COP (common on-board processor) for in-circuit hardware debugging

### Dual UART

### Contact Information

Freescale offers user's manuals, application notes and sample code for all of its communications processors. Local support for these products is also provided. Information can be found at **www.freescale.com**.

**Learn More:** For current information about Freescale products and documentation, please visit **www.freescale.com**.



Document Number: MPC8241FACT
REV 5

# Power Supply Solutions for the PowerQUICC™ Family

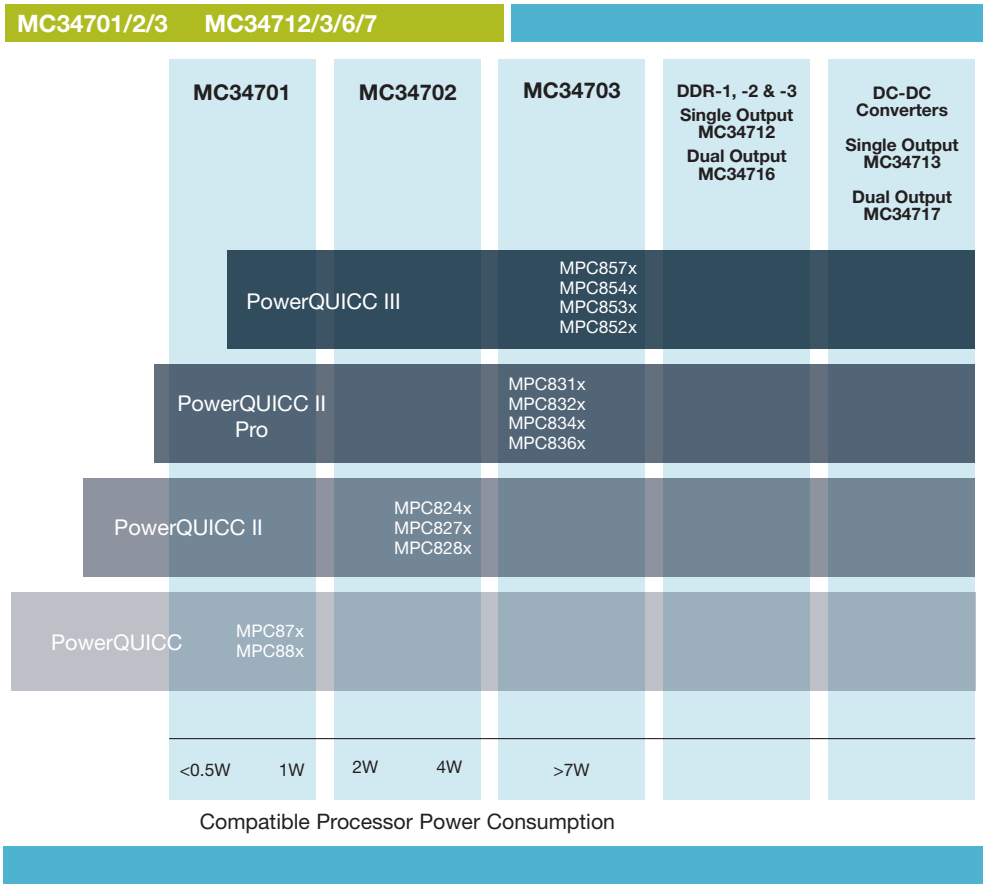
## Part Numbers: MC34701/2/3 MC34712/3/6/7

### Overview

Freescale's QUICCsupply power ICs and single and dual regulator power management ICs support the industry leading PowerQUICC™ communications processors. These versatile integrated power ICs and communications processors are designed for a variety of compute-intensive applications, excelling particularly in communications and networking products. The MC34701/2/3 and MC34712/3/6/7 products integrate system power functions into single small packages, making them an all-in-one plug-and-play product for PowerQUICC III communications processors. These combined solutions provide compact, flexible, integrated and efficient extended capabilities that computing platform manufacturers demand.

### Compatibility Benefits

- Plug 'n play attach to PowerQUICC™ MCU
  - Voltages and sequencing adapted to processor needs
- Versatile solution for general purpose applications
  - Adjustable voltages, switching frequency, dynamic voltage scaling thru I²C
- Simple implementation
  - Small BOM through integrated FETs
  - Family approach for different current capabilities
- Robust solution
  - POR, UVLO, watchdog and integrated thermal protection features




Compatible Processor Power Consumption

| QUICCsupply Power IC Family | MC34703 | MC34702 | MC34701 |
|---|---|---|---|
| **Operating Voltage** | 2.8V–13.5V | 2.8V–6V | 2.8V–6V |
| **Output Voltage** | 0.8V–5V | 0.8V–5V | 0.8V–5V |
| **Output Current** | 10A | 3A | 1.5A |
| **Operating Temperature** | -40°C to +105°C | -40°C to +85°C | -40°C to +85°C |

| Single and dual regulator ICs Family | MC34712 | MC34713 | MC34716 | MC34717 |
|---|---|---|---|---|
| **Operating Voltage** | 3.0V–6.0V | 3.0V–6.0V | 3.0V–6.0V | 3.0V–6.0V |
| **Output Voltage** | 0.7V–1.35V | 0.7V–3.6V | 0.7V–1.35V | 0.7V–3.6V |
| **Output Current** | 3A | 5A | 5A/3A | 5A/5A |
| **Operating Temperature** | -40°C to +85°C | -40°C to +85°C | -40°C to +85°C | -40°C to +85°C |

**Learn More:** For current information about Freescale products and documentation, please visit **www.freescale.com**.



Document Number: QUICCVALUPROPFS
REV 0

# PowerQUICC™ Development Tools

| QUICCstart Boards | | | | |
|---|---|---|---|---|
| **Product Family** | **Device Supported** | **Part Number** | **Price** | **Description** |
| **Various** | MPC8248 | CWH-PPC-8248N-VE | $895 | MPC8248 QUICCstart Board |
| | MPC8540 | CWH-PPC-8540N-VX*, -VE | $1,095 | MPC8540 QUICCstart Board |
| | MPC8343 | CWH-PPC-8343N-VE | $976 | MPC8343 QUICCstart Board |
| | MPC8555 | CWH-PPC-8555N-VE | $1,595 | MPC8555 QUICCstart Board |
| | MPC8548 | CWH-PPC-8548N-VE | $2,294 | MPC8548 QUICCstart Board |
| | MPC885 | CWH-PPC-885XN-VE | $799 | MPC885 QUICCstart Board |

| Development Systems | | | | |
|---|---|---|---|---|
| **Product Family** | **Device Supported** | **Part Number** | **Price** | **Description** |
| **MPC8XX** | MPC850 | MPC850SRFADS* | $2,645 | MPC850 Family Development System |
| | MPC860, MPC862, MPC866 | MPC866ADS* | $2,995 | MPC860/62/66 Development System with USB |
| | MPC852T | MPC852TADS* | $2,995 | MPC852T Development System with USB |
| | MPC852T | MPC852TADS-KIT* | $3,695 | MPC852T Development System |
| | MPC885 Family | MPC885ADSE | $2,995 | MPC885 Family Development System |
| | MPC8xx Family | MPC860SR-PHY* | $1,195 | ATM PHY Board for the MPC8xx Dev Systems |
| **MPC82XX** | MPC8260/70/80–516 PBGA | PQ2FADS-VR* | $2,995 | PowerQUICC II Family Application Development System |
| | MPC8272 Family | MPC8272ADS* | $2,995 | MPC8272 Family Application Development System |
| | All PowerQUICC II | MPC8260ADS-TCOM* | $2,995 | MPC8260 T1/T3 Communication Companion Board for ADS |
| **MPC83XX** | MPC8349 Family | MPC8349EA-MDS-PBE | $1,845 | MPC8349E Processor Board (can be stand alone) |
| | MPC8349 Family | MPC8349EA-MDSE | $4,199 | MPC8349E Dev System (proc board, I/O board, PCI card) |
| | MPC8349 Family | MPC8349E-mITXE | $699 | MPC8349E Reference Design Board miTX Form Factor |
| | MPC8349 Family | MPC8349E-mITX-GP | $299 | MPC8349E General Purpose Industrial Reference Design Board |
| | MPC8323 Family | MPC832xE-MDS-PB | $1,800 | MPC832x Processor Board (can be stand alone) |
| | MPC8323 Family | MPC8323E-RDB | $499 | MPC8323E Multi-Service Gateway Reference Design Board |
| | MPC8360 Family | MPC8360EA-MDS-PB | $1,999 | MPC8360 Processor Board (can be stand alone) |
| | MPC8313 | MPC8313E-RDB | $299 | MPC8313E Reference Design Board miTX Form Factor |
| | MPC83xx | PQ-MDS-PIBE | $2,499 | MPC83xx Platform I/O Board |
| | MPC83xx | PQ-MDS-PMCPCIE | $349 | MPC83xx PCI PMC Card |
| | MPC83xx | PQ-MDS-USB* | $349 | MPC83xx USB PMC Card |
| | MPC83xx | PQ-MDS-PCIEXP* | $995 | Multi PCI Agent PMC |
| | MPC83xx | PQ-MDS-QOC3* | $1,495 | QUAD OC-3 ATM PLUG IN CARD |
| | MPC83xx | PQ-MDS-T1*, -T1E | $1,395 | MPC83xx Slic Slac, T1/E1, TDM Card |
| **MPC85XX** | MPC8540 | MPC8540ADS-BGA* | $4,996 | PowerQUICC III MPC8540 Application Development System |
| | MPC8560 | MPC8560ADS-BGA* | $4,996 | PowerQUICC III MPC8560 Application Development System |
| | MPC8555/8541 | MPC8555CDS | $4,996 | PowerQUICC III MPC8555/8541 Configurable Development System |
| | MPC8548 | MPC8548CDS | $5,499 | PowerQUICC III MPC8548 Configurable Development System |
| | MPC8568 | MPC8568-MDS-PB | $2,495 | MPC8568 Processor Board |
| | MPC8544 | MPC8544DS | $3,395 | MPC8544 ATX Development System |

*Non-RoHS Compliant

freescale semiconductor

| Development Tools For PowerQUICC | | | | | |
|---|---|---|---|---|---|
| **Evaluation Boards, Development Kits, Board Support Packages** | **MPC8XX PowerQUICC I** | **MPC82XX PowerQUICC II** | **MPC83XX PowerQUICC II Pro** | **MPC85XX PowerQUICC III** | |
| Analogue & Micro Ltd. | x | x | x | x | www.analogue-micro.com |
| ARC International | x | x | x | x | www.arc.com |
| Artis Microsystems | | | | x | www.artismicro.com |
| Embedded Planet | x | x | | | www.embeddedplanet.com |
| Freescale Semiconductor | x | x | x | x | www.codewarrior.com |
| Green Hills Software | x | x | x | x | www.ghs.com |
| MontaVista Software | x | x | x | x | www.mvista.com |
| QNX Software Systems | x | x | x | x | www.qnx.com |
| Silicon Turnkey Express | | | x | x | www.silicontkx.com |
| TQ Components | x | x | | x | www.tq-components.com |
| Wind River Systems | x | x | x | x | www.windriver.com |
| **Real-Time Operating Systems** | | | | | |
| Accelerated Technology | x | x | | | www.acceleratedtechnology.com |
| ARC International | | x | | | www.arc.com |
| Blunk Microsystems | x | | x | x | www.blunkmicro.com |
| CMX Systems, Inc. | | x | | x | www.cmx.com |
| ENEA (OSE) | x | x | x | | www.enea.com |
| Express Logic, Inc. | x | x | x | x | www.rtos.com |
| Freescale Semiconductor | x | x | x | x | www.freescale.com |
| Green Hills Software | x | x | x | x | www.ghs.com |
| VirtualLogix | x | x | | | www.virtuallogix.com |
| Kadak Products, Ltd | | x | | x | www.kadak.com |
| Kenati Technologies | | x | x | | www.kenati.com |
| Micro Digital Inc. | x | | | | www.smx-rtos.com |
| MontaVista Software | x | x | x | x | www.mvista.com |
| QNX Software Systems | x | x | x | x | www.qnx.com |
| Wind River Systems | x | x | x | x | www.windriver.com |
| **Compilers, Simulators, Debuggers** | | | | | |
| Analogue & Micro Ltd. | x | x | | | www.analogue-micro.com |
| ARC International | x | x | | x | www.arc.com |
| Freescale Semiconductor | x | x | x | x | www.codewarrior.com |
| Green Hills Software | x | x | x | x | www.ghs.com |
| Lauterbach | | x | x | x | www.lauterbach.com |
| Wind River Systems | x | x | x | x | www.windriver.com |
| **Stacks, Drivers, Translators** | | | | | |
| Accelerated Technology | x | x | | x | www.acceleratedtechnology.com |
| ARC International | x | x | | x | www.arc.com |
| Blunk Microsystems | | | | x | www.blunkmicro.com |
| Dogav Systems Ltd | x | x | x | x | www.dogav.net |
| Flextronics | x | x | x | x | www.flextronics.com |
| Freescale Semiconductor | x | x | x | x | www.freescale.com |
| Interniche Technologies | x | x | | x | www.iniche.com |
| Kenati Technologies | | x | | x | www.kenati.com |
| Mocana Corporation | x | x | | x | www.mocana.com |
| MontaVista Software | x | x | x | x | www.mvista.com |
| QNX Software Systems | x | x | x | x | www.qnx.com |
| Quadros Systems Inc. | x | x | | x | www.quadros.com |
| Telesoft International | x | x | | | www.telesoft-intl.com |
| Wind River Systems | x | x | x | x | www.windriver.com |
| **Emulators, Probes, Wigglers** | | | | | |
| Abatron | x | x | x | x | www.abatron.com |
| Avocet Systems, Inc. | x | | | | www.avocetsystems.com |
| Corelis, Inc. | x | x | | x | www.corelis.com |
| Freescale Semiconductor | x | x | x | x | www.freescale.com |
| Green Hills Software | x | x | | x | www.ghs.com |
| International Test | x | | x | | www.intertesttech.com |
| iSYSTEM | x | | | | www.isystem.com |
| Macraigor Systems LLC | x | x | x | x | www.macraigor.com |
| Wind River Systems | x | x | x | x | www.windriver.com |
| **Microcode** | | | | | |
| Dogav Systems Ltd | x | x | | x | www.dogav.net |
| IndusRAD | | | x | x | www.indusrad.com |
| Wipro Technologies | | | x | x | www.wipro.com |

**Learn More:** For current information about Freescale products and documentation, please visit **www.freescale.com**.



Document Number: PWRQUCDEVTOLFS
REV 2

# MPC8349E-mITXE Reference Platform

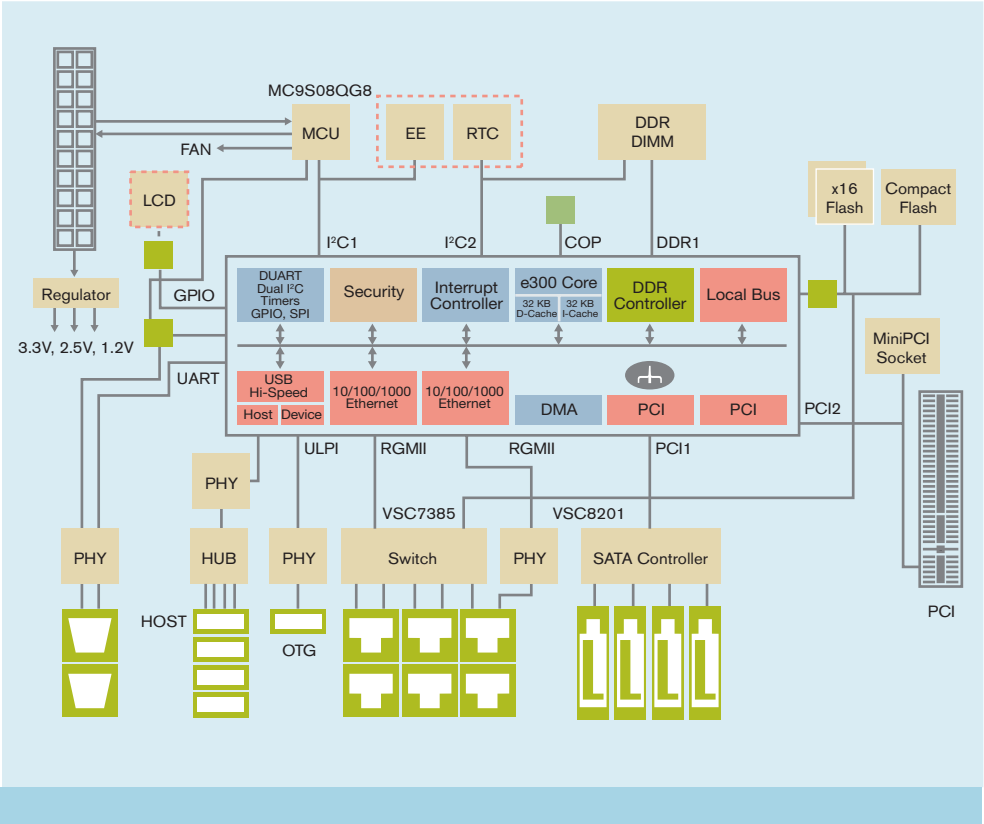
## Overview

The MPC8349E-mITXE reference platform is ideal for hardware and software development for networking applications. It leverages Freescale's highly integrated MPC8349E processor built on Power Architecture™ technology and leading-edge external components—a 5-port Gigabit Ethernet switch, four high-speed USB ports, four serial ATA ports, one Peripheral Component Interconnect (PCI) slot, one MiniPCI slot and one compact flash memory slot.

The high level of integration in the MPC8349E helps to lower system costs, improve performance and simplify board design. The MPC8349E microprocessor supports dual 10/100/1000 Mbps Ethernet controllers, dual 32-bit/single 64-bit PCI controllers, integrated security engines, USB 2.0 host and device controllers, 4-channel direct memory access (DMA), dual universal asynchronous receiver/transmitter (DUART), serial peripherals, general purpose I/O and system timers. The MPC8349E also integrates a hardware encryption block that supports different algorithms for high-performance data that is critical for supporting secure communications in the residential market. It supports DES, 3DES, MD-5, SHA-1, AES, PKEU, RNG and RC-4 encryption algorithms in hardware.

A board support package (BSP) is pre-installed on the MPC8349E-mITXE. This BSP consists of a bootloader (u-boot), a generic Power Architecture technology system based on the Linux® kernel. The u-boot and the Linux kernel reside in the on-board flash memory while the file system is pre-installed on the hard disk shipped with the MPC8349E-mITXE. On powering up, the Linux system runs on the MPC8349E-mITXE.

## MPC8349E-mITXE Block Diagram




The MPC8349E-mITXE BSP generation takes advantage of the Linux Target Image Builder (LTIB), a suite of tools that leverages existing open source configuration scripts and source code packages and bundles them all into a single BSP generation bundle. The source code packages include boot loaders and Linux kernel sources as well as many user-space source code packages to build a complete BSP. The LTIB also provides compiler packages required to build the BSP. Freescale developers use the LTIB to create BSPs for a multitude of Freescale development markets. The LTIB leverages as many BSP elements as possible for all Freescale markets supported, while offering the flexibility necessary to customize components that require platform-specific modifications.

Many third-party applications are available for the MPC8349E-mITXE. They are typically built on top of the BSP delivered by Freescale and are installed on the hard disk. To see demonstrations or to acquire details of Freescale's third-party applications for this platform, please contact your local Freescale sales office.

freescale semiconductor

## Features

- CPU:
  - Freescale MPC8349E running at 533/266 MHz (CPU/Coherent System Bus)
- Memory subsystem:
  - 256 MB unbuffered DIMM SDRAM that is expandable to 1 gigabyte
  - 16 MB flash memory (two Macronix™ MX29LV640M flash memory banks)
  - Type I compact flash connector to interface with the compact flash storage card in true IDE mode (3.3 mm thick)
- Interfaces:
  - 10/100/1000 Base-T Ethernet ports:
    - TSEC1, GMII interface: one 10/100/1000 Base-T RJ-45 with RJ-45 interface using Vitesse™ VSC8201 single-port 10/100/1000 Base-T PHY
    - TSEC 2, GMII interface: five 10/100/1000 Base-T RJ-45 with Vitesse VSC7385 SparX-G5™ 5 + 1-port Gigabit Ethernet integrated PHY switch
  - USB 2.0 OTG and hub:
    - USB1, ULPI interface: four USB 2.0 type A receptacle connectors, with Genesys Logic™ GL850A 4-port USB 2.0 hub controller
    - USB2, ULPI interface: one USB 2.0 type mini-AB receptacle connector with SMSC™
    - USB3300 high-speed USB host/ device/OTG PHY
  - Serial ATA controller:
    - Silicon Image™ SiI3114 PCI to serial ATA controller that connects to a 66 MHz PCI-1
    - Supports four independent serial ATA channel
    - One 32-bit 3.3V MiniPCI/PCI slot connected to PCI-2
  - Atmel™ AT24C08 serial EEPROM
  - Dallas™ DS1339 RTC with battery holder
  - Freescale MC9S08QG8 MCU for fan control and soft start
- Board connectors:
  - LCD interface using GPIO
  - ATX power supply connector
  - RS-232C connectors
    - 9-pin DB9 receptacle
    - 10-pin 2.54 mm connector
  - JTAG/COP for debugging
- 6-layer PCB routing (4-layer signals, 2-layer power and ground) Orderable Part Number MPC8349e-mITXE

**Learn More:** For current information about Freescale products and documentation, please visit **www.freescale.com**.



Document Number: MPC8349EPLATFS
REV 2

Built on Power Architecture™ Technology

# MPC8349E-mITX-GP Evaluation Platform for Industrial Applications

### Power Architecture™ Delivers

- Integrated products with pricing starting at $13 for 300 MHz
- Devices with a max power of less than 2 watts
- Best-in-class system performance
  - Value-added integration
  - Less frequency—allowing greater system options
  - Additional cost and power savings

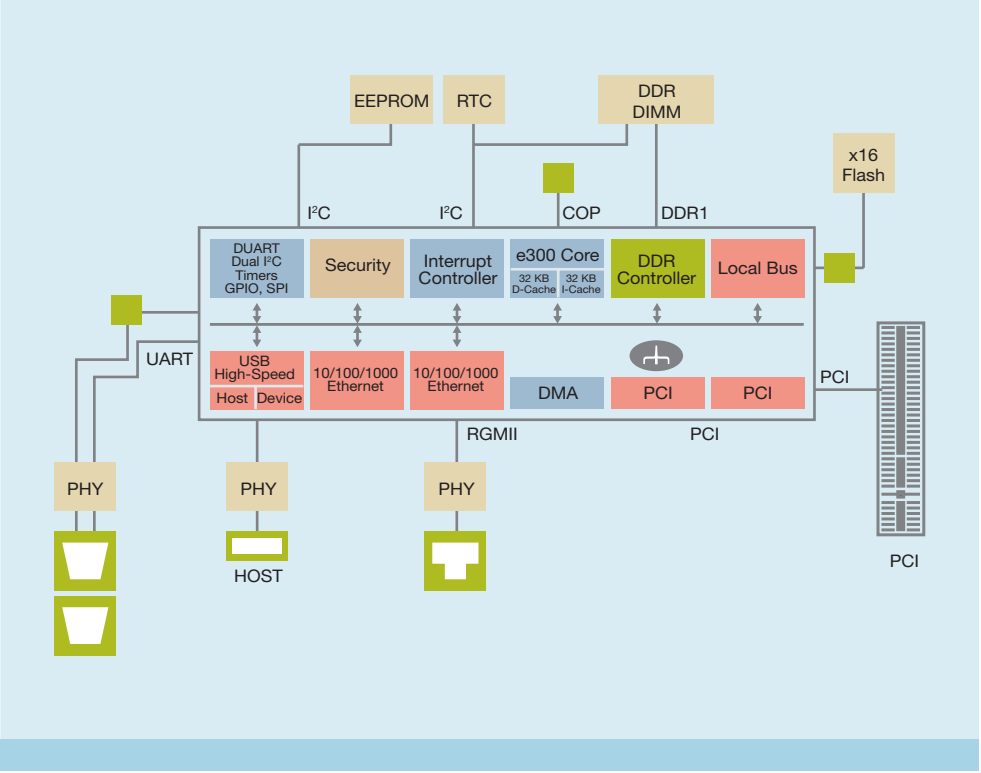
### Power Architecture is Ideally Suited for Industrial Applications

- Multi-protocol support
- Ethernet controllers integrated on many processors
- On-chip interconnect interfaces—no external bridge chips required
- On-chip memory controllers—no chipset required
- Low heat generation and extended temperature ranges for fanless operation
- Long-term product life cycles
- An extensive third-party ecosystem, including Linux® OS support

### Targets Industrial Applications, Including:

- Automation and robotics
- Test and measurement
- Process manufacturing control
- Aerospace
- Building control
- Health care

MPC8349E-mITX-GP Evaluation Platform Block Diagram




### Power Architecture: Consistency, Compatibility and Simplicity

Freescale's Power Architecture product portfolio ranges from very high-performance processor cores found in high-end, general-purpose computing applications, to high-precision microcontrollers for motor control—and everything in between. Even with enormous leaps in technology, performance and capabilities, Power Architecture processors remain consistent, compatible and well-defined from generation to generation. The PowerQUICC™ architecture has been consistent throughout its evolution, from the first PowerQUICC communications processors to the latest PowerQUICC III.

This continuity offers tremendous advantages to PowerQUICC customers, as they can rest assured that their investments in PowerQUICC processor-based products are both backward- and forward-compatible without extensive development investments.

Power Architecture is designed for scalability and software compatibility across generations and subfamilies to help simplify customer migrations and reduce costs. Multi-protocol support and connectivity to a wide variety of interfaces increases versatility, and makes Power Architecture attractive to applications in the industrial arena.

freescale semiconductor

## MPC8349E-MITX-GP Industrial Evaluation Platform

The MPC8349E-MITX-GP industrial platform demonstrates the capabilities of Freescale's MPC8349E processor and is designed for customers unfamiliar with Power Architecture to allow them to evaluate the processor family and the software development around it. The platform leverages external components to support features such as a Gigabit Ethernet port, a high-speed USB port, serial channels and a PCI slot.

## MPC8349E Microprocessor

The MPC8349E microprocessor supports dual 10/100/1000 Mbps Ethernet controllers, dual 32-bit/single 64-bit PCI controllers, integrated security engines, USB 2.0 host and device controllers, 4-channel DMA, DUART, serial peripherals, general-purpose I/O and system timers. The high level of integration in the MPC8349E helps lower system costs, improves performance and simplifies board design.

The MPC8349E also integrates a hardware encryption block that supports different algorithms for high-performance data authentication as required for secure communications in the industrial market. It supports DES, 3DES, MD-5, SHA-1, AES, PKEU, RNG and RC-4 encryption algorithms in hardware.

## MPC8349E-mITX-GP Board Support Package (BSP)

A BSP is pre-installed on the MPC8349E-mITX-GP. This BSP consists of a bootloader (u-boot), a generic PPC Linux-based system and associated file system. The u-boot, Linux® kernel and the file system reside in the onboard flash memory. Upon power-up, the system is running the u-boot bootloader and is ready to boot Linux using u-boot commands.

The MPC8349E-mITX-GP BSP generation takes advantage of a Linux Target Image Builder (LTIB). LTIB is a suite of tools that leverages existing open source configuration scripts and source code packages, and bundles them all into a single BSP. The source code packages include bootloaders and Linux kernel sources as well as many user-space source code packages that can be used to build a complete BSP. LTIB also provides compiler packages required to build the BSP. Freescale developers use LTIB to create BSPs for a multitude of Freescale development targets. LTIB leverages as many BSP elements as possible for all Freescale targets supported, while offering the flexibility required to customize, as necessary, components that require platform-specific modifications.

## Features

- CPU: Freescale MPC8349E running at 533/266 MHz (CPU/CSB (Coherent System Bus))
- Memory subsystem:
  - 128 MB unbuffered DIMM SDRAM expandable to 1 Gbyte
  - 8 MB flash memory
- Interfaces:
  - 10/100/1000 Base-T Ethernet ports:
    - TSEC1, GMII interface: one 10/100/1000 Base-T RJ-45 with RJ-45 interface using Vitesse™ VSC8201 single-port 10/100/1000 Base-T PHY
  - USB 2.0 OTG and hub:
    - USB2, ULPI interface: one USB2.0 type mini-AB receptacle connector, with SMSC™
    - USB3300 high-speed USB host/device/OTG PHY
  - One 32-bit 3.3V PCI slot
  - ST M24256 Serial EEPROM
  - Dallas™ DS1339 RTC with battery holder
  - ATX power supply connector
  - RS-232C connectors
  - 9-pin DB9 receptacle
  - 10-pin 2.54 mm connector
  - JTAG/COP test access port for debugging
  - 6-layer PCB routing (4-layer signals, 2-layer power and ground)

## Orderable Part Number

MPC8349E-MITX-GP

**Learn More:** For current information about Freescale products and documentation, please visit **www.freescale.com**.



Document Number: MPC8349EMITXGPFS
REV 1

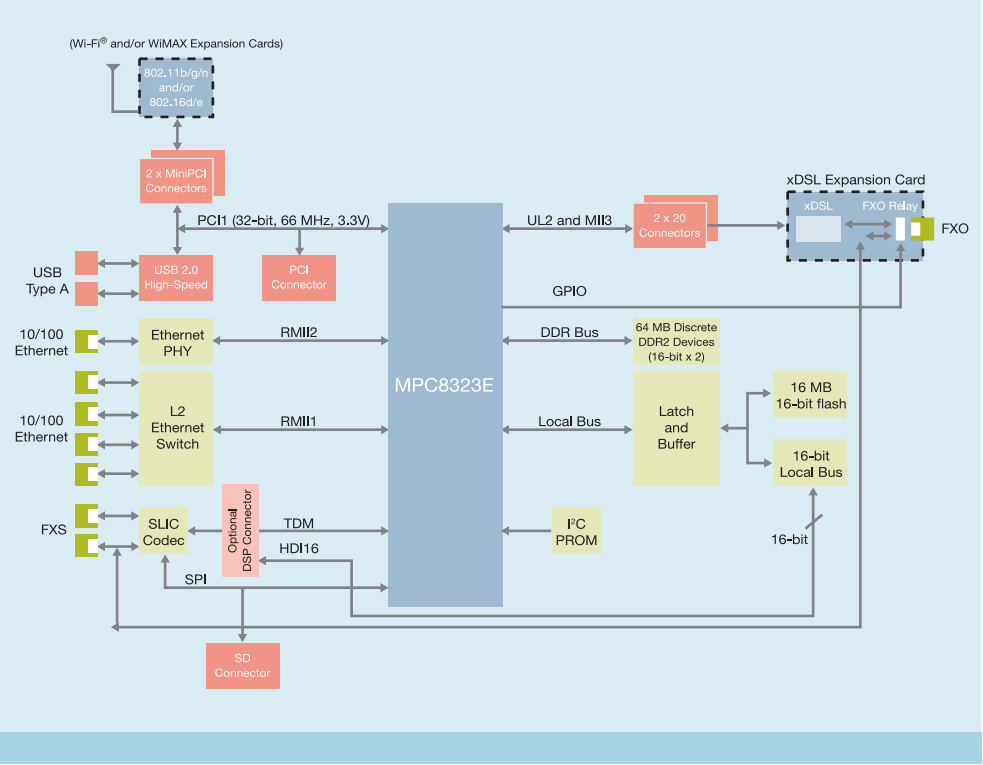
Based on PowerQUICC™ Architecture

# Integrated Multi-Service Gateway Reference Design

Next-generation residential gateway products will be challenged to maintain bridging/routing throughput speeds as WAN interfaces (WiMAX, GPON, VDSL2) stream more packets per second. The products that survive will deliver this level of performance and the flexibility to support multiple LAN interfaces (802.11n, HPNA 3.1, MoCa, HomePlug AV and UPA).

In addition to performance, these products must also bring the right balance of consumer required features and ease of use, while supplying service providers with a cost-effective platform that enables future services via remotely managed upgrades. Triple-play deployment requires better Quality-of-Service (QoS) management and security in the gateway to provide stronger protection (firewall, access, intrusion detection/prevention services, anti-virus/anti-spam). These features give service providers the confidence they need to securely deliver premium audio/video content to their valued customers.

MPC8323E Reference Design Board




## Freescale Value Proposition

Freescale brings a broad portfolio of proven PowerQUICC™ network communications products, firmware and reference designs that support multiple network interfaces. These reference designs have the flexibility to integrate new features and are adaptable across product lines to help protect your investment and maintain a “first to market” edge over the competition.

The MPC8323E-RDB is a turnkey hardware/software reference platform designed to rapidly provide the core elements of tomorrow’s multi-service gateway products.

The MPC8323E-RDB leverages the processing power of the MPC8323E PowerQUICC II Pro integrated communications processor. Built on Power Architecture™ technology, the MPC8323E family of products integrates a proper balance of architectural features (e300 core, dual integer units, 16 KB instruction and 16 KB data caches) along with a DDR 1/2 memory controller, RISC-based communications engine (QUICC Engine™) and an optional hardware security engine.

freescale semiconductor

| Performance Estimates | 64 B Packets | 256 B Packets | 512 B Packets | 1450 B Packets |
|---|---|---|---|---|
| IPv4 Forwarding Throughput (Mbps) | 142 Mbps | 200 Mbps | 200 Mbps | 200 Mbps |
| QUICC Engine™ Utilization (% of total available) | 85% | 44% | 33% | 26% |
| IPv4 Forwarding with NAPT/Firewall (Mbps) | 96 Mbps | 200 Mbps | 200 Mbps | 200 Mbps |
| QUICC Engine Utilization (% of total available) | 86% | 62% | 41% | 27% |
| IPSec ESP (3DES-HMAC-SHA-1) | 10 Mbps | 36 Mbps | 74 Mbps | 181 Mbps |

Note: Estimates based on capability of QUICC Engine running optimized microcode. Throughputs are for aggregated Ethernet to Ethernet traffic using MPC8323E 333 MHz e300 core, 200 MHz QUICC Engine.

Freescale's industry-recognized QUICC Engine technology, derived from its predecessor, the Communications Processor Module (CPM), provides a substantial performance advantage to network communications-intensive applications. Typical data path applications requiring a significant percentage of CPU cycles to process can be offloaded to the QUICC Engine technology, freeing up the CPU to perform other application-critical functions.

Similarly, the optional hardware security engine is designed to offload the CPU from processing computationally intensive encryption and authentication algorithms. This engine provides support for IPSec, SSL/TLS, SRTP and 802.11i protocols.

## System Features

- Flexible WAN interfaces
  - RJ45 100BT Ethernet and connectors for WiMAX, ADSL2+/VDSL2
- IPv4 router with VPN capability
  - Up to 640 DMIPS e300 CPU
  - QUICC Engine technology acceleration, 200 MHz
    - Bridging/routing with NAPT
    - Firewall support (ACL)
    - QoS for IPTV, VoIP and high-speed data
  - VPN termination and pass-through

**Orderable Part Number**
**MPC8323E-RDB**

## Board Interfaces

- Flexible network interfaces
  - 10/100 Ethernet
- 4-port 10/100 Ethernet LAN
- Two FXS ports for analog phones
- Two USB 2.0 host (480 Mbps) type A ports
- Two MiniPCI slots, one PCI slot
- One serial port

## Development Environment

Freescale's well established vertical ecosystem provides customers with the exact development flow they desire.

The MPC8323E-RDB is kitted with:

- Encased CPE form factor board with power supply
- Freescale Linux® 2.6 (LTIB)

## Freescale/Third-Party Software

- Ethernet Switch
- WiMAX
- Wi-Fi®
- SLIC
- VoIP

**Learn More:** For current information about Freescale products and documentation, please visit **www.freescale.com**.



Document Number: REFDESIGNFS
REV 1

# MPC8313E-RDB Reference Platform

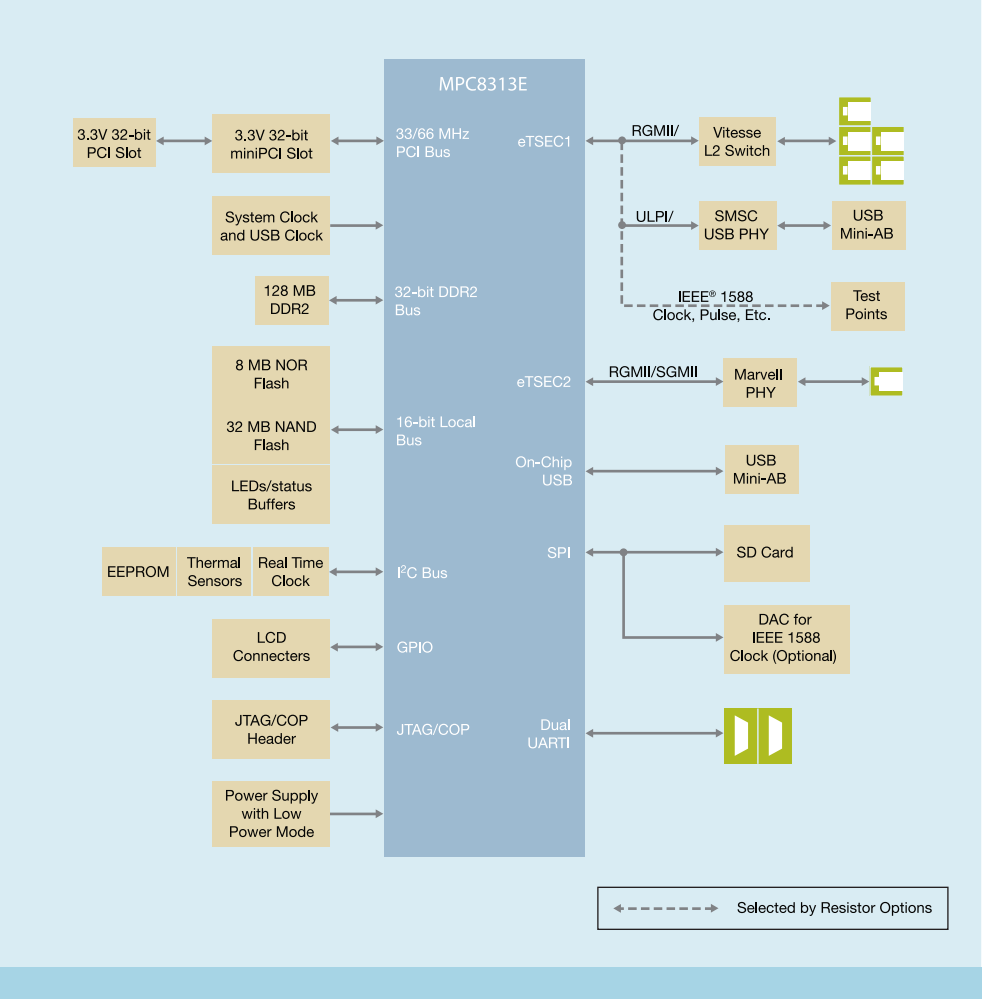
## Overview

The MPC8313E-RDB reference platform is ideal for hardware and software development for cost-optimized networking applications. The cost-effective MPC8313E communications processor family meets the requirements of several small office/home office (SOHO), printing, IP services and industrial control applications. It leverages Freescale's highly integrated MPC8313E processor built on Power Architecture™ technology and leadingedge external components—a 5-port Gigabit Ethernet switch, USB port, one Peripheral Component Interconnect (PCI) slot, one MiniPCI slot and one SD card memory slot. The high level of integration in the MPC8313E helps to lower overall system costs, improve performance and simplify board design.

The MPC8313E microprocessor supports dual 10/100/1000 Mbps Ethernet controllers, single 32-bit PCI controller, integrated security engine, USB 2.0 host, four-channel direct memory access (DMA), dual universal asynchronous receiver/transmitter (DUART), serial peripherals, general purpose I/O and system timers. The introduction of Gigabit Ethernet (SGMII), High-Speed USB 2.0, and low-power management makes it unique in the marketplace.

For extremely precise clock synchronization for applications such as time-sensitive telecommunications services, industrial network switches, powerline networks and test/measurement devices, the MPC8313E features integrated IEEE® 1588 time synchronization, the leading-edge standard.

MPC8313E Block Diagram



A board support package (BSP) is preinstalled on the MPC8313E-RDB. This BSP consists of a boot loader (u-boot), a generic Power Architecture technology system based on the Linux kernel. The u-boot and the Linux kernel reside in the on-board flash memory. On powering up, the Linux system runs on the MPC8313E-RDB. The MPC8313E-RDB BSP generation takes advantage of the Linux Target Image Builder (LTIB), a suite of tools that leverages existing open source configuration scripts and source code packages and bundles them all into a single BSP generation bundle. The source code packages include boot loaders and Linux kernel sources as well as many user-space source code packages to build a complete BSP. The LTIB also provides compiler packages required to build the BSP. Freescale developers use the LTIB to create BSPs for a multitude of Freescale development markets. The LTIB leverages as many BSP elements as possible for all Freescale markets supported, while offering the flexibility necessary to customize components that require platform-specific modifications.

Many third-party applications are available for the MPC8313E-RDB. They are typically built on top of the BSP delivered by Freescale and are installed on the hard disk. To see demonstrations or to acquire details of Freescale's third-party applications for this platform, please contact your local Freescale sales office.

## MPC8313E RDB Board Features

- CPU: Freescale MPC8313E running at 333/333 MHz (CPU/DDR2)
- Memory subsystem:
  - 128 MByte unbuffered DDR2 SDRAM discrete devices
  - 8 MByte Flash single-chip memory
  - 32 MByte NAND Flash memory
  - 256 KBit M24256 serial EEPROM
  - SD connector to interface with the SD memory card in SPI mode
- Interfaces:
  - 10/100/1000 BaseT Ethernet ports:
    - eTSEC1, RGMII interface: five 10/100/1000 BaseT RJ-45 interfaces using Vitesse™ VSC7385 L2 switch
    - eTSEC2, selectable RGMII or SGMII interface: one 10/100/1000 BaseT RJ-45 interface using Mavell™ 88E1111 PHY
  - USB 2.0 port:
    - High speed host/device USB interface: selectable on-chip PHY or external ULPI PHY interface by SMSC USB3300 USB PHY
  - PCI: 32-bit PCI interface running at up to 66 MHz
    - One 32-bit 3.3V PCI slot connected to PCI bus
    - One 32-bit 3.3V miniPCI slot connected to PCI bus
  - Dual UART ports:
    - DUART interface: supports two UART up to 115200 bps for console display
- Board connectors:
  - LCD connectors by GPIO
  - ATX power supply connector
  - JTAG/COP for debugging

**Learn More:** For current information about Freescale products and documentation, please visit **www.freescale.com**.



Document Number: MPC8313ERDBREFFS
REV 1

Reference Platform Based on PowerQUICC™ Architecture

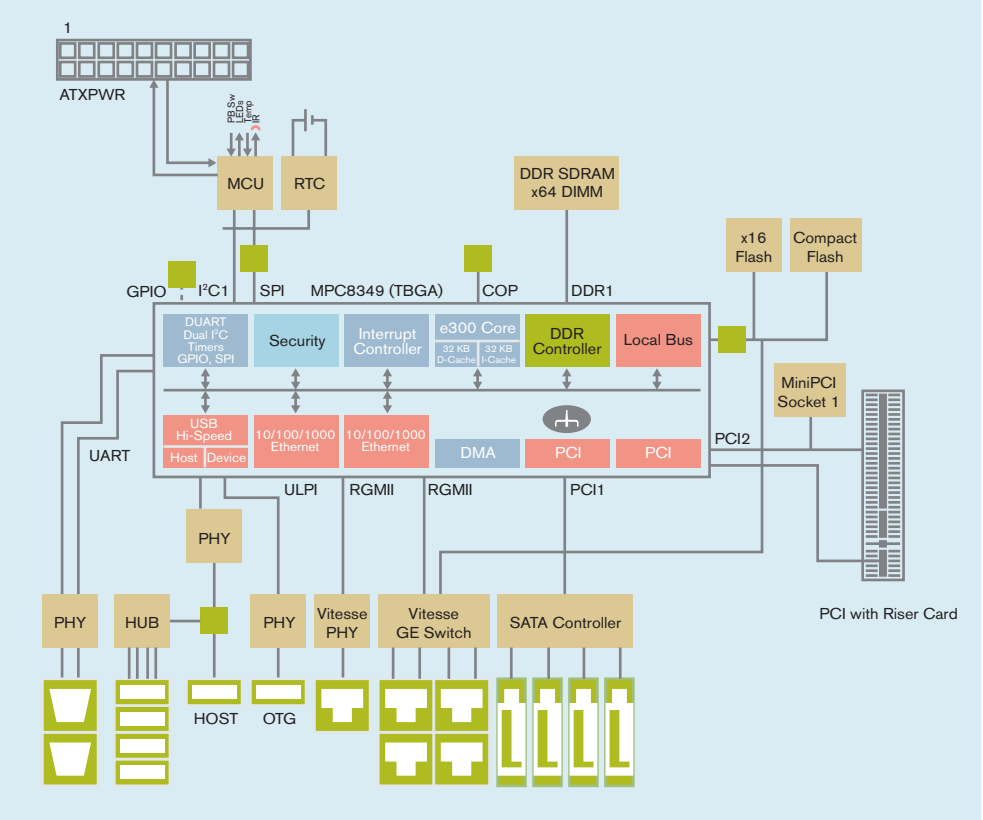
# WiMAX-Enabled CPE Solution for SOHO and Small-to-Medium Gateways

Our new integrated platform enables converged wired/wireless services and next-generation content processing-based service. The WiMAX CPE solution combines Freescale's reference boards based on the MPC8349E and MPC8323E* PowerQUICC™ II Pro processors built on Power Architecture™ technology with a Wavesat's WiMAX chipset, MiniPCI design and CPE MAC software—optimized for converged wired/wireless SOHO and SMB gateway applications. The CPE solution from Freescale and Wavesat supports WiMAX Forum 802.16d-2004 certification and is intended for upgradeability to IEEE® 802.16e-2005 standard for basic mobility in accordance with the WiMAX Forum ETG profile.

The MPC8349E mITX reference board is available in the compact mini-ITX form factor, which makes it easy to design small footprint WiMAX CPE systems. Targeting the small office/home office (SOHO) and small-medium business market, the reference board is optimized for business gateways that deliver IP-centric services. The board features the 667 MHz MPC8349E PowerQUICC II Pro processor, a robust memory subsystem, a four-port USB 2.0 interface, a 10/100/1000 Ethernet port, a five-port Gigabit Ethernet switch from Vitesse, an on-board four-port PCI serial advanced technology attachment (SATA) controller, 32-bit PCI and MiniPCI slots, a two-port RS-232C interface, a power supply and an SATA hard drive. The board ships with Linux® 2.6.x with Samba on flash. Schematics, layout files and Gerber files are available online.

*Available in Q4 2006

## MPC8349E-mITX Block Diagram




**MPC8349E-mITX reference Board**

Wavesat

freescale semiconductor

## Wavesat Evolutive™ WiMAX DM256 Chipset

The DM256 is a cost-effective, low power consumption chipset implementing the IEEE 802.16-2004 OFDM PHY layer protocol.

The PHY has two complementary functions: to process data for transmission where the output is a baseband I/Q signal or a programmable IF signal (real or complex).

The process is reversed for the second function. For data reception, the PHY implements proprietary synchronization and channel equalization methods for OFDM.

- Can be used for basestation and CPE
- Upgradeability from WiMAX fixed to 802.16e OFDM mobility
- Supports TDD, HFDD and FDD
- Industry-leading five bits per second of Hertz spectral efficiency
- 208-pin PQFP and BGA
- Programmable bandwidths and IF frequencies

### CPE MAC Software

- Complete source code is included
- Conforms to IEEE 802.16-2004
- Progressive support of additional features leading to 802.16e-2005
- High level of abstraction for operating systems—allowing for easy portability
- Based on WiMAX forum-certified CPE MAC

### 3.5 GHz MiniPCI Reference Designs

- WiMAX-certified designs for CPE
- Adaptive modulation (BPSK, QPSK, 16 quadrature amplitude modulation (QAM) and 64 QAM)
- First MiniPCI design on the market
- Meets all six SUI non line-of-sight channel models
- 37.5 Mbps of data throughput
- Support WiMAX profile: 3.5 GHz RF card, 3.5 and 7 MHz bandwidth, TDD and HFDD

### Wavesat

Wavesat is a leading fabless semiconductor company developing WiMAX chipsets, software and reference designs—enabling OEMs and ODMs to be first to market with high-performance and cost-effective WiMAX-compliant solutions.
**www.wavesat.com**

**Wavesat Chipset and MiniPCI Board**

### WiMAX Introduction

WiMAX, a broadband, last-mile, standards-based wireless technology, was conceived for data, voice and video applications over metropolitan area networks (MANs). WiMAX promises substantial bandwidth, extensive coverage, quality of service QoS) and support for a variety of wireless applications. WiMAX can provide access to fixed, portable, nomadic and mobile users. Carriers and wireless Internet service providers (WISPs) may provide WiMAX-based service, and WiMAX is also being deployed on existing wireless mesh networks.

### Freescale's Value Added Benefits

With WiMAX gaining momentum around the world, the MPC8349E-mITX WiMAX CPE reference solution is designed to enable a converged wired/wireless business gateway solution and deliver what the market needs to drive rapid deployment of broadband wireless technology in cost-effective CPE products.

### Reference Platform supports:

- Multi services
- Wired/wireless WAN/LAN interface
  - WAN: GPON/ADSL/VDSL/WiMAX
  - LAN: Ethernet, Wi-Fi, UWB, IP-PBX
- Functional integration:
  - VPN router
  - GE switch
  - IP PBX
  - Storage media server (SATA, USB)
- Common management
  - Bandwidth on demand/QoS guarantees, IPSec
  - Secured tunnel for content delivery and distribution/streaming
  - Hosted application services and free location access
- Remote diagnosis, software upgrades and management
- Platform for next-generation services including content processing

**Learn More:** For current information about Freescale products and documentation, please visit **www.freescale.com**.



Document Number: WIMAXWAVESATFS
REV 2

freescale semiconductor

Based on PowerQUICC™ Architecture

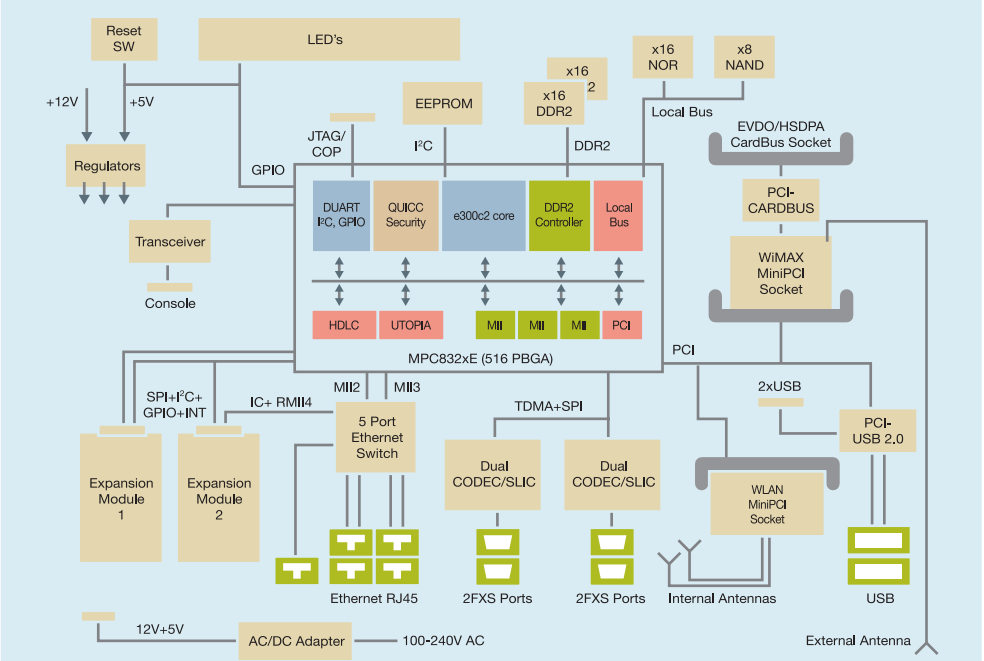
# WiMAX-Enabled CPE Production-Ready Reference Platform

**Ideal for Wireless Infrastructure, Residential and Small Office/Home Office (SOHO) Applications**

The residential gateway market is changing from just offering simple connectivity between a home network and broadband connection to handling complex quality of service (QoS) requirements and applications such as Voice-over-Internet Protocol (VoIP) and security. By partnering with Wavesat and Celestica, the solution is also WiMAX-enabled and production ready. WiMAX-Enabled CPE Production-Ready Reference Platform is a pre-developed platform for customer differentiation in the wireless telecommunications infrastructure, home and SOHO markets.

The WiMAX CPE solution is based on PowerQUICC™ II Pro processors, built on Power Architecture™ technology, with Wavesat's WiMAX chipset, MiniPCI design, CPE MAC software and a WiMAX Gateway/CPE solution from Celestica. The WiMAX CPE is a production-ready reference design optimized for converged wireless business and residential gateway applications. The integrated CPE solution from Freescale, Celestica and Wavesat supports WiMAX Forum 802.16d-2004 certification and is intended for upgradeability to IEEE® 802.16e-2005 standards for basic mobility in accordance with the WiMAX Forum ETG profile. The MPC8321E PowerQUICC II Pro is a cost-effective communications processor that meets the requirements of several SOHO, access, IP and industrial control applications. It provides better CPU performance, additional functionality and faster interfaces while addressing important time-to-market, price, power consumption and board real estate requirements.

BWA CPE Detail




**WiMAX-Enabled CPE Production-Ready Reference Platform Features Include:**

- 333 MHz Freescale MPC8321E network processor
- 32 MB DDR2 SDRAM
- 10/100 Ethernet WAN interface
- Four 10/100 Ethernet LAN interfaces
- Four FXS analog telephony ports for VoIP
- Two MiniPCI slots for wireless LAN and WiMAX support
- Four USB 2.0 High Speed host ports
- Expandable NAND flash interface

For customers seeking a pre-engineered, pre-developed solution for compressing product development cycles and driving lower costs, this platform offers numerous benefits, including:

- Support for processor and memory-intensive applications, including VoIP, advanced telephony, parental controls and cryptographic operations
- Utilization of commercial off-the-shelf MiniPCI or Cardbus WiMAX, ADSL/VDSL/VDSL2, HSDPA and EVDO adapters for maximum network backhaul interconnectivity without incurring unnecessary development costs
- Compatibility with off-the-shelf MiniPCI LAN options including Wi-Fi® for rapid deployment

CELESTICA

Wavesat

freescale semiconductor

## Wavesat Evolutive™ WiMAX DM256 Chipset

The DM256 is a cost-effective, low power consumption chipset implementing the IEEE 802.16-2004 OFDM PHY layer protocol. The PHY has two complementary functions to process data for transmission where the output is a baseband I/Q signal or a programmable IF signal (real or complex). The process is reversed for the second function. For data reception, the PHY implements proprietary synchronization and channel equalization methods for OFDM.

- Can be used for base station and CPE
- Upgradeability from WiMAX fixed to 802.16e OFDM mobility
- Supports TDD, HFDD and FDD
- Industry-leading 5-bits sec/Hertz spectral efficiency
- 208-pin PQFP and BGA
- Programmable bandwidths and IF frequency

## CPE MAC Software

- Complete source code is included
- Conforms to IEEE 802.16-2004
- Progressive support of additional features leading to 802.16e-2005
- High level of abstraction for operating system for easy portability
- Based on WiMAX Forum-certified CPE MAC

## 3.5 GHz MiniPCI Reference Designs

- A development platform to guide and support efforts in designing WiMAX-compliant wireless systems using the DM256 chipset
- Provides a plug-and-play solution for the lower layer air interface and time-critical low-level MAC functionality
- WiMAX-certified designs for CPE
- Adaptive modulation (BPSK, QPSK, 16-QAM and 64-QAM)
- First MiniPCI design on the market
- Meets all six SUI non line-of-sight channel models
- 37.5 Mbps data throughput
- Support WiMAX profile: 3.5 GHz RF card, 3.5 and 7 MHz bandwidth, TDD and HFDD

## Wavesat

Wavesat is a leading fabless semiconductor company developing WiMAX chipsets, software and reference designs, enabling OEMs and ODMs to be the first to market with high-performance and cost-effective WiMAX compliant solutions.
**www.wavesat.com**

Celestica's WiMAX Gateway/CPE solution is a production-ready solution that can be optimized with customers' intellectual property on market position. Targeted at customers in the wireless telecommunications infrastructure and SOHO markets, the CPE solution accelerator provides companies with a creative solution to shrink product design cycles and achieve full product lifecycle solutions at the lowest total cost and fastest time to market.

## Key Features and Benefits:

- Highly configurable design for production
- Leading WiMAX chipset in the industry, ensuring compatibility and a true WiMAX Forum-certified offering
- Supports Freescale PowerQUICC II Pro MPC8323, MPC8321 and MPC8313 processors
- MiniPCI-based WiMAX or other backhaul options
- MiniPCI/Cardbus-based LAN options for production
- Wavesat WiMAX optimized
- Support for CPU-intensive cryptographic operations
  - Hardware acceleration for the data encryption standard (DES, 3DES), advanced encryption standard (AES), secure hash (SHA-1) and message digest (MD5) algorithms
- Roadmap to aggressively reduce cost for production and deployment
- DDR2 DRAM interface
  - Two onboard 256 Mb to 1 Gb DDR2 devices for a total of 64 MB to 256 MB
- Five 10/100 Ethernet connections
- Four USB 2.0 High Speed host ports
- Four FXS POTS ports

## Celestica

Celestica is a world leader in the delivery of electronic manufacturing services. Celestica operates a global manufacturing network with operations in Asia, Europe and the Americas, providing a broad range of integrated service and solutions to leading original equipment manufacturers (OEMs).
**www.celestica.com**

**Learn More:** For current information about Freescale products and documentation, please visit **www.freescale.com**.



Document Number: WIMAXENCPEFS
REV 1

freescale semiconductor

Document Number: PQUICCPARCPAK
REV 0