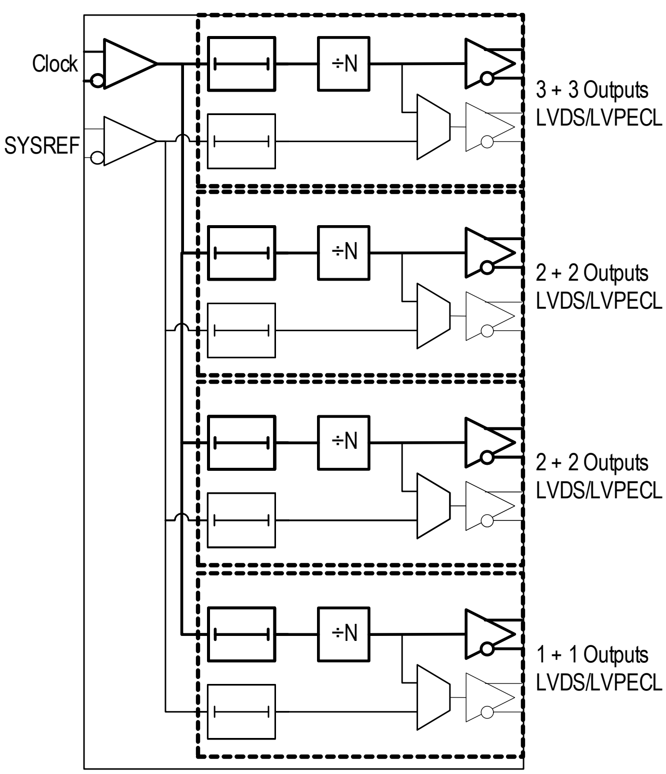
JESD204B/C Compliant Fanout Buffer and Divider

Description

The 8V79S683 is a fully integrated, clock and SYSREF signal fanout buffer for JESD204B/C applications. It is designed as a high-performance clock and converter synchronization solution for wireless base station radio equipment boards with JESD204B/C subclass 0, 1, and 2 compliance. The main function of the device is the distribution and fanout of high-frequency clocks and low-frequency system reference signals generated by a JESB204B clock generator such as the IDT 8V19N490, extending its fanout capabilities and providing additional phase-delay. The 8V79S683 is optimized to deliver very low phase noise clocks and precise, phase-adjustable SYSREF synchronization signals. Low-skew outputs, low device-to-device skew characteristics and fast output rise/fall times help the system design to achieve deterministic clock and SYSREF phase relationship across devices.

The device distributes the input clock (CLK) and JESD204B SYSREF signals (REF) to four fanout channels. Input clock signals can be frequency divided and are fanned-out to multiple clock (QCLK_y) and SYSREF (QREF_r) outputs. Configurable phase-delay circuits are available for both clock and SYSREF signals. The propagation delays in all signal paths are fully deterministic to support fixed phase relationships between clock and SYSREF signals within one device. The device facilitates synchronization between frequency dividers within the device and across multiple devices, removing phase ambiguity introduced in dividers between power and configuration cycles.

Simplified Block Diagram



Features

- Distribution, fanout, phase-delay of clock and SYSREF signals
- Very low output noise floor: -158.8dBc/Hz noise floor (245.76MHz)
- Supports clock frequencies up to 3GHz, including clock output frequencies of 983.04MHz, 491.52MHz, 245.76MHz, and 122.88MHz
- Four output channels with a total of 16 differential outputs
- Each channel contains frequency dividers and clock phase delay circuits
- Phase alignment mode across multiple buffers with any frequency divider setting
- Flexible differential outputs (LVDS/LVPECL/amplitude configurable)
- Configuration through 3-wire SPI interface
- Supply voltage:
  - 3.3V core and signal I/O
  - 1.8V Digital control SPI I/O (3.3V-tolerant inputs)
- 64-VFQFPN package (9 × 9 × 0.85 mm)
- Ambient temperature range: -40°C to +105°C (case)

Typical Applications

- Wireless infrastructure applications: 4G, 5G, and mmWave
- Frequency divider synchronization across multiple devices
- Ideal clock driver for jitter-sensitive ADC and DAC circuits
- Radar, imaging, instrumentation and medical

Applicable Standards

JESD204B/C, subclass 0, 1, and 2

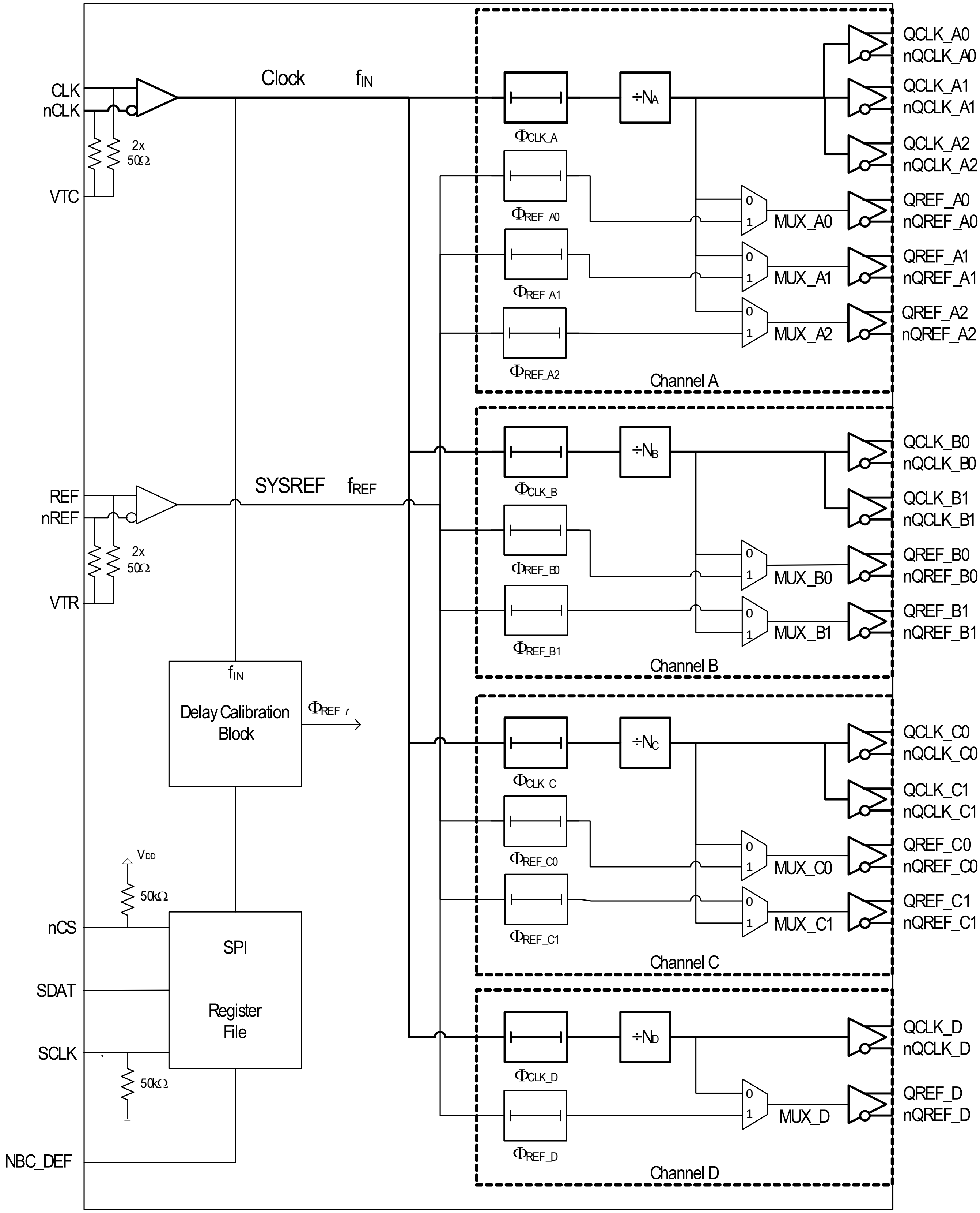
Features (Cont.)

- 4 output channels with a total of 16 differential outputs, organized in:
  - — 8 dedicated clock outputs
  - — 8 outputs configurable as SYSREF outputs with individual phase delay stages, or configurable as additional clock outputs
  - — Clock outputs are powered-on and enabled at startup
  - — QREF_r (SYSREF) outputs are disabled at startup
- Clock channel contains:
  - — frequency dividers: ÷1, ÷2, ÷3, ÷4, ÷6, ÷8, ÷12, ÷16, ÷24
  - — clock phase delay circuits, delay unit is the clock period; 256 steps
- SYSREF: Configurable precision phase delay circuits: 8 steps of 131ps, 262ps, 393ps or 524ps
- Flexible differential outputs:
  - — LVDS/LVPECL configurable
  - — Amplitude configurable
  - — Power-down modes for unused outputs
  - — Supports DC and AC coupling
  - — QREF_r (SYSREF) output pre-bias feature to prevent glitches when turning output on or off

Contents

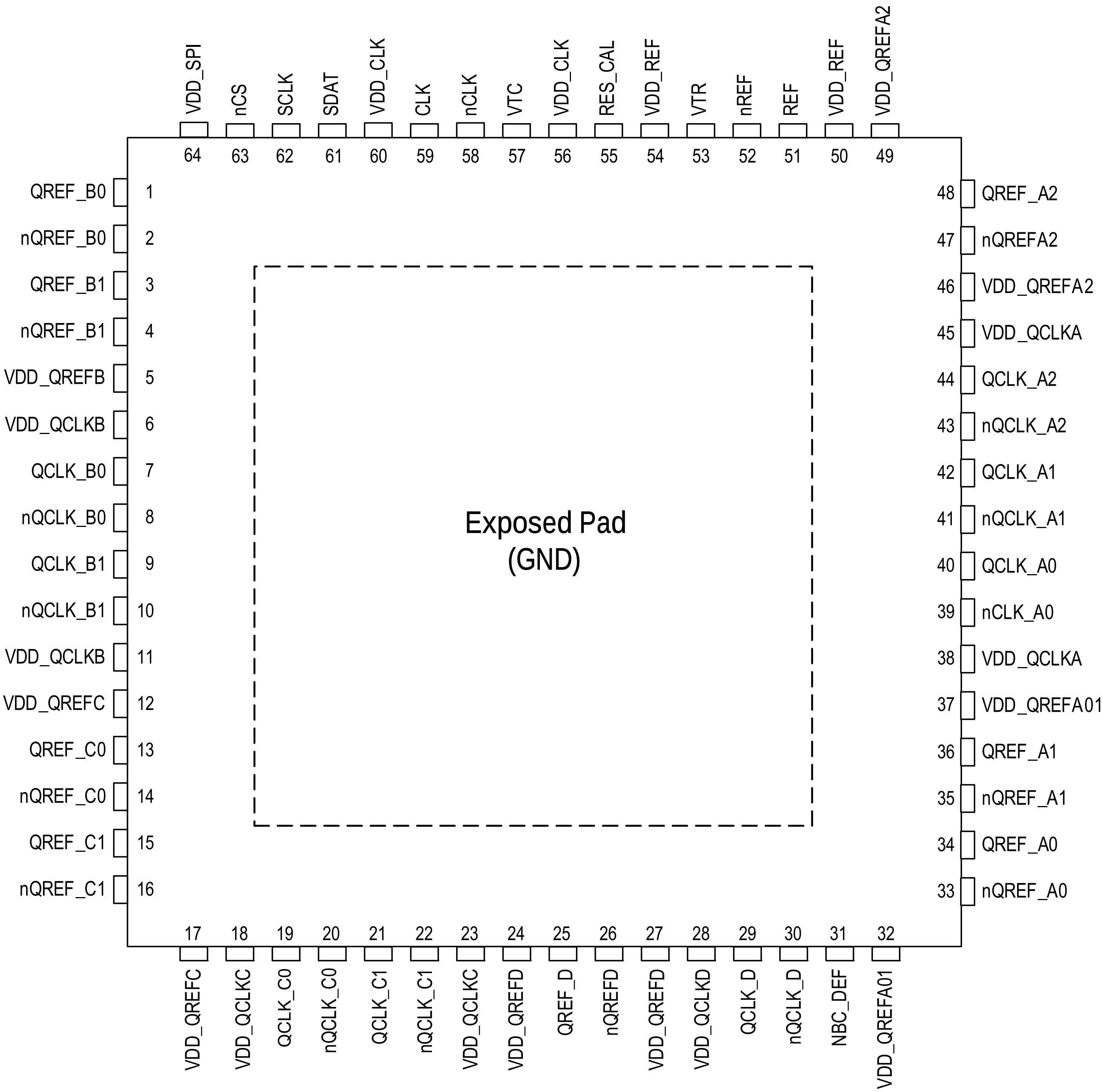
Block Diagram

Figure 1: Block Diagram



Pin Assignments

Figure 2: Pin Assignments 9 x 9 x 0.85 mm 64-VFQFPN Package (Top View)



Pin Descriptions

Table 1: Pin Descriptions

Number	Name	Type[a]		Description
1, 2	QREF_B0, nQREF_B0	Output		Differential SYSREF/clock output QREF_B0. LVDS style for SYSREF operation, configurable LVPECL/LVDS style and amplitude for clock operation.
3, 4	QREF_B1, nQREF_B1	Output		Differential SYSREF/clock output QREF_B1. LVDS style for SYSREF operation, configurable LVPECL/LVDS style and amplitude for clock operation.
5	V_{DD_QREFB}	Power		Positive supply voltage (3.3V) for the QREF_B[1:0] outputs.
6	V_{DD_QCLKB}	Power		Positive supply voltage (3.3V) for the QCLK_B[1:0] outputs.
7, 8	QCLK_B0, nQCLK_B0	Output		Differential clock output QCLK_B0. Configurable LVPECL/LVDS style and amplitude.
9, 10	QCLK_B1, nQCLK_B1	Output		Differential clock output QCLK_B1. Configurable LVPECL/LVDS style and amplitude.
11	V_{DD_QCLKB}	Power		Positive supply voltage (3.3V) for the QCLK_B[1:0] outputs.
12	V_{DD_QREFC}	Power		Positive supply voltage (3.3V) for the QREF_C[1:0] outputs.
13, 14	QREF_C0, nQREF_C0	Output		Differential SYSREF/clock output QREF_C0. LVDS style for SYSREF operation, configurable LVPECL/LVDS style and amplitude for clock operation.
15, 16	QREF_C1, nQREF_C1	Output		Differential SYSREF/clock output QREF_C1. LVDS style for SYSREF operation, configurable LVPECL/LVDS style and amplitude for clock operation.
17	V_{DD_QREFC}	Power		Positive supply voltage (3.3V) for the QREF_C[1:0] outputs.
18	V_{DD_QCLKC}	Power		Positive supply voltage (3.3V) for the QCLK_C[1:0] outputs.
19, 20	QCLK_C0, nQCLK_C0	Output		Differential clock output QCLK_C0. Configurable LVPECL/LVDS style and amplitude.
21, 22	QCLK_C1, nQCLK_C1	Output		Differential clock output QCLK_C1. Configurable LVPECL/LVDS style and amplitude.
23	V_{DD_QCLKC}	Power		Positive supply voltage (3.3V) for the QCLK_C[1:0] outputs.
24	V_{DD_QREFD}	Power		Positive supply voltage (3.3V) for the QREF_D outputs.
25, 26	QREF_D, nQREF_D	Output		Differential SYSREF/clock output QREF_D. LVDS style for SYSREF operation, configurable LVPECL/LVDS style and amplitude for clock operation.
27	V_{DD_QREFD}	Power		Positive supply voltage (3.3V) for the QREF_D outputs.
28	V_{DD_QCLKD}	Power		Positive supply voltage (3.3V) for the QCLK_D outputs.
29, 30	QCLK_D, nQCLK_D	Output		Differential clock output QCLK_D. Configurable LVPECL/LVDS style and amplitude.
31	NBC_DEF	Input	Pullup	Sets the default (power-up) value of the N_B and N_C frequency dividers.
32	$V_{DD\_QREFA01}$	Power		Positive supply voltage (3.3V) for the QREF_A[1:0] outputs.
33, 34	nQREF_A0, QREF_A0	Output		Differential SYSREF/clock output QREF_A0. LVDS style for SYSREF operation, configurable LVPECL/LVDS style and amplitude for clock operation.
35, 36	nQREF_A1, QREF_A1	Output		Differential SYSREF/clock output QREF_A1. LVDS style for SYSREF operation, configurable LVPECL/LVDS style and amplitude for clock operation.

Table 1: Pin Descriptions (Continued)

Number	Name	Type[a]		Description
37	$V_{DD\_QREFA01}$	Power		Positive supply voltage (3.3V) for the QREF_A[1:0] outputs.
38	V_{DD_QCLKA}	Power		Positive supply voltage (3.3V) for the QCLK_A[2:0] outputs.
39, 40	nQCLK_A0, QCLK_A0	Output		Differential clock output QCLK_A0. Configurable LVPECL/LVDS style and amplitude.
41, 42	nQCLK_A1, QCLK_A1	Output		Differential clock output QCLK_A1. Configurable LVPECL/LVDS style and amplitude.
43, 44	nQCLK_A2, QCLK_A2	Output		Differential clock output QCLK_A2. Configurable LVPECL/LVDS style and amplitude.
45	V_{DD_QCLKA}	Power		Positive supply voltage (3.3V) for the QCLK_A[2:0] outputs.
46	V_{DD_QREFA2}	Power		Positive supply voltage (3.3V) for the QREF_A2 output.
47, 48	nQREF_A2, QREF_A2	Output		Differential SYSREF/clock output QREF_A2. LVDS style for SYSREF operation, configurable LVPECL/LVDS style and amplitude for clock operation.
49	V_{DD_QREFA2}	Power		Positive supply voltage (3.3V) for the QREF_A2 output.
50	V_{DD_REF}	Power		Positive supply voltage (3.3V) for the differential SYSREF input REF, nREF
51, 52	REF, nREF	Input		SYSREF inverting and non-inverting differential input. Compatible with LVPECL and LVDS signals. REF and nREF are internally 50Ω terminated to the VTR pin
53	VTR	–		Internal termination for the differential clock input REF, nREF. Both REF and nREF inputs are internally terminated 50Ω to this pin. See input termination information in Section "Application Information".
54	V_{DD_REF}	Power		Positive supply voltage (3.3V) for the differential SYSREF input REF, nREF
55	RES_CAL	Analog		Connect a 2.8 kΩ (1%) resistor to GND for output current calibration.
56	V_{DD_CLK}	Power		Positive supply voltage (3.3V) for the differential device clock input CLK, nCLK.
57	VTC	–		Internal termination for the differential clock input CLK, nCLK. Both CLK and nCLK inputs are internally 50Ω terminated to the VTR pin. See input termination information in Section "Application Information".
58, 59	nCLK, CLK	Input		Device clock inverting and non-inverting differential clock input. Compatible with LVPECL and LVDS signals. CLK and nCLK are internally terminated to VTC through 50Ω.
60	V_{DD_CLK}	Power		Positive supply voltage (3.3V) for the differential device clock input CLK, nCLK.
61	SDAT	Input/ Output		Serial Control Port SPI Mode Data Input and Output. 1.8V LVCMOS/LVTTL interface levels. 3.3V tolerant when input.
62	SCLK	Input	PD	Serial Control Port SPI Mode Clock Input. 1.8V LVCMOS/LVTTL interface levels. 3.3V-tolerant when input.
63	nCS	Input	PU	Serial Control Port SPI Chip Select Input. 1.8V LVCMOS/LVTTL interface levels and 3.3V tolerant.
64	V_{DD_SPI}	Power		Positive supply voltage (3.3V) for the SPI interface.
Exposed Pad (EP)	GND	Power		Ground supply voltage (GND) and ground return path. Connect to board GND (0V).

a. Internal pull-up (PU) and pull-down (PD) resistors are indicated in parentheses. See Table 25 for values.

Principles of Operation

Overview

The 8V79S683 is a JESD204B/C Fanout Buffer with Configurable Phase Delay. The device supports the division, phase-delay and distribution of high-frequency clocks (input: CLK, nCLK) and the fanout and phase-delay of low-frequency synchronization (SYSREF) signals (input: REF/nREF). Clock and SYSREF signal paths are independent and are organized in channels, with each channel consisting of several clock and SYSREF outputs. Outputs are configurable with support for LVPECL, LVDS and four amplitude settings. Individual channels and unused circuit blocks support a powered-down state for reduced power consumption operation. The register map, accessible through a SPI interface with read-back capability controls the main device settings.

Signal Flow

The device offers four channels with the names A, B, C, and D. Each channel supports individual frequency-division, phase-delay and fan-out functions of the input clock to a total of eight QCLK_y clock outputs; each channel also distributes the SYSREF input signal to multiple QREF_r outputs with individual per-output phase delay capability.

The central clock distribution ensures low skew clock outputs within each channel; outputs are synchronous across channels (independent on the divider setting) on the incident rising clock edge for all outputs with equal phase delay settings.

SYSREF output are synchronous with each other for equal phase-delay settings. QCLK_y and QREF_r outputs will be phase-locked to each other if the CLK and REF inputs are phase-locked. The phase-delay capability in each signal path can be used to establish repeatable and deterministic clock to SYSREF phase relationships at the outputs.

The CLK and QREF signal paths are optimized for channel isolation. allowing high-speed clocks of 983.04MHz, 1474.56MHz or 1966.08MHz (up to 3GHz) and lower-speed SYSREF signals at e.g. 7.68MHz or 9.6MHz with a minimum of signal crosstalk and spurious signals.

Clock Channel Divider

Each of the four independent frequency dividers N_A-N_D can be individually set to the divider values ÷1, ÷2, ÷3, ÷4, ÷6, ÷8, ÷12, ÷16and ÷24. The dividers are synchronous and have an equal propagation delay on the incident edge. See Table 2 for the supported frequency divider settings. The default (power-up) divider value for channel A and D is ÷1, the default divider value for channel B and C is set by the state of pin 31 (NBC_DEF).

Table 2: N_{A-D} Frequency Divider Settings

N_{A-D}	Clock Divider
0000	÷1 Divider bypass and powered down
0001	÷2
0010	÷3
0011	÷4
0100	÷6
0101	÷8
0110	÷12
0111	÷16
1000	÷24

Table 3: Frequency Divider Default Settings

Divider	Default Clock Divider	
	NBC_DEF = 0	NBC_DEF = 1[a]
N_A, N_D	÷1	
N_B, N_C	÷3	÷4

a. NBC_DEF can be left open (reads logic 1)

Phase Delay

Output phase delay is independently supported on each clock channel and each SYSREF output. The delay unit of the clock channel phase-delay circuits Φ_{CLK_x} is a function of the frequency f_{IN} applied to CLK input: $1 \div f_{IN}$.

The delay unit of the SYSREF phase-delay circuits Φ_{REF_r} is a function of an internal oscillator frequency f_{DCO} and the DLC multiplier setting. The oscillator is fully self-contained and located in delay calibration block (DCB). At startup, this oscillator is calibrated with the input frequency f_{IN} as reference. After the calibration, the oscillator is turned-off to save power and to eliminate noise. See Table 4 for details on the delay unit, number of available steps and the delay range.

Table 4: Delay Circuit Characteristics

Delay Circuit	Unit	Steps	Range
Clock channel Φ_{CLK_x}	$1 \div f_{IN}$ 1.017ns at f_{IN} = 983.04MHz	256	$256 \div f_{IN}$ [a] 0 to 259.3ns at f_{IN} = 983.04MHz
SYSREF Φ_{REF_r}	T_{DCB} [b] DLC = 0: 131ps DLC = 1: 262ps DLC = 2: 393ps DLC = 3: 524ps	8	0…7 * T_{DCB} [c] DLC = 0: 0 to 0.917ns DLC = 1: 0 to 1.834ns DLC = 2: 0 to 2.751ns DLC = 3: 0 to 3.668ns

a. At f_{IN} = 983.04MHz, the clock channel delay range is equal to 260.416ns and encompasses 32 periods of a 122.88MHz clock signal.

b. $T_{DCB} \sim DLC \div (8 \cdot f_{DCO})$. f_{DCO} = 983.04MHz. DLC = 1, 2, 3 or 4.

c. SYSREF phase delay supports ≥8 delay stops within one input reference period for f_{IN} = 254.76MHz to f_{IN} = 983.04MHz.

Delay Calibration Block (DCB)

The DCB sets the *SYSREF* delay unit by providing a reference signal to the QREF_*r* delay circuits. Figure 3 shows the functional diagram. The DCB requires configuration and calibration. Verification of the calibration is optional.

Description. The DCB consists of an internal DCO running at f_{DCO} = 983.04±20MHz, three frequency dividers P_{DCB}, M_{DCB} and N_{DCB} and a digital hold circuit. The DCB input frequency is the device input frequency f_{IN} at the differential CLK, nCLK input. The input frequency acts as a reference to lock the oscillator to a stable and known frequency.

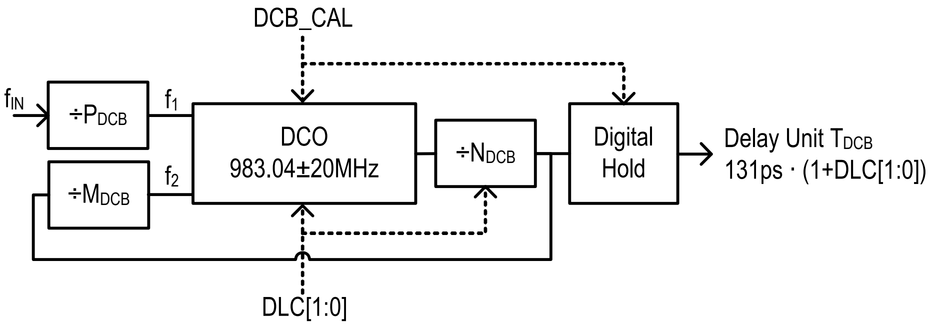
The output of the DCB is the effective delay unit T_{DCB} which is approx. one eighth of the oscillator period multiplied by the DLC multiplier. The DLC multiplier extends the delay unit by a factor of 1, 2, 3 or 4. For instance, at a DCO frequency of 983.04MHz, DLC = 1 sets the SYSREF delay unit to 131ps; DLC = 2 sets the delay unit to 262ps, etc.

Configuration. Select a desired delay unit and corresponding DLC multiplier from Table 5. DLC[1:0] also sets the N_{DCB} divider. Then, find a P_{DCB} and M_{DCB} divider configuration to locate the oscillator frequency into the range of f_{DCO} = 983.04MHz according to the formula in Figure 3. The DCO lock condition is $f_1 = f_2$ while both f_1 and f_2 must be lower than 200MHz. For instance, if f_{IN} = 245.76MHz and the smallest possible SYSREF delay unit is desired, set DLC = 1 (DLC[1:0] = 00; also sets N_{DCB} = ÷1). Then, set P_{DCB} = ÷24 and M_{DCB} = ÷96. As a result, $f_1 = f_2$ = 10.24MHz, f_{DCO} = 983.04MHz. This example configuration results in a delay unit of measured: 131ps. Figure 6 shows more configuration examples.

Calibration. Calibration requires a valid DCB configuration with the DCO locking to an input frequency. Setting DCB_CAL = 1 starts an automatic calibration. At the end, the DCB_CAL bit will clear, the delay unit value is stored digitally and the DCO, P_{DCB}, M_{DCB} and N_{DCB} frequency dividers turn off. The QREF_r delay circuits now use the stored constant delay unit. The delay unit remains digitally stored until the next power cycle. The DCB calibration must run once as part of the device startup procedure and must be re-run after each input frequency or DCB configuration change.

Verification. Verify a successful calibration by reading the DAC_CODE value. 0 < DAC_CODE< 32767 indicates a successful calibration. If DAC_CODE = 0 or DAC_CODE = 32767, the DCB calibration should be re-run with an alternative P_{DCB}, M_{DCB} setting while maintaining the desired $M_{DCB} \cdot N_{DCB}/P_{DCB}$ ratio for locking the DCO to the input frequency.

Figure 3: DCB Functional Diagram



$$\frac{f_{IN}}{P_{DCB}} = \frac{f_{DCO}}{M_{DCB} \cdot N_{DCB}}$$

$$f_{DCO} = 983\text{MHz} \pm 20\text{MHz}$$

Table 5: DCB Delay Unit at f_{DCO} = 983.04MHz

T_{DCB} Delay Unit (ps)	DLC		N_{DCB}
	DLC[1:0] Setting	Numeric Value	
131	00	1	1
262	01	2	2
393	10	3	3
524	11	4	4

Table 6: DCB Divider Configuration Examples[a]

f_{IN} (MHz)	T_{DCB} Delay Unit in ps	DLC	P_{DCB}	M_{DCB}
245.76	131	1	24	96
	262	2	24	48
	393	3	24	32
	524	4	24	24
491.52	131	1	48	96
	262	2	48	48
	393	3	48	32
	524	4	48	24
983.04	131	1	96	96
	262	2	96	48
	393	3	96	32
	524	4	96	24

a. f_{DCO} = 983.04MHz

QCLK_y to SYSREF Phase Alignment

Single Device: To achieve an output phase alignment between the QCLK_*y* clock and the QREF_*r* SYSREF outputs, the CLK and REF input signals must be phase aligned or have a known, deterministic phase relationship. Figure 4 shows an example output phase alignment for aligned clock and SYREF inputs. The closest (smallest phase error) output alignment is achieved by setting the clock phase delay register Φ_{QCLK_Y} to 0x00 (clock) and the SYSREF phase delay register Φ_{QCLK_Y} to 0x04. With a SYSREF phase delay setting of 0x03 or less, the QREF_*r* output phase is in advance of the QCLK_y phase, which is applicable in JESD204B/C application. Phase delay settings and propagation delays are independent on the clock and SYSREF frequencies. Table 7 shows recommended phase delay setting several device configurations.

Figure 4: QCLK_y to QREF Phase Alignment

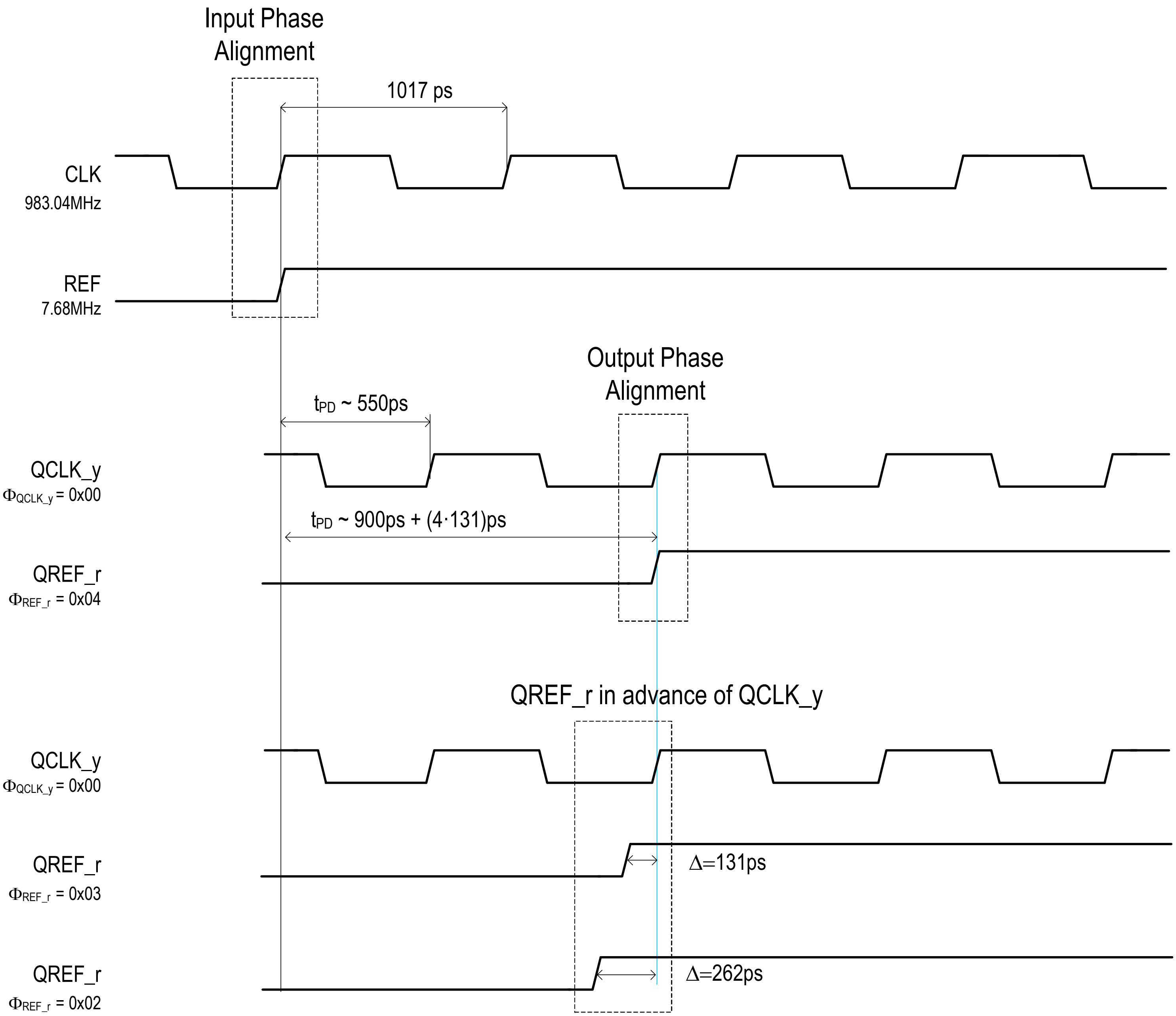


Table 7: Recommended Delay Settings for Closest Clock-SYSREF Output Phase Alignment[a]

Divider Configuration	ΦCLK_y	ΦREF_r
N = ÷1	0x00	0x04

a. QCLK_y and QREF outputs are aligned on the incident edge.

QCLK_y and QREF_r Phase Alignment Across Multiple 8V79S683 Devices

The device architecture supports phase aligned QCLK_*y* and QREF_*r* output signals across multiple 8V79S683NLGI devices. For applications that use the frequency dividers of ÷2, ÷3, ÷4, ÷6, ÷8, ÷12, ÷16 or ÷24, or any combination of these dividers, all devices participating in the output phase alignment must go through a specific alignment procedure at device startup

Pre-conditions

- Each 8V79S683NLGI device must be driven by a clock device that keeps clock and SYSREF signals aligned at the CLK and REF inputs (see setup and hold time specification)
- The frequency on the REF input must be smaller than any QCLK_y output frequency
- A valid input frequency must be applied to the CLK input, for instance 491.52MHz

Alignment Method

- Phase alignment is achieved by driving the all REF inputs with a rising edge signal at the same time with respect to the CLK input signal
- During the alignment process, the output period of the divided clock signal (on QCLK_y outputs) will have longer periods until output alignment is achieved
  - — Example: input CLK frequency is 491.52MHz, output divider is ÷4, output frequency is 122.88MHz. During the alignment procedure started by REF, the QCLK_y output period changes from 8.138ns to 10.172ns for multiple cycles. The device facilitates the period of the input signal (2.034ns) to “stretch” the output period: 8.138 ns + 2.034 ns = 10.172 ns

Alignment Procedure

- Set the MD_ALIGN_Φ bit to enable the alignment procedure
  - — wait for ≥5 µs before applying a signal to the REF input
- Apply an alignment signal (rising edge) to the REF input
  - — place the rising edge REF signal before the rising edge of the CLK signal that is shared between all participating buffers
  - — REF to CLK setup and hold time specification must be met
  - — a single REF rising edge is sufficient for starting the alignment
- Output behavior during alignment:
  - — QCLK_y outputs in ÷1 divider mode work normally as expected without cycle slips or period increases
  - — QCLK_y outputs in ÷2, ÷3, ÷4, ÷6, ÷8, ÷12, ÷16 or ÷24 divider mode expose longer periods as described above
  - — REF outputs always buffer out the REF input signal (when QREF_r outputs are powered on and are enabled)

Result

- — The procedure aligns the output phases (rising incident edge) of all QCLK_y output signals across participating buffers. This includes the output phases of the frequency-divided clock signals and the outputs divided by 1
- — The input to output delay is the same across all participating buffer devices (measured on the incident edge)
- — The alignment procedure has a maximum duration of $48\times(1 \div f_{IN})$
- — After alignment is achieved, the device auto-clears the MD_ALIGN_Φ register bit

The alignment procedure can be repeated at any time after setting the MD_ALIGN_Φ bit.

Table 8: MD_ALIGN_Φ Multi-Device Phase Alignment Function Table

MD_ALIGN_Φ	Operation	Comment
0 (default)	Multi-buffer phase alignment is disabled	SYSREF signals at the REF input are buffered out to the SYSREF outputs when output buffers are enabled.
1	A rising edge at the REF input will start an output phase alignment procedure	Requires a valid clock signal at the CLK input. REF to CLK setup and hold time specifications have to be met. This bit auto-clears after alignment is achieved.

Differential Outputs

Table 9: Output Features

Output	Style	Amplitude[a]	Disable	Power Down	DC Bias	Termination
QCLK_*y*[b], QREF_*r*[c] (Clock)	LVPECL	350-1000mV 3 steps	Yes	Yes	–	50Ω to V_T[d]
	LVDS	350, 750mV 2 steps				100Ω differential[e f]
QREF_*r* (SYSREF)	LVPECL	350-1000mV 3 steps	Yes	Yes	–	50Ω to V_T[d]
	LVDS	350, 750mV 2 steps			Yes[g]	100Ω differential[e f]

a. Amplitudes are measured single-ended. Differential amplitudes supported are 700mV, 1500mV and 2000mV.

b. y = A0, A1, A2, B0, B1, C0, C1 and D.

c. r = A0, A1, A2, B0, B1, C0, C1 and D.

d. $V_T = V_{DD\_V}$ – 1.6V (350mV amplitude setting), V_{DD_V} – 2.0V (750mV amplitude setting), V_{DD_V} – 2.25V (1000mV amplitude setting).

e. AC coupling and DC coupling supported.

f. See Application Information for output termination information.

g. In JESD204B/C applications, it is recommended to use QREF_r (SYSREF) outputs configured to LVDS and 350mV amplitude. AC-coupling and DC-coupling is supported.

Table 10: Individual Clock Output (QCLK_y) Settings[a]

PD	STYLE	EN	A[1:0]	Output Power	Termination[b]	State	Amplitude (mV)
1	X	X	X	Off	100Ω differential (LVDS) or no termination	Off	X
0	0	0	XX	On	100Ω differential (LVDS)	Disable[c]	X
		1	00			Enable	350
			01				750
	1	0	XX		50Ω to V_T (LVPECL)	Disable	X
		1	00			Enable	350
			01				750
			10				1000
			11				1000

a. Applicable to clock outputs: QCLK_*y* and QREF_*r* outputs in clock mode (MUX_*r* = 0).

b. See Application Information for output termination information.

c. Differential output is disabled in static low state: QCLK_*y* = L, nQCLK_*y* = H.

Table 11: Individual SYSREF Output (QREF_r) Settings[a]

PD	STYLE	Enable	A[1:0]	BIAS	Output Power	Termination[b]	State	Amplitude (mV)
1	X	X	X	X	Off	100Ω differential or no termination	Off	X
0	0	0	XX	0	On	100Ω differential (LVDS)	Disable[c]	X
		1	00	0			Enabled	350
			01	0			See Table 12	750
				1			Enabled	
	1	0	XX	0		50Ω to V_T (LVPECL)	Disable	X
		1	00				Enable	350
			01					750
			10					1000
			11					1000

a. Applicable QREF_*r* outputs when configured as SYSREF output (MUX_*r* = 1).

b. See Application Information for output termination information.

c. Differential output is disabled in static low state: QCLK_*y* = L, nQCLK_*y* = H.

Table 12: QREF_r Setting for JESD204B/C Applications

BIAS_TYPE	BIAS_*r*	QREF_r Outputs (LVDS)			Application
		Initial	Active Rising Edge on the REF Input	SYSREF Completed	
0	0	Static Low (QREF = L, nQREF_*r* = H)	Start switching for the number of received SYSREF pulses	Released to static low (QREF = L, nQREF_*r* = H)	QREF_*r* DC coupled
	1	Static Low (QREF = L, nQREF_*r* = H)			
1	0	Static LVDS crosspoint level (QREF = nQREF_*r* = VOS)	Start switching for the number of received SYSREF pulses	Released to static LVDS crosspoint level (QREF = nQREF_*r* = VOS)	QREF_*r* AC coupled
	1	Static LVDS crosspoint level (QREF = nQREF_*r* = VOS)			

Device Startup, Reset, and Synchronization

At startup, an internal POR (power-on reset) resets the device and sets all register bits to its default value. The default divider value of the NB and NC frequency dividers is set by the state of the NBC_DEF pin. After internal POR, the device will initialize internal circuits and for 2ms before it accepts an external clock signal at the CLK input (the CLK input is internally turned off during that time).

In the default configuration the QCLK_*y* outputs are enabled, QREF outputs are disabled at startup.

Recommended configuration sequence (in order):

1. (Optional) set the value of the CPOL register bit to define the SPI read mode, so that SPI settings can be validated by subsequent SPI read accesses.
2. Verify the completion of internal power-up by reading the ST_READY status bit in register 0x6E, bit D1. ST_READY is set to 1 by the device at the end of the internal power-up procedure. Continue the device startup once ST_READY is set to 1.
3. Configure the channel circuits and the outputs to the desired values and configure the DCB:
   - For synchronization between multiple devices: See section QCLK_y and QREF_r Phase Alignment Across Multiple 8V79S683 Devices. After the MD_ALIGN_Φ bit is set, the device will wait for a REF rising edge input to start the phase alignment. After alignment is completed, the MD_ALIGN_Φ bit will auto-clear. The multi-device alignment requires a valid clock signal to be applied to the CLK input.
   - Output source MUX_r, output divider $N_{A\text{-}D}$, clock delay $\Phi_{A\text{-}D}$; MUX-output style, amplitude and power down mode for QCLK_*y* and QREF_*r* outputs
   - (Optional) the global BIAS_TYPE bit and BIAS_*r* for each QREF_r in preparation for JESD204B/C SYSREF operation
   - Phase delay for Φ_{REF_r} values for the QREF_*r* outputs
   - Setup the DCB settings DLC, P_{DCB} and M_{DCB} as described in the paragraph *Configuration*, see Delay Calibration Block (DCB)
4. If not already applied: apply a valid input frequency to CLK. Set the PB_CAL bit and the DCB_CAL bit to start the calibration of the precision bias current circuit and the DCB calibration. Both bits will auto-clear. *See* paragraph *Configuration* in section Delay Calibration Block (DCB).
   - (Optional): verify the success of the DCB calibration by reading the DAC_CODE value. *See* paragraph *Verification* in section Delay Calibration Block (DCB)
5. (Only for using the clock delay circuits): Set the initialization bit INIT_CLK to initiate the ΦCLK_*x* delay circuits. The INIT_CLK bit will self-clear. During this initialization step, all QCLK_y and QREF_*r* outputs are reset to the logic low state.
6. Enable or disable outputs as desired by accessing the output-enable registers 0x74 and 0x76.
7. At this point, the configuration of the registers should be completed and the SPI transfer ended. Set nCS to high level.

Registers in the address range 0x78 to 0xFF should not be used. Do not write into any registers in the 0x78 to 0xFF range.

Changing Frequency Dividers and Phase Delay Values

Clock Frequency Divider and Delay

Following procedure has to be applied for a change of a clock divider and phase delay value $N_{A-D,}$ and $\Phi_{CLKA-D:}$

1. (Optional) set the value of the CPOL register to define the SPI read mode, so that SPI settings can be validated by subsequent SPI read accesses.
2. (Optional) disable the outputs whose frequency divider or delay value is changed
3. Configure the N_{A-D} dividers and the delay circuits Φ_{CLKA-D} to the desired new values
4. Set the initialization bit INIT_CLK. This will initiate all divider and delay circuits and synchronize them to each other. The INIT_CLK bit will self-clear. During this initialization step, all QCLK_y and QREF_*r* outputs are reset to the logic low state
5. (Optional) Enable the outputs whose frequency divider was changed

SYSREF Delay

Following procedure has to be applied for a change of any SYSREF phase delay value $\Phi_{REF\_r:}$

1. (Optional) set the value of the CPOL register to define the SPI read mode, so that SPI settings can be validated by subsequent SPI read accesses.
2. Configure any delay circuits Φ_{REF_r} to their desired new values. During configuration of Φ_{REF_r} outputs are not stopped or interrupted.

SPI Interface

The 8V79S683 has a 3-wire serial control port capable of responding as a slave in an SPI configuration to allow read and write access to any of the internal registers for device programming or read back. The SPI interface consists of the SCLK (clock), SDAT (serial data input and output), and nCS (chip select) pins. A data transfer consists of any integer multiple of 8 bits and is always initiated by the SPI master on the bus. Internal register data is organized in SPI bytes of 8 bits each. If nCS is at logic high, the SDAT data I/O is in high-impedance state and the SPI interface of the 8V79S683 is disabled. In a write operation, data on SDAT will be clocked in on the rising edge of SCLK. In a read operation, data on SDAT will be clocked out on the falling or rising edge of SCLK depending on the CPOL setting (CPOL = 0: output data changes on the falling edge, CPOL = 1: output data changes on the rising edge).

Starting a data transfer requires nCS to set and hold at logic low level during the entire transfer. Setting nCS = 0 will enable the SPI interface with SDAT in data input mode. The master must initiate the first 8-bit transfer. The first bit presented to the slave is the direction bit R/nW (1 = Read, 0 = Write) and the following seven bits are the address bits A[0:6] pointing to an internal register in the address space 0 to 127. Data is presented with the LSB (least significant bit) first.

Read operation from an internal register: a read operation starts with an 8 bit transfer from the master to the slave: SDAT is clocked on the rising edge of SCLK. The first bit is the direction bit R/nW which must be to 1 to indicate a read transfer, followed by 7 address bits A[0:6]. After the first 8 bits are clocked into SDAT, the SDAT I/O changes to output: the register content addressed by A[0:6] is loaded into the shift register and the next 8 SCLK falling clock cycles (if CPOL = 0) will then present the loaded register data on the SDAT output and transfer these to the master. Transfers must be completed by de-asserting nCS after any multiple 8 SCLK cycles. If nCS is de-asserted at any other number of SCLKs, the SPI behavior is undefined. SPI byte (8 bit) and back-to-back read transfers of multiple registers are supported with an address auto-increment. During multiple transfers, nCS must stay at logic low level and SDAT will present multiple registers (A), (A+1), (A+2), etc. with each 8 SCLK cycles. During SPI Read operations, the user may continue to hold nCS low and provide further bytes in a single block read.

Write operation to a 8V79S683 register: During a write transfer, a SPI master transfers one or more bytes of data into the internal registers of the 8V79S683. A write transfer starts by asserting nCS to low logic level. The first bit presented by the master must set the direction bit R/nW to 0 (Write) and the 7 address bits A[0:6] must contain the 7-bit register address. Bits D0 to D7 contain 8 bit of payload data, which is written into the register addressed by A[0:6] at the end of a 8-bit write transfer. Multiple, subsequent register transfers from the master to the slave are supported by holding nCS asserted at logic low level during write transfers. The 7 bit register address will auto-increment. Transfers must be completed by de-asserting nCS after any multiple 8 SCLK cycles. If nCS is de-asserted at any other number of SCLKs, the SPI behavior is undefined.

End of transfer: After de-asserting nCS, the SPI bus is available to transfers to other slaves on the SPI bus. See also the READ diagram (Figure 5) and WRITE diagram (Figure 6) displaying the transfer of two bytes of data from and into registers

Registers 0x78 to 0xFF: Registers in the address range 0x78 to 0xFF should not be used. Do not write into any registers in the 0x78 to 0xFF range.

Figure 5: Logic Diagram: READ Data from 8V79S683 Registers for CPOL = 0 and CPOL = 1

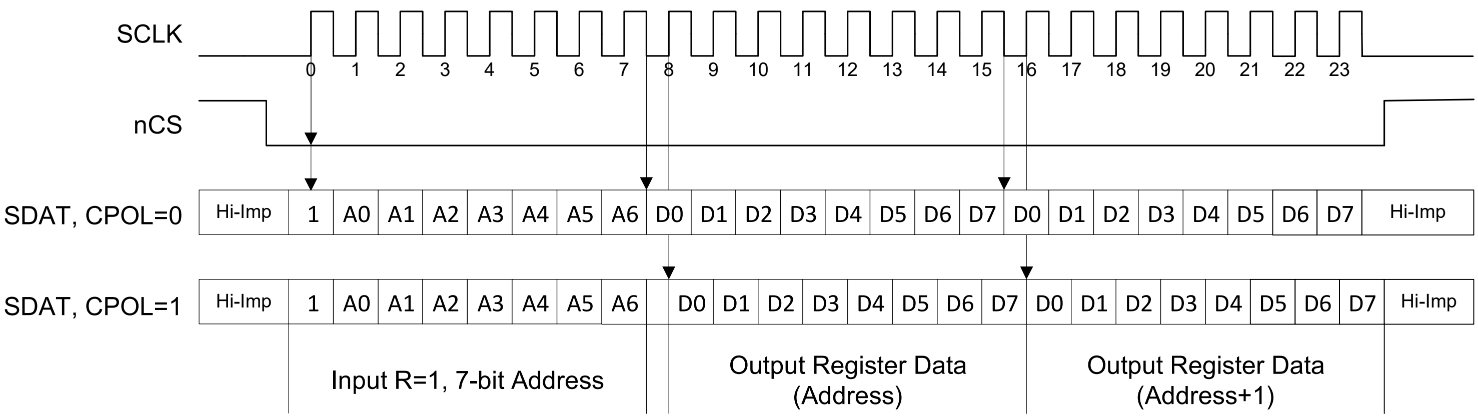


Figure 6: Logic Diagram WRITE Data into 8V79S683 Registers

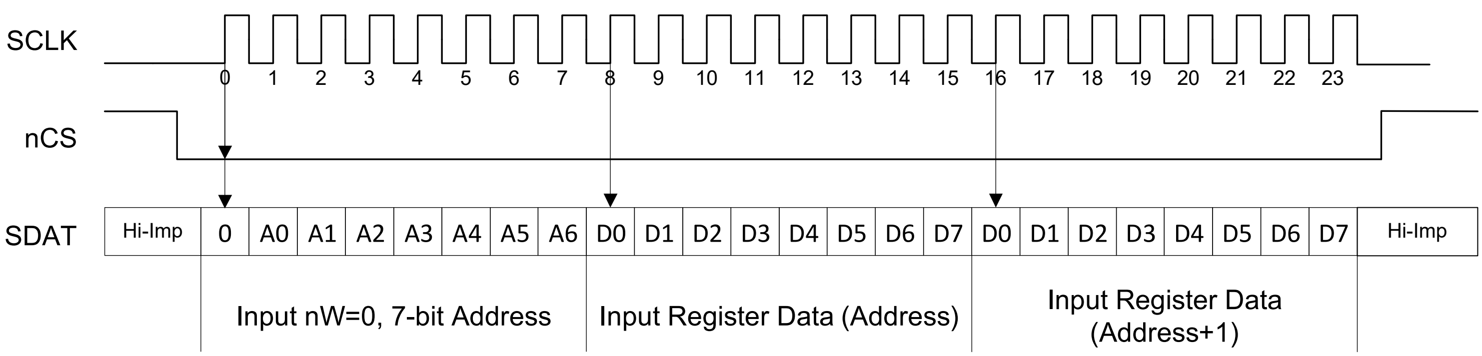
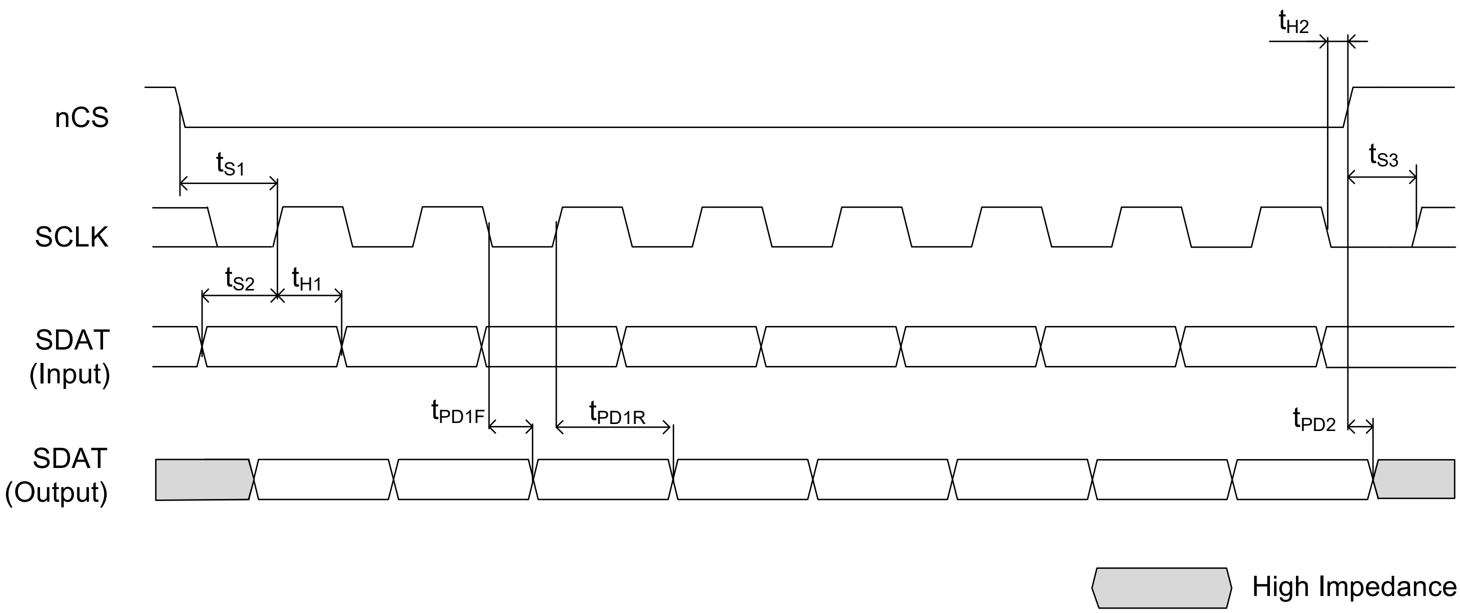


Table 13: SPI Read / Write Cycle Timing Parameters

Symbol	Parameter	Test Condition	Minimum	Maximum	Unit
f_{SCLK}	SCLK frequency			20	MHz
t_{S1}	Setup time, nCS (falling) to SCLK (rising)		5		ns
t_{S2}	Setup time, SDAT (input) to SCLK (rising)		5		ns
t_{S3}	Setup time, nCS (rising) to SCLK (rising)		5		ns
t_{H1}	Hold time, SCLK (rising) to SDAT (input)		5		ns
t_{H2}	Hold time, SCLK (falling) to nCS (rising)		5		ns
t_{PD1F}	Propagation delay, SCLK (falling) to SDAT	CPOL = 0		12	ns
t_{PD1R}	Propagation delay, SCLK (rising) to SDAT	CPOL = 1		12	ns
t_{PD2}	Propagation delay, nCS to SDAT disable			12	ns
$t_{R, F}$	Rise, Fall Time, SPI Inputs SCLK, SDAT		1	10	ns

Figure 7: SPI Timing Diagram



Register Descriptions

This section contains a list of all addressable registers and a register description, sorted by function, followed for a detailed description of each bit field for each register. Several functional blocks with multiple instances in this device have individual registers controlling their settings, but since the registers have an identical format and bit meaning, they are described only once, but with an additional table to indicate their addresses and default values. All writable register fields will come up with a default values as indicated in the Factory Defaults column unless altered by values loaded from non-volatile storage during the initialization sequence.

Fixed read-only bits will have defaults as indicated in their specific register descriptions. Read-only status bits will reflect valid status of the conditions they are designed to monitor once the internal power-up reset has been released. Unused registers and bit positions are Reserved. Reserved bit fields will be unaffected by writes and are undefined on reads.

Table 14: Configuration Registers

Register Address	Register Description
0x00 - 0x17	Reserved
0x18 - 0x1B	SYSREF, DCB and Phase Alignment Control
0x1C - 0x1F	Reserved
0x20	Channel A, Output Divider
0x21	Channel A Delay ΦCLK_*A*
0x22	Channel A PD
0x23	Reserved
0x24	Output State QCLK_*A0*
0x25	Output State QCLK_*A1*
0x26	Output State QCLK_*A2*
0x27	Reserved
0x28	ΦREF_A0 Delay, MUX

Table 14: Configuration Registers (Continued)

Register Address	Register Description
0x29	ΦREF_A1 Delay, MUX
0x2A	ΦREF_A2 Delay, MUX
0x2B	Reserved
0x2C	Output State QREF_A0
0x2D	Output State QREF_A1
0x2E	Output State QREF_A2
0x2F	Reserved
0x30	Channel B, Output Divider
0x31	Channel B Delay ΦCLK_*B*
0x32	Channel B PD
0x33	Reserved
0x34	Output State QCLK_*B0*
0x35	Output State QCLK_*B1*
0x36 - 0x37	Reserved
0x38	ΦREF_B0 Delay, MUX
0x39	ΦREF_B1 Delay, MUX
0x3A-0x3B	Reserved
0x3C	Output State QREF_B0
0x3D	Output State QREF_B1
0x3E-0x3F	Reserved
0x40	Channel C, Output Divider
0x41	Channel C Delay ΦCLK_*C*
0x42	Channel C PD
0x43	Reserved
0x44	Output State QCLK_*C0*
0x45	Output State QCLK_*C1*
0x46-0x47	Reserved
0x48	ΦREF_C0 Delay, MUX
0x49	ΦREF_C1 Delay, MUX
0x4A-0x4B	Reserved
0x4C	Output State QREF_C0
0x4D	Output State QREF_C1
0x4E-0x4F	Reserved
0x50	Channel D, Output Divider

Table 14: Configuration Registers (Continued)

Register Address	Register Description
0x51	Channel D Delay ΦCLK_*D*
0x52	Channel D PD
0x53	Reserved
0x54	Output State QCLK_*D*
0x55-0x57	Reserved
0x58	ΦREF_D Delay, MUX
0x59-0x5B	Reserved
0x5C	Output State QREF_D
0x5D-0x6B	Reserved
0x6C-0x73	General Control
0x74	Output State QCLK
0x75	Reserved
0x76	Output State QREF
0x77	Reserved
0x78	Do not use
0x79	Do not use
0x7A	Do not use
0x7B	Do not use
0x7C-0x7D	Do not use
0x7E	Do not use
0x7F	Do not use
0x80-0xFF	Do not use

Channel and Clock Output Registers

The content of the channel register and clock output registers set the clock divider, output style, amplitude, power down state, enable state and the clock phase delay.

Table 15: Channel and Clock Output Register Bit Field Locations

Bit Field Location								
Register Address	D7	D6	D5	D4	D3	D2	D1	D0
0x20 0x30 0x40 0x50	Reserved	Reserved	Reserved	Reserved	N_*A*[3:0] N_*B*[3:0] N_*C*[3:0] N_*D*[3:0]			
0x21 0x31 0x41 0x51	ΦCLK_*A*[7:0] ΦCLK_*B*[7:0] ΦCLK_*C*[7:0] ΦCLK_*D*[7:0]							
0x22 0x32 0x42 0x52	PD_*A* PD_*B* PD_*C* PD_*D*	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0x24: QCLK_A0 0x25: QCLK_A1 0x26: QCLK_A2	PD_*A0* PD_*A1* PD_*A2*	Reserved	Reserved	STYLE_*A0A1* Reserved STYLE_*A2*	A_*A0A1*[1:0] Reserved A_*A2*[1:0]		Reserved	
0x34: QCLK_B0 0x35: QCLK_B1	PD_*B0* PD_*B1*	Reserved	Reserved	STYLE_*B0B1* Reserved	A_*B0B1*[1:0] Reserved		Reserved	
0x44: QCLK_C0 0x45: QCLK_C1	PD_*C0* PD_*C1*	Reserved	Reserved	STYLE_*C0* STYLE_*C1*	A_*C0*[1:0] A_*C1*[1:0]		Reserved	
0x54: QCLK_D	PD_*D*	Reserved	Reserved	STYLE_*D*	A_*D*[1:0]		Reserved	
0x74	EN_QCLK_A0	EN_QCLK_A1	EN_QCLK_A2	EN_QCLK_B0	EN_QCLK_B1	EN_QCLK_C0	EN_QCLK_C1	EN_QCLK_D

Table 16: Channel and Clock Output Register Descriptions[a]

Register Description			
Bit Field Name	Field Type	Default (Binary)	Description
N_*x*[3:0]	R/W	N_*A* = 0000 (÷1) N_*B* = 001[NBC_DEF] (÷4/÷3) N_*C* = 001[NBC_DEF] ÷4/÷3 N_*D* = 0000 (÷1)	Output Frequency Divider N N_*x*[2:0] — Frequency Divider 0000 — ÷1 (Divider bypassed and powered-down) 0001 — ÷2 0010 — ÷3 0011 — ÷4 0100 — ÷6 0101 — ÷8 0110 — ÷12 0111 — ÷16 1000 — ÷24 The default value of the N_B and N_C divider is set by pin 31 (NBC_DEF). See Table 3.
PD_*x*	R/W	0 Value: Power up	0 = Channel *x* is powered up 1 = Channel *x* is powered down
PD_*y*	R/W	0 Value: Power up	0 = Output QCLK_*y* is powered up 1 = Output QCLK_*y* is powered down
ΦCLK_*x*[7:0]	R/W	0000 0000 Value: 0ns	CLK_*x* Phase Delay ΦCLK_*x*[7:0] — Phase Delay in units of the input period: ΦCLK_*x*[7:0] ÷ f_{IN} (256 steps). 0000 0000 — 0ps 0000 0001 — 1 ÷ f_{IN} … — … 1111 1111 — 255 ÷ f_{IN}

Table 16: Channel and Clock Output Register Descriptions[a]

<table>
<tr><th colspan="5">Register Description</th></tr>
<tr><th>Bit Field Name</th><th>Field Type</th><th>Default (Binary)</th><th colspan="2">Description</th></tr>
<tr><td rowspan="4">A_*y*[1:0]</td><td rowspan="4">R/W</td><td rowspan="4">01

Value: 750mV</td><td colspan="2">QCLK_*y* Output Amplitude</td></tr>
<tr><td>Setting for STYLE = 0 (LVDS)
Termination: 100Ω across</td><td>Setting for STYLE = 1 (LVPECL)
Termination: 50Ω to V_T</td></tr>
<tr><td>A[1:0] = 00: 350mV
A[1:0] = 01: 750mV
A[1:0] = 10: Reserved
A[1:0] = 11: Reserved</td><td>A[1:0] = 00: 350mV
A[1:0] = 01: 750mV
A[1:0] = 10: 1000mV
A[1:0] = 11: 1000mV</td></tr>
<tr><td colspan="2">The following control bits combine the A(mplitude) function for multiple outputs:
A_*A0A1* sets the output amplitude for QCLK_A0 and QCLK_A1
A_*B0B1* sets the output amplitude for QCLK_B0 and QCLK_B1</td></tr>
<tr><td>STYLE_*y*</td><td></td><td>0

Value: LVDS</td><td colspan="2">QCLK_*y* Output Format.

0 = Output(s) is/are LVDS (requires LVDS 100Ω output termination)
1 = Output(s) is LVPECL (requires LVPECL 50Ω output termination to the specified recommended termination voltage)

The following control bits combine the STYLE function for multiple outputs:
STYLE_*A0A1* sets the output format for QCLK_A0 and QCLK_A1
STYLE_*B0B1* sets the output format for QCLK_B0 and QCLK_B1</td></tr>
<tr><td>EN_*y*</td><td></td><td>1

Value: enabled</td><td colspan="2">QCLK_*y* Output Enable:
0 = QCLK_*y* Output is disabled at the logic low state
1 = QCLK_*y* Output is enabled</td></tr>
</table>

a. *x* = A, B, C, D; *y* = A0, A1, A2, B0, B1, C0, C1, D.

QREF_r Output State Registers

The content of the QREF_r output registers selects the source signal of the QREF_r outputs, set the phase delay, the style, the amplitude, the power state, the enable state and the output bias.

Table 17: QREF_r Output State Register Bit Field Locations[a]

Bit Field Location								
Register Address	D7	D6	D5	D4	D3	D2	D1	D0
0x28: QREF_A0 0x29: QREF_A1 0x2A:QREF_A2	Reserved	Reserved	Reserved	MUX_*A0* MUX_*A1* MUX_*A2*	ΦREF_*A0*[2:0] ΦREF_*A1*[2:0] ΦREF_*A2*[2:0]			Reserved
0x38: QREF_B0 0x39: QREF_B1	Reserved	Reserved	Reserved	MUX_*B0* MUX_*B1*	ΦREF_*B0*[2:0] ΦREF_*B1*[2:0]			Reserved
0x48: QREF_C0 0x49: QREF_C1	Reserved	Reserved	Reserved	MUX_*C0* MUX_*C1*	ΦREF_*C0*[2:0] ΦREF_*C1*[2:0]			Reserved
0x58: QREF_D	Reserved	Reserved	Reserved	MUX_*D*	ΦREF_*D*[2:0]			Reserved
0x2C: QREF_A0 0x2D: QREF_A1 0x2E: QREF_A2	PD_*A0* PD_*A1* PD_*A2*	Reserved	BIAS_*A0* BIAS_*A1* BIAS_*A2*	STYLE_*A0* STYLE_*A1* STYLE_*A2*	A_*A0*[1:0] A_*A1*[1:0] A_*A2*[1:0]		Reserved	Reserved
0x3C: QREF_B0 0x3D: QREF_B1	PD_*B0* PD_*B1*	Reserved	BIAS_*B0* BIAS_*B1*	STYLE_*B0* STYLE_B1	A_*B0*[1:0] A_*B1*[1:0]		Reserved	Reserved
0x4C: QREF_C0 0x4D: QREF_C1	PD_*C0* PD_*C1*	Reserved	BIAS_*C0* BIAS_*C1*	STYLE_*C0* STYLE_C1	A_*C0*[1:0] A_*C1*[1:0]		Reserved	Reserved
0x5C: QREF_D	PD_*D*	Reserved	BIAS_*D*	STYLE_*D*	A_*D*[1:0]		Reserved	Reserved
0x76	EN_QREF_A0	EN_QREF_A1	EN_QREF_A2	EN_QREF_B0	EN_QREF_B1	EN_QREF_C0	EN_QREF_C1	EN_QCLK_D

a. r = A0, A1, A2, B0, B1, C0, C1, D.

Table 18: QREF_r Output State Register Descriptions[a]

<table>
<tr><th colspan="8">Register Description</th></tr>
<tr><th>Bit Field Name</th><th>Field Type</th><th>Default (Binary)</th><th colspan="5">Description</th></tr>
<tr><td>MUX_r</td><td>R/W</td><td>1

Value:
QREF_r =
SYSREF</td><td colspan="5">0 = QREF_r output signal source is the channel's clock signal
1 = QREF_r output signal source is the centrally generated SYSREF signal</td></tr>
<tr><td rowspan="9">ΦREF_r[2:0]</td><td rowspan="9">R/W</td><td rowspan="9">000

Value: 0ps</td><td colspan="5">SYSREF Phase Delay:

QREF_r delay = ΦREF_r[2:0] · $T_{DCB.}$
Delay values for f_{DCO} = 983.04MHz. Delay values are a function of $T_{DCB.}$</td></tr>
<tr><td rowspan="2">ΦREF_r[2:0]</td><td colspan="4">QREF_r delay in ps for a DLC[1:0] setting of:</td></tr>
<tr><td>00</td><td>01</td><td>10</td><td>11</td></tr>
<tr><td>000</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>001</td><td>131</td><td>262</td><td>393</td><td>524</td></tr>
<tr><td>010</td><td>262</td><td>524</td><td>786</td><td>1048</td></tr>
<tr><td>…</td><td>…</td><td>…</td><td>…</td><td>…</td></tr>
<tr><td>111</td><td>917</td><td>1834</td><td>2751</td><td>3668</td></tr>
<tr><td colspan="5" style="display:none"></td></tr>
<tr><td rowspan="6">BIAS_r</td><td rowspan="6">R/W</td><td rowspan="6">0</td><td colspan="5">QREF_r Output Bias Voltage:
Individual QREF_r output LVDS output bias operation. Not applicable to QREF_r outputs set to LVPECL mode.

0 = Normal operation
1 = Output is biased to the LVDS cross-point voltage if BIAS_TYPE (register 0x19, bit 7) is set to 1. Bit has no effect if BIAS_TYPE = 0.</td></tr>
<tr><td>BIAS_TYPE</td><td>BIAS_r</td><td colspan="3">QREF_r output operation if set to LVDS.</td></tr>
<tr><td>0</td><td>0</td><td colspan="3">QREF_r outputs are initially logic low (QREF_r = L, nQREF_r = H) and will start switching on the first rising edge of the REF input. Use in DC-coupled applications.</td></tr>
<tr><td>0</td><td>1</td><td colspan="3">Disabled with static low/high levels. During a SYSREF event, the output remains at static low levels (QREF_r = L, nQREF_r = H).</td></tr>
<tr><td>1</td><td>0</td><td colspan="3">Both QREF_r and nQREF_r outputs are initially set to the LVDS crosspoint level (VOS) and will start switching on the first rising edge of the REF input. Use in AC-coupled applications.</td></tr>
<tr><td>1</td><td>1</td><td colspan="3">Output is statically set to the LVDS crosspoint voltage. During a SYSREF event, the output remains at the LVDS crosspoint level (VOS).</td></tr>
</table>

Table 18: QREF_r Output State Register Descriptions[a]

<table>
<tr><th colspan="5">Register Description</th></tr>
<tr><th>Bit Field Name</th><th>Field Type</th><th>Default (Binary)</th><th colspan="2">Description</th></tr>
<tr><td rowspan="3">A_*r*[1:0]</td><td rowspan="3">R/W</td><td rowspan="3">01

Value: 750mV</td><td colspan="2">QREF_*r* Output Amplitude</td></tr>
<tr><td>Setting for STYLE = 0 (LVDS)
Termination: 100Ω across</td><td>Setting for STYLE = 1 (LVPECL)
Termination: 50Ω to V_T</td></tr>
<tr><td>A[1:0] = 00: 350mV
A[1:0] = 01: 750mV
A[1:0] = 10: Reserved
A[1:0] = 11: Reserved</td><td>A[1:0] = 00: 350mV
A[1:0] = 01: 750mV
A[1:0] = 10: 1000mV
A[1:0] = 11: 1000mV</td></tr>
<tr><td>PD_*r*</td><td>R/W</td><td>0

Value: Powered up</td><td colspan="2">QREF_*r* Output Power Down:

0 = Output is powered up
1 = Output is powered down. STYLE, EN and A[1:0] settings have no effect</td></tr>
<tr><td>STYLE_*r*</td><td>R/W</td><td>0

Value: LVDS</td><td colspan="2">QREF_x Output Format.

0 = Output is LVDS (requires LVDS 100Ω output termination)
1 = Output is LVPECL (requires LVPECL 50Ω output termination of to the specified recommended termination voltage)</td></tr>
<tr><td>EN_*r*</td><td>R/W</td><td>0

Value: Disabled</td><td colspan="2">QREF_*r* Output Enable:
0 = Output is disabled at the logic low state
1 = Output is enabled</td></tr>
</table>

a. r = A0, A1, A2, B0, B1, C0, C1, D. x = A, B, C, D

SYSREF, DCB, and Phase Alignment Control Registers

Table 19: SYSREF, DCB and Phase Alignment Control Register Bit Field Locations

Bit Field Location								
Register Address	D7	D6	D5	D4	D3	D2	D1	D0
0x18	PD_S	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0x19	BIAS_TYPE	DLC[1:0]		Reserved	Reserved	Reserved	Reserved	M_DCB[8]
0x1A	M_DCB[7:0]							
0x1B	N_ALIGN	P_DCB[6:0]						

Table 20: SYSREF, DCB and Phase Alignment Control Register Descriptions

<table>
<tr><th colspan="6">Register Description</th></tr>
<tr><th>Bit Field Name</th><th>Field Type</th><th>Default (Binary)</th><th colspan="3">Description</th></tr>
<tr><td>PD_S</td><td>R/W</td><td>0

Value: Powered up</td><td colspan="3">SYSREF Global Power-down:

0 = SYSREF functional blocks are powered-up
1 = SYSREF functional blocks are powered-down</td></tr>
<tr><td rowspan="6">BIAS_TYPE</td><td rowspan="6">R/W</td><td rowspan="6">0</td><td colspan="3">SYSREF Output Voltage Bias:
Global to all QREF_*r* outputs bit to control the LVDS output operation. Not applicable to QREF_*r* outputs set to LVPECL mode.</td></tr>
<tr><td>BIAS_TYPE</td><td>BIAS_*r*</td><td>QREF_*r* output operation if set to LVDS.</td></tr>
<tr><td>0</td><td>0</td><td>QREF_*r* outputs are initially logic low (QREF_r = L, nQREF_*r* = H) and will start switching on the first rising edge of the REF input. Use in DC-coupled applications.</td></tr>
<tr><td>0</td><td>1</td><td>Disabled with static low/high levels. During a SYSREF event, the output remains at static low levels (QREF_r = L, nQREF_*r* = H).</td></tr>
<tr><td>1</td><td>0</td><td>Both QREF_*r* and nQREF_*r* outputs are initially set to the LVDS crosspoint level (VOS) and will start switching on the first rising edge of the REF input. Use in AC-coupled applications.</td></tr>
<tr><td>1</td><td>1</td><td>Output is statically set to the LVDS crosspoint voltage. During a SYSREF event, the output remains at the LVDS crosspoint level (VOS).</td></tr>
</table>

Table 20: SYSREF, DCB and Phase Alignment Control Register Descriptions

<table>
<tr><th colspan="5">Register Description</th></tr>
<tr><th>Bit Field Name</th><th>Field Type</th><th>Default (Binary)</th><th colspan="2">Description</th></tr>
<tr><td rowspan="6">DLC[1:0]</td><td rowspan="6">R/W</td><td rowspan="6">00

Value: 131ps</td><td colspan="2">Delay Unit Multiplier:
Effective delay unit for the SYSREF outputs is (1 + DLC[1:0]) ÷ (8 · f_{DCO}).</td></tr>
<tr><td>DLC[1:0]</td><td>Effective SYSREF Delay Unit for f_{DCO} = 983.04MHz</td></tr>
<tr><td>00</td><td>131ps</td></tr>
<tr><td>01</td><td>262ps</td></tr>
<tr><td>10</td><td>393ps</td></tr>
<tr><td>11</td><td>524ps</td></tr>
<tr><td>M_DCB[8:0]</td><td>R/W</td><td>0 0001 0000

Value: 16</td><td colspan="2">Delay Calibration Block (DCB) DCO feedback divider. Set in conjunction with f_{IN} and P_DCB to achieve a DCO frequency of 983.04±20MHz: $f_{DCO} = f_{IN} \div P_{DCB} \cdot M_{DCB}$.</td></tr>
<tr><td>N_ALIGN</td><td>R/W</td><td>0

Value: ÷24</td><td colspan="2">Frequency divider dividing the input clock signal (f_{IN}) to an internal reference for the multi-device phase alignment engine. Use ÷48 if any of the output clock divider is N_*x* = ÷16. The divider setting has an impact on the max. frequency f_{REF} during multi-device phase alignment (see f_{REF} in AC characteristics table).

0 = ÷24.
1 = ÷48</td></tr>
<tr><td>P_DCB[6:0]</td><td>R/W</td><td>000 1000

Value: 8</td><td colspan="2">Delay Calibration Block (DCB) DCO input divider. Set in conjunction with f_{IN} and M_DCB to achieve DCO frequency of 983.04±20MHz: $f_{DCO} = f_{IN} \div P_{DCB} \cdot M_{DCB}$. DCO phase detector frequency should not exceed 200MHz.</td></tr>
</table>

General Control Registers

Table 21: General Control Register Bit Field Locations

Bit Field Location								
Register Address	D7	D6	D5	D4	D3	D2	D1	D0
0x6C	Reserved	DAC_CODE[14:8]						
0x6D	DAC_CODE[7:0]							
0x6E	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	ST_READY	Reserved
0x6F	Reserved	Reserved	PBIAS[5:0]					
0x70	INIT_CLK	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0x71	DCB_CAL	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0x72	PB_CAL	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0x73	MD_ALIGN_Φ	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CPOL

Table 22: General Control Register Descriptions

Register Description			
Bit Field Name	Field Type	Default (Binary)	Description
DAC_CODE[14:0]	R only	X	DAC_CODE is the result of the internal DCB calibration routine. Trigger calibration by setting the DCB_CAL bit.
ST_READY	R only	X	Internal startup routine completion status. The device is ready for operation when this bit is set to 1. 0 = Incomplete 1 = Completed and device is ready for operation.
PBIAS[5:0]	R only	X	BIAS level.
INIT_CLK	W only Auto-Clear	X	Clock divider and phase clock phase delay initialization. Set INIT_CLK = 1 to initialize N_*x* divider and ΦCLK_*x* clock phase delay functions. Required as part of the startup procedure and after each change of a clock divider or clock phase delay value.
PB_CAL	W only Auto-Clear	X	Precision Bias Calibration: Set PB_CAL to 1 starts the auto-calibration of an internal precision bias current source. The bias current is used as reference for outputs configured as LVDS. This bit will auto-clear after the calibration completed. Required to set as part of the startup procedure.
DCB_CAL	W only Auto-Clear	X	DCB Calibration: Setting this bit to 1 will begin the auto-calibration of the DCB. The DCB provides a reference for the SYSREF delay circuits. This bit will auto-clear. This bit should be set as part of the startup procedure. The result of the calibration routine is stored in the DAC_CODE register.
CPOL	R/W	0	SPI Read Operation SCLK Polarity: 0 = Data bits on MISO are output at the falling edge of SCLK edge. 1 = Data bits on MISO are output at the rising edge of SCLK edge.
MD_ALIGN_Φ	R/W Auto-clear	0	Multi-Buffer Phase Alignment Enable 0 = Multi-buffer phase alignment is disabled 1 = Multi-buffer phase alignment is enabled. The next rising edge at the REF input will start the phase alignment.

Electrical Characteristics

Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the 8V79S683 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 23: Absolute Maximum Ratings

Item	Rating
Supply Voltage, V_{DD_V}	3.6V
Inputs	-0.5V to V_{DD_V} + 0.5V
Outputs, V_O (LVCMOS)	-0.5V to V_{DD_V} + 0.5V
Outputs, I_O (LVPECL) Continuous Current Surge Current	 50mA 100mA
Outputs, I_O (LVDS) Continuous Current Surge Current	 50mA 100mA
Input termination current, I_{VT}	±35mA
Junction Temperature, T_J	150°C
Storage Temperature, T_{STG}	-65°C to 150°C
ESD - Human Body Model[a]	2000V
ESD - Charged Device Model[a]	500V

a. According to JEDEC JS-001-2012/JESD22-C101.

Table 24: Recommended Operating Conditions

Item	Rating
Supply Voltage, V_{DD_V}	3.3V
Operating Junction Temperature, T_J[a]	≤125°C
Board Temperature, T_B	≤105°C

a. 125°C/10year lifetime is based on the evaluation of intrinsic wafer process technology reliability metrics. The limiting wafer level reliability factor for this technology with respect to high temperature operation is electro-migration. The device is verified to the maximum operating junction temperature through simulation.

Pin Characteristics

Table 25: Pin Characteristics, V_{DD_V} = 3.3V ± 5%, T_A = -40°C to +105°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			2	4	pF
R_{PD}	Input Pull-Down Resistor	SCLK		51		kΩ
R_{PU}	Input Pull-Up Resistor	nCS		51		kΩ
R_{OUT}	LVCMOS Output Impedance	SDAT (when output)		25		Ω

DC Characteristics

Table 26: Power Supply DC Characteristics, V_{DD_V} = 3.3V ± 5%, T_A = -40°C to +105°C[a]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD_V}	Core Supply Voltage		3.135	3.3	3.465	V
I_{DD} (Total)	Power Supply Current	QCLK_*y* and QREF_*r* set to LVDS, 750mV amplitude, terminated 100Ω, Nx dividers set to ÷1		820	960	mA

a. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

Table 27: Typical Power Supply Current Characteristics, V_{DD_V} = 3.3V, T_A = 25°C[a]

Symbol	Supply Pin Current		Test Case 1	2	3	4	5	6	Unit
	QCLK_*y*	Style	LVPECL	LVPECL	LVDS	LVDS	LVDS	LVDS	
		State	On	On	On	On	On	On	
		Amplitude	350	750	350	350	750	750	mV
	QREF_*r*	Style	LVDS	LVDS	LVDS	LVDS	LVDS	LVDS	
		State	Off	Off	Off	On	On	On	
		Amplitude	–	–	–	350	350	750	mV
I_{DD_SC}	Current through the V_{DD_SPI},V_{DD_CLK} pins		124	124	125	125	125	125	mA
I_{DD_CLKAB}	Current through the V_{DD_QCLKA}, V_{DD_QCLKB} pins		73	84	134	134	187	186	mA
I_{DD_CLKCD}	Current through the V_{DD_QCLKC}, V_{DD_QCLKD} pins		58	65	94	94	126	126	mA

Table 27: Typical Power Supply Current Characteristics, V_{DD_V} = 3.3V, T_A = 25°C[a]

Symbol	Supply Pin Current	Test Case						Unit
		1	2	3	4	5	6	
I_{DD_REFAB}	Current through the V_{DD_REF}, $V_{DD\_QREFA01}$, V_{DD_QREFA2}, V_{DD_QREFB}	37	38	107	230	230	283	mA
I_{DD_REFCD}	Current through the V_{DD_QREFC}, V_{DD_QREFD} pins	4	5	9	83	83	115	mA
P_{TOT}	Total Device Power Consumption	1.15	1.28	1.55	2.20	2.48	2.76	W
$P_{TOT, SYS}$	Total System Power Consumption[b]	1.54	1.75	1.55	2.20	2.48	2.76	W

a. f_{IN} (input) = 491.52MHz, f_{SYSREF} = 7.68MHz. Supply current is independent on the output frequency. QCLK_y outputs terminated according to amplitude settings. QREF_*r* outputs unterminated when SYSREF is turned off.

b. Includes total device power consumption and the power dissipated in external output termination components.

Table 28: LVCMOS DC Characteristics, V_{DD_V} = 3.3V ± 5%, T_A = -40°C to +105°C[a]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	NBC_DEF		2.0		V_{DD_V}	V
V_{IL}	Input Low Voltage	NBC_DEF		-0.3		0.8	V
I_{IH}	Input High Current	NBC_DEF	V_{DD_V} = 3.3V, V_{IN} = 3.3V			5	µA
I_{IL}	Input Low Current	NBC_DEF	V_{DD_V} = 3.3V, V_{IN} = 0V	-150			µA

a. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

Table 29: LVCMOS (JESD8-7A, 1.8V) DC Characteristics, V_{DD_V} = 3.3V ± 5%, T_A = -40°C to +105°C[a] [b]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{T+}	Positive-going input threshold voltage	SCLK, nCS, SDAT		0.660		1.365	V
V_{T-}	Negative-going input threshold voltage	SCLK, nCS, SDAT		0.495		1.170	V
V_H	Hysteresis Voltage	SCLK, nCS, SDAT	$V_{T+} – V_{T-}$	0.165		0.780	V
I_{IH}	Input High Current	SCLK, nCS, SDAT	V_{DD_V} = 3.3V, V_{IN} = 1.8V			150	µA
I_{IL}	Input Low Current	SCLK, nCS, SDAT	V_{DD_V} = 3.465V, V_{IN} = 0V	-150			µA
V_{OH}	Output High Voltage	SDAT (when output)	I_{OH} = -4mA	1.4			V
V_{OL}	Output Low Voltage	SDAT (when output)	I_{OL} = 4mA			0.45	V

a. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

b. Table is valid for the SPI interface pins nCS, SCLK and SDAT. SPI inputs have hysteresis.

Table 30: Differential Input DC Characteristics, V_{DD_V} = 3.3V ± 5%, T_A = -40°C to +105°C[a]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
R_{IN}	Input Resistance	CLK, nCLK REF, nREF		43.5	50	56.5	Ω
R_{IN_DIFF}	Differential Input Resistance	CLK, nCLK REF, nREF		87	100	113	Ω

a. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

Table 31: LVPECL DC Characteristics (QCLK_y, QREF_r, STYLE = 1), V_{DD_V} = 3.3V ± 5%, T_A = -40°C to +105°C[a]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage[b]	Any Amplitude Setting	V_{DD_V} - 1.20	V_{DD_V} - 0.90	V_{DD_V} - 0.60	V
V_{OL}	Output Low Voltage[b]	350mV Amplitude Setting	V_{DD_V} - 1.40	V_{DD_V} - 1.24	V_{DD_V} - 1.05	V
		750mV Amplitude Setting	V_{DD_V} - 1.90	V_{DD_V} - 1.71	V_{DD_V} - 1.60	V
		1000mV Amplitude Setting	V_{DD_V} - 2.20	V_{DD_V} - 1.98	V_{DD_V} - 1.80	V

a. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

b. Outputs terminated with 50Ω to V_T = V_{DD_V} – 1.6V (350mV amplitude setting), V_{DD_V} – 2.0V (750mV amplitude setting), V_{DD_V} – 2.25V (1000mV amplitude setting)

Table 32: LVDS DC Characteristics (QCLK_y, QREF_r, STYLE = 0), V_{DD_V} = 3.3V ± 5%, T_A = -40°C to +105°C[a] [b]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OS}	Offset Voltage[c]	350mV Amplitude Setting	1.20	1.25	1.30	V
		750mV Amplitude Setting	1.25	1.30	1.35	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

a. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

b. Outputs are terminated 100Ω.

c. V_{OS} changes with V_{DD_V}.

AC Characteristics

Table 33: AC Characteristics, V_{DD_V} = 3.3V ± 5%, T_A = -40°C to +105°C[a]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{IN}	Input Frequency[b]	CLK, nCLK	Single device	0	983.04	3000	MHz
			Phase alignment between multiple devices	>0		1000	MHz
f_{REF}	Input Frequency	REF, nREF	SYSREF operation	0		100	MHz
			During multi-device phase alignment[c] N_ALIGN = ÷24 N_ALIGN = ÷48	 >0 >0		 f_{IN} ÷ 48 f_{IN} ÷ 96	 MHz MHz
V_{IN}	Input Voltage Amplitude[d]	CLK, nCLK REF, nREF		0.15		1.2	V
V_{DIFF_IN}	Differential Input Voltage Amplitude[d e]	CLK, nCLK REF, nREF		0.3		2.4	V
V_{CMR}	Common Mode Input Voltage			1.125		V_{DD_V} – (V_{IN} / 2)	V
f_{OUT}	Output Frequency		QCLK_y, QREF_r (Clock), N = ÷1 to ÷24	0	983.04	3000÷N	MHz
			QREF_r (SYSREF)	0		100	MHz
odc	Output Duty Cycle[f]		QCLK_y, QREF_r (Clock), f_{IN} ≤ 2500MHz	45	50	55	%
			QCLK_y, QREF_r (Clock), 2500MHz < f_{IN} ≤ 3000MHz	42	50	58	%
			QREF_r (SYSREF at 7.68MHz)	45	50	55	%
t_R / t_F	Output Rise/Fall Time		QCLK_y, QREF_r (LVPECL), 20% to 80%			250	ps
			QCLK_y, QREF_r (LVDS), 20% to 80%			250	ps
			QREF_r (SYSREF, LVDS), 20% to 80%			250	ps
$V_{O(PP)}$[g]	LVPECL Output Voltage Swing, Peak-to-peak, 491.52MHz		350mV Amplitude Setting	250	350	450	mV
			750mV Amplitude Setting	650	750	850	mV
			1000mV Amplitude Setting	900	1000	1100	mV
	LVPECL Differential Output Voltage Swing, Peak-to-peak, 491.52MHz		350mV Amplitude Setting	500	700	900	mV
			750mV Amplitude Setting	1300	1500	1700	mV
			1000mV Amplitude Setting	1800	2000	2200	mV
$V_{O(PP)}$[h]	LVDS Output Voltage Swing, Peak-to-peak, 491.52MHz		350mV Amplitude Setting	250	350	450	mV
			750mV Amplitude Setting	600	750	900	mV
	LVDS Differential Output Voltage Swing, Peak-to-peak, 491.52MHz		350mV Amplitude Setting	500	700	900	mV
			750mV Amplitude Setting	1200	1500	1800	mV

Table 33: AC Characteristics, V_{DD_V} = 3.3V ± 5%, T_A = -40°C to +105°C[a]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
tsk(o)	Output Skew; NOTE[i j] All delays set to 0	QCLK_y (same N divider)[k]			100	ps
		QCLK_y (any N divider, incident rising edge)			100	ps
		QREF_r (Clock)			100	ps
		QREF_r (SYSREF)			100	ps
		QCLK_y to QREF_r (QREF_r as clock output)[k]			200	ps
tsk(pp)	Part-to-part skew All delays set to 0	CLK to any QCLK_y[k]			375	ps
		REF to any QREF_r			375	ps
t_{PD}	Propagation Delay[k] All delay circuits set to 0	CLK to QCLK_y[k]	250		750	ps
		REF to QREF_r (ΦREF_y = 0)	600	800	1000	ps
Δt_{PD}	Propagation delay variation between the clock input and any QCLK_y output	CLK to QCLK_y[k]	-100		+100	ps
t_S	Setup time[l]	REF to CLK (rising)			250	ps
t_H	Hold time	CLK (rising) to REF			250	ps
	Output isolation between any QCLK_y-QCLK_y and QREF_r-QREF_r outputs	f_{QCLK_y} = 983.04MHz[m]	60			dB
		f_{QCLK_y} = 491.52MHz[m]	65			dB
		f_{QCLK_y} = 245.76MHz[m]	70			dB
	Output isolation between any QREF_r/QCLK_y outputs	f_{QCLK_y} = 983.04MHz, 491.52MHz, 245.76MHz; f_{QREF_r} = 7.68MHz	50			dB

a. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

b. The CLK, nCLK input supports 0Hz if the applied static signal has a minimum amplitude as specified by V_{IN}, V_{DIFF_IN}.

c. Only applicable to a multi-device phase alignment procedure as a max frequency for applying multiple edges to the REF input. This specification is not applicable if a single REF edge is used for multi-device phase alignment.

d. V_{IL} should not be less than -0.3V and V_{IH} should not be greater than V_{DD_V}.

e. Common Mode Input Voltage is defined as the cross-point voltage.

f. Input = 50% duty cycle.

g. LVPECL outputs terminated with 50Ω to V_T = V_{DD_V} – 1.6V (350mV amplitude setting), V_{DD_V} – 2.0V (750mV amplitude setting), V_{DD_V} – 2.25V (1000mV amplitude setting).

h. LVDS outputs terminated 100Ω across Q, nQ.

i. This parameter is defined in accordance with JEDEC standard 65.

j. Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross points

k. All frequency dividers N are in ÷1, ÷2, ÷4 or ÷8; output amplitude setting 750mV.

l. Failure to meet CLK/REF setup and hold time can result in a failure to align output phases across multiple devices

m. Output amplitudes set to 350mV or 750mV.

Table 34: DCB and Phase Delay Characteristics, V_{DD_V} = 3.3V ± 5%, T_A = -40°C to +105°C[a]

Symbol	Parameter	Test Conditions		Minimum	Typical	Maximum	Units
f_{DCO}	DCO Lock Range			963.04	983.04	1003.04	MHz
T_{DCB}	ΦREF_*r* Delay Unit Range	f_{DCO} = 983.04MHz	DLC = 1 (DLC[1:0] = 00)	115	131	150	ps
			DLC = 2 (DLC[1:0] = 01)	230	262	300	ps
			DLC = 3 (DLC[1:0] = 10)	345	393	450	ps
			DLC = 4 (DLC[1:0] = 11)	460	524	600	ps
		f_{DCO} = 963.04MHz (min DCO frequency)	DLC = 1 (DLC[1:0] = 00)	113	134	152	ps
			DLC = 2 (DLC[1:0] = 01)	226	268	304	ps
			DLC = 3 (DLC[1:0] = 10)	339	402	456	ps
			DLC = 4 (DLC[1:0] = 11)	452	536	608	ps
		f_{DCO} = 1003.04MHz (max DCO frequency)	DLC = 1 (DLC[1:0] = 00)	112	128	142	ps
			DLC = 2 (DLC[1:0] = 01)	224	256	284	ps
			DLC = 3 (DLC[1:0] = 10)	336	384	426	ps
			DLC = 4 (DLC[1:0] = 11)	448	512	568	ps
T_{IN}[b]	ΦCLK_*x* Delay Unit	f_{IN} = 983.04MHz			1017		ps
f_1, f_2	DCO Phase Detector Frequency					200	MHz
Δt_D	Delay unit variation	ΦREF_*r* delay unit variation (deviation from nominal, DLC[1:0] = 00)		-30	0	+30	ps
		ΦCLK_*y* delay unit variation (deviation from nominal)		-20	0	+20	ps

a. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

b. ΦCLK_*x* clock channel delay unit is equal to 1 ÷ f_{IN}.

Additive Clock Phase Noise Characteristics

The 8V79S683 is a buffer device, it does not filter the phase noise on the input clock source. Phase noise caused by noise sources within the device can add to the input signal noise, resulting in an increased noise on the outputs (additive phase noise). Phase noise from within the part is not correlated with the noise on the input, therefore the root-sum-square method must be used to calculate the output phase noise: $\Phi_{OUT}^2 = \Phi_{IN}^2 + \Phi_{DEVICE}^2$. As a consequence, at frequency offsets where the input phase noise Φ_{IN} is higher than internal noise sources, the effect of additive phase noise is not measurable.

Simulations of the device phase noise performance are done with an ideal input source, however, simulation models may not account for all possible internal noise sources. Table 35 shows the simulation results for the 8V79S683 buffer with an ideal input source. Table 38 shows output phase noise measured with a low-noise input source, with one column for the measured data and a second column which de-rates the measured data by a factor to model the process variation. Table 38 shows that the input phase noise is the dominating factor in the measured data up to an offset of 100kHz. Above 100kHz, the noise floor of the device dominates the characteristics.

Table 35: Additive Clock Phase Noise Characteristics (Simulation[a]), V_{DD_V} = 3.3V ± 5%[b]

Symbol	Parameter		Test Conditions	25°C	85°C, Worst Case	Units
Φ_N(1k)	QCLK_*y* Phase Noise	245.76MHz	1kHz offset from Carrier	-146.2	-145.5	dBc/Hz
Φ_N(10k)			10kHz offset from Carrier	-156.6	-155.3	dBc/Hz
Φ_N(100k)			100kHz offset from Carrier	-161.9	-159.6	dBc/Hz
Φ_N(1M)			1MHz offset from Carrier	-162.4	-160.5	dBc/Hz
Φ_N(10M)			10MHz offset from Carrier and Noise Floor	-162.4	-160.5	dBc/Hz
Φ_N(1k)		491.52MHz	1kHz offset from Carrier	-141.6	-141.6	dBc/Hz
Φ_N(10k)			10kHz offset from Carrier	-152.7	-151.6	dBc/Hz
Φ_N(100k)			100kHz offset from Carrier	-159.2	-157.0	dBc/Hz
Φ_N(1M)			1MHz offset from Carrier	-159.8	-158.1	dBc/Hz
Φ_N(10M)			10MHz offset from Carrier and Noise Floor	-159.9	-158.2	dBc/Hz
Φ_N(1k)		983.04MHz	1kHz offset from Carrier	-134.5	-132.0	dBc/Hz
Φ_N(10k)			10kHz offset from Carrier	-141.4	-141.8	dBc/Hz
Φ_N(100k)			100kHz offset from Carrier	-155.8	-152.6	dBc/Hz
Φ_N(1M)			1MHz offset from Carrier	-157.2	-155.3	dBc/Hz
Φ_N(10M)			10MHz offset from Carrier and Noise Floor	-157.2	-155.8	dBc/Hz

a. Ideal input signal: rectangular clock signal with a slew rate of 5V/ns and without phase noise.

b. Phase noise and spurious specifications apply for device operation with QREF_*r* outputs inactive (no SYSREF pulses generated). Phase noise specifications are applicable for all outputs active, Nx not equal, process and voltage variations included.

Figure 8: Additive Clock Phase Noise Characteristics (85°C, Worst Case Simulation Model)

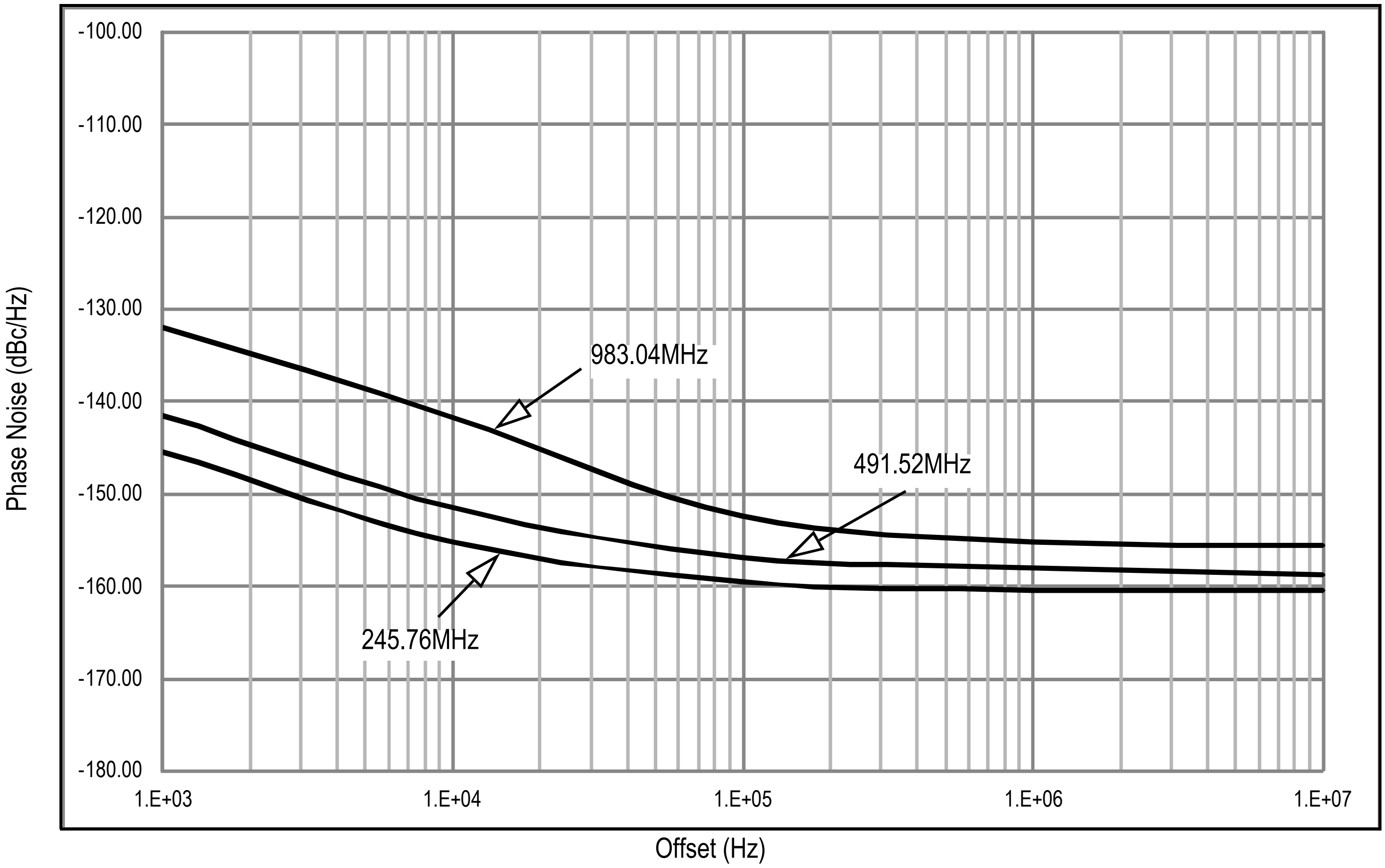


Table 36: Additive Clock Phase Noise Characteristics (Measured), V_{DD_V} = 3.3V ± 5%, T_A = -40°C to +105°C[a] [b]

Symbol	Parameter		Test Conditions	Measured[c]	De-Rated[d]	Units
Φ_N(1k)	QCLK_y Phase Noise	245.76MHz	1kHz offset from Carrier	-141.4	-137.2	dBc/Hz
Φ_N(10k)			10kHz offset from Carrier	-151.7	-149.5	dBc/Hz
Φ_N(100k)			100kHz offset from Carrier	-157.8	-155.5	dBc/Hz
Φ_N(1M)			1MHz offset from Carrier	-158.6	-156.2	dBc/Hz
Φ_N(10M)			10MHz offset from Carrier and Noise Floor	-158.8	-156.3	dBc/Hz
Φ_N(1k)		491.52MHz	1kHz offset from Carrier	-135.3	-128.4	dBc/Hz
Φ_N(10k)			10kHz offset from Carrier	-145.8	-140.5	dBc/Hz
Φ_N(100k)			100kHz offset from Carrier	-154.2	-149.5	dBc/Hz
Φ_N(1M)			1MHz offset from Carrier	-157.2	-155.4	dBc/Hz
Φ_N(10M)			10MHz offset from Carrier and Noise Floor	-157.6	-156.3	dBc/Hz
Φ_N(1k)		983.04MHz	1kHz offset from Carrier	-131.3	-125.7	dBc/Hz
Φ_N(10k)			10kHz offset from Carrier	-141.2	-138.5	dBc/Hz
Φ_N(100k)			100kHz offset from Carrier	-149.6	-146.5	dBc/Hz
Φ_N(1M)			1MHz offset from Carrier	-154.5	-152.2	dBc/Hz
Φ_N(10M)			10MHz offset from Carrier and Noise Floor	-155.3	-152.5	dBc/Hz
tjit(Ø)	Clock RMS Phase Jitter (Random)		Integration Range: 1kHz - 61.44MHz		100	fs
			Integration Range: 12kHz - 20MHz		100	fs

a. Phase noise and spurious specifications apply for device operation with QREF_*r* outputs inactive (no SYSREF pulses generated). Phase noise specifications are applicable for all outputs active, Nx not equal.

b. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

c. Measured results at the max. temperature of 85°C using an input source with a phase noise characteristics of:
- 245.76MHz: -143.7dBc/Hz (1kHz offset), -152.5dBc/Hz (10kHz), -160.8dBc/Hz (100kHz), -172.6dBc/Hz (1MHz), -179.5dBc/Hz (10MHz).
- 491.52MHz: -137.7dBc/Hz (1kHz offset), -147.4dBc/Hz (10kHz), -156.1dBc/Hz (100kHz), -167.6dBc/Hz (1MHz), -170.1dBc/Hz (10MHz).
- 983.04MHz: -132.5dBc/Hz (1kHz offset), -141.4dBc/Hz (10kHz), -149.9dBc/Hz (100kHz), -161.4dBc/Hz (1MHz), -164.2dBc/Hz (10MHz).

d. De-rating factor applied to the characterized data at 85°C to account for worst-case process variation.

Figure 9: Additive Clock Phase Noise Characteristics (Measured), f_{OUT} = 245.76MHz

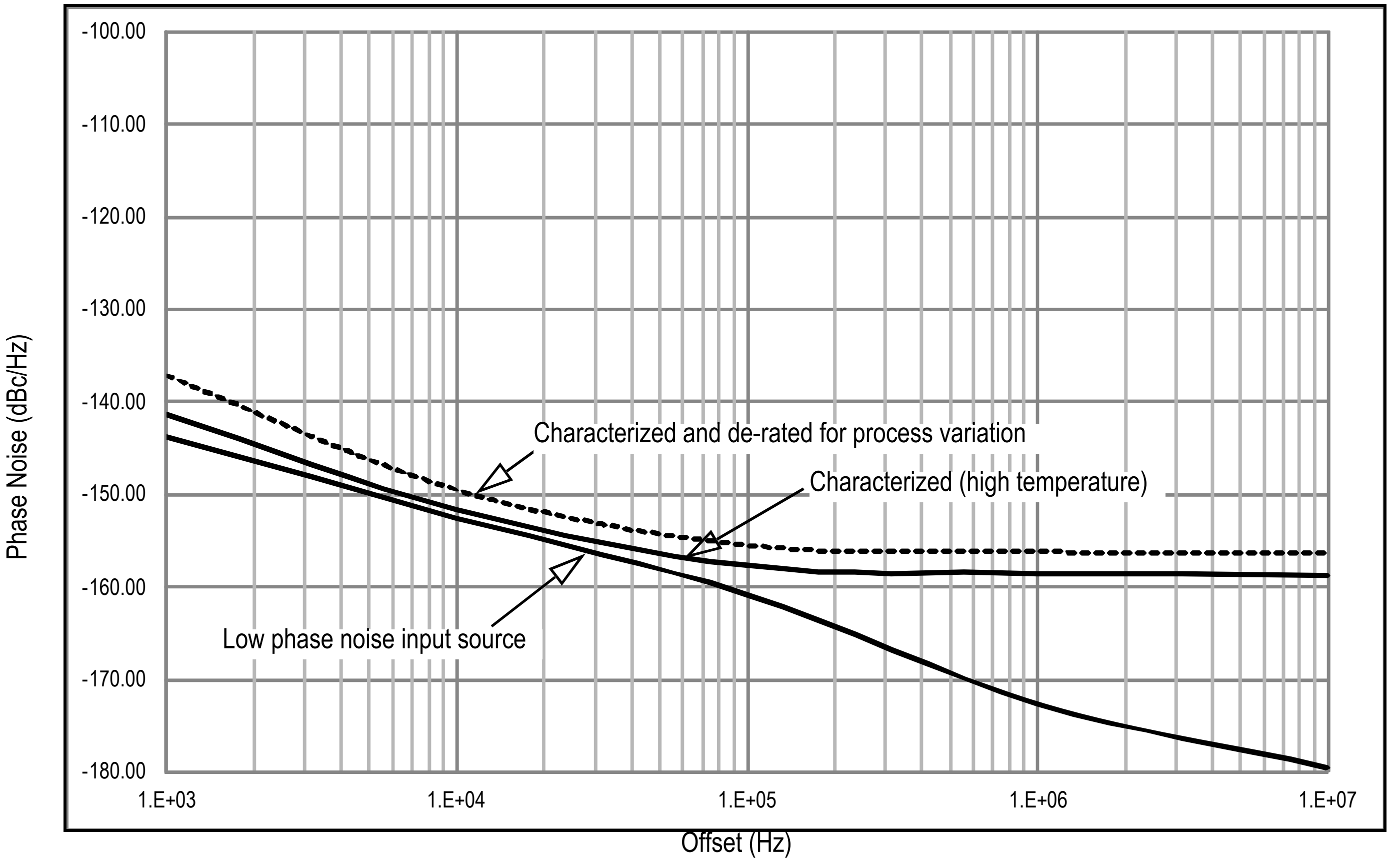


Figure 10: Additive Clock Phase Noise Characteristics (Measured), f_{OUT} = 491.52MHz

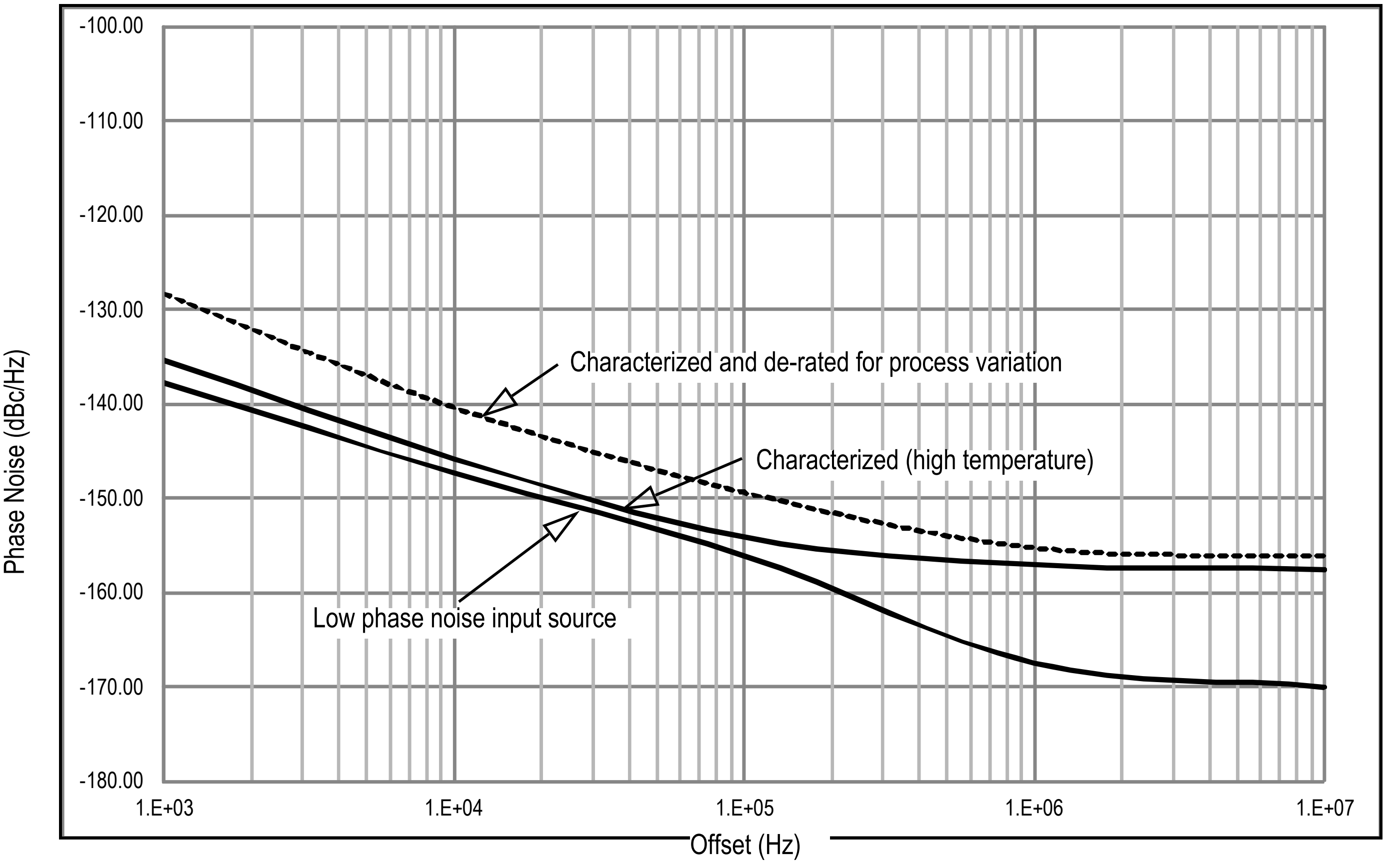
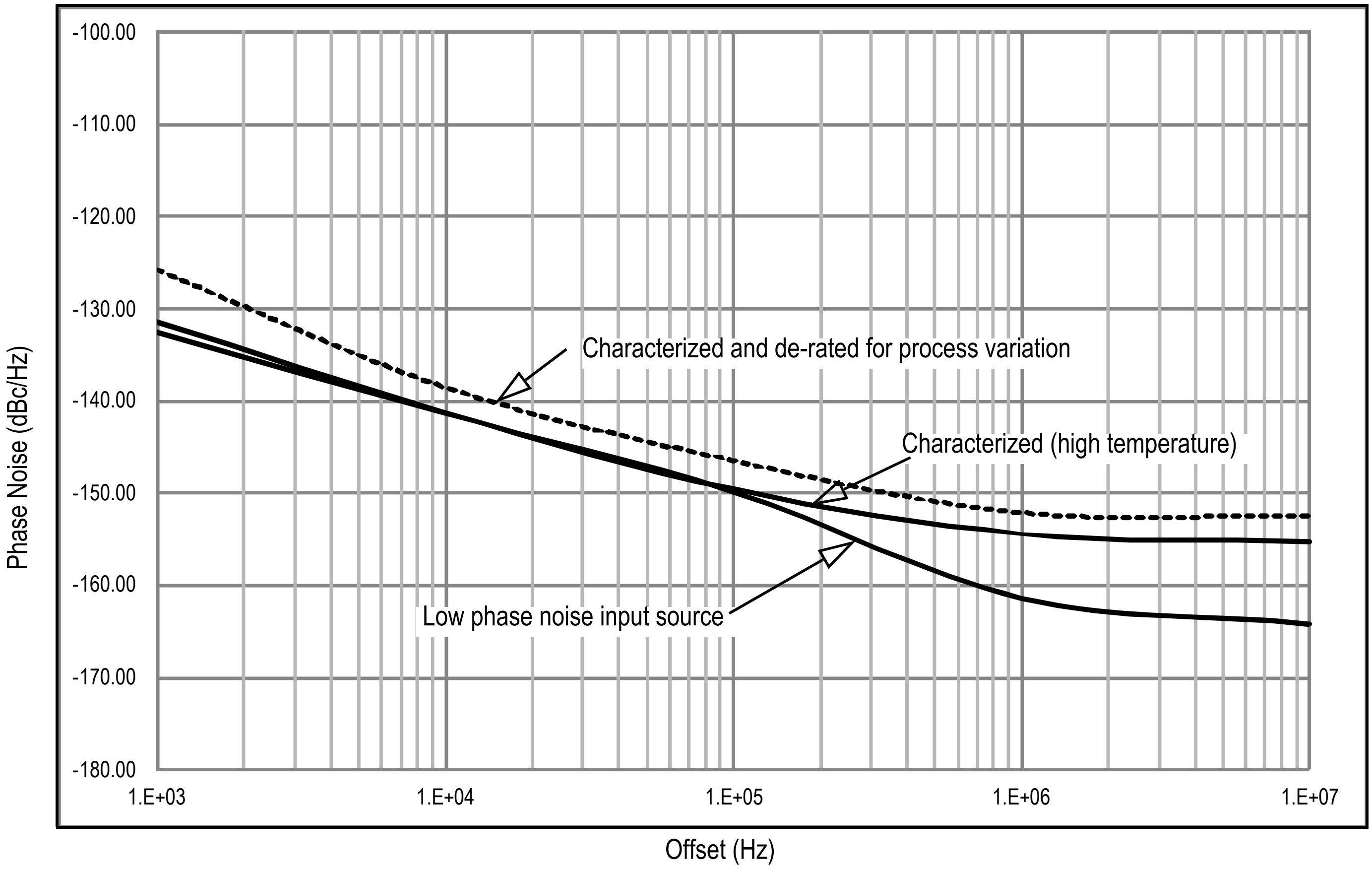


Figure 11: Additive Clock Phase Noise Characteristics (Measured), f_{OUT} = 983.04MHz



Symbol	Parameter		Test Conditions	Typical	Units
Φ_N(1k)	QREF_*r* Phase Noise	15.36MHz[a]	1kHz offset from Carrier	-146	dBc/Hz
Φ_N(10k)			10kHz offset from Carrier	-152.5	dBc/Hz
Φ_N(100k)			100kHz offset from Carrier	-156	dBc/Hz
Φ_N(1M)			1MHz offset from Carrier	-156	dBc/Hz
Φ_N(1k)		30.72MHz[c]	1kHz offset from Carrier	-147.5	dBc/Hz
Φ_N(10k)			10kHz offset from Carrier	-153.5	dBc/Hz
Φ_N(100k)			100kHz offset from Carrier	-155.5	dBc/Hz
Φ_N(1M)			1MHz offset from Carrier	-155.5	dBc/Hz

a. Measured results with DLC[1:0] = 00 and ΦREF_r = 3.

Application Information

Input Interface Circuits

Figure 12: LVDS Output Drives 8V79S683 Input with Integrated Termination Resistor (DC-Coupled)

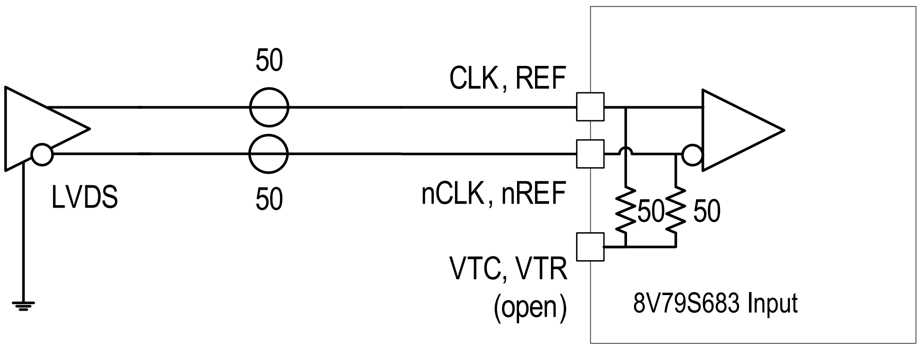


Figure 13: LVPECL Output Drives 8V79S683 Input with Integrated Termination Resistor (DC-Coupled)

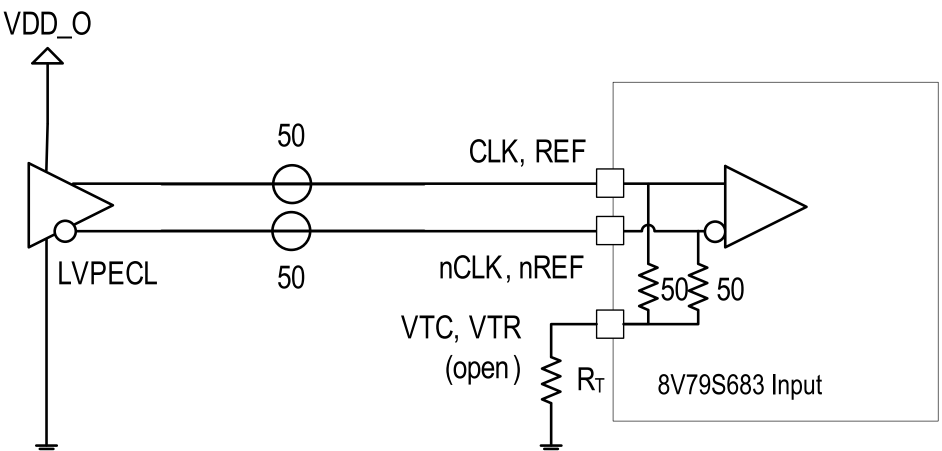


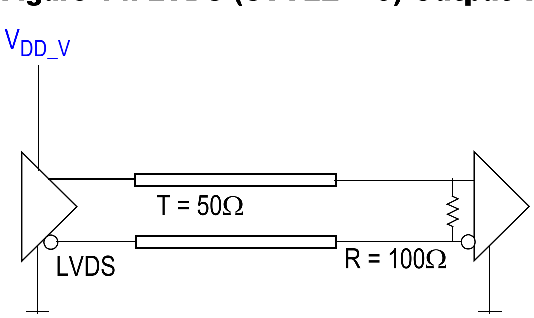
Table 37: Termination Resistors

	V_{DD_O} = 2.5V	V_{DD_O} = 3.3V
R_T	18Ω	50Ω

Termination for QCLK_y, QREF_r LVDS Outputs (STYLE = 0)

Figure 14 shows an example termination for the QCLK_*y*, QREF_*r* LVDS outputs. In this example, the characteristic transmission line impedance is 50Ω. The termination resistor R (100Ω) is matched to the line impedance. The termination resistor must be placed at the line end. No external termination resistor is required if R is an internal part of the receiver circuit. The LVDS termination in Figure 14 is applicable for any output amplitude setting specified in Table 9.

Figure 14: LVDS (STYLE = 0) Output Termination



AC Termination for QCLK_y, QREF_r LVDS Outputs (STYLE = 0)

Figure 15 and Figure 16 show example AC terminations for the QCLK_*y*, QREF_*r* LVDS outputs. In the examples, the characteristic transmission line impedance is 50Ω. In Figure 15, the termination resistor R (100Ω) is placed at the line end. No external termination resistor is required if R is an internal part of the receiver circuit, which is shown in Figure 16. The LVDS terminations in both Figure 15 and Figure 16 are applicable for any output amplitude setting specified in Table 9. The receiver input should be re-biased according to its common mode range specifications.

Figure 15: LVDS (STYLE = 0) AC Output Termination

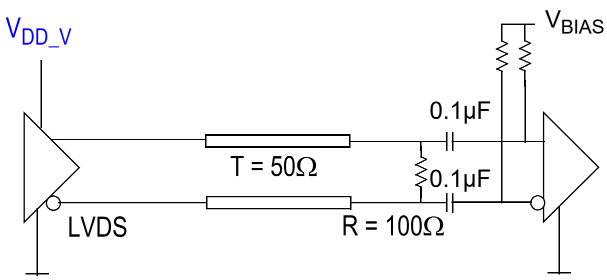
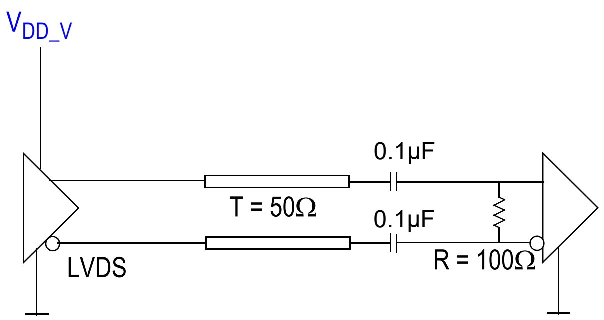


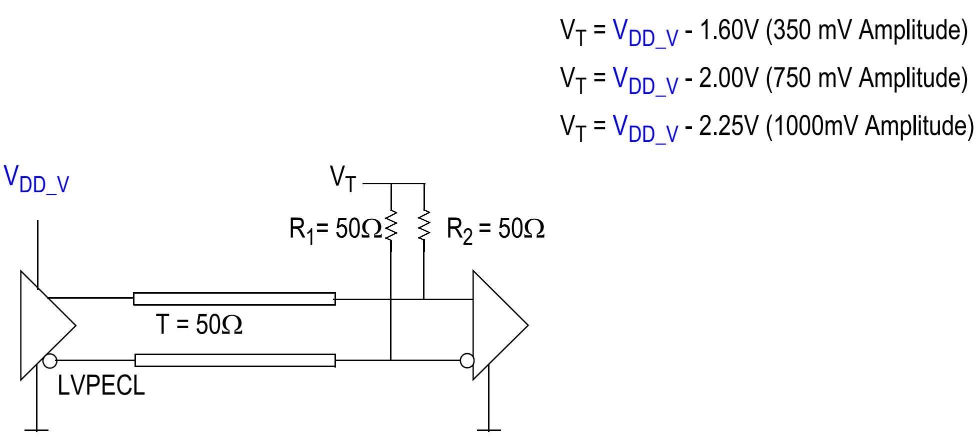
Figure 16: LVDS (STYLE = 0) AC Output Termination



Termination for QCLK_y, QREF_r LVPECL Outputs (STYLE = 1)

Figure 17 shows an example termination for the QCLK_*y*, QREF_*r* LVPECL outputs. In this example, the characteristic transmission line impedance is 50Ω. The R1 (50Ω) and R2 (50Ω) resistors are matched load terminations. The output is terminated to the termination voltage V_T. The V_T must be set according to the output amplitude setting defined in Table 9. The termination resistors must be placed close at the line end.

Figure 17: LVPECL (STYLE = 1) Output Termination

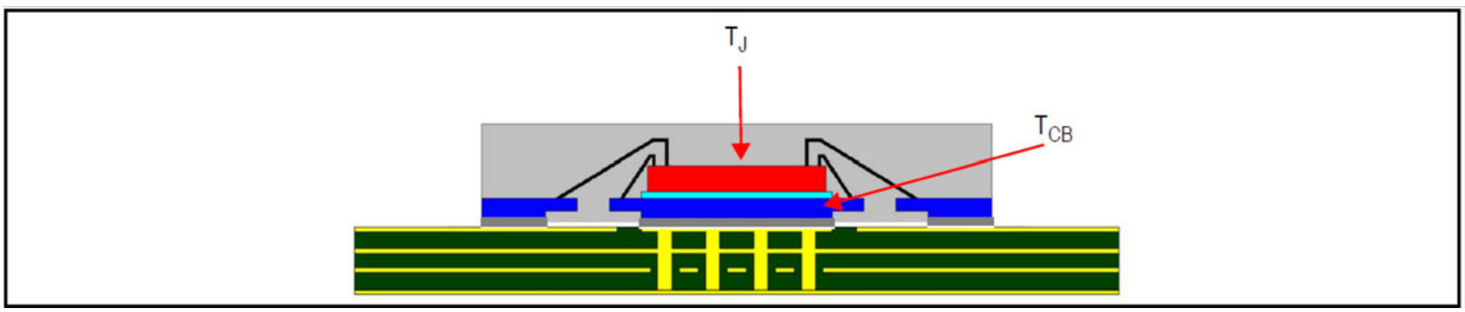


Package Exposed Pad Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in Figure 18. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/Electrically Enhance Lead-frame Base Package, Amkor Technology.

Figure 18: Assembly for Exposed Pad Thermal Release Path - Side View (drawing not to scale)



Thermal Characteristics

Table 38: Thermal Resistance for 64-VFQFPN Package[a]

Symbol	Thermal Parameter	Condition	Value	Unit
Θ_{JA}	Junction to ambient	0 m/s air flow	22.76	°C/W
		1 m/s air flow	19.25	°C/W
		2 m/s air flow	17.70	°C/W
		3 m/s air flow	16.87	°C/W
		4 m/s air flow	16.37	°C/W
		5 m/s air flow	16.03	°C/W
Θ_{JC}	Junction to case		14.33	°C/W
Θ_{JB}	Junction to board		1.1	°C/W

a. Standard JEDEC 2S2P multilayer PCB.

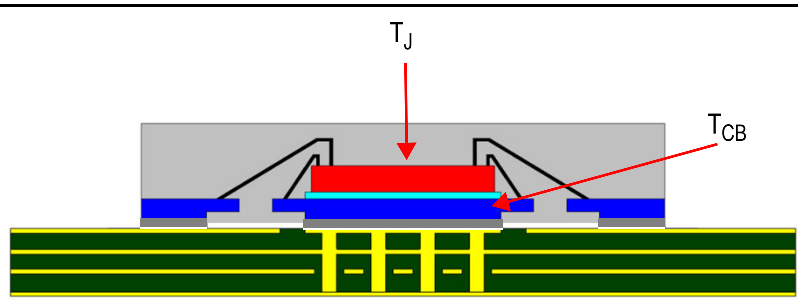
Case Temperature Considerations

This device supports applications in a natural convection environment which does not have any thermal conductivity through ambient air. The printed circuit board (PCB) is typically in a sealed enclosure without any natural or forced air flow and is kept at or below a specific temperature. The device package design incorporates an exposed pad (ePad) with enhanced thermal parameters which is soldered to the PCB where most of the heat escapes from the bottom exposed pad. For this type of application, it is recommended to use the junction-to-board thermal characterization parameter Ψ_{JB} (Psi-JB) to calculate the junction temperature (T_J) and ensure it does not exceed the maximum allowed operating junction temperature in the Absolute Maximum Rating table.

The junction-to-board thermal characterization parameter, $\Psi_{JB,}$ is calculated using the following equation:

$T_J = T_{CB} + \Psi_{JB} \times P_{D,}$ where:

- T_J = Junction temperature at steady state condition in (^oC)
- T_{CB} = Case temperature (Bottom) at steady state condition in (^oC)
- Ψ_{JB} = Thermal characterization parameter to report the difference between junction temperature and the temperature of the board measured at the top surface of the board
- P_D = power dissipation (W) in desired operating configuration



The ePad provides a low thermal resistance path for heat transfer to the PCB and represents the key pathway to transfer heat away from the IC to the PCB. It's critical that the connection of the exposed pad to the PCB is properly constructed to maintain the desired IC case temperature (T_{CB}). A good connection ensures that temperature at the exposed pad (T_{CB}) and the board temperature (T_B) are relatively the same. An improper connection can lead to increased junction temperature, increased power consumption and decreased electrical performance. In addition, there could be long-term reliability issues and increased failure rate.

Example Calculation for Junction Temperature (T_J): $T_J = T_{CB} + \Psi_{JB} \times P_D$

Table 39: Thermal Resistance for 64-VFQFPN package[a]

Package type	64-VFQFPN
Body size (mm)	9 × 9 × 0.85 mm
ePad size (mm)	6.00 × 6.00 mm
Thermal Via	8 × 8 Matrix
Ψ_{JB}	1.1 C/W
T_{CB}	105°C
P_D	2.76W[b]

a. Standard JEDEC 2S2P multilayer PCB.

b. See Table 27, test case 6.

For the variables above, the junction temperature is $T_J = T_{CB} + \Psi_{JB} \times P_D$ = 105°C + 1.1°C/W × 2.76W = 108°C. Since this operating junction temperature is below the maximum operating junction temperature of 125°C, there are no long term reliability concerns. In addition, since the junction temperature at which the device was characterized using forced convection is 108.6°C, this device can function without the degradation of the specified AC or DC parameters.

Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

www.idt.com/document/psc/64-vfqfpn-package-outline-drawing-90-x-90-x-09-mm-body-05mm-pitch-epad-60-x-60-mm-nlg64p5

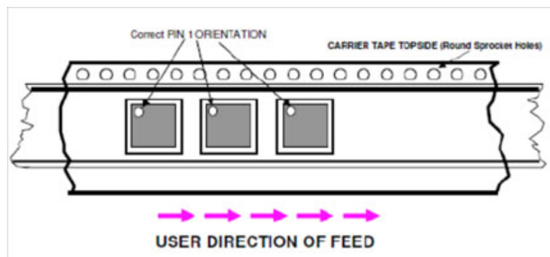
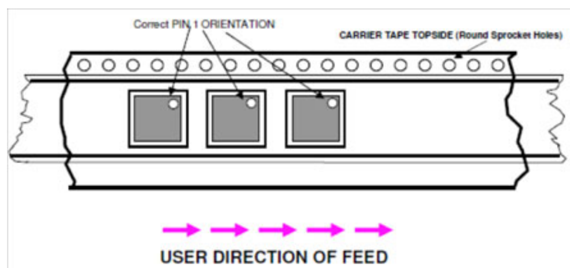
Marking Diagram

- Line 1 indicates the manufacturer.
- Line 2 indicates the part number.
- Line 3 indicates the following:
  - "#" denotes stepping.
  - "YY" is the last two digits of the year; "WW" is the work week number when the part was assembled.

Ordering Information

Orderable Part Number	Package	MSL Rating	Shipping Packaging	Temperature
8V79S683NLGI	RoHS 6/6 64-VFQFPN	3	Tray	-40°C to +85°C
8V79S683NLGI8		3	Tape and Reel, Pin 1 Orientation: EIA-481-C	
8V79S683NLGI/W		3	Tape and Reel, Pin 1 Orientation: EIA-481-D/E	

Table 40: Pin 1 Orientation in Tape and Reel Packaging

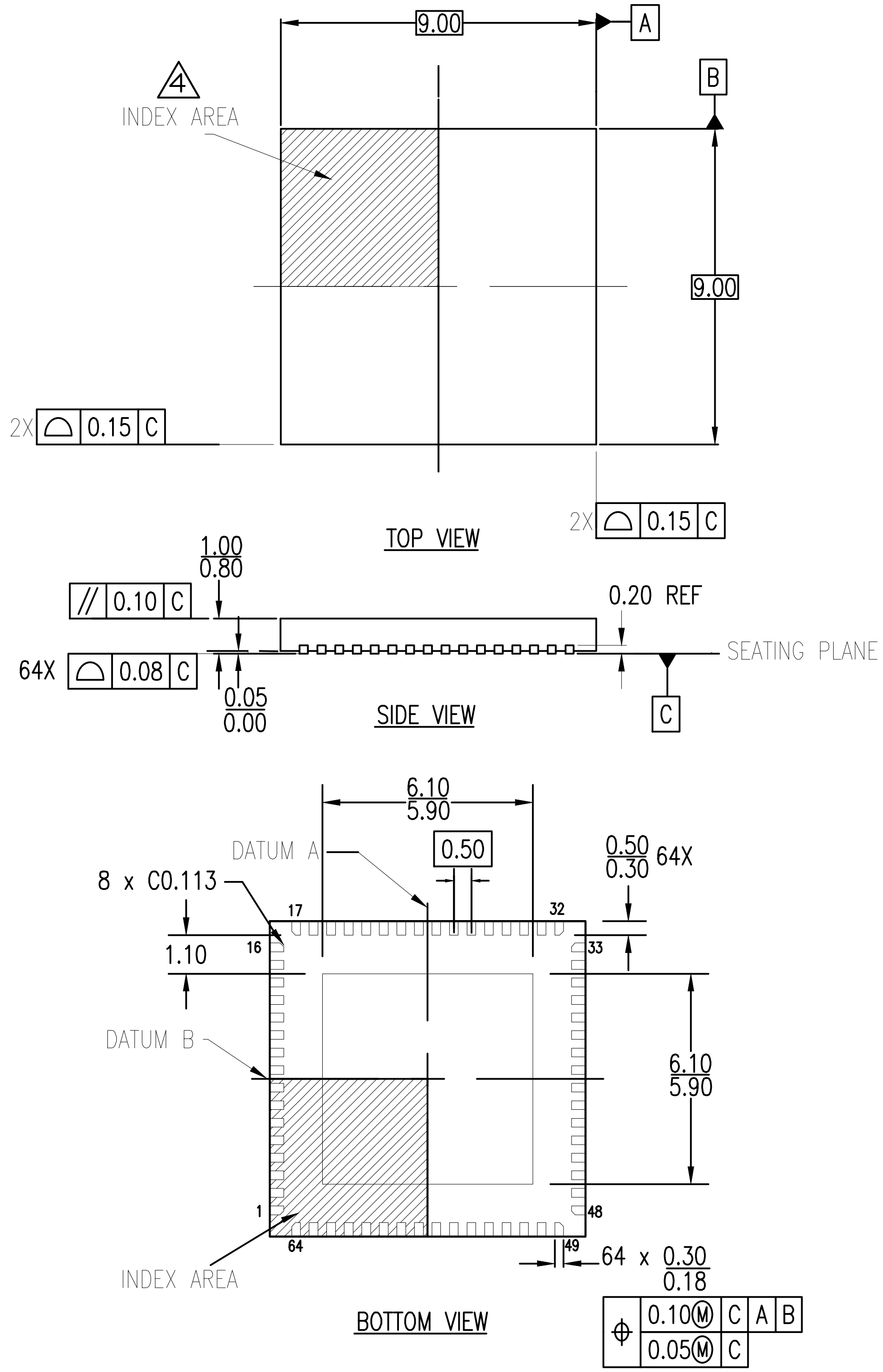
Part Number Suffix	Pin 1 Orientation	Illustration
8	Quadrant 1 (EIA-481-C)	
/W	Quadrant 2 (EIA-481-D/E)	

Glossary

Abbreviation	Description
Index *x*	Denominates a channel, channel frequency divider and the associated configuration bits. Range: A, B, C, D.
Index y	Denominates a QCLK output and associated configuration bits. Range: A0, A1, A2, B0, B1, C0, C1, D.
Index *r*	Denominates a QREF output and associated configuration bits. Range: A0, A1, A2, B0, B1, C0, C1, D.
V_{DD_V}	Denominates voltage supply pins. Range: V_{DD_QCLKA}, $V_{DD\_QREFA01}$, V_{DD_QREFA2}, V_{DD_QCLKB}, V_{DD_QREFB}, V_{DD_QCLKC}, V_{DD_QREFC}, V_{DD_QCLKD}, V_{DD_QREFD}, V_{DD_CLK}, V_{DD_REF}.
[...]	Index brackets describe a group associated with a logical function or a bank of outputs.
{...}	List of discrete values.

Revision History

Date	Description of Change
July 18, 2019	Initial release.



NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. (4) PIN1 INDEX ID IS INDICATED WITH EITHER EXPOSED PAD CORNER CHAMFER OR HALF CIRCLED CUT NEAR THE EXPOSED PAD CORNER.

64-VFQFPN, Package Outline Drawing

9.0 x 9.0 x 0.9 mm Body, 0.5mm Pitch, Epad 6.0 x 6.0 mm

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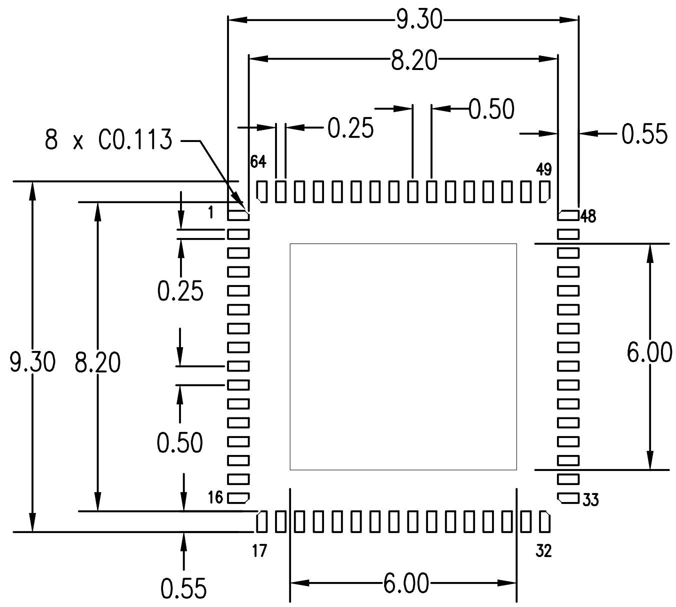

RECOMMENDED LAND PATTERN

NOTES:
1. ALL DIMENSIONS ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW AS VIEWED ON PCB.
3. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
4. LAND PATTERN RECOMMENDATION PER IPC–7351 LP CALCULATOR.

Package Revision History		
Date Created	Rev No.	Description
Feb 16, 2018	Rev 03	New Format
April 19, 2018	Rev 04	Add Chamfer on Corner Leads

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/