

## Automotive fully integrated H-bridge motor driver

Datasheet - preliminary data



### Features

| Type        | $R_{DS(on)}$            | $I_{out}$ | $V_{CCmax}$ |
|-------------|-------------------------|-----------|-------------|
| VNH7100AS-E | 100 mΩ typ<br>(per leg) | 12 A      | 41 V        |

- Automotive qualified
- Output current: 15 A
- 3 V CMOS-compatible inputs
- Undervoltage shutdown
- Overvoltage clamp
- Thermal shutdown
- Cross-conduction protection
- Current and power limitation
- Very low standby power consumption
- Protection against loss of ground and loss of  $V_{CC}$
- PWM operation up to 20 KHz
- Multisense diagnostic functions
  - Analog motor current feedback
  - Output short to ground detection
  - Thermal shutdown indication
  - OFF-state open-load detection
  - Output short to  $V_{CC}$  detection
- Output protected against short to ground and short to  $V_{CC}$
- Standby Mode
- Half Bridge Operation
- Package: ECOPACK®

### Description

The VNH7100AS-E is a full bridge motor driver intended for a wide range of automotive applications. The device incorporates a dual monolithic high-side driver and two low-side switches.

Both switches are designed using STMicroelectronics' well known and proven proprietary VIPower® M0 technology that allows to efficiently integrate on the same die a true Power MOSFET with an intelligent signal/protection circuitry. The three dies are assembled in SO-16N package on electrically isolated leadframes.

Moreover, its fully symmetrical mechanical design allows superior manufacturability at board level. The input signals  $IN_A$  and  $IN_B$  can directly interface to the microcontroller to select the motor direction and the brake condition. A SEL0 pin is available to address to the microcontroller the information available on the Multisense. The Multisense pin allows to monitor the motor current by delivering a current proportional to the motor current value. The normal operating condition is explained in the truth table.

The PWM, up to 20 KHz, allows to control the speed of the motor in all possible conditions. In all cases, a low level state on the PWM pin turns off both the  $LS_A$  and  $LS_B$  switches.

**Table 1. Device summary**

| Package | Order codes |               |
|---------|-------------|---------------|
|         | Tube        | Tape and reel |
| SO-16N  | VNH7100AS-E | VNH7100ASTR-E |

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# 1 Block diagram and pin description

Figure 1. Block diagram

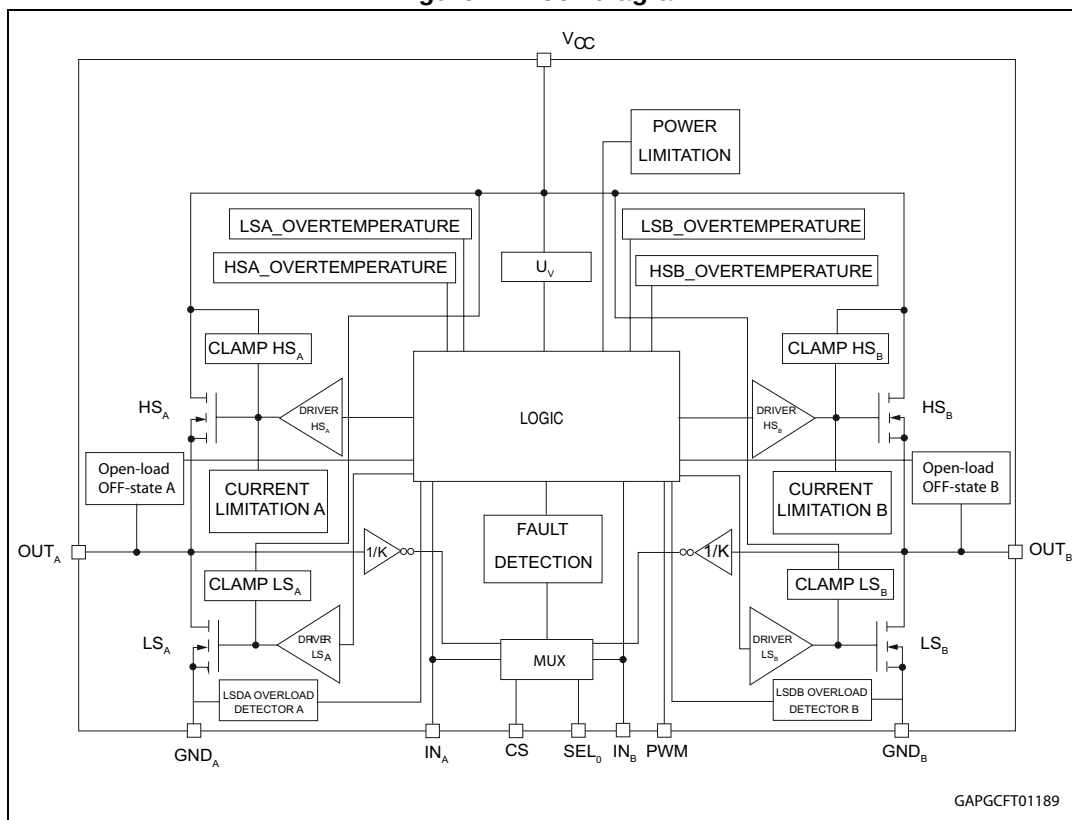


Table 2. Block description

| Name                                              | Description                                                                                                                                               |
|---------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|
| Logic control                                     | Allows the turn-on and the turn-off of the high-side and the low-side switches according to the truth table.                                              |
| Undervoltage                                      | Shuts down the device for battery voltage lower than 4 V.                                                                                                 |
| High-side and low-side clamp voltage              | Protect the high-side and the low-side switches from the high voltage on the battery line.                                                                |
| High-side and low-side driver                     | Drive the gate of the concerned switch to allow a proper $R_{on}$ for the leg of the bridge.                                                              |
| Current limitation                                | Limits the motor current in case of short circuit.                                                                                                        |
| High-side and low-side overtemperature protection | In case of short-circuit with the increase of the junction temperature, it shuts down the concerned driver to prevent degradation and to protect the die. |
| Low-side overload detector                        | Detects when low side current exceeds shutdown current and latches off the concerned Low side.                                                            |

Table 2. Block description (continued)

| Name             | Description                                                                                                  |
|------------------|--------------------------------------------------------------------------------------------------------------|
| Fault detection  | Signalizes the abnormal behavior of the switch through Multisense pin.                                       |
| Power limitation | Limits the power dissipation of the high-side driver inside safe range in case of short to ground condition. |

Figure 2. Configuration diagram (top view)

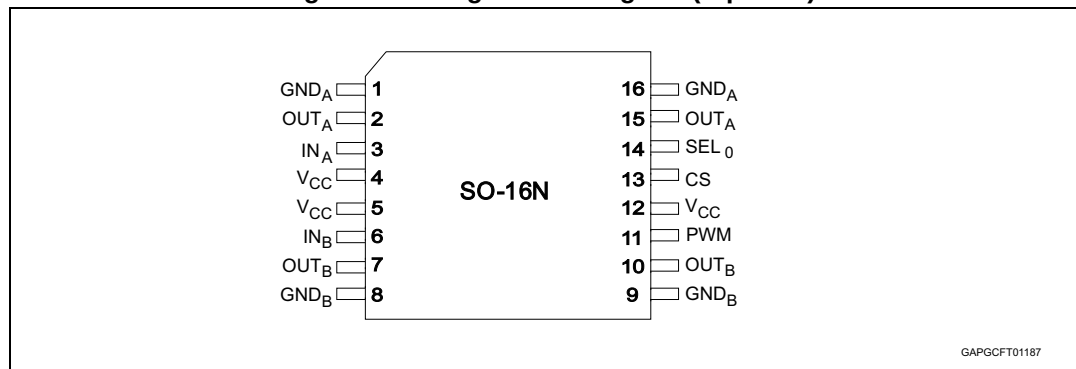
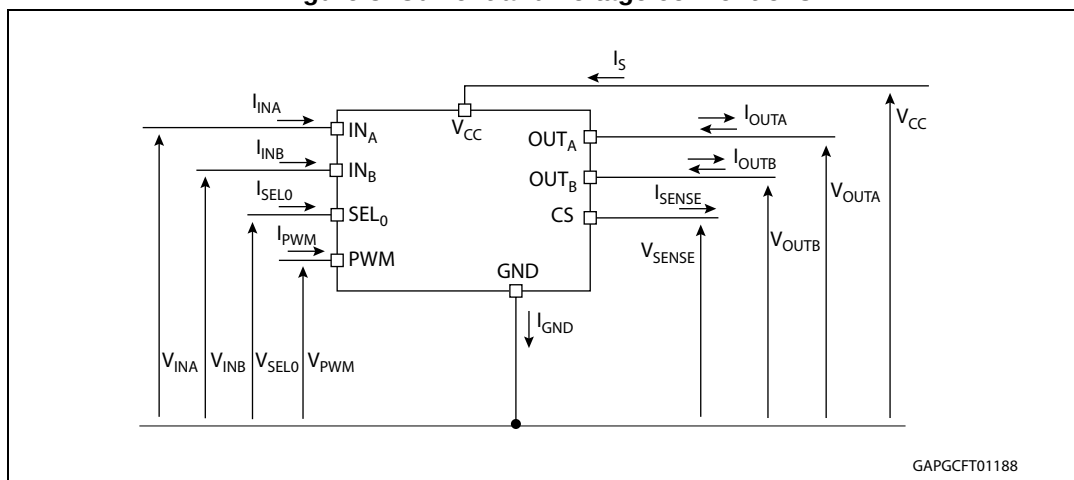


Table 3. Pin definitions and functions

| Pin N°   | Symbol           | Function                                                                                                                                                                                      |
|----------|------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1, 16    | GND <sub>A</sub> | Source of low-side switch A                                                                                                                                                                   |
| 2, 15    | OUT <sub>A</sub> | Source of high-side switch A / drain of low-side switch A                                                                                                                                     |
| 3        | IN <sub>A</sub>  | Clockwise input                                                                                                                                                                               |
| 4, 5, 12 | V <sub>CC</sub>  | Power supply voltage                                                                                                                                                                          |
| 6        | IN <sub>B</sub>  | Counter clockwise input                                                                                                                                                                       |
| 7, 10    | OUT <sub>B</sub> | Source of high-side switch B / drain of low-side switch B                                                                                                                                     |
| 8, 9     | GND <sub>B</sub> | Source of low-side switch B                                                                                                                                                                   |
| 11       | PWM              | Voltage controlled input pin with hysteresis, CMOS compatible. Gates of low-side FETS get modulated by the PWM signal during their on phase allowing speed control of the motor. Active high. |
| 13       | CS               | Multiplexed analog sense output pin; it delivers a current proportional to the motor current.                                                                                                 |
| 14       | SEL <sub>0</sub> | Active high compatible with 3 V and 5 V CMOS outputs pin; in combination with IN <sub>A</sub> , IN <sub>B</sub> , it addresses the Multisense information delivered to the micro.             |

## 2 Electrical specifications

Figure 3. Current and voltage conventions



### 2.1 Absolute maximum ratings

Stressing the device above the rating listed in [Table 4: Absolute maximum ratings](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Table 4. Absolute maximum ratings

| Symbol      | Parameter                                                                                     | Value              | Unit |
|-------------|-----------------------------------------------------------------------------------------------|--------------------|------|
| $V_{CC}$    | Supply voltage                                                                                | 38                 | V    |
| $-V_{CC}$   | Reverse DC Supply Voltage                                                                     | 0.3                | V    |
| $I_{max}$   | Maximum output current (continuous)                                                           | Internally limited | A    |
| $I_R$       | Reverse output current (continuous)                                                           | TBD                | A    |
| $V_{CCPK}$  | Maximum transient supply voltage (ISO 16750-2:2010 Test B clamped to 40 V; $R_L = 4 \Omega$ ) | 40                 | V    |
| $V_{CCJS}$  | Maximum jump start voltage for single pulse short circuit protection                          | 28                 | V    |
| $I_{IN}$    | Input current ( $IN_A$ and $IN_B$ pins)                                                       | -1 to 10           | mA   |
| $I_{SELO}$  | $SEL_0$ DC input current                                                                      | -1 to 10           | mA   |
| $I_{PWM}$   | PWM input current                                                                             | -1 to 10           | mA   |
| $-I_{GND}$  | DC reverse ground pin current                                                                 | 200                | mA   |
| $I_{SENSE}$ | CS pin DC output current ( $V_{GND} = V_{CC}$ and $V_{SENSE} < 0$ V)                          | 10                 | mA   |
|             | CS pin DC output current in reverse ( $V_{CC} < 0$ V)                                         | -20                |      |

Table 4. Absolute maximum ratings (continued)

| Symbol           | Parameter                                                            | Value      | Unit |
|------------------|----------------------------------------------------------------------|------------|------|
| V <sub>ESD</sub> | Electrostatic discharge<br>(Human body model: R = 1.5 kΩ C = 100 pF) |            |      |
|                  | – IN <sub>A</sub> , IN <sub>B</sub> , PWM                            | 2          | kV   |
|                  | – SEL <sub>0</sub>                                                   | 2          |      |
|                  | – CS                                                                 | 2          |      |
|                  | – V <sub>CC</sub>                                                    | 4          |      |
|                  | – Output                                                             | 4          |      |
| V <sub>ESD</sub> | Charge device model (CDM-AEC-Q100-011)                               | 750        | V    |
| T <sub>c</sub>   | Junction operating temperature                                       | -40 to 150 | °C   |
| T <sub>STG</sub> | Storage temperature                                                  | -55 to 150 | °C   |

## 2.2 Thermal data

Table 5. Thermal data

| Symbol               | Parameter                                                                   | Max. value | Unit |
|----------------------|-----------------------------------------------------------------------------|------------|------|
| R <sub>thj-pin</sub> | Thermal resistance junction-case (per leg) (JEDEC JESD 51-5) <sup>(1)</sup> | TBD        | °C/W |
| R <sub>thj-amb</sub> | Thermal resistance junction-ambient (JEDEC JESD 51-5) <sup>(2)</sup>        | TBD        | °C/W |
| R <sub>thj-amb</sub> | Thermal resistance junction-ambient (JEDEC JESD 51-7) <sup>(1)</sup>        | TBD        | °C/W |

1. Device mounted on four-layers 2s2p PCB.

2. Device mounted on two-layers 2s0p PCB with 2 cm<sup>2</sup> heatsink copper trace.



## 2.3 Electrical characteristics

Values specified in this section are for  $V_{CC} = 7\text{ V}$  up to  $28\text{ V}$ ;  $-40^\circ\text{C} < T_j < 150^\circ\text{C}$ , unless otherwise specified.

**Table 6. Power section**

| Symbol              | Parameter                                             | Test conditions                                                                                                                   | Min. | Typ. | Max. | Unit          |
|---------------------|-------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------|------|------|------|---------------|
| $V_{CC}$            | Operating supply voltage                              |                                                                                                                                   | 4    |      | 28   | V             |
| $I_S$               | Supply current                                        | Off-state (standby)<br>$I_{N_A} = I_{N_B} = 0$ ; $SEL_0 = 0$ ;<br>$PWM = 0$ ; $T_j = 25^\circ\text{C}$ ; $V_{CC} = 13\text{ V}$ ; |      |      | 1    | $\mu\text{A}$ |
|                     |                                                       | Off-state (standby)<br>$I_{N_A} = I_{N_B} = 0$ ; $SEL_0 = 0$ ;<br>$PWM = 0$ ; $V_{CC} = 13\text{ V}$ ; $T_j = 85^\circ\text{C}$   |      |      | 1    | $\mu\text{A}$ |
|                     |                                                       | Off-state (standby)<br>$I_{N_A} = I_{N_B} = 0$ ; $SEL_0 = 0$ ;<br>$PWM = 0$ ; $V_{CC} = 13\text{ V}$ ; $T_j = 125^\circ\text{C}$  |      |      | 3    | $\mu\text{A}$ |
|                     |                                                       | Off-state (no standby)<br>$I_{N_A} = I_{N_B} = 0$ ; $SEL_0 = 5\text{ V}$ ;<br>$PWM = 0$                                           |      | 2    | 4    | mA            |
|                     |                                                       | On-state: $I_{N_A}$ or $I_{N_B} = 5\text{ V}$ ;<br>$PWM = 0$ or $PWM = 5$ ; $SEL_0 = X$                                           |      | 3.5  | 6    | mA            |
| $t_{D\_STBY}^{(1)}$ | Standby mode blanking time                            | $V_{CC} = 13\text{ V}$ ;<br>$I_{N_A} = I_{N_B} = PMW = 0\text{ V}$ ;<br>$V_{SEL0}$ from $5\text{ V}$ to $0\text{ V}$              | 0.2  | 1    | 1.8  | ms            |
| $R_{ONHS}$          | Static high-side resistance                           | $I_{OUT} = 2.5\text{ A}$ ; $T_j = 25^\circ\text{C}$                                                                               |      | 60   |      | m $\Omega$    |
|                     |                                                       | $I_{OUT} = 2.5\text{ A}$ ; $T_j = -40$ to $150^\circ\text{C}$                                                                     |      |      | 120  | m $\Omega$    |
| $R_{ONLS}$          | Static low-side resistance                            | $I_{OUT} = 2.5\text{ A}$ ; $T_j = 25^\circ\text{C}$                                                                               |      | 40   |      | m $\Omega$    |
|                     |                                                       | $I_{OUT} = 2.5\text{ A}$ ; $T_j = -40^\circ\text{C}$ to $150^\circ\text{C}$                                                       |      |      | 80   | m $\Omega$    |
| $V_f$               | High-side free-wheeling diode forward voltage         | $I_{OUT} = -2.5\text{ A}$ ; $T_j = 150^\circ\text{C}$                                                                             |      | 0.7  | 0.9  | V             |
| $I_{L(off)}$        | Off-state output current of one leg                   | $I_{N_A} = I_{N_B} = 0$ ; $PWM = 0$ ;<br>$V_{CC} = 13\text{ V}$ ; $T_j = 25^\circ\text{C}$                                        | 0    |      | 0.5  | $\mu\text{A}$ |
|                     |                                                       | $I_{N_A} = I_{N_B} = 0$ ; $PWM = 0$ ;<br>$V_{CC} = 13\text{ V}$ ; $T_j = 125^\circ\text{C}$                                       | 0    |      | 3    | $\mu\text{A}$ |
| $I_{L(off\_h)}$     | Off-state output current of one leg with other HSD on | $I_{N_A} = 0$ ; $I_{N_B} = 5\text{ V}$ ; $PWM = 0$ ;<br>$V_{CC} = 13\text{ V}$                                                    | 20   |      | 60   | $\mu\text{A}$ |

1. To power on the device from the standby, it is recommended to toggle  $I_{N_A}$  or  $I_{N_B}$  from 0 to 1 first and then PWM from 0 to 1 to avoid any over-stress on the device in case of short-to-battery.y.

**Table 7. Logic inputs (IN<sub>A</sub>, IN<sub>B</sub>, PWM) (V<sub>CC</sub> = 7 V up to 28 V; -40°C < T<sub>j</sub> < 150°C)**

| Symbol                                                                              | Parameter                | Test conditions          | Min. | Typ. | Max. | Unit |
|-------------------------------------------------------------------------------------|--------------------------|--------------------------|------|------|------|------|
| V <sub>IL</sub>                                                                     | Input low level voltage  |                          |      |      | 0.9  | V    |
| V <sub>IH</sub>                                                                     | Input high level voltage |                          | 2.1  |      |      | V    |
| V <sub>IHYST</sub>                                                                  | Input hysteresis voltage |                          | 0.2  |      |      | V    |
| V <sub>ICL</sub>                                                                    | Input clamp voltage      | I <sub>IN</sub> = 1 mA   | 5.3  |      | 7.2  | V    |
|                                                                                     |                          | I <sub>IN</sub> = -1 mA  |      | -0.7 |      | V    |
| I <sub>INL</sub>                                                                    | Input current            | V <sub>IN</sub> = 0.9 V  | 1    |      |      | μA   |
| I <sub>INH</sub>                                                                    | Input current            | V <sub>IN</sub> = 2.1 V  |      |      | 10   | μA   |
| SEL <sub>0</sub> (V <sub>CC</sub> = 7 V up to 18 V; -40°C < T <sub>j</sub> < 150°C) |                          |                          |      |      |      |      |
| V <sub>SELL</sub>                                                                   | Input low level voltage  |                          |      |      | 0.9  | V    |
| I <sub>SELL</sub>                                                                   | Low level input current  | V <sub>SEL</sub> = 0.9 V | 1    |      |      | μA   |
| V <sub>SELH</sub>                                                                   | Input high level voltage |                          | 2.1  |      |      | V    |
| I <sub>SELH</sub>                                                                   | High level input current | V <sub>SEL</sub> = 2.1 V |      |      | 10   | μA   |
| V <sub>SEL(hyst)</sub>                                                              | Input hysteresis voltage |                          | 0.2  |      |      | V    |
| V <sub>SELCL</sub>                                                                  | Input clamp voltage      | I <sub>SEL</sub> = 1 mA  | 5.3  |      | 7.5  | V    |
|                                                                                     |                          | I <sub>SEL</sub> = -1 mA |      | -0.8 |      | V    |
| PWM (V <sub>CC</sub> = 7 V up to 28 V; -40°C < T <sub>j</sub> < 150°C)              |                          |                          |      |      |      |      |
| V <sub>PWM</sub>                                                                    | Input low level voltage  |                          |      |      | 0.9  | V    |
| I <sub>PWM</sub>                                                                    | Low level input current  | V <sub>PWM</sub> = 0.9 V | 1    |      |      | μA   |
| V <sub>PWM</sub>                                                                    | Input high level voltage |                          | 2.1  |      |      | V    |
| I <sub>PWMH</sub>                                                                   | High level input current | V <sub>PWM</sub> = 2.1 V |      |      | 10   | μA   |
| V <sub>PWM(hyst)</sub>                                                              | Input hysteresis voltage |                          | 0.2  |      |      | V    |
| V <sub>PMWCL</sub>                                                                  | Input clamp voltage      | I <sub>PWM</sub> = 1 mA  | 5.3  |      | 7.2  | V    |
|                                                                                     |                          | I <sub>PWM</sub> = -1 mA |      | -0.7 |      | V    |

**Table 8. Switching (V<sub>CC</sub> = 13 V; R<sub>LOAD</sub> = 5.2 Ω)**

| Symbol              | Parameter                   | Test conditions                                        | Min. | Typ. | Max. | Unit |
|---------------------|-----------------------------|--------------------------------------------------------|------|------|------|------|
| f <sup>(1)</sup>    | PWM frequency               |                                                        | 0    |      | 20   | kHz  |
| t <sub>d(on)</sub>  | Turn-on delay time          | Input rise time < 1 μs (see <a href="#">Figure 6</a> ) |      | 20   |      | μs   |
| t <sub>d(off)</sub> | Turn-off delay time         | Input rise time < 1 μs (see <a href="#">Figure 6</a> ) |      | 13   |      | μs   |
| t <sub>r</sub>      | Rise time                   | See <a href="#">Figure 5</a>                           |      | 1    | 2    | μs   |
| t <sub>f</sub>      | Fall time                   | See <a href="#">Figure 5</a>                           |      | 1    | 2    | μs   |
| t <sub>cross</sub>  | Low-side turn-on delay time | Input rise time < 1 μs (see <a href="#">Figure 7</a> ) | 40   | 140  | 240  | μs   |

1. Parameter guaranteed by design and characterization; not subjected to production test.

Table 9. Protections and diagnostics ( $V_{CC} = 7\text{ V}$  up to  $18\text{ V}$ ;  $-40^{\circ}\text{C} < T_j < 150^{\circ}\text{C}$ )

| Symbol             | Parameter                                                                                      | Test conditions                                                                                                                                                                      | Min. | Typ. | Max. | Unit               |
|--------------------|------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|--------------------|
| $V_{USD}$          | Undervoltage shutdown                                                                          |                                                                                                                                                                                      |      |      | 4    | V                  |
| $V_{USDreset}$     | Undervoltage shutdown reset                                                                    |                                                                                                                                                                                      |      |      | 5    | V                  |
| $V_{USDHyst}$      | Undervoltage shutdown Hysteresis                                                               |                                                                                                                                                                                      |      | 0.4  |      | V                  |
| $I_{LIM\_H}$       | High-side current limitation                                                                   |                                                                                                                                                                                      | 12   | 18   | 24   | A                  |
| $I_{SD\_LS}$       | Shutdown LS current                                                                            |                                                                                                                                                                                      | 15   | 22   | 30   | A                  |
| $t_{SD\_LS}$       | Time to shutdown for the low-side                                                              | $V_{INA} = V_{INB} = 0\text{ V}$ ;<br>PWM = 5 V (see <a href="#">Figure 8</a> )                                                                                                      |      | 5    |      | $\mu\text{s}$      |
| $V_{CL\_HSD}$      | High-side clamp voltage ( $V_{CC}$ to $OUT_A = 0$ or $OUT_B = 0$ )                             | $I_{OUT} = 100\text{ mA}$ ;<br>$t_{CLAMP} = 1\text{ ms}$                                                                                                                             | 38   | 46   |      | V                  |
| $V_{CL\_LSD}$      | Low-side clamp voltage ( $OUT_A = V_{CC}$ or $OUT_B = V_{CC}$ to GND)                          | $I_{OUT} = 100\text{ mA}$ ;<br>$t_{CLAMP} = 1\text{ ms}$                                                                                                                             | 38   | 46   |      | V                  |
| $T_{TSD\_HS}$      | High-side thermal shutdown temperature                                                         | $IN_x = 2.1\text{ V}$                                                                                                                                                                | 150  | 175  | 200  | $^{\circ}\text{C}$ |
| $T_{TR\_HS}$       | High-side thermal reset temperature                                                            |                                                                                                                                                                                      | 135  |      |      | $^{\circ}\text{C}$ |
| $T_{HYST\_HS}$     | High-side thermal hysteresis ( $T_{SD\_HS} - T_{R\_HS}$ )                                      |                                                                                                                                                                                      |      | 7    |      | $^{\circ}\text{C}$ |
| $T_{TSD\_LS}$      | Low-side thermal shutdown temperature                                                          | $IN_x = 0\text{ V}$                                                                                                                                                                  | 150  | 175  | 200  | $^{\circ}\text{C}$ |
| $V_{CL}$           | Total clamp voltage ( $V_{CC}$ to GND)                                                         | $I_{OUT} = 100\text{ mA}$ ;<br>$t_{CLAMP} = 1\text{ ms}$                                                                                                                             | 38   | 46   | 52   | V                  |
| $V_{OL}$           | OFF-state open-load voltage detection threshold                                                | $IN_A = IN_B = 0$ ; PWM = 0;<br>$V_{SEL0} = 5\text{ V}$ for CHA;<br>$V_{SEL0} = 0\text{ V}$ and within $t_{D\_STBY}$ for CHB                                                         | 2    | 3    | 4    | V                  |
| $I_{L(off2)}$      | OFF-state output sink current                                                                  | $IN_A = IN_B = 0$ ; $V_{OUTx} = V_{OL}$ ;<br>PWM = 0 V; $V_{SEL0} = 5\text{ V}$ for CHA; $V_{SEL0} = 0\text{ V}$ and within $t_{D\_STBY}$ for CHB                                    | -100 |      | -15  | $\mu\text{A}$      |
| $t_{DSTKON}$       | OFF-state diagnostic delay time from falling edge of INPUT (see <a href="#">Figure 4</a> )     | $IN_A = 5\text{ V}$ to $0\text{ V}$ ; $IN_B = 0\text{ V}$ ;<br>$V_{SEL0} = 5\text{ V}$ ; $I_{OUT} = 0\text{ A}$ ;<br>$V_{OUTA} = 4\text{ V}$ ; PWM = 0 V                             | 40   | 140  | 240  | $\mu\text{s}$      |
| $t_{D\_VOL}^{(1)}$ | OFF-state diagnostic delay time from rising edge of $V_{OUT}$ (see <a href="#">Figure 11</a> ) | $IN_A = IN_B = 0\text{ V}$ ; PWM = 0 V;<br>$V_{OUTx} = 0\text{ V}$ to $4\text{ V}$ ;<br>$V_{SEL0} = 5\text{ V}$ for CHA;<br>$V_{SEL0} = 0\text{ V}$ and within $t_{D\_STBY}$ for CHB |      | 5    | 30   | $\mu\text{s}$      |

**Table 9. Protections and diagnostics ( $V_{CC} = 7\text{ V}$  up to  $18\text{ V}$ ;  $-40^{\circ}\text{C} < T_j < 150^{\circ}\text{C}$ )**

| Symbol                            | Parameter                                                                    | Test conditions                                               | Min. | Typ. | Max. | Unit          |
|-----------------------------------|------------------------------------------------------------------------------|---------------------------------------------------------------|------|------|------|---------------|
| $t_{\text{Latch\_RST\_HD}}^{(1)}$ | Input reset time for high-side fault unlatch (see <a href="#">Figure 9</a> ) | $V_{\text{INx}} = 5\text{ V}$ to $0\text{ V}$ ; HSDx faulting | 3    | 10   | 20   | $\mu\text{s}$ |
| $t_{\text{Latch\_RST\_LS}}^{(1)}$ | Input reset time for low-side fault unlatch (see <a href="#">Figure 10</a> ) | $V_{\text{INx}} = 0\text{ V}$ to $5\text{ V}$ ; LSDx faulting | 3    | 10   | 20   | $\mu\text{s}$ |

1. Parameter guaranteed by design and characterization; not subject to production test.

**Table 10. CS ( $7\text{ V} < V_{CC} < 18\text{ V}$ ;  $-40^{\circ}\text{C} < T_j < 150^{\circ}\text{C}$ )**

| Symbol                  | Parameter                         | Test conditions                                                                                                                                                                                         | Min. | Typ. | Max. | Unit          |
|-------------------------|-----------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|---------------|
| $V_{\text{SENSE\_CL}}$  | MultiSense clamp voltage          | $V_{CC} = 18\text{ V}$ ; $I_{\text{SENSE}} = -5\text{ mA}$                                                                                                                                              |      | 11   |      | V             |
|                         |                                   | $V_{CC} = 18\text{ V}$ ; $I_{\text{SENSE}} = 5\text{ mA}$                                                                                                                                               | -13  |      | -9   | V             |
| $K_0$                   | $I_{\text{OUT}}/I_{\text{SENSE}}$ | $I_{\text{OUT}} = 0.05\text{ A}$ ; $V_{\text{SENSE}} = 0.5\text{ V}$ ; $T_j = -40^{\circ}\text{C}$ to $150^{\circ}\text{C}$                                                                             | 420  |      |      |               |
| $K_1$                   | $I_{\text{OUT}}/I_{\text{SENSE}}$ | $I_{\text{OUT}} = 0.2\text{ A}$ ; $V_{\text{SENSE}} = 0.5\text{ V}$ ; $T_j = -40^{\circ}\text{C}$ to $150^{\circ}\text{C}$                                                                              | 710  | 1190 | 1670 |               |
| $K_2$                   | $I_{\text{OUT}}/I_{\text{SENSE}}$ | $I_{\text{OUT}} = 2.5\text{ A}$ ; $V_{\text{SENSE}} = 4\text{ V}$ ; $T_j = -40^{\circ}\text{C}$ to $150^{\circ}\text{C}$                                                                                | 1010 | 1120 | 1230 |               |
| $K_3$                   | $I_{\text{OUT}}/I_{\text{SENSE}}$ | $I_{\text{OUT}} = 4\text{ A}$ ; $V_{\text{SENSE}} = 4\text{ V}$ ; $T_j = -40^{\circ}\text{C}$ to $150^{\circ}\text{C}$                                                                                  | 1030 | 1120 | 1210 |               |
| $dK_0/K_0^{(1)(2)}$     | Analog sense current drift        | $I_{\text{OUT}} = 0.05\text{ A}$ ; $V_{\text{SENSE}} = 0.5\text{ V}$ ; $T_j = -40^{\circ}\text{C}$ to $150^{\circ}\text{C}$                                                                             | -25  |      | 25   | %             |
| $dK_1/K_1^{(1)(2)}$     | Analog sense current drift        | $I_{\text{OUT}} = 0.2\text{ A}$ ; $V_{\text{SENSE}} = 0.5\text{ V}$ ; $T_j = -40^{\circ}\text{C}$ to $150^{\circ}\text{C}$                                                                              | -21  |      | 21   | %             |
| $dK_2/K_2^{(1)(2)}$     | Analog sense current drift        | $I_{\text{OUT}} = 2.5\text{ A}$ ; $V_{\text{SENSE}} = 4\text{ V}$ ; $T_j = -40^{\circ}\text{C}$ to $150^{\circ}\text{C}$                                                                                | -5   |      | 5    | %             |
| $dK_3/K_3^{(1)(2)}$     | Analog sense current drift        | $I_{\text{OUT}} = 4\text{ A}$ ; $V_{\text{SENSE}} = 4\text{ V}$ ; $T_j = -40^{\circ}\text{C}$ to $150^{\circ}\text{C}$                                                                                  | -4   |      | 4    | %             |
| $V_{\text{SENSE\_SAT}}$ | Max analog sense output voltage   | $V_{CC} = 7\text{ V}$ ; $R_{\text{SENSE}} = 10\text{ k}\Omega$ ; $V_{\text{SEL0}} = 5\text{ V}$ ; $I_{\text{OUTA}} = 4\text{ A}$ ; $V_{\text{INA}} = 5\text{ V}$ ; PWM = 0; $T_j = 150^{\circ}\text{C}$ | 5    |      |      | V             |
| $I_{\text{SENSE0}}$     | Multisense leakage current        | $I_{\text{OUT}} = 0\text{ A}$ ; $V_{\text{SENSE}} = 0\text{ V}$ ; $I_{\text{Nx}} = 0\text{ V}$ ; $\text{SEL}_0 = 0$ ; $T_j = -40^{\circ}\text{C}$ to $150^{\circ}\text{C}$ (standby)                    | 0    |      | 0.5  | $\mu\text{A}$ |
|                         |                                   | $I_{\text{OUT}} = 0\text{ A}$ ; $V_{\text{SENSE}} = 0\text{ V}$ ; $I_{\text{Nx}} = 0\text{ V}$ ; $\text{SEL}_0 = 5\text{ V}$ ; $T_j = -40^{\circ}\text{C}$ to $150^{\circ}\text{C}$ (no standby)        | 0    |      | 0.5  | $\mu\text{A}$ |
|                         |                                   | $I_{\text{Nx}} = 5\text{ V}$ ; PWM = 5 V; $T_j = -40^{\circ}\text{C}$ to $150^{\circ}\text{C}$ ; $I_{\text{OUT}} = 0\text{ A}$                                                                          | 0    |      | 5    | $\mu\text{A}$ |

Table 10. CS ( $7\text{ V} < V_{CC} < 18\text{ V}$ ;  $-40\text{ }^{\circ}\text{C} < T_j < 150\text{ }^{\circ}\text{C}$ ) (continued)

| Symbol                 | Parameter                                    | Test conditions                                                                                                                                                                                    | Min. | Typ. | Max. | Unit |
|------------------------|----------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|------|
| $V_{SENSEH}$           | Multisense output voltage in fault condition | $V_{CC} = 13\text{ V}$ ; $R_{SENSE} = 1\text{ k}\Omega$<br>– E.g: $OUT_A$ in open-load<br>$I_{NA} = 0\text{ V}$ ; $I_{OUTA} = 0\text{ A}$ ;<br>$V_{OUTA} = 4\text{ V}$ ; $V_{SEL0} = 5\text{ V}$   | 5    |      | 7    | V    |
| $V_{OUT\_MSD}^{(2)}$   | Output Voltage for MultiSense shutdown       | $V_{INA} = 5\text{ V}$ ; $V_{INB} = 0\text{ V}$ ;<br>$V_{SEL0} = 5\text{ V}$ ; $R_{SENSE} = 2.7\text{ k}\Omega$<br>$I_{OUT} = 2.5\text{ A}$                                                        |      | 5    |      | V    |
| $I_{SENSE\_SAT}^{(2)}$ | MultiSense saturation current                | $V_{CC} = 13\text{ V}$ ; $V_{SENSE} = 4\text{ V}$ ;<br>$V_{INA} = 5\text{ V}$ ; $V_{INB} = 0\text{ V}$ ;<br>$V_{SEL0} = 5\text{ V}$ ; $T_j = 150\text{ }^{\circ}\text{C}$                          | 6    |      |      | mA   |
| $I_{OUT\_SAT}^{(2)}$   | Output saturation current                    | $V_{CC} = 13\text{ V}$ ; $V_{SENSE} = 4\text{ V}$ ;<br>$V_{INA} = 5\text{ V}$ ; $V_{INB} = 0\text{ V}$ ;<br>$V_{SEL0} = 5\text{ V}$ ; $I_{OUT} = 7\text{ A}$ ; $T_j = 150\text{ }^{\circ}\text{C}$ | 7    |      |      | A    |
| $I_{SENSEH}$           | Multisense output voltage in fault condition | $V_{CC} = 13\text{ V}$ ; $V_{SENSE} = V_{SENSEH}$                                                                                                                                                  | 7    | 20   | 30   | mA   |

1. Analog sense current drift is deviation of factor K for a given device over ( $-40\text{ }^{\circ}\text{C}$  to  $150\text{ }^{\circ}\text{C}$  and  $9\text{ V} < V_{CC} < 18\text{ V}$ ) with respect to its value measured at  $T_j = 25\text{ }^{\circ}\text{C}$ ,  $V_{CC} = 13\text{ V}$ .
2. Parameter guaranteed by design and characterization; not subject to production test.

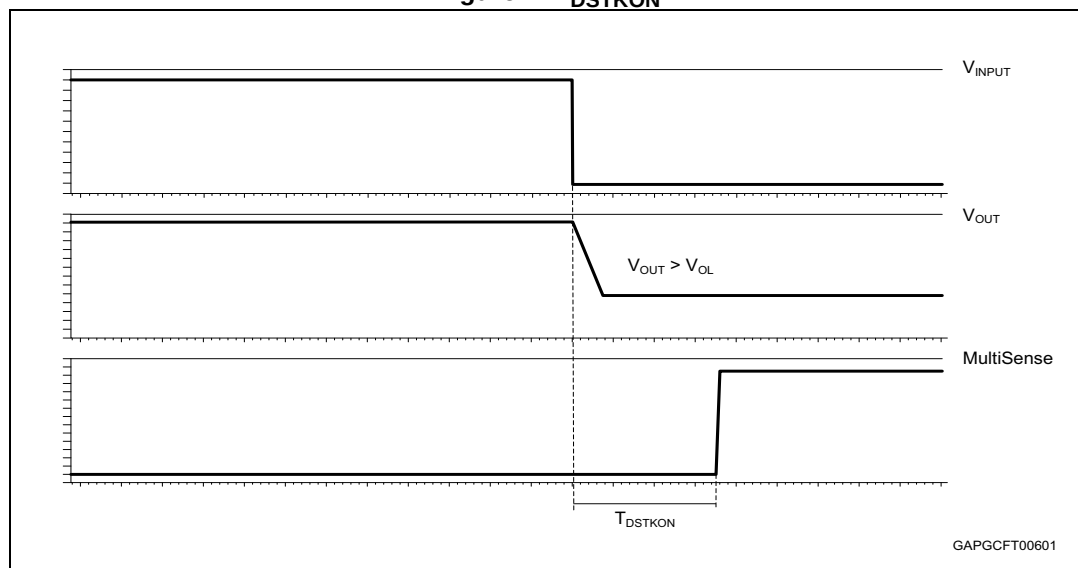
Figure 4.  $T_{DSTKON}$ 

Figure 5. Definition of the low-side switching times

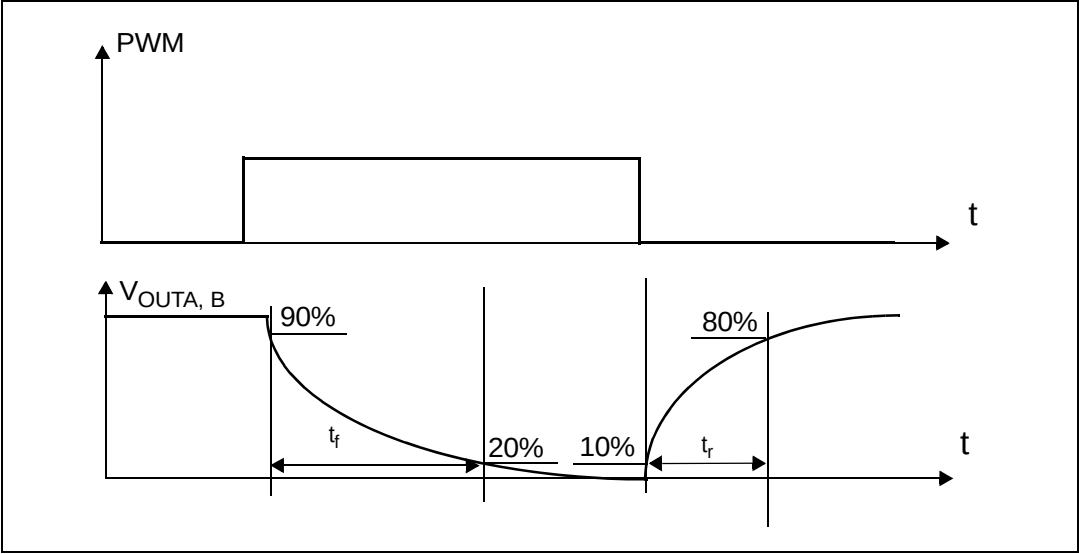


Figure 6. Definition of the high-side switching times

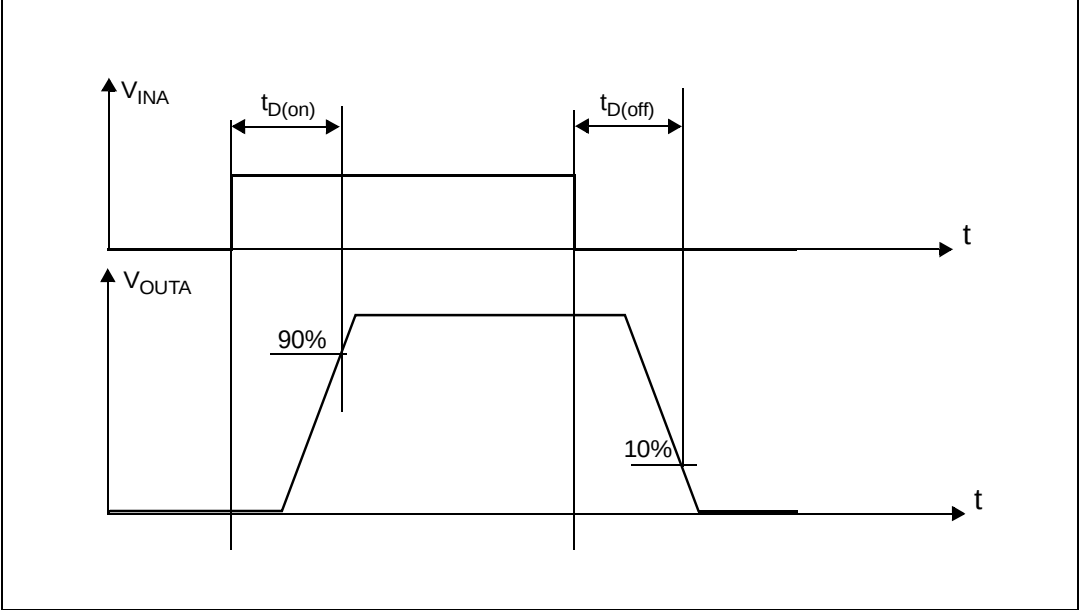


Figure 7. Low-side turn-on delay time

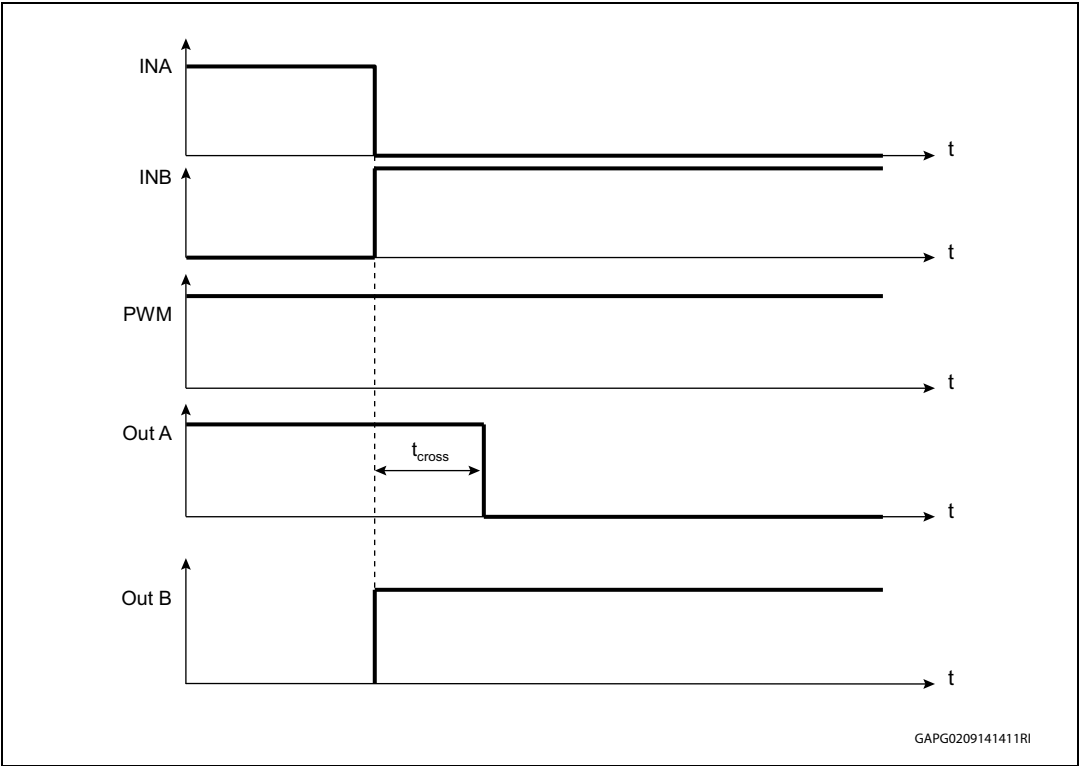


Figure 8. Time to shutdown for the low-side driver

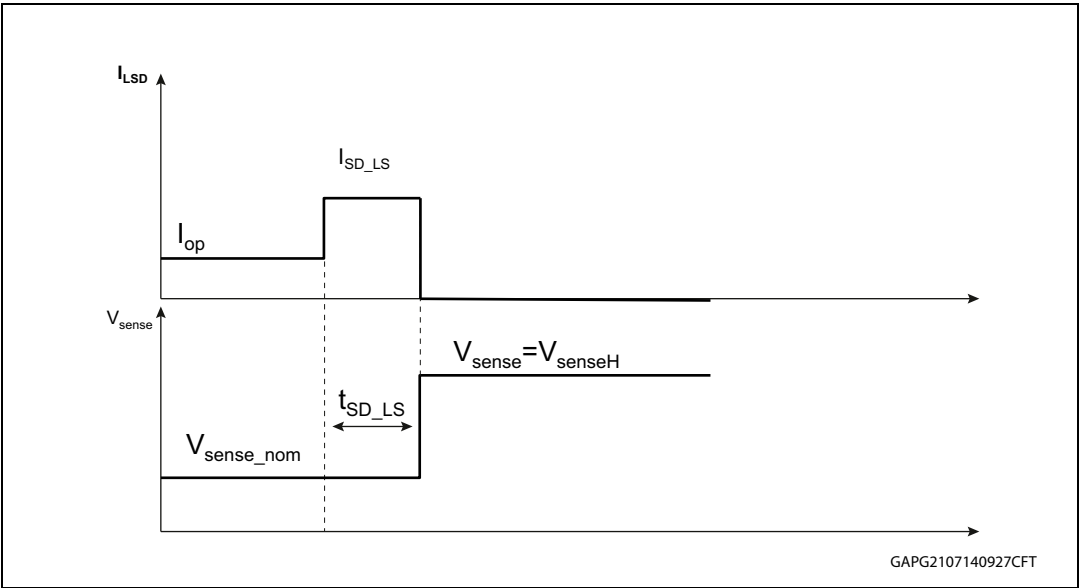


Figure 9. Input Reset time for HSD -fault unlatch

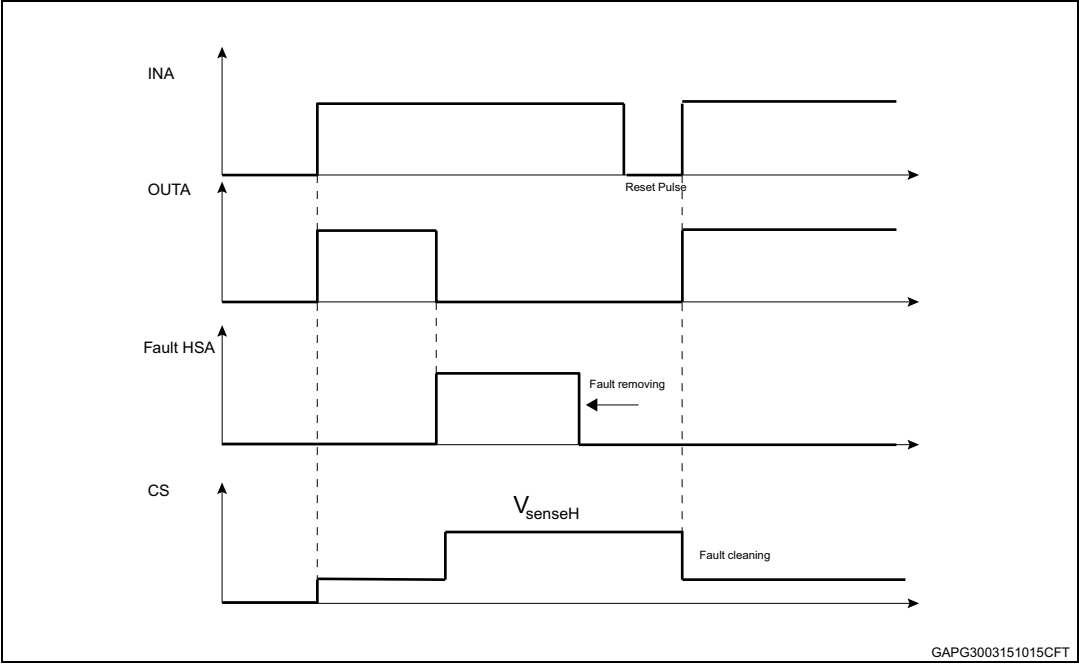


Figure 10. Input Reset time for LSD -fault unlatch

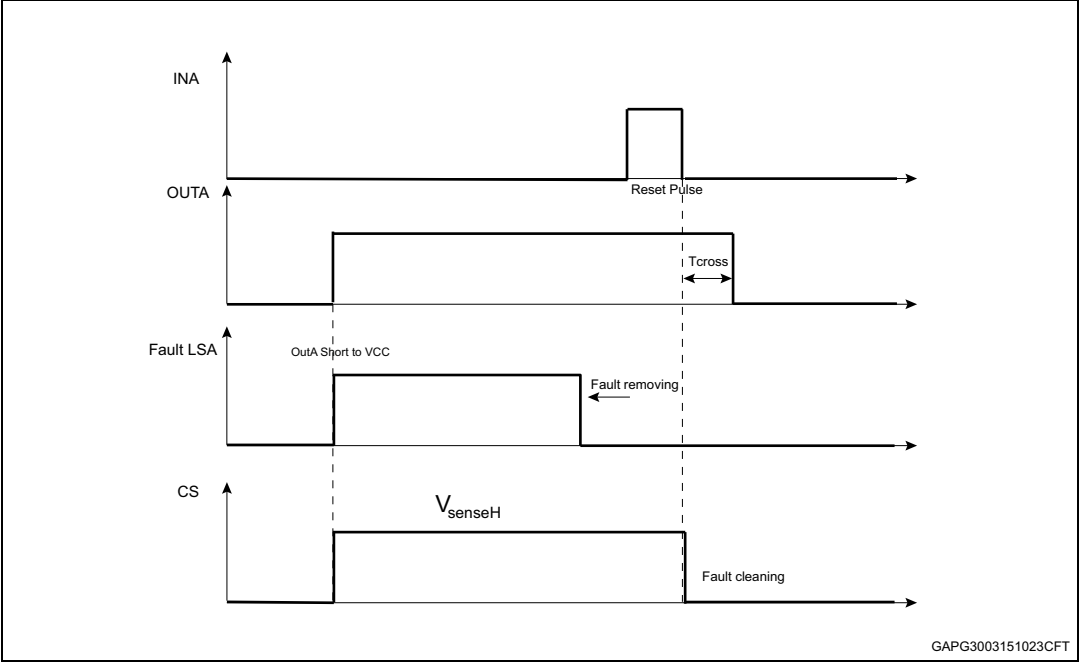




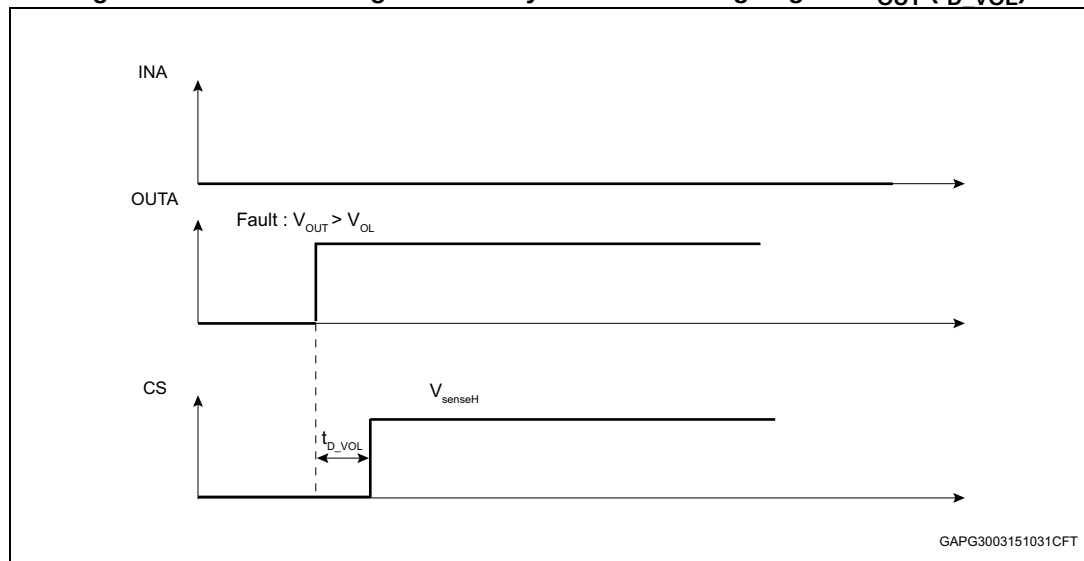
Figure 11. OFF-state diagnostic delay time from rising edge of  $V_{OUT}$  ( $t_{D\_VOL}$ )

Table 11. Operative condition - truth table

| Pin status      |                 |                  |     |                         | HSDs and LDSs Statu |      |      |      |
|-----------------|-----------------|------------------|-----|-------------------------|---------------------|------|------|------|
| IN <sub>A</sub> | IN <sub>B</sub> | SEL <sub>0</sub> | PWM | CS                      | HSDA                | LSDA | HSDB | LSDB |
| 1               | 1               | 1                | x   | Current Monitoring HSDA | On                  | Off  | On   | Off  |
|                 |                 | 0                |     | Current Monitoring HSDB |                     |      |      |      |
| 1               | 0               | 1                | 1   | Current Monitoring HSDA | On                  | Off  | Off  | On   |
|                 |                 |                  | 0   |                         | On                  | Off  | Off  | Off  |
| 1               | 0               | 0                | 1   | Hi-Z                    | On                  | Off  | Off  | On   |
|                 |                 |                  | 0   |                         | On                  | Off  | Off  | Off  |
| 0               | 1               | 1                | 1   | Hi-Z                    | Off                 | On   | On   | Off  |
|                 |                 |                  | 0   |                         | Off                 | Off  | On   | Off  |
| 0               | 1               | 0                | 1   | Current Monitoring HSDB | Off                 | On   | On   | Off  |
|                 |                 |                  | 0   |                         | Off                 | Off  | On   | Off  |
| 0               | 0               | 1                | 1   | Hi-Z                    | Off                 | On   | Off  | On   |
|                 |                 | 0                |     |                         |                     |      |      |      |
| 0               | 0               | 1                | 0   | x <sup>(1)</sup>        | Off                 | Off  | Off  | Off  |
|                 |                 | 0 <sup>(2)</sup> |     |                         | Off                 | Off  | Off  | Off  |

1. Refer to [Table 13: Off-state -truth table](#)

2. For IN<sub>A</sub> = IN<sub>B</sub> = SEL<sub>0</sub> = PWM = 0, the device enters in standby after t<sub>D\_STBY</sub>

Table 12. On-state fault conditions- truth table

| IN <sub>A</sub>     | IN <sub>B</sub> | SEL <sub>0</sub> | PWM | Out <sub>A</sub> | Out <sub>B</sub> | CS                  | Fault description                   |
|---------------------|-----------------|------------------|-----|------------------|------------------|---------------------|-------------------------------------|
| On state diagnostic |                 |                  |     |                  |                  |                     |                                     |
| 0                   | 0               | 0                | 1   | X                | H                | V <sub>SENSEH</sub> | Short to V <sub>BATT</sub> an Leg B |
| 0                   | 0               | 1                | 1   | H                | X                | V <sub>SENSEH</sub> | Short to V <sub>BATT</sub> an Leg A |
| 0                   | 1               | 0                | X   | X                | L                | V <sub>SENSEH</sub> | Out B short to GND                  |
| 0                   | 1               | 1                | 1   | H                | H                | V <sub>SENSEH</sub> | Out A short to V <sub>CC</sub>      |
| 1                   | 0               | 0                | 1   | H                | H                | V <sub>SENSEH</sub> | Out B short to V <sub>CC</sub>      |
| 1                   | 0               | 1                | X   | L                | L                | V <sub>SENSEH</sub> | Out A short to GND                  |
| 1                   | 1               | 0                | X   | X                | L                | V <sub>SENSEH</sub> | Short to GND an Leg B               |
| 1                   | 1               | 1                | X   | L                | X                | V <sub>SENSEH</sub> | Short to GND an Leg A               |

Table 13. Off-state -truth table

| IN <sub>A</sub>      | IN <sub>B</sub> | SEL <sub>0</sub>    | PWM | Out <sub>A</sub>                   | Out <sub>B</sub>                   | CS                  | Description                                                                                                                                                                                                                                                                                                                         |
|----------------------|-----------------|---------------------|-----|------------------------------------|------------------------------------|---------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Off-state diagnostic |                 |                     |     |                                    |                                    |                     |                                                                                                                                                                                                                                                                                                                                     |
| 0                    | 0               | 1                   | 0   | V <sub>outA</sub> >V <sub>OL</sub> | x                                  | V <sub>SENSEH</sub> | Case 1. Out <sub>A</sub> shorted to V <sub>CC</sub> if no pull-up is applied<br>Case 2. No open-load in full bridge configuration with an external pull-up on Out <sub>B</sub><br>Case 3. open-load in half bridge configuration with an external pull-up on Out <sub>A</sub> (motor connected between Out <sub>A</sub> and Ground) |
|                      |                 |                     |     | V <sub>outA</sub> <V <sub>OL</sub> | x                                  | Hi-Z                | Case 1. Open-load in full Bridge configuration with an external pull-up on Out <sub>B</sub><br>Case 2. No open-load in half Bridge configuration with external pull-up on Out <sub>A</sub> (motor connected between Out <sub>A</sub> and Ground)                                                                                    |
|                      |                 | 0 <sup>(1)(2)</sup> |     | X                                  | V <sub>outB</sub> >V <sub>OL</sub> | V <sub>SENSEH</sub> | Case 1. Out <sub>B</sub> shorted to V <sub>CC</sub> if no pull-up is applied<br>Case 2. No open-load in full bridge configuration with external pull-up on Out <sub>A</sub><br>Case 3. Open-load in half bridge configuration with external pull-up on Out <sub>B</sub> (motor connected between Out <sub>B</sub> and Ground)       |
|                      |                 |                     |     | X                                  | V <sub>outB</sub> <V <sub>OL</sub> | Hi-Z                | Case1. Open-load in full Bridge configuration with an external pull-up on Out <sub>A</sub><br>Case 2. No open-load in half Bridge configuration with external pull-up on Out <sub>B</sub> (motor connected between Out <sub>B</sub> and Ground)                                                                                     |

1. The device enters standby mode after t<sub>D\_STBY</sub>

2. To power on the device from the standby, it is recommended to toggle IN<sub>A</sub> or IN<sub>B</sub> from 0 to 1 first and then PWM from 0 to 1 to avoid any over-stress on the device in case of short-to-battery.

## 3 Application information

### 3.1 Reverse battery protection

Three possible solutions can be considered:

- A Schottky diode D connected to V<sub>CC</sub> pin
- An N-channel MOSFET connected to the GND pin
- A P-channel MOSFET connected to the V<sub>CC</sub> pin

The device sustains no more than -15 A in reverse battery conditions because of the two Body diodes of the Power MOSFETs. Additionally, in reverse battery condition the I/Os of the device is pulled down to the V<sub>CC</sub> line (approximately -1.5 V).

Series resistor must be inserted to limit the current sunk from the microcontroller I/Os. If I<sub>Rmax</sub> is the maximum target reverse current through microcontroller I/Os, series resistor is:

$$R = \frac{V_{IOs} - V_{CC}}{I_{Rmax}}$$

### 3.2 GND protection network against reverse battery

#### 3.2.1 Diode (D<sub>GND</sub>) in the ground line

A resistor (typ. R<sub>GND</sub> = 4.7 kΩ) should be inserted in parallel to D<sub>GND</sub> if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network produces a shift (≈600 mV) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift does not vary if more than one HSD shares the same diode/resistor network.

### 3.3 Immunity against transient electrical disturbances

The immunity of the device against transient electrical emissions, conducted along the supply lines and injected into the V<sub>CC</sub> pin, is tested in accordance with ISO7637-2:2011 (E) and ISO 16750-2:2010.

The related function performance status classification is shown in [Table 14](#).

Test pulses are applied directly to DUT (Device Under Test) both in ON and OFF-state and in accordance to ISO 7637-2:2011(E), chapter 4. The DUT is intended as the present device only, without components and accessed through V<sub>CC</sub> and GND terminals.

Status II is defined in ISO 7637-1 Function Performance Status Classification (FPSC) as follows: "The function does not perform as designed during the test but returns automatically to normal operation after the test".

Table 14. ISO 7637-2 - electrical transient conduction along supply line

| Test Pulse 2011(E)                             | Test pulse severity level with Status II functional performance status |             | Minimum number of pulses or test time | Burst cycle / pulse repetition time |        | Pulse duration and pulse generator internal impedance |
|------------------------------------------------|------------------------------------------------------------------------|-------------|---------------------------------------|-------------------------------------|--------|-------------------------------------------------------|
|                                                | Level                                                                  | $U_S^{(1)}$ |                                       | min                                 | max    |                                                       |
| 1                                              | III                                                                    | -112 V      | 500 pulses                            | 0,5 s                               |        | 2ms, 10 $\Omega$                                      |
| 2a                                             | III                                                                    | +55 V       | 500 pulses                            | 0,2 s                               | 5 s    | 50 $\mu$ s, 2 $\Omega$                                |
| 3a                                             | IV                                                                     | -220 V      | 1h                                    | 90 ms                               | 100 ms | 0.1 $\mu$ s, 50 $\Omega$                              |
| 3b                                             | IV                                                                     | +150 V      | 1h                                    | 90 ms                               | 100 ms | 0.1 $\mu$ s, 50 $\Omega$                              |
| 4 <sup>(2)</sup>                               | IV                                                                     | -7 V        | 1 pulse                               |                                     |        | 100ms, 0.0 1 $\Omega$                                 |
| <b>Load dump according to ISO 16750-2:2010</b> |                                                                        |             |                                       |                                     |        |                                                       |
| Test B <sup>(3)</sup>                          |                                                                        | 40 V        | 5 pulse                               | 1 min                               |        | 400 ms, 2 $\Omega$                                    |

1.  $U_S$  is the peak amplitude as defined for each test pulse in ISO 7637-2:2011(E), chapter 5.6.

2. Test pulse from ISO 7637-2:2004(E).

3. With 40 V external suppressor referred to ground ( $-40^\circ\text{C} < T_j < 150^\circ\text{C}$ ).

## 4 Package and packing information

### 4.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com).

ECOPACK® is an ST trademark.

### 4.2 SO-16N mechanical data

Figure 12. SO-16N package dimensions

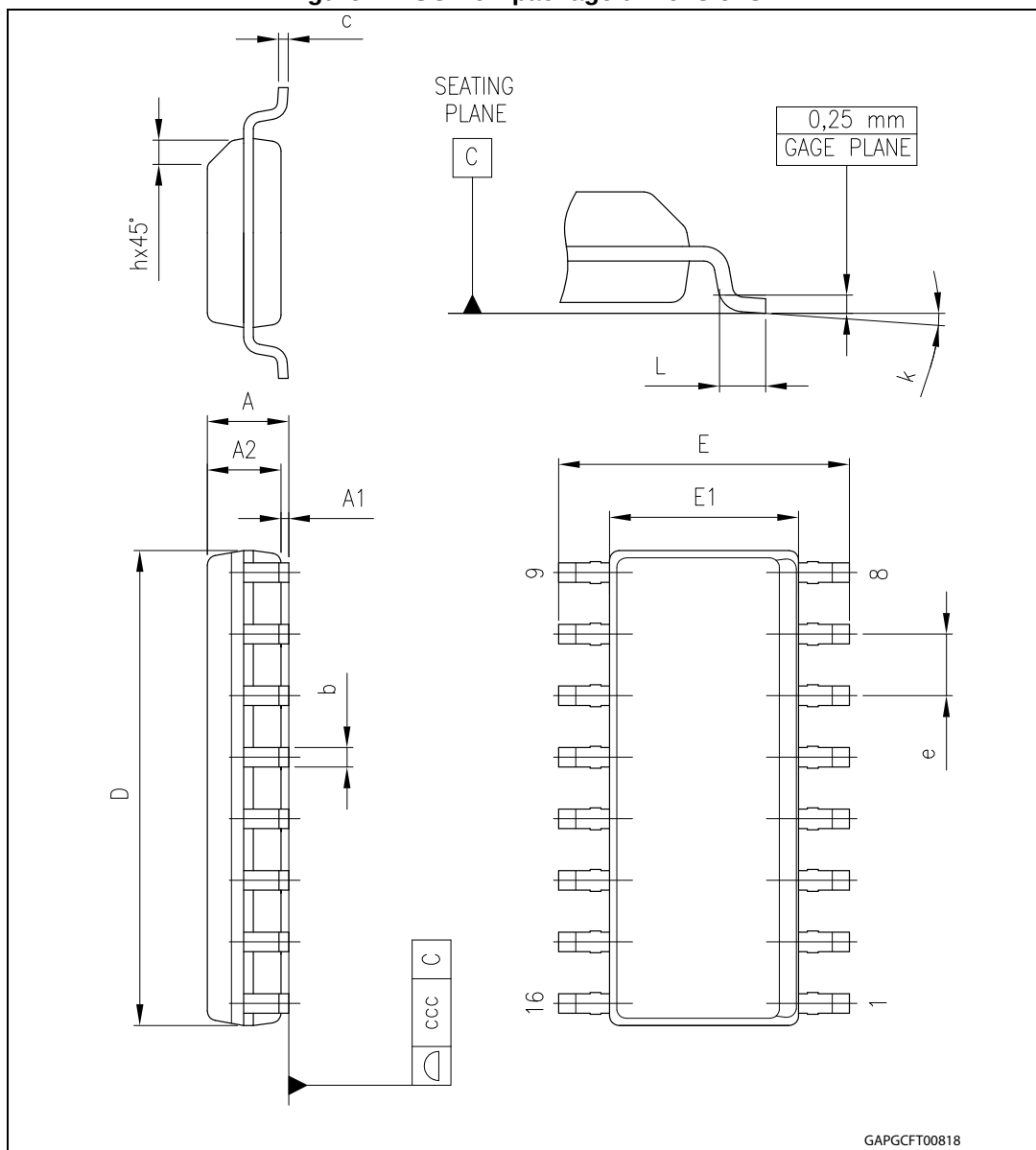


Table 15. SO-16N mechanical data

| Symbol | Millimeters |      |       |
|--------|-------------|------|-------|
|        | Min.        | Typ. | Max.  |
| A      |             |      | 1.75  |
| A1     | 0.10        |      | 0.25  |
| A2     | 1.25        |      |       |
| b      | 0.31        |      | 0.51  |
| c      | 0.17        |      | 0.25  |
| D      | 9.80        | 9.90 | 10.00 |
| E      | 5.80        | 6.00 | 6.20  |
| E1     | 3.80        | 3.90 | 4.00  |
| e      |             | 1.27 |       |
| h      | 0.25        |      | 0.50  |
| L      | 0.40        |      | 1.27  |
| k      | 0           |      | 8     |
| ccc    |             |      | 0.10  |

## 5 Revision history

**Table 16. Document revision history**

| Date        | Revision | Changes                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 19-May-2014 | 1        | Initial release.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 30-Jun-2014 | 2        | <p>Updated <a href="#">Features</a> list</p> <p>Updated <a href="#">Figure 1: Block diagram</a> and <a href="#">Figure 2: Configuration diagram (top view)</a></p> <p><a href="#">Table 3: Pin definitions and functions</a>:</p> <ul style="list-style-type: none"> <li>– Pin 13: updated symbol</li> </ul> <p><a href="#">Table 4: Absolute maximum ratings</a></p> <ul style="list-style-type: none"> <li>– <math>I_{SENSE}</math>, <math>V_{ESD}</math>: updated parameter</li> </ul> <p><a href="#">Table 6: Power section</a></p> <ul style="list-style-type: none"> <li>– <math>I_S</math>: updated values</li> <li>– <math>T_{D\_stby}</math>, <math>R_{ONHS}</math>, <math>R_{ONLS}</math>, <math>V_f</math>, <math>I_{L(off)}</math>: updated test conditions</li> <li>– <math>I_{L(off\_h)}</math>: added row</li> </ul> <p><a href="#">Table 7: Logic inputs (INA, INB, PWM) (<math>V_{CC} = 7\text{ V}</math> up to <math>28\text{ V}</math>; <math>-40^\circ\text{C} &lt; T_j &lt; 150^\circ\text{C}</math>)</a></p> <ul style="list-style-type: none"> <li>– <math>I_{PWM}</math>, <math>I_{PWMH}</math>, <math>V_{PWMCL}</math>: updated test conditions</li> </ul> <p><a href="#">Table 8: Switching (<math>V_{CC} = 13\text{ V}</math>; <math>R_{LOAD} = 5.2\ \Omega</math>)</a>:</p> <ul style="list-style-type: none"> <li>– <math>t_{d(on)}</math>, <math>t_{d(off)}</math>: updated values</li> <li>– <math>t_{cross}</math>: added row</li> </ul> <p><a href="#">Table 9: Protections and diagnostics (<math>V_{CC} = 7\text{ V}</math> up to <math>18\text{ V}</math>; <math>-40^\circ\text{C} &lt; T_j &lt; 150^\circ\text{C}</math>)</a></p> <ul style="list-style-type: none"> <li>– <math>I_{SD\_LS}</math>: updated value</li> <li>– <math>t_{SD\_LS}</math>: updated value and test conditions</li> <li>– Renamed parameter <math>V_{CLPHsd}</math> into <math>V_{CL\_HSD}</math>, <math>V_{CLPLSD}</math> into <math>V_{CL\_LSD}</math> and <math>V_{CLP}</math> into <math>V_{CL}</math>; updated test conditions</li> <li>– <math>V_{OL}</math>, <math>I_{L(off2)}</math>, <math>t_{DSTKON}</math>, <math>t_{D\_VOL}</math>: updated test conditions</li> </ul> <p><a href="#">Table 10: CS (<math>7\text{ V} &lt; V_{CC} &lt; 18\text{ V}</math>; <math>-40^\circ\text{C} &lt; T_j &lt; 150^\circ\text{C}</math>)</a></p> <ul style="list-style-type: none"> <li>– <math>K_2</math>, <math>K_3</math>, <math>dK_2/K_2</math>: updated test conditions</li> <li>– <math>I_{SENSE0}</math>: updated parameter, test conditions and value</li> <li>– Renamed <math>V_{SENSE}</math> parameter into <math>V_{SENSEH}</math>: updated value</li> </ul> <p><a href="#">Table 11: Operative condition - truth table</a>, <a href="#">Table 12: On-state fault conditions- truth table</a> and <a href="#">Table 13: Off-state -truth table</a>:</p> <ul style="list-style-type: none"> <li>– Changed Multisense with CS</li> </ul> |



Table 16. Document revision history (continued)

| Date        | Revision | Changes                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-------------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 28-Jul-2014 | 3        | <p><i>Table 4: Absolute maximum ratings:</i></p> <ul style="list-style-type: none"> <li>– <math>V_{ESD}</math>: updated value</li> </ul> <p><i>Table 6: Power section:</i></p> <ul style="list-style-type: none"> <li>– <math>t_{D\_STBY}</math>: updated test condition</li> </ul> <p><i>Table 7: Logic inputs (INA, INB, PWM) (<math>V_{CC} = 7\text{ V}</math> up to <math>28\text{ V}</math>; <math>-40^{\circ}\text{C} &lt; T_j &lt; 150^{\circ}\text{C}</math>):</i></p> <ul style="list-style-type: none"> <li>– <math>V_{SELCL}</math>, <math>V_{PMWCL}</math>: updated value</li> </ul> <p><i>Table 8: Switching (<math>V_{CC} = 13\text{ V}</math>; <math>R_{LOAD} = 5.2\ \Omega</math>):</i></p> <ul style="list-style-type: none"> <li>– updated <math>R_{LOAD}</math> value</li> <li>– <math>t_{d(on)}</math>, <math>t_{d(off)}</math>: updated value</li> </ul> <p><i>Table 9: Protections and diagnostics (<math>V_{CC} = 7\text{ V}</math> up to <math>18\text{ V}</math>; <math>-40^{\circ}\text{C} &lt; T_j &lt; 150^{\circ}\text{C}</math>):</i></p> <ul style="list-style-type: none"> <li>– <math>I_{SD\_LS}</math>, <math>V_{CL\_HSD}</math>, <math>V_{CL\_LSD}</math>, <math>V_{CL}</math>: updated value</li> <li>– <math>t_{DSTKON}</math>, <math>t_{D\_VOL}</math>: updated test condition</li> <li>– <math>t_{Latch\_RST\_HD}</math>, <math>t_{Latch\_RST\_LS}</math>: added parameter</li> </ul> <p><i>Table 10: CS (<math>7\text{ V} &lt; V_{CC} &lt; 18\text{ V}</math>; <math>-40^{\circ}\text{C} &lt; T_j &lt; 150^{\circ}\text{C}</math>):</i></p> <ul style="list-style-type: none"> <li>– <math>K_X</math>, <math>dK_X/K_X</math>, <math>V_{SENSEsat}</math>, <math>I_{SENSE0}</math>: updated test conditions</li> </ul> <p>Updated <i>Figure 8: Time to shutdown for the low-side driver</i></p> |
| 30-Oct-2014 | 4        | <p><i>Table 6: Power section:</i></p> <ul style="list-style-type: none"> <li>– <math>t_{D\_STBY}</math>: updated test condition</li> </ul> <p><i>Table 10: CS (<math>7\text{ V} &lt; V_{CC} &lt; 18\text{ V}</math>; <math>-40^{\circ}\text{C} &lt; T_j &lt; 150^{\circ}\text{C}</math>):</i></p> <ul style="list-style-type: none"> <li>– <math>V_{SENSE\_CL}</math>, <math>I_{SENSE\_SAT}</math>, <math>I_{OUT\_SAT}</math>, <math>V_{OUT\_MSD}</math>: added parameters</li> <li>– <math>V_{SENSE\_SAT}</math>, <math>I_{SENSE0}</math>, <math>V_{SENSEH}</math>, <math>I_{SENSEH}</math>: updated test conditions</li> </ul> <p>Updated <i>Figure 7: Low-side turn-on delay time</i></p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 15-Dec-2014 | 5        | <p><i>Table 6: Power section:</i></p> <ul style="list-style-type: none"> <li>– <math>I_S</math> @ on-state: updated typical value</li> <li>– <math>I_{D\_STBY}</math>: added note</li> <li>– <math>I_{L(off\_h)}</math>: updated values</li> </ul> <p><i>Table 7: Logic inputs (INA, INB, PWM) (<math>V_{CC} = 7\text{ V}</math> up to <math>28\text{ V}</math>; <math>-40^{\circ}\text{C} &lt; T_j &lt; 150^{\circ}\text{C}</math>):</i></p> <ul style="list-style-type: none"> <li>– <math>V_{SELCL}</math>: updated typical value</li> </ul> <p><i>Table 8: Switching (<math>V_{CC} = 13\text{ V}</math>; <math>R_{LOAD} = 5.2\ \Omega</math>):</i></p> <ul style="list-style-type: none"> <li>– <math>t_{d(on)}</math>, <math>t_{d(off)}</math>: updated typical value</li> </ul> <p><i>Table 9: Protections and diagnostics (<math>V_{CC} = 7\text{ V}</math> up to <math>18\text{ V}</math>; <math>-40^{\circ}\text{C} &lt; T_j &lt; 150^{\circ}\text{C}</math>):</i></p> <ul style="list-style-type: none"> <li>– <math>V_{USDHyst}</math>: updated typical value</li> </ul> <p><i>Table 10: CS (<math>7\text{ V} &lt; V_{CC} &lt; 18\text{ V}</math>; <math>-40^{\circ}\text{C} &lt; T_j &lt; 150^{\circ}\text{C}</math>):</i></p> <ul style="list-style-type: none"> <li>– <math>V_{SENSE\_CL}</math>: updated test conditions and values</li> <li>– <math>K_X</math>, <math>dK_X/K_X</math>: updated values</li> <li>– <math>V_{OUT\_MSD}</math>, <math>I_{OUT\_SAT}</math>: updated test conditions</li> </ul> <p><i>Table 13: Off-state -truth table:</i></p> <ul style="list-style-type: none"> <li>– <math>SEL_0</math>: added note</li> </ul>                                                                                                                                                                          |

Table 16. Document revision history (continued)

| Date        | Revision | Changes                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
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| 01-Apr-2015 | 6        | <p>Updated <a href="#">Figure 1: Block diagram</a></p> <p><a href="#">Table 3: Pin definitions and functions</a>:</p> <ul style="list-style-type: none"> <li>– PWM: updated function description</li> </ul> <p><a href="#">Table 9: Protections and diagnostics (VCC = 7 V up to 18 V; -40°C &lt; Tj &lt; 150°C)</a>:</p> <ul style="list-style-type: none"> <li>– V<sub>USDHyst</sub>: updated typical value</li> <li>– V<sub>CL_HSD</sub>: updated test condition and values</li> </ul> <p><a href="#">Table 10: CS (7 V &lt; VCC &lt; 18 V; -40 °C &lt; Tj &lt; 150 °C)</a>:</p> <ul style="list-style-type: none"> <li>– K<sub>3</sub>, dK<sub>3</sub>/K<sub>3</sub>, I<sub>SENSE_SAT</sub>: updated test conditions</li> <li>– I<sub>OUT_SAT</sub>: updated test conditions and value</li> </ul> <p>Added following figures:</p> <ul style="list-style-type: none"> <li>– <a href="#">Figure 9: Input Reset time for HSD -fault unlatch</a></li> <li>– <a href="#">Figure 10: Input Reset time for LSD -fault unlatch</a></li> <li>– <a href="#">Figure 11: OFF-state diagnostic delay time from rising edge of VOUT (tD_VOL)</a></li> </ul> <p>Updated <a href="#">Table 12: On-state fault conditions- truth table</a> and <a href="#">Table 15: SO-16N mechanical data</a></p> |
| 19-May-2015 | 7        | <p>Added <a href="#">Section 3.1: Reverse battery protection</a></p> <p><a href="#">Table 9: Protections and diagnostics (VCC = 7 V up to 18 V; -40°C &lt; Tj &lt; 150°C)</a>:</p> <ul style="list-style-type: none"> <li>– V<sub>CL_HSD</sub>, V<sub>CL_LSD</sub>: updated test conditions</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 09-Jun-2015 | 8        | <p><a href="#">Table 8: Switching (VCC = 13 V; RLOAD = 5.2 Ω)</a>:</p> <ul style="list-style-type: none"> <li>– f: added note</li> </ul> <p><a href="#">Table 9: Protections and diagnostics (VCC = 7 V up to 18 V; -40°C &lt; Tj &lt; 150°C)</a>:</p> <ul style="list-style-type: none"> <li>– V<sub>CL</sub>: updated test conditions</li> <li>– t<sub>D_VOL</sub>: added note</li> </ul> <p><a href="#">Table 10: CS (7 V &lt; VCC &lt; 18 V; -40 °C &lt; Tj &lt; 150 °C)</a>:</p> <ul style="list-style-type: none"> <li>– V<sub>SENSE_SAT</sub>: updated test conditions</li> <li>– dK<sub>0</sub>/K<sub>0</sub>, dK<sub>1</sub>/K<sub>1</sub>, dK<sub>2</sub>/K<sub>2</sub>, dK<sub>3</sub>/K<sub>3</sub>, I<sub>SENSE_SAT</sub>: added note</li> <li>– I<sub>OUT_SAT</sub>: updated value</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |

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