microSDHC and microSDXC Memory Card
Flash Storage Media

1. Introduction

microSDHC and microSDXC cards offer large volume data storage and optimized recording performance with support for FAT32 and exFAT file formats. In addition, Kingston's SD cards use new speed rating known as "Class" and Ultra High Speed Interface supported, which delivers a minimum data transfer rate for optimum performance with respective microSDHC and microSDXC host devices. Although identical in size to standard microSD cards, SDHC and SDXC cards are specially designed and are only recognized by SDHC and SDXC host devices respectively.

2. Part Number(S)

SDHC Class	UHS	UHS Class	VSC	App Class	Capacity	Part Number
Class 10	I	U1	V10	A1	16GB	SDCS2/16GB
Class 10	I	U1	V10	A1	32GB	SDCS2/32GB
Class 10	I	U1	V10	A1	64GB	SDCS2/64GB
Class 10	I	U1	V10	A1	128GB	SDCS2/128GB
Class 10	I	U3	V30	A1	256GB	SDCS2/256GB
Class 10	I	U3	V30	A1	512GB	SDCS2/512GB

3. microSD Memory Card Features

Table 1: microSDHC and microSDXC Card Features

Design	Standard	
Contents	None (OEM Design Available)	ID, MKB Programmed
Security Functions	SD Security Specification Ver.4.00 Compliant (Non-CPRM Based) *CPRM: Contents Protection for Recording Media Specification	
Logical Format	SD Files System Specification Ver.3.00 Compliant (microSDHC FAT32/microSDXC exFAT Based formatted)	
Electrical	Operating Voltage: 2.7V to 3.6V (Memory Operation) Interfaces: SD Card Interface, (SD: 4 or 1bit) SPI Mode Compatible SD Physical Layer Specification Ver.6.10 Compliant	
Physical	L: 15, W: 11 , T: 1.0 (mm), Weight: 0.5g (typ.) microSD Memory Card Specification Ver. 4.20 Compliant (Detailed Dimensions included at: Appendix.)	
Durability	SD Physical Layer Specification Ver.6.10 Compliant microSD Memory Card Specification Ver. 4.20 Compliant	
ROHS	ROHS Compatible	

4. Compatibility

Compliant Specifications

SD Memory Card Specifications

- Compliant with PHYSICAL LAYER SPECIFICATION Ver.6.10. (Part1)
- Compliant with FILE SYSTEM SPECIFICATION Ver.3.00. (Part2)
- Compliant with SECURITY SPECIFICATION Ver.4.00. (Part3)
- microSD Memory Card Specification Ver. 4.20

5. Physical Characteristics

5.1. Temperature

1) Operation Conditions
Temperature Range: Ta= -25 °C to +85 °C

2) Storage Conditions
Temperature Range: Tstg= -40 °C to +85 °C

5.2. Moisture (Reliability)

1) Operation Conditions
Temperature 25 °C / 95% rel. humidity

2) Storage Conditions
Temperature 40 °C / 93% rel. humidity / 500h

5.3. Application

1) Hot Insertion or Removal
   a. Kingston microSDHC and microSDXC Memory Card can be removed and/or inserted without powering off the host system.
2) Mechanical Write Protect Switch
   a. microSDHC and microSDXC Memory Card has no mechanical write protect switch.

6. Electrical Interface Outlines

6.1. microSD Card Pins

Table 2 define the pin assignment of the microSD card.
Fig.1 describes the pin location of the microSD card.

Please refer the details descriptions by SD Card Physical Layer Specification.

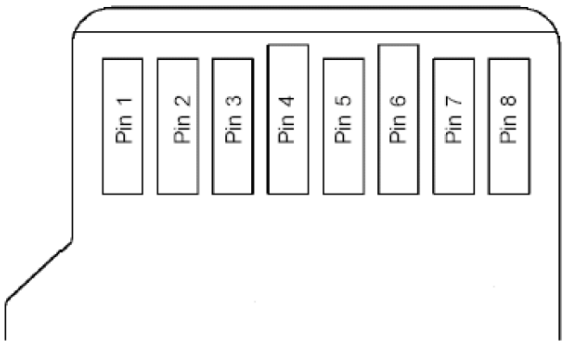

Figure 1: microSD Card Pin Assignment (Back View of Card)

Table 2: microSD Card Pin Assignment

Pins	SD Mode			SPI Mode		
	Name	IO type [1]	Description	Name	IO Type	Description
1	DAT2	I/O /PP	Data Line[Bit2]	RSV		
2	CD/ DAT3	I/O/PP	Card Detect / Data Line[Bit3]	CS	I	Chip Select (neg true)
3	CMD	PP	Command/Response	DI	I	Data In
4	V_{dd}	S	Supply Voltage	V_{dd}	S	Supply Voltage
5	CLK	I	Clock	SCLK	I	Clock
6	V_{SS}	S	Supply voltage ground	V_{SS}	S	Supply voltage ground
7	DAT0	I/O /PP	Data Line[Bit0]	DO	O/PP	Data Out
8	DAT1	I/O /PP	Data Line[Bit1]	RSV	-	Reserved (*)

1) S: Power Supply, I: Input, O: Output, I/O: Bi-Directional, PP: IO Using Push-Pull Drivers

(*) These Signals should be pulled up by host side with 10-100K ohm resistance in SPI Mode. Do not use NC pins.

6.2 microSD Card Bus Topology

The microSD Memory Card supports two alternative communication protocols: SD and SPI Bus Mode. Host System can choose either one of modes. Same Data of the microSD Card can read and write by both modes.

SD Mode allows the 4-bit high performance data transfer. SPI Mode allows easy and common interface for SPI channel. The disadvantage of this mode is loss of performance, relatively to the SD mode.

6.2.1 SD Bus Mode Protocol

The SD bus allows the dynamic configuration of the number of data line from 1 to 4 Bi-directional data signal. After power up by default, the microSD card will use only DAT0. After initialization, host can change the bus width.

Multiplied microSD cards connections are available to the host. Common V_{dd}, V_{ss} and CLK signal connections are available in the multiple connection. However, Command, Respond and Data lined (DAT0-DAT3) shall be divided for each card from host. This feature allows easy trade off between hardware cost and system performance. Communication over the microSD bus is based on command and data bit stream initiated by a start bit and terminated by stop bit.

Command:

Commands are transferred serially on the CMD line. A command is a token to starts an operation from host to the card. Commands are sent to a addressed single card(addressed Command) or to all connected cards (Broad cast command).

Response:

Responses are transferred serially on the CMD line. A response is a token to answer to a previous received command. Responses are sent from a addressed single card or from all connected cards.

Data:

Data can be transfer from the card to the host or vice versa.
Data is transferred via the data lines.

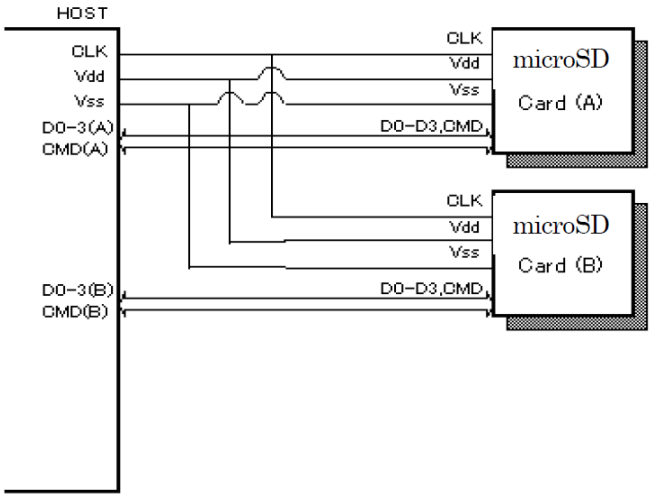

Figure 2: microSD Card (SD Mode) Connection Diagram

CLK: Host Card Clock Signal
CMD: Bi-Directional Command/Response Signal
DAT0-DAT3: 4 Bi-Directional Data Signal
V_{DD}: Power Supply
V_{SS}: GND

Table 3: SD Mode Command Set

(+: Implemented, -: Not Implemented)

CMD Index	Abbreviation	Implementation	Notes
CMD0	GO_IDLE_STATE	+	
CMD2	ALL_SEND_CID	+	
CMD3	SEND_RELATIVE_ADDR	+	
CMD4	SET_DSR	-	DSR Register is not implemented
CMD6	SWITCH_FUNC	+	
CMD7	SELECT/DESELECT_CARD	+	
CMD8	SEND_IF_COND	+	
CMD9	SEND_CSD	+	
CMD10	SEND_CID	+	
CMD11	VOLTAGE_SWITCH	+	
CMD12	STOP_TRANSMISSION	+	
CMD13	SEND_STATUS	+	
CMD15	GO_INACTIVE_STATE	+	
CMD16	SET_BLOCKLEN	+	
CMD17	READ_SINGLE_BLOCK	+	
CMD18	READ_MULTIPLE_BLOCK	+	
CMD19	READ_MULTIPLE_BLOCK	+	
CMD20	SPEED_CLASS_CONTROL	+	For SDHC/SDXC
CMD23	SET_BLOCK_COUNT	+	For UHS104 (CMD23 does not support)
CMD24	WRITE_BLOCK	+	
CMD25	WRITE_MULTIPLE_BLOCK	+	
CMD27	PROGRAM_CSD	+	
CMD28	SET_WRITE_PROT	-	Internal Write Protection is not implemented.
CMD29	CLR_WRITE_PROT	-	Internal Write Protection is not implemented.
CMD30	SEND_WRITE_PROT	-	Internal Write Protection is not implemented.
CMD32	ERASE_WR_BLK_START	+	
CMD33	ERASE_WR_BLK_END	+	
CMD38	ERASE	+	
CMD42	LOCK_UNLOCK	+	
CMD55	APP_CMD	+	
CMD56	GEN_CMD	-	This command is not specified
ACMD6	SET_BUS_WIDTH	+	
ACMD13	SD_STATUS	+	
ACMD22	SEND_NUM_WR_BLOCKS	+	
ACMD23	SET_WR_BLK_ERASE_COUNT	+	
ACMD41	SD_APP_OP_COND	+	
ACMD42	SET_CLR_CARD_DETECT	+	
ACMD51	SEND_SCR	+	
ACMD18	SECURE_READ_MULTI_BLOCK	-	
ACMD25	SECURE_WRITE_MULTI_BLOCK	-	
ACMD26	SECURE_WRITE_MKB	-	
ACMD38	SECURE_ERASE	-	
ACMD43	GET_MKB	-	
ACMD44	GET_MID	+	
ACMD45	SET_CER_RN1	-	
ACMD46	SET_CER_RN2	-	
ACMD47	SET_CER_RES2	-	
ACMD48	SET_CER_RES1	-	
ACMD49	CHANGE_SECURE_AREA	-	

- CMD28, 29 and CMD30 are Optional Commands.
- CMD4 is not implemented because DSR Register(Optional Register)
- CMD56 is for vendor specific command. Which is not defined in the standard card.

6.2.2 SPI Bus mode Protocol

The SPI bus allows 1 bit Data line by 2-chanel (Data In and Out).
The SPI compatible mode allows the MMC Host systems to use SD card with little change.
The SPI bus mode protocol is byte transfers.
All the data token are multiples of the bytes (8-bit) and always byte aligned to the CS signal.
The advantage of the SPI mode is reducing the host design in effort.
Especially, MMC host can be modified with little change.
The disadvantage of the SPI mode is the loss of performance versus SD mode.
Caution: Please use SD Card Specification. DO NOT use MMC Specification.
For example, initialization is achieved by ACMD41, and be careful with Registers.
Registers definition are different, especially CSD Register.

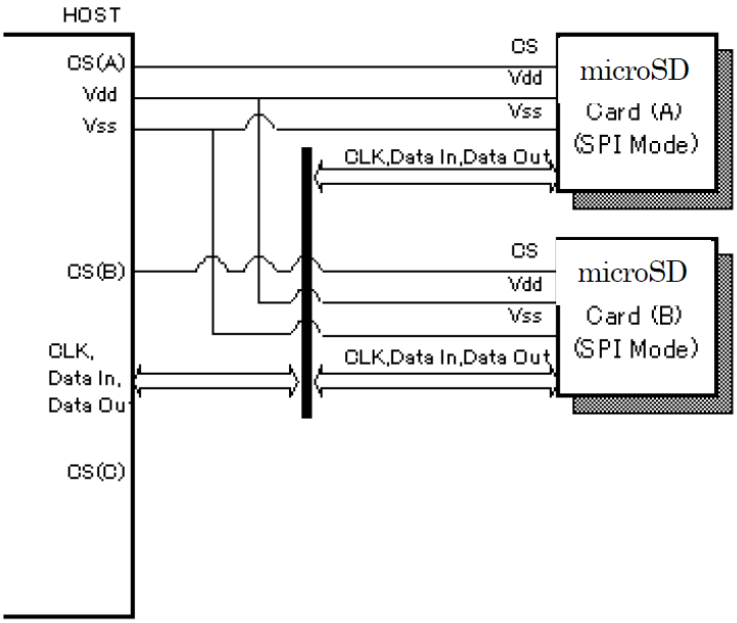

Figure 3: microSD Card(SPI Mode) Connection Diagram

CS: Card Select Signal
CLK: Host Card Clock Signal
Data In: Host to Card Data Line
Data Out: Card to Host Data Line
V_{DD}: Power Supply
V_{SS}: GND

Table.4: SPI Mode Command Set

(+: Implemented, -: Not Implemented)

CMD Index	Abbreviation	Implementation	Notes
CMD0	GO_IDLE_STATE	+	
CMD1	SEND_OP_CND	+	NOTICE: DO NOT USE (SEE Fig.6 and 9.2)
CMD6	SWITCH_FUNC	+	
CMD8	SEND_IF_COND	+	
CMD9	SEND_CSD	+	
CMD10	SEND_CID	+	
CMD12	STOP_TRANSMISSION	+	
CMD13	SEND_STATUS	+	
CMD16	SET_BLOCKLEN	+	
CMD17	READ_SINGLE_BLOCK	+	
CMD18	READ_MULTIPLE_BLOCK	+	
CMD24	WRITE_BLOCK	+	
CMD25	WRITE_MULTIPLE_BLOCK	+	
CMD27	PROGRAM_CSD	+	
CMD28	SET_WRITE_PROT	-	Internal Write Protection is not implemented.
CMD29	CLR_WRITE_PROT	-	Internal Write Protection is not implemented.
CMD30	SEND_WRITE_PROT	-	Internal Write Protection is not implemented.
CMD32	ERASE_WR_BLK_START_ADDR	+	
CMD33	ERASE_WR_BLK_END_ADDR	+	
CMD38	ERASE	+	
CMD42	LOCK_UNLOCK	+	
CMD55	APP_CMD	+	
CMD56	GEN_CMD	-	This command is not specified
CMD58	READ_OCR	+	
CMD59	CRC_ON_OFF	+	
ACMD6	SET_BUS_WIDTH	+	
ACMD13	SD_STATUS	+	
ACMD22	SEND_NUM_WR_BLOCKS	+	
ACMD23	SET_WR_BLK_ERASE_COUNT	+	
ACMD41	SD_APP_OP_COND	+	
ACMD42	SET_CLR_CARD_DETECT	+	
ACMD51	SEND_SCR	+	
ACMD18	SECURE_READ_MULTI_BLOCK	-	
ACMD25	SECURE_WRITE_MULTI_BLOCK	-	
ACMD26	SECURE_WRITE_MKB	-	
ACMD38	SECURE_ERASE	-	
ACMD43	GET_MKB	-	
ACMD44	GET_MID	+	
ACMD45	SET_CER_RN1	-	
ACMD46	SET_CER_RN2	-	
ACMD47	SET_CER_RES2	-	
ACMD48	SET_CER_RES1	-	
ACMD49	CHANGE_SECURE_AREA	-	

- CMD28, 29 and CMD30 are Optional Commends.
- CMD56 is for vendor specific command. Which is not defined in the standard card.

6.3. microSD Card Initialize

Fig.4-1 shows initialization flow chart for UHS-I hosts and Fig.4-2 shows sequence of commands to perform signal voltage switch. Red and yellow boxes are new procedure to initialize UHS-I card.

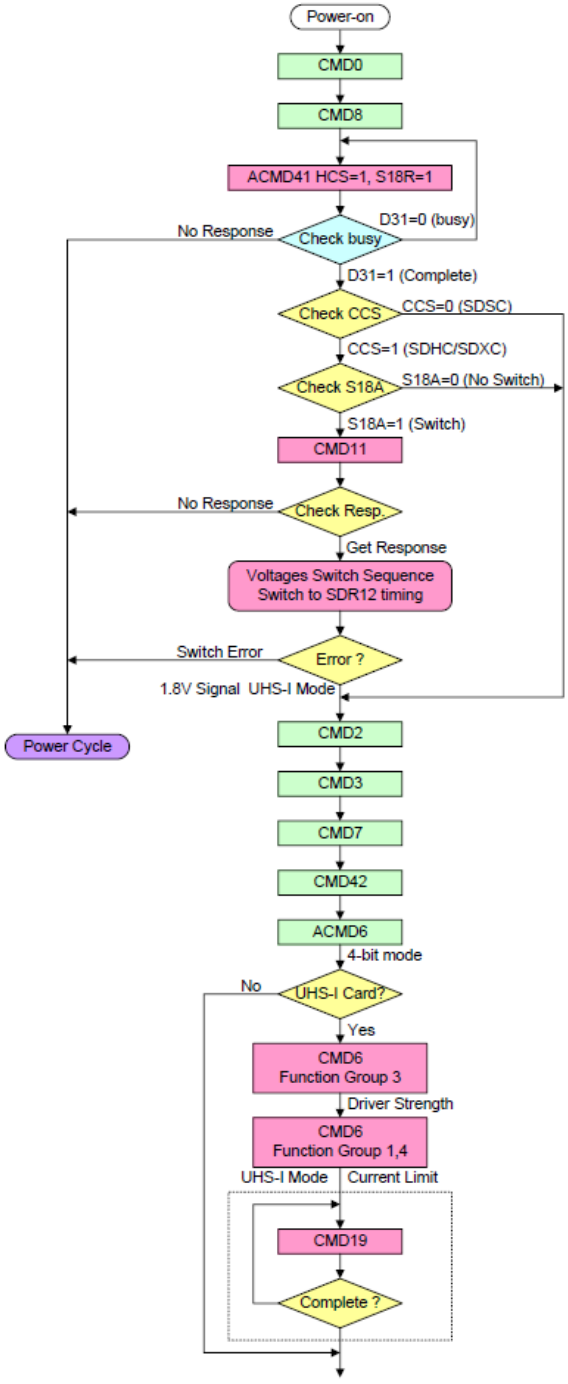

Figure 4-1: UHS-I Host Initialization Flow Diagram

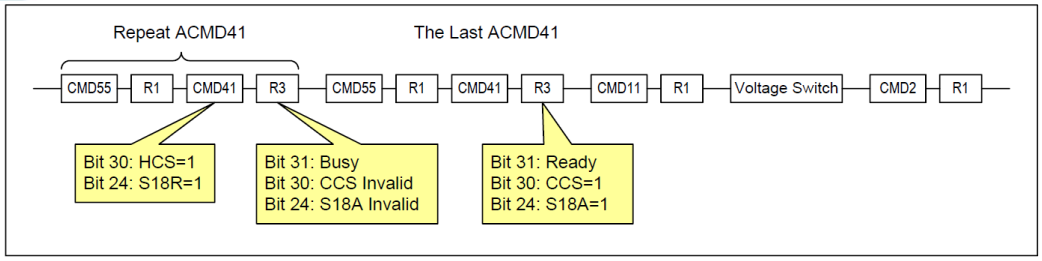

Figure 4-2: ACMD41 Timing Followed by Signal Voltage Switch Sequence

1) POWER ON：Supply Voltage for initialization.
Host System applies the Operating Voltage to the card.
Apply more than 74 cycles of Dummy-clock to the microSD card.
2) Select operation mode (SD mode or SPI mode)
In case of SPI mode operation, host should drive 1 pin (CD/DAT3) of SD Card I/F to "Low" level. Then, issue CMD0.
In case of SD mode operation, host should drive or detect 1 pin of SD Card I/F (Pull up register of 1 pin is pull up to "High" normally).
Card maintain selected operation mode except re-issue of CMD0 or power on below is SD mode initialization procedure.
3) Send Interface condition command (CMD8).
When the card is in Idle state, the host shall issue CMD8 before ACMD41.
In the argument, 'voltage supplied' is set to the host supply voltage and 'check pattern' is set to any 8-bit pattern.
The card that accepted the supplied voltage returns R7 response.
In the response, the card echoes back both the voltage range and check pattern set in the argument.
If the card does not support the host supply voltage, it shall not return response and stays in Idle state.
4) Send initialization command (ACMD41).
When signaling level is 3.3V, host repeats to issue ACMD41 with HCS=1 and S18R=1 until the response indicates ready.
The argument (HCS and S18R) of the first ACMD41 is effective but the all following ACMD41 should be issued with the same argument.
If Bit 31 indicates ready, host needs to check CCS and S18A.
The card indicates S18A=0, which means that voltage switch is not allowed and the host needs to use current signaling level.

Table 5: S18R and S18A Combinations

Current Signaling Level	18R	S18A	Comment
3.3V	0	0	1.8V signaling is not requested
	1	0	The card does not support 1.8V signaling
	1	1	Start signal voltage switch sequence
1.8V	X	0	Already switched to 1.8V

5) Send voltage switch command (CMD11).

S18A=1 means that voltage switch is allowed and host issues CMD11 to invoke voltage switch sequence.

By receiving CMD11, the card returns R1 response and start voltage switch sequence.

No response of CMD11 means that S18A was 0 and therefore host should not have sent CMD11.

Completion of voltage switch sequence is checked by high level of DAT[3:0].

Any bit of DAT[3:0] can be checked depends on ability of the host.

The card enters UHS-I mode and card input and output timings are changed (SDR12 in default) when the voltage switch sequence is completed successfully.

6) Send ALL_SEND_CID command (CMD2) and get the Card ID (CID).

7) Send SEND_RELATIVE_ADDR (CMD3) and get the RCA.

RCA value is randomly changed by access, not equal zero.

8) Send SELECT / DESELECT_CARD command (CMD7) and move to the transfer state.

When entering tran state, CARD_IS_LOCKED status in the R1 response should be checked (it is indicated in the response of CMD7).

If the CARD_IS_LOCKED status is set to 1 in the response of CMD7, CMD42 is required before ACMD6 to unlock the card.

(If the card is locked, CMD42 is required to unlock the card.)

If the card is unlocked, CMD42 can be skipped.

9) Send SET_BUS_WIDTH command (ACMD6).

UHS-I supports only 4-bit mode. Host shall select 4-bit mode by ACMD6.

If the card is locked, host needs to unlock the card by CMD42 in 1-bit mode and then needs to issue ACMD6 to change

4-bit bus mode. Operating in 1-bit mode is not assured.

10) Set driver strength.

CMD6 mode 0 is used to query which functions the card supports, and to identify the maximum current consumption of the card under the selected functions.

In case of UHS-I card, appropriate driver strength (default is Type-B buffer) is selected by CMD6 Function Group 3.

11) Set UHS-I mode current limit.

UHS-I modes (Bus Speed Mode) is selected by CMD6 Function Group 1.

Current Limit is selected by CMD6 Function Group 4.

Maximum access settings:

SDR50 = (CMD6 Function Group 1 = 2-h, CMD6 Function Group 4 = 1-h)

Note:

Function Group 4 is defined as Current Limit switch for SDR50.

The Current Limit does not act on the card in SDR12 and SDR25.

The default value of the Current Limit is 200mA (minimum setting).

Then after selecting one of SDR50 mode by Function Group 1, host needs to change the Current Limit to enable the card to operate in higher performance.

This value is determined by a host power supply capability to the card, heat release method taken by a host and the maximum current of a connector.

12) Tuning of sampling point

CMD19 sends a tuning block to the host to determine sampling point.
In SDR50 and SDR104 modes, if tuning of sampling point is required, CMD19 is repeatedly issued until tuning is completed
Then the Host can access the Data between the SD card as a storage device.

6.4. microSD card Electrical Characteristics

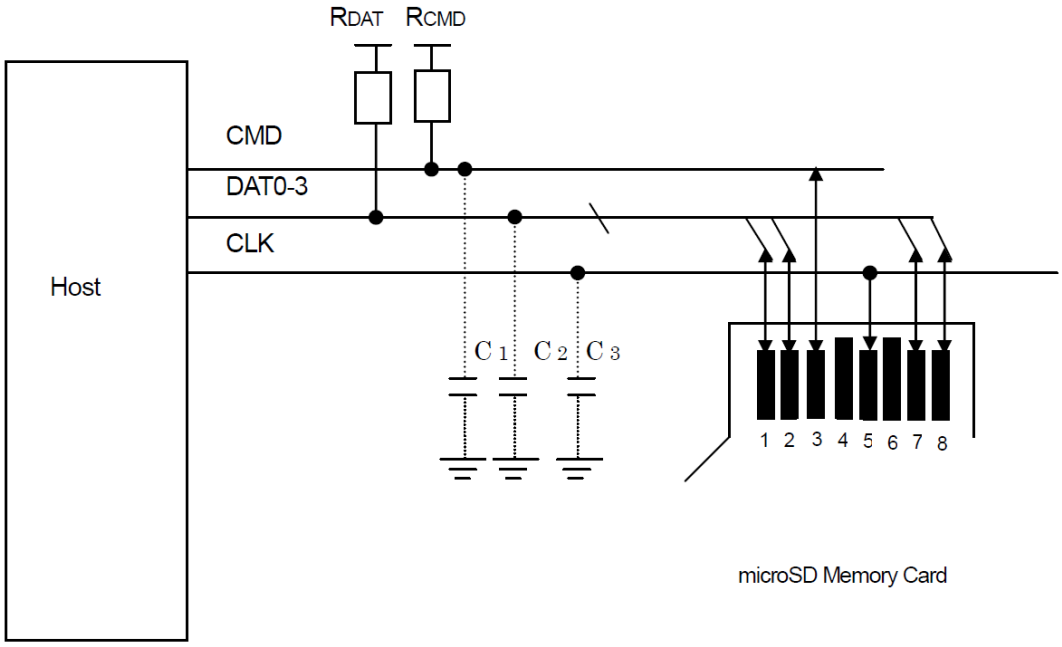

Figure 5: microSD Card Connection Diagram

6.4.1 DC Characteristics

Table 6-1: DC Characteristics (Threshold level for High Voltage Range)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Supply Voltage		V_{DD}	-	2.7	-	3.6	V	
Input Voltage	High Level	V_{IH}	-	V_{DD}*0.625	-	-	V	
	Low Level	V_{IL}	-	-	-	V_{DD}*0.25	V	
Output Voltage	High Level	V_{OH}	I_{OH} = -2mA	V_{DD}*0.75	-	-	V	
	Low Level	V_{OL}	I_{OL} = 2mA	-	-	V_{DD}*0.125	V	
Power Up Time			-	-	-	250	ms	0V to V_{DD} min

*) Peak Current: RMS value over a 10 usec period

Table 6-2: Peak Voltage and Leakage Current

Parameter	Symbol	Min.	Max.	Unit	Note
Peak Voltage on All Lines		-0.3	V_{DD}+0.3	V	
All Inputs					
Input Leakage Current		-10	10	uA	
All Outputs					
Output Leakage Current		-10	10	uA	

Table 6-3: DC Characteristics (Threshold Level for 1.8V Signaling)

Item		Symbol	Min.	Max.	Unit	Condition
Supply Voltage		V_{DD}	2.7	3.6	V	
Regulator Voltage		V_{DDIO}	1.7	1.95	V	Generated from V_{DD}
Input Voltage	High Level	V_{IH}	1.27	2.00	V	
	Low Level	V_{IL}	V_{SS}-0.3	0.58	V	
Output Voltage	High Level	V_{OH}	1.4	-	V	
	Low Level	V_{OL}	-	0.45	V	

Table 6-4: Input Leakage Current for 1.8V Signaling

Parameter	Symbol	Min.	Max.	Unit	Note
Input Leakage Current		-2	2	uA	DAT3 Pull-Up is Disconnected

Table 6-5: Power Consumption

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Standby Current	I_{CCS}	3.0V Clock Stop	-	-	1350	uA	@ 25°C
Operation Current(Peak)	I_{CCOP1} *1)	Current Limit=400mA V_{DD}=3.6V	-	-	300	mA	@ 25°C
		Current Limit=200mA V_{DD}=3.6V	-	-	300		
		(HS or DS) V_{DD}=3.6V	-	-	300		
Operation Current(Average)	I_{CCOP2} *2)	Current Limit=400mA V_{DD}=3.6V	-	-	250	mA	@ 25°C
		Current Limit=200mA V_{DD}=3.6V	-	-	200		
		(SDR25 or HS) V_{DD}=3.6V	-	-	200		
		(SDR12.5 or DS) V_{DD}=3.6V	-	-	100		

*1) Peak Current: RMS value over a 10usec period
*2) Average Current: value over 1 sec period.

Table 6-6: Signal Capacitance

Total Bus Capacitance = C_{HOST} + C_{BUS} + N*C_{Card}

Item	Symbol	Min.	Max.	Unit	Note
Pull-Up Resistance	R_{CMD} R_{DAT}	10	100	K Ohm	
Total Bus Capacitance for Each Signal Line	C_L	-	40	pF	1 Card C_{HOST}+C_{BUS} Shall Not Exceed 30pF
Card Capacitance for Each Signal Pin	C_{CARD}	-	10	pF	
Maximum Signal Line Inductance		-	16	nH	
Pull-Up Resistance Inside Card(Pin 1)	R_{DAT3}	10	90	K Ohm	May Be Used for Card Detection
Capacity Connected to Power Line	C_C	-	5	uF	To Prevent Inrush Current

Note: WP pull-up (R_{wp}) Value is depend on the Host Interface drive circuit.

6.4.2 AC Characteristics (Default)

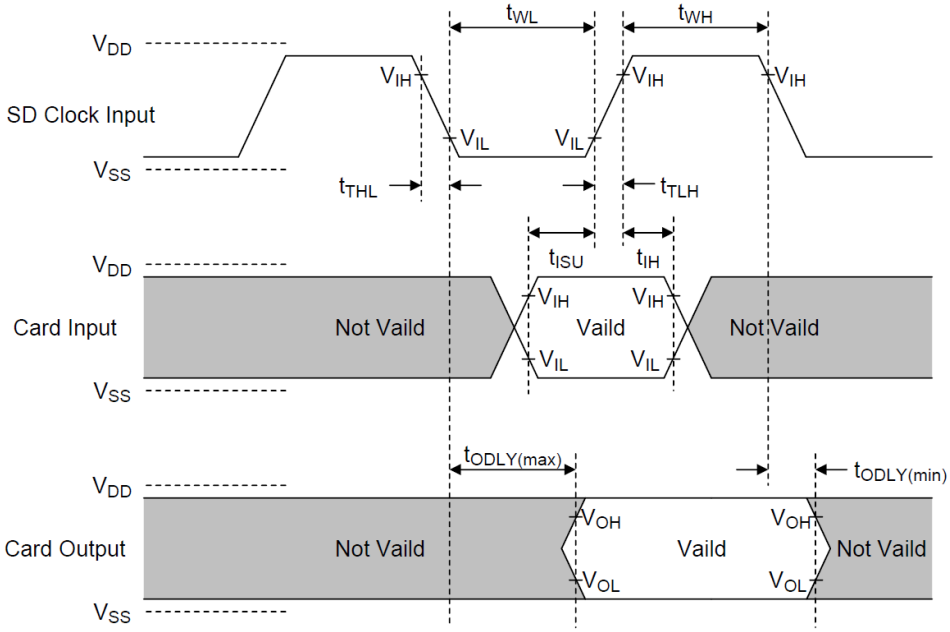

Figure 6-1: AC Timing Diagram (Default)

Table 7-1: AC Characteristics (Default)

Item	Symbol	Min.	Max.	Unit	Note
Clock Frequency (In Any State)	f_{STP}	0	25	MHz	$C_{CARD} \leq 10pF$ (1 Card)
Clock Frequency (Data Transfer Mode)	f_{PP}	0	25	MHz	
Clock Frequency (Card Identification Mode)	f_{OD}	0/100(*1)	400	KHz	
Clock Low Time	t_{WL}	10	-	ns	
Clock High Time	t_{WH}	10	-	ns	
Clock Rise Time	t_{TLH}	-	10	ns	
Clock Fall Time	t_{THL}	-	10	ns	
Input Set-up Time	t_{ISU}	5	-	ns	
Input Hold Time	t_{IH}	5	-	ns	
Output Delay Time (Data Transfer Mode)	t_{ODLY}	0	14	ns	$C_L \leq 40pF$ (1 Card)
Output Delay Time (Identification Mode)	t_{ODLY}	0	50	ns	

(*1) 0Hz means to stop the clock. The given minimum frequency range is for cases were continues clock is required.

6.4.4 AC Characteristics (High-Speed)

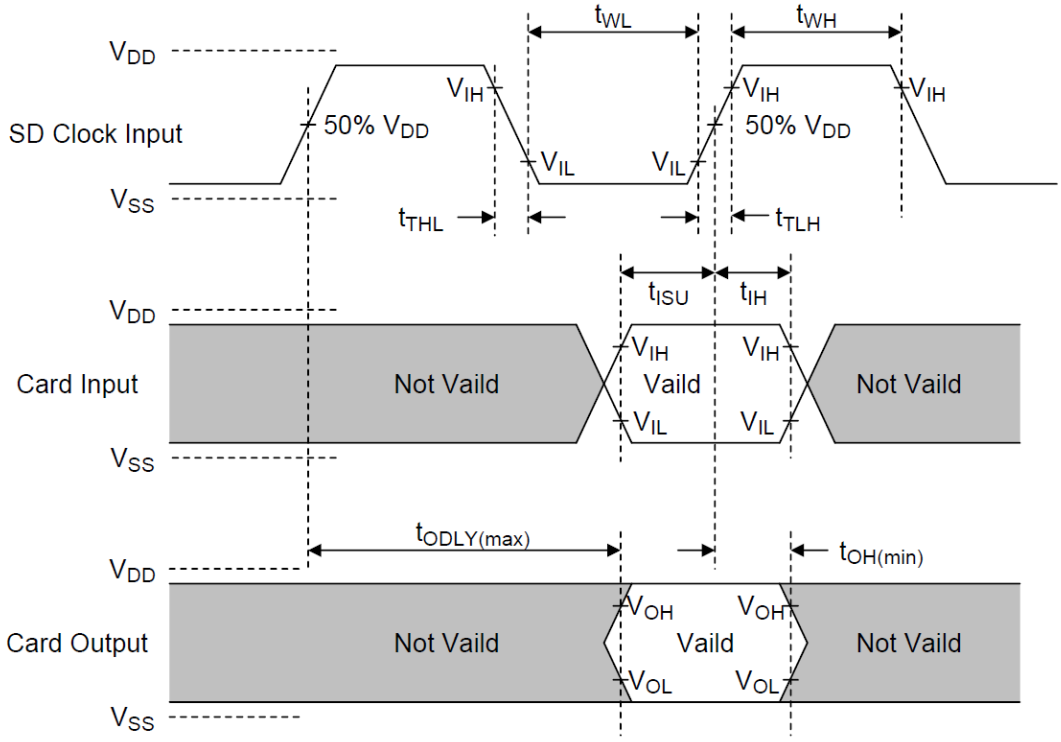

Figure 6-2: AC Timing Diagram (High-Speed)

Table 7-2: AC Characteristics (High-Speed)

Item	Symbol	Min.	Max.	Unit	Note
Clock Frequency (Data Transfer Mode)	f_{PP}	0	50	MHz	C_{CARD} ≤ 10pF (1 Card)
Clock Low Time	t_{WL}	7	-	ns	C_{CARD} ≤ 10pF (1 Card)
Clock High Time	t_{WH}	7	-	ns	C_{CARD} ≤ 10pF (1 Card)
Clock Rise Time	t_{TLH}	-	3	ns	C_{CARD} ≤ 10pF (1 Card)
Clock Fall Time	t_{THL}	-	3	ns	C_{CARD} ≤ 10pF (1 Card)
Input Set-up Time	t_{ISU}	6	-	ns	C_{CARD} ≤ 10pF (1 Card)
Input Hold Time	t_{IH}	2	-	ns	C_{CARD} ≤ 10pF (1 Card)
Output Delay Time (Data Transfer Mode)	t_{ODLY}	-	14	ns	C_{CARD} ≤ 10pF (1 Card)
Output Hold Time	T_{OH}	2.5	-	ns	C_{CARD} ≤ 10pF (1 Card)
Total System Capacitance	C_L	-	40	pF	C_{CARD}≤10pF (1 Card)

6.4.5 AC Characteristics (SDR12, SDR25, SDR50, and SDR104 Modes)

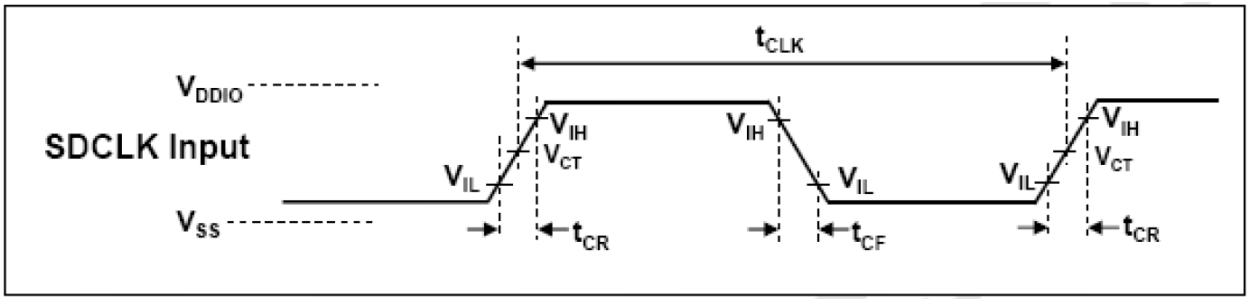

Figure 6-3: AC Timing Diagram (SDR12, SDR25, SDR50, and SDR104 Modes Input)

Table 7-3: AC Characteristics (SDR12, SDR25, SDR50, and SDR104 Modes Input)

Symbol	Min.	Max.	Unit	Remark
t_{CLK}	4.80	-	ns	208MHz(Max.), between rising edge, V_{CT}=0.975V
t_{CR}, t_{CF}	-	0.2*t_{CLK}	ns	t_{CR}, t_{CF} < 0.96ns(Max.) at 208MHz, C_{CARD} = 10pF t_{CR}, t_{CF} < 2.00ns(Max.) at 100MHz, C_{CARD} = 10pF The absolute maximum value of t_{CR}, t_{CF} is 10ns regardless of clock frequency.
Clock Duty	30	70	%	

Appendix: microSD Card Mechanical Dimensions (Unit : mm)