Application Report
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Loop Response Considerations in Peak Current Mode Buck Converter Design

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ABSTRACT

The internal loop compensated Peak Current Mode (PCM) buck converter is popular. The loop response is good for normal inductor and output capacitor design, but improper inductor and output capacitor values can lead to instability or bad transient performance. This application report details the PCM buck converter, analyzes the stability constraint, and provides a simple equation to calculate bandwidth and phase margin of the converter.

The model proposed in this application report is introduced in Section 1. Section 2 provides peak current mode loop modeling. The inside current loop is simplified as a single pole. The overall loop response transfer function is obtained. The inductor and output capacitor design limits are derived considering loop response. At the end of this section, the equation to calculate bandwidth and phase margin is provided. In Section 3, the inductor and output capacitor is designed step-by-step considering loop response. The theory is verified by simulation and bench measurement results.

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1 Introduction

The TPS560430 regulator is an easy-to-use synchronous step-down DC/DC converter operating from 4-V to 36-V supply voltage. It is capable of delivering up to 600-mA DC load current in a very small solution size. The family has different versions applicable for different applications, 1.1-MHz and 2.1-MHz switching frequency, PFM and FPWM, adjustable and fixed output voltage. The device is suitable for a wide range of applications from industrial to automotive for power conditioning from an unregulated source. The TPS560430 employs peak-current mode control with internal loop compensation, which reduces design time, and requires few external components.

A lot of PCM loop models are available for system design. The most popular model is provided in [2]. The model predicted the sample and hold effects in the current loop, while using a three-terminal switch model to calculate power stage small signal model. Using this method, a simplified loop model is provided in [3], and an equivalent circuit is obtained to simulate the loop response. However, if all of the models require simulation tools to draw the bode plot, then find a crossover frequency and phase margin based on the bode plot. Besides, the transfer function of inner current loop is quite complex, making it hard to understand how it impacts the whole loop response. In this document, a simple equation is provided to calculate bandwidth. The phase margin is obtained by simplifying the inside current loop as a single pole. The inner current loop stability criteria can be obtained based on the model. Each zero and pole in the model has a clear physical meaning, making it easy to analyze the impact of each component value on the loop response. The inductor and output capacitor design procedure of the internally compensated PCM buck converter is given using the model. The model accuracy is verified by both simulation and bench measurement results.

2 Peak Current Mode Loop Modeling

2.1 Overall Control Block Diagram and Transfer Function Derivation

Figure 1 shows the simplified schematic for the PCM buck converter.

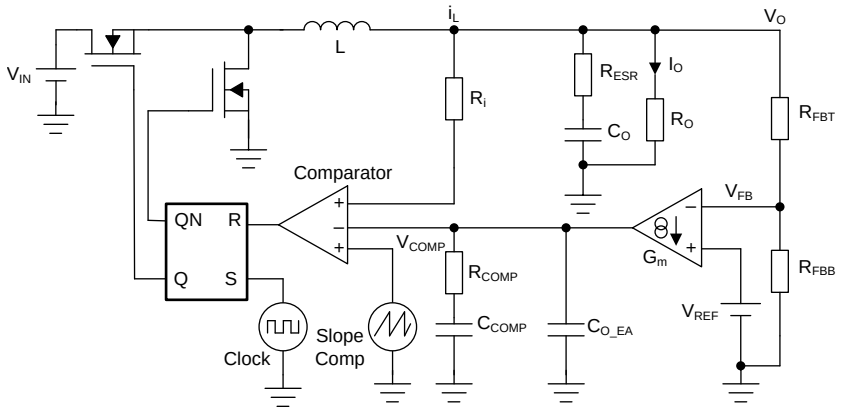

Figure 1. Simplified Schematic for PCM Buck Converter

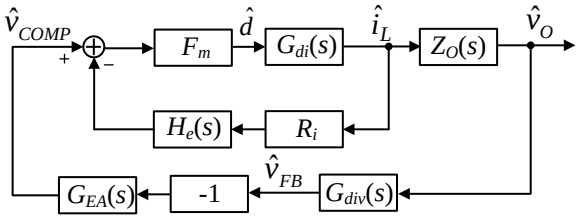

Figure 2. Overall Control Implementation

Figure 2 shows the overall control block model where:

- $G_{di}(s)$ is the duty cycle to i_L transfer function.
- $Z_O(s)$ is the transfer function of output impedance.
- $G_{div}(s)$ is the gain of the feedback resistor network.
- $G_{EA}(s)$ is the transfer function of the error amplifier with certain compensation.
- F_m is the gain of PCM PWM comparator.
- R_i is the current sensing resistor.
- $H_e(s)$ is the transfer function model of inductor current sampling-hold effect.

Equation 1 shows the transfer function from the inductor current to the output voltage.

$$Z_O(s) = \frac{\hat{v}_O(s)}{\hat{i}_L(s)} = R_O \frac{1 + sR_{ESR}C_O}{1 + s(R_{ESR} + R_O)C_O} \quad (1)$$

$G_{di}(s)$ is the duty cycle to i_L transfer function.

$$G_{di}(s) = \frac{\hat{i}_L(s)}{\hat{d}(s)} = \frac{V_{IN}(1 + sC_OR_O)}{R_O + sL + s^2LC_OR_O} \quad (2)$$

The internal loop compensation is designed so that the crossover frequency is much higher than the corner frequency, $1/(2\pi\sqrt{LC_O})$. For crossover frequency and higher frequency, Equation 2 can be simplified as Equation 3.

$$G_{di}(s) = \frac{\hat{i}_L(s)}{\hat{d}(s)} \approx \frac{V_{IN}}{sL} \quad (3)$$

The sensed inductor current, external ramp, and the output of error amplifier V_{COMP} are compared, which determines when to turn off the high side MOSFET, hence the duty cycle is determined. F_m is the comparator gain. f_{SW} is the switching frequency. S_n is the on-time slope of the sensed-current waveform and S_e is the external ramp slope.

$$F_m = \frac{f_{SW}}{S_n + S_e}$$

where

$$S_n = R_i \frac{V_{IN} - V_O}{L}$$

$$S_e = V_{Se} \times f_{SW} \quad (4)$$

$H_e(s)$ is the transfer function model of inductor current sampling-hold effect. [2]:

$$H_e(s) = \frac{s/f_{SW}}{e^{s/f_{SW}} - 1} \approx 1 - \frac{s}{2f_{SW}} + \frac{s^2}{(\pi f_{SW})^2} \quad (5)$$

Equation 6 shows the transfer function of the feedback.

$$G_{div}(s) = \frac{\hat{v}_{FB}(s)}{\hat{v}_O(s)} = \frac{V_{REF}}{V_O} \tag{6}$$

Equation 7 shows the transfer function of the error amplifier with certain compensation.

$$G_{EA}(s) = \frac{\hat{v}_{COMP}(s)}{-\hat{v}_{FB}(s)} = \frac{G_m}{C_{COMP}} \frac{1 + sR_{COMP}C_{COMP}}{s\left(1 + sR_{COMP}C_{O\_EA}\right)} \tag{7}$$

2.2 Inside Current Loop Model

Based on Equation 3 to Equation 5 and Figure 2, the transfer function from control to inductor current is $G_{ci}(s)$:

$$G_{ci}(s) = \frac{\hat{i}_L(s)}{\hat{v}_{COMP}(s)} = \frac{1}{R_i} \frac{1}{1 + s \times \left[\frac{V_{Se}f_{SW}L + \left(0.5V_{IN} - V_O\right)R_i}{V_{IN}R_i f_{SW}}\right] + s^2 \times \frac{1}{\left(\pi f_{SW}\right)^2}} \tag{8}$$

For PCM buck converter, the crossover frequency is much smaller than half switching frequency, so around crossover frequency Equation 8 can be simplified as Equation 9. The inside current loop is simplified as a single pole, which is very helpful for the loop response analysis of PCM buck converter.

$$G_{ci}(s) = \frac{\hat{i}_L(s)}{\hat{v}_{COMP}(s)} = \frac{1}{R_i} \frac{1}{1 + s \times \left[\frac{V_{Se}f_{SW}L + \left(0.5V_{IN} - V_O\right)R_i}{V_{IN}R_i f_{SW}}\right]} \tag{9}$$

If the inside current loop $G_{ci}(s)$ is not stable, subharmonic oscillation occurs. A system is stable as long as each of the poles of the closed loop transfer function lies in the left half plane. The minimum inductor value is calculated to prevent subharmonic oscillation:

$$L > \frac{R_i\left(V_O - 0.5V_{IN}\right)}{V_{Se}f_{SW}} \tag{10}$$

2.3 Overall Loop Model

f_{Z_EA} and f_{P_EA} are zeros and poles introduced by the error amplifier with certain compensation. f_{Z_OUT} and f_{P_OUT} are zeros and poles introduced by the output capacitor and load. f_{P_ci} is the pole introduced by the inside current loop. Based on Equation 1, Equation 6, Equation 7, and Equation 9, the open loop transfer function L(s) around crossover frequency is obtained:

$$L(s) = Z_O(s) \times G_{div}(s) \times G_{EA}(s) \times G_{ci}(s) = K \frac{\left(1 + \frac{s}{2\pi f_{Z\_EA}}\right) \times \left(1 + \frac{s}{2\pi f_{Z\_OUT}}\right)}{s \times \left(1 + \frac{s}{2\pi f_{P\_EA}}\right) \times \left(1 + \frac{s}{2\pi f_{P\_ci}}\right) \times \left(1 + \frac{s}{2\pi f_{P\_OUT}}\right)}$$

where

$$K = \frac{R_O V_{REF} G_m}{R_i V_O C_{COMP}}$$

$$f_{Z\_EA} = \frac{1}{2\pi R_{COMP} C_{COMP}}$$

$$f_{P\_EA} = \frac{1}{2\pi R_{COMP} C_{O\_EA}}$$

$$f_{P\_ci} = \frac{V_{IN} R_i f_{SW}}{2\pi \left[V_{Se} f_{SW} L + \left(0.5 V_{IN} - V_O\right) R_i \right]}$$

$$f_{Z\_OUT} = \frac{1}{2\pi R_{ESR} C_O}$$

$$f_{P\_OUT} = \frac{1}{2\pi \left(R_{ESR} + R_O\right) C_O} \tag{11}$$

2.4 Inductor and Output Capacitor Design Limits

Figure 3 shows the Bode plot with proper inductor and output capacitor design. $f_c \gg f_{P\_OUT}$, $f_c \gg f_{Z\_EA}$, $f_c \ll f_{P\_EA}$, $f_c \ll f_{P\_ci}$, $f_c \ll f_{Z\_OUT}$

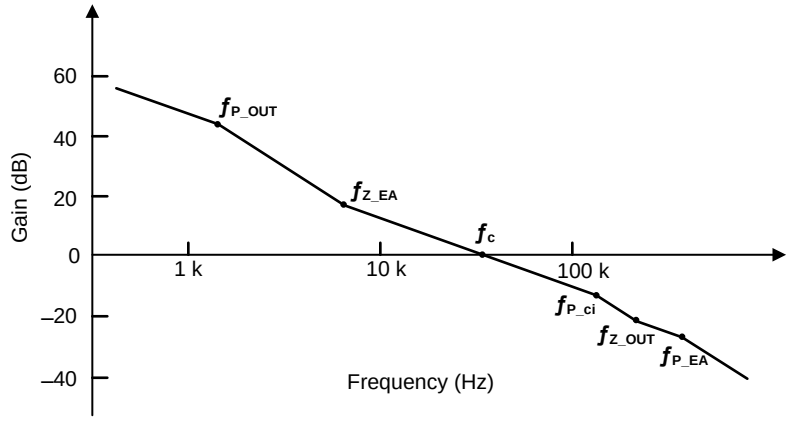

Figure 3. Bode Plot Model for PCM Buck Converter

The gain curve must go across 0 dB with a -20 dB/dec slew rate, so that the phase margin is enough. The zero introduced by the compensation network f_{Z_EA} cancels the pole of output impedance f_{P_OUT}, and they are placed far before crossover frequency: $f_{P\_OUT} \ll f_c$, $f_{Z\_EA} \ll f_c$. The parasitic capacitor of error amplifier C_{O_EA} is quite small, so $f_{P\_EA} \gg f_c$.

If L is too large, the pole introduced by the current loop f_{P_ci} is smaller than the crossover frequency f_c. The gain curve goes across 0 dB with a -40 dB/dec slew rate, and the phase margin is not enough. Besides, the loop response is influenced by V_{IN} since f_{P_ci} is influenced by V_{IN}. To prevent that from happening, L must be properly designed to ensure $f_{P\_ci} \gg f_c$. Equation 12 calculates the maximum inductor value.

$$L << \frac{V_{IN} R_i}{2\pi f_C V_{Se}} + \frac{R_i \left(V_O - 0.5 V_{IN}\right)}{V_{Se} f_{SW}} \tag{12}$$

If the Equivalent Series Resistance (ESR) of output capacitor is too large, the zero introduced by the output capacitor f_{Z_OUT} is smaller than the crossover frequency f_c. The gain curve has a 0 dB/dec slew rate after f_{Z_OUT}, which makes the crossover frequency too large. Some high frequency poles introduced by the parasitic parameters in the IC influence the phase margin, and the phase margin is not enough. To prevent that, ESR of the output capacitor must be properly designed to ensure $f_{Z\_OUT} \gg f_c$. Equation 13 calculates the maximum ESR.

$$R_{ESR} << \frac{1}{2\pi f_C C_O} \tag{13}$$

2.5 The Equation to Calculate Bandwidth and Phase Margin

From Equation 11 and considering $f_c \gg f_{P\_OUT}$, $f_c \gg f_{Z\_EA}$, $f_c \ll f_{P\_EA}$, $f_c \ll f_{P\_ci}$, and $f_c \ll f_{Z\_OUT}$, the magnitude of open loop transfer function at crossover frequency f_c is shown in Equation 14.

$$\left|L\left(j2\pi f_C\right)\right| = K \frac{\left|1 + j\frac{f_C}{f_{Z\_EA}}\right| \times \left|1 + j\frac{f_C}{f_{Z\_OUT}}\right|}{2\pi f_c \times \left|1 + j\frac{f_C}{f_{P\_EA}}\right| \times \left|1 + j\frac{f_C}{f_{P\_ci}}\right| \times \left|1 + j\frac{f_C}{f_{P\_OUT}}\right|} \approx K \times \frac{\frac{f_C}{f_{Z\_EA}}}{2\pi f_c \times \frac{f_C}{f_{P\_OUT}}} = 1 \tag{14}$$

Considering $R_{ESR} \ll R_O$, the crossover frequency f_c is obtained: Equation 15

$$f_c = \frac{V_{REF} G_m R_{COMP}}{2\pi V_O R_i C_O} \tag{15}$$

Phase margin is the phase of open loop transfer function at f_c minus -180°: Equation 16

$$\begin{aligned} &\text{PhaseMargin} \\ &= 90° - \arctan\left(2\pi f_C R_O C_O\right) \times \frac{180°}{\pi} + \arctan\left(2\pi f_C R_{COMP} C_{COMP}\right) \times \frac{180°}{\pi} \\ &- \arctan\left(2\pi f_C R_{COMP} C_{O\_EA}\right) \times \frac{180°}{\pi} - \arctan\left(\frac{2\pi f_C \left[V_{Se} f_{SW} L + \left(0.5 V_{IN} - V_O\right) R_i\right]}{V_{IN} R_i f_{SW}}\right) \times \frac{180°}{\pi} \\ &+ \arctan\left(2\pi f_C R_{ESR} C_O\right) \times \frac{180°}{\pi} \end{aligned} \tag{16}$$

3 Inductor and Output Capacitor Design

In this section, the inductor and output capacitor is designed in a practical application using TPS560430XF. The loop response is considered during the process. Table 1 lists the design specifications.

Table 1. Design Example Specification

V_{IN} (V)	V_O (V)	I_O (A)	I_{O_min} (A)	f_{SW} (kHz)	OUTPUT RIPPLE (mV)	V_{REF} (V)
7 V to 36 V, typical 12 V	5	0.6	0.1	1100	< 30	1

3.1 Inductor Design

Equation 17 calculates the value of the output conductor. K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current of the device. A reasonable value of K_{IND} is 0.2 – 0.4. Since the ripple current increases with the input voltage, the maximum input voltage is used to calculate the minimum inductance L_{MIN}, while K_{IND} = 0.4 is selected. The minimum inductor value is calculated to be 16.3 µH. Choose the nearest standard inductor: L= 18 µH.

$$L_{min} = \frac{V_{IN\_max} - V_O}{I_O \times K_{IND}} \times \frac{V_O}{V_{IN\_max} \times f_{SW}} \quad (17)$$

From Equation 12, the maximum inductor value is calculated to get enough phase margin. Three times margin is suggested and the limit is Equation 18 with the TPS560430 internal parameter. If you assume the target crossing over frequency f_c is about 20 kHz, then the result is L < 40 µH at the minimum V_{IN}. The selected 18-µH inductor meets the requirement.

$$L < \frac{1}{3}\left[\frac{V_{IN}}{2\pi f_c \times 0.476} + \frac{\left(V_O - 0.5V_{IN}\right)}{f_{SW} \times 0.476}\right] \quad (18)$$

The TPS560430 is protected from over-current conditions by the cycle-by-cycle current limit. To prevent inductor saturation in case of short circuit conditions, the inductor saturation current must be greater than the device maximum peak current limit, which is 1.4 A for the TPS560430.

3.2 Output Capacitor Design

The output capacitor is designed based on output ripple and loop response. The output voltage ripple is composed of two parts. One is caused by the inductor current ripple going through the ESR of the output capacitor, see Equation 19. The other is caused by the inductor current ripple charging and discharging the output capacitor, see Equation 20. The target output ripple is 30 mV, so ΔV_{O_ESR} < 30 mV and ΔV_{O_C} < 30 mV, then R_{ESR} < 125 mΩ and C_O > 0.91 µF.

$$\Delta V_{O\_ESR} = I_O \times K_{IND} \times R_{ESR} \quad (19)$$

$$\Delta V_{O\_C} = \frac{I_O \times K_{IND}}{8 \times f_{SW} \times C_O} \quad (20)$$

From Equation 13, the maximum ESR value is calculated to get a reasonable crossover frequency and enough phase margin. If you assume the target crossing over frequency f_c is about 20 kHz, then the result is $R_{ESR} \ll$ 612 mΩ. Three times margin is suggested and the result is R_{ESR} < 204 mΩ.

Output capacitor value determines loop response in internally compensated PCM buck converters, as Equation 15 and Equation 16. With TPS560430 internal parameter, the calculation equation is as Equation 21 and Equation 22. The target f_c is about 20 kHz, so C_O is about 15 µF. Consider of derating, one 22-µF, 16-V ceramic capacitor with 4-mΩ ESR is used. The capacitance after derating is 13 µF: C_O = 13 µF, R_{ESR} = 4 mΩ. The crossover frequency is f_c = 23.4 kHz and the phase margin is calculated as 64.2º at V_{IN} = 12 V, I_O = 0.6 A. The equation also indicates that the worst phase margin happens at minimum V_{IN} and minimum I_O, while the calculation result is 59.2º at V_{IN} = 7 V, I_O = 0.1 A. They meet design specs.

$$f_c = \frac{9.54}{2\pi V_O C_O} \quad (21)$$

$$\text{PhaseMargin} = 90° - \arctan\left(2\pi f_C R_O C_O\right) \times \frac{180°}{\pi} + \arctan\left(2\pi f_C \times 26.5\,\mu\right) \times \frac{180°}{\pi} - \arctan\left(2\pi f_C \times 1.06\,\mu\right) \times \frac{180°}{\pi} - \arctan\left(\frac{2\pi f_C \left(f_{SW} L \times 0.476 + 0.5 V_{IN} - V_O\right)}{V_{IN} f_{SW}}\right) \times \frac{180°}{\pi} + \arctan\left(2\pi f_C R_{ESR} C_O\right) \times \frac{180°}{\pi} \quad (22)$$

3.3 Simulation and Bench Verification

Figure 4 shows the schematic for bench verification. SIMPLIS is used to simulate the loop response as shown in Figure 5. Figure 6 and Figure 7 are the loop responses from the SIMPLIS simulation and bench test under V_{IN} = 12 V, V_O = 5 V, I_O = 0.6 A, and f_{SW} = 1.1 MHz. Table 2 compares the calculation results, simulation results, and bench measurement at different V_{IN}. It can be seen that the proposed model in this application report is accurate.

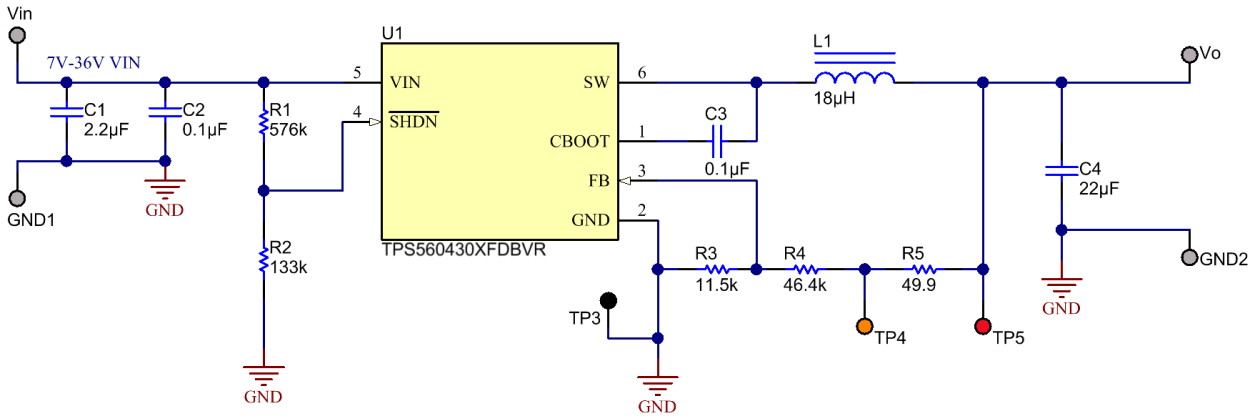

Figure 4. TPS560430XF Design With 5-V Output

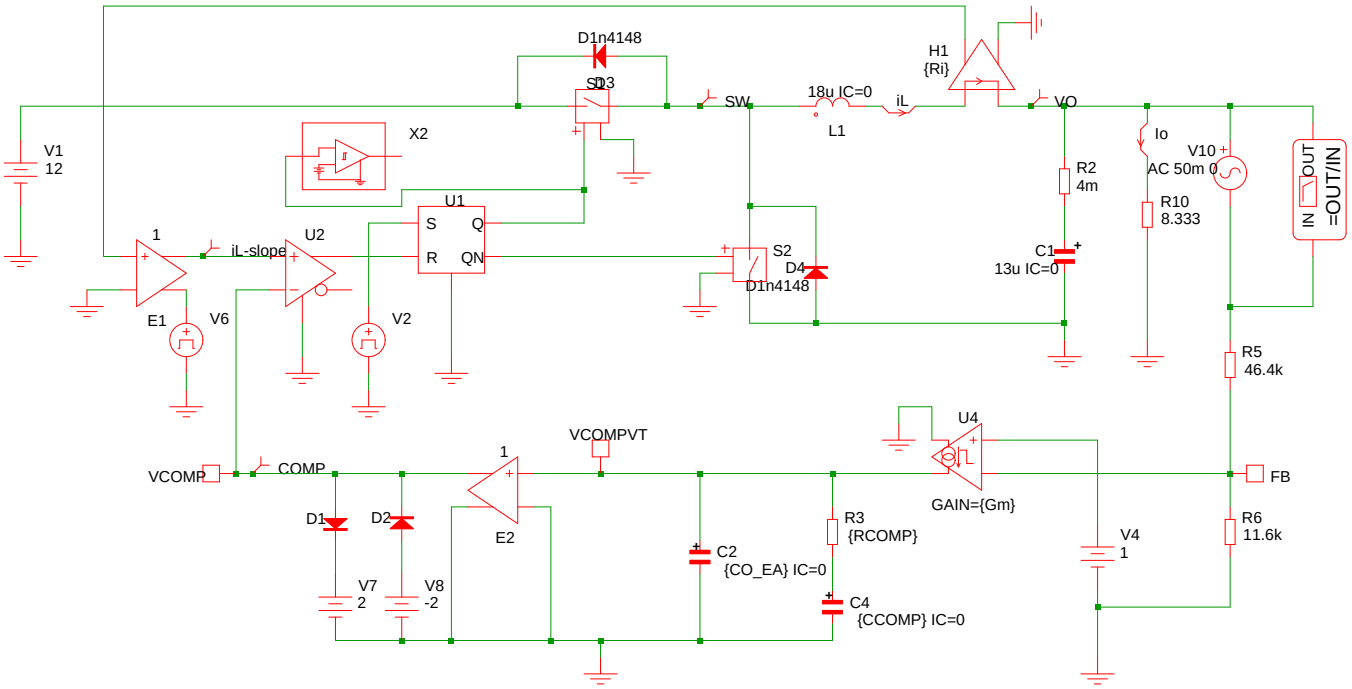

Figure 5. Schematic of A Simplified SIMPLIS Model

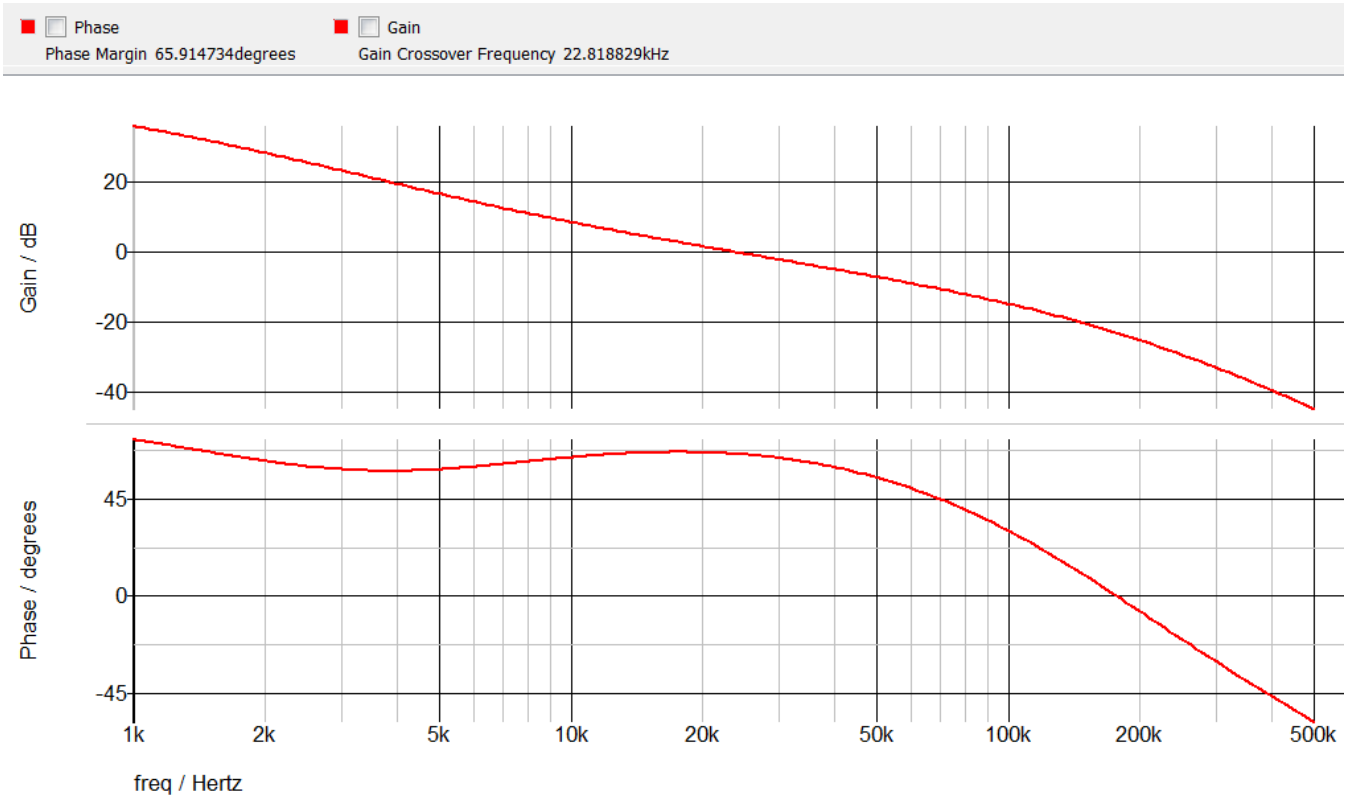

Figure 6. Bode Plot Simulation Result at V_{IN} = 12 V, I_O = 0.6 A

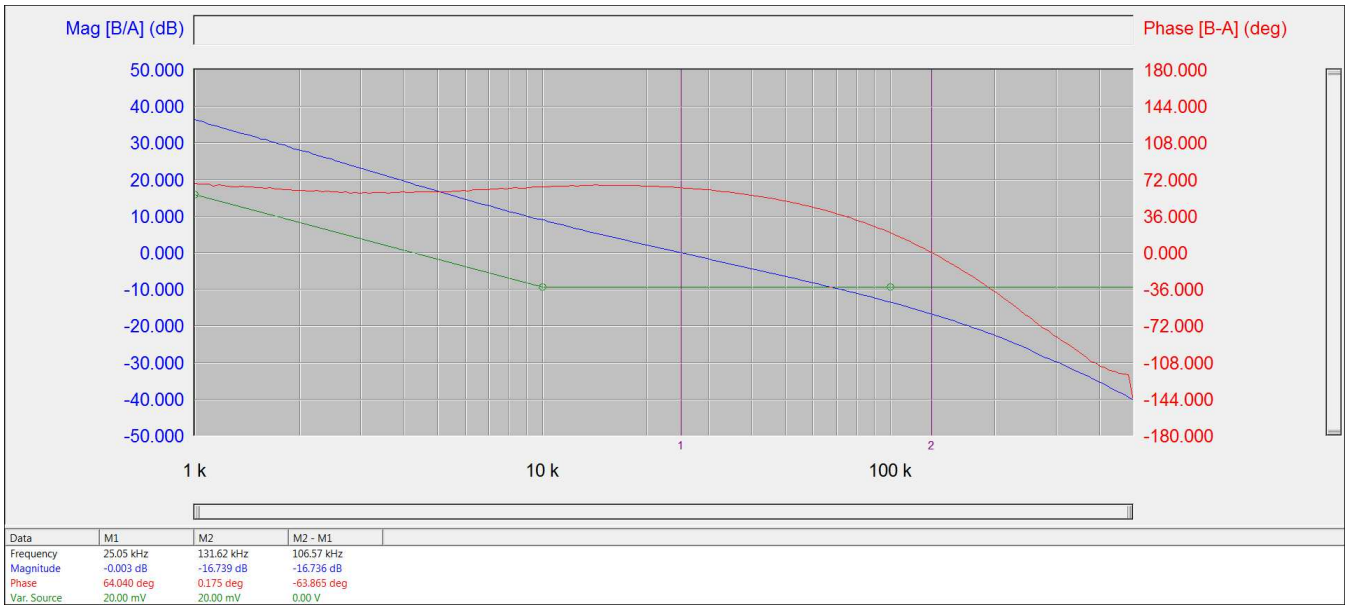

Figure 7. Bode Plot Test Result at V_{IN} = 12 V, I_O = 0.6 A

Table 2. Calculation, Simulation, and Bench Measurement Results Comparison

		CALCULATION RESULTS		SIMULATION RESULTS		BENCH MEASUREMENT	
V_{IN} (V)	I_O (A)	f_c (kHz)	PHASE MARGIN (°)	f_c (kHz)	PHASE MARGIN (°)	f_c (kHz)	PHASE MARGIN (°)
7	0.1	23.4	59.2	22.8	61.3	23.6	58.4
7	0.6	23.4	62.2	22.7	64.4	24.7	61.7
12	0.1	23.4	61.2	22.9	62.8	24.6	60.3
12	0.6	23.4	64.2	22.8	65.9	25.1	64
36	0.1	23.4	63	22.9	64.3	23.7	61.1
36	0.6	23.4	66	22.9	67.4	23.9	66.3

4 Summary

For an internally compensated, peak current mode buck converter, consider the loop response when designing inductor and output capacitor. This application report simplifies the inside current loop as a single pole, provides the constraint to ensure loop stability, and gives out an equation to calculate bandwidth and phase margin. The inductor and output capacitor is designed step-by-step considering loop response. The theory is verified by simulation and bench measurement results.

5 References

1. Texas Instruments, *TPS560430 4-V to 36-V, 600-mA Synchronous Step-Down Converter Data Sheet*
2. R.B. Ridley, A New Small-Signal Model for Current-Mode Control, PhD Dissertation, Virginia Polytechnic Institute and State University, November, 1990.
3. Texas Instruments, *TPS65270 Loop Compensation Design Consideration Application Report*
4. Texas Instruments, *How to Evaluate the Maximum Inductor in an Internal Compensation PCM Buck Converter Application Report*

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (July 2018) to A Revision	Page
• Edited application report for clarity.	1

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