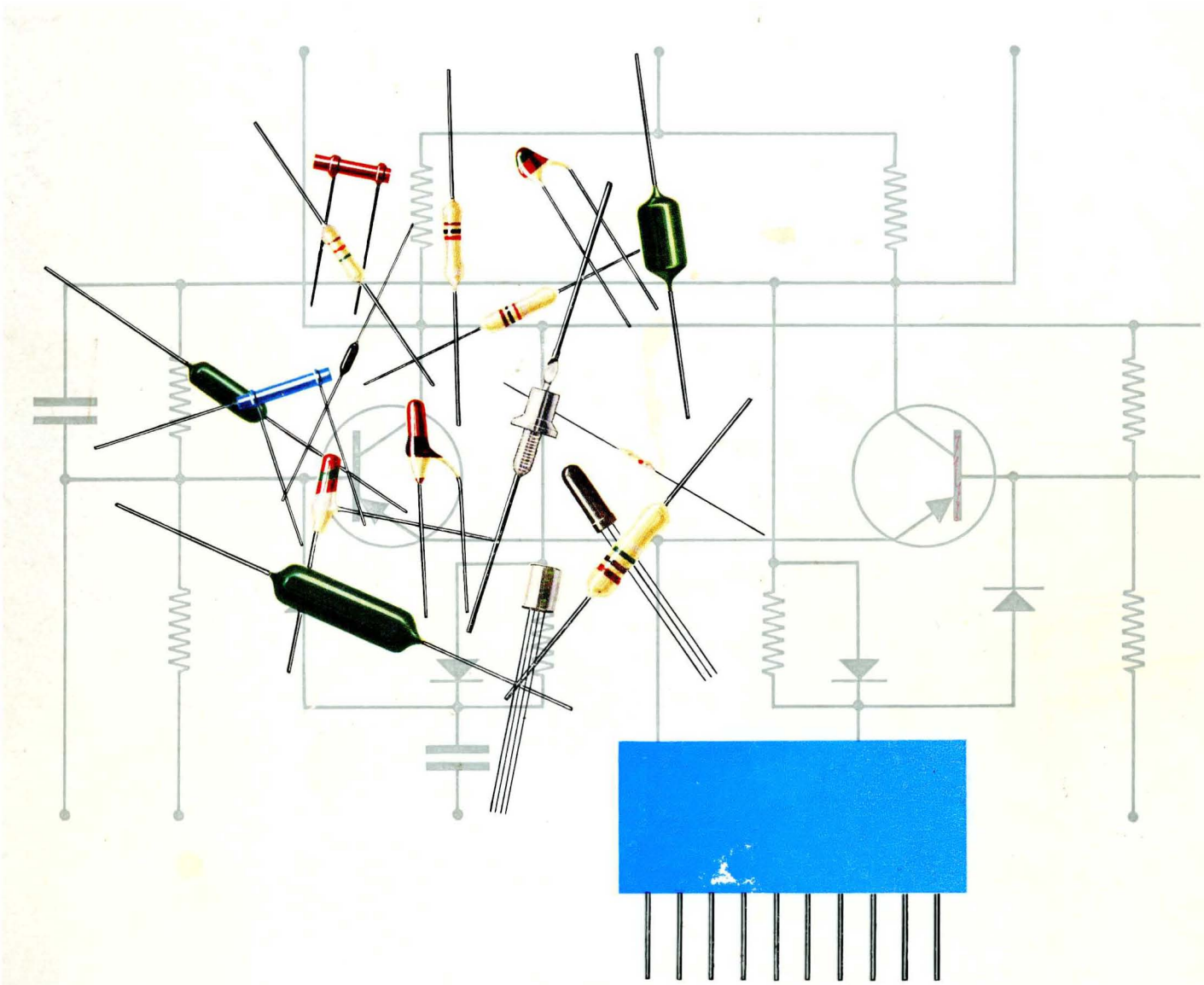


PHILIPS

CIRCUIT BLOCKS

INDUSTRIAL
COMPONENTS
AND
MATERIALS
DIVISION

The information given in this Bulletin does not imply a licence under any patent.

General Information on Circuit Blocks

APPEARANCE

A circuit block is a small encapsulated unit containing a basic electronic circuit, designed to accept and operate upon a specific type of input signal and to produce a specific type of electrical output. A number of different blocks can be combined to form larger parts of an electronic digital system.

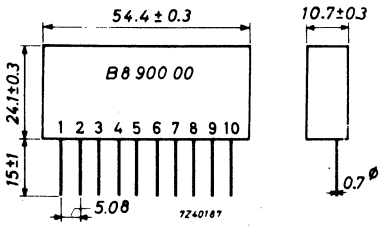


Fig.1. Dimensional drawing of the circuit block.

The dimensions of all circuit blocks are approx. 54 mm x 24 mm x 11 mm (see Fig. 1). Out of one side of 54 mm x 11 mm emerge ten wire terminals of 0.7 mm diameter and 15 mm length. The distances between the wires are 5.08 mm (0.2 ins.) in accordance with the I.E.C. standard hole grid for printed-wiring boards.

The blocks are colour-coded, a different colour being used for each group of functions.

TYPES OF CIRCUIT BLOCK

The following circuit blocks are available:

description	colour	abbreviation	type number
Pulse shaper	green	PS 1	B8 950 00
Flip-flop	red	FF1	B8 920 00
One-shot multivibrator	green	OS 1	B8 950 01
Twin emitter follower	yellow	2.EF1	B8 940 01
Emitter follower/inverter amplifier	yellow	EF1/IA1	B8 940 00
Twin inverter amplifier	yellow	2.IA1	B8 940 02
Twin 2-input negative gate	orange	2.2N1	B8 930 01
Twin 3-input negative gate	orange	2.3N1	B8 930 00
Twin 2-input positive gate	orange	2.2P1	B8 930 03
Twin 3-input positive gate	orange	2.3P1	B8 930 02
Twin inverter amplifier	yellow	2.IA2	B8 940 05
Twin emitter follower	yellow	2.EF2	B8 940 03

TYPE NUMBERING SYSTEM

The figures of which the type number is composed have the following meaning:

B8 900 00 01

- 01 → Reserved for minor changes
- 00 → Serial number
- 900 → Mechanical design
- B8 → Main circuit function

2 (red) - elements with a memory function
3 (orange) - gate circuits
4 (yellow) - amplifying elements
5 (green) - signal generators and pulse-shaping elements
6 (blue) - miscellaneous
8 - special circuits (no functional guarantee)
9 - standard circuits (functional guarantee).

ADVANTAGES OF CIRCUIT BLOCKS

Some of the outstanding advantages of circuit blocks are:

- saving of time and effort in the development and manufacture of electronic equipment;
- saving of handling, mounting and testing costs in manufacture;
- high and constant quality level;
- simplification of stock-keeping and ordering;
- rationalisation through standardised units.

FIELDS OF APPLICATION

Circuit blocks can in general be used in all digital data-handling equipment, such as:

a. test and measuring set-ups in research and development laboratories etc.;
b. bread-board models and prototypes of electronic equipment;
c. equipment or systems that are manufactured in units or in small series (project work);
d. normal or large series of measuring, regulating and control equipment, computers, telecommunication equipment, various production machines etc.

CONSTRUCTION

The construction of the circuit block can easily be seen in the cut-away view of Fig.2.

The electronic components, of which the circuit is made up (transistors, diodes, resistors, capacitors) are mounted on a printed-wiring board. This board is provided with plated-through holes to ensure reliable joints due to the large contact area of soldered contacts. The connecting leads are also mounted on the printed-wiring board.

Protection against mechanical shock and vibration is provided by the potting compound, whilst atmospheric influences are excluded by the sealing compound, by which the synthetic resin case is hermetically closed.

For the sake of reference the connecting leads are numbered (1 to 10), whilst the type number and the colour coding simplifies assembly and service.

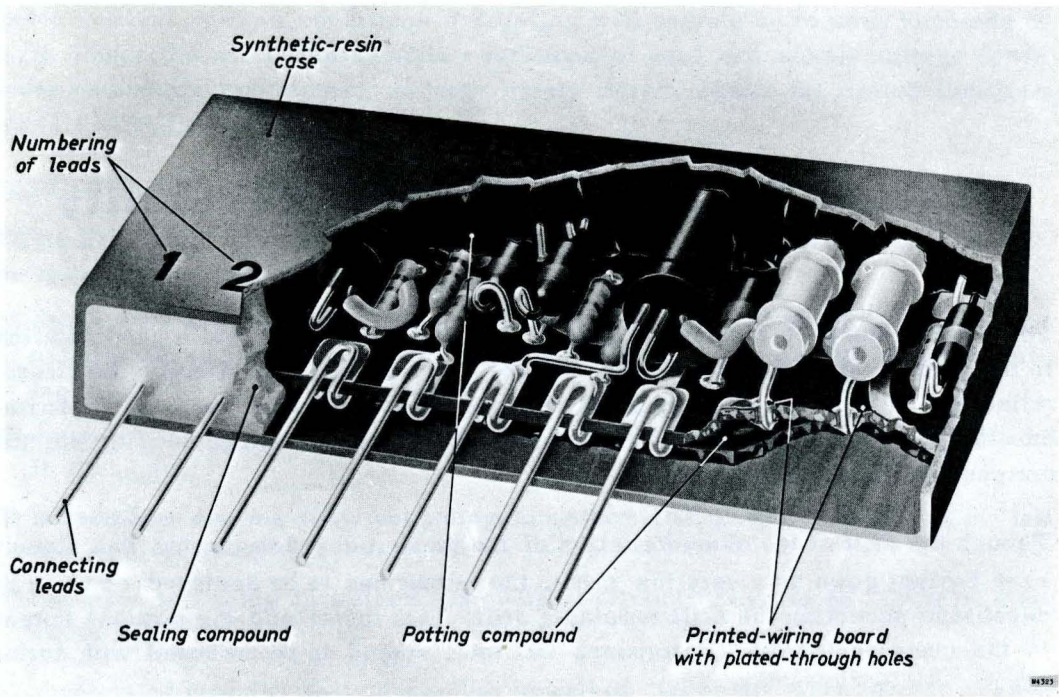


Fig.2. Cut-away view of a circuit block.

ELECTRICAL CHARACTERISTICS

Besides passive network elements (resistors, capacitors), only semiconductor devices are incorporated in the circuit blocks, viz. transistors, Ge-diodes and Si-diodes. As a result the inherent advantages of these semiconductors are reflected in the properties of the circuit blocks, such as low supply voltages and small power dissipation.

The standard supply voltage of the circuit blocks is +6 V and/or - 6 V (± 10%), so that no special measures with respect to insulation and protection need be taken.

The power dissipation of the blocks is so small (20 to 100 mW) that no special precautions are necessary with regard to cooling.

Design Considerations and Reliability

The main problem in the design of electronic equipment is to find a good solution to the problem of attaining an optimum level of reliability. The effective functional reliability of an electronic apparatus is - once a given circuit has been determined - exclusively dependent on the stability of the characteristics of the circuit components during their lives.

Though the drift of the characteristics of the present-day components has already been brought down to a very low value, the circuit has to be designed so as to be capable of accepting the still remaining drift. This factor and the nominal spread in the component values determines the total spread to be reckoned with during life.

A very safe design can be achieved by adopting the so-called "worst-case design" principle, in which these total spreads in their most unfavourable combination are taken as a design basis. As far as systematic failures are concerned, these considerations lead to a very safe circuit.

Generally, the performance of a circuit, designed on this basis, is rather poor, however, because of the extreme tolerance combinations that have been taken into account. On the other side, the probability that these extreme combinations occur is practically nil, the probability of "survival" of the circuit element being completely dependent on sudden failures, which are mostly of a non-systematic and catastrophic nature.

The choice of the components in the circuit blocks, the provisions taken in the manufacture of these components, as well as the special protective measures lead to a strong reduction of such sudden failures. Furthermore, a very safe electronic design procedure is followed, applying all available knowledge on the specific statistic behaviour of the components. In this way units with a high standard of reliability, a long life and a high electronic performance are obtained.

It stands to reason that a good performance of the circuit blocks can only be guaranteed, if the user, in his turn, sticks to the operating conditions given by the manufacturer. These operating conditions and guarantee, which apply to all types of circuit block, are given below.

CIRCUIT PERFORMANCE AND GUARANTEE

The circuit blocks are guaranteed to work properly at the maximum speed of operation under maximum load conditions as given in the "Technical Data" (see p. 14 ff) in the temperature range of -20 °C to +60 °C (-4 °F to +140 °F).

Though the circuit blocks function reliabily at any combination of the margins given with respect to supply voltage and ambient temperature, the maximum operational safety margin and the maximum life can be expected by operating the units as closely as possible to the given nominal values of +6 V and -6 V for the supply voltages and 25 °C (77 °F) for the ambient temperature.

Apart from some output devices the circuit blocks are designed for an operational speed of 100 kc/s. Because of the large safety margin that has already been taken into account, no further speed-derating is necessary.

Under nominal no-load conditions a flip-flop will operate up to many hundreds of kc/s. Under the most unfavourable conditions of load and supply voltage (even under end-of-life conditions), a large safety margin above the stated maximum speed will still remain.

TEST SPECIFICATIONS

Before and during manufacture samples of circuit blocks are regularly subjected to the following tests.

(1) Shock test and vibration test according to method 201 of MIL-STD-202, terminals tested on strength, test on mounting, soldering, lacquer and coding, heating tests.

(2) corrosion test (salt haze), according to method 101 of MIL-STD-202 (condition B, 50 hours).

(3) temperature cycling test, according to method 102 of MIL-STD-202 (5 cycles from - 20 °C to +65 °C).

(4) dip test, according to method 104 of MIL-STD-202 (2 cycles 65 °C/20 °C, condition B, NaCl).

(5) accelerated humidity test, according to method 106 of MIL-STD-202 (10 cycles 65 °C).

(6) prolonged humidity test (units not operating), according to method C of BCMT (40 °C, relative humidity: 90% to 95%, duration longer than 2000 hours, functional marginal measurements after 100, 250, 1000 etc. hours).

(7) as item 6, but units operating under the most unfavourable electrical conditions.

The Design of a Circuit with Circuit Blocks

BLOCK DIAGRAM

The growing complexity of the electronic system of to-day calls for a simple logical unambiguous way of representation in the system circuit diagram. Effective use is made of a block diagram, in which each symbol represents a specific unit function, which may represent a system component of different complexity. Such a block in the diagram may denote, for instance, anything between a complete production plant and a small basic electronic function, such as a flip-flop, a gate circuit etc. The latter can be considered as basic building bricks for electronic systems. The circuit blocks belong to this category, each type representing a single functional element or a combination of two of such elements.

BASIC LOGIC SYMBOLS

When a logic circuit is to be designed, whether it should be equipped with circuit blocks or any other elements, it may be useful to make up a block diagram without paying any attention to the technical set-up for the time being. In such a block diagram use can be made of symbols of purely functional elements, some of which are shown in Fig.3.

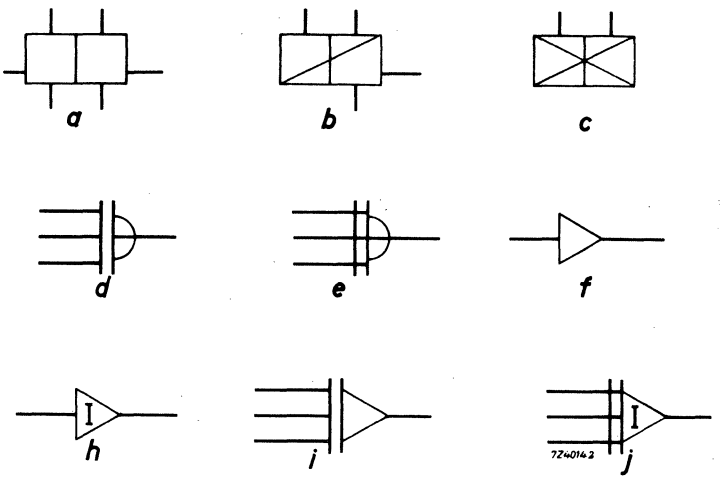


Fig.3. Symbols for logic circuits.

a. bi-stable multivibrator (flip-flop)
b. mono-stable multivibrator (one-shot)
c. *a*-stable multivibrator
d. and-gate
e. or-gate
f. non-inverting amplifier (emitter-follower)
h. inverter
i. and-gate with emitter follower
j. or-gate with inverter.

From the symbols in Fig. 3 only the and-gate, the or-gate and the inverter perform a purely logic function. According to the Boolean algebra the relations between the output signal and the input signal of these elements are as follows:

AND-gate: (Fig.3*d*): $P = A \cdot B \cdot C \cdot \ldots\ldots\ldots\ldots \cdot N$
OR-gate: (Fig.3e): $P = A + B + C + \ldots\ldots\ldots\ldots + N$
Inverter (Fig.3*h*): $P = \overline{A}$ ($\overline{A}$ = "NOT A")

A, B, C etc. can attain the values "0" (no signal) and "1" (signal). It should be remembered, that in terms of Boolean algebra $1 + 1 = 1$, so that the value of P in the OR-gate can never exceed 1. The action of the inverter is such, that an input signal "0" produces an output signal "1", or the reverse ($\overline{0} = 1$, $\overline{1} = 0$).

COMBINATION OF LOGIC SYMBOLS

When Boolean functions of a more complex character than those of the AND-gate, the OR-gate or the inverter are dealt with, combinations of these elements must be used. As an example the function $P = \overline{A \cdot (B + C)}$ will be considered. This function is performed by the following logic circuit (Fig. 4).

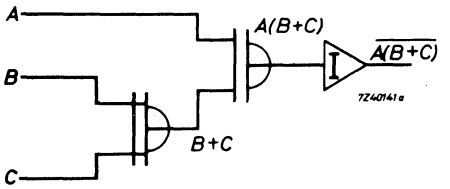


Fig. 4. Logic circuit for obtaining the function $P = \overline{A \cdot (B + C)}$.

In some cases, and specially when a particular arrangement cannot be used for technical reasons, another arrangement can be found by converting the function into an equivalent function, whereby the rules of Boolean algebra may come in useful. The function $P = \overline{A \cdot (B + C)}$ can be converted into the function $P = \overline{A} + \overline{B} \cdot \overline{C}$, which corresponds to the logic circuit of Fig. 5. From the Table below, in which all combinations of A, B and C are considered, it can easily be seen that the functions $P = \overline{A \cdot (B + C)}$ and $P = \overline{A} + \overline{B} \cdot \overline{C}$ are equivalent.

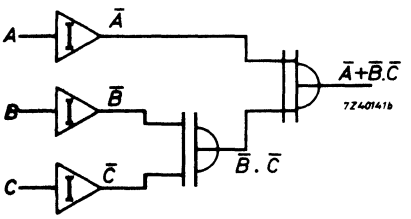


Fig. 5. Logic circuit for obtaining the function $P = \overline{A} + \overline{B} \cdot \overline{C}$.

A	B	C	$\overline{A}$	$\overline{B}$	$\overline{C}$	B+C	$\overline{B} \cdot \overline{C}$	A(B+C)	$\overline{A(B+C)}$	$\overline{A} + \overline{B} \cdot \overline{C}$
0	0	0	1	1	1	0	1	0	1	1
1	0	0	0	1	1	0	1	0	1	1
0	1	0	1	0	1	1	0	0	1	1
0	0	1	1	1	0	1	0	0	1	1
1	1	0	0	0	1	1	0	1	0	0
0	1	1	1	0	0	1	0	0	1	1
1	0	1	0	1	0	1	0	1	0	0
1	1	1	0	0	0	1	0	1	0	0

RULES OF BOOLEAN ALGEBRA

The equations given below can be used advantageously to simplify and convert logic functions. They can easily be verified by making up tables as shown above.

$A + 0 = A$ $\qquad$ $A \cdot 0 = 0$

$A + 1 = 1$ $\qquad$ $A \cdot 1 = A$

$A + A = A$ $\qquad$ $A \cdot A = A$

$A + \overline{A} = 1$ $\qquad$ $A \cdot \overline{A} = 0$

$A + AB = A$ $\qquad$ $A(A+B) = A$

$A + \overline{A}B = A + B$ $\qquad$ $A(\overline{A}+B) = AB$

$A(B+C) = AB + AC$ $\qquad$ $(A+B)(A+C) = A + BC$

$$A + B + C + \ldots\ldots + N = \overline{\overline{A} \cdot \overline{B} \cdot \overline{C} \ldots\ldots \cdot \overline{N}}$$

$$A \cdot B \cdot C \cdot \ldots\ldots \cdot N = \overline{\overline{A} + \overline{B} + \overline{C} \ldots\ldots + \overline{N}}$$

$$\overline{A} + \overline{B} + \overline{C} + \ldots\ldots + \overline{N} = \overline{A \cdot B \cdot C \ldots\ldots \cdot N}$$

$$\overline{A} \cdot \overline{B} \cdot \overline{C} \cdot \ldots\ldots \cdot \overline{N} = \overline{A + B + C \ldots\ldots + N}$$

ALLOCATION OF THE SIGNAL VALUES

In digital systems the signal values "0" and "1" are allocated to binary voltage levels. In electronic circuits with circuit blocks the voltage levels occurring at the output of multivibrators are commonly used for this purpose, viz. approx. 0 V and < -3.8 V. In principle it is immaterial which of these levels is denoted by "0" or "1". In systems, where the majority of the elements are formed by PNP common emitter circuits (which is actually the case with circuit blocks) it may be preferable to denote the binary levels by "negative high" and "negative low". In the circuit blocks these levels are given the logic values "1" and "0" respectively ("negative low" approx. 0 V and "negative high" < -3.8 V).

Once the above system is accepted, the circuit block, indicated by "negative gate" acts as an AND-gate and the "positive gate" as an OR-gate. (in the opposite case ("0" for < -3.8 V and "1" for approx. 0 V), the negative gate performs the OR function and the positive gate the AND function.)

SYMBOLS FOR CIRCUIT BLOCKS

After the block diagram with logic symbols has been made up, the logic symbols should be translated into circuit blocks. To this end it may be useful to make a second diagram in which the logic symbols are replaced by symbols representing the corresponding circuit blocks. The latter symbols, recommended for this purpose, have been entered in the Technical Data of the circuit blocks. Each of these symbols consists of a rectangle, in which the type of circuit block and the connections are indicated (Fig.6). Since also the reference numbers of the connecting leads are indicated in the symbol, the equipment can be constructed directly from the circuit block diagram.

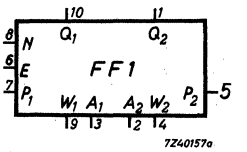


Fig.6. Typical symbol of a circuit block (FF1).

In Fig. 7 an example is given of how logic symbols can be combined so as to obtain an arrangement that can be built up from circuit blocks.

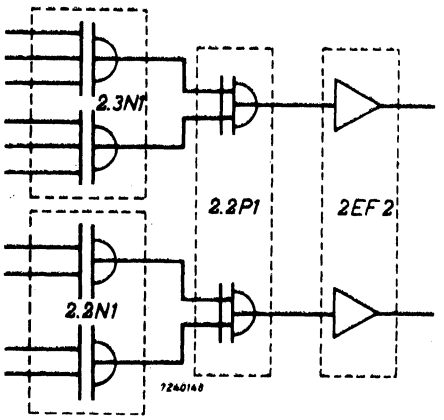


Fig.7. Combination of logic functional symbols into circuit blocks.

THE LOADING TABLE

Since the loadibility of circuit blocks is limited, they may not be arranged arbitrarily. A circuit block diagram, made up from a diagram with logic symbols, should be carefully checked on the basis of the Loading Table given on page 40. If a specific combination of circuit blocks appears to be inadmissible, it should be rearranged into a permissible combination. As was already discussed on page 12. Boolean algebra can be used for this purpose.

In some cases a loading differing slightly from that given in the Loading Table may be possible. This must be considered with the following limitations in mind:

(1) the maximum permissible output current of the driving stage;
(2) the minimum required input current of the driving stage;
(3) the maximum permissible input current of the driving stage;
(4) the required voltage level at the input of the driven stage;
(5) for AC inputs: the maximum rise time of the input signal of the driving stage.

The above limitations can be derived from the Technical Data.

Technical Data (tentative)

PULSE SHAPER (PS1)

type B8 950 00

(colour: green)

The unit B8 950 00 contains a transistor squaring-amplifier followed by an inverter circuit. The transistors are medium-speed switching types OC 47 or equivalent items.

A DC input signal having an amplitude exceeding the input threshold-voltage of the unit, is inverted and re-shaped into the standard DC level at the output. The output voltage transients are very short and can be used for driving other circuit blocks, multivibrator circuits included.

Frequency range:	0-100 kc/s
Ambient-temperature range	-20 to + 60 °C
Weight:	approx. 19 g.

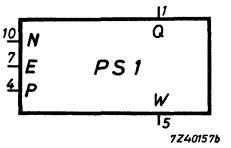


Fig.8.

CIRCUIT DATA

Terminal:
1 = Q = output
2 = internally connected
3 = internally connected
4 = P = supply +6 V
5 = W = input
6 = internally not connected
7 = E = common supply 0 V
8 = internally not connected
9 = internally connected
10 = N = supply -6 V

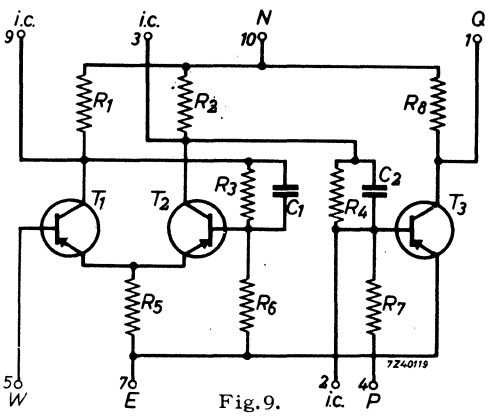


Fig.9.

POWER SUPPLY

Terminal 4: V_P = +6 V ± 10 %, I_P = 0.27 mA[1])
7: V_E = 0 V common
10: V_N = -6 V ± 10 %, $-I_N$ = 3.8-6.8 mA[1])
} Nominal value of the current

INPUT-SIGNAL REQUIREMENTS [2])

"ON" THRESHOLD

Required input current	$-I_W$	= min. 0.18 mA[1])
Input-voltage threshold	$-V_W$	= min. 0.75 V
Limiting value of input current	$-I_W$	= max. 10 mA

INPUT LEVEL "NEGATIVE LOW"

Limiting value of input voltage	V_W	= max. 10 V
Input capacitance:		about 20 pF

---

[1]) The sign is positive when the current flows towards the circuit.

[2]) These data only apply to the most adverse working condition for a combination of units, namely to supply voltages V_N = -5.4 V and V_P = +6.6 V. Unless differently specified, all the voltage and current figures represent absolute maximum values.

OUTPUT CHARACTERISTICS [2])

INPUT LEVEL "NEGATIVE HIGH" (TRANSISTOR T_3 CONDUCTING)

Voltage	$-V_Q$	= max. 0.2 V
Load current	$-I_Q$	= max. 1.2 mA [1])

INPUT LEVEL "NEGATIVE LOW" (TRANSISTOR T_3 NON-CONDUCTING)

Voltage	$-V_Q$	= min. 3.8 V
Load current	I_Q	= max. 0.6 mA [1])

Maximum capacitive load for high-speed operation: 1000 pF.

When the maximum capacitive and resistive loads are applied simultaneously, some reduction in maximum switching speed may occur.

SWITCHING AND DELAY TIMES

A square-wave input signal is assumed.

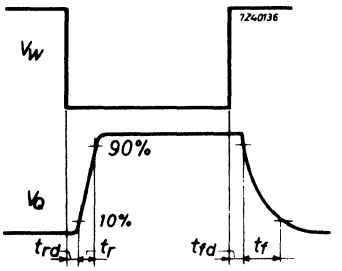


Fig. 10.

UNIT UNLOADED

Rise time	t_r	= max. 0.2 μsec
Rise delay	t_{rd}	= max. 0.1 μsec
Fall time	t_f	= max. 0.2 μsec
Fall delay	t_{fd}	= a function of driving current

OUTPUT IMPEDANCE

Positive-going output voltage	R_i = 100 Ω
Negative-going output voltage	R_i = 2200 Ω

FLIP-FLOP (FF1)

type B8 920 00

(colour: red)

The unit B8 920 00 contains a transistor bi-stable multivibrator circuit. The transistors are medium-speed switching types OC 46 or equivalent items.

The circuit constitutes a memory function when driven by means of a DC level or a positive-going voltage step (AC signal), and it can also be used as a binary scale-of-two with a positive-going input signal.

Frequency range	0-100 kc/s
Ambient temperature range	-20 to +60 °C
Weight	approx. 22 g

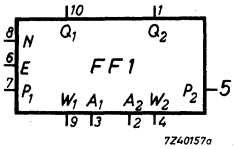


Fig. 11.

CIRCUIT DATA

Terminal
1 = Q_2 = output transistor 2
2 = A_2 = AC input transistor 2
3 = A_1 = AC input transistor 1
4 = W_2 = DC input transistor 2
5 = P_2 = supply +6 V
6 = E = common supply 0 V
7 = P_1 = supply +6 V
8 = N = supply -6 V
9 = W_1 = DC input transistor 1
10 = Q_1 = output transistor 1

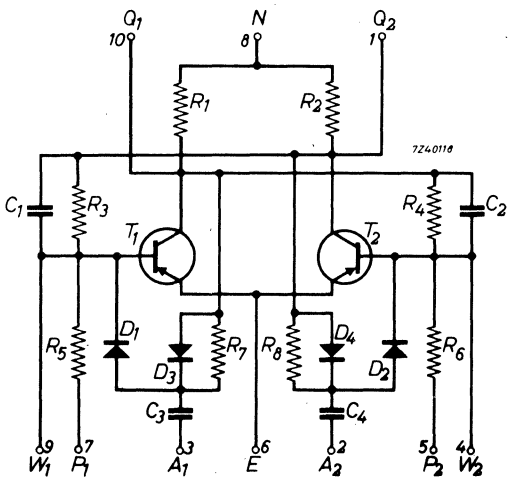


Fig. 12.

POWER SUPPLY

Terminal 5: V_{P2} = +6 V ± 10 %, I_{P2} = 0.15 mA[1])
6: V_E = 0 V common
7: V_{P1} = +6 V ± 10 %, I_{P1} = 0.15 mA[1])
8: V_N = -6 V ± 10 %, $-I_N$ = 6 mA[1])

} Nominal value of the current

INPUT-SIGNAL REQUIREMENTS[2])

AC INPUT SIGNAL (A terminals)

A positive-going voltage step is applied to terminal A_1 or A_2, or to both terminals interconnected in the case of binary scale-of-two applications. This voltage step drives the transistor T_1 (T_2) into the non-conducting state.

Driving Signal

Rise time	t_r	= max. 0.4 μsec
Voltage	$-V_{AM}$	= min. 3.8 V
		= max. V_N
Length of driving pulse	t	= min. 0.5 μsec
Input noise level:		max. 1 V

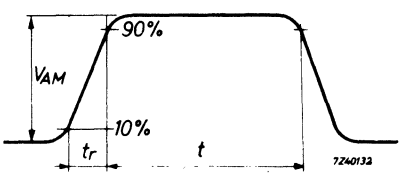


Fig. 13.

DC INPUT SIGNAL (*W* terminals)

A DC voltage level is applied to terminal W_1 or W_2. A positive voltage drives the transistor T_1 (T_2) into the non-conducting state, and a negative voltage drives it into the conducting state.

TRANSISTOR CONDUCTING

Input current	$-I_W$	= min.	0.4 mA[1]) ($-V_W$ = approx. 0.3 V)
limiting value		= max.	5 mA[1])
Input resistance	R_W	= approx.	800 Ω

TRANSISTOR NON-CONDUCTING

Input current	I_W	= min.	1 mA[1])
Input voltage	V_W	= min.	0.2 V
limiting value		= max.	10 V
Input resistance	R_W	= approx.	5600 Ω

OUTPUT CHARACTERISTICS [2])

TRANSISTOR CONDUCTING

Output voltage	$-V_Q$	= max. 0.2 V
Load current	$-I_Q$	= max. 2.5 mA[1])

TRANSISTOR NON-CONDUCTING

Output voltage	$-V_Q$	= min. 3.8 V
Load current	I_Q	= max. 0.7 mA[1])

Load currents of equal sign, up to the maximum figures given, can be drawn from the two output terminals simultaneously. In the case of simultaneous load currents of opposite sign, a substantial reduction in maximum load current must be taken into account.

Maximum capacitive load: 2000 pF

When the maximum capacitive and resistive loads are applied simultaneously, some reduction in maximum switching speed may occur.

SWITCHING AND DELAY TIMES

A square-wave input signal (A terminals) is assumed.

UNIT UNLOADED

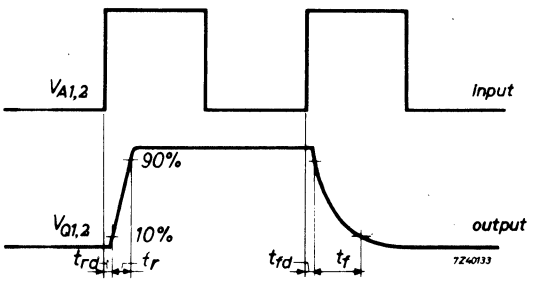


Fig. 14.

Rise time	t_r	= max. 0.3 μsec
Rise delay	t_{rd}	= max. 0.8 μsec
Fall time	t_f	= max. 2 μsec
Fall delay	t_{fd}	= max. 0.6 μsec

OUTPUT IMPEDANCE

Positive-going output voltage R_i = 100 Ω
Negative-going output voltage R_i = 1000 Ω

---

[1]) The sign is positive when the current flows towards the circuit.

[2]) These data apply to the most adverse working condition for a combination of units, namely to supply voltages V_N = -5.4 V and V_P = +6.6 V. Unless differently specified, all the voltage and current figures quoted represent absolute maximum values.

ONE-SHOT MULTIVIBRATOR (OS1)

type B8 950 01

(colour: green)

The unit B8 950 01 contains a transistor monostable multivibrator circuit. The transistors are medium-speed switching OC 47 or equivalent items.

When a positive-going voltage step is applied to terminal A_2 the circuit generates a pulse on the Q-terminals. The length of the output pulse is determined by the value of the external capacitance C between the terminals 4 and 10.

Frequency range	0 -100 kc/s
Ambient temperature	-20 to +60 °C
Weight	approx. 20 g.

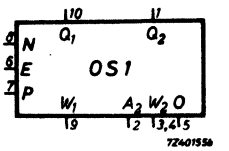


Fig. 15.

CIRCUIT DATA

Terminal
1 = Q_2 = output 2
2 = A_2 = AC input 2
3 = W_2 } = DC input 2
4 = W_2 }
5 = O = supply -6 V
6 = E = common supply 0 V
7 = P = supply +6 V
8 = N = supply - 6 V
9 = W_1 = DC input 2
10 = Q_1 = output 1

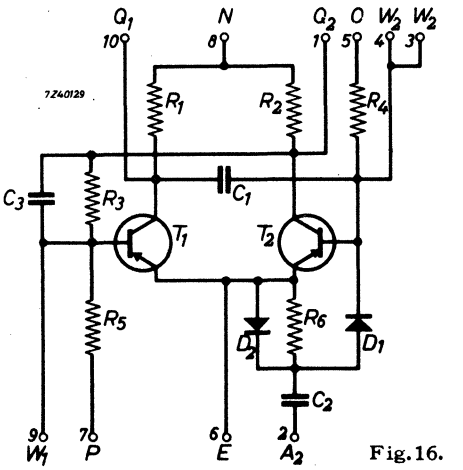


Fig. 16.

POWER SUPPLY

Terminal 6: V_E = 0 V common
7: V_P = +6 V ±10 %, I_P = 0.15 mA[1] } Nominal value of the current
8: V_N = - 6 V ±10 %, $-I_N$ = 6 mA[1] }

INPUT SIGNAL REQUIREMENTS[2])

AC INPUT SIGNAL

A positive-going voltage step is applied to terminal A_2.

Driving Signal

Rise time	t_r	= max.	0.4 μsec
Length of driving pulse	t	= min.	0.5 μsec
Voltage	V_{A2M}	= min.	3.8 V
		= max.	10 V
Input noise level:		max.	1 V
Input impedance:		about	500 pF

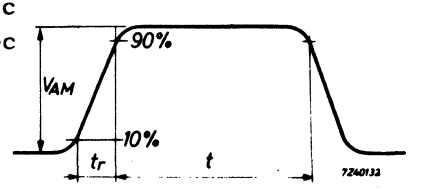


Fig. 17.

DC INPUT SIGNAL

The W terminals are normally not used.

OUTPUT CHARACTERISTICS[2])

TRANSISTOR CONDUCTING

Output voltage	$-V_Q$	= max. 0.2 V
Load current	$-I_{Q1}$	= max. 2.2 mA[1])
	$-I_{Q2}$	= max. 0.5 mA[1])

TRANSISTOR NON-CONDUCTING

Output voltage	$-V_Q$	= min. 3.8 V
Load current	I_{Q1}	= max. 1.4 mA[1])
	I_{Q2}	= max. 0.7 mA[1])

Load currents of equal sign, up to the maximum figures given, can be drawn from the two output terminals simultaneously. In the case of simultaneous load currents of opposite sign, a substantial reduction in maximum load current must be taken into account.

The maximum capacitive load for high-speed operation is 2000 pF (a capacitive load on the Q terminal may increase the length of the output pulse by max. 25 %).

When the maximum capacitive and resistive loads are applied simultaneously, some reduction in maximum switching speed may occur.

SWITCHING AND DELAY TIMES

A square-wave input signal is assumed (A_2 terminal), and an amplitude V_{AM} = min. 3.8 V.

Q_1 OUTPUT UNLOADED

Rise delay	t_{rd}	= max. 0.8 μsec
Rise time	t_r	= max. 0.3 μsec
Fall time	t_f	= dependent on the external capacitance between the terminals 4 and 10.

Q_2 OUTPUT UNLOADED

Fall delay	t_{fd}	= max. 0.2 μsec
Fall time	t_f	= max. 1.8 μsec
Rise time	t_r	= max. 1 μsec

The rise time is too long to allow driving a second multivibrator circuit. In that case, the Q_1 output should be used.

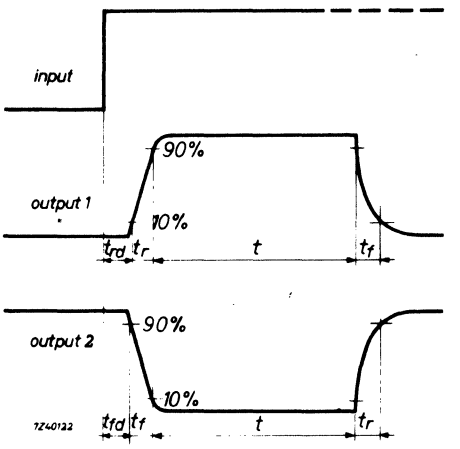


Fig. 18.

[1]) The sign is positive when the current flows towards the circuit.

[2]) These data only apply to the most adverse working condition for a combination of units, namely to supply voltages V_N = -5.4 V and V_P = +6.6 V. Unless differently specified, all the voltage and current figures quoted represent absolute maximum values.

LENGTH OF THE OUTPUT PULSE

When the unit is unloaded, t = 2.2 - 4.5 μsec.

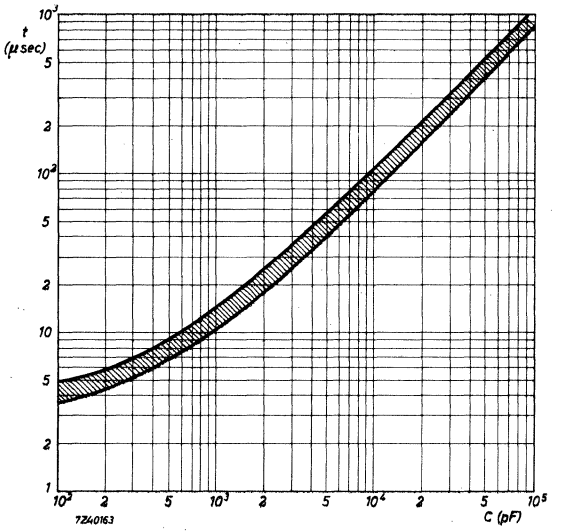


Fig.19.

In this diagram, the pulse length t has been plotted as a function of the external capacitance C between the terminals 4 and 10, at an ambient temperature of 25 °C and at supply voltages V_N = -6 V and V_p = +6 V.

Note 1 In case an electrolytic capacitor is used for C, take care that its + terminal is connected to terminal 4.

The use of electrolytic capacitors should be avoided when close-tolerance pulse lengths are required.

According as the C value is higher, the sensitivity to disturbing signals (mainly on the supply line -6 V) increases. In this case a large external blocking capacitor may be required between the -6 V supply and 0 V common, to be mounted close to the unit.

Note 2 The length t of the output pulse is affected by capacitively loading the Q_1 or Q_2 terminal. In general, t will be within 0 to +35% of the figures stated under "output unloaded".

STABILITY OF PULSE LENGTH

An increase in supply voltage V_N of 5% reduces the pulse length by less than 1%. Any variation of the supply voltage V_P has practically no influence.

An increase in ambient temperature of 1 °C reduces the pulse length by less than 0.5%.

TWIN EMITTER FOLLOWER (2EF1)

type B8 940 01

(colour: yellow)

The unit B8 940 01 contains two identical transistor emitter-follower circuits that constitute a non-inverting buffer-amplifier function with a low output impedance. The transistors are medium-speed switching types OC47 or equivalent items.

The unit is equipped with a tap on the output resistor for cases in which a level shift towards the positive supply line is required.

Frequency range:	0-100 kc/s
Ambient-temperature range:	-20 to +60 °C
Weight:	approx. 19 g

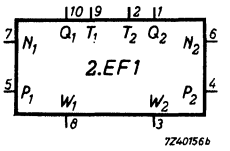


Fig.20.

CIRCUIT DATA

Terminal 1 = Q_2 = output 2
2 = T_2 = tap output 2
3 = W_2 = input 2
4 = P_2 = supply 2, +6 V
5 = P_1 = supply 1, +6 V
6 = N_2 = supply 2, -6 V
7 = N_1 = supply 1, -6 V
8 = W_1 = input 1
9 = T_1 = tap output 1
10 = Q_1 = output 1

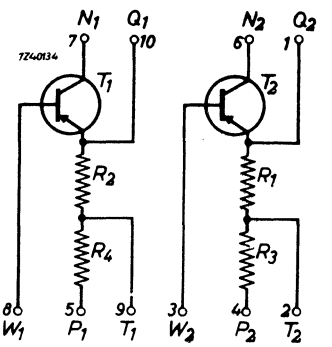


Fig.21.

POWER SUPPLY

Terminal 4: V_{P1} = +6 V ± 10 %, I_{P1} = 3.3-6.6 mA[1])
5: V_{P2} = +6 V ± 10 %, I_{P2} = 3.3-6.6 mA[1])
6: V_{N1} = - 6 V ± 10 %, $-I_{N1}$ = 3.3-9.5 mA[1])
7: V_{N2} = - 6 V ± 10 %, $-I_{N2}$ = 3.3-9.5 mA[1])
} Nominal value of the current

INPUT-SIGNAL REQUIREMENTS[2])

INPUT LEVEL "NEGATIVE HIGH"

Voltage $-V_W$ = max. V_N

Current $-I_W = \text{min.} \dfrac{I_Q + 6.1}{33}$ mA[1])

INPUT LEVEL "NEGATIVE LOW"

I_W = min. 0.07 mA[1])
Limiting value V_W = max. 10 V
Input capacitance: about 20 pF

---

[1]) The sign is positive when the current flows towards the circuit.

[2]) These data are derived from the most adverse working conditions for a combination of units, namely to supply voltages V_N = -5.4 V and V_P = +6.6 V. Unless differently specified, all the voltage and current figures quoted represent absolute maximum values.

OUTPUT CHARACTERISTICS [2])

INPUT LEVEL "NEGATIVE HIGH"

Amplitude	$-V_Q$	= $-V_W$ + approx. 0.3 V
Load current	$-I_Q$	= max. +33 I_W +6.1 mA [1])
	$-I_T$	= max. +33 I_W +5.2 mA [1])
Limiting value	I_Q	= max. 3.3 mA [1])
	I_T	= max. 2.9 mA [1]) at $-V_T$ = 0.5 V

INPUT LEVEL "NEGATIVE LOW"

Amplitude	$-V_Q$	= $-V_W$ + max. 0.3 V
Load current	I_Q	= max. 2.2 mA [1])

Maximum capacitive load for high-speed operation: 1000 pF.

When the maximum capacitive and resistive loads are applied simultaneously, some reduction in maximum switching speed may occur.

SWITCHING TIMES

A square-wave input signal is assumed with an amplitude of min. 3.8 V.

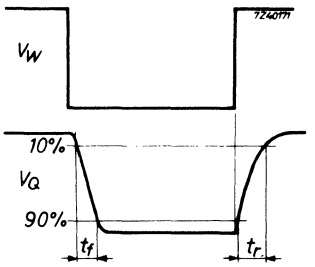


Fig.22.

UNIT UNLOADED

Fall time	t_f	= max. 0.1 μsec
Rise time	t_r	= max. 0.1 μsec

OUTPUT IMPEDANCE

Positive-going output voltage	R_i	= approx. 2000 Ω
Negative-going output voltage	R_i	= max. 0.03 Zg

(Z_g being the generator impedance of the unit driving the W terminal)

For footnotes see page 21.

EMITTER FOLLOWER/INVERTER AMPLIFIER (EF1/IA1)

type B8 940 00

(colour: yellow)

The unit B8 940 00 contains one transistor emitter-follower circuit and one transistor inverter circuit. The transistors are medium-speed switching types OC47 or equivalent items.

The two circuits, i.e. the standard circuits EF1 and IA1, can be used either independently or in combination.

Frequency range:	0-100 kc/s
Ambient-temperature range:	-20 to +60 °C
Weight:	approx. 19 g.

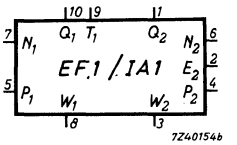


Fig. 23.

CIRCUIT DATA

Terminal 1 = Q_2 = output 2
2 = E_2 = common supply 0 V
3 = W_2 = input 2
4 = P_2 = supply +6 V
} IA1

5 = P_1 = supply +6 V - EF1
6 = N_2 = supply -6 V - IA1
7 = N_1 = supply -6 V
8 = W_1 = input 1
9 = T_1 = tapped output 1
10 = Q_1 = output 1
} EF1

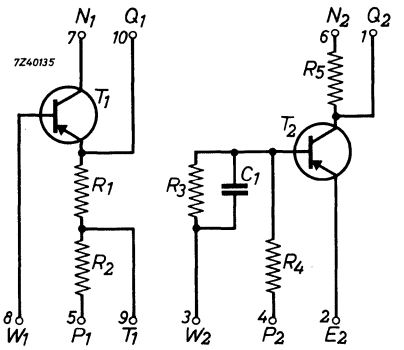


Fig. 24.

POWER SUPPLY

Terminal 2: V_{E2} = 0 V common
4: V_{P2} = +6 V ± 10%, I_{P2} = 0.12 mA[1])
5: V_{P1} = +6 V ± 10%, I_{P1} = 3.3-6.6 mA[1])
6: V_{N2} = -6 V ± 10%, $-I_{N2}$ = 0-6 mA[1])
7: V_{N1} = -6 V ± 10%, $-I_{N1}$ = 3.3-9.5 mA[1])
} Nominal value of the current

For input-signal requirements, output characteristics, switching and delay times, see B8 940 02 (2IA1) and B8 940 01 (2EF1).

1) The sign is positive when the current flows towards the circuit.

TWIN INVERTER AMPLIFIER (2IA1)

type B8 940 02

(colour: yellow)

The unit B8 940 02 contains two identical transistor inverter circuits. The transistors are medium-speed switching types OC47 or equivalent items.

The circuits constitute an inverting (NOT) function when driven by a signal on the *W* terminal.

Frequency range:	0-100 kc/s
Ambient-temperature range:	-20/+60 °C
Weight:	approx. 19 g.

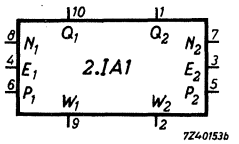


Fig.25.

CIRCUIT DATA

Terminal 1 = Q_2 = output 2
2 = W_2 = input 2
3 = E_2 = common supply 0 V (2)
4 = E_1 = common supply 0 V (1)
5 = P_2 = supply +6 V (2)
6 = P_1 = supply +6 V (1)
7 = N_2 = supply - 6 V (2)
8 = N_1 = supply - 6 V (1)
9 = W_1 = input 1
10 = Q_1 = output 1

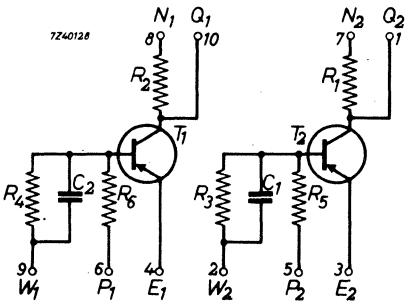


Fig.26.

POWER SUPPLY

Terminal 3: V_{E2} = 0 V common
4: V_{E1} = 0 V common
5: V_{P2} = +6 V ± 10%, I_{P1} = 0.12 mA [1])
6: V_{P1} = +6 V ± 10%, I_{P2} = 0.12 mA [1])
7: V_{N2} = -6 V ± 10%, $-I_{N1}$ = 0.6 mA [1])
8: V_{N1} = -6 V ± 10%, $-I_{N2}$ = 0.6 mA [1])

} Nominal value of the current

INPUT-SIGNAL REQUIREMENTS [2])

AC INPUT SIGNAL

Transistor conducting

Voltage	$-V_W$ = min. 3.8 V
limiting value	= max. 10 V
Input impedance:	equivalent to a capacitance of about 400 pF

Transistor non-conducting

Voltage	$-V_W$ = max. 0.3 V

DC INPUT SIGNAL

Transistor conducting

Voltage	$-V_W$ = min. 3.8 V
limiting value	= max. 10 V
Current	I_W = min. 0.6 mA [1])

Transistor non-conducting

Voltage	$-V_W$ = max. 0.3 V
limiting value	V_W = max. 10 V

OUTPUT CHARACTERISTICS [2])

TRANSISTOR CONDUCTING

Voltage	$-V_Q$	= max. 0.2 V
Load current	$-I_Q$	= max. 4.3 mA[1])
		= max. 10 mA[1]) when the N terminal is floating

TRANSISTOR NON-CONDUCTING

Voltage	$-V_Q$	= min. 3.8 V
		= max. V_N
Load current	I_Q	= max. 1.4 mA[1]) when the N terminal is floating

Maximum capacitive load for high-speed operation: 2000 pF.

When the maximum capacitive and resistive loads are applied simultaneously, some reduction in maximum switching speed may occur.

SWITCHING AND DELAY TIMES

A square-wave input signal is assumed.

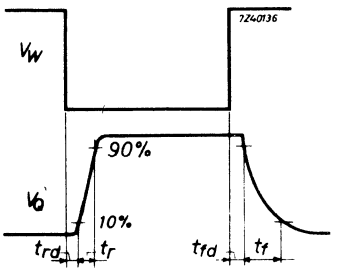


Fig.27.

UNIT UNLOADED

Rise time	t_r	= max. 0.3 μsec
Rise delay	t_{rd}	= max. 0.1 μsec
Fall time	t_f	= max. 2 μsec
Fall delay	t_{fd}	= max. 0.6 μsec

OUTPUT IMPEDANCE

Positive-going output voltage	R_i	= 100 Ω
Negative-going output voltage	R_i	= 1000 Ω

---

[1]) The sign is positive when the current flows towards the circuit.

[2]) These data only apply to the most adverse working conditions for a combination of units, namely to supply voltages V_N = -5.4 V and V_P = +6.6 V. Unless differently specified, all the voltage and current figures quoted represent absolute maximum values.

TWIN NEGATIVE GATE (2.2N1)

type B8 930 01

(colour: orange)

The unit B8 930 01 contains two two-input germanium-diode gates, that perform an AND logical operation on negative input-voltage signals.

The two gate circuits are identical and can be used separately or combined into a multiple-input gate by interconnecting the output terminals Q_1 and Q_2. In this latter case, only one negative supply terminal should be used.

Frequency range:	0-100 kc/s
Ambient-temperature range:	-20 to +60 °C
Weight:	approx. 20 g

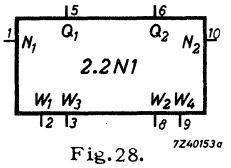


Fig.28.

CIRCUIT DATA

Terminal 1 = N_1 = supply -6 V (1)
2 = W_1 = input 1
3 = W_3 = input 3
4 = not connected
5 = Q_1 = output 1
6 = Q_2 = output 2
7 = not connected
8 = W_2 = input 2
9 = W_4 = input 4
10 = N_2 = supply -6 V (2)

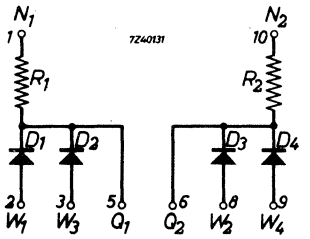


Fig.29.

POWER SUPPLY

Terminal 1: V_{N1} = -6 V ± 10%, $-I_{N1}$ = 0-0.5 mA[1])
10: V_{N2} = -6 V ± 10%, $-I_{N2}$ = 0-0.5 mA[1])
} Nominal value of the current

INPUT-SIGNAL REQUIREMENTS[2])

CURRENT

For the input terminal W_N having the least negative voltage level:
I_{Wn} = max. 0.48 mA[1]) (W_n terminal at 0 V) +
+ max. 0.04 mA[1]) for each other W terminal at -6 V (I_Q = 0).

VOLTAGE

Under all circumstances normally encountered when the unit is used in conjunction with other circuit blocks:

$V_{Wn} = V_Q$ + (0.1 to 0.5) V, dependent on the input current I_{Wn}.

---

[1]) The sign is positive when the current flows towards the circuit.

[2]) These data only apply to the most adverse working conditions for a combination of units, namely to a supply voltage V_N = -5.4 V. Unless differently specified, all the voltage and current figures quoted represent absolute maximum values.

OUTPUT CHARACTERISTICS [2])

CURRENT

At $-V_Q$ = 0.3 V, I_Q = max. 0.48 mA[1]) +
+ max. 0.04 mA[1]) for each other W terminal at -6 V.

OUTPUT LOAD IMPEDANCE

When V_Q is positive-going, the output load impedance approximates the output impedance of the driving circuit. When V_Q is negative-going, the output load impedance is max. 13 kΩ.

LIMITING VALUES

Current through conducting diode I_{W_C} = max. 10 mA.
Voltage between terminals N and W = max. 30 V.

TWIN NEGATIVE GATE (2.3N1)

type B8 930 00

(colour: orange)

The unit B8 930 00 contains two three-input germanium-diode gates, that perform an AND logical operation on negative input-voltage signals.

The two gate circuits are identical and can be used separately or combined into a multiple-input gate by interconnecting the output terminals Q_1 and Q_2. In this latter case, only one negative supply terminal should be used.

Frequency range	0-100 kc/s
Ambient-temperature range	-20 to +60 °C
Weight	approx. 20 g.

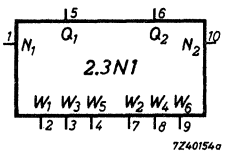


Fig. 30.

CIRCUIT DATA

Terminal 1 = N_1 = supply -6 V (1)
2 = W_2 = input 1
3 = W_3 = input 3
4 = W_5 = input 5
5 = Q_1 = output 1
6 = Q_2 = output 2
7 = W_2 = input 2
8 = W_4 = input 4
9 = W_6 = input 6
10 = N_2 = supply -6 V (2)

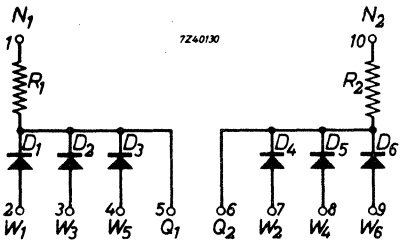


Fig. 31.

POWER SUPPLY

Terminal 1: V_{N1} = -6 V ± 10 %, $-I_{N1}$ = 0-0.5 mA [1])
10: V_{N2} = -6 V ± 10 %, $-I_{N2}$ = 0-0.5 mA [1]) } Nominal value of the current

INPUT-SIGNAL REQUIREMENTS [2])

CURRENT

For the input terminal W_n having the least negative voltage level:

I_{Wn} = max. 0.48 mA [1]) (W_n terminal at 0 V) +
+ max. 0.04 mA [1]) for each other W terminal at -6 V (I_Q = 0).

VOLTAGE

Under all circumstances normally encountered when the unit is used in conjunction with other circuit blocks:

$V_{Wn} = V_Q$ + (0.1 to 0.5) V,

dependent on the input current I_{Wn}.

---

[1]) The sign is positive when the current flows towards the circuit.

[2]) These data only apply to the most adverse working conditions for a combination of units, namely to a supply voltage V_N = -5.4 V. Unless differently specified, all the voltage and current figures quoted represent absolute maximum values.

OUTPUT CHARACTERISTICS[2])

CURRENT

At $-V_Q$ = 0.3 V, I_Q = max. 0.48 mA[1]) +
+ max. 0.04 mA[1]) for each other W terminal at -6 V.

OUTPUT LOAD IMPEDANCE

When V_Q is positive-going, the output load impedance approximates the output impedance of the driving circuit. When V_Q is negative-going, the output load impedance is max. 13 kΩ.

LIMITING VALUES

Current through conducting diode I_{Wc} = max. 10 mA
Voltage between terminals N and W: max. 30 V.

TWIN POSITIVE GATE (2.2P1)

type B8 930 03

(colour: orange)

The unit B8 930 03 contains two two-input silicon-diode gates, that perform an OR logical operation on negative input-voltage signals.

The two gate circuits are identical and can be used separately or combined into a multiple-input gate by interconnecting the output terminals Q_1 and Q_2. In this latter case, only one positive supply terminal should be used.

Frequency range	0-100 kc/s
Ambient-temperature range	-20 to +60 °C
Weight	approx. 20 g.

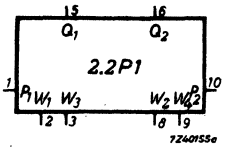


Fig.32.

CIRCUIT DATA

Terminal 1 = P_1 = supply +6 V (1)
2 = W_1 = input 1
3 = W_3 = input 3
4 = not connected
5 = Q_1 = output 1
6 = Q_2 = output 2
7 = not connected
8 = W_2 = output 2
9 = W_4 = input 4
10 = P_2 = supply +6 V (2)

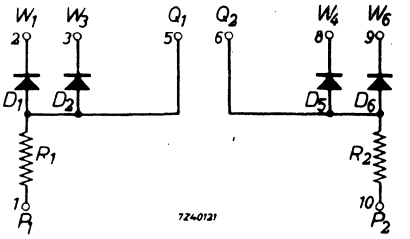


Fig.33.

POWER SUPPLY

Terminal 1: V_{P1} = 6 V ± 10 %, I_{P1} = 0.05-0.1 mA [1])
10: V_{P2} = 6 V ± 10 %, I_{P2} = 0.05-0.1 mA [1]) } Nominal value of the current

INPUT-SIGNAL REQUIREMENTS AND OUTPUT CHARACTERISTICS [2])

CURRENT

For the input terminal W_n having the most negative voltage level:

$-I_{Wn}$ = approx. I_Q + max. 0.07 mA [1]) (at $-V_Q$ = 1 V)
Load current I_Q = approx. $-I_{Wn}$ - 0.07 mA [1])

VOLTAGE

Under all circumstances normally encountered when the unit is used in conjunction with other circuit blocks:

$$-V_{Wn} = -V_Q + (0.4 \text{ to } 1) \text{ V},$$

dependent on the input current I_{Wn}.

---

[1]) The sign is positive when the current flows towards the circuit.

[2]) These data only apply to the most adverse working conditions for a combination of units, namely to a supply voltage V_P = +6.6 V. Unless differently specified, all the voltage and current figures quoted represent absolute maximum values.

OUTPUT LOAD IMPEDANCE

When V_Q is negative-going, the output load impedance approximates the output impedance of the driving circuit. When V_Q is positive-going, the output load impedance is max. 130 kΩ.

LIMITING VALUES

Current through conducting diode: I_{WC} = max. 10 mA
Voltage between terminals P and W: max. 30 V.

TWIN POSITIVE GATE (2.3P1)

type B8 930 02

(colour: orange)

The unit B8 930 02 contains two three-input silicon-diode gates, that perform an OR logical operation on negative input-voltage signals.

The two gate circuits are identical and can be used separately or combined into a multiple-input gate by interconnecting the output terminals Q_1 and Q_2. In this latter case, only one positive supply terminal should be used.

Frequency range	0-100 kc/s
Ambient temperature range	-20 to +60 °C
Weight	approx. 20 g

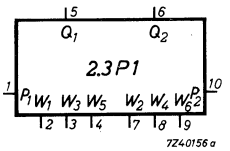


Fig. 34.

CIRCUIT DATA

Terminal 1 = P_1 = supply +6 V (1)
2 = W_1 = input 1
3 = W_3 = input 3
4 = W_5 = input 5
5 = Q_1 = output 1
6 = Q_2 = output 2
7 = W_2 = input 2
8 = W_4 = input 4
9 = W_6 = input 6
10 = P_2 = supply +6 V (2)

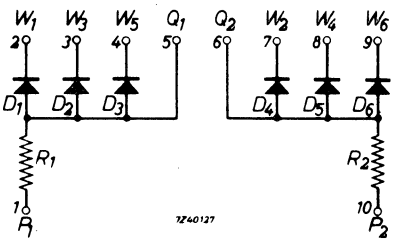


Fig. 35.

POWER SUPPLY

Terminal 1: V_{P1} = 6 V ± 10 %, I_{P1} = 0.05-0.1 mA [1]) } Nominal value of the current
10: V_{P2} = 6 V ± 10 %, I_{P2} = 0.05-0.1 mA [1]) }

INPUT-SIGNAL REQUIREMENTS AND OUTPUT CHARACTERISTICS [2])

CURRENT

For the input terminal W_n having the most negative voltage level:

$-I_{Wn}$ = approx. I_Q + max. 0.07 mA [1]) (at $-V_Q$ = 1 V)
Load current I_Q = approx. $-I_{Wn}$ - 0.07 mA [1])

VOLTAGE

Under all circumstances normally encountered when the unit is used in conjunction with other circuit blocks:

$$-V_{Wn} = -V_Q + (0.4 \text{ to } 1) \text{ V},$$

dependent on the input current I_{Wn}.

---

[1]) The sign is positive when the current flows towards the circuit.

[2]) These data only apply to the most adverse working conditions for a combination of units, namely to a supply voltage V_P = +6.6 V. Unless differently specified, all the voltage and current figures quoted represent absolute maximum values.

OUTPUT LOAD IMPEDANCE

When V_Q is negative-going, the output load impedance approximates the output impedance of the driving circuit. When V_Q is positive-going, the output load impedance is max. 130 kΩ.

LIMITING VALUES

Current through conducting diode: $-I_{WC}$ = max. 10 mA
Voltage between terminals P and W: max. 30 V.

TWIN INVERTER AMPLIFIER (2IA2)

type B8 940 05

(colour yellow)

The unit B8 940 05 contains two identical IA2 transistor inverter amplifier circuits, that constitute an inverting function with an appreciable power amplification between input and output. The unit has especially been designed to amplify the weak output signals originating from a diode gate circuit, whilst it can also be used as a driver for power stages. The transistors used are medium-speed OC47 types or equivalent items.

Frequency range:	0-100 kc/s
Ambient-temperature:	-20 to +60 °C
Weight:	approx. 21 g.

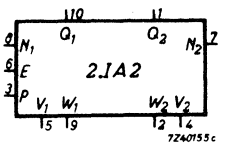


Fig.36.

CIRCUIT DATA

Terminal 1 = Q_2 = output 2
2 = Q_1 = output 1
3 = W_2 = input 2
4 = W_1 = input 1
5 = N_4 = supply -6 V[1])
6 = N_3 = supply -6 V[1])
7 = N_2 = supply -6 V[1])
8 = N_1 = supply -6 V[1])
9 = P = supply +6 V
10 = E = common supply 0 V

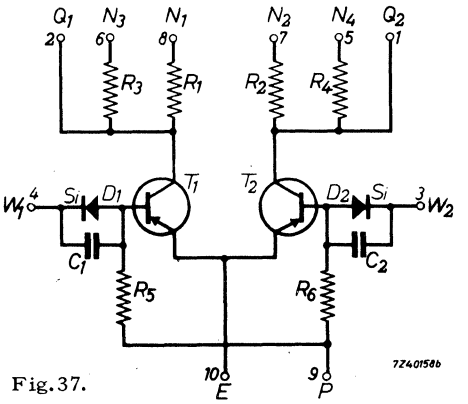


Fig.37.

POWER SUPPLY

Terminal 5:	V_{N4} = -6 V ± 10%, $-I_{N4}$ = 0-4 mA[2])	Nominal value of the current
6:	V_{N3} = -6 V ± 10%, $-I_{N3}$ = 0-4 mA[2])	
7:	N_2 = -6 V ± 10%, $-I_{N2}$ = 0-2 mA[2])	
8:	N_1 = -6 V ± 10%, $-I_{N1}$ = 0-2 mA[2])	
9:	P = +6 V ± 10%, I_P = 0.2 mA[2])	
10:	E = 0 V common	

INPUT SIGNAL DATA (W input)[3])

APPLICATION 1: (use as gate amplifier): IA2 after a standard negative (N1) gate, or standard negative (N1) gate followed by a standard positive (P1) gate circuit.

In the latter case the P supply terminal of the gate may be left floating.

These standard gate circuits are incorporated in the units B8 930 00 and B8 930 01, respectively in the units B8 930 02 and B8 930 03.

TRANSISTOR CONDUCTING

Input current: $-I_W$ = min. 0.3 mA
(under these drive conditions the input voltage will reach a value $-V_{Wd}$ = max. 1 V)

TRANSISTOR NON-CONDUCTING

Input voltage: V_W = min. 0.2 V

APPLICATION 2: (use as power amplifier): IA2 driven by a grounded emitter stage with a collector resistance of 1 kΩ, connected to the -6 V supply terminal. This driving stage can be a standard IA1 circuit (incorporated in the units B8 940 00 and B8 940 02) or another IA2 circuit with both corresponding -6 V supply terminals connected to the negative supply line. In both cases the collector (Q terminal) of the driving stage is connected directly to the W terminal of the IA2.

TRANSISTOR CONDUCTING

Input current: $-I_W$ = min. 3.7 mA [2])
(under these drive conditions the input voltage will reach a value $-V_{Wd}$ = max. 1.3 V).

LIMITING VALUES:

$-I_W$ = max. 10 mA [2])
V_W = max. 10 V

OUTPUT DATA [3])

APPLICATION 1 (see above)

Transistor conducting:

Output current $-I_Q$ = max. 5.5 mA [2]) [4])
$-I_Q$ = max. 3.6 mA [2]) [5])
$-I_Q$ = max. 0 mA [2]) [6])

Output voltage $-V_Q$ = max. 0.2 V

Transistor non-conducting:

Output current I_Q = max. 0 mA [2]) [4])
I_Q = max. 0.49 mA [2]) [5])
I_Q = max. 1.5 mA [2]) [6])

Output voltage $-V_Q$ = max. 3.8 V

APPLICATION 2 (see above)

Transistor conducting:

Output current $-I_Q$ = max. 80 mA [2]) [4])
max. 74 mA [2]) [6])

Output voltage $-V_Q$ = max. 0.25 V

Transistor non-conducting

Output current I_Q = max. 0 mA [2]) [4])
I_Q = max. 1.5 mA [2]) [6])

Output voltage $-V_Q$ = max. 3.8 V

---

[1]) Use dependent on application.

[2]) The sign is positive when the current flows towards the circuit.

[3]) These data only apply to the most adverse working conditions for a combination of units, namely to supply voltages V_N = -5.4 V and V_P = +6.6 V. Unless differently specified, all the voltage and current figures quoted represent absolute maximum values.

[4]) With all N terminals floating.

[5]) With terminals N1 or N2 connected to the -6 V supply.

[6]) With terminals N1 and N3 or N2 and N4 connected to the -6 V supply.

SWITCHING AND DELAY TIMES

For application as a gate amplifier (application 1) the unit is driven from a square-wave voltage source via a standard negative (N1) gate[7]), followed by a standard positive (P1) gate[7]).

UNIT UNLOADED

Rise delay	t_{rd}	= max. 0.2 μs
Rise time	t_r	= max. 1.5 μs
Fall delay	t_{fd}	= max. 1 μs
Fall time	t_f	= max. 2.5 μs

OUTPUT IMPEDANCE

Positive-going output voltage	R_i	= 100 Ω
Negative-going output voltage	R_i	= 1000 Ω[8]).

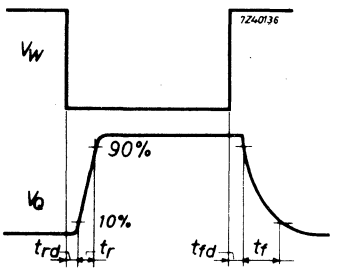


Fig. 38.

[7]) The standard N_1 gate is incorporated in the gate units B8 930 00 and B8 930 01, the standard P_1 gate is incorporated in the units B8 930 02 and B8 930 03.

[8]) All N terminals connected to the -6 V supply.

TWIN EMITTER FOLLOWER (2EF2)

type B8 940 03

(colour: yellow)

The unit B8 940 03 contains two identical EF2 transistor emitter follower circuits that constitute a buffer amplifier function (non-inverting) and is especially to be driven by a negative or positive gate circuit.

Frequency range:	0-100 kc/s
Ambient temperature:	-20 to +60 °C
Weight:	approx. 21 g.

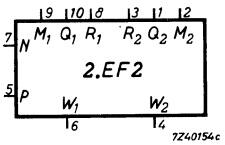


Fig.39.

CIRCUIT DATA

Terminal 1 = Q_2 = output 2
2 = M_2 = clamp diode 2
3 = R_2 = diode output 2
4 = W_2 = input 2
5 = P = supply +6 V
6 = W_1 = input 1
7 = N = supply -6 V
8 = R_1 = diode output 1
9 = M_1 = clamp diode 1
10 = Q_1 = output 1

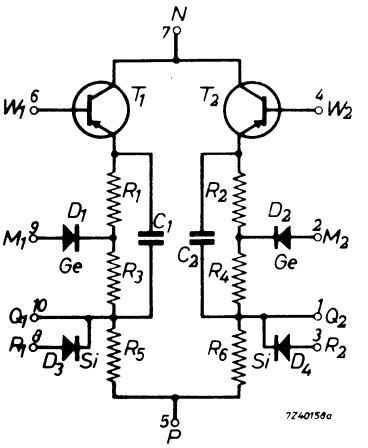


Fig.40.

POWER SUPPLY

Terminal 5: V_P = +6 V ± 10%, I_P = 3.5- 4 mA[1])
7: V_N = -6 V ± 10%, $-I_N$ = 4-12 mA[1])
} Nominal value of the current

INPUT SIGNAL DATA (W input)[2])

DC INPUT:

The unit is to be driven from a standard negative gate N1[3]) or from a negative-gate-positive gate N1-P1[3]) sequence.

Limiting values of the input voltage	$-V_W$ = max. $-V_N$
	V_W = max. 10 V
Input capacitance:	approx. 50 pF

---

[1]) The sign is positive when the current flows towards the circuit.

[2]) These data have been derived from the most adverse working conditions for a combination of units namely to supply voltages V_N = -5.4 V and V_P = +6.6 V. Unless specified otherwise, the voltages and currents quoted represent absolute maximum values.

[3]) The standard N_1 gate is incorporated in the gate units B8 930 00 and B8 930 01, the standard P_1 gate is incorporated in the units B8 930 02 and B8 930 03.

2.EF2

OUTPUT DATA[1])

The unit is designed to drive a grounded emitter transistor directly at the base. By connecting the built-in anti-bottoming diode (D_1 or D_2) via the M terminal to the collector of the driven grounded-emitter stage, the hole-storage effects in this stage are avoided. In this way short transients are maintained.

The output signal is normally taken from the Q terminal. When a flip-flop is to be set of reset by an EF2, normally the R output is used, the memory property of the flip-flop then being maintained.

In these cases the EF2 output signal can be represented by an equivalent signal source with a given EMF and internal resistance R_i in series.

EF2 driven by a standard N1[2]) negative gate:

input to the gate:	EMF	R_i	terminal	output voltage and current
"negative high"	-2.2 V	620 Ω	Q	V_Q = -0.5 V I_Q = max. 2.75 mA[3])
	-2.0 V	870 Ω	R	V_R = -0.5 V I_R = max. 1.7 mA[3])
"negative low"	+0.2 V	330 Ω	Q	V_Q = +0.2 V I_Q = max. 0 mA[3])

EF2 driven by a standard N1[2]) negative gate, followed by a standard P1[2]) positive gate:

input to the gate	EMF	R_i	terminal	output voltage and current
"negative high"	-1.0 V	600 Ω	Q	V_Q = -0.45 V I_Q = max. 0.92 mA[3])
	-0.8 V	850 Ω	R	V_R = -0.4 V I_R = max. 0.43 mA[3])
"negative low"	+0.5 V	330 Ω	Q	V_Q = 0.2 V $-I_Q$ = max. 0.8 mA[3])

SWITCHING AND DELAY TIMES

Below the switching and delay times are given for a standard application of the EF2 circuit; i.e. a square-wave driven N1-P1 gate sequence[2]) driving an OC47 grounded emitter stage via the EF2 on the Q output. The corresponding M terminal is connected to the collector of the OC47.

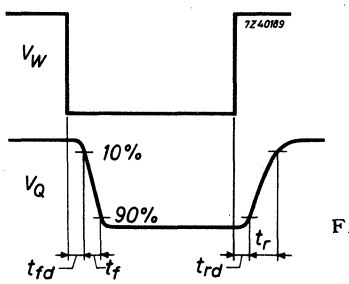


Fig.41.

The switching and delay times are given for two values of the collector current, taken from the OC47 transistor.

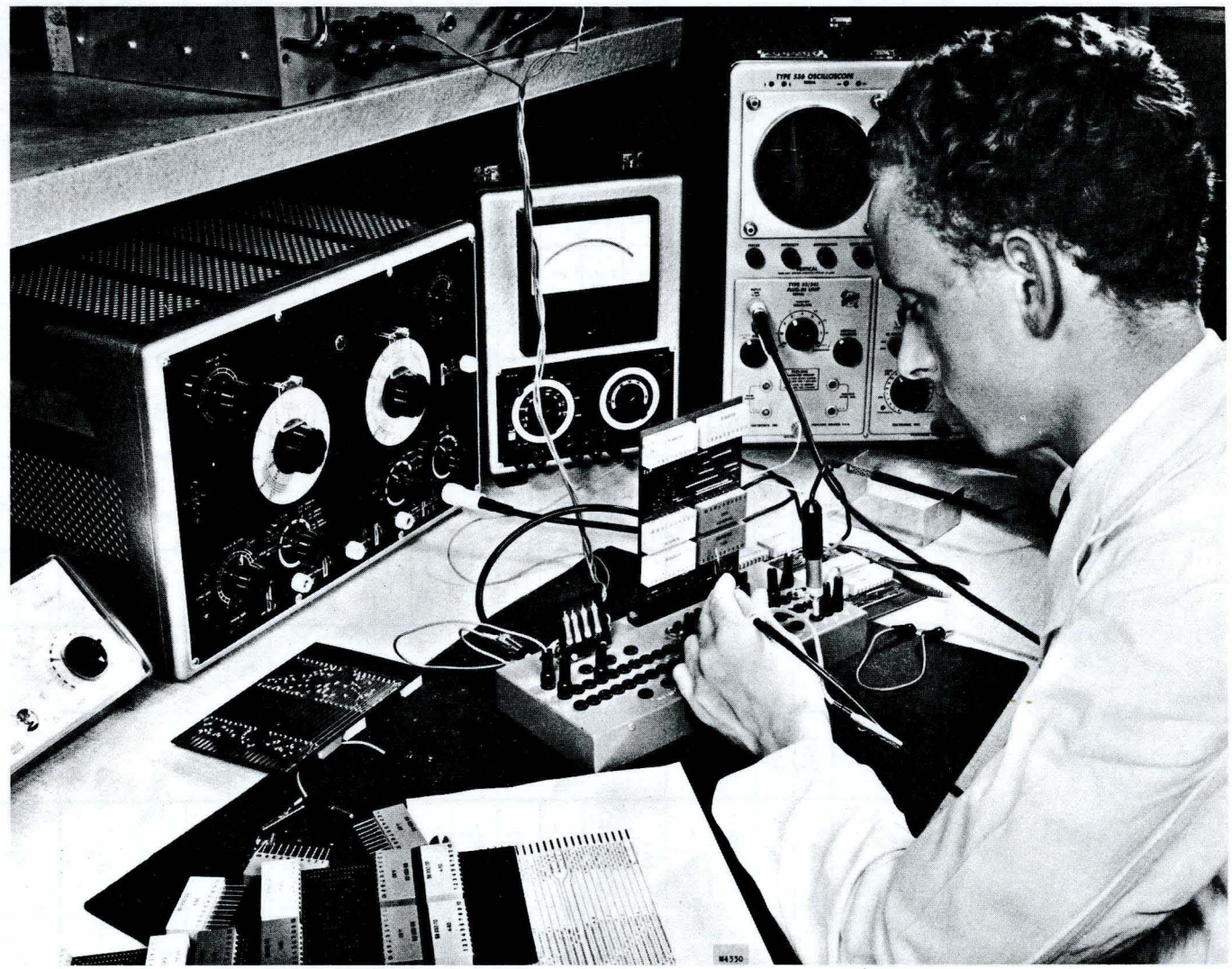
	$I_{C\,OC47}$ = 6 mA	$I_{C\,OC47}$ = 20 mA
Rise delay	t_{rd} = max. 0.3 μs	max. 0.3 μs
Rise time	t_r = max. 0.3 μs	max. 1.5 μs
Fall delay	t_{fd} = max. 2.0 μs	max. 3.5 μs
Fall time	t_f = max. 0.5 μs	max. 1.2 μs

---

[1]) These data have been derived from the most adverse working conditions for a combination of units namely to supply voltages V_N = -5.4 V and V_P = +6.6 V. Unless specified otherwise the voltages and currents quoted represent absolute maximum values.

[2]) The standard N1 gate is incorporated in the gate units B8 930 00 and B8 930 01, the standard P1 gate is incorporated in the units B8 930 02 and B8 930 03.

[3]) The sign is positive when the current flows towards the circuit.



Circuit blocks used in a laboratory set-up.

Loading Table

Preceding unit or chain of preceding units			Driving unit		via	Maximum number of driven units (n_{max})								
			Type	Output		FF1 (W_1,W_2)	FF1 (A_1, A_2)	IA1 (W)	IA2 (W)	EF1 (W)	EF2 (W)	PS1 (W)	OS1 (A_2)	N_1 (W)
			FF1			1[1]	4	1	0	1	3	4[2]	4	4
			IA1			2[1]	4[3]	2	1	2	6	8[2]	4[3]	7
	N_1	OA 200	IA2*a*)			1[1]	0	1	0	1	2	2[2]	0	6
	N_1	P_1	IA2*a*)			1[1]	0	1	0	1	2	2[2]	0	6
		IA1	IA2*b*)			2[1]	4[3]	2	1	2	6	8[2]	4[3]	60
	N_1	OA 200	IA2*b*)			2[1]	0	2	1	2	6	8[2]	0	0
	N_1	P_1	IA2*b*)			2[1]	0	2	1	2	6	8[2]	0	0
N_1	OA 200	IA2*b*)	IA2*b*)			2[1]	4[3]	2	1	2	6	8[2]	4[3]	60
N_1	P_1	IA2*b*)	IA2*b*)			2[1]	4[3]	2	1	2	6	8[2]	4[3]	60
			EF1	Q		8[1]	0	6	0			25[2]	0	4
		IA1	EF1	Q		18[1]	0	12	0			50[2]	0	4
		OS1 (Q_1 output)	EF1	Q		18[1]	0	12	0			50[2]	0	4
	N_1	P_1	EF1	Q		0	0	0	0	0	0	0	0	4
			EF1	T		1	0		1				0	
		N_1	EF2	R		1	0						0	0
	N_1	P_1	EF2	R		1	0		0				0	0
		N_1	EF2	Q		1	0		1			1	0	
		N_1	EF2	Q	OC 47[6])	2[1]	4[3]	2	1	2	6	8[2]	4[3]	60
	N_1	P_1	EF2	Q		1	0		1				0	
	N_1	P_1	EF2	Q	OC 47[6])	2[1]	4[3]	2	1	2	6	8[2]	4[3]	60
			PS1			1[1]	2	1	1	1	1	4[2]	2	2
			OS1	Q_2		1[1]	0	1	0	1	3	4[2]	0	4
			OS1	Q_1		2[1]	4	2	0	2	6	8[2] /	4	4
			N_1			0	4[4])	0	1[5])	0	1	1	4[4])	0
		N_1	P_1			0	0	0	1	1[6])	1	1	0	0

*) IA2*a* = IA2 with terminals N_3 or N_4 floating
IA2*b* = IA2 with N_1 and N_3, or N_2 and N_4 connected to V_N.

//// means: not recommended.

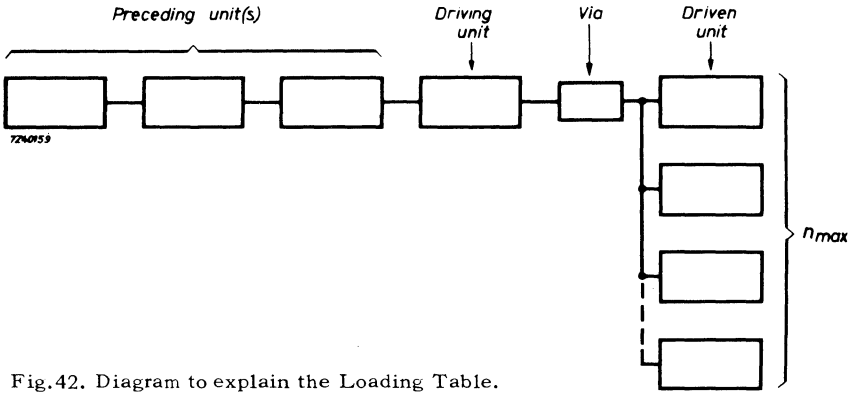


Fig.42. Diagram to explain the Loading Table.

NOTES

*P*1. Unless specified otherwise a P1 may be interposed between two units without great influence upon the loadability. "*A*" inputs of FF1, FF2 or OS1 cannot be driven from it.

[1]) Each via a 7.5 kΩ ± 5% resistor, if necessary in series with a diode OA 85, anode to driven unit.

[2]) Each via an 18 kΩ ± 5% resistor, bypassed by a 330 pF capacitor.

[3]) Only if the driving unit is driven by an FF1, FF2, PS1 or the Q_2 terminal of an OS1.

[4]) Only if the N1 gate is driven by an FF1, FF2, PS1, the Q_2 terminal of OS1, IA1 or IA2 driven by one of these units. The maximum speed is $\frac{30 \text{ kc/s}}{\text{number of units}}$.

[5]) Via a diode OA 200, cathode to N1, anode to IA2, and bypassed by a 1500 pF capacitor.

[6]) Common-emitter stage with a 1 kΩ collector resistor.

Notes on Application

This chapter contains some general and specific remarks on the application of circuit blocks.

FLIP-FLOP

DC INPUT SIGNAL

The flip-flop FF1 can be set and reset on the *W* terminals by a negative and positive DC level respectively. Attention should be paid to the *W* inputs being directly connected to the transistor base. When driven by a low-impedance source (e.g. the direct output of an emitter-follower or the negative power supply line) the transistor may be seriously overdriven and hence destroyed. The maximum permissible input current should therefore never be exceeded!

If the memory property of the flip-flop has to be maintained, the driving source should have a one-way action on the flip-flop; the source should therefore be connected to the *W* terminal by means of a series diode (see under: SET AND RESET CIRCUITS). In order to attain a correct cut-off voltage level for this diode, the emitter-follower units EF 1 and EF 2, which can be used as driving sources for the flip-flop, are provided with a tapped output. The voltage level on the tapping has the required value if the emitter-follower is driven by a "0" (negative low) signal.

The FF 2 circuit block comprises the series diode (M_1 and M_2 output terminals).

CASCADING OF FLIP-FLOPS

With *n* cascaded flip-flops FF 1 it is possible to construct frequency dividers with a dividend of 2^n. When such a chain of flip-flops is used for counting, the total counting capacity amounts to 2^n as well.

By using a pulse feedback or gating principle it is possible to skip a given number of counts, so that with *n* flip-flops any dividend up to 2^n can be obtained. When a dividend of *N* is required, the minimum number of flip-flops (*n*) can be derived from:

$$2^{n-1} < N \leqslant 2^n.$$

Pulse feedback is required when $N \neq 2^n$, so that $2^n - N$ positions are skipped. The value of 2^n-*N* gives the indication to which flip-flop in the series the feedback should be applied. In Figs 63 to 68 a few examples are given. The pulse feedback is supplied by the last flip-flop to one or more of the preceding flip-flops.

Care should be taken, that the maximum permissible capacitive load of the flip-flop that supplies the feedback pulse is not exceeded. The maximum capacitive loading of the FF 1 is 2000 pF. If a 1500 pF series capacitor is used in the feedback path, 500 pF is left for external loading on that terminal (equivalent to another flip-flop). If more feedback paths are required, the signal may also be taken from the other (complementary) output terminal.

GATES

GENERAL

As mentioned before, it is immaterial which binary level is denoted by the logic value "0" or by "1", since it has no influence whatsoever on the logic design of a circuit. However, confusion may arise when gate circuits are discussed. Many designers use the words AND and OR for the basic logic functions as well as for the electronic circuits that perform these specific logic operations. The notations AND and OR should, however, be restricted to *logic functions*, since one gate circuit can perform both the AND and OR function, dependent on the designation of "0" and "1" to the voltage levels used.

For the above reasons the circuit blocks comprising gate circuits are denoted by "NEGATIVE GATE" and "POSITIVE GATE" The negative gate performs the AND function on "negative high" signals and the OR function on "negative low" signals, whilst the positive gate performs the OR function on a "negative high" signal and the AND function on a "negative low" signal (see Table below).

Signal value "1" assigned to:	Logic function performed by	
	Positive gate	Negative gate
"Negative high" level	OR	AND
"Negative low" level	AND	OR

GATE SEQUENCE: ALWAYS NEGATIVE GATE - POSITIVE GATE

Technically it is only possible to drive a positive (*P*) gate by a negative (*N*) gate. In the system where the negative high signal corresponds to binary "1", the AND - OR sequence is therefore allowed only. This means that every OR - AND combination in the logic diagram should be converted into an AND - OR combination. An example of such a conversion was already given on page 11. It may be convenient to remember that an AND-gate is an OR-gate for the antivalent signal and vice versa. At the outputs of a flip-flop a signal and its complement are simultaneously present, so that no inverter need be used when the signal is taken from a flip-flop.

CASCADING OF GATES: NO MORE THAN TWO

Cascading of more than two gates must generally be avoided. This is due to a large increase of the load on the driving unit when gates are connected in cascade, so that the signal level shift (signal loss) may amount to impracticable values.

An *N-N* or *P-P* gate sequence is generally not allowed; such a sequence can, however, always be replaced by one multiple *N* or *P* gate respectively.

After a signal has passed an *N*-gate or an *N-P* gate sequence, it must be restored by an inverter amplifier IA2, an emitter-follower EF2 or a pulse shaper PS1.

GATES WITH MULTIPLE INPUTS

In many cases gates with more than three inputs may be required. Such a gate may be composed of any number of 2- or 3-input gates. The following rules should then be observed:

(1) Interconnect the *Q*-outputs.

(2) Connect the negative supply *N* only once for the whole gate, leaving the other terminals N_1 or N_2 floating.

(3) If the newly composed gate would have more inputs than actually necessary, leave the unused inputs floating.

(4) A *P*-gate driven by an *N*-gate may have 25 inputs at maximum.

(5) When part of the number of inputs of an *N*-gate are at "0" level and the other inputs at "1" level, the supply of the leakage currents of the diodes that are cut-off is distributed over the inputs at zero level. (The maximum of this leakage current is 40 μA for every input in the "1" position.) This may give rise to a considerable increase of the load at these inputs. (See also: Technical Data.)

POSITIVE GATES

The same general rules for *N*-gates also apply to *P*-gates. It must be noted, however, that, unlike the *N*-gate, the *P*-gate may load the driving stage at both binary levels.

The terminals P_1 or P_2 of the *P*-gate may be left floating when the following stage is already equipped with a resistor from the input to the positive supply voltage. This is the case with the flip-flop FF1, the one-shot multivibrator OS1 and the inverter-amplifiers IA1 and IA2.

When a *P*-gate is driven by an *N*-gate, the number of *P*-gate inputs may not exceed 25. On the other hand, an *N*-gate may be loaded by only one *P*-gate.

MORE THAN ONE GATE DRIVEN BY MORE THAN ONE FLIP-FLOP

The Loading Table indicates the number of gates with which the other circuit blocks may be loaded. It should be remembered, however, that *an N-gate only presents a "load" if it produces a negative low signal at its output.* When several gate inputs carry a negative low signal simultaneously, the load is divided among the driving sources. When a number of gates is driven by a number of flip-flops, it may therefore be allowed to connect each flip-flop to a number of gates greatly *exceeding* that given in the Loading Table. That is because the effective loading may be far less than the actual number of gates. This must be checked carefully for every possible state of the circuit.

The same applies, as a matter of course, for other driving sources.

VOLTAGE LEVELS IN GATE CIRCUITS

Due to the voltage drop across the diodes of the gates, a voltage level shift will occur in every gate, so that the signal, after having passed one or more gates, is no longer in agreement with the level standards of the input signals. In the Loading Table this effect has already been taken into account. When a combination of gates that is not covered by the Loading Table must be used, the following information should be borne in mind:

(1) A germanium diode in an *N*-gate causes a level shift of - 0.1 V to - 0.5 V.

(2) A silicon diode in a *P*-gate causes a level shift of +0.4 V to +1.0 V.

(3) A common emitter stage needs - 0.2 V to - 0.4 V on its base for the conducting state and approx. +0.2 V for its cut-off state [1]).

(4) the collector-voltage level of a conducting common emitter stage ("0" output) has to be taken as - 0.05 to - 0.2 V [1]).

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[1]) Related to the type of semiconductor as used in the circuit blocks and dependent on the current flowing through the diodes. In calculations on the levels the most unfavourable limit of the values given has to be applied.

CURRENTS IN GATE CIRCUITS

Since the forward resistance of a conducting diode and the input impedance of a common emitter transistor, when driven into the conducting state, is very low, a strong gate current may occur, which may overload or damage the circuit elements.

On the other hand, the generator impedance of an "open" gate is high, resulting sometimes in too low an available driving current for a given stage. When applying other combinations, such as given in the examples below or in the Loading Table, these points have therefore to be investigated.

ONE-SHOT MULTIVIBRATOR OS1

The one-shot multivibrator OS1 is intended to produce a pulse of definite length for providing a time delay. Both a positive and a negative pulse are available at the outputs. It should be noted that at the Q_2 terminal the maximum permissible load current is appreciably lower than that at the Q_1 terminal, whilst the rise time of the pulse at the Q_2 terminal is higher than that at the Q_1 terminal.

It is not recommended to use the OS1 for delays that exceed the values given in the graph (see: Technical Data), i.e. longer than 1 msec, since in this case the OS1 is more sensitive to spurious signals induced on the supply line. Moreover, the use of electrolytic capacitors would be required, which are less stable during life and may show a considerable leakage current. For long delays it is therefore recommended to use a frequency divider fed from a fixed frequency, such as the A.C. mains.

When the OS1 is used for long delays the negative supply line should be bypassed close to the unit by a large capacitor.

TRANSIENTS AND DELAY TIMES

Although all circuit blocks function properly in any permitted sequence at frequencies up to 100 kc/s, practical considerations may cause a reduction of this speed, This may happen when the total delay in a chain of cascaded circuits is too long for the specific application. It must be examined on the basis of the switching times and delay times as given under the Technical Data.

As a typical example an 8-stage binary counter with flip-flops FF1 will be considered. From the Technical Data it follows, that in this counter a total delay of $8 \cdot (t_{rd} + t_r) = 8.8\ \mu s$ occurs. If the output signal of the 8^{th} flip-flop should coincide with the input pulse of the counter for at least $2\ \mu s$, it is required for this input pulse to have a duration of minimum $8.8\ \mu s + 2\ \mu s = 10.8\ \mu s$. This requirement reduces the maximum operational frequency in the application at issue to approximately 46 kc/s.

The transients in a loaded switching circuit can be calculated from the Technical Data.

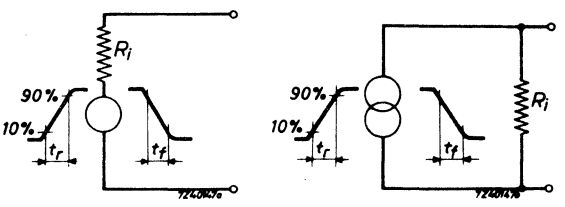


Fig.43. Equivalent diagrams of active circuit blocks.

The intrinsic switching times given in these data always apply to the unloaded condition. Generally they remain unaffected under conditions of resistive loading, whereas a capacitive load increases the switching times.

The actual switching time of a loaded circuit can easily be calculated from the equivalent diagrams shown in Fig.43. The unit can be represented by a step voltage or current source in combination with the internal (output) impedance of the unit. The value of this output impedance is given under the Technical Data of the unit under consideration. The total rise time and fall time of the output voltage are approximately equal to:

$$t_{r\,tot} = \sqrt{t_r^2 + (2.2\,\tau)^2} \quad \text{and} \quad t_{f\,tot} = \sqrt{t_f^2 + (2.2\,\tau)^2}$$

in which:

t_r = the intrinsic rise time of the unit,
t_f = the intrinsic fall time of the unit,
τ = the time constant of the load and internal resistance of the unit.

When the load consists of the parallel circuit of a resistive part R_l and a capacitive part C_l (which will mostly be the case)

$$\tau_l = \frac{R_l \cdot R_i}{R_l + R_i} \cdot C_l,$$

in which R_i is the internal resistance of the unit.

Some Practical Circuits

In this section some practical examples are given for the application of circuit blocks. Since most circuit blocks comprise twin units or two separate functional units in certain cases only half the symbol is given.

AMPLIFIER CIRCUITS FOR GATE SIGNALS

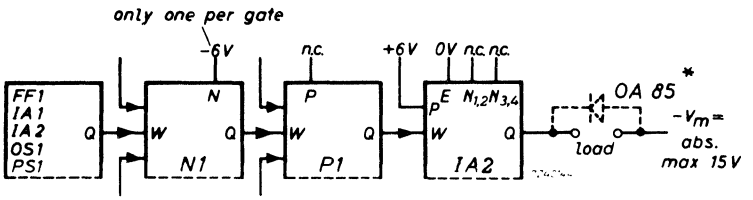


Fig.44. I_{load} = max. 5.5 mA.

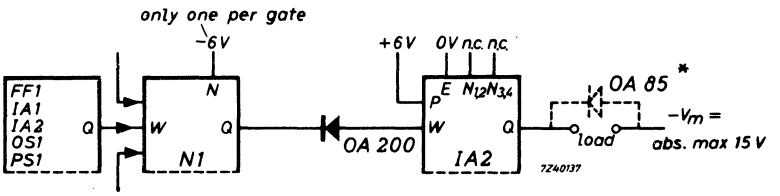


Fig.45. I_{load} = max. 5.5 mA.

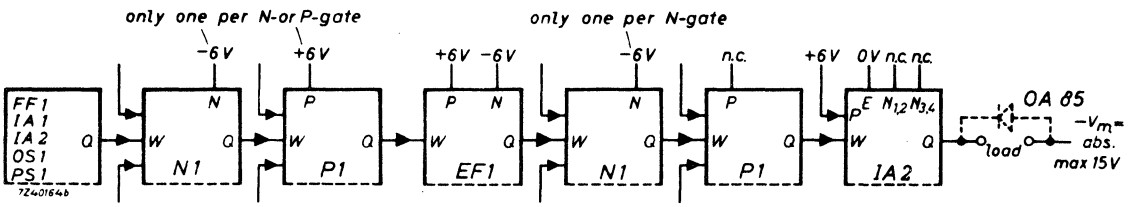


Fig.46. I_{load} = max. 5.5 mA.

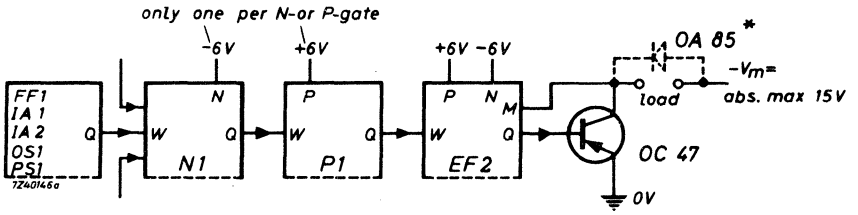


Fig.47.

$-V_m$ = 6 V ± 10 %
I_{load} = max. 22 mA
R_{load} = min. 290 Ω ± 10 %

$-V_m$ = 12 V ± 15 %
I_{load} = max. 20 mA
R_{load} = min. 560 Ω ± 10 %

*) In case of inductive loading.

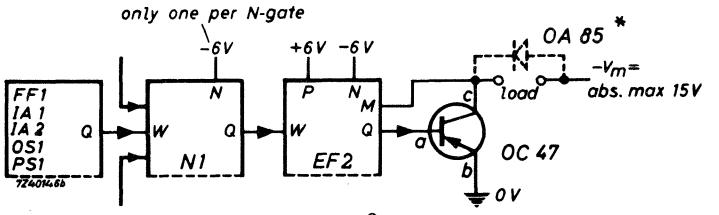


Fig.48[2]).

$-V_m$	=	6 V ± 10 %	$-V_m$	=	12 V ± 15 %
I_{load}	= max.	35 mA	I_{load}	= max.	35 mA
R_{load}	= min.	175 Ω ± 10 %	R_{load}	= min.	375 Ω ± 10 %

In the circuits of Fig.47 and 48 the output transistor OC 47 can be replaced by the EF1 circuit, as follows.

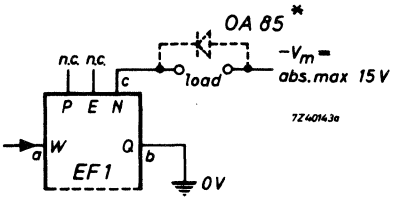


Fig.49.

POWER OUTPUT CIRCUITS

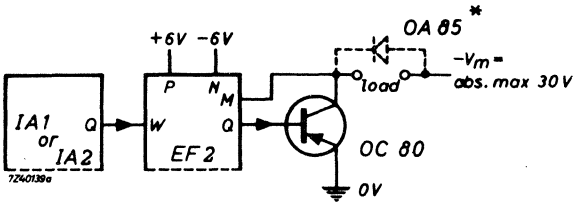


Fig.50[2]).

$-V_m$	=	12 V ± 15 %	$-V_m$	=	24 V ± 15 %
I_{load}	= max.	230 mA[1])	I_{load}	= max.	230 mA[1])
R_{load}	= min.	50 Ω ± 10 %	R_{load}	= min.	100 Ω ± 10 %
W_o	= max.	2.7 W	W_o	= max.	5.4 W

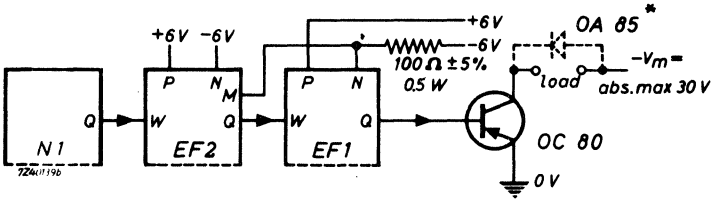


Fig.51.

$-V_m$	=	12 V ± 15 %	$-V_m$	=	24 V ± 15 %
I_{load}	= max.	230 mA[1])	I_{load}	= max.	230 mA[1])
R_{load}	= min.	50 Ω ± 10 %	R_{load}	= min.	100 Ω ± 10 %
W_o	= max.	2.7 W	W_o	= max.	5.4 W

*) In case of inductive loading.

[1]) At nominal supply voltages.

[2]) All N terminals of the IA2 connected to the -6 V supply.

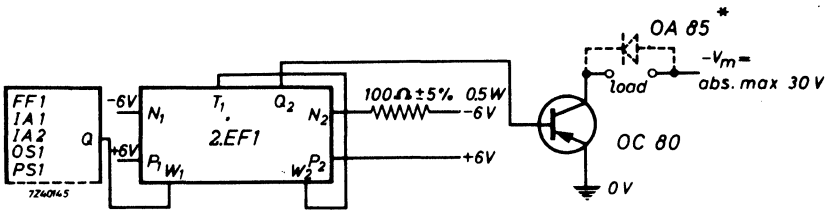


Fig.52.

$-V_m$	=	12 V ± 15 %	
I_{load}	=	max. 230 mA[1])	
R_{load}	=	min. 50 Ω ± 10 %	
W_o	=	max. 2.7 W	

$-V_m$	=	24 V ± 15 %
I_{load}	=	max. 230 mA[1])
R_{load}	=	min. 100 Ω ± 10 %
W_o	=	max. 5.4 W

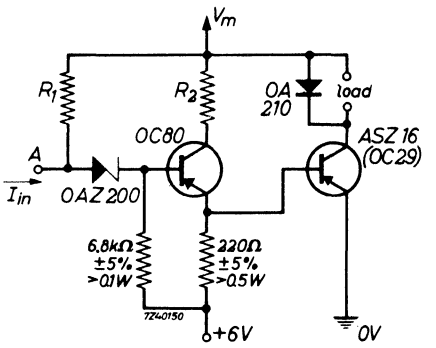


Fig.53.

$-V_m$	=	12 V ± 15 %	
R_1	=	360 Ω ± 5 %,	1 W
R_2	=	56 Ω ± 5 %,	5 W
$-I_{in}$	=	min. 50 mA	
I_{load}	=	max. 2.6 A[2])	
R_{load}	=	min. 4.2 Ω ± 10 %	
W_o	=	max. 29 W[2])	

$-V_m$	=	24 V ± 15 %
R_1	=	2.4 kΩ ± 5 %, 0.5 W
R_2	=	110 Ω ± 5 %, 10 W
$-I_{in}$	=	min. 50 mA
I_{load}	=	max. 2.9 A[2])
R_{load}	=	min. 7.9 Ω ± 10 %
W_o	=	max. 67 W[2])

If there is a preference to use an output transistor ASZ 17 or ASZ 18 instead of the ASZ 16, the stated maximum load current I_{load} and the output power W_o have to be multiplied by 0.55 and the minimum load resistance R_{load} by 1.8.

The output stage must be driven from an OC 47/ASZ 12 or a special EF1 circuit as given under Figs 47, 48 and 49 at V_m = -24 V. At V_m = -12 V only the driving circuit of Figs 48 and 49 can be used.

An alternative driver circuit for the power stage of Fig.53 can be made as follows (valid for V_m = -12 V or -24 V).

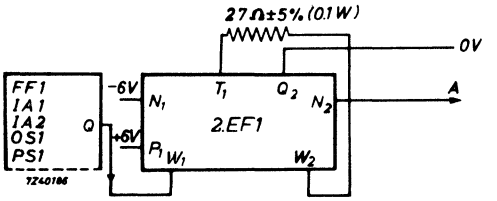


Fig.54.

*) In case of inductive loading.

1) At nominal supply voltages.

2) Nominal value.

SET AND RESET CIRCUITS

A system in which flip-flops are used, often requires a means for setting or resetting. This can be realised as indicated in the figures below.

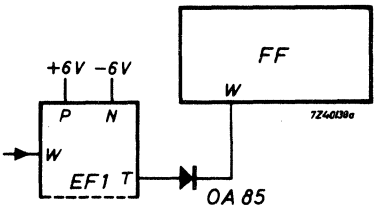


Fig.55.

Input signal for resetting: "1" (negative high)
Driving unit: FF1, IA1, IA2, OS1 or PS1
Maximum number of flip-flops: 1

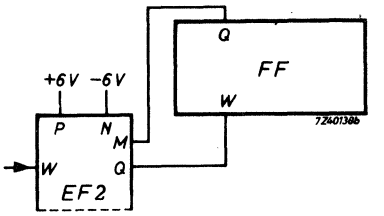


Fig.56.

Input signal for resetting: "1" (negative high)
Driving unit: *N*-gate or *N-P* gate sequence
Maximum number of flip-flops: 1

When a large number of flip-flops has to be controlled, the following arrangement can be used.

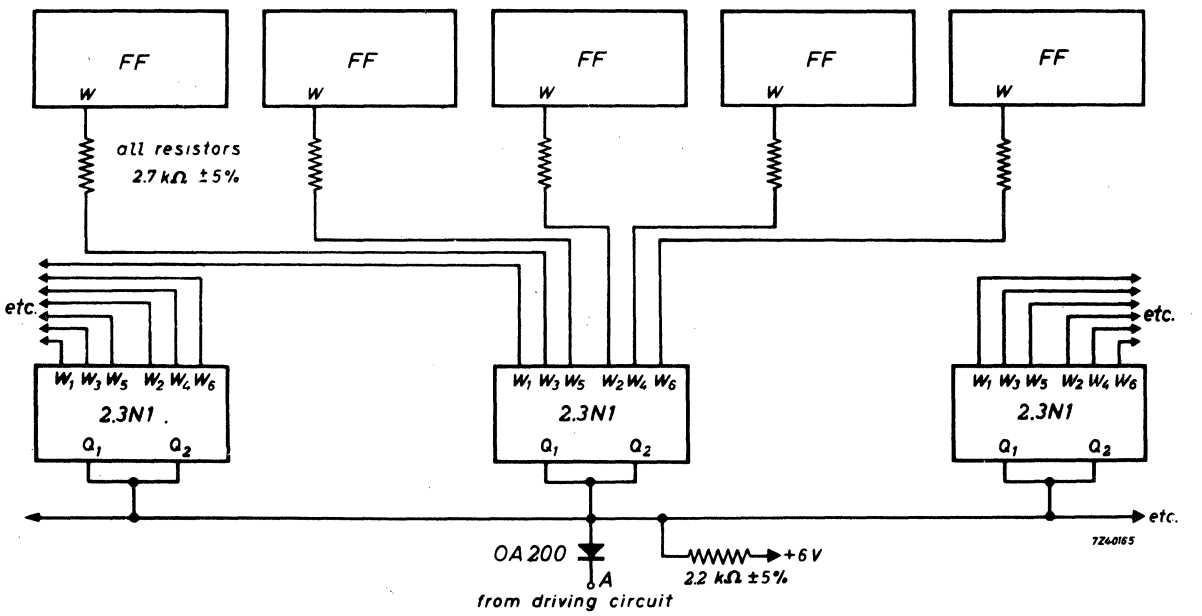


Fig.57.

The circuit of Fig.57 can be driven by the following circuits (Figs 58, 59, 60 and 61).

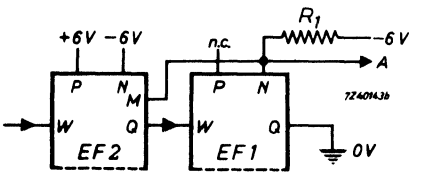


Fig.58.

Driving unit	R_1 (Ω ± 5 %)	Max. number of flip-flops
FF1, IA1, IA2, OS1, PS1	68	50
N-gate	75	45
N-P gate sequence	200	12

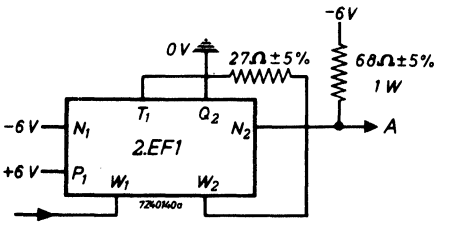


Fig.59.

(Low speed operation only.)

Input signal for resetting: "0" (negative low).
Driving unit: FF1, IA1, IA2, OS1 or PS1.
Maximum number of flip-flops: 50.

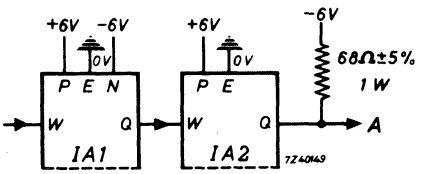


Fig.60.

Input signal for resetting: "1" (negative high).
Driving unit: FF1, IA1, IA2, OS1 or PS1.
Maximum number of flip-flops: 50.

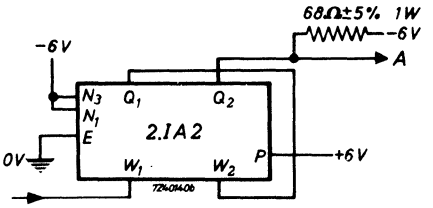


Fig.61.

Input signal for resetting: 1 (negative high)
Driving unit: *N*-gate or *N-P* gate sequence or FF1, IA1, IA2, OS1 or PS1 via a resistor of 5.6 kΩ shunted by a capacitor of 470 pF
Maximum number of flip-flops: 50.

A simple circuit for resetting flip-flops by a flip-flop FF1 is given in the figure below.

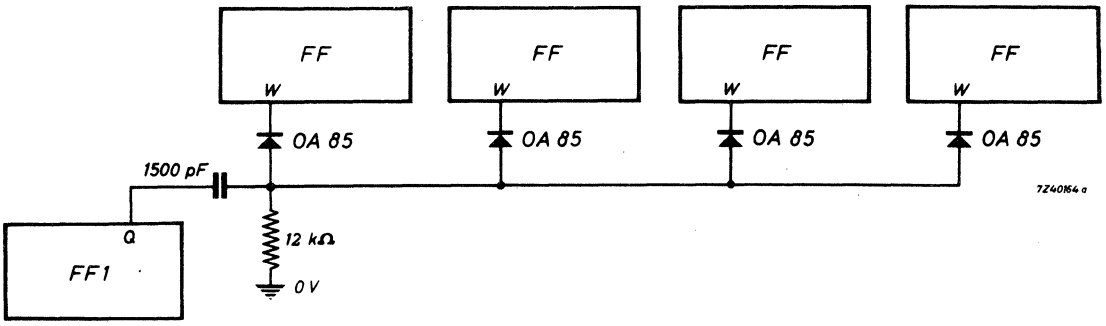


Fig.62.

Resetting takes place on a positive voltage step at the Q terminal of the driving flip-flop. To this terminal an additional capacitive load of maximum 500 pF may be connected.

SCALERS

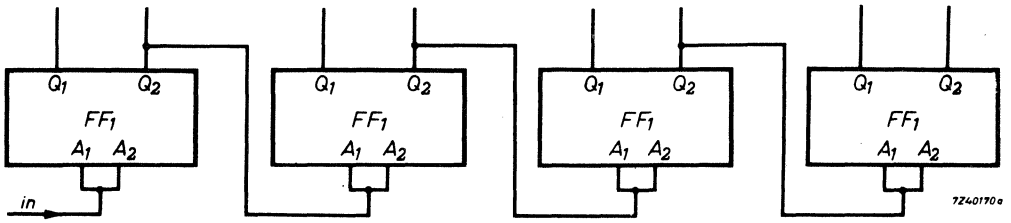


Fig.63. Scaler of 16. (Binary counter with 4 flip-flops.)

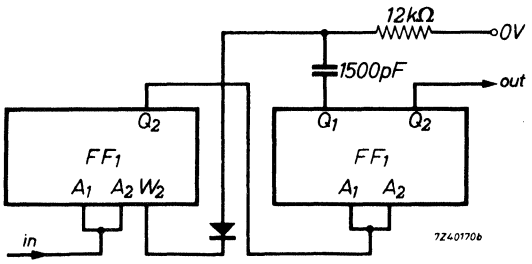


Fig.64. Scaler of 3.

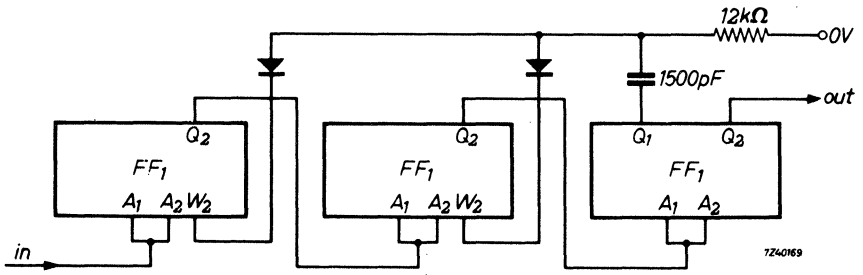


Fig.65. Scaler of 5.

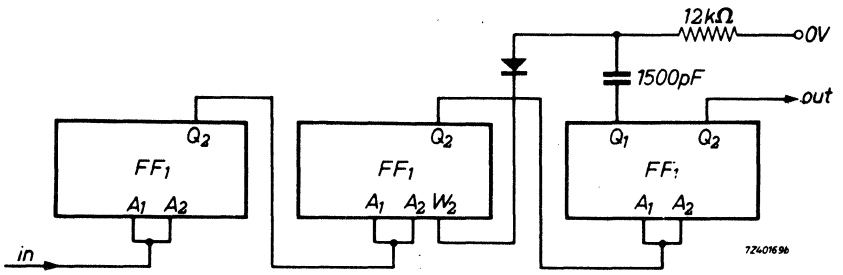


Fig.66. Scaler of 6.

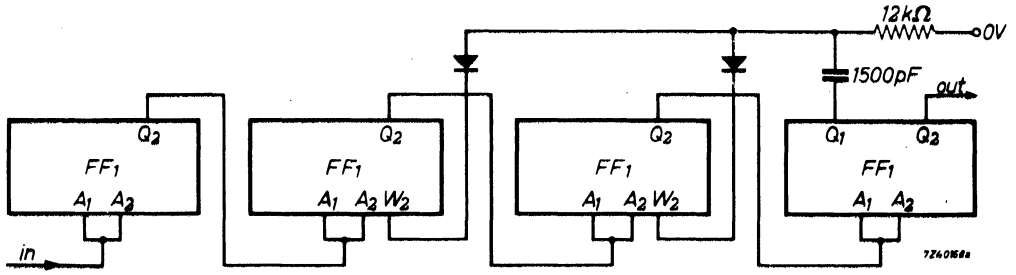


Fig.67. Scaler of 10 (decimal counter).

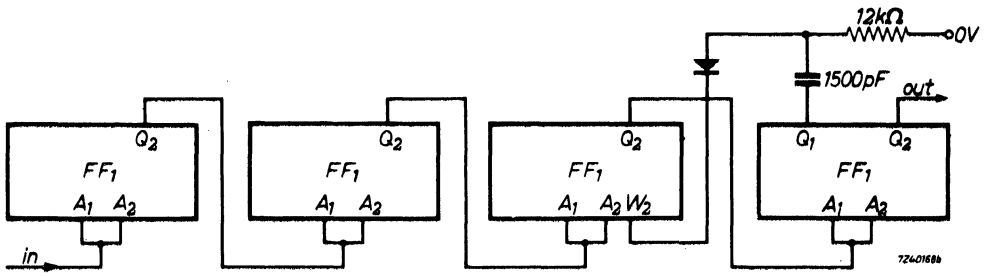


Fig.68. Scaler of 12.

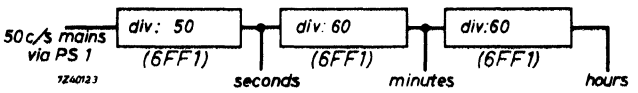


Fig.69. Time code frequency divider.

MULTIPLE-INPUT GATES.

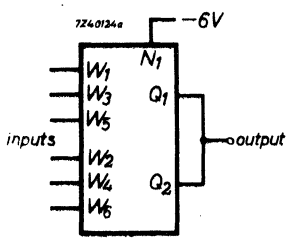


Fig.70. 6-input N-gate, composed of one 2.3N1.

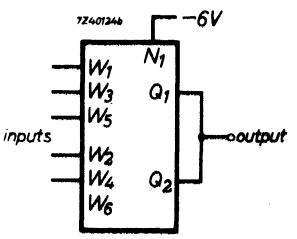


Fig.71. 5-input N-gate, composed of one 2.3N1.

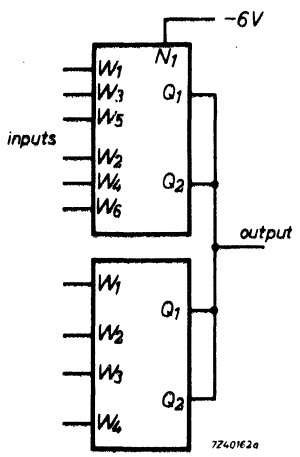


Fig.72. 10-input N-gate, composed of one 2.3N1 and one 2.3N1.

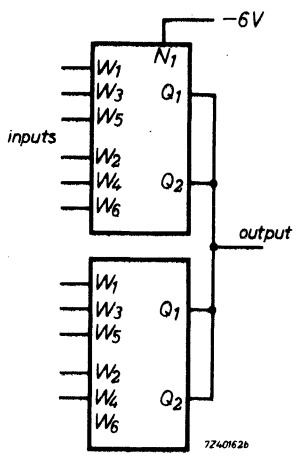


Fig.73. 11-input N-gate, composed of two 2.3N1's.

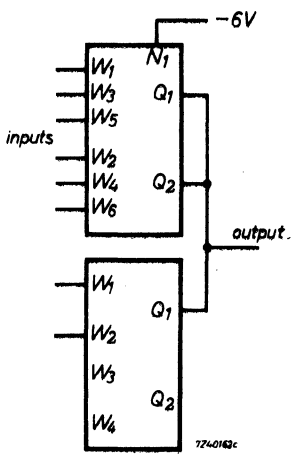


Fig.74. 8-input N-gate, composed of one 2.3N1 and half a 2.2N1.

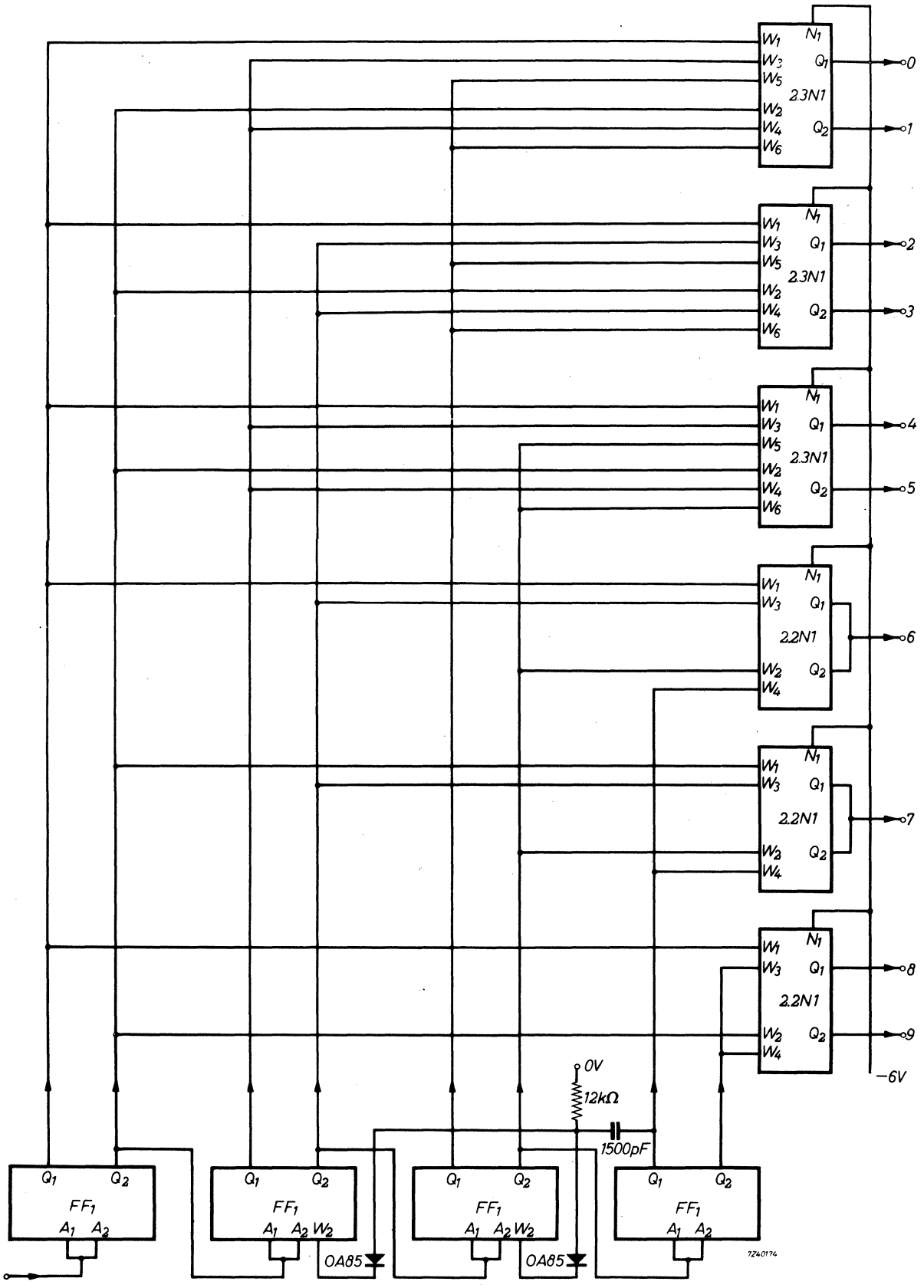


Fig.75. A count of n in the decimal counter produces a "1" signal at the output n at the right. All N, E and P terminals of the flip-flops should be connected to the corresponding supply lines.

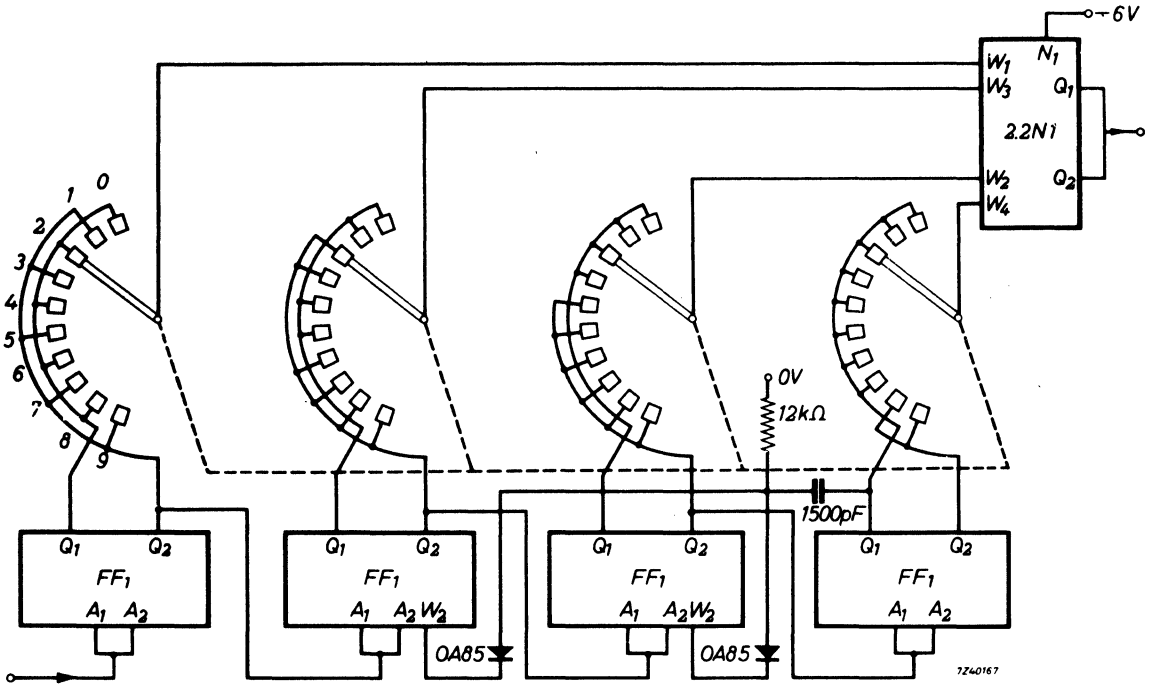


Fig.76. General purpose circuit. An output voltage is produced when the decimal counter stores the number chosen by means of the 10-position 4-wafer switch. The circuit may also be used for the determination of a time interval by counting cycles of an alternating voltage, e.g. the mains.

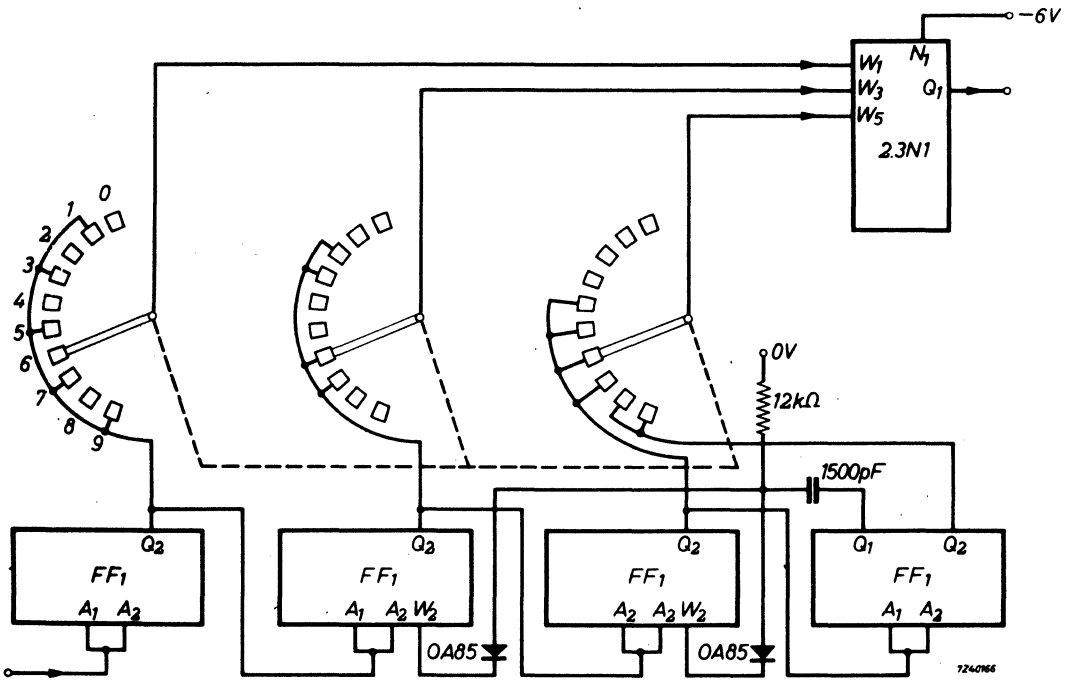


Fig. 77. Simplified circuit for special applications. An output signal is produced when the decimal counter has reached the number chosen by means of the 10-position 3-wafer switch. When this number is exceeded the output signal may stay or recur. This phenomenon makes the circuit only useful for those applications in which these spurious signals do not interfere.

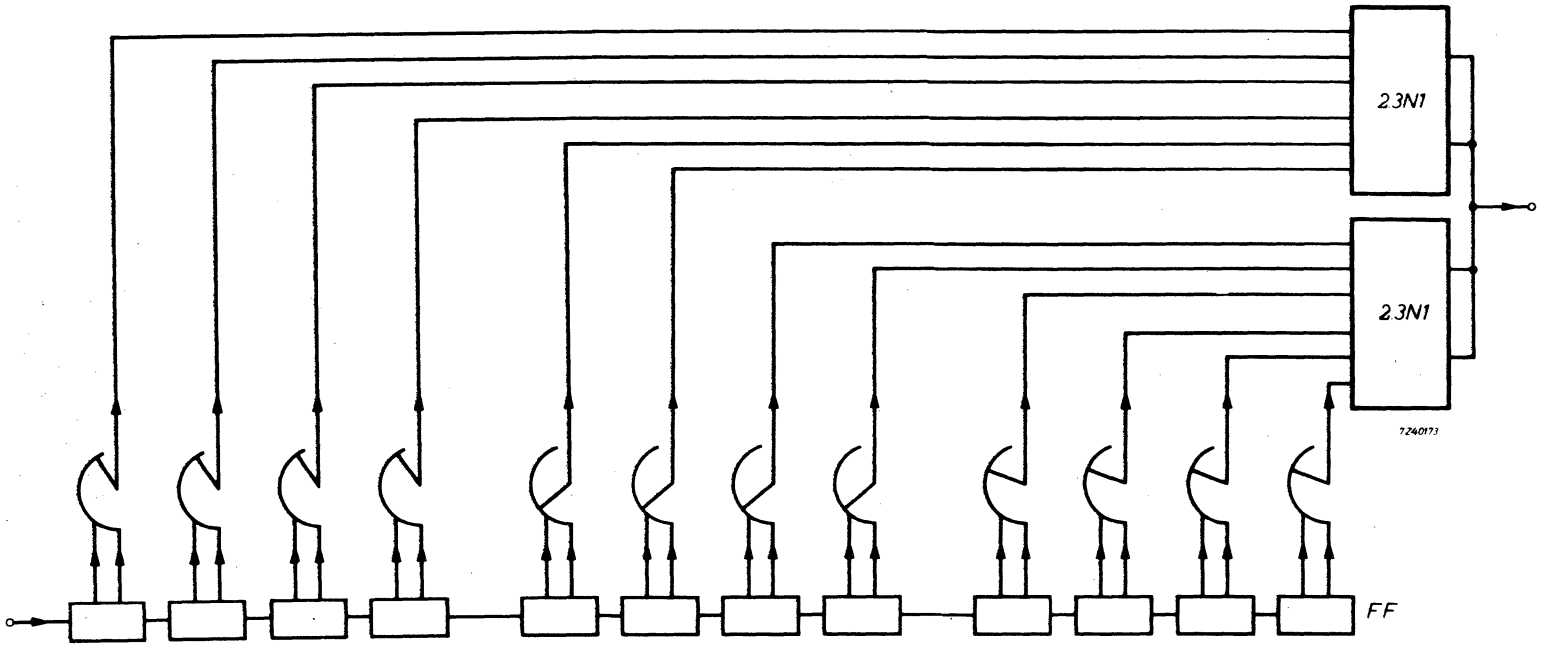


Fig.78. When the counter consists of several decades, it may be preselected by as many 10-position switches. The gates are combined to one gate. The circuit may also be of the 3-wafer switch type, as shown in Fig.77.

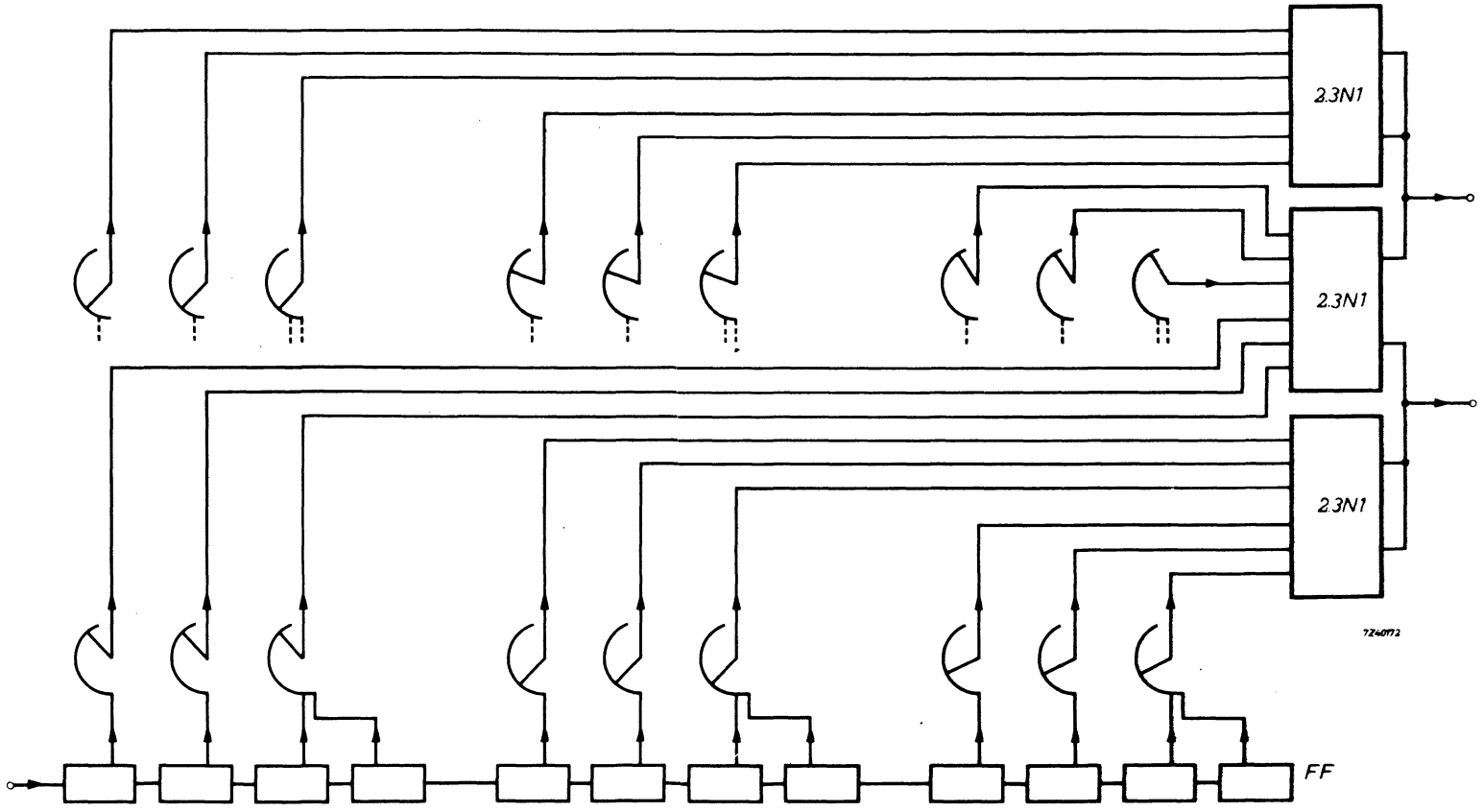


Fig.79. Preset counter with multiple programmes. More than one set of switches and gates may be connected to the same counter. Every output gives a signal when the counter has reached the number set by its associated switches. The switches may be of the 3 or 4-wafer type.

Mounting the Circuit Blocks

Since the mounting position of circuit blocks is arbitrary, mounting can be done in various ways. The commonest method is to solder the terminals onto a printed-wiring board with the circuit blocks lying flat on the non-printed side of the board, as shown in Fig.80.

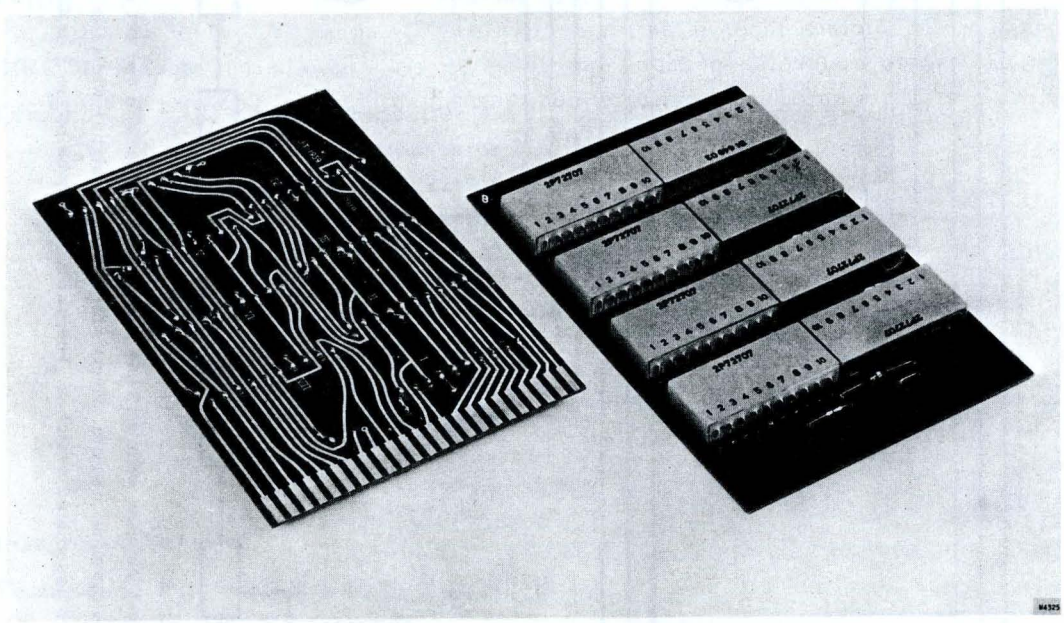


Fig.80. Circuit blocks mounted on a printed-wiring board.

Soldering can be done either by means of a soldering iron or, specially when large numbers of printed-wiring boards are concerned, by dip-soldering.

The way of mounting as in Fig.80 has the advantage, that a circuit block can easily be removed by cutting the terminal wires. If a new unit must be mounted in its place, the terminals can be soldered to the wire-ends remaining on the board. The wire ends can also be removed by unsoldering, but great care should then be taken to avoid overheating of the board.

LARGER BUILDING BRICKS

By proper arrangement of circuit blocks on a printed-wiring board, functional elements of a higher order than those inherent in a circuit block can be constructed. A decimal counter or a complete register can be built up in this way. When such an assembly is made pluggable, the thus formed "building brick" can be made easily interchangeable.

The question arises, what number of circuit blocks should be mounted on one printed-wiring board, or in other words; how comprehensive such a building brick should be. No general answer can be given to this question, since it largely depends on system requirements of a non-electronic nature.

For large equipment the main object will mostly be to have a limited number of types of building bricks for reasons of service. Large computers are generally built up from only a few types of building bricks, a maximum circuit complexity of, say, two flip-flops and one gate being used. In such a case more than 80 % of the equipment can be made up of e.g. 8 - 10 different types of building brick.

For prototypes or laboratory equipment it may be advantageous to mount the circuit blocks on the experimenter's printed-wiring board (Fig.81) or on the universal printed-wiring board (Fig.83). For smaller series-manufactured equipment it may be convenient to combine a comparatively large number of circuit blocks on one large printed-wiring board, so that only a small number of these boards is required. This may lead to low-cost manufacture and to simple maintenance.

In each individual case an optimum should be chosen between the two extremes:

1. a number of circuit blocks mounted on a printed-wiring board with only input, output and supply lines externally accessible and all logic interconnections printed on the board,
2. a versatile unit, consisting of a number of basic functions arranged merely as a matter of convenience, all logic connections being made outside the printed-wiring board.

In very simple applications it may even be undesirable to use printed-wiring boards at all, because wire-wrapping or direct soldering onto the terminals is preferred.

MOUNTING COMPONENTS

EXPERIMENTER'S PRINTED-WIRING BOARD

Fig.81 shows the front and rear side of the experimenter's printed-wiring board measuring 196 mm x 396 mm x 1.5 mm. It has plated contacts that match the FO42 printed-wiring connectors of the standard maximum length with 35 contacts. Two types of this printed-wiring board are available, type number, P8 900 79 with one-sided contacts and type number P8 900 89 with double-sided contacts. Depending on the requirements, the board can be sawn to any size.

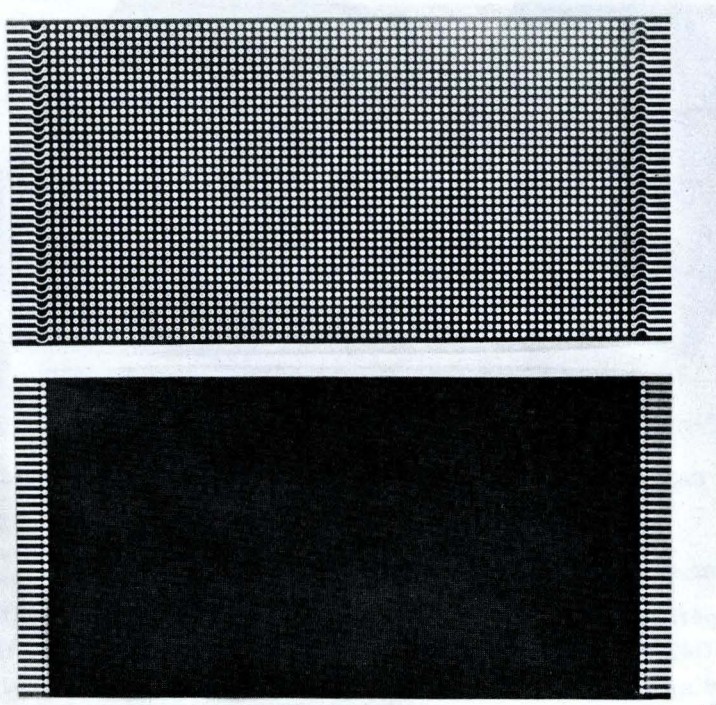


Fig.81. Front and rear view of the experimenter's printed-wiring board.

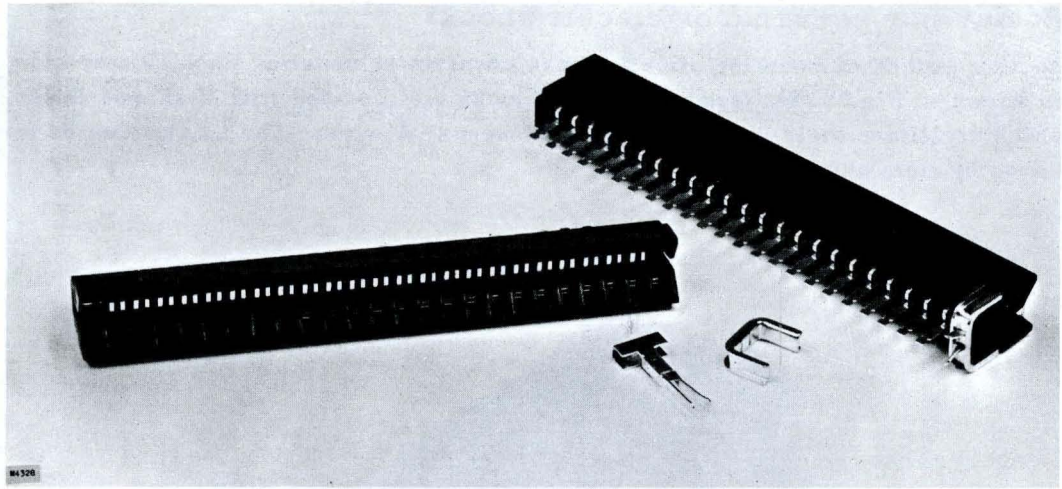


Fig.84. Contact blocks FO42.

A photograph of a contact block is shown in Fig.84.

The thickness of the printed-wiring boards with the mounted circuit blocks allows the contact blocks to be placed closely together, so that a compact arrangement can be obtained. Fig.85 shows a detail of such an assembly. In this application both ends of the contact blocks are locked in a frame, of which the dimensions are indicated in Fig.86.

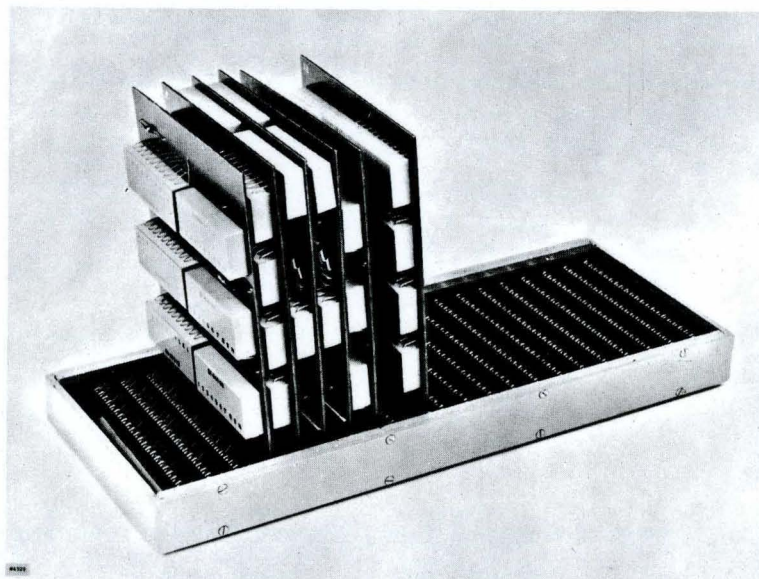


Fig.85. Assembly of contact blocks in a frame with some printed-wiring boards inserted.

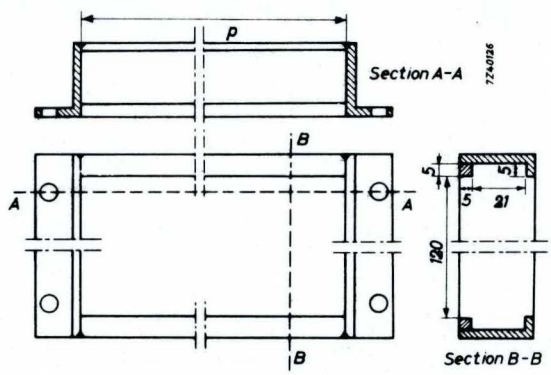


Fig.86. Dimensional drawing of the frame in Fig.85. The dimension p depends on the number of contact blocks.

SIDE-BY-SIDE MOUNTING OF CIRCUIT BLOCKS

Another method of mounting circuit blocks consists in mounting them side-by-side, as shown in Fig.87. The terminals of the blocks are provided with V-shaped bends, which facilitate their interconnection by means of wires. The blocks can be removed by mere unsoldering.

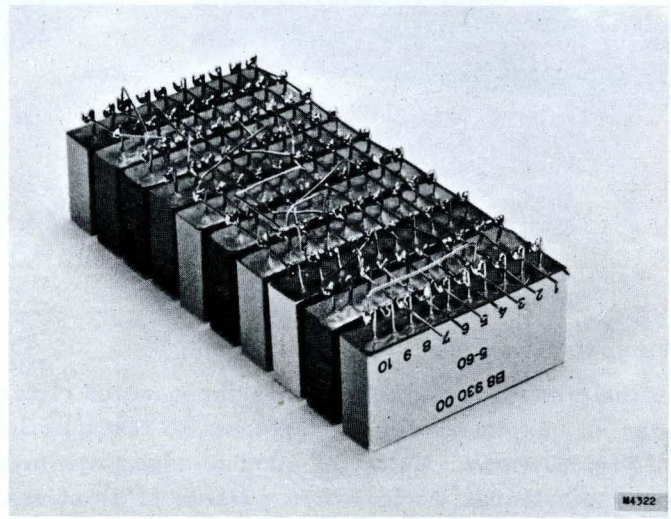


Fig.87. Circuit blocks mounted side-by-side.

Some Applications of Circuit Blocks

DIGITAL COMPUTER

GENERAL DATA

This laboratory model of a small transistorized computer, shown in Fig. 88, is designed for bookkeeping and invoicing purposes. An electric typewriter is used as input and output unit; it enables numbers to be introduced by hand and types out the results of the arithmetical operations carried out by the computer. Programming is performed by a plugging panel, which has been made interchangeable.

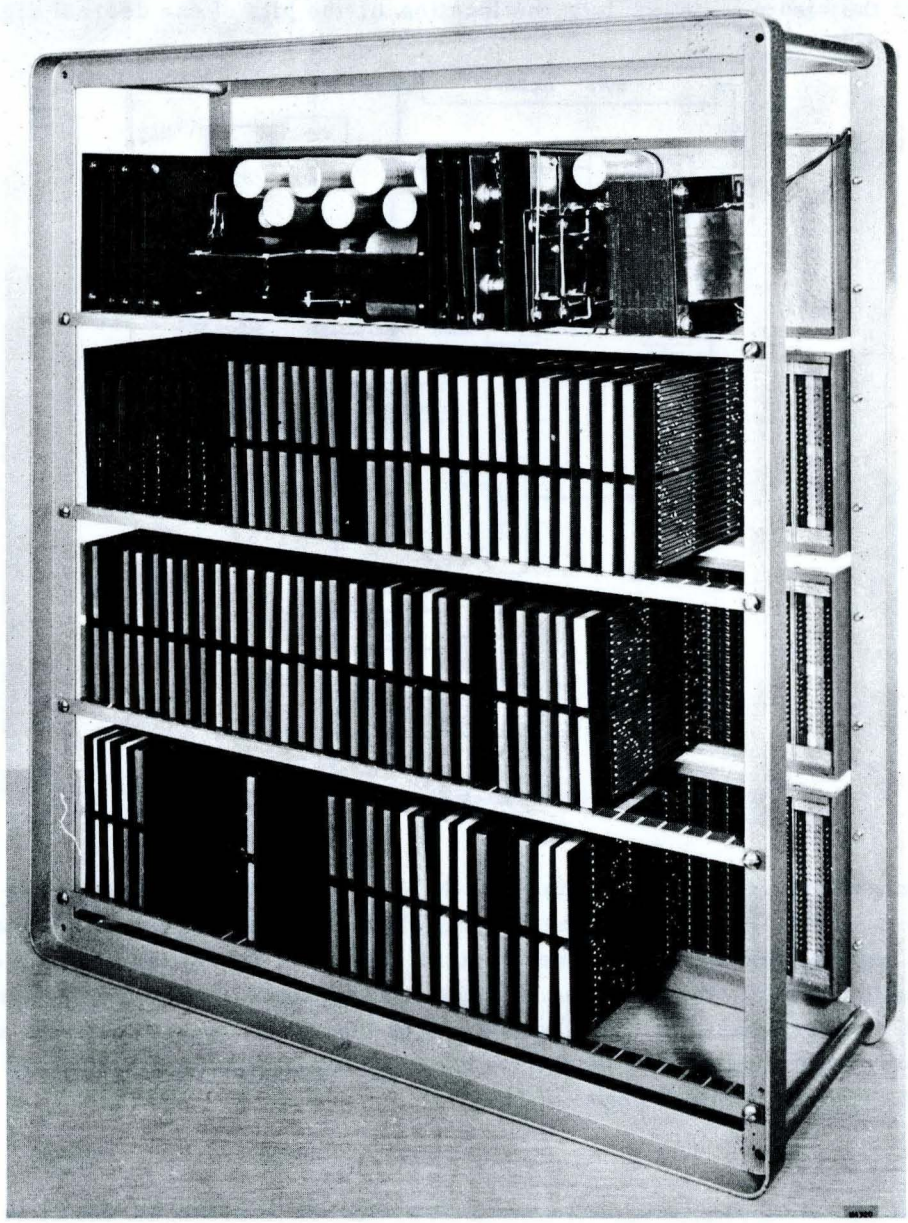


Fig. 88. Laboratory model of a digital computer equipped with circuit blocks.

The computer operates in the decimal numerical system with the excess-3 code in the internal organisation. The (fixed) decimal point can be placed in any arbitrary position beforehand.

The arithmetic unit comprises a shift register and an adder in which the digits of a number are introduced one by one (serial operation). The computer can handle 16 numbers of 16 digits each, the sign digit included.

Various types of circuit block are used in the computer. They are mounted on printed-wiring boards, which are plugged into corresponding contact blocks. The additional circuit elements, with the exception of the power supply unit, are also mounted on these printed-wiring boards. The whole assembly is mounted in a cabinet which measures 810 mm x 585 mm x 232 mm. As can be seen from Fig.88 the cabinet has five compartments; the lower four house the printed-wiring boards, whilst the power supply unit is mounted in the top compartment.

BLOCK DIAGRAM

The simplified diagram, which is shown in Fig.89, comprises the functional elements of the computer. The decimal shift register consists of 4 binary registers in parallel, each built up of 16 flip-flops FF2[1]). Each four corresponding flip-flops of the binary registers form the location of the bits of one decimal digit. On

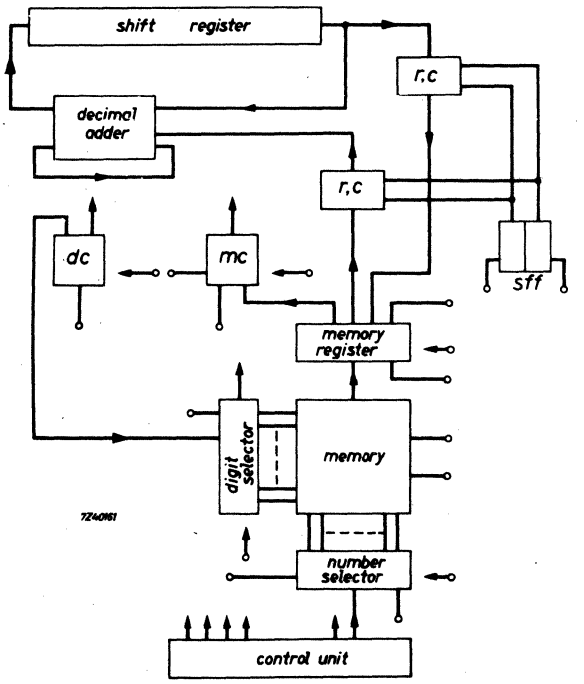


Fig.89. Simplified block diagram of the computer.

the command of a shifting pulse the bits in all four registers are shifted one position to the right. The levels of the four flip-flops in the utmost right-hand position of the register are applied to one input of the adder, whilst the contents of the adder output are introduced in the extreme left register location. By applying the bits of another number to the second input of the adder, two numbers are added. Obviously multiplication can be accomplished by repeating this procedure as many times as required for each power of 10.

[1]) Special type of flip-flop, designed for use in shift registers. This unit will shortly be made available.

The (decimal) adder, which determines the sum digit and the carry digit as the result of the addition of two digits, is composed of a number of binary adders and an inverter (see Fig.90). The binary adders are in their turn made up of AND gates, OR gates and inverters as shown in Fig.91. Circuit blocks are used for this purpose.

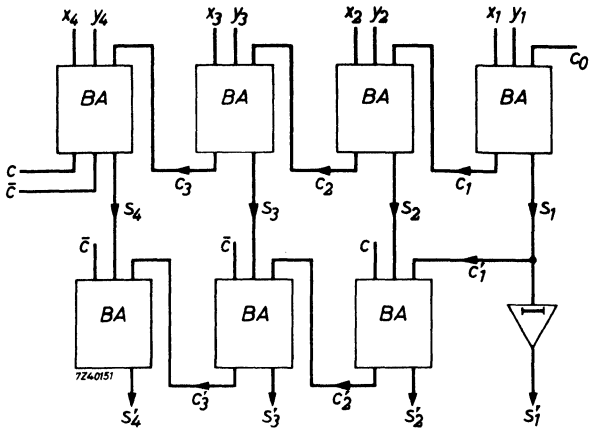


Fig.90. Block diagram of the decimal adder.

The memory comprises magnetic cores as memory elements. Four matrix planes of 16 x 16 cores are needed for the storage of the 16 numbers of 16 digits each. The memory register, in which the contents of a selected memory location appear after reading out, is composed of four flip-flops FF1. Both the number selector and the digit selector consist of four flip-flops FF1 so connected as to form a binary counter.

The same applies to the digit-counter (*dc*) and the multiplier counter (*mc*), which perform a memory function during the arithmetical operations.

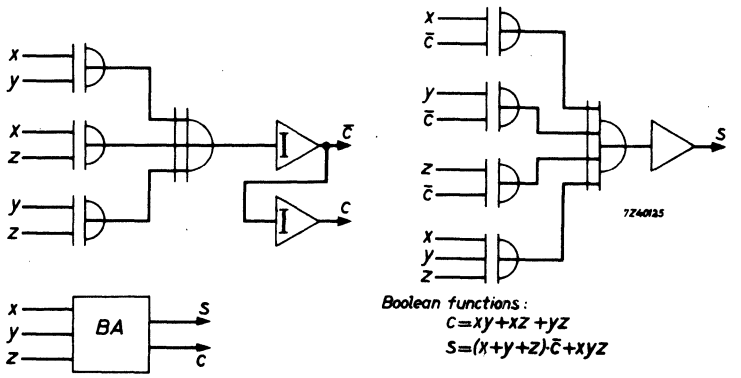


Fig.91. Block diagram of the binary adder.

The units, denoted by *r*, *c* in Fig.89, allow the passage of the bits of a decimal digit themselves or their complements. The units are built up of eight AND-gates with two inputs each (four circuit blocks 2.2 *N*1) and are controlled by the sign flip-flop *sff*.

All types of circuit block (except type FF2, which was exclusively designed for shift-registers) are used in the control unit, which establishes the various connections required for carrying out the programme under consideration.

NUMBER AND TYPES OF CIRCUIT BLOCKS

The computer contains 650 circuit blocks, specified as follows:

Type of circuit block	Number of C.b.'s
2.2N1	99
2.3N1	213
2.2P1	39
2 EF1	123
2 IA 1	17
EF1/IA1	22
FF2	65
FF1	57
OS1	15
Total	650

DIGITAL VOLTMETER

With the aid of the digital voltmeter, of which Fig.92 is a photograph, direct voltages down to 10 μV can be measured and displayed in digital form by three decade indicator tubes Z 510 M. The input impedance of this precision instrument is 1 MΩ/V, whilst the accuracy is 0.5 % ± 1 in the less significant position. The meter has three ranges, viz. 9.99 mV, 99.9 mV and 999 mV.

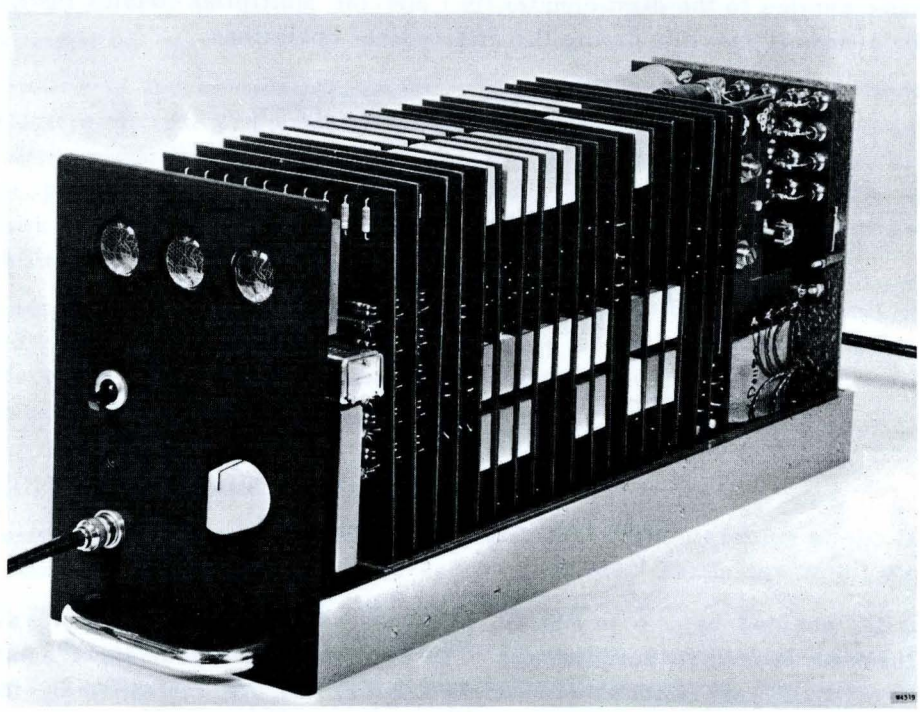


Fig.92. Photograph of the digital voltmeter.

Fig.93 shows the block diagram of the meter. Via the measuring range switch the voltage to be measured is applied to a stage in which it is compared to a variable reference voltage. The latter voltage is increased step by step (each step having

the value of a binary digit) up till the moment the difference voltage from the comparator stage is zero. To achieve this, the output voltage of the comparator is applied to a discriminator (via a d.c. - a.c. converter and an a.c. amplifier), which controls the value of the reference voltage. This is arranged in a digital-to-analogue converter consisting of a ladder network which is composed of precision resistors.

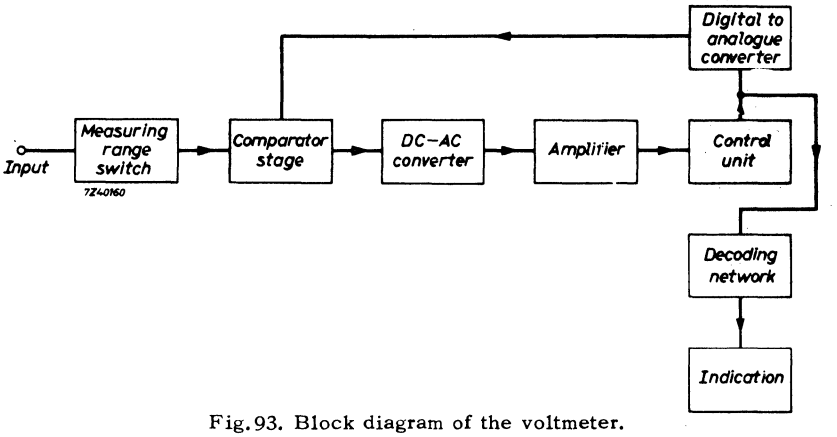


Fig. 93. Block diagram of the voltmeter.

When the reference voltage has increased so far that it equals the input voltage, it is applied to a de-coding network, which controls the decimal indicator tubes.

From the photograph of Fig. 92 it can be seen, that the (49) circuit blocks and other components are mounted on (vertical) printed-wiring boards. On the front panel the three indicator tubes, the mains switch, the measuring range switch and the input receptacle can be distinguished. The supply unit is mounted at the rear.

The power consumption of the apparatus is 60 W, the dimensions of the cabinet are 197 mm x 139 mm x 450 mm and its weight is 8.8 kg.

AUTOMATIC CONTROL OF A HYDRAULIC PRESS

During the manufacture of mass products use is made of a hydraulic press, in which the material is pressed into the required shape and consistence. The press, schematically shown in Fig. 94, consists mainly of a mould and two dies, either

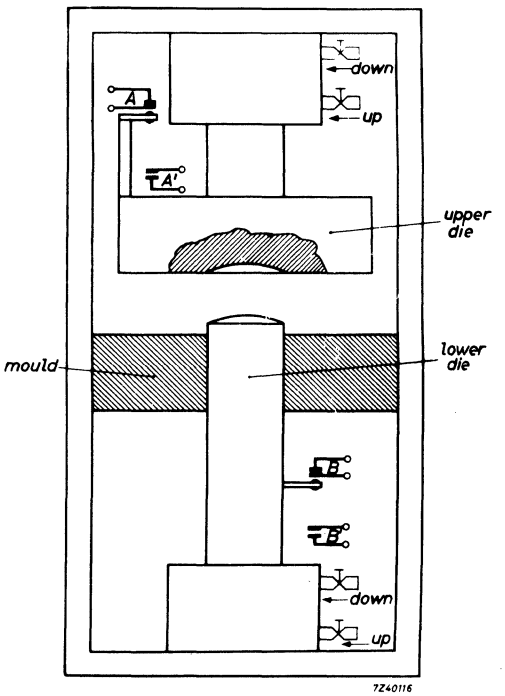


Fig. 94. Schematic drawing of the hydraulic press.

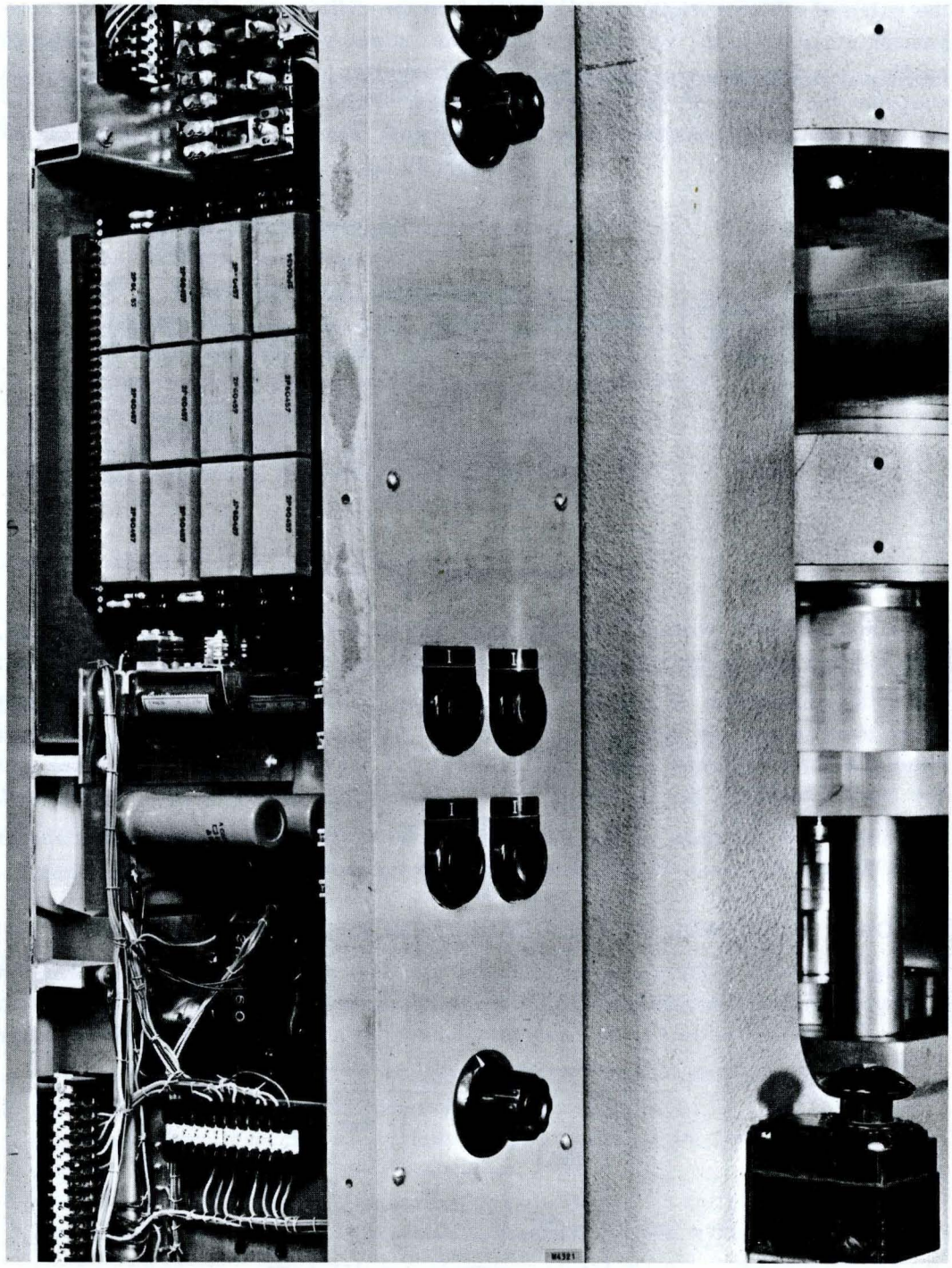


Fig.95. Part of the press with the electronic circuit.

of which is connected to a plunger of the hydraulic system. In the figure both dies are drawn in their upper positions. The upper die rests on the mould when in its lower position.

PROGRAMME

During the pressing process several valves and switches must be operated according to a specified programme. In principle they could be operated purely mechanically, but since the press is used for various kinds of products, electronic control is to be preferred with a view to greater versatility.

In the time diagram of Fig.96 the various phases of a complete cycle of the pressing process are indicated. The diagram shows the intervals during which the valves and switches are activated. In the lower part of the figure the corresponding positions of the dies are shown.

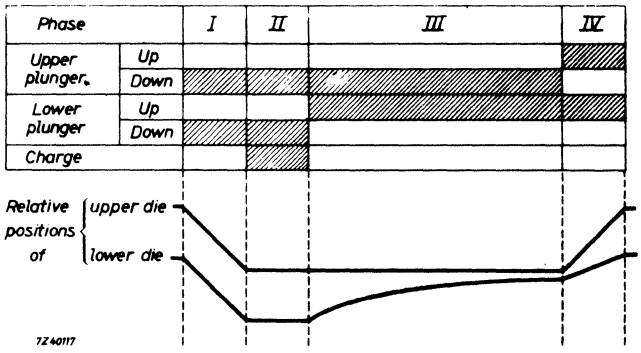


Fig.96. Time diagram of the press.

The phases are initiated by a control unit, made up of a logic circuit. The latter is, in turn, controlled by the switches A, A' and B, B' that are operated by the dies in their upper and lower positions, and by a timing circuit.

The duration of the phases I and IV is determined by the oil pressure on the plungers, that of the phases II and III by the timing circuit. The complete cycle is started by manually operated switches.

ELECTRONIC CONTROL

Both the logic circuit and the timing circuit consist of circuit blocks, namely gates and flip-flops respectively. The latter are so arranged as to form a frequency divider driven by clock pulses derived from the 50 c/s mains. To achieve a variable time diagram, the timing circuit can be pre-adjusted by means of a plugging panel. Power transistors type OC 29 energise the magnetic valves that command the oil pressure on the plungers.

Fig.95 is a photograph of the press with the electronic control circuit mounted onto it.

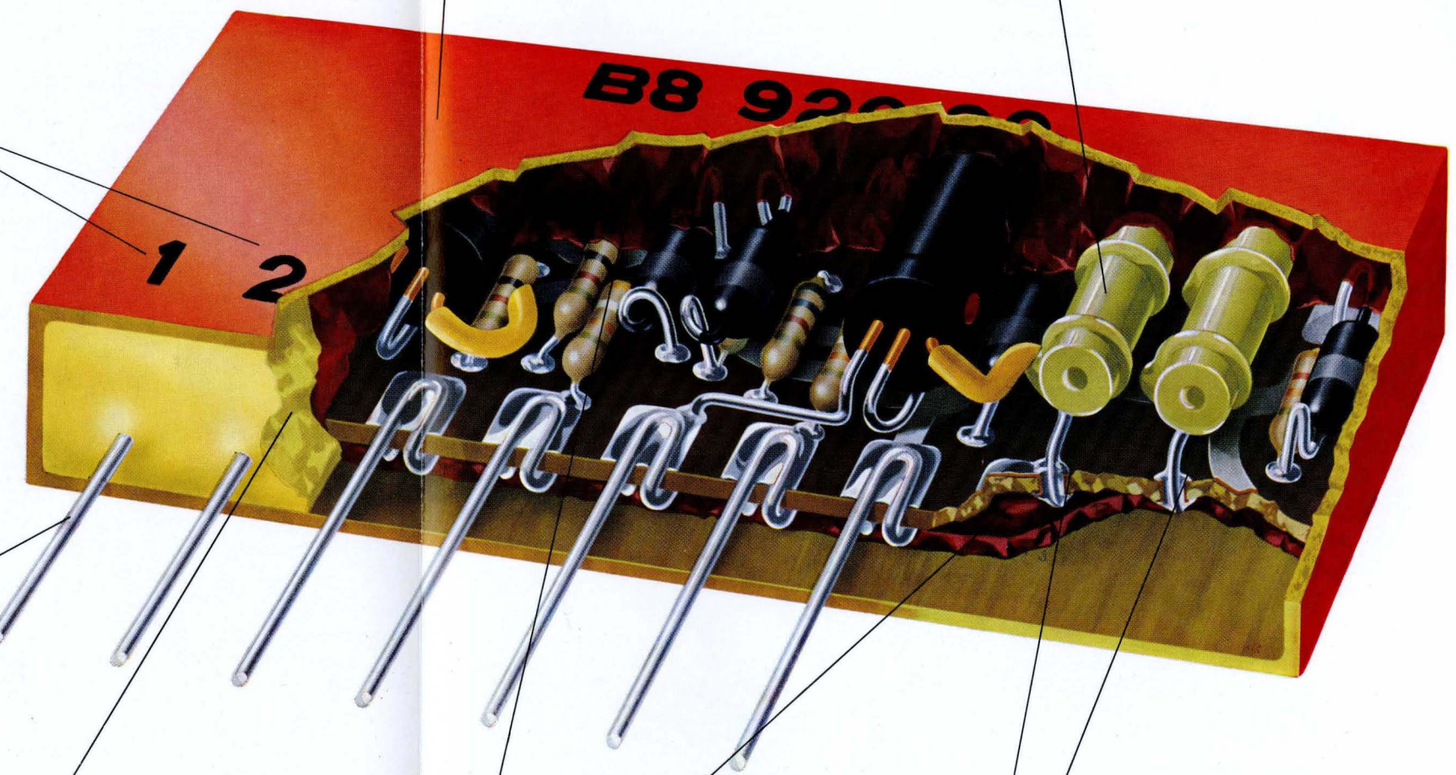
Owing to the electronic control, the programme can easily be extended (e.g. the application of multiple dies).

cut-away view of a circuit block

Synthetic-resin case provides complete protection against humidity and mechanical damage in transit or handling

High-quality components, compactly mounted, effect considerable saving of space in equipment

Numbering of leads and colour coding simplifies assembly and service



Connecting leads can be soldered to printed-wiring boards or other wiring system

Sealing compound excludes moisture *)

Potting compound gives full protection against shock and vibration, thus increasing the reliability of soldered joints and of components

Printed-wiring board with plated-through holes ensures reliable joints due to large area of soldered contacts

*) The units will withstand the corrosion, temperature cycle and accelerated humidity test specified in MIL-STD-202, and the BCMT prolonged humidity test.

In Fig.82 an example is given of the use of the experimenter's printed-wiring board with circuit blocks. The connections at the rear side are made by insulated wires.

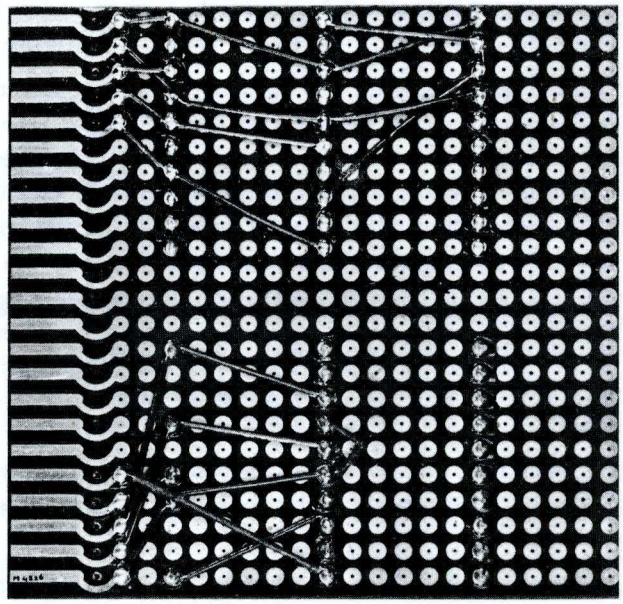


Fig.82. Rear side of an experimenter's printed wiring board with circuit blocks mounted on it.

UNIVERSAL PRINTED-WIRING BOARD

For a more advanced design a "universal printed-wiring board", type number P8 900 91.2, is available. This board is provided with a standard pattern, which allows the mounting of 6 circuit blocks, whilst the required connections can be made by wire "jumpers" (see Fig.83).

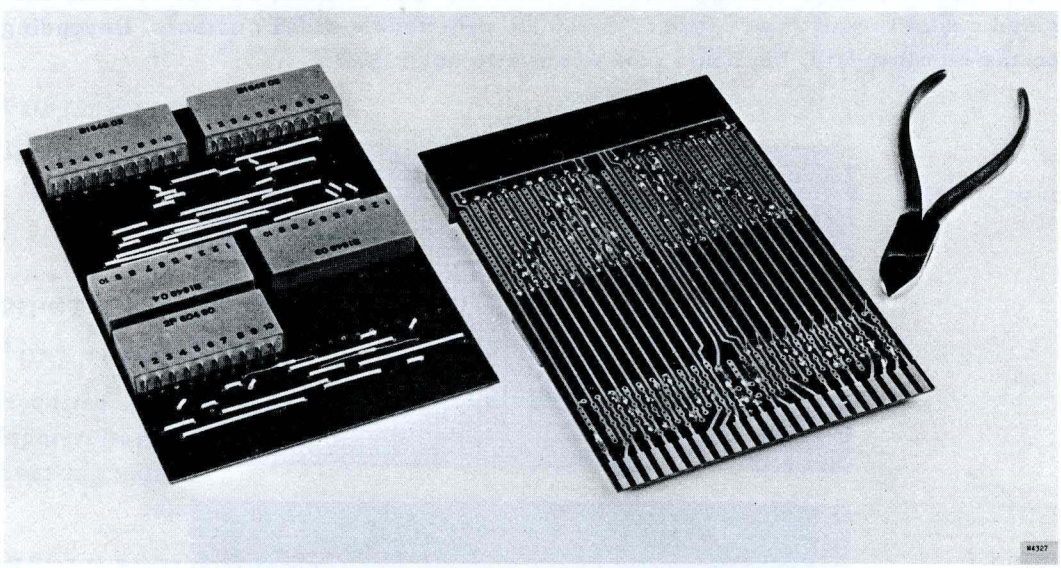


Fig.83. Circuit blocks mounted on the universal printed-wiring board.

CONTACT BLOCK FO42 FOR PLUG-IN PRINTED CIRCUITS

Both the experimenter's printed-wiring board and the universal printed-wiring board match the FO42 contact block, which is provided with one or two rows of gold- or silver-plated spring contacts, to receive printed wiring boards with single-ended and double-sided contacts respectively. The contact blocks can be made in any desired length, with up to 70 contact springs.

LOADING TABLE, supply voltage + and - 6V ± 10 %

Chain of driving units									max. number of driven units															
first			second			third			FF1		FF2		OS1	IA1	IA2		EF1	EF2	PS1	AND	OR	Type
in	type	out	in	type	out	in	type	out	S,R or Parallel	$S_d R_d$	P	$S_d R_d$	S	W	W	W'	W	W	W	W	W	In
						S,R	FF1	Q	4	1 [1]	4	1 [1]	4	1			1	3	4 [6]	4 [7]	# 12)	
								$\bar{Q}$	4	1 [1]	4	1 [1]	4	1			1	3	4 [6]	4 [7]		
						W	FF2	Q	4	1 [1]	4	1 [1]	4	1			1	3	4 [6]	4 [7]	# 12)	
								$\bar{Q}$	4	1 [1]	4	1 [1]	4	1			1	3	4 [6]	4 [7]		
						S	OS1	Q	4	1 [1]	4	1 [1]	4	1			1	3	4 [6]	4 [7]	# 12)	
								$\bar{Q}$		2 [1]		2 [1]		2			2	6	8 [6]	4 [7]		
						W	IA1	Q	4 [2]	2 [1]	4 [2]	2 [1]	4 [2]	2			2	6	8 [6]	8 [7]	# 12)	
			W	AND	Q	W	IA2	Q		2 [1]		2 [1]		2			2	6	8 [6]	4 [7]		
W	AND	Q	W	OR	Q																	
								Q	4 [2]	2 [1]	4 [2]	2 [1]	4 [2]	2			2	6	8 [6]	60 [7]	# 12)	
W	AND	Q	W	EF2	Q	W	IA2	Q^9	20 [2]	8 [1]	20 [2]	8 [1]	20 [2]	6			6	20	25 [6]	30 [7]		
								Q^{10}	30 [2]	18 [1]	30 [2]	18 [1]	30 [2]	12			12	40	50 [6]			
			W	EF2	Q	W	IA2	Q	TS APPLICATION SHEETS PAGES 46, 47, 59 and 60													
						W	EF1	Q	4 [2][3]	8 [1]	4 [2][3]	8 [1]	4 [2][3]	6					25 [6]	4 [7]		
																					# 12)	
				IA1,2	Q	W	EF1	Q	4 [2][3]	18 [1]	4 [2][3]	18 [1]	4 [2][3]	12					50 [6]	4 [7]		
				OS1	$\bar{Q}$	W	EF1	Q		18 [1]		18 [1]		12					50 [6]	4 [7]		
			W	AND	Q^9	W	EF2	Q		0 [4]		1 [4]				1 [13]						
W	AND	Q	W	OR	Q	W	EF2	Q^9		1		1									# 12)	
						W	PS1	Q	2	1 [1]	2	1 [1]	2	1			1	1	4 [6]	2 [7]	# 12)	
						W	AND	Q	4 [5]		4 [5]		4 [5]			1		1	1			1
						W	OR	Q		1 [8]		1 [8]		# 11)		# 11)	# 11)	# 11)				

NOT ALLOWED

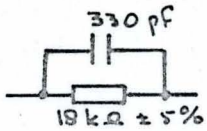
NOT RECOMMENDED

Notes to the loading table

1) Each via the following circuit: 

2) Only if the chain of driving units is driven by a FF1-2, PS1 or OS1 (Q output).
3) With OA 47 diode connected between W and Q of the EF1, cathode to Q.
4) In this connection the flip-flop is controlled directly by the emitter follower. The state of the flip-flop depends on the EF2 input level.
5) Only if the AND gate is driven by a FF1-2, PS1, OS1 (Q output) or a suitably driven IA1-2 (see under 2)). The max. speed is

$$\frac{30 \text{ kc/s}}{\text{number of driven units}} .$$

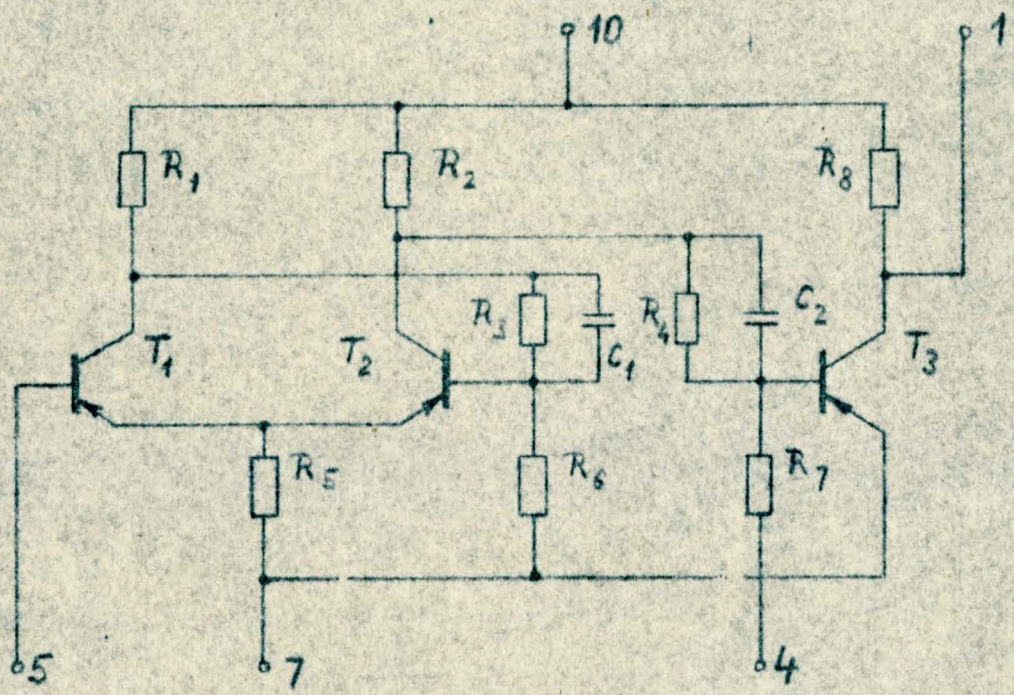
6) Each via the following circuit: 

7) Inputs of a single gate driven by the same unit count as one input.
8) Via a 7.5 kΩ ± 5 % resistor.
9) With a 470 Ω ± 5 % resistor between Q and the negative supply.
10) With a 180 Ω ± 5 % resistor between Q and the negative supply.
11) The number of units that an OR gate can drive is equal to the number that the unit driving the OR gate can drive directly under the circumstances given in the LOADING TABLE.
12) One OR gate can be applied between the "last driving" unit output and the DC input of a FF1, FF2, EF1, EF2, IA1 or IA2 (W' input) in all combinations given in this LOADING TABLE.
13) Conn. A of the EF2 must be connected to Q of the IA2.

Confidential

ICOMA

1) Electrical Circuit



R_1 , R_2	1,8	kohm	± 10%	8	mW
R_3	8,2	"	± 10%	2	"
R_4	10	"	± 10%	3,5	"
R_5	1	"	± 10%	4	"
R_6	6,8	"	± 10%	0,6	"
R_7	22	"	± 10%	1,5	"
R_8	2,2	"	± 10%	6	"
C_1	220	pF	+ 20%	30	^V
C_2	330	pF	- 30%	30	^V
T_1, T_2, T_3	OC-47		Normale spec.		

For reliable working the values of the components must be between the limits stated above.

Codenumber: 27 727 05

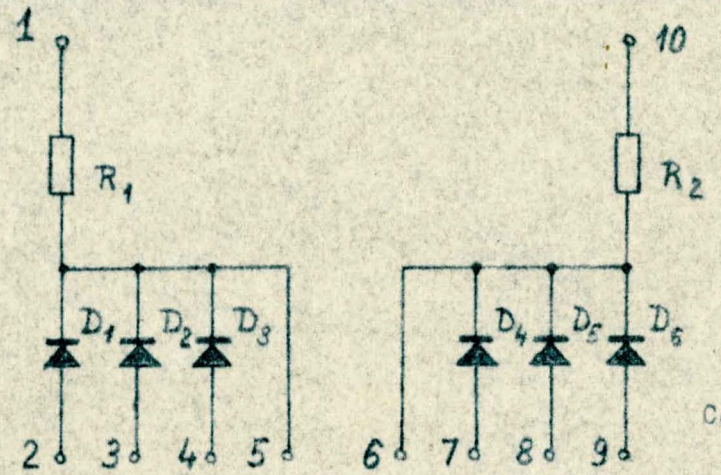
	PULSE SHAPER Class B	SCHEMA (Provisional)
		PRR 23-3-221
GET.-DRAWN DESS.-GEZ Dipl.Ing. Barany DAT 24.1.59		BLZ SH.P. 1 SL SH.P. 1 / VERV.-SUPERS REMPL.-ERS. 27.11.58

N.V. PHILIPS' GLOFILAMPENFABRIEKEN EINDHOVEN -- NEDERLAND FORM. A4

37 120 90.5

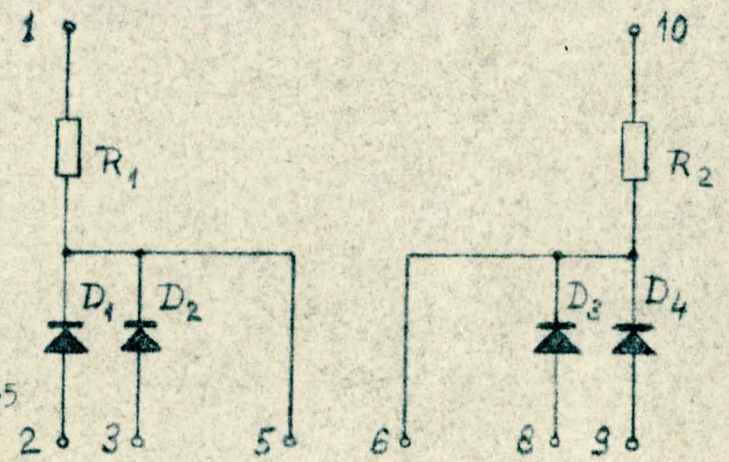
ICOMA

1) Electrical Circuit



. . . a.)

Codenumber 2P 604 32



b.) . . .

Codenumber 2P 604 55

R_1 , R_2	12 kohm	± 15 %	3 mW
D_1 - D_6	OA-95	norm. spec.	

For reliable working the values of the components must be between the limits stated avove.

TWIN AND- GATE
a.) Three Inputs
b.) Two Inputs

SCHEMA (Provisional)

PRR 23-3-222

/

GET.-DRAWN DESS.-GEZ Dipl.Ing. Barany DAT 27.11.58

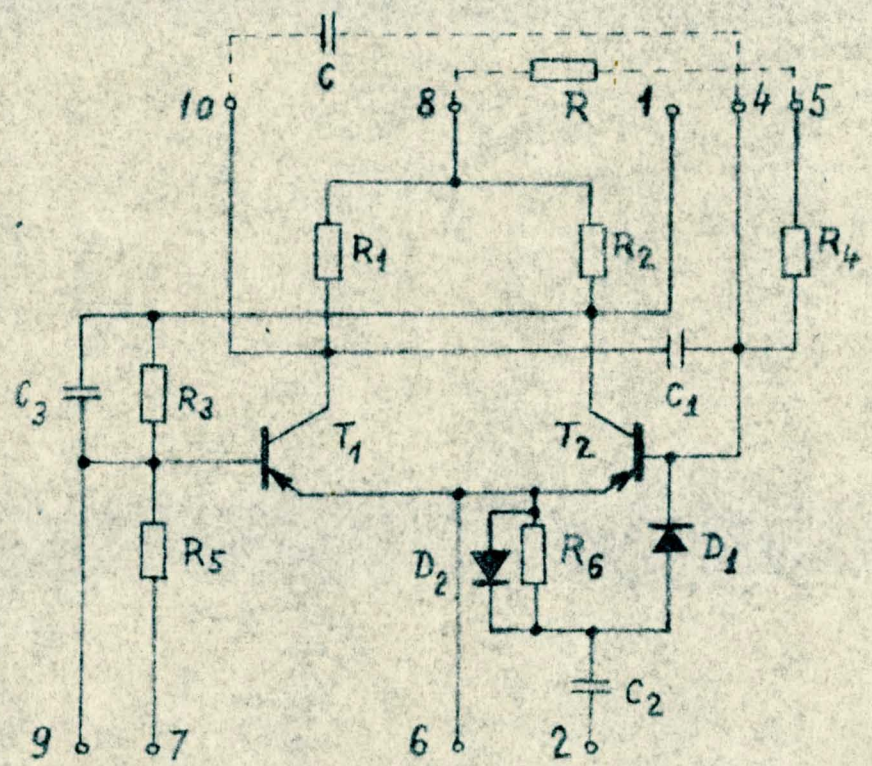
VERV.-SUPERS REMPL.-ERS.

N.V. PHILIPS' GLOEILAMPENFABRIEKEN EINDHOVEN — NEDERLAND

FORM. A4

ICOMA

1) Electrical Circuit:



R_1 , R_2	1	kohm	± 10%	36 mW
R_3	5,6	kohm	± 10%	6 mW
R_4	12	kohm	± 10%	3 mW
R_5	39	kohm	± 10%	1 mW
R_6	1	kohm	± 10%	3 mW
C_1	220	pF	+ 20% − 30%	30 V
C_2	560	pF	+ 10% − 20%	30 V
C_3	470	pF	+ 20% − 30%	30 V
D_1 , D_2	OA-95		norm. spec.	
T_1 , T_2	OC-46		norm. spec.	

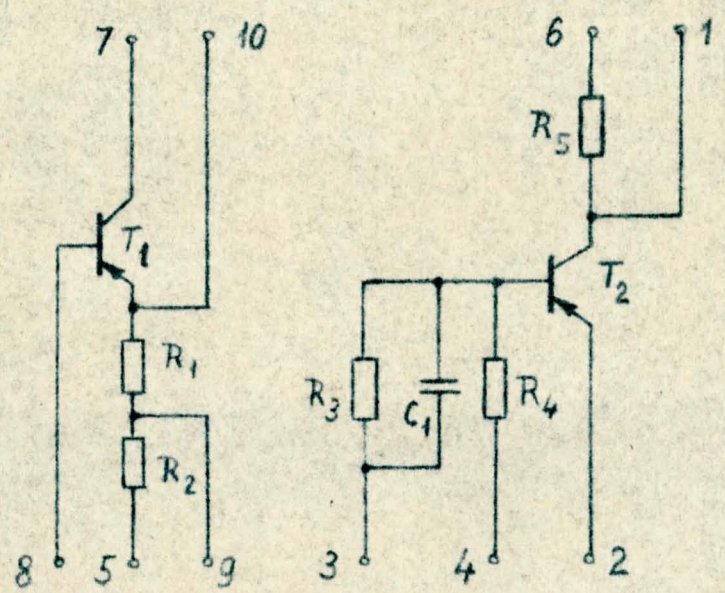
For reliable working the values of the components should be between the limits stated above

Codenumber: 2P 727 03

	ONE-SHOT MULTIVIBRATOR Class B	SCHEMA (Provisional) PRR 23-3-252
GET.-DRAWN DESS.-GEZ. Dipl.Ing. Barany	DAT. 23.3.1959	BL.-SH.P. 1 VERV.-SUPERS. REMPL.-ERS.
N.V. PHILIPS' GLOEILAMPENFABRIEKEN EINDHOVEN — NEDERLAND		FORM. A4

ICOMA

1) Electrical Circuit



R_1	330	ohm	± 15 %	65 mW
R_2	1,5	kohm	± 15 %	100 mW
R_3	6,8	kohm	± 10 %	6 mW
R_4	52	kohm	± 10 %	1 mW
R_5	1	kohm	± 10 %	36 mW
C_1	470	pF	$\pm \frac{20}{30}$ %	30 V
T_1 , T_2	OC-47		Normal spec.	

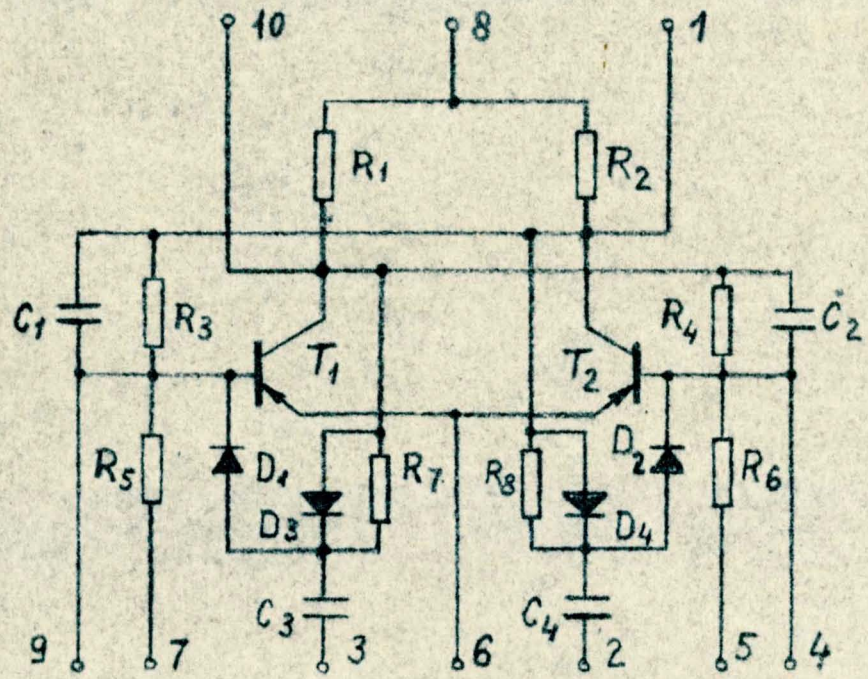
For reliable working the values of the components must be between the limits stated above.

Codenumber: 2P 727 01

	EMITTER FOLLOWER - INVERTER AMPLIFIER Class B	SCHEMA (Provisional)	
		PRR 23-3-228	
		BL. SH.P. ( ) BL. SH.P. 1	/
GET.-DRAWN DESS.-GEZ.	Dipl. Ing. Barany DAT 6.3.59.	VERV.-SUPERS. REMPL.-ERS. 27.11.58.	
	N.V. PHILIPS' GLOEILAMPENFABRIEKEN EINDHOVEN — NEDERLAND		FORM. A4

ICOMA

1) Electrical Circuit



R_1 , R_2	1	kOhm	± 10%	36 mW
R_3 , R_4	5,6	kOhm	± 10%	6 mW
R_5 , R_6	39	kOhm	± 10%	1 mW
R_7 , R_8	12	kOhm	± 10%	3 mW
C_1 , C_2	470	pF	+ 20% − 30%	30 V
C_3 , C_4	560	pF	+ 10% − 20%	30 V
D_1 , D_2 , D_3 , D_4	OA-95		Normal spec.	
T_1 , T_2	OC-46		Normal spec.	

FFA.

For reliable working the values of the components must be between the limits stated above.

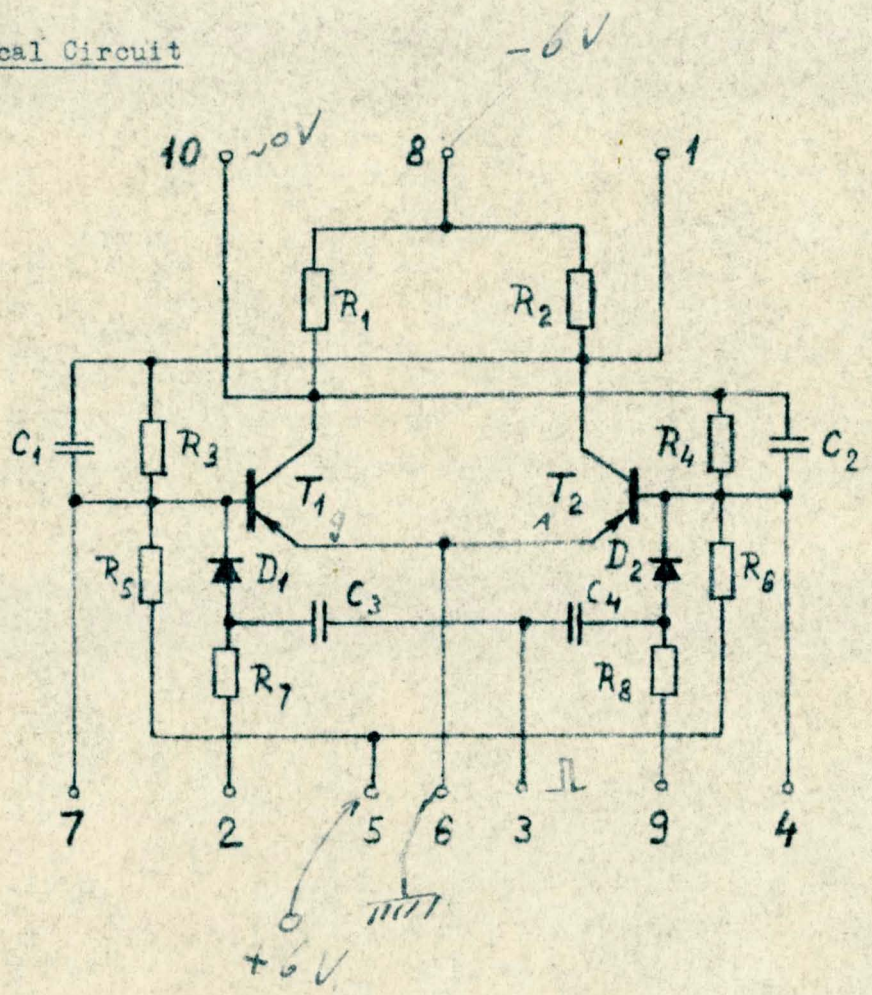
Codenumber 2P 727 06

	Counter FLIP-FLOP Class B	SCHEME (Provisional) PRR 23-3-240	
GET.-DRAWN DESS.-GEZ. Dipl. Ing. Barany	DAT. 20.2.59	VERV.-SUPERS. REMPL.-ERS. PRR 23.3.219	24.1.59
N.V. PHILIPS' GLOEILAMPENFABRIEKEN EINDHOVEN — NEDERLAND			FORM. A4

37 120 90.5

ICOMA

1) Electrical Circuit



0 V

-5 V

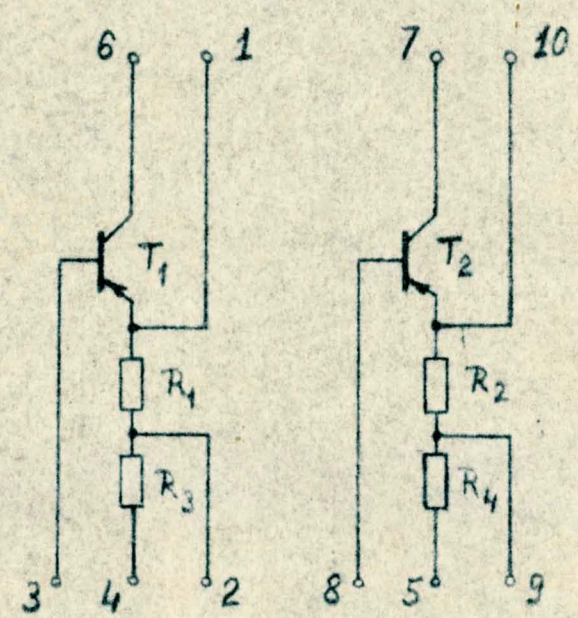
F F B.

Codenumber: 2P 727 07

	SHIFT REGISTER FLIP-FLOP Class B	SPECIFICATION PRR 23-3-295	/
GET.-DRAWN DESS.-GEZ. Dipl. Ing. Barany	DAT. 19.3.59	VERV.-SUPERS. REMPL.-ERS.	BL. SH.P. BL. SH.P.
N.V. PHILIPS' GLOEILAMPENFABRIEKEN EINDHOVEN — NEDERLAND			FORM. A4

ICOMA

1) Electrical Circuit



R_1 , R_2	330 ohm	± 15 %	65 mW
R_3 , R_4	1,5 kohm	± 15 %	100 mW
T_1 , T_2	OC-47	Normal spec.	

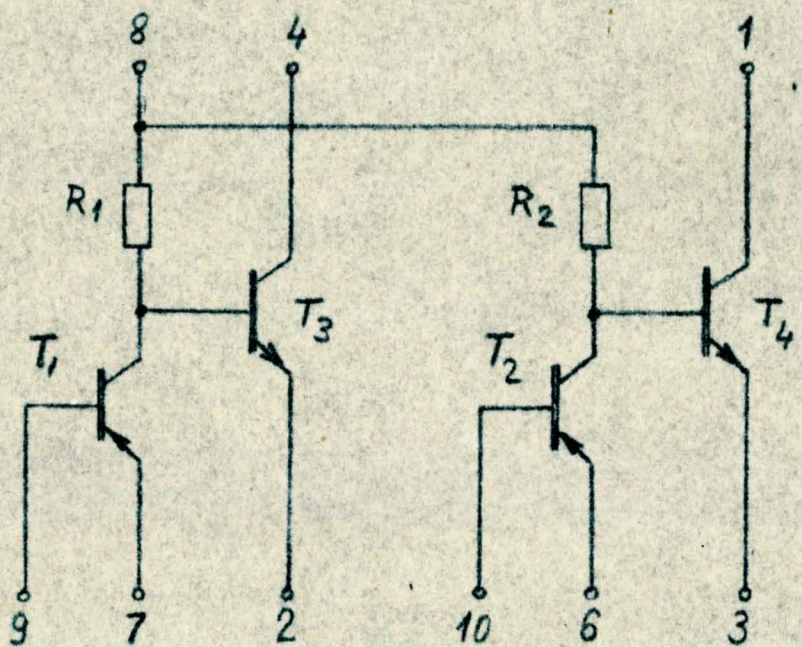
For reliable working the values of the components must be between the limits stated above.

Codenumber: 2P 725 00

	TWIN EMITTER FOLLOWER	SCHEMA (Provisional)	
	Class B	PRR 23-3-224	/
GET.-DRAWN DESS.-GEZ.	Dipl.Ing. Barany DAT 6.3.59.	VERV.-SUPERS REMPL.-ERS.	27.11.58.

ICOMA

1) Electrical Circuit



R_1, R_2	4,7 kohm	± 10%	30 mW
T_1, T_2	OC 47	Normal spec.	
T_3, T_4	OC 139	Normal spec.	

For reliable working the values of the components should be between the limits stated above.

Codenumber: 2P 604 91

TWIN CURRENT SWITCH

SPECIFICATION

PRR 23-3-249

GET.-DRAWN DESS.-GEZ. Dipl.Ing. Barany DAT. 19.3.59

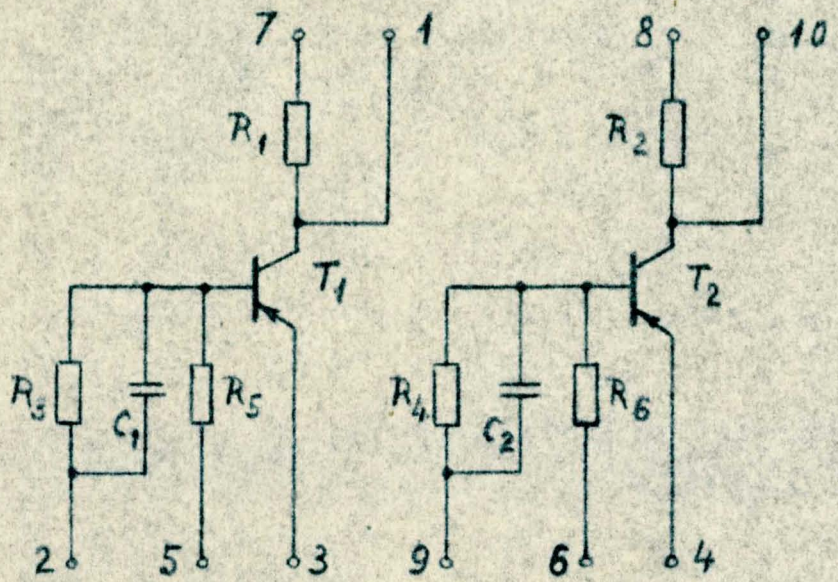
VERV.-SUPERS REMPL.-ERS.

N.V. PHILIPS' GLOEILAMPENFABRIEKEN EINDHOVEN — NEDERLAND

FORM. A4

ICOMA

1) Electrical Circuit



R_1 , R_2	1,0 kohm	± 10 %	36 mW
R_3 , R_4	6,8 kohm	± 10 %	6 mW
R_5 , R_6	52 kohm	± 10 %	1 mW
C_1 , C_2	470 pF	$\pm \frac{20}{30}$ %	30 V
T_1 , T_2	OC-47	Normal spec.	

For reliable working the values of the components must be between the limits stated above.

Codenumber: 2P 727 02

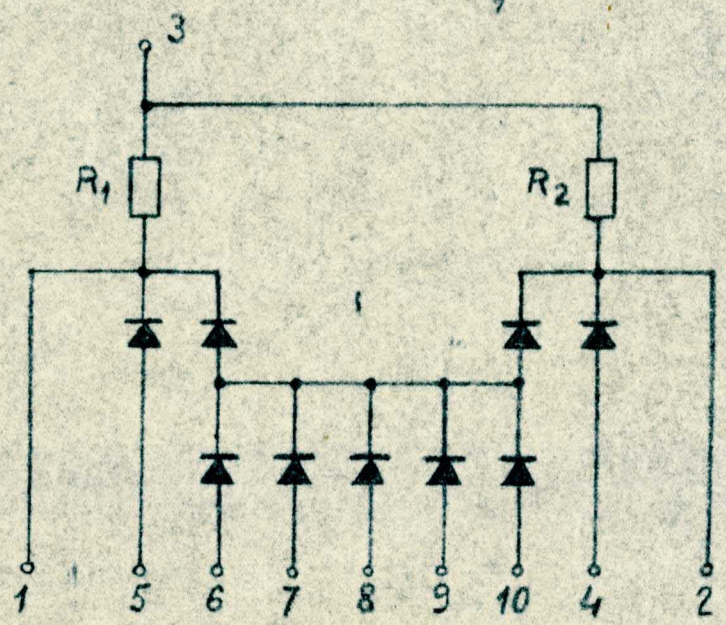
	TWIN INVERTER AMPLIFIER	SCHEMA (Provisional)	
	Class B	PRR 23-3-225	/
GET.-DRAWN DESS.-GEZ. Dipl.Ing. Barany	DAT 28.2.1959.	VERV.-SUPERS. REMPL.-ERS. 24.1.59.	

N.V. PHILIPS' GLOEILAMPENFABRIEKEN EINDHOVEN — NEDERLAND FORM. A4

37 120 90.5

ICOMA

1) Electrical Circuit



R_1, R_2	6,8 kohm	± 10%	6 mW
D_1 - D_9	OA 95	Normal spec.	

For reliable working the values of the components should be between the limits stated above.

Code number: 2P 604 90

	READ-WRITE GATE	SPECIFICATION PRR 23-3-250
GET.-DRAWN DESS.-GEZ.	Dipl.Ing. Barany DAT 19.3.1959	VERV.-SUPERS. REMPL.-ERS.

N.V. PHILIPS' GLOEILAMPENFABRIEKEN EINDHOVEN — NEDERLAND FORM. A4

37 120 90.5

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