Inverter for the Solar Panel using an MC56F8023

Designer Reference Manual

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Chapter 1
Introduction

1.1 Introduction

This designer reference manual describes a DC to AC inverter for the solar panel. This design example shows how to convert the small DC voltage with highly variable power from the solar panel to the AC output voltage 230 V / 50 Hz sine shape, see Figure 1-1 . The output power is sufficient to source small AC powered appliances or lights in the destinations without a power grid. The aim of this design is to present the maximum power point tracking (MPPT) feature. Using the Freescale MC56F8023 device ensures cost-effective implementation for this type of inverter application.

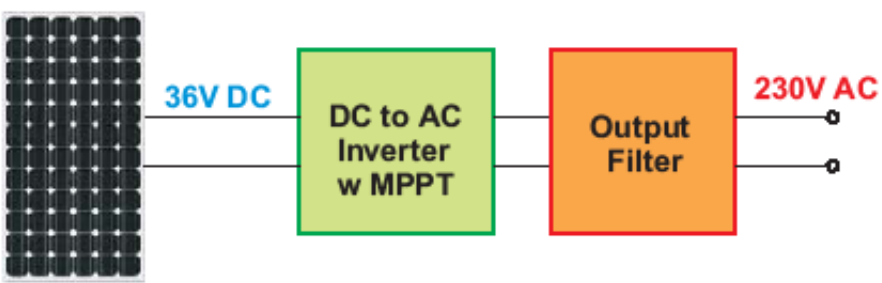


Figure 1-1. Inverter principle connection

The overall structure of this inverter can be split into two sections, the primary low voltage input side and the isolated secondary high voltage output side. The main control unit–digital signal controller (DSC) is placed on the primary side to start to run when the solar panel starts to source minimum output power. The power conversion from the DC low voltage to the high voltage DC bus is maintained by the standard push-pull type converter and isolation power transformer. The conversion from the high voltage DC bus to the standard AC power line voltage is maintained by the inverter in the full-bridge configuration. The standard AC output filter is placed at the output to meet the output voltage regulations.

The main design parameters are chosen to reach a wide range of usability:

- The inverter can be powered by one solar panel with the 36 V DC nominal output voltage or by two solar panels connected in series each with the 18 V DC nominal output voltage.
- The inverter can also be powered by the three pieces of the lead-acid accumulators connected in series. The battery charger can be implemented as the software (SW)option.
- The maximum output power depends on the solar panel properties and can reach up to 400 VA.
- The output voltage is 230 V / 50 Hz + 10 %.
- Pure sine output voltage with a maximum of 3% harmonic distortion.
- The input under-voltage and output over-current protections implemented
- Hardware for the isolated RS-485 communication line built. The communication protocol can be implemented in accordance to the final requirements..
- Efficiency better than 80 %.
- MPPT implemented, and the P&O method used.

1.2 Freescale Digital Signal Controller Advantages and Features

The Freescale MC56F80xx family is well suited for digital control, combining the DSP's calculation capability with the MCU's controller features on a single chip. These hybrid controllers offer many dedicated peripherals such as pulse width modulation (PWM) modules, analogue-to-digital converters (ADC), timers, communication peripherals (SCI, SPI, I2C), and on-board Flash and RAM.

The MC56F80xx family members provide the following peripheral blocks:

- One PWM module with PWM outputs, fault inputs, fault-tolerant design with dead time insertion, supporting both centre-aligned and edge-aligned modes
- 12-bit ADC, supporting two simultaneous conversions; ADC and PWM modules can be synchronized
- One dedicated 16-bit general purpose quad timer module
- One serial peripheral interface (SPI)
- One serial communications interface (SCI) with LIN slave functionality
- One inter-integrated circuit (I2C) port
- On-board 3.3 V to 2.5 V voltage regulator for powering internal logic and memories
- Integrated power-on reset and low voltage interrupt module
- All pins multiplexed with general purpose input/output (GPIO) pins
- Computer operating properly (COP) watchdog timer
- External reset input pin for hardware reset

- JTAG/On-Chip Emulation (OnCE™) module for unobtrusive, processor-speed-independent debugging
- Phase-locked loop (PLL) based frequency synthesizer for the hybrid controller core clock, with on-chip relaxation oscillator

Table 1-1. Memory configuration

Memory Type	MC56F8013	MC56F8023
Program Flash	16 KByte	32 KByte
Unified Data/Program RAM	4 KByte	4 KByte

The PWM block has the following features:

- Three complementary PWM signal pairs, six independent PWM signals (or a combination)
- Complementary channel operation features
- Independent top and bottom dead time insertion
- Separate top and bottom pulse width correction via current status inputs or software
- Separate top and bottom polarity control
- Edge-aligned or centre-aligned PWM reference signals
- 15-bit resolution
- Half-cycle reload capability
- Integral reload rates from one to sixteen periods
- Mask/swap capability
- Individual, software-controlled PWM output
- Programmable fault protection
- Polarity control
- 10 mA or 16 mA current sink capability on PWM pins
- Write-protectable registers

The ADC module has the following features:

- 12-bit resolution Dual ADCs per module; three input channels per ADC Maximum ADC clock frequency of 5.33 MHz with a 187 ns period
- Sampling rate of up to 1.78 million samples per second
- Single conversion time of 8.5 ADC clock cycles (8.5 x 187 ns = 1.59 ms)
- Additional conversion time of six ADC clock cycles (6 x 187 ns = 1.125 ms) Eight conversions in 26.5 ADC clock cycles (26.5 x 187 ns = 4.97 ms) using parallel mode
- Capability to use the SYNC input signal to synchronize with the PWM (provided the integration allows the PWM to trigger a timer channel connected to the SYNC input)
- Capability to sequentially scan and store up to eight measurements
- Capability to scan and store up to four measurements on each of the two ADCs operating simultaneously and in parallel
- Ability to scan and store up to four measurements on each of the two ADCs operating asynchronously to each other in parallel

- Interrupt generating capabilities at the end of a scan when an out-of-range limit is exceeded and on a zero crossing
- Optional sample correction by subtracting a pre-programmed offset value
- Signed or unsigned result
- Single-ended or differential inputs
- PWM outputs with hysteresis for three of the analogue inputs

The quad timer is an extremely flexible module, providing all required services relating to time events have the following features:

- Four 16-bit counters/timers
- Count up/down
- Counters are cascadable
- Programmable count modulus
- Maximum count rate equal to the peripheral clock/2, when counting external events
- Maximum count rate equal to the peripheral clock/1, when using internal clocks
- Count once or repeatedly
- Counters are preloadable
- Counters can share available input pins
- Each counter has a separate prescaler
- Each counter has capture and compare capability

The application uses the ADC block in single conversion mode. The start of conversion is synchronized to the PWM pulses. The PWM module provides the PWM Reload signal to start the counting on the timer channel 3. This timer channel comprises value, which represents the required delay between the PWM start edge and the ADC conversion moment. When timer channel 3 finishes counting, it provides the synchronization impulse called SYNC0 to start the ADC conversion on the ADC0 module. This configuration allows the synchonized conversion of all the currents and voltages within the required time.

The interrupt controller (INTC) provides the option to set the priority level for each interrupt used. The PWMReload interrupt has the highest priority level. On the other side, the interrupt service routine must last as short a time period as possible.

The next priority level is assigned to the fault interrupt service routine. Usually the fault interrupt has higher priority, but in this design the fault conditions are solved by the hardware.

The lowest priority is assigned to all other interrupts. The swi interrupt and the PIT0 interrupt are used. The swi interrupt is generated by the fourth PWM interrupt and starts the all computation routines. The PIT0 interrupt is exclusively used only for the demo mode of this inverter. It makes the short 1 second delay after such fault condition and restarts the inverter. The fault condition is signalized by the red LED on the front panel.

Chapter 2
System Concept

2.1 System specification

The system is designed to convert the low voltage DC power from the solar panel to the power line level AC voltage 230 V 50 Hz. The application meets the following performance specifications:

- Control of the PWM push-pull DC to DC converter
- Control of the PWM full-bridge DC to AC inverter through the digital isolator
- Control of the PWM two phase SEPIC converter for the battery charger (as option)
- Direct input voltage and current sensing by integrated on-chip analog to digital converter (ADC)
- Direct battery voltage sensing by the integrated on-chip ADC
- Direct DC-bus voltage sensing through the isolated analog amplifier and on-chip ADC
- Direct output AC voltage and AC current sensing through the isolated analog amplifiers and on-chip ADC
- Maximum power point tracking technique (MPPT) P&O method used
- Pure sine voltage generation by the PWM control
- Input under-voltage protection implemented in software
- Output high and low voltage limits implemented in software
- Output over-current protection implemented in both - hardware and software
- Isolated RS-485 communication line on board

2.2 Inverter topology concept

A standard inverter topology is chosen to meet the basic specification(see Figure 2-1). The system incorporates the following blocks:

- Solar panel
- DC to DC Converter with MPPT implemented
- DC to AC inverter
- Output filter

- Control unit with DSC MC56F8023
- Battery charger (as option)

The MC56F8023 executes the control algorithm. In response to the input power from the solar panel and feedback signals, it generates PWM signals for the push-pull DC to DC converter on the low voltage side and the PWM signals for the AC pure sine voltage generation on the isolated secondary side. High-voltage waveform generated by the DC to AC inverter goes throught the output filter to the output connector. The hardware circuitry is designed for the Off-Grid mode and for On-Grid mode. The hardware for the battery charger is also on the main board. This inverter includes the maximum power point tracking (MPPT) feature to achieve the maximum efficiency of the energy harvesting. The software for the battery charger is not yet implemented. The aim is to implement it in the second phase of the project.

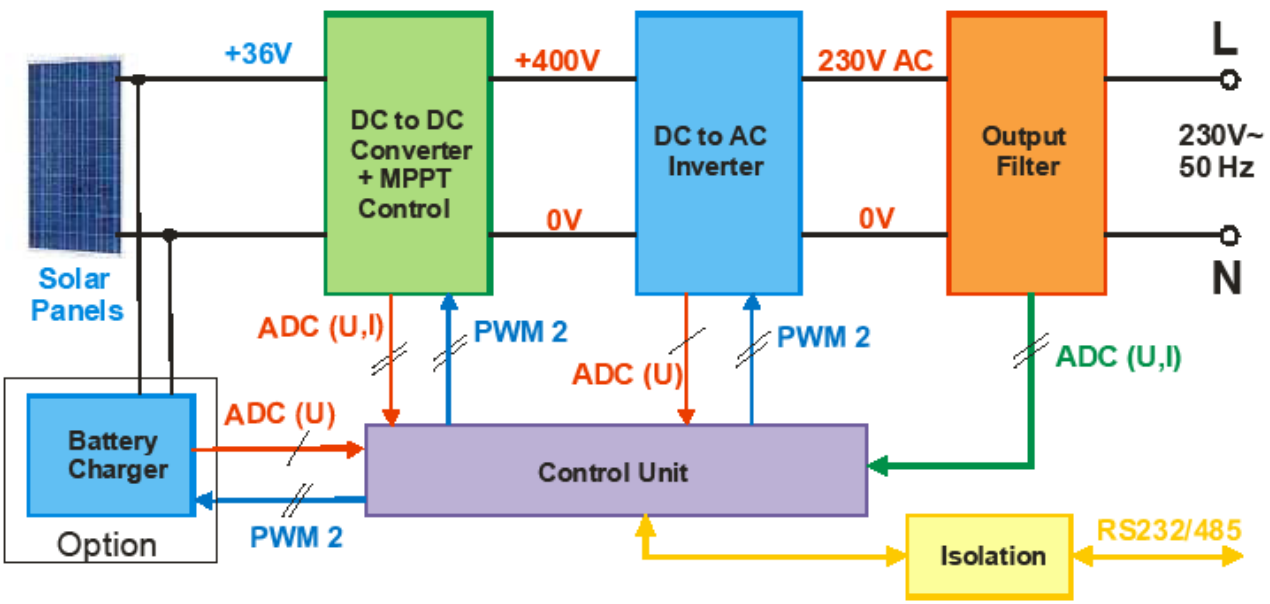


Figure 2-1. Inverter block schematic

2.3 Control process

The state of the status switch (On/Off switch as user interface) and the input voltage level from the solar panel is scanned periodically. When the inverter is switched on and there is enough voltage on input (more than 18 V), the control board starts to generate the PWM on the primary side of the DC to DC converter. The PWM on the low voltage primary side is generated, while the DC-Bus voltage reaches the required high voltage level. When the DC-bus capacitor is charged, the control board starts to generate the PWM for

the DC to AC inverter. The generated AC output voltage and current, the DC-bus voltage, the input voltage and current from the solar panel, and the battery voltage are measured periodically to provide the accurate information for the control board.

The ADC sampling is triggered by QuadTimer channel 3 and synchronized to the PWM signal. The PWM is set in the center aligned mode with positive polarity. The primary side of the DC to DC converter is controlled by the two PWM channels in the independent mode. This mode allows proper control of the push-pull stage on the primary side of the power transformer. The sampling moment is variable and is set by the control software in accordance to the duty-cycle of the PWM on the primary side. This synchronization ensures ADC sampling while the input signals are free of noise.

The MPPT is implemented. Due to this feature, the are two possible output power states in the Off-Grid mode:

- The output load of the inverter is lower than the ability of the solar panel to source the inverter. Therefore the generated output voltage is on its highest level and the maximum power point of the solar panel is not reached
- The output load of the inverter is a bit higher than the ability of the solar panel to source the inverter. In this case the output voltage will be set at the level that corresponds to the maximum power point of the solar panel. Simultaneously, in the normal working mode the output voltage must achieve the output voltage regulation.
- The overall state of the application is controlled by an application state machine (see Figure 2-2). The application state machine (ASM), consists of init, stop, switch check, start up, run, switch off and error states.

In the case of an overcurrent condition, the signals for the inverter are disabled and the fault state is entered.

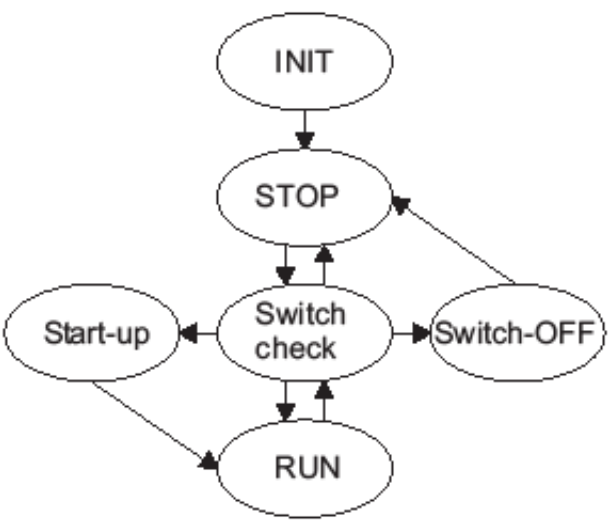


Figure 2-2. Inverter state diagram

In the demo control software the FAULT state lasts only one second. The fault LED shines during this time interval to show the state of the inverter. Then the control software makes the initialization and runs the start-up of the inverter. In case the overload conditions pertains, the fault cycle repeats.

2.4 MPPT description

The DC output power sourced from the solar panel is periodicaly computed. The P&O algorithm for the MPPTT is applied, (see Figure 2-3).

This method is based on the simple and effective P&O algorithm. In the one power point P1, you can try to sink higher power from the solar panel by inceasing the current from the panel. This implies a new power point P2. The actual new power is calculated as the input voltage multiplied by the input current. This value is compared with the previous sampled value. If the new power value is higher than the previous value, the input power grows. Thus, the moving direction of the power curve is correct. In the next step you can try to sink still higher current from the panel. The power measurement in the new point can be P3 in comparision with the previous value. The next step is analogic—this is in case the output power from the solar panel is lower (Pn)—go back and try to find the point, where the sourced power from the panel is highest. Arrows in Figure 2-3 show the moving direction of the new power point. The incremental step depends on the power change in the previous step. If the power change is higher, the next step is higher. If the power change is smaller, the step to the next power point is also smaller. The power curve on the top (in the Pmax point) is horizontally flat. This means, the power change is small and the step change is also small. Thus the maximum power point catch is very accurate. The frequency of checking the power delivered by the solar panel must be sufficiently high to properly track the MPP when the illumination conditions are quickly changed. The system was tested by the intensive deeply changing weather (illuminating) conditions, the MPP tracking was quick and accurate.

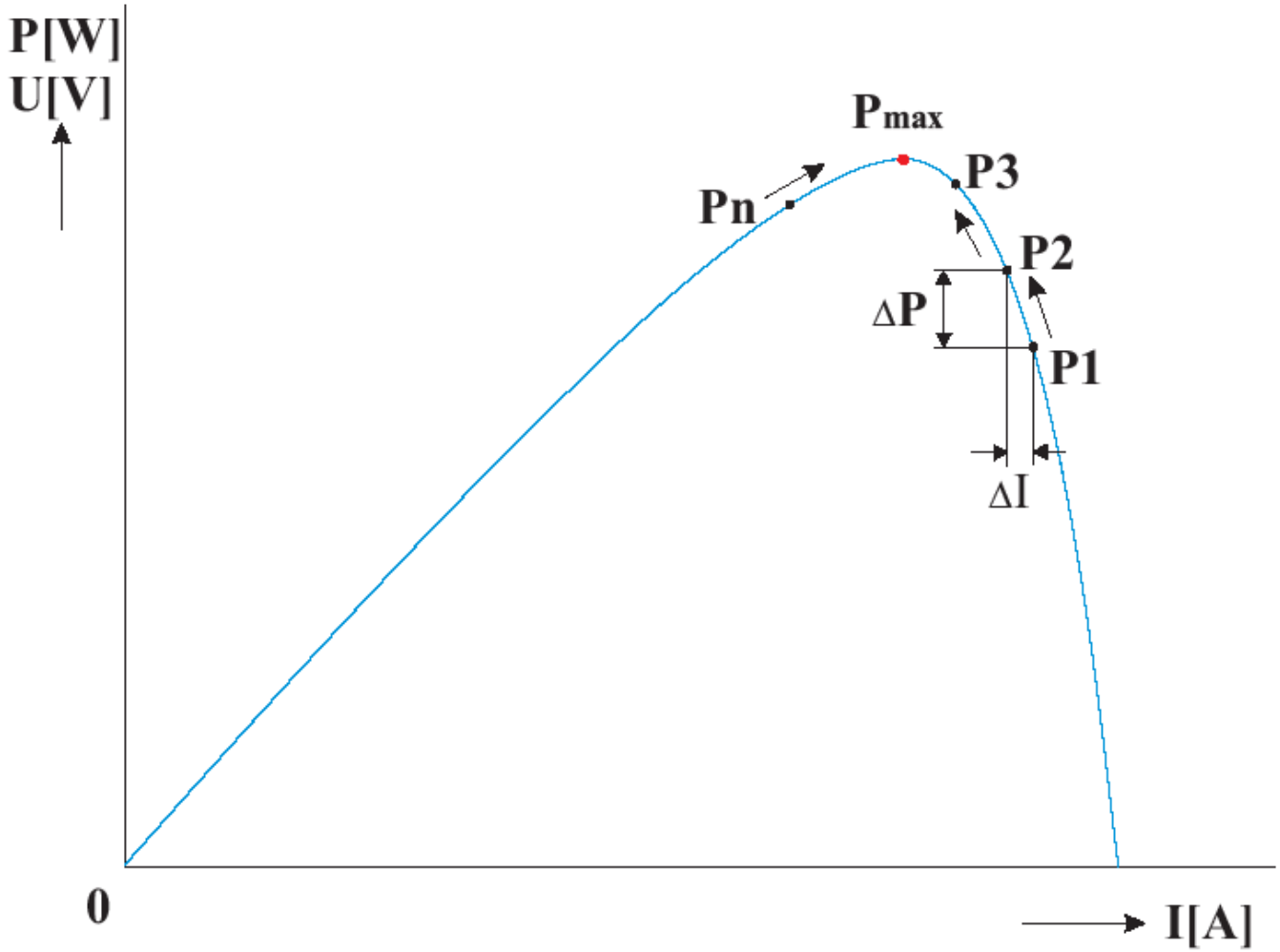


Figure 2-3. MPPT feature

Chapter 3
Hardware Parts Description

3.1 Topology

The inverter is split into two boards:

- Main power board
- Controller board

A detailed topology is shown in Figure 3-1 .

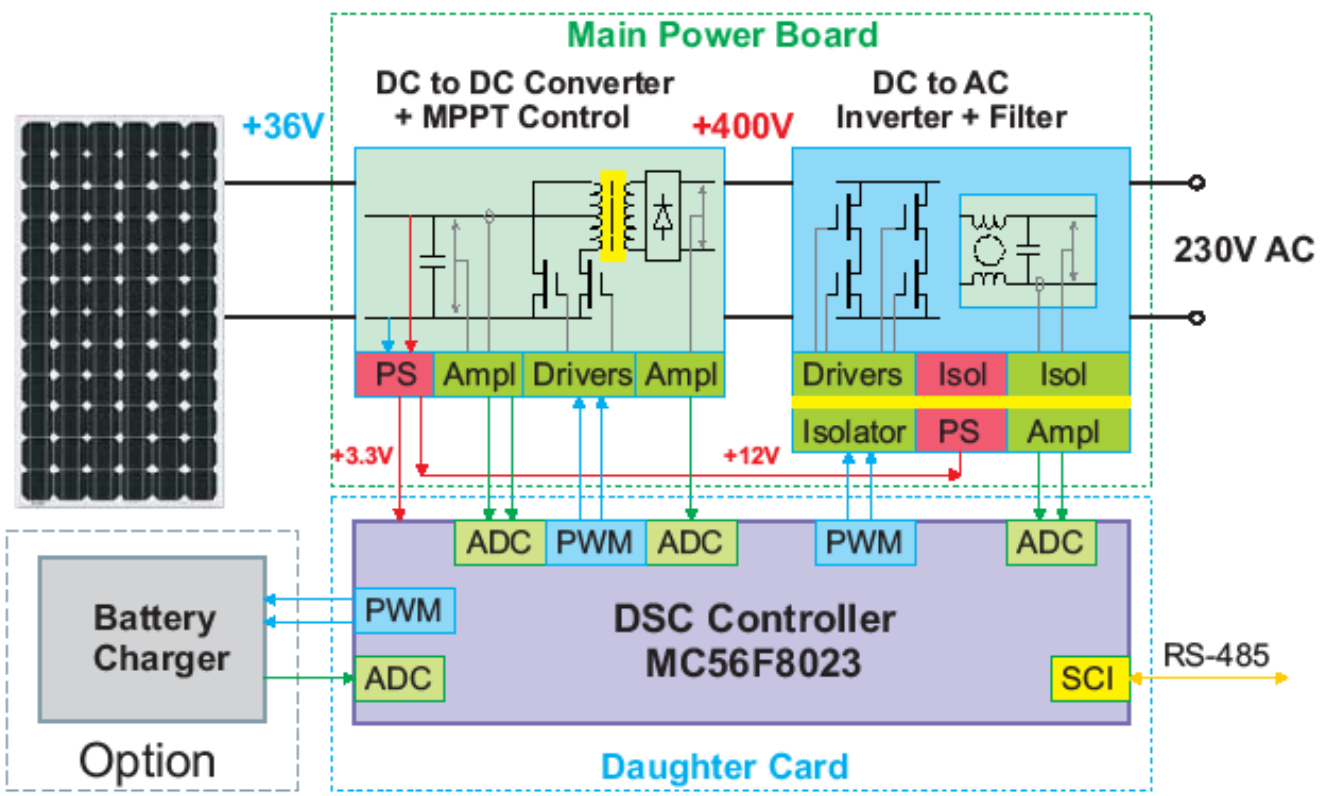


Figure 3-1. Detail block schematic

The main power board is comprised of all the power circuitry. In Figure 3-1 the green box on the left shows the DC to DC converter with the associated input LC filter, auxiliary DC power supply, MOSFET drivers for the low voltage side, and the analogue amplifiers that form the analogue signals for measurements.

The blue box on the right side represents the isolated high voltage section. In this section, the inverter in the full-bridge configuration, the output filter, isolated DC to DC power supply for the MOSFET drivers, and the linear analogue isolation amplifiers. The yellow line represents the isolation barrier.

On the main power board there are also power circuits for the optional battery charger (the grey box in Figure 3-1).

The whole inverter is controlled by the DSC placed on the small daughter card. This topology provides the option to use other suitable DSCs for the inverter control. The connection to the main board is made by the PCI edge connector. The violet box in Figure 3-1 represents the DSC control board. The blue PWM boxes are control outputs, the green ADC boxes are the inputs for the analogue measurements, and the yellow SCI box that represent the communication interface to the RS-485 line.

The red PS boxes represent the auxiliary power supplies, non-isolated for the low voltage primary side and isolated for the high voltage secondry side of the inverter.

Each block will be described in detail.

3.1.1 Auxiliary DC power supply

The auxiliary power supply works independently of the main push-pull converter and provides:

- +12 V for the MOSFET drivers on the primary low voltage side
- +5 V for the output analogue part of the isolation amplifiers
- +3.3 V analogue for the operational amplifiers for measurements
- +3.3 V digital for the DSC supply

Figure 3-2 is the block schematic of the low power DC power supplies. The input comparator senses the DC input voltage from the solar panel, where this level is lower than +18 V, the main DC to DC converter for +12 V is blocked and the whole inverter is internally powered down. The +12 V output voltage is used to power the gate drivers of the MOSFETs on the low voltage side and as the power source for the +3.3 V and +5 V supply lines. The +3.3 V level is split into two lines, analogue and digital. The +5 V line is used as an analogue line to only power the output site of the analogue isolation amplifiers.

The isolated DC to DC converters are powered by the main +12 V line. The first converter provides the isolated output voltage of +15 V for the MOSFET drivers for the full-bridge inverter, and +5 V for the isolated input side of the analogue isolation amplifier which is for the DC bus voltage measurement. The second isolated DC to DC converter provides the power for the isolated input side of the analogue isolation amplifier which is for the output voltage and current measurement.

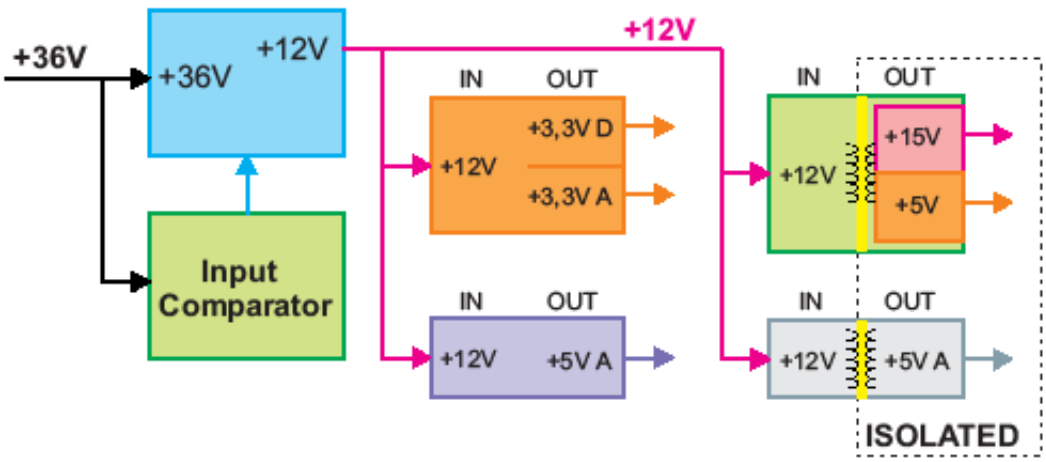


Figure 3-2. DC power supplies

These isolated transformer based high frequency DC to DC converters are dedicated integrated circuits with a 5 kV isolation capability between the input and output side. The output power reaches 2 W or 1 W respectively. This is sufficient for powering the active components on the isolated output side of the inverter.

3.1.2 Push-pull converter

There are several types of topologies that can be used for the power conversion from a +36 V low voltage to a +400 V high voltage. The selected push-pull topology is shown in Figure 3-3 .

There are several reasons to select the push-pull topology:

- One switch is connected in series with the primary winding to the low input voltage
- Good power utilization of the transformer core
- Simple to make two equal primary windings on the transformer
- Lower current through the transformer's windings.

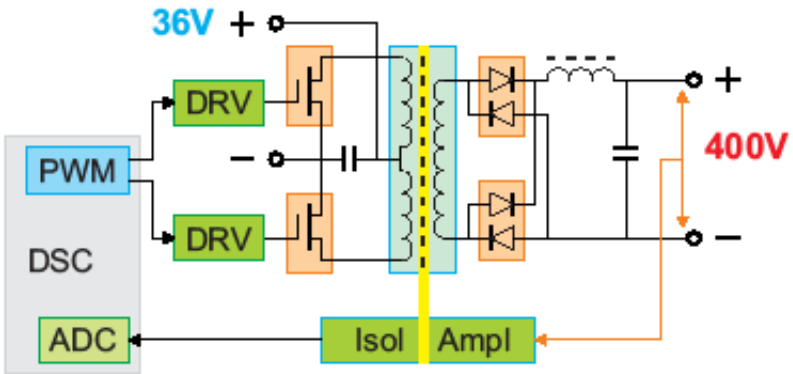


Figure 3-3. Push-Pull topology of the DC to DC converter

The nominal input voltage from the solar panel is +36 V or +25 °C. This depends on the temperature of the silicon plates with a negative coefficient of –0.38 % or °C. In summer working conditions, expect the panel temperature to be as high as +55 °C. Then the nominal output voltage can only reach +32 V , or less. The lowest voltage on the primary winding of +32 V was chosen, this is due to voltage drops on the MOSFETs and other serial connections of such a margin.

The conversion ratio of the transformer is:

Eqn3.1

$$p = Ns/Np = (Vout)/(Vin * D) = 14;$$

The EPCOS's freeware for the transformer design was used for detail design of the power transformer. The result is:

- ETD49 core, N87 material, no gap
- Primary windings 2 x 8 turns bifilar, Litz wire 1.6 mm dia
- One secondary winding 116 turns, 2 x 0.45 mm dia in parallel
- Primary and secondary windings have >4 kV isolation

The best option is to use the lowest possible switching frequency for the DC to AC inverter. On the other side, the switching frequency for the power transformer has to be higher—about 50 kHz to 100 kHz for the rated transferred power. A higher frequency is better for the core utilization, a lower frequency is better for lower switching losses in the MOSFETs used. The DSC's PWM module uses the same frequency for all the generated control signals by the PWM channels, the push-pull DC to DC converter, and for the full-bridge inverter. A 26 kHz switching frequency was then used as the compromise between these two requirements. The standard Graetz topology rectifier is used on the secondary side to take the required DC-bus voltage. The fast switching diodes are used for this purpose.

3.2 Measurement circuits

The control algorithm requires sensing the following quantities:

- Input voltage and current from the solar panel
- Battery voltage
- DC-bus voltage (isolated)
- Output AC voltage and current (isolated)
- The input voltage and the battery voltage are sensed by a standard resistor divider, followed by an operational amplifier. The output of the operational amplifier is then connected to the ADC input pin of the DSC controller. This circuit is shown in Figure 3-4.

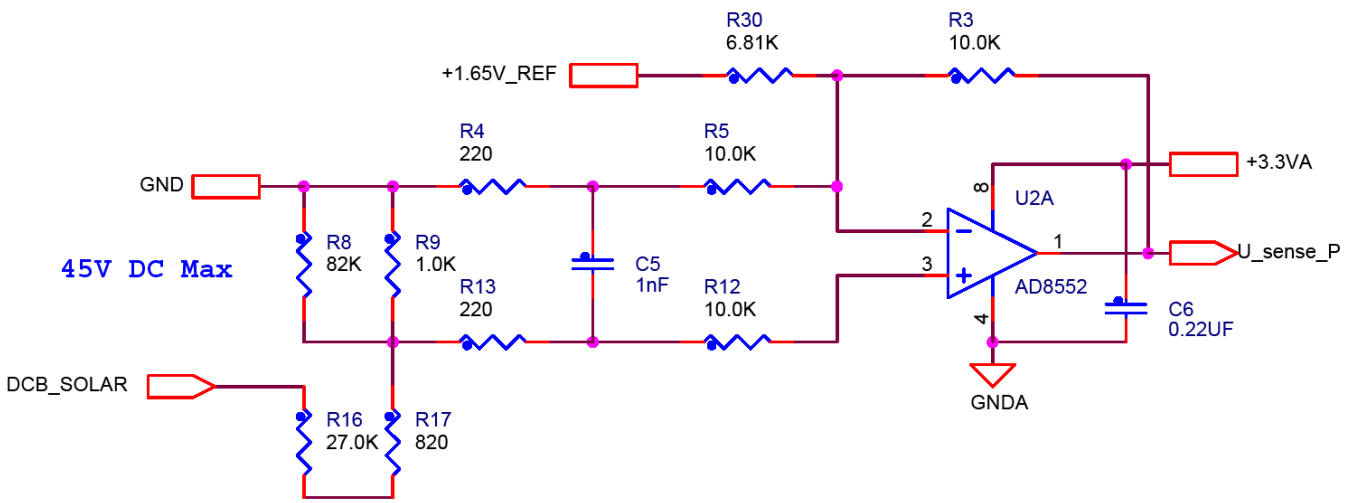


Figure 3-4. Input voltage sense circuit

The current sourced from the solar panel is sensed by the high-side current sense amplifier and the current sense resistor. The output voltage from this sensor is measured by the ADC of the DSC controller. This circuit is shown in Figure 3-5.

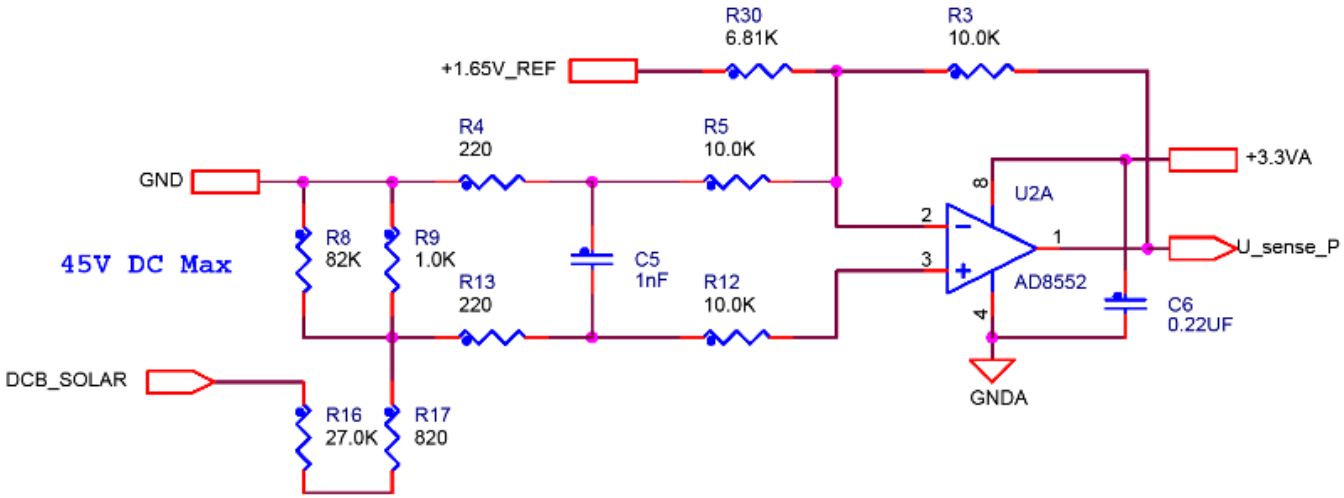


Figure 3-5. Current sense circuit

The voltages and the current on the high voltage isolated side are measured by the isolation amplifier followed by the standard operational amplifier. The resistor divider is used to sense the DC-bus voltage and the output phase voltage. The shunt resistor is used for the phase current sense. This circuit is shown in Figure 3-6

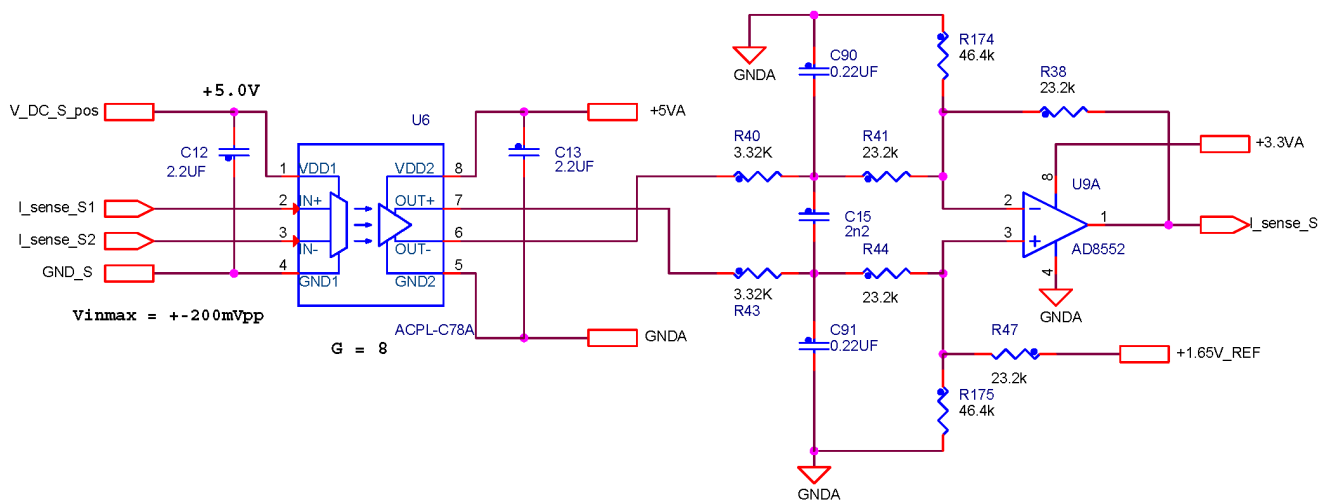


Figure 3-6. Isolation Amplifier for current or voltage

.

The MOSFET switching on the primary side of the push-pull converter generates a noise that can influence the measurement accuracy. All measurements must be executed while the currents through the primary windings are in a stable state. Therefore, the ADC sampling has to be synchronized with PWM generation. This can be ensured by the PWM to ADC synchronization implemented on the MC56F8023. This synchronization is performed by the third channel of the quad timer, where it is connected to the

synchronization input of the A/D converter, and the input of the same channel is connected to the reload signal of the PWM module. Thus, the quad timer channel 3 allows control of the delay between the PWM module reload event and the start of A/D conversion.

3.3 DSC, drivers and control circuits

The digital signal controller (DSC) MC56F8023, is the core of the whole inverter. It measures all the analogue quantities (the input and output voltages and currents) required for control, senses the main on and off switch, controls all the switches (MOSFETs) in accordance with the control algorithm, and provides the information of the actual state of the inverter, via the two LEDs on the front panel. It also can provide the main status information by the isolated RS-485 communication line. The appropriate communication protocol that meets the application requirements can be implemented in software.

The external hardware overcurrent fault circuitry on the primary side—one for each of the push-pull transistors, and also on the ground line of the DC-bus—protects the whole full-bridge inverter against overcurrent. When an overcurrent condition arises, this circuit switches off immediately the entire full-bridge and sends a signal to the DSC to block the PWM generation. See the detailed schematic.

The DSC generates the low level digital control signal for the power MOSFETs drivers. The drivers output this signal with the appropriate voltage and power ability to switch on or switch off the power MOSFETs. This circuit is shown in Figure 3-7.

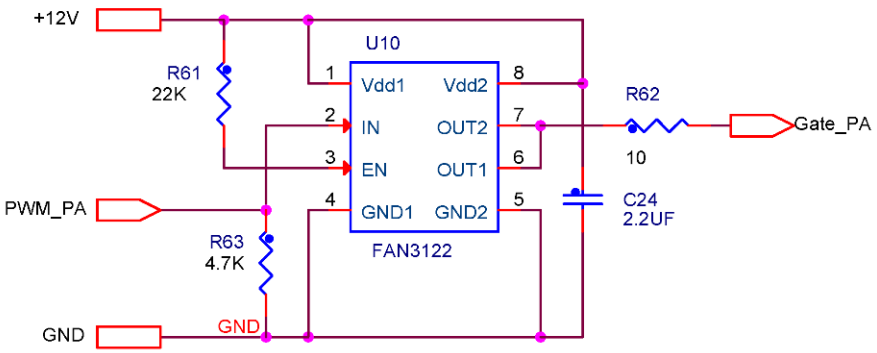


Figure 3-7. Low side driver

Standard low side drivers are used on the low voltage primary side of the push-pull converter.

3.4 Full-bridge inverter

To drive the high voltage full-bridge inverter, high voltage half-bridge drivers are used. Each driver, drives a low side and high side MOSFET. Both drivers receive the same PWM control signal, but one of them has its inputs swapped. With this connection, it is possible to control the entire full-bridge inverter by one complementary PWM pair. This circuit is shown in Figure 3-8.

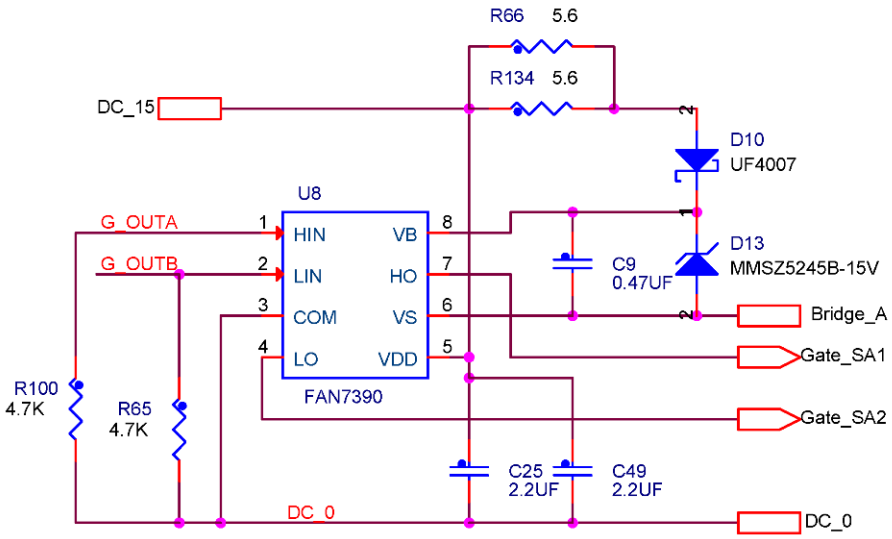


Figure 3-8. Half-bridge driver

The full-bridge topology for the inverter was selected because it only needs a +400 V DC-bus to generate a 230 V AC output voltage. The control of this topology is simple, it takes only two PWM channels. The simplified schematic can be seen in Figure 3-9.

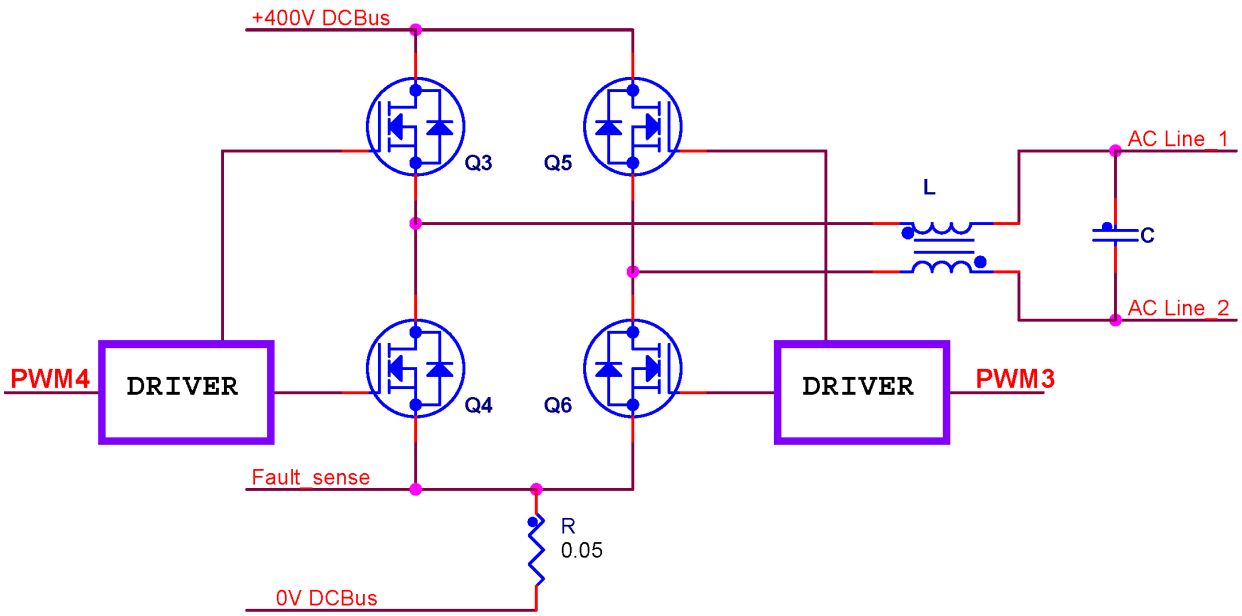


Figure 3-9. Full-bridge inverter topology

The bipolar type of the switching control is used and can handle better the non-resistive loads. The high voltage half-bridge drivers are used for driving the switching MOSFETs. The drivers receive the control PWM signal from the DSC through the digital isolator. The overcurrent in this inverter is sensed by the current sensing resistor R. The voltage drop sensed at this resistor inputs to the high speed analogue comparator. In the case of a fault, the output from this comparator immediately blocks the input signal to the drivers by the NAND gates. It then sends the fault information to the DSC through the isolation optocoupler. This configuration in the case of an overcurrent event, maintains the hardware based high speed switch-off of the entire full-bridge.

The switching MOSFETs are used as the active devices in the full-bridge inverter because of their good switching performance, low gate charge, high switching speed, and low serial resistance in the open state.

All these properties together maintain the low switching losses, even if the relative high switching frequency is used. A higher switching frequency enables the use of a relatively low output inductance L and output capacitance C to reduce the EMI. But a higher

switching frequency implies higher switching losses. Thus, the switching frequency of 26 kHz is selected as a compromise between switching losses, output filter dimension, and the ability of the power transformer to pass the power through.

3.5 Output filter

The role of the output filter is to convert the high frequency PWM modulated voltage to the low frequency sine shape voltage. The simplest way for the cut-off frequency selection is to use the average frequency in the logarithmic scale. A slightly higher frequency –2kHz was used. The filter with this cut-off frequency has good filtering properties for the 26 kHz PWM switching frequency, and has practically no attenuation for the low frequency 50 Hz. A further EMI filter is used at the output of the inverter to still improve the EMI properties.

The output relay K2 (see detailed schematic) is used for the hard power line connection. In the case of Off-Grid mode, the relay is switched on on the start of the output sine voltage generation. In the case of ON_GRID mode, the relay is switched on after the phase synchronization between the power line voltage and the software for the sine voltage generation.

3.6 MC56F8023 Debugging circuitry

The main DSC (MC56F8023) is located on a small control module. It includes an MC56F8013 or MC56F8023 part, a small power supply, input for the external power voltage source from 5.5 V to 30 V, the LED indicator for power, JTAG interface, and the basic input filters for the all ADC inputs. A PCI Express edge connector on one side of the board provides all the power and signal connections to the application. It can be used in the development of applications using the MC56F8013/23 targeted at motor control and power management applications.

The MC56F8013/23 Controller Board is flexible enough to allow full exploitation of the MC56F8013/8023's features to optimize the performance of the end product.

Chapter 4
Software Description

4.1 Introduction

This section describes the software blocks used in the inverter control. The software description is split into two main parts:

- The main software flow chart
- Interrupt routines description

4.2 Main software flow chart

The main flowchart consists of a standard init routine, the main loop, and the block of interrupts routines (see Figure 4-1). The appropriate interrupt service routines run the code for each individual event in accordance to their priority level.

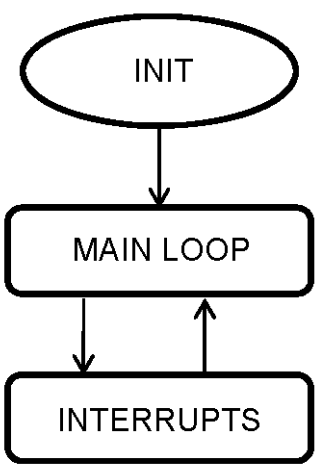


Figure 4-1. Main flow chart

4.2.1 INIT Routine

The INIT routine is the first and main initialization routine. It starts immediately after the DSC turns on.

This routine initializes all the used internal peripheral modules:

- COP
- SYS
- GPIO
- PIT_0
- SCI
- QTIMER
- Interrupt controller

The PWM module is initialized by its own routine, which is generated by the software tool QuickStart integrated in the CodeWarrior software design tool. Using the QuickStart tool, you can set all the required parameters for all the internal peripheral modules. The next routine initializes the important variables.

4.2.2 Main loop

The main loop is comprised of the software routine, which does not require an exact time scheduling. These software routines check the status of the main On/Off switch, DC-bus voltage level, and input power sourced from the solar panel. It also measures the power line output voltage and current, and for the debug option runs the FreeMASTER communication routine. All software routines included in this main loop are described in detail in the following sections.

4.2.3 Interrupts

The block of interrupts in Figure 4-1 comprises all software routines, that must run the code in exactly the scheduled time. Each routine has its own priority level. This level is set in the quick start window in accordance with the importance of the event. All interrupt routines are described in detail in Section 4.4 Interrupt service routines description .

4.3 Main loop software routines

A detailed flowchart of the main loop is shown in Figure 4-2.

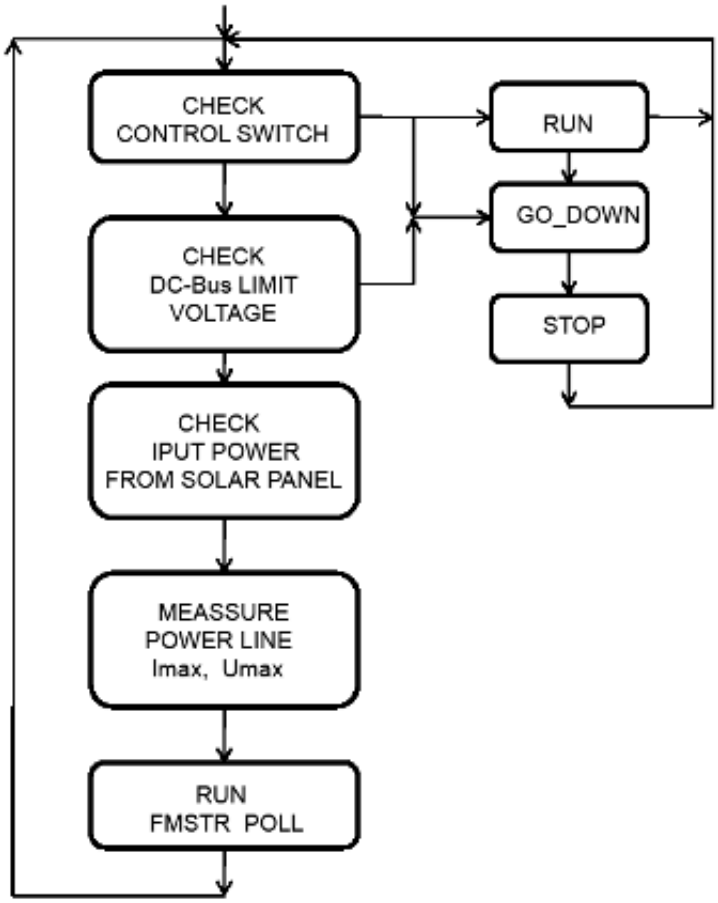


Figure 4-2. Main loop structure

4.3.1 Check control switch routine description

This routine periodically checks the status of the main On/Off switch. The output from this routine is the value of the u8StartSwitch variable. There are two possible values: RUN and STOP. The de-bounce property is also implemented.

4.3.2 Check DC-bus limit voltage

The DC to AC inverter must comply with the output voltage range rules. The output voltage must be in the range of 230 V AC–10% to 230V AC +10%. The output true sine shape voltage is generated from the DC-bus voltage, multiplied by a sine waveform with a constant amplitude equal to one. Thus, the amplitude of the output voltage can be controlled by the DC-bus voltage level. In accordance with the mentioned rules, the DC-bus minimum voltage is:

Eqn 4.1

$$Umin = (230*0.9)*1.41 + Usw = 295V$$

The Usw voltage represents the voltage on the opened MOSFET switches plus voltage damping on the output inductor – roughly 3 V altogether.

Analogically the DC-bus maximum limit voltage is:

Eqn 4.2

$$Umax = (230*1.1)*1.41 + Usw = 360V$$

This information is important only for the Off-Grid mode, where the inverter generates the output voltage autonomically. If the solar panel can not provide sufficient power through the inverter to the load, the generation of the output voltage is switched off. This is important only for some types of loads, for example, a refrigerator. It is not important for resistive type of loads–for example, with standard bulbs.

The main task for this solar panel inverter demo is to present the MPPT feature. For this reason the DC-bus voltage low limit is moved to a low level, about 25 V AC. It is possible to show the output power variation from the solar panel through its dependence on rapidly changing illumination conditions. The inverter properly selects the maximum power point even if the output power from the solar panel is too low.

4.3.3 Check input power from the solar panel

The DC output voltage and output current sourced from the solar panel are measured, and the output power is computed periodically. The P&O algorithm is applied for the MPPT, as described in Section 2.4. The PWM signals for the primary side of the DC to DC converter are generated in accordance with this MPPT algorithm, and the output power from the solar panel stays at the highest possible level.

4.3.4 Power line output measurement

The next task in the main loop is the power line output voltage and output current measurement. These two values provide the information on the output status of the inverter. This information can be sent by the RS-485 line to the higher supervisor system or can be used for some other computation. In the software, the peak and effective values of the voltage and current are available.

4.3.5 FreeMASTER poll routine

The final task in the main loop is the FreeMASTER routine. This routine provides information on the selected variables for the debug option. The SCI module is used as the communication line. In the real application the FreeMASTER poll routine is not used and the SCI module provides valuable information through the RS-485 isolated hardware interface.

4.4 Interrupt service routines description

All service routines are split into three priority levels. See Figure 4-3 .

4.4.1 PWM_Reload Interrupt

The highest priority is the interrupt service routine for the PWM reload. This part of code must be executed in the strictly defined time period.

The first task of this routine is the synchronization between PWM generation and the ADC sampling period. This is executed by writing the new value into the QTimer_3 register. Output from this timer channel is the impulse that starts the ADC sampling period and conversion.

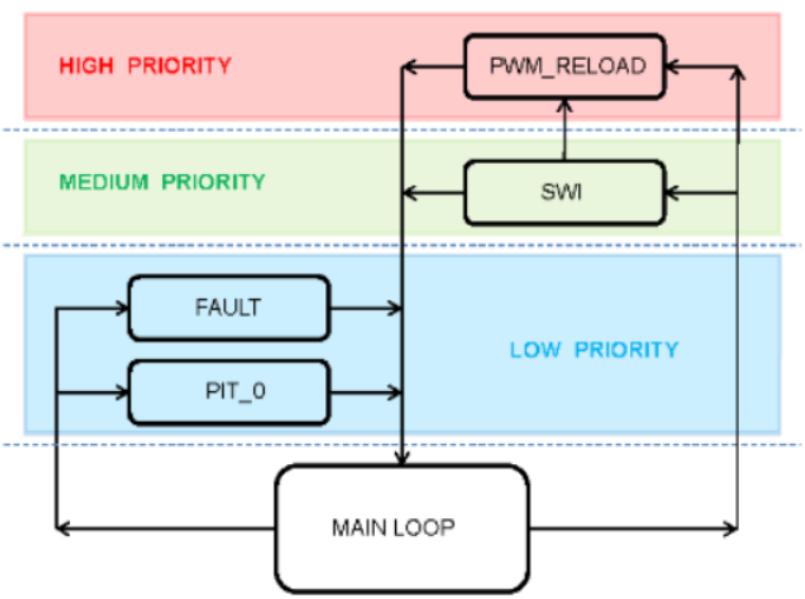


Figure 4-3. Interrupts structure

In the next task, this routine updates the new values into the PWM update registers. These new values are used at the start of the next PWM period.

The final task of this routine is to invoke the SWI interrupt. This interrupt is generated every 4 updates, which means every two PWM periods or once per 73 µsec.

4.4.2 SWI Interrupt

This interrupt is invoked by the PWM_Reload interrupt and has a medium priority. It can be interrupted by the PWM_Reload interrupt service routine, and comprises all the software routines that need to be computed for the proper PWM generation.

The first task is the sine waveform generation. This is done by the standard DSC library routine. The output is the variable with a fractional value in the range of –1 to +1.

In the next task, the value of this variable is multiplied by the DC-bus voltage value and the result is the AC sine output voltage. This value is used as the input to the PWM module for the output voltage generation. The whole computation is made in variables of the fractional type.

The next task in this routine is to take the measured values from the A to D converter and to calculate the floating average values of the input voltage, current from the solar panel, the average value of the DC-bus voltage, and the average values of the output voltage and current. The average input values are then used for the MPPT, the DC-bus value for the DC-bus regulator and the output values can be sent to the upper supervisory system by the RS-485 line or used for other computation in the application software.

The last task of this interrupt service routine is to maintain a correct switch-off process. This part of the code switches off the inverter when the immediate value of the output voltage crosses the zero level. Then, the outputs of the full-bridge inverter are in a high impedance state.

4.4.3 Fault interrupt

This interrupt has a lower priority. Where a fault event arises, the PWM outputs are immediately disabled by the DSC hardware. This interrupt service routine changes the status of the state variables and saves the fault information to the fault variable. The result of the fault event is that the inverter is switched off. You need to manually toggle the main switch to the switched off position, check the reason of the event condition, and manually switch on the inverter.

4.4.4 PIT_0 Timer Interrupt

This timer is used for the demo feature only. It is enabled by the fault interrupt service routine and generates a 1 sec time delay at the end. As the first task, the interrupt routine disables the PIT_0 timer and writes the value into a variable that represents the on/off switch. This action restarts the inverter. If the fault condition lasts, the inverter periodically tries to run and the red LED blinks. In other cases the inverter runs normal.

Chapter 5
Conclusion

5.1 Design

The entire inverter was built on one printed circuit board (see Figure 5-1).

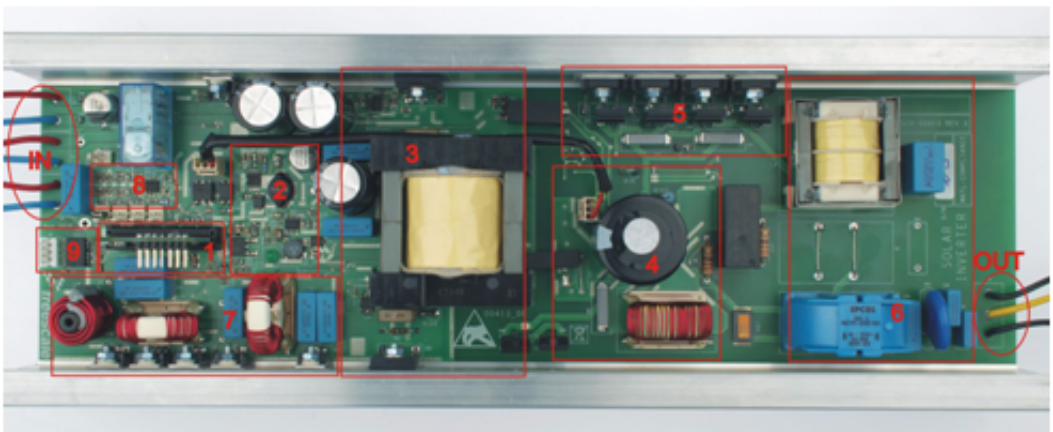


Figure 5-1. Inverter

This board is assembled on the top and bottom side. The top side covers the main power components, DSC control board, and several low power SMT circuits. The bottom side is assembled from only the SMT and covers circuits for the measurements and MOSFET drivers.

The assembled PCB is housed in a standard manufactured aluminium heatsink. The final demo is equipped with front and rear panels and covered on the top by clear plexiglass. The front panel covers the connectors for the solar panel inputs, the battery input, the signal LEDs, and the main on/off switch. The rear panel covers the standard output socket for the 230 V AC and the cooling fan. This fan runs independently, while the power transformer temperature reaches roughly at 55 °C.

5.1.1 Blocks summary

In Figure 5-1 the main blocks are highlighted by boxes with numbers. A detailed description is in the following.

5.1.1.1 Input and output

The input located on the left side of the board provides connections to the two solar panels and to one lead-acid back-up battery. On the right side of the inverter is the output connection, it provides the generated sine output voltage of 230 V AC for the load.

5.1.1.2 DSC controller board

This daughter card is in box number 1. It is assembled from an MC56F8023 digital signal controller and it controls the whole inverter. On the board there is a dedicated small power supply that can be used when the board is used outside any main board. When the DSC board is inserted into a main board, this power supply is not used.

5.1.1.3 Auxiliary power supplies

This block is in the box number 2. It is comprised of a 12 V DC power supply assembled from an LM5010A, a 3.3 V DC power supply assembled from a FAN8303, and a 5 V DC power supply for the analogue circuitry assembled from an LM317. This block provides the power for all the control and measurement circuits.

5.1.1.4 Power transformer

This transformer is in box number 3. There are two power MOSFETs in this box, placed on the heatsink, on the top and bottom sides of this box. These are push-pull MOSFETs on the primary side of the DC to DC converter. Beside the top side of box 2, and between box 2 and box 3, there are three big electrolytic capacitors together with two MP capacitors. They serve as the energy storage for the power DC/DC converter.

5.1.1.5 High voltage DC-bus

This part of the inverter is in box number 4. It is comprised of the bridge rectifier–in the bottom left edge of box 4 and in the bottom right edge of box 3—the associated inductor in the bottom side of box 4, and the main DC-Bus capacitor of 330 µF/450 V in the centre of box 4.

5.1.1.6 Full-bridge inverter

This part is in box 5. You can see in this box four power MOSFETs, four free-wheel diodes, and the associated capacitor for each half-bridge. The half-bridge drivers for this inverter are placed on the bottom side of the PCB in the box 5 area.

5.1.1.7 Output filter

The output filter is in box 6. In the upper half of this box is the main reconstruction filter–it filters the PWM switching frequency and puts through the generated 50 Hz frequency. In the bottom half of this box is the standard EMI filter.

5.1.1.8 Battery charger

This block is in box 7. You can see the L and C power components with power MOSFETs and diodes mounted on the heatsink.

5.1.1.9 Analogue measurement circuits

In box 8 are the analogue circuits–operational amplifier with associated components for the input voltage and current measurements. The other analogue circuits are placed on the bottom side of the PCB.

5.1.1.10 Communication interface

In box 9 is the isolated RS485 interface. This provides connection to the higher supervisor system.

5.2 Achieved parameters

This demo concentrates on showing the MPPT feature for the solar panel electricity conversion and the possibility of controlling the whole inverter through the MC56F8023 digital signal controller. For demo purposes, only the off-grid mode was used to show the main feature. A real solar panel with a nominal output power of 185 W was used for the MPPT test. The inverter runs on the maximum power point even if the illuminating conditions are widely changing. Standard bulbs were used as the load.

The next test was the efficiency, and the output voltage measurement. The inverter was powered by a standard DC power supply in the range of 24 V to 38 V. The output voltage was set to 230 V AC and various load bulbs were used. The results are shown in Figure 5-2 and Figure 5-3.

Figure 5-2. Efficiency vs. Vin

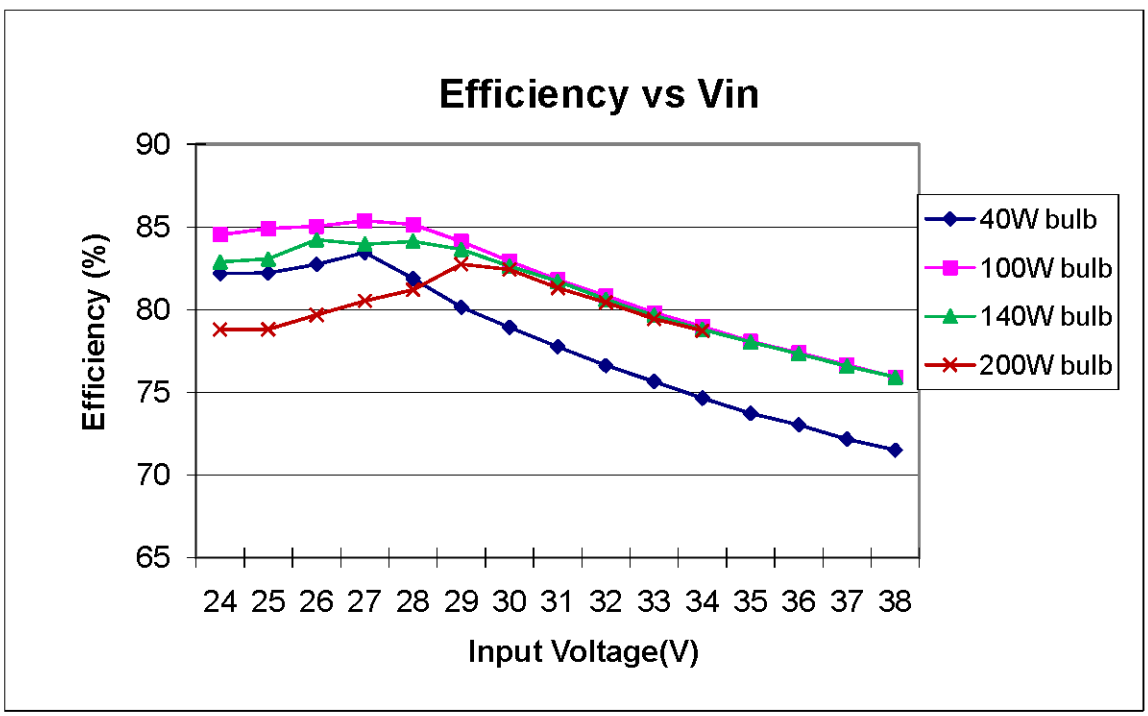
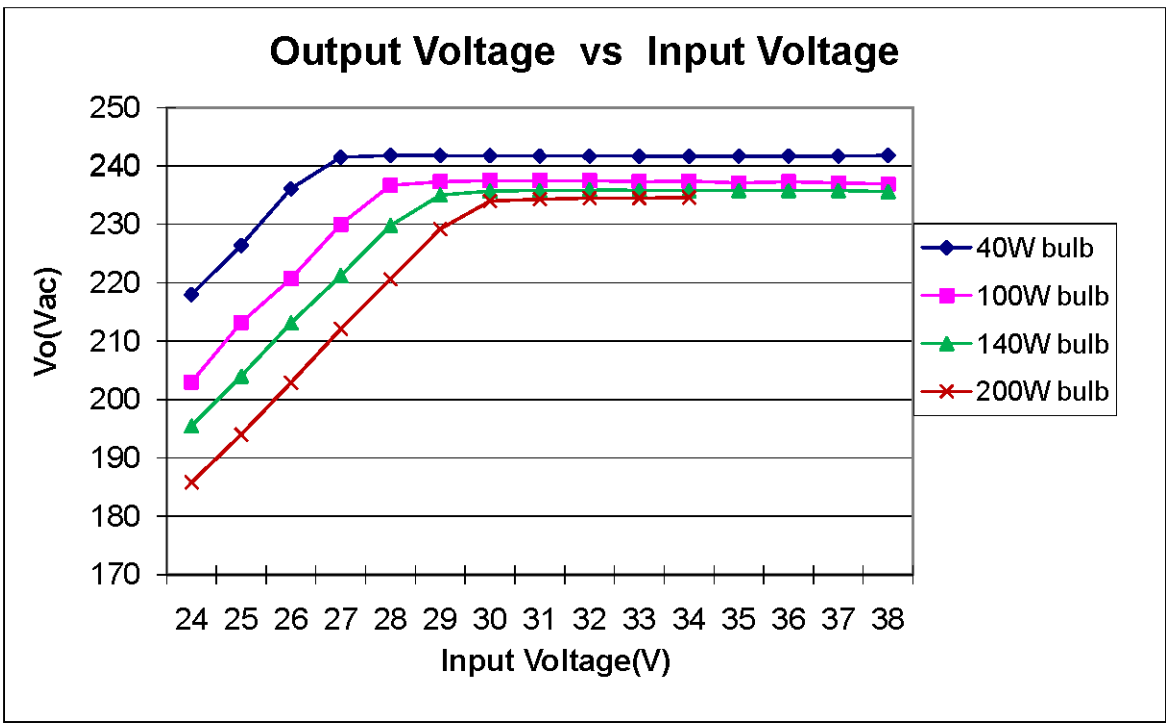


Figure 5-3. Output voltage vs input voltage



Many factors have an impact on the overall efficiency, such as the selected topology, the components mode of control, and others. The DSC is able to control various types of inverters.

5.3 Computing load on the DSC

The DSC in the control process has several tasks with differing priorities. It must measure analogue values of important voltages and currents, calculate desired control variables, and generate a clear sine output voltage. Along with these control tasks, it must be able to process the input commands from the front panel (on/off), provide the main status information via the LEDs on the front panel, and communicate the status and control information through the RS-485 line to the supervisor system. All these tasks can not significantly load the DSC.

Table 5-1. Execution time of periodic interrupts

NameExecution	Execution Period	Execution Time	DSC Load
A/D conversion time	18.3 µs	2.7 µs	2 %
PWM reload	18.3 µs	2.6 µs	14.2 %
Voltage regulator	73.25 µs	1.65 µs	2.2 %
Computation routines	73.25 µs	8.6 µs	11.7 %

Table continues on the next page...

Table 5-1. Execution time of periodic interrupts (continued)

NameExecution	Execution Period	Execution Time	DSC Load
Control routines	73.25 µs	14.0 µs	19.1 %

Memory Type	Size in Bytes	Available on MC56F8023	Memory Use
FLASH	3384	32 kB	10.3 %
RAM	662	4 kB	16.2 %
stack	256	—	—

5.3.1 Computing power usage

The main tasks of the control code (measure, compute, and control loops) take 49.2 % of the DSC's computing time. The next tasks (processes the switch status, communicates through the RS-485 and prepares important values for the supervisor system) take a further 1– 2% of the DSC's computing time. This means, the DSC is loaded up to 50%. Here, there is a sufficient time slot for the battery charger control routine. The routines are without any speed optimization. Optimized code can save on the following processing times.

5.3.2 Memory usage

The whole memory of this DSC is 32 kB of ROM 16 k of 16-bit words, and 4 kB of RAM with 2 k of 16-bit words. The code uses 1692 of words. This is 10.3 % of the whole capacity.

The internal RAM uses 331 words, which is 16.2 % of the whole capacity.

These numbers show the DSC used has sufficient free memory and computing power capacity to work reliably in this application.

5.4 Development environment used

CodeWarrior for the DSC version 8.2.3 was used to develop this application. The full source code of the example for this project is available on the internal web page. It provides all the settings of the internal peripherals used in this application and all the routines used for controlling this DC to AC inverter. It can also be used to build this application for other similar DSCs with higher computational power if needed.

5.5 Demo comments

The main aim of this demo is demonstrate the MPPT feature in the solar panel inverter application. The entire demo is designed as an isolated version of the inverter for an off-grid operation mode.

The nominal input voltage is 36 V DC. Therefore, one solar panel with an output voltage of 36 V, or two solar panels each of 18 V connected in series can be used as the power source for the inverter. For demonstration purposes, the nominal output power of the solar panels can vary from about 50 W up to 200 W per panel.

The generated output voltage of 230 V AC is a true sine shape with a maximal distortion, lower than 3%. It is possible to change the generated output voltage to 110 V AC, by changing the power transformer windings together with a change of several constants in the software.

There are very simple topologies used for the DC to DC converter and for the DC to AC inverter, thus the overall efficiency is not very high.

The whole inverter is controlled by an MC56F8023 DSC. This DSC is placed on the low voltage primary side. The control signals and the analogue signals for the measurement are transferred to the isolated secondary side by the digital isolator and by the analogue isolation amplifiers respectively. This topology shows the ability to control the whole inverter with a single DSC. The overall load of the DSC is about 50 % without the battery charger option implemented. The battery charger option takes on an added DSC load of about 10 to 12 %. It is possible to use two DSCs–one on the primary side and one on the secondary side. This option lowers the overall cost of the application by eliminating the digital isolator, isolation amplifiers, and the isolated auxiliary power supplies. It also lowers the load on each of the DSCs .

5.6 Demo purpose definition

This demo serves for demonstration purposes only. The main task is to demonstrate the MPPT feature. This is possible only if the solar panel is used as the power source. The solar panel must be placed in the exterior with good sun illumination.

The inverter can work with the standard DC power supply used as the power source, instead of the solar panel. The power supply has to meet the specification of the 30 V DC output voltage and a 4 A max output current. When the DC power supply is used, the MPPT feature does not function.

The entire hardware and software design is available on the Freescale web.

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