TLE92108 / TLE92104 – Step-by-step MOSFET driver setting guide and calculator description

About this document

Scope and purpose

This application note explains:

- the parameters and calculations needed to set the MOSFET driver of the TLE92108/104
- how to use the calculation tool for the settings of the gate drivers in PWM operation

It provides a step-by-step process to configure the MOSFET driver based on the MOSFET datasheet to control the MOSFET switching times in PWM operation:

- rise and fall times
- turn-on and turn-off delay times
- recommendations for the settings of the cross-current protection time and of the blank times

It also gives guidelines to use the “TLE92108/4 gate driver settings” tool

Intended audience

This document is intended for users who develop application with the Multi MOSFET Drivers (TLE9210x Family)

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1 Introduction

The TLE92108/04 are multiple MOSFET drivers, dedicated to control up to sixteen n-channel MOSFETs. They integrate eight half-bridge drivers for DC motor control applications such as automotive power seats, power lift gates, body controller, cargo cover, sunroof, door lock etc…

The current source gate drivers allows the control of the MOSFET switching times, which is the main point of interest in this document.

Figure 1 Block diagram – TLE92108-23x

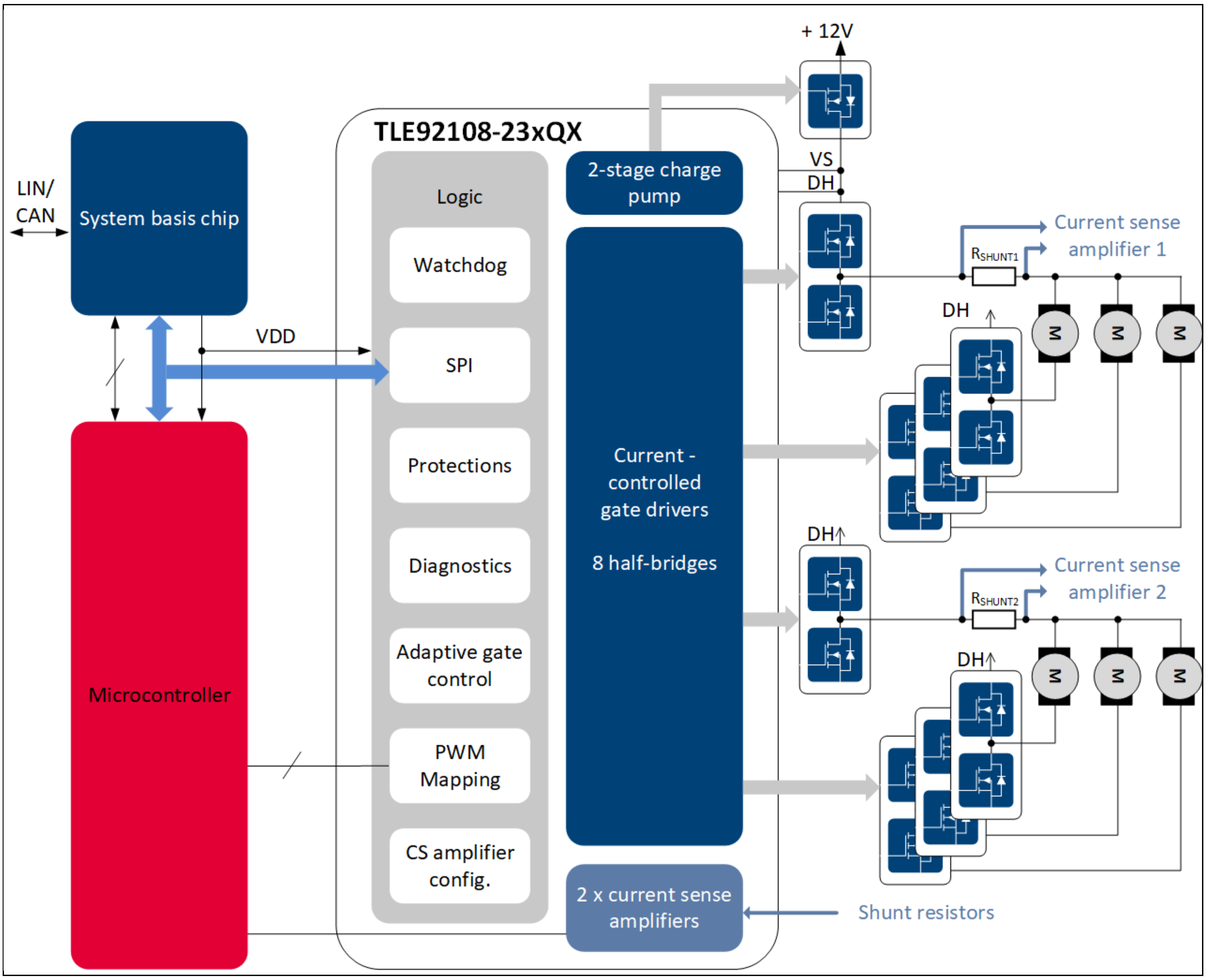
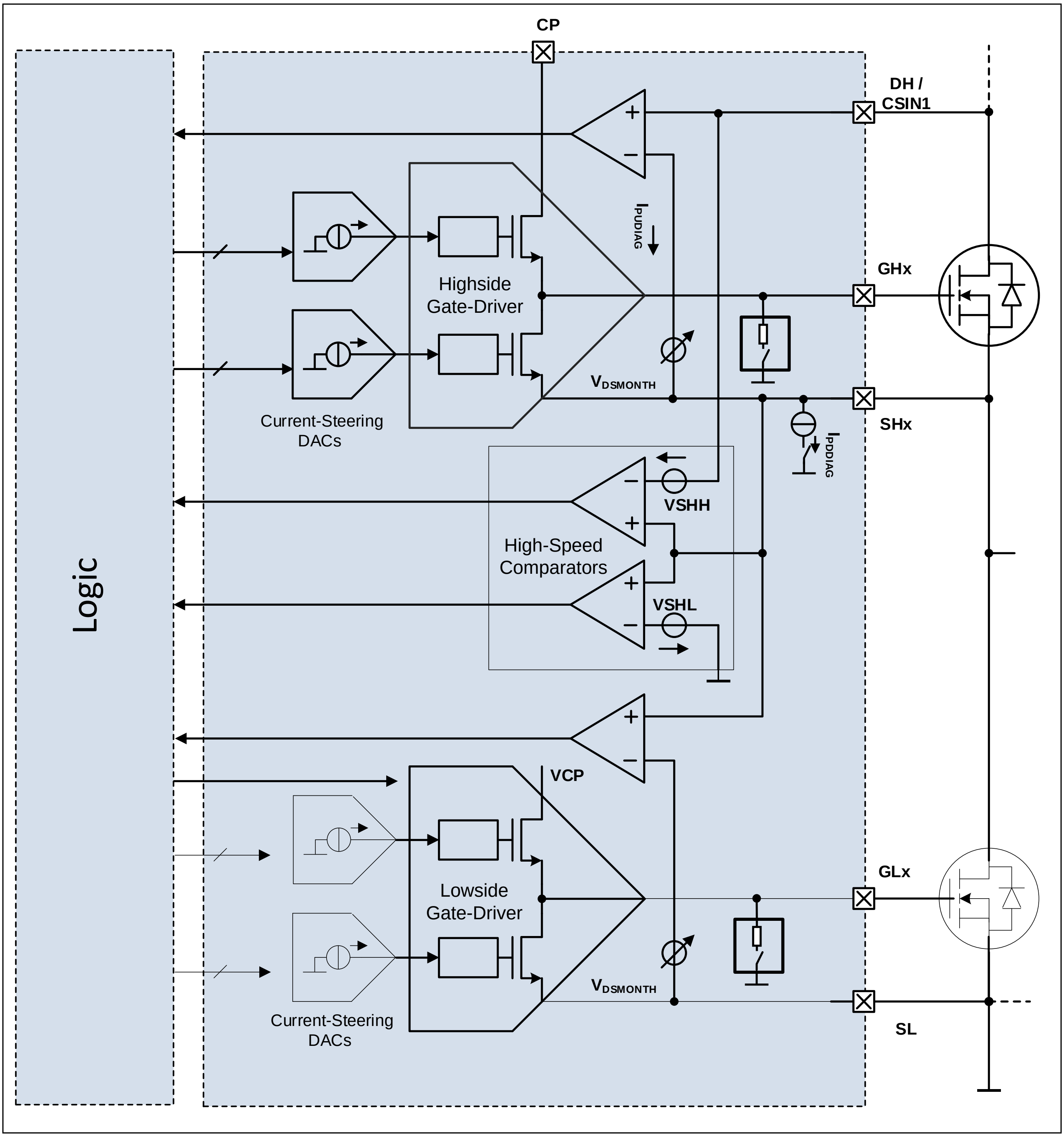


Figure 2 Block diagram of one half-bridge gate driver



2 General information

2.1 Conditions

The calculations and considerations of this document are valid for an inductive load controlled in half-bridge / full-bridge configuration with active freewheeling in PWM operation.

It is assumed that no external gate-drain / gate-source capacitance is placed at the MOSFET gate.

Note: Electrical parameters of the TLE9210x and of the MOSFETs are subject to variations such as production spread, supply voltage, temperature drift etc… The proposed calculation and settings are done with typical values for a specific MOSFET operating condition (e.g. supply voltage, load current etc…) and may differ from the tested devices under different test conditions.

2.2 Overview of the calculations steps

In this calculation tool, the user enters:

- MOSFET parameters extracted from the datasheet
- The application specific parameters and MOSFET driver's pre-charge and pre-discharge times

The calculation tool provides:

- The adapted MOSFET gate charges (Vds = Vs, Figure 5)
- The recommended settings of the MOSFET driver:
  - Gate driver currents
  - Cross-current protection times and blank times
  - Resulting switching times

Figure 3 MOSFET input parameters

Datasheet MOSFET parameters:	
Qgs_typ	7.7 nC
Qgd_typ	7.1 nC
Qg_typ	31.0 nC
Vdd_typ	32.0 V
Vgh_typ	10.0 V
Vplateau_typ	4.4 V
Vgs_th	2.8 V
Ciss_vs	1740.0 pF
Crss_vs	100.0 pF
Crss_typ	27.0 pF

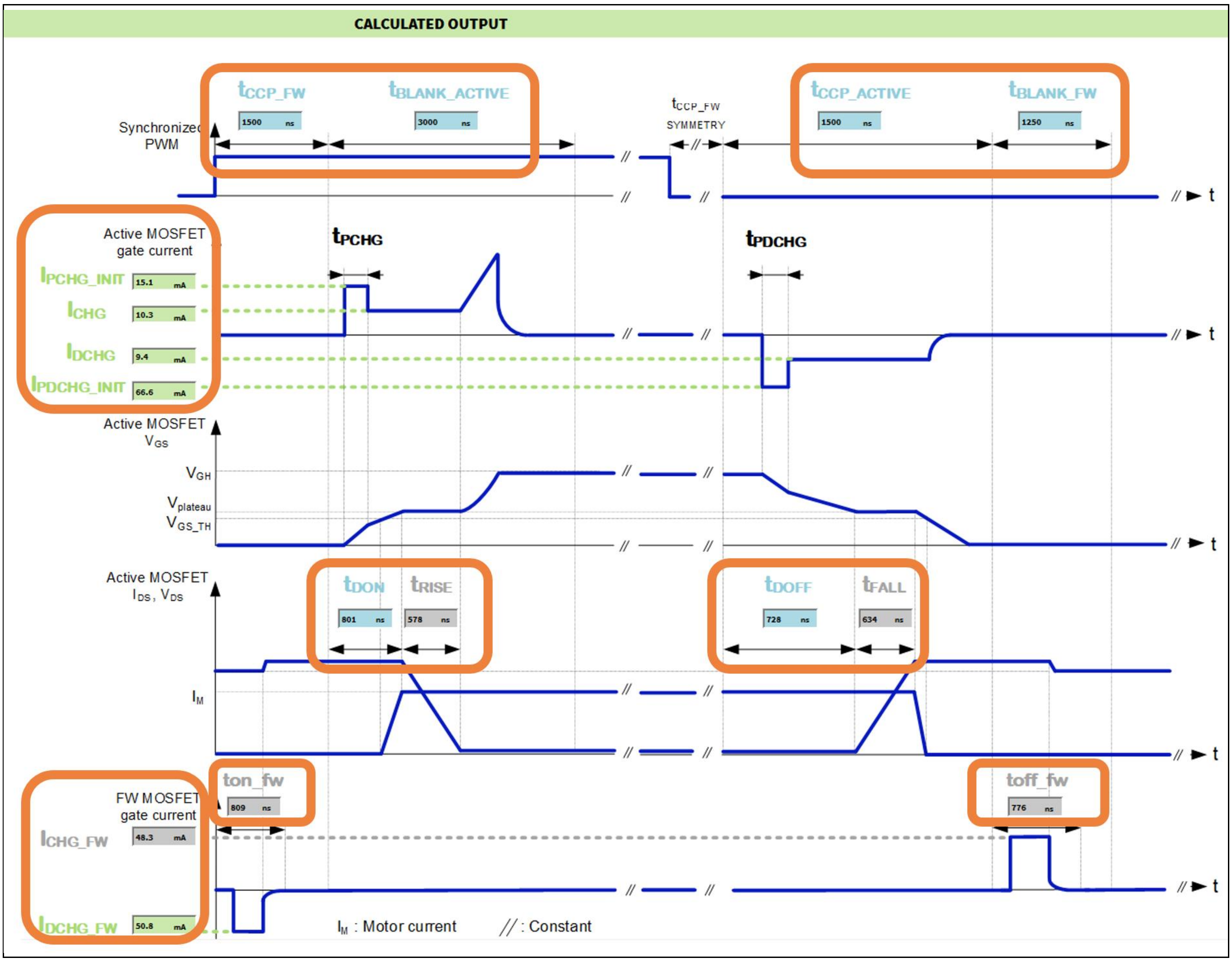
Figure 4 Application and MOSFET driver input parameters

Application conditions:	
Vs	14.0 V
Vgh	11.0 V
Vplateau	4.2 V
trise_target	600.0 ns
tfall_target	600.0 ns
toff_fw_target	800.0 ns
tdon_min_margin	300.0 ns
tdoff_min_margin	300.0 ns
t_margin	30.0 %
tpchg	125 ns
tpdchg	250 ns
Adaptive Gate Control	2

Figure 5 Outputs: MOSFET adapted gate charges (to Vds = Vs)

Calculated MOSFET parameters:		
Qgs	7.308	nC
Qgd	5.957	nC
Qg	33	nC
Ciss_0V	2893	pF

Figure 6 Outputs: recommended cross-current protection time, blank time, gate driver currents and resulting switching times



2.3 Notations

Table 1 List of notations

Abbreviation	Definition	Comment
Vds	MOSFET drain-source voltage	
Vgs	MOSFET gate-source voltage	
Ids	MOSFET drain-source current	
Vgh	MOSFET gate-source voltage when the gate is fully charged	TLE9210x parameter, Typ. 11 V
td_gdrv_on	TLE9210x gate driver turn-on delay time	150 ns
td_gdrv_off	TLE9210x gate driver turn-off delay time	150 ns
Ciss_0V	MOSFET input capacitance for drain-source voltage with Vds~ 0V and Vgs > Vplateau	Chapter 6.3

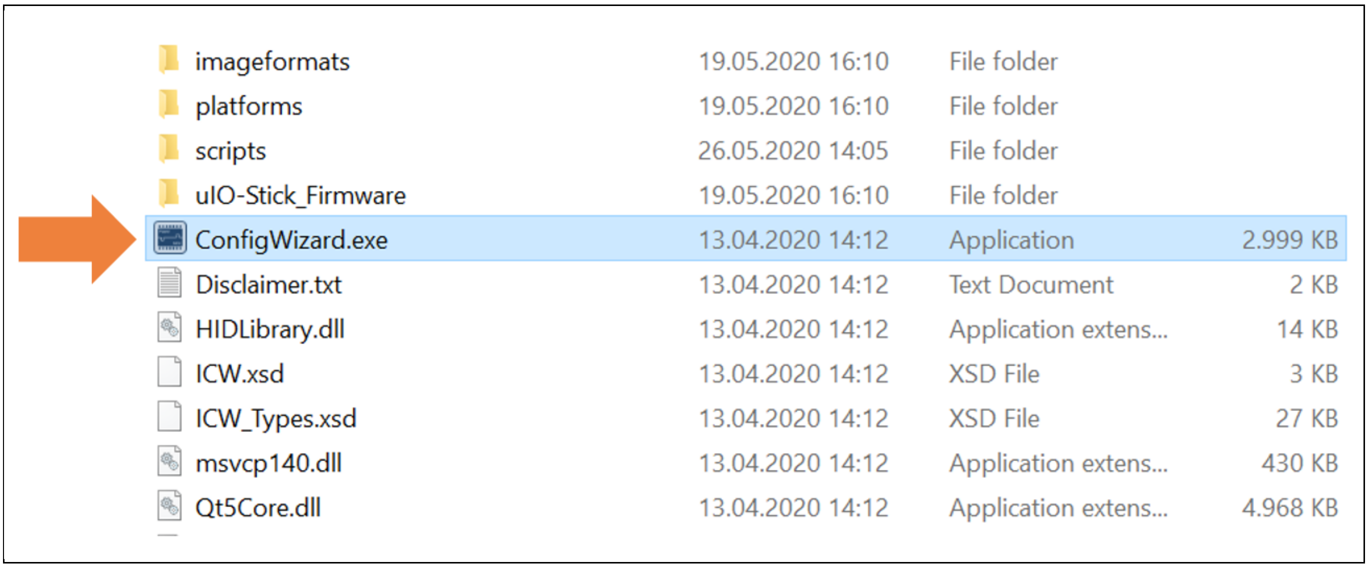
2.4 Software setup

The TLE9210x gate driver setting tool can be either downloaded from Infineons's MyICP upon access request or from the Infinon Tool Box.

Download from MyICP

The calculation tool can be downloaded upon request to Motorcontrolsolutions@infineon.com
Once the .zip file is locally extracted, start: **ConfigWizard.exe** (in the application subfolder)

Figure 7 Start of the TLE9210x gate driver setting tool after download from MyICP



Dowload from the Infineon Toolbox

The GUI is installed the Infineon Toolbox following the steps below:

1. Go to: www.infineon.com/toolbox
2. Follow the instructions provided on the toolbox installation webpage. Also see the "Download Getting Started Infineon Toolbox Guide" link for des additional user information
3. Launch the Infineon Toolbox on your PC:
4. Select **Manage Tools**
5. Search and install the tool: **Config Wizard for Multi MOSFET Driver** (Figure 8)
6. Start the **Config Wizard for Multi MOSFET Driver**
7. Click on **TLE9210x GATE DRIVER Settings** (Figure 9)

Figure 8 Install the Config Wizard for Multi MOSFET Driver

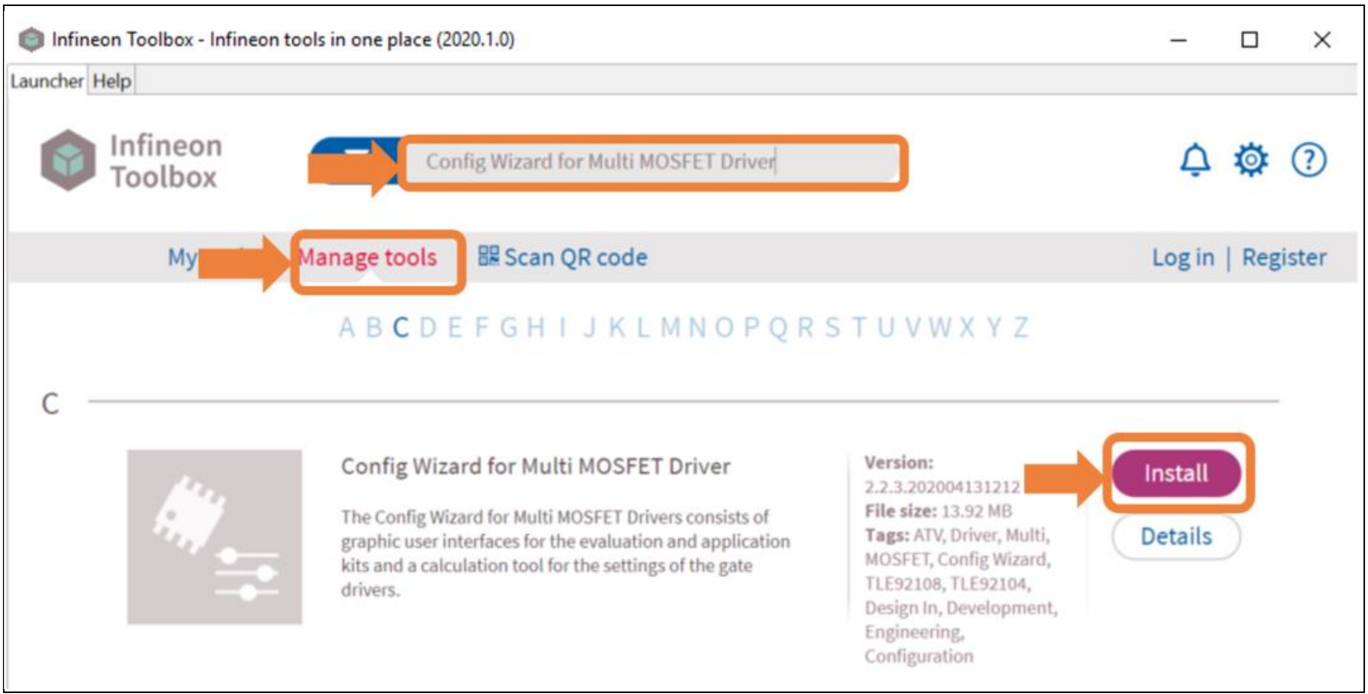
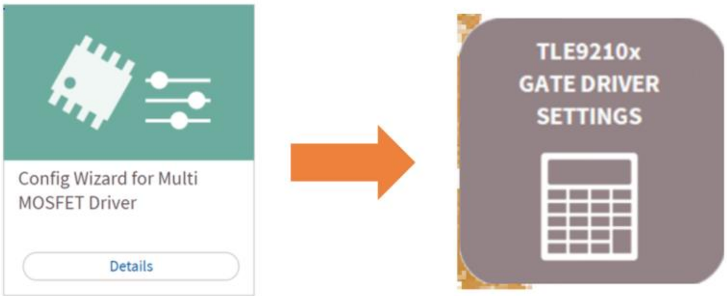


Figure 9 Starting the Gate Driver Setting tool



3 Input parameters

This chapter explains the meaning of the required input parameters.

3.1 MOSFET input parameters

This section describes the required MOSFET input parameters, and how to extract them from the MOSFET datasheet.

Table 2 List of MOSFET input parameters

Abbreviation	Definition	Unit	Comment
Qgs_typ	Typical MOSFET gate-source charge	nC	According to the datasheet conditions, Figure 11
Qgd_typ	Typical MOSFET gate-drain charge	nC	According to the datasheet conditions, Figure 11
Qg_typ	Typical MOSFET total gate charge	nC	According to the datasheet conditions (in general @Vgs = 10 V), Figure 11
Vdd_typ	Vds at which Qgd_typ is specified	V	e.g. For IPZ40N04S5-3R1: Vdd_typ = 32 V, Figure 11
Vgh_typ	Vgs at which Qg_typ is specified for full turn-on	V	e.g. For IPZ40N04S5-3R1: Vgh_typ = 10 V, Figure 11
Vplateau_typ	Vgs plateau at which Qgs_typ is specified	V	For IPZ40N04S5-3R1: Vplateau_typ=4.4 V @ Ids=40A, Figure 11
Vgs_th	Vgs threshold according to the typical application conditions (Ids, etc…)	V	According to the datasheet conditions, Figure 11
Ciss_vs	MOSFET input capacitance for drain-source voltage with Vds = Vs	pF	Figure 14, corresponding to the nominal application conditions (Vs = 14 V in this application note)
Crss_vs	MOSFET reverse transfer capacitance with Vds = Vs	pF	Figure 14
Crss_typ	MOSFET reverse transfer capacitance at Vds = Vdd_typ	pF	Figure 14

3.1.1 Gate charges Qgs_typ, Qgd_typ, Qg_typ

Qg_typ, Qgd_typ, Qg_typ are required parameters for the control of the switching times of the active MOSFET. Refer to Figure 10 for the definition.

In general the gate charges are specified for a very specific condition (32 V, 40A, Vgs from 0 to 10 V, Figure 11).

Figure 10 Gate charge definition and example (IPZ40N04S4-3R1, Infineon OptiMOS 5 MOSFET, [5])

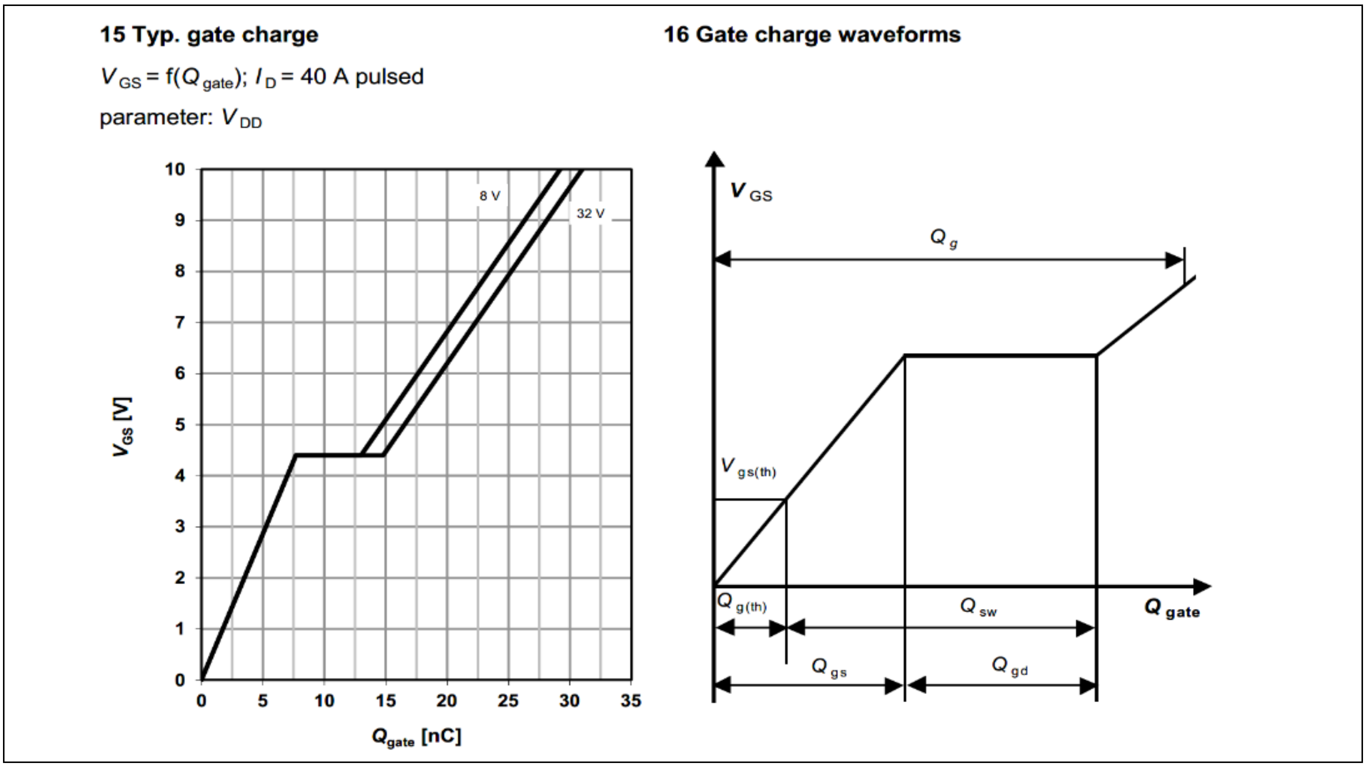


Figure 11 Example of gate charge specification (IPZ40N04S4-3R1) under specific conditions (32 V, 40A, Vgs from 0 to 10 V)

Gate Charge Characteristics[2)]						
Gate to source charge	Q_{gs}	V_{DD}=32V, I_D=40A, V_{GS}=0 to 10V	-	7.7	10.2	nC
Gate to drain charge	Q_{gd}		-	7.1	10.6	
Gate charge total	Q_g		-	31	41	
Gate plateau voltage	$V_{plateau}$		-	4.4	-	V

Note: the specified gate charges in Figure 11 correspond to Qgs_typ, Qgd_typ, and Qg_typ.

These parameters depend on the working point of the active MOSFET. Indeed, these gate charges vary (among others) with:

- the applied drain-source voltage
- the MOSFET Ids current
- the applied gate-source voltage, when the MOSFET is turned on (Vgh).

Note: Qg in the MOSFET datasheets is often given for Vgs = 0V to 10V. However, the typical Vgh of the TLE9210x is 11 V. Therefore, Qg is re-calculated by the tool (for Vgh instead of Vgs_typ, refer to chapter 6.3).

For a more accurate control of the switching times, the gate charges must be adapted to the specific application conditions. Refer to chapter 6.

3.1.2 Gate threshold voltage Vgs_th (or Vgs(th))

Vgs_th: typical MOSFET threshold voltage (Refer to Figure 10 and Figure 12).

Figure 12 IPZ40N04S4-3R1 gate threshold voltage

Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D= 1mA	40	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=30µA	2.2	2.8	3.4	

3.1.3 MOSFET input capacitances at Vds = Vs

Ciss_vs is the input capacitance under the following conditions: Vds = Vs and Vgs = 0 V

Ciss_vs is needed to set conditions on the gate driver configurations for the pre-charge phase (i.e. AGC = 2), in order to avoid a too fast current increase of Ids (i.e. high dI_{ds} / dt) during the turn-on of the MOSFET.

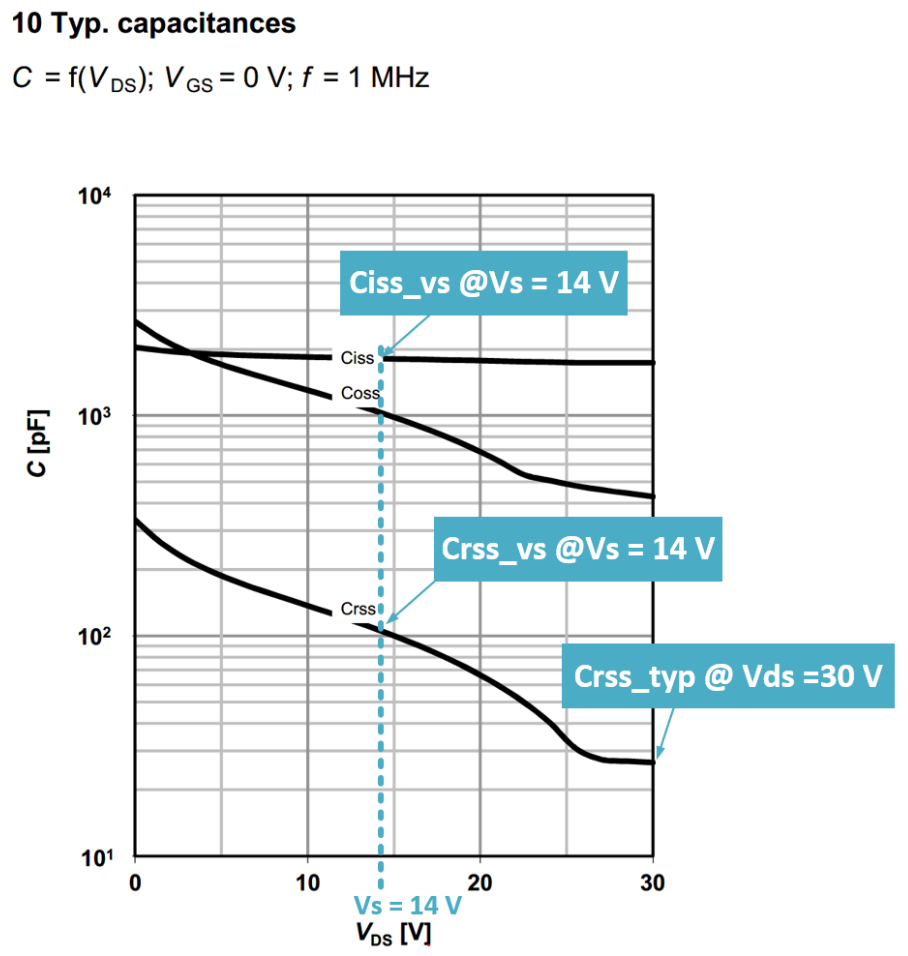
Figure 13 Specification of Ciss at Vgs = 0 V and Vds = 25 V (IPZ40N04S4-3R1)

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics[2)]						
Input capacitance	C_{iss}	V_{GS}=0V, V_{DS}=25V, f=1MHz	-	1740	2310	pF
Output capacitance	C_{oss}		-	490	650	
Reverse transfer capacitance	C_{rss}		-	35	55	

The IPZ40N04S5-3R1 shows no substantial variation for the Ciss between 14 V and 25 V (Figure 14). Therefore Ciss_vs can be considered to be equal to 1740 pF for this MOSFET.

Note: The MOSFET input capacitance depends on Vds (and Vgs). This parameter is in general specified under a specific condition, which may differ from the typical application conditions.

Figure 14 Determination of Ciss_vs, Crss_vs (IPZ40N04S5-3R1, Vs = 14V)



3.1.4 MOSFET reverse transfer capacitances at Vds = Vs and Vds = Vdd_typ

Crss_vs is the reverse transfer capacitance at Vds = Vs and Vgs = 0 V.

Crss_typ is the reverse transfer capacitance at Vds = Vdd_typ and Vgs = 0 V.

Crss_vs and Crss_typ are required to estimate Qgd at Vds = Vs, using Qgd_typ (at Vds = Vdd_typ).

The value of these capacitances can be read from Figure 14 for the IPZ40N04S5-3R1. Crss @Vds = 30 V is a good estimation of Crss_typ (at Vds = Vdd_typ = 32 V), because the Crss curve is flat in this range for this MOSFET.

3.2 Application related input parameters

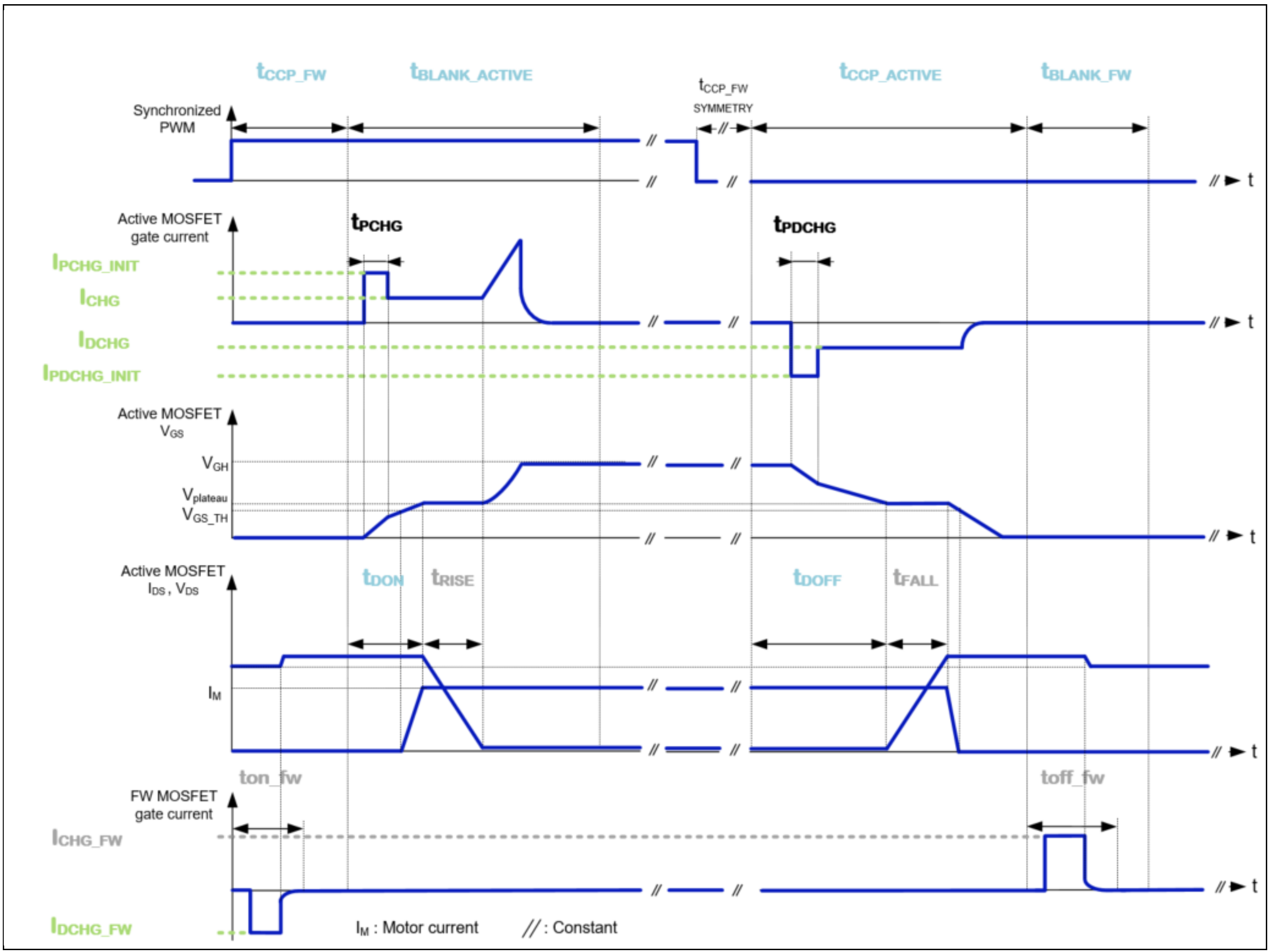
This section describes the application related input parameters, which are listed in Table 3.

Table 3 List of inputs parameters in the application conditions

Abbreviation	Definition	Unit	Comment
Vs	Nominal application supply voltage	V	Vs = 14 V in this document
Vgh	MOSFET driver gate-source voltage when the gate is fully charged [1)]	V	11 V typ. for the TLE9210x
Vplateau	Vgs plateau in the application conditions	V	Refer to Figure 16
trise_target	Active MOSFET target rise time	ns	
tfall_target	Active MOSFET target fall time	ns	
toff_fw_target	FW MOSFET target turn-off time	ns	
tdon_min_margin	Additional delay between the end of the pre-charge phase and the moment when Vgs reaches Vgs_th	ns	300 ns in the examples
tdoff_min_margin	Additional delay between the end of the pre-discharge phase and the moment when Vds decreases (Vgs reaches Vplateau)	ns	300 ns in the examples
t_margin	Margin in % added to the min. required cross-current protection time and blank time	%	30 % in the examples
tpchg	Gate driver pre-charge time	ns	Register TPRECHG (01000_B)
tpdchg	Gate driver pre-discharge time	ns	Register TPRECHG (01000_B)
AGC	Adaptive gate control bit		Register GENTCTRL1 (00000_B)

Figure 15 shows the switching times, the cross-current protection time and blank time of the active and FW MOSFETs during PWM operation (the control scheme of the active MOSFET represented on Figure 15 corresponds to AGC = 2).

Figure 15 Switching times and timings definition



trise_target: is the target rise time of the active MOSFET. This parameter is defined as the duration of the Vds slope at the turn-on of the active MOSFET (Refer to Figure 15).

tfall_target: is the target fall time of the active MOSFET. This parameter is defined as the duration of the Vds slope at the turn-off of the active MOSFET (Refer to Figure 15).

toff_fw_target is the target switch-off time of the FW MOSFET.

tccp_active is the cross-current protection time of the active MOSFET. The gate driver must be configured so that active MOSFET is off before the end of the tCCP_ACTIVE

tccp_fw is the cross-current protection time of the FW MOSFET. The gate driver must be configured so that the FW MOSFET is off before the end of the tCCP_FW.

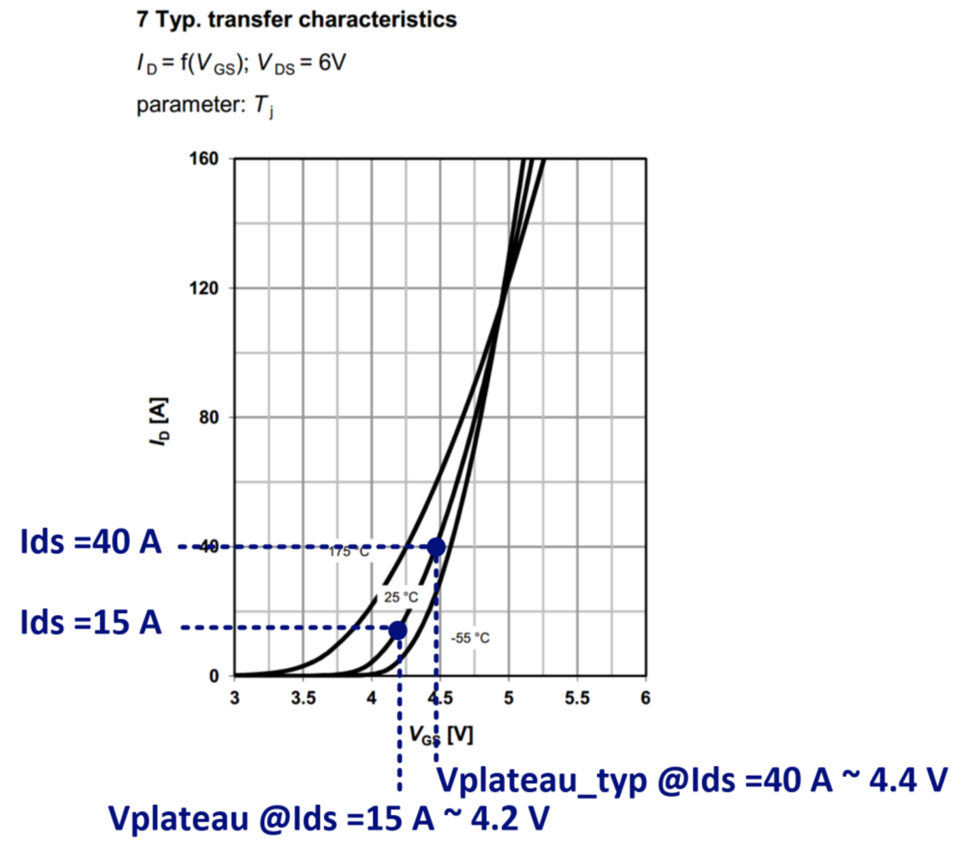
t_margin: is the margin (in percent) added to the minimum required cross-current protection times and the blank times for the active MOSFET and for the FW MOSFET.

tdon_min_margin is relevant for AGC = 2 (refer to datasheet for information about the AGC bit).

It is a minimum delay between the end of the pre-charge phase and the moment when Vgs reaches Vgs_th. Refer to chapter 4.

tdoff_min_margin: is relevant for AGC = 1 or 2. It is the minimum delay between the end of the pre-discharge phase and the beginning of tfall. Refer to chapter Refer to chapter 4.

Figure 16 Determination of Vplateau in the application conditions – IPZ40N04S5-3R1, Ids = 15 V



3.3 Output parameters

The calculation tool provides the recommended charge and discharge currents for the active and FW MOSFETs and the expected switching times. The user will also find the recommendations for the blank time and cross-current protection times.

The MOSFET gate charges Qg, Qgs and Qgd are adapted by the calculation tool according to the description in chapter 6.

Note that the maximum allowed pre-discharge current (for AGC = 1) and the max allowed pre-charge currents (for AGC = 1 or 2) is supposed to be set to 100 mA typ.

Table 4 List of output parameters

Abbreviation	Definition	Unit	Control register
ICHG	Active MOSFET charge current	mA	PWM_ICHG_ACT
IDCHG	Active MOSFET discharge current	mA	PWM_IDCHG_ACT
ICHG_FW	FW MOSFET charge current	mA	PWM_ICHG_ACT
IDCHG_FW	FW MOSFET discharge current	mA	PWM_ICHG_ACT
IPCHG_INIT	Active MOSFET initial pre-charge current	mA	PWM_PCHG_INIT
IPDCHG_INIT	Active MOSFET initial pre-discharge current	mA	PWM_PDCHG_INIT
tdon	Active MOSFET turn-on delay time	ns	
tdoff	Active MOSFET turn-off delay time	ns	
trise	Active MOSFET effective rise time	ns	
tfall	Active MOSFET achievable fall time	ns	
ton_fw	FW MOSFET turn-on time	ns	
toff_fw	FW MOSFET turn-off time	ns	
tblank_active	Active MOSFET selected blank time	ns	CCP_BLK1, CCP_BLK2_ACT and PWM_ICHGMAX_CCP_BLK3_ACT
tccp_active	Active MOSFET current-cross protection time	ns	
tblank_fw	FW MOSFET blank time	ns	CCP_BLK1, CCP_BLK2_FW and PWM_ICHGMAX_CCP_BLK3_FW
tccp_fw	FW MOSFET current-cross protection time	ns	

Notes:

1. trise, tfall, ton_fw, toff_fw may differ from trise_target, tfall_target, ton_fw_target and toff_fw_target. This difference is due to the fact that the calculation of trise, tfall, ton_fw, toff_fw considers the nearest available gate driver's charge and discharge currents (refer to Table 11)
2. tdon, tdoff, ton_fw and toff_fw include the gate driver delay times td_gdrv_on and td_gdrv_off
3. tblank_active is selected so that its **minimum** value fulfills [0.12], [1.12], [2.12]. The calculation tool displays the corresponding **typical** value.f
4. tccp_active is selected so that its **minimum** value fulfills [0.13], [1.13], [2.13]. The calculation tool displays the corresponding **typical** value.

5. tccp_fw is selected so that its **minimum** value fulfills [0.14], [1.14], [2.14]. The calculation tool displays the corresponding **typical** value.
6. tblank_fw is selected so that its **minimum** value fulfills [0.15], [1.15], [2.15]. The calculation tool displays the corresponding **typical** value.

4 Recommendations

4.1 Conditions on trise_target and tfall_target

trise_target and tfall_target are input parameters determined by the application requirements.These parameters are determined by the **trade-off between the electromagnetic emissions (EME) and the switching losses**, and must be defined for each application according to their specific requirements.

4.2 Conditions on the pre-charge phase (AGC = 2)

If the pre-charge phase is activated, **the pre-charge phase should be over before the Ids increases in the active MOSFET (i.e. before Vgs = Vgs_th).** If this condition is not fulfilled, then the possible high pre-charge current causes a fast increase of Ids, resulting in a high EME.

This criteria is taken into account in 5.3.1 Step 3 and gives a condition on IPCHG_INIT.

tdon_min_margin (e.g. 300 ns) further reduces the maximum allowed pre-charge current, in order to avoid a fast increase of Ids.

Note: tdon_min_margin is an additional delay, which is directly reflected on the turn-on delay time, explaining the name of the parameter.

4.3 Recommendation for tpchg (AGC = 2)

tpchg must fulfill two conditions:

1. It should be as short as possible in order to avoid an unnecessary increase of tdon
2. It should be long enough, so that the charges delivered during the pre-charge phase (tpchg x IPCHG) and during the charge phase allow to reach the target tdon.

For the common MOSFETs used in combination with the TLE9210x, **tpchg = 125 ns is often a good starting point**.

4.4 Conditions on the pre-discharge phase (AGC = 1 or 2)

When the pre-discharge phase is activated (AGC = 1 or 2), **the pre-discharge phase should over before the decrease of Vds.** If this condition is not fulfilled, then the possible high pre-discharge current causes a fast decrease of Vds, resulting in a high EME.

This criteria is taken into account in 5.2.1 Step 4 (AGC = 1) and 5.3.1 Step 4 (AGC = 2) and gives a condition on IPDCHG_INIT.

tdoff_min_margin (e.g. 300 ns) further reduces the maximum allowed pre-discharge current, in order to avoid that the pre-discharge phase is still active during the increase of Vds.

4.5 Recommendation for tpdchg (AGC = 1 or 2)

tpdchg must fulfill two conditions:

1. It should be as short as possible in order to avoid an unnecessary increase of tdoff
2. It should be long enough, so that the charges removed from the MOSFET's gate during the pre-discharge phase (tpdchg x IPDCHG) and during the discharge phase allow to reach the target tdoff.

For the common MOSFETs used in combination with the TLE92108 such as the IPZ40N04S5-3R1, tpdchg = 250 ns is usually suitable.

4.6 Recommendations for toff_fw_target

The turn-off (and the turn-on) of the FW MOSFET has a much lower impact on the EME than for the active MOSFET. Therefore it is possible to turn-off the FW MOSFET faster than the active MOSFET: e.g. between 600 ns and 1 µs as a starting point. toff_fw_target determines the suitable FW discharge current.

Note: IDCHG_FW is determined by toff_fw_target and by the MOSFET characteristics. The setting FW MOSFET's charge and discharge currents are set by common control bits, therefore the turn-on time of the FW MOSFET is also determined.

5 Calculation of the gate driver currents and timings

This chapter shows the calculations that apply for for AGC = 0, AGC =1 and AGC = 2.

5.1 Calculation with Adaptive Gate Control disabled (AGC = 0)

This section shows the formulas used to calculate the required gate driver settings based on the input parameters when AGC = 0.

In this mode, the pre-charge and pre-discharge phases are disabled. The gate of the active MOSFET is charged, repectively discharged with the constant currents ICHG and IDCHG.

5.1.1 Calculation of gate driver currents with AGC = 0

This section calculates the required ICHG, IDCHG, IDCHG_FW.

Table 5 Calculation of gate driver currents with AGC = 0

Step	Parameters [mA]	Formula	Look-up	
1	**Active MOSFET Charge current**	$ICHG = \frac{Qgd}{trise\_target}$	Table 11 2)	[0.1]
2	**Active MOSFET Discharge current**	$IDCHG = \frac{Qgd}{tfall\_target}$	Table 11 2)	[0.2]
3	**Active MOSFET initial pre-charge current** 1)	$IPCHG\_INIT = ICHG$		[0.3]
4	**Active MOSFET initial pre-discharge current** 1)	$IPDCHG\_INIT = IDCHG$		[0.4]
5	**FW MOSFET discharge current**3)	$IDCHG\_FW = \frac{Ciss\_0v \text{ x } Vgh}{toff\_fw\_target - td\_gdrv\_off}$	Table 11 2)	[0.5]

1) These parameters are not relevant if AGC = 0: Therefore the IPCHG_INIT and IPDCHG_INIT must not be programmed when AGC = 0.

2) Once the required current is calculated, the nearest available MOSFET driver current of the TLE9210x is selected by the calculation tool. Refer to the datasheet rev. 1.0, Table 13 and Table 14, [1] and [2].

3) The FW MOSFET charge current is automatically determined when the FW MOSFET discharge current is selected (the FW MOSFET charge and discharge currents are set by the same control bits, [1] and [2]).

5.1.2 Timing calculation with AGC = 0

This section calculates the effective trise, tfall, tdon, tdoff, ton_fw, toff_fw, tblank_active, tccp_active, tccp_fw, and tblank_fw.

Attention: ***The nearest available ICHG, IDCHG, ICHG_FW and IDCHG_FW must be used in this calculation step, according to Table 11***

Table 6 Timing calculation with AGC = 0

Step	Parameters	Formula	Look-up	
6	**Effective rise time**	$\text{trise} = \frac{\text{Qgd}}{\text{ICHG}}$		[0.6]
7	**Effective fall time**	$\text{tfall} = \frac{\text{Qgd}}{\text{IDCHG}}$		[0.7]
8	**Turn-on delay time**	$\text{tdon} = \frac{\text{Qgs}}{\text{ICHG}} + \text{td\_gdrv\_on}$		[0.8]
9	**Turn-off delay time**	$\text{tdoff} = \frac{\text{Qg}-\text{Qgs}-\text{Qgd}}{\text{IDCHG}} + \text{td\_gdrv\_off}$		[0.9]
10	**FW turn-on time**	$\text{ton\_fw} = \frac{\text{Ciss\_0v x Vgh}}{\text{ICHG\_FW}} + \text{td\_gdrv\_on}$		[0.10]
11	**FW turn-off time**	$\text{toff\_fw} = \frac{\text{Ciss\_0v x Vgh}}{\text{IDCHG\_FW}} + \text{td\_gdrv\_off}$		[0.11]
12	**Active MOSFET blank time[1)]**	$\text{tblank\_active} = (\text{tdon} + \text{trise}) \text{ x } (1 + \text{t\_margin})$	Table 12	[0.12]
13	**Active MOSFET CCP[2)] time**	$\text{tccp\_active} = (\text{tdoff} + \text{tfall} + \frac{\text{Qgs}}{\text{IDCHG}}) \text{ x } (1 + \text{t\_margin})$	Table 12	[0.13]
14	**FW CCP[2)] time**	$\text{tccp\_fw} = \text{toff\_fw x } (1 + \text{t\_margin})$	Table 12	[0.14]
15	**FW blank time**	$\text{tblank\_fw} = \text{ton\_fw x } (1 + \text{t\_margin})$	Table 12	[0.15]

1) CCP : Cross current protection

12 If the MOSFET must have the full Rdson at the end of tblank_active (i.e. Vgs = Vgh = 11V) and the postcharge phase is disabled, then [0.12] must be changed to:

$$\text{tblank\_active} = (\text{tdon} + \text{trise} + \frac{\text{Qg}-\text{Qgs}-\text{Qgd}}{\text{ICHG}}) \text{ x } (1 + \text{t\_margin}).$$

5.2 Calculation of gate driver currents with AGC = 1

This section shows the formulas used to calculate the required gate driver settings based on the input parameters when AGC = 1.

In this mode:

- the pre-charge is disabled
- the pre-discharge phase is enabled. The MOSFET is discharged with the current IPDCHG_INIT during this phase
- tdon and tdoff are not regulated by the TLE9210x

5.2.1 Calculation of gate driver currents with AGC = 1

This section calculates the effective trise, tfall, tdon, tdoff, ton_fw, toff_fw, tblank_active, tccp_active, tccp_fw, and tblank_fw.

Table 7 Calculation of gate driver currents with AGC = 1

Step	Parameters [mA]	Formula	Look-up	
1	**Active MOSFET charge current**	$\text{ICHG} = \frac{\text{Qgd}}{\text{trise\_target}}$	Table 11 2)	[1.1]
2	**Active MOSFET discharge current**	$\text{IDCHG} = \frac{\text{Qgd}}{\text{tfall\_target}}$	Table 11 2)	[1.2]
3	**Active MOSFET initial pre-charge current 1)**	$\text{IPCHG\_INIT} = \text{ICHG}$		[1.3]
4	**Active MOSFET initial pre-discharge current**	$\text{IPDCHG\_INIT} = \frac{\text{Qg}-\text{Qgs}-\text{Qgd}-(\text{tdoff\_min}-\text{td\_gdrv\_off}-\text{tpdchg})\ \text{x}\ \text{IDCHG}}{\text{tpdchg}}$	Table 11 2)	[1.4]
5	**FW MOSFET discharge current 3)**	$\text{IDCHG\_FW} = \frac{\text{Ciss\_0v x Vgh}}{\text{toff\_fw\_target} - \text{td\_gdrv\_off}}$	Table 11 2)	[1.5]

1) This parameters are not relevant if AGC = 1: Therefore the IPCHG_INIT must not be programmed if AGC = 1.

2) The nearest available current must be selected accordin to Table 11. Refer to the datasheet rev. 1.0, Table 13 and Table 14, [1] and [2].

3) The FW MOSFET charge current is automatically determined when the FW MOSFET discharge current is selected (the FW MOSFET charge and discharge currents are set by the same control bits, [1] and [2]).

4 Condition on IPDCHG_max to ensure that the pre-discharge phase is over before Vgs reaches Vplateau at the turn-off of the active MOSFET:

$$\text{IPDCHG\_INIT} \leq \text{IPDCHG\_max} = \frac{\text{Qg} - \text{Qgs} - \text{Qgd}}{\text{tpchg}}$$

$$\text{tdoff\_min} = \frac{\text{Qg} - \text{Qgs} - \text{Qgd} - \text{tpdchg x } \textbf{IPDCHG\_max}}{\text{IDCHG}} + \text{td\_gdrv\_off} + \text{tpdchg} + \text{tdoff\_min\_margin}$$

5.2.2 Timing calculation AGC = 1

Attention: *The nearest available ICHG, IDCHG, ICHG_FW and IDCHG_FW must be used in this calculation step, according to Table 11*

Table 8 Timing calculation with AGC = 1

Step	Parameters [ns]	Formula	Look-up	
6	**Effective rise time**	$\mathrm{trise} = \frac{\mathrm{Qgd}}{\mathrm{ICHG}}$	Table 11	[1.6]
7	**Effective fall time**	$\mathrm{tfall} = \frac{\mathrm{Qgd}}{\mathrm{IDCHG}}$	Table 11	[1.7]
8	**Turn-on delay time**	$\mathrm{tdon} = \frac{\mathrm{Qgs}}{\mathrm{ICHG}} + \mathrm{td\_gdrv\_on}$		[1.8]
9	**Turn-off delay time**	$\mathrm{tdoff} = \frac{\mathrm{Qg - Qgs - Qgd - tpdchg\ x\ IPDCHG\_INIT}}{\mathrm{IDCHG}} + \mathrm{td\_gdrv\_off} + \mathrm{tpdchg}$		[1.9]
10	**FW turn-on time**	$\mathrm{ton\_fw} = \frac{\mathrm{Ciss\_0v\ x\ Vgh}}{\mathrm{ICHG\_FW}} + \mathrm{td\_gdrv\_on}$		[1.10]
11	**FW turn-off time**	$\mathrm{toff\_fw} = \frac{\mathrm{Ciss\_0v\ x\ Vgh}}{\mathrm{IDCHG\_FW}} + \mathrm{td\_gdrv\_off}$		[1.11]
12	**Active MOSFET blank time**	$\mathrm{tblank\_active} = (\mathrm{tdon} + \mathrm{trise})\ \mathrm{x}\ (1 + \mathrm{t\_margin})$	Table 12	[1.12]
13	**Active MOSFET CCP time**	$\mathrm{tccp\_active} = (\mathrm{tdoff} + \mathrm{tfall})\ \mathrm{x}\ (1 + \mathrm{t\_margin})$	Table 12	[1.13]
14	**FW CCP time**	tccp_fw = toff_fw x (1 + t_margin)	Table 12	[1.14]
15	**FW blank time**	tblank_fw = ton_fw x (1 + t_margin)	Table 12	[1.15]

12 If the MOSFET must have the full Rdson at the end of tblank_active (i.e. Vgs = Vgh = 11V), then [1.12] must be changed to $\mathrm{tblank\_active} = (\mathrm{tdon} + \mathrm{trise} + \frac{\mathrm{Qg - Qgs - Qgd}}{\mathrm{ICHG}})\ \mathrm{x}\ (1 + \mathrm{t\_margin})$

5.3 Calculation with Adaptive Gate Control enabled (AGC = 2)

This section shows the formulas used to calculate the required gate driver settings based on the input parameters when AGC = 2.

In this mode:

- tdon and tdoff are regulated by the TLE9210x
- the pre-charge is enabled. The MOSFET is initially charged with the current IPCHG_INIT during this phase
- the pre-discharge phase is enabled. The MOSFET is initially discharged with the current IPDCHG_INIT during this phase

5.3.1 Calculation of gate driver currents with AGC = 2

Table 9 Calculation of gate driver currents with AGC = 2

Step	Parameters [mA]	Formula	Look-up	
1	**Active MOSFET charge current**	$\text{ICHG} = \frac{\text{Qgd}}{\text{trise\_target}}$	Table 11 [1)]	[2.1]
2	**Active MOSFET discharge current**	$\text{IDCHG} = \frac{\text{Qgd}}{\text{tfall\_target}}$	Table 11 [1)]	[2.2]
3	**Active MOSFET initial pre-charge current**	$\text{IPCHG\_INIT} = \frac{\text{Qg} - (\text{tdon\_min} - \text{td\_gdrv\_on} - \text{tpchg})\text{ x ICHG}}{\text{tpchg}}$	Table 11 [1)]	[2.3]
4	**Active MOSFET initial pre-discharge current**	$\text{IPDCHG\_INIT} = \frac{\text{Qg} - \text{Qgs} - \text{Qgd} - (\text{tdoff\_min} - \text{td\_gdrv\_off} - \text{tpdchg})\text{ x IDCHG}}{\text{tpdchg}}$	Table 11 [1)]	[2.4]
5	**FW discharge current** [2)]	$\text{IDCHG\_FW} = \frac{\text{Ciss\_0V x Vgh}}{\text{toff\_fw\_target} - \text{td\_gdrv\_off}}$	Table 11 [1)]	[2.5]

1) The nearest available current must be selected according to Table 11. Refer to the datasheet rev. 1.0, Table 13 and Table 14, [1] and [2].

2) The FW MOSFET charge current is automatically determined when the FW MOSFET discharge current is selected (the FW MOSFET charge and discharge currents are set by the same control bits, [1] and [2]).

3 Condition on IPCHG_max to ensure that the pre-charge phase is over before Vgs = Vgs_th:

$$IPCHG\_INIT \leq IPCHG\_max = \frac{Vgs\_th \times Ciss\_vs}{tpchg}$$

The minimum allowed tdon (noted tdon_min), considering a margin (tdon_min_margin) is given by:

$$tdon\_min = \frac{Qg - tpchg \times IPCHG\_max}{ICHG} + td\_gdrv\_on + tpchg + tdon\_min\_margin$$

4 Condition on IPDCHG_max to ensure that the pre-discharge phase is over before Vgs reaches Vplateau at the turn-off of the active MOSFET:

$$IPDCHG\_INIT \leq IPDCHG\_max = \frac{Qg - Qgs - Qgd}{tpdchg}$$

The minimum allowed tdoff (noted tdoff_min), considering a margin (tdoff_min_margin) is given by:

$$tdoff\_min = \frac{Qg - Qgs - Qgd - tpdchg \times IPDCHG\_max}{IDCHG} + td\_gdrv\_off + tpdchg + tdoff\_min\_margin$$

5.3.2 Timing calculation with AGC = 2

Table 10 Timing calculations with AGC = 2

Step	Parameters [ns]	Formula	Look-up	
7	**Effective rise time**	$trise = \frac{Qgd}{ICHG}$		[2.7]
8	**Effective fall time**	$tfall = \frac{Qgd}{IDCHG}$		[2.8]
9	**Turn-on delay time**	$tdon = \frac{Qgs - tpchg \times IPCHG\_INIT}{ICHG} + td\_gdrv\_on + tpchg$		[2.9]
10	**Turn-off delay time**	$tdoff = \frac{Qg - Qgs - Qgd - tpdchg \times IPDCHG\_INIT}{IDCHG} + td\_gdrv\_off + tpdchg$		[2.10]
11	**FW turn-on time**	$ton\_fw = \frac{Ciss\_0v \times Vgh}{ICHG\_FW} + td\_gdrv\_on$		[2.11]
12	**FW turn-off time**	$toff\_fw = \frac{Ciss\_0v \times Vgh}{IDCHG\_FW} + td\_gdrv\_off$		[2.12]
13	**Active MOSFET blank time**	$tblank\_active = (tdon + trise) \times (1 + t\_margin)$	Table 12	[2.13]

Step	Parameters [ns]	Formula	Look-up	
14	**Active MOSFET CCP[2] time**	$tccp\_active = (tdoff + tfall) \times (1 + t\_margin)$	Table 12	[2.14]
15	**FW CCP time**	$tccp\_fw = toff\_fw \times (1 + t\_margin)$	Table 12	[2.15]
16	**FW blank time**	$tblank\_fw = ton\_fw \times (1 + t\_margin)$	Table 12	[2.16]

Table 11 Look-up table for the selection of the nearest typical available charge / discharge currents

Charge currents in PWM operations			Discharge currents in PWM operations		
ICHGx[4:0] ICHGxFW[4:0] IPCHGINITx[4:0]	**Range**	**Nom. charge current [mA]**	**IDCHGx[4:0] IDCHGxFW[4:0] IPDCHGINITx[4:0]**	**Range**	**Nom. charge current [mA]**
00000_B	0.0 ≤ x < 1.3	1.0	00000_B	0.0 ≤ x < 1.5	1.0
00001_B	1.3 ≤ x < 1.8	1.5	00001_B	1.5 ≤ x < 2.4	1.9
00010_B	1.8 ≤ x < 2.6	2.0	00010_B	2.4 ≤ x < 3.6	2.8
00011_B	2.6 ≤ x < 3.9	3.2	00011_B	3.6 ≤ x < 5.0	4.3
00100_B	3.9 ≤ x < 5.3	4.5	00100_B	5.0 ≤ x < 6.6	5.7
00101_B	5.3 ≤ x < 7.2	6.3	00101_B	6.6 ≤ x < 8.5	7.5
00110_B	7.2 ≤ x < 9.2	8.0	00110_B	8.5 ≤ x < 10.6	9.4
00111_B	9.2 ≤ x < 11.4	10.3	00111_B	10.6 ≤ x < 13.0	11.8
01000_B	11.4 ≤ x < 13.8	12.5	01000_B	13.0 ≤ x < 15.6	14.2
01001_B	13.8 ≤ x < 16.5	15.1	01001_B	15.6 ≤ x < 18.4	17.0
01010_B	16.5 ≤ x < 19.3	17.8	01010_B	18.4 ≤ x < 21.3	19.7
01011_B	19.3 ≤ x < 22.4	20.8	01011_B	21.3 ≤ x < 24.5	22.9
01100_B	22.4 ≤ x < 25.5	23.9	01100_B	24.5 ≤ x < 27.5	26.0
01101_B	25.5 ≤ x < 28.5	27.0	01101_B	27.5 ≤ x < 30.5	29.0
01110_B	28.5 ≤ x < 31.8	30.0	01110_B	30.5 ≤ x < 35.8	32.0
01111_B	31.8 ≤ x < 35.3	33.5	01111_B	35.8 ≤ x < 37.7	35.8
10000_B	35.3≤ x < 38.9	37.1	10000_B	37.7 ≤ x < 41.3	39.5
10001_B	38.9 ≤ x < 42.5	40.7	10001_B	41.3 ≤ x < 45.0	43.1
10010_B	42.5 ≤ x < 44.5	44.3	10010_B	35.3≤ x < 48.8	46.8
10011_B	44.5 ≤ x < 50.3	48.3	10011_B	48.8 ≤ x < 52.8	50.8
10100_B	50.3 ≤ x < 54.3	52.3	10100_B	52.8 ≤ x < 56.8	54.7
10101_B	54.3 ≤ x < 58.2	56.2	10101_B	56.8 ≤ x < 60.6	58.6
10110_B	58.2 ≤ x < 62.2	60.1	10110_B	60.6 ≤ x < 64.6	62.5
10111_B	62.2 ≤ x < 66.3	64.2	10111_B	64.6 ≤ x < 68.6	66.6
11000_B	66.3 ≤ x < 70.4	68.3	11000_B	68.6 ≤ x < 72.6	70.6
11001_B	70.4 ≤ x < 74.7	72.5	11001_B	72.6 ≤ x < 76.6	74.6
11010_B	74.7 ≤ x < 79.1	76.8	11010_B	76.6 ≤ x < 80.7	78.5
11011_B	79.1≤ x < 83.7	81.4	11011_B	80.7 ≤ x < 84.9	82.8
11100_B	83.7 ≤ x < 88.5	86.0	11100_B	84.9 ≤ x < 89.0	87.0
11101_B	88.5 ≤ x < 93.5	91.0	11101_B	89.0 ≤ x < 93.0	91.0

11110_B	93.5 ≤ x < 98.0	96.0	11110_B	93.0 ≤ x < 97.5	95.0
11111_B	98.0 < x	100.0	11111_B	97.5 ≤ x	100.0

Table 12 Look-up table for the selection of the blank time and cross-current protection times

TBLANKx_ACT[2:0]	Min. tblank [ns]	Nom. tblank [ns]	TCCPx_ACT[2:0]	Min. tccp [ns]	Nom. tccp [ns]
000_B	500	625	000_B	300	375
001_B	800	1000	001_B	500	625
010_B	1000	1250	010_B	800	1000
011_B	1200	1500	011_B	1200	1500
100_B	1600	2000	100_B	1600	2000
101_B	2400	3000	101_B	2400	3000
110_B	3200	4000	110_B	3200	4000
111_B	12800	16000	111_B	12800	16000

6 Adaption of the gate charges to the application conditions

The MOSFET Qgs, Qgd and Qg are specified for specific conditions. Refer to Figure 11: IPZ40N04S5-3R1: Vs = 32 V, Vgs from 0 to 10 V and Ids = 40 A.

However, the value of the gate charge depends on the supply voltage, the load current ([3] [4]), and Vgh (11 V typ. for the TLE9210x and not 10 V as usually specified in the MOSFET datasheets).

6.1 Adaption of Qgs (at Vds = Vs)

During the turn-on of the active MOSFET until Vgs = Vplateau, the current delivered by the gate driver charges Ciss. Therefore the charge injected in the MOSFET gate until Vgs reaches Vplateau is equal to Ciss_vs x Vplateau

Qgs (at Vds = Vs) = Ciss_vs x Vplateau

Example: Vs = 14 V, Vplateau = 4.2 V

Ciss_vs ~ 1740 pF

Qgs = 1740 x 10^{-12} x 4.2 ~ 7.3 nC

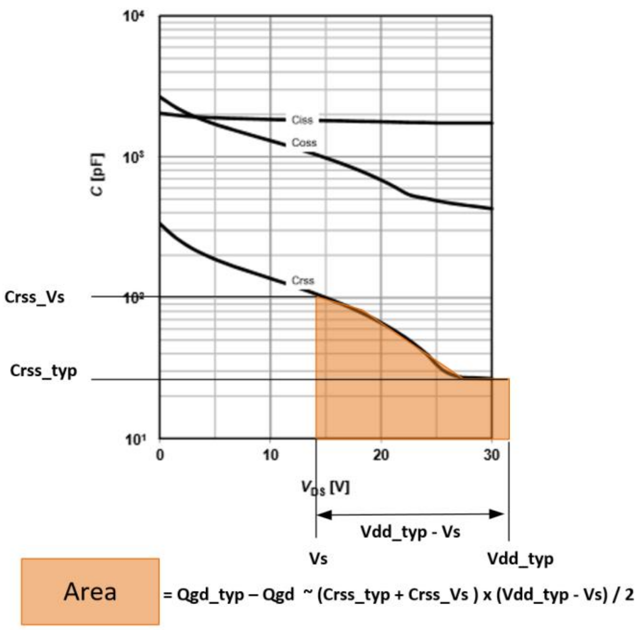
6.2 Adaption of Qgd (at Vds = Vs)

An estimation of Qgd consist in using Qgd_typ and substracting the gate charge related to Crss between Vdd_typ and Vds = Vs ([3] [4]). The gate charge difference is represented by the highlighted area in Figure 17.

Approximating this area to a trapezoid, gives Qgd_typ – Qgd ~ x (Crss_vs + Crss_typ) x (Vdd_typ - Vs) / 2.

Qgd = Qgd_typ - (Crss_vs + Crss_typ) x (Vdd_typ - Vs)/ 2.

Figure 17 Estimation of the difference between Qgd_typ and Qds



Example: MOSFET IPZ40N04S5-3R1, Vs = 14 V, Vdd_typ = 32V

Crss_vs = 100 pF, Crss_typ ~ 27 pF, Qgd_typ = 7.1 nC

Qgd = 7.1 x 10^{-9} – (100 + 27) x 10^{-12} x (32 - 14) / 2 ~ 6.0 nC

6.3 Adaption of Qg at (Vds = Vs)

During the turn-on phase of the active MOSFET, the remaining charge delivered by the MOSFET driver between the end of the Miller plateau and Vgs = Vgh represents the charge required to charge Ciss_0v from Vplateau to Vgh.

Qg – Qgd – Qgs = Ciss_0v x (Vgh – Vplateau)

Qg = Ciss_0v x (Vgh – Vplateau)

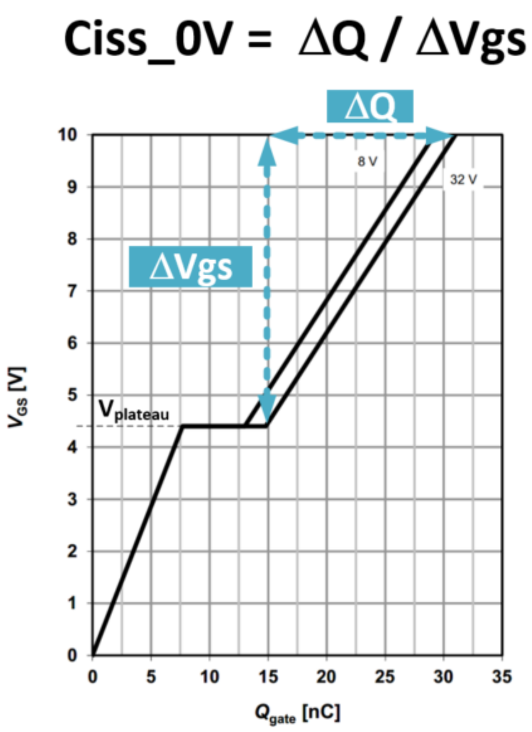
Where Ciss_0v is the MOSFET input capacitance with Vds close to 0 V

This parameter is not directly provided in the MOSFET datasheets. It is the inverse slope of the graph Vgs versus gate charge (Figure 18).

Ciss_0v = (Qg_typ – Qgs_typ – Qgd_typ) / (Vgh_typ – Vplateau_typ)

Qg = Qgd + Qgs + Ciss_0v x (Vgh – Vplateau)

Figure 18 Determination of Ciss_0v (IPZ40N04S5-3R1)



Example:

MOSFET IPZ40N04S5-3R1, Vs = 14 V,

Vgh_typ = 10V, Vgh = 11 V

Qgs_typ = 7.7 nC, Qgd_typ = 7.1 nC, Qg_typ = 31 nC

Vplateau_typ = 4.4 V, Vplateau = 4.2 V

Ciss_0V = $\frac{(31-17.1-7.7) \times 10^{-9}}{(10-4.4)}$ ~ 2.89 nF

Qg = 7.3 + 6.0 + 2.89 x 10^{-9} x (11 – 4.2) ~ 33 nC

7 Conclusions

This application note provides recommendations for the setting of the gate driver of the TLE92108/4 in PWM operation. It also gives step-by-step calculation details used by the gate driver setting tool for the determination of the MOSFET driver currents and timings and the resulting MOSFET switching times, for an open loop control.

However, the MOSFET switching times are dependent from the application conditions (e.g. current, voltage timings) and is subject to the production spread of the MOSFET and the Muti MOSFET driver itself.

To overcome the limitations of an open loop control, the TLE92104/8 also integrates features with allows a closed loop regulation of the switching times:

- a self-regulation of tdon and tdoff can be done by the TLE9210x
- a closed loop regulation of trise and tfall can be done by the microncontroller thanks to measured in-application switching times provided by theTLE9210x. The principle is described in the application note [3].

8 References

[1]. Datasheet TLE92108-231, *Link*

[2]. Datasheet TLE92108-232, *Link*

[3]. Rise and fall time regulation with current source MOSFET drivers *Link*

[4]. AND9083. MOSFET gate charge origin and its applications. *Link*

[5]. Datasheet IPZ40N04S5-3R1. *Link*

Revision history

Document version	Date of release	Description of changes
V 1.0	2020-07-23	First release

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Edition 2020-07-23

Published by

Infineon Technologies AG

81726 Munich, Germany

Do you have a question about this document?

Email: erratum@infineon.com

Document reference
Z8F69700390