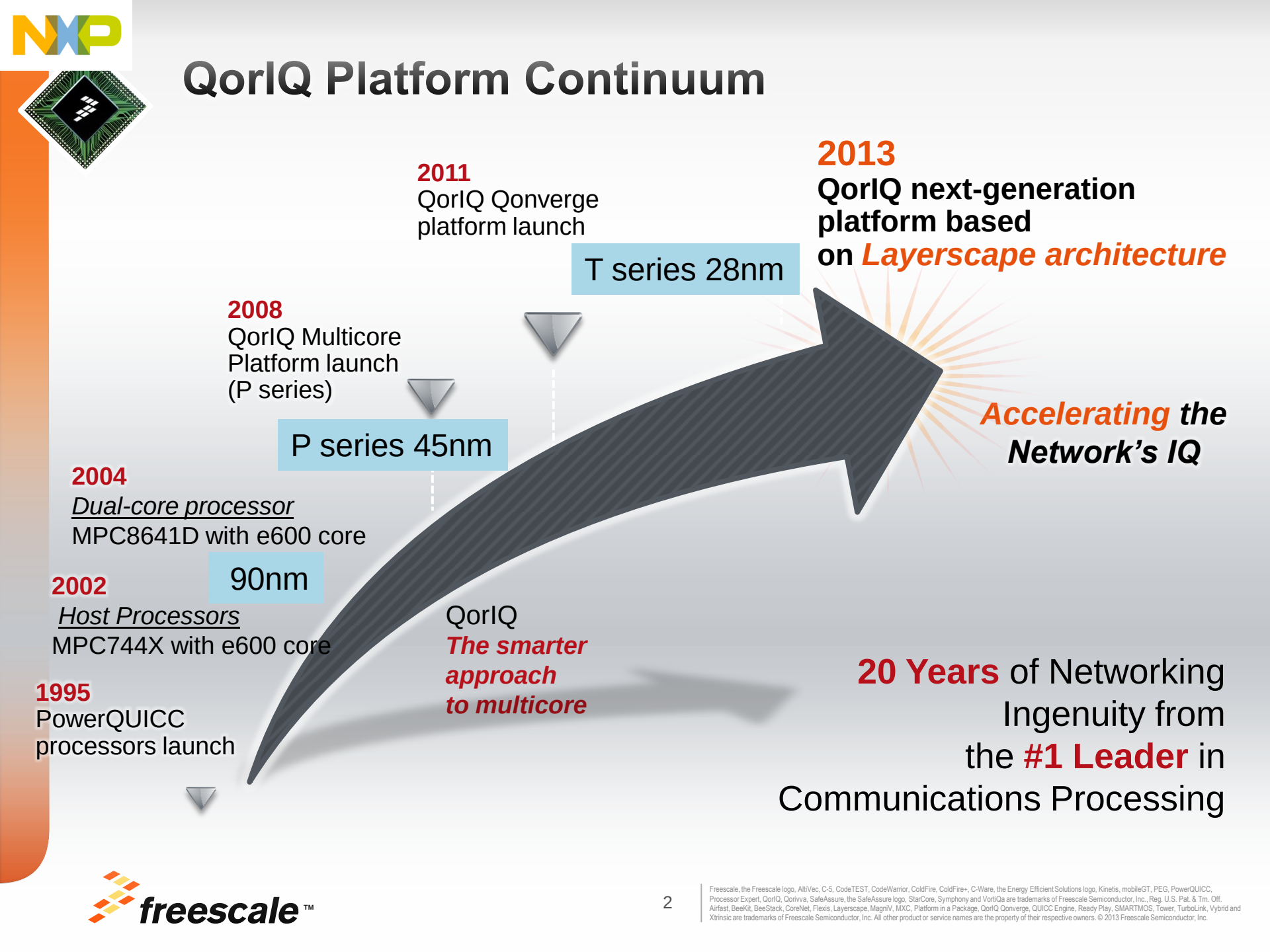
High-end Industrial and Network Processing

Nigel James
Field Applications Engineer

TechDays 2013

QorIQ Platform Continuum

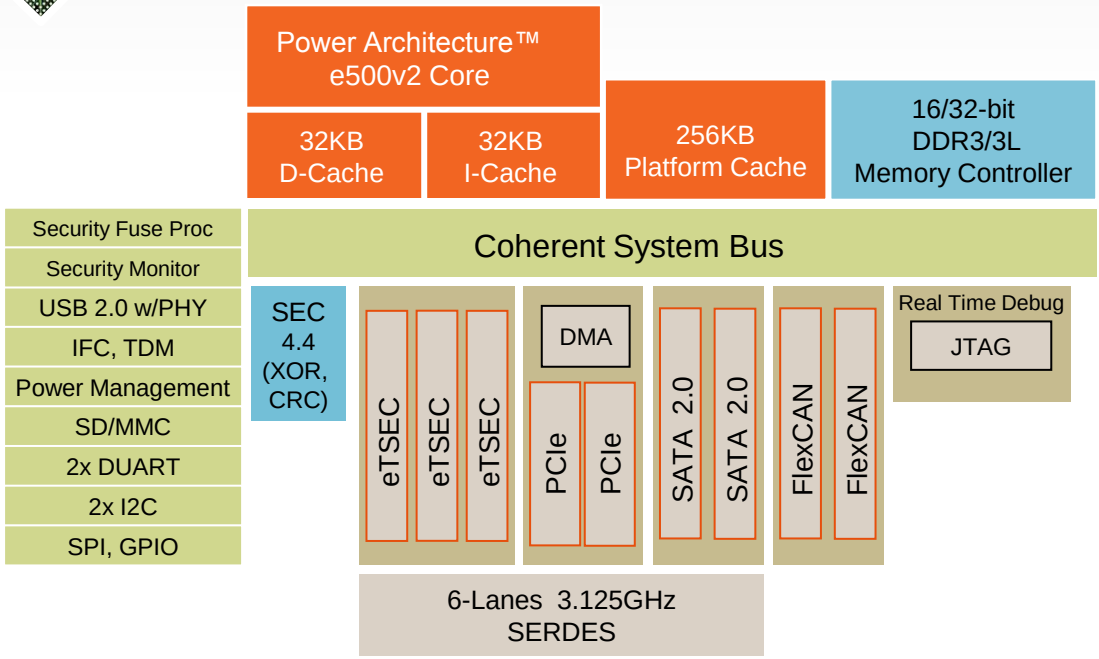


20 Years of Networking Ingenuity from the **#1 Leader** in Communications Processing

QorIQ Processing Platforms

High-performance Tier • Up to 2.4 GHz • 1 to 24 cores • Large L2 caches	• LS3 (future) • T4240/T4160 • P5040/P5021 • P5020/P5010 • P4080/P4040	 **Service Provider Routers**  **Network Admission Control**  **Storage Networks**
Mid-performance Tier • Up to 1.8 GHz • Highly-parallelized workloads • 48 Gbps IP forwarding • High amount of off-load	• LS2 (future) • T2080/T2081 • P3041 • P20x(4)	 **Metro Carrier Edge Router**  **Aerospace & Defense**  **Access Gateway**
Value-performance Tier • Up to 1.8 GHz • 3W fanless designs • Broadest portfolio of power-efficient SoCs	• LS1 families • T1040/T1042 • T1020/T1022 • P101x(8), P102x(5),	 **UTM Security Appliances**  **Industrial Computing & Networking**  **Enterprise Routers/Switches**

QorIQ P1010



Device

- 45nm SOI Process
- 425-pin TEPBGA I
- 19 x19mm, 0.8mm pitch

Power

- <3W
- -40C to +105C Tj

Processor

- e500v2, 32b, 533 - 800 MHz
  - 36-bit physical addressing
- Memory SubSystem
  - 256KB Frontside L2 cache w/ECC
  - 32-bit DDR3/3L, 800 MHz data rate
  - 16-bit DDR3/3L, 800 MHz data rate w/ECC

High Speed Serial IO

- 2 PCIe 1.1 Controllers (2.5GHz)
- 2 SATA 2.0 3Gb/s
- 1 USB 2.0 with PHY
  - Host/Device support
- 2 FlexCAN 2.0b Controllers

Network IO

- 3 eTSECs (10/100/1000)
  - Software fastpath acceleration
  - 1588v2 support
  - Up to 2 with SGMII

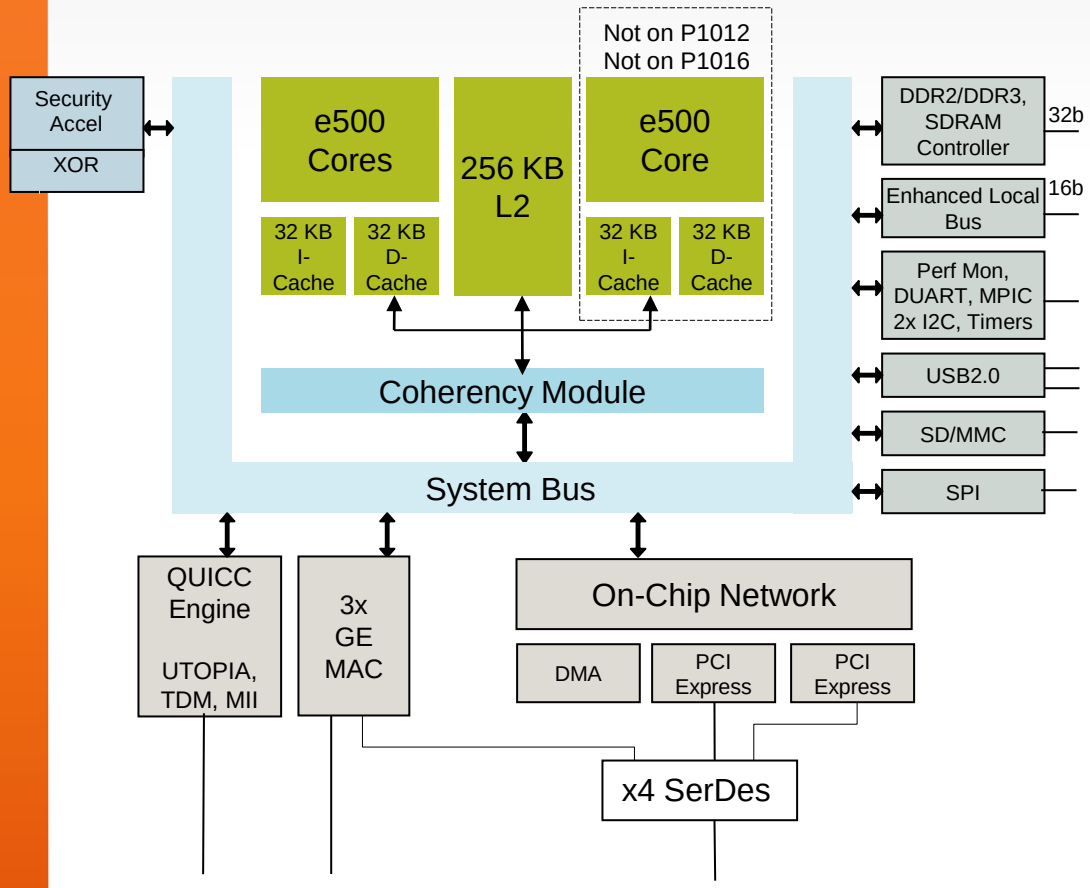
Misc IO

- TDM
- Flash Controller supporting NOR, SLC and MLC based NAND devices
- SD/MMC card controller
- 2x DUARTs, 2x I2Cs

Acceleration

- SEC 4.4 - crypto acceleration 2Gbps
- Secure Boot

QorIQ P1021/P1025 Block Diagram



- P1025/P1016 product option available in small foot print package
- Supports 400-667 MHz operation
- DDR3 only for lowest possible power
- 561-pin TePBGA-1, 23 mm x 23 mm

Dual e500v2 Power Architecture cores
- 533-800 MHz
- 256 KB frontside L2 cache w/ECC, HW cache coherent
- 36-bit physical addressing, DP-FPU

System unit
- 32-bit DDR2/DDR3, 667 MHz data rate w/ECC
- Integrated SEC 3.3 security engine
- Open programmable interrupt controller, perf mon, 2x I^2C, timers, 16 GPIOs, DUART
- 16-bit enhanced local bus supports booting from NAND Flash
- USB 2.0 controllers host/device support
- SPI controller supporting booting from SPI serial Flash
- SD/MMC card controller supporting booting from Flash cards
- Three 10/100/1000 Ethernet controllers (VeTSEC) w/jumbo frame support, SGMII interface
  - IEEE1588 v2 support
- QUICC Engine for protocol offload and legacy interfaces
  - TDM interfaces with HDLC support
  - UTOPIA-L2 interface for ATM support
- Two PCI Express 1.0a controllers operating up to 2.5 Gbps
- Power management

Process and package
- 45nm SOI, 0.95V+/-50mV, -40C to 125C Tj
- 689-pin TePBGAII

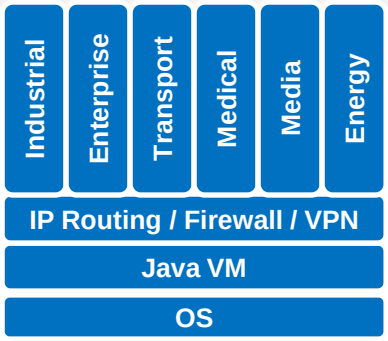
<5W max for 800 MHz

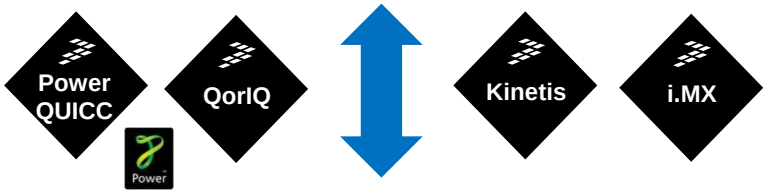
Tower Systems

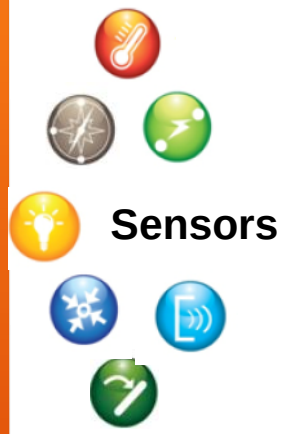
Apps

Stacks

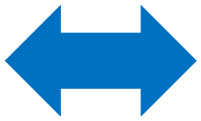
Gateway







Sensors



Wired and Wireless Backhaul

Controller Module: TWR-P1025

QorIQ P1025 Controller Module

TWR-P1025

MSRP: $199
Launch: April 2012
First Deliveries: May 2012

Hardware:

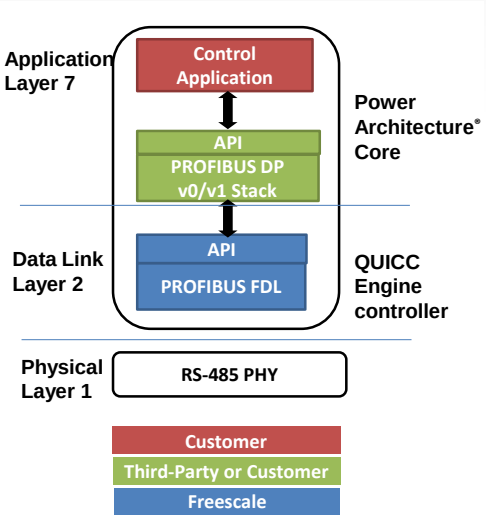
- QorIQ P1025 dual-core processor
- Tower compatible processor module
- JTAG 14-pin header
- User-controlled status LEDs
- DIP Switches and push buttons for user input
- 512 MB of DDR3 memory
- Boot from NOR flash or eSDHC
- Two GETH interfaces (both RGMII)
- One PCIe interface x1 (mini-PCIe+USB)
- Two USB 2.0 interfaces
- Two UART interfaces (via mini-USB)
- One accelerometer (on I^2C)
- QE UART header (provides RS485 connectivity via interface card)

Software:

- Linux® 3.0 SDK
- MQX™ RTOS
- CodeWarrior IDE

- Demo kit with 5x Tower System end applications
- 100% compliant with Tower System infrastructure

PROFIBUS Solution Partners



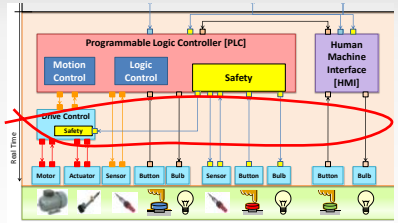
Pre-integrated, certifiable PROFIBUS solutions:

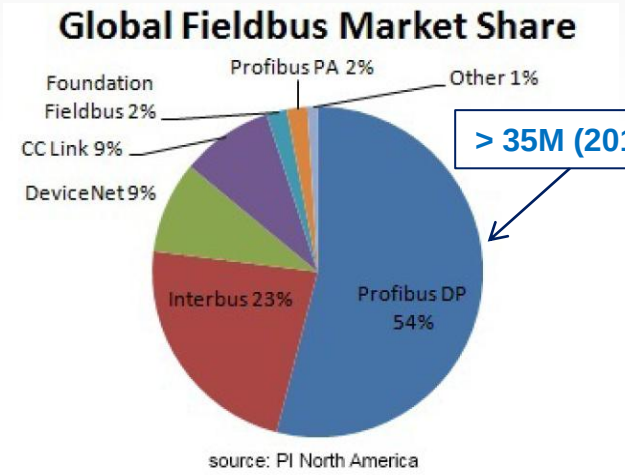
TMG Automation www.tmgte.de/en/
- PROFIBUS DP master and slave stack
- PROFIBUS development services

Freescale www.freescale.com/PROFIBUS
- QorIQ and PowerQUICC processors
- Tower System with Linux® OS
- email: profibus@freescale.com

freescale.com/PROFIBUS

Interconnect





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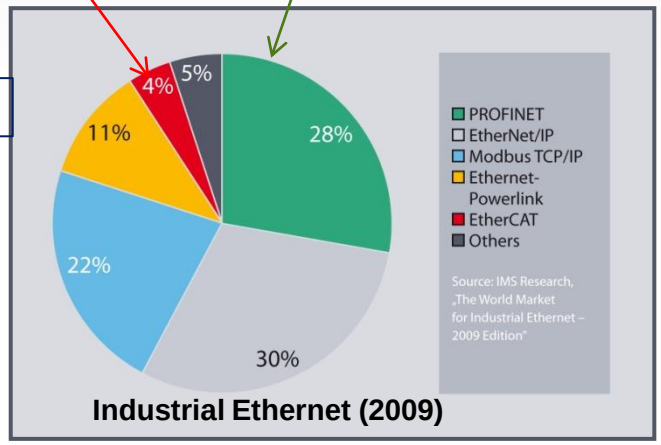


Certified on QorIQ*

Ported to QorIQ

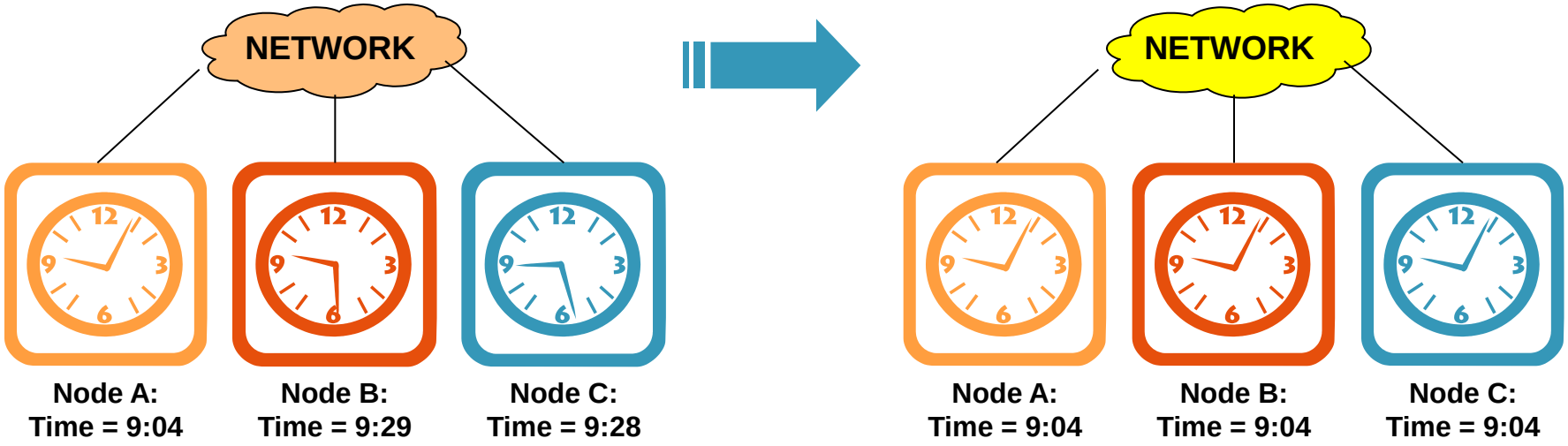
op Field bus	Compatibility	ernet protocols
PROFIBUS Master / Slave*	Siemens ← →	Siemens
DeviceNet	Rockwell ← →	Rockwell
CANopen CAN	Many ← →	Beckhoff

PROFINET IRT Slave

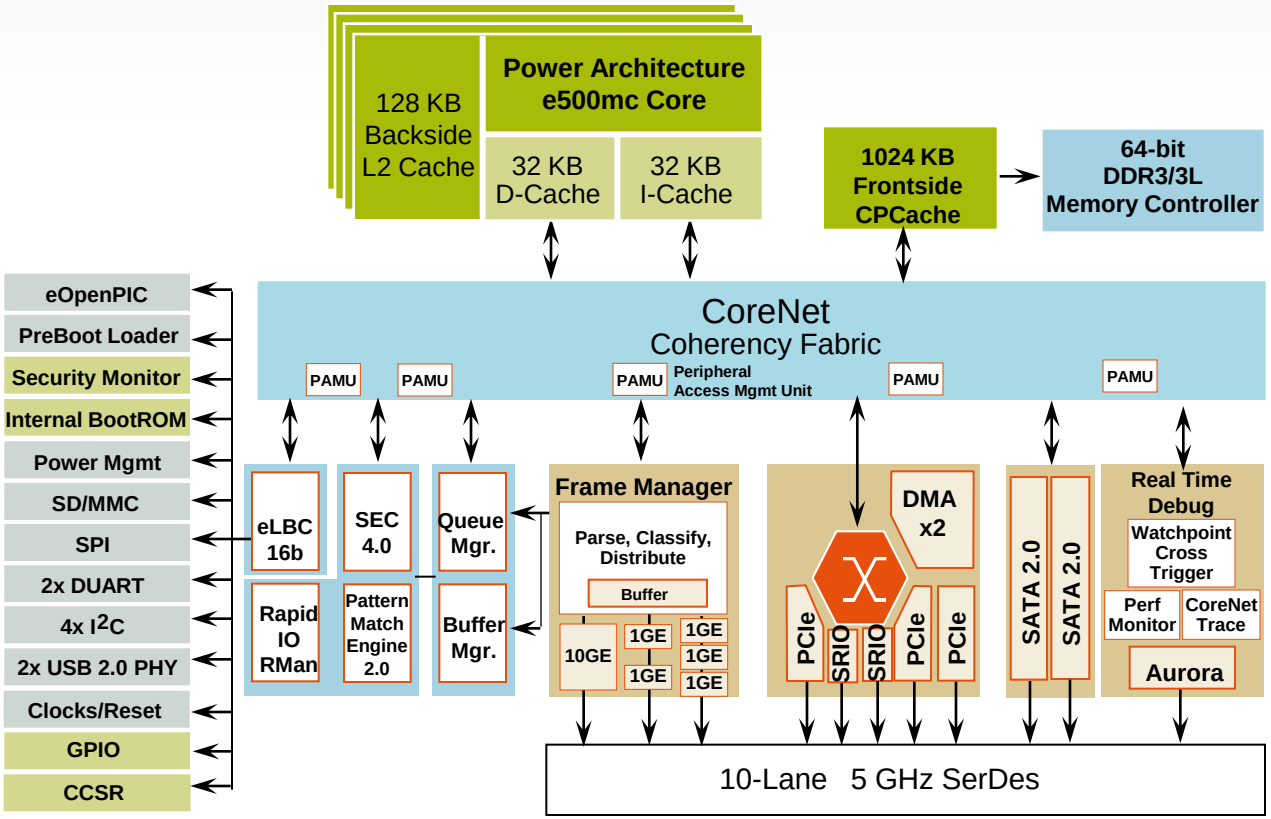
EtherNet/IP

EtherCAT (Master)

- IEEE 1588 – Standard for a Precision Clock Synchronization Protocol
  - The standard defines a Precision Time Protocol (PTP) designed to synchronize real-time clocks in a distributed system
  - Intended for local area networks using multicast communications (including Ethernet)
  - IEEE 1588 was designed to work within a building or factory
    - Intended typically for industrial automation and test and measurement systems (e.g. synchronized printing presses)
  - Targeted accuracy of microsecond to sub-microsecond
  - Version 1 approved September 2002 and published November 2002
  - Version 2 approved March 2008 and published August 2008
  - Available from the IEEE 1588 web site (http://ieee1588.nist.gov)



QorIQ P2041



Qualification Rev 1.1: Jun 2012
Qualification Rev 2.0: Apr 2013

Quad e500mc Power Architecture®
- 4 cores (up to 1.5 GHz)
- 128 KB private backside L2 per core
- 1 MB shared CoreNet platform cache w/ECC

Memory controller
- DDR3/3L SDRAM up to 1333 MHz
- 32/64 bit data bus w/ECC

High speed interconnect
- 3 PCIe 2.0 Controllers
- 2 sRapidIO 2.1 Controllers
  - Type 9 and 11 messaging
- 2 SATA 2.0

CoreNet switch fabric

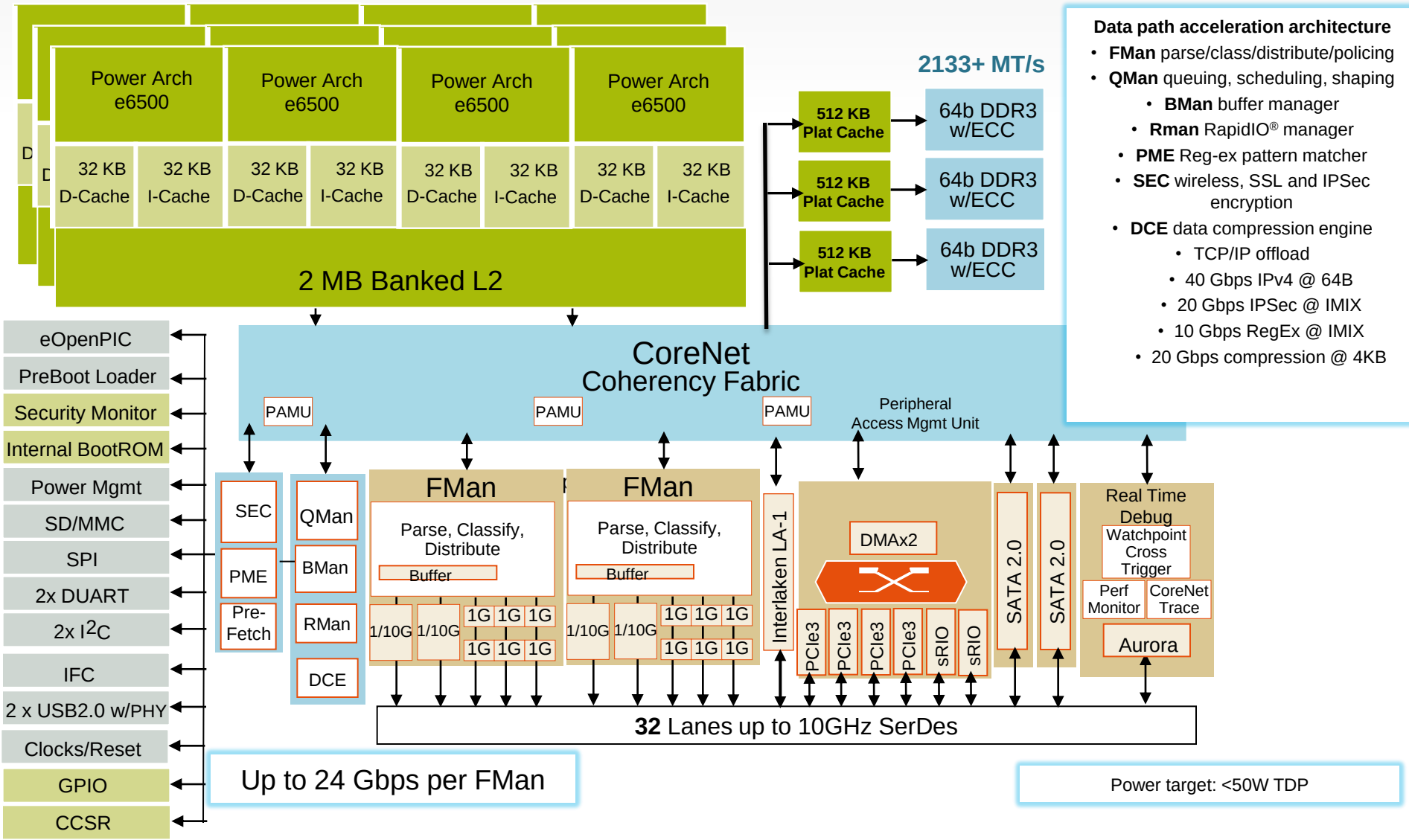
Ethernet
- 5 x 10/100/1000 Ethernet controllers
  - Or 4x 2.5 Gbps SGMII
- 1 x 10GE controller
- All w/ classification, H/W queuing, policing, buffer management, checksum offload, QoS, lossless flow control, IEEE® 1588
- Up to 5 SGMII or 2.5 Gbps SGMII, 2 RGMII

Data path acceleration
- SEC 4.0
- PME 2.0

Device
- 45nm SOI process
- 783-pin package
  - 23 x 23 mm, 0.8 mm pitch
  - Pin compatible with P2040
- 12.5W thermal max (est) w/o I/O at 1.2 GHz

QorIQ T4240

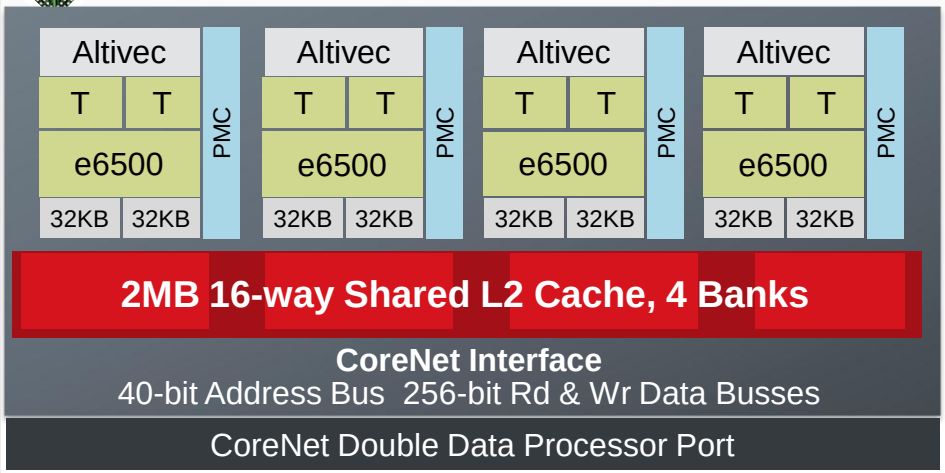
12 x 64-bit, dual-threaded cores with AltiVec—up to 1.8 GHz



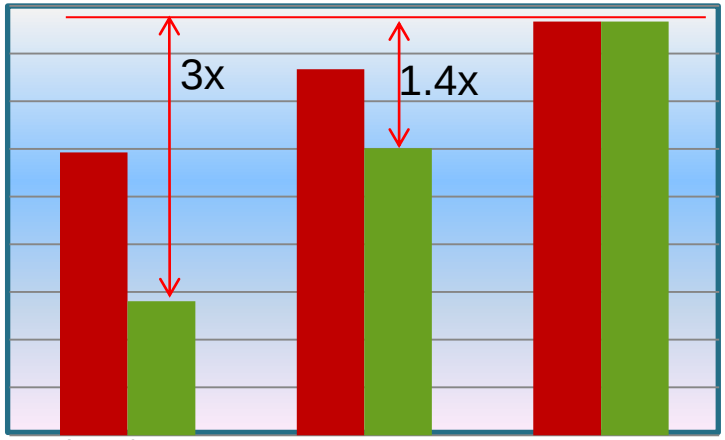
Data path acceleration architecture

- **FMan** parse/class/distribute/policing
- **QMan** queuing, scheduling, shaping
  - **BMan** buffer manager
  - **Rman** RapidIO® manager
  - **PME** Reg-ex pattern matcher
  - **SEC** wireless, SSL and IPSec encryption
  - **DCE** data compression engine
    - TCP/IP offload
    - 40 Gbps IPv4 @ 64B
    - 20 Gbps IPSec @ IMIX
    - 10 Gbps RegEx @ IMIX
    - 20 Gbps compression @ 4KB

Performance starts with the Core: e6500



Core Performance CoreMark™ Benchmarks



Dual 6C/12T server processors @2.266GHz *

32 core processor @1.5GHz*

12C/24T T4240 @1.8GHz

CoreMark™

CoreMark™ / Watt

*Source: www.coremark.org

High Performance

- 64-bit Power Architecture® ISA v2.06 core
- Dual threads provide 1.7 times the performance of a single thread
- Clustered L2 cache allowing strict allocation or full sharing
- 128-bit AltiVec SIMD unit
  - 192 GFLOP aggregate

Large Memory Space

- 40-bit physical address

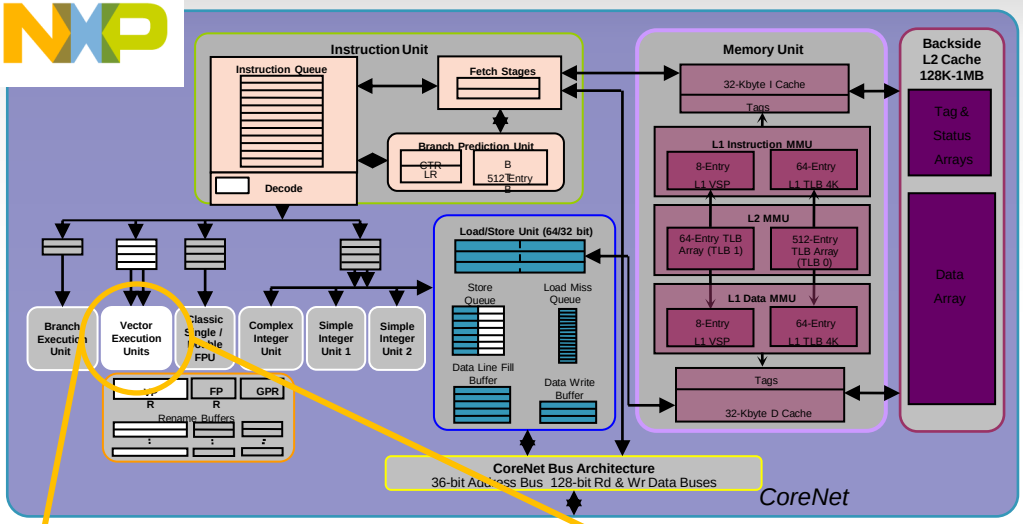
Increase Productivity

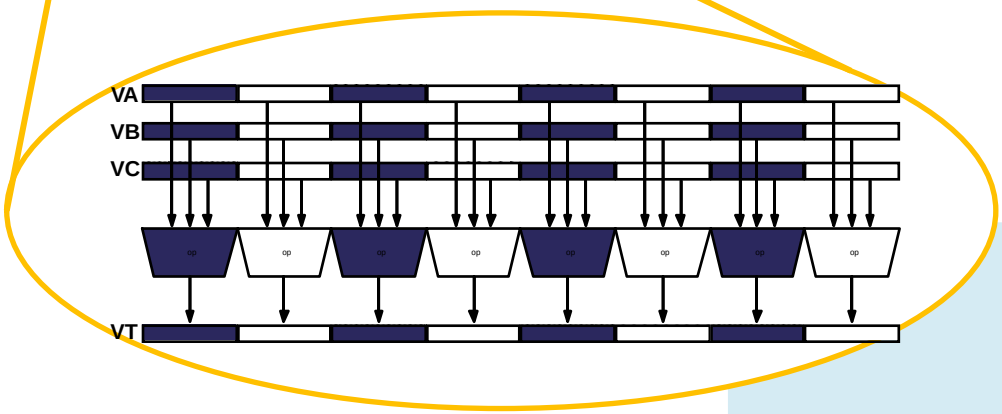
- Core Virtualization
  - Hypervisor
  - Logical to Real Address Translation

Energy Efficiency

- 1.4 to 2 times more power efficient than the nearest competition
- Drowsy: core, cluster, AltiVec

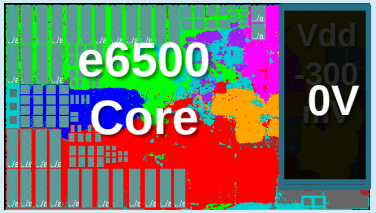
Altivec Accelerator
High-Performance, Low-Power

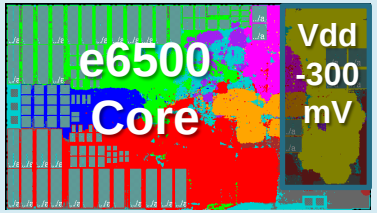




Characteristics

- 128-bit vector size
- Separate register file with 32 registers
- Vector-element datatype of 8, 16, 32-bit signed/unsigned int, and IEEE SP float
- 162 instructions
- Intra and inter-element arithmetic instructions
- Intra and inter-element conditional instructions
- Powerful Permute, Shift and Rotate, Splat, Pack/Unpack and Merge instructions
- Saturation or modulo arithmetic
- Four-operand, non-destructive instruction format
- Modeless operation for zero-overhead use of AltiVec instructions
- Simultaneous dispatch of one ALU-class vector and one permute-class vector, or either paired with a vector load/store
- All instructions fully pipelined with single-cycle throughput





Altivec is a **vector architecture** allows the simultaneous processing of multiple data items in parallel. Operations are performed on multiple data elements by a single instruction. This is referred to as Single Instruction Multiple Data (SIMD) parallel processing.

Technique	Power Gating (Shut Down)	Lowered Vdd (Drowsy w/ State Retention)
Use Cases	Products w/o AltiVec	Applications with periodic AltiVec
Idle Leakage Power (mW/Core, T4240)	5mW (90% savings)	28mW (50% savings)

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AltiVec Applications

Aerospace & Defense

Civil Radar
Military Radar
Counter-measures

Avionics

Flight computers
Flight control systems
Displays

Industrial & Communication

Image Analysis
Multi-axis control
Robotics

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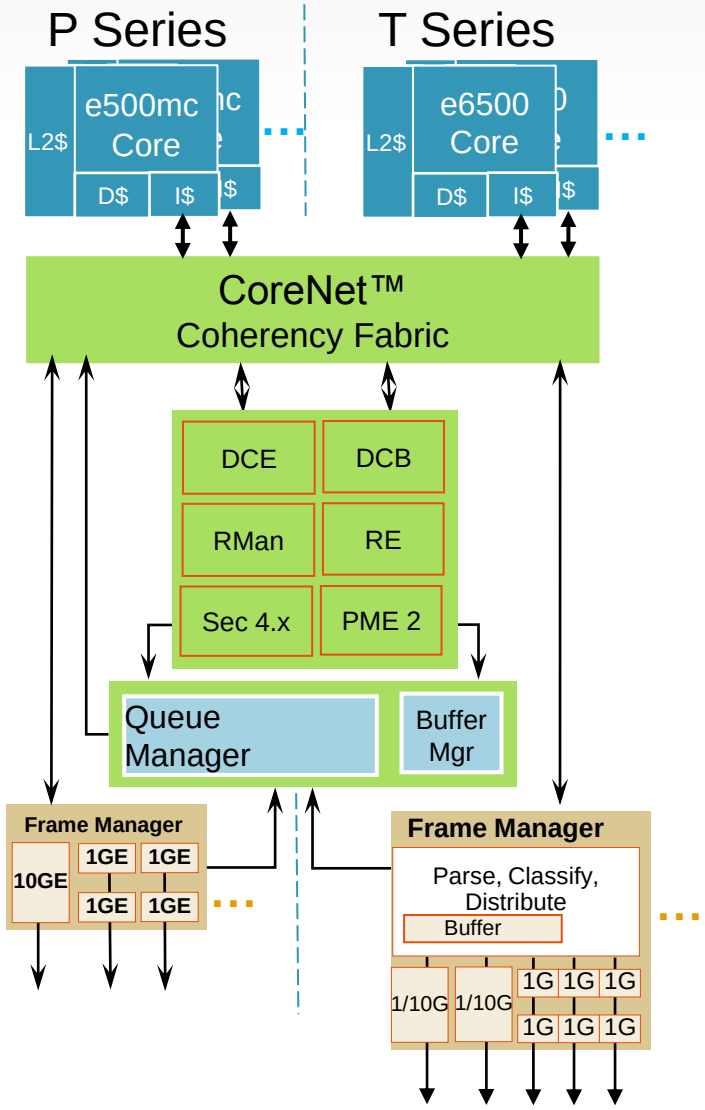
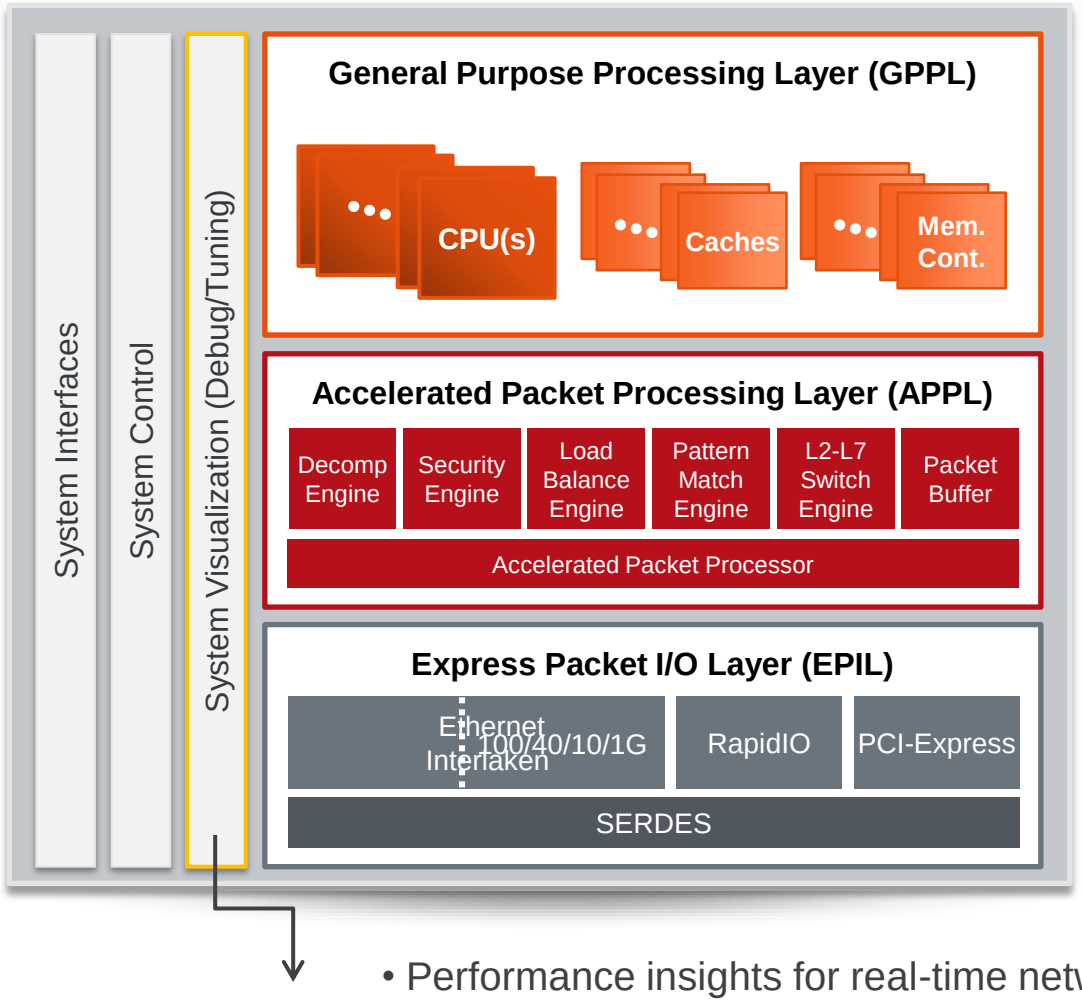
Data Path Acceleration Architecture

- DPAA is designed to balance the performance of **A**ccelerators with seamless **I**ntegration
  - ANY packet to ANY core to ANY accelerator or network interface efficiently WITHOUT locks or semaphores.
- “Infrastructure” components
  - Queue Manager (QMan)
  - Buffer Manager (BMan)
- “Worker” Components
  - Cores
  - Frame Manager (FMan)
  - RapidIO Message Manager (RMan)
  - Cryptographic accelerator (SEC)
  - Pattern matching engine (PME)
  - Decompression/Compression Engine (DCE)
  - DCB (Data Center Block)
  - RAID Engine (RE)
- CoreNet
  - Provides the interconnect between the cores and the DPAA infrastructure as well as access to memory.



QorIQ Layerscape Architecture

GPP Layer
APP Layer
EPI Layer



- Core-agnostic (Power Architecture® or ARM® cores)
- Consistent APIs/libraries with tools abstract hardware changes
- Single framework for programming GPPL/APPL

- Capable of fully autonomous offload
- Synchronous run to completion model
- True programmability

- Deterministic performance
- Scalability from 1G-100G
- Packetized I/O between all interfaces supporting L2+ switching

- Performance insights for real-time network adjustments

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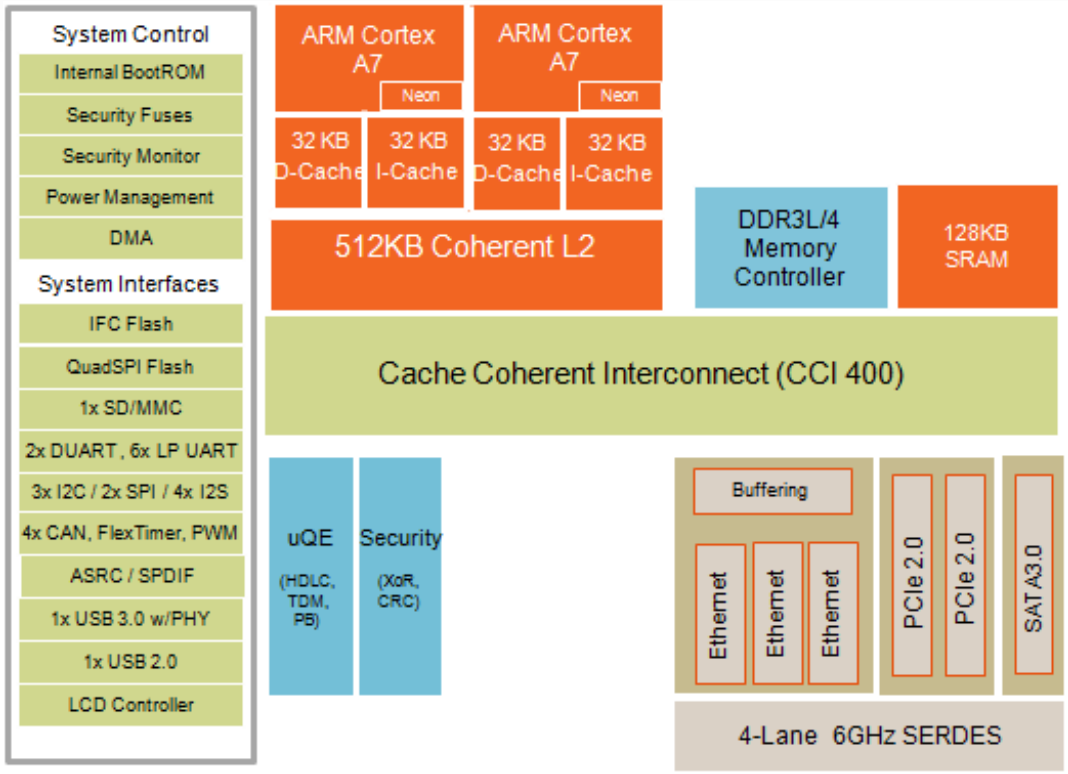
QorIQ LS1021A



- **Dual ARM Cortex-A7 cores up to 1.0 GHz**
- ECC protected L1/L2 caches
- NEON
- Excellent Coremark / mW ratio
- ARM AMBA4 MPCore™ Virtualization
- QorIQ Trust Architecture and ARM TrustZone support
- 3-port GigE with IEEE 1588
- 2x PCI Express Gen2
- Multi-protocol 4-Lane SerDes
  - PCIe, SATA3, SGMII
- QUICC Engine – HDLC/TDM/ProfiBUS
- EnergyStar support with fast wakeup
- 2Gbps IP forwarding

Key System Integration Features:

- Low-cost NAND/NOR flash systems
- DDR3L/4 interface with ECC support
- USB3 SuperSpeed
- Audio networking and motor control

Package & Board:

Package:	525-pin, 19x19mm, 0.8mm pitch
Power:	~3.7W @1.0GHz Typical
Temp:	-40C to 105C Tj
Boards:	Tower low-cost board Freescale Linux BSPs

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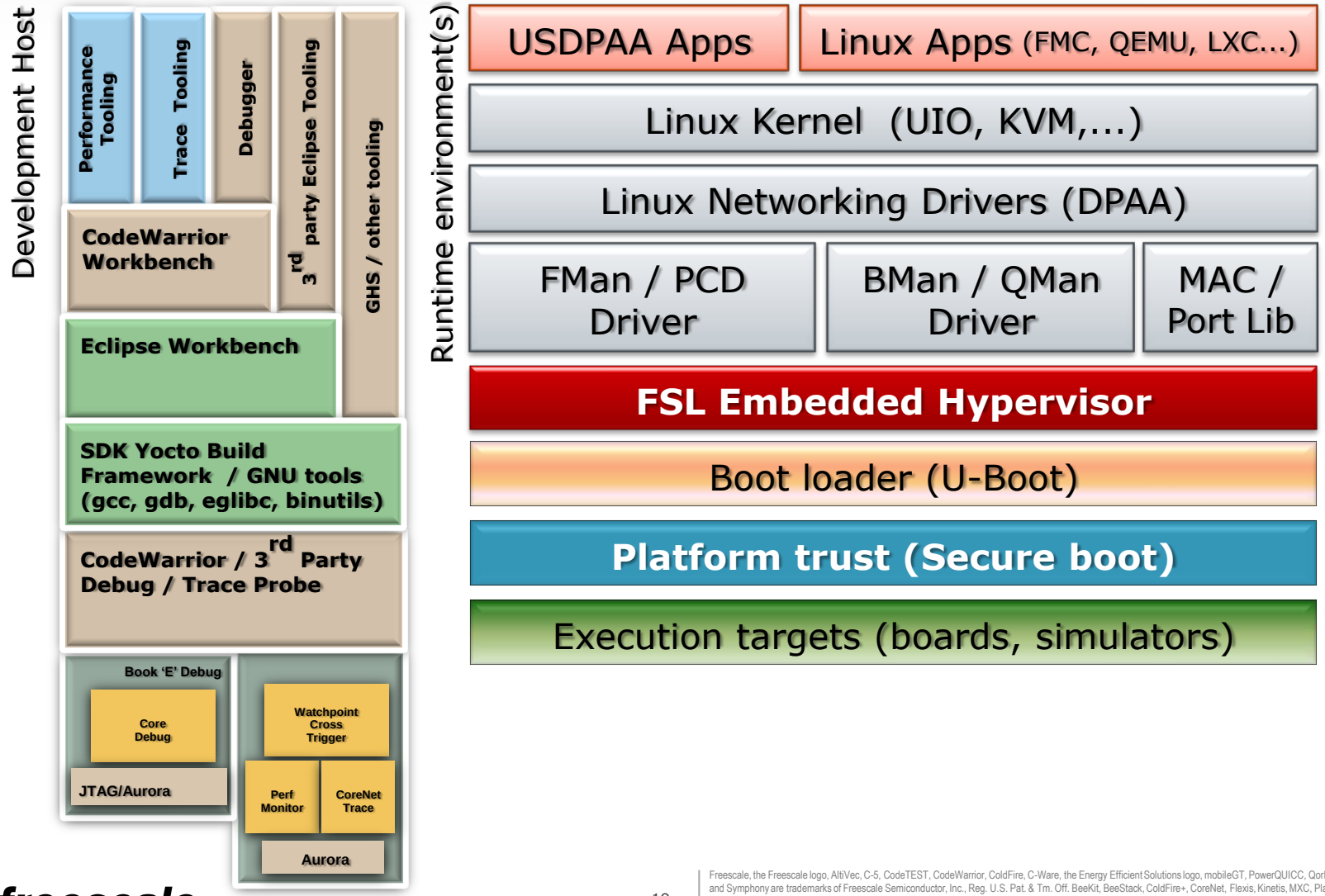
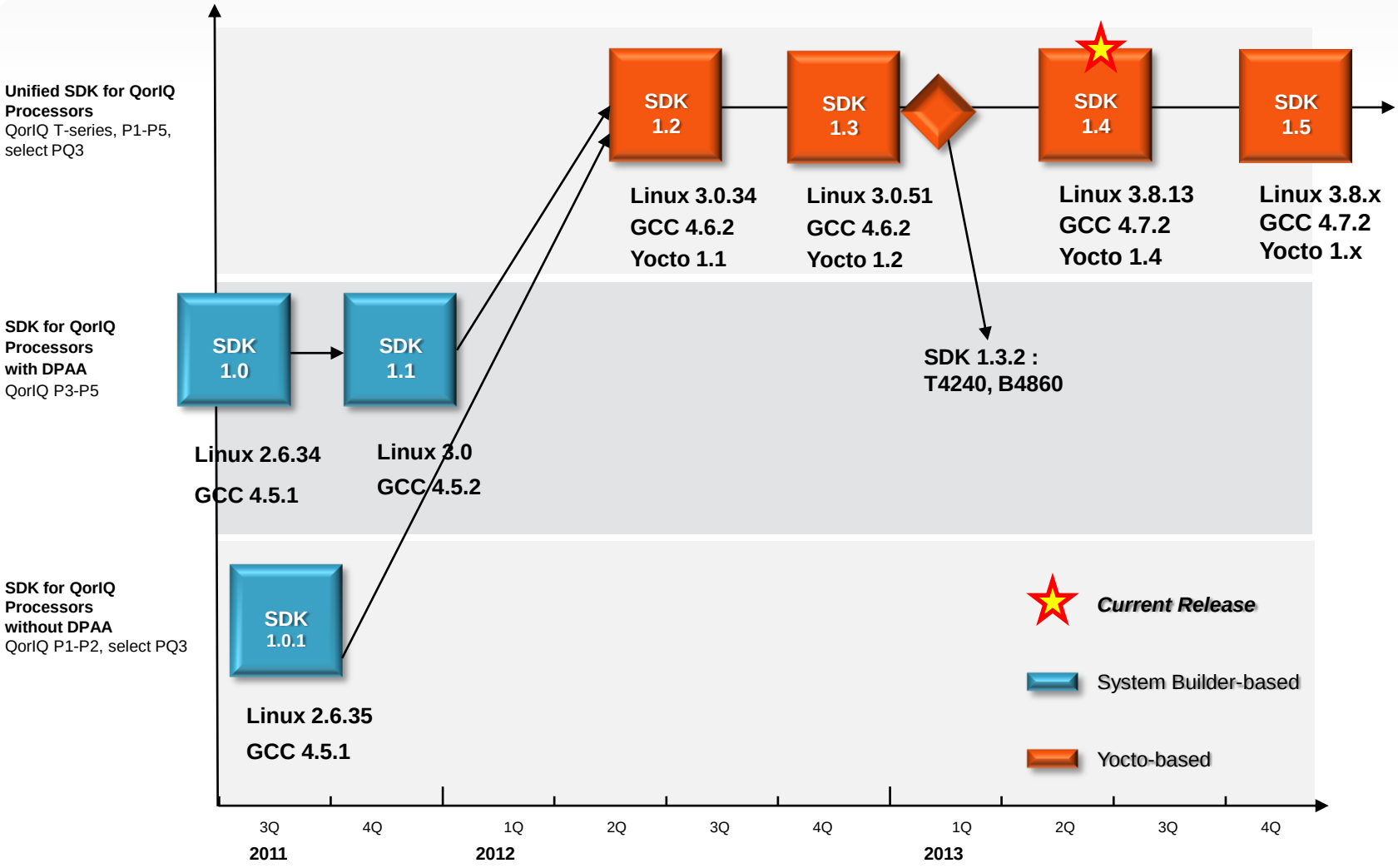
Freescale QorIQ™ SDK
Components



QorIQ Linux SDK Release Roadmap



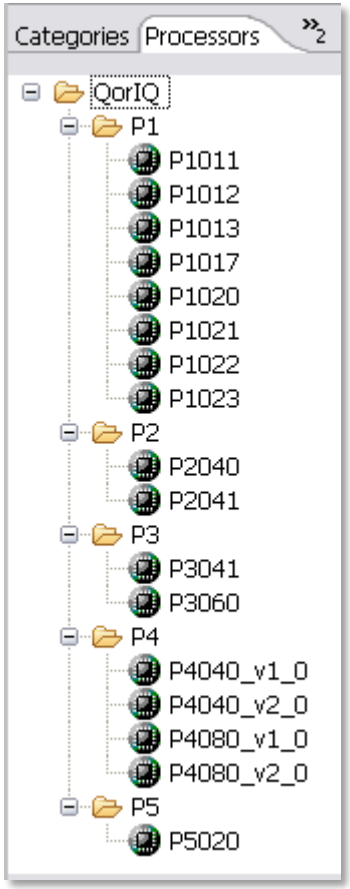
QorIQ Configuration Suite
What is QCS ?

- A no-cost configuration tool for QorIQ platforms based on Freescale's Processor Expert framework
- Generates source files for use in board initialization code
- A pure Java solution :
  - works on Windows, Linux, Solaris, Mac OS,...
- Available as an Eclipse plug-in for :
  - CodeWarrior Development Studio for Power Architecture v10.x
  - Generic Eclipse 3.5.1 or 3.6.1 C/C++ environment
  - Available for download now : **http://www.freescale.com/qcs**

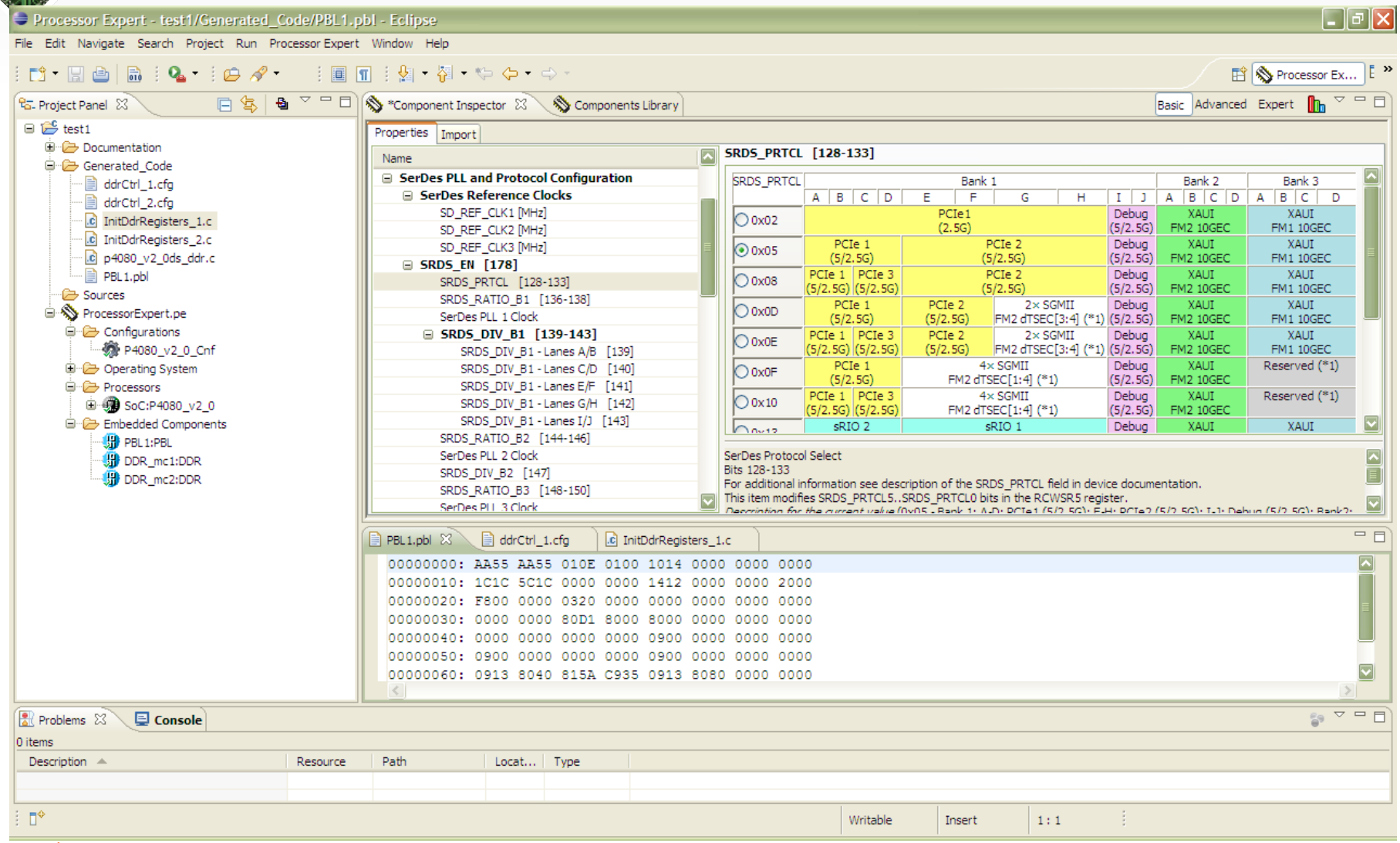
QorIQ Configuration Suite

- Configuration Tool :
  - Pre-Boot Loader (PBL) tool
  - DDR configuration tool
  - DPAA tool :
    graphical editor for data path flow configuration
  - Device Tree editor :
    supports references, synchronous GUI & XML editing, node validation based on specification bindings.

- Supported SoCs :



QCS example showing SerDes configuration



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Embedded Board Solutions

The embedded board market offers a wide range of form factor solutions that provide OEM's quicker time to market, lower development costs and resolution to many of the challenges associated with high-speed microprocessors, I/O and memory subsystems design. Combining Freescale's Power Architecture® and i.MX processors with the Embedded board ecosystem results in a robust mix of form factors built to service a broad range of applications and markets. A broad array of form factors such as VME/VPX, ATCA/AMC, COM Express, System on Modules (SOMs) and custom solutions can be found here. The end result: easing the Make vs Buy decision.

View our Embedded Board Solutions Selector Table ▸

Design Resources

- Embedded board solutions fact sheet *(pdf)*
- Broadband/LTE Base Station Brochure *(pdf)*
- Industrial Single Board Computer Applications
- COM Express Whitepaper *(pdf)*
- Trusted Computing Whitepaper *(pdf)*
- WiMAX Base Station Brochure *(pdf)*

Design Partners

- Advantech
- Boundary Devices Inc.
- BlueTechnix
- CES
- Curtiss-Wright Controls Embedded Computing
- Digi
- Embedded Planet
- Emerson
- Eurotech
- Extreme Engineering Solutions (X-ES)
- GE Intelligent Platforms
- Interface Masters Technologies
- iWave Systems Technologies Pvt Ltd.
- Mercury Computer Systems
- MicroSys Electronics
- NAT
- Orion Technologies, Inc.
- TQ

Featured Video

Embedded Board Solutions
(Video - 2:38) Overview of Freescale's Embedded board solutions.

Training & Events

On Demand Training

Simplifying the Complexities
Multicore Processors with C
Single Board Computer Solu

QorIQ Modules Accelerating
Embedded Design Webinar

Events

Freescale Technology Forur

Read More

Advancements in I/O connec
COM Express form factors

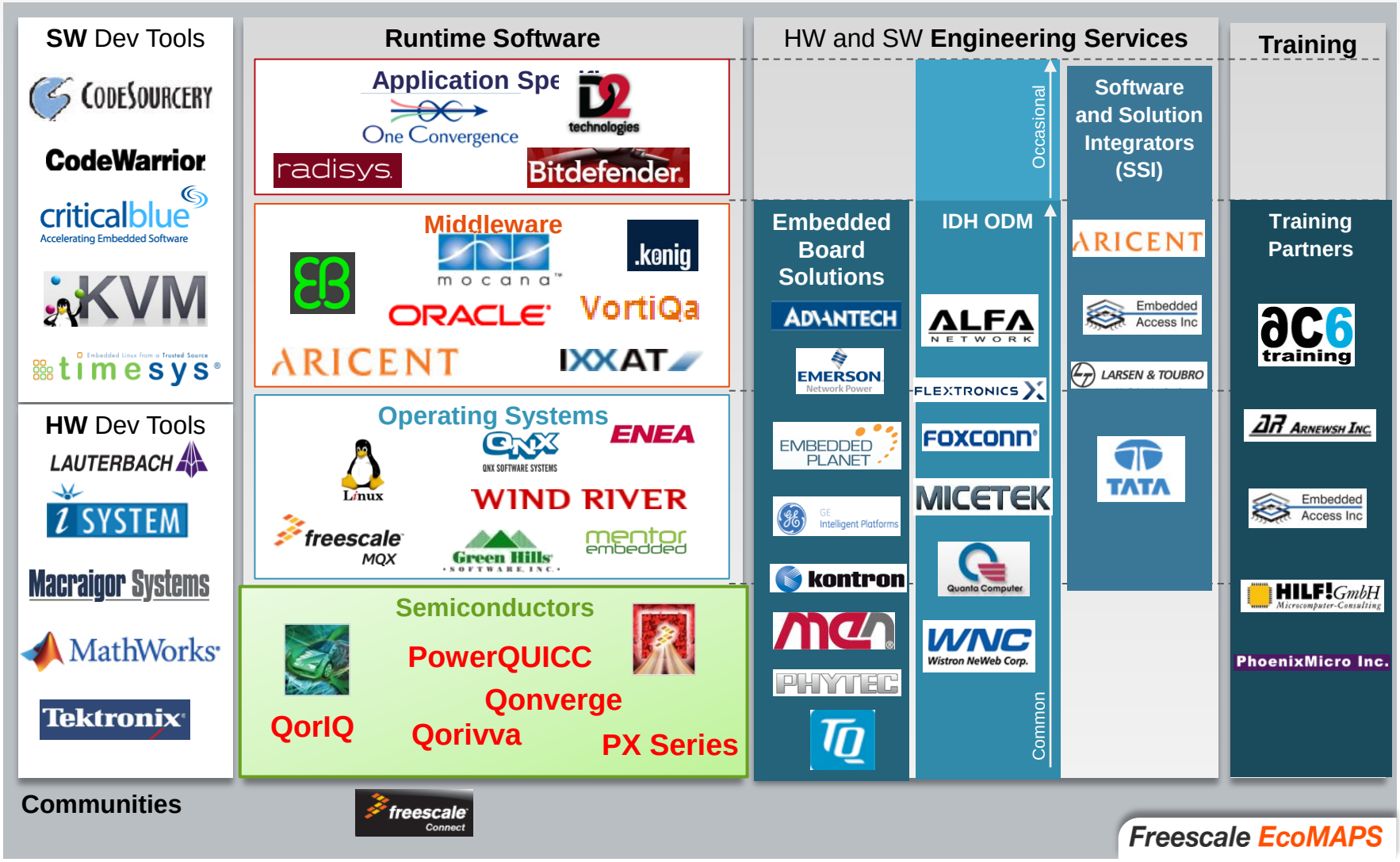
Expanding the COM Express

Connect With Us

Every Connection Matters
Freescale's Glenn Beck dis
the make vs. buy decision

Freescale EcoMAPS

Automotive Consumer Industrial Networking



For more partner options: Freescale.com/partners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