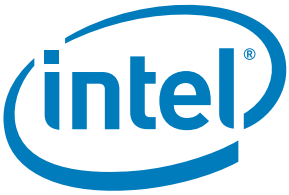


7th and 8th Generation Intel® Processor Family I/O for U/Y Platforms and 10th Generation Intel® Processor Family I/O for Y Platforms

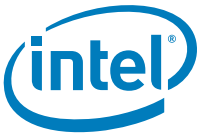
Datasheet - Volume 2 of 2

Supporting 7th Generation Intel® Processor Families for U/Y Platforms, 8th Generation Intel® Processor Family for U Platforms formerly known as Kaby Lake and Kaby Lake Refresh, 8th Generation Intel® Processor Family for Y Platforms, and 10th Generation Intel® Processor Family for Y Platforms formerly known as Amber Lake - 4 Core

August 2019

Revision 005

Document Number: 334659-005



You may not use or facilitate the use of this document in connection with any infringement or other legal analysis concerning Intel products described herein. You agree to grant Intel a non-exclusive, royalty-free license to any patent claim thereafter drafted which includes subject matter disclosed herein.

No license (express or implied, by estoppel or otherwise) to any intellectual property rights is granted by this document.

Intel technologies' features and benefits depend on system configuration and may require enabled hardware, software or service activation. Performance varies depending on system configuration. **No computer system can be absolutely secure.** Check with your system manufacturer or retailer or learn more at **intel.com.**

Intel technologies may require enabled hardware, specific software, or services activation. Check with your system manufacturer or retailer.

The products described may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Intel disclaims all express and implied warranties, including without limitation, the implied warranties of merchantability, fitness for a particular purpose, and non-infringement, as well as any warranty arising from course of performance, course of dealing, or usage in trade.

All information provided here is subject to change without notice. Contact your Intel representative to obtain the latest Intel product specifications and roadmaps

Copies of documents which have an order number and are referenced in this document may be obtained by calling 1-800-548-4725 or visit www.intel.com/design/literature.htm.

Intel, Intel Core, and the Intel logo are trademarks of Intel Corporation in the U.S. and other countries.

*Other names and brands may be claimed as the property of others.

Copyright © 2019, Intel Corporation. All Rights Reserved.

Contents

1 Introduction 65

2 LPC Interface (D31:F0) 66

2.1 LPC Configuration Registers Summary 66

2.1.1 Identifiers (ID)—Offset 0h 66

2.1.2 Device Command (CMD)—Offset 4h 67

2.1.3 Status (STS)—Offset 6h 68

2.1.4 Revision ID (RID)—Offset 8h 69

2.1.5 Class Code (CC)—Offset 9h 69

2.1.6 Header Type (HTYPE)—Offset Eh 70

2.1.7 Sub System Identifiers (SS)—Offset 2Ch 70

2.1.8 Capability List Pointer (CAPP)—Offset 34h 71

2.1.9 Serial IRQ Control (SCNT)—Offset 64h 71

2.1.10 I/O Decode Ranges (IOD)—Offset 80h 72

2.1.11 I/O Enables (IOE)—Offset 82h 73

2.1.12 LPC Generic I/O Range #1 (LGIR1)—Offset 84h 74

2.1.13 LPC Generic I/O Range #2 (LGIR2)—Offset 88h 75

2.1.14 LPC Generic I/O Range #3 (LGIR3)—Offset 8Ch 75

2.1.15 LPC Generic I/O Range #4 (LGIR4)—Offset 90h 75

2.1.16 USB Legacy Keyboard/Mouse Control (ULKMC)—Offset 94h 75

2.1.17 LPC Generic Memory Range (LGMR)—Offset 98h 76

2.1.18 FWH ID Select #1 (FS1)—Offset D0h 77

2.1.19 FWH ID Select #2 (FS2)—Offset D4h 77

2.1.20 BIOS Decode Enable (BDE)—Offset D8h 78

2.1.21 BIOS Control (BC)—Offset DCh 79

2.1.22 PCI Clock Control (PCCTL)—Offset E0h 80

2.2 LPC PCR Registers Summary 82

2.2.1 General Control & Function Disable (GCFD)—Offset 3418h 82

3 Enhanced SPI Interface (D31:F0) 83

3.1 Enhanced SPI (eSPI) Configuration Registers Summary 83

3.1.1 Identifiers (ESPI_DID_VID)—Offset 0h 83

3.1.2 Device Status and Command (ESPI_STS_CMD)—Offset 4h 84

3.1.3 Class Code and Revision ID (ESPI_CC_RID)—Offset 8h 85

3.1.4 BIST, Header Type, Primary Latency Timer, Cache Line Size (ESPI_BIST_HTYPE_PLT_CLS)—Offset Ch 86

3.1.5 Sub System Identifiers (ESPI_SS)—Offset 2Ch 86

3.1.6 Capability List Pointer (ESPI_CAPP)—Offset 34h 87

3.1.7 I/O Decode Ranges and I/O Enables (ESPI_IOD_IOE)—Offset 80h 87

3.1.8 eSPI Generic I/O Range #1 (ESPI_LGIR1)—Offset 84h 89

3.1.9 eSPI Generic I/O Range #2 (ESPI_LGIR2)—Offset 88h 90

3.1.10 eSPI Generic I/O Range #3 (ESPI_LGIR3)—Offset 8Ch 90

3.1.11 eSPI Generic I/O Range #4 (ESPI_LGIR4)—Offset 90h 91

3.1.12 USB Legacy Keyboard/Mouse Control (ESPI_ULKMC)—Offset 94h 92

3.1.13 eSPI Generic Memory Range (ESPI_LGMR)—Offset 98h 93

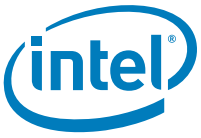
3.1.14 FWH ID Select #1 (ESPI_FS1)—Offset D0h 94

3.1.15 FWH ID Select #2 (ESPI_FS2)—Offset D4h 95

3.1.16 BIOS Decode Enable (ESPI_BDE)—Offset D8h 95

3.1.17 BIOS Control (ESPI_BC)—Offset DCh 96

3.2 eSPI PCR Registers Summary 98



3.2.1 eSPI Slave Configuration and Link Control (SLV_CFG_REG_CTL)—Offset 4000h .. 98
3.2.2 eSPI Slave Configuration Register Data (SLV_CFG_REG_DATA)—Offset 4004h 99
3.2.3 Peripheral Channel Error for Slave 0 (PCERR_SLV0)—Offset 4020h 100
3.2.4 Virtual Wire Channel Error for Channel 0 (VWERR_SLV0)—Offset 4030h 102
3.2.5 Flash Access Channel Error for Slave 0 (FCERR_SLV0)—Offset 4040h 104
3.2.6 Link Error for Slave 0 (LNKERR_SL0)—Offset 4050h 106

4 P2SB Bridge (D31:F1) 108
4.1 P2SB Configuration Registers Summary 108
4.1.1 PCI Identifier (PCIID)—Offset 0h.....109
4.1.2 PCI Command (PCICMD)—Offset 4h 109
4.1.3 Revision ID (PCIRID)—Offset 8h 110
4.1.4 Class Code (PCICC)—Offset 9h 111
4.1.5 PCI Header Type (PCIHTYPE)—Offset Eh 111
4.1.6 Sideband Register Access BAR (SBREG_BAR)—Offset 10h 112
4.1.7 Sideband Register BAR High DWORD (SBREG_BARH)—Offset 14h 112
4.1.8 PCI Subsystem Identifiers (PCIHSS)—Offset 2Ch.....113
4.1.9 VLW Bus:Device:Function (VBDF)—Offset 50h 113
4.1.10 ERROR Bus:Device:Function (EBDF)—Offset 52h.....114
4.1.11 Routing Configuration (RCFG)—Offset 54h.....114
4.1.12 High Performance Event Timer Configuration (HPTC)—Offset 60h 115
4.1.13 IOxAPIC Configuration (IOAC)—Offset 64h 115
4.1.14 IOxAPIC Bus:Device:Function (IBDF)—Offset 6Ch 116
4.1.15 HPET Bus:Device:Function (HBDF)—Offset 70h 117
4.1.16 Sideband Register posted 0 (SBREGPOSTED0)—Offset 80h.....117
4.1.17 Sideband Register posted 1 (SBREGPOSTED1)—Offset 84h.....118
4.1.18 Sideband Register posted 2 (SBREGPOSTED2)—Offset 88h.....118
4.1.19 Sideband Register posted 3 (SBREGPOSTED3)—Offset 8Ch 119
4.1.20 Sideband Register posted 4 (SBREGPOSTED4)—Offset 90h.....119
4.1.21 Sideband Register posted 5 (SBREGPOSTED5)—Offset 94h.....120
4.1.22 Sideband Register posted 6 (SBREGPOSTED6)—Offset 98h.....120
4.1.23 Sideband Register posted 7 (SBREGPOSTED7)—Offset 9Ch 121
4.1.24 Display Bus:Device:Function (DISPBDF)—Offset A0h 121
4.1.25 ICC Register Offsets (ICCOS)—Offset A4h 122
4.1.26 Endpoint Mask 0 (EPMASK0)—Offset B0h 122
4.1.27 Endpoint Mask 1 (EPMASK1)—Offset B4h 123
4.1.28 Endpoint Mask 2 (EPMASK2)—Offset B8h 123
4.1.29 Endpoint Mask 3 (EPMASK3)—Offset BCh 124
4.1.30 Endpoint Mask 4 (EPMASK4)—Offset C0h 124
4.1.31 Endpoint Mask 5 (EPMASK5)—Offset C4h 125
4.1.32 Endpoint Mask 6 (EPMASK6)—Offset C8h 125
4.1.33 Endpoint Mask 7 (EPMASK7)—Offset CCh 126
4.1.34 SBI Address (SBIADDR)—Offset D0h 126
4.1.35 SBI Data (SBIDATA)—Offset D4h 127
4.1.36 SBI Status (SBISTAT)—Offset D8h 127
4.1.37 SBI Routing Identification (SBIRID)—Offset DAh 128
4.1.38 SBI Extended Address (SBIEXTADDR)—Offset DCh.....129
4.1.39 P2SB Control (P2SBC)—Offset E0h 129
4.1.40 Power Control Enable (PCE)—Offset E4h 130

5 PMC Controller (D31:F2) 131
5.1 Power Management Configuration Registers Summary 131
5.1.1 PCI Identifier (PCIID)—Offset 0h.....131
5.1.2 Device Status & Command (PCISTS_PCICMD)—Offset 4h 132
5.1.3 Class Code & Revision ID (PCICC_PCIRID)—Offset 8h 133

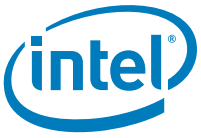
5.1.4 Header Type & Master Latency Timer (PCIHTYPE_PCIMLT)—Offset Ch 133
5.1.5 32-bit Power Management Data Base Address Register (PM_DATA_BAR)—Offset 10h 134
5.1.6 Subsystem Identifiers (PCISID)—Offset 2Ch 135
5.1.7 ACPI Base Address (ABASE)—Offset 40h 135
5.1.8 ACPI Control (ACTL)—Offset 44h 135
5.1.9 PM Base Address (PWRMBASE)—Offset 48h 136
5.1.10 General PM Configuration A (GEN_PMCON_A)—Offset A0h 137
5.1.11 General PM Configuration B (GEN_PMCON_B)—Offset A4h 140
5.1.12 BM_BREAK_EN and Cx State Configuration Register (BM_CX_CNF)—Offset A8h . 142
5.1.13 Extended Test Mode Register 3 (ETR3)—Offset ACh 143
5.2 PMC I/O Based Registers Summary 144
5.2.1 Power Management 1 Enables and Status (PM1_EN_STS)—Offset 0h 145
5.2.2 Power Management 1 Control (PM1_CNT)—Offset 4h 147
5.2.3 Power Management 1 Timer (PM1_TMR)—Offset 8h 148
5.2.4 SMI Control and Enable (SMI_EN)—Offset 30h 149
5.2.5 SMI Status Register (SMI_STS)—Offset 34h 151
5.2.6 General Purpose Event Control (GPE_CTRL)—Offset 40h 153
5.2.7 Device Activity Status Register (DEVACT_STS)—Offset 44h 154
5.2.8 PM2a Control Block (PM2A_CNT_BLK)—Offset 50h 155
5.2.9 Over-Clocking WDT Control (OC_WDT_CTL)—Offset 54h 156
5.2.10 General Purpose Event 0 Status [31:0] (GPE0_STS_31_0)—Offset 80h 157
5.2.11 General Purpose Event 0 Status [63:32] (GPE0_STS_63_32)—Offset 84h 158
5.2.12 General Purpose Event 0 Status [95:64] (GPE0_STS_95_64)—Offset 88h 159
5.2.13 General Purpose Event 0 Status [127:96] (GPE0_STS[127:96])—Offset 8Ch 159
5.2.14 General Purpose Event 0 Enable [31:0] (GPE0_EN_31_0)—Offset 90h 161
5.2.15 General Purpose Event 0 Enable [63:32] (GPE0_EN_63_32)—Offset 94h 162
5.2.16 General Purpose Event 0 Enable [95:64] (GPE0_EN_95_64)—Offset 98h 162
5.2.17 General Purpose Event 0 Enable [127:96] (GPE0_EN[127:96])—Offset 9Ch . 163
5.3 PMC Memory Mapped Registers Summary 165
5.3.1 Wake Alarm Device Timer: AC (WADT_AC)—Offset 0h 167
5.3.2 Wake Alarm Device Timer: DC (WADT_DC)—Offset 4h 167
5.3.3 Wake Alarm Device Expired Timer: AC (WADT_EXP_AC)—Offset 8h 168
5.3.4 Wake Alarm Device Expired Timer: DC (WADT_EXP_DC)—Offset Ch 169
5.3.5 Power and Reset Status (PRSTS)—Offset 10h 170
5.3.6 Chipset Initialization Register 14 (CIR14)—Offset 14h 171
5.3.7 Power Management Configuration Reg 1 (PM_CFG)—Offset 18h 171
5.3.8 Message to PMC (MTPMC)—Offset 20h 175
5.3.9 PCH Power Management Status (PCH_PM_STS2)—Offset 24h 176
5.3.10 S3 Power Gating Policies (S3_PWRGATE_POL)—Offset 28h 177
5.3.11 S4 Power Gating Policies (S4_PWRGATE_POL)—Offset 2Ch 178
5.3.12 S5 Power Gating Policies (S5_PWRGATE_POL)—Offset 30h 179
5.3.13 DeepSx Configuration (DSX_CFG)—Offset 34h 179
5.3.14 Power Management Configuration Reg 2 (PM_CFG2)—Offset 3Ch 181
5.3.15 Chipset Initialization Register 40 (CIR40)—Offset 40h 182
5.3.16 Chipset Initialization Register 44 (CIR44)—Offset 44h 182
5.3.17 Chipset Initialization Register 48 (CIR48)—Offset 48h 183
5.3.18 Chipset Initialization Register 4C (CIR4C)—Offset 4Ch 183
5.3.19 Chipset Initialization Register 50 (CIR50)—Offset 50h 183
5.3.20 Chipset Initialization Register 54 (CIR54)—Offset 54h 183
5.3.21 Chipset Initialization Register 58 (CIR58)—Offset 58h 183
5.3.22 Chipset Initialization Register 60 (CIR60)—Offset 60h 183
5.3.23 Chipset Initialziation Register 68 (CIR68)—Offset 68h 183
5.3.24 Chipset Initialization Register 78 (CIR78)—Offset 78h 183

5.3.25 Chipset Initialization Register 7C (CIR7C)—Offset 7Ch 183
5.3.26 Chipset Initialization Register 80 (CIR80)—Offset 80h 183
5.3.27 Chipset Initialization Register 84 (CIR84)—Offset 84h 183
5.3.28 Chipset Initialization Register 88 (CIR88)—Offset 88h 183
5.3.29 Chipset Initialization Register 8C (CIR8C)—Offset 8Ch 183
5.3.30 Chipset Initialization Register 90 (CIR90)—Offset 90h 184
5.3.31 Chipset Initialization Register 98 (CIR98)—Offset 98h 184
5.3.32 Chipset Initialization Register A0 (CIRA0)—Offset A0h 184
5.3.33 Chipset Initialization Register A4 (CIRA4)—Offset A4h 184
5.3.34 Chipset Initizaliation Register A8 (CIRA8)—Offset A8h 184
5.3.35 Chipset Initizaliation Register AC (CIRAC)—Offset ACh 184
5.3.36 Chipset Initialization Register B0 (CIRB0)—Offset B0h 184
5.3.37 Chipset Initialization Register B4 (CIRB4)—Offset B4h 184
5.3.38 Chipset Initialization Register C0 (CIRC0)—Offset C0h 184
5.3.39 PMSYNC Thermal Power Reporting Configuration (PMSYNC_TPR_CFG)—Offset C4h 184
5.3.40 PM_SYNC Miscellaneous Configuration (PM_SYNC_MISC_CFG)—Offset C8h ... 185
5.3.41 Chipset Initialization Register D0 (CIRD0)—Offset D0h 186
5.3.42 Chipset Initialization Register D4 (CIRD4)—Offset D4h 187
5.3.43 Chipset Initialization Register DC (CIRDC)—Offset DCh 187
5.3.44 Chipset Initialization Register E0 (CIRE0)—Offset E0h 187
5.3.45 Chipset Initialization Register E4 (CIRE4)—Offset E4h 188
5.3.46 Chipset Initializatin Register E8 (CIRE8)—Offset E8h 188
5.3.47 ACPI Timer Control (ACPI_TMR_CTL)—Offset FCh 189
5.3.48 VR Miscellaneous Control (VR_MISC_CTL)—Offset 100h 190
5.3.49 Last TSC Alarm Value[31:0] (TSC_ALARM_LO)—Offset 110h 192
5.3.50 Last TSC Alarm Value[63:32] (TSC_ALARM_HI)—Offset 114h 193
5.3.51 GPIO Configuration (GPIO_CFG)—Offset 120h 193
5.3.52 Global Reset Causes (GBLRST_CAUSE0)—Offset 124h 194
5.3.53 Global Reset Causes Register 1 (GBLRST_CAUSE1)—Offset 128h 197
5.3.54 SLP S0 RESIDENCY (SLP_S0_RES)—Offset 13Ch 198
5.3.55 ModPhy Power Management Configuration 1 (MODPHY_PM_CFG1)—Offset 200h 198
5.3.56 MODPHY Power Management Configuration 2 (MODPHY_PM_CFG2)—Offset 204h 200
5.3.57 MODPHY Power Management Configuration 3 (MODPHY_PM_CFG3)—Offset 208h 200
5.3.58 MODPHY Power Management Configuration 4 (MODPHY_PM_CFG4)—Offset 20Ch 201
5.3.59 Chipset Initialization Register 31C (CIR31C)—Offset 31Ch 202
5.3.60 Chipset Initialization Register 324 (CIR324)—Offset 324h 203
5.3.61 Chipset Initialization Register 328 (CIR328)—Offset 328h 204
5.3.62 Chipset Initialization Register 32C (CIR32C)—Offset 32Ch 204
5.3.63 Clock Source Shutdown Control Reg 2 (CS_SD_CTL2)—Offset 3ECh 204
5.3.64 PFET Enable Ack Register 0 (PPFEAR0)—Offset 590h 205
5.3.65 PFET Enable Ack Register 1 (PPFEAR1)—Offset 594h 207
5.3.66 Host SW PG Control Register 1 (HSWPGCR1)—Offset 5D0h 209
5.3.67 Static PG Function Disable 1 (ST_PG_FDIS1)—Offset 620h 209
5.3.68 Chipset Initialization Register (NST_PG_FDIS_1)—Offset 628h 210
5.3.69 Capability Disable Read Register (FUSE_DIS_RD_2)—Offset 644h 212

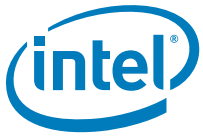
6 Intel® High Definition Audio (Intel® HD Audio) Interface (D31:F3) 214

6.1 Intel® High Definition Audio (D31:F3) PCI Configuration Registers Summary 214
6.1.1 Vendor Identification (VID)—Offset 0h 215
6.1.2 Device ID (DID)—Offset 2h 216
6.1.3 Command (CMD)—Offset 4h 216

6.1.4 Status (STS)—Offset 6h 217
6.1.5 Revision Identification (RID)—Offset 8h 218
6.1.6 Programming Interface (PI)—Offset 9h 218
6.1.7 Sub Class Code (SCC)—Offset Ah 219
6.1.8 Base Class Code (BCC)—Offset Bh 219
6.1.9 Cache Line Size (CLS)—Offset Ch 220
6.1.10 Latency Timer (LT)—Offset Dh 220
6.1.11 Header Type (HTYPE)—Offset Eh 220
6.1.12 Intel HD Audio Base Lower Address (HDALBA)—Offset 10h 221
6.1.13 Intel HD Audio Base Upper Address (HDAUBA)—Offset 14h 222
6.1.14 Shadowed PCI Configuration Lower Base Address (SPCLBA)—Offset 18h 222
6.1.15 Shadowed PCI Configuration Upper Base Address (SPCUBA)—Offset 1Ch 223
6.1.16 Audio DSP Lower Base Address (ADSPLBA)—Offset 20h 223
6.1.17 Audio DSP Upper Base Address (ADSPUBA)—Offset 24h 224
6.1.18 Subsystem Vendor ID (SVID)—Offset 2Ch 224
6.1.19 Subsystem ID (SID)—Offset 2Eh 225
6.1.20 Capability Pointer (CAPPTR)—Offset 34h 225
6.1.21 Interrupt Line (INTLN)—Offset 3Ch 226
6.1.22 Interrupt Pin (INTPN)—Offset 3Dh 226
6.1.23 Power Gating Control (PGCTL)—Offset 44h 227
6.1.24 Clock Gating Control (CGCTL)—Offset 48h 227
6.1.25 PCI Power Management Capability ID (PID)—Offset 50h 229
6.1.26 Power Management Capabilities (PC)—Offset 52h 229
6.1.27 Power Management Control And Status (PCS)—Offset 54h 230
6.1.28 MSI Capability ID (MID)—Offset 60h 231
6.1.29 Message Signal Interrupt Message Control (MMC)—Offset 62h 232
6.1.30 MSI Message Lower Address (MMLA)—Offset 64h 232
6.1.31 MSI Message Upper Address (MMUA)—Offset 68h 233
6.1.32 MSI Message Data (MMD)—Offset 6Ch 233
6.1.33 PCI Express Capability ID (PXID)—Offset 70h 234
6.1.34 PCI Express Capabilities (PXC)—Offset 72h 234
6.1.35 Device Capabilities (DEVCAP)—Offset 74h 235
6.1.36 Device Control (DEVC)—Offset 78h 236
6.1.37 Device Status (DEVS)—Offset 7Ah 237
6.1.38 Extended Mode 3 (SEM3L)—Offset C8h 238
6.1.39 Lower Extended Mode 4 (SEM4L)—Offset D0h 239
6.1.40 Virtual Channel Enhanced Capability Header (VCCAP)—Offset 100h 240
6.1.41 Port VC Capability Register 1 (PVCCAP1)—Offset 104h 241
6.1.42 Port VC Capability Register 2 (PVCCAP2)—Offset 108h 241
6.1.43 Port VC Control Register (PVCCTL)—Offset 10Ch 242
6.1.44 Port VC Status Register (PVCSTS)—Offset 10Eh 242
6.1.45 VC0 Resource Capability Register (VC0CAP)—Offset 110h 243
6.1.46 VC0 Resource Control Register (VC0CTL)—Offset 114h 244
6.1.47 VC0 Resource Status Register (VC0STS)—Offset 11Ah 244
6.1.48 VCi Resource Capability Register (VCiCAP)—Offset 11Ch 245
6.1.49 VCi Resource Control Register (VCiCTL)—Offset 120h 246
6.1.50 VCi Resource Status Register (VCiSTS)—Offset 126h 247
6.1.51 Root Complex Link Declaration Enhanced (RCCAP)—Offset 130h 247
6.1.52 Element Self Description (ESD)—Offset 134h 248
6.1.53 Link 1 Description (L1DESC)—Offset 140h 248
6.1.54 Link 1 Lower Address (L1LADD)—Offset 148h 249
6.1.55 Link 1 Upper Address (L1UADD)—Offset 14Ch 250
6.2 High Definition Audio (D31:F3) Memory Mapped I/O Registers Summary 250
6.2.1 Global Capabilities (GCAP)—Offset 0h 262
6.2.2 Minor Version (VMIN)—Offset 2h 262



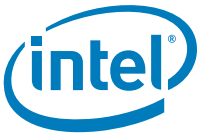
6.2.3 Major Version (VMAJ)—Offset 3h....263
6.2.4 Output Payload Capability (OUTPAY)—Offset 4h....263
6.2.5 Input Payload Capability (INPAY)—Offset 6h....264
6.2.6 Global Control (GCTL)—Offset 8h....264
6.2.7 Wake Enable (WAKEEN)—Offset Ch....265
6.2.8 Wake Status (WAKESTS)—Offset Eh....266
6.2.9 Global Capabilities 2 (GCAP2)—Offset 12h....267
6.2.10 Linked List Capabilities Header (LLCH)—Offset 14h....267
6.2.11 Output Stream Payload Capability (OUTSTRMPAY)—Offset 18h....268
6.2.12 Input Stream Payload Capability (INSTRMPAY)—Offset 1Ah....268
6.2.13 Interrupt Control (INTCTL)—Offset 20h....269
6.2.14 Interrupt Status (INTSTS)—Offset 24h....270
6.2.15 Wall Clock Counter (WALCLK)—Offset 30h....271
6.2.16 Stream Synchronization (SSYNC)—Offset 38h....271
6.2.17 CORB Lower Base Address (CORBLBASE)—Offset 40h....272
6.2.18 CORB Upper Base Address (CORBUBASE)—Offset 44h....273
6.2.19 CORB Write Pointer (CORBWP)—Offset 48h....273
6.2.20 CORB Read Pointer (CORBRP)—Offset 4Ah....274
6.2.21 CORB Control (CORBCTL)—Offset 4Ch....274
6.2.22 CORB Status (CORBSTS)—Offset 4Dh....275
6.2.23 CORB Size (CORBSIZE)—Offset 4Eh....276
6.2.24 RIRB Lower Base Address (RIRBLBASE)—Offset 50h....276
6.2.25 RIRB Upper Base Address (RIRBUBASE)—Offset 54h....277
6.2.26 RIRB Write Pointer (RIRBWP)—Offset 58h....277
6.2.27 Response Interrupt Count (RINTCNT)—Offset 5Ah....278
6.2.28 RIRB Control (RIRBCTL)—Offset 5Ch....278
6.2.29 RIRB Status (RIRBSTS)—Offset 5Dh....279
6.2.30 RIRB Size (RIRBSIZE)—Offset 5Eh....279
6.2.31 Immediate Command (IC)—Offset 60h....280
6.2.32 Immediate Response (IR)—Offset 64h....280
6.2.33 DMA Position Lower Base Address (DPLBASE)—Offset 70h....281
6.2.34 DMA Position Upper Base Address (DPUBASE)—Offset 74h....281
6.2.35 Input/Output Stream Descriptor x Control (ISD0CTL)—Offset 80h....282
6.2.36 Stream Descriptor Status (ISD0STS)—Offset 83h....284
6.2.37 Input/Output Stream Descriptor x Link Position in Buffer (ISD0LPIB)—Offset 84h 285
6.2.38 Input/Output Stream Descriptor x Cyclic Buffer Length (ISD0CBL)—Offset 88h .. 286
6.2.39 Input/Output Stream Descriptor x Last Valid Index (ISD0LVI)—Offset 8Ch ...287
6.2.40 Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD0FIFOW)—Offset 8Eh....287
6.2.41 Input/Output Stream Descriptor x FIFO Size (ISD0FIFOS)—Offset 90h....288
6.2.42 Input/Output Stream Descriptor x Format (ISD0FMT)—Offset 92h....289
6.2.43 Input/Output Stream Descriptor x FIFO Limit (ISD0FIFOL)—Offset 94h....291
6.2.44 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD0BDLPLBA)—Offset 98h....292
6.2.45 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD0BDLPUBA)—Offset 9Ch....293
6.2.46 Input/Output Stream Descriptor x Link Position in Buffer (OSD0LPIB)—Offset 164h....293
6.2.47 Input/Output Stream Descriptor x Cyclic Buffer Length (OSD0CBL)—Offset 168h 294
6.2.48 Input/Output Stream Descriptor x Last Valid Index (OSD0LVI)—Offset 16Ch.294
6.2.49 Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD0FIFOW)—Offset 16Eh....295



6.2.50 Input/Output Stream Descriptor x FIFO Size (OSD0FIFOS)—Offset 170h..... 296
6.2.51 Input/Output Stream Descriptor x Format (OSD0FMT)—Offset 172h..... 296
6.2.52 Input/Output Stream Descriptor x FIFO Limit (OSD0FIFOL)—Offset 174h..... 297
6.2.53 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD0BDLPLBA)—Offset 178h..... 298
6.2.54 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD0BDLPUBA)—Offset 17Ch..... 299
6.2.55 Global Time Synchronization Capture Control (GTSCC2)—Offset 4DCh..... 299
6.2.56 Wall Frame Counter Captured (WALFCC2)—Offset 4E0h..... 300
6.2.57 Time Stamp Counter Captured Lower (TSCCL2)—Offset 4E4h..... 300
6.2.58 Time Stamp Counter Captured Upper (TSCCU2)—Offset 4E8h..... 301
6.2.59 Linear Link Position Frame Offset Captured (LLPFOC2)—Offset 4ECh..... 301
6.2.60 Linear Link Position Captured Lower (LLPCL2)—Offset 4F0h..... 302
6.2.61 Linear Link Position Captured Upper (LLPCU2)—Offset 4F4h..... 302
6.2.62 Global Time Synchronization Capability Header (GTSCH)—Offset 500h..... 303
6.2.63 Global Time Synchronization Capability Declaration (GTSCD)—Offset 504h... 303
6.2.64 Global Time Synchronization Controller Adjust Control (GTSCTLAC)—Offset 50Ch 304
6.2.65 Global Time Synchronization Capture Control (GTSCC0)—Offset 520h..... 305
6.2.66 Wall Frame Counter Captured (WALFCC0)—Offset 524h..... 306
6.2.67 Time Stamp Counter Captured Lower (TSCCL0)—Offset 528h..... 306
6.2.68 Time Stamp Counter Captured Upper (TSCCU0)—Offset 52Ch..... 306
6.2.69 Linear Link Position Frame Offset Captured (LLPFOC0)—Offset 534h..... 307
6.2.70 Linear Link Position Captured Lower (LLPCL0)—Offset 538h..... 307
6.2.71 Linear Link Position Captured Upper (LLPCU0)—Offset 53Ch..... 308
6.2.72 Global Time Synchronization Capture Control (GTSCC1)—Offset 540h..... 308
6.2.73 Wall Frame Counter Captured (WALFCC1)—Offset 544h..... 309
6.2.74 Time Stamp Counter Captured Lower (TSCCL1)—Offset 548h..... 310
6.2.75 Time Stamp Counter Captured Upper (TSCCU1)—Offset 54Ch..... 310
6.2.76 Linear Link Position Frame Offset Captured (LLPFOC1)—Offset 554h..... 310
6.2.77 Linear Link Position Captured Lower (LLPCL1)—Offset 558h..... 311
6.2.78 Linear Link Position Captured Upper (LLPCU1)—Offset 55Ch..... 312
6.2.79 Processing Pipe Capability Header (PPCH)—Offset 800h..... 312
6.2.80 Processing Pipe Control (PPCTL)—Offset 804h..... 313
6.2.81 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC0LLPL)—Offset 810h..... 314
6.2.82 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC0LLPU)—Offset 814h..... 314
6.2.83 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC0LDPL)—Offset 818h..... 315
6.2.84 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC0LDPU)—Offset 81Ch..... 315
6.2.85 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC1LLPL)—Offset 820h..... 316
6.2.86 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC1LLPU)—Offset 824h..... 316
6.2.87 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC1LDPL)—Offset 828h..... 317
6.2.88 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC1LDPU)—Offset 82Ch..... 317
6.2.89 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC2LLPL)—Offset 830h..... 318
6.2.90 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC2LLPU)—Offset 834h..... 318
6.2.91 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC2LDPL)—Offset 838h..... 319

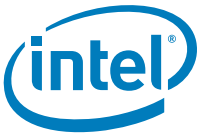
6.2.92 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC2LDPU)—Offset 83Ch 319
6.2.93 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC3LLPL)—Offset 840h 320
6.2.94 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC3LLPU)—Offset 844h 320
6.2.95 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC3LDPL)—Offset 848h 321
6.2.96 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC3LDPU)—Offset 84Ch 321
6.2.97 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC4LLPL)—Offset 850h 322
6.2.98 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC4LLPU)—Offset 854h 322
6.2.99 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC4LDPL)—Offset 858h 323
6.2.100 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC4LDPU)—Offset 85Ch 323
6.2.101 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC5LLPL)—Offset 860h 324
6.2.102 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC5LLPU)—Offset 864h 324
6.2.103 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC5LDPL)—Offset 868h 325
6.2.104 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC5LDPU)—Offset 86Ch 325
6.2.105 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC6LLPL)—Offset 870h 326
6.2.106 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC6LLPU)—Offset 874h 326
6.2.107 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC6LDPL)—Offset 878h 327
6.2.108 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC6LDPU)—Offset 87Ch 327
6.2.109 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC0LLPL)—Offset 880h 328
6.2.110 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC0LLPU)—Offset 884h 328
6.2.111 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC0LDPL)—Offset 888h 329
6.2.112 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC0LDPU)—Offset 88Ch 329
6.2.113 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC1LLPL)—Offset 890h 330
6.2.114 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC1LLPU)—Offset 894h 330
6.2.115 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC1LDPL)—Offset 898h 331
6.2.116 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC1LDPU)—Offset 89Ch 331
6.2.117 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC2LLPL)—Offset 8A0h 332
6.2.118 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC2LLPU)—Offset 8A4h 332
6.2.119 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC2LDPL)—Offset 8A8h 333

6.2.120 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC2LDPU)—Offset 8ACh 333
6.2.121 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC3LLPL)—Offset 8B0h 334
6.2.122 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC3LLPU)—Offset 8B4h 334
6.2.123 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC3LDPL)—Offset 8B8h 335
6.2.124 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC3LDPU)—Offset 8BCh 335
6.2.125 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC4LLPL)—Offset 8C0h 336
6.2.126 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC4LLPU)—Offset 8C4h 336
6.2.127 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC4LDPL)—Offset 8C8h 337
6.2.128 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC4LDPU)—Offset 8CCh 337
6.2.129 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC5LLPL)—Offset 8D0h 338
6.2.130 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC5LLPU)—Offset 8D4h 338
6.2.131 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC5LDPL)—Offset 8D8h 339
6.2.132 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC5LDPU)—Offset 8DCh 339
6.2.133 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC6LLPL)—Offset 8E0h 340
6.2.134 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC6LLPU)—Offset 8E4h 340
6.2.135 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC6LDPL)—Offset 8E8h 341
6.2.136 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC6LDPU)—Offset 8ECh 341
6.2.137 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC7LLPL)—Offset 8F0h 342
6.2.138 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC7LLPU)—Offset 8F4h 342
6.2.139 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC7LDPL)—Offset 8F8h 343
6.2.140 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC7LDPU)—Offset 8FCh 343
6.2.141 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC8LLPL)—Offset 900h 344
6.2.142 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC8LLPU)—Offset 904h 344
6.2.143 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC8LDPL)—Offset 908h 345
6.2.144 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC8LDPU)—Offset 90Ch 345
6.2.145 Input/Output Processing Pipe's Link Connection x Control (IPPLC0CTL)—Offset 910h 346
6.2.146 Input/Output Processing Pipe's Link Connection x Format (IPPLC0FMT)—Offset 914h 347
6.2.147 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC0LLPL)—Offset 918h 348



6.2.148 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC0LLPU)—Offset 91Ch 348
6.2.149 Input/Output Processing Pipe's Link Connection x Control (IPPLC1CTL)—Offset 920h 349
6.2.150 Input/Output Processing Pipe's Link Connection x Format (IPPLC1FMT)—Offset 924h 350
6.2.151 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC1LLPL)—Offset 928h 351
6.2.152 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC1LLPU)—Offset 92Ch 351
6.2.153 Input/Output Processing Pipe's Link Connection x Control (IPPLC2CTL)—Offset 930h 352
6.2.154 Input/Output Processing Pipe's Link Connection x Format (IPPLC2FMT)—Offset 934h 353
6.2.155 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC2LLPL)—Offset 938h 354
6.2.156 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC2LLPU)—Offset 93Ch 354
6.2.157 Input/Output Processing Pipe's Link Connection x Control (IPPLC3CTL)—Offset 940h 355
6.2.158 Input/Output Processing Pipe's Link Connection x Format (IPPLC3FMT)—Offset 944h 356
6.2.159 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC3LLPL)—Offset 948h 357
6.2.160 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC3LLPU)—Offset 94Ch 357
6.2.161 Input/Output Processing Pipe's Link Connection x Control (IPPLC4CTL)—Offset 950h 358
6.2.162 Input/Output Processing Pipe's Link Connection x Format (IPPLC4FMT)—Offset 954h 359
6.2.163 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC4LLPL)—Offset 958h 360
6.2.164 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC4LLPU)—Offset 95Ch 360
6.2.165 Input/Output Processing Pipe's Link Connection x Control (IPPLC5CTL)—Offset 960h 361
6.2.166 Input/Output Processing Pipe's Link Connection x Format (IPPLC5FMT)—Offset 964h 362
6.2.167 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC5LLPL)—Offset 968h 363
6.2.168 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC5LLPU)—Offset 96Ch 363
6.2.169 Input/Output Processing Pipe's Link Connection x Control (IPPLC6CTL)—Offset 970h 364
6.2.170 Input/Output Processing Pipe's Link Connection x Format (IPPLC6FMT)—Offset 974h 365
6.2.171 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC6LLPL)—Offset 978h 366
6.2.172 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC6LLPU)—Offset 97Ch 366
6.2.173 Input/Output Processing Pipe's Link Connection x Control (OPPLC0CTL)—Offset 980h 367
6.2.174 Input/Output Processing Pipe's Link Connection x Format (OPPLC0FMT)—Offset 984h 368
6.2.175 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC0LLPL)—Offset 988h 369

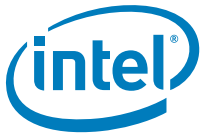
6.2.176 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC0LLPU)—Offset 98Ch 369
6.2.177 Input/Output Processing Pipe's Link Connection x Control (OPPLC1CTL)—Offset 990h 370
6.2.178 Input/Output Processing Pipe's Link Connection x Format (OPPLC1FMT)—Offset 994h 371
6.2.179 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC1LLPL)—Offset 998h 372
6.2.180 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC1LLPU)—Offset 99Ch 372
6.2.181 Input/Output Processing Pipe's Link Connection x Control (OPPLC2CTL)—Offset 9A0h 373
6.2.182 Input/Output Processing Pipe's Link Connection x Format (OPPLC2FMT)—Offset 9A4h 374
6.2.183 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC2LLPL)—Offset 9A8h 375
6.2.184 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC2LLPU)—Offset 9ACh 375
6.2.185 Input/Output Processing Pipe's Link Connection x Control (OPPLC3CTL)—Offset 9B0h 376
6.2.186 Input/Output Processing Pipe's Link Connection x Format (OPPLC3FMT)—Offset 9B4h 377
6.2.187 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC3LLPL)—Offset 9B8h 378
6.2.188 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC3LLPU)—Offset 9BCh 378
6.2.189 Input/Output Processing Pipe's Link Connection x Control (OPPLC4CTL)—Offset 9C0h 379
6.2.190 Input/Output Processing Pipe's Link Connection x Format (OPPLC4FMT)—Offset 9C4h 380
6.2.191 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC4LLPL)—Offset 9C8h 381
6.2.192 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC4LLPU)—Offset 9CCh 381
6.2.193 Input/Output Processing Pipe's Link Connection x Control (OPPLC5CTL)—Offset 9D0h 382
6.2.194 Input/Output Processing Pipe's Link Connection x Format (OPPLC5FMT)—Offset 9D4h 383
6.2.195 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC5LLPL)—Offset 9D8h 384
6.2.196 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC5LLPU)—Offset 9DCh 384
6.2.197 Input/Output Processing Pipe's Link Connection x Control (OPPLC6CTL)—Offset 9E0h 385
6.2.198 Input/Output Processing Pipe's Link Connection x Format (OPPLC6FMT)—Offset 9E4h 386
6.2.199 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC6LLPL)—Offset 9E8h 387
6.2.200 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC6LLPU)—Offset 9ECh 387
6.2.201 Input/Output Processing Pipe's Link Connection x Control (OPPLC7CTL)—Offset 9F0h 388
6.2.202 Input/Output Processing Pipe's Link Connection x Format (OPPLC7FMT)—Offset 9F4h 389
6.2.203 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC7LLPL)—Offset 9F8h 390



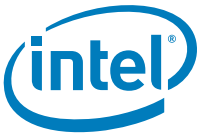
6.2.204 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC7LLPU)—Offset 9FCh 390
6.2.205 Input/Output Processing Pipe's Link Connection x Control (OPPLC8CTL)—Offset A00h 391
6.2.206 Input/Output Processing Pipe's Link Connection x Format (OPPLC8FMT)—Offset A04h 392
6.2.207 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC8LLPL)—Offset A08h 393
6.2.208 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC8LLPU)—Offset A0Ch 393
6.2.209 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC7LLPL)—Offset 4A10h 394
6.2.210 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC7LLPU)—Offset 4A14h 394
6.2.211 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC7LDPL)—Offset 4A18h 395
6.2.212 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC7LDPU)—Offset 4A1Ch 395
6.2.213 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC8LLPL)—Offset 4A20h 396
6.2.214 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC8LLPU)—Offset 4A24h 396
6.2.215 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC8LDPL)—Offset 4A28h 397
6.2.216 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC8LDPU)—Offset 4A2Ch 397
6.2.217 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC9LLPL)—Offset 4A30h 398
6.2.218 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC9LLPU)—Offset 4A34h 398
6.2.219 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC9LDPL)—Offset 4A38h 399
6.2.220 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC9LDPU)—Offset 4A3Ch 399
6.2.221 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC10LLPL)—Offset 4A40h 400
6.2.222 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC10LLPU)—Offset 4A44h 400
6.2.223 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC10LDPL)—Offset 4A48h 401
6.2.224 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC10LDPU)—Offset 4A4Ch 401
6.2.225 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC11LLPL)—Offset 4A50h 402
6.2.226 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC11LLPU)—Offset 4A54h 402
6.2.227 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC11LDPL)—Offset 4A58h 403
6.2.228 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC11LDPU)—Offset 4A5Ch 403
6.2.229 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC12LLPL)—Offset 4A60h 404
6.2.230 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC12LLPU)—Offset 4A64h 404
6.2.231 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC12LDPL)—Offset 4A68h 405

6.2.232 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC12LDPU)—Offset 4A6Ch 405
6.2.233 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC13LLPL)—Offset 4A70h 406
6.2.234 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC13LLPU)—Offset 4A74h 406
6.2.235 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC13LDPL)—Offset 4A78h 407
6.2.236 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC13LDPU)—Offset 4A7Ch 407
6.2.237 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC14LLPL)—Offset 4A80h 408
6.2.238 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC14LLPU)—Offset 4A84h 408
6.2.239 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC14LDPL)—Offset 4A88h 409
6.2.240 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC14LDPU)—Offset 4A8Ch 409
6.2.241 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC9LLPL)—Offset 4A90h 410
6.2.242 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC9LLPU)—Offset 4A94h 410
6.2.243 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC9LDPL)—Offset 4A98h 411
6.2.244 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC9LDPU)—Offset 4A9Ch 411
6.2.245 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC10LLPL)—Offset 4AA0h 412
6.2.246 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC10LLPU)—Offset 4AA4h 412
6.2.247 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC10LDPL)—Offset 4AA8h 413
6.2.248 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC10LDPU)—Offset 4AACh 413
6.2.249 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC11LLPL)—Offset 4AB0h 414
6.2.250 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC11LLPU)—Offset 4AB4h 414
6.2.251 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC11LDPL)—Offset 4AB8h 415
6.2.252 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC11LDPU)—Offset 4ABCh 415
6.2.253 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC12LLPL)—Offset 4AC0h 416
6.2.254 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC12LLPU)—Offset 4AC4h 416
6.2.255 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC12LDPL)—Offset 4AC8h 417
6.2.256 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC12LDPU)—Offset 4ACCh 417
6.2.257 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC13LLPL)—Offset 4AD0h 418
6.2.258 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC13LLPU)—Offset 4AD4h 418
6.2.259 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC13LDPL)—Offset 4AD8h 419

6.2.260 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC13LDPU)—Offset 4ADCh 419
6.2.261 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC14LLPL)—Offset 4AE0h 420
6.2.262 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC14LLPU)—Offset 4AE4h 420
6.2.263 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC14LDPL)—Offset 4AE8h 421
6.2.264 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC14LDPU)—Offset 4AECh 421
6.2.265 Input/Output Processing Pipe's Link Connection x Control (IPPLC7CTL)—Offset 4AF0h 422
6.2.266 Input/Output Processing Pipe's Link Connection x Format (IPPLC7FMT)—Offset 4AF4h 423
6.2.267 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC7LLPL)—Offset 4AF8h 424
6.2.268 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC7LLPU)—Offset 4AFCh 424
6.2.269 Input/Output Processing Pipe's Link Connection x Control (IPPLC8CTL)—Offset 4B00h 425
6.2.270 Input/Output Processing Pipe's Link Connection x Format (IPPLC8FMT)—Offset 4B04h 426
6.2.271 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC8LLPL)—Offset 4B08h 427
6.2.272 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC8LLPU)—Offset 4B0Ch 427
6.2.273 Input/Output Processing Pipe's Link Connection x Control (IPPLC9CTL)—Offset 4B10h 428
6.2.274 Input/Output Processing Pipe's Link Connection x Format (IPPLC9FMT)—Offset 4B14h 429
6.2.275 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC9LLPL)—Offset 4B18h 430
6.2.276 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC9LLPU)—Offset 4B1Ch 430
6.2.277 Input/Output Processing Pipe's Link Connection x Control (IPPLC10CTL)—Offset 4B20h 431
6.2.278 Input/Output Processing Pipe's Link Connection x Format (IPPLC10FMT)—Offset 4B24h 432
6.2.279 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC10LLPL)—Offset 4B28h 433
6.2.280 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC10LLPU)—Offset 4B2Ch 433
6.2.281 Input/Output Processing Pipe's Link Connection x Control (IPPLC11CTL)—Offset 4B30h 434
6.2.282 Input/Output Processing Pipe's Link Connection x Format (IPPLC11FMT)—Offset 4B34h 435
6.2.283 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC11LLPL)—Offset 4B38h 436
6.2.284 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC11LLPU)—Offset 4B3Ch 436
6.2.285 Input/Output Processing Pipe's Link Connection x Control (IPPLC12CTL)—Offset 4B40h 437
6.2.286 Input/Output Processing Pipe's Link Connection x Format (IPPLC12FMT)—Offset 4B44h 438
6.2.287 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC12LLPL)—Offset 4B48h 439



6.2.288 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC12LLPU)—Offset 4B4Ch 439
6.2.289 Input/Output Processing Pipe's Link Connection x Control (IPPLC13CTL)—Offset 4B50h 440
6.2.290 Input/Output Processing Pipe's Link Connection x Format (IPPLC13FMT)—Offset 4B54h 441
6.2.291 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC13LLPL)—Offset 4B58h 442
6.2.292 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC13LLPU)—Offset 4B5Ch 442
6.2.293 Input/Output Processing Pipe's Link Connection x Control (IPPLC14CTL)—Offset 4B60h 443
6.2.294 Input/Output Processing Pipe's Link Connection x Format (IPPLC14FMT)—Offset 4B64h 444
6.2.295 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC14LLPL)—Offset 4B68h 445
6.2.296 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC14LLPU)—Offset 4B6Ch 445
6.2.297 Input/Output Processing Pipe's Link Connection x Control (OPPLC9CTL)—Offset 4B70h 446
6.2.298 Input/Output Processing Pipe's Link Connection x Format (OPPLC9FMT)—Offset 4B74h 447
6.2.299 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC9LLPL)—Offset 4B78h 448
6.2.300 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC9LLPU)—Offset 4B7Ch 448
6.2.301 Input/Output Processing Pipe's Link Connection x Control (OPPLC10CTL)—Offset 4B80h 449
6.2.302 Input/Output Processing Pipe's Link Connection x Format (OPPLC10FMT)—Offset 4B84h 450
6.2.303 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC10LLPL)—Offset 4B88h 451
6.2.304 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC10LLPU)—Offset 4B8Ch 451
6.2.305 Input/Output Processing Pipe's Link Connection x Control (OPPLC11CTL)—Offset 4B90h 452
6.2.306 Input/Output Processing Pipe's Link Connection x Format (OPPLC11FMT)—Offset 4B94h 453
6.2.307 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC11LLPL)—Offset 4B98h 454
6.2.308 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC11LLPU)—Offset 4B9Ch 454
6.2.309 Input/Output Processing Pipe's Link Connection x Control (OPPLC12CTL)—Offset 4BA0h 455
6.2.310 Input/Output Processing Pipe's Link Connection x Format (OPPLC12FMT)—Offset 4BA4h 456
6.2.311 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC12LLPL)—Offset 4BA8h 457
6.2.312 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC12LLPU)—Offset 4BACh 457
6.2.313 Input/Output Processing Pipe's Link Connection x Control (OPPLC13CTL)—Offset 4BB0h 458
6.2.314 Input/Output Processing Pipe's Link Connection x Format (OPPLC13FMT)—Offset 4BB4h 459
6.2.315 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC13LLPL)—Offset 4BB8h 460



6.2.316 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC13LLPU)—Offset 4BBCh 460
6.2.317 Input/Output Processing Pipe's Link Connection x Control (OPPLC14CTL)—Offset 4BC0h 461
6.2.318 Input/Output Processing Pipe's Link Connection x Format (OPPLC14FMT)—Offset 4BC4h 462
6.2.319 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC14LLPL)—Offset 4BC8h 463
6.2.320 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC14LLPU)—Offset 4BCCh 463

7 SMBus Interface (D31:F4) 465

7.1 SMBus Configuration Registers Summary 465
7.1.1 Vendor ID (VID)—Offset 0h 465
7.1.2 Device ID (DID)—Offset 2h 466
7.1.3 Command (CMD)—Offset 4h 466
7.1.4 Device Status (DS)—Offset 6h 467
7.1.5 Revision ID (RID)—Offset 8h 468
7.1.6 Programming Interface (PI)—Offset 9h 468
7.1.7 Sub Class Code (SCC)—Offset Ah 469
7.1.8 Base Class Code (BCC)—Offset Bh 469
7.1.9 SMBus Memory Base Address_31_0 (SMBMBAR_31_0)—Offset 10h 469
7.1.10 SMBus Memory Base Address_63_32 (SMBMBAR_63_32)—Offset 14h 470
7.1.11 SMB Base Address (SBA)—Offset 20h 470
7.1.12 SVID (SVID)—Offset 2Ch 471
7.1.13 SID (SID)—Offset 2Eh 471
7.1.14 Interrupt Line (INTLN)—Offset 3Ch 472
7.1.15 Interrupt Pin (INTPN)—Offset 3Dh 472
7.1.16 Host Configuration (HCFG)—Offset 40h 473
7.1.17 TCO Base Address (TCOBASE)—Offset 50h 473
7.1.18 TCO Control (TCOCTL)—Offset 54h 474
7.1.19 Host SMBus Timing (HTIM)—Offset 64h 475
7.1.20 SMBus Power Gating (SMBSM)—Offset 80h 475
7.2 475
7.3 SMBus I/O and Memory Mapped I/O Registers Summary 475
7.3.1 Host Status Register Address (HSTS)—Offset 0h 476
7.3.2 Host Control Register (HCTL)—Offset 2h 477
7.3.3 Host Command Register (HCMD)—Offset 3h 478
7.3.4 Transmit Slave Address Register (TSA)—Offset 4h 479
7.3.5 Data 0 Register (HD0)—Offset 5h 479
7.3.6 Data 1 Register (HD1)—Offset 6h 480
7.3.7 Host Block Data (HBD)—Offset 7h 480
7.3.8 Packet Error Check Data Register (PEC)—Offset 8h 481
7.3.9 Receive Slave Address Register (RSA)—Offset 9h 481
7.3.10 Slave Data Register (SD)—Offset Ah 482
7.3.11 Auxiliary Status (AUXS)—Offset Ch 482
7.3.12 Auxiliary Control (AUXC)—Offset Dh 483
7.3.13 SMLINK_PIN_CTL Register (SMLC)—Offset Eh 484
7.3.14 SMBUS_PIN_CTL Register (SMBC)—Offset Fh 484
7.3.15 Slave Status Register (SSTS)—Offset 10h 485
7.3.16 Slave Command Register (SCMD)—Offset 11h 486
7.3.17 Notify Device Address Register (NDA)—Offset 14h 486
7.3.18 Notify Data Low Byte Register (NDLB)—Offset 16h 487
7.3.19 Notify Data High Byte Register (NDHB)—Offset 17h 487
7.4 SMBus PCR Registers Summary 488
7.4.1 TCO Configuration (TCOCFG)—Offset 0h 488

7.4.2 General Control (GC)—Offset Ch 489

8 SPI Interface (D31:F5) 490

8.1 SPI Configuration Registers Summary 490
8.1.1 Device ID and Vendor ID (BIOS_SPI_DID_VID)—Offset 0h 490
8.1.2 Status and Command (BIOS_SPI_STS_CMD)—Offset 4h 490
8.1.3 Revision ID (BIOS_SPI_CC_RID)—Offset 8h 492
8.1.4 BIST, Header Type, Latency Timer, Cache Line Size (BIOS_SPI_BIST_HTYPE_LT_CLS)—Offset Ch 492
8.1.5 SPI BAR0 MMIO (BIOS_SPI_BAR0)—Offset 10h 493
8.1.6 SPI Unsupported Request Status (BIOS_SPI_UR_STS_CTL)—Offset D0h 494
8.1.7 BIOS Decode Enable (BIOS_SPI_BDE)—Offset D8h 494
8.1.8 BIOS Control (BIOS_SPI_BC)—Offset DCh 495
8.2 SPI Memory Mapped Registers Summary 497
8.2.1 SPI BIOS MMIO PRI (BIOS_BFPREG)—Offset 0h 498
8.2.2 Hardware Sequencing Flash Status and Control (BIOS_HSFSTS_CTL)—Offset 4h 499
8.2.3 Flash Address (BIOS_FADDR)—Offset 8h 501
8.2.4 Discrete Lock Bits (BIOS_DLOCK)—Offset Ch 501
8.2.5 Flash Data 0 (BIOS_FDATA0)—Offset 10h 503
8.2.6 Flash Data 1 (BIOS_FDATA1)—Offset 14h 503
8.2.7 Flash Data 2 (BIOS_FDATA2)—Offset 18h 504
8.2.8 Flash Data 3 (BIOS_FDATA3)—Offset 1Ch 504
8.2.9 Flash Data 4 (BIOS_FDATA4)—Offset 20h 504
8.2.10 Flash Data 5 (BIOS_FDATA5)—Offset 24h 505
8.2.11 Flash Data 6 (BIOS_FDATA6)—Offset 28h 505
8.2.12 Flash Data 7 (BIOS_FDATA7)—Offset 2Ch 506
8.2.13 Flash Data 8 (BIOS_FDATA8)—Offset 30h 506
8.2.14 Flash Data 9 (BIOS_FDATA9)—Offset 34h 507
8.2.15 Flash Data 10 (BIOS_FDATA10)—Offset 38h 507
8.2.16 Flash Data 11 (BIOS_FDATA11)—Offset 3Ch 507
8.2.17 Flash Data 12 (BIOS_FDATA12)—Offset 40h 508
8.2.18 Flash Data 13 (BIOS_FDATA13)—Offset 44h 508
8.2.19 Flash Data 14 (BIOS_FDATA14)—Offset 48h 509
8.2.20 Flash Data 15 (BIOS_FDATA15)—Offset 4Ch 509
8.2.21 Flash Region Access Permissions (BIOS_FRACC)—Offset 50h 510
8.2.22 Flash Region 0 (BIOS_FREG0)—Offset 54h 510
8.2.23 Flash Region 1 (BIOS_FREG1)—Offset 58h 511
8.2.24 Flash Region 2 (BIOS_FREG2)—Offset 5Ch 512
8.2.25 Flash Region 3 (BIOS_FREG3)—Offset 60h 512
8.2.26 Flash Region 4 (BIOS_FREG4)—Offset 64h 513
8.2.27 Flash Region 5 (BIOS_FREG5)—Offset 68h 513
8.2.28 Flash Protected Range 0 (BIOS_FPR0)—Offset 84h 514
8.2.29 Flash Protected Range 1 (BIOS_FPR1)—Offset 88h 515
8.2.30 Flash Protected Range 2 (BIOS_FPR2)—Offset 8Ch 516
8.2.31 Flash Protected Range 3 (BIOS_FPR3)—Offset 90h 517
8.2.32 Flash Protected Range 4 (BIOS_FPR4)—Offset 94h 518
8.2.33 Global Protected Range 0 (BIOS_GPR0)—Offset 98h 519
8.2.34 Secondary Flash Region Access Permissions (BIOS_SFRACC)—Offset B0h 520
8.2.35 Flash Descriptor Observability Control (BIOS_FDOC)—Offset B4h 521
8.2.36 Flash Descriptor Observability Data (BIOS_FDOD)—Offset B8h 521
8.2.37 Additional Flash Control (BIOS_AFC)—Offset C0h 522
8.2.38 Vendor Specific Component Capabilities for Component 0 (BIOS_SFDP0_VSCC0)—Offset C4h 522

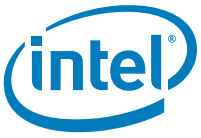
8.2.39 Vendor Specific Component Capabilities for Component 1 (BIOS_SFDP1_VSCC1)—Offset C8h 524
8.2.40 Parameter Table Index (BIOS_PTINX)—Offset CCh 526
8.2.41 Parameter Table Data (BIOS_PTDATA)—Offset D0h 526
8.2.42 SPI Bus Requester Status (BIOS_SBRS)—Offset D4h 527
8.3 BIOS Flash Program Registers Summary 528
8.3.1 Set Strap Msg Lock (SSML)—Offset F0h 528
8.3.2 Set Strap Msg Control (SSMC)—Offset F4h 528
8.3.3 Set Strap Msg Data (SSMD)—Offset F8h 529

9 Integrated GbE (D31:F6) 531
9.1 GbE Configuration Registers Summary 531
9.1.1 GbE Vendor and Device Identification Register (GBE_VID_DID)—Offset 0h ... 531
9.1.2 PCI Command & Status Register (PCICMD_STS)—Offset 4h 532
9.1.3 Revision Identification & Class Code Register (RID_CC)—Offset 8h 534
9.1.4 Cache Line Size Primary Latency Timer & Header Type Register (CLS_PLT_HEADTYP)—Offset Ch 534
9.1.5 Memory Base Address Register A (MBARA)—Offset 10h 535
9.1.6 Subsystem Vendor & Subsytem ID (DMI_CONFIG11)—Offset 2Ch 535
9.1.7 Expansion ROM Base Address Register (ERBA)—Offset 30h 536
9.1.8 Capabilities List Pointer Register (CAPP)—Offset 34h 536
9.1.9 Interrupt Information & Maximum Latency/Minimum GrantRegister (INTR_MLMG)—Offset 3Ch 537
9.1.10 LAN Disable Control (LANDISCTRL)—Offset A0h 537
9.1.11 Lock LAN Disable (LOCKLANDIS)—Offset A4h 538
9.1.12 System Time Control High Register (LTRCAP)—Offset A8h 538
9.1.13 Capabilities List and Power Managment Capabilities Register (CLIST1_PMC)—Offset C8h 539
9.1.14 PCI Power Management Control Status & Data Register (PMCS_DR)—Offset CCh 540
9.1.15 Capabilities List 2 & Message Control Register (CLIST2_MCTL)—Offset D0h .. 541
9.1.16 Message Address Low Register (MADDL)—Offset D4h 542
9.1.17 Message Address High Register (MADDH)—Offset D8h 542
9.1.18 Message Data Register (MDAT)—Offset DCh 543
9.2 GbE Memory Mapped I/O Registers Summary 543
9.2.1 Gigabit Ethernet Capabilities and Status (GBECSR_00)—Offset 0h 544
9.2.2 Gigabit Ethernet Capabilities and Status (GBECSR_18)—Offset 18h 544
9.2.3 Gigabit Ethernet Capabilities and Status (GBECSR_20)—Offset 20h 545
9.2.4 Gigabit Ethernet Capabilities and Status (GBECSR_F00)—Offset F00h 546
9.2.5 Gigabit Ethernet Capabilities and Status F10 (GBECSR_F10)—Offset F10h 546
9.2.6 Gigabit Ethernet Capabilities and Status (GBECSR_5400)—Offset 5400h 547
9.2.7 Gigabit Ethernet Capabilities and Status (GBECSR_5404)—Offset 5404h 547
9.2.8 Gigabit Ethernet Capabilities and Status (GBECSR_5800)—Offset 5800h 548
9.2.9 Gigabit Ethernet Capabilities and Status (GBECSR_5B54)—Offset 5B54h 548

10 Intel® Trace Hub (Intel® TH) 550
10.1 Intel® Trace Huh Configuration Registers Summary 550
10.1.1 Vendor and Device Identification (VID)—Offset 0h 550
10.1.2 Command and Status Register (CMD)—Offset 4h 551
10.1.3 Revision ID (RID)—Offset 8h 552
10.1.4 Header Type (HT)—Offset Ch 552
10.1.5 MTB Low BAR (MTB_LBAR)—Offset 10h 553
10.1.6 MTB Upper BAR (MTB_UBAR)—Offset 14h 554
10.1.7 SW Low BAR (SW_LBAR)—Offset 18h 554
10.1.8 SW Upper BAR (SW_UBAR)—Offset 1Ch 555
10.1.9 RTIT Low BAR (RTIT_LBAR)—Offset 20h 555

10.1.10 RTIT Upper BAR (RTIT_UBAR)—Offset 24h 556
10.1.11 Capabilities Pointer (CAP)—Offset 34h 556
10.1.12 Interrupt Line and Interrupt Pin (INTL)—Offset 3Ch 557
10.1.13 MSI Capability (MSICID)—Offset 40h 557
10.1.14 MSI Lower Message Address (MSILMA)—Offset 44h 558
10.1.15 MSI Upper Message Address (MSIUMA)—Offset 48h 559
10.1.16 MSI Message Data (MSIMD)—Offset 4Ch 559
10.1.17 Device Specific Control and Device Specific Status (NPKDSC)—Offset 80h 560

11 UART Interface (D30:F0/F1 and D25:F0) 561
11.1 UART PCI Configuration Registers Summary 561
11.1.1 Device ID and Vendor ID Register (DEVVENDID)—Offset 0h 561
11.1.2 Status and Command (STATUSCOMMAND)—Offset 4h 562
11.1.3 Revision ID and Class Code (REVCLASSCODE)—Offset 8h 563
11.1.4 Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch 564
11.1.5 Base Address Register (BAR)—Offset 10h 564
11.1.6 Base Address Register High (BAR_HIGH)—Offset 14h 565
11.1.7 Base Address Register 1 (BAR1)—Offset 18h 566
11.1.8 Base Address Register1 High (BAR1_HIGH)—Offset 1Ch 566
11.1.9 Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch 567
11.1.10 Expansion ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h 567
11.1.11 Capabilities Pointer (CAPABILITYPTR)—Offset 34h 568
11.1.12 Interrupt Register (INTERRUPTREG)—Offset 3Ch 569
11.1.13 Power Management Capability ID (POWERCAPID)—Offset 80h 569
11.1.14 PME Control and Status (PMECTRLSTATUS)—Offset 84h 570
11.1.15 PCI Device Idle Capability Record (PCIDEVIDLE_CAP_RECORD)—Offset 90h 571
11.1.16 SW LTR Update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG)—Offset 98h 571
11.1.17 Device IDLE pointer register (DEVICE_IDLE_POINTER_REG)—Offset 9Ch 572
11.1.18 Device PG Config (D0I3_MAX_POW_LAT_PG_CONFIG)—Offset A0h 573
11.2 UART Memory Mapped Registers Summary 574
11.2.1 Receive Buffer Register (RBR)—Offset 0h 574
11.2.2 Transmit Holding Register (THR)—Offset 0h 575
11.2.3 Divisor Latch Low Register (DLL)—Offset 0h 576
11.2.4 Interrupt Enable Register (IER)—Offset 4h 576
11.2.5 Divisor Latch High (DLH)—Offset 4h 577
11.2.6 Interrupt Identification (IIR)—Offset 8h 578
11.2.7 FIFO Control (FCR)—Offset 8h 579
11.2.8 Line Control Register (LCR)—Offset Ch 579
11.2.9 MCR (MCR)—Offset 10h 580
11.2.10 LSR (LSR)—Offset 14h 581
11.2.11 MSR (MSR)—Offset 18h 583
11.2.12 SCR (SCR)—Offset 1Ch 583
11.2.13 SRBR_STHR0 (SRBR_STHR0)—Offset 30h 584
11.2.14 FAR (FAR)—Offset 70h 585
11.2.15 TFR (TFR)—Offset 74h 586
11.2.16 RFW (RFW)—Offset 78h 586
11.2.17 USR (USR)—Offset 7Ch 587
11.2.18 TFL (TFL)—Offset 80h 588
11.2.19 RFL (RFL)—Offset 84h 588
11.2.20 SRR (SRR)—Offset 88h 589
11.2.21 SRTS (SRTS)—Offset 8Ch 589
11.2.22 SBCR (SBCR)—Offset 90h 590
11.2.23 SDMAM (SDMAM)—Offset 94h 591
11.2.24 SFE (SFE)—Offset 98h 591



11.2.25 SRT (SRT)—Offset 9Ch 592
11.2.26 STET (STET)—Offset A0h 593
11.2.27 HTX (HTX)—Offset A4h 593
11.2.28 DMASA (DMASA)—Offset A8h 594
11.2.29 CPR (CPR)—Offset F4h 594
11.3 UART Additional Registers Summary 596
11.3.1 CLOCKS (CLOCKS)—Offset 200h 596
11.3.2 RESETS (RESETS)—Offset 204h 597
11.3.3 Active LTR (ACTIVELTR_VALUE)—Offset 210h 598
11.3.4 IDLE LTR (IDLELTR_VALUE)—Offset 214h 598
11.3.5 reg_TX_BYTE_COUNT (TX_BYTE_COUNT)—Offset 218h 599
11.3.6 reg_RX_BYTE_COUNT (RX_BYTE_COUNT)—Offset 21Ch 600
11.3.7 SW SCRATCH 0 (SW_SCRATCH_0)—Offset 228h 601
11.3.8 reg_CLOCK_GATE (CLOCK_GATE)—Offset 238h 601
11.3.9 reg_REMAP_ADDR_LO (REMAP_ADDR_LO)—Offset 240h 602
11.3.10 reg_REMAP_ADDR_HI (REMAP_ADDR_HI)—Offset 244h 602
11.3.11 reg_DEVIDLE_CONTROL (DEVIDLE_CONTROL)—Offset 24Ch 603
11.3.12 Capabilities (CAPABLITIES)—Offset 2FCh 604
11.3.13 UART Byte Address Control (GEN_REGRW7)—Offset 618h 605
11.4 UART DMA Controller Registers Summary 605
11.4.1 DMA Transfer Source Address Low (SAR_LO0)—Offset 800h 606
11.4.2 DMA Transfer Source Address High (SAR_HI0)—Offset 804h 607
11.4.3 DMA Transfer Destination Address Low (DAR_LO0)—Offset 808h 608
11.4.4 DMA Transfer Destination Address High (DAR_HI0)—Offset 80Ch 609
11.4.5 Linked List Pointer Low (LLP_LO0)—Offset 810h 610
11.4.6 Linked List Pointer High (LLP_HI0)—Offset 814h 611
11.4.7 Control Register Low (CTL_LO0)—Offset 818h 611
11.4.8 Control Register High (CTL_HI0)—Offset 81Ch 613
11.4.9 Source Status (SSTAT0)—Offset 820h 614
11.4.10 Destination Status (DSTAT0)—Offset 828h 615
11.4.11 Source Status Address Low (SSTATAR_LO0)—Offset 830h 615
11.4.12 Source Status Address High (SSTATAR_HI0)—Offset 834h 616
11.4.13 Destination Status Address Low (DSTATAR_LO0)—Offset 838h 617
11.4.14 Destination Status Address High (DSTATAR_HI0)—Offset 83Ch 617
11.4.15 DMA Transfer Configuration Low (CFG_LO0)—Offset 840h 618
11.4.16 DMA Transfer Configuration High (CFG_HI0)—Offset 844h 620
11.4.17 Source Gather (SGR0)—Offset 848h 621
11.4.18 Destination Scatter (DSR0)—Offset 850h 622
11.4.19 Raw Interrupt Status (RawTfr)—Offset AC0h 622
11.4.20 Raw Status for Block Interrupts (RawBlock)—Offset AC8h 623
11.4.21 Raw Status for Source Transaction Interrupts (RawSrcTran)—Offset AD0h 623
11.4.22 Raw Status for Destination Transaction Interrupts (RawDstTran)—Offset AD8h 624
11.4.23 Raw Status for Error Interrupts (RawErr)—Offset AE0h 624
11.4.24 Interrupt Status (StatusTfr)—Offset AE8h 625
11.4.25 Status for Block Interrupts (StatusBlock)—Offset AF0h 625
11.4.26 Status for Source Transaction Interrupts (StatusSrcTran)—Offset AF8h 626
11.4.27 Status for Destination Transaction Interrupts (StatusDstTran)—Offset B00h 626
11.4.28 Status for Error Interrupts (StatusErr)—Offset B08h 627
11.4.29 Mask for Transfer Interrupts (MaskTfr)—Offset B10h 627
11.4.30 Mask for Block Interrupts (MaskBlock)—Offset B18h 628
11.4.31 Mask for Source Transaction Interrupts (MaskSrcTran)—Offset B20h 628
11.4.32 Mask for Destination Transaction Interrupts (MaskDstTran)—Offset B28h 629
11.4.33 Mask for Error Interrupts (MaskErr)—Offset B30h 630
11.4.34 Clear for Transfer Interrupts (ClearTfr)—Offset B38h 630

11.4.35 Clear for Block Interrupts (ClearBlock)—Offset B40h 631
11.4.36 Clear for Source Transaction Interrupts (ClearSrcTran)—Offset B48h 631
11.4.37 Clear for Destination Transaction Interrupts (ClearDstTran)—Offset B50h 632
11.4.38 Clear for Error Interrupts (ClearErr)—Offset B58h 632
11.4.39 Combined Status register (StatusInt)—Offset B60h 633
11.4.40 DMA Configuration (DmaCfgReg)—Offset B98h 633
11.4.41 DMA Channel Enable (ChEnReg)—Offset BA0h 634
11.5 UART PCR Registers Summary 635
11.5.1 PCI Configuration Control (PCICFGCTRL) 635
11.5.2 UART Byte Address Control (PCICFGCTRL) 636

12 Generic SPI Interface (D30:F2) 638
12.1 Generic SPI PCI Configuration Registers Summary 638
12.1.1 Device ID and Vendor ID Register (DEVVENDID)—Offset 0h 638
12.1.2 Status and Command (STATUSCOMMAND)—Offset 4h 639
12.1.3 Revision ID and Class Code (REVCLASSCODE)—Offset 8h 640
12.1.4 Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch 641
12.1.5 Base Address Register (BAR)—Offset 10h 641
12.1.6 Base Address Register High (BAR_HIGH)—Offset 14h 642
12.1.7 Base Address Register 1 (BAR1)—Offset 18h 643
12.1.8 Base Address Register1 High (BAR1_HIGH)—Offset 1Ch 643
12.1.9 Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch 644
12.1.10 Expansion ROM base address (EXPANSION_ROM_BASEADDR)—Offset 30h 644
12.1.11 Capabilities Pointer (CAPABILITYPTR)—Offset 34h 645
12.1.12 Interrupt Register (INTERRUPTREG)—Offset 3Ch 646
12.1.13 PowerManagement Capability ID (POWERCAPID)—Offset 80h 646
12.1.14 PME Control and Status (PMECTRLSTATUS)—Offset 84h 647
12.1.15 PCI Device Idle Capability Record (PCIDEVIDLE_CAP_RECORD)—Offset 90h 648
12.1.16 SW LTR Update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG)—Offset 98h 648
12.1.17 Device IDLE pointer register (DEVICE_IDLE_POINTER_REG)—Offset 9Ch 649
12.1.18 Device PG Config (D0I3_MAX_POW_LAT_PG_CONFIG)—Offset A0h 650
12.2 Generic SPI (GSPI) Memory Mapped Registers Summary 651
12.2.1 SSP (GSPI) Control Register 0 (SSCR0)—Offset 0h 651
12.2.2 SSP (GSPI) Control Register 1 (SSCR1)—Offset 4h 652
12.2.3 SSP (GSPI) Status Register (SSSR)—Offset 8h 653
12.2.4 SSP (GSPI) Data (SSDR)—Offset 10h 654
12.2.5 SSP (GSPI) Time Out (SSTO)—Offset 28h 655
12.2.6 SPI Transmit FIFO (SITF)—Offset 44h 656
12.2.7 SPI Receive FIFO (SIRF)—Offset 48h 657
12.3 Generic SPI (GSPI) Additional Registers Summary 657
12.3.1 CLOCKS (CLOCKS)—Offset 200h 658
12.3.2 RESETS (RESETS)—Offset 204h 658
12.3.3 ACTIVE LTR (ACTIVELTR_VALUE)—Offset 210h 659
12.3.4 Idle LTR Value (IDLELTR_VALUE)—Offset 214h 660
12.3.5 TX Bit Count (TX_BIT_COUNT)—Offset 218h 661
12.3.6 Rx Bit Count (RX_BIT_COUNT)—Offset 21Ch 662
12.3.7 reg_SSP_REG (SSP_REG)—Offset 220h 662
12.3.8 SPI CS CONTROL (SPI_CS_CONTROL)—Offset 224h 663
12.3.9 SW SCRATCH [3:0] (SW_SCRATCH)—Offset 228h 664
12.3.10 Clock Gate (CLOCK_GATE)—Offset 238h 664
12.3.11 Remap Address Low (REMAP_ADDR_LO)—Offset 240h 665
12.3.12 Remap Address High (REMAP_ADDR_HI)—Offset 244h 666
12.3.13 Device Idle Control (DEVIDLE_CONTROL)—Offset 24Ch 666
12.3.14 Delay Rx Clock (DEL_RX_CLK)—Offset 250h 667

12.3.15 Capabilities (CAPABLITIES)—Offset 2FCh 668
12.4 Generic SPI (GSPI) DMA Controller Registers Summary 669
12.4.1 DMA Transfer Source Address Low (SAR_LO0)—Offset 800h 670
12.4.2 DMA Transfer Source Address High (SAR_HI0)—Offset 804h 671
12.4.3 DMA Transfer Destination Address Low (DAR_LO0)—Offset 808h 672
12.4.4 DMA Transfer Destination Address High (DAR_HI0)—Offset 80Ch 673
12.4.5 Linked List Pointer Low (LLP_LO0)—Offset 810h 674
12.4.6 Linked List Pointer High (LLP_HI0)—Offset 814h 675
12.4.7 Control Register Low (CTL_LO0)—Offset 818h 675
12.4.8 Control Register High (CTL_HI0)—Offset 81Ch 677
12.4.9 Source Status (SSTAT0)—Offset 820h 678
12.4.10 Destination Status (DSTAT0)—Offset 828h 679
12.4.11 Source Status Address Low (SSTATAR_LO0)—Offset 830h 679
12.4.12 Source Status Address High (SSTATAR_HI0)—Offset 834h 680
12.4.13 Destination Status Address Low (DSTATAR_LO0)—Offset 838h 681
12.4.14 Destination Status Address High (DSTATAR_HI0)—Offset 83Ch 681
12.4.15 DMA Transfer Configuration Low (CFG_LO0)—Offset 840h 682
12.4.16 DMA Transfer Configuration High (CFG_HI0)—Offset 844h 684
12.4.17 Source Gather (SGR0)—Offset 848h 685
12.4.18 Destination Scatter (DSR0)—Offset 850h 686
12.4.19 Raw Interrupt Status (RawTfr)—Offset AC0h 686
12.4.20 Raw Status for Block Interrupts (RawBlock)—Offset AC8h 687
12.4.21 Raw Status for Source Transaction Interrupts (RawSrcTran)—Offset AD0h 687
12.4.22 Raw Status for Destination Transaction Interrupts (RawDstTran)—Offset AD8h .. 688
12.4.23 Raw Status for Error Interrupts (RawErr)—Offset AE0h 688
12.4.24 Interrupt Status (StatusTfr)—Offset AE8h 689
12.4.25 Status for Block Interrupts (StatusBlock)—Offset AF0h 689
12.4.26 Status for Source Transaction Interrupts (StatusSrcTran)—Offset AF8h 690
12.4.27 Status for Destination Transaction Interrupts (StatusDstTran)—Offset B00h .690
12.4.28 Status for Error Interrupts (StatusErr)—Offset B08h 691
12.4.29 Mask for Transfer Interrupts (MaskTfr)—Offset B10h 691
12.4.30 Mask for Block Interrupts (MaskBlock)—Offset B18h 692
12.4.31 Mask for Source Transaction Interrupts (MaskSrcTran)—Offset B20h 692
12.4.32 Mask for Destination Transaction Interrupts (MaskDstTran)—Offset B28h 693
12.4.33 Mask for Error Interrupts (MaskErr)—Offset B30h 694
12.4.34 Clear for Transfer Interrupts (ClearTfr)—Offset B38h 694
12.4.35 Clear for Block Interrupts (ClearBlock)—Offset B40h 695
12.4.36 Clear for Source Transaction Interrupts (ClearSrcTran)—Offset B48h 695
12.4.37 Clear for Destination Transaction Interrupts (ClearDstTran)—Offset B50h 696
12.4.38 Clear for Error Interrupts (ClearErr)—Offset B58h 696
12.4.39 Combined Status register (StatusInt)—Offset B60h 697
12.4.40 DMA Configuration (DmaCfgReg)—Offset B98h 697
12.4.41 DMA Channel Enable (ChEnReg)—Offset BA0h 698
12.5 Generic SPI (GSPI) PCR Registers Summary 699
12.5.1 PCI Configuration Control (PCICFGCTRL) 699

13 eMMC* Interface (D30:F4) 701
13.1 eMMC* PCI Configuration Registers Summary 701
13.1.1 Device & Vendor ID (VID_DID)—Offset 0h 701
13.1.2 PCI Status & Command (STATUSCOMMAND)—Offset 4h 702
13.1.3 Rev ID & Class Code (REVCLASSCODE)—Offset 8h 703
13.1.4 Carche Line & Latency & Header Type & BIST (CLLATHEADERBIST)—Offset Ch .. 704
13.1.5 Base Address Low (BAR0)—Offset 10h 704

13.1.6 Base Address Register high (BAR0_HIGH)—Offset 14h 705
13.1.7 Base Address Register1 (BAR1)—Offset 18h 706
13.1.8 (BAR1_HIGH)—Offset 1Ch 707
13.1.9 Subsystem Vendor ID (SUBSYSTEMID)—Offset 2Ch 707
13.1.10 (EXPANSION_ROM_BASEADDR)—Offset 30h 708
13.1.11 Capabilities Pointer (CAPABILITYPTR)—Offset 34h 708
13.1.12 (INTERRUPTREG)—Offset 3Ch 709
13.1.13 Power Management Capability ID Register (POWERCAPID)—Offset 80h 710
13.1.14 Power Management Control and Status Register (PMECTRLSTATUS)—Offset 84h 711
13.1.15 (PCIDEVIDLE_CAP_RECORD)—Offset 90h 711
13.1.16 (DEVID_VEND_SPECIFIC_REG)—Offset 94h 712
13.1.17 SW LTR update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG)—Offset 98h 713
13.1.18 Device IDLE Pointer Register (DEVICE_IDLE_POINTER_REG)—Offset 9Ch 713
13.1.19 DOI3 Max Power & PG Config (D0I3_MAX_POW_LAT_PG_CONFIG)—Offset A0h . 714
13.1.20 General Purpose PCI RW Register1 (GEN_REGRW1)—Offset B0h 715
13.1.21 General Purpose PCI RW Register2 (GEN_REGRW2)—Offset B4h 715
13.1.22 General Purpose PCI RW Register3 (GEN_REGRW3)—Offset B8h 716
13.1.23 General Purpose PCI RW Register4 (GEN_REGRW4)—Offset BCh 716
13.1.24 General Input Register (GEN_INPUT_REG)—Offset C0h 717
13.2 eMMC* Memory Mapped Registers Summary 718
13.2.1 SDMA System Address Register/Argument2 Register (sdmasysaddr)—Offset 0h. 719
13.2.2 Block Size Register (blocksize)—Offset 4h 720
13.2.3 Block Count Register (blockcount)—Offset 6h 720
13.2.4 Argument1 Register (argument1)—Offset 8h 721
13.2.5 Transfer Mode Register (transfermode)—Offset Ch 721
13.2.6 Command Register (command)—Offset Eh 722
13.2.7 Response Register (Reponse 0)—Offset 10h 723
13.2.8 Buffer Data Port Register (dataport)—Offset 20h 724
13.2.9 Present State Register (PRESENTSTATE)—Offset 24h 724
13.2.10 Host Control 1 Register (hostcontrol1)—Offset 28h 727
13.2.11 Power Control Register (powercontrol)—Offset 29h 728
13.2.12 Block Gap Control Register (blockgapcontrol)—Offset 2Ah 729
13.2.13 Wakeup Control Register (wakeupcontrol)—Offset 2Bh 730
13.2.14 Clock Control Register (clockcontrol)—Offset 2Ch 731
13.2.15 Timeout Control Register (timeoutcontrol)—Offset 2Eh 732
13.2.16 Software Reset Register (softwarereset)—Offset 2Fh 733
13.2.17 Normal Interrupt Status Register (normalintrsts)—Offset 30h 734
13.2.18 Error Interrupt Status Register (errorintrsts)—Offset 32h 736
13.2.19 Normal Interrupt Status Enable Register (normalintrstsena)—Offset 34h 737
13.2.20 Error Interrupt Status Enable Register (errorintrstsena)—Offset 36h 739
13.2.21 Normal Interrupt Signal Enable Register (normalintrsigena)—Offset 38h 740
13.2.22 Error Interrupt Signal Enable Register (errorintrsigena)—Offset 3Ah 741
13.2.23 Auto CMD12 Error Status Register (autocmderrsts)—Offset 3Ch 742
13.2.24 Host Control2 Register (hostcontrol2)—Offset 3Eh 743
13.2.25 Capabilities Register (capabilities)—Offset 40h 745
13.2.26 Maximum Current Capabilities Register (maxcurrentcap)—Offset 48h 748
13.2.27 Force Event REGISTER for AUTO CMD Error Status (ForceEventforAUTOCMDErrorStatus)—Offset 50h 749
13.2.28 Force Event Register for Error Interrupt Status (forceeventforerrintsts)—Offset 52h 750
13.2.29 ADMA Error Status Register (admaerrsts)—Offset 54h 751

13.2.30 ADMA System Address Register0&1 (admasysaddr01)—Offset 58h 752
13.2.31 ADMA System Address Register1 (admasysaddr2)—Offset 5Ch 753
13.2.32 ADMA System Address Register1 (admasysaddr3)—Offset 5Eh 753
13.2.33 Preset Value Register for Initialization (Preset Value 0)—Offset 60h 754
13.2.34 Preset Value Register for Default Speed (Preset Value 1)—Offset 62h 755
13.2.35 Preset Value Register for High Speed (Preset Value 2)—Offset 64h 755
13.2.36 Preset Value Register for SDR12 (Preset Value 3)—Offset 66h 755
13.2.37 Preset Value Register for SDR25 (Preset Value 4)—Offset 68h 755
13.2.38 Preset Value Register for SDR50 (Preset Value 5)—Offset 6Ah 755
13.2.39 Preset Value Register for SDR104 (Preset Value 6)—Offset 6Ch 755
13.2.40 Preset Value Register for DDR50 (Preset Value 7)—Offset 6Eh 755
13.2.41 Boot Timeout Control Register (boottimeoutcnt)—Offset 70h 756
13.2.42 Slot Interrupt Status Register (slotintrsts)—Offset FCh 756
13.2.43 Host Controller Version Register (hostcontrollerver)—Offset FEh 757
13.3 EMMC Additional Registers Summary 757
13.3.1 Software LTR Value (SW_LTR_val)—Offset 804h 758
13.3.2 Auto LTR Value (Auto_LTR_val)—Offset 808h 759
13.3.3 Capabilities Bypass (Cap_byps)—Offset 810h 759
13.3.4 Capabilities Bypass 1 (Cap_byps_reg1)—Offset 814h 760
13.3.5 (Cap_byps_reg2)—Offset 818h 761
13.3.6 (reg_D0i3)—Offset 81Ch 762
13.3.7 (Tx_CMD_dly)—Offset 820h 763
13.3.8 (Tx_DATA_dly_1)—Offset 824h 764
13.3.9 (Tx_DATA_dly_2)—Offset 828h 764
13.3.10 (Rx_CMD_Data_dly_1)—Offset 82Ch 765
13.3.11 (Rx_Strobe_Ctrl_Path)—Offset 830h 766
13.3.12 (Rx_CMD_Data_dly_2)—Offset 834h 767
13.3.13 (Master_Dll)—Offset 838h 768
13.3.14 (Auto_tuning)—Offset 840h 768

14 SDXC (D30:F6) 770
14.1 SDXC PCI Configuration Registers Summary 770
14.1.1 Device & Vendor ID (DEVVENDID)—Offset 0h 770
14.1.2 PCI Status & Command (STATUSCOMMAND)—Offset 4h 771
14.1.3 Rev ID & Class Code (REVCLASSCODE)—Offset 8h 772
14.1.4 Cache Line & Latency & Header Type & BIST (CLLATHEADERBIST)—Offset Ch 773
14.1.5 Base Address Low (BAR0)—Offset 10h 773
14.1.6 Base Address Register high (BAR0_HIGH)—Offset 14h 774
14.1.7 Base Address Register1 (BAR1)—Offset 18h 775
14.1.8 (BAR1_HIGH)—Offset 1Ch 775
14.1.9 Subsystem Vendor ID (SUBSYSTEMID)—Offset 2Ch 776
14.1.10 (EXPANSION_ROM_BASEADDR)—Offset 30h 776
14.1.11 Capabilities Pointer (CAPABILITYPTR)—Offset 34h 777
14.1.12 (INTERRUPTREG)—Offset 3Ch 778
14.1.13 Power Management Capability ID Register (POWERCAPID)—Offset 80h 778
14.1.14 Power Management Control and Status Register (PMECTRLSTATUS)—Offset 84h 779
14.1.15 (PCIDEVIDLE_CAP_RECORD)—Offset 90h 780
14.1.16 (DEVID_VEND_SPECIFIC_REG)—Offset 94h 781
14.1.17 SW LTR update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG)—Offset 98h 781
14.1.18 Device IDLE Pointer Register (DEVICE_IDLE_POINTER_REG)—Offset 9Ch 782
14.1.19 DOI3 Max Power & PG Config (D0I3_MAX_POW_LAT_PG_CONFIG)—Offset A0h .. 783

14.1.20 General Purpose PCI RW Register1 (GEN_REGRW1)—Offset B0h 784
14.1.21 General Purpose PCI RW Register2 (GEN_REGRW2)—Offset B4h 784
14.1.22 General Purpose PCI RW Register3 (GEN_REGRW3)—Offset B8h 785
14.1.23 General Purpose PCI RW Register4 (GEN_REGRW4)—Offset BCh 785
14.1.24 General Input Register (GEN_INPUT_REG)—Offset C0h 786
14.2 SDXC Memory Mapped Registers Summary 786
14.2.1 SDMA System Address Register/Argument2 Register (sdmasysaddr)—Offset 0h. 788
14.2.2 Block Size Register (blocksize)—Offset 4h 788
14.2.3 Block Count Register (blockcount)—Offset 6h 789
14.2.4 Argument1 Register (argument1)—Offset 8h 790
14.2.5 Transfer Mode Register (transfermode)—Offset Ch 791
14.2.6 Command Register (command)—Offset Eh 791
14.2.7 Response Register (Response 0)—Offset 10h 793
14.2.8 Buffer Data Port Register (dataport)—Offset 20h 793
14.2.9 Present State Register (presentstate)—Offset 24h 794
14.2.10 Host Control1 Register (hostcontrol1)—Offset 28h 797
14.2.11 PowerControl Register (powercontrol)—Offset 29h 798
14.2.12 Block Gap Control Register (blockgapcontrol)—Offset 2Ah 799
14.2.13 Wakeup Control Register (wakeupcontrol)—Offset 2Bh 800
14.2.14 Clock Control Register (clockcontrol)—Offset 2Ch 801
14.2.15 Timeout Control Register (timeoutcontrol)—Offset 2Eh 802
14.2.16 Software Reset Register (softwarereset)—Offset 2Fh 803
14.2.17 Normal Interrupt Status Register (normalintrsts)—Offset 30h 804
14.2.18 Error Interrupt Status (errorintrsts)—Offset 32h 806
14.2.19 Normal Interrupt Status Enable Register (normalintrstsena)—Offset 34h 807
14.2.20 Error Interrupt Status Enable Register (errorintrstsena)—Offset 36h 808
14.2.21 Normal Interrupt Signal Enable Register (normalintrsigena)—Offset 38h 810
14.2.22 Error Interrupt Signal Enable Register (errorintrsigena)—Offset 3Ah 811
14.2.23 Auto CMD12 Error Status Register (autocmderrsts)—Offset 3Ch 812
14.2.24 Host Control 2 Register (hostcontrol2)—Offset 3Eh 813
14.2.25 Capabilities Register (capabilities)—Offset 40h 815
14.2.26 Maximum Current Capabilities Register (maxcurrentcap)—Offset 48h 817
14.2.27 Force Event REGISTER for AUTO CMD Error Status (ForceEventforAUTOCMDErrorStatus)—Offset 50h 818
14.2.28 Force Event Register for Error Interrupt Status (forceeventforerrintsts)—Offset 52h 819
14.2.29 ADMA Error Status Register (admaerrsts)—Offset 54h 820
14.2.30 ADMA System Address Register0&1 (admasysaddr01)—Offset 58h 821
14.2.31 ADMA System Address Register1 (admasysaddr2)—Offset 5Ch 822
14.2.32 ADMA System Address Register1 (admasysaddr3)—Offset 5Eh 822
14.2.33 Preset Value Register for Initialization (Preset Value 0)—Offset 60h 823
14.2.34 Preset Value Register for Default Speed (Preset Value 1)—Offset 62h 824
14.2.35 Preset Value Register for High Speed (presetvalue2)—Offset 64h 824
14.2.36 Preset Value Register for SDR12 (presetvalue3)—Offset 66h 824
14.2.37 Preset Value Register for SDR25 (presetvalue4)—Offset 68h 824
14.2.38 Preset Value Register for SDR50 (presetvalue5)—Offset 6Ah 824
14.2.39 Preset Value Register for SDR104 (presetvalue6)—Offset 6Ch 824
14.2.40 Preset Value Register for DDR50 (presetvalue7)—Offset 6Eh 824
14.2.41 Slot Interrupt Status Register (slotintrsts)—Offset FCh 824
14.2.42 Host Controller Version Register (hostcontrollerver)—Offset FEh 825
14.3 SDXC Additional Registers Summary 826
14.3.1 Software LTR Value (SW_LTR_val)—Offset 804h 826
14.3.2 Auto LTR Value (Auto_LTR_val)—Offset 808h 827
14.3.3 Capabilities Bypass (Cap_byps)—Offset 810h 828

14.3.4 (Cap_byps_reg1)—Offset 814h 828
14.3.5 (Cap_byps_reg2)—Offset 818h 830
14.3.6 (reg_D0i3)—Offset 81Ch 831
14.3.7 (Tx_CMD_dly)—Offset 820h 832
14.3.8 (Tx_DATA_dly_1)—Offset 824h 832
14.3.9 (Tx_DATA_dly_2)—Offset 828h 833
14.3.10 (Rx_CMD_Data_dly_1)—Offset 82Ch 834
14.3.11 (Rx_Strobe_Ctrl_Path)—Offset 830h 835
14.3.12 (Rx_CMD_Data_dly_2)—Offset 834h 835
14.3.13 (Master_Dll)—Offset 838h 836
14.3.14 (Auto_tuning)—Offset 840h 837

15 PCI Express* (PCIe*) Interface (D29:F0–F7, D28:F0–F7 and D27:F0–F3) 839

15.1 PCI Express* Port Configuration Registers Summary 839
15.1.1 Identifiers (ID)—Offset 0h 841
15.1.2 Device Command; Primary Status (CMD_PSTS)—Offset 4h 841
15.1.3 Revision ID;Class Code (RID_CC)—Offset 8h 843
15.1.4 Cache Line Size; Primary Latency Timer; Header Type (CLS_PLT_HTYPE)—Offset Ch 844
15.1.5 Bus Numbers; Secondary Latency Timer (BNUM_SLT)—Offset 18h 844
15.1.6 I/O Base and Limit; Secondary Status (IOBL_SSTS)—Offset 1Ch 845
15.1.7 Memory Base and Limit (MBL)—Offset 20h 846
15.1.8 Prefetchable Memory Base and Limit (PMBL)—Offset 24h 847
15.1.9 Prefetchable Memory Base Upper 32 Bits (PMBU32)—Offset 28h 847
15.1.10 Prefetchable Memory Limit Upper 32 Bits (PMLU32)—Offset 2Ch 848
15.1.11 Capabilities List Pointer (CAPP)—Offset 34h 848
15.1.12 Interrupt Information; Bridge Control (INTR_BCTRL)—Offset 3Ch 849
15.1.13 Capabilities List; PCI Express Capabilities (CLIST_XCAP)—Offset 40h 850
15.1.14 Device Capabilities (DCAP)—Offset 44h 851
15.1.15 Device Control; Device Status (DCTL_DSTS)—Offset 48h 852
15.1.16 Link Capabilities (LCAP)—Offset 4Ch 854
15.1.17 Link Control; Link Status (LCTL_LSTS)—Offset 50h 855
15.1.18 Slot Capabilities (SLCAP)—Offset 54h 857
15.1.19 Slot Control; Slot Status (SLCTL_SLSTS)—Offset 58h 858
15.1.20 Root Control (RCTL)—Offset 5Ch 860
15.1.21 Root Status (RSTS)—Offset 60h 860
15.1.22 Device Capabilities 2 (DCAP2)—Offset 64h 861
15.1.23 Device Control 2; Device Status 2 (DCTL2_DSTS2)—Offset 68h 862
15.1.24 Link Capabilities 2 (LCAP2)—Offset 6Ch 863
15.1.25 Link Control 2; Link Status 2 (LCTL2_LSTS2)—Offset 70h 864
15.1.26 Message Signaled Interrupt Identifiers; Message Signaled Interrupt Message Control (MID_MC)—Offset 80h 867
15.1.27 Message Signaled Interrupt Message Address (MA)—Offset 84h 867
15.1.28 Message Signaled Interrupt Message Data (MD)—Offset 88h 868
15.1.29 Subsystem Vendor Capability (SVCAP)—Offset 90h 868
15.1.30 Subsystem Vendor IDs (SVID)—Offset 94h 869
15.1.31 Power Management Capability; PCI Power Management Capabilities (PMCAP_PMC)—Offset A0h 870
15.1.32 PCI Power Management Control And Status (PMCS)—Offset A4h 870
15.1.33 Miscellaneous Port Configuration 2 (MPC2)—Offset D4h 872
15.1.34 Miscellaneous Port Configuration (MPC)—Offset D8h 872
15.1.35 SMI / SCI Status (SMSCS)—Offset DCh 874
15.1.36 IOSF Primary Control And Status (IPCS)—Offset F0h 875
15.1.37 Additional Configuration 1 (STRPFUSECFG)—Offset FCh 875
15.1.38 Advanced Error Extended Reporting Capability Header (AECH)—Offset 100h 877

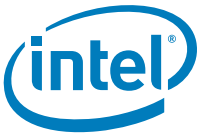
15.1.39 Uncorrectable Error Status (UES)—Offset 104h 878
15.1.40 Uncorrectable Error Mask (UEM)—Offset 108h 879
15.1.41 Uncorrectable Error Severity (UEV)—Offset 10Ch 880
15.1.42 Correctable Error Status (CES)—Offset 110h 881
15.1.43 Correctable Error Mask (CEM)—Offset 114h 882
15.1.44 Advanced Error Capabilities and Control (AECC)—Offset 118h 883
15.1.45 Root Error Command (REC)—Offset 12Ch 884
15.1.46 Root Error Status (RES)—Offset 130h 884
15.1.47 Error Source Identification (ESID)—Offset 134h 885
15.1.48 ACS Capability Register (ACSCAPR)—Offset 144h 886
15.1.49 ACS Control Register (ACSCTLR)—Offset 148h 887
15.1.50 L1 Sub-States Extended Capability Header (L1SECH)—Offset 200h 888
15.1.51 L1 Sub-States Capabilities (L1SCAP)—Offset 204h 889
15.1.52 L1 Sub-States Control 1 (L1SCTL1)—Offset 208h 890
15.1.53 L1 Sub-States Control 2 (L1SCTL2)—Offset 20Ch 891
15.1.54 Secondary PCI Express Extended Capability Header (SPEECH)—Offset 220h 892
15.1.55 Link Control 3 (LCTL3)—Offset 224h 893
15.1.56 Lane 0 and Lane 1 Equalization Control (L01EC)—Offset 22Ch 894
15.1.57 Lane 2 and Lane 3 Equalization Control (L23EC)—Offset 230h 895
15.1.58 PCI Express Configuration (PCIEDBG)—Offset 324h 896
15.1.59 PCI Express Additional Link Control (PCIEALC)—Offset 338h 897
15.1.60 Additional Configuration 2 (LTROVR)—Offset 400h 898
15.1.61 Additional Configuration 3 (LTROVR2)—Offset 404h 898
15.1.62 Additional Configuration 4 (PCIEPMECTL)—Offset 420h 898
15.1.63 Equalization Configuration 1 (EQCFG1)—Offset 450h 898
15.1.64 Remote Transmitter Preset/Coefficient List 1 (RTPCL1)—Offset 454h 899
15.1.65 Remote Transmitter Preset/Coefficient List 2 (RTPCL2) (RTPCL2)—Offset 458h 900

16 I2C Interface (D25:F1/F2, D21:F0/F1/F2/F3) 901
16.1 I^2C PCI Configuration Registers Summary 901
16.1.1 Device ID and Vendor ID Register (DEVVENDID)—Offset 0h 901
16.1.2 Status and Command (STATUSCOMMAND)—Offset 4h 902
16.1.3 Revision ID and Class Code (REVCLASSCODE)—Offset 8h 903
16.1.4 Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch 903
16.1.5 Base Address Register (BAR)—Offset 10h 904
16.1.6 Base Address Register High (BAR_HIGH)—Offset 14h 905
16.1.7 Base Address Register 1 (BAR1)—Offset 18h 905
16.1.8 Base Address Register1 High (BAR1_HIGH)—Offset 1Ch 906
16.1.9 Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch 907
16.1.10 Expansion ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h 907
16.1.11 Capabilities Pointer (CAPABILITYPTR)—Offset 34h 908
16.1.12 Interrupt Register (INTERRUPTREG)—Offset 3Ch 908
16.1.13 Power Management Capability ID (POWERCAPID)—Offset 80h 909
16.1.14 PME Control and Status (PMECTRLSTATUS)—Offset 84h 910
16.1.15 PCI Device Idle Capability Record (PCIDEVIDLE_CAP_RECORD)—Offset 90h 910
16.1.16 SW LTR Update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG)—Offset 98h 911
16.1.17 Device IDLE pointer register (DEVICE_IDLE_POINTER_REG)—Offset 9Ch 912
16.1.18 Device PG Config (D0I3_MAX_POW_LAT_PG_CONFIG)—Offset A0h 912
16.2 I^2C Memory Mapped Registers Summary 913
16.2.1 I2C Control (IC_CON)—Offset 0h 914
16.2.2 I2C Target Address (IC_TAR)—Offset 4h 916
16.2.3 I2C High Speed Master Mode Code Address (IC_HS_MADDR)—Offset Ch 917

16.2.4 I2C Rx/Tx Data Buffer and Command (IC_DATA_CMD)—Offset 10h 917
16.2.5 Standard Speed I2C Clock SCL High Count (IC_SS_SCL_HCNT)—Offset 14h .918
16.2.6 Standard Speed I2C Clock SCL Low Count (IC_SS_SCL_LCNT)—Offset 18h ..919
16.2.7 Fast Speed I2C Clock SCL High Count (IC_FS_SCL_HCNT)—Offset 1Ch 920
16.2.8 Fast Speed I2C Clock SCL Low Count (IC_FS_SCL_LCNT)—Offset 20h.....920
16.2.9 I2C Interrupt Status (IC_INTR_STAT)—Offset 2Ch 921
16.2.10 I2C Interrupt Mask (IC_INTR_MASK)—Offset 30h.....922
16.2.11 I2C Raw Interrupt Status (IC_RAW_INTR_STAT)—Offset 34h.....923
16.2.12 I2C Receive FIFO Threshold (IC_RX_TL)—Offset 38h 924
16.2.13 I2C Transmit FIFO Threshold (IC_TX_TL)—Offset 3Ch.....925
16.2.14 Clear Combined and Individual Interrupt (IC_CLR_INTR)—Offset 40h 925
16.2.15 Clear RX_UNDER Interrupt (IC_CLR_RX_UNDER)—Offset 44h 926
16.2.16 Clear RX_OVER Interrupt (IC_CLR_RX_OVER)—Offset 48h 926
16.2.17 Clear TX_OVER Interrupt (IC_CLR_TX_OVER)—Offset 4Ch.....927
16.2.18 Clear RD_REQ Interrupt (IC_CLR_RD_REQ)—Offset 50h.....927
16.2.19 Clear TX_ABRT Interrupt (IC_CLR_TX_ABRT)—Offset 54h 928
16.2.20 Clear RX_DONE Interrupt (IC_CLR_RX_DONE)—Offset 58h 928
16.2.21 Clear ACTIVITY Interrupt (IC_CLR_ACTIVITY)—Offset 5Ch 929
16.2.22 Clear STOP_DET Interrupt (IC_CLR_STOP_DET)—Offset 60h 930
16.2.23 Clear START_DET Interrupt (IC_CLR_START_DET)—Offset 64h 930
16.2.24 Clear GEN_CALL Interrupt (IC_CLR_GEN_CALL)—Offset 68h.....931
16.2.25 I2C Enable (IC_ENABLE)—Offset 6Ch 931
16.2.26 I2C Status (IC_STATUS)—Offset 70h.....932
16.2.27 I2C Transmit FIFO Level (IC_TXFLR)—Offset 74h 933
16.2.28 I2C Receive FIFO Level (IC_RXFLR)—Offset 78h.....933
16.2.29 I2C SDA Hold Time Length (IC_SDA_HOLD)—Offset 7Ch.....934
16.2.30 I2C Transmit Abort Source (IC_TX_ABRT_SOURCE)—Offset 80h 934
16.2.31 DMA Control (IC_DMA_CR)—Offset 88h 936
16.2.32 DMA Transmit Data Level (IC_DMA_TDLR)—Offset 8Ch.....937
16.2.33 I2C Receive Data Level (IC_DMA_RDLR)—Offset 90h.....937
16.2.34 I2C ACK General Call (IC_ACK_GENERAL_CALL)—Offset 98h 938
16.2.35 I2C Enable Status (IC_ENABLE_STATUS)—Offset 9Ch.....938
16.2.36 I2C SS and FS Spike Suppression Limit (IC_FS_SPKLEN)—Offset A0h 939
16.2.37 Clear RESTART_DET Interrupt (IC_CLR_RESTRART_DET)—Offset A8h.....940
16.3 I2C Additional Registers Summary.....940
16.3.1 Soft Reset (RESETS)—Offset 204h 941
16.3.2 Active LTR (ACTIVELTR_VALUE)—Offset 210h.....941
16.3.3 Idle LTR (IDLELTR_VALUE)—Offset 214h.....942
16.3.4 TX Ack Count (TX_ACK_COUNT)—Offset 218h 943
16.3.5 RX ACK Count (RX_BYTE_COUNT)—Offset 21Ch.....944
16.3.6 Interrupt Status for Tx Complete (TX_COMPLETE_INTR_STAT)—Offset 220h 945
16.3.7 Tx Complete Interrupt Clear (TX_COMPLETE_INTR_CLR)—Offset 224h.....945
16.3.8 SW Scratch Register 0 (SW_SCRATCH_0)—Offset 228h 946
16.3.9 SW Scratch Register 1 (SW_SCRATCH_1)—Offset 22Ch 946
16.3.10 SW Scratch Register 2 (SW_SCRATCH_2)—Offset 230h 947
16.3.11 SW Scratch Register 3 (SW_SCRATCH_3)—Offset 234h 947
16.3.12 Clock Gate (CLOCK_GATE)—Offset 238h 948
16.3.13 Remap Address Low (REMAP_ADDR_LO)—Offset 240h.....948
16.3.14 Remap Address High (REMAP_ADDR_HI)—Offset 244h 949
16.3.15 Device Control (DEVIDLE_CONTROL)—Offset 24Ch.....949
16.3.16 Capabilities (CAPABLITIES)—Offset 2FCh 950
16.4 I2C DMA Controller Registers Summary 951
16.4.1 DMA Transfer Source Address Low (SAR_LO0)—Offset 800h 952
16.4.2 DMA Transfer Source Address High (SAR_HI0)—Offset 804h.....953
16.4.3 DMA Transfer Destination Address Low (DAR_LO0)—Offset 808h.....954

16.4.4 DMA Transfer Destination Address High (DAR_HI0)—Offset 80Ch 955
16.4.5 Linked List Pointer Low (LLP_LO0)—Offset 810h 956
16.4.6 Linked List Pointer High (LLP_HI0)—Offset 814h 957
16.4.7 Control Register Low (CTL_LO0)—Offset 818h 957
16.4.8 Control Register High (CTL_HI0)—Offset 81Ch 959
16.4.9 Source Status (SSTAT0)—Offset 820h 960
16.4.10 Destination Status (DSTAT0)—Offset 828h 961
16.4.11 Source Status Address Low (SSTATAR_LO0)—Offset 830h 961
16.4.12 Source Status Address High (SSTATAR_HI0)—Offset 834h 962
16.4.13 Destination Status Address Low (DSTATAR_LO0)—Offset 838h 963
16.4.14 Destination Status Address High (DSTATAR_HI0)—Offset 83Ch 963
16.4.15 DMA Transfer Configuration Low (CFG_LO0)—Offset 840h 964
16.4.16 DMA Transfer Configuration High (CFG_HI0)—Offset 844h 965
16.4.17 Source Gather (SGR0)—Offset 848h 966
16.4.18 Destination Scatter (DSR0)—Offset 850h 967
16.4.19 Raw Interrupt Status (RawTfr)—Offset AC0h 968
16.4.20 Raw Status for Block Interrupts (RawBlock)—Offset AC8h 968
16.4.21 Raw Status for Source Transaction Interrupts (RawSrcTran)—Offset AD0h ... 969
16.4.22 Raw Status for Destination Transaction Interrupts (RawDstTran)—Offset AD8h .. 969
16.4.23 Raw Status for Error Interrupts (RawErr)—Offset AE0h 970
16.4.24 Interrupt Status (StatusTfr)—Offset AE8h 971
16.4.25 Status for Block Interrupts (StatusBlock)—Offset AF0h 971
16.4.26 Status for Source Transaction Interrupts (StatusSrcTran)—Offset AF8h 972
16.4.27 Status for Destination Transaction Interrupts (StatusDstTran)—Offset B00h . 972
16.4.28 Status for Error Interrupts (StatusErr)—Offset B08h 973
16.4.29 Mask for Transfer Interrupts (MaskTfr)—Offset B10h 973
16.4.30 Mask for Block Interrupts (MaskBlock)—Offset B18h 974
16.4.31 Mask for Source Transaction Interrupts (MaskSrcTran)—Offset B20h 975
16.4.32 Mask for Destination Transaction Interrupts (MaskDstTran)—Offset B28h 975
16.4.33 Mask for Error Interrupts (MaskErr)—Offset B30h 976
16.4.34 Clear for Transfer Interrupts (ClearTfr)—Offset B38h 977
16.4.35 Clear for Block Interrupts (ClearBlock)—Offset B40h 977
16.4.36 Clear for Source Transaction Interrupts (ClearSrcTran)—Offset B48h 978
16.4.37 Clear for Destination Transaction Interrupts (ClearDstTran)—Offset B50h 978
16.4.38 Clear for Error Interrupts (ClearErr)—Offset B58h 978
16.4.39 Combined Status register (StatusInt)—Offset B60h 979
16.4.40 DMA Configuration (DmaCfgReg)—Offset B98h 980
16.4.41 DMA Channel Enable (ChEnReg)—Offset BA0h 980
16.5 I^2C PCR Registers Summary 981
16.5.1 PCI Configuration Control (PCICFGCTRL) 981
16.6 982

17 SATA Interface (D23: F0) 983
17.1 SATA Configuration Registers Summary 983
17.1.1 Identifiers (ID)—Offset 0h 984
17.1.2 Command (CMD)—Offset 4h 984
17.1.3 Device Status (STS)—Offset 6h 985
17.1.4 Revision ID (RID)—Offset 8h 986
17.1.5 Programming Interface (PI)—Offset 9h 987
17.1.6 Class Code (CC)—Offset Ah 987
17.1.7 Cache Line Size (CLS)—Offset Ch 988
17.1.8 Master Latency Timer (MLT)—Offset Dh 988
17.1.9 Header Type (HTYPE)—Offset Eh 989
17.1.10 MSI-X Table Base Address (MXTBA)—Offset 10h 989



17.1.11 MXP Base Address (MXPBA)—Offset 14h 990
17.1.12 AHCI Index Data Pair Base Address (AIDPBA)—Offset 20h 991
17.1.13 AHCI Base Address (ABAR)—Offset 24h 991
17.1.14 Sub System Identifiers (SS)—Offset 2Ch 992
17.1.15 Capabilities Pointer (CAP)—Offset 34h 993
17.1.16 Interrupt Information (INTR)—Offset 3Ch 993
17.1.17 PCI Power Management Capability ID (PID)—Offset 70h 994
17.1.18 PCI Power Management Capabilities (PC)—Offset 72h 994
17.1.19 PCI Power Management Control and Status (PMCS)—Offset 74h 995
17.1.20 Message Signaled Interrupt Identifier (MID)—Offset 80h 996
17.1.21 Message Signaled Interrupt Message Control (MC)—Offset 82h 996
17.1.22 Message Signaled Interrupt Message Address (MA)—Offset 84h 997
17.1.23 Message Signaled Interrupt Message Data (MD)—Offset 88h 998
17.1.24 Port Mapping Register (MAP)—Offset 90h 998
17.1.25 Port Control and Status (PCS)—Offset 92h 999
17.1.26 SATA Clock Gating Control Register (SCLKGC)—Offset 94h 1001
17.1.27 SATA General Configuration (SATAGC)—Offset 9Ch 1001
17.1.28 SATA Initialization Register Index (SIRI)—Offset A0h 1004
17.1.29 SATA Initialization Register Data (SIRD)—Offset A4h 1005
17.1.30 Serial ATA Capability Register 0 (SATACR0)—Offset A8h 1005
17.1.31 Serial ATA Capability Register 1 (SATACR1)—Offset ACh 1006
17.1.32 Scratch Pad (SP)—Offset C0h 1007
17.1.33 MSI-X Identifiers (MXID)—Offset D0h 1007
17.1.34 MSI-X Message Control (MXC)—Offset D2h 1008
17.1.35 MSI-X Table Offset / Table BIR (MXT)—Offset D4h 1009
17.1.36 MSI-X PBA Offset / PBA BIR (MXP)—Offset D8h 1009
17.1.37 BIST FIS Control/Status (BFCS)—Offset E0h 1010
17.1.38 BIST FIS Transmit Data 1 (BFTD1)—Offset E4h 1011
17.1.39 BIST FIS Transmit Data 2 (BFTD2)—Offset E8h 1011
17.2 SATA ABAR Registers Summary 1012
17.2.1 HBA Capabilities (GHC_CAP)—Offset 0h 1014
17.2.2 Global HBA Control (GHC)—Offset 4h 1015
17.2.3 Interrupt Status Register (IS)—Offset 8h 1017
17.2.4 Ports Implemented (GHC_PI)—Offset Ch 1017
17.2.5 AHCI Version (VS)—Offset 10h 1018
17.2.6 Enclosure Management Location (EM_LOC)—Offset 1Ch 1019
17.2.7 Enclosure Management Control (EM_CTL)—Offset 20h 1019
17.2.8 HBA Capabilities Extended (GHC_CAP2)—Offset 24h 1020
17.2.9 Vendor Specific (VSP)—Offset A0h 1021
17.2.10 Vendor Specific Capabilities Register (VS_CAP)—Offset A4h 1022
17.2.11 RAID Platform ID (RPID)—Offset C0h 1023
17.2.12 Premium Feature Block (PFB)—Offset C4h 1023
17.2.13 SW Feature Mask (SFM)—Offset C8h 1024
17.2.14 Port 0 Command List Base Address (P0CLB)—Offset 100h 1025
17.2.15 Port 0 Command List Base Address Upper 32-bits (P0CLBU)—Offset 104h 1026
17.2.16 Port 0 FIS Base Address (P0FB)—Offset 108h 1026
17.2.17 Port 0 FIS Base Address Upper 32-bits (P0FBU)—Offset 10Ch 1027
17.2.18 Port 0 Interrupt Status (P0IS)—Offset 110h 1027
17.2.19 Port 0 Interrupt Enable (P0IE)—Offset 114h 1029
17.2.20 Port 0 Command (P0CMD)—Offset 118h 1030
17.2.21 Port 0 Task File Data (P0TFD)—Offset 120h 1033
17.2.22 Port 0 Signature (P0SIG)—Offset 124h 1034
17.2.23 Port 0 Serial ATA Status (P0SSTS)—Offset 128h 1034
17.2.24 Port 0 Serial ATA Control (P0SCTL)—Offset 12Ch 1036
17.2.25 Port 0 Serial ATA Error (P0SERR)—Offset 130h 1038

17.2.26 Port 0 Serial ATA Active (P0SACT)—Offset 134h 1040
17.2.27 Port 0 Command Issue (P0CI)—Offset 138h 1041
17.2.28 Port 0 Device Sleep (P0DEVSLP)—Offset 144h 1041
17.2.29 Port 1 Command List Base Address (P1CLB)—Offset 180h 1043
17.2.30 Port 1 Command List Base Address Upper 32-bits (P1CLBU)—Offset 184h .. 1043
17.2.31 Port 1 FIS Base Address (P1FB)—Offset 188h 1043
17.2.32 Port 1 FIS Base Address Upper 32-bits (P1FBU)—Offset 18Ch 1043
17.2.33 Port 1 Interrupt Status (P1IS)—Offset 190h 1043
17.2.34 Port 1 Interrupt Enable (P1IE)—Offset 194h 1043
17.2.35 Port 1 Command (P1CMD)—Offset 198h 1043
17.2.36 Port 1 Task File Data (P1TFD)—Offset 1A0h 1043
17.2.37 Port 1 Signature (P1SIG)—Offset 1A4h 1043
17.2.38 Port 1 Serial ATA Status (P1SSTS)—Offset 1A8h 1043
17.2.39 Port 1 Serial ATA Control (P1SCTL)—Offset 1ACh 1043
17.2.40 Port 1 Serial ATA Error (P1SERR)—Offset 1B0h 1043
17.2.41 Port 1 Serial ATA Active (P1SACT)—Offset 1B4h 1044
17.2.42 Port 1 Command Issue (P1CI)—Offset 1B8h 1044
17.2.43 Port 1 Device Sleep (P1DEVSLP)—Offset 1C4h 1044
17.2.44 Port 2 Command List Base Address (P2CLB)—Offset 200h 1044
17.2.45 Port 2 Command List Base Address Upper 32-bits (P2CLBU)—Offset 204h .. 1044
17.2.46 Port 2 FIS Base Address (P2FB)—Offset 208h 1044
17.2.47 Port 2 FIS Base Address Upper 32-bits (P2FBU)—Offset 20Ch 1044
17.2.48 Port 2 Interrupt Status (P2IS)—Offset 210h 1044
17.2.49 Port 2 Interrupt Enable (P2IE)—Offset 214h 1044
17.2.50 Port 2 Command (P2CMD)—Offset 218h 1044
17.2.51 Port 2 Task File Data (P2TFD)—Offset 220h 1044
17.2.52 Port 2 Signature (P2SIG)—Offset 224h 1044
17.2.53 Port 2 Serial ATA Status (P2SSTS)—Offset 228h 1045
17.2.54 Port 2 Serial ATA Control (P2SCTL)—Offset 22Ch 1045
17.2.55 Port 2 Serial ATA Error (P2SERR)—Offset 230h 1045
17.2.56 Port 2 Serial ATA Active (P2SACT)—Offset 234h 1045
17.2.57 Port 2 Command Issue (P2CI)—Offset 238h 1045
17.2.58 Port 2 Device Sleep (P2DEVSLP)—Offset 244h 1045
17.3 SATA AIDP Registers Summary 1045
17.3.1 AHCI Index Register (INDEX)—Offset 10h 1045
17.3.2 AHCI Data Register (DATA)—Offset 14h 1046
17.4 SATA MXPBA Registers Summary 1047
17.4.1 MSI-X Pending Bit Array QW 0 (MXPQW0_DW0)—Offset 0h 1047
17.5 SATA MXTBA Registers Summary 1048
17.5.1 MSI-X Table Entries 0 Message Lower Address (MXTE0MLA)—Offset 0h 1048
17.5.2 MSI-X Table Entries 0 Message Upper Address (MXTE0MUA)—Offset 4h 1048
17.5.3 MSI-X Table Entries 0 Message Data (MXTE0MD)—Offset 8h 1049
17.5.4 MSI-X Table Entries 0 Vector Control (MXTE0VC)—Offset Ch 1049
17.6 SATA Initialization (SIR) Index Registers Summary 1050
17.6.1 SATA MPHY Dynamic Power Gating Enable—Offset 50h 1050
17.6.2 Squelch Circuit Disable—Offset 54h 1051

18 Intel® Management Engine Interface (Intel® MEI) (D22:F0, D22:F1, and D22:F4) 1052
18.1 Intel® Management Engine Interface Configuration Registers Summary 1052
18.1.1 Identifiers (HECI1_ID)—Offset 0h 1053
18.1.2 Command (HECI1_CMD)—Offset 4h 1053
18.1.3 Status (HECI1_STS)—Offset 6h 1054
18.1.4 Revision ID and Class Code (HECI1_RID_CC)—Offset 8h 1055
18.1.5 Cache Line Size (HECI1_CLS)—Offset Ch 1056

18.1.6 Master Latency Timer (HECI1_MLT)—Offset Dh 1056
18.1.7 Header Type (HECI1_HTYPE)—Offset Eh 1057
18.1.8 Built In Self-Test (HECI1_BIST)—Offset Fh 1057
18.1.9 HECI MMIO Base Address Low (HECI1_MMIO_MBAR_LO)—Offset 10h 1057
18.1.10 HECI MMIO Base Address High (HECI1_MMIO_MBAR_HI)—Offset 14h 1058
18.1.11 Sub System Identifiers (HECI1_SS)—Offset 2Ch 1058
18.1.12 Capabilities Pointer (HECI1_CAP)—Offset 34h 1059
18.1.13 Interrupt Information (HECI1_INTR)—Offset 3Ch 1059
18.1.14 Minimum Grant (HECI1_MGNT)—Offset 3Eh 1060
18.1.15 Maximum Latency (HECI1_MLAT)—Offset 3Fh 1060
18.1.16 Host Firmware Status Register 1 (HFSTS1)—Offset 40h 1061
18.1.17 Host Firmware Status Register 2 (HFSTS2)—Offset 48h 1061
18.1.18 Host General Status (HECI1_H_GS1)—Offset 4Ch 1061
18.1.19 PCI Power Management Capability ID (HECI1_PID)—Offset 50h 1062
18.1.20 PCI Power Management Capabilities (HECI1_PC)—Offset 52h 1062
18.1.21 PCI Power Management Control and Status (HECI1_PMCS)—Offset 54h 1063
18.1.22 Host Firmware Status Register 3 (HFSTS3)—Offset 60h 1064
18.1.23 Host Firmware Status Register 4 (HFSTS4)—Offset 64h 1064
18.1.24 Host Firmware Status Register 5 (HFSTS5)—Offset 68h 1065
18.1.25 Host Firmware Status Register 6 (HFSTS6)—Offset 6Ch 1065
18.1.26 Host General Status 2 (HECI1_H_GS2)—Offset 70h 1065
18.1.27 Host General Status 3 (HECI1_H_GS3)—Offset 74h 1066
18.1.28 Message Signaled Interrupt Identifiers (HECI1_MID)—Offset 8Ch 1066
18.1.29 Message Signaled Interrupt Message Control (HECI1_MC)—Offset 8Eh 1067
18.1.30 Message Signaled Interrupt Message Address (HECI1_MA)—Offset 90h 1067
18.1.31 Message Signaled Interrupt Upper Address (HECI1_MUA)—Offset 94h 1068
18.1.32 Message Signaled Interrupt Message Data (HECI1_MD)—Offset 98h 1068
18.1.33 HECI Interrupt Delivery Mode (HECI1_HIDM)—Offset A0h 1069
18.2 Intel® MEI MMIO Registers Summary 1069
18.2.1 D0i3 Control (HECI1_D0I3C)—Offset 800h 1069

19 IDE Redirect (IDE-R) (D22:F2) 1071
19.1 IDE Redirect PCI Configuration (D22:F2) Registers Summary 1071
19.1.1 Device ID and Vendor ID (IDE_HOST_DID_VID)—Offset 0h 1071
19.1.2 Status and Command (IDE_HOST_STS_CMD)—Offset 4h 1072
19.1.3 Class Code and Revision ID (IDE_HOST_CC_RID)—Offset 8h 1074
19.1.4 BIST, Header Type, Latency Timer, and Cache Line Size (IDE_HOST_BIST_HTYPE_LT_CLS)—Offset Ch 1074
19.1.5 IDE Primary Command Block IO BAR (IDE_HOST_PCMDIOBAR)—Offset 10h 1075
19.1.6 IDE Primary Control Block IO BAR (IDE_HOST_PCTLIOBAR)—Offset 14h 1075
19.1.7 IDE Secondary Command Block IO BAR (IDE_HOST_SCMDIOBAR)—Offset 18h .. 1076
19.1.8 IDE Secondary Control Block IO BAR (IDE_HOST_SCTLIOBAR)—Offset 1Ch 1077
19.1.9 IDE Bus Master Block IO BAR (IDE_HOST_BMIOBAR)—Offset 20h 1077
19.1.10 Subsystem ID and Subsystem Vendor ID (IDE_HOST_SID_SVID)—Offset 2Ch ... 1078
19.1.11 Capabilities List Pointer (IDE_HOST_CAPP)—Offset 34h 1078
19.1.12 Maximum Latency, Minimum Grant, Interrupt Pin and Interrupt Line (IDE_HOST_MAXL_MING_INTP_INTL)—Offset 3Ch 1079
19.1.13 MSI Message Control, Next Pointer and Capability ID (IDE_HOST_MSIMC_MSINP_MSICID)—Offset 40h 1080
19.1.14 MSI Message Address (IDE_HOST_MSIMA)—Offset 44h 1080
19.1.15 MSI Message Upper Address (IDE_HOST_MSIMUA)—Offset 48h 1081
19.1.16 MSI Message Data (IDE_HOST_MSIMD)—Offset 4Ch 1081
19.1.17 Power Management Capabilities, Next Pointer and Capability ID (IDE_HOST_PMCAP_PMNP_PMCID)—Offset 50h 1082

19.1.18 Power Management Data, Control/Status Register Bridge Support Extensions, Control and Status (IDE_HOST_PMD_PMCSRBSE_PMCSR)—Offset 54h 1083

20 Keyboard and Text (KT) (D22:F3) 1085
20.1 Serial Port for Remote Keyboard and Text (KT) (D22:F3) Registers Summary 1085
20.1.1 Device ID and Vendor ID (KT_HOST_DID_VID)—Offset 0h 1085
20.1.2 Status and Command (KT_HOST_STS_CMD)—Offset 4h 1086
20.1.3 Class Code and Revision ID (KT_HOST_CC_RID)—Offset 8h 1088
20.1.4 BIST, Header Type, Latency Timer, and Cache Line Size (KT_HOST_BIST_HTYPE_LT_CLS)—Offset Ch 1089
20.1.5 KT IO BAR (KT_HOST_IOBAR)—Offset 10h 1089
20.1.6 KT Memory BAR (KT_HOST_MEMBAR)—Offset 14h 1090
20.1.7 Cardbus CIS Pointer (KT_HOST_CCP)—Offset 28h 1090
20.1.8 Subsystem ID and Subsystem Vendor ID (KT_HOST_SID_SVID)—Offset 2Ch 1091
20.1.9 Expansion ROM Base Address (KT_HOST_XRBAR)—Offset 30h 1091
20.1.10 Capabilities List Pointer (KT_HOST_CAPP)—Offset 34h 1092
20.1.11 Maximum Latency, Minimum Grant, Interrupt Pin and Interrupt Line (KT_HOST_MAXL_MING_INTP_INTL)—Offset 3Ch 1092
20.1.12 MSI Message Control, Next Pointer and Capability ID (KT_HOST_MSIMC_MSINP_MSICID)—Offset 40h 1093
20.1.13 MSI Message Address (KT_HOST_MSIMA)—Offset 44h 1094
20.1.14 MSI Message Upper Address (KT_HOST_MSIMUA)—Offset 48h 1094
20.1.15 MSI Message Data (KT_HOST_MSIMD)—Offset 4Ch 1095
20.1.16 Power Management Capabilities, Next Pointer and Capability ID (KT_HOST_PMCAP_PMNP_PMCID)—Offset 50h 1095
20.1.17 Power Management Data, Control/Status Register Bridge Support Extensions, Control and Status (KT_HOST_PMD_PMCSRBSE_PMCSR)—Offset 54h 1096
20.2 Keyboard and Text (KT) Additional Configuration Registers Summary 1098
20.2.1 Power Management Control and Status (KT_CSXE_PMD_PMCSRBSE_PMCSR)—Offset 54h 1098

21 USB Interface (D20: F0) 1099
21.1 xHCI Configuration Registers Summary 1099
21.1.1 Vendor ID (VID)—Offset 0h 1100
21.1.2 Device ID (DID)—Offset 2h 1100
21.1.3 Command (CMD)—Offset 4h 1101
21.1.4 Device Status (STS)—Offset 6h 1102
21.1.5 Revision ID (RID)—Offset 8h 1103
21.1.6 Programming Interface (PI)—Offset 9h 1103
21.1.7 Sub Class Code (SCC)—Offset Ah 1104
21.1.8 Base Class Code (BCC)—Offset Bh 1104
21.1.9 Master Latency Timer (MLT)—Offset Dh 1105
21.1.10 Header Type (HT)—Offset Eh 1105
21.1.11 Memory Base Address (MBAR)—Offset 10h 1105
21.1.12 USB Subsystem Vendor ID (SSVID)—Offset 2Ch 1106
21.1.13 USB Subsystem ID (SSID)—Offset 2Eh 1107
21.1.14 Capabilities Pointer (CAP_PTR)—Offset 34h 1107
21.1.15 Interrupt Line (ILINE)—Offset 3Ch 1108
21.1.16 Interrupt Pin (IPIN)—Offset 3Dh 1108
21.1.17 XHC System Bus Configuration 1 (XHCC1)—Offset 40h 1108
21.1.18 XHC System Bus Configuration 2 (XHCC2)—Offset 44h 1110
21.1.19 Clock Gating (XHCLKGTEN)—Offset 50h 1113
21.1.20 Audio Time Synchronization (AUDSYNC)—Offset 58h 1116
21.1.21 Serial Bus Release Number (SBRN)—Offset 60h 1117
21.1.22 Frame Length Adjustment (FLADJ)—Offset 61h 1118

21.1.23 Best Effort Service Latency (BESL)—Offset 62h 1119
21.1.24 PCI Power Management Capability ID (PM_CID)—Offset 70h 1119
21.1.25 Next Item Pointer #1 (PM_NEXT)—Offset 71h 1120
21.1.26 Power Management Capabilities (PM_CAP)—Offset 72h 1120
21.1.27 Power Management Control/Status (PM_CS)—Offset 74h 1121
21.1.28 Message Signaled Interrupt CID (MSI_CID)—Offset 80h 1122
21.1.29 Next item pointer (MSI_NEXT)—Offset 81h 1123
21.1.30 Message Signaled Interrupt Message Control (MSI_MCTL)—Offset 82h 1123
21.1.31 Message Signaled Interrupt Message Address (MSI_MAD)—Offset 84h 1124
21.1.32 Message Signaled Interrupt Upper Address (MSI_MUAD)—Offset 88h 1125
21.1.33 Message Signaled Interrupt Message Data (MSI_MD)—Offset 8Ch 1125
21.1.34 Vendor Specific Header (VSHDR)—Offset 94h 1126
21.1.35 Power Control Enable (PCE_REG)—Offset A2h 1127
21.1.36 High Speed Configuration 2 (HSCFG2)—Offset A4h 1127
21.1.37 XHCI USB2 Overcurrent Pin Mapping N (U2OCM)—Offset B0h 1129
21.1.38 XHCI USB3 Overcurrent Pin Mapping N (U3OCM)—Offset D0h 1130
21.2 xHCI Memory Mapped Registers Summary 1131
21.2.1 Capability Registers Length (CAPLENGTH)—Offset 0h 1134
21.2.2 Host Controller Interface Version Number (HCIVERSION)—Offset 2h 1134
21.2.3 Structural Parameters 1 (HCSPARAMS1)—Offset 4h 1135
21.2.4 Structural Parameters 2 (HCSPARAMS2)—Offset 8h 1136
21.2.5 Structural Parameters 3 (HCSPARAMS3)—Offset Ch 1137
21.2.6 Capability Parameters (HCCPARAMS)—Offset 10h 1137
21.2.7 Doorbell Offset (DBOFF)—Offset 14h 1139
21.2.8 Runtime Register Space Offset (RTSOFF)—Offset 18h 1139
21.2.9 USB Command (USBCMD)—Offset 80h 1140
21.2.10 USB Status (USBSTS)—Offset 84h 1142
21.2.11 Page Size (PAGESIZE)—Offset 88h 1144
21.2.12 Device Notification Control (DNCTRL)—Offset 94h 1145
21.2.13 Command Ring Low (CRCR_LO)—Offset 98h 1146
21.2.14 Command Ring High (CRCR_HI)—Offset 9Ch 1147
21.2.15 Device Context Base Address Array Pointer Low (DCBAAP_LO)—Offset B0h 1148
21.2.16 Device Context Base Address Array Pointer High (DCBAAP_HI)—Offset B4h 1149
21.2.17 Port N Status and Control USB2 (PORTSCN)—Offset 480h 1149
21.2.18 Port Power Management Status and Control USB2 (PORTPMSCN)—Offset 484h .. 1153
21.2.19 Port N Hardware LPM Control Register (PORTHLPMCN)—Offset 48Ch 1155
21.2.20 Port Status and Control USB3 (PORTSCXUSB3)—Offset 540h 1156
21.2.21 Port Power Management Status and Control USB3 (PORTPMSCX)—Offset 544h .. 1159
21.2.22 USB3 Port X Link Info (PORTLIX)—Offset 548h 1160
21.2.23 Microframe Index (MFINDEX)—Offset 2000h 1161
21.2.24 Interrupter x Management (IMANx)—Offset 2020h 1161
21.2.25 Interrupter x Moderation (IMODx)—Offset 2024h 1162
21.2.26 Event Ring Segment Table Size x (ERSTSZx)—Offset 2028h 1163
21.2.27 Event Ring Segment Table Base Address Low x (ERSTBA_LOx)—Offset 2030h ... 1164
21.2.28 Event Ring Segment Table Base Address High x (ERSTBA_HIx)—Offset 2034h ... 1164
21.2.29 Event Ring Dequeue Pointer Low x (ERDP_LOx)—Offset 2038h 1165
21.2.30 Event Ring Dequeue Pointer High x (ERDP_HIx)—Offset 203Ch 1166
21.2.31 Door Bell x (DBx)—Offset 3000h 1167
21.2.32 XECP_SUPP_USB2_0 (XECP_SUPP_USB2_0)—Offset 8000h 1168
21.2.33 XECP_SUPP_USB2_1 (XECP_SUPP_USB2_1)—Offset 8004h 1168
21.2.34 XECP_SUPP_USB2_2 (XECP_SUPP_USB2_2)—Offset 8008h 1169

21.2.35 XECP_SUPP_USB2_3 (Full Speed) (XECP_SUPP_USB2_3)—Offset 8010h 1170
21.2.36 XECP_SUPP_USB2_4 (Low Speed) (XECP_SUPP_USB2_4)—Offset 8014h ... 1171
21.2.37 XECP_SUPP_USB2_5 (High Speed) (XECP_SUPP_USB2_5)—Offset 8018h .. 1172
21.2.38 XECP_SUPP_USB3_0 (XECP_SUPP_USB3_0)—Offset 8020h 1173
21.2.39 XECP_SUPP_USB3_1 (XECP_SUPP_USB3_1)—Offset 8024h 1173
21.2.40 XECP_SUPP_USB3_2 (XECP_SUPP_USB3_2)—Offset 8028h 1174
21.2.41 XECP_SUPP_USB3_3 (XECP_SUPP_USB3_3)—Offset 8030h 1174
21.2.42 XECP_SUPP_USB3_4 (XECP_SUPP_USB3_4)—Offset 8034h 1175
21.2.43 XECP_SUPP_USB3_5 (XECP_SUPP_USB3_5)—Offset 8038h 1176
21.2.44 XECP_SUPP_USB3_6 (XECP_SUPP_USB3_6)—Offset 803Ch 1176
21.2.45 XECP_SUPP_USB3_7 (XECP_SUPP_USB3_7)—Offset 8040h 1177
21.2.46 XECP_SUPP_USB3_8 (XECP_SUPP_USB3_8)—Offset 8044h 1178
21.2.47 XECP_SUPP_USB3_9 (XECP_SUPP_USB3_9)—Offset 8048h 1178
21.2.48 Host Control Scheduler (HOST_CTRL_SCH_REG)—Offset 8094h..... 1179
21.2.49 Power Management Control (PMCTRL_REG)—Offset 80A4h 1180
21.2.50 HOST_CTRL_MISC_REG (HOST_CTRL_MISC_REG)—Offset 80B0h 1183
21.2.51 HOST_CTRL_MISC_REG2 (HOST_CTRL_MISC_REG2)—Offset 80B4h 1185
21.2.52 SSPE_REG (SSPE_REG)—Offset 80B8h..... 1186
21.2.53 DEVICE MODE CONTROL REG 0 (DUAL_ROLE_CFG_REG0)—Offset 80D8h .. 1186
21.2.54 AUX Power Management Control (AUX_CTRL_REG1)—Offset 80E0h..... 1188
21.2.55 SuperSpeed Port Link Control (HOST_CTRL_PORT_LINK_REG)—Offset 80ECh.... 1190
21.2.56 USB2 Port Link Control 1 (USB2_LINK_MGR_CTRL_REG1)—Offset 80F0h ... 1192
21.2.57 USB2 Port Link Control 4 (USB2_LINK_MGR_CTRL_REG4)—Offset 80FCh ... 1194
21.2.58 Power Scheduler Control-0 (PWR_SCHED_CTRL0)—Offset 8140h 1195
21.2.59 Power Scheduler Control-2 (PWR_SCHED_CTRL2)—Offset 8144h 1196
21.2.60 AUX Power Management Control (AUX_CTRL_REG2)—Offset 8154h..... 1197
21.2.61 USB2 PHY Power Management Control (USB2_PHY_PMC)—Offset 8164h 1199
21.2.62 xHCI Aux Clock Control Register (XHCI_AUX_CCR)—Offset 816Ch 1200
21.2.63 xHC Latency Tolerance Parameters - LTV Control (XLTP_LTV1)—Offset 8174h ... 1203
21.2.64 xHC Latency Tolerance Parameters - High Idle Time Control (XLTP_HITC)—Offset 817Ch 1204
21.2.65 xHC Latency Tolerance Parameters - Medium Idle Time Control (XLTP_MITC)—Offset 8180h 1205
21.2.66 xHC Latency Tolerance Parameters Low Idle Time Control (XLTP_LITC)—Offset 8184h..... 1206
21.2.67 Command Manager Control 2 (XECP_CMDM_CTRL_REG2)—Offset 8190h ... 1206
21.2.68 LFPSONCOUNT_REG (LFPSONCOUNT_REG)—Offset 81B8h..... 1206
21.2.69 USB2 PM Control (USB2PMCTRL_REG)—Offset 81C4h..... 1207
21.2.70 STRAP2_REG (STRAP2_REG)—Offset 8420h..... 1209
21.2.71 USB Legacy Support Capability (USBLEGSUP)—Offset 846Ch..... 1210
21.2.72 Port Disable Override capability register (PDO_CAPABILITY)—Offset 84F4h 1211
21.2.73 USB2 Port Disable Override (USB2PDO)—Offset 84F8h 1211
21.2.74 USB3 Port Disable Override (USB3PDO)—Offset 84FCh 1212
21.2.75 Debug Capability ID Register (DCID)—Offset 8700h 1213
21.2.76 SSIC Local and Remote Profile Registers Capability ID register (SSIC_PROFILE_CAPABILITY_ID_REG)—Offset 8900h 1213
21.2.77 SSIC Port N Register Access Control (PORT1_REGISTER_ACCESS_CONTROL)—Offset 8904h 1214
21.2.78 SSIC Port N Register Access Status (PORT1_REGISTER_ACCESS_STATUS)—Offset 8908h 1215
21.2.79 (PORT1_PROFILE_ATTRIBUTES_REG0)—Offset 890Ch 1216
21.2.80 SSIC Port N Register Access Control (PORT2_REGISTER_ACCESS_CONTROL)—Offset 8A14h 1217

21.2.81 SSIC Port N Register Access Status (PORT2_REGISTER_ACCESS_STATUS)—Offset 8A18h ... 1218
21.2.82 (PORT2_PROFILE_ATTRIBUTES_REG0)—Offset 8A1Ch ... 1219
21.2.83 Global Time Sync Capability (GLOBAL_TIME_SYNC_CAP_REG)—Offset 8E10h ... 1220
21.2.84 Global Time Sync Control (GLOBAL_TIME_SYNC_CTRL_REG)—Offset 8E14h 1220
21.2.85 Microframe Time (Local Time) (MICROFRAME_TIME_REG)—Offset 8E18h ... 1221
21.2.86 Always Running Time (ART) Low (ALWAYS_RUNNING_TIME_LOW)—Offset 8E20h 1222
21.2.87 Always Running Time (ART) High (ALWAYS_RUNNING_TIME_HIGH)—Offset 8E24h ... 1222

22 USB Dual Role/OTG Device Controller (xDCI) (D20:F1) ... 1224

22.1 USB Device Controller (xDCI) Configuration Registers Summary ... 1224
22.1.1 (DEVVENDID)—Offset 0h ... 1224
22.1.2 (STATUSCOMMAND)—Offset 4h ... 1225
22.1.3 (REVCLASSCODE)—Offset 8h ... 1226
22.1.4 (CLLATHEADERBIST)—Offset Ch ... 1226
22.1.5 (BAR)—Offset 10h ... 1227
22.1.6 (BAR_HIGH)—Offset 14h ... 1228
22.1.7 (BAR1)—Offset 18h ... 1228
22.1.8 (SUBSYSTEMID)—Offset 2Ch ... 1229
22.1.9 (EXPANSION_ROM_BASEADDR)—Offset 30h ... 1230
22.1.10 (CAPABILITYPTR)—Offset 34h ... 1231
22.1.11 (INTERRUPTREG)—Offset 3Ch ... 1231
22.1.12 (POWERCAPID)—Offset 80h ... 1232
22.1.13 (PMECTRLSTATUS)—Offset 84h ... 1233
22.1.14 (PCIDEVIDLE_CAP_RECORD)—Offset 90h ... 1233
22.1.15 (DEVID_VEND_SPECIFIC_REG)—Offset 94h ... 1234
22.1.16 (D0I3_CONTROL_SW_LTR_MMIO_REG)—Offset 98h ... 1235
22.1.17 (DEVICE_IDLE_POINTER_REG)—Offset 9Ch ... 1235
22.1.18 (D0I3_MAX_POW_LAT_PG_CONFIG)—Offset A0h ... 1236
22.1.19 (GEN_REGRW1)—Offset B0h ... 1237
22.1.20 (GEN_REGRW2)—Offset B4h ... 1237
22.1.21 (GEN_REGRW3)—Offset B8h ... 1238
22.1.22 (GEN_REGRW4)—Offset BCh ... 1238
22.1.23 (GEN_INPUT_REGRW)—Offset C0h ... 1239
22.2 xDCI MMIO Device Registers Summary ... 1240
22.2.1 Device Configuration Register (DCFG)—Offset C700h ... 1241
22.2.2 Device Control Register (DCTL)—Offset C704h ... 1242
22.2.3 Device Event Enable Register (DEVTEN)—Offset C708h ... 1245
22.2.4 Device Status Register (DSTS)—Offset C70Ch ... 1246
22.2.5 Device Generic Command Parameter (DGCMDPAR)—Offset C710h ... 1248
22.2.6 Device Generic Command Register (DGCMD)—Offset C714h ... 1249
22.2.7 Device Active USB Endpoint Enable (DALEPENA)—Offset C720h ... 1250
22.2.8 Device Physical Endpoint-n Command Parameter 2 Register (DEPCMDPAR2)—Offset C800h ... 1251
22.2.9 Device Physical Endpoint-n Command Parameter 1 Register (DEPCMDPAR1)—Offset C804h ... 1251
22.2.10 Device Physical Endpoint-n Command Parameter 0 Register (DEPCMDPAR0)—Offset C808h ... 1252
22.2.11 Device Physical Endpoint-n Command Register (DEPCMD)—Offset C80Ch ... 1252
22.3 xDCI MMIO Global Registers Summary ... 1254
22.3.1 Global SoC Bus Configuration 0 (GSBUSCFG0)—Offset C100h ... 1255
22.3.2 Global SoC Bus Configuration 1 (GSBUSCFG1)—Offset C104h ... 1256
22.3.3 Global Tx Threshold Control (GTXTHRCFG)—Offset C108h ... 1257

22.3.4 Global Rx Threshold Control (GRXTHRCFG)—Offset C10Ch 1258
22.3.5 Global Core Control (GCTL)—Offset C110h 1259
22.3.6 GPMSTS (GPMSTS)—Offset C114h 1260
22.3.7 Global Status (GSTS)—Offset C118h 1261
22.3.8 Bus Address Low (GBUSERRADDRLO)—Offset C130h 1261
22.3.9 Bus Address High (GBUSERRADDRHI)—Offset C134h 1262
22.3.10 GHWPARAMS0 (GHWPARAMS0)—Offset C140h 1262
22.3.11 GHWPARAMS1 (GHWPARAMS1)—Offset C144h 1262
22.3.12 GHWPARAMS2 (GHWPARAMS2)—Offset C148h 1263
22.3.13 GHWPARAMS3 (GHWPARAMS3)—Offset C14Ch 1263
22.3.14 GHWPARAMS4 (GHWPARAMS4)—Offset C150h 1264
22.3.15 GHWPARAMS5 (GHWPARAMS5)—Offset C154h 1265
22.3.16 GHWPARAMS6 (GHWPARAMS6)—Offset C158h 1265
22.3.17 GHWPARAMS7 (GHWPARAMS7)—Offset C15Ch 1266
22.3.18 GDBGFIFOSPACE (GDBGFIFOSPACE)—Offset C160h 1266
22.3.19 GDBGLTSSM (GDBGLTSSM)—Offset C164h 1267
22.3.20 GDBGLNMCC (GDBGLNMCC)—Offset C168h 1268
22.3.21 GDBGBMU (GDBGBMU)—Offset C16Ch 1268
22.3.22 GDBGLSP (GDBGLSP)—Offset C174h 1269
22.3.23 GDBGEPINFO0 (GDBGEPINFO0)—Offset C178h 1269
22.3.24 GDBGEPINFO1 (GDBGEPINFO1)—Offset C17Ch 1269
22.3.25 Global Transmit FIFO Size Register N (GTXFIFOSIZ0_0)—Offset C300h 1270
22.3.26 GRXFIFOSIZ0_0 (GRXFIFOSIZ0_0)—Offset C380h 1270
22.3.27 GEVNTADRLO_0 (GEVNTADRLO_0)—Offset C400h 1270
22.3.28 GEVNTADRHI_0 (GEVNTADRHI_0)—Offset C404h 1271
22.3.29 GEVNTCOUNT_0 (GEVNTCOUNT_0)—Offset C40Ch 1271
22.3.30 GTXFIFOPRIDEV (GTXFIFOPRIDEV)—Offset C610h 1271

23 Thermal Subsystem (D20: F2) 1273
23.1 Thermal Reporting Configuration Registers Summary 1273
23.1.1 Vendor Identification (VID)—Offset 0h 1273
23.1.2 Device Identification (DID)—Offset 2h 1274
23.1.3 Command (CMD)—Offset 4h 1274
23.1.4 Status (STS)—Offset 6h 1275
23.1.5 Revision Identification (RID)—Offset 8h 1276
23.1.6 Programming Interface (PI)—Offset 9h 1277
23.1.7 Sub Class Code (SCC)—Offset Ah 1277
23.1.8 Base Class Code (BCC)—Offset Bh 1277
23.1.9 Cache Line Size (CLS)—Offset Ch 1278
23.1.10 Latency Timer (LT)—Offset Dh 1278
23.1.11 Header Type (HTYPE)—Offset Eh 1279
23.1.12 Thermal Base (TBAR)—Offset 10h 1279
23.1.13 Thermal Base High DWord (TBARH)—Offset 14h 1280
23.1.14 Subsystem Vendor ID (SVID)—Offset 2Ch 1280
23.1.15 Subsystem ID (SID)—Offset 2Eh 1281
23.1.16 Capabilities Pointer (CAP_PTR)—Offset 34h 1281
23.1.17 Interrupt Line (INTLN)—Offset 3Ch 1282
23.1.18 Interrupt Pin (INTPN)—Offset 3Dh 1282
23.1.19 BIOS Assigned Thermal Base Address (TBARB)—Offset 40h 1283
23.1.20 BIOS Assigned Thermal Base High DWord (TBARBH)—Offset 44h 1283
23.1.21 Control Bits (CB)—Offset 48h 1284
23.1.22 PCI Power Management Capability ID (PID)—Offset 50h 1284
23.1.23 Power Management Capabilities (PC)—Offset 52h 1285
23.1.24 Power Management Control And Status (PCS)—Offset 54h 1285
23.1.25 Message Signaled Interrupt Identifiers (MID)—Offset 80h 1286

23.1.26 Message Signaled Interrupt Message Control (MC)—Offset 82h 1287
23.1.27 Message Signaled Interrupt Message Address (MA)—Offset 84h 1287
23.1.28 Message Signaled Interrupt Message Data (MD)—Offset 88h 1288
23.2 Thermal Reporting Memory Mapped Registers Summary 1288
23.2.1 Temperature (TEMP)—Offset 0h 1289
23.2.2 Thermal Sensor Control (TSC)—Offset 4h 1289
23.2.3 Thermal Sensor Status (TSS)—Offset 6h 1290
23.2.4 Thermal Sensor Enable and Lock (TSEL)—Offset 8h 1291
23.2.5 Thermal Sensor Reporting Enable and Lock (TSREL)—Offset Ah 1291
23.2.6 Thermal Sensor SMI Control (TSMIC)—Offset Ch 1292
23.2.7 Catastrophic Trip Point (CTT)—Offset 10h 1292
23.2.8 Thermal Alert High Value (TAHV)—Offset 14h 1293
23.2.9 Thermal Alert Low Value (TALV)—Offset 18h 1293
23.2.10 Thermal Sensor Power Management (TSPM)—Offset 1Ch 1294
23.2.11 Throttle Levels (TL)—Offset 40h 1295
23.2.12 Throttle Level 2 (TL2)—Offset 50h 1296
23.2.13 PCH Hot Level (PHL)—Offset 60h 1296
23.2.14 PHL Control (PHLC)—Offset 62h 1297
23.2.15 Thermal Alert Status (TAS)—Offset 80h 1297
23.2.16 PCI Interrupt Event Enables (TSPIEN)—Offset 82h 1298
23.2.17 General Purpose Event Enables (TSGPEN)—Offset 84h 1298
23.2.18 Thernak Controller Function Disable (TCFD)—Offset F0h 1299
23.3 1299

24 CSI2 Interface (D20:F3) 1300
24.1 CSI-2 Configuration Registers Summary 1300
24.1.1 CFG_ID (CFG_ID)—Offset 0h 1300
24.1.2 CFG_CMD (CFG_CMD_STS)—Offset 4h 1301
24.1.3 Revision ID and Class Code (CFG_CC)—Offset 8h 1302
24.1.4 CFG_CLS_LT_HTYPE_BIST (CFG_CLS_LT_HTYPE_BIST)—Offset Ch 1303
24.1.5 CFG_CIOLBA (CIOLBA)—Offset 10h 1303
24.1.6 CFG_CIOUBA (CIOUBA)—Offset 14h 1304
24.1.7 CFG_SSID (SSID)—Offset 2Ch 1304
24.1.8 CFG_CAPPTR (CAPPTR)—Offset 34h 1305
24.1.9 CFG_INTR (CFG_INTR)—Offset 3Ch 1305
24.1.10 CFG_MID_MMC (CFG_MID_MMC)—Offset 90h 1306
24.1.11 CFG_MMLA (CFG_MMLA)—Offset 94h 1307
24.1.12 CFG_MMUA (CFG_MMUA)—Offset 98h 1307
24.1.13 CFG_MMD (CFG_MMD)—Offset 9Ch 1307
24.1.14 CFG_AFID (AFID)—Offset A0h 1308
24.1.15 CFG_AF_CMD_STS (AF_CMD_STS)—Offset A4h 1309
24.1.16 CFG_PID_PC (CFG_PID_PC)—Offset D0h 1309
24.1.17 CFG_PMCSR (CFG_PMCSR)—Offset D4h 1310
24.2 CSI2 Memory Mapped I/O Registers Summary 1311
24.2.1 CSI RX Enable (csi2_pipe_a_csi_rx4_reg_rx_csi_enable)—Offset 0h 1313
24.2.2 Number of enabled data lines (csi2_pipe_a_csi_rx4_reg_rx_csi_nof_enabled_lanes)—Offset 4h 1313
24.2.3 Error Handling (csi2_pipe_a_csi_rx4_reg_rx_csi_error_handling)—Offset Ch 1314
24.2.4 Short Frame Config (csi2_pipe_a_csi_rx4_reg_rx_csi_sp_if_config)—Offset 10h 1315
24.2.5 Long Frame Config (csi2_pipe_a_csi_rx4_reg_rx_csi_lp_if_config)—Offset 14h 1315
24.2.6 Status Register (csi2_pipe_a_csi_rx4_reg_rx_status)—Offset 18h 1316
24.2.7 Clock Termination Delay (csi2_pipe_a_csi_rx4_reg_rx_csi_dly_cnt_termen_clane)—Offset 24h 1317

24.2.8 Settling delay (csi2_pipe_a_csi_rx4_reg_rx_csi_dly_cnt_settle_clane)—Offset 28h 1317
24.2.9 Delay After Termination (csi2_pipe_a_csi_rx4_reg_rx_csi_dly_cnt_termen_dlane0)—Offset 2Ch 1318
24.2.10 Settling time for Data (csi2_pipe_a_csi_rx4_reg_rx_csi_dly_cnt_settle_dlane0)—Offset 30h 1319
24.2.11 Backend Enable/Disable (csi2_pipe_a_mipi_be_mipi_backend_enable)—Offset 100h 1320
24.2.12 Backend Status (csi2_pipe_a_mipi_be_mipi_backend_status)—Offset 104h 1320
24.2.13 Compression and Prediction (csi2_pipe_a_mipi_be_mipi_backend_comp_format_reg_vc0)—Offset 108h 1321
24.2.14 Force raw8 (csi2_pipe_a_mipi_be_mipi_backend_force_raw8_reg)—Offset 120h 1323
24.2.15 IRQ Status (csi2_pipe_a_mipi_be_mipi_backend_irq_status_reg)—Offset 124h . 1323
24.2.16 Interrupt Clear (csi2_pipe_a_mipi_be_mipi_backend_irq_clear_reg)—Offset 128h 1324
24.2.17 Disregard Setting (csi2_pipe_a_mipi_be_mipi_backend_global_lut_disregard_reg)—Offset 168h... 1325
24.2.18 Stalled Packet (csi2_pipe_a_mipi_be_mipi_backend_packet_status_stall_reg)—Offset 16Ch 1326
24.2.19 Parse short packets (csi2_pipe_a_mipi_be_mipi_backend_parse_gsp_through_lp_lut_reg)—Offset 170h 1327
24.2.20 Short packets entry (csi2_pipe_a_mipi_be_mipi_backend_short_packet_lut_entry_0)—Offset 174h . 1328
24.2.21 Long packets entry (csi2_pipe_a_mipi_be_mipi_backend_long_packet_lut_entry_0)—Offset 184h... 1329
24.2.22 (csi2_pipe_a_irq_ctrl_pipe_irq_edge)—Offset 300h..... 1331
24.2.23 (csi2_pipe_a_irq_ctrl_pipe_irq_mask)—Offset 304h 1332
24.2.24 (csi2_pipe_a_irq_ctrl_pipe_irq_status)—Offset 308h 1334
24.2.25 (csi2_pipe_a_irq_ctrl_pipe_irq_clear)—Offset 30Ch..... 1335
24.2.26 (csi2_pipe_a_irq_ctrl_pipe_irq_en)—Offset 310h 1337
24.2.27 (csi2_pipe_a_irq_ctrl_pipe_irq_level_not_pulse)—Offset 314h..... 1338
24.2.28 (gpreg_dev_soft_reset_reg)—Offset 1000h..... 1340
24.2.29 (gpreg_slv_soft_reset_reg)—Offset 1004h..... 1341
24.2.30 (gpreg_fb_hpll_freq_reg)—Offset 1008h..... 1342
24.2.31 (gpreg_isclk_ratio_reg)—Offset 100Ch 1343
24.3 Camera CSI2 Host Controller MMIO 1 Registers Summary..... 1343
24.3.1 CIO2_CGC (CIO2_CGC)—Offset 1400h 1344
24.3.2 CIO2_PGC (CIO2_PGC)—Offset 1404h 1345
24.3.3 CIO2_D0I3C (CIO2_D0I3C)—Offset 1408h 1347
24.3.4 SWReset (SWReset)—Offset 140Ch 1348
24.3.5 CSI2_SENSOR_ACTIVE (CSI2_SENSOR_ACTIVE)—Offset 1410h 1348
24.3.6 INT Status (INT_STS)—Offset 1414h 1350
24.3.7 INT_STS_EXT_OE (INT_STS_EXT_OE)—Offset 1418h..... 1352
24.3.8 INT_EN (INT_EN)—Offset 1420h 1353
24.3.9 INT_EN_EXT_OE (INT_EN_EXT_OE)—Offset 1424h..... 1355
24.3.10 RCOMPCtrl (RCOMPCtrl)—Offset 1428h 1356
24.3.11 PCE (PCE)—Offset 1430h..... 1357
24.3.12 MMIO_RID (MMIO_RID)—Offset 1444h 1358
24.3.13 Frame Buffer Pointer Table base address (CDMABA[19:0])—Offset 1500h .. 1358
24.3.14 DMA Read Index Register (CDMARI[19:0])—Offset 1504h..... 1359

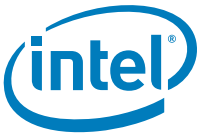
24.3.15 CIO2 DMA Control (CDMAC0[19:0])—Offset 1508h 1360
24.3.16 CIO2 DMA Control Register1 (CDMAC1[19:0])—Offset 150Ch 1362
24.4 Camera CSI2 Host Controller MMIO 2 Registers Summary 1363
24.4.1 PBM_ARB_CTRL (PBM_ARB_CTRL)—Offset 1460h 1364
24.4.2 PBM_WMCtrl1 (PBM_WMCtrl1)—Offset 1464h 1365
24.4.3 PBM_WMCtrl2 (PBM_WMCtrl2)—Offset 1468h 1366
24.4.4 PBM_TS_COUNT (PBM_TS_COUNT)—Offset 146Ch 1367
24.4.5 PBM_TS_SW_W (PBM_TS_SW_W)—Offset 1470h 1367
24.4.6 PBM_FOPN_ABORT (PBM_FOPN_ABORT)—Offset 1474h 1368
24.4.7 LTRCtrl (LTRCtrl)—Offset 1480h 1369
24.4.8 LTRVal1 (LTRVal1)—Offset 1484h 1370
24.4.9 LTRVal0 (LTRVal0)—Offset 1488h 1371
24.4.10 PBM PLL and frame period (PBM_FRAME_PERIOD_S[3:0])—Offset 148Ch ... 1372
24.4.11 PBM_FLASH_CTRL (PBM_FLASH_CTRL)—Offset 149Ch 1373
24.4.12 PBM_FLASH_TM_TO_TRG (PBM_FLASH_TM_TO_TRG)—Offset 14A0h 1374
24.4.13 PBM_FLASH_TRG_WDT (PBM_FLASH_TRG_WDT)—Offset 14A4h 1374
24.4.14 PBM_STS_0 (PBM_STS_0)—Offset 14A8h 1375
24.4.15 PBM_STS_1 (PBM_STS_1)—Offset 14ACh 1375
24.4.16 PBM_STS_2 (PBM_STS_2)—Offset 14B0h 1376
24.4.17 PBM_STS_3 (PBM_STS_3)—Offset 14B4h 1376
24.4.18 PXF formats configurations (PXM_PXF_FMT_Cfg0[0])—Offset 1700h 1377
24.4.19 PXM_FRF_cfg (PXM_FRF_cfg[3:0])—Offset 1720h 1379
24.4.20 Sensor0 PXM Sidebid (PXM_SID2BID[2-0]Sensor[3:0])—Offset 1724h 1380
24.4.21 PXM_PXF_FMT_Cfg3 (PXM_PXF_FMT_Cfg3[3])—Offset 179Ch 1381
24.4.22 Channel Merging (PXM_CHM)—Offset 17C0h 1383
24.4.23 Number Of CRC (PXM_CRC_S[3:0])—Offset 17C4h 1384
24.4.24 Number Of ECC (PXM_ECC_S[3:0])—Offset 17C8h 1384
24.4.25 Interrupt status for input error (INT_STS_EXT_IE)—Offset 17E4h 1385
24.4.26 Enable interrupt for input error (INT_EN_EXT_IE)—Offset 17E8h 1387
24.5 CSI2 Additional Configuration Registers Summary 1389
24.5.1 CSI0 RX Control (CSI0_RXCNTRL)—Offset 0h 1389
24.5.2 CSI1 RX Control (CSI1_RXCNTRL)—Offset 3h 1390
24.5.3 CSI2 RX Control (CSI2_RXCNTRL)—Offset Ah 1391
24.5.4 (CSI_CLKTRIM)—Offset Fh 1391
24.5.5 CSI3 RX Control (CSI3_RXCNTRL)—Offset 10h 1392
24.5.6 CSI Configuration (CSI_CFG)—Offset 13h 1393
24.5.7 CSI Data Trim (CSI_DATATRIM)—Offset 24h 1393
24.5.8 CSI CTLE (CSI_CTLE)—Offset 25h 1393
24.5.9 (CSI_DATATRIM1)—Offset 30h 1394

25 Integrated Sensor Hub (ISH) (D19:F0) 1395
25.1 ISH PCI Configuration Registers Summary 1395
25.1.1 Device and Vendor ID Register (DEVVENDID)—Offset 0h 1395
25.1.2 Status and Command (STATUSCOMMAND)—Offset 4h 1396
25.1.3 Revision ID and Class Code (REVCLASSCODE)—Offset 8h 1397
25.1.4 Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch 1397
25.1.5 Memory Base Address Register (BAR)—Offset 10h 1398
25.1.6 Memory Base Address Register High (BAR_HIGH)—Offset 14h 1399
25.1.7 Memory Base Address 1 (BAR1)—Offset 18h 1399
25.1.8 Memory Base Address 1 High (BAR1_HIGH)—Offset 1Ch 1400
25.1.9 Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch 1401
25.1.10 Expansion ROM base address (EXPANSION_ROM_BASEADDR)—Offset 30h . 1401
25.1.11 Capabilities Pointer (CAPABILITYPTR)—Offset 34h 1402
25.1.12 Interrupt (INTERRUPTREG)—Offset 3Ch 1402
25.1.13 PowerManagement Capability ID (POWERCAPID)—Offset 80h 1403

25.1.14 Power Management Control and Status (PMECTRLSTATUS)—Offset 84h 1404
25.1.15 General Purpose Read Write Register1 (GEN_REGRW1)—Offset A0h 1404
25.1.16 General Purpose Read Write Register2 (GEN_REGRW2)—Offset A4h 1405
25.1.17 General Purpose Read Write Register3 (GEN_REGRW3)—Offset A8h 1405
25.1.18 General Purpose Read Write Register4 (GEN_REGRW4)—Offset ACh 1406
25.1.19 General Purpose Input Register (GEN_INPUT_REG)—Offset C0h 1406
25.2 ISH MMIO Registers Summary 1407
25.2.1 ISH Host firmware status (ISH_HOST_FWSTS)—Offset 34h 1407
25.2.2 Host Communication (HOST_COMM)—Offset 38h 1408
25.2.3 (HOST2ISH_DOORBELL)—Offset 48h 1408
25.2.4 ISH-to-Host DoorBell (ISH2HOST_DOORBELL)—Offset 54h 1409
25.2.5 Message from ISH to HOST (ISH2HOST_MSG)—Offset 60h 1409
25.2.6 Message from HOST to ISH (HOST2ISH_MSG1)—Offset E0h 1410
25.2.7 ISH Remap (REMAP)—Offset 360h 1410
25.2.8 D0i3 Control (IPC_d0i3C_reg)—Offset 6D0h 1411

26 8254 Timer 1413
26.1 8254 Timer Registers Summary 1413
26.1.1 Counter 0 - Interval Timer Status Byte Format Register (C0_ITSBFR)—Offset 40h 1413
26.1.2 Counter 0 - Counter Access Ports Register (C0_CAPR)—Offset 40h 1414
26.1.3 Counter 2 - Interval Timer Status Byte Format Register (C2_ITSBFR)—Offset 42h 1414
26.1.4 Counter 2 - Counter Access Ports Register (C2_CAPR)—Offset 42h 1415
26.1.5 Timer Control Word Register (TCW)—Offset 43h 1415
26.1.6 Read Back Command (RBC)—Offset 43h 1416
26.1.7 Counter Latch Command (CLC)—Offset 43h 1416

27 Advanced Programmable Interrupt (APIC) 1418
27.1 APIC Indirect Registers Summary 1418
27.1.1 Identification Register (ID)—Offset 0h 1421
27.1.2 Version Register (VER)—Offset 1h 1422
27.1.3 Redirection Table Entry 0 (RTE0)—Offset 10h 1423
27.1.4 Redirection Table Entry 1 (RTE1)—Offset 12h 1424
27.1.5 Redirection Table Entry 2 (RTE2)—Offset 14h 1424
27.1.6 Redirection Table Entry 3 (RTE3)—Offset 16h 1424
27.1.7 Redirection Table Entry 4 (RTE4)—Offset 18h 1424
27.1.8 Redirection Table Entry 5 (RTE5)—Offset 1Ah 1424
27.1.9 Redirection Table Entry 6 (RTE6)—Offset 1Ch 1424
27.1.10 Redirection Table Entry 7 (RTE7)—Offset 1Eh 1424
27.1.11 Redirection Table Entry 8 (RTE8)—Offset 20h 1425
27.1.12 Redirection Table Entry 9 (RTE9)—Offset 22h 1425
27.1.13 Redirection Table Entry 10 (RTE10)—Offset 24h 1425
27.1.14 Redirection Table Entry 11 (RTE11)—Offset 26h 1425
27.1.15 Redirection Table Entry 12 (RTE12)—Offset 28h 1425
27.1.16 Redirection Table Entry 13 (RTE13)—Offset 2Ah 1425
27.1.17 Redirection Table Entry 14 (RTE14)—Offset 2Ch 1425
27.1.18 Redirection Table Entry 15 (RTE15)—Offset 2Eh 1425
27.1.19 Redirection Table Entry 16 (RTE16)—Offset 30h 1425
27.1.20 Redirection Table Entry 17 (RTE17)—Offset 32h 1425
27.1.21 Redirection Table Entry 18 (RTE18)—Offset 34h 1425
27.1.22 Redirection Table Entry 19 (RTE19)—Offset 36h 1425
27.1.23 Redirection Table Entry 20 (RTE20)—Offset 38h 1425
27.1.24 Redirection Table Entry 21 (RTE21)—Offset 3Ah 1426
27.1.25 Redirection Table Entry 22 (RTE22)—Offset 3Ch 1426
27.1.26 Redirection Table Entry 23 (RTE23)—Offset 3Eh 1426

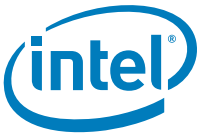


27.1.27 Redirection Table Entry 24 (RTE24)—Offset 40h 1426
27.1.28 Redirection Table Entry 25 (RTE25)—Offset 42h 1426
27.1.29 Redirection Table Entry 26 (RTE26)—Offset 44h 1426
27.1.30 Redirection Table Entry 27 (RTE27)—Offset 46h 1426
27.1.31 Redirection Table Entry 28 (RTE28)—Offset 48h 1426
27.1.32 Redirection Table Entry 29 (RTE29)—Offset 4Ah 1426
27.1.33 Redirection Table Entry 30 (RTE30)—Offset 4Ch 1426
27.1.34 Redirection Table Entry 31 (RTE31)—Offset 4Eh 1426
27.1.35 Redirection Table Entry 32 (RTE32)—Offset 50h 1426
27.1.36 Redirection Table Entry 33 (RTE33)—Offset 52h 1426
27.1.37 Redirection Table Entry 34 (RTE34)—Offset 54h 1427
27.1.38 Redirection Table Entry 35 (RTE35)—Offset 56h 1427
27.1.39 Redirection Table Entry 36 (RTE36)—Offset 58h 1427
27.1.40 Redirection Table Entry 37 (RTE37)—Offset 5Ah 1427
27.1.41 Redirection Table Entry 38 (RTE38)—Offset 5Ch 1427
27.1.42 Redirection Table Entry 39 (RTE39)—Offset 5Eh 1427
27.1.43 Redirection Table Entry 40 (RTE40)—Offset 60h 1427
27.1.44 Redirection Table Entry 41 (RTE41)—Offset 62h 1427
27.1.45 Redirection Table Entry 42 (RTE42)—Offset 64h 1427
27.1.46 Redirection Table Entry 43 (RTE43)—Offset 66h 1427
27.1.47 Redirection Table Entry 44 (RTE44)—Offset 68h 1427
27.1.48 Redirection Table Entry 45 (RTE45)—Offset 6Ah 1427
27.1.49 Redirection Table Entry 46 (RTE46)—Offset 6Ch 1427
27.1.50 Redirection Table Entry 47 (RTE47)—Offset 6Eh 1428
27.1.51 Redirection Table Entry 48 (RTE48)—Offset 70h 1428
27.1.52 Redirection Table Entry 49 (RTE49)—Offset 72h 1428
27.1.53 Redirection Table Entry 50 (RTE50)—Offset 74h 1428
27.1.54 Redirection Table Entry 51 (RTE51)—Offset 76h 1428
27.1.55 Redirection Table Entry 52 (RTE52)—Offset 78h 1428
27.1.56 Redirection Table Entry 53 (RTE53)—Offset 7Ah 1428
27.1.57 Redirection Table Entry 54 (RTE54)—Offset 7Ch 1428
27.1.58 Redirection Table Entry 55 (RTE55)—Offset 7Eh 1428
27.1.59 Redirection Table Entry 56 (RTE56)—Offset 80h 1428
27.1.60 Redirection Table Entry 57 (RTE57)—Offset 82h 1428
27.1.61 Redirection Table Entry 58 (RTE58)—Offset 84h 1428
27.1.62 Redirection Table Entry 59 (RTE59)—Offset 86h 1428
27.1.63 Redirection Table Entry 60 (RTE60)—Offset 88h 1429
27.1.64 Redirection Table Entry 61 (RTE61)—Offset 8Ah 1429
27.1.65 Redirection Table Entry 62 (RTE62)—Offset 8Ch 1429
27.1.66 Redirection Table Entry 63 (RTE63)—Offset 8Eh 1429
27.1.67 Redirection Table Entry 64 (RTE64)—Offset 90h 1429
27.1.68 Redirection Table Entry 65 (RTE65)—Offset 92h 1429
27.1.69 Redirection Table Entry 66 (RTE66)—Offset 94h 1429
27.1.70 Redirection Table Entry 67 (RTE67)—Offset 96h 1429
27.1.71 Redirection Table Entry 68 (RTE68)—Offset 98h 1429
27.1.72 Redirection Table Entry 69 (RTE69)—Offset 9Ah 1429
27.1.73 Redirection Table Entry 70 (RTE70)—Offset 9Ch 1429
27.1.74 Redirection Table Entry 71 (RTE71)—Offset 9Eh 1429
27.1.75 Redirection Table Entry 72 (RTE72)—Offset A0h 1429
27.1.76 Redirection Table Entry 73 (RTE73)—Offset A2h 1430
27.1.77 Redirection Table Entry 74 (RTE74)—Offset A4h 1430
27.1.78 Redirection Table Entry 75 (RTE75)—Offset A6h 1430
27.1.79 Redirection Table Entry 76 (RTE76)—Offset A8h 1430
27.1.80 Redirection Table Entry 77 (RTE77)—Offset AAh 1430
27.1.81 Redirection Table Entry 78 (RTE78)—Offset ACh 1430

27.1.82 Redirection Table Entry 79 (RTE79)—Offset AEh 1430
27.1.83 Redirection Table Entry 80 (RTE80)—Offset B0h 1430
27.1.84 Redirection Table Entry 81 (RTE81)—Offset B2h 1430
27.1.85 Redirection Table Entry 82 (RTE82)—Offset B4h 1430
27.1.86 Redirection Table Entry 83 (RTE83)—Offset B6h 1430
27.1.87 Redirection Table Entry 84 (RTE84)—Offset B8h 1430
27.1.88 Redirection Table Entry 85 (RTE85)—Offset BAh 1430
27.1.89 Redirection Table Entry 86 (RTE86)—Offset BCh 1431
27.1.90 Redirection Table Entry 87 (RTE87)—Offset BEh 1431
27.1.91 Redirection Table Entry 88 (RTE88)—Offset C0h 1431
27.1.92 Redirection Table Entry 89 (RTE89)—Offset C2h 1431
27.1.93 Redirection Table Entry 90 (RTE90)—Offset C4h 1431
27.1.94 Redirection Table Entry 91 (RTE91)—Offset C6h 1431
27.1.95 Redirection Table Entry 92 (RTE92)—Offset C8h 1431
27.1.96 Redirection Table Entry 93 (RTE93)—Offset CAh 1431
27.1.97 Redirection Table Entry 94 (RTE94)—Offset CCh 1431
27.1.98 Redirection Table Entry 95 (RTE95)—Offset CEh 1431
27.1.99 Redirection Table Entry 96 (RTE96)—Offset D0h 1431
27.1.100 Redirection Table Entry 97 (RTE97)—Offset D2h 1431
27.1.101 Redirection Table Entry 98 (RTE98)—Offset D4h 1431
27.1.102 Redirection Table Entry 99 (RTE99)—Offset D6h 1432
27.1.103 Redirection Table Entry 100 (RTE100)—Offset D8h 1432
27.1.104 Redirection Table Entry 101 (RTE101)—Offset DAh 1432
27.1.105 Redirection Table Entry 102 (RTE102)—Offset DCh 1432
27.1.106 Redirection Table Entry 103 (RTE103)—Offset DEh 1432
27.1.107 Redirection Table Entry 104 (RTE104)—Offset E0h 1432
27.1.108 Redirection Table Entry 105 (RTE105)—Offset E2h 1432
27.1.109 Redirection Table Entry 106 (RTE106)—Offset E4h 1432
27.1.110 Redirection Table Entry 107 (RTE107)—Offset E6h 1432
27.1.111 Redirection Table Entry 108 (RTE108)—Offset E8h 1432
27.1.112 Redirection Table Entry 109 (RTE109)—Offset EAh 1432
27.1.113 Redirection Table Entry 110 (RTE110)—Offset ECh 1432
27.1.114 Redirection Table Entry 111 (RTE111)—Offset EEh 1432
27.1.115 Redirection Table Entry 112 (RTE112)—Offset F0h 1433
27.1.116 Redirection Table Entry 113 (RTE113)—Offset F2h 1433
27.1.117 Redirection Table Entry 114 (RTE114)—Offset F4h 1433
27.1.118 Redirection Table Entry 115 (RTE115)—Offset F6h 1433
27.1.119 Redirection Table Entry 116 (RTE116)—Offset F8h 1433
27.1.120 Redirection Table Entry 117 (RTE117)—Offset FAh 1433
27.1.121 Redirection Table Entry 118 (RTE118)—Offset FCh 1433
27.1.122 Redirection Table Entry 119 (RTE119)—Offset FEh 1433
27.2 Advanced Programmable Interrupt Controller (APIC) Registers Summary 1433
27.2.1 Index Register (IDX)—Offset 0h 1434
27.2.2 Data Register (DAT)—Offset 10h 1434
27.2.3 EOI Register (EOIR)—Offset 40h 1434

28 Processor Interface 1436
28.1 Processor Interface Memory Registers Summary 1436
28.1.1 NMI Status and Control (NMI_STS_CNT)—Offset 61h 1436
28.1.2 NMI Enable (and Real Time Clock Index) (NMI_EN)—Offset 70h 1437
28.1.3 Init Register (PORT92)—Offset 92h 1437
28.1.4 Reset Control Register (RST_CNT)—Offset CF9h 1438

29 General Purpose I/O (GPIO) 1440
29.1 GPIO Community 0 Registers Summary 1440
29.1.1 Family Base Address (FAMBAR)—Offset 8h 1445



29.1.2 Pad Base Address (PADBAR)—Offset Ch 1446
29.1.3 Miscellaneous Configuration (MISCCFG)—Offset 10h 1446
29.1.4 Pad Ownership (PAD_OWN_GPP_A_0)—Offset 20h 1447
29.1.5 Pad Ownership (PAD_OWN_GPP_A_1)—Offset 24h 1449
29.1.6 Pad Ownership (PAD_OWN_GPP_A_2)—Offset 28h 1449
29.1.7 Pad Ownership (PAD_OWN_GPP_B_0)—Offset 30h 1449
29.1.8 Pad Ownership (PAD_OWN_GPP_B_1)—Offset 34h 1449
29.1.9 Pad Ownership (PAD_OWN_GPP_B_2)—Offset 38h 1449
29.1.10 Pad Configuration Lock (PADCFGLOCK_GPP_A)—Offset A0h 1449
29.1.11 Pad Configuration Lock (PADCFGLOCKTX_GPP_A)—Offset A4h 1451
29.1.12 Pad Configuration Lock (PADCFGLOCK_GPP_B)—Offset A8h 1453
29.1.13 Pad Configuration Lock (PADCFGLOCKTX_GPP_B)—Offset ACh 1453
29.1.14 Host Software Pad Ownership (HOSTSW_OWN_GPP_A)—Offset D0h 1453
29.1.15 Host Software Pad Ownership (HOSTSW_OWN_GPP_B)—Offset D4h 1454
29.1.16 GPI Interrupt Status (GPI_IS_GPP_A)—Offset 100h 1454
29.1.17 GPI Interrupt Status (GPI_IS_GPP_B)—Offset 104h 1456
29.1.18 GPI Interrupt Enable (GPI_IE_GPP_A)—Offset 120h 1456
29.1.19 GPI Interrupt Enable (GPI_IE_GPP_B)—Offset 124h 1458
29.1.20 GPI General Purpose Events Status (GPI_GPE_STS_GPP_A)—Offset 140h ... 1458
29.1.21 GPI General Purpose Events Status (GPI_GPE_STS_GPP_B)—Offset 144h ... 1460
29.1.22 GPI General Purpose Events Enable (GPI_GPE_EN_GPP_A)—Offset 160h 1460
29.1.23 GPI General Purpose Events Enable (GPI_GPE_EN_GPP_B)—Offset 164h 1462
29.1.24 SMI Status (GPI_SMI_STS_GPP_B)—Offset 184h 1462
29.1.25 SMI Enable (GPI_SMI_EN_GPP_B)—Offset 1A4h 1463
29.1.26 NMI Status (GPI_NMI_STS_GPP_B)—Offset 1C4h 1464
29.1.27 NMI Enable (GPI_NMI_EN_GPP_B)—Offset 1E4h 1465
29.1.28 Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_0)—Offset 400h 1466
29.1.29 Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_0)—Offset 404h 1468
29.1.30 Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_1)—Offset 408h 1469
29.1.31 Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_1)—Offset 40Ch 1469
29.1.32 Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_2)—Offset 410h 1469
29.1.33 Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_2)—Offset 414h 1470
29.1.34 Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_3)—Offset 418h 1470
29.1.35 Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_3)—Offset 41Ch 1470
29.1.36 Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_4)—Offset 420h 1470
29.1.37 Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_4)—Offset 424h 1470
29.1.38 Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_5)—Offset 428h 1470
29.1.39 Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_5)—Offset 42Ch 1471
29.1.40 Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_6)—Offset 430h 1471
29.1.41 Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_6)—Offset 434h 1471
29.1.42 Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_7)—Offset 438h 1471
29.1.43 Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_7)—Offset 43Ch 1471
29.1.44 Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_8)—Offset 440h 1471
29.1.45 Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_8)—Offset 444h 1471
29.1.46 Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_9)—Offset 448h 1472
29.1.47 Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_9)—Offset 44Ch 1472
29.1.48 Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_10)—Offset 450h 1472
29.1.49 Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_10)—Offset 454h 1472
29.1.50 Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_11)—Offset 458h 1472
29.1.51 Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_11)—Offset 45Ch 1472
29.1.52 Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_12)—Offset 460h 1473
29.1.53 Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_12)—Offset 464h 1473
29.1.54 Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_13)—Offset 468h 1473
29.1.55 Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_13)—Offset 46Ch 1473
29.1.56 Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_14)—Offset 470h 1473

29.1.57 Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_14)—Offset 474h 1473
29.1.58 Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_15)—Offset 478h 1473
29.1.59 Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_15)—Offset 47Ch 1473
29.1.60 Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_16)—Offset 480h 1474
29.1.61 Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_16)—Offset 484h 1474
29.1.62 Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_17)—Offset 488h 1474
29.1.63 Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_17)—Offset 48Ch 1474
29.1.64 Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_18)—Offset 490h 1474
29.1.65 Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_18)—Offset 494h 1474
29.1.66 Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_19)—Offset 498h 1474
29.1.67 Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_19)—Offset 49Ch 1475
29.1.68 Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_20)—Offset 4A0h 1475
29.1.69 Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_20)—Offset 4A4h 1475
29.1.70 Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_21)—Offset 4A8h 1475
29.1.71 Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_21)—Offset 4ACh 1475
29.1.72 Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_22)—Offset 4B0h 1475
29.1.73 Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_22)—Offset 4B4h 1475
29.1.74 Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_23)—Offset 4B8h 1475
29.1.75 Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_23)—Offset 4BCh 1476
29.1.76 Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_0)—Offset 4C0h 1476
29.1.77 Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_0)—Offset 4C4h 1476
29.1.78 Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_1)—Offset 4C8h 1476
29.1.79 Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_1)—Offset 4CCh 1476
29.1.80 Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_2)—Offset 4D0h 1476
29.1.81 Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_2)—Offset 4D4h 1476
29.1.82 Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_3)—Offset 4D8h 1476
29.1.83 Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_3)—Offset 4DCh 1477
29.1.84 Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_4)—Offset 4E0h 1477
29.1.85 Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_4)—Offset 4E4h 1477
29.1.86 Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_5)—Offset 4E8h 1477
29.1.87 Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_5)—Offset 4ECh 1477
29.1.88 Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_6)—Offset 4F0h 1477
29.1.89 Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_6)—Offset 4F4h 1477
29.1.90 Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_7)—Offset 4F8h 1477
29.1.91 Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_7)—Offset 4FCh 1478
29.1.92 Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_8)—Offset 500h 1478
29.1.93 Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_8)—Offset 504h 1478
29.1.94 Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_9)—Offset 508h 1478
29.1.95 Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_9)—Offset 50Ch 1478
29.1.96 Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_10)—Offset 510h 1478
29.1.97 Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_10)—Offset 514h 1478
29.1.98 Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_11)—Offset 518h 1478
29.1.99 Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_11)—Offset 51Ch 1479
29.1.100 Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_12)—Offset 520h 1479
29.1.101 Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_12)—Offset 524h 1479
29.1.102 Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_13)—Offset 528h 1479
29.1.103 Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_13)—Offset 52Ch 1479
29.1.104 Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_14)—Offset 530h 1479
29.1.105 Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_14)—Offset 534h 1479
29.1.106 Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_15)—Offset 538h 1480
29.1.107 Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_15)—Offset 53Ch 1480
29.1.108 Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_16)—Offset 540h 1480
29.1.109 Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_16)—Offset 544h 1480
29.1.110 Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_17)—Offset 548h 1480
29.1.111 Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_17)—Offset 54Ch 1480

29.1.112 Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_18)—Offset 550h 1480
29.1.113 Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_18)—Offset 554h 1480
29.1.114 Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_19)—Offset 558h 1481
29.1.115 Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_19)—Offset 55Ch 1481
29.1.116 Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_20)—Offset 560h 1481
29.1.117 Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_20)—Offset 564h 1481
29.1.118 Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_21)—Offset 568h 1481
29.1.119 Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_21)—Offset 56Ch 1481
29.1.120 Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_22)—Offset 570h 1481
29.1.121 Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_22)—Offset 574h 1481
29.1.122 Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_23)—Offset 578h 1482
29.1.123 Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_23)—Offset 57Ch 1482
29.2 GPIO Community 1 Registers Summary 1482
29.2.1 Family Base Address (FAMBAR)—Offset 8h 1489
29.2.2 Pad Base Address (PADBAR)—Offset Ch 1490
29.2.3 Miscellaneous Configuration (MISCCFG)—Offset 10h 1490
29.2.4 Pad Ownership (PAD_OWN_GPP_C_0)—Offset 20h 1491
29.2.5 Pad Ownership (PAD_OWN_GPP_C_1)—Offset 24h 1493
29.2.6 Pad Ownership (PAD_OWN_GPP_C_2)—Offset 28h 1493
29.2.7 Pad Ownership (PAD_OWN_GPP_D_0)—Offset 30h 1493
29.2.8 Pad Ownership (PAD_OWN_GPP_D_1)—Offset 34h 1493
29.2.9 Pad Ownership (PAD_OWN_GPP_D_2)—Offset 38h 1493
29.2.10 Pad Ownership (PAD_OWN_GPP_E_0)—Offset 40h 1493
29.2.11 Pad Ownership (PAD_OWN_GPP_E_1)—Offset 44h 1493
29.2.12 Pad Ownership (PAD_OWN_GPP_E_2)—Offset 48h 1493
29.2.13 Pad Configuration Lock (PADCFGLOCK_GPP_C)—Offset A0h 1493
29.2.14 Pad Configuration Lock (PADCFGLOCKTX_GPP_C)—Offset A4h 1495
29.2.15 Pad Configuration Lock (PADCFGLOCK_GPP_D)—Offset A8h 1497
29.2.16 Pad Configuration Lock (PADCFGLOCKTX_GPP_D)—Offset ACh 1497
29.2.17 Pad Configuration Lock (PADCFGLOCK_GPP_E)—Offset B0h 1497
29.2.18 Pad Configuration Lock (PADCFGLOCKTX_GPP_E)—Offset B4h 1497
29.2.19 Host Software Pad Ownership (HOSTSW_OWN_GPP_C)—Offset D0h 1497
29.2.20 Host Software Pad Ownership (HOSTSW_OWN_GPP_D)—Offset D4h 1499
29.2.21 Host Software Pad Ownership (HOSTSW_OWN_GPP_E)—Offset D8h 1499
29.2.22 GPI Interrupt Status (GPI_IS_GPP_C)—Offset 100h 1499
29.2.23 GPI Interrupt Status (GPI_IS_GPP_D)—Offset 104h 1501
29.2.24 GPI Interrupt Status (GPI_IS_GPP_E)—Offset 108h 1501
29.2.25 GPI Interrupt Enable (GPI_IE_GPP_C)—Offset 120h 1501
29.2.26 GPI Interrupt Enable (GPI_IE_GPP_D)—Offset 124h 1503
29.2.27 GPI Interrupt Enable (GPI_IE_GPP_E)—Offset 128h 1503
29.2.28 GPI General Purpose Events Status (GPI_GPE_STS_GPP_C)—Offset 140h ... 1503
29.2.29 GPI General Purpose Events Status (GPI_GPE_STS_GPP_D)—Offset 144h .. 1505
29.2.30 GPI General Purpose Events Status (GPI_GPE_STS_GPP_E)—Offset 148h ... 1505
29.2.31 GPI General Purpose Events Enable (GPI_GPE_EN_GPP_C)—Offset 160h 1505
29.2.32 GPI General Purpose Events Enable (GPI_GPE_EN_GPP_D)—Offset 164h 1507
29.2.33 GPI General Purpose Events Enable (GPI_GPE_EN_GPP_E)—Offset 168h 1507
29.2.34 SMI Status (GPI_SMI_STS_GPP_C)—Offset 180h 1507
29.2.35 SMI Status (GPI_SMI_STS_GPP_D)—Offset 184h 1508
29.2.36 SMI Status (GPI_SMI_STS_GPP_E)—Offset 188h 1509
29.2.37 SMI Enable (GPI_SMI_EN_GPP_C)—Offset 1A0h 1510
29.2.38 SMI Enable (GPI_SMI_EN_GPP_D)—Offset 1A4h 1511
29.2.39 SMI Enable (GPI_SMI_EN_GPP_E)—Offset 1A8h 1512
29.2.40 NMI Status (GPI_NMI_STS_GPP_C)—Offset 1C0h 1513
29.2.41 NMI Status (GPI_NMI_STS_GPP_D)—Offset 1C4h 1514
29.2.42 NMI Status (GPI_NMI_STS_GPP_E)—Offset 1C8h 1515

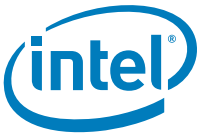
29.2.43 NMI Enable (GPI_NMI_EN_GPP_C)—Offset 1E0h 1516
29.2.44 NMI Enable (GPI_NMI_EN_GPP_D)—Offset 1E4h 1517
29.2.45 NMI Enable (GPI_NMI_EN_GPP_E)—Offset 1E8h 1518
29.2.46 PWM Control (PWMC)—Offset 204h 1519
29.2.47 GPIO Serial Blink Enable (GP_SER_BLINK)—Offset 20Ch 1519
29.2.48 GPIO Serial Blink Command/Status (GP_SER_CMDSTS)—Offset 210h 1520
29.2.49 GPIO Serial Blink Data (GP_SER_DATA)—Offset 214h 1521
29.2.50 Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_0)—Offset 400h 1521
29.2.51 Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_0)—Offset 404h 1524
29.2.52 Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_1)—Offset 408h 1524
29.2.53 Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_1)—Offset 40Ch 1524
29.2.54 Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_2)—Offset 410h 1525
29.2.55 Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_2)—Offset 414h 1525
29.2.56 Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_3)—Offset 418h 1525
29.2.57 Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_3)—Offset 41Ch 1525
29.2.58 Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_4)—Offset 420h 1525
29.2.59 Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_4)—Offset 424h 1525
29.2.60 Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_5)—Offset 428h 1525
29.2.61 Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_5)—Offset 42Ch 1525
29.2.62 Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_6)—Offset 430h 1525
29.2.63 Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_6)—Offset 434h 1526
29.2.64 Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_7)—Offset 438h 1526
29.2.65 Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_7)—Offset 43Ch 1526
29.2.66 Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_8)—Offset 440h 1526
29.2.67 Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_8)—Offset 444h 1526
29.2.68 Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_9)—Offset 448h 1526
29.2.69 Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_9)—Offset 44Ch 1526
29.2.70 Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_10)—Offset 450h 1526
29.2.71 Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_10)—Offset 454h 1526
29.2.72 Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_11)—Offset 458h 1527
29.2.73 Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_11)—Offset 45Ch 1527
29.2.74 Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_12)—Offset 460h 1527
29.2.75 Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_12)—Offset 464h 1527
29.2.76 Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_13)—Offset 468h 1527
29.2.77 Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_13)—Offset 46Ch 1527
29.2.78 Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_14)—Offset 470h 1527
29.2.79 Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_14)—Offset 474h 1527
29.2.80 Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_15)—Offset 478h 1527
29.2.81 Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_15)—Offset 47Ch 1528
29.2.82 Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_16)—Offset 480h 1528
29.2.83 Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_16)—Offset 484h 1528
29.2.84 Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_17)—Offset 488h 1529
29.2.85 Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_17)—Offset 48Ch 1529
29.2.86 Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_18)—Offset 490h 1529
29.2.87 Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_18)—Offset 494h 1529
29.2.88 Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_19)—Offset 498h 1529
29.2.89 Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_19)—Offset 49Ch 1530
29.2.90 Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_20)—Offset 4A0h 1530
29.2.91 Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_20)—Offset 4A4h 1530
29.2.92 Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_21)—Offset 4A8h 1530
29.2.93 Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_21)—Offset 4ACh 1530
29.2.94 Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_22)—Offset 4B0h 1530
29.2.95 Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_22)—Offset 4B4h 1530
29.2.96 Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_23)—Offset 4B8h 1530
29.2.97 Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_23)—Offset 4BCh 1530

29.2.98 Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_0)—Offset 4C0h 1531
29.2.99 Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_0)—Offset 4C4h 1531
29.2.100 Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_1)—Offset 4C8h 1531
29.2.101 Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_1)—Offset 4CCh 1531
29.2.102 Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_2)—Offset 4D0h 1531
29.2.103 Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_2)—Offset 4D4h 1531
29.2.104 Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_3)—Offset 4D8h 1531
29.2.105 Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_3)—Offset 4DCh 1531
29.2.106 Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_4)—Offset 4E0h 1531
29.2.107 Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_4)—Offset 4E4h 1532
29.2.108 Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_5)—Offset 4E8h 1532
29.2.109 Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_5)—Offset 4ECh 1532
29.2.110 Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_6)—Offset 4F0h 1532
29.2.111 Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_6)—Offset 4F4h 1532
29.2.112 Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_7)—Offset 4F8h 1532
29.2.113 Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_7)—Offset 4FCh 1532
29.2.114 Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_8)—Offset 500h 1532
29.2.115 Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_8)—Offset 504h 1532
29.2.116 Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_9)—Offset 508h 1533
29.2.117 Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_9)—Offset 50Ch 1533
29.2.118 Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_10)—Offset 510h 1533
29.2.119 Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_10)—Offset 514h 1533
29.2.120 Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_11)—Offset 518h 1533
29.2.121 Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_11)—Offset 51Ch 1533
29.2.122 Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_12)—Offset 520h 1533
29.2.123 Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_12)—Offset 524h 1533
29.2.124 Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_13)—Offset 528h 1533
29.2.125 Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_13)—Offset 52Ch 1534
29.2.126 Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_14)—Offset 530h 1534
29.2.127 Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_14)—Offset 534h 1534
29.2.128 Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_15)—Offset 538h 1534
29.2.129 Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_15)—Offset 53Ch 1534
29.2.130 Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_16)—Offset 540h 1534
29.2.131 Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_16)—Offset 544h 1534
29.2.132 Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_17)—Offset 548h 1534
29.2.133 Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_17)—Offset 54Ch 1534
29.2.134 Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_18)—Offset 550h 1535
29.2.135 Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_18)—Offset 554h 1535
29.2.136 Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_19)—Offset 558h 1535
29.2.137 Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_19)—Offset 55Ch 1535
29.2.138 Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_20)—Offset 560h 1535
29.2.139 Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_20)—Offset 564h 1535
29.2.140 Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_21)—Offset 568h 1535
29.2.141 Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_21)—Offset 56Ch 1535
29.2.142 Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_22)—Offset 570h 1535
29.2.143 Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_22)—Offset 574h 1536
29.2.144 Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_23)—Offset 578h 1536
29.2.145 Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_23)—Offset 57Ch 1536
29.2.146 Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_0)—Offset 580h 1536
29.2.147 Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_0)—Offset 584h 1536
29.2.148 Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_1)—Offset 588h 1536
29.2.149 Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_1)—Offset 58Ch 1536
29.2.150 Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_2)—Offset 590h 1536
29.2.151 Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_2)—Offset 594h 1536
29.2.152 Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_3)—Offset 598h 1537

29.2.153 Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_3)—Offset 59Ch 1537
29.2.154 Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_4)—Offset 5A0h 1537
29.2.155 Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_4)—Offset 5A4h 1537
29.2.156 Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_5)—Offset 5A8h 1537
29.2.157 Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_5)—Offset 5ACh 1537
29.2.158 Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_6)—Offset 5B0h 1537
29.2.159 Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_6)—Offset 5B4h 1537
29.2.160 Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_7)—Offset 5B8h 1537
29.2.161 Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_7)—Offset 5BCh 1538
29.2.162 Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_8)—Offset 5C0h 1538
29.2.163 Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_8)—Offset 5C4h 1538
29.2.164 Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_9)—Offset 5C8h 1538
29.2.165 Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_9)—Offset 5CCh 1538
29.2.166 Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_10)—Offset 5D0h 1538
29.2.167 Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_10)—Offset 5D4h 1538
29.2.168 Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_11)—Offset 5D8h 1538
29.2.169 Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_11)—Offset 5DCh 1538
29.2.170 Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_12)—Offset 5E0h 1539
29.2.171 Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_12)—Offset 5E4h 1539
29.2.172 Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_13)—Offset 5E8h 1539
29.2.173 Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_13)—Offset 5ECh 1539
29.2.174 Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_14)—Offset 5F0h 1539
29.2.175 Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_14)—Offset 5F4h 1539
29.2.176 Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_15)—Offset 5F8h 1539
29.2.177 Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_15)—Offset 5FCh 1539
29.2.178 Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_16)—Offset 600h 1539
29.2.179 Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_16)—Offset 604h 1540
29.2.180 Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_17)—Offset 608h 1540
29.2.181 Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_17)—Offset 60Ch 1540
29.2.182 Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_18)—Offset 610h 1540
29.2.183 Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_18)—Offset 614h 1540
29.2.184 Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_19)—Offset 618h 1540
29.2.185 Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_19)—Offset 61Ch 1540
29.2.186 Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_20)—Offset 620h 1540
29.2.187 Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_20)—Offset 624h 1540
29.2.188 Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_21)—Offset 628h 1541
29.2.189 Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_21)—Offset 62Ch 1541
29.2.190 Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_22)—Offset 630h 1541
29.2.191 Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_22)—Offset 634h 1541
29.2.192 Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_23)—Offset 638h 1541
29.2.193 Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_23)—Offset 63Ch 1541
29.3 GPIO Community 2 Registers Summary 1542
29.3.1 Family Base Address (FAMBAR)—Offset 8h 1543
29.3.2 Pad Base Address (PADBAR)—Offset Ch 1544
29.3.3 Miscellaneous Configuration (MISCCFG)—Offset 10h 1544
29.3.4 Pad Ownership (PAD_OWN_GPD_0)—Offset 20h 1546
29.3.5 Pad Ownership (PAD_OWN_GPD_1)—Offset 24h 1547
29.3.6 Pad Configuration Lock (PADCFGLOCK_GPD_0)—Offset A0h 1547
29.3.7 Pad Configuration Lock (PADCFGLOCKTX_GPD_0)—Offset A4h 1548
29.3.8 Host Software Pad Ownership (HOSTSW_OWN_GPD_0)—Offset D0h 1549
29.3.9 GPI Interrupt Status (GPI_IS_GPD_0)—Offset 100h 1551
29.3.10 GPI Interrupt Enable (GPI_IE_GPD_0)—Offset 120h 1552
29.3.11 GPI General Purpose Events Status (GPI_GPE_STS_GPD_0)—Offset 140h .. 1553
29.3.12 GPI General Purpose Events Enable (GPI_GPE_EN_GPD_0)—Offset 160h ... 1554
29.3.13 Pad Configuration DW0 (PAD_CFG_DW0_GPD_0)—Offset 400h 1555

29.3.14 Pad Configuration DW1 (PAD_CFG_DW1_GPD_0)—Offset 404h 1557
29.3.15 Pad Configuration DW0 (PAD_CFG_DW0_GPD_1)—Offset 408h 1558
29.3.16 Pad Configuration DW1 (PAD_CFG_DW1_GPD_1)—Offset 40Ch 1558
29.3.17 Pad Configuration DW0 (PAD_CFG_DW0_GPD_2)—Offset 410h 1558
29.3.18 Pad Configuration DW1 (PAD_CFG_DW1_GPD_2)—Offset 414h 1559
29.3.19 Pad Configuration DW0 (PAD_CFG_DW0_GPD_3)—Offset 418h 1559
29.3.20 Pad Configuration DW1 (PAD_CFG_DW1_GPD_3)—Offset 41Ch 1559
29.3.21 Pad Configuration DW0 (PAD_CFG_DW0_GPD_4)—Offset 420h 1559
29.3.22 Pad Configuration DW1 (PAD_CFG_DW1_GPD_4)—Offset 424h 1559
29.3.23 Pad Configuration DW0 (PAD_CFG_DW0_GPD_5)—Offset 428h 1559
29.3.24 Pad Configuration DW1 (PAD_CFG_DW1_GPD_5)—Offset 42Ch 1559
29.3.25 Pad Configuration DW0 (PAD_CFG_DW0_GPD_6)—Offset 430h 1559
29.3.26 Pad Configuration DW1 (PAD_CFG_DW1_GPD_6)—Offset 434h 1560
29.3.27 Pad Configuration DW0 (PAD_CFG_DW0_GPD_7)—Offset 438h 1560
29.3.28 Pad Configuration DW1 (PAD_CFG_DW1_GPD_7)—Offset 43Ch 1560
29.3.29 Pad Configuration DW0 (PAD_CFG_DW0_GPD_8)—Offset 440h 1560
29.3.30 Pad Configuration DW1 (PAD_CFG_DW1_GPD_8)—Offset 444h 1560
29.3.31 Pad Configuration DW0 (PAD_CFG_DW0_GPD_9)—Offset 448h 1560
29.3.32 Pad Configuration DW1 (PAD_CFG_DW1_GPD_9)—Offset 44Ch 1560
29.3.33 Pad Configuration DW0 (PAD_CFG_DW0_GPD_10)—Offset 450h 1560
29.3.34 Pad Configuration DW1 (PAD_CFG_DW1_GPD_10)—Offset 454h 1560
29.3.35 Pad Configuration DW0 (PAD_CFG_DW0_GPD_11)—Offset 458h 1561
29.3.36 Pad Configuration DW1 (PAD_CFG_DW1_GPD_11)—Offset 45Ch 1561
29.4 GPIO Community 3 Registers Summary 1561
29.4.1 Family Base Address (FAMBAR)—Offset 8h 1564
29.4.2 Pad Base Address (PADBAR)—Offset Ch 1565
29.4.3 Miscellaneous Configuration (MISCCFG)—Offset 10h 1565
29.4.4 Pad Ownership (PAD_OWN_GPP_F_0)—Offset 20h 1567
29.4.5 Pad Ownership (PAD_OWN_GPP_F_1)—Offset 24h 1568
29.4.6 Pad Ownership (PAD_OWN_GPP_F_2)—Offset 28h 1568
29.4.7 Pad Ownership (PAD_OWN_GPP_G_0)—Offset 30h 1568
29.4.8 Pad Configuration Lock (PADCFGLOCK_GPP_F)—Offset A0h 1569
29.4.9 Pad Configuration Lock (PADCFGLOCKTX_GPP_F)—Offset A4h 1571
29.4.10 Pad Configuration Lock (PADCFGLOCK_GPP_G)—Offset A8h 1573
29.4.11 Pad Configuration Lock (PADCFGLOCKTX_GPP_G)—Offset ACh 1573
29.4.12 Host Software Pad Ownership (HOSTSW_OWN_GPP_F)—Offset D0h 1573
29.4.13 Host Software Pad Ownership (HOSTSW_OWN_GPP_G)—Offset D4h 1575
29.4.14 GPI Interrupt Status (GPI_IS_GPP_F)—Offset 100h 1575
29.4.15 GPI Interrupt Status (GPI_IS_GPP_G)—Offset 104h 1577
29.4.16 GPI Interrupt Enable (GPI_IE_GPP_F)—Offset 120h 1577
29.4.17 GPI Interrupt Enable (GPI_IE_GPP_G)—Offset 124h 1578
29.4.18 GPI General Purpose Events Status (GPI_GPE_STS_GPP_F)—Offset 140h ... 1578
29.4.19 GPI General Purpose Events Status (GPI_GPE_STS_GPP_G)—Offset 144h .. 1580
29.4.20 GPI General Purpose Events Enable (GPI_GPE_EN_GPP_F)—Offset 160h 1580
29.4.21 GPI General Purpose Events Enable (GPI_GPE_EN_GPP_G)—Offset 164h 1582
29.4.22 Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_0)—Offset 400h 1582
29.4.23 Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_0)—Offset 404h 1584
29.4.24 Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_1)—Offset 408h 1585
29.4.25 Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_1)—Offset 40Ch 1585
29.4.26 Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_2)—Offset 410h 1585
29.4.27 Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_2)—Offset 414h 1585
29.4.28 Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_3)—Offset 418h 1585
29.4.29 Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_3)—Offset 41Ch 1586
29.4.30 Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_4)—Offset 420h 1586
29.4.31 Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_4)—Offset 424h 1586

29.4.32 Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_5)—Offset 428h 1586
29.4.33 Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_5)—Offset 42Ch 1586
29.4.34 Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_6)—Offset 430h 1586
29.4.35 Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_6)—Offset 434h 1586
29.4.36 Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_7)—Offset 438h 1586
29.4.37 Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_7)—Offset 43Ch 1586
29.4.38 Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_8)—Offset 440h 1587
29.4.39 Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_8)—Offset 444h 1587
29.4.40 Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_9)—Offset 448h 1587
29.4.41 Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_9)—Offset 44Ch 1587
29.4.42 Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_10)—Offset 450h 1587
29.4.43 Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_10)—Offset 454h 1587
29.4.44 Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_11)—Offset 458h 1587
29.4.45 Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_11)—Offset 45Ch 1587
29.4.46 Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_12)—Offset 460h 1587
29.4.47 Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_12)—Offset 464h 1588
29.4.48 Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_13)—Offset 468h 1588
29.4.49 Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_13)—Offset 46Ch 1588
29.4.50 Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_14)—Offset 470h 1588
29.4.51 Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_14)—Offset 474h 1588
29.4.52 Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_15)—Offset 478h 1588
29.4.53 Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_15)—Offset 47Ch 1588
29.4.54 Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_16)—Offset 480h 1588
29.4.55 Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_16)—Offset 484h 1588
29.4.56 Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_17)—Offset 488h 1589
29.4.57 Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_17)—Offset 48Ch 1589
29.4.58 Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_18)—Offset 490h 1589
29.4.59 Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_18)—Offset 494h 1589
29.4.60 Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_19)—Offset 498h 1589
29.4.61 Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_19)—Offset 49Ch 1589
29.4.62 Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_20)—Offset 4A0h 1589
29.4.63 Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_20)—Offset 4A4h 1589
29.4.64 Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_21)—Offset 4A8h 1589
29.4.65 Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_21)—Offset 4ACh 1590
29.4.66 Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_22)—Offset 4B0h 1590
29.4.67 Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_22)—Offset 4B4h 1590
29.4.68 Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_23)—Offset 4B8h 1590
29.4.69 Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_23)—Offset 4BCh 1590
29.4.70 Pad Configuration DW0 (PAD_CFG_DW0_GPP_G_0)—Offset 4C0h 1590
29.4.71 Pad Configuration DW1 (PAD_CFG_DW1_GPP_G_0)—Offset 4C4h 1592
29.4.72 Pad Configuration DW0 (PAD_CFG_DW0_GPP_G_1)—Offset 4C8h 1592
29.4.73 Pad Configuration DW1 (PAD_CFG_DW1_GPP_G_1)—Offset 4CCh 1592
29.4.74 Pad Configuration DW0 (PAD_CFG_DW0_GPP_G_2)—Offset 4D0h 1593
29.4.75 Pad Configuration DW1 (PAD_CFG_DW1_GPP_G_2)—Offset 4D4h 1593
29.4.76 Pad Configuration DW0 (PAD_CFG_DW0_GPP_G_3)—Offset 4D8h 1593
29.4.77 Pad Configuration DW1 (PAD_CFG_DW1_GPP_G_3)—Offset 4DCh 1593
29.4.78 Pad Configuration DW0 (PAD_CFG_DW0_GPP_G_4)—Offset 4E0h 1593
29.4.79 Pad Configuration DW1 (PAD_CFG_DW1_GPP_G_4)—Offset 4E4h 1593
29.4.80 Pad Configuration DW0 (PAD_CFG_DW0_GPP_G_5)—Offset 4E8h 1593
29.4.81 Pad Configuration DW1 (PAD_CFG_DW1_GPP_G_5)—Offset 4ECh 1593
29.4.82 Pad Configuration DW0 (PAD_CFG_DW0_GPP_G_6)—Offset 4F0h 1593
29.4.83 Pad Configuration DW1 (PAD_CFG_DW1_GPP_G_6)—Offset 4F4h 1594
29.4.84 Pad Configuration DW0 (PAD_CFG_DW0_GPP_G_7)—Offset 4F8h 1594
29.4.85 Pad Configuration DW1 (PAD_CFG_DW1_GPP_G_7)—Offset 4FCh 1594



30 High Precision Event Timer (HPET) 1595
30.1 HPET Memory Mapped Registers Summary 1595
30.1.1 General Capabilities and ID Register (GEN_CAP_ID)—Offset 0h 1595
30.1.2 General Config Register (GEN_CFG)—Offset 10h 1596
30.1.3 General Interrupt Status Register (GEN_INT_STS)—Offset 20h 1597
30.1.4 Main Counter Value (MAIN_CNTR)—Offset F0h 1598
30.1.5 Timer n Config and Capabilities (TMRn_CNF_CAP)—Offset 100h 1599
30.1.6 Timer n Comparator Value (TMRn_CMP_VAL)—Offset 108h 1601

31 Integrated Clock (ICC) 1603
31.1 Integrated Clock Controller FW Accessible Registers Summary 1603
31.1.1 Timing Control SRC Clock (TMCSRCCLK)—Offset 1000h 1603
31.1.2 Timing Control SRC Clock Register 2 (TMCSRCCLK2)—Offset 1004h 1606
31.1.3 Enable Control CLKREQ (ENCCKRQ)—Offset 1008h 1606
31.1.4 Mask Control CLKREQ (MSKCKRQ)—Offset 100Ch 1608
31.1.5 ICC Security (ICCSEC)—Offset 1020h 1609
31.1.6 CLKREQ Mapping to CLKOUT_SRC (CKRQMAPSRC)—Offset 1024h 1611
31.1.7 CLKREQ Mapping to CLKOUT_SRC Register 2 (CKRQMAPSRC2)—Offset 1028h ... 1613
31.1.8 Power Management (PM)—Offset 102Ch 1615
31.1.9 ICC Debug (ICCDBG)—Offset 1034h 1616
31.1.10 USB3Gen2PCIe PLL Control (G2PLLCTRL)—Offset 2000h 1616

32 Interrupt 1619
32.1 Interrupt Registers Summary 1619
32.1.1 Master Initialization Command Word 1 (MICW1)—Offset 20h 1619
32.1.2 Master Operational Control Word 2 (MOCW2)—Offset 20h 1620
32.1.3 Master Operational Control Word 3 (MOCW3)—Offset 20h 1621
32.1.4 Master Initialization Command Word 2 (MICW2)—Offset 21h 1622
32.1.5 Master Initialization Command Word 3 (MICW3)—Offset 21h 1623
32.1.6 Master Initialization Command Word 4 (MICW4)—Offset 21h 1623
32.1.7 Master Operational Control Word 1 (MOCW1)—Offset 21h 1624
32.1.8 Slave Initialization Command Word 1 (SICW1)—Offset A0h 1624
32.1.9 Slave Operational Control Word 2 (SOCW2)—Offset A0h 1625
32.1.10 Slave Operational Control Word 3 (SOCW3)—Offset A0h 1626
32.1.11 Slave Initialization Command Word 2 (SICW2)—Offset A1h 1627
32.1.12 Slave Initialization Command Word 3 (SICW3)—Offset A1h 1628
32.1.13 Slave Initialization Command Word 4 (SICW4)—Offset A1h 1628
32.1.14 Slave Operational Control Word 1 (SOCW1)—Offset A1h 1629
32.1.15 Master Edge/Level Control (ELCR1)—Offset 4D0h 1629
32.1.16 Slave Edge/Level Control (ELCR2)—Offset 4D1h 1630
32.2 Interrupt PCR Registers Summary 1630
32.2.1 PIRQA Routing Control (PARC)—Offset 3100h 1631
32.2.2 PIRQB Routing Control (PBRC)—Offset 3101h 1632
32.2.3 PIRQC Routing Control (PCRC)—Offset 3102h 1632
32.2.4 PIRQD Routing Control (PDRC)—Offset 3103h 1633
32.2.5 PIRQE Routing Control (PERC)—Offset 3104h 1633
32.2.6 PIRQF Routing Control (PFRC)—Offset 3105h 1634
32.2.7 PIRQG Routing Control (PGRC)—Offset 3106h 1635
32.2.8 PIRQH Routing Control (PHRC)—Offset 3107h 1635
32.2.9 General Interrupt Control (GIC)—Offset 31FCh 1636
32.2.10 Interrupt Polarity Control 0 (IPC0)—Offset 3200h 1637
32.2.11 Interrupt Polarity Control 1 (IPC1)—Offset 3204h 1637
32.2.12 Interrupt Polarity Control 2 (IPC2)—Offset 3208h 1638
32.2.13 Interrupt Polarity Control 3 (IPC3)—Offset 320Ch 1638
32.2.14 ITSS Power Reduction Control (ITSSPRC)—Offset 3300h 1639

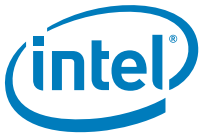
32.2.15 Master Message Control (MMC)—Offset 3334h 1640

33 Real Time Clock (RTC) 1641
33.1 Registers Summary 1641
33.1.1 Seconds (Sec)—Offset 0h 1642
33.1.2 Seconds Alarm (Sec_Alarm)—Offset 1h 1642
33.1.3 Minutes (Minutes)—Offset 2h 1642
33.1.4 Minutes Alarm (Minutes_Alarm)—Offset 3h 1642
33.1.5 Hours (Hours)—Offset 4h 1642
33.1.6 Hours Alarm (Hours_Alarm)—Offset 5h 1642
33.1.7 Day of Week (Day_of_Week)—Offset 6h 1642
33.1.8 Day of Month (Day_of_Month)—Offset 7h 1642
33.1.9 Month (Month)—Offset 8h 1642
33.1.10 Year (Year)—Offset 9h 1642
33.1.11 Register A (RTC_REGA)—Offset Ah 1643
33.1.12 Register B - General Configuration (Register_B)—Offset Bh 1643
33.1.13 Register C - Flag Register (Register_C)—Offset Ch 1644
33.1.14 Register D - Flag Register (Register_D)—Offset Dh 1645
33.2 RTC PCR Registers Summary 1646
33.2.1 RTC Configuration (RC)—Offset 3400h 1646
33.2.2 Backed Up Control (BUC)—Offset 3414h 1647
33.2.3 RTC Update In Progress SMI Control (UIPSMI)—Offset 3F04h 1648

34 System Management TCO 1650
34.1 SMBus TCO I/O Registers Summary 1650
34.1.1 TCO_RLD Register (TRLD)—Offset 0h 1650
34.1.2 TCO_DAT_IN Register (TDI)—Offset 2h 1651
34.1.3 TCO_DAT_OUT Register (TDO)—Offset 3h 1651
34.1.4 TCO1_STS Register (TSTS1)—Offset 4h 1651
34.1.5 TCO2_STS Register (TSTS2)—Offset 6h 1653
34.1.6 TCO1_CNT Register (TCTL1)—Offset 8h 1654
34.1.7 TCO2_CNT Register (TCTL2)—Offset Ah 1655
34.1.8 TCO_MESSAGE1 and TCO_MESSAGE2 (TMSG)—Offset Ch 1656
34.1.9 TCO_WDSTATUS Register (TWDS)—Offset Eh 1656
34.1.10 LEGACY_ELIM Register (LE)—Offset 10h 1657
34.1.11 TCO_TMR Register (TTMR)—Offset 12h 1657

35 Additional Configuration Registers 1659
35.1 FIA Configuration PCR Registers Summary 1659
35.1.1 Common Control (CC)—Offset 0h 1659
35.1.2 Device Reference Clock Request Mapping 1 (DRCRM1)—Offset 100h 1660
35.1.3 Device Reference Clock Request Mapping 2 (DRCRM2)—Offset 104h 1662
35.1.4 Device Reference Clock Request Mapping 3 (DRCRM3)—Offset 108h 1663
35.1.5 Strap Configuration 1 (STRPFUSECFG1)—Offset 200h 1664
35.1.6 HSIO Lane Owner Status 1 (LOS1)—Offset 250h 1665
35.1.7 HSIO Lane Owner Status 2 (LOS2)—Offset 254h 1666
35.1.8 HSIO Lane Owner Status 3 (LOS3)—Offset 258h 1667
35.1.9 Lane Owner Status 4 (LOS4)—Offset 25Ch 1668
35.2 OPI PCR Registers Summary 1669
35.2.1 Target Link Speed (TLS)—Offset 0h 1670
35.2.2 Virtual Channel 0 Resource Control (V0CTL)—Offset 2014h 1671
35.2.3 Virtual Channel 0 Resource Status (V0STS)—Offset 2018h 1672
35.2.4 Virtual Channel 1 Resource Control (V1CTL)—Offset 2020h 1672
35.2.5 Virtual Channel 1 Resource Status (V1STS)—Offset 2024h 1673
35.2.6 ME Virtual Channel (VCm) Resource Control (VMCTL)—Offset 2040h 1674
35.2.7 ME Virtual Channel (VCm) Resource Status (VMSTS)—Offset 2046h 1674

35.2.8 Uncorrectable Error Status (UES)—Offset 2084h 1675
35.2.9 Uncorrectable Error Mask (UEM)—Offset 2088h 1676
35.2.10 Uncorrectable Error Severity (UEV)—Offset 208Ch 1677
35.2.11 Correctable Error Status (CES)—Offset 2090h 1678
35.2.12 Correctable Error Mask (CEM)—Offset 2094h 1679
35.2.13 Root Error Command (REC)—Offset 20ACh 1680
35.2.14 Root Error Status (RES)—Offset 20B0h 1680
35.2.15 Error Source Identification (ESID)—Offset 20B4h 1681
35.2.16 DMI Control Register (DMIC)—Offset 2234h 1682
35.2.17 IOSF Primary Control And Status (IPCS_IOSFSBCS)—Offset 223Ch 1682
35.2.18 DMI Port Link Control (DMILINKC)—Offset 2304h 1683
35.2.19 DMI PLL Shutdown (DMIPLLDOWN)—Offset 2320h 1683
35.2.20 DMI Power Management Control (DMIPMCTL)—Offset 2334h 1683
35.2.21 Link Configuration (LCFG)—Offset 2618h 1683
35.2.22 Thermal Throttling BIOS Assigned Thermal Base Address (TTTBARB)—Offset 2724h 1684
35.2.23 Thermal Throttling BIOS Assigned Thermal Base High Address (TTTBARBH)—Offset 2728h 1684
35.2.24 LPC Generic I/O Range 1 (LPCLGIR1)—Offset 2730h 1685
35.2.25 LPC Generic I/O Range 2 (LPCLGIR2)—Offset 2734h 1686
35.2.26 LPC Generic I/O Range 3 (LPCLGIR3)—Offset 2738h 1686
35.2.27 LPC Generic I/O Range 4 (LPCLGIR4)—Offset 273Ch 1686
35.2.28 LPC Generic Memory Range (LPCGMR)—Offset 2740h 1686
35.2.29 LPC BIOS Decode Enable (LPCBDE)—Offset 2744h 1686
35.2.30 uCode Patch Region (UCPR)—Offset 2748h 1689
35.2.31 General Control and Status (GCS)—Offset 274Ch 1689
35.2.32 I/O Trap Register 1 low (IOT1_LOW)—Offset 2750h 1690
35.2.33 I/O Trap Register 1 high (IOT1_HIGH)—Offset 2754h 1691
35.2.34 I/O Trap Register 2 low (IOT2_LOW)—Offset 2758h 1691
35.2.35 I/O Trap Register 2 high (IOT2_HIGH)—Offset 275Ch 1691
35.2.36 I/O Trap Register 3 low (IOT3_LOW)—Offset 2760h 1691
35.2.37 I/O Trap Register 3 high (IOT3_HIGH)—Offset 2764h 1692
35.2.38 I/O Trap Register 4 low (IOT4_LOW)—Offset 2768h 1692
35.2.39 I/O Trap Register 4 high (IOT4_HIGH)—Offset 276Ch 1692
35.2.40 LPC I/O Decode Range (LPCIOD)—Offset 2770h 1692
35.2.41 LPC I/O Enable (LPCIOE)—Offset 2774h 1693
35.2.42 TCO Base Address (TCOBASE)—Offset 2778h 1694
35.2.43 PM Base Address (PMBASEA)—Offset 27ACh 1695
35.2.44 PM Base Control (PMBASEC)—Offset 27B0h 1695
35.2.45 ACPI Base Address (ACPIBA)—Offset 27B4h 1696
35.2.46 ACPI Base Destination ID (ACPIBDID)—Offset 27B8h 1697
35.3 DCI PCR Registers Summary 1698
35.3.1 DCI Control Register (ECTRL)—Offset 4h 1698
35.4 PSF1 PCR Registers Summary 1699
35.4.1 PCI Base Address (PSF1_T0_SHDW_GBE_REG_BASE)—Offset 200h 1700
35.4.2 D31:F6 Function Disable (PSF_1_AGNT_T0_SHDW_PCIEN_GBE_RS0_D31_F6_OFFSET2)—Offset 21Ch 1701
35.4.3 PCI Base Address (PSF1_T0_SHDW_CAM_REG_BASE)—Offset 300h 1701
35.4.4 D20:F3 Function Disable (PSF_1_AGNT_T0_SHDW_PCIEN_CAM_RS0_D20_F3)—Offset 31Ch 1702
35.4.5 D20:F3 PCI Configuration Disable (PSF_1_AGNT_T0_SHDW_CFG_DIS_CAM_RS0_D20_F3_OFFSET3)—Offset 338h 1702



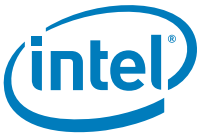
35.4.6 Function Disable (PSF_1_AGNT_T0_SHDW_PCIEN_CSE_RS0_D18_F4_OFFSET4)—Offset 41Ch.... 1703
35.4.7 D22:F2 Function Disable (PSF_1_AGNT_T0_SHDW_PCIEN_CSE_RS0_D22_F2)—Offset 61Ch 1704
35.4.8 D22:F4 Function Disable (PSF_1_AGNT_T0_SHDW_PCIEN_CSE_RS0_D22_F4)—Offset 71Ch 1704
35.4.9 D22:F1 Function Disable (PSF_1_AGNT_T0_SHDW_PCIEN_CSE_RS0_D22_F1)—Offset 81Ch 1705
35.4.10 D22:F0 Function Disable (PSF_1_AGNT_T0_SHDW_PCIEN_CSE_RS0_D22_F0_OFFSET10)—Offset A1Ch.. 1705
35.4.11 Offset 0B1Ch: PCI Configuration space enable bits (PSF_1_AGNT_T0_SHDW_PCIEN_PTIO_RS0_D22_F3_OFFSET11)—Offset B1Ch. 1706
35.4.12 Offset 0C1Ch: PCI Configuration space enable bits (PSF_1_AGNT_T0_SHDW_PCIEN_PTIO_RS0_D22_F2_OFFSET12)—Offset C1Ch. 1707
35.4.13 PCI Base Address (PSF1_T0_SHDW_SATA_REG_BASE)—Offset 1000h..... 1707
35.4.14 D23:F0 PCI Configuration Space Enable (PSF_1_AGNT_T0_SHDW_PCIEN_VR_RS0_D23_F0_OFFSET16)—Offset 101Ch.. 1708
35.4.15 PCIe Port12 PCI Configuration Space Enable (PSF_1_AGNT_T1_SHDW_PCIEN_SPC_RS0_D29_F3)—Offset 203Ch 1708
35.4.16 PCIe Port11 PCI Configuration Space Enable (PSF_1_AGNT_T1_SHDW_PCIEN_SPC_RS0_D29_F2)—Offset 213Ch 1709
35.4.17 PCIe Port10 PCI Configuration Space Enable (PSF_1_AGNT_T1_SHDW_PCIEN_SPC_RS0_D29_F1)—Offset 223Ch 1709
35.4.18 PCIe Port 9 PCI Configuration Space Enable (PSF_1_AGNT_T1_SHDW_PCIEN_SPC_RS0_D29_F0)—Offset 233Ch 1709
35.4.19 PCIe Port 8 PCI Configuration Space Enable (PSF_1_AGNT_T1_SHDW_PCIEN_SPB_RS0_D28_F7)—Offset 243Ch 1710
35.4.20 PCIe Port 7 PCI Configuration Space Enable (PSF_1_AGNT_T1_SHDW_PCIEN_SPB_RS0_D28_F6)—Offset 253Ch 1710
35.4.21 PCIe Port 6 PCI Configuration Space Enable (PSF_1_AGNT_T1_SHDW_PCIEN_SPB_RS0_D28_F5)—Offset 263Ch 1710
35.4.22 PCIe Port 5 PCI Configuration Space Enable (PSF_1_AGNT_T1_SHDW_PCIEN_SPB_RS0_D28_F4)—Offset 273Ch 1710
35.4.23 PCIe Port 4 PCI Configuration Space Enable (PSF_1_AGNT_T1_SHDW_PCIEN_SPA_RS0_D28_F3)—Offset 283Ch 1710
35.4.24 PCIe Port 3 PCI Configuration Space Enable (PSF_1_AGNT_T1_SHDW_PCIEN_SPA_RS0_D28_F2)—Offset 293Ch 1710
35.4.25 PCIe Port 2 PCI Configuration Space Enable (PSF_1_AGNT_T1_SHDW_PCIEN_SPA_RS0_D28_F1)—Offset 2A3Ch 1710
35.4.26 PCIe Port 1 PCI Configuration Space Enable (PSF_1_AGNT_T1_SHDW_PCIEN_SPA_RS0_D28_F0)—Offset 2B3Ch 1711
35.4.27 PSF Global Configuration (PSF_1_PSF_GLOBAL_CONFIG)—Offset 4000h 1711
35.4.28 Rootspace Configuration (PSF_1_ROOTSPACE_CONFIG_RS0)—Offset 4010h 1711
35.4.29 Rootspace Configuration (PSF_1_ROOTSPACE_CONFIG_RS1)—Offset 4014h 1712
35.4.30 Offset 4018h: PSF Port Configuration Register (PSF_1_PSF_PORT_CONFIG_PG0_PORT0)—Offset 4018h..... 1713
35.4.31 PSF Port Configuration (PSF_1_PSF_PORT_CONFIG_PG1_PORT7)—Offset 403Ch 1713
35.4.32 Multicast Control Register (PSF_1_PSF_MC_CONTROL_MCAST0_RS0_EOI)—Offset 4050h 1713

35.4.33 Destination ID (PSF_1_PSF_MC_AGENT_MCAST0_RS0_TGT0_EOI)—Offset 4060h 1713
35.4.34 PCI Function Configuration Header (PSF_1_T1_AGENT_FUNCTION_CONFIG_SPA_RS0_D28_F0)—Offset 4198h 1714
35.4.35 Grant Count Reload (PSF_1_DEV_GNTCNT_RELOAD_DGCR0)—Offset 41CCh 1715
35.5 PSF2 PCR Registers Summary 1716
35.5.1 D20:F2 Function Disable (PSF_2_AGNT_T0_SHDW_PCIEN_TRH_RS0_D20_F2_OFFSET1)—Offset 11Ch 1716
35.5.2 D20:F2 PCI Configuration Disable (PSF_2_AGNT_T0_SHDW_CFG_DIS_TRH_RS0_D20_F2_OFFSET1)—Offset 138h 1717
35.5.3 D30:F7 Function Disable (PSF_2_AGNT_T0_SHDW_PCIEN_SCC_RS0_D30_F7_OFFSET2)—Offset 21Ch 1717
35.5.4 PCI Base Address (PSF2_T0_SHDW_SDCARD_REG_BASE)—Offset 300h 1718
35.5.5 D30:F6 Function Disable (PSF_2_AGNT_T0_SHDW_PCIEN_SCC_RS0_D30_F6_OFFSET3)—Offset 31Ch 1719
35.5.6 D30:F5 Function Disable (PSF_2_AGNT_T0_SHDW_PCIEN_SCC_RS0_D30_F5_OFFSET4)—Offset 41Ch 1719
35.5.7 PCI Base Address (PSF2_T0_SHDW_EMMC_REG_BASE)—Offset 500h 1720
35.5.8 D30:F4 Function Disable (PSF_2_AGNT_T0_SHDW_PCIEN_SCC_RS0_D30_F4_OFFSET5)—Offset 51Ch 1720
35.5.9 PCI Base Address (PSF2_T0_SHDW_OTG_REG_BASE)—Offset 600h 1721
35.5.10 D20:F1 Function Disable (PSF_2_AGNT_T0_SHDW_PCIEN_OTG_RS0_D20_F1_OFFSET6)—Offset 61Ch.... 1721
35.5.11 D20:F0 Function Disable (PSF_2_AGNT_T0_SHDW_PCIEN_XHCI_RS0_D20_F0_OFFSET7)—Offset 71Ch... 1722
35.5.12 PSF Global Configuration (PSF_2_PSF_GLOBAL_CONFIG)—Offset 4000h ... 1723
35.5.13 Rootspace Configuration (PSF_2_ROOTSPACE_CONFIG_RS0)—Offset 4010h..... 1723
35.5.14 Rootspace Configuration (PSF_2_ROOTSPACE_CONFIG_RS1)—Offset 4014h..... 1724
35.6 PSF3 PCR Registers Summary 1725
35.6.1 PCI Base Address (PSF3_T0_SHDW_TRACE_HUB_ACPI_REG_BASE)—Offset 200h 1727
35.6.2 Offset 021Ch: PCI Configuration space enable bits (PSF_3_AGNT_T0_SHDW_PCIEN_NPK_RS0_D20_F4_OFFSET2)—Offset 21Ch 1728
35.6.3 Intel Trace Hub PCI Configuration Disable (PSF_3_AGNT_T0_SHDW_CFG_DIS_NPK_RS0_D20_F4_OFFSET2)—Offset 238h 1728
35.6.4 PCI Base Address (PSF3_T0_SHDW_TRACE_HUB_REG_BASE)—Offset 300h 1729
35.6.5 D31:F7 PCI Configuration Space Enable (PSF_3_AGNT_T0_SHDW_PCIEN_NPK_RS0_D31_F7_OFFSET3)—Offset 31Ch 1729
35.6.6 PCI Configuration Disable (PSF_3_AGNT_T0_SHDW_CFG_DIS_NPK_RS0_D31_F7_OFFSET3)—Offset 338h 1730
35.6.7 PCI Configuration Space Enable (PSF_3_AGNT_T0_SHDW_PCIEN_SMB_RS0_D31_F4_OFFSET5)—Offset 51Ch ... 1730

35.6.8 PCI Configuration Disable (PSF_3_AGNT_T0_SHDW_CFG_DIS_SMB_RS0_D31_F4_OFFSET5)—Offset 538h 1731
35.6.9 PCI Base Address (PSF3_T0_SHDW_ISH_REG_BASE)—Offset 800h..... 1732
35.6.10 D19:F0 Function Disable (PSF_3_AGNT_T0_SHDW_PCIEN_ISH_RS0_D19_F0_OFFSET8)—Offset 81Ch 1732
35.6.11 PCI Base Address (PSF3_T0_SHDW_I2C4_REG_BASE)—Offset 900h 1733
35.6.12 D25:F2 Function Disable (SF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D25_F2_OFFSET9)—Offset 91Ch.... 1733
35.6.13 Offset 0938h: PCI Configuration Disable (PSF_3_AGNT_T0_SHDW_CFG_DIS_LPSS_RS0_D25_F2_OFFSET9)—Offset 938h 1734
35.6.14 PCI Base Address (PSF3_T0_SHDW_GSPI1_REG_BASE)—Offset A00h 1734
35.6.15 D30:F3 Function Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D30_F3_OFFSET10)—Offset A1Ch 1735
35.6.16 Offset 0A38h: PCI Configuration Disable (PSF_3_AGNT_T0_SHDW_CFG_DIS_LPSS_RS0_D30_F3_OFFSET10)—Offset A38h 1735
35.6.17 PCI Base Address (PSF3_T0_SHDW_SPI0_REG_BASE)—Offset B00h 1736
35.6.18 Function Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D30_F2_OFFSET11)—Offset B1Ch 1736
35.6.19 Offset 0B38h: PCI Configuration Disable (PSF_3_AGNT_T0_SHDW_CFG_DIS_LPSS_RS0_D30_F2_OFFSET11)—Offset B38h 1737
35.6.20 PCI Base Address (PSF3_T0_SHDW_UART1_REG_BASE)—Offset C00h 1738
35.6.21 D30:F1 Function Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D30_F1_OFFSET12)—Offset C1Ch 1738
35.6.22 Offset 0C38h: PCI Configuration Disable (PSF_3_AGNT_T0_SHDW_CFG_DIS_LPSS_RS0_D30_F1_OFFSET12)—Offset C38h 1739
35.6.23 PCI Base Address (PSF3_T0_SHDW_UART0_REG_BASE)—Offset D00h 1739
35.6.24 D30:F0 Function Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D30_F0_OFFSET13)—Offset D1Ch 1740
35.6.25 Offset 0D38h: PCI Configuration Disable (PSF_3_AGNT_T0_SHDW_CFG_DIS_LPSS_RS0_D30_F0_OFFSET13)—Offset D38h 1740
35.6.26 PCI Base Address (PSF3_T0_SHDW_I2C5_REG_BASE)—Offset E00h 1741
35.6.27 D25:F1 Function Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D25_F1_OFFSET14)—Offset E1Ch 1741
35.6.28 Offset 0E38h: PCI Configuration Disable (PSF_3_AGNT_T0_SHDW_CFG_DIS_LPSS_RS0_D25_F1_OFFSET14)—Offset E38h 1742
35.6.29 PCI Base Address (PSF3_T0_SHDW_UART2_REG_BASE)—Offset F00h..... 1743
35.6.30 D25:F0 Function Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D25_F0_OFFSET15)—Offset F1Ch. 1743
35.6.31 Offset 0F38h: PCI Configuration Disable (PSF_3_AGNT_T0_SHDW_CFG_DIS_LPSS_RS0_D25_F0_OFFSET15)—Offset F38h..... 1744
35.6.32 PCI Base Address (PSF3_T0_SHDW_I2C3_REG_BASE)—Offset 1000h 1744

35.6.33 D21:F3 Function Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D21_F3_OFFSET16)—Offset 101Ch 1745
35.6.34 Offset 1038h: PCI Configuration Disable (PSF_3_AGNT_T0_SHDW_CFG_DIS_LPSS_RS0_D21_F3_OFFSET16)—Offset 1038h 1745
35.6.35 PCI Base Address (PSF3_T0_SHDW_I2C2_REG_BASE)—Offset 1100h 1746
35.6.36 D21:F2 Function Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D21_F2_OFFSET17)—Offset 111Ch 1746
35.6.37 Offset 1138h: PCI Configuration Disable (PSF_3_AGNT_T0_SHDW_CFG_DIS_LPSS_RS0_D21_F2_OFFSET17)—Offset 1138h 1747
35.6.38 PCI Base Address (PSF3_T0_SHDW_I2C1_REG_BASE)—Offset 1200h 1748
35.6.39 D21:F1 Function Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D21_F1_OFFSET18)—Offset 121Ch 1748
35.6.40 Offset 1238h: PCI Configuration Disable (PSF_3_AGNT_T0_SHDW_CFG_DIS_LPSS_RS0_D21_F1_OFFSET18)—Offset 1238h 1749
35.6.41 PCI Base Address (PSF3_T0_SHDW_I2C0_REG_BASE)—Offset 1300h 1749
35.6.42 D21:F0 Function Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D21_F0_OFFSET19)—Offset 131Ch 1750
35.6.43 Offset 1338h: PCI Configuration Disable (PSF_3_AGNT_T0_SHDW_CFG_DIS_LPSS_RS0_D21_F0_OFFSET19)—Offset 1338h 1750
35.6.44 Function Disable (PSF_3_AGNT_T0_SHDW_PCIEN_SPI_RS0_D31_F0_OFFSET23)—Offset 171Ch . 1751
35.6.45 PCI Base Address (PSF3_T0_SHDW_AUD_REG_BASE)—Offset 1900h 1752
35.6.46 PCI Configuration Space Enable (PSF_3_AGNT_T0_SHDW_PCIEN_AUD_RS0_D31_F3_OFFSET25)—Offset 191Ch 1752
35.6.47 PSF Global Configuration (PSF_3_PSF_GLOBAL_CONFIG)—Offset 4000h 1753
35.6.48 Root Space Config (PSF_3_ROOTSPACE_CONFIG_RS0)—Offset 4010h 1753
35.6.49 Rootspace Configuration (PSF_3_ROOTSPACE_CONFIG_RS1)—Offset 4014h..... 1754
35.6.50 Multicast Control (PSF_3_PSF_MC_CONTROL_MCAST0_RS0_EOI)—Offset 404Ch 1755
35.6.51 Destination ID (PSF_3_PSF_MC_AGENT_MCAST0_RS0_TGT0_EOI)—Offset 4054h 1755
35.7 PSF4 PCR Registers Summary 1756
35.7.1 PSF Global Configuration (PSF_4_PSF_GLOBAL_CONFIG)—Offset 4000h 1756
35.7.2 Root Space Configuration (PSF_4_ROOTSPACE_CONFIG_RS0)—Offset 4010h 1757
35.7.3 Root Space Configuration (PSF_4_ROOTSPACE_CONFIG_RS1)—Offset 4014h 1757
35.8 IO Trap Registers Summary 1758
35.8.1 PSTH Control Register (PSTHCTL)—Offset 1D00h 1759
35.8.2 Trap Status Register (TRPSTS)—Offset 1E00h..... 1759
35.8.3 Trapped Cycle Register (TRPCYC1)—Offset 1E10h 1760
35.8.4 Trapped Write Data Register (TRPWRDATA1)—Offset 1E18h 1760
35.8.5 I/O Trap Registers 1 (IOTRP1_1)—Offset 1E80h..... 1761
35.8.6 I/O Trap Registers 1 (IOTRP1_2)—Offset 1E84h..... 1762
35.8.7 I/O Trap Registers 2 (IOTRP2_1)—Offset 1E88h..... 1762
35.8.8 I/O Trap Registers 2 (IOTRP2_2)—Offset 1E8Ch 1763

35.8.9 I/O Trap Registers 3 (IOTRP3_1)—Offset 1E90h 1764
35.8.10 I/O Trap Registers 3 (IOTRP3_2)—Offset 1E94h 1765
35.8.11 I/O Trap Registers 4 (IOTRP4_1)—Offset 1E98h 1765
35.8.12 I/O Trap Registers 4 (IOTRP4_2)—Offset 1E9Ch 1766



Tables

2-1 Summary of LPC Configuration Registers 66
2-2 Summary of LPC PCR Registers..... 82
3-1 Summary of Enhanced SPI (eSPI) Configuration Registers..... 83
3-2 Summary of eSPI PCR Registers 98
4-1 Summary of P2SB Configuration Registers 108
5-1 Summary of Power Management Configuration Registers 131
5-2 Summary of PMC I/O Based Registers 145
5-3 Summary of PMC Memory Mapped Registers 165
6-1 Summary of Intel® High Definition Audio (D31:F3) PCI Configuration Registers.....214
7-1 Summary of SMBus Configuration Registers 465
7-2 Summary of SMBus I/O and Memory Mapped I/O Registers 475
7-3 Summary of SMBus PCR Registers 488
8-1 Summary of SPI Configuration Registers 490
8-2 Summary of SPI Memory Mapped Registers.....497
8-3 Summary of BIOS Flash Program Registers 528
9-1 Summary of GbE Configuration Registers 531
10-1 Summary of Intel Trace Huh Configuration Registers 550
11-1 Summary of UART PCI Configuration Registers 561
11-2 Summary of UART Memory Mapped Registers 574
11-3 Summary of UART Additional Registers 596
11-4 Summary of UART DMA Controller Registers 605
11-5 Summary of UART PCR Registers 635
12-1 Summary of Generic SPI PCI Configuration Registers.....638
12-2 Summary of Generic SPI (GSPI) Memory Mapped Registers 651
12-3 Summary of Generic SPI (GSPI) Additional Registers 657
12-4 Summary of Generic SPI (GSPI) DMA Controller Registers 669
12-5 Summary of GSPI PCR Registers 699
13-1 Summary of eMMC* PCI Configuration Registers 701
13-2 Summary of eMMC* Memory Mapped Registers 718
13-3 Summary of EMMC Additional Registers 758
14-1 Summary of SDXC PCI Configuration Registers 770
14-2 Summary of SDXC Memory Mapped Registers.....787
14-3 Summary of SDXC Additional Registers.....826
15-1 Summary of PCI Express* Port Configuration Registers 839
16-1 Summary of I^2C PCI Configuration Registers 901
16-2 Summary of I^2C Memory Mapped Registers 913
16-3 Summary of I^2C Additional Registers 940
16-4 Summary of I^2C DMA Controller Registers 951
16-5 Summary of I^2C PCR Registers 981
17-1 Summary of SATA Configuration Registers 983
17-2 Summary of SATA ABAR Registers 1012
17-3 Summary of SATA AIDP Registers 1045
17-4 Summary of SATA MXPBA Registers 1047
17-5 Summary of SATA MXTBA Registers 1048
17-6 Summary of SATA SIR Index Registers 1050
18-1 Summary of Intel(R) Management Engine Interface Configuration Registers 1052
18-2 Summary of Intel® MEI MMIO Registers 1069
19-1 Summary of IDE Redirect PCI Configuration (D22:F2) Registers 1071
20-1 Summary of Serial Port for Remote Keyboard and Text (KT) (D22:F3) Registers..... 1085
20-2 Summary of Keyboard and Text (KT) Additional Configuration Registers..... 1098
21-1 Summary of xHCI Configuration Registers..... 1099
21-2 Summary of xHCI Memory Mapped Registers..... 1131
22-1 Summary of USB Device Controller (xDCI) Configuration Registers..... 1224

22-2 Summary of xDCI MMIO Device Registers 1240
23-1 Summary of Thermal Reporting Configuration Registers 1273
23-2 Summary of Thermal Reporting Memory Mapped Registers 1289
24-1 Summary of CSI-2 Configuration Registers 1300
24-2 Summary of CSI2 Memory Mapped I/O Registers 1311
24-3 Summary of CSI2 Additional Configuration Registers 1389
25-1 Summary of ISH PCI Configuration Registers 1395
25-2 Summary of ISH MMIO Registers 1407
26-1 Summary of 8254 Timer Registers 1413
27-1 Summary of APIC Indirect Registers 1418
27-2 Summary of Advanced Programmable Interrupt Controller (APIC) Registers 1433
28-1 Summary of Processor Interface Memory Registers 1436
29-1 Summary of GPIO Community 0 Registers 1440
29-2 Summary of GPIO Community 1 Registers 1482
29-3 Summary of GPIO Community 2 Registers 1542
29-4 Summary of GPIO Community 3 Registers 1561
30-1 Summary of HPET Memory Mapped Registers 1595
31-1 Summary of Integrated Clock Controller FW Accessible Registers 1603
32-1 Summary of Interrupt Registers 1619
32-2 Summary of Interrupt PCR Registers 1630
33-1 Summary of Registers 1641
33-2 Summary of RTC PCR Registers 1646
34-1 Summary of SMBus TCO I/O Registers 1650
35-1 Summary of FIA Configuration PCR Registers 1659
35-2 Summary of OPI PCR Registers 1669
35-3 Summary of DCI PCR Registers 1698
35-4 Summary of PSF1 PCR Registers 1699
35-5 Summary of PSF2 PCR Registers 1716
35-6 Summary of PSF3 PCR Registers 1725
35-7 Summary of PSF4 PCR Registers 1756
35-8 Summary of IO Trap Registers 1758

Revision History

Revision Number	Description	Revision Date
001	• Initial release	August 2016
002	• Minor updates for clarity • Updated Chapter 14 registers	January 2017
003	• Updated registers	June 2017
004	• Added Chapter 1, “Introduction” • Updated Chapter 13, “eMMC Interface (D30:F4)” • Updated Chapter 29, “General Purpose I/O (GPIO)” • Updated Chapter 33, “Additional Configuration Registers” • Added support for 8th Generation Intel® Processor Family I/O for U Quad Core Platforms • Minor updates throughout for clarity.	August 2017
005	• Updated document title to include 10th Generation Intel® Processor Family I/O for Y Platforms	August 2019

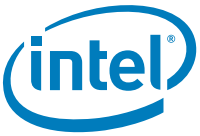
§ §

1 Introduction

This document (Volume 2) describes the PCH registers that are located in the PCI configuration space, memory space, or IO space. The following notations and definitions are used in the register description.

Attribute	Description
RO	Read Only. Writes to this register bit have no effect.
WO	Write Only. Reads to this register bit have no effect.
RW	Read/Write Once. A register bit with this attribute can be written only once after power up. After the first write, the bit becomes read only.
RW/O	Read/Write Once. A register bit with this attribute can be written only once after power up. After the first write, the bit becomes read only.
RW/1C	Read/Write Clear. The register bit is set to 1 by hardware and cleared by software writing a 1 to it.
RW/1S	Read/Write Set. The register bit is set to 1 by software and cleared by hardware.
RW/L	Read/Write Locked. A register bit with this attribute can be read and write, but cannot be written after the lock bit is set.
/V	Volatile or variable. This attribute indicates that the register bit can be updated by hardware (aside from resetting it). For example, RO/V means hardware controls the value; RW/V means that generally the bit is written by SW/FW but can be also updated by hardware.
/P	This attribute indicates that the register is reset only on loss of power.
/S	This attribute indicates that the initial value of the register bit is taken from software.

§ §



2 LPC Interface (D31:F0)

2.1 LPC Configuration Registers Summary

Table 2-1. Summary of LPC Configuration Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	Identifiers (ID)—Offset 0h	xxxx8086h
4h	5h	Device Command (CMD)—Offset 4h	7h
6h	7h	Status (STS)—Offset 6h	200h
8h	8h	Revision ID (RID)—Offset 8h	See Register
9h	Ch	Class Code (CC)—Offset 9h	60100h
Eh	Eh	Header Type (HTYPE)—Offset Eh	80h
2Ch	2Fh	Sub System Identifiers (SS)—Offset 2Ch	0h
34h	34h	Capability List Pointer (CAPP)—Offset 34h	0h
64h	64h	Serial IRQ Control (SCNT)—Offset 64h	10h
80h	81h	I/O Decode Ranges (IOD)—Offset 80h	0h
82h	83h	I/O Enables (IOE)—Offset 82h	0h
84h	87h	LPC Generic I/O Range #1 (LGIR1)—Offset 84h	0h
88h	8Bh	LPC Generic I/O Range #2 (LGIR2)—Offset 88h	0h
8Ch	8Fh	LPC Generic I/O Range #3 (LGIR3)—Offset 8Ch	0h
90h	93h	LPC Generic I/O Range #4 (LGIR4)—Offset 90h	0h
94h	97h	USB Legacy Keyboard/Mouse Control (ULKMC)—Offset 94h	0h
98h	9Bh	LPC Generic Memory Range (LGMR)—Offset 98h	0h
D0h	D3h	FWH ID Select #1 (FS1)—Offset D0h	112233h
D4h	D5h	FWH ID Select #2 (FS2)—Offset D4h	4567h
D8h	D9h	BIOS Decode Enable (BDE)—Offset D8h	FFCFh
DCh	DCh	BIOS Control (BC)—Offset DCh	20h
E0h	E3h	PCI Clock Control (PCCTL)—Offset E0h	0h

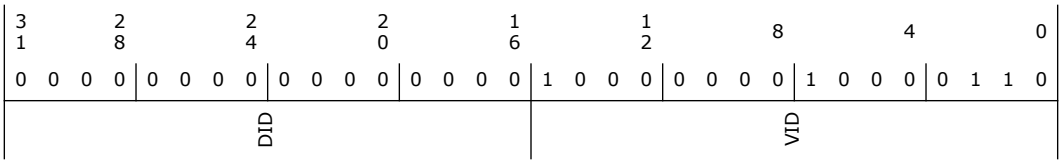
2.1.1 Identifiers (ID)—Offset 0h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 0

Default: xxxx8086h



Bit Range	Default & Access	Field Name (ID): Description
31:16	-- RO	**Device Identification (DID):** This is a 16-bit value assigned to the PCH LPC bridge. See the Device and Version ID Table in Volume 1 for the default value.
15:0	8086h RO	**Vendor Identification (VID):** Indicates Intel

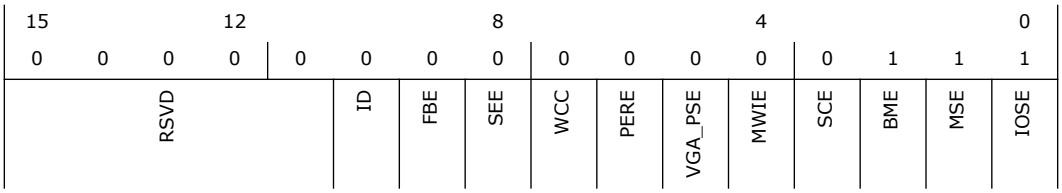
2.1.2 Device Command (CMD)—Offset 4h

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 0

Default: 7h



Bit Range	Default & Access	Field Name (ID): Description
15:11	0h RO	Reserved.
10	0h RO	**Interrupt Disable (ID):** The LPC bridge has no interrupts to disable
9	0h RO	**Fast Back to Back Enable (FBE):** Reserved as 0 per PCI-Express spec.
8	0h RW	**SERR# Enable (SEE):** The LPC bridge generates SERR# if this bit is set.
7	0h RO	**Wait Cycle Control (WCC):** Reserved as 0 per PCI-Express spec.
6	0h RW	**Parity Error Response Enable (PERE):** When this bit is set to 1, it enables the LPC bridge to response to parity errors detected on backbone interface.
5	0h RO	**VGA Palette Snoop (VGA_PSE):** Reserved as 0 per PCI-Express spec.
4	0h RO	**Memory Write and Invalidate Enable (MWIE):** Reserved as 0 per PCI-Express spec.
3	0h RO	**Special Cycle Enable (SCE):** Reserved as 0 per PCI-Express spec.

Bit Range	Default & Access	Field Name (ID): Description
2	1h RO	**Bus Master Enable (BME):** Bus Masters cannot be disabled.
1	1h RO	**Memory Space Enable (MSE):** Memory space cannot be disabled on LPC.
0	1h RO	**I/O Space Enable (IOSE):** I/O space cannot be disabled on LPC.

2.1.3 Status (STS)—Offset 6h

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 0

Default: 200h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
DPE	SSE	RMA	RTA	STA	DTS		DPD	FBC	RSVD	C66	CLIST	IS	RSVD		

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1C	**Detected Parity Error (DPE):** Set when the bridge detects a parity error on the internal backbone. This bit gets set even if CMD.PERE is not set.
14	0h RW/1C	**Signaled System Error (SSE):** Set when the LPC bridge signals a system error to the internal SERR# logic.
13	0h RO	**Received Master Abort (RMA):** Set when the bridge receives a completion with unsupported request status from the backbone. LPC is a target only controller.
12	0h RO	**Received Target Abort (RTA):** Set when the bridge receives a completion with completer abort status from the backbone. LPC is a target only controller.
11	0h RW/1C	**Signaled Target Abort (STA):** Set when the bridge generates a completion packet with target abort status on the backbone.
10:9	1h RO	**DEVSEL# Timing Status (DTS):** Indicates medium timing, although this has no meaning on the backbone.
8	0h RW/1C	**Data Parity Error Detected (DPD):** Set when the bridge receives a completion packet from the backbone from a previous request, and detects a parity error, and CMD.PERE is set.
7	0h RO	**Fast Back to Back Capable (FBC):** Reserved.
6	0h RO	Reserved.
5	0h RO	**66 MHz Capable (C66):** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RO	**Capabilities List (CLIST):** There is a capabilities list in the LPC bridge.
3	0h RO	**Interrupt Status (IS):** The LPC bridge does not generate interrupts.
2:0	0h RO	Reserved.

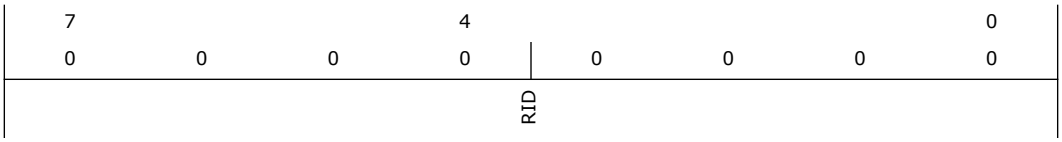
2.1.4 Revision ID (RID)—Offset 8h

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 31
Function: 0

Default: See Register



Bit Range	Default & Access	Field Name (ID): Description
7:0	-- RO	**Revision ID (RID):** Indicates the PCH revision. Refer to Device and Revision ID table in Volume 1 for specific value.

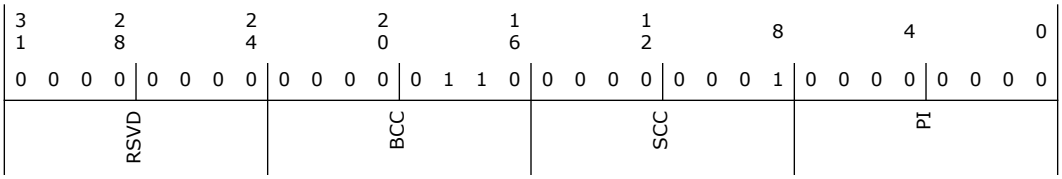
2.1.5 Class Code (CC)—Offset 9h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 0

Default: 60100h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:16	6h RO	**Base Class Code (BCC):** Indicates the device is a bridge device.
15:8	1h RO	**Sub-Class Code (SCC):** Indicates the device a PCI to ISA bridge.
7:0	0h RO	**Programming Interface (PI):** The LPC bridge has no programming interface.

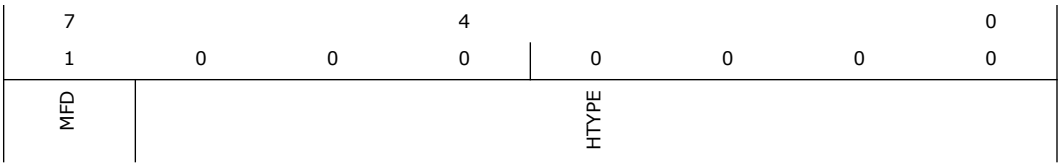
2.1.6 Header Type (HTYPE)—Offset Eh

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 31
Function: 0

Default: 80h



Bit Range	Default & Access	Field Name (ID): Description
7	1h RO	**Multi-function Device (MFD):** This bit is 1 to indicate a multifunction device.
6:0	0h RO	**Header Type (HTYPE):** Identifies the header layout of the configuration space, which is a generic device.

2.1.7 Sub System Identifiers (SS)—Offset 2Ch

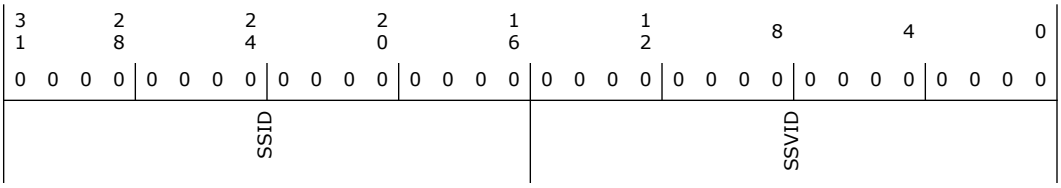
This register is initialized to logic 0 by the assertion of PLTRST#. This register can be written only once after PLTRST# de-assertion.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW/O	**Subsystem ID (SSID):** This is written by BIOS. No hardware action taken on this value.
15:0	0h RW/O	**Subsystem Vendor ID (SSVID):** This is written by BIOS. No hardware action taken on this value.

2.1.8 Capability List Pointer (CAPP)—Offset 34h

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 31
Function: 0

Default: 0h

7				4			0
0	0	0	0	0	0	0	0
CP							

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RO	**Capability Pointer (CP):** Indicates the offset of the first Capability Item.

2.1.9 Serial IRQ Control (SCNT)—Offset 64h

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 31
Function: 0

Default: 10h

7				4			0
0	0	0	1	0	0	0	0
EN	MD	FS				SFPW	

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Enable (EN):** When set, serial IRQs will be recognized.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**Mode (MD):** When set, the serial IRQ machine will be in continuous mode. When cleared, the serial IRQ machine will be in quiet mode. When setting the EN bit, this bit must also be written as a one to guarantee that the first action of the serial IRQ machine will be a start frame.
5:2	4h RO	**Frame Size (FS):** Fixed field that indicates the size of the SERIRQ frame as 21 frames.
1:0	0h RW	**Start Frame Pulse Width (SFPW):** This is the number of 33 MHz clocks that the SERIRQ pin will be driven low by the Serial IRQ controller to signal a start frame. In continuous mode, the controller will drive the start frame for the number of clocks specified. In quiet mode, the controller will drive the start frame for the number of clocks specified minus one, as the first clock was driven by the peripheral. Bits Clocks 00 4 01 6 10 8 11 Reserved

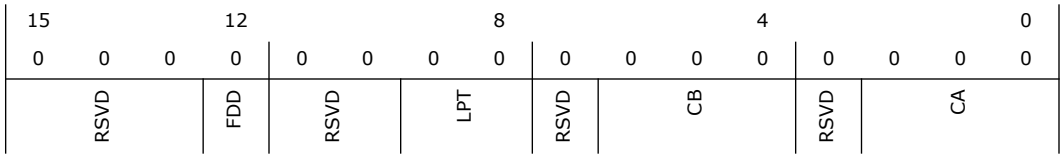
2.1.10 I/O Decode Ranges (IOD)—Offset 80h

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO	Reserved.
12	0h RW	**FDD Range (FDD):** The following table describes which range to decode for the FDD Port Bits Decode Range 0 3F0h - 3F5h, 3F7h (Primary) 1 370h - 375h, 377h (Secondary)
11:10	0h RO	Reserved.
9:8	0h RW	**LPT Range (LPT):** The following table describes which range to decode for the LPT Port: Bits Decode Range 00 378h - 37Fh and 778h - 77Fh 01 278h - 27Fh (port 279h is read only) and 678h - 67Fh 10 3BCh - 3BEh and 7BCh - 7BEh 11 Reserved
7	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
6:4	0h RW	**ComB Range (CB):** The following table describes which range to decode for the COMB Port Bits Decode Range 000 3F8h - 3FFh (COM 1) 001 2F8h - 2FFh (COM 2) 010 220h - 227h 011 228h - 22Fh 100 238h - 23Fh 101 2E8h - 2EFh (COM 4) 110 338h - 33Fh 111 3E8h - 3EFh (COM 3)
3	0h RO	Reserved.
2:0	0h RW	**ComA Range (CA):** The following table describes which range to decode for the COMA Port Bits Decode Range 000 3F8h - 3FFh (COM 1) 001 2F8h - 2FFh (COM 2) 010 220h - 227h 011 228h - 22Fh 100 238h - 23Fh 101 2E8h - 2EFh (COM 4) 110 338h - 33Fh 111 3E8h - 3EFh (COM 3)

2.1.11 I/O Enables (IOE)—Offset 82h

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 0

Default: 0h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD		ME2	SE	ME1	KE	HGE	LGE	RSVD				FDE	PPE	CBE	CAE

Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RO	Reserved.
13	0h RW	**Microcontroller Enable #2 (ME2):** Enables decoding of I/O locations 4Eh and 4Fh to LPC.
12	0h RW	**SuperI/O Enable (SE):** Enables decoding of I/O locations 2Eh and 2Fh to LPC.
11	0h RW	**Microcontroller Enable #1 (ME1):** Enables decoding of I/O locations 62h and 66h to LPC.
10	0h RW	**Keyboard Enable (KE):** Enables decoding of the keyboard I/O locations 60h and 64h to LPC.
9	0h RW	**High Gameport Enable (HGE):** Enables decoding of the I/O locations 208h to 20Fh to LPC.
8	0h RW	**Low Gameport Enable (LGE):** Enables decoding of the I/O locations 200h to 207h to LPC.

Bit Range	Default & Access	Field Name (ID): Description
7:4	0h RO	Reserved.
3	0h RW	**Floppy Drive Enable (FDE):** Enables decoding of the FDD range to LPC. Range is selected by LIOD.FDE
2	0h RW	**Parallel Port Enable (PPE):** Enables decoding of the LPT range to LPC. Range is selected by LIOD.LPT.
1	0h RW	**Com Port B Enable (CBE):** Enables decoding of the COMB range to LPC. Range is selected LIOD.CB.
0	0h RW	**Com Port A Enable (CAE):** Enables decoding of the COMA range to LPC. Range is selected LIOD.CA.

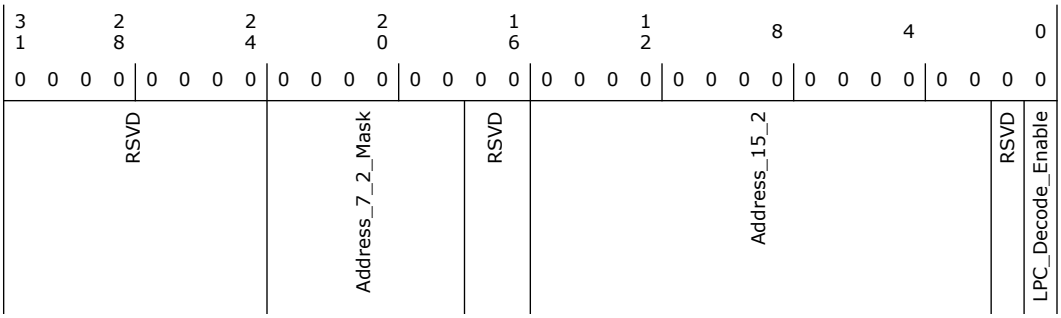
2.1.12 LPC Generic I/O Range #1 (LGIR1)—Offset 84h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:18	0h RW	**Address[7:2] Mask (Address_7_2_Mask):** A 1 in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for decoding blocks up to 256 bytes in size.
17:16	0h RO	Reserved.
15:2	0h RW	**Address[15:2] (Address_15_2):** DWord-aligned address. Note that PCH does not provide decode down to the word or byte level.
1	0h RO	Reserved.
0	0h RW	**LPC Decode Enable (LPC_Decode_Enable):** When this bit is set to 1, then the range specified in this register is enabled for decoding to LPC.

2.1.13 LPC Generic I/O Range #2 (LGIR2)—Offset 88h

Same bit definition as Generic I/O Range #1 (LGIR1).

2.1.14 LPC Generic I/O Range #3 (LGIR3)—Offset 8Ch

Same bit definition as Generic I/O Range #1 (LGIR1).

2.1.15 LPC Generic I/O Range #4 (LGIR4)—Offset 90h

Same bit definition as Generic I/O Range #1 (LGIR1).

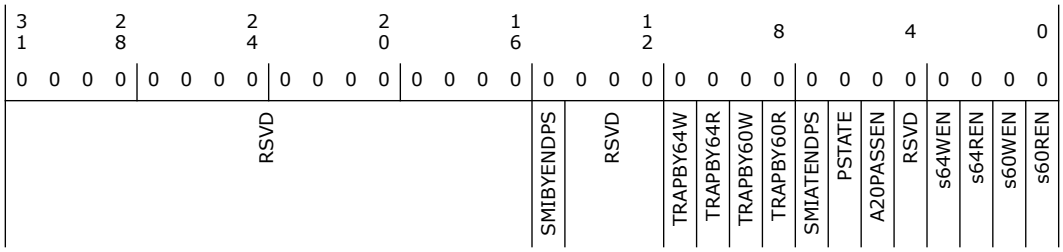
2.1.16 USB Legacy Keyboard/Mouse Control (ULKMC)—Offset 94h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	0h RW/1C	**SMI Caused by End of Pass-through (SMIBYENDPS):** Indicates if the event occurred. Note that even if the corresponding enable bit is not set in the Bit 7, then this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. Writing a 1 to this bit will clear the latch.
14:12	0h RO	Reserved.
11	0h RW/1C	**SMI Caused by Port 64 Write (TRAPBY64W):** Indicates if the event occurred. Note that even if the corresponding enable bit is not set in the Bit 3, then this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. Writing a 1 to this bit will clear the latch. Note that the A20Gate Pass-Through Logic allows specific port 64h Writes to complete without setting this bit.
10	0h RW/1C	**SMI Caused by Port 64 Read (TRAPBY64R):** Indicates if the event occurred. Note that even if the corresponding enable bit is not set in the Bit 2, then this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. Writing a 1 to this bit will clear the latch.
9	0h RW/1C	**SMI Caused by Port 60 Write (TRAPBY60W):** Indicates if the event occurred. Note that even if the corresponding enable bit is not set in the Bit 1, then this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. Writing a 1 to this bit will clear the latch. Note that the A20Gate Pass-Through Logic allows specific port 60h Writes to complete without setting this bit.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW/1C	**SMI Caused by Port 60 Read (TRAPBY60R):** Indicates if the event occurred. Note that even if the corresponding enable bit is not set in the Bit 0, then this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. Writing a 1 to this bit will clear the latch.
7	0h RW	**SMI at End of Pass-through Enable (SMIATENDPS):** May need to cause SMI at the end of a pass-through. Can occur if an SMI is generated in the middle of a pass through, and needs to be serviced later.
6	0h RO	**Pass Through State (PSTATE):** This read-only bit indicates that the state machine is in the middle of an A20GATE pass-through sequence. If software needs to reset this bit, it should set Bit 5 0.
5	0h RW	**A20Gate Pass-Through Enable (A20PASSEN):** When enabled, allows A20GATE sequence Pass-Through function (see details below in Section 20.14). When enabled, a specific cycle sequence involving writes to port 60h and port 64h does not result in the setting of the SMI status bits.SMI# will not be generated, even if the various enable bits are set.
4	0h RO	Reserved.
3	0h RW	**SMI on Port 64 Writes Enable (s64WEN):** When set, a 1 in bit 11 will cause an SMI event.
2	0h RW	**SMI on Port 64 Reads Enable (s64REN):** When set, a 1 in bit 10 will cause an SMI event.
1	0h RW	**SMI on Port 60 Writes Enable (s60WEN):** When set, a 1 in bit 9 will cause an SMI event.
0	0h RW	**SMI on Port 60 Reads Enable (s60REN):** When set, a 1 in bit 8 will cause an SMI event.

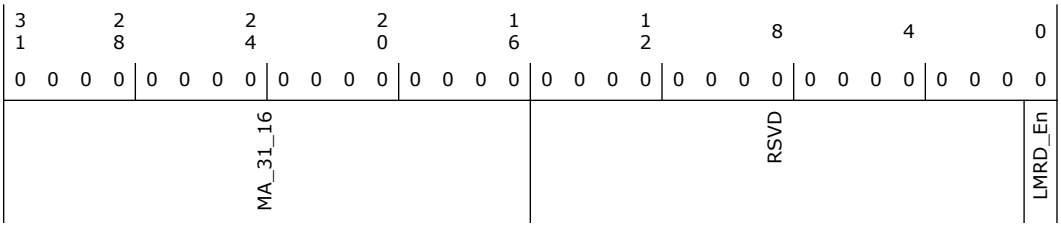
2.1.17 LPC Generic Memory Range (LGMR)—Offset 98h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Memory Address[31:16] (MA_31_16):** This field specifies a 64KB memory block anywhere in the 4GB memory space that will be decoded to LPC as standard LPC Memory Cycle if enabled.
15:1	0h RO	Reserved.
0	0h RW	**LPC Memory Range Decode Enable (LMRD_En):** When this bit is set to 1, then the range specified in this register is enabled for decoding to LPC.

2.1.18 FWH ID Select #1 (FS1)—Offset D0h

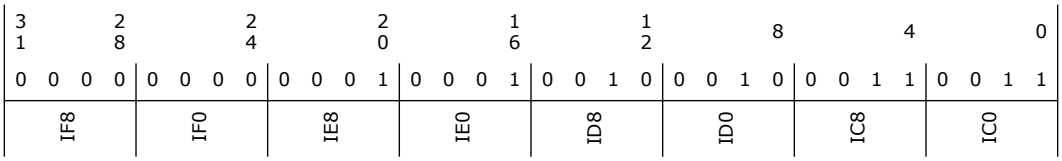
This register contains the IDSEL fields the LPC Bridge uses for memory cycles going to the FWH.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 0

Default: 112233h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**F8-FF IDSEL (IF8):** IDSEL to use in FWH cycle for range enabled by BDE.EF8.
27:24	0h RW	**F0-F7 IDSEL (IF0):** IDSEL to use in FWH cycle for range enabled by BDE.EF0.
23:20	1h RW	**E8-EF IDSEL (IE8):** IDSEL to use in FWH cycle for range enabled by BDE.EE8.
19:16	1h RW	**E0-E7 IDSEL (IE0):** IDSEL to use in FWH cycle for range enabled by BDE.EE0.
15:12	2h RW	**D8-DF IDSEL (ID8):** IDSEL to use in FWH cycle for range enabled by BDE.ED8.
11:8	2h RW	**D0-D7 IDSEL (ID0):** IDSEL to use in FWH cycle for range enabled by BDE.ED0.
7:4	3h RW	**C8-CF IDSEL (IC8):** IDSEL to use in FWH cycle for range enabled by BDE.EC8.
3:0	3h RW	**C0-C7 IDSEL (IC0):** IDSEL to use in FWH cycle for range enabled by BDE.EC0.

2.1.19 FWH ID Select #2 (FS2)—Offset D4h

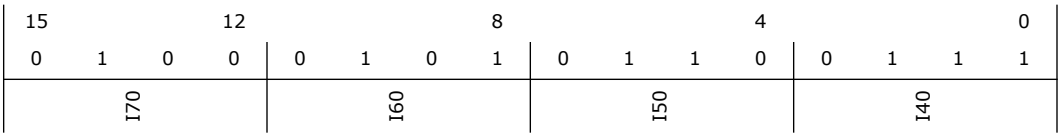
This register contains the additional IDSEL fields the LPC Bridge uses for memory cycles
going to the FWH.

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 0

Default: 4567h



Bit Range	Default & Access	Field Name (ID): Description
15:12	4h RW	**70-7F IDSEL (I70):** IDSEL to use in FWH cycle for range enabled by BDE.E70.
11:8	5h RW	**60-6F IDSEL (I60):** IDSEL to use in FWH cycle for range enabled by BDE.E60.
7:4	6h RW	**50-5F IDSEL (I50):** IDSEL to use in FWH cycle for range enabled by BDE.E50.
3:0	7h RW	**40-4F IDSEL (I40):** IDSEL to use in FWH cycle for range enabled by BDE.E40.

2.1.20 BIOS Decode Enable (BDE)—Offset D8h

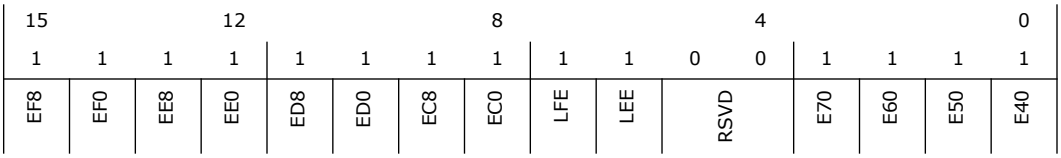
Note that this register effects the BIOS decode regardless of whether the BIOS is resident on LPC or SPI. The concept of Feature Space does not apply to SPI-based flash. PCH simply decodes these ranges as memory accesses when enabled for the SPI flash interface.

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 0

Default: FFCFh



Bit Range	Default & Access	Field Name (ID): Description
15	1h RO	**F8-FF Enable (EF8):** Enables decoding of 512K of the following BIOS range: Data space: FFF80000h - FFFFFFFFh Feature space: FFB80000h - FFBFFFFFh
14	1h RW	**F0-F8 Enable (EF0):** Enables decoding of 512K of the following BIOS range: Data space: FFF00000h - FFF7FFFFh Feature space: FFB00000h - FFB7FFFFh
13	1h RW	**E8-EF Enable (EE8):** Enables decoding of 512K of the following BIOS range: Data space: FFE80000h - FFEFFFFFh Feature space: FFA80000h - FFAFFFFFh
12	1h RW	**E0-E8 Enable (EE0):** Enables decoding of 512K of the following BIOS range: Data space: FFE00000h - FFE7FFFFh Feature Space: FFA00000h - FFA7FFFFh

Bit Range	Default & Access	Field Name (ID): Description
11	1h RW	**D8-DF Enable (ED8):** Enables decoding of 512K of the following BIOS range: Data space: FFD80000h - FFDFFFFFh Feature space: FF980000h - FF9FFFFFh
10	1h RW	**D0-D7 Enable (ED0):** Enables decoding of 512K of the following BIOS range: Data space: FFD00000h - FFD7FFFFh Feature space: FF900000h - FF97FFFFh
9	1h RW	**C8-CF Enable (EC8):** Enables decoding of 512K of the following BIOS range: Data space: FFC80000h - FFCFFFFFh Feature space: FF880000h - FF8FFFFFh
8	1h RW	**C0-C7 Enable (EC0):** Enables decoding of 512K of the following BIOS range: Data space: FFC00000h - FFC7FFFFh Feature space: FF800000h - FF87FFFFh
7	1h RW	**Legacy F Segment Enable (LFE):** This enables the decoding of the legacy 64KB range at F0000h - FFFFFh Note that decode for the BIOS legacy F segment is enabled by the LFE bit only, it is not affected by the GEN_PMCON_1.iA64_EN bit.
6	1h RW	**Legacy E Segment Enable (LEE):** This enables the decoding of the legacy 64KB range at E0000h - EFFFFh Note that decode for the BIOS legacy E segment is enabled by the LEE bit only, it is not affected by the GEN_PMCON_1.iA64_EN bit.
5:4	0h RO	Reserved.
3	1h RW	**70-7F Enable (E70):** Enables decoding of 1MB of the following BIOS range: Data space: FF700000h - FF7FFFFFh Feature space: FF300000h - FF3FFFFFh
2	1h RW	**60-6F Enable (E60):** Enables decoding of 1MB of the following BIOS range: Data space: FF600000h - FF6FFFFFh Feature Space: FF200000h - FF2FFFFFh
1	1h RW	**50-5F Enable (E50):** Enables decoding of 1MB of the following BIOS range: Data space: FF500000h - FF5FFFFFh Feature space: FF100000h - FF1FFFFFh
0	1h RW	**40-4F Enable (E40):** Enables decoding of 1MB of the following BIOS range: Data space: FF400000h - FF4FFFFFh Feature space: FF000000h - FF0FFFFFh

2.1.21 BIOS Control (BC)—Offset DCh

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 31
Function: 0

Default: 20h

7			4				0
0	0	1	0	0	0	0	0
BILD	BBS	EISS	TS	LPC_ESPI		LE	WPD

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW/1L	**BIOS Interface Lock-Down (BILD):** When set, prevents BC.TS and BC.BBS from being changed. This bit can only be written from 0 to 1 once. BIOS Note: This bit is not backed up in the RTC well. This bit should also be set in the BUC register in the RTC device to record the last state of this value following a cold reset.
6	0h RW/L	**Boot BIOS Strap (BBS):** This field determines the destination of accesses to the BIOS memory range. For the default, Functional Strap section of Signal Description chapter for details. Bits Description 0 SPI 1 LPC When SPI or LPC is selected, the range that is decoded is further qualified by other configuration bits described in the respective sections. The value in this field can be overwritten by software as long as the BIOS Interface Lock-Down is not set.
5	1h RW/L	**Enable InSMM.STS (EISS):** When this bit is set, the BIOS region is not writable until SMM sets the InSMM.STS bit. Today BIOS Flash is writable if WPD is a 1. If this bit [5] is set, then WPD must be a 1 and InSMM.STS (0xFED3_0880[0]) must be 1 also. If this bit [5] is clear, then BIOS is writable based only on WPD = 1 and the InSMM.STS is a dont care.
4	0h RO	**Top Swap (TS):** When set, PCH will invert either A16, A17, A18, A19 or A20 for cycles going to the BIOS space (but not the feature space). When cleared, PCH will not invert the lines. If booting from LPC (FWH), then the Boot Blook size is 64KB and A16 is inverted if Top Swap is enabled. If booting from SPI, then the BOOT_BLOCK_SIZE soft strap determines if A16, A17, A18, A19 or A20 should be inverted if Top Swap is enabled. *If PCH is strapped for Top-Swap is low at rising edge of PWROK, then this bit cannot be cleared by software. The strap jumper should be removed and the system rebooted. BIOS Note: 1) This bit provides a read-only path to view the state of the Top Swap strap. It is backed up and driven from the RTC well. Bios will need to program the corresponding register in the RTC Controller (in RTC well), which will be reflected in this register. 2) The Register portion of the Top Swap is lockable by the Bios Interface Lockdown Bit (BC.BILD)
3:2	0h RW	**LPC or eSPI Strap (LPC_ESPI):** Bit 3: Reserved Bit 2: This field determines the destination of accesses to the D31:F0 and related Fixed and Variable IO and Memory decode ranges, including BIOS memory range. 0 = LPC is the D31:F0 target. 1 = eSPI is the D31:F0 target. Note: This field cannot be overwritten by software.
1	0h RW/1L	**Lock Enable (LE):** When set, setting the WP bit will cause SMI. When cleared, setting the WP bit will not cause SMI. Once set, this bit can only be cleared by a PLTRST#. When this bit is set, EISS - bit [5] of this register is locked down.
0	0h RW	**Write Protect Disable (WPD):** When set, access to the BIOS space is enabled for both read and write cycles to BIOS. When cleared, only read cycles are permitted to the FWH or SPI flash. When this bit is written from a 0 to a 1 and the LE bit is also set, an SMI# is generated. This ensures that only SMM code can update BIOS.

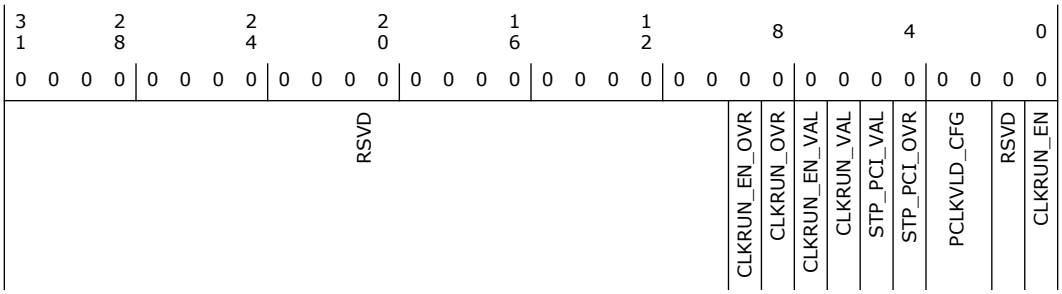
2.1.22 PCI Clock Control (PCCTL)—Offset E0h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9	0h RO	**CLKRUN# Buffer Enable Override (CLKRUN_EN_OVR):** When set to '1', SW is in control of the CLKRUN# buffer enable and the value in CLKRUN_EN_VAL will be propagated to the output buffer enable. When this bit is '0', HW will determine the value of the buffer enable.
8	0h RO	**CLKRUN# Override (CLKRUN_OVR):** When set to '1', SW is in control of the CLKRUN# pin and the value in CLKRUN_VAL will be propagated to the output pin. When this bit is '0', HW will determine the value of the pin.
7	0h RO	**CLKRUN# Buffer Enable Value (CLKRUN_EN_VAL):** Either HW or SW may own control of the CLKRUN# pin. This bit provides the value to drive on the active low CLKRUN# buffer enable if CLKRUN_EN_OVR is set to '1'.
6	0h RO	**CLKRUN# Pin Output Value (CLKRUN_VAL):** Either HW or SW may own control of the CLKRUN# pin. This bit provides the value to drive on the pin if CLKRUN_OVR is set to '1'.
5	0h RO	**Stop PCI# Value (STP_PCI_VAL):** Either Hardware or Software may own control of the internal STP_PCI#. This bit provides the value to drive on the STP_PCI# if STP_PCI_OVR is set to 1. Note: SW cannot control the STP_PCI# pin while PLTRST# is asserted (the pin will be at its reset default value).
4	0h RO	**Stop PCI# Override (STP_PCI_OVR):** This field determines the relationship between the internally broadcast indication of the external PCI clock being valid vs. the STP_PCI# pin. Encodings: 00: 1 flop stage of delay from STP_PCI# (default). Expected setting for Full Integration Mode 01: No delay (edges match STP_PCI#). For CK505 legacy mode 10: 2 flop stages of delay from STP_PCI# 11: Tie high (indicate that PCI clock is always valid)
3:2	0h RW	**LPC Clock Valid Configuration (PCLKVLD_CFG):** This field determines the relationship between the internally broadcast indication of the external LPC clock being valid vs. the STP_PCI# pin. Encodings: 00: 1 flop stage of delay from STP_PCI# (default) 01: No delay (edges match STP_PCI# 10: 2 flop stages of delay from STP_PCI# 11: Tie high (indicate that LPC clock is always valid)
1	0h RO	Reserved.
0	0h RW	**Clock Run Enable (CLKRUN_EN):** Enables the CLKRUN# logic to stop the LPC clocks. If the SLP_EN bit is set, then the Intel PCH will drive CLKRUN# low. This will keep the LPC and LPC clocks running on the way to the sleeping state. This is required to meet an LPC specification. This does not necessarily mean that the CLKRUN_EN bit is forced low when SLP_EN is set. Even though the CLKRUN# signal will be low when SLP_EN is set, the state of the CLKRUN_EN bit is ignored when SLP_EN bit is set. This gives flexibility in the implementation.

2.2 LPC PCR Registers Summary

These registers are within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID + Register Offset).

Table 2-2. Summary of LPC PCR Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
3418h	341Bh	General Control & Function Disable (GCFD)—Offset 3418h	0h

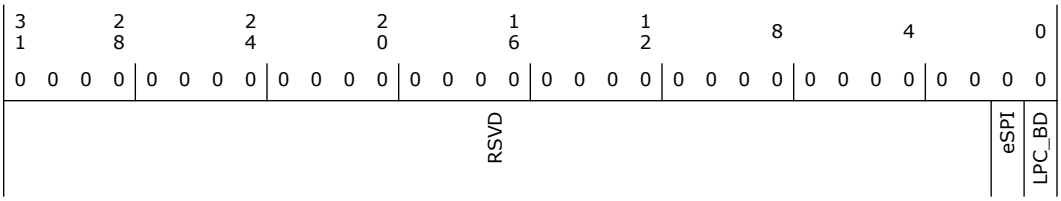
2.2.1 General Control & Function Disable (GCFD)—Offset 3418h

Access Method

Type: MSG Register
(Size: 32 bits)

Device: 31
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1	0h RO	**eSPI Enable Pin Strap (eSPI):** This field determines the destination of accesses to the D31:F0 and related Fixed and Variable IO and Memory decode ranges, including BIOS memory range. 0: LPC is the D31:F0 target. 1: eSPI is the D31:F0 target. Note: This field, along with BC.BBS strap setting determines the final Bios Boot Location.
0	0h RW	**LPC Bridge Disable (LPC_BD):** When set, the LPC bridge is disabled. When disabled the following spaces will no longer be decoded by the LPC bridge: 1) D31:F0 PCI Configuration space 2) Memory cycles below 16MB (1000000h) 3) I/O cycles below 64kB (10000h)

§ §

3 Enhanced SPI Interface (D31:F0)

3.1 Enhanced SPI (eSPI) Configuration Registers Summary

Table 3-1. Summary of Enhanced SPI (eSPI) Configuration Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	Identifiers (ESPI_DID_VID)—Offset 0h	XXXX8086h
4h	7h	Device Status and Command (ESPI_STS_CMD)—Offset 4h	403h
8h	Bh	Class Code and Revision ID (ESPI_CC_RID)—Offset 8h	60100XXh
Ch	Fh	BIST, Header Type, Primary Latency Timer, Cache Line Size (ESPI_BIST_HTYPE_PLT_CLS)—Offset Ch	800000h
2Ch	2Fh	Sub System Identifiers (ESPI_SS)—Offset 2Ch	0h
34h	37h	Capability List Pointer (ESPI_CAPP)—Offset 34h	E0h
80h	83h	I/O Decode Ranges and I/O Enables (ESPI_IOD_IOE)—Offset 80h	0h
84h	87h	eSPI Generic I/O Range #1 (ESPI_LGIR1)—Offset 84h	0h
88h	8Bh	eSPI Generic I/O Range #2 (ESPI_LGIR2)—Offset 88h	0h
8Ch	8Fh	eSPI Generic I/O Range #3 (ESPI_LGIR3)—Offset 8Ch	0h
90h	93h	eSPI Generic I/O Range #4 (ESPI_LGIR4)—Offset 90h	0h
94h	97h	USB Legacy Keyboard/Mouse Control (ESPI_ULKMC)—Offset 94h	0h
98h	9Bh	eSPI Generic Memory Range (ESPI_LGMR)—Offset 98h	0h
D0h	D3h	FWH ID Select #1 (ESPI_FS1)—Offset D0h	112233h
D4h	D7h	FWH ID Select #2 (ESPI_FS2)—Offset D4h	4567h
D8h	DBh	BIOS Decode Enable (ESPI_BDE)—Offset D8h	FFCFh
DCh	DFh	BIOS Control (ESPI_BC)—Offset DCh	20h

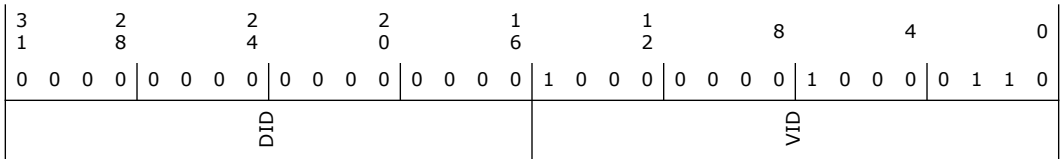
3.1.1 Identifiers (ESPI_DID_VID)—Offset 0h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 0

Default: XXXX8086h



Bit Range	Default & Access	Field Name (ID): Description
31:16	-- RO/V	**Device Identification (DID):** Indicates the Device ID of the controller. See the Device and Version ID Table in Volume 1 for the default value.
15:0	8086h RO	**Vendor Identification (VID):** Indicates Intel

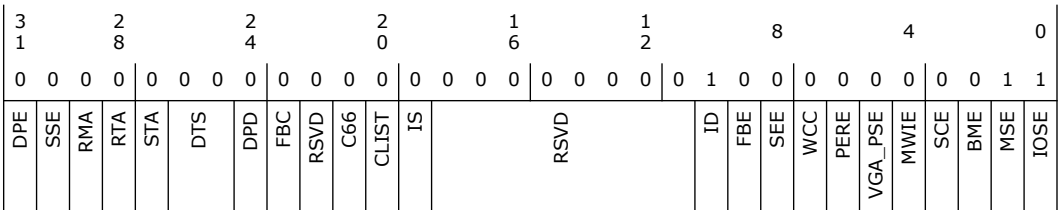
3.1.2 Device Status and Command (ESPI_STS_CMD)—Offset 4h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 0

Default: 403h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C/V	**Detected Parity Error (DPE):** Set when the bridge detects a parity error on the internal backbone. This bit gets set even if CMD.PERE is not set.
30	0h RW/1C/V	**Signaled System Error (SSE):** Set when the LPC bridge signals a system error to the internal SERR# logic.
29	0h RW/1C/V	**Received Master Abort (RMA):** Set when the bridge receives a completion with unsupported request status.
28	0h RW/1C/V	**Received Target Abort (RTA):** Set when the bridge receives a completion with completer abort status.
27	0h RW/1C/V	**Signaled Target Abort (STA):** Set when the bridge generates a completion packet with target abort status.
26:25	0h RO	**DEVSEL# Timing Status (DTS):** Indicates medium timing, although this has no meaning on the HW.
24	0h RW/1C/V	**Data Parity Error Detected (DPD):** Set when the bridge receives a completion packet from the backbone from a previous request, and detects a parity error, and CMD.PERE is set.
23	0h RO	**Fast Back to Back Capable (FBC):** Reserved - bit has no meaning on the HW.
22	0h RO	Reserved.
21	0h RO	**66 MHz Capable (C66):** Reserved - bit has no meaning on the HW.
20	0h RO	**Capabilities List (CLIST):** There is a capabilities list in the LPC bridge.

Bit Range	Default & Access	Field Name (ID): Description
19	0h RO	**Interrupt Status (IS):** The LPC bridge does not generate interrupts.
18:11	0h RO	Reserved.
10	1h RO	**Interrupt Disable (ID):** The LPC bridge has no interrupts to disable
9	0h RO	**Fast Back to Back Enable (FBE):** Reserved as 0 per PCI-Express spec.
8	0h RW	**SERR# Enable (SEE):** The LPC bridge generates SERR# if this bit is set.
7	0h RO	**Wait Cycle Control (WCC):** Reserved as 0 per PCI-Express spec.
6	0h RW	**Parity Error Response Enable (PERE):** When this bit is set to 1, it enables the LPC bridge to response to parity errors detected.
5	0h RO	**VGA Palette Snoop (VGA_PSE):** Reserved as 0 per PCI-Express spec.
4	0h RO	**Memory Write and Invalidate Enable (MWIE):** Reserved as 0 per PCI-Express spec.
3	0h RO	**Special Cycle Enable (SCE):** Reserved as 0 per PCI-Express spec.
2	0h RW	**Bus Master Enable (BME):** Bus Masters cannot be disabled.
1	1h RO	**Memory Space Enable (MSE):** Memory space cannot be disabled on LPC.
0	1h RO	**I/O Space Enable (IOSE):** I/O space cannot be disabled on LPC.

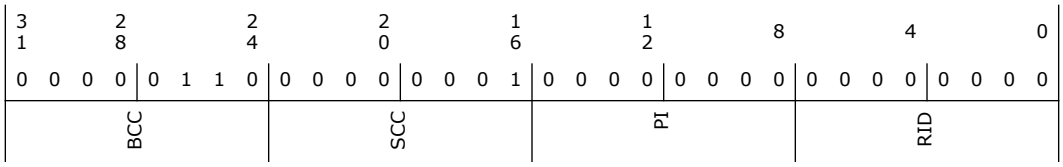
3.1.3 Class Code and Revision ID (ESPI_CC_RID)—Offset 8h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 0

Default: 60100XXh



Bit Range	Default & Access	Field Name (ID): Description
31:24	6h RO	**Base Class Code (BCC):** Indicates the device is a bridge device.
23:16	1h RO	**Sub-Class Code (SCC):** Indicates the device a PCI to ISA bridge.
15:8	0h RO	**Programming Interface (PI):** The LPC bridge has no programming interface.
7:0	-- RO/V	**Revision ID (RID):** Indicates stepping of the host controller. Refer to Device and Revision ID table in Volume 1 for specific value.

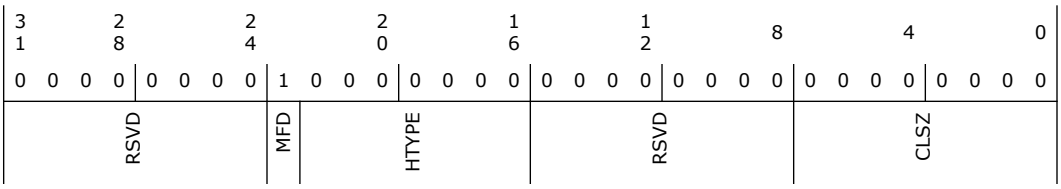
3.1.4 BIST, Header Type, Primary Latency Timer, Cache Line Size (ESPI_BIST_HTYPE_PLT_CLS)—Offset Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 0

Default: 800000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	1h RO	**Multi-function Device (MFD):** This bit is 1 to indicate a multifunction device.
22:16	0h RO	**Header Type (HTYPE):** Identifies the header layout of the configuration space, which is a generic device.
15:8	0h RO	Reserved.
7:0	0h RO	**Cacheline Size (CLSZ):** Cacheline Size

3.1.5 Sub System Identifiers (ESPI_SS)—Offset 2Ch

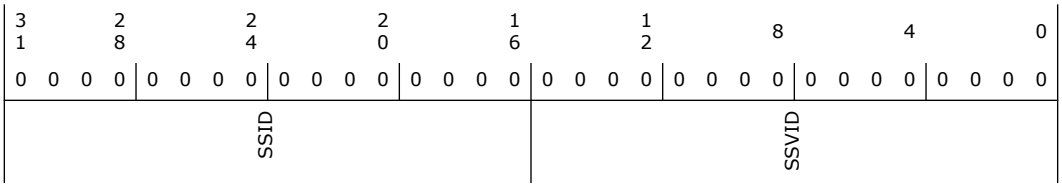
This register is initialized to logic 0 by the assertion of PLTRST#. This register can be written only once after PLTRST# de-assertion.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW/O	**Subsystem ID (SSID):** This is written by BIOS. No hardware action taken on this value.
15:0	0h RW/O	**Subsystem Vendor ID (SSVID):** This is written by BIOS. No hardware action taken on this value.

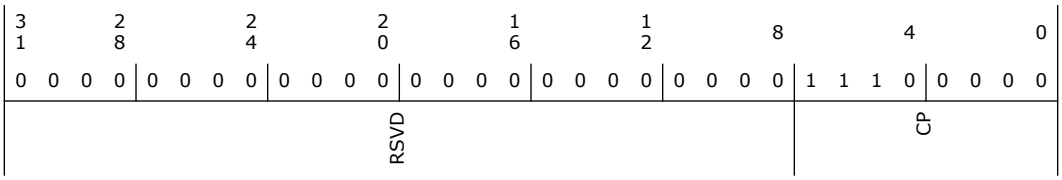
3.1.6 Capability List Pointer (ESPI_CAPP)—Offset 34h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 0

Default: E0h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	E0h RO	**Capability Pointer (CP):** Indicates the offset of the first Capability Item.

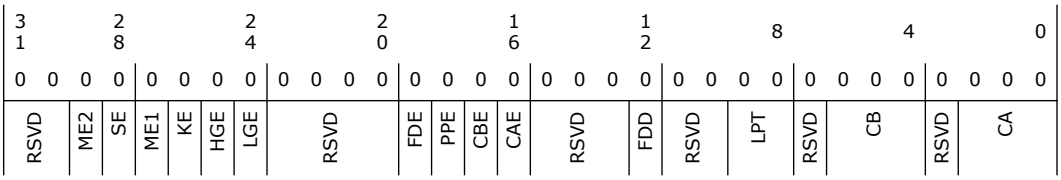
3.1.7 I/O Decode Ranges and I/O Enables (ESPI_IOD_IOE)—Offset 80h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29	0h RW	**Microcontroller Enable #2 (ME2):** Enables decoding of I/O locations 4Eh and 4Fh.
28	0h RW	**SuperI/O Enable (SE):** Enables decoding of I/O locations 2Eh and 2Fh.
27	0h RW	**Microcontroller Enable #1 (ME1):** Enables decoding of I/O locations 62h and 66h.
26	0h RW	**Keyboard Enable (KE):** Enables decoding of the keyboard I/O locations 60h and 64h.
25	0h RW	**High Gameport Enable (HGE):** Enables decoding of the I/O locations 208h to 20Fh.
24	0h RW	**Low Gameport Enable (LGE):** Enables decoding of the I/O locations 200h to 207h.
23:20	0h RO	Reserved.
19	0h RW	**Floppy Drive Enable (FDE):** Enables decoding of the FDD range. Range is selected by LIOD.FDE
18	0h RW	**Parallel Port Enable (PPE):** Enables decoding of the LPT range. Range is selected by LIOD.LPT.
17	0h RW	**Com Port B Enable (CBE):** Enables decoding of the COMB range. Range is selected by LIOD.CB.
16	0h RW	**Com Port A Enable (CAE):** Enables decoding of the COMA range. Range is selected by LIOD.CA.
15:13	0h RO	Reserved.
12	0h RW	**FDD Range (FDD):** The following table describes which range to decode for the FDD Port Bits Decode Range 0 3F0h - 3F5h, 3F7h (Primary) 1 370h - 375h, 377h (Secondary)
11:10	0h RO	Reserved.
9:8	0h RW	**LPT Range (LPT):** The following table describes which range to decode for the LPT Port: Bits Decode Range 00 378h - 37Fh and 778h - 77Fh 01 278h - 27Fh (port 279h is read only) and 678h - 67Fh 10 3BCh - 3BEh and 7BCh - 7BEh 11 Reserved
7	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
6:4	0h RW	**ComB Range (CB):** The following table describes which range to decode for the COMB Port Bits Decode Range 000 3F8h - 3FFh (COM 1)] 001 2F8h - 2FFh (COM 2) 010 220h - 227h 011 228h - 22Fh 100 238h - 23Fh 101 2E8h - 2EFh (COM 4) 110 338h - 33Fh 111 3E8h - 3EFh (COM 3)
3	0h RO	Reserved.
2:0	0h RW	**ComA Range (CA):** The following table describes which range to decode for the COMA Port Bits Decode Range 000 3F8h - 3FFh (COM 1) 001 2F8h - 2FFh (COM 2) 010 220h - 227h 011 228h - 22Fh 100 238h - 23Fh 101 2E8h - 2EFh (COM 4) 110 338h - 33Fh 111 3E8h - 3EFh (COM 3)

3.1.8 eSPI Generic I/O Range #1 (ESPI_LGIR1)—Offset 84h

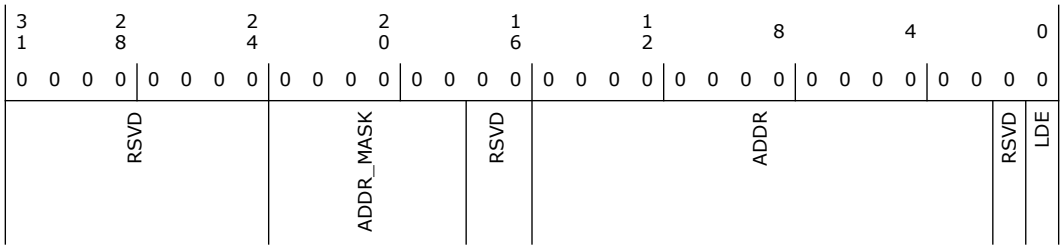
Access Method

Type: CFG Register (Size: 32 bits)

Device: 31

Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:18	0h RW	**Address[7:2] Mask (ADDR_MASK):** A 1 in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for decoding blocks up to 256 bytes in size.
17:16	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
15:2	0h RW	**Address[15:2] (ADDR):** DWord-aligned address. Note that PCH does not provide decode down to the word or byte level.
1	0h RO	Reserved.
0	0h RW	**eSPI Decode Enable (LDE):** When this bit is set to 1, then the range specified in this register is enabled for decoding to eSPI.

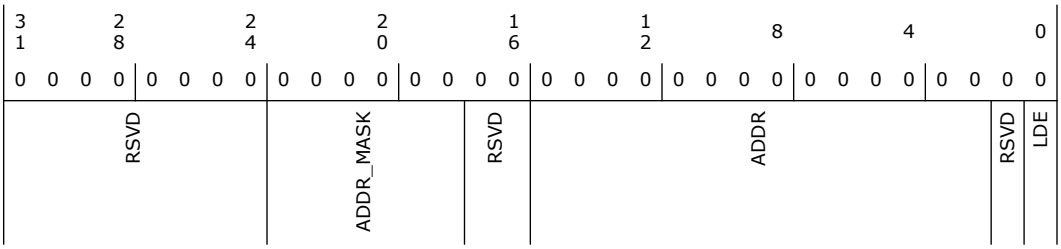
3.1.9 eSPI Generic I/O Range #2 (ESPI_LGIR2)—Offset 88h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:18	0h RW	**Address[7:2] Mask (ADDR_MASK):** A 1 in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for decoding blocks up to 256 bytes in size.
17:16	0h RO	Reserved.
15:2	0h RW	**Address[15:2] (ADDR):** DWord-aligned address. Note that PCH does not provide decode down to the word or byte level.
1	0h RO	Reserved.
0	0h RW	**LPC Decode Enable (LDE):** When this bit is set to 1, then the range specified in this register is enabled for decoding to eSPI.

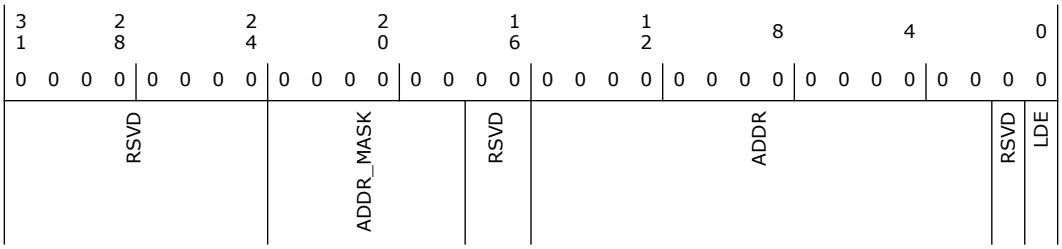
3.1.10 eSPI Generic I/O Range #3 (ESPI_LGIR3)—Offset 8Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:18	0h RW	**Address[7:2] Mask (ADDR_MASK):** A 1 in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for decoding blocks up to 256 bytes in size.
17:16	0h RO	Reserved.
15:2	0h RW	**Address[15:2] (ADDR):** DWord-aligned address. Note that PCH does not provide decode down to the word or byte level.
1	0h RO	Reserved.
0	0h RW	**LPC Decode Enable (LDE):** When this bit is set to 1, then the range specified in this register is enabled for decoding to eSPI.

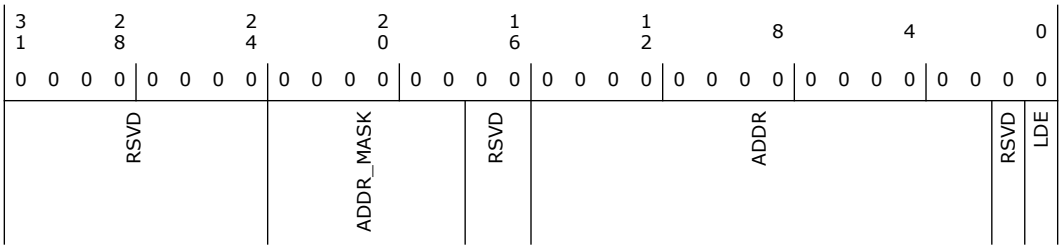
3.1.11 eSPI Generic I/O Range #4 (ESPI_LGIR4)—Offset 90h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:18	0h RW	**Address[7:2] Mask (ADDR_MASK):** A 1 in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for decoding blocks up to 256 bytes in size.
17:16	0h RO	Reserved.
15:2	0h RW	**Address[15:2] (ADDR):** DWord-aligned address. Note that PCH does not provide decode down to the word or byte level.
1	0h RO	Reserved.
0	0h RW	**LPC Decode Enable (LDE):** When this bit is set to 1, then the range specified in this register is enabled for decoding to eSPI.

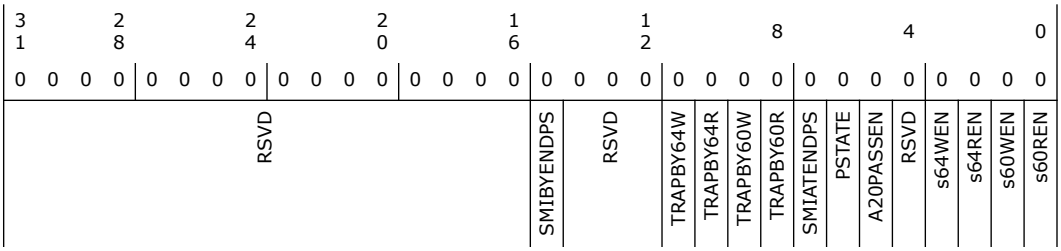
3.1.12 USB Legacy Keyboard/Mouse Control (ESPI_ULKMC)—Offset 94h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	0h RW/1C/V	**SMI Caused by End of Pass-through (SMIBYENDPS):** Indicates if the event occurred. Note that even if the corresponding enable bit is not set in the Bit 7, then this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. Writing a 1 to this bit will clear the latch.
14:12	0h RO	Reserved.
11	0h RW/1C/V	**SMI Caused by Port 64 Write (TRAPBY64W):** Indicates if the event occurred. Note that even if the corresponding enable bit is not set in the Bit 3, then this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. Writing a 1 to this bit will clear the latch. Note that the A20Gate Pass-Through Logic allows specific port 64h Writes to complete without setting this bit.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW/1C/V	**SMI Caused by Port 64 Read (TRAPBY64R):** Indicates if the event occurred. Note that even if the corresponding enable bit is not set in the Bit 2, then this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. Writing a 1 to this bit will clear the latch.
9	0h RW/1C/V	**SMI Caused by Port 60 Write (TRAPBY60W):** Indicates if the event occurred. Note that even if the corresponding enable bit is not set in the Bit 1, then this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. Writing a 1 to this bit will clear the latch. Note that the A20Gate Pass-Through Logic allows specific port 60h Writes to complete without setting this bit.
8	0h RW/1C/V	**SMI Caused by Port 60 Read (TRAPBY60R):** Indicates if the event occurred. Note that even if the corresponding enable bit is not set in the Bit 0, then this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. Writing a 1 to this bit will clear the latch.
7	0h RW	**SMI at End of Pass-through Enable (SMIATENDPS):** May need to cause SMI at the end of a pass-through. Can occur if an SMI is generated in the middle of a pass through, and needs to be serviced later.
6	0h RO/V	**Pass Through State (PSTATE):** This read-only bit indicates that the state machine is in the middle of an A20GATE pass-through sequence. If software needs to reset this bit, it should set Bit 5 0.
5	0h RW	**A20Gate Pass-Through Enable (A20PASSEN):** When enabled, allows A20GATE sequence Pass-Through function (see details below in Section 20.14). When enabled, a specific cycle sequence involving writes to port 60h and port 64h does not result in the setting of the SMI status bits.SMI# will not be generated, even if the various enable bits are set.
4	0h RO	Reserved.
3	0h RW	**SMI on Port 64 Writes Enable (s64WEN):** When set, a 1 in bit 11 will cause an SMI event.
2	0h RW	**SMI on Port 64 Reads Enable (s64REN):** When set, a 1 in bit 10 will cause an SMI event.
1	0h RW	**SMI on Port 60 Writes Enable (s60WEN):** When set, a 1 in bit 9 will cause an SMI event.
0	0h RW	**SMI on Port 60 Reads Enable (s60REN):** When set, a 1 in bit 8 will cause an SMI event.

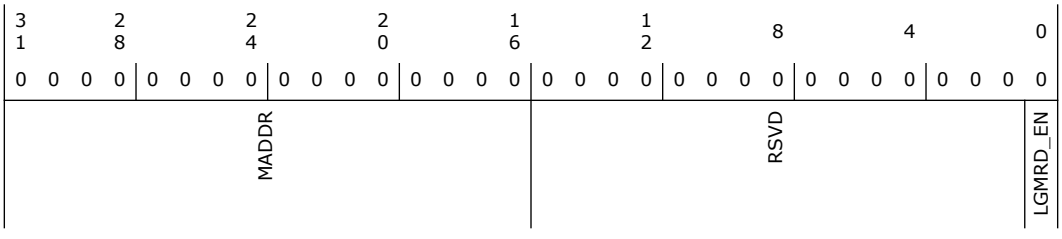
3.1.13 eSPI Generic Memory Range (ESPI_LGMR)—Offset 98h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Memory Address[31:16] (MADDR):** This field specifies a 64KB memory block anywhere in the 4GB memory space that will be decoded to eSPI as standard LPC Memory Cycle if enabled.
15:1	0h RO	Reserved.
0	0h RW	**LPC Memory Range Decode Enable (LGMRD_EN):** When this bit is set to 1, then the range specified in this register is enabled for decoding to eSPI.

3.1.14 FWH ID Select #1 (ESPI_FS1)—Offset D0h

This register contains the IDSEL fields the LPC Bridge uses for memory cycles going to the FWH.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 0

Default: 112233h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 1	0 0 0 1	0 0 1 0	0 0 1 0	0 0 1 1	0 0 1 1	
IF8	IF0	IE8	IE0	ID8	ID0	IC8	IC0	

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**F8-FF IDSEL (IF8):** IDSEL to use in FWH cycle for range enabled by BDE.EF8.
27:24	0h RW	**F0-F7 IDSEL (IF0):** IDSEL to use in FWH cycle for range enabled by BDE.EF0.
23:20	1h RW	**E8-EF IDSEL (IE8):** IDSEL to use in FWH cycle for range enabled by BDE.EE8.
19:16	1h RW	**E0-E7 IDSEL (IE0):** IDSEL to use in FWH cycle for range enabled by BDE.EE0.
15:12	2h RW	**D8-DF IDSEL (ID8):** IDSEL to use in FWH cycle for range enabled by BDE.ED8.
11:8	2h RW	**D0-D7 IDSEL (ID0):** IDSEL to use in FWH cycle for range enabled by BDE.ED0.
7:4	3h RW	**C8-CF IDSEL (IC8):** IDSEL to use in FWH cycle for range enabled by BDE.EC8.
3:0	3h RW	**C0-C7 IDSEL (IC0):** IDSEL to use in FWH cycle for range enabled by BDE.EC0.

3.1.15 FWH ID Select #2 (ESPI_FS2)—Offset D4h

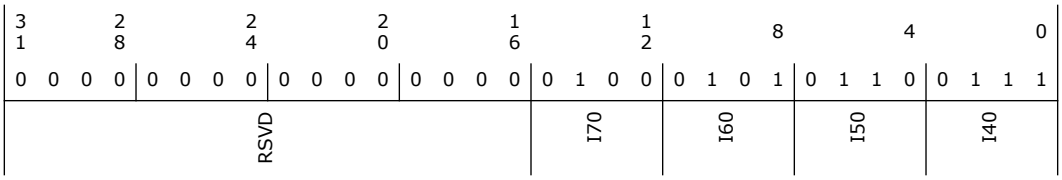
This register contains the additional IDSEL fields the LPC Bridge uses for memory cycles going to the FWH.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 0

Default: 4567h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:12	4h RW	**70-7F IDSEL (I70):** IDSEL to use in FWH cycle for range enabled by BDE.E70.
11:8	5h RW	**60-6F IDSEL (I60):** IDSEL to use in FWH cycle for range enabled by BDE.E60.
7:4	6h RW	**50-5F IDSEL (I50):** IDSEL to use in FWH cycle for range enabled by BDE.E50.
3:0	7h RW	**40-4F IDSEL (I40):** IDSEL to use in FWH cycle for range enabled by BDE.E40.

3.1.16 BIOS Decode Enable (ESPI_BDE)—Offset D8h

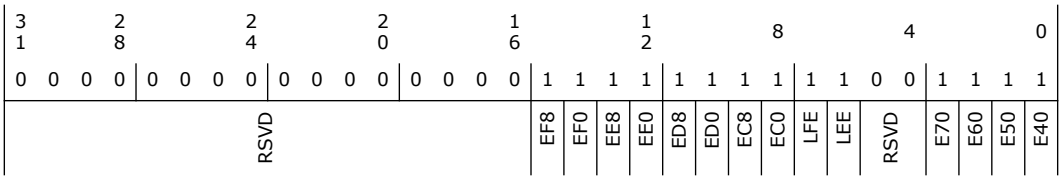
Note that this register effects the BIOS decode regardless of whether the BIOS is resident on LPC or SPI. The concept of Feature Space does not apply to SPI-based flash. PCH simply decodes these ranges as memory accesses when enabled for the SPI flash interface.

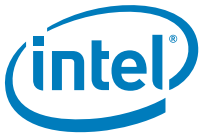
Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 0

Default: FFCFh





Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	1h RO	**F8-FF Enable (EF8):** Enables decoding of 512K of the following BIOS range: Data space: FFF80000h - FFFFFFFFh Feature space: FFB80000h - FFBFFFFFh
14	1h RW	**F0-F8 Enable (EF0):** Enables decoding of 512K of the following BIOS range: Data space: FFF00000h - FFF7FFFFh Feature space: FFB00000h - FFB7FFFFh
13	1h RW	**E8-EF Enable (EE8):** Enables decoding of 512K of the following BIOS range: Data space: FFE80000h - FFEFFFFFh Feature space: FFA80000h - FFAFFFFFh
12	1h RW	**E0-E8 Enable (EE0):** Enables decoding of 512K of the following BIOS range: Data space: FFE00000h - FFE7FFFFh Feature Space: FFA00000h - FFA7FFFFh
11	1h RW	**D8-DF Enable (ED8):** Enables decoding of 512K of the following BIOS range: Data space: FFD80000h - FFDFFFFFh Feature space: FF980000h - FF9FFFFFh
10	1h RW	**D0-D7 Enable (ED0):** Enables decoding of 512K of the following BIOS range: Data space: FFD00000h - FFD7FFFFh Feature space: FF900000h - FF97FFFFh
9	1h RW	**C8-CF Enable (EC8):** Enables decoding of 512K of the following BIOS range: Data space: FFC80000h - FFCFFFFFh Feature space: FF880000h - FF8FFFFFh
8	1h RW	**C0-C7 Enable (EC0):** Enables decoding of 512K of the following BIOS range: Data space: FFC00000h - FFC7FFFFh Feature space: FF800000h - FF87FFFFh
7	1h RW	**Legacy F Segment Enable (LFE):** This enables the decoding of the legacy 64KB range at F0000h - FFFFFh Note that decode for the BIOS legacy F segment is enabled by the LFE bit only, it is not affected by the GEN_PMCON_1.iA64_EN bit.
6	1h RW	**Legacy E Segment Enable (LEE):** This enables the decoding of the legacy 64KB range at E0000h - EFFFFh Note that decode for the BIOS legacy E segment is enabled by the LEE bit only, it is not affected by the GEN_PMCON_1.iA64_EN bit.
5:4	0h RO	Reserved.
3	1h RW	**70-7F Enable (E70):** Enables decoding of 1MB of the following BIOS range: Data space: FF700000h - FF7FFFFFh Feature space: FF300000h - FF3FFFFFh
2	1h RW	**60-6F Enable (E60):** Enables decoding of 1MB of the following BIOS range: Data space: FF600000h - FF6FFFFFh Feature Space: FF200000h - FF2FFFFFh
1	1h RW	**50-5F Enable (E50):** Enables decoding of 1MB of the following BIOS range: Data space: FF500000h - FF5FFFFFh Feature space: FF100000h - FF1FFFFFh
0	1h RW	**40-4F Enable (E40):** Enables decoding of 1MB of the following BIOS range: Data space: FF400000h - FF4FFFFFh Feature space: FF000000h - FF0FFFFFh

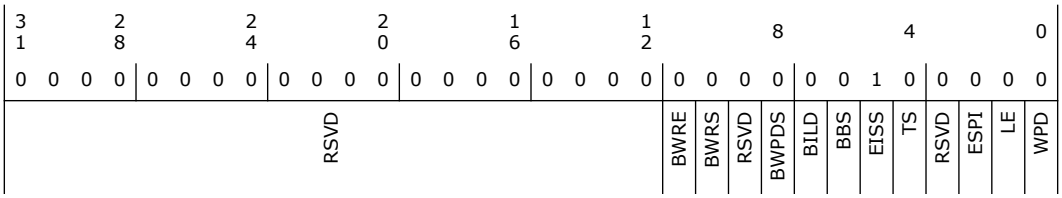
3.1.17 BIOS Control (ESPI_BC)—Offset DCh

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 0

Default: 20h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	Reserved.
11	0h RW/L	**BIOS Write Reporting (Async-SMI) Enable (BWRE):** 0: Disable reporting of BIOS Write event. 1: Enable reporting of BIOS Write event (PCBC.BWRS = 1) using Async-SMI.
10	0h RW/1C/V	**BIOS Write Status (BWRS):** HW sets this bit if a memory write access is detected to a protected BIOS range. 0: Memory write to BIOS region not attempted or attempted with PCBC.WPD = 1. 1: A memory write transaction to BIOS region has been received with PCBC.WPD = 0. Note: SW must write a 1 to this bit to clear.
9	0h RO	Reserved.
8	0h RW/1C/V	**BIOS Write Protect Disable Status (BWPDS):** HW sets this bit if configuration write access is detected to protected PCBC.WPD bit. 0: No attempt has been made to set PCBC.WPD with PCBC.LE = 1. 1: A configuration write request has been received to set PCBC.WPD (from 0 to 1) with PCBC.LE = 1. Note: SW must write a 1 to this bit to clear it.
7	0h RW/L	**BIOS Interface Lock-Down (BILD):** When set, prevents BC.TS and BC.BBS from being changed. This bit can only be written from 0 to 1 once. BIOS Note: This bit is not backed up in the RTC well. This bit should also be set in the BUC register in the RTC device to record the last state of this value following a cold reset.
6	0h RW/V/L	**Boot BIOS Strap (BBS):** This field determines the destination of accesses to the BIOS memory range. For the default, see the Strap section for details. 0: SPI 1: LPC/eSPI When SPI or LPC/eSPI is selected, the range that is decoded is further qualified by other configuration bits described in the respective sections. The value in this field can be overwritten by software as long as the BIOS Interface Lock-Down is not set.
5	1h RW/L	**Enable InSMM.STS (EISS):** When this bit is set, the BIOS region is not writable until SMM sets the InSMM.STS bit.br] If this bit (5) is set, then WPD must be a 1 and InSMM.STS (0xFED3_0880(0)) must be 1 also. If this bit (5) is clear, then BIOS is writable based only on WPD = 1 and the InSMM.STS is a dont care.
4	0h RO/V	**Top Swap (TS):** When set, PCH will invert either A16, A17, A18, A19, or A20 for cycles going to the BIOS space (but not the Feature space). When cleared, PCH will not invert the lines. If booting from LPC (FWH) or eSPI, then the Boot Block Size is fixed at 64KB and A16 is inverted if Top Swap is enabled. If booting from SPI, then the BOOT_BLOCK_SIZE soft strap determines if A16, A17, A18, A19, or A20 should be inverted if Top Swap is enabled. Note: If the Top-Swap strap is asserted, then this bit cannot be cleared by software. The strap jumper should be removed and the system rebooted. BIOS Note: This bit provides a read-only path to view the state of the Top Swap strap. It is backed up and driven from the RTC well. BIOS will need to program the corresponding register in the RTC well, which will be reflected in this register.
3	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO/V	**eSPI Enable Pin Strap (ESPI):** This field determines the destination of accesses to the D31:F0 and related Fixed and Variable IO and Memory decode ranges, including BIOS memory range. 0 = LPC is the D31:F0 target. 1 = eSPI is the D31:F0 target. Note: This field cannot be overwritten by software (unlike the PCBC.BBS field).
1	0h RW/L	**Lock Enable (LE):** When set, setting the WP bit will cause SMI. When cleared, setting the WP bit will not cause SMI. Once set, this bit can only be cleared by a PLTRST#. When this bit is set, EISS - bit (5) of this register is locked down.
0	0h RW	**Write Protect Disable (WPD):** When set, access to the BIOS space is enabled for both read and write cycles to BIOS. When cleared, only read cycles are permitted to the FWH or SPI flash. When this bit is written from a 0 to a 1 and the LE bit is also set, an SMI# is generated. This ensures that only SMM code can update BIOS.

3.2 eSPI PCR Registers Summary

These registers are within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID + Register Offset).

Table 3-2. Summary of eSPI PCR Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
4000h	4003h	eSPI Slave Configuration and Link Control (SLV_CFG_REG_CTL)—Offset 4000h	0h
4004h	4007h	eSPI Slave Configuration Register Data (SLV_CFG_REG_DATA)—Offset 4004h	0h
4020h	4023h	Peripheral Channel Error for Slave 0 (PCERR_SLV0)—Offset 4020h	0h
4030h	4033h	Virtual Wire Channel Error for Channel 0 (VWERR_SLV0)—Offset 4030h	0h
4040h	4043h	Flash Access Channel Error for Slave 0 (FCERR_SLV0)—Offset 4040h	0h
4050h	4053h	Link Error for Slave 0 (LNKERR_SL0)—Offset 4050h	FF00h

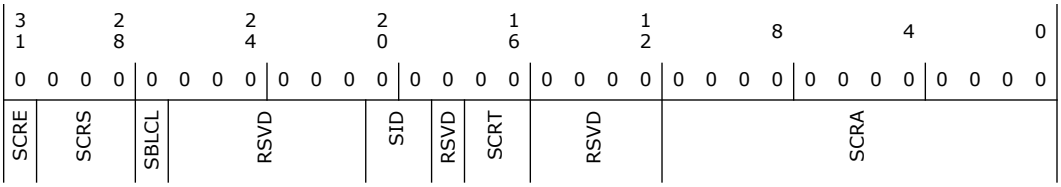
3.2.1 eSPI Slave Configuration and Link Control (SLV_CFG_REG_CTL)—Offset 4000h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S/V	**Slave Configuration Register Access Enable (SCRE):** Writing a 1 to this field triggers an access (SCRT) to a Slave Config Register ('Go'). Note: Hardware clears this bit to 0 (& sets the SCRS field) when the transaction has completed on the eSPI bus. In the case of a configuration/status register read, the data is valid only after this bit has been cleared by HW. Note: The SCRE is effective only if SCRS is clear.
30:28	0h RW/1C/V	**Slave Configuration Register Access Status (SCRS):** This field is set by upon the completion of a configuration register access (SCRE). Software must clear this field by writing all 1s before initiating another Slave configuration register access (SCRE). 0h: Status not valid 1h: Slave No_Response 2h: Slave Response CRC Error 3h: Slave Response Fatal Error 4h: Slave Response Non-Fatal Error 5h – 6h: Reserved 7h: No errors (transaction completed successfully)
27	0h RW/1S	**SB eSPI Link Configuration Lock (SBLCL):** When set, eSPI controller prevents writes (i.e., SET_CONFIGURATION)to any eSPI Specification defined Slave Capabilities and Configuration registers in the reserved register address range (0h – 7FFh). Access to Slave implementation specific configuration registers outside this range are not impacted by this lock bit and are always available – access protections to such registers are Slave implementation dependent. Note: This bit cannot be written to 0 once it has been set to 1. It can only be cleared by PLTRST# assertion. The lock is automatically disabled if and while the LNKERR_SLV0.SLCRR register bit is asserted (upon an eSPI link Fatal Error condition) to allow BIOS (or another SW agent) to attempt to recover the link. Note: This bit has no effect when PLTRST# is asserted. BIOS Note: BIOS must ensure that this bit is set to 1 after initial eSPI link configuration is over to prevent any further (unintentional or malicious) changes to the eSPI link configuration
26:21	0h RO	Reserved.
20:19	0h RW	**Slave ID (SID):** eSPI Slave ID (CS#) to which the Slave Configuration Register Access (SCRT) is directed. 00: eSPI Slave 0 (EC/BMC) 01: eSPI Slave 1 (for Server SKU only and when a when a second eSPI Slave device is present) 10 – 2'b11: Reserved
18	0h RO	Reserved.
17:16	0h RW	**Slave Configuration Register Access Type (SCRT):** 00: Slave Configuration register read from address SCRA[11:0] (GET_CONFIG)(br) 01: Slave Configuration register write to address SCRA[11:0] (SET_CONFIG)(br) 10: Slave Status register read (GET_STATUS)(br) 11: In-Band Reset Note: Writes to Slave Configuration registers in the reserved address range (0h – 7FFh) are gated by the SBLCL bit. Note: Setting this field to 10 triggers a Get_Status command to the Slave. In this case, the SCRA field is ignored and only the lower 16-bits of the returned data (SLV_CFG_REG_DATA[15:0]) are valid. Note: Setting this field to 11 triggers an In-Band Reset command to the Slave. In this case, the SCRA field is ignored and no data is returned. This command resets the link for the targeted Slave to a default configuration. Software is responsible for reinitializing the link to optimized (higher performance) settings using these registers.
15:12	0h RO	Reserved.
11:0	0h RW	**Slave Configuration Register Address (SCRA)**

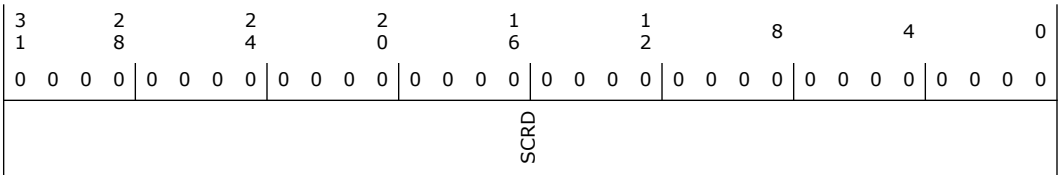
3.2.2 eSPI Slave Configuration Register Data (SLV_CFG_REG_DATA)—Offset 4004h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Slave Configuration Register for Read and Write data (SCRD):** Configuration register Write data from software or read data from the Slave. For writes, this register must be programmed before the CTL register. For reads, data in this register is valid after the CTL.SCRE bit has been cleared by HW and the CTL.SCRS field indicates a successful transaction.

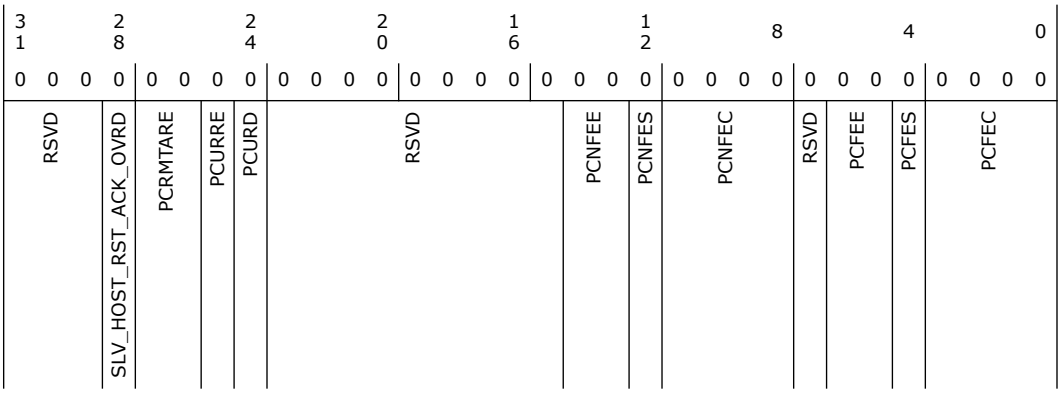
3.2.3 Peripheral Channel Error for Slave 0 (PCERR_SLV0)—Offset 4020h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	Reserved.
28	0h RW	**SLV_HOST_RST_ACK_OVRD:** A 1 in this bit will cause the eSPI-MC to not wait for the Slave HOST_RESET_ACK Virtual Wire before (immediately) asserting the ResetPrepAck (Host space, GenPrep). The Host_Reset_Warn VW will be transmitted to the Slave independent of the setting for this bit.
27:26	0h RW	**Peripheral Channel Received Master or Target Abort Reporting Enable (PCRMTARE):** 00: Disable RMA or RTA Reporting 01: Reserved 10: Enable RMA or RTA Reporting as SERR 11: Enable RMA or RTA Reporting as SMI Note: SERR enable is also qualified by PCCMD.SEE (Offset 04h) when PLTRST# is deasserted. Note: SERR also sets PCSTS.SSE (Offset 06h) when PLTRST# is deasserted.
25	0h RW	**Peripheral Channel Unsupported Request Reporting Enable (PCURRE):** If set to 1 by software, it allows reporting of an Unsupported Request (UR) as a System Error (SERR). If eSPI controller decodes a Posted transaction that is not supported, it sets the PCURD bit. If PCCMD.SEE (SERR enable) is also set to 1, then eSPIMC sets the PCSTS.SSE (Signaled System Error) bit and sends a Do_SErr message. Note: If the transaction was a Non-Posted request, then the agent handles the transaction as an Advisory Non-Fatal error, and no error logging or signaling is done. The Completion with UR Completion Status serves the purpose of error reporting.
24	0h RW/1C/V	**Peripheral Channel Unsupported Request Detected (PCURD):** Set to 1 by hardware upon detecting an Unspported Request (UR) that is not considered an Advisory Non- Fatal error and PCERR.PCURRE is set. Cleared to 0 when software writes a 1 to this register.
23:15	0h RO	Reserved.
14:13	0h RW	**Peripheral Channel Non-Fatal Error Reporting Enable (PCNFEE):** 00: Disable Non-Fatal Error Reporting 01: Reserved 10: Enable Non-Fatal Error Reporting as SERR 11: Enable Non-Fatal Error Reporting as SMI Note: SERR enable is also qualified by PCCMD.SEE (Offset 04h) when PLTRST# is deasserted. Note: SERR also sets PCSTS.SSE (Offset 06h) when PLTRST# is deasserted. Note: SMI/SERR messages are not generated if the Host is in reset (PLTRST# asserted).
12	0h RW/1C/V	**Peripheral Channel Non-Fatal Status (PCNFES):** This field is set by hardware if a Non-Fatal Error condition is detected on the Peripheral Channel. Software must clear this bit. 0: No Non-Fatal Error detected 1: Non-Fatal Error detected (PCNFEC has a non-zero value) Note: Clearing this unlocks the PCNFEC field and triggers a SB Deassert_SMI message if PCNFEE is set to SMI. Note: Setting of this bit is independent of the enable to generate a SMI/SERR (PCNFEE)
11:8	0h RO/V	**Peripheral Channel Non-Fatal Status (PCNFEC):** 0h: No error 1h: Slave Response Code: NONFATAL_ERROR 2h: Slave Response Code: Unsuccessful Completion 3h: Unexpected completion received from Slave (i.e. completion without non-posted request or completion with invalid tag or completion with invalid length) 4h: Unsupported Cycle Type (w.r.t. Command) 5h: Unsupported Message Code 6h: Unsupported Address/Length alignment (upstream only): Memory: Address + Length > 64 B (aligned) [for both Posted and Non-Posted transactions] 7h: Unsupported Address/Length alignment (upstream only): Memory: 64-bit Address with Addr[63:32] = 0h [for both Posted and Non-Posted transactions] 8h – Fh: Reserved Note: This field is updated after a Peripheral channel transaction is completed if the PCNFES bit is not set.
7	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
6:5	0h RW	**Peripheral Channel Fatal Error Reporting (PCFEE):** 00: Disable Fatal Error Reporting 01: Reserved 10: Enable Fatal Error Reporting as SERR (IOSF-SB Do_SErr message) 11: Enable Fatal Error Reporting as SMI (IOSF-SB Assert_SMI message) Note: SERR enable is also qualified by PCCMD.SEE (Offset 04h) when PLTRST# is deasserted. Note: SERR also sets PCSTS.SSE (Offset 06h) when PLTRST# is deasserted. Note: SMI/SERR messages are not generated if the Host is in reset (PLTRST# asserted).
4	0h RW/1C/V	**Peripheral Channel Fatal Error Reporting (PCFES):** This field is set by hardware if a Fatal Error condition is detected on the Peripheral Channel. Software must clear this bit by writing a 1 to it. 0: No Fatal Error detected 1: Fatal Error Type 2 detected (PCFEC has a non-zero value) Note: Clearing this unlocks the PCFEC field and triggers an SB Deassert_SMI message if PCFEE is set to SMI. Note: Setting of this bit is independent of the enable to generate a SMI/SERR (PCFEE).
3:0	0h RO/V	**Peripheral Channel Fatal Error Cause (PCFEC):** 0h: No error 1h – 7h: Reserved 8h: Malformed Slave Response Payload: Payload length > Max Payload Size (aligned) [Type 2] 9h: Malformed Slave Response Payload: Read request size > Max Read Request Size (aligned) [Type 2] Ah: Malformed Slave Response Payload: Address + Length > 4KB (aligned) [Type 2] Bh – Fh: Reserved Note: This field is updated after a Peripheral channel transaction is completed if the PCFES bit is not set.

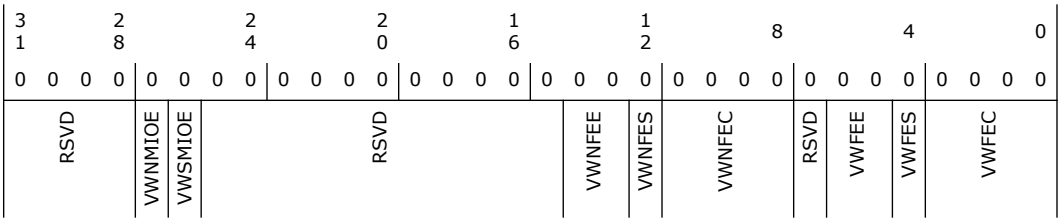
3.2.4 Virtual Wire Channel Error for Channel 0 (VWERR_SLV0)—Offset 4030h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	Reserved.
27	0h RW	**Master NMIOUT (Virtual Wire) to Slave Enable (VWNMIOE):** 0: Disable NMIOUT# reporting 1: Enable NMIOUT# reporting to Slave via eSPI Virtual Wire Note: This field is supported for server platforms only [Server SKU]. Note: This bit is locked when VWNSMIEL = 1.
26	0h RW	**Master SMIOUT (Virtual Wire) to Slave Enable (VWSMIOE):** 0: Disable SMIOUT# reporting (SMI#_Sent indication from PMC is ignored) 1: Enable SMIOUT# reporting to Slave via eSPI Virtual Wire (upon receiving a SMI#_Sent indication from PMC) Note: This field is supported for server platforms only [Server SKU. Note: This bit is locked when VWNSMIEL = 1.
25:15	0h RO	Reserved.
14:13	0h RW	**Virtual Wire Channel Non-Fatal Error Reporting Enable (VWNFEE):** 00: Disable Non-Fatal Error Reporting 01: Reserved 10: Enable Non-Fatal Error Reporting as SERR (SB Do_SErr message) 11: Enable Non-Fatal Error Reporting as SMI (SB Assert_SMI message) Note: SERR enable is also qualified by PCCMD.SEE (Offset 04h) when PLTRST# is deasserted. Note: SERR also sets PCSTS.SSE (Offset 06h) when PLTRST# is deasserted. Note: SMI/SERR messages are not generated if the Host is in reset (PLTRST# asserted).
12	0h RW/1C/V	**Virtual Wire Channel Non-Fatal Error Status (VWNFES):** This field is set by hardware if a Non-Fatal Error condition is detected on the Virtual Wire Channel. Software must clear this bit. 0: No Non-Fatal Error detected 1: Non-Fatal Error detected (VWNFEC has a non-zero value) Note: Clearing this unlocks the VWNFEC field and triggers an SB Deassert_SMI message if VWNFEE is set to SMI. Note: Setting of this bit is independent of the enable to generate a SMI/SERR (VWNFEE).
11:8	0h RO/V	**Virtual Wire Channel Non-Fatal Error Cause (VWNFEC):** 0h: No error 1h: Slave Response Code: NONFATAL_ERROR 2h – Dh: Reserved Eh: Slave Virtual Wire: NON_FATAL_ERROR: 0 to 1 transition (1 to 0 transition on this VW is ignored) Fh: Reserved Note: This field is updated after a Virtual Wire Channel transaction is completed if the VWNFES bit is not set.
7	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
6:5	0h RW	**Virtual Wire Channel Fatal Error Reporting Enable (VWFEE):** 00: Disable Fatal Error Reporting 01: Reserved 10: Enable Fatal Error Reporting as SERR (IOSF-SB Do_SErr message) 11: Enable Fatal Error Reporting as SMI (SB Assert_SMI message) Note: SERR enable is also qualified by PCCMD.SEE (Offset 04h) when PLTRST# is deasserted. Note: SERR also sets PCSTS.SSE (Offset 06h) when PLTRST# is deasserted. Note: SMI/SERR messages are not generated if the Host is in reset (PLTRST# asserted).
4	0h RW/1C/V	**Virtual Wire Channel Fatal Error Status (VWFES):** This field is set by hardware if a Fatal Error condition is detected on the Virtual Wire Channel. Software must clear this bit by writing all 1s to it. 0: No Fatal Error detected 1: Fatal Error Type 2 detected (VWFEC has a non-zero value) Note: Clearing this unlocks the VWFEC field and triggers an SB Deassert_SMI message if VWFEE is set to SMI. Note: Setting of this bit is independent of the enable to generate a SMI/SERR (VWFEE).
3:0	0h RO/V	**Virtual Wire Channel Fatal Error Cause (VWFEC):** 0h: No error 1h – 7h: Reserved 8h: Malformed Slave Response Payload: VW Count > Max. VW Count [Type 2] 9h – 4'hD: Reserved Eh: Slave Virtual Wire: FATAL_ERROR 0 to 1 transition (1 to 0 transition on this VW is ignored) [Type 2] Fh: Reserved Note: This field is updated after a Virtual Wire Channel transaction is completed if the VWFES bit is not set.

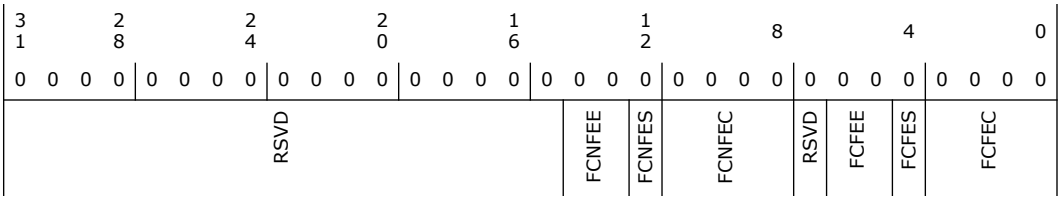
3.2.5 Flash Access Channel Error for Slave 0 (FCERR_SLV0)—Offset 4040h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RO	Reserved.
14:13	0h RW	**Flash Access Channel Non-Fatal Error Reporting Enable (FCNFEE):** 00: Disable Non-Fatal Error Reporting 01: Reserved 10: Enable Non-Fatal Error Reporting as SERR (SB Do_SErr message) 11: Enable Non-Fatal Error Reporting as SMI (SB Assert_SMI message) Note: SERR enable is also qualified by PCCMD.SEE (Offset 04h) when PLTRST# is deasserted. Note: SERR also sets PCSTS.SSE (Offset 06h) when PLTRST# is deasserted. Note: SMI/SERR messages are not generated if the Host is in reset (PLTRST# asserted).
12	0h RW/1C/V	**Flash Access Channel Non-Fatal Error Status (FCNFES):** This field is set by hardware if a Non-Fatal Error condition is detected on the Flash Access Channel. Software must clear this bit. 0: No Non-Fatal Error detected 1: Non-Fatal Error detected (FCNFEC has a non-zero value) Note: Clearing this unlocks the FCNFEC field and triggers an SB Deassert_SMI message if FCNFEE is set to SMI. Note: Setting of this bit is independent of the enable to generate a SMI/SERR (FCNFEE).
11:8	0h RO/V	**Flash Access Channel Non-Fatal Error Cause (FCNFEC):** 0h: No error 1h: Slave Response Code: NONFATAL_ERROR 2h: Slave Response Code: Unsuccessful Completion [for Slave-Attached Flash accesses only] 3h: Unexpected completion received from Slave (i.e. completion without non-posted request or completion with invalid tag or completion with invalid length) [for Slave-Attached Flash accesses only] 2h – 3h: Reserved 4h: Unsupported Cycle Type (w.r.t. Command) [for SPT-LP Master Attached Flash this should only be unsupported Erase Block Size] 5h: Reserved 6h: Unsupported Address (i.e., address > Flash linear address range) [for Master-Attached Flash accesses only] set to Flash Access Error 7h: Reserved 8h – Fh: Reserved Note: This field is updated after a Flash Access Channel transaction is completed if the FCNFES bit is not set
7	0h RO	Reserved.
6:5	0h RW	**Flash Access Channel Fatal Error Reporting Enable (FCFEE):** 00: Disable Fatal Error Reporting 01: Reserved 10: Enable Fatal Error Reporting as SERR (SB Do_SErr message) 11: Enable Fatal Error Reporting as SMI (SB Assert_SMI message) Note: SERR enable is also qualified by PCCMD.SEE (Offset 04h) when PLTRST# is deasserted. Note: SERR also sets PCSTS.SSE (Offset 06h) when PLTRST# is deasserted. Note: SMI/SERR messages are not generated if the Host is in reset (PLTRST# asserted).
4	0h RW/1C/V	**Flash Access Channel Fatal Error Status (FCFES):** This field is set by hardware if a Fatal Error condition is detected on the Flash Access Channel. Software must clear this bit by writing a 1 to it. 0: No Fatal Error detected 1: Fatal Error Type 2 detected (FCFEC has a non-zero value) Note: Clearing this unlocks the FCFEC field and triggers an IOSF-SB Deassert_SMI message if FCFEE is set to SMI. Note: Setting of this bit is independent of the enable to generate a SMI/SERR (FCFEE).
3:0	0h RO/V	**Flash Access Channel Fatal Error Cause (FCFEC):** 0h: No error 1h – 7h: Reserved 8h: Malformed Slave Response Payload: Payload length > Max Payload Size [Type 2] 9h: Malformed Slave Response Payload: Read request size > Max Read Request Size [for Master-Attached Flash accesses only] [Type 2] Ah – Fh: Reserved Note: This field is updated after a Flash Access Channel transaction is completed if the FCFES bit is not set.

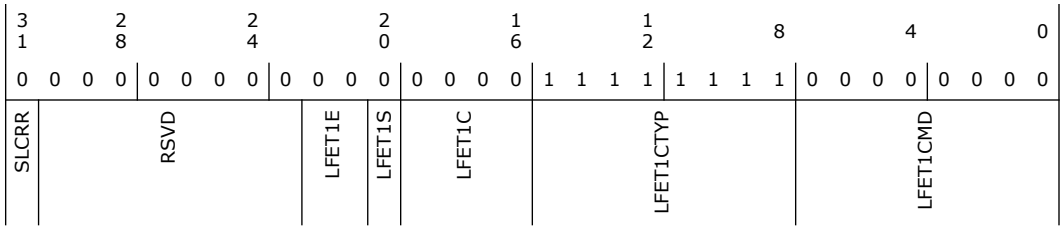
3.2.6 Link Error for Slave 0 (LNKERR_SL0)—Offset 4050h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: FF00h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C/V	**eSPI Link and Slave Channel Recovery Required (SLCRR):** HW sets this bit when it has detected a Type 1 Fatal Error condition, for any channel (LFET1C is non-zero). Setting of this bit will trigger an error handling sequence by the eSPI controller followed by the suspension of all HW initiated transactions on the eSPI link with the Slave. SW must clear this bit (by writing a 1 to it) after it has taken all necessary actions to recover the link. This indicates the eSPI controller to resume HW initiated transactions with the Slave.
30:23	0h RO	Reserved.
22:21	0h RW	**Fatal Error Type 1 Reporting Enable (LFET1E):** 00: Disable Fatal Error Type 1 Reporting 01: Reserved 10: Enable Fatal Error Type 1 Reporting as SERR (SB Do_SErr message) 11: Enable Fatal Error Type 1 Reporting as SMI (SB Assert_SMI message) Note: SERR enable is also qualified by PCCMD.SEE (Offset 04h) when PLTRST# is deasserted. Note: SERR also sets PCSTS.SSE (Offset 06h) when PLTRST# is deasserted. Note: SMI/SERR messages are not generated if the Host is in reset (PLTRST# asserted). Note: When this error is reported, SW must also inspect and handle the SLCRR field.
20	0h RW/1C/V	**Fatal Error Type 1 Reporting Status (LFET1S):** This field is set by hardware if a Link Fatal Error Type 1 condition is detected on the eSPI link (any transaction). Software must clear this bit by writing a 1 to it. 0: No Link Fatal Error Type 1 detected 1: Fatal Error Type 1 detected (LFET1C has a non-zero value. Note: Clearing this unlocks the LFET1C field and triggers an SB Deassert_SMI message if LFET1E is set to SMI. Note: Setting of this bit is independent of the enable to generate a SMI/SERR (LFET1E).

Bit Range	Default & Access	Field Name (ID): Description
19:16	0h RO/V	**Link Fatal Type 1 cause (LFET1C):** 0h: No error 1h: Slave Response Code: NO_RESPONSE [Type 1] 2h: Slave Response Code: FATAL_ERROR [Type 1] 3h: Slave Response Code: CRC_ERROR [Type 1] 4h: Invalid Slave Response Code (w.r.t. to Command) [Type 1] 5h: Invalid Slave Cycle Type (w.r.t. to Command) [Type 1] 6h – Fh: Reserved Note: This field is updated after a transaction (any channel) is completed if the LFET1S bit is clear. Note: A non-zero value in this field also causes the SLCRR bit to be set.
15:8	FFh RO/V	**Link Fatal Error Type 1 Cycle Type (LFET1CTYP):** When LFET1C is set, this field reflects the Cycle Type for the transaction that encountered the Fatal Error Type 1. If no valid Cycle Type exists w.r.t. the Command (LFET1CMD), this field is set to FFh to indicate that it should be ignored. Note: This field is updated after a transaction (any channel) is completed if the LFET1S bit is clear.
7:0	0h RO/V	**Link Fatal Error Type 1 Command (LFET1CMD):** When LFET1C is set, this field reflects the Command for the transaction that encountered the Fatal Error Type 1. Note: This field is updated after a transaction (any channel) is completed if the LFET1S bit is clear.

§ §

4 P2SB Bridge (D31:F1)

4.1 P2SB Configuration Registers Summary

Table 4-1. Summary of P2SB Configuration Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	PCI Identifier (PCIID)—Offset 0h	XXXX8086h
4h	5h	PCI Command (PCICMD)—Offset 4h	4h
8h	8h	Revision ID (PCIRID)—Offset 8h	See Register
9h	Ch	Class Code (PCICC)—Offset 9h	58000h
Eh	Eh	PCI Header Type (PCIHTYPE)—Offset Eh	0h
10h	13h	Sideband Register Access BAR (SBREG_BAR)—Offset 10h	4h
14h	17h	Sideband Register BAR High DWORD (SBREG_BARH)—Offset 14h	0h
2Ch	2Fh	PCI Subsystem Identifiers (PCIHSS)—Offset 2Ch	0h
50h	51h	VLW Bus:Device:Function (VBDF)—Offset 50h	F8h
52h	53h	ERROR Bus:Device:Function (EBDF)—Offset 52h	F8h
54h	57h	Routing Configuration (RCFG)—Offset 54h	C700h
60h	60h	High Performance Event Timer Configuration (HPTC)—Offset 60h	0h
64h	65h	IOxAPIC Configuration (IOAC)—Offset 64h	0h
6Ch	6Dh	IOxAPIC Bus:Device:Function (IBDF)—Offset 6Ch	F8h
70h	71h	HPET Bus:Device:Function (HBDF)—Offset 70h	F8h
80h	83h	Sideband Register posted 0 (SBREGPOSTED0)—Offset 80h	0h
84h	87h	Sideband Register posted 1 (SBREGPOSTED1)—Offset 84h	0h
88h	8Bh	Sideband Register posted 2 (SBREGPOSTED2)—Offset 88h	0h
8Ch	8Fh	Sideband Register posted 3 (SBREGPOSTED3)—Offset 8Ch	0h
90h	93h	Sideband Register posted 4 (SBREGPOSTED4)—Offset 90h	0h
94h	97h	Sideband Register posted 5 (SBREGPOSTED5)—Offset 94h	0h
98h	9Bh	Sideband Register posted 6 (SBREGPOSTED6)—Offset 98h	0h
9Ch	9Fh	Sideband Register posted 7 (SBREGPOSTED7)—Offset 9Ch	0h
A0h	A3h	Display Bus:Device:Function (DISPBDF)—Offset A0h	60010h
A4h	A5h	ICC Register Offsets (ICCOS)—Offset A4h	0h
B0h	B3h	Endpoint Mask 0 (EPMASK0)—Offset B0h	0h
B4h	B7h	Endpoint Mask 1 (EPMASK1)—Offset B4h	0h
B8h	BBh	Endpoint Mask 2 (EPMASK2)—Offset B8h	0h
BCh	BFh	Endpoint Mask 3 (EPMASK3)—Offset BCh	0h
C0h	C3h	Endpoint Mask 4 (EPMASK4)—Offset C0h	0h
C4h	C7h	Endpoint Mask 5 (EPMASK5)—Offset C4h	0h
C8h	CBh	Endpoint Mask 6 (EPMASK6)—Offset C8h	0h
CCh	CFh	Endpoint Mask 7 (EPMASK7)—Offset CCh	0h

Table 4-1. Summary of P2SB Configuration Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
D0h	D3h	SBI Address (SBIADDR)—Offset D0h	0h
D4h	D7h	SBI Data (SBIDATA)—Offset D4h	0h
D8h	D9h	SBI Status (SBISTAT)—Offset D8h	0h
DAh	DBh	SBI Routing Identification (SBIRID)—Offset DAh	0h
DCh	DFh	SBI Extended Address (SBIEXTADDR)—Offset DCh	0h
E0h	E3h	P2SB Control (P2SBC)—Offset E0h	0h
E4h	E4h	Power Control Enable (PCE)—Offset E4h	1h

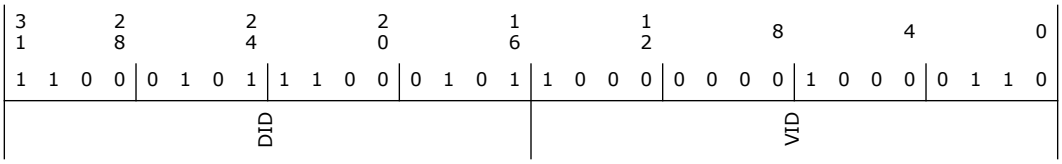
4.1.1 PCI Identifier (PCIID)—Offset 0h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 1

Default: XXXX8086h



Bit Range	Default & Access	Field Name (ID): Description
31:16	XXXXh RO	**Device Identification (DID):** Indicates the device identification. See Volume 1 for the specific value.
15:0	8086h RO	**Vendor Identification (VID):** Indicates Intel

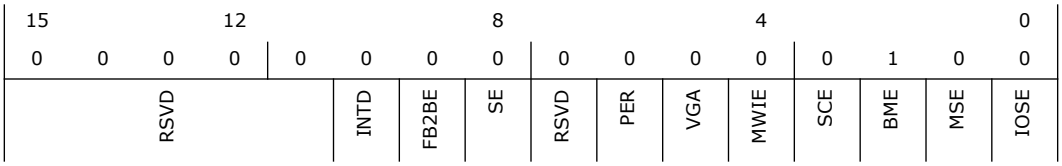
4.1.2 PCI Command (PCICMD)—Offset 4h

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 1

Default: 4h



Bit Range	Default & Access	Field Name (ID): Description
15:11	0h RO	Reserved.
10	0h RO	**Interrupt Disable (INTD):** P2SB does not issue any interrupts on its own behalf
9	0h RO	**Fast Back to Back Enable (FB2BE):** Not applicable
8	0h RO	**SERR# Enable (SE):** P2SB does not issue SERR# on its own behalf.
7	0h RO	Reserved.
6	0h RO	**Parity Error Response (PER):** No support for parity error detection.
5	0h RO	**VGA Palette Snoop (VGA):** Not applicable.
4	0h RO	**Memory Write & Invalidate Enable (MWIE):** Not applicable.
3	0h RO	**Special Cycle Enable (SCE):** Not applicable.
2	1h RO	**Bus Master Enable (BME):** Bus mastering cannot be disabled as this device acts as a proxy for non-PCI devices.
1	0h RW	**Memory Space Enable (MSE):** Will control the P2SB acceptance of PCI MMIO BARs only. Other legacy regions are unaffected by this bit.
0	0h RW	**I/O Space Enable (IOSE):** Legacy regions are unaffected by this bit.

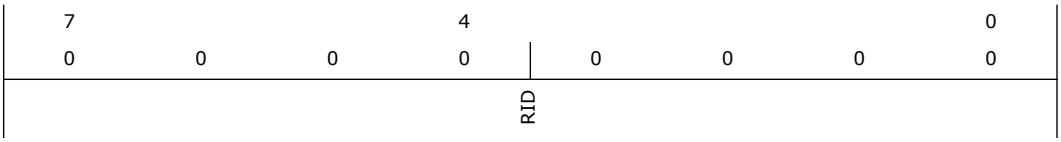
4.1.3 Revision ID (PCIRID)—Offset 8h

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 31
Function: 1

Default: See Register



Bit Range	Default & Access	Field Name (ID): Description
7:0	--- RO	**Revision ID (RID):** Indicates stepping of the host controller. Refer to Device and Revision ID table in Vol1 for specific value.

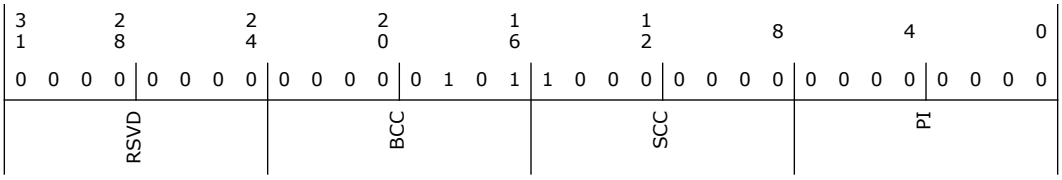
4.1.4 Class Code (PCICC)—Offset 9h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 1

Default: 58000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:16	5h RO	**Base Class Code (BCC):** Indicates a memory controller device class.
15:8	80h RO	**Sub-Class Code (SCC):** Indicates an unspecified other memory controller.
7:0	0h RO	**Programming Interface (PI):** No programming interface.

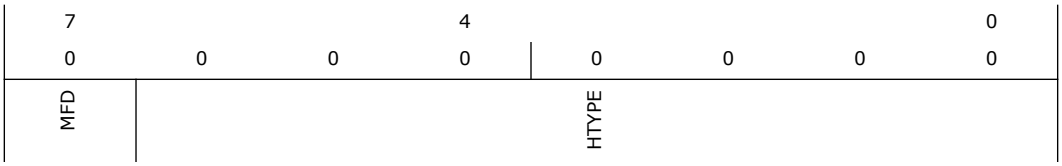
4.1.5 PCI Header Type (PCIHTYPE)—Offset Eh

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 31
Function: 1

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Multi-Function Device (MFD):** Indicates that this is part of a multi-function device.
6:0	0h RO	**Header Type (HTYPE):** Indicates a generic device header.

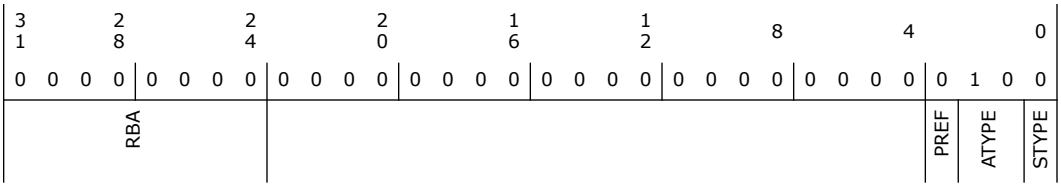
4.1.6 Sideband Register Access BAR (SBREG_BAR)—Offset 10h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 1

Default: 4h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW	**Register Base Address (RBA):** Lower DWORD of the base address for the sideband register access BAR.
23:4	0h RO	**:** Hardwired to 0 to request a BAR of 16MB
3	0h RO	**Prefetchable (PREF):** Indicates this is not prefetchable.
2:1	2h RO	**Address Type (ATYPE):** Indicates that this can be placed anywhere in 64b space.
0	0h RO	**Space Type (STYPE):** Indicates memory space

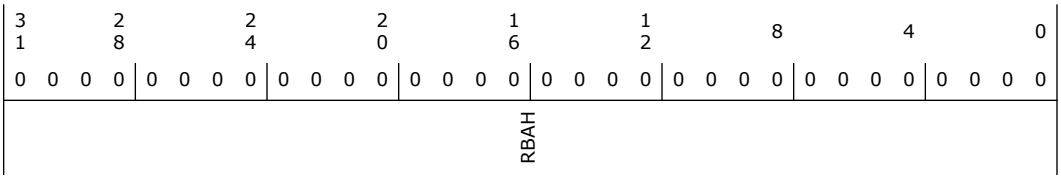
4.1.7 Sideband Register BAR High DWORD (SBREG_BARH)—Offset 14h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 1

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Register Base Address (RBAH):** Upper DWORD of the base address for the sideband register access BAR.

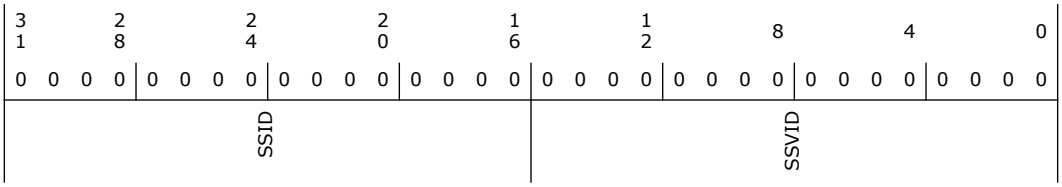
4.1.8 PCI Subsystem Identifiers (PCIHSS)—Offset 2Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 1

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW/O	**Subsystem ID (SSID):** Written by BIOS. Not used by hardware.
15:0	0h RW/O	**Subsystem Vendor ID (SSVID):** Written by BIOS. Not used by hardware.

4.1.9 VLW Bus:Device:Function (VBDF)—Offset 50h

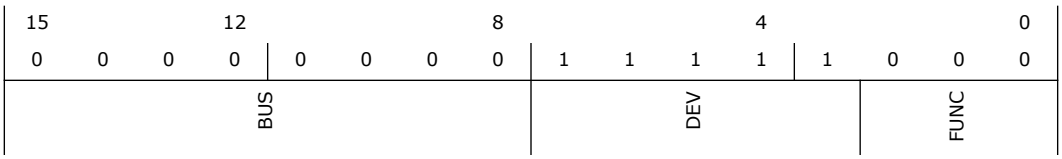
This register specifies the bus:device:function ID that will be used for its Requester ID. This field is default to Bus 0: Device 31: Function 0 after reset. BIOS shall program this field accordingly if unique bus:device:function number is required.

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 1

Default: F8h



Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RW	**Bus Number (BUS)**
7:3	1Fh RW	**Device Number (DEV)**
2:0	0h RW	**Function Number (FUNC)**

4.1.10 ERROR Bus:Device:Function (EBDF)—Offset 52h

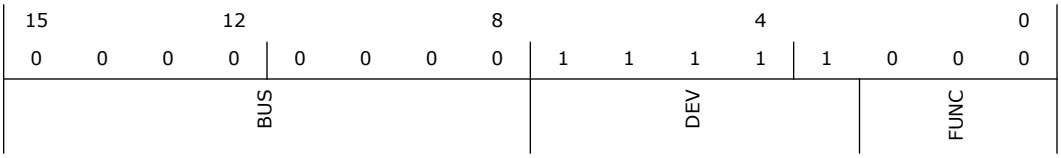
This register specifies the bus:device:function ID that the Error Signalling messages will use for its Requester ID. This field is default to Bus 0: Device 31: Function 0 after reset. BIOS shall program this field accordingly if unique bus:device:function number is required.

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 1

Default: F8h



Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RW	**Bus Number (BUS)**
7:3	1Fh RW	**Device Number (DEV)**
2:0	0h RW	**Function Number (FUNC)**

4.1.11 Routing Configuration (RCFG)—Offset 54h

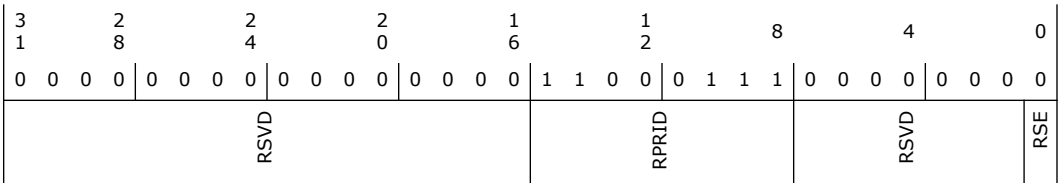
This register contains information used for routing transactions between primary and sideband interfaces.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 1

Default: C700h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:8	C7h RW	**Reserved Page Register Destination ID (RPRID):** Specifies the IOSF-SB destination ID for sending Reserved Page Register cycles (e.g. Port 80h). By default this will load to the ID of the LPC or eSPI device depending on which has been strapped active in the system.
7:1	0h RO	Reserved.
0	0h RW	**RTC Shadow Enable (RSE):** When set, all IO writes to the RTC will be also sent to the PMC. This allows cases where the battery backed storage is in an external PMIC.

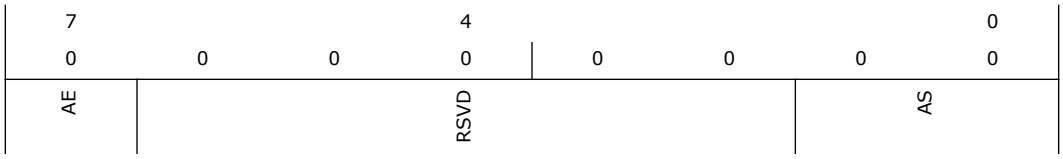
4.1.12 High Performance Event Timer Configuration (HPTC)—Offset 60h

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 31
Function: 1

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Address Enable (AE):** When set, the P2SB will decode the High Performance Timer memory address range selected by bits 1:0 below.
6:2	0h RO	Reserved.
1:0	0h RW	**Address Select (AS):** This 2-bit field selects 1 of 4 possible memory address ranges for the High Performance Timer functionality. The encodings are: 00 : FED0_0000h - FED0_03FFFh 01 : FED0_1000h - FED0_13FFFh 10 : FED0_2000h - FED0_23FFFh 11 : FED0_3000h - FED0_33FFFh

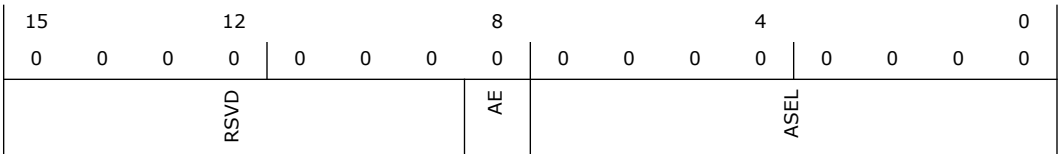
4.1.13 IOxAPIC Configuration (IOAC)—Offset 64h

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 1

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:9	0h RO	Reserved.
8	0h RW	**Address Enable (AE):** When set, the P2SB will decode the IOxAPIC memory address range selected by bits 7:0 below.
7:0	0h RW	**APIC Range Select (ASEL):** These bits define address bits 19:12 for the IOxAPIC range. The default value of 00h enables compatibility with prior products as an initial value. This value must not be changed unless the IOxAPIC Enable bit is cleared.

4.1.14 IOxAPIC Bus:Device:Function (IBDF)—Offset 6Ch

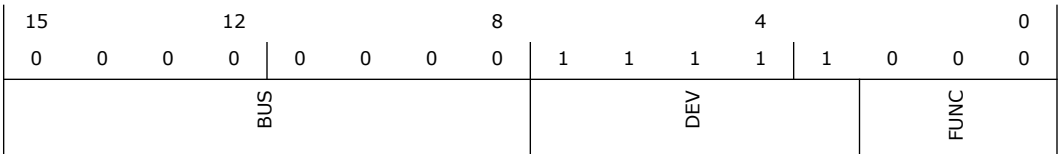
This register specifies the bus:device:function ID that the IOxAPIC will use in the following: As the Requester ID when initiating Interrupt Messages to the CPU As the Completer ID when responding to the reads targeting the IOxAPICs Memory-Mapped I/O registers This field is default to Bus 0: Device 31: Function 0 after reset. BIOS shall program this field accordingly if unique bus:device:function number is required for the internal IOxAPIC.

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 1

Default: F8h



Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RW	**Bus Number (BUS)**
7:3	1Fh RW	**Device Number (DEV)**
2:0	0h RW	**Function Number (FUNC)**

4.1.15 HPET Bus:Device:Function (HBDF)—Offset 70h

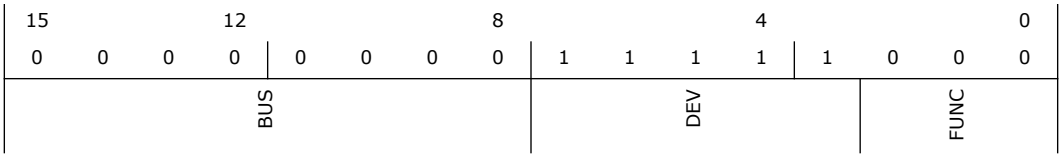
This register specifies the bus:device:function ID that the HPET device will use in the following : As the Requester ID when initiating Interrupt Messages to the CPU As the Completer ID when responding to the reads targeting the corresponding HPETs Memory-Mapped I/O registers This field is default to Bus 0: Device 31: Function 0 after reset. BIOS shall program this field accordingly if unique bus:device:function number is required for the corresponding HPET.

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 1

Default: F8h



Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RW	**Bus Number (BUS)**
7:3	1Fh RW	**Device Number (DEV)**
2:0	0h RW	**Function Number (FUNC)**

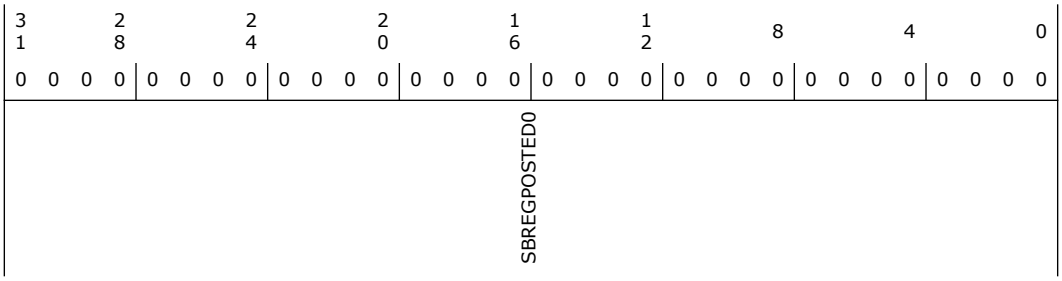
4.1.16 Sideband Register posted 0 (SBREGPOSTED0)—Offset 80h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 1

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Sideband Register posted 0 (SBREGPOSTED0):** One hot masks for setting SBREG to posted posted for IOSF-SB endpoint IDs 31-0.

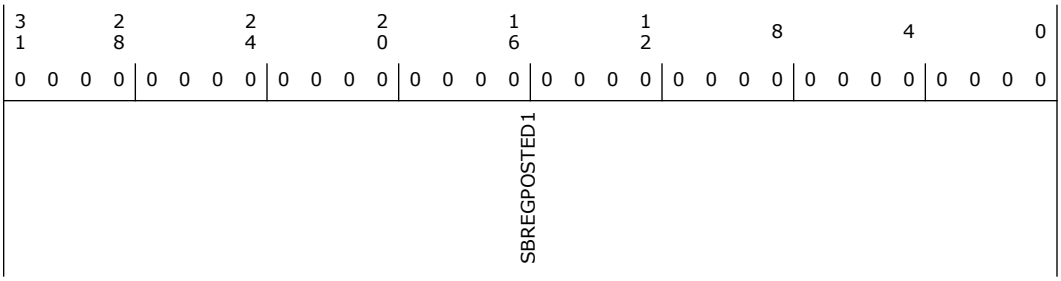
4.1.17 Sideband Register posted 1 (SBREGPOSTED1)—Offset 84h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 1

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Sideband Register posted 1 (SBREGPOSTED1):** One hot masks for setting SBREG to posted posted for IOSF-SB endpoint IDs 63-32.

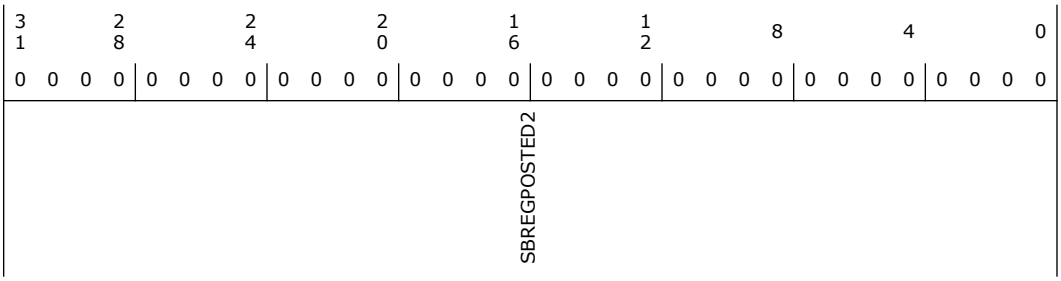
4.1.18 Sideband Register posted 2 (SBREGPOSTED2)—Offset 88h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 1

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Sideband Register posted 0 (SBREGPOSTED2):** One hot masks for setting SBREG to posted posted for IOSF-SB endpoint IDs 95-64.

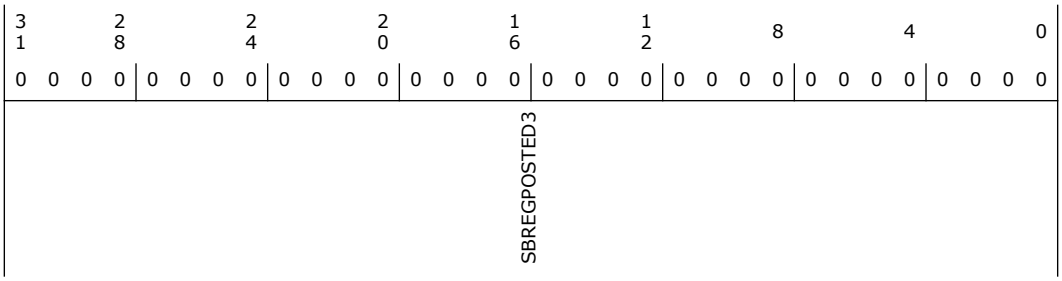
4.1.19 Sideband Register posted 3 (SBREGPOSTED3)—Offset 8Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 1

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Sideband Register posted 3 (SBREGPOSTED3):** One hot masks for setting SBREG to posted posted for IOSF-SB endpoint IDs 127-96.

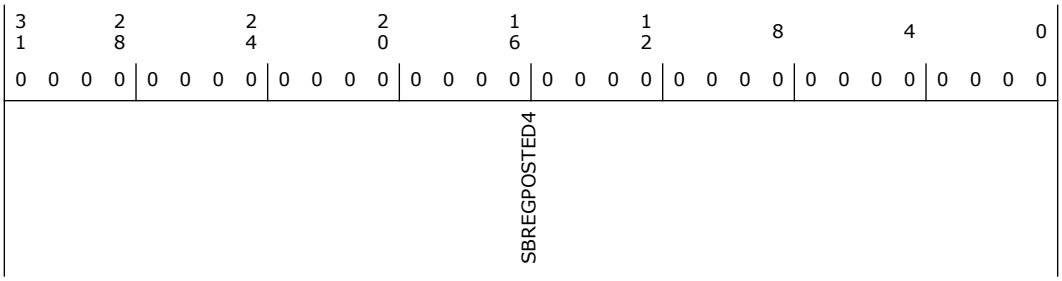
4.1.20 Sideband Register posted 4 (SBREGPOSTED4)—Offset 90h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 1

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Sideband Register posted 4 (SBREGPOSTED4):** One hot masks for setting SBREG to posted posted for IOSF-SB endpoint IDs 159-128.

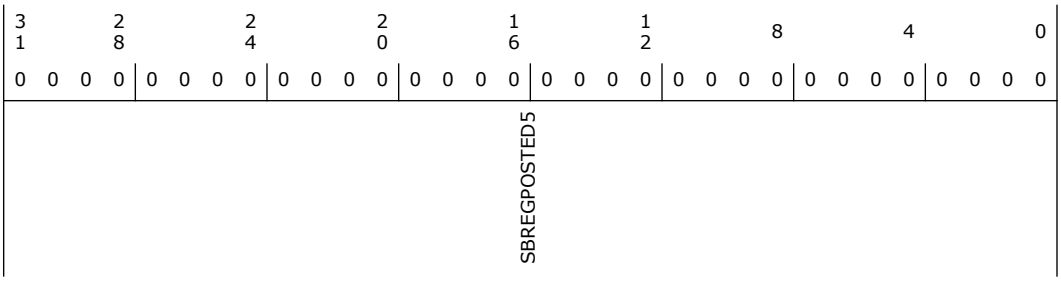
4.1.21 Sideband Register posted 5 (SBREGPOSTED5)—Offset 94h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 1

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Sideband Register posted 5 (SBREGPOSTED5):** One hot masks for setting SBREG to posted posted for IOSF-SB endpoint IDs 191-160.

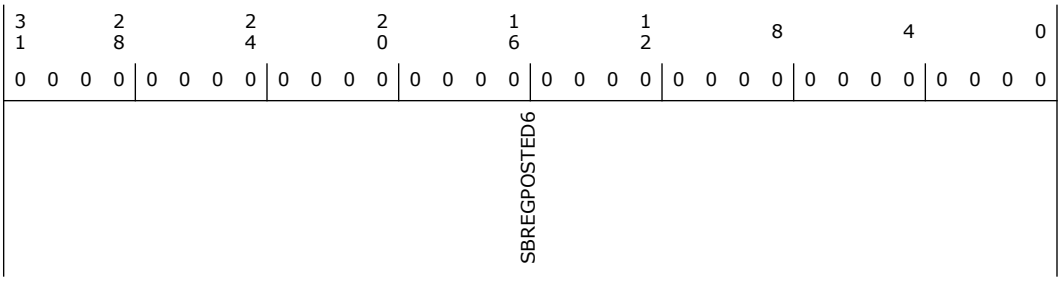
4.1.22 Sideband Register posted 6 (SBREGPOSTED6)—Offset 98h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 1

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Sideband Register posted 6 (SBREGPOSTED6):** One hot masks for setting SBREG to posted posted for IOSF-SB endpoint IDs 223-192.

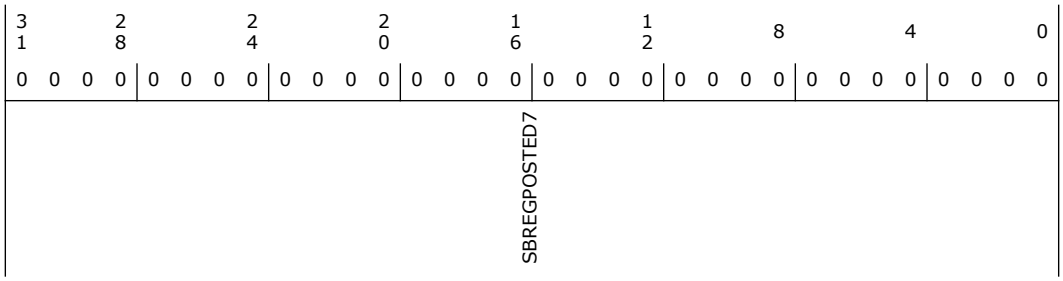
4.1.23 Sideband Register posted 7 (SBREGPOSTED7)—Offset 9Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 1

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Sideband Register posted 7 (SBREGPOSTED7):** One hot masks for setting SBREG to posted posted for IOSF-SB endpoint IDs 255-224.

4.1.24 Display Bus:Device:Function (DISPBDF)—Offset A0h

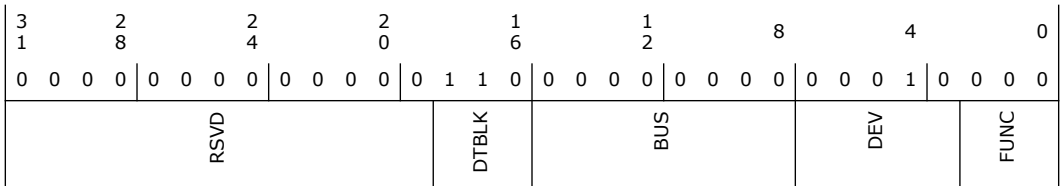
This register specifies the bus:device:function ID that the Display initiated upstream RAVDMs will use for its Requester ID. This will also be used for the claiming these Route-by-ID RAVDMs downstream.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 1

Default: 60010h



Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	Reserved.
18:16	6h RW	**Display Target Block (DTBLK):** This register contains the Target BLK field that will be used when sending RAVDM messages to the CPU Complex North Display.
15:8	0h RW	**Bus Number (BUS):** The bus number of the Display in the CPU Complex.
7:3	2h RW	**Device Number (DEV):** The bus number of the Display in the CPU Complex.
2:0	0h RW	**Function Number (FUNC):** The function number of the Display in the CPU Complex

4.1.25 ICC Register Offsets (ICCOS)—Offset A4h

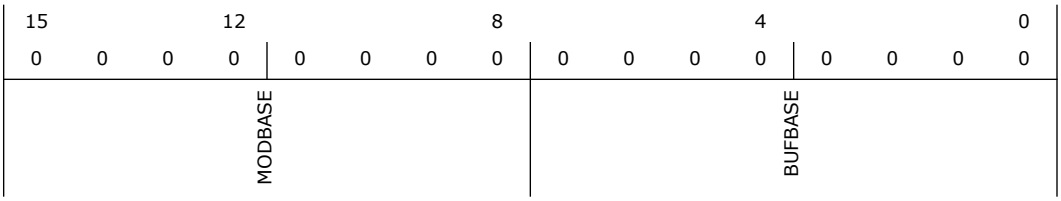
This register contains the offsets to be used when sending RAVDMs to the Integrated Clock Controller. Each of the two spaces decoded for the ICC have a separate base address that will be used when sending those transactions on IOSF-SB to the ICC.

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 1

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RW	**Modulator Control Address Offset (MODBASE):** This specifies the upper 8b for the 16b address that will be used for sending RAVDM access that target the Modulator Control range of the ICC (FFF00h - FFFFFh).
7:0	0h RW	**Buffer Address Offset (BUFBASE):** This specifies the upper 8b for the 16b address that will be used for sending RAVDM access that target the Buffer range of the ICC (FFE00h - FFEFFh).

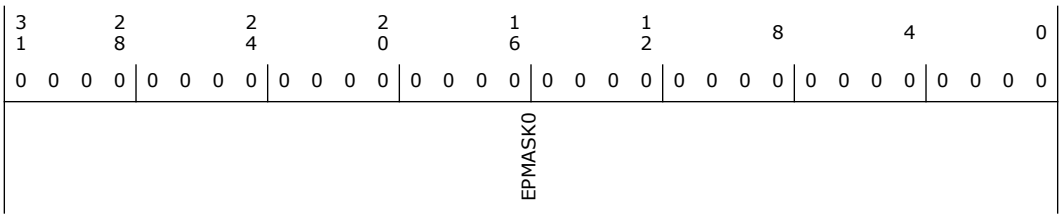
4.1.26 Endpoint Mask 0 (EPMASK0)—Offset B0h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 1

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/L	**Endpoint Mask 0 (EPMASK0):** One hot masks for disabling IOSF-SB endpoint IDs 31-0.

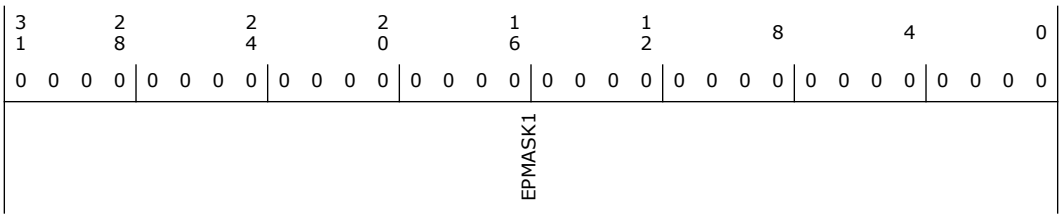
4.1.27 Endpoint Mask 1 (EPMASK1)—Offset B4h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 1

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/L	**Endpoint Mask 1 (EPMASK1):** One hot masks for disabling IOSF-SB endpoint IDs 63-32.

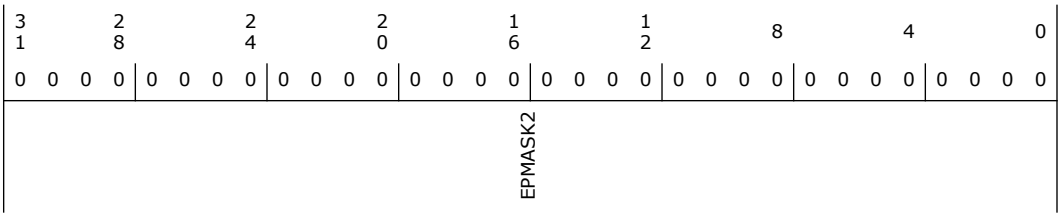
4.1.28 Endpoint Mask 2 (EPMASK2)—Offset B8h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 1

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/L	**Endpoint Mask 2 (EPMASK2):** One hot masks for disabling IOSF-SB endpoint IDs 95-64

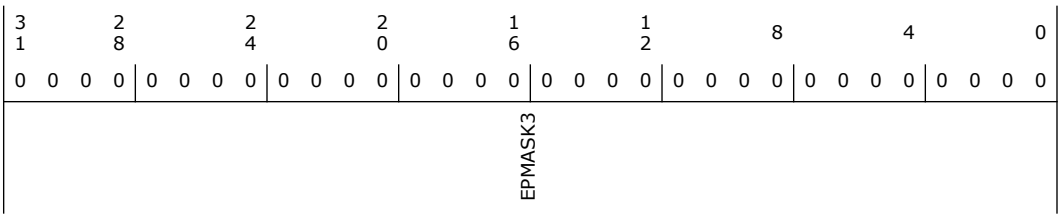
4.1.29 Endpoint Mask 3 (EPMASK3)—Offset BCh

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 1

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/L	**Endpoint Mask 3 (EPMASK3):** One hot masks for disabling IOSF-SB endpoint IDs 127-96

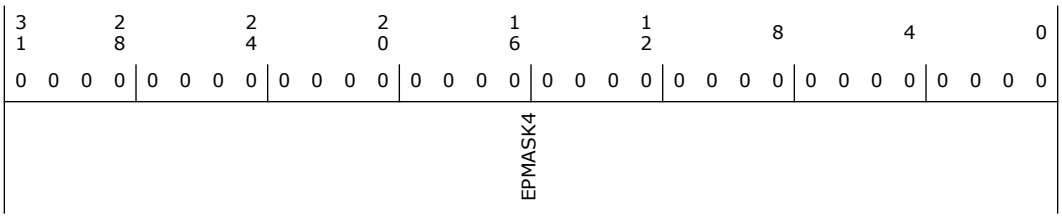
4.1.30 Endpoint Mask 4 (EPMASK4)—Offset C0h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 1

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/L	**Endpoint Mask 4 (EPMASK4):** One hot masks for disabling IOSF-SB endpoint IDs 128-159

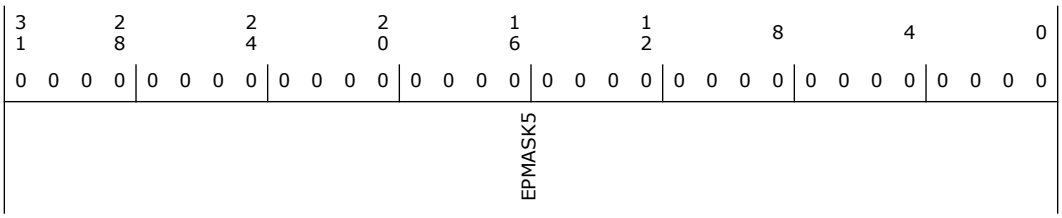
4.1.31 Endpoint Mask 5 (EPMASK5)—Offset C4h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 1

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/L	**Endpoint Mask 5 (EPMASK5):** One hot masks for disabling IOSF-SB endpoint IDs 191-160

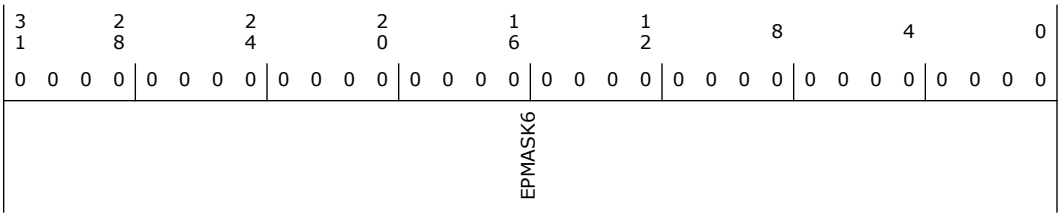
4.1.32 Endpoint Mask 6 (EPMASK6)—Offset C8h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 1

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/L	**Endpoint Mask 6 (EPMASK6):** One hot masks for disabling IOSF-SB endpoint IDs 223-192

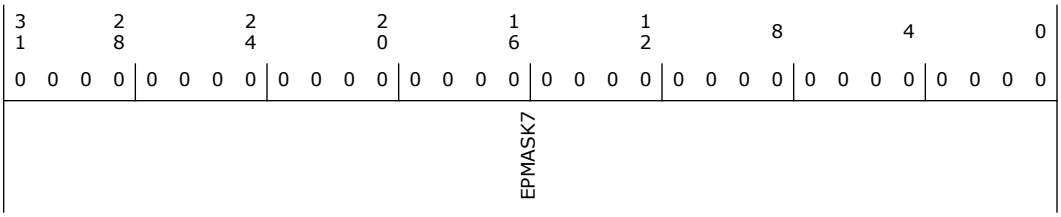
4.1.33 Endpoint Mask 7 (EPMASK7)—Offset CCh

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 1

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/L	**Endpoint Mask 7 (EPMASK7):** One hot masks for disabling IOSF-SB endpoint IDs 255-224

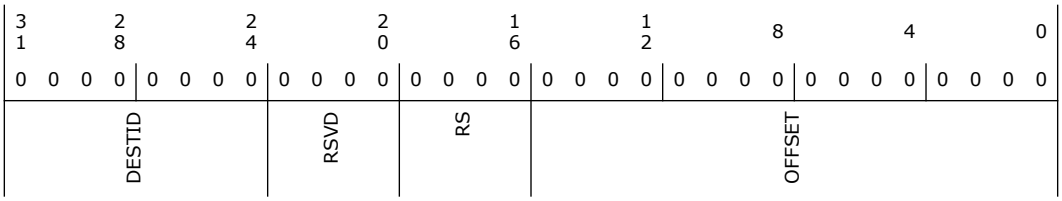
4.1.34 SBI Address (SBIADDR)—Offset D0h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 1

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW	**Destination Port ID (DESTID):** The content of this register field is sent in the IOSF Sideband Message Register Access dest field.
23:20	0h RO	Reserved.
19:16	0h RW	**Root Space (RS):** Destination IOSF-SB Root Space. *Note: This register may only be written during manufacturing test. P2SB will only accept writes to this register from transactions with a SAI equal to the SBI_RS_ACCESS_SAI parameter. This should be assigned to the SAI used by the functional test module (typically TAM) that will perform this register write on IOSF-P.
15:0	0h RW	**Address Offset (OFFSET):** Register address offset. The content of this register field is sent in the IOSF Sideband Message Register Access address(15:0) field.

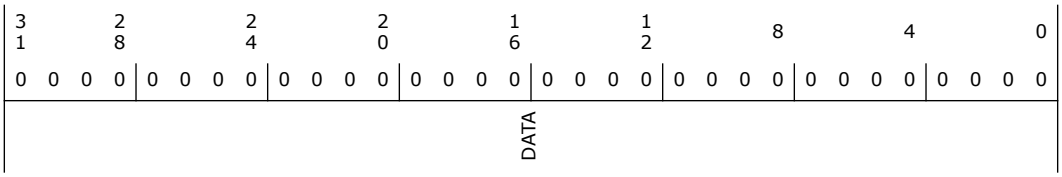
4.1.35 SBI Data (SBIDATA)—Offset D4h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 1

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Data (DATA):** The content of this register field is sent on the IOSF sideband Message Register Access data(31:0) field.

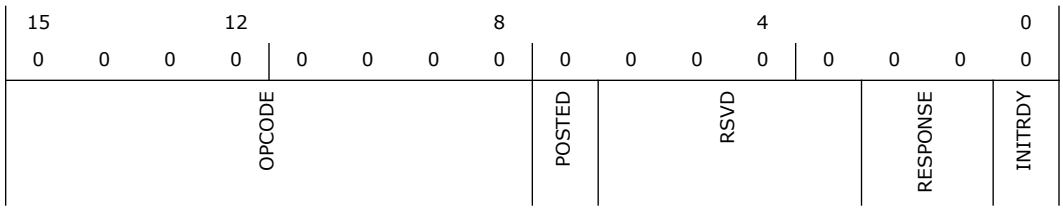
4.1.36 SBI Status (SBISTAT)—Offset D8h

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 1

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RW	**Opcode (OPCODE):** This is the Opcode sent in the IOSF sideband message.
7	0h RW	**Posted (POSTED):** When set to 1, the message will be send as a posted message instead of non-posted. This should only be used if the receiver is known to support posted operations for the specified operation.
6:3	0h RO	Reserved.
2:1	0h RO/V	**Response Status (RESPONSE):** 00 - Successful 01 - Unsuccessful / Not Supported 10 - Powered Down 11 - Multi-cast Mixed This register reflects the response status for the previously completed transaction. The value of this register is only meaningful if SBISTAT.INITRDY is zero.
0	0h RW/V/L	**Initiate/ Ready# (INITRDY):** 0: The IOSF sideband interface is ready for a new transaction 1: The IOSF sideband interface is busy with the previous transaction. A write to set this register bit to 1 will trigger an IOSF sideband message on the private IOSF sideband interface. The message will be formed based on the values programmed in the Sideband Message Interface Register Access registers. Software needs to ensure that the interface is not busy (SBISTAT.INITRDY is clear) before writing to this register.

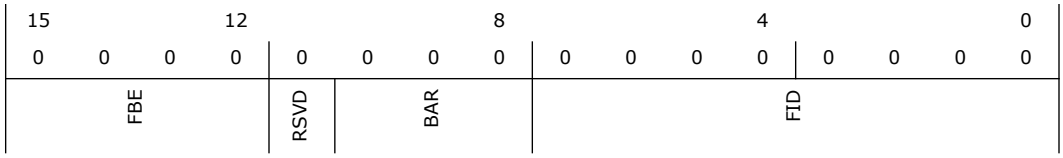
4.1.37 SBI Routing Identification (SBIRID)—Offset DAh

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 1

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:12	0h RW	**First Byte Enable (FBE):** The content of this field is sent in the IOSF Sideband Register Access FBE field.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RO	Reserved.
10:8	0h RW	**Base Address Register (BAR):** The contents of this field are sent in the IOSF Sideband Register Access BAR field. This should be zero performing a Memory Mapped operation to a PCI compliant device.
7:0	0h RW	**Function ID (FID):** The contents of this field are sent in the IOSF Sideband Register access FID field. This field should generally remain at zero unless specifically required by a particular application.

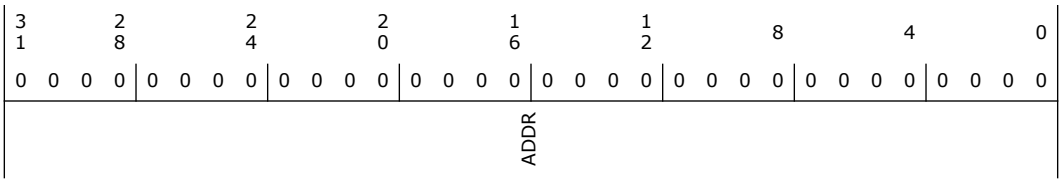
4.1.38 SBI Extended Address (SBIEXTADDR)—Offset DCh

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 1

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Extended Address (ADDR):** The content of this register field is sent on the IOSF sideband Message Register Access address(48:32) field. This must be set to all 0 if 16b addressing is desired.

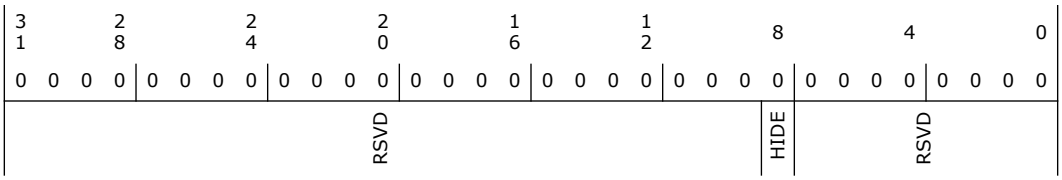
4.1.39 P2SB Control (P2SBC)—Offset E0h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 1

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h RW	**Hide Device (HIDE):** When this bit is set, the P2SB will return 1s on any PCI Configuration Read on IOSF-P. All other transactions including PCI Configuration Writes are unaffected by this. This does not affect reads performed on the IOSF-SB interface.
7:0	0h RO	Reserved.

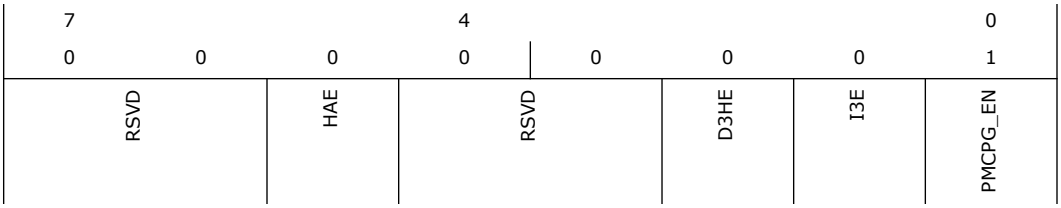
4.1.40 Power Control Enable (PCE)—Offset E4h

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 31
Function: 1

Default: 1h



Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	Reserved.
5	0h RW	**Hardware Autonomous Enable (HAE):** When set, the P2SB will automatically engage power gating when it has reached its idle condition.
4:3	0h RO	Reserved.
2	0h RO	**D3-Hot Enable (D3HE):** No support for D3 Hot power gating.
1	0h RO	**I3 Enable (I3E):** No support for S0i3 power gating.
0	1h RW	**PMC Power Gating Enable (PMCPG_EN):** When set to 1, the P2SB will engage power gating if it is idle and the pmc_p2sb_sw_pg_req_b signal is asserted.

§ §

5 PMC Controller (D31:F2)

5.1 Power Management Configuration Registers Summary

The power management registers are distributed within the PCI Device 31: Function 2 space, with dedicated I/O and memory-mapped spaces.
Bits not explicitly defined in each register are assumed to be reserved. Writes to reserved bits must retain their previous values. Other than a read/modify/write, software should not attempt to use the value read from a reserved bit, as it may not be consistently 1 or 0.

Table 5-1. Summary of Power Management Configuration Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	PCI Identifier (PCIID)—Offset 0h	8086h
4h	7h	Device Status & Command (PCISTS_PCICMD)—Offset 4h	4h
8h	Bh	Class Code & Revision ID (PCICC_PCIRID)—Offset 8h	5800000h
Ch	Fh	Header Type & Master Latency Timer (PCIHTYPE_PCIMLT)—Offset Ch	800000h
10h	13h	32-bit Power Management Data Base Address Register (PM_DATA_BAR)—Offset 10h	0h
2Ch	2Fh	Subsystem Identifiers (PCISID)—Offset 2Ch	0h
40h	43h	ACPI Base Address (ABASE)—Offset 40h	1h
44h	47h	ACPI Control (ACTL)—Offset 44h	0h
48h	4Bh	PM Base Address (PWRMBASE)—Offset 48h	0h
A0h	A3h	General PM Configuration A (GEN_PMCON_A)—Offset A0h	A0000000h
A4h	A7h	General PM Configuration B (GEN_PMCON_B)—Offset A4h	4006h
A8h	ABh	BM_BREAK_EN and Cx State Configuration Register (BM_CX_CNF)—Offset A8h	200h
ACh	AFh	Extended Test Mode Register 3 (ETR3)—Offset ACh	0h

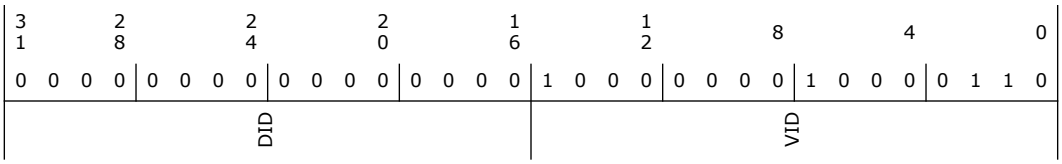
5.1.1 PCI Identifier (PCIID)—Offset 0h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 2

Default: 8086h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO/V	**Device Identification (DID):** These bits are controlled as follows: Bits [15:10]: Hardwired to 101111 for SPT-LP Bits [9:7]: Global device ID - 000 (Default) Bits [6:5]: Hardwired to 10 for SPT Bits [4:0]: DID (00 to 1F - variable).
15:0	8086h RO	**Vendor Identification (VID):** This is a 16-bit value assigned to Intel. Intel VID=8086h.

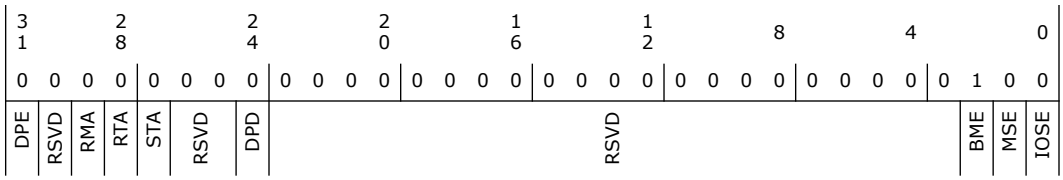
5.1.2 Device Status & Command (PCISTS_PCICMD)—Offset 4h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 2

Default: 4h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C/V	**Detected Parity Error (DPE):** Set when the bridge detects a parity error on the internal backbone. This bit is reset by PLTRST# assertion.
30	0h RO	Reserved.
29	0h RW/1C/V	**Received Master Abort (RMA):** Set when the bridge receives a completion with unsupported request status from the backbone. This bit is reset by PLTRST# assertion.
28	0h RW/1C/V	**Received Target Abort (RTA):** Set when the bridge receives a completion with completer abort status from the backbone. This bit is reset by PLTRST# assertion.
27	0h RW/1C/V	**Signaled Target Abort (STA):** Set when the bridge generates a completion packet with target abort status on the backbone. This bit is reset by PLTRST# assertion.
26:25	0h RO	Reserved.
24	0h RW/1C/V	**Data Parity Error Detected (DPD):** Set when the bridge receives a completion packet from the backbone from a previous request, and detects a parity error. This bit is reset by PLTRST# assertion.
23:3	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
2	1h RW	**Bus Master Enable (BME):** Bus master Enable does not apply to messages sent out by PMC. This bit is reset by PLTRST# assertion.
1	0h RW	**Memory Space Enable (MSE):** Controls a device's response to Memory Space accesses. This bit controls whether the host to PMC MMIO BAR is enabled or not. This bit is reset by PLTRST# assertion.
0	0h RO	**I/O Space Enable (IOSE):** PMC does not define any IO BARs in the standard PCI header BAR offsets.

5.1.3 Class Code & Revision ID (PCICC_PCIRID)—Offset 8h

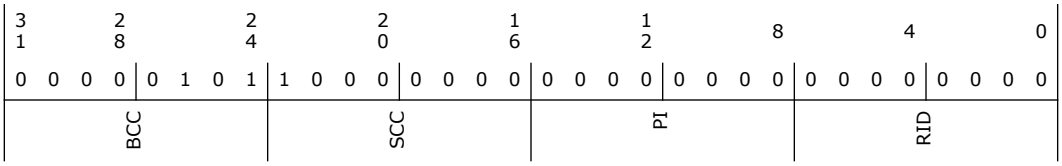
Writing to btis 7:0 of this register controls what is reported in the all of the RID fields of the corresponding registers in the component. The value written does not get directly loaded in this register. However, the value is checked to see which value to report.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 2

Default: 5800000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	5h RO	**Base Class Code (BCC):** Indicates a memory controller device class.
23:16	80h RO	**Sub-Class Code (SCC):** Indicates an unspecified 'other' memory controller.
15:8	0h RO	**Programming Interface (PI):** No programming interface.
7:0	0h RW/V	**Revision ID (RID):** Indicates stepping of the host controller. Refer to Device and Revision ID table in Volume 1 for specific value. This field is reset by PLTRST# assertion.

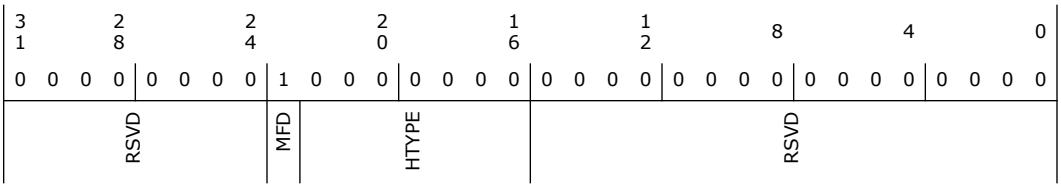
5.1.4 Header Type & Master Latency Timer (PCIHTYPE_PCIMLT)—Offset Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 2

Default: 800000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	1h RO	**Multi-Function Device (MFD):** Indicates that this is part of a multi-function device.
22:16	0h RO	**Header Type (HTYPE):** Indicates a generic device header.
15:0	0h RO	Reserved.

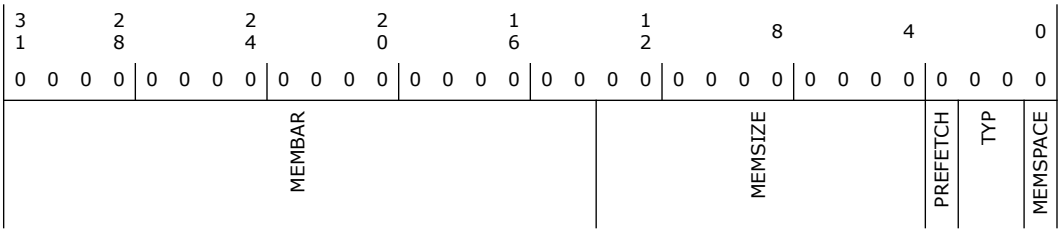
5.1.5 32-bit Power Management Data Base Address Register (PM_DATA_BAR)—Offset 10h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RW	**Memory BAR (MEMBAR):** Software programs this register with the base address of the device's memory region. This field is reset by PLTRST# assertion.
13:4	0h RO	**Memory Size (MEMSIZE):** Hardwired to 0 to indicate 16KB of memory space
3	0h RO	**Prefetchable (PREFETCH):** A device can mark a range as prefetchable if there are no side effects on reads, the device returns all bytes on reads regardless of the byte enables. Hardwired to 0 to indicate the device's memory space as notprefetchable.
2:1	0h RO	**Type (TYP):** Hardwired to 0 to indicate that Base register is 32 bits wide and mapping can be done anywhere in the 32-bit Memory Space.
0	0h RO	**Memory Space Indicator (MEMSPACE):** Hardwired to 0 to identify a Memory BAR.

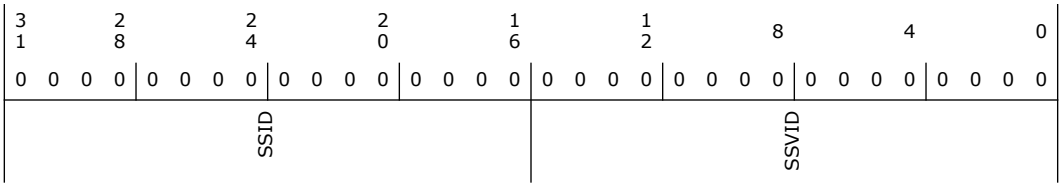
5.1.6 Subsystem Identifiers (PCISID)—Offset 2Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW/O	**Subsystem ID (SSID):** Written by BIOS. Not used by hardware. This field is reset by PLTRST# assertion.
15:0	0h RW/O	**Subsystem Vendor ID (SSVID):** Written by BIOS. Not used by hardware. This field is reset by PLTRST# assertion.

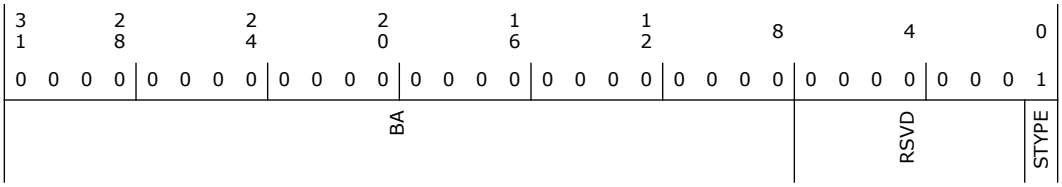
5.1.7 ACPI Base Address (ABASE)—Offset 40h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 2

Default: 1h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RW/L	**Base Address (BA):** Provides the 256 bytes of I/O space for ACPI logic. This field is reset by PLTRST# assertion.
7:1	0h RO	Reserved.
0	1h RO	**Space Type (STYPE):** Always 1 to indicate I/O space.

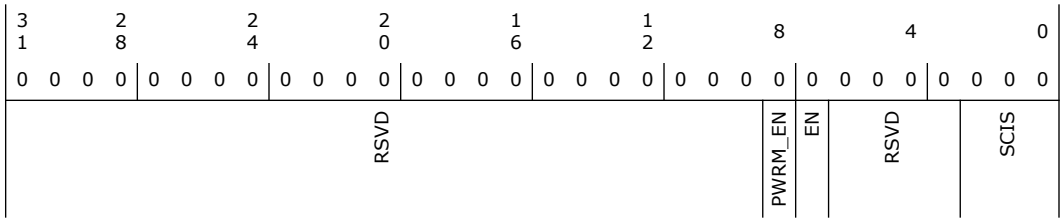
5.1.8 ACPI Control (ACTL)—Offset 44h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h RW	**PWRM Enable (PWRM_EN):** When set, decode of the memory range pointed by PWRMBASE is enabled. This bit is reset by PLTRST# assertion.
7	0h RW	**ACPI Enable (EN):** When set, decode of the I/O range pointed to by the ACPI base register is enabled and the ACPI power management function is enabled. This bit is reset by PLTRST# assertion.
6:3	0h RO	Reserved.
2:0	0h RW	**SCI IRQ Select (SCIS):** Specifies on which IRQ the SCI will internally appear. If not using the APIC, the SCI must be routed to IRQ[9-11], and that interrupt is not sharable with the SERIRQ stream, but is shareable with other PCI interrupts. If using the APIC, the SCI can also be mapped to IRQ20-23, and can be shared with other interrupts. Bits - SCI Map ---- - ------- 000 - IRQ9 001 - IRQ10 010 - IRQ11 011 - Reserved 100 - IRQ20 (only if APIC is enabled) 101 - IRQ21 (only if APIC is enabled) 110 - IRQ22 (only if APIC is enabled) 111 - IRQ23 (only if APIC is enabled) When the interrupt is mapped to APIC interrupts 9, 10 or 11, the APIC should be programmed for active-high reception. When the interrupt is mapped to APIC interrupts 20 through 23, the APIC should be programmed for active-low reception. This field is reset by PLTRST# assertion.

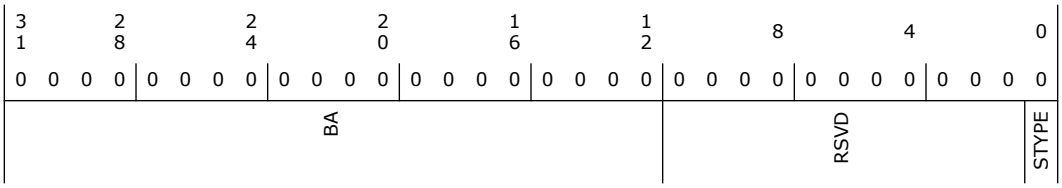
5.1.9 PM Base Address (PWRMBASE)—Offset 48h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW	**Base Address (BA):** Provides the 4K bytes of memory space for Power Management registers. This field is reset by PLTRST# assertion.
11:1	0h RO	Reserved.
0	0h RO	**Space Type (STYPE):** Always 0 to indicate memory space.

5.1.10 General PM Configuration A (GEN_PMCON_A)—Offset A0h

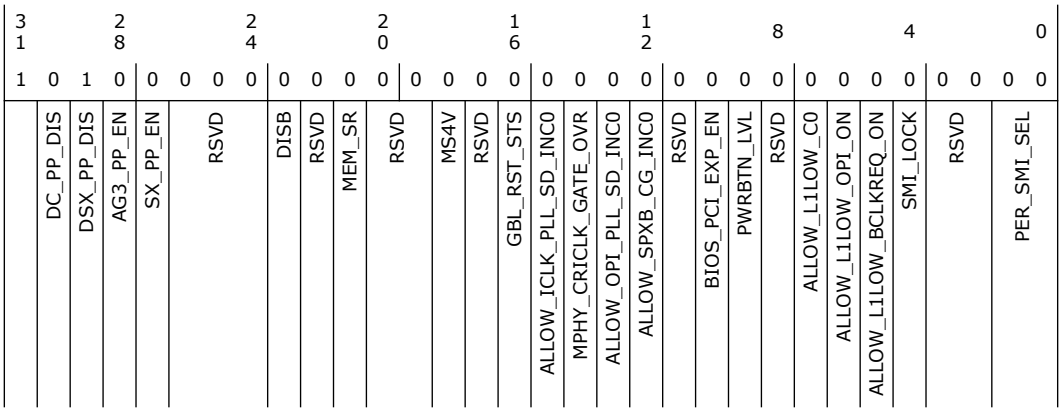
Usage ACPI, Legacy. Available Desktop, Mobile.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 2

Default: A0000000h



Bit Range	Default & Access	Field Name (ID): Description
31	1h RW	**:** Reserved
30	0h RW	**DC PHY Power Disable (DC_PP_DIS):** This bit determines the Host software contribution to whether the LAN PHY remains powered in Sx/MOFF or Deep Sx while on battery. This bit is reset by RTCRST# assertion.
29	1h RW	**Deep Sx PHY Power Disable (DSX_PP_DIS):** This bit determines the Host software contribution to whether the LAN PHY remains powered in Deep Sx. If this bit is cleared, for the PHY to be powered in Deep Sx state, SX_PP_EN must be set to '1'. This bit is reset by RTCRST# assertion.
28	0h RW	**After G3 PHY Power Enable (AG3_PP_EN):** This bit determines the Host software contribution to whether the LAN PHY is powered up after exiting G3 (to either Sx/MOFF or Deep Sx). This bit is reset by RTCRST# assertion.
27	0h RW	**Sx PHY Power Enable (SX_PP_EN):** This bit determines the Host software contribution to whether the LAN PHY remains powered in an Sx/MOFF state that was entered from S0 (rather than from G3). This bit is reset by DSW_PWROK de-assertion.
26:24	0h RO	Reserved.
23	0h RW	**DRAM Initialization Scratchpad Bit (DISB):** This bit does not effect hardware functionality in any way. It is provided as a scratchpad bit that is maintained through main power well resets and CF9h-initiated resets. BIOS is expected to set this bit prior to starting the DRAM initialization sequence and to clear this bit after completing the DRAM initialization sequence. BIOS can detect that a DRAM initialization sequence was interrupted by a reset by reading this bit during the boot sequence. If the bit is 1, then the DRAM initialization was interrupted. This bit is reset by RSMRST# assertion.
22	0h RO	Reserved.
21	0h RO/V	**Memory Placed in Self-Refresh (MEM_SR):** This bit will be set to '1' if DRAM should have remained powered and held in Self-Refresh through the last power state transition (i.e. the last time the system left S0). The scenarios where this should be the case are: - successful S3 entry / exit - successful Host partition reset without power cycle These scenarios both involve a handshake between the PCH and the Processor. The acknowledge from the Processor back to the PCH is assumed to imply that memory was successfully placed into Self-Refresh (the PCH has no way to verify whether that actually occurred). This bit will be cleared whenever the PCH begins a transition out of S0.
20:19	0h RO	Reserved.
18	0h RW/1C/V	**Minimum SLP_S4# Assertion Width Violation Status (MS4V):** Hardware sets this bit when the SLP_S4# assertion width is less than the time programmed in the SLP_S4# Minimum Assertion Width field (D31.F0.A4h.5:4). The PCH begins the timer when SLP_S4# pin (including ME override logic) is asserted during S4/S5 entry, or when the RSMRST# input is deasserted during Primary well power-up. Notes: 1) The status bit is cleared by software writing a 1 to the bit. 2)This bit is functional regardless of the value in the "SLP_S4# Assertion Stretch Enable" and the "Disable SLP_X Stretching After SUS Power Failure" bits. 3)This bit is reset by the assertion of the RSMRST# pin, but can be set in some cases before the default value is readable.
17	0h RO	Reserved.
16	0h RW/1C/V	**Global Reset Status (GBL_RST_STS):** This bit is set after a global reset (not G3 or Deep Sx) occurs. See the GEN_PMCON_B.HOST_RST_STS bit for potential usage models. The status bit is cleared by software writing a 1 to the bit.
15	0h RW	**Allow iCLK PLL Shutdown in C0 (ALLOW_ICLK_PLL_SD_INC0):** 0 = PMC allows iCLK PLL Shutdown only when the CPU is in a non-C0 (Cx) state. (Default) 1 = iCLK PLL can be shut down when the CPU is in C0 or Cx state assuming all other gating conditions are satisfied. This bit is reset by PLTRST# assertion.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW	**Dynamic mPHY CRI Clock Gate Override (MPHY_CRICLK_GATE_OVR):** 0 = Enable CRI clock gating in the modPHY. (Default) 1 = Disable CRI clock gating in the modPHY This bit is reset by PLTRST# assertion.
13	0h RW	**Allow OPI PLL Shutdown in C0 (ALLOW_OPI_PLL_SD_INC0):** 0 = PMC allows OPI PLL Shutdown only when the CPU is in a non-C0 (Cx)state. (Default) 1 = OPI PLL can be shut down when the CPU is in C0 or Cx state assuming all other gating conditions are satisfied. Note: The signal driven by this configuration bit is connected to both OPI and USB3/PXP PLLs to support PLL shutdown when backbone clock is sourced from the USB3/PXP PLL (a backup mode). This bit is reset by PLTRST# assertion.
12	0h RW	**Allow SPXB Clock Gating in C0 (ALLOW_SPXB_CG_INC0):** 0 = PMC allows SBXB backbone clock gating only when the CPU is in a non-C0 state (Cx). (Default) 1 = SPXB backbone clock can be gated when the CPU is in C0 or Cx state assuming all other gating conditions are satisfied. This bit is reset by PLTRST# assertion.
11	0h RO	Reserved.
10	0h RW	**BIOS PCI Express Enable (BIOS_PCI_EXP_EN):** This bit acts as a global enable for the SCI associated with the PCI express ports. 0 = The various PCI Express* ports and processor CANNOT cause PCI_EXP_STS bit to go active. (Default) 1 = The various PCI Express* ports and processor CAN cause PCI_EXP_STS bit to go active. This bit is reset by PLTRST# assertion.
9	0h RO/V	**Power Button Level (PWRBTN_LVL):** This read-only bit indicates the current state of the PWRBTN# signal. 1= High, 0 = Low. The value reflected in this bit is dependent upon PM_CFG1.PB_DB_MODE. The PB_DB_MODE bit's value causes the following behavior: - '0': PWRBTN_LVL is taken from the debounced PWRBTN# pin value that is seen at the output of a 16ms debouncer. - '1': PWRBTN_LVL is taken from the raw PWRBTN# pin (before the debouncer).
8	0h RO	Reserved.
7	0h RW	**Allow L1.LOW Entry During C0 (ALLOW_L1LOW_C0):** 0 = PMC only allows L1.LOW entry if the CPU is in a non-C0 state (Cx). (Default) 1 = PMC allows L1.LOW entry in C0 or Cx state. This bit is reset by PLTRST# assertion.
6	0h RW	**Allow L1.LOW Entry with OPI Voltage On (ALLOW_L1LOW_OPI_ON):** 0 = PMC only allows L1.LOW entry if the OPI voltage is off. (Default) 1 = PMC allows L1.LOW entry regardless of whether the OPI voltage is on/off. This bit is reset by PLTRST# assertion.
5	0h RW	**Allow L1.LOW Entry with CPU BCLK REQ Asserted (ALLOW_L1LOW_BCLKREQ_ON):** 0 = PMC only allows L1.LOW entry if the CPU's BCLK request is de-asserted.(Default) 1 = PMC allows L1.LOW entry regardless of whether the CPU's BCLK request is asserted/de-asserted. This bit is reset by PLTRST# assertion.
4	0h RW/L	**SMI Lock (SMI_LOCK):** When this bit is set, writes to the GLB_SMI_EN bit will have no effect. Once the SMI_LOCK bit is set, writes of '0' to SMI_LOCK bit will have no effect (i.e. once set, this bit can only be cleared by PLTRST# assertion).
3:2	0h RO	Reserved.
1:0	0h RW	**Period SMI Select (PER_SMI_SEL):** Software sets these bits to control the rate at which the periodic SMI# is generated: 00 = 64 seconds (Default), 01 = 32 seconds, 10 = 16 seconds, 11 = 8 seconds Tolerance for the timer is +/- 1 second. This field is reset by PLTRST# assertion.

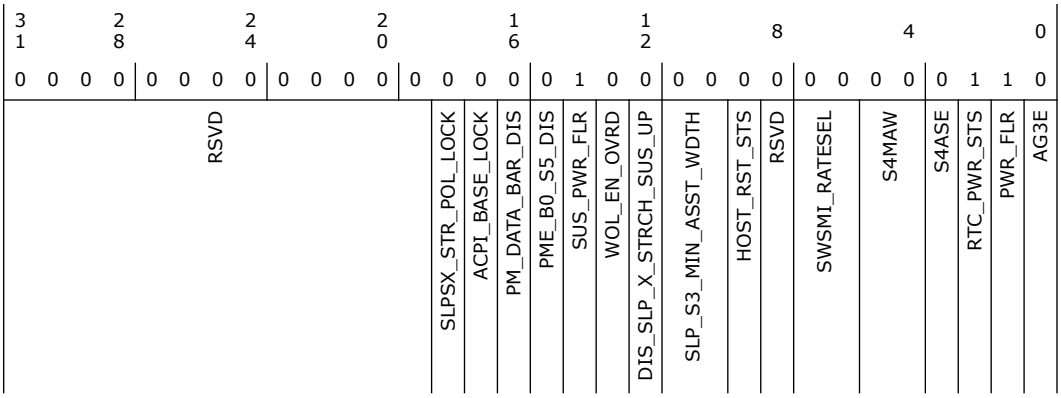
5.1.11 General PM Configuration B (GEN_PMCON_B)—Offset A4h

Access Method

Type: CFG Register
(Size: 32 bits)

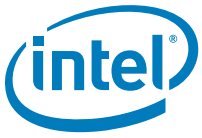
Device: 31
Function: 2

Default: 4006h



Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	Reserved.
18	0h RW/L	**SLP_Sx# Stretching Policy Lock-Down (SLPSX_STR_POL_LOCK):** When set to 1, this bit locks down the following fields: (Those bits become read-only.) - GEN_PMCON_3.DIS_SLP_X_STRCH_SUSPF - GEN_PMCON_3.SLP_S3_MIN_ASST_WDTH - GEN_PMCON_3.S4MAW - GEN_PMCON_3.S4ASE - PM_CFG.SLP_A_MIN_ASST_WDTH - PM_CFG.SLP_LAN_MIN_ASST_WDTH - PM_CFG.PWR_CYC_DUR Writes of '0' to this bit are always ignored. This bit becomes locked when a value of '1' is written to it. Once locked, the only way to clear this bit is to perform a platform reset (PLTRST# assertion).
17	0h RW/L	**ACPI Base Lock (ACPI_BASE_LOCK):** When set to 1, this bit locks down the ACPI Base Address Register (ABASE) at offset 40h. The Base Address Field becomes read-only. Writes of '0' to this bit are always ignored. This bit becomes locked when a value of '1' is written to it. Once locked, the only way to clear this bit is to perform a platform reset (PLTRST# assertion).
16	0h RW/L	**Power Management Data BAR Disable (PM_DATA_BAR_DIS):** When set to 1, this bit disables all accesses to the MMIO range pointed to by PM_DATA_BAR. This does not affect the BAR value itself, which can still be changed after this bit is set. But once the bit is set to '1', the PMC will drop writes to the data region pointed to by PM_DATA_BAR. And reads will return 0. Writes of '0' to this bit are always ignored. This bit becomes locked when a value of '1' is written to it. Once locked, the only way to clear this bit is to perform a platform reset (PLTRST# assertion).

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**PME B0 S5 Disable (PME_B0_S5_DIS):** When set to '1', this bit blocks wake events from PME_B0_STS in S5, regardless of the state of PME_B0_EN. When cleared (default), wake events from PME_B0_STS are allowed in S5 if PME_B0_EN = '1'. Wakes from power states other than S5 are not affected by this policy bit. The net effect of setting PME_B0_S5_DIS = '1' is described by the truth table below: Y = Wake; N = Don't wake; B0 = PME_B0_EN; OV = WOL Enable Override B0/OV | S3/S4 | S5 00 | N | N 01 | N | Y (LAN only) 11 | Y (all PME B0 sources) | Y (LAN only) 10 | Y (all PME B0 sources) | N This bit is cleared by the RTCRST# assertion.
14	1h RW/1C	**SUS Well Power Failure (SUS_PWR_FLR):** This bit is set to '1' whenever Primary well power is lost, as indicated by RSMRST# assertion. Software writes a 1 to this bit to clear it. This bit is in the Primary well, and defaults to '1' based on RSMRST# assertion (not cleared by any type of reset).
13	0h RW	**WOL Enable Override (WOL_EN_OVRD):** 0 = WoL polices are determined by OS-visible bits. 1 = WoL is enabled enabled to wake the system from S5 regardless of the value in the PME_B0_EN bit in the GPE0_EN register. This allows the system BIOS to enable WoL regardless of the policies selected through the OS. This bit is maintained in the RTC power well, therefore permitting WOL following a surprise power failure even in cases in which the system may have been running in S0 without the PME Enables set. (Note that the LAN NVRAM configuration must support WOL after SUS power loss.) This bit has no effect on wakes from S1, S3, or S4. This bit is cleared by the RTCRST# assertion.
12	0h RW/L	**Disable SLP_X Stretching After SUS Well Power Up (DIS_SLP_X_STRCH_SUS_UP):** 0 = SLP_* stretching will be performed after SUS power failure as enabled in various other fields. SLP_* stretch timers start on SUS well power up (the PCH has no ability to count stretch time while the SUS well is powered down). 1 = All SLP_* pin stretching is disabled when powering up after a SUS well power loss. Note: This policy bit has a different effect on SLP_SUS# stretching than on the other SLP_* pins, since SLP_SUS# is the control signal for one of the scenarios where SUS well power is lost (Deep Sx). The effect of setting this bit to '1' on: - SLP_S3#, SLP_S4#, SLP_A# and SLP_LAN# stretching: disabled after any SUS power loss - SLP_SUS# stretching: disabled after G3, but no impact on Deep Sx This field is not writable when the SLP_Sx# Stretching Policy Lock-Down bit is set. This bit is cleared by the RTCRST# assertion.
11:10	0h RW/L	**SLP_S3# Minimum Assertion Width (SLP_S3_MIN_ASST_WDTH):** This 2-bit value indicates the minimum assertion width of the SLP_S3# signal to guarantee that the Main power supplies have been fully power-cycled. This value may be modified per platform depending on power supply capacitance, board capacitance, power failure detection circuits, etc. Settings are: 00: 60 usec 01: 1 ms 10: 50 ms 11: 2 sec This field is not writable when the SLP_Sx# Stretching Policy Lock- Down bit is set. This bit is cleared by the RSMRST# pin.
9	0h RW/1C/V	**Host Reset Status (HOST_RST_STS):** This bit is set by hardware when a host partition reset (not a global reset, Deep Sx, or G3) occurs. This bit is an optional tool to help BIOS determine when a host partition reset might have collided with a wake from a valid sleep state. A possible usage model would be to consult and then write a '1' to clear this bit during the boot flow before determining what action to take based on reading PM1_STS.WAK_STS = '1'. If HOST_RST_STS = '1' and/or GEN_PMCON_A.GBL_RST_STS = '1', the cold reset boot path could be followed rather than the resume path, regardless of the setting of WAK_STS. This bit does not affect PCH operation in any way, and can therefore be left set if BIOS chooses not to use it.
8	0h RO	Reserved.
7:6	0h RW	**SWSMI Rate Select (SWSMI_RATESEL):** This 2-bit value indicates when the SWSMI timer will time out. Valid values are: 00 [=] 1.5ms +/- 0.6ms 01 [=] 16ms +/- 4ms 10 [=] 32ms +/- 4ms 11 [=] 64ms +/- 4ms These bits are not cleared by any type of reset except RTCRST# assertion.



Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW/L	**SLP_S4# Minimum Assertion Width (S4MAW):** This 2-bit value indicates the minimum assertion width of the SLP_S4# signal to guarantee that the DRAMs have been safely power-cycled. This value may be modified per platform depending on DRAM types, power supply capacitance, etc. Valid values are: 11: 1 second 10: 2 seconds 01: 3 seconds 00: 4 seconds This value is used in two ways: 1. If the SLP_S4# assertion width is ever shorter than this time, a status bit (D31.F0.A2h.2) is set for BIOS to read when S0 is entered 2. If enabled by bit 3 in this register, the hardware will prevent the SLP_S4# signal from deasserting within this minimum time period after asserting. Note that the logic that measures this time is in the Primary well. Therefore, when leaving a G3 or Deep Sx state, the minimum time is measured from the deassertion of the internal Primary well reset (unless the "Disable_SLP_X Stretching After SUS Power Failure" bit is set). This field is not writable when the SLP_Sx# Stretching Policy Lock-Down bit is set. RTCRST# forces this field to the conservative default state (00b).
3	0h RW/L	**SLP_S4# Assertion Stretch Enable (S4ASE):** 0 = The minimum assertion time for SLP_S4# is the same as the timing defined in the Skylake Platform Design Guide, Power Sequencing Specification Chapter. 1 = The SLP_S4# pin (which includes the ME override logic) will minimally assert for the time specified in bits 5:4 of this register. This bit is not writable when the SLP_Sx# Stretching Policy Lock-Down bit is set. This bit is cleared by RTCRST# assertion.
2	1h RW	**RTC Power Status (RTC_PWR_STS):** Intel PCH will set this bit to '1' when RTCRST# indicates a weak or missing battery. The bit will remain set until the software clears it by writing a '0' back to this bit position. This bit is not cleared by any type of reset.
1	1h RW/1C	**Power Failure (PWR_FLR):** This bit is in the DSW well and defaults to '1' based on DSW_PWROK assertion (not cleared by any type of reset). 0 = Indicates that the trickle current has not failed since the last time the bit was cleared. 1 = Indicates that the trickle current (from the main battery or trickle supply) was removed or failed. Software writes a '1' to this bit to clear it.
0	0h RW	**AFTERG3_EN (AG3E):** Determines what state to go to when power is reapplied after a power failure (G3 state). 0 = System will return to an S0 state (boot) after power is re-applied. 1 = System will return to the S5 state (except if it was in S4, in which case it will return to S4-like state). In the S5 state, the only enabled wake-up event is the Power Button or any enabled wake event that was preserved through the power failure. This bit is in the RTC well and is only cleared by RTCRST# assertion.

5.1.12 BM_BREAK_EN and Cx State Configuration Register (BM_CX_CNF)—Offset A8h

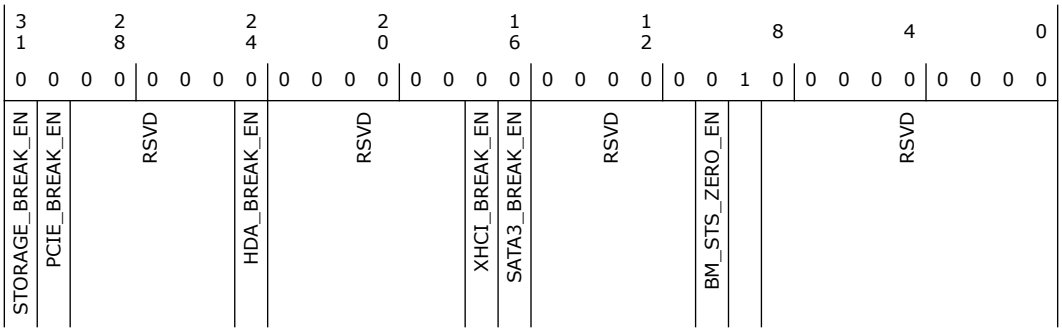
Usage ACPI, Legacy. Power well Primary. Available: Desktop and Mobile. This register is used to enable BM break events and C-state related modes. Note that these C-state settings have no effect if the C-states are not entered

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 2

Default: 200h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Storage Break Enable (STORAGE_BREAK_EN):** When this bit is a 1, Serial ATA traffic will cause BM_STS to be set, even if the BM_STS_ZERO_EN bit is set. This bit is reset by PLTRST# assertion.
30	0h RW	**PCI Express Break Enable (PCIE_BREAK_EN):** When this bit is a 1, PCI Express traffic will cause BM_STS to be set, even if the BM_STS_ZERO_EN bit is set. This bit is reset by PLTRST# assertion.
29:25	0h RO	Reserved.
24	0h RW	**HD Audio Break Enable (HDA_BREAK_EN):** When this bit is a 1, HD Audio traffic will cause BM_STS to be set, even if the BM_STS_ZERO_EN bit is set. This bit is reset by PLTRST# assertion.
23:18	0h RO	Reserved.
17	0h RW	**XHCI Break Enable (XHCI_BREAK_EN):** When this bit is a 1, XHCI traffic will cause BM_STS to be set, even if the BM_STS_ZERO_EN bit is set. This bit is reset by PLTRST# assertion.
16	0h RW	**SATA3 Break Enable (SATA3_BREAK_EN):** When this bit is a 1, SATA3 traffic will cause BM_STS to be set, even if the BM_STS_ZERO_EN bit is set. This bit is reset by PLTRST# assertion.
15:11	0h RO	Reserved.
10	0h RW	**Bus Master Status Zero Enable (BM_STS_ZERO_EN):** When this bit is a 1, PCH will not set the BM_STS if there is bus master activity from PCI, PCI Express and internal bus masters. Note: If the BM_STS bit is already set when the BM_STS_ZERO_EN bit is set, the BM_STS bit will remain set. Software will still need to clear the BM_STS bit. Note: BM_STS_ZERO_EN does not apply to PHOLD (LPC DMA or LPC bus master activity). A separate policy bit (PHOLD_BM_STS_BLOCK) determines whether PHOLD will set BM_STS. This bit is reset by PLTRST# assertion.
9	1h RW	**:** Reserved
8:0	0h RO	Reserved.

5.1.13 Extended Test Mode Register 3 (ETR3)—Offset ACh

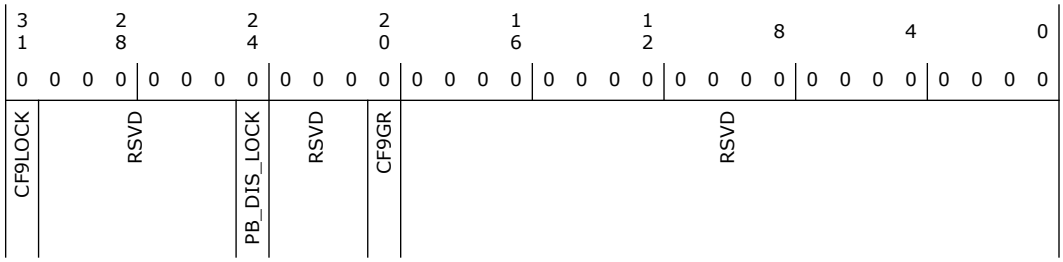
This register resides in the primary well. All bits except bit[23:16] are reset by host_deep_rst_b. Bit[23:16] are reset by pri_pwrgood_rst_b only.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/V/L	**CF9h Lockdown (CF9LOCK):** 0 = CF9h Global Reset bit R/W. 1 = CF9h Global Reset bit RO. When set, this bit becomes RO and is reset by a CF9h reset or RSMRST# assertion (other reset types are not applicable). In manufacturing/debug environments this bit should be left as default '0'. In all other environments, BIOS must program this bit to '1'.
30:25	0h RO	Reserved.
24	0h RW/L	**Power Button Disable Lock (PB_DIS_LOCK):** Once set, this bit cannot be changed until the next global reset. When this bit is set to 1, the PM_CFG*.PB_DIS bit can no longer be changed.
23:21	0h RO	Reserved.
20	0h RW/L	**CF9h Global Reset (CF9GR):** 0 = A CF9h write of 6h or Eh will only reset the Host partition. 1 = A CF9h write of 6h or Eh will cause a Global Reset of both the Host and the ME partitions. It is recommended that BIOS should set this bit early on in the boot sequence, and then clear it and set the CF9LOCK bit prior to loading the OS in both an ME Enabled and a ME Disabled system. This register is locked by the CF9 Lockdown (CF9LOCK) bit. This register is not reset by a CF9h reset. It is reset by RSMRST# assertion.
19:0	0h RO	Reserved.

5.2 PMC I/O Based Registers Summary

The below table shows registers associated with ACPI and Legacy power management support. These register locations are all offsets from ACPI base address defined in PCI Device 31: Function 2 (ABASE), and can be moved to any 256-byte aligned I/O location. In order to access these registers, the ACPI Enable bit in ACPI Control Register (B0:D31:F2 offset 44h) must be set. The registers are defined to support the ACPI 4.0a specification and generally use the same bit names.
Note: All reserved bits and registers will always return 0 when read and will have no effect when written.

Table 5-2. Summary of PMC I/O Based Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	Power Management 1 Enables and Status (PM1_EN_STS)—Offset 0h	0h
4h	7h	Power Management 1 Control (PM1_CNT)—Offset 4h	0h
8h	Bh	Power Management 1 Timer (PM1_TMR)—Offset 8h	0h
30h	33h	SMI Control and Enable (SMI_EN)—Offset 30h	2h
34h	37h	SMI Status Register (SMI_STS)—Offset 34h	0h
40h	43h	General Purpose Event Control (GPE_CTRL)—Offset 40h	0h
44h	47h	Device Activity Status Register (DEVACT_STS)—Offset 44h	0h
50h	53h	PM2a Control Block (PM2A_CNT_BLK)—Offset 50h	0h
54h	57h	Over-Clocking WDT Control (OC_WDT_CTL)—Offset 54h	2000h
80h	83h	General Purpose Event 0 Status [31:0] (GPE0_STS_31_0)—Offset 80h	0h
84h	87h	General Purpose Event 0 Status [63:32] (GPE0_STS_63_32)—Offset 84h	0h
88h	8Bh	General Purpose Event 0 Status [95:64] (GPE0_STS_95_64)—Offset 88h	0h
8Ch	8Fh	General Purpose Event 0 Status [127:96] (GPE0_STS[127:96])—Offset 8Ch	0h
90h	93h	General Purpose Event 0 Enable [31:0] (GPE0_EN_31_0)—Offset 90h	0h
94h	97h	General Purpose Event 0 Enable [63:32] (GPE0_EN_63_32)—Offset 94h	0h
98h	9Bh	General Purpose Event 0 Enable [95:64] (GPE0_EN_95_64)—Offset 98h	0h
9Ch	9Fh	General Purpose Event 0 Enable [127:96] (GPE0_EN[127:96])—Offset 9Ch	0h

5.2.1 Power Management 1 Enables and Status (PM1_EN_STS)—Offset 0h

Access Method

Type: IO Register
(Size: 32 bits)

Device: 31
Function: 2

Default: 0h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD	PCIEXP_WAKE_DIS	RSVD					RTC_EN	RSVD	PWRBTN_EN	RSVD	GBL_EN	RSVD			TMROF_EN	WAK_STS	PCIEXP_WAKE_STS	RSVD		PWRBTNOR_STS	RTC_STS	RSVD	PWRBTN_STS	RSVD		GBL_STS	BM_STS	RSVD			TMROF_STS

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	Reserved.
30	0h RW	**PCI Express Wake Disable (PCIEXP_WAKE_DIS):** This bit disables the inputs to the PCIEXP_WAKE_STS bit in the PM1 Status register from waking the system. Modification of this bit has no impact on the value of the PCIEXP_WAKE_STS bit. This bit is reset by DSW_PWROK de-assertion.
29:27	0h RO	Reserved.
26	0h RW/V	**RTC Alarm Enable (RTC_EN):** This is the RTC alarm enable bit. It works in conjunction with the SCI_EN bit: RTC_EN SCI_EN Effect when RTC_STS is set 0 X No SMI# or SCI. If system was in S3-S5, no wake even occurs. 1 0 SMI#. If system was in S3-S5, then a wake event occurs before the SMI#. 1 1 SCI. If system was in S3-S5, then a wake event occurs before the SCI. Note: This bit is in the RTC well and is reset by RTCRST# assertion, to allow an RTC event to wake after a power failure.
25	0h RO	Reserved.
24	0h RW/V	**Power Button Enable (PWRBTN_EN):** This bit is the power button enable. It works in conjunction with the SCI_EN bit: PWRBTN_EN SCI_EN Effect when PWRBTN_STS is set 0 X No SMI# or SCI. 1 0 SMI#. 1 1 SCI. NOTE: PWRBTN_EN has no effect on the PWRBTN_STS bit being set by the assertion of the power button. The Power Button is always enabled as a Wake event.
23:22	0h RO	Reserved.
21	0h RW	**Global Enable (GBL_EN):** Global enable bit. When both the GBL_EN and the GBL_STS are set, PCH generates an SCI. This bit is reset by PLTRST# assertion.
20:17	0h RO	Reserved.
16	0h RW	**Timer Overflow Interrupt Enable (TMROF_EN):** This is the timer overflow interrupt enable bit. It works in conjunction with the SCI_EN bit: TMROF_EN SCI_EN Effect when TMROF_STS is set 0 X No SMI# or SCI. 1 0 SMI#. 1 1 SCI. This bit is reset by PLTRST# assertion.
15	0h RW/1C/V	**Wake Status (WAK_STS):** This bit is set when the system is in one of the Sleep states (via the SLP_EN bit) and an enabled Intel PCH Wake event occurs. Upon setting this bit, the Intel PCH will transition the system to the ON state. This bit can only be set by hardware and can only be cleared by writing a one to this bit position. This bit is not affected by hard resets caused by a CF9 write, but is reset by RSMRST#. If a power failure occurs (such as removed batteries) without the SLP_EN bit set, the WAK_STS bit will not be set when the power returns if the AFTER_G3 bit is 0. If the AFTER_G3 bit is 1, then the WAK_STS bit will be set after waking from a power failure. If necessary, the BIOS can clear the WAK_STS bit in this case.
14	0h RW/1C/V	**PCI Express Wake Status (PCIEXP_WAKE_STS):** This bit is set by hardware to indicate that the system woke due to a PCI Express wakeup event. This event can be caused by the PCI Express WAKE# pin being active, or one or more of the PCI Express ports being in beacon state, or recept of a PCI Express PME message at root port. This bit should only be set when one of these events causes the system to transition from a non-S0 system power state to the S0 system power state. This bit is set independant of the PCIEXP_WAKE_DIS bit. Software writes a 1 to clear this bit. If WAKE# pin is still active during the write or one or more PCI Express ports is in the beacon state or PME message received indication is not cleared in the root port, then the bit will remain active (i.e. all inputs to this bit are level sensitive) Note: This bit does not itself cause a wake event or prevent entry to a sleeping state. Thus if the bit is 1 and the system is put into a sleeping state, the system will not automatically wake.
13:12	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW/1C/V	**Power Button Override (PWRBTNOR_STS):** This bit is set any time a Power Button Override Event occurs (i.e. the power button is pressed for at least 4 consecutive seconds), the corresponding bit is received in the SMBus slave message, the ME-Initiated Power Button Override bit is set, the ME-Initiated Host Reset with Power Down is set, or due to an internal thermal sensor catastrophic condition. These events cause an unconditional transition to the S5 state. The BIOS or SCI handler clears this bit by writing a 1 to it. This bit is not affected by hard resets via CF9h writes, and is not reset by RSMRST#. Thus, this bit is on RTC well and is preserved through power failures (reset by RTCRST#). Note that this bit is still asserted when the global SCI_EN is set to '1' then an SCI will be generated.
10	0h RW/1C/V	**RTC Status (RTC_STS):** This bit is set when the RTC generates an alarm (assertion of the IRQ8# signal), and is not affected by any other enable bit. See RTC_EN for the effect when RTC_STS goes active. This bit is only set by hardware and can only be reset by writing a one to this bit position. This bit is not affected by hard resets caused by a CF9 write, but is reset by DSW_PWROK de-assertion.
9	0h RO	Reserved.
8	0h RW/1C/V	**Power Button Status (PWRBTN_STS):** This bit is set when the PWRBTN# signal is asserted (low), independent of any other enable bit. See PWRBTN_EN for the effect when PWRBTN_STS goes active. PWRBTN_STS is always a wake event. This bit is only set by hardware and can be cleared by software writing a one to this bit position. This bit is not affected by hard resets caused by a CF9 write, but is reset by DSW_PWROK de-assertion. If the PWRBTN# signal is held low for more than 4 seconds, the Intel PCH clears the PWRBTN_STS bit, sets the PWRBTNOR_STS bit, the system transitions to the S5 state, and only PWRBTN# is enabled as a wake event. If PWRBTN_STS bit is cleared by software while the PWRBTN# pin is still held low, this will not cause the PWRBTN_STS bit to be set. The PWRBTN# signal must go inactive and active again to set the PWRBTN_STS bit. Note that the SMBus Unconditional Powerdown message, the CPU Thermal Trip and the Internal Thermal Sensors' Catastrophic Condition result in behavior matching the Powerbutton Override, which includes clearing this bit.
7:6	0h RO	Reserved.
5	0h RW/1C/V	**GBL Status (GBL_STS):** This bit is set when an SCI is generated due to the BIOS wanting the attention of the SCI handler. BIOS has a corresponding bit, BIOS_RLS, which will cause an SCI and set this bit. The SCI handler should then clear this bit by writing a 1 to it. This bit will not cause wake events or SMI#. This bit is not effected by SCI_EN. Note: GBL_STS being set will cause an SCI, even if the SCI_EN bit is not set. Software must take great care not to set the BIOS_RLS bit (which causes GBL_STS to be set) if the SCI handler is not in place. This bit is reset by PLTRST# assertion.
4	0h RW/1C/V	**Bus Master Status (BM_STS):** This bit is set to 1 by the Intel PCH when a PCH-visible bus master requests access to memory or the BM_BUSY# signal is active. This bit is cleared by the Processor writing a 1 to this bit position. This bit will not cause a wake event, SCI, or SMI. This bit is reset by PLTRST# assertion.
3:1	0h RO	Reserved.
0	0h RW/1C/V	**Timer Overflow Status (TMROF_STS):** This is the timer overflow status bit. This bit gets set anytime bit 22 of the 24 bit timer goes low (bits are counted from 0 to 23). This will occur every 2.3435 seconds. See TMROF_EN for the effect when TMROF_STS goes active. Software clears this bit by writing a 1 to it. This bit is reset by PLTRST# assertion.

5.2.2 Power Management 1 Control (PM1_CNT)—Offset 4h

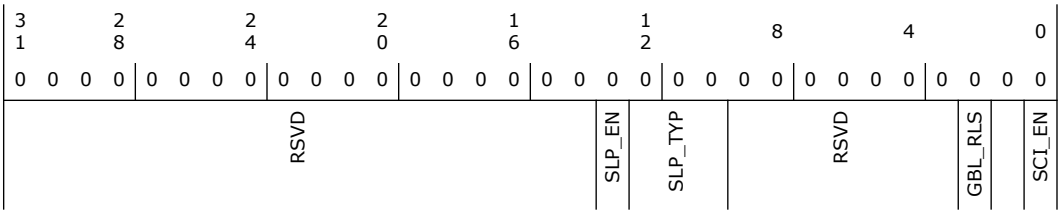
Lockable: No Usage: ACPI or Legacy Power Well: Bits 0-9, 13-31: Primary, Bits 10-12: RTC Available: Desktop, Mobile

Access Method

Type: IO Register
(Size: 32 bits)

Device: 31
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13	0h WO	**Sleep Enable (SLP_EN):** This is a write-only bit and reads to it always return a zero. Setting this bit causes the system to sequence into the Sleep state defined by the SLP_TYP field. This bit is reset by PLTRST# assertion.
12:10	0h RW	**Sleep Type (SLP_TYP):** This 3-bit field defines the type of Sleep the system should enter when the SLP_EN bit is set to 1. Bits Mode Typical Mapping 000 ON S0 001 Reserved 010 Reserved 011 Reserved 100 Reserved 101 Suspend-To-RAM S3 110 Suspend-To-Disk S4 111 Soft Off S5 These bits are reset by RTCRST# only.
9:3	0h RO	Reserved.
2	0h WO	**Global Release (GBL_RLS):** This bit always reads as 0. ACPI software writes a '1' to this bit to raise an event to the BIOS. BIOS sfotware has corresponding enable and status bits to control its ability to receive ACPI events.
1	0h RW	**Scratchpad**
0	0h RW	**SCI Enable (SCI_EN):** Selects the SCI interrupt or the SMI# for various events. 0 = These events will generate an SMI#. 1 = These events will generate an SCI. This bit is reset by PLTRST# assertion.

5.2.3 Power Management 1 Timer (PM1_TMR)—Offset 8h

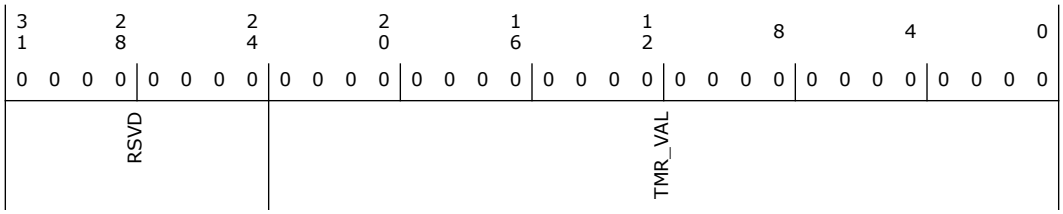
Lockable: No Usage: ACPI Power Well: Primary Available: Desktop, Mobile

Access Method

Type: IO Register
(Size: 32 bits)

Device: 31
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:0	0h RO/V	**Timer Value (TMR_VAL):** This read-only field returns the running count of the PM timer. This counter runs off a 3.579545 MHz clock (derived from 14.31818 MHz divided by 4). It is reset (to 0) during a PCI reset, and then continues counting as long as the system is in the S0 state. Anytime bit 22 of the timer goes HIGH to LOW (bits referenced from 0 to 23), the TMROF_STS bit is set. The High-to-Low transition will occur every 2.3435 seconds. Writes to this register have no effect.

5.2.4 SMI Control and Enable (SMI_EN)—Offset 30h

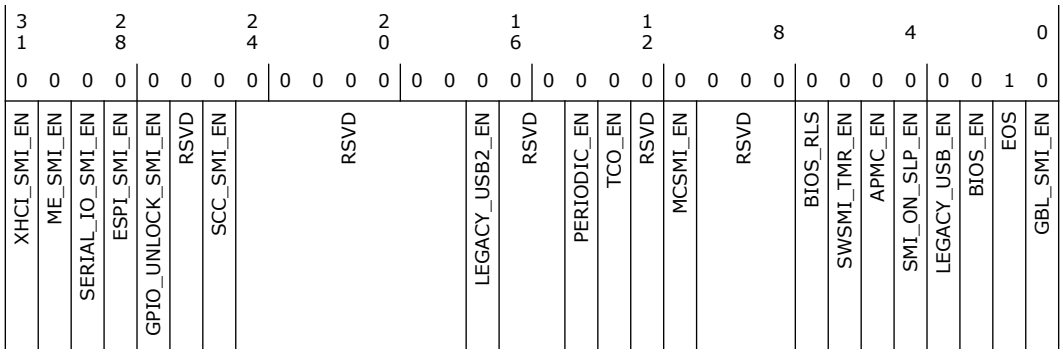
Lockable: No
Usage: ACPI or Legacy
Power Well: Primary Available: Desktop, Mobile
Note: This register is symmetrical to the SMI Status Register.

Access Method

Type: IO Register
(Size: 32 bits)

Device: 31
Function: 2

Default: 2h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**XHCI SMI Enable (XHCI_SMI_EN):** Software sets this bit to enable XHCI SMI events. This bit is reset by PLTRST# assertion.
30	0h RW	**ME SMI Enable (ME_SMI_EN):** Software sets this bit to enable ME SMI# events. This bit is reset by PLTRST# assertion.
29	0h RW	**Intel Serial I/O SMI Enable (SERIAL_IO_SMI_EN):** Software sets this bit to enable Intel Serial I/O SMI events. This bit is reset by PLTRST# assertion.
28	0h RW/L	**eSPI SMI Enable (ESPI_SMI_EN):** Software sets this bit to enable eSPI SMI events. This bit is reset by PLTRST# assertion.
27	0h RW/1S	**GPIO Unlock SMI Enable (GPIO_UNLOCK_SMI_EN):** Setting this bit will cause the Intel PCH to generate an SMI# when the GPIO_UNLOCK_SMI_STS bit is set in the SMI_STS register. Once written to '1', this bit can only be cleared by PLTRST# assertion.
26	0h RO	Reserved.
25	0h RW	**SCC SMI Enable (SCC_SMI_EN):** Software sets this bit to enable SCC SMI events. This bit is reset by PLTRST# assertion.
24:18	0h RO	Reserved.
17	0h RW	**Legacy USB 2 SMI# Enable (LEGACY_USB2_EN):** Enables legacy USB2 logic to cause SMI#.
16:15	0h RO	Reserved.
14	0h RW	**Periodic Enable (PERIODIC_EN):** Setting this bit will cause the Intel PCH to generate an SMI# when the PERIODIC_STS bit is set in the SMI_STS register. This bit is reset by PLTRST# assertion.
13	0h RW/L	**TCO Enable (TCO_EN):** 1 = Enables the TCO logic to generate SMI#. 0 = Disables TCO logic from generating an SMI#. If the NMI2SMI_EN bit is set, then SMI's that are caused by NMI's (i.e. rerouted) will not be gated by the TCO_EN bit . Even if the TCO_EN bit is 0, the NMI's will still be routed to cause the SMI#. NOTE: This bit can not be written once the TCO_LOCK bit (at offset 08h of TCO I/O Space) is set. This prevents unauthorized software from disabling the generation of TCO-based SMI's. This bit is reset by PLTRST# assertion.
12	0h RO	Reserved.
11	0h RW	**Microcontroller SMI Enable (MCSMI_EN):** Software sets this bit to 1 to enables Intel PCH to trap access to the microcontroller range (62h or 66h). A 'trapped' cycles will be claimed by Intel PCH, but not forwarded to LPC. An SMI# will also be generated. This bit is reset by PLTRST# assertion.
10:8	0h RO	Reserved.
7	0h WO	**BIOS Release (BIOS_RLS):** Enables the generation of an SCI interrupt for ACPI software when a '1' is written to this bit position by BIOS software. This bit always reads a '0'. NOTE: GBL_STS being set will cause an SCI, even if the SCI_EN bit is not set. Software must take great care not to set the BIOS_RLS bit (which causes GBL_STS to be set) if the SCI handler is not in place. This bit is reset by PLTRST# assertion.
6	0h RW	**Software SMI Timer Enable (SWSMI_TMR_EN):** Software sets this bit to a '1' to start the Software SMI# Timer. When the timer expires (depending on the SWSMI_RATE_SEL bits), it will generate an SMI# and set the SWSMI_TMR_STS bit. The SWSMI_TMR_EN bit will remain at 1 until software sets it back to 0. Clearing the SWSMI_TMR_EN bit before the timer expires will reset the timer and the SMI# will not be generated. The default for this bit is 0. This bit is reset by PLTRST# assertion.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**APMC Enable (APMC_EN):** If set, this enables writes to the APM_CNT register to cause an SMI#. This bit is reset by PLTRST# assertion.
4	0h RW	**SMI On Sleep Enable (SMI_ON_SLP_EN):** If this bit is set, the Intel PCH will generate an SMI# when a write access attempts to set the SLP_EN bit (in the PM1_CNT register). Furthermore, the Intel PCH will not put the system to a sleep state. It is expected that the SMI# handler will turn off the SMI_ON_SLP_EN bit before actually setting the SLP_EN bit. This bit is reset by PLTRST# assertion.
3	0h RW	**Legacy USB Enable (LEGACY_USB_EN):** Enables legacy USB circuit to cause SMI#. This bit is reset by PLTRST# assertion.
2	0h RW	**BIOS Enable (BIOS_EN):** Enables the generation of SMI# when ACPI software writes a 1 to the GBL_RLS bit. Note that if the BIOS_STS bit, which gets set when software writes a 1 to GBL_RLS bit, is already a 1 at the time that BIOS_EN becomes 1, an SMI# will be generated when BIOS_EN gets set. This bit is reset by PLTRST# assertion.
1	1h RW/1S/V	**End of SMI (EOS):** This bit controls the arbitration of the SMI signal to the processor. This bit must be set in order for Intel PCH to assert SMI# low to the processor after SMI# has been asserted previously. Once Intel ICH asserts SMI# low, the EOS bit is automatically cleared. In the SMI handler, the CPU should clear all pending SMIs (by servicing them and then clearing their respective status bits), set the EOS bit, and exit SMM. This will allow the SMI arbiter to reassert SMI upon detection of an SMI event and the setting of a SMI status bit. The SMI# signal will go inactive for 4 PCI clocks. This bit is reset by PLTRST# assertion.
0	0h RW/L	**Global SMI Enable (GBL_SMI_EN):** 0 = No SMI# will be generated by PCH. 1 = Enables the generation of SMI# in the system upon any enabled SMI event. NOTE: When the SMI_LOCK bit is set, this bit cannot be changed. This bit is reset by PLTRST# assertion.

5.2.5 SMI Status Register (SMI_STS)—Offset 34h

Lockable: No
Usage: ACPI or Legacy
Power Well: Primary
Note: If the corresponding _EN bit is set when the _STS bit is set, the Intel PCH will cause an SMI# (except bits 8-10, which don't cause SMI#)

Access Method

Type: IO Register
(Size: 32 bits)

Device: 31
Function: 2

Default: 0h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
XHCI_SMI_STS	ME_SMI_STS	Serial_IO_SMI_STS	ESPI_SMI_STS	GPIO_UNLOCK_SMI_STS	SPI_SMI_STS	SCC_SMI_STS	RSVD				MONITOR_STS	PCI_EXP_SMI_STS	RSVD				SMBUS_SMI_STS	SERIRQ_SMI_STS	PERIODIC_STS	TCO_STS	DEVMON_STS	MCSMI_STS	GPIO_SMI_STS	GPE0_STS	PM1_STS_REG	RSVD			SWSMI_TMR_STS	APM_STS	SMI_ON_SLP_EN_STS	LEGACY_USB_STS	BIOS_STS	RSVD			

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**XHCI SMI Status (XHCI_SMI_STS):** This bit will be set when any USB3 (XHCI) Host Controller is requesting an SMI.
30	0h RO/V	**ME SMI Status (ME_SMI_STS):** This bit will be set when ME is requesting an SMI#.
29	0h RW/1C/V	**Intel Serial I/O SMI Status (Serial_IO_SMI_STS):** This bit gets set when Intel Serial I/O agent is requesting SMI #. This bit is set by hardware and cleared by software writing a 1 to this bit position.
28	0h RO/V	**eSPI SMI Status (ESPI_SMI_STS):** This bit is set if an eSPI agent is requesting an SMI#. This bit is set by hardware and cleared by software writing a 1 to its bit position.
27	0h RW/1C/V	**GPIO Unlock SMI Status (GPIO_UNLOCK_SMI_STS):** This bit will be set of the GPIO registers lockdown logic is requesting an SMI#. Writing a '1' to this bit position clears this bit to '0'. This bit is reset by PLTRST# assertion.
26	0h RO/V	**SPI SMI Status (SPI_SMI_STS):** This bit will be set when the SPI logic is requesting an SMI#. This bit is read only because the sticky status and enable bits associated with this function are located in the SPI registers.
25	0h RW/1C/V	**SCC SMI Status (SCC_SMI_STS):** This bit gets set when SCC agent is requesting SMI#.This bit is set by hardware and cleared by software writing a 1 to this bit position
24:22	0h RO	Reserved.
21	0h RO/V	**Monitor Status (MONITOR_STS):** This bit will be set if the Trap/SMI logic has caused the SMI. This will occur when the CPU or a bus master accesses an assigned register (or a sequence of accesses).
20	0h RO/V	**PCI_EXP_SMI Status (PCI_EXP_SMI_STS):** 1- PCI Express SMI event occurred. This could be due to a PCI Express PME event or Hot Plug Event.
19:17	0h RO	Reserved.
16	0h RW/1C/V	**SMBus SMI Status (SMBUS_SMI_STS):** 0 = This bit is set from the 64 KHz clock domain used by the SMBus. Software must wait at least 15.63 microseconds after initial assertion of this bit before clearing it. This bit is sticky and is cleared by writing a 1 to this bit position. 1 = Indicates that the SMI# was caused by: 1.The SMBus Slave receiving a message that an SMI# should be caused, or 2. The SMBALERT# signal goes active and the SMB_SMI_EN bit is set and the SMBALERT_DIS bit is cleared, or 3. The SMBus Slave receiving a HOST_NOTIFY message and the HOST_NOTIFY_INTREN and the SMB_SMI_EN bits are set, or 4. The SMBus Slave receiving a "SMI in S0" message. This bit is reset by PLTRST# assertion.
15	0h RO/V	**SERIRQ_SMI Status (SERIRQ_SMI_STS):** 1 = Indicates the SMI# was caused by the SERIRQ decoder. 0 = SMI# not caused by SERIRQ decoder. NOTE: this bit is not sticky. Writes to this bit will have no effect.
14	0h RW/1C/V	**Periodic Status (PERIODIC_STS):** This bit will be set at the rate determined by the PER_SMI_SEL bits. If the PERIODIC_EN bit is also set, the Intel PCH will generate an SMI#. This bit is cleared by writing a 1 to this bit position. This bit is reset by PLTRST# assertion.
13	0h RW/1C/V	**TCO Status (TCO_STS):** 0 = SMI not caused by TCO logic. 1 = Indicates SMI was caused by the TCO logic. NOTE: Will not cause wake event. This bit is cleared by writing a 1 to this bit position. This bit is reset by PLTRST# assertion.
12	0h RO/V	**DEVMON Status (DEVMON_STS):** This read-only bit is set when bit 0 in the DEVTRAP_STS register is set. It is not sticky, so writes to this bit will have no effect.
11	0h RW/1C/V	**Microcontroller SMI Status (MCSMI_STS):** This bit is set if there is an access to the power management microcontroller range (62h or 66h). If this bit is set, and the MCSMI_EN bit is also set, the Intel PCH will generate an SMI#. This bit is set by hardware and cleared by software writing a 1 to its bit position. This bit is reset by PLTRST# assertion.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RO/V	**GPIO SMI Status (GPIO_SMI_STS):** This bit will be a 1 if any GPIO that is enabled to trigger SMI is asserted. GPIOs that are not routed to cause an SMI will have no effect on this bit. This bit is NOT sticky. Writes to this bit will have no effect. Note: See the GPIO chapter for the individual GPIO SMI status, enable, and routing bit definitions.
9	0h RO/V	**GPE0 Status (GPE0_STS):** There are several status/enable bit pairs in GPE0_STS/EN_127_96 that are capable of triggering SMI#s. This bit is a logical OR of all of those pairs (i.e. this bit is asserted whenever at least one of those pairs has both the status and enable bit asserted). This bit is NOT sticky. Writes to this bit will have no effect. Note: The setting of this bit does not cause the SMI#. The following bit pairs are included in this logical OR: - GPE0_STS/EN_127_96 [18, 17, 16, 13, 11, 10, 8, 2]
8	0h RO/V	**PM1 Status Register (PM1_STS_REG):** This is an OR of the bits (except for bits 5 and 4) in the ACPI PM1 Status Reg. Not sticky. Writes to this bit have no effect. Note: The setting of this bit does not cause the SMI#.
7	0h RO	Reserved.
6	0h RW/1C/V	**Software SMI Timer Status (SWSMI_TMR_STS):** This bit will be set to 1 by the hardware when the Software SMI# Timer expires. This bit will remain 1 until the software writes a 1 to this bit. This bit is reset by PLTRST# assertion.
5	0h RW/1C/V	**APM Status (APM_STS):** SMI# was generated by a write access to the APM control register and if the APMC_EN bit is set. This bit is cleared by writing a one to its bit position. This bit is reset by PLTRST# assertion.
4	0h RW/1C/V	**SMI_ON_SLP_EN Status (SMI_ON_SLP_EN_STS):** This bit will be set by the Intel PCH when a write access attempts to set the SLP_EN bit. This bit is cleared by writing a 1 to this bit position. This bit is reset by PLTRST# assertion.
3	0h RO/V	**Legacy USB Status (LEGACY_USB_STS):** This non-sticky read-only bit is a logical OR of each of the SMI status bits in the USB Legacy Keybd Register ANDed with the corresponding enable bits. This bit will not be active if the enable bits are not set. Writes to this bit will have no effect.
2	0h RW/1C/V	**BIOS Status (BIOS_STS):** This bit gets set by hardware when a 1 is written by software to the GBL_RLS bit. When both BIOS_EN and the BIOS_STS bit are set, an SMI# will be generated. The BIOS_STS bit is cleared when software writes a 1 to this bit position. This bit is reset by PLTRST# assertion.
1:0	0h RO	Reserved.

5.2.6 General Purpose Event Control (GPE_CTRL)—Offset 40h

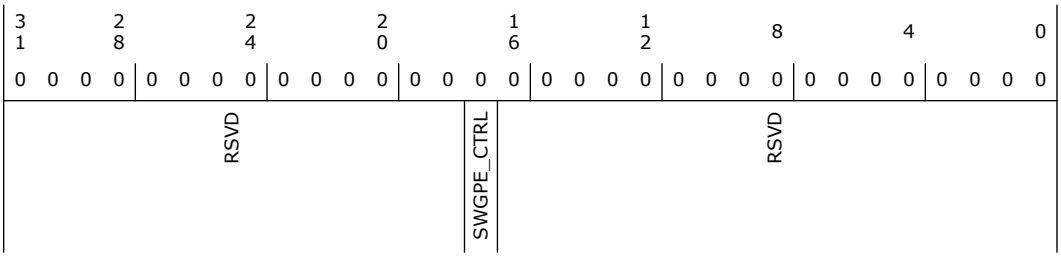
Lockable: No Usage: ACPI or Legacy Power Well: Primary Available: Desktop, Mobile

Access Method

Type: IO Register
(Size: 32 bits)

Device: 31
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17	0h RW/V	**Software GPE Control (SWGPE_CTRL):** This bit allows software to control the assertion of SWGPE_STS bit. This bit is used by hardware as the level input signal for the SWGPE_STS bit in the GPE0_STS register. When SWGPE_CTRL is 1, SWGPE_STS will be set to 1, and writes to SWGPE_STS with a value of 1 to clear SWGPE_STS will result in SWGPE_STS being set back to 1 by hardware. When SWGPE_CTRL is 0, writes to SWGPE_STS with a value of 1 will clear SWGPE_STS to 0. This bit is reset by RSMRST# assertion.
16:0	0h RO	Reserved.

5.2.7 Device Activity Status Register (DEVACT_STS)—Offset 44h

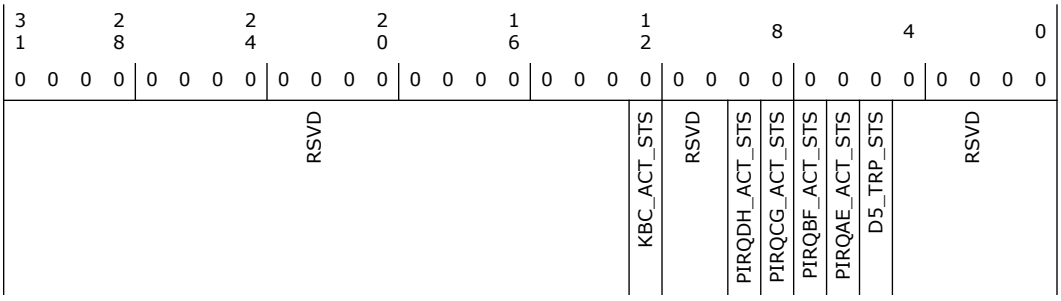
Each bit indicates if an access has occured to the corresponding device's trap range, or for bits 6:9, if the corresponding PCI interrupt is active. This register is used in conjunction with the Periodic SMI# timer to detect any system activity for legacy power management. The periodic SMI# timer indicates if it is the right time to read the DEVACT_STS register.
Note, software clears bits that are set in this register by writing a 1 to the bit position.

Access Method

Type: IO Register
(Size: 32 bits)

Device: 31
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	Reserved.
12	0h RW/1C/V	**Keyboard Controller Device Activity (KBC_ACT_STS):** KBC (60/64h). 0 = Indicates that there has been no access to this device I/O range. 1 = This device I/O range has been accessed. Clear this bit by writing a 1 to the bit location. This bit is reset by PLTRST# assertion.
11:10	0h RO	Reserved.
9	0h RW/1C/V	**PIRQDH Activity Status (PIRQDH_ACT_STS):** PIRQ[D or H] 0 = The corresponding PCI interrupts have not been active. 1 = At least one of the corresponding PCI interrupts have been active. Clear this bit by writing a 1 to the bit location. This bit is cleared by PLTRST# assertion.
8	0h RW/1C/V	**PIRQCG Activity Status (PIRQCG_ACT_STS):** PIRQ[C or G] 0 = The corresponding PCI interrupts have not been active. 1 = At least one of the corresponding PCI interrupts have been active. Clear this bit by writing a 1 to the bit location. This bit is cleared by PLTRST# assertion.
7	0h RW/1C/V	**PIRQBF Activitiy Status (PIRQBF_ACT_STS):** PIRQ[B or F] 0 = The corresponding PCI interrupts have not been active. 1 = At least one of the corresponding PCI interrupts have been active. Clear this bit by writing a 1 to the bit location. This bit is cleared by PLTRST# assertion.
6	0h RW/1C/V	**PIRQAE Activity Status (PIRQAE_ACT_STS):** PIRQ[A or E] 0 = The corresponding PCI interrupts have not been active. 1 = At least one of the corresponding PCI interrupts have been active. Clear this bit by writing a 1 to the bit location. This bit is cleared by PLTRST# assertion.
5	0h RW/1C/V	**D5 Trap Status (D5_TRP_STS):** 0 = The corresponding I/O have not been accessed. 1 = The following are accessed (as determined by the I/O ranges in the LPC decoder and even if the LPC forwarding is not enabled): SP1, SP2, PP, FDC. Clear this bit by writing a 1 to the bit location. This bit is cleared by PLTRST# assertion.
4:0	0h RO	Reserved.

5.2.8 PM2a Control Block (PM2A_CNT_BLK)—Offset 50h

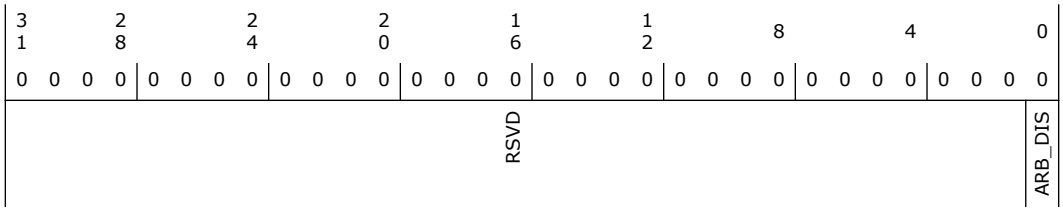
Lockable: No Usage: ACPI or Legacy Power Well: Primary Available: Desktop, Mobile
Note: BIOS must describe this register as 1 byte wide to the OS

Access Method

Type: IO Register
(Size: 32 bits)

Device: 31
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RW	**Arbiter Disable (ARB_DIS):** This bit is a scratchpad bit for legacy software compatibility. This bit is reset by PLTRST# assertion.

5.2.9 Over-Clocking WDT Control (OC_WDT_CTL)—Offset 54h

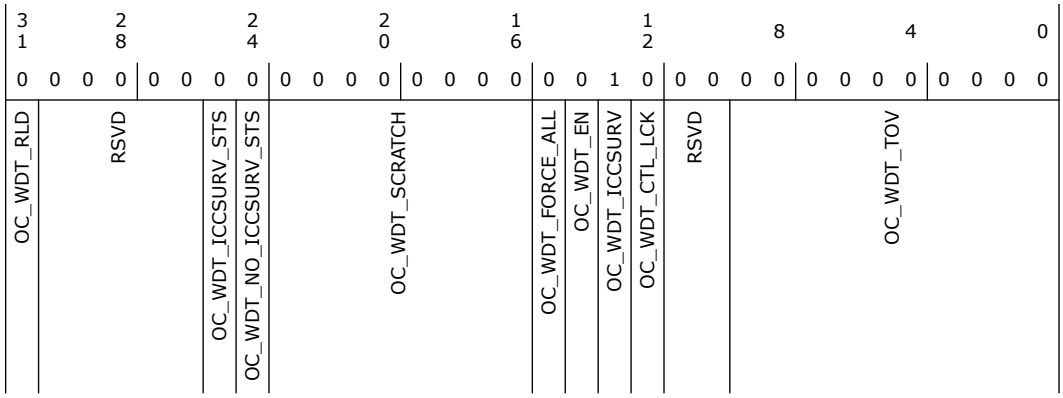
This register controls the operation of the PCH Over-Clocking Watchdog Timer.

Access Method

Type: IO Register
(Size: 32 bits)

Device: 31
Function: 2

Default: 2000h



Bit Range	Default & Access	Field Name (ID): Description
31	0h WO	**Over-Clocking WDT Reload (OC_WDT_RLD):** Software can write a '1' to this bit to reload ("ping") the PCH over-clocking watchdog timer while it is running. A write of '0' to this bit has no effect. A write of '1' to this bit while OC_WDT_EN=0, or with the clearing of OC_WDT_EN, does not start or reload the WDT (i.e. OC_WDT_EN takes precedence). The value in OC_WDT_TOV may be changed by software along with its setting of this bit. On a WDT reload, the current (potentially new) value in OC_WDT_TOV is loaded into the WDT as the new timeout value.
30:26	0h RO	Reserved.
25	0h RW/1C/V	**Over-Clocking WDT ICC Survivability Mode Timeout Status (OC_WDT_ICCSURV_STS):** This bit is set to '1' if the over-clocking WDT has timed out and triggered a global reset while running in a mode that has ICC survivability impact (OC_WDT_ICCSURV=1). It is cleared by a software write of '1' or by RSMRST# assertion.
24	0h RW/1C/V	**Over-Clocking WDT Non-ICC Survivability Mode Timeout Status (OC_WDT_NO_ICCSURV_STS):** This bit is set to '1' if the over-clocking WDT has timed out and triggered a global reset while running in a mode that does not have ICC survivability impact (OC_WDT_ICCSURV=0). It is cleared by a software write of '1' or by RSMRST# assertion.
23:16	0h RW	**Over-Clocking WDT Scratchpad (OC_WDT_SCRATCH):** This field is available as scratchpad space for software and has no effect on PCH HW operation. This bit is reset by RSMRST# assertion.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/L	**Over-Clocking WDT Force All (OC_WDT_FORCE_ALL):** GATE_BIT:OC_WDT_CTL.OC_WDT_CTL_LCK.HIGH When this bit is set to '1' and the OC_WDT is running, any included global reset source will behave as though the OC_WDT expired. This bit is reset by RSMRST# assertion or CF9 reset.
14	0h RW/V/L	**Over-Clocking WDT Enable (OC_WDT_EN):** Software sets this bit to '1' to enable the PCH over-clocking watchdog timer. While the counter is running, if it expires before being reloaded by software via the OC_WDT_RLD bit or halted by software clearing this bit, then one of the status bits will be set (which one depends on the WDT operating mode at the time - see the OC_WDT_ICCSURV bit description), and a global reset will be triggered. This bit is also set by the hardware when conditions allow the OC_WDT to self-start at power cycle reboot (effectively changes the default of this bit as seen by software).
13	1h RW/L	**Over-Clocking WDT ICC Survivability Impact (OC_WDT_ICCSURV):** This bit determines whether OC_WDT expiration will have an impact on ICC (Integrated Clock Controller) bootstrap survivability. OC_WDT_ICCSURV=1 (default) An OC_WDT timeout while operating in this mode causes certain ICC hardware auto-recovery actions to take place. A timeout in this mode will set OC_WDT_ICCSURV_STS.OC_WDT_ICCSURV=0 Software should configure the OC_WDT to this mode if no ICC hardware auto-recovery actions are desired in the event of a timeout. A timeout in this mode will set OC_WDT_NO_ICCSURV_STS
12	0h RW/L	**OC_WDT_CTL Register Lock (OC_WDT_CTL_LCK):** This bit controls write-ability to this register. Encodings: 0: All fields of register OC_WDT_CTL operate as normal and can be updated by software. Reads to the register operate as normal. 1: All RW/L fields of register OC_WDT_CTL, including this lock control bit, are locked. Writes to these register fields have no effect and the register fields retain their current states. Reads to the register operate as normal. Once this bit is set, it can only be cleared by Primary well power loss (via RSMRST# assertion).
11:10	0h RO	Reserved.
9:0	0h RW/V/L	**Over-Clocking WDT Timeout Value (OC_WDT_TOV):** Software programs the desired over-clocking WDT timeout value into this register. This timer is zero-based and has a granularity of 1 second. Example timeout values: 000h: 1 second 001h: 2 seconds ... 3FFh: ~17 minutes (1024 seconds) The value of OC_WDT_TOV may be changed by software along with its setting of the OC_WDT_RLD bit. On a WDT reload, the current (potentially new) value in OC_WDT_TOV is loaded into the WDT as the new timeout value. This field is also updated by the hardware when conditions allow the OC_WDT to self-start at power cycle reboot (effectively changes the default of this field as seen by software).

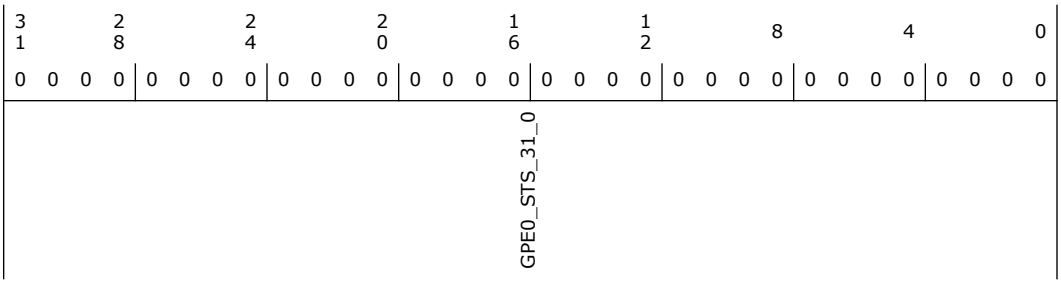
5.2.10 General Purpose Event 0 Status [31:0] (GPE0_STS_31_0)—Offset 80h

Access Method

Type: IO Register (Size: 32 bits)

Device: 31
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/1C/V	**General Purpose Event 0 Status [31:0] (GPE0_STS_31_0):** These bits are set any time the corresponding GPIO is setup as an input and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPE0_EN_31_0 register, then when the GPE0_STS_31_0 bit is set: - If system is in an S3-S5 state, the event will also wake the system. - If system is in an S0 state (or upon waking back to S0), an SCI will be caused, depending on the GPIROUTSCI bit for the corresponding GPI. These bits are sticky bits and are cleared by writing a 1 back to this bit position. Note: The GPP/GPD group mapped to this GPE0_STS_31_0 is configured via GPIO_CFG.DW0 and MISCCFG.DW0. Both GPIO_CFG.DW0 and MISCCFG.DW0 must be programmed to the same value.

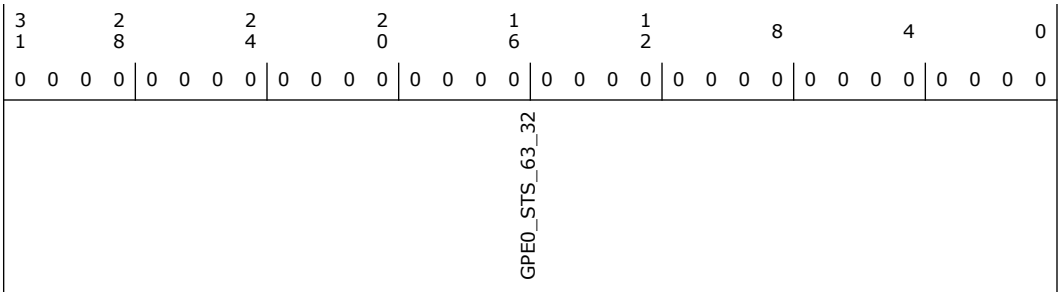
5.2.11 General Purpose Event 0 Status [63:32] (GPE0_STS_63_32)—Offset 84h

Access Method

Type: IO Register
(Size: 32 bits)

Device: 31
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/1C/V	**General Purpose Event 0 Status [63:32] (GPE0_STS_63_32):** These bits are set any time the corresponding GPIO is setup as an input and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPE0_EN_63_32 register, then when the GPE0_STS_63_32 bit is set: - If system is in an S3-S5 state, the event will also wake the system. - If system is in an S0 state (or upon waking back to S0), an SCI will be caused, depending on the GPIROUTSCI bit for the corresponding GPI. These bits are sticky bits and are cleared by writing a 1 back to this bit position. Note: The GPP/GPD group mapped to this GPE0_STS_63_32 is configured via GPIO_CFG.DW1 and MISCCFG.DW1. Both GPIO_CFG.DW1 and MISCCFG.DW1 must be programmed to the same value.

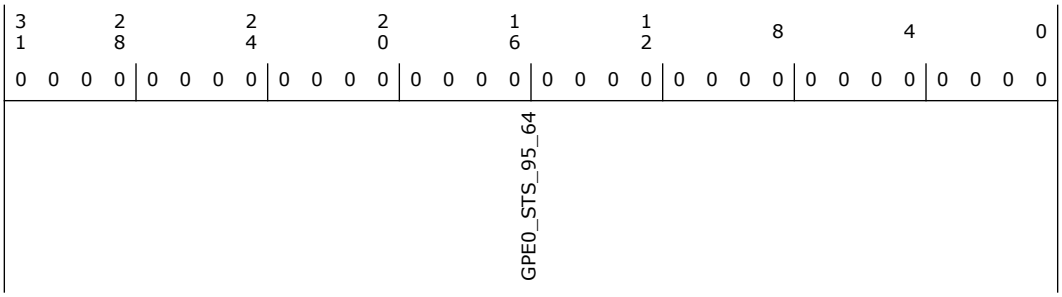
5.2.12 General Purpose Event 0 Status [95:64] (GPE0_STS_95_64)—Offset 88h

Access Method

Type: IO Register
(Size: 32 bits)

Device: 31
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/1C/V	**General Purpose Event 0 Status [95:64] (GPE0_STS_95_64):** These bits are set any time the corresponding GPIO is setup as an input and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPE0_EN_95_64 register, then when the GPE0_STS_95_64 bit is set: - If system is in an S3-S5 state, the event will also wake the system. - If system is in an S0 state (or upon waking back to S0), an SCI will be caused, depending on the GPIROUTSCI bit for the corresponding GPI. These bits are sticky bits and are cleared by writing a 1 back to this bit position. Note: The GPP/GPD group mapped to this GPE0_STS_95_64 is configured via GPIO_CFG.DW2 and MISCCFG.DW2. Both GPIO_CFG.DW2 and MISCCFG.DW2 must be programmed to the same value.

5.2.13 General Purpose Event 0 Status [127:96] (GPE0_STS[127:96])—Offset 8Ch

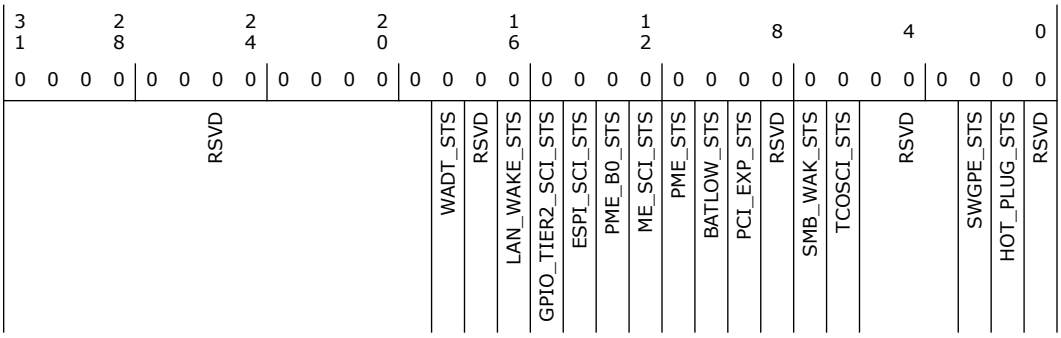
Note: This register is symmetrical to the General Purpose Event 0 Enable [127:96] Register. Unless indicated otherwise below, if the corresponding _EN bit is set, then when the STS bit get set, the Intel PCH will generate a Wake Event. Once back in an S0 state (or if already in an S0 state when the event occurs), the Intel PCH will also generate an SCI if the SCI_EN bit is set, or an SMI# if the SCI_EN bit is not set and GBL_SMI_EN is set.
Note that GPE0_STS bits 95:0 are claimed by the GPIO register block.

Access Method

Type: IO Register
(Size: 32 bits)

Device: 31
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	Reserved.
18	0h RW/1C/V	**Wake Alarm Device Timer Status (WADT_STS):** This bit is set whenever the any of the wake alarm device timers signal a timer expiration. This bit is reset by RSMRST# assertion.
17	0h RO	Reserved.
16	0h RW/1C/V	**LAN_WAKE# Pin Status (LAN_WAKE_STS):** This bit is set whenever LAN_WAKE# pin is seen asserted low. Note that unlike the GPI[n]_STS bits, LAN_WAKE# is always monitored as an input for the purpose of setting this bit, regardless of the actual GPIO configuration.
15	0h RW/1C/V	**GPIO Tier2 SCI Status (GPIO_TIER2_SCI_STS):** This bit is a logical OR of sci_wake from tier 2 GPIO's.
14	0h RW/1C/V	**eSPI SCI Status (ESPI_SCI_STS):** This bit will be set when an agent attached to eSPI is requesting an SCI. Note: This source is not able to cause a wake event. This bit is reset by RSMRST# assertion.
13	0h RW/1C/V	**Power Management Event Bus 0 Status (PME_B0_STS):** This bit will be set to 1 by the Intel PCH when any internal device with PCI Power Management capabilities on bus 0 asserts the equivalent of the PME# signal. Additionally, if the PME_B0_EN and SCI_EN bits are set, and the system is in an S0 state, then the setting of the PME_B0_STS bit will generate an SCI (or SMI# if SCI_EN is not set). If the PME_B0_EN bit is set, and the system is in an S3-S4 state (or S5 state due to SLP_TYP and SLP_EN), then the setting of the PME_B0_STS bit will generate a wake event. If the system is in an S5 state due to power button override, then the PME_B0_STS bit will not cause a wake event or SCI. This bit is cleared by a software write of '1'. Internal devices which can set this bit: - Integrated LAN - HD Audio/Audio DSP - SATA - EHCI ('USB2') - XHCI ('USB3') - ME Maskable Host Wake This bit is reset by RSMRST# assertion.
12	0h RW/1C/V	**ME SCI Status (ME_SCI_STS):** This bit will be set when ME is requesting an SCI. Software must clear the ME source of the SCI before clearing this bit. Note: This source is not able to cause a wake event. This bit is reset by RSMRST# assertion.
11	0h RW/1C/V	**Power Management Event Status (PME_STS):** This bit will be set to 1 by hardware when the PME# signal goes active. Additionally, if the PME_EN and SCI_EN bits are set, and system is in an S0 state, then the setting of the PME_STS bit will generate an SCI (or SMI# if SCI_EN is not set). If the PME_EN bit is set, and the system is in an S3-S4 state (or S5 state due to SLP_TYP and SLP_EN), then the setting of the PME_STS bit will generate a wake event. If the system is in an S5 state due to power button override, then PME_STS will not cause a wake event or SCI. This bit is cleared by writing a 1 to this bit position or RSMRST# assertion.
10	0h RW/1C/V	**Battery Low Status (BATLOW_STS):** In Mobile Mode this bit will be set to 1 by hardware when the BATLOW# signal goes low. Software clears the bit by writing a 1 to the bit position. In Desktop Mode, this bit will be treated as Reserved. This bit is reset by RSMRST# assertion.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW/1C/V	**PCI Express Status (PCI_EXP_STS):** This bit will be set to 1 by hardware to indicate that: - The PME event message was received on one or more of the PCI-Express Ports - An Assert PMEGPE message received from the MCH via DMI Note: The PCI WAKE# pin and the PCI-Express Beacons have no impact on this bit. Software attempts to clear this bit by writing a 1 to this bit position. If the PCI_EXP_STS bit went active due to an Assert PMEGPE message, then a Deassert PMEGPE message must be received prior to the software write in order for the bit to be cleared. If the bit is not cleared and the corresponding PCI_EXP_EN bit is set, the leveltriggered SCI will remain active. Note that a race condition exists where the PCI Express device sends another PME message because the PCI Express device was not serviced within the time when it must resend the message. This may result in a spurious interrupt, and this is comprehended and approved by the PCI Express specification. The window for this race condition is approximately 95-105 milliseconds. This bit is reset by RSMRST# assertion.
8	0h RO	Reserved.
7	0h RW/1C/V	**SMBus Wake Status (SMB_WAK_STS):** This bit is set to 1 by the hardware to indicate that the wake event was caused by the PCH's SMBus logic. This could be due to either the SM Bus slave unit receiving a message or the SMBALERT# signal going active. NOTES: 1. The SMBus controller will independently cause an SMI# so this bit does not need to do so (unlike the other bits in this register). 2. This bit is set by the SMBus slave command 01h (Wake/SMI#) even when the system is in the S0 state. Therefore, to avoid an instant wake on subsequent transitions to sleep states, software must clear this bit after each reception of the Wake/SMI# command or just prior to entering the sleep state. 3. The SMBALERT_STS bit (D31:F3:I/O Offset 00h:bit 5) should be cleared by software before clearing this bit. This bit is reset by RSMRST# assertion.
6	0h RW/1C/V	**TCOSCI Status (TCOSCI_STS):** This bit will be set to 1 by hardware when the TCO logic or Thermal Sensor logic causes an SCI. This bit can be reset by writing a one to this bit position or by RSMRST# assertion.
5:3	0h RO	Reserved.
2	0h RW/1C/V	**Software GPE Status (SWGPE_STS):** The SWGPE_CTRL bit (bit 1 of GPE_CTRL reg) acts as a level input to this bit. This bit is reset by RSMRST# assertion.
1	0h RW/1C/V	**Hot Plug Status (HOT_PLUG_STS):** Enables PCH to cause an SCI when the HOT_PLUG_STS bit is set. This is used to allow the PCI Express ports to cause an SCI due to hot-plug events. The following events cause HOT_PLUG_STS bit to set - Assert GPE message received from any of the PCIE ports in PCH - Assert HPGPE message received from any of the PCIE ports in PCH - Assert GPE message received downstream from MCH - Assert HPGPE message received downstream from MCH. This bit is reset by RSMRST# assertion.
0	0h RO	Reserved.

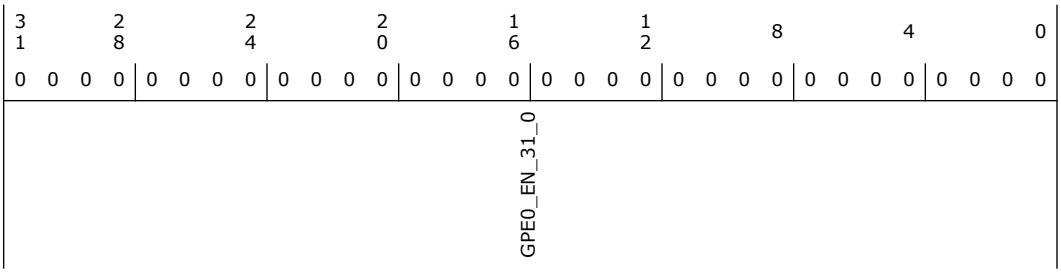
5.2.14 General Purpose Event 0 Enable [31:0] (GPE0_EN_31_0)—Offset 90h

Access Method

Type: IO Register
(Size: 32 bits)

Device: 31
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**General Purpose Event 0 Enable [31:0] (GPE0_EN_31_0):** These bits enable the corresponding GPE0_STS[31:0] bits being set to cause an SCI and/or wake event. Note: The GPP/GPD group mapped to this GPE0_EN_31_0 is configured via GPIO_CFG.DW0 and MISCCFG.DW0. Both GPIO_CFG.DW0 and MISCCFG.DW0 must be programmed to the same value.

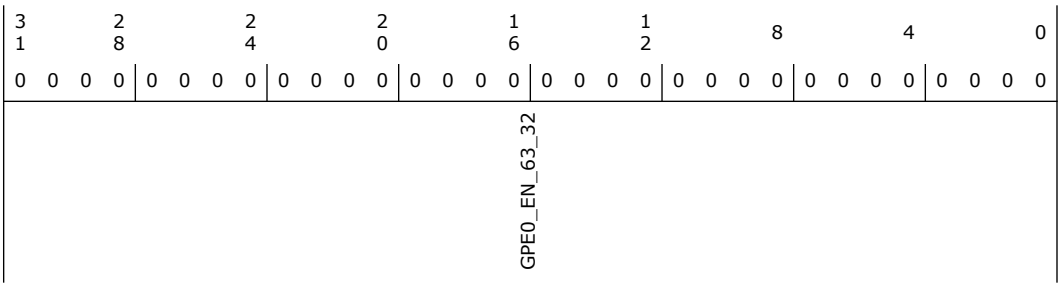
5.2.15 General Purpose Event 0 Enable [63:32] (GPE0_EN_63_32)—Offset 94h

Access Method

Type: IO Register
(Size: 32 bits)

Device: 31
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**General Purpose Event 0 Enable [63:32] (GPE0_EN_63_32):** These bits enable the corresponding GPE0_STS[63:32] bits being set to cause an SCI and/or wake event. Note: The GPP/GPD group mapped to this GPE0_EN_63_32 is configured via GPIO_CFG.DW1 and MISCCFG.DW1. Both GPIO_CFG.DW1 and MISCCFG.DW1 must be programmed to the same value.

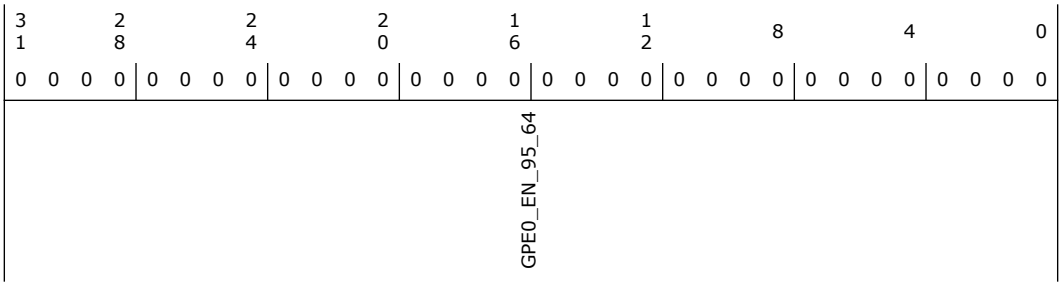
5.2.16 General Purpose Event 0 Enable [95:64] (GPE0_EN_95_64)—Offset 98h

Access Method

Type: IO Register
(Size: 32 bits)

Device: 31
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**General Purpose Event 0 Enable [95:64] (GPE0_EN_95_64):** These bits enable the corresponding GPE0_STS[95:64] bits being set to cause an SCI and/or wake event. Note: The GPP/GPD group mapped to this GPE0_EN_95_64 is configured via GPIO_CFG.DW2 and MISCCFG.DW2. Both GPIO_CFG.DW2 and MISCCFG.DW2 must be programmed to the same value.

5.2.17 General Purpose Event 0 Enable [127:96] (GPE0_EN[127:96])—Offset 9Ch

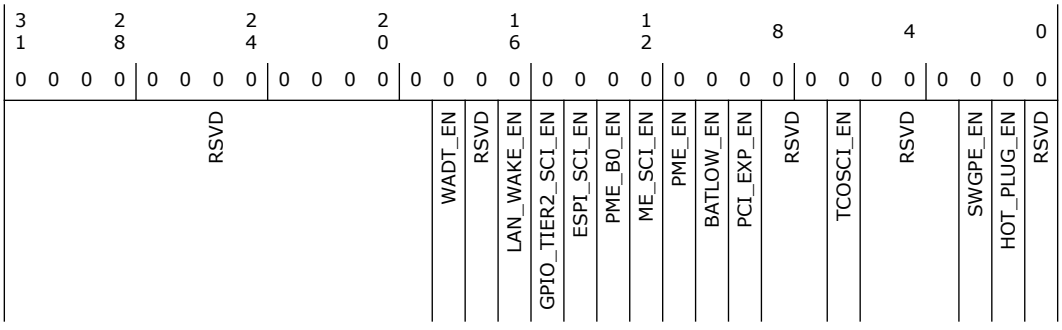
Note: This register is symmetrical to the General Purpose Event 0 Status [127:96] Register.
Note that GPE0_STS bits 95:0 are claimed by the GPIO register block.

Access Method

Type: IO Register
(Size: 32 bits)

Device: 31
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	Reserved.
18	0h RW	**Wake Alarm Device Timer Enable (WADT_EN):** Used to enable the setting of the WADT_STS bit to generate Wake/SMI#/SCI. This bit is reset by DSW_PWROK de-assertion.
17	0h RO	Reserved.
16	0h RW	**LAN_WAKE# Pin Enable (LAN_WAKE_EN):** Used to enable the setting of the LAN_WAKE_STS bit to generate wake/SMI#/SCI. Host wake events from the PHY through LAN_WAKE# cannot be disabled by clearing this bit. Note that LAN_WAKE# pin is a valid host wake event from Deep-Sx (when configured as native function). But the wake enable configuration must persist even after a G3. So this bit is in the RTC well.
15	0h RW/V	**GPIO Tier2 SCI EN (GPIO_TIER2_SCI_EN):** Used to enable the setting of GPIO_TIER2_SCI_STS to generate wake/SCI#.
14	0h RW/V	**eSPI SCI Enable (ESPI_SCI_EN):** Used to enable the setting of the ESPI_SCI_STS bit to generate a SCI.
13	0h RW/V	**PME_B0 Enable (PME_B0_EN):** Enables the setting of the PME_B0_STS bit to generate a wake event and/or an SCI or SMI#. This bit is reset by RTCRST# assertion.
12	0h RW/V	**ME SCI Enable (ME_SCI_EN):** Used to enable the setting of the ME_SCI_STS bit to generate a SCI.
11	0h RW/V	**Power Management Event Enable (PME_EN):** Enables the setting of the PME_STS to generate a wake event and/or an SCI. This bit is reset by RTCRST# assertion.
10	0h RW/V	**Low Battery Enable (BATLOW_EN):** In Mobile Mode, this bit enables the BATLOW# signal to cause an SMI# or SCI (depending on the SCI_EN bit) when it goes low.This bit does not prevent the BATLOW# signal from inhibiting the wake event. In Desktop Mode this bit will be treated as Reserved. This bit is reset by RTCRST# assertion.
9	0h RW/V	**PCI Express Enable (PCI_EXP_EN):** Enables PCH to cause an SCI when PCI_EXP_STS bit is set. This is used to allow the PCI Express ports, including the link to the MCH, to cause an SCI due to wake/PME events.
8:7	0h RO	Reserved.
6	0h RW/V	**TCOSCI Enable (TCOSCI_EN):** When TCOSCI_EN and TCOSCI_STS are both set, an SCI will be generated. This bit is reset by RSMRST# assetion.
5:3	0h RO	Reserved.
2	0h RW/V	**Software GPE Enable (SWGPE_EN):** This bit, when set to 1, enables the SW GPE function. If SWGPE_CTRL is written to a 1, hardware will set SWGPE_STS (acts as a level input) If SWGPE_STS, SWGPE_EN, and SCI_EN are all 1's, an SCI will be generated If SWGPE_STS = 1, SWGPE_EN = 1, SCI_EN = 0, and GBL_SMI_EN = 1 then an SMI# will be generated
1	0h RW/V	**Hot Plug Enable (HOT_PLUG_EN):** Enables PCH to cause an SCI when the HOT_PLUG_STS bit is set. This is used to allow the PCI Express ports to cause an SCI due to hot-plug events. The following events cause HOT_PLUG_STS bit to set - Assert GPE message received from any of the PCIE ports in PCH - Assert HPGPE message received from any of the PCIE ports in PCH - Assert GPE message received downstream from MCH - Assert HPGPE message received downstream from MCH
0	0h RO	Reserved.

5.3 PMC Memory Mapped Registers Summary

The PMC memory mapped registers are accessed based upon offsets from PM Base Address (PWRMBASE) defined in PCI Device 31: Function 2, offset 48h.

Table 5-3. Summary of PMC Memory Mapped Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	Wake Alarm Device Timer: AC (WADT_AC)—Offset 0h	FFFFFFFFh
4h	7h	Wake Alarm Device Timer: DC (WADT_DC)—Offset 4h	FFFFFFFFh
8h	Bh	Wake Alarm Device Expired Timer: AC (WADT_EXP_AC)—Offset 8h	FFFFFFFFh
Ch	Fh	Wake Alarm Device Expired Timer: DC (WADT_EXP_DC)—Offset Ch	FFFFFFFFh
10h	13h	Power and Reset Status (PRSTS)—Offset 10h	0h
14h	17h	Chipset Initialization Register 14 (CIR14)—Offset 14h	0h
18h	1Bh	Power Management Configuration Reg 1 (PM_CFG)—Offset 18h	20h
20h	23h	Message to PMC (MTPMC)—Offset 20h	0h
24h	27h	PCH Power Management Status (PCH_PM_STS2)—Offset 24h	0h
28h	2Bh	S3 Power Gating Policies (S3_PWRGATE_POL)—Offset 28h	0h
2Ch	2Fh	S4 Power Gating Policies (S4_PWRGATE_POL)—Offset 2Ch	0h
30h	33h	S5 Power Gating Policies (S5_PWRGATE_POL)—Offset 30h	0h
34h	37h	DeepSx Configuration (DSX_CFG)—Offset 34h	0h
3Ch	3Fh	Power Management Configuration Reg 2 (PM_CFG2)—Offset 3Ch	0h
40h	43h	Chipset Initialization Register 40 (CIR40)—Offset 40h	0h
44h	47h	Chipset Initialization Register 44 (CIR44)—Offset 44h	0h
48h	4Bh	Chipset Initialization Register 48 (CIR48)—Offset 48h	0h
4Ch	4Fh	Chipset Initialization Register 4C (CIR4C)—Offset 4Ch	0h
50h	53h	Chipset Initialization Register 50 (CIR50)—Offset 50h	0h
54h	57h	Chipset Initialization Register 54 (CIR54)—Offset 54h	0h
58h	5Bh	Chipset Initialization Register 58 (CIR58)—Offset 58h	0h
60h	63h	Chipset Initialization Register 60 (CIR60)—Offset 60h	0h
68h	6Bh	Chipset Initialziation Register 68 (CIR68)—Offset 68h	0h
78h	7Bh	Chipset Initialization Register 78 (CIR78)—Offset 78h	0h
7Ch	7Fh	Chipset Initialization Register 7C (CIR7C)—Offset 7Ch	0h
80h	83h	Chipset Initialization Register 80 (CIR80)—Offset 80h	0h
84h	87h	Chipset Initialization Register 84 (CIR84)—Offset 84h	0h
88h	8Bh	Chipset Initialization Register 88 (CIR88)—Offset 88h	0h
8Ch	8Fh	Chipset Initialization Register 8C (CIR8C)—Offset 8Ch	0h
90h	93h	Chipset Initialization Register 90 (CIR90)—Offset 90h	0h
98h	9Bh	Chipset Initialization Register 98 (CIR98)—Offset 98h	0h
A0h	A3h	Chipset Initialization Register A0 (CIRA0)—Offset A0h	0h
A4h	A7h	Chipset Initialization Register A4 (CIRA4)—Offset A4h	0h
A8h	ABh	Chipset Initizaliation Register A8 (CIRA8)—Offset A8h	0h
ACh	AFh	Chipset Initizaliation Register AC (CIRAC)—Offset ACh	0h

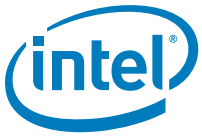


Table 5-3. Summary of PMC Memory Mapped Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
B0h	B3h	Chipset Initialization Register B0 (CIRB0)—Offset B0h	0h
B4h	B7h	Chipset Initialization Register B4 (CIRB4)—Offset B4h	0h
C0h	C3h	Chipset Initialization Register C0 (CIRC0)—Offset C0h	0h
C4h	C7h	PMSYNC Thermal Power Reporting Configuration (PMSYNC_TPR_CFG)—Offset C4h	0h
C8h	CBh	PM_SYNC Miscellaneous Configuration (PM_SYNC_MISC_CFG)—Offset C8h	0h
D0h	D3h	Chipset Initialization Register D0 (CIRD0)—Offset D0h	0h
D4h	D7h	Chipset Initialization Register D4 (CIRD4)—Offset D4h	0h
DCh	DFh	Chipset Initialization Register DC (CIRDC)—Offset DCh	0h
E0h	E3h	Chipset Initialization Register E0 (CIRE0)—Offset E0h	0h
E4h	E7h	Chipset Initialization Register E4 (CIRE4)—Offset E4h	0h
E8h	EBh	Chipset Initializatin Register E8 (CIRE8)—Offset E8h	8000h
FCh	FFh	ACPI Timer Control (ACPI_TMR_CTL)—Offset FCh	0h
100h	103h	VR Miscellaneous Control (VR_MISC_CTL)—Offset 100h	0h
110h	113h	Last TSC Alarm Value[31:0] (TSC_ALARM_LO)—Offset 110h	0h
114h	117h	Last TSC Alarm Value[63:32] (TSC_ALARM_HI)—Offset 114h	0h
120h	123h	GPIO Configuration (GPIO_CFG)—Offset 120h	432h
124h	127h	Global Reset Causes (GBLRST_CAUSE0)—Offset 124h	0h
128h	12Bh	Global Reset Causes Register 1 (GBLRST_CAUSE1)—Offset 128h	0h
13Ch	13Fh	SLP S0 RESIDENCY (SLP_S0_RES)—Offset 13Ch	0h
200h	203h	ModPhy Power Management Configuration 1 (MODPHY_PM_CFG1)—Offset 200h	FFFFh
204h	207h	MODPHY Power Management Configuration 2 (MODPHY_PM_CFG2)—Offset 204h	0h
208h	20Bh	MODPHY Power Management Configuration 3 (MODPHY_PM_CFG3)—Offset 208h	0h
20Ch	20Fh	MODPHY Power Management Configuration 4 (MODPHY_PM_CFG4)—Offset 20Ch	0h
31Ch	31Fh	Chipset Initialization Register 31C (CIR31C)—Offset 31Ch	0h
324h	327h	Chipset Initialization Register 324 (CIR324)—Offset 324h	0h
328h	32Bh	Chipset Initialization Register 328 (CIR328)—Offset 328h	0h
32Ch	32Fh	Chipset Initialization Register 32C (CIR32C)—Offset 32Ch	0h
3ECh	3EFh	Clock Source Shutdown Control Reg 2 (CS_SD_CTL2)—Offset 3ECh	0h
590h	593h	PFET Enable Ack Register 0 (PPFEAR0)—Offset 590h	0h
594h	597h	PFET Enable Ack Register 1 (PPFEAR1)—Offset 594h	0h
5D0h	5D3h	Host SW PG Control Register 1 (HSWPGCR1)—Offset 5D0h	0h
620h	623h	Static PG Function Disable 1 (ST_PG_FDIS1)—Offset 620h	0h
628h	62Bh	Chipset Initialization Register (NST_PG_FDIS_1)—Offset 628h	0h
644h	647h	Capability Disable Read Register (FUSE_DIS_RD_2)—Offset 644h	8h

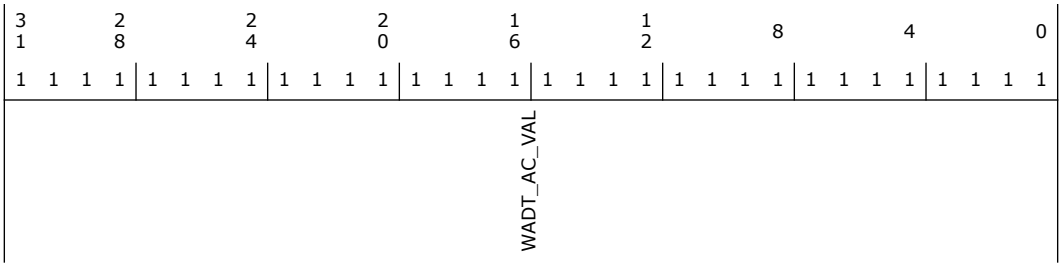
5.3.1 Wake Alarm Device Timer: AC (WADT_AC)—Offset 0h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 2

Default: FFFFFFFFh



Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW/V	**Wake Alarm Device Timer Value for AC Mode (WADT_AC_VAL):** This field contains the 32-bit wake alarm device timer value (granularity 1s) for AC power. The timer begins decrementing when written to a value other than FFFFFFFFh (regardless of the power source when the write occurs). Upon counting down to 0: - If on AC power, GPE0b_STS.WADT_STS will be set. This status bit being set will generate a host wake if GPE0b_EN.WADT_EN is 1. - If the power source is DC at this time, the status bit is not set. However, if AC power subsequently returns to the platform, the AC Expired Timer begins running. See the WADT_EXP_AC register for details. - The timer returns to its default value of FFFFFFFFh. This bit is reset by DSW_PWROK de-assertion.

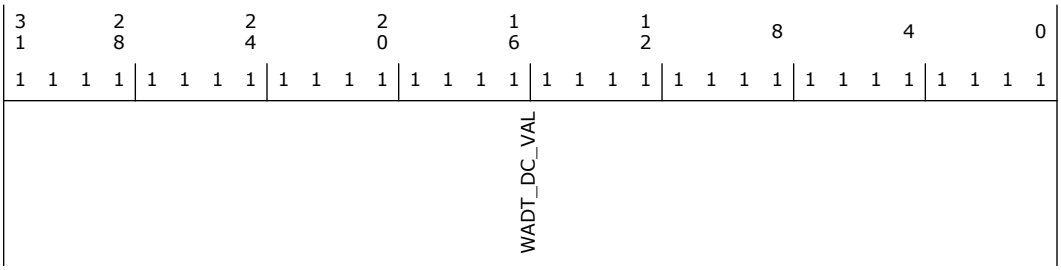
5.3.2 Wake Alarm Device Timer: DC (WADT_DC)—Offset 4h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 2

Default: FFFFFFFFh



Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW/V	**Wake Alarm Device Timer Value for DC Mode (WADT_DC_VAL):** This field contains the 32-bit wake alarm device timer value (granularity 1s) for DC power. The timer begins decrementing when written to a value other than FFFFFFFFh (regardless of the power source when the write occurs). Upon counting down to 0: - If on DC power, GPE0b_STS.WADT_STS will be set. This status bit being set will generate a host wake if GPE0b_EN.WADT_EN is 1. - If the power source is AC at this time, the status bit is not set. However, if DC power subsequently returns to the platform, the DC Expired Timer begins running. See the WADT_EXP_DC register for details. - The timer returns to its default value of FFFFFFFFh. This bit is reset by DSW_PWROK de-assertion.

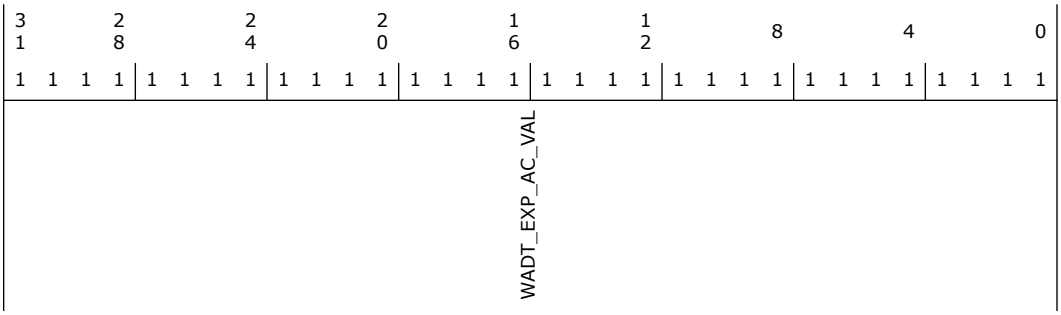
5.3.3 Wake Alarm Device Expired Timer: AC (WADT_EXP_AC)—Offset 8h

Access Method

Type: MEM Register (Size: 32 bits)

Device: 31
Function: 2

Default: FFFFFFFFh



Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW/V	**Wake Alarm Device Expired Timer Value for AC Mode (WADT_EXP_AC_VAL):** This field contains the 32-bit wake alarm device "Expired Timer" value (granularity 1s) for AC power. The timer begins decrementing after switching from DC to AC power. In the case where the WADT_AC timer has already expired while the platform was on DC power, this timer only decrements while operating on AC power. So if the power source switches back to DC power, the timer will stop (but not reset). When AC power returns, the timer will again begin decrementing. Note: This timer will only begin decrementing under the conditions described above if this field has been configured for something other than its default value of FFFFFFFFh (i.e. FFFFFFFFh = disabled). Upon expiration of this timer: - If on AC power, GPE0b_STS.WADT_STS will be set. This status bit being set will generate a host wake if GPE0b_EN.WADT_EN is 1. - BOTH the AC and DC Expired Timers return to their defaults value of FFFFFFFFh. This bit is reset by DSW_PWROK de-assertion.

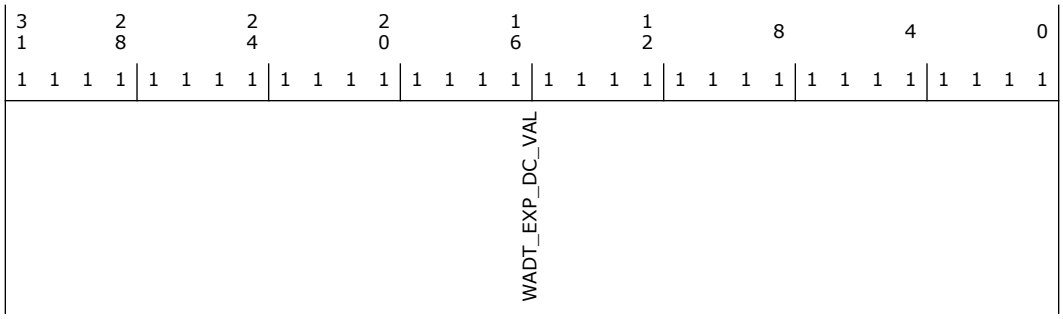
5.3.4 Wake Alarm Device Expired Timer: DC (WADT_EXP_DC)—Offset Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 2

Default: FFFFFFFFh



Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW/V	**Wake Alarm Device Expired Timer Value for DC Mode (WADT_EXP_DC_VAL):** This field contains the 32-bit wake alarm device "Expired Timer" value (granularity 1s) for DC power.The timer begins decrementing after switching from AC to DC power. In the case where the WADT_DC timer has already expired while the platform was on AC power, this timer only decrements while operating on DC power. So if the power source switches back to AC power, the timer will stop (but not reset). When DC power returns, the timer will again begin decrementing. Note: This timer will only begin decrementing under the conditions described above if this field has been configured for something other than its default value of FFFFFFFFh (i.e. FFFFFFFFh = disabled). Upon expiration of this timer: - If on DC power, GPE0b_STS.WADT_STS will be set. This status bit being set will generate a host wake if GPE0b_EN.WADT_EN is 1. - BOTH the AC and DC Expired Timers return to their defaults value of FFFFFFFFh. This bit is reset by DSW_PWROK de-assertion.

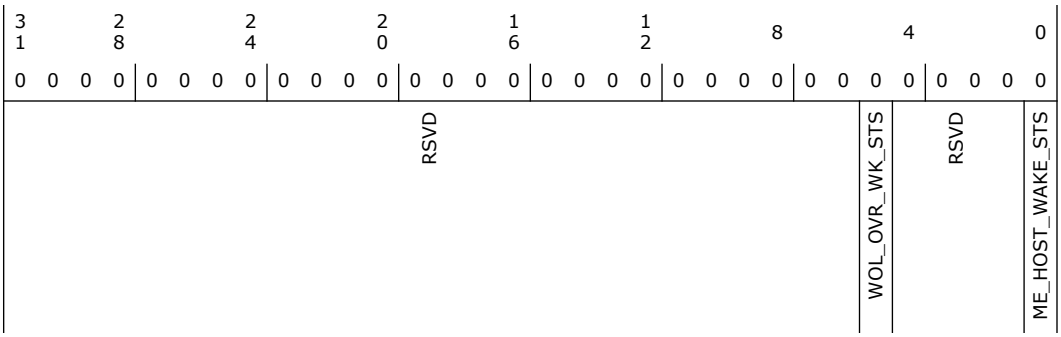
5.3.5 Power and Reset Status (PRSTS)—Offset 10h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	Reserved.
5	0h RW/1C/V	**Wake On LAN Override Wake Status (WOL_OVR_WK_STS):** This bit gets set when integrated LAN Signals a Power Management Event AND the system is in S5. BIOS can read this status bit to determine this wake source. Software clears this bit by writing a 1 to it.
4:1	0h RO	Reserved.
0	0h RW/1C/V	**ME_HOST_WAKE_STS (ME_HOST_WAKE_STS):** This bit is set when the ME generates a non-maskable wake event and is not affected by any other enable bit. When this bit is set, the host power management logic wakes to S0.

5.3.6 Chipset Initialization Register 14 (CIR14)—Offset 14h

BIOS may write to the register

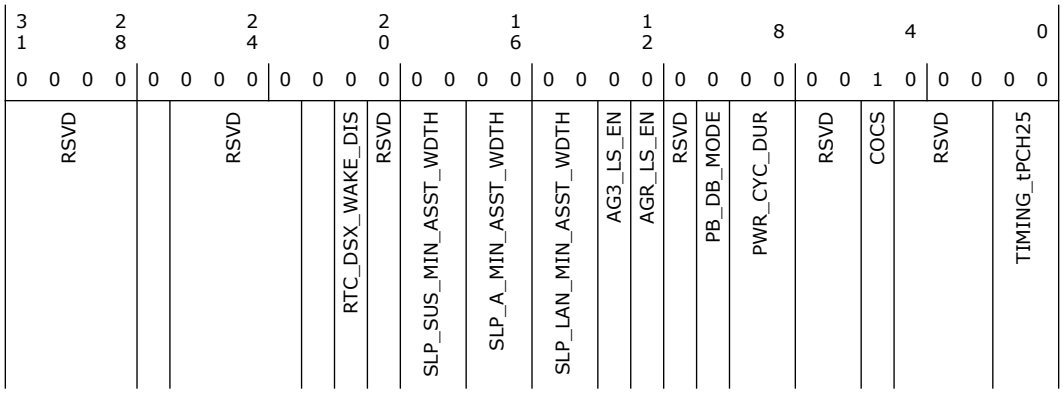
5.3.7 Power Management Configuration Reg 1 (PM_CFG)—Offset 18h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 2

Default: 20h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	Reserved.
27	0h RW/L	**Reserved:** BIOS may program this register bit.
26:23	0h RO	Reserved.
22	0h RW/L	**Reserved:** BIOS may need to program this bit.
21	0h RW	**RTC Wake from DeepSx Disable (RTC_DSX_WAKE_DIS):** When set, this bit disables RTC wakes from waking the system from DeepSx. This bit is reset by RTCRST# assertion.
20	0h RO	Reserved.
19:18	0h RW/L	**SLP_SUS# Minimum Assertion Width (SLP_SUS_MIN_ASST_WDTH):** This 2-bit value indicates the minimum assertion width of the SLP_SUS# signal to guarantee that the SUS well power supplies have been fully power-cycled. This value may be modified per platform depending on power supply capacitance, board capacitance, power failure detection circuits, etc. Settings are: 00 = 0 ms (i.e. stretching disabled - default) 01 = 500ms 10 = 1s 11 = 4s This field is not writable when the SLP_Sx# Stretching Policy Lock-Down bit is set. This field is ignored when exiting a G3 state if the "Disable SLP_X Stretching After SUS Power Failure" bit is set. Note that unlike with all other SLP_* pin stretching, this disable bit only impacts SLP_SUS# stretching during G3 exit rather than both G3 and DeepSx exit. SLP_SUS# stretching always applies to DeepSx regardless of the disable bit. Programming Note: For platforms that enable DeepSx, BIOS must program SLP_SUS# stretching to be greater than or equal to the largest stretching value on any other SLP_* pin (SLP_S3#, SLP_S4#, SLP_LAN#, or SLP_A#). This bit is cleared by the RTCRST# pin.

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RW/L	**SLP_A# Minimum Assertion Width (SLP_A_MIN_ASST_WDTH):** This 2-bit value indicates the minimum assertion width of the SLP_A# signal to guarantee that the ASW power supplies have been fully power-cycled. This value may be modified per platform depending on power supply capacitance, board capacitance, power failure detection circuits, etc. Settings are: 00 = 0 ms (i.e. stretching disabled - default) 01 = 4 s 10 = 98 ms 11 = 2 s This field is not writable when the SLP_Sx# Stretching Policy Lock-Down bit is set. This field is ignored when exiting a G3 or Deep Sx state if the "Disable SLP_X Stretching After SUS Power Failure" bit is set. This bit is cleared by the RTCRST# pin.
15:14	0h RW/L	**SLP_LAN# Minimum Assertion Width (SLP_LAN_MIN_ASST_WDTH):** This 2-bit value indicates the minimum assertion width of the SLP_LAN# signal to guarantee that the power to the PHY has been fully power-cycled. This value may be modified per platform depending on power supply, capacitance, board capacitance, power failure detection circuits, etc. This field is not writable when the SLP_Sx# Stretching Policy Lock Down bit is set to 1. This bit is reset by RTCRST# assertion.
13	0h RW	**After G3 Last State Enable (AG3_LS_EN):** When PM_CFG.AG3E is '0', AG3_LS_EN determines whether the PCH will consider the platform's previous state when determining whether to power-up after G3. Encodings: 0: PCH power-up policies after G3 do not depend on the platform's state when the G3 occurred. (default) 1: PCH power-up policies after G3 depend on the platform's state when the G3 occurred. - If the power failure occurred while the platform was in S0 or while in the process of going to S0, the platform will power-up to S0 upon exiting G3. - If the power failure occurred while the platform was in Sx or while in the process of going to Sx, the platform will stay in S4/S5 upon exiting G3. Note: This bit applies only when GEN_PMCON_3.AG3E is '0'. If AG3E is '1', the platform will always stay in S4/S5 after G3 regardless of the value of AG3_LS_EN.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW	**After Global Reset Last State Enable (AGR_LS_EN):** AGR_LS_EN determines whether the PCH will consider the platform's previous state when determining whether to power-up after non-thermal and non-explicitly requested global resets. Encodings: 0 (default): PCH power-up policies after a global reset do not depend on the platform's state when the reset occurred. 1: PCH power-up policies after a global reset depend on the platform's state when the reset occurred. If the global reset occurred while the platform was in S0 or while in the process of going to S0, the platform will power-up to S0 after the reset. If the global reset occurred while the platform was in Sx or while in the process of going to Sx, the platform will stay in S5 upon exiting G3.
11	0h RO	Reserved.
10	0h RW	**Power Button Debounce Mode (PB_DB_MODE):** This bit controls when interrupts (SMI#, SCI) are generated in response to assertion of the PWRBTN# pin. This bit's values cause the following behavior: - '0': The 16ms debounce period applies to all usages of the PWRBTN# pin (legacy behavior). - '1': When a falling edge occurs on the PWRBTN# pin, an interrupt is generated and the 16ms debounce timer starts. Subsequent interrupts are masked while the debounce timer is running. Note: Power button override logic always samples the post-debounce version of the pin. This bit is reset by RTCRST# assertion.

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h RW/L	**Reset Power Cycle Duration (PWR_CYC_DUR):** The value in this register determines the minimum time a platform will stay in reset (SLP_S3#, SLP_S4#, SLP_S5# asserted and also SLP_A# and SLP_LAN# asserted if applicable) during a host partition reset with power cycle or a global reset. The duration programmed in this register takes precedence over the applicable SLP_# stretch timers in these reset scenarios. This field is not writable when the SLP_Sx# Stretching Policy Lock-Down bit is set. Note that the duration programmed in this register should never be smaller than the stretch duration programmed in the following registers - - GEN_PMCON_3.SLP_S3_MIN_ASST_WDTH - GEN_PMCON_3.S4MAW - PM_CFG.SLP_A_MIN_ASST_WDTH - PM_CFG.SLP_LAN_MIN_ASST_WDTH This bit is reset by RTCRST# assertion. 00 = 4 - 5 seconds 01 = 3 - 4 seconds 10 = 2 - 3 seconds 11 = 1 - 2 seconds
7:6	0h RO	Reserved.
5	1h RW/V	**CPU OC Strap (COCS):** SW programs this pin with the value that should be reflected to the GPIO8_OCS pin, when the pin is in native mode. Hardware also sets this bit when the over-clocking watchdog timer expires. This bit is reset by RSMRST# assertion.
4:2	0h RO	Reserved.
1:0	0h RW/V	**Timing tPCH25 (TIMING_tPCH25):** This field configures the tPCH25 timing involved in the power down flow (PROCPWRGD de-assertion to CLKOUT_BCLK turning OFF). Encodings (all min timings): 00: 10 us (default) 01: 100 us 10: 1 ms 11: 10 ms

5.3.8 Message to PMC (MTPMC)—Offset 20h

BIOS may need to program this register.

5.3.9 PCH Power Management Status (PCH_PM_STS2)—Offset 24h

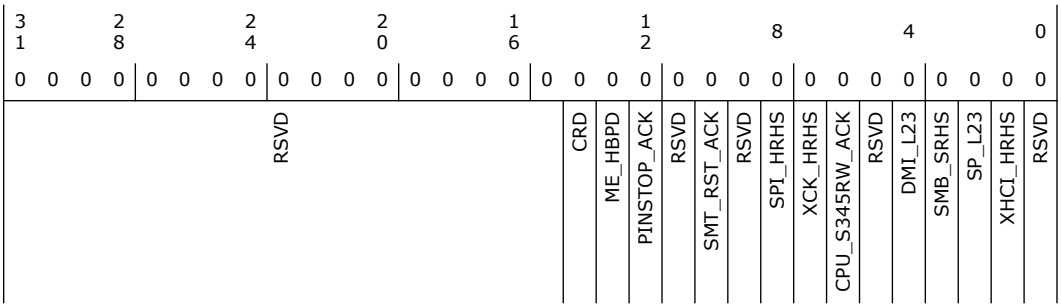
This register contains misc. fields used to record events pertaining to PCH power management. Unless otherwise indicated, all RWC bits are cleared with a write of '1' by software.

Access Method

Type: MEM Register (Size: 32 bits)

Device: 31
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RO	Reserved.
14	0h RW/1C/V	**CPU Reset Done Failure (CRD):** CPU Reset Done message did not arrive from the CPU.
13	0h RW/1C/V	**ME Host Boot Prep Done Failure (ME_HBPD):** ME Host Boot Preparation did not complete.
12	0h RW/1C/V	**PINSTOP Acknowledge Failure (PINSTOP_ACK):** The GbE PHY did not respond to the PINSTOP message.
11	0h RO	Reserved.
10	0h RW/1C/V	**SMT Reset Acknowledge Failure (SMT_RST_ACK):** One or more SMT controllers did not respond to the CSME bus reset warning.
9	0h RO	Reserved.
8	0h RW/1C/V	**SPI Common Prep Handshake Failure (SPI_HRHS):** The SPI controller did not complete the host partition reset/Sx entry handshake.
7	0h RW/1C/V	**XCK Common Prep Handshake Failure (XCK_HRHS):** The integrated clocking unit did not complete the host partition reset/ Sx entry handshake.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW/1C/V	**CPU S345/Reset Warn Acknowledge Failure (CPU_S345RW_ACK):** The CPU did not respond to the GO_S345 or RESET_WARN message.
5	0h RO	Reserved.
4	0h RW/1C/V	**DMI L23 Entry Failure (DMI_L23):** The DMI interface did not respond to the request to entry L23.
3	0h RW/1C/V	**SMBus Host Reset Handshaking Failure (SMB_SRHS):** The host SMBus controller did not complete the host partition reset handshake.
2	0h RW/1C/V	**South Port L23 Entry Failure (SP_L23):** The PCH PCI Express ports did not complete the host partition reset/Sx entry handshake.
1	0h RW/1C/V	**XHCI Common Prep Handshake Failure (XHCI_HRHS):** The XHCI controller did not complete the host partition reset/Sx entry handshake.
0	0h RO	Reserved.

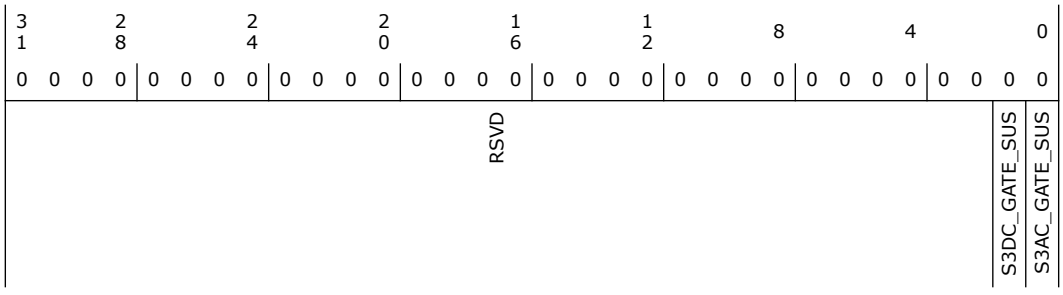
5.3.10 S3 Power Gating Policies (S3_PWRGATE_POL)—Offset 28h

This register contains policy bits to configure various power gating options while the system is in S3. Note that setting any of these policies to "enabled" may not directly result in power gating - in some cases other HW qualifications may be dynamically applied.
This register is in the RTC power well and is reset by RTCRST# assertion.

Access Method

Type: MEM Register (Size: 32 bits)
Device: 31
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1	0h RW	**S3 Power Gate Enable in DC Mode: SUS Well (S3DC_GATE_SUS):** A '1' in this bit enables power gating of the SUS well in S3 while operating on DC power (based on the AC_PRESENT pin value).
0	0h RW	**S3 Power Gate Enable in AC Mode: SUS Well (S3AC_GATE_SUS):** A '1' in this bit enables power gating of the SUS well in S3 while operating on AC power (based on the AC_PRESENT pin value).

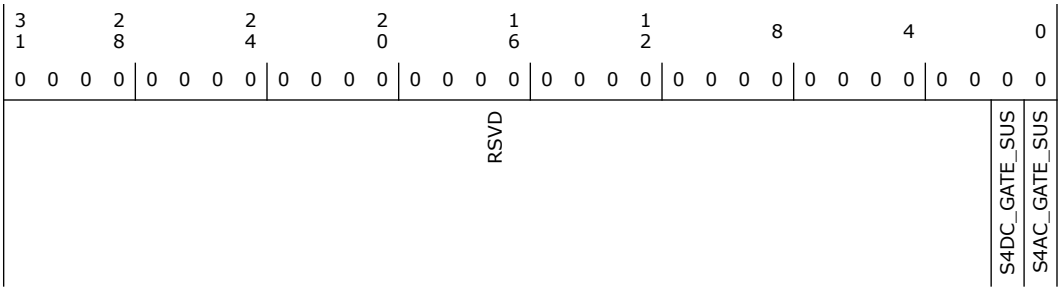
5.3.11 S4 Power Gating Policies (S4_PWRGATE_POL)—Offset 2Ch

This register contains policy bits to configure various power gating options while the system is in S4. Note that setting any of these policies to "enabled" may not directly result in power gating - in some cases other HW qualifications may be dynamically applied.
This register is in the RTC power well and is reset by RTCRST# assertion.

Access Method

Type: MEM Register (Size: 32 bits)
Device: 31
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1	0h RW	**S4 Power Gate Enable in DC Mode: SUS Well (S4DC_GATE_SUS):** A '1' in this bit enables power gating of the SUS well in S4 while operating on DC power (based on the AC_PRESENT pin value).
0	0h RW	**S4 Power Gate Enable in AC Mode: SUS Well (S4AC_GATE_SUS):** A '1' in this bit enables power gating of the SUS well in S4 while operating on AC power (based on the AC_PRESENT pin value).

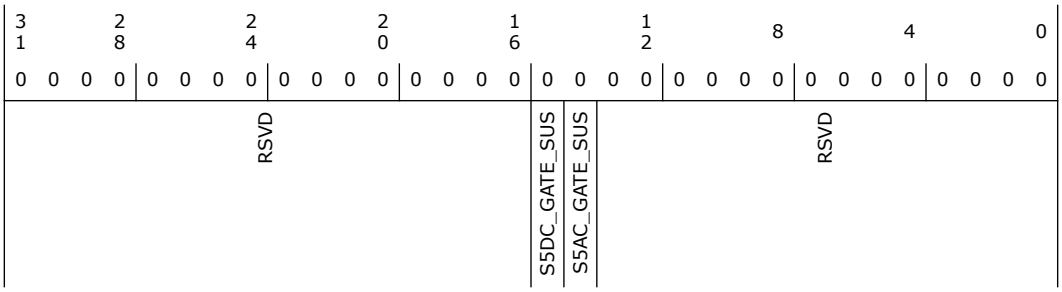
5.3.12 S5 Power Gating Policies (S5_PWRGATE_POL)—Offset 30h

This register contains policy bits to configure various power gating options while the system is in S5. Note that setting any of these policies to "enabled" may not directly result in power gating - in some cases other HW qualifications may be dynamically applied.
This register is in the RTC power well and is reset by RTCRST# assertion.

Access Method

Type: MEM Register (Size: 32 bits)
Device: 31
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	0h RW	**S5 Power Gate Enable in DC Mode: SUS Well (S5DC_GATE_SUS):** A '1' in this bit enables power gating of the SUS well in S5 while operating on DC power (based on the AC_PRESENT pin value).
14	0h RW	**S5 Power Gate Enable in AC Mode: SUS Well (S5AC_GATE_SUS):** A '1' in this bit enables power gating of the SUS well in S5 while operating on AC power (based on the AC_PRESENT pin value).
13:0	0h RO	Reserved.

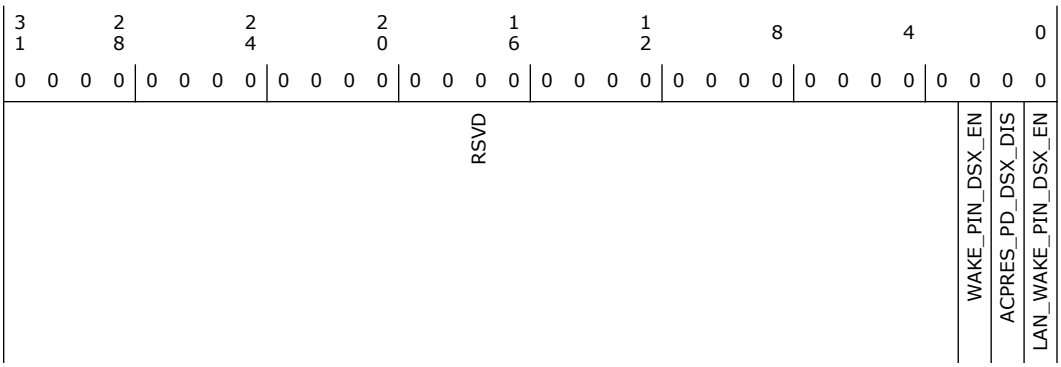
5.3.13 DeepSx Configuration (DSX_CFG)—Offset 34h

This register contains misc. fields used to configure the PCH's power management behavior.
This register is in the RTC power well and is reset by RTCRST# assertion.

Access Method

Type: MEM Register (Size: 32 bits)
Device: 31
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**WAKE# Pin DeepSx Enable (WAKE_PIN_DSX_EN):** When this bit is 1, the PCI Express WAKE# pin is monitored while in Deep Sx, supporting waking from Deep Sx due to assertion of this pin. In this case, the platform must externally pull up the pin to the DSW (instead of pulling up to the SUS as has historically been the case). When this bit is 0: - DeepSx enabled configurations: The PCH internal pull-down on the WAKE# pin is enabled in Deep Sx and during G3 exit and the pin is not monitored during this time. -Deep Sx disabled configurations: The PCH internal pull-down on the WAKE# pin is never enabled Note: Deep Sx disabled configurations must leave this bit at 0.
1	0h RW	**AC_PRESENT Pin Pulldown in DeepSx Disable (ACPRES_PD_DSX_DIS):** When this bit is 1, the internal pull-down on the ACPRESENT pin is disabled. However, the pulldown is not necessarily enabled if the bit is '0'. This bit must be left at '0' for Deep Sx disabled configurations, and the pulldown is disabled for those configurations even though the bit is '0'. To support ME wakes from Deep Sx, the pin is always monitored regardless of the value of this host policy bit. When this bit is '0': DeepSx enabled configurations: The PCH internal pull-down on ACPRESENT is enabled in Deep Sx and during G3 exit. Deep Sx disabled configurations: The PCH internal pull-down on ACPRESENT is always disabled.
0	0h RW	**LAN_WAKE# Pin DeepSx Enable (LAN_WAKE_PIN_DSX_EN):** When this bit is 1, the LAN_WAKE# pin is monitored while in DeepSx, supporting waking from DeepSx due to assertion of this pin. In this case, the platform must drive the pin to the correct value while in DeepSx. DeepSx disabled configurations must leave this bit at 0. When this bit is 0: DeepSx enabled configurations: The PCH internal pull-down on LAN_WAKE# pin is enabled in deep-Sx and during G3 exit and the pin is not monitored during this time. DeepSx disabled configurations: The PCH internal pull-down is never enabled

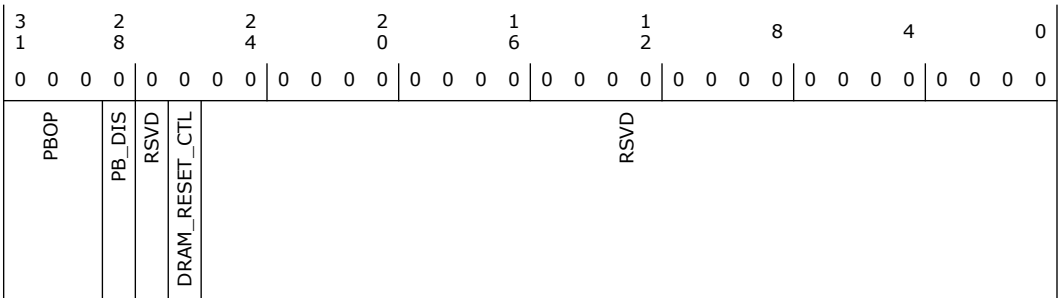
5.3.14 Power Management Configuration Reg 2 (PM_CFG2)—Offset 3Ch

Access Method

Type: MEM Register (Size: 32 bits)

Device: 31
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RW	**Power Button Override Period (PBOP):** This field determines, while the power button remains asserted, how long the PMC will wait before initiating a global reset. Encoding: 000b - 4 seconds 001b - 6 seconds 010b - 8 seconds 011b - 10 seconds 100b - 12 seconds 101b - 14 seconds Others - Reserved This bit is reset by DSW_PWROK de-assertion.
28	0h RW/L	**Power Button Native Mode Disable (PB_DIS):** When this bit is '0' (default), the PMC's power button logic will act upon the input value from the GPIO unit, as normal. When this bit is set to '1', the PMC must force its internal version of the power button pin to '1'. This will result in the PMC logic constantly seeing the pin as de-asserted. This bit is reset by RTCRST# assertion.
27	0h RO	Reserved.
26	0h RW/V	**DRAM_RESET# Control (DRAM_RESET_CTL):** BIOS uses this bit to control the DRAM_RESET# pin from the PCH, which is routed to the reset pin on the DRAM. Encoding: 0 = DRAM_RESET# output is asserted (driven low) 1 = DRAM_RESET# output is tri-stated. Note: This bit is cleared to '0' by HW when SLP_S4# goes low. This bit is reset by DSW_PWROK de-assertion.
25:0	0h RO	Reserved.

5.3.15 Chipset Initialization Register 40 (CIR40)—Offset 40h

BIOS may program this register.

5.3.16 Chipset Initialization Register 44 (CIR44)—Offset 44h

BIOS may program this register.

5.3.17 Chipset Initialization Register 48 (CIR48)—Offset 48h

BIOS may program this register.

5.3.18 Chipset Initialization Register 4C (CIR4C)—Offset 4Ch

BIOS may program this register.

5.3.19 Chipset Initialization Register 50 (CIR50)—Offset 50h

BIOS may program this register.

5.3.20 Chipset Initialization Register 54 (CIR54)—Offset 54h

BIOS may program this register.

5.3.21 Chipset Initialization Register 58 (CIR58)—Offset 58h

BIOS may program this register.

5.3.22 Chipset Initialization Register 60 (CIR60)—Offset 60h

BIOS may program this register.

5.3.23 Chipset Initialziation Register 68 (CIR68)—Offset 68h

BIOS may program this register.

5.3.24 Chipset Initialization Register 78 (CIR78)—Offset 78h

BIOS may program this register.

5.3.25 Chipset Initialization Register 7C (CIR7C)—Offset 7Ch

BIOS may program this register.

5.3.26 Chipset Initialization Register 80 (CIR80)—Offset 80h

BIOS may program this register.

5.3.27 Chipset Initialization Register 84 (CIR84)—Offset 84h

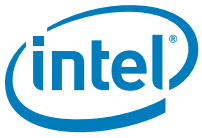
BIOS may program this register.

5.3.28 Chipset Initialization Register 88 (CIR88)—Offset 88h

BIOS may program this register.

5.3.29 Chipset Initialization Register 8C (CIR8C)—Offset 8Ch

BIOS may program this register.



5.3.30 Chipset Initialization Register 90 (CIR90)—Offset 90h

BIOS may program this register.

5.3.31 Chipset Initialization Register 98 (CIR98)—Offset 98h

BIOS may program this register.

5.3.32 Chipset Initialization Register A0 (CIRA0)—Offset A0h

BIOS may program this register.

5.3.33 Chipset Initialization Register A4 (CIRA4)—Offset A4h

BIOS may program this register.

5.3.34 Chipset Initizaliation Register A8 (CIRA8)—Offset A8h

BIOS may program this register.

5.3.35 Chipset Initizaliation Register AC (CIRAC)—Offset ACh

BIOS may program this register.

5.3.36 Chipset Initialization Register B0 (CIRB0)—Offset B0h

BIOS may program this register.

5.3.37 Chipset Initialization Register B4 (CIRB4)—Offset B4h

BIOS may program this register.

5.3.38 Chipset Initialization Register C0 (CIRC0)—Offset C0h

BIOS may program this register.

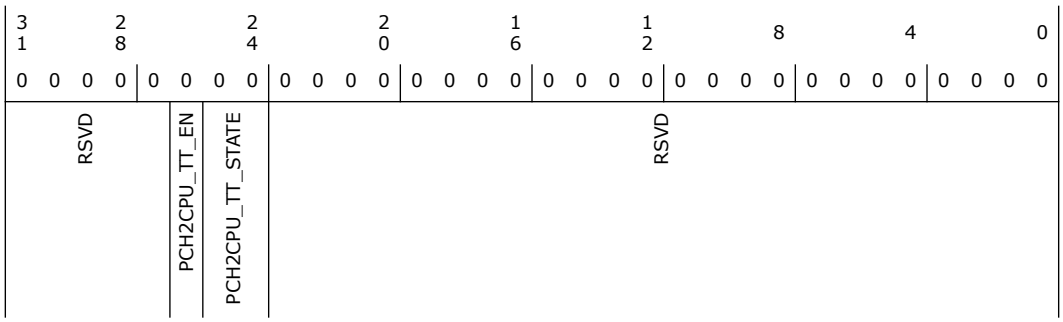
5.3.39 PMSYNC Thermal Power Reporting Configuration (PMSYNC_TPR_CFG)—Offset C4h

This register contains configuration bits that apply to PCH reporting of thermal and power status to the Processor.
Power Well: Primary.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** 31 **Function:** 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	Reserved.
26	0h RW/L	**PCH-to-CPU Thermal Throttle Enable (PCH2CPU_TT_EN):** When this bit is set to '1' the PCH is enabled to set the thermal throttle request to the PROC using the PMSYNC PCH_THERM_STATUS bit. When this bit is '0', the PCH-to-CPU Thermal Throttling request is disabled.
25:24	0h RW/L	**PCH-to-CPU Thermal Throttle State (PCH2CPU_TT_STATE):** This field specifies the PCH T-State level at which the PMC asserts the Thermal Throttle (PCH_THERM_STATUS) bit to the PROC. The PMC requests thermal throttling when the T-State, which is reported from the Thermal Sensor cluster, is greater than or equal to this state. Note: Refer to BIOS specification on the supported setting.
23:0	0h RO	Reserved.

5.3.40 PM_SYNC Miscellaneous Configuration (PM_SYNC_MISC_CFG)—Offset C8h

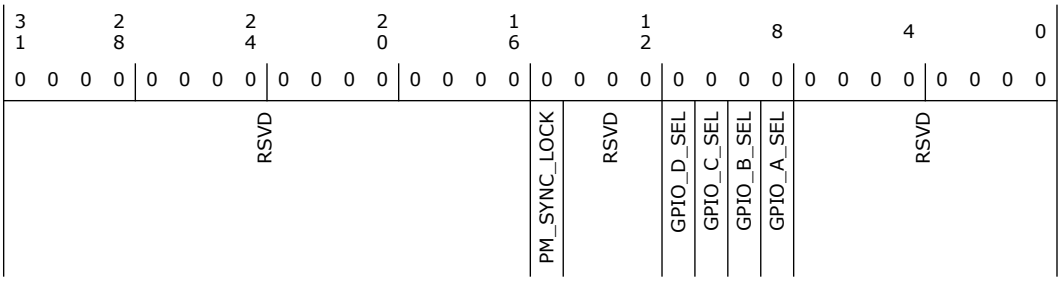
This register is used to configure miscellaneous aspects of the PM_SYNC pin. This register is in the CORE power well and is reset by PLTRST#.

Access Method

Type: MEM Register (Size: 32 bits)

Device: 31
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	0h RW/L	**PM_SYNC Configuration Lock (PM_SYNC_LOCK):** The bit is used to lock down the settings of several PM_SYNC-related configuration bits. This bit is self-locking (i.e. once written to '1', it can only be cleared by PLTRST#).
14:12	0h RO	Reserved.
11	0h RW/L	**GPIO_D Pin Selection (GPIO_D_SEL):** There are two possible GPIOs that can be routed to the GPIO_D PM_SYNC state. This bit selects between them: 0: CPU_GP_3 (default) 1: CPU_GP_2 This field is not writeable when PM_SYNC_LOCK=1.
10	0h RW/L	**GPIO_C Pin Selection (GPIO_C_SEL):** There are two possible GPIOs that can be routed to the GPIO_C PM_SYNC state. This bit selects between them: 0: CPU_GP_0 (default) 1: CPU_GP_1 This field is not writeable when PM_SYNC_LOCK=1.
9	0h RW/L	**GPIO_B Pin Selection (GPIO_B_SEL):** There are two possible GPIOs that can be routed to the GPIO_B PM_SYNC state. This bit selects between them: 0: CPU_GP_2 (default) 1: CPU_GP_0 This field is not writeable when PM_SYNC_LOCK=1.
8	0h RW/L	**GPIO_A Pin Selection (GPIO_A_SEL):** There are two possible GPIOs that can be routed to the GPIO_A PM_SYNC state. This bit selects between them: 0: CPU_GP_1 (default) 1: CPU_GP_3 This field is not writeable when PM_SYNC_LOCK=1.
7:0	0h RO	Reserved.

5.3.41 Chipset Initialization Register D0 (CIRD0)—Offset D0h

BIOS may program this register.

5.3.42 Chipset Initialization Register D4 (CIRD4)—Offset D4h

BIOS may program this register.

5.3.43 Chipset Initialization Register DC (CIRDC)—Offset DCh

BIOS may program this register.

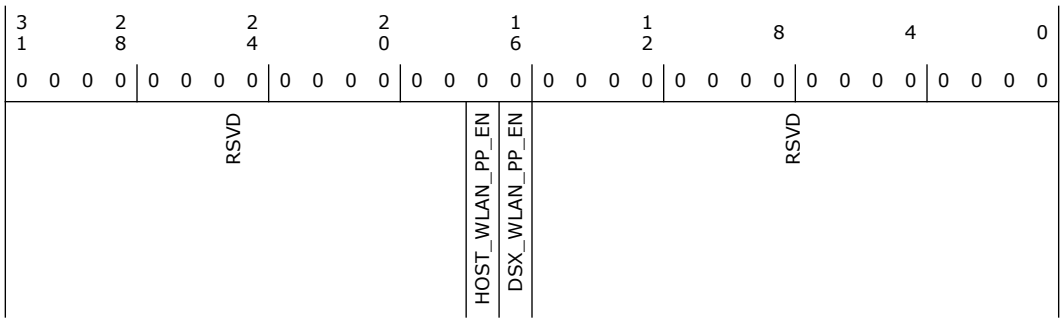
5.3.44 Chipset Initialization Register E0 (CIRE0)—Offset E0h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17	0h RW	**Host Wireless LAN Phy Power Enable (HOST_WLAN_PP_EN):** This policy bit is set by Host software when it desires the wireless LAN PHY to be powered in Sx power states for wakes over wireless LAN (WoWLAN). This bit is reset by DSW_PWROK de-assertion.
16	0h RW	**Deep Sx WLAN Phy Power Enable (DSX_WLAN_PP_EN):** When set to '1, PMC will keep SLP_WLAN# high in deep-Sx to enable WoWLAN. Note: 1. This policy bit will be applied for Deep Sx entry from S3, S4 and S5. 2. This bit does not affect SLP_WLAN# behaviour in Sx after G3 or after a global reset 3. HOST_WLAN_PP_EN must be set when this bit is set. This bit is reset by DSW_PWROK de-assertion.
15:0	0h RO	Reserved.

5.3.45 Chipset Initialization Register E4 (CIRE4)—Offset E4h

BIOS may program this register.

5.3.46 Chipset Initializatin Register E8 (CIRE8)—Offset E8h

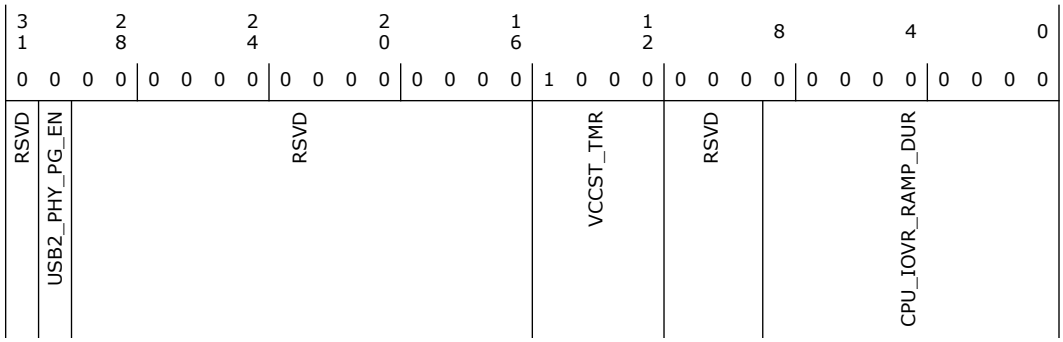
BIOS may program this register.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 2

Default: 8000h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	Reserved.
30	0h RW	**USB2 PHY SUS Well Power Gating Enable (USB2_PHY_PG_EN):** If this bit is '1', dynamic power gating of the USB2 PHY SUS well is enabled. If this bit is '0', it prevents HW from initiating power gating entry. Note: the USB2 PHY SUS well is power gated by default while in Sx after global_rst_b assertion. So HW will not spontaneously exit power gating while in Sx just because this bit is 0.
29:16	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
15:12	8h RW	**VccST Ramp Timer (VCCST_TMR):** This field determines the time from when SLP_S0# de-asserts until the CPU's VccST gated rail has ramped back up after being gated in C10. This timer starts when SLP_S0# asserts and has the effect of delaying any transactions on PM_SYNC until it expires. Encoding: 0h: 0us(disabled) 1h: 30us 2h: 35us 3h: 40us ... Fh: 100us Note: If the VccST bit in the CPU shutdown overrides virtual register is set to '1', the VccST gated domain will never be shut down (SLP_S0# will remain at '1' in C10). And so this timer will never start, allowing the PMC to send PM_SYNC traffic without waiting for this timer during C10 exit. This field is reset by PLTRST# assertion.
11:9	0h RO	Reserved.
8:0	0h RW	**CPU I/O VR Ramp Duration (CPU_IOVR_RAMP_DUR):** This value is used in the CPU I/O VR ramp timer and has a 10us granularity. Encoding: 000h: reserved 001h: 10us 002h: 20us 003h: 30us ... 1FFh: 5.1ms This field is reset by PLTRST# assertion.

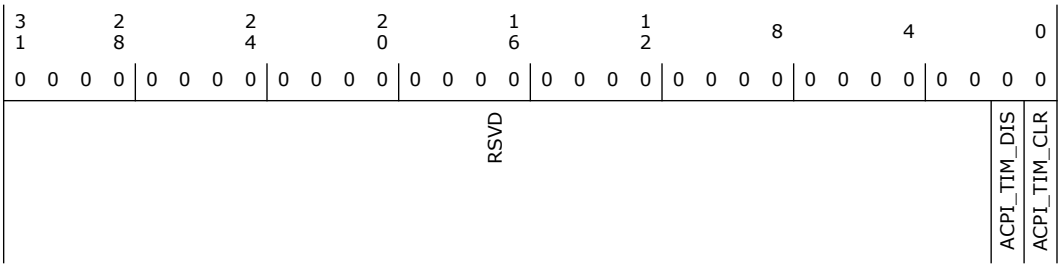
5.3.47 ACPI Timer Control (ACPI_TMR_CTL)—Offset FCh

This register allows software to disable the ACPI Timer, which could result in power savings for the PCH.
This register is in the CORE power well and is reset by PLTRST#

Access Method

Type: MEM Register (Size: 32 bits)
Device: 31
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1	0h RW	**ACPI Timer Disable (ACPI_TIM_DIS):** This bit determines whether the ACPI Timer is enabled to run. - 0: ACPI Timer is enabled (default) - 1: ACPI Timer is disabled (halted at the current value) Even when enabled, the timer only runs during S0. This bit must only be set to "1" if the operating system can tolerate disabling the 14.31818 MHz ACPI PM Timer. Note: 1.Some operating systems may only tolerate disabling the timer during entry into deep idle states. In such cases, the bit must be set to "1" during entry into those states and cleared to "0" during exit. This bit is reset by PLTRST# assertion.
0	0h RW/1S/V	**ACPI Timer Clear (ACPI_TIM_CLR):** Writing a 1 to this bit will clear the ACPI Timer to all 0s. Hardware will automatically clear the bit back to 0 once the timer clear operation has completed. Writing a 0 to this bit has no effect. Implementation Note: The PCH must be capable of honoring this bit even while ACPI_TIM_DIS=1. This bit is reset by PLTRST# assertion.

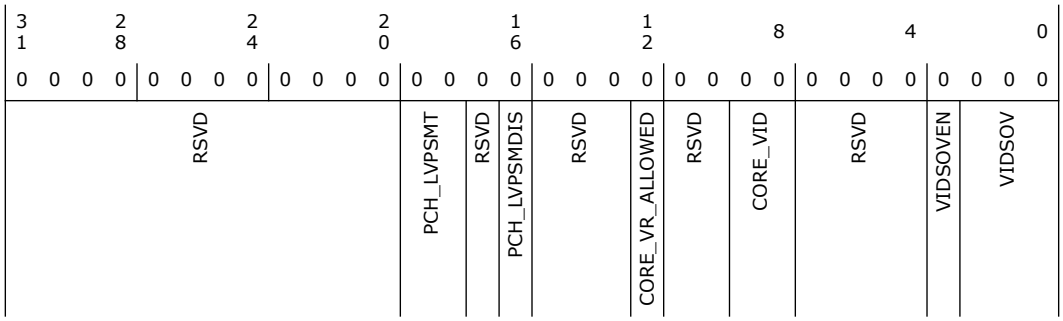
5.3.48 VR Miscellaneous Control (VR_MISC_CTL)—Offset 100h

This register allows software to program various VR modes for the PCH. This register is in the PRIMARY power well and is reset by RSMRST# assertion.

Access Method

Type: MEM Register (Size: 32 bits)
Device: 31
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	Reserved.
19:18	0h RO/V	**PCH Low Voltage Power Save Mode Target (PCH_LVPSMT):** These bits reflect the supported voltage for PCH Low Voltage Power Save Mode Target. The PCH LVPSM allows PCH 1.0 V rails to be lowered during Connected Standby, SLP_S0 assertion. 11 PCH Low Voltage Power Save Mode capability is Disabled 10 0.80V 01 0.75V 00 0.7V
17	0h RO	Reserved.
16	0h RO/V	**PCH Low Voltage Power Save Mode Disable (PCH_LVPSMDIS):** This bit reflects whether PCH Low Voltage Power Save Mode is disabled: 0=PCH Low Voltage Power Save Mode is Enabled 1=PCH Low Voltage Power Save Mode is Disabled.
15:13	0h RO	Reserved.
12	0h RO/V	**CORE VR Allowed (CORE_VR_ALLOWED):** This field reports the Separate Core VR support for VCCPRIM_CORE. 0 = PCH does not support a separate core VR for VCCPRIM_CORE. CORE_VID1 and CORE_VID0 signals are invalid. 1 = PCH supports a separate core VR, VCCPRIM_CORE, programmed to the voltage output as described by the CORE_VID field. This bit is reset by RSMRST# assertion.
11:10	0h RO	Reserved.
9:8	0h RO/V	**CORE Voltage ID (CORE_VID):** This field reports the supported core voltage ID 00 = 0.85V 01 = 0.90V 10 = 0.95V 11 = 1.0V (Default) These bits are only valid when CORE_VR_ALLOWED bit is 1. This field is reset by RSMRST# assertion.

Bit Range	Default & Access	Field Name (ID): Description
7:4	0h RO	Reserved.
3	0h RW	**VID status override enable (VIDSOVEN):** When set to 1 the bits in Primary VID Status Override (VIDSOV) are valid. This bit is reset by RSMRST# assertion.
2:0	0h RW	**Primary VID status override (VIDSOV):** SW can program this register to reflect the actual voltage of the core power rail, VCCPRIM_CORE, if the system is not using the PCH VID control mechanism, CORE_VID1 and CORE_VID0. The accurate voltage is required for PCH power reporting. 000: 1.0V 001: 0.95V 010: 0.90V 011: 0.85V 100-111: Reserved The value in these bits is only used by PCH HW/FW when bit 3 of this register is set. This field is reset by RSMRST# assertion.

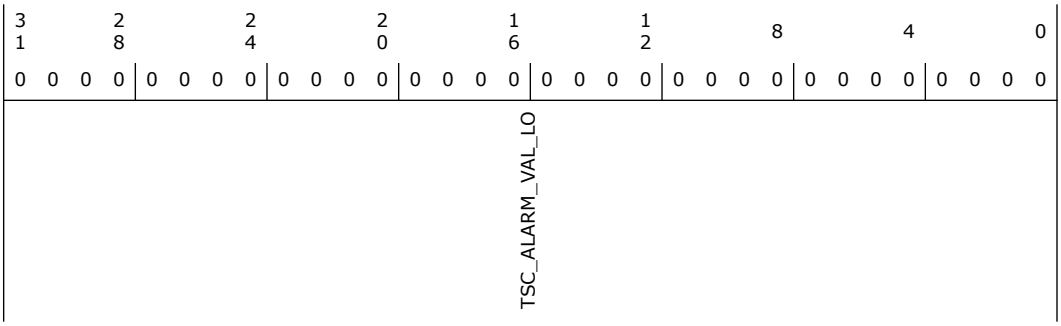
5.3.49 Last TSC Alarm Value[31:0] (TSC_ALARM_LO)—Offset 110h

Access Method

Type: MEM Register (Size: 32 bits)

Device: 31
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Last TSC Alarm Value [31:0] (TSC_ALARM_VAL_LO):** This field contains bits 31:0 of the last TSC alarm value received from the CPU. This field is reset by PLTRST# assertion.

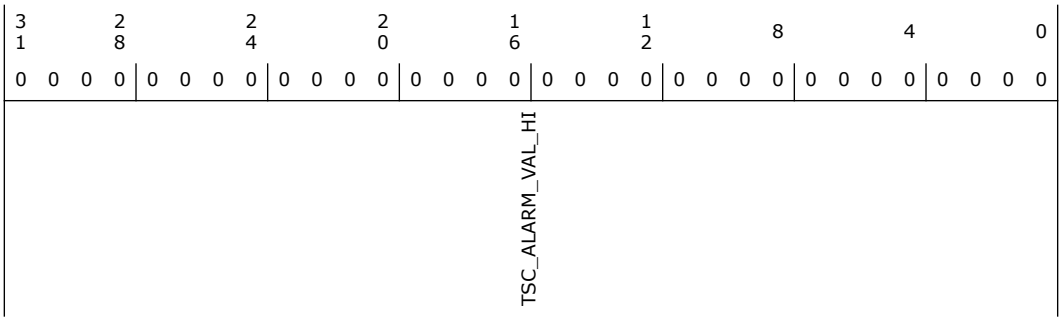
5.3.50 Last TSC Alarm Value[63:32] (TSC_ALARM_HI)—Offset 114h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Last TSC Alarm Value [63:32] (TSC_ALARM_VAL_HI):** This field contains bits 63:32 of the last TSC alarm value received from the CPU. This field is reset by PLTRST# assertion.

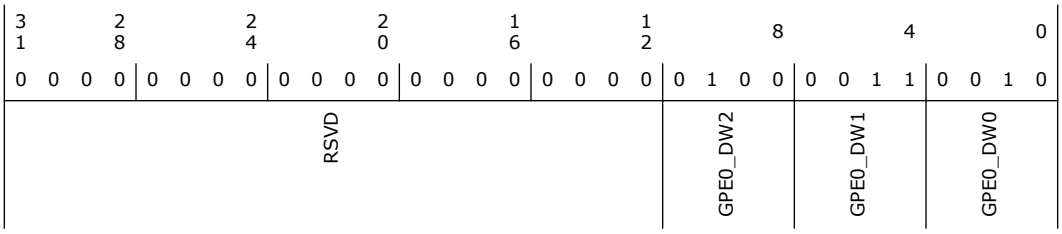
5.3.51 GPIO Configuration (GPIO_CFG)—Offset 120h

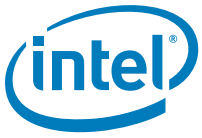
Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 2

Default: 432h





Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	Reserved.
11:8	4h RW	**GPIO Group to GPE_DW2 assignment encoding (GPE0_DW2):** This register assigns a specific GPIO Group to the ACPI GPE0[95:64]. The selected GPIO group will be mapped to lower bits of the GPE register 0h = GPP_A[23:0] mapped to GPE[87:64]; GPE[95:88] not used. 1h = GPP_B[23:0] mapped to GPE[87:64]; GPE[95:88] not used. 2h = GPP_C[23:0] mapped to GPE[87:64]; GPE[95:88] not used. 3h = GPP_D[23:0] mapped to GPE[87:64]; GPE[95:88] not used. 4h = GPP_E[23:0] mapped to GPE[87:64]; GPE[95:88] not used. 5h = GPP_F[23:0] mapped to GPE[87:64]; GPE[95:88] not used. 6h = GPP_G[7:0] mapped to GPE[51:64]; GPE[95:52] not used. 7h = GPD[11:0] mapped to GPE[75:64]; GPE[95:76] not used.
7:4	3h RW	**GPIO Group to GPE_DW1 assignment encoding (GPE0_DW1):** This register assigns a specific GPIO Group to the ACPI GPE0[63:32]. The selected GPIO group will be mapped to lower bits of the GPE register 0h = GPP_A[23:0] mapped to GPE[55:32]; GPE[63:56] not used. 1h = GPP_B[23:0] mapped to GPE[55:32]; GPE[63:56] not used. 2h = GPP_C[23:0] mapped to GPE[55:32]; GPE[63:56] not used. 3h = GPP_D[23:0] mapped to GPE[55:32]; GPE[63:56] not used. 4h = GPP_E[23:0] mapped to GPE[55:32]; GPE[63:56] not used. 5h = GPP_F[23:0] mapped to GPE[55:32]; GPE[63:56] not used. 6h = GPP_G[7:0] mapped to GPE[39:32]; GPE[63:40] not used. 7h = GPD[11:0] mapped to GPE[43:32]; GPE[63:44] not used.
3:0	2h RW	**GPIO Group to GPE_DW0 assignment encoding (GPE0_DW0):** This register assigns a specific GPIO Group to the ACPI GPE0[31:0]. The selected GPIO group will be mapped to lower bits of the GPE register 0h = GPP_A[23:0] mapped to GPE[23:0]; GPE[31:24] not used. 1h = GPP_B[23:0] mapped to GPE[23:0]; GPE[31:24] not used. 2h = GPP_C[23:0] mapped to GPE[23:0]; GPE[31:24] not used. 3h = GPP_D[23:0] mapped to GPE[23:0]; GPE[31:24] not used. 4h = GPP_E[23:0] mapped to GPE[23:0]; GPE[31:24] not used. 5h = GPP_F[23:0] mapped to GPE[23:0]; GPE[31:24] not used. 6h = GPP_G[7:0] mapped to GPE[7:0]; GPE[31:8] not used. 7h = GPD[11:0] mapped to GPE[11:0]; GPE[31:12] not used.

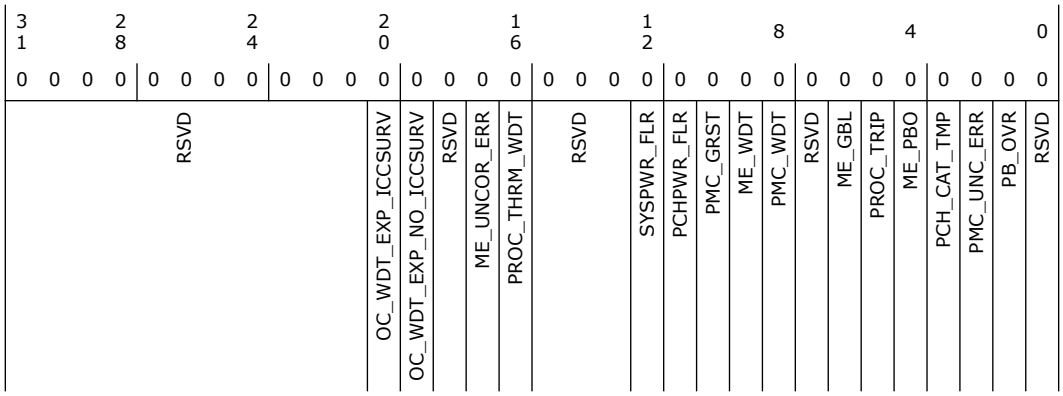
5.3.52 Global Reset Causes (GBLRST_CAUSE0)—Offset 124h

This register logs causes of host partition resets.

Access Method

Type: MEM Register (Size: 32 bits)
Device: 31
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved (RSVD)**
20	0h RW/1C/V	**Over-Clocking WDT Expiration In ICC Survivability Mode (OC_WDT_EXP_ICCSURV):** This bit is set to 1 by hardware when a global reset is triggered by the expiration of the over-clocking watchdog timer while running in a mode that has ICC survivability impact (OC_WDT_ICCSURV=1). This bit is reset by DSW_PWROK de-assertion.
19	0h RW/1C/V	**Over-Clocking WDT Expiration In Non-ICC Survivability Mode (OC_WDT_EXP_NO_ICCSURV):** This bit is set to 1 by hardware when a global reset is triggered by the expiration of the over-clocking watchdog timer while running in a mode that does not have ICC survivability impact (OC_WDT_ICCSURV=0). This bit is reset by DSW_PWROK de-assertion.
18	0h RO	Reserved.
17	0h RW/1C/V	**Intel ME HW Uncorrectable Error (ME_UNCOR_ERR):** This bit is set to '1' by hardware when a global reset is triggered by Intel ME hardware due to the detection of an uncorrectable ECC or parity error on a data read from one of its SRAMs. This bit is reset by DSW_PWROK de-assertion.
16	0h RW/1C/V	**Processor Thermal Runaway Watchdog Timer (PROC_THRM_WDT):** This bit is set to '1' by hardware when a global reset is triggered by the expiration of the Processor Thermal Runaway Watchdog Timer. This bit is reset by DSW_PWROK de-assertion.
15:13	0h RO	Reserved.
12	0h RW/1C/V	**SYS_PWROK Failure (SYSPWR_FLR):** This bit is set to '1' by hardware when a global reset is triggered by an unexpected loss of SYS_PWROK. This bit is reset by DSW_PWROK de-assertion.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW/1C/V	**PCH_PWROK Failure (PCHPWR_FLR):** This bit is set to '1' by hardware when a global reset is triggered by an unexpected loss of PCH_PWROK. This bit is reset by DSW_PWROK de-assertion.
10	0h RW/1C/V	**Power Management Controller Global Reset (PMC_GRST):** This bit is set to '1' by hardware when a global reset is triggered by a request from power management controller. This bit is reset by DSW_PWROK de-assertion.
9	0h RW/1C/V	**Intel Management Engine Watchdog Timer (ME_WDT):** This bit is set to '1' by hardware when a global reset is triggered by the second expiration of the Intel® Management Engine watchdog timer. This bit is reset by DSW_PWROK de-assertion.
8	0h RW/1C/V	**Power Management Controller Watchdog Timer (PMC_WDT):** This bit is set to '1' by hardware when a global reset is triggered by the second expiration of the PMC watchdog timer. This bit is reset by DSW_PWROK de-assertion.
7	0h RO	Reserved.
6	0h RW/1C/V	**ME-Initiated Global Reset (ME_GBL):** This bit is set to '1' by hardware when a global reset is triggered by Intel ME FW. This bit is reset by DSW_PWROK de-assertion.
5	0h RW/1C/V	**Processor Thermal Trip (PROC_TRIP):** This bit is set to '1' by hardware when a global reset is triggered by a processor thermal trip event (i.e. an assertion of the THRMTRIP# pin). This bit is reset by DSW_PWROK de-assertion.
4	0h RW/1C/V	**ME-Initiated Power Button Override (ME_PBO):** This bit is set to '1' by hardware when a global reset is triggered by ME-Initiated Power Button Override. This bit is reset by DSW_PWROK de-assertion.
3	0h RW/1C/V	**PCH Catastrophic Temperature Event (PCH_CAT_TMP):** This bit is set to '1 by hardware when a global reset is triggered by a catastrophic temperature event from the PCH internal thermal sensor. This bit is reset by DSW_PWROK de-assertion.
2	0h RW/1C/V	**PMC SUS RAM Uncorrectable Error (PMC_UNC_ERR):** This bit is set to '1' by hardware when a global reset is triggered due to an uncorrectable parity error on a data read from one of the PMC SUS well register files. This bit is reset by DSW_PWROK de-assertion.
1	0h RW/1C/V	**Power Button Override (PB_OVR):** This bit is set to '1' by hardware when a global reset is triggered by a power button override (i.e. an assertion of the PWRBTN# pin for 5 seconds). This bit is reset by DSW_PWROK de-assertion.
0	0h RO	Reserved.

5.3.53 Global Reset Causes Register 1 (GBLRST_CAUSE1)—Offset 128h

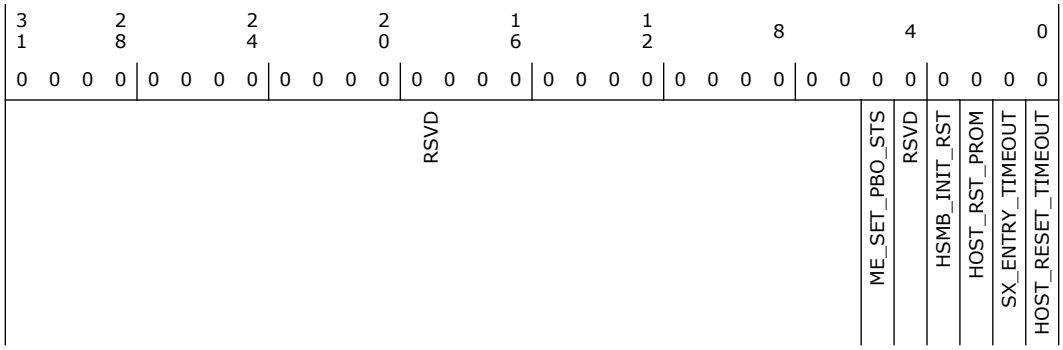
This register logs causes of host partition resets.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	Reserved.
5	0h RW/1C/V	**ME Set Power Button Status (ME_SET_PBO_STS):** If this bit is set, the cause of the previous global reset was ME FW setting the power button override status. This bit is reset by DSW_PWROK de-assertion.
4	0h RO	Reserved.
3	0h RW/1C/V	**Host SMBus Initiated Reset (HSMB_INIT_RST):** If this bit is set, the cause of the previous global reset was a global reset request received over the host SMBus interface. This bit is reset by DSW_PWROK de-assertion.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1C/V	**Host Partition Reset Promotion (HOST_RST_PROM):** If this bit is set, the cause of the previous global reset was a host partition reset that was promoted to a global reset either due to ME or host policy. This bit is reset by DSW_PWROK de-assertion.
1	0h RW/1C/V	**Sx Entry Timeout (SX_ENTRY_TIMEOUT):** If this bit is set, the cause of the previous global reset was an expiration of the timer that runs during Sx entry. This bit is reset by DSW_PWROK de-assertion.
0	0h RW/1C/V	**Host Partition Reset Timeout (HOST_RESET_TIMEOUT):** If this bit is set, the cause of the previous global reset was an expiration of the timer that runs during host partition resets. This bit is reset by DSW_PWROK de-assertion.

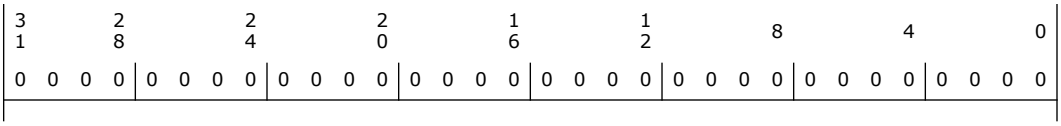
5.3.54 SLP S0 RESIDENCY (SLP_S0_RES)—Offset 13Ch

Access Method

Type: MEM Register (Size: 32 bits)

Device: 31
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Residency In S0:** This field contains the amount of time that the SLP_S0 has been asserted before. Note that this counter can wrap and that should not be of any concern. It will also count in 100us granularity. This field is reset by PLTRST# assertion.

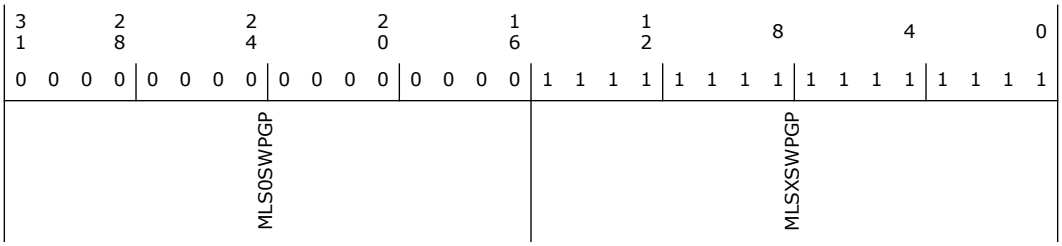
5.3.55 ModPhy Power Management Configuration 1 (MODPHY_PM_CFG1)—Offset 200h

Access Method

Type: MEM Register (Size: 32 bits)

Device: 31
Function: 2

Default: FFFFh



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**MODPHY Lane S0 SUS Well Power Gating Policy [15:0] (MLS0SWPGP):** This is a bit per lane that controls SUS Well Power Gating for a ModPHY lane to be used for S0 and S0ix use models. Bit 0: Corresponds to ModPHY Lane 0 Bit 1: Corresponds to ModPHY Lane 1 Bit 2: Corresponds to ModPHY Lane 2 : : Bit 15: Corresponds to ModPHY Lane 15 For each lane: 0: Lane power gating not permitted in S0. 1: Lane power gating is permitted in S0. Note that strap information/PCIe Lane reversal information will be factored by BIOS when programming these bits in the configuration registers. Note that it is illegal SW programming to have a bit location to be 1 in this field and the corresponding bit position to be 0 in MLSXSWPGP
15:0	FFFFh RW	**MODPHY Lane Sx SUS Well Power Gating Policy [15:0] (MLSXSWPGP):** This is a bit per lane that controls SUS Well Power Gating for a ModPHY lane when system is in Sx. Bit 0: Corresponds to ModPHY Lane 0 Bit 1: Corresponds to ModPHY Lane 1 Bit 2: Corresponds to ModPHY Lane 2 : : Bit 15: Corresponds to ModPHY Lane 15 For each lane: 0: Lane power gating not permitted in Sx. 1: Lane power gating is permitted in Sx. Note that strap information/PCIe Lane reversal information will be factored by BIOS when programming these bits in the configuration registers. For ease of PMC implementation, this field will be used to manage Sx policies even in S0. In other words, the earlier restriction that BIOS does not have to program this field if MLSPDDGE is 1 does not apply any more. BIOS shall set this field appropriately for all cases.

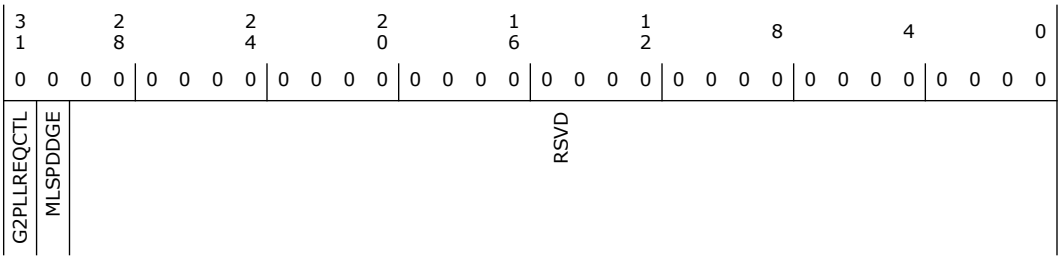
5.3.56 MODPHY Power Management Configuration 2 (MODPHY_PM_CFG2)—Offset 204h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Gen2PLL Request Control (G2PLLREQCTL):** This bit controls how PMC should treat Gen2PLL power request for ModPHY power gating flows. 0 = PMC should treat Gen2PLL request as non restore power request 1 = PMC should treat Gen2PLL request as restore power request
30	0h RW	**MODPHY Lane SUS Power Domain Dynamic Gating Enable (MLSPDDGE):** When this bit is set to 1, MODPHY Lane SUS Well Dynamic Gating is enabled. When this bit is 0, MODPHY Lane SUS Well Gating can still be done at a more coarse level using MLSXSWPGP and MLS0SWPGP fields. This bit is reset by PLTRST# assertion.
29:0	0h RO	Reserved.

5.3.57 MODPHY Power Management Configuration 3 (MODPHY_PM_CFG3)—Offset 208h

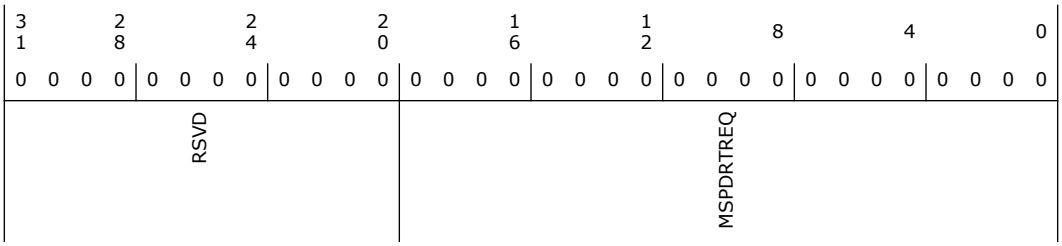
This register contains misc. fields used to configure the PCH's power management behavior with respect to the modPHY.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	Reserved.
19:0	0h RW	**Controller SPD RTD3 Request [19:0] (MSPDRTREQ):** This field represents ASL code trigger request for ModPHY SPD gating. If this bit is set (to 1) for a controller, it implies that ASL code provides consent for SPD to be gated for the corresponding controller's lanes. ASL code will exist for all controllers that are enabled. However, the controllers that are not enabled (Function Disabled), this field will be statically set by BIOS to activate ASL component in SPD gating equations. Bit 0: Corresponds to PCIe Controller A, Function 0 Bit 1: Corresponds to PCIe Controller A, Function 1 Bit 2: Corresponds to PCIe Controller A, Function 2 Bit 3: Corresponds to PCIe Controller A, Function 3 Bit 4: Corresponds to PCIe Controller B, Function 0 Bit 5: Corresponds to PCIe Controller B, Function 1 Bit 6: Corresponds to PCIe Controller B, Function 2 Bit 7: Corresponds to PCIe Controller B, Function 3 Bit 8: Corresponds to PCIe Controller C, Function 0 Bit 9: Corresponds to PCIe Controller C, Function 1 Bit 10: Corresponds to PCIe Controller C, Function 2 Bit 11: Corresponds to PCIe Controller C, Function 3 Bit 12: Corresponds to SATA Controller Bit 13: Corresponds to Gbe Controller Bit 14: Corresponds to xHCI Controller Bit 15: Corresponds to xDCI Controller Bits[19:16]: Reserved This field is reset by PLTRST# assertion.

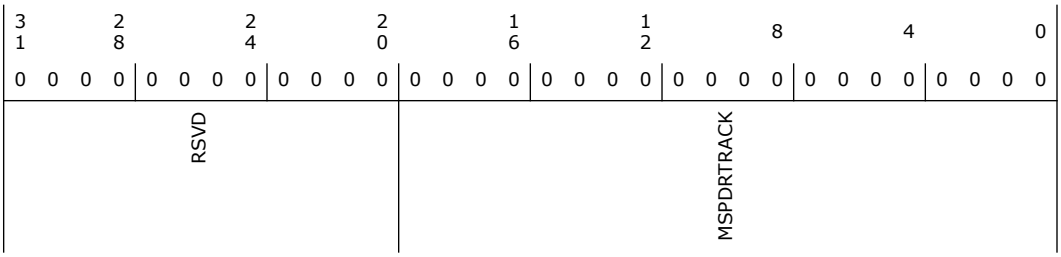
5.3.58 MODPHY Power Management Configuration 4 (MODPHY_PM_CFG4)—Offset 20Ch

Access Method

Type: MEM Register (Size: 32 bits)

Device: 31
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	Reserved.
19:0	0h RO/V	**Controller SPD RTD3 Request Acknowledge [19:0] (MSPDRTRACK):** This field represents the acknowledge for ASL code trigger request for ModPHY SPD gating. PMC sets a bit in this field to 1 to acknowledge that it has registered the corresponding MSPDRTREQ. Note that the action of setting this bit to 1 is immediate, no other gating conditions are involved in this. Actual SPD shutdown may happen later once other power gating conditions have been satisfied as well. PMC clears a bit to 0 in this field once the corresponding MSPTDRTREQ is cleared by the ASL code and SPD state has been fully restored. Bit 0: Corresponds to PCIe Controller A, Function 0 Bit 1: Corresponds to PCIe Controller A, Function 1 Bit 2: Corresponds to PCIe Controller A, Function 2 Bit 3: Corresponds to PCIe Controller A, Function 3 Bit 4: Corresponds to PCIe Controller B, Function 0 Bit 5: Corresponds to PCIe Controller B, Function 1 Bit 6: Corresponds to PCIe Controller B, Function 2 Bit 7: Corresponds to PCIe Controller B, Function 3 Bit 8: Corresponds to PCIe Controller C, Function 0 Bit 9: Corresponds to PCIe Controller C, Function 1 Bit 10: Corresponds to PCIe Controller C, Function 2 Bit 11: Corresponds to PCIe Controller C, Function 3 Bit 12: Corresponds to SATA Controller Bit 13: Corresponds to Gbe Controller Bit 14: Corresponds to xHCI Controller Bit 15: Corresponds to xDCI Controller Bits[19:16]: Reserved This field is reset by PLTRST# assertion.

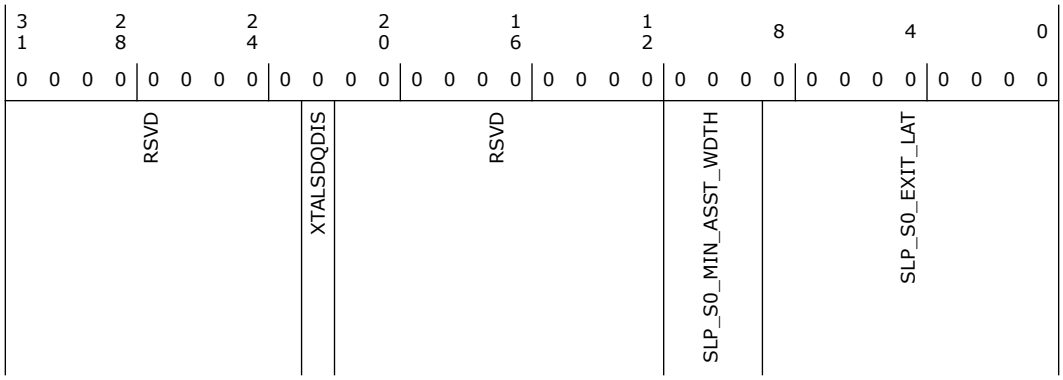
5.3.59 Chipset Initialization Register 31C (CIR31C)—Offset 31Ch

Access Method

Type: MEM Register (Size: 32 bits)

Device: 31
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	Reserved.
22	0h RW	**24MHz Crystal Shutdown Qualification Disable (XTALSDQDIS):** 0 = SLP_S0# assertion requires the 24MHz Crystal Oscillator to be shutdown. Once SLP_S0# is asserted, the Crystal oscillator should be kept off until PMC notifies it is allowed to be re-enabled. 1 = SLP_S0# assertion does not require the 24MHz Crystal to be shutdown.
21:12	0h RO	Reserved.
11:9	0h RW	**SLP_S0# Minimum Assertion Width (SLP_S0_MIN_ASST_WDTH):** 000 = 2us 001 = 4us 010 = 10us 011 = 26us 100 = 50us 101 = 100us 110 = 500us 111 = 1ms Implementation Note: These encodings are defined as even numbers in order to ease the HW operations that use them.
8:0	0h RW	**SLP_S0# De-assertion Exit Latency (SLP_S0_EXIT_LAT):** This value is used in the SLP_S0# exit timer and has a 10us granularity. 000h = 0us (reserved) 001h = 10us 002h = 20us 003h = 30us 1FFh = 5.1ms

5.3.60 Chipset Initialization Register 324 (CIR324)—Offset 324h

BIOS may program this register.

5.3.61 Chipset Initialization Register 328 (CIR328)—Offset 328h

BIOS may program this register.

5.3.62 Chipset Initialization Register 32C (CIR32C)—Offset 32Ch

BIOS may program this register.

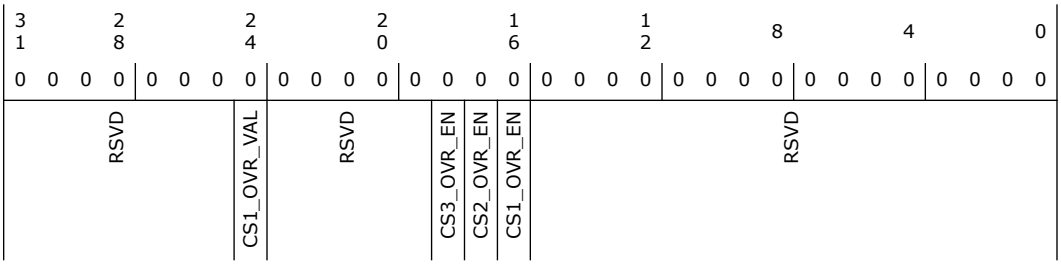
5.3.63 Clock Source Shutdown Control Reg 2 (CS_SD_CTL2)—Offset 3ECh

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	Reserved.
24	0h RW	**Clock Source 1 Override Value (CS1_OVR_VAL):** When CS1_OVR_EN = 1, CS1_OVR_VAL will be driven on the PLLOFFOK signal for clock source 1. Note: Clock source 1 maps to Gen2 PLL which is used to generate the IOSF primary clock.
23:19	0h RO	Reserved.
18	0h RW	**Clock Source 3 Override Enable (CS3_OVR_EN):** When CS2_OVR_EN = 1, CS2_OVR_VAL will be driven on the PLLOFFOK signal for clock source 3.
17	0h RW	**Clock Source 2 Override Enable (CS2_OVR_EN):** When CS2_OVR_EN = 1, CS2_OVR_VAL will be driven on the PLLOFFOK signal for clock source 2.
16	0h RW	**Clock Source 1 Override Enable (CS1_OVR_EN):** When CS1_OVR_EN = 1, CS1_OVR_VAL will be driven on the PLLOFFOK signal for clock source 1.
15:0	0h RO	Reserved.

5.3.64 PFET Enable Ack Register 0 (PPFEAR0)—Offset 590h

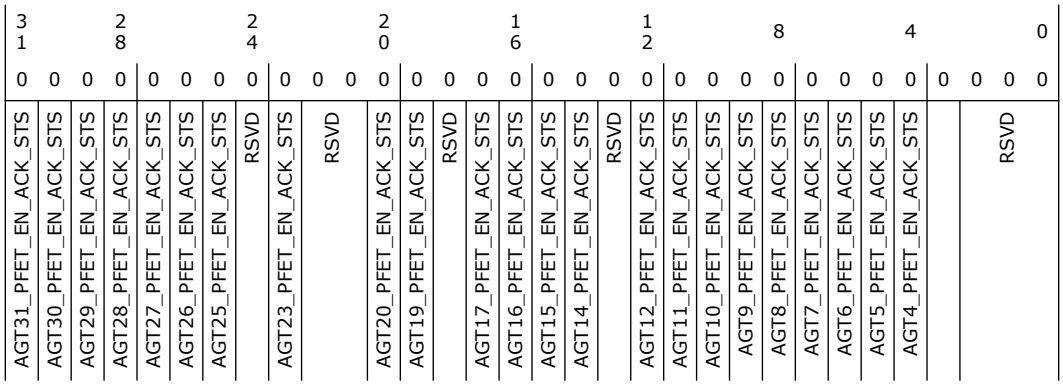
Intel(R) IP is power gated when the corresponding bit in PPFEAR0 or PPFEAR1 is set to 1

Access Method

Type: MEM Register (Size: 32 bits)

Device: 31
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**Intel(R) ME domain 5 PFET Enable Acknowledge Status (AGT31_PFET_EN_ACK_STS):** When AGT31_PFET_EN_ACK_STS = 1, Intel(R) ME domain 5 is power gated.
30	0h RO/V	**Intel(R) ME domain 4 PFET Enable Acknowledge Status (AGT30_PFET_EN_ACK_STS):** When AGT30_PFET_EN_ACK_STS = 1, Intel(R) ME domain 4 is power gated.
29	0h RO/V	**Intel(R) ME domain 3 PFET Enable Acknowledge Status (AGT29_PFET_EN_ACK_STS):** When AGT29_PFET_EN_ACK_STS = 1, Intel(R) ME domain 3 is power gated.
28	0h RO/V	**Intel(R) ME domain 2 PFET Enable Acknowledge Status (AGT28_PFET_EN_ACK_STS):** When AGT28_PFET_EN_ACK_STS = 1, Intel(R) ME domain 2 is power gated.
27	0h RO/V	**Intel(R) ME domain 1 PFET Enable Acknowledge Status (AGT27_PFET_EN_ACK_STS):** When AGT27_PFET_EN_ACK_STS = 1, Intel(R) ME domain 1 is power gated.
26	0h RO/V	**DCI PFET Enable Acknowledge Status (AGT26_PFET_EN_ACK_STS):** When AGT26_PFET_EN_ACK_STS = 1, DCI is power gated.

Bit Range	Default & Access	Field Name (ID): Description
25	0h RO/V	**xDCI domain PFET Enable Acknowledge Status (AGT25_PFET_EN_ACK_STS):** When AGT25_PFET_EN_ACK_STS = 1, xDCI domain is power gated.
24	0h RO	Reserved.
23	0h RO/V	**CSI2 domain PFET Enable Acknowledge Status (AGT23_PFET_EN_ACK_STS):** When AGT23_PFET_EN_ACK_STS = 1, CSI2 domain is power gated.
22:21	0h RO	Reserved.
20	0h RO/V	**eMMC and SDXC domains PFET Enable Acknowledge Status (AGT20_PFET_EN_ACK_STS):** When AGT20_PFET_EN_ACK_STS = 1, eMMC and SDXC domains are power gated.
19	0h RO/V	**Intel(R) Trace Hub PFET Enable Acknowledge Status (AGT19_PFET_EN_ACK_STS):** When AGT19_PFET_EN_ACK_STS = 1, Intel(R) Trace Hub is power gated.
18	0h RO	Reserved.
17	0h RO/V	**ISH domain PFET Enable Acknowledge Status (AGT17_PFET_EN_ACK_STS):** When AGT17_PFET_EN_ACK_STS = 1, ISH domain is power gated.
16	0h RO/V	**SMB domain PFET Enable Acknowledge Status (AGT16_PFET_EN_ACK_STS):** When AGT16_PFET_EN_ACK_STS = 1, SMB domain is power gated.
15	0h RO/V	**LPC domain PFET Enable Acknowledge Status (AGT15_PFET_EN_ACK_STS):** When AGT15_PFET_EN_ACK_STS = 1, LPC domain is power gated.
14	0h RO/V	**Serial I/O domains PFET Enable Acknowledge Status (AGT14_PFET_EN_ACK_STS):** When AGT14_PFET_EN_ACK_STS = 1, Serial I/O domains are power gated.
13	0h RO	Reserved.
12	0h RO/V	**ADSP domain 3 PFET Enable Acknowledge Status (AGT12_PFET_EN_ACK_STS):** When AGT12_PFET_EN_ACK_STS = 1, ADSP domain 3 is power gated.
11	0h RO/V	**ADSP domain 2 PFET Enable Acknowledge Status (AGT11_PFET_EN_ACK_STS):** When AGT11_PFET_EN_ACK_STS = 1, ADSP domain 2 is power gated.
10	0h RO/V	**ADSP domain 1 PFET Enable Acknowledge Status (AGT10_PFET_EN_ACK_STS):** When AGT10_PFET_EN_ACK_STS = 1, ADSP domain 1 is power gated.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RO/V	**Legacy Audio Controller domain PFET Enable Acknowledge Status (AGT9_PFET_EN_ACK_STS):** When AGT9_PFET_EN_ACK_STS = 1, Legacy Audio Controller domain is power gated.
8	0h RO/V	**SATA domain PFET Enable Acknowledge Status (AGT8_PFET_EN_ACK_STS):** When AGT8_PFET_EN_ACK_STS = 1, SATA domain is power gated.
7	0h RO/V	**GbE domain PFET Enable Acknowledge Status (AGT7_PFET_EN_ACK_STS):** When AGT7_PFET_EN_ACK_STS = 1, GbE domain is power gated.
6	0h RO/V	**PCIe Controller 3 domain PFET Enable Acknowledge Status (AGT6_PFET_EN_ACK_STS):** When AGT6_PFET_EN_ACK_STS = 1, PCIe Controller 3 domain is power gated.
5	0h RO/V	**PCIe Controller 2 domain PFET Enable Acknowledge Status (AGT5_PFET_EN_ACK_STS):** When AGT5_PFET_EN_ACK_STS = 1, PCIe Controller 2 domain is power gated.
4	0h RO/V	**PCIe Controller 1 domain PFET Enable Acknowledge Status (AGT4_PFET_EN_ACK_STS):** When AGT4_PFET_EN_ACK_STS = 1, PCIe Controller 1 domain is power gated.
3	0h RO/V	**xHCI domain PFET Enable Acknowledge Status ( ):** When AGT3_PFET_EN_ACK_STS = 1, xHCI domain is power gated.
2:0	0h RO	Reserved.

5.3.65 PFET Enable Ack Register 1 (PPFEAR1)—Offset 594h

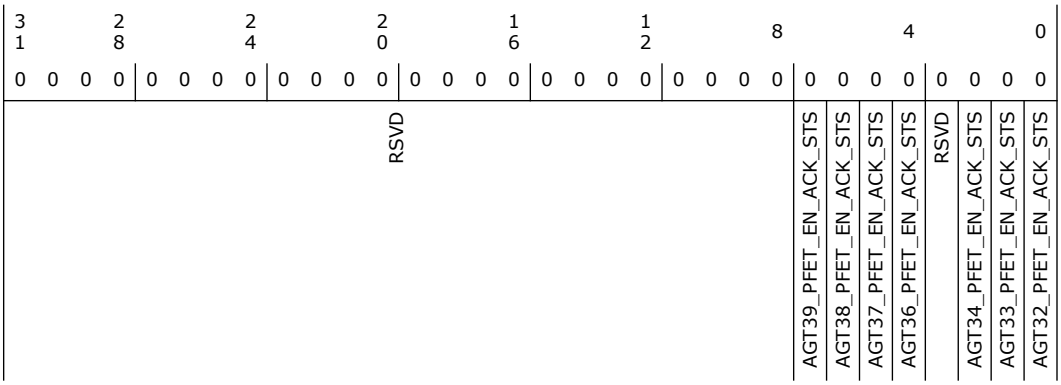
Intel(R) IP is power gated when the corresponding bit in PPFEAR0 or PPFEAR1 is set to 1

Access Method

Type: MEM Register (Size: 32 bits)

Device: 31
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7	0h RO/V	**Intel(R) ME domain 12 PFET Enable Acknowledge Status (AGT39_PFET_EN_ACK_STS):** When AGT39_PFET_EN_ACK_STS = 1, Intel(R) ME domain 12 is power gated.
6	0h RO/V	**Intel(R) ME domain 11 PFET Enable Acknowledge Status (AGT38_PFET_EN_ACK_STS):** When AGT38_PFET_EN_ACK_STS = 1, Intel(R) ME domain 11 is power gated.
5	0h RO/V	**Intel(R) ME domain 10 PFET Enable Acknowledge Status (AGT37_PFET_EN_ACK_STS):** When AGT37_PFET_EN_ACK_STS = 1, Intel(R) ME domain 10 is power gated.
4	0h RO/V	**Intel(R) ME domain 9 PFET Enable Acknowledge Status (AGT36_PFET_EN_ACK_STS):** When AGT36_PFET_EN_ACK_STS = 1, Intel(R) ME domain 9 is power gated.
3	0h RO	Reserved.
2	0h RO/V	**Intel(R) ME domain 8 PFET Enable Acknowledge Status (AGT34_PFET_EN_ACK_STS):** When AGT34_PFET_EN_ACK_STS = 1, Intel(R) ME domain 8 is power gated.
1	0h RO/V	**Intel(R) ME domain 7 PFET Enable Acknowledge Status (AGT33_PFET_EN_ACK_STS):** When AGT33_PFET_EN_ACK_STS = 1, Intel(R) ME domain 7 is power gated.
0	0h RO/V	**Intel(R) ME domain 6 PFET Enable Acknowledge Status (AGT32_PFET_EN_ACK_STS):** When AGT32_PFET_EN_ACK_STS = 1, Intel(R) ME domain 6 is power gated.

5.3.66 Host SW PG Control Register 1 (HSWPGCR1)—Offset 5D0h

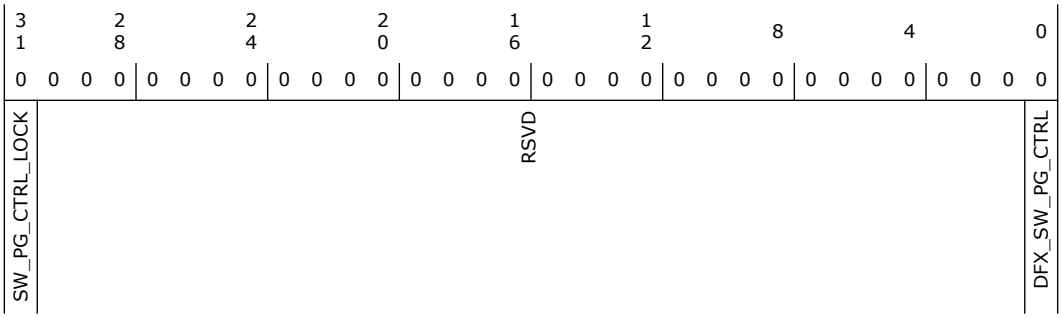
BIOS may program this register.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**SW PG Req Control Lock (SW_PG_CTRL_LOCK):** 0: All other bits in this register are RW (can be set or cleared). 1: All bits in this register are locked (including this bit). Note: BIOS is expected to always write to this bit before handing off control to the OS, even if it has not changed any of the values in this register. This is because this Lock bit resets on platform reset, and needs to be set on every boot to S0 (to prevent any post-BIOS s/w from accessing or updating bits in this register).
30:1	0h RO	Reserved.
0	0h RW/L	**DFX SW PG Req Control (DFX_SW_PG_CTRL):** 0: DFX PGD is not requested to power-gate. DFX logic remains active and available for use. 1: DFX PGD is requested to power-gate by PMC

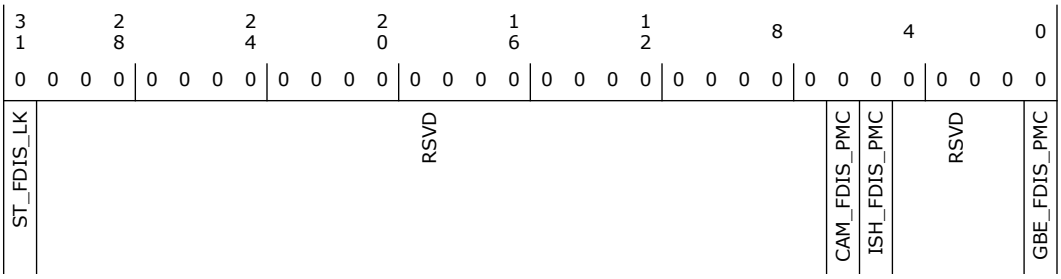
5.3.67 Static PG Function Disable 1 (ST_PG_FDIS1)—Offset 620h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**Static Function Disable Lock (ST_FDIS_LK):** Lock control for all ST_PG_FDIS* and NST_PG_FDIS_* registers. Also self-locks when written to 1. This bit is reset by RSMRST# assertion.
30:7	0h RO	Reserved.
6	0h RW/L	**Camera Function Disable PMC Version (CAM_FDIS_PMC):** BIOS is required to set this bit when Camera function is configured to be function disabled. This bit is reset by RTCRST# assertion.
5	0h RW/L	**ISH Function Disable PMC Version (ISH_FDIS_PMC):** BIOS is required to set this bit when ISH function is configured to be function disabled. This bit is reset by RTCRST# assertion.
4:1	0h RO	Reserved.
0	0h RW/L	**GBE Function Disable PMC Version (GBE_FDIS_PMC):** BIOS is required to set this bit when GBE function is configured to be function disabled. This bit is reset by RTCRST#

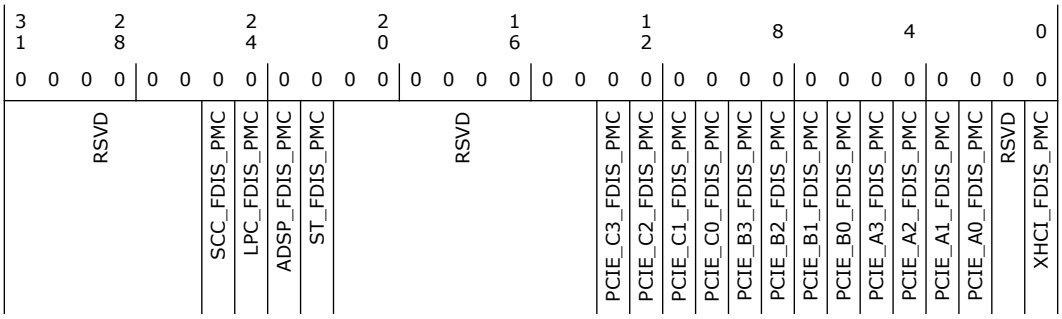
5.3.68 Chipset Initialization Register (NST_PG_FDIS_1)—Offset 628h

BIOS may need to program this register.

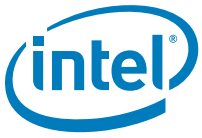
Access Method

Type: MEM Register (Size: 32 bits)
Device: 31
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	Reserved.
25	0h RW/L	**SCC Function Disable (PMC Version) (SCC_FDIS_PMC):** BIOS is required to set this bit when all functions in this IP block (i.e. eMMC and SDXC) are configured to be function disabled.
24	0h RW/L	**XDCI Function Disable (PMC Version) (LPC_FDIS_PMC):** BIOS is required to set this bit when this IP block (single function) is configured to be function disabled.
23	0h RW/L	**ADSP Function Disable (PMC Version) (ADSP_FDIS_PMC):** BIOS is required to set this bit when this IP block (single function) is configured to be function disabled.
22	0h RW/L	**SATA Controller Function Disable (PMC Version) (ST_FDIS_PMC):** BIOS is required to set this bit when the SATA controller (single function) is configured to be function disabled.
21:14	0h RO	Reserved.
13	0h RW/L	**PCIe Controller C Port 3 Function Disable (PMC Version) (PCIE_C3_FDIS_PMC):** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled.
12	0h RW/L	**PCIe Controller C Port 2 Function Disable (PMC Version) (PCIE_C2_FDIS_PMC):** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled.
11	0h RW/L	**PCIe Controller C Port 1 Function Disable (PMC Version) (PCIE_C1_FDIS_PMC):** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled.
10	0h RW/L	**PCIe Controller C Port 0 Function Disable (PMC Version) (PCIE_C0_FDIS_PMC):** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled.
9	0h RW/L	**PCIe Controller B Port 3 Function Disable (PMC Version) (PCIE_B3_FDIS_PMC):** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled.



Bit Range	Default & Access	Field Name (ID): Description
8	0h RW/L	**PCIe Controller B Port 2 Function Disable (PMC Version) (PCIE_B2_FDIS_PMC):** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled.
7	0h RW/L	**PCIe Controller B Port 1 Function Disable (PMC Version) (PCIE_B1_FDIS_PMC):** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled.
6	0h RW/L	**PCIe Controller B Port 0 Function Disable (PMC Version) (PCIE_B0_FDIS_PMC):** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled.
5	0h RW/L	**PCIe Controller A Port 3 Function Disable (PMC Version) (PCIE_A3_FDIS_PMC):** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled.
4	0h RW/L	**PCIe Controller A Port 2 Function Disable (PMC Version) (PCIE_A2_FDIS_PMC):** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled.
3	0h RW/L	**PCIe Controller A Port 1 Function Disable (PMC Version) (PCIE_A1_FDIS_PMC):** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled.
2	0h RW/L	**PCIe Controller A Port 0 Function Disable (PMC Version) (PCIE_A0_FDIS_PMC):** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled.
1	0h RO	Reserved.
0	0h RW/L	**XHCI Function Disable (PMC Version) (XHCI_FDIS_PMC):** BIOS is required to set this bit when this IP block (single logical function) is configured to be function disabled.

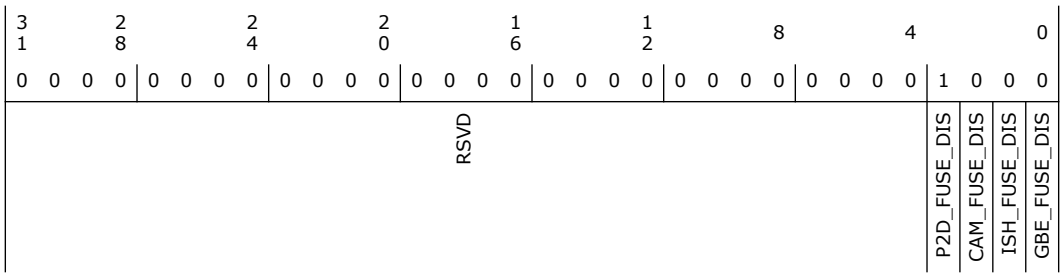
5.3.69 Capability Disable Read Register (FUSE_DIS_RD_2)—Offset 644h

Access Method

Type: MEM Register (Size: 32 bits)

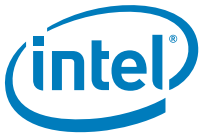
Device: 31
Function: 2

Default: 8h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3	1h RO/V	**2D Disable (P2D_FUSE_DIS):** RO bit indicating if 2D function is disabled.
2	0h RO/V	**Camera Disable (CAM_FUSE_DIS):** RO bit indicating if Camera function is disabled.
1	0h RO/V	**ISH Disable (ISH_FUSE_DIS):** RO bit indicating if ISH function is disabled.
0	0h RO/V	**GBE Fuse Disable (GBE_FUSE_DIS):** RO bit indicating if GBE function is disabled.

§ §



6 Intel® High Definition Audio (Intel® HD Audio) Interface (D31:F3)

6.1 Intel® High Definition Audio (D31:F3) PCI Configuration Registers Summary

Table 6-1. Summary of Intel® High Definition Audio (D31:F3) PCI Configuration Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	1h	Vendor Identification (VID)—Offset 0h	8086h
2h	3h	Device ID (DID)—Offset 2h	See register
4h	5h	Command (CMD)—Offset 4h	0h
6h	7h	Status (STS)—Offset 6h	10h
8h	8h	Revision Identification (RID)—Offset 8h	See register
9h	9h	Programming Interface (PI)—Offset 9h	0h
Ah	Ah	Sub Class Code (SCC)—Offset Ah	3h
Bh	Bh	Base Class Code (BCC)—Offset Bh	4h
Ch	Ch	Cache Line Size (CLS)—Offset Ch	0h
Dh	Dh	Latency Timer (LT)—Offset Dh	0h
Eh	Eh	Header Type (HTYPE)—Offset Eh	0h
10h	13h	Intel HD Audio Base Lower Address (HDALBA)—Offset 10h	4h
14h	17h	Intel HD Audio Base Upper Address (HDAUBA)—Offset 14h	0h
18h	1Bh	Shadowed PCI Configuration Lower Base Address (SPCLBA)—Offset 18h	4h
1Ch	1Fh	Shadowed PCI Configuration Upper Base Address (SPCUBA)—Offset 1Ch	0h
20h	23h	Audio DSP Lower Base Address (ADSPLBA)—Offset 20h	4h
24h	27h	Audio DSP Upper Base Address (ADSPUBA)—Offset 24h	0h
2Ch	2Dh	Subsystem Vendor ID (SVID)—Offset 2Ch	0h
2Eh	2Fh	Subsystem ID (SID)—Offset 2Eh	0h
34h	34h	Capability Pointer (CAPPTR)—Offset 34h	50h
3Ch	3Ch	Interrupt Line (INTLN)—Offset 3Ch	0h
3Dh	3Dh	Interrupt Pin (INTPN)—Offset 3Dh	1h
44h	47h	Power Gating Control (PGCTL)—Offset 44h	0h
48h	4Bh	Clock Gating Control (CGCTL)—Offset 48h	803F01F9h
50h	51h	PCI Power Management Capability ID (PID)—Offset 50h	6001h
52h	53h	Power Management Capabilities (PC)—Offset 52h	C843h
54h	57h	Power Management Control And Status (PCS)—Offset 54h	8h
60h	61h	MSI Capability ID (MID)—Offset 60h	7005h
62h	63h	Message Signal Interrupt Message Control (MMC)—Offset 62h	80h

Table 6-1. Summary of Intel® High Definition Audio (D31:F3) PCI Configuration Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
64h	67h	MSI Message Lower Address (MMLA)—Offset 64h	0h
68h	6Bh	MSI Message Upper Address (MMUA)—Offset 68h	0h
6Ch	6Dh	MSI Message Data (MMD)—Offset 6Ch	0h
70h	71h	PCI Express Capability ID (PXID)—Offset 70h	10h
72h	73h	PCI Express Capabilities (PXC)—Offset 72h	91h
74h	77h	Device Capabilities (DEVCAP)—Offset 74h	10000000h
78h	79h	Device Control (DEVC)—Offset 78h	2800h
7Ah	7Bh	Device Status (DEVS)—Offset 7Ah	10h
C8h	CBh	Extended Mode 3 (SEM3L)—Offset C8h	2800000h
D0h	D3h	Lower Extended Mode 4 (SEM4L)—Offset D0h	2800000h
100h	103h	Virtual Channel Enhanced Capability Header (VCCAP)—Offset 100h	0h
104h	107h	Port VC Capability Register 1 (PVCCAP1)—Offset 104h	1h
108h	10Bh	Port VC Capability Register 2 (PVCCAP2)—Offset 108h	0h
10Ch	10Dh	Port VC Control Register (PVCCTL)—Offset 10Ch	0h
10Eh	10Fh	Port VC Status Register (PVCSTS)—Offset 10Eh	0h
110h	113h	VC0 Resource Capability Register (VC0CAP)—Offset 110h	0h
114h	117h	VC0 Resource Control Register (VC0CTL)—Offset 114h	800000FFh
11Ah	11Bh	VC0 Resource Status Register (VC0STS)—Offset 11Ah	0h
11Ch	11Fh	VCi Resource Capability Register (VCiCAP)—Offset 11Ch	0h
120h	123h	VCi Resource Control Register (VCiCTL)—Offset 120h	0h
126h	127h	VCi Resource Status Register (VCiSTS)—Offset 126h	0h
130h	133h	Root Complex Link Declaration Enhanced (RCCAP)—Offset 130h	10005h
134h	137h	Element Self Description (ESD)—Offset 134h	F000100h
140h	143h	Link 1 Description (L1DESC)—Offset 140h	1h
148h	14Bh	Link 1 Lower Address (L1LADD)—Offset 148h	0h
14Ch	14Fh	Link 1 Upper Address (L1UADD)—Offset 14Ch	0h

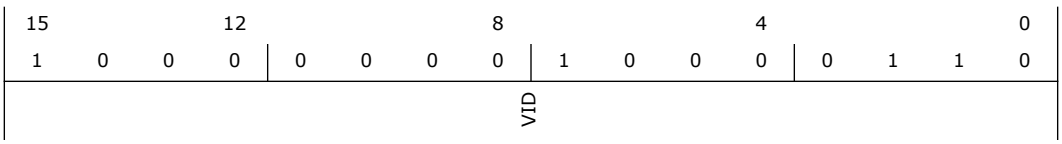
6.1.1 Vendor Identification (VID)—Offset 0h

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 8086h



Bit Range	Default & Access	Field Name (ID): Description
15:0	8086h RO	**Vendor ID (VID):** Indicates that Intel is the vendor.

6.1.2 Device ID (DID)—Offset 2h

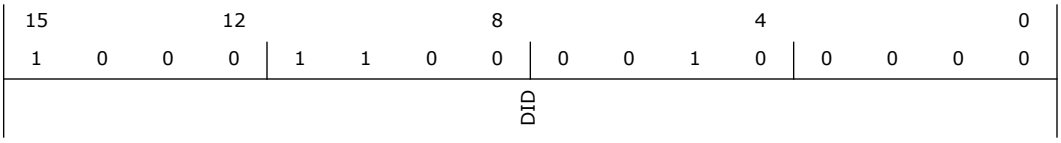
This register is not affected by D3HOT to D0 reset or FLR.

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 3

Default: See register



Bit Range	Default & Access	Field Name (ID): Description
15:0	-- RO/V	**Device ID (DID):** Indicates the device ID .See the Device and Version ID Table in Volume 1 for the default value.

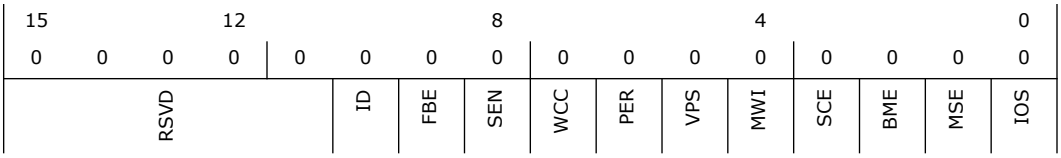
6.1.3 Command (CMD)—Offset 4h

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:11	0h RO	Reserved.
10	0h RW	**Interrupt Disable (ID):** Enables the device to assert an INTx#. When set, the Intel(r) HD Audio controller's INTx# signal will be de-asserted. When cleared, the INTx# signal may be asserted. Note that this bit does not affect the generation of MSI's.
9	0h RO	**Fast Back to Back Enable (FBE):** Not implemented. Hardwired to 0.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**SERR Enable (SEN):** Functionality not implemented. This bit is R/W to pass PCIe compliance testing.
7	0h RO	**Wait Cycle Control (WCC):** Not implemented. Hardwired to 0.
6	0h RW	**Parity Error Response (PER):** Functionality not implemented. This bit is R/W to pass PCIe compliance testing.
5	0h RO	**VGA Palette Snoop (VPS):** Not implemented. Hardwired to 0.
4	0h RO	**Memory Write and Invalidate Enable (MWI):** Not implemented. Hardwired to 0.
3	0h RO	**Special Cycle Enable (SCE):** Not implemented. Hardwired to 0.
2	0h RW	**Bus Master Enable (BME):** 1 = Enable, 0 = Disable. Controls standard PCI Express bus mastering capabilities for Memory and IO, reads and writes. Note that this also controls MSI generation since MSI are essentially Memory writes.
1	0h RW	**Memory Space Enable (MSE):** When set, enables memory space accesses to the Intel HD Audio controller.
0	0h RO	**I/O Space (IOS):** The Intel HD Audio controller does not implement IO Space, therefore this bit is hardwired to 0.

6.1.4 Status (STS)—Offset 6h

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 10h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
DPE	SERRS	RMA	RTA	STA	DEVT		MDPE	FBC	RSVD	C66	CLIST	IS	RSVD		

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Detected Parity Error (DPE):** Not implemented. Hardwired to 0.
14	0h RO	**SERR# Status (SERRS):** Not implemented. Hardwired to 0.
13	0h RW/1C/V	**Received Master Abort (RMA):** If the completion status received from IOSF is UR, this bit is set. SW writes a 1 to this bit to clear it.
12	0h RW/1C/V	**Received Target Abort (RTA):** If the completion status received from IOSF is CA, this bit is set. SW writes a 1 to this bit to clear it.
11	0h RO	**Signaled Target-Abort (STA):** Not implemented. Hardwired to 0.

Bit Range	Default & Access	Field Name (ID): Description
10:9	0h RO	**DEVSEL# Timing Status (DEVT):** Does not apply. Hardwired to 0.
8	0h RO	**Master Data Parity Error (MDPE):** Not implemented. Hardwired to 0.
7	0h RO	**Fast Back to Back Capable (FBC):** Does not apply. Hardwired to 0.
6	0h RO	Reserved.
5	0h RO	**66 MHz Capable (C66):** Does not apply. Hardwired to 0.
4	1h RO	**Capabilities List Exists (CLIST):** Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h.
3	0h RO/V	**Interrupt Status (IS):** Reflects the state of the INTx# signal at the input of the enable/disable circuit. This bit is a 1 when the INTx# is asserted. This bit is a 0 after the interrupt is cleared (independent of the state of the Interrupt Disable bit in the command register). Note that this bit is not set by an MSI.
2:0	0h RO	Reserved.

6.1.5 Revision Identification (RID)—Offset 8h

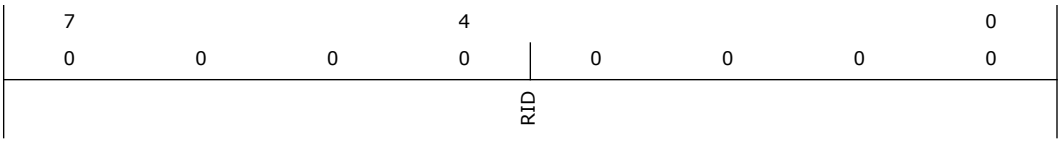
This register is not affected by D3HOT to D0 reset or FLR

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 31
Function: 3

Default: See register



Bit Range	Default & Access	Field Name (ID): Description
7:0	-- RO/V	**Revision ID (RID):** Indicates stepping of the host controller. Refer to Device and Revision ID table in Volume 1 for specific value.

6.1.6 Programming Interface (PI)—Offset 9h

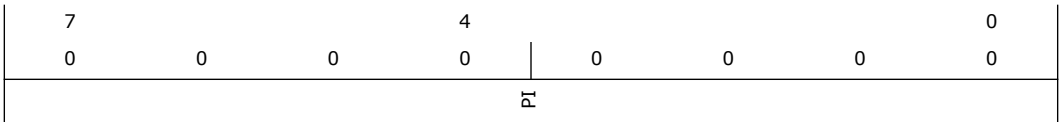
This register is not affected by D3HOT to D0 reset or FLR

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW/L	**Programming Interface (PI):** Value assigned to the Intel HD Audio subsystem. Locked when FNCFG.BCLD = 1.

6.1.7 Sub Class Code (SCC)—Offset Ah

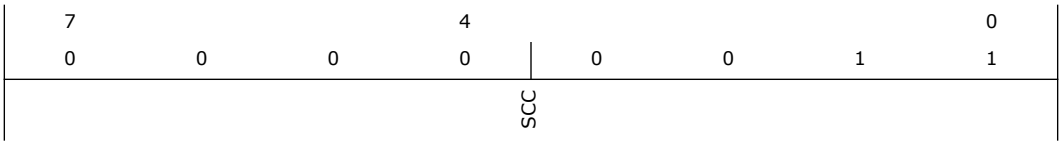
This register is not affected by D3HOT to D0 reset or FLR

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 31
Function: 3

Default: 3h



Bit Range	Default & Access	Field Name (ID): Description
7:0	3h RW/L	**Sub Class Code (SCC):** This indicates the device is an Intel HD Audio audio device, in the context of a multimedia device. Locked when FNCFG.BCLD = 1.

6.1.8 Base Class Code (BCC)—Offset Bh

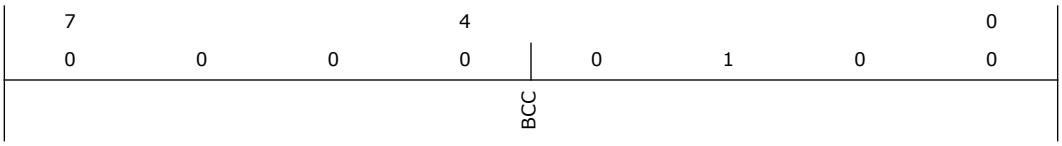
This register is not affected by D3HOT to D0 reset or FLR

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 31
Function: 3

Default: 4h



Bit Range	Default & Access	Field Name (ID): Description
7:0	4h RW/L	**Base Class Code (BCC):** This register indicates that the function implements a multimedia device. Locked when FNCFG.BCLD = 1.

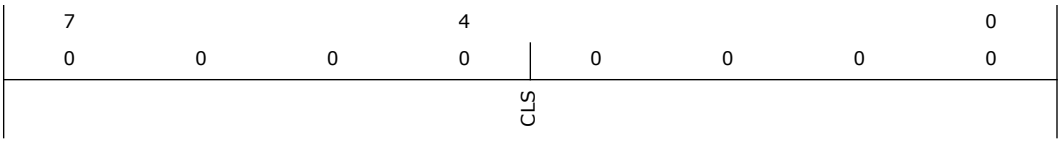
6.1.9 Cache Line Size (CLS)—Offset Ch

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**Cache Line Size (CLS):** Doesn't apply to PCI Express. PCI Express spec requires this to be implemented as a R/W register but has no functional impact on the PCH.

6.1.10 Latency Timer (LT)—Offset Dh

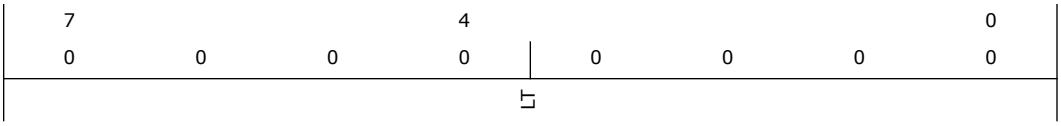
RO. Hardwired to 00

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW/L	**Latency Timer (LT):** Doesn t apply to PCI Express. RO as 00h if PCI Express. If configured to appear as PCI device, maintain RW for Legacy PCI SW compliancy. Locked when FNCFG.HDASPCID = 0

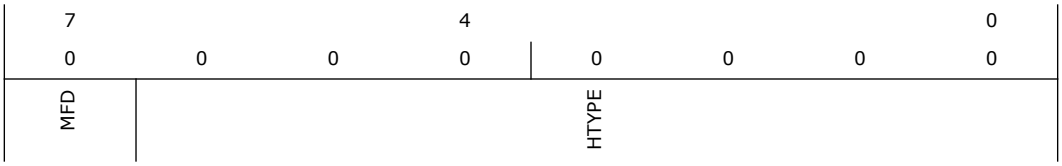
6.1.11 Header Type (HTYPE)—Offset Eh

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7	0h RW/L	**Multi Function Device (MFD):** Value of 0 indicates a single function device. Value of 1 indicates a multi function device. Locked when FNCFG.BCLD = 1.
6:0	0h RO	**Header Type (HTYPE):** Implements Type 0 Configuration header.

6.1.12 Intel HD Audio Base Lower Address (HDALBA)—Offset 10h

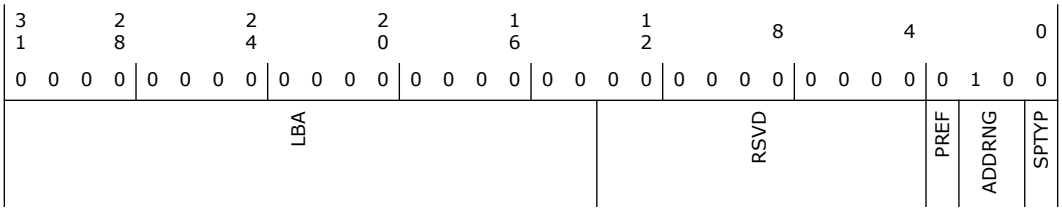
This BAR creates a selected size of memory space to signify the base address of the Intel HD Audio memory mapped configuration registers depending on implementation.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 4h



Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RW	**Lower Base Address (LBA):** Base address for the Intel HD Audio subsystem s memory mapped configuration registers. 16 Kbytes are requested by hardwiring bits 13:4 to 0 s.
13:4	0h RO	Reserved.
3	0h RO	**Prefetchable (PREF):** Indicates that this BAR is NOT pre-fetchable.
2:1	2h RO	**Address Range (ADDRNG):** Indicates that this BAR can be located anywhere in 64-bit address space.
0	0h RO	**Space Type (SPTYP):** Indicates that this BAR is located in memory space.

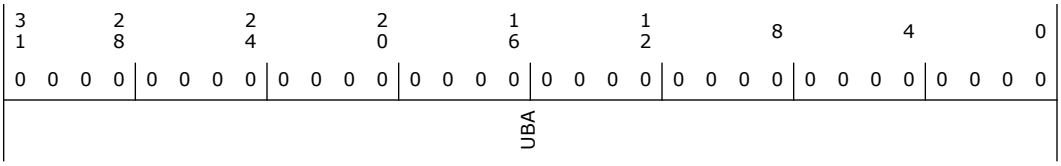
6.1.13 Intel HD Audio Base Upper Address (HDAUBA)—Offset 14h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Intel HD Audio Upper Base Address (UBA):** Upper 32 bits of the Base address for the Intel(r) HD Audio controller's memory mapped configuration registers.

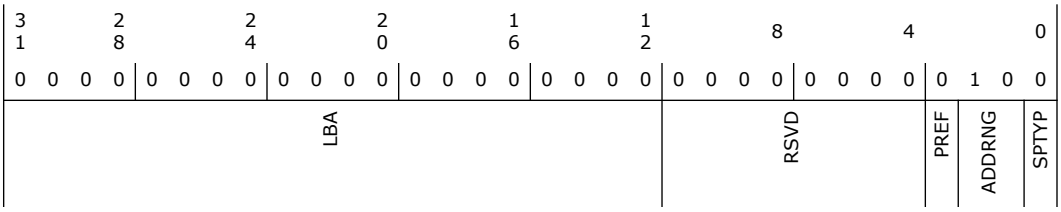
6.1.14 Shadowed PCI Configuration Lower Base Address (SPCLBA)—Offset 18h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 4h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW/L	**Lower Base Address (LBA):** Base address for the PCI Configuration register shadowed to memory mapped. 4 KB is requested by hardwiring bits 11:4 to 0 s. Locked when PCICFGCTL0.SPCBAD = 1.
11:4	0h RO	Reserved.
3	0h RO	**Prefetchable (PREF):** Indicates that this BAR is NOT pre-fetchable.
2:1	2h RO/V	**Address Range (ADDRNG):** Indicates that this BAR can be located anywhere in 64-bit address space.
0	0h RO	**Space Type (SPTYP):** Indicates that this BAR is located in memory space.

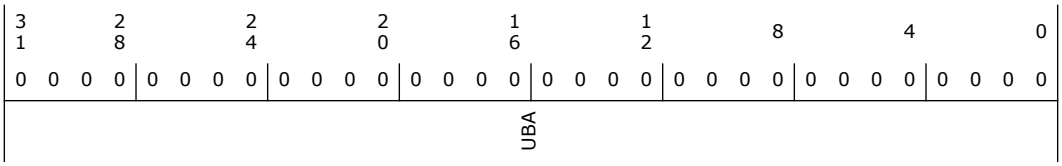
6.1.15 Shadowed PCI Configuration Upper Base Address (SPCUBA)—Offset 1Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/L	**Upper Base Address (UBA):** Upper 32 bits of the Base address for the PCI Configuration register shadowed to memory mapped. Locked when PCICFGCTL0.SPCBAD = 1.

6.1.16 Audio DSP Lower Base Address (ADSPLBA)—Offset 20h

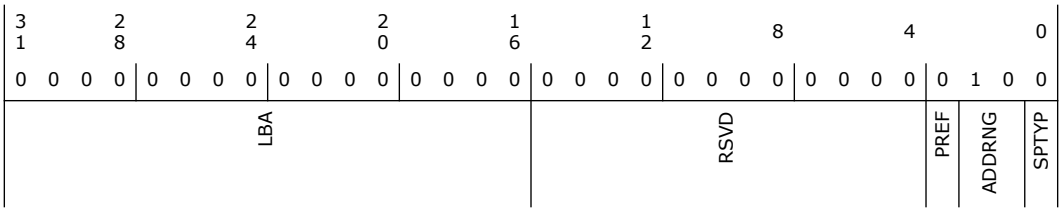
This BAR creates a selected size of memory space to signify the base address of the Audio DSP memory mapped configuration registers depending on implementation.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 4h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Lower Base Address (LBA):** Base address for the Audio DSP memory mapped configuration registers.
15:4	0h RO	**Reserved (RSVD)**

Bit Range	Default & Access	Field Name (ID): Description
3	0h RO	**Prefetchable (PREF):** Indicates that this BAR is NOT pre-fetchable.
2:1	2h RO	**Address Range (ADDRNG):** Indicates that this BAR can be located anywhere in 64-bit address space.
0	0h RO	**Space Type (SPTYP):** Indicates that this BAR is located in memory space.

6.1.17 Audio DSP Upper Base Address (ADSPUBA)—Offset 24h

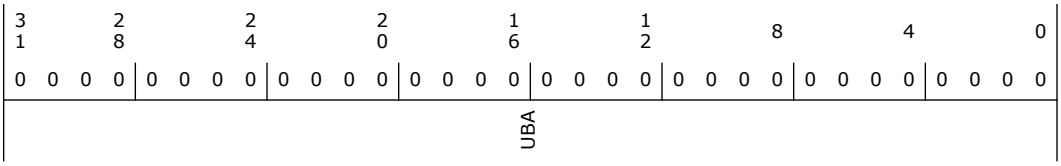
Upper Base address for the Audio DSP memory mapped configuration registers.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Upper Base Address (UBA):** Upper 32 bits of the Base address for the Audio DSP memory mapped configuration registers.

6.1.18 Subsystem Vendor ID (SVID)—Offset 2Ch

This register should be implemented for any function that could be instantiated more than once in a given system, for example, a system with 2 audio subsystems, one down on the motherboard and the other plugged into a PCI expansion slot, should have the SVID register implemented. The SVID register, in combination with the Subsystem ID register, enables the operating environment to distinguish one audio subsystem from the other(s).
Software (BIOS) will write the value to this register. After that, the value can be read, but writes to the register will have no effect. The write to this register should be combined with the write to the SID to create one 32-bit write. This register is not affected by D3HOT to D0 reset or FLR

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW/L	**SVID (SVID):** These RW bits have no functionality. Locked when FNCFG.BCLD = 1.

6.1.19 Subsystem ID (SID)—Offset 2Eh

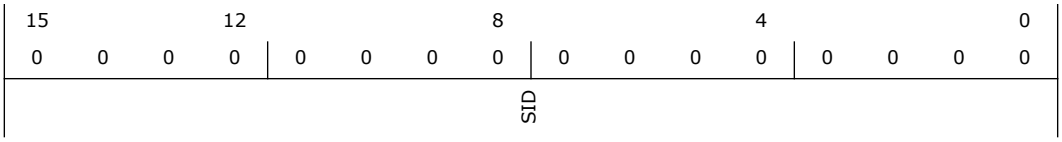
This register should be implemented for any function that could be instantiated more than once in a given system, for example, a system with 2 audio subsystems, one down on the motherboard and the other plugged into a PCI expansion slot. The SID register, in combination with the Subsystem Vendor ID register make it possible for the operating environment to distinguish one audio subsystem from the other(s). Software (BIOS) will write the value to this register. After that, the value can be read, but writes to the register will have no effect. The write to this register should be combined with the write to the SVID to create one 32-bit write. This register is not affected by D3HOT to D0 reset or FLR.

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW/L	**SID (SID):** These RW bits have no functionality. Locked when FNCFG.BCLD = 1.

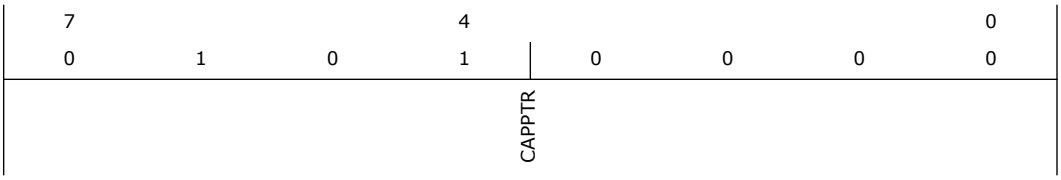
6.1.20 Capability Pointer (CAPPTR)—Offset 34h

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 31
Function: 3

Default: 50h



Bit Range	Default & Access	Field Name (ID): Description
7:0	50h RO	**Capability Pointer (CAPPTR):** Indicates that the first capability pointer offset is offset 50h (Power Management Capability).

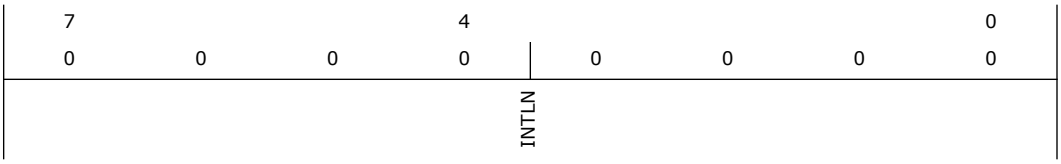
6.1.21 Interrupt Line (INTLN)—Offset 3Ch

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**Interrupt Line (INTLN):** Hardware does not use this field directly. It is used to communicate to software the interrupt line that the interrupt pin is connected to.

6.1.22 Interrupt Pin (INTPN)—Offset 3Dh

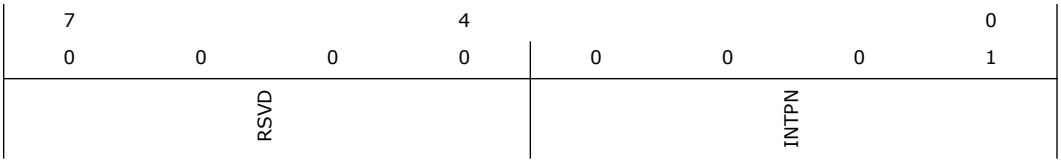
This register is not affected by D3HOT to D0 reset or FLR.

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 31
Function: 3

Default: 1h



Bit Range	Default & Access	Field Name (ID): Description
7:4	0h RO	Reserved.
3:0	1h RW/L	**Interrupt Pin (INTPN):** Identifies the interrupt pin the function uses. 0h: No interrupt pin 1h: INTA 2h: INTB 3h: INTC 4h: INTD 5h Fh: reserved Locked when FNCFG.BCLD = 1.

6.1.23 Power Gating Control (PGCTL)—Offset 44h

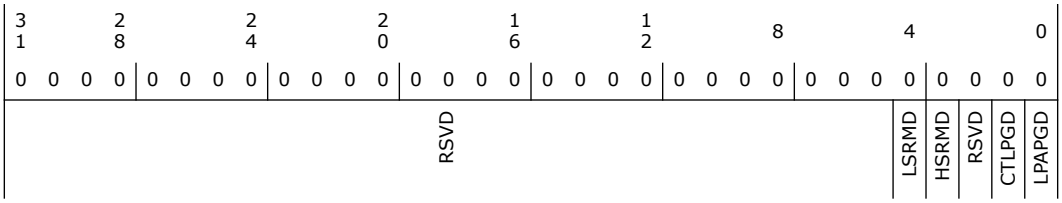
D3PGD are meant for the Intel HD Audio driver software to control whether the Intel HD Audio subsystem should be power gated or not in D3.
Note that the power gating will only be initiated when out of platform reset, if conditions are met.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4	0h RW	**LP SRAM Retention Module Disable (LSRMD):** Register is used to disable the LP SRAM retention mode capbility of the L2 SRAMs.
3	0h RW	**HP SRAM Retention Module Disable (HSRMD):** Register is used to disable the HP SRAM retention mode capbility of the L2 SRAMs.
2	0h RO	Reserved.
1	0h RW	**D3 Power Gating Disable (CTLPGD):** Register is used to disable the power gating capbility during D3 state.
0	0h RW	**Low Power Audio Power Gating Disable (LPAPGD):** Register is used to disable the power gating capbility of the Primary well (gated-controller) domain.

6.1.24 Clock Gating Control (CGCTL)—Offset 48h

The trunk clock gating enable and local clock gating enables are meant for BIOS or driver to enable or disable the HW capability to detect idle condition and clock gate accordingly. HW should treat these clock gate enable register bits as 0 if FNCFG.CGD =

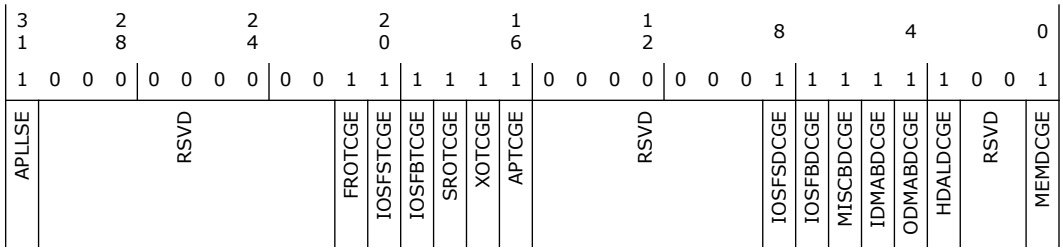
1 or FUSVAL.CGD = 1.
Note that the clock gating will only be initiated when out of platform reset, if conditions are met.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 803F01F9h



Bit Range	Default & Access	Field Name (ID): Description
31	1h RW	**Audio PLL Shutdown Enable (APLLSE):** Set to 1 to enable PLL shutdown after trunk clock gating.
30:22	0h RO	Reserved.
21	1h RW	**Fast RING Oscillator Trunk Clock Gating Enable (FROTCGE):** Set to 1 to enable trunk clock gating. If enabled, HW will trunk clock gate when no logic are using this clock (i.e. all local clock gating condition is true).
20	1h RW	**IOSF Sideband Trunk Gate Enable (IOSFSTCGE):** Enable IOSF trunk clock gating functionality on IOSF interface. When set, IOSF Sideband interface clock request can de-assert to allow trunk clock gating.
19	1h RW	**IOSF Backbone Trunk Gate Enable (IOSFBTCGE):** Enable IOSF trunk clock gating functionality on IOSF interface. When set, IOSF Primary interface clock request can de-assert to allow trunk clock gating.
18	1h RW	**Slow RING Oscillator Trunk Clock Gating Enable (SROTCGE):** Set to 1 to enable trunk clock gating. If enabled, HW will trunk clock gate when no logic are using this clock (i.e. all local clock gating condition is true).
17	1h RW	**XTAL Oscillator Trunk Clock Gating Enable (XOTCGE):** Set to 1 to enable trunk clock gating. If enabled, HW will trunk clock gate when no logic are using this clock (i.e. all local clock gating condition is true).
16	1h RW	**Audio PLL Trunk Clock Gating Enable (APTCGE):** Set to 1 to enable trunk clock gating. If enabled, HW will trunk clock gate when no logic are using this clock (i.e. all local clock gating condition is true).
15:9	0h RO	Reserved.
8	1h RW	**IOSF Sideband Dynamic Clock Gate Enable (IOSFSDCGE):** Enable IOSF dynamic clock gating functionality inside IOSF interface. When set, IOSF Sideband clock gating functionality is enabled.
7	1h RW	**IOSF Backbone Dynamic Clock Gate Enable (IOSFBDCGE):** Enable IOSF dynamic clock gating functionality inside IOSF interface. When set, IOSF Primary clock gating functionality is enabled.
6	1h RW	**Miscellaneous Backbone Dynamic Clock Gating Enable (MISCBDCGE):** This controls dynamic clock gating of backbone (Command/data) clocks to the rest of the Intel HD Audio controller (i.e. other than the IOSF, Input DMA engine, and Output DMA engine). When this bit is asserted, dynamic clock gating logic is enabled for backbone clocks to the rest of the Intel HD Audio controller.

Bit Range	Default & Access	Field Name (ID): Description
5	1h RW	**IDMA Backbone Dynamic Clock Gating Enable (IDMABDCGE):** This controls dynamic clock gating of backbone (Command/data) clocks to each Input DMA engine. When this bit is asserted, dynamic clock gating logic is enabled for backbone clocks to each Input DMA engine.
4	1h RW	**ODMA Backbone Dynamic Clock Gating Enable (ODMABDCGE):** This controls dynamic clock gating of backbone (Command/data) clocks to each Output DMA engines. When this bit is asserted, dynamic clock gating logic is enabled for backbone clocks to each Output DMA engine.
3	1h RW	**HD Audio Link Dynamic Clock Gating Enable (HDALDCGE):** This controls dynamic clock gating of bitclk to Link Layer and each Input/Output DMA engine. When this bit is asserted, dynamic clock gating logic is enabled for bitclk.
2:1	0h RO	Reserved.
0	1h RW	**Memory Dynamic Clock Gating Enable (MEMDCGE):** When set to 1, it allows HW to automatically detect for idle condition and clock gate Memory block. When clear to 0, it disables this HW auto detect idle clock gating.

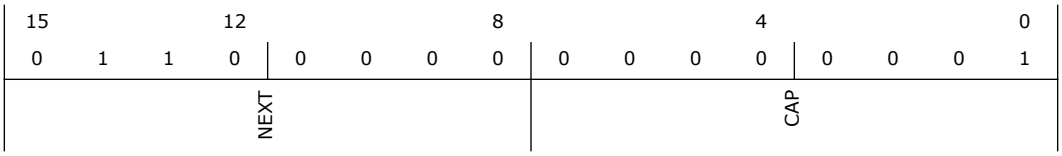
6.1.25 PCI Power Management Capability ID (PID)—Offset 50h

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 6001h



Bit Range	Default & Access	Field Name (ID): Description
15:8	60h RW/L	**Next Capability (NEXT):** Points to the next capability structure (MSI). Locked when FNCFG.BCLD = 1.
7:0	1h RO	**Cap ID (CAP):** Indicates that this pointer is a PCI power management capability

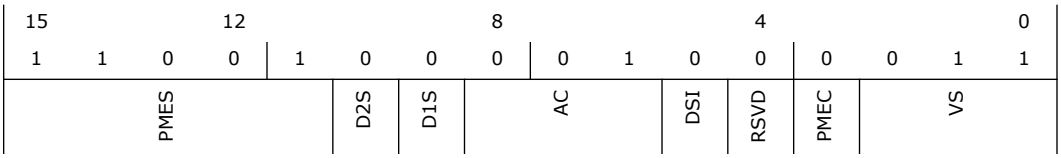
6.1.26 Power Management Capabilities (PC)—Offset 52h

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 3

Default: C843h



Bit Range	Default & Access	Field Name (ID): Description
15:11	19h RW/L	**PME_Support (PMES):** Indicates PME# can be generated from D3 and D0 states. Programmable by BIOS for the option to declare SUS well wake is supported or not: 19h (SUS well wake supported) or 09h (SUS well wake not supported). Locked when FNCFG.BCLD = 1
10	0h RO	**D2_Support (D2S):** The D2 state is not supported.
9	0h RO	**D1_Support (D1S):** The D1 state is not supported.
8:6	1h RW/L	**Aux_Current (AC):** Reports 55 mA maximum Suspend well current required when in the D3cold state. Programmable by BIOS for the option to declare SUS well wake is supported or not: 001b (SUS well wake supported) or 000b (SUS well wake not supported). Locked when FNCFG.BCLD = 1.
5	0h RO	**Device Specific Initialization (DSI):** Indicates that no device-specific initialization is required.
4	0h RO	Reserved.
3	0h RO	**PME Clock (PMEC):** Does not apply. Hardwired to 0.
2:0	3h RW/L	**Version (VS):** Indicates support for Revision 1.2 of the PCI Power Management Specification. Programmable by BIOS to older revision if compatibility issue is found. Locked when FNCFG.BCLD = 1.

6.1.27 Power Management Control And Status (PCS)—Offset 54h

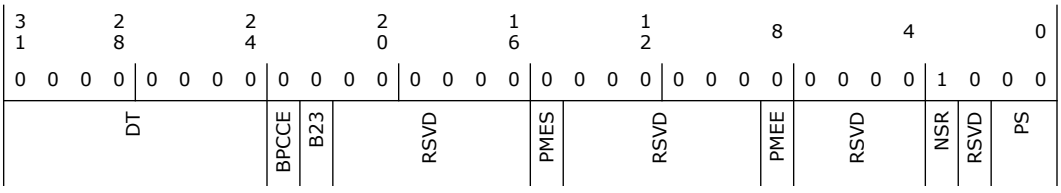
PMES and PMEE bits reside in Resume well, and reset by resume reset.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 8h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Data (DT):** Does not apply. Hardwired to 0's.
23	0h RO	**Bus Power/Clock Control Enable (BPCCE):** Does not apply. Hardwired to0.
22	0h RO	**B2/B3 Support (B23):** Does not apply. Hardwired to 0.
21:16	0h RO	Reserved.
15	0h RW/1C/V	**PME Status (PMES):** This bit is set when the Intel HD Audio controller would normally assert the PME# signal independent of the state of the PME bit. This bit is cleared on a power-on reset. Software must not make assumptions about the reset state of this bit and must set it appropriately.
14:9	0h RO	Reserved.
8	0h RW	**PME Enable (PMEE):** When set, and if corresponding PMES is also set, the Intel HD Audio subsystem send PME to PMC. This bit is cleared on a power-on reset. Software must not make assumptions about the reset state of this bit and must set it appropriately.
7:4	0h RO	Reserved.
3	1h RW/L	**No Soft Reset (NSR):** When set (1), this bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved. Upon transition from the D3hot to the D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the PowerState bits. When clear (0), devices do perform an internal reset upon transitioning from D3hot to D0 via software control of the PowerState bits. Configuration Context is lost when performing the soft reset. Upon transition from the D3hot to the D0 state, full reinitialization sequence is needed to return the device to D0 Initialized. Regardless of this bit, devices that transition from D3hot to D0 by a system or bus segment reset will return to the device state D0 Uninitialized with only PME context preserved if PME is supported and enabled. Locked when FNCFG.BCLD = 1.
2	0h RO	Reserved.
1:0	0h RW	**Power State (PS):** This field is used both to determine the current power state of the Intel HD Audio subsystem and to set a new power state. The values are: 00 D0 state 11 D3HOT state If software attempts to write a value of 10b or 01b in to this field, the write operation must complete normally, however, the data is discarded and no state change occurs. When in the D3HOT states, the Intel HD Audio subsystem s configuration space is available, but the I/O and memory spaces are not. Additionally, interrupts are blocked. When software changes this value from the D3HOT state to the D0 state, an internal warm (soft) reset is generated, and software must re-initialize the function.

6.1.28 MSI Capability ID (MID)—Offset 60h

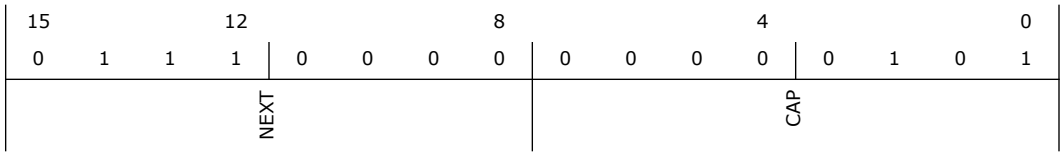
NEXT field is not affected by D3HOT to D0 reset or FLR

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 7005h



Bit Range	Default & Access	Field Name (ID): Description
15:8	70h RO/V	**Next Capability (NEXT):** Points to the PCI Express* capability structure. The value of this field depends on the FNCFG.HDASPCID bit. When FNCFG.HDASPCID is 0 , this field has a value of 70h where it points to the PCI Express capability structure. When FNCFG.HDASPCID bit is 1 , this field has a value of 00h to indicate that this is the last capability structure in the list.
7:0	5h RO	**Cap ID (CAP):** Indicates that this pointer is a MSI capability

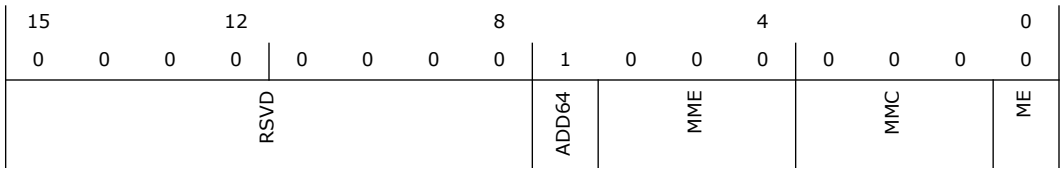
6.1.29 Message Signal Interrupt Message Control (MMC)—Offset 62h

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 80h



Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	Reserved.
7	1h RO	**64b Address Capability (ADD64):** RO. Hardwired to 1. Indicates the ability to generate a 64-bitmessage address
6:4	0h RO	**Multiple Message Enable (MME):** Normally this is a R/W register. Howeversince only 1 message is supported, these bits are hardwired to 000 = 1 message.
3:1	0h RO	**Multiple Message Capable (MMC):** Hardwired to 0 indicating request for 1 message.
0	0h RW	**MSI Enable (ME):** R/W. 0 = An MSI may not be generated. 1 = an MSI will be generated instead of an INTx signal.

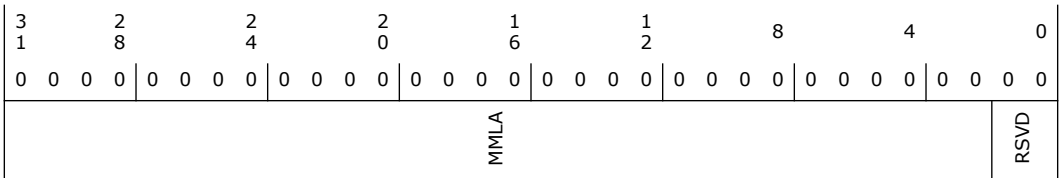
6.1.30 MSI Message Lower Address (MMLA)—Offset 64h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**MSI Message Lower Address (MMLA):** Lower Address used for MSI Message.
1:0	0h RO	Reserved.

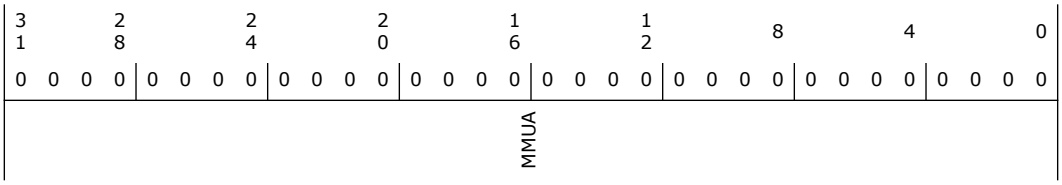
6.1.31 MSI Message Upper Address (MMUA)—Offset 68h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**MSI Message Upper Address (MMUA):** Upper 32 bits of address used for MSIMessage.

6.1.32 MSI Message Data (MMD)—Offset 6Ch

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW	**MSI Message Data (MMD):** Data used for MSI Message.

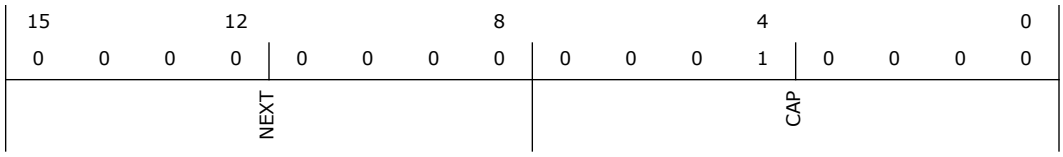
6.1.33 PCI Express Capability ID (PXID)—Offset 70h

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 10h



Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Next Capability (NEXT):** Indicates that this is the last capability structure inthe list.
7:0	10h RO	**Cap ID (CAP):** Indicates that this pointer is a PCI Express capability structure.

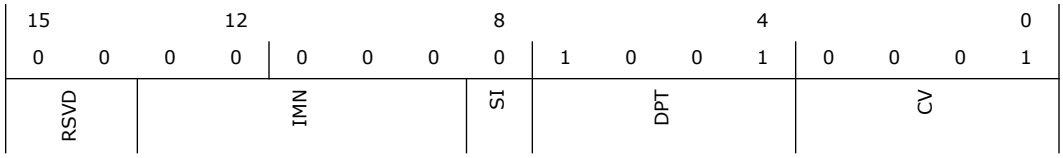
6.1.34 PCI Express Capabilities (PXC)—Offset 72h

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 91h



Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RO	Reserved.
13:9	0h RO	**Interrupt Message Number (IMN):** Hardwired to 0.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RO	**Slot Implemented (SI):** Hardwired to 0.
7:4	9h RO	**Device/Port Type (DPT):** Indicates that this is a Root Complex IntegratedEndpoint Device.
3:0	1h RO	**Capability Version (CV):** Indicates version #1 PCI Express capability

6.1.35 Device Capabilities (DEVCAP)—Offset 74h

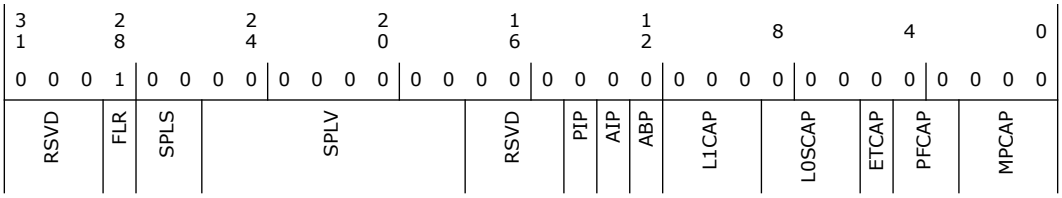
This register is not affected by D3HOT to D0 reset or FLR.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 10000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	Reserved.
28	1h RW/L	**Functional Level Reset (FLR):** A 1 indicates that the Intel HD Audio subsystem supports the Function Level Reset capability. Locked when FNCFG.BCLD = 1.
27:26	0h RO	**Captured Slot Power Limit Scale (SPLS):** Hardwired to 0.
25:18	0h RO	**Captured Slot Power Limit Value (SPLV):** Hardwired to 0.
17:15	0h RO	Reserved.
14	0h RO	**Power Indicator Present (PIP):** Hardwired to 0.
13	0h RO	**Attention Indicator Present (AIP):** Hardwired to 0.
12	0h RO	**Attention Button Present (ABP):** Hardwired to 0.
11:9	0h RW/L	**Endpoint L1 Acceptable Latency (L1CAP):** This bit field is defined in the PCI Express spec as RO. At this time it is risky to assign a hardwired value to this bit field. Making it RW would cause a WHQL failure. By making it RW/L it will appear as RO to WHQL testing while allowing BIOS to write a value at boot that is determined by post silicon system testing. Locked when FNCFG.BCLD = 1.

Bit Range	Default & Access	Field Name (ID): Description
8:6	0h RW/L	**Endpoint L0s Acceptable Latency (L0SCAP):** This bit field is defined in the PCI Express spec as RO. At this time it is risky to assign a hardwired value to this bit field. Making it RW would cause a WHQL failure. By making it RW/L it will appear as RO to WHQL testing while allowing BIOS to write a value at boot that is determined by post silicon system testing. Locked when FNCFG.BCLD = 1.
5	0h RO	**Extended Tag Field Support (ETCAP):** Indicates 5 bit tag supported.
4:3	0h RO	**Phantom Functions Supported (PFCAP):** Indicates phantom functions not supported.
2:0	0h RO	**Max Payload Size Supported (MPCAP):** Indicates 128B maximum payloadsize capability.

6.1.36 Device Control (DEVC)—Offset 78h

NSNPEN bit is not affected by D3HOT to D0 reset or FLR.

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 2800h

15			12				8				4				0
0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0
IF	MRRS			NSNPEN	AUXPEN	PFEN	ETEN	MAXPAY			ROEN	URREN	FEREN	NFEREN	CEREN

Bit Range	Default & Access	Field Name (ID): Description
15	0h WO	**Initiate FLR (IF):** Used to initiate FLR transition. A write of 1 initiates FLR transition. Since hardware must not respond to any cycles until FLR completion, the read value by software from this bit is 0 .
14:12	2h RW	**Max Read Request Size (MRRS):** This field sets the maximum Read Request size for the Function as a Requester. The Function must not generate Read Requests with size exceeding the set value. Defined encodings for this field are: 000: 128 B 001: 256 B 010: 512 B 011: 1024 B 100: 2048 B 101: 4096 B 110 - 111: Reserved
11	1h RW	**Enable No Snoop (NSNPEN):** When set to 1 (or EM2.FNSNPEN = 1) the Intel HD Audio controller is permitted to set the No Snoop bit in the Requester Attributes of a bus master transaction. In this case VC0, VCp, or VC1 may be used for isochronous transfers. When set to 0 (and EM2.FNSNPEN = 0) the Intel HD Audio controller will not set the No Snoop bit. In the case isochronous transfers will not use VC1(VCi) even if it is enabled since VC1 is never snooped. Isochronous transfers will use either VCp or VC0. This bit is not affected by D3HOT to D0 reset or FLR.
10	0h RO	**Auxiliary (AUX) Power PM Enable (AUXPEN):** Hardwired to 0 indicating Intel HD Audio device does not draw AUX power.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RO	**Phantom Functions Enable (PFEN):** Hardwired to 0 disabling phantom functions.
8	0h RO	**Extended Tag Field Enable (ETEN):** Hardwired to 0 enabling 5-bit tag.
7:5	0h RO	**Max Payload Size (MAXPAY):** Hardwired to 000 indicating 128 B.
4	0h RO	**Enable Relaxed Ordering (ROEN):** Hardwired to 0 disabling relaxed ordering.
3	0h RW	**Unsupported Request Reporting Enable (URREN):** Functionality not implemented. This bit is R/W to pass PCIe compliance testing.
2	0h RW	**Fatal Error Reporting Enable (FEREN):** Functionality not implemented. This bit is R/W to pass PCIe compliance testing.
1	0h RW	**Non-Fatal Error Reporting Enable (NFEREN):** Functionality not implemented. This bit is R/W to pass PCIe compliance testing.
0	0h RW	**Correctable Error Reporting Enable (CEREN):** Functionality not implemented. This bit is R/W to pass PCIe compliance testing.

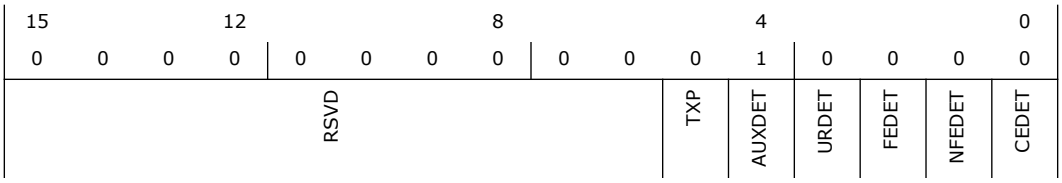
6.1.37 Device Status (DEVS)—Offset 7Ah

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 10h



Bit Range	Default & Access	Field Name (ID): Description
15:6	0h RO	Reserved.
5	0h RO/V	**Transactions Pending (TXP):** A 1 indicates that the Intel HD Audio controller has issued Non-Posted requests which have not been completed. A 0 indicates that Completions for all Non-Posted Requests have been received.
4	1h RW/L	**AUX Power Detected (AUXDET):** Hardwired to 1 indicating the device is connected to Suspend power. Programmable by BIOS for the option to declare SUS well wake is supported or not: 1b (SUS well wake supported) or 0b (SUS well wake not supported). Locked when FNCFG.BCLD = 1.
3	0h RO	**Unsupported Request Detected (URDET):** Not implemented. Hardwired to 0.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	**Fatal Error Detected (FEDET):** Not implemented. Hardwired to 0.
1	0h RO	**Non-Fatal Error Detected (NFEDET):** Not implemented. Hardwired to 0.
0	0h RO	**Correctable Error Detected (CEDET):** Not implemented. Hardwired to 0.

6.1.38 Extended Mode 3 (SEM3L)—Offset C8h

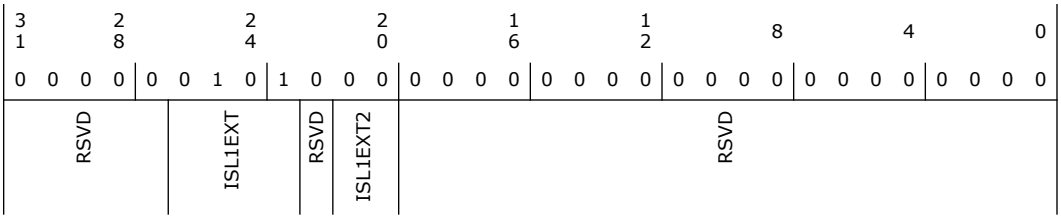
This register resides in Primary well (always on).

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 2800000h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	Reserved.
26:23	5h RW	**Input Stream L1 Exit Threshold (ISL1EXT):** This field determines the minimum amount of free space (no. of frames) available in which the PCH HD Audio controller will begin the signaling of DMI L1 exit event. If the value specified here is larger than the percentage L1 exit threshold specified in ISL1EXT2 field (or percentage L1 exit threshold is disabled), then the L1 exit threshold is equal to the value specified here. If the value specified here is smaller or equal to the percentage L1 exit threshold specified in the ISL1EXT2 field, then the L1 exit threshold is equal to the value specified in ISL1EXT2 field. This field only has effect when L1SEN bit is '1'. Bits Free Space Available (no. of frames) 0000 Reserved 0001 1 0010 2 ... ... 1111 15

Bit Range	Default & Access	Field Name (ID): Description
22	0h RO	Reserved.
21:20	0h RW	**Input Stream L1 Exit Threshold 2 (ISL1EXT2):** This field determines the amount of free space (no. of frames) available in the input stream FIFO in which the PCH HD Audio controller will begin the signaling of percentage based DMI L1 exit event. If the value specified here is smaller or equal to the minimum L1 exit threshold specified in ISL1EXT field (or percentage L1 exit threshold is disabled), then the L1 exit threshold is equal to the value specified in ISL1EXT field. If the value specified here is larger than the minimum L1 exit threshold specified in the ISL1EXT field, then the L1 exit threshold is equal to the value specified in this field. 00: percentage L1 exit threshold disabled. 01: Reserved 10: 1/8 of effective FIFO size. 11: 1/4 of effective FIFO size.
19:0	0h RO	Reserved.

6.1.39 Lower Extended Mode 4 (SEM4L)—Offset D0h

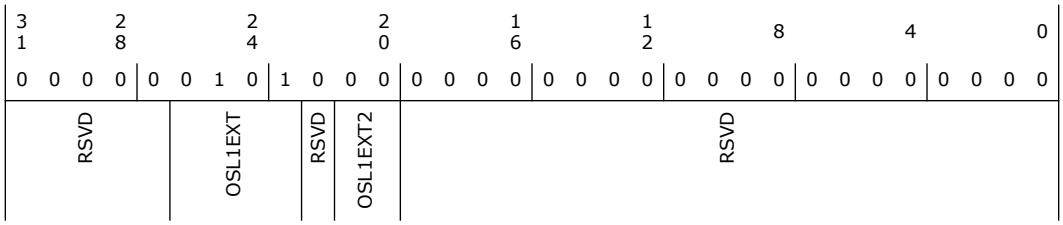
This register resides in Primary well (always on).

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 2800000h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	Reserved.
26:23	5h RW	**Output Stream L1 Exit Threshold (OSL1EXT):** This field determines the minimum amount of data (no. of frames) available in the output stream FIFO in which the Intel HD Audio controller will begin the signaling of DMI L1 exit event. If the value specified here is larger than the percentage L1 exit threshold specified in OSL1EXT2 field (or percentage L1 exit threshold is disabled), then the L1 exit threshold is equal to the value specified here. If the value specified here is smaller or equal to the percentage L1 exit threshold specified in the OSL1EXT2 field, then the L1 exit threshold is equal to the value specified in OSL1EXT2 field. This field only has effect when L1SEN bit is '1'. Bits Data Available (no. of frames) 0000 Reserved 0001 1 0010 2 ... ... 1111 15

Bit Range	Default & Access	Field Name (ID): Description
22	0h RO	Reserved.
21:20	0h RW	**Output Stream L1 Exit Threshold 2 (OSL1EXT2):** This field determines the amount of data (no. of frames) available in the output stream FIFO in which the PCH HD Audio controller will begin the signaling of percentage based DMI L1 exit event. If the value specified here is smaller or equal to the minimum L1 exit threshold specified in OSL1EXT field (or percentage L1 exit threshold is disabled), then the L1 exit threshold is equal to the value specified in OSL1EXT field. If the value specified here is larger than the minimum L1 exit threshold specified in the OSL1EXT field, then the L1 exit threshold is equal to the value specified in this field. 00: percentage L1 exit threshold disabled. 01: reserved 10: 1/8 of effective FIFO size. 11: 1/4 of effective FIFO size.
19:0	0h RO	Reserved.

6.1.40 Virtual Channel Enhanced Capability Header (VCCAP)—Offset 100h

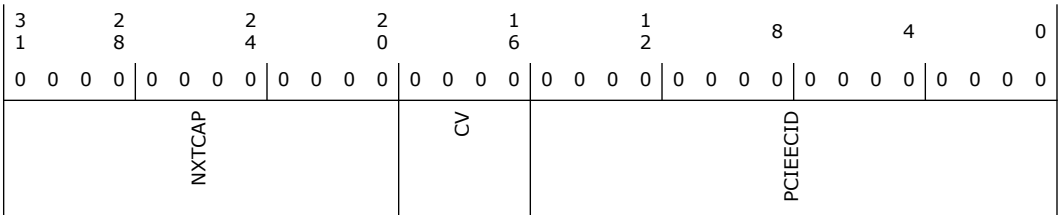
This register is not affected by D3HOT to D0 reset or FLR.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW/L	**Next Capability Offset (NXTCAP):** Points to the next capability header, which is the Root Complex Link Declaration Enhanced Capability Header. This register is RW/L to support removing the Root Complex Topology Capability from the PCI Express Extended Capability List. For systems which support the Root Complex Topology Capability Structure, boot BIOS should write a 130h to this register, otherwise boot BIOS should write a 000h to this register. Locked when FNCFG.BCLD = 1.
19:16	0h RW/L	**Capability Version (CV):** This register is RW/L to support removing the PCI Express Extended Capabilities from the Intel HD Audio subsystem. For systems which support the PCI Express Virtual Channel capability and the Root Complex Topology Capability Structure, boot BIOS should write a 1h to this register, otherwise boot BIOS should write a 0h to this register. Locked when FNCFG.BCLD = 1.
15:0	0h RW/L	**PCI Express Extended Capability ID (PCIEECID):** This register is RW/L to support removing the PCI Express Extended Capabilities from the Intel HD Audio subsysterm. For systems which support the PCI Express Virtual Channel capability and the Root Complex Topology Capability Structure, boot BIOS should write a 0002h to this register, otherwise boot BIOS should write a 0000h to this register. Locked when FNCFG.BCLD = 1.

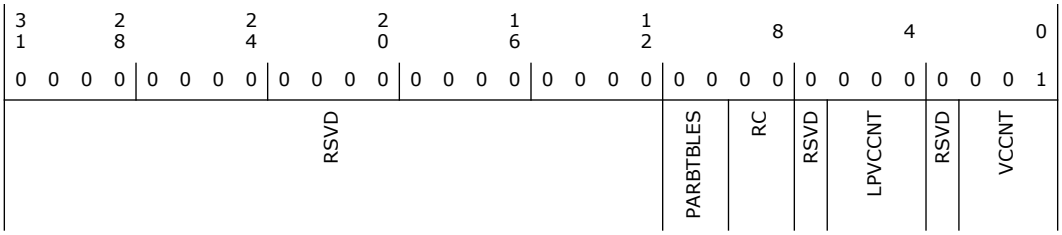
6.1.41 Port VC Capability Register 1 (PVCCAP1)—Offset 104h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 1h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	Reserved.
11:10	0h RO	**Port Arbitration Table Entry Size (PARBTBLES):** This is an endpoint device therefore this field is hardwired to 0 s.
9:8	0h RO	**Reference Clock (RC):** This is an endpoint device therefore this field is hardwired to 0 s.
7	0h RO	Reserved.
6:4	0h RO	**Low Priority Extended VC Count (LPVCCNT):** Indicates that only VC0 belongs to the low-priority VC group.
3	0h RO	Reserved.
2:0	1h RO	**Extended VC Count (VCCNT):** Indicates that one extended VC (in addition to VC0) is supported by the Intel(r) HD Audio controller.

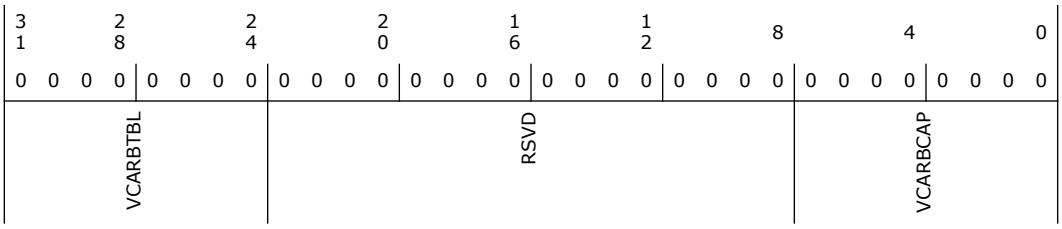
6.1.42 Port VC Capability Register 2 (PVCCAP2)—Offset 108h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**VC Arbitration Table Offset (VCARBTBL):** Hardwired to 0 indicating that a VC Arbitration Table is not present.
23:8	0h RO	Reserved.
7:0	0h RO	**VC Arbitration Capability (VCARBCAP):** Hardwired to 0 s. These bits are not applicable since the Intel HD Audio controller reports a 0 in the Low Priority Extended VC Count field.

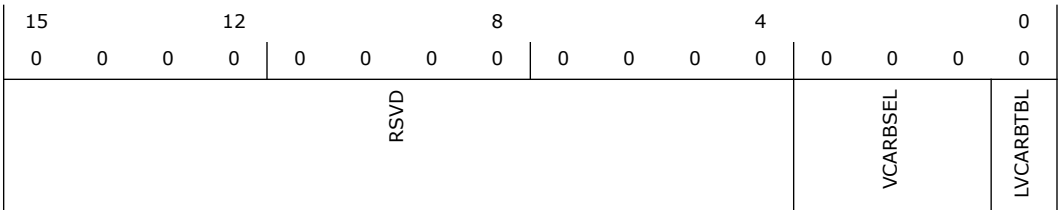
6.1.43 Port VC Control Register (PVCCTL)—Offset 10Ch

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:4	0h RO	Reserved.
3:1	0h RO	**VC Arbitration Select (VCARBSEL):** Hardwired to 0 s. Normally these bits are RW. But these bits are not applicable since the Intel HD Audio controller reports a 0 in the Low Priority Extended VC Count field.
0	0h RO	**Load VC Arbitration Table (LVCARBTBL):** Hardwired to 0 since an arbitration table is not present.

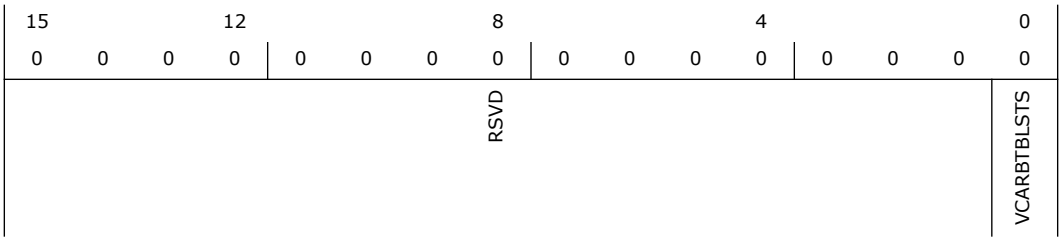
6.1.44 Port VC Status Register (PVCSTS)—Offset 10Eh

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:1	0h RO	Reserved.
0	0h RO	**VC Arbitration Table Status (VCARBTBLSTS):** Hardwired to 0 since the VC Arbitration Table is not present.

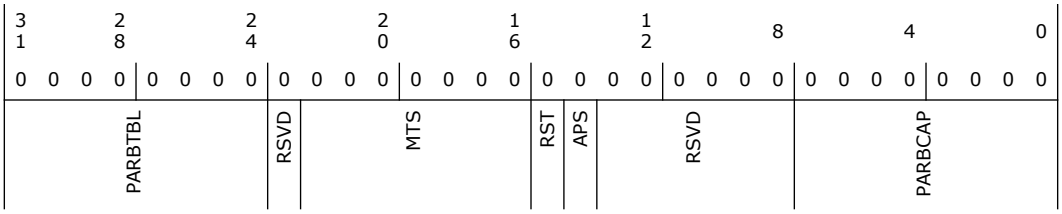
6.1.45 VC0 Resource Capability Register (VC0CAP)—Offset 110h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Port Arbitration Table Offset (PARBTBL):** Hardwired to 0 since this field is not valid for endpoint devices.
23	0h RO	Reserved.
22:16	0h RO	**Maximum Time Slots (MTS):** Hardwired to 0 since this field is not valid for endpoint devices.
15	0h RO	**Reject Snoop Transactions (RST):** Hardwired to 0 since this field is not valid for endpoint devices.
14	0h RO	**Advanced Packet Switching (APS):** Hardwired to 0 since this field is not valid for endpoint devices.
13:8	0h RO	Reserved.
7:0	0h RO	**Port Arbitration Capability (PARBCAP):** Hardwired to 0 since this field is not valid for endpoint devices.

6.1.46 VC0 Resource Control Register (VC0CTL)—Offset 114h

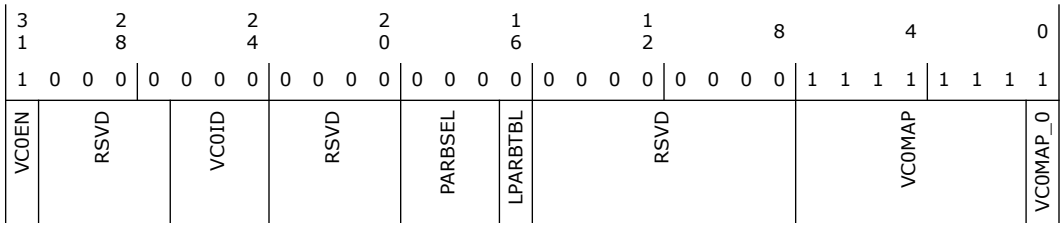
VC0MAP(7:1) field is not affected by FLR.
Implementation Notes: Due to legacy implementation of the VC0MAP field being implemented as reset by D3HOT to D0 Reset but not FLR and already work well with existing SW (and there is no clear definition in the PCI and PCIe Specification whether it should be reset by D3HOT to D0 Reset or not), this legacy implementation remains no change and documented here as reset by D3ONLY, which is a deviation from D3RST definition by excluding FLR.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 800000FFh



Bit Range	Default & Access	Field Name (ID): Description
31	1h RO	**VC0 Enable (VC0EN):** Hardwired to 1 for VC0.
30:27	0h RO	Reserved.
26:24	0h RO	**VC0 ID (VC0ID):** Hardwired to 0 since the first VC is always assigned as VC0.
23:20	0h RO	Reserved.
19:17	0h RO	**Port Arbitration Select (PARBSEL):** Hardwired to 0 since this field is not valid for endpoint devices.
16	0h RO	**Load Port Arbitration Table (LPARBTBL):** Hardwired to 0 since this field is not valid for endpoint devices.
15:8	0h RO	Reserved.
7:1	7Fh RW	**TC/VC0 Map (VC0MAP):** Bits (7:1) are implemented as R/W bits. This field is not used by the hardware, but it is RW to avoid confusing software.
0	1h RO	**TC/VC0 Map (VC0MAP_0):** Bit 0 is hardwired to 1 since TC0 is always mapped to VC0

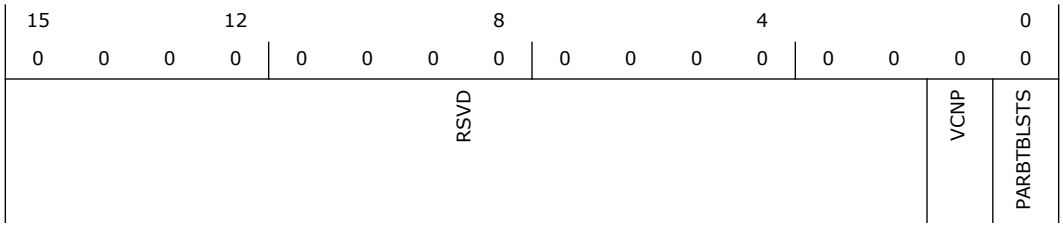
6.1.47 VC0 Resource Status Register (VC0STS)—Offset 11Ah

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:2	0h RO	Reserved.
1	0h RO	**VC0 Negotiation Pending (VCNP):** This bit does not apply to the integrated Intel HD Audio device and is therefore hardwired to 0.
0	0h RO	**Port Arbitration Table Status (PARBTBLSTS):** Hardwired to 0 since this field is not valid for endpoint devices.

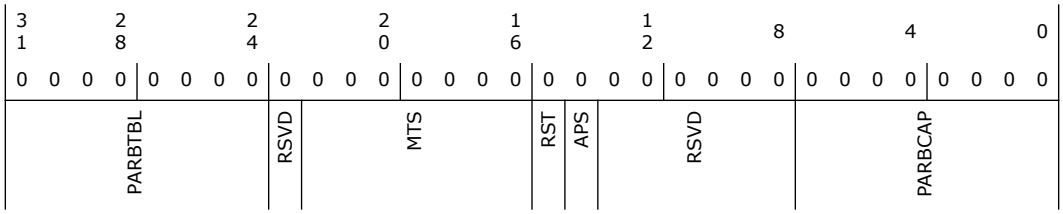
6.1.48 VCi Resource Capability Register (VCiCAP)—Offset 11Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Port Arbitration Table Offset (PARBTBL):** Hardwired to 0 since this field is not valid for endpoint devices.
23	0h RO	Reserved.
22:16	0h RO	**Maximum Time Slots (MTS):** Hardwired to 0 since this field is not valid for endpoint devices.
15	0h RO	**Reject Snoop Transactions (RST):** Hardwired to 0 since this field is not valid for endpoint devices.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RO	**Advanced Packet Switching (APS):** Hardwired to 0 since this field is not valid for endpoint devices.
13:8	0h RO	Reserved.
7:0	0h RO	**Port Arbitration Capability (PARBCAP):** Hardwired to 0 since this field is not valid for endpoint devices.

6.1.49 VCi Resource Control Register (VCiCTL)—Offset 120h

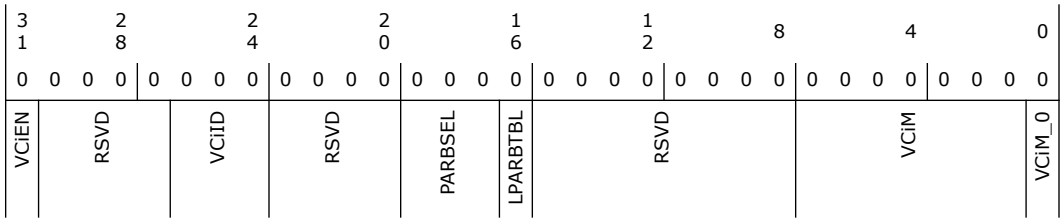
VCiEN bit and VCiID field are not affected by D3HOT to D0 Reset or FLR.
VCiM(7:1) field is not affected by FLR.
Implementation Notes: Due to legacy implementation of the VCiM field being implemented as reset by D3HOT to D0 Reset but not FLR and already work well with existing SW (and there is no clear definition in the PCI and PCIe Specification whether it should be reset by D3HOT to D0 Reset or not), this legacy implementation remains no change and documented here as reset by D3ONLY, which is a deviation from D3RST definition by excluding FLR.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**VCi Enable (VCiEN):** When set to 1, VCi is enabled. This bit is not affected by D3HOT to D0 reset.
30:27	0h RO	Reserved.
26:24	0h RW	**VCi ID (VCiID):** This fields assigns a VC ID to the VCi resource. This field is not used by the PCH hardware, but it is RW to avoid confusing software. These bits are not affected by D3HOT to D0 reset.
23:20	0h RO	Reserved.
19:17	0h RO	**Port Arbitration Select (PARBSEL):** Hardwired to 0 since this field is not valid for endpoint devices.
16	0h RO	**Load Port Arbitration Table (LPARBTBL):** Hardwired to 0 since this field is not valid for endpoint devices.

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	Reserved.
7:1	0h RW	**TC/VCi Map (VCiM):** This field indicates the TCs that are mapped to the VCi resource. Bits (7:1) are implemented as RW bits. This field is not used by the hardware, but it is RW to avoid confusing software.
0	0h RO	**TC/VCi Map (VCiM_0):** This field indicates the TCs that are mapped to the VCi resource. Bit 0 is hardwired to 0 indicating it can not be mapped to VCi. This field is not used by the hardware.

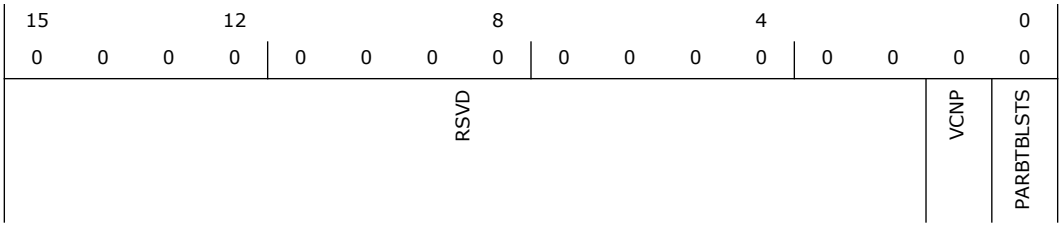
6.1.50 VCi Resource Status Register (VCiSTS)—Offset 126h

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:2	0h RO	Reserved.
1	0h RO	**VCi Negotiation Pending (VCNP):** This bit does not apply to the integrated Intel HD Audio subsystem and is therefore hardwired to 0.
0	0h RO	**Port Arbitration Table Status (PARBTBLSTS):** Hardwired to 0 since this field is not valid for endpoint devices.

6.1.51 Root Complex Link Declaration Enhanced (RCCAP)—Offset 130h

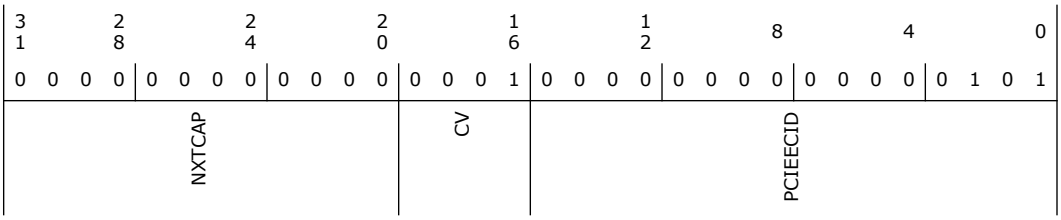
Capability Header

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 10005h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Next Capability Offset (NXTCAP):** Indicates this is the last capability.
19:16	1h RO	**Capability Version (CV)**
15:0	5h RO	**PCI Express Extended Capability ID (PCIEECID)**

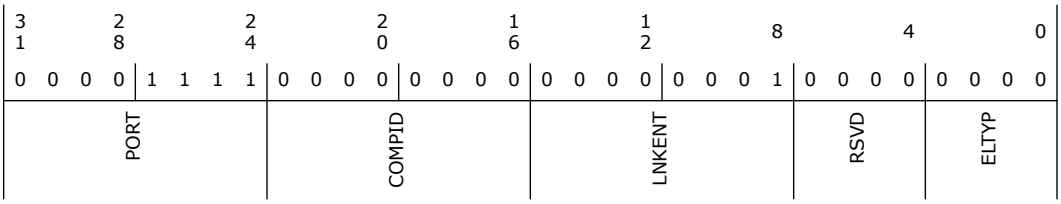
6.1.52 Element Self Description (ESD)—Offset 134h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 3

Default: F000100h



Bit Range	Default & Access	Field Name (ID): Description
31:24	Fh RO	**Port Number (PORT):** Intel HD Audio assigned as Port #15.
23:16	0h RW/L	**Component ID (COMPID):** Indicates the component ID assigned to this element by software. This is written once by platform BIOS and is locked until a platform reset. Locked when FNCFG.BCLD = 1.
15:8	1h RO	**Number of Link Entries (LNKENT):** The Intel HD Audio controller only connects to one device, the SOC egress port. Therefore this field reports a value of 1.
7:4	0h RO	Reserved.
3:0	0h RO	**Element Type (ELTYP):** The Intel HD Audio controller is an Integrated Root Complex Device. Therefore this field reports a value of 0h.

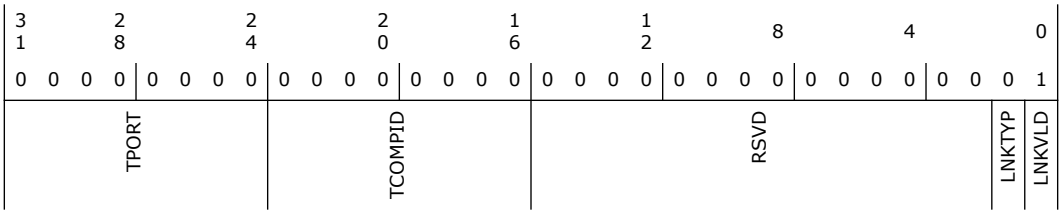
6.1.53 Link 1 Description (L1DESC)—Offset 140h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 1h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Target Port Number (TPORT):** The Intel HD Audio controller targets the SOC RCRB egress port, which is port #0.
23:16	0h RW/L	**Target Component ID (TCOMPID):** This field is programmed by platform BIOS to match the component ID of the SOC RCRB that is attached to this RCRB Locked when FNCFG.BCLD = 1.
15:2	0h RO	Reserved.
1	0h RO	**Link Type (LNKTYP):** Indicates Type 0.
0	1h RO	**Link Valid (LNKVLD):** Hardwired to 1.

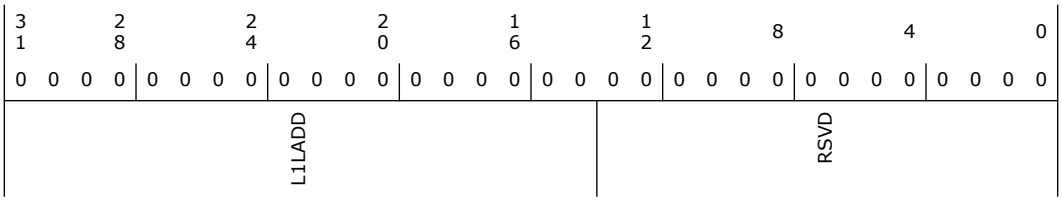
6.1.54 Link 1 Lower Address (L1LADD)—Offset 148h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO/V	**Link 1 Lower Address (L1LADD):** Hardwired to match the RCBA register value in the PCI-LPC bridge.
13:0	0h RO	Reserved.

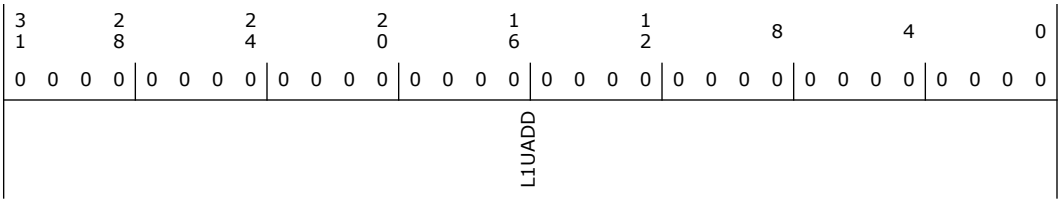
6.1.55 Link 1 Upper Address (L1UADD)—Offset 14Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Link 1 Upper Address (L1UADD):** Hardwired to match the RCBA register value in the PCI-LPC bridge.

6.2 High Definition Audio (D31:F3) Memory Mapped I/O Registers Summary

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	1h	Global Capabilities (GCAP)—Offset 0h	9701h
2h	2h	Minor Version (VMIN)—Offset 2h	0h
3h	3h	Major Version (VMAJ)—Offset 3h	1h
4h	5h	Output Payload Capability (OUTPAY)—Offset 4h	3Ch
6h	7h	Input Payload Capability (INPAY)—Offset 6h	1Dh
8h	Bh	Global Control (GCTL)—Offset 8h	0h
Ch	Dh	Wake Enable (WAKEEN)—Offset Ch	0h
Eh	Fh	Wake Status (WAKESTS)—Offset Eh	0h
12h	13h	Global Capabilities 2 (GCAP2)—Offset 12h	1h
14h	15h	Linked List Capabilities Header (LLCH)—Offset 14h	C00h
18h	19h	Output Stream Payload Capability (OUTSTRMPAY)—Offset 18h	30h
1Ah	1Bh	Input Stream Payload Capability (INSTRMPAY)—Offset 1Ah	18h
20h	23h	Interrupt Control (INTCTL)—Offset 20h	0h
24h	27h	Interrupt Status (INTSTS)—Offset 24h	0h
30h	33h	Wall Clock Counter (WALCLK)—Offset 30h	0h
38h	3Bh	Stream Synchronization (SSYNC)—Offset 38h	0h
40h	43h	CORB Lower Base Address (CORBLBASE)—Offset 40h	0h
44h	47h	CORB Upper Base Address (CORBUBASE)—Offset 44h	0h
48h	49h	CORB Write Pointer (CORBWP)—Offset 48h	0h

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
4Ah	4Bh	CORB Read Pointer (CORBRP)—Offset 4Ah	0h
4Ch	4Ch	CORB Control (CORBCTL)—Offset 4Ch	0h
4Dh	4Dh	CORB Status (CORBSTS)—Offset 4Dh	0h
4Eh	4Eh	CORB Size (CORBSIZE)—Offset 4Eh	42h
50h	53h	RIRB Lower Base Address (RIRBLBASE)—Offset 50h	0h
54h	57h	RIRB Upper Base Address (RIRBUBASE)—Offset 54h	0h
58h	59h	RIRB Write Pointer (RIRBWP)—Offset 58h	0h
5Ah	5Bh	Response Interrupt Count (RINTCNT)—Offset 5Ah	0h
5Ch	5Ch	RIRB Control (RIRBCTL)—Offset 5Ch	0h
5Dh	5Dh	RIRB Status (RIRBSTS)—Offset 5Dh	0h
5Eh	5Eh	RIRB Size (RIRBSIZE)—Offset 5Eh	42h
60h	63h	Immediate Command (IC)—Offset 60h	0h
64h	67h	Immediate Response (IR)—Offset 64h	0h
70h	73h	DMA Position Lower Base Address (DPLBASE)—Offset 70h	0h
74h	77h	DMA Position Upper Base Address (DPUBASE)—Offset 74h	0h
80h	83h	Input/Output Stream Descriptor x Control (ISD0CTL)—Offset 80h	40000h
83h	83h	Stream Descriptor Status (ISD0STS)—Offset 83h	0h
84h	87h	Input/Output Stream Descriptor x Link Position in Buffer (ISD0LPIB)—Offset 84h	0h
88h	8Bh	Input/Output Stream Descriptor x Cyclic Buffer Length (ISD0CBL)—Offset 88h	0h
8Ch	8Dh	Input/Output Stream Descriptor x Last Valid Index (ISD0LVI)—Offset 8Ch	0h
8Eh	8Fh	Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD0FIFOW)—Offset 8Eh	4h
90h	91h	Input/Output Stream Descriptor x FIFO Size (ISD0FIFOS)—Offset 90h	0h
92h	93h	Input/Output Stream Descriptor x Format (ISD0FMT)—Offset 92h	0h
94h	95h	Input/Output Stream Descriptor x FIFO Limit (ISD0FIFOL)—Offset 94h	0h
98h	9Bh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD0BDLPLBA)—Offset 98h	0h
9Ch	9Fh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD0BDLPUBA)—Offset 9Ch	0h
164h	167h	Input/Output Stream Descriptor x Link Position in Buffer (OSD0LPIB)—Offset 164h	0h
168h	16Bh	Input/Output Stream Descriptor x Cyclic Buffer Length (OSD0CBL)—Offset 168h	0h
16Ch	16Dh	Input/Output Stream Descriptor x Last Valid Index (OSD0LVI)—Offset 16Ch	0h
16Eh	16Fh	Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD0FIFOW)—Offset 16Eh	4h
170h	171h	Input/Output Stream Descriptor x FIFO Size (OSD0FIFOS)—Offset 170h	0h
172h	173h	Input/Output Stream Descriptor x Format (OSD0FMT)—Offset 172h	0h
174h	175h	Input/Output Stream Descriptor x FIFO Limit (OSD0FIFOL)—Offset 174h	0h
178h	17Bh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD0BDLPLBA)—Offset 178h	0h

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
17Ch	17Fh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD0BDLPUBA)—Offset 17Ch	0h
4DCh	4DFh	Global Time Synchronization Capture Control (GTSCC2)—Offset 4DCh	0h
4E0h	4E3h	Wall Frame Counter Captured (WALFCC2)—Offset 4E0h	0h
4E4h	4E7h	Time Stamp Counter Captured Lower (TSCCL2)—Offset 4E4h	0h
4E8h	4EBh	Time Stamp Counter Captured Upper (TSCCU2)—Offset 4E8h	0h
4ECh	4EFh	Linear Link Position Frame Offset Captured (LLPFOC2)—Offset 4ECh	0h
4F0h	4F3h	Linear Link Position Captured Lower (LLPCL2)—Offset 4F0h	0h
4F4h	4F7h	Linear Link Position Captured Upper (LLPCU2)—Offset 4F4h	0h
500h	503h	Global Time Synchronization Capability Header (GTSCH)—Offset 500h	11F00h
504h	507h	Global Time Synchronization Capability Declaration (GTSCD)—Offset 504h	0h
50Ch	50Fh	Global Time Synchronization Controller Adjust Control (GTSCTLAC)—Offset 50Ch	0h
520h	523h	Global Time Synchronization Capture Control (GTSCC0)—Offset 520h	0h
524h	527h	Wall Frame Counter Captured (WALFCC0)—Offset 524h	0h
528h	52Bh	Time Stamp Counter Captured Lower (TSCCL0)—Offset 528h	0h
52Ch	52Fh	Time Stamp Counter Captured Upper (TSCCU0)—Offset 52Ch	0h
534h	537h	Linear Link Position Frame Offset Captured (LLPFOC0)—Offset 534h	0h
538h	53Bh	Linear Link Position Captured Lower (LLPCL0)—Offset 538h	0h
53Ch	53Fh	Linear Link Position Captured Upper (LLPCU0)—Offset 53Ch	0h
540h	543h	Global Time Synchronization Capture Control (GTSCC1)—Offset 540h	0h
544h	547h	Wall Frame Counter Captured (WALFCC1)—Offset 544h	0h
548h	54Bh	Time Stamp Counter Captured Lower (TSCCL1)—Offset 548h	0h
54Ch	54Fh	Time Stamp Counter Captured Upper (TSCCU1)—Offset 54Ch	0h
554h	557h	Linear Link Position Frame Offset Captured (LLPFOC1)—Offset 554h	0h
558h	55Bh	Linear Link Position Captured Lower (LLPCL1)—Offset 558h	0h
55Ch	55Fh	Linear Link Position Captured Upper (LLPCU1)—Offset 55Ch	0h
800h	803h	Processing Pipe Capability Header (PPCH)—Offset 800h	30500h
804h	807h	Processing Pipe Control (PPCTL)—Offset 804h	0h
810h	813h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC0LLPL)—Offset 810h	0h
814h	817h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC0LLPU)—Offset 814h	0h
818h	81Bh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC0LDPL)—Offset 818h	0h
81Ch	81Fh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC0LDPU)—Offset 81Ch	0h
820h	823h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC1LLPL)—Offset 820h	0h
824h	827h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC1LLPU)—Offset 824h	0h
828h	82Bh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC1LDPL)—Offset 828h	0h
82Ch	82Fh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC1LDPU)—Offset 82Ch	0h

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
830h	833h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC2LLPL)—Offset 830h	0h
834h	837h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC2LLPU)—Offset 834h	0h
838h	83Bh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC2LDPL)—Offset 838h	0h
83Ch	83Fh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC2LDPU)—Offset 83Ch	0h
840h	843h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC3LLPL)—Offset 840h	0h
844h	847h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC3LLPU)—Offset 844h	0h
848h	84Bh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC3LDPL)—Offset 848h	0h
84Ch	84Fh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC3LDPU)—Offset 84Ch	0h
850h	853h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC4LLPL)—Offset 850h	0h
854h	857h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC4LLPU)—Offset 854h	0h
858h	85Bh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC4LDPL)—Offset 858h	0h
85Ch	85Fh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC4LDPU)—Offset 85Ch	0h
860h	863h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC5LLPL)—Offset 860h	0h
864h	867h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC5LLPU)—Offset 864h	0h
868h	86Bh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC5LDPL)—Offset 868h	0h
86Ch	86Fh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC5LDPU)—Offset 86Ch	0h
870h	873h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC6LLPL)—Offset 870h	0h
874h	877h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC6LLPU)—Offset 874h	0h
878h	87Bh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC6LDPL)—Offset 878h	0h
87Ch	87Fh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC6LDPU)—Offset 87Ch	0h
880h	883h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC0LLPL)—Offset 880h	0h
884h	887h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC0LLPU)—Offset 884h	0h
888h	88Bh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC0LDPL)—Offset 888h	0h
88Ch	88Fh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC0LDPU)—Offset 88Ch	0h
890h	893h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC1LLPL)—Offset 890h	0h
894h	897h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC1LLPU)—Offset 894h	0h

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
898h	89Bh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC1LDPL)—Offset 898h	0h
89Ch	89Fh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC1LDPU)—Offset 89Ch	0h
8A0h	8A3h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC2LLPL)—Offset 8A0h	0h
8A4h	8A7h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC2LLPU)—Offset 8A4h	0h
8A8h	8ABh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC2LDPL)—Offset 8A8h	0h
8ACh	8AFh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC2LDPU)—Offset 8ACh	0h
8B0h	8B3h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC3LLPL)—Offset 8B0h	0h
8B4h	8B7h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC3LLPU)—Offset 8B4h	0h
8B8h	8BBh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC3LDPL)—Offset 8B8h	0h
8BCh	8BFh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC3LDPU)—Offset 8BCh	0h
8C0h	8C3h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC4LLPL)—Offset 8C0h	0h
8C4h	8C7h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC4LLPU)—Offset 8C4h	0h
8C8h	8CBh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC4LDPL)—Offset 8C8h	0h
8CCh	8CFh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC4LDPU)—Offset 8CCh	0h
8D0h	8D3h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC5LLPL)—Offset 8D0h	0h
8D4h	8D7h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC5LLPU)—Offset 8D4h	0h
8D8h	8DBh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC5LDPL)—Offset 8D8h	0h
8DCh	8DFh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC5LDPU)—Offset 8DCh	0h
8E0h	8E3h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC6LLPL)—Offset 8E0h	0h
8E4h	8E7h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC6LLPU)—Offset 8E4h	0h
8E8h	8EBh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC6LDPL)—Offset 8E8h	0h
8ECh	8EFh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC6LDPU)—Offset 8ECh	0h
8F0h	8F3h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC7LLPL)—Offset 8F0h	0h
8F4h	8F7h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC7LLPU)—Offset 8F4h	0h
8F8h	8FBh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC7LDPL)—Offset 8F8h	0h
8FCh	8FFh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC7LDPU)—Offset 8FCh	0h

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
900h	903h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC8LLPL)—Offset 900h	0h
904h	907h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC8LLPU)—Offset 904h	0h
908h	90Bh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC8LDPL)—Offset 908h	0h
90Ch	90Fh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC8LDPU)—Offset 90Ch	0h
910h	913h	Input/Output Processing Pipe's Link Connection x Control (IPPLC0CTL)—Offset 910h	0h
914h	915h	Input/Output Processing Pipe's Link Connection x Format (IPPLC0FMT)—Offset 914h	0h
918h	91Bh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC0LLPL)—Offset 918h	0h
91Ch	91Fh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC0LLPU)—Offset 91Ch	0h
920h	923h	Input/Output Processing Pipe's Link Connection x Control (IPPLC1CTL)—Offset 920h	0h
924h	925h	Input/Output Processing Pipe's Link Connection x Format (IPPLC1FMT)—Offset 924h	0h
928h	92Bh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC1LLPL)—Offset 928h	0h
92Ch	92Fh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC1LLPU)—Offset 92Ch	0h
930h	933h	Input/Output Processing Pipe's Link Connection x Control (IPPLC2CTL)—Offset 930h	0h
934h	935h	Input/Output Processing Pipe's Link Connection x Format (IPPLC2FMT)—Offset 934h	0h
938h	93Bh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC2LLPL)—Offset 938h	0h
93Ch	93Fh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC2LLPU)—Offset 93Ch	0h
940h	943h	Input/Output Processing Pipe's Link Connection x Control (IPPLC3CTL)—Offset 940h	0h
944h	945h	Input/Output Processing Pipe's Link Connection x Format (IPPLC3FMT)—Offset 944h	0h
948h	94Bh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC3LLPL)—Offset 948h	0h
94Ch	94Fh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC3LLPU)—Offset 94Ch	0h
950h	953h	Input/Output Processing Pipe's Link Connection x Control (IPPLC4CTL)—Offset 950h	0h
954h	955h	Input/Output Processing Pipe's Link Connection x Format (IPPLC4FMT)—Offset 954h	0h
958h	95Bh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC4LLPL)—Offset 958h	0h
95Ch	95Fh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC4LLPU)—Offset 95Ch	0h
960h	963h	Input/Output Processing Pipe's Link Connection x Control (IPPLC5CTL)—Offset 960h	0h
964h	965h	Input/Output Processing Pipe's Link Connection x Format (IPPLC5FMT)—Offset 964h	0h

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
968h	96Bh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC5LLPL)—Offset 968h	0h
96Ch	96Fh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC5LLPU)—Offset 96Ch	0h
970h	973h	Input/Output Processing Pipe's Link Connection x Control (IPPLC6CTL)—Offset 970h	0h
974h	975h	Input/Output Processing Pipe's Link Connection x Format (IPPLC6FMT)—Offset 974h	0h
978h	97Bh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC6LLPL)—Offset 978h	0h
97Ch	97Fh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC6LLPU)—Offset 97Ch	0h
980h	983h	Input/Output Processing Pipe's Link Connection x Control (OPPLC0CTL)—Offset 980h	0h
984h	985h	Input/Output Processing Pipe's Link Connection x Format (OPPLC0FMT)—Offset 984h	0h
988h	98Bh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC0LLPL)—Offset 988h	0h
98Ch	98Fh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC0LLPU)—Offset 98Ch	0h
990h	993h	Input/Output Processing Pipe's Link Connection x Control (OPPLC1CTL)—Offset 990h	0h
994h	995h	Input/Output Processing Pipe's Link Connection x Format (OPPLC1FMT)—Offset 994h	0h
998h	99Bh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC1LLPL)—Offset 998h	0h
99Ch	99Fh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC1LLPU)—Offset 99Ch	0h
9A0h	9A3h	Input/Output Processing Pipe's Link Connection x Control (OPPLC2CTL)—Offset 9A0h	0h
9A4h	9A5h	Input/Output Processing Pipe's Link Connection x Format (OPPLC2FMT)—Offset 9A4h	0h
9A8h	9ABh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC2LLPL)—Offset 9A8h	0h
9ACh	9AFh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC2LLPU)—Offset 9ACh	0h
9B0h	9B3h	Input/Output Processing Pipe's Link Connection x Control (OPPLC3CTL)—Offset 9B0h	0h
9B4h	9B5h	Input/Output Processing Pipe's Link Connection x Format (OPPLC3FMT)—Offset 9B4h	0h
9B8h	9BBh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC3LLPL)—Offset 9B8h	0h
9BCh	9BFh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC3LLPU)—Offset 9BCh	0h
9C0h	9C3h	Input/Output Processing Pipe's Link Connection x Control (OPPLC4CTL)—Offset 9C0h	0h
9C4h	9C5h	Input/Output Processing Pipe's Link Connection x Format (OPPLC4FMT)—Offset 9C4h	0h
9C8h	9CBh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC4LLPL)—Offset 9C8h	0h
9CCh	9CFh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC4LLPU)—Offset 9CCh	0h

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
9D0h	9D3h	Input/Output Processing Pipe's Link Connection x Control (OPPLC5CTL)—Offset 9D0h	0h
9D4h	9D5h	Input/Output Processing Pipe's Link Connection x Format (OPPLC5FMT)—Offset 9D4h	0h
9D8h	9DBh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC5LLPL)—Offset 9D8h	0h
9DCh	9DFh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC5LLPU)—Offset 9DCh	0h
9E0h	9E3h	Input/Output Processing Pipe's Link Connection x Control (OPPLC6CTL)—Offset 9E0h	0h
9E4h	9E5h	Input/Output Processing Pipe's Link Connection x Format (OPPLC6FMT)—Offset 9E4h	0h
9E8h	9EBh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC6LLPL)—Offset 9E8h	0h
9ECh	9EFh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC6LLPU)—Offset 9ECh	0h
9F0h	9F3h	Input/Output Processing Pipe's Link Connection x Control (OPPLC7CTL)—Offset 9F0h	0h
9F4h	9F5h	Input/Output Processing Pipe's Link Connection x Format (OPPLC7FMT)—Offset 9F4h	0h
9F8h	9FBh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC7LLPL)—Offset 9F8h	0h
9FCh	9FFh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC7LLPU)—Offset 9FCh	0h
A00h	A03h	Input/Output Processing Pipe's Link Connection x Control (OPPLC8CTL)—Offset A00h	0h
A04h	A05h	Input/Output Processing Pipe's Link Connection x Format (OPPLC8FMT)—Offset A04h	0h
A08h	A0Bh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC8LLPL)—Offset A08h	0h
A0Ch	A0Fh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC8LLPU)—Offset A0Ch	0h
4A10h	4A13h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC7LLPL)—Offset 4A10h	0h
4A14h	4A17h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC7LLPU)—Offset 4A14h	0h
4A18h	4A1Bh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC7LDPL)—Offset 4A18h	0h
4A1Ch	4A1Fh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC7LDPU)—Offset 4A1Ch	0h
4A20h	4A23h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC8LLPL)—Offset 4A20h	0h
4A24h	4A27h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC8LLPU)—Offset 4A24h	0h
4A28h	4A2Bh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC8LDPL)—Offset 4A28h	0h
4A2Ch	4A2Fh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC8LDPU)—Offset 4A2Ch	0h
4A30h	4A33h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC9LLPL)—Offset 4A30h	0h
4A34h	4A37h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC9LLPU)—Offset 4A34h	0h

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
4A38h	4A3Bh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC9LDPL)—Offset 4A38h	0h
4A3Ch	4A3Fh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC9LDPU)—Offset 4A3Ch	0h
4A40h	4A43h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC10LLPL)—Offset 4A40h	0h
4A44h	4A47h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC10LLPU)—Offset 4A44h	0h
4A48h	4A4Bh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC10LDPL)—Offset 4A48h	0h
4A4Ch	4A4Fh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC10LDPU)—Offset 4A4Ch	0h
4A50h	4A53h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC11LLPL)—Offset 4A50h	0h
4A54h	4A57h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC11LLPU)—Offset 4A54h	0h
4A58h	4A5Bh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC11LDPL)—Offset 4A58h	0h
4A5Ch	4A5Fh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC11LDPU)—Offset 4A5Ch	0h
4A60h	4A63h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC12LLPL)—Offset 4A60h	0h
4A64h	4A67h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC12LLPU)—Offset 4A64h	0h
4A68h	4A6Bh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC12LDPL)—Offset 4A68h	0h
4A6Ch	4A6Fh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC12LDPU)—Offset 4A6Ch	0h
4A70h	4A73h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC13LLPL)—Offset 4A70h	0h
4A74h	4A77h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC13LLPU)—Offset 4A74h	0h
4A78h	4A7Bh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC13LDPL)—Offset 4A78h	0h
4A7Ch	4A7Fh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC13LDPU)—Offset 4A7Ch	0h
4A80h	4A83h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC14LLPL)—Offset 4A80h	0h
4A84h	4A87h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC14LLPU)—Offset 4A84h	0h
4A88h	4A8Bh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC14LDPL)—Offset 4A88h	0h
4A8Ch	4A8Fh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC14LDPU)—Offset 4A8Ch	0h
4A90h	4A93h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC9LLPL)—Offset 4A90h	0h
4A94h	4A97h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC9LLPU)—Offset 4A94h	0h
4A98h	4A9Bh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC9LDPL)—Offset 4A98h	0h
4A9Ch	4A9Fh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC9LDPU)—Offset 4A9Ch	0h

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
4AA0h	4AA3h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC10LLPL)—Offset 4AA0h	0h
4AA4h	4AA7h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC10LLPU)—Offset 4AA4h	0h
4AA8h	4AABh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC10LDPL)—Offset 4AA8h	0h
4AACh	4AAFh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC10LDPU)—Offset 4AACh	0h
4AB0h	4AB3h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC11LLPL)—Offset 4AB0h	0h
4AB4h	4AB7h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC11LLPU)—Offset 4AB4h	0h
4AB8h	4ABBh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC11LDPL)—Offset 4AB8h	0h
4ABCh	4ABFh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC11LDPU)—Offset 4ABCh	0h
4AC0h	4AC3h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC12LLPL)—Offset 4AC0h	0h
4AC4h	4AC7h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC12LLPU)—Offset 4AC4h	0h
4AC8h	4ACBh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC12LDPL)—Offset 4AC8h	0h
4ACCh	4ACFh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC12LDPU)—Offset 4ACCh	0h
4AD0h	4AD3h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC13LLPL)—Offset 4AD0h	0h
4AD4h	4AD7h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC13LLPU)—Offset 4AD4h	0h
4AD8h	4ADBh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC13LDPL)—Offset 4AD8h	0h
4ADCh	4ADFh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC13LDPU)—Offset 4ADCh	0h
4AE0h	4AE3h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC14LLPL)—Offset 4AE0h	0h
4AE4h	4AE7h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC14LLPU)—Offset 4AE4h	0h
4AE8h	4AEBh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC14LDPL)—Offset 4AE8h	0h
4AECh	4AEFh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC14LDPU)—Offset 4AECh	0h
4AF0h	4AF3h	Input/Output Processing Pipe's Link Connection x Control (IPPLC7CTL)—Offset 4AF0h	0h
4AF4h	4AF5h	Input/Output Processing Pipe's Link Connection x Format (IPPLC7FMT)—Offset 4AF4h	0h
4AF8h	4AFBh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC7LLPL)—Offset 4AF8h	0h
4AFCh	4AFFh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC7LLPU)—Offset 4AFCh	0h
4B00h	4B03h	Input/Output Processing Pipe's Link Connection x Control (IPPLC8CTL)—Offset 4B00h	0h
4B04h	4B05h	Input/Output Processing Pipe's Link Connection x Format (IPPLC8FMT)—Offset 4B04h	0h

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
4B08h	4B0Bh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC8LLPL)—Offset 4B08h	0h
4B0Ch	4B0Fh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC8LLPU)—Offset 4B0Ch	0h
4B10h	4B13h	Input/Output Processing Pipe's Link Connection x Control (IPPLC9CTL)—Offset 4B10h	0h
4B14h	4B15h	Input/Output Processing Pipe's Link Connection x Format (IPPLC9FMT)—Offset 4B14h	0h
4B18h	4B1Bh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC9LLPL)—Offset 4B18h	0h
4B1Ch	4B1Fh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC9LLPU)—Offset 4B1Ch	0h
4B20h	4B23h	Input/Output Processing Pipe's Link Connection x Control (IPPLC10CTL)—Offset 4B20h	0h
4B24h	4B25h	Input/Output Processing Pipe's Link Connection x Format (IPPLC10FMT)—Offset 4B24h	0h
4B28h	4B2Bh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC10LLPL)—Offset 4B28h	0h
4B2Ch	4B2Fh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC10LLPU)—Offset 4B2Ch	0h
4B30h	4B33h	Input/Output Processing Pipe's Link Connection x Control (IPPLC11CTL)—Offset 4B30h	0h
4B34h	4B35h	Input/Output Processing Pipe's Link Connection x Format (IPPLC11FMT)—Offset 4B34h	0h
4B38h	4B3Bh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC11LLPL)—Offset 4B38h	0h
4B3Ch	4B3Fh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC11LLPU)—Offset 4B3Ch	0h
4B40h	4B43h	Input/Output Processing Pipe's Link Connection x Control (IPPLC12CTL)—Offset 4B40h	0h
4B44h	4B45h	Input/Output Processing Pipe's Link Connection x Format (IPPLC12FMT)—Offset 4B44h	0h
4B48h	4B4Bh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC12LLPL)—Offset 4B48h	0h
4B4Ch	4B4Fh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC12LLPU)—Offset 4B4Ch	0h
4B50h	4B53h	Input/Output Processing Pipe's Link Connection x Control (IPPLC13CTL)—Offset 4B50h	0h
4B54h	4B55h	Input/Output Processing Pipe's Link Connection x Format (IPPLC13FMT)—Offset 4B54h	0h
4B58h	4B5Bh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC13LLPL)—Offset 4B58h	0h
4B5Ch	4B5Fh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC13LLPU)—Offset 4B5Ch	0h
4B60h	4B63h	Input/Output Processing Pipe's Link Connection x Control (IPPLC14CTL)—Offset 4B60h	0h
4B64h	4B65h	Input/Output Processing Pipe's Link Connection x Format (IPPLC14FMT)—Offset 4B64h	0h
4B68h	4B6Bh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC14LLPL)—Offset 4B68h	0h
4B6Ch	4B6Fh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC14LLPU)—Offset 4B6Ch	0h

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
4B70h	4B73h	Input/Output Processing Pipe's Link Connection x Control (OPPLC9CTL)—Offset 4B70h	0h
4B74h	4B75h	Input/Output Processing Pipe's Link Connection x Format (OPPLC9FMT)—Offset 4B74h	0h
4B78h	4B7Bh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC9LLPL)—Offset 4B78h	0h
4B7Ch	4B7Fh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC9LLPU)—Offset 4B7Ch	0h
4B80h	4B83h	Input/Output Processing Pipe's Link Connection x Control (OPPLC10CTL)—Offset 4B80h	0h
4B84h	4B85h	Input/Output Processing Pipe's Link Connection x Format (OPPLC10FMT)—Offset 4B84h	0h
4B88h	4B8Bh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC10LLPL)—Offset 4B88h	0h
4B8Ch	4B8Fh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC10LLPU)—Offset 4B8Ch	0h
4B90h	4B93h	Input/Output Processing Pipe's Link Connection x Control (OPPLC11CTL)—Offset 4B90h	0h
4B94h	4B95h	Input/Output Processing Pipe's Link Connection x Format (OPPLC11FMT)—Offset 4B94h	0h
4B98h	4B9Bh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC11LLPL)—Offset 4B98h	0h
4B9Ch	4B9Fh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC11LLPU)—Offset 4B9Ch	0h
4BA0h	4BA3h	Input/Output Processing Pipe's Link Connection x Control (OPPLC12CTL)—Offset 4BA0h	0h
4BA4h	4BA5h	Input/Output Processing Pipe's Link Connection x Format (OPPLC12FMT)—Offset 4BA4h	0h
4BA8h	4BABh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC12LLPL)—Offset 4BA8h	0h
4BACh	4BAFh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC12LLPU)—Offset 4BACh	0h
4BB0h	4BB3h	Input/Output Processing Pipe's Link Connection x Control (OPPLC13CTL)—Offset 4BB0h	0h
4BB4h	4BB5h	Input/Output Processing Pipe's Link Connection x Format (OPPLC13FMT)—Offset 4BB4h	0h
4BB8h	4BBBh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC13LLPL)—Offset 4BB8h	0h
4BBCh	4BBFh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC13LLPU)—Offset 4BBCh	0h
4BC0h	4BC3h	Input/Output Processing Pipe's Link Connection x Control (OPPLC14CTL)—Offset 4BC0h	0h
4BC4h	4BC5h	Input/Output Processing Pipe's Link Connection x Format (OPPLC14FMT)—Offset 4BC4h	0h
4BC8h	4BCBh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC14LLPL)—Offset 4BC8h	0h
4BCCh	4BCFh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC14LLPU)—Offset 4BCCh	0h

6.2.1 Global Capabilities (GCAP)—Offset 0h

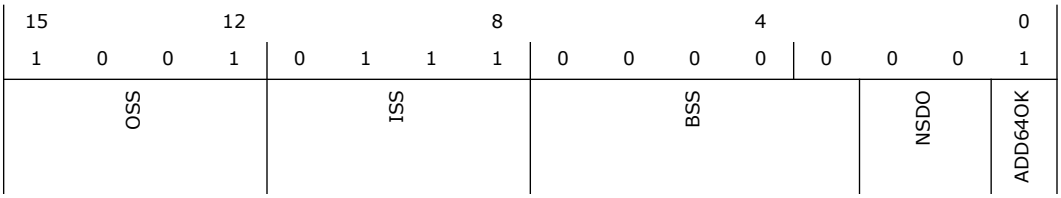
This register resides in Primary well (always on), or resides in Primary well (gated) with state retention, and reset by platform reset.

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 9701h



Bit Range	Default & Access	Field Name (ID): Description
15:12	9h RW/L	**Number of Output Streams Supported (OSS):** 0100b indicates that the Intel HD Audio controller supports four output streams. Locked when FNCFG.BCLD = 1.
11:8	7h RW/L	**Number of Input Streams Supported (ISS):** 0100b indicates that the Intel HD Audio controller supports four input streams. Locked when FNCFG.BCLD = 1.
7:3	0h RO	**Number of Bidirectional Streams Supported (BSS):** 00000b indicates that the Intel HD Audio controller supports 0 bidirectional streams.
2:1	0h RW/L	**Number of Serial Data Out Signals (NSDO):** 00b indicates that the Intel HD Audio controller supports one Serial Data Output signal. For the case of multiple link segments is supported, this field indicates the number of SDO for link 0. Locked when FNCFG.BCLD = 1.
0	1h RW/L	**64 Bit Address Supported (ADD64OK):** A 1 indicates that the Intel HD Audio controller supports 64 bit addressing for BDL addresses, data buffer addresses, and command buffer addresses. Locked when FNCFG.BCLD = 1.

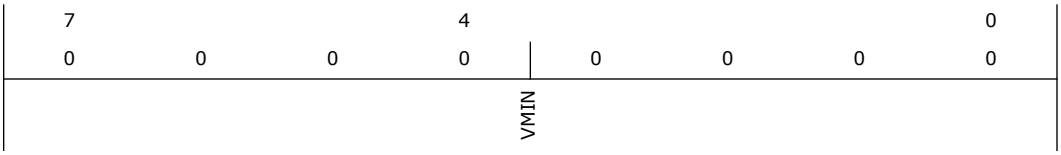
6.2.2 Minor Version (VMIN)—Offset 2h

Access Method

Type: MEM Register
(Size: 8 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RO	**Minor Version (VMIN):** Indicates the Intel HD Audio controller supports minor revision number 00h of the Intel HD Audio specification.

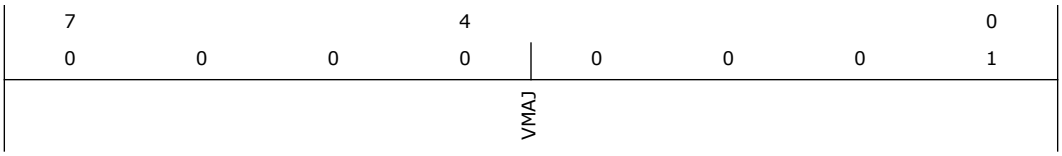
6.2.3 Major Version (VMAJ)—Offset 3h

Access Method

Type: MEM Register
(Size: 8 bits)

Device: 31
Function: 3

Default: 1h



Bit Range	Default & Access	Field Name (ID): Description
7:0	1h RO	**Major Version (VMAJ):** Indicates the Intel HD Audio controller supports major revision number 1 of the Intel HD Audio specification.

6.2.4 Output Payload Capability (OUTPAY)—Offset 4h

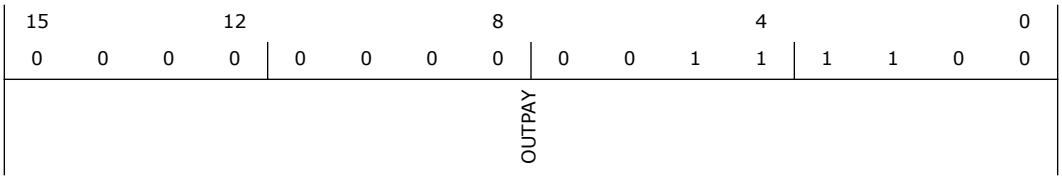
This register resides in Primary well (always on), or resides in Primary well (gated) with state retention, and reset by platform reset.

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 3Ch



Bit Range	Default & Access	Field Name (ID): Description
15:0	3Ch RW/L	**Output Payload Capability (OUTPAY):** Indicates the total output payload available on the link. This does not include bandwidth used for command and control. This measurement is in 16-bit word quantities per 48 kHz frame. The default link clock speed of 24.000 MHz (the data is double pumped) provides 1000 bits per frame, or 62.5 words in total. 40 bits are used for command and control, leaving 60 words available for data payload. Note that this value does not reflect any bandwidth increase due to support for multiple SDO lines. 00h: 0 words 01h: 1 word payload ... FFh: 255h word payload Note: In the event that multiple links is supported (GCAP2.LCOUNT) 0), the payload advertised will be the lowest common denominator offered by the default clock frequency on each link. Locked when FNCFG.BCLD = 1.

6.2.5 Input Payload Capability (INPAY)—Offset 6h

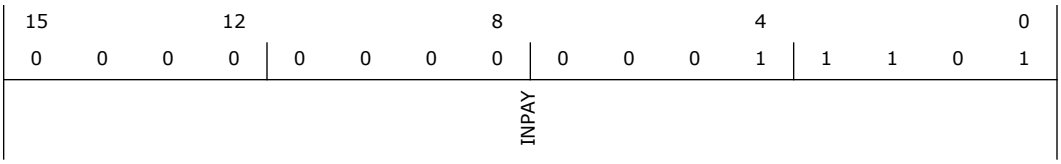
This register resides in Primary well (always on), or resides in Primary well (gated) with state retention, and reset by platform reset.

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 1Dh



Bit Range	Default & Access	Field Name (ID): Description
15:0	1Dh RW/L	**Input Payload Capability (INPAY):** Indicates the total input payload available on the link. This does not include bandwidth used for response. This measurement is in 16-bit word quantities per 48 kHz frame. The default link clock speed of 24.000 MHz provides 500 bits per frame, or 31.25 words in total. 36 bits are used for response, leaving 29 words for data payload. Note that this value does not reflect any bandwidth increase due to support for multiple SDI lines. 00h: 0 words 01h: 1 word payload ... FFh: 255h word payload Note: In the event that multiple links is supported (GCAP2.LCOUNT) 0), the payload advertised will be the lowest common denominator offered by the default clock frequency on each link. Locked when FNCFG.BCLD = 1.

6.2.6 Global Control (GCTL)—Offset 8h

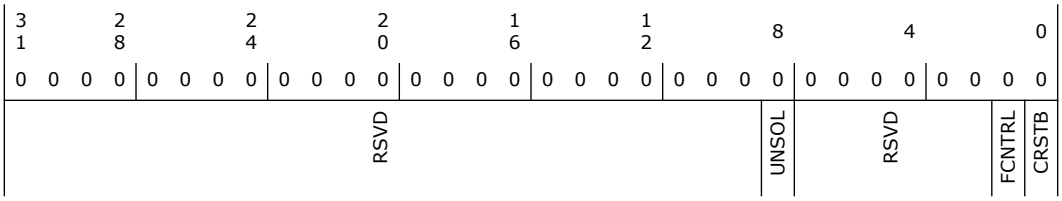
CRSTB bit is not affected by controller reset.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved (RSVD)**
8	0h RW	**Accept Unsolicited Response Enable (UNSOL):** If UNSOL is a 1, Unsolicited Responses from the codecs are accepted by the controller and placed into the Response Input Ring Buffer. If UNSOL is a 0, unsolicited responses are not accepted, and dropped on the floor.
7:2	0h RO	Reserved.
1	0h RW/1S/V	**Flush Control (FCNTRL):** Writing a 1 to this bit initiates a flush. When the flush completion is received by the controller, hardware sets the Flush Status bit and clears this Flush Control bit. Before a flush cycle is initiated, the DMA Position Buffer must be programmed with a valid memory address by software, but the DMA Position Buffer bit 0 need not be set to enable the position reporting mechanism. Also, all streams must be stopped (the associated RUN bit must be 0). When the flush is initiated, the controller will flush pipelines to memory to guarantee that the hardware is ready to transition to a D3 state. Setting this bit is not a critical step in the power state transition if the content of the FIFOs is not critical.
0	0h RW/V	**Controller Reset# (CRSTB):** After the hardware has completed sequencing into the reset state, it will report a 0 in this bit. Software must read a 0 from this bit to verify that the controller is in reset. Writing a 1 to this bit causes the controller to exit its reset state and deassert the Intel HD Audio link RESET# signal. Software is responsible for setting/clearing this bit such that the minimum Intel HD Audio link RESET# signal assertion pulse width specification is met. When the controller hardware is ready to begin operation, it will report a 1 in this bit. Software must read a 1 from this bit before accessing any controller registers. The CRST bit defaults to a 0 after hardware reset, therefore software needs to write a 1 to this bit to begin operation. Note that the CORB/RIRB RUN bits and all Stream RUN bits must be verified cleared to zero before CRST bit is written to 0 (asserted) in order to assure a clean re-start. When setting or clearing CRST, software must ensure that minimum link timing requirements (minimum RESET# assertion time, etc.) are met. When CRST is 0 indicating that the controller is in reset, writes to all Intel HD Audio memory mapped registers are ignored as if the device is not present. The only exception is the Global Control register containing the CRST bit itself. The Global Control register is write-able as a DWord, Word, or Byte even when CRST is 0 if the byte enable for the byte containing the CRST bit (Byte Enable 0) is active. If Byte Enable 0 is not active, writes to the Global Control register will be ignored when CRST is 0. When CRST is 0, reads to Intel HD Audio memory mapped registers will return their default value except for registers that are not reset with PLTRST# or on a D3hot to D0 transition.

6.2.7 Wake Enable (WAKEEN)—Offset Ch

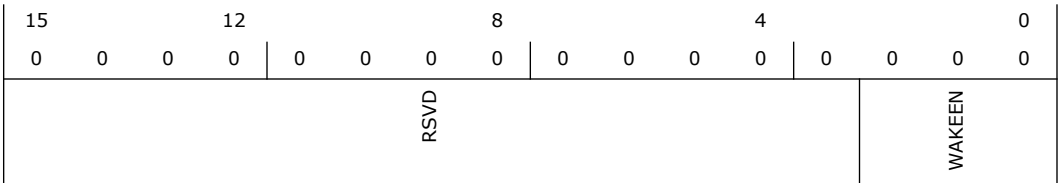
This register resides in Primary well (always on), or resides in Primary well (gated) with state retention, and reset by resume reset.
The number of WAKEEN bits in this register is depending on the total number of codec address implemented, represented as x in the register table.
The x value is determined by the parameter CADC. For SPT implementation, x = 4.

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:3	0h RO	Reserved.
2:0	0h RW	**SDIN Wake Enable Flags (WAKEEN):** Bits which control which SDI signal(s) may generate a wake event. A 1 bit in the bit mask indicates that the associated SDIN signal is enabled to generate a wake. These bits are cleared on a power-on reset. Software must not make assumptions about the reset state of these bits and must set them appropriately.

6.2.8 Wake Status (WAKESTS)—Offset Eh

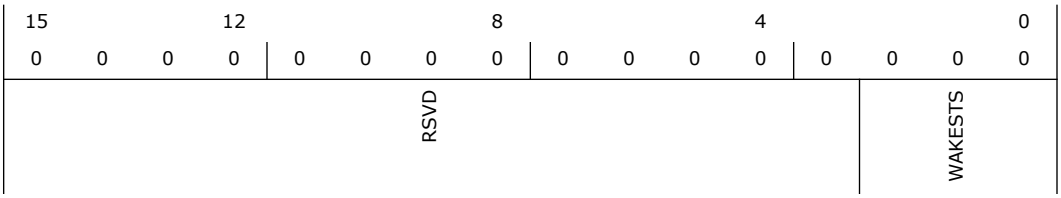
This register resides in Primary well (always on), and reset by resume reset.
The number of WAKESTS bits in this register is depending on the total number of codec address implemented, represented as x in the register table. The x value is determined by the parameter CADC. For SPT implementation, x = 4.

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:3	0h RO	Reserved.
2:0	0h RW/1C/V	**SDIN State Change Status Flags (WAKESTS):** Flag bits that indicate which SDI signal(s) received a State Change event. The bits are cleared by writing 1's to them. These bits are cleared on a power-on reset. Software must not make assumptions about the reset state of these bits and must set them appropriately.

6.2.9 Global Capabilities 2 (GCAP2)—Offset 12h

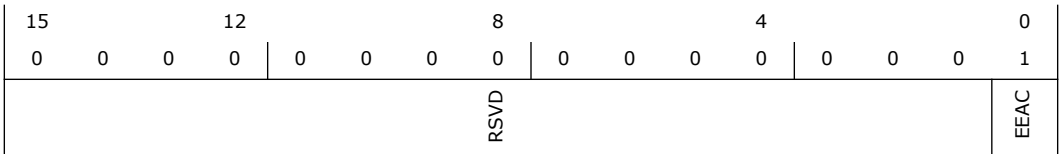
This register resides in Primary well (always on), or resides in Primary well (gated) with state retention, and reset by platform reset.

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 1h



Bit Range	Default & Access	Field Name (ID): Description
15:1	0h RO	Reserved.
0	1h RW/V/L	**Energy Efficient Audio Capability (EEAC):** Indicates whether the energy efficient audio with deeper buffering is supported or not. 0 = Not supported. br] 1 = Supported. Locked when FNCFG.BCLD = 1 or FUSVAL.CPPMD = 1.

6.2.10 Linked List Capabilities Header (LLCH)—Offset 14h

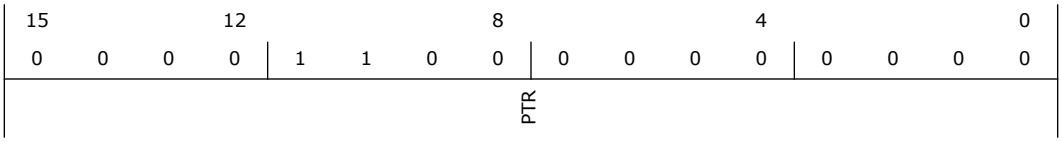
This register resides in Primary well (always on), or resides in Primary well (gated) with state retention, and reset by platform reset.

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 31
Function: 3

Default: C00h



Bit Range	Default & Access	Field Name (ID): Description
15:0	C00h RW/L	**First Capability Pointer (PTR):** This field contains the offset to the first capability structure of the linked list capabilities, or 0000h if no linked list capabilities exist. Point to Multiple Links Capability. Locked when FNCFG.BCLD = 1.

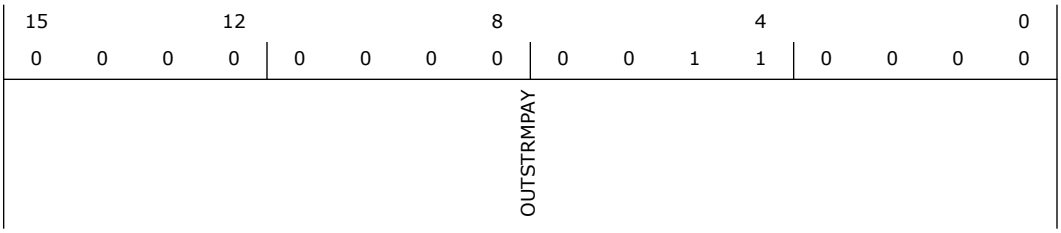
6.2.11 Output Stream Payload Capability (OUTSTRMPAY)—Offset 18h

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 30h



Bit Range	Default & Access	Field Name (ID): Description
15:0	30h RO	**Output Stream Payload Capability (OUTSTRMPAY):** Indicates maximum number of words per frame for any single output stream. This measurement is in 16 bit word quantities per 48 kHz frame. 48 Words (96B) is the maximum supported, therefore a value of 30h is reported in this register. Software must ensure that a format which would cause more words per frame than indicated is not programmed into the Output Stream Descriptor register. 00h: 0 words 01h: 1 word payload ... FFh: 255h word payload

6.2.12 Input Stream Payload Capability (INSTRMPAY)—Offset 1Ah

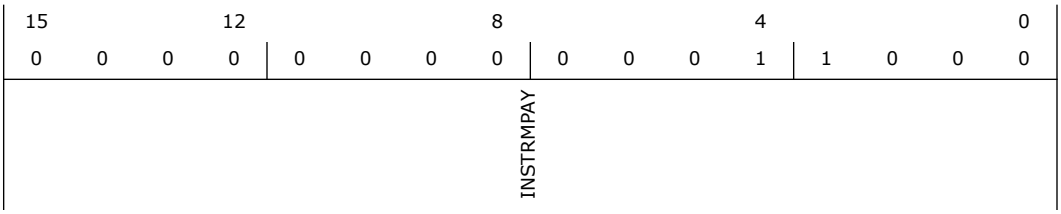
This register indicates the maximum number of Words per frame for any single input stream.

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 18h



Bit Range	Default & Access	Field Name (ID): Description
15:0	18h RO	**Input Stream Payload Capability (INSTRMPAY):** Indicates maximum number of words per frame for any single input stream. This measurement is in 16 bit word quantities per 48 kHz frame. 24 Words (48B) is the maximum supported, therefore a value of 18h is reported in this register. Software must ensure that a format which would cause more words per frame than indicated is not programmed into the Input Stream Descriptor register. 00h: 0 words 01h: 1 word payload ... FFh: 255h word payload

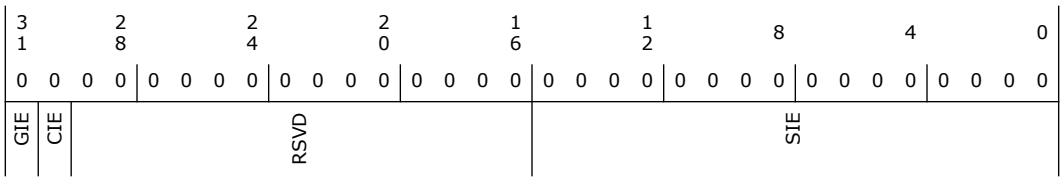
6.2.13 Interrupt Control (INTCTL)—Offset 20h

The Interrupt Status and Control register provides a central point for controlling and monitoring interrupt generation. The SIE (Stream Interrupt Enable) register controls the interrupt mask for each individual Input or Output Stream. Setting a 1 in the appropriate bit allows the particular interrupt source to generate a processor interrupt. The SIS (Stream Interrupt Status) register indicates the current interrupt status of each interrupt source. A 1 indicates that an interrupt is being requested. Note that the state of these bits is independent of the SIE bits; even if the corresponding bit is set to a 0 in the Stream Interrupt Enable register to disable processor interrupt generation, the Status bit may still be set to indicate that stream is requesting service. This can be used by polling software to determine which Streams need attention without incurring system interrupts.
The CIE (Controller Interrupt Enable) and CIS (Controller Interrupt Status) control and indicate the status of the general controller interrupt. General controller interrupt sources are to a Response Interrupt, a Response Buffer Overrun, and State Change events. Note that the CIS is independent of the CIE bit; even if the CIE bit is set to a 0 to disable processor interrupt generation, the CIS bit may still be set to indicate that stream is requesting service.
The GIE (Global Interrupt Enable) and GIS (Global Interrupt Status) control and indicate the status of all hardware interrupt sources in the Intel HD Audio controller. If GIS bit is a 1, a processor interrupt is currently being requested. If GIE is a 1, a processor interrupt may be requested; if GIE is a 0, then no processor interrupt may be requested. Note that the GIS is independent of the GIE bit; even if the GIE bit is set to a 0 to disable processor interrupt generation, the GIS bit may still be set to indicate that stream is requesting service.
GIE and CIE bits are not affected by controller reset.
The number of SIE bits in this register is depending on the total number of stream DMA implemented, represented as x in the register table. The x value is determined by the sum of parameter HSTISC and HSTOSC. For SPT implementation, x = 16.

Access Method

Type: MEM Register (Size: 32 bits)
Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Global Interrupt Enable (GIE):** Global bit to enable device interrupt generation. When set to 1 the Intel HD Audio function is enabled to generate an interrupt. This control is in addition to any bits in the bus specific address space, such as the Interrupt Enable bit in the PCI Configuration Space.
30	0h RW	**Controller Interrupt Enable (CIE):** Enables the general interrupt for controller functions. When set to 1 (and GIE is enabled), the controller generates an interrupt when the CIS bit gets set.
29:16	0h RO	Reserved.
15:0	0h RW	**Stream Interrupt Enable (SIE):** When set to 1 the individual Streams are enabled to generate an interrupt when the corresponding stream status bits get set. A stream interrupt will be caused as a result of a buffer with IOC=1 in the BDL entry being completed, or as a result of a FIFO error (underrun or overrun) occurring. Control over the generation of each of these sources is in the associated Stream Descriptor. The streams are numbered and the SIE bits assigned sequentially, based on their order in the register set.

6.2.14 Interrupt Status (INTSTS)—Offset 24h

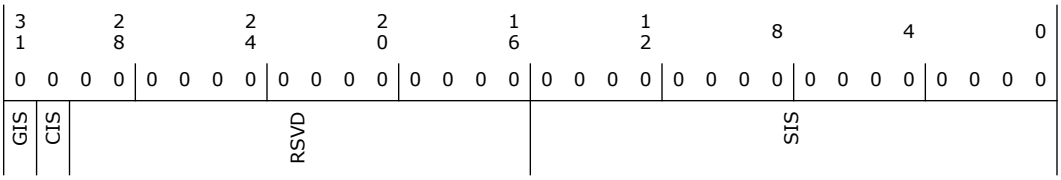
GIS and CIS bits are not affected by controller reset.
The number of SIS bits in this register is depending on the total number of stream DMA implemented, represented as x in the register table. The x value is determined by the sum of parameter HSTISC and HSTOSC.
For SPT implementation, x = 16.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**Global Interrupt Status (GIS):** This bit is an OR of all of the interrupt status bits in this register and PPSTS register

Bit Range	Default & Access	Field Name (ID): Description
30	0h RW/V	**Controller Interrupt Status (CIS):** Status of general controller interrupt. A 1 indicates that an interrupt condition occurred due to a Response Interrupt, a Response Buffer Overrun Interrupt, CORB Memory Error Interrupt, Error Present Interrupt, or a SDIN State Change event. The exact cause can be determined by interrogating other registers. Note that a HW interrupt will not be generated unless the corresponding enable bit is set. This bit is an OR of all of the stated interrupt status bits for this register.
29:16	0h RO	Reserved.
15:0	0h RW/V	**Stream Interrupt Status (SIS):** A 1 indicates that an interrupt condition occurred on the corresponding Stream. Note that a HW interrupt will not be generated unless the corresponding enable bit is set. This bit is an OR of all of an individual stream s interrupt status bits. The streams are numbered and the SIS bits assigned sequentially, based on their order in the register set.

6.2.15 Wall Clock Counter (WALCLK)—Offset 30h

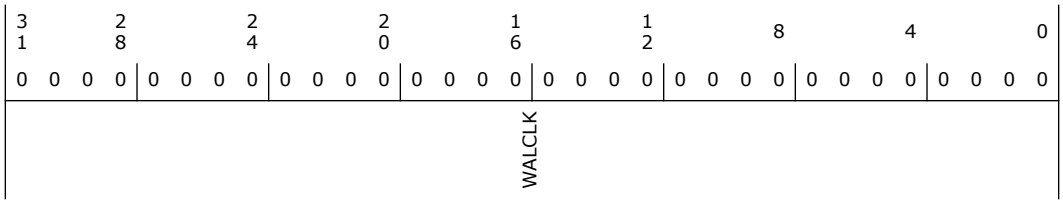
The 32 bit monotonic counter provides a 'wall clock' that can be used by system software to synchronize independent audio controllers. The counter must be implemented.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Wall Clock Counter (WALCLK):** 32 bit counter that is incremented on each link BCLK period and rolls over from FFFF_FFFFh to 0000_0000h. This counter will roll over to zero with a period of approximately 179 seconds. This counter is enabled while the BCLK bit is set to 1. Software uses this counter to synchronize between multiple controllers. Will be reset on controller reset. With the introduction of multiple link segments for the Intel HD Audio controller, and the capability of running each link segment at different clock speed, the BCLK definition for this counter is fixed at 24 MHz equivalent rate always, independent of the physical link clock speed, and reports the link 0 wall clock value.

6.2.16 Stream Synchronization (SSYNC)—Offset 38h

To synchronize two or more streams the corresponding SSYNC bits for the streams to be synchronized should be set to 1 before the 'RUN' bit for each stream is set.
The RUN bit for the corresponding stream must be set to 1 (and FIFORDY=1) prior to that stream's SSYNC bit being written to 0. To start multiple streams synchronously, the stream sync bits for those streams should be written to 0 at the same time. For all SSYNC bits on output engines that transition from 1 to 0 on the same write, the

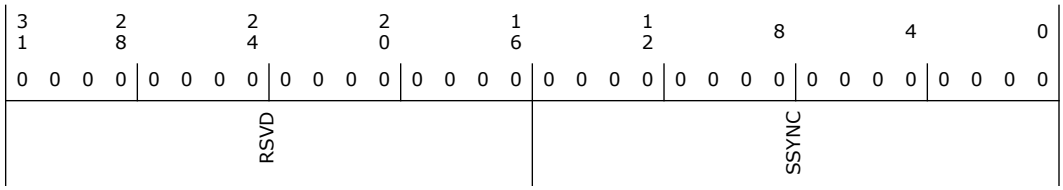
formatter will deliver a sample over the link in the same 48kHz frame. For all SSYNC bits on input engines that transition from 1 to 0 on the same write, the formatter will take stream data off the link and place it in the FIFO.
If synchronization is not desired, the stream synchronization bits may be left 0, and the stream will simply begin running normally when the stream's 'RUN' bit is set.
In addition to platform reset, FLR, and controller reset, the register is also reset by stream reset.
The number of SSYNC bits in this register is depending on the total number of stream DMA implemented, represented as x in the register table. The x value is determined by the sum of parameter HSTISC and HSTOSC. For SPT implementation, x = 16.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	0h RW	**Stream Synchronization Bits (SSYNC):** The Stream Synchronization bits, when set to 1, block data from being sent on or received from the link. Each bit controls the associated Stream Descriptor, bit 0 corresponds to the first Stream Descriptor, etc. To synchronously start a set of DMA engines, the bits in the SSYNC register are first set to a 1. The RUN bits for the associated Stream Descriptors are then set to a 1 to start the DMA engines. When all streams are ready (FIFORDY=1), the associated SSYNC bits can all be set to 0 at the same time, and transmission or reception of bits to or from the link will begin together at the start of the next full link frame. To synchronously stop streams, first the bits are set in the SSYNC register, and then the individual RUN bits in the Stream Descriptors are cleared by software. The streams are numbered and the SSYNC bits assigned sequentially, based on their order in the register set.

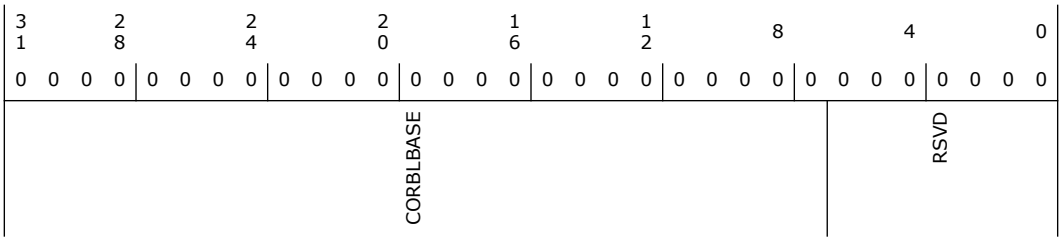
6.2.17 CORB Lower Base Address (CORBLBASE)—Offset 40h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RW	**CORB Lower Base Address (CORBLBASE):** Lower address of the Command Output Ring Buffer, allowing the CORB Base Address to be assigned on any 128-B boundary. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted.
6:0	0h RO	Reserved.

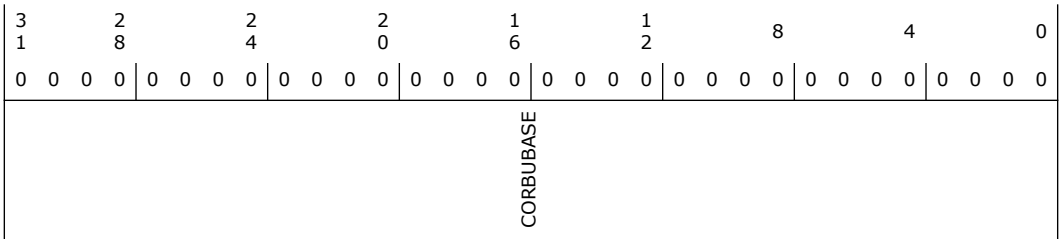
6.2.18 CORB Upper Base Address (CORBUBASE)—Offset 44h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/L	**CORB Upper Base Address (CORBUBASE):** Upper 32 bits of address of the Command Output Ring Buffer. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted. Locked when GCAP.ADD64OK = 0.

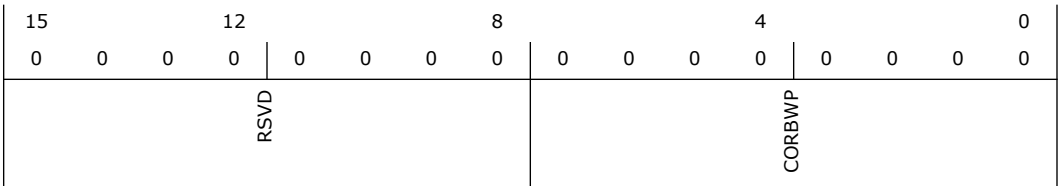
6.2.19 CORB Write Pointer (CORBWP)—Offset 48h

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	Reserved.
7:0	0h RW	**CORB Write Pointer (CORBWP):** Software writes the last valid CORB entry offset into this field in Dword granularity. The DMA engine fetches commands from the CORB until the Read Pointer matches the Write Pointer. Supports 256 CORB entries (256 x 4B=1KB). This field may be written while the DMA engine is running.

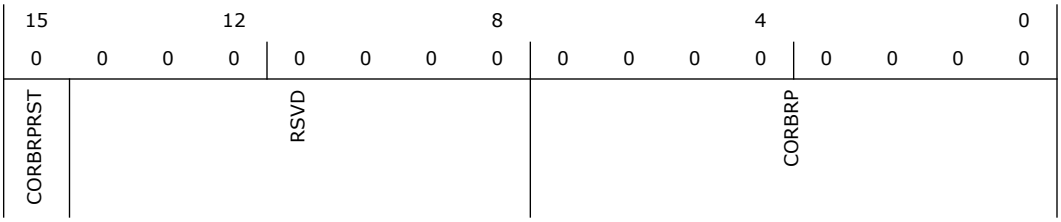
6.2.20 CORB Read Pointer (CORBRP)—Offset 4Ah

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/V	**CORB Read Pointer Reset (CORBRPRST):** Software writes a 1 to this bit to reset the CORB Read Pointer to 0 and clear any residual pre-fetched commands in the CORB hardware buffer within the Intel Audio controller. The hardware will physically update this bit to 1 when the CORB Pointer reset is complete. Software must read a 1 to verify that the reset completed correctly. Software must clear this bit back to 0 and read back the 0 to verify that the clear completed correctly. The CORB DMA engine must be stopped prior to resetting the Read Pointer or else DMA transfer may be corrupted.
14:8	0h RO	Reserved.
7:0	0h RO/V	**CORB Read Pointer (CORBRP):** Software reads this field to determine how many commands it can write to the CORB without over-running. The value read indicates the CORB Read Pointer offset in Dword granularity. The offset entry read from this field has been successfully fetched by the DMA controller and may be over-written by software. Supports 256 CORB entries (256 x 4B=1KB). This field may be read while the DMA engine is running.

6.2.21 CORB Control (CORBCTL)—Offset 4Ch

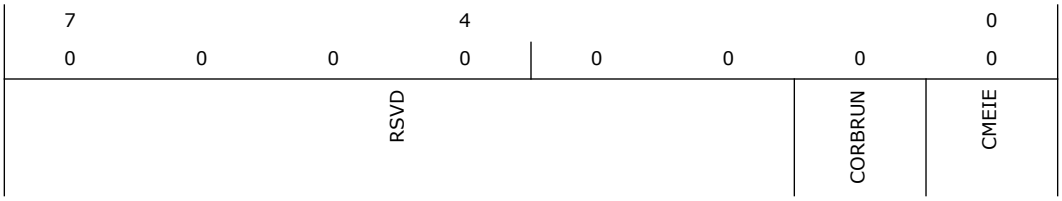
Length: 1 bytes

Access Method

Type: MEM Register
(Size: 8 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7:2	0h RO	Reserved.
1	0h RW/V	**Enable CORB DMA Engine (CORBRUN):** 0 = DMA Stop 1 = DMA Run After SW writes a 0 to this bit, the HW may not stop immediately. The hardware will physically update the bit to a 0 when the DMA engine is truly stopped. SW must read a 0 from this bit to verify that the DMA is truly stopped.
0	0h RW	**CORB Memory Error Interrupt Enable (CMEIE):** If this bit is set (and GIE and CIE are enabled), the controller will generate an interrupt if the MEI status bit is set.

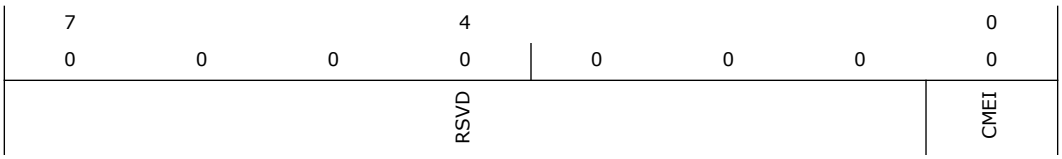
6.2.22 CORB Status (CORBSTS)—Offset 4Dh

Access Method

Type: MEM Register
(Size: 8 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7:1	0h RO	Reserved.
0	0h RW/1C/V	**CORB Memory Error Indication (CMEI):** If this status bit is set, the controller has detected an error in the pathway between the controller and memory. This may be an ECC bit error or any other type of detectable data error which renders the command data fetched invalid. Software can clear this bit by writing a 1 to it. However, this type of error leaves the audio subsystem in an unviable state and typically requires CRST#.

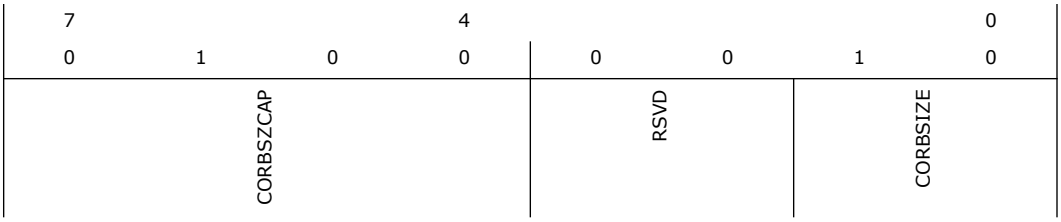
6.2.23 CORB Size (CORBSIZE)—Offset 4Eh

Access Method

Type: MEM Register
(Size: 8 bits)

Device: 31
Function: 3

Default: 42h



Bit Range	Default & Access	Field Name (ID): Description
7:4	4h RO	**CORB Size Capability (CORBSZCAP):** 0100b indicates that the PCH only supports a CORB size of 256 CORB entries (1024B).
3:2	0h RO	Reserved.
1:0	2h RO	**CORB Size (CORBSIZE):** Hardwired to 10b which sets the CORB size to 256 entries (1024B).

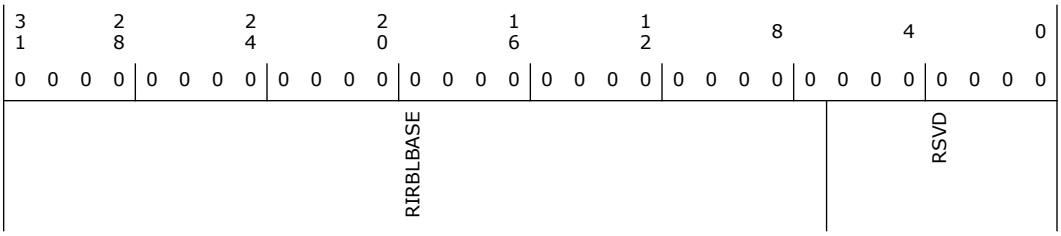
6.2.24 RIRB Lower Base Address (RIRBLBASE)—Offset 50h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RW	**RIRB Lower Base Address (RIRBLBASE):** Lower address of the Response Input Ring Buffer, allowing the RIRB Base Address to be assigned on any 128-B boundary. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted.
6:0	0h RO	Reserved.

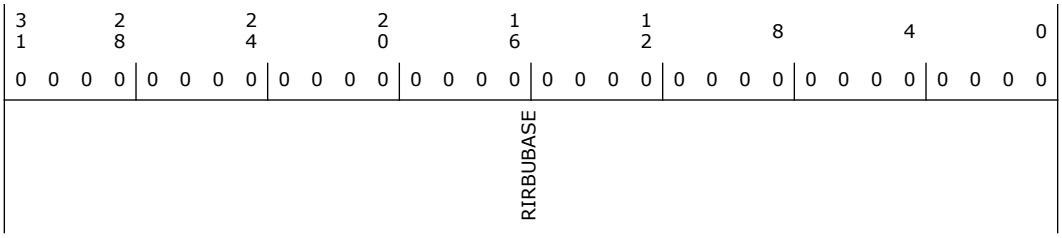
6.2.25 RIRB Upper Base Address (RIRBUBASE)—Offset 54h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/L	**RIRB Upper Base Address (RIRBUBASE):** Upper 32 bits of address of the Command Output Ring Buffer. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted. Locked when GCAP.64OK = 0.

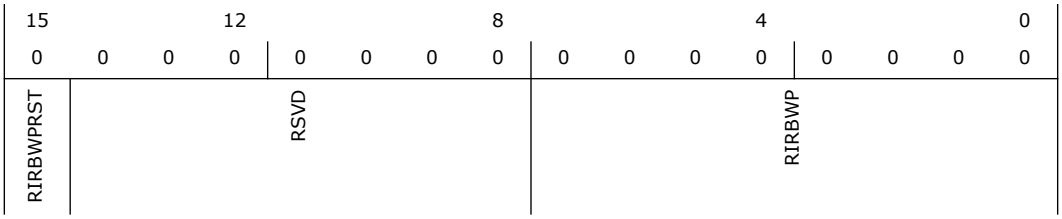
6.2.26 RIRB Write Pointer (RIRBWP)—Offset 58h

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15	0h WO	**RIRB Write Pointer Reset (RIRBWPRST):** Software writes a 1 to this bit to reset the RIRB Write Pointer to 0's. The RIRB DMA engine must be stopped prior to resetting the Write Pointer or else DMA transfer may be corrupted. This bit will always be read as 0.
14:8	0h RO	Reserved.
7:0	0h RO/V	**RIRB Write Pointer (RIRBWP):** Indicates the last valid RIRB entry written by the DMA controller. Software reads this field to determine how many responses it can read from the RIRB. The value read indicates the RIRB Write Pointer offset in 2 Dword RIRB entry units (since each RIRB entry is 2 Dwords long). Supports up to 256 RIRB entries (256 x 8B=2KB). This field may be read while the DMA engine is running.

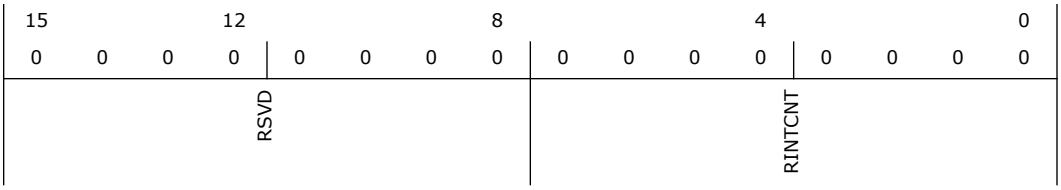
6.2.27 Response Interrupt Count (RINTCNT)—Offset 5Ah

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	Reserved.
7:0	0h RW	**N Response Interrupt Count (RINTCNT):** 0000_0001b = 1 Response sent to RIRB ... 1111_1111b = 255 Responses sent to RIRB 0000_0000b = 256 Responses sent to RIRB The DMA engine should be stopped when changing this field or else an interrupt may be lost. Note that each Response occupies 2 Dwords in the RIRB. This is compared to the total number of responses that have been returned, as opposed to the number of frames in which there were responses. If more than one codec responds in one frame, then the count is increased by the number of responses received in the frame.

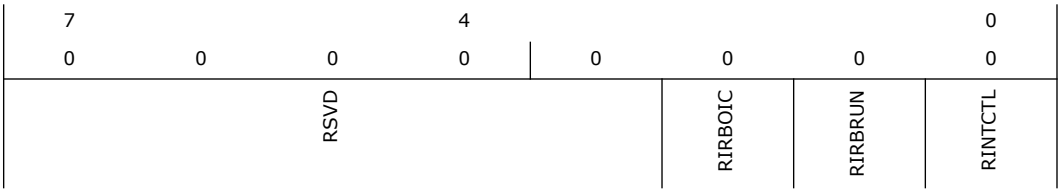
6.2.28 RIRB Control (RIRBCTL)—Offset 5Ch

Access Method

Type: MEM Register
(Size: 8 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7:3	0h RO	Reserved.
2	0h RW	**Response Overrun Interrupt Control (RIRBOIC):** If this bit is set (and GIE and CIE are enabled), the hardware will generate an interrupt when the Response Overrun Interrupt Status bit is set.
1	0h RW/V	**RIRB DMA Enable (RIRBRUN):** 0 = DMA Stop 1 = DMA Run After SW writes a 0 to this bit, the HW may not stop immediately. The hardware will physically update the bit to a 0 when the DMA engine is truly stopped. SW must read a 0 from this bit to verify that the DMA is truly stopped.
0	0h RW	**Response Interrupt Control (RINTCTL):** 0 = Disable Interrupt 1 = Generate an interrupt (if GIE and CIE are enabled) after N number of Responses are sent to the RIRB buffer OR when an empty Response slot is encountered on all SDI_x inputs (whichever occurs first). The N counter is reset when the interrupt is generated.

6.2.29 RIRB Status (RIRBSTS)—Offset 5Dh

Access Method

Type: MEM Register
(Size: 8 bits)

Device: 31
Function: 3

Default: 0h

7			4				0
0	0	0	0	0	0	0	0
RSVD					RIRBOIS	RSVD	RINTFL

Bit Range	Default & Access	Field Name (ID): Description
7:3	0h RO	Reserved.
2	0h RW/1C/V	**Response Overrun Interrupt Status (RIRBOIS):** Hardware sets this bit to a 1 when the RIRB DMA engine is not able to write the incoming responses to memory before additional incoming responses overrun the internal FIFO. When the overrun occurs, the hardware will drop the responses which overrun the buffer. An interrupt may be generated if the Response Overrun Interrupt Control bit is set. Note that this status bit is set even if an interrupt is not enabled for this event. Software clears this flag by writing a 1 to this bit.
1	0h RO	Reserved.
0	0h RW/1C/V	**Response Interrupt (RINTFL):** Hardware sets this bit to a 1 when an interrupt has been generated after N number of Responses are sent to the RIRB buffer OR when an empty Response slot is encountered on all SDI(x) inputs (whichever occurs first). Note that this status bit is set even if an interrupt is not enabled for this event. Software clears this flag by writing a 1 to this bit.

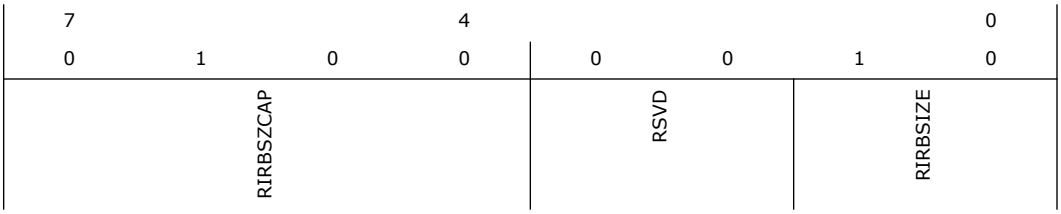
6.2.30 RIRB Size (RIRBSIZE)—Offset 5Eh

Access Method

Type: MEM Register
(Size: 8 bits)

Device: 31
Function: 3

Default: 42h



Bit Range	Default & Access	Field Name (ID): Description
7:4	4h RO	**RIRB Size Capability (RIRBSZCAP):** 0100b indicates that the PCH only supports a RIRB size of 256 RIRB entries (2048B).
3:2	0h RO	Reserved.
1:0	2h RO	**RIRB Size (RIRBSIZE):** Hardwired to 10b which sets the RIRB size to 256 entries (2048B).

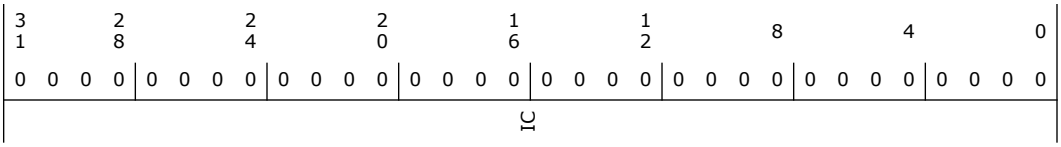
6.2.31 Immediate Command (IC)—Offset 60h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Immediate Command (IC):** The command to be sent to the codec via the Immediate Command mechanism is written to this register. The command stored in this register is sent out over the link during the next available frame after a 1 is written to the ICB bit.

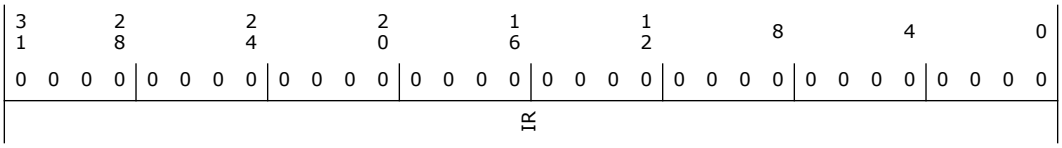
6.2.32 Immediate Response (IR)—Offset 64h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Immediate Response (IR):** This register contains the response received from a codec resulting from a command sent via the Immediate Command mechanism. If multiple codecs responded in the same frame, there is no guarantee as to which response will be latched. Therefore broadcast-type commands must not be issued via the Immediate Command mechanism.

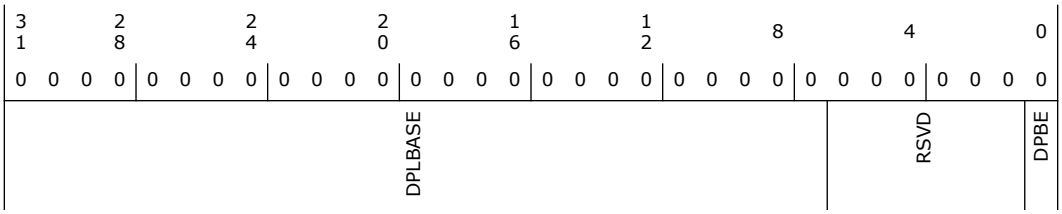
6.2.33 DMA Position Lower Base Address (DPLBASE)—Offset 70h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RW	**DMA Position Lower Base Address (DPLBASE):** Lower 32 bits of the DMA Position Buffer Base Address. This register field must not be written when any DMA engine is running or the DMA transfer may be corrupted. This same address is used by the Flush Control, and must be programmed with a valid value before the FLCNRTL bit is set.
6:1	0h RO	Reserved.
0	0h RW	**DMA Position Buffer Enable (DPBE):** When this bit is set to a '1', the controller will write the DMA positions of each of the DMA engines to the buffer in main memory periodically (typically once/frame). Software can use this value to know what data in memory is valid data. The controller must guarantee that the values in the DMA Position Buffer that the software can read represent positions in the stream for which valid data exists in the Stream's DMA buffer. This has particular relevance in systems which support isochronous transfer, the stream positions in the software-visible memory buffer must represent stream data which has reached the Global Observation point.

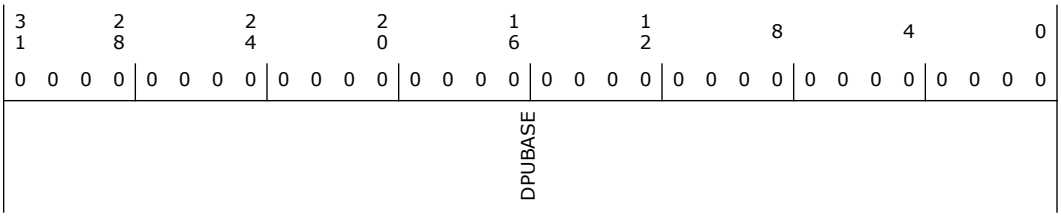
6.2.34 DMA Position Upper Base Address (DPUBASE)—Offset 74h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/L	**DMA Position Upper Base Address (DPUBASE):** Upper 32 bits of address of the DMA Position Buffer Base Address. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted. Locked when GCAP.ADD64OK = 0.

6.2.35 Input/Output Stream Descriptor x Control (ISD0CTL)—Offset 80h

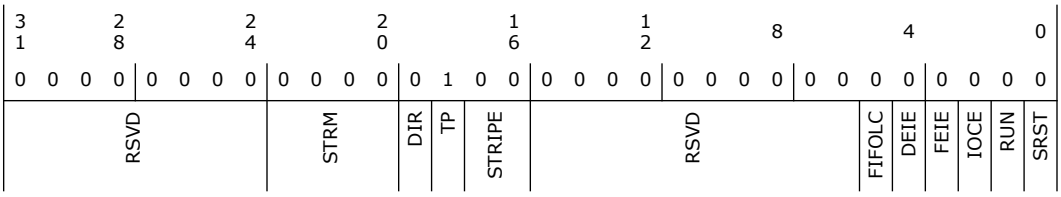
NOTE: This register definition applies to all of the following input and output streams at the corresponding offsets:
Input stream 0: offset 80h
Input stream 1: offset A0h
Input stream 2: offset C0h
Input stream 3: offset E0h
Input stream 4: offset 100h
Input stream 5: offset 120h
Input stream 6: offset 140h
Input stream 7: offset 280h
Output stream 0: offset 160h
Output stream 1: offset 180h
Output stream 2: offset 1A0h
Output stream 3: offset 1C0h
Output stream 4: offset 1E0h
Output stream 5: offset 200h
Output stream 6: offset 220h
output stream 7: offset 240h
Output stream 8: offset 260h
Output stream 9: offset 380h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 40000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. 0000=Reserved (Indicates Unused) 0001=Stream 1 ... 1110=Stream 14 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.
19	0h RO	**Bidirectional Direction Control (DIR):** This bit is only meaningful for Bidirectional streams. Therefore this bit is hardwired to 0.
18	1h RO	**Traffic Priority (TP):** Hardwired to 1 indicating that all streams will use VC1 if it is enabled throughout the PCI Express registers.
17:16	0h RW/L	**Stripe Control (STRIPE):** Input Stream: This field is meaningless for input streams. Output Stream: For output streams it controls the number of SDO signals to stripe data across. Locked when GCAP.NSDO = 00b.
15:6	0h RO	Reserved.
5	0h RW/V/L	**FIFO Limit Change (FIFOLC):** Writing a 1 to this bit indicates a new update to the FIFOL register has been made. After the HW has completed sequencing into the new effective FIFO size, it will clear this bit. This bit is RO if GCAP2.EEAC = 0. If GCAP2.EEAC = 1 and GCAP2.DFIFOLCC = 0 (static), this bit will only have effect when the stream is idle (before the first time RUN bit is set). If GCAP2.EEAC = 1 and GCAP2.DFIFOLCC = 1 (dynamic), on top of supporting the static behavior describe above, this bit also has effect when the stream is active (after the first time RUN bit is set).
4	0h RW	**Descriptor Error Interrupt Enable (DEIE):** Controls whether an interrupt is generated when the Descriptor Error Status (DESE) bit is set.
3	0h RW	**FIFO Error Interrupt Enable (FEIE):** This bit controls whether the occurrence of a FIFO error (overrun for input or underrun for output) will cause an interrupt or not. If this bit is not set, bit 3 in the Status register will be set, but the interrupt will not occur. Either way, the samples will be dropped.
2	0h RW	**Interrupt On Completion Enable (IOCE):** This bit controls whether or not an interrupt occurs when a buffer completes with the IOC bit set in its descriptor. If this bit is not set, bit 2 in the Status register will be set, but the interrupt will not occur
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this input stream will be enabled to transfer data in the FIFO to main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. When cleared to 0 the DMA engine associated with this input stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

6.2.36 Stream Descriptor Status (ISD0STS)—Offset 83h

NOTE: This register applies to the following input and output streams at the corresponding offsets:
Input stream 0: offset 83h
Input stream 1: offset A3h
Input stream 2: offset C3h
Input stream 3: offset E3h
Input stream 4: offset 103h
Input stream 5: offset 123h
Input stream 6: offset 143h
Input stream 7: offset 283h
Output stream 0: offset 163h
Output stream 1: offset 183h
Output stream 2: offset 1A3h
Output stream 3: offset 1C3h
Output stream 4: offset 1E3h
Output stream 5: offset 203h
Output stream 6: offset 223h
output stream 7: offset 243h
Output stream 8: offset 263h
Output stream 9: offset 383h

Access Method

Type: MEM Register (Size: 8 bits)

Device: 31
Function: 3

Default: 0h

7			4				0
0	0	0	0	0	0	0	0
RSVD		FIFORDY	DESE	FIFOE	BCIS	RSVD	

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	Reserved.
5	0h RO/V	**FIFO Ready (FIFORDY):** This bit defaults to 0 on reset because the FIFO is cleared on a reset. Input Stream: For input streams, the controller hardware will set this bit to 1 when a valid descriptor is loaded and the engine is ready for the RUN bit to be set. Output Stream: For output streams, the controller hardware will set this bit to a 1 while the output DMA FIFO contains enough data to maintain the stream on then link.
4	0h RW/1C/V	**Descriptor Error (DESE):** Indicates that a serious error occurred during the fetch of a descriptor. This could be a result of a Master Abort, a Parity or ECC error on the bus, or any other error which renders the current Buffer Descriptor or Buffer Descriptor List useless. This error is treated as a fatal stream error, as the stream cannot continue running. The RUN bit will be cleared and the stream will stop. Software may attempt to restart the stream engine after addressing the cause of the error and writing a 1 to this bit to clear it.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW/1C/V	**FIFO Error (FIFOE):** Set when a FIFO error occurs. Bit is cleared by writing a 1 to this bit position. This bit is set even if an interrupt is not enabled. Input Stream: For an input stream, this indicates a FIFO overrun occurring while the RUN bit is set. When this happens, the FIFO pointers don't increment and the incoming data is not written into the FIFO, thereby being lost. Output Stream: For an output stream, this indicates a FIFO under run when there are still buffers to send. The hardware should not transmit anything on the link for the associated stream if there is not valid data to send.
2	0h RW/1C/V	**Buffer Completion Interrupt Status (BCIS):** This bit is set to 1 by the hardware after the last sample of a buffer has been processed, AND if the Interrupt on Completion (IOC) bit is set in the command byte of the buffer descriptor. It remains active until software clears it by writing a 1 to this bit position.
1:0	0h RO	Reserved.

6.2.37 Input/Output Stream Descriptor x Link Position in Buffer (ISD0LPIB)—Offset 84h

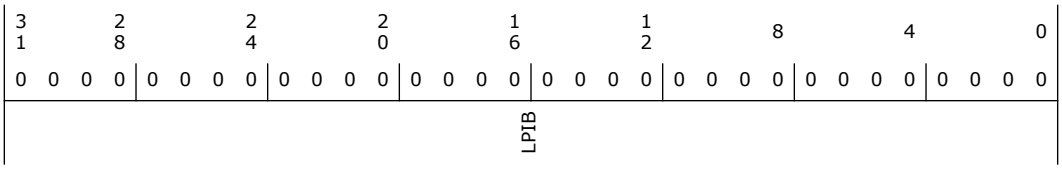
NOTE: This register applies to the following input and output streams at the corresponding offsets:
Input stream 0: offset 84h
Input stream 1: offset A4h
Input stream 2: offset C4h
Input stream 3: offset E4h
Input stream 4: offset 104h
Input stream 5: offset 124h
Input stream 6: offset 144h
Input stream 7: offset 284h
Output stream 0: offset 164h
Output stream 1: offset 184h
Output stream 2: offset 1A4h
Output stream 3: offset 1C4h
Output stream 4: offset 1E4h
Output stream 5: offset 204h
Output stream 6: offset 224h
output stream 7: offset 244h
Output stream 8: offset 264h
Output stream 9: offset 384h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Link Position in Buffer (LPIB):** Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

6.2.38 Input/Output Stream Descriptor x Cyclic Buffer Length (ISD0CBL)—Offset 88h

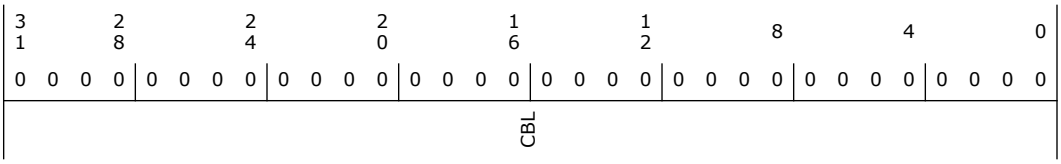
NOTE: This register applies to the following input and output streams at the corresponding offsets:
Input stream 0: offset 88h
Input stream 1: offset A8h
Input stream 2: offset C8h
Input stream 3: offset E8h
Input stream 4: offset 108h
Input stream 5: offset 128h
Input stream 6: offset 148h
Input stream 7: offset 288h
Output stream 0: offset 168h
Output stream 1: offset 188h
Output stream 2: offset 1A8h
Output stream 3: offset 1C8h
Output stream 4: offset 1E8h
Output stream 5: offset 208h
Output stream 6: offset 228h
output stream 7: offset 248h
Output stream 8: offset 268h
Output stream 9: offset 388h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Cyclic Buffer Length (CBL):** Indicates the number of bytes in the complete cyclic buffer. CBL must represent an integer number of samples. Link Position in Buffer (LPIB) will be reset when it reaches this value. Software may only write to this register after Global Reset, Controller Reset, or Stream Reset has occurred. This value should only be modified when the RUN bit is '0'. Once the RUN bit has been set to enable the engine, software must not write to this register until after the next reset is asserted, or transfers may be corrupted.

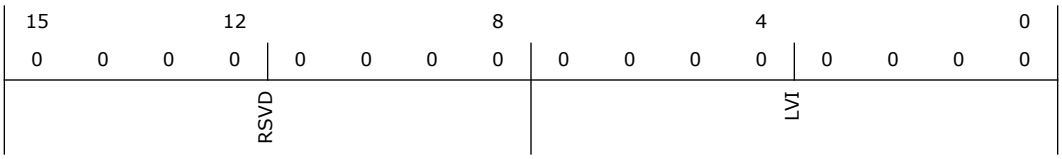
6.2.39 Input/Output Stream Descriptor x Last Valid Index (ISD0LVI)—Offset 8Ch

NOTE: This register applies to the following input and output streams at the corresponding offsets:
Input stream 0: offset 8Ch
Input stream 1: offset ACh
Input stream 2: offset CCh
Input stream 3: offset ECh
Input stream 4: offset 10Ch
Input stream 5: offset 12Ch
Input stream 6: offset 14Ch
Input stream 7: offset 28Ch
Output stream 0: offset 16Ch
Output stream 1: offset 18Ch
Output stream 2: offset 1ACh
Output stream 3: offset 1CCh
Output stream 4: offset 1ECh
Output stream 5: offset 20Ch
Output stream 6: offset 22Ch
output stream 7: offset 24Ch
Output stream 8: offset 26Ch
Output stream 9: offset 38Ch

Access Method

Type: MEM Register (Size: 16 bits)
Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	Reserved.
7:0	0h RW	**Last Valid Index (LVI):** The value written to this register indicates the index for the last valid Buffer Descriptor in the BDL. After the controller has processed this descriptor, it will wrap back to the first descriptor in the list and continue processing. LVI must be at least 1, i.e., there must be at least two valid entries in the b uffer descriptor list before DMA operations can begin. This value should only be modified when the RUN bit is '0'

6.2.40 Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD0FIFOW)—Offset 8Eh

NOTE: This register applies to the following input and output streams at the corresponding offsets:
Input stream 0: offset 8Eh
Input stream 1: offset AEh

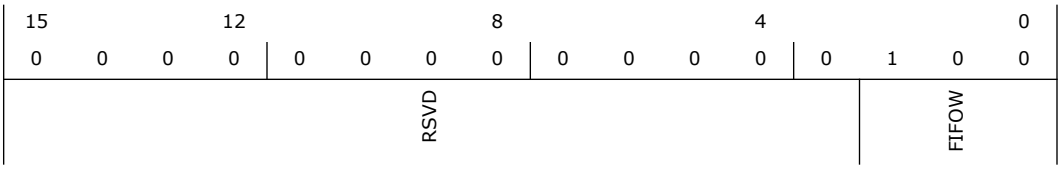
Input stream 2: offset CEh
Input stream 3: offset EEh
Input stream 4: offset 10Eh
Input stream 5: offset 12Eh
Input stream 6: offset 14Eh
Input stream 7: offset 28Eh
Output stream 0: offset 16Eh
Output stream 1: offset 18Eh
Output stream 2: offset 1AEh
Output stream 3: offset 1CEh
Output stream 4: offset 1EEh
Output stream 5: offset 20Eh
Output stream 6: offset 22Eh
output stream 7: offset 24Eh
Output stream 8: offset 26Eh
Output stream 9: offset 38Eh

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 4h



Bit Range	Default & Access	Field Name (ID): Description
15:3	0h RO	Reserved.
2:0	4h RO/V	**FIFOW (FIFOW):** Indicates the minimum number of bytes accumulated (for input) or free (for output) in the FIFO before the controller will start an eviction (for input) or fetch (for output) of data. The PCH HD Audio controller hardwires the FIFO Watermark, either 32B or 64B based on the following. Bit(2:0) Description 000-011 Reserved 100 32 B Supported. The 32 B request is aligned to 32 B boundaries. 101 64 B Supported. The 64 B request is aligned to 64 B boundaries. 110-111 Reserved Input Stream: For input streams, the FIFOW value is determined by the EM3.ISRWS (SEM3.ISRWS) field. Output Stream: For output streams, the FIFOW value is determined by the EM4.OSRWS (SEM4.OSRWS) field.

6.2.41 Input/Output Stream Descriptor x FIFO Size (ISD0FIFOS)—Offset 90h

NOTE: This register applies to the following input and output streams at the corresponding offsets:
Input stream 0: offset 90h

Input stream 1: offset B0h
Input stream 2: offset D0h
Input stream 3: offset F0h
Input stream 4: offset 110h
Input stream 5: offset 130h
Input stream 6: offset 150h
Input stream 7: offset 290h
Output stream 0: offset 170h
Output stream 1: offset 190h
Output stream 2: offset 1B0h
Output stream 3: offset 1D0h
Output stream 4: offset 1F0h
Output stream 5: offset 210h
Output stream 6: offset 230h
output stream 7: offset 250h
Output stream 8: offset 270h
Output stream 9: offset 3A0h

Access Method

Type: MEM Register (Size: 16 bits)
Device: 31
Function: 3

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW/V	**FIFO Size (FIFOS):** When GCAP2.EEAC = 0, indicates the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time. This is the maximum number of bytes that may have been received into the HW buffer but not yet transferred out, and is also the maximum possible value that the PICB count will increase by at one time. The FIFO size is calculated based on the stream format programmed in (I/O)SDxFMT register, the min frame of buffering setting in EM(3/4)(SEM(3/4)).(I/O)SBSMFA[1:0] field, and the minimum buffer size threshold setting in EM2.BSMT[1:0] field. As the default value is zero, SW must write to the (I/O)SDxFMT register to kick off the FIFO size calculation, and read back to find out the HW allocated FIFO size. When GCAP2.EEAC = 1, this FIFOS value represent the minimum FIFO size HW required to operate efficiently. SW can program FIFOL register to extend the effective FIFO size in HW beyond this minimum value advertised. In this case, the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time, the maximum number of bytes that may have been received into the HW buffer but not yet transferred out, and also the maximum possible value that the PICB count will increase by one time, all these maximum value could be larger than FIFOS value, depending on the FIFOL register setting. When EM2.HWFIFOL = 1, this FIFOS value will reflect the larger FIFO size of up to 10 ms, if extra buffer space is available.

6.2.42 Input/Output Stream Descriptor x Format (ISD0FMT)—Offset 92h

NOTE: This register applies to the following input and output streams at the corresponding offsets:
Input stream 0: offset 92h

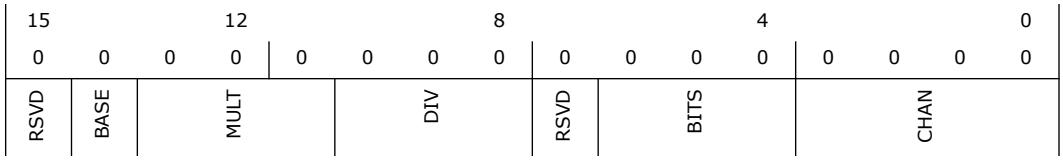
Input stream 1: offset B2h
Input stream 2: offset D2h
Input stream 3: offset F2h
Input stream 4: offset 112h
Input stream 5: offset 132h
Input stream 6: offset 152h
Input stream 7: offset 292h
Output stream 0: offset 172h
Output stream 1: offset 192h
Output stream 2: offset 1B2h
Output stream 3: offset 1D2h
Output stream 4: offset 1F2h
Output stream 5: offset 212h
Output stream 6: offset 232h
output stream 7: offset 252h
Output stream 8: offset 272h
Output stream 9: offset 3A2h

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	Reserved.
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	Reserved.
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

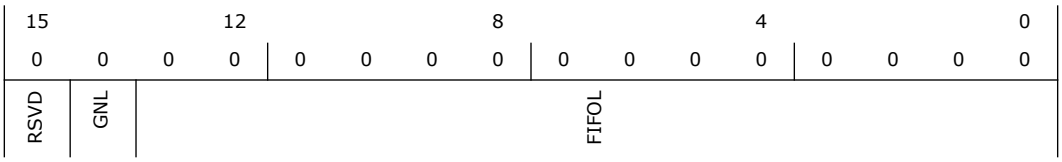
6.2.43 Input/Output Stream Descriptor x FIFO Limit (ISD0FIFOL)—Offset 94h

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	Reserved.
14	0h RW/L	**Granularity (GNL):** Granularity associated with LMT field definition. The LMT value needs to be multiplied with 125 us or 1 ms to get the access limit in time domain. 0 = 125 us 1 = 1 ms This bit is locked if GCAP2.EEAC = 0 (thus appear to be RO).
13:0	0h RW/L	**FIFO Limit (FIFOL):** Indicate how far the media player / application intend to process ahead, in units of time. HW can extend the effective FIFO size to fetch (for output stream) or evict (for input stream) more data in the cyclic buffer beyond the minimum FIFO size advertised in FIFOS register, up to this access limit. Need to multiply with the granularity (125 us vs. 1 ms) as defined in GNL bit, to get the actual processing ahead time. 0 = Disabled (FIFOS is the limit) 0001h 3FFFh = 1 16383 units When value) 0 (enabled), setting FIFOLC bit will trigger HW to evaluate the access limit change and update effective FIFO size (depending on the capability supported). SW shall make sure the FIFOL field is not changed in the progress of access limit change sequence. This bit is locked if GCAP2.EEAC = 0 (thus appear to be RO).

6.2.44 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD0BDLPLBA)—Offset 98h

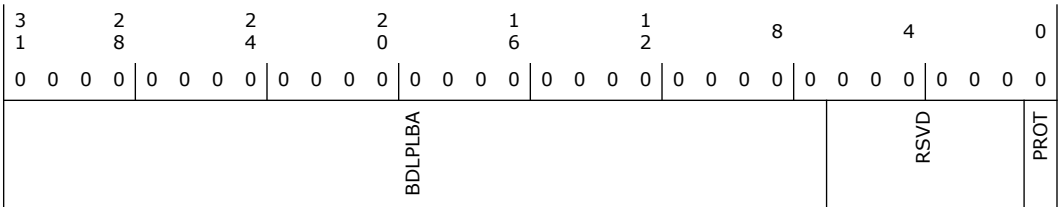
NOTE: This register applies to the following input and output streams at the corresponding offsets:
Input stream 0: offset 98h
Input stream 1: offset B8h
Input stream 2: offset D8h
Input stream 3: offset F8h
Input stream 4: offset 118h
Input stream 5: offset 138h
Input stream 6: offset 158h
Input stream 7: offset 298h
Output stream 0: offset 178h
Output stream 1: offset 198h
Output stream 2: offset 1B8h
Output stream 3: offset 1D8h
Output stream 4: offset 1F8h
Output stream 5: offset 218h
Output stream 6: offset 238h
output stream 7: offset 258h
Output stream 8: offset 278h
Output stream 9: offset 3A8h

Access Method

Type: MEM Register (Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RW	**Buffer Descriptor List Lower Base Address (BDLPLBA):** Lower address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or DMA transfers may be corrupted.
6:1	0h RO	Reserved.
0	0h RW/L	**Protect (PROT):** When this bit is set to 1, bits [31:7, 0] of this register are WO and will return 0's when read. When this bit is cleared to 0, bits [31:7, 0] are RW. Note that this bit can only be changed when all four bytes of this register are written in a single write operation. If less than four bytes are written this bit retains its previous value.

6.2.45 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD0BDLPUBA)—Offset 9Ch

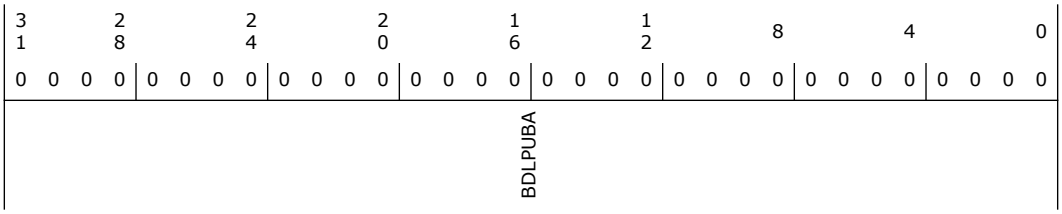
NOTE: This register applies to the following input and output streams at the corresponding offsets:
Input stream 0: offset 9Ch
Input stream 1: offset BCh
Input stream 2: offset DCh
Input stream 3: offset FCh
Input stream 4: offset 11Ch
Input stream 5: offset 13Ch
Input stream 6: offset 15Ch
Input stream 7: offset 29Ch
Output stream 0: offset 17Ch
Output stream 1: offset 19Ch
Output stream 2: offset 1BCh
Output stream 3: offset 1DCh
Output stream 4: offset 1FCh
Output stream 5: offset 21Ch
Output stream 6: offset 23Ch
output stream 7: offset 25Ch
Output stream 8: offset 27Ch
Output stream 9: offset 3ACh

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/L	**Buffer Descriptor List Upper Base Address (BDLPUBA):** Upper 32-bit address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or the DMA transfer may be corrupted. Locked when GCAP.64OK = 0.

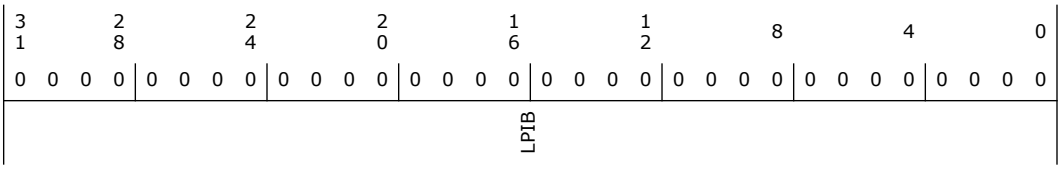
6.2.46 Input/Output Stream Descriptor x Link Position in Buffer (OSD0LPIB)—Offset 164h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Link Position in Buffer (LPIB):** Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

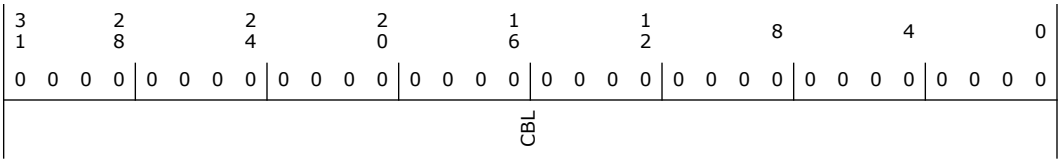
6.2.47 Input/Output Stream Descriptor x Cyclic Buffer Length (OSD0CBL)—Offset 168h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Cyclic Buffer Length (CBL):** Indicates the number of bytes in the complete cyclic buffer. CBL must represent an integer number of samples. Link Position in Buffer (LPIB) will be reset when it reaches this value. Software may only write to this register after Global Reset, Controller Reset, or Stream Reset has occurred. This value should only be modified when the RUN bit is '0'. Once the RUN bit has been set to enable the engine, software must not write to this register until after the next reset is asserted, or transfers may be corrupted.

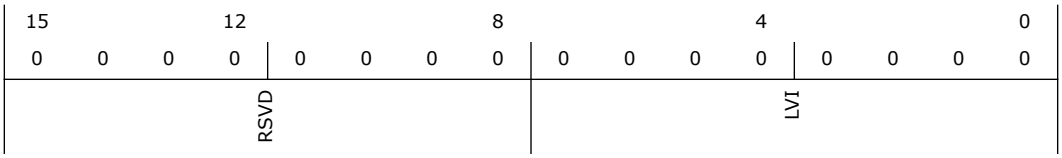
6.2.48 Input/Output Stream Descriptor x Last Valid Index (OSD0LVI)—Offset 16Ch

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	Reserved.
7:0	0h RW	**Last Valid Index (LVI):** The value written to this register indicates the index for the last valid Buffer Descriptor in the BDL. After the controller has processed this descriptor, it will wrap back to the first descriptor in the list and continue processing. LVI must be at least 1, i.e., there must be at least two valid entries in the b uffer descriptor list before DMA operations can begin. This value should only be modified when the RUN bit is '0'

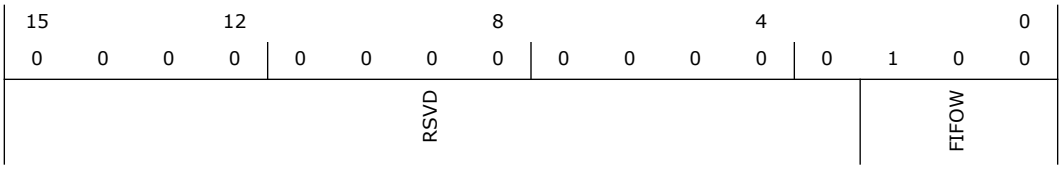
6.2.49 Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD0FIFOW)—Offset 16Eh

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 4h



Bit Range	Default & Access	Field Name (ID): Description
15:3	0h RO	Reserved.
2:0	4h RO/V	**FIFOW (FIFOW):** Indicates the minimum number of bytes accumulated (for input) or free (for output) in the FIFO before the controller will start an eviction (for input) or fetch (for output) of data. The PCH HD Audio controller hardwires the FIFO Watermark, either 32B or 64B based on the following. Bit(2:0) Description 000-011 Reserved 100 32 B Supported. The 32 B request is aligned to 32 B boundaries. 101 64 B Supported. The 64 B request is aligned to 64 B boundaries. 110-111 Reserved Input Stream: For input streams, the FIFOW value is determined by the EM3.ISRWS (SEM3.ISRWS) field. Output Stream: For output streams, the FIFOW value is determined by the EM4.OSRWS (SEM4.OSRWS) field.

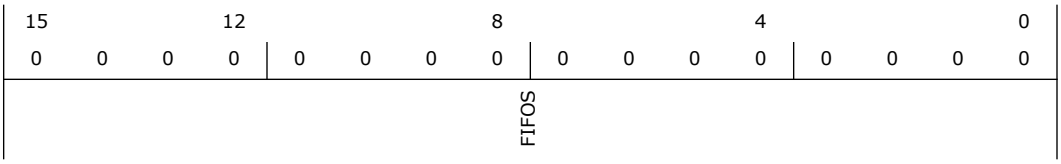
6.2.50 Input/Output Stream Descriptor x FIFO Size (OSD0FIFOS)—Offset 170h

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW/V	**FIFO Size (FIFOS):** When GCAP2.EEAC = 0, indicates the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time. This is the maximum number of bytes that may have been received into the HW buffer but not yet transferred out, and is also the maximum possible value that the PICB count will increase by at one time. The FIFO size is calculated based on the stream format programmed in (I/O)SDxFMT register, the min frame of buffering setting in EM(3/4)(SEM(3/4)).(I/O)SBSMFA[1:0] field, and the minimum buffer size threshold setting in EM2.BSMT[1:0] field. As the default value is zero, SW must write to the (I/O)SDxFMT register to kick off the FIFO size calculation, and read back to find out the HW allocated FIFO size. When GCAP2.EEAC = 1, this FIFOS value represent the minimum FIFO size HW required to operate efficiently. SW can program FIFOL register to extend the effective FIFO size in HW beyond this minimum value advertised. In this case, the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time, the maximum number of bytes that may have been received into the HW buffer but not yet transferred out, and also the maximum possible value that the PICB count will increase by one time, all these maximum value could be larger than FIFOS value, depending on the FIFOL register setting. When EM2.HWFIFOL = 1, this FIFOS value will reflect the larger FIFO size of up to 10 ms, if extra buffer space is available.

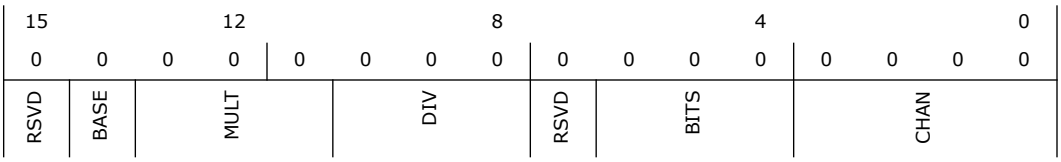
6.2.51 Input/Output Stream Descriptor x Format (OSD0FMT)—Offset 172h

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	Reserved.
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)
7	0h RO	Reserved.
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

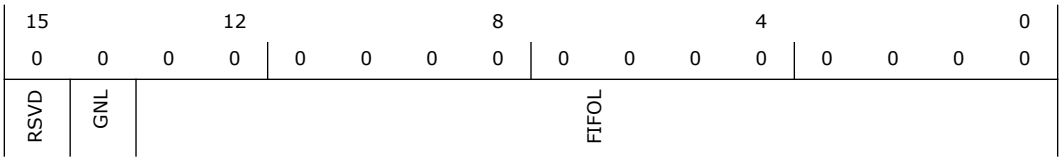
6.2.52 Input/Output Stream Descriptor x FIFO Limit (OSD0FIFOL)—Offset 174h

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	Reserved.
14	0h RW/L	**Granularity (GNL):** Granularity associated with LMT field definition. The LMT value needs to be multiplied with 125 us or 1 ms to get the access limit in time domain. 0 = 125 us 1 = 1 ms This bit is locked if GCAP2.EEAC = 0 (thus appear to be RO).
13:0	0h RW/L	**FIFO Limit (FIFOL):** Indicate how far the media player / application intend to process ahead, in units of time. HW can extend the effective FIFO size to fetch (for output stream) or evict (for input stream) more data in the cyclic buffer beyond the minimum FIFO size advertised in FIFOS register, up to this access limit. Need to multiply with the granularity (125 us vs. 1 ms) as defined in GNL bit, to get the actual processing ahead time. 0 = Disabled (FIFOS is the limit) 0001h 3FFFh = 1 16383 units When value) 0 (enabled), setting FIFOLC bit will trigger HW to evaluate the access limit change and update effective FIFO size (depending on the capability supported). SW shall make sure the FIFOL field is not changed in the progress of access limit change sequence. This bit is locked if GCAP2.EEAC = 0 (thus appear to be RO).

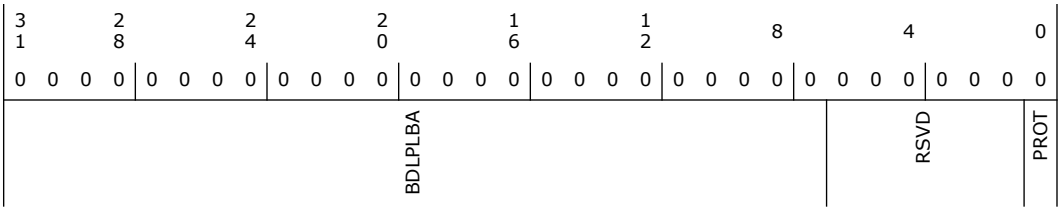
6.2.53 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD0BDLPLBA)—Offset 178h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RW	**Buffer Descriptor List Lower Base Address (BDLPLBA):** Lower address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or DMA transfers may be corrupted.
6:1	0h RO	Reserved.
0	0h RW/L	**Protect (PROT):** When this bit is set to 1, bits [31:7, 0] of this register are WO and will return 0's when read. When this bit is cleared to 0, bits [31:7, 0] are RW. Note that this bit can only be changed when all four bytes of this register are written in a single write operation. If less than four bytes are written this bit retains its previous value.

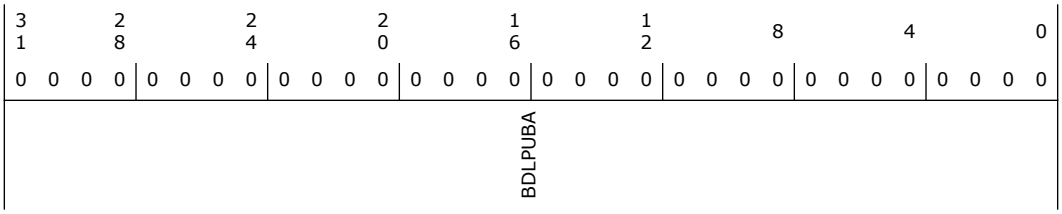
6.2.54 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD0BDLPUBA)—Offset 17Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/L	**Buffer Descriptor List Upper Base Address (BDLPUBA):** Upper 32-bit address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or the DMA transfer may be corrupted. Locked when GCAP.64OK = 0.

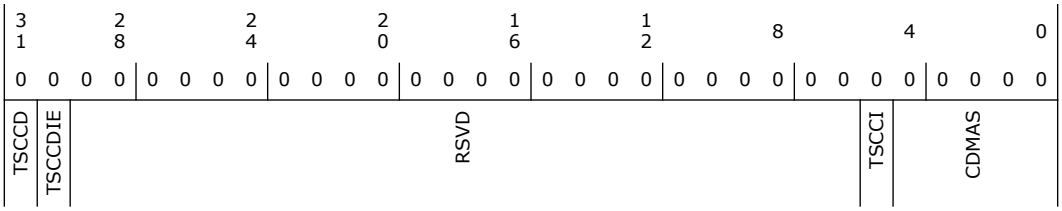
6.2.55 Global Time Synchronization Capture Control (GTSCC2)—Offset 4DCh

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C/V	**Time Stamp Counter Capture Done (TSCCD):** This bit is set when a valid TSC value has been captured: WALFCC, TSCCL, TSCCU, LLPFOC, LLPCL, and LLPCH contain valid data. The Intel HD Audio driver software must acknowledge the completion by writing 1 to clear this bit.
30	0h RW	**Time Stamp Counter Capture Done Interrupt Enable (TSCCDIE):** If set to 1, TSCCD bit can pass through to cause an interrupt status reported in INTSTS.CIS bit, and cause an interrupt to CPU if INTCTL.CIE = 1 and INTCTL.GIE = 1.
29:6	0h RO	Reserved.
5	0h RW/1S/V	**Time Stamp Counter Capture Initiate (TSCCI):** Write to 1 to initiate Global Time Synchronization capture for measuring TSC offset to local wall frame info. Cleared to 0 by hardware when the process is completed.
4:0	0h RW	**Capture DMA Select (CDMAS):** To select which DMA's LLPL, and LLPU value to be captured together with the TSC value. Bit 4 = 1 for ODMA, 0 for IDMA Bit 3:0 indicates the respective DMA engine index. Programmed before TSCCI = 1.

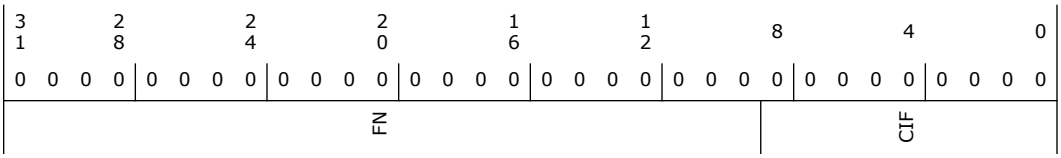
6.2.56 Wall Frame Counter Captured (WALFCC2)—Offset 4E0h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO/V	**Frame Number (FN):** Indicates the 23 bit frame number captured as a result of Global Time Synchronization capture request. Valid and static when GTSCC.TSCCD = 1.
8:0	0h RO/V	**Clock in Frame (CIF):** Indicates the 9 bit clock in frame value captured as a result of Global Time Synchronization capture request. Valid and static when GTSCC.TSCCD = 1.

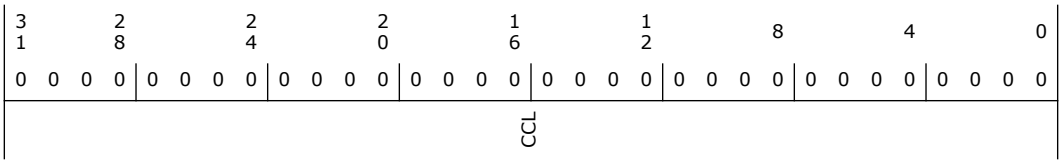
6.2.57 Time Stamp Counter Captured Lower (TSCCL2)—Offset 4E4h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Counter Captured Lower (CCL):** Indicates the lower 32 bit TSC value captured as a result of Global Time Synchronization capture request. Valid and static when GTSCC.TSCCD = 1.

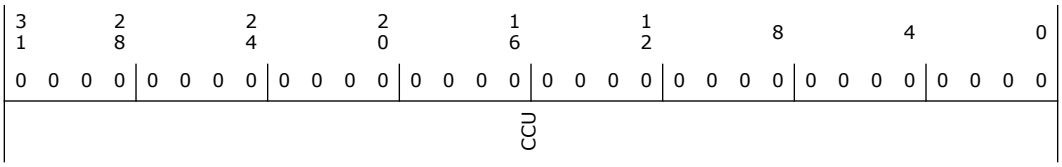
6.2.58 Time Stamp Counter Captured Upper (TSCCU2)—Offset 4E8h

Access Method

Type: MEM Register (Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Counter Captured Upper (CCU):** Indicates the upper 32 bit TSC value captured as a result of Global Time Synchronization capture request. Valid and static when GTSCC.TSCCD = 1.

6.2.59 Linear Link Position Frame Offset Captured (LLPFOC2)—Offset 4ECh

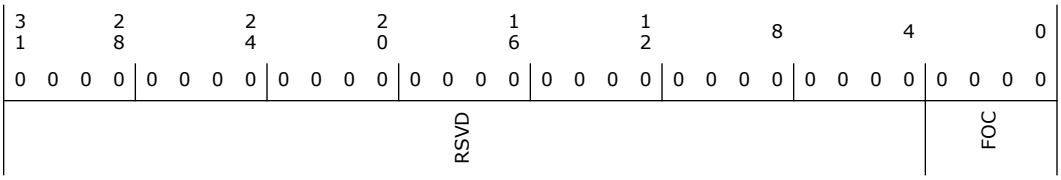
This register is to report additional accuracy details for captures made in between of two updates of LLP values, in number of 48 KHz HD Audio frames of the corresponding link. Audio streams with 44.1 KHz base rate and non zero divider FMT value will skip frames periodically on the Intel HD Audio link and Intel iDisplay Audio link in order to normalize its sampling rate to the 48 KHz HD Audio frame rate; hence; the frame offset will be useful in these cases.

Access Method

Type: MEM Register (Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3:0	0h RO/V	**Frame Offset Captured (FOC):** When the LLPCL and LLPCU registers are updated, this field records the elapsed number of 48 KHz HD Audio frames since the last LLP value change. Valid and static when GTSCC.TSCCD = 1

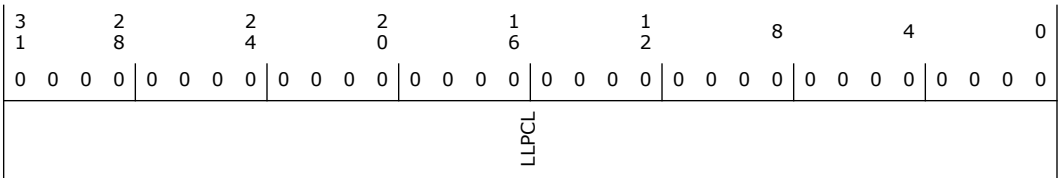
6.2.60 Linear Link Position Captured Lower (LLPCL2)—Offset 4F0h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Linear Link Position Captured Lower (LLPCL):** Indicates the lower 32 bit linear link position value of the link DMA captured as a result of Global Time Synchronization capture request. Note that the LLPCL value that is captured is the LLPL value at the previous HD Audio frame boundary, not the live LLPL register value which may be changing in the middle of the current frame. Valid and static when GTSCC.TSCCD = 1.

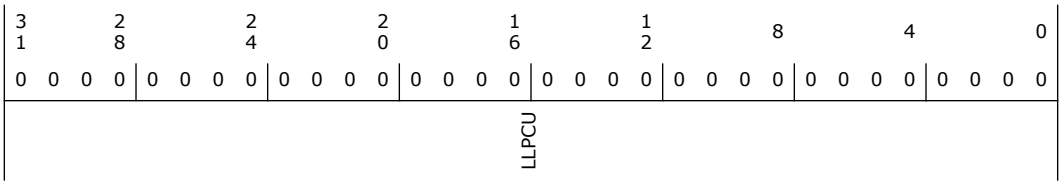
6.2.61 Linear Link Position Captured Upper (LLPCU2)—Offset 4F4h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Linear Link Position Captured Upper (LLPCU):** Indicates the upper 32 bit linear link position value of the link DMA captured as a result of Global Time Synchronization capture request. Note that the LLPCU value that is captured is the LLPU value at the previous HD Audio frame boundary, not the live LLPU register value which may be changing in the middle of the current frame. Valid and static when GTSCC.TSCCD = 1.

6.2.62 Global Time Synchronization Capability Header (GTSCH)—Offset 500h

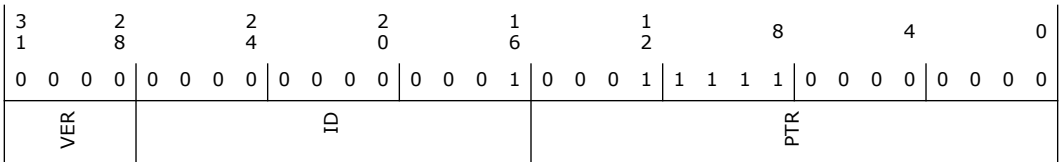
This register resides in Primary well (always on), or resides in Primary well (gated) with state retention, and reset by platform reset.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 11F00h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RW/L	**Capability Version (VER):** This field is an Intel HD Audio Specification defined version number that indicates the version of the capability structure present. Locked when FNCFG.BCLD = 1.
27:16	1h RW/L	**Capability Identifier (ID):** This field is an Intel HD Audio Specification defined ID number that indicates the nature and format of the capability. Locked when FNCFG.BCLD = 1.
15:0	1F00h RW/L	**Next Capability Pointer (PTR):** This field contains the offset to the next capability structure or 000h if no other items exist in the linked list of capabilities. Point to DMA resume capability. Locked when FNCFG.BCLD = 1.

6.2.63 Global Time Synchronization Capability Declaration (GTSCD)—Offset 504h

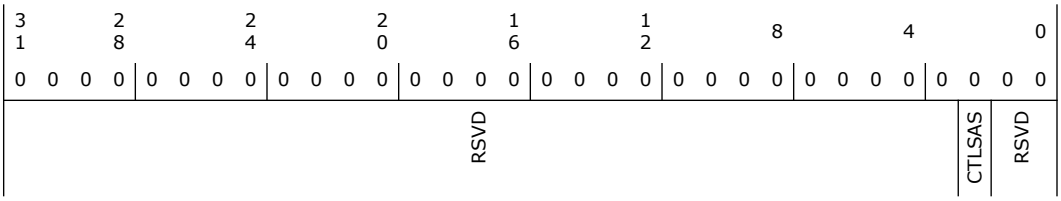
This register resides in Primary well (always on), or resides in Primary well (gated) with state retention, and reset by platform reset.
Note that CTLSAS = 1 is not a POR feature. It is only for testing purposes.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	Reserved.
2	0h RW/L	**Controller Based Synchronization Adjust Supported (CTLSAS):** When set, it indicates that the controller based synchronization adjustment is supported. By adjusting the global link clock which is used as reference clock for the codecs DAC / ADC, the codec will indirectly changing the rate of all its active streams. Locked when FNCFG.BCLD = 1.
1:0	0h RO	Reserved.

6.2.64 Global Time Synchronization Controller Adjust Control (GTSCTLAC)—Offset 50Ch

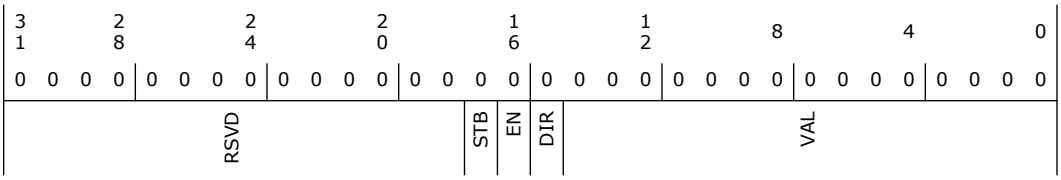
This register controls the fractional divider feature of the Audio PLL.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17	0h RW/L	**Strobe (STB):** SW set to 1 enables the Audio PLL latching in the EN bit and VAL field into the PLL CKT and reflect the new fractional divider state. SW must clear this bit to 0 after at least 200 ns to complete the strobe pulse sequence. For each strobing of a new fractional divider value, SW should wait for fractional divider settling time to reflect the new ppm value before initiating the next strobing of another new fractional divider value. Locked when GTSCD.CTLSAS = 0.
16	0h RW/L	**Enable (EN):** When set, it allows the fractional divider of the Audio PLL to operate, per the fractional value specified in VAL field. The value needs to be latched into the Audio PLL by pulsing the STB bit Locked when GTSCD.CTLSAS = 0.
15	0h RW/L	**Direction (DIR):** Indicates the direction of the ppm shift adjustment. 0: positive direction. 1: negative direction. Locked when GTSCD.CTLSAS = 0.
14:0	0h RW/L	**Value (VAL):** Indicates the value of the fractional divider if enabled. Locked when GTSCD.CTLSAS = 0.

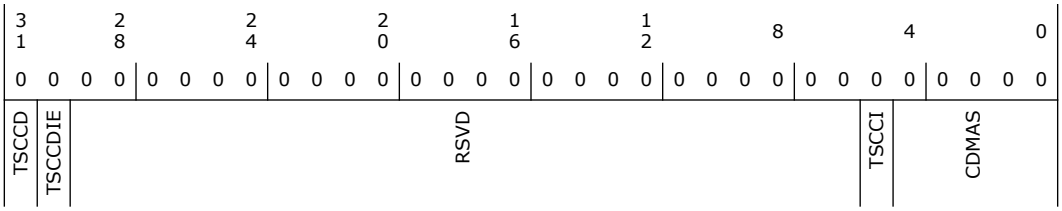
6.2.65 Global Time Synchronization Capture Control (GTSCC0)—Offset 520h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C/V	**Time Stamp Counter Capture Done (TSCCD):** This bit is set when a valid TSC value has been captured: WALFCC, TSCCL, TSCCU, LLPFOC, LLPCL, and LLPCH contain valid data. The Intel HD Audio driver software must acknowledge the completion by writing 1 to clear this bit.
30	0h RW	**Time Stamp Counter Capture Done Interrupt Enable (TSCCDIE):** If set to 1, TSCCD bit can pass through to cause an interrupt status reported in INTSTS.CIS bit, and cause an interrupt to CPU if INTCTL.CIE = 1 and INTCTL.GIE = 1.
29:6	0h RO	Reserved.
5	0h RW/1S/V	**Time Stamp Counter Capture Initiate (TSCCI):** Write to 1 to initiate Global Time Synchronization capture for measuring TSC offset to local wall frame info. Cleared to 0 by hardware when the process is completed.
4:0	0h RW	**Capture DMA Select (CDMAS):** To select which DMA's LLPL, and LLPU value to be captured together with the TSC value. Bit 4 = 1 for ODMA, 0 for IDMA Bit 3:0 indicates the respective DMA engine index. Programmed before TSCCI = 1.

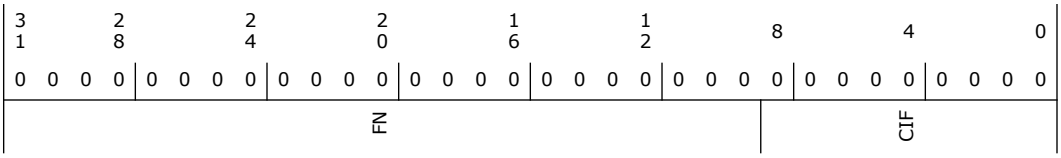
6.2.66 Wall Frame Counter Captured (WALFCC0)—Offset 524h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO/V	**Frame Number (FN):** Indicates the 23 bit frame number captured as a result of Global Time Synchronization capture request. Valid and static when GTSCC.TSCCD = 1.
8:0	0h RO/V	**Clock in Frame (CIF):** Indicates the 9 bit clock in frame value captured as a result of Global Time Synchronization capture request. Valid and static when GTSCC.TSCCD = 1.

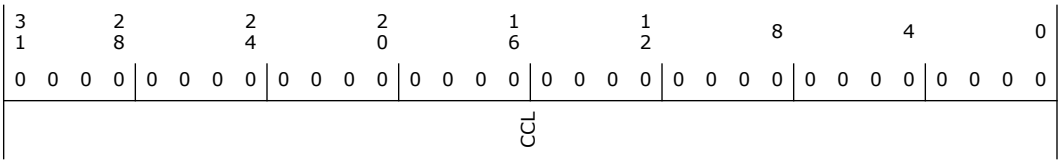
6.2.67 Time Stamp Counter Captured Lower (TSCCL0)—Offset 528h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Counter Captured Lower (CCL):** Indicates the lower 32 bit TSC value captured as a result of Global Time Synchronization capture request. Valid and static when GTSCC.TSCCD = 1.

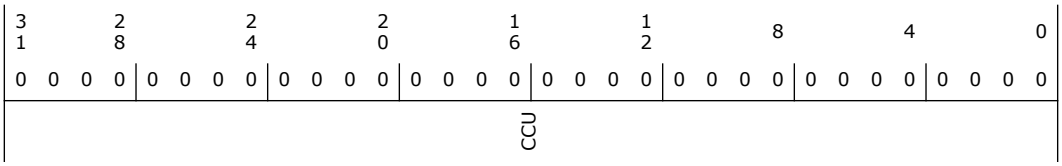
6.2.68 Time Stamp Counter Captured Upper (TSCCU0)—Offset 52Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Counter Captured Upper (CCU):** Indicates the upper 32 bit TSC value captured as a result of Global Time Synchronization capture request. Valid and static when GTSCC.TSCCD = 1.

6.2.69 Linear Link Position Frame Offset Captured (LLPFOC0)—Offset 534h

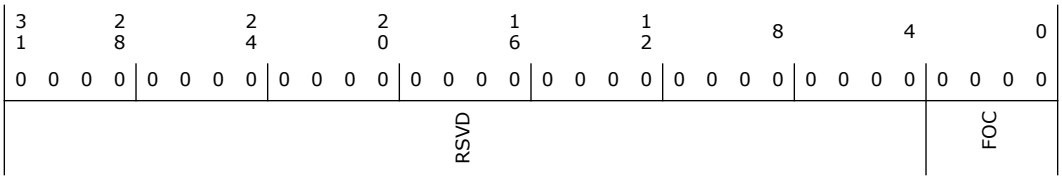
This register is to report additional accuracy details for captures made in between of two updates of LLP values, in number of 48 KHz HD Audio frames of the corresponding link. Audio streams with 44.1 KHz base rate and non zero divider FMT value will skip frames periodically on the Intel HD Audio link and Intel iDisplay Audio link in order to normalize its sampling rate to the 48 KHz HD Audio frame rate; hence; the frame offset will be useful in these cases.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3:0	0h RO/V	**Frame Offset Captured (FOC):** When the LLPCL and LLPCU registers are updated, this field records the elapsed number of 48 KHz HD Audio frames since the last LLP value change. Valid and static when GTSCC.TSCCD = 1

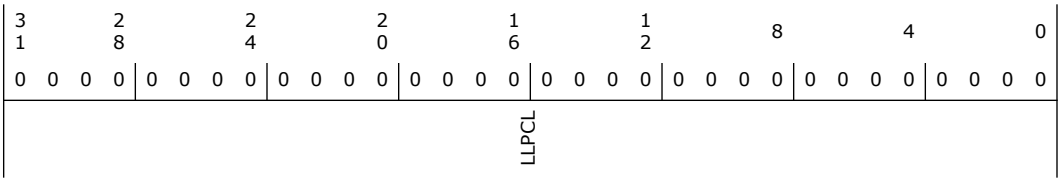
6.2.70 Linear Link Position Captured Lower (LLPCL0)—Offset 538h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Linear Link Position Captured Lower (LLPCL):** Indicates the lower 32 bit linear link position value of the link DMA captured as a result of Global Time Synchronization capture request. Note that the LLPCL value that is captured is the LLPL value at the previous HD Audio frame boundary, not the live LLPL register value which may be changing in the middle of the current frame. Valid and static when GTSCC.TSCCD = 1.

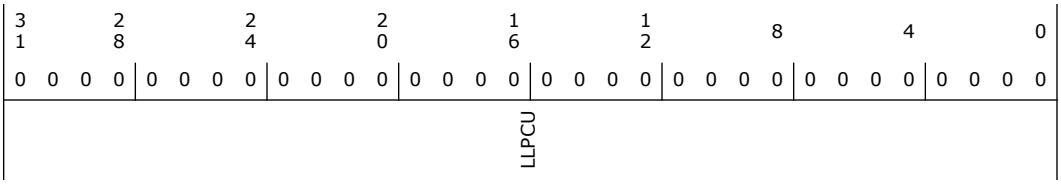
6.2.71 Linear Link Position Captured Upper (LLPCU0)—Offset 53Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Linear Link Position Captured Upper (LLPCU):** Indicates the upper 32 bit linear link position value of the link DMA captured as a result of Global Time Synchronization capture request. Note that the LLPCU value that is captured is the LLPU value at the previous HD Audio frame boundary, not the live LLPU register value which may be changing in the middle of the current frame. Valid and static when GTSCC.TSCCD = 1.

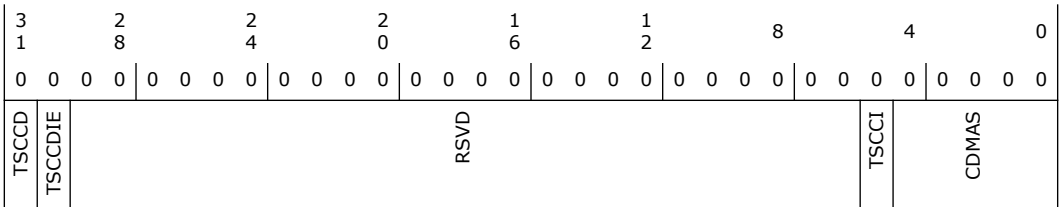
6.2.72 Global Time Synchronization Capture Control (GTSCC1)—Offset 540h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C/V	**Time Stamp Counter Capture Done (TSCCD):** This bit is set when a valid TSC value has been captured: WALFCC, TSCCL, TSCCU, LLPFOC, LLPCL, and LLPCH contain valid data. The Intel HD Audio driver software must acknowledge the completion by writing 1 to clear this bit.
30	0h RW	**Time Stamp Counter Capture Done Interrupt Enable (TSCCDIE):** If set to 1, TSCCD bit can pass through to cause an interrupt status reported in INTSTS.CIS bit, and cause an interrupt to CPU if INTCTL.CIE = 1 and INTCTL.GIE = 1.
29:6	0h RO	Reserved.
5	0h RW/1S/V	**Time Stamp Counter Capture Initiate (TSCCI):** Write to 1 to initiate Global Time Synchronization capture for measuring TSC offset to local wall frame info. Cleared to 0 by hardware when the process is completed.
4:0	0h RW	**Capture DMA Select (CDMAS):** To select which DMA's LLPL, and LLPU value to be captured together with the TSC value. Bit 4 = 1 for ODMA, 0 for IDMA Bit 3:0 indicates the respective DMA engine index. Programmed before TSCCI = 1.

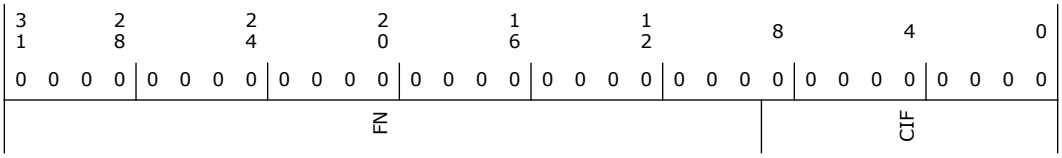
6.2.73 Wall Frame Counter Captured (WALFCC1)—Offset 544h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO/V	**Frame Number (FN):** Indicates the 23 bit frame number captured as a result of Global Time Synchronization capture request. Valid and static when GTSCC.TSCCD = 1.
8:0	0h RO/V	**Clock in Frame (CIF):** Indicates the 9 bit clock in frame value captured as a result of Global Time Synchronization capture request. Valid and static when GTSCC.TSCCD = 1.

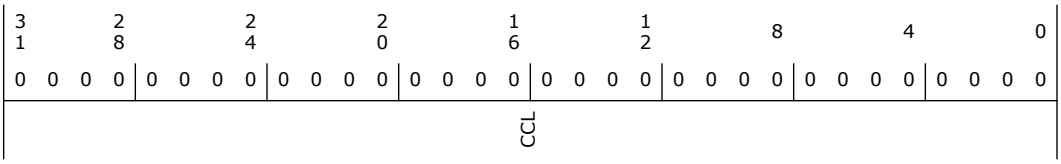
6.2.74 Time Stamp Counter Captured Lower (TSCCL1)—Offset 548h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Counter Captured Lower (CCL):** Indicates the lower 32 bit TSC value captured as a result of Global Time Synchronization capture request. Valid and static when GTSCC.TSCCD = 1.

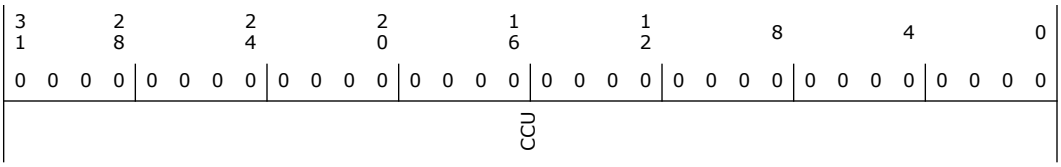
6.2.75 Time Stamp Counter Captured Upper (TSCCU1)—Offset 54Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Counter Captured Upper (CCU):** Indicates the upper 32 bit TSC value captured as a result of Global Time Synchronization capture request. Valid and static when GTSCC.TSCCD = 1.

6.2.76 Linear Link Position Frame Offset Captured (LLPFOC1)—Offset 554h

This register is to report additional accuracy details for captures made in between of two updates of LLP values, in number of 48 KHz HD Audio frames of the corresponding link. Audio streams with 44.1 KHz base rate and non zero divider FMT value will skip

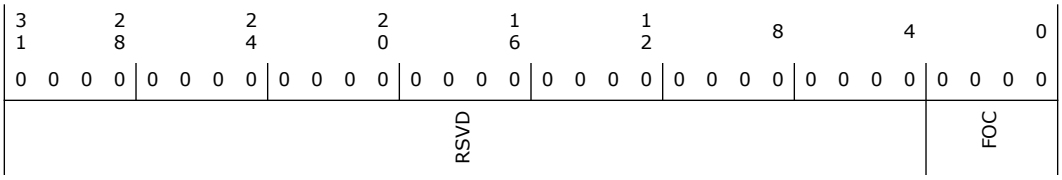
frames periodically on the Intel HD Audio link and Intel iDisplay Audio link in order to normalize its sampling rate to the 48 KHz HD Audio frame rate; hence; the frame offset will be useful in these cases.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3:0	0h RO/V	**Frame Offset Captured (FOC):** When the LLPCL and LLPCU registers are updated, this field records the elapsed number of 48 KHz HD Audio frames since the last LLP value change. Valid and static when GTSCC.TSCCD = 1

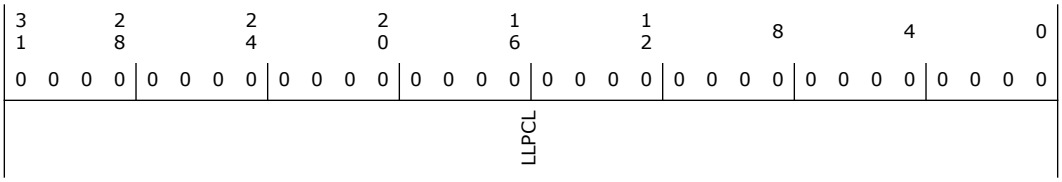
6.2.77 Linear Link Position Captured Lower (LLPCL1)—Offset 558h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Linear Link Position Captured Lower (LLPCL):** Indicates the lower 32 bit linear link position value of the link DMA captured as a result of Global Time Synchronization capture request. Note that the LLPCL value that is captured is the LLPL value at the previous HD Audio frame boundary, not the live LLPL register value which may be changing in the middle of the current frame. Valid and static when GTSCC.TSCCD = 1.

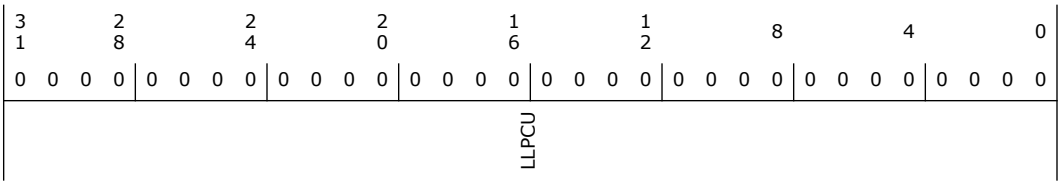
6.2.78 Linear Link Position Captured Upper (LLPCU1)—Offset 55Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Linear Link Position Captured Upper (LLPCU):** Indicates the upper 32 bit linear link position value of the link DMA captured as a result of Global Time Synchronization capture request. Note that the LLPCU value that is captured is the LLPU value at the previous HD Audio frame boundary, not the live LLPU register value which may be changing in the middle of the current frame. Valid and static when GTSCC.TSCCD = 1.

6.2.79 Processing Pipe Capability Header (PPCH)—Offset 800h

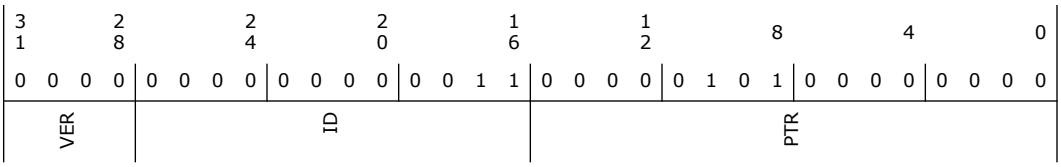
This register resides in Primary well (always on), or resides in Primary well (gated) with state retention, and reset by platform reset.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 30500h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RW/L	**Capability Version (VER):** This field is an Intel HD Audio Specification defined version number that indicates the version of the capability structure present. Locked when FNCFG.BCLD = 1.
27:16	3h RW/L	**Capability Identifier (ID):** This field is an Intel HD Audio Specification defined ID number that indicates the nature and format of the capability. Locked when FNCFG.BCLD = 1.
15:0	500h RW/L	**Next Capability Pointer (PTR):** This field contains the offset to the next capability structure or 000h if no other items exist in the linked list of capabilities. Point to Global Time Synchronization capability. Locked when FNCFG.BCLD = 1.

6.2.80 Processing Pipe Control (PPCTL)—Offset 804h

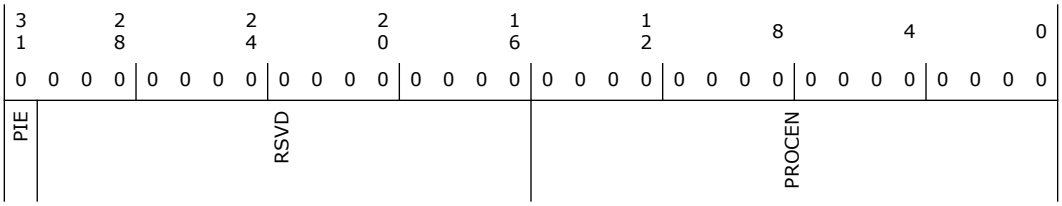
This register is not affected by stream reset.
Note that the PROCEN bit should only be modified when the corresponding host DMA and link DMA are idle, i.e. RUN bits are cleared, and the DMA contexts have been destroyed through SRST bits if it was previously activated.
Note that GPROCEN bit does not really enable or disable the Audio DSP operation, but mainly to workaround some legacy Intel HD Audio driver software such that if GPROCEN = 0, ADSPxBA (BAR2) is mapped to the Intel HD Audio memory mapped configuration registers, for compliancy with some legacy SW implementation. If GPROCEN = 1, only then ADSPxBA (BAR2) is mapped to the actual Audio DSP memory mapped configuration registers.
The number of PROCEN bits in this register is depending on the total number of stream DMA implemented, represented as x in the register table.
The x value is determined by the parameter equation: HSTISC + HSTOSC. For SPT implementation, x = 16.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Processing Interrupt Enable (PIE):** Enables the general interrupt for the Audio DSP function. When set to 1 (and GIE is enabled), the Audio DSP generates an interrupt when the PIS bit gets set.
30:16	0h RO	Reserved.
15:0	0h RW	**Processing Enable (PROCEN):** When set to 1 the DMA engine associated with this stream will be enabled to route the audio stream to DSP audio pipes in the Audio DSP for processing. When cleared to 0 the DMA engine associated with this stream will be bypassing the Audio DSP and route the audio stream directly to the audio link.

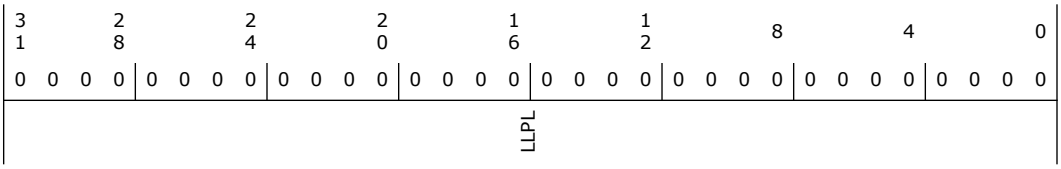
6.2.81 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC0LLPL)—Offset 810h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

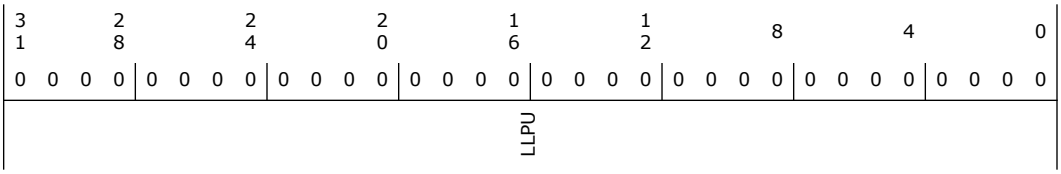
6.2.82 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC0LLPU)—Offset 814h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

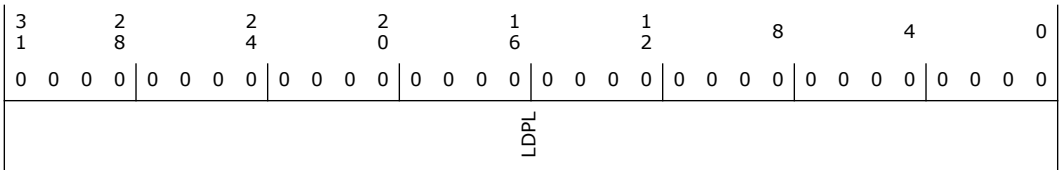
6.2.83 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC0LDPL)—Offset 818h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

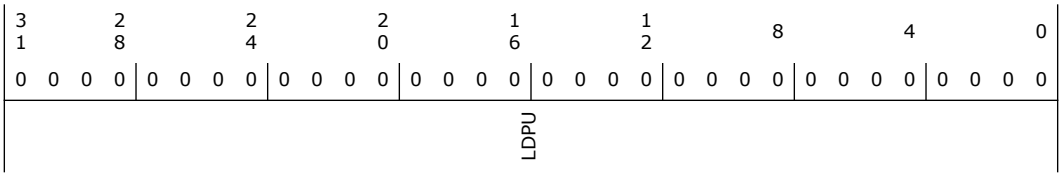
6.2.84 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC0LDPU)—Offset 81Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

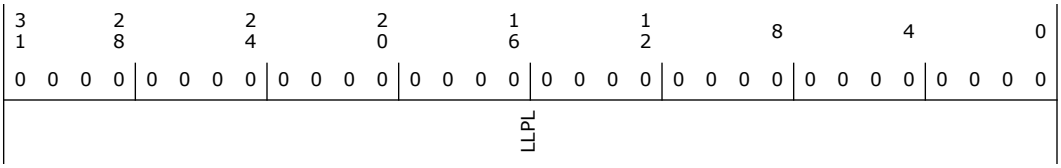
6.2.85 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC1LLPL)—Offset 820h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

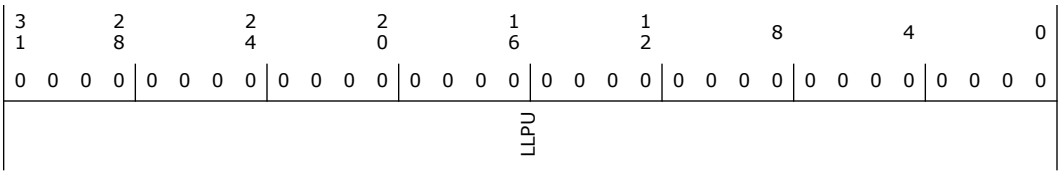
6.2.86 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC1LLPU)—Offset 824h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

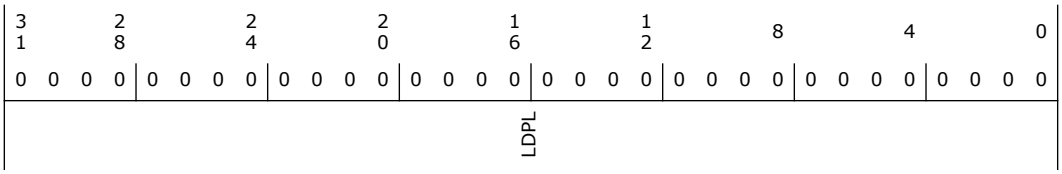
6.2.87 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC1LDPL)—Offset 828h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

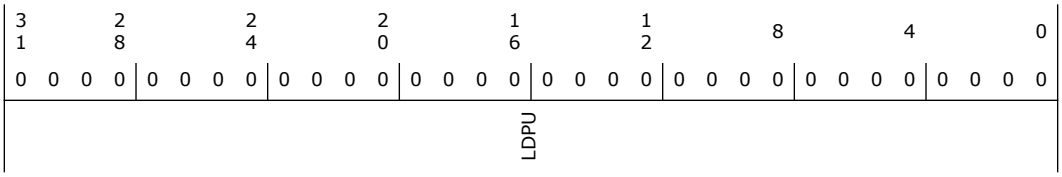
6.2.88 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC1LDPU)—Offset 82Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

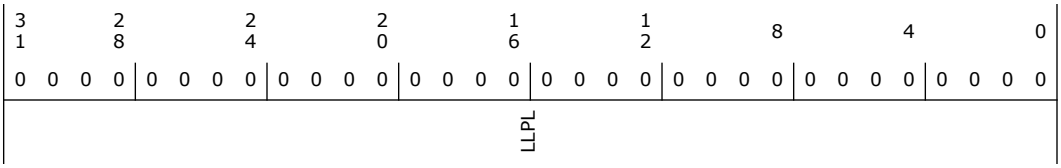
6.2.89 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC2LLPL)—Offset 830h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

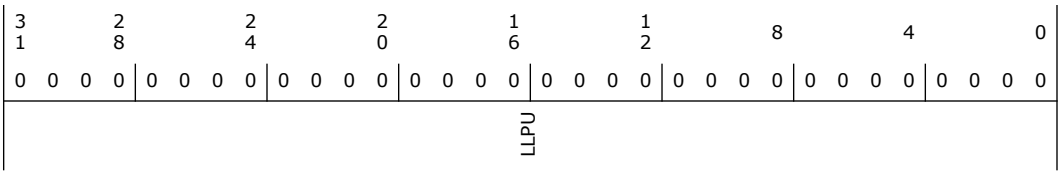
6.2.90 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC2LLPU)—Offset 834h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

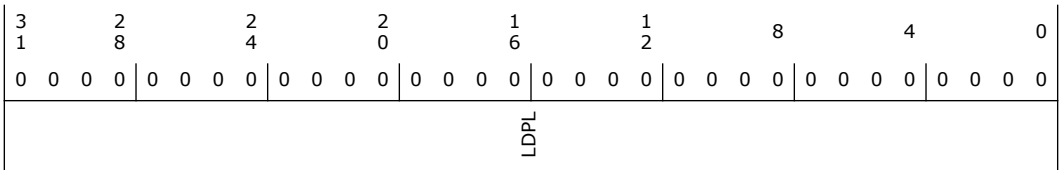
6.2.91 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC2LDPL)—Offset 838h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

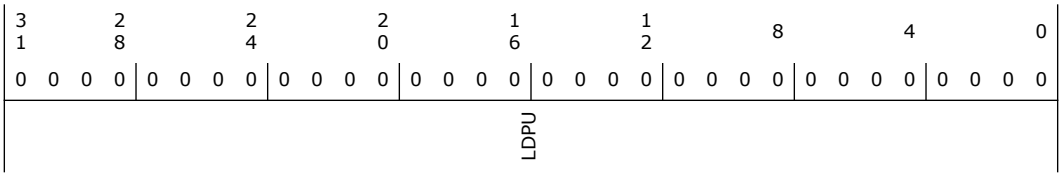
6.2.92 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC2LDPU)—Offset 83Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

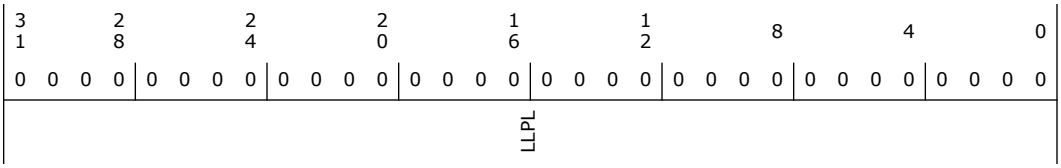
6.2.93 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC3LLPL)—Offset 840h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

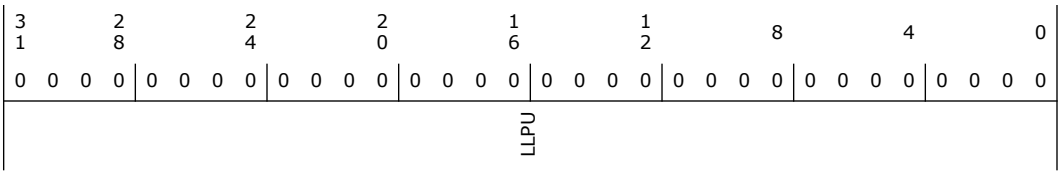
6.2.94 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC3LLPU)—Offset 844h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

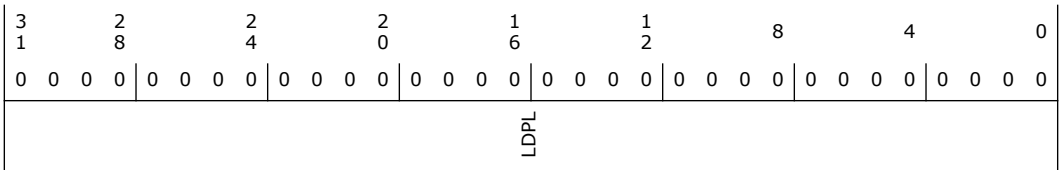
6.2.95 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC3LDPL)—Offset 848h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

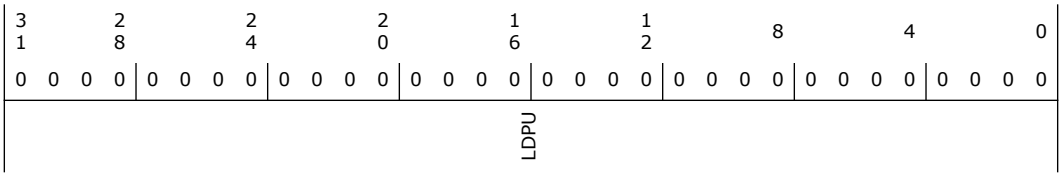
6.2.96 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC3LDPU)—Offset 84Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

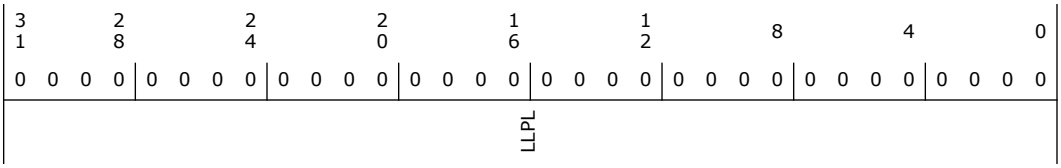
6.2.97 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC4LLPL)—Offset 850h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

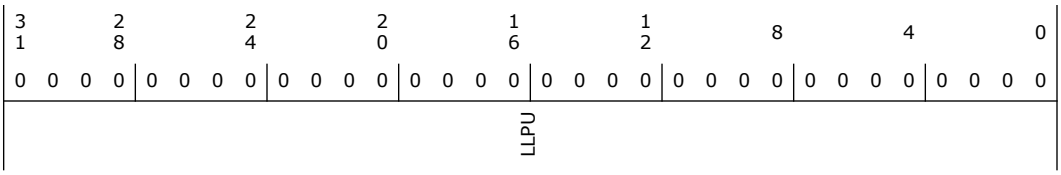
6.2.98 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC4LLPU)—Offset 854h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

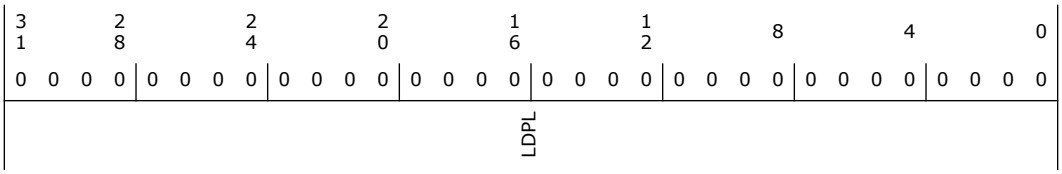
6.2.99 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC4LDPL)—Offset 858h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

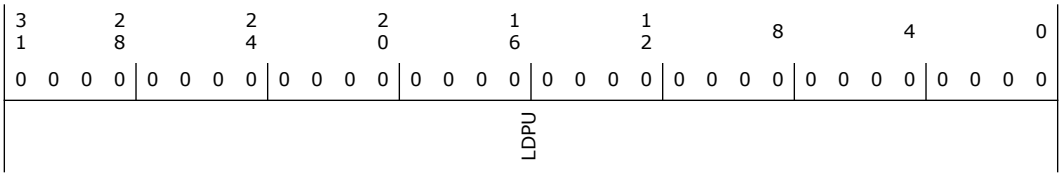
6.2.100 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC4LDPU)—Offset 85Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

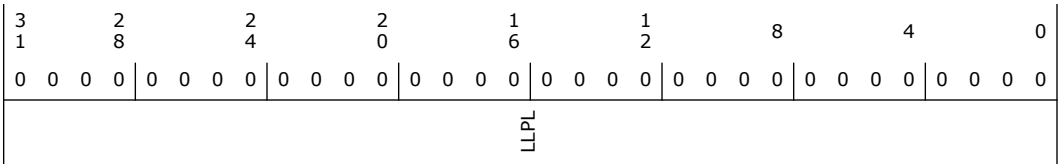
6.2.101 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC5LLPL)—Offset 860h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

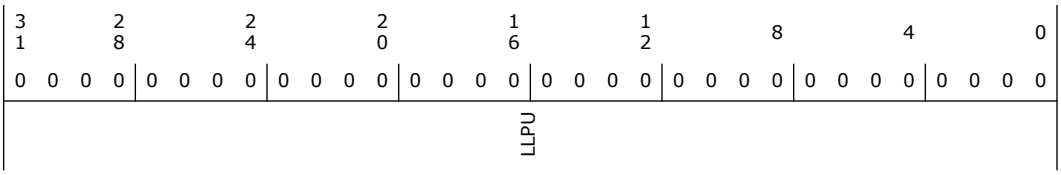
6.2.102 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC5LLPU)—Offset 864h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

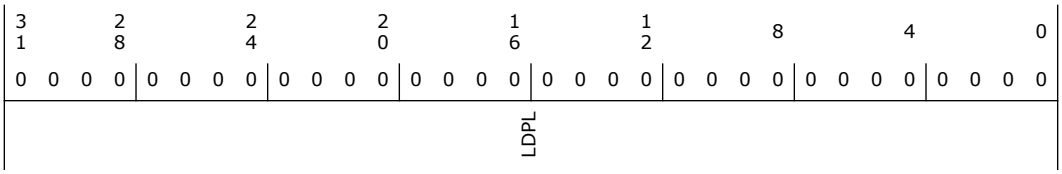
6.2.103 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC5LDPL)—Offset 868h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

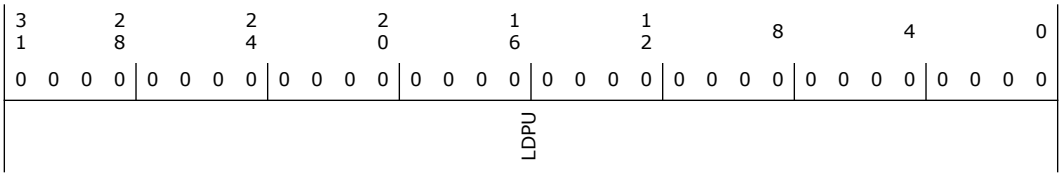
6.2.104 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC5LDPU)—Offset 86Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

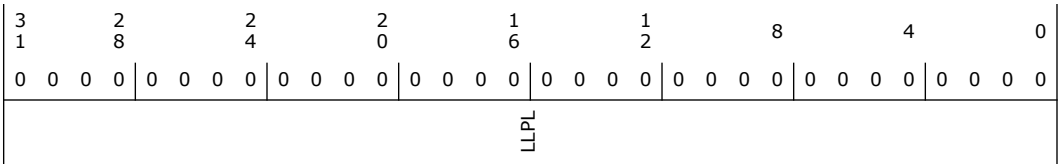
6.2.105 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC6LLPL)—Offset 870h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

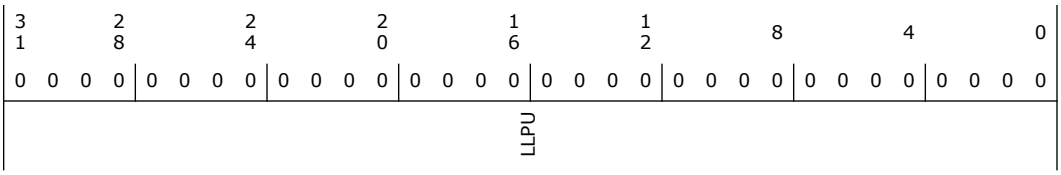
6.2.106 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC6LLPU)—Offset 874h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

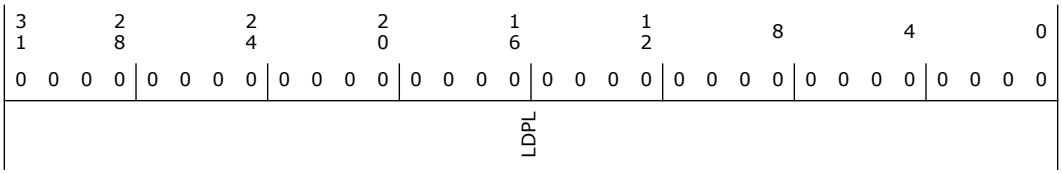
6.2.107 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC6LDPL)—Offset 878h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

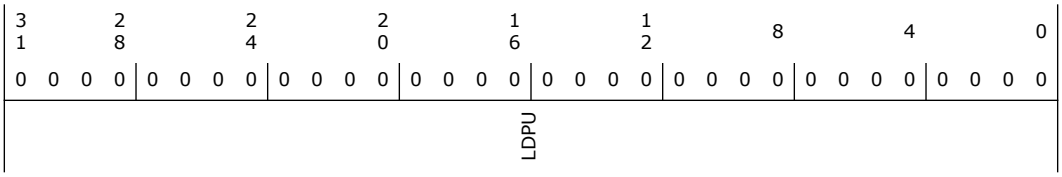
6.2.108 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC6LDPU)—Offset 87Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

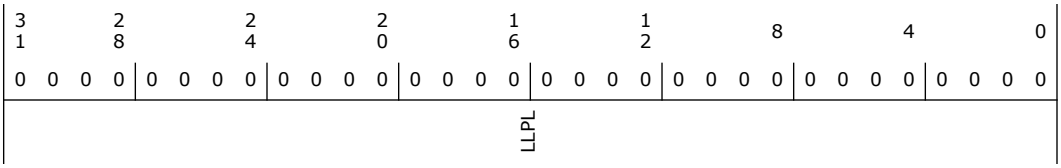
6.2.109 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC0LLPL)—Offset 880h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

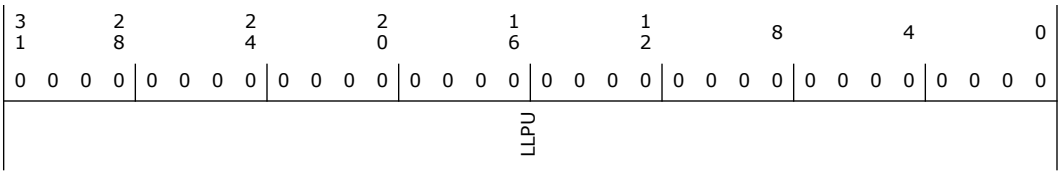
6.2.110 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC0LLPU)—Offset 884h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

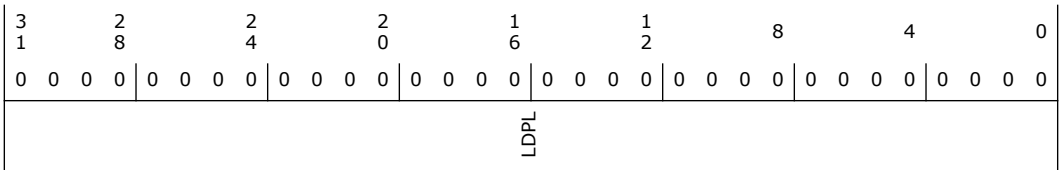
6.2.111 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC0LDPL)—Offset 888h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

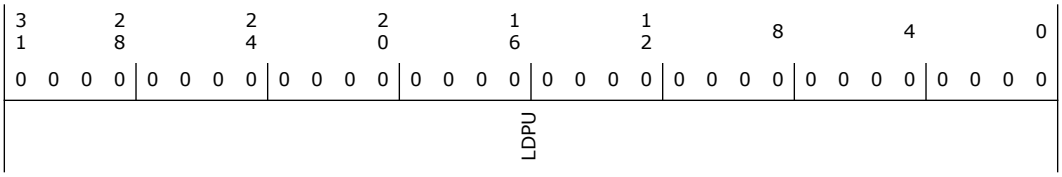
6.2.112 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC0LDPU)—Offset 88Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

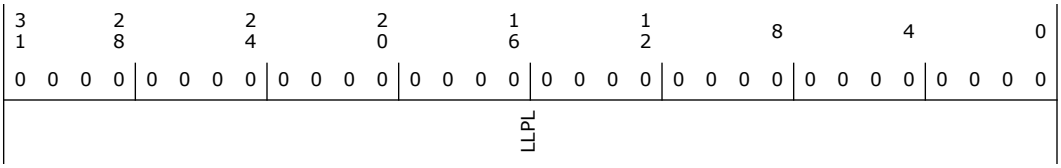
6.2.113 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC1LLPL)—Offset 890h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

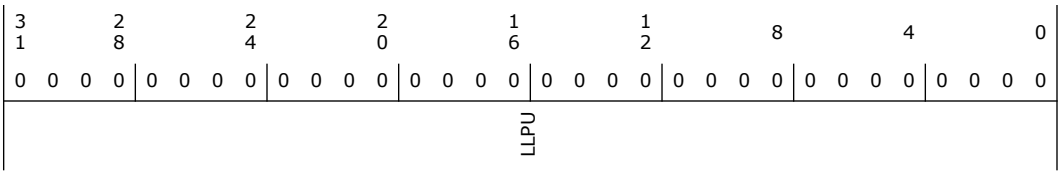
6.2.114 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC1LLPU)—Offset 894h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

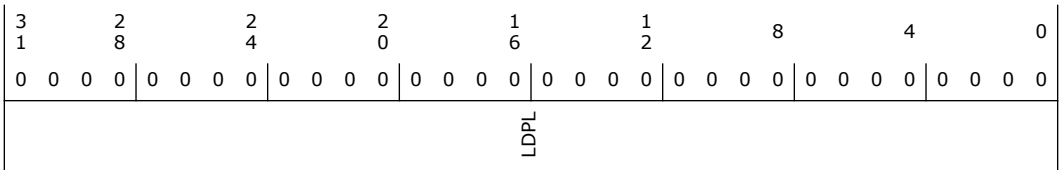
6.2.115 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC1LDPL)—Offset 898h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

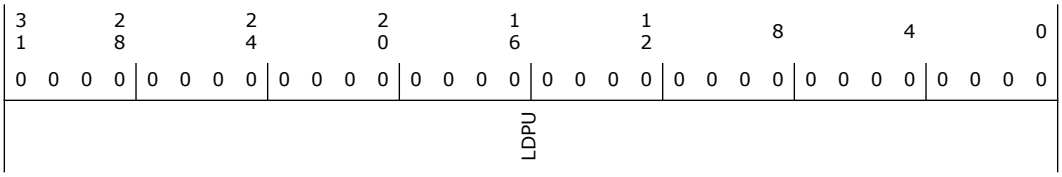
6.2.116 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC1LDPU)—Offset 89Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

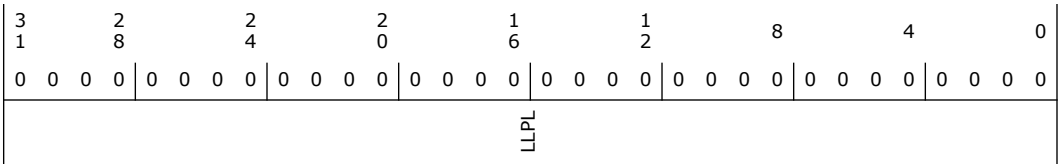
6.2.117 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC2LLPL)—Offset 8A0h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

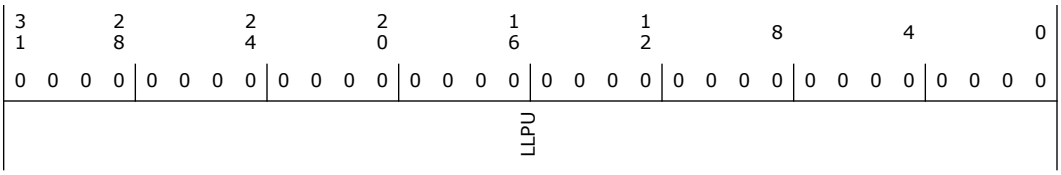
6.2.118 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC2LLPU)—Offset 8A4h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

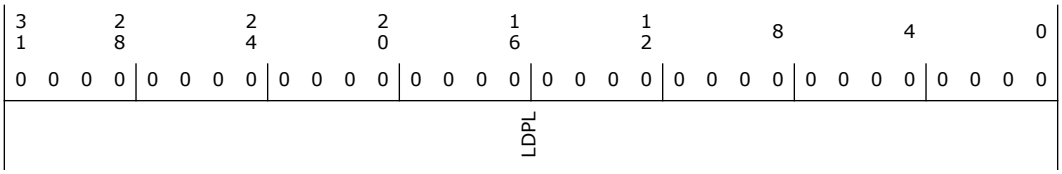
6.2.119 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC2LDPL)—Offset 8A8h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

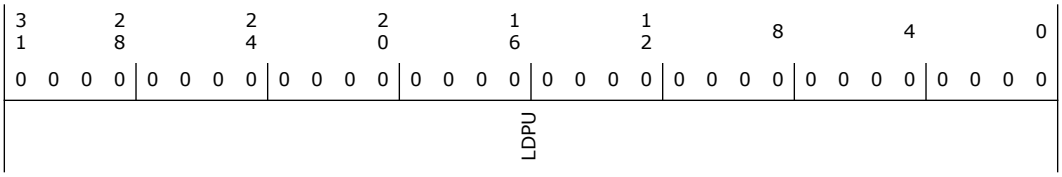
6.2.120 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC2LDPU)—Offset 8ACh

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

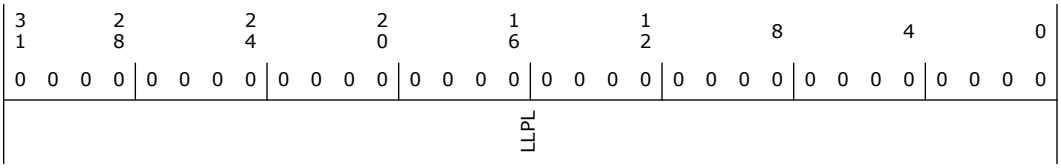
6.2.121 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC3LLPL)—Offset 8B0h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

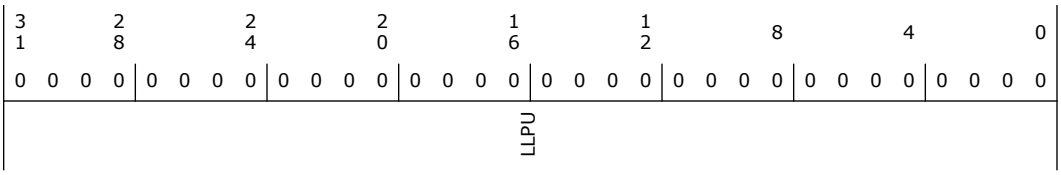
6.2.122 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC3LLPU)—Offset 8B4h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

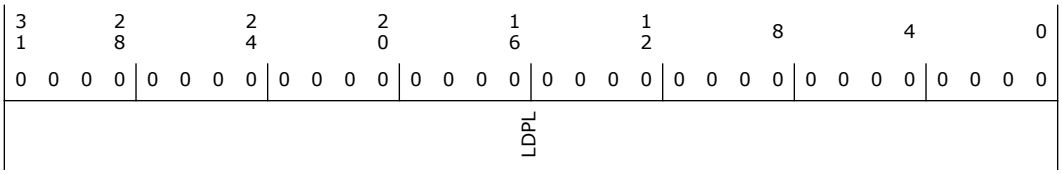
6.2.123 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC3LDPL)—Offset 8B8h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

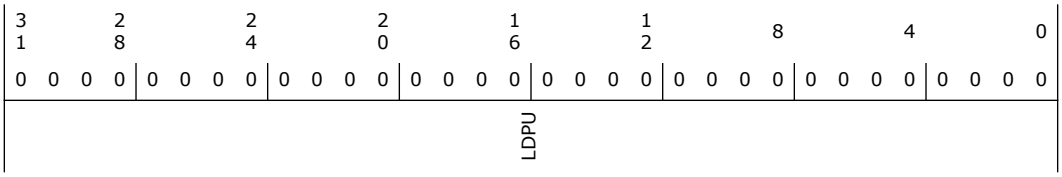
6.2.124 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC3LDPU)—Offset 8BCh

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

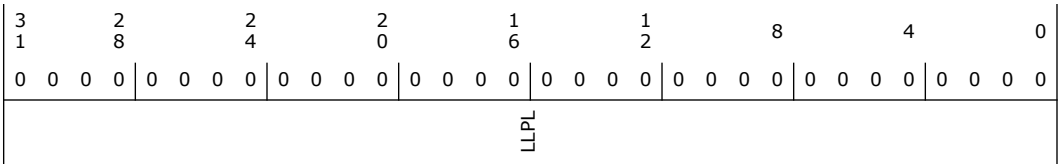
6.2.125 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC4LLPL)—Offset 8C0h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

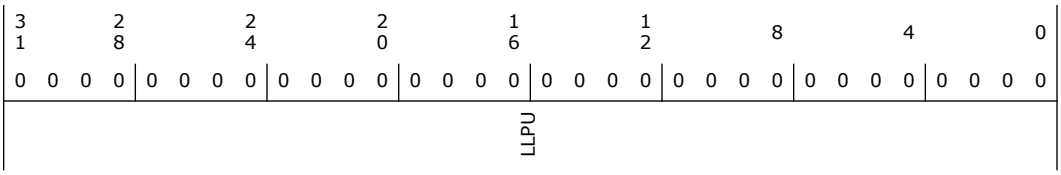
6.2.126 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC4LLPU)—Offset 8C4h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

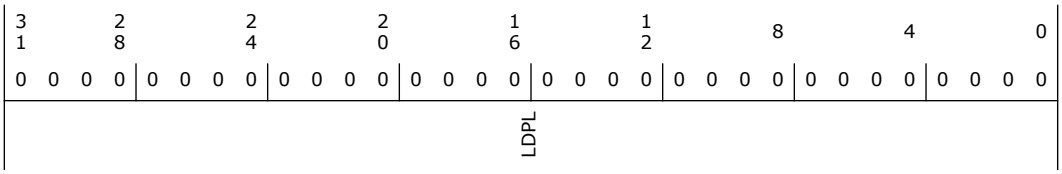
6.2.127 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC4LDPL)—Offset 8C8h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

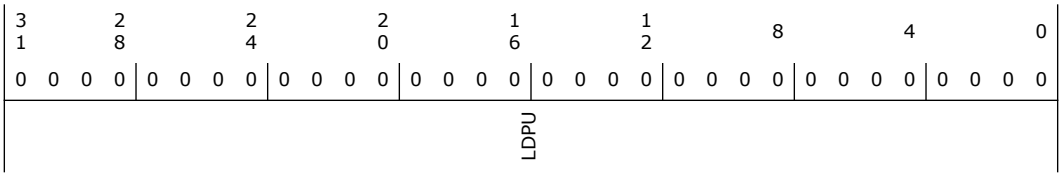
6.2.128 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC4LDPU)—Offset 8CCh

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

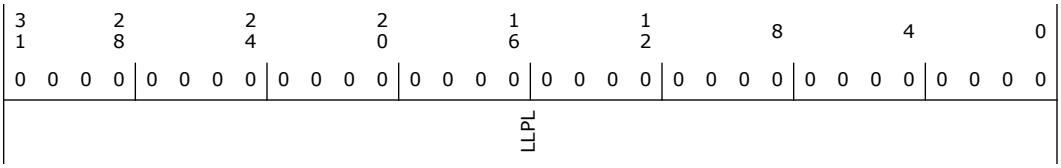
6.2.129 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC5LLPL)—Offset 8D0h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

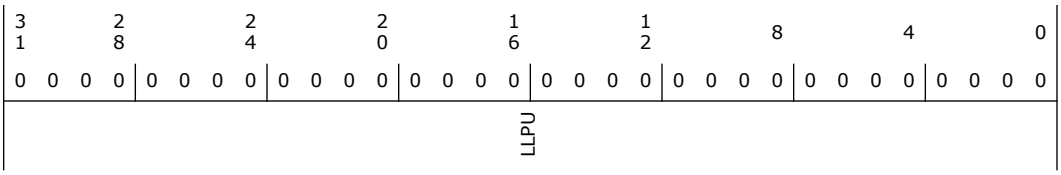
6.2.130 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC5LLPU)—Offset 8D4h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

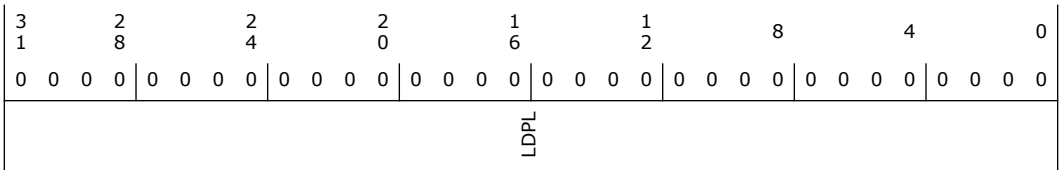
6.2.131 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC5LDPL)—Offset 8D8h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

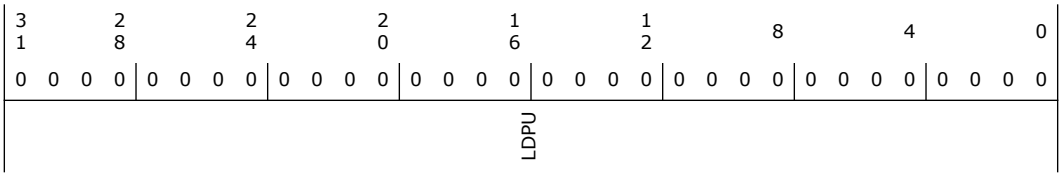
6.2.132 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC5LDPU)—Offset 8DCh

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

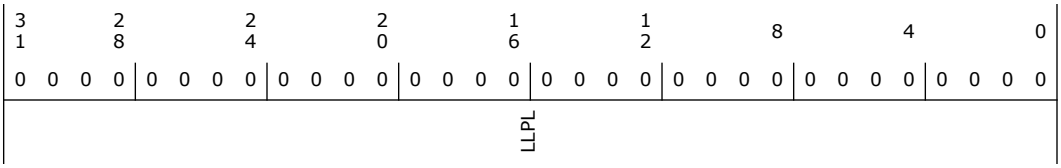
6.2.133 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC6LLPL)—Offset 8E0h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

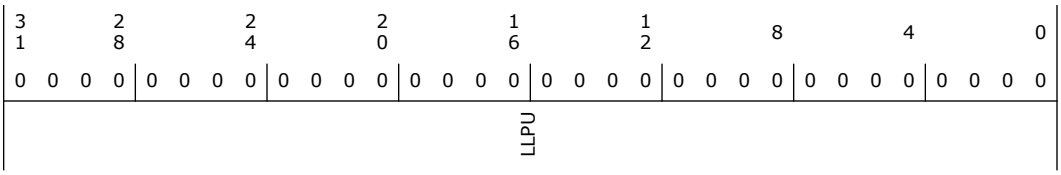
6.2.134 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC6LLPU)—Offset 8E4h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

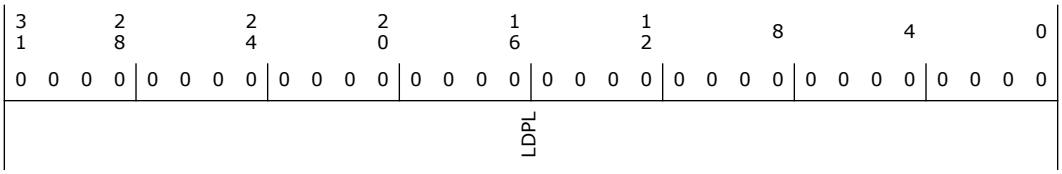
6.2.135 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC6LDPL)—Offset 8E8h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

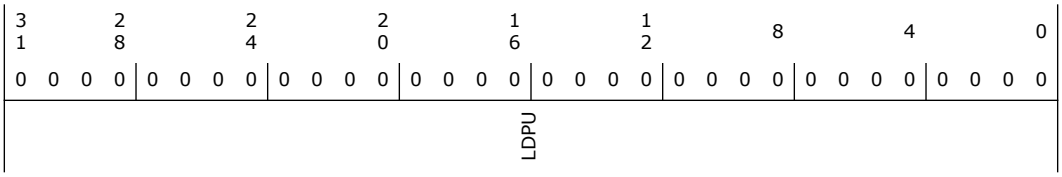
6.2.136 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC6LDPU)—Offset 8ECh

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

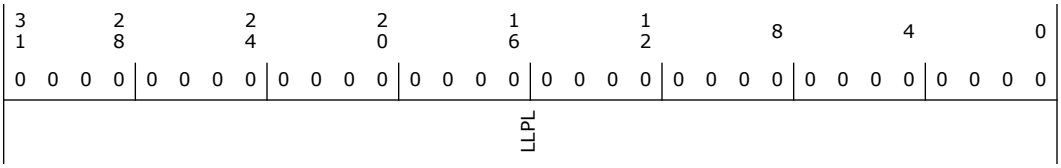
6.2.137 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC7LLPL)—Offset 8F0h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

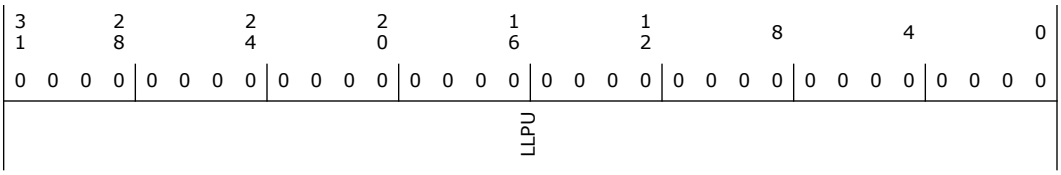
6.2.138 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC7LLPU)—Offset 8F4h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

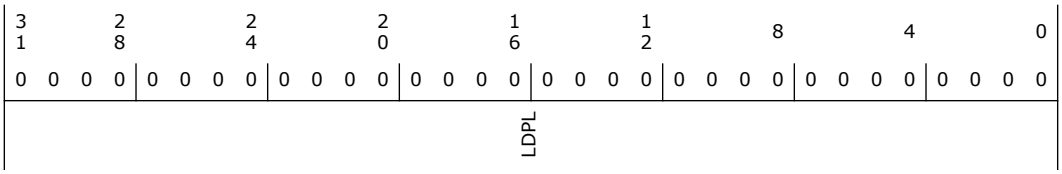
6.2.139 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC7LDPL)—Offset 8F8h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

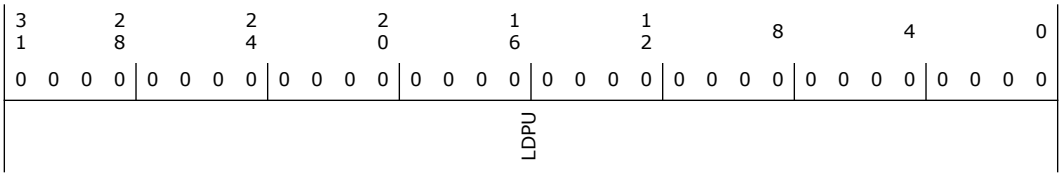
6.2.140 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC7LDPU)—Offset 8FCh

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

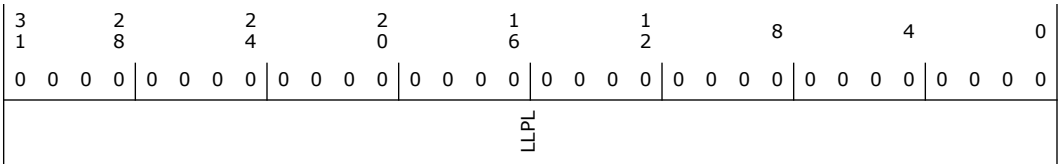
6.2.141 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC8LLPL)—Offset 900h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

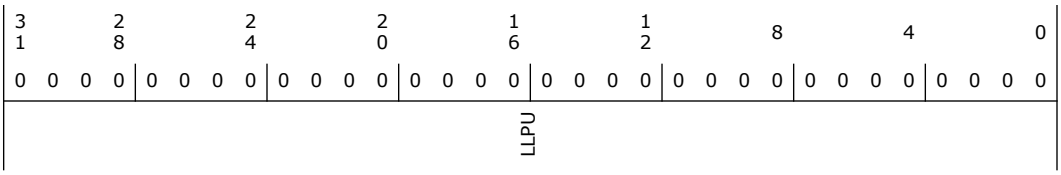
6.2.142 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC8LLPU)—Offset 904h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

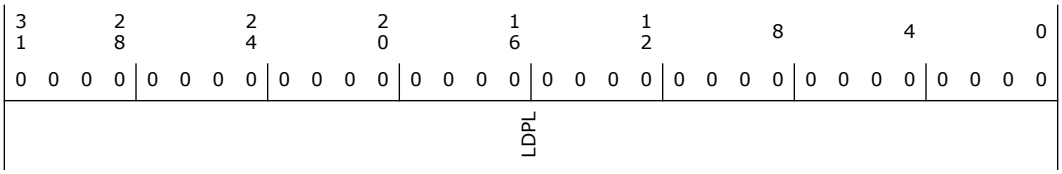
6.2.143 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC8LDPL)—Offset 908h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

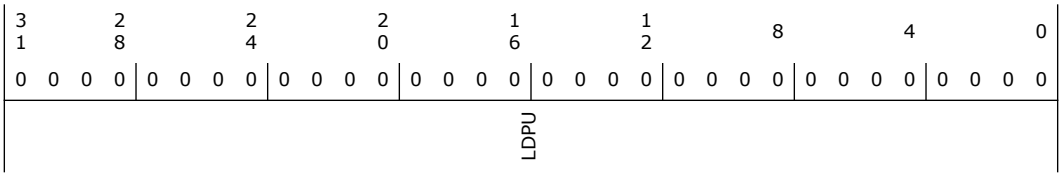
6.2.144 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC8LDPU)—Offset 90Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

6.2.145 Input/Output Processing Pipe's Link Connection x Control (IPPLC0CTL)—Offset 910h

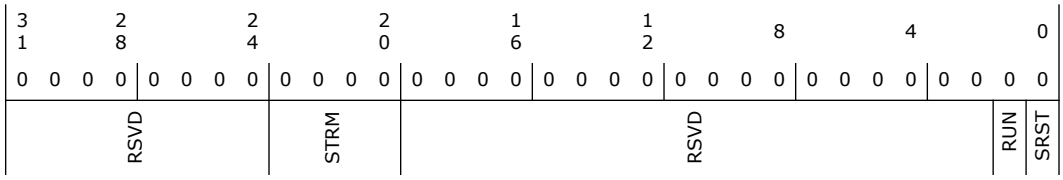
SRST bit is not affected by stream reset.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. 0000=Reserved (Indicates Unused) 0001=Stream 1 ... 1110=Stream 14 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Bit Range	Default & Access	Field Name (ID): Description
19:2	0h RO	Reserved.
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

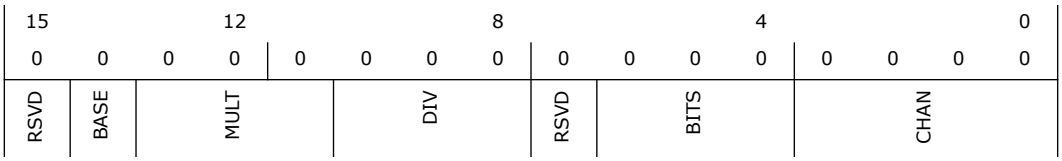
6.2.146 Input/Output Processing Pipe's Link Connection x Format (IPPLC0FMT)—Offset 914h

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	Reserved.
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	Reserved.
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

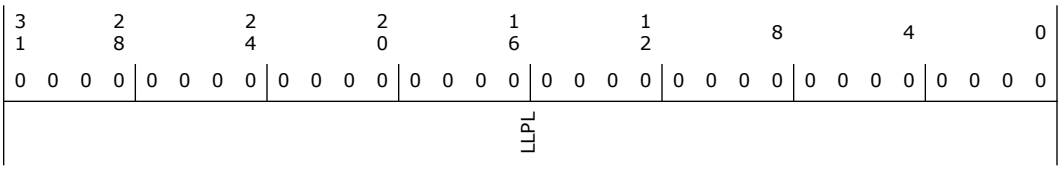
6.2.147 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC0LLPL)—Offset 918h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

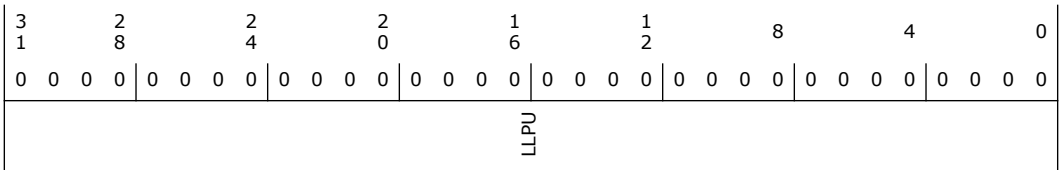
6.2.148 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC0LLPU)—Offset 91Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

6.2.149 Input/Output Processing Pipe's Link Connection x Control (IPPLC1CTL)—Offset 920h

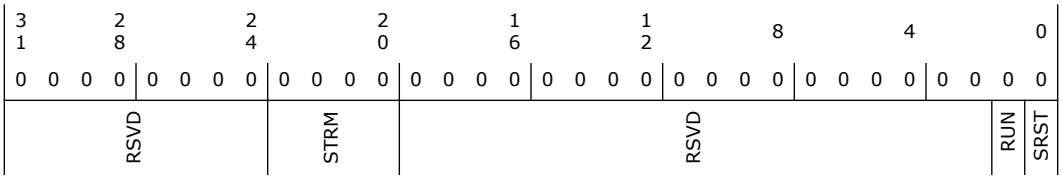
SRST bit is not affected by stream reset.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. 0000=Reserved (Indicates Unused) 0001=Stream 1 ... 1110=Stream 14 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Bit Range	Default & Access	Field Name (ID): Description
19:2	0h RO	Reserved.
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

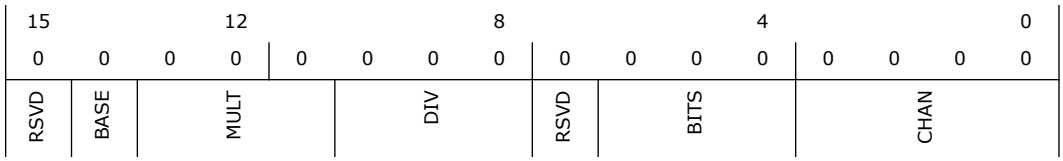
6.2.150 Input/Output Processing Pipe's Link Connection x Format (IPPLC1FMT)—Offset 924h

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	Reserved.
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	Reserved.
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

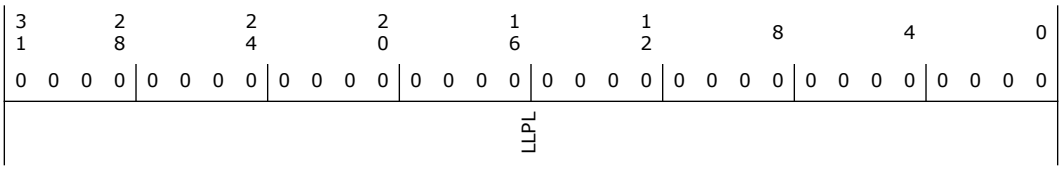
6.2.151 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC1LLPL)—Offset 928h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

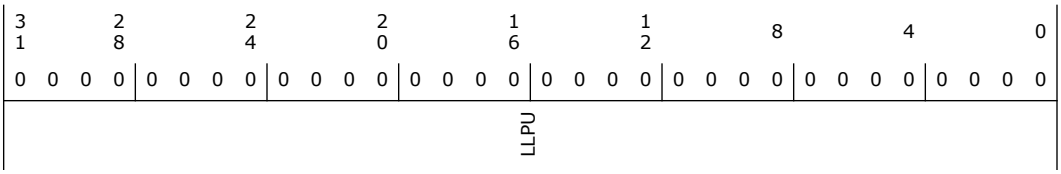
6.2.152 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC1LLPU)—Offset 92Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

6.2.153 Input/Output Processing Pipe's Link Connection x Control (IPPLC2CTL)—Offset 930h

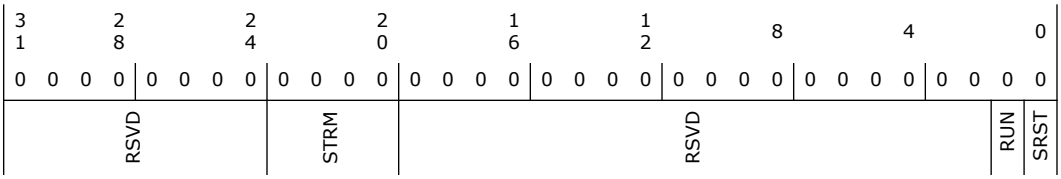
SRST bit is not affected by stream reset.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. 0000=Reserved (Indicates Unused) 0001=Stream 1 ... 1110=Stream 14 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Bit Range	Default & Access	Field Name (ID): Description
19:2	0h RO	Reserved.
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

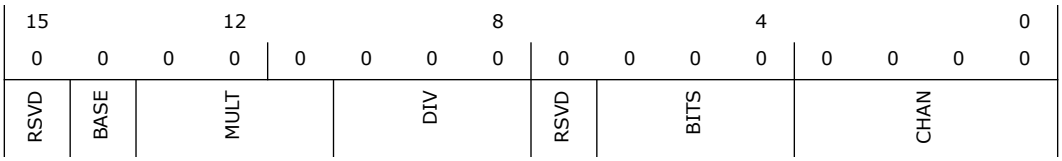
6.2.154 Input/Output Processing Pipe's Link Connection x Format (IPPLC2FMT)—Offset 934h

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	Reserved.
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	Reserved.
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

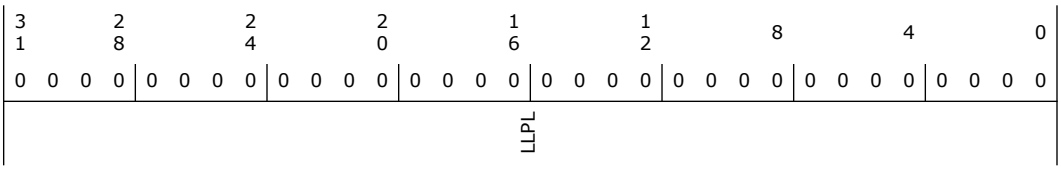
6.2.155 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC2LLPL)—Offset 938h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

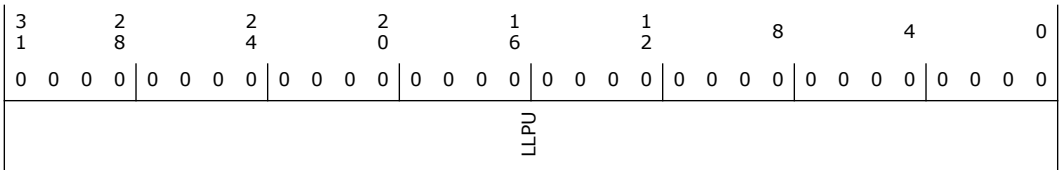
6.2.156 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC2LLPU)—Offset 93Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

6.2.157 Input/Output Processing Pipe's Link Connection x Control (IPPLC3CTL)—Offset 940h

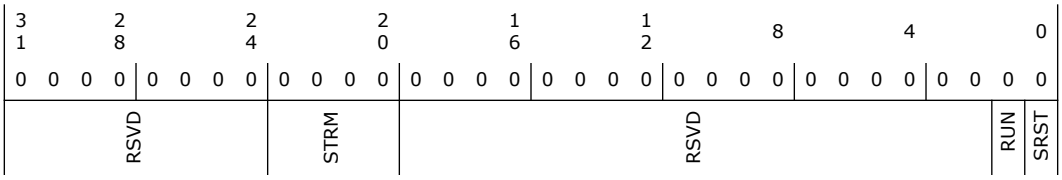
SRST bit is not affected by stream reset.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. 0000=Reserved (Indicates Unused) 0001=Stream 1 ... 1110=Stream 14 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Bit Range	Default & Access	Field Name (ID): Description
19:2	0h RO	Reserved.
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

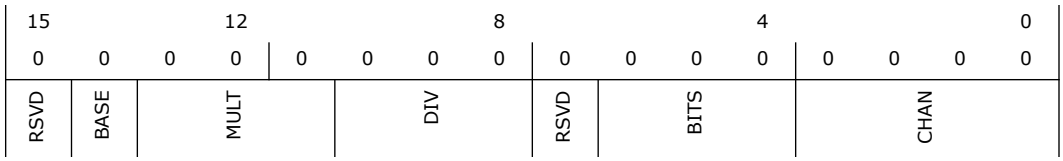
6.2.158 Input/Output Processing Pipe's Link Connection x Format (IPPLC3FMT)—Offset 944h

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	Reserved.
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	Reserved.
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

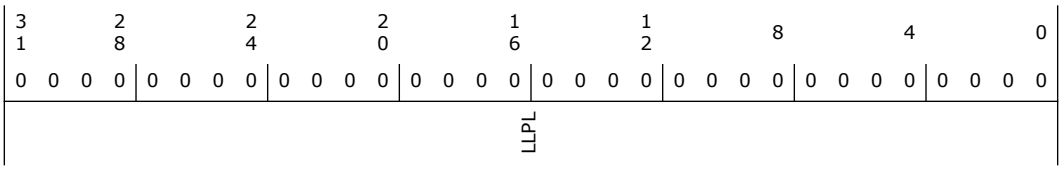
6.2.159 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC3LLPL)—Offset 948h

Access Method

Type: MEM Register (Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

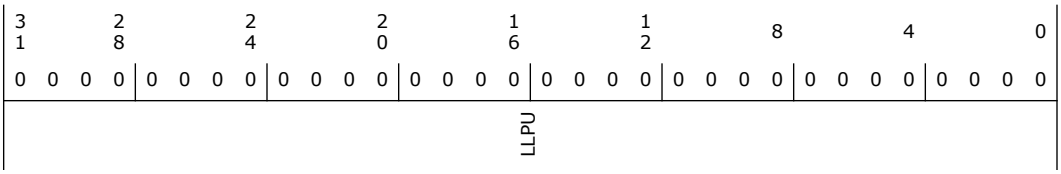
6.2.160 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC3LLPU)—Offset 94Ch

Access Method

Type: MEM Register (Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

6.2.161 Input/Output Processing Pipe's Link Connection x Control (IPPLC4CTL)—Offset 950h

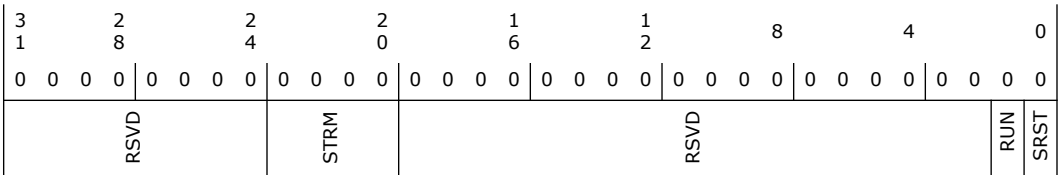
SRST bit is not affected by stream reset.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. 0000=Reserved (Indicates Unused) 0001=Stream 1 ... 1110=Stream 14 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Bit Range	Default & Access	Field Name (ID): Description
19:2	0h RO	Reserved.
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

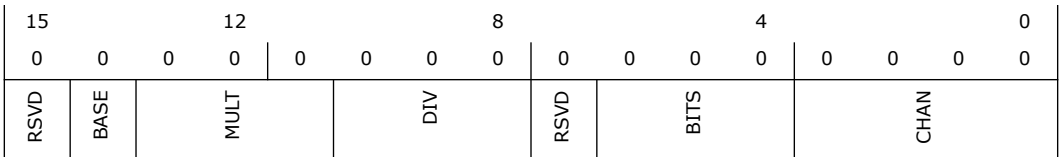
6.2.162 Input/Output Processing Pipe's Link Connection x Format (IPPLC4FMT)—Offset 954h

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	Reserved.
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	Reserved.
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

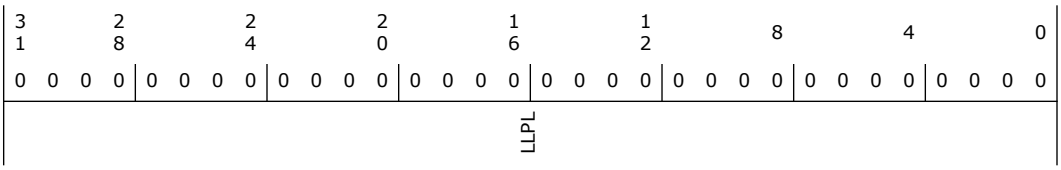
6.2.163 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC4LLPL)—Offset 958h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

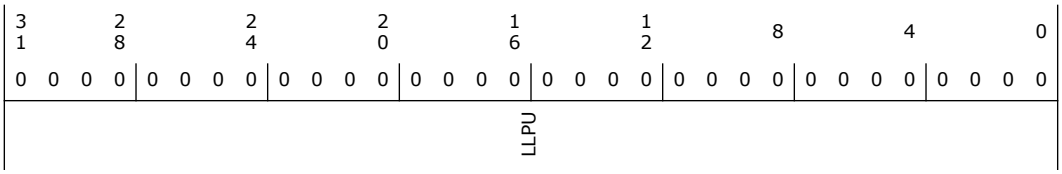
6.2.164 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC4LLPU)—Offset 95Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

6.2.165 Input/Output Processing Pipe's Link Connection x Control (IPPLC5CTL)—Offset 960h

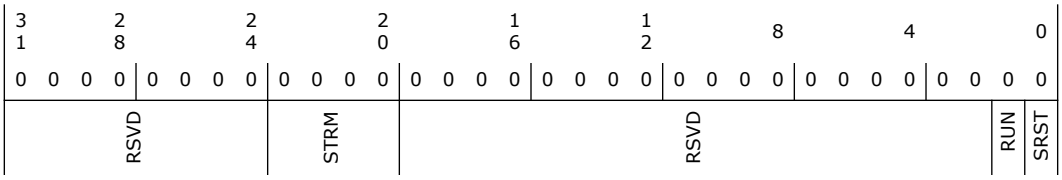
SRST bit is not affected by stream reset.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. 0000=Reserved (Indicates Unused) 0001=Stream 1 ... 1110=Stream 14 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Bit Range	Default & Access	Field Name (ID): Description
19:2	0h RO	Reserved.
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

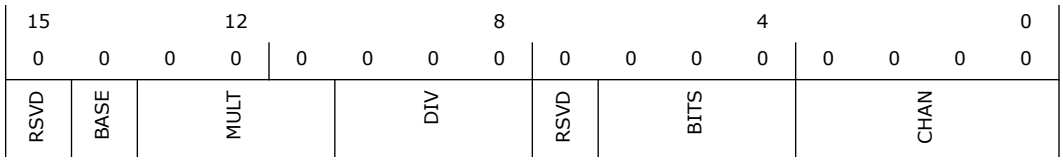
6.2.166 Input/Output Processing Pipe's Link Connection x Format (IPPLC5FMT)—Offset 964h

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	Reserved.
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	Reserved.
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

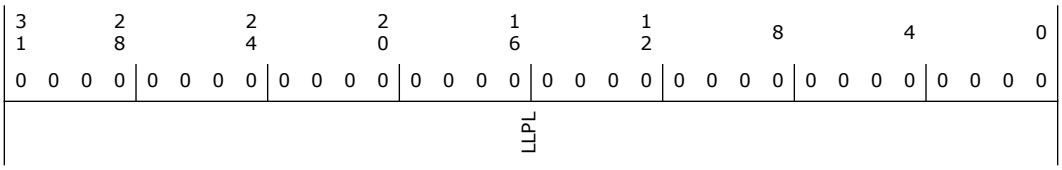
6.2.167 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC5LLPL)—Offset 968h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

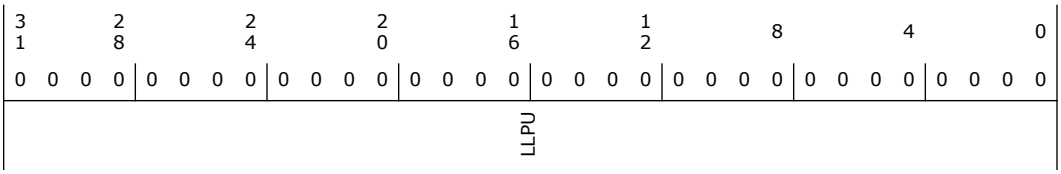
6.2.168 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC5LLPU)—Offset 96Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

6.2.169 Input/Output Processing Pipe's Link Connection x Control (IPPLC6CTL)—Offset 970h

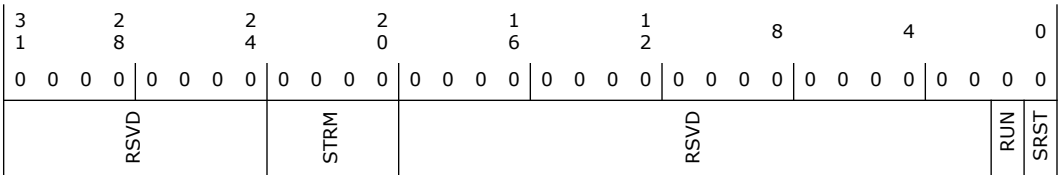
SRST bit is not affected by stream reset.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. 0000=Reserved (Indicates Unused) 0001=Stream 1 ... 1110=Stream 14 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Bit Range	Default & Access	Field Name (ID): Description
19:2	0h RO	Reserved.
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

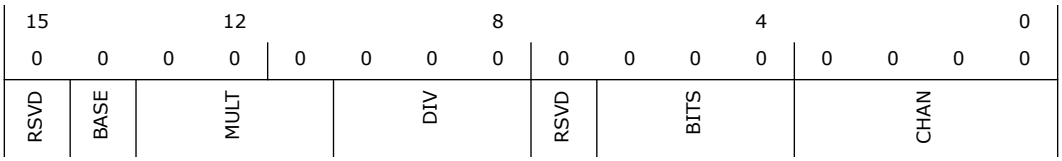
6.2.170 Input/Output Processing Pipe's Link Connection x Format (IPPLC6FMT)—Offset 974h

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	Reserved.
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	Reserved.
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

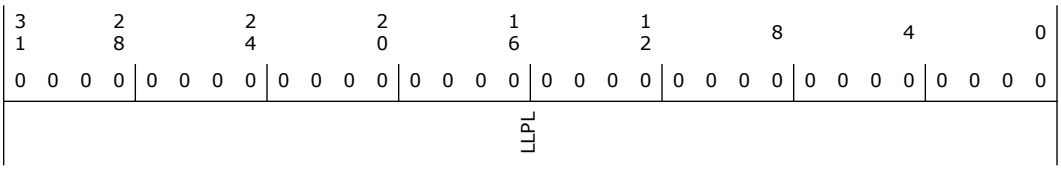
6.2.171 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC6LLPL)—Offset 978h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

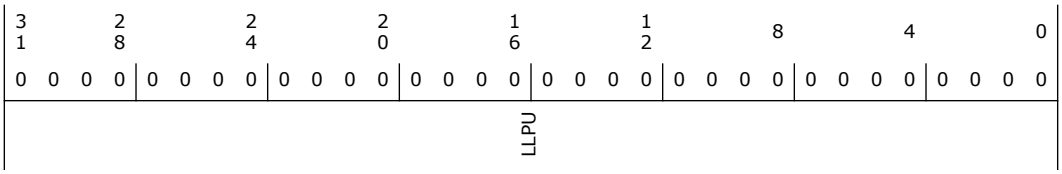
6.2.172 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC6LLPU)—Offset 97Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

6.2.173 Input/Output Processing Pipe's Link Connection x Control (OPPLC0CTL)—Offset 980h

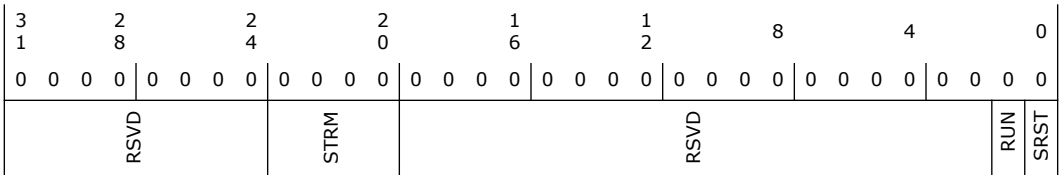
SRST bit is not affected by stream reset.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. 0000=Reserved (Indicates Unused) 0001=Stream 1 ... 1110=Stream 14 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Bit Range	Default & Access	Field Name (ID): Description
19:2	0h RO	Reserved.
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

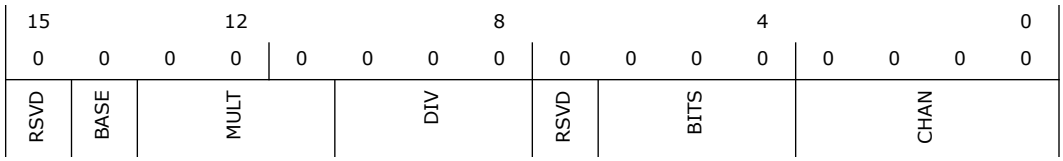
6.2.174 Input/Output Processing Pipe's Link Connection x Format (OPPLC0FMT)—Offset 984h

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	Reserved.
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	Reserved.
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

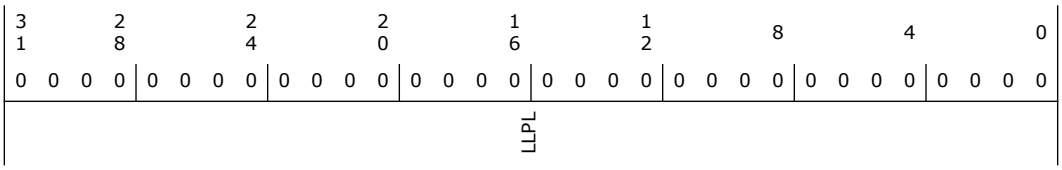
6.2.175 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC0LLPL)—Offset 988h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

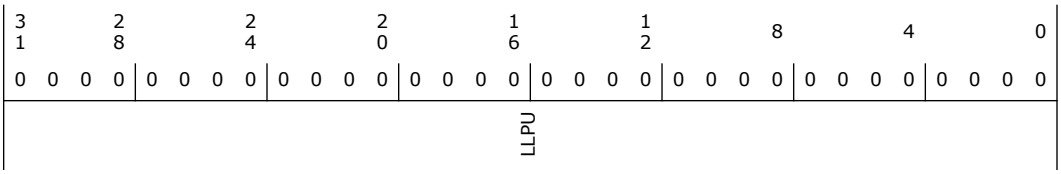
6.2.176 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC0LLPU)—Offset 98Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

6.2.177 Input/Output Processing Pipe's Link Connection x Control (OPPLC1CTL)—Offset 990h

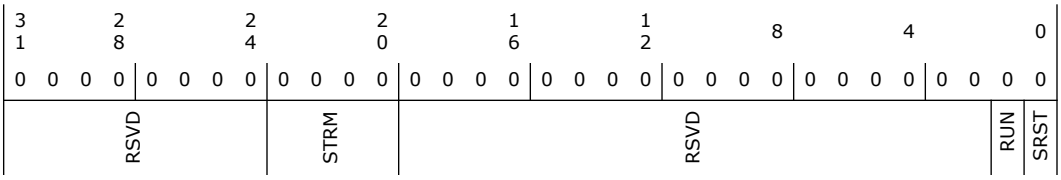
SRST bit is not affected by stream reset.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. 0000=Reserved (Indicates Unused) 0001=Stream 1 ... 1110=Stream 14 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Bit Range	Default & Access	Field Name (ID): Description
19:2	0h RO	Reserved.
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

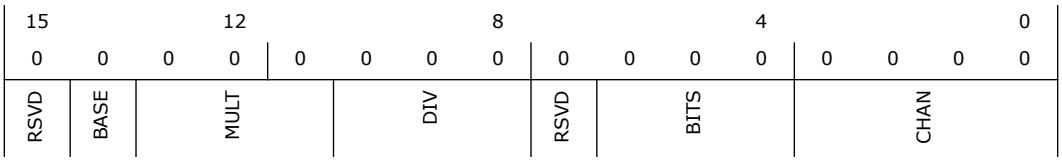
6.2.178 Input/Output Processing Pipe's Link Connection x Format (OPPLC1FMT)—Offset 994h

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	Reserved.
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	Reserved.
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

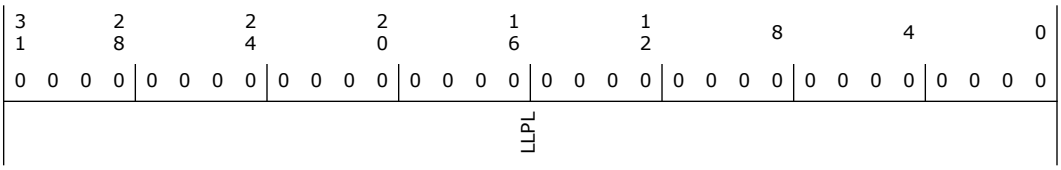
6.2.179 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC1LLPL)—Offset 998h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

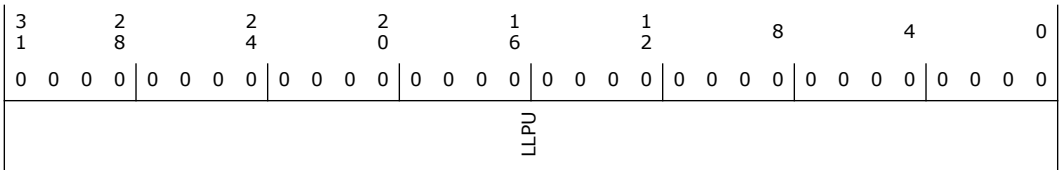
6.2.180 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC1LLPU)—Offset 99Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

6.2.181 Input/Output Processing Pipe's Link Connection x Control (OPPLC2CTL)—Offset 9A0h

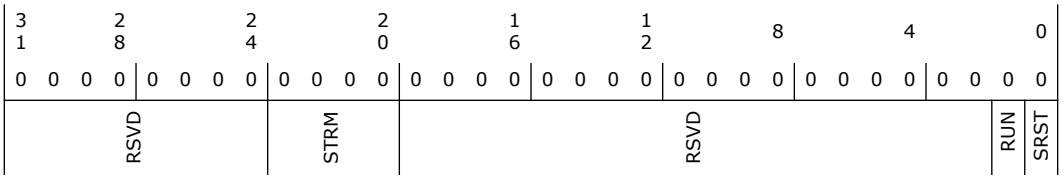
SRST bit is not affected by stream reset.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. 0000=Reserved (Indicates Unused) 0001=Stream 1 ... 1110=Stream 14 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Bit Range	Default & Access	Field Name (ID): Description
19:2	0h RO	Reserved.
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

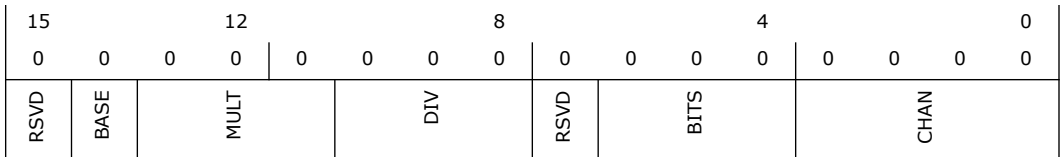
6.2.182 Input/Output Processing Pipe's Link Connection x Format (OPPLC2FMT)—Offset 9A4h

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	Reserved.
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	Reserved.
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

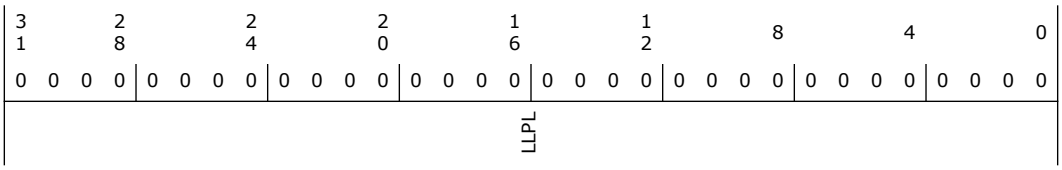
6.2.183 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC2LLPL)—Offset 9A8h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

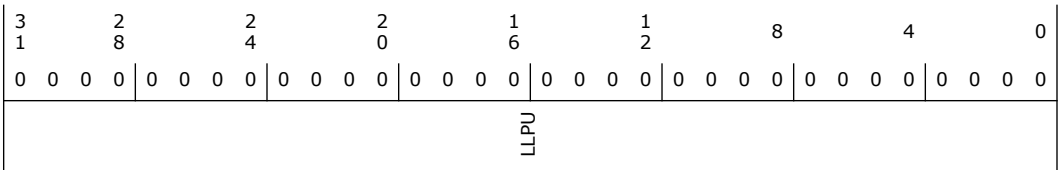
6.2.184 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC2LLPU)—Offset 9ACh

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

6.2.185 Input/Output Processing Pipe's Link Connection x Control (OPPLC3CTL)—Offset 9B0h

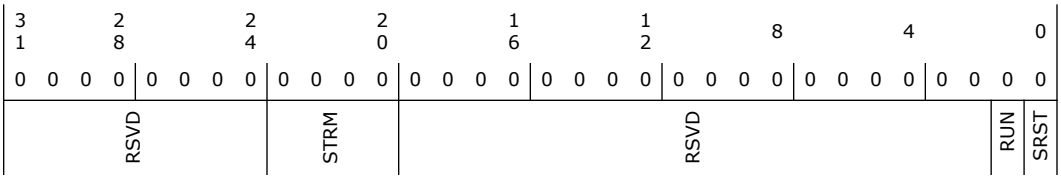
SRST bit is not affected by stream reset.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. 0000=Reserved (Indicates Unused) 0001=Stream 1 ... 1110=Stream 14 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Bit Range	Default & Access	Field Name (ID): Description
19:2	0h RO	Reserved.
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

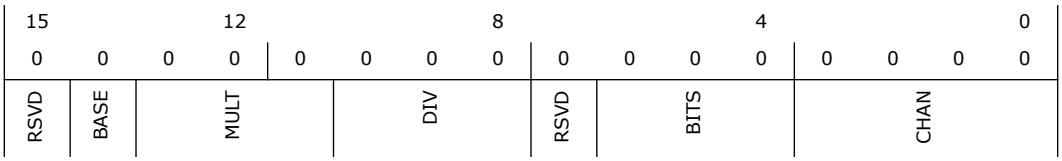
6.2.186 Input/Output Processing Pipe's Link Connection x Format (OPPLC3FMT)—Offset 9B4h

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	Reserved.
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	Reserved.
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

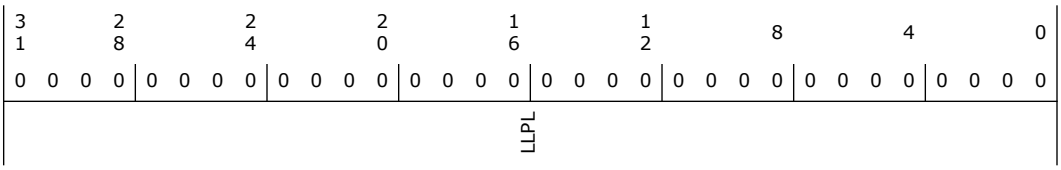
6.2.187 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC3LLPL)—Offset 9B8h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

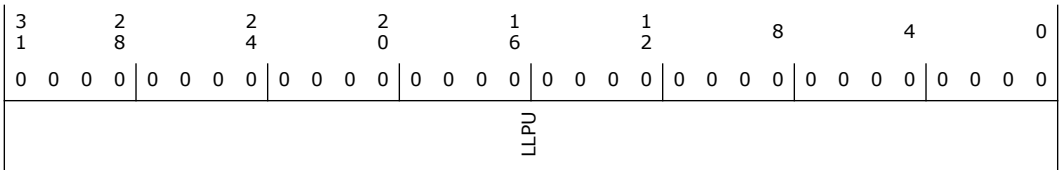
6.2.188 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC3LLPU)—Offset 9BCh

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

6.2.189 Input/Output Processing Pipe's Link Connection x Control (OPPLC4CTL)—Offset 9C0h

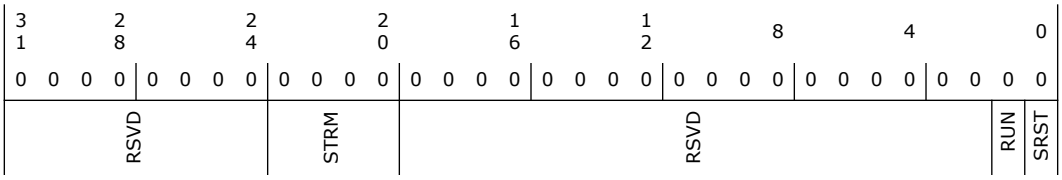
SRST bit is not affected by stream reset.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. 0000=Reserved (Indicates Unused) 0001=Stream 1 ... 1110=Stream 14 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Bit Range	Default & Access	Field Name (ID): Description
19:2	0h RO	Reserved.
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

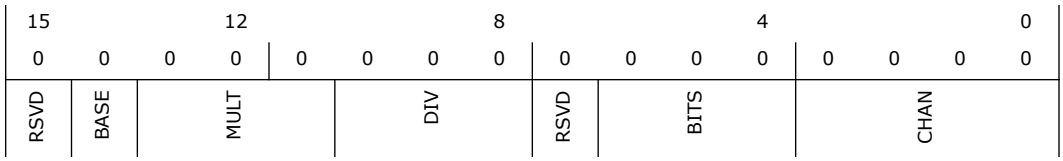
6.2.190 Input/Output Processing Pipe's Link Connection x Format (OPPLC4FMT)—Offset 9C4h

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	Reserved.
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	Reserved.
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

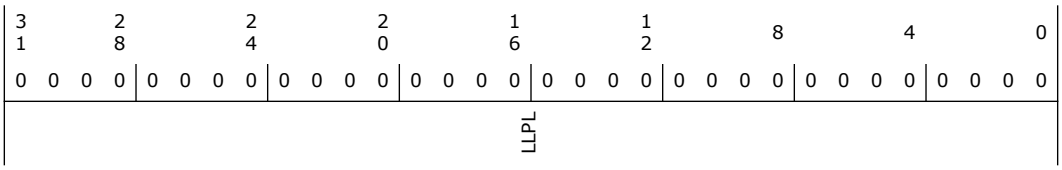
6.2.191 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC4LLPL)—Offset 9C8h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

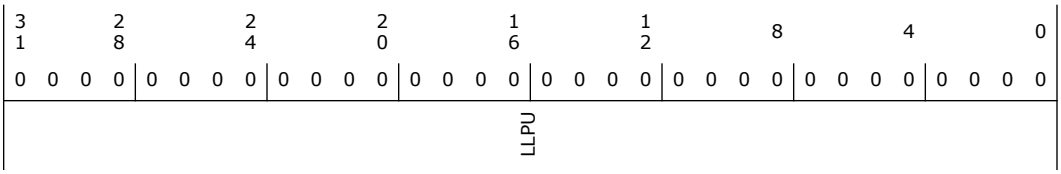
6.2.192 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC4LLPU)—Offset 9CCh

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

6.2.193 Input/Output Processing Pipe's Link Connection x Control (OPPLC5CTL)—Offset 9D0h

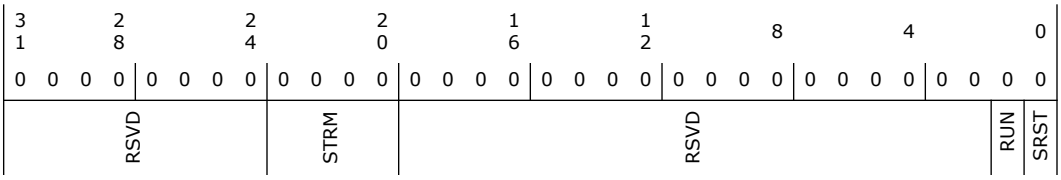
SRST bit is not affected by stream reset.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. 0000=Reserved (Indicates Unused) 0001=Stream 1 ... 1110=Stream 14 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Bit Range	Default & Access	Field Name (ID): Description
19:2	0h RO	Reserved.
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

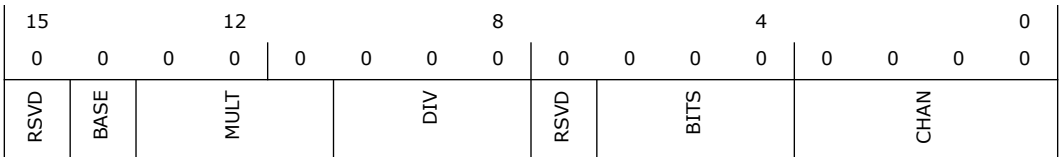
6.2.194 Input/Output Processing Pipe's Link Connection x Format (OPPLC5FMT)—Offset 9D4h

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	Reserved.
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	Reserved.
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

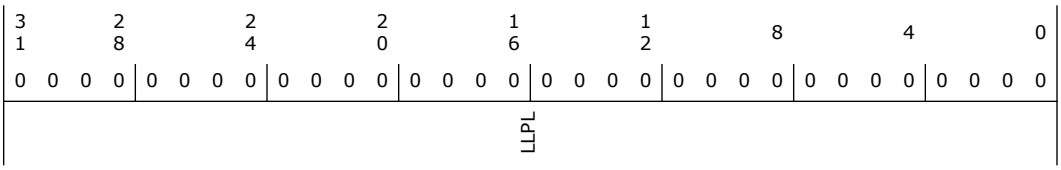
6.2.195 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC5LLPL)—Offset 9D8h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

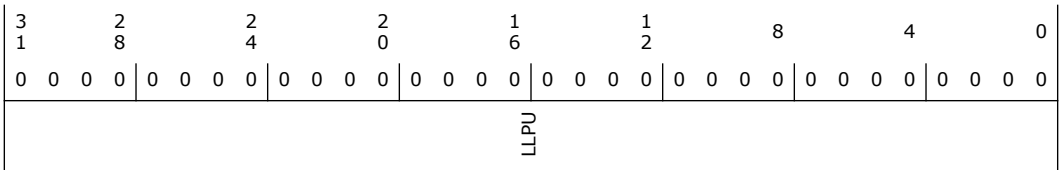
6.2.196 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC5LLPU)—Offset 9DCh

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

6.2.197 Input/Output Processing Pipe's Link Connection x Control (OPPLC6CTL)—Offset 9E0h

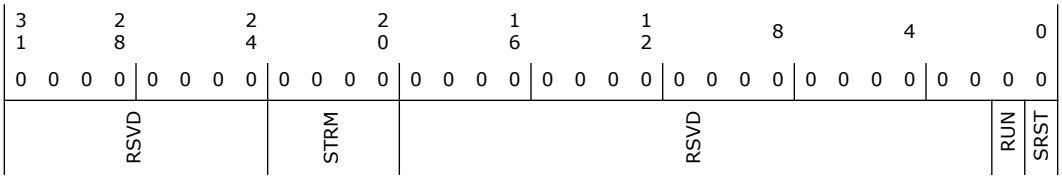
SRST bit is not affected by stream reset.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. 0000=Reserved (Indicates Unused) 0001=Stream 1 ... 1110=Stream 14 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Bit Range	Default & Access	Field Name (ID): Description
19:2	0h RO	Reserved.
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

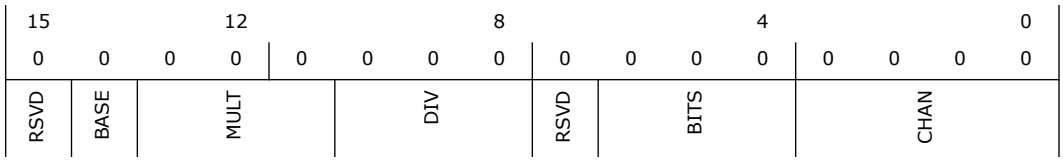
6.2.198 Input/Output Processing Pipe's Link Connection x Format (OPPLC6FMT)—Offset 9E4h

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	Reserved.
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	Reserved.
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

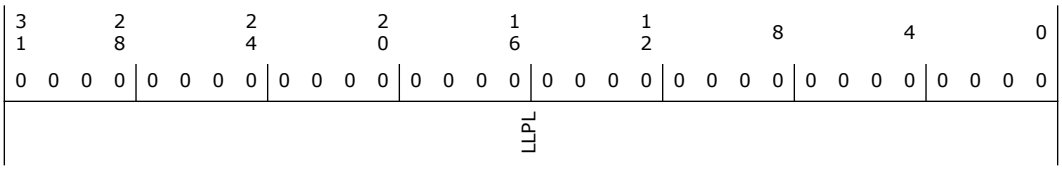
6.2.199 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC6LLPL)—Offset 9E8h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

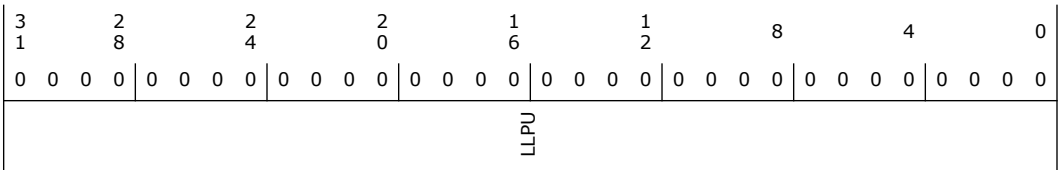
6.2.200 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC6LLPU)—Offset 9ECh

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

6.2.201 Input/Output Processing Pipe's Link Connection x Control (OPPLC7CTL)—Offset 9F0h

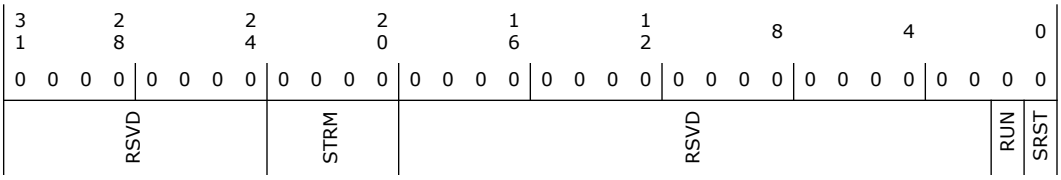
SRST bit is not affected by stream reset.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. 0000=Reserved (Indicates Unused) 0001=Stream 1 ... 1110=Stream 14 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Bit Range	Default & Access	Field Name (ID): Description
19:2	0h RO	Reserved.
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

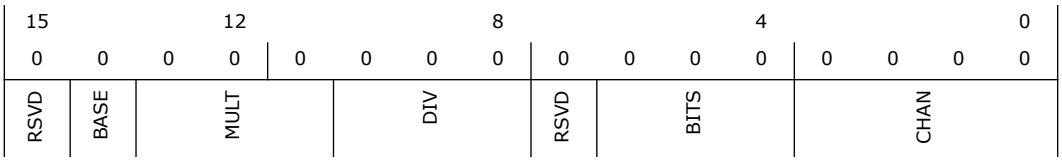
6.2.202 Input/Output Processing Pipe's Link Connection x Format (OPPLC7FMT)—Offset 9F4h

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	Reserved.
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	Reserved.
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

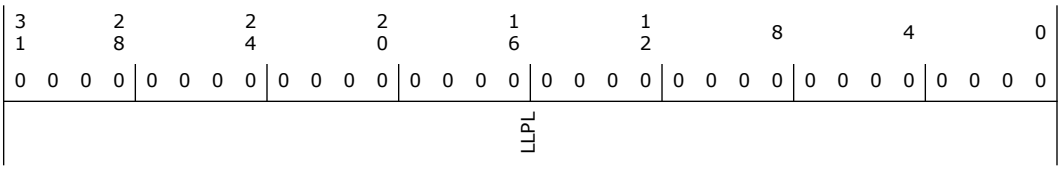
6.2.203 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC7LLPL)—Offset 9F8h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

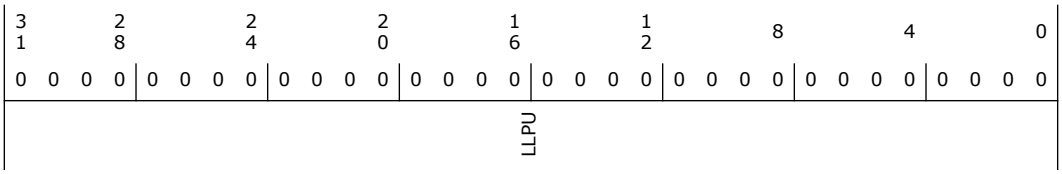
6.2.204 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC7LLPU)—Offset 9FCh

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

6.2.205 Input/Output Processing Pipe's Link Connection x Control (OPPLC8CTL)—Offset A00h

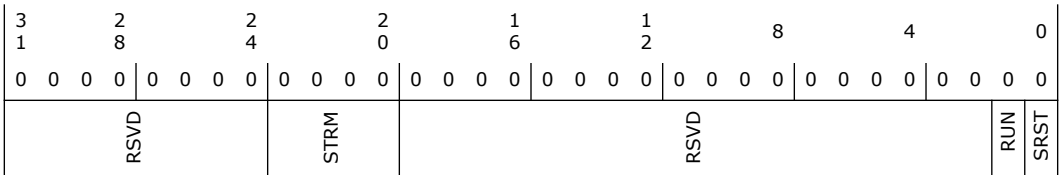
SRST bit is not affected by stream reset.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. 0000=Reserved (Indicates Unused) 0001=Stream 1 ... 1110=Stream 14 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Bit Range	Default & Access	Field Name (ID): Description
19:2	0h RO	Reserved.
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

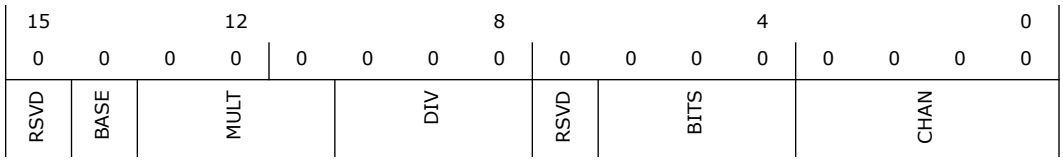
6.2.206 Input/Output Processing Pipe's Link Connection x Format (OPPLC8FMT)—Offset A04h

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	Reserved.
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	Reserved.
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

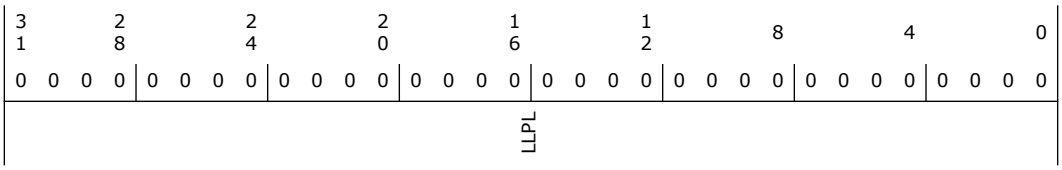
6.2.207 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC8LLPL)—Offset A08h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

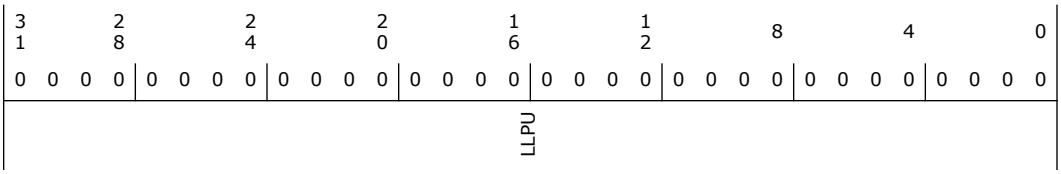
6.2.208 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC8LLPU)—Offset A0Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

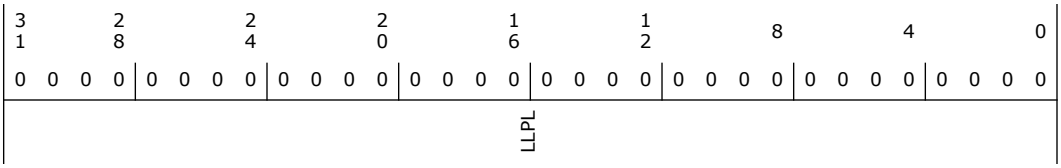
6.2.209 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC7LLPL)—Offset 4A10h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

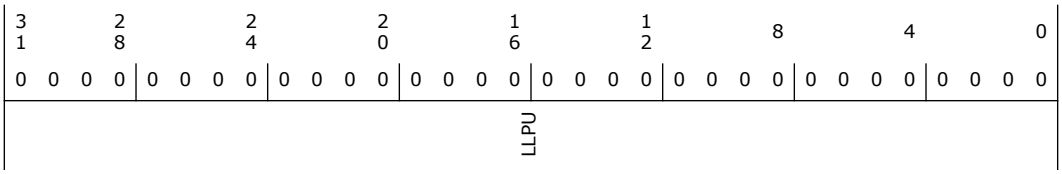
6.2.210 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC7LLPU)—Offset 4A14h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

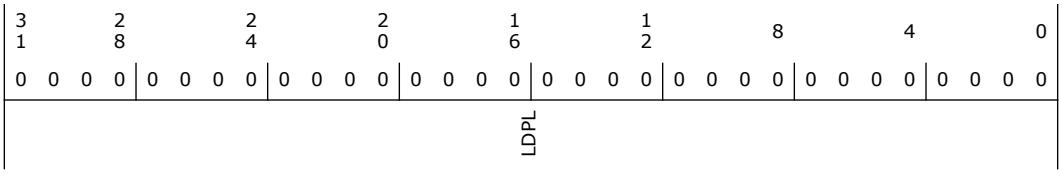
6.2.211 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC7LDPL)—Offset 4A18h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

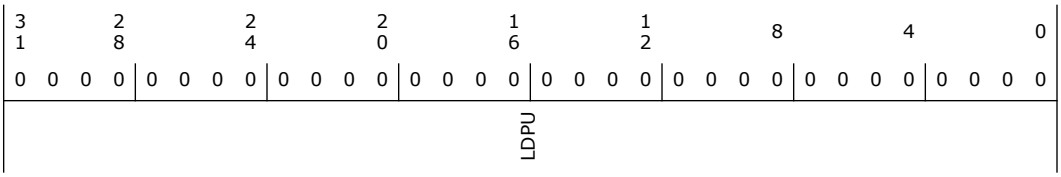
6.2.212 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC7LDPU)—Offset 4A1Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

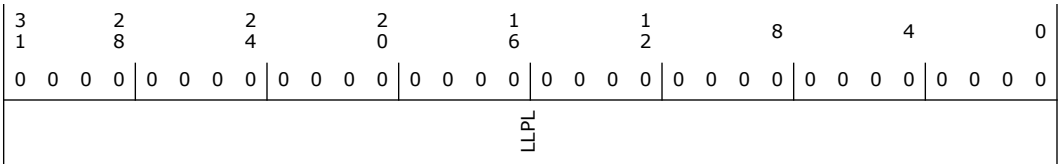
6.2.213 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC8LLPL)—Offset 4A20h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

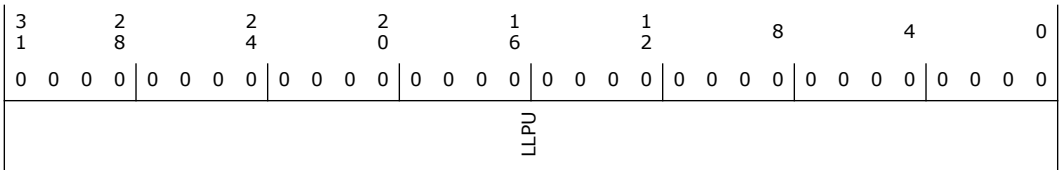
6.2.214 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC8LLPU)—Offset 4A24h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

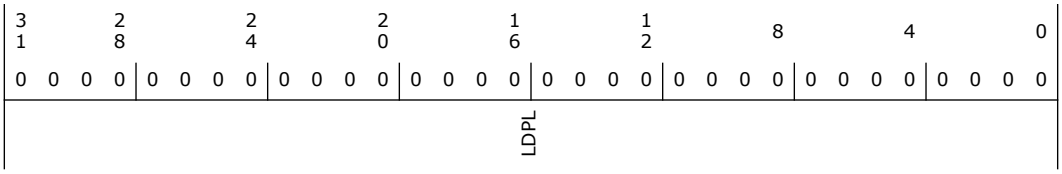
6.2.215 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC8LDPL)—Offset 4A28h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

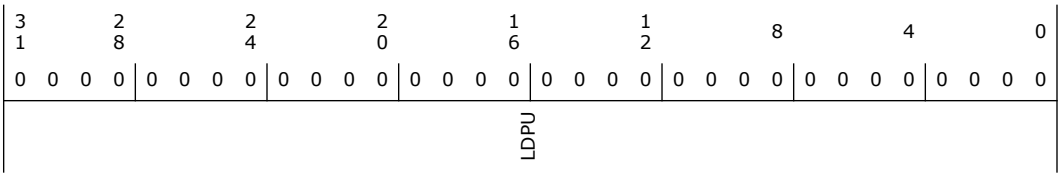
6.2.216 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC8LDPU)—Offset 4A2Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

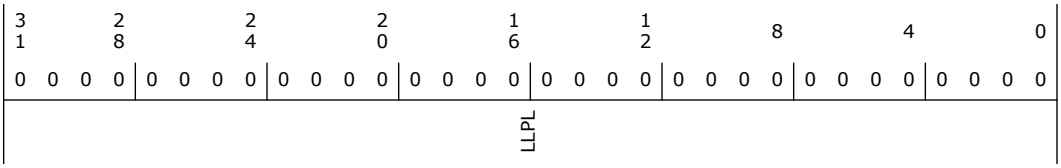
6.2.217 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC9LLPL)—Offset 4A30h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

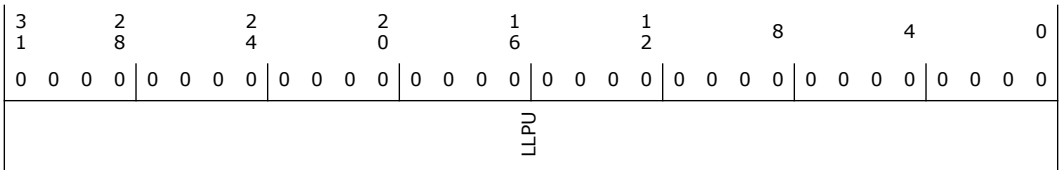
6.2.218 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC9LLPU)—Offset 4A34h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

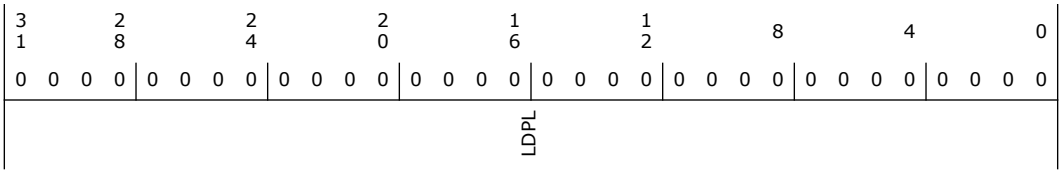
6.2.219 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC9LDPL)—Offset 4A38h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

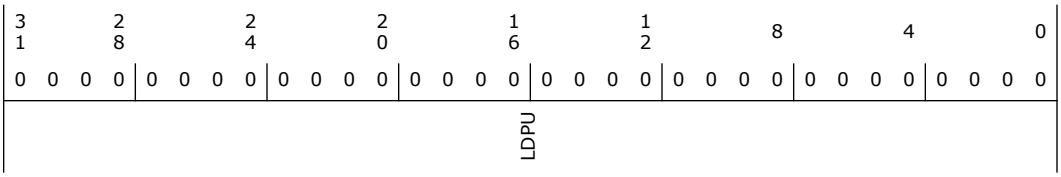
6.2.220 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC9LDPU)—Offset 4A3Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

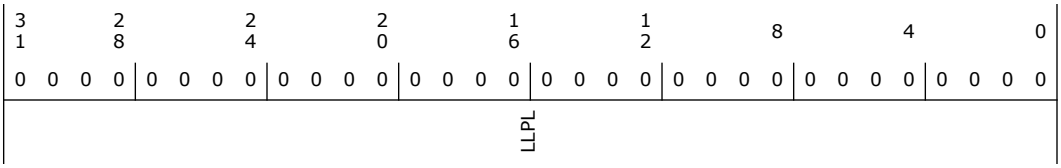
6.2.221 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC10LLPL)—Offset 4A40h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

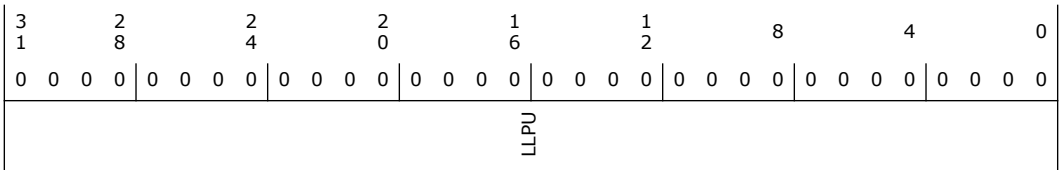
6.2.222 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC10LLPU)—Offset 4A44h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

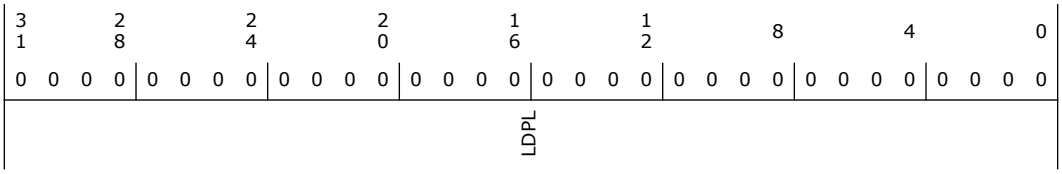
6.2.223 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC10LDPL)—Offset 4A48h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

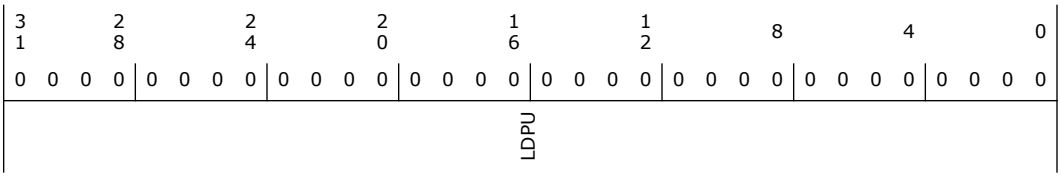
6.2.224 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC10LDPU)—Offset 4A4Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

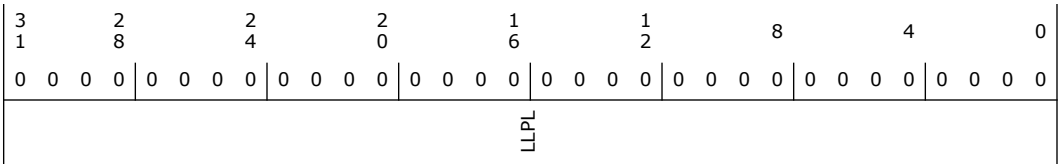
6.2.225 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC11LLPL)—Offset 4A50h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

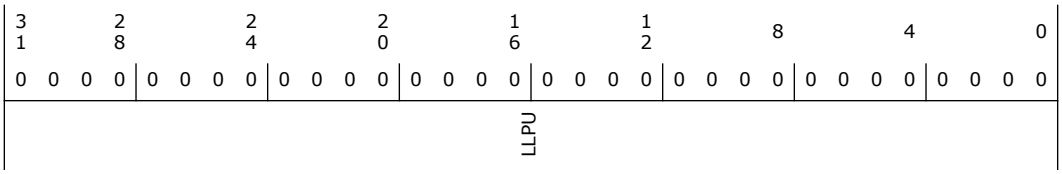
6.2.226 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC11LLPU)—Offset 4A54h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

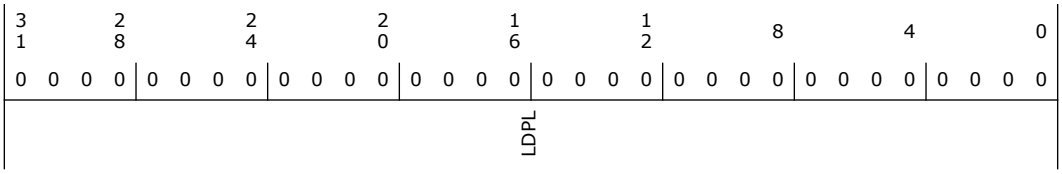
6.2.227 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC11LDPL)—Offset 4A58h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

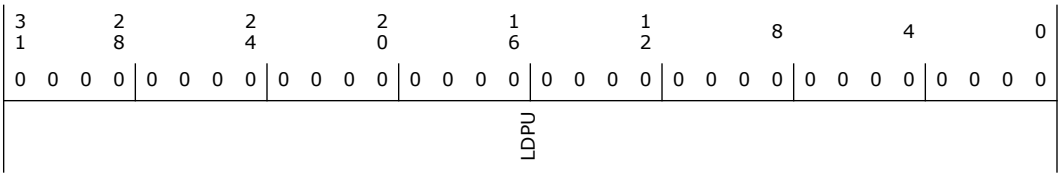
6.2.228 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC11LDPU)—Offset 4A5Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

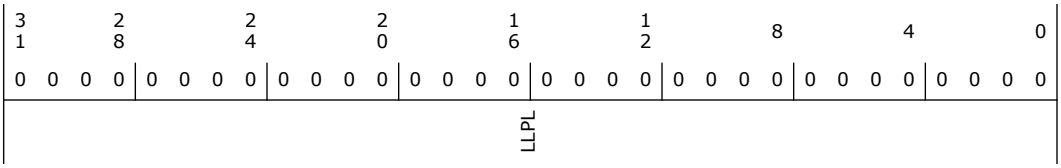
6.2.229 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC12LLPL)—Offset 4A60h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

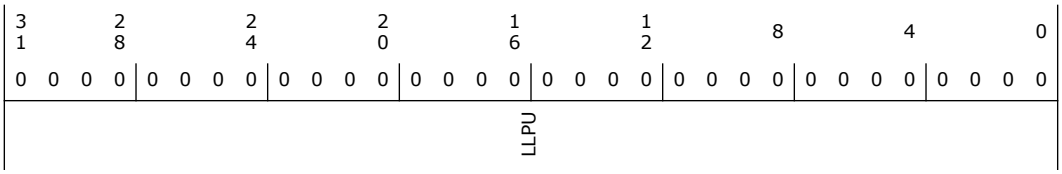
6.2.230 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC12LLPU)—Offset 4A64h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

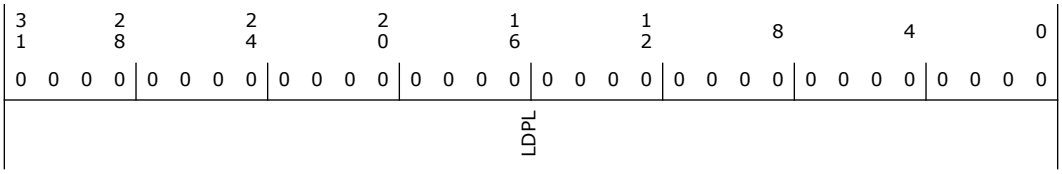
6.2.231 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC12LDPL)—Offset 4A68h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

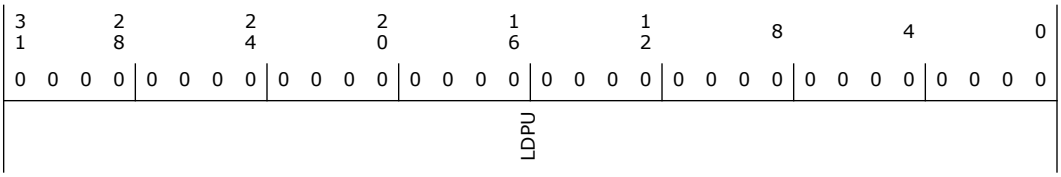
6.2.232 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC12LDPU)—Offset 4A6Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

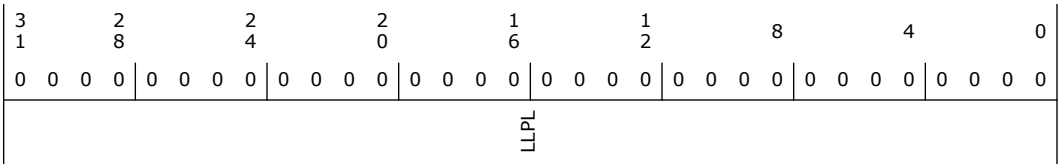
6.2.233 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC13LLPL)—Offset 4A70h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

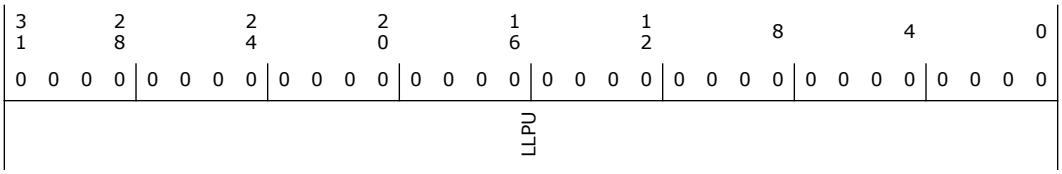
6.2.234 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC13LLPU)—Offset 4A74h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

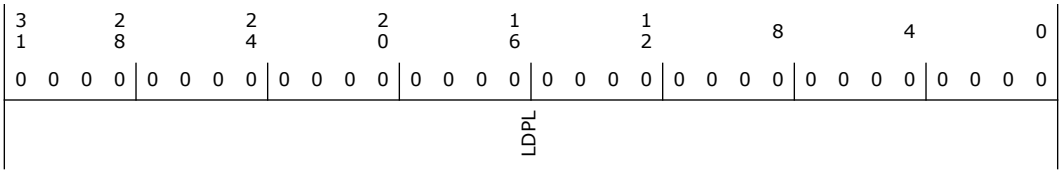
6.2.235 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC13LDPL)—Offset 4A78h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

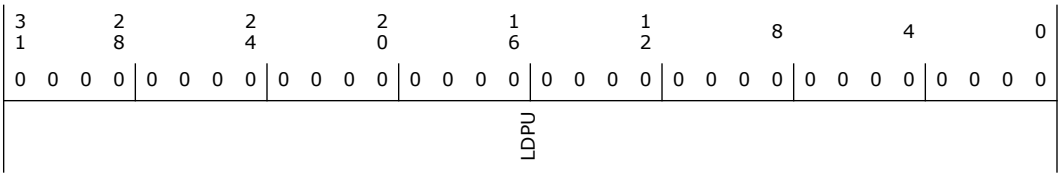
6.2.236 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC13LDPU)—Offset 4A7Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

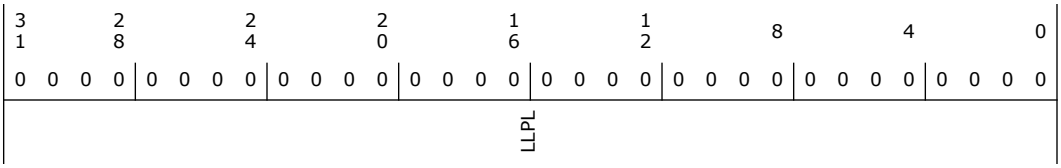
6.2.237 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC14LLPL)—Offset 4A80h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

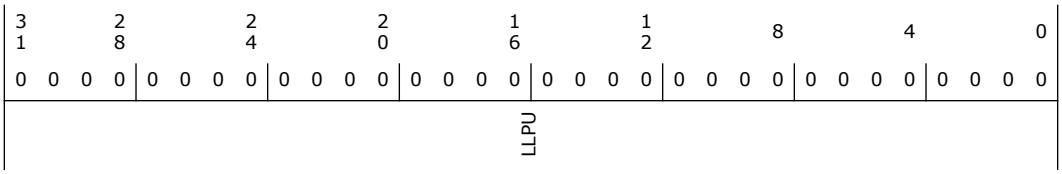
6.2.238 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC14LLPU)—Offset 4A84h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

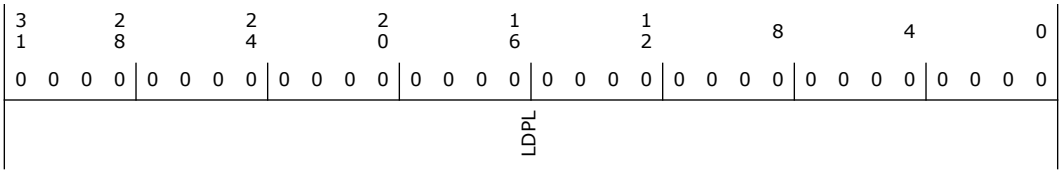
6.2.239 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC14LDPL)—Offset 4A88h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

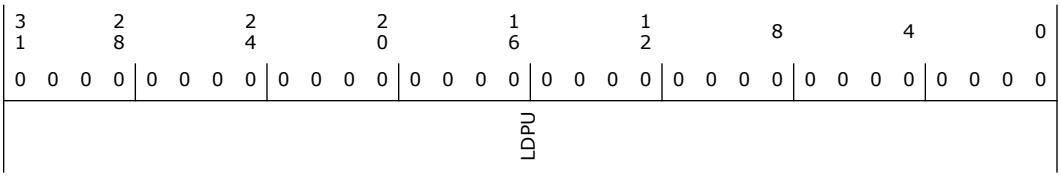
6.2.240 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC14LDPU)—Offset 4A8Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

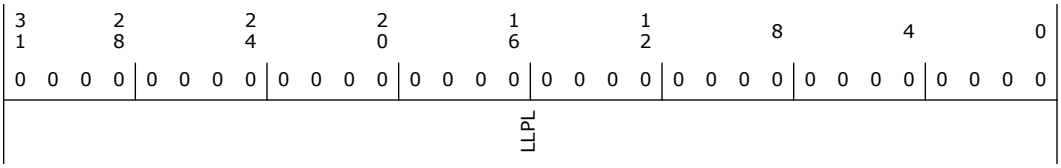
6.2.241 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC9LLPL)—Offset 4A90h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

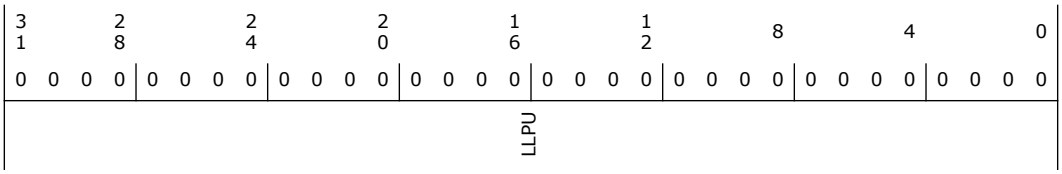
6.2.242 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC9LLPU)—Offset 4A94h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

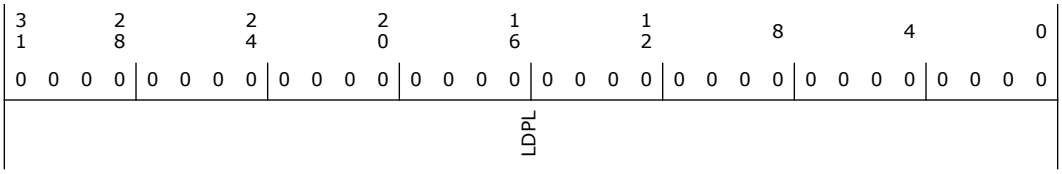
6.2.243 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC9LDPL)—Offset 4A98h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

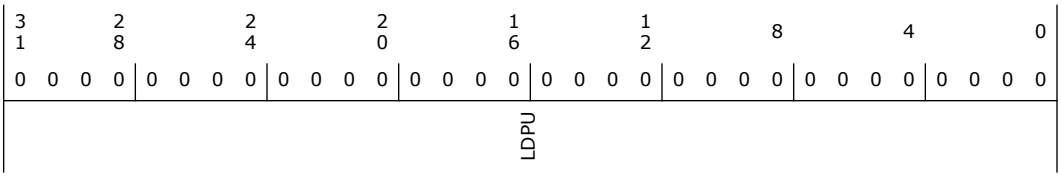
6.2.244 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC9LDPU)—Offset 4A9Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

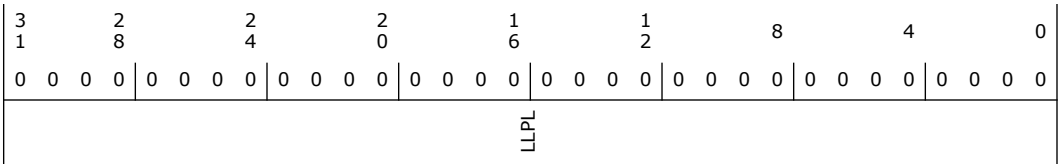
6.2.245 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC10LLPL)—Offset 4AA0h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

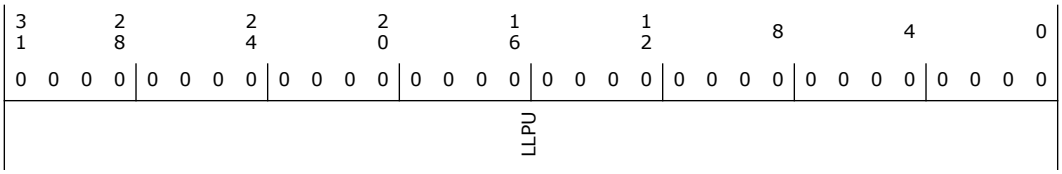
6.2.246 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC10LLPU)—Offset 4AA4h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

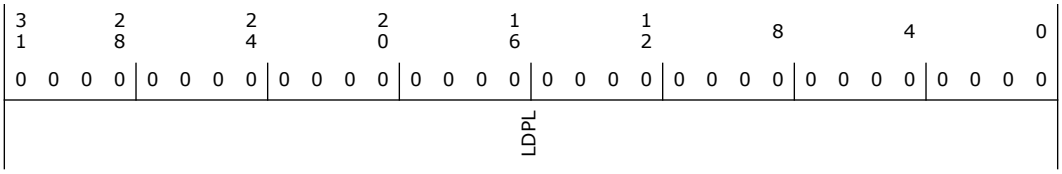
6.2.247 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC10LDPL)—Offset 4AA8h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

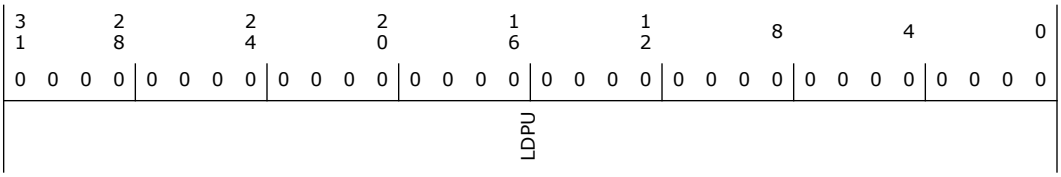
6.2.248 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC10LDPU)—Offset 4AACh

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

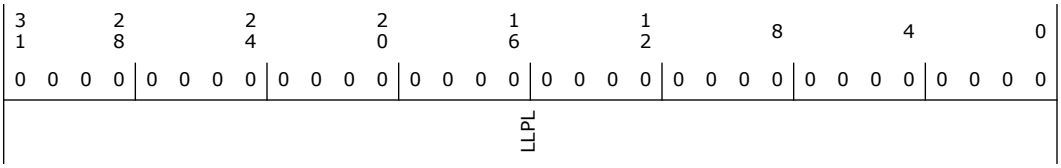
6.2.249 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC11LLPL)—Offset 4AB0h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

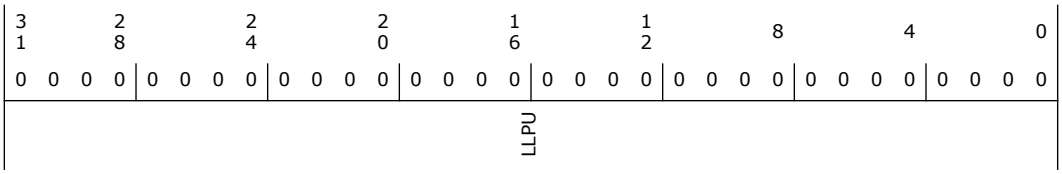
6.2.250 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC11LLPU)—Offset 4AB4h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

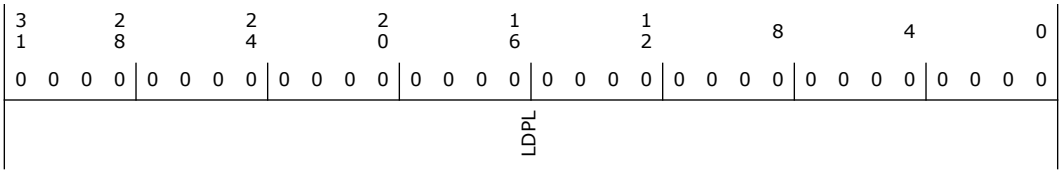
6.2.251 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC11LDPL)—Offset 4AB8h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

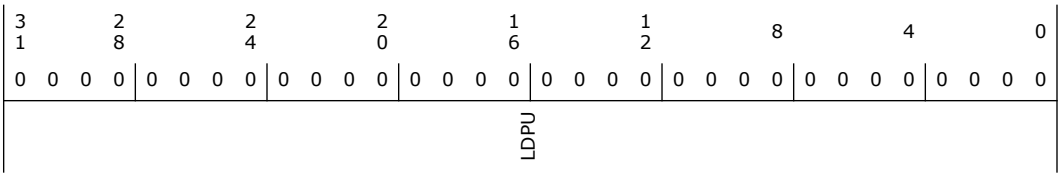
6.2.252 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC11LDPU)—Offset 4ABCh

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

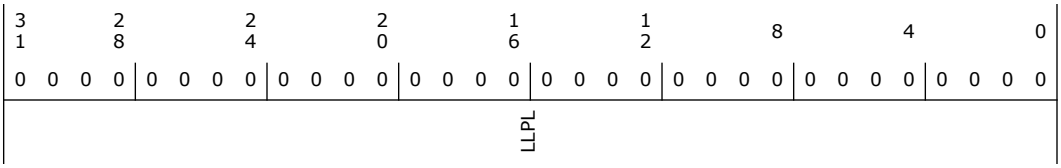
6.2.253 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC12LLPL)—Offset 4AC0h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

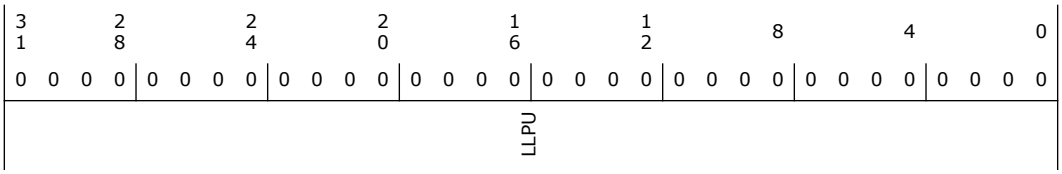
6.2.254 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC12LLPU)—Offset 4AC4h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

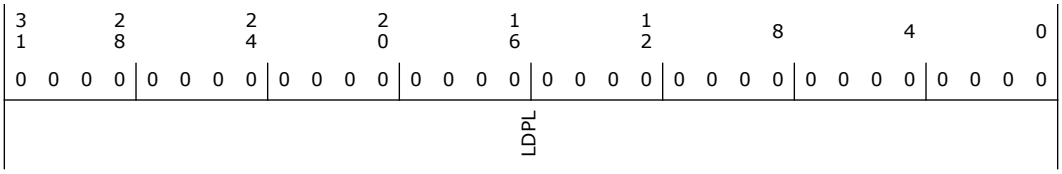
6.2.255 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC12LDPL)—Offset 4AC8h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

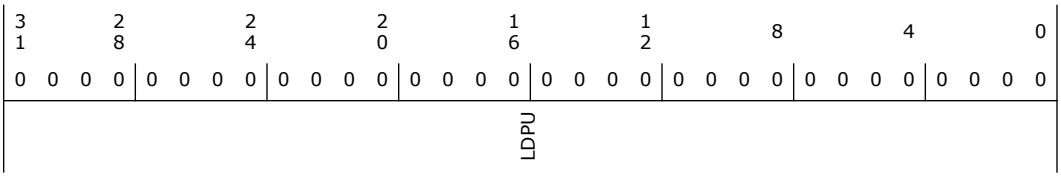
6.2.256 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC12LDPU)—Offset 4ACCh

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

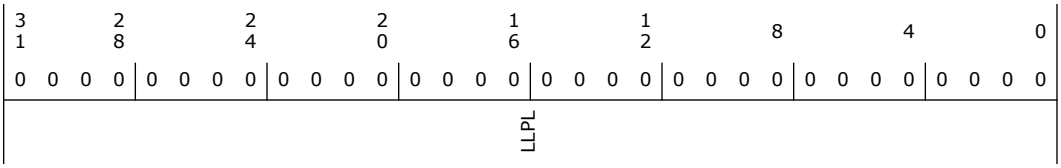
6.2.257 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC13LLPL)—Offset 4AD0h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

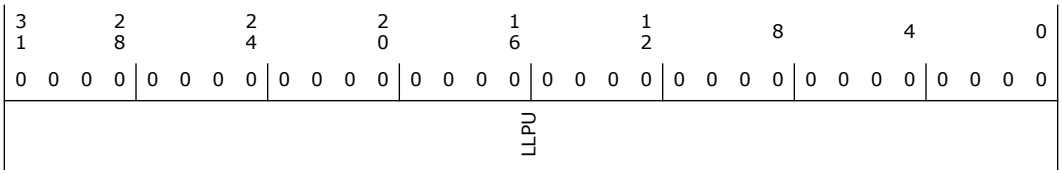
6.2.258 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC13LLPU)—Offset 4AD4h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

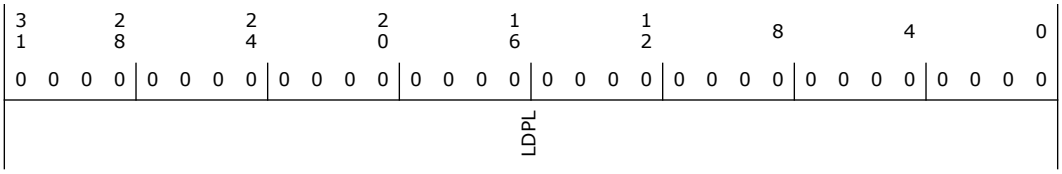
6.2.259 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC13LDPL)—Offset 4AD8h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

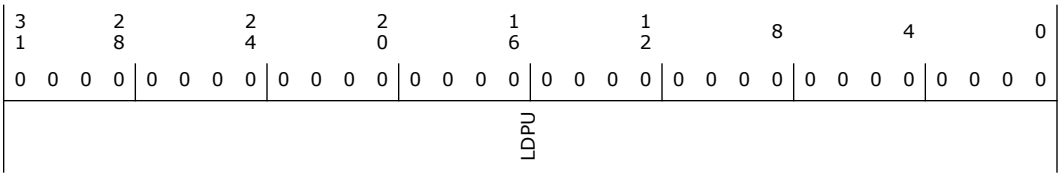
6.2.260 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC13LDPU)—Offset 4ADCh

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

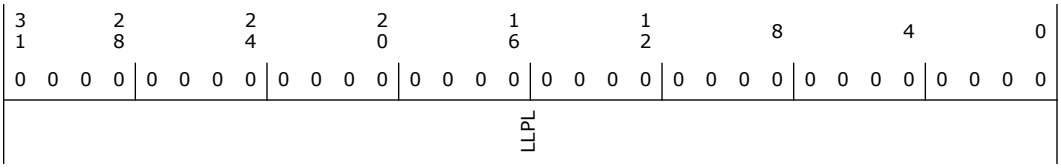
6.2.261 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC14LLPL)—Offset 4AE0h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

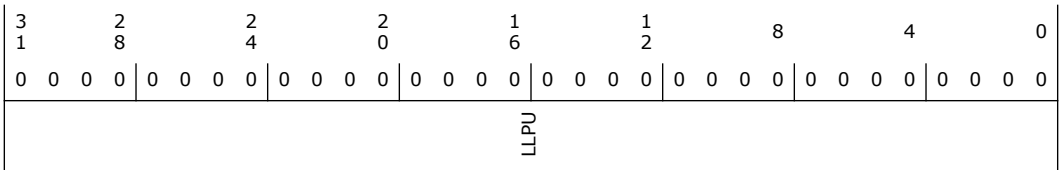
6.2.262 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC14LLPU)—Offset 4AE4h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

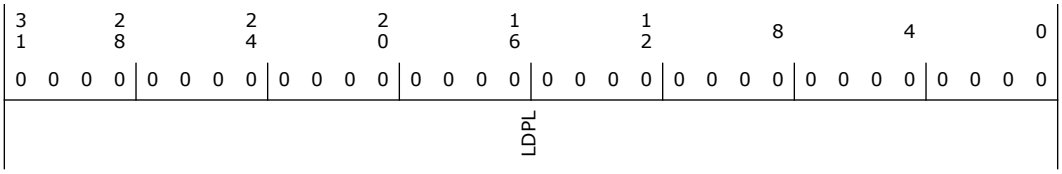
6.2.263 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC14LDPL)—Offset 4AE8h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

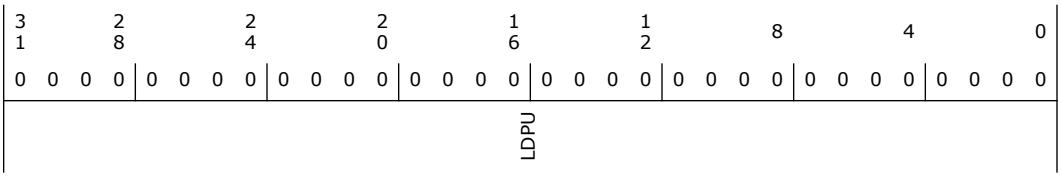
6.2.264 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC14LDPU)—Offset 4AECh

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

6.2.265 Input/Output Processing Pipe's Link Connection x Control (IPPLC7CTL)—Offset 4AF0h

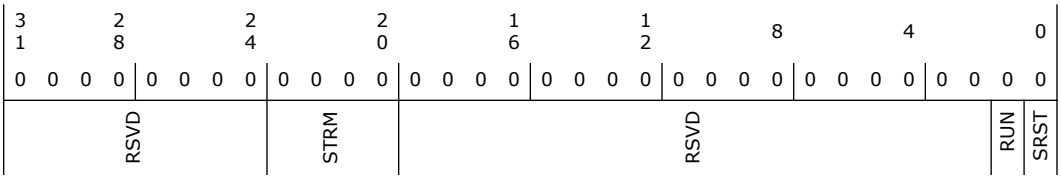
SRST bit is not affected by stream reset.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. 0000=Reserved (Indicates Unused) 0001=Stream 1 ... 1110=Stream 14 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Bit Range	Default & Access	Field Name (ID): Description
19:2	0h RO	Reserved.
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

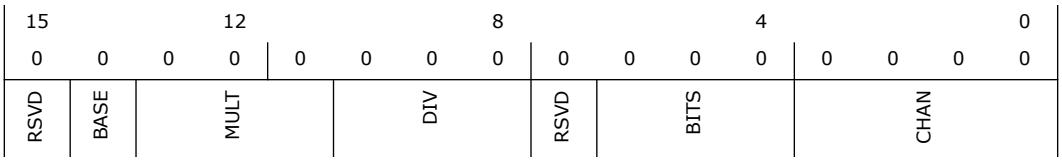
6.2.266 Input/Output Processing Pipe's Link Connection x Format (IPPLC7FMT)—Offset 4AF4h

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	Reserved.
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	Reserved.
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

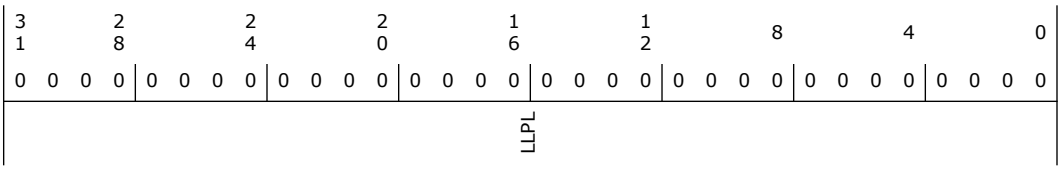
6.2.267 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC7LLPL)—Offset 4AF8h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

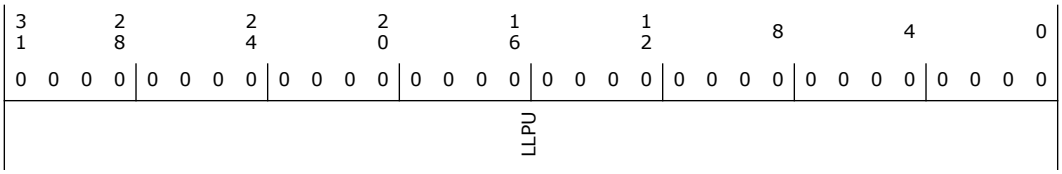
6.2.268 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC7LLPU)—Offset 4AFCh

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

6.2.269 Input/Output Processing Pipe's Link Connection x Control (IPPLC8CTL)—Offset 4B00h

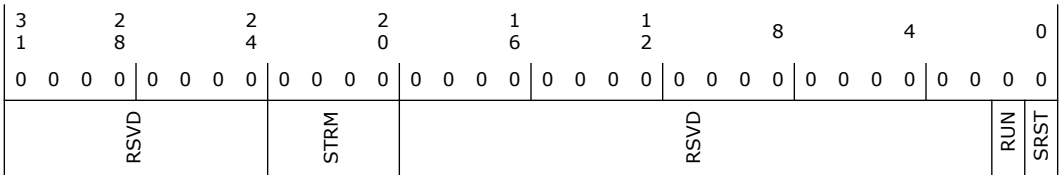
SRST bit is not affected by stream reset.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. 0000=Reserved (Indicates Unused) 0001=Stream 1 ... 1110=Stream 14 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Bit Range	Default & Access	Field Name (ID): Description
19:2	0h RO	Reserved.
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

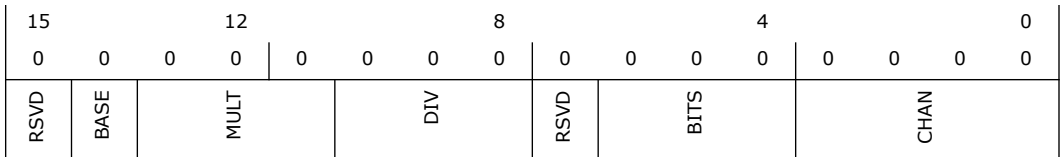
6.2.270 Input/Output Processing Pipe's Link Connection x Format (IPPLC8FMT)—Offset 4B04h

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	Reserved.
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	Reserved.
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

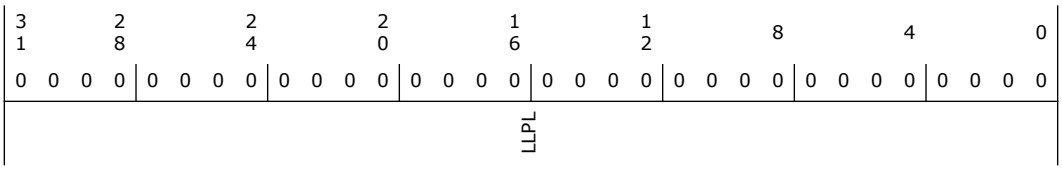
6.2.271 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC8LLPL)—Offset 4B08h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

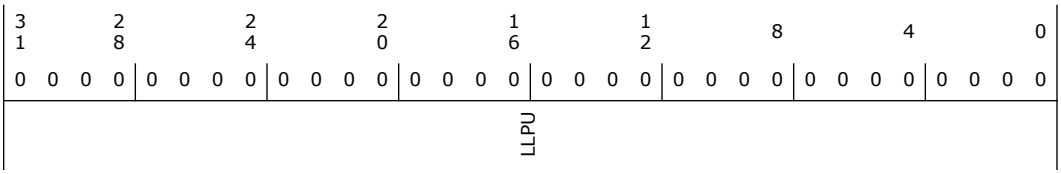
6.2.272 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC8LLPU)—Offset 4B0Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

6.2.273 Input/Output Processing Pipe's Link Connection x Control (IPPLC9CTL)—Offset 4B10h

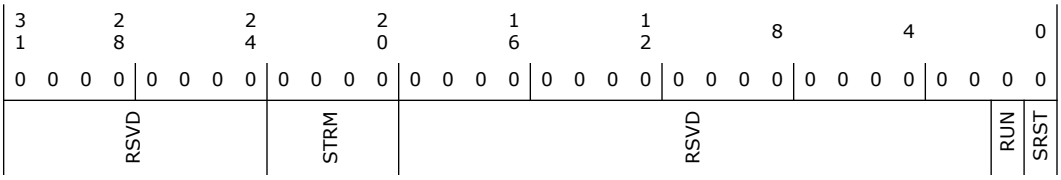
SRST bit is not affected by stream reset.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. 0000=Reserved (Indicates Unused) 0001=Stream 1 ... 1110=Stream 14 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Bit Range	Default & Access	Field Name (ID): Description
19:2	0h RO	Reserved.
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

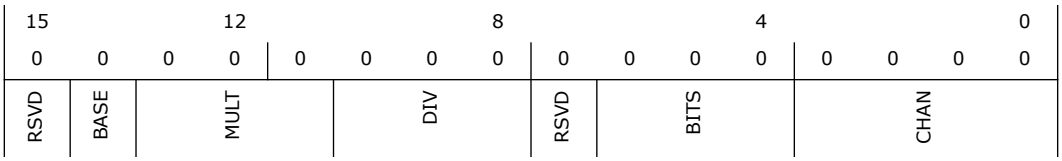
6.2.274 Input/Output Processing Pipe's Link Connection x Format (IPPLC9FMT)—Offset 4B14h

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	Reserved.
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	Reserved.
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

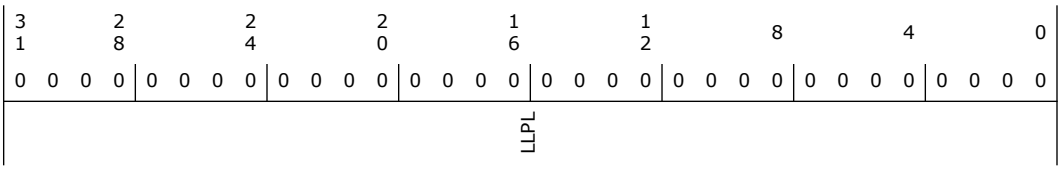
6.2.275 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC9LLPL)—Offset 4B18h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

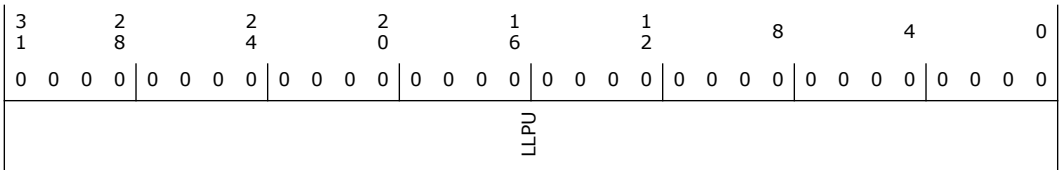
6.2.276 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC9LLPU)—Offset 4B1Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

6.2.277 Input/Output Processing Pipe's Link Connection x Control (IPPLC10CTL)—Offset 4B20h

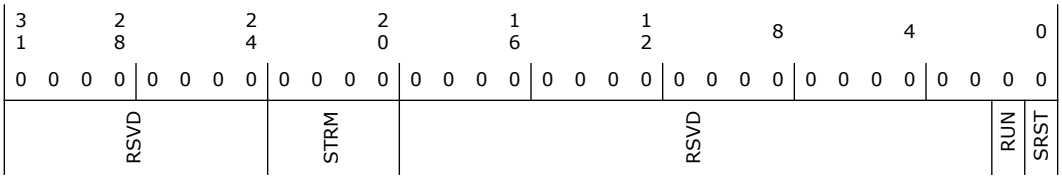
SRST bit is not affected by stream reset.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. 0000=Reserved (Indicates Unused) 0001=Stream 1 ... 1110=Stream 14 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Bit Range	Default & Access	Field Name (ID): Description
19:2	0h RO	Reserved.
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

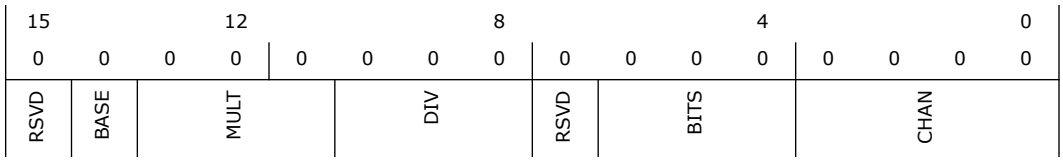
6.2.278 Input/Output Processing Pipe's Link Connection x Format (IPPLC10FMT)—Offset 4B24h

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	Reserved.
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)

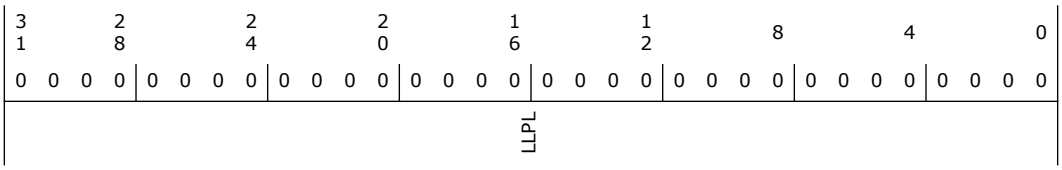
Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	Reserved.
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

6.2.279 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC10LLPL)—Offset 4B28h

Access Method

Type: MEM Register (Size: 32 bits)
Device: 31
Function: 3

Default: 0h



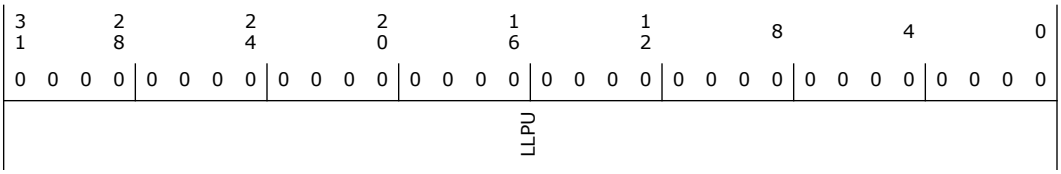
Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

6.2.280 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC10LLPU)—Offset 4B2Ch

Access Method

Type: MEM Register (Size: 32 bits)
Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

6.2.281 Input/Output Processing Pipe's Link Connection x Control (IPPLC11CTL)—Offset 4B30h

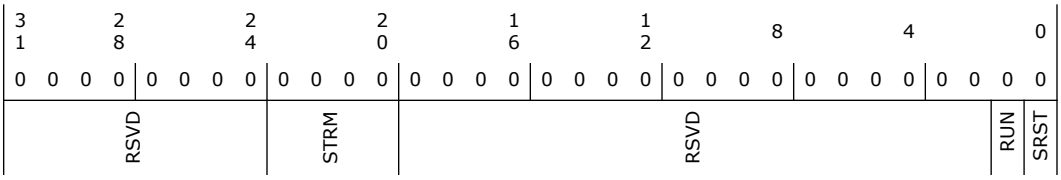
SRST bit is not affected by stream reset.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. 0000=Reserved (Indicates Unused) 0001=Stream 1 ... 1110=Stream 14 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Bit Range	Default & Access	Field Name (ID): Description
19:2	0h RO	Reserved.
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

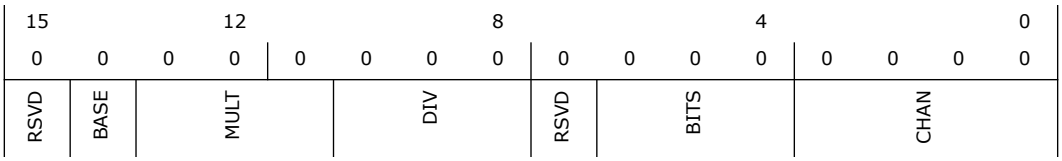
6.2.282 Input/Output Processing Pipe's Link Connection x Format (IPPLC11FMT)—Offset 4B34h

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	Reserved.
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	Reserved.
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

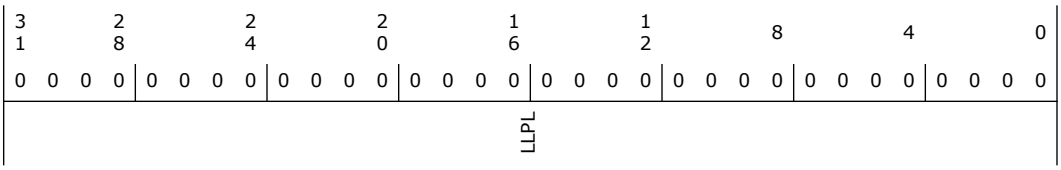
6.2.283 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC11LLPL)—Offset 4B38h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

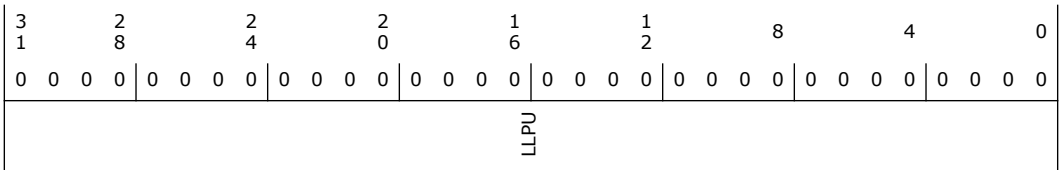
6.2.284 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC11LLPU)—Offset 4B3Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

6.2.285 Input/Output Processing Pipe's Link Connection x Control (IPPLC12CTL)—Offset 4B40h

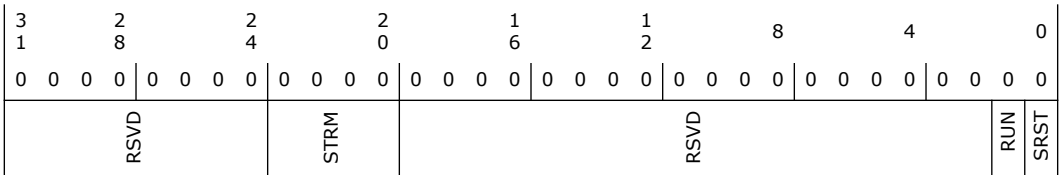
SRST bit is not affected by stream reset.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. 0000=Reserved (Indicates Unused) 0001=Stream 1 ... 1110=Stream 14 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Bit Range	Default & Access	Field Name (ID): Description
19:2	0h RO	Reserved.
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

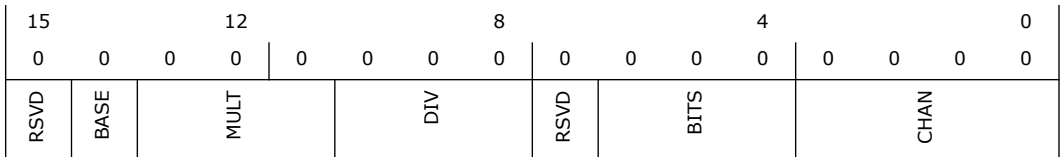
6.2.286 Input/Output Processing Pipe's Link Connection x Format (IPPLC12FMT)—Offset 4B44h

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	Reserved.
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	Reserved.
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

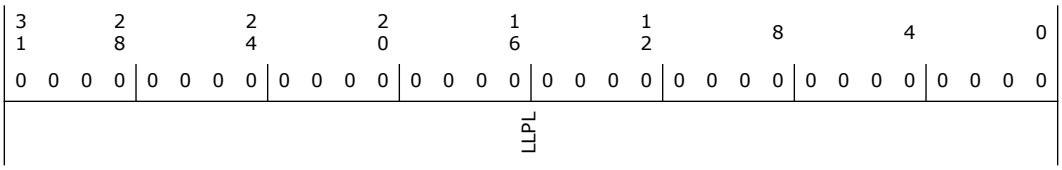
6.2.287 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC12LLPL)—Offset 4B48h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

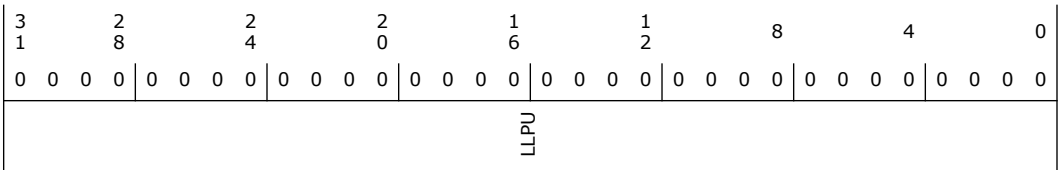
6.2.288 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC12LLPU)—Offset 4B4Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

6.2.289 Input/Output Processing Pipe's Link Connection x Control (IPPLC13CTL)—Offset 4B50h

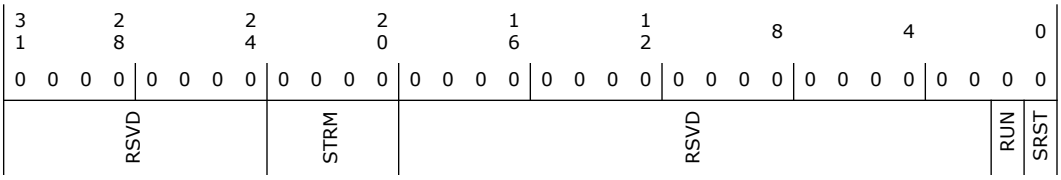
SRST bit is not affected by stream reset.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. 0000=Reserved (Indicates Unused) 0001=Stream 1 ... 1110=Stream 14 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Bit Range	Default & Access	Field Name (ID): Description
19:2	0h RO	Reserved.
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

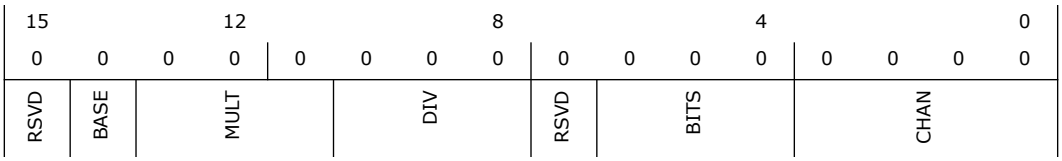
6.2.290 Input/Output Processing Pipe's Link Connection x Format (IPPLC13FMT)—Offset 4B54h

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	Reserved.
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	Reserved.
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

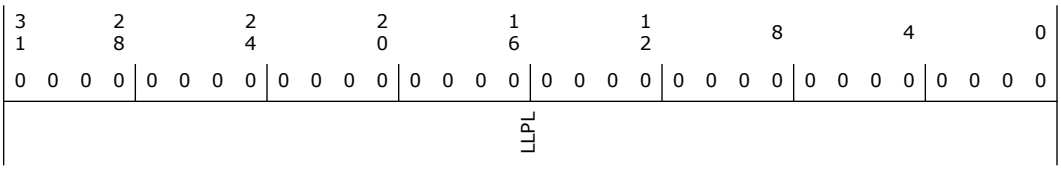
6.2.291 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC13LLPL)—Offset 4B58h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

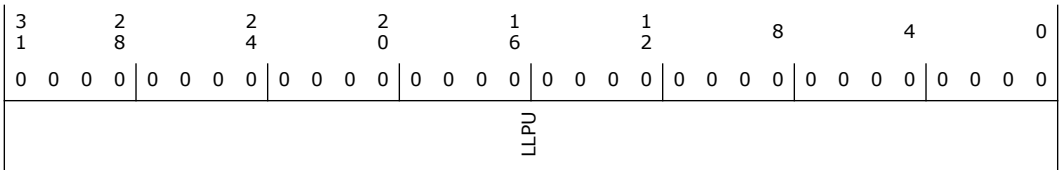
6.2.292 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC13LLPU)—Offset 4B5Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

6.2.293 Input/Output Processing Pipe's Link Connection x Control (IPPLC14CTL)—Offset 4B60h

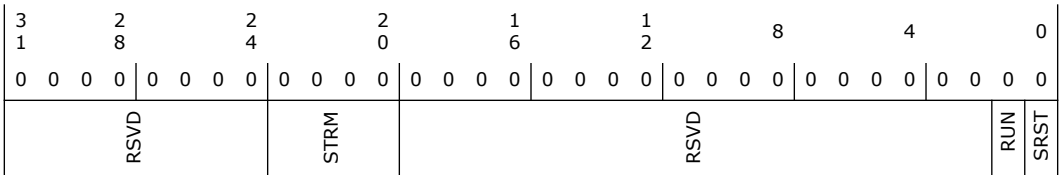
SRST bit is not affected by stream reset.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. 0000=Reserved (Indicates Unused) 0001=Stream 1 ... 1110=Stream 14 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Bit Range	Default & Access	Field Name (ID): Description
19:2	0h RO	Reserved.
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

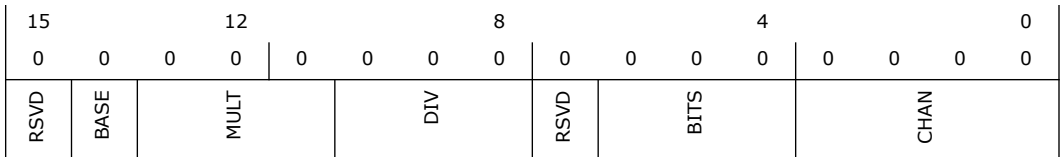
6.2.294 Input/Output Processing Pipe's Link Connection x Format (IPPLC14FMT)—Offset 4B64h

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	Reserved.
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	Reserved.
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

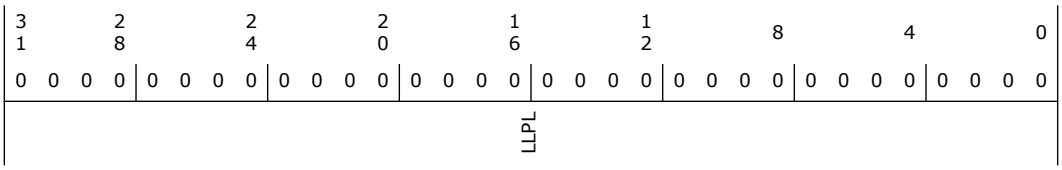
6.2.295 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC14LLPL)—Offset 4B68h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

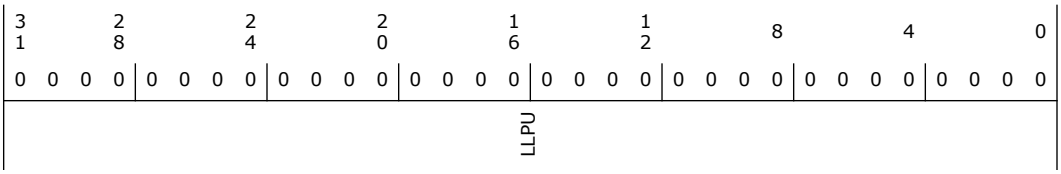
6.2.296 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC14LLPU)—Offset 4B6Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

6.2.297 Input/Output Processing Pipe's Link Connection x Control (OPPLC9CTL)—Offset 4B70h

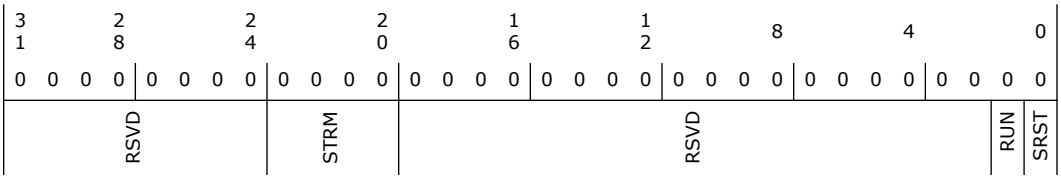
SRST bit is not affected by stream reset.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. 0000=Reserved (Indicates Unused) 0001=Stream 1 ... 1110=Stream 14 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Bit Range	Default & Access	Field Name (ID): Description
19:2	0h RO	Reserved.
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

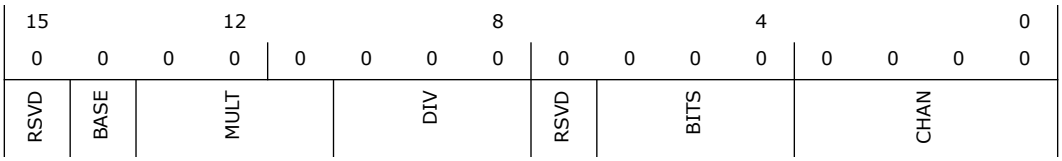
6.2.298 Input/Output Processing Pipe's Link Connection x Format (OPPLC9FMT)—Offset 4B74h

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	Reserved.
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	Reserved.
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

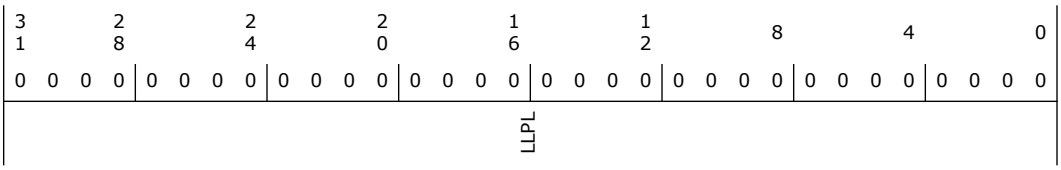
6.2.299 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC9LLPL)—Offset 4B78h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

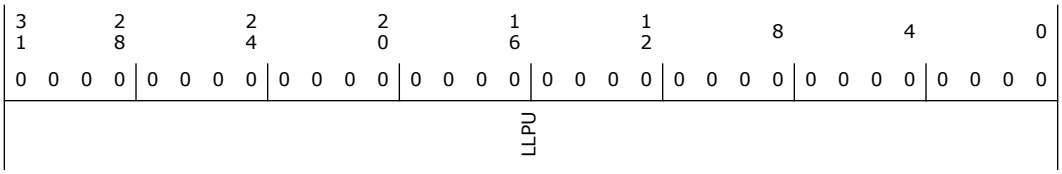
6.2.300 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC9LLPU)—Offset 4B7Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

6.2.301 Input/Output Processing Pipe's Link Connection x Control (OPPLC10CTL)—Offset 4B80h

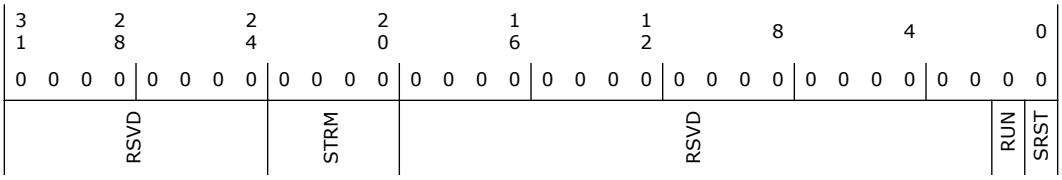
SRST bit is not affected by stream reset.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. 0000=Reserved (Indicates Unused) 0001=Stream 1 ... 1110=Stream 14 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Bit Range	Default & Access	Field Name (ID): Description
19:2	0h RO	Reserved.
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

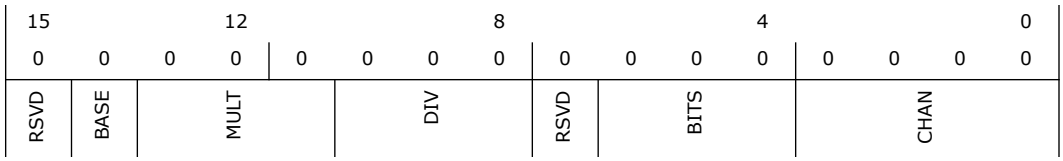
6.2.302 Input/Output Processing Pipe's Link Connection x Format (OPPLC10FMT)—Offset 4B84h

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	Reserved.
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	Reserved.
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

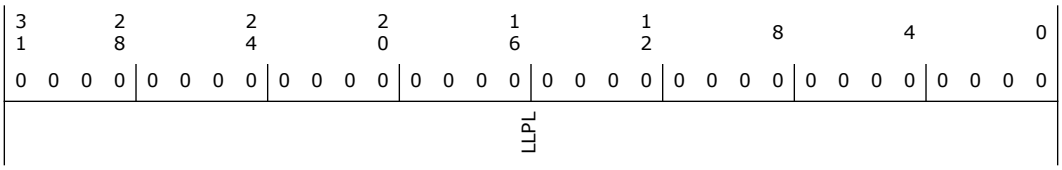
6.2.303 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC10LLPL)—Offset 4B88h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

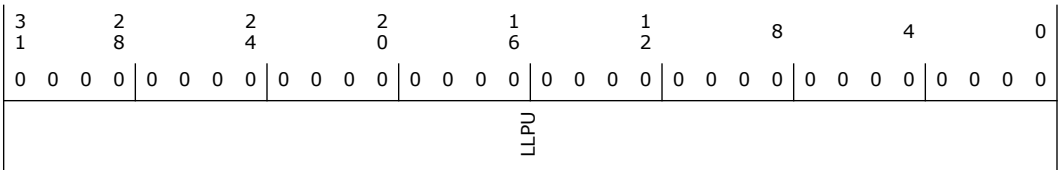
6.2.304 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC10LLPU)—Offset 4B8Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

6.2.305 Input/Output Processing Pipe's Link Connection x Control (OPPLC11CTL)—Offset 4B90h

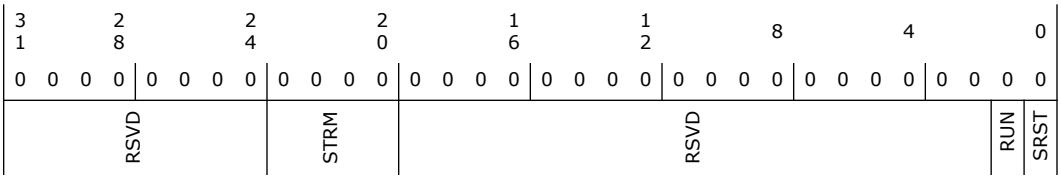
SRST bit is not affected by stream reset.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. 0000=Reserved (Indicates Unused) 0001=Stream 1 ... 1110=Stream 14 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Bit Range	Default & Access	Field Name (ID): Description
19:2	0h RO	Reserved.
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

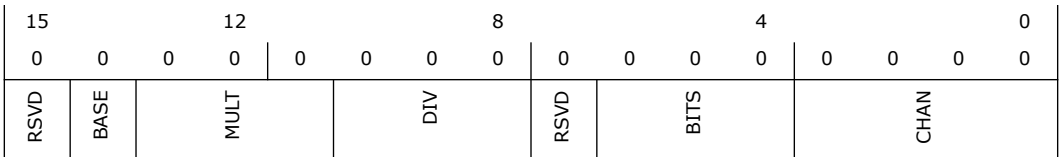
6.2.306 Input/Output Processing Pipe's Link Connection x Format (OPPLC11FMT)—Offset 4B94h

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	Reserved.
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	Reserved.
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

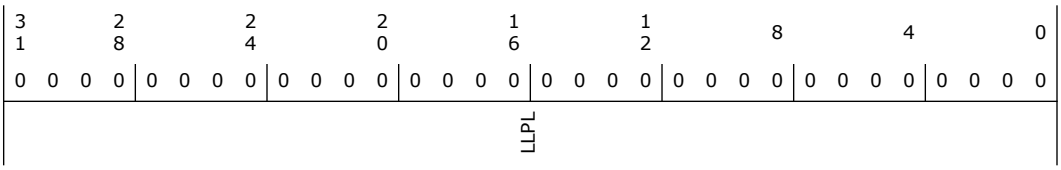
6.2.307 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC11LLPL)—Offset 4B98h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

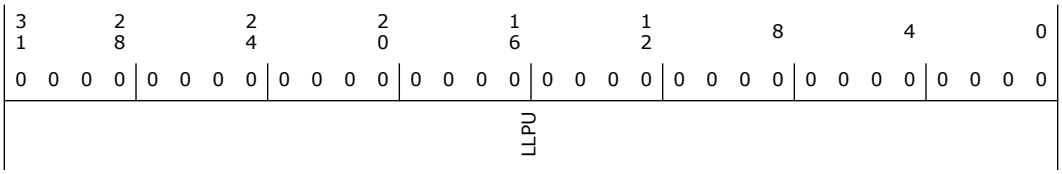
6.2.308 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC11LLPU)—Offset 4B9Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

6.2.309 Input/Output Processing Pipe's Link Connection x Control (OPPLC12CTL)—Offset 4BA0h

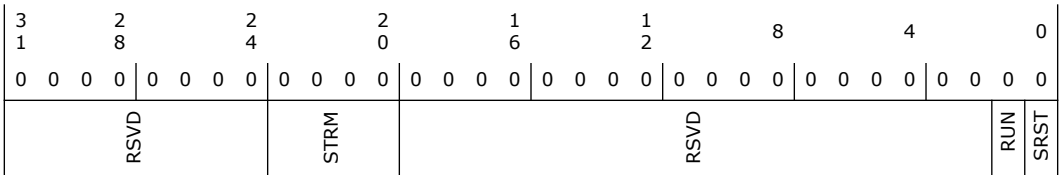
SRST bit is not affected by stream reset.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. 0000=Reserved (Indicates Unused) 0001=Stream 1 ... 1110=Stream 14 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Bit Range	Default & Access	Field Name (ID): Description
19:2	0h RO	Reserved.
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

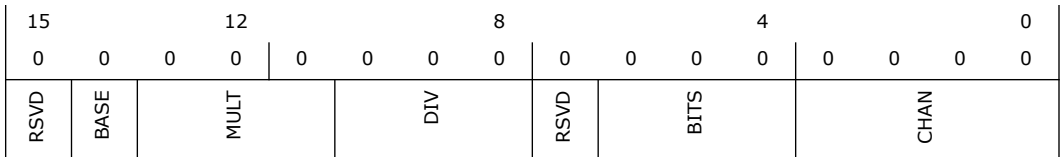
6.2.310 Input/Output Processing Pipe's Link Connection x Format (OPPLC12FMT)—Offset 4BA4h

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	Reserved.
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	Reserved.
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

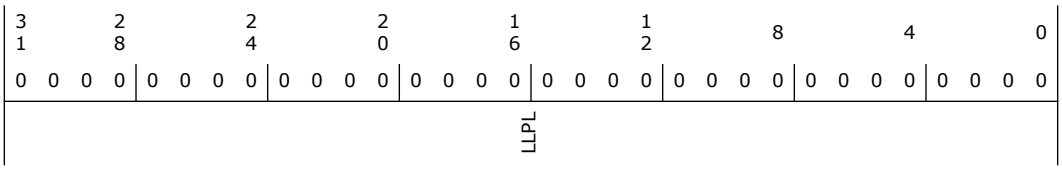
6.2.311 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC12LLPL)—Offset 4BA8h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

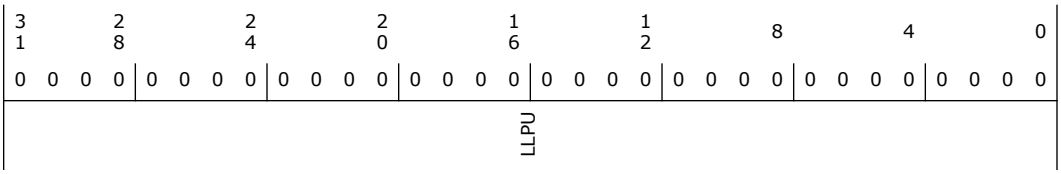
6.2.312 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC12LLPU)—Offset 4BACh

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

6.2.313 Input/Output Processing Pipe's Link Connection x Control (OPPLC13CTL)—Offset 4BB0h

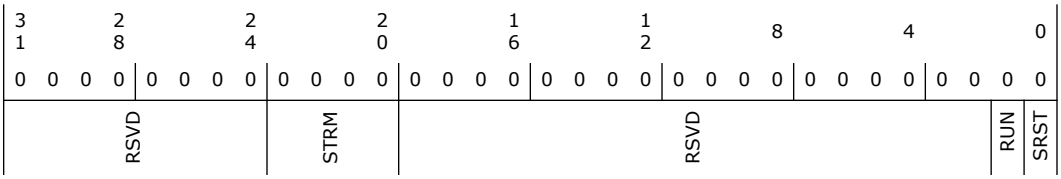
SRST bit is not affected by stream reset.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. 0000=Reserved (Indicates Unused) 0001=Stream 1 ... 1110=Stream 14 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Bit Range	Default & Access	Field Name (ID): Description
19:2	0h RO	Reserved.
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

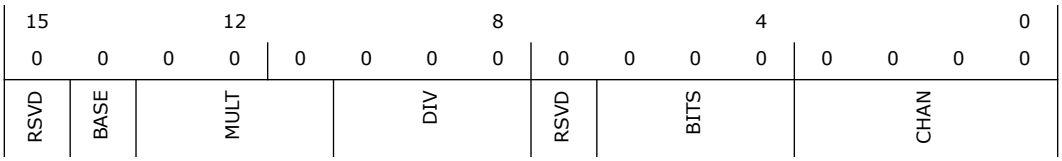
6.2.314 Input/Output Processing Pipe's Link Connection x Format (OPPLC13FMT)—Offset 4BB4h

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	Reserved.
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	Reserved.
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

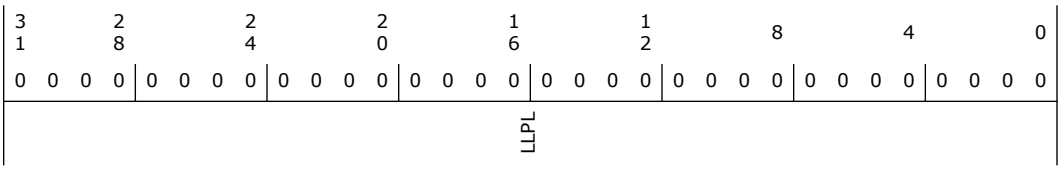
6.2.315 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC13LLPL)—Offset 4BB8h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

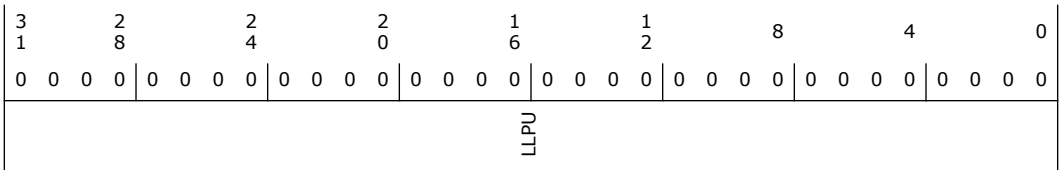
6.2.316 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC13LLPU)—Offset 4BBCh

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

6.2.317 Input/Output Processing Pipe's Link Connection x Control (OPPLC14CTL)—Offset 4BC0h

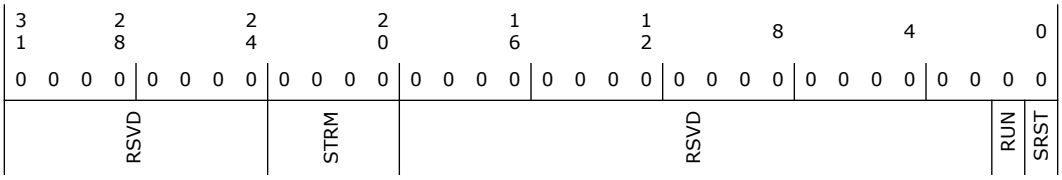
SRST bit is not affected by stream reset.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. 0000=Reserved (Indicates Unused) 0001=Stream 1 ... 1110=Stream 14 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Bit Range	Default & Access	Field Name (ID): Description
19:2	0h RO	Reserved.
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

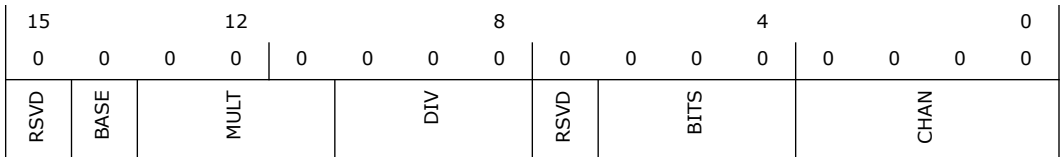
6.2.318 Input/Output Processing Pipe's Link Connection x Format (OPPLC14FMT)—Offset 4BC4h

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	Reserved.
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	Reserved.
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

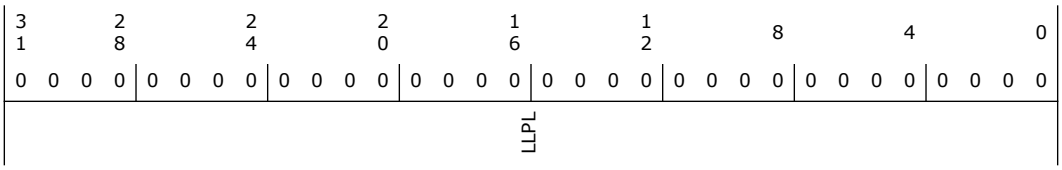
6.2.319 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC14LLPL)—Offset 4BC8h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

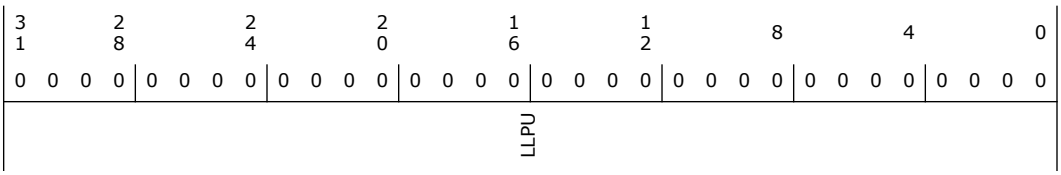
6.2.320 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC14LLPU)—Offset 4BCCh

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

§ §

7 SMBus Interface (D31:F4)

7.1 SMBus Configuration Registers Summary

Table 7-1. Summary of SMBus Configuration Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	1h	Vendor ID (VID)—Offset 0h	8086h
2h	3h	Device ID (DID)—Offset 2h	XXXXh
4h	5h	Command (CMD)—Offset 4h	0h
6h	7h	Device Status (DS)—Offset 6h	280h
8h	8h	Revision ID (RID)—Offset 8h	See register
9h	9h	Programming Interface (PI)—Offset 9h	0h
Ah	Ah	Sub Class Code (SCC)—Offset Ah	5h
Bh	Bh	Base Class Code (BCC)—Offset Bh	Ch
10h	13h	SMBus Memory Base Address_31_0 (SMBMBAR_31_0)—Offset 10h	4h
14h	17h	SMBus Memory Base Address_63_32 (SMBMBAR_63_32)—Offset 14h	0h
20h	23h	SMB Base Address (SBA)—Offset 20h	1h
2Ch	2Dh	SVID (SVID)—Offset 2Ch	0h
2Eh	2Fh	SID (SID)—Offset 2Eh	0h
3Ch	3Ch	Interrupt Line (INTLN)—Offset 3Ch	0h
3Dh	3Dh	Interrupt Pin (INTPN)—Offset 3Dh	1h
40h	40h	Host Configuration (HCFG)—Offset 40h	0h
50h	53h	TCO Base Address (TCOBASE)—Offset 50h	1h
54h	57h	TCO Control (TCOCTL)—Offset 54h	0h
64h	67h	Host SMBus Timing (HTIM)—Offset 64h	0h
80h	83h	SMBus Power Gating (SMBSM)—Offset 80h	40000h

7.1.1 Vendor ID (VID)—Offset 0h

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 4

Default: 8086h

15			12				8				4				0
1	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0
VID															

Bit Range	Default & Access	Field Name (ID): Description
15:0	8086h RO	**Vendor ID (VID):** Value indicates Intel as the vendor

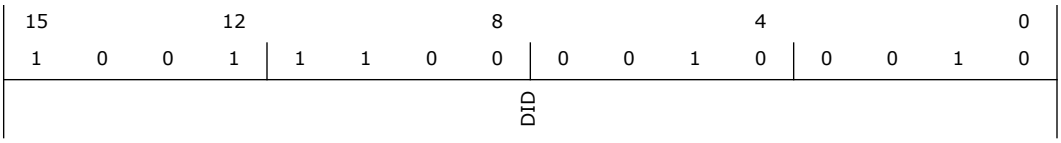
7.1.2 Device ID (DID)—Offset 2h

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 4

Default: XXXXh



Bit Range	Default & Access	Field Name (ID): Description
15:0	-- RO	**Device ID (DID):** Indicates the value assigned to the PCH SMBus controller. Refer to Device and Revision ID table in Volume 1 for specific value.

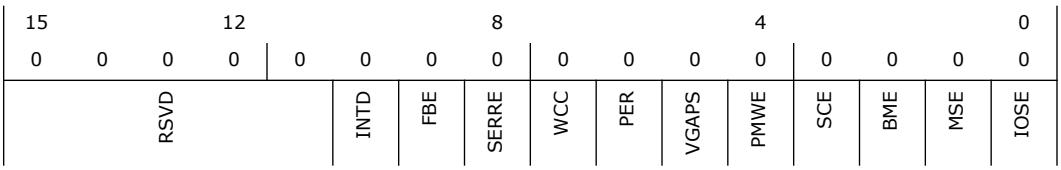
7.1.3 Command (CMD)—Offset 4h

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 4

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:11	0h RO	Reserved.
10	0h RW	**Interrupt Disable (INTD):** 1 = Disables SMBus to assert its PIRQB# signal. Defaults to 0.
9	0h RW	**Fast Back to Back Enable (FBE):** Reserved as 0. Read Only.
8	0h RW	**SERR# Enable (SERRE):** 1 = Enables SERR# generation

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Wait Cycle Control (WCC):** Reserved as 0. Read Only.
6	0h RW	**Parity Error Response (PER):** 1 = Sets Detected Parity Error bit when parity error is detected
5	0h RW	**VGA Palette Snoop (VGAPS):** Reserved as 0. Read Only.
4	0h RW	**Postable Memory Write Enable (PMWE):** Reserved as 0. Read Only.
3	0h RW	**Special Cycle Enable (SCE):** Reserved as 0. Read Only.
2	0h RW	**Bus Master Enable (BME):** Reserved as 0. Read Only.
1	0h RW	**Memory Space Enable (MSE):** 1= Enables memory mapped config space.
0	0h RW	**I/O Space Enable (IOSE):** 1= enables access to the SM Bus I/O space registers as defined by the Base Address Register.

7.1.4 Device Status (DS)—Offset 6h

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 4

Default: 280h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0
DPE	SSE	RMA	RTA	STA	DEVT		DPED	FBC	UDF	C_66M	CLI	INTS	RSVD		

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1C	**Detected Parity Error (DPE):** 1 = Parity error detected
14	0h RW/1C	**Signaled System Error (SSE):** 1 = System error detected
13	0h RO	**Received Master Abort (RMA):** Reserved as 0.
12	0h RO	**Received Target Abort (RTA):** Reserved as '0'.
11	0h RO	**Signaled Target-Abort Status (STA):** Reserved as 0.
10:9	1h RO	**DEVSEL# Timing Status (DEVT):** This 2-bit field defines the timing for DEVSEL# assertion. These read only bits indicate the Intel PCH's DEVSEL# timing when performing a positive decode. Note: Intel PCH generates DEVSEL# with medium time.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RO	**Data Parity Error Detected (DPED):** Reserved as 0.
7	1h RO	**Fast Back-to-Back Capable (FBC):** Reserved as '1'.
6	0h RO	**User Definable Features (UDF):** Reserved as 0.
5	0h RO	**66 MHz Capable (C_66M):** Reserved as 0.
4	0h RO	**Capabilities List Indicator (CLI):** Hardwired to 0 because there are no capability list structures in this function.
3	0h RO	**Interrupt Status (INTS):** This bit indicates that an interrupt is pending. It is independent from the state of the Interrupt Enable bit in the command register.
2:0	0h RO	Reserved.

7.1.5 Revision ID (RID)—Offset 8h

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 31
Function: 4

Default: See register

7			4				0
0	0	0	0	0	0	0	0
RID							

Bit Range	Default & Access	Field Name (ID): Description
7:0	-- RO	**Revision ID (RID):** Indicates stepping of the host controller. Refer to Device and Revision ID table in Volume 1 for specific value.

7.1.6 Programming Interface (PI)—Offset 9h

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 31
Function: 4

Default: 0h

7			4				0
0	0	0	0	0	0	0	0
PI							

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RO	**Programming Interface (PI):** No programming interface defined.

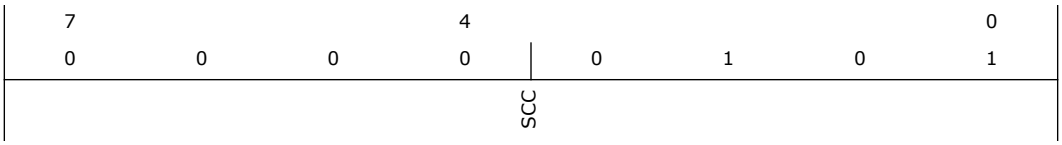
7.1.7 Sub Class Code (SCC)—Offset Ah

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 31
Function: 4

Default: 5h



Bit Range	Default & Access	Field Name (ID): Description
7:0	5h RO	**Sub Class Code (SCC):** A value of 05h indicates that this device is a SM Bus serial controller.

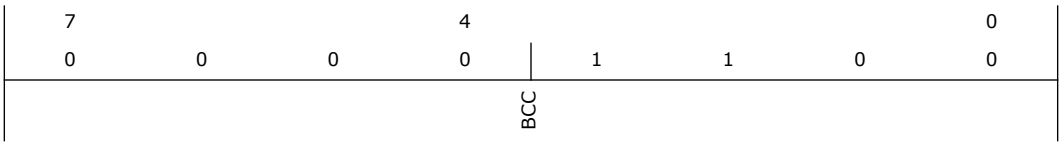
7.1.8 Base Class Code (BCC)—Offset Bh

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 31
Function: 4

Default: Ch



Bit Range	Default & Access	Field Name (ID): Description
7:0	Ch RO	**Base Class Code (BCC):** A value of 0Ch indicates that this device is a serial controller

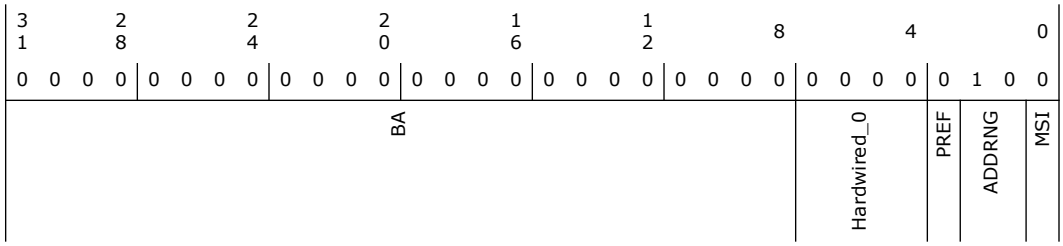
7.1.9 SMBus Memory Base Address_31_0 (SMBMBAR_31_0)—Offset 10h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 4

Default: 4h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RW	**Base Address (BA):** Provides the 32 byte system memory base address for the Intel PCH SMB logic.
7:4	0h RO	**Hardwired_0 (Hardwired_0):** Hardwired to 0.
3	0h RO	**Prefetchable (PREF):** Hardwired to 0. Indicated that SMBMBAR is not pre-fetchable
2:1	2h RO	**Address Range (ADDRNG):** Indicates that this SMBMBAR can be located anywhere in 64 bit address space
0	0h RO	**Memory Space Indicator (MSI):** Indicates that the SMB logic is memory mapped.

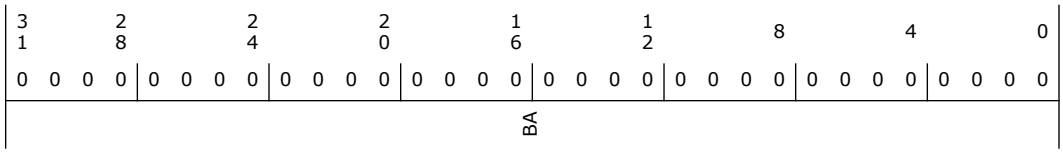
7.1.10 SMBus Memory Base Address_63_32 (SMBMBAR_63_32)—Offset 14h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 4

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Base Address (BA):** Bits 63-32 of SMbus Memory Base Address

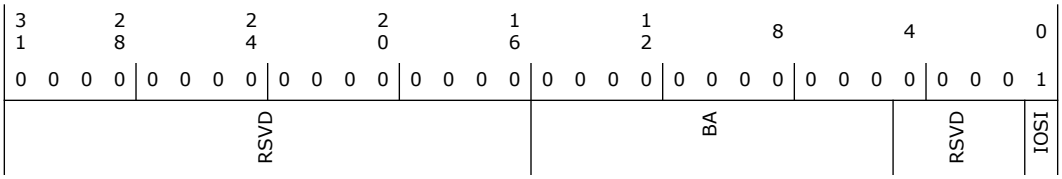
7.1.11 SMB Base Address (SBA)—Offset 20h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 4

Default: 1h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:5	0h RW	**Base Address (BA):** Provides the 32 byte system I/O base address for the SMB logic.
4:1	0h RO	Reserved.
0	1h RO	**IO Space Indicator (IOSI):** This read-only bit always is 1, indicating that the SMB logic is I/O mapped.

7.1.12 SVID (SVID)—Offset 2Ch

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 4

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW/O	**SVID (SVID):** BIOS sets the value in this register to identify the Subsystem Vendor ID. The SMBus SVID register, in combination with the SMBus Subsystem ID register, enables the operating system to distinguish each subsystem from the others. Note: The software can write to this register only once per core well reset. Writes should be done as a single 16-bit cycle.

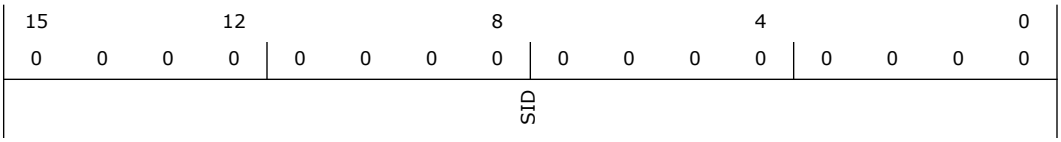
7.1.13 SID (SID)—Offset 2Eh

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 4

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW/O	**SID (SID):** BIOS can write to this register to identify the Subsystem ID. The SID register, in combination with the SVID, enable the operating system to distinguish each subsystem from other(s). Note: The software can write to this register only once per core well reset. Writes should be done as a single 16-bit cycle.

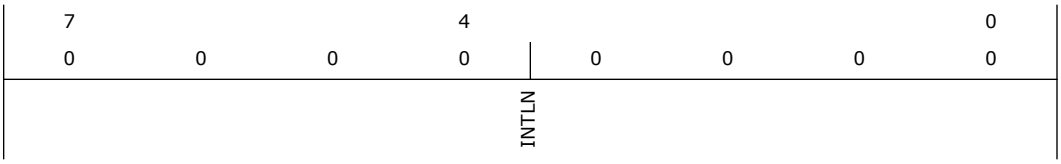
7.1.14 Interrupt Line (INTLN)—Offset 3Ch

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 31
Function: 4

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**Interrupt Line (INTLN):** This data is not used by the hardware. It is to communicate to software the interrupt line that the interrupt pin is connected to PIRQB#.

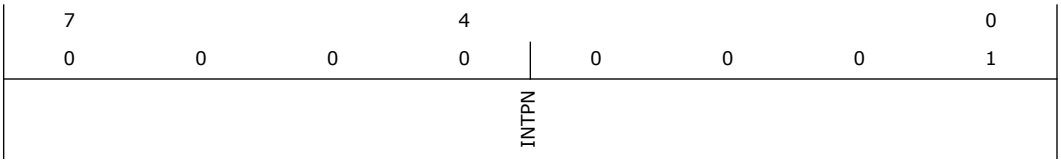
7.1.15 Interrupt Pin (INTPN)—Offset 3Dh

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 31
Function: 4

Default: 1h



Bit Range	Default & Access	Field Name (ID): Description
7:0	1h RW/O	**Interrupt Pin (INTPN):** This defines the interrupt pin to be used by the SMBus controller. Bits : Pins 0h : No Interrupt 1h : INTA# 2h : INTB# 3h : INTC# 4h : INTD# 5h-Fh : Reserved

7.1.16 Host Configuration (HCFG)—Offset 40h

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 31
Function: 4

Default: 0h

7			4				0
0	0	0	0	0	0	0	0
RSVD			SPDWD	SSRESET	I2CEN	SSEN	HSTEN

Bit Range	Default & Access	Field Name (ID): Description
7:5	0h RO	Reserved.
4	0h RW/O	**SPD Write Disable (SPDWD):** When this bit is set to 1, writes to SMBus addresses 50h – 57h are disabled. Note: This bit is R/WO and will be reset on PLTRST# assertion. This bit should be set by BIOS to '1'. Software can only program this bit when both the START bit and Host Busy bit are '0'; otherwise, the write may result in undefined behavior.
3	0h RW	**SSRESET (SSRESET):** Soft SMBUS Reset: When this bit is 1, the SMbus state machine and logic in PCH is reset. The HW will reset this bit to 0 when reset operation is completed.
2	0h RW	**I2C_EN (I2CEN):** When this bit is 1, the Intel PCH is enabled to communicate with I2C devices. This will change the formatting of some commands. When this bit is 0, behavior is for SMBus.
1	0h RW	**SMB_SMI_EN (SSEN):** When this bit is set, any source of an SMB interrupt will instead be routed to generate an SMI#.
0	0h RW	**HST_EN (HSTEN):** When set, the SMB Host Controller interface is enabled to execute commands. The HST_INT_EN bit needs to be enabled in order for the SMB Host Controller to interrupt or SMI#. Additionally, the SMB Host Controller will not respond to any new requests until all interrupt requests have been cleared.

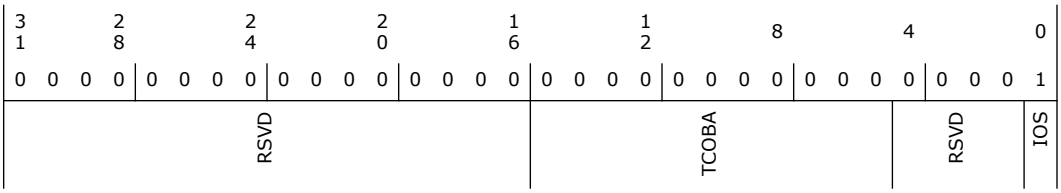
7.1.17 TCO Base Address (TCOBASE)—Offset 50h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 4

Default: 1h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:5	0h RW	**TCO Base Address (TCOBA):** Provides the 32 bytes of I/O space for TCO logic, mappable anywhere in the 64k I/O space on 32-byte boundaries.
4:1	0h RO	Reserved.
0	1h RO	**I/O Space (IOS):** Indicates an I/O Space

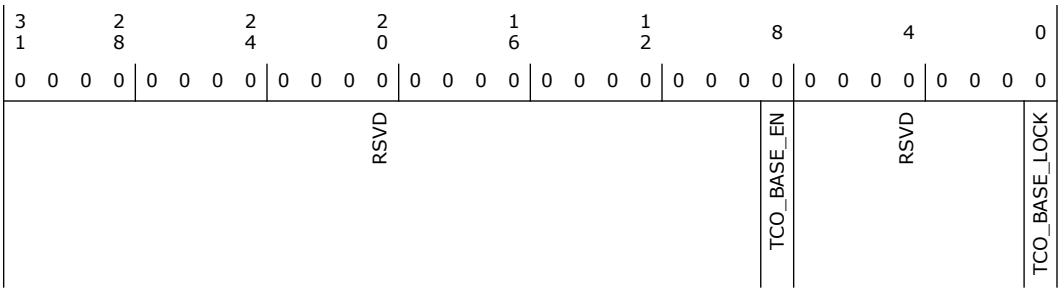
7.1.18 TCO Control (TCOCTL)—Offset 54h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 4

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h RW	**TCO Base Enable (TCO_BASE_EN):** When set, decode of the I/O range pointed to by the TCO base register is enabled.
7:1	0h RO	Reserved.
0	0h RW/O	**TCO Base Lock (TCO_BASE_LOCK):** When set to 1, this bit locks down the TCO Base Address Register (TCOBASE) at offset 50h. The Base Address Field becomes read-only. This bit becomes locked when a value of 1b is written to it. Writes of 0 to this bit are always ignored. Once locked by writing 1, the only way to clear this bit is to perform a platform reset.

7.1.19 Host SMBus Timing (HTIM)—Offset 64h

BIOS may need to program this register.

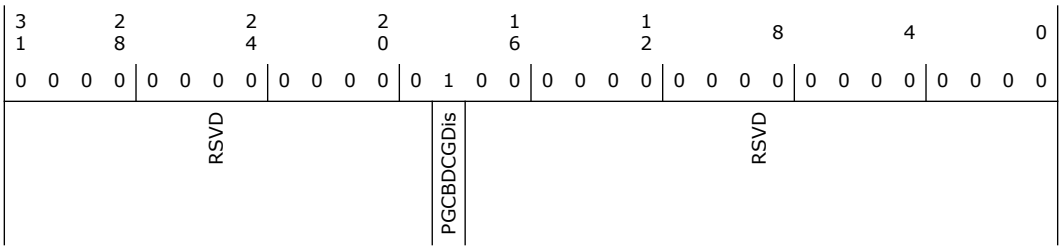
7.1.20 SMBus Power Gating (SMBSM)—Offset 80h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 4

Default: 40000h



Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	Reserved.
18	1h RW	**SMBus Dynamic Clock Gating (PGCBDCGDis):** Setting this bit will disable the SMBus dynamic clock gating.
17:0	0h RO	Reserved.

7.2

7.3 SMBus I/O and Memory Mapped I/O Registers Summary

The SMBus registers can be accessed through I/O BAR or Memory BAR registers in PCI configuration space. The offsets are the same for both I/O and Memory Mapped I/O registers.

Table 7-2. Summary of SMBus I/O and Memory Mapped I/O Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	0h	Host Status Register Address (HSTS)—Offset 0h	0h
2h	2h	Host Control Register (HCTL)—Offset 2h	0h
3h	3h	Host Command Register (HCMD)—Offset 3h	0h
4h	4h	Transmit Slave Address Register (TSA)—Offset 4h	0h
5h	5h	Data 0 Register (HD0)—Offset 5h	0h

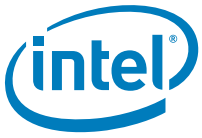


Table 7-2. Summary of SMBus I/O and Memory Mapped I/O Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
6h	6h	Data 1 Register (HD1)—Offset 6h	0h
7h	7h	Host Block Data (HBD)—Offset 7h	0h
8h	8h	Packet Error Check Data Register (PEC)—Offset 8h	0h
9h	9h	Receive Slave Address Register (RSA)—Offset 9h	44h
Ah	Bh	Slave Data Register (SD)—Offset Ah	0h
Ch	Ch	Auxiliary Status (AUXS)—Offset Ch	0h
Dh	Dh	Auxiliary Control (AUXC)—Offset Dh	0h
Eh	Eh	SMLINK_PIN_CTL Register (SMLC)—Offset Eh	4h
Fh	Fh	SMBUS_PIN_CTL Register (SMBC)—Offset Fh	4h
10h	10h	Slave Status Register (SSTS)—Offset 10h	0h
11h	11h	Slave Command Register (SCMD)—Offset 11h	0h
14h	14h	Notify Device Address Register (NDA)—Offset 14h	0h
16h	16h	Notify Data Low Byte Register (NDLB)—Offset 16h	0h
17h	17h	Notify Data High Byte Register (NDHB)—Offset 17h	0h

7.3.1 Host Status Register Address (HSTS)—Offset 0h

All status bits are set by hardware and cleared by the software writing a one to the particular bit position. Writing a zero to any bit position has no affect.

Access Method

Type: IO Register
(Size: 8 bits)

Device: 31
Function: 4

Default: 0h

7			4				0
0	0	0	0	0	0	0	0
BDS	IUS	SMSTS	FAIL	BERR	DERR	INTR	HBSY

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW/1C	**BYTE_DONE_STS (BDS):** This bit will be set to 1 when the host controller has received a byte (for Block Read commands) or if it has completed transmission of a byte (for Block Write commands) when the 32-byte buffer is not being used. Note that this bit will be set, even on the last byte of the transfer. Software clears the bit by writing a 1 to the bit position. This bit has no meaning for block transfers when the 32- byte buffer is enabled. Note: When the last byte of a block message is received, the host controller will set this bit. However, it will not immediately set the INTR bit (bit 1 in this register). When the interrupt handler clears the BYTE_DONE_STS bit, the message is considered complete, and the host controller will then set the INTR bit (and generate another interrupt). Thus, for a block message of n bytes, the Intel PCH will generate n+1 interrupts. The interrupt handler needs to be implemented to handle these cases.
6	0h RW	**In Use Status (IUS):** After a full PCI reset, a read to this bit returns a 0. After the first read, subsequent reads will return a 1. A write of a 1 to this bit will reset the next read value to 0. Writing a 0 to this bit has no effect. Software can poll this bit until it reads a 0, and will then own the usage of the host controller. This bit has no other effect on the hardware, and is only used as semaphore among various independent software threads that may need to use the Intel PCHs SMBus logic.
5	0h RW/1C	**SMBALERT_STS (SMSTS):** Intel PCH sets this bit to a 1 to indicates source of the interrupt or SMI# was the SMBAlert# signal. Software resets this bit by writing a 1 to this location. This bit should also be cleared by RSMRST# (but not PLTRST#).
4	0h RW/1C	**Failed (FAIL):** When set, this indicates that the source of the interrupt or SMI# was a failed bus transaction. This is set in response to the KILL bit being set to terminate the host transaction.
3	0h RW/1C	**Bus Error (BERR):** When set, this indicates the source of the interrupt or SMI# was a transaction collision.
2	0h RW/1C	**Device Error (DERR):** When set, this indicates that the source of the interrupt or SMI# was due one of the following: Illegal Command Field Unclaimed Cycle (host initiated) Host Device Time-out Error. CRC Error
1	0h RW/1C	**Interrupt (INTR):** When set, this indicates that the source of the interrupt or SMI# was the successful completion of its last command.
0	0h RW/1C	**Host Busy (HBSY):** A 1 indicates that the Intel PCH is running a command from the host interface. No SMB registers should be accessed while this bit is set. Exception: The BLOCK DATA REGISTER can be accessed when this bit is set ONLY when the SMB_CMD bits (in Host control register) are programmed for Block command or I2C Read command. This is necessary in order to check the DONE_STS bit.

7.3.2 Host Control Register (HCTL)—Offset 2h

Note: A read to this register will clear the pointer in the 32-byte buffer.

Access Method

Type: IO Register
(Size: 8 bits)

Device: 31
Function: 4

Default: 0h

7			4				0
0	0	0	0	0	0	0	0
PEC_EN	START	LAST_BYTE	SMB_CMD			KILL	INTREN

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**PEC_EN (PEC_EN):** When set to 1, this bit causes the host controller to perform the SMBus transaction with the Packet Error Checking phase appended. For writes, the value of the PEC byte is transferred from the PEC Register. For reads, the PEC byte is loaded in to the PEC Register. When this bit is cleared to 0, the SMBus host controller does not perform the transaction with the PEC phase appended. This bit must be written prior to the write in which the START bit is set.
6	0h RW	**START (START):** This write-only bit is used to initiate the command described in the SMB_CMD field. All registers should be setup prior to writing a 1 to this bit position. This bit always reads zero. The HOST_BUSY bit in the Host Status register (offset 00h) can be used to identify when the Intel PCH has finished the command.
5	0h RW	**LAST_BYTE (LAST_BYTE):** This bit is used for I2C Read commands. Software sets this bit to indicate that the next byte will be the last byte to be received for the block. This causes the PCH to send a NACK (instead of an ACK) after receiving the last byte. Note: This bit may be set when the TCO timer causes the SECOND_TO_STS bit to be set. SW should clear the LAST_BYTE bit (if it is set) before starting any new command. Note: In addition to I2C Read Commands, the LAST_BYTE bit will also cause Block Read/Write cycles to stop prematurely (at the end of the next byte).
4:2	0h RW	**SMB_CMD (SMB_CMD):** As shown by the bit encoding below, indicates which command the Intel PCH is to perform. If enabled, the Intel PCH will generate an interrupt or SMI# when the command has completed If the value is for a non-supported or reserved command, the Intel PCH will set the device error (DEV_ERR) status bit and generate an interrupt when the START bit is set. The Intel PCH will perform no command, and will not operate until DEV_ERR is cleared. Val - Command Description: 000 - Quick: The slave address and read/write value (bit 0) are stored in the tx slave address register. 001 - Byte: This command uses the transmit slave address and command registers. Bit 0 of the slave address register determines if this is a read or write command. 010 - Byte Data: This command uses the transmit slave address, command, and DATA0 registers. Bit 0 of the slave address register determines if this is a read or write command. If it is a read, the DATA0 register will contain the read data. 011 - Word Data: This command uses the transmit slave address, command, DATA0 and DATA1 registers. Bit 0 of the slave address register determines if this is a read or write command. If it is a read, after the command completes the DATA0 and DATA1 registers will contain the read data. 100 - Process Call: This command uses the transmit slave address, command, DATA0 and DATA1 registers. Bit 0 of the slave address register determines if this is a read or write command. After the command completes, the DATA0 and DATA1 registers will contain the read data. 101 - Block: This command uses the transmit slave address,command, and DATA0 registers, and the Block Data Byte register. For block write, the count is stored in the DATA0 register and indicates how many bytes of data will be transferred. For block reads, the count is received and stored in the DATA0 register. Bit 0 of the slave address register selects if this is a read or write command. For writes, data is retrieved from the first n (where n is equal to the specified count) addresses of the SRAM array. For reads, the data is stored in the Block Data Byte register. 110 - I2C Read: This command uses the transmit slave address, command, DATA0, DATA1 registers, and the Block Data Byte register. The read data is stored in the Block Data Byte register. The Intel PCH will continue reading data until the NAK is received. 111 - Block-Process: This command uses the transmit slave address, command, DATA0 and the Block Data Byte register. For block write, the count is stored in the DATA0 register and indicates how many bytes of data will be transferred. For block read, the count is received and stored in the DATA0 register. Bit 0 of the slave address register always indicate a write command. For writes, data is retrieved from the first m (where m is equal to the specified count) addresses of the SRAM array. For reads, the data is stored in the Block Data Byte register. Note: E32B bit in the Auxiliary Control Register must be set for this command to work.
1	0h RW	**KILL (KILL):** When set, kills the current host transaction taking place, sets the FAILED status bit, and asserts the interrupt (or SMI#) selected by the SMB_INTRSEL field. This bit, once set, must be cleared to allow the SMB Host Controller to function normally.
0	0h RW	**INTREN (INTREN):** Enable the generation of an interrupt or SMI# upon the completion of the command.

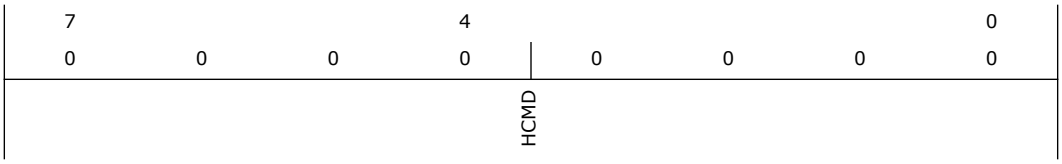
7.3.3 Host Command Register (HCMD)—Offset 3h

Access Method

Type: IO Register
(Size: 8 bits)

Device: 31
Function: 4

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**Host Command Register (HCMD):** This eight bit field is transmitted by the host controller in the command field of the SMB protocol during the execution of any command.

7.3.4 Transmit Slave Address Register (TSA)—Offset 4h

This register is transmitted by the host controller in the slave address field of the SMB protocol. This is the address of the target.

Access Method

Type: IO Register
(Size: 8 bits)

Device: 31
Function: 4

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:1	0h RW	**ADDRESS (ADDR):** 7-bit address of the targeted slave. Note: Writes to TSA values of A0h - AEh are blocked depending on the setting of the SPD write disable bit in HCFG - HostConfiguration.
0	0h RW	**RW (RW):** Direction of the host transfer. 1 = read, 0 = write

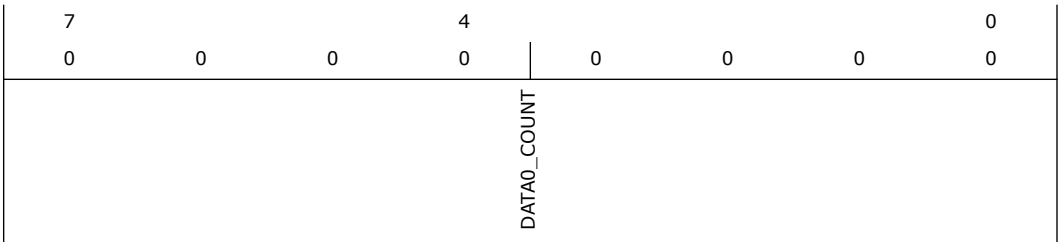
7.3.5 Data 0 Register (HD0)—Offset 5h

Access Method

Type: IO Register
(Size: 8 bits)

Device: 31
Function: 4

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**DATA0/COUNT (DATA0_COUNT):** This field contains the eight bit data sent in the DATA0 field of the SMB protocol. For block write commands, this register reflects the number of bytes to transfer. This register should be programmed to a value between 1 and 32 for block counts. A count of 0 or a count above 32 will result in unpredictable behavior. The host controller does not check or log illegal block counts.

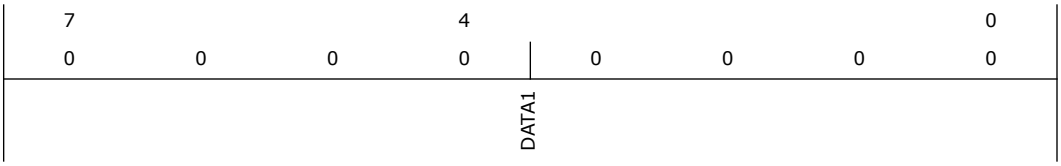
7.3.6 Data 1 Register (HD1)—Offset 6h

Access Method

Type: IO Register
(Size: 8 bits)

Device: 31
Function: 4

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**DATA1 (DATA1):** This eight bit register is transmitted in the DATA1 field of the SMB protocol during the execution of any command.

7.3.7 Host Block Data (HBD)—Offset 7h

Access Method

Type: IO Register
(Size: 8 bits)

Device: 31
Function: 4

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**Block Data (BDTA):** This is either a register, or a pointer into a 32- byte block array, depending upon whether the E32B bit is set in the Auxiliary Control register. When the E32B bit is cleared, this is a register containing a byte of data to be sent on a block write or read from on a block read, just as it behaved on the INTEL PCH. When the E32B bit is set, reads and writes to this register are used to access the 32-byte block data storage array. An internal index pointer is used to address the array, which is reset to 0 by reading the HCTL register (offset 02h). The index pointer then increments automatically upon each access to this register. The transfer of block data into (read) or out of (write) this storage array during an SMBus transaction always starts at index address 0. When the E2B bit is set, for writes, software will write up to 32-bytes to this register as part of the setup for the command. After the Host Controller has sent the Address, Command, and Byte Count fields, it will send the bytes in the SRAM pointed to by this register. When the E2B bit is cleared for writes, software will place a single byte in this register. After the host controller has sent the address, command, and byte count fields, it will send the byte in this register. If there is more data to send, software will write the next series of bytes to the SRAM pointed to by this register and clear the DONE_STS bit. The controller will then send the next byte. During the time between the last byte being transmitted to the next byte being transmitted, the controller will insert wait-states on the interface. When the E2B bit is set for reads, after receiving the byte count into the Data0 register, the first series of data bytes go into the SRAM pointed to by this register. If the byte count has been exhausted or the 32-byte SRAM has been filled, the controller will generate an SMI# or interrupt (depending on configuration) and set the DONE_STS bit. Software will then read the data. During the time between when the last byte is read from the SRAM to when the DONE_STS bit is cleared, the controller will insert waitstates on the interface.

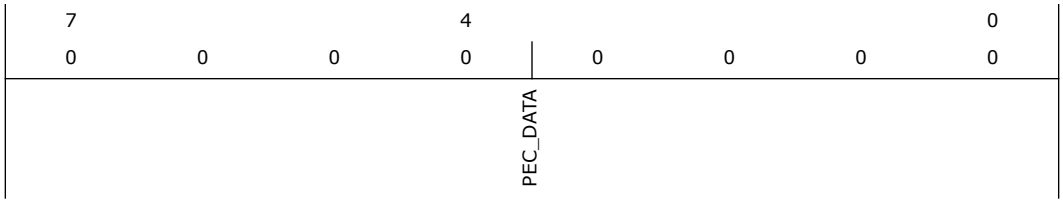
7.3.8 Packet Error Check Data Register (PEC)—Offset 8h

Access Method

Type: IO Register
(Size: 8 bits)

Device: 31
Function: 4

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**PEC_DATA (PEC_DATA):** This 8-bit register is written with the SMBus PEC data prior to a write transaction. For read transactions, the PEC data is loaded from the SMBus into this register and is then read by software. Software must ensure that the INUSE_STS bit is properly maintained to avoid having this field over-written by a write transaction following a read transaction.

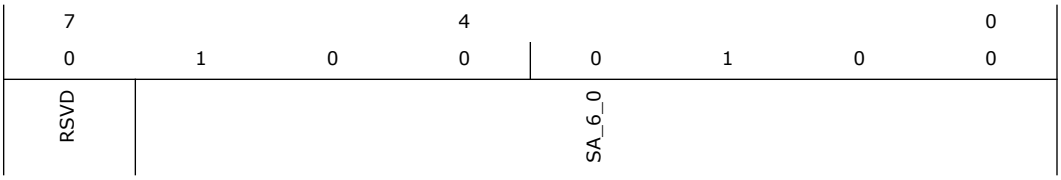
7.3.9 Receive Slave Address Register (RSA)—Offset 9h

Access Method

Type: IO Register
(Size: 8 bits)

Device: 31
Function: 4

Default: 44h



Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	Reserved.
6:0	44h RW	**SLAVE_ADDR[6:0] (SA_6_0):** This field is the slave address that the Intel PCH decodes for read and write cycles. The default is not 0 so that it can respond even before the CPU comes up (or if the CPU is dead). This register is reset by RSMRST#, but not by PLTRST#.

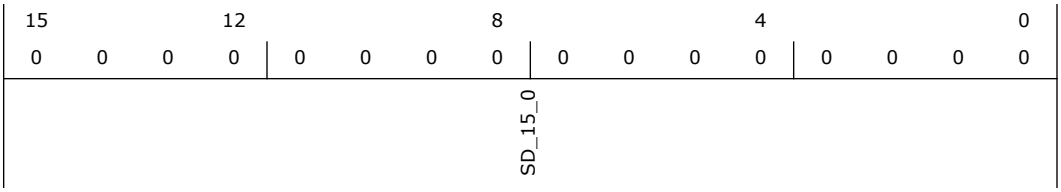
7.3.10 Slave Data Register (SD)—Offset Ah

Access Method

Type: IO Register
(Size: 16 bits)

Device: 31
Function: 4

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW	**SLAVE_DATA[15:0] (SD_15_0):** This field is the 16-bit data value written by the external SMBus master. The CPU can then read the value from this register. This register is reset by RSMRST#, but not by PLTRST#. SLAVE_DATA(7:0) corresponds to the Data Message Byte 0 at Slave Write Register 4 in the table. SLAVE_(15:8) corresponds to the Data Message Byte 1 at Slave Write Register 5 in the table.

7.3.11 Auxiliary Status (AUXS)—Offset Ch

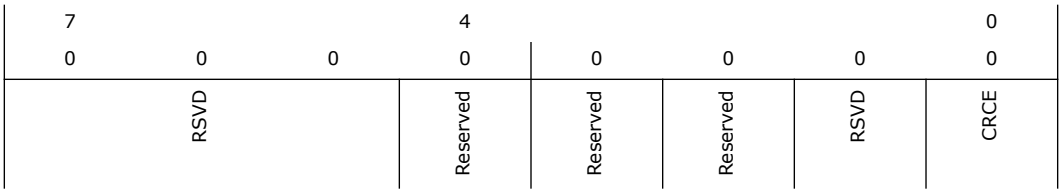
All bits in this register are in the core well.

Access Method

Type: IO Register
(Size: 8 bits)

Device: 31
Function: 4

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7:5	0h RO	Reserved.
4	0h RO	**Reserved**
3	0h RO	**Reserved**
2	0h RO	**Reserved**
1	0h RO	Reserved.
0	0h RW/1C	**CRC Error (CRCE):** This bit is set if a received message contained a CRC error. When this bit is set, the DERR bit of the host status register will also be set. This bit will be set by the controller if a software abort occurs in the middle of the CRC portion of the cycle or an abort happens after Intel PCH has received the final data bit transmitted by external slave.

7.3.12 Auxiliary Control (AUXC)—Offset Dh

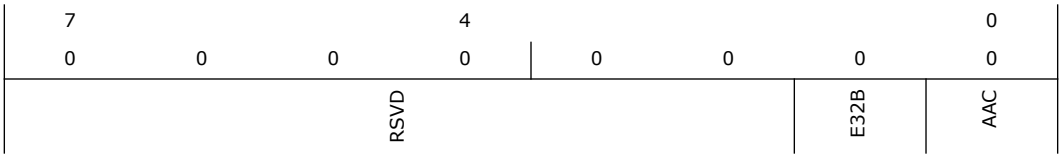
All bits in this register are in the resume well.

Access Method

Type: IO Register
(Size: 8 bits)

Device: 31
Function: 4

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7:2	0h RO	Reserved.
1	0h RW	**Enable 32-byte Buffer (E32B):** When set, the Host Block Data register is a pointer into a 32-byte buffer, as opposed to a single register. This enables the block commands to transfer or receive up to 32-bytes before the Intel PCH generates an interrupt.
0	0h RW	**Automatically Append CRC (AAC):** When set, the Intel PCH will automatically append the CRC. This bit must not be changed during SM Bus transactions, or undetermined behavior will result. It should be programmed only once during the lifetime of the function.

7.3.13 SMLINK_PIN_CTL Register (SMLC)—Offset Eh

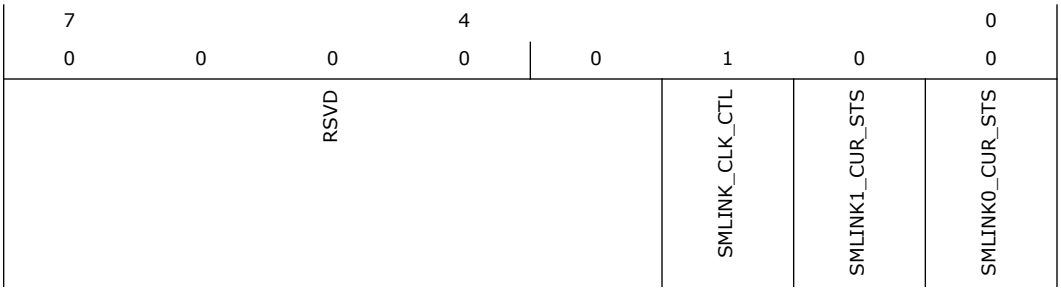
Note: This register is in the resume well and is reset by RSMRST#

Access Method

Type: IO Register
(Size: 8 bits)

Device: 31
Function: 4

Default: 4h



Bit Range	Default & Access	Field Name (ID): Description
7:3	0h RO	Reserved.
2	1h RW	**SMLINK_CLK_CTL (SMLINK_CLK_CTL):** 0 = Intel PCH will drive the SMLINK(0) pin low, independent of what the other SMLINK logic would otherwise indicate for the SMLINK(0) pin. 1 = The SMLINK(0) pin is Not overdriven low. The other SMLINK logic controls the state of the pin.
1	0h RO	**SMLINK[1]_CUR_STS (SMLINK1_CUR_STS):** This bit has a default value that is dependent on an external signal level. This returns the value on the SMLINK(1) pin. It will be 1 to indicate high, 0 to indicate low. This allows software to read the current state of the pin.
0	0h RO	**SMLINK[0]_CUR_STS (SMLINK0_CUR_STS):** This bit has a default value that is dependent on an external signal level. This returns the value on the SMLINK(0) pin. It will be 1 to indicate high, 0 to indicate low. This allows software to read the current state of the pin.

7.3.14 SMBUS_PIN_CTL Register (SMBC)—Offset Fh

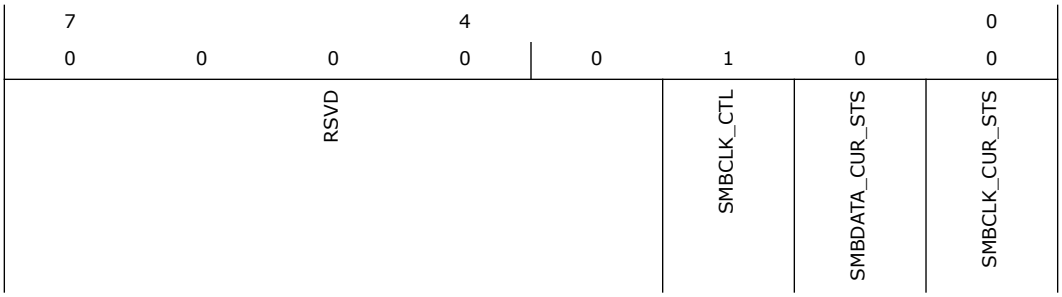
Note: This register is in the resume well and is reset by RSMRST#

Access Method

Type: IO Register
(Size: 8 bits)

Device: 31
Function: 4

Default: 4h



Bit Range	Default & Access	Field Name (ID): Description
7:3	0h RO	Reserved.
2	1h RW	**SMBCLK_CTL (SMBCLK_CTL):** 0 = Intel PCH will drive the SMBCLK pin low, independent of what the other SMB logic would otherwise indicate for the SMBCLK pin. 1 = The SMBCLK pin is Not overdriven low. The other SMBus logic controls the state of the pin.
1	0h RO	**SMBDATA_CUR_STS (SMBDATA_CUR_STS):** This bit has a default value that is dependent on an external signal level. This returns the value on the SMBDATA pin. It will be 1 to indicate high, 0 to indicate low. This allows software to read the current state of the pin.
0	0h RO	**SMBCLK_CUR_STS (SMBCLK_CUR_STS):** This bit has a default value that is dependent on an external signal level. This returns the value on the SMBCLK pin. It will be 1 to indicate high, 0 to indicate low. This allows software to read the current state of the pin.

7.3.15 Slave Status Register (SSTS)—Offset 10h

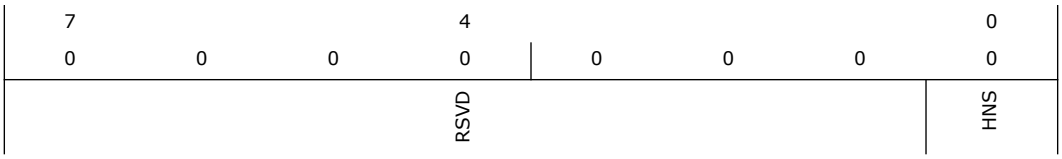
All bits in this register are implemented in the 64 kHz clock domain. Therefore, software must poll the register until a write takes effect before assuming that a write has completed internally.

Access Method

Type: IO Register
(Size: 8 bits)

Device: 31
Function: 4

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7:1	0h RO	Reserved.
0	0h RW/1C	**HOST_NOTIFY_STS (HNS):** The Intel PCH sets this bit to a 1 when it has completely received a successful Host Notify Command on the SMBus pins. Software reads this bit to determine that the source of the interrupt or SMI# was the reception of the Host Notify Command. Software clears this bit after reading any information needed from the Notify address and data registers by writing a 1 to this bit. Note that the Intel PCH will allow the Notify Address and Data registers to be over-written once this bit has been cleared. When this bit is 1, the Intel PCH will NACK the first byte (host address) of any new Host Notify commands on the SMBus. Writing a 0 to this bit has no effect.

7.3.16 Slave Command Register (SCMD)—Offset 11h

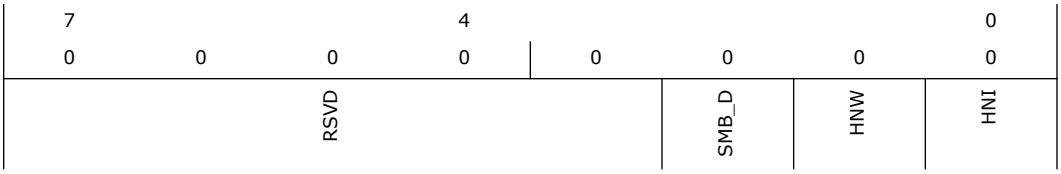
All bits in this register are implemented in the 64 kHz clock domain. Therefore, software must poll the register until a write takes effect before assuming that a write has completed internally. Also, software must confirm the prior written value before writing to the register again.

Access Method

Type: IO Register
(Size: 8 bits)

Device: 31
Function: 4

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7:3	0h RO	Reserved.
2	0h RW	**SMBALERT_DIS (SMB_D):** Software sets this bit to 1 to block the generation of the interrupt or SMI# due to the SMBALERT# source. This bit is logically inverted and ANDed with the SMBALERT_STS bit. The resulting signal is distributed to the SMI# and/or interrupt generation logic. This bit does not effect the wake logic.
1	0h RW	**HOST_NOTIFY_WKEN (HNW):** Software sets this bit to 1 to enable the reception of a Host Notify command as a wake event. When enabled this event is ORed in with the other SMBus wake events and is reflected in the SMB_WAK_STS bit of the General Purpose Event 0 Status register.
0	0h RW	**HOST_NOTIFY_INTREN (HNI):** Software sets this bit to 1 to enable the generation of interrupt or SMI# when HOST_NOTIFY_STS is 1. This enable does not affect the setting of the HOST_NOTIFY_STS bit. When the interrupt is generated, either PIRQB or SMI# is generated, depending on the value of the SMB_SMI_EN bit (D31, F3, Off40h, B1). If the HOST_NOTIFY_STS bit is set when this bit is written to a 1, then the interrupt (or SMI#) will be generated. The interrupt (or SMI#) is logically generated by ANDing the STS and INTREN bits.

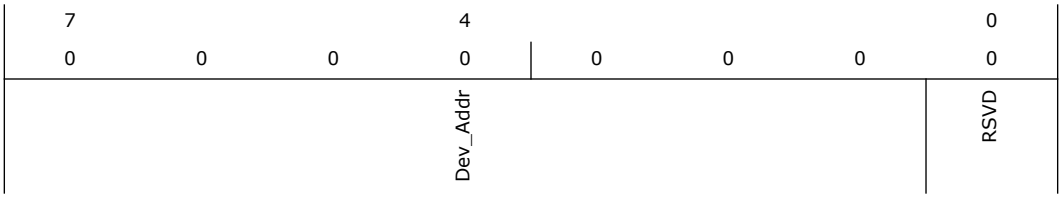
7.3.17 Notify Device Address Register (NDA)—Offset 14h

Access Method

Type: IO Register
(Size: 8 bits)

Device: 31
Function: 4

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7:1	0h RW	**DEVICE_ADDRESS (Dev_Addr):** This field contains the 7-bit device address received during the Host Notify protocol of the SMBus 2.0 specification. Software should only consider this field valid when the HOST_NOTIFY_STS bit is set to 1.
0	0h RO	Reserved.

7.3.18 Notify Data Low Byte Register (NDLB)—Offset 16h

Access Method

Type: IO Register
(Size: 8 bits)

Device: 31
Function: 4

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RO	**DATA_LOW_BYTE (DLB):** This field contains the first (low) byte of data received during the Host Notify protocol of the SMBus 2.0 specification. Software should only consider this field valid when the HOST_NOTIFY_STS bit is set to 1.

7.3.19 Notify Data High Byte Register (NDHB)—Offset 17h

Access Method

Type: IO Register
(Size: 8 bits)

Device: 31
Function: 4

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RO	**DATA_HIGH_BYTE (DHB):** This field contains the second (high) byte of data received during the Host Notify protocol of the SMBus 2.0 specification. Software should only consider this field valid when the HOST_NOTIFY_STS bit is set to 1.

7.4 SMBus PCR Registers Summary

These registers are within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID + Register Offset). The offsets are DWORD aligned byte addresses.

Table 7-3. Summary of SMBus PCR Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	TCO Configuration (TCOCFG)—Offset 0h	0h
Ch	Fh	General Control (GC)—Offset Ch	0h

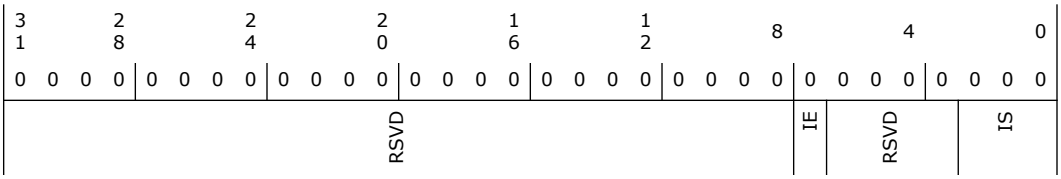
7.4.1 TCO Configuration (TCOCFG)—Offset 0h

Access Method

Type: MSG Register
(Size: 32 bits)

Device: 31
Function: 4

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**TCO IRQ Enable (IE):** When set, TCO IRQ is enabled, as selected by the TCO_IRQ_SEL field. When cleared, TCO IRQ is disabled.
6:3	0h RO	Reserved.
2:0	0h RW	**TCO IRQ Select (IS):** Specifies on which IRQ the TCO will internally appear. If not using the APIC, the TCO interrupt must be routed to IRQ9-11, and that interrupt is not sharable with the SERIRQ stream, but is shareable with other PCI interrupts. If using the APIC, the TCO interrupt can also be mapped to IRQ20-23, and can be shared with other interrupt. Bits TCO Map 000 IRQ9 (maps to 8259 and APIC) 001 IRQ10 maps to 8259 and APIC) 010 IRQ11 (maps to 8259 and APIC) 011 Reserved 100 IRQ20 (maps to APIC) 101 IRQ21 (maps to APIC) 110 IRQ22 (maps to APIC) 111 IRQ23 (maps to APIC) When setting the these bits, the IE bit should be cleared to prevent glitching. When the interrupt is mapped to APIC interrupts 9, 10 or 11, the APIC should be programmed for active-high reception. When the interrupt is mapped to APIC interrupts 20 through 23, the APIC should be programmed for active-low reception.

7.4.2 General Control (GC)—Offset Ch

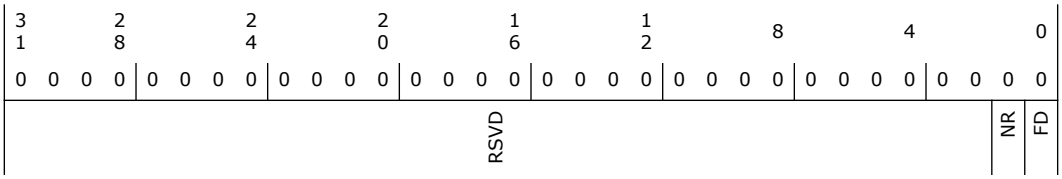
Access Method

Type: MSG Register (Size: 32 bits)

Device: 31

Function: 4

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1	0h RW	**No Reboot (NR):** This bit is set when the No Reboot strap is sampled high on PWROK. This bit may be set or cleared by software if the strap is sampled low but may not override the strap when it indicates No Reboot. When set, the TCO timer will count down and generate the SMI# on the first timeout, but will not reboot on the second timeout.
0	0h RW	**Function Disable (FD):** When set to one, this disables the PCI config register space for the SMBus device.

§ §

8 SPI Interface (D31:F5)

8.1 SPI Configuration Registers Summary

Table 8-1. Summary of SPI Configuration Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	Device ID and Vendor ID (BIOS_SPI_DID_VID)—Offset 0h	XXXX8086h
4h	7h	Status and Command (BIOS_SPI_STS_CMD)—Offset 4h	400h
8h	Bh	Revision ID (BIOS_SPI_CC_RID)—Offset 8h	See register
Ch	Fh	BIST, Header Type, Latency Timer, Cache Line Size (BIOS_SPI_BIST_HTYPE_LT_CLS)—Offset Ch	0h
10h	13h	SPI BAR0 MMIO (BIOS_SPI_BAR0)—Offset 10h	0h
D0h	D3h	SPI Unsupported Request Status (BIOS_SPI_UR_STS_CTL)—Offset D0h	0h
D8h	DBh	BIOS Decode Enable (BIOS_SPI_BDE)—Offset D8h	FFCFh
DCh	DFh	BIOS Control (BIOS_SPI_BC)—Offset DCh	28h

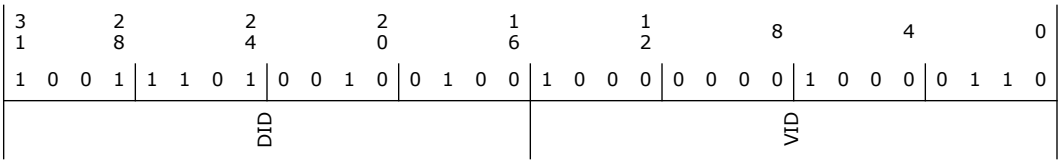
8.1.1 Device ID and Vendor ID (BIOS_SPI_DID_VID)—Offset 0h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 5

Default: XXXX8086h



Bit Range	Default & Access	Field Name (ID): Description
31:16	XXXXh RO/V	**Device Identification (DID):** Identifier for the SPI Flash Controller. See the Device and Version ID Table in Volume 1 for the default value.
15:0	8086h RO	**Vendor Identification (VID):** This field identifies the manufacturer of the device. 0x8086 indicates Intel

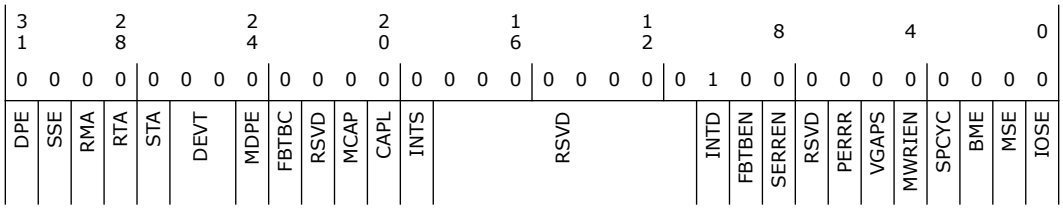
8.1.2 Status and Command (BIOS_SPI_STS_CMD)—Offset 4h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 5

Default: 400h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C/V	**Detected Parity Error (DPE):** Detected Parity Error (DPE)
30	0h RW/1C/V	**Signaled System Error (SSE):** Signaled System Error (SSE)
29	0h RO	**Received Master Abort (RMA):** Received Master Abort(RMA)
28	0h RO	**Received Target Abort (RTA):** Received Target Abort(RTA)
27	0h RW/1C/V	**Signaled Target Abort (STA):** Signaled Target Abort(STA)
26:25	0h RO	**Devsel Timing (DEVT):** Devsel Timing (DEVT)
24	0h RO	**Master Data Parity Error (MDPE):** Master Data Parity Error (MDPE)
23	0h RO	**Fast Back to Back Capable (FBTBC):** Fast Back to Back Capable (FBTBC)
22	0h RO	Reserved.
21	0h RO	**66 MHz Capable (MCAP):** Not 66MHz Capable Device
20	0h RO	**Capabilities List (CAPL):** Capabilities List
19	0h RO	**Interrupt Status (INTS):** Interrupt Status
18:11	0h RO	Reserved.
10	1h RO	**Interrupt Disable (INTD):** Interrupt Disable
9	0h RO	**Fast Back to Back Enable (FBTBEN):** Fast Back to Back Enable
8	0h RW	**System Error Enable (SERREN):** System Error Enable
7	0h RO	Reserved.
6	0h RW	**Parity Error Response (PERRR):** Parity Error Response
5	0h RO	**VGA Palette Snoop (VGAPS):** VGA Palette Snoop

Bit Range	Default & Access	Field Name (ID): Description
4	0h RO	**Memory Write and Invalidate Enable (MWRIEN):** Memory Write and Invalidate Enable.
3	0h RO	**Special Cycles (SPCYC):** Special Cycles
2	0h RW	**Bus Master Enable (BME):** Bus Master Enable
1	0h RW	**Memory Space Enable (MSE):** Memory Space Enable
0	0h RO	**IO Space Enable (IOSE):** IO Space Enable

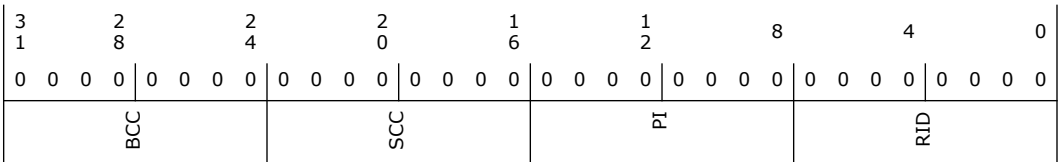
8.1.3 Revision ID (BIOS_SPI_CC_RID)—Offset 8h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 5

Default: See register



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Base Class Code (BCC):** Base Class Code
23:16	0h RO	**Sub-Class Code (SCC):** Sub-Class Code
15:8	0h RO	**Programming Interface (PI):** Programming Interface
7:0	-- RO/V	**Revision ID (RID):** Indicates the part revision. See the Device and Version ID Table in Volume 1 for the default value.

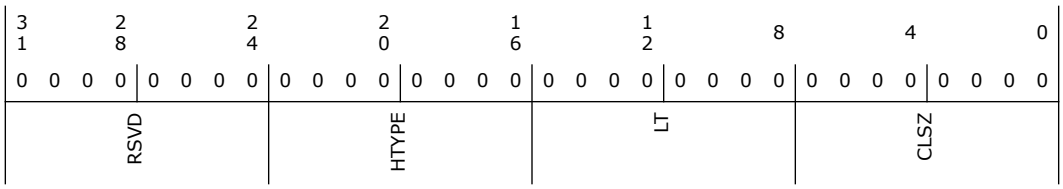
8.1.4 BIST, Header Type, Latency Timer, Cache Line Size (BIOS_SPI_BIST_HTYPE_LT_CLS)—Offset Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 5

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:16	0h RO	**Header Type (HTYPE):** Header Type
15:8	0h RO	**Latency Timer (LT):** Latency Timer
7:0	0h RO	**Cacheline Size (CLSZ):** Cacheline Size

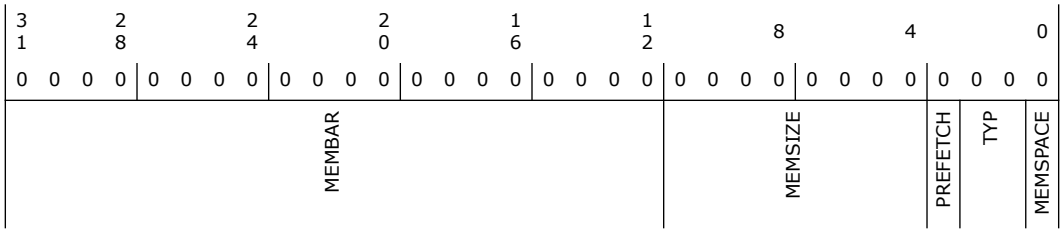
8.1.5 SPI BAR0 MMIO (BIOS_SPI_BAR0)—Offset 10h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 5

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW	**Memory BAR (MEMBAR):** Software programs this register with the base address of the device's memory region. The Host/BIOS MMIO registers in the flash controller are offset from this BAR.
11:4	0h RO	**Memory Size (MEMSIZE):** Hardwired to 0 to indicate 4KB of memory space
3	0h RO	**Prefetchable (PREFETCH):** A device can mark a range as prefetchable if there are no side effects on reads, the device returns all bytes on reads regardless of the byte enables. Hardwired to 1 to indicate the device's memory space as prefetchable.
2:1	0h RO	**Type (TYP):** Hardwired to 0 to indicate that Base register is 32 bits wide and mapping can be done anywhere in the 32-bit Memory Space.
0	0h RO	**Memory Space Indicator (MEMSPACE):** Hardwired to 0 to identify a Memory BAR.

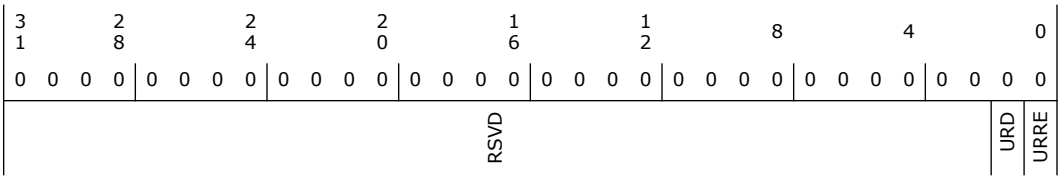
8.1.6 SPI Unsupported Request Status (BIOS_SPI_UR_STS_CTL)—Offset D0h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 5

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1	0h RW/1C/V	**Unsupported Request Detected (URD):** Set to 1 by hardware upon detecting an Unspported Request that is not considered an Advisory Non-Fatal error. Cleared to 0 when software writes a 1 to this register.
0	0h RW	**Unsupported Request Reporting Enabled (URRE):** If set to 1 by software, the flash controller generates a DoSERR sideband message when the URD bit transitions from 0 to 1.

8.1.7 BIOS Decode Enable (BIOS_SPI_BDE)—Offset D8h

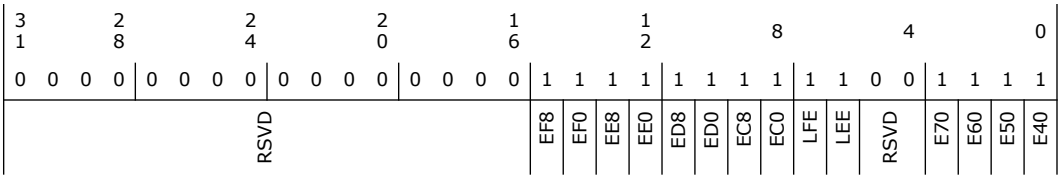
This register only effects BIOS decode if BIOS is resident on SPI.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 5

Default: FFCFh



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	1h RO	**F8-FF Enable (EF8):** F8-FF Enable (EF8): Enables decoding of 512K of the following BIOS range: Data space: FFF80000h - FFFFFFFFh
14	1h RW	**F0-F8 Enable (EF0):** F0-F8 Enable (EF0): Enables decoding of 512K of the following BIOS range: Data space: FFF00000h - FFF7FFFFh
13	1h RW	**E8-EF Enable (EE8):** E8-EF Enable (EE8): Enables decoding of 512K of the following BIOS range: Data space: FFE80000h - FFEFFFFFh
12	1h RW	**E0-E8 Enable (EE0):** E0-E8 Enable (EE0): Enables decoding of 512K of the following BIOS range: Data space: FFE00000h - FFE7FFFFh
11	1h RW	**D8-DF Enable (ED8):** D8-DF Enable (ED8): Enables decoding of 512K of the following BIOS range: Data space: FFD80000h - FFDFFFFFh
10	1h RW	**D0-D7 Enable (ED0):** D0-D7 Enable (ED0): Enables decoding of 512K of the following BIOS range: Data space: FFD00000h - FFD7FFFFh
9	1h RW	**C8-CF Enable (EC8):** C8-CF Enable (EC8): Enables decoding of 512K of the following BIOS range: Data space: FFC80000h - FFCFFFFFh
8	1h RW	**C0-C7 Enable (EC0):** C0-C7 Enable (EC0): Enables decoding of 512K of the following BIOS range: Data space: FFC00000h - FFC7FFFFh
7	1h RW	**Legacy F Segment Enable (LFE):** Legacy F Segment Enable (LFE): This enables the decoding of the legacy 64KB range at F0000h - FFFFFh
6	1h RW	**Legacy E Segment Enable (LEE):** Legacy E Segment Enable (LFE): This enables the decoding of the legacy 64KB range at E0000h - EFFFFh
5:4	0h RO	Reserved.
3	1h RW	**70-7F Enable (E70):** 70-7F Enable (E70): Enables decoding of 1MB of the following BIOS range: Data space: FF700000h - FF7FFFFFh
2	1h RW	**60-6F Enable (E60):** 60-6F Enable (E60): Enables decoding of 1MB of the following BIOS range: Data space: FF600000h - FF6FFFFFh
1	1h RW	**50-5F Enable (E50):** 50-5F Enable (E50): Enables decoding of 1MB of the following BIOS range: Data space: FF500000h - FF5FFFFFh
0	1h RW	**40-4F Enable (E40):** 40-4F Enable (E40): Enables decoding of 1MB of the following BIOS range: Data space: FF400000h - FF4FFFFFh

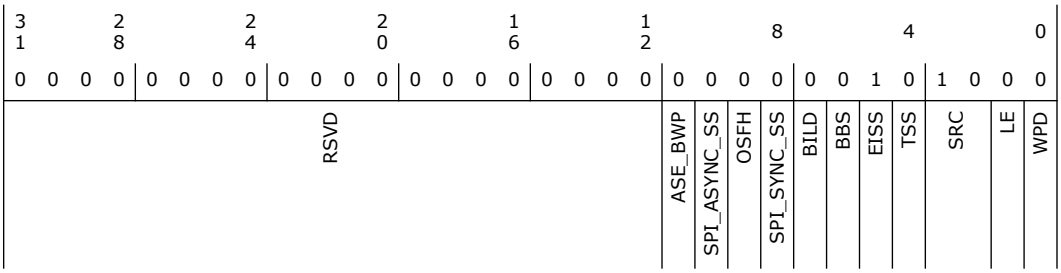
8.1.8 BIOS Control (BIOS_SPI_BC)—Offset DCh

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 5

Default: 28h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	Reserved.
11	0h RW/L	**Async SMI Enable for BIOS Write Protection (ASE_BWP):** When set to '1' the flash controller will generate an SMI when it blocks a BIOS write or erase due to WPD = 0. The value in this field can be written by software as long as the BIOS Interface Lock-Down (BILD) is not set.
10	0h RO/V	**Asynchronous SMI Status (SPI_ASYNC_SS):** Status indication that the SPI Flash Controller has asserted an asynchronous SMI. Hardware clears the bit when it sends the De-assert SMI message. 0 : default state 1 : SPI flash controller asserted asynchronous SMI
9	0h RO	**OS Function Hide (OSFH):** This bit controls read access to SPI's Device ID, Vendor ID PCI Config register. This bit does not affect access to any other PCI Config registers. This bit is locked with BILD. Trusted BIOS must set this bit prior to starting the OS. 0 : DeviceID, VendorID can be read 1 : reads to Device ID, Vendor ID return invalid data
8	0h RO/V	**Synchronous SMI Status (SPI_SYNC_SS):** Status indication that the SPI Flash Controller has asserted a synchronous SMI. Hardware clears the bit when it sends the De-assert Synchronous SMI message. 0 : default state 1 : SPI flash controller asserted Synchronous SMI
7	0h RW/L	**BIOS Interface Lock-Down (BILD):** When set, prevents TS and BBS from being changed. This bit can only be written from 0 to 1 once.
6	0h RW/V/L	**Boot BIOS Strap (BBS):** This field determines the destination of accesses to the BIOS memory range. 0 = SPI 1 = LPC When SPI or LPC is selected, the range that is decoded is further qualified by BIOS Decode Enable. The value in this field can be overwritten by software as long as the BIOS Interface Lock-Down (BILD) is not set
5	1h RW/L	**Enable InSMM.STS (EISS):** When this bit is set, the BIOS region is not writable until the CPU sets the InSMM.STS bit. If this bit [5] is set, then WPD must be a '1' and InSMM.STS(0xFED3_0880[0]) must be '1' also in order to write to BIOS region of SPI Flash. If this bit [5] is clear, then the InSMM.STS is a don't care. This bit is locked by LE
4	0h RO/V	**Top Swap Status (TSS):** This bit provides a read-only path to view the state of the Top Swap bit. It is duplicated here to be consistent with the LPC version of the BC register.

Bit Range	Default & Access	Field Name (ID): Description
3:2	2h RW	**SPI Read Configuration (SRC):** These bits are located in PCI Config space to allow them to be set early in the boot flow. This 2-bit field controls two policies related to BIOS reads on the SPI interface: Bit 3- Prefetch Enable Bit 2- Cache Disable Settings are summarized below: 00 = No prefetching, but caching enabled. Direct Memory reads load the read buffer cache with valid data, allowing repeated reads to the same range to complete quickly 01 = No prefetching and no caching. One-to-one correspondence of host BIOS reads to SPI cycles. This value can be used to invalidate the cache. 10 = Prefetching and Caching enabled. This mode is used for long sequences of short reads to consecutive addresses (i.e. shadowing) 11 = Illegal. Caching must be enabled when Prefetching is enabled.
1	0h RW/L	**Lock Enable (LE):** When set, setting the WPD bit will cause SMI. When cleared, setting the WPD bit will not cause SMI. Once set, this bit can only be cleared by a PLTRST#. When this bit is set, EISS - bit [5] of this register is locked down.
0	0h RW	**Write Protect Disable (WPD):** When set, access to the BIOS space is enabled for both read and write cycles to BIOS. When cleared, only read cycles are permitted to the FWH or SPI flash. When this bit is written from a '0' to a '1' and the LE bit is also set, an SMI# is generated. This ensures that only SMM code can update BIOS.

8.2 SPI Memory Mapped Registers Summary

The SPI memory mapped registers are accessed based upon offsets from SPI_BAR0 (in PCI config SPI_BAR0 register).

Table 8-2. Summary of SPI Memory Mapped Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	SPI BIOS MMIO PRI (BIOS_BFPREG)—Offset 0h	0h
4h	7h	Hardware Sequencing Flash Status and Control (BIOS_HSFSTS_CTL)—Offset 4h	2000h
8h	Bh	Flash Address (BIOS_FADDR)—Offset 8h	0h
Ch	Fh	Discrete Lock Bits (BIOS_DLOCK)—Offset Ch	0h
10h	13h	Flash Data 0 (BIOS_FDATA0)—Offset 10h	0h
14h	17h	Flash Data 1 (BIOS_FDATA1)—Offset 14h	0h
18h	1Bh	Flash Data 2 (BIOS_FDATA2)—Offset 18h	0h
1Ch	1Fh	Flash Data 3 (BIOS_FDATA3)—Offset 1Ch	0h
20h	23h	Flash Data 4 (BIOS_FDATA4)—Offset 20h	0h
24h	27h	Flash Data 5 (BIOS_FDATA5)—Offset 24h	0h
28h	2Bh	Flash Data 6 (BIOS_FDATA6)—Offset 28h	0h
2Ch	2Fh	Flash Data 7 (BIOS_FDATA7)—Offset 2Ch	0h
30h	33h	Flash Data 8 (BIOS_FDATA8)—Offset 30h	0h
34h	37h	Flash Data 9 (BIOS_FDATA9)—Offset 34h	0h
38h	3Bh	Flash Data 10 (BIOS_FDATA10)—Offset 38h	0h
3Ch	3Fh	Flash Data 11 (BIOS_FDATA11)—Offset 3Ch	0h
40h	43h	Flash Data 12 (BIOS_FDATA12)—Offset 40h	0h
44h	47h	Flash Data 13 (BIOS_FDATA13)—Offset 44h	0h
48h	4Bh	Flash Data 14 (BIOS_FDATA14)—Offset 48h	0h
4Ch	4Fh	Flash Data 15 (BIOS_FDATA15)—Offset 4Ch	0h

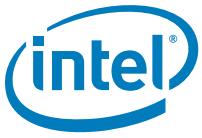


Table 8-2. Summary of SPI Memory Mapped Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
50h	53h	Flash Region Access Permissions (BIOS_FRACC)—Offset 50h	42C2h
54h	57h	Flash Region 0 (BIOS_FREG0)—Offset 54h	7FFFh
58h	5Bh	Flash Region 1 (BIOS_FREG1)—Offset 58h	7FFFh
5Ch	5Fh	Flash Region 2 (BIOS_FREG2)—Offset 5Ch	7FFFh
60h	63h	Flash Region 3 (BIOS_FREG3)—Offset 60h	7FFFh
64h	67h	Flash Region 4 (BIOS_FREG4)—Offset 64h	7FFFh
68h	6Bh	Flash Region 5 (BIOS_FREG5)—Offset 68h	7FFFh
84h	87h	Flash Protected Range 0 (BIOS_FPR0)—Offset 84h	0h
88h	8Bh	Flash Protected Range 1 (BIOS_FPR1)—Offset 88h	0h
8Ch	8Fh	Flash Protected Range 2 (BIOS_FPR2)—Offset 8Ch	0h
90h	93h	Flash Protected Range 3 (BIOS_FPR3)—Offset 90h	0h
94h	97h	Flash Protected Range 4 (BIOS_FPR4)—Offset 94h	0h
98h	9Bh	Global Protected Range 0 (BIOS_GPR0)—Offset 98h	0h
B0h	B3h	Secondary Flash Region Access Permissions (BIOS_SFRACC)—Offset B0h	0h
B4h	B7h	Flash Descriptor Observability Control (BIOS_FDOC)—Offset B4h	0h
B8h	BBh	Flash Descriptor Observability Data (BIOS_FDOD)—Offset B8h	0h
C0h	C3h	Additional Flash Control (BIOS_AFC)—Offset C0h	0h
C4h	C7h	Vendor Specific Component Capabilities for Component 0 (BIOS_SFDP0_VSCC0)—Offset C4h	2000h
C8h	CBh	Vendor Specific Component Capabilities for Component 1 (BIOS_SFDP1_VSCC1)—Offset C8h	2000h
CCh	CFh	Parameter Table Index (BIOS_PTINX)—Offset CCh	0h
D0h	D3h	Parameter Table Data (BIOS_PTDATA)—Offset D0h	0h
D4h	D7h	SPI Bus Requester Status (BIOS_SBRS)—Offset D4h	0h

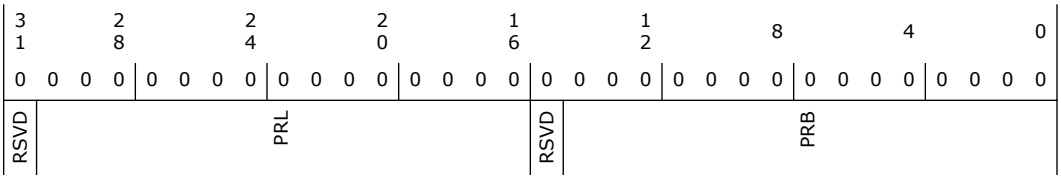
8.2.1 SPI BIOS MMIO PRI (BIOS_BFPREG)—Offset 0h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 5

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	Reserved.
30:16	0h RO/V	**BIOS Flash Primary Region Limit (PRL):** This specifies address bits 26:12 for the Primary Region Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG1.Region Limit, or the Flash Descriptor.FLREG6.Region Limit depending on the BFPREG.SBRS bit.
15	0h RO	Reserved.
14:0	0h RO/V	**BIOS Flash Primary Region Base (PRB):** This specifies address bits 26:12 for the Primary Region Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREG1.Region Base, or the Flash Descriptor.FLREG6.Region Base depending on the BFPREG.SBRS bit.

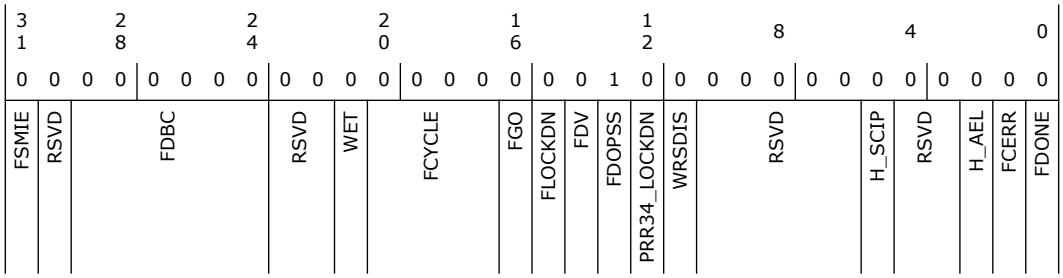
8.2.2 Hardware Sequencing Flash Status and Control (BIOS_HSFSTS_CTL)—Offset 4h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 5

Default: 2000h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Flash SPI SMI# Enable (FSMIE):** When set to 1, the SPI asserts an SMI# request whenever the Flash Cycle Done bit is 1.
30	0h RO	Reserved.
29:24	0h RW	**Flash Data Byte Count (FDBC):** This field specifies the number of bytes to shift in or out during the data portion of the SPI cycle. The contents of this register are 0s based with 0b representing 1 byte and 3Fh representing 64 bytes. The number of bytes transferred is the value of this field plus 1. This field is ignored for the Block Erase command.
23:22	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RW	**Write Enable Type (WET):** 0: Use 06h as the write enable instruction 1: Use 50h as the write enable instruction. Note that this setting is not supported as no supported flash devices require the 50h opcode to enable a non-volatile status register write.
20:17	0h RW	**FLASH Cycle (FCYCLE):** This field defines the Flash SPI cycle type generated to the FLASH when the FGO bit is set as defined below: 0 Read (1 up to 64 bytes by setting FDBC) 1 Reserved 2 Write (1 up to 64 bytes by setting FDBC) 3 4k Block Erase 4 64k Sector erase 5 Read SFDP 6 Read JEDEC ID 7 write status 8 read status 9 RPMC Op1 A RPMC Op2 Flash controller hardware automatically inserts a write enable opcode prior to Write and erase operations. Hardware automatically polls for device not-busy using read status after write and erase operations. If the device does not support 64k erase size (or if it doesn't support SFDP) then only 4k is allowed. Note: if reserved 1 is programmed to this field, flash controller will handle it as if it is 0 (Read)
16	0h RW/1S/V	**Flash Cycle Go (FGO):** A write to this register with a 1 in this bit initiates a request to the Flash SPI Arbiter to start a cycle. This register is cleared by hardware when the cycle is granted by the SPI arbiter to run the cycle on the SPI bus. When the cycle is complete, the FDONE bit is set. Software is forbidden to write to any register in the HSFLCTL register between the FGO bit getting set and the FDONE bit being cleared. Any attempt to violate this rule will be ignored by hardware. Hardware allows other bits in this register to be programmed for the same transaction when writing this bit to 1. This saves an additional memory write. This bit always returns 0 on reads.
15	0h RW/L	**Flash Configuration Lock-Down (FLOCKDN):** When set to 1, those Flash Program Registers that are locked down by this FLOCKDN bit cannot be written. Once set to 1, this bit can only be cleared by a hardware reset.
14	0h RO/V	**Flash Descriptor Valid (FDV):** This bit is set to a 1 if the Flash Controller read the correct Flash Descriptor Signature. If the Flash Descriptor Valid bit is not 1 , software cannot use the Hardware Sequencing registers, but must use the software sequencing registers. Any attempt to use the Hardware Sequencing registers will result in the FCERR bit being set
13	1h RO/V	**Flash Descriptor Override Pin-Strap Status (FDOPSS):** This register reflects the value the Flash Descriptor Override Pin-Strap. '1': No override '0': The Flash Descriptor Override strap is set
12	0h RW/L	**PRR3 PRR4 Lock-Down (PRR34_LOCKDN):** When set to 1, the BIOS PRR3 and PRR4 registers cannot be written. Once set to 1, this bit can only be cleared by a hardware reset.
11	0h RW/L	**Flash Configuration Lock-Down (WRSDIS):** 0 = Write status operation may be issued using Hardware Sequencing. 1 = Write status is not allowed as a Hardware Sequencing operation. The flash controller will block the operation and set the FCERR bit when software sets the 'go' bit. This bit is locked when FLOCKDN is set.
10:6	0h RO	Reserved.
5	0h RO/V	**SPI Cycle In Progress (H_SCIP):** Hardware sets this bit when software sets the Flash Cycle Go (FGO) bit in the Hardware Sequencing Flash Control register. This bit remains set until the cycle completes on the SPI interface. Hardware automatically sets and clears this bit so that software can determine when read data is valid and/or when it is safe to begin programming the next command. Software must only program the next command when this bit is 0.
4:3	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1C/V	**Access Error Log (H_AEL):** Hardware sets this bit to a 1 when an attempt was made to access the BIOS region using the direct access method or an access to the BIOS Program Registers that violated the security restrictions. This bit is simply a log of an access security violation. This bit is cleared by software writing a '1'.
1	0h RW/1C/V	**Flash Cycle Error (FCERR):** Hardware sets this bit to 1 when a program register access is blocked to the FLASH due to one of the protection policies or when any of the programmed cycle registers is written while a programmed access is already in progress. This bit remains asserted until cleared by software writing a 1 or until hardware reset occurs. Software must clear this bit before setting the FLASH Cycle GO bit in this register.
0	0h RW/1C/V	**Flash Cycle Done (FDONE):** The PCH sets this bit to 1 when the SPI Cycle completes after software previously set the FGO bit. This bit remains asserted until cleared by software writing a 1 or hardware reset. When this bit is set and the SPI SMI# Enable bit is set, an internal signal is asserted to the SMI# generation block. Software must make sure this bit is cleared prior to enabling the SPI SMI# assertion for a new programmed access.

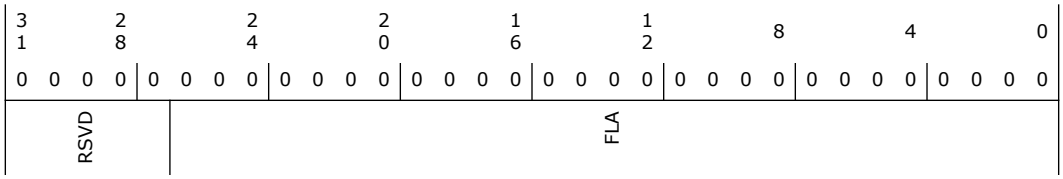
8.2.3 Flash Address (BIOS_FADDR)—Offset 8h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 5

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	Reserved.
26:0	0h RW	**Flash Linear Address (FLA):** The FLA is the starting byte linear address of a SPI Read or Write cycle or an address within a Block for the Block Erase command. The Flash Linear Address must fall within a region for which BIOS has access permissions. Hardware must convert the FLA into a Flash Physical Address (FPA) before running this cycle on the SPI bus.

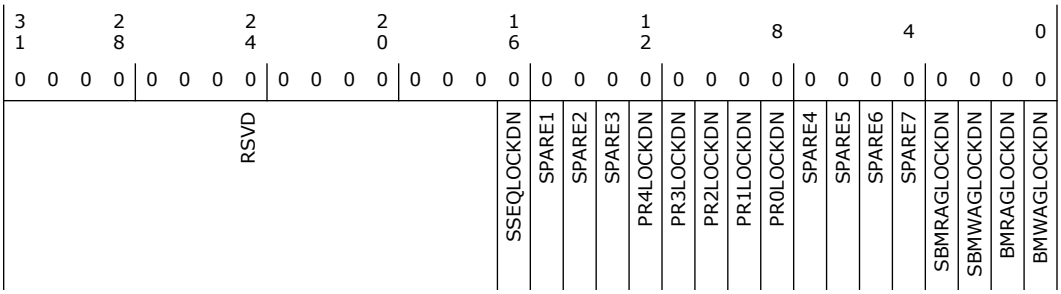
8.2.4 Discrete Lock Bits (BIOS_DLOCK)—Offset Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 5

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	Reserved.
16	0h RW/L	**SSEQ Lock-Down (SSEQLOCKDN)**
15	0h RW/L	**Spare1 (SPARE1)**
14	0h RW/L	**Spare2 (SPARE2)**
13	0h RW/L	**Spare3 (SPARE3)**
12	0h RW/L	**PR4 Lock-Down (PR4LOCKDN)**
11	0h RW/L	**PR3 Lock-Down (PR3LOCKDN)**
10	0h RW/L	**PR2 Lock-Down (PR2LOCKDN)**
9	0h RW/L	**PR1 Lock-Down (PR1LOCKDN)**
8	0h RW/L	**PR0 Lock-Down (PR0LOCKDN)**
7	0h RW/L	**Spare4 (SPARE4)**
6	0h RW/L	**Spare5 (SPARE5)**
5	0h RW/L	**Spare6 (SPARE6)**
4	0h RW/L	**Spare7 (SPARE7)**
3	0h RW/L	**SBMRAG Lock-Down (SBMRAGLOCKDN)**
2	0h RW/L	**SBMWAG Lock-Down (SBMWAGLOCKDN)**
1	0h RW/L	**BMRAG Lock-Down (BMRAGLOCKDN)**
0	0h RW/L	**BMWAG Lock-Down (BMWAGLOCKDN)**

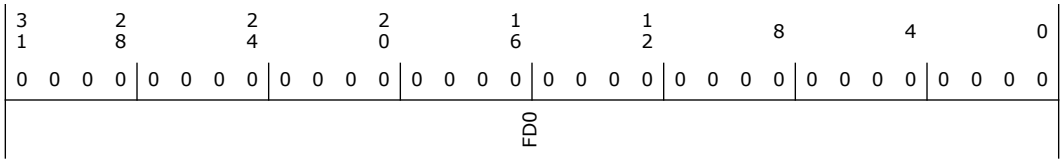
8.2.5 Flash Data 0 (BIOS_FDATA0)—Offset 10h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 5

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Flash Data 0 (FD0):** This field is shifted out as the SPI Data on the Master-Out Slave-In Data pin during the data portion of the SPI cycle. This register also shifts in the data from the Master-In Slave-Out pin into this register during the data portion of the SPI cycle. The data is always shifted starting with the least significant byte, msb to lsb, followed by the next least significant byte, msb to lsb, etc. Specifically, the shift order on SPI in terms of bits within this register is: 7-6-5-4-3-2-1-0-15-14-13-...8-23-22-...16-31...24. Bit 24 is the last bit shifted out/in. There are no alignment assumptions; byte 0 always represents the value specified by the cycle address. Note that the data in this register may be modified by the hardware during any programmed SPI transaction. Direct Memory Reads do not modify the contents of this register.

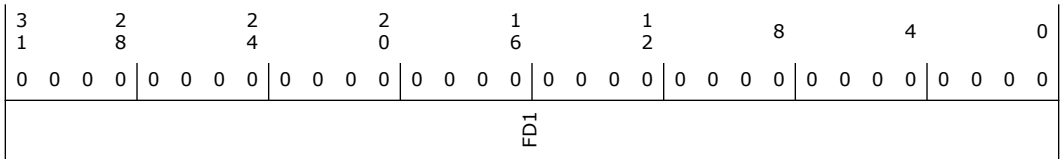
8.2.6 Flash Data 1 (BIOS_FDATA1)—Offset 14h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 5

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Flash Data 1 (FD1):** Flash Data 1 (FD1): Similar definition as Flash Data 0. However, this register does not begin shifting until FD0 has completely shifted in/out.

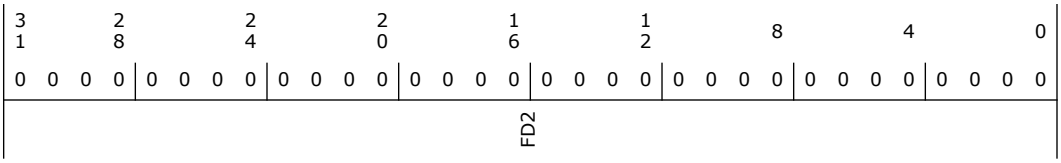
8.2.7 Flash Data 2 (BIOS_FDATA2)—Offset 18h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 5

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Flash Data 2 (FD2):** Flash Data 2 (FD2): Similar definition as Flash Data 0. However, this register does not begin shifting until FD1 has completely shifted in/out.

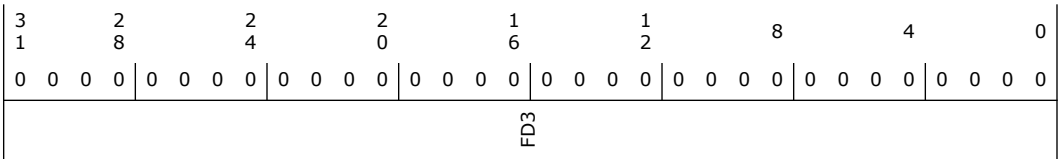
8.2.8 Flash Data 3 (BIOS_FDATA3)—Offset 1Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 5

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Flash Data 3 (FD3):** Flash Data 3 (FD3): Similar definition as Flash Data 0. However, this register does not begin shifting until FD2 has completely shifted in/out.

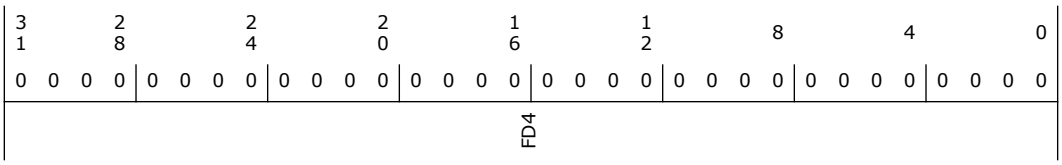
8.2.9 Flash Data 4 (BIOS_FDATA4)—Offset 20h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 5

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Flash Data 4 (FD4):** Flash Data 4 (FD4): Similar definition as Flash Data 0. However, this register does not begin shifting until FD3 has completely shifted in/out.

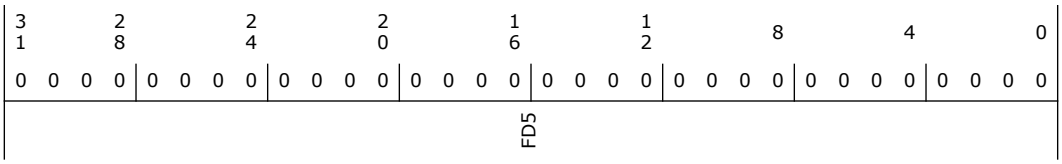
8.2.10 Flash Data 5 (BIOS_FDATA5)—Offset 24h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 5

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Flash Data 5 (FD5):** Flash Data 5 (FD5): Similar definition as Flash Data 0. However, this register does not begin shifting until FD4 has completely shifted in/out.

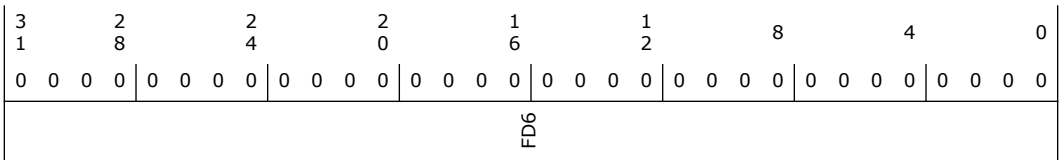
8.2.11 Flash Data 6 (BIOS_FDATA6)—Offset 28h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 5

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Flash Data 6 (FD6):** Flash Data 6 (FD6): Similar definition as Flash Data 0. However, this register does not begin shifting until FD5 has completely shifted in/out.

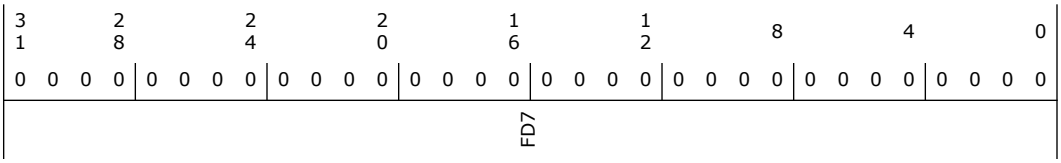
8.2.12 Flash Data 7 (BIOS_FDATA7)—Offset 2Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 5

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Flash Data 7 (FD7):** Flash Data 7 (FD7): Similar definition as Flash Data 0. However, this register does not begin shifting until FD6 has completely shifted in/out.

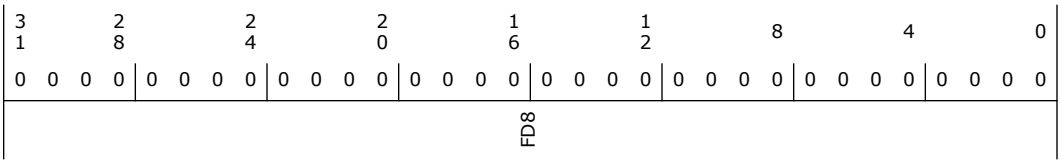
8.2.13 Flash Data 8 (BIOS_FDATA8)—Offset 30h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 5

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Flash Data 8 (FD8):** Flash Data 8 (FD8): Similar definition as Flash Data 0. However, this register does not begin shifting until FD7 has completely shifted in/out.

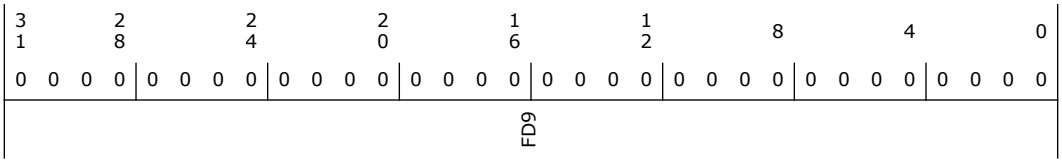
8.2.14 Flash Data 9 (BIOS_FDATA9)—Offset 34h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 5

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Flash Data 9 (FD9):** Flash Data 9 (FD9): Similar definition as Flash Data 0. However, this register does not begin shifting until FD8 has completely shifted in/out.

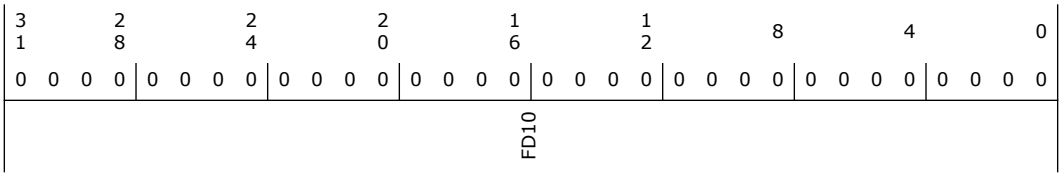
8.2.15 Flash Data 10 (BIOS_FDATA10)—Offset 38h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 5

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Flash Data 10 (FD10):** Flash Data 10 (FD10): Similar definition as Flash Data 0. However, this register does not begin shifting until FD9 has completely shifted in/out.

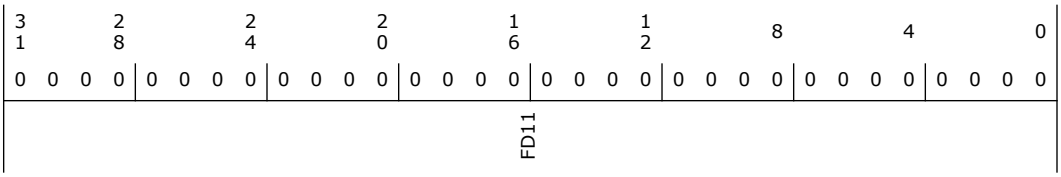
8.2.16 Flash Data 11 (BIOS_FDATA11)—Offset 3Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 5

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Flash Data 11 (FD11):** Flash Data 11 (FD11): Similar definition as Flash Data 0. However, this register does not begin shifting until FD10 has completely shifted in/out.

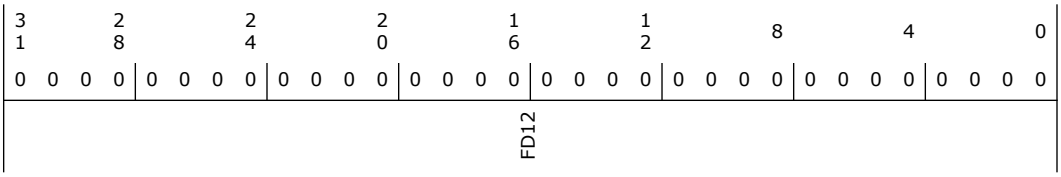
8.2.17 Flash Data 12 (BIOS_FDATA12)—Offset 40h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 5

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Flash Data 12 (FD12):** Flash Data 12 (FD12): Similar definition as Flash Data 0. However, this register does not begin shifting until FD11 has completely shifted in/out.

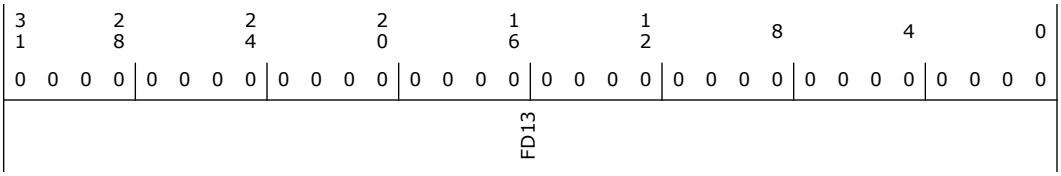
8.2.18 Flash Data 13 (BIOS_FDATA13)—Offset 44h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 5

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Flash Data 13 (FD13):** Flash Data 13 (FD13): Similar definition as Flash Data 0. However, this register does not begin shifting until FD12 has completely shifted in/out.

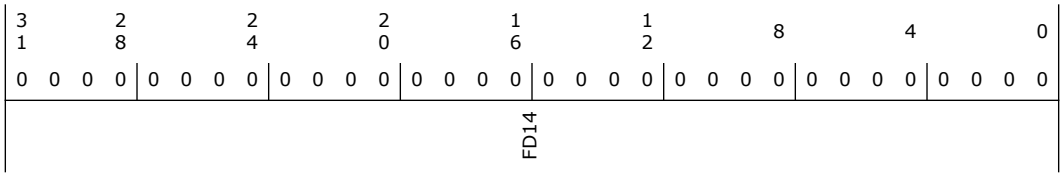
8.2.19 Flash Data 14 (BIOS_FDATA14)—Offset 48h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 5

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Flash Data 14 (FD14):** Flash Data 14 (FD14): Similar definition as Flash Data 0. However, this register does not begin shifting until FD13 has completely shifted in/out.

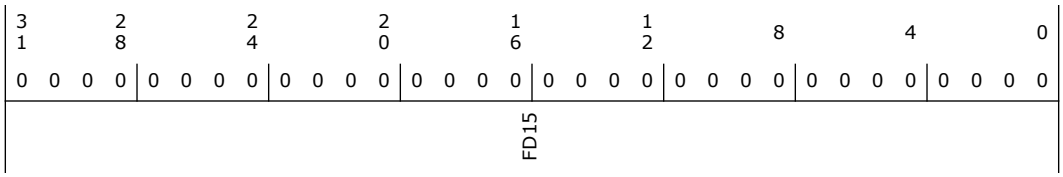
8.2.20 Flash Data 15 (BIOS_FDATA15)—Offset 4Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 5

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Flash Data 15 (FD15):** Flash Data 15 (FD15): Similar definition as Flash Data 0. However, this register does not begin shifting until FD14 has completely shifted in/out.

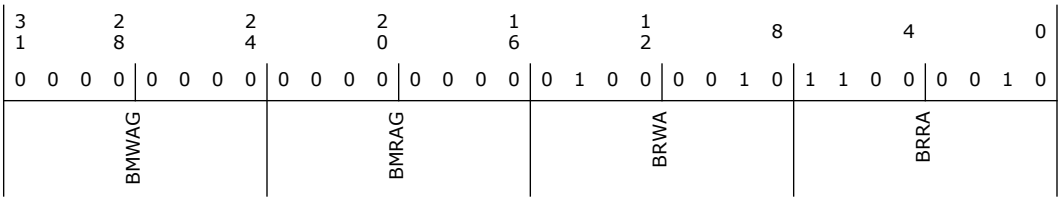
8.2.21 Flash Region Access Permissions (BIOS_FRACC)—Offset 50h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 5

Default: 42C2h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW/L	**BIOS Master Write Access Grant (BMWAG):** BIOS Master Write Access Grant (BMWAG): Each bit [31:24] corresponds to Master[7:0]. BIOS can grant one or more masters write access to the BIOS region 1 overriding the permissions in the Flash Descriptor. The contents of this register are locked by the FLOCKDN bit.
23:16	0h RW/L	**BIOS Master Read Access Grant (BMRAG):** BIOS Master Read Access Grant (BMRAG): Each bit [23:16] corresponds to Master[7:0]. BIOS can grant one or more masters read access to the BIOS region 1 overriding the read permissions in the Flash Descriptor. The contents of this register are locked by the FLOCKDN bit
15:8	42h RO/V	**BIOS Region Write Access (BRWA):** BIOS Region Write Access (BRWA): Each bit [15:8] corresponds to Regions [7:0]. If the bit is set, this master can erase and write that particular region through register accesses. The contents of this register are that of the Flash Descriptor.Flash Master 1.Master Region Write Access OR a particular master has granted BIOS write permissions in their Master Write Access Grant register OR the Flash Descriptor Security Override strap is set. BIOS always have the write access to its own Region 1 and Region 6 by default.
7:0	C2h RO/V	**BIOS Region Read Access (BRRA):** BIOS Region Read Access (BRRA): Each bit [7:0] corresponds to Regions [7:0]. If the bit is set, this master can read that particular region through register accesses. The contents of this register are that of the Flash Descriptor.Flash Master 1.Master Region Write Access OR a particular master has granted BIOS read permissions in their Master Read Access Grant register OR the Flash Descriptor Security Override strap is set. BIOS always have the read access to its own Region 1 and Region 6 by default.

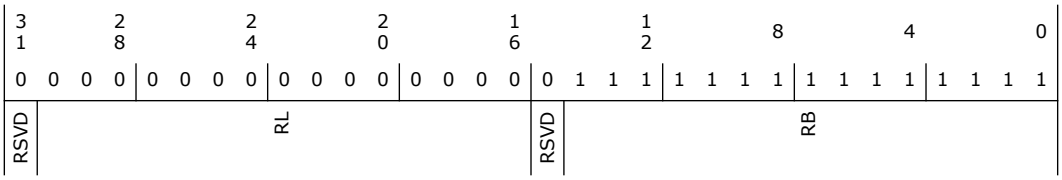
8.2.22 Flash Region 0 (BIOS_FREG0)—Offset 54h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 5

Default: 7FFFh



Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	Reserved.
30:16	0h RO/V	**Region Limit (RL):** Region Limit (RL) : This specifies address bits 26:12 for the Region 0 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG0.Region Limit
15	0h RO	Reserved.
14:0	7FFFh RO/V	**Region Base (RB):** Region Base (RB) : This specifies address bits 26:12 for the Region 0 Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREG0.Region Base

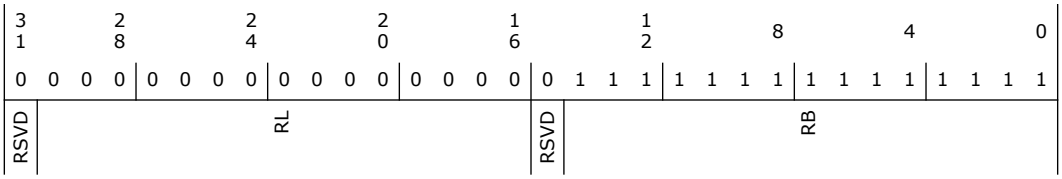
8.2.23 Flash Region 1 (BIOS_FREG1)—Offset 58h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 5

Default: 7FFFh



Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	Reserved.
30:16	0h RO/V	**Region Limit (RL):** Region Limit (RL) :This specifies address bits 26:12 for the Region 1 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG1.Region Limit
15	0h RO	Reserved.
14:0	7FFFh RO/V	**Region Base (RB):** Region Base (RB) : This specifies address bits 26:12 for the Region 1 Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREG1.Region Base

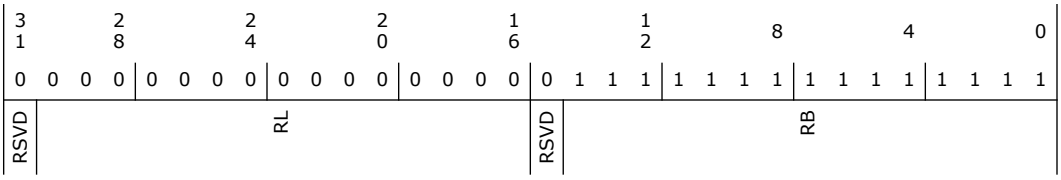
8.2.24 Flash Region 2 (BIOS_FREG2)—Offset 5Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 5

Default: 7FFFh



Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	Reserved.
30:16	0h RO/V	**Region Limit (RL):** Region Limit (RL): This specifies address bits 26:12 for the Region 2 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG2.Region Limit
15	0h RO	Reserved.
14:0	7FFFh RO/V	**Region Base (RB):** Region Base (RB) : This specifies address bits 26:12 for the Region 2 Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREG2.Region Base

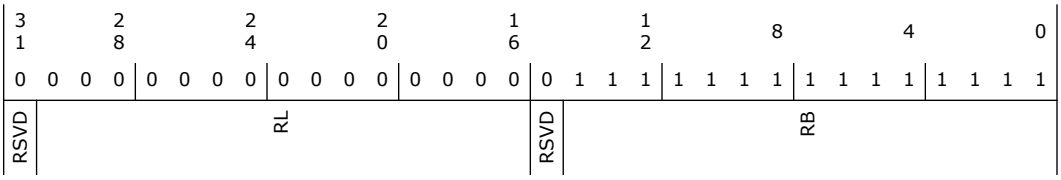
8.2.25 Flash Region 3 (BIOS_FREG3)—Offset 60h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 5

Default: 7FFFh



Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	Reserved.
30:16	0h RO/V	**Region Limit (RL):** Region Limit (RL): This specifies address bits 26:12 for the Region 3 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG3.Region Limit
15	0h RO	Reserved.
14:0	7FFFh RO/V	**Region Base (RB):** Region Base (RB) : This specifies address bits 26:12 for the Region 3 Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREG3.Region Base

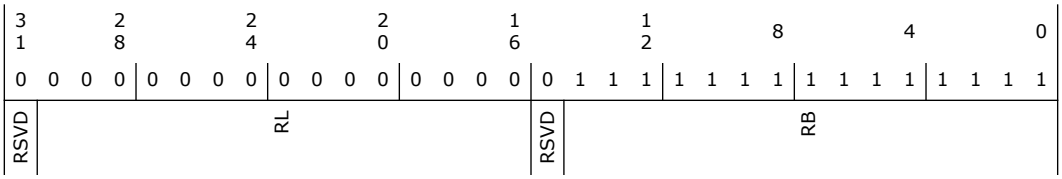
8.2.26 Flash Region 4 (BIOS_FREG4)—Offset 64h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 5

Default: 7FFFh



Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	Reserved.
30:16	0h RO/V	**Region Limit (RL):** Region Limit (RL): This specifies address bits 26:12 for the Region 4 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG4.Region Limit
15	0h RO	Reserved.
14:0	7FFFh RO/V	**Region Base (RB):** Region Base (RB): This specifies address bits 26:12 for the Region 4 Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREG4.Region Base

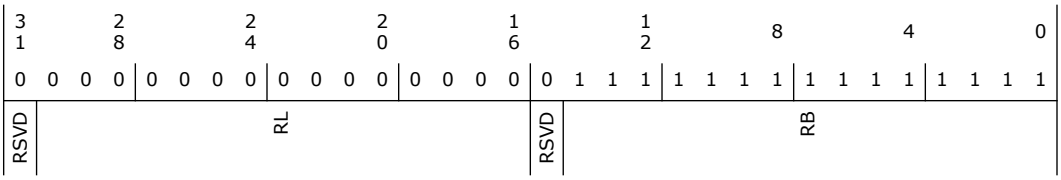
8.2.27 Flash Region 5 (BIOS_FREG5)—Offset 68h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 5

Default: 7FFFh



Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	Reserved.
30:16	0h RO/V	**Region Limit (RL):** Region Limit (RL): This specifies address bits 26:12 for the Region 5 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG5.Region Limit
15	0h RO	Reserved.
14:0	7FFFh RO/V	**Region Base (RB):** Region Base (RB): This specifies address bits 26:12 for the Region 5 Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREG5.Region Base

8.2.28 Flash Protected Range 0 (BIOS_FPR0)—Offset 84h

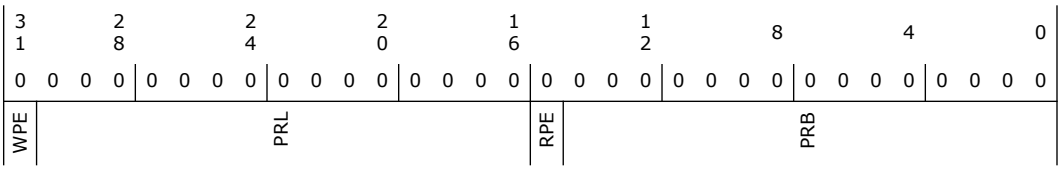
This register cannot be written when the FLOCKDN bit is set to 1.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 5

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**Write Protection Enable (WPE):** Write Protection Enable: When set, this bit indicates that the Base and Limit fields in this register are valid and that writes and erases directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
30:16	0h RW/L	**Protected Range Limit (PRL):** Protected Range Limit: This field corresponds to FLA address bits 26:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be FFFh for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range.
15	0h RW/L	**Read Protection Enable (RPE):** Read Protection Enable: When set, this bit indicates that the Base and Limit fields in this register are valid and that read directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
14:0	0h RW/L	**Protected Range Base (PRB):** Protected Range Base: This field corresponds to FLA address bits 26:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 000h for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range.

8.2.29 Flash Protected Range 1 (BIOS_FPR1)—Offset 88h

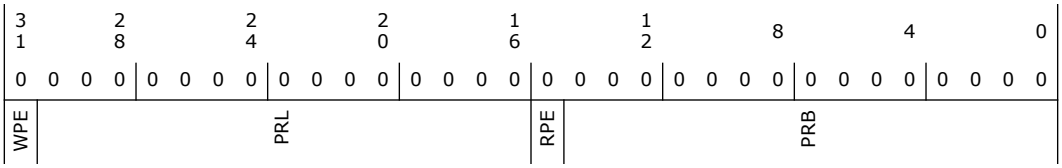
This register cannot be written when the FLOCKDN bit is set to 1.[

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 5

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**Write Protection Enable (WPE):** Write Protection Enable: When set, this bit indicates that the Base and Limit fields in this register are valid and that writes and erases directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
30:16	0h RW/L	**Protected Range Limit (PRL):** Protected Range Limit: This field corresponds to FLA address bits 26:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be FFFh for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range.
15	0h RW/L	**Read Protection Enable (RPE):** Read Protection Enable: When set, this bit indicates that the Base and Limit fields in this register are valid and that read directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
14:0	0h RW/L	**Protected Range Base (PRB):** Protected Range Base: This field corresponds to FLA address bits 26:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 000h for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range.

8.2.30 Flash Protected Range 2 (BIOS_FPR2)—Offset 8Ch

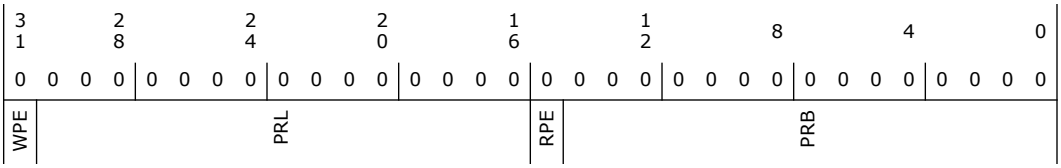
This register cannot be written when the FLOCKDN bit is set to 1.[

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 5

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**Write Protection Enable (WPE):** Write Protection Enable: When set, this bit indicates that the Base and Limit fields in this register are valid and that writes and erases directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
30:16	0h RW/L	**Protected Range Limit (PRL):** Protected Range Limit: This field corresponds to FLA address bits 26:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be FFFh for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range.
15	0h RW/L	**Read Protection Enable (RPE):** Read Protection Enable: When set, this bit indicates that the Base and Limit fields in this register are valid and that read directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
14:0	0h RW/L	**Protected Range Base (PRB):** Protected Range Base: This field corresponds to FLA address bits 26:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 000h for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range.

8.2.31 Flash Protected Range 3 (BIOS_FPR3)—Offset 90h

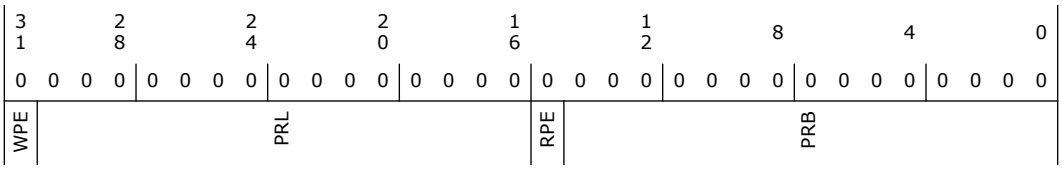
This register cannot be written when the PRR34_LOCKDN bit is set to 1

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 5

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**Write Protection Enable (WPE):** Write Protection Enable: When set, this bit indicates that the Base and Limit fields in this register are valid and that writes and erases directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
30:16	0h RW/L	**Protected Range Limit (PRL):** Protected Range Limit: This field corresponds to FLA address bits 26:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be FFFh for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range.
15	0h RW/L	**Read Protection Enable (RPE):** Read Protection Enable: When set, this bit indicates that the Base and Limit fields in this register are valid and that read directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
14:0	0h RW/L	**Protected Range Base (PRB):** Protected Range Base: This field corresponds to FLA address bits 26:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 000h for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range.

8.2.32 Flash Protected Range 4 (BIOS_FPR4)—Offset 94h

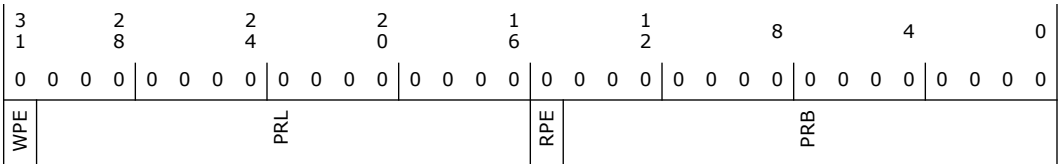
This register cannot be written when the PRR34_LOCKDN bit is set to 1

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 5

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**Write Protection Enable (WPE):** Write Protection Enable: When set, this bit indicates that the Base and Limit fields in this register are valid and that writes and erases directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
30:16	0h RW/L	**Protected Range Limit (PRL):** Protected Range Limit: This field corresponds to FLA address bits 26:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be FFFh for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range.
15	0h RW/L	**Read Protection Enable (RPE):** Read Protection Enable: When set, this bit indicates that the Base and Limit fields in this register are valid and that read directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
14:0	0h RW/L	**Protected Range Base (PRB):** Protected Range Base: This field corresponds to FLA address bits 26:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 000h for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range.

8.2.33 Global Protected Range 0 (BIOS_GPR0)—Offset 98h

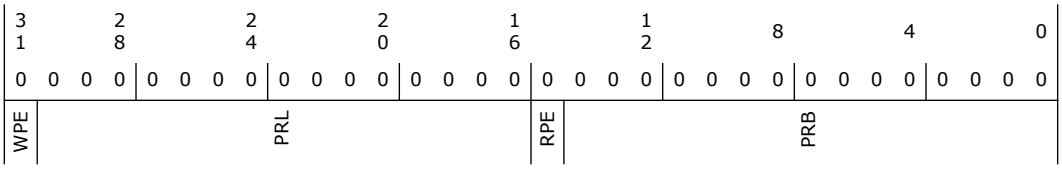
This register is initialized via softstraps. This protected range applies globally to all masters / flash requesters.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 5

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**Write Protection Enable (WPE):** Write Protection Enable: When set, this bit indicates that the Base and Limit fields in this register are valid and that writes and erases directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
30:16	0h RO/V	**Protected Range Limit (PRL):** Protected Range Limit: This field corresponds to FLA address bits 26:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be FFFh for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range.
15	0h RO/V	**Read Protection Enable (RPE):** Read Protection Enable: When set, this bit indicates that the Base and Limit fields in this register are valid and that read directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
14:0	0h RO/V	**Protected Range Base (PRB):** Protected Range Base: This field corresponds to FLA address bits 26:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 000h for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range.

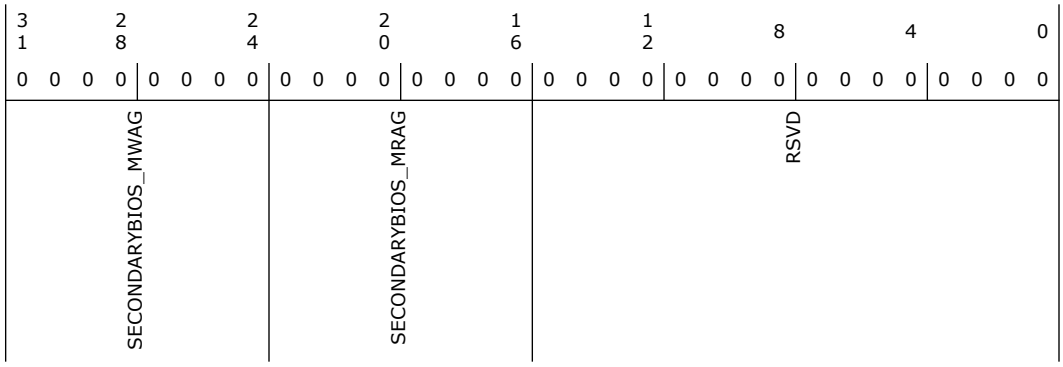
8.2.34 Secondary Flash Region Access Permissions (BIOS_SFRACC)—Offset B0h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 5

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW/L	**Secondary BIOS Master Write Access Grant (SECONDARYBIOS_MWAG):** Each bit 31:29 corresponds to Master7:0. BIOS can grant one or more masters write access to the Secondary BIOS region 6 overriding the permissions in the Flash Descriptor. Bits for unassigned masters are reserved. The contents of this register are locked by the FLOCKDN bit.
23:16	0h RW/L	**Secondary BIOS Master Read Access Grant (SECONDARYBIOS_MRAG):** Each bit 28:16 corresponds to Master7:0. BIOS can grant one or more masters read access to the Secondary BIOS region 6 overriding the read permissions in the Flash Descriptor. Bits for unassigned masters are reserved. The contents of this register are locked by the FLOCKDN bit.
15:0	0h RO	Reserved.

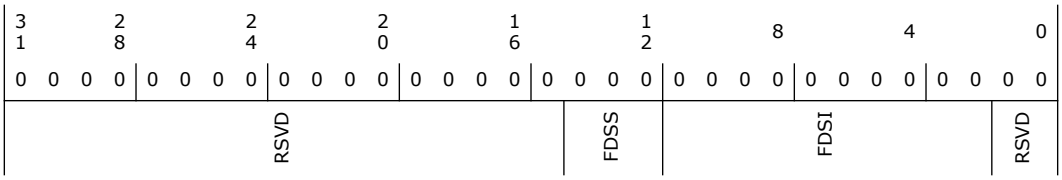
8.2.35 Flash Descriptor Observability Control (BIOS_FDOC)—Offset B4h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 5

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RO	Reserved.
14:12	0h RW	**Flash Descriptor Section Select (FDSS):** Selects which section within the loaded Flash Descriptor to observe. 000: Flash Signature and Descriptor Map 001: Component 010: Region 011: Master Others: Reserved
11:2	0h RW	**Flash Descriptor Section Index (FDSI):** Selects the DW offse within the Flash Descriptor Section to observe.
1:0	0h RO	Reserved.

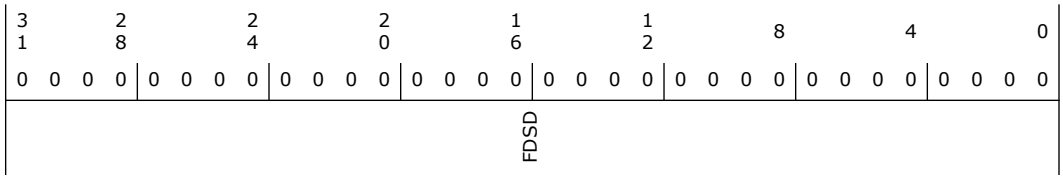
8.2.36 Flash Descriptor Observability Data (BIOS_FDOD)—Offset B8h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 5

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Flash Descriptor Section Data (FDSD):** Returns the DW of data to observe as selected in the Flash Descriptor Observability Control.

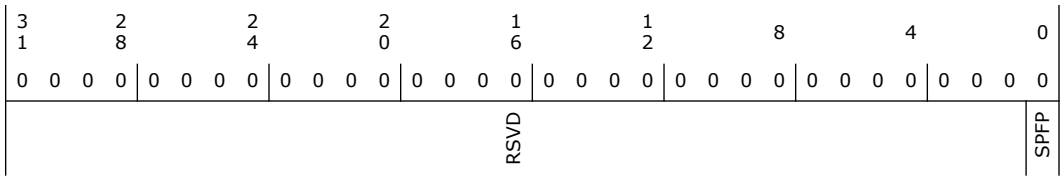
8.2.37 Additional Flash Control (BIOS_AFC)—Offset C0h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 5

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RW/V/P	**Stop Prefetch on Flush Pending (SPFP):** When set to 1, the in progress of a prefetch will be ended if subsequence access from the master of the same interface is detected to be a cache-miss and read cache will be flushed. When set to 0, the prefetch will be allowed to complete prior to flushing.

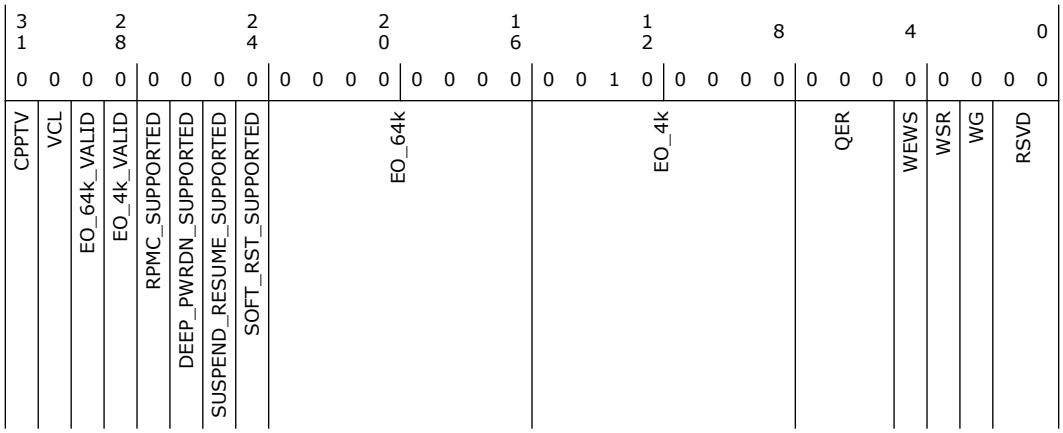
8.2.38 Vendor Specific Component Capabilities for Component 0 (BIOS_SFDP0_VSCC0)—Offset C4h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 5

Default: 2000h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**Component Property Parameter Table Valid (CPPTV):** This bit is set to a 1 if the Flash Controller detects a valid SFDP Component Property Parameter Table in Component 0. Note: If this bit is set software must not overwrite bits that were initialized by hardware via SFDP discovery.
30	0h RW/L	**Vendor Component Lock (VCL):** 0: The lock bit is not set 1: The Vendor Component Lock bit is set. This register locks itself when set.
29	0h RW/V/L	**64k Erase Valid (EO_64k_VALID):** 0: The EO_64k opcode is not valid. 1: The EO_64k opcode is valid.
28	0h RW/V/L	**4k Erase Valid (EO_4k_VALID):** 0: The EO_4k opcode is not valid. 1: The EO_4k opcode is valid.
27	0h RW/L	**RPMC Supported (RPMC_SUPPORTED):** 0 the device does not support RPMC 1 the device supports RPMC
26	0h RW/V/L	**Deep Powerdown Supported (DEEP_PWRDN_SUPPORTED):** 0 the device does not support Deep Powerdown 1 the device supports Deep Powerdown
25	0h RW/V/L	**Suspend/Resume Supported (SUSPEND_RESUME_SUPPORTED):** 0 the device does not support Suspend/Resume 1 the device supports Suspend/Resume
24	0h RW/V/L	**Soft Reset Supported (SOFT_RST_SUPPORTED):** 0 the device does not support Soft Reset 1 the device supports Soft Reset
23:16	0h RW/V/L	**64k Erase Opcode (EO_64k):** This register is programmed with the Flash 64k sector erase instruction opcode for component 0. This register is locked by the Vendor Component Lock (VCL) bit or the CPPTV bit.
15:8	20h RW/V/L	**4k Erase Opcode (EO_4k):** This register is programmed with the Flash 64k sector erase instruction opcode for component 0. This register is locked by the Vendor Component Lock (VCL) bit or the CPPTV bit.
7:5	0h RW/V/L	**Quad Enable Requirements (QER):** 000 = Part does not require a Quad Enable bit to be set, either because Quad is not supported or because the manufacturer somehow permanently enables Quad capability. 001 = Part requires bit 9 in status register 2 to be set to enable quad IO. Writing one byte to status register clears all bits in register 2, therefore status register writes MUST be two bytes. 010 = Part requires bit 6 of status register 1 to be set to enable quad IO. 011 = Part requires bit 7 of the configuration register to be set to enable Quad. 100 = Part requires bit 9 in status register 2 to be set to enable quad IO. Writing one byte to the status register does not clear the second byte. This register is locked by the Vendor Component Lock (VCL) bit. If the SFDP table contains this information, the flash controller loads these bits from the table. The flash controller uses this information to prevent clearing the QE bit in the flash device's status register when WSR=1.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW/V/L	**Write Enable on Write Status (WEWS):** 0 = 50h is the opcode to enable a status register write 1 : 06h is the opcode to enable a status register write This register is locked by the Vendor Component Lock (VCL) bit or the CPPTV bit. Note: Hardware ignores the state of this bit.
3	0h RW/V/L	**Write Status Required (WSR):** 0 = No requirement to write to the Write Status Register prior to a write 1 = A write is required to the Write Status Register prior to write and erase to remove any protection. This is required for SST components. This register is locked by the Vendor Component Lock (VCL) bit or the CPPTV bit. Note: Hardware ignores the state of this bit.
2	0h RW/V/L	**Write Granularity (WG):** 0 : Reserved 1 : 64 Byte This register is locked by the Vendor Component Lock (VCL) bit or the CPPTV bit. Note: Hardware ignores the state of this bit.
1:0	0h RO	Reserved.

8.2.39 Vendor Specific Component Capabilities for Component 1 (BIOS_SFDP1_VSCC1)—Offset C8h

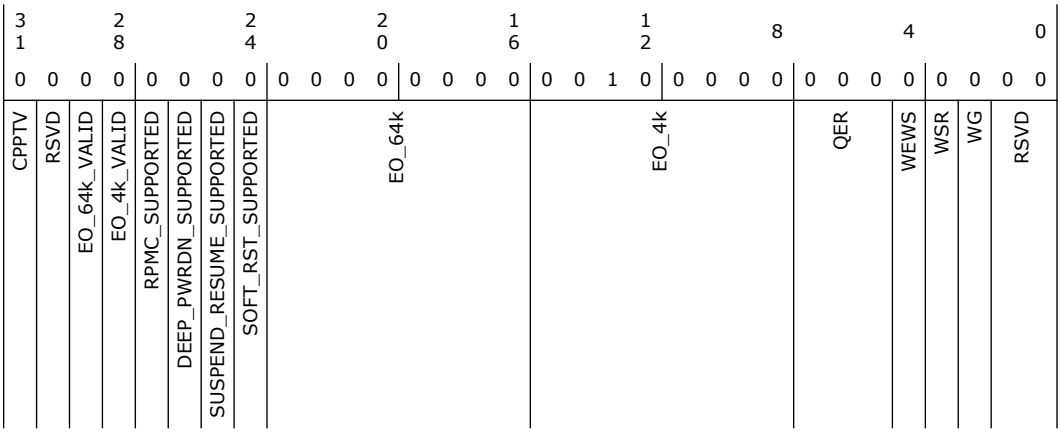
This register pertain to cycles targeting addresses outside of Component 0. The lockable bits in this register are locked when either CPPTV is set to 1 by hardware or when VCL is 1.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 5

Default: 2000h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**Component Property Parameter Table Valid (CPPTV):** This bit is set to a 1 if the Flash Controller detects a valid SFDP Component Property Parameter Table in Component 1. Note: If this bit is set software must not overwrite bits that were initialized by hardware via SFDP discovery RO
30	0h RO	Reserved.
29	0h RW/V/L	**64k Erase Valid (EO_64k_VALID):** 0: The EO_64k opcode is not valid. 1: The EO_64k opcode is valid.
28	0h RW/V/L	**4k Erase Valid (EO_4k_VALID):** 0: The EO_4k opcode is not valid. 1: The EO_4k opcode is valid.
27	0h RW/L	**RPMC Supported (RPMC_SUPPORTED):** 0 the device does not support RPMC 1 the device supports RPMC
26	0h RW/V/L	**Deep Powerdown Supported (DEEP_PWRDN_SUPPORTED):** 0 the device does not support Deep Powerdown 1 the device supports Deep Powerdown
25	0h RW/V/L	**Suspend/Resume Supported (SUSPEND_RESUME_SUPPORTED):** 1 the device supports Suspend/Resume
24	0h RW/V/L	**Soft Reset Supported (SOFT_RST_SUPPORTED):** 0 the device does not support Soft Reset 1 the device supports Soft Reset
23:16	0h RW/V/L	**64k Erase Opcode (EO_64k):** This register is programmed with the Flash 64k sector erase instruction opcode for component 1. This register is locked by the Vendor Component Lock (VCL) bit or the CPPTV bit.
15:8	20h RW/V/L	**4k Erase Opcode (EO_4k):** This register is programmed with the Flash 4k subsector erase instruction opcode for component 1. Software must program this register if the SFDP table for this component does not show 4 kByte erase capability. This register is locked by the Vendor Component Lock (VCL) bit or the CPPTV bit.
7:5	0h RW/V/L	**Quad Enable Requirements (QER):** 000 = Part does not require a Quad Enable bit to be set, either because Quad is not supported or because the manufacturer somehow permanently enables Quad capability. 001 = Part requires bit 9 in status register 2 to be set to enable quad IO. Writing one byte to status register clears all bits in register 2, therefore status register writes MUST be two bytes. 010 = Part requires bit 6 of status register 1 to be set to enable quad IO. 011 = Part requires bit 7 of the configuration register to be set to enable Quad. 100 = Part requires bit 9 in status register 2 to be set to enable quad IO. Writing one byte to the status register does not clear the second byte. This register is locked by the Vendor Component Lock (VCL) bit. If the SFDP table contains this information, the flash controller loads these bits from the table. The flash controller uses this information to prevent clearing the QE bit in the flash device's status register when WSR=1.
4	0h RW/V/L	**Write Enable on Write Status (WEWS):** 0 : 50h is the opcode to enable a status register write 1 : 06h is the opcode to enable a status register write This register is locked by the Vendor Component Lock (VCL) bit or the CPPTV bit.
3	0h RW/V/L	**Write Status Required (WSR):** 0: No requirement to write to the Write Status Register prior to a write 1: A write is required to the Write Status Register prior to write and erase to remove any protection. This is required for SST components. This register is locked by the Vendor Component Lock (VCL) bit or the CPPTV bit.
2	0h RW/V/L	**Write Granularity (WG):** 0 : Reserved 1 : 64 Byte This register is locked by the Vendor Component Lock (VCL) bit orthe CPPTV bit. Note: Hardware ignores the state of this bit.
1:0	0h RO	Reserved.

8.2.40 Parameter Table Index (BIOS_PTINX)—Offset CCh

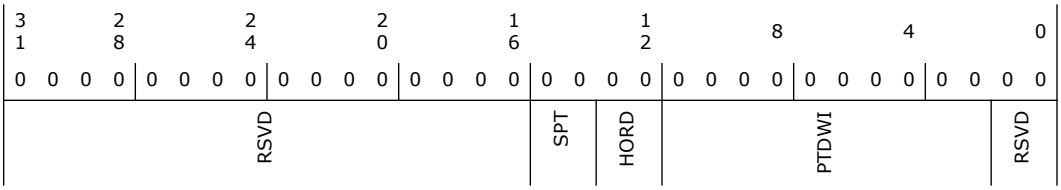
Observability control for Component Property Tables

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 5

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:14	0h RW	**Supported Parameter Table (SPT):** Selects which supported parameter table to observe. 00 : Component 0 Property Parameter Table 01 : Component 1 Property Parameter Table 10 - 11 : Reserved
13:12	0h RW	**Header or Data (HORD):** Select parameter table header DW vs Data DW. 00 : SFDP Header 01 : Parameter Table Header 10 : Data 11 : Reserved
11:2	0h RW	**Parameter Table DW Index (PTDWI):** Selects the DW offset within the parameter table to observe.
1:0	0h RO	Reserved.

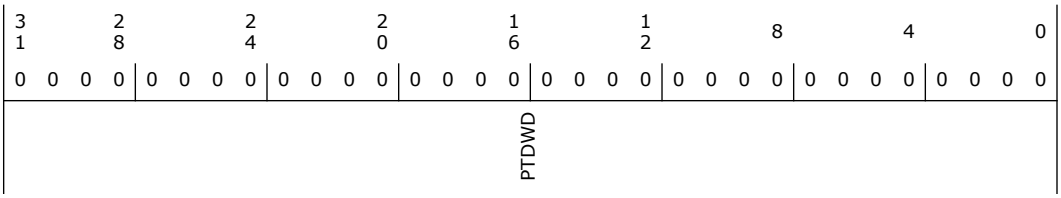
8.2.41 Parameter Table Data (BIOS_PTDATA)—Offset D0h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 5

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Parameter Table DW Data (PTDWD):** Returns the DW of data to observe as selected in the Parameter Table Index register. Note: The returned value of reserved fields in the SFDP header or table must be ignored by software. The flash controller may return either 0 or 1 for these fields.

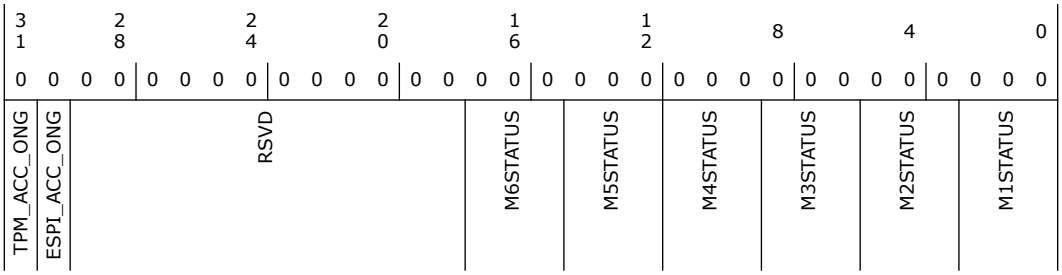
8.2.42 SPI Bus Requester Status (BIOS_SBRS)—Offset D4h

Access Method

Type: MEM Register (Size: 32 bits)

Device: 31
Function: 5

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**TPM access ongoing (TPM_ACC_ONG)**
30	0h RO/V	**eSPI access ongoing (ESPI_ACC_ONG)**
29:18	0h RO	Reserved.
17:15	0h RO/V	**Master 6 Status (M6STATUS):** Master 6 Status (M6STATUS): See description under M1STATUS
14:12	0h RO/V	**Master 5 Status (M5STATUS):** Master 5 Status (M5STATUS): See description under M1STATUS
11:9	0h RO/V	**Master 4 Status (M4STATUS):** Master 4 Status (M4STATUS): See description under M1STATUS
8:6	0h RO/V	**Master 3 Status (M3STATUS):** Master 3 Status (M3STATUS): See description under M1STATUS
5:3	0h RO/V	**Master 2 Status (M2STATUS):** Master 2 Status (M2STATUS): See description under M1STATUS
2:0	0h RO/V	**Master 1 Status (M1STATUS):** Indicates whether this master has an outstanding transaction enqueued or in flight and the transaction type. 0xx : no transaction 100 : flash read transaction 101 : flash write transaction 110 : flash erase transaction 111 : flash RPMC transaction

8.3 BIOS Flash Program Registers Summary

Table 8-3. Summary of BIOS Flash Program Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
F0h	F3h	Set Strap Msg Lock (SSML)—Offset F0h	0h
F4h	F7h	Set Strap Msg Control (SSMC)—Offset F4h	0h
F8h	FBh	Set Strap Msg Data (SSMD)—Offset F8h	0h

8.3.1 Set Strap Msg Lock (SSML)—Offset F0h

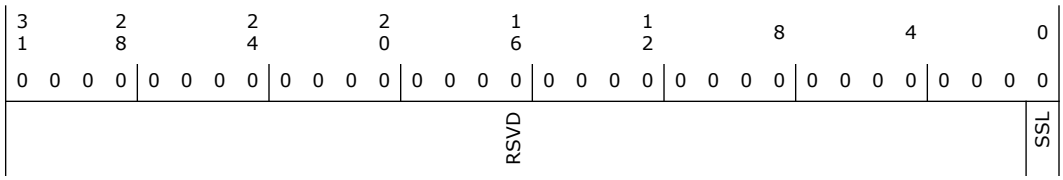
Lockable: Yes
Power Well: Resume
reset_type= wrsmrst#

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 5

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RW/L	**Set_Strap Lock (SSL):** When set to '1', all of SSML, SSMC and SSMD is locked, including this Lock bit. Note that this bit is reset on CF9 resets.

8.3.2 Set Strap Msg Control (SSMC)—Offset F4h

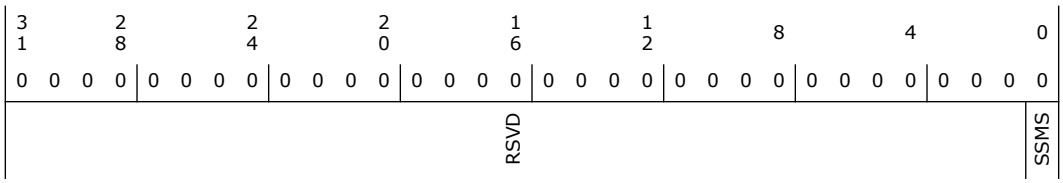
Lockable: Yes
Power Well: DSW
reset_type= dsw_pok
The DSW bits are all cleared by dsw_pok, but must not be cleared by CF9h resets.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 5

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RW/L	**Set_Strap Mux Select (SSMS):** When set to '1', the Set strap message bits [47:32] come from the Set_Strap Msg Data register. This bit is reset by the RSMRST# pin only. When '0', the Set-Strap data continues to come from the soft straps themselves. This register field is locked by the Set Strap Lock (SSML.SSL) bit.

8.3.3 Set Strap Msg Data (SSMD)—Offset F8h

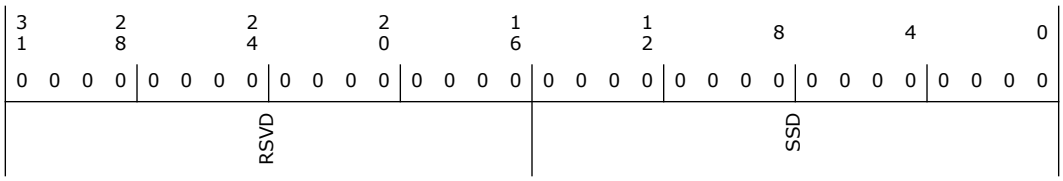
Lockable: Yes
Power Well: DSW
Reset Type: dsw_pok
This register is used to provide a BIOS programmable sticky register which contains data that will be used in the Set-Strap type 1 msg on subsequent resets. These bits are in the resume well, so only reset on G3.
The usage model is that on each reset BIOS will check the state of the CPU. If the state is correct then BIOS continues. If not, then BIOS writes the SSMD and SSMC registers and does a CF9 reset.
On the reset the value of what was written to SSMD takes effect.
Note that some mobile platforms force G3 on S5 requests. For those platforms, if the user/BIOS wants to have these bits set, there will be 2 resets on every power-on. If the platform accepts the default of '0' for these controls, then there is only one reset.
The bits are in DSW and not RTC well because this allows a user upgrade, assuming the user unplugged the system before doing the upgrade, to revert to a setting of 0. This should reduce any interoperability concerns regarding user upgrades.
The DSW bits are all cleared dsw_pok, and must not be cleared by CF9h resets.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 5

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	0h RW/L	**Set_Strap Data (SSD):** When SSMS is '1', then this data is sent in the Set-Strap msg Type 1 upon reset. This data is sent in the 2nd DW of data, bits[15:0]. This register field is locked by the Set Strap Lock (SSML.SSL) bit.

§ §

9 Integrated GbE (D31:F6)

9.1 GbE Configuration Registers Summary

Table 9-1. Summary of GbE Configuration Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	GbE Vendor and Device Identification Register (GBE_VID_DID)—Offset 0h	156F8086h
4h	7h	PCI Command & Status Register (PCICMD_STS)—Offset 4h	100000h
8h	Bh	Revision Identification & Class Code Register (RID_CC)—Offset 8h	20000XXh
Ch	Fh	Cache Line Size Primary Latency Timer & Header Type Register (CLS_PLT_HEADTYP)—Offset Ch	0h
10h	13h	Memory Base Address Register A (MBARA)—Offset 10h	0h
2Ch	2Fh	Subsystem Vendor & Subsytem ID (DMI_CONFIG11)—Offset 2Ch	8086h
30h	33h	Expansion ROM Base Address Register (ERBA)—Offset 30h	0h
34h	37h	Capabilities List Pointer Register (CAPP)—Offset 34h	C8h
3Ch	3Fh	Interrupt Information & Maximum Latency/Minimum GrantRegister (INTR_MLMG)—Offset 3Ch	100h
A0h	A3h	LAN Disable Control (LANDISCTRL)—Offset A0h	0h
A4h	A7h	Lock LAN Disable (LOCKLANDIS)—Offset A4h	0h
A8h	ABh	System Time Control High Register (LTRCAP)—Offset A8h	0h
C8h	CBh	Capabilities List and Power Managment Capabilities Register (CLIST1_PMC)—Offset C8h	23D001h
CCh	CFh	PCI Power Management Control Status & Data Register (PMCS_DR)—Offset CCh	0h
D0h	D3h	Capabilities List 2 & Message Control Register (CLIST2_MCTL)—Offset D0h	80E005h
D4h	D7h	Message Address Low Register (MADDL)—Offset D4h	0h
D8h	DBh	Message Address High Register (MADDH)—Offset D8h	0h
DCh	DFh	Message Data Register (MDAT)—Offset DCh	0h

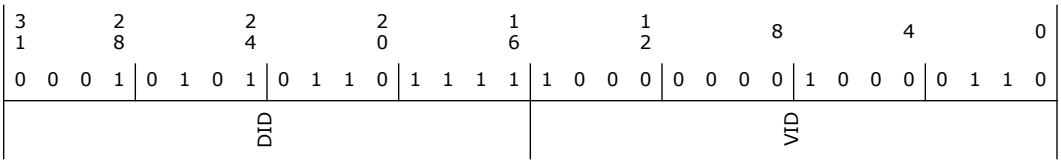
9.1.1 GbE Vendor and Device Identification Register (GBE_VID_DID)—Offset 0h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 6

Default: 156F8086h



Bit Range	Default & Access	Field Name (ID): Description
31:16	156Fh RW/V	**Device ID (DID):** This is a 16-bit value assigned to the PCH Gigabit LAN controller. The field may be auto-loaded from the NVM word 0Dh during initialization time depending on the "Load Vendor/ Device ID" bit field in NVM word 0Ah.
15:0	8086h RW/V	**Vendor ID (VID):** This is a 16-bit value assigned to Intel. The field may be auto-loaded from the NVM at address 0Dh during INIT time depending on the "Load Vendor/Device ID" bit field in NVM word 0Ah with a default value of 8086h.

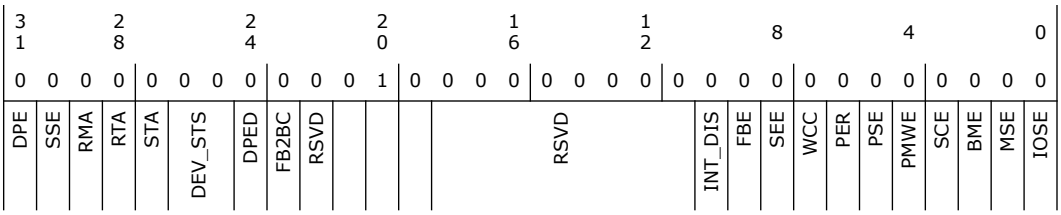
9.1.2 PCI Command & Status Register (PCICMD_STS)—Offset 4h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 6

Default: 100000h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/V	**Detected Parity Error (DPE):** 0 = No parity error detected. 1 = Set when the Gb LAN controller receives a command or data from the backbone with a parity error. This is set even if PCIMD.PER (D25:F0, bit 6) is not set.
30	0h RW/V	**Signaled System Error (SSE):** 0 = No system error signaled. 1 = Set when the Gb LAN controller signals a system error to the internal SERR# logic.
29	0h RW/V	**Received Master Abort (RMA):** 0 = Root port has not received a completion with unsupported request status from the backbone. 1 = Set when the GbE LAN controller receives a completion with unsupported request status from the backbone.
28	0h RW/V	**Received Target Abort (RTA):** 0 = Root port has not received a completion with completer abort from the backbone. 1 = Set when the Gb LAN controller receives a completion with completer abort from the backbone.
27	0h RW/V	**Signaled Target Abort (STA):** 0 = No target abort received. 1 = Set whenever the Gb LAN controller forwards a target abort received from the downstream device onto the backbone.
26:25	0h RW/V	**DEVSEL# Timing Status (DEV_STS):** Hardwired to 0.
24	0h RW/V	**Master Data Parity Error Detected (DPED):** 0 = No data parity error received. 1 = Set when the Gb LAN Controller receives a completion with a data parity error on the backbone and PCIMD.PER (D25:F0, bit 6) is set.

Bit Range	Default & Access	Field Name (ID): Description
23	0h RW/V	**Fast Back to Back Capable (FB2BC):** Hardwired to 0.
22	0h RO	Reserved.
21	0h RW/V	**66 MHz Capable:** Hardwired to 0.
20	1h RW/V	**Capabilities List:** Hardwired to 1. Indicates the presence of a capabilities list.
19	0h RW/V	**Interrupt Status:** Indicates status of hot-plug and power management interrupts on the root port that result in INTx# message generation. 0 = Interrupt is de-asserted. 1 = Interrupt is asserted. This bit is not set if MSI is enabled. If MSI is not enabled, this bit is set regardless of the state of PCICMD.Interrupt Disable bit (D25:F0:04h:bit 10).
18:11	0h RO	Reserved.
10	0h RW	**Interrupt Disable (INT_DIS):** This disables pin-based INTx# interrupts on enabled hot-plug and power management events. This bit has no effect on MSI operation. 0 = Internal INTx# messages are generated if there is an interrupt for hot-plug or power management and MSI is not enabled. 1 = Internal INTx# messages will not be generated. This bit does not affect interrupt forwarding from devices connected to the root port. Assert_INTx and de-assert_INTx messages will still be forwarded to the internal interrupt controllers if this bit is set.
9	0h RW/V	**Fast Back to Back Enable (FBE):** Hardwired to 0.
8	0h RW	**SERR# Enable (SEE):** 0 = Disable 1 = Enables the Gb LAN controller to generate an SERR# message when PSTS.SSE is set.
7	0h RW/V	**Wait Cycle Control (WCC):** Hardwired to 0.
6	0h RW	**Parity Error Response (PER):** 0 = Disable. 1 = Indicates that the device is capable of reporting parity errors as a master on the backbone.
5	0h RW/V	**Palette Snoop Enable (PSE):** Hardwired to 0.
4	0h RW/V	**Postable Memory Write Enable (PMWE):** Hardwired to 0.
3	0h RW/V	**Special Cycle Enable (SCE):** Hardwired to 0.
2	0h RW	**Bus Master Enable (BME):** 0 = Disable. All cycles from the device are master aborted 1 = Enable. Allows the root port to forward cycles onto the backbone from a Gigabit LAN device.
1	0h RW	**Memory Space Enable (MSE):** 0 = Disable. Memory cycles within the range specified by the memory base and limit registers are master aborted on the backbone. 1 = Enable. Allows memory cycles within the range specified by the memory base and limit registers can be forwarded to the Gigabit LAN device.
0	0h RW/V	**I/O Space Enable (IOSE):** This bit controls access to the I/O space registers. 0 = Disable. I/O cycles within the range specified by the I/O base and limit registers are master aborted on the backbone. 1 = Enable. Allows I/O cycles within the range specified by the I/O base and limit registers can be forwarded to the Gigabit LAN device.

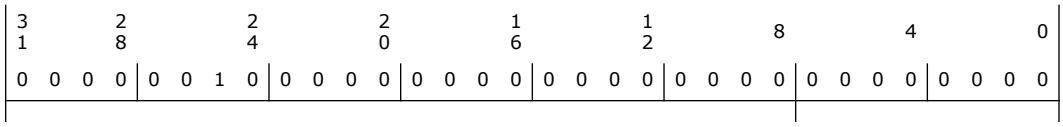
9.1.3 Revision Identification & Class Code Register (RID_CC)—Offset 8h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 6

Default: 20000xxh



Bit Range	Default & Access	Field Name (ID): Description
31:8	20000h RW/V	**Class Code:** Identifies the device as an Ethernet Adapter. 020000h = Ethernet Adapter.
7:0	0h RW/V	**Revision ID:** Indicates stepping of the host controller. Refer to Device and Revision ID table in Vol1 for specific value.

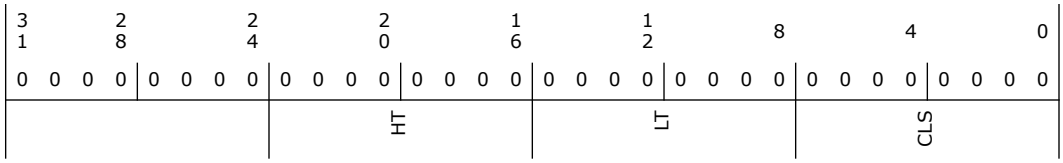
9.1.4 Cache Line Size Primary Latency Timer & Header Type Register (CLS_PLT_HEADTYP)—Offset Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 6

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW/V	**Reserved**
23:16	0h RW/V	**Header Type (HT):** 00h = Indicates this is a single function device.
15:8	0h RW/V	**Latency Timer (LT):** Hardwired to 0.
7:0	0h RW/V	**Cache Line Size (CLS):** This field is implemented by PCI devices as a read/write field for legacy compatibility purposes but has no impact on any device functionality.

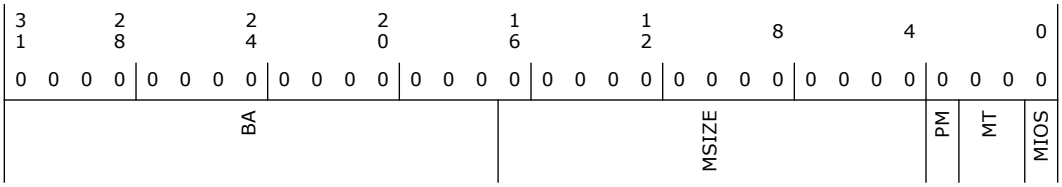
9.1.5 Memory Base Address Register A (MBARA)—Offset 10h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 6

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RW	**Base Address (BA):** Software programs this field with the base address of this region.
16:4	0h RW/V	**Memory Size (MSIZE):** Memory size is 128KB.
3	0h RW/V	**Prefetchable Memory (PM):** The GbE LAN controller does not implement prefetchable memory.
2:1	0h RW/V	**Memory Type (MT):** Set to 00b indicating a 32-bit BAR.
0	0h RW/V	**Memory/I/O Space (MIOS):** Set to 0 indicating a Memory Space BAR.

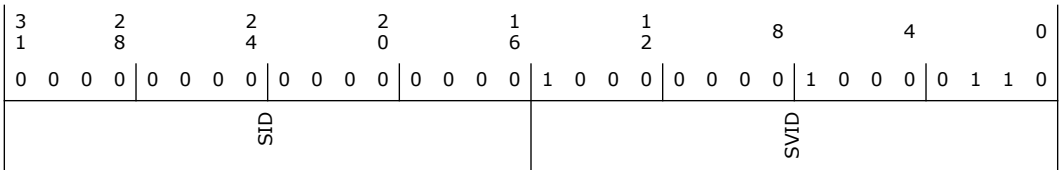
9.1.6 Subsystem Vendor & Subsytem ID (DMI_CONFIG11)—Offset 2Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 6

Default: 8086h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW/V	**Subsystem ID (SID):** This value may be loaded automatically from the NVM Word 0Bh upon power up or reset depending on the "Load Subsystem ID" bit field in NVM word 0Ah with a default value of 0000h. This value is loadable from NVM word location 0Ah.
15:0	8086h RW/V	**Subsystem Vendor ID (SVID):** This value may be loaded automatically from the NVM Word 0Ch upon power up or reset depending on the "Load Subsystem ID" bit field in NVM word 0Ah. A value of 8086h is default for this field upon power up if the NVM does not respond or is not programmed. All functions are initialized to the same value.

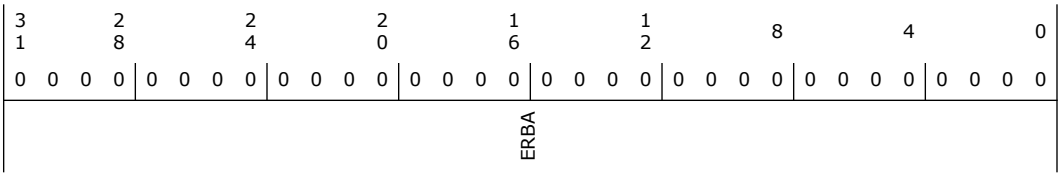
9.1.7 Expansion ROM Base Address Register (ERBA)—Offset 30h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 6

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Expansion ROM Base Address (ERBA):** This register is used to define the address and size information for boot-time access to the optional FLASH memory. If no Flash memory exists, this register reports 00000000h.

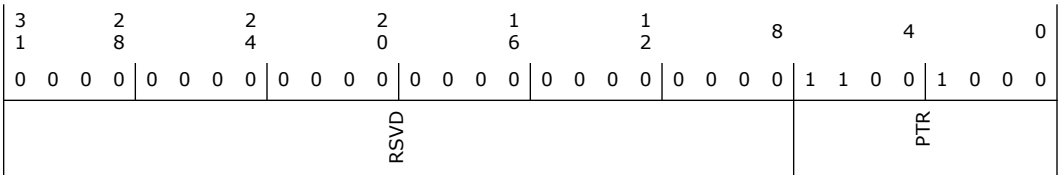
9.1.8 Capabilities List Pointer Register (CAPP)—Offset 34h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 6

Default: C8h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	C8h RW/V	**Capabilities Pointer (PTR):** Indicates that the pointer for the first entry in the capabilities list is at C8h in configuration space.

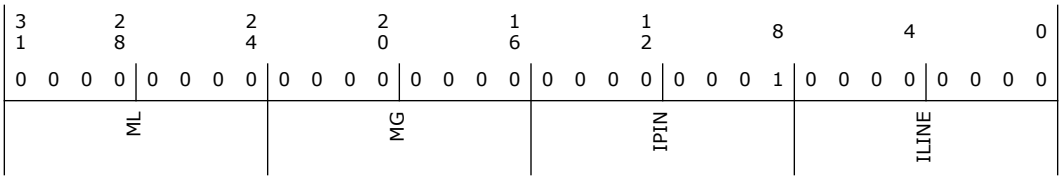
9.1.9 Interrupt Information & Maximum Latency/Minimum GrantRegister (INTR_MLMG)—Offset 3Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 6

Default: 100h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW/V	**Maximum Latency (ML):** Not used. Hardwired to 00h.
23:16	0h RW/V	**Minimum Grant (MG):** Not used. Hardwired to 00h.
15:8	1h RW/V	**Interrupt Pin (IPIN):** Indicates the interrupt pin driven by the GbE LAN controller. 01h = The GbE LAN controller implements legacy interrupts on INTA.
7:0	0h RW	**Interrupt Line (ILINE):** Default = 00h. Software written value indicates which interrupt line (vector) the interrupt is connected. No hardware action is taken on this register.

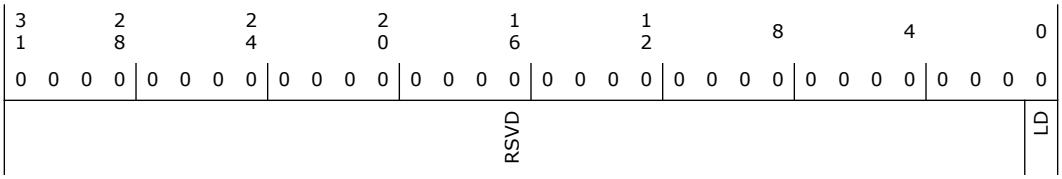
9.1.10 LAN Disable Control (LANDISCTRL)—Offset A0h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 6

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RW	**LAN Disable (LD):** Setting this bit to 1 will disable the LAN Controller functionality.

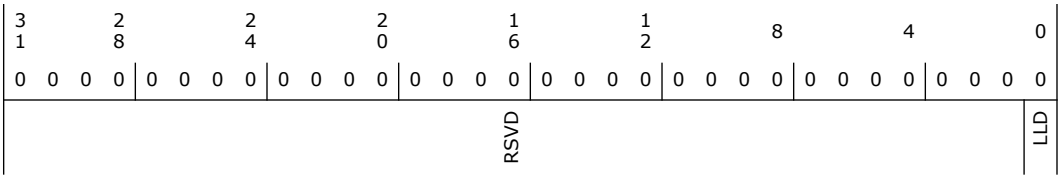
9.1.11 Lock LAN Disable (LOCKLANDIS)—Offset A4h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 6

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RW	**Lock LAN Disable (LLD):** When set this bit blocks writes to the LANDISCTRL register. Note: Once set this bit will only be cleared on host reset.

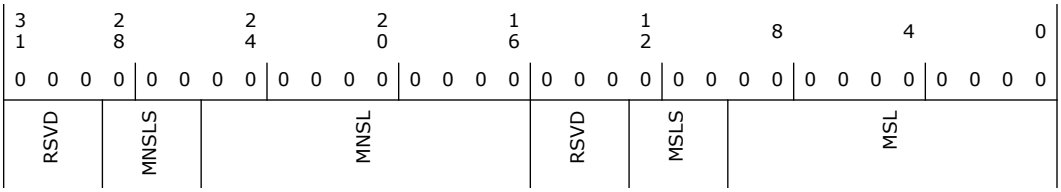
9.1.12 System Time Control High Register (LTRCAP)—Offset A8h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 6

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	Reserved.
28:26	0h RW	**Maximum Non-Snoop Latency Scale (MNSLS):** Provides a scale for the value contained within the Maximum Non-Snoop Latency Value field. 000b = Value times 1 ns 001b = Value times 32 ns 010b = Value times 1,024 ns 011b = Value times 32,768 ns 100b = Value times 1,048,576 ns 101b = Value times 33,554,432 ns 110b–111b = Reserved
25:16	0h RW	**Maximum Non-Snoop Latency (MNSL):** Specifies the maximum non-snoop latency that a device is permitted to request. Software should set this to the platform's maximum supported latency or less. This field is also an indicator of the platforms maximum latency, should an endpoint send up LTR Latency Values with the Requirement bit not set.
15:13	0h RO	Reserved.
12:10	0h RW	**Maximum Snoop Latency Scale (MSLS):** Provides a scale for the value contained within the Maximum Snoop Latency Value field. 000b = Value times 1 ns 001b = Value times 32 ns 010b = Value times 1,024 ns 011b = Value times 32,768 ns 100b = Value times 1,048,576 ns 101b = Value times 33,554,432 ns 110b–111b = Reserved
9:0	0h RW	**Maximum Snoop Latency (MSL):** Specifies the maximum snoop latency that a device is permitted to request. Software should set this to the platform's maximum supported latency or less. This field is also an indicator of the platforms maximum latency, should an endpoint send up LTR Latency Values with the Requirement bit not set.

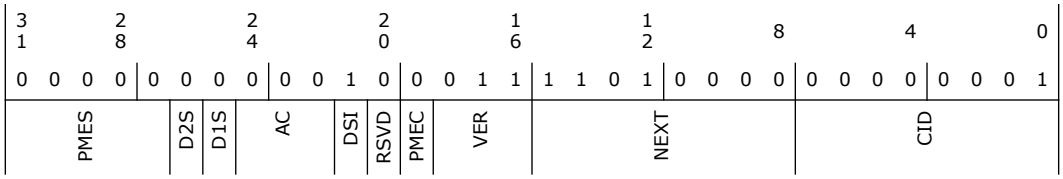
9.1.13 Capabilities List and Power Managment Capabilities Register (CLIST1_PMC)—Offset C8h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 6

Default: 23D001h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RW/V	**PME_SUPPORT (PMES):** This five-bit field indicates the power states in which the function may assert PME#. It depend on PM Ena and AUX-PWR bits in word 0Ah in the NVM: Condition Functionality Value PM Ena=0 No PME at all states 0000b PM Ena and AUX-PWR=0 PME at D0 and D3HOT 01001b PM Ena and AUX-PWR=1 PME at D0, D3HOT and D3COLD 11001b These bits are not reset by Function Level Reset.
26	0h RW/V	**D2_SUPPORT (D2S):** The D2 state is not supported.
25	0h RW/V	**D1_SUPPORT (D1S):** The D1 state is not supported.
24:22	0h RW/V	**AUX_CURRENT (AC):** Required current defined in the Data register.
21	1h RW/V	**Device Specific Initialization (DSI):** Set to 1. The GbE LAN Controller requires its device driver to be executed following transition to the D0 un-initialized state.
20	0h RO	Reserved.
19	0h RW/V	**PME Clock (PMEC):** Hardwired to 0.
18:16	3h RW/V	**Version (VER):** Hardwired to 010b to indicate support for Revision 1.1 of the PCI Power Management Specification.
15:8	D0h RW/V	**Next Capability (NEXT):** Value of D0h indicates the location of the next pointer.
7:0	1h RW/V	**Capability ID (CID):** Indicates the linked list item is a PCI Power Management Register.

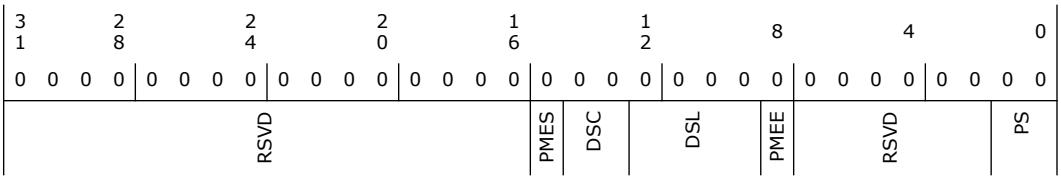
9.1.14 PCI Power Management Control Status & Data Register (PMCS_DR)—Offset CCh

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 6

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	0h RW/V	**PME STATUS (PMES):** This bit is set to 1 when the function detects a wake-up event independent of the state of the PMEE bit. Writing a 1 will clear this bit.
14:13	0h RW/V	**DATA SCALE (DSC):** This field indicates the scaling factor to be used when interpreting the value of the Data register. For the GbE LAN and common functions this field equals 01b (indicating 0.1 watt units) if the PM is enabled in the NVM, and the Data_Select field is set to 0, 3, 4, 7, (or 8 for Function 0). Otherwise, it equals 00b. For the manageability functions, this field equals 10b (indicating 0.01 watt units) if the PM is enabled in the NVM, and the Data_Select field is set to 0, 3, 4, 7. Otherwise, it equals 00b.
12:9	0h RW	**Data Select (DSL):** This four-bit field is used to select which data is to be reported through the Data register (offset CFh) and Data_Scale field. These bits are writeable only when Power Management is enabled using NVM. 0h = D0 Power Consumption 3h = D3 Power Consumption 4h = D0 Power Dissipation 7h = D3 Power Dissipation 8h = Common Power All other values are reserved.
8	0h RW	**PME Enable (PMEE):** If Power Management is enabled in the NVM, writing a 1 to this bit will enable Wakeup. If Power Management is disabled in the NVM, writing a 1 to this bit has no affect, and will not set the bit to 1. This bit is not reset by Function Level Reset.
7:2	0h RO	Reserved.
1:0	0h RW/V	**Power State (PS):** This field is used both to determine the current power state of the GbE LAN Controller and to set a new power state. The values are: 00 = D0 state (default) 01 = Ignored 10 = Ignored 11 = D3 state (Power Management must be enabled in the NVM or this cycle will be ignored).

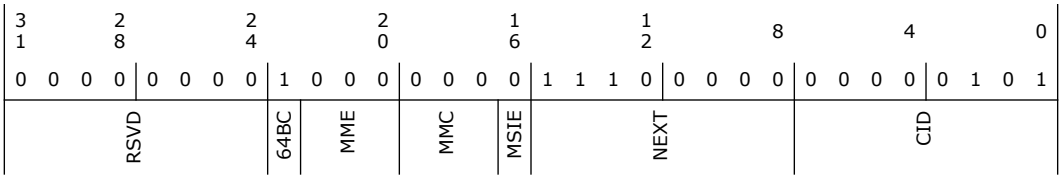
9.1.15 Capabilities List 2 & Message Control Register (CLIST2_MCTL)—Offset D0h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 6

Default: 80E005h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	1h RW/V	**64-bit Capable (64BC):** Set to 1 to indicate that the GbE LAN Controller is capable of generating 64-bit message addresses.
22:20	0h RW/V	**Multiple Message Enable (MME):** Returns 000b to indicate that the GbE LAN controller only supports a single message.
19:17	0h RW/V	**Multiple Message Capable (MMC):** The GbE LAN controller does not support multiple messages.
16	0h RW	**Message Signal Interrupt Enable (MSIE):** 0 = MSI generation is disabled. 1 = The Gb LAN controller will generate MSI for interrupt assertion instead of INTx signaling.
15:8	E0h RW/V	**Next Capability (NEXT):** Value of E0h points to the Function Level Reset capability structure. These bits are not reset by Function Level Reset.
7:0	5h RW/V	**Capability ID (CID):** Indicates the linked list item is a Message Signaled Interrupt Register.

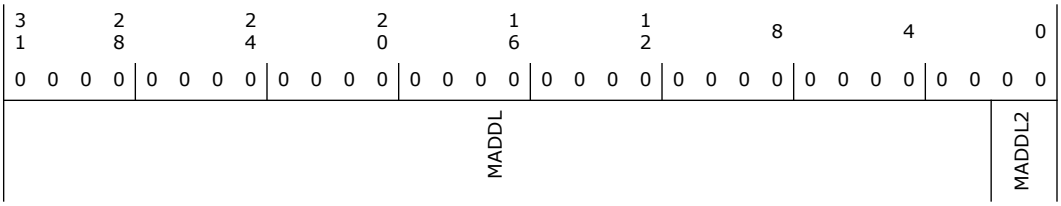
9.1.16 Message Address Low Register (MADDL)—Offset D4h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 6

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW/V	**Message Address Low (MADDL):** These bits combine with MADDL2 to create one 32 bit field which is written by the system to indicate the lower 32 bits of the address to use for the MSI memory write transaction.
1:0	0h RW/V	**Message Address Low 2 (MADDL2):** These bits combine with MADDL to create one 32 bit field which is written by the system to indicate the lower 32 bits of the address to use for the MSI memory write transaction. These lower two bits will always return 0.

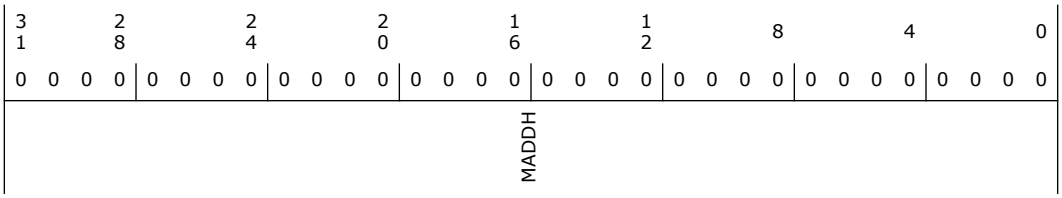
9.1.17 Message Address High Register (MADDH)—Offset D8h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 6

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Message Address High (MADDH):** Written by the system to indicate the upper 32 bits of the address to use for the MSI memory write transaction.

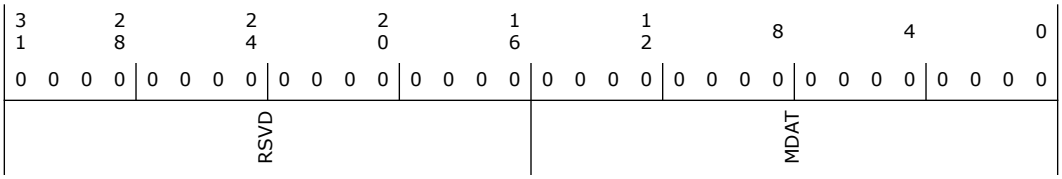
9.1.18 Message Data Register (MDAT)—Offset DCh

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 6

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	0h RW	**Message Data (MDAT):** Written by the system to indicate the lower 16 bits of the data written in the MSI memory write DWord transaction. The upper 16 bits of the transaction are written as 0000h.

9.2 GbE Memory Mapped I/O Registers Summary

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	Gigabit Ethernet Capabilities and Status (GBECSR_00)—Offset 0h	0h
18h	1Bh	Gigabit Ethernet Capabilities and Status (GBECSR_18)—Offset 18h	0h
20h	23h	Gigabit Ethernet Capabilities and Status (GBECSR_20)—Offset 20h	10000000h
F00h	F03h	Gigabit Ethernet Capabilities and Status (GBECSR_F00)—Offset F00h	0h
F10h	F13h	Gigabit Ethernet Capabilities and Status F10 (GBECSR_F10)—Offset F10h	Ch
5400h	5403h	Gigabit Ethernet Capabilities and Status (GBECSR_5400)—Offset 5400h	0h

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
5404h	5407h	Gigabit Ethernet Capabilities and Status (GBECSR_5404)—Offset 5404h	0h
5800h	5803h	Gigabit Ethernet Capabilities and Status (GBECSR_5800)—Offset 5800h	0h
5B54h	5B57h	Gigabit Ethernet Capabilities and Status (GBECSR_5B54)—Offset 5B54h	0h

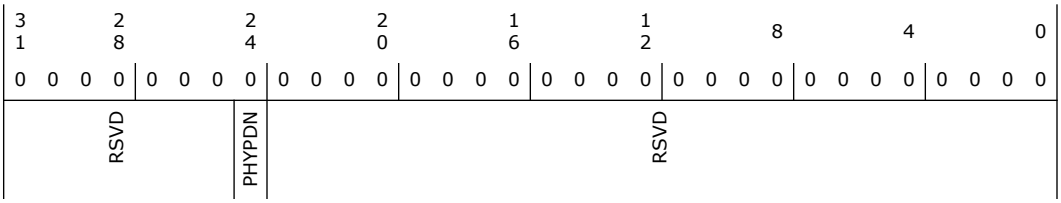
9.2.1 Gigabit Ethernet Capabilities and Status (GBECSR_00)—Offset 0h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 6

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	Reserved.
24	0h RW	**PHY Power Down (PHYPDN):** When cleared (0b), the PHY power down setting is controlled by the internal logic of PCH.
23:0	0h RO	Reserved.

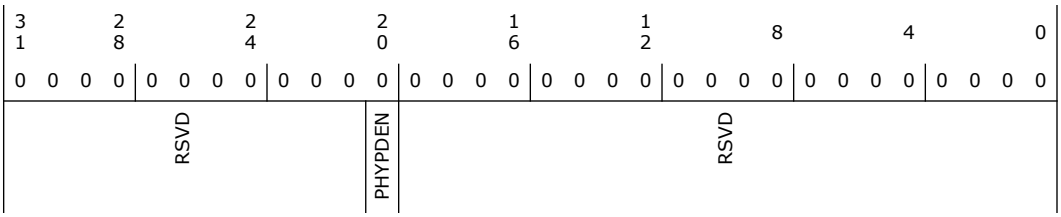
9.2.2 Gigabit Ethernet Capabilities and Status (GBECSR_18)—Offset 18h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 6

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	Reserved.
20	0h RW	**PHY Power Down Enable (PHYPDEN):** When set, this bit enables the PHY to enter a low-power state when the LAN controller is at the DMOff/ D3 or with no WOL.
19:0	0h RO	Reserved.

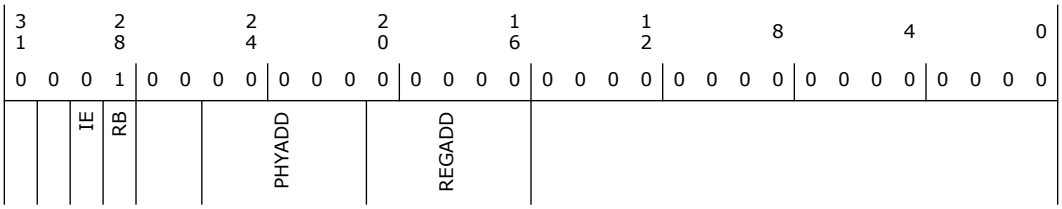
9.2.3 Gigabit Ethernet Capabilities and Status (GBECSR_20)—Offset 20h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 6

Default: 10000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/V	**Wait:** Set to 1 by the Gigabit Ethernet Controller to indicate that a PCI Express* to SMBus transition is taking place. The ME/Host should not issue new MDIC transactions while this bit is set to 1. This bit is auto cleared by hardware after the transition has occurred.
30	0h RW/V	**Error:** Set to 1 by the Gigabit Ethernet Controller when it fails to complete an MDI read. Software should make sure this bit is clear before making an MDI read or write command.
29	0h RW/V	**Interrupt Enable (IE):** hen set to 1 by software, it will cause an Interrupt to be asserted to indicate the end of an MDI cycle.
28	1h RW/V	**Ready Bit (RB):** Set to 1 by the Gigabit Ethernet Controller at the end of the MDI transaction. This bit should be reset to 0 by software at the same time the command is written.
27:26	0h RW/V	**MDI Type:** 01 = MDI Write 10 = MDI Read All other values are reserved.
25:21	0h RW/V	**LAN Connected Device Address (PHYADD)**
20:16	0h RW/V	**LAN Connected Device Register Address (REGADD)**
15:0	0h RW/V	**DATA:** In a Write command, software places the data bits and the MAC shifts them out to the LAN Connected Device. In a Read command, the MAC reads these bits serially from the LAN Connected Device and software can read them from this location.

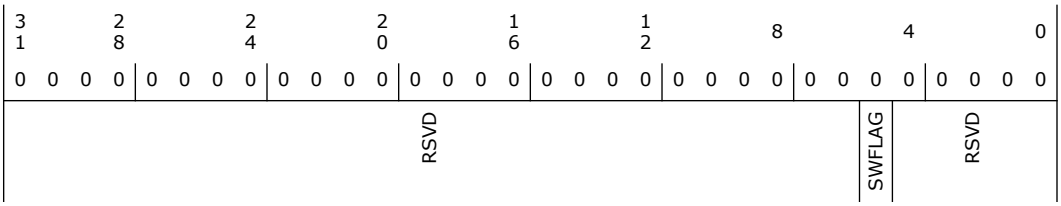
9.2.4 Gigabit Ethernet Capabilities and Status (GBECSR_F00)—Offset F00h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 6

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	Reserved.
5	0h RW/V	**Software Semaphore FLAG (SWFLAG):** This bit is set by the device driver to gain access permission to shared CSR registers with the firmware and hardware.
4:0	0h RO	Reserved.

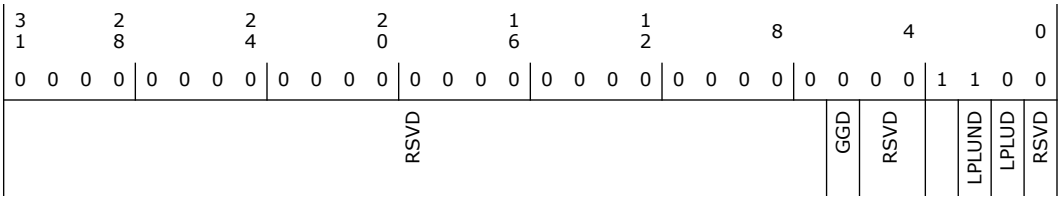
9.2.5 Gigabit Ethernet Capabilities and Status F10 (GBECSR_F10)—Offset F10h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 6

Default: Ch



Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	Reserved.
6	0h RW	**Global GbE Disable (GGD):** Prevents the PHY from auto-negotiating 1000Mb/s link in all power states.
5:4	0h RO	Reserved.
3	1h RW	**GbE Disable at non D0a—:** Prevents the PHY from auto-negotiating 1000Mb/s link in all power states except D0a. This bit must be set since GbE is not supported in Sx states.
2	1h RW	**LPLU in non D0a (LPLUND):** Enables the PHY to negotiate for the slowest possible link in all power states except D0a.
1	0h RW	**LPLU in D0a (LPLUD):** Enables the PHY to negotiate for the slowest possible link in all power states. This bit overrides bit 2.
0	0h RO	Reserved.

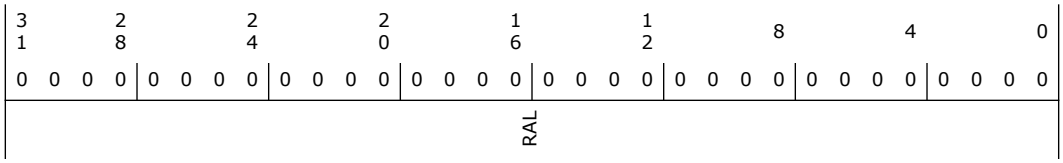
9.2.6 Gigabit Ethernet Capabilities and Status (GBECSR_5400)—Offset 5400h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 6

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Receive Address Low (RAL):** The lower 32 bits of the 48-bit Ethernet Address.

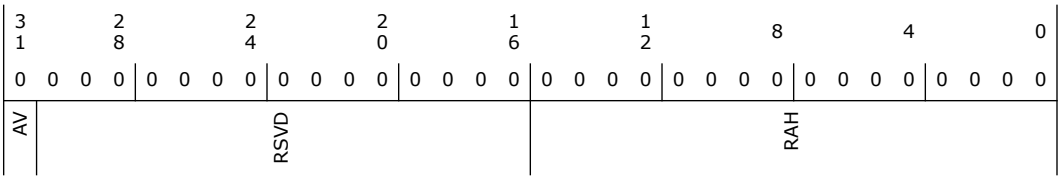
9.2.7 Gigabit Ethernet Capabilities and Status (GBECSR_5404)—Offset 5404h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 6

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Valid (AV)**
30:16	0h RO	Reserved.
15:0	0h RW	**Receive Address High (RAH):** The lower 16 bits of the 48-bit Ethernet Address.

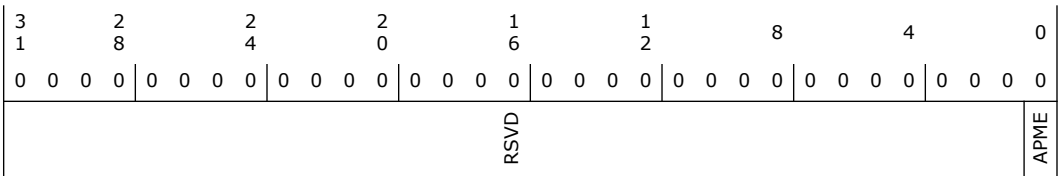
9.2.8 Gigabit Ethernet Capabilities and Status (GBECSR_5800)—Offset 5800h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 6

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RW	**Advanced Power Management Enable (APME):** 1 = APM Wakeup is enabled 0 = APM Wakeup is disabled

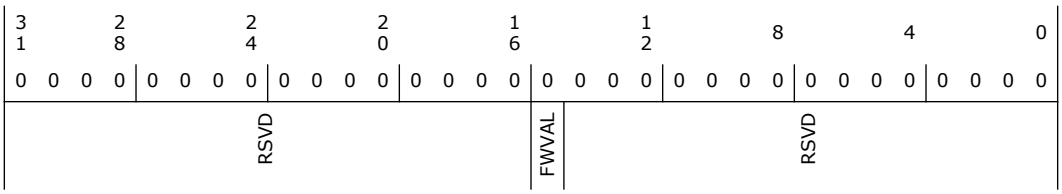
9.2.9 Gigabit Ethernet Capabilities and Status (GBECSR_5B54)—Offset 5B54h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 31
Function: 6

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	0h RW	**Firmware Valid Bit (FWVAL):** 1 = Firmware is ready 0 = Firmware is not ready
14:0	0h RO	Reserved.

§ §

10 Intel® Trace Hub (Intel® TH)

10.1 Intel® Trace Huh Configuration Registers Summary

Table 10-1. Summary of Intel Trace Huh Configuration Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	Vendor and Device Identification (VID)—Offset 0h	XXXX8086h
4h	7h	Command and Status Register (CMD)—Offset 4h	100000h
8h	Bh	Revision ID (RID)—Offset 8h	000013XXh
Ch	Fh	Header Type (HT)—Offset Ch	0h
10h	13h	MTB Low BAR (MTB_LBAR)—Offset 10h	4h
14h	17h	MTB Upper BAR (MTB_UBAR)—Offset 14h	0h
18h	1Bh	SW Low BAR (SW_LBAR)—Offset 18h	4h
1Ch	1Fh	SW Upper BAR (SW_UBAR)—Offset 1Ch	0h
20h	23h	RTIT Low BAR (RTIT_LBAR)—Offset 20h	4h
24h	27h	RTIT Upper BAR (RTIT_UBAR)—Offset 24h	0h
34h	37h	Capabilities Pointer (CAP)—Offset 34h	40h
3Ch	3Fh	Interrupt Line and Interrupt Pin (INTL)—Offset 3Ch	1FFh
40h	43h	MSI Capability (MSICID)—Offset 40h	2800005h
44h	47h	MSI Lower Message Address (MSILMA)—Offset 44h	0h
48h	4Bh	MSI Upper Message Address (MSIUMA)—Offset 48h	0h
4Ch	4Fh	MSI Message Data (MSIMD)—Offset 4Ch	0h
80h	83h	Device Specific Control and Device Specific Status (NPKDSC)—Offset 80h	1h

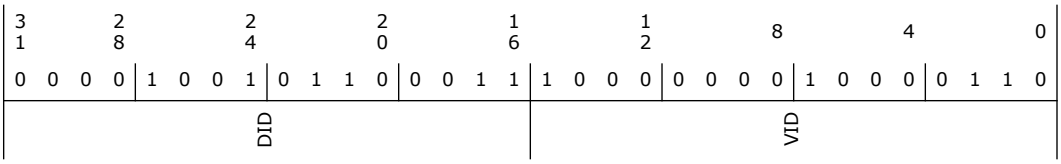
10.1.1 Vendor and Device Identification (VID)—Offset 0h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 7

Default: xxxx8086h



Bit Range	Default & Access	Field Name (ID): Description
31:16	-- RO	**Device ID (DID):** The value that uniquely identifies the Intel(R) Trace Hub from all other PCI devices. See the Device and Version ID Table in Volume 1 for the default value.
15:0	8086h RO	**Vendor ID (VID):** 8086 is Intel Vendor Identification code

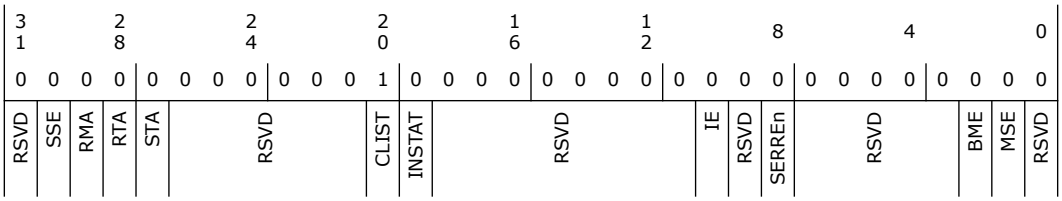
10.1.2 Command and Status Register (CMD)—Offset 4h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 7

Default: 100000h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	Reserved.
30	0h RW/1C	**SSE:** This bit is set when the device has detected an un-correctable error and reported it via SERR message over sideband. This requires SERR Enable bit to be set in Command register.
29	0h RW/1C	**RMA:** This bit is set when device receives a Completion transaction with Unsupported Request completion status. No error will be reported
28	0h RW/1C	**RTA:** This bit is set when device receives a Completion transaction with Completer Abort completion status. No error will be reported
27	0h RW/1C	**STA:** Set by the device when aborting a request that violates the device programming model. When SERR Enable is set SERR message will be send over sideband
26:21	0h RO	Reserved.
20	1h RO	**CLIST:** Indicates the controller contains a capabilities pointer list and the capability pointer register is implemented at offset 0x40 in the configuration space
19	0h RO	**INSTAT:** Interrupt Status: Reflects the state of the interrupt pin at the input of the enable/disable circuit. When the interrupt is asserted, and cleared when the interrupt is cleared (independent of the state of Interrupt Disable bit in command register. This bit is only associated with the INTx messages and has no meaning if the device is using MSI
18:11	0h RO	Reserved.
10	0h RW	**Interrupt Disable (IE):** Disables the function to generate INTx interrupt. A value of 0 enables the function to generate INTA messages on IOSF sideband. Note: this bit has no effect on MSI generation.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RO	Reserved.
8	0h RW	**System Error Enable (SERREn):** Setting this bit enables the generation of System Error message.
7:3	0h RO	Reserved.
2	0h RW	**Bus Master Enable (BME):** When set enables the ability to issue Memory or IO requests, including MSI.
1	0h RW	**Memory Space Enable (MSE):** When set, Memory Space Decoding is enabled and memory transactions targeting the device are accepted. Note: The MSE has to be set to accept any memory transaction on the primary interface targeting any of the Trace Hub's BARs
0	0h RO	Reserved.

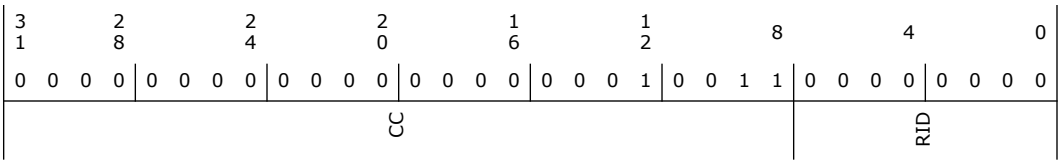
10.1.3 Revision ID (RID)—Offset 8h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 7

Default: 000013XXh



Bit Range	Default & Access	Field Name (ID): Description
31:8	13h RO	**Class Code (CC)**
7:0	-- RO	**Revision ID (RID):** Indicates stepping of the host controller. Refer to Device and Revision ID table in Vol1 for specific value.

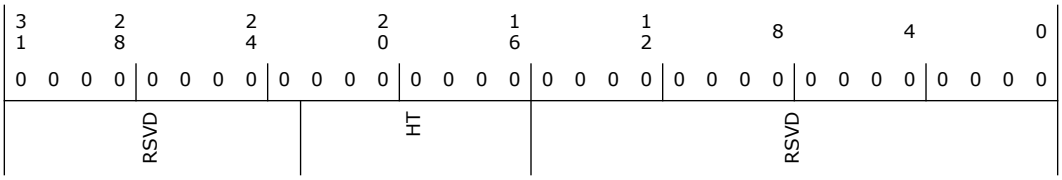
10.1.4 Header Type (HT)—Offset Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 7

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	Reserved.
22:16	0h RO	**Header Type (HT):** Implements a Type 0 configuration header
15:0	0h RO	Reserved.

10.1.5 MTB Low BAR (MTB_LBAR)—Offset 10h

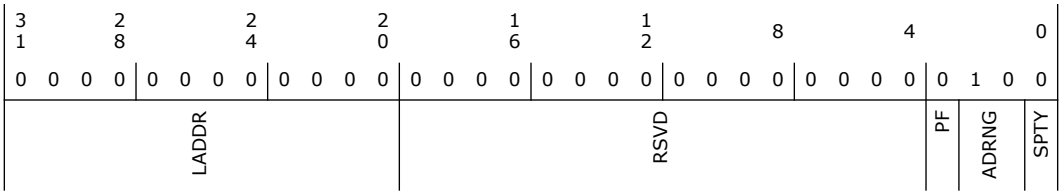
This register sets the lower BAR value for all memory mapped CSRs and the MTB.MSC Trace Buffer

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 7

Default: 4h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**Lower Base Address (LADDR):** Lower programmable Base Address.
19:4	0h RO	Reserved.
3	0h RO	**Prefetchable (PF):** Value of 0 indicates the BAR cannot be prefetched
2:1	2h RO	**Address Range (ADRNG):** Value of 0x2 indicates that the BAR is located anywhere system memory space (i.e. 64-bit addressing)
0	0h RO	**Space Type (SPTY):** Value of 0 indicates the BAR is located in memory space.

10.1.6 MTB Upper BAR (MTB_UBAR)—Offset 14h

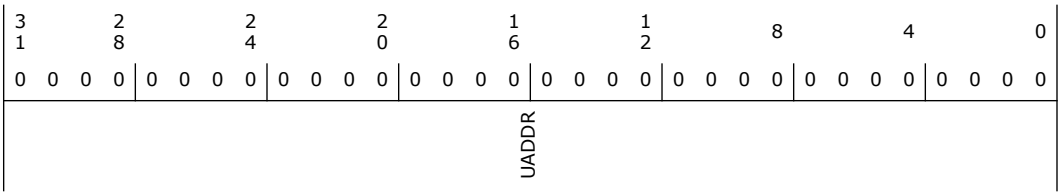
This register sets the upper BAR value for all memory mapped CSRs and the MTB.MSC Trace Buffer

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 7

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Upper Base Address (UADDR):** Upper programmable Base Address

10.1.7 SW Low BAR (SW_LBAR)—Offset 18h

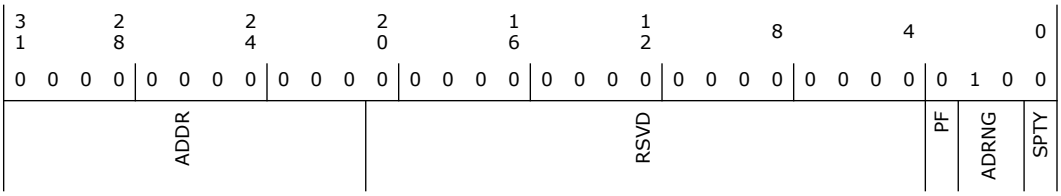
This register sets the lower 32 bits of the BAR value for the STMR STH target.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 7

Default: 4h



Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RW	**Lower Base Address (ADDR):** Lower programmable Base Address
20:4	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RO	**Prefetchable (PF):** Value of 0 indicates the BAR cannot be prefetched
2:1	2h RO	**Address Range (ADRNG):** Value of 0x2 indicates that the BAR is located anywhere system memory space (i.e. 64-bit addressing)
0	0h RO	**Space Type (SPTY):** Value of 0 indicates the BAR is located in memory space

10.1.8 SW Upper BAR (SW_UBAR)—Offset 1Ch

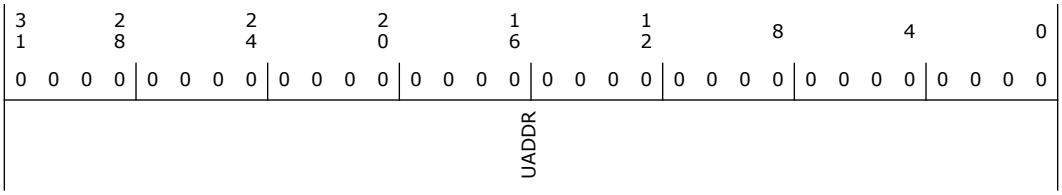
This register sets the upper 32 bits of the BAR value for the STMR STH target.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 7

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Upper Base Address (UADDR):** Upper programmable Base Address

10.1.9 RTIT Low BAR (RTIT_LBAR)—Offset 20h

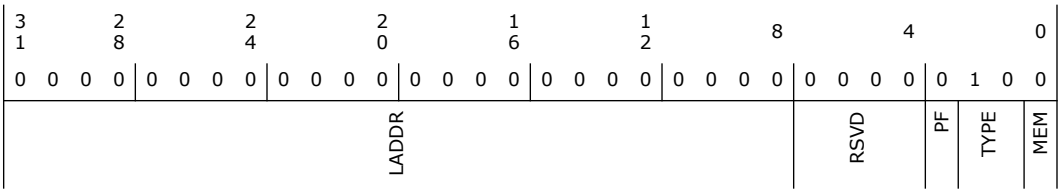
This register sets the lower BAR value for the STH RTIT trace sources. It is to be noted that if the RTIT_PRESENT parameter is not set, this register will become read-only and will return all zeros if read.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 7

Default: 4h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RW	**Lower Base Address (LADDR):** Lower programmable Base Address
7:4	0h RO	Reserved.
3	0h RO	**Prefetchable (PF):** Value of 0 indicates the BAR cannot be prefetched
2:1	2h RO	**Address Range (TYPE):** Value of 0x2 indicates that the BAR is located anywhere system memory space (i.e. 64-bit addressing)
0	0h RO	**Space Type (MEM):** Value of 0 indicates the BAR is located in memory space

10.1.10 RTIT Upper BAR (RTIT_UBAR)—Offset 24h

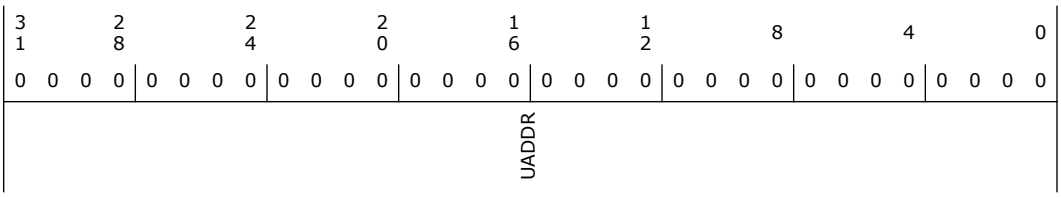
This register sets the upper BAR value for the Software Trace Hub RTIT trace sources. It is to be noted that if the RTIT_PRESENT parameter is not set, this register will become read-only and will return all zeros if read.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 7

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Upper Base Address (UADDR):** Upper programmable Base Address

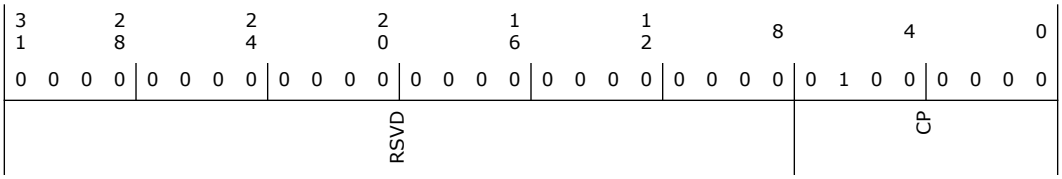
10.1.11 Capabilities Pointer (CAP)—Offset 34h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 7

Default: 40h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	40h RO	**Capability Pointer (CP):** Pointer to first capability structure at 40h

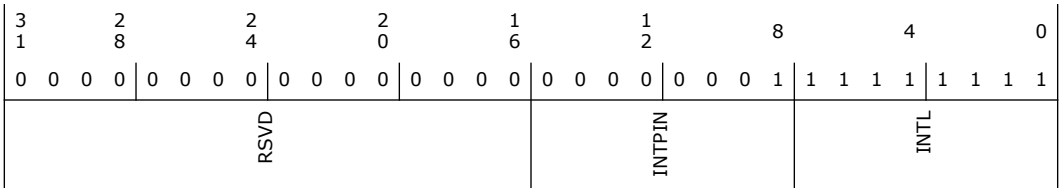
10.1.12 Interrupt Line and Interrupt Pin (INTL)—Offset 3Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 7

Default: 1FFh



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:8	1h RO	**Interrupt Pin (INTPIN):** The Trace Hub uses a single INTx interrupt bonded to INTA
7:0	FFh RW	**Interrupt Line (INTL):** Hardware does not use this field. Rather it is programmed by system software and device drivers to communicate interrupt line routing information

10.1.13 MSI Capability (MSICID)—Offset 40h

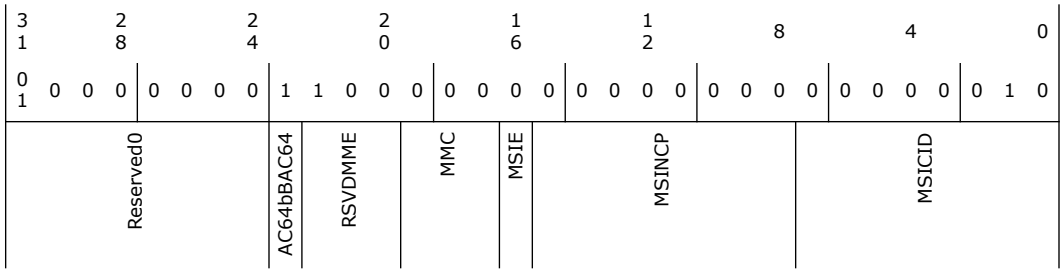
MSI Capability ID,MSI Next Capability Pointer, MSI Message Control Register

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 7

Default: 2800005h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved0**
23	1h RO	**AC64b**
22:24	0h RO	Reserved.
23	1h RO	**64-bit Address Capable (BAC64):** Trace Hub is capable of generating 64-bit memory addresses
22:20	0h RW	**Multiple Message Enable (MME):** Indicates the number of messages allocated to the device
19:17	0h RO	**Multiple Message Capable (MMC):** Value of 0 indicates the device only support single interrupt message
16	0h RW	**MSI Enable (MSIE):** If set, MSI is enabled and the legacy interrupts messages will not be generated
15:8	0h RO	**Multiple Message Enable (MSINCP):** Indicates the number of messages allocated to the device
7:0	5h RO	**MSI Capability ID (MSICID):** A value of 05h indicating the presence of the MSI capability register set

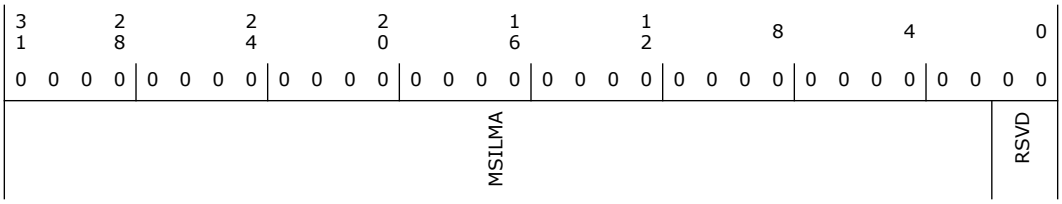
10.1.14 MSI Lower Message Address (MSILMA)—Offset 44h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 7

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**MSI Message Lower Address (MSILMA):** Lower 32-bits of system software assigned message address to the device with bits[1:0] always cleared indicating message address has to always be DW aligned
1:0	0h RO	Reserved.

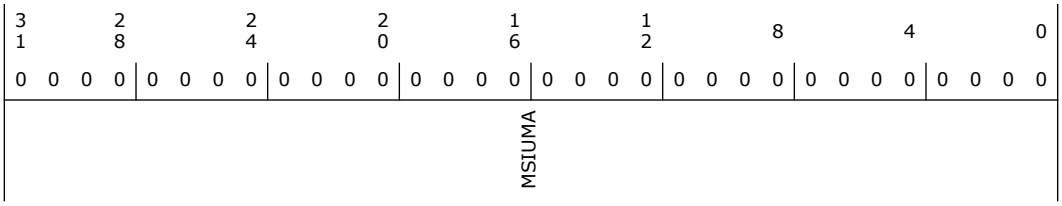
10.1.15 MSI Upper Message Address (MSIUMA)—Offset 48h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 7

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**MSI Message Upper Address (MSIUMA):** Upper 32-bits of system software assigned message address to the device

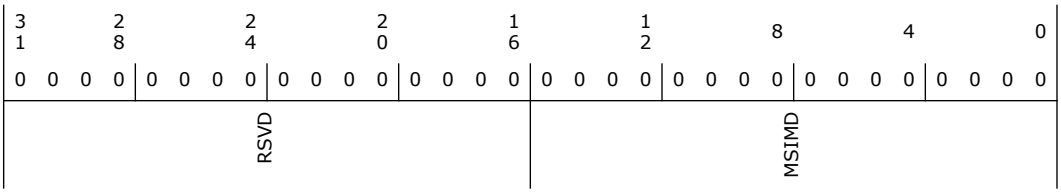
10.1.16 MSI Message Data (MSIMD)—Offset 4Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 7

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	0h RW	**MSI Message Data (MSIMD):** 16-bit message data pattern assigned by the system software to the device. When MSI is generated the actual data is 32-bit and the upper 16 bits are always 0

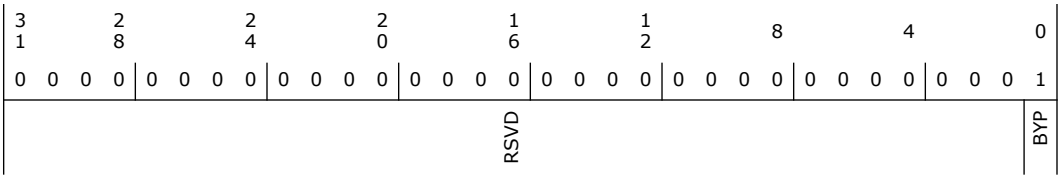
10.1.17 Device Specific Control and Device Specific Status (NPKDSC)—Offset 80h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 7

Default: 1h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	1h RW	**Trace Hub Bypass (BYP):** If set, the Trace Hub logic will be bypassed

§ §

11 UART Interface (D30:F0/F1 and D25:F0)

11.1 UART PCI Configuration Registers Summary

Table 11-1. Summary of UART PCI Configuration Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	Device ID and Vendor ID Register (DEVVENDID)—Offset 0h	XXXX8086
4h	7h	Status and Command (STATUSCOMMAND)—Offset 4h	100000h
8h	Bh	Revision ID and Class Code (REVCLASSCODE)—Offset 8h	118000XXh
Ch	Fh	Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch	0h
10h	13h	Base Address Register (BAR)—Offset 10h	0h
14h	17h	Base Address Register High (BAR_HIGH)—Offset 14h	0h
18h	1Bh	Base Address Register 1 (BAR1)—Offset 18h	0h
1Ch	1Fh	Base Address Register1 High (BAR1_HIGH)—Offset 1Ch	0h
2Ch	2Fh	Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch	0h
30h	33h	Expansion ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h	0h
34h	37h	Capabilities Pointer (CAPABILITYPTR)—Offset 34h	80h
3Ch	3Fh	Interrupt Register (INTERRUPTREG)—Offset 3Ch	100h
80h	83h	Power Management Capability ID (POWERCAPID)—Offset 80h	00030001h
84h	87h	PME Control and Status (PMECTRLSTATUS)—Offset 84h	8h
90h	93h	PCI Device Idle Capability Record (PCIDEVIDLE_CAP_RECORD)—Offset 90h	F0140009h
98h	9Bh	SW LTR Update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG)—Offset 98h	0h
9Ch	9Fh	Device IDLE pointer register (DEVICE_IDLE_POINTER_REG)—Offset 9Ch	0h
A0h	A3h	Device PG Config (D0I3_MAX_POW_LAT_PG_CONFIG)—Offset A0h	800h

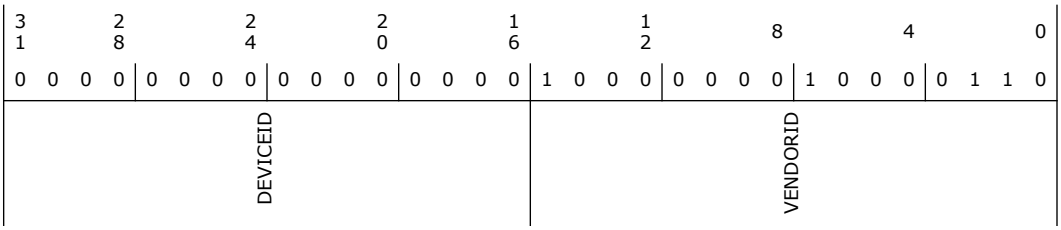
11.1.1 Device ID and Vendor ID Register (DEVVENDID)—Offset 0h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 0

Default: xxxx8086



Bit Range	Default & Access	Field Name (ID): Description
31:16	-- RO	**Device ID (DEVICEID):** This is a 16-bit value assigned to the controller. See the Device and Version ID Table in Volume 1 for the default value.
15:0	8086h RO	**Vendor ID (VENDORID):** Identifies the manufacturer of the device.

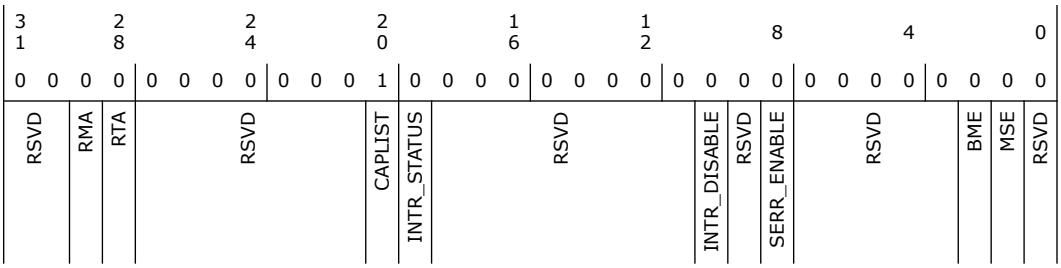
11.1.2 Status and Command (STATUSCOMMAND)—Offset 4h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 100000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29	0h RW/1C	**Received Master Abort (RMA):** If the completion status received from is UR, this bit is set. S/W writes a '1' to this bit to clear it.
28	0h RW/1C	**Received Target Abort (RTA):** If the completion status received is CA, this bit is set. S/W writes a '1' to this bit to clear it.
27:21	0h RO	Reserved.
20	1h RO	**Capabilities List (CAPLIST):** Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h.

Bit Range	Default & Access	Field Name (ID): Description
19	0h RO	**Interrupt Status (INTR_STATUS):** This bit reflects state of interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the device's/function's interrupt message be sent. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. This bit reflects Legacy interrupt status.
18:11	0h RO	Reserved.
10	0h RW	**Interrupt Disable (INTR_DISABLE):** Setting this bit disables INTx assertion. The interrupt disabled is legacy INTx# interrupt.
9	0h RO	Reserved.
8	0h RW	**SERR# Enable (SERR_ENABLE):** Not implemented
7:3	0h RO	Reserved.
2	0h RW	**Bus Master Enable (BME)**
1	0h RW	**Memory Space Enable (MSE):** 0 = Disables memory mapped Configuration space. 1 = Enables memory mapped Configuration space.
0	0h RO	Reserved.

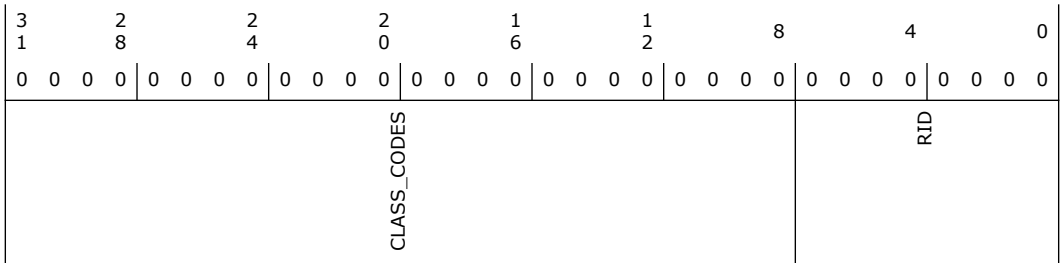
11.1.3 Revision ID and Class Code (REVCLASSCODE)—Offset 8h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 118000XXh



Bit Range	Default & Access	Field Name (ID): Description
31:8	118000h RO	**Class Codes (CLASS_CODES):** The register is read-only and is used to identify the generic function of the device.
7:0	-- RO	**Revision ID (RID):** Indicates stepping of the host controller. Refer to Device and Revision ID table in Vol1 for specific value.

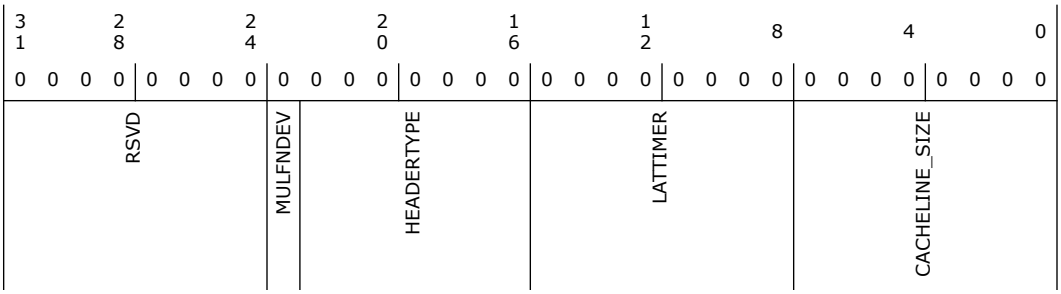
11.1.4 Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RO	**Multi Function Device (MULFNDEV):** 0 = Single Function Device 1 = Multi Function device
22:16	0h RO	**Header Type (HEADERTYPE):** Implements Type 0 Configuration header.
15:8	0h RO	**Latency Timer (LATTIMER).** Hardwired to 00h
7:0	0h RW	**Cache Line Size (CACHELINE_SIZE)**

11.1.5 Base Address Register (BAR)—Offset 10h

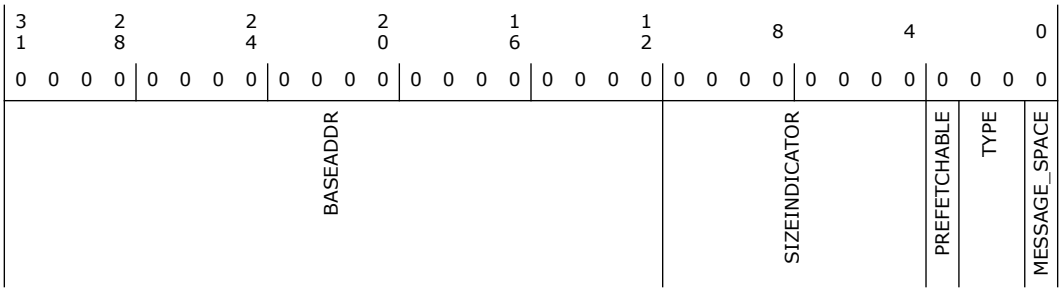
Bits [31:12] indicate the Base Address register. Power-up software can determine how much address space the Interface Module requires by writing a value of all ones to the register and then reading the value back. The register returns zeros in all don't-care address bits, effectively specifying the address space required.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW	**Base Address (BASEADDR):** Provides system memory base address for the controller.
11:4	0h RO	**Size Indicator (SIZEINDICATOR)**
3	0h RO	**Prefetchable (PREFETCHABLE):** Indicates that this BAR is not prefetchable.
2:1	0h RO	**Type (TYPE):** 00 indicates BAR lies in 32bit address range 10 Indicates BAR lies in 64 bit address range
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE):** '0' Indicates this BAR is present in the memory space.

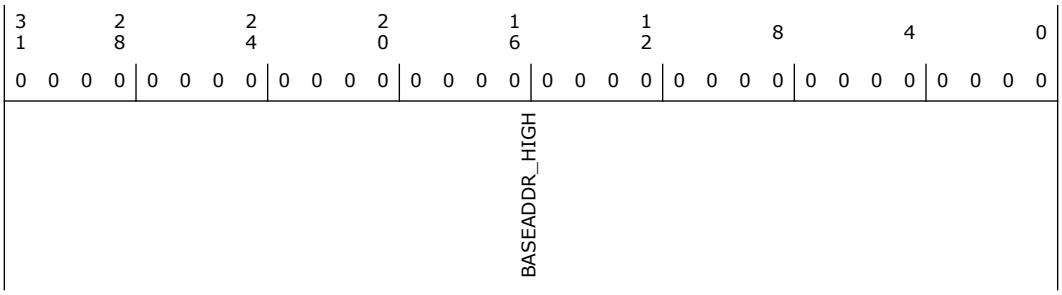
11.1.6 Base Address Register High (BAR_HIGH)—Offset 14h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Base Address High (BASEADDR_HIGH)**

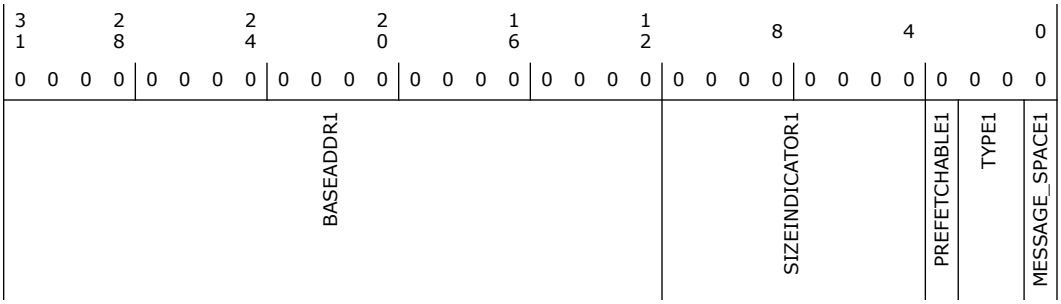
11.1.7 Base Address Register 1 (BAR1)—Offset 18h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW	**Base Address Register1 (BASEADDR1):** This field is present if BAR1 is enabled.
11:4	0h RO	**Size Indicator (SIZEINDICATOR1):** Always will be zero as minimum size is 4K.
3	0h RO	**Prefetchable (PREFETCHABLE1):** Indicates that this BAR is not prefetchable.
2:1	0h RO	**Type (TYPE1):** 00 indicates BAR lies in 32bit address range 10 Indicates BAR lies in 64 bit address range.
0	0h RO	**MESSAGE_SPACE1**

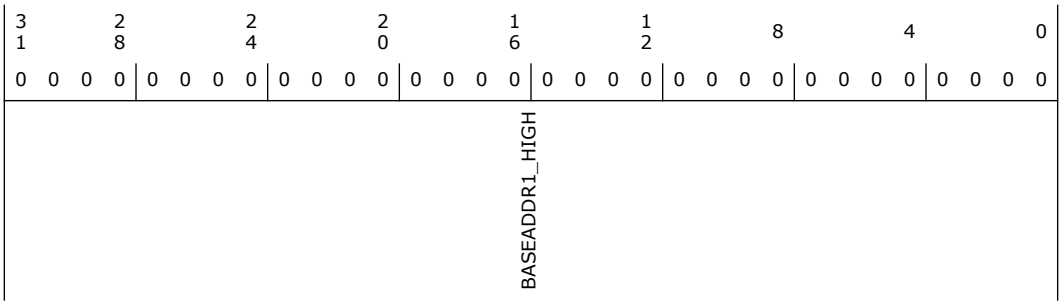
11.1.8 Base Address Register1 High (BAR1_HIGH)—Offset 1Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Base Address High 1 (BASEADDR1_HIGH)**

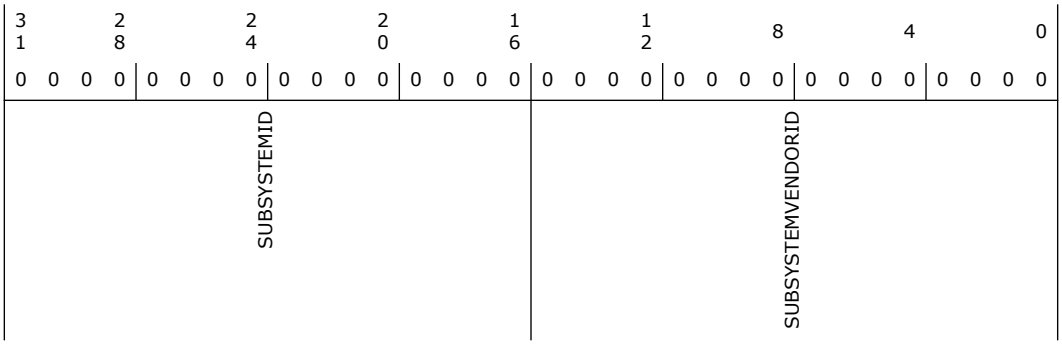
11.1.9 Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW/O	**Subsystem ID (SUBSYSTEMID):** The register, in combination with the Subsystem Vendor ID register make it possible for the operating environment to distinguish one subsystem from the other. This register is a Read Write Once type register.
15:0	0h RW/O	**Subsystem Vendor ID (SUBSYSTEMVENDORID):** The register, in combination with the Subsystem ID register, enables the operating environment to distinguish one subsystem from the other. This register is a Read Write Once register.

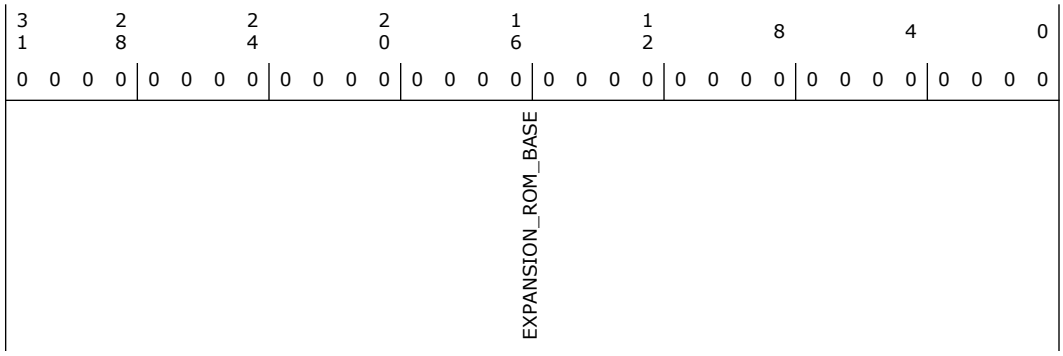
11.1.10 Expansion ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**Expansion ROM Base (EXPANSION_ROM_BASE):** Value of 0 indicates no support for Expansion ROM

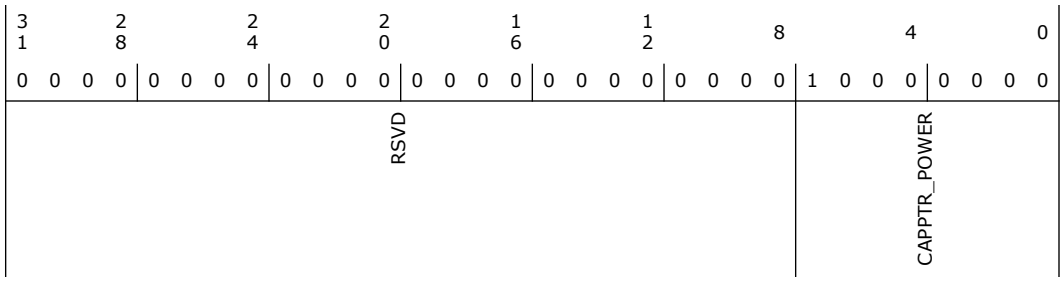
11.1.11 Capabilities Pointer (CAPABILITYPTR)—Offset 34h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 80h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	80h RO	**Capabilities Pointer (CAPPTR_POWER):** Indicates what the next capability is. This capability points to the PM Capability (0x80) structure.

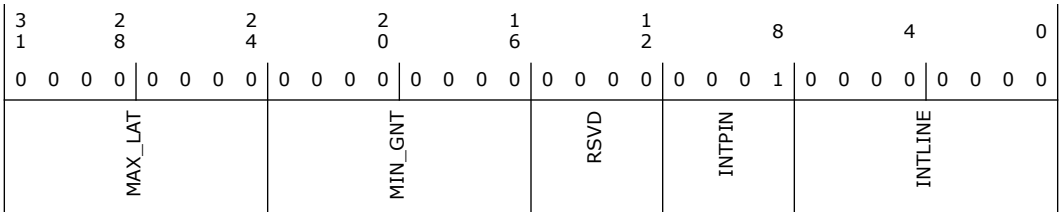
11.1.12 Interrupt Register (INTERRUPTREG)—Offset 3Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 100h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Max Latency (MAX_LAT):** Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	0h RO	**Min Latency (MIN_GNT):** Value of 0 indicates device has no major requirements for the settings of latency timers
15:12	0h RO	Reserved.
11:8	1h RO	**Interrupt Pin (INTPIN)**
7:0	0h RW	**Interrupt Line (INTLINE):** Used to communicate to software the interrupt line that the interrupt pin is connected to.

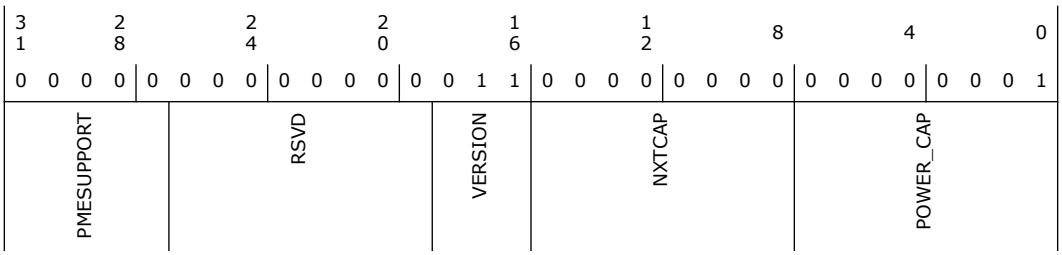
11.1.13 Power Management Capability ID (POWERCAPID)—Offset 80h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 48030001h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**PME Support (PMESUPPORT)**
26:19	0h RO	Reserved.
18:16	3h RO	**Version (VERSION):** Indicates support for Revision 1.2 of the PCI Power Management Specification
15:8	0h RO	**Next Capability (NXTCAP):** Points to the next capability structure. This points to NULL.
7:0	1h RO	**Power Management Capability (POWER_CAP):** Indicates power management capability.

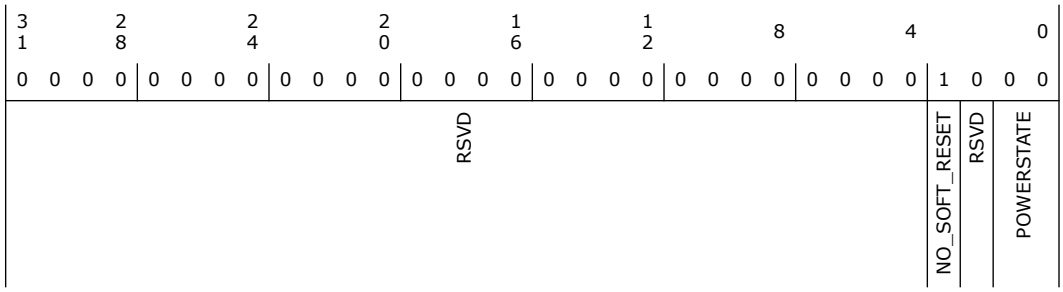
11.1.14 PME Control and Status (PMECTRLSTATUS)—Offset 84h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 8h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3	1h RO	**No Soft Reset (NO_SOFT_RESET):** When set, this bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved.
2	0h RO	Reserved.
1:0	0h RW	**Power State (POWERSTATE):** This field is used both to determine the current power state and to set a new power state. The values are: 00 = D0 state 11 = D3HOT state Others = Reserved Notes: If software attempts to write a value of 01b or 10b in to this field,the data is discarded and no state change occurs. When in the D3HOT states, interrupts are blocked.

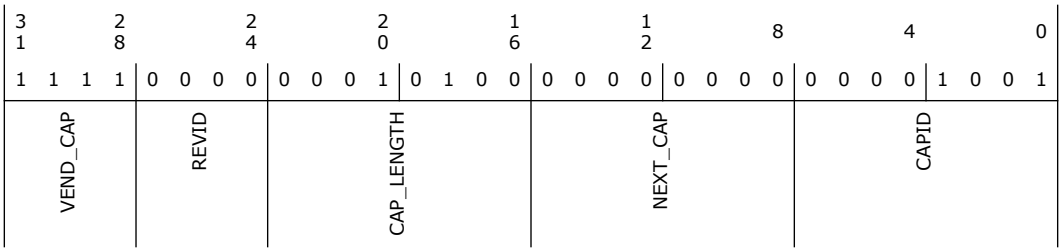
11.1.15 PCI Device Idle Capability Record (PCIDEVIDLE_CAP_RECORD)—Offset 90h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 0

Default: F0140009h



Bit Range	Default & Access	Field Name (ID): Description
31:28	Fh RO	**Vendor Capability (VEND_CAP):** Indicates this is Vendor Specific capability.
27:24	0h RO	**Revision ID (REVID):** Revision ID of capability structure
23:16	14h RO	**Length (CAP_LENGTH):** Indicates the number of bytes in the capability structure.
15:8	0h RO	**Next Capability (NEXT_CAP):** Points to the next capability structure. This points to NULL.
7:0	9h RO	**Capability ID (CAPID)**

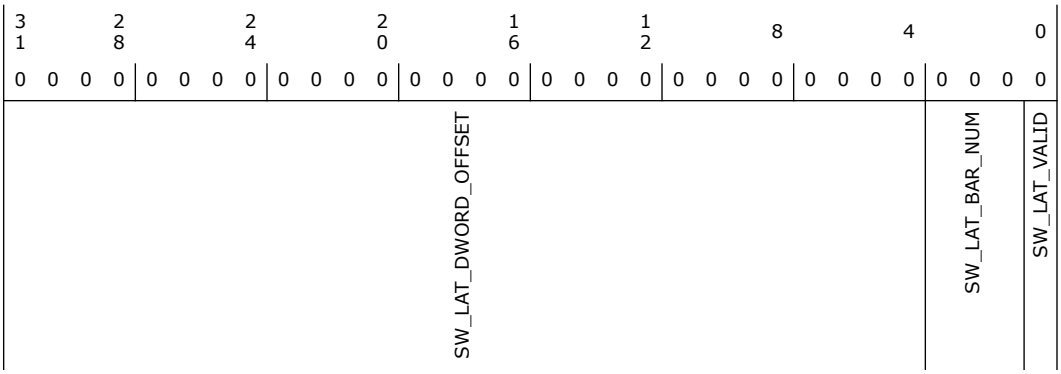
11.1.16 SW LTR Update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG)—Offset 98h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Location Pointer Offset (SW_LAT_DWORD_OFFSET):** This register contains the location pointer to the SW LTR register in MMIO space, as an offset from the specified BAR. The value of this register is a don't care, if the Valid bit is not set.
3:1	0h RO	**BAR Number (SW_LAT_BAR_NUM):** Indicates that the SW LTR update MMIO location is always at BAR0.
0	0h RO	**Valid (SW_LAT_VALID)**

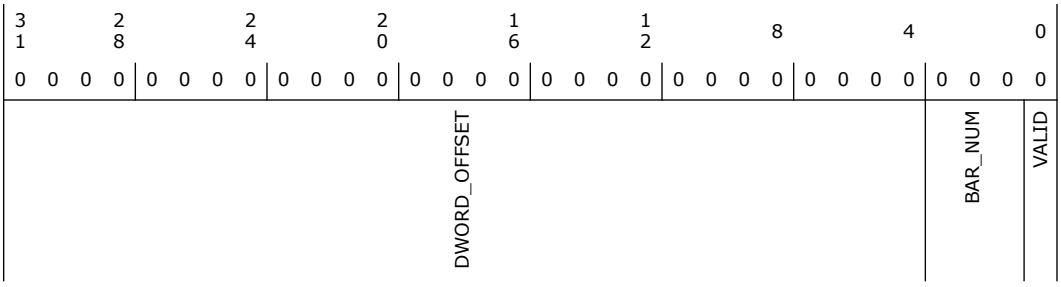
11.1.17 Device IDLE pointer register (DEVICE_IDLE_POINTER_REG)—Offset 9Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**DevIdle Pointer (DWORD_OFFSET):** This register contains the location pointer to the DevIdle register in MMIO space, as an offset from the specified BAR. The value of this register is a don't care, if the Valid bit is not set.
3:1	0h RO	**BAR Number (BAR_NUM):** Indicates that the DevIdle update MMIO location is always at BAR0
0	0h RO	**Valid (VALID):** 0= not valid 1= valid

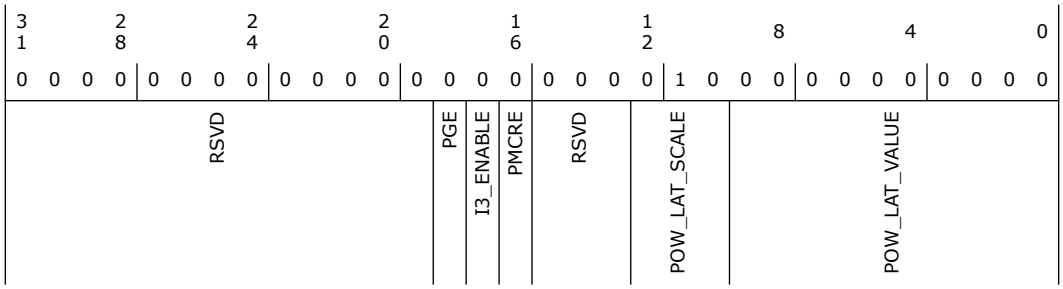
11.1.18 Device PG Config (D0I3_MAX_POW_LAT_PG_CONFIG)—Offset A0h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 800h



Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	Reserved.
18	0h RW	**PG Enable (PGE):** If clear, then the controller will never request a PG. If set, then the controller may request PG when proper conditions are met. Note: This Bit must be set by BIOs for PG to function
17	0h RW	**I3 Enable (I3_ENABLE):** If '1', then the function will power gate when idle and the DevIdle register (DevIdleC[2] = '1') is set.
16	0h RW	**PMC Request Enable (PMCRE):** If this bit is set to '1', the function will power gate when idle.
15:13	0h RO	Reserved.
12:10	2h RW/O	**Power On Latency Scale (POW_LAT_SCALE):** Support for codes 010 (1us) or 011 (32us) for Exit Latency Scale (1us - 32ms total span) only. This value is written by BIOS to communicate to the Driver.
9:0	0h RW/O	**Power On Latency Value (POW_LAT_VALUE):** This value is written by BIOS to communicate to the Driver.

11.2 UART Memory Mapped Registers Summary

The registers in this section are memory-mapped registers based on the BAR defined in PCH Configuration space.

Table 11-2. Summary of UART Memory Mapped Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	Receive Buffer Register (RBR)—Offset 0h	0h
0h	3h	Transmit Holding Register (THR)—Offset 0h	0h
0h	3h	Divisor Latch Low Register (DLL)—Offset 0h	0h
4h	7h	Interrupt Enable Register (IER)—Offset 4h	0h
4h	7h	Divisor Latch High (DLH)—Offset 4h	0h
8h	Bh	Interrupt Identification (IIR)—Offset 8h	0h
8h	Bh	FIFO Control (FCR)—Offset 8h	1h
Ch	Fh	Line Control Register (LCR)—Offset Ch	0h
10h	13h	MCR (MCR)—Offset 10h	0h
14h	17h	LSR (LSR)—Offset 14h	60h
18h	1Bh	MSR (MSR)—Offset 18h	0h
1Ch	1Fh	SCR (SCR)—Offset 1Ch	0h
30h	33h	SRBR_STHR0 (SRBR_STHR0)—Offset 30h	0h
70h	73h	FAR (FAR)—Offset 70h	0h
74h	77h	TFR (TFR)—Offset 74h	0h
78h	7Bh	RFW (RFW)—Offset 78h	0h
7Ch	7Fh	USR (USR)—Offset 7Ch	6h
80h	83h	TFL (TFL)—Offset 80h	0h
84h	87h	RFL (RFL)—Offset 84h	0h
88h	8Bh	SRR (SRR)—Offset 88h	0h
8Ch	8Fh	SRTS (SRTS)—Offset 8Ch	0h
90h	93h	SBCR (SBCR)—Offset 90h	0h
94h	97h	SDMAM (SDMAM)—Offset 94h	0h
98h	9Bh	SFE (SFE)—Offset 98h	0h
9Ch	9Fh	SRT (SRT)—Offset 9Ch	0h
A0h	A3h	STET (STET)—Offset A0h	0h
A4h	A7h	HTX (HTX)—Offset A4h	0h
A8h	ABh	DMASA (DMASA)—Offset A8h	0h
F4h	F7h	CPR (CPR)—Offset F4h	43F32h

11.2.1 Receive Buffer Register (RBR)—Offset 0h

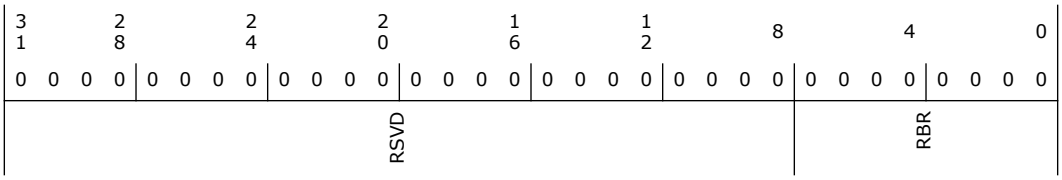
RBR mode is only available when LCR register, DLAB bit = 0.

Access Method

Type: MEM Register (Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	0h RO	**Receive Buffer (RBR):** Data byte received on the serial input port in UART mode. The data in this register is valid only if the Data Ready (DR) bit in the Line Status Register (LCR) is set. If FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an over-run error. If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO is preserved, but any incoming data are lost and an over-run error occurs.

11.2.2 Transmit Holding Register (THR)—Offset 0h

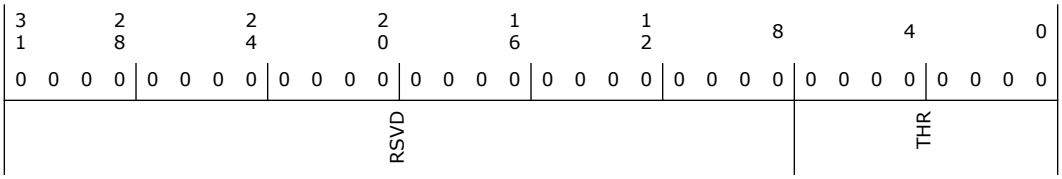
THR mode is only available when LCR register, DLAB bit = 0.

Access Method

Type: MEM Register (Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	0h WO	**Transmit Holding Register (THR):** Data to be transmitted on the serial output port in UART mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If FIFOs are disabled (FCR[0] = 0) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If FIFOs are enabled (FCR[0] = 1) and THRE is set, 64 characters of data may be written to the THR before the FIFO is full. Any attempt to write data when the FIFO is full results in the write data being lost.

11.2.3 Divisor Latch Low Register (DLL)—Offset 0h

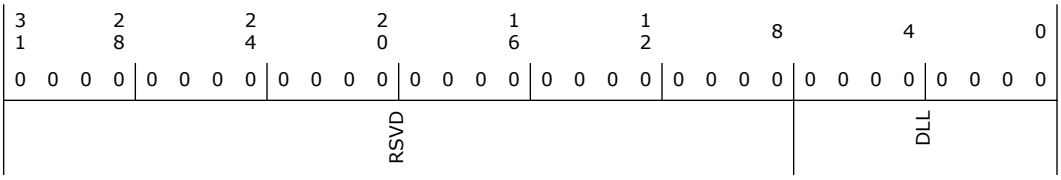
DLL mode is only available when LCR register, DLAB bit = 1.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	0h RW	**Devisor Latch Low (DLL):** Lower 8 bits of a 16-bit, read/write Divisor Latch register that contains the baud rate divisor for the UART. This register may be accessed only when the DLAB bit (LCR[7]) is set. The output baud rate is equal to the serial clock frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock freq) / (16 * divisor). Note that with the Divisor Latch Registers (DLL and DLH) set to zero, the baud clock is disabled and no serial communications occur.

11.2.4 Interrupt Enable Register (IER)—Offset 4h

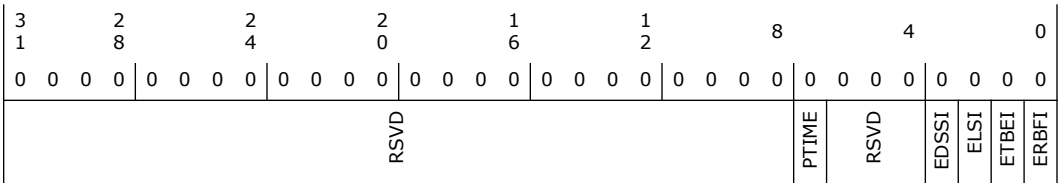
IER mode is only available when LCR register [7] (DLAB bit) = 0.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7	0h RW	**PTIME (PTIME):** THRE Interrupt Mode Enable: This is used to enable/disable the generation of THRE Interrupt. 0 = disabled 1 = enabled
6:4	0h RO	Reserved.
3	0h RW	**EDSSI (EDSSI):** Enable Modem Status Interrupt: This is used to enable/disable the generation of Modem Status Interrupt. This is the fourth highest priority interrupt. 0 = disabled 1 = enabled
2	0h RW	**ELSI (ELSI):** Enable Receiver Line Status Interrupt. This is used to enable/disable the generation of Receiver Line Status Interrupt. This is the highest priority interrupt. 0 = disabled 1 = enabled
1	0h RW	**ETBEI (ETBEI):** Enable Transmit Holding Register Empty Interrupt. This is used to enable/disable the generation of Transmitter Holding Register Empty Interrupt. This is the third highest priority interrupt. 0 = disabled 1 = enabled
0	0h RW	**ERBFI (ERBFI):** Enable Received Data Available Interrupt. This is used to enable/disable the generation of Received Data Available Interrupt and the Character Timeout Interrupt (if in FIFO mode and FIFOs enabled). These are the second highest priority interrupts. 0 = disabled 1 = enabled

11.2.5 Divisor Latch High (DLH)—Offset 4h

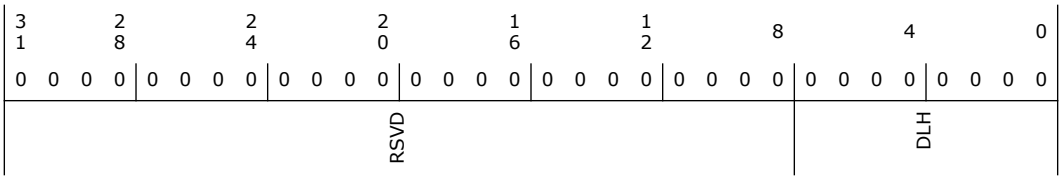
DLH mode is only available when LCR register [7] (DLAB bit) = 1

Access Method

Type: MEM Register (Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	0h RW	**Devisor Latch High (DLH):** Upper 8-bits of a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART. This register may be accessed only when the DLAB bit (LCR[7]) is set. The output baud rate is equal to the serial clock frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock freq) / (16 * divisor). Note that with the Divisor Latch Registers (DLL and DLH) set to zero, the baud clock is disabled and no serial communications occur.

11.2.6 Interrupt Identification (IIR)—Offset 8h

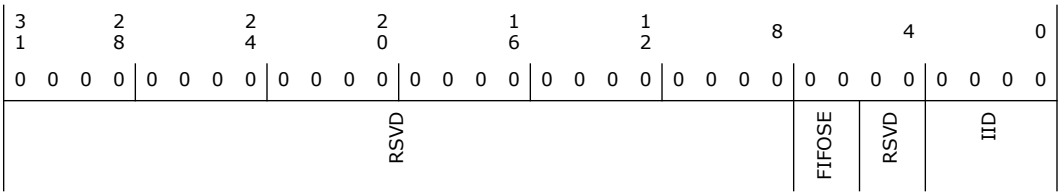
Note that the register can also be used as FIFO Control Register (FCR) when it is written to.

Access Method

Type: MEM Register (Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:6	0h RO	**FIFOSE (FIFOSE):** FIFOs Enabled. This is used to indicate whether the FIFOs are enabled or disabled. 00 = disabled 11 = enabled
5:4	0h RO	Reserved.
3:0	0h RO	**Interrupt ID. (IID):** This indicates the highest priority pending interrupt which can be one of the following types: 0000 = modem status 0001 = no interrupt pending 0010 = THR empty 0100 = received data available 0110 = receiver line status 0111 = busy detect 1100 = character timeout Note: An interrupt of type 0111 (busy detect) is never indicated because the controller is compatible with UART_16550 mode. Bit 3 indicates an interrupt can only occur when the FIFOs are enabled and used to distinguish a Character Timeout condition interrupt.

11.2.7 FIFO Control (FCR)—Offset 8h

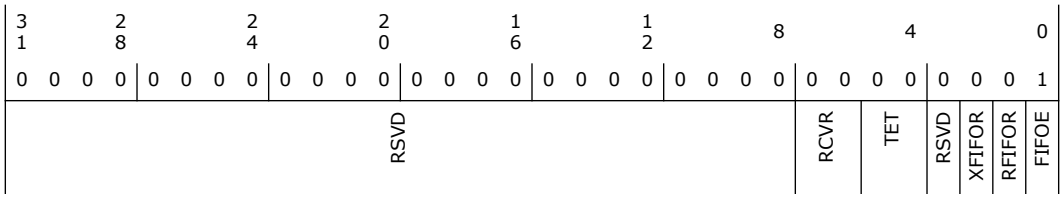
Note that the register can also be used as Interrupt Identification register (IIR)when it is read from.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 1h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:6	0h WO	**RCVR Trigger (RCVR):** This is used to select the trigger level in the receiver FIFO at which the Received Data Available Interrupt is generated. The following trigger levels are supported: 00 = 1 character in the FIFO 01 = FIFO ¼ full 10 = FIFO ½ full 11 = FIFO 2 less than full
5:4	0h WO	**TX Empty Trigger (TET):** This is used to select the empty threshold level at which the THRE Interrupts are generated when the mode is active. The following trigger levels are supported: 00 = FIFO empty 01 = 2 characters in the FIFO 10 = FIFO ¼ full 11 = FIFO ½ full
3	0h RO	Reserved.
2	0h WO	**XMIT FIFO Reset (XFIFOR):** This resets the control portion of the transmit FIFO and treats the FIFO as empty. Note that this bit is 'self-clearing'. It is not necessary to clear this bit.
1	0h WO	**RCVR FIFO Reset (RFIFOR):** This resets the control portion of the receive FIFO and treats the FIFO as empty. Note that this bit is 'self-clearing'. It is not necessary to clear this bit.
0	1h WO	**FIFOs Enabled (FIFOE):** This is used to indicate whether the FIFOs are enabled or disabled. 00 = disabled 11 = enabled

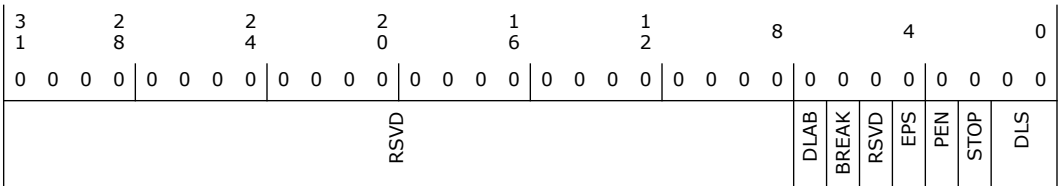
11.2.8 Line Control Register (LCR)—Offset Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7	0h RW	**Divisor Latch Access Bit (DLAB):** This bit is used to enable reading and writing of the Divisor Latch register(DLL and DLH) to set the baud rate of the UART. This bit must be cleared after initialbaud rate setup in order to access other registers
6	0h RW	**Break Control Bit (BREAK):** This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the serial out line is forced low until the Break bit is cleared. If SIR_MODE == Enabled and active (MCR[6] set to one) the sir_out_n line is continuously pulsed. When in Loopback Mode, the break condition is internally looped back to the receiver and the sir_out_n line is forced low.
5	0h RO	Reserved.
4	0h RW	**Even Parity Select (EPS):** Even Parity Select. If UART_16550_COMPATIBLE == NO, then writeable only when UART is not busy (USR[0] is zero); otherwise always writable, always readable. This is used to select between even and odd parity, when parity is enabled (PEN set to one). If set to one, an even number of logic 1s is transmitted or checked. If set to zero, an odd number of logic 1s is transmitted or checked. Reset Value: 0x0
3	0h RW	**Parity Enable (PEN):** Parity Enable. This bit is used to enable and disable parity generation and detection in transmitted and received serial character respectively. 0 = parity disabled 1 = parity enabled
2	0h RW	**Number of Stop Bits (STOP):** This is used to select the number of stop bits per character that the peripheral transmits and receives. If set to zero, one stop bit is transmitted in the serial data. If set to one and the data bits are set to 5 (LCR[1:0] set to zero) one and a half stop bits is transmitted. Otherwise, two stop bits are transmitted. Note that regardless of the number of stop bits selected, the receiver checks only the first stop bit. 0 = 1 stop bit 1 = 1.5 stop bits when DLS (LCR[1:0]) is zero, else 2 stop bit
1:0	0h RW	**Data Length Select (DLS):** This is used to select the number of data bits per character that the peripheral transmits and receives. The number of bit that may be selected areas follows: 00 = 5 bits 01 = 6 bits 10 = 7 bits 11 = 8 bits

11.2.9 MCR (MCR)—Offset 10h

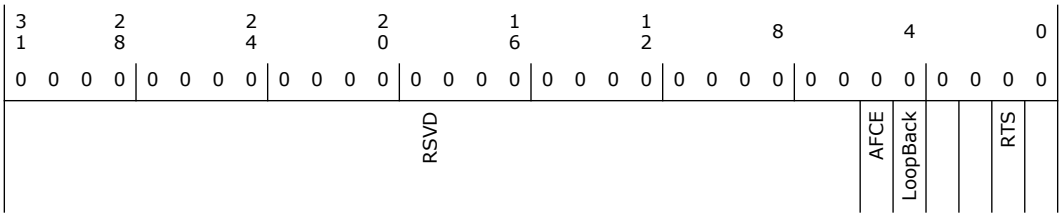
Modem Control Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	Reserved.
5	0h RW	**AFCE (AFCE):** Auto Flow Control Enable. When FIFOs are enabled and the Auto Flow Control Enable (AFCE) bit is set. The bit is used to help for flow control using external IO pins with the pairing device. 0 = Auto Flow Control Mode disabled 1 = Auto Flow Control Mode enabled
4	0h RW	**LoopBack (LoopBack):** LoopBack Bit. This is used to put the UART into a diagnostic mode for test purposes. Data on the serial out line is held high, while serial data output is looped back to the serial in line, internally. In this mode all the interrupts are fully functional. Also, in loop back mode, the modem control input (cts_n,) are disconnected and the modem control output (rts_n) are looped back to the inputs, internally.
3	0h RW	**Reserved**
2	0h RW	**Reserved**
1	0h RW	**RTS (RTS):** Request to Send. This is used to directly control the Request to Send (rts_n) output. The Request To Send output is used to inform the modem or data set that the UART is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] set to zero), the rts_n signal is set low by programming MCR[1] (RTS) to a high. In Auto Flow Control, (MCR[5] set to one) and FIFOs enable (FCR[0] set to one), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). The rts_n signal is de-asserted when MCR[1] is set low. Note that in Loopback mode (MCR[4] set to one), the rts_n output is held inactive high while the value of this location is internally looped back to an input.
0	0h RW	**Reserved**

11.2.10 LSR (LSR)—Offset 14h

Line Status Register

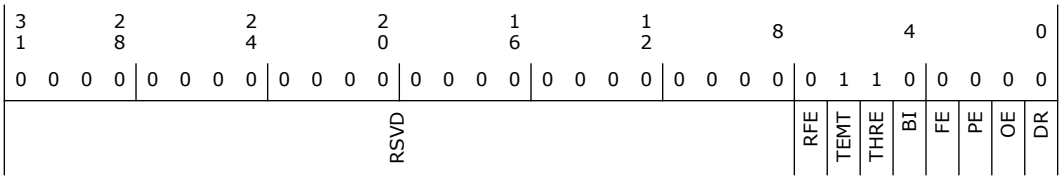
Access Method

Type: MEM Register (Size: 32 bits)

Device: 30

Function: 0

Default: 60h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7	0h RW	**RFE (RFE):** Receiver FIFO Error bit. This bit is only relevant when FIFOs are enabled (FCR[0] set to one). This is used to indicate if there is at least one parity error, framing error, or break indication in the FIFO. 0 = no error in RX FIFO 1 = error in RX FIFO This bit is cleared when the LSR is read and the character with the error is at the top of the receiver FIFO and there are no subsequent errors in the FIFO
6	1h RW	**TEMT (TEMT):** Transmitter Empty bit. If FIFOs enabled(FCR[0] set to one), this bit is set whenever the Transmitter Shift Register and the FIFO are both empty. If FIFOs are disabled, this bit is set whenever the Transmitter Holding Register and the Transmitter Shift Register are both empty.
5	1h RW	**THRE (THRE):** Transmit Holding Register Empty bit. If THRE mode is disabled (IER[7] set to zero) and regardless of FIFO's being implemented/enabled or not, this bit indicates that the THR or TX FIFO is empty. This bit is set whenever data is transferred from the THR or TX FIFO to the transmitter shift register and no new data has been written to the THR or TX FIFO. This also causes a THRE Interrupt to occur, if the THRE Interrupt is enabled. If both THRE Interrupt and FIFO modes are active (IER[7] set to one and FCR[0] set to one respectively), the functionality is switched to indicate the transmitter FIFO is full, and no longer controls THRE interrupts, which are then controlled by the FCR[5:4] threshold setting
4	0h RW	**BI (BI):** Break Interrupt bit. This is used to indicate the detection of a break sequence on the serial input data. It is set whenever the serial input (sin) is held in a logic '0' state for longer than the sum of start time + data bits + parity + stop bits. A break condition on serial input causes one and only one character, consisting of all zeros, to be received by the UART. In the FIFO mode, the character associated with the break condition is carried through the FIFO and is revealed when the character is at the top of the FIFO. Reading the LSR clears the BI bit. In the non-FIFO mode, the BI indication occurs immediately and persists until the LSR is read.
3	0h RW	**FE (FE):** Framing Error bit. This is used to indicate the occurrence of a framing error in the receiver. A framing error occurs when the receiver does not detect a valid STOP bit in the received data. In the FIFO mode, since the framing error is associated with a character received, it is revealed when the character with the framing error is at the top of the FIFO. When a framing error occurs, the UART tries to resynchronize. It does this by assuming that the error was due to the start bit of the next character and then continues receiving the other bit i.e. data, and/or parity and stop. It should be noted that the Framing Error (FE) bit(LSR[3]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit(LSR[4]). 0 = no framing error 1 = framing error Reading the LSR clears the FE bit.
2	0h RW	**PE (PE):** Parity Error bit. This is used to indicate the occurrence of a parity error in the receiver if the Parity Enable (PEN) bit (LCR[3]) is set. In the FIFO mode, since the parity error is associated with a character received, it is revealed when the character with the parity error arrives at the top of the FIFO. It should be noted that the Parity Error (PE) bit (LSR[2]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). 0 = no parity error 1 = parity error Reading the LSR clears the PE bit.
1	0h RW	**OE (OE):** Overrun error bit. This is used to indicate the occurrence of an overrun error. This occurs if a new data character was received before the previous data was read. In the non-FIFO mode, the OE bit is set when a new character arrives in the receiver before the previous character was read from the RBR. When this happens, the data in the RBR is overwritten. In the FIFO mode, an overrun error occurs when the FIFO is full and anew character arrives at the receiver. The data in the FIFO is retained and the data in the receive shift register is lost. 0 = no overrun error 1 = overrun error Reading the LSR clears the OE bit.
0	0h RW	**DR (DR):** Data Ready bit. This is used to indicate that the receiver contains at least one character in the RBR or the receiver FIFO. 0 = no data ready 1 = data ready This bit is cleared when the RBR is read in non-FIFO mode, or when the receiver FIFO is empty, in FIFO mode.

11.2.11 MSR (MSR)—Offset 18h

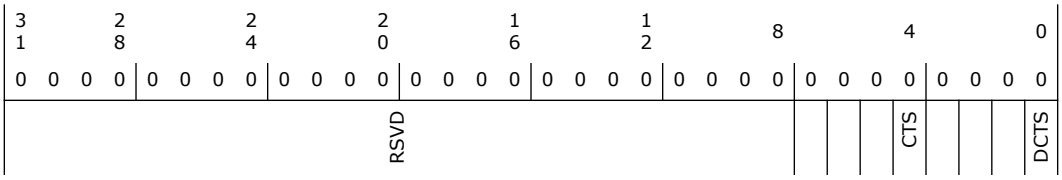
Modem Status Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7	0h RO	**Reserved**
6	0h RO	**Reserved**
5	0h RO	**Reserved**
4	0h RO	**CTS (CTS):** Clear to Send. This is used to indicate the current state of the modem control line cts_n.This bit is the complement of cts_n. When the Clear to Send input (cts_n) is asserted it isan indication that the modem or data set is ready to exchange data with the UART. 0 = cts_n input is de-asserted (logic 1) 1 = cts_n input is asserted (logic 0) In Loopback Mode (MCR[4] = 1), CTS is the same as MCR[1] (RTS).
3	0h RO	**Reserved**
2	0h RO	**Reserved**
1	0h RO	**Reserved**
0	0h RO	**DCTS (DCTS):** Delta Clear to Send. This is used to indicate that the modem control line cts_n has changed since the last time the MSR was read. 0 = no change on cts_n since last read of MSR 1 = change on cts_n since last read of MSR Reading the MSR clears the DCTS bit. In Loopback Mode (MCR[4] = 1), DCTS reflects changes on MCR[1] (RTS).Note, if the DCTS bit is not set and the cts_n signal is asserted (low) and a reset occurs(software or otherwise), then the DCTS bit is set when the reset is removed if the cts_nsignal remains asserted.

11.2.12 SCR (SCR)—Offset 1Ch

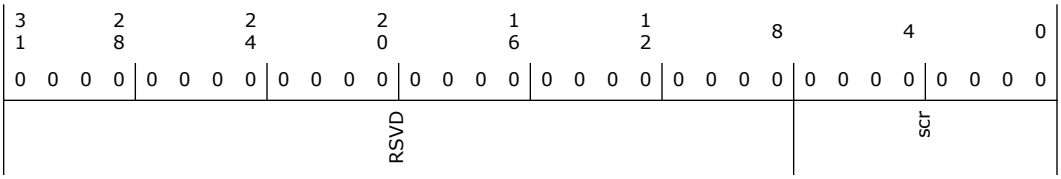
Scratchpad Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	0h RW	**scr (scr):** This register is for programmers to use as a temporary storage space.

11.2.13 SRBR_STHR0 (SRBR_STHR0)—Offset 30h

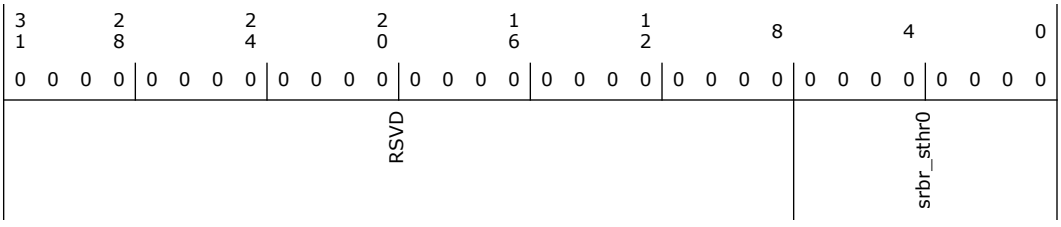
NOTE: There are a total of 16 Shadow Receive Buffer Registers (SRBR_STHR[15:0]. The register description is the same for all of them. The other registers are at the following offsets:
SRBR_STHR1 at offset 34h
SRBR_STHR2 at offset 38h
SRBR_STHR3 at offset 3Ch
.....
SRBR_STHR14 at offset 68h
SRBR_STHR15 at offset 6Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	0h RW	**srbr_sthr0 (srbr_sthr0):** Used as SRBR: This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an overrun error. If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO are preserved, but any incoming data is lost. An overrun error also occurs. Used as STHR: This is a shadow register for the THR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If FIFOs are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If FIFOs are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost.

11.2.14 FAR (FAR)—Offset 70h

FIFO Access Register

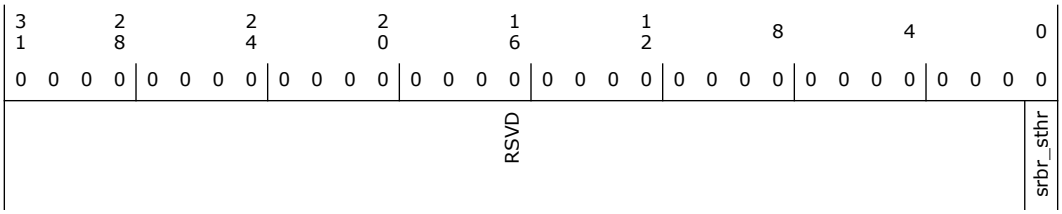
Access Method

Type: MEM Register (Size: 32 bits)

Device: 30

Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RW	**srbr_sthr (srbr_sthr):** Writes have no effect when FIFO_ACCESS == No, always readable. This register is use to enable a FIFO access mode for testing, so that the receive FIFO can be written by the master and the transmit FIFO can be read by the master when FIFOs are implemented and enabled. When FIFOs are not implemented or not enabled it allows the RBR to be written by the master and the THR to be read by the master. 0 = FIFO access mode disabled 1 = FIFO access mode enabled Note, that when the FIFO access mode is enabled/disabled, the control portion of the receive FIFO and transmit FIFO is reset and the FIFOs are treated as empty. Reset Value: 0x0

11.2.15 TFR (TFR)—Offset 74h

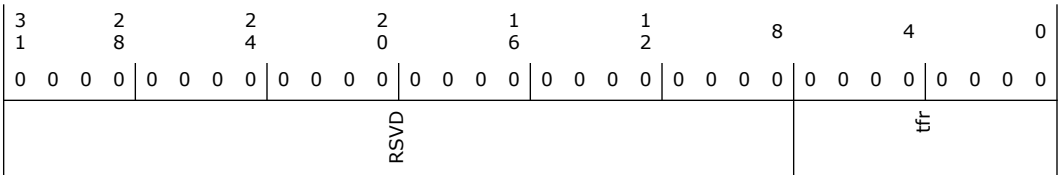
Transmit FIFO Read

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	0h RW	**tfr (tfr):** Transmit FIFO Read. These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are implemented and enabled, reading this register gives the data at the top of the transmit FIFO. Each consecutive read pops the transmit FIFO and gives the next data value that is currently at the top of the FIFO. When FIFOs are not implemented or not enabled, reading this register gives the data in the THR. Reset Value: 0x0

11.2.16 RFW (RFW)—Offset 78h

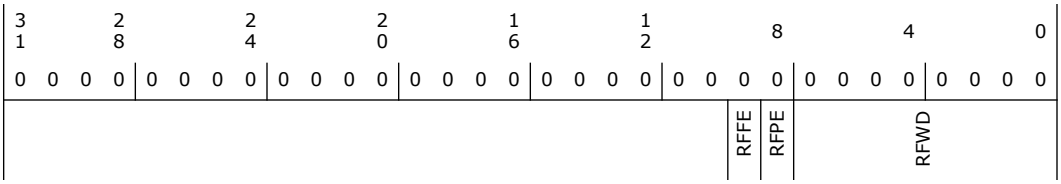
Receive FIFO Write

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0h na	**Reserved**
9	0h WO	**RFFE (RFFE):** Receive FIFO Framing Error. These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are enabled, this bit is used to write framing error detection information to the receive FIFO. When FIFOs are not implemented or not enabled, this bit is used to write framing error detection information to the RBR.
8	0h WO	**RFPE (RFPE):** Receive FIFO Parity Error. These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are enabled, this bit is used to write parity error detection information to the receive FIFO. When FIFOs are not implemented or not enabled, this bit is used to write parity error detection information to the RBR.
7:0	0h WO	**RFWD (RFWD):** Receive FIFO Write Data. These bits are only valid when FIFO access mode is enabled(FAR[0] is set to one). When FIFOs are enabled, the data that is written to the RFWD is pushed into the receive FIFO. Each consecutive write pushes the new data to the next write location in the receive FIFO. When FIFOs are not implemented or not enabled, the data that is written to the RFWD is pushed into the RBR.

11.2.17 USR (USR)—Offset 7Ch

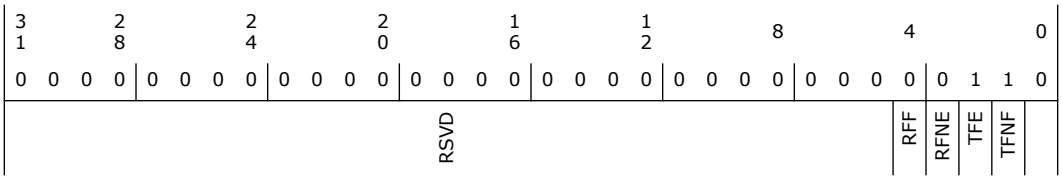
UART Status Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 6h



Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4	0h RO	**RFF (RFF):** Receive FIFO Full. This is used to indicate that the receive FIFO is completely full. 0 = Receive FIFO not full 1 = Receive FIFO Full This bit is cleared when the RX FIFO is no longer full.
3	0h RO	**RFNE (RFNE):** Receive FIFO Not Empty. This is used to indicate that the receive FIFO contains one or more entries. 0 = Receive FIFO is empty 1 = Receive FIFO is not empty This bit is cleared when the RX FIFO is empty.

Bit Range	Default & Access	Field Name (ID): Description
2	1h RO	**TFE (TFE):** Transmit FIFO Empty. This is used to indicate that the transmit FIFO is completely empty. 0 = Transmit FIFO is not empty 1 = Transmit FIFO is empty This bit is cleared when the TX FIFO is no longer empty
1	1h RO	**TFNF (TFNF):** Transmit FIFO Not Full. This is used to indicate that the transmit FIFO in not full. 0 = Transmit FIFO is full 1 = Transmit FIFO is not full This bit is cleared when the TX FIFO is full.
0	0h RO	**Reserved**

11.2.18 TFL (TFL)—Offset 80h

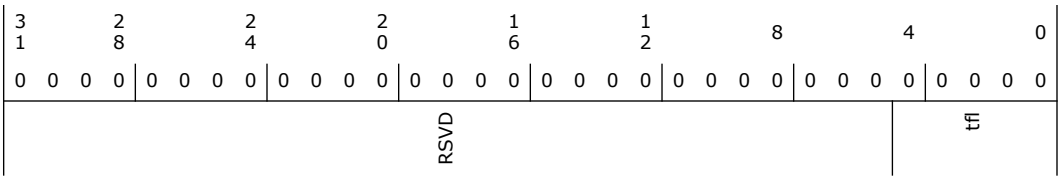
Transmit FIFO Level

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4:0	0h RO	**tfl (tfl):** Transmit FIFO Level. This is indicates the number of data entries in the transmit FIFO. Reset Value: 0x0

11.2.19 RFL (RFL)—Offset 84h

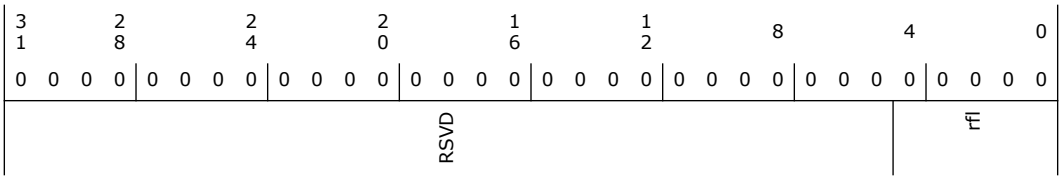
Receive FIFO Level

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4:0	0h RO	**rfl (rfl):** Receive FIFO Level. This is indicates the number of data entries in the receive FIFO. Reset Value: 0x0

11.2.20 SRR (SRR)—Offset 88h

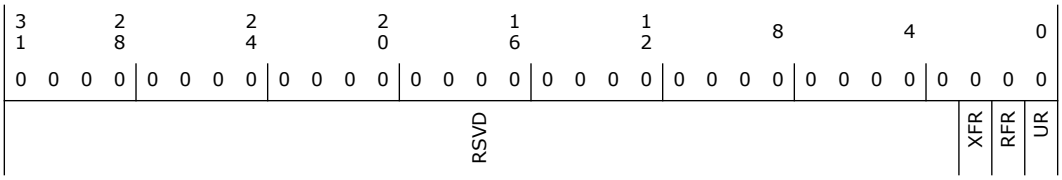
Software Reset Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	Reserved.
2	0h RW	**XFR (XFR):** XMIT FIFO Reset. This is a shadow register for the XMIT FIFO Reset bit (FCR[2]). This can be used to remove the burden on software having to store previously written FCR values (which are pretty static) just to reset the transmit FIFO. This resets the control portion of the transmit FIFO and treats the FIFO as empty. Note that this bit is 'self-clearing'. It is not necessary to clear this bit.
1	0h RW	**RFR (RFR):** RCVR FIFO Reset. This is a shadow register for the RCVR FIFO Reset bit (FCR[1]). This can be used to remove the burden on software having to store previously written FCR values (which are pretty static) just to reset the receive FIFO This resets the control portion of the receive FIFO and treats the FIFO as empty. Note that this bit is 'self-clearing'. It is not necessary to clear this bit.
0	0h RW	**UR (UR):** UART Reset. This asynchronously resets the UART controller and synchronously removes the reset assertion.

11.2.21 SRTS (SRTS)—Offset 8Ch

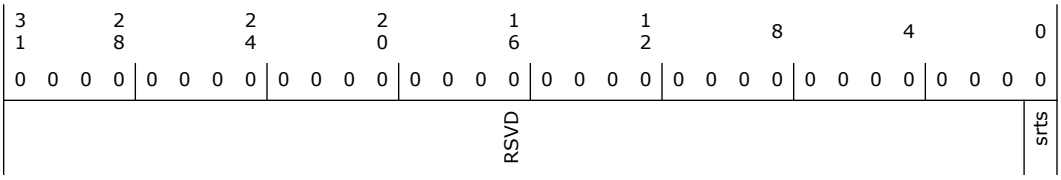
Shadow Request to Send

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RW	**srts (srts):** Shadow Request to Send. This is a shadow register for the RTS bit (MCR[1]), this can be used to remove the burden of having to performing a read-modify-write on the MCR. This is used to directly control the Request to Send (rts_n) output. The Request To Send (rts_n) output is used to inform the modem or data set that the DW_apb_uart is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] = 0), the rts_n signal is set low by programming MCR[1] (RTS) to a high. In Auto Flow Control, AFCE_MODE == Enabled and active (MCR[5] = 1) and FIFOs enable (FCR[0] = 1), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). Note that in Loopback mode (MCR[4] = 1), the rts_n output is held inactive-high while the value of this location is internally looped back to an input. Reset Value: 0x0

11.2.22 SBCR (SBCR)—Offset 90h

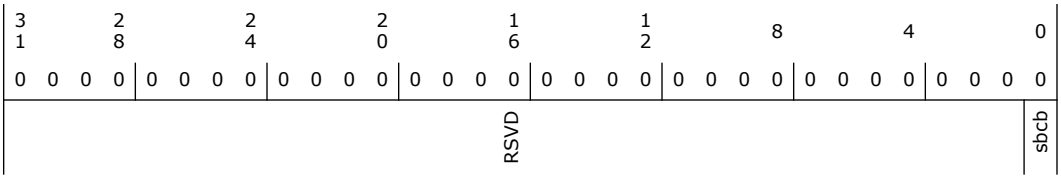
Shadow Break Control Bit

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RW	**sbcb (sbcb):** Shadow Break Control Register. This is a shadow register for the Break bit (LCR[6]), this can be used to remove the burden of having to performing a read modify write on the LCR. This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared. When in Loopback Mode, the break condition is internally looped back to the receiver.

11.2.23 SDMAM (SDMAM)—Offset 94h

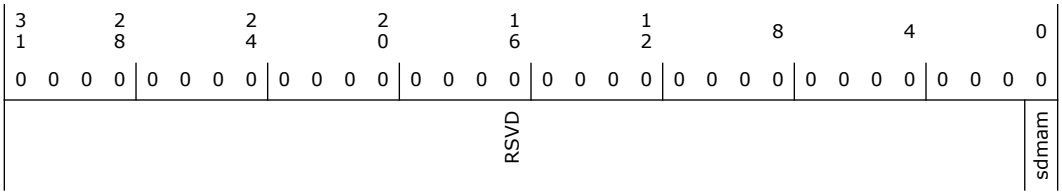
Shadow DMA Mode

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RW	**sdmam (sdmam):** Shadow DMA Mode. This is a shadow register for the DMA mode bit (FCR[3]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the DMA Mode bit gets updated. 0 = mode 0 1 = mode 1

11.2.24 SFE (SFE)—Offset 98h

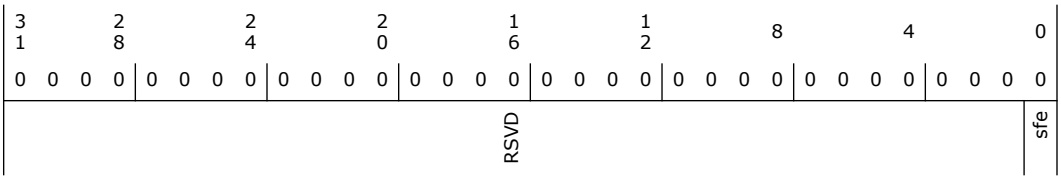
Shadow FIFO Enable

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RW	**sfe (sfe):** Shadow FIFO Enable. This is a shadow register for the FIFO enable bit (FCR[0]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the FIFO enable bit gets updated.This enables/disables the transmit (XMIT) and receive (RCVR) FIFOs. If this bit is set to zero (disabled) after being enabled then both the XMIT and RCVR controller portion of FIFOs are reset. Reset Value: 0x0

11.2.25 SRT (SRT)—Offset 9Ch

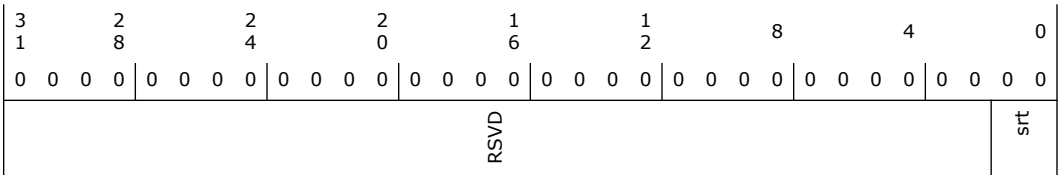
Shadow RCVR Trigger

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RW	**srt (srt):** Shadow RCVR Trigger. This is a shadow register for the RCVR trigger bits(FCR[7:6]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the RCVR trigger bit gets updated. This is used to select the trigger level in the receiver FIFO at which the Received Data Available Interrupt is generated. It also determines when the dma_rx_req_n signal is asserted when DMA Mode (FCR[3]) = 1. The following trigger levels are supported: 00 = 1 character in the FIFO 01 = FIFO ¼ full 10 = FIFO ½ full 11 = FIFO 2 less than full

11.2.26 STET (STET)—Offset A0h

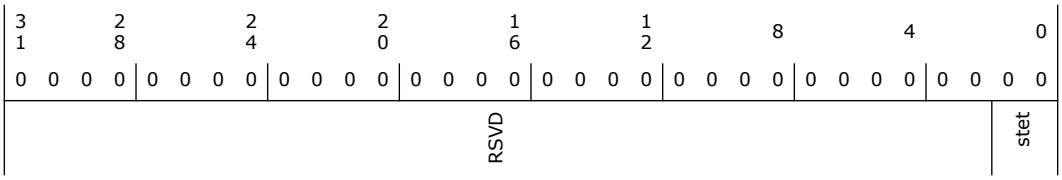
Shadow TX Empty Trigger. This is a shadow register for the TX empty trigger bits(FCR[5:4]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the TXempty trigger bit gets updated. This is used to select the empty threshold level at which the THRE Interrupts are generated when the mode is active.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RW	**stet (stet):** Shadow TX Empty Trigger: This is a shadow register for the TX empty trigger bits(FCR[5:4]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the TX empty trigger bit gets updated. 165 This is used to select the empty threshold level at which the THRE Interrupts are generated when the mode is active. The following trigger levels are supported: 00 = FIFO empty 01 = 2 characters in the FIFO 10 = FIFO ¼ full 11 = FIFO ½ full

11.2.27 HTX (HTX)—Offset A4h

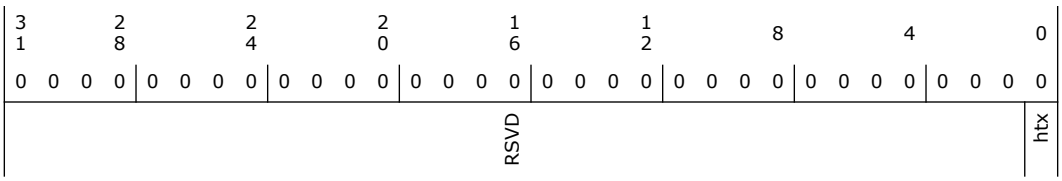
Halt TX

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RW	**htx (htx):** This register is use to halt transmissions for testing, so that the transmit FIFO can be filled by the master when FIFOs are implemented and enabled. 0 = Halt TX disabled 1 = Halt TX enabled Note, if FIFOs are not enabled, the setting of the halt TX register has no effect on operation.

11.2.28 DMASA (DMASA)—Offset A8h

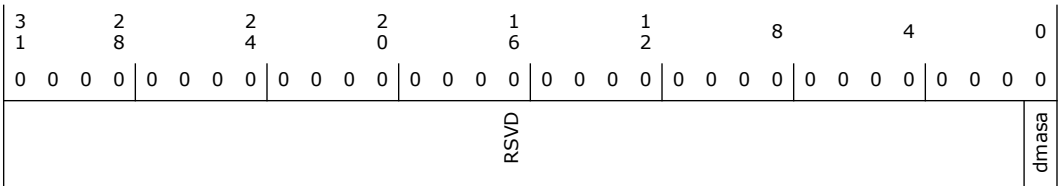
DMA Software Acknowledge

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h WO	**dmasa (dmasa):** This register is use to perform a DMA software acknowledge if a transfer needs to be terminated due to an error condition. For example, if the DMA disables the channel, then the UART should clear its request. This causes the TX request, TX single, RX request and RX single signals to de-assert. Note that this bit is 'self-clearing'. It is not necessary to clear this bit.

11.2.29 CPR (CPR)—Offset F4h

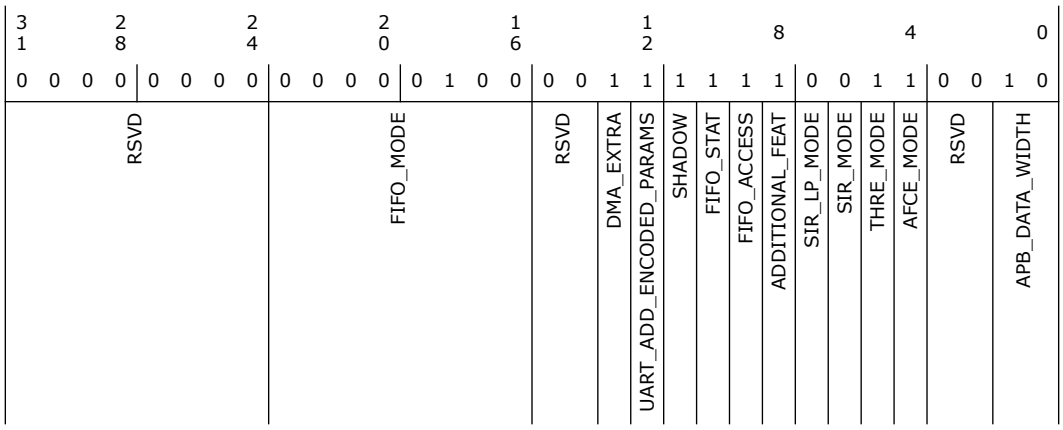
Component Parameter Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 43F32h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:16	4h RO	**FIFO_MODE (FIFO_MODE):** 0x00 = 0 0x01 = 16 0x02 = 32 to 0x80 = 2048 0x81-0xff = reserved
15:14	0h RO	Reserved.
13	1h RO	**DMA_EXTRA (DMA_EXTRA):** 0 = FALSE, 1 = TRUE
12	1h RO	**UART_ADD_ENCODED_PARAMS (UART_ADD_ENCODED_PARAMS):** 0 = FALSE, 1 = TRUE
11	1h RO	**SHADOW (SHADOW):** 0 = FALSE, 1 = TRUE
10	1h RO	**FIFO_STAT (FIFO_STAT):** 0 = FALSE, 1 = TRUE
9	1h RO	**FIFO_ACCESS (FIFO_ACCESS):** 0 = FALSE, 1 = TRUE
8	1h RO	**ADDITIONAL_FEAT (ADDITIONAL_FEAT):** 0 = FALSE, 1 = TRUE
7	0h RO	**SIR_LP_MODE (SIR_LP_MODE):** 0 = FALSE, 1 = TRUE
6	0h RO	**SIR_MODE (SIR_MODE):** 0 = FALSE, 1 = TRUE
5	1h RO	**THRE_MODE (THRE_MODE):** 0 = FALSE, 1 = TRUE
4	1h RO	**AFCE_MODE (AFCE_MODE):** 0 = FALSE, 1 = TRUE
3:2	0h RO	Reserved.
1:0	2h RO	**APB_DATA_WIDTH (APB_DATA_WIDTH):** 00 = 8 bits 01 = 16 bits 10 = 32 bits 11 = reserved

11.3 UART Additional Registers Summary

The registers in this section are memory-mapped registers based on the BAR defined in PCH Configuration space.

Table 11-3. Summary of UART Additional Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
200h	203h	CLOCKS (CLOCKS)—Offset 200h	0h
204h	207h	RESETS (RESETS)—Offset 204h	0h
210h	213h	Active LTR (ACTIVELTR_VALUE)—Offset 210h	800h
214h	217h	IDLE LTR (IDLELTR_VALUE)—Offset 214h	800h
218h	21Bh	reg_TX_BYTE_COUNT (TX_BYTE_COUNT)—Offset 218h	0h
21Ch	21Fh	reg_RX_BYTE_COUNT (RX_BYTE_COUNT)—Offset 21Ch	0h
228h	22Bh	SW SCRATCH 0 (SW_SCRATCH_0)—Offset 228h	0h
238h	23Bh	reg_CLOCK_GATE (CLOCK_GATE)—Offset 238h	0h
240h	243h	reg_REMAP_ADDR_LO (REMAP_ADDR_LO)—Offset 240h	0h
244h	247h	reg_REMAP_ADDR_HI (REMAP_ADDR_HI)—Offset 244h	0h
24Ch	24Fh	reg_DEVIDLE_CONTROL (DEVIDLE_CONTROL)—Offset 24Ch	8h
2FCh	2FFh	Capabilities (CAPABLITIES)—Offset 2FCh	10h
618h	61Bh	UART Byte Address Control (GEN_REGRW7)—Offset 618h	0h

11.3.1 CLOCKS (CLOCKS)—Offset 200h

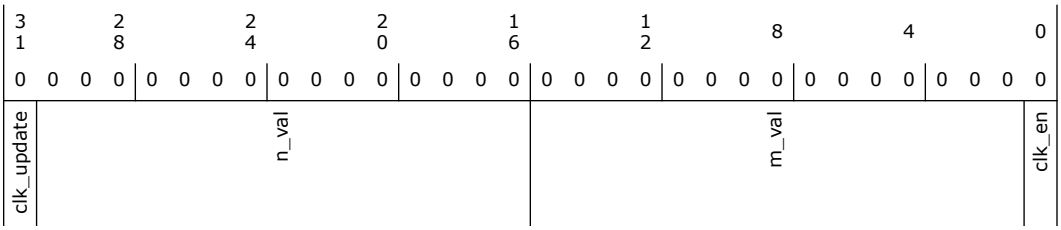
Private Clock Configuration

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**clk_update (clk_update):** Update the clock divider after seeting new m and n values. 0 – No clock Update 1 – Clock gets updated.
30:16	0h RW	**N_VAL (n_val):** This is the denominator value (N) for the M over N divider logic that creates CLK_OUT. Used to generate the input clk to the UART.
15:1	0h RW	**M_VAL (m_val):** The numerator value (M) for the M over N divider logic that creates the CLK_OUT. Used to generate the input clk to the UART.
0	0h RW	**clk_en (clk_en):** UART Serial Clock (output of M/N, input to UART) Clock Enable 0 – Clock disabled 1 – Clock Enabled.

11.3.2 RESETS (RESETS)—Offset 204h

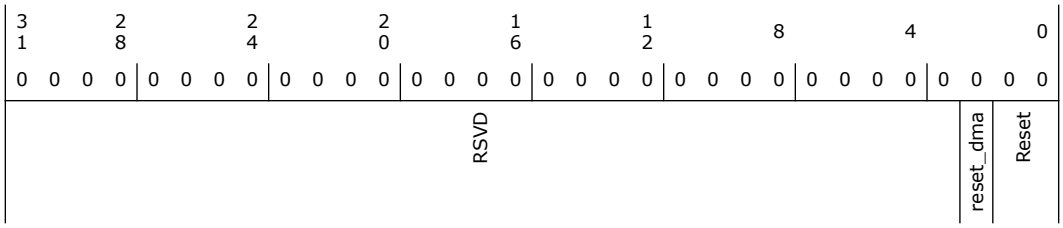
Software Reset

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	Reserved.
2	0h	**Reset_DMA (reset_dma):** Reset the DMA controller
1:0	0h	**Reset_UART (Reset):** UART Host Controller reset. Used to reset the UART Host Controller by SW control. All Configuration State and Operational State will be forced to the Default state. There is no timing requirement (SW can assert and de-assert in back to back transactions) This reset does NOT impact the settings by BIOS, the PCI configuration header information, DMA channel configuration and interrupt assignment/mapping/etc. Driver should re-initialize registers related to Driver context following an UART host controller reset. 00 = UART Host Controller is in reset (Reset Asserted) 01 = Reserved 10 = Reserved 11 = UART Host Controller is NOT at reset (Reset Released)

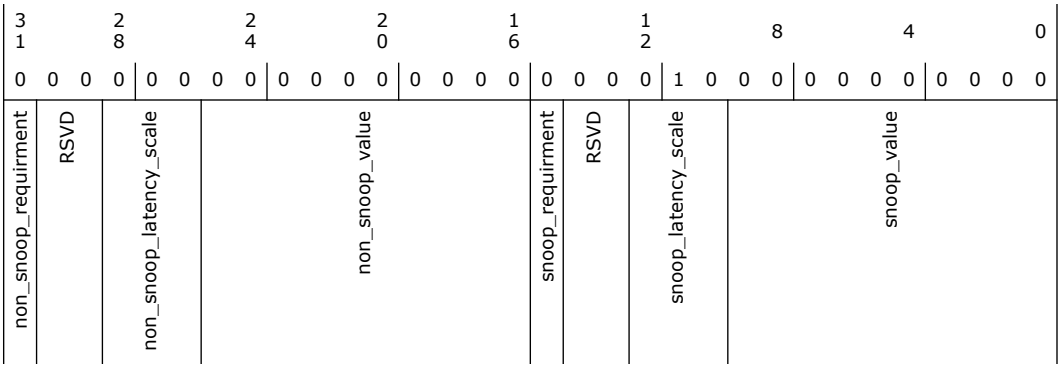
11.3.3 Active LTR (ACTIVELTR_VALUE)—Offset 210h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 800h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Non_Snoop_Requirment (non_snoop_requirment):** If the Requirement (bit 15) is clear, that indicates that the device has no LTR requirement for this type of traffic (i.e. it can wait for service indefinitely). If the 10-bit latency value is zero it indicates that the device cannot tolerate any delay and needs the best possible service/ response time.
30:29	0h RO	Reserved.
28:26	0h RO	**Non_Snoop_latency_scale (non_snoop_latency_scale):** Support for codes 010 (1us) or 011 (32us) for Snoop Latency Scale (1us -> 32ms total span) only. Writes to this CSR which don't match those values will be dropped completely, next read will return previous value.
25:16	0h RO	**Non_Snoop_value (non_snoop_value):** 10-bit latency value
15	0h RW	**Snoop_Requirment (snoop_requirment):** If the Requirement (bit 15) is clear, that indicates that the device has no LTR requirement for this type of traffic (i.e. it can wait for service indefinitely). If the 10-bit latency value is zero it indicates that the device cannot tolerate any delay and needs the best possible service/response time.
14:13	0h RO	Reserved.
12:10	2h RW	**Snoop_latency_scale (snoop_latency_scale):** Support for codes 010 (1us) or 011 (32us) for Snoop Latency Scale(1us -> 32ms total span) only. Writes to this CSR which don't match those values will be dropped completely, next read will return previous value.
9:0	0h RW	**Snoop_value (snoop_value):** 10-bit latency value

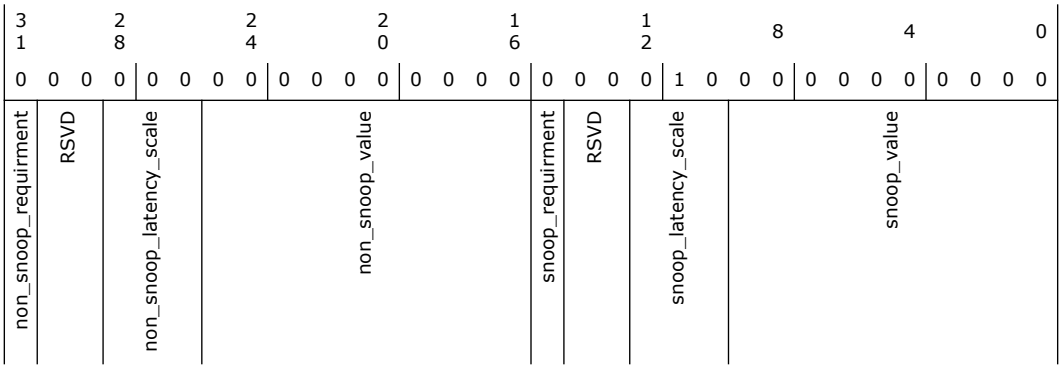
11.3.4 IDLE LTR (IDLELTR_VALUE)—Offset 214h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 800h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Non_Snoop_Requirment (non_snoop_requirment):** If the Requirement (bit 15) is clear, that indicates that the device has no LTR requirement for this type of traffic (i.e. it can wait for service indefinitely). If the 10-bit latency value is zero it indicates that the device cannot tolerate any delay and needs the best possible service/ response time.
30:29	0h RO	Reserved.
28:26	0h RO	**Non_Snoop_latency_scale (non_snoop_latency_scale):** Support for codes 010 (1us) or 011 (32us) for Snoop Latency Scale (1us -> 32ms total span) only. Writes to this CSR which don't match those values will be dropped completely, next read will return previous value.
25:16	0h RO	**Non_Snoop_value (non_snoop_value):** 10-bit latency value
15	0h RW	**Snoop_Requirment (snoop_requirment):** If the Requirement (bit 15) is clear, that indicates that the device has no LTR requirement for this type of traffic (i.e. it can wait for service indefinitely). If the 10-bit latency value is zero it indicates that the device cannot tolerate any delay and needs the best possible service/response time.
14:13	0h RO	Reserved.
12:10	2h RW	**Snoop_latency_scale (snoop_latency_scale):** Support for codes 010 (1us) or 011 (32us) for Snoop Latency Scale(1us -> 32ms total span) only. Writes to this CSR which don't match those values will be dropped completely, next read will return previous value.
9:0	0h	**Snoop_value (snoop_value):** 10-bit latency value

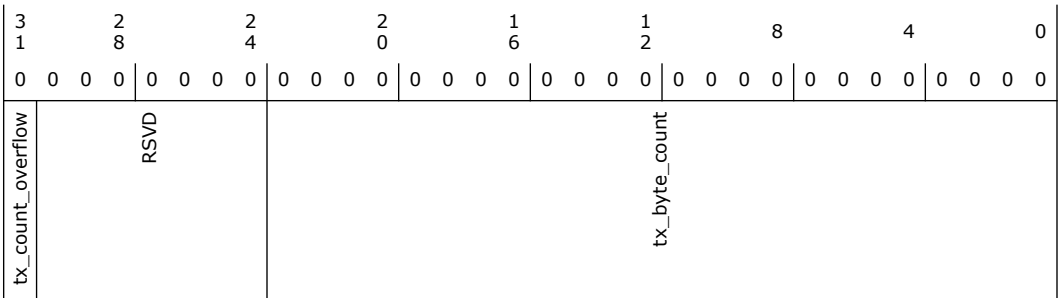
11.3.5 reg_TX_BYTE_COUNT (TX_BYTE_COUNT)—Offset 218h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**tx_count_overflow (tx_count_overflow):** 0= count valid 1= count overflow/invalid
30:24	0h RO	Reserved.
23:0	0h RO	**tx_byte_count (tx_byte_count):** 24-bit up-counter which counts the number of TX Bytes on the Serial bus. The Counter is forced to be cleared by software Read.

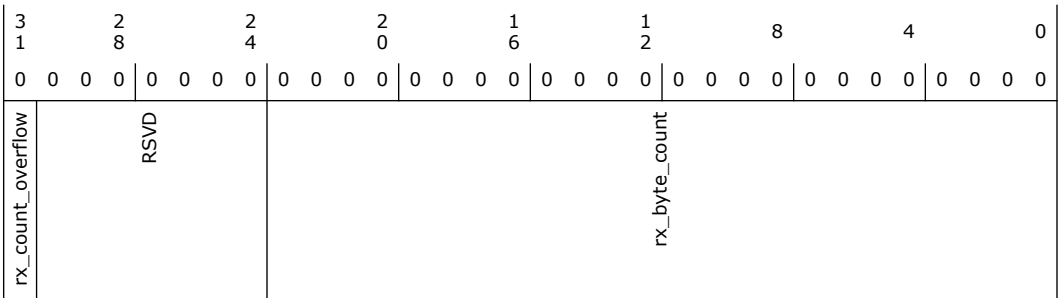
11.3.6 reg_RX_BYTE_COUNT (RX_BYTE_COUNT)—Offset 21Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**rx_count_overflow (rx_count_overflow):** 0= count valid 1= count overflow/invalid
30:24	0h RO	Reserved.
23:0	0h RO	**rx_byte_count (rx_byte_count):** 24-bit up-counter which counts the number of RX Bytes on the Serial bus. The Counter is forced to be cleared by software Read.

11.3.7 SW SCRATCH 0 (SW_SCRATCH_0)—Offset 228h

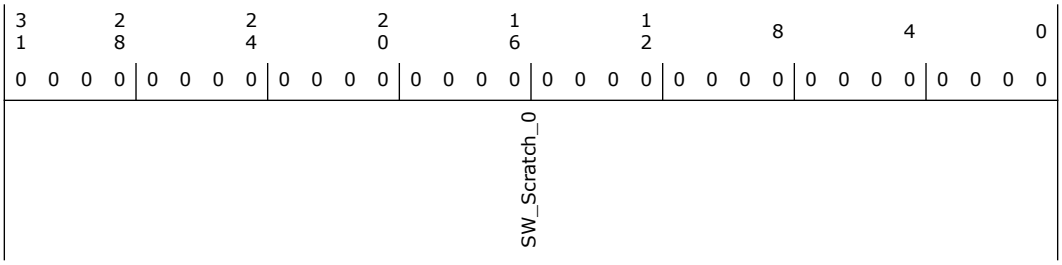
NOTE: The same registers are available at the following offsets:
SW SCRATCH 1: offset 22Ch
SW SCRATCH 2: offset 230h
SW SCRATCH 3: offset 234h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**reg_SW_Scratch_0 (SW_Scratch_0)**

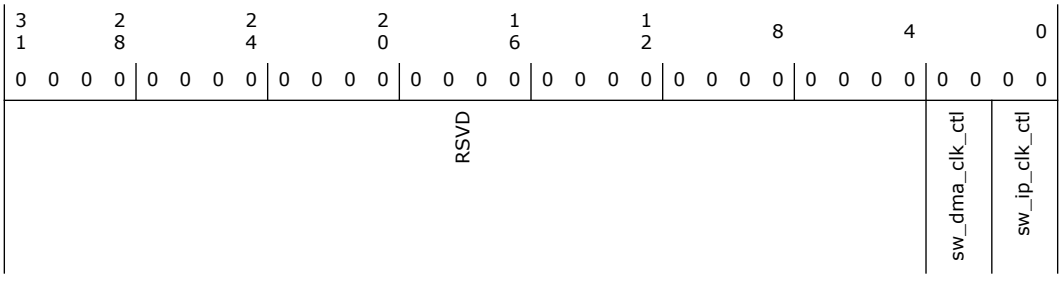
11.3.8 reg_CLOCK_GATE (CLOCK_GATE)—Offset 238h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3:2	0h	**sw_dma_clk_ctl (sw_dma_clk_ctl):** DMA Clock Control 00 = Dyanamic Clock Gate Enable 01 = Reserved 10 = Force iDMA Clock off 11 = Force iDMA Clock on
1:0	0h	**sw_ip_clk_ctl (sw_ip_clk_ctl):** Clock Control 00 = Dyanamic Clock Gate Enable 01 = Reserved 10 = Force IP Clocks off 11 = Force IP Clocks on

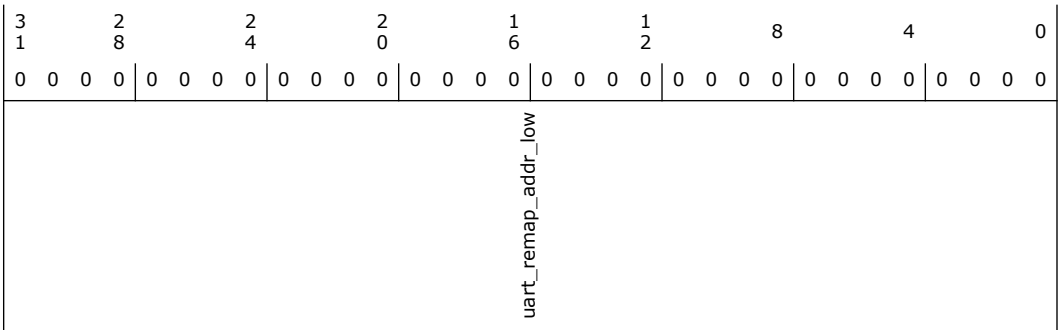
11.3.9 reg_REMAP_ADDR_LO (REMAP_ADDR_LO)—Offset 240h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**uart_remap_addr_low (uart_remap_addr_low):** Low 32 bits of BAR address read by SW

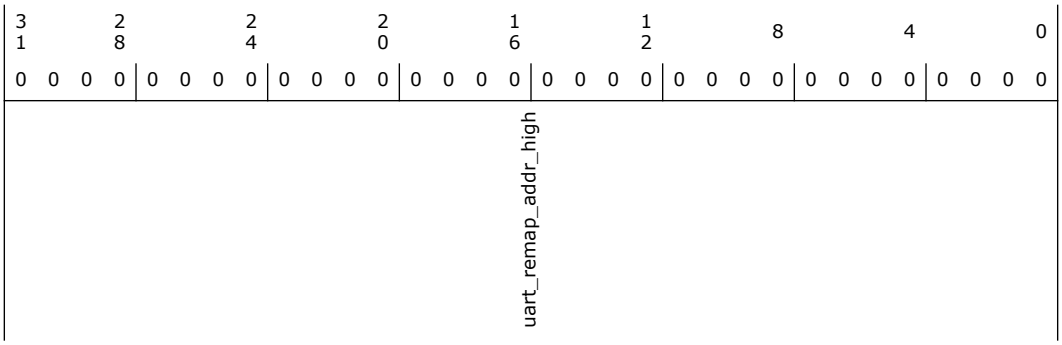
11.3.10 reg_REMAP_ADDR_HI (REMAP_ADDR_HI)—Offset 244h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**uart_remap_addr_high (uart_remap_addr_high):** High 32 bits of BAR address read by SW

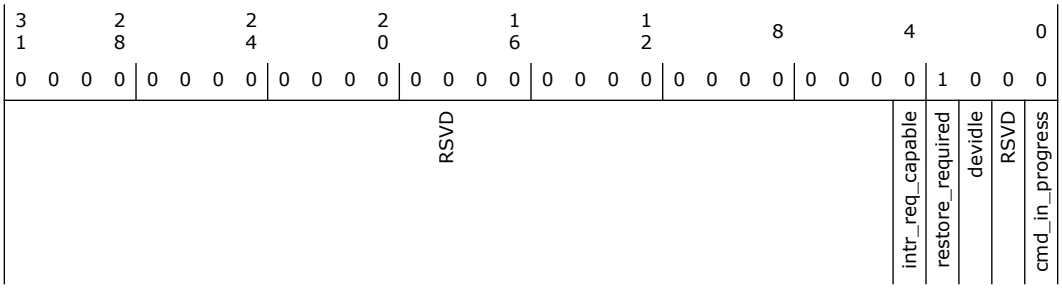
11.3.11 reg_DEVIDLE_CONTROL (DEVIDLE_CONTROL)—Offset 24Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 8h



Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4	0h RO	**Interrupt Request Capable (intr_req_capable):** Set to '1' by HW if it is capable of generating an interrupt on command completion, else '0'.
3	1h RW1C	**Restore Require (restore_required):** When set (by HW), SW must restore state to the controller. The state may have been lost due to a reset or full power lost. SW clears the bit by writing a '1'. This bit will be set on initial power up.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Device Idle (devidle):** SW sets this bit to '1' to move the function into the DevIdle state. Writing this bit to '0' will return the function to the fully active D0 state (D0i0).
1	0h RO	Reserved.
0	0h RO	**Command-In-Progress (cmd_in_progress):** HW sets this bit on a 1->0 or 0->1 transition of DEVIDLE. While set, the other bits in this register are not valid and it is illegal for SW to write to any bit in this register. HW clears this bit upon completing the DevIdle transition command. When clear, all the other bits in the register are valid and SW may write to any bit. If Interrupt Request (IR) was set for the current command, HW may clear this bit before the interrupt has been made visible to SW, since when SW actually handles a particular interrupt is not visible to the HW. SW writes to this bit have no effect.

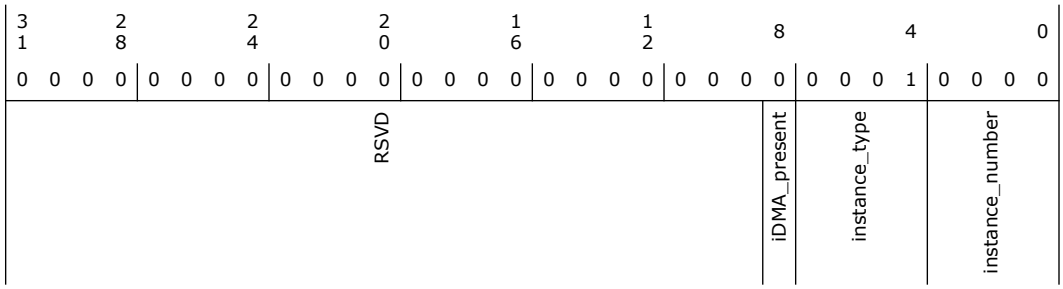
11.3.12 Capabilities (CAPABLITIES)—Offset 2FCh

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 10h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h RO	**DMA Present (iDMA_present):** 0= DMA present 1= DMA not present
7:4	1h RO	**Instant Type (instance_type):** 0000 = IC2 0001 = UART 0010 = SPI 0011 – 1111 = Reserved
3:0	0h RO	**Instant Number (instance_number)**

11.3.13 UART Byte Address Control (GEN_REGRW7)—Offset 618h

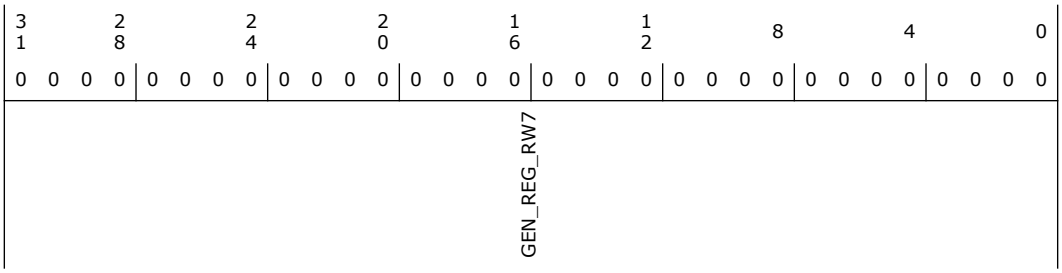
This register controls the 16550 8-Bit Addressing Mode.
After setting any of the bits in this register, BIOs/SW must immediately issue an MMIO Read transaction to a UARTn BAR0 + Offset Register (For example: 0x0F8, the read data can be disgarded). This MUST BE done in order for the UART 16550 8-bit Legacy Mode to become active.

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**UART Byte Address Enable (GEN_REG_RW7):** Settings: 0 = Inactive (Off) 1 = Active (On) The following bits are assigned to the UART controllers: Bit 0: UART0 controller Bit 1: UART1 controller Bit 2: UART2 controller Other bits are reserved

11.4 UART DMA Controller Registers Summary

The registers in this section are memory-mapped registers based on the BAR defined in PCH Configuration space.

Table 11-4. Summary of UART DMA Controller Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
800h	803h	DMA Transfer Source Address Low (SAR_LO0)—Offset 800h	0h
804h	807h	DMA Transfer Source Address High (SAR_HI0)—Offset 804h	0h
808h	80Bh	DMA Transfer Destination Address Low (DAR_LO0)—Offset 808h	0h
80Ch	80Fh	DMA Transfer Destination Address High (DAR_HI0)—Offset 80Ch	0h
810h	813h	Linked List Pointer Low (LLP_LO0)—Offset 810h	0h
814h	817h	Linked List Pointer High (LLP_HI0)—Offset 814h	0h
818h	81Bh	Control Register Low (CTL_LO0)—Offset 818h	0h
81Ch	81Fh	Control Register High (CTL_HI0)—Offset 81Ch	0h

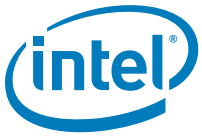


Table 11-4. Summary of UART DMA Controller Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
820h	823h	Source Status (SSTAT0)—Offset 820h	0h
828h	82Bh	Destination Status (DSTAT0)—Offset 828h	0h
830h	833h	Source Status Address Low (SSTATAR_LO0)—Offset 830h	0h
834h	837h	Source Status Address High (SSTATAR_HI0)—Offset 834h	0h
838h	83Bh	Destination Status Address Low (DSTATAR_LO0)—Offset 838h	0h
83Ch	83Fh	Destination Status Address High (DSTATAR_HI0)—Offset 83Ch	0h
840h	843h	DMA Transfer Configuration Low (CFG_LO0)—Offset 840h	203h
844h	847h	DMA Transfer Configuration High (CFG_HI0)—Offset 844h	0h
848h	84Bh	Source Gather (SGR0)—Offset 848h	0h
850h	853h	Destination Scatter (DSR0)—Offset 850h	0h
AC0h	AC3h	Raw Interrupt Status (RawTfr)—Offset AC0h	0h
AC8h	ACBh	Raw Status for Block Interrupts (RawBlock)—Offset AC8h	0h
AD0h	AD3h	Raw Status for Source Transaction Interrupts (RawSrcTran)—Offset AD0h	0h
AD8h	ADBh	Raw Status for Destination Transaction Interrupts (RawDstTran)—Offset AD8h	0h
AE0h	AE3h	Raw Status for Error Interrupts (RawErr)—Offset AE0h	0h
AE8h	AEBh	Interrupt Status (StatusTfr)—Offset AE8h	0h
AF0h	AF3h	Status for Block Interrupts (StatusBlock)—Offset AF0h	0h
AF8h	AFBh	Status for Source Transaction Interrupts (StatusSrcTran)—Offset AF8h	0h
B00h	B03h	Status for Destination Transaction Interrupts (StatusDstTran)—Offset B00h	0h
B08h	B0Bh	Status for Error Interrupts (StatusErr)—Offset B08h	0h
B10h	B13h	Mask for Transfer Interrupts (MaskTfr)—Offset B10h	0h
B18h	B1Bh	Mask for Block Interrupts (MaskBlock)—Offset B18h	0h
B20h	B23h	Mask for Source Transaction Interrupts (MaskSrcTran)—Offset B20h	0h
B28h	B2Bh	Mask for Destination Transaction Interrupts (MaskDstTran)—Offset B28h	0h
B30h	B33h	Mask for Error Interrupts (MaskErr)—Offset B30h	0h
B38h	B3Bh	Clear for Transfer Interrupts (ClearTfr)—Offset B38h	0h
B40h	B43h	Clear for Block Interrupts (ClearBlock)—Offset B40h	0h
B48h	B4Bh	Clear for Source Transaction Interrupts (ClearSrcTran)—Offset B48h	0h
B50h	B53h	Clear for Destination Transaction Interrupts (ClearDstTran)—Offset B50h	0h
B58h	B5Bh	Clear for Error Interrupts (ClearErr)—Offset B58h	0h
B60h	B63h	Combined Status register (StatusInt)—Offset B60h	0h
B98h	B9Bh	DMA Configuration (DmaCfgReg)—Offset B98h	0h
BA0h	BA3h	DMA Channel Enable (ChEnReg)—Offset BA0h	0h

11.4.1 DMA Transfer Source Address Low (SAR_LO0)—Offset 800h

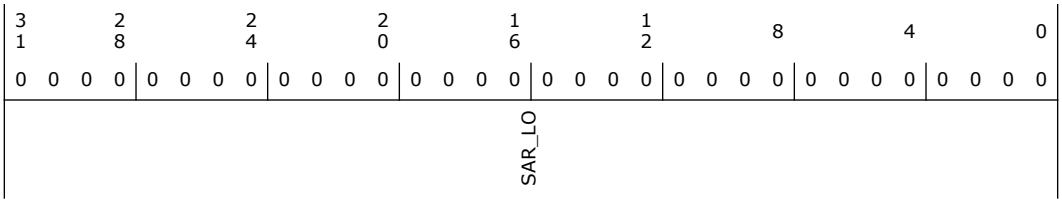
NOTE: SAR_LO0 is for DMA Channel 0. The same register definition,SAR_LO1, is available for Channel 1 at address 858h.
SAR_LO0 (CH0): offset 800h

SAR_LO1 (CH1): offset 858h
The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

Access Method

Type: MEM Register (Size: 32 bits)
Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**SAR_LO:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length > 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected). 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported.

11.4.2 DMA Transfer Source Address High (SAR_HI0)—Offset 804h

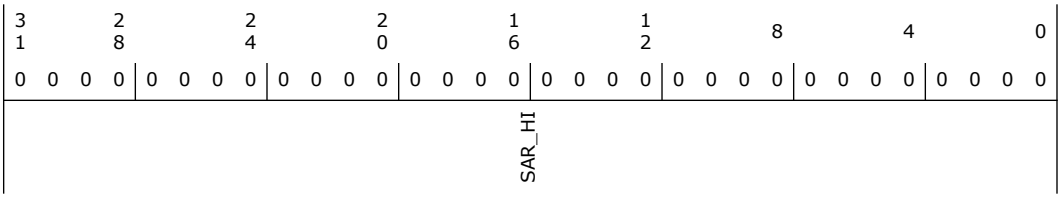
NOTE: SAR_HI0 is for DMA Channel 0. The same register definition, SAR_HI1, is available for Channel 1 at address 85Ch.
SAR_HI0 (CH0): offset 804h
SAR_HI1 (CH1): offset 85Ch
The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**SAR_HI:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length > 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported.

11.4.3 DMA Transfer Destination Address Low (DAR_LO0)—Offset 808h

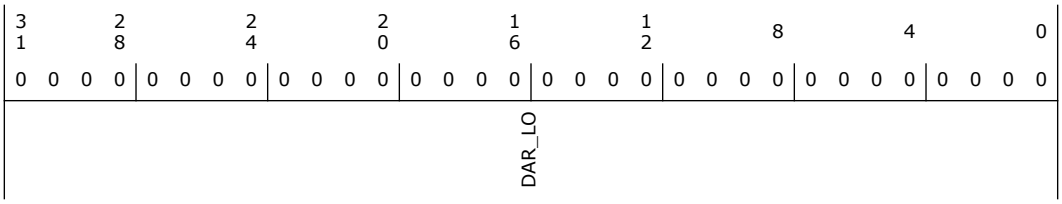
NOTE: DAR_LO0 is for DMA Channel 0. The same register definition, DAR_LO1, is available for Channel 1 at address 860h.
DAR_LO0 (CH0): offset 808h
DAR_LO1 (CH1): offset 860h
The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DAR_LO:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length > 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported.

11.4.4 DMA Transfer Destination Address High (DAR_HI0)—Offset 80Ch

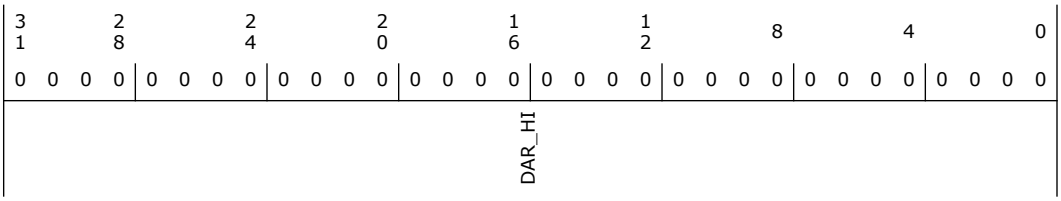
NOTE: DAR_HI0 is for DMA Channel 0. The same register definition, DAR_HI1, is available for Channel 1 at address 864h.
DAR_HI0 (CH0): offset 80Ch
DAR_HI1 (CH1): offset 864h
The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DAR_HI:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length > 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported.

11.4.5 Linked List Pointer Low (LLP_LO0)—Offset 810h

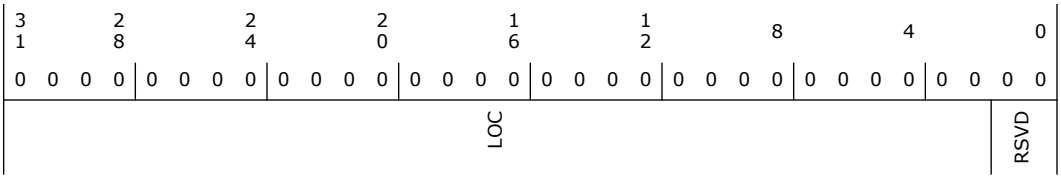
NOTE: LLP_LO0 is for DMA Channel 0. The same register definition, LLP_LO1, is available for Channel 1 at address 868h.
LLP_LO0 (CH0): offset 810h
LLP_LO1 (CH1): offset 868h
The register needs to be programmed to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0h RO	Reserved.

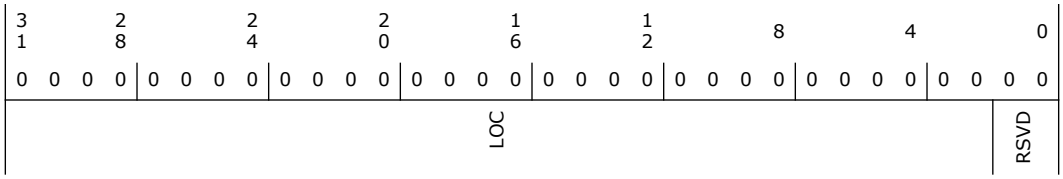
11.4.6 Linked List Pointer High (LLP_HI0)—Offset 814h

NOTE: LLP_HI0 is for DMA Channel 0. The same register definition, LLP_HI1, is available for Channel 1 at address 86Ch.
LLP_HI0 (CH0): offset 814h
LLP_LO1 (CH1): offset 86Ch
The register needs to be programmed to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled.

Access Method

Type: MEM Register (Size: 32 bits)
Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0h RO	Reserved.

11.4.7 Control Register Low (CTL_LO0)—Offset 818h

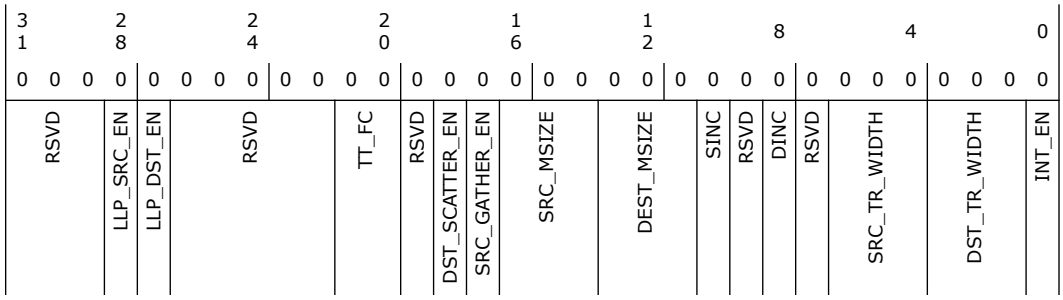
NOTE: CTL_LO0 is for DMA Channel 0. The same register definition, CTL_LO1, is available for Channel 1 at address 870h.
LLP_HI0 (CH0): offset 818h
LLP_LO1 (CH1): offset 870h
This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled. If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	Reserved.
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	0h RO	Reserved.
21:20	0h RW	**TT_FC:** The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	0h RO	Reserved.
18	0h RW	**DST_SCATTER_EN:** 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0h RW	**SRC_GATHER_EN:** 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0h RW	**SRC_MSIZE:** Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source.
13:11	0h RW	**DEST_MSIZE:** Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination.
10	0h RW	**SINC:** Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)

Bit Range	Default & Access	Field Name (ID): Description
9	0h RO	Reserved.
8	0h RW	**DINC:** Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0h RO	Reserved.
6:4	0h RW	**SRC_TR_WIDTH:** BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width < 4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations)
3:1	0h RW	**DST_TR_WIDTH:** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width < 4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations)
0	0h RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

11.4.8 Control Register High (CTL_HI0)—Offset 81Ch

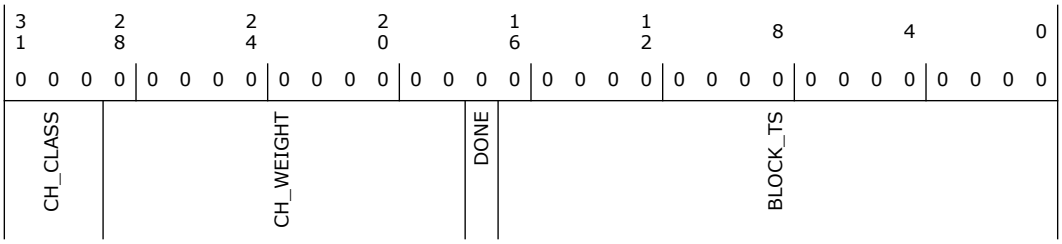
NOTE: CTL_HI0 is for DMA Channel 0. The same register definition, CTL_HI1, is available for Channel 1 at address 874h.
CTL_HI0 (CH0): offset 81Ch
CTL_HI1 (CH1): offset 874h
This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RW	**CH_CLASS:** A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior.
28:18	0h RW	**CH_WEIGHT**
17	0h RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	0h RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It doesn't mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

11.4.9 Source Status (SSTAT0)—Offset 820h

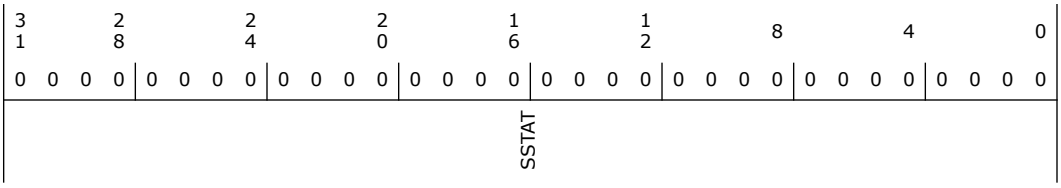
NOTE: SSTAT0 is for DMA Channel 0. The same register definition, SSTAT1, is available for Channel 1 at address 878h.
SSTAT0 (CH0): offset 820h
SSTAT1 (CH1): offset 878h
After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block.
Note : This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

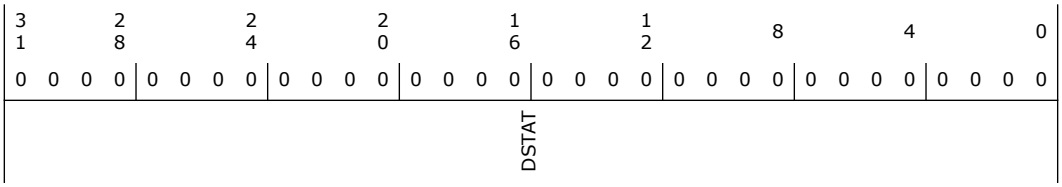
11.4.10 Destination Status (DSTAT0)—Offset 828h

NOTE: DSTAT0 is for DMA Channel 0. The same register definition, DSTAT1, is available for Channel 1 at address 880h.
DSTAT0 (CH0): offset 828h
DSTAT1 (CH1): offset 880h
After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI.
Note : This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

Access Method

Type: MEM Register (Size: 32 bits)
Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

11.4.11 Source Status Address Low (SSTATAR_LO0)—Offset 830h

NOTE: SSTATAR_LO0 is for DMA Channel 0. The same register definition, SSTATAR_LO1, is available for Channel 1 at address 888h.
SSTATAR_LO0(CH0): offset 830h

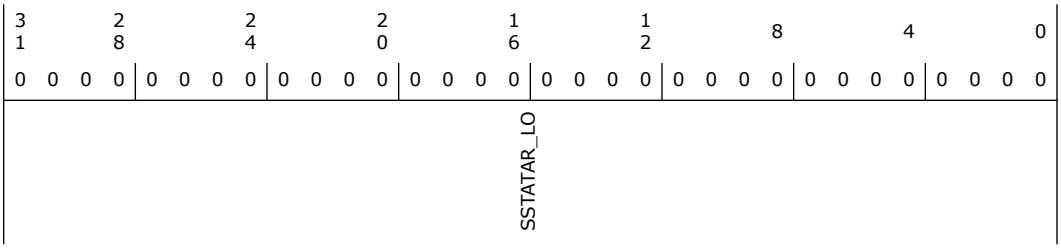
SSTATAR_LO1(CH1): offset 888h
After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**SSTATAR_LO:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

11.4.12 Source Status Address High (SSTATAR_HI0)—Offset 834h

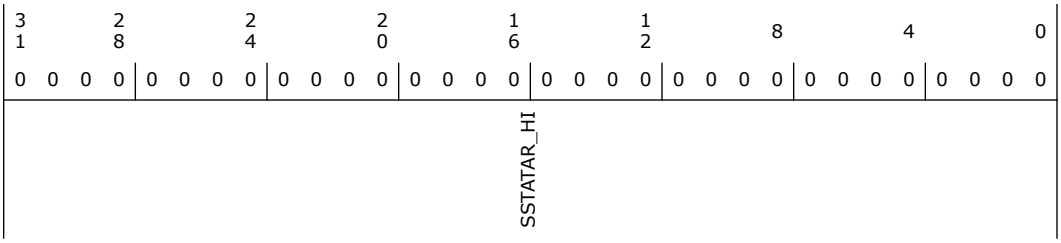
NOTE: SSTATAR_HI0 is for DMA Channel 0. The same register definition, SSTATAR_HI1, is available for Channel 1 at address 88Ch.
SSTATAR_HI0(CH0): offset 834h
SSTATAR_HI1(CH1): offset 88Ch
After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**SSTATAR_HI:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

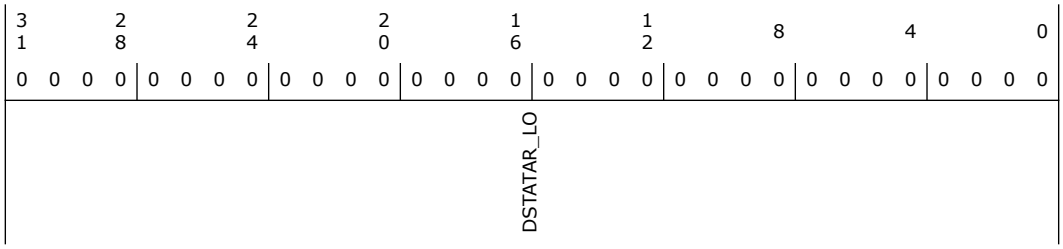
11.4.13 Destination Status Address Low (DSTATAR_LO0)—Offset 838h

NOTE: DSTATAR_LO0 is for DMA Channel 0. The same register definition, DSTATAR_LO1, is available for Channel 1 at address 890h.
DSTATAR_LO0(CH0): offset 838h
DSTATAR_LO1(CH1): offset 890h
After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Access Method

Type: MEM Register (Size: 32 bits)
Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DSTATAR_LO:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

11.4.14 Destination Status Address High (DSTATAR_HI0)—Offset 83Ch

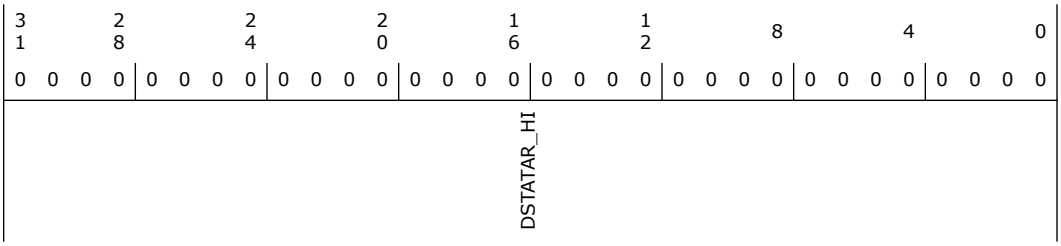
NOTE: DSTATAR_LO0 is for DMA Channel 0. The same register definition, DSTATAR_HI1, is available for Channel 1 at address 894h.
DSTATAR_HI0(CH0): offset 83Ch
DSTATAR_HI1(CH1): offset 894h
After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DSTATAR_HI:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

11.4.15 DMA Transfer Configuration Low (CFG_LO0)—Offset 840h

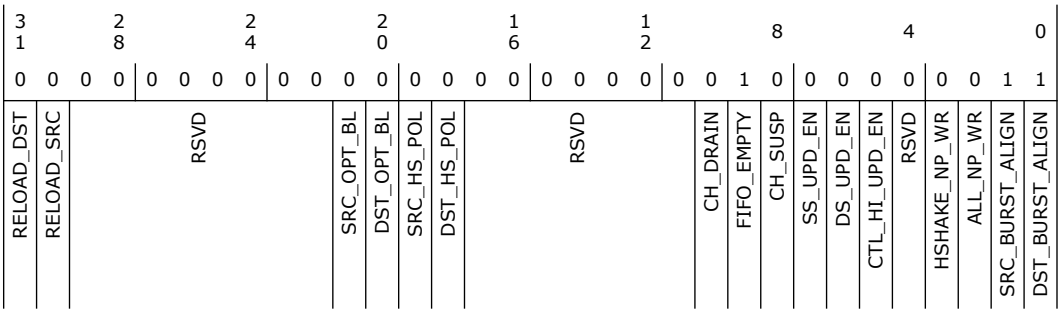
NOTE: CFG_LO0 is for DMA Channel 0. The same register definition, CFG_LO1, is available for Channel 1 at address 898h.
CFG_LO0(CH0): offset 840h
CFG_LO1(CH1): offset 898h
This register contains fields that configure the DMA transfer. The channel configuration register remains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 203h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
30	0h RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	0h RO	Reserved.
21	0h RW	**SRC_OPT_BL:** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 <= BL <= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled
20	0h RW	**DST_OPT_BL:** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 <= BL <= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled
19	0h RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0h RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17:11	0h RO	Reserved.
10	0h RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND is asserted.
9	1h RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty
8	0h RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0h RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
6	0h RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0h RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0h RO	Reserved.
3	0h RW	**HSHAKE_NP_WR:** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted) This bit must be set to 1 for proper operation

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**ALL_NP_WR:** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	1h RW	**SRC_BURST_ALIGN:** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary
0	1h RW	**DST_BURST_ALIGN:** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary.

11.4.16 DMA Transfer Configuration High (CFG_HI0)—Offset 844h

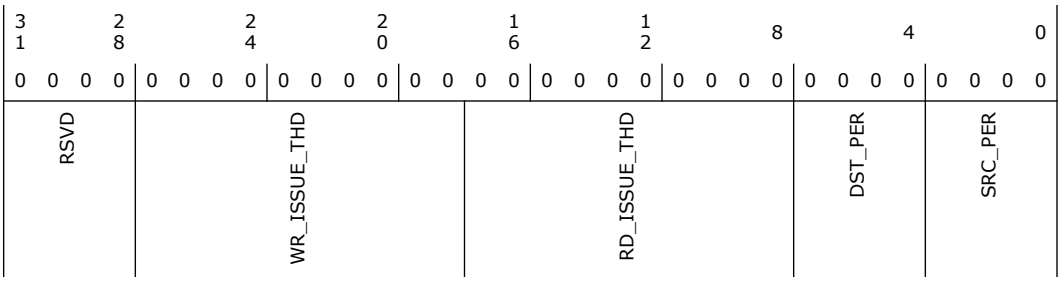
NOTE: CFG_HI0 is for DMA Channel 0. The same register definition, CFG_HI1, is available for Channel 1 at address 89Ch.
CFG_HI0(CH0): offset 844h
CFG_HI1(CH1): offset 89Ch
This register contains fields that configure the DMA transfer. The channel configuration register remains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	Reserved.
27:18	0h RW	**WR_ISSUE_THD:** Write Issue Threshold. Used to relax the issue criterion for Writes. Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.

Bit Range	Default & Access	Field Name (ID): Description
17:8	0h RW	**RD_ISSUE_THD:** Read Issue Threshold. Used to relax the issue criterion for Reads. Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.
7:4	0h RW	**DST_PER:** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface.
3:0	0h RW	**SRC_PER:** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface.

11.4.17 Source Gather (SGR0)—Offset 848h

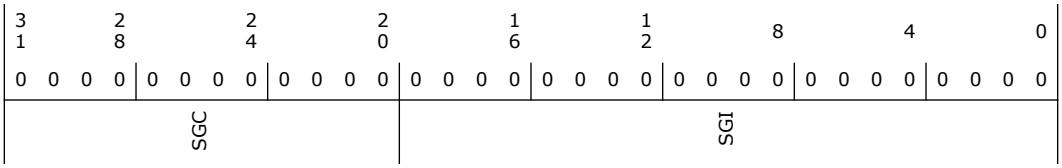
NOTE: SGR0 is for DMA Channel 0. The same register definition, SGR1, is available for Channel 1 at address 8A0h.
SGR0(CH0): offset 848h
SGR1(CH1): offset 8A0h
The Source Gather register contains two fields: Source gather count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gather interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

Access Method

Type: MEM Register (Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**SGC**
19:0	0h RW	**SGI**

11.4.18 Destination Scatter (DSR0)—Offset 850h

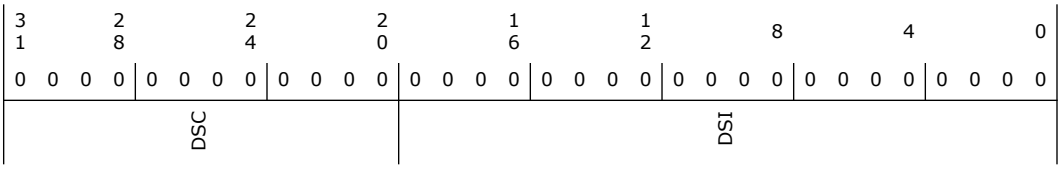
NOTE: DSR0 is for DMA Channel 0. The same register definition, DSR1, is available for Channel 1 at address 8A8h.
DSR0(CH0): offset 850h
DSR1(CH1): offset 8A8h
The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC) . Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI) . Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**DSC**
19:0	0h RW	**DSI**

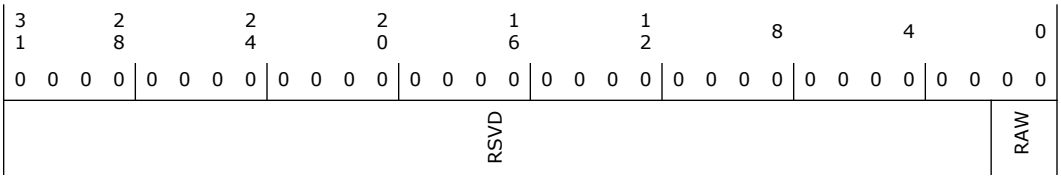
11.4.19 Raw Interrupt Status (RawTfr)—Offset AC0h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**RAW:** Bit0 for channel 0 and bit 1 for channel 1.

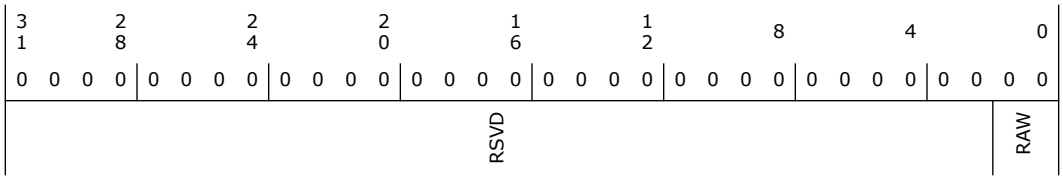
11.4.20 Raw Status for Block Interrupts (RawBlock)—Offset AC8h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**RAW:** Bit 0 for channel 0 and bit 1 for channel 1.

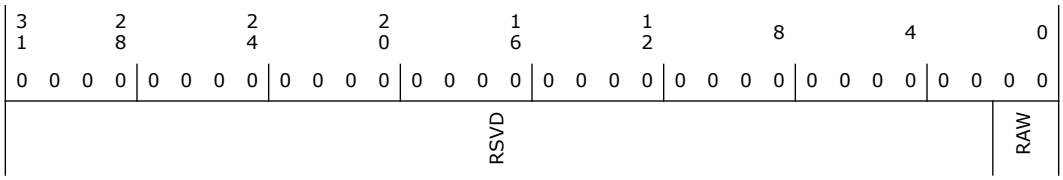
11.4.21 Raw Status for Source Transaction Interrupts (RawSrcTran)—Offset AD0h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**RAW:** Bit 0 for channel 0 and bit 1 for channel 1.

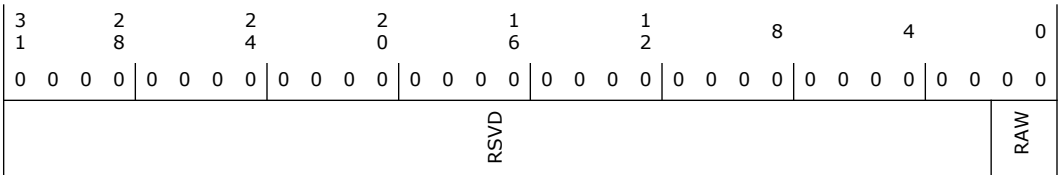
11.4.22 Raw Status for Destination Transaction Interrupts (RawDstTran)—Offset AD8h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**RAW:** Bit 0 for channel 0 and bit 1 for channel 1.

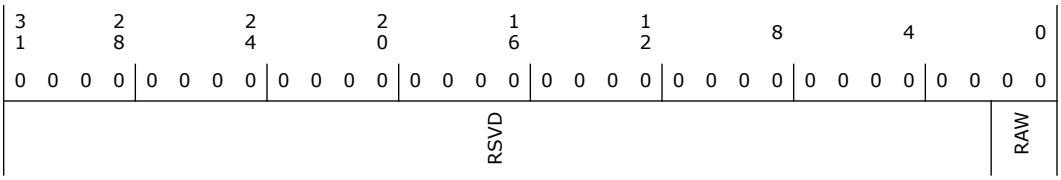
11.4.23 Raw Status for Error Interrupts (RawErr)—Offset AE0h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**RAW:** Bit 0 for channel 0 and bit 1 for channel 1.

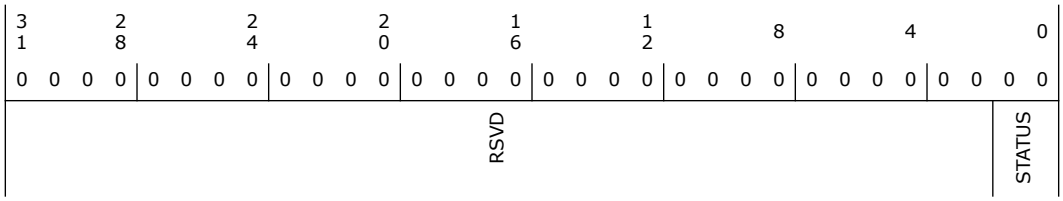
11.4.24 Interrupt Status (StatusTfr)—Offset AE8h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**STATUS:** Bit 0 for channel 0 and bit 1 for channel 1.

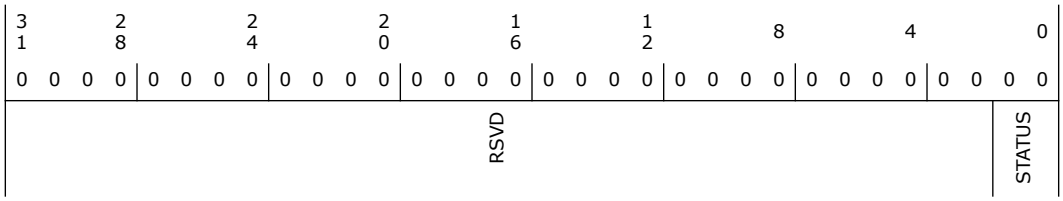
11.4.25 Status for Block Interrupts (StatusBlock)—Offset AF0h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**STATUS:** Bit 0 for channel 0 and bit 1 for channel 1.

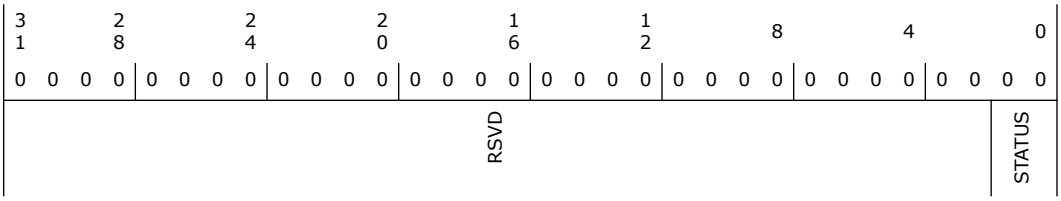
11.4.26 Status for Source Transaction Interrupts (StatusSrcTran)—Offset AF8h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**STATUS:** Bit 0 is for channel 0 and bit 1 is for channel 1.

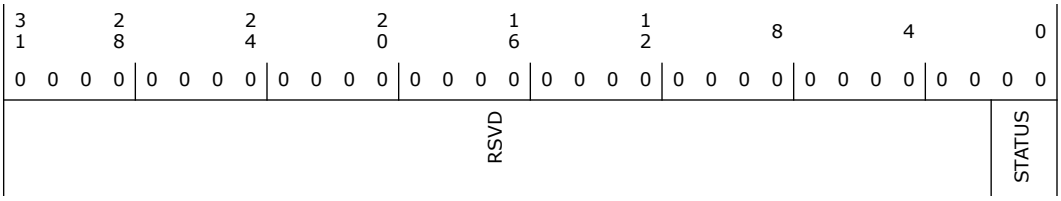
11.4.27 Status for Destination Transaction Interrupts (StatusDstTran)—Offset B00h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**STATUS:** Bit 0 is for channel 0 and bit 1 is for channel 1.

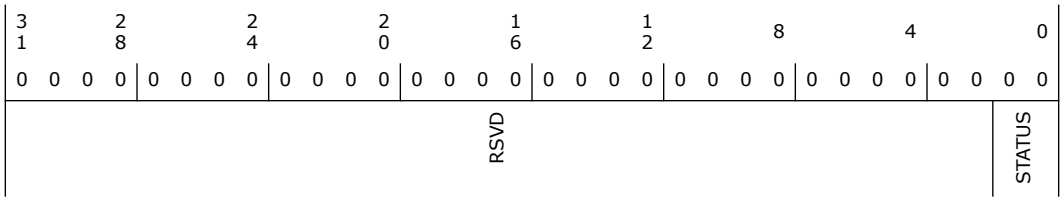
11.4.28 Status for Error Interrupts (StatusErr)—Offset B08h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**STATUS:** Bit 0 is for channel 0 and bit 1 is for channel 1.

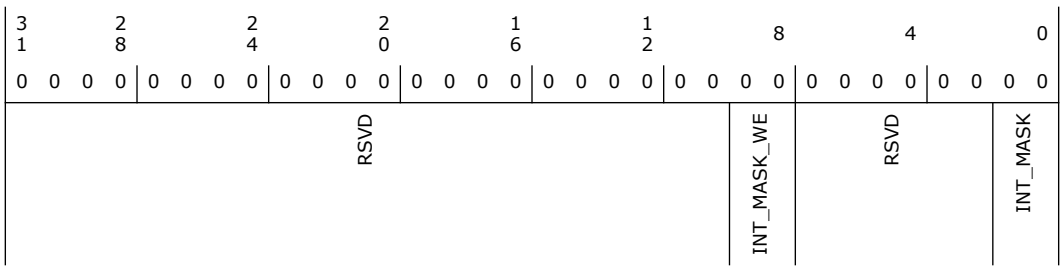
11.4.29 Mask for Transfer Interrupts (MaskTfr)—Offset B10h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:8	0h WO	**INT_MASK_WE:** 0 = write disabled 1 = write enabled
7:2	0h RO	Reserved.
1:0	0h RW	**INT_MASK:** 0-mask 1-unmask

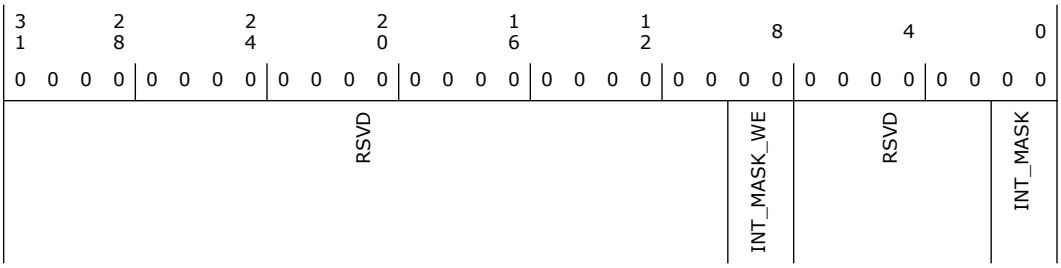
11.4.30 Mask for Block Interrupts (MaskBlock)—Offset B18h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:8	0h WO	**INT_MASK_WE:** 0 = write disabled 1 = write enabled
7:2	0h RO	Reserved.
1:0	0h RW	**INT_MASK:** 0-mask 1-unmask

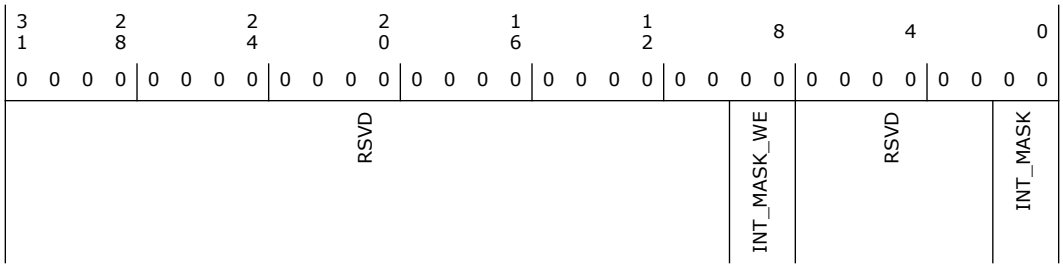
11.4.31 Mask for Source Transaction Interrupts (MaskSrcTran)—Offset B20h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:8	0h WO	**INT_MASK_WE:** 0 = write disabled 1 = write enabled
7:2	0h RO	Reserved.
1:0	0h RW	**INT_MASK:** 0-mask 1-unmask

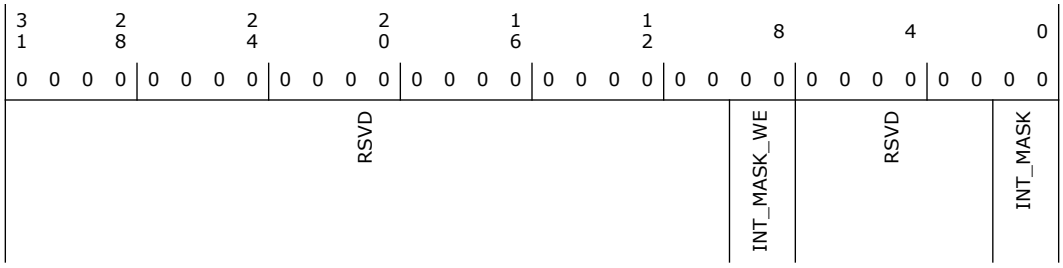
11.4.32 Mask for Destination Transaction Interrupts (MaskDstTran)—Offset B28h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:8	0h WO	**INT_MASK_WE:** 0 = write disabled 1 = write enabled
7:2	0h RO	Reserved.
1:0	0h RW	**INT_MASK:** 0-mask 1-unmask

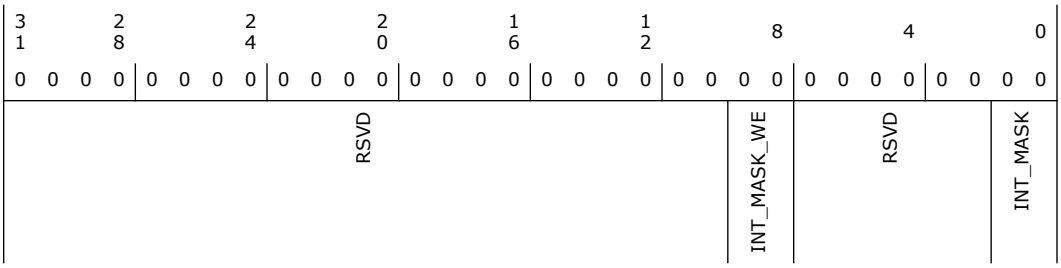
11.4.33 Mask for Error Interrupts (MaskErr)—Offset B30h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:8	0h WO	**INT_MASK_WE:** 0 = write disabled 1 = write enabled
7:2	0h RO	Reserved.
1:0	0h RW	**INT_MASK:** 0-mask 1-unmask

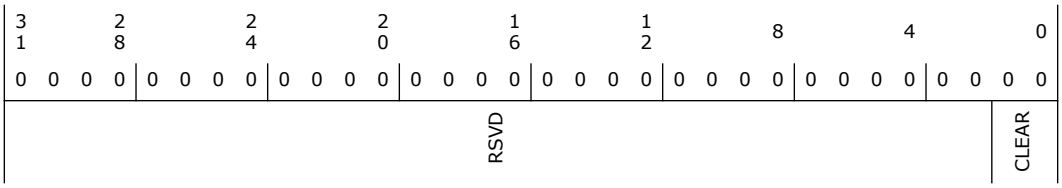
11.4.34 Clear for Transfer Interrupts (ClearTfr)—Offset B38h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h WO	**CLEAR:** 0 = no effect 1 = clear interrupt

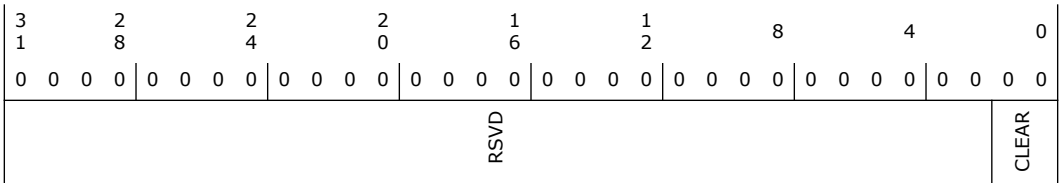
11.4.35 Clear for Block Interrupts (ClearBlock)—Offset B40h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h WO	**CLEAR:** 0 = no effect 1 = clear interrupt

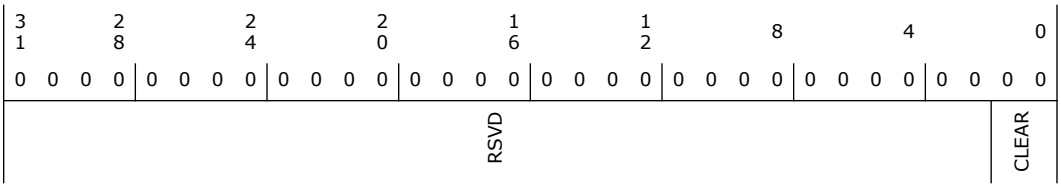
11.4.36 Clear for Source Transaction Interrupts (ClearSrcTran)—Offset B48h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h WO	**CLEAR:** 0 = no effect 1 = clear interrupt

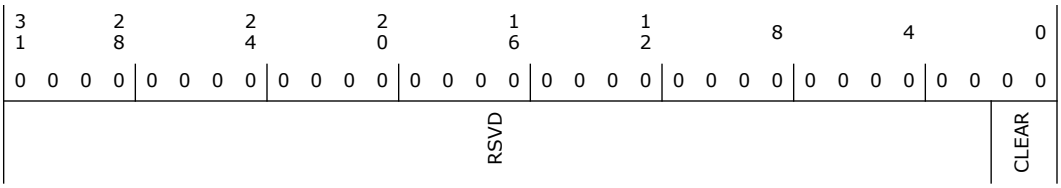
11.4.37 Clear for Destination Transaction Interrupts (ClearDstTran)—Offset B50h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h WO	**CLEAR:** 0 = no effect 1 = clear interrupt

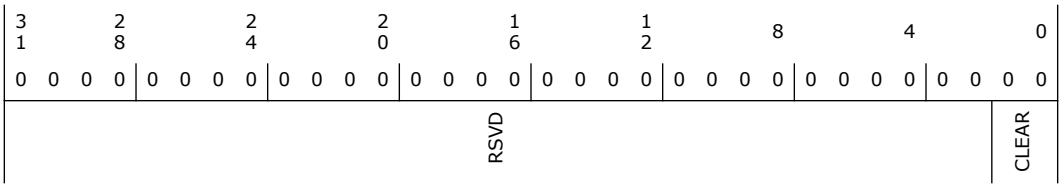
11.4.38 Clear for Error Interrupts (ClearErr)—Offset B58h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h WO	**CLEAR:** 0 = no effect 1 = clear interrupt

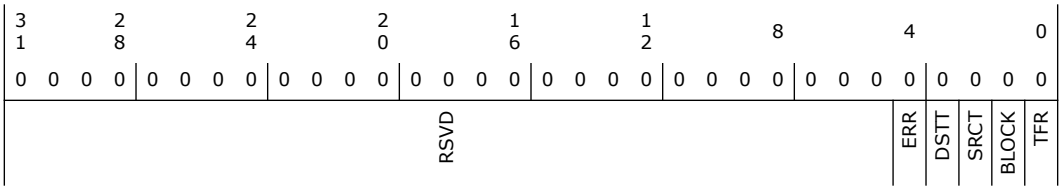
11.4.39 Combined Status register (StatusInt)—Offset B60h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4	0h RO	**ERR:** OR of the contents of StatusErr register.
3	0h RO	**DSTT:** OR of the contents of StatusDst register.
2	0h RO	**SRCT:** OR of the contents of StatusSrcTran register
1	0h RO	**BLOCK:** OR of the contents of StatusBlock register.
0	0h RO	**TFR:** OR of the contents of StatusTfr register.

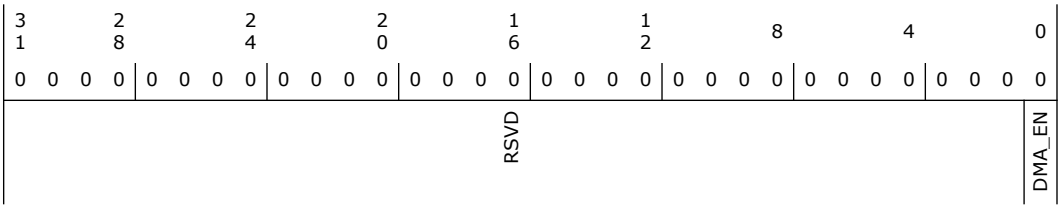
11.4.40 DMA Configuration (DmaCfgReg)—Offset B98h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RW	**DMA_EN:** 0 = DMA Disabled 1 = DMA Enabled

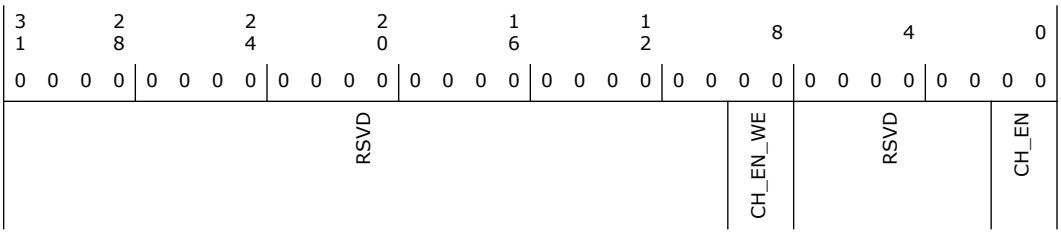
11.4.41 DMA Channel Enable (ChEnReg)—Offset BA0h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h WO	**CH_EN_WE**
7:2	0h RO	Reserved.
1:0	0h RW	**CH_EN:** Enables/Disables the channel. Setting this bit enables a channel, clearing this bit disables the channel. 0 = Disable the Channel 1 = Enable the Channel The ChEnReg.CH_EN bit is automatically cleared by hardware to disable the channel after the last OCP transfer of the DMA transfer to the destination has completed. Software can therefore poll this bit to determine when this channel is free for a new DMA transfer.

11.5 UART PCR Registers Summary

These registers are within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID + Register Offset).

Table 11-5. Summary of UART PCR Registers

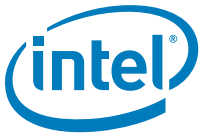
Offset Start	Offset End	Register Name (ID)—Offset	Default Value
218h	21Bh	PCI Configuration Control (PCICFGCTRL) for UART0	00000100h
21Ch	21Fh	PCI Configuration Control (PCICFGCTRL) for UART1	00000100h
220h	223h	PCI Configuration Control (PCICFGCTRL) for UART2	00000100h
618h	61Bh	UART Byte Address Control (GPPRVRW7)	00000000h

11.5.1 PCI Configuration Control (PCICFGCTRL)

Default: 00000100h

NOTE: This register applies to the following UART controllers as follows:

UART0: at offset 218h
UART1: at offset 21Ch
UART2: at offset 220h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
27:20	0h RW	**PCI IRQ:** IRQ number to be sent in the message with data field for Assert_IRQ and Deassert_IRQ message, Note: Bridge does not wire-or the interrupts from different functions before sending them even if they are tied to the same IPIN value of the same IRQ value by the BIOS. It is the responsibility of the interrupt controller to ensure that interrupts are wire-ored. Note: each PCI device (B:D:F) for Intel Serial IO interfaces (i.e.I2C, UART, GSPI) is limit to 4 functions max per PCI device, allowing each function to map to dedicated INT[A-D] and thus a unique IRQ number. Sharing IRQs is not allowed across any Serial IO interfaces B:D:F. All Serial IO interface B:D:F must have a unique IRQ number.
19:12	0h RW	**ACPI IRQ:** IRQ number to be sent in the message with data field for Assert_IRQ and Deassert_IRQ message, Note: Bridge does not wire-or the interrupts from different functions before sending them even if they are tied to the same IPIN value of the same IRQ value by the BIOS. It is the responsibility of the interrupt controller to ensure that interrupts are wire-ored. Note: each PCI device (B:D:F) for Intel Serial IO interfaces (i.e.I2C, UART, GSPI) is limit to 4 functions max per PCI device, allowing each function to map to dedicated INT[A-D] and thus a unique IRQ number. Sharing IRQs is not allowed across any Serial IO interfaces B:D:F. All Serial IO interface B:D:F must have a unique IRQ number.
11:8	0h RW	**Interrupt Pin:** This register indicates the values to be used for Global Interrupts. This value will also be reflected in the PCOS register IPIN value. 0 = No interrupt Pin 1 = INTA 2 = INTB 3 = INTC 4 = INTD 5 - FF: Reserved
7	0h RW	**BAR1 Disable:** BAR1 register in the PCOS space will become Read Only when this bit is set,
6:2	0h RW	**PME Support:** The value in this register will be XOR with the value in the PME_support strap and reflected in the PME_support register in the PCI configuration space. This register can be used as a mechanism to change the value of the PME_Status PCI config register field.
1	0h RW	**ACPI_INTR_EN:** When set, ACPI IRQ number field (bits 19:12) will be used for IRQ messages. When 0, PCI IRQ number field (bits 27:20) will be used for IRQ message.
0	0h RW	**PCI_CFG_DIS:** When set, PCI configuration accesses return UR response. When 0, PCI configuration accesses are supported.

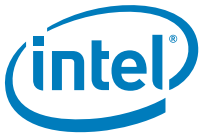
11.5.2 UART Byte Address Control (PCICFGCTRL)

Control bit for 16550 8-Bit Addressing Mode.
NOTE: After setting any bit in this register, the BIOs/SW must immediately issue an MMIO Read transaction to a UARTn BAR0 + Offset Register (For example: 0x0F8, the read data can be discarded). This MUST BE done in order for the UART 16550 8-bit Legacy Mode to become active.

Default: 00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	Reserved.
2	0h RW	**UART2 Byte Address Enable:** 0 = Inactive (Off) 1 = Active (On)
1	0h RW	**UART1 Byte Address Enable:** 0 = Inactive (Off) 1 = Active (On)
0	0h RW	**UART0 Byte Address Enable:** 0 = Inactive (Off) 1 = Active (On)

§ §



12 Generic SPI Interface (D30:F2)

12.1 Generic SPI PCI Configuration Registers Summary

Table 12-1. Summary of Generic SPI PCI Configuration Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	Device ID and Vendor ID Register (DEVVENDID)—Offset 0h	XXXX8086
4h	7h	Status and Command (STATUSCOMMAND)—Offset 4h	100000h
8h	Bh	Revision ID and Class Code (REVCLASSCODE)—Offset 8h	118000XXh
Ch	Fh	Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch	0h
10h	13h	Base Address Register (BAR)—Offset 10h	0h
14h	17h	Base Address Register High (BAR_HIGH)—Offset 14h	0h
18h	1Bh	Base Address Register 1 (BAR1)—Offset 18h	0h
1Ch	1Fh	Base Address Register1 High (BAR1_HIGH)—Offset 1Ch	0h
2Ch	2Fh	Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch	0h
30h	33h	Expansion ROM base address (EXPANSION_ROM_BASEADDR)—Offset 30h	0h
34h	37h	Capabilities Pointer (CAPABILITYPTR)—Offset 34h	80h
3Ch	3Fh	Interrupt Register (INTERRUPTREG)—Offset 3Ch	100h
80h	83h	PowerManagement Capability ID (POWERCAPID)—Offset 80h	00030001h
84h	87h	PME Control and Status (PMECTRLSTATUS)—Offset 84h	8h
90h	93h	PCI Device Idle Capability Record (PCIDEVIDLE_CAP_RECORD)—Offset 90h	F0140009h
98h	9Bh	SW LTR Update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG)—Offset 98h	0h
9Ch	9Fh	Device IDLE pointer register (DEVICE_IDLE_POINTER_REG)—Offset 9Ch	0h
A0h	A3h	Device PG Config (D0I3_MAX_POW_LAT_PG_CONFIG)—Offset A0h	800h

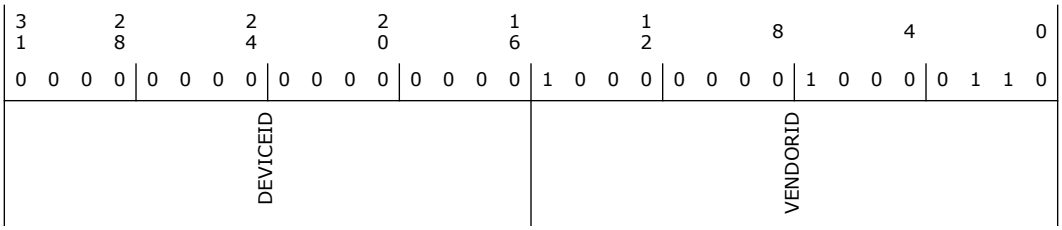
12.1.1 Device ID and Vendor ID Register (DEVVENDID)—Offset 0h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 2

Default: xxxx8086h



Bit Range	Default & Access	Field Name (ID): Description
31:16	-- RO	**Device Identification (DEVICEID):** This is a 16-bit value assigned to the controller See the Device and Version ID Table in Volume 1 for the default value.
15:0	8086h RO	**Vendor Identification (VENDORID)** Identifies the manufacturer of the device.

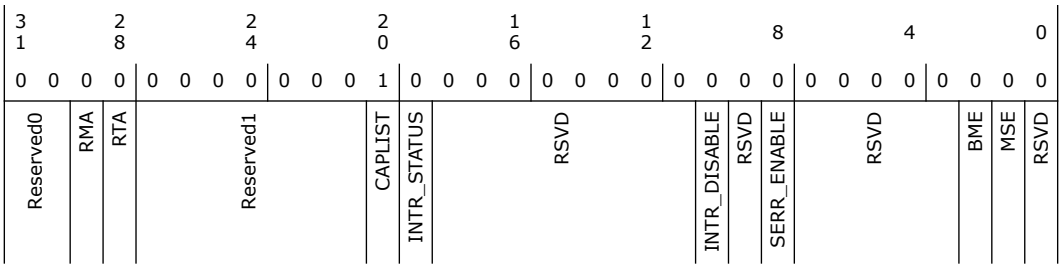
12.1.2 Status and Command (STATUSCOMMAND)—Offset 4h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 2

Default: 100000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved
29	0h RW/1C	**Received Master Abort (RMA):** If the completion status received from is UR, this bit is set. S/W writes a '1' to this bit to clear it.
28	0h RW/1C	**Received Target Abort (RTA):** If the completion status received is CA, this bit is set. S/W writes a '1' to this bit to clear it.
27:21	0h RO	Reserved
20	1h RO	**CAPLIST**

Bit Range	Default & Access	Field Name (ID): Description
19	0h RO	**Interrupt Status (INTR_STATUS):** This bit reflects state of interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the device's/function's interrupt message be sent. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. This bit reflects Legacy interrupt status.
18:11	0h RO	Reserved.
10	0h RW	**Interrupt Disable (INTR_DISABLE):** Setting this bit disables INTx assertion. The interrupt disabled is legacy INTx# interrupt.
9	0h RO	Reserved.
8	0h RW	**SERR# Enable (SERR_ENABLE):** Not implemented
7:3	0h RO	Reserved.
2	0h RW	**Bus Master Enable (BME)**
1	0h RW	**Memory Space Enable (MSE):** 0 = Disables memory mapped Configuration space. 1 = Enables memory mapped Configuration space.
0	0h RO	Reserved.

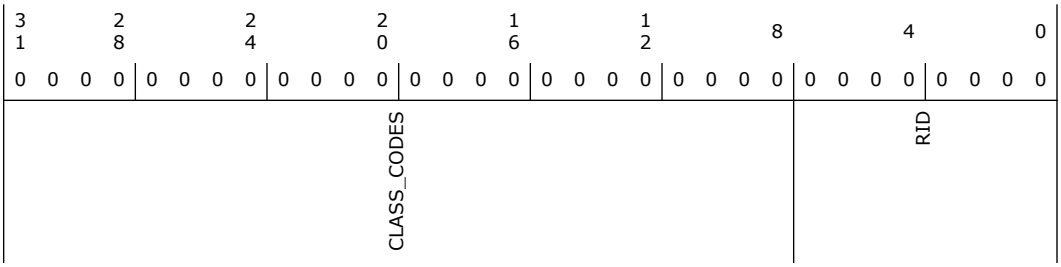
12.1.3 Revision ID and Class Code (REVCLASSCODE)—Offset 8h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 2

Default: 118000XXh



Bit Range	Default & Access	Field Name (ID): Description
31:8	118000h RO	**Class Codes (CLASS_CODES):** The register is read-only and is used to identify the generic function of the device.
7:0	-- RO	**Revision ID (RID):** Indicates stepping of the host controller. Refer to Device and Revision ID table in Volume 1 for specific value.

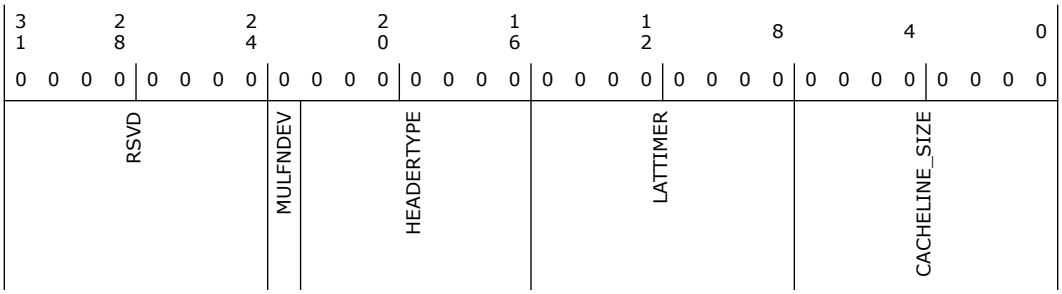
12.1.4 Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RO	**Multi Function Device (MULFNDEV):** 0 = Single Function Device 1 = Multi Function device
22:16	0h RO	**Header Type (HEADERTYPE):** Implements Type 0 Configuration header.
15:8	0h RO	**Latency Timer (LATTIMER)**
7:0	0h RW	**Cache Line Size (CACHELINE_SIZE)**

12.1.5 Base Address Register (BAR)—Offset 10h

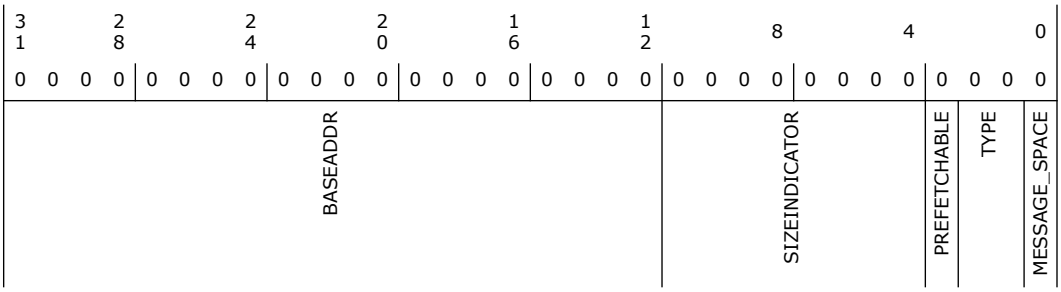
Bits [31:12] indicate the Base Address register. Power-up software can determine how much address space the Interface Module requires by writing a value of all ones to the register and then reading the value back. The register returns zeros in all don't-care address bits, effectively specifying the address space required.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW	**Base Address (BASEADDR):** Provides system memory base address for the controller.
11:4	0h RO	**SIZEINDICATOR**
3	0h RO	**Prefetchable (PREFETCHABLE):** Indicates that this BAR is not prefetchable.
2:1	0h RO	**Type (TYPE):** 00 indicates BAR lies in 32bit address range 10 Indicates BAR lies in 64 bit address range
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE):** '0' Indicates this BAR is present in the memory space.

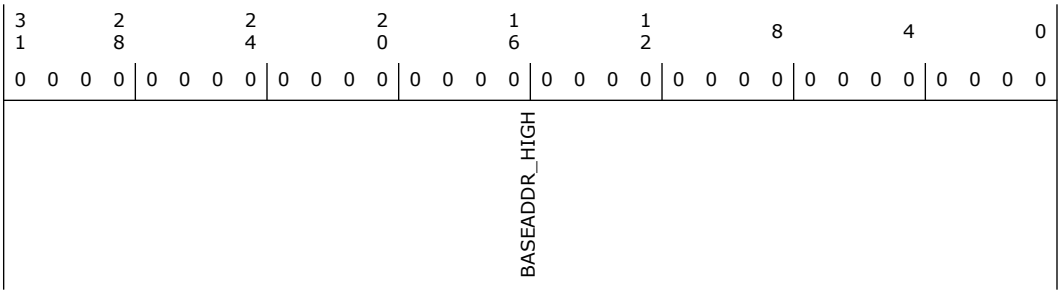
12.1.6 Base Address Register High (BAR_HIGH)—Offset 14h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Base Address High (BASEADDR_HIGH)**

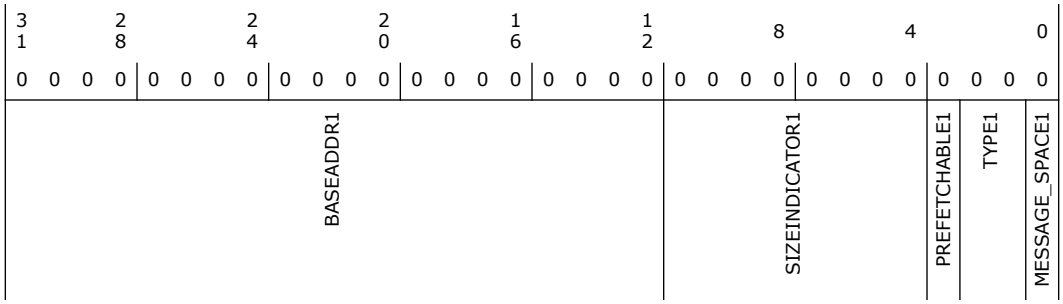
12.1.7 Base Address Register 1 (BAR1)—Offset 18h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW	**BASEADDR1**
11:4	0h RO	**SIZEINDICATOR1**
3	0h RO	**Prefetchable (PREFETCHABLE1):** Indicates that this BAR is not prefetchable.
2:1	0h RO	**Type (TYPE1):** 00 indicates BAR lies in 32bit address range 10 Indicates BAR lies in 64 bit address range.
0	0h RO	**MESSAGE_SPACE1**

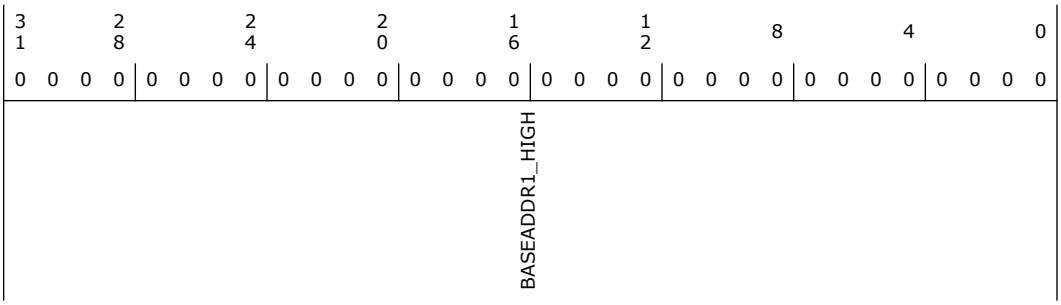
12.1.8 Base Address Register1 High (BAR1_HIGH)—Offset 1Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**BASEADDR1_HIGH**

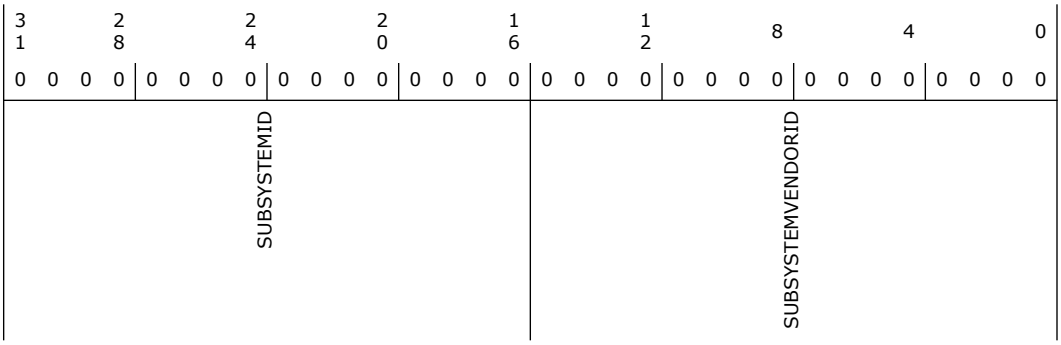
12.1.9 Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW/O	**Subsystem ID (SUBSYSTEMID):** The register, in combination with the Subsystem Vendor ID register make it possible for the operating environment to distinguish one subsystem from the other. This register is a Read Write Once type register.
15:0	0h RW/O	**Subsystem Vendor ID (SUBSYSTEMVENDORID):** The register, in combination with the Subsystem ID register, enables the operating environment to distinguish one subsystem from the other. This register is a Read Write Once register.

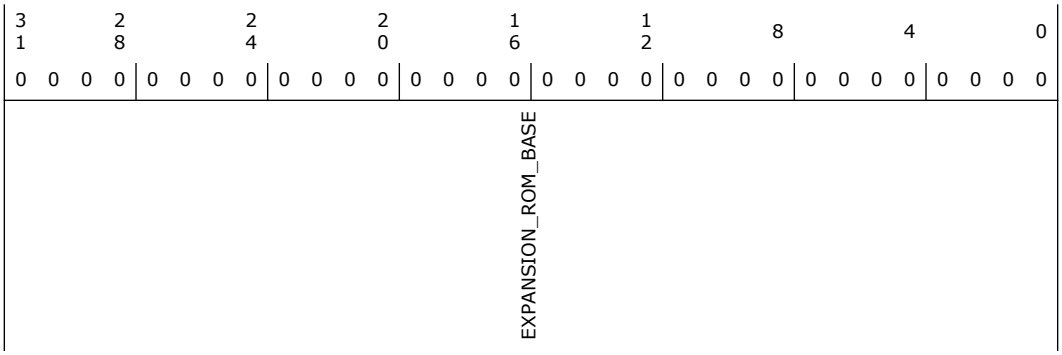
12.1.10 Expansion ROM base address (EXPANSION_ROM_BASEADDR)—Offset 30h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**Expansion ROM Base (EXPANSION_ROM_BASE)** Value of 0 indicates no support for Expansion ROM.

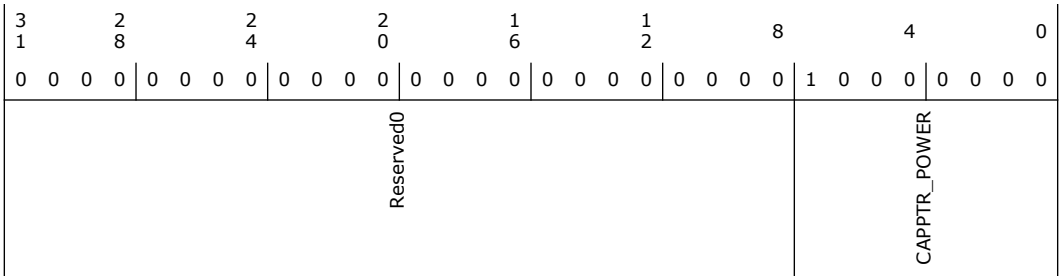
12.1.11 Capabilities Pointer (CAPABILITYPTR)—Offset 34h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 2

Default: 80h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved
7:0	80h RO	**Capability Pointer (CAPPTR_POWER):** Indicates what the next capability is. This capability points to the PM Capability (0x80) structure.

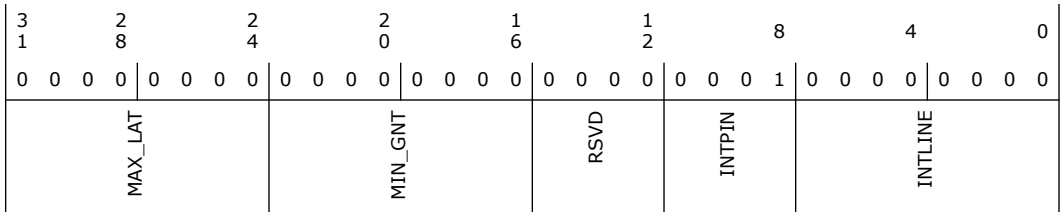
12.1.12 Interrupt Register (INTERRUPTREG)—Offset 3Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 2

Default: 100h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Max Latency (MAX_LAT):** Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	0h RO	**Min Latency (MIN_GNT):** Value of 0 indicates device has no major requirements for the settings of latency timers
15:12	0h RO	Reserved.
11:8	1h RO	**Interrupt Pin (INTPIN)**
7:0	0h RW	**Interrupt Line (INTLINE):** Used to communicate to software the interrupt line that the interrupt pin is connected to.

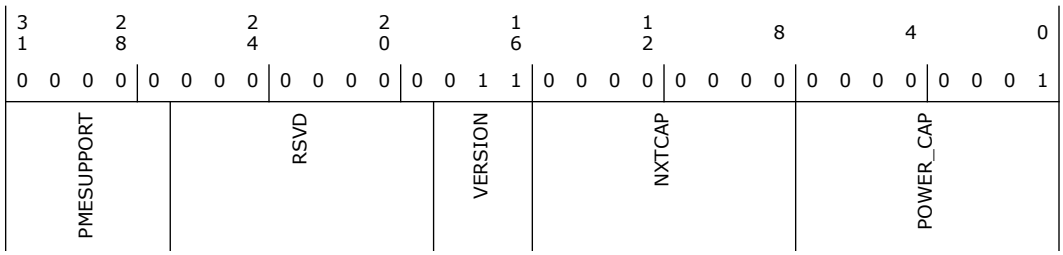
12.1.13 PowerManagement Capability ID (POWERCAPID)—Offset 80h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 2

Default: 48030001h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**PME Support (PMESUPPORT)**
26:19	0h RO	Reserved.
18:16	3h RO	**VERSION:** Indicates support for Revision 1.2 of the PCI Power Management Specification
15:8	0h RO	**Next Capability (NXTCAP):** Points to the next capability structure. This points to NULL.
7:0	1h RO	**Power Management Capability (POWER_CAP):** Indicates power management capability.

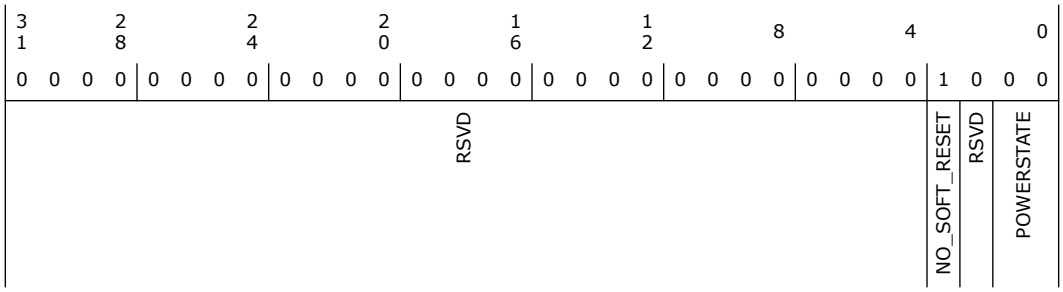
12.1.14 PME Control and Status (PMECTRLSTATUS)—Offset 84h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 2

Default: 8h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3	1h RO	**No Soft Reset (NO_SOFT_RESET):** When set, this bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved.
2	0h RO	Reserved.
1:0	0h RW	**Power State (POWERSTATE):** This field is used both to determine the current power state and to set a new power state. The values are: 00 = D0 state 11 = D3HOT state Others = Reserved Notes: If software attempts to write a value of 01b or 10b in to this field,the data is discarded and no state change occurs. When in the D3HOT states, interrupts are blocked.

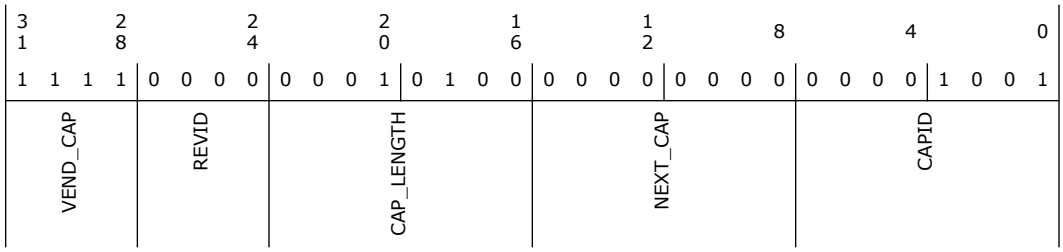
12.1.15 PCI Device Idle Capability Record (PCIDEVIDLE_CAP_RECORD)—Offset 90h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 2

Default: F0140009h



Bit Range	Default & Access	Field Name (ID): Description
31:28	Fh RO	**Vendor Capability (VEND_CAP):** Indicates this is Vendor Specific capability.
27:24	0h RO	**Revision ID (REVID):** Revision ID of capability structure
23:16	14h RO	**CAP_LENGTH**
15:8	0h RO	**Next Capability (NEXT_CAP):** Points to the next capability structure. This points to NULL.
7:0	9h RO	**Capability ID (CAPID)**

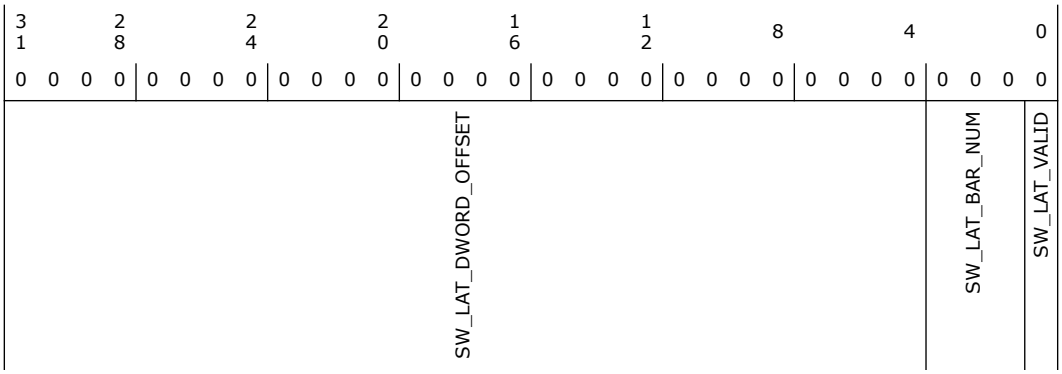
12.1.16 SW LTR Update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG)—Offset 98h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Location Pointer Offset (SW_LAT_DWORD_OFFSET):** This register contains the location pointer to the SW LTR register in MMIO space, as an offset from the specified BAR. The value of this register is a don't care, if the Valid bit is not set.
3:1	0h RO	**BAR Number (SW_LAT_BAR_NUM):** Indicates that the SW LTR update MMIO location is always at BAR0.
0	0h RO	**Valid (SW_LAT_VALID)**

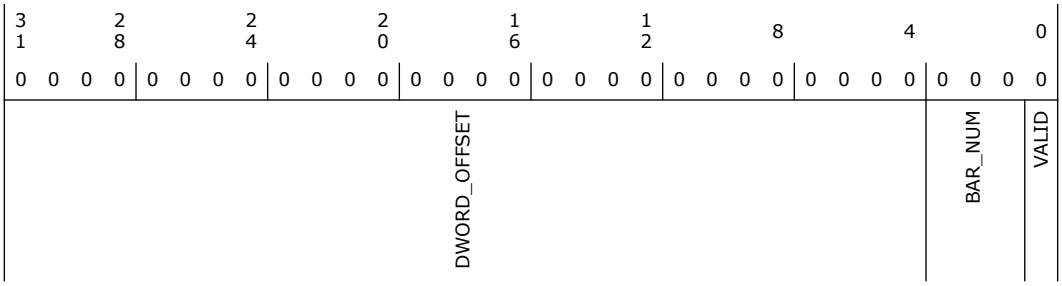
12.1.17 Device IDLE pointer register (DEVICE_IDLE_POINTER_REG)—Offset 9Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**DevIdle Pointer (DWORD_OFFSET):** This register contains the location pointer to the DevIdle register in MMIO space, as an offset from the specified BAR. The value of this register is a don't care, if the Valid bit is not set.
3:1	0h RO	**BAR Number (BAR_NUM):** Indicates that the DevIdle update MMIO location is always at BAR0
0	0h RO	**Valid (VALID):** 0= not valid 1= valid

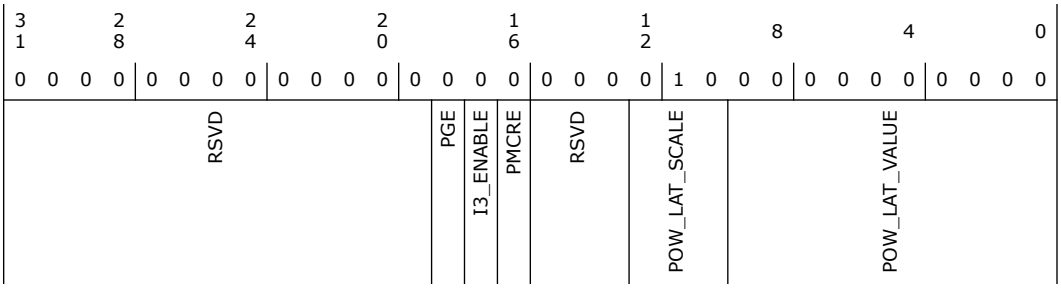
12.1.18 Device PG Config (D0I3_MAX_POW_LAT_PG_CONFIG)—Offset A0h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 2

Default: 800h



Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	Reserved.
18	0h RW	**Power Gate Enable (PGE):** If clear, then the controller will never request a PG. If set, then the controller may request PG when proper conditions are met. Note: This Bit must be set by BIOs for PG to function
17	0h RW	**I3 Enable (I3_ENABLE):** If '1', then the function will power gate when idle and the DevIdle register (DevIdleC[2] = '1') is set.
16	0h RW	**PMC Request Enable (PMCRE):** If this bit is set to '1', the function will power gate when idle.
15:13	0h RO	Reserved.
12:10	2h RW/O	**Power On Latency Scale (POW_LAT_SCALE):** Support for codes 010 (1us) or 011 (32us) for Exit Latency Scale (1us - 32ms total span) only. This value is written by BIOS to communicate to the Driver.
9:0	0h RW/O	**Power On Latency Value (POW_LAT_VALUE):** This value is written by BIOS to communicate to the Driver.

12.2 Generic SPI (GSPI) Memory Mapped Registers Summary

Table 12-2. Summary of Generic SPI (GSPI) Memory Mapped Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	SSP (GSPI) Control Register 0 (SSCR0)—Offset 0h	0h
4h	7h	SSP (GSPI) Control Register 1 (SSCR1)—Offset 4h	0h
8h	Bh	SSP (GSPI) Status Register (SSSR)—Offset 8h	4h
10h	13h	SSP (GSPI) Data (SSDR)—Offset 10h	0h
28h	2Bh	SSP (GSPI) Time Out (SSTO)—Offset 28h	0h
44h	47h	SPI Transmit FIFO (SITF)—Offset 44h	0h
48h	4Bh	SPI Receive FIFO (SIRF)—Offset 48h	0h

12.2.1 SSP (GSPI) Control Register 0 (SSCR0)—Offset 0h

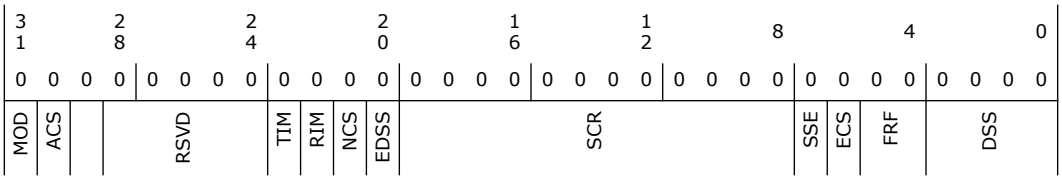
All bits must be set to the preferred value before enabling the Enhanced SSP. Note that Writes to reserved bits must be zeroes, and Read values of these bits is undetermined.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**MOD (MOD):** Mode Set to 0 - Normal SSP Mode : Full Duplex Serial peripheral interface. 1 = reserved
30	0h RW	**ACS (ACS):** Audio Clock Select 0 - Clock selection is determined by the NCS and ECS bits 1 - reserved
29	0h RW	**Reserved**
28:24	0h RO	Reserved.
23	0h RW	**TIM (TIM):** Transmit FIFO Under Run Interrupt Mask When set, this bit will mask the Transmit FIFO Under Run (TUR) event from generating an SSP interrupt. The SSSR status register will still indicate that an TUR event has occurred. This bit can be written to at any time (before or after SSP is enabled). 0 = Transmit FIFO Under Run(TUR) events will generate an SSP interrupt 1 = TUR events will be masked

Bit Range	Default & Access	Field Name (ID): Description
22	0h RW	**RIM (RIM):** Receive FIFO Over Run Interrupt Mask When set, this bit will mask the Receive FIFO Over Run (ROR) event from generating an SSP interrupt. The SSSR status register will still indicate that an ROR event has occurred. This bit can be written to at any time (before or after SSP is enabled) 0 = receive FIFO Over Run(ROR) events will generate an SSP interrupt 1 = ROR events will be masked
21	0h RW	**NCS (NCS):** Network Clock Select The SSCR0.NCS bit in conjunction with SSCR0.ECS determines which clock is used. 0 - Clock selection is determined by ECS bit 1 – Reserved
20	0h RW	**EDSS (EDSS):** Extended Data Size Select The 1-bit extended field is used in conjunction with the data size select SSCR0.DSS bits to select the size of the data transmitted and received by the Enhanced SSP. 0 = A zero is prepended to the DSS value which sets the DSS range from 4-16 bits 1 = A one is pre-appended to the DSS value which sets the DSS range from 17-32 bits
19:8	0h RW	**SCR (SCR):** Serial Clock Rate Value (0 to 4095) used to generate transmission rate of SSP. Serial bit rate = SSP clock/(SCR+1), where SCR is decimal integer.
7	0h RW	**SSE (SSE):** Synchronous Serial Port Enable 0 - SSP operation disabled 1 - SSP operation enabled
6	0h RW	**ECS (ECS):** External Clock Select: 0 = use On-chip clock (output of M/N Divider) to produce the SSP's serial clock (SSPSCLK). Selects the use of the the output of the M/N Divider (MBAR0 + 0x800, CLOCKS) to create the SSP's serial clock (SSPCLK) Note: Setting M=N=1 will provide a pass through of the M/N Divider of the serial clock. See SCR for Serial Clock Rate generation. 1 = Reserved
5:4	0h RW	**FRF (FRF):** Frame Format Set to 00 - Motorola Serial Peripheral Interface (SPI) 01 - 10 = reserved
3:0	0h RW	**DSS (DSS):** Data Size Select With EDSS as MSB, value+1 gives data size. Values 4 to 32 allowed.

12.2.2 SSP (GSPI) Control Register 1 (SSCR1)—Offset 4h

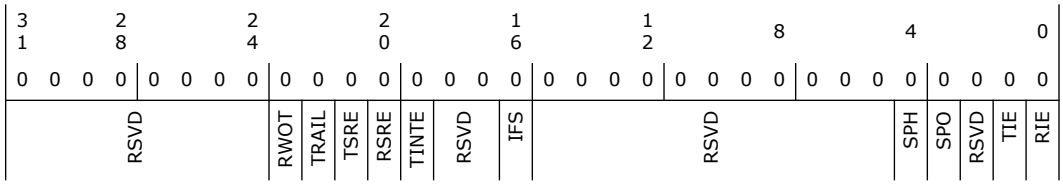
The Enhanced SSP Control 1 registers contain bit fields that control various SSP functions. Bits must be set to the preferred value before enabling the Enhanced SSP. Note that Writes to reserved bits should be zeroes, and Read value of these bits are undetermined.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RW	**RWOT (RWOT):** Receive With Out Transmit 0 = Transmit/Receive mode 1 = Receive without transmit mode
22	0h RW	**TRAIL (TRAIL):** Trailing Byte 0 = Processor based, trailing bytes are handled by processor 1 - DMA based, trailing bytes are handled by DMA
21	0h RW	**TSRE (TSRE):** Transmit Service Request Enable 0 = DMA Service Request is disabled 1 = DMA Service Request is enabled
20	0h RW	**RSRE (RSRE):** Receive Service Request Enable 0 = DMA Service Request is disabled 1 = DMA Service Request is enabled
19	0h RW	**TINTE (TINTE):** Receiver Time-out Interrupt Enable 0 - Receiver Time-out interrupts are disabled 1 - Receiver Time-out interrupts are enabled
18:17	0h RO	Reserved.
16	0h RW	**IFS (IFS):** Invert Frame Signal 0 = Frame signal (Chip Select) is active low 1 = Frame signal (Chip Select) is active high
15:5	0h RO	Reserved.
4	0h RW	**SPH (SPH):** Motorola SPI SSPSCLK phase setting 0 = SSPSCLK is inactive one sycle at the start of a frame and cycle at the end of a frame 1 = SSPSCLK is inactive for one half cycle at the start of a frame and one cycle at the end of a frame
3	0h RW	**SPO (SPO):** Motorola SPI SSPSCLK polarity setting 0 = The inactive or idle state of SSPSCLK is low 1 = The inactive or idle state of SSPSCLK is high
2	0h RO	Reserved.
1	0h RW	**TIE (TIE):** Transmit FIFO Interrupt Enable 0 = Transmit FIFO level interrupt is disabled 1 = Transmit FIFO level interrupt is enabled
0	0h RW	**RIE (RIE):** Receive FIFO Interrupt Enable 0 = Receive FIFO level interrupt is disabled 1 = Receive FIFO level interrupt is enabled

12.2.3 SSP (GSPI) Status Register (SSSR)—Offset 8h

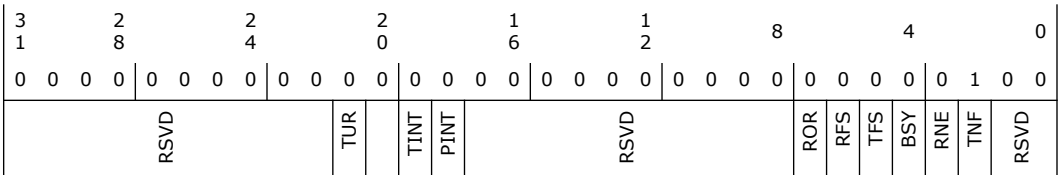
The Enhanced SSP Status registers contain bits that signal overrun errors as well as the Transmit and Receive FIFO service requests. Each of these hardware-detected events signals an Interrupt request to the Interrupt controller. The Status register also contains flags that indicate when the Enhanced SSP is actively transmitting data, when the Transmit FIFO is not full, and when the Receive FIFO is not empty. One Interrupt signal is sent to the Interrupt Controller for each SSP. These events can cause an Interrupt: End-of-Chain, Receiver Time-out, Peripheral Trailing Byte, Receive FIFO overrun, Receive FIFO request, and Transmit FIFO request.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 2

Default: 4h



Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	Reserved.
21	0h RW1C	**TUR (TUR):** Transmit FIFO Under Run 0 = Transmit FIFO has not experienced an under run 1 = Attempted read from the transmit FIFO when the FIFO was empty, request interrupt
20	0h RW1C	**Reserved**
19	0h RW1C	**TINT (TINT):** Receiver Time-out Interrupt 0 = No receiver time-out pending 1 = Receiver time-out pending
18	0h RW1C	**PINT (PINT):** Peripheral Trailing Byte Interrupt 0 - No peripheral trailing byte interrupt pending 1 - Peripheral trailing byte interrupt pending
17:8	0h RO	Reserved.
7	0h RW1C	**ROR (ROR):** Receive FIFO Overrun 0 = Receive FIFO has not experienced an overrun 1 = Attempted data write to full receive FIFO, request interrupt
6	0h RO	**RFS (RFS):** Receive FIFO Service Request 0 = Receive FIFO level is at or below RFT threshold (RFT), or SSP disabled 1 = Receive FIFO level exceeds RFT threshold (RFT), request interrupt
5	0h RO	**TFS (TFS):** Transmit FIFO Service Request 0 = Transmit FIFO level exceeds the Low Water Mark Transmit FIFO (SITF.LWMTF), or SSP disabled 1 = Transmit FIFO level is at or below the Low Water Mark Transmit FIFO (SITF.LWMTF), request interrupt
4	0h RO	**BSY (BSY):** SSP Busy 0 = SSP is idle or disabled 1 = SSP currently transmitting or receiving a frame
3	0h RO	**RNE (RNE):** Receive FIOF Not Empty 0 = Receive FIFO is empty 1 = Receive FIFO is not empty
2	1h RO	**TNF (TNF):** Transmit FIFO Not Full 0 = Transmit FIFO is full 1 = Transmit FIFO is not full
1:0	0h RO	Reserved.

12.2.4 SSP (GSPI) Data (SSDR)—Offset 10h

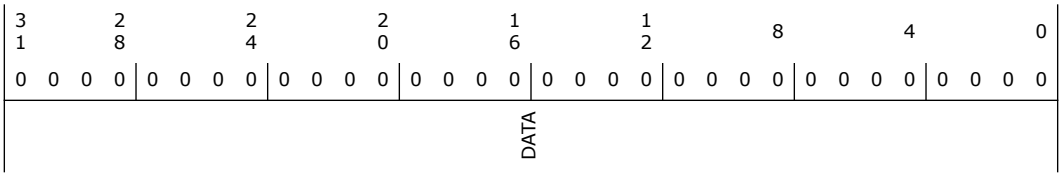
The Enhanced SSP Data registers are single address locations that Read-Write data transfers can access.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**DATA (DATA):** Data word to be written to/read from transmit/receive FIFO

12.2.5 SSP (GSPI) Time Out (SSTO)—Offset 28h

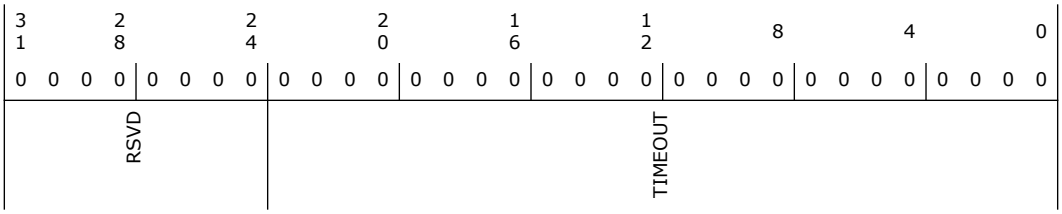
The Enhanced SSP Time-Out registers have single bit fields that specify the time-out value used to signal a period of inactivity within the Receive FIFO. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:0	0h RW	**TIMEOUT (TIMEOUT):** Timeout Value Is the value that defines the timeout interval for the rcv FIFO. The Interval is given by TIMEOUT/Parallel (Bus) Clock Frequency. When the number of samples in the Receive FIFO is less than rcv FIFO trigger threshold level, and no additional data is received, the Timeout timer will decrement. The time-out timer is reset after a new sample is received. In DMA Mode of operation this value needs to be set when the Rcv FIFO Trigger Threshold is greater than 1 Rcv FIFO Entry (the required MSize (Single Burst) for SSP DMA peripheral transfers) When in PIO mode of operation this value needs to be set when the total transfer size is not a even divison of the Rcv FIFO trigger threshold level. Is such a case the TIMEOUT value is calculated to be greater than the time to transfer the FIFO Entry size at the desired Bit Rate.

12.2.6 SPI Transmit FIFO (SITF)—Offset 44h

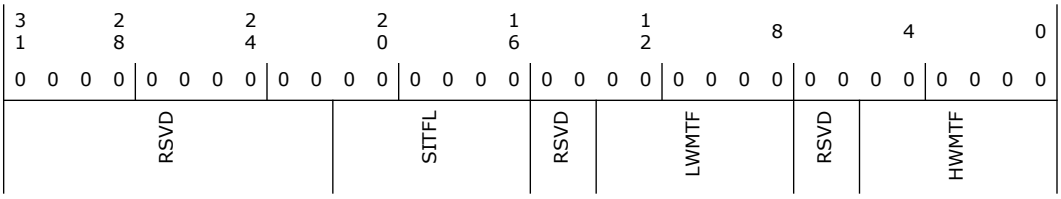
The SPI Transmit FIFO register is for writing the water mark for the SPI transmit FIFO and also for reading the number of entries in the SPI transmit FIFO

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	Reserved.
21:16	0h RO	**SITFL (SITFL):** SPI Transmit FIFO Level Number of entries in SPI Transmit FIFO.
15:14	0h RO	Reserved.
13:8	0h RW	**LWMTF (LWMTF):** Low Water Mark Transmit FIFO. Set the low water mark of the SPI transmit FIFO. 6'b000000 = 1 entry through 6'b111111 = 64 entries
7:6	0h RO	Reserved.
5:0	0h RW	**HWMTF (HWMTF):** High Water Mark Transmit FIFO. Set the high water mark of the SPI transmit FIFO. 6'b000000 = 1 entry through 6'b111111 = 64 entries

12.2.7 SPI Receive FIFO (SIRF)—Offset 48h

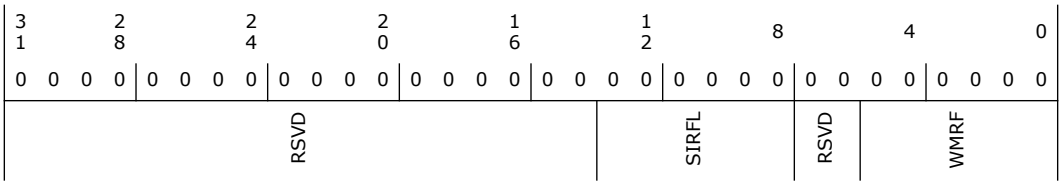
The SPI Receive FIFO register is for writing the water mark for the SPI receive FIFO and also for reading the number of entries in the SPI receive FIFO

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:8	0h RO	**SIRFL (SIRFL):** SPI Receive FIFO Level Number of entries in SPI Receive FIFO.
7:6	0h RO	Reserved.
5:0	0h RW	**WMRF (WMRF):** Water Mark Receive FIFO. Set the water mark of the SPI receive FIFO. 6'b000000 = 1 entry through 6'b111111 = 64 entries

12.3 Generic SPI (GSPI) Additional Registers Summary

The registers in this section are memory mapped based on the BAR defined in PCI configuration space.

Table 12-3. Summary of Generic SPI (GSPI) Additional Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
200h	203h	CLOCKS (CLOCKS)—Offset 200h	0h
204h	207h	RESETS (RESETS)—Offset 204h	0h
210h	213h	ACTIVE LTR (ACTIVELTR_VALUE)—Offset 210h	800h
214h	217h	Idle LTR Value (IDLELTR_VALUE)—Offset 214h	800h
218h	21Bh	TX Bit Count (TX_BIT_COUNT)—Offset 218h	0h
21Ch	21Fh	Rx Bit Count (RX_BIT_COUNT)—Offset 21Ch	0h
220h	223h	reg_SSP_REG (SSP_REG)—Offset 220h	0h
224h	227h	SPI CS CONTROL (SPI_CS_CONTROL)—Offset 224h	1000h
228h	22Bh	SW SCRATCH [3:0] (SW_SCRATCH)—Offset 228h	0h

Table 12-3. Summary of Generic SPI (GSPI) Additional Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
238h	23Bh	Clock Gate (CLOCK_GATE)—Offset 238h	0h
240h	243h	Remap Address Low (REMAP_ADDR_LO)—Offset 240h	0h
244h	247h	Remap Address High (REMAP_ADDR_HI)—Offset 244h	0h
24Ch	24Fh	Device Idle Control (DEVIDLE_CONTROL)—Offset 24Ch	8h
250h	253h	Delay Rx Clock (DEL_RX_CLK)—Offset 250h	0h
2FCh	2FFh	Capabilities (CAPABLITIES)—Offset 2FCh	1E20h

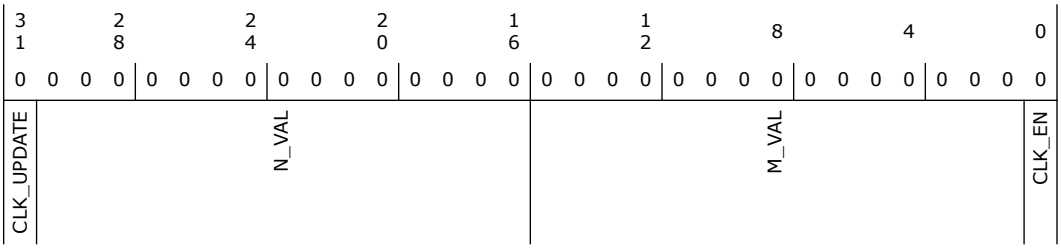
12.3.1 CLOCKS (CLOCKS)—Offset 200h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Clock Update (CLK_UPDATE):** Update the clock divider after seeing new m and n values 0 = No clock Update. 1 – Clock gets updated.
30:16	0h RW	**N_VAL (N_VAL):** n value for the m over n divider
15:1	0h RW	**M_Value (M_VAL):** m value for the m over n divider.
0	0h RW	**Clock Enable (CLK_EN):** Clock Enable of the m over n divider 0 = Clock disabled 1 = Clock Enabled.

12.3.2 RESETS (RESETS)—Offset 204h

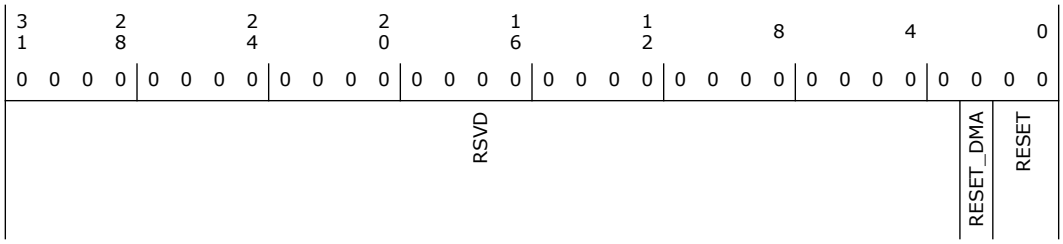
Software reset

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	Reserved.
2	0h	**DMA Reset (RESET_DMA):** DMA Software Reset Control 0 = DMA is in reset (Reset Asserted) 1 = DMA is NOT at reset (Reset Released)
1:0	0h	**Host Controller reset (RESET):** Used to reset the Host Controller by SW control. All SSP Configuration State and Operational State will be forced to the Default state. There is no timing requirement (SW can assert and de-assert in back to back transactions) 00 = Host Controller is in reset (Reset Asserted) 01 = Reserved 10 = Reserved 11 = Host Controller is NOT at reset (Reset Released)

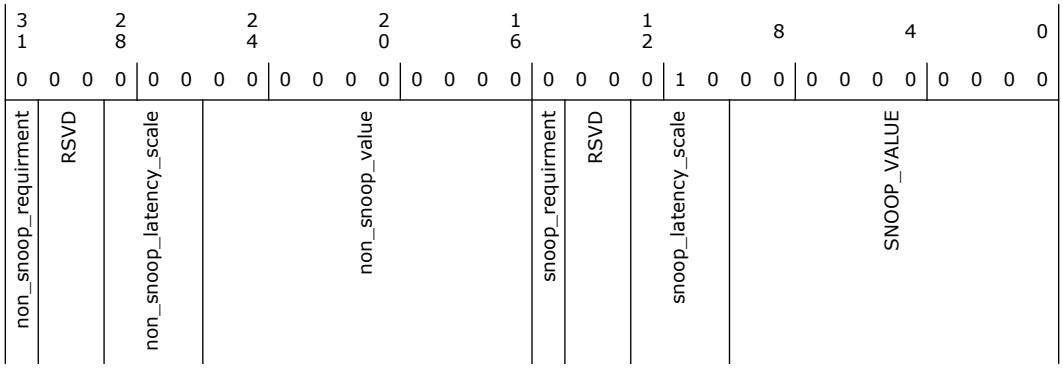
12.3.3 ACTIVE LTR (ACTIVELTR_VALUE)—Offset 210h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 800h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Non Snoop Requirment (non_snoop_requirment):** If the Requirement (bit 15) is clear, that indicates that the device has no LTR requirement for this type of traffic (i.e. it can wait for service indefinitely). If the 10-bit latency value is zero it indicates that the device cannot tolerate any delay and needs the best possible service/ response time.
30:29	0h RO	Reserved.
28:26	0h RO	**Non-Snoop Latency Scale (non_snoop_latency_scale):** Support for codes 010 (1us) or 011 (32us) for Snoop Latency Scale (1us -> 32ms total span) only. Writes to this CSR which dont match those values will be dropped completely, next read will return previous value.
25:16	0h RO	**Non-Snoop Value (non_snoop_value):** 10-bit latency value
15	0h RW	**Snoop Requirement (snoop_requirment):** If the Requirement (bit 15) is clear, that indicates that the device has no LTR requirement for this type of traffic (i.e. it can wait for service indefinitely). If the 10-bit latency value is zero it indicates that the device cannot tolerate any delay and needs the best possible service/response time.
14:13	0h RO	Reserved.
12:10	2h RW	**Snoop Latency Scale (snoop_latency_scale):** Support for codes 010 (1us) or 011 (32us) for Snoop Latency Scale(1us -> 32ms total span) only. Writes to this CSR which dont match those values will be dropped completely, next read will return previous value.
9:0	0h RW	**Snoop Value (SNOOP_VALUE):** 10-bit latency value

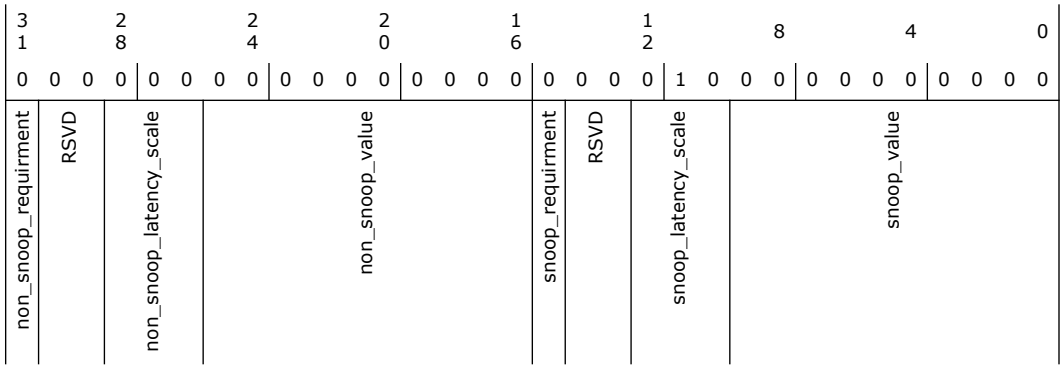
12.3.4 Idle LTR Value (IDLELTR_VALUE)—Offset 214h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 800h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Non Snoop Requirment (non_snoop_requirment):** If the Requirement (bit 15) is clear, that indicates that the device has no LTR requirement for this type of traffic (i.e. it can wait for service indefinitely). If the 10-bit latency value is zero it indicates that the device cannot tolerate any delay and needs the best possible service/ response time.
30:29	0h RO	Reserved.
28:26	0h RO	**Non Snoop Latency Scale (non_snoop_latency_scale):** Support for codes 010 (1us) or 011 (32us) for Snoop Latency Scale (1us -> 32ms total span) only. Writes to this CSR which dont match those values will be dropped completely, next read will return previous value.
25:16	0h RO	**Non Snoop Value (non_snoop_value):** 10-bit latency value
15	0h RW	**Snoop Requirment (snoop_requirment):** If the Requirement (bit 15) is clear, that indicates that the device has no LTR requirement for this type of traffic (i.e. it can wait for service indefinitely). If the 10-bit latency value is zero it indicates that the device cannot tolerate any delay and needs the best possible service/response time.
14:13	0h RO	Reserved.
12:10	2h RW	**Snoop Latency Scale (snoop_latency_scale):** Support for codes 010 (1us) or 011 (32us) for Snoop Latency Scale(1us -> 32ms total span) only. Writes to this CSR which dont match those values will be dropped completely, next read will return previous value.
9:0	0h	**Snoop Value (snoop_value):** 10-bit latency value.

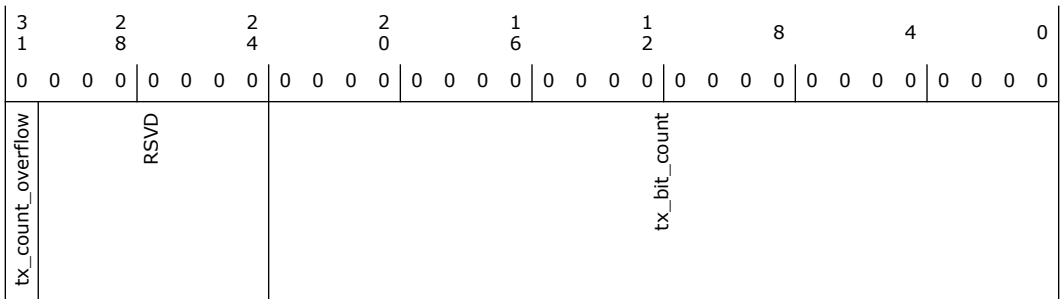
12.3.5 TX Bit Count (TX_BIT_COUNT)—Offset 218h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Tx Count Overflow (tx_count_overflow):** 0 = Count valid 1 = count overflow/invalid
30:24	0h RO	Reserved.
23:0	0h RO	**Tx Bit Count (tx_bit_count):** 24-bit up-counter which counts the number of TX bits on the Serial bus. The counter is forced to be cleared by software Read

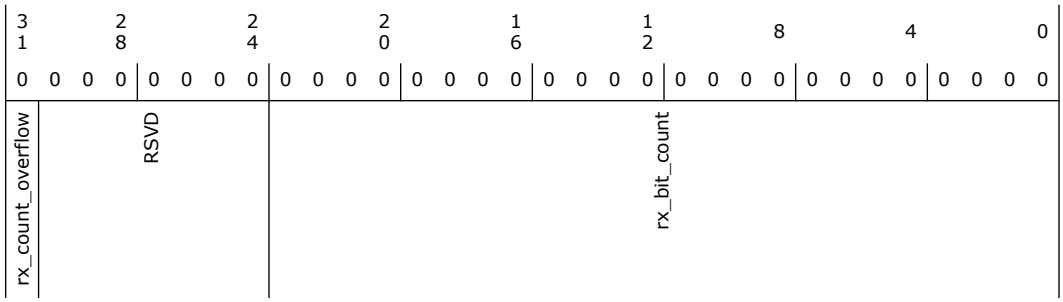
12.3.6 Rx Bit Count (RX_BIT_COUNT)—Offset 21Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Rx Count Overflow (rx_count_overflow):** 0 = count valid 1 = count overflow/invalid
30:24	0h RO	Reserved.
23:0	0h RO	**Rx Bit Count (rx_bit_count):** 24-bit up-counter which counts the number of RX Bits on the Serial bus. The counter is forced to be cleared by software Read

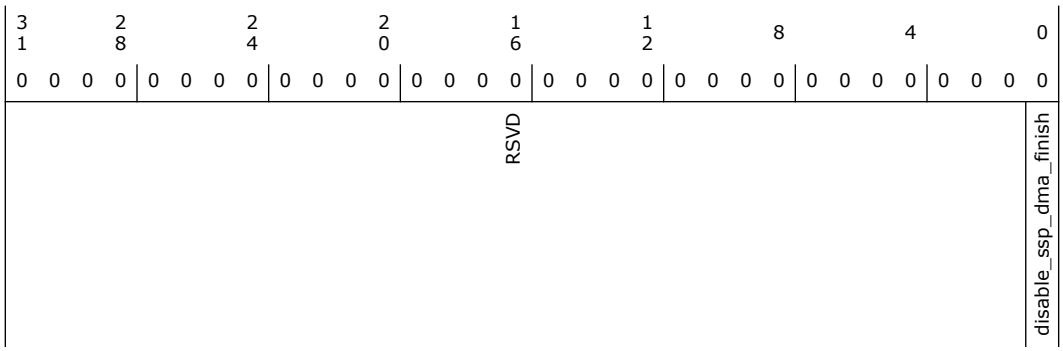
12.3.7 reg_SSP_REG (SSP_REG)—Offset 220h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h	**Disable DMA Finish (disable_ssp_dma_finish):** This bit needs to be set to 1 if SPI is using DMA multi-Block Chaining and the SW driver does not plan to re-enable the DMA manually after every Link List completion 1 = DMA finish Disabled Note: Required for multi-block transfer 0 – DMA finish not disabled.

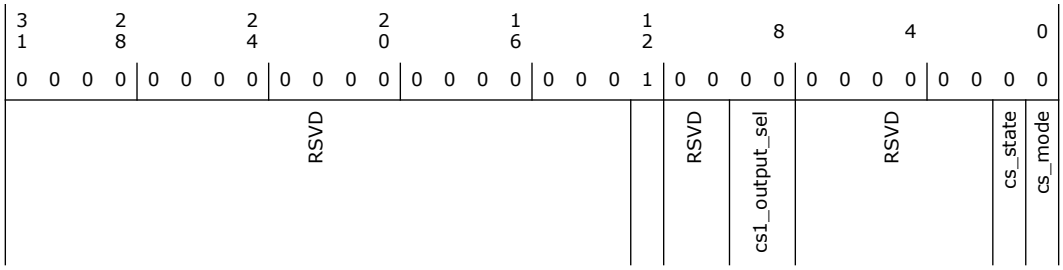
12.3.8 SPI CS CONTROL (SPI_CS_CONTROL)—Offset 224h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 1000h



Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	Reserved.
12	1h	**Chip Select Polarity:** 0 = low, 1 = high
11:10	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h	**cs_output_sel (cs1_output_sel):** These Bits select which SPI CS Signal is to be driven by the SSP Frame (CS). 00 = SPI CS0 01 = Reserved 10 = Reserved 11= Reserved
7:2	0h RO	Reserved.
1	0h	**Chip Select State (cs_state):** Manual SW control of SPI Chip Select (CS) 0 = CS is set to low 1 = CS is set to high
0	0h	**Chip Select Mode (cs_mode):** SPI Chip Select Mode Section. 0 = HW Mode- CS is under SSP control 1 = SW Mode – CS is under SW Control using cs_state bit

12.3.9 SW SCRATCH [3:0] (SW_SCRATCH)—Offset 228h

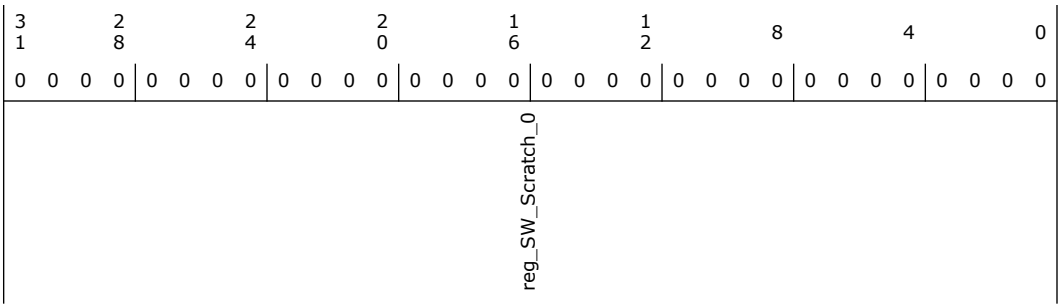
NOTE: The same registers are available at the following offsets:
SW SCRATCH 1: offset 22Ch
SW SCRATCH 2: offset 230h
SW SCRATCH 3: offset 234h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**SW Scratch Pad (reg_SW_Scratch_0):** Scratch Pad Register for SW to generate Local DATA for DMA

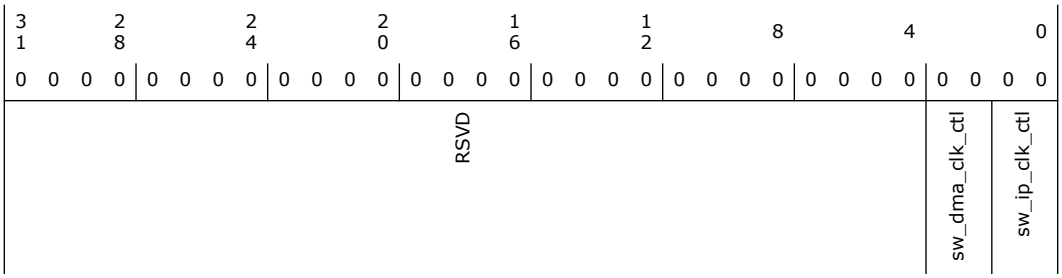
12.3.10 Clock Gate (CLOCK_GATE)—Offset 238h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3:2	0h	**DMA Clock Control (sw_dma_clk_ctl):** DMA Clock Control 00 = Dyanamic Clock Gate Enable 01 = Reserved 10 = Force DMA Clock off 11 = Force DMA Clock on
1:0	0h	**Clock Control (sw_ip_clk_ctl):** Clock Control 00 = Dyanamic Clock Gate Enable 01 = Reserved 10 = Force Clocks off 11 = Force Clocks on

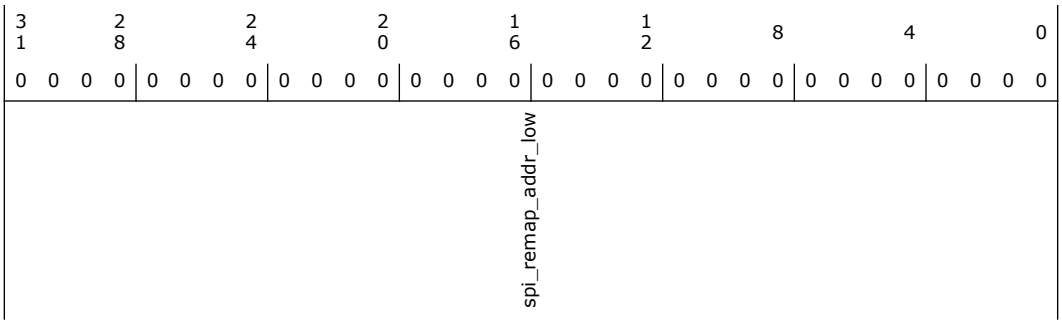
12.3.11 Remap Address Low (REMAP_ADDR_LO)—Offset 240h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Remap Address Low (spi_remap_addr_low):** Low 32 bits of BAR address read by SW

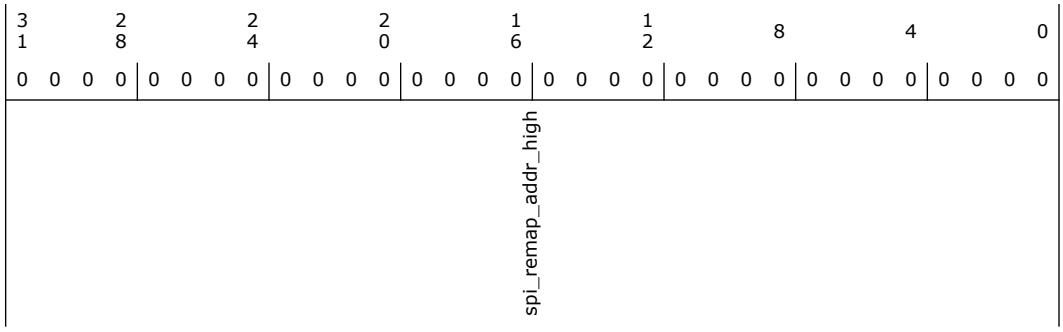
12.3.12 Remap Address High (REMAP_ADDR_HI)—Offset 244h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Remap Address High (spi_remap_addr_high):** High 32 bits of BAR address read by SW

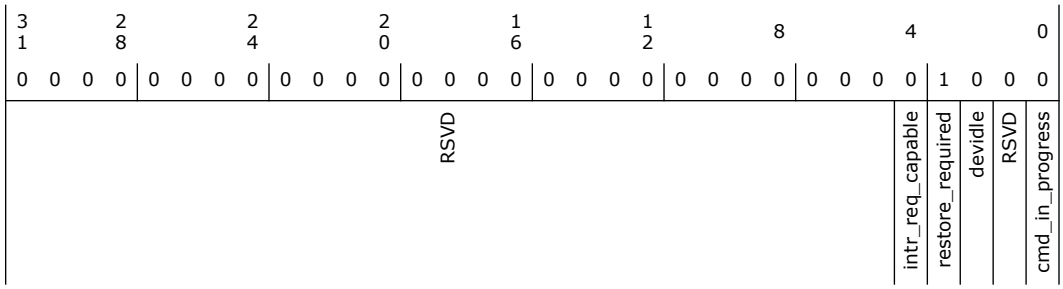
12.3.13 Device Idle Control (DEVIDLE_CONTROL)—Offset 24Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 8h



Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4	0h RO	**Interrupt Request Capable (intr_req_capable):** Set to '1' by HW if it is capable of generating an interrupt on command completion, else '0'.
3	1h RW1C	**Restore Required (restore_required):** When set (by HW), SW must restore state to the controller. The state may have been lost due to a reset or full power lost. SW clears the bit by writing a '1'. This bit will be set on initial power up.
2	0h RW	**Device Idle (devidle):** SW sets this bit to '1' to move the function into the DevIdle state. Writing this bit to '0' will return the function to the fully active D0 state (D0i0).
1	0h RO	Reserved.
0	0h RO	**CMD In Progress (cmd_in_progress):** HW sets this bit on a 1->0 or 0->1 transition of DEVIDLE. While set, the other bits in this register are not valid and it is illegal for SW to write to any bit in this register. HW clears this bit upon completing the DevIdle transition command. When clear, all the other bits in the register are valid and SW may write to any bit. If Interrupt Request (IR) was set for the current command, HW may clear this bit before the interrupt has been made visible to SW, since when SW actually handles a particular interrupt is not visible to the HW. SW writes to this bit have no effect.

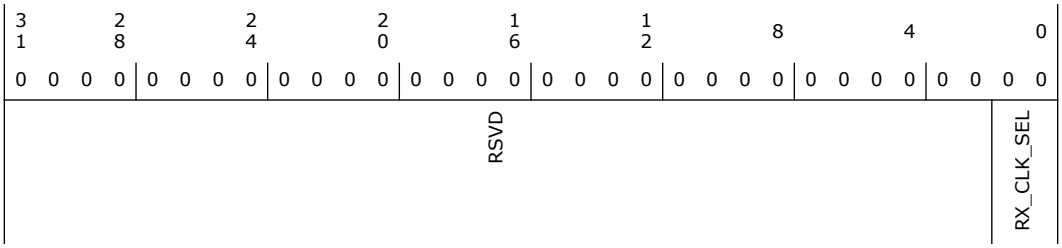
12.3.14 Delay Rx Clock (DEL_RX_CLK)—Offset 250h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RW	**Delayed Rx Clock Select (RX_CLK_SEL):** 00 = The output of the internal (M/N and/or baud rate) clock divider is used as-is to clock in the receive data to the RxFIFO. 01 = An internally delayed version of the internal clock divider output is used to clock in the receive data to the RxFIFO. This allows some additional setup time on the PCH side. 10 = The receive data is clocked on the subsequent negedge of the Tx clock, allowing a full cycle propagation delay on the platform. 11: The receive data is clocked on the subsequent negedge of the delayed Rx clock, maximizing the amount of delay allowed for capturing the receive data. Note: This capability is only supported for default SSP configuration with active high clocks (SSCR1.SPO = 0 and SSCR1.SPH = 0). Other combinations of SPO and SPH setting are not supported for non-zero settings of this field.

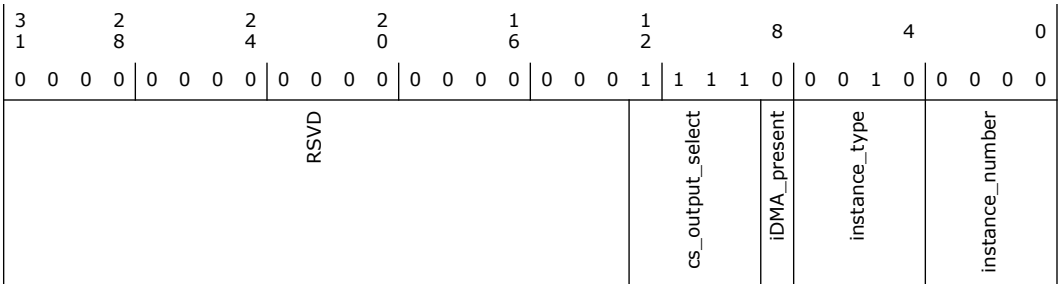
12.3.15 Capabilities (CAPABLITIES)—Offset 2FCh

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 1E20h



Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	Reserved.
12:9	Fh RO	**CS Output Select (cs_output_select):** 0 = Un connected ; 1 = connected
8	0h RO	**DMA Present (iDMA_present):** 0= DMA present 1= DMA not present
7:4	2h RO	**instance_type (instance_type):** 0000 = IC2 0001 = UART 0010 = SPI 0011 – 1111 = Reserved
3:0	0h RO	**Instance Number (instance_number):** 0h: SPI0 1h: SPI1

12.4 Generic SPI (GSPI) DMA Controller Registers Summary

The registers in this section are memory mapped based on the BAR defined in PCI configuration space.

Table 12-4. Summary of Generic SPI (GSPI) DMA Controller Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
800h	803h	DMA Transfer Source Address Low (SAR_LO0)—Offset 800h	0h
804h	807h	DMA Transfer Source Address High (SAR_HI0)—Offset 804h	0h
808h	80Bh	DMA Transfer Destination Address Low (DAR_LO0)—Offset 808h	0h
80Ch	80Fh	DMA Transfer Destination Address High (DAR_HI0)—Offset 80Ch	0h
810h	813h	Linked List Pointer Low (LLP_LO0)—Offset 810h	0h
814h	817h	Linked List Pointer High (LLP_HI0)—Offset 814h	0h
818h	81Bh	Control Register Low (CTL_LO0)—Offset 818h	0h
81Ch	81Fh	Control Register High (CTL_HI0)—Offset 81Ch	0h
820h	823h	Source Status (SSTAT0)—Offset 820h	0h
828h	82Bh	Destination Status (DSTAT0)—Offset 828h	0h
830h	833h	Source Status Address Low (SSTATAR_LO0)—Offset 830h	0h
834h	837h	Source Status Address High (SSTATAR_HI0)—Offset 834h	0h
838h	83Bh	Destination Status Address Low (DSTATAR_LO0)—Offset 838h	0h
83Ch	83Fh	Destination Status Address High (DSTATAR_HI0)—Offset 83Ch	0h
840h	843h	DMA Transfer Configuration Low (CFG_LO0)—Offset 840h	203h
844h	847h	DMA Transfer Configuration High (CFG_HI0)—Offset 844h	0h
848h	84Bh	Source Gather (SGR0)—Offset 848h	0h
850h	853h	Destination Scatter (DSR0)—Offset 850h	0h
AC0h	AC3h	Raw Interrupt Status (RawTfr)—Offset AC0h	0h
AC8h	ACBh	Raw Status for Block Interrupts (RawBlock)—Offset AC8h	0h
AD0h	AD3h	Raw Status for Source Transaction Interrupts (RawSrcTran)—Offset AD0h	0h
AD8h	ADBh	Raw Status for Destination Transaction Interrupts (RawDstTran)—Offset AD8h	0h
AE0h	AE3h	Raw Status for Error Interrupts (RawErr)—Offset AE0h	0h
AE8h	AEBh	Interrupt Status (StatusTfr)—Offset AE8h	0h
AF0h	AF3h	Status for Block Interrupts (StatusBlock)—Offset AF0h	0h
AF8h	AFBh	Status for Source Transaction Interrupts (StatusSrcTran)—Offset AF8h	0h
B00h	B03h	Status for Destination Transaction Interrupts (StatusDstTran)—Offset B00h	0h
B08h	B0Bh	Status for Error Interrupts (StatusErr)—Offset B08h	0h
B10h	B13h	Mask for Transfer Interrupts (MaskTfr)—Offset B10h	0h
B18h	B1Bh	Mask for Block Interrupts (MaskBlock)—Offset B18h	0h
B20h	B23h	Mask for Source Transaction Interrupts (MaskSrcTran)—Offset B20h	0h
B28h	B2Bh	Mask for Destination Transaction Interrupts (MaskDstTran)—Offset B28h	0h
B30h	B33h	Mask for Error Interrupts (MaskErr)—Offset B30h	0h
B38h	B3Bh	Clear for Transfer Interrupts (ClearTfr)—Offset B38h	0h

Table 12-4. Summary of Generic SPI (GSPI) DMA Controller Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
B40h	B43h	Clear for Block Interrupts (ClearBlock)—Offset B40h	0h
B48h	B4Bh	Clear for Source Transaction Interrupts (ClearSrcTran)—Offset B48h	0h
B50h	B53h	Clear for Destination Transaction Interrupts (ClearDstTran)—Offset B50h	0h
B58h	B5Bh	Clear for Error Interrupts (ClearErr)—Offset B58h	0h
B60h	B63h	Combined Status register (StatusInt)—Offset B60h	0h
B98h	B9Bh	DMA Configuration (DmaCfgReg)—Offset B98h	0h
BA0h	BA3h	DMA Channel Enable (ChEnReg)—Offset BA0h	0h

12.4.1 DMA Transfer Source Address Low (SAR_LO0)—Offset 800h

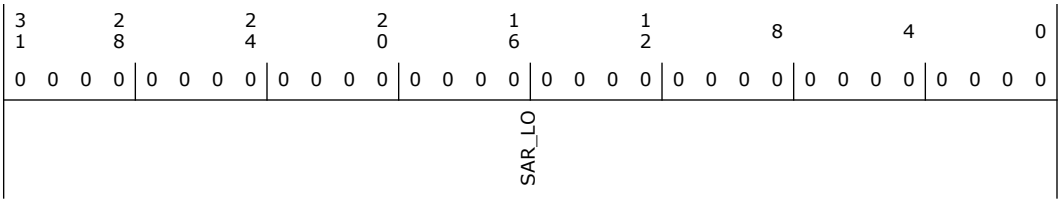
NOTE: SAR_LO0 is for DMA Channel 0. The same register definition,SAR_LO1, is available for Channel 1 at address 858h.
SAR_LO0 (CH0): offset 800h
SAR_LO1 (CH1): offset 858h
The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

Access Method

Type: MEM Register (Size: 32 bits)

Device: 30
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**SAR_LO:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length > 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported.

12.4.2 DMA Transfer Source Address High (SAR_HI0)—Offset 804h

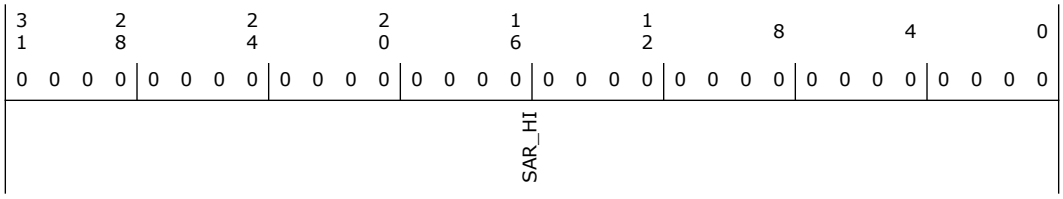
NOTE: SAR_HI0 is for DMA Channel 0. The same register definition, SAR_HI1, is available for Channel 1 at address 85Ch.
SAR_HI0 (CH0): offset 804h
SAR_HI1 (CH1): offset 85Ch
The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**SAR_HI:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length > 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported.

12.4.3 DMA Transfer Destination Address Low (DAR_LO0)—Offset 808h

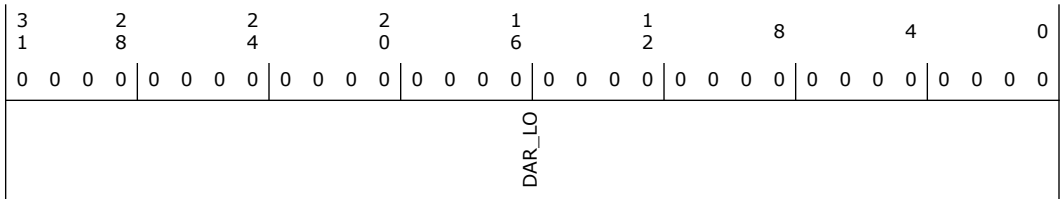
NOTE: DAR_LO0 is for DMA Channel 0. The same register definition, DAR_LO1, is available for Channel 1 at address 860h.
DAR_LO0 (CH0): offset 808h
DAR_LO1 (CH1): offset 860h
The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DAR_LO:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length > 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported.

12.4.4 DMA Transfer Destination Address High (DAR_HI0)—Offset 80Ch

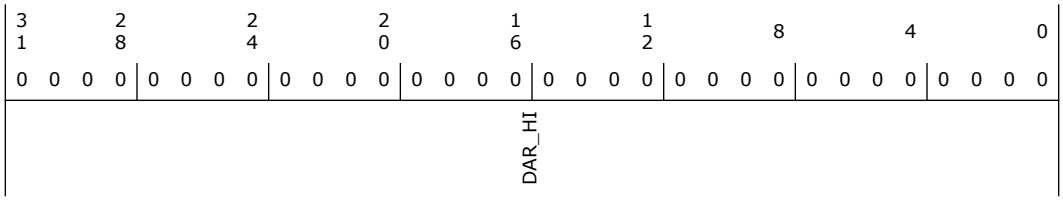
NOTE: DAR_HI0 is for DMA Channel 0. The same register definition, DAR_HI1, is available for Channel 1 at address 864h.
DAR_HI0 (CH0): offset 80Ch
DAR_HI1 (CH1): offset 864h
The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

Access Method

Type: MEM Register (Size: 32 bits)

Device: 30
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DAR_HI:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length > 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported.

12.4.5 Linked List Pointer Low (LLP_LO0)—Offset 810h

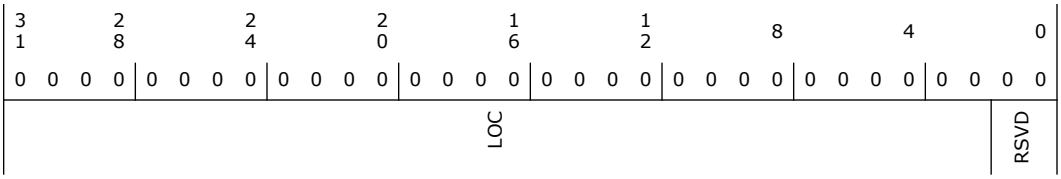
NOTE: LLP_LO0 is for DMA Channel 0. The same register definition, LLP_LO1, is available for Channel 1 at address 868h.
LLP_LO0 (CH0): offset 810h
LLP_LO1 (CH1): offset 868h
The register needs to be programmed to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0h RO	Reserved.

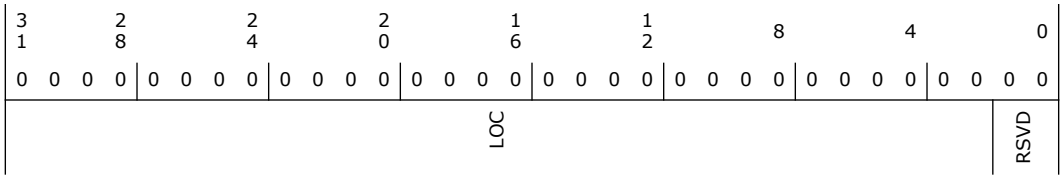
12.4.6 Linked List Pointer High (LLP_HI0)—Offset 814h

NOTE: LLP_HI0 is for DMA Channel 0. The same register definition, LLP_HI1, is available for Channel 1 at address 86Ch.
LLP_HI0 (CH0): offset 814h
LLP_LO1 (CH1): offset 86Ch
The register needs to be programmed to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled.

Access Method

Type: MEM Register (Size: 32 bits)
Device: 30
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**LOC:** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0h RO	Reserved.

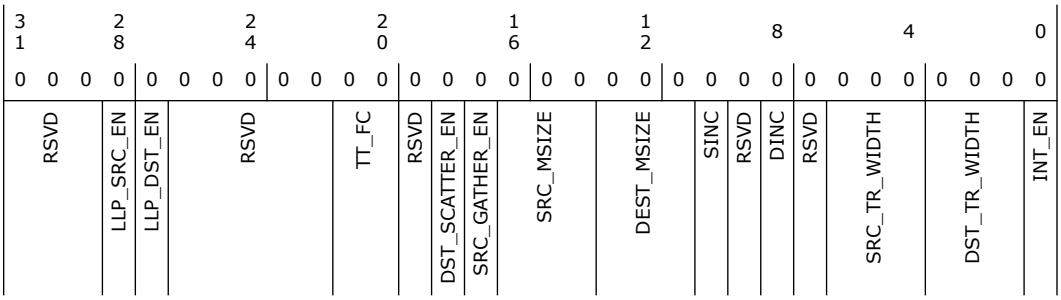
12.4.7 Control Register Low (CTL_LO0)—Offset 818h

NOTE: CTL_LO0 is for DMA Channel 0. The same register definition, CTL_LO1, is available for Channel 1 at address 870h.
LLP_HI0 (CH0): offset 818h
LLP_LO1 (CH1): offset 870h
This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled. If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Access Method

Type: MEM Register (Size: 32 bits)
Device: 30
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	Reserved.
28	0h RW	**LLP_SRC_EN:** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0h RW	**LLP_DST_EN:** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	0h RO	Reserved.
21:20	0h RW	**TT_FC:** The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	0h RO	Reserved.
18	0h RW	**DST_SCATTER_EN:** 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0h RW	**SRC_GATHER_EN:** 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0h RW	**SRC_MSIZE:** Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source.
13:11	0h RW	**DEST_MSIZE:** Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination.
10	0h RW	**SINC:** Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)
9	0h RO	Reserved.
8	0h RW	**DINC:** Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
6:4	0h RW	**SRC_TR_WIDTH:** BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width < 4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations)
3:1	0h RW	**DST_TR_WIDTH:** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width < 4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations)
0	0h RW	**INT_EN:** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

12.4.8 Control Register High (CTL_HI0)—Offset 81Ch

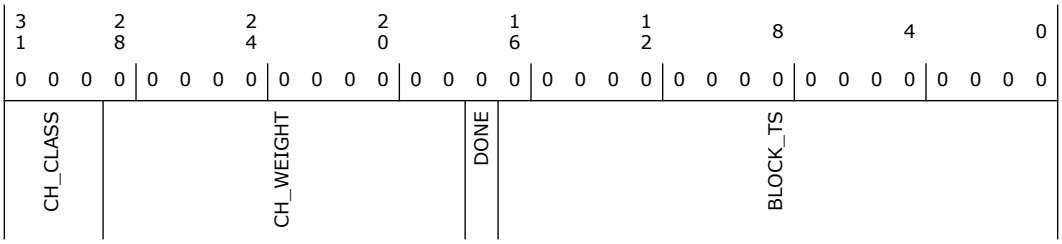
NOTE: CTL_HI0 is for DMA Channel 0. The same register definition, CTL_HI1, is available for Channel 1 at address 874h.
CTL_HI0 (CH0): offset 81Ch
CTL_HI1 (CH1): offset 874h
This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RW	**CH_CLASS:** A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior.

Bit Range	Default & Access	Field Name (ID): Description
28:18	0h RW	**CH_WEIGHT**
17	0h RW	**DONE:** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	0h RW	**BLOCK_TS:** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It doesn't mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

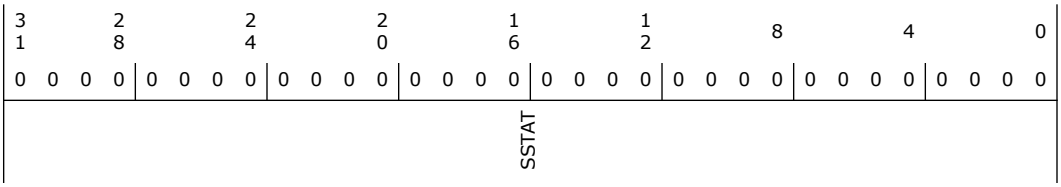
12.4.9 Source Status (SSTAT0)—Offset 820h

NOTE: SSTAT0 is for DMA Channel 0. The same register definition, SSTAT1, is available for Channel 1 at address 878h.
SSTAT0 (CH0): offset 820h
SSTAT1 (CH1): offset 878h
After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block.
Note : This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

Access Method

Type: MEM Register (Size: 32 bits)
Device: 30
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**SSTAT:** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

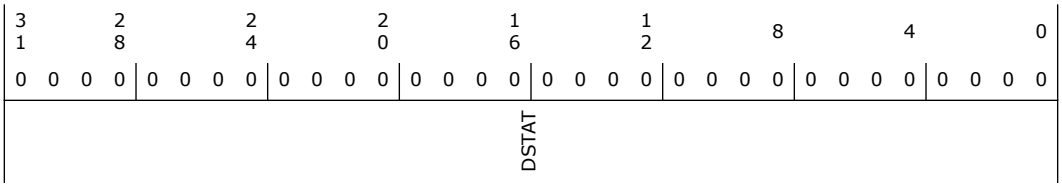
12.4.10 Destination Status (DSTAT0)—Offset 828h

NOTE: DSTAT0 is for DMA Channel 0. The same register definition, DSTAT1, is available for Channel 1 at address 880h.
DSTAT0 (CH0): offset 828h
DSTAT1 (CH1): offset 880h
After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI.
Note : This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

Access Method

Type: MEM Register (Size: 32 bits)
Device: 30
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DSTAT:** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

12.4.11 Source Status Address Low (SSTATAR_LO0)—Offset 830h

NOTE: SSTATAR_LO0 is for DMA Channel 0. The same register definition, SSTATAR_LO1, is available for Channel 1 at address 888h.
SSTATAR_LO0(CH0): offset 830h

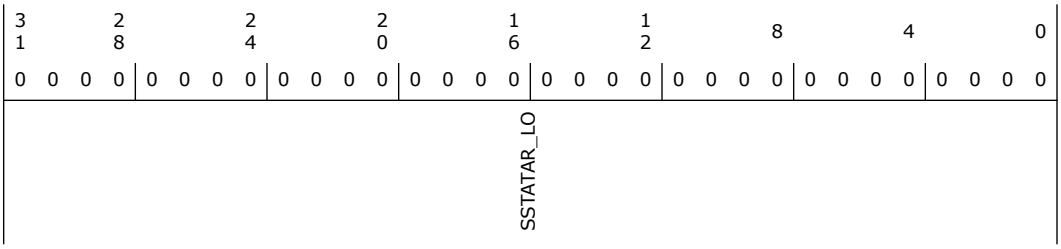
SSTATAR_LO1(CH1): offset 888h
After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**SSTATAR_LO:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

12.4.12 Source Status Address High (SSTATAR_HI0)—Offset 834h

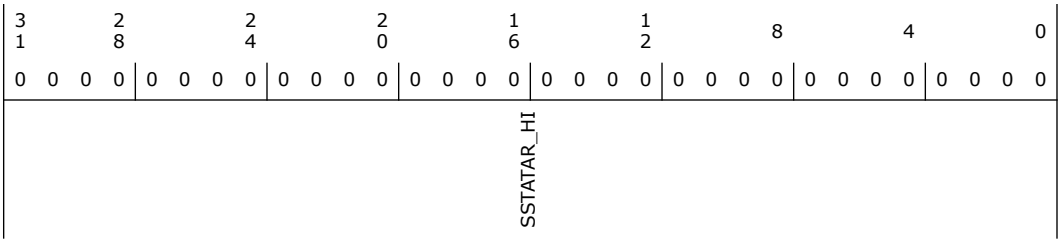
NOTE: SSTATAR_HI0 is for DMA Channel 0. The same register definition, SSTATAR_HI1, is available for Channel 1 at address 88Ch.
SSTATAR_HI0(CH0): offset 834h
SSTATAR_HI1(CH1): offset 88Ch
After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**SSTATAR_HI:** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

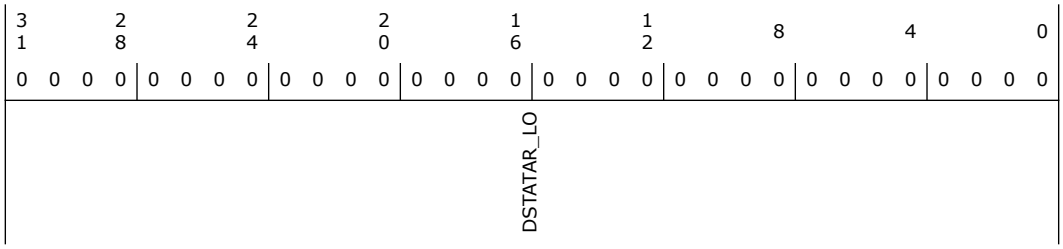
12.4.13 Destination Status Address Low (DSTATAR_LO0)—Offset 838h

NOTE: DSTATAR_LO0 is for DMA Channel 0. The same register definition, DSTATAR_LO1, is available for Channel 1 at address 890h.
DSTATAR_LO0(CH0): offset 838h
DSTATAR_LO1(CH1): offset 890h
After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Access Method

Type: MEM Register (Size: 32 bits)
Device: 30
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DSTATAR_LO:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

12.4.14 Destination Status Address High (DSTATAR_HI0)—Offset 83Ch

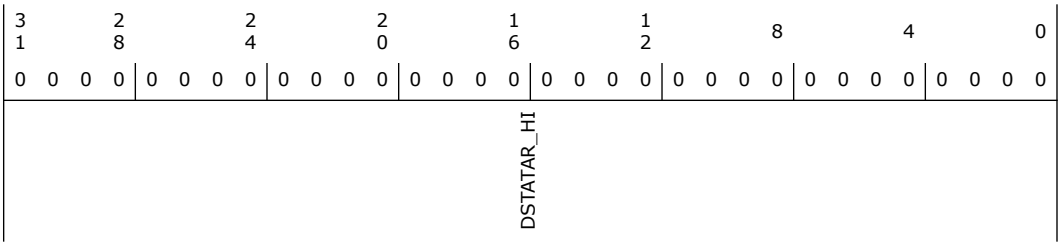
NOTE: DSTATAR_LO0 is for DMA Channel 0. The same register definition, DSTATAR_HI1, is available for Channel 1 at address 894h.
DSTATAR_HI0(CH0): offset 83Ch
DSTATAR_HI1(CH1): offset 894h
After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DSTATAR_HI:** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

12.4.15 DMA Transfer Configuration Low (CFG_LO0)—Offset 840h

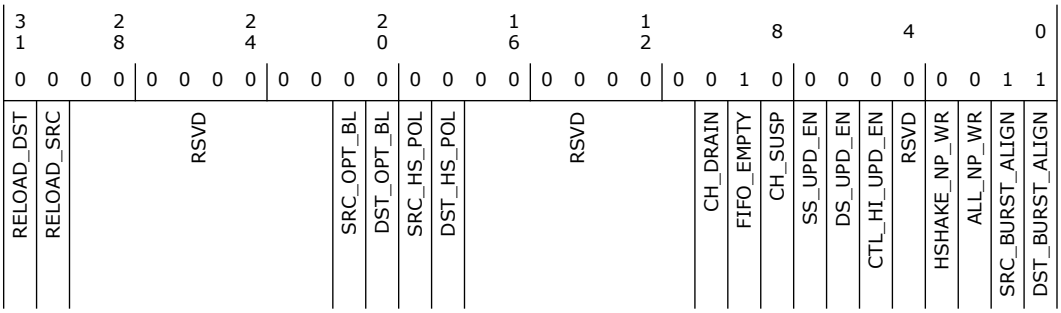
NOTE: CFG_LO0 is for DMA Channel 0. The same register definition, CFG_LO1, is available for Channel 1 at address 898h.
CFG_LO0(CH0): offset 840h
CFG_LO1(CH1): offset 898h
This register contains fields that configure the DMA transfer. The channel configuration register remains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 2

Default: 203h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
30	0h RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	0h RO	Reserved.
21	0h RW	**SRC_OPT_BL:** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 <= BL <= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled
20	0h RW	**DST_OPT_BL:** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 <= BL <= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled
19	0h RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0h RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17:11	0h RO	Reserved.
10	0h RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND is asserted
9	1h RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty
8	0h RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0h RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
6	0h RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0h RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0h RO	Reserved.
3	0h RW	**HSHAKE_NP_WR:** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted) This bit must be set to 1 for proper operation

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**ALL_NP_WR:** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	1h RW	**SRC_BURST_ALIGN:** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary
0	1h RW	**DST_BURST_ALIGN:** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary.

12.4.16 DMA Transfer Configuration High (CFG_HI0)—Offset 844h

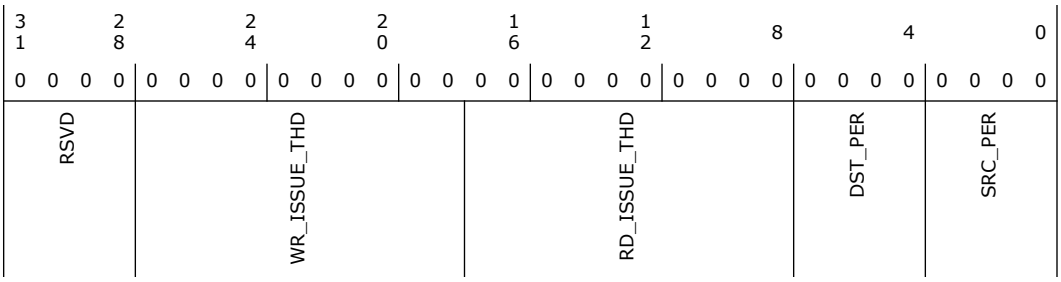
NOTE: CFG_HI0 is for DMA Channel 0. The same register definition, CFG_HI1, is available for Channel 1 at address 89Ch.
CFG_HI0(CH0): offset 844h
CFG_HI1(CH1): offset 89Ch
This register contains fields that configure the DMA transfer. The channel configuration register remains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	Reserved.
27:18	0h RW	**WR_ISSUE_THD:** Write Issue Threshold. Used to relax the issue criterion for Writes. Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.

Bit Range	Default & Access	Field Name (ID): Description
17:8	0h RW	**RD_ISSUE_THD:** Read Issue Threshold. Used to relax the issue criterion for Reads. Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.
7:4	0h RW	**DST_PER:** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface.
3:0	0h RW	**SRC_PER:** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface.

12.4.17 Source Gather (SGR0)—Offset 848h

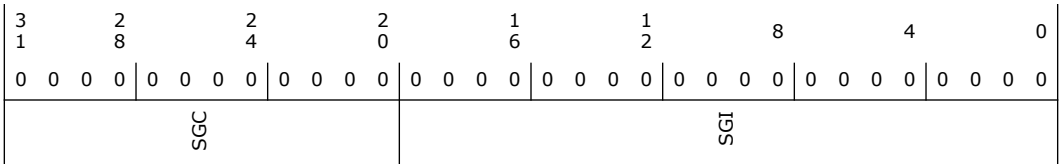
NOTE: SGR0 is for DMA Channel 0. The same register definition, SGR1, is available for Channel 1 at address 8A0h.
SGR0(CH0): offset 848h
SGR1(CH1): offset 8A0h
The Source Gather register contains two fields: Source gather count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gather interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

Access Method

Type: MEM Register (Size: 32 bits)

Device: 30
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**SGC**
19:0	0h RW	**SGI**

12.4.18 Destination Scatter (DSR0)—Offset 850h

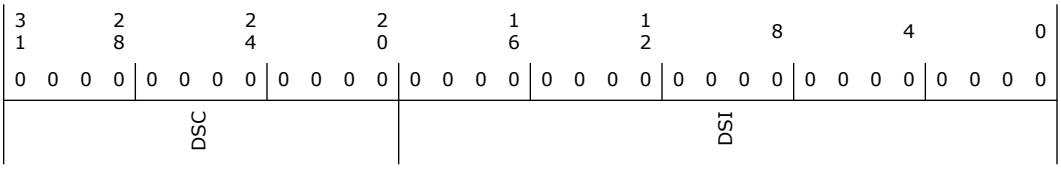
NOTE: DSR0 is for DMA Channel 0. The same register definition, DSR1, is available for Channel 1 at address 8A8h.
DSR0(CH0): offset 850h
DSR1(CH1): offset 8A8h
The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC) . Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI) . Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**DSC**
19:0	0h RW	**DSI**

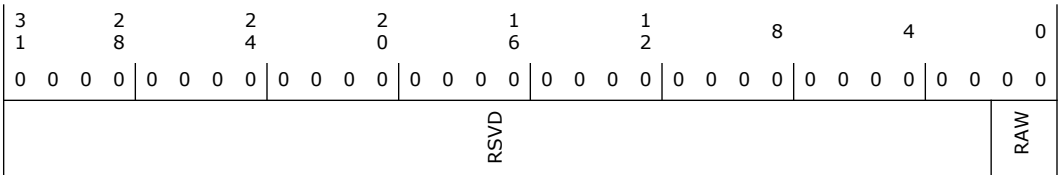
12.4.19 Raw Interrupt Status (RawTfr)—Offset AC0h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**RAW:** Bit0 for channel 0 and bit 1 for channel 1.

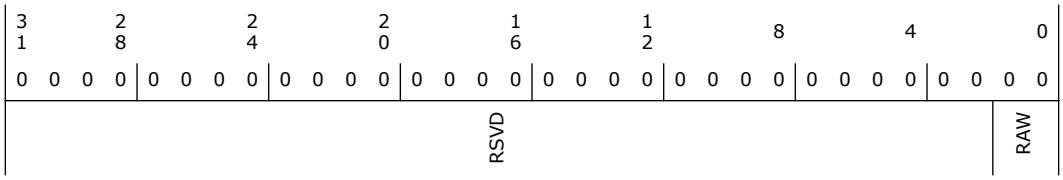
12.4.20 Raw Status for Block Interrupts (RawBlock)—Offset AC8h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**RAW:** Bit 0 for channel 0 and bit 1 for channel 1.

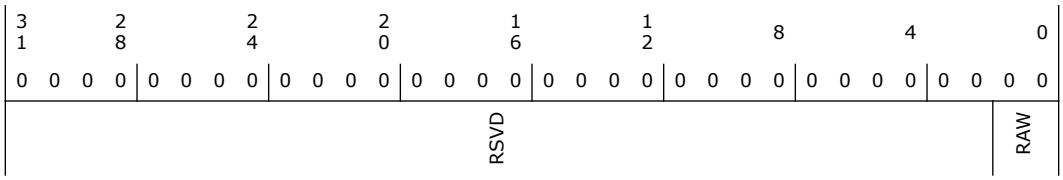
12.4.21 Raw Status for Source Transaction Interrupts (RawSrcTran)—Offset AD0h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**RAW:** Bit 0 for channel 0 and bit 1 for channel 1.

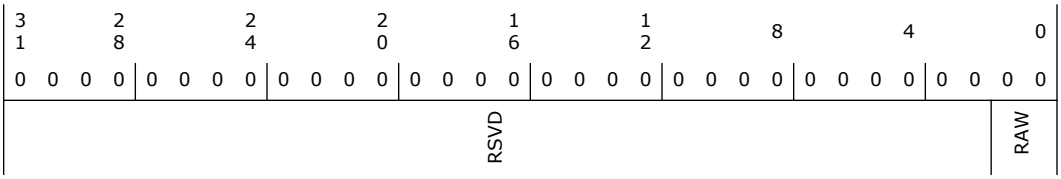
12.4.22 Raw Status for Destination Transaction Interrupts (RawDstTran)—Offset AD8h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**RAW:** Bit 0 for channel 0 and bit 1 for channel 1.

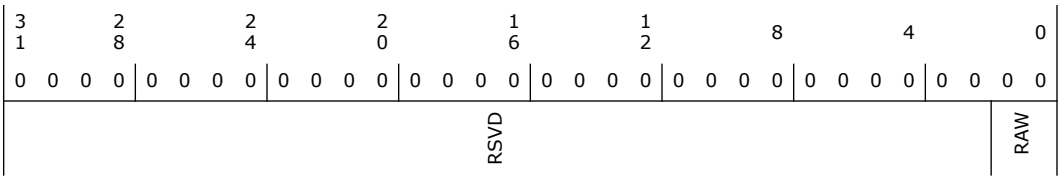
12.4.23 Raw Status for Error Interrupts (RawErr)—Offset AE0h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**RAW:** Bit 0 for channel 0 and bit 1 for channel 1.

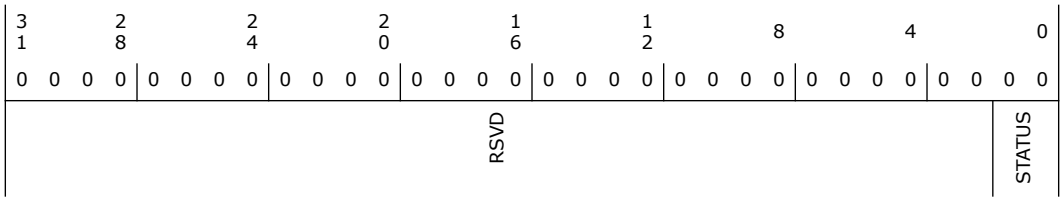
12.4.24 Interrupt Status (StatusTfr)—Offset AE8h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**STATUS:** Bit 0 for channel 0 and bit 1 for channel 1.

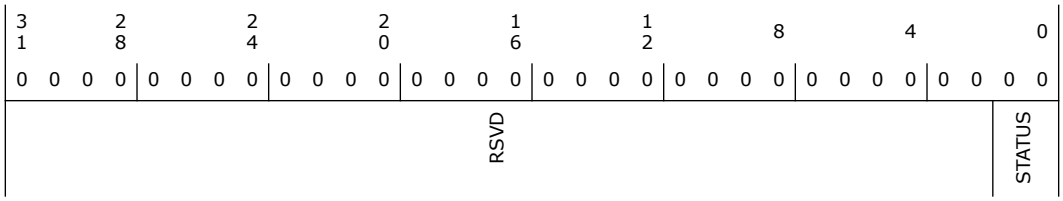
12.4.25 Status for Block Interrupts (StatusBlock)—Offset AF0h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**STATUS:** Bit 0 for channel 0 and bit 1 for channel 1.

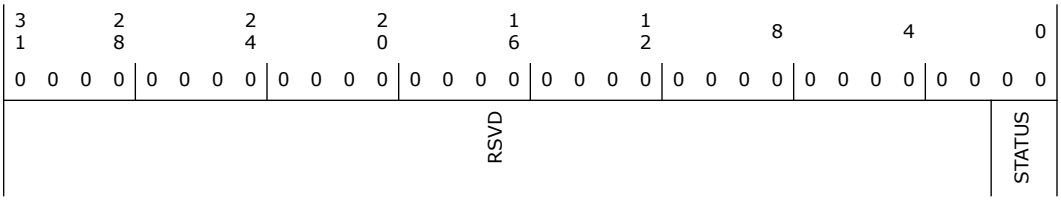
12.4.26 Status for Source Transaction Interrupts (StatusSrcTran)—Offset AF8h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**STATUS:** Bit 0 is for channel 0 and bit 1 is for channel 1.

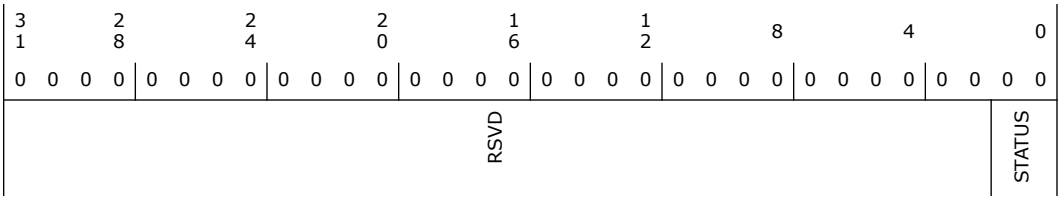
12.4.27 Status for Destination Transaction Interrupts (StatusDstTran)—Offset B00h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**STATUS:** Bit 0 is for channel 0 and bit 1 is for channel 1.

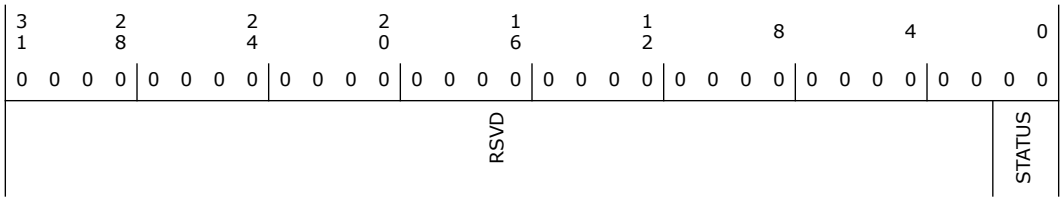
12.4.28 Status for Error Interrupts (StatusErr)—Offset B08h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**STATUS:** Bit 0 is for channel 0 and bit 1 is for channel 1.

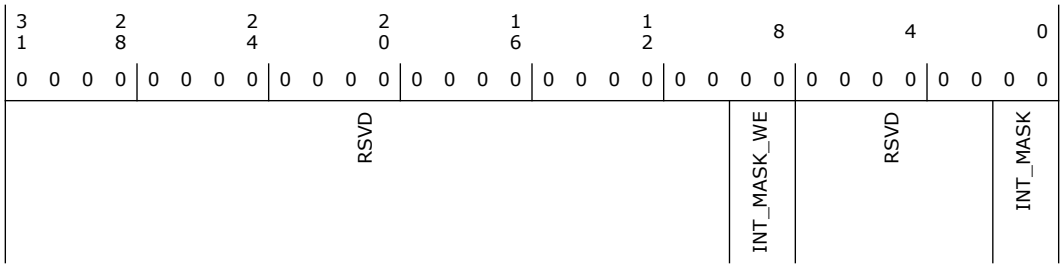
12.4.29 Mask for Transfer Interrupts (MaskTfr)—Offset B10h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:8	0h WO	**INT_MASK_WE:** 0 = write disabled 1 = write enabled
7:2	0h RO	Reserved.
1:0	0h RW	**INT_MASK:** 0-mask 1-unmask

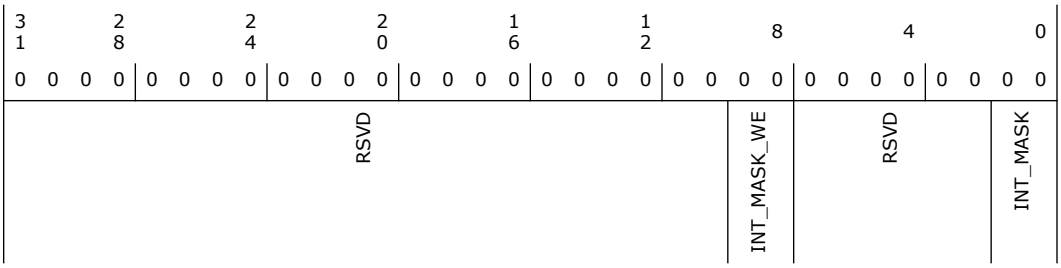
12.4.30 Mask for Block Interrupts (MaskBlock)—Offset B18h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:8	0h WO	**INT_MASK_WE:** 0 = write disabled 1 = write enabled
7:2	0h RO	Reserved.
1:0	0h RW	**INT_MASK:** 0-mask 1-unmask

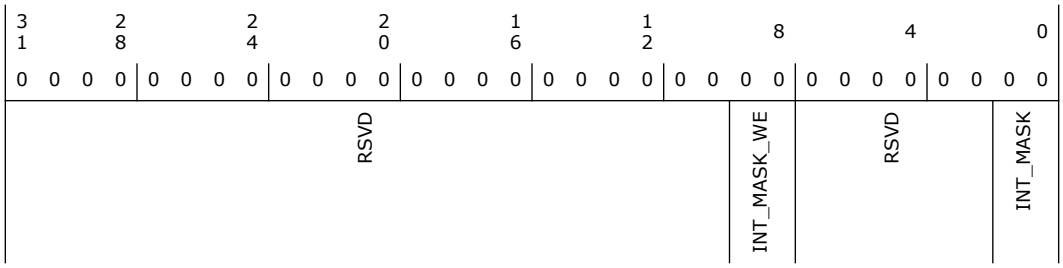
12.4.31 Mask for Source Transaction Interrupts (MaskSrcTran)—Offset B20h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:8	0h WO	**INT_MASK_WE:** 0 = write disabled 1 = write enabled
7:2	0h RO	Reserved.
1:0	0h RW	**INT_MASK:** 0-mask 1-unmask

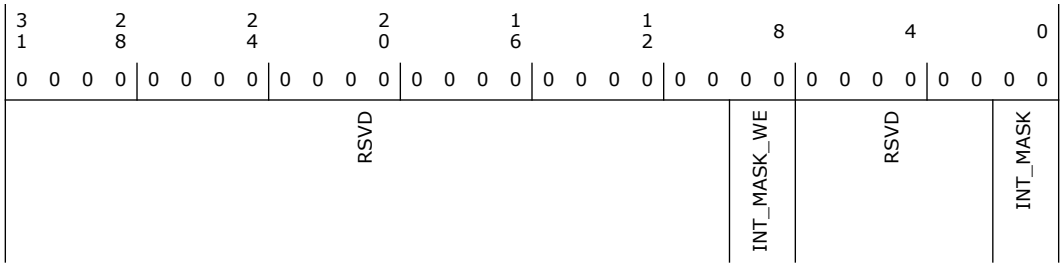
12.4.32 Mask for Destination Transaction Interrupts (MaskDstTran)—Offset B28h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:8	0h WO	**INT_MASK_WE:** 0 = write disabled 1 = write enabled
7:2	0h RO	Reserved.
1:0	0h RW	**INT_MASK:** 0-mask 1-unmask

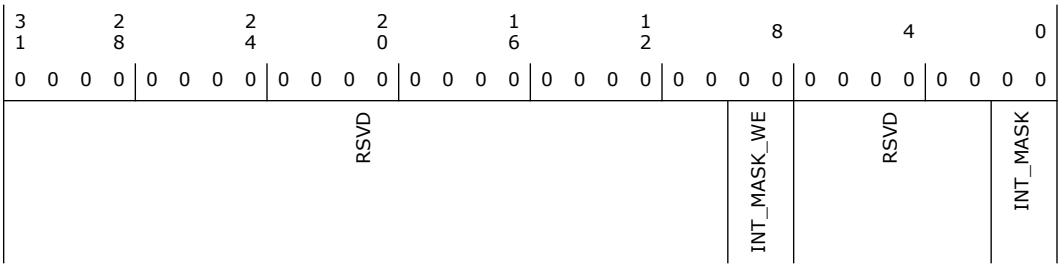
12.4.33 Mask for Error Interrupts (MaskErr)—Offset B30h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:8	0h WO	**INT_MASK_WE:** 0 = write disabled 1 = write enabled
7:2	0h RO	Reserved.
1:0	0h RW	**INT_MASK:** 0-mask 1-unmask

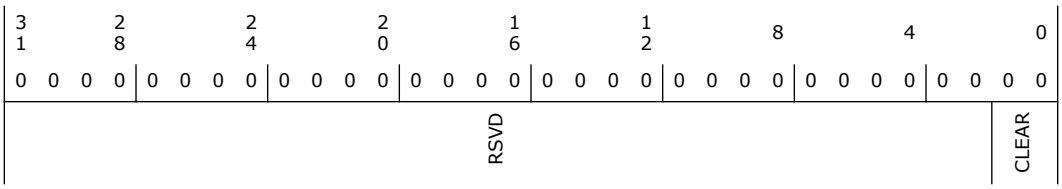
12.4.34 Clear for Transfer Interrupts (ClearTfr)—Offset B38h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h WO	**CLEAR:** 0 = no effect 1 = clear interrupt

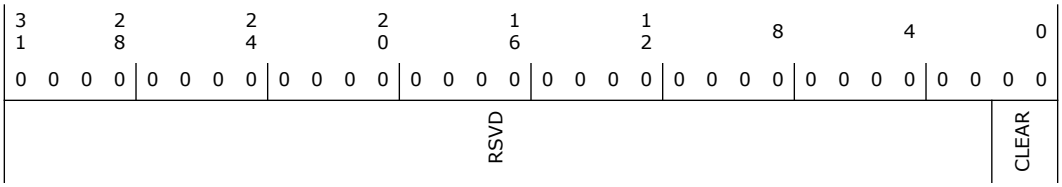
12.4.35 Clear for Block Interrupts (ClearBlock)—Offset B40h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h WO	**CLEAR:** 0 = no effect 1 = clear interrupt

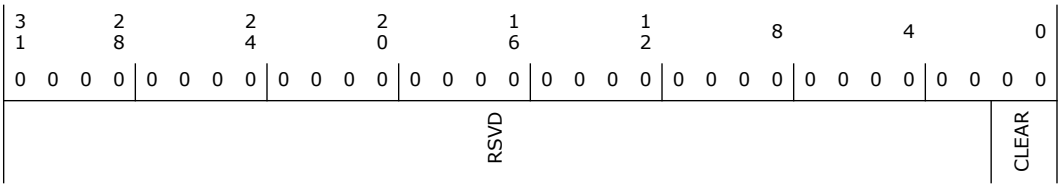
12.4.36 Clear for Source Transaction Interrupts (ClearSrcTran)—Offset B48h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h WO	**CLEAR:** 0 = no effect 1 = clear interrupt

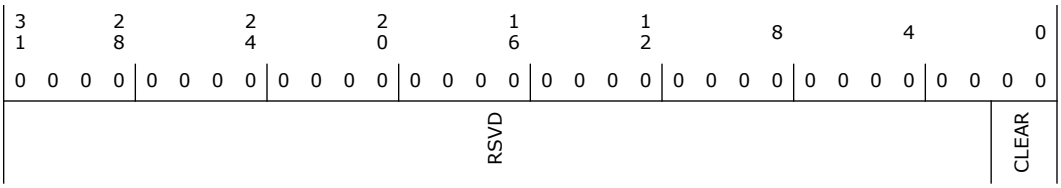
12.4.37 Clear for Destination Transaction Interrupts (ClearDstTran)—Offset B50h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h WO	**CLEAR:** 0 = no effect 1 = clear interrupt

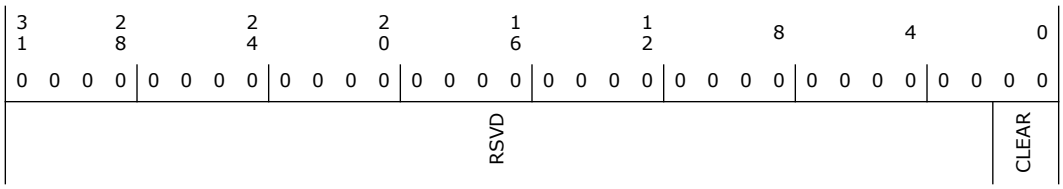
12.4.38 Clear for Error Interrupts (ClearErr)—Offset B58h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h WO	**CLEAR:** 0 = no effect 1 = clear interrupt

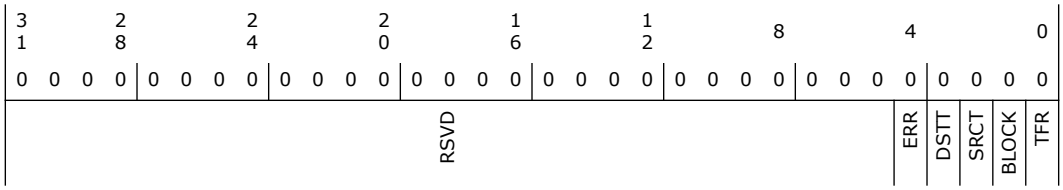
12.4.39 Combined Status register (StatusInt)—Offset B60h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4	0h RO	**ERR:** OR of the contents of StatusErr register.
3	0h RO	**DSTT:** OR of the contents of StatusDst register.
2	0h RO	**SRCT:** OR of the contents of StatusSrcTran register
1	0h RO	**BLOCK:** OR of the contents of StatusBlock register.
0	0h RO	**TFR:** OR of the contents of StatusTfr register.

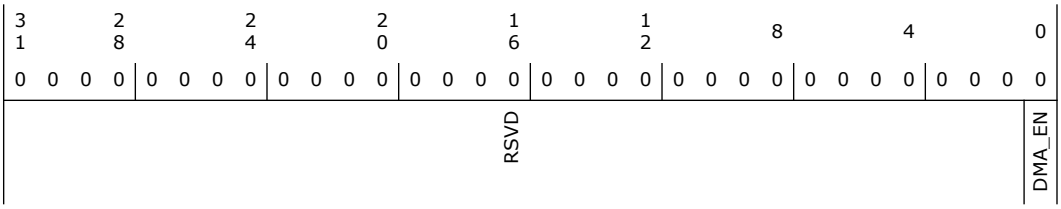
12.4.40 DMA Configuration (DmaCfgReg)—Offset B98h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RW	**DMA_EN:** 0 = DMA Disabled 1 = DMA Enabled

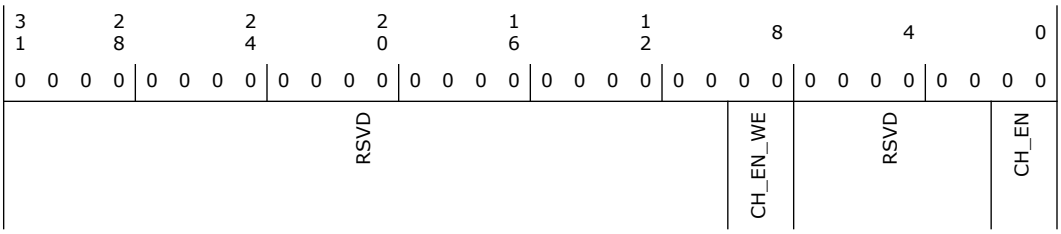
12.4.41 DMA Channel Enable (ChEnReg)—Offset BA0h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
9:8	0h WO	**CH_EN_WE**
7:2	0h RO	Reserved.
1:0	0h RW	**CH_EN:** Enables/Disables the channel. Setting this bit enables a channel, clearing this bit disables the channel. 0 = Disable the Channel 1 = Enable the Channel The ChEnReg.CH_EN bit is automatically cleared by hardware to disable the channel after the last OCP transfer of the DMA transfer to the destination has completed. Software can therefore poll this bit to determine when this channel is free for a new DMA transfer.

12.5 Generic SPI (GSPI) PCR Registers Summary

These registers are within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID + Register Offset).

Table 12-5. Summary of GSPI PCR Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
224h	227h	PCI Configuration Control (PCICFGCTRL) for GSPI0	00000100h
228h	22Bh	PCI Configuration Control (PCICFGCTRL) for GSPI1	00000100h

12.5.1 PCI Configuration Control (PCICFGCTRL)

Default: 00000100h

NOTE: This register applies to the following GSPI controllers as follows:

GSPI0: at offset 224h
GSPI1: at offset 228h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
27:20	0h RW	**PCI IRQ:** IRQ number to be sent in the message with data field for Assert_IRQ and Deassert_IRQ message, Note: Bridge does not wire-or the interrupts from different functions before sending them even if they are tied to the same IPIN value of the same IRQ value by the BIOS. It is the responsibility of the interrupt controller to ensure that interrupts are wire-ored. Note: each PCI device (B:D:F) for Intel Serial IO interfaces (i.e.I2C, UART, GSPI) is limit to 4 functions max per PCI device, allowing each function to map to dedicated INT[A-D] and thus a unique IRQ number. Sharing IRQs is not allowed across any Serial IO interfaces B:D:F. All Serial IO interface B:D:F must have a unique IRQ number.
19:12	0h RW	**ACPI IRQ:** IRQ number to be sent in the message with data field for Assert_IRQ and Deassert_IRQ message, Note: Bridge does not wire-or the interrupts from different functions before sending them even if they are tied to the same IPIN value of the same IRQ value by the BIOS. It is the responsibility of the interrupt controller to ensure that interrupts are wire-ored. Note: each PCI device (B:D:F) for Intel Serial IO interfaces (i.e.I2C, UART, GSPI) is limit to 4 functions max per PCI device, allowing each function to map to dedicated INT[A-D] and thus a unique IRQ number. Sharing IRQs is not allowed across any Serial IO interfaces B:D:F. All Serial IO interface B:D:F must have a unique IRQ number.
11:8	0h RW	**Interrupt Pin:** This register indicates the values to be used for Global Interrupts. This value will also be reflected in the PCOS register IPIN value. 0 = No interrupt Pin 1 = INTA 2 = INTB 3 = INTC 4 = INTD 5 - FF: Reserved
7	0h RW	**BAR1 Disable:** BAR1 register in the PCOS space will become Read Only when this bit is set,
6:2	0h RW	**PME Support:** The value in this register will be XOR with the value in the PME_support strap and reflected in the PME_support register in the PCI configuration space. This register can be used as a mechanism to change the value of the PME_Status PCI config register field.
1	0h RW	**ACPI_INTR_EN:** When set, ACPI IRQ number field (bits 19:12) will be used for IRQ messages. When 0, PCI IRQ number field (bits 27:20) will be used for IRQ message.
0	0h RW	**PCI_CFG_DIS:** When set, PCI configuration accesses return UR response. When 0, PCI configuration accesses are supported.

§ §

13 eMMC* Interface (D30:F4)

13.1 eMMC* PCI Configuration Registers Summary

Table 13-1. Summary of eMMC* PCI Configuration Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	Device & Vendor ID (VID_DID)—Offset 0h	9D2B8086h
4h	7h	PCI Status & Command (STATUSCOMMAND)—Offset 4h	100000h
8h	Bh	Rev ID & Class Code (REVCLASSCODE)—Offset 8h	80501XXh
Ch	Fh	Carche Line & Latency & Header Type & BIST (CLLATHEADERBIST)—Offset Ch	800000h
10h	13h	Base Address Low (BAR0)—Offset 10h	4h
14h	17h	Base Address Register high (BAR0_HIGH)—Offset 14h	0h
18h	1Bh	Base Address Register1 (BAR1)—Offset 18h	4h
1Ch	1Fh	(BAR1_HIGH)—Offset 1Ch	0h
2Ch	2Fh	Subsystem Vendor ID (SUBSYSTEMID)—Offset 2Ch	0h
30h	33h	(EXPANSION_ROM_BASEADDR)—Offset 30h	0h
34h	37h	Capabilities Pointer (CAPABILITYPTR)—Offset 34h	80h
3Ch	3Fh	(INTERRUPTREG)—Offset 3Ch	100h
80h	83h	Power Management Capability ID Register (POWERCAPID)—Offset 80h	39001h
84h	87h	Power Management Control and Status Register (PMECTRLSTATUS)—Offset 84h	8h
90h	93h	(PCIDEVIDLE_CAP_RECORD)—Offset 90h	F0140009h
94h	97h	(DEVID_VEND_SPECIFIC_REG)—Offset 94h	1400010h
98h	9Bh	SW LTR update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG)—Offset 98h	8041h
9Ch	9Fh	Device IDLE Pointer Register (DEVICE_IDLE_POINTER_REG)—Offset 9Ch	81C1h
A0h	A3h	DOI3 Max Power & PG Config (D0I3_MAX_POW_LAT_PG_CONFIG)—Offset A0h	90800h
B0h	B3h	General Purpose PCI RW Register1 (GEN_REGRW1)—Offset B0h	0h
B4h	B7h	General Purpose PCI RW Register2 (GEN_REGRW2)—Offset B4h	0h
B8h	BBh	General Purpose PCI RW Register3 (GEN_REGRW3)—Offset B8h	0h
BCh	BFh	General Purpose PCI RW Register4 (GEN_REGRW4)—Offset BCh	0h
C0h	C3h	General Input Register (GEN_INPUT_REG)—Offset C0h	0h

13.1.1 Device & Vendor ID (VID_DID)—Offset 0h

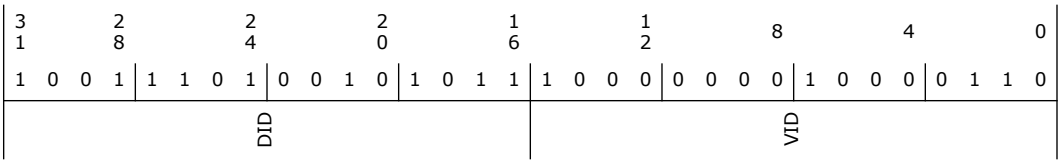
DEVICEVENDORID - Device ID and Vendor ID Register

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 4

Default: 9D2B8086h



Bit Range	Default & Access	Field Name (ID): Description
31:16	9D2Bh RO	**Device ID (DID):** Identifies the device.
15:0	8086h RO	**Vendor ID (VID):** Intel default value is 8086h

13.1.2 PCI Status & Command (STATUSCOMMAND)—Offset 4h

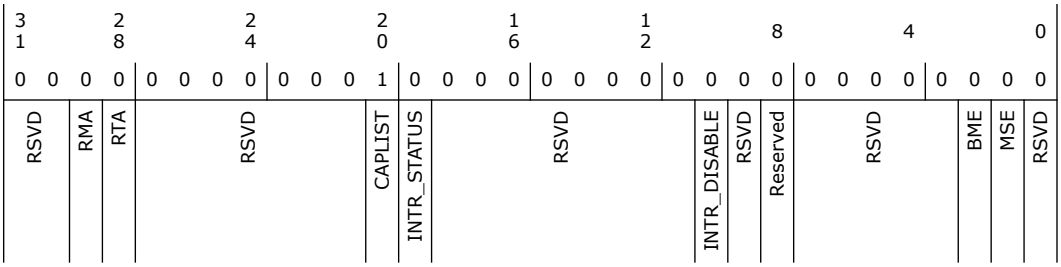
STATUSCOMMAND- Status and Command

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 4

Default: 100000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29	0h RW/1C	**Received Master Abort (RMA):** The software writes a 1 to this bit to clear it.
28	0h RW/1C	**Received Target Abort (RTA):** The software writes a 1 to this bit to clear it.
27:21	0h RO	Reserved.
20	1h RO	**Capabilities List (CAPLIST):** Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at the configuration offset 34h.
19	0h RO	**Interrupt Status (INTR_STATUS):** This bit reflects state of interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, is the device/function interrupt message sent.

Bit Range	Default & Access	Field Name (ID): Description
18:11	0h RO	Reserved.
10	0h RW	**Interrupt Disable (INTR_DISABLE):** Setting this bit disables INTx assertion.
9	0h RO	Reserved.
8	0h RW	**Reserved**
7:3	0h RO	Reserved.
2	0h RW	**Bus Master Enable (BME):** 0 = the Bridge does not generate any new upstream transaction on IOSF as a master. Reset value of this bit is 0.
1	0h RW	**Memory Space Enable (MSE):** MSE is part of the Type PCI configuration space each device has. When disabled no downstream traffic from the bridge is available.
0	0h RO	Reserved.

13.1.3 Rev ID & Class Code (REVCLASSCODE)—Offset 8h

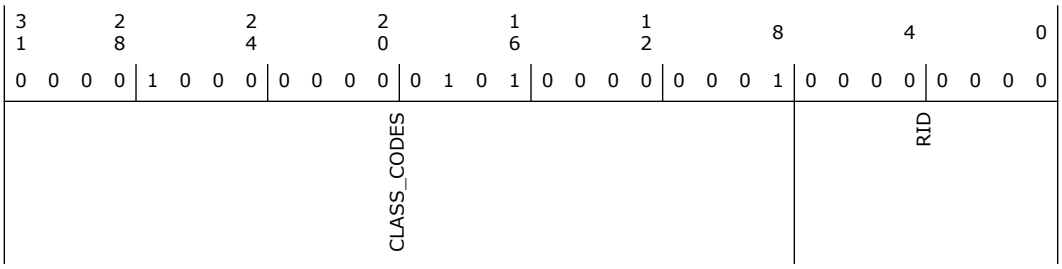
REVCLASSCODE - Revision ID and Class Code

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 4

Default: 80501xxh



Bit Range	Default & Access	Field Name (ID): Description
31:8	80501h RO	**Class Code (CLASS_CODES):** The Class Code register is read-only and is used to identify the generic function of the device, and in some cases, a specific register-level programming interface. The register is broken into 3 Byte-size fields. - The upper Byte (at offset 0Bh) is a base class code that broadly classifies the type of function the device performs. - The middle Byte (at offset 0Ah) is a sub-class code that identifies more specifically the function of the device. - The lower Byte (at offset 09h) identifies a specific register-level programming interface (if any) so that device independent software can interact with the device. This register is tied to a strap at the top level.
7:0	-- RO	**Rev ID (RID):** Revision ID identifies the revision of particular PCI device. See the Device and Version ID Table in Volume 1 for the default value.

13.1.4 Carche Line & Latency & Header Type & BIST (CLLATHEADERBIST)—Offset Ch

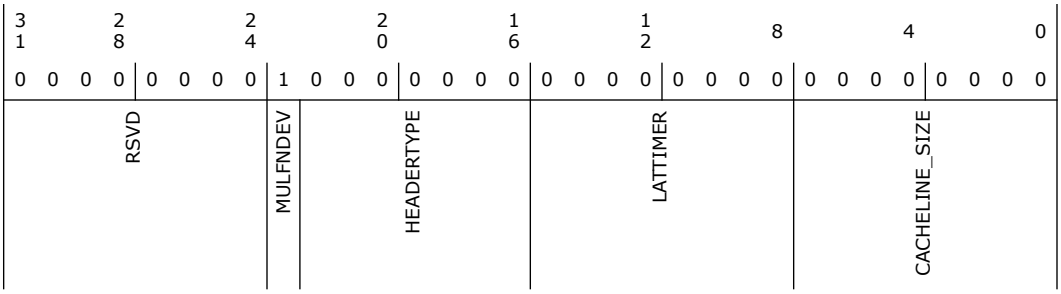
CLLATHEADERBIST - Cache Line Latency Header and BIST

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 4

Default: 800000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	1h RO	**Multi-Function Device (MULFNDEV):** This bit is 0 or 1 depending upon the value assigned o the top level strap
22:16	0h RO	**Header Type (HEADERTYPE):** Implements Type 0 Configuration header.
15:8	0h RO	**Latency Timer (LATTIMER):** This register is implemented as R/W with default as 0.
7:0	0h RW	**Cacheline Size (CACHELINE_SIZE):** This register is implemented as R/W with default as 0.

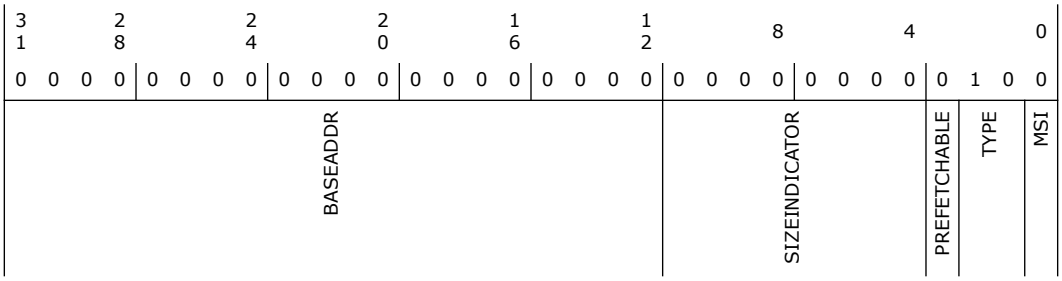
13.1.5 Base Address Low (BAR0)—Offset 10h

BAR -Base Address Register

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 30 **Function:** 4

Default: 4h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW	**BARL (BASEADDR):** Base address of the memory space.
11:4	0h RO	**Size Indicator (SIZEINDICATOR):** Size Indicator Read Only. The size of this register depends on the size of the memory space.
3	0h RO	**Prefetchable (PREFETCHABLE):** Indicates that this BAR is not prefetchable.
2:1	2h RO	**TYPE:** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range. If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range.
0	0h RO	**Memory Space Indicator (MSI):** 0 indicates this BAR is present in the memory space.

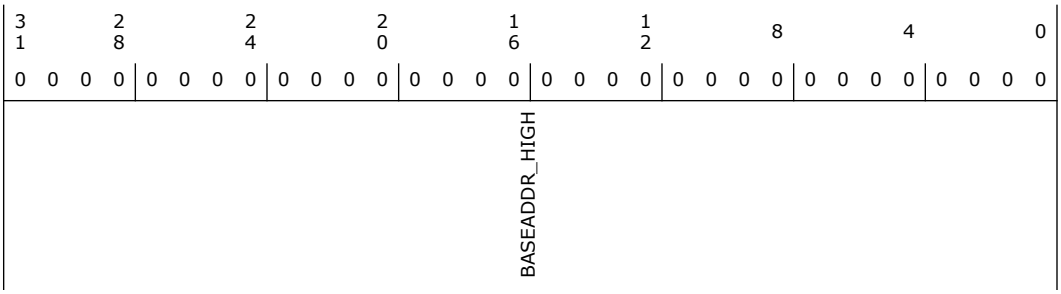
13.1.6 Base Address Register high (BAR0_HIGH)—Offset 14h

This register is present on if BAR_64_EN is set as 1.
This register enables 64-bit BARs.
If BAR_64_EN is 0, then this register is RO.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 30 **Function:** 4

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**BARH (BASEADDR_HIGH):** Base address of the OCP fabric memory space.

13.1.7 Base Address Register1 (BAR1)—Offset 18h

Memory accesses to BAR1 region are aliased to the PCI configuration space. The BAR1 region is always 4K.

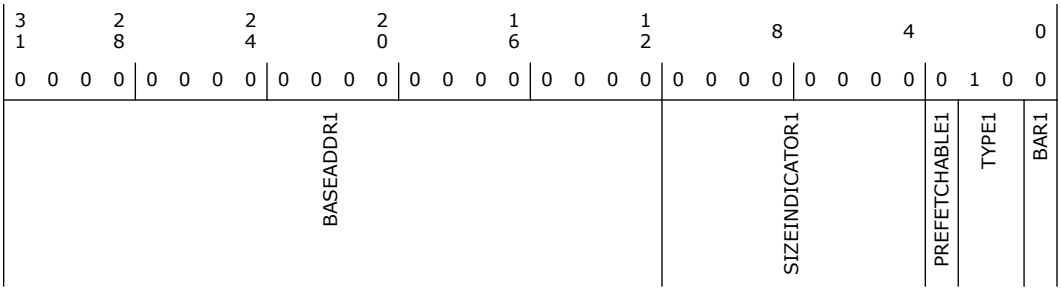
Access Method

Type: CFG Register (Size: 32 bits)

Device: 30

Function: 4

Default: 4h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW	**Base Address Register1 (BASEADDR1):** This field is present if BAR1 is enabled through private configuration space.
11:4	0h RO	**SIZEBAR1 (SIZEINDICATOR1):** Always is 0 as minimum size is 4K
3	0h RO	**Prefetchable (PREFETCHABLE1):** Indicates that this BAR is not prefetchable.
2:1	2h RO	**TYPE (TYPE1):** Always 0 as minimum size is 4K
0	0h RO	**Base Address Register1 (BAR1):** This field is present if BAR1 is enabled through private configuration space.

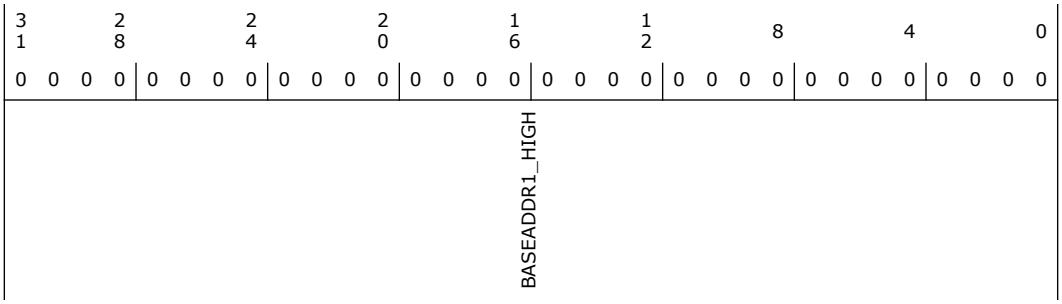
13.1.8 (BAR1_HIGH)—Offset 1Ch

This register is present on if BAR_64_EN is set as 1.
This register enables 64bit BARs.
If BAR_64_EN is 0 then this register is RO.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 30 **Function:** 4

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**BASEADDR1_HIGH:** Base address of the OCP fabric memory space.

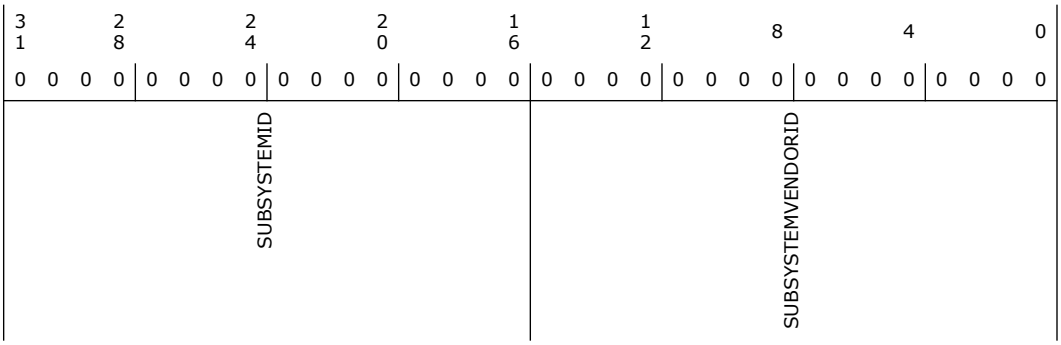
13.1.9 Subsystem Vendor ID (SUBSYSTEMID)—Offset 2Ch

This register must be implemented for any function that can be instantiated more than once in a given system. The SVID register, in combination with the Subsystem ID register, enables the operating environment to distinguish one subsystem from the other.
This register is a Read Write Once register

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 30 **Function:** 4

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW/O	**SUBSYSTEMID**
15:0	0h RW/O	**SUBSYSTEMVENDORID**

13.1.10 (EXPANSION_ROM_BASEADDR)—Offset 30h

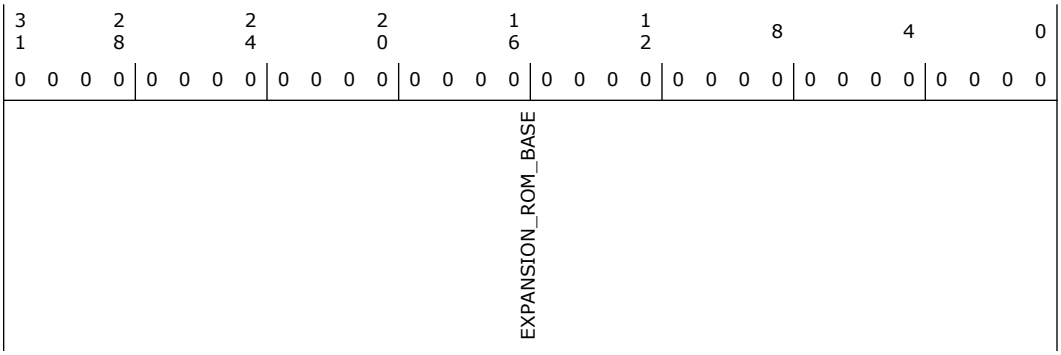
EXPANSION ROM base address

Access Method

Type: CFG Register (Size: 32 bits)

Device: 30
Function: 4

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**EXPANSION_ROM_BASE:** Value of all zeros indicates no support for Expansion ROM.

13.1.11 Capabilities Pointer (CAPABILITYPTR)—Offset 34h

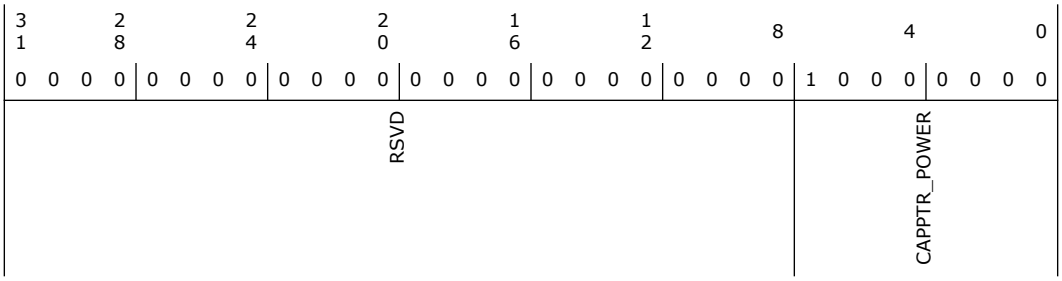
This capability points to the PM Capability (0x80) structure.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 4

Default: 80h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	80h RO	**CAPPTR_POWER**

13.1.12 (INTERRUPTREG)—Offset 3Ch

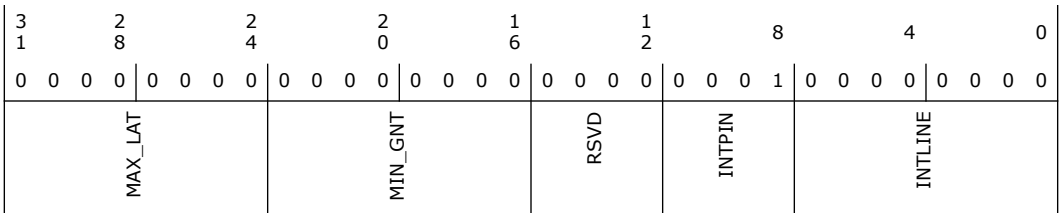
INTERRUPTREG - Interrupt Register

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 4

Default: 100h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Maximum Latency (MAX_LAT):** Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	0h RO	**Min Latency (MIN_GNT):** Value of 0 indicates device has no major requirements for the settings of latency timers.

Bit Range	Default & Access	Field Name (ID): Description
15:12	0h RO	Reserved.
11:8	1h RO	**Interrupt Pin (INTPIN):** Interrupt Pin Value in this register is reflected from the IPIN value in the private configuration space. For a single function device, this ideally is INTA.
7:0	0h RW	**Interrupt Line (INTLINE):** It is used to communicate to software, the interrupt line to which the interrupt pin is connected.

13.1.13 Power Management Capability ID Register (POWERCAPID)—Offset 80h

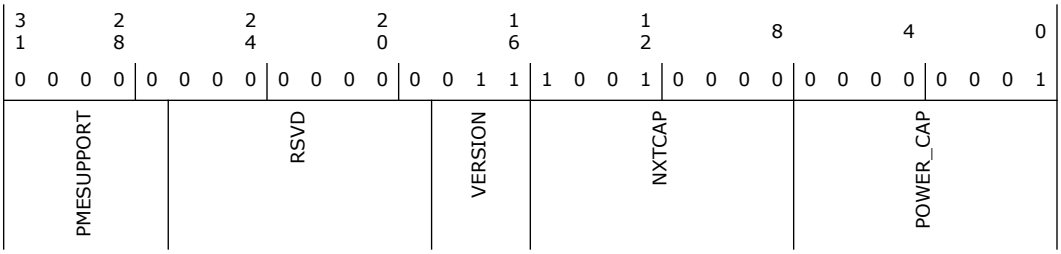
POWERCAPID - PowerManagement Capability ID

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 4

Default: 39001h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**PME_Support (PMESUPPORT):** This 5-bit field indicates the power states in which the function can assert the PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal in that power state. bit 27 = 1: PME# can be asserted from D0 bit28 = 1: PME# can be asserted from D1. bit 29 = 1: PME# can be asserted from D2. bit30 = 1:PME# can be asserted from D3hot bit 31 = 1:PME# can be asserted from D3cold.
26:19	0h RO	Reserved.
18:16	3h RO	**Version (VERSION):** Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	90h RO	**Next Capability (NXTCAP):** Points to the next capability structure. This points to NULL if either ENABLE_PCI_IDLE_CAP is 0 or if Disable PCI Device Idle capability bit is set as 1 in the private space. Else this points to PCI Device Idle capability structure at offset 90h
7:0	1h RO	**Power Management Capability (POWER_CAP):** Indicates this is power management capability.

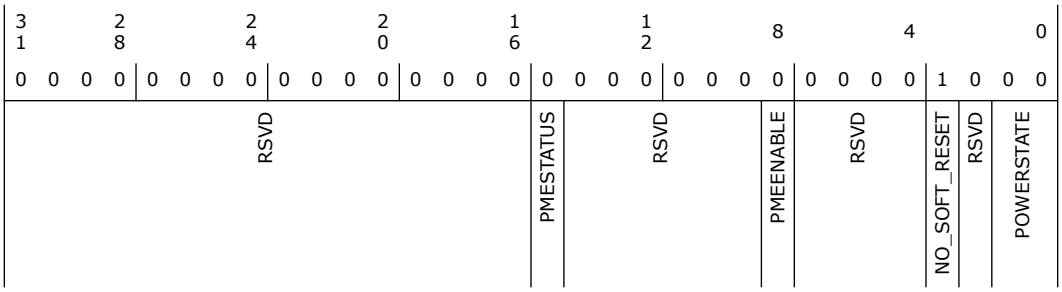
13.1.14 Power Management Control and Status Register (PMECTRLSTATUS)—Offset 84h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 4

Default: 8h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	0h RW/1C	**PME Status (PMESTATUS):** 0: Software clears the bit by writing a 1 to it. 1: This bit is set when the PME# signal is asserted independent of the state of the PME Enable bit (bit 8 in this register)
14:9	0h RO	Reserved.
8	0h RW	**PME Enable (PMEENABLE):** 1: Enables the function to assert PME#. 0: PME# message on Sideband is disabled.
7:4	0h RO	Reserved.
3	1h RO	**NO_SOFT_RESET:** This bit indicates that devices transitioning from D3hot to D0 because of Powerstate commands do not perform an internal reset. Configuration Context is preserved.
2	0h RO	Reserved.
1:0	0h RW	**Power State (POWERSTATE):** This field is used both to determine the current power state and to set a new power state. The values are: 00 D0 state 11 D3HOT state

13.1.15 (PCIDEVIDLE_CAP_RECORD)—Offset 90h

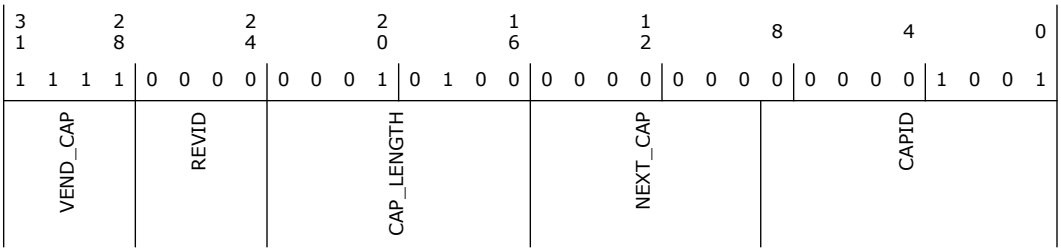
PCI DEVICE IDLE CAPABILITY RECORD

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 4

Default: F0140009h



Bit Range	Default & Access	Field Name (ID): Description
31:28	Fh RO	**Vendor ID (VEND_CAP):** Indicates this is Vendor Specific capability.
27:24	0h RO	**REVID:** Revision ID of capability structure.
23:16	14h RO	**Length (CAP_LENGTH):** Indicates the number of bytes in the capability structure.
15:9	0h RO	**Next Capability (NEXT_CAP):** Points to the next capability structure. This points to NULL.
8:0	9h RO	**Capability ID (CAPID):** Capability ID.

13.1.16 (DEVID_VEND_SPECIFIC_REG)—Offset 94h

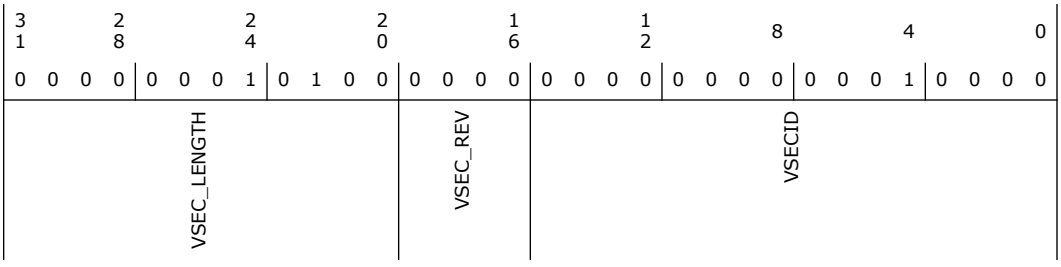
DEVID VENDOR SPECIFIC REG

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 4

Default: 1400010h



Bit Range	Default & Access	Field Name (ID): Description
31:20	14h RO	**VSEC Length (VSEC_LENGTH):** Vendor Specific Capability Length.
19:16	0h RO	**Vendor Revision (VSEC_REV):** Vendor specific revision.
15:0	10h RO	**Vendor ID (VSECID):** Vendor specific ID.

13.1.17 SW LTR update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG)—Offset 98h

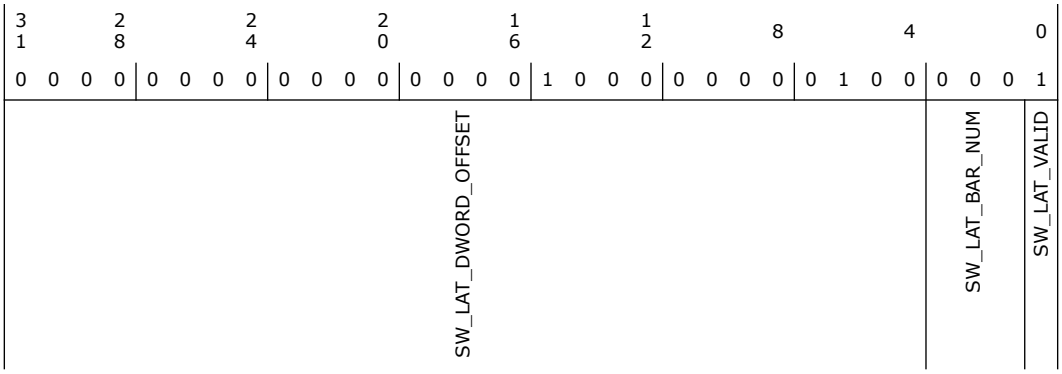
SW LTR Update MMIO Location Register

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 4

Default: 8041h



Bit Range	Default & Access	Field Name (ID): Description
31:4	804h RO	**SWLTRLOC (SW_LAT_DWORD_OFFSET):** This register contains the location pointer to the SW LTR register in MMIO space, as an offset from the specified BAR.
3:1	0h RO	**BAR NUM (SW_LAT_BAR_NUM):** Indicates that the SW LTR update MMIO location is always at BAR0.
0	1h RO	**SW_LAT_VALID:** This value is reflected from the SW LTR valid strap at the top level.

13.1.18 Device IDLE Pointer Register (DEVICE_IDLE_POINTER_REG)—Offset 9Ch

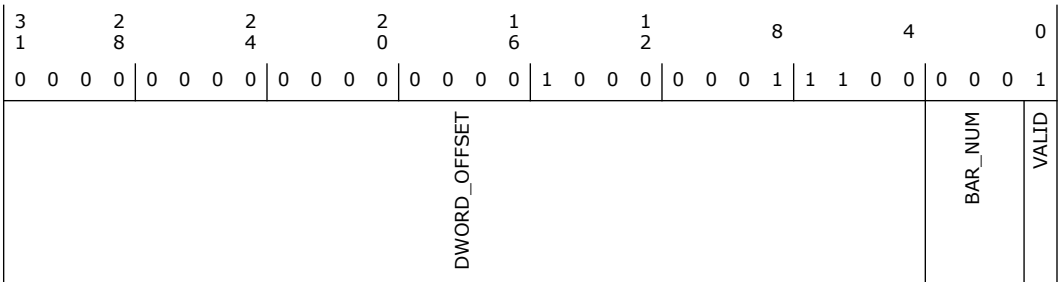
Device IDLE pointer register

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 4

Default: 81C1h



Bit Range	Default & Access	Field Name (ID): Description
31:4	81Ch RO	**DWORD_OFFSET:** This register contains the location pointer to the SW LTR register in MMIO space, as an offset from the specified BAR.
3:1	0h RO	**BAR_NUM:** Indicates that the D0i3 MMIO location is always at BAR0.
0	1h RO	**VALID:** 0= not valid 1= valid

13.1.19 D0I3 Max Power & PG Config (D0I3_MAX_POW_LAT_PG_CONFIG)—Offset A0h

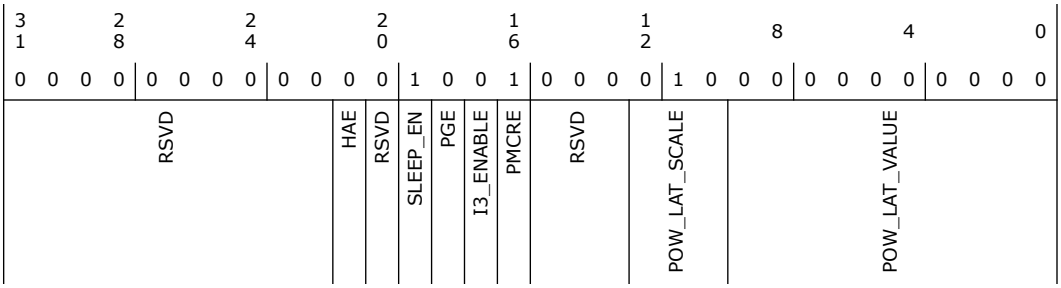
D0idle_Max_Power_On_Latency is set by BIOS at boot and read by device driver SW to calculate approximate cost of a D0idle entry + exit cycle. This allows driver to avoid idle entry in cases where device duty cycle is larger than D0idle entry + exit cycle.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 4

Default: 90800h



Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	Reserved.
21	0h RW	**Hardware Autonomous Enable (HAE):** If set, then the PGCB may request a PG whenever it is idle.
20	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
19	1h RW	**SLEEP_EN:** if clear, then IP will never asset Sleep to the retention flops. If set, then IP may assert Sleep during PG'ing.
18	0h RW	**PG Enable (PGE):** If clear, then IP will never request a PG. If set, then IP may request PG when proper conditions are met.
17	0h RW	**I3_ENABLE:** if set, then IP will PG when idle and the D0i3 register (in PGCB) is set. If this bit is set, the IP will not PG unless the IPs D0i3 control bit ='1'. Bit [5] is not required to be set when this bit is set.
16	1h RW	**PMC Request Enable (PMCRE):** When bits [1:0] = '11', power gating is enabled whenever either the D3 register or the D0i3 register is set.
15:13	0h RO	Reserved.
12:10	2h RW	**Power On Latency Scale (POW_LAT_SCALE):** Support for codes 010 (1us) or 011 (32us) for Exit Latency Scale (1us -) 32ms total span) only.
9:0	0h RW	**Power On Latency value (POW_LAT_VALUE):** This value is written by BIOS to communicate to the Driver.

13.1.20 General Purpose PCI RW Register1 (GEN_REGRW1)—Offset B0h

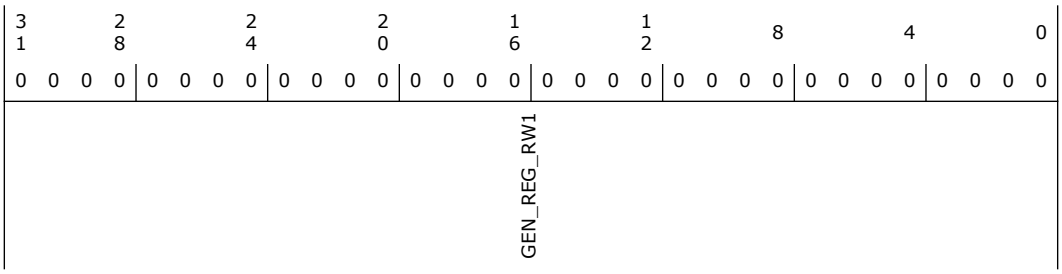
General Purpose PCI Register

Access Method

Type: CFG Register (Size: 32 bits)

Device: 30
Function: 4

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**GEN_REG_RW1**

13.1.21 General Purpose PCI RW Register2 (GEN_REGRW2)—Offset B4h

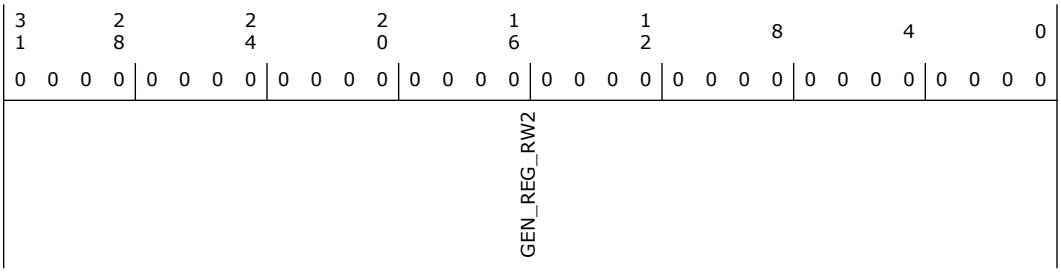
General Purpose PCI Register

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 4

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**GEN_REG_RW2**

13.1.22 General Purpose PCI RW Register3 (GEN_REGRW3)—Offset B8h

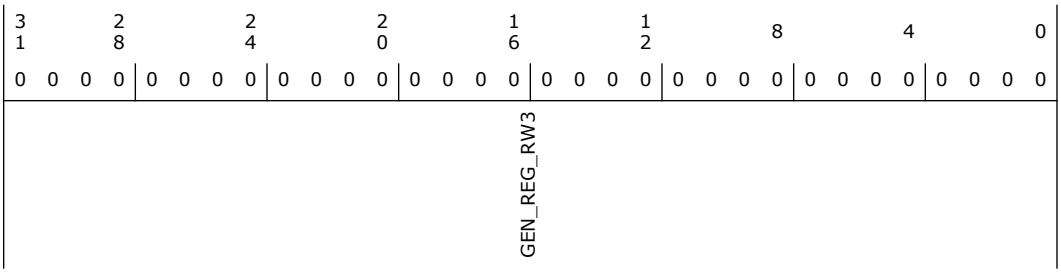
General Purpose PCI Register.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 4

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**GEN_REG_RW3**

13.1.23 General Purpose PCI RW Register4 (GEN_REGRW4)—Offset BCh

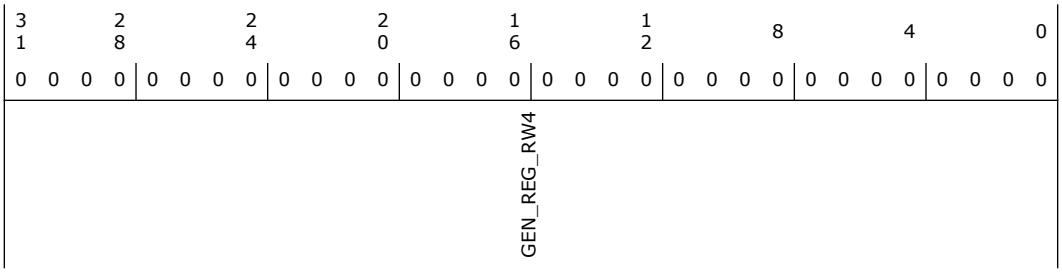
General Purpose PCI Register

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 4

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**GEN_REG_RW4**

13.1.24 General Input Register (GEN_INPUT_REG)—Offset C0h

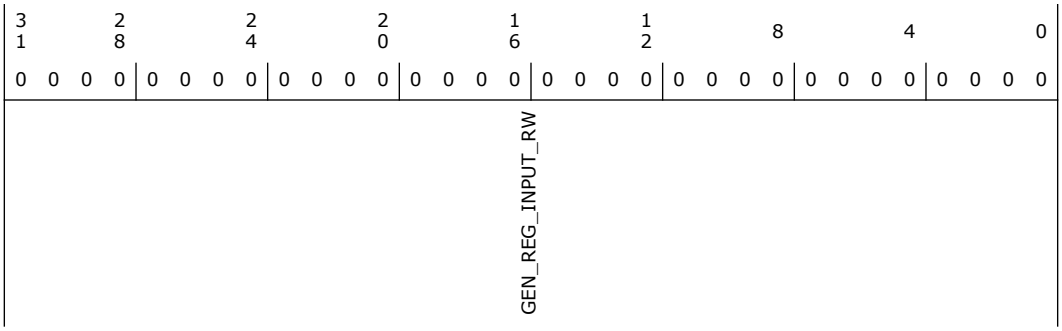
General Purpose Input Register.

Access Method

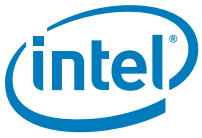
Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 4

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**GEN_REG_INPUT_RW**



13.2 eMMC* Memory Mapped Registers Summary

These registers are memory mapped based on BAR0 defined in PCI configuration space.

Table 13-2. Summary of eMMC* Memory Mapped Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	SDMA System Address Register/Argument2 Register (sdmasysaddr)—Offset 0h	0h
4h	5h	Block Size Register (blocksize)—Offset 4h	0h
6h	7h	Block Count Register (blockcount)—Offset 6h	0h
8h	Bh	Argument1 Register (argument1)—Offset 8h	0h
Ch	Dh	Transfer Mode Register (transfermode)—Offset Ch	0h
Eh	Fh	Command Register (command)—Offset Eh	0h
10h	13h	Response Register (Reponse 0)—Offset 10h	0h
20h	23h	Buffer Data Port Register (dataport)—Offset 20h	0h
24h	27h	Present State Register (PRESENTSTATE)—Offset 24h	0h
28h	28h	Host Control 1 Register (hostcontrol1)—Offset 28h	0h
29h	29h	Power Control Register (powercontrol)—Offset 29h	0h
2Ah	2Ah	Block Gap Control Register (blockgapcontrol)—Offset 2Ah	80h
2Bh	2Bh	Wakeup Control Register (wakeupcontrol)—Offset 2Bh	0h
2Ch	2Dh	Clock Control Register (clockcontrol)—Offset 2Ch	0h
2Eh	2Eh	Timeout Control Register (timeoutcontrol)—Offset 2Eh	0h
2Fh	2Fh	Software Reset Register (softwarereset)—Offset 2Fh	0h
30h	31h	Normal Interrupt Status Register (normalintrsts)—Offset 30h	0h
32h	33h	Error Interrupt Status Register (errorintrsts)—Offset 32h	0h
34h	35h	Normal Interrupt Status Enable Register (normalintrstsena)—Offset 34h	0h
36h	37h	Error Interrupt Status Enable Register (errorintrstsena)—Offset 36h	0h
38h	39h	Normal Interrupt Signal Enable Register (normalintrsigena)—Offset 38h	0h
3Ah	3Bh	Error Interrupt Signal Enable Register (errorintrsigena)—Offset 3Ah	0h
3Ch	3Dh	Auto CMD12 Error Status Register (autocmderrsts)—Offset 3Ch	0h
3Eh	3Fh	Host Control2 Register (hostcontrol2)—Offset 3Eh	0h
40h	47h	Capabilities Register (capabilities)—Offset 40h	0h
48h	4Fh	Maximum Current Capabilities Register (maxcurrentcap)—Offset 48h	0h
50h	51h	Force Event REGISTER for AUTO CMD Error Status (ForceEventforAUTOCMDErrorStatus)—Offset 50h	0h
52h	53h	Force Event Register for Error Interrupt Status (forceeventforerrintsts)—Offset 52h	0h
54h	54h	ADMA Error Status Register (admaerrsts)—Offset 54h	0h
58h	5Bh	ADMA System Address Register0&1 (admasysaddr01)—Offset 58h	0h

Table 13-2. Summary of eMMC* Memory Mapped Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
5Ch	5Dh	ADMA System Address Register1 (admasysaddr2)—Offset 5Ch	0h
5Eh	5Fh	ADMA System Address Register1 (admasysaddr3)—Offset 5Eh	0h
60h	61h	Preset Value Register for Initialization (Preset Value 0)—Offset 60h	3h
62h	63h	Preset Value Register for Default Speed (Preset Value 1)—Offset 62h	0h
64h	65h	Preset Value Register for High Speed (Preset Value 2)—Offset 64h	0h
66h	67h	Preset Value Register for SDR12 (Preset Value 3)—Offset 66h	0h
68h	69h	Preset Value Register for SDR25 (Preset Value 4)—Offset 68h	0h
6Ah	6Bh	Preset Value Register for SDR50 (Preset Value 5)—Offset 6Ah	0h
6Ch	6Dh	Preset Value Register for SDR104 (Preset Value 6)—Offset 6Ch	0h
6Eh	6Fh	Preset Value Register for DDR50 (Preset Value 7)—Offset 6Eh	0h
70h	73h	Boot Timeout Control Register (boottimeoutcnt)—Offset 70h	0h
FCh	FDh	Slot Interrupt Status Register (slotintrsts)—Offset FCh	0h
FEh	FFh	Host Controller Version Register (hostcontrollerver)—Offset FEh	1002h

13.2.1 SDMA System Address Register/Argument2 Register (sdmasysaddr)—Offset 0h

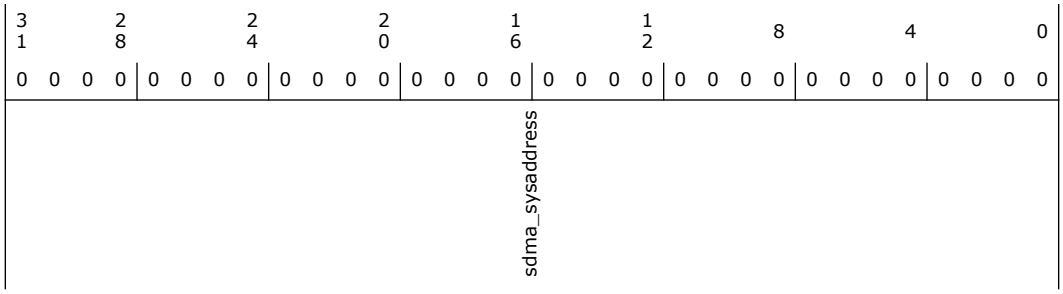
This register contains concatinates reg_sdmasysaddrlo and reg_sdmasysaddrhi

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 4

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h	**SDMA System Address Register/Argument2 Register (sdma_sysaddress):** This register contains the physical system memory address used for DMA transfers or the second argument for the Auto CMD23.

13.2.2 Block Size Register (blocksize)—Offset 4h

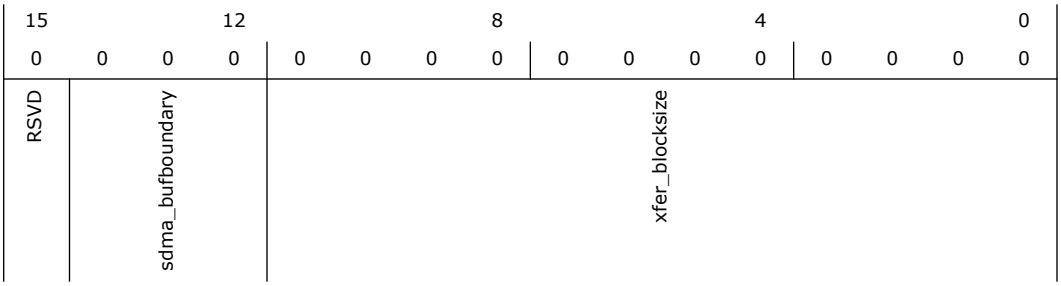
This register is used to configure the number of bytes in a data block

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 30
Function: 4

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	Reserved.
14:12	0h	**Host DMA Buffer Size (sdma_bufboundary):** To perform long DMA transfer, System Address register shall be updated at every system boundary during DMA transfer. These bits specify the size of contiguous buffer in the system memory. These bits shall support when the DMA Support in the Capabilities register is set to 1 and this function is active when the DMA Enable in the Transfer Mode register is set to 1. 000b - 4KB(Detects A11 Carry out) 001b - 8KB(Detects A12 Carry out) 010b - 16KB(Detects A13 Carry out) 011b - 32KB(Detects A14 Carry out) 100b - 64KB(Detects A15 Carry out) 101b -128KB(Detects A16 Carry out) 110b - 256KB(Detects A17 Carry out) 111b - 512KB(Detects A18 Carry out)
11:0	0h	**Transfer Block Size (xfer_blocksize):** This register specifies the block size for block data transfers for CMD17, CMD18, CMD24, CMD25, and CMD53. It can be accessed only if no transaction is executing. Read operations during transfer return an invalid value and write operations shall be ignored. 0000h - No Data Transfer 0001h - 1 Byte 0002h - 2 Bytes 0003h - 3 Bytes 0004h - 4 Bytes 01FFh - 511 Bytes 0200h - 512 Bytes 0800h - 2048 Bytes

13.2.3 Block Count Register (blockcount)—Offset 6h

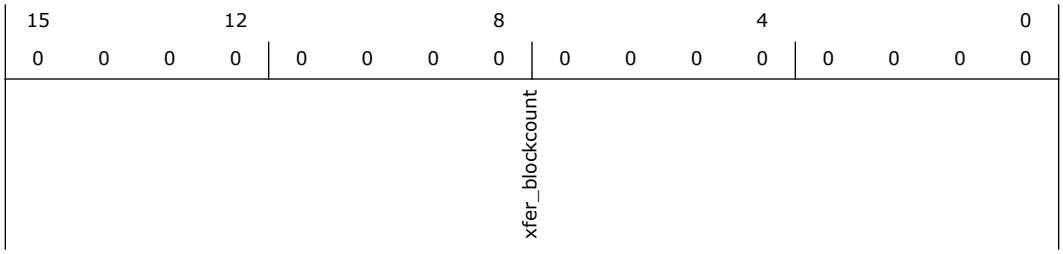
This register is enabled when Block Count Enable in the Transfer Mode register is set to 1 and is valid only for multiple block transfers. The HC decrements the block count after each block transfer and stops when the count reaches zero.
0000h - Stop Count
0001h - 1 block
0002h - 2 blocks
FFFFh - 65535 blocks.

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 30
Function: 4

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:0	0h	**xfer_blockcount (xfer_blockcount):** This Register specifies Block Size for Data Transfers

13.2.4 Argument1 Register (argument1)—Offset 8h

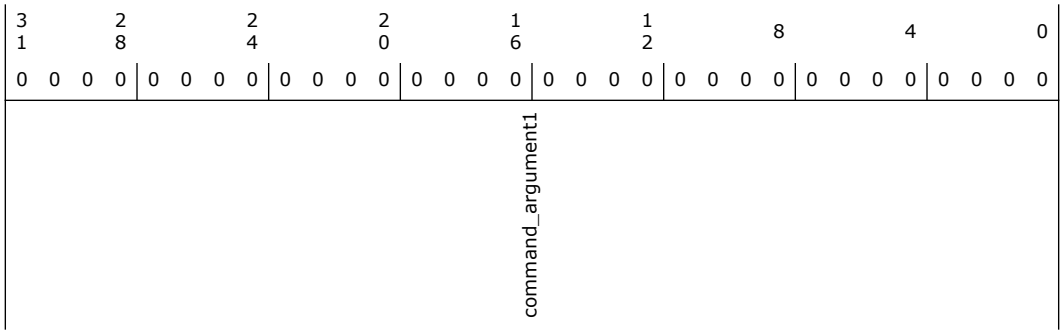
The SD/eMMC* Command Argument is specified as bit39- 8 of Command-Format.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 4

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h	**command_argument1 (command_argument1):** The Command Argument is specified as bit39-8 of Command-Format

13.2.5 Transfer Mode Register (transfermode)—Offset Ch

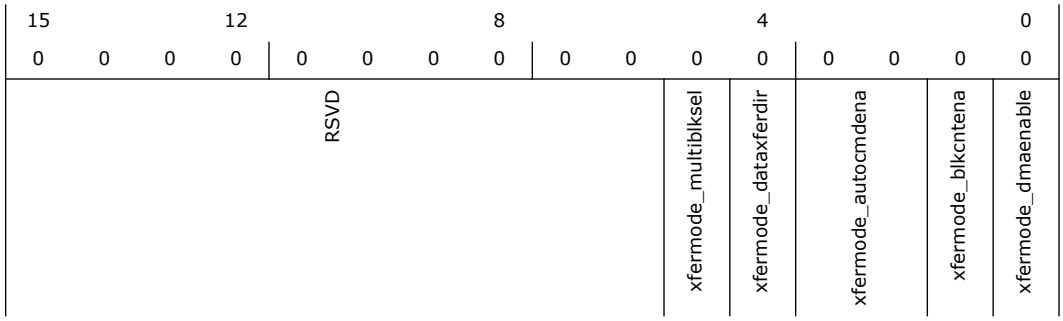
This register is used to control the operations of data transfers

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 30
Function: 4

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:6	0h RO	Reserved.
5	0h	**Multi / Single Block Select (xfermode_multiblksel):** This bit enables multiple block data transfers. 0 - Single Block 1 - Multiple Block.
4	0h	**Data Transfer Direction Select (xfermode_dataxferdir):** This bit defines the direction of data transfers. 0 - Write (Host to Card) 1 - Read (Card to Host)
3:2	0h	**Auto CMD Enable (xfermode_autocmdena):** This field determines use of auto command functions 00b - Auto Command Disabled 01b - Auto CMD12 Enable 10b - Auto CMD23 Enable.
1	0h	**Block Count Enable (xfermode_blkcntena):** This bit is used to enable the Block count register, which is only relevant for multiple block transfers. When this bit is 0, the Block Count register is disabled, which is useful in executing an infinite transfer. 0 - Disable 1 - Enable.
0	0h	**DMA Enable (xfermode_dmaenable):** If this bit is set to 1, a DMA operation shall begin when the HD writes to the upper byte of Command register (00Fh). 0 - Disable 1 - Enable.

13.2.6 Command Register (command)—Offset Eh

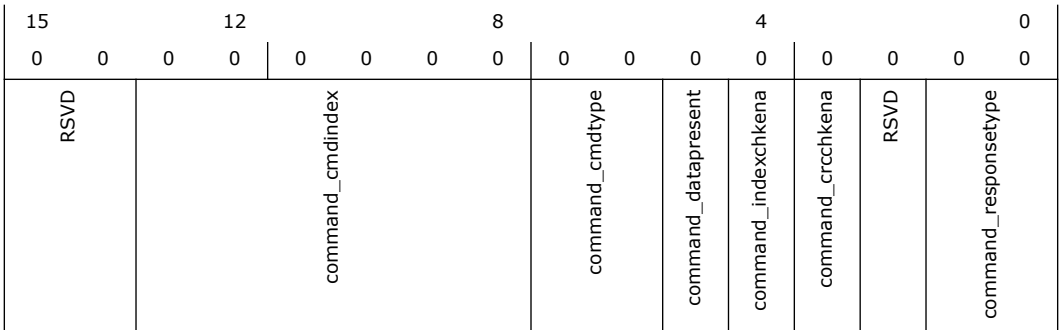
This register is used to program the Command for host controller

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 30
Function: 4

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RO	Reserved.
13:8	0h	**Command Index (command_cmdindex):** This bit shall be set to the command number (CMD0-63, ACMD0-63).
7:6	0h	**Command Type (command_cmdtype):** There are three types of special commands; Suspend, Resume and Abort. These bits shall bet set to 00b for all other commands.
5	0h	**Data Present Select (command_datapresent):** This bit is set to 1 to indicate that data is present and shall be transferred using the DAT line.
4	0h	**Command Index Check Enable (command_indexchkena):** If this bit is set to 1, the HC shall check the index field in the response to see if it has the same value as the command index.
3	0h	**Command CRC Check Enable (command_crcchkena):** If this bit is set to 1, the HC shall check the CRC field in the response.
2	0h RO	Reserved.
1:0	0h	**Response Type Select (command_responsetype):** 00 - No Response 01 - Response length 136 10 - Response length 48.

13.2.7 Response Register (Reponse 0)—Offset 10h

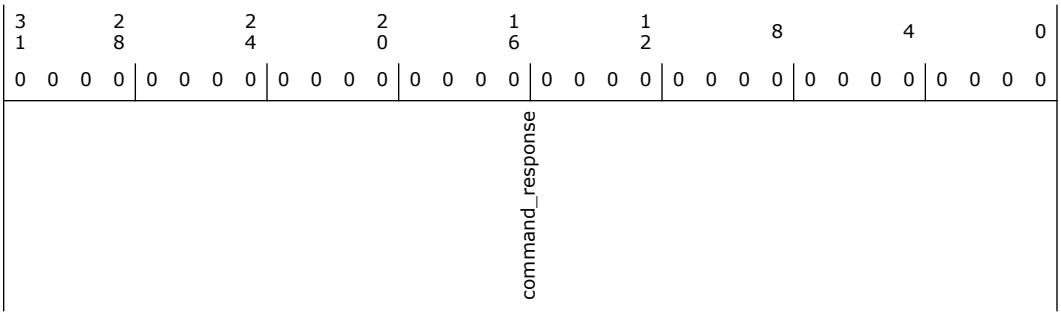
The response registers contains the 128 bit response received from the External Device . The response registers are available at the following offset: Response Register 0: offset 0x010h
Response Register 1: offset 0x012h
Response Register 2: offset 0x014h
Response Register 3: offset 0x016h
Response Register 4: offset 0x018h
Response Register 5: offset 0x01Ah
Response Register 6: offset 0x01Ch
Response Register 7: offset 0x01Eh.

Access Method

Type: MEM Register (Size: 32 bits)

Device: 30
Function: 4

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h	**command_response (command_response):** R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit

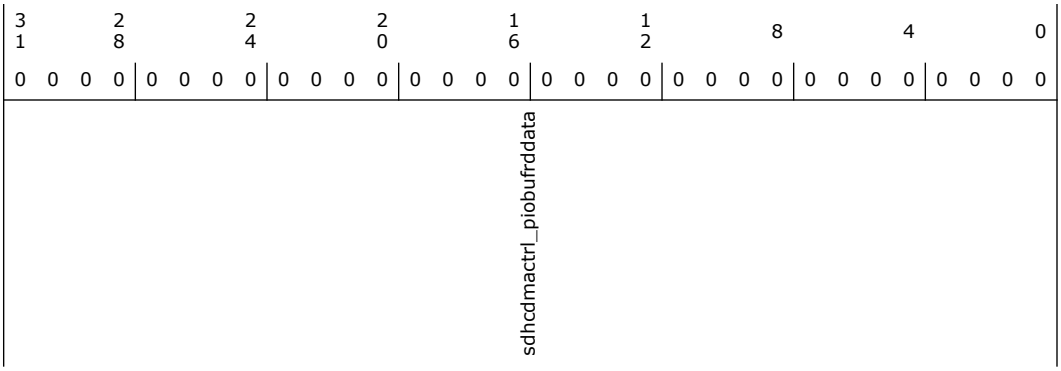
13.2.8 Buffer Data Port Register (dataport)—Offset 20h

The Host Controller Buffer can be accessed through this 32-bit Data Port Register.

Access Method

Type: MEM Register (Size: 32 bits)
Device: 30
Function: 4

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**sdhcdmactrl_piobufrddata:** The Host Controller Buffer can be accessed through this 32-bit Data Port Register.

13.2.9 Present State Register (PRESENTSTATE)—Offset 24h

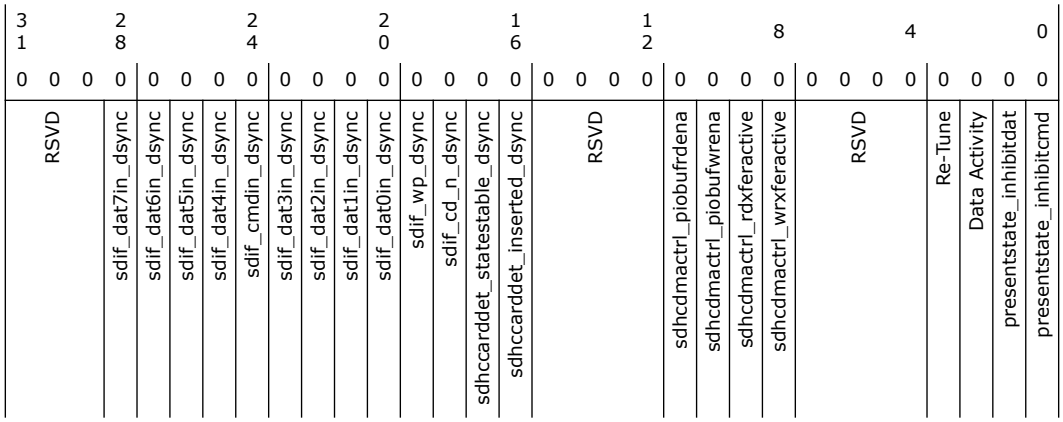
The Host Driver can get status of the Host Controller from this 32-bit read-only register

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 4

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	Reserved.
28	0h RO	**DAT7 Line Signal Level (sdif_dat7in_dsync):** This status is used to check DAT line level to recover from errors, and for debugging.
27	0h RO	**DAT6 Line Signal Level (sdif_dat6in_dsync):** This status is used to check DAT line level to recover from errors, and for debugging.
26	0h RO	**DAT5 Line Signal Level (sdif_dat5in_dsync):** This status is used to check DAT line level to recover from errors, and for debugging.
25	0h RO	**DAT4 Line Signal Level (sdif_dat4in_dsync):** This status is used to check DAT line level to recover from errors, and for debugging.
24	0h RO	**CMD Line Signal Level (sdif_cmdin_dsync):** This status is used to check CMD line level to recover from errors, and for debugging
23	0h RO	**DAT3 Line Signal Level (sdif_dat3in_dsync):** This status is used to check DAT line level to recover from errors, and for debugging. This is
22	0h RO	**DAT2 Line Signal Level (sdif_dat2in_dsync):** This status is used to check DAT line level to recover from errors, and for debugging. This is
21	0h RO	**DAT1 Line Signal Level (sdif_dat1in_dsync):** This status is used to check DAT line level to recover from errors, and for debugging.
20	0h RO	**DAT0 Line Signal Level (sdif_dat0in_dsync):** This status is used to check DAT line level to recover from errors, and for debugging.
19	0h RO	**Write Protect Switch Pin Level (sdif_wp_dsync):** The Write Protect Switch is supported for memory and combo cards. This bit reflects the SDWP# pin. 0 - Write protected (SDWP# = 0) 1 - Write enabled (SDWP# = 1).
18	0h RO	**Card Level Detect (sdif_cd_n_dsync):** This bit reflects the inverse value of the SDCD# pin. 0 - No Card present (SDCD# = 1) 1 - Card present (SDCD# = 0).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**Card State Stable (sdhccarddet_statestable_dsync):** This bit is used for testing. If it is 0, the Card Detect Pin Level is not stable. If this bit is set to 1, it means the Card Detect Pin Level is stable. The Software Reset For All in the Software Reset Register shall not affect this bit. 0 - Reset of Debouncing 1 - No Card or Inserted.
16	0h RO	**Card Inserted (sdhccarddet_inserted_dsync):** This bit indicates whether a card has been inserted. Changing from 0 to 1 generates a Card Insertion Interrupt in the Normal Interrupt Status register and changing from 1 to 0 generates a Card Removal Interrupt in the Normal Interrupt Status register.
15:12	0h RO	Reserved.
11	0h RO	**Buffer Read Enable (sdhcdmactrl_piobufrdena):** This status is used for non-DMA read transfers. This read only flag indicates that valid data exists in the host side buffer status. If this bit is 1, readable data exists in the buffer. A change of this bit from 1 to 0 occurs when all the block data is read from the buffer. A change of this bit from 0 to 1 occurs when all the block data is ready in the buffer and generates the Buffer Read Ready Interrupt. 0 - Read Disable 1 - Read Enable
10	0h RO	**Buffer Write Enable (sdhcdmactrl_piobufwrena):** This status is used for non-DMA write transfers. This read only flag indicates if space is available for write data. If this bit is 1, data can be written to the buffer. A change of this bit from 1 to 0 occurs when all the block data is written to the buffer.
9	0h RO	**Read Transfer Active (sdhcdmactrl_rdxferactive):** This status is used for detecting completion of a read transfer. This bit is set to 1 for either of the following conditions: • After the end bit of the read command • When writing a 1 to continue Request in the Block Gap Control register to restart a read transfer. This bit is cleared to 0 for either of the following conditions: • When the last data block as specified by block length is transferred to the system. • When all valid data blocks have been transferred to the system and no current block transfers are being sent as a result of the Stop At Block Gap Request set to 1. A transfer complete interrupt is generated when this bit changes to 0. 1 - Transferring data 0 - No valid data
8	0h RO	**Write Transfer Active (sdhcdmactrl_wrxferactive):** This status indicates a write transfer is active. If this bit is 0, it means no valid write data exists in the HC. This bit is set in either of the following cases: • After the end bit of the write command. • When writing a 1 to Continue Request in the Block Gap Control register to restart a write transfer. This bit is cleared in either of the following cases: • After getting the CRC status of the last data block as specified by the transfer count (Single or Multiple) • After getting a CRC status of any block where data transmission is about to be stopped by a Stop At Block Gap Request. During a write transaction, a Block Gap Event interrupt is generated when this bit is changed to 0, as a result of the Stop At Block Gap Request being set. This status is useful for the HD in determining when to issue commands during write busy. 1 - transferring data 0 - No valid data
7:4	0h RO	Reserved.
3	0h RO	**Re-Tuning Request (Re-Tune):** Host Controller may request Host Driver to execute re-tuning sequence by setting this bit when the data window is shifted by temperature drift and any issue receiving the correct data. This bit is cleared when a command is issued with setting Execute Tuning in the Host Control 2 register. Changing of this bit from 0 to 1 generates Re-Tuning Event. This bit is cleared when a command is issued with setting Execute Tuning in the Host Control 2 register. Changing of this bit from 0 to 1 generates Re-Tuning Event. Refer to Normal Interrupt registers for more detail. This bit isn't set to 1 if Sampling Clock Select in the Host Control 2 register is set to 0 (using fixed sampling clock). 1: Sampling clock needs re-tuning 0: Fixed or well tuned sampling clock

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	**DATA line Active (Data Activity):** This bit indicates whether one of the DAT line on SD bus is in use. 1 - DAT line active 0 - DAT line inactive
1	0h RO	**Command Inhibit (DAT) (presentstate_inhibitdat):** This status bit is generated if either the DAT Line Active or the Read transfer Active is set to 1. If this bit is 0, it indicates the HC can issue the next SD command. Commands with busy signal belong to Command Inhibit (DAT). Changing from 1 to 0 generates a Transfer Complete interrupt in the Normal interrupt status register.
0	0h RO	**Command Inhibit (CMD) (presentstate_inhibitcmd):** If this bit is 0, it indicates the CMD line is not in use and the HC can issue a SD command using the CMD line. This bit is set immediately after the Command register (00Fh) is written. This bit is cleared when the command response is received. Even if the Command Inhibit (DAT) is set to 1, Commands using only the CMD line can be issued if this bit is 0. Changing from 1 to 0 generates a Command complete interrupt in the Normal Interrupt Status register. If the HC cannot issue the command because of a command conflict error or because of Command Not Issued By Auto CMD12 Error, this bit shall remain 1 and the Command Complete is not set. Status issuing Auto CMD12 is not read from this bit. Auto CMD12 and Auto CMD23 consist of two responses. In this case, this bit is not cleared by the response of CMD12 or CMD23 but cleared by the response of a read/write command. Status issuing Auto CMD12 is not read from this bit. So if a command is issued during Auto CMD12 operation, Host Controller shall manage to issue two commands: CMD12 and a command set by Command register.

13.2.10 Host Control 1 Register (hostcontrol1)—Offset 28h

This register is used to program DMA modes, LED Control, Data Transfer Width, High Speed Enable, Card detect test level and signal selection

Access Method

Type: MEM Register (Size: 8 bits)

Device: 30

Function: 4

Default: 0h

7			4				0
0	0	0	0	0	0	0	0
hostctrl1_cdsigselect	hostctrl1_cdtestlevel	hostctrl1_extdatawidth	hostctrl1_dmaselect		hostctrl1_highspeedena	hostctrl1_datawidth	hostctrl1_ledcontrol

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Card Detect Signal Detection (hostctrl1_cdsigselect):** This bit selects source for card detection. 1- The card detect test level is selected 0- SDCD# is selected (for normal use).
6	0h RW	**Card Detect Test Level (hostctrl1_cdtestlevel):** This bit is enabled while the Card Detect Signal Selection is set to 1 and it indicates card inserted or not. Generates (card ins or card removal) interrupt when the normal int sts enable bit is set. 1 - Card Inserted 0 - No Card.
5	0h RW	**Extended Data Transfer Width (hostctrl1_extdatawidth):** This bit controls 8-bit bus width mode for embedded device. Support of this function is indicated in 8-bit Support for Embedded Device in the Capabilities register. If a device supports 8-bit bus mode, this bit may be set to 1. If this bit is 0, bus width is controlled by Data Transfer Width in the Host Control 1 register.
4:3	0h RW	**DMA Select (hostctrl1_dmaselect):** One of supported DMA modes can be selected. The host driver shall check support of DMA modes by referring the Capabilities register. 00 - SDMA is selected 01 - 32-bit Address ADMA1 is selected 10 - 32-bit Address ADMA2 is selected 11 - 64-bit Address ADMA2 is selected.
2	0h	**High Speed Enable (hostctrl1_highspeedena):** This bit is optional. Before setting this bit, the HD shall check the High Speed Support in the capabilities register. If this bit is set to 0 (default), the HC outputs CMD line and DAT lines at the falling edge of the SD clock (up to 25 MHz/ 20MHz for MMC). If this bit is set to 1, the HC outputs CMD line and DAT lines at the rising edge of the SD clock (up to 50 MHz for SD/52MHz for MMC)/ 208Mhz.
1	0h	**Data Transfer Width (hostctrl1_datawidth):** This bit selects the data width of the HC. The HD shall select it to match the data width of the SD card. 1 - 4 bit mode 0 - 1 bit mode.
0	0h RW	**LED Control (hostctrl1_ledcontrol):** This bit is used to caution the user not to remove the card while the SD card is being accessed. If the software is going to issue multiple SD commands, this bit can be set during all transactions. It is not necessary to change for each transaction. 1 - LED on 0 - LED off.

13.2.11 Power Control Register (powercontrol)—Offset 29h

This register is used to program the SD Bus power and voltage level

Access Method

Type: MEM Register (Size: 8 bits)

Device: 30
Function: 4

Default: 0h

7			4				0
0	0	0	0	0	0	0	0
	RSVD		emmc_hwreset	pwrctrl_sdbusvoltage			pwrctrl_sdbuspower

Bit Range	Default & Access	Field Name (ID): Description
7:5	0h RO	Reserved.
4	0h RW	**eMMC HW Reset (emmc_hwreset):** Hardware reset signal is generated for eMMC* card when this bit is set '1' - Drives the hardware reset pin as ZERO (Active LOW to eMMC* card) '0' - Deassert the hardware reset pin.
3:1	0h RW	**SD Bus Voltage Select (pwrctrl_sdbusvoltage):** By setting these bits, the HC selects the voltage level for the SD card. Before setting this register, the HC shall check the voltage support bits in the capabilities register. If unsupported voltage is selected, the Host System shall not supply SD bus voltage 111b - 3.3 V 110b - 3.0 V 101b - 1.8 V.
0	0h RW	**SD Bus Power (pwrctrl_sdbuspower):** Before setting this bit, the SD host driver shall set SD Bus Voltage Select. If the HC detects the No Card State, this bit shall be cleared. 1 - Power on 0 - Power off.

13.2.12 Block Gap Control Register (blockgapcontrol)—Offset 2Ah

This register is used to program the block gap request, read wait control and interrupt at block gap.

Access Method

Type: MEM Register (Size: 8 bits)

Device: 30
Function: 4

Default: 80h

7			4				0
1	0	0	0	0	0	0	0
blkgapctrl_bootackena	blkgapctrl_altbootmode	blkgapctrl_bootenable	blkgapctrl_spimode	blkgapctrl_interrupt	blkgapctrl_rdwaitctrl	blkgapctrl_continue	blkgapctrl_stopatblkgap

Bit Range	Default & Access	Field Name (ID): Description
7	1h RW	**Boot Acknowledge Check (blkgapctrl_bootackena):** To check for the boot acknowledge in boot operation. 1 - wait for boot ack from eMMC* card 0 - Will not wait for boot ack from eMMC* card.
6	0h RW	**Alternate Boot Enable (blkgapctrl_altbootmode):** To start boot code access in alternative mode. 1- To start alternate boot mode access 0 - To stop alternate boot mode access.
5	0h RW	**Boot Code Access (blkgapctrl_bootenable):** To start boot code access 1- To start boot code access 0 - To stop boot code access

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**SPI mode enable (blkgapctrl_spimode):** SPI mode enable bit. 1- SPI mode 0 - SD mode
3	0h RW	**Interrupt at Block Gap (blkgapctrl_interrupt):** This bit is valid only in 4-bit mode of the SDIO card and selects a sample point in the interrupt cycle. Setting to 1 enables interrupt detection at the block gap for a multiple block transfer. If the card cannot signal an interrupt during a multiple block transfer, this bit should be set to 0. When the HD detects an SD card insertion, it shall set this bit according to the CCCR of the card.
2	0h RW	**Read Wait Control (blkgapctrl_rdwaitctrl):** The read wait function is optional for SDIO cards. If the card supports read wait, set this bit to enable use of the read wait protocol to stop read data using DAT[2] line. Otherwise the HC has to stop the SD clock to hold read data, which restricts commands generation. When the HD detects a card insertion, it shall set this bit according to the CCCR of the card. If the card does not support read wait, this bit shall never be set to 1 otherwise DAT line conflict may occur. If this bit is set to 0, Suspend / Resume cannot be supported 1 - Enable Read Wait Control 0 - Disable Read Wait Control
1	0h RW	**Continue Request (blkgapctrl_continue):** This bit is used to restart a transaction which was stopped using the Stop At Block Gap Request. To cancel stop at the block gap, set Stop At block Gap Request to 0 and set this bit to restart the transfer. The HC automatically clears this bit in either of the following cases: 1) In the case of a read transaction, the DAT Line Active changes from 0 to 1 as a read transaction restarts. 2) In the case of a write transaction, the Write transfer active changes from 0 to 1 as the write transaction restarts.
0	0h RW	**Stop At Block Gap Request (blkgapctrl_stopatblkgap):** This bit is used to stop executing a transaction at the next block gap for non- DMA,SDMA and ADMA transfers. Until the transfer complete is set to 1, indicating a transfer completion the HD shall leave this bit set to 1. Clearing both the Stop At Block Gap Request and Continue Request shall not cause the transaction to restart.

13.2.13 Wakeup Control Register (wakeupcontrol)—Offset 2Bh

This register is used to program the wakeup functionality.

Access Method

Type: MEM Register (Size: 8 bits)

Device: 30

Function: 4

Default: 0h

7			4				0
0	0	0	0	0	0	0	0
RSVD					wkupctrl_cardremoval	wkupctrl_cardinsertion	wkupctrl_cardinterrupt

Bit Range	Default & Access	Field Name (ID): Description
7:3	0h RO	Reserved.
2	0h RW	**Wakeup Event On SD Card Removal (wkupctrl_cardremoval):** This bit enables wakeup event via Card Removal assertion in the Normal Interrupt Status register. FN_WUS (Wake up Support) in CIS does not affect this bit. 1 - Enable 0 – Disable.
1	0h RW	**Wakeup On Card Insertion (wkupctrl_cardinsertion):** This bit enables wakeup event via Card Insertion assertion in the Normal Interrupt Status register. FN_WUS (Wake up Support) in CIS does not affect this bit. 1 - Enable 0 – Disable
0	0h RW	**Wakeup Event Enable On Card Interrupt (wkupctrl_cardinterrupt):** This bit enables wakeup event via Card Interrupt assertion in the Normal Interrupt Status register. This bit can be set to 1 if FN_WUS (Wake Up Support) in CIS is set to 1. 1 - Enable 0 - Disable.

13.2.14 Clock Control Register (clockcontrol)—Offset 2Ch

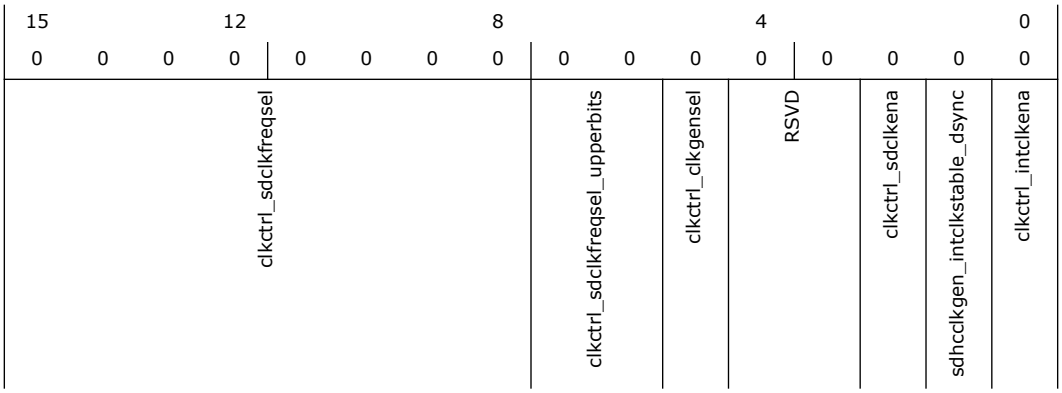
This register is used to program the Clock frequency select, generator select, Clock enable,Internal Clock state fields.

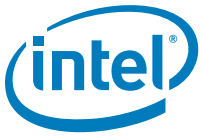
Access Method

Type: MEM Register (Size: 16 bits)

Device: 30
Function: 4

Default: 0h





Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RW	**SDCLK Frequency Select (clkctrl_sdclkfreqsel):** This register is used to select the frequency of the SDCLK pin. The frequency is not programmed directly; rather this register holds the divisor of the Base Clock Frequency For SD clock in the capabilities register. Only the following settings are allowed. 80h - base clock divided by 256 40h - base clock divided by 128 20h - base clock divided by 64 10h - base clock divided by 32 08h - base clock divided by 16 04h - base clock divided by 8 02h - base clock divided by 4 01h - base clock divided by 2 00h - base clock(10MHz-63MHz) Setting 00h specifies the highest frequency of the SD Clock.
7:6	0h RW	**Upper Bits of SDCLK Frequency Select (clkctrl_sdclkfreqsel_upperbits):** Bit 07-06 is assigned to bit 09-08 of clock divider in SDCLK Frequency Select.
5	0h RW	**Clock Generator Select (clkctrl_clkgensel):** This bit is used to select the clock generator mode in SDCLK Frequency Select. If the Programmable Clock Mode is supported (non-zero value is set to Clock Multiplier in the Capabilities register), this bit attribute is RW, and if not supported,this bit attribute is RO and zero is read. This bit depends on the setting of Preset Value Enable in the Host Control 2 register. If the Preset Value Enable = 0, this bit is set by Host Driver. If the Preset Value Enable = 1, this bit is automatically set to a value specified in one of Preset Value registers. 1: Programmable Clock Mode 0: Divided Clock Mode.
4:3	0h RO	Reserved.
2	0h RW	**SD Clock Enable (clkctrl_sdclkena):** The HC shall stop SDCLK when writing this bit to 0. SDCLK frequency Select can be changed when this bit is 0.
1	0h RO	**Internal Clock Stable (sdhcclkgen_intclkstable_dsync):** This bit is set to 1 when SD clock is stable after writing to Internal Clock Enable in this register to 1. The SD Host Driver shall wait to set SD Clock Enable until this bit is set to 1.
0	0h RW	**Internal Clock Enable (clkctrl_intclkena):** This bit is set to 0 when the HD is not using the HC or the HC awaits a wakeup event. The HC should stop its internal clock to go very low power state. 1 - Oscillate 0 - Stop.

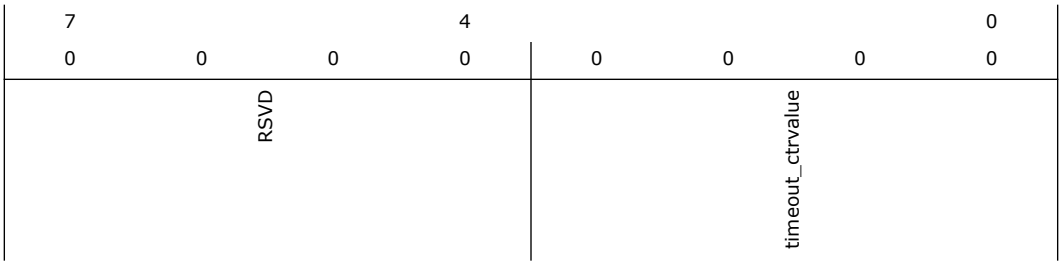
13.2.15 Timeout Control Register (timeoutcontrol)—Offset 2Eh

This value determines the interval by which DAT line time-outs are detected. Refer to the Data Time-out Error in the Error Interrupt Status register for information on factors that dictate time-out generation. Time-out clock frequency will be generated by dividing the sd clock TMCLK by this value. When setting this register, prevent inadvertent time-out events by clearing the Data Time-out Error Status Enable (in the Error Interrupt Status Enable register)
1110 - TMCLK * 2^27
0001 - TMCLK * 2^14
0000 - TMCLK * 2^13.

Access Method

Type: MEM Register (Size: 8 bits)
Device: 30
Function: 4

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7:4	0h RO	Reserved.
3:0	0h RW	**Data Timeout Counter Value (timeout_ctrvalue):** This value determines the interval by which DAT line time-outs are detected.

13.2.16 Software Reset Register (softwarereset)—Offset 2Fh

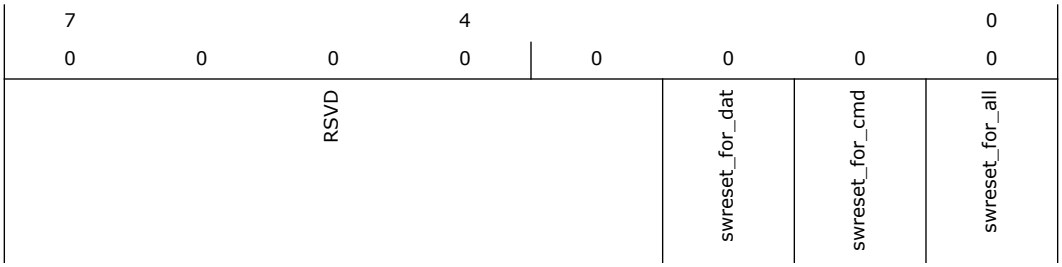
This register is used to program the software reset for data, command and for all.

Access Method

Type: MEM Register
(Size: 8 bits)

Device: 30
Function: 4

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7:3	0h RO	Reserved.
2	0h RW	**Software Reset for DAT Line (swreset_for_dat):** Only part of data circuit is reset. The following registers and bits are cleared by this bit: Buffer Data Port Register - Buffer is cleared and initialized. Present State register - Buffer read Enable - Buffer write Enable - Read Transfer Active - Write Transfer Active - DAT Line Active - Command Inhibit (DAT) Block Gap Control register - Continue Request - Stop At Block Gap Request Normal Interrupt Status register - Buffer Read Ready - Buffer Write Ready - Block Gap Event - Transfer Complete 1 - Reset 0 - Work.
1	0h RW	**Software Reset for CMD Line (swreset_for_cmd):** Only part of command circuit is reset. The following registers and bits are cleared by this bit: Present State register - Command Inhibit (CMD) Normal Interrupt Status register - Command Complete 1 - Reset 0 - Work.
0	0h RW	**Software Reset for All (swreset_for_all):** This reset affects the entire HC except for the card detection circuit. Register bits of type ROC, RW, RW1C, RWAC are cleared to 0. During its initialization, the HD shall set this bit to 1 to reset the HC. The HC shall reset this bit to 0 when capabilities registers are valid and the HD can read them. Additional use of Software Reset For All may not affect the value of the Capabilities registers. If this bit is set to 1, the SD card shall reset itself and must be re initialized by the HD. 1 - Reset 0 - Work

13.2.17 Normal Interrupt Status Register (normalintrsts)—Offset 30h

This register gives the status of all the interrupts

Access Method

Type: MEM Register (Size: 16 bits)

Device: 30

Function: 4

Default: 0h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
reg_errorintrsts	normalintrsts_bootcomplete	normalintrsts_rcvbootack	normalintrsts_retuningevent	normalintrsts_intc	normalintrsts_intb	normalintrsts_inta	normalintrsts_cardintsts	normalintrsts_cardremsts	normalintrsts_cardinssts	normalintrsts_bufrdready	normalintrsts_bufwrready	normalintrsts_dmainterrupt	normalintrsts_blkgapevent	normalintrsts_xfercomplete	normalintrsts_cmdcomplete

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Error Interrupt (reg_errorintrsts):** If any of the bits in the Error Interrupt Status Register are set, then this bit is set. Therefore the HD can test for an error by checking this bit first. 0 - No Error 1 – Error.
14	0h RW1C	**Boot terminate Interrupt (normalintrsts_bootcomplete):** This status is set if the boot operation get terminated 0 - Boot operation is not terminated 1 - Boot operation is terminated.
13	0h RW1C	**Boot Acknowledge Rcv (normalintrsts_rcvbootack):** This status is set if the boot acknowledge is received from device. 0 - Boot ack is not received 1 - Boot ack is received.
12	0h RO	**Re-Tuning Event (normalintrsts_retuningevent):** This status is set if Re-Tuning Request in the Present State register changes from 0 to 1. Host Controller requests Host Driver to perform re-tuning for next data transfer. Current data transfer (not large block count) can be completed without retuning. 1 Re-Tuning should be performed 0 Re-Tuning is not required.
11	0h RO	**INT_C_ Status (normalintrsts_intc):** This status is set if INT_C is enabled and INT_C# pin is in low level. Writing this bit to 1 does not clear this bit. It is cleared by resetting the INT_C interrupt factor.
10	0h RO	**INT_B_Status (normalintrsts_intb):** This status is set if INT_B is enabled and INT_B# pin is in low level. Writing this bit to 1 does not clear this bit. It is cleared by resetting the INT_B interrupt factor.
9	0h RO	**INT_A Status (normalintrsts_inta):** This status is set if INT_A is enabled and INT_A# pin is in low level. Writing this bit to 1 does not clear this bit. It is cleared by resetting the INT_A interrupt factor.
8	0h RO	**Card Interrupt (normalintrsts_cardintsts):** In 1-bit mode, the HC shall detect the Card Interrupt without SD Clock to support wakeup. In 4-bit mode, the card interrupt signal is sampled during the interrupt cycle, so there are some sample delays between the interrupt signal from the card and the interrupt to the Host system. 0 - No Card Interrupt 1 - Generate Card Interrupt.
7	0h RW1C	**Card Removal (normalintrsts_cardremsts):** This status is set if the Card Inserted in the Present State register changes from 1 to 0. When the HD writes this bit to 1 to clear this status the status of the Card Inserted in the Present State register should be confirmed. 0 - Card State Stable or Debouncing 1 - Card Removed.
6	0h RW1C	**Card Insertion (normalintrsts_cardinssts):** This status is set if the Card Inserted in the Present State register changes from 0 to 1.
5	0h	**Buffer Read Ready (normalintrsts_bufrdready):** This status is set if the Buffer Read Enable changes from 0 to 1.
4	0h RW1C	**Buffer Write Ready (normalintrsts_bufwrready):** This status is set if the Buffer Write Enable changes from 0 to 1.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW1C	**DMA Interrupt (normalintrsts_dmainterrupt):** This status is set if the HC detects the Host DMA Buffer Boundary in the Block Size Register.
2	0h RW1C	**Block Gap Event (normalintrsts_blkgapevent):** If the Stop At Block Gap Request in the Block Gap Control Register is set, this bit is set.
1	0h RW1C	**Transfer Complete (normalintrsts_xfercomplete):** This bit is set when a read / write transaction is completed.
0	0h RW1C	**Command Complete (normalintrsts_cmdcomplete):** This bit is set when we get the end bit of the command response (Except Auto CMD12 and Auto CMD23). 0 - No Command Complete 1 - Command Complete

13.2.18 Error Interrupt Status Register (errorintrsts)—Offset 32h

This register gives the status of the error interrupts

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 30
Function: 4

Default: 0h

15			12			8			4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD			errorintrsts_hosterror	RSVD		errorintrsts_admaerror	errorintrsts_autocmderror	errorintrsts_currlimiterror	errorintrsts_dataendbiterror	errorintrsts_datacrcerror	errorintrsts_datatimeouterror	errorintrsts_cmdindexerror	errorintrsts_cmdendbiterror	errorintrsts_cmdcrcerror	errorintrsts_cmdtimeouterror

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO	Reserved.
12	0h	**Target Response Error (errorintrsts_hosterror):** Occurs when detecting ERROR in DMA transaction 0 - no error 1 – error.
11:10	0h RO	Reserved.
9	0h RW	**ADMA Error (errorintrsts_admaerror):** This bit is set when the Host Controller detects errors during ADMA based data transfer. The state of the ADMA at an error occurrence is saved in the ADMA Error Status Register. 1- Error 0- No error.
8	0h RW	**Auto CMD Error (errorintrsts_autocmderror):** This bit is set when detecting that one of the bits D00-D04 in Auto CMD Error Status register has changed from 0 to 1.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Current Limit Error (errorintrsts_currlimiterror):** By setting the SD Bus Power bit in the Power Control Register, the HC is requested to supply power for the SD Bus.
6	0h RW	**Data End Bit Error (errorintrsts_dataendbiterror):** Occurs when detecting 0 at the end bit position of read data which uses the DAT line or the end bit position of the CRC status. 0 - No Error 1 – Error.
5	0h RW	**Data CRC Error (errorintrsts_datacrcerror):** Occurs when detecting CRC error when transferring read data which uses the DAT line or when detecting the Write CRC Status having a value of other than “010”. 0 - No Error 1 – Error.
4	0h RW	**Data Timeout Error (errorintrsts_datatimeouterror):** Occurs when detecting one of following timeout conditions. 1. Busy Timeout for R1b, R5b type. 2. Busy Timeout after Write CRC status 3. Write CRC status Timeout 4. Read Data Timeout 0 - No Error 1 – Timeout.
3	0h RW	**Command Index Error (errorintrsts_cmdindexerror):** Occurs if a Command Index error occurs in the Command Response. 0 - No Error 1 – Error.
2	0h RW	**Command End Bit Error (errorintrsts_cmdendbiterror):** Occurs when detecting that the end bit of a command response is 0. 0 - No Error 1 - End Bit Error Generated.
1	0h RW	**Command CRC Error (errorintrsts_cmdcrcerror):** 0 - No Error 1 - CRC Error Generated.
0	0h RW	**Command Timeout Error (errorintrsts_cmdtimeouterror):** Occurs only if the no response is returned within 64 SDCLK cycles from the end bit of the command. 0 - No Error 1 – Timeout.

13.2.19 Normal Interrupt Status Enable Register (normalintrstsena)—Offset 34h

This register is used to enable the normal interrupt status register fields

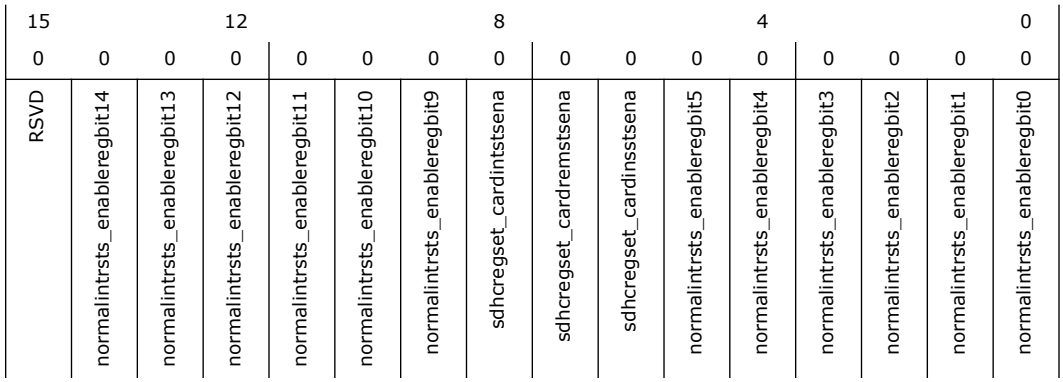
Access Method

Type: MEM Register (Size: 16 bits)

Device: 30

Function: 4

Default: 0h



15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD	normalintrsts_enableregbit14	normalintrsts_enableregbit13	normalintrsts_enableregbit12	normalintrsts_enableregbit11	normalintrsts_enableregbit10	normalintrsts_enableregbit9	sdhcregset_cardintstsena	sdhcregset_cardremstsena	sdhcregset_cardinsstsena	normalintrsts_enableregbit5	normalintrsts_enableregbit4	normalintrsts_enableregbit3	normalintrsts_enableregbit2	normalintrsts_enableregbit1	normalintrsts_enableregbit0

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	Reserved.
14	0h RW	**Boot terminate Interrupt enable (normalintrsts_enableregbit14):** This status is set if the boot operation gets terminated.>BR> 0 - Masked 1 – Enabled.
13	0h RW	**Boot ack rcv enable (normalintrsts_enableregbit13):** This status is set if the boot acknowledge is received from device. 0 - Masked 1 – Enabled.
12	0h	**Re-Tuning Event Status Enable (normalintrsts_enableregbit12):** This status is set if Re-Tuning Request in the Present State register changes from 0 to 1. 0 - Masked 1 – Enabled.
11	0h RW	**INT_C Status Enable (normalintrsts_enableregbit11):** If this bit is set to 0, the Host Controller shall clear the interrupt request to the System. The Host Driver may clear this bit before servicing the INT_C and may set this bit again after all interrupt requests to INT_C pin are cleared to prevent inadvertent interrupts
10	0h RW	**INT_B Status Enable (normalintrsts_enableregbit10):** If this bit is set to 0, the Host Controller shall clear the interrupt request to the System. The Host Driver may clear this bit before servicing the INT_B and may set this bit again after all interrupt requests to INT_B pin are cleared to prevent inadvertent interrupts.
9	0h RW	**INT_A Status Enable (normalintrsts_enableregbit9):** If this bit is set to 0, the Host Controller shall clear the interrupt request to the System. The Host Driver may clear this bit before servicing the INT_A and may set this bit again after all interrupt requests to INT_A pin are cleared to prevent inadvertent interrupts.
8	0h RW	**Card Interrupt Status Enable (sdhcregset_cardintstsena):** If this bit is set to 0, the HC shall clear Interrupt request to the System. The Card Interrupt detection is stopped when this bit is cleared and restarted when this bit is set to 1.
7	0h RW	**Card Removal Status Enable (sdhcregset_cardremstsena):** This status is set if the Card Inserted in the Present State register changes from 1 to 0.
6	0h RW	**Card Insertion Status Enable (sdhcregset_cardinsstsena):** This status is set if the Card Inserted in the Present State register changes from 0 to 1.
5	0h RW	**Buffer Read Ready Status Enable (normalintrsts_enableregbit5):** This status is set if the Buffer Read Enable changes from 0 to 1.
4	0h RW	**Buffer Write Ready Status Enable (normalintrsts_enableregbit4):** This status is set if the Buffer Write Enable changes from 0 to 1.
3	0h RW	**DMA Interrupt Status Enable (normalintrsts_enableregbit3):** This status is set if the HC detects the Host DMA Buffer Boundary in the Block Size register.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Block Gap Event Status Enable (normalintrsts_enableregbit2):** If the Stop At Block Gap Request in the BlockGap Control Register is set, this bit is set.
1	0h RW	**Transfer Complete Status Enable (normalintrsts_enableregbit1):** This bit is set when a read / write transaction is completed.
0	0h RW	**Command Complete Status Enable (normalintrsts_enableregbit0):** This bit is set when we get the end bit of the command response.

13.2.20 Error Interrupt Status Enable Register (errorintrstsena)—Offset 36h

This register is used to enable the Error Interrupt Status register fields.

Access Method

Type: MEM Register (Size: 16 bits)

Device: 30

Function: 4

Default: 0h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD			errorintrsts_enableregbit12	RSVD	errorintrsts_enableregbit10	errorintrsts_enableregbit9	errorintrsts_enableregbit8	errorintrsts_enableregbit7	errorintrsts_enableregbit6	errorintrsts_enableregbit5	errorintrsts_enableregbit4	errorintrsts_enableregbit3	errorintrsts_enableregbit2	errorintrsts_enableregbit1	errorintrsts_enableregbit0

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO	Reserved.
12	0h	**Target Response Error /Host Error Status Enable (errorintrsts_enableregbit12):** 0 - Masked 1 - Enabled
11	0h RO	Reserved.
10	0h	**Tuning error status enable (errorintrsts_enableregbit10):** 0 - Masked 1 - Enabled
9	0h	**ADMA Error Status Enable (errorintrsts_enableregbit9):** 0 - Masked 1 - Enabled
8	0h	**Auto CMD12 Error Status Enable (errorintrsts_enableregbit8):** 0 - Masked 1 - Enabled
7	0h	**Current Limit Error Status Enable (errorintrsts_enableregbit7):** 0 - Masked 1 - Enabled

Bit Range	Default & Access	Field Name (ID): Description
6	0h	**Data End Bit Error Status Enable (errorintrsts_enableregbit6):** 0 - Masked 1 - Enabled
5	0h	**Data CRC Error Status Enable (errorintrsts_enableregbit5):** 0 - Masked 1 - Enabled
4	0h	**Data Timeout Error Status Enable (errorintrsts_enableregbit4):** 0 - Masked 1 - Enabled
3	0h	**Command Index Error Status Enable (errorintrsts_enableregbit3):** 0 - Masked 1 - Enabled
2	0h	**Command End Bit Error Status Enable (errorintrsts_enableregbit2):** 0 - Masked 1 - Enabled
1	0h RW	**Command CRC Error Status Enable (errorintrsts_enableregbit1):** 0 - Masked 1 - Enabled
0	0h RW	**Command Timeout Error Status Enable (errorintrsts_enableregbit0):** 0 - Masked 1 - Enabled

13.2.21 Normal Interrupt Signal Enable Register (normalintrsigena)—Offset 38h

This register is used to enable the Normal Interrupt Signal register. All the bits are RW, except for Reserved bits, and defined as follows:
0 - Masked
1 - Enabled.

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 30
Function: 4

Default: 0h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
normalintrsts_enableregbit15	normalintrsts_enableregbit14	normalintrsts_enableregbit13	normalintrsts_enableregbit12	normalintrsts_enableregbit11	normalintrsts_enableregbit10	normalintrsts_enableregbit9	sdhcregset_cardintstsena	sdhcregset_cardremstsena	sdhcregset_cardinsstsena	normalintrsts_enableregbit5	normalintrsts_enableregbit4	normalintrsts_enableregbit3	normalintrsts_enableregbit2	normalintrsts_enableregbit1	normalintrsts_enableregbit0

Bit Range	Default & Access	Field Name (ID): Description
15	0h	**normalintrsts_enableregbit15 (normalintrsts_enableregbit15):** The HD controls the error Interrupts using the Error Interrupt Signal Enable register.
14	0h	**Boot Terminate Interrupt Signal Enable (normalintrsts_enableregbit14):** Boot Terminate Interrupt Signal Enable
13	0h	**Boot ack rcv Signal Enable (normalintrsts_enableregbit13):** Boot ack rcv Signal Enable
12	0h	**Re-Tuning Event Signal Enable (normalintrsts_enableregbit12):** Re-Tuning Event Signal Enable
11	0h	**INT_C Signal Enable (normalintrsts_enableregbit11):** INT_C Signal Enable
10	0h	**INT_B Signal Enable (normalintrsts_enableregbit10):** INT_B Signal Enable
9	0h	**INT_A Signal Enable (normalintrsts_enableregbit9):** INT_A Signal Enable
8	0h	**Card Interrupt Signal Enable (sdhcregset_cardintstsena):** Card Interrupt Signal Enable
7	0h	**Card Removal Signal Enable (sdhcregset_cardremstsena):** Card Removal Signal Enable
6	0h	**Card Insertion Signal Enable (sdhcregset_cardinsstsena):** Card Insertion Signal Enable
5	0h	**Buffer Read Ready Signal Enable (normalintrsts_enableregbit5):** Buffer Read Ready Signal Enable
4	0h	**Buffer Write Ready Signal Enable (normalintrsts_enableregbit4):** Buffer Write Ready Signal Enable
3	0h	**DMA Interrupt Signal Enable (normalintrsts_enableregbit3):** DMA Interrupt Signal Enable
2	0h	**Block Gap Event Signal Enable (normalintrsts_enableregbit2):** Block Gap Event Signal Enable
1	0h	**Transfer Complete Signal Enable (normalintrsts_enableregbit1):** Transfer Complete Signal Enable
0	0h	**Command Complete Signal Enable (normalintrsts_enableregbit0):** Command Complete Signal Enable

13.2.22 Error Interrupt Signal Enable Register (errorintrsigena)—Offset 3Ah

This register is used to enable the Normal Interrupt Signal register. All the bits are RW, except for Reserved bits, and defined as follows:
0 - Masked
1 - Enabled.

Access Method

Type: MEM Register (Size: 16 bits)

Device: 30
Function: 4

Default: 0h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD			errorintrsig_enableregbit12	RSVD	errorintrsig_enableregbit10	errorintrsig_enableregbit9	errorintrsig_enableregbit8	errorintrsig_enableregbit7	errorintrsig_enableregbit6	errorintrsig_enableregbit5	errorintrsig_enableregbit4	errorintrsig_enableregbit3	errorintrsig_enableregbit2	errorintrsig_enableregbit1	errorintrsig_enableregbit0

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO	Reserved.
12	0h	**errorintrsig_enableregbit12 (errorintrsig_enableregbit12):** Target Response Error Signal Enable
11	0h RO	Reserved.
10	0h	**errorintrsig_enableregbit10 (errorintrsig_enableregbit10):** Tuning Error Signal Enable
9	0h	**errorintrsig_enableregbit9 (errorintrsig_enableregbit9):** ADMA Error Signal Enable
8	0h	**errorintrsig_enableregbit8 (errorintrsig_enableregbit8):** Auto CMD Error Signal Enable
7	0h	**errorintrsig_enableregbit7 (errorintrsig_enableregbit7):** Current Limit Error Signal Enable
6	0h	**errorintrsig_enableregbit6 (errorintrsig_enableregbit6):** Data End Bit Error Signal Enable
5	0h	**errorintrsig_enableregbit5 (errorintrsig_enableregbit5):** Data CRC Error Signal Enable
4	0h	**errorintrsig_enableregbit4 (errorintrsig_enableregbit4):** Data Timeout Error Signal Enable
3	0h	**errorintrsig_enableregbit3 (errorintrsig_enableregbit3):** Command Index Error Signal Enable
2	0h	**errorintrsig_enableregbit2 (errorintrsig_enableregbit2):** Command End Bit Error Signal Enable
1	0h	**errorintrsig_enableregbit1 (errorintrsig_enableregbit1):** Command CRC Error Signal Enable
0	0h	**errorintrsig_enableregbit0 (errorintrsig_enableregbit0):** Command Timeout Error Signal Enable

13.2.23 Auto CMD12 Error Status Register (autocmderrsts)—Offset 3Ch

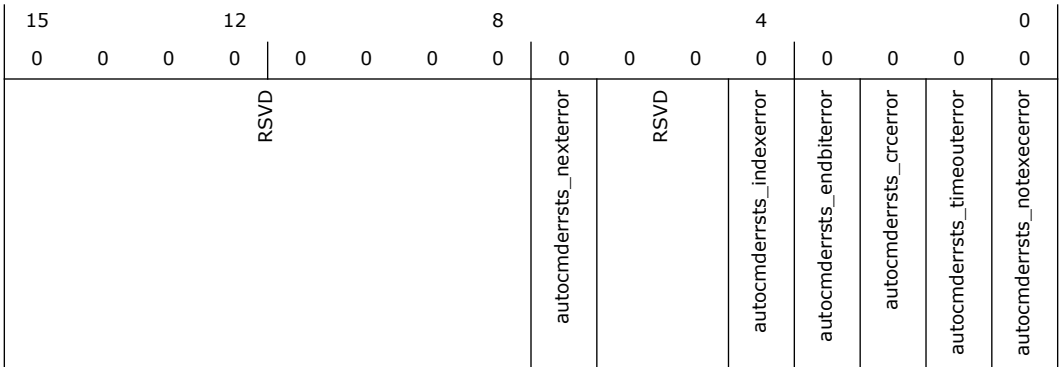
This register is used to indicate CMD12 response error of Auto CMD12 and CMD23 response error of Auto CMD 23

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 30
Function: 4

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	Reserved.
7	0h	**Command Not Issued By Auto CMD12 Error (autocmderrsts_nexterror):** Setting this bit to 1 means CMD_wo_DAT is not executed due to an Auto CMD12 error(D04- D01) in this register. This bit is set to 0 when Auto CMD Error is generated by Auto CMD23 0 – No Error 1 – Not Issued.
6:5	0h RO	Reserved.
4	0h	**Auto CMD Index Error (autocmderrsts_indexerror):** Occurs if the Command Index error occurs in response to a command. 0 – No Error 1 – Error
3	0h RO	**Auto CMD End Bit Error (autocmderrsts_endbiterror):** Occurs when detecting that the end bit of command response is 0. 0 – No Error 1 – End Bit Error Generated.
2	0h RO	**Auto CMD CRC Error (autocmderrsts_crcerror):** Occurs when detecting a CRC error in the command response. 0 – No Error 1 – CRC Error Generated.
1	0h RO	**Auto CMD Timeout Error (autocmderrsts_timeouterror):** Occurs if the no response is returned within 64 SDCLK cycles from the end bit of the command. If this bit is set to 1, the other error status bits (D04 - D02) are meaningless. 0 - No Error 1 - Timeout.
0	0h	**Auto CMD12 not Executed (autocmderrsts_notexecerror):** If memory multiple block data transfer is not started due to command error, this bit is not set because it is not necessary to issue Auto CMD12. Setting this bit to 1 means the HC cannot issue Auto CMD12 to stop memory multiple block transfer due to some error. 0 - Executed 1 - Not Executed.

13.2.24 Host Control2 Register (hostcontrol2)—Offset 3Eh

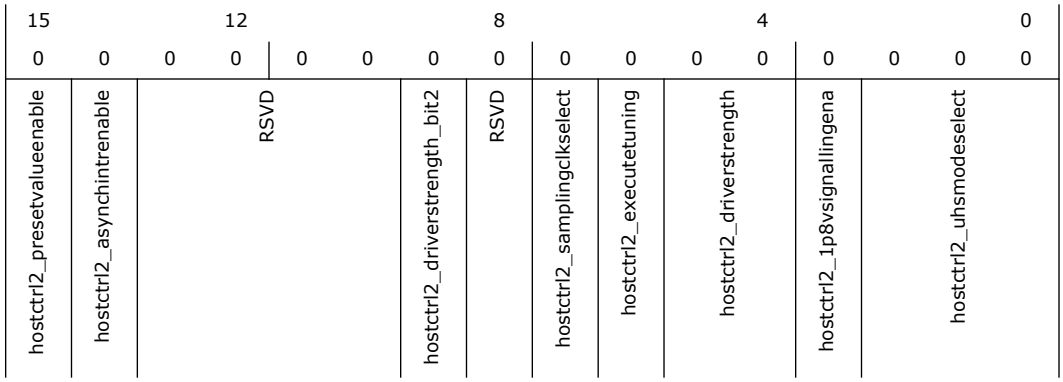
This register is used to program UHS Select Mode,UHS Select Mode,Driver Strength Select,Execute Tuning,Sampling Clock Select,Asynchronous Interrupt Enable and Preset value enable

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 30
Function: 4

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**Preset Value Enable (hostctrl2_presetvalueenable):** Host Controller Version 3.00 supports this bit. As the operating SDCLK frequency and I/O driver strength depend on the Host System implementation, it is difficult to determine these parameters in the Standard Host Driver. When Preset Value Enable is set to automatic. This bit enables the functions defined in the Preset Value registers. 1 Automatic Selection by Preset Value are Enabled 0 SDCLK and Driver Strength are controlled by Host Driver.
14	0h RW	**Asynchronous Interrupt Enable (hostctrl2_asynchintrenable):** This bit can be set to 1 if a card support asynchronous interrupt and Asynchronous Interrupt Support is set to 1 in the Capabilities register. 0 – Disabled 1 – Enabled.
13:10	0h RO	Reserved.
9	0h RW	**Driver strength (hostctrl2_driverstrength_bit2):** This is the programmed Drive Strength output and it[2] of the sdhccore_drivestrength value.
8	0h RO	Reserved.
7	0h RW	**Sampling Clock Select (hostctrl2_samplingclkselect):** This bit is set by tuning procedure when Execute Tuning is cleared. Writing 1 to this bit is meaningless and ignored. Setting 1 means that tuning is completed successfully and setting 0 means that tuning is failed. Controller is receiving response or a read data block. 0 - Fixed clock is used to sample data 1 - Tuned clock is used to sample data
6	0h RW	**Execute Tuning (hostctrl2_executetuning):** This bit is set to 1 to start tuning procedure and automatically cleared when tuning procedure is completed. The result of tuning is indicated to Sampling Clock Select. Tuning procedure is aborted by writing 0 for more detail about tuning procedure. 0 - Not Tuned or Tuning Completed 1 - Execute Tuning.

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW	**Driver Strength Select (hostctrl2_driverstrength):** Host Controller output driver in 1.8V signaling is selected by this bit. In 3.3V signaling, this field is not effective.
3	0h	**1.8V Signaling Enable (hostctrl2_1p8vsignallingena):** This bit controls voltage regulator for I/O cell. 3.3V is supplied to the card regardless of signaling voltage. Setting this bit from 0 to 1 starts changing signal voltage from 3.3V to 1.8V.
2:0	0h RW	**UHS Mode Select (hostctrl2_uhsmodeselect):** This field is used to select one of UHS-I modes and effective when 1.8V Signaling Enable is set to 1. Select in the Clock Control register and Driver Strength Select according to Preset Value registers. In this case, one of preset value registers is selected by this field. Host Driver needs to reset SD Clock Enable before changing this field to avoid generating clock glitch. After setting this field, Host Driver sets SD Clock Enable again. 000b - SDR12 001b - SDR25 010b - SDR50 011b - SDR104 100b - DDR50 101b - HS400

13.2.25 Capabilities Register (capabilities)—Offset 40h

This register provides the host driver with information specific to the host controller implementation. Please note, that the default values shown here assume no bypass of the capabilities register. In case software decides to bypass the default capabilities register values the reset values will present the bypassed value.

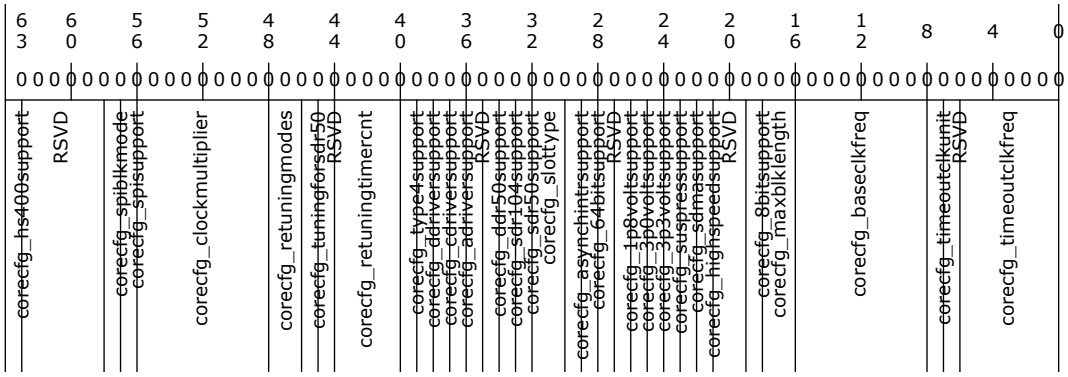
Access Method

Type: MEM Register (Size: 64 bits)

Device: 30

Function: 4

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
63	0h	**HS 400 Support (corecfg_hs400support):** This field indicates whether HS400 is supported or not. 0 –Not Supported 1 –Supported.
62:58	0h RO	Reserved.
57	0h	**SPI Block Mode (corecfg_spiblkmode):** This field indicates whether SPI Block Mode is supported or not. 0 –Not Supported 1 –Supported.
56	0h	**SPI Mode Support (corecfg_spisupport):** This field indicates whether SPI Mode is supported or not. 0 –Not Supported 1 –Supported
55:48	0h	**Clock Multiplier (corecfg_clockmultiplier):** This field indicates clock multiplier value of programmable clock generator. Refer to Clock Control register. Setting 00h means that Host Controller does not support programmable clock generator. FFh Clock Multiplier M = 256 02h Clock Multiplier M = 3 01h Clock Multiplier M = 2 00h Clock Multiplier is Not Supported.
47:46	0h	**Re-tuning modes (corecfg_retuningmodes):** This field defines the re-tuning capability of a Host Controller and how to manage the data transfer length and a Re-Tuning Timer by the Host Driver 00 - Mode1 01 - Mode2 10 - Mode3.
45	0h	**Use Tuning for SDR50 (corecfg_tuningforsdr50):** If this bit is set to 1, this Host Controller requires tuning to operate SDR50. (Tuning is always required to operate SDR104.) 1 SDR50 requires tuning 0 SDR50 does not require tuning.
44	0h RO	Reserved.
43:40	0h	**Timer count for Re-Tuning (corecfg_retuningtimercnt):** This field indicates an initial value of the Re-Tuning Timer for Re-Tuning Mode 1 to 3.
39	0h	**Driver Type 4 Support (corecfg_type4support):** This bit indicates support of Type 4 Driver. 1 Driver Type 4 is Supported 0 Driver Type 4 is Not Supported.
38	0h	**Driver Type D Support (corecfg_ddriversupport):** This bit indicates support of Driver Type D for 1.8 Signaling. 1 Driver Type D is Supported 0 Driver Type D is Not Supported.
37	0h	**Driver Type C Support (corecfg_cdriversupport):** This bit indicates support of Driver Type C for 1.8 Signaling. 1 Driver Type C is Supported 0 Driver Type C is Not Supported.
36	0h	**Driver Type A Support (corecfg_adriversupport):** This bit indicates support of Driver Type A for 1.8 Signaling. 1 Driver Type A is Supported 0 Driver Type A is Not Supported.
35	0h RO	Reserved.
34	0h	**DDR50 Support (corecfg_ddr50support):** This bit indicates whether DDR50 is supported. 0 –Not Supported 1 –Supported.
33	0h	**SDR104 Support (corecfg_sdr104support):** This bit indicates whether SDR104 is supported.SDR104 requires tuning. 0 –Not Supported 1 –Supported.

Bit Range	Default & Access	Field Name (ID): Description
32	0h	**SDR50 Support (corecfg_sdr50support):** This bit indicates whether SDR50 is supported. 0 –Not Supported 1 –Supported.
31:30	0h	**Slot Type (corecfg_slottype):** This field indicates usage of a slot by a specific Host System. (A host controller register set is defined per slot.) Embedded slot for one device (01b) means that only one on-removable device is connected to a SD bus slot. Shared Bus Slot (10b) can be set if Host Controller supports Shared Bus Control register. The Standard Host Driver controls only a removable card or one embedded device is connected to a SD bus slot.
29	0h	**Asynchronous Interrupt Support (corecfg_asynchintrsupport):** This bit indicates whether the HC supports Asynchronous Interrupt 0 –Not Supported 1 –Supported.
28	0h	**64-bit System Bus Support (corecfg_64bitsupport):** This bit indicates whether the HC supports 64bit System Bus 0 –Not Supported 1 –Supported.
27	0h RO	Reserved.
26	0h	**Voltage Support 1.8V (corecfg_1p8voltsupport):** This bit indicates whether the HC supports 1.8V. 0 –Not Supported 1 –Supported.
25	0h	**Voltage Support 3.0V (corecfg_3p0voltsupport):** This bit indicates whether the HC supports 3.0V. 0 –Not Supported 1 –Supported.
24	0h RO	**Voltage Support 3.3V (corecfg_3p3voltsupport):** This bit indicates whether the HC supports 3.3V. 0 –Not Supported 1 –Supported.
23	0h RO	**Suspend / Resume Support (corecfg_suspressupport):** This bit indicates whether the HC supports Suspend/Resume functionality. 0 –Not Supported 1 –Supported.
22	0h RO	**SDMA Support (corecfg_sdmasupport):** This bit indicates whether the HC is capable of using DMA to transfer data between system memory and the HC directly. (SDMA Mode) 0 –Not Supported 1 –Supported
21	0h RO	**High Speed Support (corecfg_highspeedsupport):** This bit indicates whether the HC and the Host System support High Speed mode. 0 –Not Supported 1 –Supported
20:19	0h RO	Reserved.
18	0h RO	**8 Bit Support for Embedded Device (corecfg_8bitsupport):** This bit indicates whether the Host Controller is capable of using 8-bit bus width mode.
17:16	0h RO	**Max Block Length (corecfg_maxblklength):** This value indicates the maximum block size that the HD can read and write to the buffer in the HC. The buffer shall transfer this block size without wait cycles. Sizes can be defined as indicated below. 00 - 512 byte 01 - 1024 byte 10 - 2048 byte 11 - 4096 byte.

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Base Clock Frequency for SD Clock (corecfg_baseclkfreq):** (1) 6-bit Base Clock Frequency This mode is supported by the Host Controller Version 1.00 and 2.00. Upper 2- bit is not effective and always 0. Unit values are1MHz. The supported clock range is 10MHz to 63MHz. 0011 1111b 63MHz 0000 0010b 2MHz 0000 0001b 1MHz (2) 8-bit Base Clock Frequency This mode is supported by the Host Controller Version 3.00. Unit values are 1MHz. The supported clock range is 10MHz to 255MHz. FFh 255MHz 02h 2MHz 01h 1MHz.
7	0h RO	**Timeout Clock Unit (corecfg_timeoutclkunit):** This bit shows the unit of base clock frequency used to detect Data Timeout Error. 0 - KHz 1 - MHz.
6	0h RO	Reserved.
5:0	0h RO	**Timeout Clock Frequency (corecfg_timeoutclkfreq):** This bit shows the base clock frequency used to detect Data Timeout Error. Not 0 - 1Khz to 63Khz or 1Mhz to 63Mhz.

13.2.26 Maximum Current Capabilities Register (maxcurrentcap)—Offset 48h

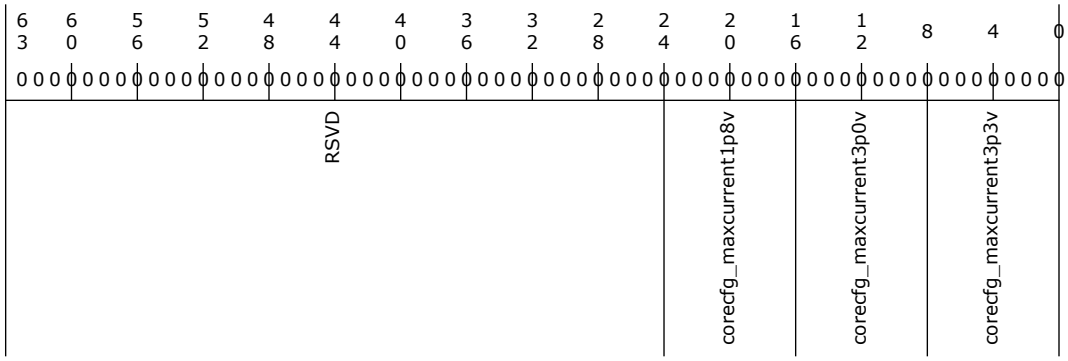
This register indicates maximum current capability for each voltage

Access Method

Type: MEM Register (Size: 64 bits)

Device: 30
Function: 4

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
63:24	0h RO	Reserved.
23:16	0h RO	**Maximum Current for 1.8V (corecfg_maxcurrent1p8v):** 0 – Get value via another method 1 – 4mA 2 – 8mA 3 – 12mA … 255 – 1020mA
15:8	0h RO	**Maximum Current for 3.0V (corecfg_maxcurrent3p0v):** 0 – Get value via another method 1 – 4mA 2 – 8mA 3 – 12mA … 255 – 1020mA
7:0	0h RO	**corecfg_maxcurrent3p3v (corecfg_maxcurrent3p3v):** 0 – Get value via another method 1 – 4mA 2 – 8mA 3 – 12mA … 255 – 1020mA

13.2.27 Force Event REGISTER for AUTO CMD Error Status (ForceEventforAUTOCMDErrorStatus)—Offset 50h

This register is not physically implemented, rather it is an address where Auto CMD Error Status register can be written.

Access Method

Type: MEM Register (Size: 16 bits)

Device: 30
Function: 4

Default: 0h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD								forcecmdnotissuedbyautocmd12err	RSVD		forceautocmdindexerr	forceautocmdendbiterr	forceautocmdcrcerr	forceautocmdtimeouterr	forceautocmdnotexec

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	Reserved.
7	0h RO	**forcecmdnotissuedbyautocmd12err (forcecmdnotissuedbyautocmd12err):** Force Event for Command Not Issued by AUTO CMD12 Error 1 – Interrupt is generated 0 – No Interrupt
6:5	0h RO	Reserved.
4	0h RO	**forceautocmdindexerr (forceautocmdindexerr):** Force Event for AUTO CMD Index Error 1 – Interrupt is generated 0 – No Interrupt
3	0h RO	**forceautocmdendbiterr (forceautocmdendbiterr):** Force Event for AUTO CMD End Bit Error 1 – Interrupt is generated 0 – No Interrupt
2	0h RO	**forceautocmdcrcerr (forceautocmdcrcerr):** Force Event for AUTO CMD Timeout Error 1 – Interrupt is generated 0 – No Interrupt
1	0h RO	**forceautocmdtimeouterr (forceautocmdtimeouterr):** Force Event for AUTO CMD Timeout Error 1 – Interrupt is generated 0 – No Interrupt
0	0h RO	**forceautocmdnotexec (forceautocmdnotexec):** Force Event for AUTO CMD12 Not Executed 1 – Interrupt is generated 0 – No Interrupt

13.2.28 Force Event Register for Error Interrupt Status (forceeventforerrintsts)—Offset 52h

This register is not physically implemented, rather it is an address where Error Interrupt Status register can be written.

Access Method

Type: MEM Register (Size: 16 bits)

Device: 30
Function: 4

Default: 0h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD					forcetuningerr	forceadmaerr	forceautocmderr	forcecurrlimerr	forcedatendbiterr	forcedatcrcerr	forcedattimeouterr	forcecmdindexerr	forcecmdendbiterr	forcecmdcrcerr	forcecmdtimeouterr

Bit Range	Default & Access	Field Name (ID): Description
15:11	0h RO	Reserved.
10	0h RO	**forcetuningerr (forcetuningerr):** Force Event for Tuning Error
9	0h RO	**forceadmaerr (forceadmaerr):** Force Event for ADMA Error'0' no interrupt, '1' interrupt generated
8	0h RO	**forceautocmderr (forceautocmderr):** Force Event for Auto CMD Error '0' no interrupt, '1' interrupt generated
7	0h RO	**forcecurrlimerr (forcecurrlimerr):** Force Event for Current Limit Error '0' no interrupt, '1' interrupt generated
6	0h RO	**forcedatendbiterr (forcedatendbiterr):** Force Event for Data End Bit Error. '0' no interrupt, '1' interrupt generated
5	0h RO	**forcedatcrcerr (forcedatcrcerr):** Force Event for Data CRC Error
4	0h RO	**forcedattimeouterr (forcedattimeouterr):** Force Event for Data Timeout Error '0' no interrupt, '1' interrupt generated
3	0h RO	**forcecmdindexerr (forcecmdindexerr):** Force Event for Command Index Error
2	0h RO	**forcecmdendbiterr (forcecmdendbiterr):** Force Event for Command End Bit Error '0' no interrupt, '1' interrupt generated
1	0h RO	**forcecmdcrcerr (forcecmdcrcerr):** Force Event for Command CRC Error
0	0h RO	**forcecmdtimeouterr (forcecmdtimeouterr):** Force Event for CMD Timeout Error '0' No interrupt, '1' interrupt generated

13.2.29 ADMA Error Status Register (admaerrsts)—Offset 54h

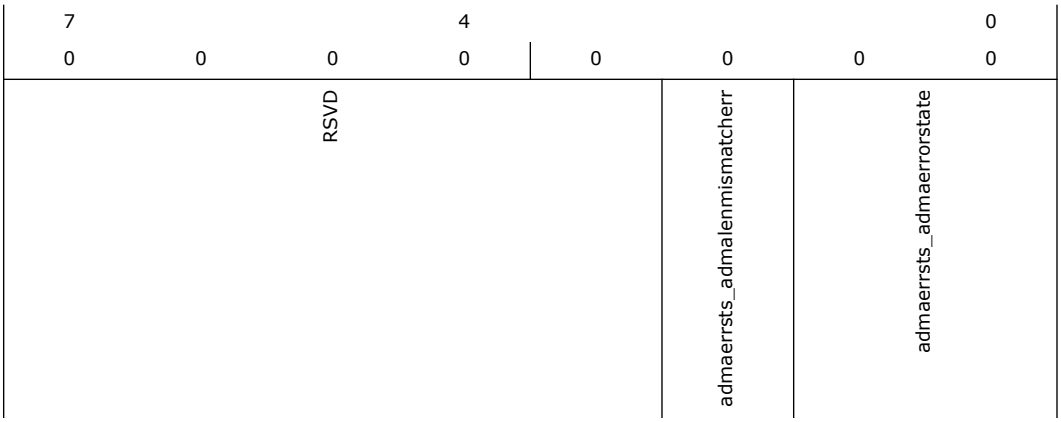
When the ADMA Error interrupt occur, this register holds the ADMA State in ADMA Error States field and ADMA System Address holds address around the error descriptor

Access Method

Type: MEM Register (Size: 8 bits)

Device: 30
Function: 4

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7:3	0h RO	Reserved.
2	0h RO	**admaerrsts_admalenmismatcherr (admaerrsts_admalenmismatcherr):** ADMA Length Mismatch Error This error occurs in the following 2 cases. While Block Count Enable being set, the total data length specified by the Descriptor table is different from that specified by the Block Count and Block Length. Total data length can not be divided by the block length. 1 - Error 0 - No error
1:0	0h RO	**admaerrsts_admaerrorstate (admaerrsts_admaerrorstate):** This field indicates the state of ADMA when error is occurred during ADMA data transfer. This field never indicates "10" because ADMA never stops in this state. D01 – D00 : ADMA Error State when error occurred Contents of SYS_SDR register. 00 - ST_STOP (Stop DMA) Points to next of the error descriptor. 01 - ST_FDS (Fetch Descriptor) Points to the error descriptor 10 - Never set this state (Not used). 11 - ST_TFR (Transfer Data) Points to the next of the error descriptor

13.2.30 ADMA System Address Register0&1 (admasysaddr01)—Offset 58h

This register contains the physical address used for ADMA data transfer

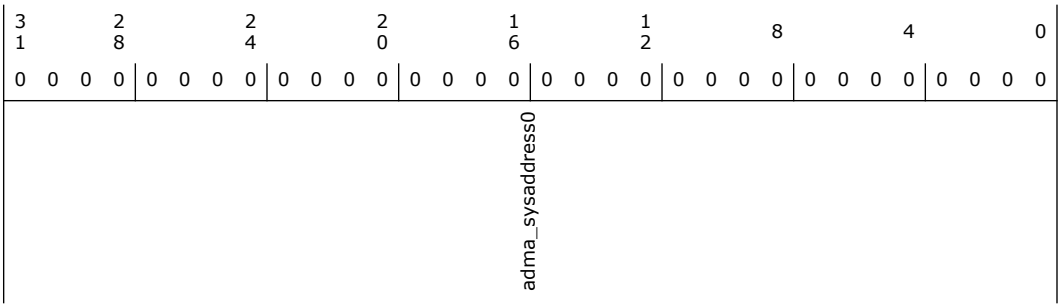
Access Method

Type: MEM Register (Size: 32 bits)

Device: 30

Function: 4

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h	**adma_sysaddress0 (adma_sysaddress0):** This register holds byte address of executing command of the Descriptor table.

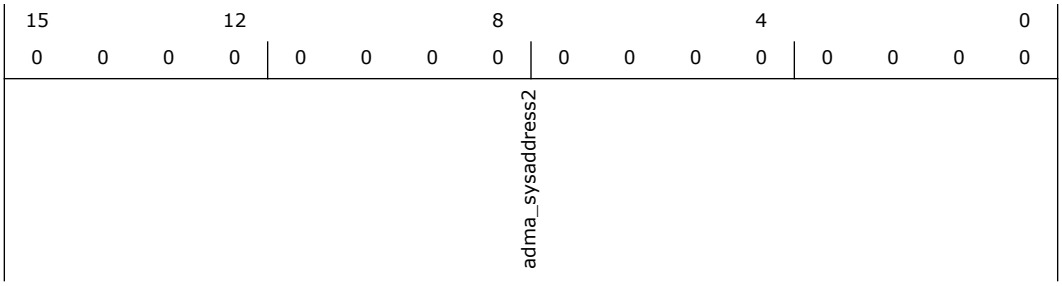
13.2.31 ADMA System Address Register1 (admasysaddr2)—Offset 5Ch

This register contains the physical address used for ADMA data transfer

Access Method

Type: MEM Register (Size: 16 bits)
Device: 30
Function: 4

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:0	0h	**adma_sysaddress2 (adma_sysaddress2):** This register holds byte address of executing command of the Descriptor table.

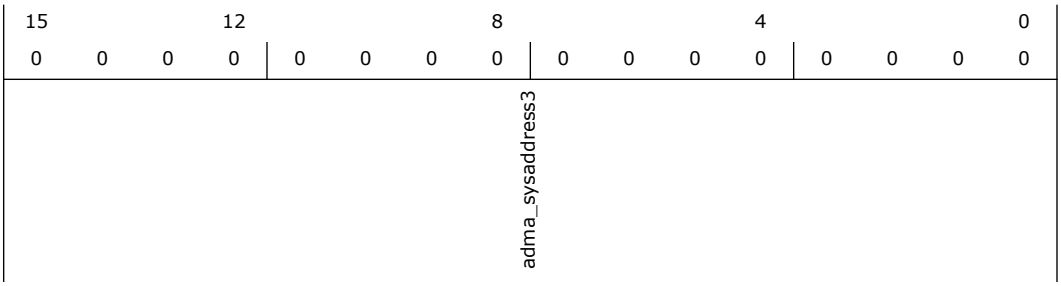
13.2.32 ADMA System Address Register1 (admasysaddr3)—Offset 5Eh

This register contains the physical address used for ADMA data transfer

Access Method

Type: MEM Register (Size: 16 bits)
Device: 30
Function: 4

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:0	0h	**adma_sysaddress3 (adma_sysaddress3):** This register holds byte address of executing command of the Descriptor table.

13.2.33 Preset Value Register for Initialization (Preset Value 0)—Offset 60h

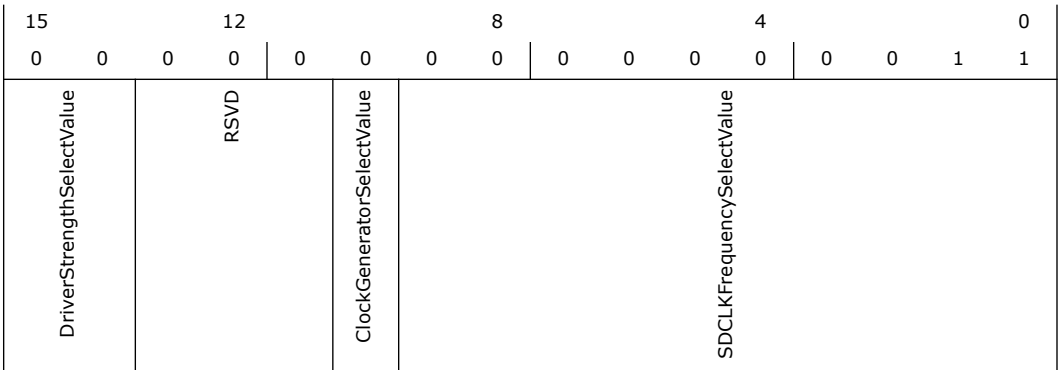
This register is used to read the SDCLK Frequency Select Value,Clock Generator Select Value,Driver Strength Select Value

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 30
Function: 4

Default: 3h



Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RO	**DriverStrengthSelectValue (DriverStrengthSelectValue):** Driver Strength is supported by 1.8V signaling bus speed modes. This field is meaningless for 3.3V signaling. 11b Driver Type D is Selected 10b Driver Type C is Selected 01b Driver Type A is Selected 00b Driver Type B is Selected
13:11	0h RO	Reserved.
10	0h RO	**ClockGeneratorSelectValue (ClockGeneratorSelectValue):** This bit is effective when Host Controller supports programmable clock generator. 1: Programmable Clock Generator 0: Host Controller Ver2.00 Compatible Clock Generator
9:0	3h RO	**SDCLKFrequencySelectValue (SDCLKFrequencySelectValue):** 10-bit preset value to set SDCLK Frequency Select in the Clock Control Register is described by a host system.

13.2.34 Preset Value Register for Default Speed (Preset Value 1)—Offset 62h

Same description as Preset Value 0 register.

13.2.35 Preset Value Register for High Speed (Preset Value 2)—Offset 64h

Same description as Preset Value 0 register.

13.2.36 Preset Value Register for SDR12 (Preset Value 3)—Offset 66h

Same description as Preset Value 0 register.

13.2.37 Preset Value Register for SDR25 (Preset Value 4)—Offset 68h

Same description as Preset Value 0 register.

13.2.38 Preset Value Register for SDR50 (Preset Value 5)—Offset 6Ah

Same description as Preset Value 0 register.

13.2.39 Preset Value Register for SDR104 (Preset Value 6)—Offset 6Ch

Same description as Preset Value 0 register.

13.2.40 Preset Value Register for DDR50 (Preset Value 7)—Offset 6Eh

Same description as Preset Value 0 register.

13.2.41 Boot Timeout Control Register (boottimeoutcnt)—Offset 70h

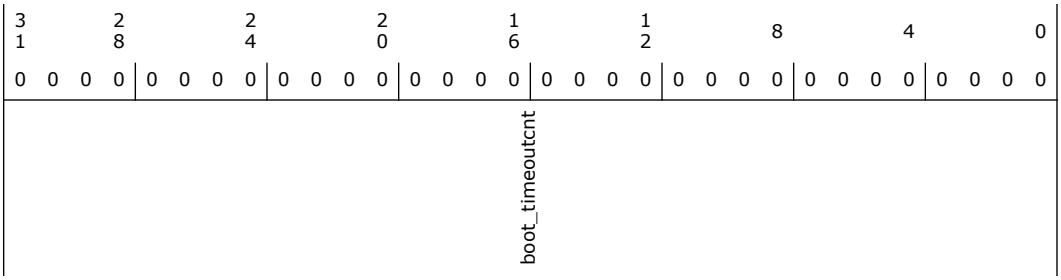
This is used to program the boot timeout value counter

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 4

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**boot_timeoutcnt (boot_timeoutcnt):** This value determines the interval by which DAT line time-outs are detected during boot operation for eMMC* card.

13.2.42 Slot Interrupt Status Register (slotintrsts)—Offset FCh

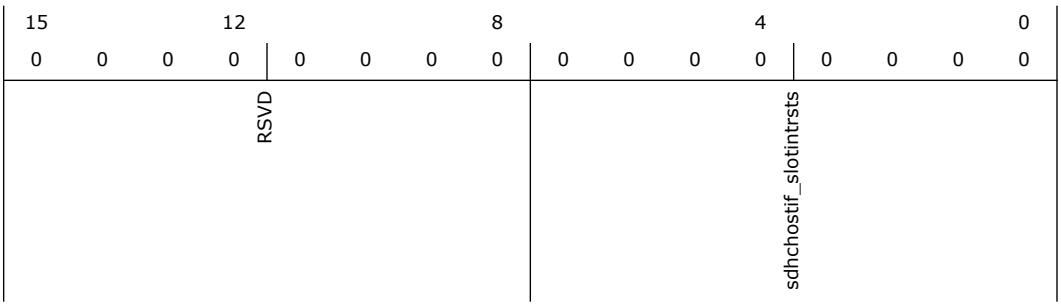
This register is used to read the interrupt signal for each slot.

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 30
Function: 4

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	Reserved.
7:0	0h	**sdhchostif_slotintrsts (sdhchostif_slotintrsts):** These status bits indicate the logical OR of Interrupt signal and Wakeup signal for each slot.

13.2.43 Host Controller Version Register (hostcontrollerver)—Offset FEh

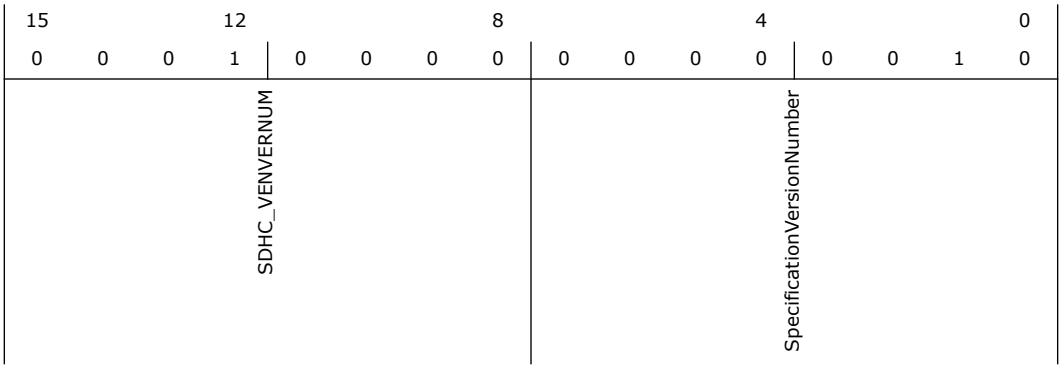
This register is used to read the vendor version number and specification version number

Access Method

Type: MEM Register (Size: 16 bits)

Device: 30
Function: 4

Default: 1002h



Bit Range	Default & Access	Field Name (ID): Description
15:8	10h RO	**SDHC_VENVERNUM (SDHC_VENVERNUM):** This status is reserved for the vendor version number.
7:0	2h RO	**SpecificationVersionNumber (SpecificationVersionNumber):** This status indicates the Host Controller Spec. Version. The upper and lower 4-bits indicate the version.

13.3 EMMC Additional Registers Summary

These registers are memory mapped based on BAR0 defined in PCI configuration space.

Table 13-3. Summary of EMMC Additional Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
804h	807h	Software LTR Value (SW_LTR_val)—Offset 804h	800h
808h	80Bh	Auto LTR Value (Auto_LTR_val)—Offset 808h	800h
810h	813h	Capabilities Bypass (Cap_byps)—Offset 810h	0h
814h	817h	Capabilities Bypass 1 (Cap_byps_reg1)—Offset 814h	3001EF3Ch
818h	81Bh	(Cap_byps_reg2)—Offset 818h	4004000h
81Ch	81Fh	(reg_D0i3)—Offset 81Ch	0h
820h	823h	(Tx_CMD_dly)—Offset 820h	400h
824h	827h	(Tx_DATA_dly_1)—Offset 824h	A18h
828h	82Bh	(Tx_DATA_dly_2)—Offset 828h	1C1C1C00h
82Ch	82Fh	(Rx_CMD_Data_dly_1)—Offset 82Ch	1C1C1C00h
830h	833h	(Rx_Strobe_Ctrl_Path)—Offset 830h	500h
834h	837h	(Rx_CMD_Data_dly_2)—Offset 834h	181Ch
838h	83Bh	(Master_Dll)—Offset 838h	1h
840h	843h	(Auto_tuning)—Offset 840h	0h

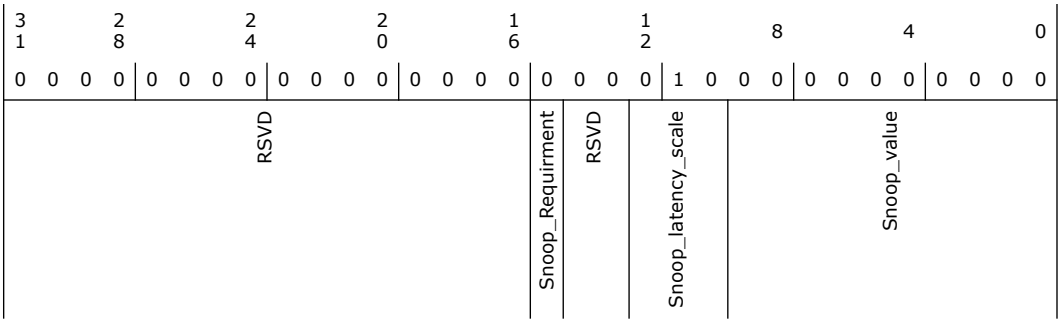
13.3.1 Software LTR Value (SW_LTR_val)—Offset 804h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 4

Default: 800h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	0h RW	**Snoop_Requirment:** If the Requirement (bit 15) is clear, that indicates that the device has no LTR requirement for this type of traffic (i.e. it can wait for service indefinitely). If the 10-bit latency value is zero it indicates that the device cannot tolerate any delay and needs the best possible service/response time.

Bit Range	Default & Access	Field Name (ID): Description
14:13	0h RO	Reserved.
12:10	2h RW	**Snoop_latency_scale:** Support for codes 010 (1us) or 011 (32us) for Snoop Latency Scale(1us -) 32ms total span) only. Writes to this CSR which dont match those values will be dropped completely, next read will return previous value.
9:0	0h RW	**Snoop_value:** 10-bit latency value

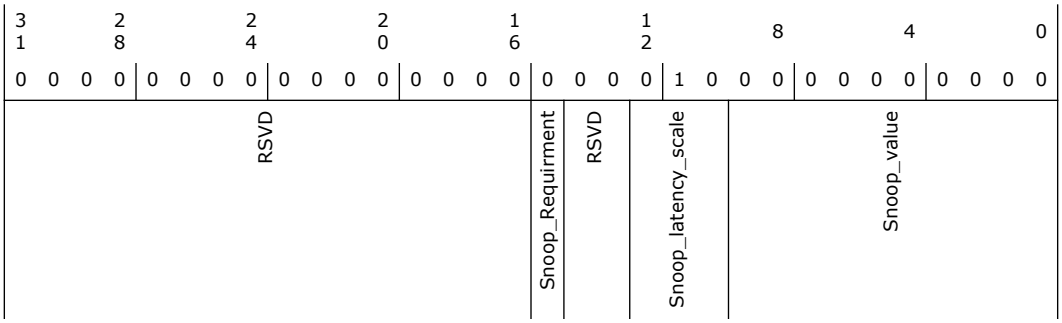
13.3.2 Auto LTR Value (Auto_LTR_val)—Offset 808h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 4

Default: 800h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	0h RW	**Snoop_Requirment:** If the Requirement (bit 15) is clear, that indicates that the device has no LTR requirement for this type of traffic (i.e. it can wait for service indefinitely). If the 10-bit latency value is zero it indicates that the device cannot tolerate any delay and needs the best possible service/response time.
14:13	0h RO	Reserved.
12:10	2h RW	**Snoop_latency_scale:** Support for codes 010 (1us) or 011 (32us) for Snoop Latency Scale(1us -) 32ms total span) only. Writes to this CSR which dont match those values will be dropped completely, next read will return previous value.
9:0	0h RW	**Snoop_value:** 10-bit latency value

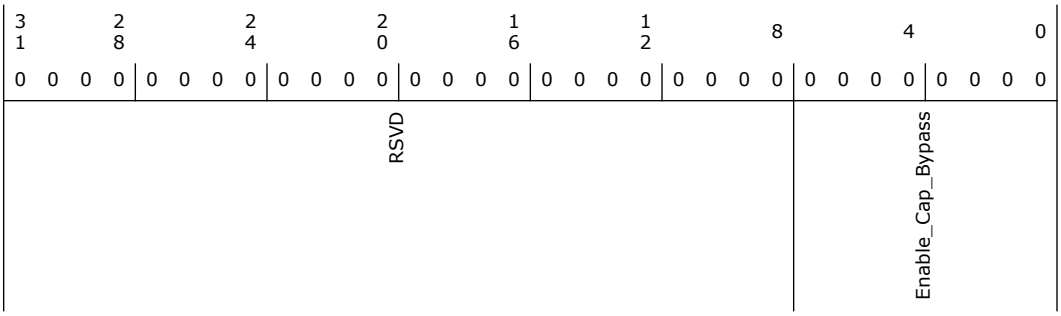
13.3.3 Capabilities Bypass (Cap_byps)—Offset 810h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 4

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	0h RW	**Enable Capabilities Bypass (Enable_Cap_Bypass):** 5Ah: Enable Capabilities Bypass Others: Capabilities Bypass disabled (using default values)

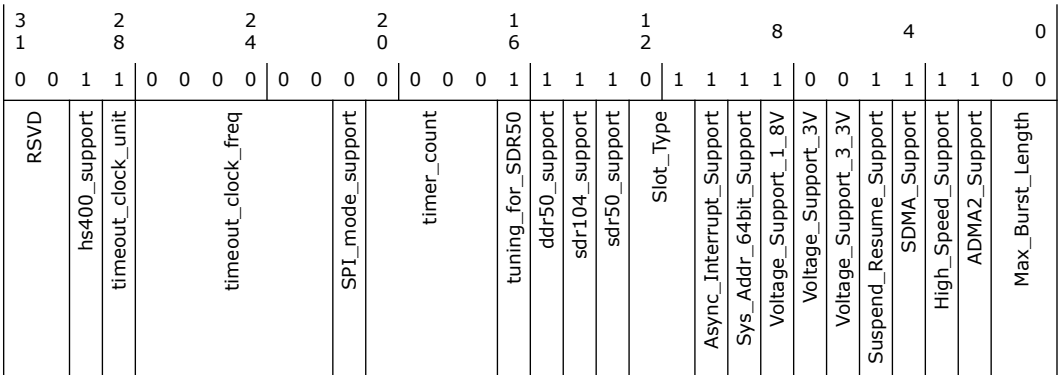
13.3.4 Capabilities Bypass 1 (Cap_byps_reg1)—Offset 814h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 4

Default: 3001EF3Ch



Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29	1h RW	**hs400_support:** 1: HS400 Mode Supported. 0: HS400 Mode NOT Supported
28	1h RW	**timeout_clock_unit:** 1 - to Select MHz Clock 0 - to Select KHz Clock

Bit Range	Default & Access	Field Name (ID): Description
27:22	0h RW	**timeout_clock_freq:** Timeout clock frequency
21	0h RW	**SPI Mode Support (SPI_mode_support):** 1: SPI Mode Supported 0: SPI Mode Not Supported
20:17	0h RW	**Timer Count for Re-Tuning (timer_count):** This is the Timer Count for Re-Tuning Timer for Re-Tuning Mode 1 to 3. Setting to 0h disables Re-Tuning Timer.
16	1h RW	**Use Tuning for SDR50 (tuning_for_SDR50):** 1 = Use Tuning 0 = Don't use Tuning
15	1h RW	**ddr50_support:** 1: DDR50 Mode Supported. 0: DDR50 Mode NOT Supported
14	1h RW	**sdr104_support:** 1: SDR104 Mode Supported. 0: SDR104 Mode NOT Supported
13	1h RW	**sdr50_support:** 1: SDR50 Mode Supported. 0: SDR50 Mode NOT Supported
12:11	1h RW	**Slot_Type:** 00 - Removable SD Card Slot. 01 - Embedded Slot for One Device. 10 - Shared Bus Slot. 11 - Reserved
10	1h RW	**Async_Interrupt_Support:** 1: Asynchronous Interrupt Supported. 0: Asynchronous Interrupt NOT Supported
9	1h RW	**Sys_Addr_64bit_Support:** 1 - Core supports 64-bit System Address Bus. 0 - Core supports only 32-bit System Address Bus
8	1h RW	**Voltage_Support_1_8V:** 1: 1.8V Supported. 0: 1.8V NOT Supported
7	0h RW	**Voltage_Support_3V:** 1: 3.0V Supported. 0: 3.0V NOT Supported
6	0h RW	**Voltage_Support_3_3V:** 1: 3.3V Supported. 0: 3.3V NOT Supported
5	1h RW	**Suspend_Resume_Support:** 1: Suspend/Resume Supported. 0: Suspend/Resume NOT Supported
4	1h RW	**SDMA_Support:** 1: SDMA mode Supported. 0: SDMA mode NOT Supported
3	1h RW	**High_Speed_Support:** 1: HIGH_SPEED mode Supported. 0: HIGH_SPEED mode NOT Supported
2	1h RW	**ADMA2_Support:** 1: ADMA2 mode Supported. 0: ADMA2 mode NOT Supported
1:0	0h RW	**Max_Burst_Length:** Maximum Block Length supported by the Core/Device. 00: 512 (Bytes). 01: 1024. 10: 2048. 11: Reserved

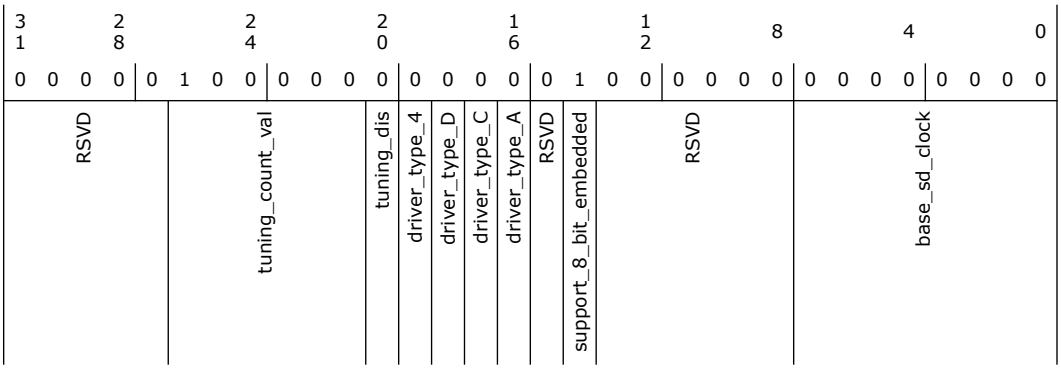
13.3.5 (Cap_byps_reg2)—Offset 818h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 4

Default: 4004000h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	Reserved.
26:21	20h RW	**tuning_count_val:** Tuning Count Value Configures the Number of Taps (Phases) of the rxclk_in that is supported. The Tuning State machine uses this information to select one of the Taps (Phases) of the rxclk_in during the Tuning Procedure.
20	0h RW	**tuning_dis:** Disable the 1.5x Tuning count when calculating total tuning count. The internal tuning count will be set to the corecfg_Tuningcount when this signal is asserted
19	0h RW	**Driver Type 4 Support (driver_type_4):** 1: Supported 0: NOT Supported
18	0h RW	**Driver Type D Support (driver_type_D):** 1: Supported 0: NOT Supported
17	0h RW	**Driver Type C Support (driver_type_C):** 1: Supported 0: NOT Supported
16	0h RW	**Driver Type A Support (driver_type_A):** 1: Supported 0: NOT Supported
15	0h RO	Reserved.
14	1h RW	**8-bit Support for Embedded Device (support_8_bit_embedded):** 1: Supported 0: NOT Supported
13:8	0h RO	Reserved.
7:0	0h RW	**base_sd_clock:** Base Clock Frequency for SD Clock

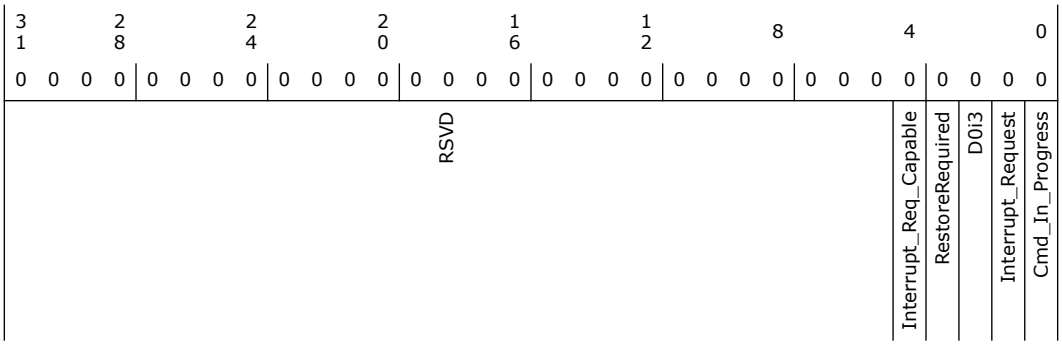
13.3.6 (reg_D0i3)—Offset 81Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 4

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4	0h RO	**Interrupt_Req_Capable:** 0: HW not capable to issue in interrupt on command completion. 1: HW capable to issue an interrupt on command completion
3	0h RO	**RestoreRequired:** When set (by HW), SW must restore state to the IP. The state may have been lost due to a reset or full power lost. SW clears the bit by writing a 1. This bit will be set on initial power up.
2	0h RW	**D0i3:** SW sets this bit to 1 to move the IP into the D0i3 state. Writing this bit to 0 will return the IP to the fully active D0 state (D0i0).
1	0h RO	**Interrupt_Request:** SW sets this bit to 1 to ask for an interrupt to be generated on completion of the command. SW must clear or set this on each write to this register. Not supported in SCS!
0	0h RO	**Cmd_In_Progress:** HW sets this bit on a 1->0 or 0->1 transition of bit [2]. While set, the other bits in this register are not valid and it is illegal for SW to write to any bit in this register. When clear all the other bits in the register are valid and SW may write to any bit. If Interrupt Request bit [1] was set for the current command, HW may clear this bit before the interrupt has been made visible to SW, since when SW actually handles

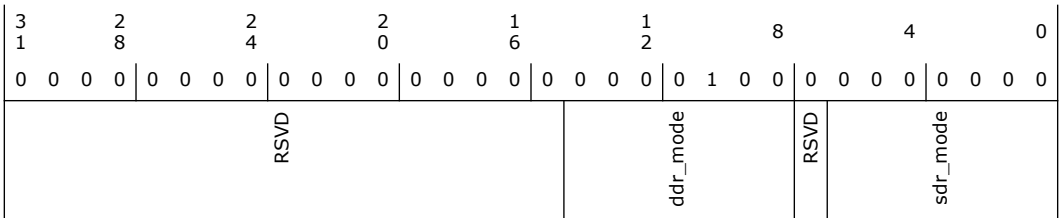
13.3.7 (Tx_CMD_dly)—Offset 820h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 4

Default: 400h



Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RO	Reserved.
14:8	4h RW	**ddr_mode:** Tx CMD Delay (DDR Mode). 0 - 39: Select number of active delay elements. Each = 125pSec. 40 - 127: Reserved
7	0h RO	Reserved.
6:0	0h RW	**sdr_mode:** Tx CMD Delay (SDR Mode). 0 - 39: Select number of active delay elements. Each = 125pSec. 40 - 127 - Reserved

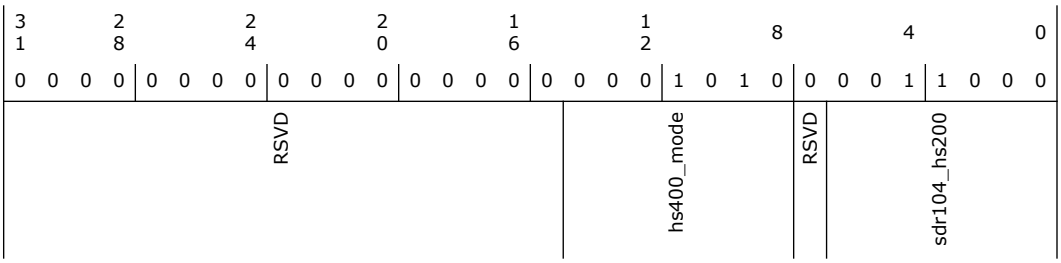
13.3.8 (Tx_DATA_dly_1)—Offset 824h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 4

Default: A18h



Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RO	Reserved.
14:8	Ah RW	**hs400_mode:** Tx Data Delay (HS400 Mode). 0 - 78: Select number of active delay elements. Each = 125pSec. 79 - 127: Reserved
7	0h RO	Reserved.
6:0	18h RW	**sdr104_hs200:** Tx Data Delay (SDR104/HS200 Mode) 0-79: Select the required delay, as a multiple of 125pSec. 80 - 127: Reserved

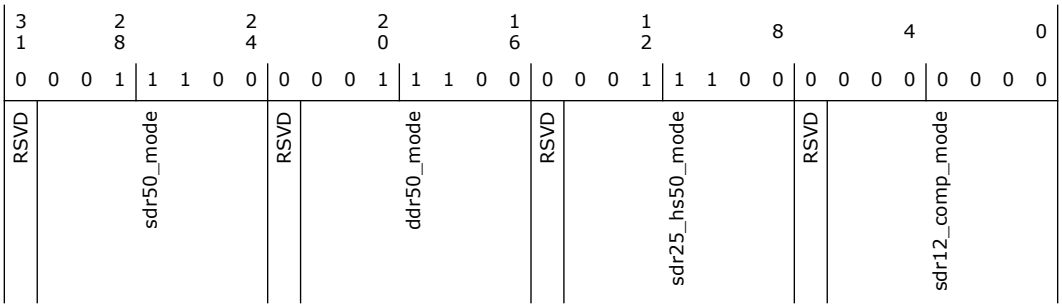
13.3.9 (Tx_DATA_dly_2)—Offset 828h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 4

Default: 1C1C1C00h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	Reserved.
30:24	1Ch RW	**sdr50_mode:** Tx Data Delay (SDR50 Mode) 0 - 79: Select the required delay, as a multiple of 125pSec. 80 - 127: Reserved
23	0h RO	Reserved.
22:16	1Ch RW	**ddr50_mode:** Tx Data Delay (DDR50 Mode). 0 - 78: Select number of active delay elements. Each = 125pSec. 79 - 127: Reserved
15	0h RO	Reserved.
14:8	1Ch RW	**sdr25_hs50_mode:** Tx Data Delay (SDR25/HS50 Mode) 0 - 79: Select the required delay, as a multiple of 125pSec. 80 - 127: Reserved
7	0h RO	Reserved.
6:0	0h RW	**sdr12_comp_mode:** Tx Data Delay (SDR12/Compatibility Mode) 0 - 79: Select the required delay, as a multiple of 125pSec. 80 - 127: Reserved

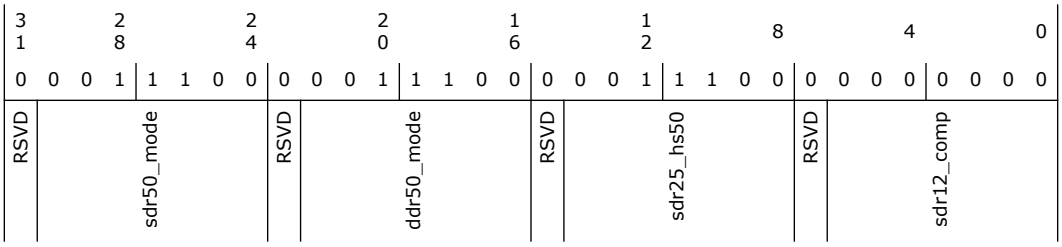
13.3.10 (Rx_CMD_Data_dly_1)—Offset 82Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 4

Default: 1C1C1C00h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	Reserved.
30:24	1Ch RW	**sdr50_mode:** Rx CMD + Data Delay (SDR50 Mode). 0 – 79: Select the required delay, as a multiple of 125pSec. 80 –127: Reserved
23	0h RO	Reserved.
22:16	1Ch RW	**ddr50_mode:** Rx CMD + Data Delay (DDR50 Mode). 0-78: Select number of active delay elements. Each = 125 pSec. 79-127: Reserved
15	0h RO	Reserved.
14:8	1Ch RW	**sdr25_hs50:** Rx CMD + Data Delay (SDR25/HS50 Mode) 0-79: Select the required delay, as a multiple of 125 pSec. 80-127: Reserved
7	0h RO	Reserved.
6:0	0h RW	**sdr12_comp:** Rx CMD + Data Delay (SDR12/Compatibility Mode) 0-79: Select the required delay, as a multiple of 125 pSec. 80-127: Reserved

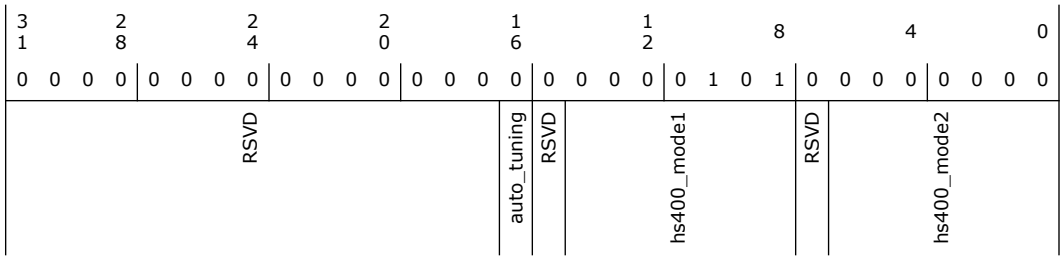
13.3.11 (Rx_Strobe_Ctrl_Path)—Offset 830h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 4

Default: 500h



Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	Reserved.
16	0h RW	**auto_tuning:** Enable Auto Tuning for HS400 Strobe Path. 0: Auto Tuning Disabled 1: Auto Tuning Enabled
15	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
14:8	5h RW	**hs400_mode1:** Rx Strobe Delay DLL 1(HS400 Mode). 0-39: Select number of active delay elements. Each = 125 pSec. 0-63: Reserved
7	0h RO	Reserved.
6:0	0h RW	**hs400_mode2:** Rx Strobe Delay DLL 2(HS400 Mode). 0-39: Select number of active delay elements. Each = 125 pSec. 40-63: Reserved

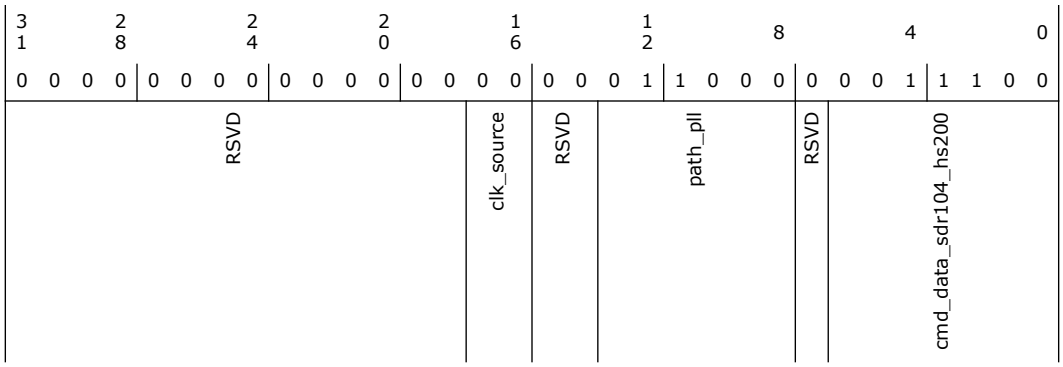
13.3.12 (Rx_CMD_Data_dly_2)—Offset 834h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 4

Default: 181Ch



Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17:16	0h RW	**clk_source:** Clock Source for Rx Path. 00: Rx Clock after Output Buffer 01: Rx Clock before Output Buffer 10: Automatic Selection based on Working mode (HS 200 before buffer, all others after buffer) 11 - Reserved
15:14	0h RO	Reserved.
13:8	18h RW	**path_pll:** Rx Path PLL #3 Delay value For Auto Tuning Mode. 0-39: Select the required delay, as a multiple of 125 pSec. 40-63: Reserved
7	0h RO	Reserved.
6:0	1Ch RW	**cmd_data_sdr104_hs200:** Rx CMD + Data Delay (SDR104/HS200 Mode). 0-79: Select the required delay, as a multiple of 125 pSec. 80-127: Reserved

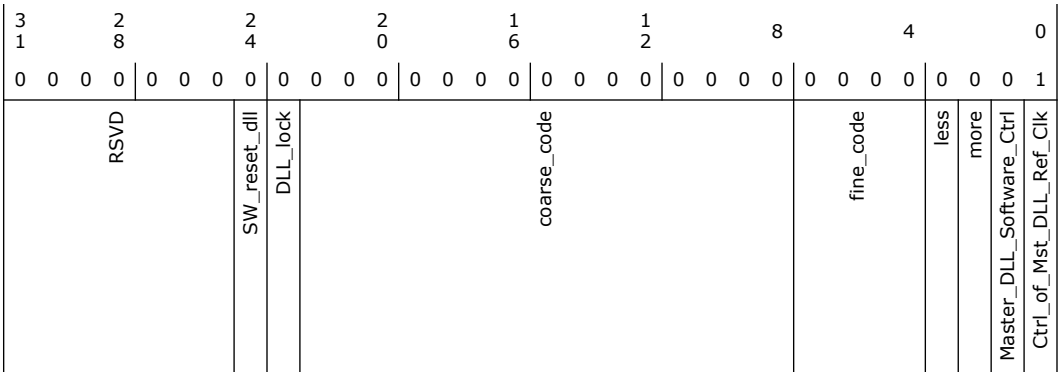
13.3.13 (Master_Dll)—Offset 838h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 4

Default: 1h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	Reserved.
24	0h RO	**SW_reset_dll:** SW reset for Master DLL 0: No SW Reset for Master DLL 1: Force Reset for Master DLL
23	0h RO	**DLL_lock:** Master DLL Lock Indication
22:8	0h RW	**coarse_code:** Set coarse code to DLL. (only valid when Software control is Enabled)
7:4	0h RW	**fine_code:** Set fine code to DLL. (only valid when Software control is Enabled)
3	0h RO/V	**less:** Phase Detection Less Indication
2	0h RO/V	**more:** Phase Detector More Indication
1	0h RW	**Master_DLL_Software_Ctrl:** Master DLL Software Ctrl. 0: Master DLL Automatic Control (SW Control Disabled). 1: Master DLL Software Control Enabled
0	1h RW	**Ctrl_of_Mst_DLL_Ref_Clk:** Ctrl of Master DLL Ref Clock. 0: Clock is Disabled. 1: Clock is Enabled

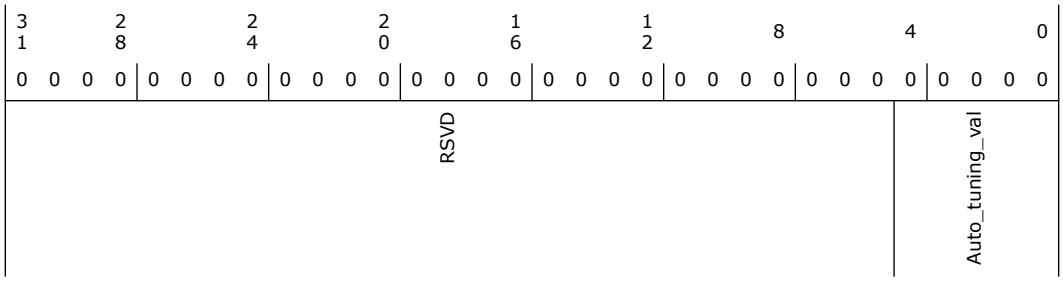
13.3.14 (Auto_tuning)—Offset 840h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 4

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4:0	0h RO	**Auto_tuning_val**

§ §

14 SDXC (D30:F6)

14.1 SDXC PCI Configuration Registers Summary

Table 14-1. Summary of SDXC PCI Configuration Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	Device & Vendor ID (DEVVENDID)—Offset 0h	9D2D8086h
4h	7h	PCI Status & Command (STATUSCOMMAND)—Offset 4h	100000h
8h	Bh	Rev ID & Class Code (REVCLASSCODE)—Offset 8h	80501XXh
Ch	Fh	Cache Line & Latency & Header Type & BIST (CLLATHEADERBIST)—Offset Ch	800000h
10h	13h	Base Address Low (BAR0)—Offset 10h	4h
14h	17h	Base Address Register high (BAR0_HIGH)—Offset 14h	0h
18h	1Bh	Base Address Register1 (BAR1)—Offset 18h	4h
1Ch	1Fh	(BAR1_HIGH)—Offset 1Ch	0h
2Ch	2Fh	Subsystem Vendor ID (SUBSYSTEMID)—Offset 2Ch	0h
30h	33h	(EXPANSION_ROM_BASEADDR)—Offset 30h	0h
34h	37h	Capabilities Pointer (CAPABILITYPTR)—Offset 34h	80h
3Ch	3Fh	(INTERRUPTREG)—Offset 3Ch	100h
80h	83h	Power Management Capability ID Register (POWERCAPID)—Offset 80h	39001h
84h	87h	Power Management Control and Status Register (PMECTRLSTATUS)—Offset 84h	8h
90h	93h	(PCIDEVIDLE_CAP_RECORD)—Offset 90h	F0140009h
94h	97h	(DEVID_VEND_SPECIFIC_REG)—Offset 94h	1400010h
98h	9Bh	SW LTR update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG)—Offset 98h	8041h
9Ch	9Fh	Device IDLE Pointer Register (DEVICE_IDLE_POINTER_REG)—Offset 9Ch	81C1h
A0h	A3h	DOI3 Max Power & PG Config (D0I3_MAX_POW_LAT_PG_CONFIG)—Offset A0h	90800h
B0h	B3h	General Purpose PCI RW Register1 (GEN_REGRW1)—Offset B0h	0h
B4h	B7h	General Purpose PCI RW Register2 (GEN_REGRW2)—Offset B4h	0h
B8h	BBh	General Purpose PCI RW Register3 (GEN_REGRW3)—Offset B8h	0h
BCh	BFh	General Purpose PCI RW Register4 (GEN_REGRW4)—Offset BCh	0h
C0h	C3h	General Input Register (GEN_INPUT_REG)—Offset C0h	0h

14.1.1 Device & Vendor ID (DEVVENDID)—Offset 0h

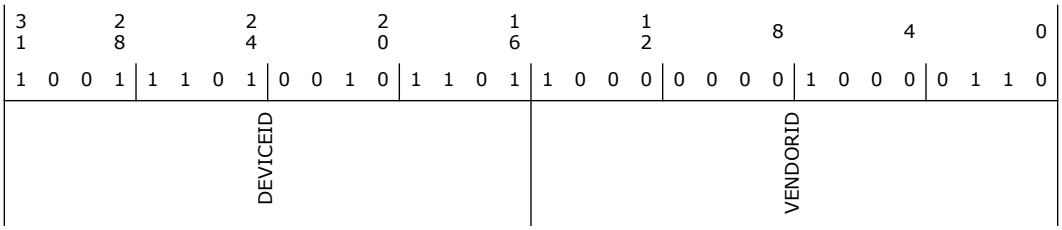
DEVICEVENDORID - Device ID and Vendor ID Register

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 6

Default: 9D2D8086h



Bit Range	Default & Access	Field Name (ID): Description
31:16	9D2Dh RO	**Device ID (DEVICEID):** Identifies the device.
15:0	8086h RO	**Vendor ID (VENDORID):** Intel default value is 8086h

14.1.2 PCI Status & Command (STATUSCOMMAND)—Offset 4h

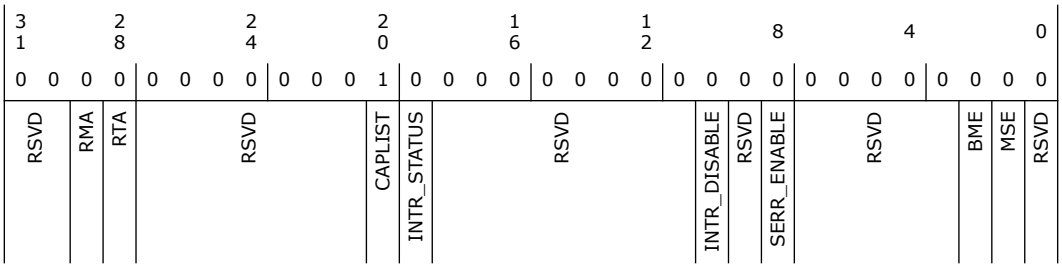
STATUSCOMMAND- Status and Command

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 6

Default: 100000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29	0h RW/1C	**Received Master Abort (RMA):** The software writes a 1 to this bit to clear it.
28	0h RW/1C	**Received Target Abort (RTA):** The software writes a 1 to this bit to clear it.
27:21	0h RO	Reserved.
20	1h RO	**Capabilities List (CAPLIST):** Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at the configuration offset 34h.

Bit Range	Default & Access	Field Name (ID): Description
19	0h RO	**Interrupt Status (INTR_STATUS):** This bit reflects state of interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, is the device/function interrupt message sent.
18:11	0h RO	Reserved.
10	0h RW	**Interrupt Disable (INTR_DISABLE):** Setting this bit disables INTx assertion.
9	0h RO	Reserved.
8	0h RW	**SERR_ENABLE**
7:3	0h RO	Reserved.
2	0h RW	**Bus Master Enable (BME):** 0 = the Bridge does not generate any new upstream transaction on IOSF as a master. Reset value of this bit is 0.
1	0h RW	**Memory Space Enable (MSE):** MSE is part of the Type PCI configuration space each device has. When disabled no downstream traffic from the bridge is available.
0	0h RO	Reserved.

14.1.3 Rev ID & Class Code (REVCLASSCODE)—Offset 8h

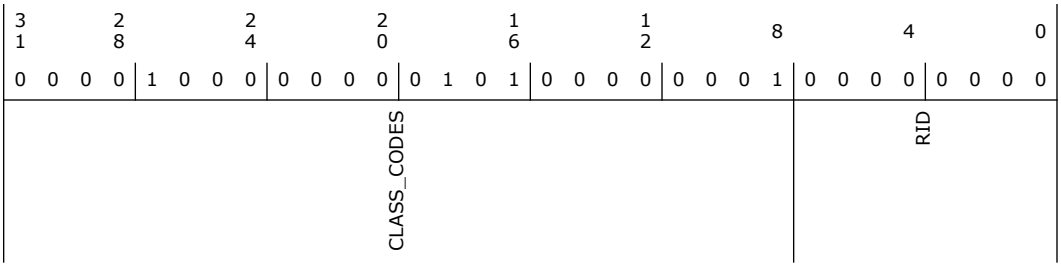
REVCLASSCODE - Revision ID and Class Code

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 6

Default: 80501xxh



Bit Range	Default & Access	Field Name (ID): Description
31:8	80501h RO	**Class Code (CLASS_CODES):** The Class Code register is read-only and is used to identify the generic function of the device, and in some cases, a specific register-level programming interface. The register is broken into 3 Byte-size fields. - The upper Byte (at offset 0Bh) is a base class code that broadly classifies the type of function the device performs. - The middle Byte (at offset 0Ah) is a sub-class code that identifies more specifically the function of the device. - The lower Byte (at offset 09h) identifies a specific register-level programming interface (if any) so that device independent software can interact with the device. This register is tied to a strap at the top level.
7:0	0h RO	**Rev ID (RID):** Revision ID identifies the revision of particular PCI device. See the Device and Version ID Table in Volume 1 for the default value.

14.1.4 Cache Line & Latency & Header Type & BIST (CLLATHEADERBIST)—Offset Ch

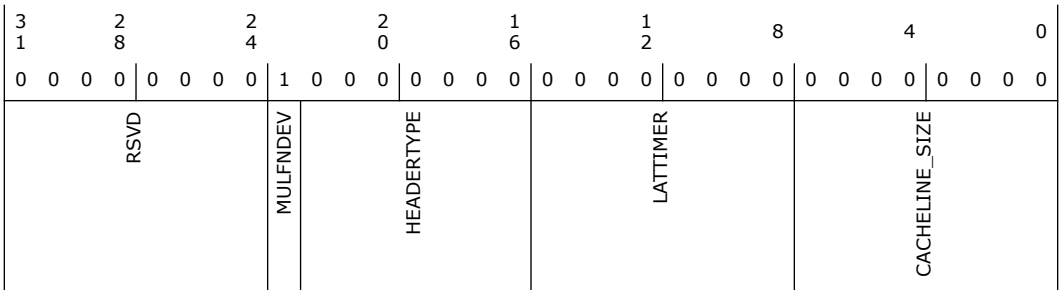
CLLATHEADERBIST - Cache Line Latency Header and BIST

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 6

Default: 800000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	1h RO	**Multi-Function Device (MULFNDEV):** This bit is 0 or 1 depending upon the value assigned o the top level strap
22:16	0h RO	**Header Type (HEADERTYPE):** Implements Type 0 Configuration header.
15:8	0h RO	**Latency Timer (LATTIMER):** This register is implemented as R/W with default as 0.
7:0	0h RW	**Cacheline Size (CACHELINE_SIZE):** This register is implemented as R/W with default as 0.

14.1.5 Base Address Low (BAR0)—Offset 10h

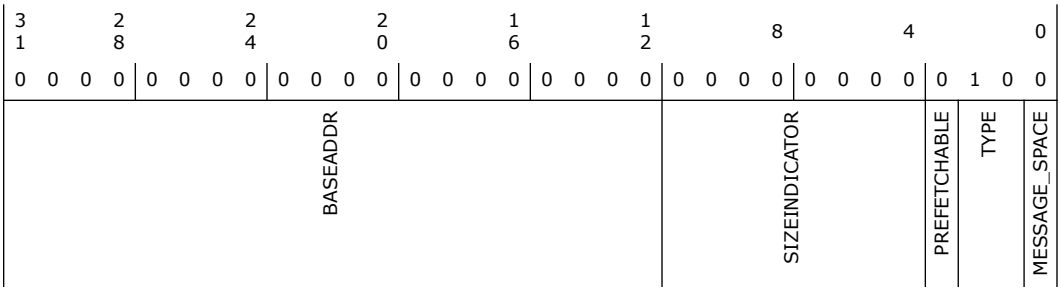
BAR -Base Address Register

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 6

Default: 4h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW	**BARL (BASEADDR):** Base address of the OCP fabric memory space.
11:4	0h RO	**Size Indicator (SIZEINDICATOR):** Size Indicator Read Only. The size of this register depends on the size of the memory space.
3	0h RO	**Prefetchable (PREFETCHABLE):** Indicates that this BAR is not prefetchable.
2:1	2h RO	**TYPE:** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range. If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE):** 0 indicates this BAR is present in the memory space.

14.1.6 Base Address Register high (BAR0_HIGH)—Offset 14h

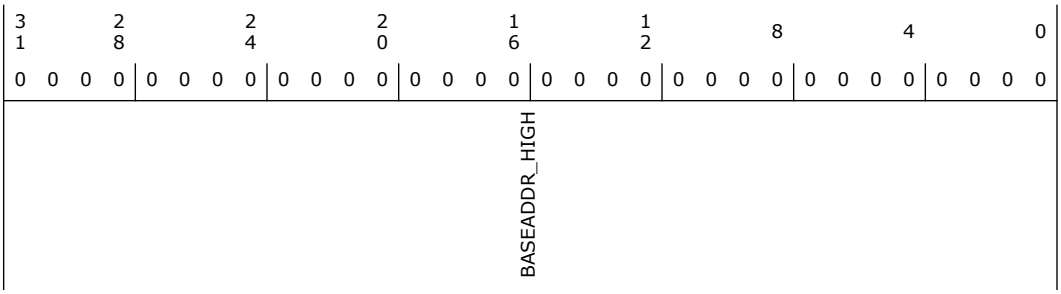
BAR -Base Address Register High

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 6

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**BARH (BASEADDR_HIGH):** Base address of the OCP fabric memory space.

14.1.7 Base Address Register1 (BAR1)—Offset 18h

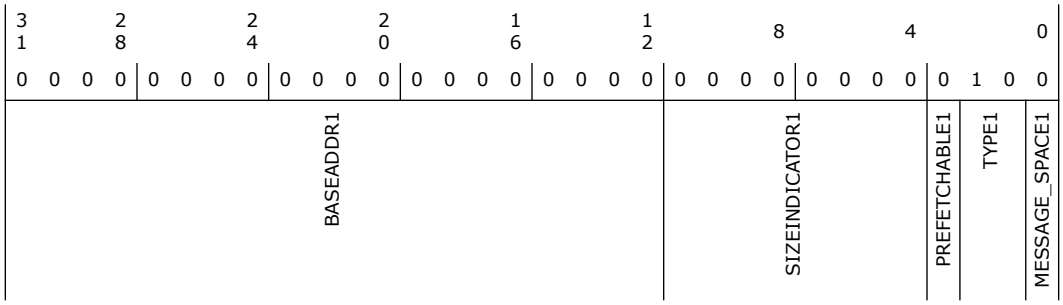
BAR1 -Base Address Register1

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 6

Default: 4h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW	**Base Address Register1 (BASEADDR1):** This field is present if BAR1 is enabled through private configuration space.
11:4	0h RO	**SIZEBAR1 (SIZEINDICATOR1):** Always is 0 as minimum size is 4K
3	0h RO	**Prefetchable (PREFETCHABLE1):** Indicates that this BAR is not prefetchable.
2:1	2h RO	**TYPE (TYPE1):** Always 0 as minimum size is 4K
0	0h RO	**Base Address Register1 (MESSAGE_SPACE1):** This field is present if BAR1 is enabled through private configuration space.

14.1.8 (BAR1_HIGH)—Offset 1Ch

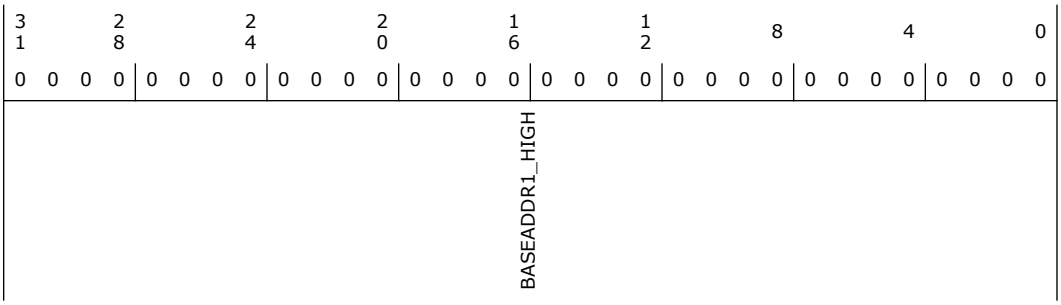
BAR1 -Base Address Register1 High

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 6

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**BASEADDR1_HIGH:** Base address of the OCP fabric memory space.

14.1.9 Subsystem Vendor ID (SUBSYSTEMID)—Offset 2Ch

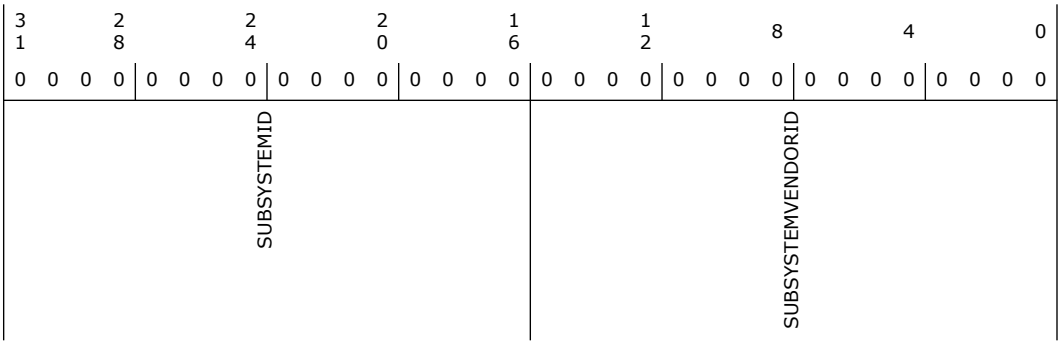
SUBSYSTEMID -Subsystem Vendor and Subsystem ID

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 6

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW/O	**SUBSYSTEMID**
15:0	0h RW/O	**SUBSYSTEMVENDORID**

14.1.10 (EXPANSION_ROM_BASEADDR)—Offset 30h

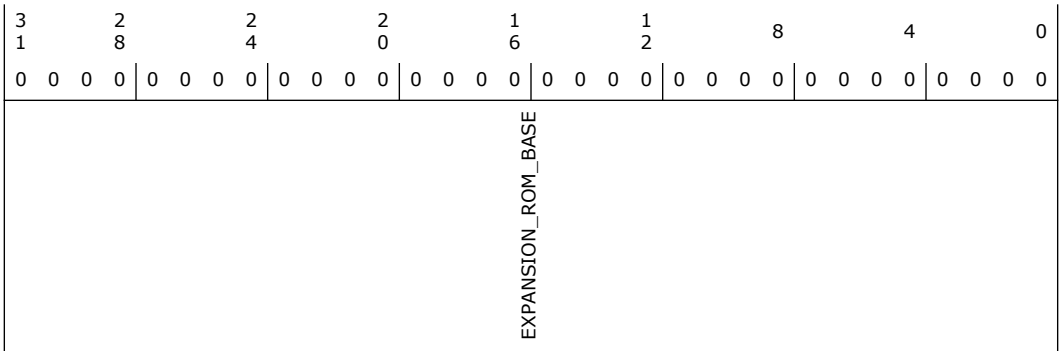
EXPANSION ROM base address

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 6

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**EXPANSION_ROM_BASE:** Value of all zeros indicates no support for Expansion ROM.

14.1.11 Capabilities Pointer (CAPABILITYPTR)—Offset 34h

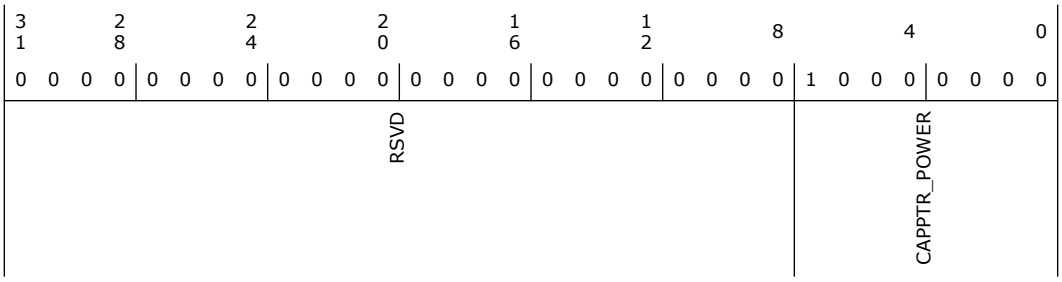
CAPABILITYPTR - Capabilities Pointer

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 6

Default: 80h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	80h RO	**CAPPTR_POWER**

14.1.12 (INTERRUPTREG)—Offset 3Ch

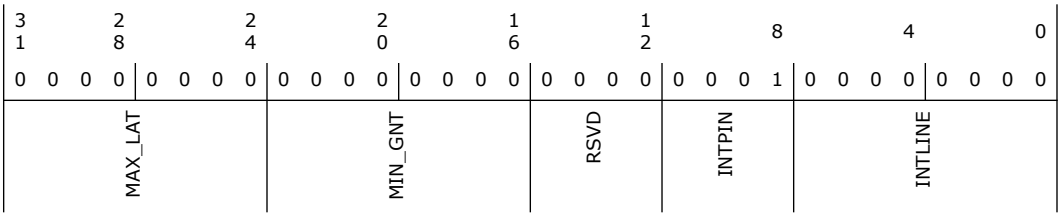
INTERRUPTREG - Interrupt Register

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 6

Default: 100h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Maximum Latency (MAX_LAT):** Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	0h RO	**MIN_GNT:**
15:12	0h RO	Reserved.
11:8	1h RO	**Interrupt Pin (INTPIN):** Interrupt Pin Value in this register is reflected from the IPIN value in the private configuration space. For a single function device, this ideally is INTA.
7:0	0h RW	**Interrupt Line (INTLINE):** It is used to communicate to software, the interrupt line to which the interrupt pin is connected.

14.1.13 Power Management Capability ID Register (POWERCAPID)—Offset 80h

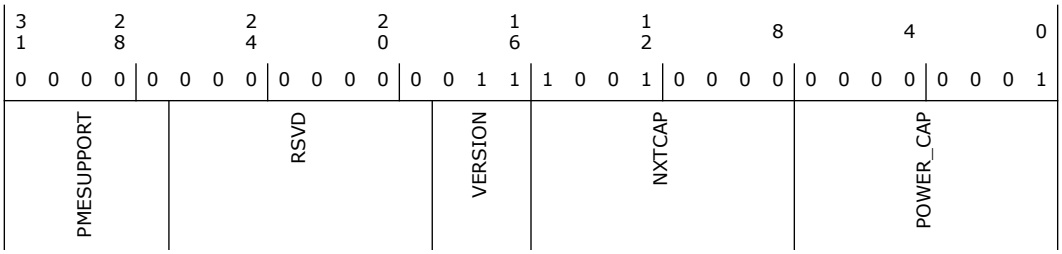
POWERCAPID - PowerManagement Capability ID

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 6

Default: 39001h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**PME_Support (PMESUPPORT):** This 5-bit field indicates the power states in which the function can assert the PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal in that power state. bit 27 = 1: PME# can be asserted from D0 bit28 = 1: PME# can be asserted from D1. bit 29 = 1: PME# can be asserted from D2. bit30 = 1:PME# can be asserted from D3hot bit 31 = 1:PME# can be asserted from D3cold.
26:19	0h RO	Reserved.
18:16	3h RO	**Version (VERSION):** Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	90h RO	**Next Capability (NXTCAP):** Points to the next capability structure. This points to NULL if either ENABLE_PCI_IDLE_CAP is 0 or if Disable PCI Device Idle capability bit is set as 1 in the private space. Else this points to PCI Device Idle capability structure at offset 90h
7:0	1h RO	**Power Management Capability (POWER_CAP):** Indicates this is power management capability.

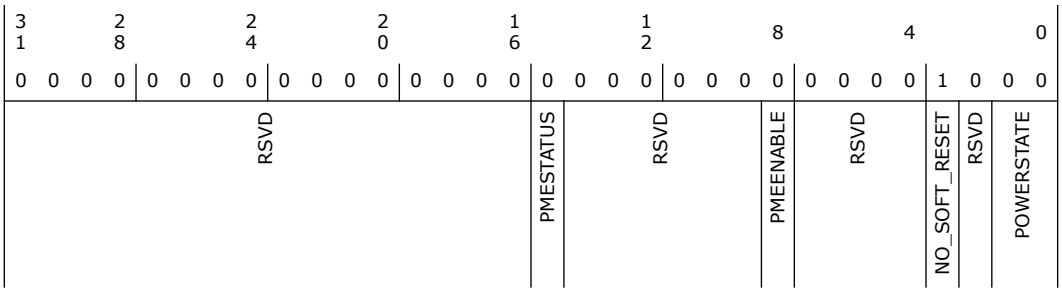
14.1.14 Power Management Control and Status Register (PMECTRLSTATUS)—Offset 84h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 6

Default: 8h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	0h RW/1C	**PME Status (PMESTATUS):** 0: Software clears the bit by writing a 1 to it. 1: This bit is set when the PME# signal is asserted independent of the state of the PME Enable bit (bit 8 in this register)
14:9	0h RO	Reserved.
8	0h RW	**PME Enable (PMEENABLE):** 1: Enables the function to assert PME#. 0: PME# message on Sideband is disabled.
7:4	0h RO	Reserved.
3	1h RO	**NO_SOFT_RESET:** This bit indicates that devices transitioning from D3hot to D0 because of Powerstate commands do not perform an internal reset. Configuration Context is preserved.
2	0h RO	Reserved.
1:0	0h RW	**Power State (POWERSTATE):** This field is used both to determine the current power state and to set a new power state. The values are: 00 D0 state 11 D3HOT state

14.1.15 (PCIDEVIDLE_CAP_RECORD)—Offset 90h

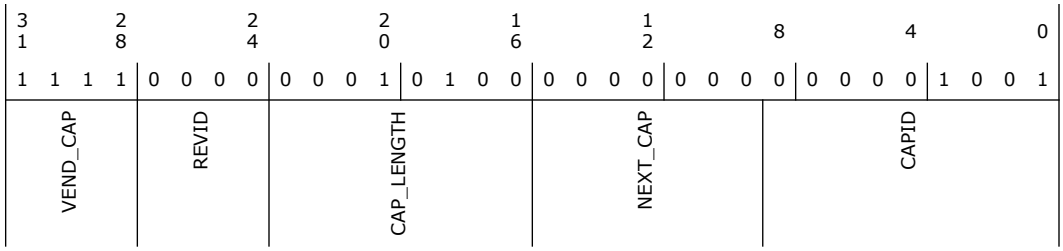
PCI DEVICE IDLE CAPABILITY RECORD

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 6

Default: F0140009h



Bit Range	Default & Access	Field Name (ID): Description
31:28	Fh RO	**Vendor ID (VEND_CAP):** Indicates this is Vendor Specific capability.
27:24	0h RO	**REVID:** Revision ID of capability structure.

Bit Range	Default & Access	Field Name (ID): Description
23:16	14h RO	**Length (CAP_LENGTH):** Indicates the number of bytes in the capability structure.
15:9	0h RO	**Next Capability (NEXT_CAP):** Points to the next capability structure. This points to NULL.
8:0	9h RO	**Capability ID (CAPID):**

14.1.16 (DEVID_VEND_SPECIFIC_REG)—Offset 94h

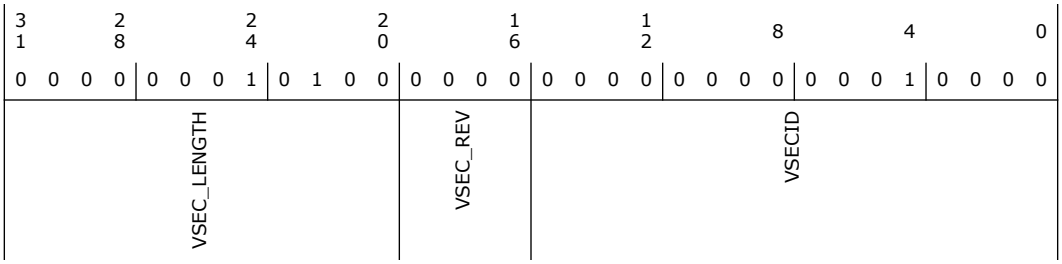
DEVID VENDOR SPECIFIC REG

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 6

Default: 1400010h



Bit Range	Default & Access	Field Name (ID): Description
31:20	14h RO	**VSEC Length (VSEC_LENGTH):** Vendor Specific Capability Length.
19:16	0h RO	**Vendor Revision (VSEC_REV):** Vendor specific revision.
15:0	10h RO	**Vendor ID (VSECID):** Vendor specific ID.

14.1.17 SW LTR update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG)—Offset 98h

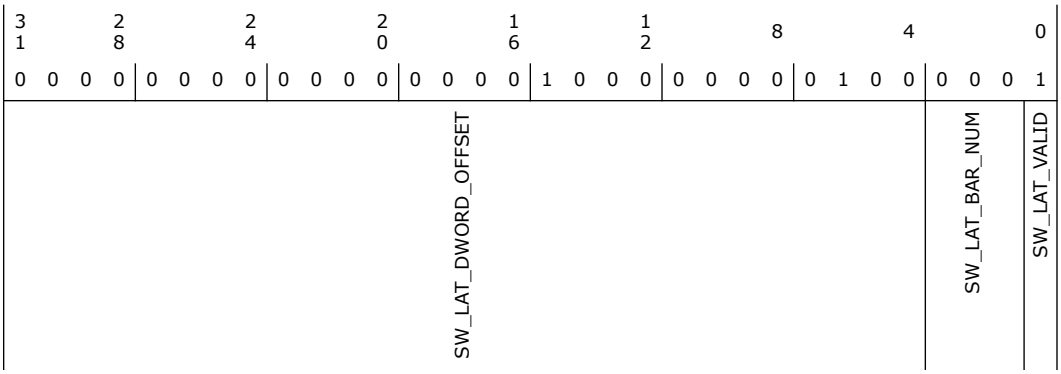
SW LTR Update MMIO Location Register

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 6

Default: 8041h



Bit Range	Default & Access	Field Name (ID): Description
31:4	804h RO	**SWLTRLOC (SW_LAT_DWORD_OFFSET):** This register contains the location pointer to the SW LTR register in MMIO space, as an offset from the specified BAR.
3:1	0h RO	**BAR NUM (SW_LAT_BAR_NUM):** Indicates that the SW LTR update MMIO location is always at BAR0.
0	1h RO	**SW_LAT_VALID:** This value is reflected from the SW LTR valid strap at the top level.

14.1.18 Device IDLE Pointer Register (DEVICE_IDLE_POINTER_REG)—Offset 9Ch

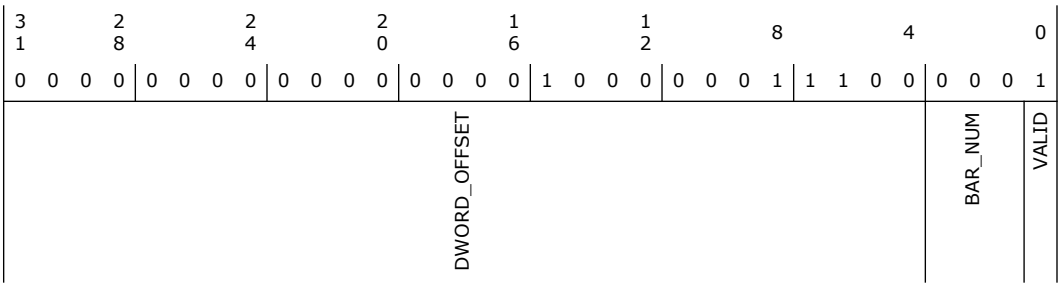
Device IDLE pointer register

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 6

Default: 81C1h



Bit Range	Default & Access	Field Name (ID): Description
31:4	81Ch RO	**DWORD_OFFSET:** This register contains the location pointer to the SW LTR register in MMIO space, as an offset from the specified BAR.
3:1	0h RO	**BAR_NUM:** Indicates that the D0i3 MMIO location is always at BAR0.
0	1h RO	**VALID:**

14.1.19 D0I3 Max Power & PG Config (D0I3_MAX_POW_LAT_PG_CONFIG)—Offset A0h

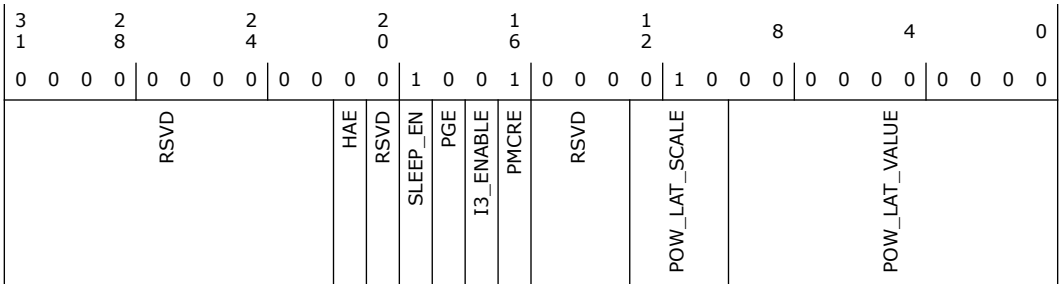
DEVICE PG CONFIG

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 6

Default: 90800h



Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	Reserved.
21	0h RW	**Hardware Autonomous Enable (HAE):** If set, then the PGCB may request a PG whenever it is idle.
20	0h RO	Reserved.
19	1h RW	**SLEEP_EN:** if clear, then IP will never asset Sleep to the retention flops. If set, then IP may assert Sleep during PG'ing.
18	0h RW	**PG Enable (PGE):** If clear, then IP will never request a PG. If set, then IP may request PG when proper conditions are met.
17	0h RW	**I3_ENABLE:** if set, then IP will PG when idle and the D0i3 register (in PGCB) is set. If this bit is set, the IP will not PG unless the IPs D0i3 control bit ='1'. Bit [5] is not required to be set when this bit is set.
16	1h RW	**PMC Request Enable (PMCRE):** When bits [1:0] = '11', power gating is enabled whenever either the D3 register or the D0i3 register is set.

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO	Reserved.
12:10	2h RW	**Power On Latency Scale (POW_LAT_SCALE):** Support for codes 010 (1us) or 011 (32us) for Exit Latency Scale (1us -) 32ms total span) only.
9:0	0h RW	**Power On Latency value (POW_LAT_VALUE):** This value is written by BIOS to communicate to the Driver.

14.1.20 General Purpose PCI RW Register1 (GEN_REGRW1)—Offset B0h

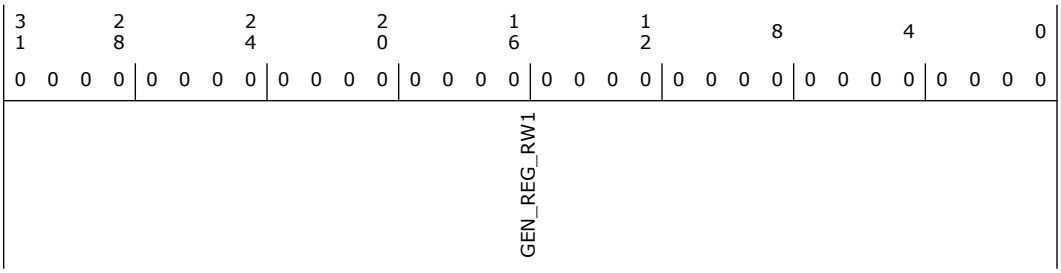
General Purpose Read Write Register1

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 6

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**GEN_REG_RW1**

14.1.21 General Purpose PCI RW Register2 (GEN_REGRW2)—Offset B4h

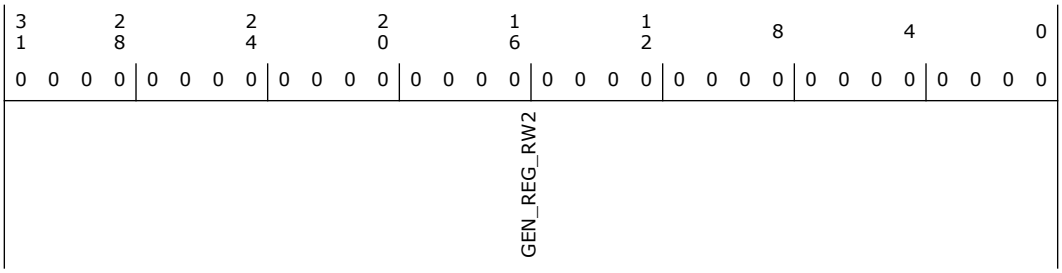
General Purpose Read Write Register2

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 6

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**GEN_REG_RW2**

14.1.22 General Purpose PCI RW Register3 (GEN_REGRW3)—Offset B8h

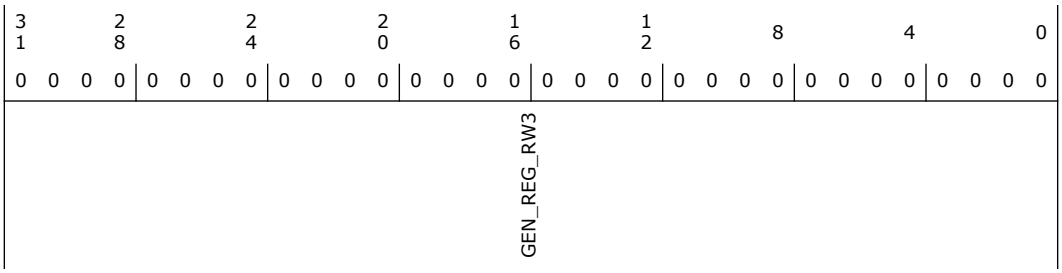
General Purpose Read Write Register3

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 6

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**GEN_REG_RW3**

14.1.23 General Purpose PCI RW Register4 (GEN_REGRW4)—Offset BCh

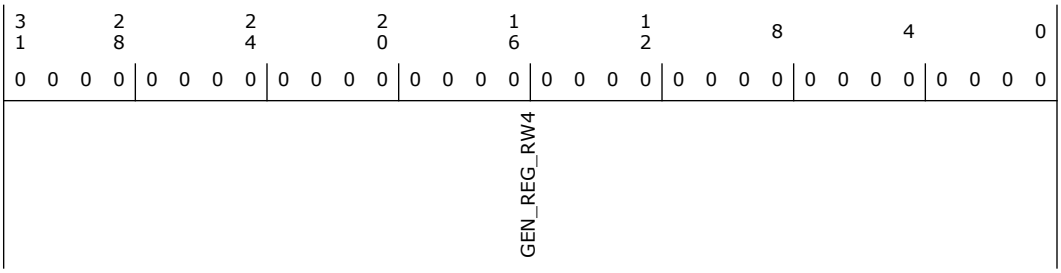
General Purpose Read Write Register4

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 6

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**GEN_REG_RW4**

14.1.24 General Input Register (GEN_INPUT_REG)—Offset C0h

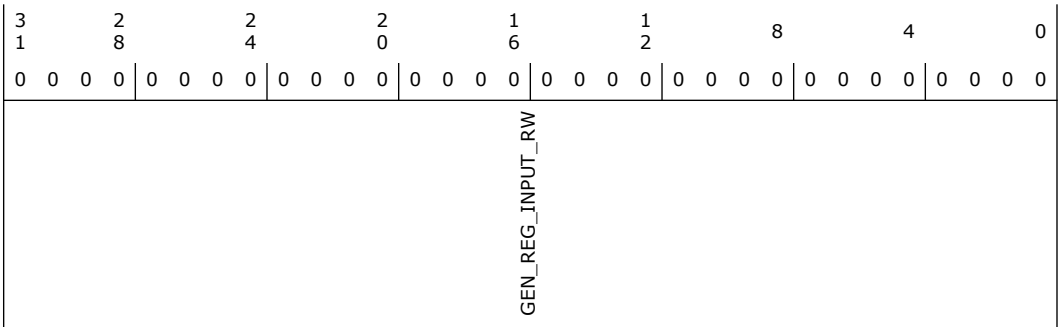
General Purpose Input Register

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 6

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**GEN_REG_INPUT_RW**

14.2 SDXC Memory Mapped Registers Summary

These registers are memory mapped based on BAR0 defined in PCI configuration space.

Table 14-2. Summary of SDXC Memory Mapped Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	SDMA System Address Register/Argument2 Register (sdmasysaddr)—Offset 0h	0h
4h	5h	Block Size Register (blocksize)—Offset 4h	0h
6h	7h	Block Count Register (blockcount)—Offset 6h	0h
8h	Bh	Argument1 Register (argument1)—Offset 8h	0h
Ch	Dh	Transfer Mode Register (transfermode)—Offset Ch	0h
Eh	Fh	Command Register (command)—Offset Eh	0h
10h	13h	Response Register (Response 0)—Offset 10h	0h
20h	23h	Buffer Data Port Register (dataport)—Offset 20h	0h
24h	27h	Present State Register (presentstate)—Offset 24h	0h
28h	28h	Host Control1 Register (hostcontrol1)—Offset 28h	0h
29h	29h	PowerControl Register (powercontrol)—Offset 29h	0h
2Ah	2Ah	Block Gap Control Register (blockgapcontrol)—Offset 2Ah	80h
2Bh	2Bh	Wakeup Control Register (wakeupcontrol)—Offset 2Bh	0h
2Ch	2Dh	Clock Control Register (clockcontrol)—Offset 2Ch	0h
2Eh	2Eh	Timeout Control Register (timeoutcontrol)—Offset 2Eh	0h
2Fh	2Fh	Software Reset Register (softwarereset)—Offset 2Fh	0h
30h	31h	Normal Interrupt Status Register (normalintrsts)—Offset 30h	0h
32h	33h	Error Interrupt Status (errorintrsts)—Offset 32h	0h
34h	35h	Normal Interrupt Status Enable Register (normalintrstsena)—Offset 34h	0h
36h	37h	Error Interrupt Status Enable Register (errorintrstsena)—Offset 36h	0h
38h	39h	Normal Interrupt Signal Enable Register (normalintrsigena)—Offset 38h	0h
3Ah	3Bh	Error Interrupt Signal Enable Register (errorintrsigena)—Offset 3Ah	0h
3Ch	3Dh	Auto CMD12 Error Status Register (autocmderrsts)—Offset 3Ch	0h
3Eh	3Fh	Host Control 2 Register (hostcontrol2)—Offset 3Eh	0h
40h	47h	Capabilities Register (capabilities)—Offset 40h	0h
48h	4Fh	Maximum Current Capabilities Register (maxcurrentcap)—Offset 48h	0h
50h	51h	Force Event REGISTER for AUTO CMD Error Status (ForceEventforAUTOCMDErrorStatus)—Offset 50h	0h
52h	53h	Force Event Register for Error Interrupt Status (forceeventforerrintsts)—Offset 52h	0h
54h	54h	ADMA Error Status Register (admaerrsts)—Offset 54h	0h
58h	5Bh	ADMA System Address Register0&1 (admasysaddr01)—Offset 58h	0h
5Ch	5Dh	ADMA System Address Register1 (admasysaddr2)—Offset 5Ch	0h
5Eh	5Fh	ADMA System Address Register1 (admasysaddr3)—Offset 5Eh	0h
60h	61h	Preset Value Register for Initialization (Preset Value 0)—Offset 60h	3h

Table 14-2. Summary of SDXC Memory Mapped Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
62h	63h	Preset Value Register for Default Speed (Preset Value 1)—Offset 62h	0h
64h	65h	Preset Value Register for High Speed (presetvalue2)—Offset 64h	0h
66h	67h	Preset Value Register for SDR12 (presetvalue3)—Offset 66h	0h
68h	69h	Preset Value Register for SDR25 (presetvalue4)—Offset 68h	0h
6Ah	6Bh	Preset Value Register for SDR50 (presetvalue5)—Offset 6Ah	0h
6Ch	6Dh	Preset Value Register for SDR104 (presetvalue6)—Offset 6Ch	0h
6Eh	6Fh	Preset Value Register for DDR50 (presetvalue7)—Offset 6Eh	0h
FCh	FDh	Slot Interrupt Status Register (slotintrsts)—Offset FCh	0h
FEh	FFh	Host Controller Version Register (hostcontrollerver)—Offset FEh	1002h

14.2.1 SDMA System Address Register/Argument2 Register (sdmasysaddr)—Offset 0h

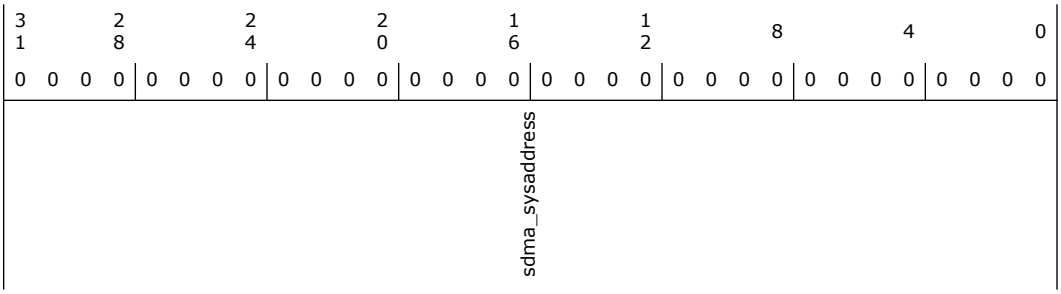
This register contains concatinates reg_sdmasysaddrlo and reg_sdmasysaddrhi

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 6

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h	**sdma_sysaddress (sdma_sysaddress):** refer to reg_sdmasysaddrlo and reg_sdmasysaddrhi

14.2.2 Block Size Register (blocksize)—Offset 4h

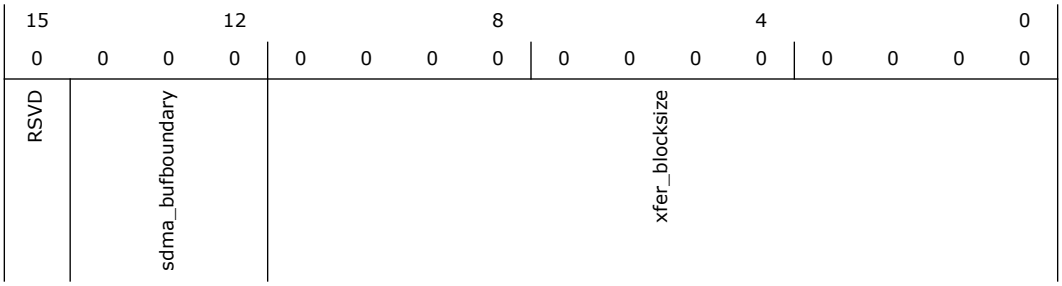
This register is used to configure the number of bytes in a data block

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 30
Function: 6

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	Reserved.
14:12	0h RW	**Host DMA Buffer Size (sdma_bufboundary):** To perform long DMA transfer, System Address register shall be updated at every system boundary during DMA transfer. These bits specify the size of contiguous buffer in the system memory. The DMA transfer shall wait at the every boundary specified by these fields and the HC generates the DMA Interrupt to request the HD to update the System Address register. These bits shall support when the DMA Support in the Capabilities register is set to 1 and this function is active when the DMA Enable in the Transfer Mode register is set to 1. 000b - 4KB(Detects A11 Carry out) 001b - 8KB(Detects A12 Carry out) 010b - 16KB(Detects A13 Carry out) 011b - 32KB(Detects A14 Carry out) 100b - 64KB(Detects A15 Carry out) 101b -128KB(Detects A16 Carry out) 110b - 256KB(Detects A17 Carry out) 111b - 512KB(Detects A18 Carry out)
11:0	0h RW	**Transfer Blocksize (xfer_blocksize):** This register specifies the block size for block data transfers for CMD17, CMD18, CMD24, CMD25, and CMD53. It can be accessed only if no transaction is executing (i.e after a transaction has stopped). Read operations during transfer return an invalid value and write operations shall be ignored. 0000h - No Data Transfer 0001h - 1 Byte 0002h - 2 Bytes 0003h - 3 Bytes 0004h - 4 Bytes --- --- 01FFh - 511 Bytes 0200h - 512 Bytes --- --- 0800h - 2048 Bytes

14.2.3 Block Count Register (blockcount)—Offset 6h

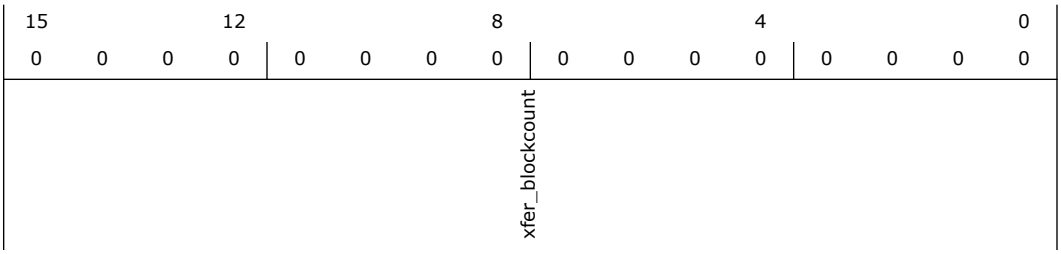
This register is used to configure the number of data blocks

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 30
Function: 6

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:0	0h	**xfer_blockcount (xfer_blockcount):** This register is enabled when Block Count Enable in the Transfer Mode register is set to 1 and is valid only for multiple block transfers. The HC decrements the block count after each block transfer and stops when the count reaches zero. It can be accessed only if no transaction is executing (i.e. after a transaction has stopped). Read operations during transfer return an invalid value and write operations shall be ignored. When saving transfer context as a result of Suspend command, the number of blocks yet to be transferred can be determined by reading this register. When restoring transfer context prior to issuing a Resume command, the HD shall restore the previously save block count. 0000h - Stop Count 0001h - 1 block 0002h - 2 blocks --- --- FFFFh - 65535 blocks

14.2.4 Argument1 Register (argument1)—Offset 8h

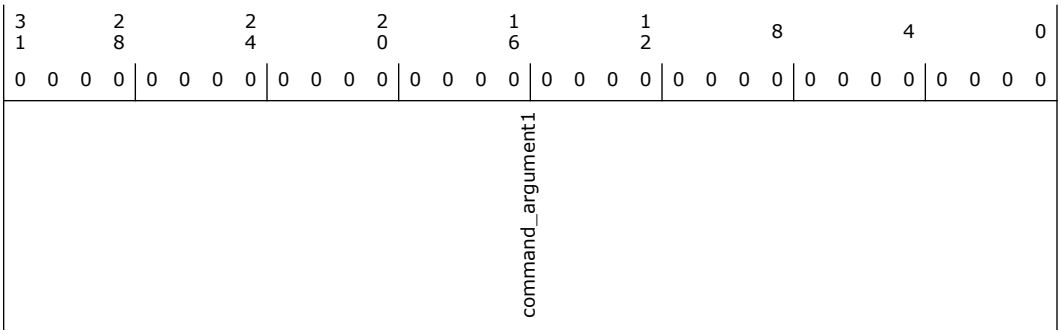
This register contains concatinates argument1lo and argument1hi registers to result SD Command Argument

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 6

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**command_argument1 (command_argument1):** The SD/eMMC Command Argument is specified as bit39-8 of Command-Format

14.2.5 Transfer Mode Register (transfermode)—Offset Ch

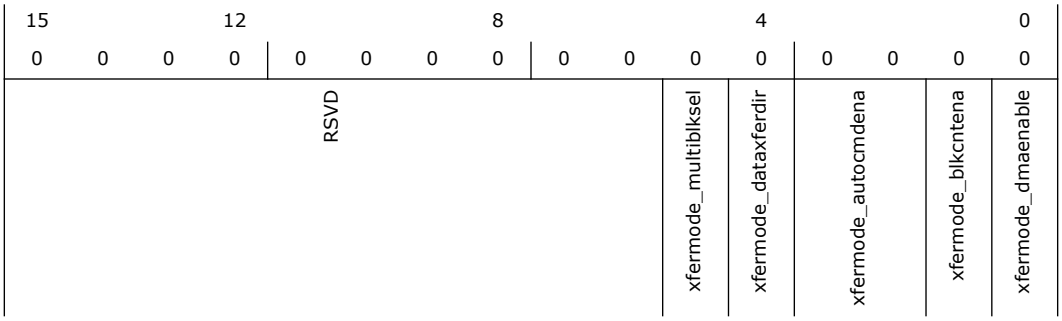
This register is used to control the operations of data transfers

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 30
Function: 6

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:6	0h RO	Reserved.
5	0h RW	**Multi / Single Block Select (xfermode_multiblksel):** This bit enables multiple block data transfers. 0 - Single Block 1 - Multiple Block.
4	0h RW	**Data Transfer Direction Select (xfermode_dataxferdir):** This bit defines the direction of data transfers. 0 - Write (Host to Card) 1 - Read (Card to Host)
3:2	0h RW	**Auto CMD Enable (xfermode_autocmdena):** This field determines use of auto command functions 00b - Auto Command Disabled 01b - Auto CMD12 Enable 10b - Auto CMD23 Enable 11b - Reserved
1	0h RW	**Block Count Enable (xfermode_blkcntena):** This bit is used to enable the Block count register, which is only relevant for multiple block transfers. When this bit is 0, the Block Count register is disabled, which is useful in executing an infinite transfer. 0 - Disable 1 - Enable
0	0h RW	**DMA Enable (xfermode_dmaenable):** DMA can be enabled only if DMA Support bit in the Capabilities register is set. If this bit is set to 1, a DMA operation shall begin when the HD writes to the upper byte of Command register (00Fh). 0 - Disable 1 - Enable

14.2.6 Command Register (command)—Offset Eh

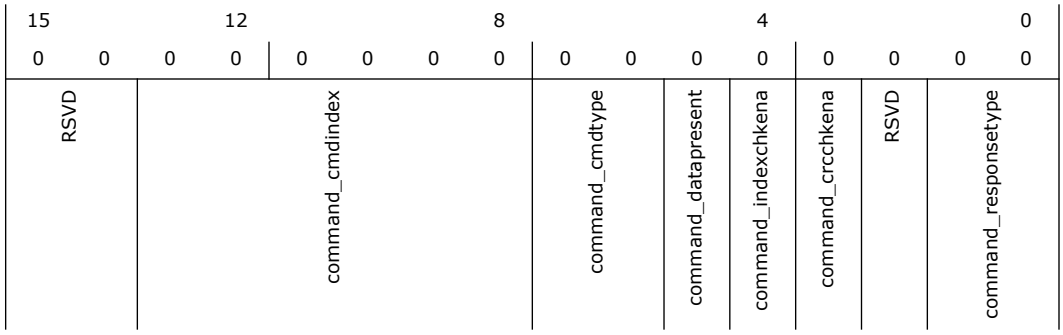
This register is used to program the Command for host controller

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 30
Function: 6

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RO	Reserved.
13:8	0h	**command_cmdindex (command_cmdindex):** This bit shall be set to the command number (CMD0-63, ACMD0-63).
7:6	0h RW	**Command Type (command_cmdtype):** There are three types of special commands. Suspend, Resume and Abort. These bits shall bet set to 00b for all other commands. Suspend Command If the Suspend command succeeds, the HC shall assume the SD Bus has been released and that it is possible to issue the next command which uses the DAT line. The host controller shall de-assert Read Wait for read transactions and stop checking busy for write transactions. The Interrupt cycle shall start, in 4-bit mode. If the Suspend command fails, the HC shall maintain its current state. and the HD shall restart the transfer by setting Continue Request in the Block Gap Control Register. Resume Command The HD re-starts the data transfer by restoring the registers in the range of 000-00Dh. The HC shall check for busy before starting write transfers. Abort Command If this command is set when executing a read transfer, the HC shall stop reads to the buffer. If this command is set when executing a write transfer, the HC shall stop driving the DAT line. After issuing the Abort command, the HD should issue a software reset 00b - Normal 01b - Suspend 10b - Resume 11b - Abort
5	0h RW	**Data Present Select (command_datapresent):** This bit is set to 1 to indicate that data is present and shall be transferred using the DAT line. If is set to 0 for the following: 1. Commands using only CMD line(ex. CMD52) 2. Commands with no data transfer but using busy signal on DAT[0] line (R1b or R5b ex. CMD38) 3. Resume Command 0 - No Data Present 1 - Data Present
4	0h RW	**Command Index Check Enable (command_indexchkena):** If this bit is set to 1, the HC shall check the index field in the response to see if it has the same value as the command index. If it is not, it is reported as a Command Index Error. If this bit is set to 0, the Index field is not checked. 0 - Disable 1 - Enable

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**Command CRC Check Enable (command_crcchkena):** If this bit is set to 1, the host controller shall check the CRC field in the response. If an error is detected, it is reported as a Command CRC Error. If this bit is set to 0, the CRC field is not checked. 0 - Disable 1 – Enable
2	0h RO	Reserved.
1:0	0h RW	**command_responsetype (command_responsetype):** Response Type Select: 00 - No Response 01 - Response length 136 10 - Response length 48 11 - Response length 48 check Busy after response

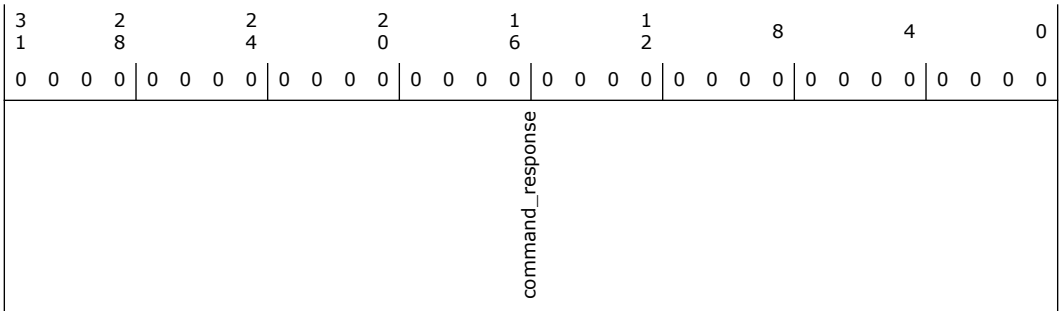
14.2.7 Response Register (Response 0)—Offset 10h

The response registers contains the 128 bit response received from the External Device.
The response registers are available at the following offset: Response Register 0: offset 0x010h
Response Register 1: offset 0x012h
Response Register 2: offset 0x014h
Response Register 3: offset 0x016h
Response Register 4: offset 0x018h
Response Register 5: offset 0x01Ah
Response Register 6: offset 0x01Ch
Response Register 7: offset 0x01Eh.

Access Method

Type: MEM Register (Size: 32 bits)
Device: 30
Function: 6

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h	**command_response (command_response):** R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit

14.2.8 Buffer Data Port Register (dataport)—Offset 20h

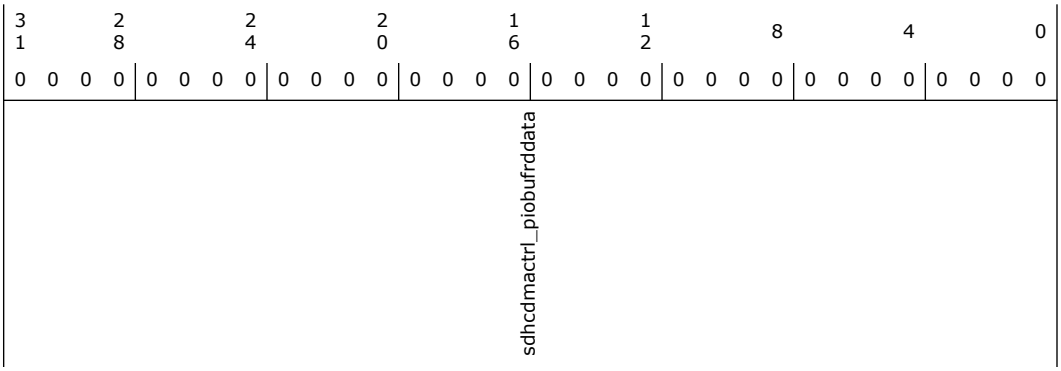
This register is used to access internal buffer

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 6

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**sdhcdmactrl_piobufrddata:** The Host Controller Buffer can be accessed through this 32-bit Data Port Register.

14.2.9 Present State Register (presentstate)—Offset 24h

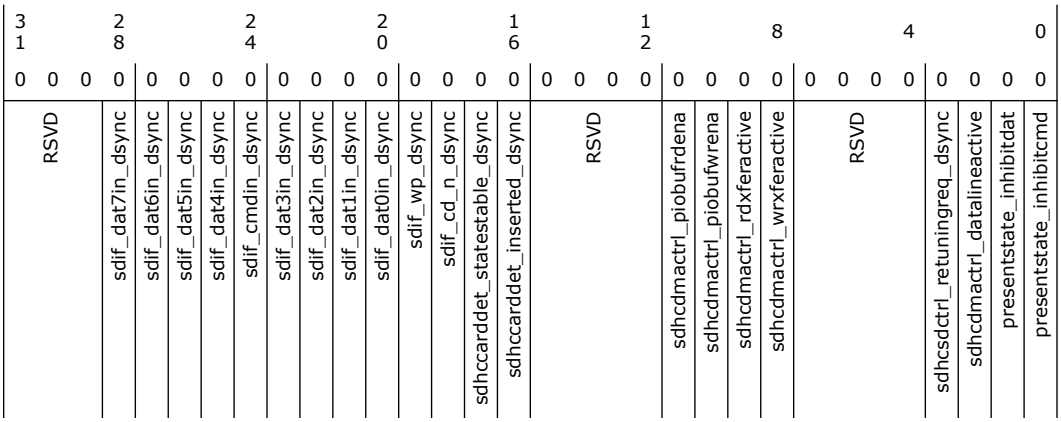
The Host Driver can get status of the Host Controller from this 32-bit read-only register

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 6

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	Reserved.
28	0h RO	**DAT7 Line Signal Level (sdif_dat7in_dsync):** This status is used to check DAT line level to recover from errors, and for debugging.
27	0h RO	**DAT6 Line Signal Level (sdif_dat6in_dsync):** This status is used to check DAT line level to recover from errors, and for debugging.
26	0h RO	**DAT5 Line Signal Level (sdif_dat5in_dsync):** This status is used to check DAT line level to recover from errors, and for debugging.
25	0h RO	**DAT4 Line Signal Level (sdif_dat4in_dsync):** This status is used to check DAT line level to recover from errors, and for debugging.
24	0h RO	**CMD Line Signal Level (sdif_cmdin_dsync):** This status is used to check DAT line level to recover from errors, and for debugging.
23	0h	**DAT3 Line Signal Level (sdif_dat3in_dsync):** This status is used to check DAT line level to recover from errors, and for debugging. This is
22	0h RO	**DAT2 Line Signal Level (sdif_dat2in_dsync):** This status is used to check DAT line level to recover from errors, and for debugging. This is
21	0h RO	**DAT1 Line Signal Level (sdif_dat1in_dsync):** This status is used to check DAT line level to recover from errors, and for debugging. This is
20	0h RO	**DAT0 Line Signal Level (sdif_dat0in_dsync):** This status is used to check DAT line level to recover from errors, and for debugging. This is
19	0h RO	**Write Protect Switch Pin Level (sdif_wp_dsync):** The Write Protect Switch is supported for memory and combo cards. This bit reflects the SDWP# pin. 0 - Write protected (SDWP# = 0) 1 - Write enabled (SDWP# = 1).
18	0h RO	**Card Level Detect (sdif_cd_n_dsync):** This bit reflects the inverse value of the SDCD# pin. 0 - No Card present (SDCD# = 1) 1 - Card present (SDCD# = 0).
17	0h RO	**Card State Stable (sdhccarddet_statestable_dsync):** This bit is used for testing. If it is 0, the Card Detect Pin Level is not stable. If this bit is set to 1, it means the Card Detect Pin Level is stable. The Software Reset For All in the Software Reset Register shall not affect this bit. 0 - Reset of Debouncing 1 - No Card or Inserted.
16	0h RO	**Card Inserted (sdhccarddet_inserted_dsync):** This bit indicates whether a card has been inserted. Changing from 0 to 1 generates a Card Insertion Interrupt in the Normal Interrupt Status register and changing from 1 to 0 generates a Card Removal Interrupt in the Normal Interrupt Status register. The Software Reset For All in the Software Reset register shall not affect this bit. If a Card is removed while its power is on and its clock is oscillating, the HC shall clear SD Bus Power in the Power Control register and SD Clock Enable in the Clock control register. In addition the HD should clear the HC by the Software Reset For All in Software register. The card detect is active regardless of the SD Bus Power. 0 - Reset or Debouncing or No Card 1 - Card Inserted
15:12	0h RO	Reserved.
11	0h RO	**Buffer Read Enable (sdhcdmactrl_piobufrdena):** This status is used for non-DMA read transfers. This read only flag indicates that valid data exists in the host side buffer status. If this bit is 1, readable data exists in the buffer. A change of this bit from 1 to 0 occurs when all the block data is read from the buffer. A change of this bit from 0 to 1 occurs when all the block data is ready in the buffer and generates the Buffer Read Ready Interrupt. 0 - Read Disable 1 - Read Enable
10	0h	**sdhcdmactrl_piobufwrena (sdhcdmactrl_piobufwrena):** This status is used for non-DMA write transfers.This read only flag indicates if space is available for write data.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RO	**Read Transfer Active (sdhcdmactrl_rdxferactive):** This status is used for detecting completion of a read transfer. This bit is set to 1 for either of the following conditions: • After the end bit of the read command • When writing a 1 to continue Request in the Block Gap Control register to restart a read transfer. This bit is cleared to 0 for either of the following conditions: • When the last data block as specified by block length is transferred to the system. • When all valid data blocks have been transferred to the system and no current block transfers are being sent as a result of the Stop At Block Gap Request set to 1. A transfer complete interrupt is generated when this bit changes to 0. 1 - Transferring data 0 - No valid data
8	0h RO	**Write Transfer Active (sdhcdmactrl_wrxferactive):** This status indicates a write transfer is active. If this bit is 0, it means no valid write data exists in the HC. This bit is set in either of the following cases: • After the end bit of the write command. • When writing a 1 to Continue Request in the Block Gap Control register to restart a write transfer. This bit is cleared in either of the following cases: • After getting the CRC status of the last data block as specified by the transfer count (Single or Multiple) • After getting a CRC status of any block where data transmission is about to be stopped by a Stop At Block Gap Request. During a write transaction, a Block Gap Event interrupt is generated when this bit is changed to 0, as a result of the Stop At Block Gap Request being set. This status is useful for the HD in determining when to issue commands during write busy. 1 - transferring data 0 - No valid data
7:4	0h RO	Reserved.
3	0h RO	**sdhcsdctrl_retuningreq_dsync (sdhcsdctrl_retuningreq_dsync):** Host Controller may request Host Driver to execute re-tuning sequence by setting this bit when the data window is shifted by temperature drift and any issue receiving the correct data. This bit is cleared when a command is issued with setting Execute Tuning in the Host Control 2 register. Changing of this bit from 0 to 1 generates Re-Tuning Event. This bit is cleared when a command is issued with setting Execute Tuning in the Host Control 2 register. Changing of this bit from 0 to 1 generates Re-Tuning Event. Refer to Normal Interrupt registers for more detail. This bit isn't set to 1 if Sampling Clock Select in the Host Control 2 register is set to 0 (using fixed sampling clock). 1: Sampling clock needs re-tuning 0: Fixed or well tuned sampling clock
2	0h RO	**DATA Line Active (sdhcdmactrl_datalineactive):** This bit indicates whether one of the DAT line on SD bus is in use. 1 - DAT line active 0 - DAT line inactive
1	0h RO	**Command Inhibit (DAT) (presentstate_inhibitdat):** This status bit is generated if either the DAT Line Active or the Read transfer Active is set to 1. If this bit is 0, it indicates the HC can issue the next SD command. Commands with busy signal belong to Command Inhibit (DAT) (ex. R1b, R5b type). Changing from 1 to 0 generates a Transfer Complete interrupt in the Normal interrupt status register. Note: The SD Host Driver can save registers in the range of 000-00Dh for a suspend transaction after this bit has changed from 1 to 0. 1 - Cannot issue command which uses the DAT line 0 - Can issue command which uses the DAT line
0	0h RO	**Command Inhibit (CMD) (presentstate_inhibitcmd):** If this bit is 0, it indicates the CMD line is not in use and the HC can issue a SD command using the CMD line. This bit is set immediately after the Command register (00Fh) is written. This bit is cleared when the command response is received. Even if the Command Inhibit (DAT) is set to 1, Commands using only the CMD line can be issued if this bit is 0. Changing from 1 to 0 generates a Command complete interrupt in the Normal Interrupt Status register. If the HC cannot issue the command because of a command conflict error or because of Command Not Issued By Auto CMD12 Error, this bit shall remain 1 and the Command Complete is not set. Status issuing Auto CMD12 is not read from this bit. Auto CMD12 and Auto CMD23 consist of two responses. In this case, this bit is not cleared by the response of CMD12 or CMD23 but cleared by the response of a read/write command. Status issuing Auto CMD12 is not read from this bit. So if a command is issued during Auto CMD12 operation, Host Controller shall manage to issue two commands: CMD12 and a command set by Command register.

14.2.10 Host Control1 Register (hostcontrol1)—Offset 28h

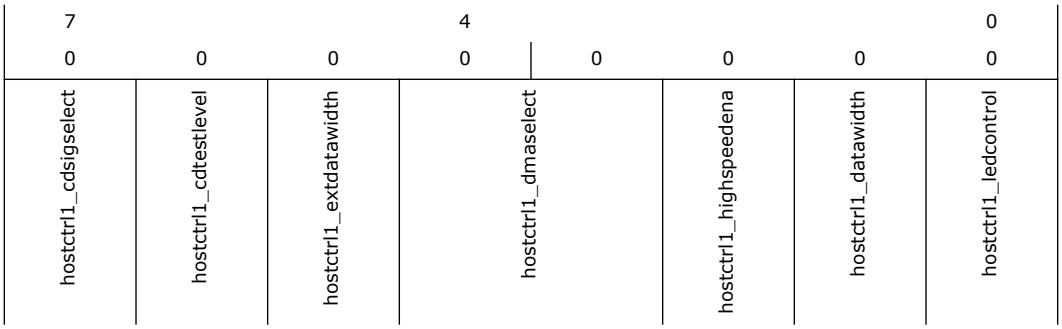
This register is used to program DMA modes, LED Control, Data Transfer Width, High Speed Enable, Card detect test level and signal selection

Access Method

Type: MEM Register
(Size: 8 bits)

Device: 30
Function: 6

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Card Detect Signal Detection (hostctrl1_cdsigselect):** This bit selects source for card detection. 1- The card detect test level is selected 0- SDCD# is selected (for normal use).
6	0h RW	**Card Detect Test Level (hostctrl1_cdtestlevel):** This bit is enabled while the Card Detect Signal Selection is set to 1 and it indicates card inserted or not. Generates (card ins or card removal) interrupt when the normal int sts enable bit is set. 1 - Card Inserted 0 - No Card.
5	0h RW	**Extended Data Transfer Width (hostctrl1_extdatawidth):** This bit controls 8-bit bus width mode for embedded device. Support of this function is indicated in 8-bit Support for Embedded Device in the Capabilities register. If a device supports 8-bit bus mode, this bit may be set to 1. If this bit is 0, bus width is controlled by Data Transfer Width in the Host Control 1 register.
4:3	0h RW	**DMA Select (hostctrl1_dmaselect):** One of supported DMA modes can be selected. The host driver shall check support of DMA modes by referring the Capabilities register. 00 - SDMA is selected 01 - 32-bit Address ADMA1 is selected 10 - 32-bit Address ADMA2 is selected 11 - 64-bit Address ADMA2 is selected.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**High Speed Enable (hostctrl1_highspeedena):** This bit is optional. Before setting this bit, the HD shall check the High Speed Support in the capabilities register. If this bit is set to 0 (default), the HC outputs CMD line and DAT lines at the falling edge of the SD clock (up to 25 MHz/ 20MHz for MMC). If this bit is set to 1, the HC outputs CMD line and DAT lines at the rising edge of the SD clock (up to 50 MHz for SD/52MHz for MMC)/ 208Mhz.
1	0h RW	**Data Transfer Width (hostctrl1_datawidth):** This bit selects the data width of the HC. The HD shall select it to match the data width of the SD card. 1 - 4 bit mode 0 - 1 bit mode.
0	0h RW	**LED Control (hostctrl1_ledcontrol):** This bit is used to caution the user not to remove the card while the SD card is being accessed. If the software is going to issue multiple SD commands, this bit can be set during all transactions. It is not necessary to change for each transaction. 1 - LED on 0 - LED off.

14.2.11 PowerControl Register (powercontrol)—Offset 29h

This register is used to program the SD Bus power and voltage level

Access Method

Type: MEM Register
(Size: 8 bits)

Device: 30
Function: 6

Default: 0h

7			4				0
0	0	0	0	0	0	0	0
	RSVD		emmc_hwreset	pwrctrl_sdbusvoltage			pwrctrl_sdbuspower

Bit Range	Default & Access	Field Name (ID): Description
7:5	0h RO	Reserved.
4	0h RW	**HW Reset (emmc_hwreset):** Hardware reset signal is generated when this bit is set '1' - Drives the hardware reset pin as ZERO (Active LOW to eMMC card) '0' - Deassert the hardware reset pin.
3:1	0h RW	**SD Bus Voltage Select (pwrctrl_sdbusvoltage):** By setting these bits, the HC selects the voltage level for the SD card. Before setting this register, the HC shall check the voltage support bits in the capabilities register. If unsupported voltage is selected, the Host System shall not supply SD bus voltage 111b - 3.3 V 110b - 3.0 V 101b - 1.8 V.
0	0h RW	**SD Bus Power (pwrctrl_sdbuspower):** Before setting this bit, the SD host driver shall set SD Bus Voltage Select. If the HC detects the No Card State, this bit shall be cleared. 1 - Power on 0 - Power off.

14.2.12 Block Gap Control Register (blockgapcontrol)—Offset 2Ah

This register is used to program the block gap request, read wait control and interrupt at block gap.

Access Method

Type: MEM Register
(Size: 8 bits)

Device: 30
Function: 6

Default: 80h

7			4				0
1	0	0	0	0	0	0	0
blkgapctrl_bootackena	blkgapctrl_altbootmode	blkgapctrl_bootenable	blkgapctrl_spimode	blkgapctrl_interrupt	blkgapctrl_rdwaitctrl	blkgapctrl_continue	blkgapctrl_stopatblkgap

Bit Range	Default & Access	Field Name (ID): Description
7	1h RW	**Boot Acknowledge Check (blkgapctrl_bootackena):** To check for the boot acknowledge in boot operation. 1 - wait for boot ack from the card 0 - Will not wait for boot ack from the card.
6	0h RW	**Alternate Boot Enable (blkgapctrl_altbootmode):** To start boot code access in alternative mode. 1- To start alternate boot mode access 0 - To stop alternate boot mode access.
5	0h RW	**Boot Code Access (blkgapctrl_bootenable):** To start boot code access 1- To start boot code access 0 - To stop boot code access
4	0h RW	**SPI mode enable (blkgapctrl_spimode):** SPI mode enable bit. 1- SPI mode 0 - SD mode
3	0h RW	**Interrupt at Block Gap (blkgapctrl_interrupt):** This bit is valid only in 4-bit mode of the SDIO card and selects a sample point in the interrupt cycle. Setting to 1 enables interrupt detection at the block gap for a multiple block transfer. If the SD card cannot signal an interrupt during a multiple block transfer, this bit should be set to 0. When the HD detects an SD card insertion, it shall set this bit according to the CCCR of the card.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Read Wait Control (blkgapctrl_rdwaitctrl):** The read wait function is optional for SDIO cards. If the card supports read wait, set this bit to enable use of the read wait protocol to stop read data using DAT[2] line. Otherwise the HC has to stop the SD clock to hold read data, which restricts commands generation. When the HD detects a card insertion, it shall set this bit according to the CCCR of the card. If the card does not support read wait, this bit shall never be set to 1 otherwise DAT line conflict may occur. If this bit is set to 0, Suspend / Resume cannot be supported 1 - Enable Read Wait Control 0 - Disable Read Wait Control
1	0h RW	**Continue Request (blkgapctrl_continue):** This bit is used to restart a transaction which was stopped using the Stop At Block Gap Request. To cancel stop at the block gap, set Stop At block Gap Request to 0 and set this bit to restart the transfer. The HC automatically clears this bit in either of the following cases: 1) In the case of a read transaction, the DAT Line Active changes from 0 to 1 as a read transaction restarts. 2) In the case of a write transaction, the Write transfer active changes from 0 to 1 as the write transaction restarts.
0	0h RW	**Stop At Block Gap Request (blkgapctrl_stopatblkgap):** This bit is used to stop executing a transaction at the next block gap for non- DMA,SDMA and ADMA transfers. Until the transfer complete is set to 1, indicating a transfer completion the HD shall leave this bit set to 1. Clearing both the Stop At Block Gap Request and Continue Request shall not cause the transaction to restart.

14.2.13 Wakeup Control Register (wakeupcontrol)—Offset 2Bh

This register is used to program the wakeup functionality.

Access Method

Type: MEM Register
(Size: 8 bits)

Device: 30
Function: 6

Default: 0h

7				4			0
0	0	0	0	0	0	0	0
		RSVD			wkupctrl_cardremoval	wkupctrl_cardinsertion	wkupctrl_cardinterrupt

Bit Range	Default & Access	Field Name (ID): Description
7:3	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Wakeup On SD Card Removal (wkupctrl_cardremoval):** This bit enables wakeup event via Card Removal assertion in the Normal Interrupt Status register. FN_WUS (Wake up Support) in CIS does not affect this bit. 1 - Enable 0 – Disable.
1	0h RW	**Wakeup On SD Card Insertion (wkupctrl_cardinsertion):** This bit enables wakeup event via Card Insertion assertion in the Normal Interrupt Status register. FN_WUS (Wake up Support) in CIS does not affect this bit. 1 - Enable 0 – Disable
0	0h RW	**Wakeup Event Enable On Card Interrupt (wkupctrl_cardinterrupt):** This bit enables wakeup event via Card Interrupt assertion in the Normal Interrupt Status register. This bit can be set to 1 if FN_WUS (Wake Up Support) in CIS is set to 1. 1 - Enable 0 - Disable.

14.2.14 Clock Control Register (clockcontrol)—Offset 2Ch

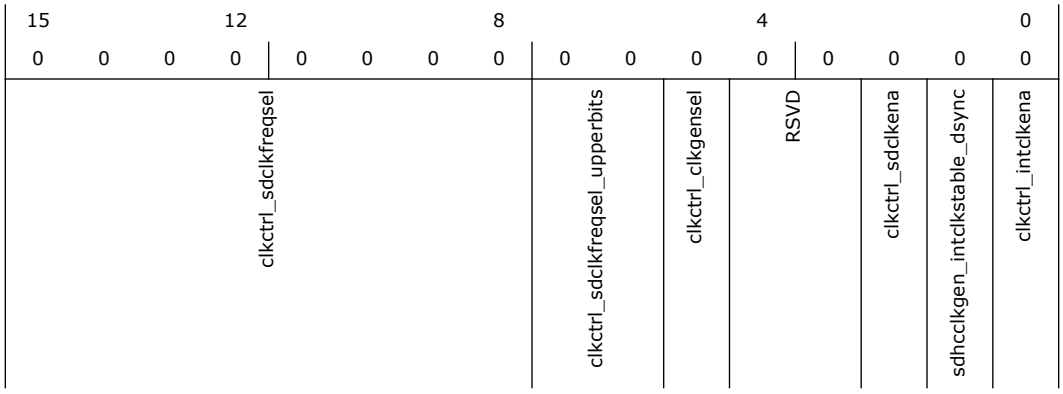
This register is used to program the Clock frequency select, generator select, Clock enable, Internal Clock state fields.

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 30
Function: 6

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RW	**SDCLK Frequency Select (clkctrl_sdclkfreqsel):** This register is used to select the frequency of the SDCLK pin. The frequency is not programmed directly; rather this register holds the divisor of the Base Clock Frequency For SD clock in the capabilities register. Only the following settings are allowed. 80h - base clock divided by 256 40h - base clock divided by 128 20h - base clock divided by 64 10h - base clock divided by 32 08h - base clock divided by 16 04h - base clock divided by 8 02h - base clock divided by 4 01h - base clock divided by 2 00h - base clock(10MHz-63MHz) Setting 00h specifies the highest frequency of the SD Clock.
7:6	0h RW	**Upper Bits of SDCLK Frequency Select (clkctrl_sdclkfreqsel_upperbits):** Bit 07-06 is assigned to bit 09-08 of clock divider in SDCLK Frequency Select
5	0h RW	**Clock Generator Select (clkctrl_clkgensel):** This bit is used to select the clock generator mode in SDCLK Frequency Select. If the Programmable Clock Mode is supported (non-zero value is set to Clock Multiplier in the Capabilities register), this bit attribute is RW, and if not supported,this bit attribute is RO and zero is read. This bit depends on the setting of Preset Value Enable in the Host Control 2 register. If the Preset Value Enable = 0, this bit is set by Host Driver. If the Preset Value Enable = 1, this bit is automatically set to a value specified in one of Preset Value registers. 1: Programmable Clock Mode 0: Divided Clock Mode.
4:3	0h RO	Reserved.
2	0h RW	**SD Clock Enable (clkctrl_sdclkena):** The HC shall stop SDCLK when writing this bit to 0. SDCLK frequency Select can be changed when this bit is 0.
1	0h RO	**Internal Clock Stable (sdhcclkgen_intclkstable_dsync):** This bit is set to 1 when SD clock is stable after writing to Internal Clock Enable in this register to 1. The SD Host Driver shall wait to set SD Clock Enable until this bit is set to 1.
0	0h RW	**Internal Clock Enable (clkctrl_intclkena):** This bit is set to 0 when the HD is not using the HC or the HC awaits a wakeup event. The HC should stop its internal clock to go very low power state. 1 - Oscillate 0 - Stop.

14.2.15 Timeout Control Register (timeoutcontrol)—Offset 2Eh

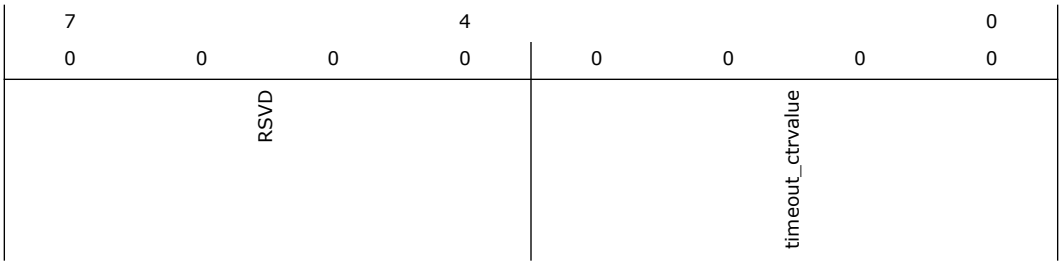
This value determines the interval by which DAT line time-outs are detected. Refer to the Data Time-out Error in the Error Interrupt Status register for information on factors that dictate time-out generation. Time-out clock frequency will be generated by dividing the sd clock TMCLK by this value. When setting this register, prevent inadvertent time-out events by clearing the Data Time-out Error Status Enable (in the Error Interrupt Status Enable register)
1110 - TMCLK * 2^27
0001 - TMCLK * 2^14
0000 - TMCLK * 2^13.

Access Method

Type: MEM Register (Size: 8 bits)

Device: 30
Function: 6

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7:4	0h RO	Reserved.
3:0	0h RW	**Data Timeout Counter Value (timeout_ctrvalue):** This value determines the interval by which DAT line time-outs are detected.

14.2.16 Software Reset Register (softwarereset)—Offset 2Fh

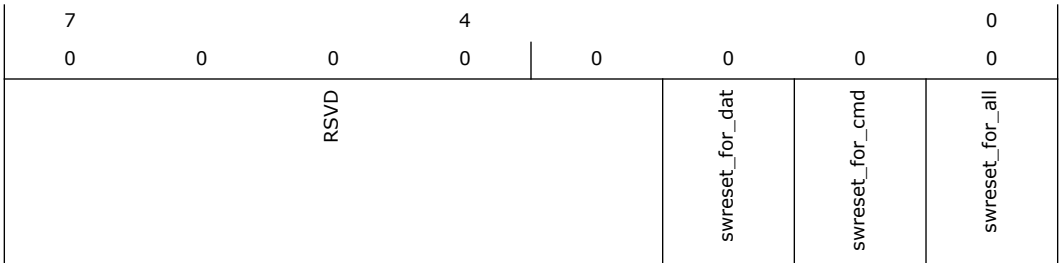
This register is used to program the software reset for data, command and for all.

Access Method

Type: MEM Register (Size: 8 bits)

Device: 30
Function: 6

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7:3	0h RO	Reserved.
2	0h RW	**Software Reset for DAT Line (swreset_for_dat):** Only part of data circuit is reset. The following registers and bits are cleared by this bit: Buffer Data Port Register - Buffer is cleared and initialized. Present State register - Buffer read Enable - Buffer write Enable - Read Transfer Active - Write Transfer Active - DAT Line Active - Command Inhibit (DAT) Block Gap Control register - Continue Request - Stop At Block Gap Request Normal Interrupt Status register - Buffer Read Ready - Buffer Write Ready - Block Gap Event - Transfer Complete 1 - Reset 0 - Work.
1	0h RW	**Software Reset for CMD Line (swreset_for_cmd):** Only part of command circuit is reset. The following registers and bits are cleared by this bit: Present State register - Command Inhibit (CMD) Normal Interrupt Status register - Command Complete 1 - Reset 0 - Work.
0	0h RW	**SW Reset for All (swreset_for_all):** This reset affects the entire HC except for the card detection circuit. Register bits of type ROC, RW, RW1C, RWAC are cleared to 0. During its initialization, the HD shall set this bit to 1 to reset the HC. The HC shall reset this bit to 0 when capabilities registers are valid and the HD can read them. Additional use of Software Reset For All may not affect the value of the Capabilities registers. If this bit is set to 1, the SD card shall reset itself and must be re initialized by the HD. 1 - Reset 0 - Work

14.2.17 Normal Interrupt Status Register (normalintrsts)—Offset 30h

This register gives the status of all the interrupts

Access Method

Type: MEM Register (Size: 16 bits)

Device: 30
Function: 6

Default: 0h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
reg_errorintrsts	normalintrsts_bootcomplete	normalintrsts_rcvbootack	normalintrsts_retuningevent	normalintrsts_intc	normalintrsts_intb	normalintrsts_inta	normalintrsts_cardintsts	normalintrsts_cardremsts	normalintrsts_cardinssts	normalintrsts_bufrdready	normalintrsts_bufwrready	normalintrsts_dmainterrupt	normalintrsts_blkgapevent	normalintrsts_xfercomplete	normalintrsts_cmdcomplete

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Error Interrupt (reg_errorintrsts):** If any of the bits in the Error Interrupt Status Register are set, then this bit is set. Therefore the HD can test for an error by checking this bit first. 0 - No Error 1 – Error.
14	0h RW1C	**Boot Terminate Interrupt (normalintrsts_bootcomplete):** This status is set if the boot operation get terminated 0 - Boot operation is not terminated 1 - Boot operation is terminated.
13	0h RW1C	**Boot Ack Rcv (normalintrsts_rcvbootack):** This status is set if the boot acknowledge is received from device. 0 - Boot ack is not received 1 - Boot ack is received.
12	0h RO	**Re-Tuning Event (normalintrsts_retuningevent):** This status is set if Re-Tuning Request in the Present State register changes from 0 to 1. Host Controller requests Host Driver to perform re-tuning for next data transfer. Current data transfer (not large block count) can be completed without retuning. 1 Re-Tuning should be performed 0 Re-Tuning is not required.
11	0h RO	**INT_C Status (normalintrsts_intc):** This status is set if INT_C is enabled and INT_C# pin is in low level. It is cleared by resetting the INT_C interrupt factor.
10	0h RO	**INT_B Status (normalintrsts_intb):** This status is set if INT_B is enabled and INT_B# pin is in low level. It is cleared by resetting
9	0h RO	**INT_A Status (normalintrsts_inta):** This status is set if INT_A is enabled and INT_A# pin is in low level. It is cleared by resetting
8	0h RO	**Card Interrupt (normalintrsts_cardintsts):** In 1-bit mode, the HC shall detect the Card Interrupt without SD Clock to support wakeup. In 4-bit mode, the card interrupt signal is sampled during the interrupt cycle, so there are some sample delays between the interrupt signal from the card and the interrupt to the Host system. 0 - No Card Interrupt 1 - Generate Card Interrupt.
7	0h RW1C	**Card Removal (normalintrsts_cardremsts):** This status is set if the Card Inserted in the Present State register changes from 1 to 0. When the HD writes this bit to 1 to clear this status the status of the Card Inserted in the Present State register should be confirmed. 0 - Card State Stable or Debouncing 1 - Card Removed.
6	0h RW1C	**Card Insertion (normalintrsts_cardinssts):** This status is set if the Card Inserted in the Present State register changes from 0 to 1. When the HD writes this bit to 1 to clear this status the status of the Card Inserted in the Present State register should be confirmed. Because the card detect may possibly be changed when the HD clear this bit an Interrupt event may not be generated. 0 - Card State Stable or Debouncing 1 - Card Inserted

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW1C	**Buffer Read Ready (normalintrsts_bufrdready):** This status is set if the Buffer Read Enable changes from 0 to 1. Buffer Read Ready is set to 1 for every CMD19 execution in tuning procedure. 0 - Not Ready to read Buffer. 1 - Ready to read Buffer
4	0h RW1C	**Buffer Write Ready (normalintrsts_bufwrready):** This status is set if the Buffer Write Enable changes from 0 to 1.
3	0h RW1C	**DMA Interrupt (normalintrsts_dmainterrupt):** This status is set if the HC detects the Host DMA Buffer Boundary in the Block Size register.
2	0h RW1C	**Block Gap Event (normalintrsts_blkgapevent):** If the Stop At Block Gap Request in the BlockGap Control Register is set, this bit is set.
1	0h RW1C	**Transfer Complete (normalintrsts_xfercomplete):** This bit is set when a read / write transaction is completed.
0	0h RW1C	**Command Complete (normalintrsts_cmdcomplete):** This bit is set when we get the end bit of the command response (Except Auto CMD12 and Auto CMD23). 0 - No Command Complete 1 - Command Complete

14.2.18 Error Interrupt Status (errorintrsts)—Offset 32h

This register gives the status of the error interrupts

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 30
Function: 6

Default: 0h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD			errorintrsts_hosterror	RSVD		errorintrsts_admaerror	errorintrsts_autocmderror	errorintrsts_currlimiterror	errorintrsts_dataendbiterror	errorintrsts_datacrcerror	errorintrsts_datatimeouterror	errorintrsts_cmdindexerror	errorintrsts_cmdendbiterror	errorintrsts_cmdcrcerror	errorintrsts_cmdtimeouterror

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO	Reserved.
12	0h RW	**Target Response Error (errorintrsts_hosterror):** Occurs when detecting Host ERROR
11:10	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**ADMA Error (errorintrsts_admaerror):** This bit is set when the Host Controller detects errors during ADMA based data transfer.
8	0h RW	**Auto CMD Error (errorintrsts_autocmderror):** This bit is set when detecting that one of the bits D00-D04 in Auto CMD Error Status register has changed from 0 to 1.
7	0h RW	**Current Limit Error (errorintrsts_currlimiterror):** If this bit is 1, it means that the HC is not supplying power to SD card due to some failure.Reading 0 means that the HC is supplying power and no error has occurred.
6	0h RW	**Data End Bit Error (errorintrsts_dataendbiterror):** Occurs when detecting 0 at the end bit position of read data which uses the DAT line or the end bit position of the CRC status.
5	0h RW	**Data CRC Error (errorintrsts_datacrcerror):** Occurs when detecting CRC error when transferring read data which uses the DAT line or when detecting the Write CRC Status having a value of other than 010b.
4	0h RW	**Data Timeout Error (errorintrsts_datatimeouterror):** This status is set if Data Timeout error occurs.
3	0h RW	**Command Index Error (errorintrsts_cmdindexerror):** Occurs if a Command Index error occurs in the Command Response.
2	0h RW	**Command End Bit Error (errorintrsts_cmdendbiterror):** Occurs when detecting that the end bit of a command response is 0.
1	0h RW	**Command CRC Error (errorintrsts_cmdcrcerror):** This bit is set when Command CRC Error is generated. '0' No Error, '1' CRC Error
0	0h RW	**Command Timeout Error (errorintrsts_cmdtimeouterror):** This bit is set if no response is returned within 64 SDCLK cycles from the end bit of the command.

14.2.19 Normal Interrupt Status Enable Register (normalintrstsena)—Offset 34h

This register is used to enable the normal interrupt status register fields

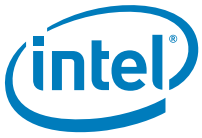
Access Method

Type: MEM Register
(Size: 16 bits)

Device: 30
Function: 6

Default: 0h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD	normalintrsts_enableregbit14	normalintrsts_enableregbit13	normalintrsts_enableregbit12	normalintrsts_enableregbit11	normalintrsts_enableregbit10	normalintrsts_enableregbit9	sdhcregset_cardintstsena	sdhcregset_cardremstsena	sdhcregset_cardinsstsena	normalintrsts_enableregbit5	normalintrsts_enableregbit4	normalintrsts_enableregbit3	normalintrsts_enableregbit2	normalintrsts_enableregbit1	normalintrsts_enableregbit0



Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	Reserved.
14	0h RW	**Boot Terminate Interrupt Enable (normalintrsts_enableregbit14):** This status is set if the boot operation gets terminated.
13	0h RW	**Boot Ack rcv Enable (normalintrsts_enableregbit13):** This status is set if the boot acknowledge is received from device.
12	0h RW	**Re-Tuning Event Status Enable (normalintrsts_enableregbit12):** This status is set if Re-Tuning Request in the Present State register changes from 0 to 1.
11	0h RW	**INT_C Status Enable (normalintrsts_enableregbit11):** If this bit is set to 0, the Host Controller shall clear the interrupt request to the System.
10	0h RW	**INT_B Status Enable (normalintrsts_enableregbit10):** If this bit is set to 0, the Host Controller shall clear the interrupt request to the System.
9	0h RW	**INT_A Status Enable (normalintrsts_enableregbit9):** If this bit is set to 0, the Host Controller shall clear the interrupt request to the System.
8	0h RW	**Card Interrupt Status Enable (sdhcregset_cardintstsena):** If this bit is set to 0, the HC shall clear Interrupt request to the System. The Card Interrupt detection is stopped when this bit is cleared and restarted when this bit is set to 1.
7	0h RW	**Card Removal Status Enable (sdhcregset_cardremstsena):** This status is set if the Card Inserted in the Present State register changes from 1 to 0.
6	0h RW	**Card Insertion Status Enable (sdhcregset_cardinsstsena):** This status is set if the Card Inserted in the Present State register changes from 0 to 1.
5	0h RW	**Buffer Read Ready Status Enable (normalintrsts_enableregbit5):** This status is set if the Buffer Read Enable changes from 0 to 1.
4	0h RW	**Buffer Write Ready Status Enable (normalintrsts_enableregbit4):** This status is set if the Buffer Write Enable changes from 0 to 1.
3	0h RW	**DMA Interrupt Status Enable (normalintrsts_enableregbit3):** This status is set if the HC detects the Host DMA Buffer Boundary in the Block Size regiser.
2	0h RW	**Block Gap Event Status Enable (normalintrsts_enableregbit2):** If the Stop At Block Gap Request in the BlockGap Control Register is set, this bit is set.
1	0h RW	**Transfer Complete Status Enable (normalintrsts_enableregbit1):** This bit is set when a read / write transaction is completed.
0	0h RW	**Command Complete Status Enable (normalintrsts_enableregbit0):** This bit is set when we get the end bit of the command response.

14.2.20 Error Interrupt Status Enable Register (errorintrstsena)—Offset 36h

This register is used to enable the Error Interrupt Status register fields.
The register is RW except for the reserved bits which are RO.

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 30
Function: 6

Default: 0h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD			errorintrsts_enableregbit12	RSVD	errorintrsts_enableregbit10	errorintrsts_enableregbit9	errorintrsts_enableregbit8	errorintrsts_enableregbit7	errorintrsts_enableregbit6	errorintrsts_enableregbit5	errorintrsts_enableregbit4	errorintrsts_enableregbit3	errorintrsts_enableregbit2	errorintrsts_enableregbit1	errorintrsts_enableregbit0

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO	Reserved.
12	0h RW	**Target Response Error /Host Error Status Enable (errorintrsts_enableregbit12):** 0 - Masked 1 - Enabled
11	0h RO	Reserved.
10	0h RW	**Tuning error status enable (errorintrsts_enableregbit10):** 0 - Masked 1 - Enabled
9	0h RW	**ADMA Error Status Enable (errorintrsts_enableregbit9):** 0 - Masked 1 - Enabled
8	0h RW	**Auto CMD12 Error Status Enable (errorintrsts_enableregbit8):** 0 - Masked 1 - Enabled
7	0h RW	**Current Limit Error Status Enable (errorintrsts_enableregbit7):** 0 - Masked 1 - Enabled
6	0h RW	**Data End Bit Error Status Enable (errorintrsts_enableregbit6):** 0 - Masked 1 - Enabled
5	0h RW	**Data CRC Error Status Enable (errorintrsts_enableregbit5):** 0 - Masked 1 - Enabled
4	0h RW	**Data Timeout Error Status Enable (errorintrsts_enableregbit4):** 0 - Masked 1 - Enabled
3	0h RW	**Command Index Error Status Enable (errorintrsts_enableregbit3):** 0 - Masked 1 - Enabled
2	0h RW	**Command End Bit Error Status Enable (errorintrsts_enableregbit2):** 0 - Masked 1 - Enabled
1	0h RW	**Command CRC Error Status Enable (errorintrsts_enableregbit1):** 0 - Masked 1 - Enabled
0	0h RW	**Command Timeout Error Status Enable (errorintrsts_enableregbit0):** 0 - Masked 1 - Enabled

14.2.21 Normal Interrupt Signal Enable Register (normalintrsigena)—Offset 38h

This register is used to enable the Normal Interrupt Signal register. All the bits are RW, except for Reserved bits, and defined as follows:
0 - Masked
1 - Enabled.

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 30
Function: 6

Default: 0h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
normalintrsts_enableregbit15	normalintrsts_enableregbit14	normalintrsts_enableregbit13	normalintrsts_enableregbit12	normalintrsts_enableregbit11	normalintrsts_enableregbit10	normalintrsts_enableregbit9	sdhcregset_cardintstsena	sdhcregset_cardremstsena	sdhcregset_cardinsstsena	normalintrsts_enableregbit5	normalintrsts_enableregbit4	normalintrsts_enableregbit3	normalintrsts_enableregbit2	normalintrsts_enableregbit1	normalintrsts_enableregbit0

Bit Range	Default & Access	Field Name (ID): Description
15	0h	**normalintrsts_enableregbit15 (normalintrsts_enableregbit15):** The HD shall control error Interrupts using the Error Interrupt Signal Enable register.
14	0h	**normalintrsts_enableregbit14 (normalintrsts_enableregbit14):** Boot Terminate Interrupt Signal Enable
13	0h	**normalintrsts_enableregbit13 (normalintrsts_enableregbit13):** Boot ack rcv Signal Enable
12	0h	**normalintrsts_enableregbit12 (normalintrsts_enableregbit12):** Re-Tuning Event Signal Enable
11	0h	**normalintrsts_enableregbit11 (normalintrsts_enableregbit11):** INT_C Signal Enable
10	0h	**normalintrsts_enableregbit10 (normalintrsts_enableregbit10):** INT_B Signal Enable
9	0h	**normalintrsts_enableregbit9 (normalintrsts_enableregbit9):** INT_A Signal Enable
8	0h	**sdhcregset_cardintstsena (sdhcregset_cardintstsena):** Card Interrupt Signal Enable
7	0h	**sdhcregset_cardremstsena (sdhcregset_cardremstsena):** Card Removal Signal Enable
6	0h	**sdhcregset_cardinsstsena (sdhcregset_cardinsstsena):** Card Insertion Signal Enable

Bit Range	Default & Access	Field Name (ID): Description
5	0h	**normalintrsts_enableregbit5 (normalintrsts_enableregbit5):** Buffer Read Ready Signal Enable
4	0h	**normalintrsts_enableregbit4 (normalintrsts_enableregbit4):** Buffer Write Ready Signal Enable
3	0h	**normalintrsts_enableregbit3 (normalintrsts_enableregbit3):** DMA Interrupt Signal Enable
2	0h	**normalintrsts_enableregbit2 (normalintrsts_enableregbit2):** Block Gap Event Signal Enable
1	0h	**normalintrsts_enableregbit1 (normalintrsts_enableregbit1):** Transfer Complete Signal Enable
0	0h	**normalintrsts_enableregbit0 (normalintrsts_enableregbit0):** Command Complete Signal Enable

14.2.22 Error Interrupt Signal Enable Register (errorintrsigena)—Offset 3Ah

This register is used to enable the Normal Interrupt Signal register. All the bits are RW, except for Reserved bits, and defined as follows:
0 - Masked
1 - Enabled.

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 30
Function: 6

Default: 0h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD			errorintrsig_enableregbit12	RSVD	errorintrsig_enableregbit10	errorintrsig_enableregbit9	errorintrsig_enableregbit8	errorintrsig_enableregbit7	errorintrsig_enableregbit6	errorintrsig_enableregbit5	errorintrsig_enableregbit4	errorintrsig_enableregbit3	errorintrsig_enableregbit2	errorintrsig_enableregbit1	errorintrsig_enableregbit0

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO	Reserved.
12	0h	**errorintrsig_enableregbit12 (errorintrsig_enableregbit12):** Target Response Error Signal Enable
11	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
10	0h	**errorintrsig_enableregbit10 (errorintrsig_enableregbit10):** Tuning Error Signal Enable
9	0h	**errorintrsig_enableregbit9 (errorintrsig_enableregbit9):** ADMA Error Signal Enable
8	0h	**errorintrsig_enableregbit8 (errorintrsig_enableregbit8):** Auto CMD Error Signal Enable
7	0h	**errorintrsig_enableregbit7 (errorintrsig_enableregbit7):** Current Limit Error Signal Enable
6	0h	**errorintrsig_enableregbit6 (errorintrsig_enableregbit6):** Data End Bit Error Signal Enable
5	0h	**errorintrsig_enableregbit5 (errorintrsig_enableregbit5):** Data CRC Error Signal Enable
4	0h	**errorintrsig_enableregbit4 (errorintrsig_enableregbit4):** Data Timeout Error Signal Enable
3	0h	**errorintrsig_enableregbit3 (errorintrsig_enableregbit3):** Command Index Error Signal Enable
2	0h	**errorintrsig_enableregbit2 (errorintrsig_enableregbit2):** Command End Bit Error Signal Enable
1	0h	**errorintrsig_enableregbit1 (errorintrsig_enableregbit1):** Command CRC Error Signal Enable
0	0h	**errorintrsig_enableregbit0 (errorintrsig_enableregbit0):** Command Timeout Error Signal Enable

14.2.23 Auto CMD12 Error Status Register (autocmderrsts)—Offset 3Ch

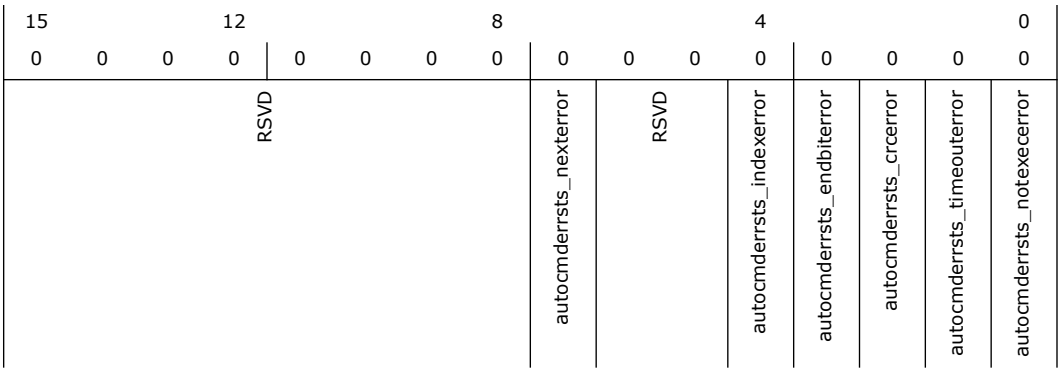
This register is used to indicate CMD12 response error of Auto CMD12 and CMD23 response error of Auto CMD 23

Access Method

Type: MEM Register (Size: 16 bits)

Device: 30
Function: 6

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	Reserved.
7	0h RO	**Command Not Issued By Auto CMD12 Error (autocmderrsts_nexterror):** Setting this bit to 1 means CMD_wo_DAT is not executed due to an Auto CMD12 error(D04- D01) in this register. This bit is set to 0 when Auto CMD Error is generated by Auto CMD23 0 – No Error 1 – Not Issued
6:5	0h RO	Reserved.
4	0h RO	**Auto CMD Index Error (autocmderrsts_indexerror):** Occurs if the Command Index error occurs in response to a command. 0 – No Error 1 – Error
3	0h RO	**Auto CMD End Bit Error (autocmderrsts_endbiterror):** Occurs when detecting that the end bit of command response is 0. 0 – No Error 1 – End Bit Error Generated
2	0h RO	**Auto CMD CRC Error (autocmderrsts_crcerror):** Occurs when detecting a CRC error in the command response. 0 – No Error 1 – CRC Error Generated
1	0h RO	**Auto CMD Timeout Error (autocmderrsts_timeouterror):** Occurs if the no response is returned within 64 SDCLK cycles from the end bit of the command. If this bit is set to 1, the other error status bits (D04 - D02) are meaningless. 0 - No Error 1 - Timeout.
0	0h RO	**Auto CMD12 not Executed (autocmderrsts_notexecerror):** If memory multiple block data transfer is not started due to command error, this bit is not set because it is not necessary to issue Auto CMD12. Setting this bit to 1 means the HC cannot issue Auto CMD12 to stop memory multiple block transfer due to some error. 0 - Executed 1 - Not Executed.

14.2.24 Host Control 2 Register (hostcontrol2)—Offset 3Eh

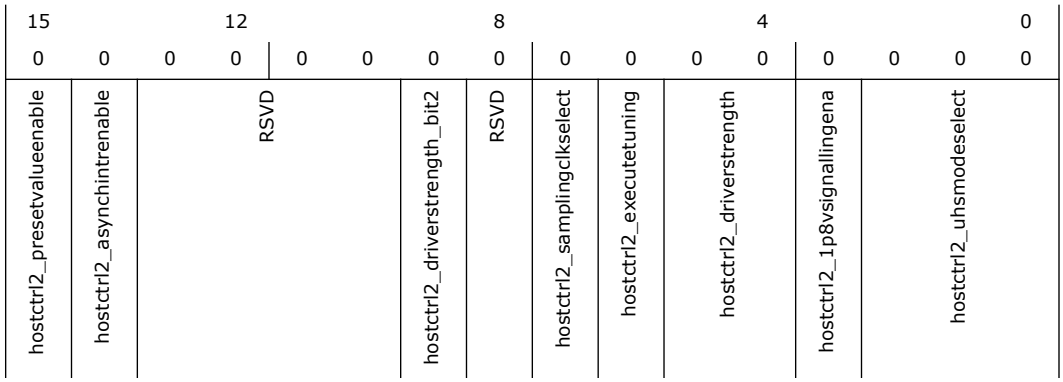
This register is used to program UHS Select Mode,UHS Select Mode,Driver Strength Select,Execute Tuning,Sampling Clock Select,Asynchronous Interrupt Enable and Preset value enable

Access Method

Type: MEM Register (Size: 16 bits)

Device: 30
Function: 6

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15	0h	**hostctrl2_presetvalueenable (hostctrl2_presetvalueenable):** This bit enables the functions defined in the Preset Value registers.
14	0h RW	**Asynchronous Interrupt Enable (hostctrl2_asynchintrenable):** This bit can be set to 1 if a card support asynchronous interrupt and Asynchronous Interrupt Support is set to 1 in the Capabilities register. 0 – Disabled 1 – Enabled.
13:10	0h RO	Reserved.
9	0h RW	**Driver strength (hostctrl2_driverstrength_bit2):** This is the programmed Drive Strength output and it[2] of the sdhccore_drivestrength value.
8	0h RO	Reserved.
7	0h RW	**Sampling Clock Select (hostctrl2_samplingclkselect):** This bit is set by tuning procedure when Execute Tuning is cleared. Writing 1 to this bit is meaningless and ignored. Setting 1 means that tuning is completed successfully and setting 0 means that tuning is failed. Controller is receiving response or a read data block. 0 - Fixed clock is used to sample data 1 - Tuned clock is used to sample data
6	0h RW	**Execute Tuning (hostctrl2_executetuning):** This bit is set to 1 to start tuning procedure and automatically cleared when tuning procedure is completed. The result of tuning is indicated to Sampling Clock Select. Tuning procedure is aborted by writing 0 for more detail about tuning procedure. 0 - Not Tuned or Tuning Completed 1 - Execute Tuning.
5:4	0h RW	**Driver Strength Select (hostctrl2_driverstrength):** Host Controller output driver in 1.8V signaling is selected by this bit. In 3.3V signaling, this field is not effective.
3	0h RW	**1.8V Signaling Enable (hostctrl2_1p8vsignallingena):** This bit controls voltage regulator for I/O cell. 3.3V is supplied to the card regardless of signaling voltage. Setting this bit from 0 to 1 starts changing signal voltage from 3.3V to 1.8V.
2:0	0h RW	**UHS Mode Select (hostctrl2_uhsmodeselect):** This field is used to select one of UHS-I modes and effective when 1.8V Signaling Enable is set to 1. Select in the Clock Control register and Driver Strength Select according to Preset Value registers. In this case, one of preset value registers is selected by this field. Host Driver needs to reset SD Clock Enable before changing this field to avoid generating clock glitch. After setting this field, Host Driver sets SD Clock Enable again. 000b - SDR12 001b - SDR25 010b - SDR50 011b - SDR104 100b - DDR50 101b - HS400

14.2.25 Capabilities Register (capabilities)—Offset 40h

This register provides the host driver with information specific to the host controller implementation. Please note, that the default values shown here assume no bypass of the capabilities register. In case software decides to bypass the default capabilities register values the reset values will present the bypassed value.

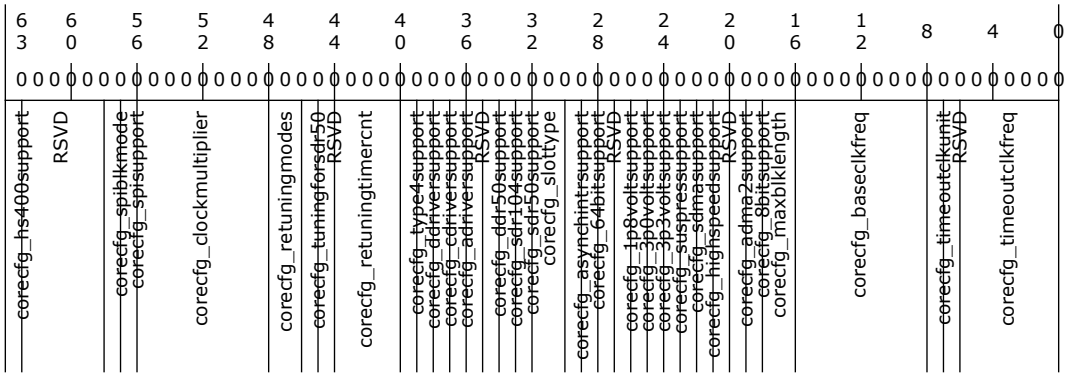
Access Method

Type: MEM Register (Size: 64 bits)

Device: 30

Function: 6

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
63	0h RO	**HS 400 Support (corecfg_hs400support):** This field indicates whether HS400 is supported or not. 0 –Not Supported 1 –Supported
62:58	0h RO	Reserved.
57	0h RO	**SPI Block Mode (corecfg_spiblkmode):** This field indicates whether SPI Block Mode is supported or not. 0 –Not Supported 1 –Supported
56	0h RO	**SPI Mode Support (corecfg_spisupport):** This field indicates whether SPI Mode is supported or not. 0 –Not Supported 1 –Supported
55:48	0h RO	**Clock Multiplier (corecfg_clockmultiplier):** This field indicates clock multiplier value of programmable clock generator. Setting 00h means that Host Controller does not support programmable clock generator.
47:46	0h RO	**Re-tuning Modes (corecfg_retuningmodes):** This field defines the re-tuning capability of a Host Controller and how to manage the data transfer length and a Re-Tuning Timer by the Host Driver 00 - Mode1 01 - Mode2 10 - Mode3 11 - Reserved There are two re-tuning timings: Re-Tuning Request and expiration of a Re-Tuning Timer. By receiving either timing, the Host Driver executes the re-tuning procedure just before a next command issue.

Bit Range	Default & Access	Field Name (ID): Description
45	0h RO	**Use Tuning for SDR50 (corecfg_tuningforsdr50):** If this bit is set to 1, this Host Controller requires tuning to operate SDR50. (Tuning is always required to operate SDR104.) 1 SDR50 requires tuning 0 SDR50 does not require tuning
44	0h RO	Reserved.
43:40	0h RO	**Timer count for Re-Tuning (corecfg_retuningtimercnt):** This field indicates an initial value of the Re-Tuning Timer for Re-Tuning Mode 1 to 3. 0h - Get information via other source 1h = 1 seconds 2h = 2 seconds 3h = 4 seconds 4h = 8 seconds -- n = 2(n-1) seconds -- Bh = 1024 seconds Fh - Ch = Reserved
39	0h RO	**Driver Type 4 Support (corecfg_type4support):** This bit indicates support of Type 4 Driver.
38	0h RO	**Driver Type D Support (corecfg_ddriversupport):** This bit indicates support of Driver Type D for 1.8 Signaling.
37	0h RO	**Driver Type C Support (corecfg_cdriversupport):** This bit indicates support of Driver Type C for 1.8 Signaling.
36	0h RO	**Driver Type A Support (corecfg_adriversupport):** This bit indicates support of Driver Type A for 1.8 Signaling.
35	0h RO	Reserved.
34	0h RO	**DDR50 Support (corecfg_ddr50support):** This bit indicates whether DDR50 is supported.
33	0h RO	**SDR104 Support (corecfg_sdr104support):** This bit indicates whether SDR104 is supported.SDR104 requires tuning.
32	0h RO	**SDR50 Support (corecfg_sdr50support):** This bit indicates whether SDR50 is supported.
31:30	0h RO	**Slot Type (corecfg_slottype):** 00b Removable Card Slot 01b Embedded Slot for One Device 10b Shared Bus Slot 11b Reserved
29	0h RO	**Asynchronous Interrupt Support (corecfg_asynchintrsupport):** Asynchronous Interrupt Support
28	0h RO	**64-bit System Bus Support (corecfg_64bitsupport):** This bit indicates whether the HC supports 64bit System Bus
27	0h RO	Reserved.
26	0h RO	**Voltage Support 1.8V (corecfg_1p8voltsupport):** This bit indicates whether the HC supports 1.8V.
25	0h RO	**Voltage Support 3.0V (corecfg_3p0voltsupport):** This bit indicates whether the HC supports 3.0V.
24	0h RO	**Voltage Support 3.3V (corecfg_3p3voltsupport):** This bit indicates whether the HC supports 3.3V.
23	0h RO	**Suspend / Resume Support (corecfg_suspressupport):** This bit indicates whether the HC supports Suspend/Resume functionality.

Bit Range	Default & Access	Field Name (ID): Description
22	0h RO	**SDMA Support (corecfg_sdmasupport):** This bit indicates whether the HC is capable of using DMA to transfer data between system memory and the HC directly. (SDMA Mode) 0 –Not Supported 1 –Supported
21	0h RO	**High Speed Support (corecfg_highspeedsupport):** This bit indicates whether the HC and the Host System support High Speed mode. 0 –Not Supported 1 –Supported
20	0h RO	Reserved.
19	0h RO	**ADMA2 Support (corecfg_adma2support):** ADMA2 not supported. Hardwired to 0.
18	0h RO	**8 Bit Support for Embedded Device (corecfg_8bitsupport):** This bit indicates whether the Host Controller is capable of using 8-bit bus width mode.
17:16	0h RO	**Max Block Length (corecfg_maxblklength):** This value indicates the maximum block size that the HD can read and write to the buffer in the HC. The buffer shall transfer this block size without wait cycles. Sizes can be defined as indicated below. 00 - 512 byte 01 - 1024 byte 10 - 2048 byte 11 - 4096 byte.
15:8	0h RO	**Base Clock Frequency for SD Clock (corecfg_baseclkfreq):** (1) 6-bit Base Clock Frequency This mode is supported by the Host Controller Version 1.00 and 2.00. Upper 2- bit is not effective and always 0. Unit values are 1MHz. The supported clock range is 10MHz to 63MHz. 0011 1111b 63MHz 0000 0010b 2MHz 0000 0001b 1MHz (2) 8-bit Base Clock Frequency This mode is supported by the Host Controller Version 3.00. Unit values are 1MHz. The supported clock range is 10MHz to 255MHz. FFh 255MHz 02h 2MHz 01h 1MHz.
7	0h RO	**Timeout Clock Unit (corecfg_timeoutclkunit):** This bit shows the unit of base clock frequency used to detect Data Timeout Error. 0 - KHz 1 - MHz
6	0h RO	Reserved.
5:0	0h RO	**Timeout Clock Frequency (corecfg_timeoutclkfreq):** This bit shows the base clock frequency used to detect Data Timeout Error. Not 0 - 1Khz to 63Khz or 1Mhz to 63Mhz.

14.2.26 Maximum Current Capabilities Register (maxcurrentcap)—Offset 48h

This register indicates maximum current capability for each voltage

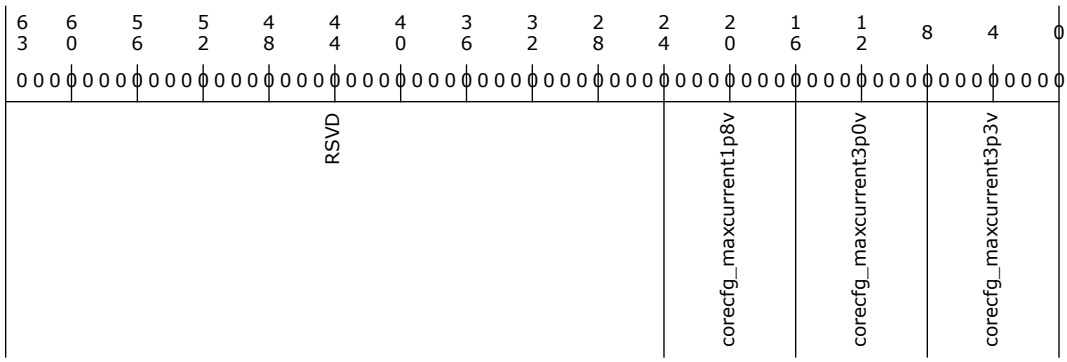
Access Method

Type: MEM Register (Size: 64 bits)

Device: 30

Function: 6

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
63:24	0h RO	Reserved.
23:16	0h RO	**Maximum Current for 1.8V (corecfg_maxcurrent1p8v):** Maximum Current for 1.8V 0 – Get value via another method 1 – 4mA 2 – 8mA 3 – 12mA ... 255 – 1020mA
15:8	0h RO	**Maximum Current for 3.0V (corecfg_maxcurrent3p0v):** Maximum Current for 3.0V 0 – Get value via another method 1 – 4mA 2 – 8mA 3 – 12mA ... 255 – 1020mA
7:0	0h RO	**Maximum Current for 3.3V (corecfg_maxcurrent3p3v):** Maximum Current for 3.3V 0 – Get value via another method 1 – 4mA 2 – 8mA 3 – 12mA ... 255 – 1020mA

14.2.27 Force Event REGISTER for AUTO CMD Error Status (ForceEventforAUTOCMDErrorStatus)—Offset 50h

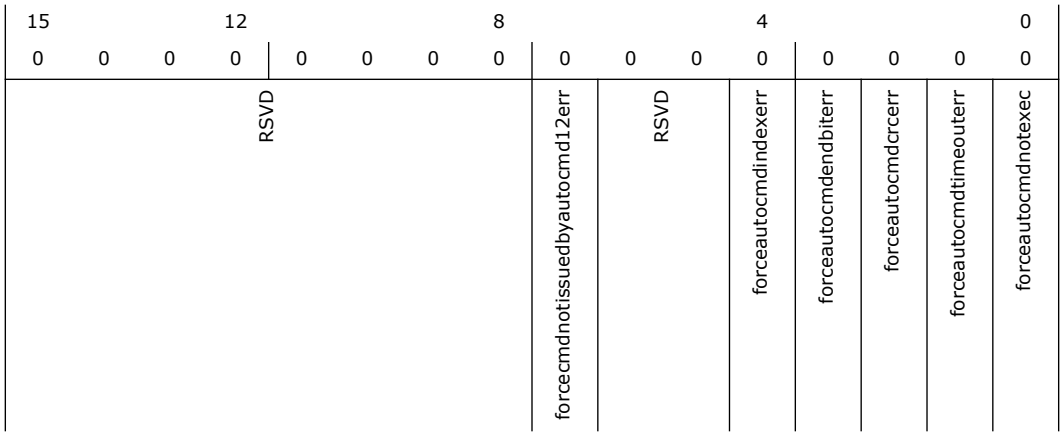
All bits in this register are RO.

Access Method

Type: MEM Register (Size: 16 bits)

Device: 30
Function: 6

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	Reserved.
7	0h	**forcecmdnotissuedbyautocmd12err (forcecmdnotissuedbyautocmd12err):** Force Event for Command Not Issued by AUTO CMD12 Error
6:5	0h RO	Reserved.
4	0h	**forceautocmdindexerr (forceautocmdindexerr):** Force Event for AUTO CMD Index Error
3	0h	**forceautocmdendbiterr (forceautocmdendbiterr):** Force Event for AUTO CMD End Bit Error
2	0h	**forceautocmdcrcerr (forceautocmdcrcerr):** Force Event for AUTO CMD Timeout Error
1	0h	**forceautocmdtimeouterr (forceautocmdtimeouterr):** Force Event for AUTO CMD Timeout Error
0	0h	**forceautocmdnotexec (forceautocmdnotexec):** Force Event for AUTO CMD12 Not Executed

14.2.28 Force Event Register for Error Interrupt Status (forceeventforerrintsts)—Offset 52h

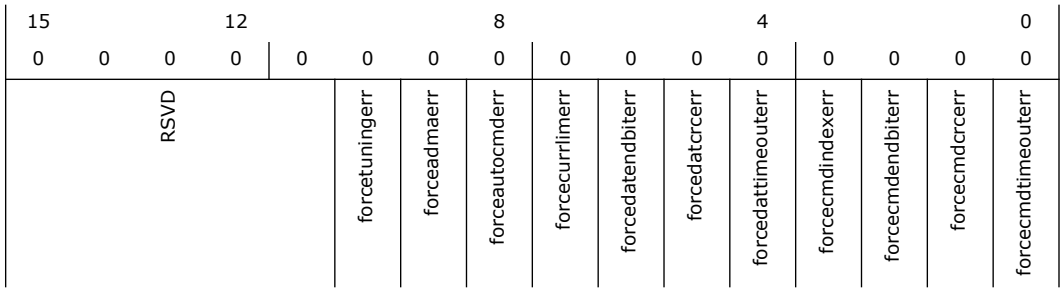
All bits in this register are RO.

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 30
Function: 6

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:11	0h RO	Reserved.
10	0h	**forcetuningerr (forcetuningerr):** Force Event for Tuning Error
9	0h	**forceadmaerr (forceadmaerr):** Force Event for ADMA Error'0' no interrupt, '1' interrupt generated
8	0h	**forceautocmderr (forceautocmderr):** Force Event for Auto CMD Error '0' no interrupt, '1' interrupt generated
7	0h	**forcecurrlimerr (forcecurrlimerr):** Force Event for Current Limit Error '0' no interrupt, '1' interrupt generated
6	0h	**forcedatendbiterr (forcedatendbiterr):** Force Event for Data End Bit Error. '0' no interrupt, '1' interrupt generated
5	0h	**forcedatcrcerr (forcedatcrcerr):** Force Event for Data CRC Error
4	0h	**forcedattimeouterr (forcedattimeouterr):** Force Event for Data Timeout Error '0' no interrupt, '1' interrupt generated
3	0h	**forcecmdindexerr (forcecmdindexerr):** Force Event for Command Index Error
2	0h	**forcecmdendbiterr (forcecmdendbiterr):** Force Event for Command End Bit Error '0' no interrupt, '1' interrupt generated
1	0h	**forcecmdcrcerr (forcecmdcrcerr):** Force Event for Command CRC Error
0	0h	**forcecmdtimeouterr (forcecmdtimeouterr):** Force Event for CMD Timeout Error '0' No interrupt, '1' interrupt generated

14.2.29 ADMA Error Status Register (admaerrsts)—Offset 54h

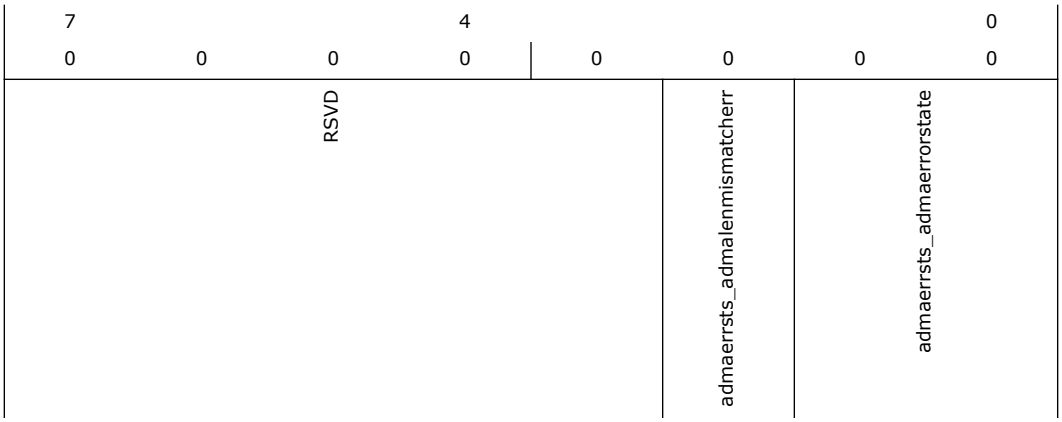
All bits in this register are RO

Access Method

Type: MEM Register
(Size: 8 bits)

Device: 30
Function: 6

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7:3	0h RO	Reserved.
2	0h	**admaerrsts_admalenmismatcherr (admaerrsts_admalenmismatcherr):** ADMA Length Mismatch Error
1:0	0h RO	**ADMA Error State (admaerrsts_admaerrorstate):** This field indicates the state of ADMA when error is occurred during ADMA data transfer. This field never indicates "10" because ADMA never stops in this state. D01 – D00 : ADMA Error State when error occurred Contents of SYS_SDR register 00 - ST_STOP (Stop DMA) Points to next of the error descriptor 01 - ST_FDS (Fetch Descriptor) Points to the error descriptor 10 - Never set this state (Not used) 11 - ST_TFR (Transfer Data) Points to the next of the error descriptor

14.2.30 ADMA System Address Register0&1 (admasysaddr01)—Offset 58h

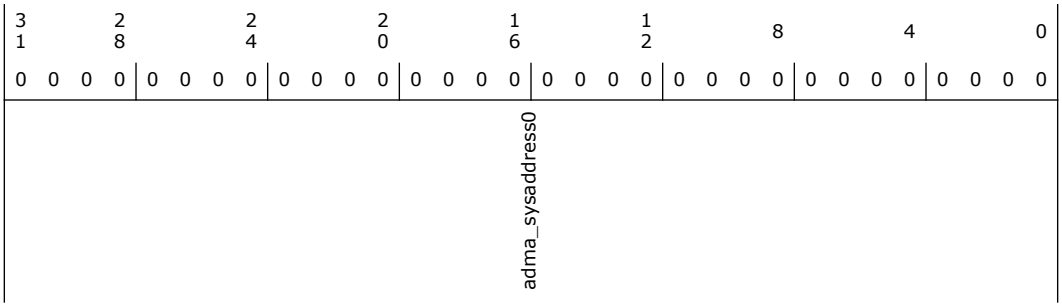
This register contains the physical address used for ADMA data transfer

Access Method

Type: MEM Register (Size: 32 bits)

Device: 30
Function: 6

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**adma_sysaddress0 (adma_sysaddress0):** This register holds byte address of executing command of the Descriptor table.

14.2.31 ADMA System Address Register1 (admasysaddr2)—Offset 5Ch

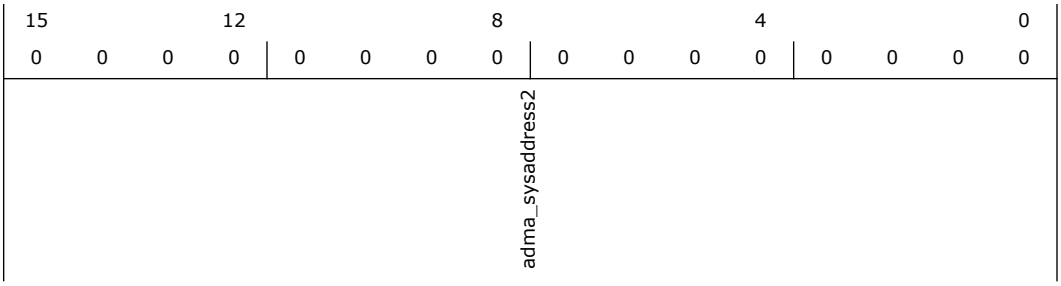
This register contains the physical address used for ADMA data transfer

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 30
Function: 6

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW	**adma_sysaddress2 (adma_sysaddress2):** This register holds byte address of executing command of the Descriptor table.

14.2.32 ADMA System Address Register1 (admasysaddr3)—Offset 5Eh

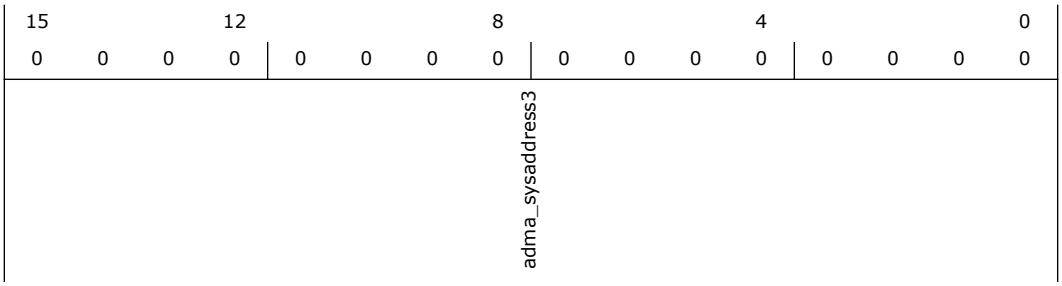
This register contains the physical address used for ADMA data transfer

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 30
Function: 6

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW	**adma_sysaddress3 (adma_sysaddress3):** This register holds byte address of executing command of the Descriptor table.

14.2.33 Preset Value Register for Initialization (Preset Value 0)—Offset 60h

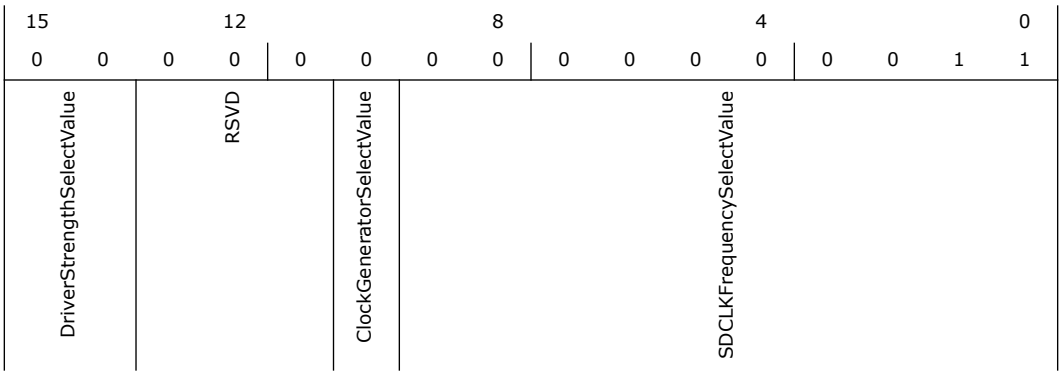
All bits in this register are RO.

Access Method

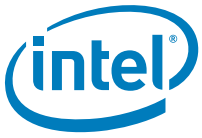
Type: MEM Register
(Size: 16 bits)

Device: 30
Function: 6

Default: 3h



Bit Range	Default & Access	Field Name (ID): Description
15:14	0h	**DriverStrengthSelectValue (DriverStrengthSelectValue):** Driver Strength Select Value
13:11	0h RO	Reserved.
10	0h	**ClockGeneratorSelectValue (ClockGeneratorSelectValue):** This bit is effective when Host Controller supports programmable clock
9:0	3h	**SDCLKFrequencySelectValue (SDCLKFrequencySelectValue):** 10-bit preset value to set SDCLK Frequency Select in the Clock Control Register is described by a host system.



14.2.34 Preset Value Register for Default Speed (Preset Value 1)—Offset 62h

Same description as Preset Value 0 register.

14.2.35 Preset Value Register for High Speed (presetvalue2)—Offset 64h

Same description as Preset Value 0 register.

14.2.36 Preset Value Register for SDR12 (presetvalue3)—Offset 66h

Same description as Preset Value 0 register.

14.2.37 Preset Value Register for SDR25 (presetvalue4)—Offset 68h

Same description as Preset Value 0 register.

14.2.38 Preset Value Register for SDR50 (presetvalue5)—Offset 6Ah

Same description as Preset Value 0 register.

14.2.39 Preset Value Register for SDR104 (presetvalue6)—Offset 6Ch

Same description as Preset Value 0 register.

14.2.40 Preset Value Register for DDR50 (presetvalue7)—Offset 6Eh

Same description as Preset Value 0 register.

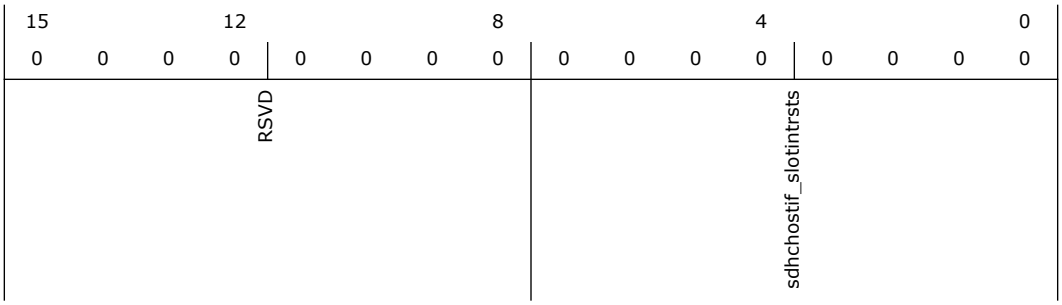
14.2.41 Slot Interrupt Status Register (slotintrsts)—Offset FCh

This register is used to read the interrupt signal for each slot.

Access Method

Type: MEM Register (Size: 16 bits)	**Device:** 30 **Function:** 6

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	Reserved.
7:0	0h RO	**sdhchostif_slotintrsts (sdhchostif_slotintrsts):** These status bits indicate the logical OR of Interrupt signal and Wakeup signal for each slot.

14.2.42 Host Controller Version Register (hostcontrollerver)—Offset FEh

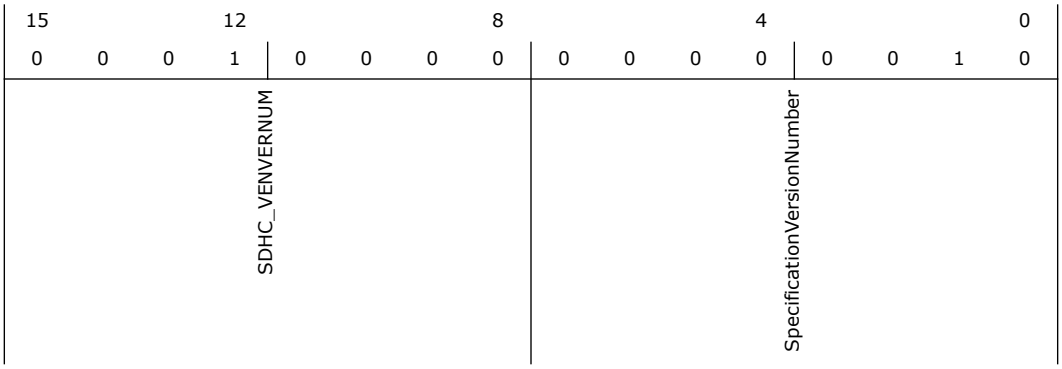
This register is used to read the vendor version number and specification version number

Access Method

Type: MEM Register (Size: 16 bits)

Device: 30
Function: 6

Default: 1002h



Bit Range	Default & Access	Field Name (ID): Description
15:8	10h RO	**SDHC_VENVERNUM (SDHC_VENVERNUM):** This status is reserved for the vendor version number.
7:0	2h RO	**SpecificationVersionNumber (SpecificationVersionNumber):** This status indicates the Host Controller Spec. Version. The upper and lower 4-bits indicate the version.

14.3 SDXC Additional Registers Summary

These registers are memory mapped based on BAR0 defined in PCI configuration space.

Table 14-3. Summary of SDXC Additional Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
804h	807h	Software LTR Value (SW_LTR_val)—Offset 804h	800h
808h	80Bh	Auto LTR Value (Auto_LTR_val)—Offset 808h	800h
810h	813h	Capabilities Bypass (Cap_byps)—Offset 810h	0h
814h	817h	(Cap_byps_reg1)—Offset 814h	3001EF3Ch
818h	81Bh	(Cap_byps_reg2)—Offset 818h	4004000h
81Ch	81Fh	(reg_D0i3)—Offset 81Ch	0h
820h	823h	(Tx_CMD_dly)—Offset 820h	400h
824h	827h	(Tx_DATA_dly_1)—Offset 824h	A18h
828h	82Bh	(Tx_DATA_dly_2)—Offset 828h	1C1C1C00h
82Ch	82Fh	(Rx_CMD_Data_dly_1)—Offset 82Ch	1C1C1C00h
830h	833h	(Rx_Strobe_Ctrl_Path)—Offset 830h	500h
834h	837h	(Rx_CMD_Data_dly_2)—Offset 834h	181Ch
838h	83Bh	(Master_Dll)—Offset 838h	1h
840h	843h	(Auto_tuning)—Offset 840h	0h

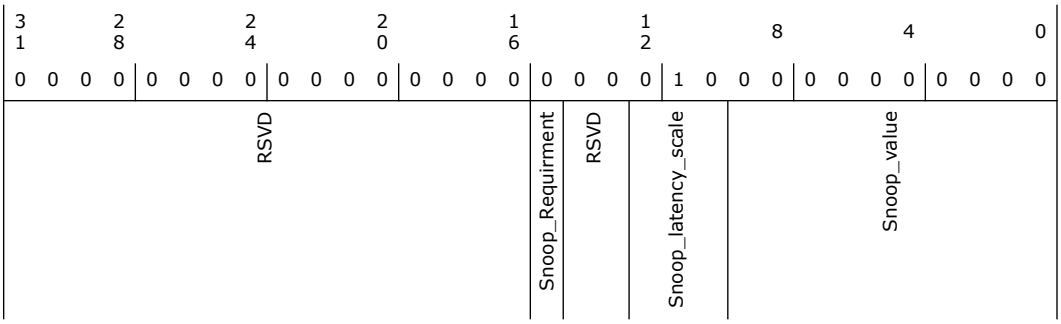
14.3.1 Software LTR Value (SW_LTR_val)—Offset 804h

Access Method

Type: MEM Register (Size: 32 bits)

Device: 30
Function: 6

Default: 800h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	0h RW	**Snoop_Requirment:** If the Requirement (bit 15) is clear, that indicates that the device has no LTR requirement for this type of traffic (i.e. it can wait for service indefinitely). If the 10-bit latency value is zero it indicates that the device cannot tolerate any delay and needs the best possible service/response time.
14:13	0h RO	Reserved.
12:10	2h RW	**Snoop_latency_scale:** Support for codes 010 (1us) or 011 (32us) for Snoop Latency Scale(1us -) 32ms total span) only. Writes to this CSR which dont match those values will be dropped completely, next read will return previous value.
9:0	0h RW	**Snoop_value:** 10-bit latency value

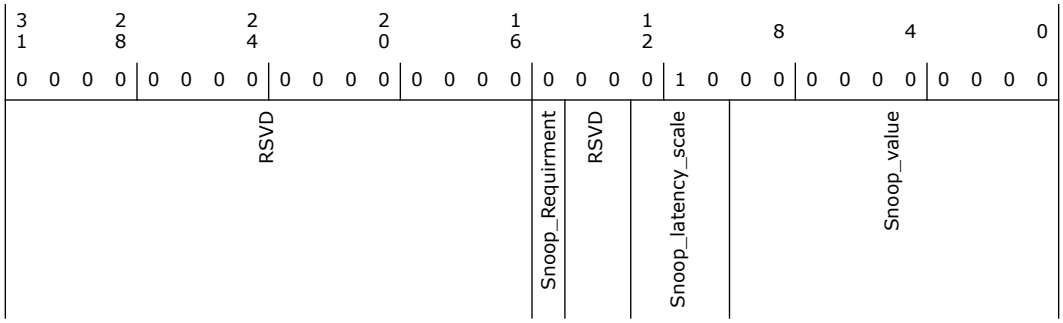
14.3.2 Auto LTR Value (Auto_LTR_val)—Offset 808h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 6

Default: 800h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	0h RW	**Snoop_Requirment:** If the Requirement (bit 15) is clear, that indicates that the device has no LTR requirement for this type of traffic (i.e. it can wait for service indefinitely). If the 10-bit latency value is zero it indicates that the device cannot tolerate any delay and needs the best possible service/response time.
14:13	0h RO	Reserved.
12:10	2h RW	**Snoop_latency_scale:** Support for codes 010 (1us) or 011 (32us) for Snoop Latency Scale(1us -) 32ms total span) only. Writes to this CSR which dont match those values will be dropped completely, next read will return previous value.
9:0	0h RW	**Snoop_value:** 10-bit latency value

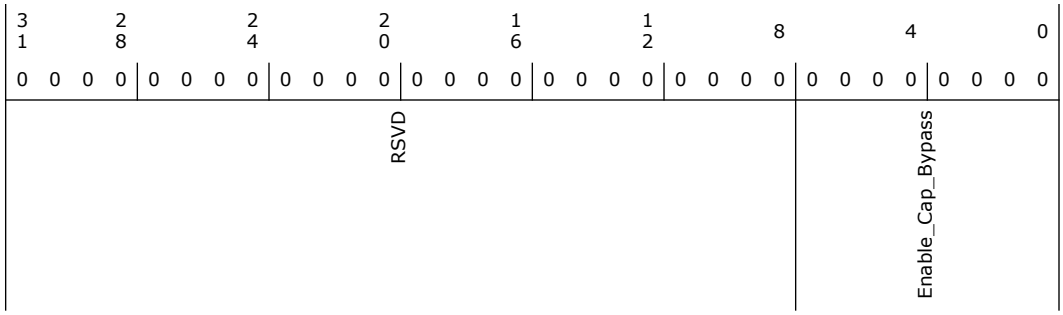
14.3.3 Capabilities Bypass (Cap_byps)—Offset 810h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 6

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	0h RW	**Capabilities Bypass Enable (Enable_Cap_Bypass):** 5Ah: Enable Capabilities Bypass. All others: Capabilities Bypass Disable (using default values)

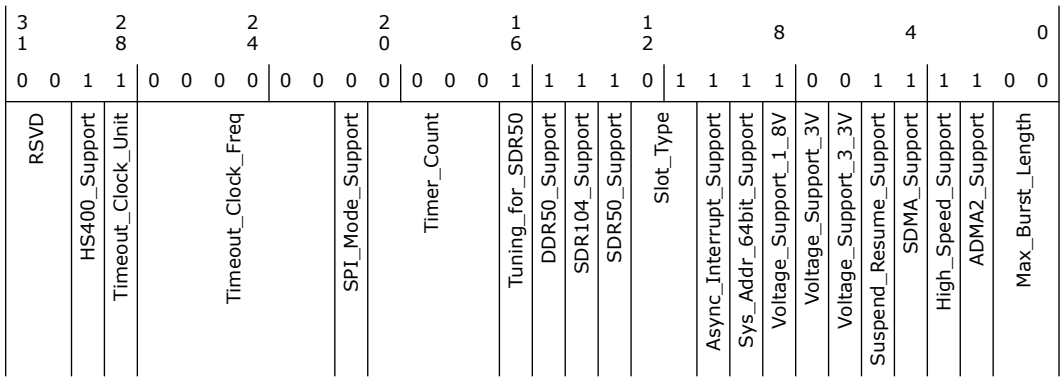
14.3.4 (Cap_byps_reg1)—Offset 814h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 6

Default: 3001EF3Ch



Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29	1h RW	**HS400_Support:** 1: HS400 Mode Supported. 0: HS400 Mode NOT Supported
28	1h RW	**Timeout_Clock_Unit:** 1: to Select MHz Clock 0: to Select KHz Clock
27:22	0h RW	**Timeout_Clock_Freq:** Timeout clock frequency
21	0h RW	**SPI_Mode_Support:** SPI Mode Support 1: SPI Mode Supported 0: SPI Mode Not Supported
20:17	0h RW	**Timer_Count:** Timer Count for Re-Tuning This is the Timer Count for Re-Tuning Timer for Re-Tuning Mode 1 to 3. Setting to 0 disables Re-Tuning Timer
16	1h RW	**Tuning_for_SDR50:** Use Tuning for SDR50 1: Use Tuning 0: Do not use Tuning
15	1h RW	**DDR50_Support:** 1: DDR50 Mode Supported. 0: DDR50 Mode NOT Supported
14	1h RW	**SDR104_Support:** 1: SDR104 Mode Supported. 0: SDR104 Mode NOT Supported
13	1h RW	**SDR50_Support:** 1: SDR50 Mode Supported. 0: SDR50 Mode NOT Supported
12:11	1h RW	**Slot_Type:** 00: Removable SD Card Slot. 01: Embedded Slot for One Device. 10: Shared Bus Slot. 11: Reserved
10	1h RW	**Async_Interrupt_Support:** 1: Asynchronous Interrupt Supported. 0: Asynchronous Interrupt NOT Supported
9	1h RW	**Sys_Addr_64bit_Support:** 1: Core supports 64-bit System Address Bus. 0: Core supports only 32-bit System Address Bus
8	1h RW	**Voltage_Support_1_8V:** 1: 1.8V Supported. 0: 1.8V NOT Supported
7	0h RW	**Voltage_Support_3V:** 1: 3.0V Supported. 0: 3.0V NOT Supported
6	0h RW	**Voltage_Support_3_3V:** 1: 3.3V Supported. 0: 3.3V NOT Supported
5	1h RW	**Suspend_Resume_Support:** 1: Suspend/Resume Supported. 0: Suspend/Resume NOT Supported
4	1h RW	**SDMA_Support:** 1: SDMA mode Supported. 0: SDMA mode NOT Supported

Bit Range	Default & Access	Field Name (ID): Description
3	1h RW	**High_Speed_Support:** 1: HIGH_SPEED mode Supported. 0: HIGH_SPEED mode NOT Supported
2	1h RW	**ADMA2_Support:** 1: ADMA2 mode Supported. 0: ADMA2 mode NOT Supported
1:0	0h RW	**Max_Burst_Length:** Maximum Block Length supported by the Core/Device. 00: 512 (Bytes) 01: 1024 10: 2048. 11: Reserved

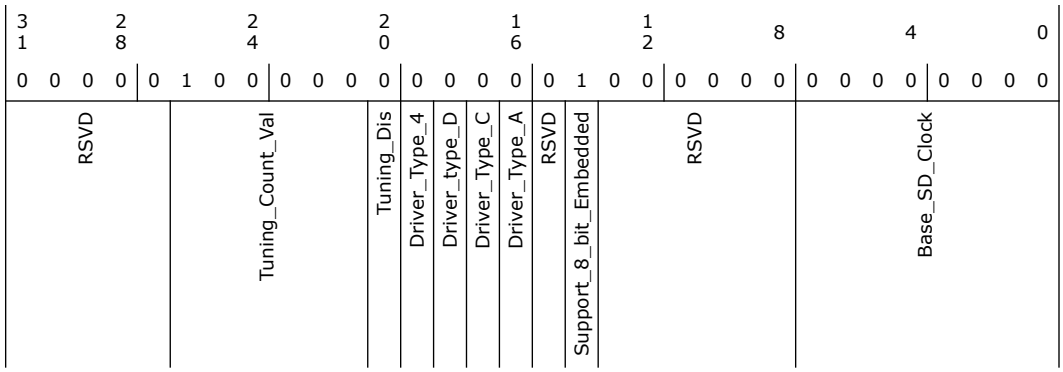
14.3.5 (Cap_byps_reg2)—Offset 818h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 6

Default: 4004000h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	Reserved.
26:21	20h RW	**Tuning_Count_Val:** Tuning Count Value Configures the Number of Taps (Phases) of the rxclk_in that is supported. The Tuning State machine uses this information to select one of the Taps (Phases) of the rxclk_in during the Tuning Procedure.
20	0h RW	**Tuning_Dis:** Disable the 1.5x Tuning count when calculating total tuning count. The internal tuning count will be set to the corecfg_Tuningcount when this signal is asserted
19	0h RW	**Driver_Type_4:** Driver Type 4 Support 1: Supported 0: NOT Supported
18	0h RW	**Driver_type_D:** Driver Type D Support 1: Supported 0: NOT Supported
17	0h RW	**Driver_Type_C:** Driver Type C Support 1: Supported 0: NOT Supported

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**Driver_Type_A:** Driver Type A Support 1: Supported 0: NOT Supported
15	0h RO	Reserved.
14	1h RW	**Support_8_bit_Embedded:** 8-bit Support for Embedded Device 1: Supported 0: NOT Supported
13:8	0h RO	Reserved.
7:0	0h RW	**Base_SD_Clock:** Base Clock Frequency for SD Clock

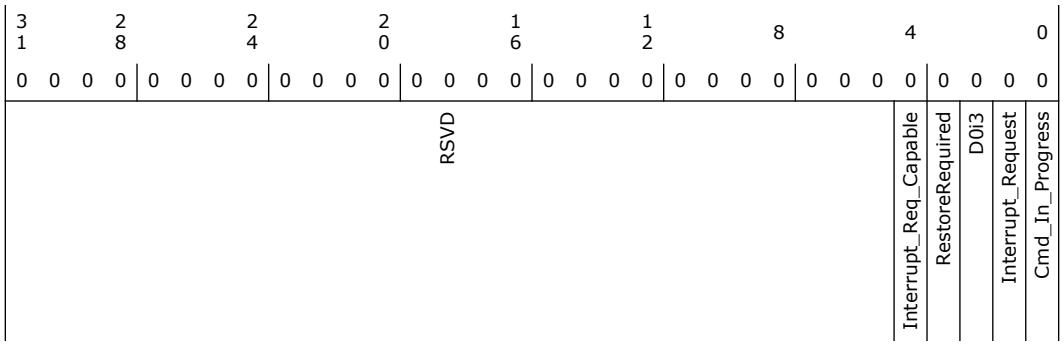
14.3.6 (reg_D0i3)—Offset 81Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 6

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4	0h RO	**Interrupt_Req_Capable:** 0: HW not capable to issue in interrupt on command completion. 1: HW capable to issue an interrupt on command completion
3	0h RO	**RestoreRequired:** When set (by HW), SW must restore state to the IP. The state may have been lost due to a reset or full power lost. SW clears the bit by writing a 1. This bit will be set on initial power up.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**D0i3:** SW sets this bit to 1 to move the IP into the D0i3 state. Writing this bit to 0 will return the IP to the fully active D0 state (D0i0).
1	0h RO	**Interrupt_Request:** SW sets this bit to 1 to ask for an interrupt to be generated on completion of the command. SW must clear or set this on each write to this register. Not supported in SCS!
0	0h RO	**Cmd_In_Progress:** HW sets this bit on a 1->0 or 0->1 transition of bit [2]. While set, the other bits in this register are not valid and it is illegal for SW to write to any bit in this register. When clear all the other bits in the register are valid and SW may write to any bit. If Interrupt Request bit [1] was set for the current command, HW may clear this bit before the interrupt has been made visible to SW, since when SW actually handles

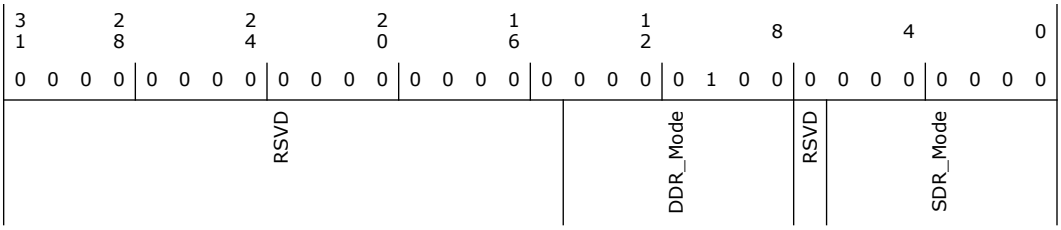
14.3.7 (Tx_CMD_dly)—Offset 820h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 6

Default: 400h



Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RO	Reserved.
14:8	4h RW	**DDR_Mode:** Tx CMD Delay (DDR Mode). 0 - 39: Select number of active delay elements. Each = 125pSec. 40 - 127: Reserved
7	0h RO	Reserved.
6:0	0h RW	**SDR_Mode:** Tx CMD Delay (SDR Mode). 0 - 39: Select number of active delay elements. Each = 125pSec. 40 - 127: Reserved

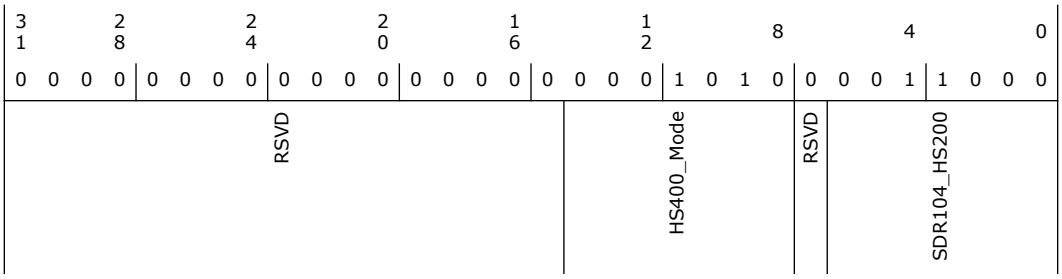
14.3.8 (Tx_DATA_dly_1)—Offset 824h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 6

Default: A18h



Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RO	Reserved.
14:8	Ah RW	**HS400_Mode:** Tx Data Delay (HS400 Mode). 0 - 78: Select number of active delay elements. Each = 125pSec. 79 - 127: Reserved
7	0h RO	Reserved.
6:0	18h RW	**SDR104_HS200:** Tx Data Delay (SDR104/HS200 Mode) 0 - 79: Select the required delay, as a multiple of 125pSec. 80 - 127: Reserved

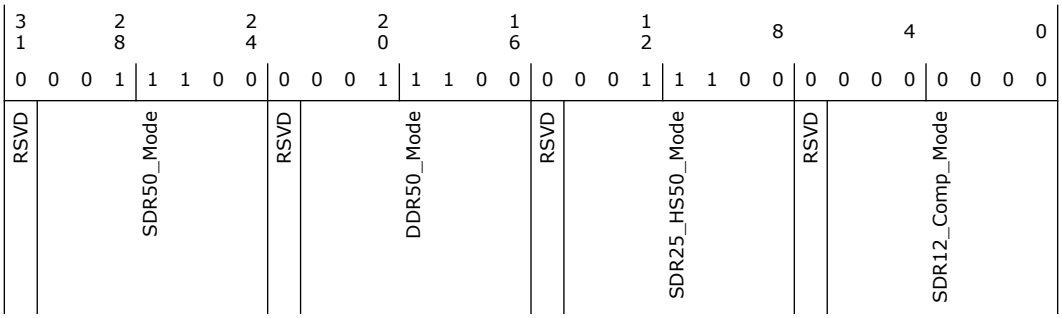
14.3.9 (Tx_DATA_dly_2)—Offset 828h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 6

Default: 1C1C1C00h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	Reserved.
30:24	1Ch RW	**SDR50_Mode:** Tx Data Delay (SDR50 Mode) 0 - 79: Select the required delay, as a multiple of 125pSec. 80 - 127: Reserved
23	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
22:16	1Ch RW	**DDR50_Mode:** Tx Data Delay (DDR50 Mode). 0 - 78: Select number of active delay elements. Each = 125pSec. 79 - 127: Reserved
15	0h RO	Reserved.
14:8	1Ch RW	**SDR25_HS50_Mode:** Tx Data Delay (SDR25/HS50 Mode) 0 - 79: Select the required delay, as a multiple of 125pSec. 80 - 127: Reserved
7	0h RO	Reserved.
6:0	0h RW	**SDR12_Comp_Mode:** Tx Data Delay (SDR12/Compatibility Mode) 0 - 79: Select the required delay, as a multiple of 125pSec. 80 - 127: Reserved

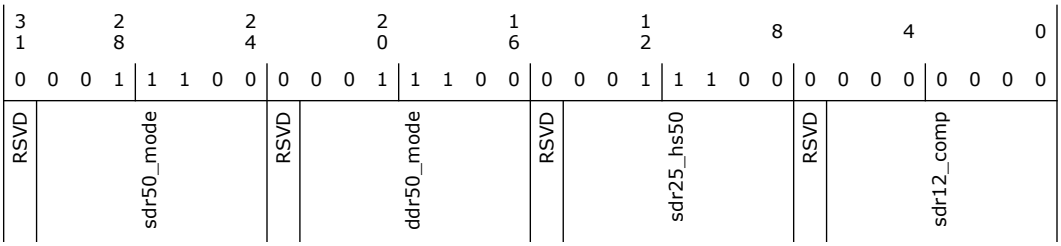
14.3.10 (Rx_CMD_Data_dly_1)—Offset 82Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 6

Default: 1C1C1C00h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	Reserved.
30:24	1Ch RW	**sdr50_mode:** Rx CMD + Data Delay (SDR50 Mode). 0-79: Select the required delay, as a multiple of 125pSec. 80-127: Reserved
23	0h RO	Reserved.
22:16	1Ch RW	**ddr50_mode:** Rx CMD + Data Delay (DDR50 Mode). 0-78: Select number of active delay elements. Each = 125pSec. 79-127: Reserved
15	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
14:8	1Ch RW	**sdr25_hs50:** Rx CMD + Data Delay (SDR25/HS50 Mode) 0-79: Select the required delay, as a multiple of 125pSec. 80-127: Reserved
7	0h RO	Reserved.
6:0	0h RW	**sdr12_comp:** Rx CMD + Data Delay (SDR12/Compatibility Mode) 0-79: Select the required delay, as a multiple of 125pSec. 80-127: Reserved

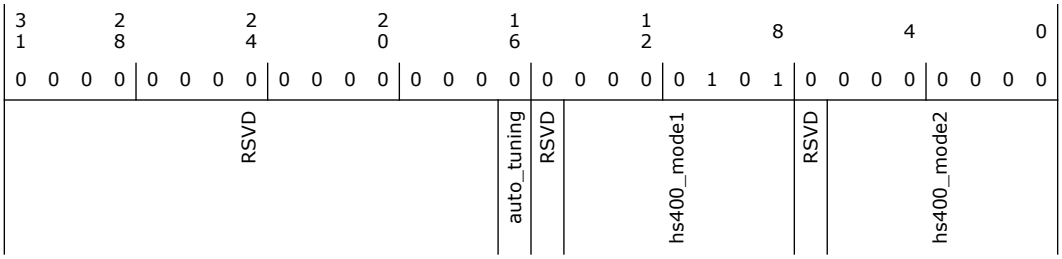
14.3.11 (Rx_Strobe_Ctrl_Path)—Offset 830h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 6

Default: 500h



Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	Reserved.
16	0h RW	**auto_tuning:** Enable Auto Tuning for HS400 Strobe Path 0: Auto Tuning Disabled 1: Auto Tuning Enabled
15	0h RO	Reserved.
14:8	5h RW	**hs400_mode1:** Rx Strobe Delay DLL 1(HS400 Mode) 0-39: Select number of active delay elements. Each = 125pSec 0-63 - Reserved
7	0h RO	Reserved.
6:0	0h RW	**hs400_mode2:** Rx Strobe Delay DLL 2(HS400 Mode) 0-39: Select number of active delay elements. Each = 125pSec 40-63 - Reserved

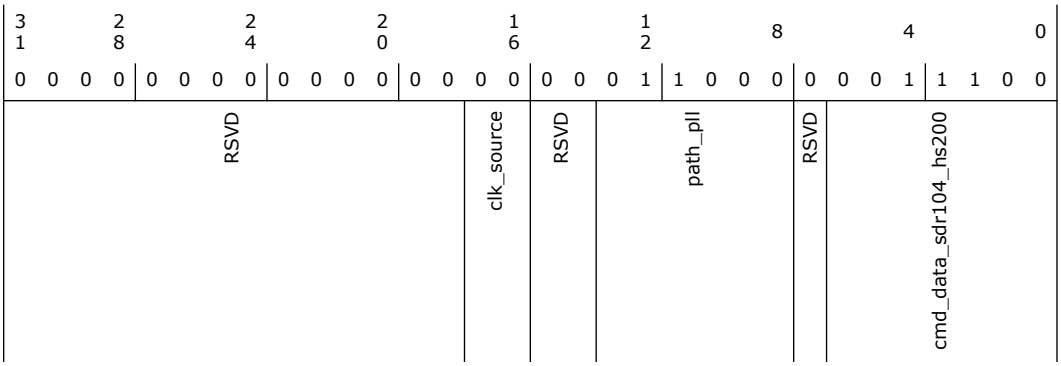
14.3.12 (Rx_CMD_Data_dly_2)—Offset 834h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 6

Default: 181Ch



Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17:16	0h RW	**clk_source:** Clock Source for Rx Path 00: Rx Clock after Output Buffer 01: Rx Clock before Output Buffer 10: Automatic Selection based on Working mode (HS 200 before buffer, all others after buffer) 11 - Reserved
15:14	0h RO	Reserved.
13:8	18h RW	**path_pll:** Rx Path PLL #3 Delay value For Auto Tuning Mode 0-39 - Select the required delay, as a multiple of 125pSec. 40 – 63: Reserved
7	0h RO	Reserved.
6:0	1Ch RW	**cmd_data_sdr104_hs200:** Rx CMD + Data Delay (SDR104/HS200 Mode) 0-79: Select the required delay, as a multiple of 125pSec. 80-127: Reserved

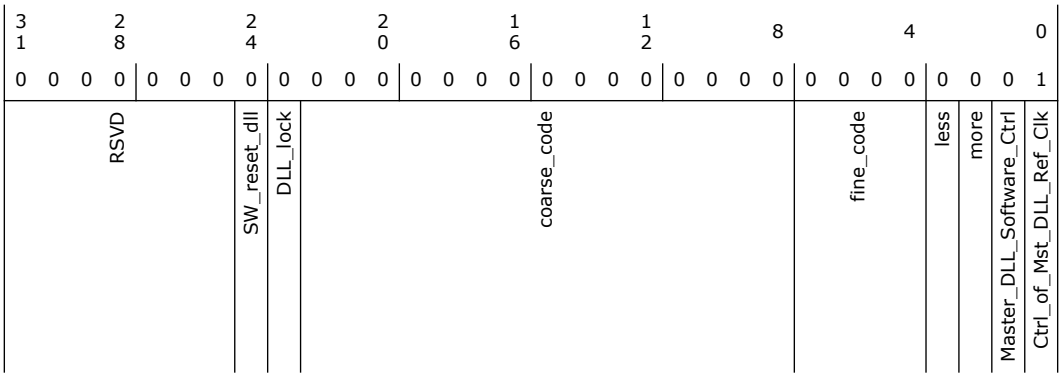
14.3.13 (Master_Dll)—Offset 838h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 6

Default: 1h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	Reserved.
24	0h RO	**SW_reset_dll:** SW reset for Master DLL 0: No SW Reset for Master DLL 1: Force Reset for Master DLL
23	0h RO	**DLL_lock:** Master DLL Lock Indication
22:8	0h RW	**coarse_code:** Set coarse code to DLL. (only valid when Software control is Enabled)
7:4	0h RW	**fine_code:** Set fine code to DLL. (only valid when Software control is Enabled)
3	0h RO/V	**less:** Phase Detection Less Indication
2	0h RO/V	**more:** Phase Detector More Indication
1	0h RW	**Master_DLL_Software_Ctrl:** Master DLL Software Ctrl. 0: Master DLL Automatic Control (SW Control Disabled). 1: Master DLL Software Control Enabled
0	1h RW	**Ctrl_of_Mst_DLL_Ref_Clk:** Ctrl of Master DLL Ref Clock. 0 - Clock is Disabled. 1 - Clock is Enabled

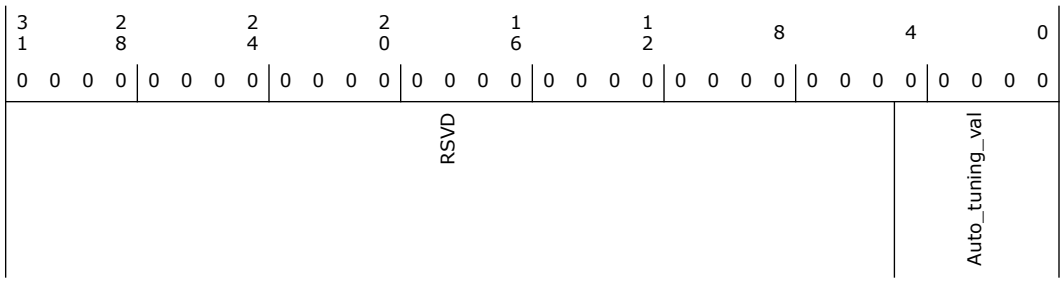
14.3.14 (Auto_tuning)—Offset 840h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 30
Function: 6

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4:0	0h RO	**Auto_tuning_val**

§ §

15 PCI Express* (PCIe*) Interface (D29:F0–F7, D28:F0–F7 and D27:F0–F3)

15.1 PCI Express* Port Configuration Registers Summary

There are twelve sets of the following configuration registers used for PCH PCI Express* Port Configurations. Each PCH PCI Express* Configuration Register set covers a single PCI Express* Port and maps out as the following Device/Function:
D28/F0 = Port1
D28/F1 = Port2
D28/F2 = Port3
D28/F3 = Port4
D28/F4 = Port5
D28/F5 = Port6
D28/F6 = Port7
D28/F7 = Port8
D29/F0 = Port9
D29/F1 = Port10
D29/F2 = Port11
D29/F3 = Port12

Table 15-1. Summary of PCI Express* Port Configuration Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	Identifiers (ID)—Offset 0h	8086h
4h	7h	Device Command; Primary Status (CMD_PSTS)—Offset 4h	100000h
8h	Bh	Revision ID;Class Code (RID_CC)—Offset 8h	60400F0h
Ch	Fh	Cache Line Size; Primary Latency Timer; Header Type (CLS_PLT_HTYPE)—Offset Ch	810000h
18h	1Bh	Bus Numbers; Secondary Latency Timer (BNUM_SLT)—Offset 18h	0h
1Ch	1Fh	I/O Base and Limit; Secondary Status (IOBL_SSTS)—Offset 1Ch	0h
20h	23h	Memory Base and Limit (MBL)—Offset 20h	0h
24h	27h	Prefetchable Memory Base and Limit (PMBL)—Offset 24h	10001h
28h	2Bh	Prefetchable Memory Base Upper 32 Bits (PMBU32)—Offset 28h	0h
2Ch	2Fh	Prefetchable Memory Limit Upper 32 Bits (PMLU32)—Offset 2Ch	0h
34h	37h	Capabilities List Pointer (CAPP)—Offset 34h	40h
3Ch	3Fh	Interrupt Information; Bridge Control (INTR_BCTRL)—Offset 3Ch	0h
40h	43h	Capabilities List; PCI Express Capabilities (CLIST_XCAP)—Offset 40h	428010h
44h	47h	Device Capabilities (DCAP)—Offset 44h	8001h
48h	4Bh	Device Control; Device Status (DCTL_DSTS)—Offset 48h	100000h
4Ch	4Fh	Link Capabilities (LCAP)—Offset 4Ch	710C00h

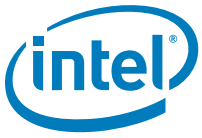


Table 15-1. Summary of PCI Express* Port Configuration Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
50h	53h	Link Control; Link Status (LCTL_LSTS)—Offset 50h	10000h
54h	57h	Slot Capabilities (SLCAP)—Offset 54h	40060h
58h	5Bh	Slot Control; Slot Status (SLCTL_SLSTS)—Offset 58h	0h
5Ch	5Fh	Root Control (RCTL)—Offset 5Ch	0h
60h	63h	Root Status (RSTS)—Offset 60h	0h
64h	67h	Device Capabilities 2 (DCAP2)—Offset 64h	80837h
68h	6Bh	Device Control 2; Device Status 2 (DCTL2_DSTS2)—Offset 68h	0h
6Ch	6Fh	Link Capabilities 2 (LCAP2)—Offset 6Ch	0h
70h	73h	Link Control 2; Link Status 2 (LCTL2_LSTS2)—Offset 70h	1h
80h	83h	Message Signaled Interrupt Identifiers; Message Signaled Interrupt Message Control (MID_MC)—Offset 80h	9005h
84h	87h	Message Signaled Interrupt Message Address (MA)—Offset 84h	0h
88h	8Bh	Message Signaled Interrupt Message Data (MD)—Offset 88h	0h
90h	93h	Subsystem Vendor Capability (SVCAP)—Offset 90h	A00Dh
94h	97h	Subsystem Vendor IDs (SVID)—Offset 94h	0h
A0h	A3h	Power Management Capability; PCI Power Management Capabilities (PMCAP_PMC)—Offset A0h	C8030001h
A4h	A7h	PCI Power Management Control And Status (PMCS)—Offset A4h	8h
D4h	D7h	Miscellaneous Port Configuration 2 (MPC2)—Offset D4h	0h
D8h	DBh	Miscellaneous Port Configuration (MPC)—Offset D8h	1110000h
DCh	DFh	SMI / SCI Status (SMSCS)—Offset DCh	0h
F0h	F3h	IOSF Primary Control And Status (IPCS)—Offset F0h	0h
FCh	FFh	Additional Configuration 1 (STRPFUSECFG)—Offset FCh	0h
100h	103h	Advanced Error Extended Reporting Capability Header (AECH)—Offset 100h	0h
104h	107h	Uncorrectable Error Status (UES)—Offset 104h	0h
108h	10Bh	Uncorrectable Error Mask (UEM)—Offset 108h	0h
10Ch	10Fh	Uncorrectable Error Severity (UEV)—Offset 10Ch	60011h
110h	113h	Correctable Error Status (CES)—Offset 110h	0h
114h	117h	Correctable Error Mask (CEM)—Offset 114h	2000h
118h	11Bh	Advanced Error Capabilities and Control (AECC)—Offset 118h	0h
12Ch	12Fh	Root Error Command (REC)—Offset 12Ch	0h
130h	133h	Root Error Status (RES)—Offset 130h	0h
134h	137h	Error Source Identification (ESID)—Offset 134h	0h
144h	147h	ACS Capability Register (ACSCAPR)—Offset 144h	Fh
148h	14Bh	ACS Control Register (ACSCTLR)—Offset 148h	0h
200h	203h	L1 Sub-States Extended Capability Header (L1SECH)—Offset 200h	0h
204h	207h	L1 Sub-States Capabilities (L1SCAP)—Offset 204h	28281Fh
208h	20Bh	L1 Sub-States Control 1 (L1SCTL1)—Offset 208h	0h
20Ch	20Fh	L1 Sub-States Control 2 (L1SCTL2)—Offset 20Ch	28h
220h	223h	Secondary PCI Express Extended Capability Header (SPEECH)—Offset 220h	0h

Table 15-1. Summary of PCI Express* Port Configuration Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
224h	227h	Link Control 3 (LCTL3)—Offset 224h	0h
22Ch	22Fh	Lane 0 and Lane 1 Equalization Control (L01EC)—Offset 22Ch	7F7F7F7Fh
230h	233h	Lane 2 and Lane 3 Equalization Control (L23EC)—Offset 230h	7F7F7F7Fh
324h	327h	PCI Express Configuration (PCIEDBG)—Offset 324h	2000000h
338h	33Bh	PCI Express Additional Link Control (PCIEALC)—Offset 338h	0h
400h	403h	Additional Configuration 2 (LTROVR)—Offset 400h	0h
404h	407h	Additional Configuration 3 (LTROVR2)—Offset 404h	0h
420h	423h	Additional Configuration 4 (PCIEPMECTL)—Offset 420h	0h
450h	453h	Equalization Configuration 1 (EQCFG1)—Offset 450h	0h
454h	457h	Remote Transmitter Preset/Coefficient List 1 (RTPCL1)—Offset 454h	0h
458h	45Bh	Remote Transmitter Preset/Coefficient List 2 (RTPCL2) (RTPCL2)—Offset 458h	0h

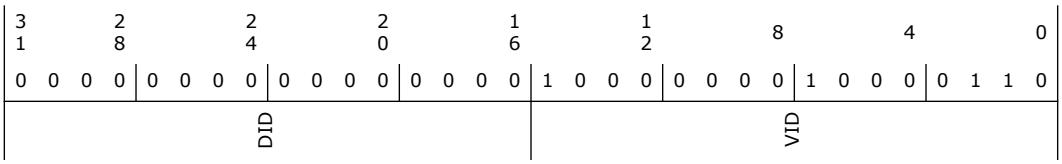
15.1.1 Identifiers (ID)—Offset 0h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 8086h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO/V	**Device Identification (DID):** The value of this ID is product specific.
15:0	8086h RO	**Vendor Identification (VID):** Indicates Intel

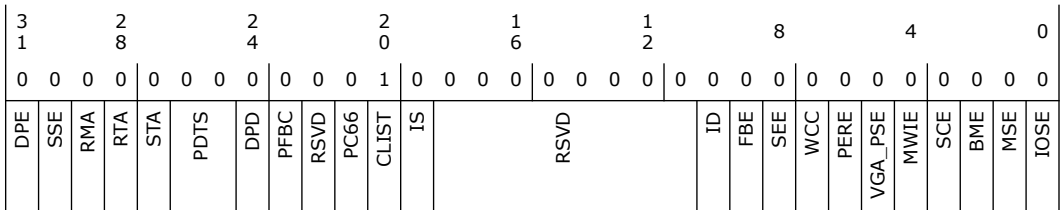
15.1.2 Device Command; Primary Status (CMD_PSTS)—Offset 4h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 100000h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C/V	**DPE - Detected Parity Error (DPE):** Set when the root port receives a command or data from the backbone with a parity error. This is set even if CMD.PERE is not set.
30	0h RW/1C/V	**Signaled System Error (SSE):** Set when the root port signals a system error to the internal SERR# logic.
29	0h RW/1C/V	**Received Master Abort (RMA):** Set when the root port receives a completion with unsupported request status from the backbone.
28	0h RW/1C/V	**Received Target Abort (RTA):** Set when the root port receives a completion with completer abort from the backbone.
27	0h RW/1C/V	**Signaled Target Abort (STA):** Set whenever the root port forwards a target abort received from the downstream device onto the backbone.
26:25	0h RO	**Primary DEVSEL# Timing Status (PDTS):** Reserved per PCI-Express spec
24	0h RW/1C/V	**Master Data Parity Error Detected (DPD):** Set when the root port receives a completion with a data parity error on the backbone and CMD.PERE is set.
23	0h RO	**Primary Fast Back to Back Capable (PFBC):** Reserved per PCI-Express spec.
22	0h RO	Reserved.
21	0h RO	**Primary 66 MHz Capable (PC66):** Reserved per PCI-Express spec.
20	1h RO	**Capabilities List (CLIST):** Indicates the presence of a capabilities list.
19	0h RO/V	**Interrupt Status (IS):** Indicates status of hot plug and power management interrupts on the root port that result in INTx# message generation. This bit is not set if MSI is enabled. If MSI is not enabled, this bit is set regardless of the state of CMD.ID.
18:11	0h RO	Reserved.
10	0h RW/V2	**Interrupt Disable (ID):** This disables pin-based INTx# interrupts on enabled hot plug and power management events. This bit has no effect on MSI operation. When set, internal INTx# messages will not be generated. When cleared, internal INTx# messages are generated if there is an interrupt for hot plug or power management and MSI is not enabled. This bit does not affect interrupt forwarding from devices connected to the root port. Assert_INTx and Deassert_INTx messages will still be forwarded to the internal interrupt controllers if this bit is set. For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register is RO and returns a value of 0 when read, else it is RW with the functionality described above.
9	0h RO	**Fast Back to Back Enable (FBE):** Reserved per PCI-Express spec.
8	0h RW	**SERR# Enable (SEE):** When set, enables the root port to generate an SERR# message when PSTS.SSE is set.
7	0h RO	**Wait Cycle Control (WCC):** Reserved per PCI-Express spec.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**Parity Error Response Enable (PERE):** Indicates that the device is capable of reporting parity errors as a master on the backbone.
5	0h RO	**VGA Palette Snoop (VGA_PSE):** Reserved per PCI-Express spec.
4	0h RO	**Memory Write and Invalidate Enable (MWIE):** Reserved per PCI-Express spec.
3	0h RO	**Special Cycle Enable (SCE):** Reserved per PCI-Express and PCI bridge spec.
2	0h RW	**Bus Master Enable (BME):** When set, allows the root port to forward Memory and I/O Read/Write cycles onto the backbone from a PCI-Express device. When this bit is 0b, Memory and I/O requests received at a Root Port must be handled as Unsupported Requests (UR). This bit does not affect forwarding of Completions in either the Upstream or Downstream direction. The forwarding of Requests other than Memory or I/O requests is not controlled by this bit.
1	0h RW	**Memory Space Enable (MSE):** When set, memory cycles within the range specified by the memory base and limit registers can be forwarded to the PCI-Express device. When cleared, these memory cycles are master aborted on the backbone.
0	0h RW	**I/O Space Enable (IOSE):** When set, I/O cycles within the range specified by the I/O base and limit registers can be forwarded to the PCI-Express device. When cleared, these cycles are master aborted on the backbone..

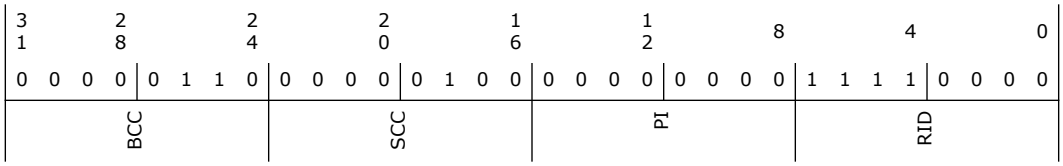
15.1.3 Revision ID;Class Code (RID_CC)—Offset 8h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 60400F0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	6h RO	**Base Class Code (BCC):** Indicates the device is a bridge device.
23:16	4h RO/V	**Sub-Class Code (SCC):** The default indicates the device is a PCI-to-PCI bridge. If the MPC.BT register is set to a '1' fora Host Bridge, this register reads 00h.
15:8	0h RO/V	**Programming Interface (PI):** The value reported in this register is a function of the Decode Control.Subtractive Decode Enable (SDE) register. SDE Value reported in this register 0: 00h 1: 01h
7:0	F0h RO/V	**Revision ID (RID):** Indicates stepping of the host controller. Refer to Device and Revision ID table in Vol1 for specific value.

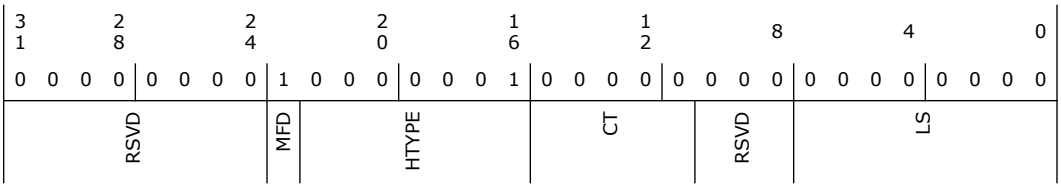
15.1.4 Cache Line Size; Primary Latency Timer; Header Type (CLS_PLT_HTYPE)—Offset Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 810000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	1h RO	**Multi-function Device (MFD):** This bit is '1' toindicate a multi-function device.
22:16	1h RO/V	**Header Type (HTYPE):** The default mode identifies the header layout of the configuration space, which is a PCI-to-PCI bridge. If the MPC.BT register is set to a '1' fora Host Bridge, this register reads 00h.
15:11	0h RO	**Latency Count (CT):** Reserved per PCI-Express spec
10:8	0h RO	Reserved.
7:0	0h RW	**Line Size (LS):** This is read/write but contains no functionality, per PCI-Express spec

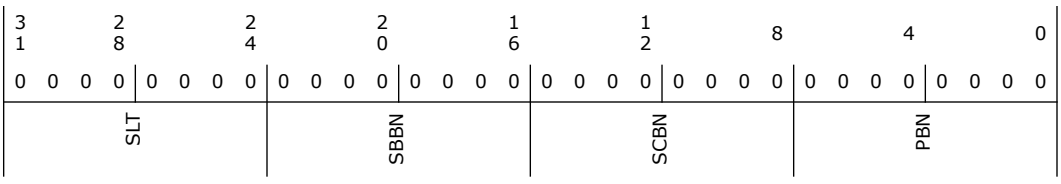
15.1.5 Bus Numbers; Secondary Latency Timer (BNUM_SLT)—Offset 18h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW/V2	**Secodary Latency Timer (SLT):** For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is a RW register; else this register is RO and returns 0. This register does not affect the behavior of any HW logic.
23:16	0h RW	**Subordinate Bus Number (SBBN):** Indicates the highest PCI bus number below the bridge.
15:8	0h RW	**Secondary Bus Number (SCBN):** Indicates the bus number the port.
7:0	0h RW	**Primary Bus Number (PBN):** Indicates the bus number of the backbone.

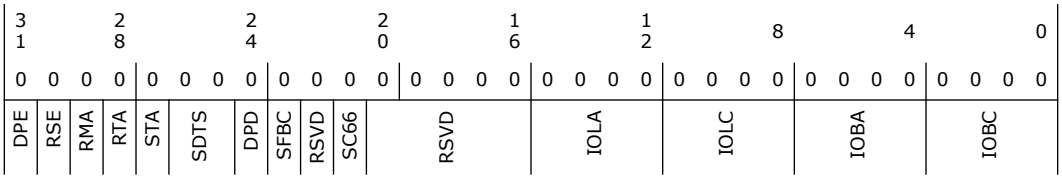
15.1.6 I/O Base and Limit; Secondary Status (IOBL_SSTS)—Offset 1Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C/V	**Detected Parity Error (DPE):** Set when the port receives a poisoned TLP.
30	0h RW/1C/V	**Received System Error (RSE):** Set when the port receives an ERR_FATAL or ERR_NONFATAL message from the device.
29	0h RW/1C/V	**Received Master Abort (RMA):** Set when the port receives a completion with 'Unsupported Request' status from the device.
28	0h RW/1C/V	**Received Target Abort (RTA):** Set when the port receives a completion with 'Completion Abort' status from the device.
27	0h RW/1C/V	**Signaled Target Abort (STA):** Set when the port generates a completion with 'Completion Abort' status to the device.
26:25	0h RO/V	**Secondary DEVSEL# Timing Status (SDTS):** Reserved per PCI-Express spec For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register returns a value of 01b when read, else this register returns a value of 00b.
24	0h RW/1C/V	**Data Parity Error Detected (DPD):** Set when the BCTRL.PERE, and either of the following two conditions occurs: Port receives completion marked poisoned. Port poisons a write request to the secondary side.
23	0h RO/V	**Secondary Fast Back to Back Capable (SFBC):** Reserved per PCI Express spec For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register returns a value of 1b when read, else this register returns a value of 0b.
22	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RO	**Secondary 66 MHz Capable (SC66):** Reserved per PCI Express spec
20:16	0h RO	Reserved.
15:12	0h RW	**I/O Address Limit (IOLA):** I/O Base bits corresponding to address lines 15:12 for 4KB alignment. Bits 11:0 are assumed to be padded to FFFh.
11:8	0h RO	**I/O Limit Address Capability (IOLC):** Indicates that the bridge does not support 32-bit I/O addressing.
7:4	0h RW	**I/O Base Address (IOBA):** I/O Base bits corresponding to address lines 15:12 for 4KB alignment. Bits 11:0 are assumed to be padded to 000h.
3:0	0h RO	**I/O Base Address Capability (IOBC):** Indicates that the bridge does not support 32-bit I/O addressing.

15.1.7 Memory Base and Limit (MBL)—Offset 20h

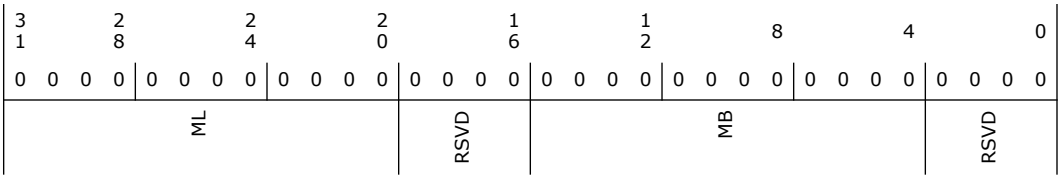
Accesses that are within the ranges specified in this register will be sent to the attached device if CMD.MSE is set. Accesses from the attached device that are outside the ranges specified will be forwarded to the backbone if CMD.BME is set. The comparison performed is MB [gt]= AD[lb]31:20[rb] [lt]= ML.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**Memory Limit (ML):** These bits are compared with bits 31:20 of the incoming address to determine the upper 1MB aligned value of the range.
19:16	0h RO	Reserved.
15:4	0h RW	**Memory Base (MB):** These bits are compared with bits 31:20 of the incoming address to determine the lower 1MB aligned value of the range.
3:0	0h RO	Reserved.

15.1.8 Prefetchable Memory Base and Limit (PMBL)—Offset 24h

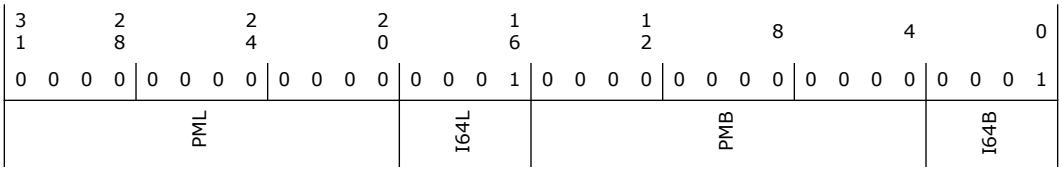
Accesses that are within the ranges specified in this register will be sent to the device if CMD.MSE is set. Accesses from the device that are outside the ranges specified will be forwarded to the backbone if CMD.BME is set. The comparison performed is PMBU32:PMB[gt]= AD[lb]63:32[rb]:AD[lb]31:20[rb] [lt]= PMLU32:PML.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 10001h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**Prefetchable Memory Limit (PML):** These bits are compared with bits 31:20 of the incoming address to determine the upper 1MB aligned value of the range.
19:16	1h RO	**64-bit Indicator (I64L):** Indicates support for 64-bit addressing.
15:4	0h RW	**Prefetchable Memory Base (PMB):** These bits are compared with bits 31:20 of the incoming address to determine the lower 1MB aligned value of the range.
3:0	1h RO	**64-bit Indicator (I64B):** Indicates support for 64-bit addressing.

15.1.9 Prefetchable Memory Base Upper 32 Bits (PMBU32)—Offset 28h

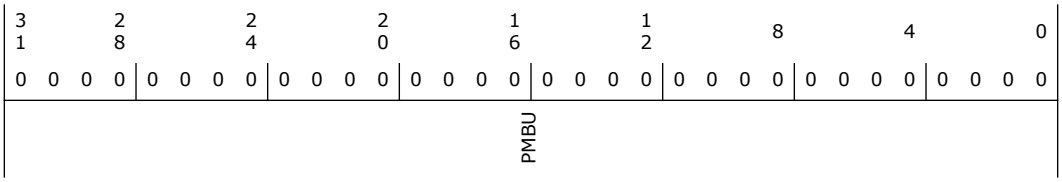
Size:32 bits

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Prefetchable Memory Base Upper Portion (PMBU):** Upper 32-bits of the prefetchable address base.

15.1.10 Prefetchable Memory Limit Upper 32 Bits (PMLU32)—Offset 2Ch

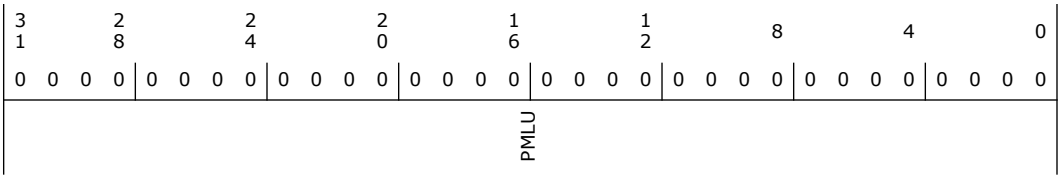
Size:32 bits

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Prefetchable Memory Limit Upper Portion (PMLU):** Upper 32-bits of the prefetchable address limit.

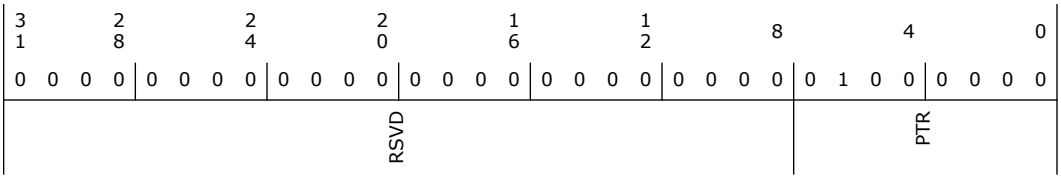
15.1.11 Capabilities List Pointer (CAPP)—Offset 34h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 40h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	40h RW/O	**Capabilities Pointer (PTR):** Indicates that the pointer for the first entry in the capabilities list. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value. Capability Linked List (Default Settings) OffsetCapability Next Pointer 40h PCI Express 80h 80h Message Signaled Interrupt (MSI) 90h 90h Subsystem Vendor A0h A0h PCI Power Management 00h Extended PCIe Capability Linked List OffsetCapability Next Pointer 100h Advanced Error Reporting 000h

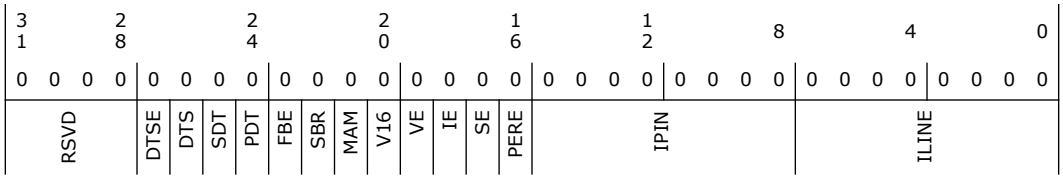
15.1.12 Interrupt Information; Bridge Control (INTR_BCTRL)—Offset 3Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	Reserved.
27	0h RW/V2	**Discard Timer SERR# Enable (DTSE):** Reserved per PCI-Express spec. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port.
26	0h RO	**Discard Timer Status (DTS):** Reserved per PCI-Express spec. For PCI Bus Emulation Mode compatibility, this register can remain RO as no secondary discard timer exists that will ever cause it to be set.
25	0h RW/V2	**Secondary Discard Timer (SDT):** Reserved per Express spec. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port.
24	0h RW/V2	**Primary Discard Timer (PDT):** Reserved per Express spec. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port.
23	0h RO	**Fast Back to Back Enable (FBE):** Reserved per Express spec.

Bit Range	Default & Access	Field Name (ID): Description
22	0h RW	**Secondary Bus Reset (SBR):** Triggers a Hot Reset on the PCI-Express port.
21	0h RW/V2	**Master Abort Mode (MAM):** Reserved per Express spec. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port.
20	0h RW	**VGA 16-Bit Decode (V16):** When set, indicates that the I/O aliases of the VGA range (see BCTRL:VEdefinition below), are not enabled. 0: Execute 10-bit address decode on VGA I/O accesses. 1: Execute 16-bit address decode on VGA I/O accesses.
19	0h RW	**VGA Enable (VE):** When set, the following ranges will be claimed off the backbone by the root port: Memory ranges A0000h-BFFFFh I/O ranges 3B0h 3BBh and 3C0h 3DFh, and all aliases of bits 15:10 in any combination of 1's
18	0h RW	**ISA Enable (IE):** This bit only applies to I/O addresses that are enabled by the I/O Base and I/O Limit registers and are in the first 64KB of PCI I/O space. If this bit is set, the root port will block any forwarding from the backbone to the device of I/O transactions addressing the last 768 bytes in each 1KB block (offsets 100h to 3FFh).
17	0h RW	**SERR# Enable (SE):** When set, ERR_COR, ERR_NONFATAL, and ERR_FATAL messages received are forwarded to the backbone. When cleared, they are not.
16	0h RW	**Parity Error Response Enable (PERE):** When set, poisoned write TLPs and completions indicating poisoned TLPs will set the SSTS.DPD.
15:8	0h RO/V	**Interrupt Pin (IPIN):** Indicates the interrupt pin driven by the root port. At reset, this register takes on the following values, which reflect the reset state of the STRPFUSECFG register in chipset config space: Port Bits[lb]15:12[rb] Bits[lb]11:08[rb] 1 0h STRPFUSECFG.P1IP 2 0h STRPFUSECFG.P2IP 3 0h STRPFUSECFG.P3IP 4 0h STRPFUSECFG.P4IP 5 0h STRPFUSECFG.P5IP 6 0h STRPFUSECFG.P6IP 7 0h STRPFUSECFG.P7IP 8 0h STRPFUSECFG.P8IP The value that is programmed into STRPFUSECFG.PxIP is always reflected in this register. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register returns a value of 00h when read, else this register returns the value from the table above.
7:0	0h RW	**Interrupt Line (ILINE):** Software written value to indicate which interrupt line (vector) the interrupt is connected to. No hardware action is taken on this register.

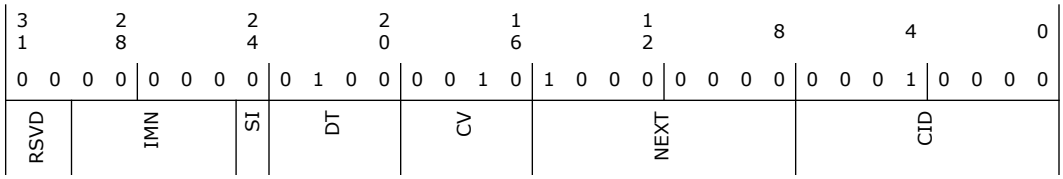
15.1.13 Capabilities List; PCI Express Capabilities (CLIST_XCAP)—Offset 40h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 428010h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29:25	0h RO	**Interrupt Message Number (IMN):** The root port does not have multiple MSI interrupt numbers.
24	0h RW/O	**Slot Implemented (SI):** Indicates whether the root port is connected to a slot. Slot support is platform specific. BIOS programs this field, and it is maintained until a platform reset.
23:20	4h RO	**Device / Port Type (DT):** Indicates this is a PCI-Express root port
19:16	2h RO	**Capability Version (CV):** Version 2.0 indicates devices compliant to the PCI Express 2.0 specification which incorporates the Register Expansion ECN.
15:8	80h RW/O	**Next Capability (NEXT):** Indicates the location of the next capability. The default value of this register is 80h which points to the MSI Capability structure. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value.
7:0	10h RO	**Capability ID (CID):** Indicates this is a PCI Express capability

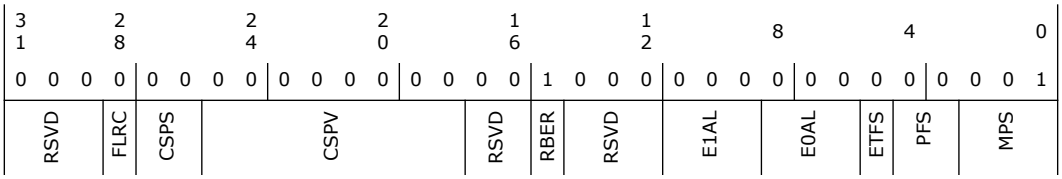
15.1.14 Device Capabilities (DCAP)—Offset 44h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 8001h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	Reserved.
28	0h RO	**Function Level Reset Capable (FLRC):** Not supported in Root Ports
27:26	0h RO	**Captured Slot Power Limit Scale (CSPS):** Not supported
25:18	0h RO	**Captured Slot Power Limit Value (CSPV):** Not supported
17:16	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
15	1h RO	**Role Based Error Reporting (RBER):** When Set, this bit indicates that the Function implements the functionality originally defined in the Error Reporting ECN for PCI Express Base Specification, Revision 1.0a, and later incorporated into PCI Express Base Specification, Revision 1.1. This bit must be Set by all Functions conforming to the ECN, PCI Express Base Specification, Revision 1.1, or subsequent PCI Express Base Specification revisions.
14:12	0h RO	Reserved.
11:9	0h RO	**Endpoint L1 Acceptable Latency (E1AL):** Reserved for root ports.
8:6	0h RO	**Endpoint L0 Acceptable Latency (E0AL):** Reserved for Root port.
5	0h RO	**Extended Tag Field Supported (ETFS):** The root port never needs to initiate a transaction as a Requester with the Extended Tag bits being set. This bit does not affect the root port's ability to forward requests as a bridge as the root port always supports forwarding requests with extended tags.
4:3	0h RO	**Phantom Functions Supported (PFS):** No phantom functions supported
2:0	1h RW/O	**Max Payload Size Supported (MPS):** BIOS should write to this field during system initialization. Only Max Payload Size of up to 256B is supported. Programming this field to any values other than 128B max payload size will result in aliasing to 128B max payload size. 000b: 128 bytes max payload size. 001b: 256 bytes max payload size. 010b: 512 bytes max payload size. 011b: 1024 bytes max payload size. 100b: 2048 bytes max payload size. 101b: 4096 bytes max payload size. 110b: Reserved. 111b: Reserved. This field applies only to the PCIe link interface.

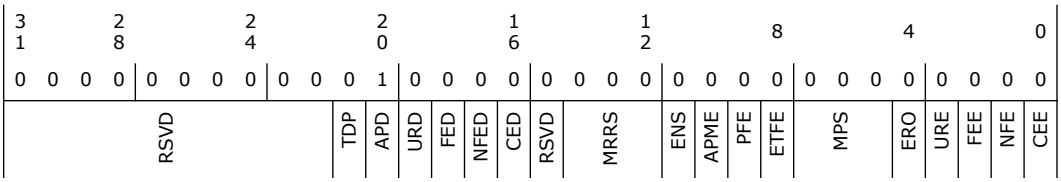
15.1.15 Device Control; Device Status (DCTL_DSTS)—Offset 48h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 100000h



Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	Reserved.
21	0h RO	**Transactions Pending (TDP):** This bit has no meaning for the root port since it never initiates a non-posted request with its own Requester ID.
20	1h RO	**AUX Power Detected (APD):** The root port contains AUX power for wakeup

Bit Range	Default & Access	Field Name (ID): Description
19	0h RW/1C/V	**Unsupported Request Detected (URD):** Indicates an unsupported request was detected.
18	0h RW/1C/V	**Fatal Error Detected (FED):** Indicates a fatal error was detected. Set when a fatal error occurred on from a data link protocol error, buffer overflow, or malformed tlp
17	0h RW/1C/V	**Non-Fatal Error Detected (NFED):** Indicates a non-fatal error was detected. Set when an received a non-fatal error occurred from a poisoned tlp, unexpected completions, unsupported requests, completor abort, or completer timeout
16	0h RW/1C/V	**Correctable Error Detected (CED):** Indicates a correctable error was detected. Set when received an internal correctable error from receiver errors / framing errors, tlp crc error, dllp crc error, replay num rollover, replay timeout.
15	0h RO	Reserved.
14:12	0h RO	**Max Read Request Size (MRRS):** Hardwired to 0. This field applies only to the PCIe link interface.
11	0h RO	**Enable No Snoop (ENS):** Not supported. The root port will never issue non-snoop requests.
10	0h RW/P	**Aux Power PM Enable (APME):** The OS will set this bit to '1' ifthe device connected has detected aux power.
9	0h RO	**Phantom Functions Enable (PFE):** Not supported
8	0h RO	**Extended Tag Field Enable (ETFE):** Not supported
7:5	0h RW	**Max Payload Size (MPS):** The root port only supports up to 256B max payload. Programming this field to any values other than 128B or 256B max payload size will result in aliasing to 128B max payload size. If the DCAP.MPS indicates 128B max payload size support, programming this field to any values other than 128B will result in aliasing to 128B max payload size. Programming this field to any values greater than DCAP.MPS will result in aliasing to 128B max payload size. 000b: 128 bytes max payload size. 001b: 256 bytes max payload size. 010b: 512 bytes max payload size. 011b: 1024 bytes max payload size. 100b: 2048 bytes max payload size. 101b: 4096 bytes max payload size. 110b: Reserved. 111b: Reserved. This field applies only to the PCIe link interface. Note: Software should ensure that the system is quiescent and no TLP is in progress prior to changing this field. BIOS should program this field prior to enabling BME.
4	0h RO	**Enable Relaxed Ordering (ERO):** Not supported
3	0h RW	**Unsupported Request Reporting Enable (URE):** When set, allows signaling ERR_NONFATAL, ERR_FATAL, or ERR_COR to the Root Control register when detecting an unmasked Unsupported Request (UR). An ERR_COR is signaled when aunmasked Advisory Non-Fatal UR is received. An ERR_FATAL, ERR_or NONFATAL, is sent to the Root Control Register when an uncorrectable non-Advisory UR is received with the severity set by the Uncorrectable Error Severity register.
2	0h RW	**Fatal Error Reporting Enable (FEE):** enablessignaling of ERR_FATAL to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.
1	0h RW	**Non-Fatal Error Reporting Enable (NFE):** When set, enables signaling of ERR_NONFATAL to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.
0	0h RW	**Correctable Error Reporting Enable (CEE):** When set, enables signaling of ERR_CORR to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.

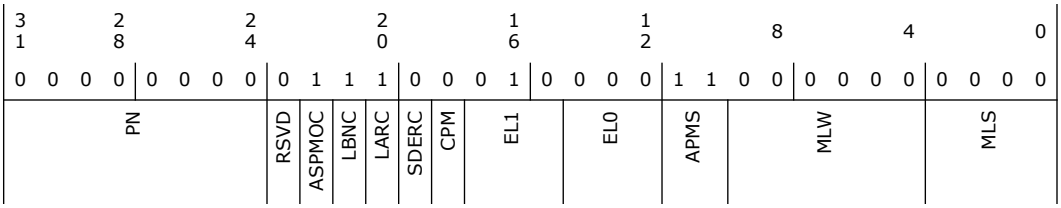
15.1.16 Link Capabilities (LCAP)—Offset 4Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 710C00h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO/V	**Port Number (PN):** Indicates the port number for the root port. This value is different for each implemented port: Port # Value of PN field 1 01h 2 02h 3 03h 4 04h
23	0h RO	Reserved.
22	1h RW/O	**ASPM Optionality Compliance (ASPMOC):** ASPM Optionality Compliance(ASPMOC): This bit must be set to 1b for PCIe 3.0 compliant port. Components implemented against certain earlier versions of this specificationwill have this bit set to 0b. Software is permitted to use the value of this bit to help determinewhether to enable ASPM or whether to run ASPM compliance tests.
21	1h RO	**Link Bandwidth Notification Capability (LBNC):** This port supports Link Bandwidth Notification status and interrupt mechanisms.
20	1h RO	**Link Active Reporting Capable (LARC):** This port supports the optional capability of reporting the DL_Active state of the Data Link Control and Management State Machine.
19	0h RO	**Surprise Down Error Reporting Capable (SDERC):** Set to '0' to indicate the root port does not support Surprise Down Error Reporting
18	0h RO	**Clock Power Management (CPM):** '0' Indicatesthat root ports do not support the CLKREQ# mechanism.
17:15	2h RW/O	**L1 Exit Latency (EL1):** Indicates an exit latency of 2us to 4us. 000b Less than 1 us 001b 1 us to less than 2 us 010b 2 us to less than 4 us 011b 4 us to less than 8 us 100b 8 us to less than 16 us 101b 16 us to less than 32 us 110b 32 us to 64 us 111b More than 64 us Note: If PXP PLL shutdown is enabled, BIOS should program this latency to comprehend PLL lock latency.
14:12	0h RO/V	**L0s Exit Latency (EL0):** Indicates an exit latency based upon common-clock configuration: LCTL.CCC Value 0 MPC.UCEL 1 MPC.CCEL

Bit Range	Default & Access	Field Name (ID): Description
11:10	3h RW/O	**Active State Link PM Support (APMS):** Indicates the level of active state power management on this link Bits Definition 00 No ASPM Supported 01 L0s Supported 10 L1 Supported 11 L0s and L1 supported Note: If STRPFUSECFG.ASPMDIS is 1, the default of this field is '01'. Otherwise, the default of this field is '11'. If STRPFUSECFG.ASPMDIS is 1, BIOS writing '11' to this field will have the same effect as writing '01'. '01' will be reflected on this register when read and the register will turn to Read-Only once written once.
9:4	0h RO/V	**Maximum Link Width (MLW):** For the root ports, several values can be taken, based upon the value of the chipset configuration register field RPC.PC1 for ports 1-4: Port # Value of PN field RPC.PC1 00 01 10 11 1 01h 02h 02h 04h 2 01h 01h 01h 01h 3 01h 01h 02h 01h 4 01h 01h 01h 01h
3:0	0h RO/V	**Max Link Speeds (MLS):** Indicates the supported link speeds of the Root Port. 0001b 2.5 GT/s Link speed supported 0010b 5.0 GT/s and 2.5GT/s Link speeds supported This register reports a value of 0001b if the Root Port Gen2 Disable Fuse is set or the MPC.PCIEGEN2DIS bit is set, else this register reports a value of 0010b. Max Link Speeds (MLS): This field indicates the maximum Link speed of the associated Port. The encoded value specifies a bit location in the Supported Link Speeds Vector (in the Link Capabilities 2 register) that corresponds to the maximum Link speed. Defined encodings are: 0001b: Supported Link Speeds Vector field bit 0. 0010b: Supported Link Speeds Vector field bit 1. 0011b: Supported Link Speeds Vector field bit 2. 0100b: Supported Link Speeds Vector field bit 3. 0101b: Supported Link Speeds Vector field bit 4. 0110b: Supported Link Speeds Vector field bit 5. 0111b: Supported Link Speeds Vector field bit 6. All other encodings are reserved. This register reports a value of 0001b if GEN1 data rate is supported but both GEN2 and GEN3 data rate support are disabled through Fuse or MPC.PCIESD register. This register reports a value of 0010b if both GEN1 and GEN2 data rate are supported but GEN3 data rate support is disabled through Fuse or MPC.PCIESD register.

15.1.17 Link Control; Link Status (LCTL_LSTS)—Offset 50h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 10000h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
LABS	LBMS	LA	SCC	LT	RSVD	NLW						CLS				RSVD				LABIE	LBMIE	HAWD	ECPM	ES	CCC	RL	LD	RCBC	RSVD	ASPM	

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C/V	**Link Autonomous Bandwidth Status (LABS):** This bit is Set by hardware to indicate that hardware has autonomously changed Link speed or width, without the Port transitioning through DL_Down status, for reasons other than to attempt to correct unreliable Link operation. This bit must be set if the Physical Layer reports a speed or width change was initiated by the Downstream component that was indicated as an autonomous change. The default value of this bit is 0b.
30	0h RW/1C/V	**Link Bandwidth Management Status (LBMS):** This bit is Set by hardware to indicate that either of the following has occurred without the Port transitioning through DL_Down status: - A Link retraining has completed following a write of 1b to the Retrain Link bit Note: This bit is Set following any write of 1b to the Retrain Link bit, including when the Link is in the process of retraining for some other reason. - Hardware has changed Link speed or width to attempt to correct unreliable Link operation, either through an LTSSM timeout or a higher level process This bit must be set if the Physical Layer reports a speed or width change was initiated by the Downstream component that was not indicated as an autonomous change. The default value of this bit is 0b.
29	0h RO/V	**Link Active (LA):** Set to 1b when the Data Link Control and Management State Machine is in the DL_Active state, 0b otherwise.
28	0h RO/V	**Slot Clock Configuration (SCC):** In normal mode, root port uses the same reference clock as on the platform and does not generate its own clock. Note: The default of this register bit is dependent on the 'PCIe Non-Common Clock With SSC Mode Enable Strap'. If the strap enables non-common clock with SSC support, this bit shall default to '0'. Otherwise, this bit shall default to '1'.
27	0h RO/V	**Link Training (LT):** The root port sets this bit whenever link training is occurring, or that 1b was written to the Retrain Link bit but Link training has not yet begun. It clears the bit upon completion of link training.
26	0h RO	Reserved.
25:20	0h RO/V	**Negotiated Link Width (NLW):** For the root ports, this register could take on several values: Port # Value of PN field RPC.PC1 00 01 10 11 1 01h 02h 02h 04h 2 01h 01h 01h 01h 3 01h 01h 02h 01h 4 01h 01h 01h 01h The value of this register is undefined if the link has not successfully trained.
19:16	1h RO/V	**Current Link Speed (CLS):** 0001b Link is 2.5Gb/s Link 0010b 5.0 GT/s Link This field indicates the negotiated Link speed of the given link. The encoded value specifies a bit location in the Supported Link Speeds Vector (in the Link Capabilities 2 register) that corresponds to the current Link speed. Defined encodings are: 0001b: Supported Link Speeds Vector field bit 0. 0010b: Supported Link Speeds Vector field bit 1. 0011b: Supported Link Speeds Vector field bit 2. 0100b: Supported Link Speeds Vector field bit 3. 0101b: Supported Link Speeds Vector field bit 4. 0110b: Supported Link Speeds Vector field bit 5. 0111b: Supported Link Speeds Vector field bit 6. All other encodings are reserved. The value of this field is undefined if the link is not up.
15:12	0h RO	Reserved.
11	0h RW	**Link Autonomous Bandwidth Interrupt Enable (LABIE):** Link Autonomous Bandwidth Interrupt Enable - When Set, this bit enables the generation of an interrupt to indicate that the Link Autonomous Bandwidth Status bit has been Set.
10	0h RW	**Link Bandwidth Management Interrupt Enable (LBMIE):** When Set, this bit enables the generation of an interrupt to indicate that the Link Bandwidth Management Status bit has been Set. This bit is not applicable and is reserved for Endpoints, PCI Express-to-PCI/PCI-X bridges, and Upstream Ports of Switches. Functions that do not implement the Link Bandwidth Notification Capability must hardwire this bit to 0b. Default value of this bit is 0b.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Hardware Autonomous Width Disable (HAWD):** When Set, this bit disables hardware from changing the Link width for reasons other than attempting to correct unreliable Link operation by reducing Link width. Default value of this bit is 0b. Note: When operating as PCI Express, this bit defines the value of the Link Upconfigure Capability in TS2 Ordered Sets.
8	0h RO	**Enable Clock Power Management (ECPM):** Reserved. Not supported on Root Ports.
7	0h RW	**Extended Synch (ES):** When set, forces extended transmission of FTS ordered sets in FTS and extra TS2 at exit from L1 prior to entering L0. Note: This functionality is not applicable for Mobile Express.
6	0h RW	**Common Clock Configuration (CCC):** When set, indicates that the root port and device are operating with a distributed common reference clock.
5	0h WO	**Retrain Link (RL):** When set, the root port will train its downstream link. This bit always returns '0' whenread. Software uses LSTS.LT to check the status of training. It is permitted to write 1b to this bit while simultaneously writing modified values to other fields in this register. If the LTSSM is not already in Recovery or Configuration, the resulting Link training must use the modified values. If the LTSSM is already in Recovery or Configuration, the modified values are not required to affect the Link training that's already in progress.
4	0h RW	**Link Disable (LD):** When set, the root port will disable the link by directing the LTSSM to the Disabled state.
3	0h RW/O	**Read Completion Boundary Control (RCBC):** Indicates the read completion boundary is 64 bytes.
2	0h RO	Reserved.
1:0	0h RW	**Active State Link PM Control (ASPM):** Indicates whether the root port should enter L0s or L1 or both. Bits Definition 00 Disabled 01 L0s Entry Enabled 10 L1 Entry Enabled 11 L0s and L1 Entry Enabled The value of this register is used unless the Root Port ASPM Control Override Enable register is set, in which case the Root Port ASPM Control Override value is used. Note: If STRPFUSECFG.ASPMDIS is '1', hardware will always see '00' as an output from this register. BIOS reading this register should always return the correct value.

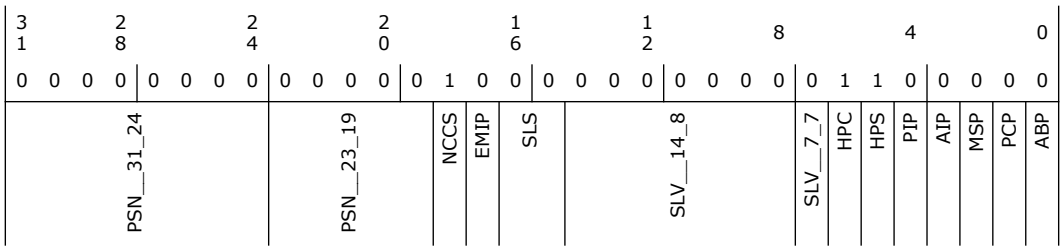
15.1.18 Slot Capabilities (SLCAP)—Offset 54h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 40060h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW/O	**Physical Slot Number (PSN__31_24):** This is a value that is unique to the slot number. BIOS sets this field and it remains set until a platform reset.
23:19	0h RW/O	**Physical Slot Number (PSN__23_19):** This is a value that is unique to the slot number. BIOS sets this field and it remains set until a platform reset.
18	1h RO	**No Command Completed Support (NCCS):** Set to '1' asthis port does not implement a Hot Plug controller and can handle back-2-back writes to all fields of the slot control register without delay between successive writes.
17	0h RO	**Electromechanical Interlock Present (EMIP):** Set to 0 to indicate that no electro-mechanical interlock is implemented.
16:15	0h RW/O	**Slot Power Limit Scale (SLS):** specifiesthe scale used for the slot power limit value. BIOS sets this field and it remains set until a platform reset.
14:8	0h RW/O	**Slot Power Limit Value (SLV__14_8):** Specifies the upper limit (in conjunction with SLS value), on the upper limit on power supplied by the slot. The two values together indicate the amount of power in watts allowed for the slot. BIOS sets this field and it remains set until a platform reset.
7	0h RW/O	**Slot Power Limit Value (SLV__7_7):** Specifies the upper limit (in conjunction with SLS value), on the upper limit on power supplied by the slot. The two values together indicate the amount of power in watts allowed for the slot. BIOS sets this field and it remains set until a platform reset.
6	1h RW/O	**Hot Plug Capable (HPC):** When set, Indicates that hot plug is supported.
5	1h RW/O	**Hot Plug Surprise (HPS):** When set, indicates the device may be removed from the slot without prior notification.
4	0h RO	**Power Indicator Present (PIP):** Indicates that a power indicator LED is not present for this slot.
3	0h RO	**Attention Indicator Present (AIP):** Indicates that an attention indicator LED is not present for this slot.
2	0h RO	**MRL Sensor Present (MSP):** Indicates that an MRL sensor is not present
1	0h RO	**Power Controller Present (PCP):** Indicates that a power controller is not implemented for this slot
0	0h RO	**Attention Button Present (ABP):** Indicates that an attention button is not implemented for this slot.

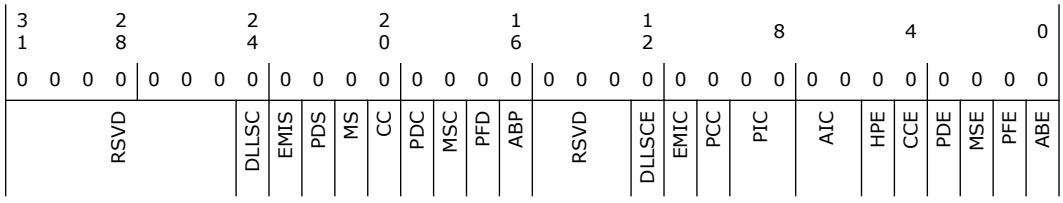
15.1.19 Slot Control; Slot Status (SLCTL_SLSTS)—Offset 58h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	Reserved.
24	0h RW/1C/V	**Data Link Layer State Changed (DLLSC):** This bit is set when the value reported in Data Link Layer Link Active field of the Link Status register is changed. In response to a Data Link Layer State Changed event, software must read Data Link Layer Link Active field of the Link Status register to determine if the link is active before initiating configuration cycles to the hot plugged device.
23	0h RO	**Electromechanical Interlock Status (EMIS):** Reserved as this port does not support and electromechanical interlock.
22	0h RO/V	**Presence Detect State (PDS):** If XCAP.SI is set (indicating that this root port spawns a slot), then this bit indicates whether a device is connected ('1') or empty ('0'). If XCAP.SI is cleared, this bit is a '1'.
21	0h RO	**MRL Sensor State (MS):** Reserved as the MRL sensor is not implemented.
20	0h RO	**Command Completed (CC):** This register is RO as this port does not implement a Hot Plug Controller..
19	0h RW/1C/V	**Presence Detect Changed (PDC):** This bit is set by the root port when the SLSTS.PDS bit changes state.
18	0h RO	**MRL Sensor Changed (MSC):** Reserved as the MRL sensor is not implemented.
17	0h RO	**Power Fault Detected (PFD):** Reserved as a power controller is not implemented.
16	0h RO	**Attention Button Pressed (ABP):** This register is RO as this port does not implement an attention button
15:13	0h RO	Reserved.
12	0h RW	**Data Link Layer State Changed Enable (DLLSCE):** When set, this field enables generation of a hot plug interrupt when the Data Link Layer Link Active field is changed
11	0h RO	**Electromechanical Interlock Control (EMIC):** Reserved as this port does not support an Electromechanical Interlock.
10	0h RO	**Power Controller Control (PCC):** This bit has no meaning for module based hot plug.
9:8	0h RO	**Power Indicator Control (PIC):** This register is RO as this port does not implement a Hot Plug Controller..
7:6	0h RO	**Attention Indicator Control (AIC):** This register is RO as this port does not implement a Hot Plug Controller..
5	0h RW	**Hot Plug Interrupt Enable (HPE):** When set, enables generation of a hot plug interrupt on enabled hot plug events.
4	0h RO	**Command Completed Interrupt Enable (CCE):** This register is RO as this port does not implement a Hot Plug Controller..
3	0h RW	**Presence Detect Changed Enable (PDE):** When set, enables the generation of a hot plug interrupt or wake message when the presence detect logic changes state.
2	0h RO	**MRL Sensor Changed Enable (MSE):** This register is RO as this port does not implement a Hot Plug Controller..
1	0h RO	**Power Fault Detected Enable (PFE):** This register is RO as this port does not implement a Hot Plug Controller...
0	0h RO	**Attention Button Pressed Enable (ABE):** This register is RO as this port does not implement a Hot Plug Controller..

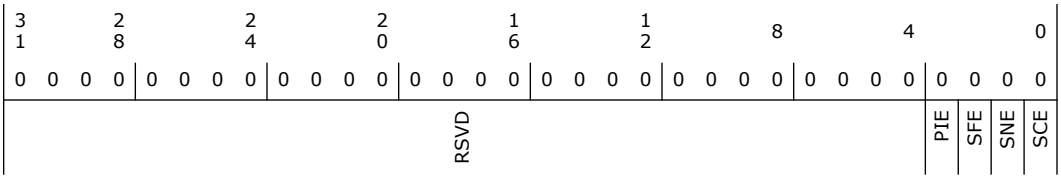
15.1.20 Root Control (RCTL)—Offset 5Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3	0h RW	**PME Interrupt Enable (PIE):** When set, enables interrupt generation when RSTS.PS is in a set state (either due to a '0' to'1' transition, or due to this bit being set with RSTS.PS already set).
2	0h RW	**System Error on Fatal Error Enable (SFE):** When set, an SERR# will be generated if a fatal error is reported by any of the devices in the hierarchy of this root port, including fatal errors in this root port. This register is not dependent on CMD.SEE being set.
1	0h RW	**System Error on Non-Fatal Error Enable (SNE):** When set, an SERR# will be generated if a non-fatal error is reported by any of the devices in the hierarchy of this root port, including non-fatal errors in this root port. This register is not dependent on CMD.SEE being set.
0	0h RW	**System Error on Correctable Error Enable (SCE):** When set, an SERR# will be generated if a correctable error is reported by any of the devices in the hierarchy of this root port, including correctable errors in this root port. This register is not dependent on CMD.SEE being set.

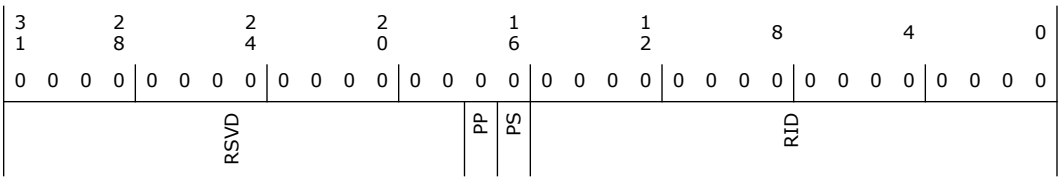
15.1.21 Root Status (RSTS)—Offset 60h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17	0h RO/V	**PME Pending (PP):** Indicates another PME is pending when the PME status bit is set. When the original PME is cleared by software, it will be set again, the requestor ID will be updated, and this bit will be cleared. Root ports have a one deep PME pending queue.
16	0h RW/1C/V	**PME Status (PS):** Indicates that PME was asserted by the requestor ID in RID. Subsequent PMEs are kept pending until this bit is cleared.
15:0	0h RO/V	**PME Requestor ID (RID):** Indicates the PCI requestor ID of the last PME requestor. Valid only when PS is set. Root ports are capable of storing the requester ID for two PM_PME messages, with one active (this register) and a one deep pending queue. Subsequent PM_PME messages will be dropped.

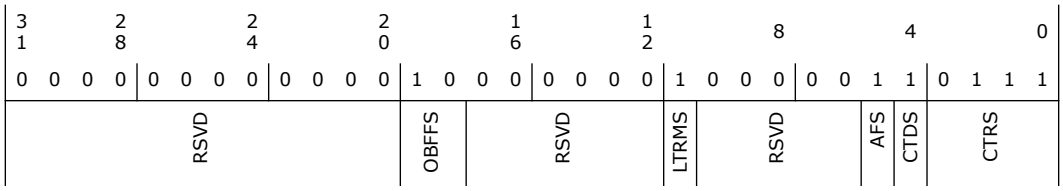
15.1.22 Device Capabilities 2 (DCAP2)—Offset 64h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 80837h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	Reserved.
19:18	2h RW/O	**Optimized Buffer Flush/Fill Supported (OBFFS):** 00b - OBFF is not supported. 01b - OBFF is supported using Message signaling only. 10b - OBFF is supported using WAKE# signaling only. 11b - OBFF is supported using WAKE# and Message signaling. BIOS shall program this field to 00b since OBFF messaging is not supported.
17:12	0h RO	Reserved.
11	1h RW/O	**LTR Mechanism Supported (LTRMS):** A value of 1b indicates support for the optional Latency Tolerance Reporting (LTR) mechanism capability. BIOS must write to this register with either a '1' ora '0' to enable/disable the root port from declaring support for the LTR capability.
10:6	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
5	1h RO	**ARI Forwarding Supported (AFS):** ARI Forwarding Supported (AFS): Applicable only to Switch Downstream Ports and Root Ports; must be 0b for other Function types. This bit must be set to 1b if a Switch Downstream Port or Root Port supports this optional capability. Note: This bit is not made RWO to simplify implementation, since there is a requirement that the ARI Forwarding Enable bit must be hardwired to 0b if ARI Forwarding Supported bit is 0b. It is low risk to keep this risk 1b.
4	1h RO	**Completion Timeout Disable Supported (CTDS):** A value of 1b indicates support for the Completion Timeout Disable mechanism.
3:0	7h RO	**Completion Timeout Ranges Supported (CTRS):** This field indicates device support for the optional Completion Timeout programmability mechanism. This mechanism allows system software to modify the Completion Timeout value. This field is applicable only to Root Ports, Endpoints that issue requests on their own behalf, and PCI Express to PCI/PCI-X Bridges that take ownership of requests issued on PCI Express. For all other devices this field is reserved and must be hardwired to 0000b. Four time value ranges are defined: Range A: 50us to 10ms Range B: 10ms to 250ms Range C: 250ms to 4s Range D: 4s to 64s Bits are set according to the table below to show timeout value ranges supported. 0000b Completion Timeout programming not supported. 0001b Range A 0010b Range B 0011b Ranges A [amp] B 0110b Ranges B [amp] C 0111b Ranges A, B [amp] C [lt]-- This is what PCH supports 1110b Ranges B, C [amp] D 1111b Ranges A, B, C [amp] D All other values are reserved.

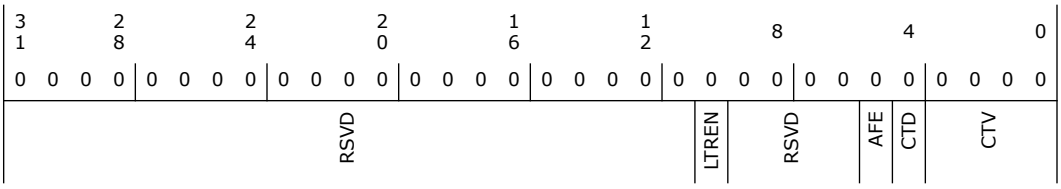
15.1.23 Device Control 2; Device Status 2 (DCTL2_DSTS2)—Offset 68h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:11	0h RO	Reserved.
10	0h RW	**LTR Mechanism Enable (LTREN):** When Set to 1b, this bit enables the Latency Tolerance Reporting (LTR) mechanism. For Downstream Ports, this bit must be reset to the default value if the Port goes to DL_Down status. If DCAP2.LTRMS is clear, programming this field to any non-zero values will have no effect.
9:6	0h RO	Reserved.
5	0h RW	**ARI Forwarding Enable (AFE):** ARI Forwarding Enable (AFE): When set, the Downstream Port disables its traditional Device Number field being 0b enforcement when turning a Type 1 Configuration Request into a Type 0 Configuration Request, permitting access to Extended Functions in an ARI Device immediately below the Port.
4	0h RW	**Completion Timeout Disable (CTD):** When set to 1b, this bit disables the Completion Timeout mechanism. This field is required for all devices that support the Completion Timeout Disable Capability. Software is permitted to set or clear this bit at any time. When set, the Completion Timeout detection mechanism is disabled. If there are outstanding requests when the bit is cleared, it is permitted but not required for hardware to apply the completion timeout mechanism to the outstanding requests. If this is done, it is permitted to base the start time for each request on either the time this bit was cleared or the time each request was issued.
3:0	0h RW	**Completion Timeout Value (CTV):** In Devices that support Completion Timeout programmability, this field allows system software to modify the Completion Timeout value. This field is applicable to Root Ports, Endpoints that issue requests on their own behalf, and PCI Express to PCI/PCI-X Bridges that take ownership of requests issued on PCI Express. For all other devices this field is reserved and must be hardwired to 0000b. A Device that does not support this optional capability must hardwire this field to 0000b and is required to implement a timeout value in the range 50us to 50ms. Devices that support Completion Timeout programmability must support the values given below corresponding to the programmability ranges indicated in the Completion Timeout Values Supported field. The root port targeted configurable ranges are listed below, along with the range allowed by the PCI Express 2.0 specification. Defined encodings: 0000b Default range: 40-50ms (spec range 50us to 50ms) Values available if Range A (50us to 10 ms) programmability range is supported: 0001b 90-100us (spec range is 50 us to 100 us) 0010b 9-10ms (spec range is 1ms to 10 ms) Values available if Range B (10ms to 250ms) programmability range is supported: 0101b 40-50ms (spec range is 16ms to 55ms) 0110b 160-170ms (spec range is 65ms to 210ms) Values available if Range C (250ms to 4s) programmability range is supported: 1001b 400-500ms (spec range is 260ms to 900ms) 1010b 1.6-1.7s (spec range is 1s to 3.5s) Values not defined above are Reserved. Software is permitted to change the value in this field at any time. For requests already pending when the Completion Timeout Value is changed, hardware is permitted to use either the new or the old value for the outstanding requests, and is permitted to base the start time for each request either when this value was changed or when each request was issued.

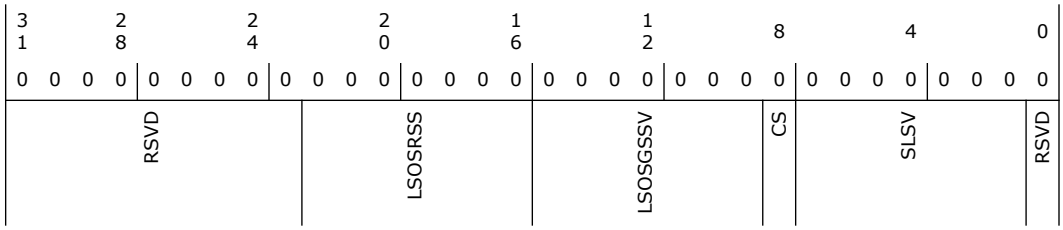
15.1.24 Link Capabilities 2 (LCAP2)—Offset 6Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	Reserved.
22:16	0h RO	**Lower SKP OS Reception Supported Speeds Vector (LSOSRSS):** Lower SKP OS Reception Supported Speeds Vector(LSOSRSS): If this field is non-zero, it indicates that the Port, when operating at the indicated speed(s) supports SRIS and also supports receiving SKP OS at the rate defined for SRNS while running in SRIS. Bit definitions within this field are: Bit 0 2.5 GT/s Bit 1 5.0 GT/s Bit 2 8.0 GT/s Bits 6:3 RsvdP Behavior is undefined if a bit is set in this field and the corresponding bit is not set in the Supported Link Speeds Vector.
15:9	0h RO	**Lower SKP OS Generation Supported Speeds Vector (LSOSGSSV):** Lower SKP OS Generation Supported Speeds Vector(LSOSGSSV): If this field is non-zero, it indicates that the Port, when operating at the indicated speed(s) supports SRIS and also supports software control of the SKP Ordered Set transmission scheduling rate. Bit definitions within this field are: Bit 0 2.5 GT/s Bit 1 5.0 GT/s Bit 2 8.0 GT/s Bits 6:3 RsvdP Behavior is undefined if a bit is set in this field and the corresponding bit is not set in the Supported Link Speeds Vector.
8	0h RO	**Crosslink Supported (CS):** Crosslink Supported (CS): No support for Crosslink.
7:1	0h RO/V	**Supported Link Speeds Vector (SLSV):** Supported Link Speeds Vector (SLSV): This field indicates the supported Link speed of the associated Port. For each bit, a value of 1b indicates that the corresponding Link speed is supported; otherwise, the Link speed is not supported. Bit definitions within this field are: Bit 0: 2.5 GT/s. Bit 1: 5.0 GT/s. Bit 2: 8.0 GT/s. Bits 6:3: Reserved. This register reports a value of 0001b if GEN1 data rate is supported but both GEN2 and GEN3 data rate support are disabled through Fuse or MPC.PCIESD register. This register reports a value of 0011b if both GEN1 and GEN2 data rate are supported but GEN3 data rate support is disabled through Fuse or MPC.PCIESD register.
0	0h RO	Reserved.

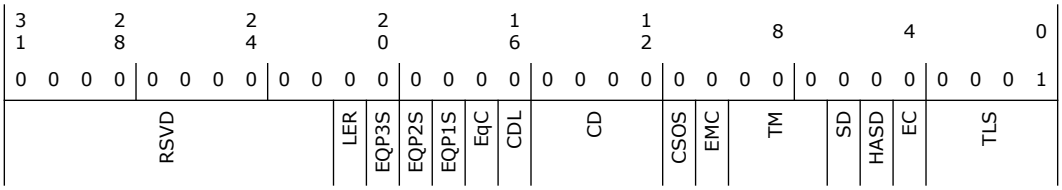
15.1.25 Link Control 2; Link Status 2 (LCTL2_LSTS2)—Offset 70h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 1h



Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	Reserved.
21	0h RW/1C/V/P	**Link Equalization Request (LER):** Link Equalization Request (LER): This bit is set by hardware to request the Link equalization process to be performed on the Link. Register Attribute: Dynamic.
20	0h RO/V/P	**Equalization Phase 3 Successful (EQP3S):** Equalization Phase 3 Successful (EQP3S): When set to 1, this bit indicates that Phase 3 of the Transmitter Equalization procedure has successfully completed.
19	0h RO/V/P	**Equalization Phase 2 Successful (EQP2S):** Equalization Phase 2 Successful (EQP2S): When set to 1, this bit indicates that Phase 2 of the Transmitter Equalization procedure has successfully completed.
18	0h RO/V/P	**Equalization Phase 1 Successful (EQP1S):** Equalization Phase 1 Successful (EQP1S): When set to 1, this bit indicates that Phase 1 of the Transmitter Equalization procedure has successfully completed.
17	0h RO/V/P	**Equalization Complete (EqC):** Equalization Complete (EC): When set to 1, this bit indicates that the Transmitter Equalization procedure has completed
16	0h RO/V	**Current De-emphasis Level (CDL):** When the Link is operating at 5.0 GT/s speed, this bit reflects the level of de-emphasis. Encodings: 1b -3.5 dB 0b -6 dB The value in this bit is undefined when the Link is not operating at 5.0 GT/s speed.
15:12	0h RW/P	**Compliance Preset/De-emphasis (CD):** For 8.0 GT/s Data Rate: This field sets the Transmitter Preset in Polling.Compliance state if the entry occurred due to the Enter Compliance bit being 1b. Results are undefined if a reserved preset encoding is used when entering Polling.Compliance in this way. For 5.0 GT/s Data Rate: This bit sets the de-emphasis level in Polling.Compliance state if the entry occurred due to the Enter Compliance bit being 1b. Encodings: 0001b -3.5 dB 0000b -6 dB When the Link is not operating at 5.0 GT/s speed, the setting of this bit has no effect. The default value of this field is 0000b. This bit is intended for debug, compliance testing purposes. System firmware and software is allowed to modify this bit only during debug or compliance testing. In all other cases, the system must ensure that this field is set to the default value.
11	0h RW/P	**Compliance SOS (CSOS):** When set to 1b, the LTSSM is required to send SKP Ordered Sets periodically in between the (modified) compliance patterns. The default value of this bit is 0b. This bit is applicable when the Link is operating at 2.5 GT/s or 5.0 GT/s data rates only.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW/P	**Enter Modified Compliance (EMC):** When this bit is set to 1b, the device transmits Modified Compliance Pattern if the LTSSM enters Polling.Compliance substate. Default value of this bit is 0b. This register is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this register only during debug or compliance testing. In all other cases, the system must ensure that this register is set to the default value.
9:7	0h RW/P	**Transmit Margin (TM):** This field controls the value of the nondeemphasized voltage level at the Transmitter pins. This field is reset to 000b on entry to the LTSSM Polling.Configuration substate (see PCI Express Chapter 4 for details of how the Transmitter voltage level is determined in various states). Encodings: 000b Normal operating range 001b 800-1200 mV for full swing and 400-700 mV for half-swing 010b - (n-1) Values must be monotonic with a non-zero slope. The value of n must be greater than 3 and less than 7. At least two of these must be below the normal operating range of n : 200-400 mV for full-swing and 100-200 mV for half-swing n - 111b reserved For a Multi-Function device associated with an Upstream Port, the field in Function 0 is of type RWS, and only Function 0 controls the component's Link behavior. In all other Functions of that device, this field is of type RsvdP. Default value of this field is 000b. Components that support only the 2.5 GT/s speed are permitted tohardwire this bit to 000b. This register is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this register only during debug or compliance testing. In all other cases, the system must ensure that this register is set to the default value.
6	0h RW/P	**Selectable De-emphasis (SD):** When the Link is operating at 5.0 GT/s speed, this bit selects the level of de-emphasis for an Upstream component. Encodings: 1b -3.5 dB 0b -6 dB When the Link is not operating at 5.0 GT/s speed, the setting of this bit has no effect. When the Link is operating at 2.5 GT/s speed, the setting of this bit has no effect.
5	0h RO	**Hardware Autonomous Speed Disable (HASD):** Reserved. This port cannot autonomously change speeds.
4	0h RW/P	**Enter Compliance (EC):** Software is permitted to force a Link to enter Compliance mode at the speed indicated in the Target Link Speed field by setting this bit to 1b in both components on a Link and then initiating a hot reset on the Link. Default value of this bit following Fundamental Reset is 0b. This bit is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this bit only during debug or compliance testing. In all other cases, the system must ensure that this bit is set to the default value. This bit is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this bit only during debug or compliance testing. In all other cases, the system must ensure that this bit is set to the default value.
3:0	1h RW/V/P	**Target Link Speed (TLS):** Target Link Speed (TLS): This field sets an upper limit on Link operational speed by restricting the values advertised by the upstream component in its training sequences. The encoded value specifies a bit location in the Supported Link Speeds Vector (in the Link Capabilities 2 register) that corresponds to the current Link speed. Defined encodings are: 0001b: Supported Link Speeds Vector field bit 0. 0010b: Supported Link Speeds Vector field bit 1. 0011b: Supported Link Speeds Vector field bit 2. 0100b: Supported Link Speeds Vector field bit 3. 0101b: Supported Link Speeds Vector field bit 4. 0110b: Supported Link Speeds Vector field bit 5. 0111b: Supported Link Speeds Vector field bit 6. All other encodings are reserved. If a value is written to this field that does not correspond to a supported speed, as indicated by the Supported Link Speeds Vector, the result is undefined. The default value of this field is GEN1. Note: This register field could be used by REUT software to limit the link speed to 2.5 GT/s or 5 GT/s data rate.

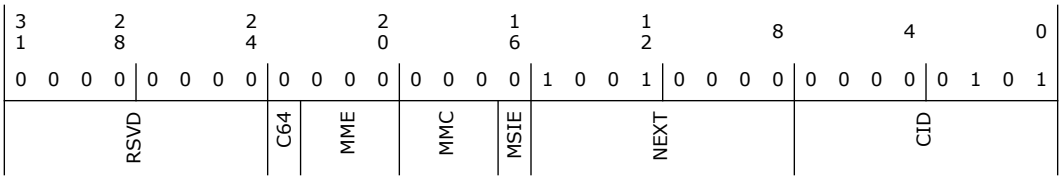
15.1.26 Message Signaled Interrupt Identifiers; Message Signaled Interrupt Message Control (MID_MC)—Offset 80h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 9005h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RO	**64-Bit Address Capable (C64):** Capable of generating a 32-bit message only.
22:20	0h RW	**Multiple Message Enable (MME):** These bits are RW for software compatibility, but only one message is ever sent by the root port.
19:17	0h RO	**Multiple Message Capable (MMC):** Only one message is required.
16	0h RW	**MSI Enable (MSIE):** If set, MSI is enabled and traditional interrupt pins are not used to generate interrupts. CMD.BME must be set for an MSI to be generated. If CMD.BME is cleared, and this bit is set, no interrupts (not even pin based) are generated.
15:8	90h RW/O	**Next Pointer (NEXT):** Indicates the location of the next capability in the list. The default value of this register is 90h which points to the Subsystem Vendor capability structure. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value.
7:0	5h RO	**Capability ID (CID):** Capabilities ID indicates MSI.

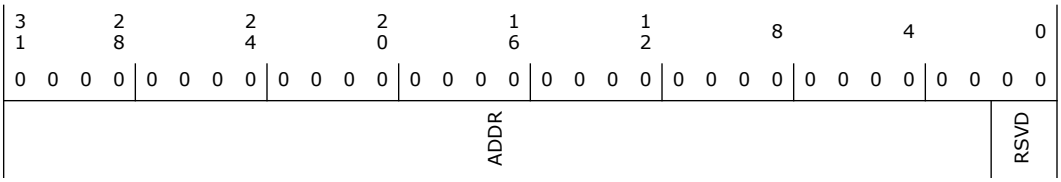
15.1.27 Message Signaled Interrupt Message Address (MA)—Offset 84h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**Address (ADDR):** Lower 32 bits of the system specified message address, always DW aligned.
1:0	0h RO	Reserved.

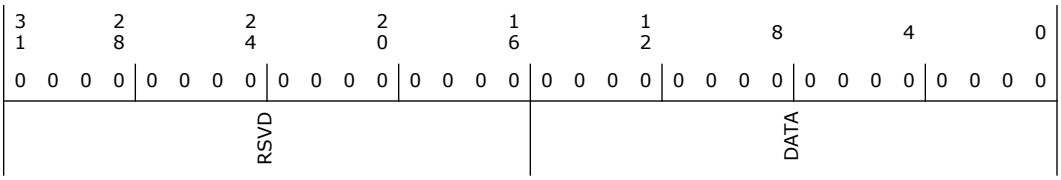
15.1.28 Message Signaled Interrupt Message Data (MD)—Offset 88h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	0h RW	**Data (DATA):** This 16-bit field is programmed by system software if MSI is enabled. Its content is driven onto the lower word (PCI AD[lb]15:0[rb]) during the data phase of the MSI memory write transaction.

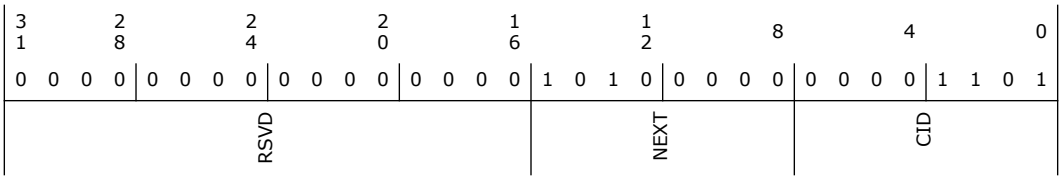
15.1.29 Subsystem Vendor Capability (SVCAP)—Offset 90h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: A00Dh



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:8	A0h RW/O	**Next Capability (NEXT):** Indicates the location of the next capability in the list. The default value of this register is A0h which points to the PCI Power Management capability structure. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value.
7:0	Dh RO	**Capability Identifier (CID):** Value of 0Dh indicates this is a PCI bridge subsystem vendor capability.

15.1.30 Subsystem Vendor IDs (SVID)—Offset 94h

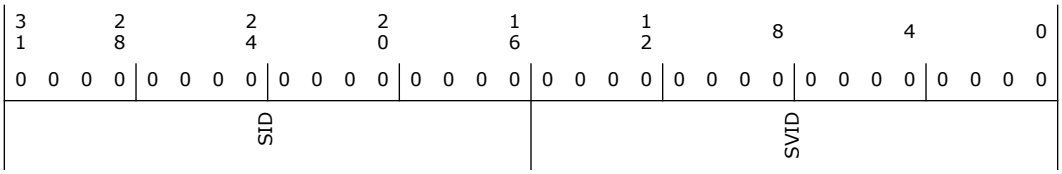
Size:32 bits

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW/O	**Subsystem Identifier (SID):** Indicates the subsystem as identified by the vendor. This field is write once and is locked down until a bridge reset occurs (not the PCI bus reset).
15:0	0h RW/O	**Subsystem Vendor Identifier (SVID):** Indicates the manufacturer of the subsystem. This field is write once and is locked down until a bridge reset occurs (not the PCI bus reset).

15.1.31 Power Management Capability; PCI Power Management Capabilities (PMCAP_PMC)—Offset A0h

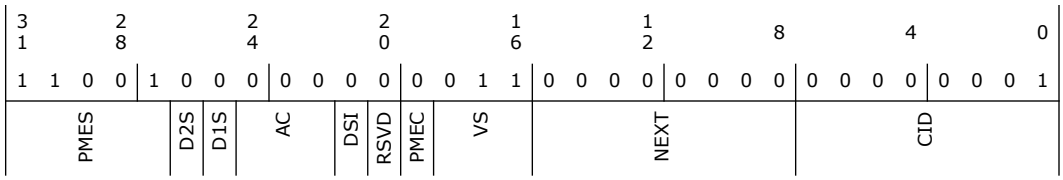
Size:32 bits

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: C8030001h



Bit Range	Default & Access	Field Name (ID): Description
31:27	19h RO	**PME Support (PMES):** Indicates PME# is supported for states D0, D3HOT and D3COLD. The root port does not generate PME#, but reporting that it does is necessary for legacy Microsoft operating systems to enable PME# in devices connected behind this root port.
26	0h RO	**D2_Support (D2S):** The D2 state is not supported.
25	0h RO	**D1_Support (D1S):** The D1 state is not supported.
24:22	0h RO	**Aux_Current (AC):** Reports 0mA (self-powered), as use of this controller does not add to suspect well power consumption.
21	0h RO	**Device Specific Initialization (DSI):** Indicates that no device-specific initialization is required.
20	0h RO	Reserved.
19	0h RO	**PME Clock (PMEC):** Indicates that PCI clock is not required to generate PME#.
18:16	3h RO	**Version (VS):** Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	0h RO	**Next Capability (NEXT):** Indicates this is the last item in the list.
7:0	1h RO	**Capability Identifier (CID):** Value of 01h indicates this is a PCI power management capability.

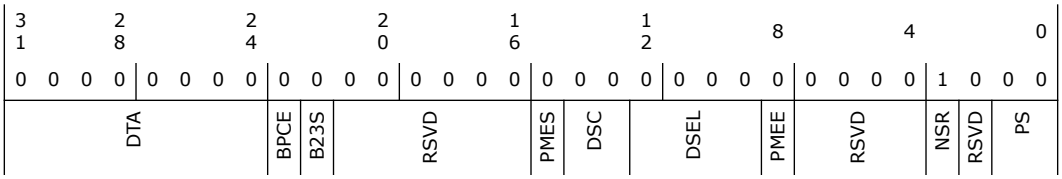
15.1.32 PCI Power Management Control And Status (PMCS)—Offset A4h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 8h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Data (DTA):** Reserved
23	0h RO	**Bus Power / Clock Control Enable (BPCE):** Reserved per PCI Express specification
22	0h RO	**B2/B3 Support (B23S):** Reserved per PCI Express specification.
21:16	0h RO	Reserved.
15	0h RO	**PME Status (PMES):** Indicates a PME was received on the downstream link.
14:13	0h RO	**Data Scale (DSC):** Reserved
12:9	0h RO	**Data Select (DSEL):** Reserved
8	0h RW/P	**PME Enable (PMEE):** Indicates PME is enabled. The root port takes no action on this bit, but it must be RW for legacy Microsoft operating systems to enable PME# on devices connected to this root port.
7:4	0h RO	Reserved.
3	1h RW/O	**No Soft Reset (NSR):** When set to 1 this bit indicates that devices transitioning from D3hot to D0 because of Power State commands do not perform an internal reset. Configuration context is preserved. Upon transition from D3hot to D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the Power State bits. When clear, devices do perform an internal reset upon transitioning from D3hot to D0 via software control of the Power State bits. Configuration Context is lost when performing the soft reset. Upon transition from D3hot to D0 state, full reinitialization sequence is needed to return the device to D0 Initialized. Regardless of this bit, devices that transition from D3hot to D0 by a system or bus segment reset will return to the device state D0 Uninitialized with only PME context preserved if PME is supported and enabled.
2	0h RO	Reserved.
1:0	0h RW	**Power State (PS):** This field is used both to determine the current power state of the root port and to set a new power state. The values are: 00 D0 state 11 D3HOT state When in the D3HOT state, the controller's configuration space is available, but the I/O and memory spaces are not. Type 1 configuration cycles are also not accepted. Interrupts are not required to be blocked as software will disable interrupts prior to placing the port into D3HOT. If software attempts to write a '10' or'01' to these bits, the write will be ignored.

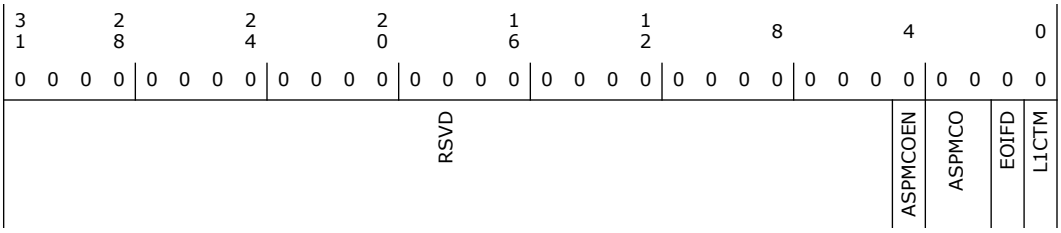
15.1.33 Miscellaneous Port Configuration 2 (MPC2)—Offset D4h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4	0h RW	**ASPM Control Override Enable (ASPMCOEN):** When set to '1', the PCIe Root Port will use the values in the ASPM Control Override registers instead of ASPM Registers in the Link Control register. This register allows BIOS to control the DMI ASPM settings instead of the OS. Note: If STRPFUSECFG.ASPMDIS is '1'. Hardware will always see the output of this field as '1' regardlessof the setting of this field. BIOS reading this register should always return the correct value.
3:2	0h RW	**ASPM Control Override (ASPMCO):** Provides BIOS control of whether root port should enter L0s or L1 or both. 00 = Disabled 01 = L0s Entry Enabled 10 = L1 Entry Enabled 11 = L0s and L1 Entry Enabled.
1	0h RW	**EOI Forwarding Disable (EOIFD):** 0 = Broadcast EOI messages that are sent on the backbone are claimed by this port and forwarded across the PCIe* link.{br] 1 = Broadcast EOI messages are not claimed on the backbone by this port and will not be forwarded across the PCIe* Link.
0	0h RW	**L1 Completion Timeout Mode (L1CTM):** 0 = PCI Express* Specification Compliant. Completion timeout is disabled during software initiated L1, and enabled during ASPM initiate L1. 1 = Completion timeout is enabled during L1, regardless of how L1 entry was initiated.

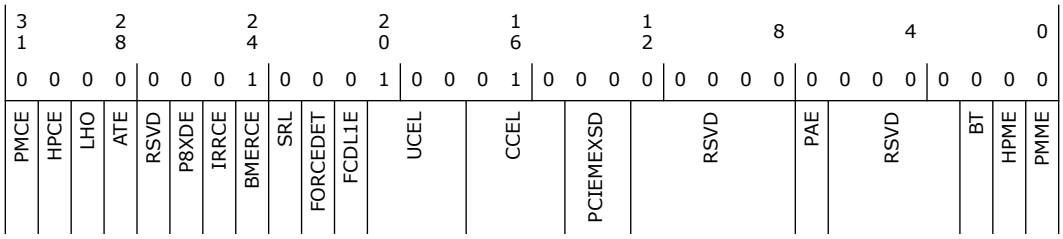
15.1.34 Miscellaneous Port Configuration (MPC)—Offset D8h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 1110000h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Power Management SCI Enable (PMCE):** 0 = SCI generation based on a power management event is disabled. 1 = Enables the root port to generate SCI whenever a power management event is detected.
30	0h RW	**Hot Plug SCI Enable (HPCE):** 0 = SCI generation based on a hot-plug event is disabled. 1 = Enables the root port to generate SCI whenever a hot-plug event is detected.
29	0h RW/L	**Link Hold Off (LHO):** When set, the port will not take any TLP. This is used during loopback mode to fill up the downstream queue.
28	0h RW/L	**Address Translater Enable (ATE):** Used to enable address translation via the AT bits in this register during loopback mode. 0: Disable 1: Enable
27	0h RO	Reserved.
26	0h RW/L	**Port8xh Decode Enable (P8XDE):** When set, allows PCIe Root Port to claim I/O cycles within the range from 80h - 8Fh inclusive and forwarding the cycle to the link. The claiming of these cycles are independent of I/O Base/Limit and IO Space Enable bits. BIOS must ensure that at any one time, no more than one PCIe Root Port are enabled to claim Port 8xh cycles.
25	0h RW/L	**Invalid Receive Range Check Enable (IRRCE):** When set, the receive transaction layer will treat the TLP as an Unsupported Request error if the address range of a Memory request does not fall outside the range between prefetchable and non-prefetchable base and limit. Messages, IO, Config, and Completions are never checked for valid address ranges This register bit is Read-Only when the MPC.SRL bit is set.
24	1h RW/L	**BME Receive Check Enable (BMERCE):** When set, the receive transaction layer will treat the TLP as an Unsupported Request error if a memory or I/O read or write request is received and the Bus Master Enable bit is not set. Messages, Config, and Completions are never checked for BME.
23	0h RW/O	**Secured Register Lock (SRL):** When this bit is set, all the secured registers will be locked and will be Read-Only.
22	0h RW/L	**Detect Override (FORCEDET):** 0: Normal operation. Detect output from AFE is sampled for presence detection. 1: Override mode. Ignores AFE detect output and Link Training proceeds as if a device were detected.
21	0h RW	**Flow Control During L1 Entry (FCDL1E):** br] 0: No flow control update DLLPs sent during L1 Ack transmission 1: Flow control update DLLPs sent during L1 Ack transmission as required to meet the 30us periodic flow control update.
20:18	4h RW	**Unique Clock Exit Latency (UCEL):** This value represents the L0s Exit Latency for unique-clock configurations (LCTL.CCC = '0'). It defaults to 512ns to less than 1us, but may be overridden by BIOS.
17:15	2h RW	**Common Clock Exit Latency (CCEL):** This value represents the L0s Exit Latency for common-clock configurations (LCTL.CCC = '1'). It defaults to 128ns to less than 256ns, but may be overridden by BIOS.

Bit Range	Default & Access	Field Name (ID): Description
14:13	0h RW	**PCIe MEx Speed Disable (PCIEMEXSD):** When operating as PCI Express: 00: PCIe supported data rate is as defined by the Supported Link Speed and Target Link Speed register. 01: PCIe supported data rate is limited to just 2.5 GT/s. Supported Link Speed field will reflect 0000001b. Max Link Speed field will reflect 0001b. 10: PCIe supported data rate is limited to 2.5 GT/s and 5.0 GT/s. Supported Link Speed register will reflect 0000011b. Max Link Speed field will reflect 0010b. 11: Reserved. When operating as Mobile Express: 00: MEx supported data rate is as defined by the Supported Link Speed and Target Link Speed register. 01: MEx supported data rate is limited to just HS-G1. Supported Link Speed field will reflect 0000001b. Max Link Speed field will reflect 0000b. 10: PCIe supported data rate is limited to HS-G1 and HS-G2. Supported Link Speed register will reflect 0000001b. Max Link Speed field will reflect 0000b. 11: Reserved. When this bit is changed, link retrain needs to be performed for the change to be effective.
12:8	0h RO	Reserved.
7	0h RW	**Port I/OxApic Enable (PAE):** When set, a range is opened through the bridge for the following memory addresses: Port# Address 1 FEC1_0000h - FEC1_7FFFh 2 FEC1_8000h - FEC1_FFFFh 3 FEC2_0000h - FEC2_7FFFh 4 FEC2_8000h - FEC2_FFFFh 5 FEC3_0000h - FEC3_7FFFh 6 FEC3_8000h - FEC3_FFFFh 7 FEC4_0000h - FEC4_7FFFh 8 FEC4_8000h - FEC4_FFFFh When cleared, the hole is disabled.
6:3	0h RO	Reserved.
2	0h RW/O	**Bridge Type (BT):** This register can be used to modify the Base Class and Header Type fields from the default PCI-to-PCI bridge to a Host Bridge. Having the root port appear as a Host Bridge is useful in some server configurations. 0 = The root port bridge type is a PCI-to-PCI Bridge, Header Sub-Class = 04h, and Header Type = Type 1. 1 = The root port bridge type is a PCI-to-PCI Bridge, Header Sub-Class = 00h, and Header Type = Type 0.
1	0h RW	**Hot Plug SMI Enable (HPME):** 0 = SMI generation based on a hot-plug event is disabled. 1 = Enables the root port to generate SMI whenever a hot-plug event is detected.
0	0h RW	**Power Management SMI Enable (PMME):** 0 = SMI generation based on a power management event is disabled. 1 = Enables the root port to generate SMI whenever a power management event is detected.

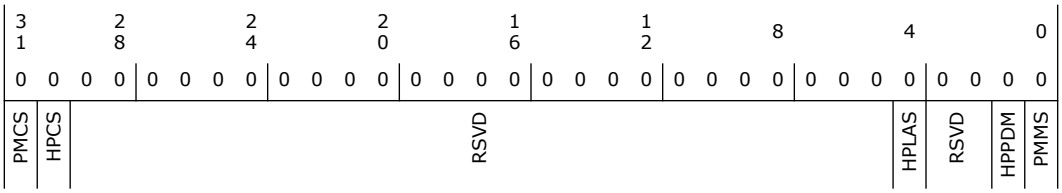
15.1.35 SMI / SCI Status (SMSCS)—Offset DCh

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C/V	**Power Management SCI Status (PMCS):** This bit is set if the root port PME control logic needs to generate an interrupt, and this interrupt has been routed to generate an SCI.
30	0h RW/1C/V	**Hot Plug SCI Status (HPCS):** This bit is set if the hot plug controller needs to generate an interrupt, and has this interrupt been routed to generate an SCI.
29:5	0h RO	Reserved.
4	0h RW/1C/V	**Hot Plug Link Active State Changed SMI Status (HPLAS):** This bit is set when SLSTS.DLLSC transitions from '0' to '1', and MPC.HPME is set. When this bit is set, an SMI# will be generated.
3:2	0h RO	Reserved.
1	0h RW/1C/V	**Hot Plug Presence Detect SMI Status (HPPDM):** This bit is set when SLSTS.PDC transitions from '0' to'1', and MPC.HPME is set. When this bit is set, an SMI# will be generated.
0	0h RW/1C/V	**Power Management SMI Status (PMMS):** This bit is set when RSTS.PS transitions from '0' to'1', and MPC.PMME is set.

15.1.36 IOSF Primary Control And Status (IPCS)—Offset F0h

BIOS may need to program this register.

15.1.37 Additional Configuration 1 (STRPFUSECFG)—Offset FCh

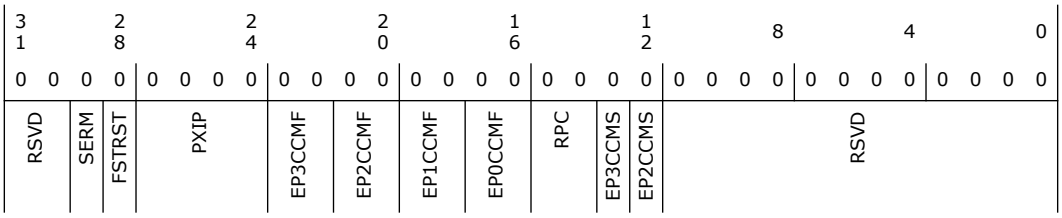
BIOS may need to program this register.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29	0h RW	**Server Error Reporting Mode (SERM):** Server Error Reporting Mode (SERM): When set, if the PCIe port detects a fatal, non-fatal, or correctable error on the link, it sends one of ERR_FATAL, ERR_NONFATAL, or ERR_CORR to IOSF Primary fabric. If the PCIe port receives an ERR_* message from the downstream device, it sends that message to IOSF Primary fabric. Only the value from Port 1 is used for ports 1-4. Note: This register field is only applicable to PC Client SoC.
28	0h RO/V	**Fast Reset Mode Strap (FSTRST):** 0: Normal reset mode. 1: Fast reset mode. Note: Fast reset strap to be used to decrease the time out values of LTSSM counters for pre-silicon simulation purpose. Only the value from Port 1 is used for ports 1-4.
27:24	0h RW	**PCI Express Interrupt Pin (PXIP):** 0000: No interrupt 0001: INTA# 0010: INTB# 0011: INTC# 0100: INTD# Others: Reserved Default Table: 0001: Port 1 0010: Port 2 0011: Port 3 0100: Port 4 Note: This is a proprietary register that can be configured by BIOS to assign the legacy interrupt pins to the PCIe Root Port.
23:22	0h RO/V	**Express Port 3 Combo Controller Mode Fuse (EP3CCMF):** Express Port 3 Combo Controller Mode Fuse (EP3CCMF): 00b :Port 3 is statically configured as PCI Express. 01b :Port 3 is statically configured as Mobile Express. 10b :Port 3 is statically configured as PCI Express or Mobile Express based on Port 3 Combo Controller Mode Soft-Strap. 11b : Reserved
21:20	0h RO/V	**Express Port 2 Combo Controller Mode Fuse (EP2CCMF):** Express Port 2 Combo Controller Mode Fuse (EP2CCMF): 00b :Port 2 is statically configured as PCI Express. 01b :Port 2 is statically configured as Mobile Express. 10b :Port 2 is statically configured as PCI Express or Mobile Express based on Port 2 Combo Controller Mode Soft-Strap. 11b : Reserved
19:18	0h RO/V	**Express Port 1 Combo Controller Mode Fuse (EP1CCMF):** Express Port 1 Combo Controller Mode Fuse (EP1CCMF): 00b :Port 1 is statically configured as PCI Express. 01b :Port 1 is statically configured as Mobile Express. 10b :Port 1 is statically configured as PCI Express or Mobile Express based on Port 1 Combo Controller Mode Soft-Strap. 11b : Reserved
17:16	0h RO/V	**Express Port 0 Combo Controller Mode Fuse (EP0CCMF):** Express Port 0 Combo Controller Mode Fuse (EP0CCMF): 00b :Port 0 is statically configured as PCI Express. 01b :Port 0 is statically configured as Mobile Express. 10b :Port 0 is statically configured as PCI Express or Mobile Express based on Port 0 Combo Controller Mode Soft-Strap. 11b : Reserved

Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RO/V	**Root Port Configuration Strap (RPC):** For Port 1: For a x4 controller : [quote]11[/quote]: 1x4 Port 0 (x4), Ports 1-3 (disabled) [quote]10[/quote]: 2x2 Port 0 (x2), Port 2 (x2), Ports 1, 3 (disabled) [quote]01[/quote]: 1x2, 2x1 Port 0 (x2), Port 1 (disabled), Ports 2, 3 (x1) [quote]00[/quote]: 4x1 Ports 0-3 (x1) For a x2 controller: [quote]01[/quote]: 1x2 Port 0 (x2), Port 1 (disabled) [quote]00[/quote]: 2x1 Ports 0-1 (x1) Only the value from Port 0 is used for ports 1-3.
13	0h RO/V	**Express Port 3 Combo Controller Mode Strap (EP3CCMS):** Express Port 3 Combo Controller Mode Strap (EP3CCMS): 0 : Port 3 is statically configured as PCI Express 1 :Port 3 is statically configured as Mobile Express. This soft strap only has effect if it is allowed by the Port 3 Combo Controller Mode fuse.
12	0h RO/V	**Express Port 2 Combo Controller Mode Strap (EP2CCMS):** Express Port 2 Combo Controller Mode Strap (EP2CCMS): 0 : Port 2 is statically configured as PCI Express 1 :Port 2 is statically configured as Mobile Express. This soft strap only has effect if it is allowed by the Port 2 Combo Controller Mode fuse.
11:0	0h RO	Reserved.

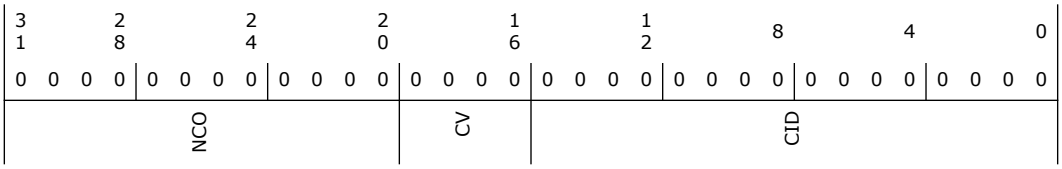
15.1.38 Advanced Error Extended Reporting Capability Header (AECH)—Offset 100h

Size:32 bits
The AER capability can optionally be included or excluded from the capabilities list. The full AER is supported.

Access Method

Type: CFG Register (Size: 32 bits)
Device: 28
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW/O	**Next Capability Offset (NCO):** Set to 000h as this is the last capability in the list.
19:16	0h RW/O	**Capability Version (CV):** For systems that support AER, BIOS should write a 1h to this register else it should write 0
15:0	0h RW/O	**Capability ID (CID):** For systems that support AER, BIOS should write a 0001h to this register else it should write 0

15.1.39 Uncorrectable Error Status (UES)—Offset 104h

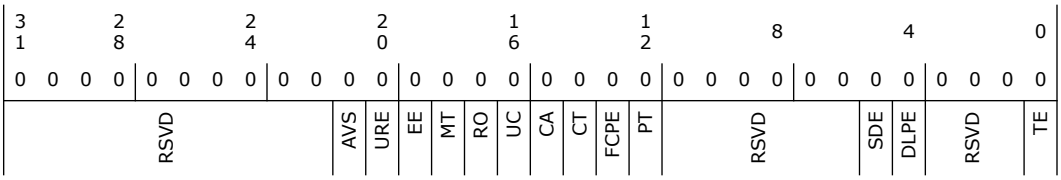
This register must maintain its state through a platform reset. It loses its state upon loss of core power.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	Reserved.
21	0h RW/1C/V/P	**ACS Violation Status (AVS):** Reserved. Access Control Services are not supported
20	0h RW/1C/V/P	**Unsupported Request Error Status (URE):** Indicates an unsupported request was received.
19	0h RO	**ECRC Error Status (EE):** ECRC is not supported.
18	0h RW/1C/V/P	**Malformed TLP Status (MT):** Indicates a malformed TLP was received.
17	0h RW/1C/V/P	**Receiver Overflow Status (RO):** Indicates a receiver overflow occurred.
16	0h RW/1C/V/P	**Unexpected Completion Status (UC):** Indicates an unexpected completion was received.
15	0h RW/1C/V/P	**Completor Abort Status (CA):** Indicates a completer abort was received

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW/1C/V/P	**Completion Timeout Status (CT):** Indicates a completion timed out. This is signaled if Completion Timeout is enabled and a completion fails to return within the amount of time specified by the Completion Timeout Value
13	0h RO	**Flow Control Protocol Error Status (FCPE):** Not supported.
12	0h RW/1C/V/P	**Poisoned TLP Status (PT):** Indicates a poisoned TLP was received.
11:6	0h RO	Reserved.
5	0h RO	**Surprise Down Error Status (SDE):** Surprise Down is not supported.
4	0h RW/1C/V/P	**Data Link Protocol Error Status (DLPE):** Indicates a data link protocol error occurred.
3:1	0h RO	Reserved.
0	0h RO	**Training Error Status (TE):** Not supported.

15.1.40 Uncorrectable Error Mask (UEM)—Offset 108h

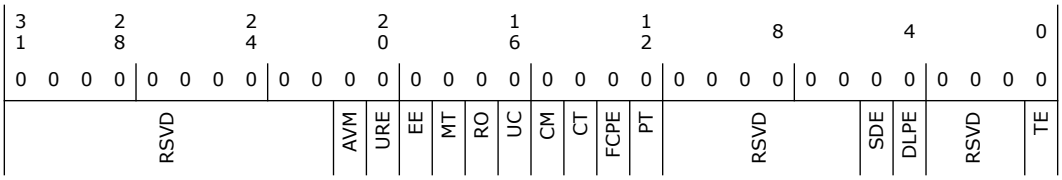
When set, the corresponding error in the UES register is masked, and the logged error will cause no action. When cleared, the corresponding error is enabled. This register is only reset by a loss of core power.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	Reserved.
21	0h RW/P	**ACS Violation Mask (AVM):** Reserved. Access Control Services are not supported
20	0h RW/P	**Unsupported Request Error Mask (URE):** Mask for uncorrectable errors.
19	0h RO	**ECRC Error Mask (EE):** ECRC is not supported.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW/P	**Malformed TLP Mask (MT):** Mask for malformed TLPs
17	0h RW/P	**Receiver Overflow Mask (RO):** Mask for receiver overflows.
16	0h RW/P	**Unexpected Completion Mask (UC):** Mask for unexpected completions.
15	0h RW/P	**Completor Abort Mask (CM):** Mask for completer abort.
14	0h RW/P	**Completion Timeout Mask (CT):** Mask for completion timeouts.
13	0h RO	**Flow Control Protocol Error Mask (FCPE):** Not supported.
12	0h RW/P	**Poisoned TLP Mask (PT):** Mask for poisoned TLPs.
11:6	0h RO	Reserved.
5	0h RO	**Surprise Down Error Mask (SDE):** Surprise Down is not supported.
4	0h RW/P	**Data Link Protocol Error Mask (DLPE):** Mask for data link protocol errors.
3:1	0h RO	Reserved.
0	0h RO	**Training Error Mask (TE):** Not supported.

15.1.41 Uncorrectable Error Severity (UEV)—Offset 10Ch

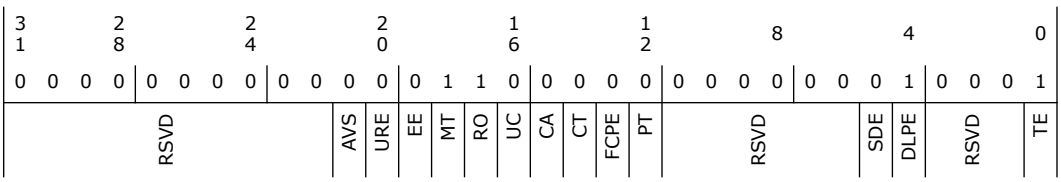
This register gives the option to make an uncorrectable error fatal or non-fatal. An error is fatal if the bit is set. An error is non-fatal if the bit is cleared. This register is only reset by a loss of core power.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 60011h



Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	Reserved.
21	0h RW/P	**ACS Violation Severity (AVS):** Severity for ACS violation.
20	0h RW/P	**Unsupported Request Error Severity (URE):** Severity for unsupported request reception.
19	0h RO	**ECRC Error Severity (EE):** ECRC is not supported.
18	1h RW/P	**Malformed TLP Severity (MT):** Severity for malformed TLP reception.
17	1h RW/P	**Receiver Overflow Severity (RO):** Severity for receiver overflow occurrences.
16	0h RW/P	**Unexpected Completion Severity (UC):** Severity for unexpected completion reception.
15	0h RW/P	**Completor Abort Severity (CA):** Severity for completer abort.
14	0h RW/P	**Completion Timeout Severity (CT):** Severity for completion timeout.
13	0h RO	**Flow Control Protocol Error Severity (FCPE):** Not supported.
12	0h RW/P	**Poisoned TLP Severity (PT):** Severity for poisoned TLP reception.
11:6	0h RO	Reserved.
5	0h RO	**Surprise Down Error Severity (SDE):** Surprise Down is not supported.
4	1h RW/P	**Data Link Protocol Error Severity (DLPE):** Severity for data link protocol errors.
3:1	0h RO	Reserved.
0	1h RO	**Training Error Severity (TE):** TE not supported. This bit is left as RO='1' forease of implementation..

15.1.42 Correctable Error Status (CES)—Offset 110h

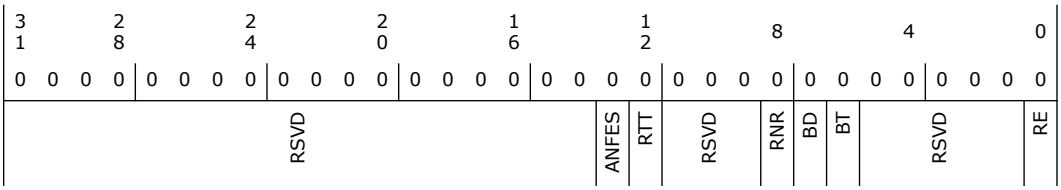
This register is only reset by a loss of core power

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13	0h RW/1C/V/P	**Advisory Non-Fatal Error Status (ANFES):** When set, indicates that an Advisory Non-Fatal Error occurred.
12	0h RW/1C/V/P	**Replay Timer Timeout Status (RTT):** Indicates the replay timer timed out.
11:9	0h RO	Reserved.
8	0h RW/1C/V/P	**Replay Number Rollover Status (RNR):** Indicates the replay number rolled over.
7	0h RW/1C/V/P	**Bad DLLP Status (BD):** Indicates a bad DLLP was received.
6	0h RW/1C/V/P	**Bad TLP Status (BT):** Indicates a bad TLP was received.
5:1	0h RO	Reserved.
0	0h RW/1C/V/P	**Receiver Error Status (RE):** Indicates a receiver error occurred.

15.1.43 Correctable Error Mask (CEM)—Offset 114h

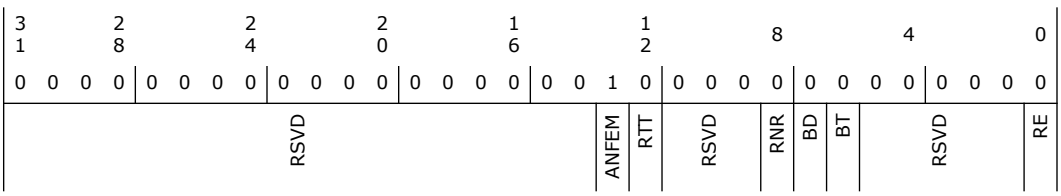
When set, the corresponding error in the CES register is masked, and the logged error will cause no action. When cleared, the corresponding error is enabled. This register is only reset by a loss of core power.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 2000h



Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13	1h RW/P	**Advisory Non-Fatal Error Mask (ANFEM):** When set, masks Advisory Non-Fatal errors from (a) signaling ERR_COR to the device control register and (b) updating the Uncorrectable Error Status register. This register is set by default to enable compatibility with software that does not comprehend Role-Based Error Reporting.
12	0h RW/P	**Replay Timer Timeout Mask (RTT):** Mask for replay timer timeout.
11:9	0h RO	Reserved.
8	0h RW/P	**Replay Number Rollover Mask (RNR):** Mask for replay number rollover.
7	0h RW/P	**Bad DLLP Mask (BD):** Mask for bad DLLP reception.
6	0h RW/P	**Bad TLP Mask (BT):** Mask for bad TLP reception.
5:1	0h RO	Reserved.
0	0h RW/P	**Receiver Error Mask (RE):** Mask for receiver errors.

15.1.44 Advanced Error Capabilities and Control (AECC)—Offset 118h

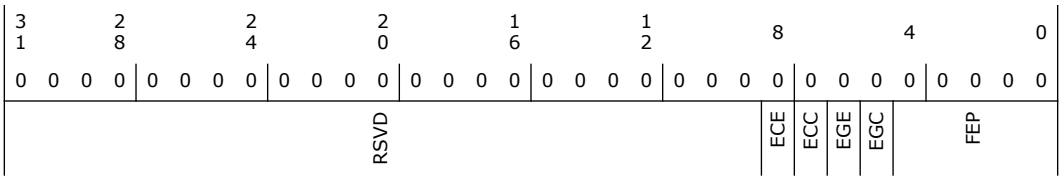
This register is only reset by a loss of core power.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h RO	**ECRC Check Enable (ECE):** ECRC is not supported.
7	0h RO	**ECRC Check Capable (ECC):** ECRC is not supported.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RO	**ECRC Generation Enable (EGE):** ECRC is not supported.
5	0h RO	**ECRC Generation Capabile (EGC):** ECRC is not supported.
4:0	0h RO/V/P	**First Error Pointer (FEP):** Identifies the bit position of the first error reported in the Uncorrectable Error Status Register.

15.1.45 Root Error Command (REC)—Offset 12Ch

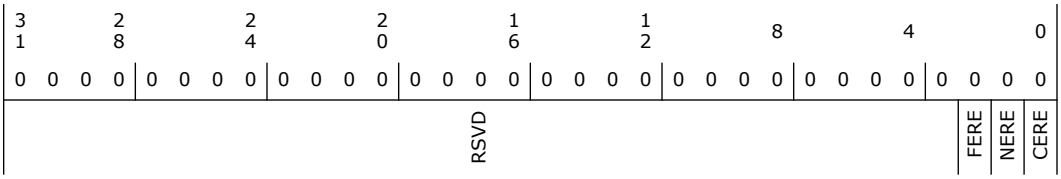
This register allows errors to generate interrupts.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	Reserved.
2	0h RW	**Fatal Error Reporting Enable (FERE):** When set, the root port will generate an interrupt when a fatal error is reported by the attached device.
1	0h RW	**Non-fatal Error Reporting Enable (NERE):** When set, the root port will generate an interrupt when a non-fatal error is reported by the attached device.
0	0h RW	**Correctable Error Reporting Enable (CERE):** When set, the root port will generate an interrupt when a correctable error is reported by the attached device.

15.1.46 Root Error Status (RES)—Offset 130h

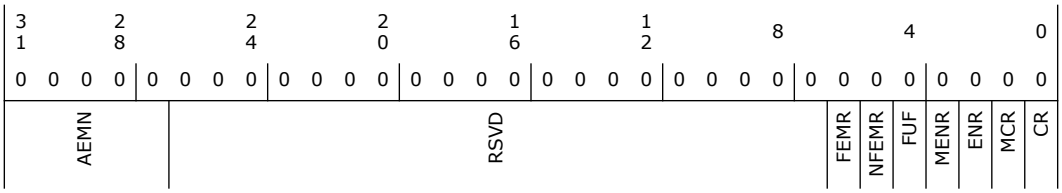
This register can track more than one error and set the 'multiple' bits if a second or subsequent error occurs and the first has not been serviced. This register is only reset by a loss of core power.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**Advanced Error Interrupt Message Number (AEMN):** Reserved. There is only one error interrupt allocated.
26:7	0h RO	Reserved.
6	0h RW/1C/V/P	**Fatal Error Message Received (FEMR):** Set when one or more Fatal Uncorrectable Error Messages have been received.
5	0h RW/1C/V/P	**Non-Fatal Error Messages Received (NFEMR):** Set when one or more Non-Fatal Uncorrectable error messages have been received
4	0h RW/1C/V/P	**First Uncorrectable Fatal (FUF):** Set when the first Uncorrectable Error message received is for a fatal error.
3	0h RW/1C/V/P	**Multiple ERR_FATAL/NONFATAL Received (MENR):** Set when either a fatal or a non-fatal error is received and the ENR bit is already set.
2	0h RW/1C/V/P	**ERR_FATAL/NONFATAL Received (ENR):** Set when either a fatal or a non-fatal error message is received.
1	0h RW/1C/V/P	**Multiple ERR_COR Received (MCR):** Set when a correctable error message is received and the CR bit is already set.
0	0h RW/1C/V/P	**ERR_COR Received (CR):** Set when a correctable error message is received.

15.1.47 Error Source Identification (ESID)—Offset 134h

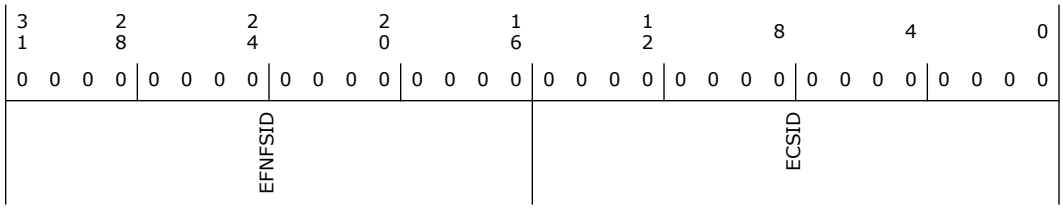
Size:32 bits
Identifies the source (Requester ID) of the first correctable and uncorrectable (Non-Fatal / Fatal) errors reported in the Root Error Status register. This register is only reset by a loss of core power.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO/V/P	**ERR_FATAL/NONFATAL Source Identification (EFNFSID):** Loaded with the Requester ID indicated in the received ERR_FATAL or ERR_NONFATAL Message with the ERR_FATAL/NONFATAL Received register is not already set.
15:0	0h RO/V/P	**ERR_COR Source Identification (ECSID):** Loaded with the Requester ID indicated in the received ERR_COR Message with the ERR_COR Received register is not already set.

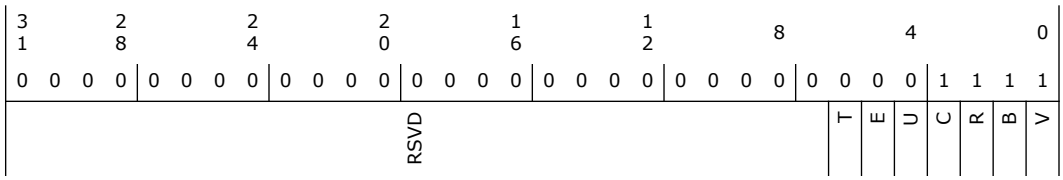
15.1.48 ACS Capability Register (ACSCAPR)—Offset 144h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: Fh



Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	Reserved.
6	0h RO	**ACS Direct Translated P2P (T):** ACS Direct Translated P2P (T): ACS Direct Translated P2P is not supported.
5	0h RO	**ACS P2P Egress Control (E):** ACS P2P Egress Control (E): ACS P2P Egress Control is not supported.
4	0h RO	**ACS Upstream Forwarding (U):** ACS Upstream Forwarding (U): ACS Upstream Forwarding is not supported.
3	1h RW/O	**ACS P2P Completion Redirect (C):** ACS P2P Completion Redirect (C): Required for all Functions that support ACS P2P Request Redirect; must be hardwired to 0b otherwise. If 1b, indicates that the component implements ACS P2P Completion Redirect.

Bit Range	Default & Access	Field Name (ID): Description
2	1h RW/O	**ACS P2P Request Redirect (R):** ACS P2P Request Redirect (R): Required for Root Ports that support peer-to-peer traffic with other Root Ports; required for Switch Downstream Ports; required for multi-function device Functions that support peer-to-peer traffic with other Functions; must be hardwired to 0b otherwise. If 1b, indicates that the component implements ACS P2P Request Redirect.
1	1h RW/O	**ACS Translation Blocking (B):** ACS Translation Blocking (B): Required for Root Ports and Switch Downstream Ports; must be hardwired to 0b otherwise. If 1b, indicates that the component implements ACS Translation Blocking.
0	1h RW/O	**ACS Source Validation (V):** ACS Source Validation (V): Required for Root Ports and Switch Downstream Ports; must be hardwired to 0b otherwise. If 1b, indicates that the component implements ACS Source Validation.

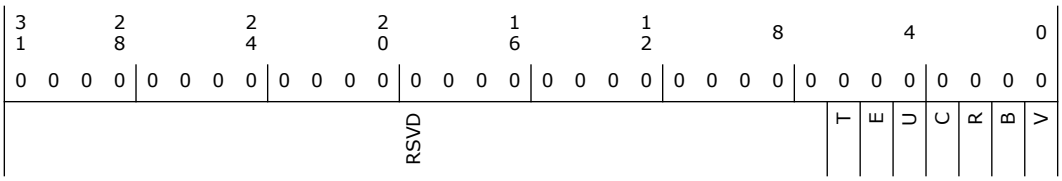
15.1.49 ACS Control Register (ACSCTLR)—Offset 148h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	Reserved.
6	0h RO	**ACS Direct Translated P2P Enable (T):** ACS Direct Translated P2P Enable (T): ACS Direct Translated P2P is not supported.
5	0h RO	**ACS P2P Egress Control Enable (E):** ACS P2P Egress Control Enable (E): ACS P2P Egress Control is not supported.
4	0h RO	**ACS Upstream Forwarding Enable (U):** ACS Upstream Forwarding Enable (U): ACS Upstream Forwarding is not supported.
3	0h RW	**ACS P2P Completion Redirect (C):** ACS P2P Completion Redirect (C): Determines when the component redirects peer-to-peer Completions upstream; applicable only to Read Completions whoseRelaxed Ordering Attribute is clear.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**ACS P2P Request Redirect (R):** ACS P2P Request Redirect (R): Determines when the component redirects peer-to-peer memory Requests targeting another peer port upstream. I/O, Configuration, VDM Messages and Completions are never affected by ACS P2P Request Redirect.
1	0h RW	**ACS Translation Blocking (B):** ACS Translation Blocking (B): When set, the component blocks all upstream Memory Requests whose Address Translation (AT) field is not set to the default value. I/O, Configuration, Completions and Messages are never affected by ACS Translation Blocking.
0	0h RW	**ACS Source Validation (V):** ACS Source Validation (V): When set, the component validates the Bus Number from the Requester ID of upstream Requests against the secondary / subordinate Bus Numbers. I/O, Configuration and Completions are never affected by ACS Source Validation.

15.1.50 L1 Sub-States Extended Capability Header (L1SECH)—Offset 200h

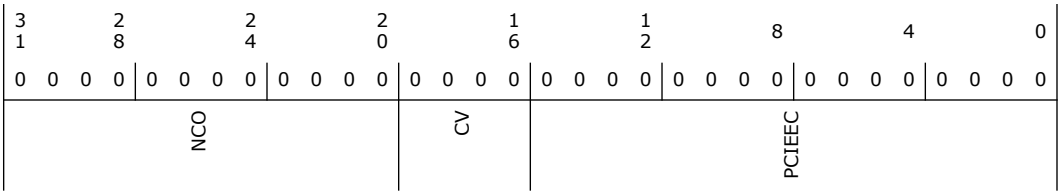
Size:32 bits
Note: When operating in Mobile Express mode, this capability should not be enabled.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW/O	**Next Capability Offset (NCO):** This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh. The bottom 2 bits of this offset are Reserved and must be implemented as 00b and software must mask them to allow for future uses of these bits.
19:16	0h RW/O	**Capability Version (CV):** This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. Must be 1h for this version of the specification. For systems that support L1 Sub-State Extended Capability, BIOS should set this field to 1h
15:0	0h RW/O	**PCI Express Extended Capability ID (PCIEEC):** This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. For systems that support L1 Sub-State Extended Capability, BIOS should set this field to 001Eh. .

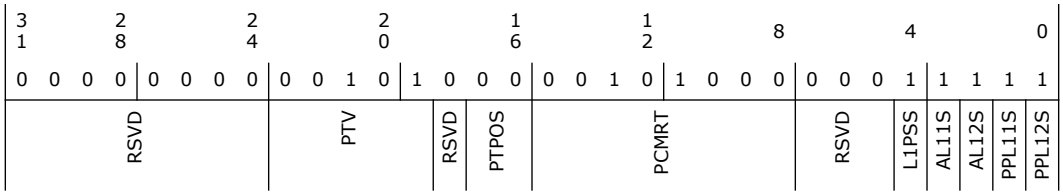
15.1.51 L1 Sub-States Capabilities (L1SCAP)—Offset 204h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 28281Fh



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:19	5h RW/O	**Port Tpower_on Value (PTV):** Along with the Port T_POWER_ON Scale Field in the L1 Substates Capabilities register sets theTime (in us) that this Port requires the port on the opposite side of Link to wait in L1.OFF_EXIT after sampling CLKREQ# asserted before actively driving the interface. Port Tpower_on is calculated by multiplying the value in this field by the value in the Port Tpower_on scale field in the L1 Sub-States Capabilities 2 register. Required for all Ports that support L1.OFF.
18	0h RO	Reserved.
17:16	0h RW/O	**Port Tpower_on Scale (PTPOS):** Specifies the scale used for Tpower_on value field in the L1 Substates Capabilities register. '00b': 2 us '01b': 10 us '10b': 100 us '11b': Reserved Required for all Ports that support L1.OFF.
15:8	28h RW/O	**Port Common Mode Restore Time (PCMRT):** This is the time (in us) required for this Port to re-establish common mode. Required for all ports that support L1.OFF.
7:5	0h RO	Reserved.
4	1h RW/O	**L1 PM Substates Supported (L1PSS):** When Set this bit indicates that this Port supports L1 PM Substates. For compatibility with possible future extensions, software must not enable L1 PM Substates unless this bit is set. This RWO field must be programmed prior to enabling ASPM.
3	1h RW/O	**ASPM L1.1 Substates Supported (AL11S):** When set, this bit indicates that this port supports L1 substates for ASPM L1.SNOOZ. Required for both Upstream and Downstream ports. This RWO field must be programmed prior to enabling ASPM. Register Attribute: Static

Bit Range	Default & Access	Field Name (ID): Description
2	1h RW/O	**ASPM L1.2 Supported (AL12S):** When set, this bit indicates that ASPM_L1.OFF is supported. Required for both Upstream and Downstream ports. This RWO field must be programmed prior to enabling ASPM. Register Attribute: Static
1	1h RW/O	**PCI-PM L1.1 Supported (PPL11S):** When set, this bit indicates that L1.SNOOZ sub-state is supported and this bit must be set by all ports implementing L1 Sub-States. A port that supports L1.OFF must support L1.SNOOZ. Required for both upstream and downstream ports. This RWO field must be programmed prior to enabling ASPM. Register Attribute: Static
0	1h RW/O	**PCI-PM L1.2 Supported (PPL12S):** When set, this bit indicates that L1.OFF power management feature is supported. Required for both upstream and downstream ports. This RWO field must be programmed prior to enabling ASPM. Register Attribute: Static

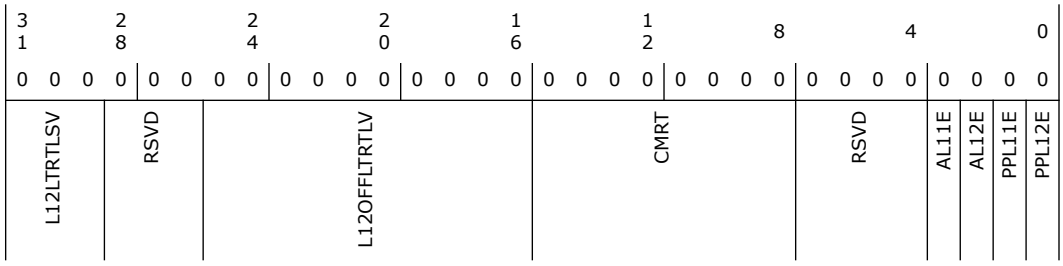
15.1.52 L1 Sub-States Control 1 (L1SCTL1)—Offset 208h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RW	**L1.2 LTR Threshold Latency ScaleValue (L12LTRTLSV):** This field contains the L1.OFF LTR Threshold Latency Scale Value for this particular PCIe root port. The value in this field, together with L12LTRTLV is compared against both the snoop and non-snoop LTR values of the device. 000: L12LTRSTLV times 1 ns 001: L12LTRSTLV times 32 ns 010: L12LTRSTLV times 1024 ns 011: L12LTRSTLV times 32768 ns 100: L12LTRSTLV times 1048576 ns 101: L12LTRSTLV times 33554432 ns Others: Not Permitted. This field must be programmed prior to enabling L1.OFF. Register Attribute: Static
28:26	0h RO	Reserved.
25:16	0h RW	**L1.2 LTR Threshold Latency Value (L12OFFLTRTLV):** This field contains the L1.2 LTR Threshold Latency Value for this particular PCIe root port. The value in this field, together with L12LTRTLSV is compared against both the snoop and non-snoop LTR values of the device. This field must be programmed prior to enabling L1.OFF. Register Attribute: Static

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RW	**Common Mode Restore Time (CMRT):** This is the Tcommon_mode time the PCIe root port needs to continue sending TS1 and refrain from sending TS2 in Recovery state to allow the TX common mode to be established prior to sending TS2. The timer starts from the time when the first TS1 has been sent and the receiver has detected un-squelch. The value in this field defines the time in micro-seconds. This field must be programmed prior to enabling L1.OFF. Register Attribute: Static
7:4	0h RO	Reserved.
3	0h RW	**ASPM L1.1 Enabled (AL11E):** When set, this bit indicates that ASPM L1.SNOOZ substates are enabled for ASPM. Required for both upstream and downstream ports. Register Attribute: Dynamic
2	0h RW	**ASPM L1.2 Enable (AL12E):** When set, this bit indicates that ASPM L1.OFF substates are enabled for PCI-PM. Required for both upstream and downstream ports. Register Attribute: Dynamic
1	0h RW	**PCI-PM L1.SNOOZ Enable (PPL11E):** When set, this bit indicates that PCI-PM L1.SNOOZ power management feature is enabled. If L1.OFF is enabled, L1.SNOOZ must also be enabled. This field must be programmed prior to enabling ASPM L1. Register Attribute: Dynamic Note: If STRPFUSECFG.mPHYIOPMDIS is '1', hardware will always see '0' asan output from this register. BIOS reading this register should always return the correct value.
0	0h RW	**PCI-PM L1.2 Enabled (PPL12E):** When set, this bit indicates that PCI-PM L1.OFF power management feature is enabled. L1.OFF can only be enabled if the platform supports bi-directional CLKREQPLUS#. This field must be programmed prior to enabling ASPM L1. Ports that support L1.OFF shall support Latency Tolerance Reporting. Register Attribute: Dynamic Note: If STRPFUSECFG.mPHYIOPMDIS is '1', hardware will always see '0' asan output from this register. BIOS reading this register should always return the correct value.

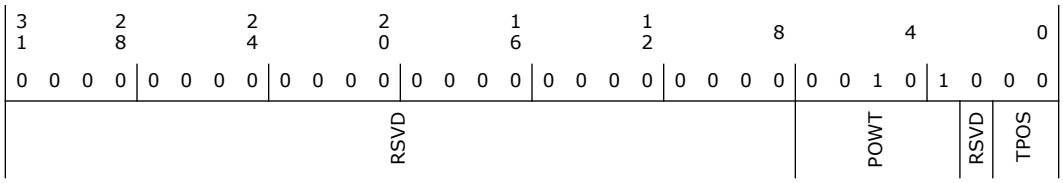
15.1.53 L1 Sub-States Control 2 (L1SCTL2)—Offset 20Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 28h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:3	5h RW	**Power On Wait Time (POWT):** Along with the Tpower_on Scale sets the minimum amount of time (in us) that the Port must wait in L1.OFF EXIT after sampling CLKREQPLUS# asserted before actively driving the interface. The timer starts counting when CLKREQPLUS# is sampled asserts in L1.OFF state. Tpower_on value is calculated by multiplying the value in this field by the value in the TPOS field. This field must be programmed prior to enabling L1.OFF. Register Attribute: Static
2	0h RO	Reserved.
1:0	0h RW	**Tpower_on Scale (TPOS):** Specifies the scale used for Tpower_on value. '00b': 2 us '01b': 10 us '10b': 100us '11b': Reserved. Required for all Ports that support L1.OFF. Register Attribute: Static

15.1.54 Secondary PCI Express Extended Capability Header (SPEECH)—Offset 220h

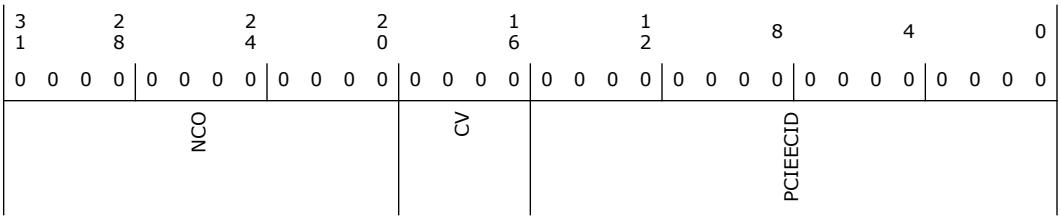
Size:32 bits
Note: When operating in Mobile Express mode, this capability should not be enabled.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW/O	**Next Capability Offset (NCO):** Next Capability Offset (NCO): This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh. The bottom 2 bits of this offset are Reserved and must be implemented as 00b and software must mask them to allow for future uses of these bits.
19:16	0h RW/O	**Capability Version (CV):** Capability Version (CV): This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. For systems that support Secondary PCI Express Extended Capability, BIOS should write a 1h to this register else it should write 0
15:0	0h RW/O	**PCI Express Extended Capability ID (PCIEECID):** PCI Express Extended Capability ID (PCIEECID): This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. PCI Express Extended Capability ID for the Secondary PCI Express Extended Capability is 0019h. For systems that support Secondary PCI Express Extended Capability, BIOS should write a 0019h to this register else it should write 0.

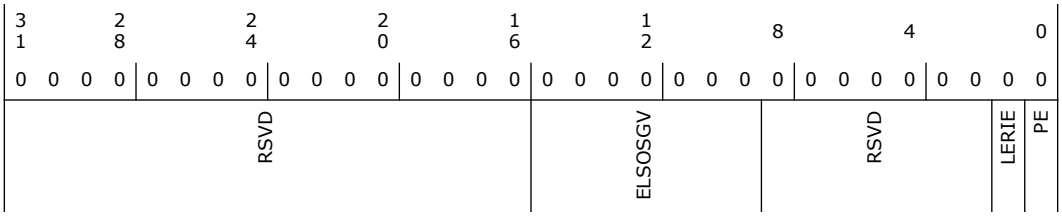
15.1.55 Link Control 3 (LCTL3)—Offset 224h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:9	0h RO	**Enable Lower SKP OS Generation Vector (ELSOSGV):** Enable Lower SKP OS Generation Vector(ELSOSGV): When the Link is in L0 and the bit in this field corresponding to the current Link speed is Set, SKP Ordered Sets are scheduled at the rate defined for SRNS, overriding the rate required based on the clock tolerance architecture. Bit definitions within this field are: Bit 0 2.5 GT/s Bit 1 5.0 GT/s Bit 2 8.0 GT/s Bits 6:3 RsvdP Behavior is undefined if a bit is Set in this field and the corresponding bit in the Lower SKP OS Generation Supported Speeds Vector is not set.

Bit Range	Default & Access	Field Name (ID): Description
8:2	0h RO	Reserved.
1	0h RW	**Link Equalization Request Interrupt Enable (LERIE):** Link Equalization Request Interrupt Enable (LERIE): When set, this bit enables the generation of an interrupt to indicate that the Link Equalization Request bit has been set.
0	0h RW	**Perform Equalization (PE):** Perform Equalization (PE): When this bit is 1b and Link Retrain bit is set with the Target Link Speed field set to 8 GT/s, the Downstream Port must perform Link Equalization. This bit is cleared by Root Port upon entry to Link Equalization

15.1.56 Lane 0 and Lane 1 Equalization Control (L01EC)—Offset 22Ch

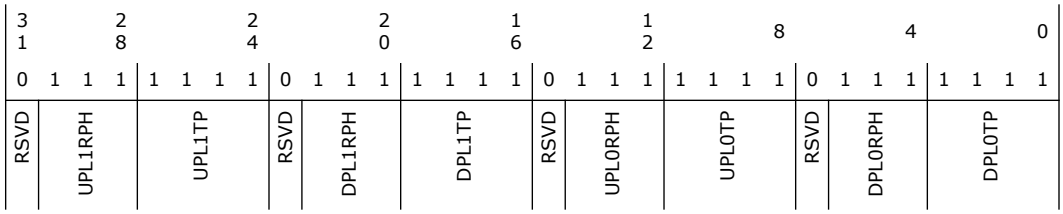
Each entry contains the values for the Lane with the corresponding default Lane number which is invariant to Link width and Lane reversal negotiation that occurs during Link training.
Based on the Port Configuration setting, if the maximum link width of the port is less than x4, the upper lane status bits should be ignored

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 7F7F7F7Fh



Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	Reserved.
30:28	7h RW	**Upstream Port Lane 1 Receiver Preset Hint (UPL1RPH):** Upstream Port Lane 1 Receiver Preset Hint (UPL1RPH): Field contains the Receiver Preset Hint value sent or received during Link Equalization.
27:24	Fh RW	**Upstream Port Lane 1 Transmitter Preset (UPL1TP):** Upstream Port Lane 1 Transmitter Preset (UPL1TP): Field contains the Transmit Preset value sent or received during Link Equalization.
23	0h RO	Reserved.
22:20	7h RW	**Downstream Port Lane 1 Receiver Preset Hint (DPL1RPH):** Downstream Port Lane 1 Receiver Preset Hint (DPL1RPH): Receiver Preset Hint may be used as a hint for receiver equalization by this Port when the Port is operating as a Downstream Port.

Bit Range	Default & Access	Field Name (ID): Description
19:16	Fh RW	**Downstream Port Lane 1 Transmitter Preset (DPL1TP):** Downstream Port Lane 1 Transmitter Preset (DPL1TP): Transmitter Preset used for equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
15	0h RO	Reserved.
14:12	7h RW	**Upstream Port Lane 0 Receiver Preset Hint (UPL0RPH):** Upstream Port Lane 0 Receiver Preset Hint (UPL0RPH): Field contains the Receiver Preset Hint value sent or received during Link Equalization.
11:8	Fh RW	**Upstream Port Lane 0 Transmitter Preset (UPL0TP):** Upstream Port Lane 0 Transmitter Preset (UPL0TP): Field contains the Transmit Preset value sent or received during Link Equalization.
7	0h RO	Reserved.
6:4	7h RW	**Downstream Port Lane 0 Receiver Preset Hint (DPL0RPH):** Downstream Port Lane 0 Receiver Preset Hint (DPL0RPH): Receiver Preset Hint may be used as a hint for receiver equalization by this Port when the Port is operating as a Downstream Port.
3:0	Fh RW	**Downstream Port Lane 0 Transmitter Preset (DPL0TP):** Downstream Port Lane 0 Transmitter Preset (DPL0TP): Transmitter Preset used for equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.

15.1.57 Lane 2 and Lane 3 Equalization Control (L23EC)—Offset 230h

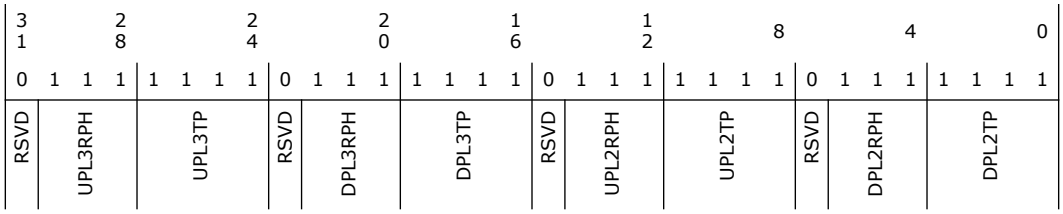
Each entry contains the values for the Lane with the corresponding default Lane number which is invariant to Link width and Lane reversal negotiation that occurs during Link training.
Based on the Port Configuration setting, if the maximum link width of the port is less than x4, the upper lane status bits should be ignored

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 7F7F7F7Fh



Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	Reserved.
30:28	7h RW	**Upstream Port Lane 3 Receiver Preset Hint (UPL3RPH):** Upstream Port Lane 3 Receiver Preset Hint (UPL3RPH): Field contains the Receiver Preset Hint value sent or received during Link Equalization.
27:24	Fh RW	**Upstream Port Lane 3 Transmitter Preset (UPL3TP):** Upstream Port Lane 3 Transmitter Preset (UPL3TP): Field contains the Transmit Preset value sent or received during Link Equalization.
23	0h RO	Reserved.
22:20	7h RW	**Downstream Port Lane 3 Receiver Preset Hint (DPL3RPH):** Downstream Port Lane 3 Receiver Preset Hint (DPL3RPH): Receiver Preset Hint may be used as a hint for receiver equalization by this Port when the Port is operating as a Downstream Port.
19:16	Fh RW	**Downstream Port Lane 3 Transmitter Preset (DPL3TP):** Downstream Port Lane 3 Transmitter Preset (DPL3TP): Transmitter Preset used for equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
15	0h RO	Reserved.
14:12	7h RW	**Upstream Port Lane 2 Receiver Preset Hint (UPL2RPH):** Upstream Port Lane 2 Receiver Preset Hint (UPL2RPH): Field contains the Receiver Preset Hint value sent or received during Link Equalization.
11:8	Fh RW	**Upstream Port Lane 2 Transmitter Preset (UPL2TP):** Upstream Port Lane 2 Transmitter Preset (UPL2TP): Field contains the Transmit Preset value sent or received during Link Equalization.
7	0h RO	Reserved.
6:4	7h RW	**Downstream Port Lane 2 Receiver Preset Hint (DPL2RPH):** Downstream Port Lane 2 Receiver Preset Hint (DPL2RPH): Receiver Preset Hint may be used as a hint for receiver equalization by this Port when the Port is operating as a Downstream Port.
3:0	Fh RW	**Downstream Port Lane 2 Transmitter Preset (DPL2TP):** Downstream Port Lane 2 Transmitter Preset (DPL2TP): Transmitter Preset used for equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.

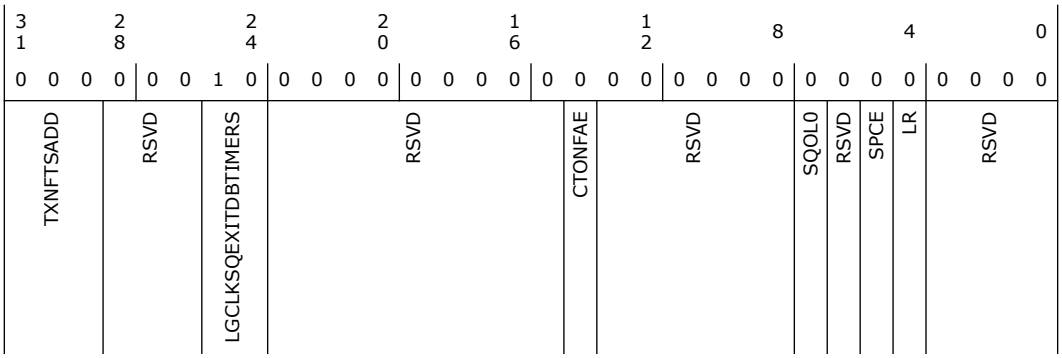
15.1.58 PCI Express Configuration (PCIEDBG)—Offset 324h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 2000000h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RW	**Transmit nFTS Adder (TXNFTSADD):** This field specifies the 1-based number of additional nFTS sets to be transmitted to the opposite device on TXL0s exit on top of the actual number of nFTS sets. 000: No additional nFTS to be transmitted on top of actual nFTS. 001: 1 additional nFTS to be transmitted on top of actual nFTS. 010: 2 additional nFTS to be transmitted on top of actual nFTS. : : 111: 7 additional nFTS to be transmitted on top of actual nFTS.
28:26	0h RO	Reserved.
25:24	2h RW	**Configuration Field (LGCLKSQEXITDBTIMERS):** BIOS may program this register bit.
23:15	0h RO	Reserved.
14	0h RW	**Configuration Field (CTONFAE):** BIOS may program this register bit.
13:8	0h RO	Reserved.
7	0h RW	**Configuration Field (SQOL0):** BIOS may program this register bit.
6	0h RO	Reserved.
5	0h RW	**Configuration Field (SPCE):** BIOS may program this register bit.
4	0h RO/V	**Lane Reversal (LR):** This register reflects the PCIe* Lane Reversal Configuration soft strap. It defines if the Root Port associated with a PCIe* Controller is configured with Lane Reversal enabled or disabled 0 = Disabled 1 = Enabled
3:0	0h RO	Reserved.

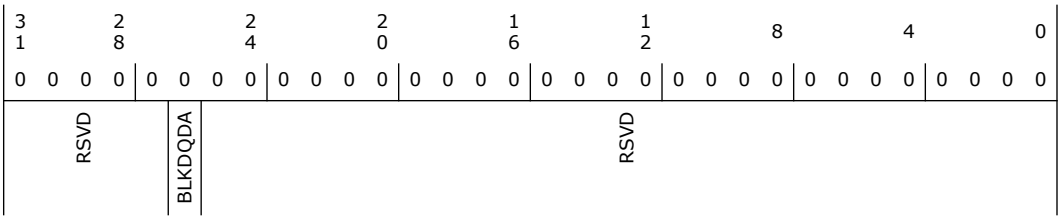
15.1.59 PCI Express Additional Link Control (PCIEALC)—Offset 338h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	Reserved.
26	0h RW/V/P	**Block Detect.Quiet to Detec.Active Transition (BLKDQDA):** 0: Allow transition (Normal Operation) 1: Block transition. Prevents the present state from leaving the Detect.Quiet state. Note that this bit has no effect unless the present state is in the Detect.Quiet state. It will not force the present state into Detect.Quiet from any other state. Typically a warm reset of the platform is required after this bit is set.
25:0	0h RO	Reserved.

15.1.60 Additional Configuration 2 (LTROVR)—Offset 400h

BIOS may need to program this register.

15.1.61 Additional Configuration 3 (LTROVR2)—Offset 404h

BIOS may need to program this register.

15.1.62 Additional Configuration 4 (PCIEPMECTL)—Offset 420h

BIOS may need to program this register.

15.1.63 Equalization Configuration 1 (EQCFG1)—Offset 450h

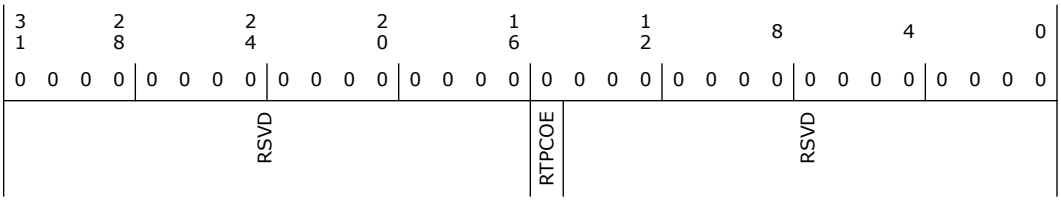
Note: This register must be configured prior to enabling 8.0 GT/s data rate

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	0h RW	**Remote Transmitter Preset/Coefficient Override Enable (RTPCOE): (RTPCOE):** 0 = Reserved 1 = Enables Set Preset/Coefficient values specified by the fields in RTPCL1 and RTPCL2
14:0	0h RO	Reserved.

15.1.64 Remote Transmitter Preset/Coefficient List 1 (RTPCL1)—Offset 454h

Note: This register must be configured prior to enabling 8.0 GT/s data rate

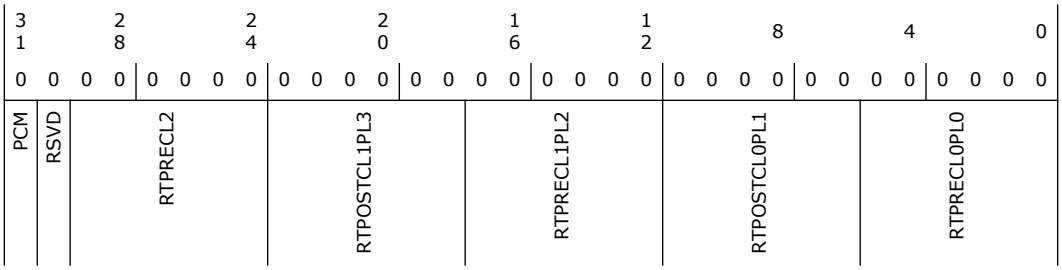
Access Method

Type: CFG Register (Size: 32 bits)

Device: 28

Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Preset/Coefficient Mode (PCM):** This bit defines whether the Preset values or Coefficient values should be sent to the remote TX to adjust the remote TX settings used in Phase 3 of Link Equalization 0 = Preset Mode is enabled 1 = Coefficient Mode is enabled
30	0h RO	Reserved.
29:24	0h RW	**Remote Transmitter Pre-Cursor Coefficient List 2 (RTPRECL2):** If RTPCL1.PCM = 0 these bits are not applicable If RTPCL1.PCM = 1 these bits represent the PCIe* Controller Lane 2 Pre-Cursor Coefficient Value
23:18	0h RW	**Remote Transmitter Post-Cursor Coefficient List 1/Preset List 3 (RTPOSTCL1PL3):** If RTPCL1.PCM = 0 these bits represent the PCIe* Controller Lane 3 Preset value If RTPCL1.PCM = 1 these bits represent the PCIe* Controller Lane 1 Post-Cursor Coefficient value

Bit Range	Default & Access	Field Name (ID): Description
17:12	0h RW	**Remote Transmitter Pre-Cursor Coefficient List 1/Preset List 2 (RTPRECL1PL2):** If RTPCL1.PCM = 0 these bits represent the PCIe* Controller Lane 2 Preset value If RTPCL1.PCM = 1 these bits represent the PCIe* Controller Lane 1 Pre-Cursor Coefficient value
11:6	0h RW	**Remote Transmitter Post-Cursor Coefficient List 0/Preset List 1 (RTPOSTCL0PL1):** If RTPCL1.PCM = 0 these bits represent the PCIe* Controller Lane 1 Preset value If RTPCL1.PCM = 1 these bits represent the PCIe* Controller Lane 0 Post-Cursor Coefficient value
5:0	0h RW	**Remote Transmitter Pre-Cursor Coefficient List 0/Preset List 0 (RTPRECL0PL0):** If RTPCL1.PCM = 0 these bits represent the PCIe* Controller Lane 0 Preset value If RTPCL1.PCM = 1 these bits represent the PCIe* Controller Lane 0 Pre-Cursor Coefficient value

15.1.65 Remote Transmitter Preset/Coefficient List 2 (RTPCL2) (RTPCL2)—Offset 458h

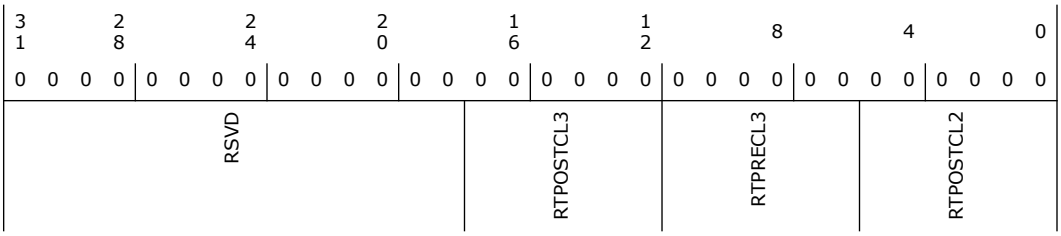
Note: This register must be configured prior to enabling 8.0 GT/s data rate

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17:12	0h RW	**Remote Transmitter Post-Cursor Coefficient List 3 (RTPOSTCL3): (RTPOSTCL3):** If RTPCL1.PCM = 0 these bits are not applicable If RTPCL1.PCM = 1 these bits represent the PCIe* Controller Lane 3 Post-Cursor Coefficient Value
11:6	0h RW	**Remote Transmitter Pre-Cursor Coefficient List 3 (RTPRECL3): (RTPRECL3):** If RTPCL1.PCM = 0 these bits are not applicable If RTPCL1.PCM = 1 these bits represent the PCIe* Controller Lane 3 Pre-Cursor Coefficient value
5:0	0h RW	**Remote Transmitter Post-Cursor Coefficient List 2 (RTPOSTCL2): (RTPOSTCL2):** If RTPCL1.PCM = 0 these bits are not applicable If RTPCL1.PCM = 1 these bits represent the PCIe* Controller Lane 2 Post-Cursor Coefficient Value

§ §

16 I²C Interface (D25:F1/F2, D21:F0/F1/F2/F3)

16.1 I²C PCI Configuration Registers Summary

Table 16-1. Summary of I²C PCI Configuration Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	Device ID and Vendor ID Register (DEVVENDID)—Offset 0h	X_8086
4h	7h	Status and Command (STATUSCOMMAND)—Offset 4h	100000h
8h	Bh	Revision ID and Class Code (REVCLASSCODE)—Offset 8h	118000XXh
Ch	Fh	Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch	0h
10h	13h	Base Address Register (BAR)—Offset 10h	0h
14h	17h	Base Address Register High (BAR_HIGH)—Offset 14h	0h
18h	1Bh	Base Address Register 1 (BAR1)—Offset 18h	0h
1Ch	1Fh	Base Address Register1 High (BAR1_HIGH)—Offset 1Ch	0h
2Ch	2Fh	Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch	0h
30h	33h	Expansion ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h	0h
34h	37h	Capabilities Pointer (CAPABILITYPTR)—Offset 34h	80h
3Ch	3Fh	Interrupt Register (INTERRUPTREG)—Offset 3Ch	100h
80h	83h	Power Management Capability ID (POWERCAPID)—Offset 80h	00030001h
84h	87h	PME Control and Status (PMECTRLSTATUS)—Offset 84h	8h
90h	93h	PCI Device Idle Capability Record (PCIDEVIDLE_CAP_RECORD)—Offset 90h	F0140009h
98h	9Bh	SW LTR Update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG)—Offset 98h	0h
9Ch	9Fh	Device IDLE pointer register (DEVICE_IDLE_POINTER_REG)—Offset 9Ch	0h
A0h	A3h	Device PG Config (D0I3_MAX_POW_LAT_PG_CONFIG)—Offset A0h	800h

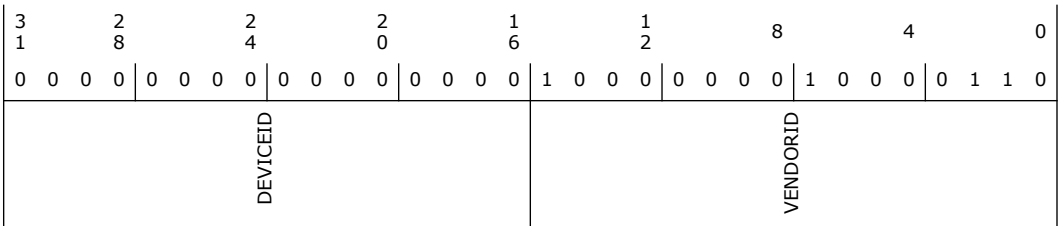
16.1.1 Device ID and Vendor ID Register (DEVVENDID)—Offset 0h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 21
Function: 0

Default: xxxx8086



Bit Range	Default & Access	Field Name (ID): Description
31:16	-- RO	**Device ID (DEVICEID):** This is a 16-bit value assigned to the controller. See the Device and Version ID Table in Volume 1 for the default value.
15:0	8086h RO	**Vendor ID (VENDORID)** Identifies the manufacturer of the device.

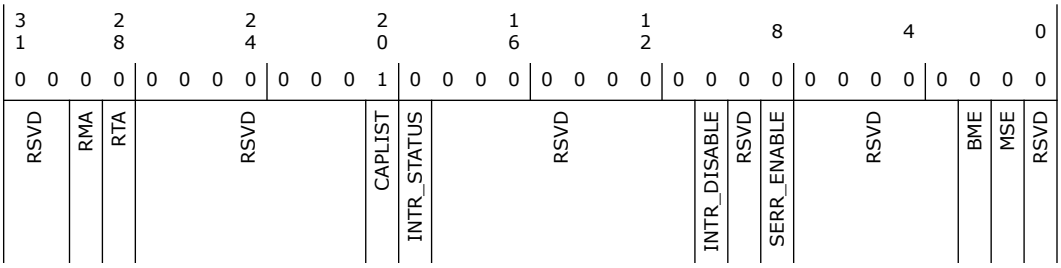
16.1.2 Status and Command (STATUSCOMMAND)—Offset 4h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 100000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29	0h RW/1C	**Received Master Abort (RMA):** If the completion status received from is UR, this bit is set. S/W writes a '1' to this bit to clear it.
28	0h RW/1C	**Received Target Abort (RTA):** If the completion status received is CA, this bit is set. S/W writes a '1' to this bit to clear it.
27:21	0h RO	Reserved.
20	1h RO	**Capabilities List (CAPLIST):** Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h.
19	0h RO	**Interrupt Status (INTR_STATUS):** This bit reflects state of interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the device's/function's interrupt message be sent. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. This bit reflects Legacy interrupt status.

Bit Range	Default & Access	Field Name (ID): Description
18:11	0h RO	Reserved.
10	0h RW	**Interrupt Disable (INTR_DISABLE):** Setting this bit disables INTx assertion. The interrupt disabled is legacy INTx# interrupt.
9	0h RO	Reserved.
8	0h RW	**SERR# Enable (SERR_ENABLE):** Not implemented
7:3	0h RO	Reserved.
2	0h RW	**Bus Master Enable (BME)**
1	0h RW	**Memory Space Enable (MSE):** 0 = Disables memory mapped Configuration space. 1 = Enables memory mapped Configuration space.
0	0h RO	Reserved.

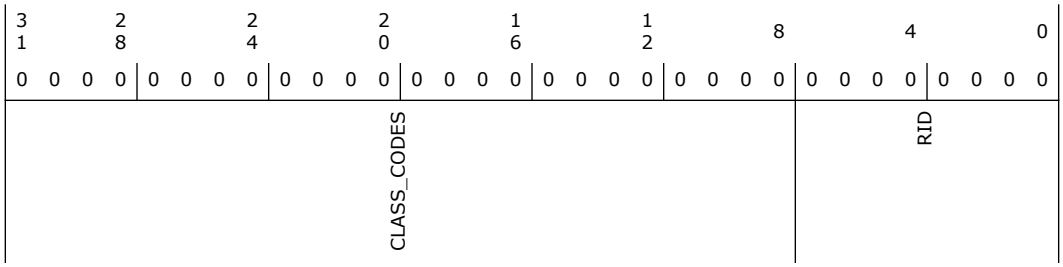
16.1.3 Revision ID and Class Code (REVCLASSCODE)—Offset 8h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:8	118000h RO	**Class Codes (CLASS_CODES):** The register is read-only and is used to identify the generic function of the device.
7:0	0h RO	**Revision ID (RID):** Indicates stepping of the host controller. Refer to Device and Revision ID table in Volume 1 for specific value.

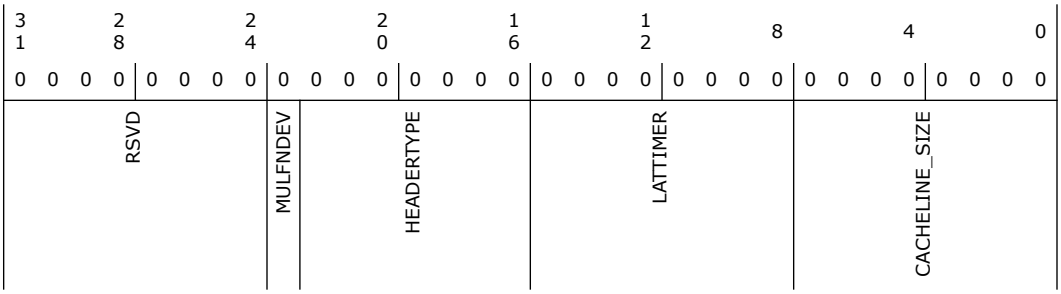
16.1.4 Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RO	**Multi Function Device (MULFNDEV):** 0 = Single Function Device 1 = Multi Function device
22:16	0h RO	**HEADERTYPE:** Implements Type 0 Configuration header.
15:8	0h RO	**Latency Timer (LATTIMER)**
7:0	0h RW	**CACHELINE_SIZE:** Cache Line Size

16.1.5 Base Address Register (BAR)—Offset 10h

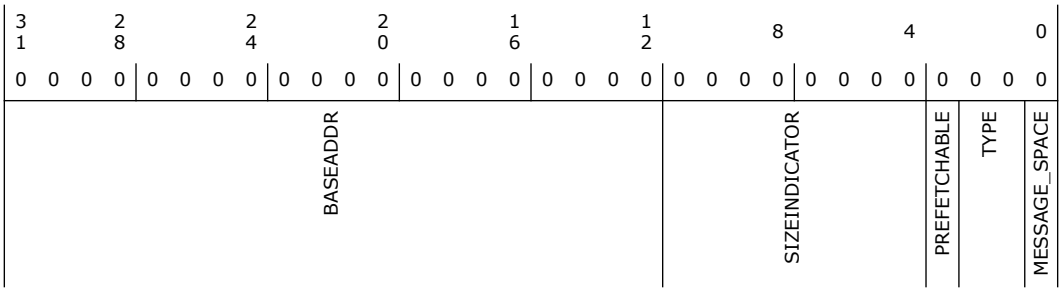
Bits [31:12] indicate the Base Address register. Power-up software can determine how much address space the Interface Module requires by writing a value of all ones to the register and then reading the value back. The register returns zeros in all don't-care address bits, effectively specifying the address space required.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW	**Base Address (BASEADDR):** Provides system memory base address for the controller.
11:4	0h RO	**Size Indicator (SIZEINDICATOR)**
3	0h RO	**Prefetchable (PREFETCHABLE):** Indicates that this BAR is not prefetchable.
2:1	0h RO	**Type (TYPE):** 00 indicates BAR lies in 32bit address range 10 Indicates BAR lies in 64 bit address range
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE):** '0' Indicates this BAR is present in the memory space.

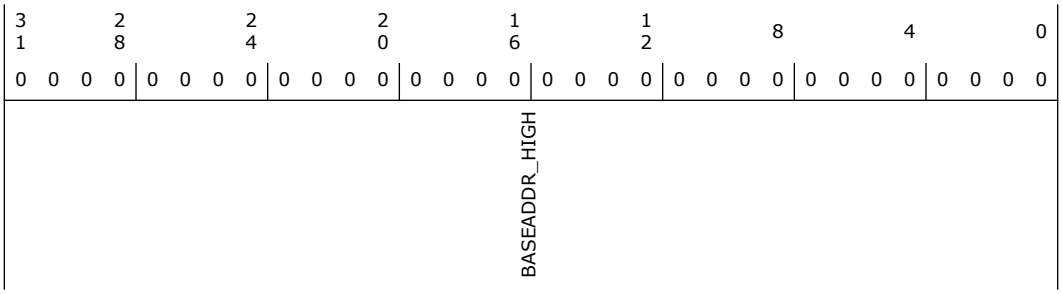
16.1.6 Base Address Register High (BAR_HIGH)—Offset 14h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Base Address High (BASEADDR_HIGH)**

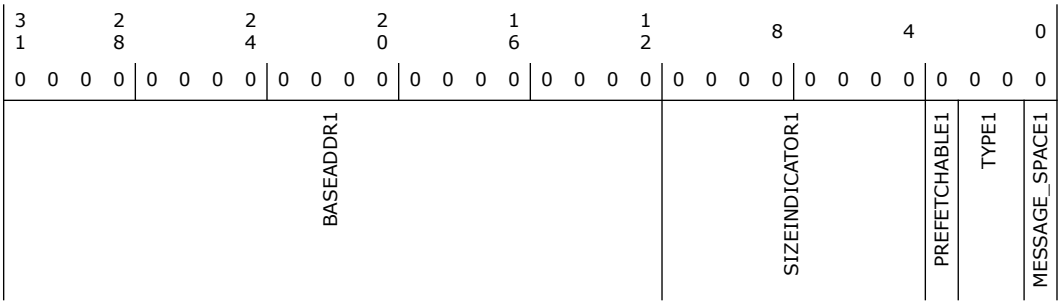
16.1.7 Base Address Register 1 (BAR1)—Offset 18h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW	**Base Address Register1 (BASEADDR1):** This field is present if BAR1 is enabled.
11:4	0h RO	**Size Indicator (SIZEINDICATOR1):** Always will be zero as minimum size is 4K.
3	0h RO	**Prefetchable (PREFETCHABLE1):** Indicates that this BAR is not prefetchable.
2:1	0h RO	**Type (TYPE1):** 00 indicates BAR lies in 32bit address range 10 Indicates BAR lies in 64 bit address range.
0	0h RO	**MESSAGE_SPACE1**

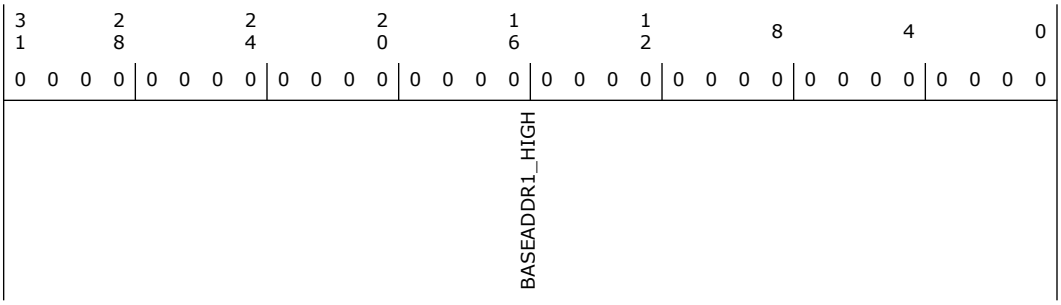
16.1.8 Base Address Register1 High (BAR1_HIGH)—Offset 1Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Base Address High 1 (BASEADDR1_HIGH)**

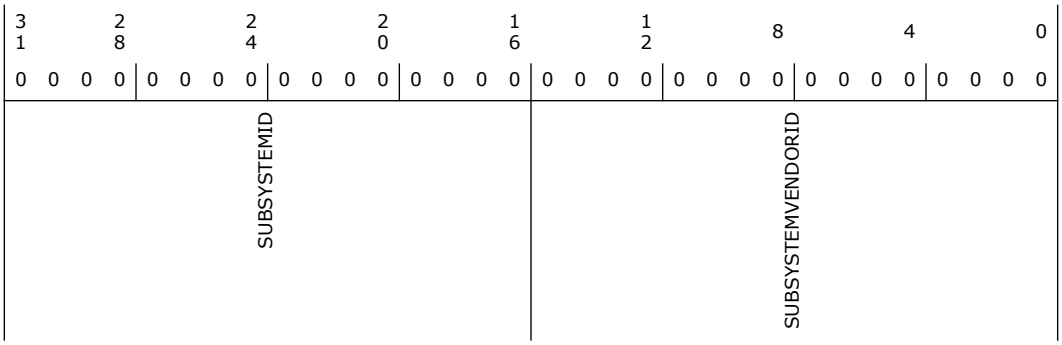
16.1.9 Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW/O	**Subsystem ID (SUBSYSTEMID):** The register, in combination with the Subsystem Vendor ID register make it possible for the operating environment to distinguish one subsystem from the other. This register is a Read Write Once type register.
15:0	0h RW/O	**Subsystem Vendor ID (SUBSYSTEMVENDORID):** The register, in combination with the Subsystem ID register, enables the operating environment to distinguish one subsystem from the other. This register is a Read Write Once register.

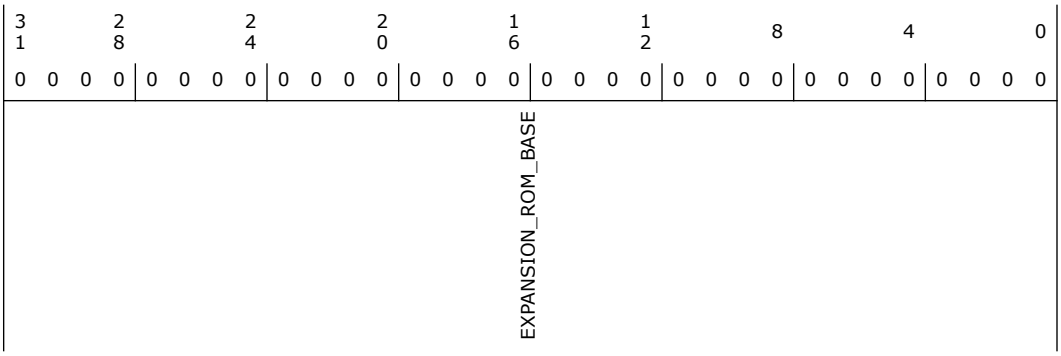
16.1.10 Expansion ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**Expansion ROM Base (EXPANSION_ROM_BASE)** Value of 0 indicates no support for Expansion ROM.

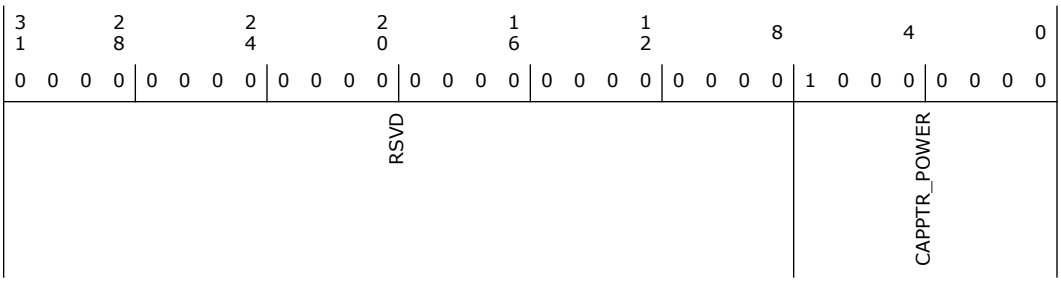
16.1.11 Capabilities Pointer (CAPABILITYPTR)—Offset 34h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 80h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	80h RO	**Capabilities Pointer (CAPPTR_POWER):** Indicates what the next capability is. This capability points to the PM Capability (0x80) structure.

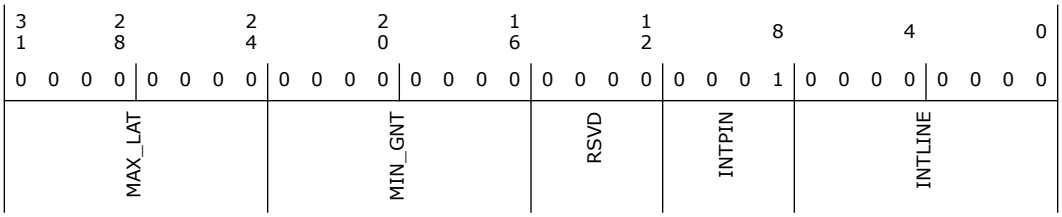
16.1.12 Interrupt Register (INTERRUPTREG)—Offset 3Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 100h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Max Latency (MAX_LAT):** Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	0h RO	**Min Latency (MIN_GNT):** Value of 0 indicates device has no major requirements for the settings of latency timers
15:12	0h RO	Reserved.
11:8	1h RO	**Interrupt Pin (INTPIN)**
7:0	0h RW	**Interrupt Line (INTLINE):** Used to communicate to software the interrupt line that the interrupt pin is connected to.

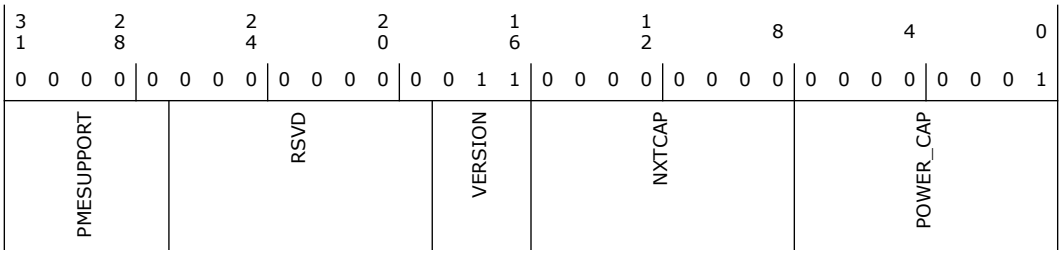
16.1.13 Power Management Capability ID (POWERCAPID)—Offset 80h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 48030001h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**PME Support (PMESUPPORT)**
26:19	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
18:16	3h RO	**Version (VERSION):** Indicates support for Revision 1.2 of the PCI Power Management Specification
15:8	0h RO	**Next Capability (NXTCAP):** Points to the next capability structure. This points to NULL.
7:0	1h RO	**Power Management Capability (POWER_CAP):** Indicates power management capability.

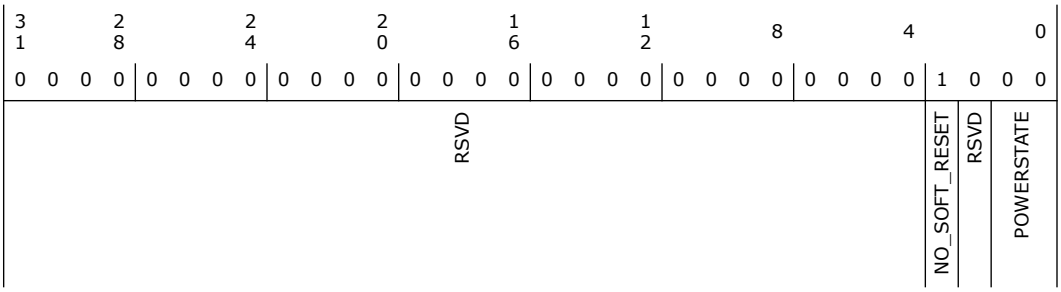
16.1.14 PME Control and Status (PMECTRLSTATUS)—Offset 84h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 8h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3	1h RO	**No Soft Reset (NO_SOFT_RESET):** When set, this bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved.
2	0h RO	Reserved.
1:0	0h RW	**Power State (POWERSTATE):** This field is used both to determine the current power state and to set a new power state. The values are: 00 = D0 state 11 = D3HOT state Others = Reserved Notes: If software attempts to write a value of 01b or 10b in to this field,the data is discarded and no state change occurs. When in the D3HOT states, interrupts are blocked.

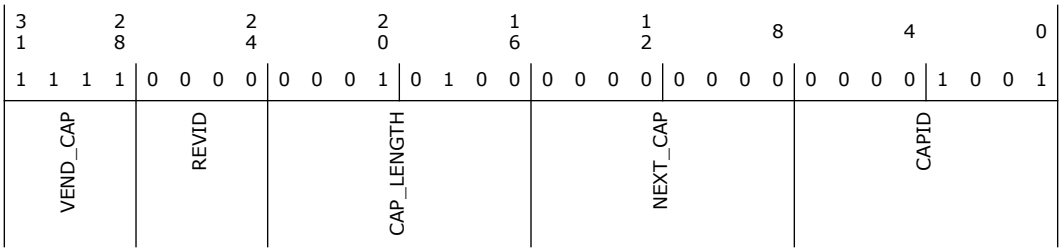
16.1.15 PCI Device Idle Capability Record (PCIDEVIDLE_CAP_RECORD)—Offset 90h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 21
Function: 0

Default: F0140009h



Bit Range	Default & Access	Field Name (ID): Description
31:28	Fh RO	**Vendor Capability (VEND_CAP):** Indicates this is Vendor Specific capability.
27:24	0h RO	**Revision ID (REVID):** Revision ID of capability structure
23:16	14h RO	**Length (CAP_LENGTH):** Indicates the number of bytes in the capability structure.
15:8	0h RO	**Next Capability (NEXT_CAP):** Points to the next capability structure. This points to NULL.
7:0	9h RO	**Capability ID (CAPID)**

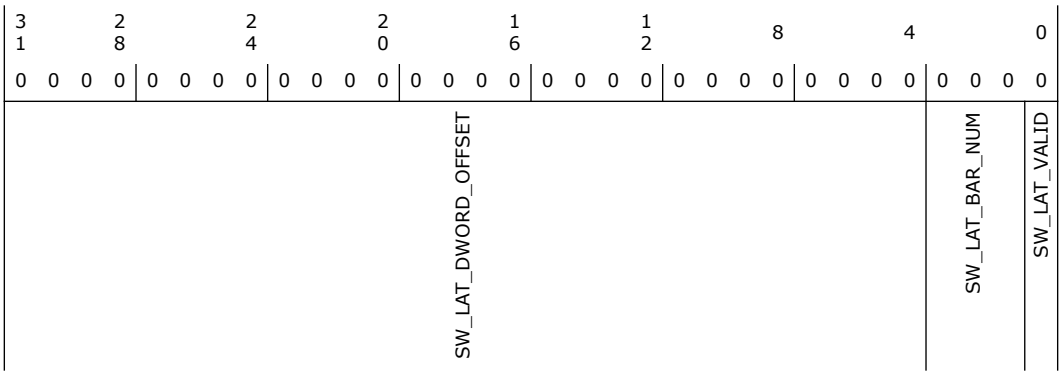
16.1.16 SW LTR Update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG)—Offset 98h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Location Pointer Offset (SW_LAT_DWORD_OFFSET):** This register contains the location pointer to the SW LTR register in MMIO space, as an offset from the specified BAR. The value of this register is a don't care, if the Valid bit is not set.
3:1	0h RO	**BAR Number (SW_LAT_BAR_NUM):** Indicates that the SW LTR update MMIO location is always at BAR0.
0	0h RO	**Valid (SW_LAT_VALID)**

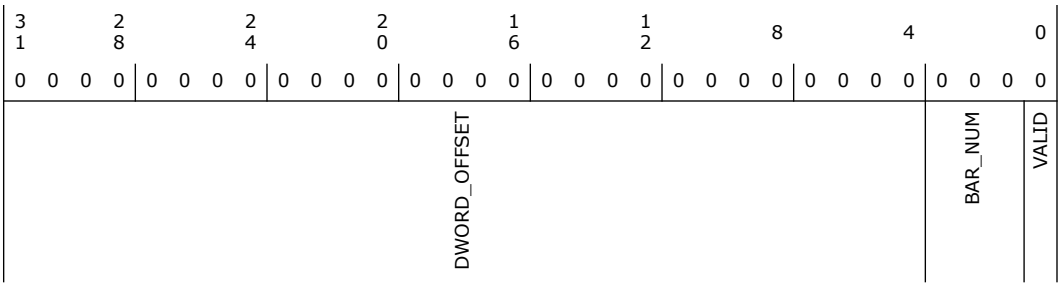
16.1.17 Device IDLE pointer register (DEVICE_IDLE_POINTER_REG)—Offset 9Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**DevIdle Pointer (DWORD_OFFSET):** This register contains the location pointer to the DevIdle register in MMIO space, as an offset from the specified BAR. The value of this register is a don't care, if the Valid bit is not set.
3:1	0h RO	**BAR_NUM:** Indicates that the DevIdle update MMIO location is always at BAR0
0	0h RO	**Valid (VALID):** 0= not valid 1= valid

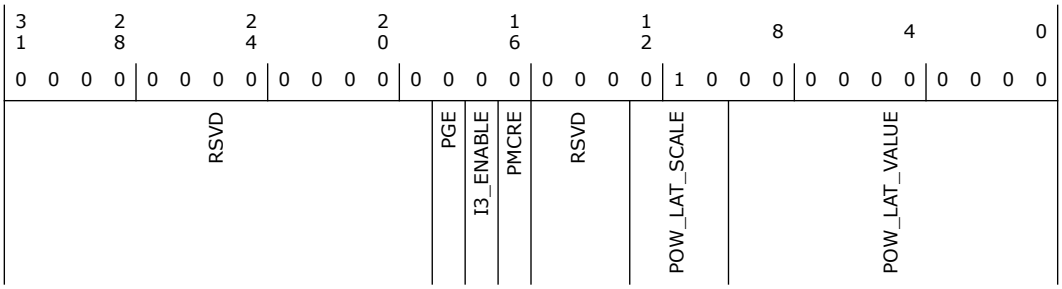
16.1.18 Device PG Config (D0I3_MAX_POW_LAT_PG_CONFIG)—Offset A0h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 800h



Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	Reserved.
18	0h RW	**Power Gate Enable (PGE):** If clear, then the controller will never request a PG. If set, then the controller may request PG when proper conditions are met. Note: This Bit must be set by BIOs for PG to function
17	0h RW	**I3 Enable (I3_ENABLE):** If '1', then the function will power gate when idle and the DevIdle register (DevIdleC[2] = '1') is set.
16	0h RW	**PMC Request Enable (PMCRE):** If this bit is set to '1', the function will power gate when idle.
15:13	0h RO	Reserved.
12:10	2h RW/O	**Power On Latercy Scale (POW_LAT_SCALE):** Support for codes 010 (1us) or 011 (32us) for Exit Latency Scale (1us - 32ms total span) only. This value is written by BIOS to communicate to the Driver.
9:0	0h RW/O	**Power On Latency Value (POW_LAT_VALUE):** This value is written by BIOS to communicate to the Driver.

16.2 I²C Memory Mapped Registers Summary

The registers in this section are memory-mapped registers based on the BAR defined in PCH Configuration space.

Table 16-2. Summary of I²C Memory Mapped Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	I2C Control (IC_CON)—Offset 0h	77h
4h	7h	I2C Target Address (IC_TAR)—Offset 4h	1055h
Ch	Fh	I2C High Speed Master Mode Code Address (IC_HS_MADDR)—Offset Ch	1h
10h	13h	I2C Rx/Tx Data Buffer and Command (IC_DATA_CMD)—Offset 10h	0h
14h	17h	Standard Speed I2C Clock SCL High Count (IC_SS_SCL_HCNT)—Offset 14h	1F4h
18h	1Bh	Standard Speed I2C Clock SCL Low Count (IC_SS_SCL_LCNT)—Offset 18h	24Ch
1Ch	1Fh	Fast Speed I2C Clock SCL High Count (IC_FS_SCL_HCNT)—Offset 1Ch	4Bh
20h	23h	Fast Speed I2C Clock SCL Low Count (IC_FS_SCL_LCNT)—Offset 20h	A3h
2Ch	2Fh	I2C Interrupt Status (IC_INTR_STAT)—Offset 2Ch	0h
30h	33h	I2C Interrupt Mask (IC_INTR_MASK)—Offset 30h	8FFh
34h	37h	I2C Raw Interrupt Status (IC_RAW_INTR_STAT)—Offset 34h	0h

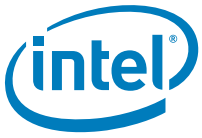


Table 16-2. Summary of I2C Memory Mapped Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
38h	3Bh	I2C Receive FIFO Threshold (IC_RX_TL)—Offset 38h	0h
3Ch	3Fh	I2C Transmit FIFO Threshold (IC_TX_TL)—Offset 3Ch	0h
40h	43h	Clear Combined and Individual Interrupt (IC_CLR_INTR)—Offset 40h	0h
44h	47h	Clear RX_UNDER Interrupt (IC_CLR_RX_UNDER)—Offset 44h	0h
48h	4Bh	Clear RX_OVER Interrupt (IC_CLR_RX_OVER)—Offset 48h	0h
4Ch	4Fh	Clear TX_OVER Interrupt (IC_CLR_TX_OVER)—Offset 4Ch	0h
50h	53h	Clear RD_REQ Interrupt (IC_CLR_RD_REQ)—Offset 50h	0h
54h	57h	Clear TX_ABRT Interrupt (IC_CLR_TX_ABRT)—Offset 54h	0h
58h	5Bh	Clear RX_DONE Interrupt (IC_CLR_RX_DONE)—Offset 58h	0h
5Ch	5Fh	Clear ACTIVITY Interrupt (IC_CLR_ACTIVITY)—Offset 5Ch	0h
60h	63h	Clear STOP_DET Interrupt (IC_CLR_STOP_DET)—Offset 60h	0h
64h	67h	Clear START_DET Interrupt (IC_CLR_START_DET)—Offset 64h	0h
68h	6Bh	Clear GEN_CALL Interrupt (IC_CLR_GEN_CALL)—Offset 68h	0h
6Ch	6Fh	I2C Enable (IC_ENABLE)—Offset 6Ch	0h
70h	73h	I2C Status (IC_STATUS)—Offset 70h	6h
74h	77h	I2C Transmit FIFO Level (IC_TXFLR)—Offset 74h	0h
78h	7Bh	I2C Receive FIFO Level (IC_RXFLR)—Offset 78h	0h
7Ch	7Fh	I2C SDA Hold Time Length (IC_SDA_HOLD)—Offset 7Ch	1h
80h	83h	I2C Transmit Abort Source (IC_TX_ABRT_SOURCE)—Offset 80h	0h
88h	8Bh	DMA Control (IC_DMA_CR)—Offset 88h	0h
8Ch	8Fh	DMA Transmit Data Level (IC_DMA_TDLR)—Offset 8Ch	0h
90h	93h	I2C Receive Data Level (IC_DMA_RDLR)—Offset 90h	0h
98h	9Bh	I2C ACK General Call (IC_ACK_GENERAL_CALL)—Offset 98h	1h
9Ch	9Fh	I2C Enable Status (IC_ENABLE_STATUS)—Offset 9Ch	0h
A0h	A3h	I2C SS and FS Spike Suppression Limit (IC_FS_SPKLEN)—Offset A0h	7h
A8h	ABh	Clear RESTART_DET Interrupt (IC_CLR_RESTRART_DET)—Offset A8h	0h

16.2.1 I2C Control (IC_CON)—Offset 0h

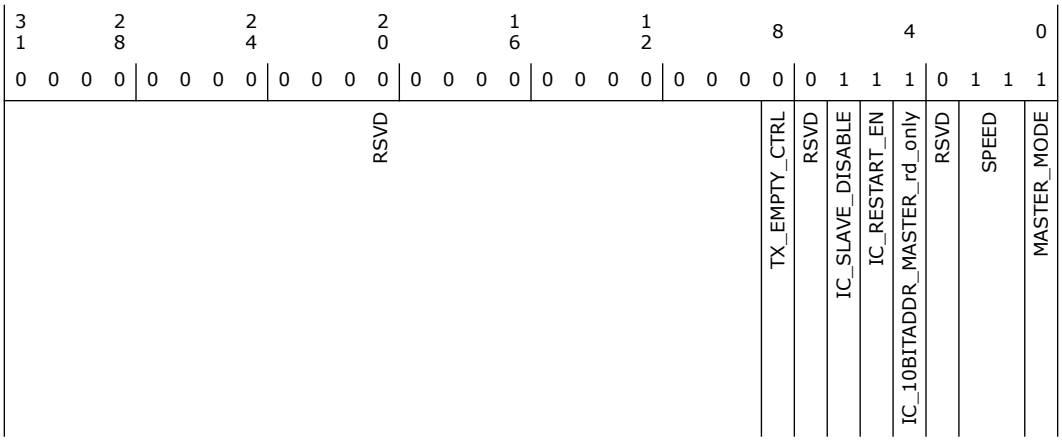
This register can be written only when the I2C is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect

Access Method

Type: MEM Register (Size: 32 bits)

Device: 21
Function: 0

Default: 77h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h RW	**TX_EMPTY_CTRL (TX_EMPTY_CTRL):** This bit controls the generation of the TX_EMPTY interrupt, as described in the IC_RAW_INTR_STAT register.
7	0h RO	Reserved.
6	1h RW	**IC_SLAVE_DISABLE (IC_SLAVE_DISABLE):** This bit controls whether I2C has its slave disabled. If this bit is set (slave is disabled), the function only works as a master and does not perform any action that requires a slave. 0:Reserved 1: slave is disabled NOTE: For Master Device Configuration Software must ensure that this bit is set to 1, and bit 0 must also be set to 1. Else this will result in configuration error
5	1h RO	**IC_RESTART_EN (IC_RESTART_EN):** Determines whether RESTART conditions may be sent when I2C is acting as a master. 0: Restart disable 1: Restart enable When the RESTART is disabled, the IP is incapable of performing the following functions: • Sending a START BYTE • Performing any high-speed mode operation • Performing direction changes in combined format mode • Performing a read operation with a 10-bit address By replacing RESTART condition followed by a STOP and a subsequent START condition, split operations are broken down into multiple transfers. If the above operations are performed, it will result in setting bit 6 (TX_ABRT) of the IC_RAW_INTR_STAT register.
4	1h RO	**IC_10BITADDR_MASTER (IC_10BITADDR_MASTER_rd_only):** Identifies if I2C operates in 7 or 10 bit addressing. 0: 7-bit addressing 1: 10-bit addressing
3	0h RO	Reserved.
2:1	3h RW	**SPEED (SPEED):** These bits control at which speed the I2C operates. 01: standard mode (0 to 100 kbit/s) 10: fast mode (400 kbit/s) Others: reserved
0	1h RW	**MASTER_MODE (MASTER_MODE):** This bit controls whether I2C master is enabled. 0 = Reserved 1 = Master Enabled Note: For Master Device Configuration Software must ensure that this bit is set to 1, and bit 6 must also be set to 1. Else this will result in configuration error.

16.2.2 I2C Target Address (IC_TAR)—Offset 4h

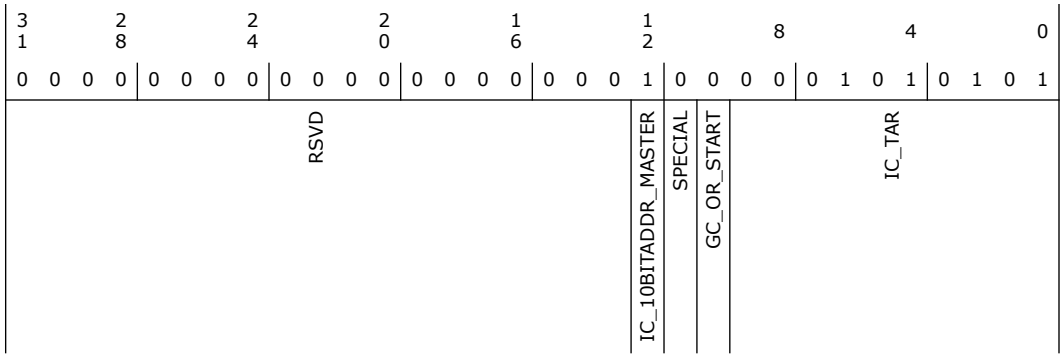
The register should only be updated when the I2C is not enabled (IC_ENABLE=0) or No Master mode operations are active (IC_STATUS[5] = 0 and IC_CON[0] = 1 and IC_STATUS[2] = 1).

Access Method

Type: MEM Register (Size: 32 bits)

Device: 21
Function: 0

Default: 1055h



Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	Reserved.
12	1h RW	**IC_10BITADDR_MASTER (IC_10BITADDR_MASTER):** This bit controls whether the I2C starts its transfers in 7-or 10-bit addressing mode when acting as a master. 0: 7 bit addressing 1: 10-bit addressing
11	0h RW	**SPECIAL (SPECIAL):** This bit indicates whether software performs a General Call or START BYTE command. 0: ignore bit 10 GC_OR_START and use IC_TAR normally. 1: perform special I2C command as specified in GC_OR_START bit
10	0h RW	**GC_OR_START (GC_OR_START):** If bit 11 (SPECIAL) is set to 1, then this bit indicates whether a General Call or START byte command is to be performed by the I2C. 0: General Call Address – after issuing a General Call, only writes may be performed. Attempting to issue a read command results in setting bit 6 (TX_ABRT) of the IC_RAW_INTR_STAT register. The I2C remains in General Call mode until the SPECIAL bit value (bit 11) is cleared. 1: START BYTE
9:0	55h RW	**IC_TAR (IC_TAR):** This is the target address for any master transaction. When transmitting a General Call, these bits are ignored. To generate a START BYTE, the CPU needs to write only once into these bits. Note: If the IC_TAR and IC_SAR are the same, loopback exists but the FIFOs are shared between master and slave, so full loopback is not feasible. Only one direction loopback mode is supported (simplex), not duplex. A master cannot transmit to itself; it can transmit to only a slave.

16.2.3 I2C High Speed Master Mode Code Address (IC_HS_MADDR)—Offset Ch

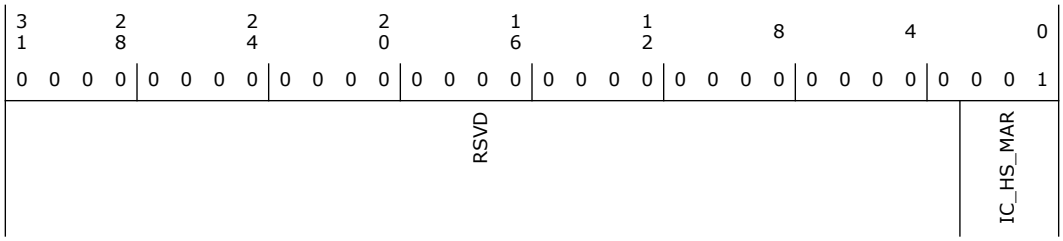
I2C High Speed Master Mode Code Address Register. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect

Access Method

Type: MEM Register (Size: 32 bits)

Device: 21
Function: 0

Default: 1h



Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	Reserved.
2:0	1h RW	**IC_HS_MAR (IC_HS_MAR):** This bit field holds the value of the I2C HS mode master code. HS-mode master codes are reserved 8-bit codes (00001xxx) that are not used for slave addressing or other purposes. Each master has its unique master code; up to eight highspeed mode masters can be present on the same I2C bus system. Valid values are from 0 to 7. This register goes away and becomes read-only returning 0s if the IC_MAX_SPEED_MODE configuration parameter is set to either Standard (1) or Fast (2).

16.2.4 I2C Rx/Tx Data Buffer and Command (IC_DATA_CMD)—Offset 10h

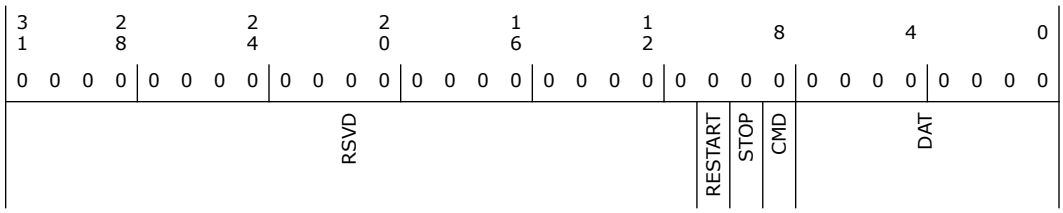
This register is used by the processor to write to when filling the Tx FIFO and to read from when retrieving bytes form Tx FIFO. In order for the I2C controller to continue acknowledging reads, a read command should be written for every byte that is to be received; otherwise, the controller will stop acknowledging.

Access Method

Type: MEM Register (Size: 32 bits)

Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:11	0h RO	Reserved.
10	0h RW	**RESTART (RESTART):** This bit controls whether a RESTART is issued before the byte is sent or received. 1: a RESTART is issued before the data is sent/received (according to the value of CMD), regardless of whether or not the transfer direction is changing from the previous command. 0: a RESTART is issued only if the transfer direction is changing from the previous command
9	0h RW	**STOP (STOP):** This bit controls whether a STOP is issued after the byte is sent or received. 1: STOP is issued after this byte, regardless of whether or not the Tx FIFO is empty. If the Tx FIFO is not empty, the master immediately tries to start a new transfer by issuing a START and arbitrating for the bus. 0: STOP is not issued after this byte, regardless of whether or not the Tx FIFO is empty. If the Tx FIFO is not empty, the master continues the current transfer by sending/receiving data bytes according to the value of the CMD bit. If the Tx FIFO is empty, the master holds the SCL line low and stalls the bus until a new command is available in the Tx FIFO.
8	0h RW	**CMD (CMD):** This bit controls whether a read or a write is performed. 1 = Read. 0 = Write When programming this bit, note the following: attempting to perform a read operation after a General Call command has been sent results in a TX_ABRT interrupt (bit 6 of the IC_RAW_INTR_STAT register), unless bit 11 (SPECIAL) in the IC_TAR register has been cleared. If a "1" is written to this bit after receiving a RD_REQ interrupt, then a TX_ABRT interrupt occurs.
7:0	0h RW	**DAT (DAT):** This register contains the data to be transmitted or received on the I2C bus. If you are writing to this register and want to perform a read, bits 7:0 (DAT) are ignored by the I2C. However, when you read this register, these bits return the value of data received on the I2C interface.

16.2.5 Standard Speed I2C Clock SCL High Count (IC_SS_SCL_HCNT)—Offset 14h

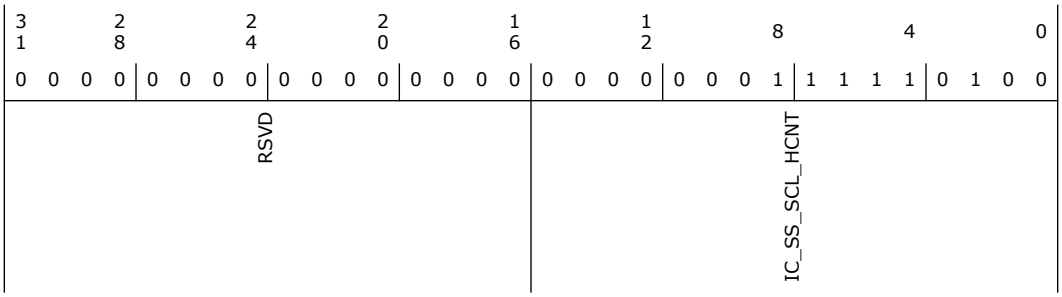
This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 1F4h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	1F4h RW	**IC_SS_SCL_HCNT (IC_SS_SCL_HCNT):** This register sets the SCL clock high-period count for standard speed. The value of the registers should be within the range {6, 65525}

16.2.6 Standard Speed I2C Clock SCL Low Count (IC_SS_SCL_LCNT)—Offset 18h

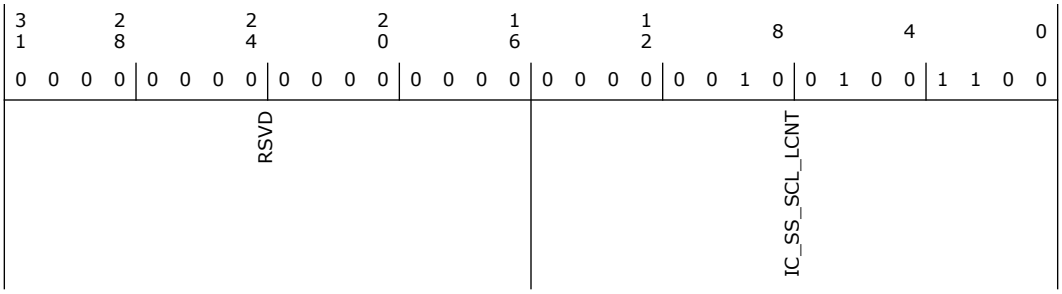
This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

Access Method

Type: MEM Register (Size: 32 bits)

Device: 21
Function: 0

Default: 24Ch



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	24Ch RW	**IC_SS_SCL_LCNT (IC_SS_SCL_LCNT):** Standard Speed I2C Clock SCL Low Count Register. The register value should always be >= 8

16.2.7 Fast Speed I2C Clock SCL High Count (IC_FS_SCL_HCNT)—Offset 1Ch

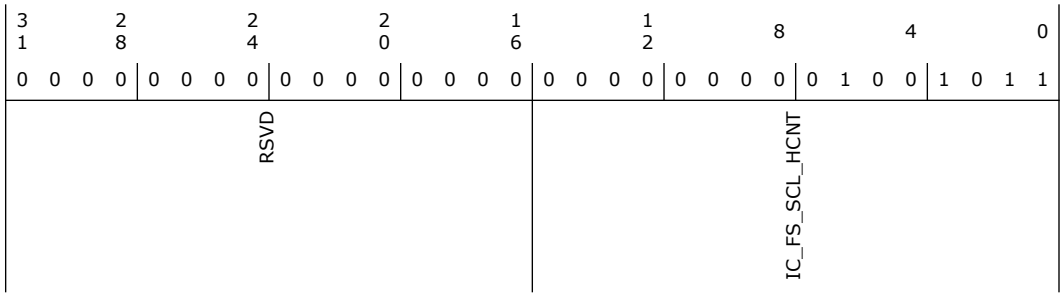
This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

Access Method

Type: MEM Register (Size: 32 bits)

Device: 21
Function: 0

Default: 4Bh



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	4Bh RW	**IC_FS_SCL_HCNT (IC_FS_SCL_HCNT):** This register sets the SCL clock high-period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. The minimum value of this field is 6.

16.2.8 Fast Speed I2C Clock SCL Low Count (IC_FS_SCL_LCNT)—Offset 20h

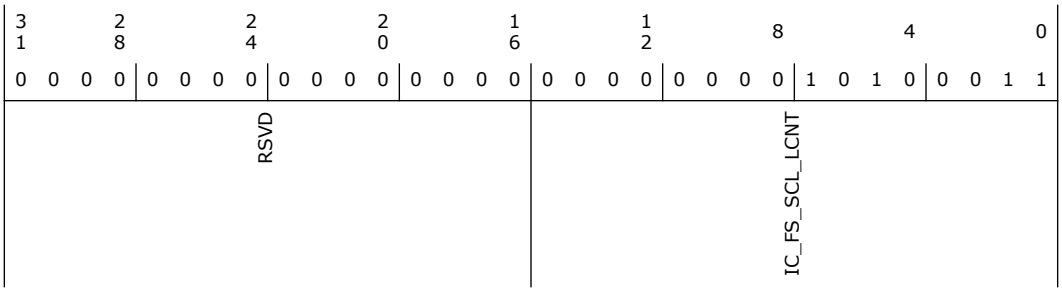
This register must be set before any I2C bus transaction can take place to ensure proper I/O timing.

Access Method

Type: MEM Register (Size: 32 bits)

Device: 21
Function: 0

Default: A3h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	A3h RW	**IC_FS_SCL_LCNT (IC_FS_SCL_LCNT):** This register sets the SCL clock low period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. The register should be programmed with a minimum value of 8.

16.2.9 I2C Interrupt Status (IC_INTR_STAT)—Offset 2Ch

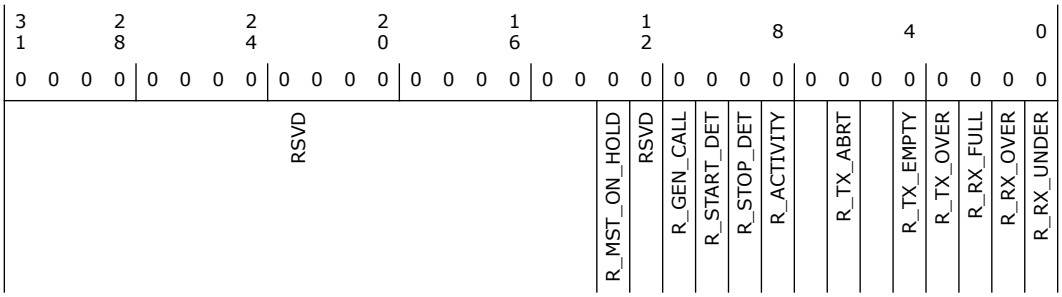
Each bit in this register has a corresponding mask bit in the IC_INTR_MASK register. These bits are cleared by reading the matching interrupt clear register

Access Method

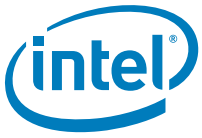
Type: MEM Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13	0h RO	**R_MST_ON_HOLD (R_MST_ON_HOLD):** Indicates whether a master is holding the bus and the TX FIFO is empty. Enabled only when I2C_DYNAMIC_TAR_UPDATE = 1 and IC_EMPTYFIFO_HOLD_MASTER_EN = 1
12	0h RO	Reserved.
11	0h RO	**R_GEN_CALL (R_GEN_CALL):** Set only when a General Call address is received and it is acknowledged. It stays set until it is cleared either by disabling the controller or when the processor reads bit 0 of the IC_CLR_GEN_CALL register



Bit Range	Default & Access	Field Name (ID): Description
10	0h RO	**R_START_DET (R_START_DET):** Indicates whether a START or RESTART condition has occurred on the I2C interface
9	0h RO	**R_STOP_DET (R_STOP_DET):** Indicates whether a STOP condition has occurred on the I2C interface.
8	0h RO	**R_ACTIVITY (R_ACTIVITY):** This bit captures the controller activity and stays set until it is cleared. There are four ways to clear it: 1. Disabling the controller, 2. Reading the IC_CLR_ACTIVITY register, 3. Reading the IC_CLR_INTR register, 4. System reset Note: Once this bit is set, it stays set unless one of the four methods is used to clear it. Even if the controller is idle, this bit remains set until cleared, indicating that there was activity on the bus.
7	0h RO	**Reserved**
6	0h RO	**R_TX_ABRT (R_TX_ABRT):** This bit indicates if the controler, as an I2C transmitter, is unable to complete the intended actions on the contents of the transmit FIFO. When this bit is set to 1, the IC_TX_ABRT_SOURCE register indicates the reason why the transmit abort takes places. NOTE: The controller flushes/resets/empties the TX FIFO whenever this bit is set. The TX FIFO remains in this flushed state until the register IC_CLR_TX_ABRT is read. Once this read is performed, the TX FIFO is then ready to accept more data bytes.
5	0h RO	**Reserved**
4	0h RO	**R_TX_EMPTY (R_TX_EMPTY):** The behavior of the TX_EMPTY interrupt status differs based on the TX_EMPTY_CTRL selection in the IC_CON register. - When TX_EMPTY_CTRL = 0: This bit is set to 1 when the transmit buffer is at or below the threshold value set in the IC_TX_TL register. - When TX_EMPTY_CTRL = 1: This bit is set to 1 when the transmit buffer is at or below the threshold value set in the IC_TX_TL register and the transmission of the address/data from the internal shift register for the most recently popped command is completed. It is automatically cleared by hardware when the buffer level goes above the threshold. When IC_ENABLE[0] is set to 0, the TX FIFO is flushed and held in reset. Then the TX FIFO looks like it has no data within it, so this bit is set to 1, provided there is activity in the master or slave state machines. When there is no longer any activity, then with ic_en=0, this bit is set to 0.
3	0h RO	**R_TX_OVER (R_TX_OVER):** Set during transmit if the transmit buffer is filled to IC_TX_BUFFER_DEPTH and the processor attempts to issue another I2C command by writing to the IC_DATA_CMD register.
2	0h RO	**R_RX_FULL (R_RX_FULL):** Set when the receive buffer reaches or goes above the RX_TL threshold in the IC_RX_TL register. It is automatically cleared by hardware when buffer level goes below the threshold. NOTE: If IC_RX_FULL_HLD_BUS_EN=1, then the RX_OVER interrupt is never set to 1, because the criteria to set this interrupt are never met.
1	0h	**R_RX_OVER (R_RX_OVER):** Set if the receive buffer is completely filled to IC_RX_BUFFER_DEPTH and an additional byte is received from an external I2C device. The controller acknowledges this, but any data bytes received after the FIFO is full are lost.
0	0h RO	**R_RX_UNDER (R_RX_UNDER):** Set if the processor attempts to read the receive buffer when it is empty by reading from the IC_DATA_CMD register.

16.2.10 I2C Interrupt Mask (IC_INTR_MASK)—Offset 30h

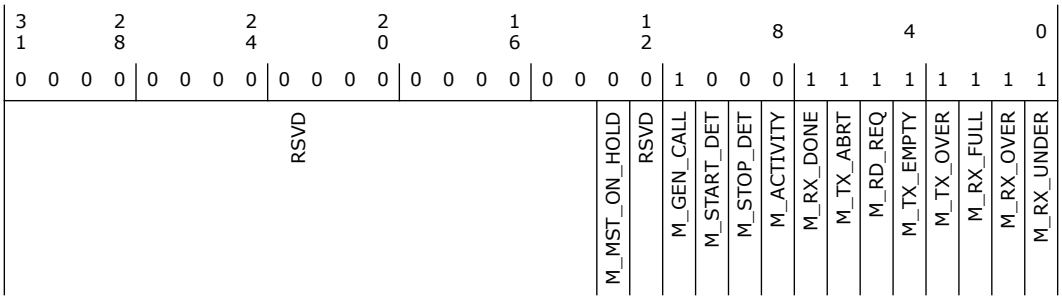
I2C Interrupt Mask Register. These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register

Access Method

Type: MEM Register (Size: 32 bits)

Device: 21
Function: 0

Default: 8FFh



Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13	0h RW	**M_MST_ON_HOLD (M_MST_ON_HOLD)**
12	0h RO	Reserved.
11	1h RW	**M_GEN_CALL (M_GEN_CALL)**
10	0h RW	**M_START_DET (M_START_DET)**
9	0h RW	**M_STOP_DET (M_STOP_DET)**
8	0h RW	**M_ACTIVITY (M_ACTIVITY)**
7	1h RW	**M_RX_DONE (M_RX_DONE)**
6	1h RW	**M_TX_ABRT (M_TX_ABRT)**
5	1h RW	**M_RD_REQ (M_RD_REQ)**
4	1h RW	**M_TX_EMPTY (M_TX_EMPTY)**
3	1h RW	**M_TX_OVER (M_TX_OVER)**
2	1h RW	**M_RX_FULL (M_RX_FULL)**
1	1h RW	**M_RX_OVER (M_RX_OVER)**
0	1h RW	**M_RX_UNDER (M_RX_UNDER)**

16.2.11 I2C Raw Interrupt Status (IC_RAW_INTR_STAT)—Offset 34h

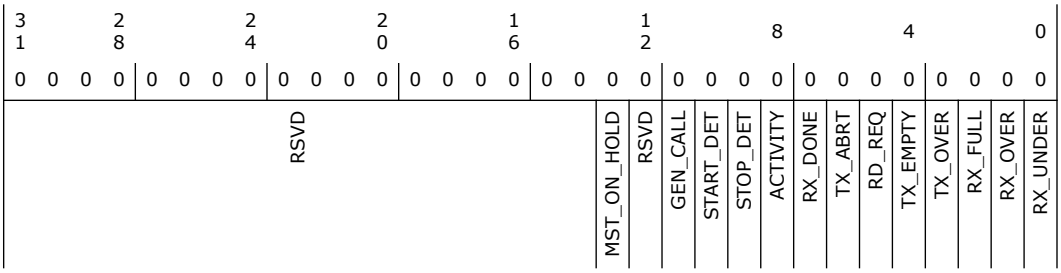
Unlike the IC_INTR_STAT register, these bits are not masked so they always show the true status of the controller

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13	0h RO	**MST_ON_HOLD (MST_ON_HOLD):** Same as in IC_INTR_STAT.
12	0h RO	Reserved.
11	0h RO	**GEN_CALL (GEN_CALL):** Same as in IC_INTR_STAT.
10	0h RO	**START_DET (START_DET):** Same as in IC_INTR_STAT.
9	0h RO	**STOP_DET (STOP_DET):** Same as in IC_INTR_STAT.
8	0h RO	**ACTIVITY (ACTIVITY):** Same as in IC_INTR_STAT.
7	0h RO	**RX_DONE (RX_DONE):** Same as in IC_INTR_STAT.
6	0h RO	**TX_ABRT (TX_ABRT):** Same as in IC_INTR_STAT.
5	0h RO	**RD_REQ (RD_REQ):** Same as in IC_INTR_STAT.
4	0h RO	**TX_EMPTY (TX_EMPTY):** Same as in IC_INTR_STAT.
3	0h RO	**TX_OVER (TX_OVER):** Same as in IC_INTR_STAT.
2	0h RO	**RX_FULL (RX_FULL):** Same as in IC_INTR_STAT.
1	0h RO	**RX_OVER (RX_OVER):** Same as in IC_INTR_STAT.
0	0h RO	**RX_UNDER (RX_UNDER):** Same as in IC_INTR_STAT.

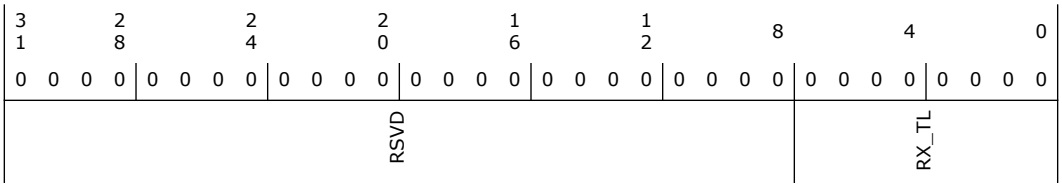
16.2.12 I2C Receive FIFO Threshold (IC_RX_TL)—Offset 38h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	0h RW	**RX_TL (RX_TL):** Receive FIFO Threshold Level. Controls the level of entries (or above) that triggers the RX_FULL interrupt (bit 2 in IC_RAW_INTR_STAT register). The valid range is 0-0x3F. (Values > 0x3F are set to depth of the buffer). A value of 0 sets the threshold for 1 entry, and a value of 63 sets the threshold for 64 entries. WARNING: When operating with DMA, the Watermark for I2C RX fifo must be programmed to be equal to M-Size (burst size) of the DMA; Any other programming value will put controller at risk of a deadlock.

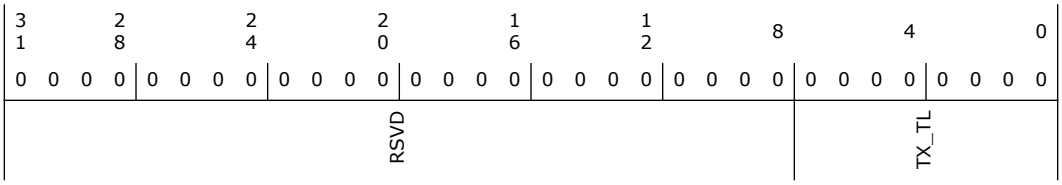
16.2.13 I2C Transmit FIFO Threshold (IC_TX_TL)—Offset 3Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	0h RW	**TX_TL (TX_TL):** Controls the level of entries (or below) that trigger the TX_EMPTY interrupt (bit 4 in IC_RAW_INTR_STAT register). The valid range is 0-0x3F, (Values > 0x3F are set to depth of the buffer). A value of 0 sets the threshold for 1 entry, and a value of 63 sets the threshold for 64 entries.

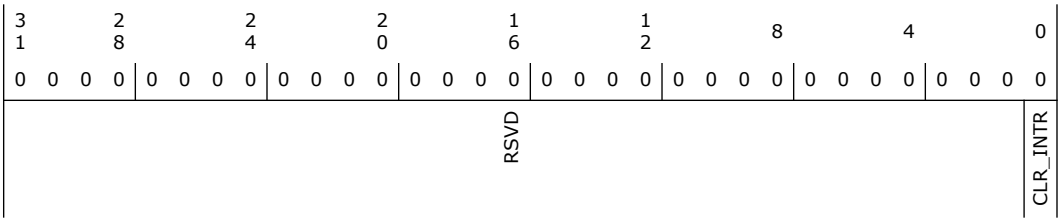
16.2.14 Clear Combined and Individual Interrupt (IC_CLR_INTR)—Offset 40h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RO	**CLR_INTR (CLR_INTR):** Read this register to clear the combined interrupt, all individual interrupts, and the IC_TX_ABRT_SOURCE register. This bit does not clear hardware clearable interrupts but software clearable interrupts. Refer to Bit 9 of the IC_TX_ABRT_SOURCE register for an exception to clearing IC_TX_ABRT_SOURCE.

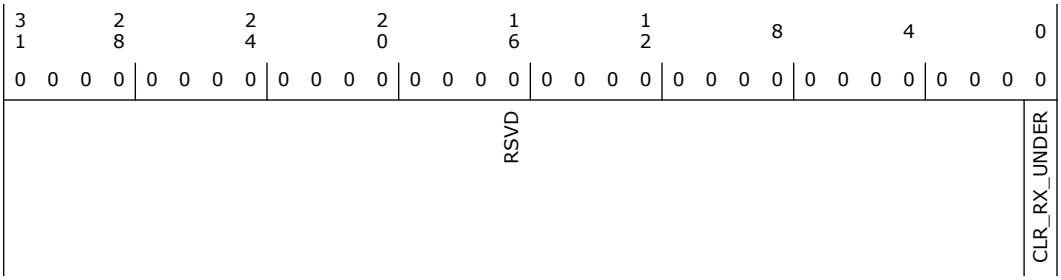
16.2.15 Clear RX_UNDER Interrupt (IC_CLR_RX_UNDER)—Offset 44h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RO	**CLR_RX_UNDER (CLR_RX_UNDER):** Read this register to clear the RX_UNDER interrupt (bit 0) of the IC_RAW_INTR_STAT register.

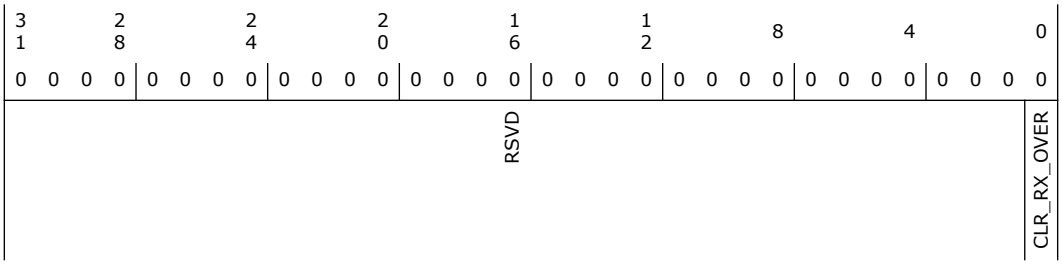
16.2.16 Clear RX_OVER Interrupt (IC_CLR_RX_OVER)—Offset 48h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RO	**CLR_RX_OVER (CLR_RX_OVER):** Read this register to clear the RX_OVER interrupt (bit 1) of the IC_RAW_INTR_STAT register.

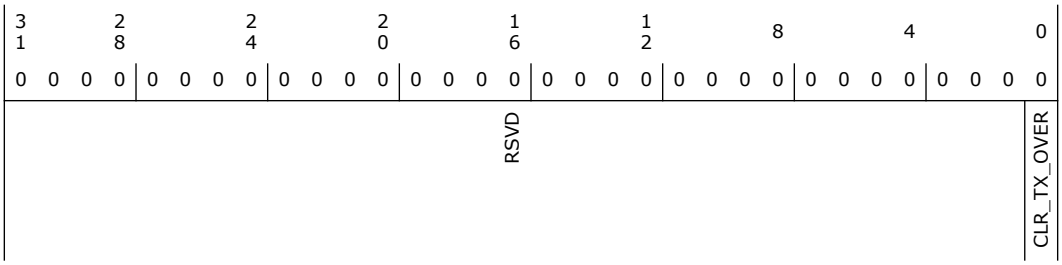
16.2.17 Clear TX_OVER Interrupt (IC_CLR_TX_OVER)—Offset 4Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RO	**CLR_TX_OVER (CLR_TX_OVER):** Read this register to clear the TX_OVER interrupt (bit 3) of the IC_RAW_INTR_STAT register.

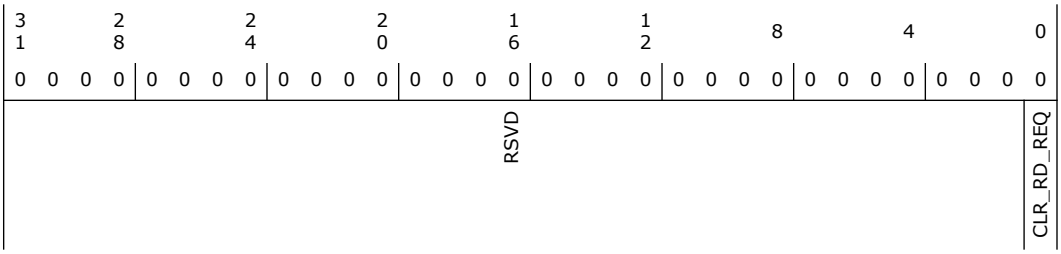
16.2.18 Clear RD_REQ Interrupt (IC_CLR_RD_REQ)—Offset 50h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RO	**CLR_RD_REQ (CLR_RD_REQ):** Read this register to clear the RD_REQ interrupt (bit 5) of the IC_RAW_INTR_STAT register.

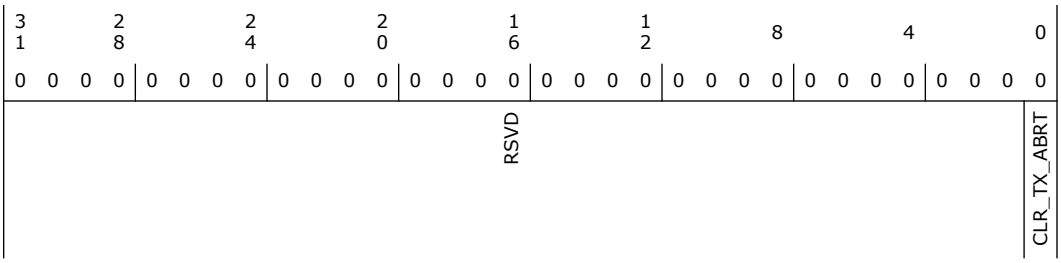
16.2.19 Clear TX_ABRT Interrupt (IC_CLR_TX_ABRT)—Offset 54h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RO	**CLR_TX_ABRT (CLR_TX_ABRT):** Read this register to clear the TX_ABRT interrupt (bit 6) of the IC_RAW_INTR_STAT register, and the IC_TX_ABRT_SOURCE register. This also releases the TX FIFO from the flushed/reset state, allowing more writes to the TX FIFO. Refer to Bit 9 of the IC_TX_ABRT_SOURCE register for an exception to clearing IC_TX_ABRT_SOURCE

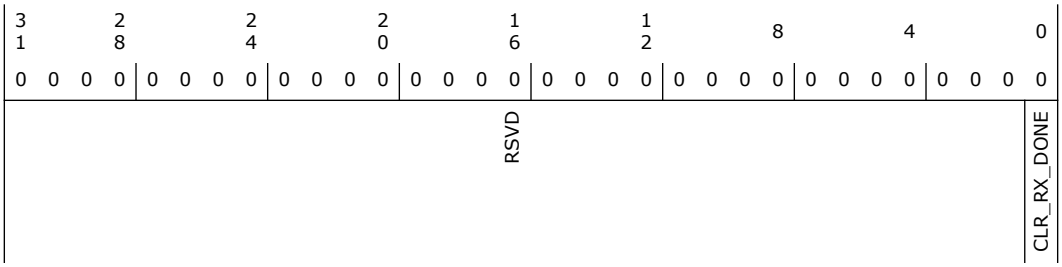
16.2.20 Clear RX_DONE Interrupt (IC_CLR_RX_DONE)—Offset 58h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RO	**CLR_RX_DONE (CLR_RX_DONE):** Read this register to clear the RX_DONE interrupt (bit 7) of the IC_RAW_INTR_STAT register.

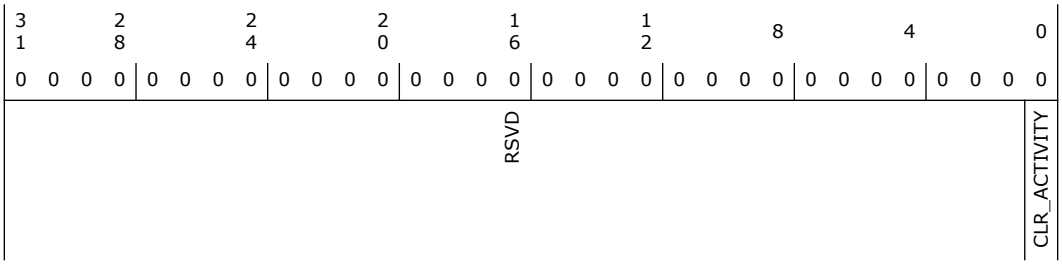
16.2.21 Clear ACTIVITY Interrupt (IC_CLR_ACTIVITY)—Offset 5Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RO	**CLR_ACTIVITY (CLR_ACTIVITY):** Reading this register clears the ACTIVITY interrupt if the I2C is not active anymore. If the I2C module is still active on the bus, the ACTIVITY interrupt bit continues to be set. It is automatically cleared by hardware if the module is disabled and if there is no further activity on the bus. The value read from this register to get status of the ACTIVITY interrupt (bit 8) of the IC_RAW_INTR_STAT register.

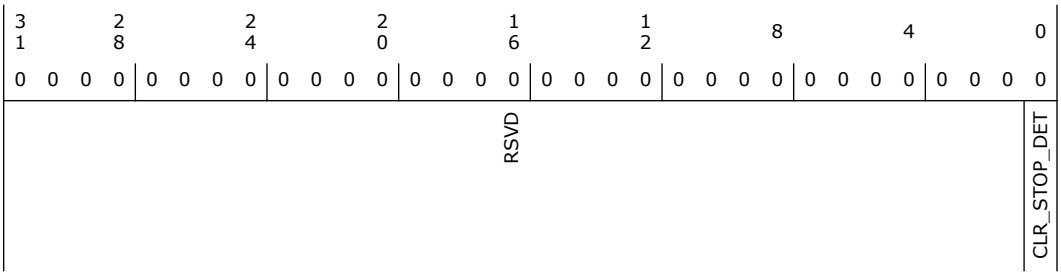
16.2.22 Clear STOP_DET Interrupt (IC_CLR_STOP_DET)—Offset 60h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RO	**CLR_STOP_DET (CLR_STOP_DET):** Read this register to clear the STOP_DET interrupt (bit 9) of the IC_RAW_INTR_STAT register.

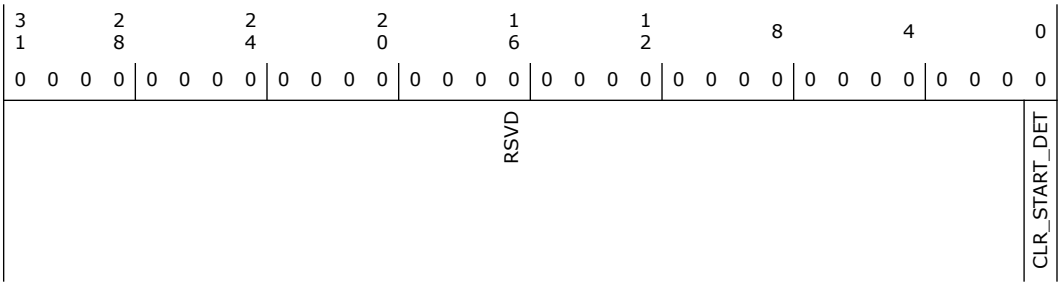
16.2.23 Clear START_DET Interrupt (IC_CLR_START_DET)—Offset 64h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RO	**CLR_START_DET (CLR_START_DET):** Read this register to clear the START_DET interrupt (bit 10) of the IC_RAW_INTR_STAT register.

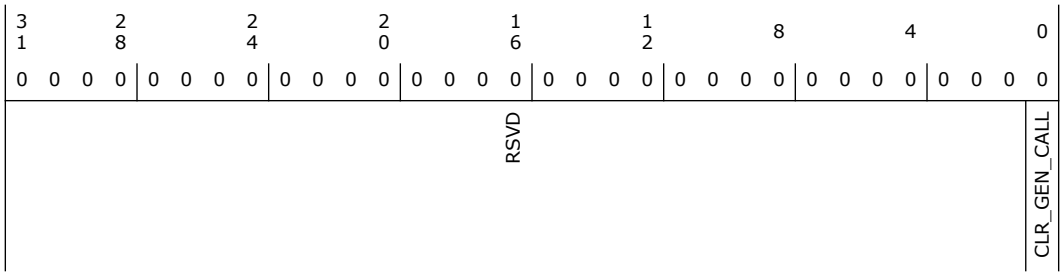
16.2.24 Clear GEN_CALL Interrupt (IC_CLR_GEN_CALL)—Offset 68h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RO	**CLR_GEN_CALL (CLR_GEN_CALL):** Read this register to clear the GEN_CALL interrupt (bit 11) of IC_RAW_INTR_STAT register.

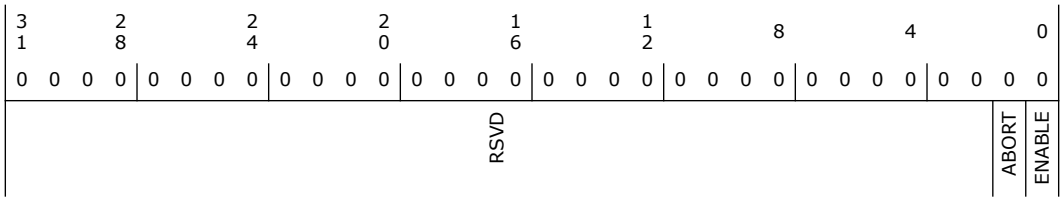
16.2.25 I2C Enable (IC_ENABLE)—Offset 6Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1	0h	**ABORT (ABORT):** Sofware can abort I2C transfer by setting this bit. Hw will clear this ABORT bit once the STOP has been detected
0	0h RW	**ENABLE (ENABLE):** Controls whether the controller is enabled. 0: Disables I2C controller(TX and RX FIFOs are held in an erased state) 1: Enables I2C controller. Software can disable the controller while it is active. However, it is important that care be taken to ensure that the controller is disabled properly. When the controller is disabled, the following occurs: -The TX FIFO and RX FIFO get flushed. -Status bits in the IC_INTR_STAT register are still active until the controller goes into IDLE state. If the module is transmitting, it stops as well as deletes the contents of the transmit buffer after the current transfer is complete. If the module is receiving, the controller stops the current transfer at the end of the current byte and does not acknowledge the transfer.

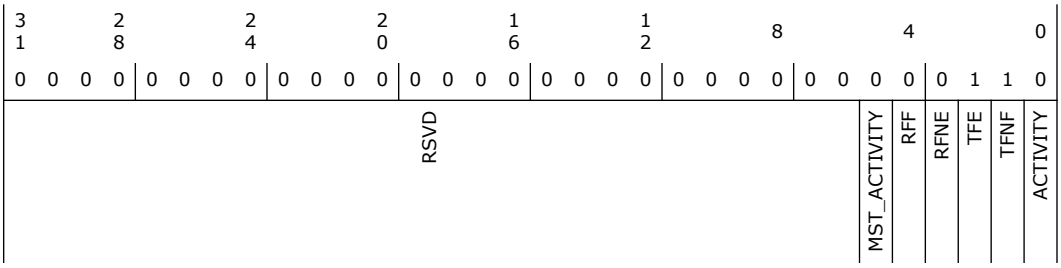
16.2.26 I2C Status (IC_STATUS)—Offset 70h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 6h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	Reserved.
5	0h RO	**Master Activity Status (MST_ACTIVITY):** When the Master state machine is not in the IDLE state, this bit is set. 0: Master is in IDLE state 1: Master is not in IDLE
4	0h RO	**Receive FIFO Completely Full (RFF):** When the receive FIFO is completely full, this bit is set. When the receive FIFO contains one or more empty location, this bit is cleared. 0: Receive FIFO is not full 1: Receive FIFO is full
3	0h RO	**Receive FIFO Not Empty (RFNE):** This bit is set when the receive FIFO contains one or more entries; it is cleared when the receive FIFO is empty. 0: Receive FIFO is empty 1: Receive FIFO is not empty

Bit Range	Default & Access	Field Name (ID): Description
2	1h RO	**Transmit FIFO Completely Empty (TFE):** When the transmit FIFO is completely empty, this bit is set. When it contains one or more valid entries, this bit is cleared. This bit field does not request an interrupt. 0: Transmit FIFO is not empty 1: Transmit FIFO is empty
1	1h RO	**Transmit FIFO Not Full (TFNF):** Set when the transmit FIFO contains one or more empty locations, and is cleared when the FIFO is full. 0: Transmit FIFO is full 1: Transmit FIFO is not full
0	0h RO	**ACTIVITY (ACTIVITY):** I2C Activity Status

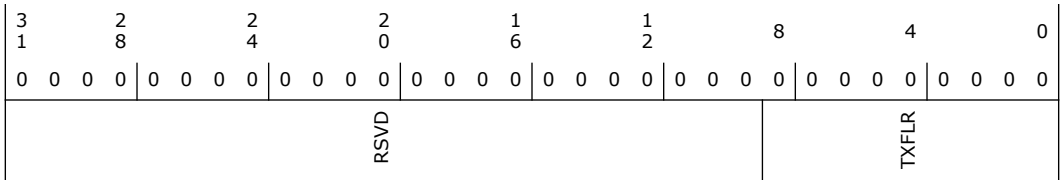
16.2.27 I2C Transmit FIFO Level (IC_TXFLR)—Offset 74h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8:0	0h RO	**Transmit FIFO Level (TXFLR):** Contains the number of valid data entries in the transmit FIFO.

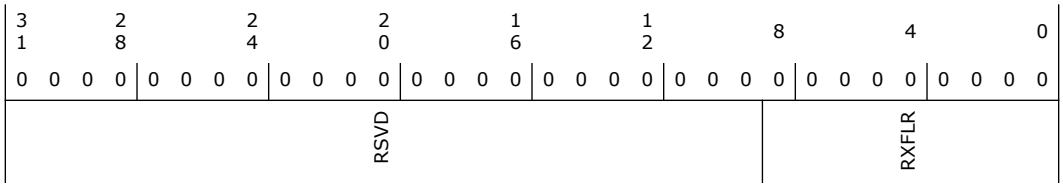
16.2.28 I2C Receive FIFO Level (IC_RXFLR)—Offset 78h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8:0	0h RO	**Receive FIFO Level (RXFLR):** Receive FIFO Level. Contains the number of valid data entries in the receive FIFO.

16.2.29 I2C SDA Hold Time Length (IC_SDA_HOLD)—Offset 7Ch

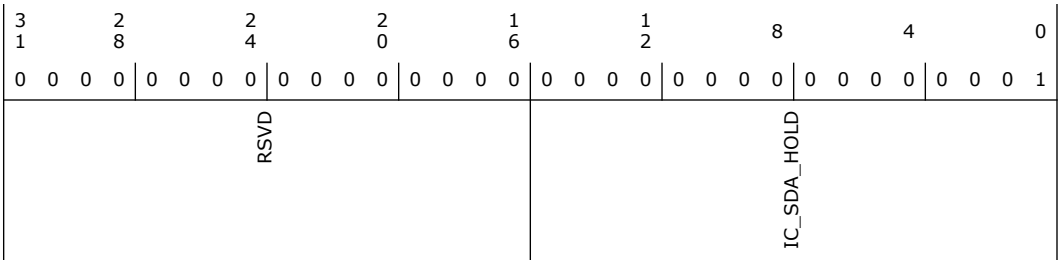
This register controls the amount of hold time on the SDA signal after a negative edge of SCL, in units of 10 MHz.
The value programmed must be greater than the minimum hold time in each mode for the value to be implemented—one cycle in master mode.
Writes to this register succeed only when IC_ENABLE=0.
The programmed SDA hold time cannot exceed at any time the duration of the low part of SCL. Therefore, the programmed value cannot be larger than N_SCL_LOW-2, where N_SCL_LOW is the duration of the low part of the SCL period measured in ic_clk cycles (10 MHz).

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 1h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	1h RW	**IC_SDA_HOLD (IC_SDA_HOLD):** Sets the required SDA hold time in units of ic_clk period.

16.2.30 I2C Transmit Abort Source (IC_TX_ABRT_SOURCE)—Offset 80h

This register has 32 bits that indicate the source of the TX_ABRT bit. Except for Bit 9, this register is cleared whenever the IC_CLR_TX_ABRT register or the IC_CLR_INTR register is read. To clear Bit 9, the source of the ABRT_SBYTE_NORSTRT must be fixed first; RESTART must be enabled (IC_CON[5]=1), the SPECIAL bit must be cleared (IC_TAR[11]), or the GC_OR_START bit must be cleared (IC_TAR[10]).
Once the source of the ABRT_SBYTE_NORSTRT is fixed, then this bit can be cleared in

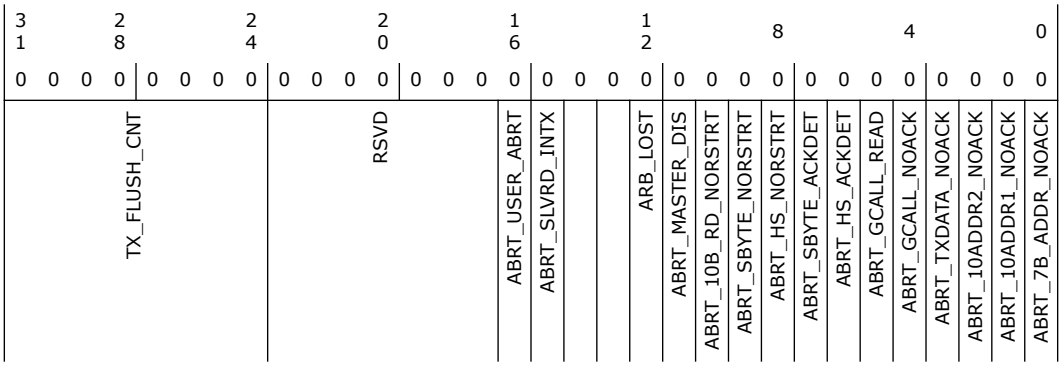
the same manner as other bits in this register. If the source of the ABRT_SBYTE_NORSTRT is not fixed before attempting to clear this bit, Bit 9 clears for one cycle and is then re-asserted.

Access Method

Type: MEM Register (Size: 32 bits)

Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**TX_FLUSH_CNT (TX_FLUSH_CNT):** This field preserves the TXFLR value prior to the last TX_ABRT event. It is cleared whenever I2C is disabled.
23:17	0h RO	Reserved.
16	0h RO	**ABRT_USER_ABRT (ABRT_USER_ABRT):** Master has detected the user initiated transfer abort (IC_ENABLE[1])
15	0h RO	**ABRT_SLVRD_INTX (ABRT_SLVRD_INTX)**
14	0h RO	**Reserved**
13	0h RO	**Reserved**
12	0h RO	**ARB_LOST (ARB_LOST):** 1: Master has lost arbitration, or if IC_TX_ABRT_SOURCE[14] is also set, then the slave transmitter has lost arbitration.
11	0h RO	**ABRT_MASTER_DIS (ABRT_MASTER_DIS):** 1: User tries to initiate a Master operation with the Master mode disabled.
10	0h RO	**ABRT_10B_RD_NORSTRT (ABRT_10B_RD_NORSTRT):** 1: The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the master sends a read command in 10-bit addressing mode.
9	0h RO	**ABRT_SBYTE_NORSTRT (ABRT_SBYTE_NORSTRT):** 1: The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the user is trying to send a START Byte. To clear Bit 9, the source of the ABRT_SBYTE_NORSTRT must be fixed first; restart must be enabled (IC_CON[5]=1), the SPECIAL bit must be cleared (IC_TAR[11]), or the GC_OR_START bit must be cleared (IC_TAR[10]). Once the source of the ABRT_SBYTE_NORSTRT is fixed, then this bit can be cleared in the same manner as other bits in this register. If the source of the ABRT_SBYTE_NORSTRT is not fixed before attempting to clear this bit, bit 9 clears for one cycle and then gets re-asserted.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RO	**ABRT_HS_NORSTRT (ABRT_HS_NORSTRT):** 1: The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the user is trying to use the master to transfer data in High Speed mode.
7	0h RO	**ABRT_SBYTE_ACKDET (ABRT_SBYTE_ACKDET):** 1: Master has sent a START Byte and the START Byte was acknowledged (wrong behavior).
6	0h RO	**ABRT_HS_ACKDET (ABRT_HS_ACKDET):** 1: Master is in High Speed mode and the High Speed Master code was acknowledged (wrong behavior).
5	0h RO	**ABRT_GCALL_READ (ABRT_GCALL_READ):** 1: Controller in master mode sent a General Call but the user programmed the byte following the General Call to be a read from the bus (IC_DATA_CMD[9] is set to 1).
4	0h RO	**ABRT_GCALL_NOACK (ABRT_GCALL_NOACK):** 1: controller in master mode sent a General Call and no slave on the bus acknowledged the General Call.
3	0h RO	**ABRT_TXDATA_NOACK (ABRT_TXDATA_NOACK):** 1: This is a master-mode only bit. Master has received an acknowledgement for the address, but when it sent data byte(s) following the address, it did not receive an acknowledge from the remote slave(s).
2	0h RO	**ABRT_10ADDR2_NOACK (ABRT_10ADDR2_NOACK):** 1: Master is in 10-bit address mode and the second address byte of the 10-bit address was not acknowledged by any slave.
1	0h RO	**ABRT_10ADDR1_NOACK (ABRT_10ADDR1_NOACK):** 1: Master is in 10-bit address mode and the first 10-bit address byte was not acknowledged by any slave.
0	0h RO	**ABRT_7B_ADDR_NOACK (ABRT_7B_ADDR_NOACK):** 1: Master is in 7-bit addressing mode and the address sent was not acknowledged by any slave.

16.2.31 DMA Control (IC_DMA_CR)—Offset 88h

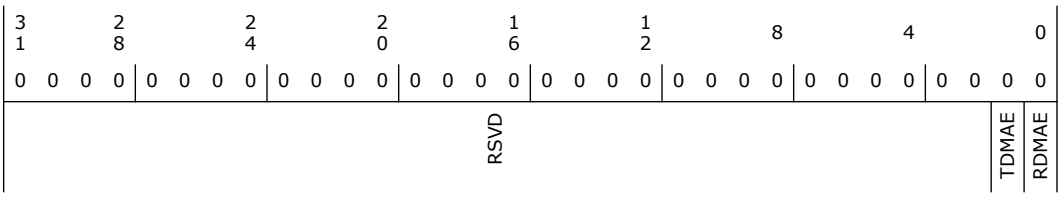
This register is only valid when the controller is configured with a set of DMA Controller interface signals (IC_HAS_DMA = 1).
When the controller is not configured for DMA operation, this register does not exist and writing to the register's address has no effect and reading from this register address will return zero.
The register is used to enable the DMA Controller interface operation. There is a separate bit for transmit and receive. This can be programmed regardless of the state of IC_ENABLE.

Access Method

Type: MEM Register (Size: 32 bits)

Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1	0h RW	**Transmit DMA Enable (TDMAE):** This bit enables/disables the transmit FIFO DMA channel. 0 = Transmit DMA disabled 1 = Transmit DMA enabled
0	0h RW	**Receive DMA Enable (RDMAE):** This bit enables/disables the receive FIFO DMA channel. 0 = Receive DMA disabled 1 = Receive DMA enabled

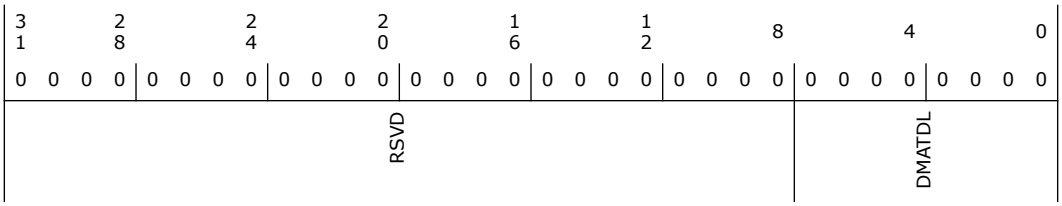
16.2.32 DMA Transmit Data Level (IC_DMA_TDLR)—Offset 8Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	0h RW	**Transmit Data Level (DMATDL):** This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the transmit FIFO is equal to or below this field value, and TDMAE = 1.

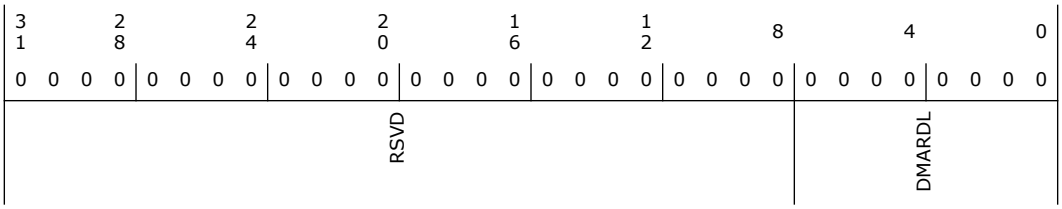
16.2.33 I2C Receive Data Level (IC_DMA_RDLR)—Offset 90h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	0h RW	**DMARDL (DMARDL):** This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or more than this field value + 1, and RDMAE =1. For instance, when DMARDL is 0, then dma_rx_req is asserted when 1 or more data entries are present in the receive FIFO.

16.2.34 I2C ACK General Call (IC_ACK_GENERAL_CALL)—Offset 98h

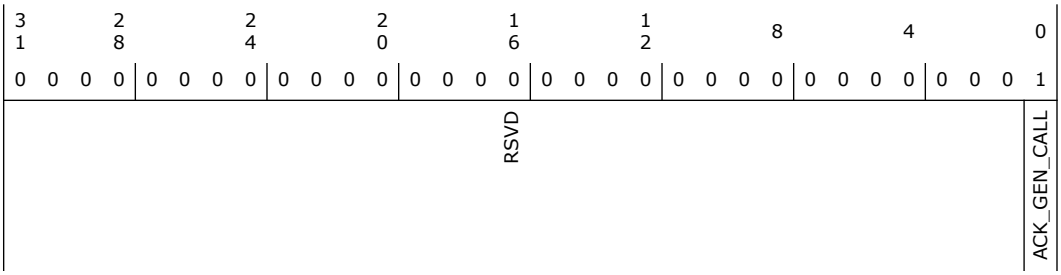
The register controls whether the controller responds with a ACK or NACK when it receives an I2C General Call address.

Access Method

Type: MEM Register (Size: 32 bits)

Device: 21
Function: 0

Default: 1h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	1h RW	**ACK_GEN_CALL (ACK_GEN_CALL):** When set to 1, the controller responds with a ACK when it receives a General Call. When set to 0, the controller does not generate General Call interrupts

16.2.35 I2C Enable Status (IC_ENABLE_STATUS)—Offset 9Ch

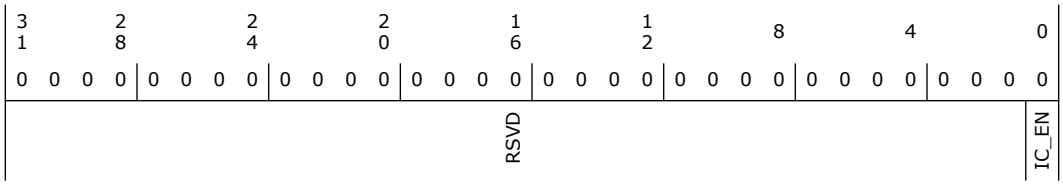
The register is used to report the hardware status when the IC_ENABLE register is set from 1 to 0; that is, when the controller is disabled.
If IC_ENABLE has been set to 1, bits 2:1 are forced to 0, and bit 0 is forced to 1.
If IC_ENABLE has been set to 0, bits 2:1 is only be valid as soon as bit 0 is read as '0'.
When IC_ENABLE has been written with '0,' a delay occurs for bit 0 to be read as '0' because disabling the controller depends on I2C bus activities.

Access Method

Type: MEM Register (Size: 32 bits)

Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RO	**I2C Enable Status (IC_EN):** When read as 1, the controller is deemed to be in an enabled state. When read as 0, the controller is deemed completely inactive.

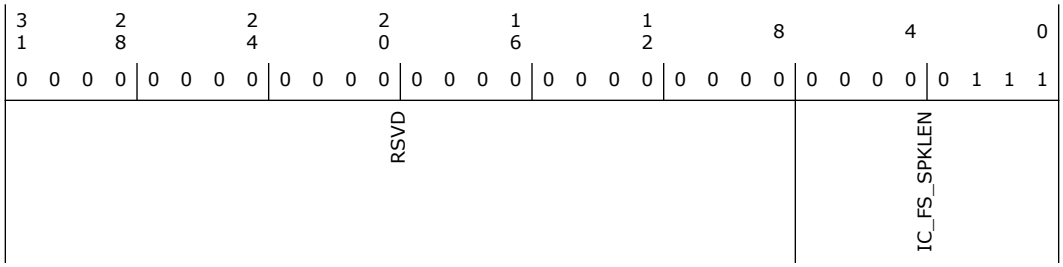
16.2.36 I2C SS and FS Spike Suppression Limit (IC_FS_SPKLEN)—Offset A0h

This register is used to store the duration, measured in ic_clk cycles, of the longest spike that is filtered out by the spike suppression logic when the component is operating in SS or FS modes.
The relevant I2C requirement is tSP as detailed in the I2C Bus Specification. This register must be programmed with a minimum value of 1.

Access Method

Type: MEM Register (Size: 32 bits)
Device: 21
Function: 0

Default: 7h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	7h RW	**IC_FS_SPKLEN (IC_FS_SPKLEN):** This register must be set before any I2C bus transaction can take place to ensure stable operation. This register sets the duration, measured in ic_clk cycles, of the longest spike in the SCL or SDA lines that are filtered out by the spike suppression logic. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 1; hardware prevents values less than this being written, and if attempted results in 2 being set.

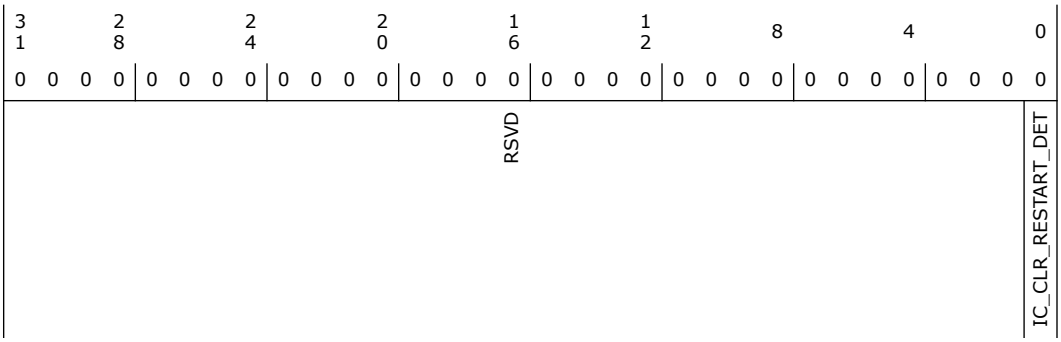
16.2.37 Clear RESTART_DET Interrupt (IC_CLR_RESTRART_DET)—Offset A8h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RO	**IC_CLR_RESTART_DET (IC_CLR_RESTART_DET):** Read this register to clear the RESTART_DET interrupt (bit 12) of the IC_RAW_INTR_STAT register. This register is present only when IC_SLV_RESTART_DET_EN = 1.

16.3 I²C Additional Registers Summary

The registers in this section are memory-mapped registers based on the BAR defined in PCH Configuration space.

Table 16-3. Summary of I²C Additional Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
204h	207h	Soft Reset (RESETS)—Offset 204h	0h
210h	213h	Active LTR (ACTIVELTR_VALUE)—Offset 210h	800h
214h	217h	Idle LTR (IDLELTR_VALUE)—Offset 214h	800h
218h	21Bh	TX Ack Count (TX_ACK_COUNT)—Offset 218h	0h
21Ch	21Fh	RX ACK Count (RX_BYTE_COUNT)—Offset 21Ch	0h
220h	223h	Interrupt Status for Tx Complete (TX_COMPLETE_INTR_STAT)—Offset 220h	0h
224h	227h	Tx Complete Interrupt Clear (TX_COMPLETE_INTR_CLR)—Offset 224h	0h
228h	22Bh	SW Scratch Register 0 (SW_SCRATCH_0)—Offset 228h	0h
22Ch	22Fh	SW Scratch Register 1 (SW_SCRATCH_1)—Offset 22Ch	0h
230h	233h	SW Scratch Register 2 (SW_SCRATCH_2)—Offset 230h	0h

Table 16-3. Summary of I²C Additional Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
234h	237h	SW Scratch Register 3 (SW_SCRATCH_3)—Offset 234h	0h
238h	23Bh	Clock Gate (CLOCK_GATE)—Offset 238h	0h
240h	243h	Remap Address Low (REMAP_ADDR_LO)—Offset 240h	0h
244h	247h	Remap Address High (REMAP_ADDR_HI)—Offset 244h	0h
24Ch	24Fh	Device Control (DEVIDLE_CONTROL)—Offset 24Ch	8h
2FCh	2FFh	Capabilities (CAPABLITIES)—Offset 2FCh	0h

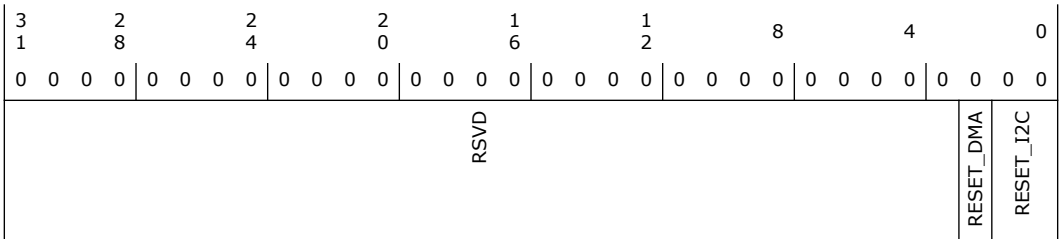
16.3.1 Soft Reset (RESETS)—Offset 204h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	Reserved.
2	0h RW	**DMA Software Reset Control (RESET_DMA):** DMA Software Reset Control 0 – DMA is in reset (Reset Asserted) 1 – DMA is NOT at reset (Reset Released)
1:0	0h RW	**I2C Host Controller Reset (RESET_I2C):** Used to reset the I2C Host Controller by SW control. All I2C Configuration State and Operational State will be forced to the Default state. There is no timing requirement (SW can assert and de-assert in back to back transactions). This reset does NOT impact the I2C level settings by BIOS, the PCI configuration header information, DMA channel configuration and interrupt assignment/mapping/ etc. Driver should re-initialize registers related to Driver context following an I2C host controller reset. 00 = I2C Host Controller is in reset (Reset Asserted) 01 = Reserved 10 = Reserved 11 = I2C Host Controller is NOT at reset (Reset Released)

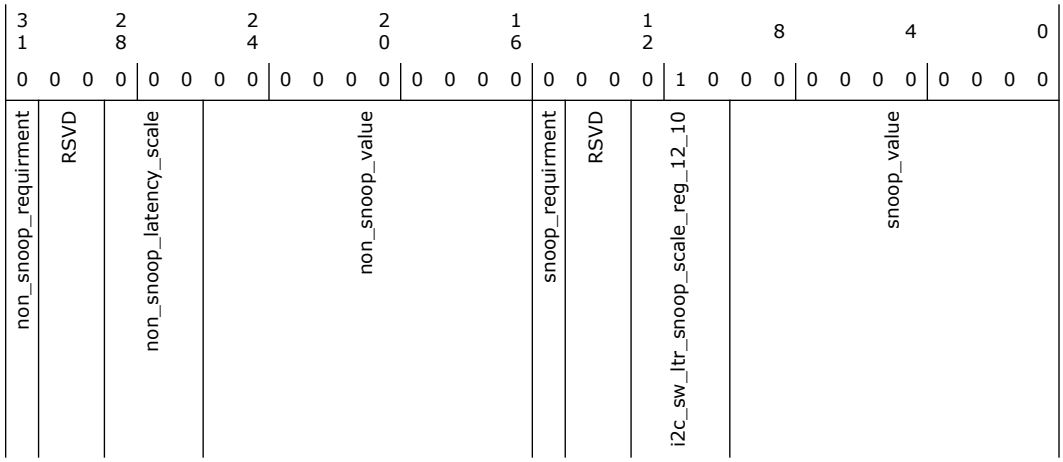
16.3.2 Active LTR (ACTIVELTR_VALUE)—Offset 210h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 800h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Non-Snoop Requirement (non_snoop_requirment):** If the Requirement (bit 15) is clear, that indicates that the device has no LTR requirement for this type of traffic (i.e. it can wait for service indefinitely). If the 10-bit latency value is zero it indicates that the device cannot tolerate any delay and needs the best possible service/ response time.
30:29	0h RO	Reserved.
28:26	0h RO	**Non-Snoop Latency Scale (non_snoop_latency_scale):** Support for codes 010 (1us) or 011 (32us) for Snoop Latency Scale (1us -> 32ms total span) only. Writes to this CSR which don't match those values will be dropped completely, next read will return previous value.
25:16	0h RO	**Non-Snoop Value (non_snoop_value):** 10-bit latency value
15	0h RW	**Snoop Requirement (snoop_requirment):** If the Requirement (bit 15) is clear, that indicates that the device has no LTR requirement for this type of traffic (i.e. it can wait for service indefinitely). If the 10-bit latency value is zero it indicates that the device cannot tolerate any delay and needs the best possible service/response time.
14:13	0h RO	Reserved.
12:10	2h	**Snoop Latency Scale (i2c_sw_ltr_snoop_scale_reg_12_10):** Support for codes 010 (1us) or 011 (32us) for Snoop Latency Scale(1us -> 32ms total span) only. Writes to this CSR which don't match those values will be dropped completely, next read will return previous value.
9:0	0h RW	**Snoop Value (snoop_value):** 10-bit latency value

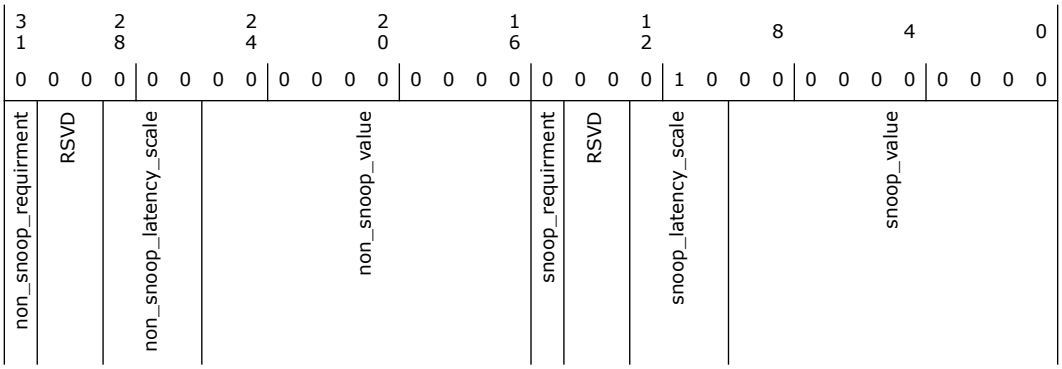
16.3.3 Idle LTR (IDLELTR_VALUE)—Offset 214h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 800h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Non-Snoop Requirement (non_snoop_requirment):** If the Requirement (bit 15) is clear, that indicates that the device has no LTR requirement for this type of traffic (i.e. it can wait for service indefinitely). If the 10-bit latency value is zero it indicates that the device cannot tolerate any delay and needs the best possible service/ response time.
30:29	0h RO	Reserved.
28:26	0h RO	**Non-Snoop Latency Scale (non_snoop_latency_scale):** Support for codes 010 (1us) or 011 (32us) for Snoop Latency Scale (1us -> 32ms total span) only. Writes to this CSR which don't match those values will be dropped completely, next read will return previous value.
25:16	0h RO	**Non-Snoop Value (non_snoop_value):** 10-bit latency value
15	0h RW	**Snoop Requirement (snoop_requirment):** If the Requirement (bit 15) is clear, that indicates that the device has no LTR requirement for this type of traffic (i.e. it can wait for service indefinitely). If the 10-bit latency value is zero it indicates that the device cannot tolerate any delay and needs the best possible service/response time.
14:13	0h RO	Reserved.
12:10	2h RW	**Snoop_latency_scale (snoop_latency_scale):** Support for codes 010 (1us) or 011 (32us) for Snoop Latency Scale(1us -> 32ms total span) only. Writes to this CSR which don't match those values will be dropped completely, next read will return previous value.
9:0	0h RW	**Snoop Value (snoop_value):** 10-bit latency value

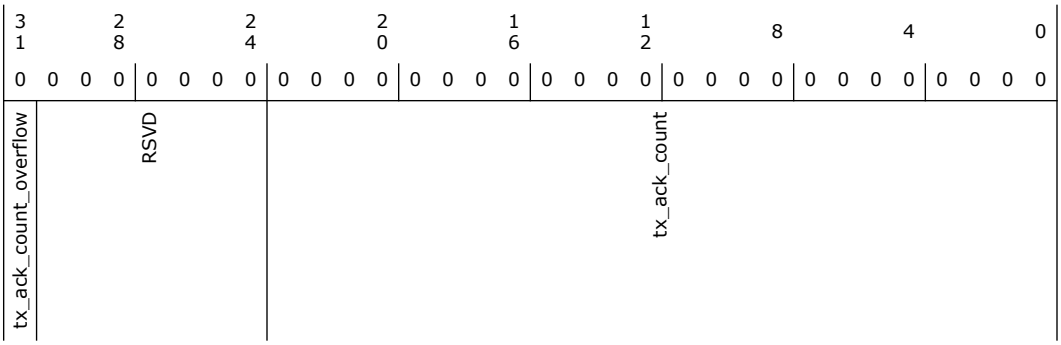
16.3.4 TX Ack Count (TX_ACK_COUNT)—Offset 218h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Tx Count Overflow (tx_ack_count_overflow):** Tx_count_overflow 0= count valid 1= count overflow/invalid
30:24	0h RO	Reserved.
23:0	0h RO	**TX Ack Count (tx_ack_count):** 24-bit up-counter which counts the number of TX ACKs on the I2C bus. The Counter is forced to be cleared by software Read.

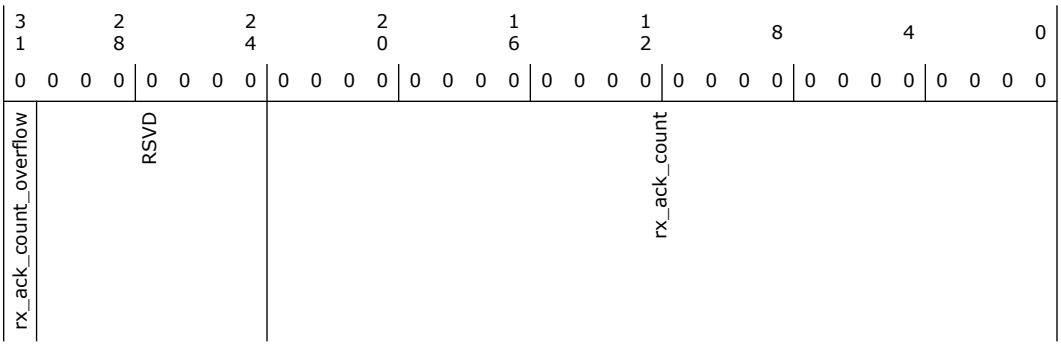
16.3.5 RX ACK Count (RX_BYTE_COUNT)—Offset 21Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**RX ACK Count Overflow (rx_ack_count_overflow):** Rx ACK count_overflow 0= count valid 1= count overflow/invalid
30:24	0h RO	Reserved.
23:0	0h RO	**Rx ACK Count (rx_ack_count):** 24-bit readable (MMIO) up-counter which counts the number of RX bytes received on the I2C bus. The Counter is forced to be cleared by software Read

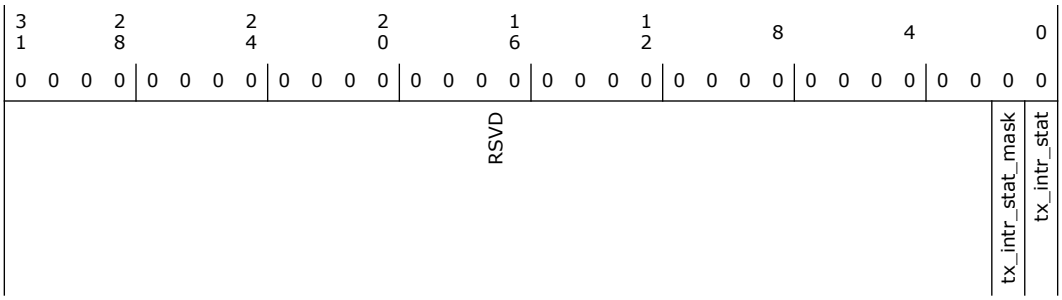
16.3.6 Interrupt Status for Tx Complete (TX_COMPLETE_INTR_STAT)—Offset 220h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1	0h RW	**TX completion interrupt Mask (tx_intr_stat_mask):** 0 = Unmask 1= Mask
0	0h RO	**Tx Completion Interrupt (tx_intr_stat):** 0 = Low 1 = High

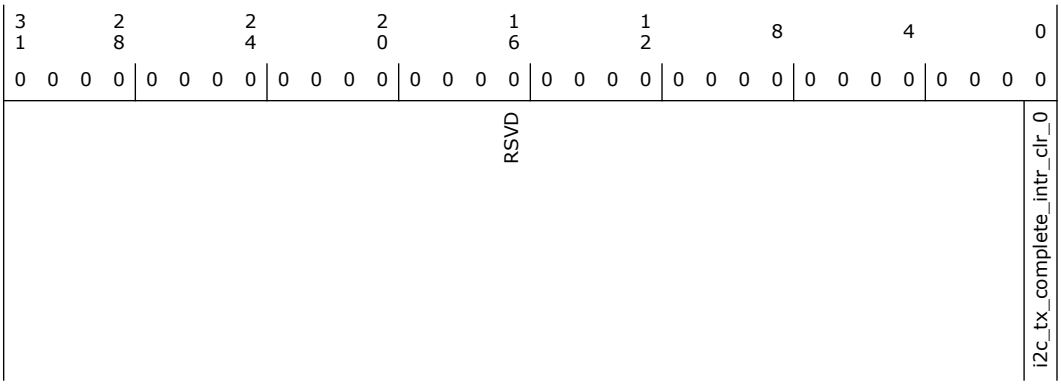
16.3.7 Tx Complete Interrupt Clear (TX_COMPLETE_INTR_CLR)—Offset 224h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RO	**TX completion interrupt Clear (i2c_tx_complete_intr_clr_0):** Read this register to clear the TX_COMPLETE_INTR_STAT register

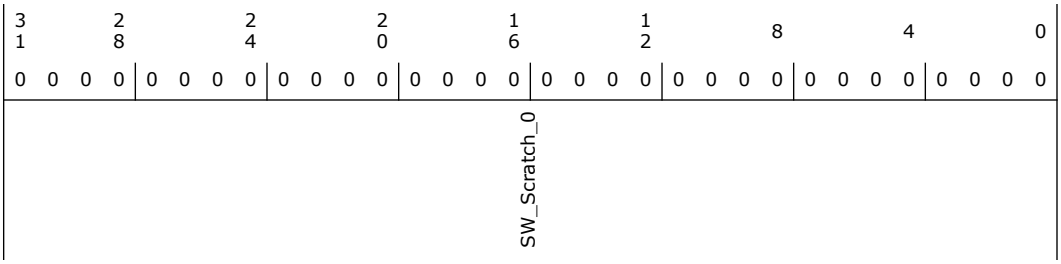
16.3.8 SW Scratch Register 0 (SW_SCRATCH_0)—Offset 228h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**SW Scratch Reg 0 (SW_Scratch_0):** Scratch Pad Register for SW to generated Local CMD or DATA for DMA

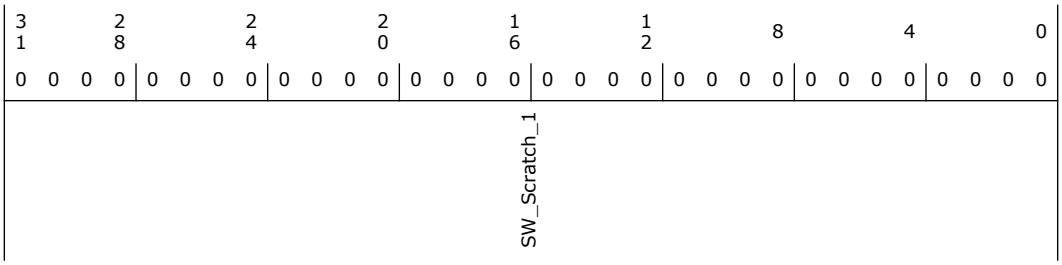
16.3.9 SW Scratch Register 1 (SW_SCRATCH_1)—Offset 22Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**SW Scratch Register 1 (SW_Scratch_1):** Scratch Pad Register for SW to generated Local CMD or DATA for DMA.

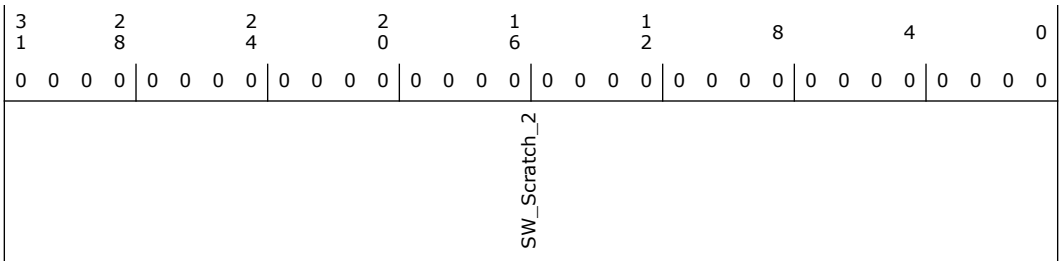
16.3.10 SW Scratch Register 2 (SW_SCRATCH_2)—Offset 230h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**SW Scratch Register 2 (SW_Scratch_2):** Scratch Pad Register for SW to generated Local CMD or DATA for DMA

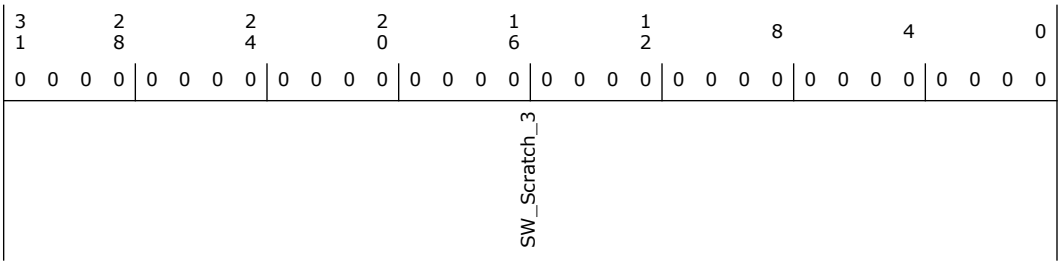
16.3.11 SW Scratch Register 3 (SW_SCRATCH_3)—Offset 234h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**SW Scratch Register 3 (SW_Scratch_3):** Scratch Pad Register for SW to generated Local CMD or DATA for DMA

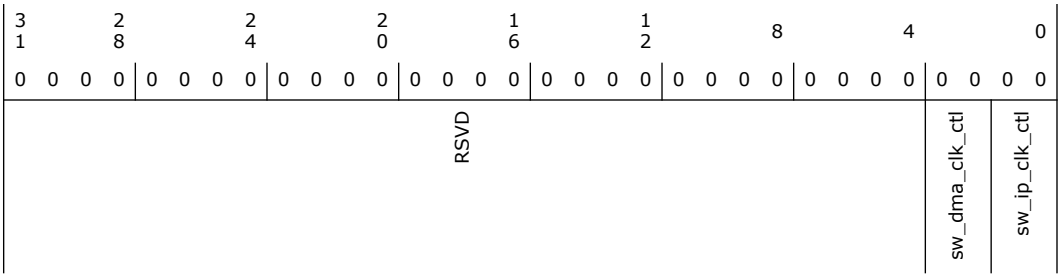
16.3.12 Clock Gate (CLOCK_GATE)—Offset 238h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3:2	0h RW	**DMA Clock Control (sw_dma_clk_ctl):** 00 = Dyanamic Clock Gate Enable 01 = Reserved 10 = Force DMA Clock off 11 = Force DMA Clock on
1:0	0h RW	**Controller Clock Control (sw_ip_clk_ctl):** 00 = Dynamic Clock Gate Enable 01 = Reserved 10 = Force Clocks off 11 = Force Clocks on

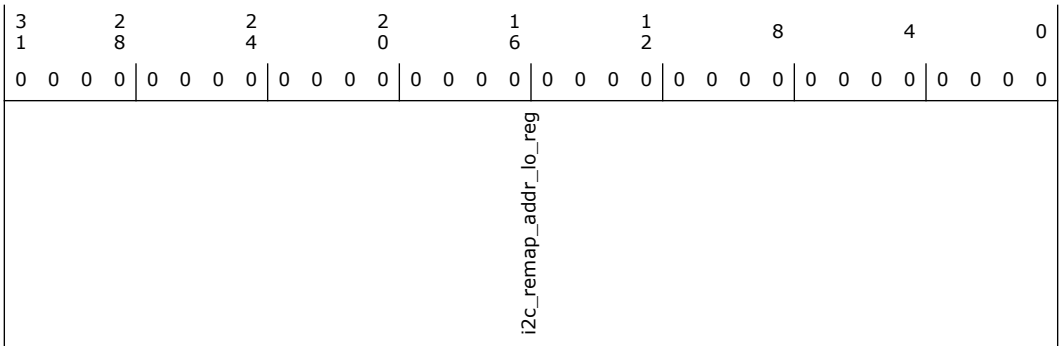
16.3.13 Remap Address Low (REMAP_ADDR_LO)—Offset 240h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Remap Address Low (i2c_remap_addr_lo_reg):** Must be programmed to the same value as low 32 bits (0x 010 BAR Low) Note: Must be programed for all I2C controllers configurations (DMA or PIO only)

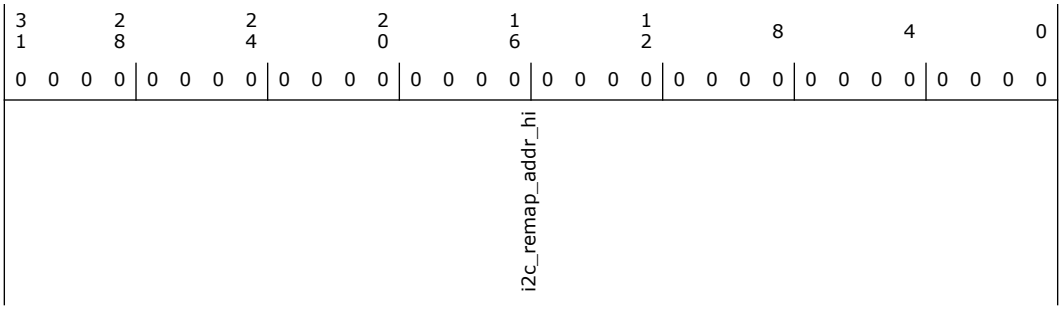
16.3.14 Remap Address High (REMAP_ADDR_HI)—Offset 244h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Remap Address High (i2c_remap_addr_hi):** Must be programmed to the same value as low 32 bits (0x 014 BAR High)

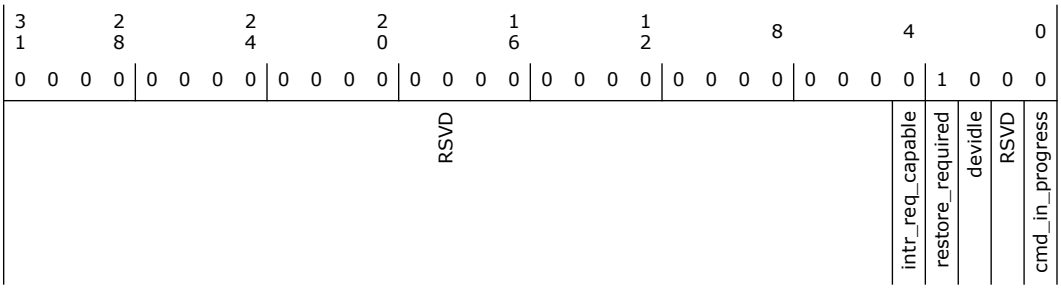
16.3.15 Device Control (DEVIDLE_CONTROL)—Offset 24Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 8h



Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4	0h RO	**Interrupt Request Capable (intr_req_capable):** Set to '1' by HW if it is capable of generating an interrupt on command completion, else '0'.
3	1h RW1C	**Restore Require (restore_required):** When set (by HW), SW must restore state to the controller. The state may have been lost due to a reset or full power lost. SW clears the bit by writing a '1'. This bit will be set on initial power up.
2	0h RW	**Device Idle (devidle):** SW sets this bit to '1' to move the function into the DevIdle state. Writing this bit to '0' will return the function to the fully active D0 state.
1	0h RO	Reserved.
0	0h RO	**Command In Progress (cmd_in_progress):** HW sets this bit on a 1->0 or 0->1 transition of DEVIDLE. While set, the other bits in this register are not valid and it is illegal for SW to write to any bit in this register. HW clears this bit upon completing the DevIdle transition command. When clear, all the other bits in the register are valid and SW may write to any bit. If Interrupt Request (IR) was set for the current command, HW may clear this bit before the interrupt has been made visible to SW, since when SW actually handles a particular interrupt is not visible to the HW. SW writes to this bit have no effect.

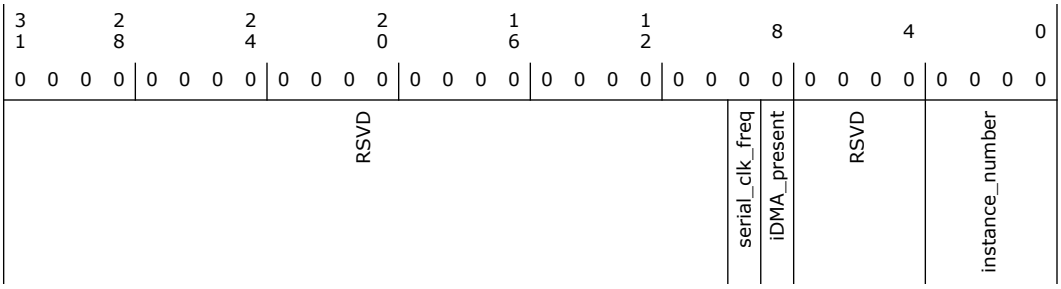
16.3.16 Capabilities (CAPABLITIES)—Offset 2FCh

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9	0h RO	**Serial Clock Frequency (serial_clk_freq):** 0 indicates 120 MHz clock.
8	0h RO	**DMA Present (iDMA_present):** 0= DMA present 1= DMA not present
7:4	0h RO	Reserved.
3:0	0h RO	**Instant Number (instance_number):** 0h: I2C0 1h: I2C1 2h: I2C2 ... 5h: I2C5[br

16.4 I2C DMA Controller Registers Summary

The registers in this section are memory-mapped registers based on the BAR defined in PCH Configuration space.

Table 16-4. Summary of I2C DMA Controller Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
800h	803h	DMA Transfer Source Address Low (SAR_LO0)—Offset 800h	0h
804h	807h	DMA Transfer Source Address High (SAR_HI0)—Offset 804h	0h
808h	80Bh	DMA Transfer Destination Address Low (DAR_LO0)—Offset 808h	0h
80Ch	80Fh	DMA Transfer Destination Address High (DAR_HI0)—Offset 80Ch	0h
810h	813h	Linked List Pointer Low (LLP_LO0)—Offset 810h	0h
814h	817h	Linked List Pointer High (LLP_HI0)—Offset 814h	0h
818h	81Bh	Control Register Low (CTL_LO0)—Offset 818h	0h
81Ch	81Fh	Control Register High (CTL_HI0)—Offset 81Ch	0h
820h	823h	Source Status (SSTAT0)—Offset 820h	0h
828h	82Bh	Destination Status (DSTAT0)—Offset 828h	0h
830h	833h	Source Status Address Low (SSTATAR_LO0)—Offset 830h	0h
834h	837h	Source Status Address High (SSTATAR_HI0)—Offset 834h	0h
838h	83Bh	Destination Status Address Low (DSTATAR_LO0)—Offset 838h	0h
83Ch	83Fh	Destination Status Address High (DSTATAR_HI0)—Offset 83Ch	0h
840h	843h	DMA Transfer Configuration Low (CFG_LO0)—Offset 840h	203h
844h	847h	DMA Transfer Configuration High (CFG_HI0)—Offset 844h	0h
848h	84Bh	Source Gather (SGR0)—Offset 848h	0h
850h	853h	Destination Scatter (DSR0)—Offset 850h	0h
AC0h	AC3h	Raw Interrupt Status (RawTfr)—Offset AC0h	0h
AC8h	ACBh	Raw Status for Block Interrupts (RawBlock)—Offset AC8h	0h
AD0h	AD3h	Raw Status for Source Transaction Interrupts (RawSrcTran)—Offset AD0h	0h

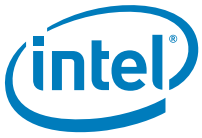


Table 16-4. Summary of I2C DMA Controller Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
AD8h	ADBh	Raw Status for Destination Transaction Interrupts (RawDstTran)—Offset AD8h	0h
AE0h	AE3h	Raw Status for Error Interrupts (RawErr)—Offset AE0h	0h
AE8h	AEBh	Interrupt Status (StatusTfr)—Offset AE8h	0h
AF0h	AF3h	Status for Block Interrupts (StatusBlock)—Offset AF0h	0h
AF8h	AFBh	Status for Source Transaction Interrupts (StatusSrcTran)—Offset AF8h	0h
B00h	B03h	Status for Destination Transaction Interrupts (StatusDstTran)—Offset B00h	0h
B08h	B0Bh	Status for Error Interrupts (StatusErr)—Offset B08h	0h
B10h	B13h	Mask for Transfer Interrupts (MaskTfr)—Offset B10h	0h
B18h	B1Bh	Mask for Block Interrupts (MaskBlock)—Offset B18h	0h
B20h	B23h	Mask for Source Transaction Interrupts (MaskSrcTran)—Offset B20h	0h
B28h	B2Bh	Mask for Destination Transaction Interrupts (MaskDstTran)—Offset B28h	0h
B30h	B33h	Mask for Error Interrupts (MaskErr)—Offset B30h	0h
B38h	B3Bh	Clear for Transfer Interrupts (ClearTfr)—Offset B38h	0h
B40h	B43h	Clear for Block Interrupts (ClearBlock)—Offset B40h	0h
B48h	B4Bh	Clear for Source Transaction Interrupts (ClearSrcTran)—Offset B48h	0h
B50h	B53h	Clear for Destination Transaction Interrupts (ClearDstTran)—Offset B50h	0h
B58h	B5Bh	Clear for Error Interrupts (ClearErr)—Offset B58h	0h
B60h	B63h	Combined Status register (StatusInt)—Offset B60h	0h
B98h	B9Bh	DMA Configuration (DmaCfgReg)—Offset B98h	0h
BA0h	BA3h	DMA Channel Enable (ChEnReg)—Offset BA0h	0h

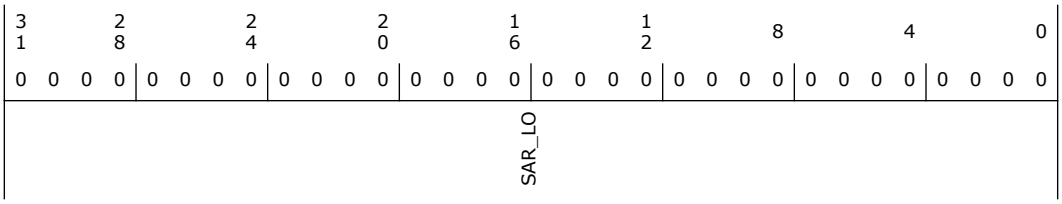
16.4.1 DMA Transfer Source Address Low (SAR_LO0)—Offset 800h

NOTE: SAR_LO0 is for DMA Channel 0. The same register definition,SAR_LO1, is available for Channel 1 at address 858h.
SAR_LO0 (CH0): offset 800h
SAR_LO1 (CH1): offset 858h
The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

Access Method

Type: MEM Register (Size: 32 bits)
Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**SAR_LO:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length > 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported.

16.4.2 DMA Transfer Source Address High (SAR_HI0)—Offset 804h

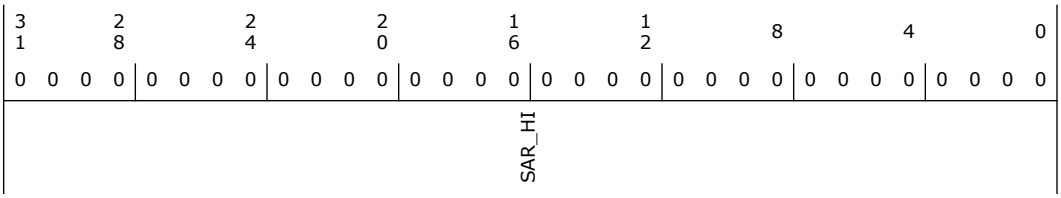
NOTE: SAR_HI0 is for DMA Channel 0. The same register definition, SAR_HI1, is available for Channel 1 at address 85Ch.
SAR_HI0 (CH0): offset 804h
SAR_HI1 (CH1): offset 85Ch
The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**SAR_HI:** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length > 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported.

16.4.3 DMA Transfer Destination Address Low (DAR_LO0)—Offset 808h

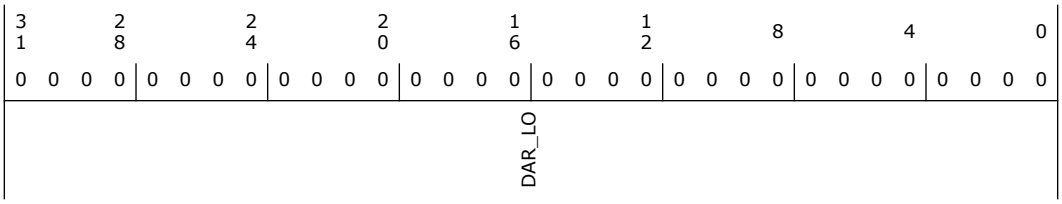
NOTE: DAR_LO0 is for DMA Channel 0. The same register definition, DAR_LO1, is available for Channel 1 at address 860h.
DAR_LO0 (CH0): offset 808h
DAR_LO1 (CH1): offset 860h
The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DAR_LO:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length > 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported.

16.4.4 DMA Transfer Destination Address High (DAR_HI0)—Offset 80Ch

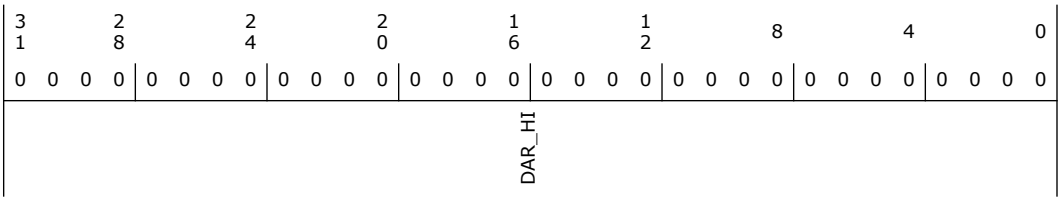
NOTE: DAR_HI0 is for DMA Channel 0. The same register definition, DAR_HI1, is available for Channel 1 at address 864h.
DAR_HI0 (CH0): offset 80Ch
DAR_HI1 (CH1): offset 864h
The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DAR_HI:** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length > 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported.

16.4.5 Linked List Pointer Low (LLP_LO0)—Offset 810h

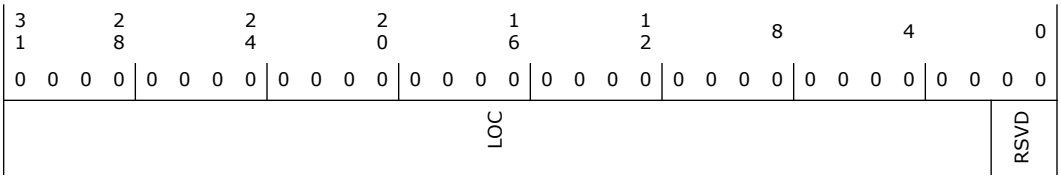
NOTE: LLP_LO0 is for DMA Channel 0. The same register definition, LLP_LO1, is available for Channel 1 at address 868h.
LLP_LO0 (CH0): offset 810h
LLP_LO1 (CH1): offset 868h
The register needs to be programmed to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**LOC (LOC):** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0h RO	Reserved.

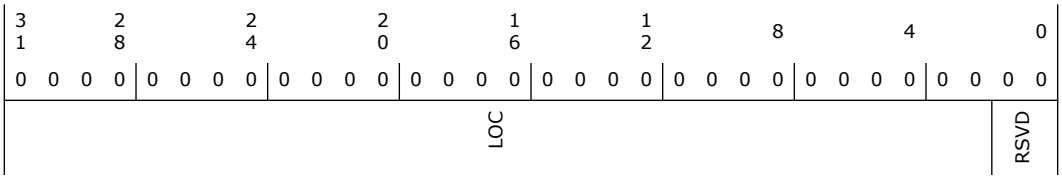
16.4.6 Linked List Pointer High (LLP_HI0)—Offset 814h

NOTE: LLP_HI0 is for DMA Channel 0. The same register definition, LLP_HI1, is available for Channel 1 at address 86Ch.
LLP_HI0 (CH0): offset 814h
LLP_LO1 (CH1): offset 86Ch
The register needs to be programmed to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled.

Access Method

Type: MEM Register (Size: 32 bits)
Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**LOC (LOC):** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0h RO	Reserved.

16.4.7 Control Register Low (CTL_LO0)—Offset 818h

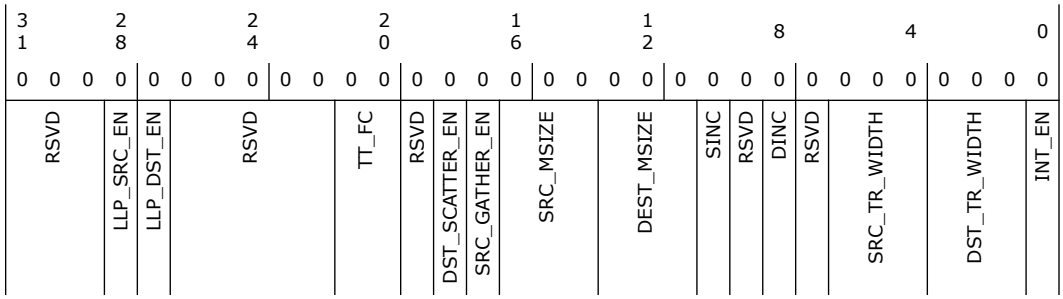
NOTE: CTL_LO0 is for DMA Channel 0. The same register definition, CTL_LO1, is available for Channel 1 at address 870h.
LLP_HI0 (CH0): offset 818h
LLP_LO1 (CH1): offset 870h
This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled. If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	Reserved.
28	0h RW	**LLP Source Enable (LLP_SRC_EN):** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0h RW	**LLP Destination Enable (LLP_DST_EN):** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	0h RO	Reserved.
21:20	0h RW	**Transfer Type and Flow Control (TT_FC):** The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	0h RO	Reserved.
18	0h RW	**Destination Scatter Enable (DST_SCATTER_EN):** 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0h RW	**Source Gather Enable (SRC_GATHER_EN):** 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0h RW	**Source Burst Transaction Length (SRC_MSIZE):** Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source.
13:11	0h RW	**Destination Burst Transaction Length (DEST_MSIZE):** Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination.
10	0h RW	**Source Address Increment (SINC):** Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)
9	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**Destination Address Increment (DINC):** Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0h RO	Reserved.
6:4	0h RW	**Source Transfer Width (SRC_TR_WIDTH):** BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width < 4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations)
3:1	0h RW	**Destination Transfer Width (DST_TR_WIDTH):** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width < 4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations)
0	0h RW	**Interrupt Enable (INT_EN):** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

16.4.8 Control Register High (CTL_HI0)—Offset 81Ch

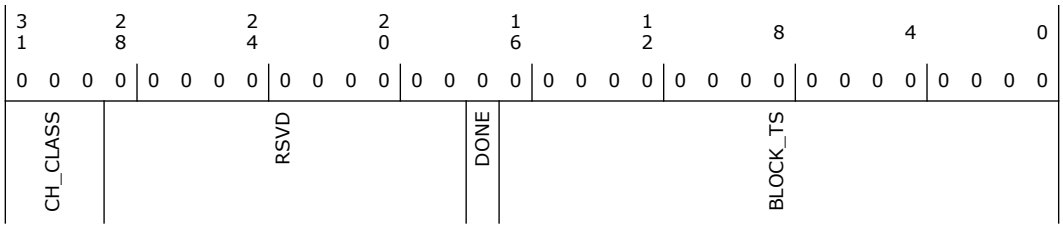
NOTE: CTL_HI0 is for DMA Channel 0. The same register definition, CTL_HI1, is available for Channel 1 at address 874h.
CTL_HI0 (CH0): offset 81Ch
CTL_HI1 (CH1): offset 874h
This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RW	**Channel Class (CH_CLASS):** A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior.
28:18	0h RO	Reserved.
17	0h RW	**DONE (DONE):** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	0h RW	**Block Transfer Size (BLOCK_TS):** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It doesn't mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

16.4.9 Source Status (SSTAT0)—Offset 820h

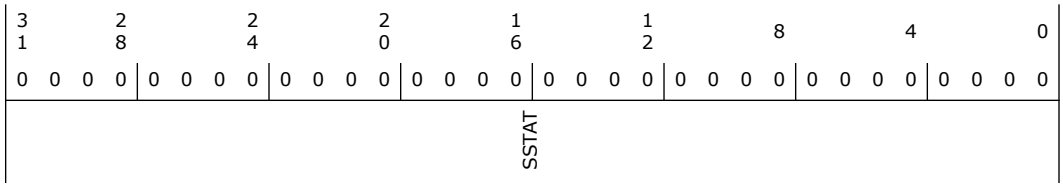
NOTE: SSTAT0 is for DMA Channel 0. The same register definition, SSTAT1, is available for Channel 1 at address 878h.
SSTAT0 (CH0): offset 820h
SSTAT1 (CH1): offset 878h
After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block.
Note : This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Source Status (SSTAT):** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

16.4.10 Destination Status (DSTAT0)—Offset 828h

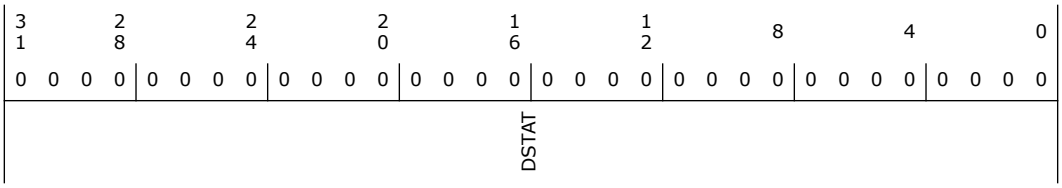
NOTE: DSTAT0 is for DMA Channel 0. The same register definition, DSTAT1, is available for Channel 1 at address 880h.
DSTAT0 (CH0): offset 828h
DSTAT1 (CH1): offset 880h
After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI.
Note : This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Destination Status (DSTAT):** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

16.4.11 Source Status Address Low (SSTATAR_LO0)—Offset 830h

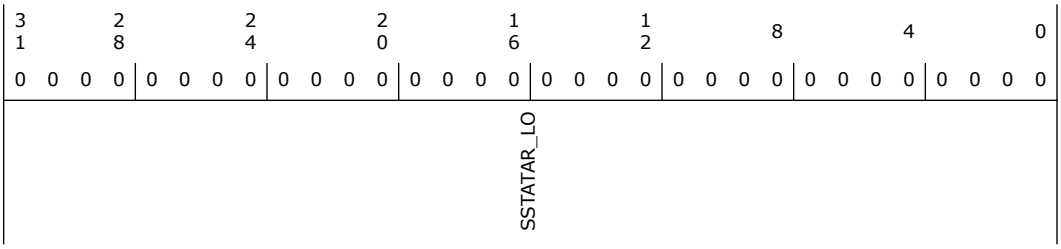
NOTE: SSTATAR_LO0 is for DMA Channel 0. The same register definition, SSTATAR_LO1, is available for Channel 1 at address 888h.
SSTATAR_LO0(CH0): offset 830h
SSTATAR_LO1(CH1): offset 888h
After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Source Status Address (SSTATAR_LO):** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

16.4.12 Source Status Address High (SSTATAR_HI0)—Offset 834h

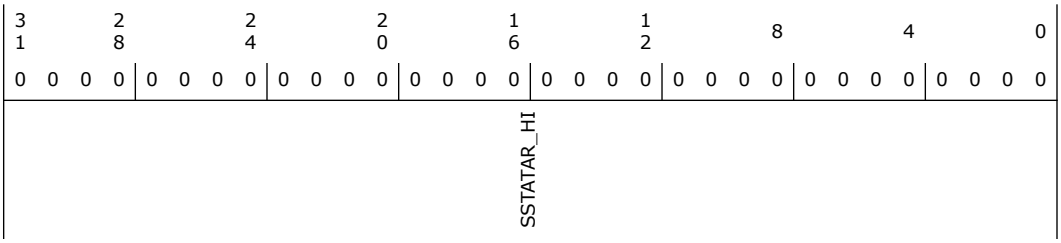
NOTE: SSTATAR_HI0 is for DMA Channel 0. The same register definition, SSTATAR_HI1, is available for Channel 1 at address 88Ch.
SSTATAR_HI0(CH0): offset 834h
SSTATAR_HI1(CH1): offset 88Ch
After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Source Status Address (SSTATAR_HI):** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

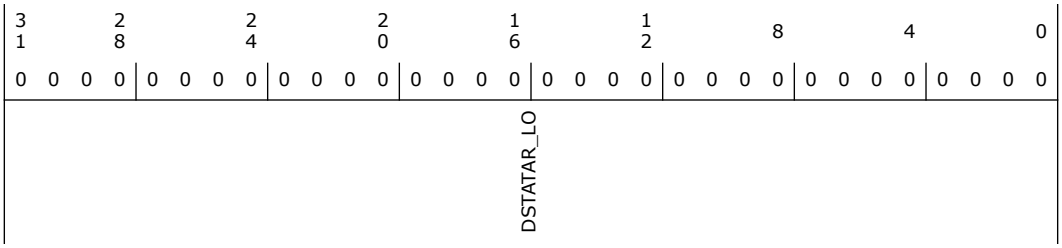
16.4.13 Destination Status Address Low (DSTATAR_LO0)—Offset 838h

NOTE: DSTATAR_LO0 is for DMA Channel 0. The same register definition, DSTATAR_LO1, is available for Channel 1 at address 890h.
DSTATAR_LO0(CH0): offset 838h
DSTATAR_LO1(CH1): offset 890h
After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Access Method

Type: MEM Register (Size: 32 bits)
Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Destination Status Address (DSTATAR_LO):** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

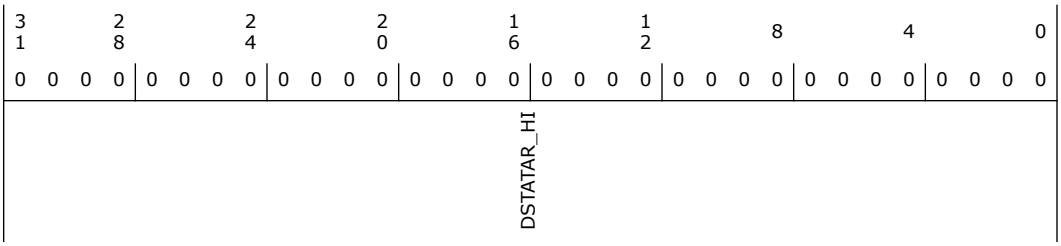
16.4.14 Destination Status Address High (DSTATAR_HI0)—Offset 83Ch

NOTE: DSTATAR_LO0 is for DMA Channel 0. The same register definition, DSTATAR_HI1, is available for Channel 1 at address 894h.
DSTATAR_HI0(CH0): offset 83Ch
DSTATAR_HI1(CH1): offset 894h
After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Access Method

Type: MEM Register (Size: 32 bits)
Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Destination Status Address (DSTATAR_HI):** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

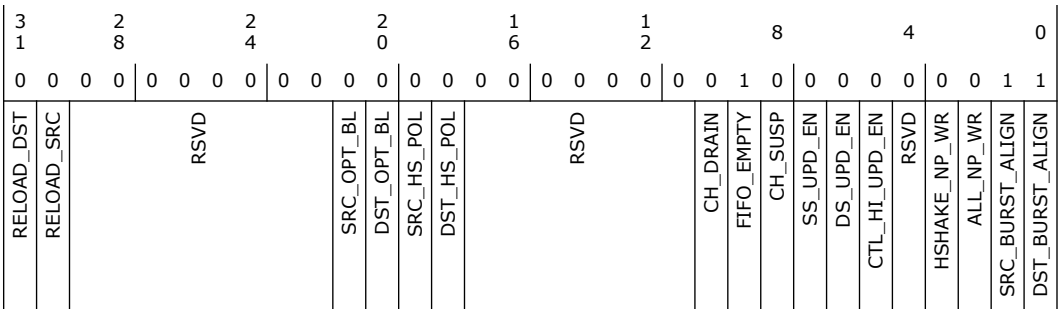
16.4.15 DMA Transfer Configuration Low (CFG_LO0)—Offset 840h

NOTE: CFG_LO0 is for DMA Channel 0. The same register definition, CFG_LO1, is available for Channel 1 at address 898h.
CFG_LO0(CH0): offset 840h
CFG_LO1(CH1): offset 898h
This register contains fields that configure the DMA transfer. The channel configuration register remains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Access Method

Type: MEM Register (Size: 32 bits)
Device: 21
Function: 0

Default: 203h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**RELOAD_DST:** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
30	0h RW	**RELOAD_SRC:** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RW	**SRC_OPT_BL:** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 <= BL <= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled
20	0h RW	**DST_OPT_BL:** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 <= BL <= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled
19	0h RW	**SRC_HS_POL:** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0h RW	**DST_HS_POL:** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17:11	0h RO	Reserved.
10	0h RW	**CH_DRAIN:** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND is asserted
9	1h RO	**FIFO_EMPTY:** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty
8	0h RW	**CH_SUSP:** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0h RW	**SS_UPD_EN:** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
6	0h RW	**DS_UPD_EN:** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0h RW	**CTL_HI_UPD_EN:** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0h RO	Reserved.
3	0h RW	**HSHAKE_NP_WR:** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted) This bit must be set to 1 for proper operation
2	0h RW	**ALL_NP_WR:** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	1h RW	**SRC_BURST_ALIGN:** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary
0	1h RW	**DST_BURST_ALIGN:** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary.

16.4.16 DMA Transfer Configuration High (CFG_HI0)—Offset 844h

NOTE: CFG_HI0 is for DMA Channel 0. The same register definition, CFG_HI1, is available for Channel 1 at address 89Ch.
CFG_HI0(CH0): offset 844h

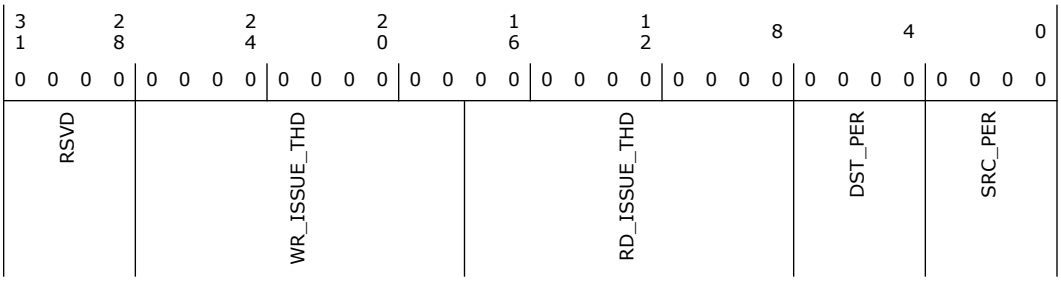
CFG_HI1(CH1): offset 89Ch
This register contains fields that configure the DMA transfer. The channel configuration register remains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	Reserved.
27:18	0h RW	**WR_ISSUE_THD:** Write Issue Threshold. Used to relax the issue criterion for Writes. Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	0h RW	**RD_ISSUE_THD:** Read Issue Threshold. Used to relax the issue criterion for Reads. Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.
7:4	0h RW	**DST_PER:** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface.
3:0	0h RW	**SRC_PER:** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface.

16.4.17 Source Gather (SGR0)—Offset 848h

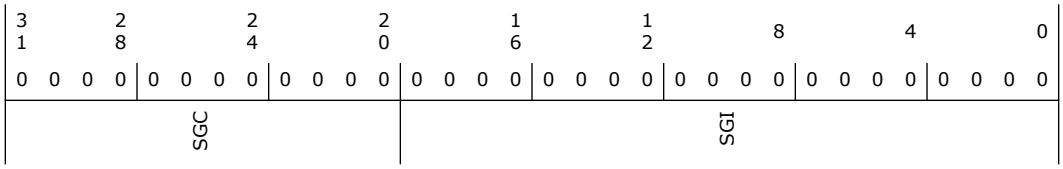
NOTE: SGR0 is for DMA Channel 0. The same register definition, SGR1, is available for Channel 1 at address 8A0h.
SGR0(CH0): offset 848h
SGR1(CH1): offset 8A0h
The Source Gather register contains two fields: Source gather count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gather interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled

for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

Access Method

Type: MEM Register (Size: 32 bits)
Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**SGC (SGC)**
19:0	0h RW	**SGI (SGI)**

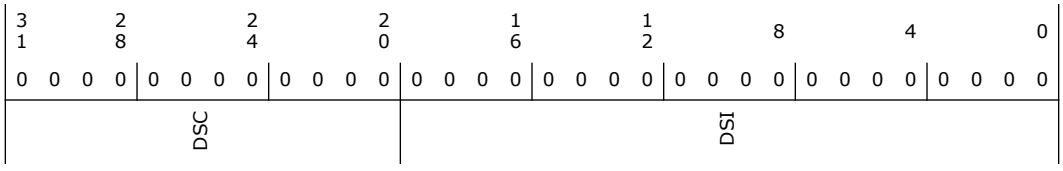
16.4.18 Destination Scatter (DSR0)—Offset 850h

NOTE: DSR0 is for DMA Channel 0. The same register definition, DSR1, is available for Channel 1 at address 8A8h.
DSR0(CH0): offset 850h
DSR1(CH1): offset 8A8h
The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC) . Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI) . Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

Access Method

Type: MEM Register (Size: 32 bits)
Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**DSC (DSC)**
19:0	0h RW	**DSI (DSI)**

16.4.19 Raw Interrupt Status (RawTfr)—Offset AC0h

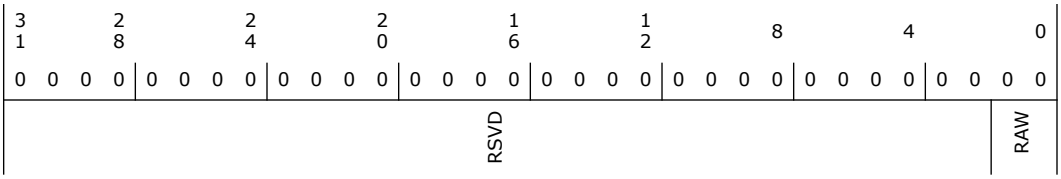
Interrupt events are stored in these Raw Interrupt Status registers before masking: RawBlock, RawDstTran, RawErr, RawSrcTran, and RawTfr. Each Raw Interrupt Status register has a bit allocated per channel, for example, RawTfr(2) is the Channel 2 raw transfer complete interrupt. Each bit in these registers is cleared by writing a 1 to the corresponding location in the ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr registers
The following RAW registers are available in the DMA
RawTfr - Raw Status for Transfer Interrupts
RawBlock - Raw Status for Block Interrupts Register
RawSrcTran - Raw Status for Source Transaction Interrupts Register
RawDstTran - Raw Status for Destination Transaction Interrupts Register
RawErr - Raw Status for Error Interrupts Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**Raw Interrupt Status (RAW):** Bit0 for channel 0 and bit 1 for channel 1.

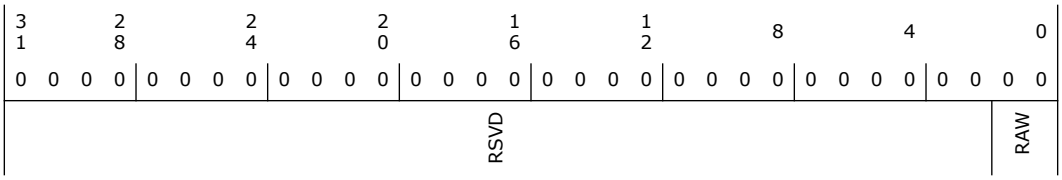
16.4.20 Raw Status for Block Interrupts (RawBlock)—Offset AC8h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**Raw interrupt status (RAW):** Bit 0 for channel 0 and bit 1 for channel 1.

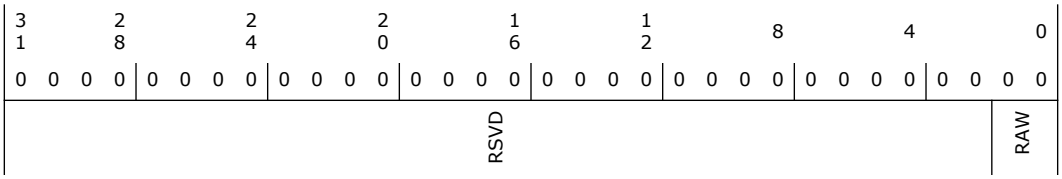
16.4.21 Raw Status for Source Transaction Interrupts (RawSrcTran)—Offset AD0h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**Raw interrupt status (RAW):** Bit 0 for channel 0 and bit 1 for channel 1.

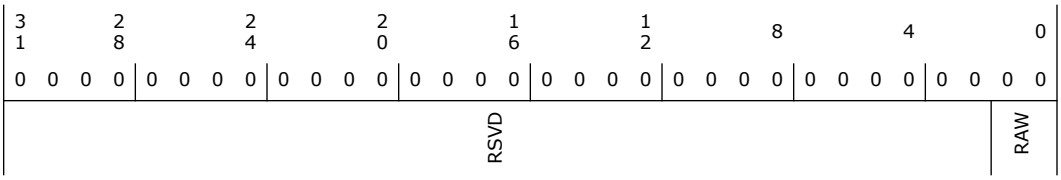
16.4.22 Raw Status for Destination Transaction Interrupts (RawDstTran)—Offset AD8h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**RAW:** Bit 0 for channel 0 and bit 1 for channel 1.

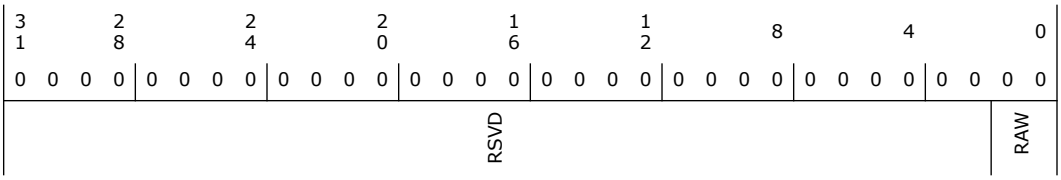
16.4.23 Raw Status for Error Interrupts (RawErr)—Offset AE0h

Interrupt events are stored in these Raw Interrupt Status registers before masking: RawBlock, RawDstTran, RawErr, RawSrcTran, and RawTfr. Each Raw Interrupt Status register has a bit allocated per channel, for example, RawTfr(2) is the Channel 2 raw transfer complete interrupt. Each bit in these registers is cleared by writing a 1 to the corresponding location in the ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr registers
The following RAW registers are available in the DMA
RawTfr - Raw Status for Transfer Interrupts
RawBlock - Raw Status for Block Interrupts Register
RawSrcTran - Raw Status for Source Transaction Interrupts Register
RawDstTran - Raw Status for Destination Transaction Interrupts Register
RawErr - Raw Status for Error Interrupts Register

Access Method

Type: MEM Register (Size: 32 bits)
Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**Raw Interrupt Status (RAW):** Bit 0 for channel 0 and bit 1 for channel 1.

16.4.24 Interrupt Status (StatusTfr)—Offset AE8h

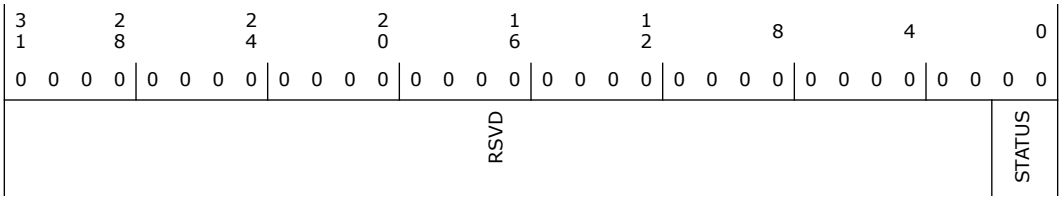
All interrupt events from all channels are stored in these Interrupt Status registers after masking: StatusBlock, StatusDstTran, StatusErr, StatusSrcTran, and StatusTfr. Each Interrupt Status register has a bit allocated per channel, for example, StatusTfr(2) is the Channel 2 status transfer complete interrupt. The contents of these registers are used to generate the interrupt signals (int or int_n bus, depending on interrupt polarity) leaving the DMA.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**Interrupt Status (STATUS):** Bit 0 for channel 0 and bit 1 for channel 1.

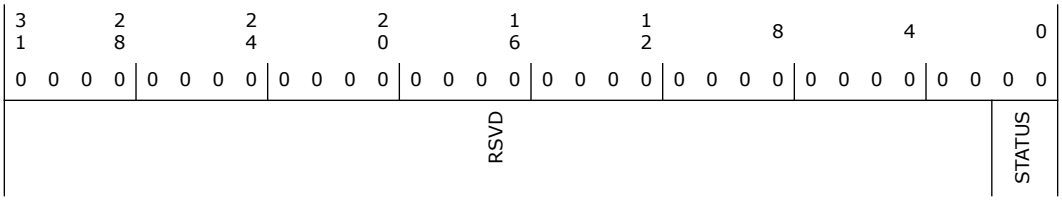
16.4.25 Status for Block Interrupts (StatusBlock)—Offset AF0h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**Interrupt status (STATUS):** Bit 0 for channel 0 and bit 1 for channel 1.

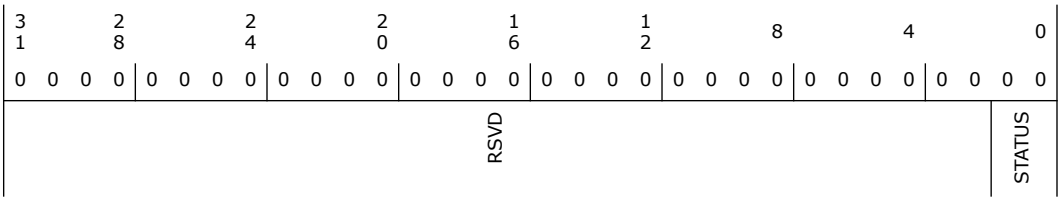
16.4.26 Status for Source Transaction Interrupts (StatusSrcTran)—Offset AF8h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**Interrupt status (STATUS):** Bit 0 is for channel 0 and bit 1 is for channel 1.

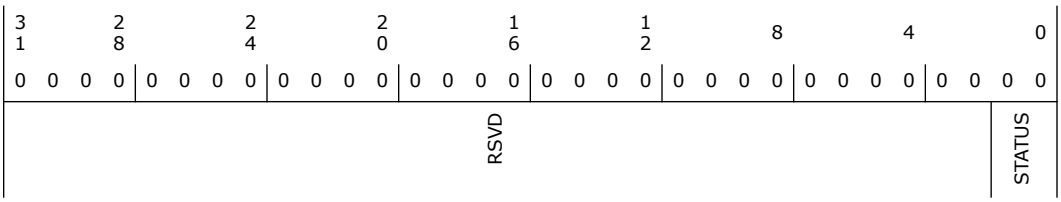
16.4.27 Status for Destination Transaction Interrupts (StatusDstTran)—Offset B00h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**Interrupt status (STATUS):** Bit 0 is for channel 0 and bit 1 is for channel 1.

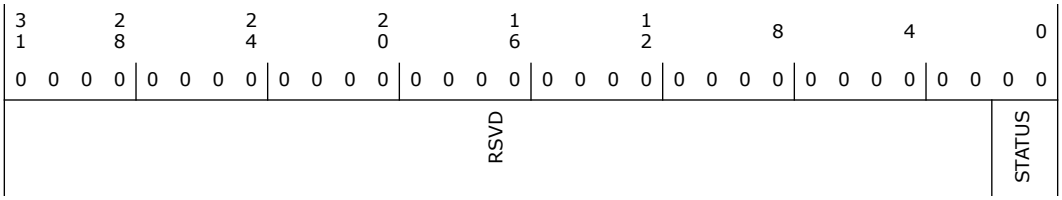
16.4.28 Status for Error Interrupts (StatusErr)—Offset B08h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**Interrupt status (STATUS):** Bit 0 is for channel 0 and bit 1 is for channel 1.

16.4.29 Mask for Transfer Interrupts (MaskTfr)—Offset B10h

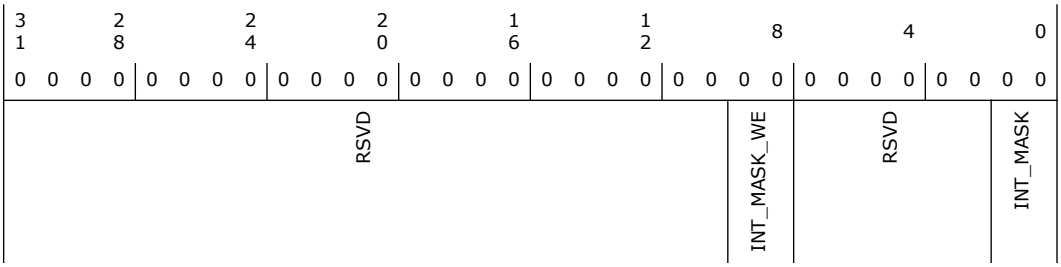
The contents of the Raw Status registers are masked with the contents of the Mask registers: MaskBlock, MaskDstTran, MaskErr, MaskSrcTran, and MaskTfr. Each Interrupt Mask register has a bit allocated per channel, for example, MaskTfr(2) is the mask bit for the Channel 2 transfer complete interrupt. When the source peripheral of DMA channel i is memory, then the source transaction complete interrupt, MaskSrcTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined signal. Similarly, when the destination peripheral of DMA channel i is memory, then the destination transaction complete interrupt, MaskDstTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined(_n) signal. A channel INT_MASK bit will be written only if the corresponding mask write enable bit in the INT_MASK_WE field is asserted on the same OCP write transfer. This allows software to set a mask bit without performing a read-modified write operation. For example, writing hex 01x1 to the MaskTfr register writes a 1 into MaskTfr(0), while MaskTfr(7:1) remains unchanged. Writing hex 00xx leaves MaskTfr(7:0) unchanged. Writing a 1 to any bit in these registers unmasks the corresponding interrupt, thus allowing the DMA to set the appropriate bit in the Status registers and int_* port signals.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:8	0h WO	**Interrupt Mask Write Enable (INT_MASK_WE):** 0 = write disabled 1 = write enabled
7:2	0h RO	Reserved.
1:0	0h RW	**Interrupt mask (INT_MASK):** 0-mask 1-unmask

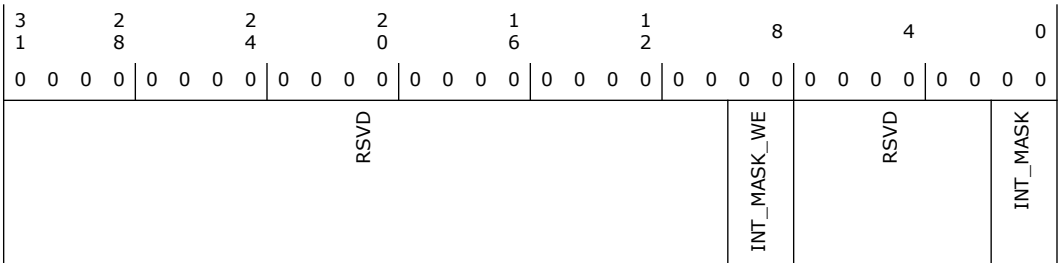
16.4.30 Mask for Block Interrupts (MaskBlock)—Offset B18h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:8	0h WO	**Interrupt Mask Write Enable (INT_MASK_WE):** 0 = write disabled 1 = write enabled
7:2	0h RO	Reserved.
1:0	0h RW	**Interrupt mask (INT_MASK):** 0-mask 1-unmask

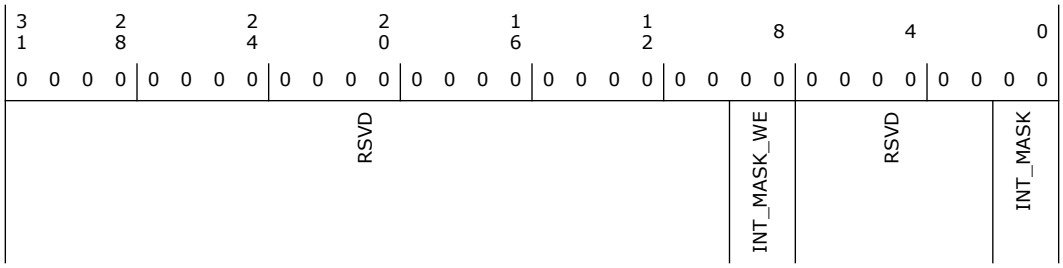
16.4.31 Mask for Source Transaction Interrupts (MaskSrcTran)—Offset B20h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:8	0h WO	**Interrupt Mask Write Enable (INT_MASK_WE):** 0 = write disabled 1 = write enabled
7:2	0h RO	Reserved.
1:0	0h RW	**Interrupt mask (INT_MASK):** 0-mask 1-unmask

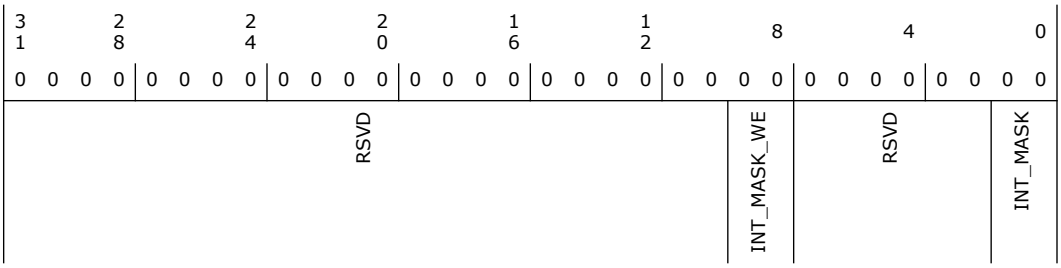
16.4.32 Mask for Destination Transaction Interrupts (MaskDstTran)—Offset B28h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:8	0h WO	**Interrupt Mask Write Enable (INT_MASK_WE):** 0 = write disabled 1 = write enabled
7:2	0h RO	Reserved.
1:0	0h RW	**Interrupt mask (INT_MASK):** 0-mask 1-unmask

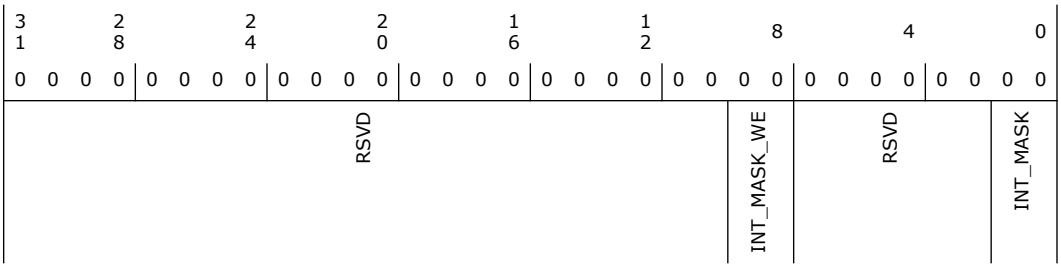
16.4.33 Mask for Error Interrupts (MaskErr)—Offset B30h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:8	0h WO	**Interrupt Mask Write Enable (INT_MASK_WE):** 0 = write disabled 1 = write enabled
7:2	0h RO	Reserved.
1:0	0h RW	**Interrupt mask (INT_MASK):** 0-mask 1-unmask

16.4.34 Clear for Transfer Interrupts (ClearTfr)—Offset B38h

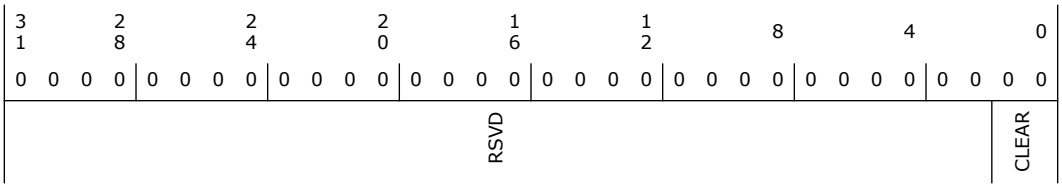
Each bit in the Raw Status and Status registers is cleared on the same cycle by writing a 1 to the corresponding location in the Clear registers: ClearBlock, ClearDstTran, ClearErr, ClearSrcTran, and ClearTfr. Each Interrupt Clear register has a bit allocated per channel, for example, ClearTfr(2) is the clear bit for the Channel 2 transfer complete interrupt. Writing a 0 has no effect. These registers are not readable.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h WO	**Interrupt Clear (CLEAR):** 0 = no effect 1 = clear interrupt

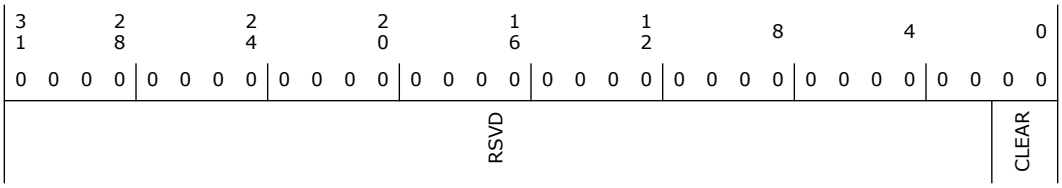
16.4.35 Clear for Block Interrupts (ClearBlock)—Offset B40h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h WO	**Interrupt Clear (CLEAR):** 0 = no effect 1 = clear interrupt

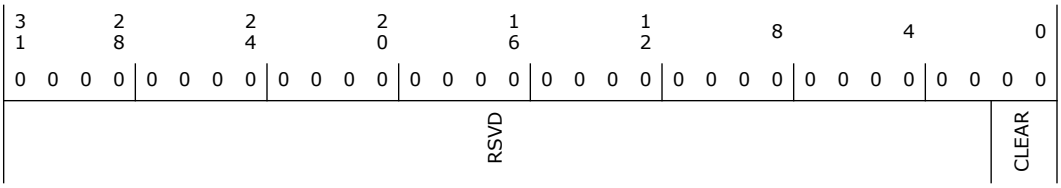
16.4.36 Clear for Source Transaction Interrupts (ClearSrcTran)—Offset B48h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h WO	**Interrupt clear (CLEAR):** 0 = no effect 1 = clear interrupt

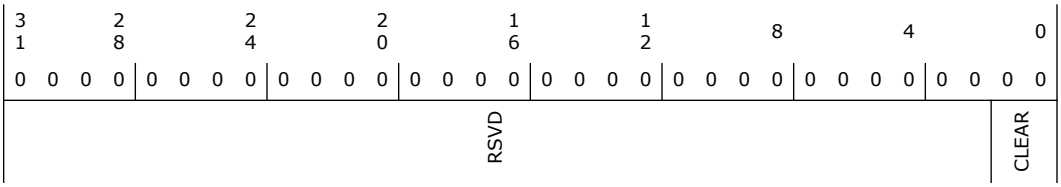
16.4.37 Clear for Destination Transaction Interrupts (ClearDstTran)—Offset B50h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h WO	**Interrupt Clear (CLEAR):** 0 = no effect 1 = clear interrupt

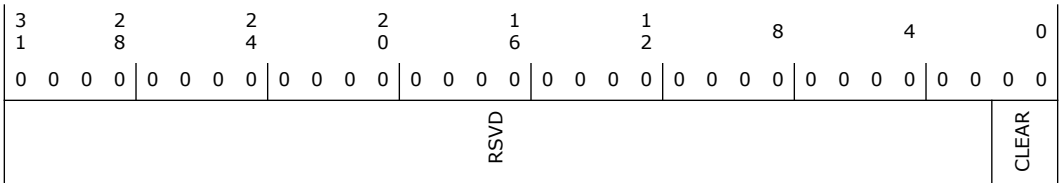
16.4.38 Clear for Error Interrupts (ClearErr)—Offset B58h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h WO	**Interrupt clear (CLEAR):** 0 = no effect 1 = clear interrupt

16.4.39 Combined Status register (StatusInt)—Offset B60h

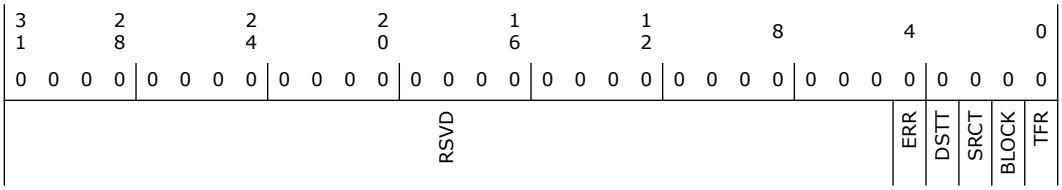
The contents of each of the five Status registers StatusTfr, StatusBlock, StatusSrcTran, StatusDstTran,StatusErr is ORed to produce a single bit for each interrupt type in the Combined Status register (StatusInt). This register is read-only.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4	0h RO	**ERR (ERR):** OR of the contents of StatusErr register.
3	0h RO	**DSTT (DSTT):** OR of the contents of StatusDst register.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	**SRCT (SRCT):** OR of the contents of StatusSrcTran register
1	0h RO	**Block (BLOCK):** OR of the contents of StatusBlock register.
0	0h RO	**TFR (TFR):** OR of the contents of StatusTfr register.

16.4.40 DMA Configuration (DmaCfgReg)—Offset B98h

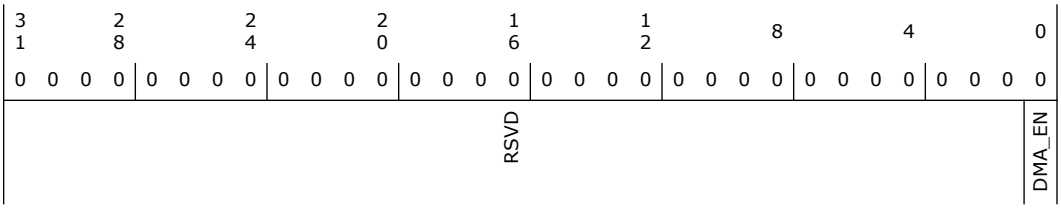
This register is used to enable the DMA, which must be done before any channel activity can begin. If the global channel enable bit is cleared while any channel is still active, then DmaCfgReg.DMA_EN still returns 1 to indicate that there are channels still active until hardware has terminated all activity on all channels, at which point the DmaCfgReg.DMA_EN bit returns 0.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RW	**DMA Enable (DMA_EN):** 0 = DMA Disabled 1 = DMA Enabled

16.4.41 DMA Channel Enable (ChEnReg)—Offset BA0h

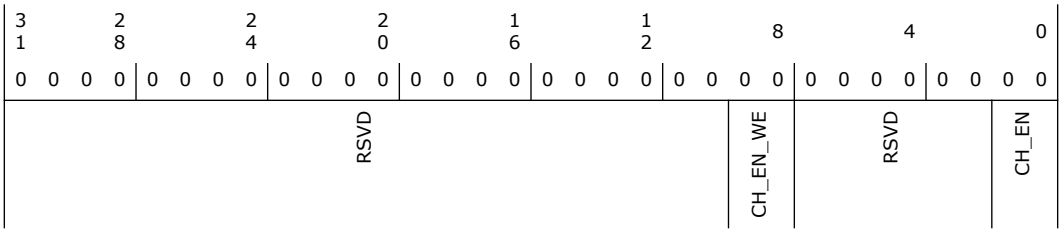
This is the DMA Channel Enable Register. If software needs to set up a new channel, then it can read this register in order to find out which channels are currently inactive, it can then enable an inactive channel with the required priority. All bits of this register are cleared to 0 when the global DMA channel enable bit, DmaCfgReg(0), is 0. When the global channel enable bit is 0, then a write to the ChEnReg register is ignored and a read will always read back 0. The channel enable bit, ChEnReg.CH_EN, is written only if the corresponding channel write enable bit, ChEnReg.CH_EN_WE, is asserted on the same OCP write transfer. For example, writing hex 01x1 writes a 1 into ChEnReg(0), while ChEnReg(7:1) remains unchanged. Writing hex 00xx leaves ChEnReg(7:0) unchanged. Note that a read-modified write is not required.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:8	0h WO	**CH_EN_WE**
7:2	0h RO	Reserved.
1:0	0h RW	**Channel Enable (CH_EN):** Enables/Disables the channel. Setting this bit enables a channel, clearing this bit disables the channel. 0 = Disable the Channel 1 = Enable the Channel The ChEnReg.CH_EN bit is automatically cleared by hardware to disable the channel after the last OCP transfer of the DMA transfer to the destination has completed. Software can therefore poll this bit to determine when this channel is free for a new DMA transfer.

16.5 I2C PCR Registers Summary

These registers are within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID + Register Offset).

Table 16-5. Summary of I2C PCR Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
200h	203h	PCI Configuration Control (PCICFGCTRL) for I2C0	00000100h
204h	207h	PCI Configuration Control (PCICFGCTRL) for I2C1	00000100h
208h	20Bh	PCI Configuration Control (PCICFGCTRL) for I2C2	00000100h
20Ch	20Fh	PCI Configuration Control (PCICFGCTRL) for I2C3	00000100h
210h	213h	PCI Configuration Control (PCICFGCTRL) for I2C4	00000100h
214h	217h	PCI Configuration Control (PCICFGCTRL) for I2C5	00000100h

16.5.1 PCI Configuration Control (PCICFGCTRL)

Default: 00000100h

NOTE: This register applies to the following I2C controller as follows:

I2C0: at offset 200h
I2C1: at offset 204h
I2C2: at offset 208h
I2C3: at offset 20Ch
I2C4: at offset 210h
I2C5: at offset 214h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
27:20	0h RW	**PCI IRQ:** IRQ number to be sent in the message with data field for Assert_IRQ and Deassert_IRQ message, Note: Bridge does not wire-or the interrupts from different functions before sending them even if they are tied to the same IPIN value of the same IRQ value by the BIOS. It is the responsibility of the interrupt controller to ensure that interrupts are wire-ored. Note: each PCI device (B:D:F) for Intel Serial IO interfaces (i.e.I2C, UART, GSPI) is limit to 4 functions max per PCI device, allowing each function to map to dedicated INT[A-D] and thus a unique IRQ number. Sharing IRQs is not allowed across any Serial IO interfaces B:D:F. All Serial IO interface B:D:F must have a unique IRQ number.
19:12	0h RW	**ACPI IRQ:** IRQ number to be sent in the message with data field for Assert_IRQ and Deassert_IRQ message, Note: Bridge does not wire-or the interrupts from different functions before sending them even if they are tied to the same IPIN value of the same IRQ value by the BIOS. It is the responsibility of the interrupt controller to ensure that interrupts are wire-ored. Note: each PCI device (B:D:F) for Intel Serial IO interfaces (i.e.I2C, UART, GSPI) is limit to 4 functions max per PCI device, allowing each function to map to dedicated INT[A-D] and thus a unique IRQ number. Sharing IRQs is not allowed across any Serial IO interfaces B:D:F. All Serial IO interface B:D:F must have a unique IRQ number.
11:8	0h RW	**Interrupt Pin:** This register indicates the values to be used for Global Interrupts. This value will also be reflected in the PCOS register IPIN value. 0 = No interrupt Pin 1 = INTA 2 = INTB 3 = INTC 4 = INTD 5 - FF: Reserved
7	0h RW	**BAR1 Disable:** BAR1 register in the PCOS space will become Read Only when this bit is set,
6:2	0h RW	**PME Support:** The value in this register will be XOR with the value in the PME_support strap and reflected in the PME_support register in the PCI configuration space. This register can be used as a mechanism to change the value of the PME_Status PCI config register field.
1	0h RW	**ACPI_INTR_EN:** When set, ACPI IRQ number field (bits 19:12) will be used for IRQ messages. When 0, PCI IRQ number field (bits 27:20) will be used for IRQ message.
0	0h RW	**PCI_CFG_DIS:** When set, PCI configuration accesses return UR response. When 0, PCI configuration accesses are supported.

16.6

§ §

17 SATA Interface (D23: F0)

17.1 SATA Configuration Registers Summary

Table 17-1. Summary of SATA Configuration Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	Identifiers (ID)—Offset 0h	X_8086h
4h	5h	Command (CMD)—Offset 4h	0h
6h	7h	Device Status (STS)—Offset 6h	210h
8h	8h	Revision ID (RID)—Offset 8h	See Register
9h	9h	Programming Interface (PI)—Offset 9h	1h
Ah	Bh	Class Code (CC)—Offset Ah	106h
Ch	Ch	Cache Line Size (CLS)—Offset Ch	0h
Dh	Dh	Master Latency Timer (MLT)—Offset Dh	0h
Eh	Eh	Header Type (HTYPE)—Offset Eh	0h
10h	13h	MSI-X Table Base Address (MXTBA)—Offset 10h	0h
14h	17h	MXP Base Address (MXPBA)—Offset 14h	0h
20h	23h	AHCI Index Data Pair Base Address (AIDPBA)—Offset 20h	1h
24h	27h	AHCI Base Address (ABAR)—Offset 24h	0h
2Ch	2Fh	Sub System Identifiers (SS)—Offset 2Ch	0h
34h	34h	Capabilities Pointer (CAP)—Offset 34h	80h
3Ch	3Dh	Interrupt Information (INTR)—Offset 3Ch	100h
70h	71h	PCI Power Management Capability ID (PID)—Offset 70h	A801h
72h	73h	PCI Power Management Capabilities (PC)—Offset 72h	4003h
74h	75h	PCI Power Management Control and Status (PMCS)—Offset 74h	8h
80h	81h	Message Signaled Interrupt Identifier (MID)—Offset 80h	7005h
82h	83h	Message Signaled Interrupt Message Control (MC)—Offset 82h	0h
84h	87h	Message Signaled Interrupt Message Address (MA)—Offset 84h	0h
88h	89h	Message Signaled Interrupt Message Data (MD)—Offset 88h	0h
90h	93h	Port Mapping Register (MAP)—Offset 90h	0h
92h	95h	Port Control and Status (PCS)—Offset 92h	0h
94h	97h	SATA Clock Gating Control Register (SCLKGC)—Offset 94h	0h
9Ch	9Fh	SATA General Configuration (SATAGC)—Offset 9Ch	0h
A0h	A0h	SATA Initialization Register Index (SIRI)—Offset A0h	0h
A4h	A7h	SATA Initialization Register Data (SIRD)—Offset A4h	0h
A8h	ABh	Serial ATA Capability Register 0 (SATACR0)—Offset A8h	100012h
ACh	AFh	Serial ATA Capability Register 1 (SATACR1)—Offset ACh	48h
C0h	C3h	Scratch Pad (SP)—Offset C0h	0h
D0h	D1h	MSI-X Identifiers (MXID)—Offset D0h	11h

Table 17-1. Summary of SATA Configuration Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
D2h	D3h	MSI-X Message Control (MXC)—Offset D2h	0h
D4h	D7h	MSI-X Table Offset / Table BIR (MXT)—Offset D4h	0h
D8h	DBh	MSI-X PBA Offset / PBA BIR (MXP)—Offset D8h	0h
E0h	E3h	BIST FIS Control/Status (BFCS)—Offset E0h	0h
E4h	E7h	BIST FIS Transmit Data 1 (BFTD1)—Offset E4h	0h
E8h	EBh	BIST FIS Transmit Data 2 (BFTD2)—Offset E8h	0h

17.1.1 Identifiers (ID)—Offset 0h

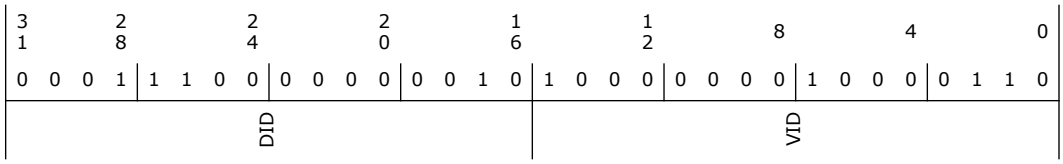
Identifiers

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 23
Function: 0

Default: xxxx8086h



Bit Range	Default & Access	Field Name (ID): Description
31:16	-- RO	**Device ID (DID):** Indicates the Device ID of the controller. See the Device and Version ID Table in Volume 1 for the default value.
15:0	8086h RO	**Vendor ID (VID):** 16-bit field which indicates the company vendor as Intel.

17.1.2 Command (CMD)—Offset 4h

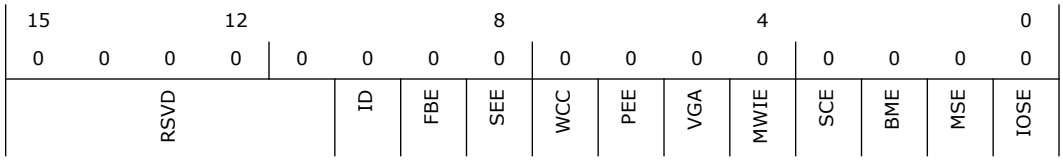
Command

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 23
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:11	0h RO	Reserved.
10	0h RW	**Interrupt Disable (ID):** This disables pin-based INTx# interrupts. This bit has no effect on MSI operation. 0 = Internal INTx# messages are generated if there is an interrupt and MSI is not enabled. 1 = Internal INTx# messages will not be generated.
9	0h RO	**Fast Back-to-Back Enable (FBE):** Hardwired to 0.
8	0h RW	**SERR# Enable (SEE):** 0 = SERR# messages will not be generated. 1 = SERR# messages are generated if STS.DPD register is set or bit 8 of the SATAGC.URD register is set.
7	0h RO	**Wait Cycle Enable (WCC):** Hardwired to 0.
6	0h RW	**Parity Error Response Enable (PEE):** 0 = Disabled. SATA controller will not generate PERR# when a data parity error is detected. 1 = Enabled. SATA controller will generate PERR# when a data parity error is detected.
5	0h RO	**VGA Palette Snooping Enable (VGA):** Hardwired to 0.
4	0h RO	**Memory Write and Invalidate Enable (MWIE):** Hardwired to 0.
3	0h RO	**Special Cycle Enable (SCE):** Hardwired to 0.
2	0h RW	**Bus Master Enable (BME):** Controls the SATA Controller's ability to act as a master for data transfers. This bit does not impact the generation of completions for split transaction commands.
1	0h RW	**Memory Space Enable (MSE):** Controls access to the SATA Controller's target memory space (for AHCI).
0	0h RW	**I/O Space Enable (IOSE):** Controls access to the SATA Controller's target I/O space.

17.1.3 Device Status (STS)—Offset 6h

Device Status

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 23
Function: 0

Default: 210h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0
DPE	SSE	RMA	RTA	STA	DEVT		DPD	RSVD			CL	IS	RSVD		

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1C	**Detected Parity Error (DPE):** 0 = No parity error detected by SATA controller. 1 = SATA controller detects a parity error on its interface.
14	0h RW/1C	**Signaled System Error (SSE):** 0 = No SERR# detected by SATA controller. 1 = SATA controller detects a SERR# on its interface.
13	0h RW/1C	**Received Master-Abort Status (RMA):** 0 = Master abort not generated. 1 = SATA controller received a master abort.
12	0h RW/1C	**Received Target-Abort Status (RTA):** 0 = Target abort not generated. 1 = SATA controller received a target abort.
11	0h RW/1C	**Signaled Target-Abort Status (STA):** This bit must be set by a target device whenever it terminates a transaction with Target-Abort. Devices that will never signal Target-Abort do not need to implement this bit.
10:9	1h RO	**DEVSEL# Timing Status (DEVT):** 01 = Hardwired; Controls the device select time for the SATA controller's PCI interface.
8	0h RW/1C	**Master Data Parity Error Detected (DPD):** For PCH, this bit can only be set on read completions received from the bus when there is a parity error. 0 = No data parity error received. 1 = SATA controller, as a master, either detects a parity error or sees the parity error line asserted, and the parity error response bit—bit 6 of the command register is set.
7:5	0h RO	Reserved.
4	1h RO	**Capabilities List (CL):** Indicates the presence of a capabilities list. The minimum requirement for the capabilities list must be PCI power management for the SATA Controller.
3	0h RO	**Interrupt Status (IS):** Reflects the state of INTx# messages, IRQ14 or IRQ15. 0 = Interrupt is cleared (independent of the state of CMD.ID). 1 = Interrupt is to be asserted
2:0	0h RO	Reserved.

17.1.4 Revision ID (RID)—Offset 8h

Revision ID

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 23
Function: 0

Default: See Register

7			4				0
0	0	0	0	0	0	0	0
RID							

Bit Range	Default & Access	Field Name (ID): Description
7:0	-- RO	**Revision ID (RID):** Indicates stepping of the host controller hardware. See the Device and Version ID Table in Volume 1 for default value.

17.1.5 Programming Interface (PI)—Offset 9h

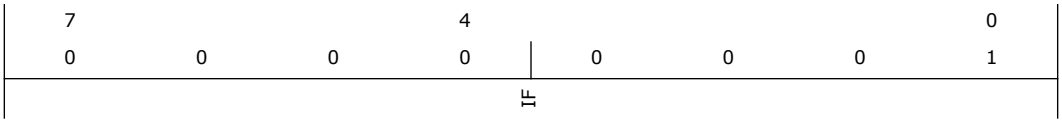
Programming Interface

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 23
Function: 0

Default: 1h



Bit Range	Default & Access	Field Name (ID): Description
7:0	1h RO	**Interface (IF):** If CC.SCC=06h (AHCI mode), it indicates that this is an AHCI HBA that has a major revision of 1. If CC.SCC=04h (RAID mode), it indicates that there is no programming interface (IF=00h).

17.1.6 Class Code (CC)—Offset Ah

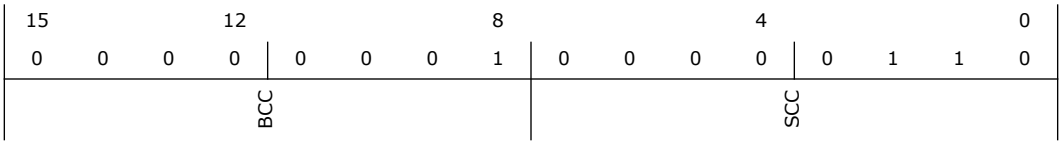
Class Code

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 23
Function: 0

Default: 106h



Bit Range	Default & Access	Field Name (ID): Description
15:8	1h RO	**Base Class Code (BCC):** Indicates that this is a mass storage device.
7:0	6h RO	**Sub Class Code (SCC):** This field specifies the sub-class code of the controller, per the table below: **MAP.SMS** — **SCC Register Value** 0b — 06h (AHCI Controller) 1b — 04h (RAID Controller)

17.1.7 Cache Line Size (CLS)—Offset Ch

Cache Line Size

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 23
Function: 0

Default: 0h

7			4				0
0	0	0	0	0	0	0	0
CLS							

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RO	**Cache Line Size (CLS):** This register has no meaning for the SATA controller.

17.1.8 Master Latency Timer (MLT)—Offset Dh

Master Latency Timer

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 23
Function: 0

Default: 0h

7			4				0
0	0	0	0	0	0	0	0
MLT							

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RO	**Master Latency Timer (MLT):** This register has no meaning for the SATA controller.

17.1.9 Header Type (HTYPE)—Offset Eh

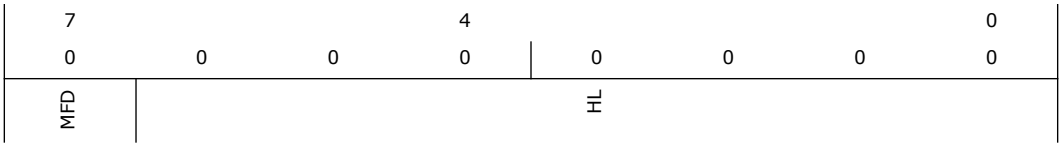
Header Type

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 23
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Multi-function Device (MFD):** Indicates this controller is not part of a multi-function device.
6:0	0h RO	**Header Layout (HL):** Indicates that the controller uses a target device layout.

17.1.10 MSI-X Table Base Address (MXTBA)—Offset 10h

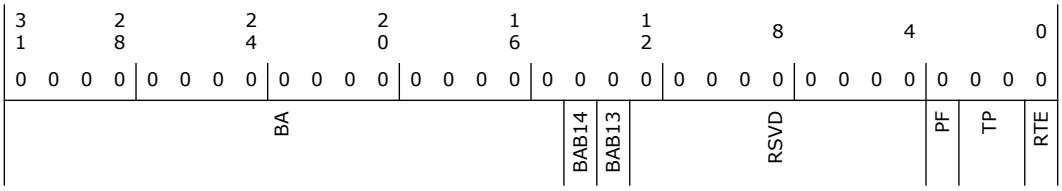
MSI-X Table Base Address. This BAR is used to allocate 32K, 16K or 8K Memory space for the MSI-X Table. The Memory space size is determined by BIOS by making bit-14 and bit-13 Read-Only '1' or Read-Write '0' based on SATAGC.MSS[1:0].

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RW	**Base Address (BA):** Base address of memory space.
14	0h RW	**Base Address Bit 14 (BAB14):** When SATAGC.MSS[1:0]=00, this bit is Read Only '0' else it's Read Write '0'.
13	0h RW	**Base Address Bit 13 (BAB13):** When SATAGC.MSS[1:0]=00 or 01, this bit is Read Only '0' else it's Read Write '0'.
12:4	0h RO	Reserved.
3	0h RO	**Prefetchable (PF):** Indicates that this range is not pre-fetchable.
2:1	0h RO	**Type (TP):** Indicates that this range can be mapped anywhere in 32-bit address space.
0	0h RO	**Resource Type Indicator (RTE):** Indicates a request for Memory space.

17.1.11 MXP Base Address (MXPBA)—Offset 14h

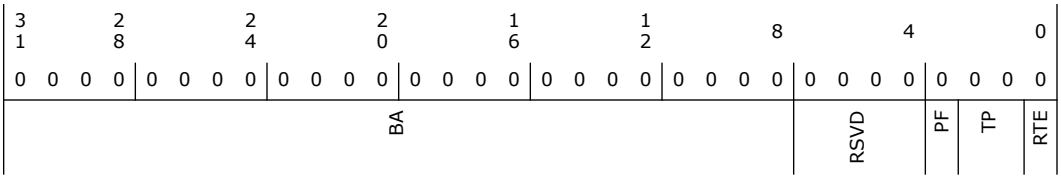
This BAR is used to allocate 256-byte Memory space for the MSI-X PBA.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RW	**Base Address (BA):** Base address of memory space (aligned to 256B).
7:4	0h RO	Reserved.
3	0h RO	**Prefetchable (PF):** Indicates that this range is not pre-fetchable.
2:1	0h RO	**Type (TP):** Indicates that this range can be mapped anywhere in 32-bit address space.
0	0h RO	**Resource Type Indicator (RTE):** Indicates a request for Memory space.

17.1.12 AHCI Index Data Pair Base Address (AIDPBA)—Offset 20h

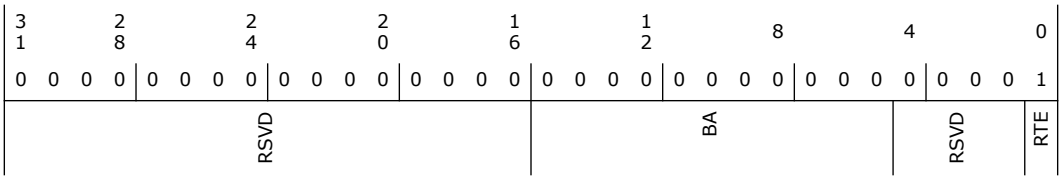
AHCI Index Data Pair Base Address. This BAR is used to allocate I/O space for the AHCI index/data pair mechanism. Note that hardware does not clear the BA bits (including BA4) when switching from IDE mode to non-IDE mode or vice versa. BIOS is responsible for clearing those bits to 0 since the number of writable bits changes after mode switching.

Access Method

Type: CFG Register (Size: 32 bits)

Device: 23
Function: 0

Default: 1h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:5	0h RW	**Base Address (BA):** Base address of the I/O space.
4:1	0h RO	Reserved.
0	1h RO	**Resource Type Indicator (RTE):** Indicates a request for IO space.

17.1.13 AHCI Base Address (ABAR)—Offset 24h

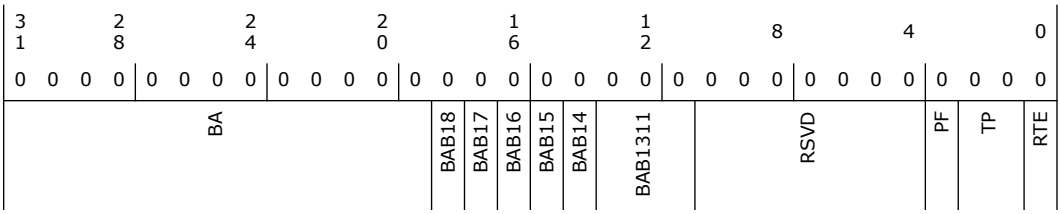
ABAR - AHCI Base Address. This egister represents a memory BAR allocating space for the AHCI memory registers. Note that bit[31:16] of this register must be programmed to a value greater than 0 to ensure the memory is mapped to an address of 1 MBytes and greater (i.e. ABAR must be 00010000h or greater). Otherwise, memory cycle targeting the ABAR range may not be accepted.. The Memory space size is determined by BIOS by making bit 15:11 Read-Only '1' or Read-Write '0' based on SATAGC.ASSEL[1:0].

Access Method

Type: CFG Register (Size: 32 bits)

Device: 23
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RW	**Base Address (BA):** Base address of register memory space.
18	0h RW	**Base Address Bit 18 (BAB18):** When SATAGC.ASSEL[2:0] selects an ABAR size bigger than 256K, this bit is Read Only '0' else it's Read Write '0'.
17	0h RW	**Base Address Bit 17 (BAB17):** When SATAGC.ASSEL[2:0] selects an ABAR size bigger than 128K, this bit is Read Only '0' else it's Read Write '0'.
16	0h RW	**Base Address Bit 16 (BAB16):** When SATAGC.ASSEL[2:0] selects an ABAR size bigger than 64K, this bit is Read Only '0' else it's Read Write '0'.
15	0h RW	**Base Address Bit 15 (BAB15):** When SATAGC.ASSEL[2:0] selects an ABAR size bigger than 32K, this bit is Read Only '0' else it's Read Write '0'.
14	0h RW	**Base Address Bit 14 (BAB14):** When SATAGC.ASSEL[2:0] selects an ABAR size bigger than 16K, this bit is Read Only '0' else it's Read Write '0'.
13:11	0h RW	**Base Address Bit 13-11 (BAB1311):** When SATAGC.ASSEL[2:0] selects an ABAR size bigger than 2K, this bit is Read Only '0' else it's Read Write '0'.
10:4	0h RO	Reserved.
3	0h RO	**Prefetchable (PF):** Indicates that this range is not pre-fetchable
2:1	0h RO	**Type (TP):** Indicates that this range can be mapped anywhere in 32-bit address space
0	0h RO	**Resource Type Indicator (RTE):** Indicates a request for register memory space.

17.1.14 Sub System Identifiers (SS)—Offset 2Ch

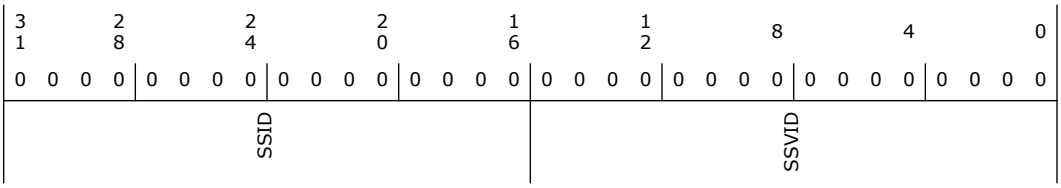
Sub System Identifiers. This register is initialized to logic 0 by the assertion of PLTRST#. This register can be written only once after PLTRST# de-assertion. This register is not reset by FLR.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW/O	**Subsystem ID (SSID):** This is written by BIOS. No hardware action taken on this value.
15:0	0h RW/O	**Subsystem Vendor ID (SSVID):** This is written by BIOS. No hardware action taken on this value.

17.1.15 Capabilities Pointer (CAP)—Offset 34h

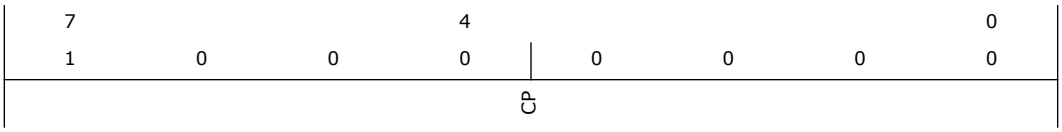
Capabilities Pointer

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 23
Function: 0

Default: 80h



Bit Range	Default & Access	Field Name (ID): Description
7:0	80h RW/L	**Capability Pointer (CP):** Indicates that the first capability pointer offset is 80h. **Note:** Refer to SATAGC.REGLOCK description in order to lock the register to become RO. This register is not reset by FLR.

17.1.16 Interrupt Information (INTR)—Offset 3Ch

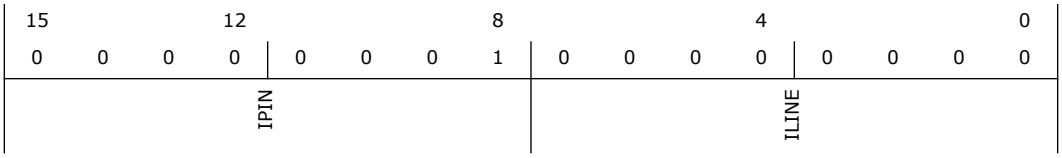
Interrupt Information

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 23
Function: 0

Default: 100h



Bit Range	Default & Access	Field Name (ID): Description
15:8	1h RW/O	**Interrupt Pin (IPIN):** This register tells which interrupt pin the device function uses. A value of 1 corresponds to INTA#. A value of 2 corresponds to INTB#. A value of 3 corresponds to INTC#. A value of 4 corresponds to INTD#. This register is not reset by FLR.
7:0	0h RW	**Interrupt Line (ILINE):** Software written value to indicate which interrupt line (vector) the interrupt is connected to. No hardware action is taken on this register. Interrupt Line register is not reset by FLR.

17.1.17 PCI Power Management Capability ID (PID)—Offset 70h

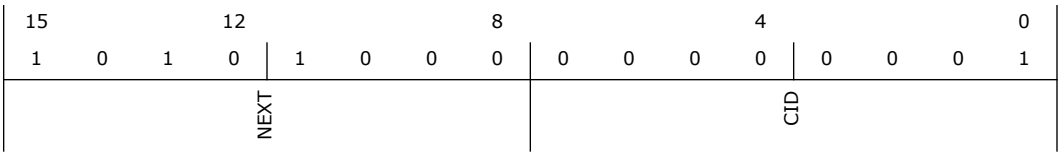
PCI Power Management Capability ID

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 23
Function: 0

Default: A801h



Bit Range	Default & Access	Field Name (ID): Description
15:8	A8h RW/L	**Next Capability (NEXT):** A8h is the location of the Serial ATA capability structure. **Note:** Refer to the SGC.REGLOCK description in order to lock the register to become RO.
7:0	1h RO	**Cap ID (CID):** Indicates that this pointer is a PCI power management capability.

17.1.18 PCI Power Management Capabilities (PC)—Offset 72h

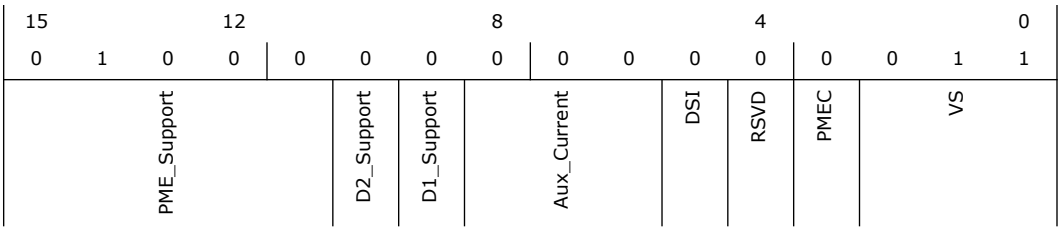
PCI Power Management Capabilities

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 23
Function: 0

Default: 4003h



Bit Range	Default & Access	Field Name (ID): Description
15:11	8h RO	**PME_Support (PME_Support):** The default value is 01000 which indicates PME# can be generated from the D3HOT state in the SATA controller.
10	0h RO	**D2_Support (D2_Support):** The D2 state is not supported.
9	0h RO	**D1_Support (D1_Support):** The D1 state is not supported.
8:6	0h RO	**Aux_Current (Aux_Current):** PME# from D3COLD state is not supported, therefore this field is 000b.
5	0h RO	**Device Specific Initialization (DSI):** Indicates that no device-specific initialization is required.
4	0h RO	Reserved.
3	0h RO	**PME Clock (PMEC):** Indicates that PCI clock is not required to generate PME#.
2:0	3h RO	**Version (VS):** Indicates support for Revision 1.2 of the PCI Power Management Specification.

17.1.19 PCI Power Management Control and Status (PMCS)—Offset 74h

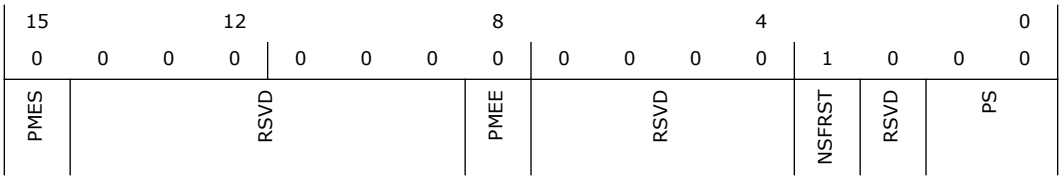
PCI Power Management Control and Status

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 23
Function: 0

Default: 8h



Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1C	**PME Status (PMES):** Bit is set when a PME event is to be requested, and if this bit and PMEE is set, a PME# will be generated from the SATA controller.
14:9	0h RO	Reserved.
8	0h RW	**PME Enable (PMEE):** When set, the SATA controller asserts PME# when exiting $D3_{HOT}$ on a wake event. **Note:** Software is advised to clear PMEE and PMES together prior to changing CC.SCC through MAP.SMS.
7:4	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
3	1h RO	**No Soft Reset (NSFRST):** These bits are used to indicate whether devices transitioning from $D3_{HOT}$ state to D0 state will perform an internal reset. 0 = Device transitioning from $D3_{HOT}$ state to D0 state perform an internal reset. 1 = Device transitioning from $D3_{HOT}$ state to D0 state do not perform an internal reset. Configuration content is preserved. Upon transition from the $D3_{HOT}$ state to D0 state initialized state, no additional operating system intervention is required to preserve configuration context beyond writing to the PowerState bits. Regardless of this bit, the controller transition from $D3_{HOT}$ state to D0 state by a system or bus segment reset will return to the state D0 uninitialized with only PME context preserved if PME is supported and enabled.
2	0h RO	Reserved.
1:0	0h RW	**Power State (PS):** These bits are used both to determine the current power state of the SATA controller and to set a new power state. 00 = D0 state 11 = $D3_{HOT}$ state When in the $D3_{HOT}$ state, the controller's configuration space is available, but the I/O and memory spaces are not. Additionally, interrupts are blocked.

17.1.20 Message Signaled Interrupt Identifier (MID)—Offset 80h

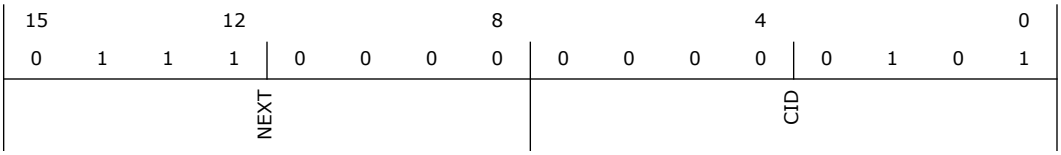
Message Signaled Interrupt Identifier

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 23
Function: 0

Default: 7005h



Bit Range	Default & Access	Field Name (ID): Description
15:8	70h RW/L	**Next Pointer (NEXT):** Indicates the next item in the list is the PCI power management pointer. BIOS may program this field to A8h indicating that the next item is Serial ATA Capability Structure. **Note:** Refer the SGC.REGLOCK description in order to lock the register to become RO.
7:0	5h RO	**Capability ID (CID):** Capabilities ID indicates MSI.

17.1.21 Message Signaled Interrupt Message Control (MC)—Offset 82h

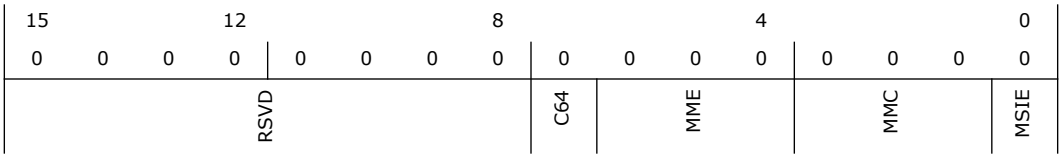
Message Signaled Interrupt Message Control

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 23
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	Reserved.
7	0h RO	**64 Bit Address Capable (C64):** Capable of generating a 32-bit message only.
6:4	0h RO	**Multiple Message Enable (MME):** When this field is cleared to 000 (and MSIE is set), only a single MSI message will be generated for all SATA ports, and bits [15:0] of the message vector will be driven from MD[15:0].
3:1	0h RO	**Multiple Message Capable (MMC):** Not supported.
0	0h RW	**MSI Enable (MSIE):** If set, MSI is enabled and traditional interrupt pins are not used to generate interrupts. Note that CMD.ID bit has not effect on MSI. Software must clear this bit to 0 to disable MSI first before changing the number of messages allocated in the MMC field.

17.1.22 Message Signaled Interrupt Message Address (MA)—Offset 84h

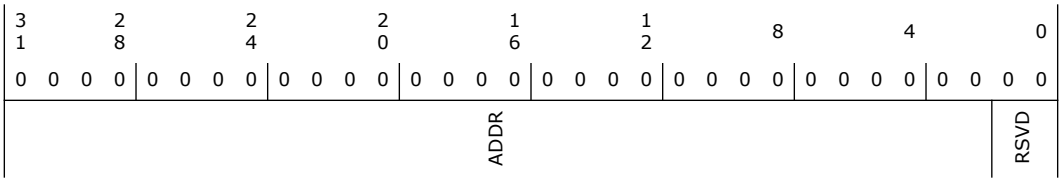
Message Signaled Interrupt Message Address

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**Address (ADDR):** Lower 32 bits of the system specified message address, always DWORD aligned.
1:0	0h RO	Reserved.

17.1.23 Message Signaled Interrupt Message Data (MD)—Offset 88h

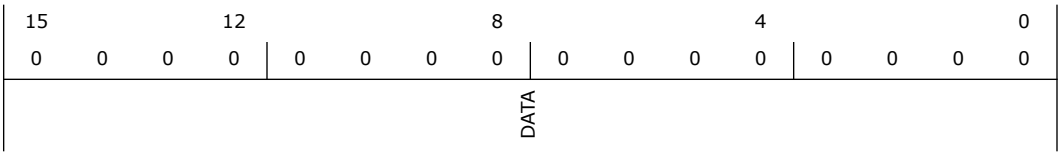
Message Signaled Interrupt Message Data

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 23
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW	**Data (DATA):** This 16-bit field is programmed by system software if MSI is enabled. Its content is driven onto the lower word of the data bus of the MSI memory write transaction.

17.1.24 Port Mapping Register (MAP)—Offset 90h

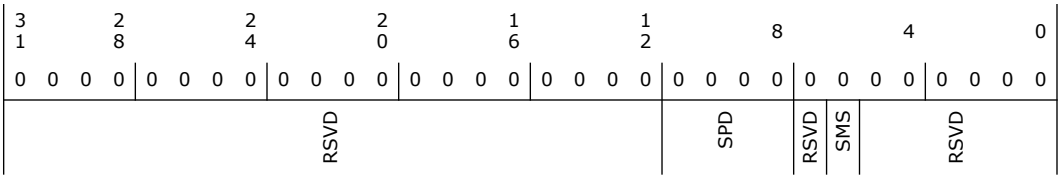
Port Mapping Register

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	Reserved.
11:8	0h RW/O	**SATA Port Disable (SPD):** Software programs these bits to disable a SATA port on the controller. 0 = Corresponding port is enabled. [Bit 8 = Port 0 and Bit 10 = Port 2; Bit 11 Reserved.] 1 = Corresponding port is disabled. [Bit 8 = Port 0 and Bit 10 = Port 2; Bit 11 Reserved.] **Notes:** 1. To ensure a port is properly disabled, BIOS shall configure MAP.SPD first and then configure PCS.PxE. 2. This field is not reset by FLR.
7	0h RO	Reserved.
6	0h RW	**SATA Mode Select (SMS):** Software programs these bits to control the mode in which the SATA Controller should operate: 0b = AHCI mode 1b = RAID mode **Notes:** 1. Software shall not manipulate MAP.SMS during runtime operation; i.e. the operating system will not do this. The BIOS may choose to switch from one mode to another during POST. 2. These bits are not reset by FLR.
5:0	0h RO	Reserved.

17.1.25 Port Control and Status (PCS)—Offset 92h

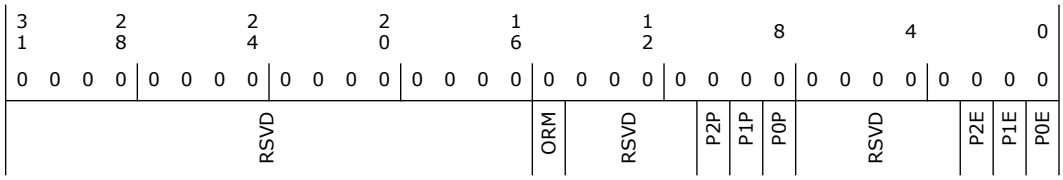
Port Control and Status. By default, the SATA ports are set (by hardware) to the disabled state (e.g. bits[5:0] == '0') as a result of an initial power on reset. When enabled by software, the ports can transition between the on, partial, and slumber states and can detect devices. When disabled, the port is in the off state and cannot detect any devices. This register is not reset by FLR. Note: AHCI specific notes: If an AHCI-aware or RAID enabled operating system is being booted then system BIOS shall insure that all supported SATA ports are enabled prior to passing control to the OS. Once the AHCI aware OS is booted it becomes the enabling/disabling policy owner for the individual SATA ports. This is accomplished by manipulating a port's PxSCTL.DET and PxCMD.SUD fields. Because an AHCI or RAID aware OS will typically not have knowledge of the PxE bits and because the PxE bits act as master on/off switches for the ports, pre-boot software must insure that these bits are set to '1' prior to booting the OS, regardless as to whether or not a device is currently on the port.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	0h RW	**OOB Retry Mode (ORM):** 0 = The SATA controller will not retry after an OOB failure 1 = The SATA controller will continue to retry after an OOB failure until successful (infinite retry)
14:11	0h RO	Reserved.
10	0h RO	**Port 2 Present (P2P):** This bit is set when COMINIT is received as a response to COMRESET. 0 = No device detected. 1 = The presence of a device on Port 2 has been detected. The status of this bit may change at any time. This bit is cleared when the port is disabled using P2E. This bit is not cleared upon surprise removal of a device.
9	0h RO	**Port 1 Present (P1P):** This bit is set when COMINIT is received as a response to COMRESET. 0 = No device detected. 1 = The presence of a device on Port 1 has been detected. The status of this bit may change at any time. This bit is cleared when the port is disabled using P1E. This bit is not cleared upon surprise removal of a device.
8	0h RO	**Port 0 Present (P0P):** This bit is set when COMINIT is received as a response to COMRESET. 0 = No device detected. 1 = The presence of a device on Port 0 has been detected. The status of this bit may change at any time. This bit is cleared when the port is disabled using P0E. This bit is not cleared upon surprise removal of a device.
7:3	0h RO	Reserved.
2	0h RW	**Port 2 Enabled (P2E):** 0 = Disabled. The port is in the 'off' state and cannot detect any devices. 1 = Enabled. The port can transition between the on, partial, and slumber states and can detect devices. **Note:** This bit takes precedence over P2CMD.SUD (offset ABAR+218h:bit 1). When MAP.SPD[2] is 1, this is reserved and is read-only 0.
1	0h RW	**Port 1 Enabled (P1E):** 0 = Disabled. The port is in the 'off' state and cannot detect any devices. 1 = Enabled. The port can transition between the on, partial, and slumber states and can detect devices. **Note:** This bit takes precedence over P1CMD.SUD (offset ABAR+198h:bit 1). When MAP.SPD[1] is 1, this is reserved and is read-only 0.
0	0h RW	**Port 0 Enabled (P0E):** 0 = Disabled. The port is in the 'off' state and cannot detect any devices. Enabled. The port can transition between the on, partial, and slumber states and can detect devices. **Note:** This bit takes precedence over P0CMD.SUD (offset ABAR+118h:bit 1). When MAP.SPD[0] is 1, this is reserved and is read-only 0.

17.1.26 SATA Clock Gating Control Register (SCLKGC)—Offset 94h

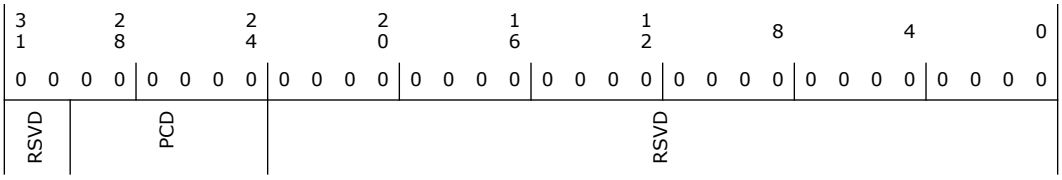
SATA Clock Gating Control Register. Software must not change the default value of any of the reserved bits. If the software changes any of those bits, the result is undefined and the controller may malfunction.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29:24	0h RW	**Port Clock Disable (PCD):** 0 = All clocks to the associated port logic will operate normally. 1 = The backbone clock driven to the associated port logic is gated and will not toggle. Assignment of the bits is: Bit 29: Reserved Bit 28: Reserved Bit 27: Reserved Bit 26: Port 2, this bit is only applicable to project(s): That has port 2 physically; Bit 25: Port 1, this bit is only applicable to project(s): That has port 1 physically; Bit 24: Port 0, this bit is only applicable to project(s): That has port 0 physically. If a particular port is not available, software shall set the corresponding bit to 1. Software can also set the corresponding bit(s) to 1 after disabling particular port(s). Software cannot set the PCD [port x]='1' if the corresponding PCS.PxE='1' or AHCI GHC.PI[x]='1'.
23:0	0h RO	Reserved.

17.1.27 SATA General Configuration (SATAGC)—Offset 9Ch

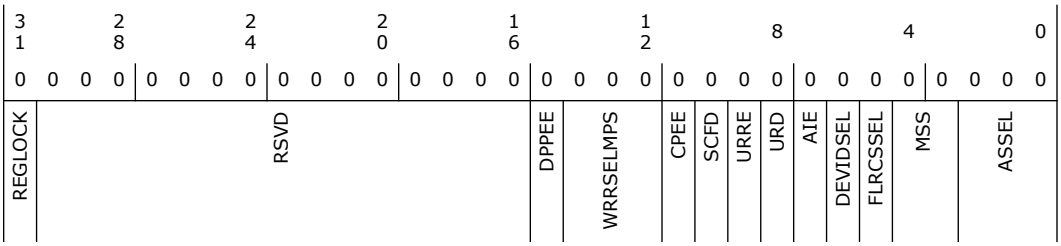
SATA General Configuration

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/O	**Register Lock (REGLOCK):** 0 = Will not lock CAP.CP, PID.NEXT, MID.NEXT, or SATACR0.NEXT 1 = Setting this bit will lock CAP.CP, PID.NEXT, MID.NEXT, and SATACR0.NEXT. Once locked, these register bits will become RO. BIOS is requested to program this field to '1' prior to OS handoff. **Note:** This field is not reset by FLR.
30:16	0h RO	Reserved.
15	0h RW	**Data Phase Parity Error Eenable (DPPEE):** When '1', IOSF data phase parity error handling is enabled. When '0', the data phase parity error handling is disabled. **Note:** This field is not reset by FLR.
14:12	0h RW	**Write Request_Size Select/Max_Payload_Size (WRRSELMPS):** These two bits select the max write request size that SATA host controller will initiate for DMA write to memory. SATA host controller will internally break up larger write request based on these bits. The request is address-aligned to the selected size. Defined encodings for this field are: 000b = 128 address aligned bytes max payload size 111b = 64 address aligned bytes max payload size. All other values are reserved for SATA host controller. **Note:** This field is not reset by FLR (not supported).
11	0h RW	**Command Parity Error Enable (CPEE):** When '1', command parity error handing is enable. When '0' the command parity error handling is disabled. **Note:** This field is not reset by FLR.
10	0h RW	**SATA Controller Function Disable (SCFD):** BIOS program this bit to 1 to disable the SATA Controller function. When 0, SATA Controller function is enabled. When disable, SATA Host Controller will not claimed the register access targeting its Configuration Space. In IOSF primary Fabric Decode scheme, it's expected BIOS also program the corresponding bit used by the Fabric Decoder accordingly hence both SATA SIP and Fabric Decoder are in sync, and BIOS need to program this bit before programming the one in Fabric Decoder. Once this bit is set, BIOS isnot able to revert it back to Function Enable until next round of platform reset.
9	0h RW	**Unsupported Request Reporting Enable (URRE):** If set to 1 by software, it allows reporting of an Unsupported Request as a system error. If both URRE and PCI configuration SERR# Enable registers are set to a 1, then the agent must set the Signaled System Error bit in the PCI Status register and send a DO_SERR message in IOSF-SB interface.
8	0h RW/1C	**Unsupported Request Detected (URD):** Set to 1 by hardware upon detecting an Unspported Request on IOSF Primary interface that is not considered Advisory Non-Fatal. Cleared to 0 by SW.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW/O	**Alternate ID Enable (AIE):** 0 = Clearing this bit when in RAID mode, the SATA Controller located at Device 23: Function 0 will report its Device ID as 2822h for Desktop SKUs or 282Ah for Mobile SKUs of the PCH. Clearing this bit is required for the Intel® Rapid Storage Technology driver (including the Microsoft* Windows* Vista operating system and later in-box version of the driver) to load on the platform. Intel® Smart Response Technology also requires that the bit be cleared in order to be enabled on the platform. 1 = Setting this bit when in RAID mode, the SATA Controller located at Device 23: Function 0 will report its Device ID as A107h for Desktop SKUs or 9D07h for Mobile SKUs of the Chipset. This setting will prevent the Intel® Rapid Storage Technology driver (including the Microsoft* Windows* operating system in-box version of the driver) from loading on the platform. During the Microsoft* Windows* OS installation, the user will be required to "load" (formerly done by pressing the F6 button on the keyboard) the appropriate RAID storage driver that is enabled by this setting. **Note:** BIOS is recommended to program this bit prior to programming the MAP.SMS field to reflect RAID. This field is reset by PLTRST# and BIOS is required to reprogram the value (either 0 or 1) after resuming from S3, S4 or S5. This insures that the value is properly and cannot be changed during runtime. **Note:** This field is not reset by FLR (not supported).
6	0h RW/O	**AIE0 DevID Selection (DEVIDSEL):** This register allows BIOS to select Device ID when AIE=0 and Server Feature (SATA AIE DEVIDSEL) Disable Fuse =0. This bit only has effect in Desktop SKU. In Mobile SKU this bit has no effect at all. Refer to config register offset 09h PI for usage. 0 : 2822h 1 : 2826h **Note:** WBG BIOS is required to program this field to 1 together with the write to the AIE bit in a single configuration write cycle. LPT BIOS is required to program this bit to 0 together with the write to the AIE bit in a single configuration write cycle. **Note:** When Server Feature (SATA AIE DEVIDSEL) Disable Fuse is programmed to 1, this disables the writeability of this DEVIDSEL register bit, and becomes RO with a value of 0, which only allows a choice of 2822h. **Note:** This field is not reset by FLR.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW/O	**FLR Capability Selection (FLRCSSEL):** This allows the FLR Capability to be bypassed. Refer to config offset B0h. BIOS is required to program this bit to 1 and config offset A8h SATACR0.NEXT to 00h. **Note:** This field is not reset by FLR.
4:3	0h RW/O	**MXTBA Size Select (MSS):** These 2 bits select the size of the Memory space for the MSI-X Table defined in BAR 0 (Configuration space offset 10h). **MSS[1:0] — MSI-X Table Memory space size** 00 — 32K 01 — 16K 10 — 8K 11 — Reserved **Note:** This field is not reset by FLR (not supported).
2:0	0h RW/O	**ABAR Size Select (ASSEL):** These 3 bits select the size of the Memory space for the ABAR in BAR 5 (Configuration space offset 24h). **ASSEL[2:0] — ABAR Memory space size** 000 — 2K 001 — 16K 010 — 32K 011 — 64K 100 — 128K 101 — 256K 110 — 512K 111 — Reserved **Note:** This field is not reset by FLR (not supported).

17.1.28 SATA Initialization Register Index (SIRI)—Offset A0h

SATA Initialization Register Index

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 23
Function: 0

Default: 0h

7			4				0
0	0	0	0	0	0	0	0
IDX						RSVD	

Bit Range	Default & Access	Field Name (ID): Description
7:2	0h RW	**Index (IDX):** 6-bit index pointer into the 256-byte space. Data is written into the SIRD register and read from the SIRD register. This point to a DWord register. The byte enables on the SIRD register affect what will be written. Refer to SATA Initialization Register section for detail of the register space.
1:0	0h RO	Reserved.

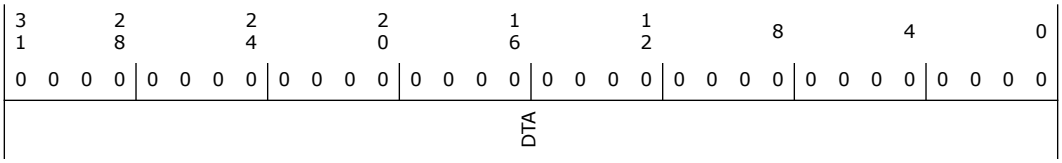
17.1.29 SATA Initialization Register Data (SIRD)—Offset A4h

SATA Initialization Register Data

Access Method

Type: CFG Register (Size: 32 bits)
Device: 23
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data (DTA):** 32-bit data value that is written to the register pointed to by SIRI, or read from the register pointed to by SIRI.

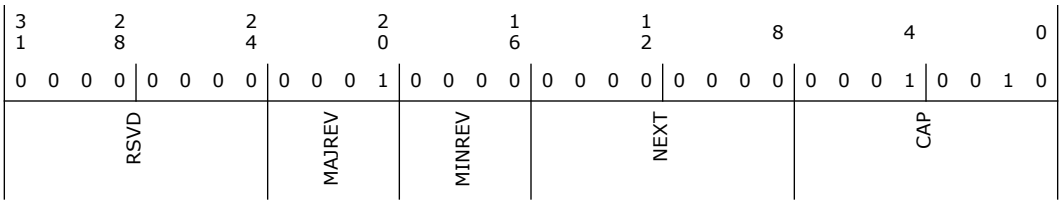
17.1.30 Serial ATA Capability Register 0 (SATACR0)—Offset A8h

Note that the SATACR0.NEXT is not changed from RO to become RWO because there is an existing method (SATAGC.FLRCSSEL bit) to bypass the FLR Capability structure. And FLR Capability ID.NEXT is already indicating end of capability structure, it does not need change to be RWO.

Access Method

Type: CFG Register (Size: 32 bits)
Device: 23
Function: 0

Default: 100012h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:20	1h RO	**Major Revision (MAJREV):** Major revision number of the SATA Capability Pointer implemented.
19:16	0h RO	**Minor Revision (MINREV):** Minor revision number of the SATA Capability Pointer implemented.
15:8	0h RW/L	**Next Capability Pointer (NEXT):** 00h indicating the final item in the Capability List. The RW/L register attribute allows for flexibility in determining the capability structure available in this PCI function. Refer to SATAGC.REGLOCK description in order to lock the register to become RO. This register is not reset by FLR.
7:0	12h RO	**Capability ID (CAP):** The value of 12h has been assigned by the PCI SIG to designate the SATA Capability pointer.

17.1.31 Serial ATA Capability Register 1 (SATACR1)—Offset ACh

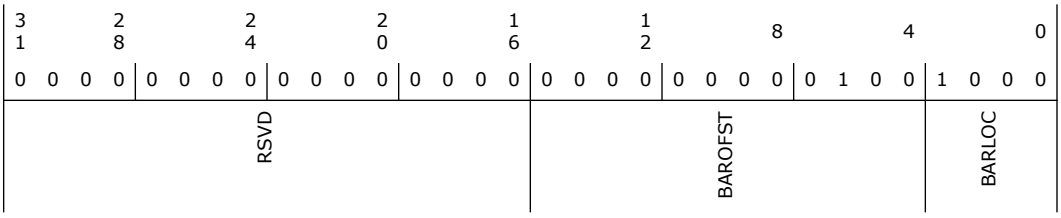
Serial ATA Capability Register 1.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 48h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:4	4h RO	**BAR Offset (BAROFST):** Indicates the offset into the BAR where the Index/Data pair are located (in DWord granularity). The Index and Data I/O registers are located at offset 10h within the I/O space defined by LBAR. A value of 004h indicates offset 10h. 000h = 0h offset 001h = 4h offset 002h = 8h offset 003h = Bh offset 004h = 10h offset ... FFFh = 3FFFh offset (maximum 16KB)
3:0	8h RO	**BAR Location (BARLOC):** Indicates the absolute PCI Configuration register address of the BAR containing the Index/Data pair (in DWord granularity). The Index and Data I/O registers reside within the space defined by LBAR in the SATA controller. A value of 8h indicates offset 20h, which is LBAR. 0000 - 0011b = reserved 0100b = 10h => BAR0 0101b = 14h => BAR1 0110b = 18h => BAR2 0111b = 1Ch => BAR3 1000b = 20h => LBAR 1001b = 24h => BAR5 1010–1110b = reserved 1111b = Index/Data pair in PCI Configuration space. This is not supported in the PCH.

17.1.32 Scratch Pad (SP)—Offset C0h

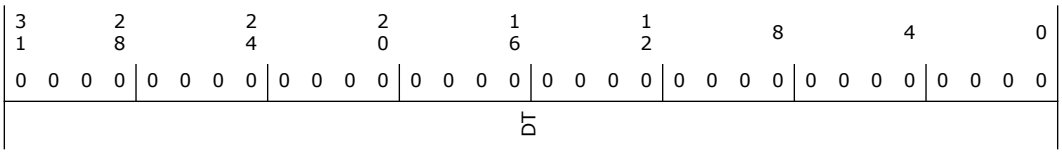
Scratch Pad.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data (DT):** This is a read/write register that is available for software to use. No hardware action is taken on this register.

17.1.33 MSI-X Identifiers (MXID)—Offset D0h

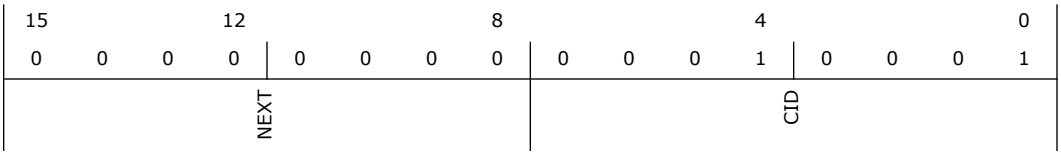
MSI-X Identifiers

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 23
Function: 0

Default: 11h



Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RW/L	**Next Pointer (NEXT):** Indicates the next item in the list. This may be other capability pointers or it may be the last item in the list.The RW/L register attribute allows for flexibility in determining the capability structure available in this PCI function. Refer to SATAGC.REGLOCK description in order to lock the register to become RO. This register is not reset by FLR.
7:0	11h RO	**Capability ID (CID):** Capabilities ID indicates this is an MSI-X capability.

17.1.34 MSI-X Message Control (MXC)—Offset D2h

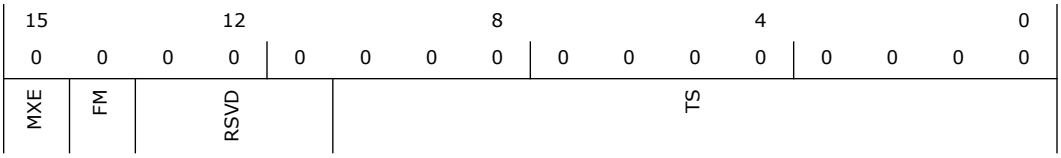
MSI-X Message Control

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 23
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**MSI-X Enable (MXE):** If set to '1' and the MSI Enable bit in the MSI Message Control register is cleared to '0', the function is permitted to use MSI-X to request service and is prohibited from using its INTx# pin (if implemented). If cleared to '0', the function is prohibited from using MSI-X to request service.
14	0h RW	**Function Mask (FM):** If set to '1', all of the vectors associated with the function are masked, regardless of their per vector Mask bit states. If cleared to '0', each vector's Mask bit determines whether the vector is masked or not. Setting or clearing the MSI-X Function Mask bit has no effect on the state of the per vector Mask bits.
13:11	0h RO	Reserved.
10:0	0h RO	**Table Size (TS):** This value indicates the size of the MSI-X Table as the value n, which is encoded as n - 1. For example, a returned value of 3h corresponds to a table size of 4.

17.1.35 MSI-X Table Offset / Table BIR (MXT)—Offset D4h

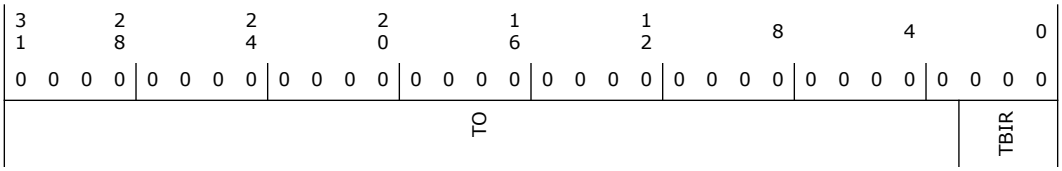
MSI-X Table Offset / Table BIR

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Table Offset (TO):** Used as an offset from the address contained by one of the function's Base Address registers to point to the base of the MSI-X Table. The lower three Table BIR bits are masked off (cleared to 000b) by system software to form a 32-bit Qword-aligned offset.
2:0	0h RO	**Table BIR (TBIR):** This field indicates which one of a function's Base Address registers, located beginning at 10h in Configuration Space, is used to map the function's MSI-X Table into system memory. A read-only value of '0' means 10h.

17.1.36 MSI-X PBA Offset / PBA BIR (MXP)—Offset D8h

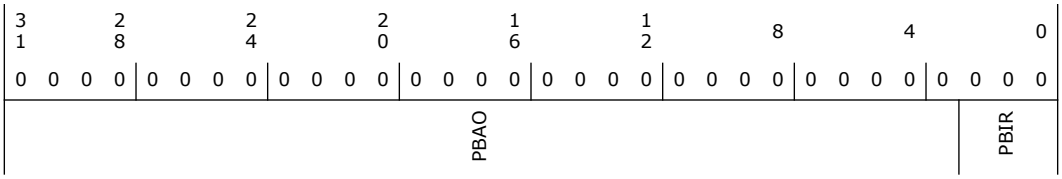
MSI-X PBA Offset / PBA BIR

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**PBA Offset (PBAO):** Used as an offset from the address contained by one of the function's Base Address registers to point to the base of the MSI-X PBA. The lower three PBA BIR bits are masked off (cleared to 000b) by software to form a 32-bit Qword-aligned offset.
2:0	0h RO	**PBA BIR (PBIR):** This field indicates which one of a function's Base Address registers, located beginning at 10h in Configuration Space, is used to map the function's MSI-X PBA into system memory. A read-only value of '1' means 14h.

17.1.37 BIST FIS Control/Status (BFCS)—Offset E0h

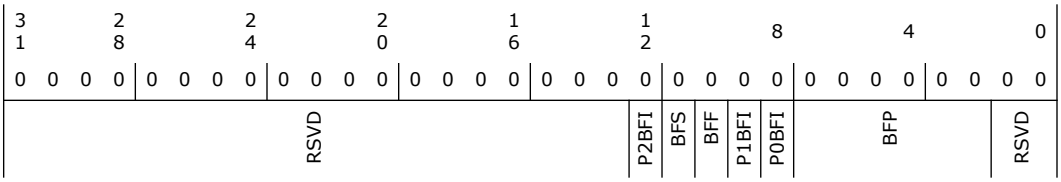
BIST FIS Control/Status

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	Reserved.
12	0h RW	**Port 2 BIST FIS Initiate (P2BFI):** When a rising edge is detected on this bit field, the PCH initiates a BIST FIS to the device on Port 2,using the parameters specified in this register and the data specified in BFTD1 and BFTD2. The BIST FIS will only be initiated if a device on Port 2 is present and ready (not partial/slumber state). After a BIST FIS is successfully completed, software must disable and re-enable the port using the PCS.P2E prior to attempting additional BIST FISes or to return the PCH to a normal operational mode. If the BIST FIS fails to complete, as indicated by the BFF bit in the register, then software can clear then set the P2BFI bit to initiate another BIST FIS. This can be retried until the BIST FIS eventually completes successfully. **Note:** Bit may be Reserved depending on if port is available in the given SKU. See Volume 1, Chapter 1 for details if port is available.
11	0h RW/1C	**BIST FIS Successful (BFS):** 0 = Software clears this bit by writing a 1 to it. 1 = This bit is set any time a BIST FIS transmitted by PCH receives an R_OK completion status from the device. **Note:** This bit must be cleared by software prior to initiating a BIST FIS.
10	0h RW/1C	**BIST FIS Failed (BFF):** 0 = Software clears this bit by writing a 1 to it. 1 = This bit is set any time a BIST FIS transmitted by PCH receives an R_ERR completion status from the device. **Note:** This bit must be cleared by software prior to initiating a BIST FIS.
9	0h RW	**Port 1 BIST FIS Initiate (P1BFI):** When a rising edge is detected on this bit field, the PCH initiates a BIST FIS to the device on Port 1,using the parameters specified in this register and the data specified in BFTD1 and BFTD2. The BIST FIS will only be initiated if a device on Port 1 is present and ready (not partial/slumber state). After a BIST FIS is successfully completed, software must disable and re-enable the port using the PCS.P1E prior to attempting additional BIST FISes or to return the PCH to a normal operational mode. If the BIST FIS fails to complete, as indicated by the BFF bit in the register, then software can clear then set the P1BFI bit to initiate another BIST FIS. This can be retried until the BIST FIS eventually completes successfully.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**Port 0 BIST FIS Initiate (P0BFI):** When a rising edge is detected on this bit field, the PCH initiates a BIST FIS to the device on Port 0,using the parameters specified in this register and the data specified in BFTD1 and BFTD2. The BIST FIS will only be initiated if a device on Port 0 is present and ready (not partial/slumber state). After a BIST FIS is successfully completed, software must disable and re-enable the port using the PCS.P0E prior to attempting additional BIST FISes or to return the PCH to a normal operational mode. If the BIST FIS fails to complete, as indicated by the BFF bit in the register, then software can clear then set the P0BFI bit to initiate another BIST FIS. This can be retried until the BIST FIS eventually completes successfully.
7:2	0h RW	**BIST FIS Parameters (BFP):** These 6 bits form the contents of the upper 6 bits of the BIST FIS Pattern Definition in any BIST FIS transmitted by the PCH. This field is not port specific— its contents will be used for any BIST FIS initiated on port 0, port 1, port 2, or port 3. The specific bit definitions are: Bit 7: T – Far End Transmit mode Bit 6: A – Align Bypass mode Bit 5: S – Bypass Scrambling Bit 4: L – Far End Retimed Loopback Bit 3: F – Far End Analog Loopback Bit 2: P – Primitive bit for use with Transmit mode
1:0	0h RO	Reserved.

17.1.38 BIST FIS Transmit Data 1 (BFTD1)—Offset E4h

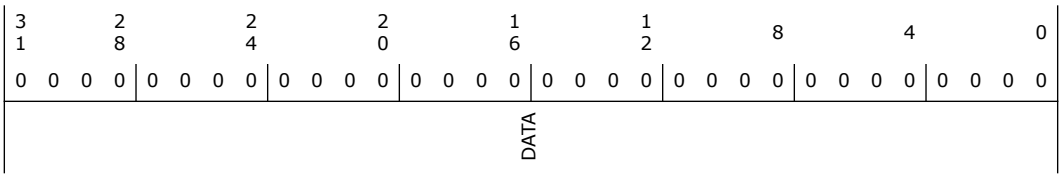
BIST FIS Transmit Data 1

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data (DATA):** The data programmed into this register will form the contents of the second DW of any BIST FIS initiated by the SATA controller. This register is not port specific - its contents will be used for BIST FIS initiated on any port. Although the 2nd and 3rd DWs of the BIST FIS are only meaningful when the T bit of the BIST FIS is set to indicate Far-End Transmit mode, this register's contents will be transmitted as the BIST FIS 2nd DW regardless of whether or not the T bit is indicated in the BFCS register.

17.1.39 BIST FIS Transmit Data 2 (BFTD2)—Offset E8h

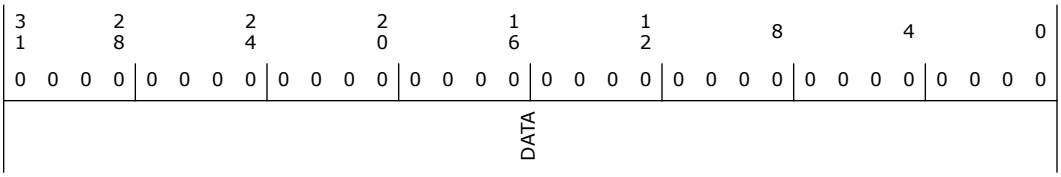
BIST FIS Transmit Data 2

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data (DATA):** The data programmed into this register will form the contents of the third DW of any BIST FIS initiated by the SATA controller. This register is not port specific - its contents will be used for BIST FIS initiated on any port. Although the 2nd and 3rd DWs of the BIST FIS are only meaningful when the T bit of the BIST FIS is set to indicate Far-End Transmit mode, this register's contents will be transmitted as the BIST FIS 3rd DW regardless of whether or not the T bit is set in the BFCS register.

17.2 SATA ABAR Registers Summary

Table 17-2. Summary of SATA ABAR Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	HBA Capabilities (GHC_CAP)—Offset 0h	FF34FF07h
4h	7h	Global HBA Control (GHC)—Offset 4h	80000000h
8h	Bh	Interrupt Status Register (IS)—Offset 8h	0h
Ch	Fh	Ports Implemented (GHC_PI)—Offset Ch	0h
10h	13h	AHCI Version (VS)—Offset 10h	10300h
1Ch	1Fh	Enclosure Management Location (EM_LOC)—Offset 1Ch	1600002h
20h	23h	Enclosure Management Control (EM_CTL)—Offset 20h	7010000h
24h	27h	HBA Capabilities Extended (GHC_CAP2)—Offset 24h	3Ch
A0h	A3h	Vendor Specific (VSP)—Offset A0h	48h
A4h	A7h	Vendor Specific Capabilities Register (VS_CAP)—Offset A4h	1002DEh
C0h	C3h	RAID Platform ID (RPID)—Offset C0h	311C02h
C4h	C5h	Premium Feature Block (PFB)—Offset C4h	0h
C8h	C9h	SW Feature Mask (SFM)—Offset C8h	3Fh
100h	103h	Port 0 Command List Base Address (P0CLB)—Offset 100h	0h
104h	107h	Port 0 Command List Base Address Upper 32-bits (P0CLBU)—Offset 104h	0h
108h	10Bh	Port 0 FIS Base Address (P0FB)—Offset 108h	0h
10Ch	10Fh	Port 0 FIS Base Address Upper 32-bits (P0FBU)—Offset 10Ch	0h
110h	113h	Port 0 Interrupt Status (P0IS)—Offset 110h	0h
114h	117h	Port 0 Interrupt Enable (P0IE)—Offset 114h	0h
118h	11Bh	Port 0 Command (P0CMD)—Offset 118h	4h
120h	123h	Port 0 Task File Data (P0TFD)—Offset 120h	9h
124h	127h	Port 0 Signature (P0SIG)—Offset 124h	FFFFFFFFh

Table 17-2. Summary of SATA ABAR Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
128h	12Bh	Port 0 Serial ATA Status (P0SSTS)—Offset 128h	0h
12Ch	12Fh	Port 0 Serial ATA Control (P0SCTL)—Offset 12Ch	0h
130h	133h	Port 0 Serial ATA Error (P0SERR)—Offset 130h	0h
134h	137h	Port 0 Serial ATA Active (P0SACT)—Offset 134h	0h
138h	13Bh	Port 0 Command Issue (P0CI)—Offset 138h	0h
144h	147h	Port 0 Device Sleep (P0DEVSLP)—Offset 144h	1E022852h
180h	183h	Port 1 Command List Base Address (P1CLB)—Offset 180h	0h
184h	187h	Port 1 Command List Base Address Upper 32-bits (P1CLBU)—Offset 184h	0h
188h	18Bh	Port 1 FIS Base Address (P1FB)—Offset 188h	0h
18Ch	18Fh	Port 1 FIS Base Address Upper 32-bits (P1FBU)—Offset 18Ch	0h
190h	193h	Port 1 Interrupt Status (P1IS)—Offset 190h	0h
194h	197h	Port 1 Interrupt Enable (P1IE)—Offset 194h	0h
198h	19Bh	Port 1 Command (P1CMD)—Offset 198h	0h
1A0h	1A3h	Port 1 Task File Data (P1TFD)—Offset 1A0h	0h
1A4h	1A7h	Port 1 Signature (P1SIG)—Offset 1A4h	0h
1A8h	1ABh	Port 1 Serial ATA Status (P1SSTS)—Offset 1A8h	0h
1ACh	1AFh	Port 1 Serial ATA Control (P1SCTL)—Offset 1ACh	0h
1B0h	1B3h	Port 1 Serial ATA Error (P1SERR)—Offset 1B0h	0h
1B4h	1B7h	Port 1 Serial ATA Active (P1SACT)—Offset 1B4h	0h
1B8h	1BBh	Port 1 Command Issue (P1CI)—Offset 1B8h	0h
1C4h	1C7h	Port 1 Device Sleep (P1DEVSLP)—Offset 1C4h	0h
200h	203h	Port 2 Command List Base Address (P2CLB)—Offset 200h	0h
204h	207h	Port 2 Command List Base Address Upper 32-bits (P2CLBU)—Offset 204h	0h
208h	20Bh	Port 2 FIS Base Address (P2FB)—Offset 208h	0h
20Ch	20Fh	Port 2 FIS Base Address Upper 32-bits (P2FBU)—Offset 20Ch	0h
210h	213h	Port 2 Interrupt Status (P2IS)—Offset 210h	0h
214h	217h	Port 2 Interrupt Enable (P2IE)—Offset 214h	0h
218h	21Bh	Port 2 Command (P2CMD)—Offset 218h	0h
220h	223h	Port 2 Task File Data (P2TFD)—Offset 220h	0h
224h	227h	Port 2 Signature (P2SIG)—Offset 224h	0h
228h	22Bh	Port 2 Serial ATA Status (P2SSTS)—Offset 228h	0h
22Ch	22Fh	Port 2 Serial ATA Control (P2SCTL)—Offset 22Ch	0h
230h	233h	Port 2 Serial ATA Error (P2SERR)—Offset 230h	0h
234h	237h	Port 2 Serial ATA Active (P2SACT)—Offset 234h	0h
238h	23Bh	Port 2 Command Issue (P2CI)—Offset 238h	0h
244h	247h	Port 2 Device Sleep (P2DEVSLP)—Offset 244h	0h

17.2.1 HBA Capabilities (GHC_CAP)—Offset 0h

HBA Capabilities. This register indicates basic capabilities of the HBA to driver software. The RWO bits in this register are only cleared upon PLTRST#. This register is not reset by FLR.

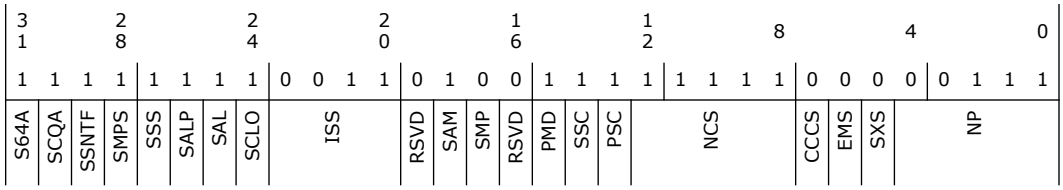
Access Method

Type: MEM Register (Size: 32 bits)

Device: 23

Function: 0

Default: FF34FF07h



Bit Range	Default & Access	Field Name (ID): Description
31	1h RW/O	**Supports 64-bit Addressing (S64A):** Indicates that the SATA controller can access 64-bit data structures. The 32-bit upper bits of the port DMA Descriptor, the PRD Base, and each PRD entry are read/write.
30	1h RW/O	**Supports Native Command Queuing Acceleration (SCQA):** When set to 1, indicates that the SATA controller supports SATA command queuing using the DMA Setup FIS. The PCH handles DMA Setup FISes natively, and can handle auto-activate optimization through that FIS.
29	1h RW/O	**Supports SNotification Register (SSNTF):** When set to 1, indicates the SATA controller supports the PxSNTF (SNotification) register and its associated functionality. When cleared to 0, the SATA controller does not support the PxSNTF (SNotification) register and its associated functionality.
28	1h RW/O	**Supports Mechanical Presence Switch (SMPS):** When set to 1, indicates whether the SATA controller supports mechanical presence switches on its ports for use in hot-plug operations. This value is loaded by platform BIOS prior to operating system initialization. If this bit is set, BIOS must also map the SATAGP pins to the SATA controller through GPIO space.
27	1h RW/O	**Supports Staggered Spin-up (SSS):** Indicates whether the SATA controller supports staggered spin-up on its ports, for use in balancing power spikes. This value is loaded by platform BIOS prior to OS initialization. 0 = Staggered spin-up not supported. 1 = Staggered spin-up supported.
26	1h RW/O	**Supports Aggressive Link Power Management (SALP):** 0 = Software shall treat the PxCMD.ALPE and PxCMD.ASP bits as reserved. 1 = The SATA controller supports auto-generating link requests to the partial or slumber states when there are no commands to process.
25	1h RW/O	**Supports Activity LED (SAL):** Indicates the SATA controller supports a single output pin (SATALED#) which indicates activity.
24	1h RW/O	**Supports Command List Override (SCLO):** When set to 1, indicates that the HBA supports the PxCMD.CLO bit and it's associated function. When cleared to 0., The HBA is not capable of clearing the BSY and DRQ bits in the Status register in order to issue a software reset if these bits are still set from a previous operation.

Bit Range	Default & Access	Field Name (ID): Description
23:20	3h RW/O	**Interface Speed Support (ISS):** Indicates the maximum speed the SATA controller can support on its ports. 1h = 1.5Gb/s 2h = 3Gb/s 3h = 6Gb/s The default of this field is dependent upon the PCH SKU. If at least one PCH SATA port supports 6Gb/s, the default will be 3h. If no PCH SATA ports support 6Gb/s, then the default will be 2h and writes of 3h will be ignored by the PCH. Refer to Volume 1, Chapter 1 for details on 6Gb/s port availability.
19	0h RO	Reserved.
18	1h RO	**Supports AHCI mode only (SAM):** The SATA controller may optionally support AHCI access mechanism only. 0 = SATA controller supports both IDE and AHCI Modes 1 = SATA controller supports AHCI Mode Only **Note:** BIOS should program this field as "1" since IDE mode is not supported.
17	0h RO	**Supports Port Multiplier (SMP):** Not supported.
16	0h RO	Reserved.
15	1h RO	**PIO Multiple DRQ Block (PMD):** Hardwired to 1. The SATA controller supports PIO Multiple DRQ Command Block.
14	1h RW/O	**Slumber State Capable (SSC):** When set to 1, the SATA controller supports the slumber state.
13	1h RW/O	**Partial State Capable (PSC):** When set to 1, the SATA controller supports the partial state.
12:8	1Fh RO	**Number of Command Slots (NCS):** Hardwired to 1Fh to indicate support for 32 slots.
7	0h RO	**Command Completion Coalescing Supported (CCCS):** 0 = Command Completion Coalescing Not Supported 1 = Command Completion Coalescing Supported
6	0h RO	**Enclosure Management Supported (EMS):** 0 = Enclosure Management Not Supported 1 = Enclosure Management Supported
5	0h RW/O	**Supports External SATA (SXS):** 0 = External SATA is not supported on any ports 1 = External SATA is supported on one or more ports When set, software can examine each SATA port's Command register (PxCMD.ESP) to determine which port is routed externally.
4:0	7h RO	**Number of Ports (NP):** Indicates number of supported ports. The number of ports indicated in this field may be more than the number of ports indicated in the PI (ABAR + 0Ch) register. Field value dependent on number of ports available in a given SKU.

17.2.2 Global HBA Control (GHC)—Offset 4h

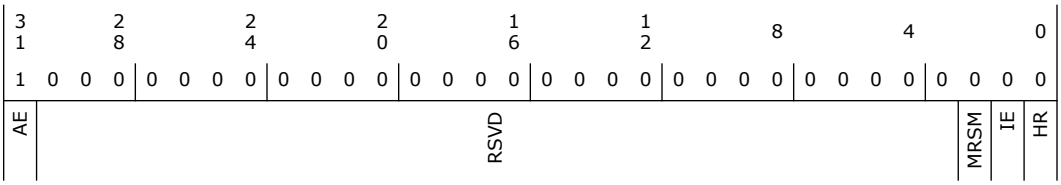
Global HBA Control. This register controls various global actions of the HBA.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 80000000h



Bit Range	Default & Access	Field Name (ID): Description
31	1h RO	**AHCI Enable (AE):** When set, indicates that an AHCI driver is loaded and communication to the HBA shall be via AHCI mechanisms. This can be used by an HBA that supports both legacy mechanisms (such as SFF-8038i) and AHCI to know when the HBA is running under an AHCI driver. 0 = Software will only communicate with the HBA using legacy mechanisms. 1 = Software shall only talk to the HBA using AHCI. The HBA will not have to allow command processing via both AHCI and legacy mechanisms. **Note:** Software shall set this bit to 1 before accessing other AHCI registers. **Note:** The implementation of this bit is dependent upon the value of the CAP.SAM bit. If CAP.SAM is '0', then GHC.AE should be RW and shall have a reset value of '0'. If CAP.SAM is '1', then GHC.AE shall be read only and shall have a reset value of '1'.
30:3	0h RO	Reserved.
2	0h RO	**MSI Revert to Single Message (MRSM):** When set to 1 by hardware, indicates that the HBA requested more than one MSI vector but has reverted to using the first vector only. When this bit is cleared to 0, the HBA has not reverted to single MSI mode (i.e. hardware is already in single MSI mode, software has allocated the number of messages requested, or hardware is sharing interrupt vectors if MC.MME < MC.MMC). The HBA may revert to single MSI mode when the number of vectors allocated by the host is less than the number requested. This bit shall only be set to 1 when the following conditions hold: MC.MSIE = 1 (MSI is enabled) MC.MMC > 0 (multiple messages requested) MC.MME > 0 (more than one message allocated) MC.MME != MC.MMC (messages allocated not equal to number requested) When this bit is set to 1, single MSI mode operation is in use and software is responsible for clearing bits in the IS register to clear interrupts. This bit shall be cleared to 0 by hardware when any of the four conditions stated is false. This bit is also cleared to 0 when MC.MSIE = 1 and MC.MME = 0h. In this case, the hardware has been programmed to use single MSI mode, and is not reverting to that mode. For PCH, the HBA shall always revert to single MSI mode when the number of vectors allocated by the host is leass than the number requested. Value of MRSM is a don't care when GHC.HR=1.
1	0h RW	**Interrupt Enable (IE):** This global bit enables interrupts from the PCH. 0 = All interrupt sources from all ports are disabled. 1 = Interrupts are allowed from the AHCI controller.
0	0h RW/1S	**HBA Reset (HR):** Resets the PCH AHCI controller. 0 = No effect 1 = When set by software, this bit causes an internal reset of the PCH AHCI controller. All state machines that relate to data transfers and queuing return to an idle condition, and all ports are re-initialized using COMRESET. **Note:** For further details, refer to Section 10.4.3 of the Serial ATA Advanced Host Controller Interface specification, revision 1.3.

17.2.3 Interrupt Status Register (IS)—Offset 8h

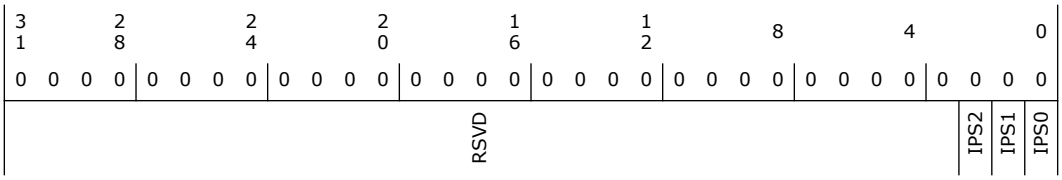
Interrupt Status Register. This register indicates which of the ports within the controller have an interrupt pending and require service.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	Reserved.
2	0h RW/1C	**Interrupt Pending Status Port 2 (IPS2):** This bit is only applicable to system that has Port 2 physically. 0 = No interrupt pending. 1 = Port 2 has an interrupt pending. Software can use this information to determine which ports require service after an interrupt.
1	0h RW/1C	**Interrupt Pending Status Port 1 (IPS1):** This bit is only applicable to system that has Port 1 physically. 0 = No interrupt pending. 1 = Port 1 has an interrupt pending. Software can use this information to determine which ports require service after an interrupt.
0	0h RW/1C	**Interrupt Pending Status Port 0 (IPS0):** This bit is only applicable to system that has Port 0 physically. 0 = No interrupt pending. 1 = Port 0 has an interrupt pending. Software can use this information to determine which ports require service after an interrupt.

17.2.4 Ports Implemented (GHC_PI)—Offset Ch

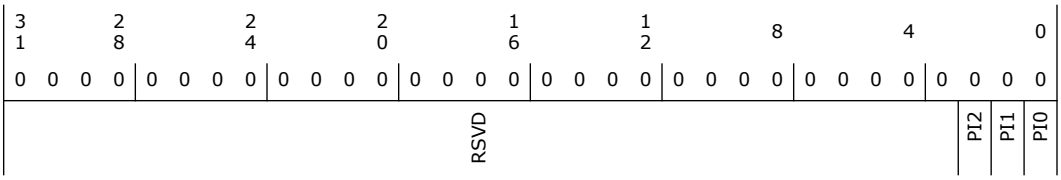
Ports Implemented. This register indicates which ports are exposed to the HBA. It is loaded by platform BIOS. It indicates which ports that the device supports are available for software to use. Any available port may not be implemented. This register is not reset by FLR. There is BIOS programming requirement on the PI register. Please refer to section 7.9.13.1.1 for details.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	Reserved.
2	0h RW/O	**Port 2 Implemented (PI2):** 0 = The port is not implemented. 1 = The port is implemented. **Note:** This bit may be Reserved and is RO '0' depending on if port is available in the given SKU. Refer to Volume 1, Chapter 1 for details if port is available.
1	0h RW/O	**Port 1 Implemented (PI1):** 0 = The port is not implemented. 1 = The port is implemented.
0	0h RW/O	**Port 0 Implemented (PI0):** 0 = The port is not implemented. 1 = The port is implemented.

17.2.5 AHCI Version (VS)—Offset 10h

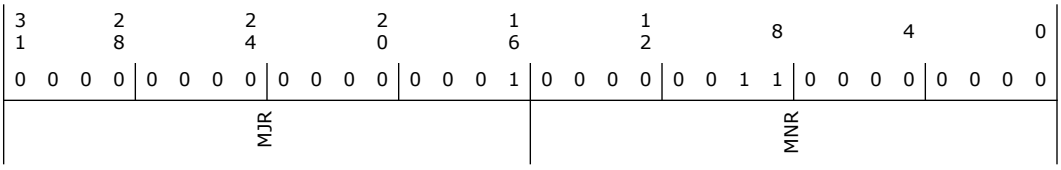
AHCI Version. This register indicates the major and minor version of the AHCI specification. It is BCD encoded. The upper two bytes represent the major version number, and the lower two bytes represent the minor version number. Example: Version 3.12 would be represented as 00030102h.

Access Method

Type: MEM Register (Size: 32 bits)

Device: 23
Function: 0

Default: 10300h



Bit Range	Default & Access	Field Name (ID): Description
31:16	1h RO	**Major Version Number (MJR):** Indicates the major version is 1
15:0	300h RO	**Minor Version Number (MNR):** Indicates the minor version is 30

17.2.6 Enclosure Management Location (EM_LOC)—Offset 1Ch

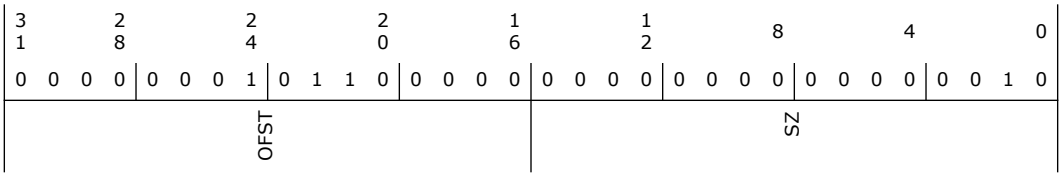
Enclosure Management Location. The enclosure management location register identifies the location and size of the enclosure management message buffer. This register is not implemented if enclosure management is not supported (i.e. CAP.EMS = 0).

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 1600002h



Bit Range	Default & Access	Field Name (ID): Description
31:16	160h RO	**Offset (OFST):** The offset of the message buffer in Dwords from the beginning of the ABAR.
15:0	2h RO	**Buffer Size (SZ):** Specifies the size of the transmit message buffer area in Dwords. If both transmit and receive buffers are supported, then the transmit buffer begins at ABAR[EM_LOC.OFST*4] and the receive buffer directly follows it. If both transmit and receive buffers are supported, both buffers are of the size indicated in the Buffer Size field. A value of 0 is invalid. Note that SATA controller only supports transmit buffer.

17.2.7 Enclosure Management Control (EM_CTL)—Offset 20h

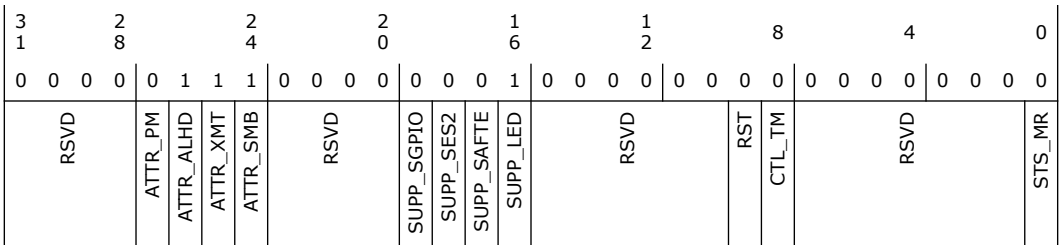
Enclosure Management Control. This register is used to control and obtain status for the enclosure management interface. The register includles information on the attributes of the implementation, enclosure management messages supported, the status of the interface, whether any messages are pending, and is used to initiate sending messages. This register is not implemented if enclosure management is not supported (i.e. CAP.EMS = 0).

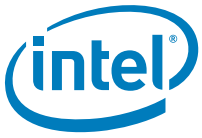
Access Method

Type: MEM Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 7010000h





Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	Reserved.
27	0h RO	**Port Multiplier Support (ATTR_PM):** The HBA does not support enclosure management messages for devices attached via a Port Multiplier. Software should use the Serial ATA enclosure management bridge that is built into many Port Multipliers for enclosure services with these devices. For more information on Serial ATA enclosure management bridges, refer to the Serial ATA II: Extensions to Serial ATA 1.0a revision 1.2 specification.
26	1h RW/O	**Activity LED Hardware Driven (ATTR_ALHD):** If set to 1, the HBA drives the activity LED for the LED message type in hardware and does not utilize software settings for this LED. The HBA does not begin transmitting the hardware based activity signal until after software has written CTL.TM=1 after a reset condition.
25	1h RO	**Transmit Only (ATTR_XMT):** If set to 1, the HBA only supports transmitting messages and does not support receiving messages. If cleared to 0, the HBA supports transmitting and receiving messages.
24	1h RO	**Single Message Buffer (ATTR_SMB):** If set to 1, the HBA has one message buffer that is shared for messages to transmit and messages received. In this case, unsolicited receive messages are not supported and it is software's responsibility to manage access to this buffer. If cleared to 0, there are separate receive and transmit buffers such that unsolicited messages could be supported.
23:20	0h RO	Reserved.
19	0h RO	**SGPIO Enclosure Management Messages (SUPP_SGPIO):** If set to 1, the HBA supports the SGPIO register interface message type.
18	0h RO	**SES-2 Enclosure Management Messages (SUPP_SES2):** If set to 1, the HBA supports the SES-2 message type.
17	0h RO	**SAF-TE Enclosure Management Messages (SUPP_SAFTE):** If set to 1, the HBA supports the SAF-TE message type.
16	1h RO	**LED Message Types (SUPP_LED):** If set to 1, the HBA supports the LED message type defined in LED Message Type.
15:10	0h RO	Reserved.
9	0h RW/1S	**Reset (RST):** When set to 1 by software, the HBA shall reset all enclosure management message logic and take all appropriate reset actions to ensure messages can be transmitted/received after the reset. After the HBA completes the reset operation, the HBA shall set the value to 0. A write of 0 by software to this field shall have no effect.
8	0h RW/1S	**Transmit Message (CTL_TM):** When set to 1 by software, the HBA shall transmit the message contained in the message buffer. When the message is completely sent, the HBA shall clear this bit to 0. A write of 0 to this bit by software shall have no effect. Software shall not change the contents of the message buffer while CTL.TM is set to 1.
7:1	0h RO	Reserved.
0	0h RO	**Message Received (STS_MR):** Message received is not supported.

17.2.8 HBA Capabilities Extended (GHC_CAP2)—Offset 24h

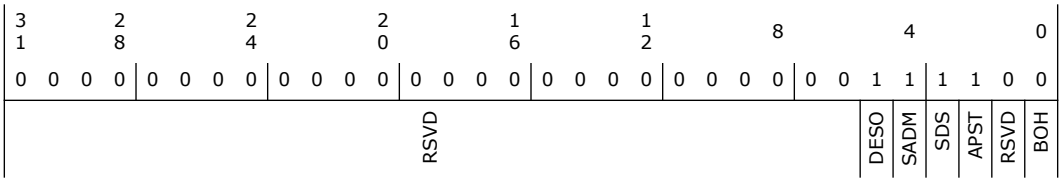
HBA Capabilities Extended. This register indicates basic capabilities of the HBA to driver software. The RWO bits in this register are only cleared upon PLTRST#. This register is not reset by FLR.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 3Ch



Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	Reserved.
5	1h RW/O	**DEVSLP Entrance from Slumber Only (DESO):** This bit specifies that the HBA shall only assert DEVSLP if the interface is in Slumber. 0 = The host may enter DEVSLP from any link state (Active, Partial, or Slumber) 1 = The host shall ignore software direct entrance to DEVSLP by means of PxCMD.ICC bit unless PxSSTS.IPM = 6h.
4	1h RW/O	**Supports Aggressive DEVSLP Management (SADM):** 0 = Aggressive DEVSLP Management is not supported and software will treat the PxDEVSLP.ADSE field as reserved. 1 = The host supports hardware assertion of the DEVSLP signal after the idle timeout expires.
3	1h RW/O	**Supports DEVSLP (SDS):** 0 = DEVSLP is not supported 1 = DEVSLP is supported
2	1h RW/O	**Automatic Partial to Slumber Transitions (APST):** 0 = Automatic Partial to Slumber Transition is not supported. 1 = Supports Automatic Partial to Slumber Transitions.
1	0h RO	Reserved.
0	0h RO	**BIOS/OS Handoff (BOH):** Not supported.

17.2.9 Vendor Specific (VSP)—Offset A0h

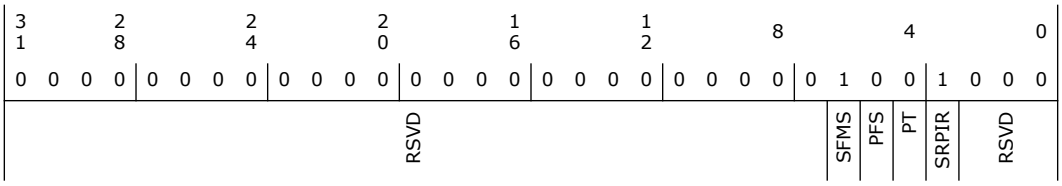
Vendor Specific

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 48h



Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	Reserved.
6	1h RO	**Software Feature Mask Supported (SFMS):** Set to 1 if the platform is enabled for premium storage features mask (SFM) as described in VS MMIO space at offset ABAR[RPID.(OFST*4)+4].
5	0h RO	**Premium Features Supported (PFS):** Set to 1 if the platform is enabled for premium storage features (PFB) as described in VS MMIO space at offset ABAR[RPID.OFST*4]. Set to 0 if the platform is not enabled for premium storage features.
4	0h RO	**Platform Type (PT):** Set to 1 if mobile platform. Clear (0) if desktop.
3	1h RO	**Supports RAID Platform ID Reporting (SRPIR):** If set to 1, then indicates that the RAID Platform ID is reported via ABAR + C0h. Set to 0 if this ID is not reported via MMIO space.
2:0	0h RO	Reserved.

17.2.10 Vendor Specific Capabilities Register (VS_CAP)—Offset A4h

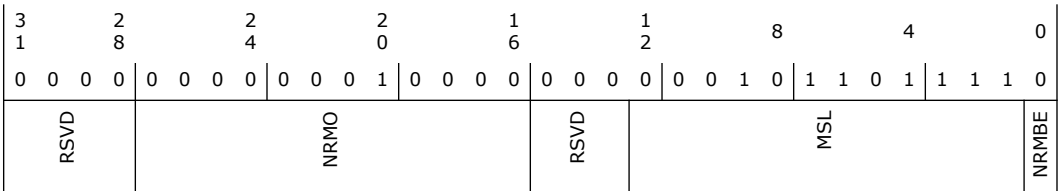
Vendor Specific Capabilities Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 1002DEh



Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	Reserved.
27:16	10h RW/O	**NVM Remapped Register Offset (NRMO):** Specifies the offset (in 128B unit) within ABAR as to where the PCIe NAND memory BAR register space is remapped. For example, NRMO=1 means ABAR + 128B. This allows the remapped offset to shift between ABAR + 0B, and ABAR + 512KK - 128B, with 128B step. The remapped offset into the AHCI memory space must not overlap with the memory space used for SATA. The remapped offset into the AHCI memory space and the remapped size must not exceed the allocated AHCI memory space of the integrated AHCI controller. Only valid when NRMBE = 1. The reset default of this field is 10h, this places the start of the PCIe NAND memory BAR register space at ABAR + 2K. This field is not reset by FLR.

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO	Reserved.
12:1	16Fh RW/O	**Memory Space Limit. (MSL):** This field specifies the size (in 128B unit) of the remapped memory space for the PCIe NAND device. It is a 0-based field. For example, MSL=1 means 256B. This allows the remapped size to shift between 128B and 512K with the step of 128B.Memory BAR offset from 0 to MSL of the PCIe NAND device are remapped under the integrated AHCI controller memory space.The remapped offset into the AHCI memory space and the value programmed in this field must not exceed the allocated AHCI memory space of the integrated AHCI controller. Only valid when NRMBE = 1. The reset default of this field is 16Fh which specifies the size of the remapped memory space as 34k.This field is not reset by FLR.
0	0h RW/O	**PCIe NAND Memory BAR Remapped Enable (NRMBE):** Set to 1 if a PCIe NAND device is present and remapping of its memory BAR register space is enabled. Cleared to 0 if there is no PCIe NAND device present or the remapping of its memory BAR register space is disabled. This bit is not reset by FLR.

17.2.11 RAID Platform ID (RPID)—Offset C0h

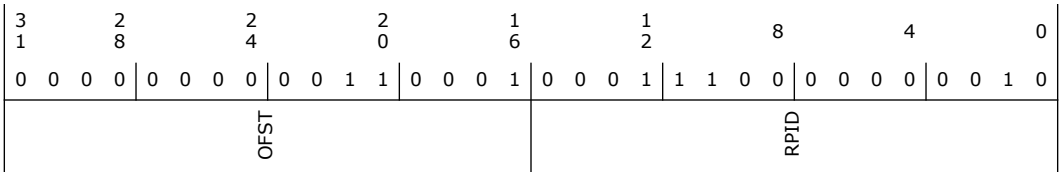
RAID Platform ID. This register is used by the Intel Matrix Storage Manager OROM to match the features supported by the OROM with the platform on which the OROM is executing. This prevents the use of an OROM designed for newer chipsets from being use on older chipsets as this could reduce up-sell potential.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 311C02h



Bit Range	Default & Access	Field Name (ID): Description
31:16	31h RO	**Offset (OFST):** The offset of the Premium Feature Block (PFB) in DWords from the beginning of the ABAR. SFM follows directly after PFB.
15:0	1C02h RO	**RAID Platform ID (RPID):** Specifies the DID value that has been assigned to the platform. This is the same DID that is reported by the SATA controller when SATAGC.AIE is set to 1 except that the DID is always reported through this register, regardless if the programming of SATAGC.AIE.

17.2.12 Premium Feature Block (PFB)—Offset C4h

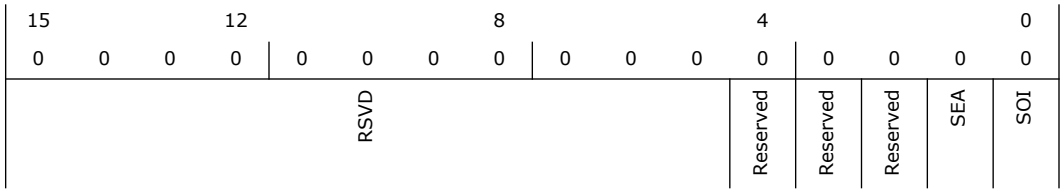
Premium Feature Block. Note: Bits 4-0 are not bit-mapped to individual fuses and/or soft SKU settings; rather a single fuse FFSATA5& FFSATA 3 /soft sku is used to indicate support for all of these features (refer to VSP.PFS). These registers indicate to the Intel Rapid Storage Technology AHCI driver that those premium RAID features that can be supported on the platform.

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 23
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:5	0h RO	Reserved.
4	0h RO	**Reserved (Reserved):** Read value is the same as VSP.PFS.
3	0h RO	**Reserved (Reserved):** Read value is the same as VSP.PFS.
2	0h RO	**Reserved (Reserved):** Read value is the same as VSP.PFS.
1	0h RO	**Supports Email Alert (SEA):** Read value is the same as VSP.PFS. If set to 1, then this feature is supported as part of the premium feature set.
0	0h RO	**Supports OEM IOCTL (SOI):** Read value is the same as VSP.PFS. If set to 1, then this feature is supported as part of the premium feature set.

17.2.13 SW Feature Mask (SFM)—Offset C8h

SW Feature Mask. The following will be programmed by the BIOS when VS_CAP.SFMS == 1. The feature mask is used by SW to determine which non-premium features shall be supported by SW. These register bits are not reset by FLR since they are programmed by BIOS.

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 23
Function: 0

Default: 3Fh

15			12			8				4							0
0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
RSVD				OROM_UI_Normal_Delay		Smart_Response_Technology	IRRT_Only_on_ESATA	LED_Locate	HDDUNLOCK	OROM_UI_and_BANNER	IRRT	R5	R10	R1	R0		

Bit Range	Default & Access	Field Name (ID): Description
15:12	0h RO	Reserved.
11:10	0h RW/O	**OROM UI Normal Delay. (OROM_UI_Normal_Delay):** Values of these bits specify the delay of the OROM UI Splash Screen in a normal status. 00 = 2 secs (default and previous value); 01 = 4 secs; 10 = 6 secs; 11 = 8 secs. If bit 5 == 0, then these values are disregarded.
9	0h RW/O	**Smart Response Technology. (Smart_Response_Technology):** If set to '1', then Smart Response Technology is enabled. If cleared to '0', the feature is disabled.
8	0h RW/O	**RRT Only on ESATA (IRRT_Only_on_ESATA):** If set to 1, then only RRT volumes can span internal and external SATA ports (e.g. eSATA). If cleared to 0, then any RAID volume can span internal and external SATA ports (e.g. eSATA).
7	0h RW/O	**LED Locate (LED_Locate):** If set to 1, then LED/SGPIO hardware is attached and the ping to locate feature is enabled in the OS.
6	0h RW/O	**HDDUNLOCK (HDDUNLOCK):** If set to 1, then HDD password unlock is enabled in the OS.
5	1h RW/O	**OROM UI and BANNER (OROM_UI_and_BANNER):** If set to 1, then the OROM UI is displayed. When cleared to 0, the OROM UI and BANNER are not displayed if all disks and volumes have a normal status.
4	1h RW/O	**RRT (IRRT):** If set to 1, then Rapid Recovery Technology is enabled.
3	1h RW/O	**R5 (R5):** If set to 1, then RAID5 is enabled
2	1h RW/O	**R10 (R10):** If set to 1, then RAID10 is enabled
1	1h RW/O	**R1 (R1):** If set to 1, then RAID1 is enabled
0	1h RW/O	**R0 (R0):** If set to 1, then RAID0 is enabled

17.2.14 Port 0 Command List Base Address (P0CLB)—Offset 100h

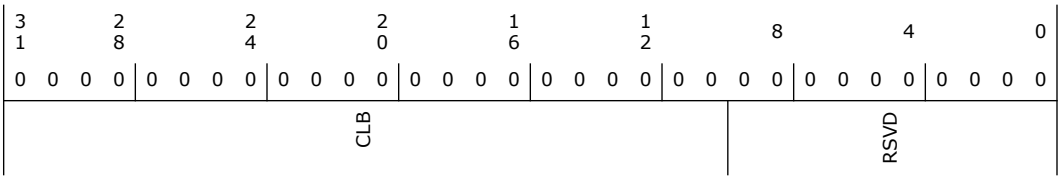
Port 0 Command List Base Address

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RW	**Command List Base Address (CLB):** Indicates the 32-bit base for the command list for this port. This base is used when fetching commands to execute. This address must be 1K aligned as indicated by bits 31:10 being read/write. Note that these bits are not reset on a HBA reset.
9:0	0h RO	Reserved.

17.2.15 Port 0 Command List Base Address Upper 32-bits (P0CLBU)—Offset 104h

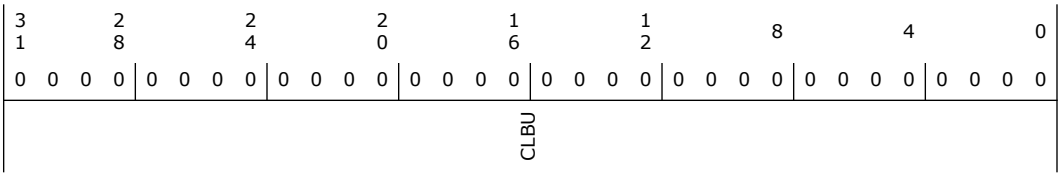
Port 0 Command List Base Address Upper 32-bits

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Command List Base Address Upper (CLBU):** Indicates the upper 32-bits for the command list base address for this port. This base is used when fetching commands to execute. Note that these bits are not reset on a HBA reset.

17.2.16 Port 0 FIS Base Address (P0FB)—Offset 108h

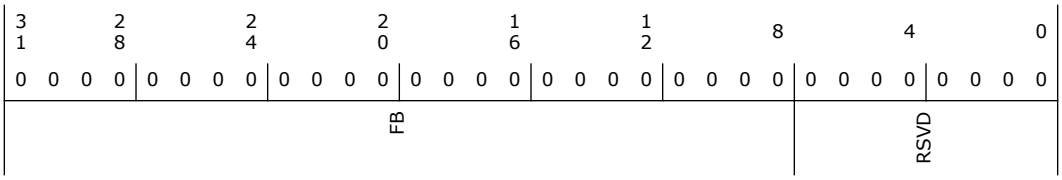
Port 0 FIS Base Address

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RW	**FIS Base Address (FB):** Indicates the 32-bit base for received FISes. This address must be 256-byte aligned as indicated by bits 31:08 being read/write. When FIS-based switching is in use, this structure is 4KB in length and the address shall be 4KB aligned. Note that these bits are not reset on a HBA reset.
7:0	0h RO	Reserved.

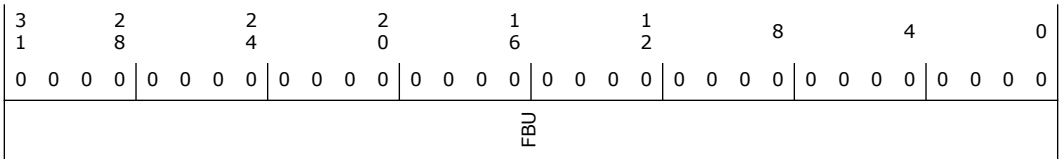
17.2.17 Port 0 FIS Base Address Upper 32-bits (P0FBU)—Offset 10Ch

Port 0 FIS Base Address Upper 32-bits

Access Method

Type: MEM Register (Size: 32 bits)
Device: 23
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**FIS Base Address Upper (FBU):** Indicates the upper 32-bits for the received FIS base for this port. Note that these bits are not reset on a HBA reset.

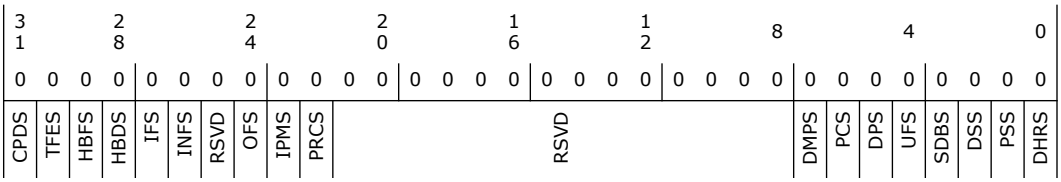
17.2.18 Port 0 Interrupt Status (P0IS)—Offset 110h

Port 0 Interrupt Status

Access Method

Type: MEM Register (Size: 32 bits)
Device: 23
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Cold Presence Detect Status (CPDS):** The SATA controller does not support cold presence detect.
30	0h RW/1C	**Task File Error Status (TFES):** This bit is set whenever the status register is updated by the device and the error bit (bit 0 of the Status field in the received FIS) is set.
29	0h RW/1C	**Host Bus Fatal Error Status (HBFS):** Indicates that the HBA encountered a host bus error that it cannot recover from, such as a bad software pointer. In PCI, such an indication would be a target or master abort.
28	0h RW/1C	**Host Bus Data Error Status (HBDS):** Indicates that the HBA encountered a data error (uncorrectable ECC / parity) when reading from or writing to system memory.
27	0h RW/1C	**Interface Fatal Error Status (IFS):** Indicates that the HBA encountered an error on the SATA interface which caused the transfer to stop.
26	0h RW/1C	**Interface Non-fatal Error Status (INFS):** Indicates that the HBA encountered an error on the SATA interface but was able to continue operation.
25	0h RO	Reserved.
24	0h RW/1C	**Overflow Status (OFS):** Indicates that the HBA received more bytes from a device than was specified in the PRD table for the command.
23	0h RW/1C	**Incorrect Port Multiplier Status (IPMS):** Indicates that the HBA received a FIS from a device whose port multiplier field did not match what was expected. The IPMS bit may be set during emuneration process. It is recommended that IPMS only be used after enumeration is complete on the Port Multiplier.
22	0h RO	**PhyRdy Change Status (PRCS):** When set to one indicates the internal PhyRdy signal changed state. This bit reflects the state of PxSERR.DIAG.N. This bit is RO and is only cleared when PxSERR.DIAG.N is cleared.
21:8	0h RO	Reserved.
7	0h RW/1C	**Device Mechanical Presence Status (DMPS):** When set, indicates that a platform mechanical presence switch has been opened or closed, which may lead to a change in the connection state of the device. This bit is only valid in systems that support mechanical presence switch (CAP.SMPS and PxCMD.MPSP are set).
6	0h RO	**Port Connect Change Status (PCS):** This bit reflects the state of PxSERR.DIAG.X. This bit is only cleared when PxSERR.DIAG.X is cleared. 1 = Change in Current Connect Status. 0 = No change in Current Connect Status.
5	0h RW/1C	**Descriptor Processed (DPS):** A PRD with the I. bit set has transferred all of its data.
4	0h RO	**Unknown FIS Interrupt (UFS):** When set to 1 indicates that an unknown FIS was received and has been copied into system memory. This bit is cleared to 0 by software clearing the PxSERR.DIAG.F bit to 0. Note that this bit does not directly reflect the PxSERR.DIAG.F bit. PxSERR.DIAG.F is set immediately when an unknown FIS is detected, whereas this bit is set when the FIS is posted to memory. Software should wait to act on an unknown FIS until this bit is set to 1 or the two bits may become out of sync.
3	0h RW/1C	**Set Device Bits Interrupt (SDBS):** A Set Device Bits FIS has been received with the I. bit set and has been copied into system memory.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1C	**DMA Setup FIS Interrupt (DSS):** A DMA Setup FIS has been received with the I. bit set and has been copied into system memory.
1	0h RW/1C	**PIO Setup FIS Interrupt (PSS):** A PIO Setup FIS has been received with the I. bit set, it has been copied into system memory, and the data related to that FIS has been transferred. This bit shall be set even if the data transfer resulted in an error.
0	0h RW/1C	**Device to Host Register FIS Interrupt (DHRS):** A D2H register FIS has been received with the I. bit set, and has been copied into system memory.

17.2.19 Port 0 Interrupt Enable (P0IE)—Offset 114h

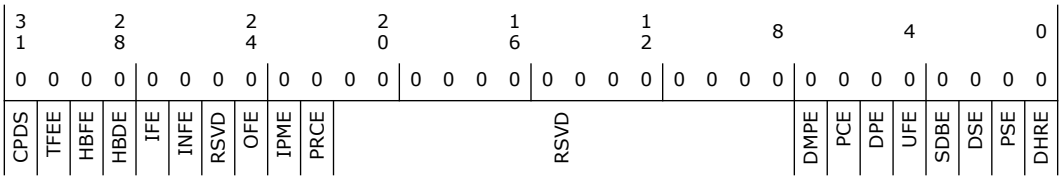
Port 0 Interrupt Enable

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Cold Presence Detect Enable (CPDS):** The SATA controller does not support cold presence detect.
30	0h RW	**Task File Error Enable (TFEE):** When set, GHC.IE is set, and P0S.TFES is set, the HBA shall generate an interrupt.
29	0h RW	**Host Bus Fatal Error Enable (HBFE):** When set, GHC.IE is set, and P0IS.HBFS is set, the HBA shall generate an interrupt.
28	0h RW	**Host Bus Data Error Enable (HBDE):** When set, GHC.IE is set, and P0IS.HBDS is set, the HBA shall generate an interrupt.
27	0h RW	**Interface Fatal Error Enable (IFE):** When set, GHC.IE is set, and P0IS.IFS is set, the HBA shall generate an interrupt.
26	0h RW	**Interface Non-fatal Error Enable (INFE):** When set, GHC.IE is set, and P0IS.INFS is set, the HBA shall generate an interrupt.
25	0h RO	Reserved.
24	0h RW	**Overflow Enable (OFE):** When set, and GHC.IE and P0IS.OFS are set, the HBA shall generate an interupt.
23	0h RW	**Incorrect Port Multiplier Enable (IPME):** When set, and GHC.IE and P0IS.IPMS are set, the HBA shall generate an interupt. BIOS is required to program this field to '0'. The same applies to AHCI driver.
22	0h RW	**PhyRdy Change Interrupt Enable (PRCE):** When set, and GHC.IE is set, and PxIS.PRCS is set, the HBA shall generate an interrupt.

Bit Range	Default & Access	Field Name (ID): Description
21:8	0h RO	Reserved.
7	0h RW	**Device Mechanical Enable (DMPE):** When set, and P0IS.DMPS is set, the HBA shall generate an interrupt.
6	0h RW	**Port Change Interrupt Enable (PCE):** When set, GHC.IE is set, and P0IS.PCS is set, the HBA shall generate an interrupt.
5	0h RW	**Descriptor Processed Interrupt Enable (DPE):** When set, GHC.IE is set, and P0IS.DPS is set, the HBA shall generate an interrupt.
4	0h RW	**Unknown FIS Interrupt Enable (UFE):** When set, GHC.IE is set, and PxIS.UFS is set to 1, the HBA shall generate an interrupt.
3	0h RW	**Set Device Bits FIS Interrupt Enable (SDBE):** When set, GHC.IE is set, and P0IS.SDBS is set, the HBA shall generate an interrupt.
2	0h RW	**DMA Setup FIS Interrupt Enable (DSE):** When set, GHC.IE is set, and P0IS.DSS is set, the HBA shall generate an interrupt.
1	0h RW	**PIO Setup FIS Interrupt Enable (PSE):** When set, GHC.IE is set, and P0IS.PSS is set, the HBA shall generate an interrupt.
0	0h RW	**Device to Host Register FIS Interrupt Enable (DHRE):** When set, GHC.IE is set, and P0IS.DHRS is set, the HBA shall generate an interrupt.

17.2.20 Port 0 Command (P0CMD)—Offset 118h

Port 0 Command

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 4h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
ICC				ASP	ALPE	DLAE	ATAPI	APSTE	FBSCP	ESP	CPD	MPSP	HPCP	PMA	RSVD	CR	FR	MPSS	CCS				RSVD	PSP	RSVD	FRE	CLO	POD	SUD	ST		

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RW	**Interface Communication Control (ICC):** This is a four bit field which can be used to control reset and power states of the interface. Writes to this field will cause actions on the interface, either as primitives or an OOB sequence, and the resulting status of the interface will be reported in the PxSSTS register. **Value** — **Definition** Fh–9h — Reserved 8 — DEVSLP: This will cause the PCH to assert the DEVSLP signal associated with the port. The PCH will ignore the DEVSLP idle timeout value that is specified by PxDEVSLP.DITO. Software will only request DEVSLP when the interface is in an idle state (that is, PxCI is cleared to 0h and PxSACT is cleared to 0h). If the interface is not idle at the time this register is written, then the PCH will take no action and the interface will remain in its current state. If PxCAP2.DESO is set to '1' and PxSSTS.IPM is not set to '6h', then the host will take no action on the interface and will remain in its current state. Additionally, the HBA shall not assert the DEVSLP signal until PHYRDY has been achieved (after a previous de-assertion). 7 — Reserved 6h — Slumber: This will cause the PCH to request a transition of the interface to the slumber state. The SATA device may reject the request and the interface will remain in its current state. 5h–3h — Reserved 2h — Partial: This will cause the PCH to request a transition of the interface to the partial state. The SATA device may reject the request and the interface will remain in its current state. 1h — Active: This will cause the PCH to request a transition of the interface into the active state. If the requested transition is from the DEVSLP state, then the host controller shall wait until PxDEVSLP.DMAT has expired before deasserting the DEVSLP Signal. 0h — No-Op/Idle: When software reads this value, it indicates the PCH is not in the process of changing the interface state or sending a device reset, and a new link command may be issued. When system software writes a non-reserved value other than No-Op (0h), the HBA shall perform the action and update this field back to Idle (0h). If software writes to this field to change the state to a state the link is already in (i.e. interface is in the active state and a request is made to go to the active state), the HBA shall take no action and return this field to Idle. If the interface is in a low power state and the software wants to transition to a different low power state, software must first bring the link to active and then initiate the transition to the desired low power state (with the exception of DEVSLP). The transition to DEVSLP may occur from any other state if CAP2.DESO is cleared to '0'. If CAP2.DESO is set to '1', then DEVSLP may only be transitioned to if the link is in Slumber.
27	0h RW	**Aggressive Slumber Partial (ASP):** When set to 1, and the ALPE bit is set, the HBA shall aggressively enter the Slumber state when it clears a bit in the PxCI or PxSACT register and the register values are then PxCI = 0h and PxSACT = 0h. When cleared, and the ALPE bit is set, the HBA will aggressively enter the Partial state when it clears a bit in the PxCI or PxSACT register and the register values are then PxCI = 0h and PxSACT = 0h. If CAP.SALP is cleard to 0., software shall treat this bit as reserved.
26	0h RW	**Aggressive Link Power Management Enable (ALPE):** When set, the HBA will aggressively enter a lower link power state (Partial or Slumber) based upon the setting of the ASP bit. Software shall only set this bit to 1 if CAP.SALP is set to 1. If CAP.SALP is cleared to 0, software shall treat this bit as reserved. BIOS is recommeded to program this field to 1.
25	0h RW	**Drive LED on ATAPI Enable (DLAE):** When set, the HBA will drive the LED pin active for commands regardless of the state of PxCMD.ATAPI. When cleared, the HBA will only drive the LED pin active for commands if PxCMD.ATAPI is set to 0.. This bit is set by software

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Device is ATAPI (ATAPI):** When set, the connected device is an ATAPI device. This bit is used by the HBA to control whether or not to generate the desktop LED when commands are active.
23	0h RW	**Automatic Partial to Slumber Transitions Enabled (APSTE):** 0 = This port will not perform Automatic Partial to Slumber Transitions. 1 = The HBA may perform Automatic Partial to Slumber Transitions. **Note:** Software shall only set this bit to '1' if CAP2.APST is set to '1'; if CAP2.APST is cleared to '0' software shall treat this bit as reserved.
22	0h RO	**FIS-based Switching Capable Port (FBSCP):** The SATA controller does not support FIS-Based Switching.
21	0h RW/O	**External SATA Port (ESP):** 0 = This port supports internal SATA devices only. 1 = This port will be used with an external SATA device and hot-plug is supported. When set, CAP.SXS must also be set. This bit is not reset by Function Level Reset.
20	0h RO	**Cold Presence Detection (CPD):** The SATA controller does not support cold presence detect.
19	0h RW/O	**Mechanical Presence Switch Attached to Port (MPSP):** If set to 1, the platform supports a mechanical presence switch attached to this port. If cleared to 0, the platform does not support a mechanical presence switch attached to this port.
18	0h RW/O	**Hot Plug Capable Port (HPCP):** This indicates whether the this port is connected to a device which can be hot plugged. SATA by definition is hot-pluggable, but not all platforms are constructed to allow the device to be removed (it may be screwed into the chassis, for example). This bit can be used by system software to indicate a feature such as eject device to the end-user. 0 = Port is not capable of hot-plug. 1 = Port is hot-plug capable. The HBA takes no action on the state of this bit – it is for system software only. For example, if this bit is cleared, and a hot plug event occurs, the HBA shall still treat it as a proper hot plug event. **Note:** This bit is not reset on a HBA reset. This field is not reset by FLR.
17	0h RO	**Port Multiplier Attached (PMA):** When set, a Port Multiplier is attached to the HBA for this port. When cleared, a Port Multiplier is not attached to the HBA for this port. This bit is a read only 0. when CAP.PMS = 0., and read/write when CAP.PMS = 1.. Note that this bit is set by software; hardware does not auto-detect that a Port Multiplier is attached.
16	0h RO	Reserved.
15	0h RO	**Command List Running (CR):** When this bit is set it indicates that the command list DMA engine for the port is running.
14	0h RO	**FIS Receive Running (FR):** When this bit is set it indicates that the FIS Receive DMA engine for the port is running. Note to software: When FR bit stays set, please read the PxIS.PCS and PxSERR.DET.X to service the PCS interrupt accordingly if any
13	0h RO	**Mechanical Presence Switch State (MPSS):** The MPSS bit reports the state of a mechanical presence switch attached to this port. If CAP.SMPS is set to 1 and the mechanical presence switch is closed then this bit is cleared to 0. If CAP.SMPS is set to 1 and the mechanical presence switch is open then this bit is set to 1. If CAP.SMPS is set to 0 then this bit is cleared to 0. Software should only use this bit if both CAP.SMPS and PxCMD.MPSP are set to 1.
12:8	0h RO	**Current Command Slot (CCS):** Indicates the current command slot the HBA is processing. This field is valid when the PxCMD.ST bit is set, and is constantly updated by the HBA. This field can be updated as soon as the HBA recognizes an active command slot, or at some point soon after when it begins processing the command. When PxCMD.ST transitions from a 1 to a 0, the HBA will reset this field to 0. After PxCMD.ST transitions from 0 to 1, the highest priority slot to issue from next is command slot 0. After the first command has been issued, the highest priority slot to issue from next is PxCMD.CCS + 1. For example, after the HBA has issued its first command, if PxCMD.CCS = 0h and PxCI is set to 3h, the next command that will be issued is from command slot 1.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	Reserved.
6	0h RO	**PHYSLP Present (PSP):** If set to '1', the platform supports PHYSLP on this port. If cleared to '0', the platform does not support PHYSLP on this port. This bit may only be set to '1' if CAP2.SPS is set to '1'.
5	0h RO	Reserved.
4	0h RW	**FIS Receive Enable (FRE):** When set, the HBA may post received FISes into the FIS receive area pointed to by PxFB and PxFBU. When cleared, received FISes are not accepted by the HBA, except for the first D2H register FIS after the initialization sequence.
3	0h RW/1S	**Command List Override (CLO):** Setting this bit to 1 causes PxTFD.STS.BSY and PxTFD.STS.DRQ to be cleared to 0. This allows a software reset to be transmitted to the device regardless of whether the BSY and DRQ bits are still set in the PxTFD.STS register. The HBA sets this bit to 0 when PxTFD.STS.BSY and PxTFD.STS.DRQ have been cleared to 0. A write to this register with a value of 0 shall have no effect.
2	1h RO	**Power On Device (POD):** The SATA controller does not support cold presence detect.
1	0h RW	**Spin-Up Device (SUD):** This bit is read/write and default to 0 for HBAs that support staggered spin-up via CAP.SSS. This bit is read only 1 for HBAs that do not support staggered spin-up. 0 = No action. 1 = On an edge detect from 0 to 1, the PCH starts a COMRESET initialization sequence to the device. Clearing this bit causes no action on the interface. Clearing this bit to 0 does not cause any OOB signal to be sent on the interface. When this bit is cleared to 0 and PxSCTL.DET = 0h, the HBA will enter listen mode.
0	0h RW	**Start (ST):** When set, the HBA may process the command list. When cleared, the HBA may not process the command list. Whenever this bit is changed from a 0 to a 1, the HBA starts processing the command list at entry 0. Whenever this bit is changed from a 1 ot a 0, the PxCI and PxSACT register is cleared by the HBA upon the HBA putting the controller into an idle state. PxTFD shall be updated also.

17.2.21 Port 0 Task File Data (P0TFD)—Offset 120h

Port 0 Task File Data

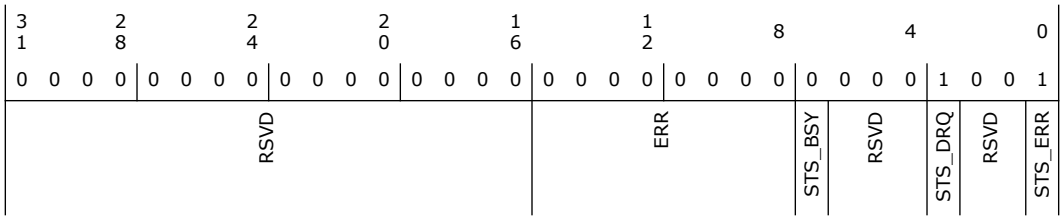
Access Method

Type: MEM Register (Size: 32 bits)

Device: 23

Function: 0

Default: 9h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:8	0h RO	**Error (ERR):** Contains the latest copy of the task file error register.
7	0h RO	**Status Busy (STS_BSY):** Status - Indicates the interface is busy.
6:4	0h RO	Reserved.
3	1h RO	**Status Drq (STS_DRQ):** Status - Indicates a data transfer is requested.
2:1	0h RO	Reserved.
0	1h RO	**Status Err (STS_ERR):** Status - Indicates an error during the transfer.

17.2.22 Port 0 Signature (P0SIG)—Offset 124h

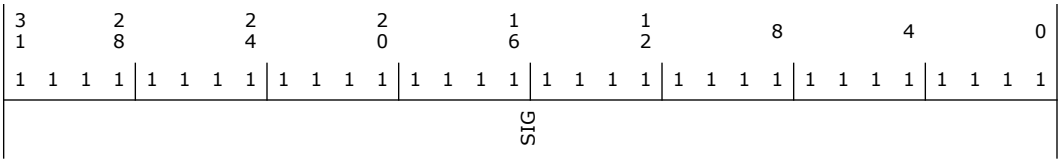
Port 0 Signature

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 23
Function: 0

Default: FFFFFFFFh



Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RO	**Signature (SIG):** Contains the signature received from a device on the first D2H Register FIS. The bit order is as follows: **Bit** — **Field** 31:24 — LBA High Register 23:16 — LBA Mid Register 15:8 — LBA Low Register 7:0 — Sector Count Register

17.2.23 Port 0 Serial ATA Status (P0SSTS)—Offset 128h

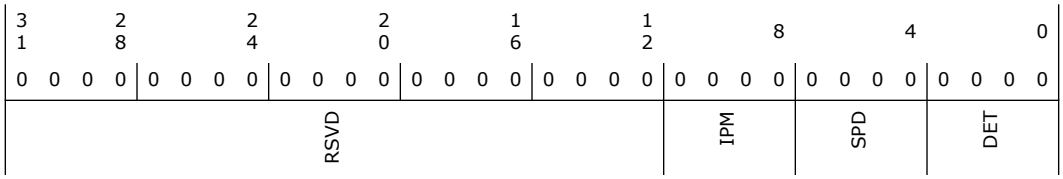
Port 0 Serial ATA Status

Access Method

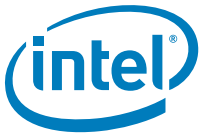
Type: MEM Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	Reserved.



Bit Range	Default & Access	Field Name (ID): Description
11:8	0h RO	**Interface Power Management (IPM):** Indicates the current interface state. **Value** — **Description** 0h — Device not present or communication not established 1h — Interface in active state 2h — Interface in PARTIAL power management state 6h — Interface in SLUMBER power management state 8h — DEVSLP asserted All other values reserved. This field reflects the interface power management state for both device and host initiated power management. **Note:** If an Automatic Partial to Slumber Transition occurs, PxSSTS.IPM shall reflect that the host has entered Slumber (PxSSTS.IPM = '6h').
7:4	0h RO	**Current Interface Speed (SPD):** Indicates the negotiated interface communication speed. **Value** — **Description** 0h — Device not present or communication not established 1h — Gen 1 communication rate negotiated 2h — Gen 2 communication rate negotiated 3h — Gen 3 communication rate negotiated All other values reserved. **Note:** If software changes SPD after port has been enabled, software is required to perform a port reset via DET=1h.
3:0	0h RO	**Device Detection (DET):** Indicates the interface device detection and Phy state. **Value** — **Description** 0h — No device detected and Phy communication not established 1h — Device presence detected but Phy communication not established 3h — Device presence detected and Phy communication established 4h — Phy in offline mode as a result of the interface being disabled or running in a BIST loopback mode All other values reserved. **Note:** While the true reset default value of this register is 0h, the value read from this register depends on drive presence and the point in time within the initialization process when the register is read. **Note:** The means by which the implementation determines device presence may be vendor specific. However, device presence shall always be indicated anytime a COMINIT signal is received.

17.2.24 Port 0 Serial ATA Control (P0SCTL)—Offset 12Ch

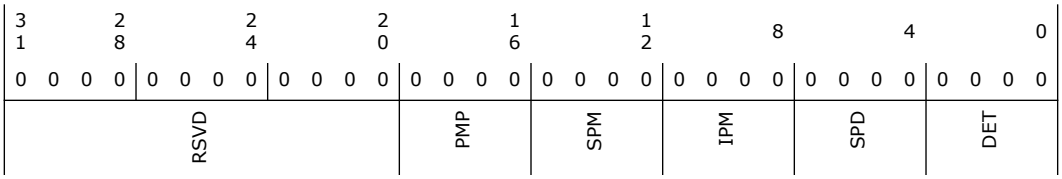
Port 0 Serial ATA Control

Access Method

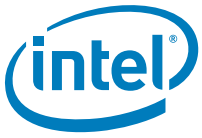
Type: MEM Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	Reserved.
19:16	0h RW	**Port Multiplier Port (PMP):** This field is not used by AHCI.
15:12	0h RW	**Select Power Management (SPM):** This field is not used by AHCI.



Bit Range	Default & Access	Field Name (ID): Description
11:8	0h RW	**Interface Power Management Transitions Allowed (IPM):** Indicates which power states the HBA is allowed to transition to. If an interface power management state is not allowed via this register field, the HBA will not initiate that state and the HBA will PMNAKp any request from the device to enter that state. **Value** — **Description** 0h — No interface power management (PM) state restrictions 1h — Transitions to the PARTIAL state PM disabled 2h — Transitions to the SLUMBER state PM disabled 3h — Transitions to both PARTIAL and SLUMBER PM states disabled 4h — Transitions to DEVSLP PM state are disabled 5h — Transitions to Partial and DEVSLP PM states are disabled 6h — Transitions to Slumber and DEVSLP PM states are disabled 7h — Transitions to Partial, Slumber and DEVSLP PM states are disabled All other values reserved.
7:4	0h RW	**Speed Allowed (SPD):** Indicates the highest allowable speed of the interface. **Value** — **Description** 0h — No speed negotiation restrictions 1h — Limit speed negotiation to Gen 1 communication rate 2h — Limit speed negotiation to Gen 2 communication rate 3h — Limit speed negotiation to Gen 3 communication rate All other values reserved
3:0	0h RW	**Device Detection Initialization (DET):** Controls the HBA.s device detection and interface initialization. **Value** — **Description** 0h — No device detection or initialization action requested 1h — Perform interface communication initialization sequence to establish communication. This is functionally equivalent to a hard reset and results in the interface being reset and communications re-initialized. While this field is 1h, COMRESET is continuously transmitted on the interface. Software should leave the DET field set to 1h for a minimum of 1 millisecond to ensure that a COMRESET is sent on the interface. 4h — Disable the Serial ATA interface and put Phy in offline mode All other values reserved. This field may only be changed when PxCMD.ST is '0'. Changing this field while the HBA is running results in undefined behavior. When PxCMD.ST is set to '1', this field should have a value of 0h. **Note:** It is permissible to implement any of the Serial ATA defined behaviors for transmission of COMRESET when PxSCTL.DET = 1h.

17.2.25 Port 0 Serial ATA Error (P0SERR)—Offset 130h

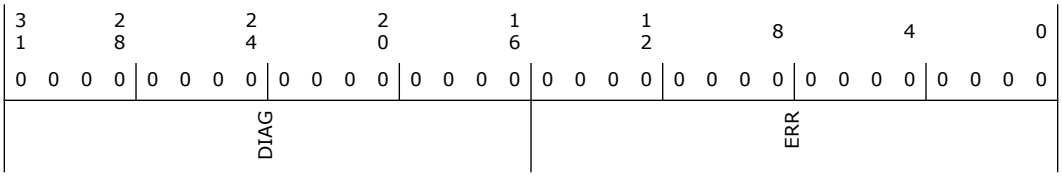
Port 0 Serial ATA Error

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW/1C	**Diagnostics (DIAG):** Contains diagnostic error information for use by diagnostic software in validating correct operation or isolating failure modes. **Bit** — **Field** 31:27 — Reserved 26 — **Exchanged (X)**: When set to one this bit indicates that a change in device presence has been detected since the last time this bit was cleared. The means by which the implementation determines that the device presence has changed is vendor specific. This bit shall always be set to one anytime a COMINIT signal is received. This bit is reflected in the P0IS.PCS bit. 25 — **Unrecognized FIS Type (F)**: Indicates that one or more FISs were received by the Transport layer with good CRC, but had a type field that was not recognized/known. 24 — **Transport state transition error (T)**: Indicates that an error has occurred in the transition from one state to another within the Transport layer since the last time this bit was cleared. 23 — **Link Sequence Error (S)**: Indicates that one or more Link state machine error conditions were encountered. The Link Layer state machine defines the conditions under which the link layer detects an erroneous transition. 22 — **Handshake Error (H):** Indicates that one or more R_ERR handshake response was received in response to frame transmission. Such errors may be the result of a CRC error detected by the recipient, a disparity or 8b/10b decoding error, or other error condition leading to a negative handshake on a transmitted frame. 21 — **CRC Error (C)**: Indicates that one or more CRC errors occurred with the Link Layer. 20 — **Disparity Error (D)**: This field is not used by AHCI. 19 — **10B to 8B Decode Error (B)**: Indicates that one or more 10B to 8B decoding errors occurred. 18 — **Comm Wake (W)**: Indicates that a Comm Wake signal was detected by the Phy. 17 — **Phy Internal Error (I)**: Indicates that the Phy detected some internal error. 16 — **PhyRdy Change (N)**: When set to 1 this bit indicates that the internal PhyRdy signal changed state since the last time this bit was cleared. The state of this bit is reflected in the PxIS.PRCS interrupt status bit and an interrupt will be generated if enabled.

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW/1C	**Error (ERR):** The ERR field contains error information for use by host software in determining the appropriate response to the error condition. If one or more of bits 11:8 of this register are set, the controller will stop the current transfer. **Bit** — **Field** 15:12 — Reserved 11 — **Internal Error (E)**: The SATA controller failed due to a master or target abort when attempting to access system memory. 10 — **Protocol Error (P)**: A violation of the Serial ATA protocol was detected. 9 — **Persistent Communication or Data Integrity Error (C)**: A communication error that was not recovered occurred that is expected to be persistent. Persistent communications errors may arise from faulty interconnect with the device, from a device that has been removed or has failed, or a number of other causes. 8 — **Transient Data Integrity Error (T)**: A data integrity error occurred that was not recovered by the interface. 7:2 — Reserved 1 — **Recovered Communications Error (M)**: Communications between the device and host was temporarily lost but was re-established. This can arise from a device temporarily being removed, from a temporary loss of Phy synchronization, or from other causes and may be derived from the PhyNRdy signal between the Phy and Link layers. 0 — **Recovered Data Integrity Error (I)**: A data integrity error occurred that was recovered by the interface through a retry operation or other recovery action.

17.2.26 Port 0 Serial ATA Active (P0SACT)—Offset 134h

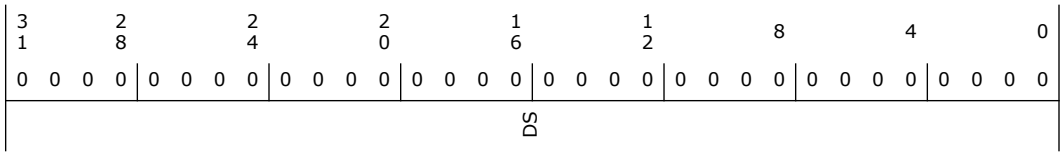
Port 0 Serial ATA Active

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/1S	**Device Status (DS):** System software sets this bit for native command queuing commands prior to setting the PxCI.CI bit in the same command slot entry. This field is cleared via the Set Device Bits FIS. This field is also cleared when PxCMD.ST is cleared by software. Note that this field is not cleared by COMRESET or SRST.

17.2.27 Port 0 Command Issue (P0CI)—Offset 138h

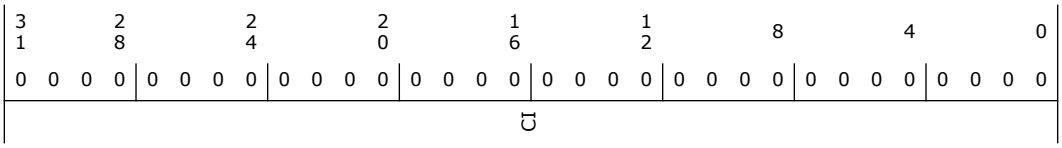
Port 0 Commands Issued

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Commands Issued (CI):** This field is set by software to indicate to the HBA that a command has been built in system memory for a command slot and may be sent to the device. When the HBA receives a FIS which clears the BSY, ERR, and DRQ bits for the command, it clears the corresponding bit in this register for that command slot. Bits in this field shall only be set to '1' by software when PxCMD.ST is set to '1'. This field is also cleared when PxCMD.ST is written from a '1' to a '0' by software.

17.2.28 Port 0 Device Sleep (P0DEVSLP)—Offset 144h

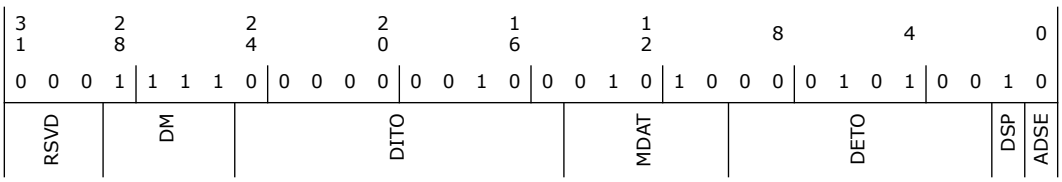
Port 0 Device Sleep

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 1E022852h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	Reserved.
28:25	Fh RW/O	**DITO Multiplier (DM):** DITO multiplier that the HBA applies to the specified DITO value, effectively extending the range of DITO from 1ms to 16368ms. A value of 0h indicates a multiplier of 1. A maximum multiplier of 16 may be applied. The HBA computes the total idle timeout as a product of DM and DITO (i.e. DITO actual = DITO * (DM+1)). **Note:** These bits are not reset by controller reset.
24:15	4h RW	**DEVSLP Idle Timeout (DITO):** This field specifies the amount of the time (in approximate 1ms granularity) that the HBA shall wait before driving the DEVSLP signal. Hardware reloads its port specific DEVSLP timer with this value each time the port transitions out of DEVSLP state. For example: from DEVSLP to active or PxDEVSLP.ADSE transitions from 0 to a 1. If CAP2.SDS or CAP2.SADM or PxDEVSLP.DSP is cleared to 0 then these bits are read-only 0h and software shall treat these bits as reserved. Software shall only set this value when PxCMD.ST is cleared to 0 and PxDEVSLP.ADSE is cleared to 0. **Note:** These bits are not reset by controller reset.
14:10	Ah RW	**DEVSLP Minimum Assertion Time (MDAT):** This field specifies the minimum amount of time (in 1ms granulatity) that the HBA must assert the DEVSLP signal before it may be de-asserted. The norminal value is 10ms and the minimum is 1ms depending on device identification information. If CAP2.SDS is cleared to 0 or PxDEVSLP.DSP is cleared to 0 then these bits are read-only 0h and software shall treat these bits as reserved. Software shall only set this value when PxCMD.ST is cleared to 0, PxDEVSLP.ADSE is cleared to 0, and prior to setting PxCMD.ICC to 8h. **Note:** These bits are not reset by controller reset.
9:2	14h RW	**DEVSLP Exit Timeout (DETO):** This field specifies the maximum duration (in approximate 1ms granularity) from DEVSLP de-assertion until the device is ready to accept OOB. The norminal value is 20ms while the max value is 255ms depending on device identification information. If CAP2.SDS is cleared to 0 or PxDEVSLP.DSP is cleared to 0 then these bits are read-only 0h and software shall treat these bits as reserved. Software shall only set this value when PxCMD.ST is cleared to 0, PxDEVSLP.ADSE is cleared to 0, and prior to setting PxCMD.ICC to 8h. **Note:** These bits are not reset by controller reset.
1	1h RW/O	**DEVSLP Present (DSP):** If set to '1', the platform supports DEVSLP on this port. If cleared to '0', the platform does not support DEVSLP on this port. This bit may only be set to '1' if CAP2.SDS is set to '1'. DSP is mutually exclusive with the PxCMD.HPCP bit and PxCMD.ESP bit. BIOS is required to program this field to ‘1’ if the system supports the DEVSLP feature. **Note:** These bits are not reset by controller reset.
0	0h RW	**Aggressive DEVSLP Enable (ADSE):** This bit is read/write for HBAs that support aggressive DEVSLP management (CAP2. SADM = '1'). When this bit is set to '1', the HBA shall assert the DEVSLP signal after the port has been idle (PxCI = 0h and PxSACT = 0h) for the amount of time specified by the PxDEVSLP.DITO register and the interface is in Slumber (PxSSTS.IPM = 6h). When this bit is cleared to '0', the HBA does not enter DEVSLP unless software directed via PxCMD.ICC. This bit shall only be set to '1' if PxDEVSLP.DSP is set to '1'. If this bit is set to '1' and software clears the bit to '0', then the HBA shall de-assert the DEVSLP signal if asserted. Note that these bits are not reset on a HBA reset. BIOS is recommended to program this field to '1' if the platform support the DEVSLP feature. If CAP2.SDS is cleared to '0' or CAP2.SADM is cleared to '0', or if PxDEVSLP.DSP is cleared to '0' then these bits are read-only 0h and software shall treat these bits as reserved.

17.2.29 Port 1 Command List Base Address (P1CLB)—Offset 180h

Same bit definition as P0CLB.

17.2.30 Port 1 Command List Base Address Upper 32-bits (P1CLBU)—Offset 184h

Same bit definition as P0CLBU.

17.2.31 Port 1 FIS Base Address (P1FB)—Offset 188h

Same bit definition as P0FB.

17.2.32 Port 1 FIS Base Address Upper 32-bits (P1FBU)—Offset 18Ch

Same bit definition as P0FBU.

17.2.33 Port 1 Interrupt Status (P1IS)—Offset 190h

Same bit definition as P0IS.

17.2.34 Port 1 Interrupt Enable (P1IE)—Offset 194h

Same bit definition as P0IE.

17.2.35 Port 1 Command (P1CMD)—Offset 198h

Same bit definition as P0CMD.

17.2.36 Port 1 Task File Data (P1TFD)—Offset 1A0h

Same bit definition as P0TFD.

17.2.37 Port 1 Signature (P1SIG)—Offset 1A4h

Same bit definition as P0SIG.

17.2.38 Port 1 Serial ATA Status (P1SSTS)—Offset 1A8h

Same bit definition as P0SSTS.

17.2.39 Port 1 Serial ATA Control (P1SCTL)—Offset 1ACh

Same bit definition as P0SCTL.

17.2.40 Port 1 Serial ATA Error (P1SERR)—Offset 1B0h

Same bit definition as P0SERR.

17.2.41 Port 1 Serial ATA Active (P1SACT)—Offset 1B4h

Same bit definition as P0SACT.

17.2.42 Port 1 Command Issue (P1CI)—Offset 1B8h

Same bit definition as P0CI.

17.2.43 Port 1 Device Sleep (P1DEVSLP)—Offset 1C4h

Same bit definition as P0DEVSLP.

17.2.44 Port 2 Command List Base Address (P2CLB)—Offset 200h

Same bit definition as P0CLB.

17.2.45 Port 2 Command List Base Address Upper 32-bits (P2CLBU)—Offset 204h

Same bit definition as P0CLBU.

17.2.46 Port 2 FIS Base Address (P2FB)—Offset 208h

Same bit definition as P0FB.

17.2.47 Port 2 FIS Base Address Upper 32-bits (P2FBU)—Offset 20Ch

Same bit definition as P0FBU.

17.2.48 Port 2 Interrupt Status (P2IS)—Offset 210h

Same bit definition as P0IS.

17.2.49 Port 2 Interrupt Enable (P2IE)—Offset 214h

Same bit definition as P0IE.

17.2.50 Port 2 Command (P2CMD)—Offset 218h

Same bit definition as P0CMD.

17.2.51 Port 2 Task File Data (P2TFD)—Offset 220h

Same bit definition as P0TFD.

17.2.52 Port 2 Signature (P2SIG)—Offset 224h

Same bit definition as P0SIG.

17.2.53 Port 2 Serial ATA Status (P2SSTS)—Offset 228h

Same bit definition as P0SSTS.

17.2.54 Port 2 Serial ATA Control (P2SCTL)—Offset 22Ch

Same bit definition as P0SCTL.

17.2.55 Port 2 Serial ATA Error (P2SERR)—Offset 230h

Same bit definition as P0SERR.

17.2.56 Port 2 Serial ATA Active (P2SACT)—Offset 234h

Same bit definition as P0SACT.

17.2.57 Port 2 Command Issue (P2CI)—Offset 238h

Same bit definition as P0CI.

17.2.58 Port 2 Device Sleep (P2DEVSLP)—Offset 244h

Same bit definition as P0DEVSLP.

17.3 SATA AIDP Registers Summary

Table 17-3. Summary of SATA AIDP Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
10h	13h	AHCI Index Register (INDEX)—Offset 10h	0h
14h	17h	AHCI Data Register (DATA)—Offset 14h	0h

17.3.1 AHCI Index Register (INDEX)—Offset 10h

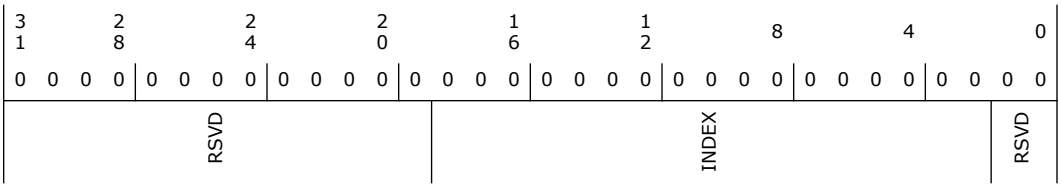
AHCI Index Register. This registers are only available if CC.SCC is not 01h to index into all memory registers defined in Memory Registers and the message buffer used for enclosure management. If CC.SCC is 01h, these AHCI Index Data Pair registers are not accessible and SINDEX/SDATA register pair shall be used to index into a subset of the memory registers defined in (See Memory Registers for more information on which registers could be indexed).

Access Method

Type: IO Register (Size: 32 bits)

Device: 23
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	Reserved.
18:2	0h RW	**Index (INDEX):** This Index register is used to select the Dword offset of the Memory Mapped AHCI register to be accessed. A Dword, Word or Byte access is specified by the active byte enables of the I/O access to the Data register.
1:0	0h RO	Reserved.

17.3.2 AHCI Data Register (DATA)—Offset 14h

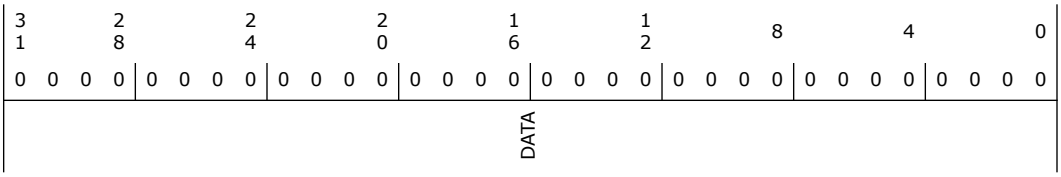
AHCI Data Register. This registers are index into all memory registers defined in Memory Registers and the message buffer used for enclosure management.

Access Method

Type: IO Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data (DATA):** This Data register is a window through which data is read or written to the memory mapped register pointed to by the Index register. Note that a physical register is not actually implemented as the data is actually stored in the memory mapped registers. Since this is not a physical register, the default value is the same as the default value of the register pointed to by Index.

17.4 SATA MXPBA Registers Summary

Table 17-4. Summary of SATA MXPBA Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	MSI-X Pending Bit Array QW 0 (MXPQW0_DW0)—Offset 0h	0h

17.4.1 MSI-X Pending Bit Array QW 0 (MXPQW0_DW0)—Offset 0h

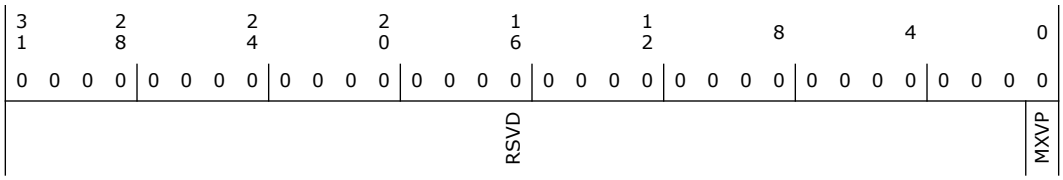
MSI-X Pending Bit Array QW 0

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RO	**MSI-X vector Pending (MXVP):** For each Pending Bit that is set, the function has a pending message for the associated MSI-X Table entry. Pending bits that have no associated MSI-X Table entry are reserved. After reset, the state of reserved Pending bits must be 0. Software should never write, and should only read Pending Bits. If software writes to Pending Bits, the result is undefined. Each Pending Bit's state after reset is 0 (no message pending).

17.5 SATA MXTBA Registers Summary

Table 17-5. Summary of SATA MXTBA Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	MSI-X Table Entries 0 Message Lower Address (MXTE0MLA)—Offset 0h	0h
4h	7h	MSI-X Table Entries 0 Message Upper Address (MXTE0MUA)—Offset 4h	0h
8h	Bh	MSI-X Table Entries 0 Message Data (MXTE0MD)—Offset 8h	0h
Ch	Fh	MSI-X Table Entries 0 Vector Control (MXTE0VC)—Offset Ch	1h

17.5.1 MSI-X Table Entries 0 Message Lower Address (MXTE0MLA)—Offset 0h

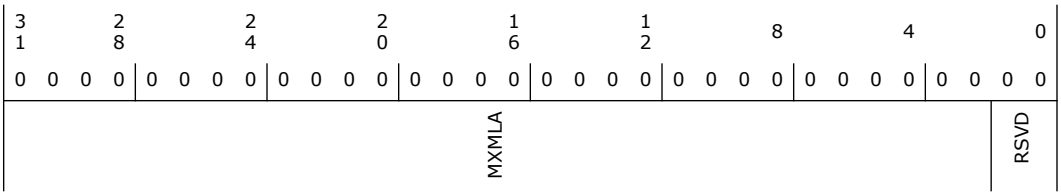
MSI-X Table Entries 0 Message Lower Address

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**MSI-X message lower address (MXMLA):** Specifies the lower 32-bit of the DWORD-aligned address (Addr[31:02]) of the MSI-X Message
1:0	0h RO	Reserved.

17.5.2 MSI-X Table Entries 0 Message Upper Address (MXTE0MUA)—Offset 4h

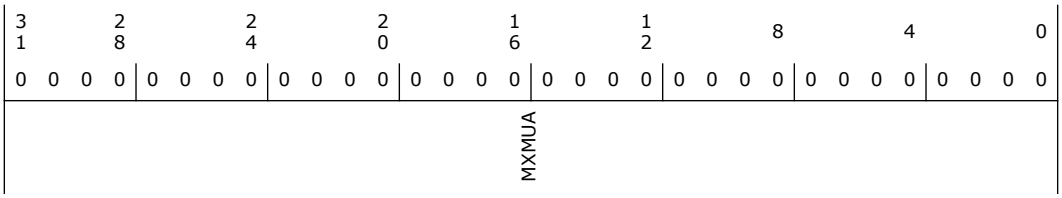
MSI-X Table Entries 0 Message Upper Address

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**MSI-X message upper 32-bit address (MXMUA):** Specifies the upper 32-bit of the MSI-X Message.

17.5.3 MSI-X Table Entries 0 Message Data (MXTE0MD)—Offset 8h

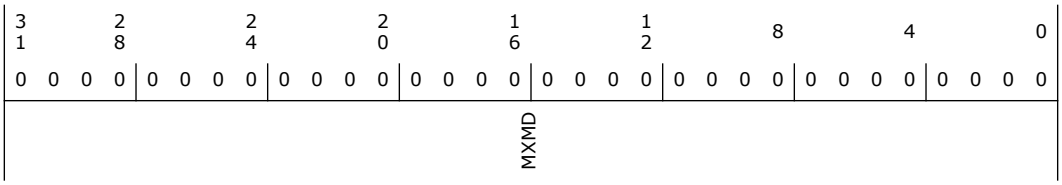
MSI-X Table Entries 0 Message Data

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**MSI-X message Data (MXMD):** Specifies the 32-bit Data of the MSI-X Message.

17.5.4 MSI-X Table Entries 0 Vector Control (MXTE0VC)—Offset Ch

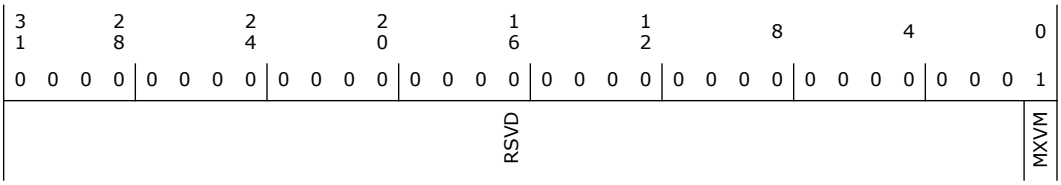
MSI-X Table Entries 0 Vector Control

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 1h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	1h RW	**MSI-X vector Mask (MXVM):** When this bit is set, the function is prohibited from sending a message using this MSI-X Table entry. However, any other MSI-X Table entries programmed with the same vector will still be capable of sending an equivalent message unless they are also masked. This bit's state after reset is 1 (entry is masked).

17.6 SATA Initialization (SIR) Index Registers Summary

Table 17-6. Summary of SATA SIR Index Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
50h	53h	SATA MPHY Dynamic Power Gating Enable—Offset 50h	0h
54h	57h	Squelch Circuit Disable—Offset 54h	0h

17.6.1 SATA MPHY Dynamic Power Gating Enable—Offset 50h

Default: 0h

Access: RW/RO

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	Reserved.
18	0h RW	**SATA MPHY Dynamic Power Gating Enable for Port 2(PHYDPGEP2):** Same definition as bit 0, but applies to port 2.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**SATA MPHY Dynamic Power Gating Enable for Port 1(PHYDPGEP1):** Same definition as bit 0, but applies to port 1.
16	0h RW	**SATA MPHY Dynamic Power Gating Enable for Port 0 (PHYDPGEP0):** 0 = SATA host controller does not perform dynamic MPhy power gating. 1 = SATA host controller supports MPhy dynamic power gating. For platforms with only internal SSDs or HDDs, set PHYDPWE0[2:0] to enable SATA MPhy dynamic power gating flow. Use the default value of 0 if the platform has one or more of the following: - SATA hot-plug enabled port (PxCMD.HPCP = 1) - SATA external port (PxCMD.ESP = 1) - SATA slimline port with zero-power ODD (ZPODD) attached (or other AN capable ODD) Note: BIOS is requested to program this field to 1 if the system supports MPhy dynamic power gating for SATA port 0 and SATA port 0 does not require Listen Mode usage. BIOS shall program this field to 1 until after BIOS has enumerated the SATA device of this port.
15:0	0h RO	Reserved.

17.6.2 Squelch Circuit Disable—Offset 54h

Default: 0h

Access: RW/RO

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	Reserved.
2	0h RW	**Port 2 Squelch Circuit Disable (P2SQOFFIDLED):** Same as bit 16, except this is for Port 2.
1	0h RW	**Port 1 Squelch Circuit Disable (P1SQOFFIDLED):** Same as bit 16, except this is for Port 1.
0	0h RW	**Port 0 Squelch Circuit Disable (P0SQOFFIDLED):** When this bit is set, port 0 Squelch Circuit is disabled when the interface is in Slumber state and no AHCI command outstanding. This feature is only applicable if GHC.AE = 1. With the Squelch Circuit is disabled, device initiated wake from Slumber is not supported. BIOS may enable this feature if the DEVSLP feature is not supported on the port. This feature shall be mutually exclusive with the DEVSLP feature.

§ §

18 Intel® Management Engine Interface (Intel® MEI) (D22:F0, D22:F1, and D22:F4)

18.1 Intel® Management Engine Interface Configuration Registers Summary

This section describes the registers for the Intel(R) Management Engine Interface 1 (MEI 1) at Device 22: Function 0.

These registers also apply to the following controllers:

MEI 2 at D22:F1

MEI 3 at D22:F4.

Table 18-1. Summary of Intel(R) Management Engine Interface Configuration Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	Identifiers (HECI1_ID)—Offset 0h	X_8086h
4h	5h	Command (HECI1_CMD)—Offset 4h	0h
6h	7h	Status (HECI1_STS)—Offset 6h	10h
8h	Bh	Revision ID and Class Code (HECI1_RID_CC)—Offset 8h	78000XXh
Ch	Ch	Cache Line Size (HECI1_CLS)—Offset Ch	0h
Dh	Dh	Master Latency Timer (HECI1_MLT)—Offset Dh	0h
Eh	Eh	Header Type (HECI1_HTYPE)—Offset Eh	80h
Fh	Fh	Built In Self-Test (HECI1_BIST)—Offset Fh	0h
10h	13h	HECI MMIO Base Address Low (HECI1_MMIO_MBAR_LO)—Offset 10h	4h
14h	17h	HECI MMIO Base Address High (HECI1_MMIO_MBAR_HI)—Offset 14h	0h
2Ch	2Fh	Sub System Identifiers (HECI1_SS)—Offset 2Ch	0h
34h	37h	Capabilities Pointer (HECI1_CAP)—Offset 34h	50h
3Ch	3Dh	Interrupt Information (HECI1_INTR)—Offset 3Ch	100h
3Eh	3Eh	Minimum Grant (HECI1_MGNT)—Offset 3Eh	0h
3Fh	3Fh	Maximum Latency (HECI1_MLAT)—Offset 3Fh	0h
40h	43h	Host Firmware Status Register 1 (HFSTS1)—Offset 40h	0h
48h	4Bh	Host Firmware Status Register 2 (HFSTS2)—Offset 48h	0h
4Ch	4Fh	Host General Status (HECI1_H_GS1)—Offset 4Ch	0h
50h	51h	PCI Power Management Capability ID (HECI1_PID)—Offset 50h	8C01h
52h	53h	PCI Power Management Capabilities (HECI1_PC)—Offset 52h	4003h
54h	55h	PCI Power Management Control and Status (HECI1_PMCS)—Offset 54h	8h
60h	63h	Host Firmware Status Register 3 (HFSTS3)—Offset 60h	0h
64h	67h	Host Firmware Status Register 4 (HFSTS4)—Offset 64h	0h

Table 18-1. Summary of Intel(R) Management Engine Interface Configuration Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
68h	6Bh	Host Firmware Status Register 5 (HFSTS5)—Offset 68h	0h
6Ch	6Fh	Host Firmware Status Register 6 (HFSTS6)—Offset 6Ch	0h
70h	73h	Host General Status 2 (HECI1_H_GS2)—Offset 70h	0h
74h	77h	Host General Status 3 (HECI1_H_GS3)—Offset 74h	0h
8Ch	8Dh	Message Signaled Interrupt Identifiers (HECI1_MID)—Offset 8Ch	5h
8Eh	8Fh	Message Signaled Interrupt Message Control (HECI1_MC)—Offset 8Eh	80h
90h	93h	Message Signaled Interrupt Message Address (HECI1_MA)—Offset 90h	0h
94h	97h	Message Signaled Interrupt Upper Address (HECI1_MUA)—Offset 94h	0h
98h	99h	Message Signaled Interrupt Message Data (HECI1_MD)—Offset 98h	0h
A0h	A0h	HECI Interrupt Delivery Mode (HECI1_HIDM)—Offset A0h	0h

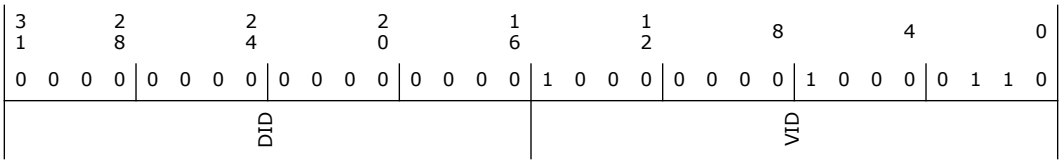
18.1.1 Identifiers (HECI1_ID)—Offset 0h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 0

Default: X_8086h



Bit Range	Default & Access	Field Name (ID): Description
31:16	-- RO/V	**Device ID (DID):** Indicates what device number assigned by Intel. See the Device and Version ID Table in Volume 1 for the default value.
15:0	8086h RO	**Vendor ID (VID):** 16-bit field which indicates Intel is the vendor.

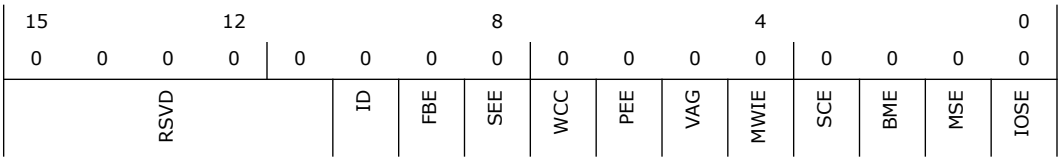
18.1.2 Command (HECI1_CMD)—Offset 4h

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 22
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:11	0h RO	Reserved.
10	0h RW	**Interrupt Disable (ID)**
9	0h RO	**Fast Back-to-Back Enable (FBE):** Not implemented, hardwired to 0.
8	0h RO	**SERR# Enable (SEE):** Not implemented, hardwired to 0.
7	0h RO	**Wait Cycle Enable (WCC):** Not implemented, hardwired to 0.
6	0h RO	**Parity Error Response Enable (PEE):** Not implemented, hardwired to 0.
5	0h RO	**VGA Palette Snooping Enable (VAG):** Not implemented, hardwired to 0.
4	0h RO	**Memory Write and Invalidate Enable (MWIE):** Not implemented, hardwired to 0.
3	0h RO	**Special Cycle Enable (SCE):** Not implemented, hardwired to 0.
2	0h RW	**Bus Master Enable (BME):** Controls the HECI host controller's ability to act as a system memory master for data transfers. When this bit is cleared, HECI bus master activity stops and any active DMA engines return to an idle condition.
1	0h RW	**Memory Space Enable (MSE):** Controls access to the HECI host controllers memory mapped register space.
0	0h RO	**I/O Space Enable (IOSE):** Not implemented, hardwired to 0.

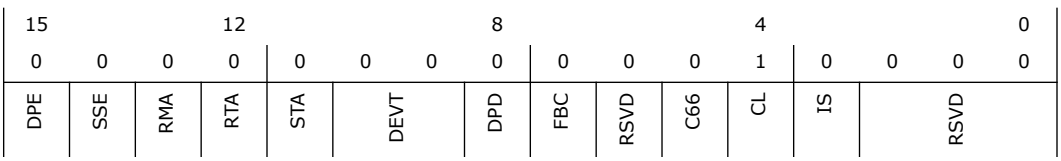
18.1.3 Status (HECI1_STS)—Offset 6h

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 22
Function: 0

Default: 10h



Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Detected Parity Error (DPE)**
14	0h RO	**Signaled System Error (SSE)**
13	0h RO	**Received Master-Abort (RMA)**
12	0h RO	**Received Target Abort (RTA):** Not implemented, hardwired to 0.
11	0h RO	**Signaled Target-Abort (STA):** Not implemented, hardwired to 0.
10:9	0h RO	**DEVSEL# Timing (DEVT):** Not implemented, hardwired to 0.
8	0h RO	**Master Data Pariy Error Detected (DPD):** Not implemented, hardwired to 0.
7	0h RO	**Fast Back-to-Back Capable (FBC):** Not implemented, hardwired to 0.
6	0h RO	Reserved.
5	0h RO	**66 MHz Capable (C66):** Not implemented, hardwired to 0.
4	1h RO	**Capabilities List (CL):** Indicates the presence of a capabilities list, hardwired to 1.
3	0h RO/V	**Interrupt Status (IS):** Reflects the state of the INTx# signal at the input of the enable/disable circuit. This bit is a 1 when the INTx# is asserted.This bit is a 0 after the interrupt is cleared (independent of the state of the Interrupt Disable bit in the command register). Note that this bit is not set by an MSI.
2:0	0h RO	Reserved.

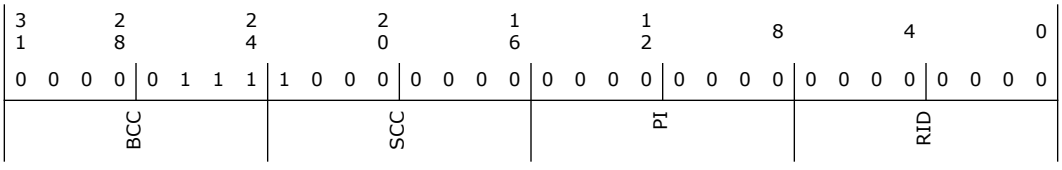
18.1.4 Revision ID and Class Code (HECI1_RID_CC)—Offset 8h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 0

Default: 78000xxh



Bit Range	Default & Access	Field Name (ID): Description
31:24	7h RO	**Base Class Code (BCC):** Indicates the base class code of the host controller device.
23:16	80h RO	**Sub Class Code (SCC):** Indicates the sub class code of the host controller device.
15:8	0h RO	**Programming Interface (PI):** Indicates the programming interface of the host controller device.
7:0	---- RO/V	**Revision ID (RID):** Indicates stepping of the host controller. Refer to Device and Revision ID table in Vol1 for specific value.

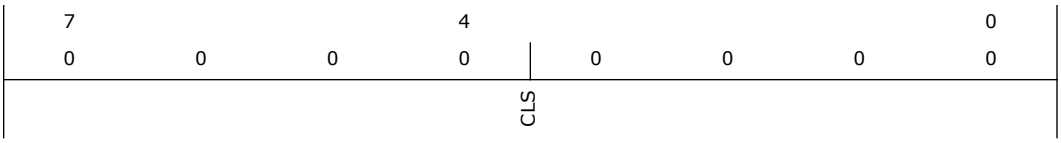
18.1.5 Cache Line Size (HECI1_CLS)—Offset Ch

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 22
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RO	**Cache Line Size (CLS):** Not implemented, hardwired to 0.

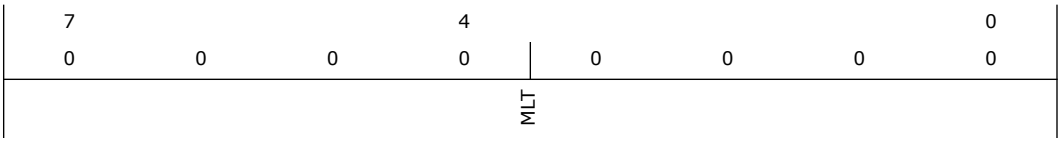
18.1.6 Master Latency Timer (HECI1_MLT)—Offset Dh

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 22
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RO	**Master Latency Timer (MLT):** Not implemented, hardwired to 0.

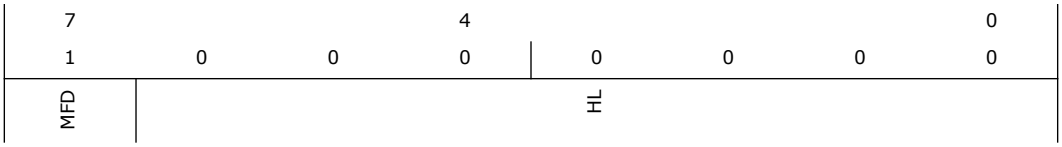
18.1.7 Header Type (HECI1_HTYPE)—Offset Eh

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 22
Function: 0

Default: 80h



Bit Range	Default & Access	Field Name (ID): Description
7	1h RO	**Multi-Function Device (MFD):** Indicates the host controller is part of a multi-function device.
6:0	0h RO	**Header Layout (HL):** Indicates that the host controller uses a target device layout.

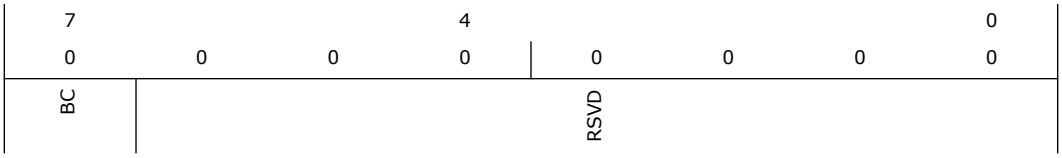
18.1.8 Built In Self-Test (HECI1_BIST)—Offset Fh

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 22
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**BIST Capable (BC):** Not implemented, hardwired to 0.
6:0	0h RO	Reserved.

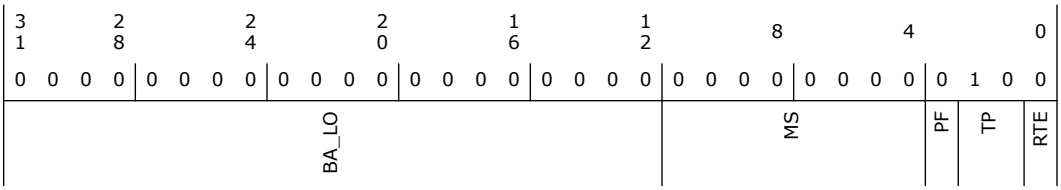
18.1.9 HECI MMIO Base Address Low (HECI1_MMIO_MBAR_LO)—Offset 10h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 0

Default: 4h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW	**Base Address Low (BA_LO):** Lower 32 bits of base address of register memory space.
11:4	0h RO	**Memory Size (MS):** This field is hardwired to 0 to indicate that HECI device requests 4KB of memory space.
3	0h RO	**Prefetchable (PF):** Indicates that this range is not pre-fetchable
2:1	2h RO	**Type (TP):** Indicates that this range can be mapped anywhere in 64-bitaddress space.
0	0h RO	**Resource Type Indicator (RTE):** Indicates a request for register memory space.

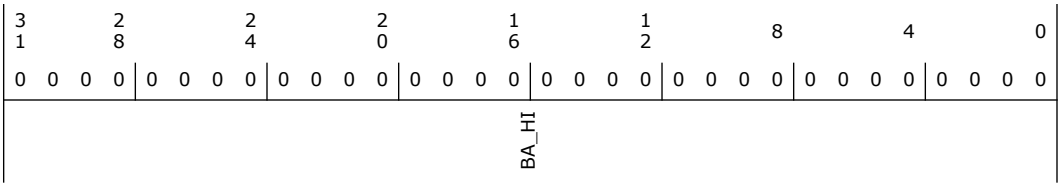
18.1.10 HECI MMIO Base Address High (HECI1_MMIO_MBAR_HI)—Offset 14h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Base Address High (BA_HI):** Upper 32 bits of base address of register memory space.

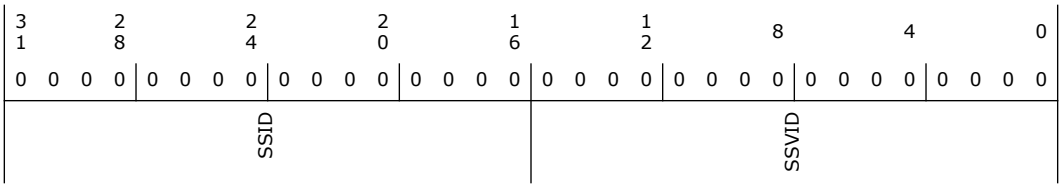
18.1.11 Sub System Identifiers (HECI1_SS)—Offset 2Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW/O	**Subsystem ID (SSID):** Indicates the sub- system identifier. This field should be programmed by BIOS during boot-up. Once written, this register becomes Read Only.
15:0	0h RW/O	**Subsystem Vendor ID (SSVID):** Indicates the sub-system vendor identifier. This field should be programmed by BIOS during boot- up. Once written, this register becomes Read Only.

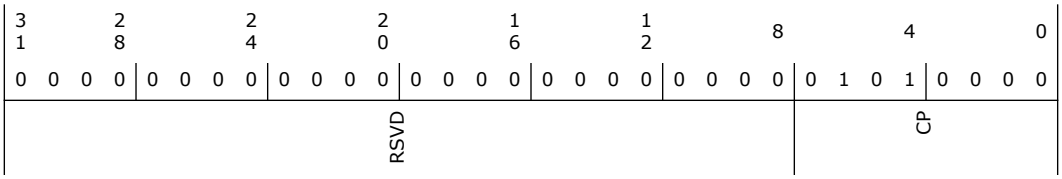
18.1.12 Capabilities Pointer (HECI1_CAP)—Offset 34h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 0

Default: 50h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	50h RO	**Capability Pointer (CP):** Indicates the first capability pointer offset. It points to the PCI power management capability offset.

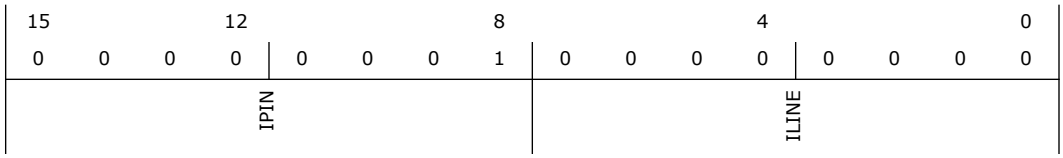
18.1.13 Interrupt Information (HECI1_INTR)—Offset 3Ch

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 22
Function: 0

Default: 100h



Bit Range	Default & Access	Field Name (ID): Description
15:8	1h RO/V	**Interrupt Pin (IPIN):** This field indicates the virtual interrupt pin the host controller uses. A value of 0x1/0x2/0x3/0x4 indicates that this function implements legacy interrupt on INTA/INTB/INTC/INTD, respectively. When legacy interrupt is not used this register should be set to 0x0.
7:0	0h RW	**Interrupt Line (ILINE):** Software written value to indicate which interrupt line (vector) theinterrupt is connected to. No hardware action is taken on this field.

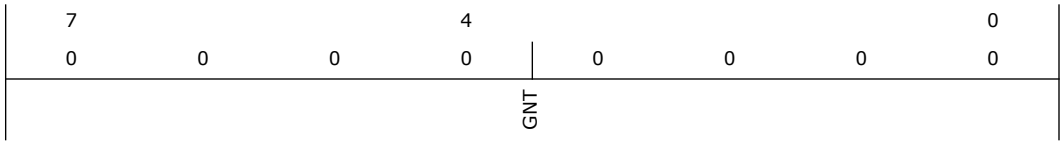
18.1.14 Minimum Grant (HECI1_MGNT)—Offset 3Eh

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 22
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RO	**Grant (GNT):** Not implemented, hardwired to 0.

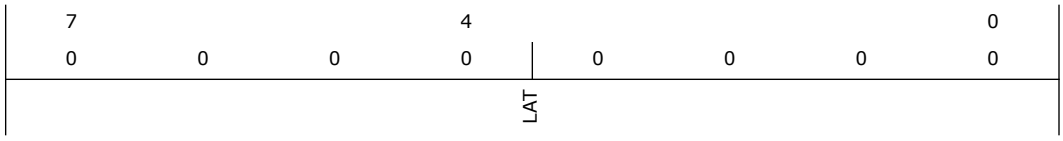
18.1.15 Maximum Latency (HECI1_MLAT)—Offset 3Fh

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 22
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RO	**Latency (LAT):** Not implemented, hardwired to 0.

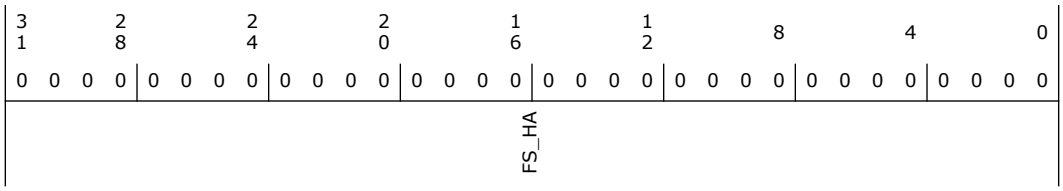
18.1.16 Host Firmware Status Register 1 (HFSTS1)—Offset 40h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Host Firmware Status (FS_HA):** Indicates current status of the firmware for the controller. This field is the host's read only access to the FS field in the ME Firmware Status register. **This field is reset during CSE partition reset flow.**

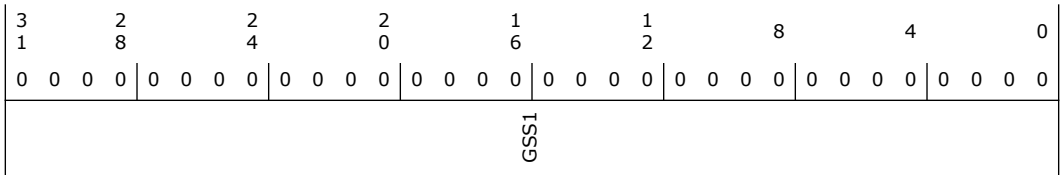
18.1.17 Host Firmware Status Register 2 (HFSTS2)—Offset 48h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Host Firmware Status (GSS1):** This field is host side shadow of General Status 1 (CSE_GS1) register.**This field is reset during ME partition reset flow.**

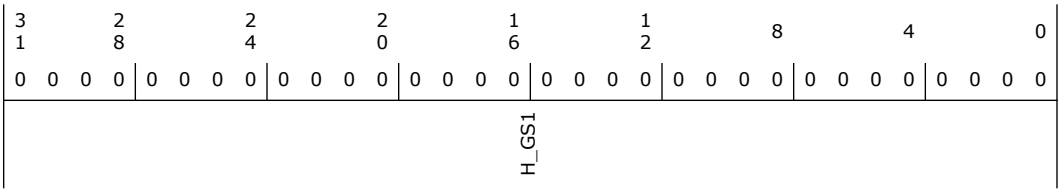
18.1.18 Host General Status (HECI1_H_GS1)—Offset 4Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Host General Status (H_GS1):** General status of Host. This field is not used by hardware.

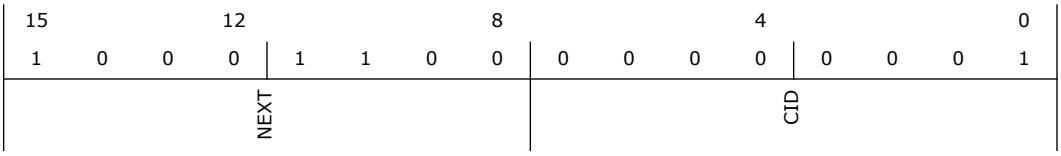
18.1.19 PCI Power Management Capability ID (HECI1_PID)—Offset 50h

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 22
Function: 0

Default: 8C01h



Bit Range	Default & Access	Field Name (ID): Description
15:8	8Ch RO	**Next Capability (NEXT):** Indicates the location of the next capability item in the list. This is the Message Signaled Interrupts capability.
7:0	1h RO	**Cap ID (CID):** Indicates that this pointer is a PCI power management.

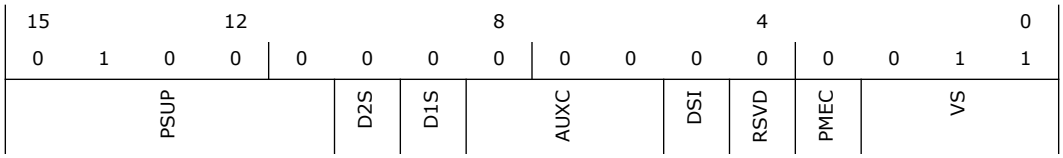
18.1.20 PCI Power Management Capabilities (HECI1_PC)—Offset 52h

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 22
Function: 0

Default: 4003h



Bit Range	Default & Access	Field Name (ID): Description
15:11	8h RO	**PME Support (PSUP):** Indicates the states that can generate PME#. The controller can assert PME# from D3hot only.
10	0h RO	**D2 Support (D2S):** The D2 state is not supported for the host controller.
9	0h RO	**D _Support (D1S):** The D1 state is not supported for the host controller.
8:6	0h RO	**Aux_Current (AUXC):** Reports the maximum Suspend well current required when in the D3COLD state. Value of 0 is reported.
5	0h RO	**Device Specific Initialization (DSI):** Indicates whether device-specific initialization is required.
4	0h RO	Reserved.
3	0h RO	**PME Clock (PMEC):** Indicates that PCI clock is not required to generate PME#.
2:0	3h RO	**Version (VS):** Indicates support for Revision 1.2 of the PCI Power Management Specification.

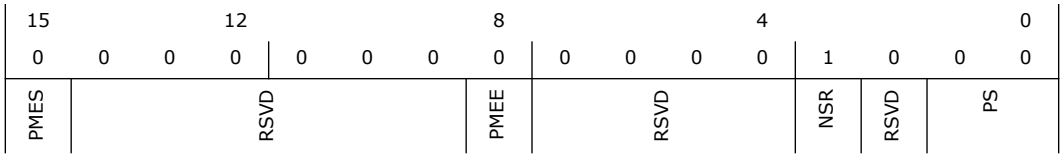
18.1.21 PCI Power Management Control and Status (HECI1_PMCS)—Offset 54h

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 22
Function: 0

Default: 8h



Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1C/V	**PME Status (PMES):** The PME Status bit can be set to '1' by the FW. This bit is cleared by host CPU writing a '1' to it. FW cannot clear this bit. Host CPU writes with value '0' have no effect on this bit.
14:9	0h RO	Reserved.
8	0h RW	**PME Enable (PMEE):** When set, PME_assert and PME_deassert messages are sent over Sideband to PMC based on the PMES bit. When reset these messages may not be sent.

Bit Range	Default & Access	Field Name (ID): Description
7:4	0h RO	Reserved.
3	1h RO	**No Soft Reset (NSR):** This bit indicates that when the controller is transitioning from D3hot to D0 due to power state command, it does not perform and internal reset.
2	0h RO	Reserved.
1:0	0h RW	**Power State (PS):** This field is used both to determine the current power state of the controller and to set a new power state. The values are: 00 - D0 state 11 - D3HOT state. The D1 and D2 states are not supported for this controller. If software attempts to write an unsupported, optional state to this field, the write operation must complete normally on the bus; however, the data is discarded and no state change occurs. When in the D3HOT state, the HBA's configuration space is available, but the registers memory space is not. Additionally, interrupts are blocked.

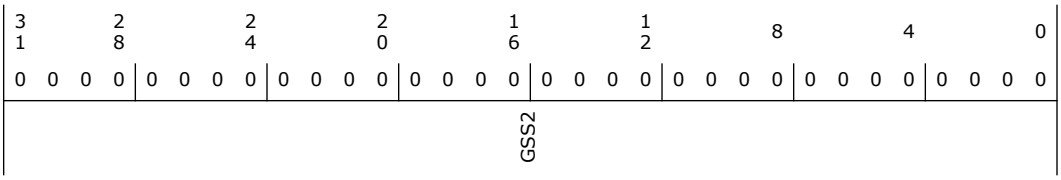
18.1.22 Host Firmware Status Register 3 (HFSTS3)—Offset 60h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Host Firmware Status (GSS2):** This field is host side shadow of ME General Status 2 (CSE_GS2). **This field is reset during ME partition reset flow.**

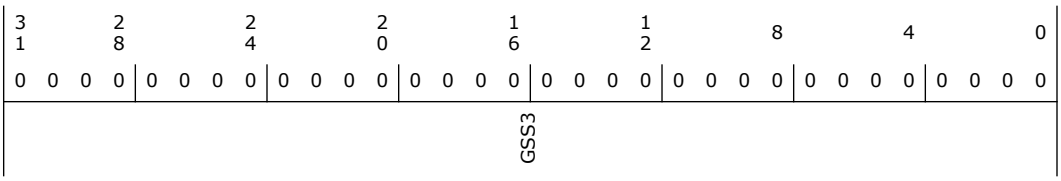
18.1.23 Host Firmware Status Register 4 (HFSTS4)—Offset 64h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Host Firmware Status (GSS3):** This field is host side shadow of CSE General Status 3 (CSE_GS3). **This field is reset during ME partition reset flow.**

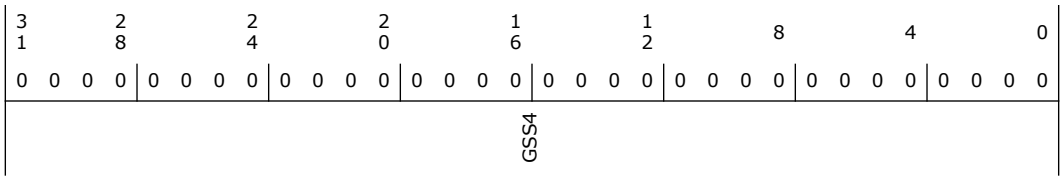
18.1.24 Host Firmware Status Register 5 (HFSTS5)—Offset 68h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Host Firmware Status (GSS4):** This field is host side shadow of ME General Status 4 (CSE_GS4). **This field is reset during ME partition reset flow.**

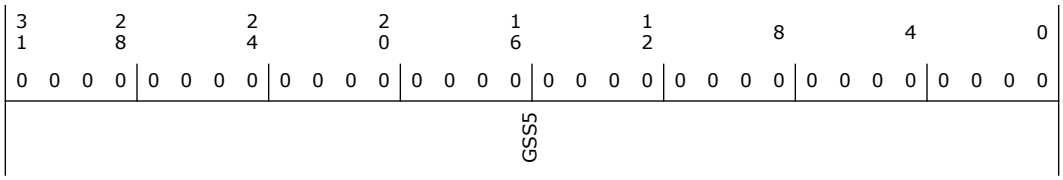
18.1.25 Host Firmware Status Register 6 (HFSTS6)—Offset 6Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Host Firmware Status (GSS5):** This field is host side shadow of ME General Status 5 (CSE_GS5). **This field is reset during ME partition reset flow.**

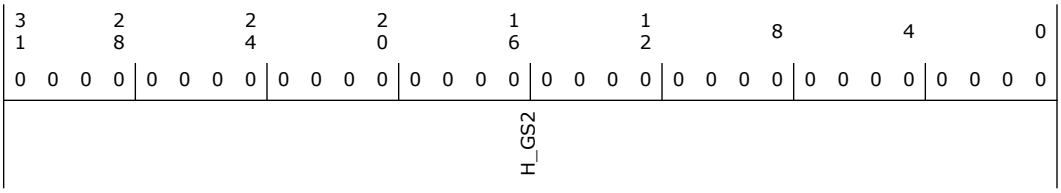
18.1.26 Host General Status 2 (HECI1_H_GS2)—Offset 70h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Host General Status 2 (H_GS2):** General status of Host. This field is not used by hardware.

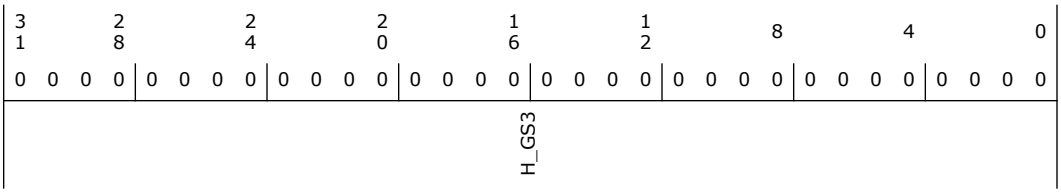
18.1.27 Host General Status 3 (HECI1_H_GS3)—Offset 74h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Host General Status 3 (H_GS3):** General status of Host. This field is not used by hardware.

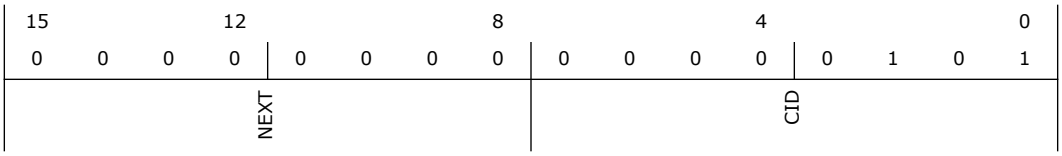
18.1.28 Message Signaled Interrupt Identifiers (HECI1_MID)—Offset 8Ch

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 22
Function: 0

Default: 5h



Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Next Pointer (NEXT):** Indicates the next item in the list. This can be other capability pointers (such as PCI-X or PCI- Express) or it can be the last item in the list.
7:0	5h RO	**Capability ID (CID):** Indicates MSI.

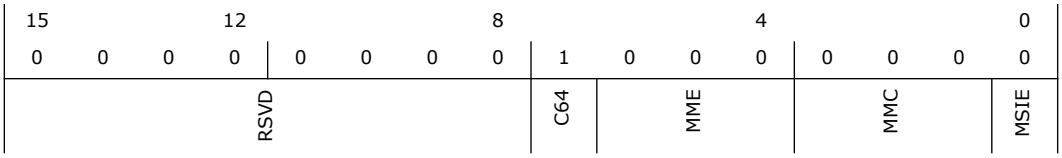
18.1.29 Message Signaled Interrupt Message Control (HECI1_MC)—Offset 8Eh

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 22
Function: 0

Default: 80h



Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	Reserved.
7	1h RO	**64 Bit Address Capable (C64):** Specifies whether capable of generating 64-bit messages.
6:4	0h RO	**Multiple Message Enable (MME):** Not implemented, hardwired to 0.
3:1	0h RO	**Multiple Message Capable (MMC):** Not implemented, hardwired to 0.
0	0h RW	**MSI Enable (MSIE):** If set, MSI is enabled and INTx virtual wires are not used to generate interrupts.

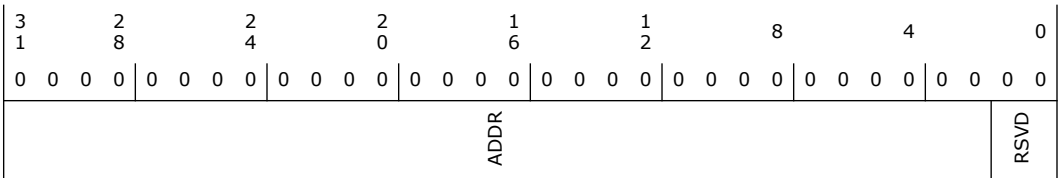
18.1.30 Message Signaled Interrupt Message Address (HECI1_MA)—Offset 90h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**Address (ADDR):** Lower 32 bits of the system specified message address, always DW aligned.
1:0	0h RO	Reserved.

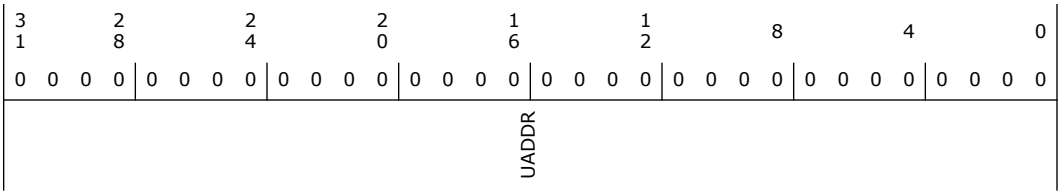
18.1.31 Message Signaled Interrupt Upper Address (HECI1_MUA)—Offset 94h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Upper Address (UADDR):** Upper 32 bits of the system specified message address. This register is optional and only implemented if MC.C64=1.

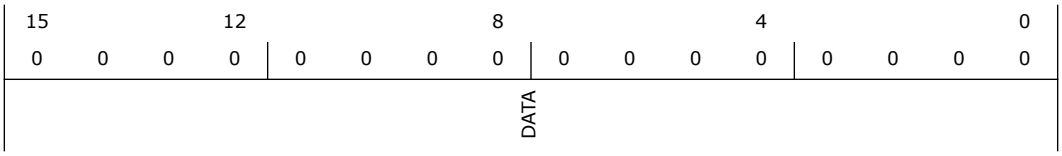
18.1.32 Message Signaled Interrupt Message Data (HECI1_MD)—Offset 98h

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 22
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW	**Data (DATA):** This 16-bit field is programmed by system software if MSI is enabled.

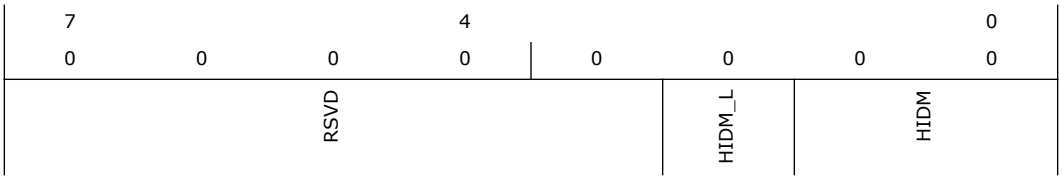
18.1.33 HECI Interrupt Delivery Mode (HECI1_HIDM)—Offset A0h

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 22
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7:3	0h RO	Reserved.
2	0h RW/1S	**HIDM Lock (HIDM_L):** Writing 1 to this bit locks the HIDM field.
1:0	0h RW/L	**HECI Interrupt Delivery Mode (HIDM):** These bits control what type of interrupt the controller will send when ME FW writes to set the CSE_IG bit. They are interpreted as follows: 00 - Generate Legacy or MSI interrupt; 01 - Generate SCI; 10 - Generate SMI; This field may be locked by writing 1 to HIDM_L bit.

18.2 Intel® MEI MMIO Registers Summary

Table 18-2. Summary of Intel® MEI MMIO Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
800h	803h	D0i3 Control (HECI1_D0I3C)—Offset 800h	0h

18.2.1 D0i3 Control (HECI1_D0I3C)—Offset 800h

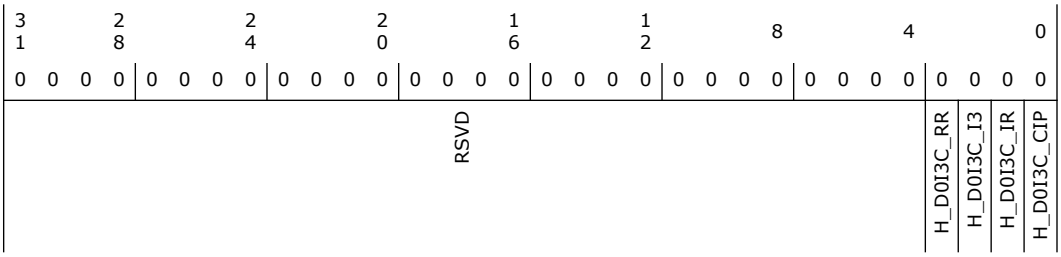
This register allows host to configure the power mode using D0i0/D0i3 support.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 22
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3	0h RO	**Restore Required (H_D0I3C_RR):** SW sets this bit to 1 in order to move the interface into the D0i3 state. Clearing this bit will return the interface into the fully active D0 state (D0i0).
2	0h RW	**D0i3 (H_D0I3C_I3):** SW sets this bit to 1 in order to move the IP into the D0i3 state. Clearing this bit will return the IP into the fully active D0 state (D0i0). When this bit changes state, mIA may be interrupted (see H_PCI_CSR.D0I3C_IS register's description)
1	0h RW	**Interrupt Request (H_D0I3C_IR):** SW sets this bit to 1 to ask for an interrupt to be generated on completion of the command. SW must clear or set this bit on each write to this register.
0	0h RO/V	**Command-in-Progress (H_D0I3C_CIP):** HW sets this bit on a 0->1 or 1->0 transition of D0i3 bit (bit [2]). While set, the other bits in this register are not valid and it is illegal for SW to write to any of them. While clear, all other bits in this register are valid and SW may write to them. If Interrupt Request (bit [1]) was set for the current command, HW may clear this bit before the interrupt has been made visible to SW, since when SW actually handles a particular interrupt is not visible to HW. SW writes to this bit have no effect. This bit is auto-cleared by HW one cycle after it is set.

§ §

19 IDE Redirect (IDE-R) (D22:F2)

19.1 IDE Redirect PCI Configuration (D22:F2) Registers Summary

Table 19-1. Summary of IDE Redirect PCI Configuration (D22:F2) Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	Device ID and Vendor ID (IDE_HOST_DID_VID)—Offset 0h	X_8086h
4h	7h	Status and Command (IDE_HOST_STS_CMD)—Offset 4h	B00000h
8h	Bh	Class Code and Revision ID (IDE_HOST_CC_RID)—Offset 8h	10185xxh
Ch	Fh	BIST, Header Type, Latency Timer, and Cache Line Size (IDE_HOST_BIST_HTYPE_LT_CLS)—Offset Ch	800000h
10h	13h	IDE Primary Command Block IO BAR (IDE_HOST_PCMDIOBAR)—Offset 10h	1h
14h	17h	IDE Primary Control Block IO BAR (IDE_HOST_PCTLIOBAR)—Offset 14h	1h
18h	1Bh	IDE Secondary Command Block IO BAR (IDE_HOST_SCMDIOBAR)—Offset 18h	1h
1Ch	1Fh	IDE Secondary Control Block IO BAR (IDE_HOST_SCTLIOBAR)—Offset 1Ch	1h
20h	23h	IDE Bus Master Block IO BAR (IDE_HOST_BMIOBAR)—Offset 20h	1h
2Ch	2Fh	Subsystem ID and Subsystem Vendor ID (IDE_HOST_SID_SVID)—Offset 2Ch	8086h
34h	37h	Capabilities List Pointer (IDE_HOST_CAPP)—Offset 34h	40h
3Ch	3Fh	Maximum Latency, Minimum Grant, Interrupt Pin and Interrupt Line (IDE_HOST_MAXL_MING_INTP_INTL)—Offset 3Ch	0h
40h	43h	MSI Message Control, Next Pointer and Capability ID (IDE_HOST_MSIMC_MSINP_MSICID)—Offset 40h	805005h
44h	47h	MSI Message Address (IDE_HOST_MSIMA)—Offset 44h	0h
48h	4Bh	MSI Message Upper Address (IDE_HOST_MSIMUA)—Offset 48h	0h
4Ch	4Fh	MSI Message Data (IDE_HOST_MSIMD)—Offset 4Ch	0h
50h	53h	Power Management Capabilities, Next Pointer and Capability ID (IDE_HOST_PMCAP_PMNP_PMCID)—Offset 50h	230001h
54h	57h	Power Management Data, Control/Status Register Bridge Support Extensions, Control and Status (IDE_HOST_PMD_PMCSRBSE_PMCSR)—Offset 54h	8h

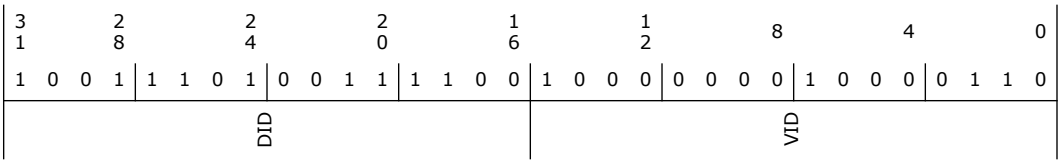
19.1.1 Device ID and Vendor ID (IDE_HOST_DID_VID)—Offset 0h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 2

Default: xxxx8086h



Bit Range	Default & Access	Field Name (ID): Description
31:16	-- RO/V	**Device ID (DID):** This field identifies the particular device. See the Device and Version ID Table in Volume 1 for the default value.
15:0	8086h RO	**Vendor ID (VID):** This field identifies the manufacturer of the device. The value of 0x8086 indicates Intel.

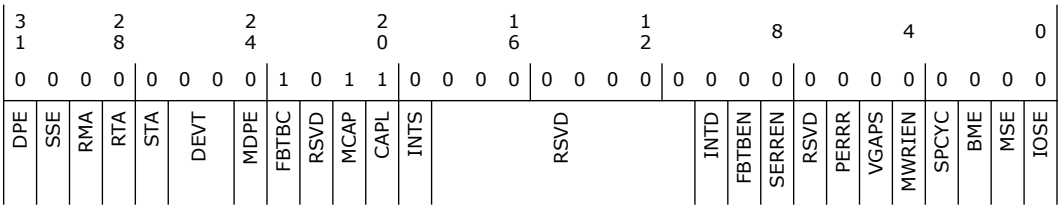
19.1.2 Status and Command (IDE_HOST_STS_CMD)—Offset 4h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 2

Default: B00000h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Detected Parity Error (DPE):** Not implemented. Hardwired to 0.
30	0h RO	**Signaled System Error (SSE):** Not implemented. Hardwired to 0.
29	0h RW/1C/V	**Received Master Abort (RMA):** This bit must be set by a master device whenever its transaction (except for Special Cycle) is completed with Unsupported Request Completion Status (a.k.a. Master-Abort). All master devices must implement this bit.
28	0h RW/1C/V	**Received Target Abort (RTA):** This bit must be set by a master device whenever its transaction is completed with Completer Abort Completion Status (a.k.a. Target-Abort). All master devices must implement this bit.
27	0h RW/1C/V	**Signaled Target Abort (STA):** This bit must be set by a target device whenever it completes a Posted or Non-Posted transaction with a Completer Abort (a.k.a. Target-Abort) error. Devices that will never signal Completer Abort (a.k.a. Target-Abort) do not need to implement this bit.
26:25	0h RO	**Devsel Timing (DEVT):** These bits encode the timing of DEVSEL#. There are three allowable timings for assertion of DEVSEL# as described below: 00b: fast; 01b: medium; 10b: slow; 11b: reserved. These bits are read-only and must indicate the slowest time that a device asserts DEVSEL# for any bus command except Configuration Read and Configuration Write. Hardwired to 00b.

Bit Range	Default & Access	Field Name (ID): Description
24	0h RO	**Master Data Parity Error (MDPE):** Not implemented. Hardwired to 0.
23	1h RO	**Fast Back to Back Capable (FBTBC):** This bit indicates whether or not the target is capable of accepting fast back-to-back transactions when the transactions are not to the same agent. This bit can be set to 1 if the device can accept these transactions and must be set to 0 otherwise. Hardwired to 1.
22	0h RO	Reserved.
21	1h RO	**66 Mhz Capable (MCAP):** This bit indicates whether or not this device is capable of running at 66 MHz. A value of 0 indicates 33 MHz. A value of 1 indicates that the device is 66 MHz capable. Hardwired to 1.
20	1h RO	**Capabilities List (CAPL):** This optional read-only bit indicates whether or not this device implements the pointer for a New Capabilities linked list at offset 34h. A value of zero indicates that no New Capabilities linked list is available. A value of one indicates that the value read at offset 34h is a pointer in Configuration Space to a linked list of new capabilities.
19	0h RO	**Interrupt Status (INTS):** This read-only bit reflects the state of the interrupt in the device/function. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the device's/function's INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. Read-only and hardwired to 0 for a device that does NOT support pin-based interrupt.
18:11	0h RO	Reserved.
10	0h RW	**Interrupt Disable (INTD):** This bit disables the device/function from asserting INTx#. A value of 0 enables the assertion of its INTx# signal. A value of 1 disables the assertion of its INTx# signal. This bit's state after RST# is 0.
9	0h RO	**Fast Back to Back Enable (FBTBEN):** Not implemented. Hardwired to 0.
8	0h RO	**System Error Enable (SERREN):** Not implemented. Hardwired to 0.
7	0h RO	Reserved.
6	0h RO	**Parity Error Response (PERRR):** Not implemented. Hardwired to 0.
5	0h RO	**VGA Palette Snoop (VGAPS):** Not implemented. Hardwired to 0.
4	0h RO	**Memory Write and Invalidate Enable (MWRIEN):** Not implemented. Hardwired to 0.
3	0h RO	**Special Cycles (SPCYC):** Not implemented. Hardwired to 0.
2	0h RW	**Bus Master Enable (BME):** This bit controls the PCI device's ability to act as a master for data transfers. This bit does not impact the generation of completions for split transaction commands.
1	0h RO	**Memory Space Enable (MSE):** Read-only and hardwired to 0 because IDE does NOT support Memory Space accesses.
0	0h RW	**IO Space Enable (IOSE):** Controls a device's response to I/O Space accesses. A value of 0 disables the device response. A value of 1 allows the device to respond to I/O Space accesses. State after RST# is 0.

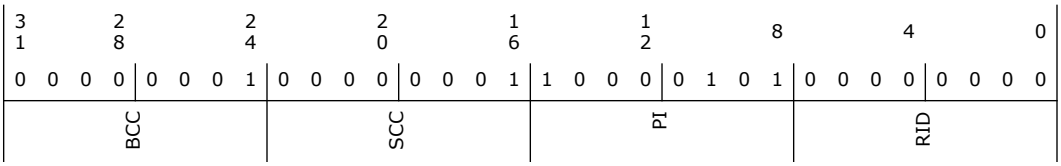
19.1.3 Class Code and Revision ID (IDE_HOST_CC_RID)—Offset 8h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 2

Default: 10185xxh



Bit Range	Default & Access	Field Name (ID): Description
31:24	1h RO	**Base Class Code (BCC):** Identifies the Base Class Code of an external IDE controller device driver.
23:16	1h RO	**Sub-Class Code (SCC):** Identifies the Sub-Class Code of an external IDE controller device driver.
15:8	85h RO	**Programming Interface (PI):** Identifies the Programming Interface of an IDE controller device driver.
7:0	-- RO/V	**Revision ID (RID):** This register specifies a device specific revision identifier. Refer to Device and Revision ID table in Vol1 for specific value.

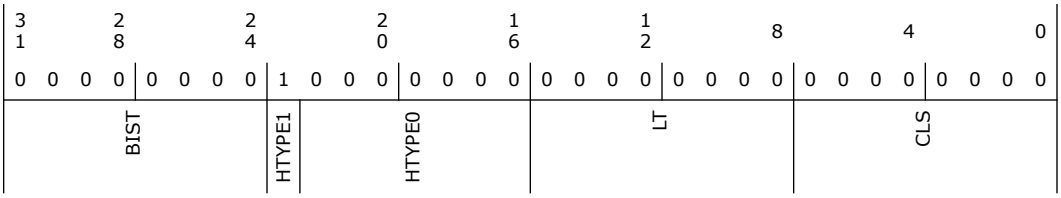
19.1.4 BIST, Header Type, Latency Timer, and Cache Line Size (IDE_HOST_BIST_HTYPE_LT_CLS)—Offset Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 2

Default: 800000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Built In Self Test (BIST):** Not implemented. Hardwired to 0.
23	1h RO/V	**Header Type 1 (HTYPE1):** This bit identifies whether or not the device contains multiple functions. - If the bit is 0, then the device is single function. - If the bit is 1, then the device has multiple functions.
22:16	0h RO	**Header Type 0 (HTYPE0):** Hardwired to 0 to identify the non-bridge Configuration Space Header.
15:8	0h RO	**Latency Timer (LT):** Not implemented. Hardwired to 0.
7:0	0h RO	**Cache Line Size (CLS):** Not implemented. Hardwired to 0.

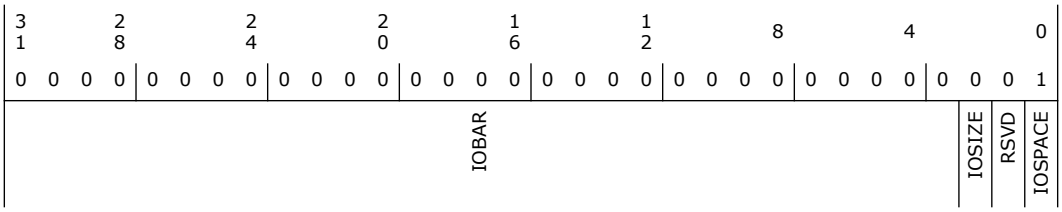
19.1.5 IDE Primary Command Block IO BAR (IDE_HOST_PCMDIOBAR)—Offset 10h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 2

Default: 1h



Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RW	**IO BAR (IOBAR):** Software programs this space with the base address of the device's IO region
2	0h RO	**IO Size (IOSIZE):** Hardwired to 0 to indicate 8B of IO space
1	0h RO	Reserved.
0	1h RO	**IO Space Indicator (IOSPACE):** Hardwired to 1 to identify an IO BAR.

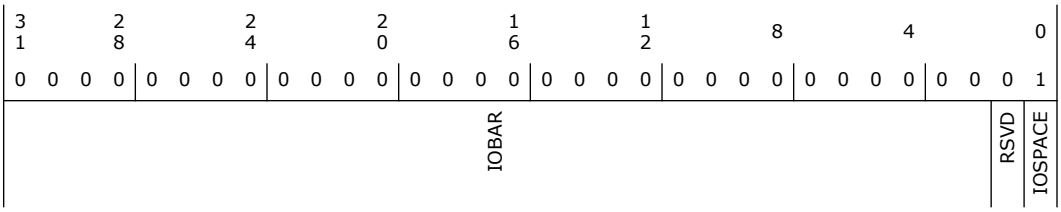
19.1.6 IDE Primary Control Block IO BAR (IDE_HOST_PCTLIOBAR)—Offset 14h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 2

Default: 1h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**IO BAR (IOBAR):** Software programs this space with the base address of the device's IO region
1	0h RO	Reserved.
0	1h RO	**IO Space Indicator (IOSPACE):** Hardwired to 1 to identify an IO BAR.

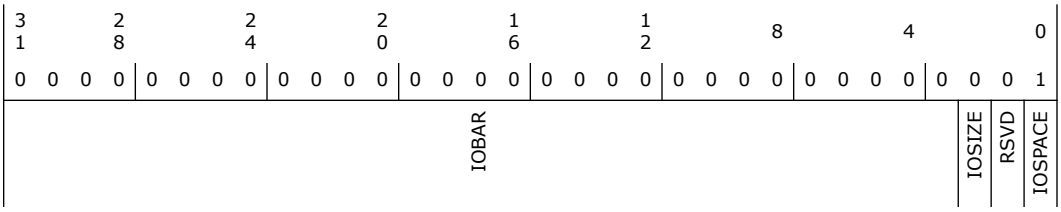
19.1.7 IDE Secondary Command Block IO BAR (IDE_HOST_SCMDIOBAR)—Offset 18h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 2

Default: 1h



Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RW	**IO BAR (IOBAR):** Software programs this space with the base address of the device's IO region
2	0h RO	**IO Size (IOSIZE):** Hardwired to 0 to indicate 8B of IO space
1	0h RO	Reserved.
0	1h RO	**IO Space Indicator (IOSPACE):** Hardwired to 1 to identify an IO BAR.

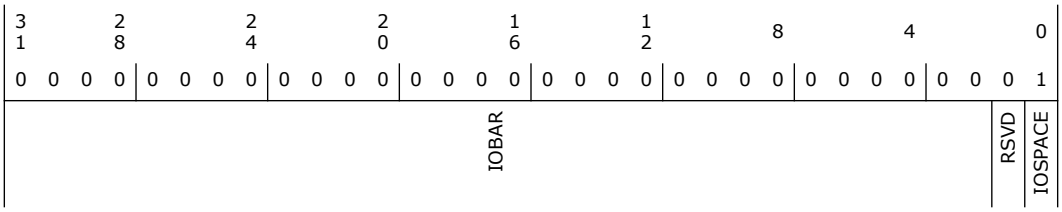
19.1.8 IDE Secondary Control Block IO BAR (IDE_HOST_SCTLIOBAR)—Offset 1Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 2

Default: 1h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**IO BAR (IOBAR):** Software programs this space with the base address of the device's IO region
1	0h RO	Reserved.
0	1h RO	**IO Space Indicator (IOSPACE):** Hardwired to 1 to identify an IO BAR.

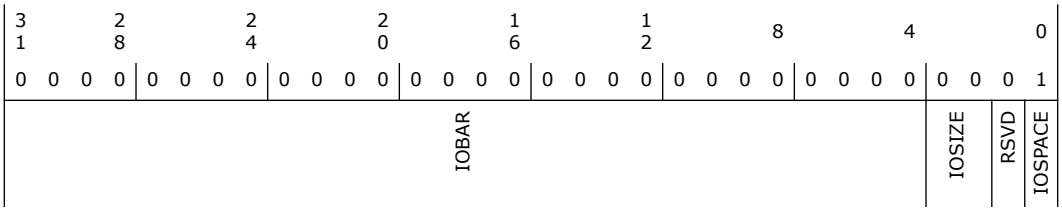
19.1.9 IDE Bus Master Block IO BAR (IDE_HOST_BMIOBAR)—Offset 20h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 2

Default: 1h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RW	**IO BAR (IOBAR):** Software programs this space with the base address of the device's IO region
3:2	0h RO	**IO Size (IOSIZE):** Hardwired to 0 to indicate 16B of IO space
1	0h RO	Reserved.
0	1h RO	**IO Space Indicator (IOSPACE):** Hardwired to 1 to identify an IO BAR.

19.1.10 Subsystem ID and Subsystem Vendor ID (IDE_HOST_SID_SVID)—Offset 2Ch

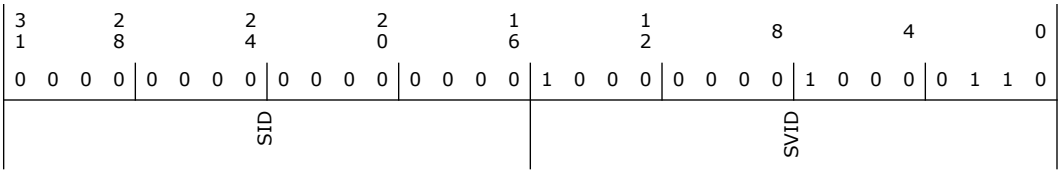
These registers are used to uniquely identify the add-in card or subsystem where the PCI device resides. They provide a mechanism for add-in card vendors to distinguish their add-in cards from one another even though the add-in cards may have the same PCI controller on them (and, therefore, the same Vendor ID and Device ID).

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 2

Default: 8086h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW/O	**Subsystem ID (SID):** Value of this field is vendor-specific. This is written by BIOS. No hardware action will be taken on this value.
15:0	8086h RW/O	**Subsystem Vendor ID (SVID):** This field identifies the vendor of the add-in card or subsystem. This is written by BIOS. No hardware action will be taken on this value.

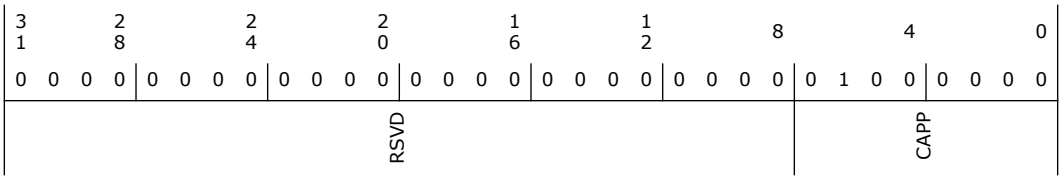
19.1.11 Capabilities List Pointer (IDE_HOST_CAPP)—Offset 34h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 2

Default: 40h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	40h RO	**Capabilities Pointer (CAPP):** Indicates the pointer for the first entry in the capabilities list which is the MSI Capability.

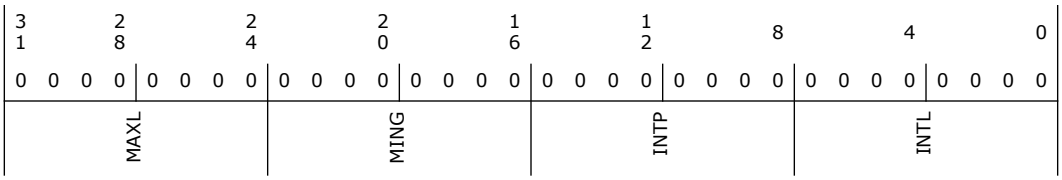
19.1.12 Maximum Latency, Minimum Grant, Interrupt Pin and Interrupt Line (IDE_HOST_MAXL_MING_INTP_INTL)—Offset 3Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Maximum Latency (MAXL):** Not implemented. Hardwired to 0.
23:16	0h RO	**Minimum Grant (MING):** Not implemented. Hardwired to 0.
15:8	0h RO/V	**Interrupt Pin (INTP):** This register specifies which interrupt pin IDE uses in PCI interrupt mode. Value Decoding 00h The function does NOT use an interrupt pin. 01h INTA 02h INTB 03h INTC 04h INTD 05h - FFh Reserved.
7:0	0h RW	**Interrupt Line (INTL):** The value written in this register indicates which input of the system interrupt controller, the device's interrupt pin is connected to. This value is used by the operating system and the device driver, and has no affect on the hardware

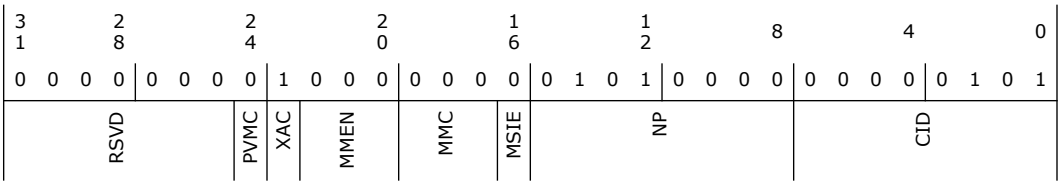
19.1.13 MSI Message Control, Next Pointer and Capability ID (IDE_HOST_MSIMC_MSINP_MSICID)—Offset 40h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 2

Default: 805005h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	Reserved.
24	0h RO	**Per Vector Masking Capable (PVMC):** Not implemented. Hardwired to 0 to indicate the function does NOT support MSI per-vector masking.
23	1h RO	**64 bit address capable (XAC):** Hardwired to 1 to indicate the function is capable of sending a 64-bit message address.
22:20	0h RW	**Multiple Message Enable (MMEN):** Encoded number of interrupt vectors allocated by SW. This field is RW for software compatibility, but only one interrupt vector is ever sent by the function.
19:17	0h RO	**Multiple Message Capable (MMC):** Encoded number of interrupt vectors requested by a device. Hardwired to 0 to indicate one requested interrupt vector.
16	0h RW	**MSI Enable (MSIE):** If set, MSI interrupt delivery is enabled whereas pin-based interrupt delivery SHALL be disabled. If cleared, prior to returning the configuration write (that clears this field) completion, the function must send any pending MSI(s).
15:8	50h RO	**Next Item Pointer (NP):** Indicates the pointer for the next entry in the capabilities list. Hardwired to 50h to point to the PM Capability list
7:0	5h RO	**Capability ID (CID):** Hardwired to 05h to indicate the linked list item as the MSI Capability registers

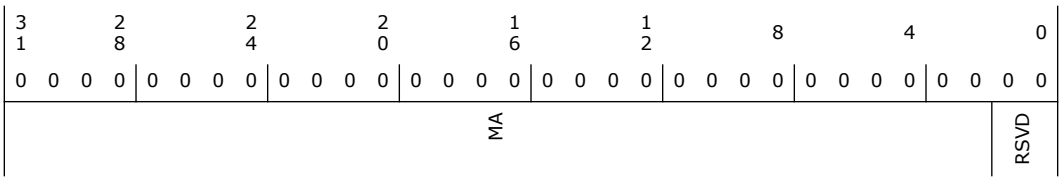
19.1.14 MSI Message Address (IDE_HOST_MSIMA)—Offset 44h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**Message Address (MA):** 32-bit DW-aligned MSI message address.
1:0	0h RO	Reserved.

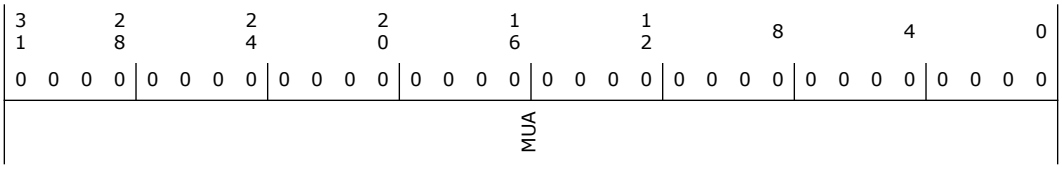
19.1.15 MSI Message Upper Address (IDE_HOST_MSIMUA)—Offset 48h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Message Upper Address (MUA):** Upper 32-bit of a 64-bit DW-aligned MSI message address.

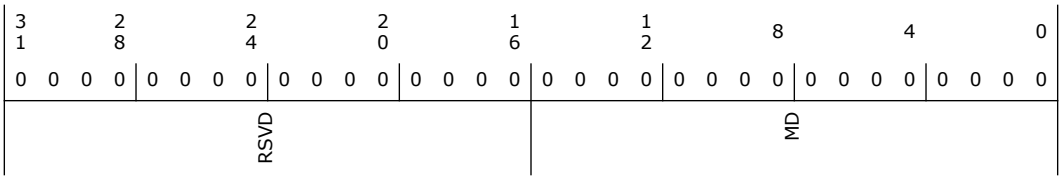
19.1.16 MSI Message Data (IDE_HOST_MSIMD)—Offset 4Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	0h RW	**Message Data (MD):** MSI Message Data

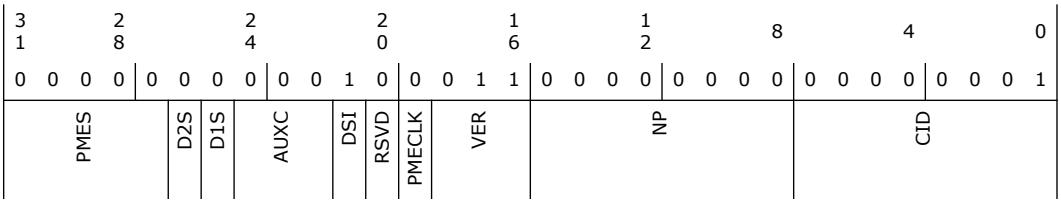
19.1.17 Power Management Capabilities, Next Pointer and Capability ID (IDE_HOST_PMCAP_PMNP_PMCID)—Offset 50h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 2

Default: 230001h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**PME Support (PMES):** This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. bit(27) X XXX1b - PME# can be asserted from D0 bit(28) X XX1Xb - PME# can be asserted from D1 bit(29) X X1XXb - PME# can be asserted from D2 bit(30) X 1XXXb - PME# can be asserted from D3hot bit(31) 1 XXXXb - PME# can be asserted from D3cold
26	0h RO	**D2 Support (D2S):** Hardwired to 0 to indicate that this device does not support D2
25	0h RO	**D1 Support (D1S):** Hardwired to 0 to indicate that this device does not support D1
24:22	0h RO	**Aux Current (AUXC):** Not implemented. Hardwired to 0.
21	1h RO	**Device Specific Initialization (DSI):** indicates whether special initialization of this function is required (beyond the standard PCI configuration header) before the generic class device driver is able to use it. A 1 indicates that the function requires a device specific initialization sequence following transition to the D0 uninitialized state. Hardwired to 1 to indicate Device Specific Initialization is required.
20	0h RO	Reserved.
19	0h RO	**PME Clock (PMECLK):** Not implemented. Hardwired to 0.

Bit Range	Default & Access	Field Name (ID): Description
18:16	3h RO	**Version (VER):** Hardwired to value of 011b indicates that this function complies with rev 1.2 of PCI Power Management Interface Spec
15:8	0h RO	**Next Item Pointer (NP):** Indicates the pointer for the next entry in the capabilities list. Hardwired to 0 to indicate no more linked list item.
7:0	1h RO	**Capability ID (CID):** Hardwired to 01h to indicate the linked list item as the PCI Power Management registers

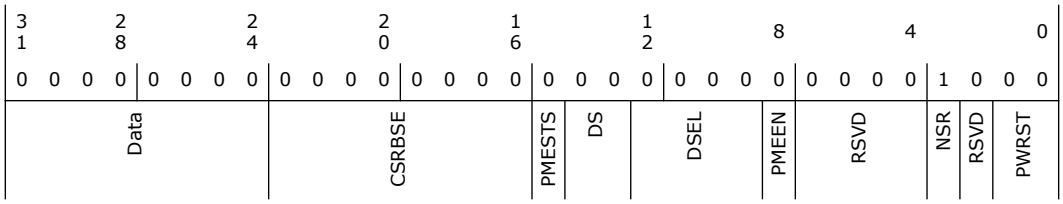
19.1.18 Power Management Data, Control/Status Register Bridge Support Extensions, Control and Status (IDE_HOST_PMD_PMCSRBSE_PMCSR)—Offset 54h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 2

Default: 8h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Data (Data):** Not implemented. Hardwired to 0.
23:16	0h RO	**Control/Status Register Bridge Support Extensions (CSRBSE):** Not implemented. Hardwired to 0.
15	0h RO	**PME Status (PMESTS):** Not implemented. Hardwired to 0.
14:13	0h RO	**Data Scale (DS):** Not implemented. Hardwired to 0.
12:9	0h RO	**Data Select (DSEL):** Not implemented. Hardwired to 0.
8	0h RO	**PME Enable (PMEEN):** Not implemented. Hardwired to 0.
7:4	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
3	1h RO	**No Soft Reset (NSR):** When set to 1, this bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved. Upon transition from the D3hot to the D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the PowerState bits.
2	0h RO	Reserved.
1:0	0h RW	**Power State (PWRST):** This 2-bit field is used both to determine the current power state of a function and to set the function into a new power state. The definition of the field values is given below: 00b - D0 01b - D1 10b - D2 11b - D3hot If software attempts to write an unsupported, optional state to this field, the write operation must complete normally on the bus; however, the data is discarded and no state change occurs.

§ §

20 Keyboard and Text (KT) (D22:F3)

20.1 Serial Port for Remote Keyboard and Text (KT) (D22:F3) Registers Summary

Table 20-1. Summary of Serial Port for Remote Keyboard and Text (KT) (D22:F3) Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	Device ID and Vendor ID (KT_HOST_DID_VID)—Offset 0h	X_8086h
4h	7h	Status and Command (KT_HOST_STS_CMD)—Offset 4h	B00000h
8h	Bh	Class Code and Revision ID (KT_HOST_CC_RID)—Offset 8h	70002XXh
Ch	Fh	BIST, Header Type, Latency Timer, and Cache Line Size (KT_HOST_BIST_HTYPE_LT_CLS)—Offset Ch	800000h
10h	13h	KT IO BAR (KT_HOST_IOBAR)—Offset 10h	1h
14h	17h	KT Memory BAR (KT_HOST_MEMBAR)—Offset 14h	0h
28h	2Bh	Cardbus CIS Pointer (KT_HOST_CCP)—Offset 28h	0h
2Ch	2Fh	Subsystem ID and Subsystem Vendor ID (KT_HOST_SID_SVID)—Offset 2Ch	8086h
30h	33h	Expansion ROM Base Address (KT_HOST_XRBAR)—Offset 30h	0h
34h	37h	Capabilities List Pointer (KT_HOST_CAPP)—Offset 34h	40h
3Ch	3Fh	Maximum Latency, Minimum Grant, Interrupt Pin and Interrupt Line (KT_HOST_MAXL_MING_INTP_INTL)—Offset 3Ch	0h
40h	43h	MSI Message Control, Next Pointer and Capability ID (KT_HOST_MSIMC_MSINP_MSICID)—Offset 40h	805005h
44h	47h	MSI Message Address (KT_HOST_MSIMA)—Offset 44h	0h
48h	4Bh	MSI Message Upper Address (KT_HOST_MSIMUA)—Offset 48h	0h
4Ch	4Fh	MSI Message Data (KT_HOST_MSIMD)—Offset 4Ch	0h
50h	53h	Power Management Capabilities, Next Pointer and Capability ID (KT_HOST_PMCAP_PMNP_PMCID)—Offset 50h	230001h
54h	57h	Power Management Data, Control/Status Register Bridge Support Extensions, Control and Status (KT_HOST_PMD_PMCSRBSE_PMCSR)—Offset 54h	8h

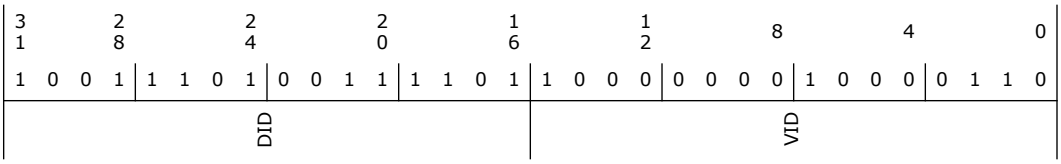
20.1.1 Device ID and Vendor ID (KT_HOST_DID_VID)—Offset 0h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 3

Default: X_8086h



Bit Range	Default & Access	Field Name (ID): Description
31:16	---- RO/V	**Device ID (DID):** This field identifies the particular device. See the Device and Version ID Table in Volume 1 for the default value.
15:0	8086h RO	**Vendor ID (VID):** This field identifies the manufacturer of the device. The value of 0x8086 indicates Intel.

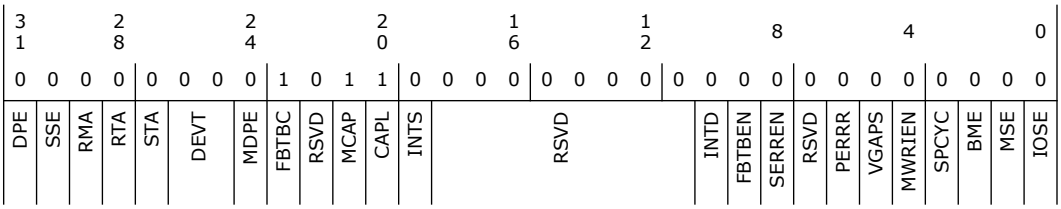
20.1.2 Status and Command (KT_HOST_STS_CMD)—Offset 4h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 3

Default: B00000h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Detected Parity Error (DPE):** Not implemented. Hardwired to 0.
30	0h RO	**Signaled System Error (SSE):** Not implemented. Hardwired to 0.
29	0h RW/1C/V	**Received Master Abort (RMA):** This bit must be set by a master device whenever its transaction (except for Special Cycle) is completed with Unsupported Request Completion Status (a.k.a. Master-Abort). All master devices must implement this bit.
28	0h RW/1C/V	**Received Target Abort (RTA):** This bit must be set by a master device whenever its transaction is completed with Completer Abort Completion Status (a.k.a. Target-Abort). All master devices must implement this bit.
27	0h RW/1C/V	**Signaled Target Abort (STA):** This bit must be set by a target device whenever it completes a Posted or Non-Posted transaction with a Completer Abort (a.k.a. Target-Abort) error. Devices that will never signal Completer Abort (a.k.a. Target-Abort) do not need to implement this bit.
26:25	0h RO	**Devsel Timing (DEVT):** These bits encode the timing of DEVSEL#. There are three allowable timings for assertion of DEVSEL# as described below: 00b: fast; 01b: medium; 10b: slow; 11b: reserved. These bits are read-only and must indicate the slowest time that a device asserts DEVSEL# for any bus command except Configuration Read and Configuration Write. Hardwired to 00b.

Bit Range	Default & Access	Field Name (ID): Description
24	0h RO	**Master Data Parity Error (MDPE):** Not implemented. Hardwired to 0.
23	1h RO	**Fast Back to Back Capable (FBTBC):** This bit indicates whether or not the target is capable of accepting fast back-to-back transactions when the transactions are not to the same agent. This bit can be set to 1 if the device can accept these transactions and must be set to 0 otherwise. Hardwired to 1.
22	0h RO	Reserved.
21	1h RO	**66 Mhz Capable (MCAP):** This bit indicates whether or not this device is capable of running at 66 MHz. A value of 0 indicates 33 MHz. A value of 1 indicates that the device is 66 MHz capable. Hardwired to 1.
20	1h RO	**Capabilities List (CAPL):** This optional read-only bit indicates whether or not this device implements the pointer for a New Capabilities linked list at offset 34h. A value of zero indicates that no New Capabilities linked list is available. A value of one indicates that the value read at offset 34h is a pointer in Configuration Space to a linked list of new capabilities.
19	0h RO	**Interrupt Status (INTS):** This read-only bit reflects the state of the interrupt in the device/function. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the device's/function's INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. Read-only and hardwired to 0 for a device that does NOT support pin-based interrupt.
18:11	0h RO	Reserved.
10	0h RW	**Interrupt Disable (INTD):** This bit disables the device/function from asserting INTx#. A value of 0 enables the assertion of its INTx# signal. A value of 1 disables the assertion of its INTx# signal. This bit's state after RST# is 0.
9	0h RO	**Fast Back to Back Enable (FBTBEN):** Not implemented. Hardwired to 0.
8	0h RO	**System Error Enable (SERREN):** Not implemented. Hardwired to 0.
7	0h RO	Reserved.
6	0h RO	**Parity Error Response (PERRR):** Not implemented. Hardwired to 0.
5	0h RO	**VGA Palette Snoop (VGAPS):** Not implemented. Hardwired to 0.
4	0h RO	**Memory Write and Invalidate Enable (MWRIEN):** Not implemented. Hardwired to 0.
3	0h RO	**Special Cycles (SPCYC):** Not implemented. Hardwired to 0.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Bus Master Enable (BME):** Controls the ability of a PCI device to issue Memory and I/O Read/Write Requests, and the ability of a PCI bridge to forward Memory and I/O Read/Write Requests in the Upstream direction. Devices: When this bit is Set, the PCI device function is allowed to issue Memory or I/O Requests. When this bit is Clear, the PCI device function is not allowed to issue any Memory or I/O Requests. Note that as MSI/MSI-X interrupt Messages are in-band memory writes, setting the Bus Master Enable bit to 0b disables MSI/MSI-X interrupt Messages as well. Requests other than Memory or I/O Requests are not controlled by this bit. Default value of this bit is 0b. This bit is hardwired to 0b if a PCI device function does not generate Memory or I/O Requests. Bridges: This bit controls forwarding of Memory or I/O Requests by a bridge in the Upstream direction. When this bit is 0b, Memory and I/O Requests received at the Downstream side of a bridge must be handled as Unsupported Requests (UR), and for Non-Posted Requests a Completion with UR completion status must be returned. This bit does not affect forwarding of Completions in either the Upstream or Downstream direction. The forwarding of Requests other than Memory or I/O Requests is not controlled by this bit. Default value of this bit is 0b.
1	0h RW	**Memory Space Enable (MSE):** Controls a device's response to Memory Space accesses. A value of 0 disables the device response. A value of 1 allows the device to respond to Memory Space accesses. State after RST# is 0.
0	0h RW	**IO Space Enable (IOSE):** Controls a device's response to I/O Space accesses. A value of 0 disables the device response. A value of 1 allows the device to respond to I/O Space accesses. State after RST# is 0.

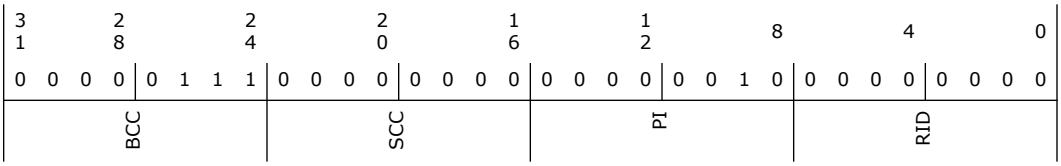
20.1.3 Class Code and Revision ID (KT_HOST_CC_RID)—Offset 8h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 3

Default: 70002xxh



Bit Range	Default & Access	Field Name (ID): Description
31:24	7h RO	**Base Class Code (BCC):** Identifies the Base Class Code of an external 16550-compatible serial controller device driver.
23:16	0h RO	**Sub-Class Code (SCC):** Identifies the Sub-Class Code of an external 16550-compatible serial controller device driver.
15:8	2h RO	**Programming Interface (PI):** Identifies the Programming Interface of an external 16550-compatible serial controller device driver.
7:0	---- RO/V	**Revision ID (RID):** Indicates stepping of the host controller. Refer to Device and Revision ID table in Vol1 for specific value.

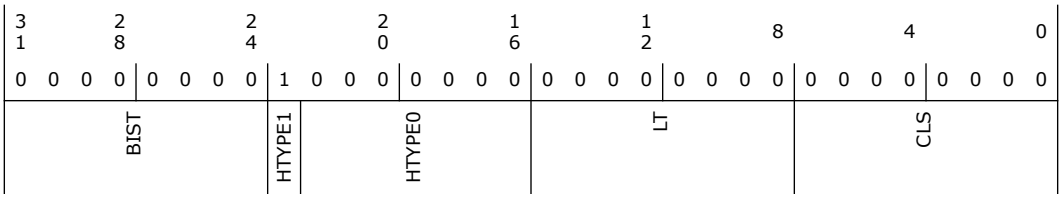
20.1.4 BIST, Header Type, Latency Timer, and Cache Line Size (KT_HOST_BIST_HTYPE_LT_CLS)—Offset Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 3

Default: 800000h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Built In Self Test (BIST):** Not implemented. Hardwired to 0.
23	1h RO/V	**Header Type 1 (HTYPE1):** This bit identifies whether or not the device contains multiple functions. - If the bit is 0, then the device is single function. - If the bit is 1, then the device has multiple functions.
22:16	0h RO	**Header Type 0 (HTYPE0):** This field identifies the layout of the second part of the predefined header (beginning at byte 10h in Configuration Space). - The encoding 00h specifies the non-bridge Configuration Space Header. - The encoding 01h specifies the PCI-to-PCI bridge Configuration Space Header. - The encoding 02h specifies the CardBus bridge Configuration Space Header. - All other encodings are reserved. Hardwired to 0 to identify the non-bridge Configuration Space Header.
15:8	0h RO	**Latency Timer (LT):** Not implemented. Hardwired to 0.
7:0	0h RO	**Cache Line Size (CLS):** Not implemented. Hardwired to 0.

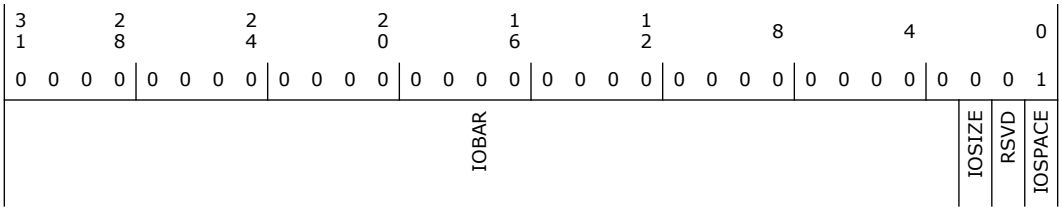
20.1.5 KT IO BAR (KT_HOST_IOBAR)—Offset 10h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 3

Default: 1h



Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RW	**IO BAR (IOBAR):** Software programs this space with the base address of the device's IO region
2	0h RO	**IO Size (IOSIZE):** Hardwired to 0 to indicate 8B of IO space
1	0h RO	Reserved.
0	1h RO	**IO Space Indicator (IOSPACE):** Hardwired to 1 to identify an IO BAR.

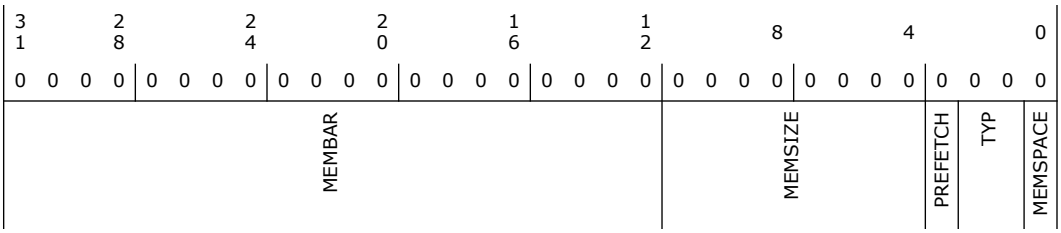
20.1.6 KT Memory BAR (KT_HOST_MEMBAR)—Offset 14h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW	**Memory BAR (MEMBAR):** Software programs this register with the base address of the device's memory region
11:4	0h RO	**Memory Size (MEMSIZE):** Hardwired to 0 to indicate 4KB of memory space
3	0h RO	**Prefetchable (PREFETCH):** A device can mark a range as prefetchable if there are no side effects on reads, the device returns all bytes on reads regardless of the byte enables. Hardwired to 0 to indicate the device's memory space as non-prefetchable.
2:1	0h RO	**Type (TYP):** Hardwired to 0 to indicate that Base register is 32 bits wide and mapping can be done anywhere in the 32-bit Memory Space.
0	0h RO	**Memory Space Indicator (MEMSPACE):** Hardwired to 0 to identify a Memory BAR.

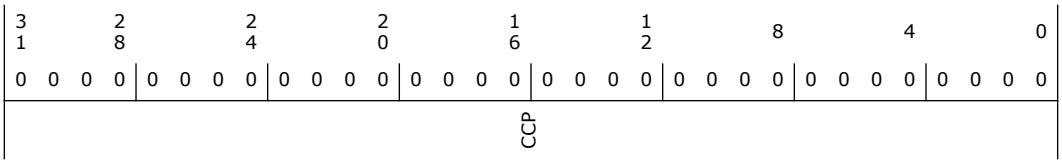
20.1.7 Cardbus CIS Pointer (KT_HOST_CCP)—Offset 28h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**Cardbus CIS Pointer (CCP):** Not implemented. Hardwired to 0.

20.1.8 Subsystem ID and Subsystem Vendor ID (KT_HOST_SID_SVID)—Offset 2Ch

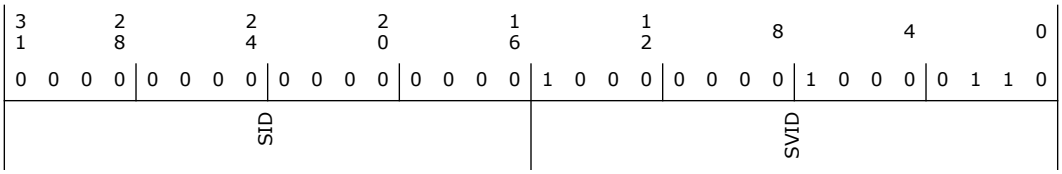
These registers are used to uniquely identify the add-in card or subsystem where the PCI device resides. They provide a mechanism for add-in card vendors to distinguish their add-in cards from one another even though the add-in cards may have the same PCI controller on them (and, therefore, the same Vendor ID and Device ID).

Access Method

Type: CFG Register (Size: 32 bits)

Device: 22
Function: 3

Default: 8086h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW/O	**Subsystem ID (SID):** Value of this field is vendor-specific. This is written by BIOS. No hardware action will be taken on this value. Implementation Note: The Write-Once lock must be implemented per field. SID should have its own lock.
15:0	8086h RW/O	**Subsystem Vendor ID (SVID):** This field identifies the vendor of the add-in card or subsystem. This is written by BIOS. No hardware action will be taken on this value. Implementation Note: The Write-Once lock must be implemented per field. SVID should have its own lock.

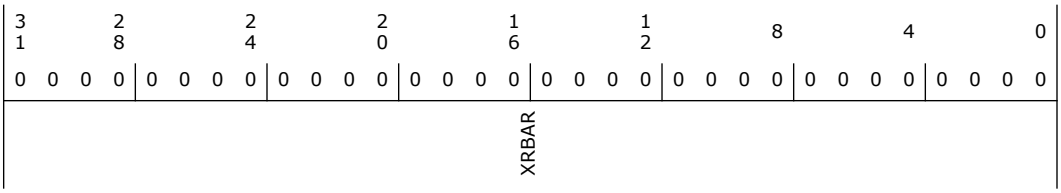
20.1.9 Expansion ROM Base Address (KT_HOST_XRBAR)—Offset 30h

Access Method

Type: CFG Register (Size: 32 bits)

Device: 22
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**Expansion ROM Base Address (XRBAR):** Not implemented. Hardwired to 0.

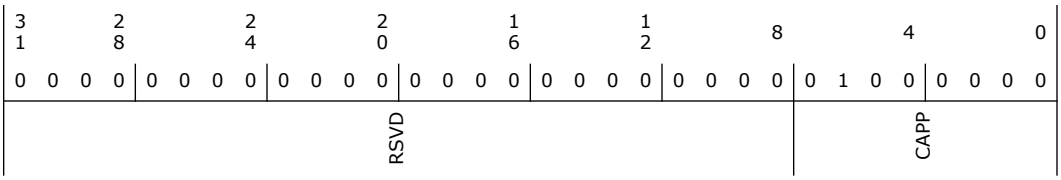
20.1.10 Capabilities List Pointer (KT_HOST_CAPP)—Offset 34h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 3

Default: 40h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	40h RO	**Capabilities Pointer (CAPP):** Indicates the pointer for the first entry in the capabilities list which is the MSI Capability.

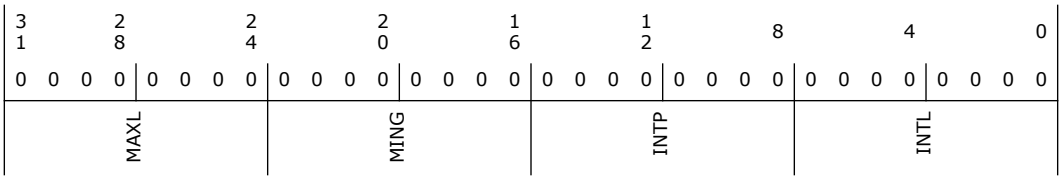
20.1.11 Maximum Latency, Minimum Grant, Interrupt Pin and Interrupt Line (KT_HOST_MAXL_MING_INTP_INTL)—Offset 3Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Maximum Latency (MAXL):** Not implemented. Hardwired to 0.
23:16	0h RO	**Minimum Grant (MING):** Not implemented. Hardwired to 0.
15:8	0h RO/V	**Interrupt Pin (INTP):** This register specifies which interrupt pin KT uses in PCI interrupt mode. Value Decoding 00h The function does NOT use an interrupt pin. 01h INTA 02h INTB 03h INTC 04h INTD 05h - FFh Reserved. Note: this field shadows the KTHIPINR.IPIN field in the PTIO Host private CR space which is configured by BIOS over IOSF SB.
7:0	0h RW	**Interrupt Line (INTL):** This register is used to communicate interrupt line routing information. POST software will write the routing information into this register as it initializes and configures the system. The value in this register tells which input of the system interrupt controller(s) the device's interrupt pin is connected to. The device itself does not use this value, rather it is used by device drivers and operating systems. Device drivers and operating systems can use this information to determine priority and vector information. Values in this register are system architecture specific.

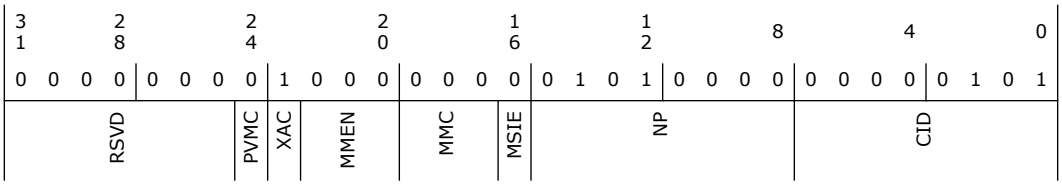
20.1.12 MSI Message Control, Next Pointer and Capability ID (KT_HOST_MSIMC_MSINP_MSICID)—Offset 40h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 3

Default: 805005h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	Reserved.
24	0h RO	**Per Vector Masking Capable (PVMC):** Not implemented. Hardwired to 0 to indicate the function does NOT support MSI per-vector masking.
23	1h RO	**64 bit address capable (XAC):** Hardwired to 1 to indicate the function is capable of sending a 64-bit message address.
22:20	0h RW	**Multiple Message Enable (MMEN):** Encoded number of interrupt vectors allocated by SW. This field is RW for software compatibility, but only one interrupt vector is ever sent by the function.
19:17	0h RO	**Multiple Message Capable (MMC):** Encoded number of interrupt vectors requested by a device. Hardwired to 0 to indicate one requested interrupt vector.
16	0h RW	**MSI Enable (MSIE):** If set, MSI interrupt delivery is enabled whereas pin-based interrupt delivery SHALL be disabled. If cleared, prior to returning the configuration write (that clears this field) completion, the function must send any pending MSI(s).
15:8	50h RO	**Next Item Pointer (NP):** Indicates the pointer for the next entry in the capabilities list. Hardwired to 50h to point to the PM Capability list
7:0	5h RO	**Capability ID (CID):** Hardwired to 05h to indicate the linked list item as the MSI Capability registers

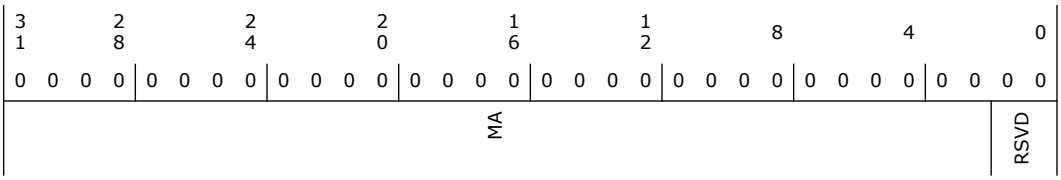
20.1.13 MSI Message Address (KT_HOST_MSIMA)—Offset 44h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**Message Address (MA):** 32-bit DW-aligned MSI message address.
1:0	0h RO	Reserved.

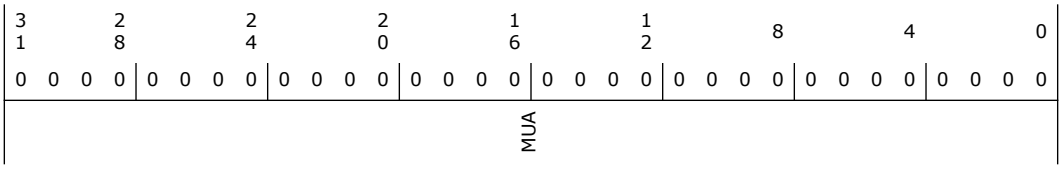
20.1.14 MSI Message Upper Address (KT_HOST_MSIMUA)—Offset 48h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Message Upper Address (MUA):** Upper 32-bit of a 64-bit DW-aligned MSI message address.

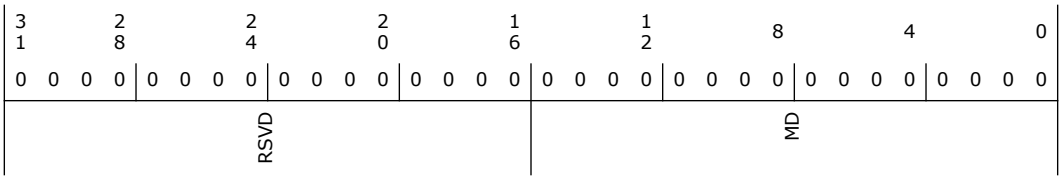
20.1.15 MSI Message Data (KT_HOST_MSIMD)—Offset 4Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	0h RW	**Message Data (MD):** MSI Message Data

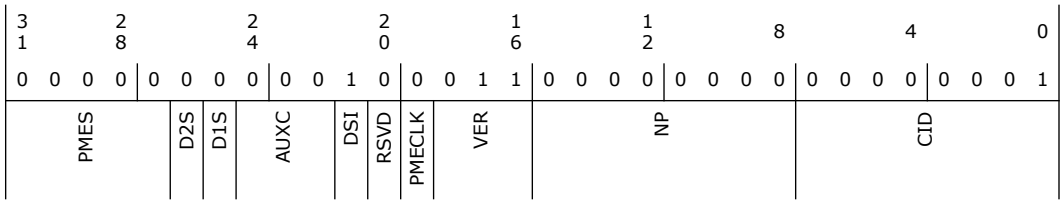
20.1.16 Power Management Capabilities, Next Pointer and Capability ID (KT_HOST_PMCAP_PMNP_PMCID)—Offset 50h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 3

Default: 230001h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**PME Support (PMES):** This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. bit(27) X XXX1b - PME# can be asserted from D0 bit(28) X XX1Xb - PME# can be asserted from D1 bit(29) X X1XXb - PME# can be asserted from D2 bit(30) X 1XXXb - PME# can be asserted from D3hot bit(31) 1 XXXXb - PME# can be asserted from D3cold
26	0h RO	**D2 Support (D2S):** Hardwired to 0 to indicate that this device does not support D2
25	0h RO	**D1 Support (D1S):** Hardwired to 0 to indicate that this device does not support D1
24:22	0h RO	**Aux Current (AUXC):** Not implemented. Hardwired to 0.
21	1h RO	**Device Specific Initialization (DSI):** indicates whether special initialization of this function is required (beyond the standard PCI configuration header) before the generic class device driver is able to use it. A 1 indicates that the function requires a device specific initialization sequence following transition to the D0 uninitialized state. Hardwired to 1 to indicate Device Specific Initialization is required.
20	0h RO	Reserved.
19	0h RO	**PME Clock (PMECLK):** Not implemented. Hardwired to 0.
18:16	3h RO	**Version (VER):** Hardwired to value of 011b indicates that this function complies with rev 1.2 of PCI Power Management Interface Spec
15:8	0h RO	**Next Item Pointer (NP):** Indicates the pointer for the next entry in the capabilities list. Hardwired to 0 to indicate no more linked list item.
7:0	1h RO	**Capability ID (CID):** Hardwired to 01h to indicate the linked list item as the PCI Power Management registers

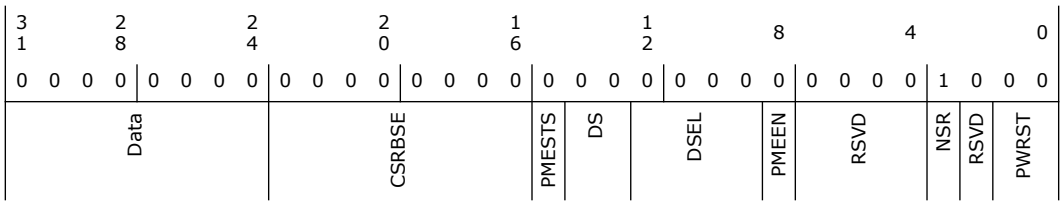
20.1.17 Power Management Data, Control/Status Register Bridge Support Extensions, Control and Status (KT_HOST_PMD_PMCSRBSE_PMCSR)—Offset 54h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 3

Default: 8h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Data (Data):** Not implemented. Hardwired to 0.
23:16	0h RO	**Control/Status Register Bridge Support Extensions (CSRBSE):** Not implemented. Hardwired to 0.
15	0h RO	**PME Status (PMESTS):** This bit is set when the function would normally assert the PME signal independent of the state of the PME_En bit. Writing a 1 to this bit will clear it and cause the function to stop asserting a PME (if enabled). Writing a 0 has no effect. If the function supports PME from D3cold, then this bit is sticky and must be explicitly cleared by the operating system each time the operating system is initially loaded. Not implemented. Hardwired to 0.
14:13	0h RO	**Data Scale (DS):** Not implemented. Hardwired to 0.
12:9	0h RO	**Data Select (DSEL):** Not implemented. Hardwired to 0.
8	0h RO	**PME Enable (PMEEN):** A 1 enables the function to assert PME. When 0, PME assertion is disabled. This bit defaults to 0 if the function does not support PME generation from D3cold. If the function supports PME from D3cold then this bit is sticky and must be explicitly cleared by the operating system each time it is initially loaded. Not implemented. Hardwired to 0.
7:4	0h RO	Reserved.
3	1h RO	**No Soft Reset (NSR):** When set to 1, this bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved. Upon transition from the D3hot to the D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the PowerState bits.
2	0h RO	Reserved.
1:0	0h RW	**Power State (PWRST):** This 2-bit field is used both to determine the current power state of a function and to set the function into a new power state. The definition of the field values is given below: 00b - D0 01b - D1 10b - D2 11b - D3hot If software attempts to write an unsupported, optional state to this field, the write operation must complete normally on the bus; however, the data is discarded and no state change occurs.

20.2 Keyboard and Text (KT) Additional Configuration Registers Summary

Table 20-2. Summary of Keyboard and Text (KT) Additional Configuration Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
54h	57h	Power Management Control and Status (KT_CSXE_PMD_PMCSRBSE_PMCSR)—Offset 54h	8h

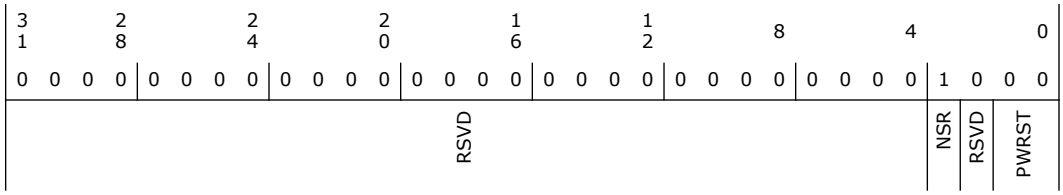
20.2.1 Power Management Control and Status (KT_CSXE_PMD_PMCSRBSE_PMCSR)—Offset 54h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 13
Function: 1

Default: 8h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3	1h RO	**No Soft Reset (NSR):** When set to 1, this bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved. Upon transition from the D3hot to the D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the PowerState bits.
2	0h RO	Reserved.
1:0	0h RW	**Power State (PWRST):** This 2-bit field is used both to determine the current power state of a function and to set the function into a new power state. The definition of the field values is given below: 00b - D0 01b - D1 10b - D2 11b - D3hot If software attempts to write an unsupported, optional state to this field, the write operation will complete normally on the bus; however, the data is discarded and no state change occurs.

§ §

21 USB Interface (D20: F0)

21.1 xHCI Configuration Registers Summary

Table 21-1. Summary of xHCI Configuration Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	1h	Vendor ID (VID)—Offset 0h	8086h
2h	3h	Device ID (DID)—Offset 2h	0h
4h	5h	Command (CMD)—Offset 4h	0h
6h	7h	Device Status (STS)—Offset 6h	290h
8h	8h	Revision ID (RID)—Offset 8h	0h
9h	9h	Programming Interface (PI)—Offset 9h	30h
Ah	Ah	Sub Class Code (SCC)—Offset Ah	3h
Bh	Bh	Base Class Code (BCC)—Offset Bh	Ch
Dh	Dh	Master Latency Timer (MLT)—Offset Dh	0h
Eh	Eh	Header Type (HT)—Offset Eh	0h
10h	17h	Memory Base Address (MBAR)—Offset 10h	4h
2Ch	2Dh	USB Subsystem Vendor ID (SSVID)—Offset 2Ch	0h
2Eh	2Fh	USB Subsystem ID (SSID)—Offset 2Eh	0h
34h	34h	Capabilities Pointer (CAP_PTR)—Offset 34h	70h
3Ch	3Ch	Interrupt Line (ILINE)—Offset 3Ch	0h
3Dh	3Dh	Interrupt Pin (IPIN)—Offset 3Dh	0h
40h	43h	XHC System Bus Configuration 1 (XHCC1)—Offset 40h	1FDh
44h	47h	XHC System Bus Configuration 2 (XHCC2)—Offset 44h	3C000h
50h	53h	Clock Gating (XHCLKGTEN)—Offset 50h	0h
58h	5Bh	Audio Time Synchronization (AUDSYNC)—Offset 58h	0h
60h	60h	Serial Bus Release Number (SBRN)—Offset 60h	30h
61h	61h	Frame Length Adjustment (FLADJ)—Offset 61h	60h
62h	62h	Best Effort Service Latency (BESL)—Offset 62h	0h
70h	70h	PCI Power Management Capability ID (PM_CID)—Offset 70h	1h
71h	71h	Next Item Pointer #1 (PM_NEXT)—Offset 71h	80h
72h	73h	Power Management Capabilities (PM_CAP)—Offset 72h	C1C2h
74h	75h	Power Management Control/Status (PM_CS)—Offset 74h	8h
80h	80h	Message Signaled Interrupt CID (MSI_CID)—Offset 80h	5h
81h	81h	Next item pointer (MSI_NEXT)—Offset 81h	0h
82h	83h	Message Signaled Interrupt Message Control (MSI_MCTL)—Offset 82h	86h
84h	87h	Message Signaled Interrupt Message Address (MSI_MAD)—Offset 84h	0h
88h	8Bh	Message Signaled Interrupt Upper Address (MSI_MUAD)—Offset 88h	0h

Table 21-1. Summary of xHCI Configuration Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
8Ch	8Dh	Message Signaled Interrupt Message Data (MSI_MD)—Offset 8Ch	0h
94h	97h	Vendor Specific Header (VSHDR)—Offset 94h	1400010h
A2h	A3h	Power Control Enable (PCE_REG)—Offset A2h	8h
A4h	A7h	High Speed Configuration 2 (HSCFG2)—Offset A4h	2000h
B0h	B3h	XHCI USB2 Overcurrent Pin Mapping N (U2OCM)—Offset B0h	0h
D0h	D3h	XHCI USB3 Overcurrent Pin Mapping N (U3OCM)—Offset D0h	0h

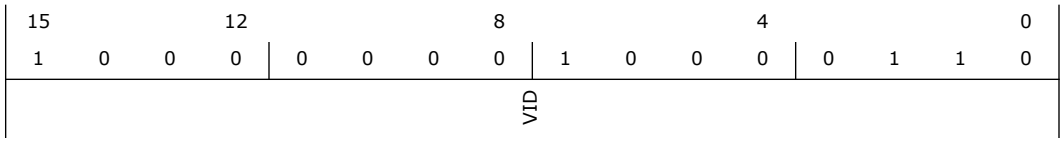
21.1.1 Vendor ID (VID)—Offset 0h

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 20
Function: 0

Default: 8086h



Bit Range	Default & Access	Field Name (ID): Description
15:0	8086h RO	**Vendor ID (VID):** 8086h indicates Intel.

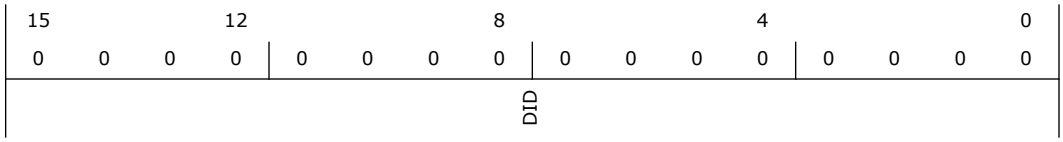
21.1.2 Device ID (DID)—Offset 2h

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 20
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RO/V	**Device ID (DID):** See the Device and Version ID Table in Volume 1 for the default value.

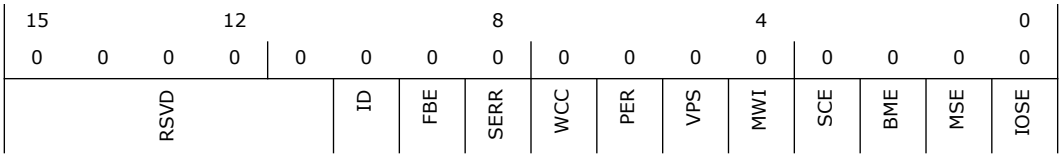
21.1.3 Command (CMD)—Offset 4h

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 20
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:11	0h RO	Reserved.
10	0h RW	**Interrupt Disable (ID):** When cleared to 0, the function is capable of generating interrupts. When 1, the function can not generate its interrupt to the interrupt controller. Note that the corresponding Interrupt Status bit is not affected by the interrupt enable.
9	0h RO	**Fast Back to Back Enable (FBE)**
8	0h RW	**SERR# Enable (SERR):** When set to 1, the XHC is capable of generating (internally) SERR#.
7	0h RO	**Wait Cycle Control (WCC)**
6	0h RW	**Parity Error Response (PER):** When set to 1, the XHCI Host Controller will check for correct parity (on its internal interface) and halt operation when bad parity is detected during the data phase as recommended by the XHCI specification. Note that this applies to both requests and completions from the system interface. This bit must be set in order for the parity errors to generate SERR#.
5	0h RO	**VGA Palette Snoop (VPS)**
4	0h RO	**Memory Write Invalidate (MWI)**
3	0h RO	**Special Cycle Enable (SCE)**

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Bus Master Enable (BME):** When set, it allows XHC to act as a bus master. When cleared, it disable XHC from initiating transactions on the system bus.
1	0h RW	**Memory Space Enable (MSE):** This bit controls access to the XHC Memory Space registers. If this bit is set, accesses to the XHC registers are enabled. The Base Address register for the XHC should be programmed before this bit is set.
0	0h RO	**I/O Space Enable (IOSE):** Reserved as 0. Read-Only.

21.1.4 Device Status (STS)—Offset 6h

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 20
Function: 0

Default: 290h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	0	1	0	0	1	0	0	0	0
DPE	SSE	RMA	RTA	STA	DEVT		MDPED	FBBC	UDF	MC	CL	IS	RSVD		

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1C	**Detected Parity Error (DPE):** This bit is set by the Intel PCH whenever a parity error is seen on the internal interface to the XHC host controller, regardless of the setting of bit 6 or bit 8 in the Command register or any other conditions. Software clears this bit by writing a 1 to this bit location.
14	0h RW/1C	**Signaled System Error (SSE):** This bit is set by the Intel PCH whenever it signals SERR# (internally). The SERR_EN bit (bit 8 in the Command Register) must be 1 for this bit to be set. Software clears this bit by writing a 1 to this bit location.
13	0h RW/1C	**Received Master-Abort Status (RMA):** This bit is set when XHC, as a master, receives a master-abort status on a memory access. This is treated as a Host Error and halts the DMA engines. Software clears this bit by writing a 1 to this bit location.
12	0h RW/1C	**Received Target Abort Status (RTA):** This bit is set when XHC, as a master, receives a target abort status on a memory access. This is treated as a Host Error and halts the DMA engines. Software clears this bit by writing a 1 to this bit location.
11	0h RW/1C	**Signaled Target-Abort Status (STA):** This bit is used to indicate when the XHC function responds to a cycle with a target abort.

Bit Range	Default & Access	Field Name (ID): Description
10:9	1h RO	**DEVSEL# Timing Status (DEVT):** This 2-bit field defines the timing for DEVSEL# assertion. Read-Only.
8	0h RW/1C	**Master Data Parity Error Detected (MDPED):** This bit is set by the Intel PCH whenever a data parity error is detected on a XHC read completion packet on the internal interface to the XHC host controller and bit 6 of the Command register is set to 1. Software clears this bit by writing a 1 to this bit location.
7	1h RO	**Fast Back-to-Back Capable (FBBC):** Reserved as 1 Read-Only.
6	0h RO	**User Definable Features (UDF):** Reserved as 0. Read-Only.
5	0h RO	**66 MHz Capable (MC):** Reserved as 0. Read-Only.
4	1h RO	**Capabilities List (CL):** Hardwired to 1 indicating that offset 34h contains a valid capabilities pointer.
3	0h RO/V	**Interrupt Status (IS):** This read-only bit reflects the state of this function's interrupt at the input of the enable/disable logic. This bit is a 1 when the interrupt is asserted. This bit will be 0 when the interrupt is deasserted. The value reported in this bit is independent of the value in the Interrupt Enable bit.
2:0	0h RO	Reserved.

21.1.5 Revision ID (RID)—Offset 8h

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 20
Function: 0

Default: 0h

7			4				0
0	0	0	0	0	0	0	0
RID							

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RO/V	**Revision ID (RID):** Indicates stepping of the host controller. Refer to Device and Revision ID table in Volume 1 for specific value.

21.1.6 Programming Interface (PI)—Offset 9h

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 20
Function: 0

Default: 30h

7			4				0
0	0	1	1	0	0	0	0
PI							

Bit Range	Default & Access	Field Name (ID): Description
7:0	30h RO	**Programming Interface (PI):** A value of 30h indicates that this USB Host Controller conforms to the XHCI specification.

21.1.7 Sub Class Code (SCC)—Offset Ah

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 20
Function: 0

Default: 3h

7			4				0
0	0	0	0	0	0	1	1
SCC							

Bit Range	Default & Access	Field Name (ID): Description
7:0	3h RO	**Sub Class Code (SCC):** A value of 03h indicates that this is a Universal Serial Bus Host Controller.

21.1.8 Base Class Code (BCC)—Offset Bh

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 20
Function: 0

Default: Ch

7			4				0
0	0	0	0	1	1	0	0
BCC							

Bit Range	Default & Access	Field Name (ID): Description
7:0	Ch RO	**Base Class Code (BCC):** A value of 0Ch indicates that this is a Serial Bus controller.

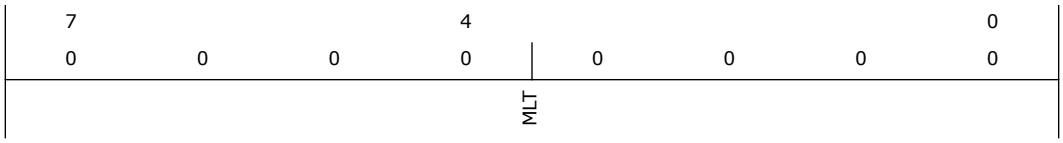
21.1.9 Master Latency Timer (MLT)—Offset Dh

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 20
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RO	**Master Latency Timer (MLT):** Because the XHC controller is internally implemented with arbitration on an internal interface, it does not need a master latency timer. The bits will be fixed at 0.

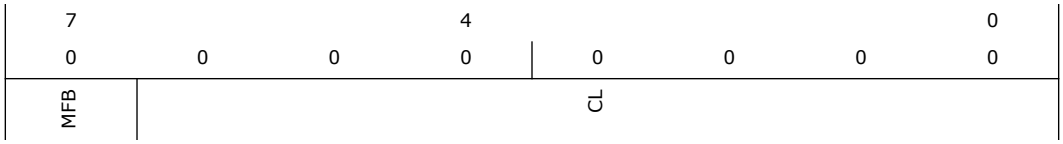
21.1.10 Header Type (HT)—Offset Eh

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 20
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Multi-Function Bit (MFB):** Read only indicating single function device.
6:0	0h RO	**Configuration layout (CL):** Hardwired to 0 to indicate a standard PCI configuration layout.

21.1.11 Memory Base Address (MBAR)—Offset 10h

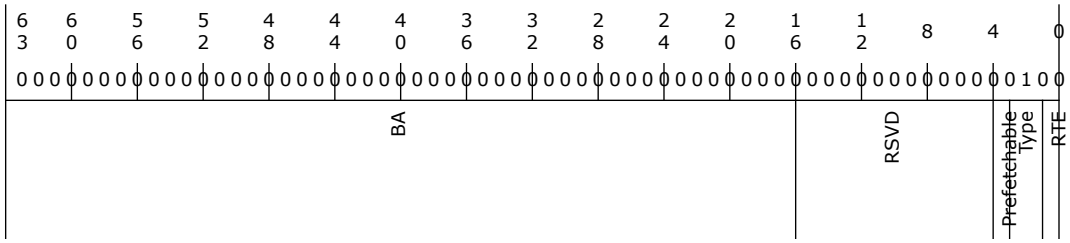
Value in this register will be different after the enumeration process.

Access Method

Type: CFG Register
(Size: 64 bits)

Device: 20
Function: 0

Default: 4h



Bit Range	Default & Access	Field Name (ID): Description
63:16	0h RW	**Base Address (BA):** Bits (63:16) correspond to memory address signals (63:16), respectively. This gives 64 KB of relocatable memory space aligned to 64 KB boundaries.
15:4	0h RO	Reserved.
3	0h RO	**Prefetchable (Prefetchable):** This bit is hardwired to 0 indicating that this range should not be prefetched.
2:1	2h RO	**Type (Type):** If this field is hardwired to 00 it indicates that this range can be mapped anywhere within 32-bit address space. If this field is hardwired to 10 it indicates that this range can be mapped anywhere within 64-bit address space.
0	0h RO	**Resource Type Indicator (RTE):** This bit is hardwired to 0 indicating that the base address field in this register maps to memory space

21.1.12 USB Subsystem Vendor ID (SSVID)—Offset 2Ch

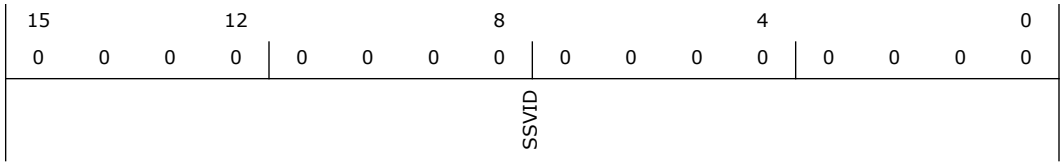
This register is modified and maintained by BIOS

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 20
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW/L	**USB Subsystem Vendor ID (SSVID):** This register, in combination with the USB Subsystem ID register, enables the operating system to distinguish each subsystem from the others.

21.1.13 USB Subsystem ID (SSID)—Offset 2Eh

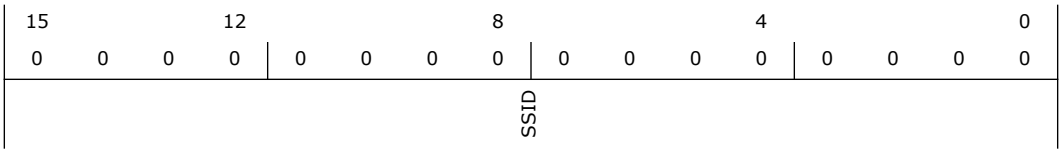
This register is modified and maintained by BIOS

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 20
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW/L	**USB Subsystem ID (SSID):** BIOS sets the value in this register to identify the Subsystem ID. This register, in combination with the Subsystem Vendor ID register, enables the operating system to distinguish each subsystem from other(s).

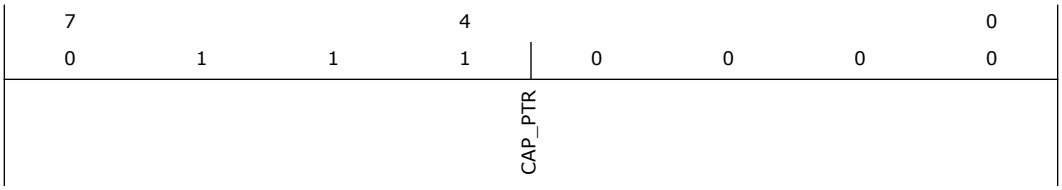
21.1.14 Capabilities Pointer (CAP_PTR)—Offset 34h

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 20
Function: 0

Default: 70h



Bit Range	Default & Access	Field Name (ID): Description
7:0	70h RO	**Capabilities Pointer (CAP_PTR):** This register points to the starting offset of the capabilities ranges.

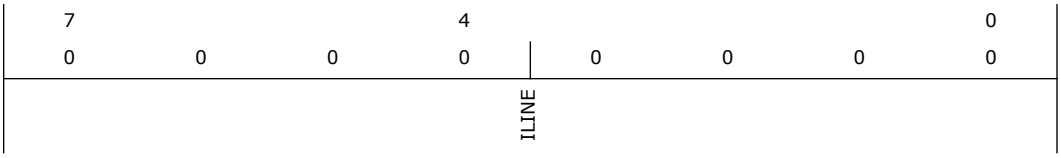
21.1.15 Interrupt Line (ILINE)—Offset 3Ch

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 20
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**Interrupt Line (ILINE):** This data is not used by the Intel PCH. It is used as a scratchpad register to communicate to software the interrupt line that the interrupt pin is connected to.

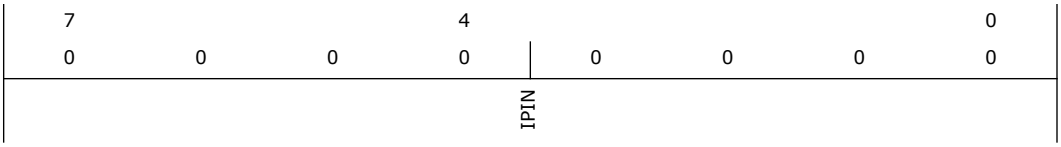
21.1.16 Interrupt Pin (IPIN)—Offset 3Dh

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 20
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW/L	**Interrupt pin (IPIN):** Bits 7:0 reflect the Interrupt Pin assigned to the host controller by the platform (and are hardwired).

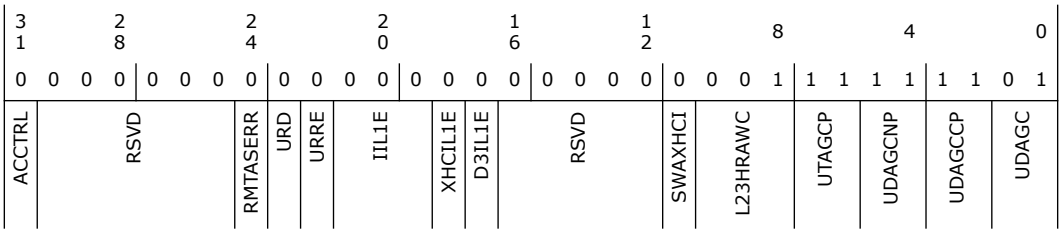
21.1.17 XHC System Bus Configuration 1 (XHCC1)—Offset 40h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 0

Default: 1FDh



Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/O	**Access Control (ACCTRL):** This bit is used by BIOS to lock/ unlock lockable bits. When set to '1' the write access to bits locked by this bit is disabled (locked state). When set to '0', the write access to bit locked by this bit is enabled (unlocked state). Writable once after platform reset.
30:25	0h RO	Reserved.
24	0h RW	**Master/Target Abort SERR (RMTASERR):** When set, it allows the out-of-band error reporting from the xHCI Controller to be reported as SERR# (if SERR# reporting is enabled) and thus set the STS.SSE bit.
23	0h RW/C	**Unsupported Request Detected (URD):** Set the HW when xHCI Controller received an unsupported request posted cycle. Cleared by SW when the bit is written with value of '1'.
22	0h RW	**Unsupported Request Report Enable (URRE):** When set this bit allows the URD bit to be reported as SERR# (if SERR# reporting is enabled) and thus set the STS.SSE bit.
21:19	0h RW	**Inactivity Initiated L1 Enable (IIL1E):** If programmed to non-zero, it allows L1 power managed to be enabled after the time-out period specified. 000: Disabled 001: 32 bb_cclk 010: 64 bb_cclk 011: 128 bb_cclk 100: 256 bb_cclk 101: 512 bb_cclk 110: 1024 bb_cclk 111: 131072 bb_cclk
18	0h RW	**XHC Initiated L1 Enable (XHCIL1E):** If set, allow the XHC initiated L1 power mangement to be enabled.
17	0h RW	**D3 Initiated L1 Enable (D3IL1E):** If set, allow PCI device state D3 initiated L1 power managment to be enables. This bit can only be set if the XHCI L1 Override P2 bit is set.
16:12	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW	**SW Assisted xHC Idle (SWAXHCI):** This bit being set will indicate xHC idleness (through SW means), which must be a '1' to allow L1 entry, and subsequently allow backbone clock to be gated. This bit is to be set by Intel xHCI driver after checking that the xHCI Controller will stay in idle state for a significant period of time, e.g. all ports disconnected. This bit can be cleared under the following conditions (see SWAXHCI Policy bits in xHC System Bus Configuration 2 register) SW: SW could write 0 to clear this bit.n HW: HW, under policy control, will clear this bit on an MMIO access to the Host Controller.n HW: HW, under policy control, will clear this bit when HW exits Idle state.
10:8	1h RW	**L23 to Host Reset Acknowledge Wait Count (L23HRAWC):** If programmed to non zero, it allows a wait period after the L23 PHY has shutdown before returning host reset acknowledge to PMC. 000: Disabled 001: 128 bb_cclk 010: 256 bb_cclk 011: 512 bb_cclk 100: 1024 bb_cclk 101: 2048 bb_cclk 110: 4096 bb_cclk 111: 131072 bb_cclk
7:6	3h RW	**Upstream Type Arbiter Grant Count Posted (UTAGCP):** Grant count for IOSF upstream L2 request type arbiter for posted type
5:4	3h RW	**Upstream Type Arbiter Grant Count Non Posted (UDAGCNP):** Grant count for IOSF upstream L2 type arbiter for non-posted type
3:2	3h RW	**Upstream Type Arbiter Grant Count Completion (UDAGCCP) (UDAGCCP):** Grant count for IOSF upstream L2 type arbiter for completion type
1:0	1h RW	**Upstream Device Arbiter Grant Count (UDAGC) (UDAGC):** Grant count for IOSF upstream L1 device arbiter

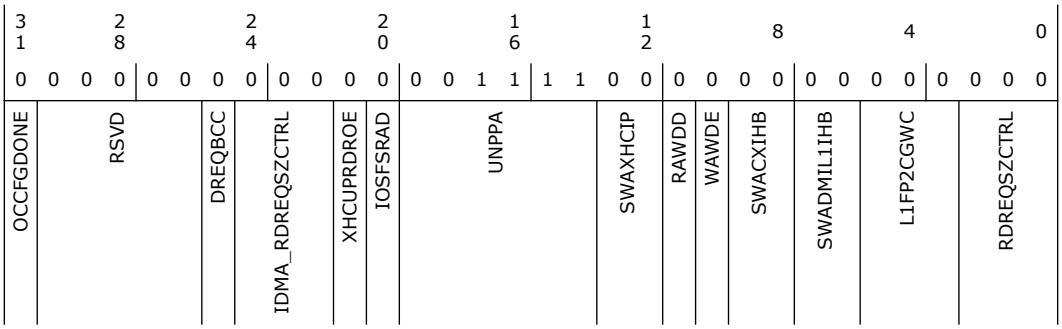
21.1.18 XHC System Bus Configuration 2 (XHCC2)—Offset 44h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 0

Default: 3C000h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**OC Configuration Done (OCCFGDONE):** This bit is used by BIOS to prevent spurious switching during OC configuration. It must be set by BIOS after configuration of the OC mapping bits is complete. Once this bit is set, OC mapping shall not be changed by SW.
30:26	0h RO	Reserved.
25	0h RW	**DMA Request Boundary Crossing Control (DREQBCC):** This bit controls the boundary crossing limit of each Read/Write Request. 0: 4KB 1: 64B
24:22	0h RW	**IDMA Read Request Size Control (IDMA_RDREQSZCTRL):** Read Request Size Control: This bit controls the maximum size of each Read Request. 000: 128B 001: 256B 011 - 110: Reserved 111: 64B
21	0h RW	**XHC Upstream Read Relaxed Ordering Enable (XHCUPRDROE):** This policy controls the Relaxed Ordering attribute for upstream reads. 0 - xHC will clear RO for all upstream read requests. 1 - xHC will set RO for all upstream read requests.
20	0h RW	**IOSF Sideband Register Access Disable (IOSFSRAD):** When set, it disables the IOSF sideband interface from accepting any host space register access.
19:14	Fh RW	**Upstream Non-Posted Pre-Allocation (UNPPA):** This field reserves data sizes, in 64 byte chunks, of the downstream completion resource. This value is zero based. 000000 - 111111: Pre-allocate 64 bytes - 4096 bytes If set greater than the default allows over-allocation If set less than default allows under-allocation Only allowed to be programmed when BME = 0 and no outstanding downstream completion

Bit Range	Default & Access	Field Name (ID): Description
13:12	0h RW	**SW Assisted xHC Idle Policy (SWAXHCIP):** Note: Irrespective of the setting of this field, SW write of 0 to SWAXHCI will clear the bit. 00b (default): xHC HW clears SWAXHCI bit upon MMIO access to Host Controller OR xHC HW exits Idle state 01b: xHC HW does not autonomously clear SWAXHCI bit. The bit could be cleared only by SW. 10b: xHC HW clears SWAXHCI upon MMIO acces to Host Controller. xHC HW exit from Idle state will not clear SWAXHCI. 11b: Reserved
11	0h RW	**MMIO Read After MMIO Write Delay Disable (RAWDD):** This field controls delay on MMIO Read after MMIO Write. 0b (Default): Delay MMIO Read after MMIO Write 1b: Do not delay MMIO Read after MMIO Write Note that this delay applies after the second of the two DW writes in the case where the IOSF Gasket splits a QW write into two single DW writes to the IP.
10	0h RW	**MMIO Write After MMIO Write Delay Enable (WAWDE):** This field controls delay on MMIO Write after previous MMIO Write. 0b (Default): Do not delay MMIO Write after previous MMIO Write 1b: Delay MMIO Write after previous MMIO Write Note that the delay count does not apply on the second of the two DW writes that are generated by IOSF Gasket when it splits a QW write into two. In other words, the second of the two DW writes could happen without any delay with respect to the first DW write. This choice is being made for ease of ECO. The delay count, in this case, will apply after the second of the two DW writes.
9:8	0h RW	**SW Assisted Cx Inhibit (SWACXIHB):** This field controls how the DMI L1 inhibit signal from USB3 to PMC will behave. 00: Never inhibit Cx 01: Inhibit Cx when Isochronous Endpoint is active (PPT Behavior) 10: Inhibit Cx when Periodic Active as defined in 40.4.3.2. 111: Always inhibit Cx

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RW	**SW Assisted DMI L1 Inhibit (SWADMIL1IHB):** This field controls how the DMI L1 inhibit signal from USB3 to DMI will behave. 00: Never inhibit DMI L1. 01: Inhibit DMI L1 when Isochronous Endpoint is active (PPT Behavior). 10: Inhibit DMI L1 when Priodic Active as defined in 40.4.3.2.1. 11: Inhibit DMI L1 if XHCC1.SWAXHCI = 0.
5:3	0h RW	**L1 Force P2 Clock Gating Wait Count (L1FP2CGWC):** If programmed to non zero, it allows L1 force P2 gating off the clock to be delayed after the time-out period specified. If wake up event is detected before the time-out, pclk remains alive and trigger L1 exit as though CPU host is causing the wake, 000: Disabled 001: 128 bb_cclk 010: 256 bb_cclk 011: 512 bb_cclk 100: 1024 bb_cclk 101: 2048 bb_cclk 110: 4096 bb_cclk 111: 131072 bb_cclk
2:0	0h RW	**Read Request Size Control (RDREQSZCTRL):** Read Request Size Control: This bit controls the maximum size of each Read Request. 000: 128B 001: 256B 010: 512B 011 - 110: Reserved 111: 64B

21.1.19 Clock Gating (XHCLKGTEN)—Offset 50h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 0

Default: 0h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD			NUEFBCGPS	SRAMPGTEN	SSLSE	USB2PLLSE	IOSFSTCGE	HSTCGE				SSTCGE				XHCIGEU3S	XHCFTCLKSE	XHCBBTCGIPISO	XHCHSTCGU2NRWE	XHCUSB2PLLSDLE	HSUXDMIPLLSE	SSPLLSUE			XHCBLCGE	HSLTCGE	SSLTCGE	IOSFBTCGE	IOSFBLCGE		

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	Reserved.
28	0h RW	**Naking USB2.0 EPs for Backbone Clock Gating and PLL Shutdown (NUEFBCGPS):** This field controls whether Naking USB2.0 EPs, once in Naking low priority schedule, should be considered as active for the considerations for backbone clock gating and PLL shutdown or not. 0: Naking USB2.0 EPs are not considered to be active for Backbone Clock Gating and PLL Shutdown evaluation. 1: Naking USB2.0 EPs are considered to be active for Backbone clock gating and PLL shutdown evaluation.
27	0h RW	**SRAM Power Gate Enable (SRAMPGTEN):** This register enables the SRAM Power Gating when PLL shutdown conditions for all clock domains have been met 0 - Disallow SRAM Power Gating. 1 - Allow SRAM Power Gating
26	0h RW	**SS Link PLL Shutdown Enable (SSLSE):** This register enables the SS P3 state to be exposed to PXP PLL Shutdown conditions on behalf of all USB SS Ports ontop of trunk clock gating. 0 - P3 state NOT allowed to result in PXP PLL shutdown. 1- P3 state allowed to result in PXP PLL shutdown
25	0h RW	**USB2 PLL Shutdown Enable (USB2PLLSE):** When set, this bit allows USB2 PLL to be shutdown when HS Link trunk clock is gated, and xHC can tolerate PLL spin up time for subsequent clock request. Note: if USB2 PLL Shutdown Disable Fuse is '1', hardware will always see '0' as an output from this register. BIOS reading this register should always return the correct value.
24	0h RW	**IOSF Sideband Trunk Clock Gating Enable (IOSFSTCGE):** When set, this bit allows the IOSF sideband clock trunk to be gated when idle conditions are met.
23:20	0h RW	**HS Backbone PXP Trunk Clock Gate Enable (HSTCGE):** This register determines the HS Ux state(s) which will be exposed to Backbone PXP trunk gating of core clock. Uy is a state allowed to result in trunk gating when ss_tcg_ux_en(x) is asserted. (0) ==) U0 or deeper (1) ==) NA (no support for U1) (2) ==) U2 (L1) or deeper (3) ==) U3 (L2) or deeper
19:16	0h RW	**SS Backbone PXP Trunk Clock Gate Enable (SSTCGE):** This register determines the SS Ux state(s) which will be exposed to Backbone PXP trunk gating of core clock. Uy is a state allowed to result in trunk gating when ss_tcg_ux_en(x) is asserted. (0) ==> U0 or deeper (1) ==> U1 or deeper (2) ==> U2 or deeper (3) ==> U3 or deeper

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**XHC Ignore_EU3S (XHCIGEU3S):** This register determines if the xHC will use the EU3S as a condition to allow for Frame timer gating. 0 - xHC may allow frame timer to be gated when EU3S is set and all ports are in the required state. 1 - xHC may allow frame timer to be gated regardless of EU3S.
14	0h RW	**XHC Frame Timer Clock Shutdown Enable (XHCFTCLKSE):** This register determines if the xHC will allow the frame timer clock to be gated. 0 - xHC will not allow ICC PLL 96MHz output to be shutdown thus keeping the frame timer running. 1 - xHC will allow ICC PLL 96MHz output to be shutdown under specific conditions.
13	0h RW	**XHC Backbone PXP Trunk Clock Gate In Presence of ISOCH EP (XHCBBTCGIPISO):** This register controls the policy on allowing Backbone PXP trunk clock gate in the presence of IDLE ISOCH EP s with active DB. Allows the periodic active to be used in enabling Backbone PXP trunk clock gating of core clock. 0 - Trunk gate of core clock is not allowed when ISOCH EP DB is set and ISOCH EP s are idle. 1 - Allow trunk gate of core clock when ISOCH EP DB is set and ISOCH EP s are idle.
12	0h RW	**XHC HS Backbone PXP Trunk Clock Gate U2 non RWE (XHCHSTCGU2NRWE):** This register controls the policy on allowing Backbone PXP trunk gating of core clock when there is atleast 1 non Remote Wake Enabled HS Port in U2. 0 - Prevent trunk gate of core clock when a non RWE HS Port is in U2. 1 - Allow trunk gate of core clock when a non RWE HS Port is in U2.
11:10	0h RW	**XHC USB2 PLL Shutdown Lx Enable (XHCUSB2PLLSDLE):** This register determines the HS Link state(s) which will be exposed to USB2 PLL Shutdown conditions on behalf of all USB2 HS Ports. Ly is a state allowed to result in USB2 PLL Shutdown when en(x) is asserted. (0) ==> L1 or deeper (1) ==> L2 or deeper
9:8	0h RW	**HS Backbone PXP PLL Shutdown Ux Enable (HSUXDMIPLLSE):** This register determines the Ux state(s) which will be exposed to PXP PLL Shutdown conditions. PLL Shutdown is allowed in: 00b Disabled (Link states shall be disabled for DMI PLL shutdown) 01b U0 or conditions for 10b setting. 10b U2 or conditions for 11b setting. 10b U3, Disconnected, Disabled or Powered-Off.

Bit Range	Default & Access	Field Name (ID): Description
7:5	0h RW	**SS Backbone PXP PLL Shutdown Ux Enable (SSPLLSUE):** This register determines the Ux state(s) which will be exposed to DMI PLL Shutdown conditions. PLL Shutdown is allowed in: 000b Disabled (Link states shall be ignored for DMI PLL shutdown). 001b U0 or conditions for 010b setting. 010b U1 or conditions for 011b setting. 011b U2 or conditions for 100b setting. 100b U3, Disconnected, Disabled or Powered-Off
4	0h RW	**XHC Backbone Local Clock Gating Enable (XHCBLCGE):** When set, this bit allows XHCI Controller IP backbone clock to be locally gated when idle conditions are met. Note: if XHC Dynamic Clock Gating Disable Fuse is '1', hardware will always see '0' as an output from this register. BIOS reading this register should always return the correct value.
3	0h RW	**HS Link Trunk Clock Gating Enable (HSLTCGE):** When set, this bit allows High Speed Link control's 480 MHz and its 48/60 MHz link clock trunk to be gated when idle conditions are met. Note: if XHC Dynamic Clock Gating Disable Fuse is '1', hardware will always see '0' as an output from this register. BIOS reading this register should always return the correct value. BIOS need to query fuses to see if HW is enabled.
2	0h RW	**SS Link Trunk Clock Gating Enable (SSLTCGE):** When set, this bit allows the SuperSpeed Link control's 250 MHz and its divided 125 MHz link clock trunk to ge gated when idle conditions are met. Note: if XHC Dynamic Clock Gating Disable Fuse is '1', hardware will always see '0' as an output from this register. BIOS reading this register should always return the correct value. BIOS need to query fuses to see if HW is enabled.
1	0h RW	**IOSF Backbone Trunk Clock Gating Enable (IOSFBTCGE):** When set, this bit allows the IOSF backbone clock trunk to be gated when idle conditions are met.
0	0h RW	**IOSF Gasket Backbone Local Clock Gating Enable (IOSFBLCGE):** When set, this bit allows the IOSF Gasket backbone clock to be locally gated when idle conditions are met. Note: if XHC Dynamic Clock Gating Disable Fuse is '1', hardware will always see '0' as an output from this register. BIOS reading this register should always return the correct value. BIOS need to query fuses to see if HW is enabled.

21.1.20 Audio Time Synchronization (AUDSYNC)—Offset 58h

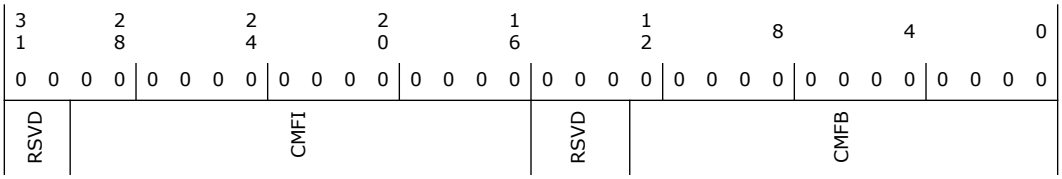
This 32 bit register is used for audio stream synchronization across different devices. Global signal sample_now captures a value in AUDSYNC register.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29:16	0h RO/V	**Captured Frame List Current Index/Frame Number (CMFI):** The value in this register is updated in response to sample_now signal. Bits (29:16) reflect state of bits (13:0) of FRINDEX
15:13	0h RO	Reserved.
12:0	0h RO/V	**Captured Micro-frame BLIF (CMFB):** The value is updated in response to sample_now signal and provides information about offset within micro-frame. Captured value represents number of 8 high-speed bit time units from start of micro-frame. At the beginning of micro-frame captured value will be 0 and increase to maximum value at the end. Default maximum value is 7499 but it may be changed as result of adjustment done in FLA.

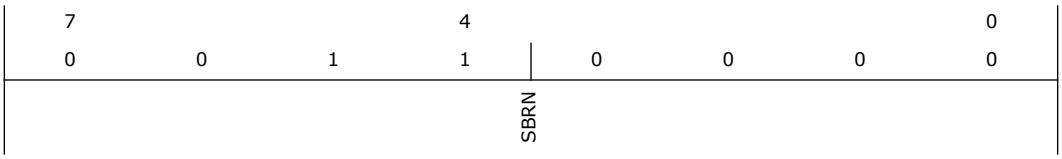
21.1.21 Serial Bus Release Number (SBRN)—Offset 60h

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 20
Function: 0

Default: 30h



Bit Range	Default & Access	Field Name (ID): Description
7:0	30h RO	**Serial Bus Release Number (SBRN):** A value of 30h indicates that this controller follows USB release 3.0.

21.1.22 Frame Length Adjustment (FLADJ)—Offset 61h

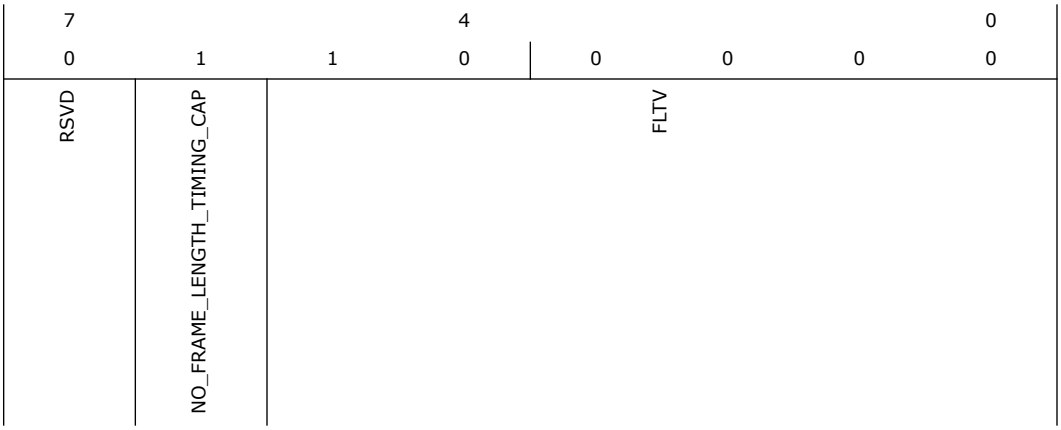
This feature is used to adjust any offset from the clock source that generates the clock that drives the SOF counter. When a new value is written into these six bits, the length of the frame is adjusted. Its initial programmed value is system dependent based on the accuracy of hardware USB clock and is initialized by system BIOS. This register should only be modified when the HChalted bit in the USBSTS register is a one. Changing value of this register while the host controller is operating yields undefined results.

Access Method

Type: CFG Register (Size: 8 bits)

Device: 20
Function: 0

Default: 60h



Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	Reserved.
6	1h RO	**No Frame Length Timing Capability (NO_FRAME_LENGTH_TIMING_CAP):** This flag is set to 1 to indicate that the host controller does not support a programmable Frame Length Timing Value field.
5:0	20h RO	**Frame Length Timing Value (FLTV):** SOF micro-frame length) is equal to 59488 + value in this field. The default value is decimal 32 (20h), which gives a SOF cycle time of 60000. Frame Length (number of High Speed bit times) FLADJ Value (decimal) (decimal) 59488 0 (00h) 59504 1 (01h) 59520 2 (02h) ... 59984 31 (1Fh) 60000 32 (20h) ... 60480 62 (3Eh) 60496 63 (3Fh) Each decimal value change to this register corresponds to 16 high-speed bit times. The SOF cycle time (number of SOF counter clock periods to generate a SOF micro-frame length) is equal to 59488 + value in this field. The default value is decimal 32 (20h), which gives a SOF cycle time of 60000. Frame Length (# High Speed bit times) FLADJ Value

21.1.23 Best Effort Service Latency (BESL)—Offset 62h

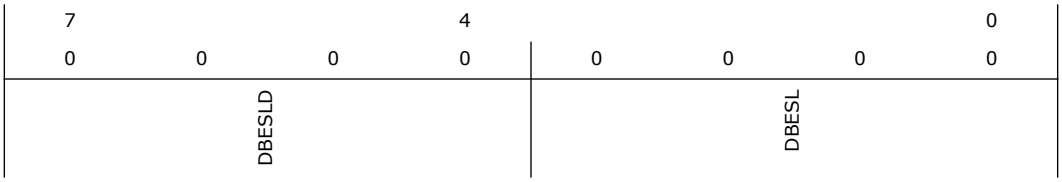
Bset Effort Service Latency.

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 20
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7:4	0h RW/L	**Default Best Effort Service Latency Deep (DBESLD):** Default Best Effort Service Latency (DBESLD) If the value of this field is non-zero, it defines the recommended value for programming the PORTPMSC register BESLD field. This is programmed by BIOS based on platform parameters.
3:0	0h RW/L	**Default Best Effort Service Latency (DBESL):** If the value of this field is non-zero, it defines the recommended value for programming the PORTPMSC register BESL field. This is programmed by BIOS based on platform parameters.

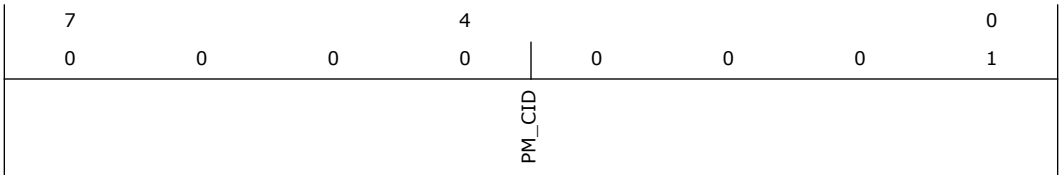
21.1.24 PCI Power Management Capability ID (PM_CID)—Offset 70h

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 20
Function: 0

Default: 1h



Bit Range	Default & Access	Field Name (ID): Description
7:0	1h RO	**PCI Power Management Capability ID (PM_CID):** A value of 01h indicates that this is a PCI Power Management capabilities field.

21.1.25 Next Item Pointer #1 (PM_NEXT)—Offset 71h

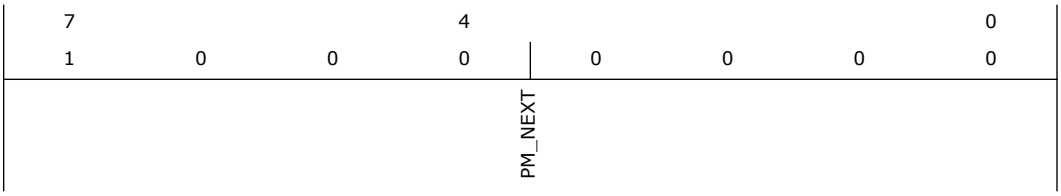
This register is modified and maintained by BIOS

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 20
Function: 0

Default: 80h



Bit Range	Default & Access	Field Name (ID): Description
7:0	80h RW/L	**Next Item Pointer #1 (PM_NEXT):** This register defaults to 80h, which indicates that the next capability registers begin at configuration offset 80h. This register is writable when the Access Control bit is set to '0'. This allows BIOS to effectively hide the next capability registers, if necessary. This register should only be written during system initialization before the plug-and-play software has enabled any master-initiated traffic. Values of: 80h implies next capability is MSI 00h implies that MSI capability is hidden. Note: This value is never expected to be programmed.

21.1.26 Power Management Capabilities (PM_CAP)—Offset 72h

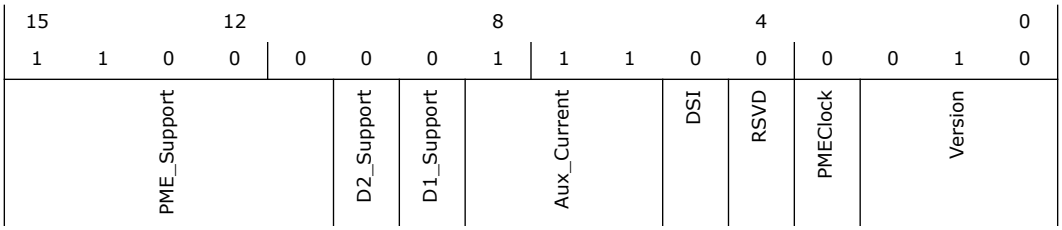
Normally, this register is read-only to report capabilities to the power management software. In order to report different power management capabilities depending on the system in which the Intel PCH is used, the write access to this register is controlled by the Access Control bit (ACCTRL). The value written to this register does not affect the hardware other than changing the value returned during a read. This register is modified and maintained by BIOS

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 20
Function: 0

Default: C1C2h



Bit Range	Default & Access	Field Name (ID): Description
15:11	18h RW/L	**PME_Support (PME_Support):** This 5-bit field indicates the power states in which the function may assert PME#. The Intel PCH XHC does not support the D1 or D2 states. For all other states, the Intel PCH XHC is capable of generating PME#. Software should never need to modify this field.
10	0h RW/L	**D2_Support (D2_Support):** The D2 state is not supported.
9	0h RW/L	**D1_Support (D1_Support):** The D1 state is not supported.
8:6	7h RW/L	**Aux_Current (Aux_Current):** The Intel PCH XHC reports 375mA maximum Suspend well current required when in the D3cold state. This value can be written by BIOS when a more accurate value is known.
5	0h RW/L	**DSI (DSI):** The Intel PCH reports 0, indicating that no device-specific initialization is required.
4	0h RO	Reserved.
3	0h RW/L	**PME Clock (PMEClock):** The Intel PCH reports 0, indicating that no PCI clock is required to generate PME#.
2:0	2h RW/L	**Version (Version):** The Intel PCH reports 010, indicating that it complies with Revision 1.1 of the PCI Power Management Specification.

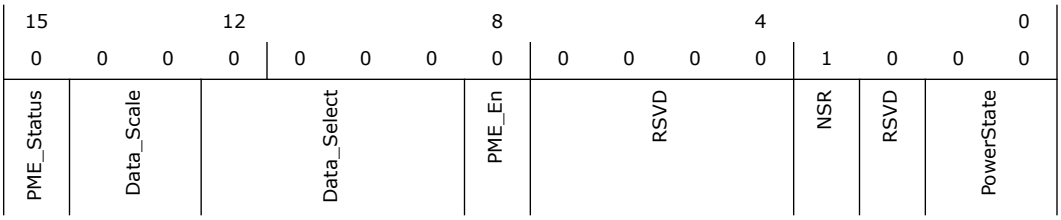
21.1.27 Power Management Control/Status (PM_CS)—Offset 74h

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 20
Function: 0

Default: 8h



Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1C	**PME_Status (PME_Status):** This bit is set when the Intel PCH XHC would normally assert the PME# signal independent of the state of the PME_En bit. Writing a 1 to this bit will clear it and cause the internal PME to deassert (if enabled). Writing a 0 has no effect. This bit must be explicitly cleared by the operating system each time the operating system is loaded.
14:13	0h RO	**Data_Scale (Data_Scale):** The Intel PCH hardwires these bits to 00 because it does not support the associated Data register.
12:9	0h RO	**Data_Select (Data_Select):** The Intel PCH hardwires these bits to 0000 because it does not support the associated Data register.
8	0h RW	**PME_En (PME_En):** A 1 enables the Intel PCH XHC to generate an internal PME signal when PME_Status is 1. This bit must be explicitly cleared by the operating system each time it is initially loaded.
7:4	0h RO	Reserved.
3	1h RO	**No Soft Reset (NSR):**), this bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved. Upon transition from the D3hot to the D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the PowerState bits. Transition from D3hot to D0 by a system or bus segment reset will return to the device state D0 Uninitialized with only PME context preserved if PME is supported and enabled.
2	0h RO	Reserved.
1:0	0h RW	**PowerState (PowerState):** This 2-bit field is used both to determine the current power state of XHC function and to set a new power state. The definition of the field values are: 00b - D0 state 11b - D3hot state If software attempts to write a value of 10b or 01b in to this field, the write operation must complete normally, however, the data is discarded and no state change occurs. When in the D3hot state, the Intel PCH must not accept accesses to the XHC memory range, but the configuration space must still be accessible.

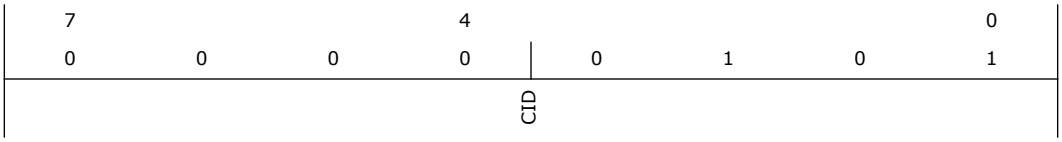
21.1.28 Message Signaled Interrupt CID (MSI_CID)—Offset 80h

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 20
Function: 0

Default: 5h



Bit Range	Default & Access	Field Name (ID): Description
7:0	5h RO	**Capability ID (CID):** Indicates that this is an MSI capability

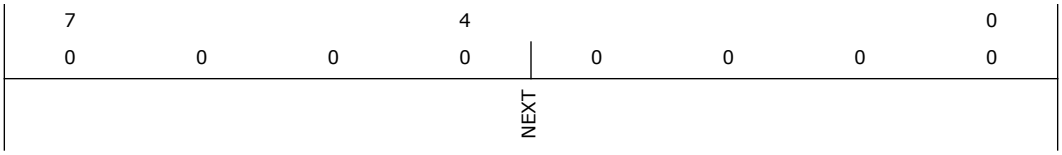
21.1.29 Next item pointer (MSI_NEXT)—Offset 81h

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 20
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RO	**Next Pointer (NEXT):** Indicates that this is the last item on the capability list

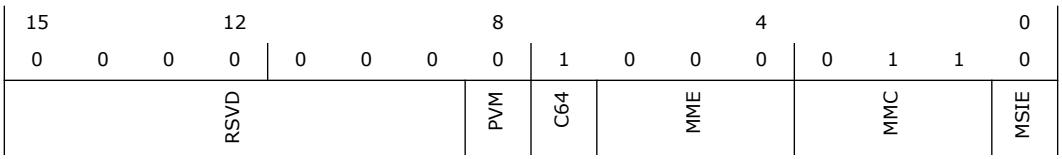
21.1.30 Message Signaled Interrupt Message Control (MSI_MCTL)—Offset 82h

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 20
Function: 0

Default: 86h



Bit Range	Default & Access	Field Name (ID): Description
15:9	0h RO	Reserved.
8	0h RO	**Per-Vector Masking Capable (PVM):** Specifies whether controller supports MSI per vector masking. Not supported
7	1h RO	**64 Bit Address Capable (C64):** Specifies whether capable of generating 64-bit messages. This device is 64-bit capable.
6:4	0h RW	**Multiple Message Enable (MME):** Indicates the number of messages the controller should assert. This device supports multiple message MSI.
3:1	3h RO	**Multiple Message Capable (MMC):** Indicates the number of messages the controller wishes to assert.This field must be set by HW to reflect the number of Interrupters supported. Encoding number of Vectors requested (number of Interrupters) 000 1 001 2 010 4 011 8 100 16 101 32 110-111 Reserved
0	0h RW	**MSI Enable (MSIE):** If set to 1, MSI is enabled and the traditional interrupt pins are not used to generate interrupts. If cleared to 0, MSI operation is disabled and the traditional interrupt pins are used.

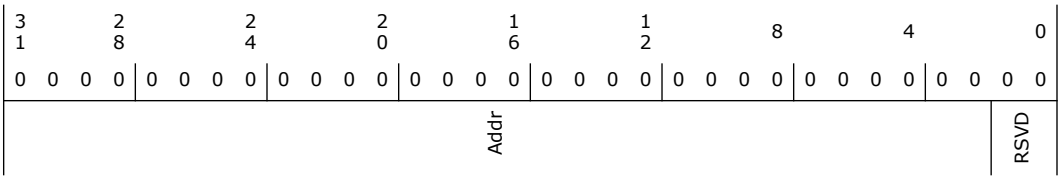
21.1.31 Message Signaled Interrupt Message Address (MSI_MAD)—Offset 84h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**Addr (Addr):** Lower DW of system specified message address, always DWORD aligned
1:0	0h RO	Reserved.

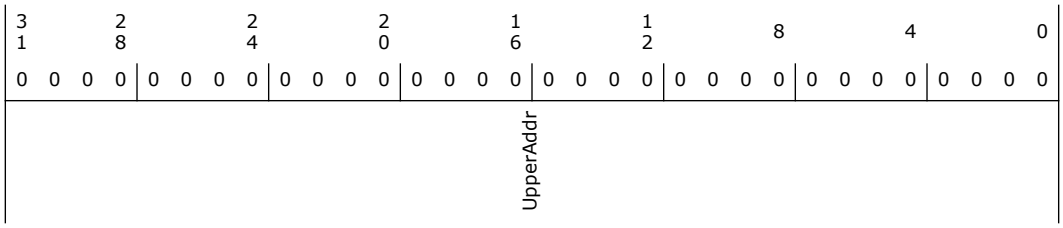
21.1.32 Message Signaled Interrupt Upper Address (MSI_MUAD)—Offset 88h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Upper Addr (UpperAddr):** Upper DW of system specified message address.

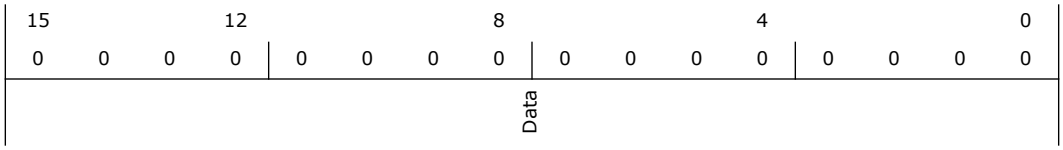
21.1.33 Message Signaled Interrupt Message Data (MSI_MD)—Offset 8Ch

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 20
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW	**Data (Data):** This 16-bit field is programmed by system software if MSI is enabled. Its content is driven onto the lower word (PCI AD(15:0)) during the data phase of the MSI memory write transaction. The Multiple Message Enable field (bits 6-4 of the Message Control register) defines the number of low order message data bits the function is permitted to modify to generate its system software allocated vectors. For example, a Multiple Message Enable encoding of 010 indicates the function has been allocated four vectors and is permitted to modify message data bits 1 and 0 (a function modifies the lower message data bits to generate the allocated number of vectors). If the Multiple Message Enable field is 000, the function is not permitted to modify the message data.

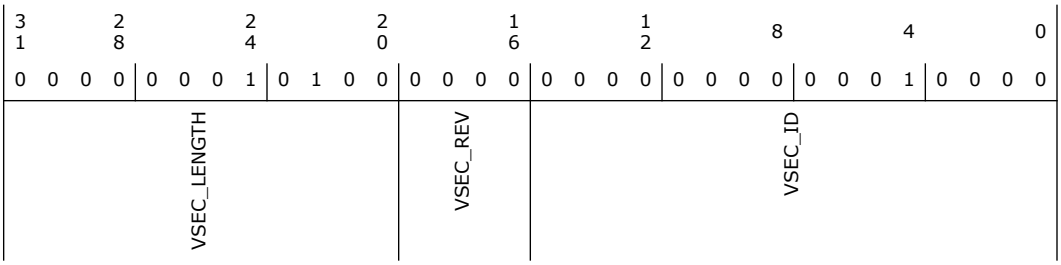
21.1.34 Vendor Specific Header (VSHDR)—Offset 94h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 0

Default: 1400010h



Bit Range	Default & Access	Field Name (ID): Description
31:20	14h RO	**VSEC Length (VSEC_LENGTH):** This field indicates the number of bytes in the entire VSEC structure, including the PCI Extended Capability header, the Vendor- Specific header, and the Vendor-Specific register
19:16	0h RO	**VSEC Rev (VSEC_REV):** This field is a vendor-defined version number that indicates the version of the VSEC structure. Software must qualify the Vendor ID and VSEC ID before interpreting this field.
15:0	10h RO	**VSEC ID (VSEC_ID):** This field is a vendor-defined ID number that indicates the nature and format of the VSEC structure. Software must qualify the Vendor ID before interpreting this field.

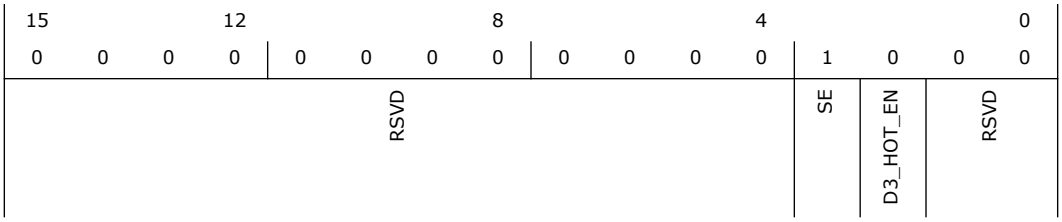
21.1.35 Power Control Enable (PCE_REG)—Offset A2h

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 20
Function: 0

Default: 8h



Bit Range	Default & Access	Field Name (ID): Description
15:4	0h RO	Reserved.
3	1h RW	**Sleep Enable (SE):** 0: xHCI will never asset Sleep 1: xHCI may assert Sleep during PG'ing. Note that some platforms may default this bit to '0', others to '1'.
2	0h RW	**D3 HOT ENABLE (D3_HOT_EN):** 0: xHCI will not power gate when idle 1: xHCI will power gate when idle
1:0	0h RO	Reserved.

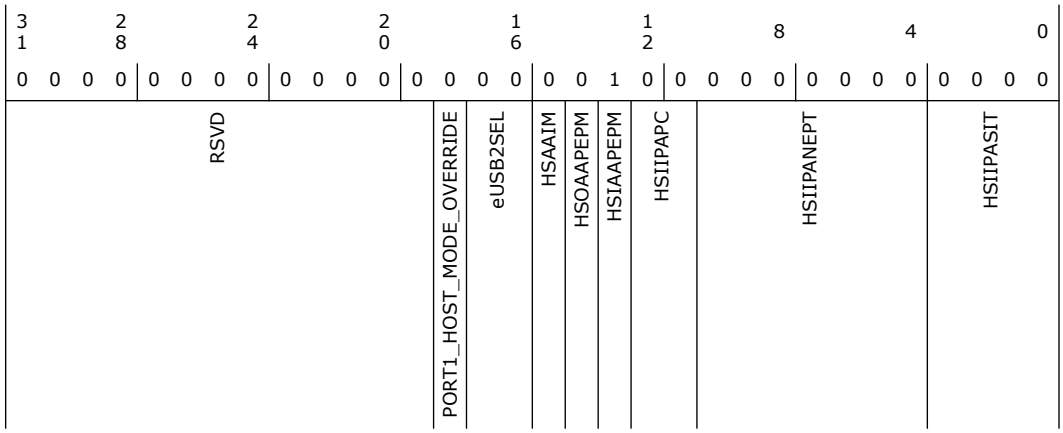
21.1.36 High Speed Configuration 2 (HSCFG2)—Offset A4h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 0

Default: 2000h



Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	Reserved.
18	0h RW	**PORT1_HOST_MODE_OVERRIDE (PORT1_HOST_MODE_OVERRIDE):** When set, this bit causes the Host_Device mux on port 1 to be forced into the Host mode.
17:16	0h RW	**eUSB2SEL (eUSB2SEL):** The two bits are associate with USB2 ports 1 - bit 16 and 2 - bit 2 0: Port is mapped to USB2 1: Port is mapped to eUSB2
15	0h RW	**HS ASYNC Active IN Mask (HSAAIM):** Determines if the Async Active will mask/ignore IN EP s. 0 HS ASYNC Active will include IN EP s. 1 HS ASYNC Active will mask/ignore IN EP s.
14	0h RW	**HS OUT ASYNC Active Polling EP Mask (HSOAAPEPM):** Determines if the Async Active for OUT HS/FS/LS masks/ignores EP s that are polling/PINGing (HS) due to NAK. 0 HS OUT ASYNC Active will include EP s that are polling. 1 HS OUT ASYNC Active will mask/ignore EP s that are polling.
13	1h RW	**HS IN ASYNC Active Polling EP Mask (HSIAAPEPM):** Determines if the Async Active for IN HS/FS/LS masks/ignores EP s that are polling due to NAK. 0 HS IN ASYNC Active will include EP s that are polling. 1 HS IN ASYNC Active will mask/ignore EP s that are polling.

Bit Range	Default & Access	Field Name (ID): Description
12:11	0h RW	**HS INTR IN Periodic Active Policy Control (HSIIPAPC):** Controls how the HS INTR IN periodic active is used to generate the global periodic active. This will determine how the smallest service interval among active EP s and number of active EP s are used. 0 HS INTR IN periodic active will be used to generate periodic active if Service Interval Threshold OR Numb of EP Threshold values meet the requirement. 1 HS INTR IN periodic active will be used to generate periodic active if Service Interval Threshold AND Numb of EP Threshold values meet the requirement. 2 Always allow HS INTR EP s to be used in the generation of the global Periodic Active indication. 3 Never allow HS INTR EP s to be used in the generation of the global Periodic Active indicaiton
10:4	0h RW	**HS INTR IN Periodic Active Num of EP Threshold (HSIIPANEPT):** Defines the threshold used to determine if Periodic Acive may include HS/FS/LS INTR IN EP active indication. If there are more than NumEPThreshold active HS/FS/LS INTR EP s then they may be included as part of the periodic active generation.
3:0	0h RW	**HS INTR IN Periodic Active Service Interval Threshold (HSIIPASIT):** Defines the Service Interval threshold used to determine if Periodic Acive will include HS/FS/LS INTR IN EP active indication. If there are any active HS/FS/LS INTR EP s with a service interval less than or equal to this threshold then they may be included as part of the periodic active generation.

21.1.37 XHCI USB2 Overcurrent Pin Mapping N (U2OCM)—Offset B0h

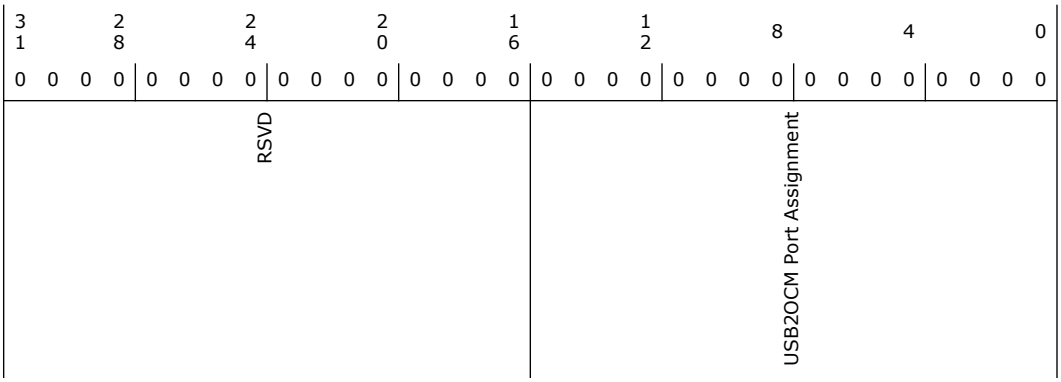
Address Offset: B0-B3h, ... (B0h+(NumOC-1)*4) to (B3h+(NumOC–1)*4)
The RW/L property of this register is controlled by OCCFDONE bit.
Each OC pin can be assigned to one or more of upto 32 Standard USB2 ports.
Each DWord maps one OC pin across upto 32 USB2 ports.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	0h RW/L	**USB2 Port Assignment OC Mapping (USB2OCM Port Assignment):** USB2 Port assignment Set to 1 to map port, Bit 0 maps to USB2 port 1 Bit 1 maps to USB2 port 2 Bit N maps to USB2 port N. The total number of USB2 ports will depend on the SKU. There are 8 OC registers. Each OC register will have the mapping above. Depending on the SKU the upper bits may not apply. Note: The USB-R port which is the most significant USB2 port does not have an OC pin. Thus the OC assignment for the USB-R port is ignored.

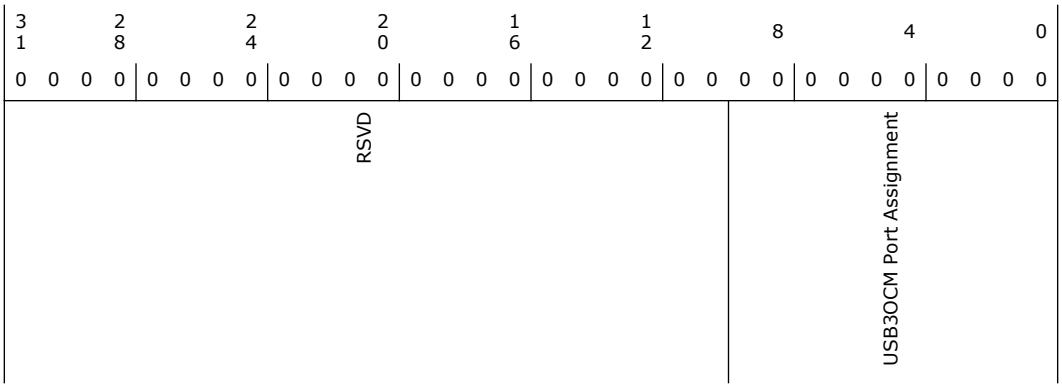
21.1.38 XHCI USB3 Overcurrent Pin Mapping N (U3OCM)—Offset D0h

Address Offset: D0-D3h, ... (D0h+(NumOC-1)*4) to (D3h+(NumOC–1)*4)
The RW/L property of this register is controlled by OCCFDONE bit.
Each OC pin can be assigned to one or more of upto 32 Standard USB2 ports.
Each DWord maps one OC pin across upto 32 USB2 ports.

Access Method

Type: CFG Register (Size: 32 bits)
Device: 20
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:0	0h RW/L	**USB3 Port Assignment OC Mapping (USB3OCM Port Assignment):** USB3 Port assignment When Set to 1, Bit 0 maps to USB3 port 1 Bit 1 maps to USB3 port 2 Bit N maps to USB3 port N. The total number of USB3 ports will depend on the SKU. There are 8 OC registers. Each OC register will have the mapping above.

21.2 xHCI Memory Mapped Registers Summary

Table 21-2. Summary of xHCI Memory Mapped Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	0h	Capability Registers Length (CAPLENGTH)—Offset 0h	20h
2h	3h	Host Controller Interface Version Number (HCIVERSION)—Offset 2h	100h
4h	7h	Structural Parameters 1 (HCSPARAMS1)—Offset 4h	1A000840h
8h	Bh	Structural Parameters 2 (HCSPARAMS2)—Offset 8h	14200054h
Ch	Fh	Structural Parameters 3 (HCSPARAMS3)—Offset Ch	40001h
10h	13h	Capability Parameters (HCCPARAMS)—Offset 10h	200077C1h
14h	17h	Doorbell Offset (DBOFF)—Offset 14h	3000h
18h	1Bh	Runtime Register Space Offset (RTSOFF)—Offset 18h	2000h
80h	83h	USB Command (USBCMD)—Offset 80h	0h
84h	87h	USB Status (USBSTS)—Offset 84h	1h
88h	8Bh	Page Size (PAGESIZE)—Offset 88h	1h
94h	97h	Device Notification Control (DNCTRL)—Offset 94h	0h
98h	9Bh	Command Ring Low (CRCR_LO)—Offset 98h	0h
9Ch	9Fh	Command Ring High (CRCR_HI)—Offset 9Ch	0h

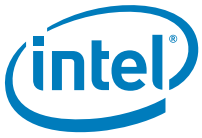


Table 21-2. Summary of xHCI Memory Mapped Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
B0h	B3h	Device Context Base Address Array Pointer Low (DCBAAP_LO)—Offset B0h	0h
B4h	B7h	Device Context Base Address Array Pointer High (DCBAAP_HI)—Offset B4h	0h
480h	483h	Port N Status and Control USB2 (PORTSCN)—Offset 480h	2A0h
484h	487h	Port Power Management Status and Control USB2 (PORTPMSCN)—Offset 484h	0h
48Ch	48Fh	Port N Hardware LPM Control Register (PORTHLPMCN)—Offset 48Ch	0h
540h	543h	Port Status and Control USB3 (PORTSCXUSB3)—Offset 540h	2A0h
544h	547h	Port Power Management Status and Control USB3 (PORTPMSCX)—Offset 544h	0h
548h	54Bh	USB3 Port X Link Info (PORTLIX)—Offset 548h	0h
2000h	2003h	Microframe Index (MFINDEX)—Offset 2000h	0h
2020h	2023h	Interrupter x Management (IMANx)—Offset 2020h	0h
2024h	2027h	Interrupter x Moderation (IMODx)—Offset 2024h	FA0h
2028h	202Bh	Event Ring Segment Table Size x (ERSTSZx)—Offset 2028h	0h
2030h	2033h	Event Ring Segment Table Base Address Low x (ERSTBA_LOx)—Offset 2030h	0h
2034h	2037h	Event Ring Segment Table Base Address High x (ERSTBA_HIx)—Offset 2034h	0h
2038h	203Bh	Event Ring Dequeue Pointer Low x (ERDP_LOx)—Offset 2038h	0h
203Ch	203Fh	Event Ring Dequeue Pointer High x (ERDP_HIx)—Offset 203Ch	0h
3000h	3003h	Door Bell x (DBx)—Offset 3000h	0h
8000h	8003h	XECP_SUPP_USB2_0 (XECP_SUPP_USB2_0)—Offset 8000h	2000802h
8004h	8007h	XECP_SUPP_USB2_1 (XECP_SUPP_USB2_1)—Offset 8004h	20425355h
8008h	800Bh	XECP_SUPP_USB2_2 (XECP_SUPP_USB2_2)—Offset 8008h	30181001h
8010h	8013h	XECP_SUPP_USB2_3 (Full Speed) (XECP_SUPP_USB2_3)—Offset 8010h	C0021h
8014h	8017h	XECP_SUPP_USB2_4 (Low Speed) (XECP_SUPP_USB2_4)—Offset 8014h	5DC0012h
8018h	801Bh	XECP_SUPP_USB2_5 (High Speed) (XECP_SUPP_USB2_5)—Offset 8018h	1E00023h
8020h	8023h	XECP_SUPP_USB3_0 (XECP_SUPP_USB3_0)—Offset 8020h	3001402h
8024h	8027h	XECP_SUPP_USB3_1 (XECP_SUPP_USB3_1)—Offset 8024h	20425355h
8028h	802Bh	XECP_SUPP_USB3_2 (XECP_SUPP_USB3_2)—Offset 8028h	30000A11h
8030h	8033h	XECP_SUPP_USB3_3 (XECP_SUPP_USB3_3)—Offset 8030h	4E00121h
8034h	8037h	XECP_SUPP_USB3_4 (XECP_SUPP_USB3_4)—Offset 8034h	9C00122h
8038h	803Bh	XECP_SUPP_USB3_5 (XECP_SUPP_USB3_5)—Offset 8038h	13800123h
803Ch	803Fh	XECP_SUPP_USB3_6 (XECP_SUPP_USB3_6)—Offset 803Ch	50134h
8040h	8043h	XECP_SUPP_USB3_7 (XECP_SUPP_USB3_7)—Offset 8040h	5B10125h
8044h	8047h	XECP_SUPP_USB3_8 (XECP_SUPP_USB3_8)—Offset 8044h	B630126h
8048h	804Bh	XECP_SUPP_USB3_9 (XECP_SUPP_USB3_9)—Offset 8048h	16C60127h
8094h	8097h	Host Control Scheduler (HOST_CTRL_SCH_REG)—Offset 8094h	100h
80A4h	80A7h	Power Management Control (PMCTRL_REG)—Offset 80A4h	2DFF90h
80B0h	80B3h	HOST_CTRL_MISC_REG (HOST_CTRL_MISC_REG)—Offset 80B0h	1037Fh

Table 21-2. Summary of xHCI Memory Mapped Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
80B4h	80B7h	HOST_CTRL_MISC_REG2 (HOST_CTRL_MISC_REG2)—Offset 80B4h	0h
80B8h	80BBh	SSPE_REG (SSPE_REG)—Offset 80B8h	0h
80D8h	80DBh	DEVICE MODE CONTROL REG 0 (DUAL_ROLE_CFG_REG0)—Offset 80D8h	800h
80E0h	80E3h	AUX Power Management Control (AUX_CTRL_REG1)—Offset 80E0h	808D3CA0h
80ECh	80EFh	SuperSpeed Port Link Control (HOST_CTRL_PORT_LINK_REG)—Offset 80ECh	18010000h
80F0h	80F3h	USB2 Port Link Control 1 (USB2_LINK_MGR_CTRL_REG1)—Offset 80F0h	310803A0h
80FCh	80FFh	USB2 Port Link Control 4 (USB2_LINK_MGR_CTRL_REG4)—Offset 80FCh	8003h
8140h	8143h	Power Scheduler Control-0 (PWR_SCHED_CTRL0)—Offset 8140h	A019132h
8144h	8147h	Power Scheduler Control-2 (PWR_SCHED_CTRL2)—Offset 8144h	33Fh
8154h	8157h	AUX Power Management Control (AUX_CTRL_REG2)—Offset 8154h	1390206h
8164h	8167h	USB2 PHY Power Management Control (USB2_PHY_PMC)—Offset 8164h	FCh
816Ch	816Fh	xHCI Aux Clock Control Register (XHCI_AUX_CCR)—Offset 816Ch	400h
8174h	8177h	xHC Latency Tolerance Parameters - LTV Control (XLTP_LTV1)—Offset 8174h	40047Dh
817Ch	817Fh	xHC Latency Tolerance Parameters - High Idle Time Control (XLTP_HITC)—Offset 817Ch	0h
8180h	8183h	xHC Latency Tolerance Parameters - Medium Idle Time Control (XLTP_MITC)—Offset 8180h	0h
8184h	8187h	xHC Latency Tolerance Parameters Low Idle Time Control (XLTP_LITC)—Offset 8184h	0h
8190h	8193h	Command Manager Control 2 (XECP_CMDM_CTRL_REG2)—Offset 8190h	0h
81B8h	81BBh	LFPSONCOUNT_REG (LFPSONCOUNT_REG)—Offset 81B8h	20C8h
81C4h	81C7h	USB2 PM Control (USB2PMCTRL_REG)—Offset 81C4h	0h
8420h	8423h	STRAP2_REG (STRAP2_REG)—Offset 8420h	0h
846Ch	846Fh	USB Legacy Support Capability (USBLEGSUP)—Offset 846Ch	2201h
84F4h	84F7h	Port Disable Override capability register (PDO_CAPABILITY)—Offset 84F4h	3C6h
84F8h	84FBh	USB2 Port Disable Override (USB2PDO)—Offset 84F8h	0h
84FCh	84FFh	USB3 Port Disable Override (USB3PDO)—Offset 84FCh	0h
8700h	8703h	Debug Capability ID Register (DCID)—Offset 8700h	5100Ah
8900h	8903h	SSIC Local and Remote Profile Registers Capability ID register (SSIC_PROFILE_CAPABILITY_ID_REG)—Offset 8900h	C5h
8904h	8907h	SSIC Port N Register Access Control (PORT1_REGISTER_ACCESS_CONTROL)—Offset 8904h	C00000h
8908h	890Bh	SSIC Port N Register Access Status (PORT1_REGISTER_ACCESS_STATUS)—Offset 8908h	0h
890Ch	890Fh	(PORT1_PROFILE_ATTRIBUTES_REG0)—Offset 890Ch	0h
8A14h	8A17h	SSIC Port N Register Access Control (PORT2_REGISTER_ACCESS_CONTROL)—Offset 8A14h	C00000h
8A18h	8A1Bh	SSIC Port N Register Access Status (PORT2_REGISTER_ACCESS_STATUS)—Offset 8A18h	0h
8A1Ch	8A1Fh	(PORT2_PROFILE_ATTRIBUTES_REG0)—Offset 8A1Ch	0h
8E10h	8E13h	Global Time Sync Capability (GLOBAL_TIME_SYNC_CAP_REG)—Offset 8E10h	C9h

Table 21-2. Summary of xHCI Memory Mapped Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
8E14h	8E17h	Global Time Sync Control (GLOBAL_TIME_SYNC_CTRL_REG)—Offset 8E14h	0h
8E18h	8E1Bh	Microframe Time (Local Time) (MICROFRAME_TIME_REG)—Offset 8E18h	0h
8E20h	8E23h	Always Running Time (ART) Low (ALWAYS_RUNNING_TIME_LOW)—Offset 8E20h	0h
8E24h	8E27h	Always Running Time (ART) High (ALWAYS_RUNNING_TIME_HIGH)—Offset 8E24h	0h

21.2.1 Capability Registers Length (CAPLENGTH)—Offset 0h

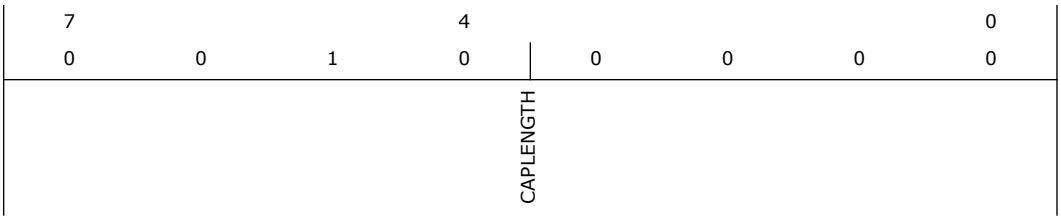
This register is modified and maintained by BIOS

Access Method

Type: MEM Register
(Size: 8 bits)

Device: 20
Function: 0

Default: 20h



Bit Range	Default & Access	Field Name (ID): Description
7:0	20h RW/L	**Capability Registers Length (CAPLENGTH):** This register is used as an offset to add to the Memory Base Register (D29:F0:10h) to find the beginning of the Operational Register Space. This field is hardwired to 20h indicating that the Operation Registers begin at offset 20h

21.2.2 Host Controller Interface Version Number (HCIVERSION)—Offset 2h

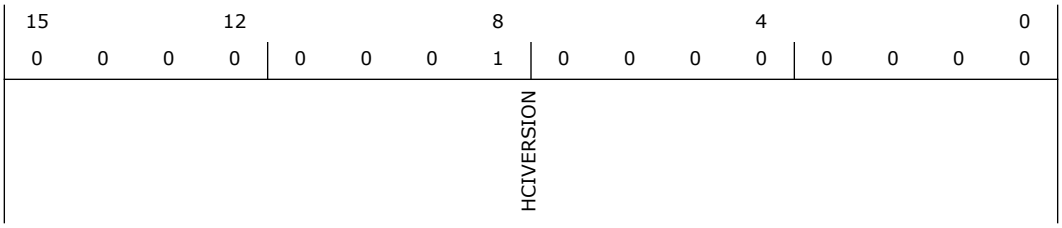
This register is modified and maintained by BIOS

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 20
Function: 0

Default: 100h



Bit Range	Default & Access	Field Name (ID): Description
15:0	100h RW/L	**Host Controller Interface Version Number (HCIVERSION):** This is a two-byte register containing a BCD encoding of the version number of interface that this host controller interface conforms.

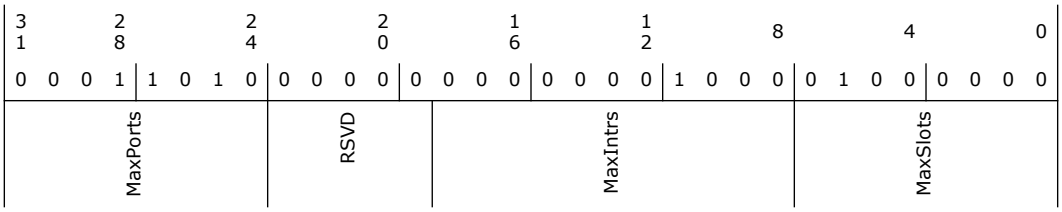
21.2.3 Structural Parameters 1 (HCSPARAMS1)—Offset 4h

This register is modified and maintained by BIOS

Access Method

Type: MEM Register (Size: 32 bits)
Device: 20
Function: 0

Default: 1A000840h



Bit Range	Default & Access	Field Name (ID): Description
31:24	1Ah RW/L	**Number of Ports (MaxPorts):** This field specifies the number of physical downstream ports implemented on this host controller. The value of this field determines how many port registers are addressable in the Operational Register Space. Default value = 0Eh
23:19	0h RO	Reserved.
18:8	8h RW/L	**Number of Interrupters (MaxIntrs):** This field specifies the number of interrupters implemented on this host controller. Each interrupter is allocated to a vector of MSI and controls its generation and moderation.
7:0	40h RW/L	**Number of Device Slots (MaxSlots):** This field specifies the number of Device Context Structures and Doorbell Array entries this host controller can support. Valid values are in the range of 1 to 255.

21.2.4 Structural Parameters 2 (HCSPARAMS2)—Offset 8h

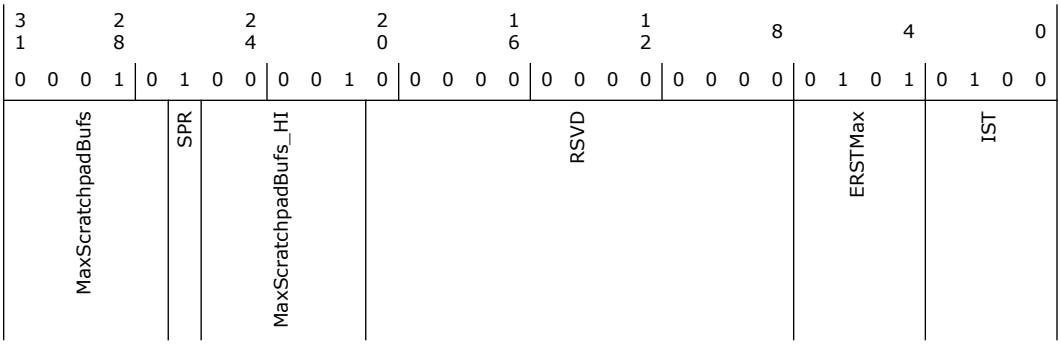
This register is modified and maintained by BIOS

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 20
Function: 0

Default: 14200054h



Bit Range	Default & Access	Field Name (ID): Description
31:27	2h RW/L	**Max Scratchpad Buffers LO (MaxScratchpadBufs):** Indicates the number of Scratchpad Buffers system software shall reserve for the xHC.
26	1h RW/L	**Scratchpad Restore (SPR):** 0 = Indicates the Scratchpad buffer space may be freed and reallocated between power events. 1 = Indicates that the xHC requires the integrity of the Scratchpad buffer space to be maintained across power events.
25:21	1h RW/L	**Max Scratchpad Buffers HI (MaxScratchpadBufs_HI)**
20:8	0h RO	Reserved.
7:4	5h RW/L	**Event Ring Segment Table Max (ERSTMax):** This field determines the maximum value supported by the Event Ring Segment Table Base Size registers.
3:0	4h RW/L	**Isochronous Scheduling Threshold (IST):** This field indicates to system software the minimum distance (in time) that it is required to stay ahead of the xHC while adding TRBs, in order to have the xHC process them at the correct time. The value is specified in the number if frames/ microframes. If bit [3] of IST is cleared to 0b, software can add a TRB no later than IST [2:0] microframes before that TRB is scheduled to be executed. If bit [3] of IST is set to 1b, software can add a TRB no later than IST[2:0] frames before that TRB is scheduled to be executed.

21.2.5 Structural Parameters 3 (HCSPARAMS3)—Offset Ch

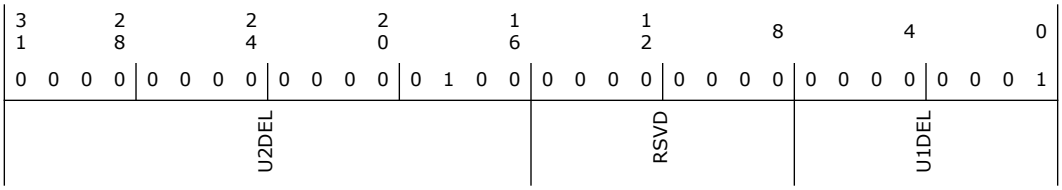
This register is modified and maintained by BIOS

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 20
Function: 0

Default: 40001h



Bit Range	Default & Access	Field Name (ID): Description
31:16	4h RW/L	**U2 Device Exit Latency (U2DEL):** Indicates the worst case latency to transition from U2 to U0. Applies to all root hub ports. The following are permissible values: Value Description 00h Zero 01h Less than 1 µs 02h Less than 2 µs ... 0Bh-FFh Reserved
15:8	0h RO	Reserved.
7:0	1h RW/L	**U1 Device Exit Latency (U1DEL):** Worst case latency to transition a root hub Port Link State (PLS) from U1 to U0. Applies to all root hub ports. The following are permissible values: Value Description 00h Zero 01h Less than 1 µs 02h Less than 2 µs ... 0800h-FFFFh Reserved

21.2.6 Capability Parameters (HCCPARAMS)—Offset 10h

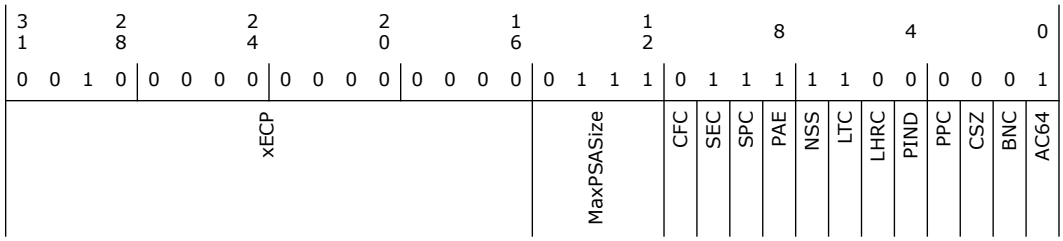
This register is modified and maintained by BIOS

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 20
Function: 0

Default: 200077C1h



Bit Range	Default & Access	Field Name (ID): Description
31:16	2000h RW/L	**xHCI Extended Capabilities Pointer (xECP):** This field indicates the existence of a capabilities list. The value of this field indicates a relative offset, in 32-bit words, from Base to the beginning of the first extended capability.
15:12	7h RW/L	**Maximum Primary Stream Array Size (MaxPSASize):** RW/L. This fields identifies the maximum size Primary Stream Array that the xHC supports. The Primary Stream Array size = 2MaxPSASize+1. Valid MaxPSASize values are 1 to 15.
11	0h RW/L	**Contiguous Frame ID Capability (CFC)**
10	1h RW/L	**Stopped EDLTA Capabilty (SEC):** This flag indicates that the host controller implementation Stream Context support a Stopped EDLTA field.
9	1h RW/L	**Stopped - Short Packet Capability (SPC):** This flag indicates that the host controller implementation is capable of generating a Stopped-Short Packet Completion Code.
8	1h RW/L	**Parst All Event Data (PAE)**
7	1h RW/L	**No Secondary SID Support (NSS):** Hardwired to '0' indicating Secondary Stream ID decoding is supported.
6	1h RW/L	**Latency Tolerance Messaging Capability (LTC):** 0 = Latency Tolerance Messaging is not supported. 1 = Latency Tolerance Messaging is supported
5	0h RW/L	**Light HC Reset Capability (LHRC):** 0 = Light Host Controller Reset is not supported. 1 = Light Host Controller Reset is supported
4	0h RW/L	**Port Indicators (PIND):** This bit indicates whether the xHC root hub ports support port indicator control. When this bit is a '1', the port status and control registers include a read/writeable field for controlling the state of the port indicator.
3	0h RW/L	**Port Power Control (PPC):** This bit indicates whether the host controller implementation includes port power control. A '1' in this bit indicates the ports have port power switches. A '0' in this bit indicates the port do not have port power switches.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/L	**Context Size (CSZ):** If this bit is set to '1', then the xHC uses 64 byte Context data structures. If this bit is cleared to '0', then the xHC uses 32 byte Context data structures.
1	0h RW/L	**BW Negotiation Capability (BNC):** 0 = Not capable of BW Negotiation. 1 = Capable of BW Negotiation.
0	1h RW/L	**64-bit Addressing Capability (AC64):** This bit documents the addressing range capability of the xHC. The value of this flag determines whether the xHC has implemented the high order 32-bits of 64-bit register and data structure pointer fields. Values for this flag have the following interpretation: 0 = Supports 32-bit address memory pointers 1 = Supports 64-bit address memory pointers If 32-bit address memory pointers are implemented, the xHC shall ignore the high order 32- bits of 64-bit data structure pointer fields, and system software shall ignore the high order 32- bits of 64- bit xHC registers.

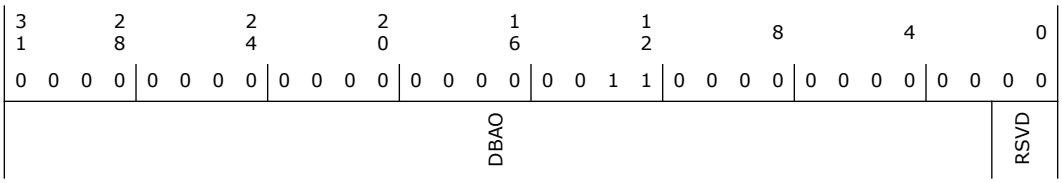
21.2.7 Doorbell Offset (DBOFF)—Offset 14h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 20
Function: 0

Default: 3000h



Bit Range	Default & Access	Field Name (ID): Description
31:2	C00h RO	**Doorbell Array Offset (DBAO):** This field defines the DWord offset of the Doorbell Array base address from the Base (for example, the base address of the xHCI Capability register address space).
1:0	0h RO	Reserved.

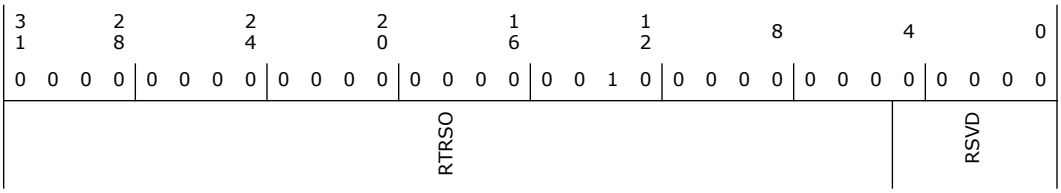
21.2.8 Runtime Register Space Offset (RTSOFF)—Offset 18h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 20
Function: 0

Default: 2000h



Bit Range	Default & Access	Field Name (ID): Description
31:5	100h RO	**Runtime Register Space Offset (RTRSO):** This field defines the 32-byte offset of the xHCI Runtime Registers from the Base. That is, Runtime Register Base Address = Base + Runtime Register Set Offset.
4:0	0h RO	Reserved.

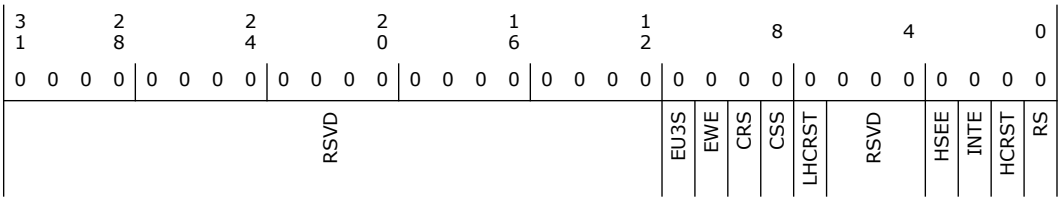
21.2.9 USB Command (USBCMD)—Offset 80h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 20
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	Reserved.
11	0h RW	**Enable U3 MFINDEX Stop (EU3S):** When set to 1b, the xHC may stop the MFINDEX counting action if all Root Hub ports are in the U3, Disconnected, Disabled, or Powered-off state. When cleared to 0b, the xHC may stop the MFINDEX counting action if all Root Hub ports are in the Disconnected, Disabled, or Powered-off state.
10	0h RW	**Enable Wrap Event (EWE):** When set to 1b, the xHC shall generate a MFINDEX Wrap Event every time the MFINDEX register transitions from 03FFFh to 0. When cleared to 0b, no MFINDEX Wrap Events are generated.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Controller Restore State (CRS):** When set to 1b, MEM_BASE+80h:bit 0= 0b, and MEM_BASE+80h:bit 8 = 1b, the xHC shall perform a Restore State operation and restore its internal state. When set to 1b and MEM_BASE+80h:bit 0= 1b or MEM_BASE+80h:bit 8 = 0b, or when cleared to '0', no Restore State operation shall be performed.
8	0h RW	**Controller Save State (CSS):** When written by software with 1b and MEM_BASE+80h:bit 0=0b, the xHC shall save any internal state that will be restored by a subsequent Restore State operation. When written by software with 1b and MEM_BASE+80h:bit 0= 1b, or written with '0', no Save State operation shall be performed.
7	0h RW	**Light Host Controller Reset (LHCRST):** If the Light HC Reset Capability (LHRC) bit (MEM_BASE=10h:bit 5) is 1b, then setting this bit to 1b allows the driver to reset the xHC without affecting the state of the ports. A system software read of this bit as 0b indicates the Light Host Controller Reset has completed and it is safe for software to re-initialize the xHC. A software read of this bit as a 1b indicates the Light Host Controller Reset has not yet completed.
6:4	0h RO	Reserved.
3	0h RW	**Host System Error Enable (HSEE):** When this bit is set to 1b, and the HSE bit (MEM_BASE+84h:bit 2) is set to 1b, the xHC shall assert out-of-band error signaling to the host. The signaling is acknowledged by software clearing the HSE bit.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Interrupter Enable (INTE):** This control bit is used by software to reset the host controller. When software sets this bit to 1b, the Host Controller resets its internal pipelines, timers, counters, state machines, and so forth, to their initial value. Any transaction currently in progress on USB is immediately terminated. A USB reset is not driven on downstream ports. PCI Configuration registers are not affected by this reset. All operational registers, including port registers and port state machines are set to their initial values.
1	0h RW	**Host Controller Reset (HCRST):** This control bit is used by software to reset the host controller. When software sets this bit to 1b, the Host Controller resets its internal pipelines, timers, counters, state machines, and so forth, to their initial value. Any transaction currently in progress on USB is immediately terminated. A USB reset is not driven on downstream ports. PCI Configuration registers are not affected by this reset. All operational registers, including port registers and port state machines are set to their initial values.
0	0h RW	**Run/Stop (RS):** When set to 1b, the xHC proceeds with execution of the schedule. The xHC continues execution as long as this bit is set to 1b. When this bit is cleared to 0b, the xHC completes the current and any actively pipelined transactions on the USB and then halts. The xHC shall halt within 16 microframes after software clears the Run/ Stop bit. The HCHalted (HCH) bit (MEM_BASE+84h:bit 0) indicates when the xHC has finished its pending pipelined transactions and has entered the stopped state. Software shall not write a '1' to this flag unless the xHC is in the Halted state (that is, HCH in the USBSTS register is '1'); doing so will yield undefined results.

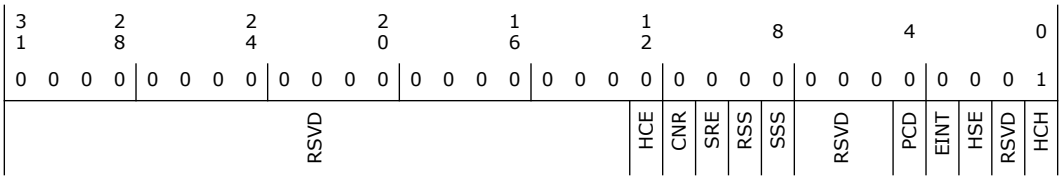
21.2.10 USB Status (USBSTS)—Offset 84h

This register indicates pending interrupts and various states of the Host controller. The status resulting from a transaction on the serial bus is not indicated in this register. See the Interrupts description in section 4 of the xHCI specification for additional information concerning interrupt conditions.
Note: For the writable bits, software must write a 1 to clear bits that are set. Writing a 0 has no effect.

Access Method

Type: MEM Register (Size: 32 bits)
Device: 20
Function: 0

Default: 1h



Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	Reserved.
12	0h RO	**Host Controller Error (HCE):** This flag shall be set to indicate that an internal error condition has been detected which requires software to reset and re-initialize the xHC. 0 = No internal xHC error conditions exist. 1 = Internal xHC error condition exists.
11	0h RO	**Controller Not Ready (CNR):** 0 = Ready 1 = Not Ready Software shall not write any Doorbell or Operational register of the xHC, other than the USBSTS register, until CNR = 0b. This flag is set by the xHC after a Hardware Reset and cleared when the xHC is ready to begin accepting register writes. This flag shall remain cleared (0b) until the next Chip Hardware Reset.
10	0h RW/C	**Save/Restore Error (SRE):** If an error occurs during a Save or Restore operation this bit shall be set to 1b. This bit shall be cleared to 0b when a Save or Restore operation is initiated or when written with 1b.
9	0h RO	**Restore State Status (RSS):** When the Controller Restore State (CRS) flag in the USB_CMDregister is written with 1b this bit shall be set to 1b and remain set while the xHC restores its internalstate. Note: When the Restore State operation is complete, this bit shall be cleared to 0b.
8	0h RO	**Save State Status (SSS):** When the Controller Save State (CSS) flag in the USB_CMD register is written with 1b this bit shall be set to 1b and remain set while the xHC saves its internal state. Note: When the Save State operation is complete, this bit shall be cleared to 0b.
7:5	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW/C	**Port Change Detect (PCD):** This bit is allowed to be maintained in the Auxiliary power well. Alternatively, it is also acceptable that on a D3 to D0 transition of the xHC, this bit is loaded with the OR of all of the PORTSC change bits (including: Force port resume, overcurrent change, enable/ disable change and connect status change). Regardless of the implementation, when this bit is readable (that is, in the D0 state), it must provide a valid view of the Port Status registers. 0 = No change bit transition from a 0 to 1 or No Force Port Resume bit transition from 0 to 1 as a result of a J-K transition detected on a suspended port. 1 = The Host controller sets this bit to 1 when any port for which the Port Owner bit is set to 0 has a change bit transition from a 0 to 1 or a Force Port Resume bit transition from 0 to 1 as a result of a J-K transition detected on a suspended port.
3	0h RW/C	**Event Interrupt (EINT):** The xHC sets this bit to 1b when the Interrupt Pending (IP) bit of any Interrupter is transitions from 0b to 1b. Software that uses EINT shall clear it prior to clearing any IP flags. A race condition will occur if software clears the IP flags then clears the EINT flag, and between the operations another IP '0' to '1' transition occurs. In this case the new IP transition will be lost.
2	0h RW/C	**Host System Error (HSE):** The xHC sets this bit to 1b when a serious error is detected, either internal to the xHC or during a host system access involving the xHC module. Conditions that set this bit to '1' include PCI Parity error, PCI Master Abort, and PCI Target Abort. When this error occurs, the xHC clears the Run/Stop (R/S) bit in the USB_CMD register to prevent further execution of the scheduled TDs. If the HSEE bit in the USB_CMD register is 1b, the xHC shall also assert out-ofband error signaling to the host.
1	0h RO	Reserved.
0	1h RO	**HCHalted (HCH):** This bit is a '0' whenever the Run/Stop (R/S) bit is set to 1b. The xHC sets this bit to 1b after it has stopped executing as a result of the Run/Stop (R/S) bit being cleared to 0b, either by software or by the xHC hardware (for example, internal error). If this bit is set to1b, then SOFs, microSOFs, or Isochronous Timestamp Packets (ITP) shall not be generated by the xHC.

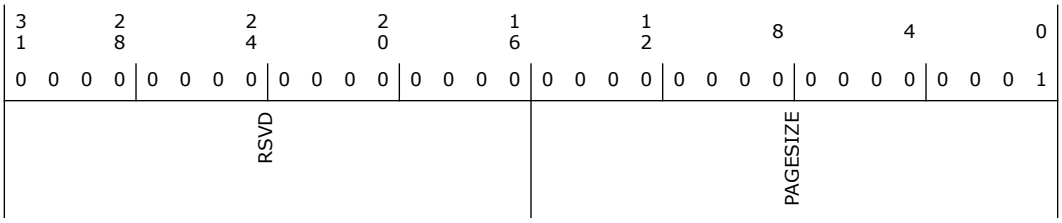
21.2.11 Page Size (PAGESIZE)—Offset 88h

Offset: MEM_BASE + 88h–8Bh Attribute: RO
Default Value: 00000001h Size: 32 bits

Access Method

Type: MEM Register (Size: 32 bits)
Device: 20
Function: 0

Default: 1h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	1h RO	**Page Size (PAGESIZE):** Hardwired to 1h to indicate support for 4 Kbyte page sizes.

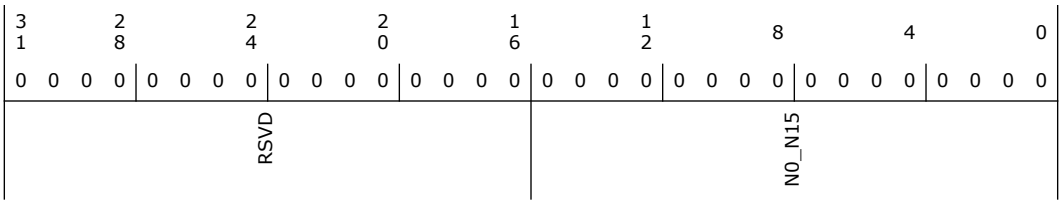
21.2.12 Device Notification Control (DNCTRL)—Offset 94h

Offset: MEM_BASE + 94h–97h Attribute: R/W
Default Value: 00000000h Size: 32 bits

Access Method

Type: MEM Register (Size: 32 bits)
Device: 20
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	0h RW	**Notification Enable (N0_N15):** When a Notification Enable bit is set, a Device Notification Event will be generated when a Device Notification Transaction Packet is received with the matching value in the Notification Type field. For example, setting N1 to '1' enables Device Notification Event generation if a Device Notification TP is received with its Notification Type field set to '1' (FUNCTION_WAKE), and so on

21.2.13 Command Ring Low (CRCR_LO)—Offset 98h

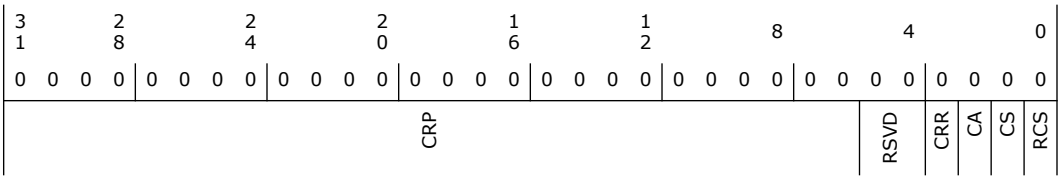
Offset: MEM_BASE + 98h–9Bh Attribute: R/W, RO
Default Value: 00000000h Size: 32 bits

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 20
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RW	**Command Ring Pointer (CRP):** This field defines low order bits of the initial value of the 64-bit Command Ring Dequeue Pointer. Notes: 1. Writes to this field are ignored when Command Ring Running bit (CRR) = 1b. 2. If the CRCR register is written while the Command Ring is stopped (CRR = 0b), the value of this field shall be used to fetch the first Command TRB the next time the Host Controller Doorbell register is written with the DB Reason field set to Host Controller Command. 3. If the CRCR register is not written while the Command Ring is stopped (CRR = 0b), then the Command Ring shall begin fetching Command TRBs at the current value of the internal xHC Command Ring Dequeue Pointer. 4. Reading this field always returns 0b.
5:4	0h RO	Reserved.
3	0h RO	**Command Ring Running (CRR):** This bit is set to 1b if the Run/Stop (R/S) bit is 1b and the Host Controller Doorbell register is written with the DB Reason field set to Host Controller Command. It is cleared to 0b when the Command Ring is stopped after writing a 1b to the Command Stop (CS) or Command Abort (CA) bits, or if the R/S bit is cleared to 0b.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1S	**Command Abort (CA):** Writing a 1b to this bit shall immediately terminate the currently executing command, stop the Command Ring, and generate a Command Completion Event with the Completion Code set to Command Ring Stopped. The next write to the Host Controller Doorbell with DB Reason field set to Host Controller Command shall restart the Command Ring operation. Notes: 1. Writes to this flag are ignored by the xHC if Command Ring Running (CRR) = 0b. 2. Reading this bit always returns 0b.
1	0h RW/1S	**Command Stop (CS):** Writing a 1b to this bit shall stop the operation of the Command Ring after the completion of the currently executing command, and generate a Command Completion Event with the Completion Code set to Command Ring Stopped and the Command TRB Pointer set to the current value of the Command Ring Dequeue Pointer. The next write to the Host Controller Doorbell with DB Reason field set to Host Controller Command shall restart the Command Ring operation. Notes: 1. Writes to this flag are ignored by the xHC if Command Ring Running (CRR) bit = 0b. 2. Reading this bit always returns 0b.
0	0h RW	**Ring Cycle State (RCS):** This bit identifies the value of the xHC Consumer Cycle State (CCS) flag for the TRB referenced by the Command Ring Pointer. Notes: 1. Writes to this bit are ignored when the Command Ring Running (CRR) bit = 1b. 2. If the CRCR register is written while the Command Ring is stopped (CCR = 0b), then the value of this flag shall be used to fetch the first Command TRB the next time the Host Controller Doorbell register is written with the DB Reason field set to Host Controller Command. 3. If the CRCR register is not written while the Command Ring is stopped (CCR = 0b), then the Command Ring will begin fetching Command TRBs using the current value of the internal Command Ring CCS flag. 4. Reading this flag always returns 0b.

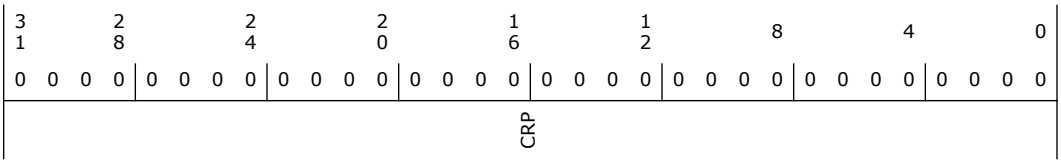
21.2.14 Command Ring High (CRCR_HI)—Offset 9Ch

Access Method

Type: MEM Register (Size: 32 bits)

Device: 20
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Command Ring Pointer (CRP):** Command Ring Pointer—R/W. This field defines high order bits of the initial value of the 64-bit Command Ring Dequeue Pointer. Notes: 1. Writes to this field are ignored when Command Ring Running bit (CRR) = 1b. 2. If the CRCR register is written while the Command Ring is stopped (CRR = 0b), the value of this field shall be used to fetch the first Command TRB the next time the Host Controller Doorbell register is written with the DB Reason field set to Host Controller Command. 3. If the CRCR register is not written while the Command Ring is stopped (CRR = 0b), then the Command Ring shall begin fetching Command TRBs at the current value of the internal xHC Command Ring Dequeue Pointer. 4. Reading this field always returns 0b.

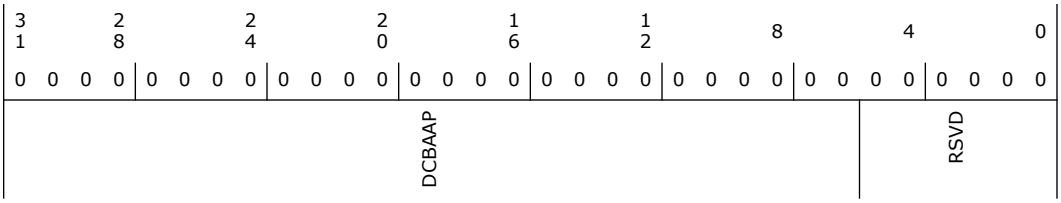
21.2.15 Device Context Base Address Array Pointer Low (DCBAAP_LO)—Offset B0h

Access Method

Type: MEM Register (Size: 32 bits)

Device: 20
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RW	**Device Context Base Address Array Pointer (DCBAAP):** This field defines low order bits of the 64-bit base address of the Device Context Pointer Array table (a table of address pointers that reference Device Context structures for the devices attached to the host.
5:0	0h RO	Reserved.

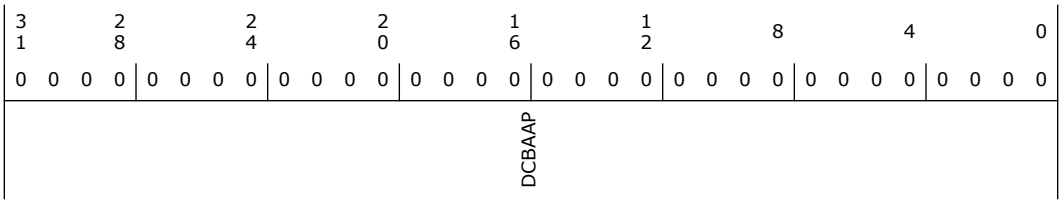
21.2.16 Device Context Base Address Array Pointer High (DCBAAP_HI)—Offset B4h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 20
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Device Context Base Address Array Pointer (DCBAAP):** This field defines high order bits of the 64-bit base address of the Device Context Pointer Array table (a table of address pointers that reference Device Context structures for the devices attached to the host.)

21.2.17 Port N Status and Control USB2 (PORTSCN)—Offset 480h

Note that this USB2 Port Status and Control register is available at the following offsets for all applicable USB2 ports:

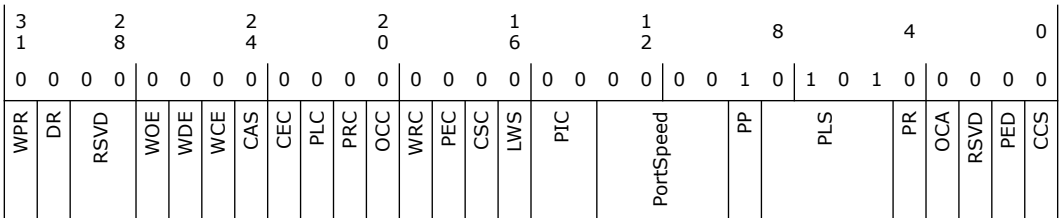
USB2 Port 1: 480h
USB2 Port 2: 490h
USB2 Port 3: 4A0h
.....
USB2 Port 9: 500h
USB2 Port 10: 510h

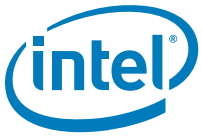
Access Method

Type: MEM Register
(Size: 32 bits)

Device: 20
Function: 0

Default: 2A0h





Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S	**Warm Port Reset (WPR):** When software sets this bit to 1b, the Warm Reset sequence is
30	0h RW/L	**Device Removable (DR):** This bit indicates if this port has a removable device. 0 = Device is removable. 1 = Device is non-removable.
29:28	0h RO	Reserved.
27	0h RW	**Wake on Over-current Enable (WOE):** 0 = Disable. (Default) 1 = Enable. Writing this bit to a 1b enables the port to be sensitive to overcurrent conditions as system wake-up events.
26	0h RW	**Wake on Disconnect Enable (WDE):** 0 = Disable. (Default) 1 = Enable. Writing this bit to a 1b enables the port to be sensitive to device disconnects as system wake-up events.
25	0h RW	**Wake on Connect Enable (WCE):** 0 = Disable. (Default) 1 = Enable. Writing this bit to a 1b enables the port to be sensitive to device connects as system wake-up events.
24	0h RO	**Cold Attach Status (CAS):** This bit indicates that far-end terminations were detected in the Disconnected state and the Root Hub Port State Machine was unable to advance to the Enabled state. Software shall clear this bit by writing a 1b to the WPR bit or the xHC shall clear this bit if the CSS bit transitions to 1.
23	0h RW/C	**Port Config Error Change (CEC):** This flag indicates that the port failed to configure its link partner.Software shall clear this bit by writing a 1 to it.
22	0h RW/C	**Port Link State Change (PLC):** 0 = No change 1 = Link Status Change This flag is set to ‘1’ due to the following Port Link State (PLS) transitions:
21	0h RW/C	**Port Reset Change (PRC):** This flag is set to ‘1’ due a '1' to '0' transition of Port Reset (PR), for example, when any reset processing on this port is complete. 0 = No change 1 = Reset Complete
20	0h RW/C	**Over-current Change (OCC):** The functionality of this bit is not dependent upon the port owner. Software clears this bit by writing a 1 to it. 0 = No change. (Default) 1 = There is a change to Overcurrent Active.

Bit Range	Default & Access	Field Name (ID): Description
19	0h RW/C	**Warm Port Reset Change (WRC):** This bit is set when Warm Reset processing on this port completes. 0 = No change. (Default) 1 = Warm reset complete
18	0h RW/C	**Port Enabled Disabled Change (PEC):** 0 = No change. (Default) 1 = There is a change to PED bit.
17	0h RW/C	**Connect Status Change (CSC):** R/WC. This flag indicates a change has occurred in the port's Current Connect Status (CCS) or Cold Attach Status (CAS) bits. 0 = No change. (Default) 1 = There is a change to the CCS or CAS bit. The xHC sets this bit to 1b for all changes to the port device connect status, even if system software has not cleared an existing Connect Status Change. For example, the insertion status changes twice before system software has cleared the changed condition, root hub hardware will be "setting" an already-set bit (that is, the bit will remain 1b).
16	0h RW	**Port Link State Write Strobe (LWS):** 0 = When 0b, write data in PLS field is ignored. (Default) 1 = When this bit is set to 1b on a write reference to this register, this flag enables writes to the PLS field. Reads to this bit return '0'.
15:14	0h RW	**Port Indicator Control (PIC)**
13:10	0h RW	**Port Speed (PortSpeed):** A device attached to this port operates at a speed defined by the following codes: Value Speed 0001b Full-speed 0010b Low speed 0011b Highspeed All other values reserved. Refer to the eXtensible Host Controller Interface for Universal Serial Bus Specification for additional details.
9	1h RW	**Port Power (PP):** Read-only with a value of 1. This indicates that the port does have power.

Bit Range	Default & Access	Field Name (ID): Description
8:5	5h RW	**Port Link State (PLS):** This field is used to power manage the port and reflects its currentlink state.When the port is in the Enabled state, system software may set the link U-state by writing this field. System software may also write this field to force a Disabled to Disconnected state transition of the port. Write Value and Description 0: The link shall transition to a U0 state from any of the U-states. 2: USB 2.0 ports only. The link should transition to the U2 State. 3: The link shall transition to a U3 state from any of the U-states. This action selectively suspends the device connected to this port. While the Port LinkState = U3, the hub does not propagate downstream-directed traffic to this port, but the hub will respond to resume signaling from the port. 5: USB 3.0 ports only. If the port is in the Disabled state (PLS = Disabled, PP= 1), then the link shall transition to a RxDetect state and the port shall transition to the Disconnected state, else ignored. 15: USB 2.0 ports only. If the port is in the U3 state (PLS = U3), then the link shall remain in the U3 state and the port shall transition to the U3Exit substate, else ignored. All other values are ignored Read Value and Definition 0: Link is in the U0 State 1: Link is in the U1 State 2: Link is in the U2 State 3: Link is in the U3 State (Device Suspended) 4: Link is in the Disabled State 5:Link is in the RxDetect State 6:Link is in the Inactive State 7: Link is in the Polling State 8:Link is in the Recovery State 9: Link is in the Hot Reset State 10: Link is in the Compliance Mode State 11: Link is in the Test Mode State 12–14: Reserved 15: Link is in the Resume State
4	0h RW/1S	**Port Reset (PR):** When software writes a 1 to this bit (from a 0), the bus reset sequence as 1=port in reset 0=port not in reset
3	0h RO	**Over-current Active (OCA):** 0 = This port does not have an overcurrent condition. (Default) 1 = This port currently has an overcurrent condition. This bit will automatically transition from 1 to 0 when the overcurrent condition is removed. The PCH automatically disables the port when the overcurrent active bit is 1.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	Reserved.
1	0h RW/C	**Port Enabled Disabled (PED):** Ports can only be enabled by the host controller as a part of the reset and enable. Software cannot enable a port by writing a 1 to this bit. Ports can be disabled by either a fault condition (disconnect event or other fault condition) or by host software. The bit status does not change until the port state actually changes. There may be a delay in disabling or enabling a port due to other host controller and bus events. 0=disable 1=enable(default)
0	0h RW	**Current Connect Status (CCS):** This value reflects the current state of the port, and may not correspond directly to the event that caused the Connect Status Change bit (Bit 1) to be set. 0=no device is present 1=device is present on port.

21.2.18 Port Power Management Status and Control USB2 (PORTPMSCN)—Offset 484h

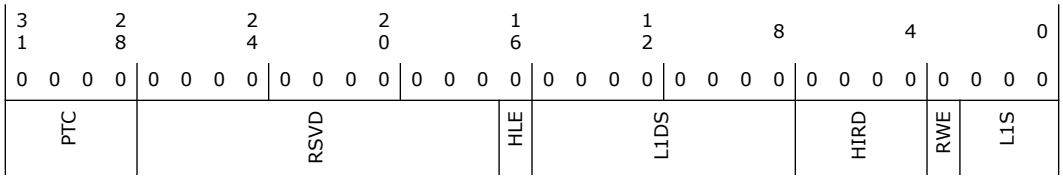
Note that this USB2 Port Power Management Status and Control register is available at the following offsets for all applicable USB2 ports:

USB2 Port 1: 484h
USB2 Port 2: 494h
USB2 Port 3: 4A4h
..... USB2 Port 9: 504h
USB2 Port 10: 514h

Access Method

Type: MEM Register (Size: 32 bits)
Device: 20
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RW	**Port Test Control (PTC):** When this field is '0', the port is not operating in a test mode. (Default) A non-zero value indicates that the port is operating in test mode and the specific test mode is indicated by the specific value. A non-zero Port Test Control value is only valid to a port that is in the Disabled state. If the port is not in this state, the xHC shall respond with the Port Test Control field set to Port Test Control Error. The encoding of the Test Mode bits for a USB 2.0 port are: Value Test Mode 0h Test mode not enabled 1h Test J_STATE 2h Test K_STATE 3h Test SE0_NAK 4h Test Packet 5h Test FORCE_ENABLE 6h–14h Reserved. 15 Port Test Control Error
27:17	0h RO	Reserved.
16	0h RW	**Hardware LPM Enable (HLE):** 0=disable 1=Enable. When this bit is a 1, hardware controlled LPM shall be enabled for this port. Refer to section 4 of the USB 2.0 LPM Specification for more information.
15:8	0h RW	**L1 Device Slot (L1DS):** System software sets this field to indicate the ID of the Device Slot associated with the device directly attached to the Root Hub port. A value of 0 indicates there is no device present.
7:4	0h RW	**Host Initiated Resume Duration (HIRD):** System software sets this field to indicate to the recipient device how long the xHC will drive resume if it (the xHC) initiates an exit from L1. The HIRD value is encoded as follows: The value of 0000b is interpreted as 50 µs. Each incrementing value up adds 75 µs to the previous value. For example, 0001b is 125 µs, 0010b is 200µs and so on. Based on this rule, the maximum value resume drive time is at encoding value 1111b which represents 1.2ms. Refer to section 4 of the USB 2.0 LPM Specification for more information.
3	0h RW	**Remote Wake Enable (RWE):** The host system sets this flag to enable or disable the device for remote wake from L1. 0=disable 1=enable The value of this flag will temporarily (while in L1) override the current setting of the Remote Wake feature set by the standard Set/ClearFeature() commands defined in Universal Serial Bus Specification, revision 2.0, Chapter 9.
2:0	0h RW	**L1 Status (L1S)**

21.2.19 Port N Hardware LPM Control Register (PORTHLPMCN)—Offset 48Ch

Note that this Port Hardware Control register is available at the following offsets for all applicable USB ports:

USB2 Port 1: 48Ch
USB2 Port 2: 49Ch
USB2 Port 3: 4ACh
..... USB2 Port 9: 50Ch
USB2 Port 10: 51Ch

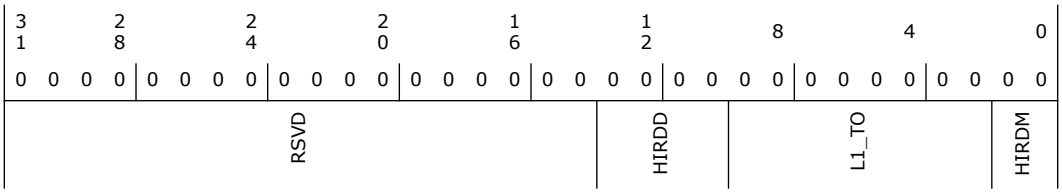
This register is reset only by platform hardware during cold reset or in response to a Host Controller Reset (HCRST).The definition for the fields depend on the protocol supported.
For USB3 this register is reserved and shall be treated by software as RsvdP.
For USB2 the definition is given below. Fields contain parameters neccessary for xHC to automatically generate an LPM Token to the downstream device.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 20
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**Host Initiated Resume Duration-Deep (HIRDD):** System software sets this field to indicate to the recipient device how long the xHC will drive resume if an exit from L1. The HIRDD value is is encoded as follows: 0h: 50 us (default) 1h: 125 us 2h: 200 us...Fh: 1.175ms The value of 0h is interpreted as 50 us. Each incrementing value adds 75 us to the previous value.
9:2	0h RW	**L1 Timeout (L1_TO):** Timeout value for L1 inactivity timer. This field shall be set to 00h by assertion of PR to '1'. Following are permissible values: 00h: 128 us (default) 01h: 256 us....FFh: 65,280us
1:0	0h RW	**Host Initiated Resume Duration Mode (HIRDM):** Indicates which HIRD value should be used. Following are permissible values: 0: Initiate L1 using HIRD only time out (default) 1: Initiate HIRDDon timeout. If rejected by device, initiate L1 using HIRD 2,3: Reserved Note: This register is sticky.

21.2.20 Port Status and Control USB3 (PORTSCXUSB3)—Offset 540h

The USB3 Port Status and Control registers are available at the following offsets for applicable USB3 ports:

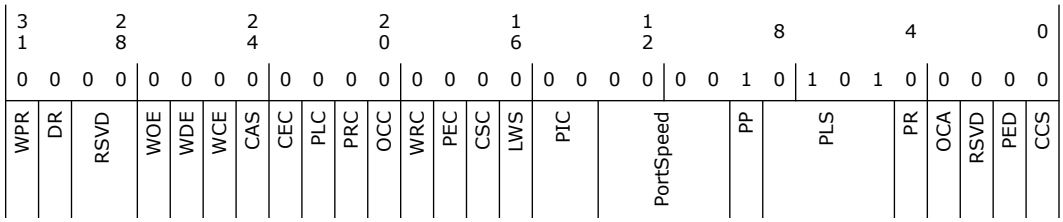
USB3 Port 1: 540h
USB3 port 2: 550h
USB3 port 3: 560h
USB3 port 4: 570h
USB3 port 5: 580h
USB3 port 6: 590h

Access Method

Type: MEM Register (Size: 32 bits)

Device: 20
Function: 0

Default: 2A0h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S	**Warm Port Reset (WPR)**
30	0h RW/L	**Device Removable (DR)**
29:28	0h RO	Reserved.
27	0h RW	**Wake on Over-current Enable (WOE):** Note: This register is sticky.
26	0h RW	**Wake on Disconnect Enable (WDE):** Note: This register is sticky.
25	0h RW	**Wake on Connect Enable (WCE):** Note: This register is sticky.
24	0h RO	**Cold Attach Status (CAS)**
23	0h RW/C	**Port Config Error Change (CEC):** Note: This register is sticky.
22	0h RW/C	**Port Link State Change (PLC):** Note: This register is sticky.
21	0h RW/C	**Port Reset Change (PRC):** Note: This register is sticky.
20	0h RW/C	**Over-current Change (OCC):** Note: This register is sticky.
19	0h RW/C	**Warm Port Reset Change (WRC):** Note: This register is sticky.
18	0h RW/C	**Port Enabled Disabled Change (PEC):** Note: This register is sticky.
17	0h RW/C	**Connect Status Change (CSC):** Note: This register is sticky.
16	0h RW	**Port Link State Write Strobe (LWS)**
15:14	0h RW	**Port Indicator Control (PIC):** Note: This register is sticky.
13:10	0h RO	**Port Speed (PortSpeed):** A device attached to this port operates at a speed defined by the following codes:{br] 0100b: SuperSpeed (5Gb/s)
9	1h RO	**Port Power (PP):** Read-only with a value of 1. This indicates that the port does have power.

Bit Range	Default & Access	Field Name (ID): Description
8:5	5h RW	**Port Link State (PLS):** This field is used to power manage the port and reflects its current link state. When the port is in the Enabled state, system software may set the link U-state by writing this field. System software may also write this field to force a Disabled to Disconnected state transition of the port. Write Value and Description: 0: The link shall transition to a U0 state from any of the U-states. 2: USB 2.0 ports only. The link should transition to the U2 State. 3: The link shall transition to a U3 state from any of the U-states. This action selectively suspends the device connected to this port. While the Port Link State = U3, the hub does not propagate downstream-directed traffic to this port, but the hub will respond to resume signaling from the port. 5: USB 3.0 ports only. If the port is in the Disabled state (PLS = Disabled, PP = 1), then the link shall transition to a RxDetect state and the port shall transition to the Disconnected state, else ignored. 15: USB 2.0 ports only. If the port is in the U3 state (PLS = U3), then the link shall remain in the U3 state and the port shall transition to the U3Exit substate, else ignored. All other values Ignored Note: The Port Link State Write Strobe (LWS) shall be set to 1b to write this field. Read Value and Definition: 0: Link is in the U0 State 1: Link is in the U1 State 2: Link is in the U2 State 3: Link is in the U3 State (Device Suspended) 4: Link is in the Disabled State 5: Link is in the RxDetect State 6: Link is in the Inactive State 7: Link is in the Polling State 8: Link is in the Recovery State 9: Link is in the Hot Reset State 10: Link is in the Compliance Mode State 11: Link is in the Test Mode State 12–14: Reserved 15: Link is in the Resume State

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW/1S	**Port Reset (PR):** Port Reset (PR)—R/W. When software writes a 1 to this bit (from a 0), the bus reset sequence as defined in the USB Specification, Revision 2.0 is started. Software writes a 0 to this bit to terminate the bus reset sequence. Software must keep this bit at a 1 long enough to ensure the reset sequence completes as specified in the USB Specification, Revision 2.0. USB 3.0 ports shall execute the Hot Reset sequence as defined in the USB 3.0 Specification. PR remains set until reset signaling is completed by the root hub. 1 = Port is in Reset. 0 = Port is not in Reset.
3	0h RO	**Over-current Active (OCA):** 0 = This port does not have an overcurrent condition. (Default) 1 = This port currently has an overcurrent condition. This bit will automatically transition from 1 to 0 when the overcurrent condition is removed. The PCH automatically disables the port when the overcurrent active bit is 1.
2	0h RO	Reserved.
1	0h RW/C	**Port Enabled Disabled (PED):** Ports can only be enabled by the host controller as a part of thereset and enable. Software cannot enable a port by writing a 1 to this bit. Ports can be disabled by either a fault condition (disconnect event or other fault condition) or by host software. The bit status does not change until the port state actually changes. There may be a delay in disabling or enabling a port due to other host controller and bus events. 0 = Disable. 1 = Enable. (Default)
0	0h RO	**Current Connect Status (CCS):** This value reflects the current state of the port, and may not correspond directly to the event that caused the Connect Status Change bit (Bit 1) to be set. 0 = No device is present. (Default) 1 = Device is present on port.

21.2.21 Port Power Management Status and Control USB3 (PORTPMSCX)—Offset 544h

The USB3 Port Status and Control registers are available at the following offsets for applicable USB3 ports:

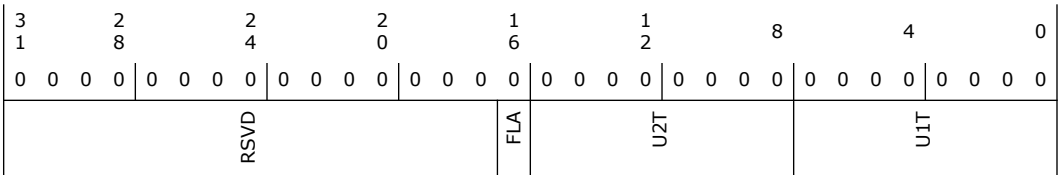
USB3 Port 1: 544h
USB3 port 2: 554h
USB3 port 3: 564h
USB3 port 4: 574h
USB3 port 5: 584h
USB3 port 6: 594h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 20
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	Reserved.
16	0h RW	**Force Link PM Accept (FLA)**
15:8	0h RW/S	**U2 Timeout (U2T)**
7:0	0h RW/S	**U1 Timeout (U1T)**

21.2.22 USB3 Port X Link Info (PORTLIX)—Offset 548h

Note that this USB3 Port Link Info register is available at the following offsets for all applicable USB3 ports:

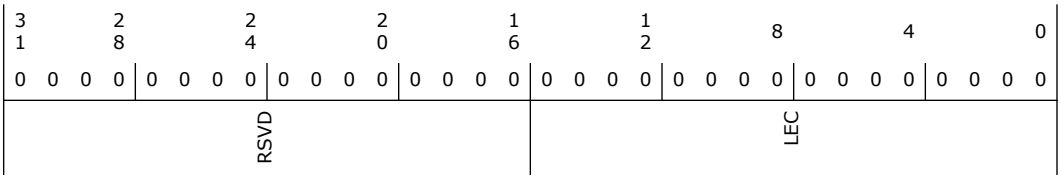
USB3 Port 1: 548h
USB3 port 2: 558h
USB3 port 3: 568h
USB3 port 4: 578h
USB3 port 5: 588h
USB3 port 6: 598h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 20
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	0h RO	**Link Error Count (LEC):** Displays the Link Error Count for the USB 3 port.

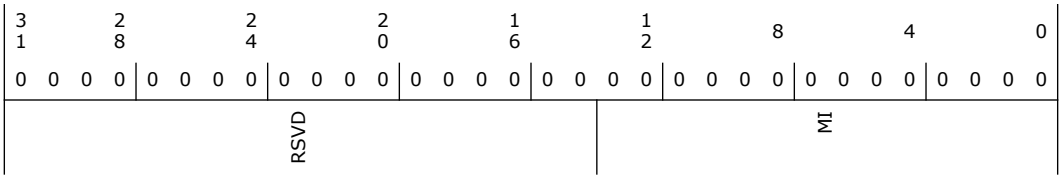
21.2.23 Microframe Index (MFINDEX)—Offset 2000h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 20
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:0	0h RO	**Microframe Index (MI):** The value in this register increments at the end of each microframe (for example, 125 µs.). Bits [13:3] may be used to determine the current 1ms. Frame Index.

21.2.24 Interrupter x Management (IMANx)—Offset 2020h

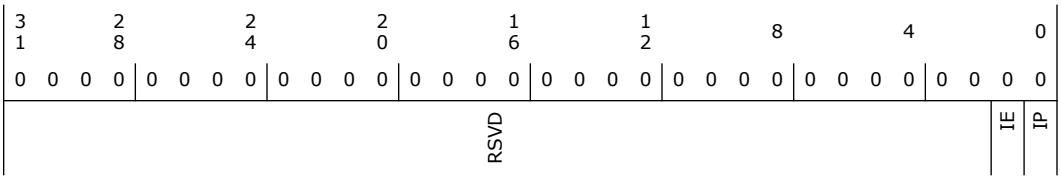
Note that there are a total of 8 IMAN registers at the following offsets:
IMAN0: at offset 2020h
IMAN1: at offset 2040h
IMAN2: at offset 2060h
.....
IMAN6: at offset 20E0h
IMAN7; at offset 2100h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 20
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1	0h RW	**Interrupt Enable (IE):** This flag specifies whether the Interrupter is capable of generating an interrupt. 0 = The Interrupter is prohibited from generating interrupts. 1 = When this bit and the IP bit are set (1b), the Interrupter shall generate an interrupt when the Interrupter Moderation Counter reaches '0'.
0	0h RW/C	**Interrupt Pending (IP):** 0 = No interrupt is pending for the Interrupter. 1 = An interrupt is pending for this Interrupter. This bit is set to 1b when IE = 1, the IMODI Interrupt Moderation Counter field = 0b, the Event Ring associated with the Interrupter is not empty (or for the Primary Interrupter when the HCE flag is set to 1b), and EHB = 0. If MSI interrupts are enabled, this flag shall be cleared automatically when the PCI DWord write generated by the Interrupt assertion is complete. If PCI Pin Interrupts are enabled, this flag shall be cleared by software.

21.2.25 Interrupter x Moderation (IMODx)—Offset 2024h

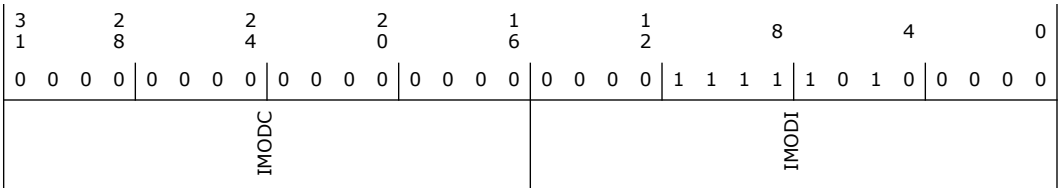
Note that there are a total of 8 IMOD registers at the following offsets:
IMOD0 : at offset 2024h
IMOD1: at offset 2044h
IMOD2: at offset 2064h
.....
IMOD6: at offset 20E4h
IMOD7; at offset 2104h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 20
Function: 0

Default: FA0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Interrupt Moderation Counter (IMODC):** Down counter. Loaded with Interval Moderation value—value of bits 15:0, whenever the IP bit is cleared to 0b, counts down to '0', and stops. The associated interrupt shall be signaled whenever this counter is '0', the Event Ring is not empty, the IE and IP bits = 1, and EHB = 0. This counter may be directly written by software at any time to alter the interrupt rate
15:0	FA0h RW	**Interrupt Moderation Interval (IMODI):** Minimum inter-interrupt interval. The interval isspecified in 250 ns increments. A value of '0' disables interrupt throttling logic and interrupts shall be generated immediately if IP = 0, EHB = 0, and the Event Ring is not empty.

21.2.26 Event Ring Segment Table Size x (ERSTSZx)—Offset 2028h

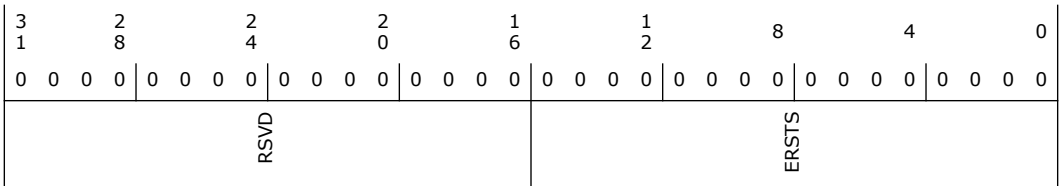
There are 8 ERSTSZ registers available at the following address offsets:
ERSTSZ0: at offset 2028h
ERSTSZ1: at offset 2048h
ERSTSZ2: at offset 2068h
ERSTSZ3: at offset 2088h
ERSTSZ4: at offset 20A8h
ERSTSZ5: at offset 20C8h
ERSTSZ6: at offset 20E8h
ERSTSZ7: at offset 2108h
Address Offset: 2028-202Bh, 2048-204Bh, ..., 2028+(MaxInts-1)*20h-202B+(MaxInts-1)*20h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 20
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	0h RW	**Event Ring Segment Table Size (ERSTS):** This field identifies the number of valid Event Ring Segment Table entries in the Event Ring Segment Table pointed to by the Event Ring Segment Table Base Address register.

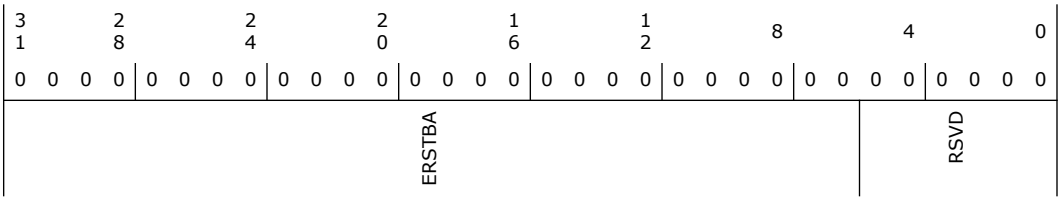
21.2.27 Event Ring Segment Table Base Address Low x (ERSTBA_LOx)—Offset 2030h

There are 8 ERSTBA_LO registers available at the following address offsets:
ERSTBA_LO0: at offset 2030h
ERSTBA_LO1: at offset 2050h
ERSTBA_LO2: at offset 2070h
ERSTBA_LO3: at offset 2090h
ERSTBA_LO4: at offset 20B0h
ERSTBA_LO5: at offset 20D0h
ERSTBA_LO6: at offset 20F0h
ERSTBA_LO7: at offset 2110h

Access Method

Type: MEM Register (Size: 32 bits)
Device: 20
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RW	**Event Ring Segment Table Base Address Register (ERSTBA):** This field defines the low order bits of the start address of the Event Ring Segment Table. This field shall not be modified if HCHalted (HCH) = 0.
5:0	0h RO	Reserved.

21.2.28 Event Ring Segment Table Base Address High x (ERSTBA_HIx)—Offset 2034h

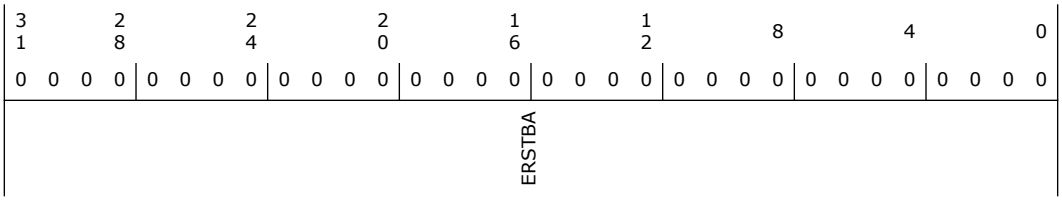
There are 8 ERSTBA_HI registers available at the following address offsets:
ERSTBA_HI0: at offset 2034h
ERSTBA_HI1: at offset 2054h

ERSTBA_HI2: at offset 2074h
ERSTBA_HI3: at offset 2094h
ERSTBA_HI4: at offset 20B4h
ERSTBA_HI5: at offset 20D4h
ERSTBA_HI6: at offset 20F4h
ERSTBA_HI7: at offset 2114h

Access Method

Type: MEM Register (Size: 32 bits)
Device: 20
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Event Ring Segment Table Base Address (ERSTBA):** This field defines the low order bits of the start address of the Event Ring Segment Table. This field shall not be modified if HCHalted (HCH) = 0.

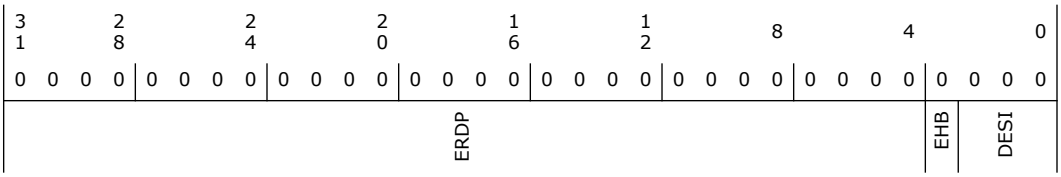
21.2.29 Event Ring Dequeue Pointer Low x (ERDP_LOx)—Offset 2038h

There are 8 ERDP_LO registers available at the following address offsets:
ERDP_LO0: at offset 2038h
ERDP_LO1: at offset 2058h
ERDP_LO2: at offset 2078h
ERDP_LO3: at offset 2098h
ERDP_LO4: at offset 20B8h
ERDP_LO5: at offset 20D8h
ERDP_LO6: at offset 20F8h
ERDP_LO7: at offset 2118h

Access Method

Type: MEM Register (Size: 32 bits)
Device: 20
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RW	**Event Ring Dequeue Pointer (ERDP):** This field may be used by the xHC to accelerate checking the Event Ring full condition. This field is written with the low order 3 bits of the offset of the ERST entry which defines the Event Ring segment that Event Ring Dequeue Pointer resides in.
3	0h RW/C	**Event Handler Busy (EHB):** This flag shall be set to '1' when the IP bit is set to '1' and cleared to '0' by software when the Dequeue Pointer register is written.
2:0	0h RW	**Dequeue ERST Segment Index (DESI):** This field may be used by the xHC to accelerate checking the Event Ring full condition. This field is written with the low order 3 bits of the offset of the ERST entry which defines the Event Ring segment that Event Ring Dequeue Pointer resides in.

21.2.30 Event Ring Dequeue Pointer High x (ERDP_HIx)—Offset 203Ch

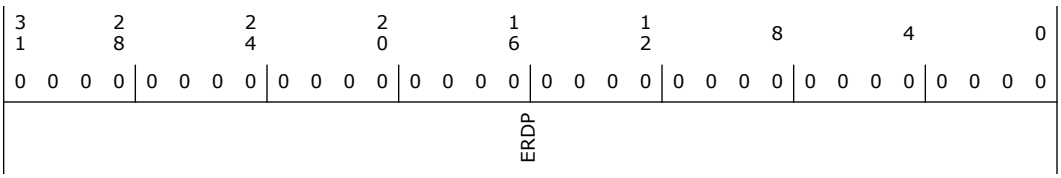
There are 8 ERDP_LO registers available at the following address offsets:
ERDP_HI0: at offset 203Ch
ERDP_HI1: at offset 205Ch
ERDP_HI2: at offset 207Ch
ERDP_HI3: at offset 209Ch
ERDP_HI4: at offset 20BCh
ERDP_HI5: at offset 20DCh
ERDP_HI6: at offset 20FCh
ERDP_HI7: at offset 211Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 20
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Event Ring Dequeue Pointer (ERDP):** This field defines the low order bits of the 64- bit address of the current Event Ring Dequeue Pointer.

21.2.31 Door Bell x (DBx)—Offset 3000h

Door Bell registers are an array of 32 registers.
The door bell registers are at the following offset:

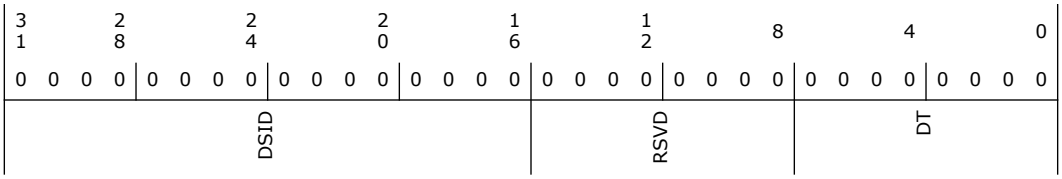
Door Bell 0: 3000-3003h
Door Bell 1: 3004-3007h
.....
Door Bell 30: 3078-307Bh
Door Bell 31: 307C-307Fh

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 20
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**DB Stream ID (DSID):** If the endpoint of a Device Context Doorbell defines Streams, then this field shall be used to identify which Stream of the endpoint the doorbell reference is targeting. System software is responsible for ensuring that the value written to this field is valid. If the endpoint does not define Streams (MaxPStreams = 0) and a non-'0' value is written to this field, the doorbell reference shall be ignored. This field only applies to Device Context Doorbells and shall be cleared to '0' for Host Controller Commands. This field returns '0' when read.
15:8	0h RO	Reserved.
7:0	0h RW	**DB Target (DT):** This field defines the target of the doorbell reference. The table below defines the xHC notification that is generated by ringing the doorbell. Doorbell Register 0 is dedicated to Command Ring and decodes this field differently than the other Doorbell Registers. Refer to the xHCI Specification for definitions of the values.

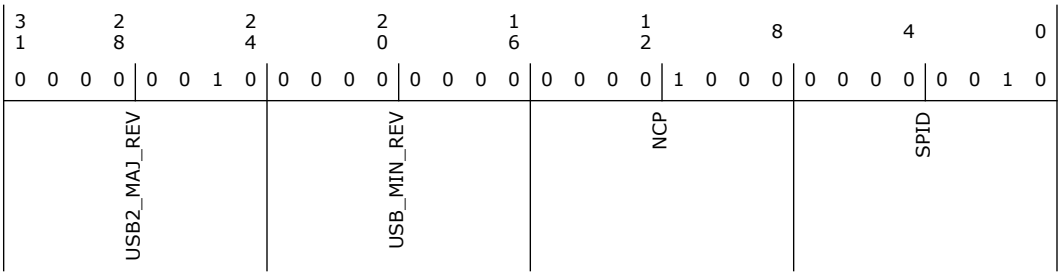
21.2.32 XECP_SUPP_USB2_0 (XECP_SUPP_USB2_0)—Offset 8000h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 20
Function: 0

Default: 2000802h



Bit Range	Default & Access	Field Name (ID): Description
31:24	2h RO	**USB Major Revision: 2.0 (USB2_MAJ_REV):** Major Specification Release Number in Binary-Coded Decimal (i.e., version 3.x is 03h). This field identifies the major release number component of the specification with which the xHC is compliant.
23:16	0h RO	**USB Minor Revision (USB_MIN_REV):** Minor Specification Release Number in Binary-Coded Decimal (i.e., version x.10 is 10h). This field identifies the minor release number component of the specification with which the xHC is compliant.
15:8	8h RO	**Next Capability Pointer (NCP):** This field indicates the location of the next capability with respect to the effective address of this capability. Refer to Table 145 for more information on this field.
7:0	2h RO	**Supported Protocol ID (SPID):** This field identifies the xHCI Extended capability. Refer to Table 146 for a list of the valid xHCI extended capabilities.

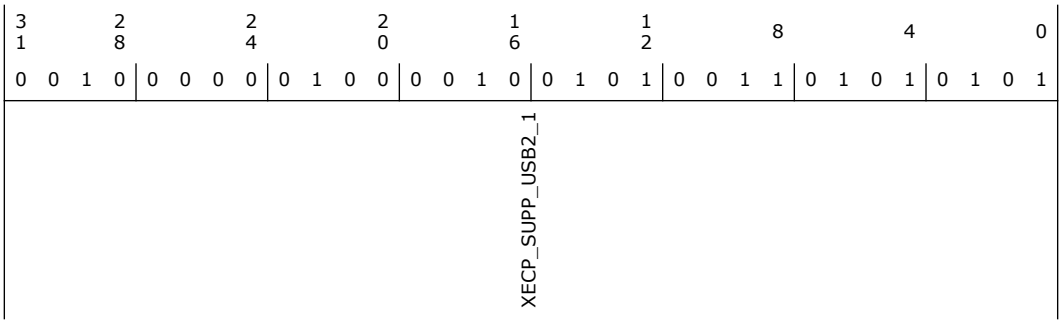
21.2.33 XECP_SUPP_USB2_1 (XECP_SUPP_USB2_1)—Offset 8004h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 20
Function: 0

Default: 20425355h



Bit Range	Default & Access	Field Name (ID): Description
31:0	20425355h RO	**XECP_SUPP_USB2_1 (XECP_SUPP_USB2_1):** This field is a mnemonic name string that references the specification with which the xHC is compliant. Four ASCII characters may be defined. Allowed characters are: alphanumeric, space, and underscore. Alpha characters are case sensitive.

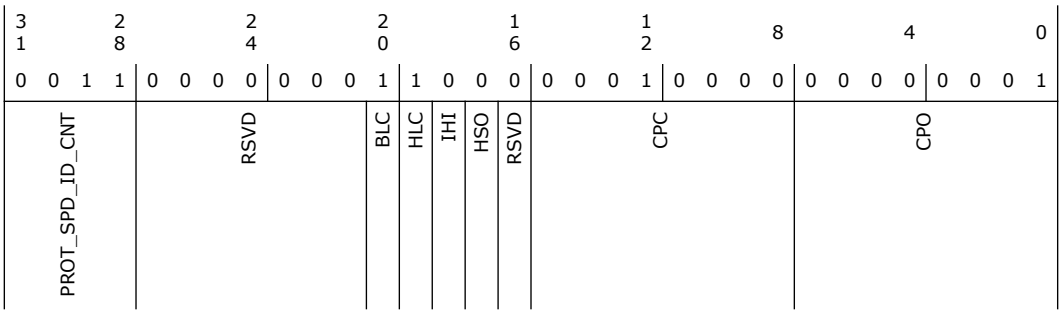
21.2.34 XECP_SUPP_USB2_2 (XECP_SUPP_USB2_2)—Offset 8008h

Access Method

Type: MEM Register (Size: 32 bits)

Device: 20
Function: 0

Default: 30181001h



Bit Range	Default & Access	Field Name (ID): Description
31:28	3h RO	**Protocol Speed ID Count (PROT_SPD_ID_CNT):** 3 USB 2.0 Speed (High, Full, Low)
27:21	0h RO	Reserved.
20	1h RW/L	**BESL LPM Capability (BLC):** Bit is set to 1 to indicate that the the ports described by this xHCI Supported Protocol Capability will apply BESL timing to BESL and BESLD fields of the PORTPMSC and PORTHLPMCC registers.

Bit Range	Default & Access	Field Name (ID): Description
19	1h RW/L	**Protocol Defined - Hardware LMP Capability (HLC)**
18	0h RO	**Protocol Defined - Integrated Hub Implementation (IHI)**
17	0h RO	**Protocol Defined - High SPeed Only (HSO):** This field indicates the number of Protocol Speed ID (PSI) Dwords that the xHCI Supported Protocol Capability data structure contains. If this field is non-zero, then all speeds supported by the protocol shall be defined using PSI Dwords, i.e. no implied Speed ID mappings apply.
16	0h RO	Reserved.
15:8	10h RO	**Compatible Port Count (CPC):** This field identifies the number of consecutive Root Hub Ports (starting at the Compatible Port Offset) that support this protocol. Valid values are 1 to MaxPorts.
7:0	1h RO	**Compatible Port Offset (CPO):** This field specifies the starting Port Number of Root Hub Ports that support this protocol. Valid values are '1' to MaxPorts.

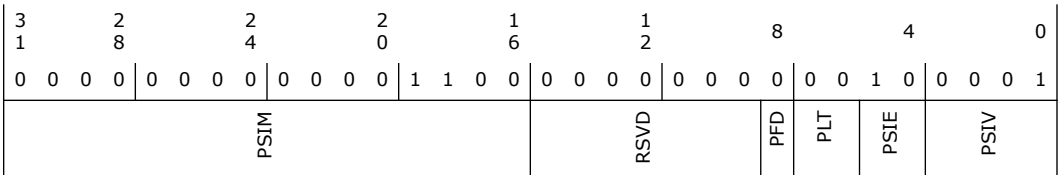
21.2.35 XECP_SUPP_USB2_3 (Full Speed) (XECP_SUPP_USB2_3)—Offset 8010h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 20
Function: 0

Default: C0021h



Bit Range	Default & Access	Field Name (ID): Description
31:16	Ch RO	**Protocol Speed ID Mantissa (PSIM):** This field defines the mantissa that shall be applied to the PSIE when calculating the maximum bit rate represented by this PSI Dword.
15:9	0h RO	Reserved.
8	0h RO	**PSI Full Duplex (PFD):** If this bit is '1' the link is full-duplex (dual-simplex), and if '0' the link is half-duplex (simplex).

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**PSI Type (PLT):** This field identifies whether the PSI Dword defines a symmetric or asymmetric bit rate, and if asymmetric, then this field also indicates if this Dword defines the receive or transmit bit rate. Note that the Asymmetric PSI Dwords shall be paired, i.e. an Rx immediately followed by a Tx, and both Dwords shall define the same value for the PSIV. PLT Value Bit Rate Note 0 Symmetric Single PSI Dword 1 Reserved 2 Asymmetric Rx Paired with Asymmetric Tx PSI Dword 3 Asymmetric Tx Immediately follows Rx Asymmetric PSI Dword
5:4	2h RO	**Protocol Speed ID Exponent (PSIE):** This field defines the base 10 exponent times 3, that shall be applied to the Protocol Speed ID Mantissa when calculating the maximum bit rate represented by this PSI Dword. PSIE Value Bit Rate 0 Bits per second 1 Kb/s 2 Mb/s 3 Gb/s
3:0	1h RO	**Protocol Speed ID Value (PSIV):** . If a device is attached that operates at the bit rate defined by this PSI Dword, then the value of this field shall be reported in the Port Speed field of PORTSC register (5.4.8) of a compatible port. Note, the PSIV value of '0' is reserved and shall not be defined by a PSI.

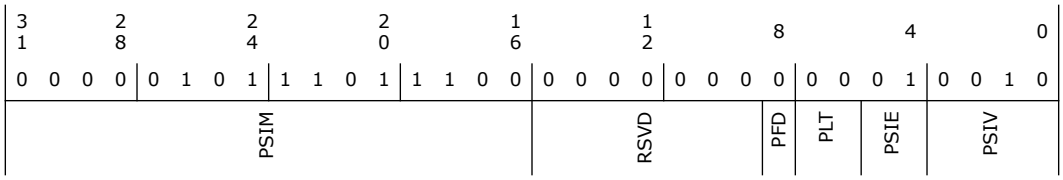
21.2.36 XECP_SUPP_USB2_4 (Low Speed) (XECP_SUPP_USB2_4)—Offset 8014h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 20
Function: 0

Default: 5DC0012h



Bit Range	Default & Access	Field Name (ID): Description
31:16	5DCh RO	**Protocol Speed ID Mantissa (PSIM)**
15:9	0h RO	Reserved.
8	0h RO	**PSI Full Duplex (PFD)**
7:6	0h RO	**PSI Type (PLT)**
5:4	1h RO	**Protocol Speed ID Exponent (PSIE)**
3:0	2h RO	**Protocol Speed ID Value (PSIV)**

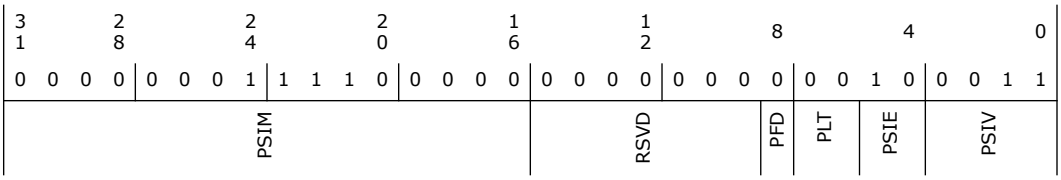
21.2.37 XECP_SUPP_USB2_5 (High Speed) (XECP_SUPP_USB2_5)—Offset 8018h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 20
Function: 0

Default: 1E00023h



Bit Range	Default & Access	Field Name (ID): Description
31:16	1E0h RO	**Protocol Speed ID Mantissa (PSIM)**
15:9	0h RO	Reserved.
8	0h RO	**PSI Full Duplex (PFD)**
7:6	0h RO	**PSI Type (PLT)**
5:4	2h RO	**Protocol Speed ID Exponent (PSIE)**
3:0	3h RO	**Protocol Speed ID Value (PSIV)**

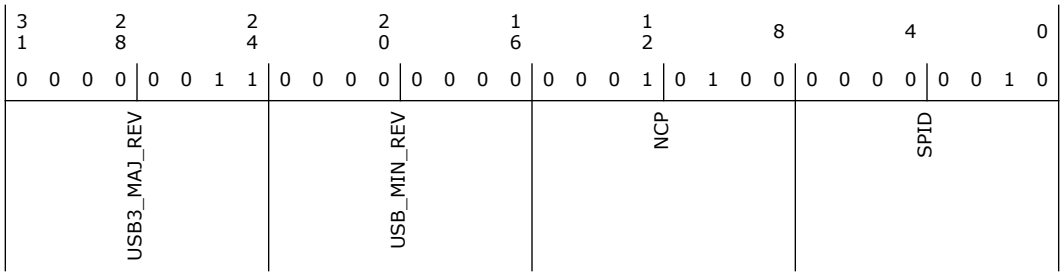
21.2.38 XECP_SUPP_USB3_0 (XECP_SUPP_USB3_0)—Offset 8020h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 20
Function: 0

Default: 3001402h



Bit Range	Default & Access	Field Name (ID): Description
31:24	3h RO	**USB Major Revision: 3.0 (USB3_MAJ_REV)**
23:16	0h RO	**USB Minor Revision (USB_MIN_REV)**
15:8	14h RO	**Next Capability Pointer (NCP)**
7:0	2h RO	**Supported Protocol ID (SPID)**

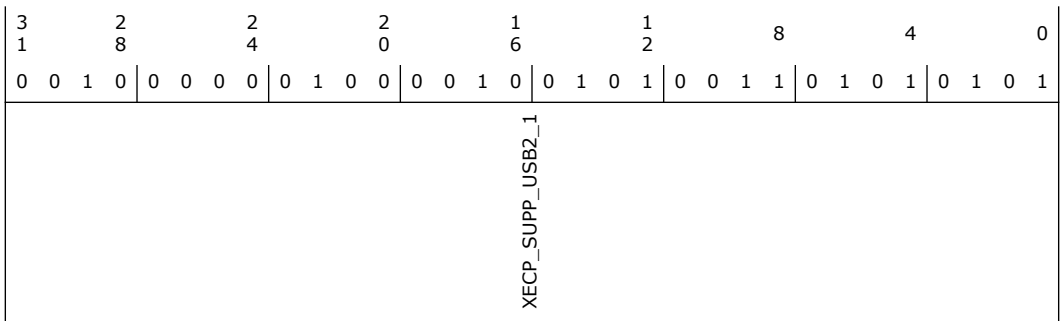
21.2.39 XECP_SUPP_USB3_1 (XECP_SUPP_USB3_1)—Offset 8024h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 20
Function: 0

Default: 20425355h



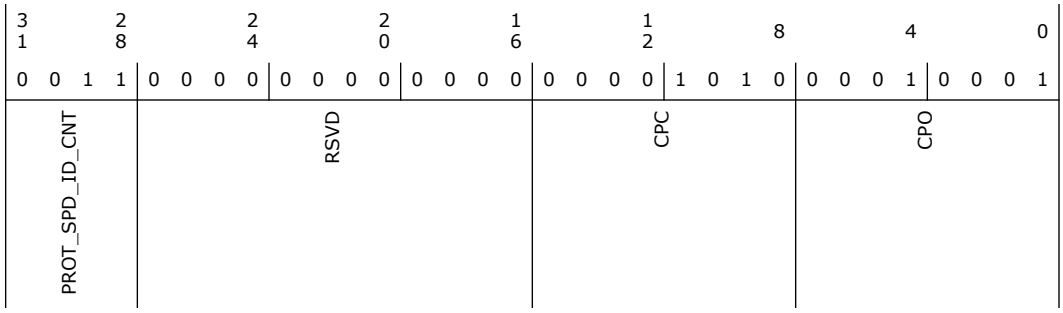
Bit Range	Default & Access	Field Name (ID): Description
31:0	20425355h RO	**XECP_SUPP_USB2_1 (XECP_SUPP_USB2_1):** Namestring USB

21.2.40 XECP_SUPP_USB3_2 (XECP_SUPP_USB3_2)—Offset 8028h

Access Method

Type: MEM Register (Size: 32 bits)
Device: 20
Function: 0

Default: 30000A11h



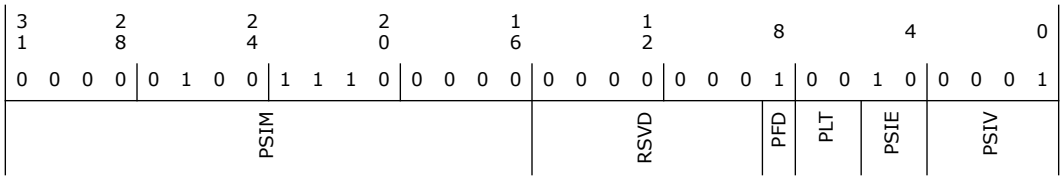
Bit Range	Default & Access	Field Name (ID): Description
31:28	3h RO	**Protocol Speed ID Count (PROT_SPD_ID_CNT):** 1 USB 3.0 Speed (Supper Speed)
27:16	0h RO	Reserved.
15:8	Ah RO	**Compatible Port Count (CPC)**
7:0	11h RO	**Compatible Port Offset (CPO)**

21.2.41 XECP_SUPP_USB3_3 (XECP_SUPP_USB3_3)—Offset 8030h

Access Method

Type: MEM Register (Size: 32 bits)
Device: 20
Function: 0

Default: 4E00121h



Bit Range	Default & Access	Field Name (ID): Description
31:16	4E0h RO	**Protocol Speed ID Mantissa (PSIM)**
15:9	0h RO	Reserved.
8	1h RO	**PSI Full Duplex (PFD)**
7:6	0h RO	**PSI Type (PLT)**
5:4	2h RO	**Protocol Speed ID Exponent (PSIE)**
3:0	1h RO	**Protocol Speed ID Value (PSIV)**

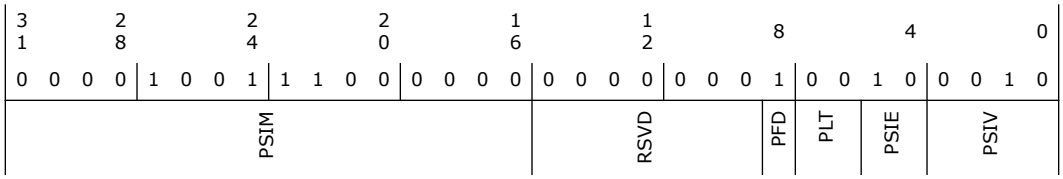
21.2.42 XECP_SUPP_USB3_4 (XECP_SUPP_USB3_4)—Offset 8034h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 20
Function: 0

Default: 9C00122h



Bit Range	Default & Access	Field Name (ID): Description
31:16	9C0h RO	**Protocol Speed ID Mantissa (PSIM)**
15:9	0h RO	Reserved.
8	1h RO	**PSI Full Duplex (PFD)**

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**PSI Type (PLT)**
5:4	2h RO	**Protocol Speed ID Exponent (PSIE)**
3:0	2h RO	**Protocol Speed ID Value (PSIV)**

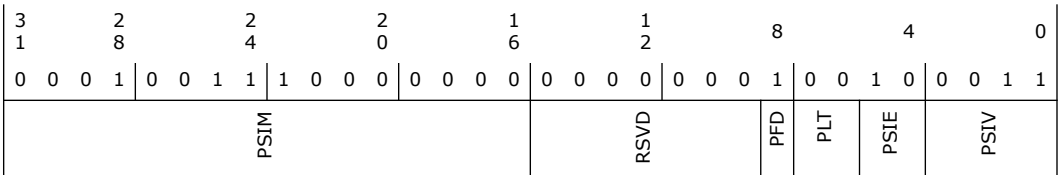
21.2.43 XECP_SUPP_USB3_5 (XECP_SUPP_USB3_5)—Offset 8038h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 20
Function: 0

Default: 13800123h



Bit Range	Default & Access	Field Name (ID): Description
31:16	1380h RO	**Protocol Speed ID Mantissa (PSIM)**
15:9	0h RO	Reserved.
8	1h RO	**PSI Full Duplex (PFD)**
7:6	0h RO	**PSI Type (PLT)**
5:4	2h RO	**Protocol Speed ID Exponent (PSIE)**
3:0	3h RO	**Protocol Speed ID Value (PSIV)**

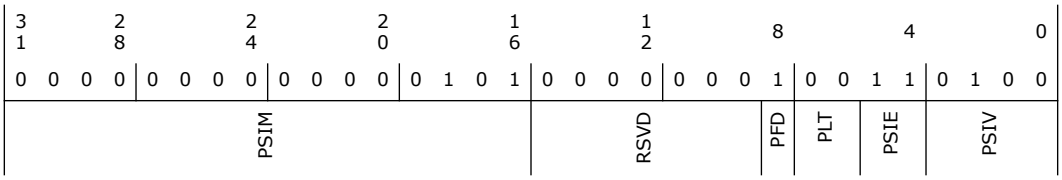
21.2.44 XECP_SUPP_USB3_6 (XECP_SUPP_USB3_6)—Offset 803Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 20
Function: 0

Default: 50134h



Bit Range	Default & Access	Field Name (ID): Description
31:16	5h RO	**Protocol Speed ID Mantissa (PSIM)**
15:9	0h RO	Reserved.
8	1h RO	**PSI Full Duplex (PFD)**
7:6	0h RO	**PSI Type (PLT)**
5:4	3h RO	**Protocol Speed ID Exponent (PSIE)**
3:0	4h RO	**Protocol Speed ID Value (PSIV)**

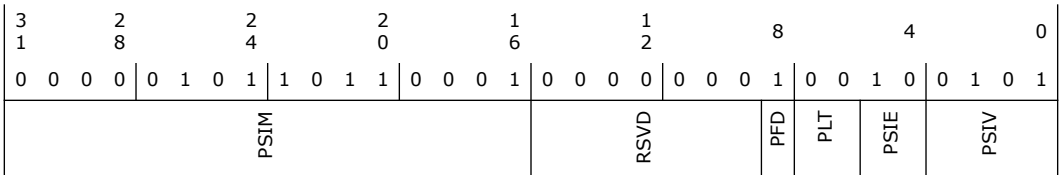
21.2.45 XECP_SUPP_USB3_7 (XECP_SUPP_USB3_7)—Offset 8040h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 20
Function: 0

Default: 5B10125h



Bit Range	Default & Access	Field Name (ID): Description
31:16	5B1h RO	**Protocol Speed ID Mantissa (PSIM)**
15:9	0h RO	Reserved.
8	1h RO	**PSI Full Duplex (PFD)**

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**PSI Type (PLT)**
5:4	2h RO	**Protocol Speed ID Exponent (PSIE)**
3:0	5h RO	**Protocol Speed ID Value (PSIV)**

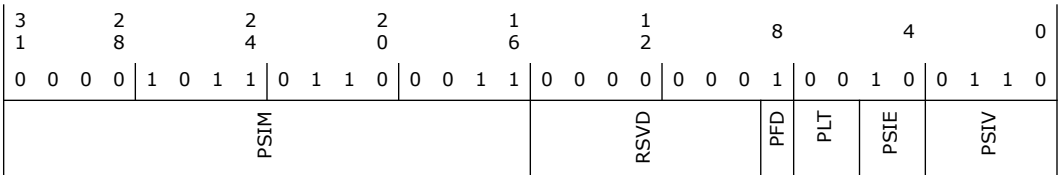
21.2.46 XECP_SUPP_USB3_8 (XECP_SUPP_USB3_8)—Offset 8044h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 20
Function: 0

Default: B630126h



Bit Range	Default & Access	Field Name (ID): Description
31:16	B63h RO	**Protocol Speed ID Mantissa (PSIM)**
15:9	0h RO	Reserved.
8	1h RO	**PSI Full Duplex (PFD)**
7:6	0h RO	**PSI Type (PLT)**
5:4	2h RO	**Protocol Speed ID Exponent (PSIE)**
3:0	6h RO	**Protocol Speed ID Value (PSIV)**

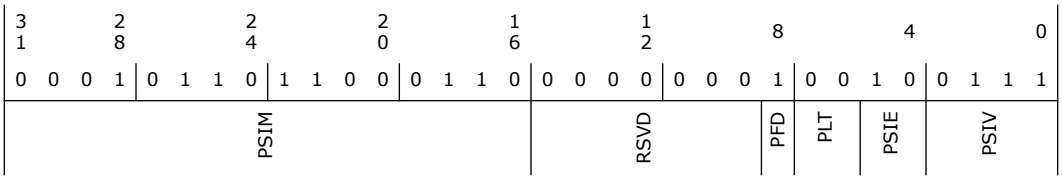
21.2.47 XECP_SUPP_USB3_9 (XECP_SUPP_USB3_9)—Offset 8048h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 20
Function: 0

Default: 16C60127h



Bit Range	Default & Access	Field Name (ID): Description
31:16	16C6h RO	**Protocol Speed ID Mantissa (PSIM)**
15:9	0h RO	Reserved.
8	1h RO	**PSI Full Duplex (PFD)**
7:6	0h RO	**PSI Type (PLT)**
5:4	2h RO	**Protocol Speed ID Exponent (PSIE)**
3:0	7h RO	**Protocol Speed ID Value (PSIV)**

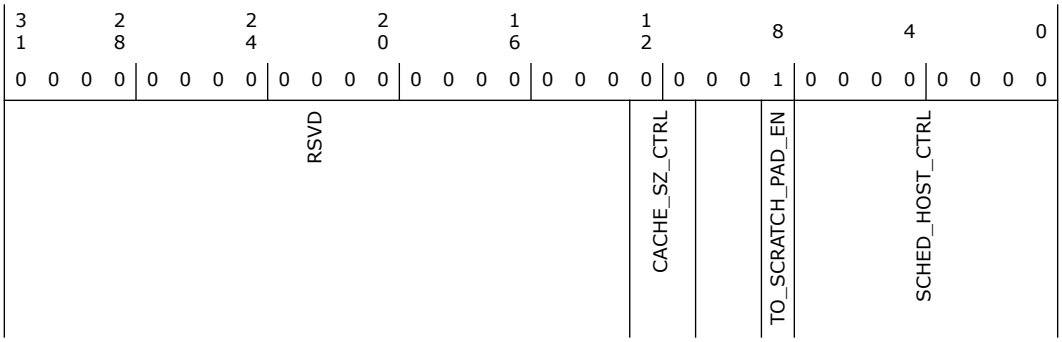
21.2.48 Host Control Scheduler (HOST_CTRL_SCH_REG)—Offset 8094h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 20
Function: 0

Default: 100h



Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	Reserved.
12:11	0h RW	**Cache Size Control Reg (CACHE_SZ_CTRL):** 0: 64 1: 32 2,3: 16
10:9	0h RW	**Reserved**
8	1h RW	**Turn on scratch_pad_en (TO_SCRATCH_PAD_EN)**
7:0	0h RW	**Scheduler Host Control Reg (SCHED_HOST_CTRL):** (0): disable poll delay (1): disable TRM active in EP valid check (2): enable TTE overlap prevention on interrupt IN EPs (at cost of possible service interval slip) (3) enable TTE overlap prevention on interrupt OUT EPs (at cost of possible service interval slip) (5:4) scheduler sort pattern 00 (default) search ISO ahead of interrupt within each service interval 01 - search USB2-ISO, USB3-ISO, USB2-Interrupt, USB3-Interrupt within each service interval 10 - search strictly by interval 11 - search all ISO intervals ahead interrupt intervals and within each interval, USB2 ahead of USB3 (6): disable 1 pack scheduling limit when ISO pending in present microframe (7): enable check to stop scheduling on port that are not connected

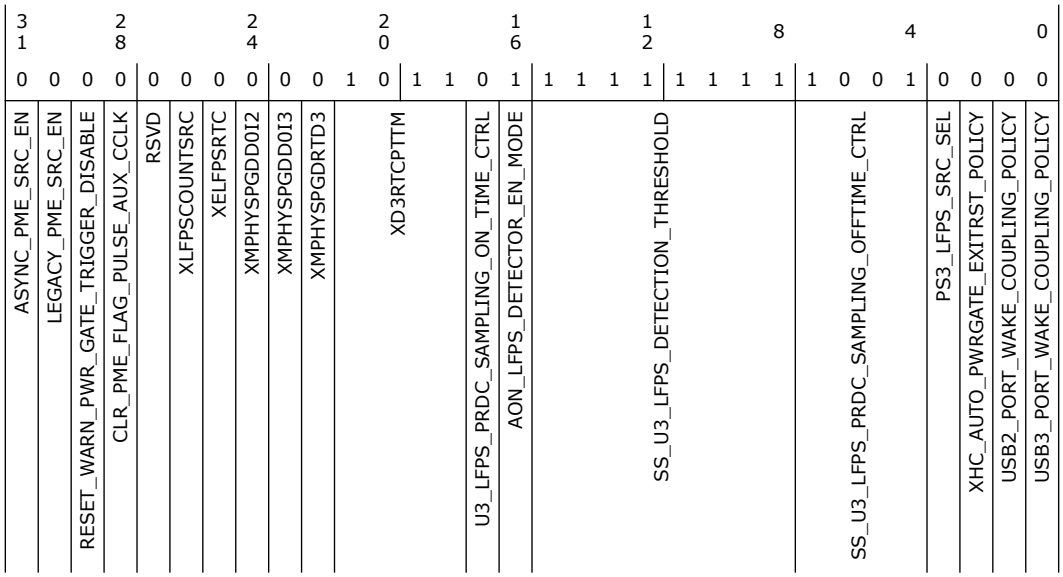
21.2.49 Power Management Control (PMCTRL_REG)—Offset 80A4h

Access Method

Type: MEM Register (Size: 32 bits)

Device: 20
Function: 0

Default: 2DFF90h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Async PME Source Enable (ASYNC_PME_SRC_EN):** This field allows the async PME source to be allowed to generate PME. This is specifically required for SOCs that do not allow for any clock other than RTC to be available during RTD3.
30	0h RW	**Legacy PME Source Enable (LEGACY_PME_SRC_EN):** This field allows the legacy PME source to be used in PME generation. The legacy source in in reference to the source prior to the RTD3 changes.
29	0h RW	**Reset Warn Power Gate Trigger Disable (RESET_WARN_PWR_GATE_TRIGGER_DISABLE):** This field controls the actions taken for due to reset warn. 0 - Reset Warn will trigger a HW autonomous Power Gate 1 - Reset Warn will not trigger a HW autonomous Power Gate
28	0h RW	**CLR_PME_FLAG_PULSE_AUX_CCLK (CLR_PME_FLAG_PULSE_AUX_CCLK):** Internal PME flag Clear This Write-Only bit can be used to clear the internal PME flag. SW write to '1' will clear the PME flag. SW write to '0' will have no effect and be ignored by the controller.
27	0h RO	Reserved.
26	0h RW	**XLFPSCOUNTSRC (XLFPSCOUNTSRC):** XLFPSCOUNTSRC (Source for LFPS OFF Counter) 0: Central RTC Counter for LFPS detection 1: Local Counter for LFPS detection
25	0h RW	**XELFPSRTC (XELFPSRTC):** XELFPSRTC (Enable LFPS Filtering on RTC) 0: Use Oscillator clock for LFPS Filtering during P3 1: Use RTC Clock for LFPS Filtering during P3

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**XMPHYSPGDD0I2 (XMPHYSPGDD0I2):** XMPHYSPGDD0I2 (ModPhy Sus Well Power Gate Disable for D0I2) 0 : Modphy sus well power gating enabled 1 : Modphy sus well power gating disabled
23	0h RW	**XMPHYSPGDD0I3 (XMPHYSPGDD0I3):** XMPHYSPGDD0I3 (ModPhy Sus Well Power Gate Disable for D0I3) 0 : Modphy sus well power gating enabled 1 : Modphy sus well power gating disabled
22	0h RW	**XMPHYSPGDRTD3 (XMPHYSPGDRTD3):** XMPHYSPGDRTD3 (ModPhy Sus Well Power Gate Disable for RTD3) 0 : Modphy sus well power gating enabled 1 : Modphy sus well power gating disabled
21:18	Bh RW	**XD3RTCPTTM (XD3RTCPTTM):** XD3RTCPTTM (D3 RTC Port Timer Tick Multiplier) This register will be the multiplication factor for determining SSIC Wake Detection Frequency and RXDET based on the XD3RTCPTTC value. If XD3RTCPTTC is 9h and this register is Bh, frequency for RXDET and SSIC H8EXIT detection while MODPHY SUS Power gating is enabled would be 99ms.
17	0h RW	**U3 LFPS Periodic Sampling ON Time Control (U3_LFPS_PRDC_SAMPLING_ON_TIME_CTRL):** This field controls the ON time for the LFPS periodic sampling for USB3/ SSIC ports. 0 ON time is 2 rtc clocks 1 ON time is 3 rtc clocks Note: This field is ignored if USB3/SSIC PHY SUS Well Power Gating is enabled.
16	1h RW	**AON LFPS Detector Enable Mode (AON_LFPS_DETECTOR_EN_MODE):** 1 - Allow the LFSP Detector in AON to own LFPS detection when the port is in PS3 for U2/U3 - not RxD regardless of port ownership. 0 - Allow the LFPS Detector in AON to own the LFPS detection only when the AON owns the port and in U2/U3 - not RxD
15:8	FFh RW	**SS U3 LFPS Detection Threshold (SS_U3_LFPS_DETECTION_THRESHOLD):** This field controls the threshold used to determine when a valid U3 Wake is detected through when using the unfiltered LFPS source. The value on this field will reflect the binary count required to have been detected on the counter being clocked by the unfiltered lfps source to result in a valid U3 wake detection.
7:4	9h RW	**SS_U3_LFPS_PRDC_SAMPLING_OFFTIME_CTRL (SS_U3_LFPS_PRDC_SAMPLING_OFFTIME_CTRL):** This field controls the OFF time for the LFPS periodic sampling for USB3 Ports 0x0 periodic sampling is disabled. 0x1 OFF time is 1ms 0x2 OFF time is 2ms 0xF OFF time is 15ms The ON Time is determined by the amount of time required to reliably determine if there is a valid LFPS and is HW implementation specific. A speed up mode shall be implemented where this field is in units of us. i.e. 0x1 = 1 us OFF time, 0x2 = 2 us OFF time, etc.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**PS3 LFPS Source Select (PS3_LFPS_SRC_SEL):** 0 LFPS Source is unfiltered 1 LFPS Source is filtered (Rx-Elec-Idle) LFPS Source is Rx-Elec-Idle for any non PS3 state.
2	0h RW	**XHCI Engine Autonomous Power Gate Exit Reset Policy (XHC_AUTO_PWRGATE_EXITRST_POLICY):** Controls when the xHCI engine is brought out of reset due to a power ungate. 0 Engine is brought out of reset when D3 to D0 is triggered. This allows for a quick power up sequence while leaving the virtual PCIe LTSSM in L23 is power ungate is not due to D3 to D0. 1 Engine is brought out of reset along with the rest of the IP. This is required for PMC save/restore flow.
1	0h RW	**USB2 Port Wake Unit Coupling Policy (USB2_PORT_WAKE_COUPLING_POLICY):** Controls the trigger for USB2 Port Wake Units to initiate Port Level Power Off Preparation. 0 RTD3 triggered 1 - Port Triggered when in L1, L2 or Disabled, Disconnected
0	0h RW	**USB3 Port Wake Unit Coupling Policy (USB3_PORT_WAKE_COUPLING_POLICY):** Controls the trigger for USB3 Port Wake Units to initiate Port Level Power Off Preparation. 0 - RTD3 Triggered 1 - Port Triggered when in PS3 due to RxDetect, U3, U2 or Disabled

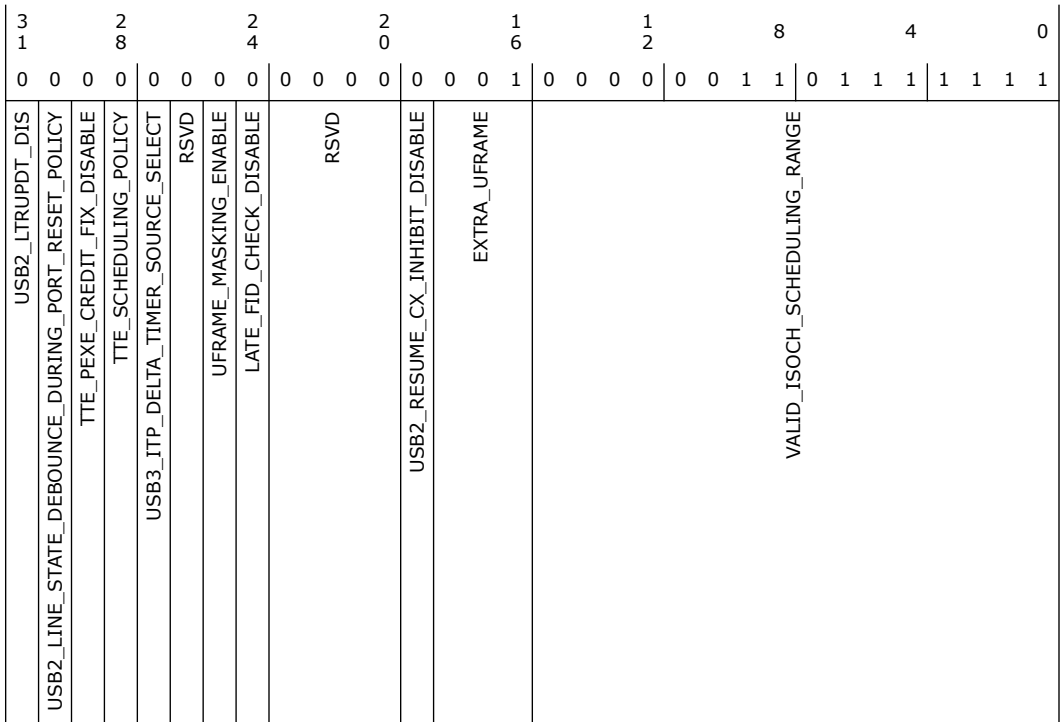
21.2.50 HOST_CTRL_MISC_REG (HOST_CTRL_MISC_REG)—Offset 80B0h

Access Method

Type: MEM Register (Size: 32 bits)

Device: 20
Function: 0

Default: 1037Fh



Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**USB2_LTRUPDT_DIS (USB2_LTRUPDT_DIS)**
30	0h RW	**USB2 Line State Debounce During Port Reset Policy (USB2_LINE_STATE_DEBOUNCE_DURING_PORT_RESET_POLICY):** This register controls how the debounce is enforced during the Port Reset phase. 0 do not enable the line state debounce during port reset. 1 enable the line state debounce during port reset.
29	0h RW	**TTE PEXE Credit Fix Disable (TTE_PEXE_CREDIT_FIX_DISABLE):** When set, it disables a fix implemented to re-deem PEXE credits when a port is disconnected
28	0h RW	**TTE Scheduling policy (TTE_SCHEDULING_POLICY):** This register controls a fix made to prevent over-scheduling by not account for 188B in each uFrame. Setting this bit will disable the fix and allow for over-scheduling.
27	0h RW	**USB3 ITP Delta Timer Source Select (USB3_ITP_DELTA_TIMER_SOURCE_SELECT):** This register selects the source for the delta timer tracking used for ITP generation. 0 the source is a 16.666 ns tick generated from a crystal reference clock 1 - the source is a 16.666 ns tick generated from the aux_cclk. This field needs to remain in sync with Frame Timer Source Select to ensure the are both set or both cleared. There is no support for any other combination.

Bit Range	Default & Access	Field Name (ID): Description
26	0h RO	Reserved.
25	0h RW	**uFrame Masking Enable (UFRAME_MASKING_ENABLE):** If set, enables the uFrame tick to be masked due to ports being in U3/NC. This controls a fix made to disable the auto masking of uFrame tick due to port state w/o any pipeline idle condition. When cleared, we rely on gating of frame timer due to proper port state and idleness tracking from the pipeline.
24	0h RW	**Late FID Check Disable (LATE_FID_CHECK_DISABLE):** This register disables the Late FID Check performed when starting an ISOCH stream.
23:20	0h RO	Reserved.
19	0h RW	**USB2 Resume Cx Inhibit Disable (USB2_RESUME_CX_INHIBIT_DISABLE):** Controls if USB2 L1 Resume is allowed to contribute to DMA Active which will inhibit Cx state. 0 USB2 L1 Resume is allowed to inhibit Cx via DMA Active 1 USB2 L1 Resume is NOT allowed to inhibit Cx via DMA Active When cleared, Cx will only be inhibited when the DMA traffic for the port begins.
18:16	1h RW	**Extra uFrame (EXTRA_UFRAME):** This register controls the extra number of uFrames added onto the advancing of late FID check.
15:0	37Fh RW	**Valid Isoch Scheduling Range (VALID_ISOCH_SCHEDULING_RANGE):** This register defines the window in miliseconds from the current Frame that will be considered for scheduling in an upcoming Frame. Anything scheduled outside of this window will be considered as late and will trigger the Missed Service Error.

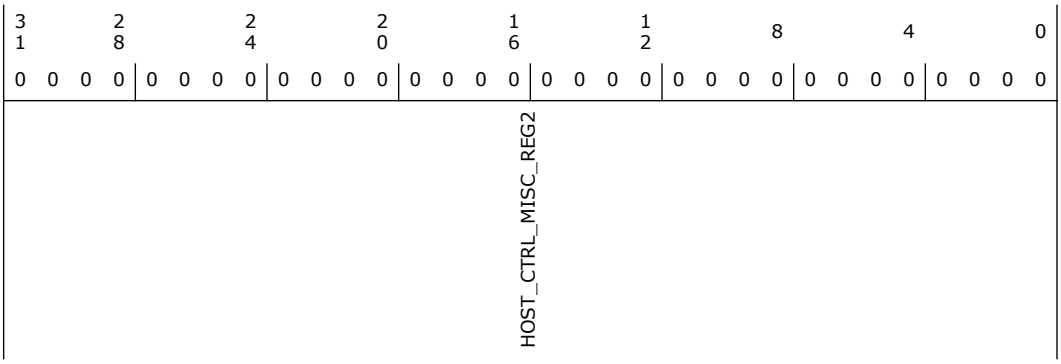
21.2.51 HOST_CTRL_MISC_REG2 (HOST_CTRL_MISC_REG2)—Offset 80B4h

Access Method

Type: MEM Register (Size: 32 bits)

Device: 20
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**HOST_CTRL_MISC_REG2 (HOST_CTRL_MISC_REG2)**

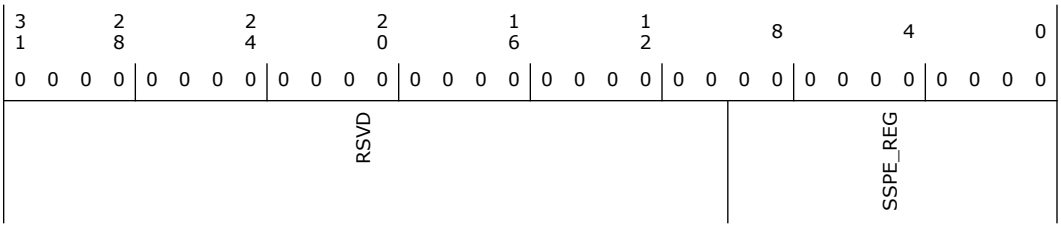
21.2.52 SSPE_REG (SSPE_REG)—Offset 80B8h

Access Method

Type: MEM Register (Size: 32 bits)

Device: 20
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:0	0h RW	**SSPE_REG (SSPE_REG)**

21.2.53 DEVICE MODE CONTROL REG 0 (DUAL_ROLE_CFG_REG0)—Offset 80D8h

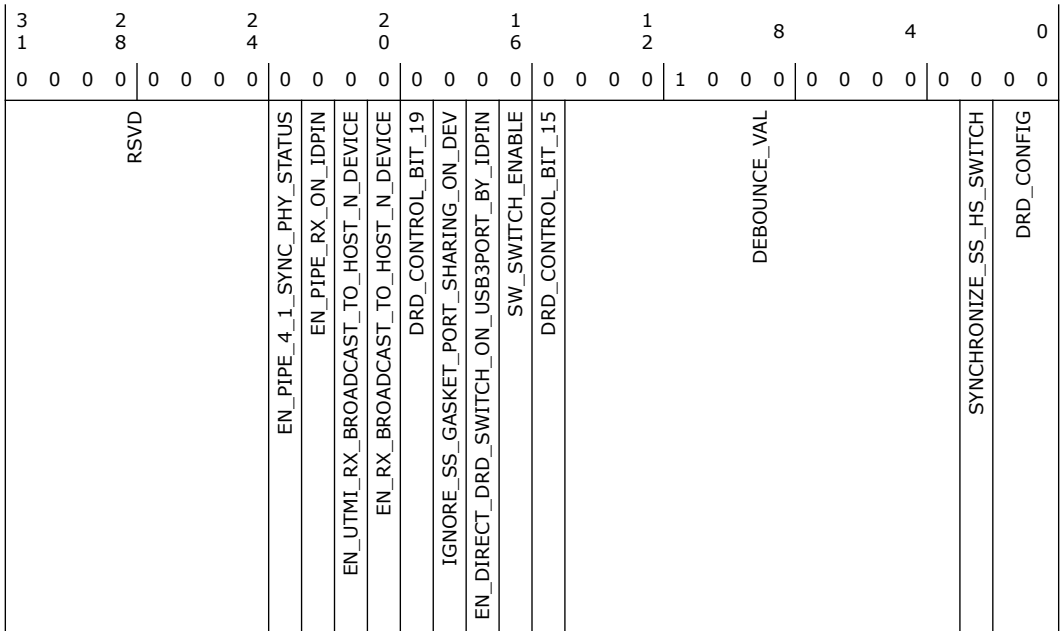
All bits in this register must be in the Always ON Power domain (ungated SUS or AON as appropriate)

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 20
Function: 0

Default: 800h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RW	**EN_PIPE_4_1_SYNC_PHY_STATUS (EN_PIPE_4_1_SYNC_PHY_STATUS)**
22	0h RW	**EN_PIPE_RX_ON_IDPIN (EN_PIPE_RX_ON_IDPIN):** During the connection to a device, there may be a delay in DRD switch from XDCI to XHCI mode,the rx term can be low after idpin deasserts. If this bit is 0, the rx term will be assert immediately after idpin toggle. Otherwise, the device may fall back to USB2 mode. 1 -- drive 0s on utmi rx signals to controller if not connected.
21	0h RW	**EN_UTMI_RX_BROADCAST_TO_HOST_N_DEVICE (EN_UTMI_RX_BROADCAST_TO_HOST_N_DEVICE):** 0 enable the utmi rx signal broadcast to both host and device 1 -- drive 0s on utmi rx signals to controller if not connected.
20	0h RW	**EN_RX_BROADCAST_TO_HOST_N_DEVICE (EN_RX_BROADCAST_TO_HOST_N_DEVICE):** 0 enable the rx signal broadcast to both host and device 1 -- drive 0s on rx signals to controller if not connected.
19	0h RW	**DRD_CONTROL_BIT_19 (DRD_CONTROL_BIT_19)**

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW	**IGNORE_SS_GASKET_PORT_SHARING_ON_DEV (IGNORE_SS_GASKET_PORT_SHARING_ON_DEV):** 0 ignore the SS gasket port sharing on device port 1 use the SS gasket port sharing
17	0h RW	**EN_DIRECT_DRD_SWITCH_ON_USB3PORT_BY_IDPIN (EN_DIRECT_DRD_SWITCH_ON_USB3PORT_BY_IDPIN):** 0 enable the direct DRD switch on USB3 port by idpin 1 disable the direct DRD switch
16	0h RW	**SW_SWITCH_ENABLE (SW_SWITCH_ENABLE):** SW switch enable 0 (default) ID pin HW controlled DRD. 1 -- SW controlled DRD (ignore idpin), switch based on the DRD_CONFIG.
15	0h RW	**DRD_CONTROL_BIT_15 (DRD_CONTROL_BIT_15)**
14:3	100h RW	**DEBOUNCE_VAL (DEBOUNCE_VAL):** ID ping debounce timer (DEBOUNCE_VAL): in the unit of RTC clock (33us) default to 8.448 ms
2	0h RW	**SYNCHRONIZE_SS_HS_SWITCH (SYNCHRONIZE_SS_HS_SWITCH):** Synchronize the SS and HS switch: 0 (default) Does not synchronize. i.e. HS switch on the debounced id pin, while SS switch independently controlled by the sequencer. 1 synchronize HS and SS switch. Both speeds switch when sequencer switch.
1:0	0h RW	**DRD_CONFIG (DRD_CONFIG):** 00 Dynamic DRD switch mode 01 static host mode 10 static device mode 11 -- reserved

21.2.54 AUX Power Management Control (AUX_CTRL_REG1)—Offset 80E0h

Access Method

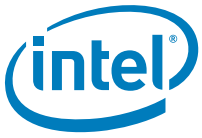
Type: MEM Register
(Size: 32 bits)

Device: 20
Function: 0

Default: 808D3CA0h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	0	0	0	0	0	1	0	0	0	1	1	0	1	0	0	1	1	1	1	0	0	1	0	1	0	0	0	0	0
D3_HOT_FXN_EN	ALL_L1_CORE_CG	AL_EP_SEXT	ALL_EP_RCP	AL_PERST_FRST	OVR_PCIE_P2_P1	SET_ISSV_1	CLR_ISSV_0	EN_SRE_SW_LD	RSVD	FORCE_SR1	CPTR	CIDS1	CIDS0	EN_CFG_UP2	CCGD	RSVD	EN_CFG_PIPE_RST	EN_FILT_TX_IDLE	EN_HE_GEN_PME	EN_ISOL	EN_L1_P2_OVR	EN_CORE_CG	EN_PHY_STS_TO	IGN_APE_PC	EN_P2_OVR_P1	EN_P2_REM_WAKE	FORCED_PM_STATE				INIT_FPMS

Bit Range	Default & Access	Field Name (ID): Description
31	1h RW	**D3 Hot function enable register (D3_HOT_FXN_EN):** This bit is from pin input which is set 1. But we allow software to alter it if it is needed. 1: D3 hot enabled 0: D3 hot not abled.
30	0h RW	**Allow L1 Core Clock Gating (ALL_L1_CORE_CG):** When set to 1 allows core clock being gated during L1 state.
29	0h RW	**Allow Engine PHY Status Extension (AL_EP_SEXT):** When set to 1 allows the engine to extend PHY status of PCIe PIPE for one more cycle. This is due to the fact that our rate change function has a potential of not being able to sample the phystatus signal.
28	0h RW	**Allow Engine PCIe Rate Change Passing (ALL_EP_RCP):** When set to 1 allows the engine to pass PCIe rate change signal as it is from PCIe core to PCIe PHY.
27	0h RW	**Allow Engine PERST Fundamental Reset (AL_PERST_FRST):** When set to 1 allow engine to treat PERST# as a foundamental reset
26	0h RW	**Overwrite PCIe P2 to P1 (OVR_PCIE_P2_P1):** When set to 1 will overwrite a PCIe powerdown state of P2 to P1.
25	0h RW	**Set Internal SSV 1 (SET_ISSV_1):** When set to 1 set the internal SSV to 1.
24	0h RW	**Clear Internal SSV 0 (CLR_ISSV_0):** When set to 1 clear the internal SSV to 0.
23	1h RW	**Enable save_restore_enable SW Loading (EN_SRE_SW_LD):** This is a bit that enables the save_restore_enable signal being loaded when a software command has set Save bit. This is a debug function.
22	0h RO	Reserved.
21	0h RW	**Force save_restore 1 (FORCE_SR1):** When set to 1, it will force the save_restore flag to 1. This flag is an bit to ensure that we have masked the update during low power state. If software write this bit to 1, it must write it to 0 in order to resume the normal save and restore function.
20	0h RW	**cfg pcie txreg rd (CPTR)**
19	1h RW	**cfg iob drivestrength[1] (CIDS1)**
18	1h RW	**cfg iob drivestrength[0] (CIDS0)**
17	0h RW	**Enable CFG USB P2 (EN_CFG_UP2):** When set to '1' enable cfg usb p2
16	1h RW	**cfg clk gate dis (CCGD)**
15	0h RO	Reserved.



Bit Range	Default & Access	Field Name (ID): Description
14	0h RW	**Enable CFG PIPE Reset (EN_CFG_PIPE_RST):** When set to '1' enable cfg pipe rst
13	1h RW	**Enable Filter TX Idle (EN_FILT_TX_IDLE):** When set to 1 enables a filter function to TX electrical idle signal at PCie PIPE. We have a filter that will set TXelecidle signal of PCIe PIPE to 1 whenever we are in isolation state or power down transition states.
12	1h RW	**Enable Host Engine Generate PME (EN_HE_GEN_PME):** This is a global switch to whether or not eable this host engine to generate PME message.
11	1h RW	**Enable Isolation (EN_ISOL):** When set to '1' enable isolation
10	1h RW	**Enable L1 Caused P2 Overwrite (EN_L1_P2_OVR):** Set 1 to enable a new feature. This new feature is designed to use L1 as a state to identify whether we should do P2 Overwrite or not. We used to use P1 state to identify whether or not to invoke P2 overwrite function.
9	0h RW	**Enable Core Clock Gating (EN_CORE_CG):** When set to '1' enable core clock gating based on low power state entered
8	0h RW	**Enable PHY Status Timeout (EN_PHY_STS_TO):** When set to '1' enable PHY status timeout function which is designed to cover the PCIePHY issue that we may have not able to detect the PHY status toggle.
7	1h RW	**Ignore aux_pm_en PCIe Core (IGN_APE_PC):** When set to '1' ignore the aux_pm_en reg from PCIe core to continue the remote wake/clock switching support
6	0h RW	**Enable P2 Overwrite P1 (EN_P2_OVR_P1):** When set to '1' enable P2 overwrite P1 when PCIe core has indicated the transition from P0 to P1. This is to enable entering the even lower power state.
5	1h RW	**Enable P2 Remote Wake (EN_P2_REM_WAKE):** When set 1 '1' enable the remote wake function by allowing P2 clock/ switching and P2 entering
4:1	0h RW	**Forced PM State (FORCED_PM_STATE)**
0	0h RW	**Initiate Force PM State (INIT_FPMS):** When set to '1' force PM state to go to the state indicated in bit 4:1

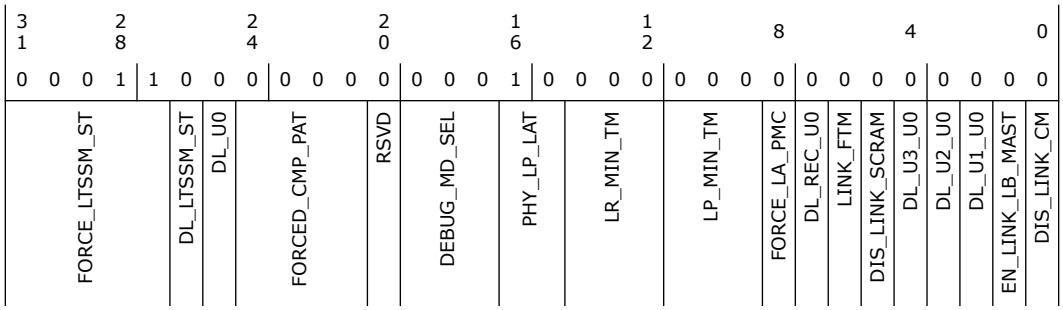
21.2.55 SuperSpeed Port Link Control (HOST_CTRL_PORT_LINK_REG)—Offset 80ECh

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 20
Function: 0

Default: 18010000h



Bit Range	Default & Access	Field Name (ID): Description
31:27	3h RW	**Force LTSSM State (FORCE_LTSSM_ST):** LTSSM state to be forced This value is for test purpose only.
26	0h RW	**Direct Link LTSSM State (DL_LTSSM_ST):** 0: Normal operation mode 1: Direct link to a specific state specified by bit 31:27 This bit is for test purpose only. It shall be written 0 in normal operation mode.
25	0h RW	**Direct Link To U0 (DL_U0):** 0: Normal operation mode 1: Direct link to U0 This bit is for test purpose only. It shall be written 0 in normal operation mode.
24:21	0h RW	**Forced Compliance Pattern (FORCED_CMP_PAT):** Compliance pattern to be forced to enter compliance mode This value is for test purpose only.
20	0h RO	Reserved.
19:17	0h RW	**Debug Mode Select (DEBUG_MD_SEL)**
16:15	2h RW	**PHY Low Power Latency (PHY_LP_LAT):** This field defines the latency to drive the PHY to enter low power mode 0: 4 cycles 1: 8 cycles 2: 16 cycles 3: 32 cycles
14:12	0h RW	**Link Recovery Minimum Time (LR_MIN_TM):** This value defines the minimum time for the link to stay in Recovery.Active other than from U3. The granuity is 128us.
11:9	0h RW	**Link Polling Minimum Time (LP_MIN_TM):** This value defines the minimum time for the link to stay in Polling.Active and Recovery.Active from U3. The granuity is 128us.
8	0h RW	**Force Link Accept PM Command (FORCE_LA_PMC):** 0: Normal operation mode 1: Force link to accept power management command
7	0h RW	**Direct Link Recovery U0 (DL_REC_U0):** 0: Normal operation mode 1: Direct link to Recovery from U0
6	0h RW	**Link Fast Training Mode (LINK_FTM):** 0: Normal operation mode 1: Link fast training mode This bit should be written 0 in normal operation.
5	0h RW	**Disable Link Scrambler (DIS_LINK_SCRAM):** 0: Enable link scrambler 1: Disable link scramber

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**Direct Link U3 From U0 (DL_U3_U0):** 0: Normal operation mode 1: Direct link to U3 from U0 This bit is for test purpose only. It shall be written 0 in normal operation mode.
3	0h RW	**Direct Link U3 From U0 (DL_U2_U0):** 0: Normal operation mode 1: Direct link to U2 from U0 This bit is for test purpose only. It shall be written 0 in normal operation mode.
2	0h RW	**Direct Link U3 From U0 (DL_U1_U0):** 0: Normal operation mode 1: Direct link to U1 from U0 This bit is for test purpose only. It shall be written 0 in normal operation mode.
1	0h RW	**Enable Link Loopback Master Mode (EN_LINK_LB_MAST):** 0: Disable link loopback master mode 1: Enable link loopback master mode
0	0h RW	**Disable Link Compliance Mode (DIS_LINK_CM):** 0: Enable link compliance mode 1: Disable link compliance mode

21.2.56 USB2 Port Link Control 1 (USB2_LINK_MGR_CTRL_REG1)—Offset 80F0h

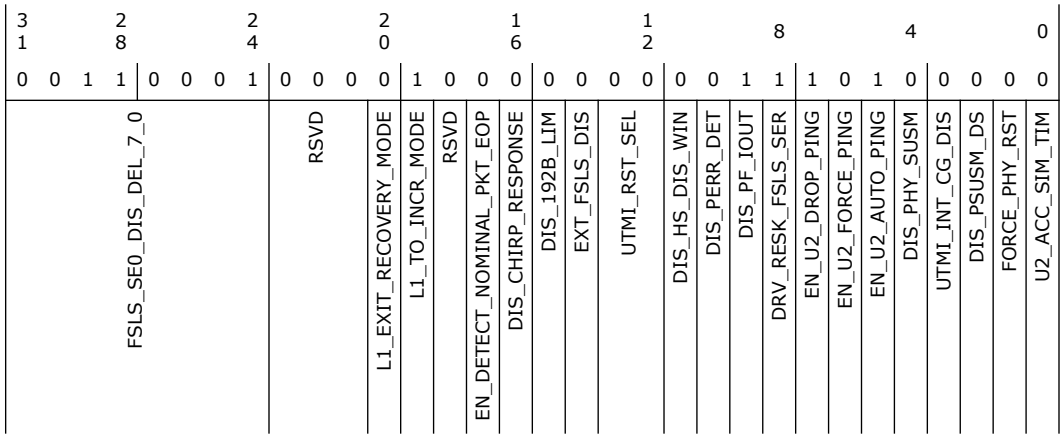
These set of registers is used to control jey USB set of timers. They are spread over 4 registers each 32 bits wide.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 20
Function: 0

Default: 310803A0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	31h RW	**FS/LS Mode SE0 Disconnect Delay[7:0] (FSLS_SE0_DIS_DEL_7_0):** # of microseconds of SE0 in FS/LS mode to register disconnect had occurred.
23:21	0h RO	Reserved.
20	0h RW	**L1_EXIT_RECOVERY_MODE (L1_EXIT_RECOVERY_MODE):** Mode for extended L1 Exit recovery delay: 0: 12us 1: 50us
19	1h RW	**L1_TO_INCR_MODE (L1_TO_INCR_MODE):** Mode select for L1 Timeout increments: 0: time out increments are in 125us 1: L1 Timeout increments are in 256us. Refer to USB2 PORTHLPMC.L1 Timeout in XHCI Spec for additional details
18	0h RO	Reserved.
17	0h RW	**EN_DETECT_NOMINAL_PKT_EOP (EN_DETECT_NOMINAL_PKT_EOP):** 0: Detect minimal packet EOP. 1: Detect nominal packet EOP.
16	0h RW	**Disable Chirp Response (DIS_CHIRP_RESPONSE):** 0: Normal 1: Force full speed on host ports (disable chirp response)
15	0h RW	**Disable 192 Byte Limit Check (DIS_192B_LIM):** 0: Enforce 192 byte limit on complete-split INs. Treat any packet) 192 as babble case. 1: Disable 192 byte limit check.
14	0h RW	**External Provided FS/LS Disconnect (EXT_FSLS_DIS):** 0: Internal FS/LS Disconnect from linestate(1:0) 1: External provided FS/LS Disconnect from hostdisconnect input
13:12	0h RW	**UTMI Reset Source Select (UTMI_RST_SEL):** Select UTMI Reset Source (FRD UTMI Reset Only) 00: HCReset or Force PHY Reset or internal reset after disconnect/suspend for restart (default) 01,11: UTMI reset = ~UTMI suspendm 10: UTMI reset = ~UTMI suspendm and synchronization to port clk.
11	0h RW	**Disable HS Disconnect Window (DIS_HS_DIS_WIN):** 0: Enable HS Disconnect Window Function 1: Disable HS Disconnect Window Function
10	0h RW	**Disable Port Error Detection (DIS_PERR_DET):** 0: Enable Port Error Detection (default) 1: Disable Port Error Detection
9	1h RW	**Disable Peek Function for ISO-OUT (DIS_PF_IOUT):** 0: Enable Peek function for ISO-OUT (default) 1: Disable Peek function for ISO-OUT
8	1h RW	**Drive Resume-K FS/LS Serial Interface (DRV_RESK_FSLS_SER):** 0: Drive Resume-K on parallel Interface 1: Drive Resume-K directly on FS/LS Serial Interface (default)
7	1h RW	**Enable USB2 Drop-Ping (EN_U2_DROP_PING):** 0: Disable Drop-Ping Function in USB2 Protocol (default) 1: Enable Drop-Ping Function in USB2 Protocol

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**Enable USB2 Force-Ping (EN_U2_FORCE_PING):** 0: Disable Force-Ping Function in USB2 Protocol (default) 1: Enable Force-Ping Function in USB2 Protocol
5	1h RW	**Enable USB2 Auto-Ping (EN_U2_AUTO_PING):** 0: Disable Auto-Ping Function 1: Enable Auto-Ping Function in USB2 Protocol (default)
4	0h RW	**Disable PHY SuspendM (DIS_PHY_SUSM):** 0: PHY is suspend=U3,U2,disconnect (default) 1: Disable PHY SuspendM in All States
3	0h RW	**UTMI Internal Clock Gate Disable (UTMI_INT_CG_DIS):** 0: Normal operation (internal clock gated in U2,U3,disconnect) 1: UTMI Internal Clock Gate Disable
2	0h RW	**Disable PHY SuspendM in Disconnect State (DIS_PSUSM_DS):** 0: PHY is suspendM=0 in Disconnect State (default) 1: Disable PHY SuspendM in Disconnect State
1	0h RW	**Force PHY Reset (FORCE_PHY_RST):** 0: Normal Operation (default) 1: Force PHY Reset
0	0h RW	**USB2 Accelerated Simulation Timing (U2_ACC_SIM_TIM):** 0: Normal Operation (default - FPGA/ASIC) 1: USB2 Accelerated Simulation Timing (default - simulation)

21.2.57 USB2 Port Link Control 4 (USB2_LINK_MGR_CTRL_REG4)—Offset 80FCh

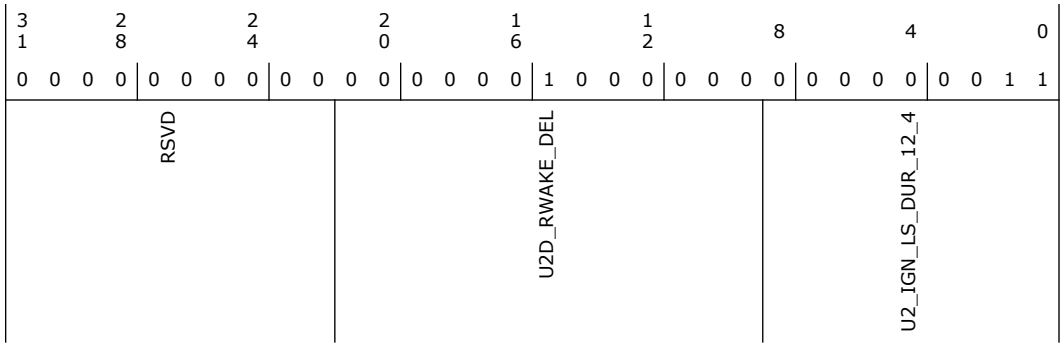
These set of registers is used to control jey USB set of timers. They are spread over 4 registers each 32 bits wide.

Access Method

Type: MEM Register (Size: 32 bits)

Device: 20
Function: 0

Default: 8003h



Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	Reserved.
21:9	40h RW	**U2 Detect Remote Wake Delay (U2D_RWAKE_DEL):** #of microseconds after detecting U2 remote wake condition to reflect K
8:0	3h RW	**U2 Entry Ignore Linestate Changes Duration[12:4] (U2_IGN_LS_DUR_12_4):** # of microseconds after entering U2, linestate changes are ignored as bus settles

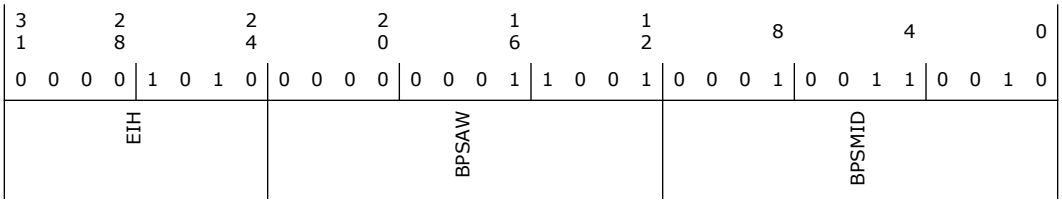
21.2.58 Power Scheduler Control-0 (PWR_SCHED_CTRL0)—Offset 8140h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 20
Function: 0

Default: A019132h



Bit Range	Default & Access	Field Name (ID): Description
31:24	Ah RW	**Engine Idle Hysteresis (EIH):** This register controls the min. idle span that has to be observed from the engine idle indicators before the power state flags (xhc_*_idle) will indicate a 1.
23:12	19h RW	**Backbone PLL Shutdown Advance Wake (BPSAW):** This register controls the time before the next scheduled transaction where the Backbone PLL request will assert. Register Format: Bits [11:7] # of 125us uframes Bits [6:0] # of microseconds (0-124)
11:0	132h RW	**Backbone PLL Shutdown Min. Idle Duration (BPSMID):** The sum of this register plus the Backbone PLL Shutdown Advance Wake form to a Total Idle time. When the next scheduled periodic transaction is after present time + Total Idle, the Backbone PLL request will de-assert, allowing the PLL to shutdwon. Register Format: Bits [11:7] # of 125us uframes Bits [6:0] # of microseconds (0-124)

21.2.59 Power Scheduler Control-2 (PWR_SCHED_CTRL2)—Offset 8144h

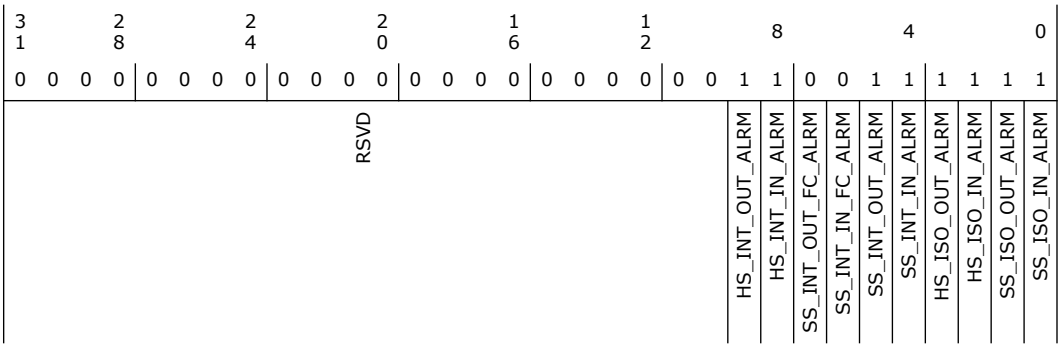
These bit enable by EP type those EPs classes that are considered for determining next periodic active interval for pre-wake of the periodic_active signal. EP classes that are disabled may never be observed in setting of the periodic_active signal.

Access Method

Type: MEM Register (Size: 32 bits)

Device: 20
Function: 0

Default: 33Fh



Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9	1h RW	**HS Interrupt-OUT Alarm (HS_INT_OUT_ALRM)**
8	1h RW	**HS Interrupt-IN Alarm (HS_INT_IN_ALRM)**
7	0h RW	**SS Interrupt-OUT FC Alarm (SS_INT_OUT_FC_ALRM)**
6	0h RW	**SS Interrupt-IN Alarm (SS_INT_IN_FC_ALRM)**
5	1h RW	**SS Interrupt-OUT & not in FC Alarm (SS_INT_OUT_ALRM)**
4	1h RW	**SS Interrupt-IN & not in FC Alarm (SS_INT_IN_ALRM)**
3	1h RW	**HS ISO-OUT Alarm (HS_ISO_OUT_ALRM)**
2	1h RW	**HS ISO-IN Alarm (HS_ISO_IN_ALRM)**
1	1h RW	**SS ISO-OUT Alarm (SS_ISO_OUT_ALRM)**
0	1h RW	**SS ISO-IN Alarm (SS_ISO_IN_ALRM)**

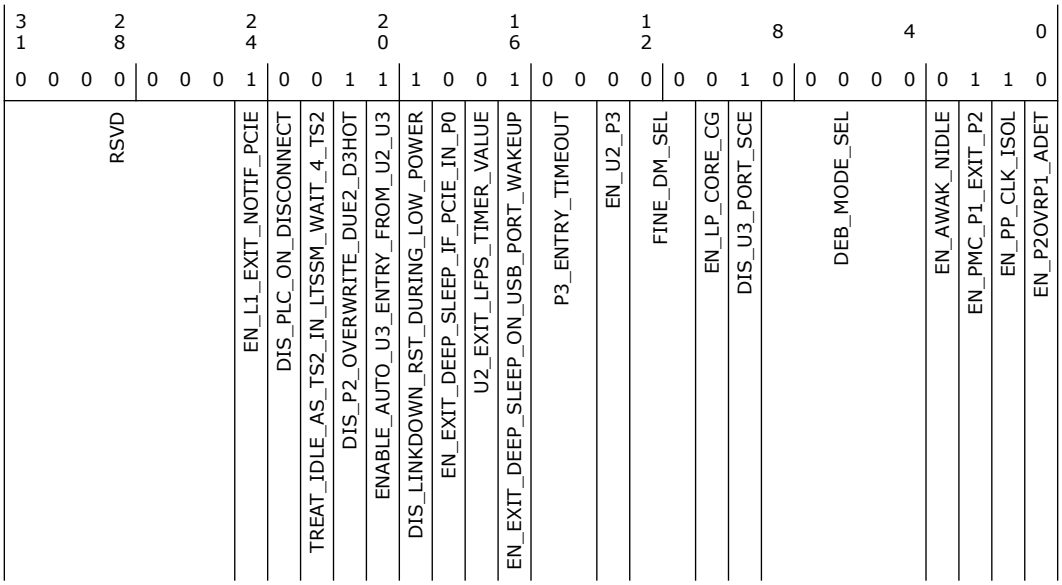
21.2.60 AUX Power Management Control (AUX_CTRL_REG2)—Offset 8154h

Access Method

Type: MEM Register (Size: 32 bits)

Device: 20
Function: 0

Default: 1390206h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	Reserved.
24	1h RW	**Enable L1 exit notification to SNPS PCIe core (EN_L1_EXIT_NOTIF_PCIE):** This bit enables a L1 exit notification to SNPS PCIe core. There is a case where USB ports have waked up and AUX PM module has started the wakeup process. The AUX PM control state got into a wait for P0 state because it needs to wait until PCIe core to signal powerdown state change. Due to the fact that the core is in D3Hot, there is no run_stop bit set such that no internal interrupt will be fired. This causes the LTSSM of PCIe stayed in L1 even though AUX PM has known that it needs an L1 exit. This bit works together with bit21 of this register. 1: enables this feature 0: disables this feature.
23	0h RW	**DISABLE PLC ON DISCONNECT (DIS_PLC_ON_DISCONNECT):** 1: do not assert PLC for disconnection 0: assert PLC for disconnection

Bit Range	Default & Access	Field Name (ID): Description
22	0h RW	**TREAT_IDLE_AS_TS2_IN_LTSSM_WAIT_4_TS2 (TREAT_IDLE_AS_TS2_IN_LTSSM_WAIT_4_TS2):** This bit enables a feature in PCie core LTSSM to treat IDLE received as TS2 when LTSSM is in wait for TS2 receive state. This is a function requested from PHY where it is possible to not able to receive TS2 without error. 1: treat Logic IDLE as TS2 received when in some PCIe LTSSM state. 0: disable this feature.
21	1h RW	**Disable p2 overwrite due to the D3HOT where PCIe core enters the L1 (DIS_P2_OVERWRITE_DUE2_D3HOT):** We added a feature where if PCIe core LTSSM enters L1 due to the D3hot, the aux PM control will not start a P2 overwrite function in anticipating for the next L23 enter. 1: disables p2 overwrite due to the D3HOT where PCIe core enters the L1. 0: enables P2 overwrite even if we are in D3Hot.
20	1h RW	**Enable the port to enter U3 automatically when in U1/U2 (ENABLE_AUTO_U3_ENTRY_FROM_U2_U3):** 1: enables the port to enter U3 automatically when in U1/U2 0: disables the port to enter U3 automatically when in U1/U2
19	1h RW	**No linkdown reset is issue during low power state (DIS_LINKDOWN_RST_DURING_LOW_POWER):** No linkdown reset is issue during low power state
18	0h RW	**EN_EXIT_DEEP_SLEEP_IF_PCIE_IN_P0 (EN_EXIT_DEEP_SLEEP_IF_PCIE_IN_P0):** This bit enables a feature in AUX PM module where if PCIe core LTSSM is in P0 for a duration of time, we will exit the deep sleep state. This is for failure control in case. 1: enables this feature 0: disable this feature
17	0h RW	**U2_EXIT_LFPS_TIMER_VALUE (U2_EXIT_LFPS_TIMER_VALUE):** This bit selects U2 exit LFPS timer value 0: 320ns 400ns in 25MHz domain 1: 240ns 320ns in 25MHz domain
16	1h RW	**EN_EXIT_DEEP_SLEEP_ON_USB_PORT_WAKEUP (EN_EXIT_DEEP_SLEEP_ON_USB_PORT_WAKEUP):** This bit enables a function that AUX PM module exits from the deep sleep state due to the USB ports wakeup level signal. We have added this feature where USB ports will generated a wakeup level signal to wakeup the AUX PM module if it is in deep sleep state and this level signal will be cleared if the change bits are updated by software. 1: enables this function 0: disables this function which means that a wakeup pulse generated from each USB PortSC event will wake up the AUX PM module from deep sleep if the D3 state is programmed.
15:14	0h RW	**P3_ENTRY_TIMEOUT (P3_ENTRY_TIMEOUT):** This field defines the timeout value to enter P3 mode in U2. 00: 7us 8us 01: 511us 512us 10: disables the timer (0us) 11: disables the timer (0us)
13	0h RW	**Enable U2 P3 Mode (EN_U2_P3):** 0: Disable U2 P3 mode 1: Enable U2 P3 mode

Bit Range	Default & Access	Field Name (ID): Description
12:11	0h RW	**Fine Debug Mode Select (FINE_DM_SEL)**
10	0h RW	**Enable Low Power State Based Core Clock Gating (EN_LP_CORE_CG):** When set to '1' enable core clock gating based on low power state entered
9	1h RW	**Disable USB3 Port Status Changed Event (DIS_U3_PORT_SCE):** 0: Enable USB3 port status change event generation if any change bit is not cleared 1: Disable USB3 port status change event generation if any change bit is not cleared Bit 12 default 0
8:4	0h RW	**Debug Mode Select Register (DEB_MODE_SEL)**
3	0h RW	**Enable Auto Wakeup Non-IDLE (EN_AWAK_NIDLE):** When set to 1 enables the auto wakeup function when engine has identified non IDLE condition.
2	1h RW	**Enable PM Control P1 Exit P2 (EN_PMC_P1_EXIT_P2):** When set 1 enables the PM control module to transition to P1 instead of P0 when exit P2.
1	1h RW	**Enable PCIe PIPE CLK Isolation (EN_PP_CLK_ISOL):** When set to 1 enables the PCIe PIPE CLK to be isolated when main power is removed.
0	0h RW	**Enable P2 Overwrite P1 Allowed Detect (EN_P2OVRP1_ADET):** When set to 1 enables a function that can detect whether or not enable P2 overwrite P1 function. The condition to get to P2 overwrite is when engine is in idle conditions. This means that there is no ISO EP pending.

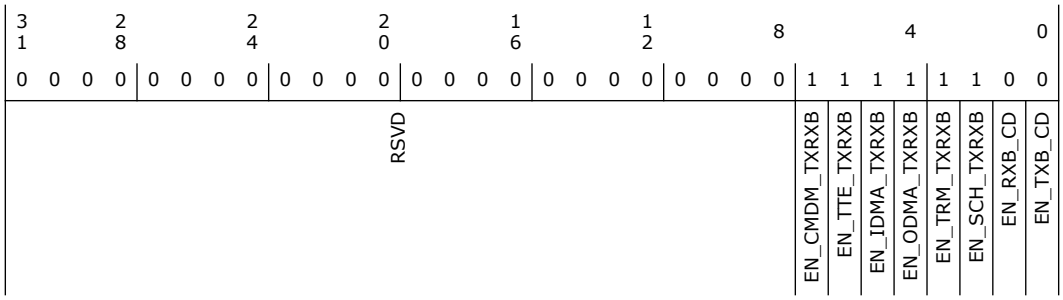
21.2.61 USB2 PHY Power Management Control (USB2_PHY_PMC)—Offset 8164h

Access Method

Type: MEM Register (Size: 32 bits)

Device: 20
Function: 0

Default: FCh



Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7	1h RW	**EN_CMDM_TXRXB (EN_CMDM_TXRXB):** Enable Command Manager Active indication for Tx/Rx Bias circuit HS Phy PM Policy
6	1h RW	**EN_TTE_TXRXB (EN_TTE_TXRXB):** Enable TTE Active indication for Tx/Rx Bias circuit HS Phy PM Policy
5	1h RW	**EN_IDMA_TXRXB (EN_IDMA_TXRXB):** Enable IDMA Active indication for Tx/Rx Bias circuit HS Phy PM Policy
4	1h RW	**EN_ODMA_TXRXB (EN_ODMA_TXRXB):** Enable ODMA Active indication for Tx/Rx Bias circuit HS Phy PM Policy
3	1h RW	**EN_TRM_TXRXB (EN_TRM_TXRXB):** Enable Transfer Manager Active indication for Tx/Rx Bias circuit HS Phy PM Policy
2	1h RW	**EN_SCH_TXRXB (EN_SCH_TXRXB):** Enable Scheduler Active indication for Tx/Rx Bias circuit HS Phy PM Policy
1	0h RW	**Enable Rx Bias ckt disable (EN_RXB_CD):** When set enables the Rx bias ckt to be disabled when conditions met (as described by the HS phy PM policy bits)
0	0h RW	**Enable Tx Bias ckt disable (EN_TXB_CD):** When set enables the Tx bias ckt to be disabled when conditions met (as described by the HS phy PM policy bits)

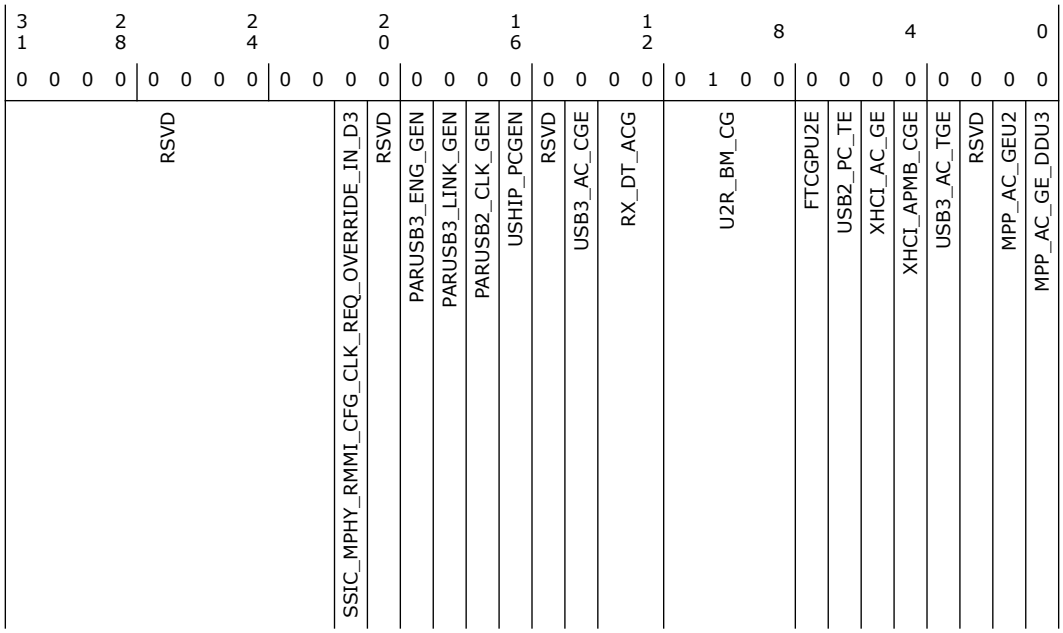
21.2.62 xHCI Aux Clock Control Register (XHCI_AUX_CCR)—Offset 816Ch

Access Method

Type: MEM Register (Size: 32 bits)

Device: 20
Function: 0

Default: 400h



Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	Reserved.
21	0h RW	**SSIC_MPHY_RMMI_CFG_CLK_REQ_OVERRIDE_IN_D3 (SSIC_MPHY_RMMI_CFG_CLK_REQ_OVERRIDE_IN_D3):** An override to ignore RMMI Config Clock request in D3. When this is enabled the MPHY request will not block CG of SOSC trunk. 0: No override 1: Ignore RMMI Config Clock request in D3
20	0h RO	Reserved.
19	0h RW	**USB3 Partition Engine/Link trunk gating Enable (PARUSB3_ENG_GEN):** When set to 1 enables gating of the SOSC trunk to the XHCI engine and link in the PARUSB3 partition.
18	0h RW	**USB3 Partition Frame Timer trunk gating Enable (PARUSB3_LINK_GEN):** When set to 1 enables gating of the SOSC trunk to the Frame timer in the PARUSB3 partition.
17	0h RW	**USB2 link partition clock gating enable (PARUSB2_CLK_GEN):** When set to 1 enables gating of the SOSC trunk to the USB2 link and Phy logic in the PARUSB2 partition.
16	0h RW	**USB2/USHIP 12.5 MHz partition clock gating enable (USHIP_PCGEN):** When set to 1 enables gating of the 12.5 MHz SOSC trunk to the USB2 and USHIP logic in the PARUSB2 partition.
15	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RW	**USB3 Port Aux/Core clock gating enable (USB3_AC_CGE):** When set, allows the aux_cclk clock into the USB3 port to be gated when conditions are met. Usage of this bit is further qualified with xHC Dynamic Clock Gating Disable fuse. If the fuse disables dynamic clock gating, Aux clock gating will not be enabled either. This bit always returns the value that was written to it irrespective of the setting of xHC Dynamic Clock Gating Disable fuse.
13:12	0h RW	**Rx Detect Timer when port Aux Clock is Gated (RX_DT_ACG):** This field defines the value of the timer used to perform Rx Detect when port Aux Clock has been gated. 0x0: 100ms 0x1: 12ms Others: Reserved Note: This timer shall use the Fast Training Timer Tick (about 1us tick) for simulation purposes. For Fast Training mode, the above timeouts will become about 11us and about 100us, +/- implementation uncertainty, respectively.
11:8	4h RW	**U2 Residency Before ModPHY Clock Gating (U2R_BM_CG):** Before gating ModPHY Aux clock, Host Controller shall wait for this time in U2. This time is meant to ensure that the attached device has entered U2 as well. 0x0: 1us 0x1: 128us 0x2: 256us 0x3: 512us 0x4: 640us 0x5: 768us 0x6: 896us 0x7: 1024us Others: Reserved Note: This counter shall start counting once pipe has entered PS3 state in response to link in U2.
7	0h RW	**Frame Timer Clock Gating Ports in U2 Enable (FTCGPU2E):** This bit, when set, allows Host Controller to gate the clock to the Frame Timer when ports are in U2.
6	0h RW	**USB2 port clock throttle enable (USB2_PC_TE):** When set, allows the Aux clock into the USB2 ports to be throttled when conditions allow.
5	0h RW	**XHCI Engine Aux clock gating enable (XHCI_AC_GE):** When set, allows the aux clock into the XHCI engine to be gated when idle.Usage of this bit is further qualified with xHC Dynamic Clock Gating Disable fuse. If the fuse disables dynamic clock gating, Aux clock gating will not be enabled either.This bit always returns the value that was written to it irrespective of the setting of xHC Dynamic Clock Gating Disable fuse.
4	0h RW	**XHCI Aux PM block clock gating enable (XHCI_APMB_CGE):** When set, allows the aux clock into the Aux PM block to be gated when idle. Usage of this bit is further qualified with xHC Dynamic Clock Gating Disable fuse. If the fuse disables dynamic clock gating, Aux clock gating will not be enabled either. This bit always returns the value that was written to it irrespective of the setting of xHC Dynamic Clock Gating Disable fuse.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**USB3 Aux Clock Trunk Gating Enable (USB3_AC_TGE):** When set, allows Aux Clock Trunk feeding to USB3.0 ports to be gated when port Aux clock is gated at all USB3.0 ports and all USB3.0 modPHY instances. Usage of this bit is further qualified with xHC Dynamic Clock Gating Disable fuse. If the fuse disables dynamic clock gating, Aux clock gating will not be enabled either. This bit always returns the value that was written to it irrespective of the setting of xHC Dynamic Clock Gating Disable fuse.
2	0h RO	Reserved.
1	0h RW	**ModPHY port Aux clock gating enable in U2 (MPP_AC_GEU2):** When set, allows the aux clock into the ModPhy to be gated when Link is in U2 and pipe has been in PS3 for at least the time defined by U2 Residency Before ModPHY Clock Gating field. Usage of this bit is further qualified with xHC Dynamic Clock Gating Disable fuse. If the fuse disables dynamic clock gating, Aux clock gating will not be enabled either. This bit always returns the value that was written to it irrespective of the setting of xHC Dynamic Clock Gating Disable fuse.
0	0h RW	**ModPHY port Aux clock gating enable in Disconnected, U3 or Disabled (MPP_AC_GE_DDU3):** When set, allows the aux clock into the ModPHY to be gated when Link is in Disconnected, U3 or Disabled state. Usage of this bit is further qualified with xHC Dynamic Clock Gating Disable fuse. If the fuse disables dynamic clock gating, Aux clock gating will not be enabled either. This bit always returns the value that was written to it irrespective of the setting of xHC Dynamic Clock Gating Disable fuse.

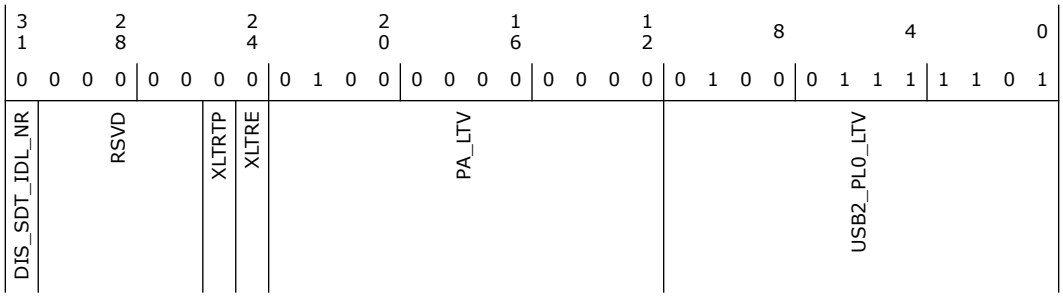
21.2.63 xHC Latency Tolerance Parameters - LTV Control (XLTP_LTV1)—Offset 8174h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 20
Function: 0

Default: 40047Dh



Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Disable scheduler direct transition from IDLE to NO requirement (DIS_SDT_IDL_NR):** 0: (default) allow scheduler direct transition from IDLE to NO requirement 1: Disable scheduler direct transition from IDLE to NO requirement
30:26	0h RO	Reserved.
25	0h RW	**XHCI LTR Transition Policy (XLTRTP):** When '0', LTR messaging state machine transitions from High, Medium, or Low LTR states to Active state upon the Alarm Timer timout and stays in Active until the next service boundary.When '1', the LTR messaging state machine transitions through High - Med - Low - Active states assuming enough latency is available for each transition.
24	0h RW	**XHCI LTR Enable (XLTRE):** This bit must be set to enable LTV messaging from XHCI to the PMC.
23:12	400h RW	**Periodic Active LTV (PA_LTV):** 23:22 Latency Scale 00b : Reserved 01b : Latency Value to be multiplied by 1024 10b : Latency Value to be multiplied by 32,768 11b : Latency Value to be multiplied by 1,048,576 21:12 Latency Value (ns) Defaults to 0 micro seconds
11:0	47Dh RW	**USB2 Port L0 LTV (USB2_PL0_LTV):** 11:10 Latency Scale 00b : Reserved 01b : Latency Value to be multiplied by 1024 10b : Latency Value to be multiplied by 32,768 11b : Latency Value to be multiplied by 1,048,576 9:0 Latency Value (ns) Defaults to 128 Micro Seconds

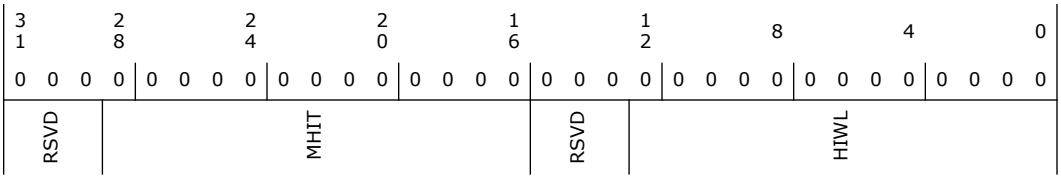
21.2.64 xHC Latency Tolerance Parameters - High Idle Time Control (XLTP_HITC)—Offset 817Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 20
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	Reserved.
28:16	0h RW	**Minimum High Idle Time (MHIT):** LTR value can be indicated. This value must be larger than HIWL 12:7 - Time value in # of 125 Micro Seconds Bus Intervals (0 - 8ms) 6:0 - Fractional BI Time value in Micro Seconds (0 - 124 Micro Seconds)
15:13	0h RO	Reserved.
12:0	0h RW	**High Idle Wake Latency (HIWL):** This is the latency to access memory from the High Idle Latency state. This value must be larger than MIWL and LIWL 12:7 - Time value in # of 125 Micro Seconds Bus Intervals (0 - 8ms) 6:0 - Fractional BI Time value in Micro Seconds (0 - 124 Micro Seconds)

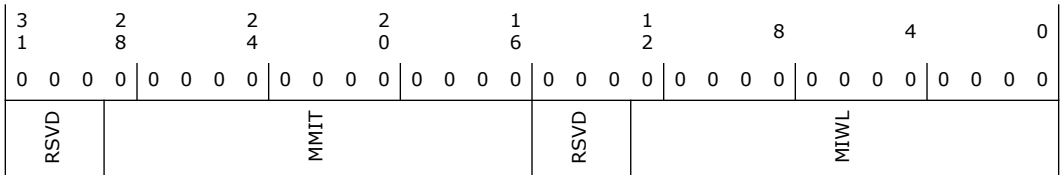
21.2.65 xHC Latency Tolerance Parameters - Medium Idle Time Control (XLTP_MITC)—Offset 8180h

Access Method

Type: MEM Register (Size: 32 bits)

Device: 20
Function: 0

Default: 0h



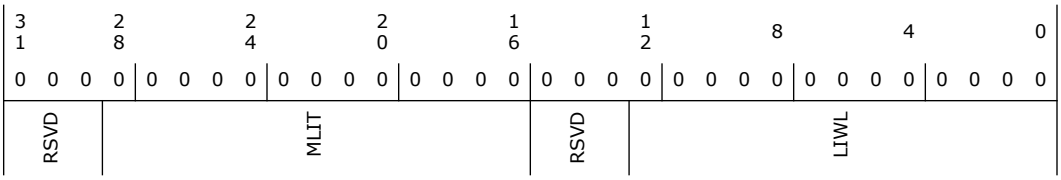
Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	Reserved.
28:16	0h RW	**Minimum Medium Idle Time (MMIT):** LTR value can be indicated. This value must be larger than MIWL 12:7 - Time value in # of 125 Micro Seconds Bus Intervals (0 - 8ms) 6:0 - Fractional BI Time value in Micro Seconds (0 - 124 Micro Seconds)
15:13	0h RO	Reserved.
12:0	0h RW	**Medium Idle Wake Latency (MIWL):** This is the latency to access memory from the Medium Idle Latency state. This value must be larger than LIWL 12:7 - Time value in # of 125 Micro Seconds Bus Intervals (0 - 8ms) 6:0 - Fractional BI Time value in Micro Seconds (0 - 124 Micro Seconds)

21.2.66 xHC Latency Tolerance Parameters Low Idle Time Control (XLTP_LITC)—Offset 8184h

Access Method

Type: MEM Register (Size: 32 bits)
Device: 20
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	Reserved.
28:16	0h RW	**Minimum Low Idle Time (MLIT):** LTR value can be indicated. This value must be larger than LIWL 12:7 - Time value in # of 125 Micro Seconds Bus Intervals (0 - 8ms) 6:0 - Fractional BI Time value in Micro Seconds (0 - 124 Micro Seconds)
15:13	0h RO	Reserved.
12:0	0h RW	**Low Idle Wake Latency (LIWL):** This is the latency to access memory from the Medium Idle Latency state. 12:7 - Time value in # of 125 Micro Seconds Bus Intervals (0 - 8ms) 6:0 - Fractional BI Time value in Micro Seconds (0 - 124 Micro Seconds)

21.2.67 Command Manager Control 2 (XECP_CMDM_CTRL_REG2)—Offset 8190h

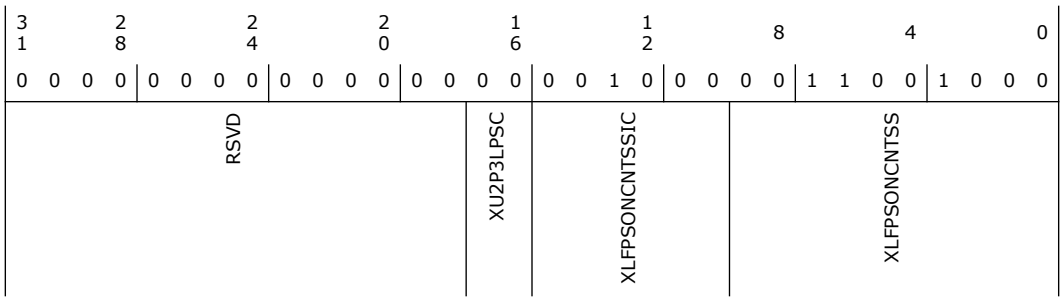
BIOS may program this register.

21.2.68 LFPSONCOUNT_REG (LFPSONCOUNT_REG)—Offset 81B8h

Access Method

Type: MEM Register (Size: 32 bits)
Device: 20
Function: 0

Default: 20C8h



Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17:16	0h RW	**U2P3 LFPS Periodic Sampling Control (XU2P3LPSC):** This field controls the OFF time for the LFPS periodic sampling for SS and SSIC ports in U2P3. If LFPSPM for a port is 1, it will override the OFF time and LFPS receiver will remain OFF permanently. For Fast Sim mode, 500us will be equivalent to 5us. 0x0 Polling Disable. (RXDET Polling will become 100ms.) 0x1 500us OFF Time 0x2 1ms OFF Time 0x3 1.5ms OFF Time
15:10	8h RW	**XLFPSONCNTSSIC (XLFPSONCNTSSIC):** This time would describe the number of clocks SSIC LFPS will remain ON. SSIC LFPS detection operation may be carried out on using RTC clock or Oscillator clock. The value of this register should be adjusted accordingly. For RTC recommended value is 2. For Oscillator clock, recommended value is 8.
9:0	C8h RW	**XLFPSONCNTSS (XLFPSONCNTSS):** This time would describe the number of clocks LFPS will remain ON. LFPS detection operation may be carried out on using RTC clock or Oscillator clock. The value of this register should be adjusted accordingly. For RTC recommended value is 2. For Oscillator clock, recommended value is 200.

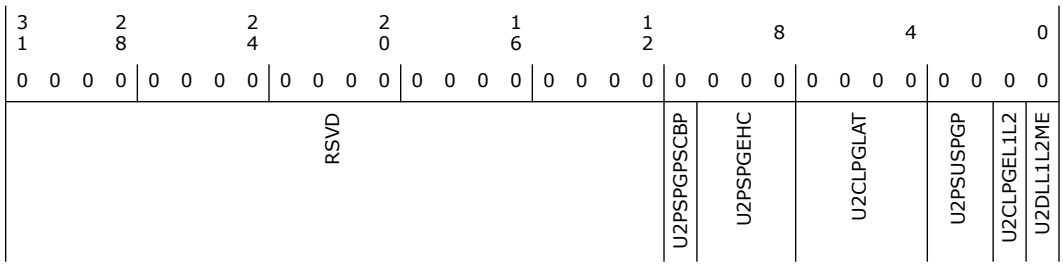
21.2.69 USB2 PM Control (USB2PMCTRL_REG)—Offset 81C4h

Access Method

Type: MEM Register (Size: 32 bits)

Device: 20
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	Reserved.
11	0h RW	**USB2 PHY SUS Power Gate PORTSC Block Policy (U2PSPGPSCBP):** This controls the policy for blocking PORTSC Updates while the USB2 PHY SUS Well is power gated. When set, the controller will block any updates to the PORTSC caused by port status change if the USB2 PHY SUS is power gated.
10:8	0h RW	**USB2 PHY SUS Well Power Gate Entry Hysteresis Count (U2PSPGEHC):** This controls the amount of hysteresis time the controller will enforce after detecting the USB2 PHY SUS Power Gate entry condition. 0h 0 clocks 1h 32 clocks 2h 64 clocks 3h 128 clocks 4h 256 clocks 5h 512 clocks 6h 1024 clocks 7h 2048 clocks
7:4	0h RW	**USB2 PHY SUS Power Gate PORTSC Block Policy (U2CLPGLAT):** This field represents the worst case latency for the USB2 Common Lane to enter and exit its power gate state. This fields is required to be compared to a ports HIRD/HIRD value for the ports that have allowed L1 to L2 mapping to determine if the Common Lane can be allowed to power off. If the power gate entry/exit latency is greater than the HIRD/HIRDD then the common lane should not be allowed to power gate as this will result in a L1 exit violation. 0h 100 us 1h 200 us 2h 300 us Eh 1500us Fh 1600 us

Bit Range	Default & Access	Field Name (ID): Description
3:2	0h RW	**USB2 PHY SUS Well Power Gate Policy (U2PSUSPGP):** This field controls when to enable the USB2 PHY SUS Well Power Gating when the proper conditions are met.00 USB2 PHY SUS Power Gating is Disabled.01 USB2 PHY SUS Power Gating is Enabled in Only D0 and D0i2 (Excludes D0i3 and D3)10 USB2 PHY SUS Power Gating is Eanabled in only in D0, D0i2 and D0i3 (Excludes D3)11 USB2 PHY SUS Power Gating is Eanabled in D0/ D0i2/D0i3/D3
1	0h RW	**USB2 Common Lane Power Gating Enable During L1 to L2 Mapping for USB2 PHY Power Gating (U2CLPGEL1L2):** This field when set enables the controller to allow for the common lane power gating to be enabled when all ports are exposed as in L2 to the USB2 PHY while at least 1 port has been mapped to L2 from L1. This field alone does not guarantee power gating since the L1 HIRD/HIRDD Value must be compared with the PHYs power gate exit latency (U2CLPGLAT) held in this register to ensure that L1 exit is not violated. 0 USB2 Common Lane Power Gating is disabled when any port has been mapped from L1 to L2. 1 USB2 Common Lane Power Gating is allowed when any port has been mapped to L2 from L1 with the additional condition that the HIRD/ HIRDD is greater than the PHYs Power Gate exit latency.
0	0h RW	**USB2 Data Lane L1 to L2 Mapping Enable for USB2 PHY Power Gating (U2DLL1L2ME):** This field when set enables the controller to map an L1 entry directly to L2 to allow the USB2 PHY to trigger its Autonomous Power Gating. The USB2 PHY will trigger PG only when in L2 since it does not fully understand the requirements for L1. 0 USB2 L1 to L2 mapping is disabled for all ports 1 USB2 L1 to L2 mapping is enabled for all ports

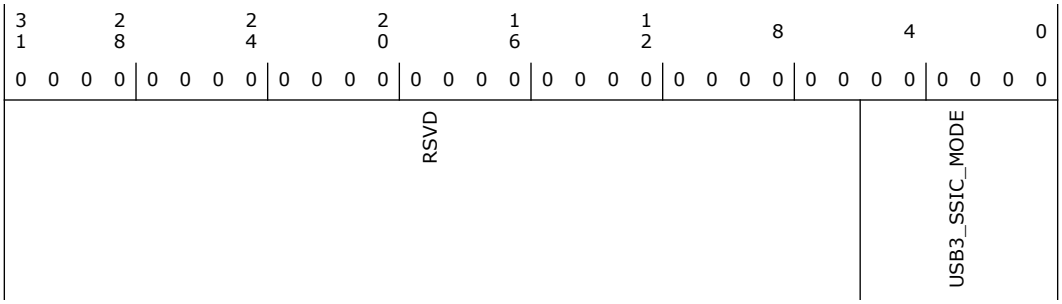
21.2.70 STRAP2_REG (STRAP2_REG)—Offset 8420h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 20
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	Reserved.
5:0	0h RO	**USB3_SSIC_MODE (USB3_SSIC_MODE):** Each bit corresponds to the appropriately numbered USB3 port (zero based) Bit 0 = port 1, Bit 1 = port 2. 0: Port is operated in USB3 mode. 1: Port is operated in SSIC mode.

21.2.71 USB Legacy Support Capability (USBLEGSUP)—Offset 846Ch

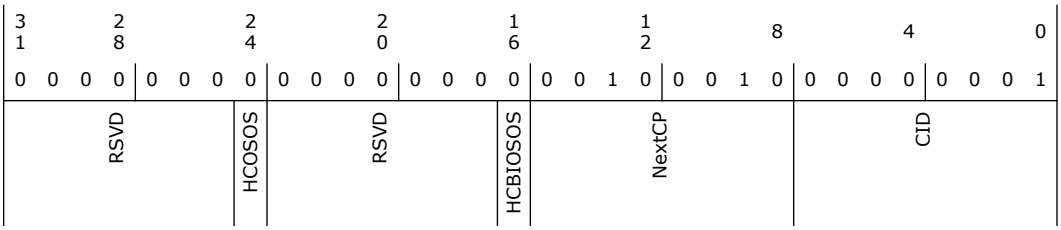
This register is modified and maintained by BIOS

Access Method

Type: MEM Register (Size: 32 bits)

Device: 20
Function: 0

Default: 2201h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	Reserved.
24	0h RW	**HC OS Owned Semaphore (HCOSOS):** Default = '0'. System software sets this bit to request ownership of the xHC. Ownership is obtained when this bit reads as '1' and the HC BIOS Owned Semaphore bit reads as '0'.
23:17	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**HC BIOS Owned Semaphore (HCBIOSOS):** Default = '0'. The BIOS sets this bit to establish ownership of the xHC. System BIOS will set this bit to a '0' in response to a request for ownership of the xHC by system software.
15:8	22h RW/S	**Next Capability Pointer (NextCP):** This field indicates the location of the next capability with respect to the effective address of this capability. Refer to Table 145 for more information on this field.
7:0	1h RW/L	**Capability ID (CID):** This field identifies the extended capability. Refer to Table 146 for the value that identifies the capability as Legacy Support. This extended capability requires one additional 32-bit register for control/status information (USBLEGCTLSTS), and this register is located at offset xECP+04h.

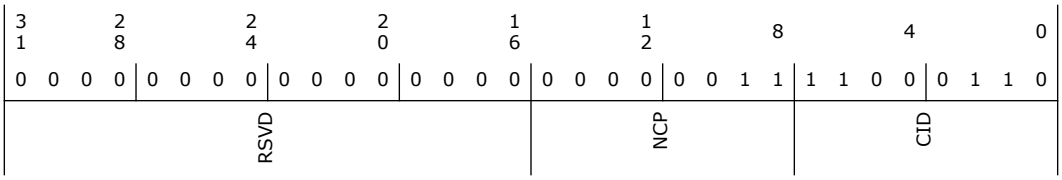
21.2.72 Port Disable Override capability register (PDO_CAPABILITY)—Offset 84F4h

Access Method

Type: MEM Register (Size: 32 bits)

Device: 20
Function: 0

Default: 3C6h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:8	3h RO	**Next Capability Pointer (NCP)**
7:0	C6h RO	**Capability ID (CID)**

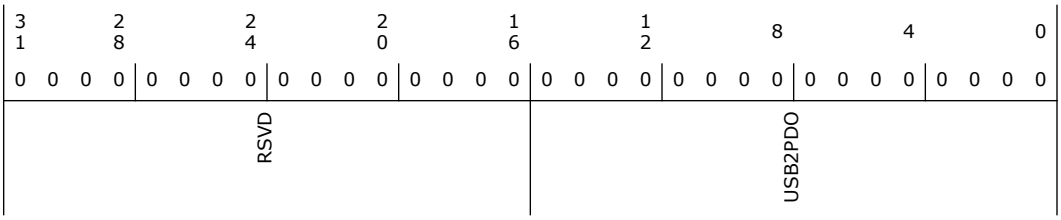
21.2.73 USB2 Port Disable Override (USB2PDO)—Offset 84F8h

Access Method

Type: MEM Register (Size: 32 bits)

Device: 20
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	0h RW/O	**USB2PDO (USB2PDO):** A '1' in a bit position prevents the corresponding USB2 port from reporting a Device Connection to the XHC. This applies across all USB2 protocol ports 0 = Allows corresponding USB port to report a device connection to the xHC. 1 = Prevents the corresponding USB port from reporting a device Connection to the xHC. Port to bit mapping is in one-hot encoding, that is bit 0 controls port 1 and so on. Bit 0 = USB 2.0 port 1 ... Bit N-1 = USB 2.0 port N

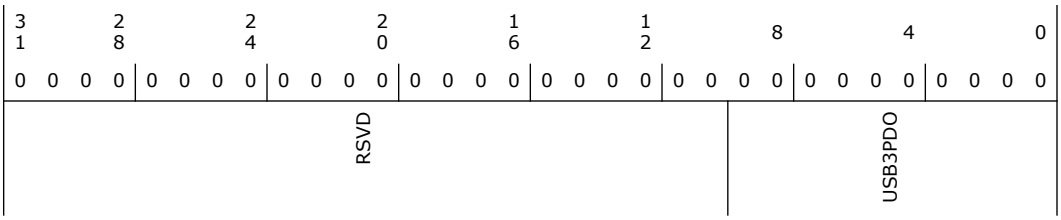
21.2.74 USB3 Port Disable Override (USB3PDO)—Offset 84FCh

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 20
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:0	0h RW/O	**USB3 Port Disable Override (USB3PDO):** 0 = Allows corresponding USB port to report a Device Connection to the xHC. 1 = Prevents the corresponding USB port from reporting a Device Connection to the xHC. Bit 0 = USB 3.0 Port 1 ... Bit N-1 = USB 3.0 Port N

21.2.75 Debug Capability ID Register (DCID)—Offset 8700h

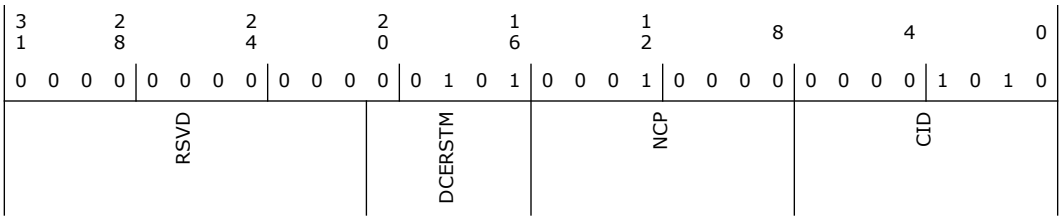
This register is modified and maintained by BIOS

Access Method

Type: MEM Register (Size: 32 bits)

Device: 20
Function: 0

Default: 5100Ah



Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	Reserved.
20:16	5h RW	**Debug Capability Event Ring Segment Table Max (DCERSTM):** Note: This register is sticky.
15:8	10h RW	**Next Capability Pointer (NCP):** Note: This register is sticky.
7:0	Ah RW	**Capability ID (CID):** Note: This register is sticky.

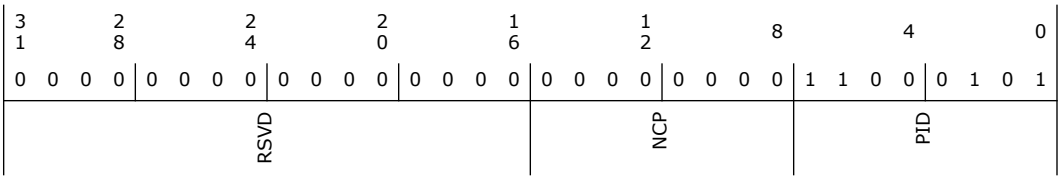
21.2.76 SSIC Local and Remote Profile Registers Capability ID register (SSIC_PROFILE_CAPABILITY_ID_REG)—Offset 8900h

Access Method

Type: MEM Register (Size: 32 bits)

Device: 20
Function: 0

Default: C5h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:8	0h RO	**Next Capability Pointer (NCP)**
7:0	C5h RO	**Supported Protocol ID (PID)**

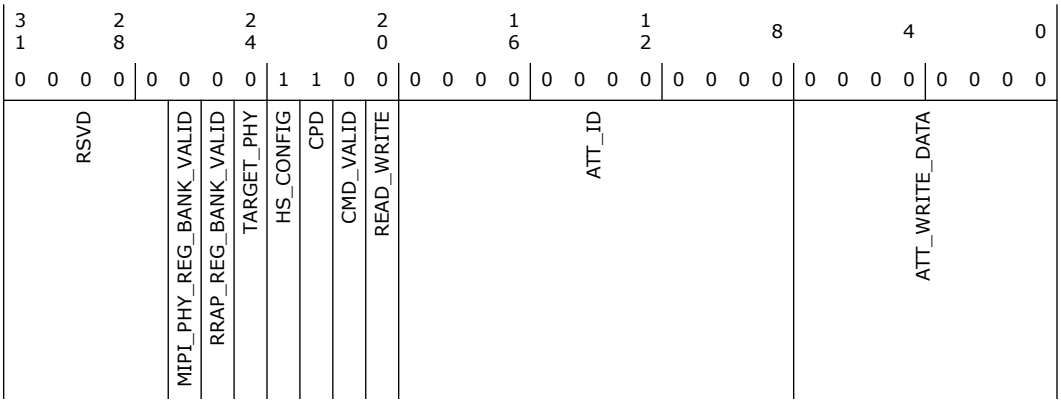
21.2.77 SSIC Port N Register Access Control (PORT1_REGISTER_ACCESS_CONTROL)—Offset 8904h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 20
Function: 0

Default: C00000h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	Reserved.
26	0h RW	**MIPI PHY Register Bank Valid (MIPI_PHY_REG_BANK_VALID):** 0 = No valid Commands in the Lane N register bank for Local PHY. Host Controller can proceed to HSBURST once commands from this register are completed. 1 = Valid commands present in the Lane N register bank. Host controller must complete commands from the register bank before proceeding to HSBURST.
25	0h RW	**RRAP Register Bank Valid (RRAP_REG_BANK_VALID):** 0 = No valid Commands in the Lane N register bank. Host Controller can close the PWM burst once commands from this register are completed. 1 = Valid commands present in the Lane N register bank. Host controller must complete commands from the register bank before closing the burst.
24	0h RW	**Target Phy (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy Setting this bit to 1 allows the use of this command mechanism to write to local Phy profile and AFE tuning registers Primarily as a back up option.
23	1h RW	**HS_Config (HS_CONFIG):** When this bit is set to 1 the host controller will issue an RRAP write with HS_Config=1 once it sees Command Phase Done = 1
22	1h RW	**Command Phase Done (CPD):** When set to 1, this indicates that SW has completed performing RRAP cycles through the command register.
21	0h RW	**Command Valid (CMD_VALID):** When written to 1 indicates that the Attribute ID and Attribute Data for writes fields are valid.
20	0h RW	**Read_Write (READ_WRITE):** 0 = Write 1= Read
19:8	0h RW	**Attribute ID (ATT_ID):** Attribute ID that is being written or read
7:0	0h RW	**Attribute Write Data (ATT_WRITE_DATA):** Data byte that is required to be written to either the local phy or the remote phy

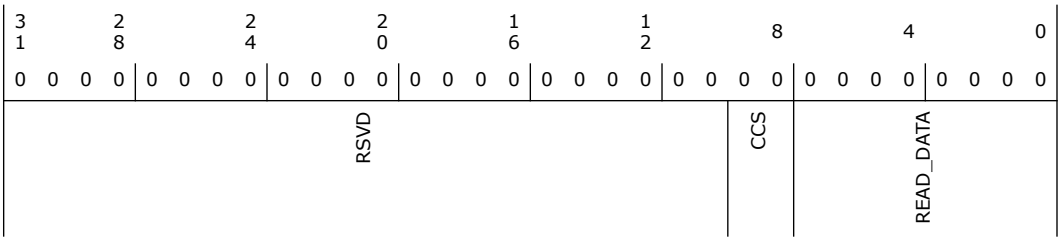
21.2.78 SSIC Port N Register Access Status (PORT1_REGISTER_ACCESS_STATUS)—Offset 8908h

Access Method

Type: MEM Register (Size: 32 bits)

Device: 20
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:8	0h RW	**Command Completion Status (CCS):** 00 = Command not complete 01 = Command complete with Success 10 = Command complete with Error These bits must be cleared before a new command is initiated.
7:0	0h RO	**Read data (READ_DATA):** Data read as a result of the RRAP operation

21.2.79 (PORT1_PROFILE_ATTRIBUTES_REG0)—Offset 890Ch

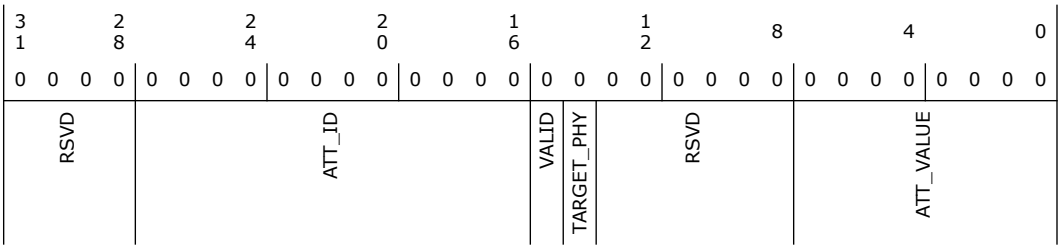
Address Offsets: 0Ch - 0Fh, upto 108h - 10Bh
64 Dwords per Port

This bank of registers provides 64 Dwords per port to be used to store attributes that need to be written into the local and remote phy every time the link enters the PWM state.

Access Method

Type: MEM Register (Size: 32 bits)
Device: 20
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	Reserved.
27:16	0h RW	**Attribute ID (ATT_ID):** {Upper Address [3:0], Lower Address [7:0]}
15	0h RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16
14	0h RW	**TARGET_PHY (TARGET_PHY):** 0 = RemotePhy 1 = Local Phy
13:8	0h RO	Reserved.
7:0	0h RW	**ATTRIBUTE VALUE (ATT_VALUE)**

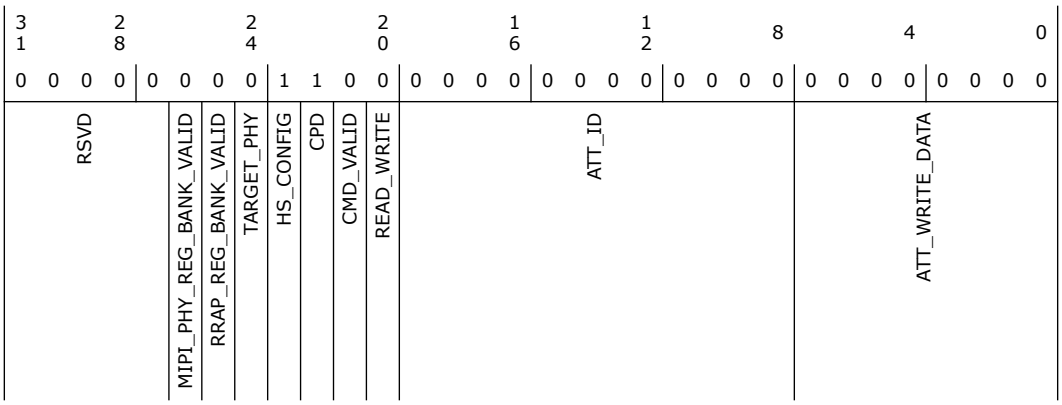
21.2.80 SSIC Port N Register Access Control (PORT2_REGISTER_ACCESS_CONTROL)—Offset 8A14h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 20
Function: 0

Default: C00000h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	Reserved.
26	0h RW	**MIPI PHY Register Bank Valid (MIPI_PHY_REG_BANK_VALID):** 0 = No valid Commands in the Lane N register bank for Local PHY. Host Controller can proceed to HSBURST once commands from this register are completed. 1 = Valid commands present in the Lane N register bank. Host controller must complete commands from the register bank before proceeding to HSBURST.
25	0h RW	**RRAP Register Bank Valid (RRAP_REG_BANK_VALID):** 0 = No valid Commands in the Lane N register bank. Host Controller can close the PWM burst once commands from this register are completed. 1 = Valid commands present in the Lane N register bank. Host controller must complete commands from the register bank before closing the burst.
24	0h RW	**Target Phy (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy Setting this bit to 1 allows the use of this command mechanism to write to local Phy profile and AFE tuning registers Primarily as a back up option.
23	1h RW	**HS_Config (HS_CONFIG):** When this bit is set to 1 the host controller will issue an RRAP write with HS_Config=1 once it sees Command Phase Done = 1
22	1h RW	**Command Phase Done (CPD):** When set to 1, this indicates that SW has completed performing RRAP cycles through the command register.
21	0h RW	**Command Valid (CMD_VALID):** When written to 1 indicates that the Attribute ID and Attribute Data for writes fields are valid.
20	0h RW	**Read_Write (READ_WRITE):** 0 = Write 1= Read
19:8	0h RW	**Attribute ID (ATT_ID):** Attribute ID that is being written or read
7:0	0h RW	**Attribute Write Data (ATT_WRITE_DATA):** Data byte that is required to be written to either the local phy or the remote phy

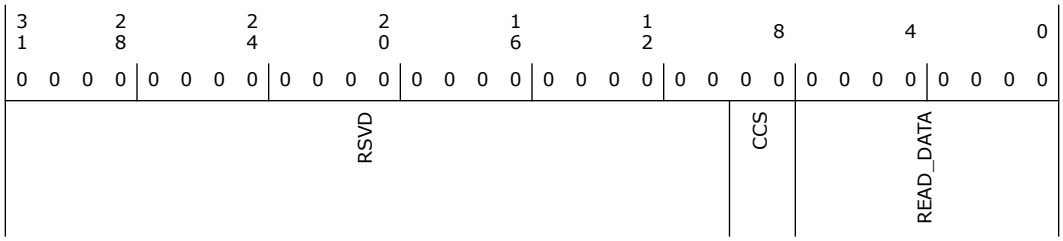
21.2.81 SSIC Port N Register Access Status (PORT2_REGISTER_ACCESS_STATUS)—Offset 8A18h

Access Method

Type: MEM Register (Size: 32 bits)

Device: 20
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:8	0h RW	**Command Completion Status (CCS):** 00 = Command not complete 01 = Command complete with Success 10 = Command complete with Error These bits must be cleared before a new command is initiated.
7:0	0h RO	**Read data (READ_DATA):** Data read as a result of the RRAP operation

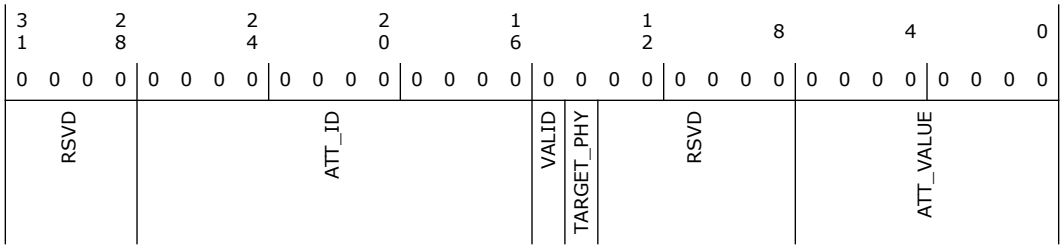
21.2.82 (PORT2_PROFILE_ATTRIBUTES_REG0)—Offset 8A1Ch

Address offset: 11Ch - 11Fh up to 218h - 21Bh
Port 2: 11Ch, 120h, … , 218h
This bank of registers provides 64 Dwords per port to be used to store attributes that need to be written into the local and remote phy every time the link enters the PWM state.

Access Method

Type: MEM Register (Size: 32 bits)
Device: 20
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	Reserved.
27:16	0h RW	**Attribute ID (ATT_ID)**
15	0h RW	**Valid (VALID):** When set, indicates that the attribute value in bits 7:0 must be written to the address specified in bits 27:16
14	0h RW	**TARGET_PHY (TARGET_PHY):** 0 = Remote Phy 1 = Local Phy
13:8	0h RO	Reserved.
7:0	0h RW	**ATTRIBUTE VALUE (ATT_VALUE)**

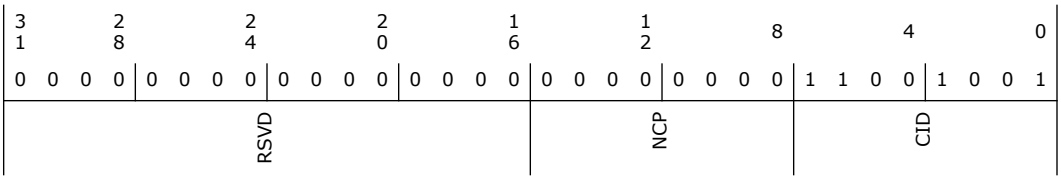
21.2.83 Global Time Sync Capability (GLOBAL_TIME_SYNC_CAP_REG)—Offset 8E10h

Access Method

Type: MEM Register (Size: 32 bits)

Device: 20
Function: 0

Default: C9h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:8	0h RO	**Next Capability pointer (NCP)**
7:0	C9h RO	**Capability ID (CID)**

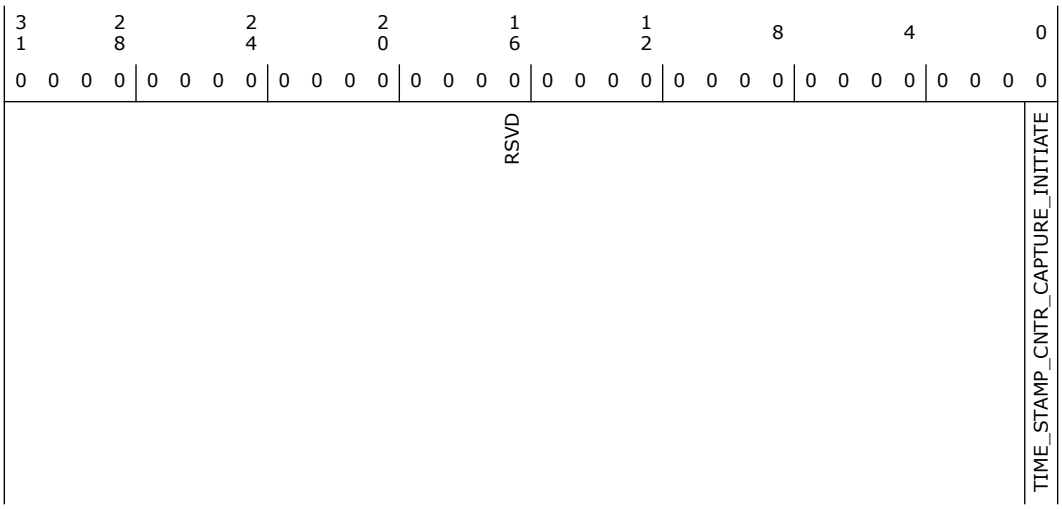
21.2.84 Global Time Sync Control (GLOBAL_TIME_SYNC_CTRL_REG)—Offset 8E14h

Access Method

Type: MEM Register (Size: 32 bits)

Device: 20
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RW/1S	**Always Running Time (ART) Capture Initiate (TIME_STAMP_CNTR_CAPTURE_INITIATE):** SW sets this bit to initiate a time capture. Once the time capture is complete and the time values are valid in the Local and Global time capture registers, HW clears the bit.

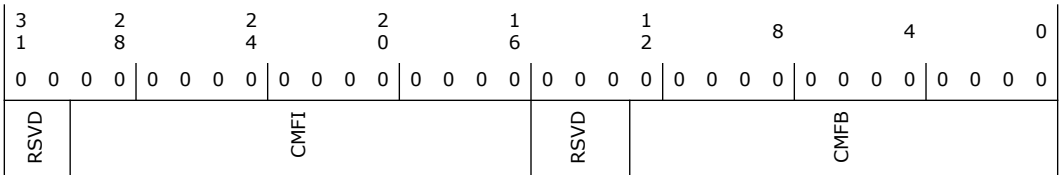
21.2.85 Microframe Time (Local Time) (MICROFRAME_TIME_REG)—Offset 8E18h

Access Method

Type: MEM Register (Size: 32 bits)

Device: 20
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29:16	0h RO	**Captured Frame List Current Index/Frame Number (CMFI):** The value in this register is updated in response to sample_now signal. Bits [29:16] reflect state of bits [13:0] of FRINDEX
15:13	0h RO	Reserved.
12:0	0h RO	**Captured Micro-frame BLIF (CMFB):** The value is updated in response to sample_now signal and provides information about offset within micro-frame. Captured value represents number of 8 high-speed bit time units from start of micro-frame. At the beginning of micro-frame captured value will be 0 and increase to maximum value at the end. Default maximum value is 7499 but it may be changed as result of adjustment done via Bus Interval Adjust (BIA).

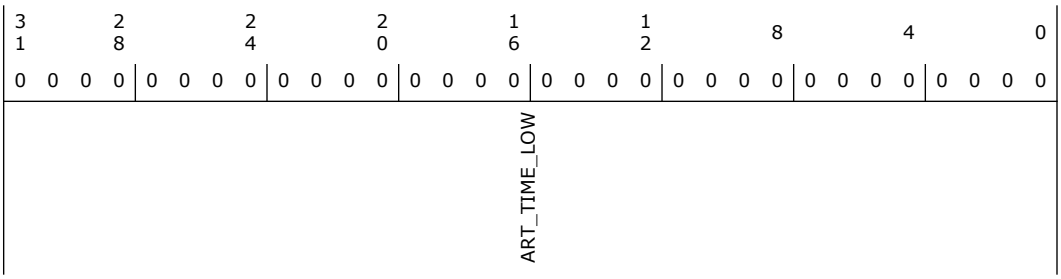
21.2.86 Always Running Time (ART) Low (ALWAYS_RUNNING_TIME_LOW)—Offset 8E20h

Access Method

Type: MEM Register (Size: 32 bits)

Device: 20
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**ART Value (Low) (ART_TIME_LOW):** Lower Dword of the ART value captured based on the time sync initiated by SW.

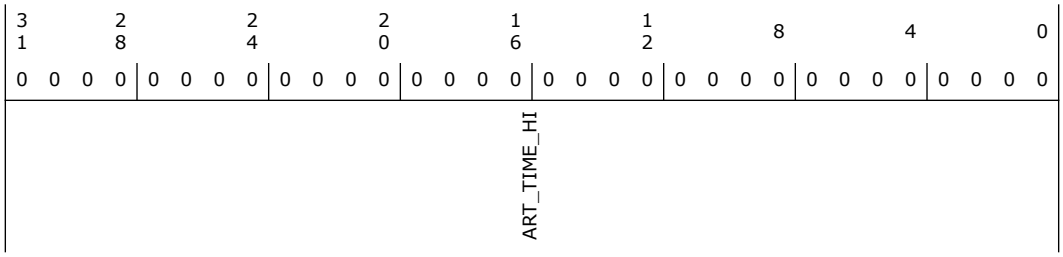
21.2.87 Always Running Time (ART) High (ALWAYS_RUNNING_TIME_HIGH)—Offset 8E24h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 20
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**ART Value (High) (ART_TIME_HI):** Upper Dword of the ART value captured based on the time sync initiated by SW.

§ §

22 USB Dual Role/OTG Device Controller (xDCI) (D20:F1)

22.1 USB Device Controller (xDCI) Configuration Registers Summary

Table 22-1. Summary of USB Device Controller (xDCI) Configuration Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	(DEVVENDID)—Offset 0h	22B78086h
4h	7h	(STATUSCOMMAND)—Offset 4h	100000h
8h	Bh	(REVCLASSCODE)—Offset 8h	C03FEXXh
Ch	Fh	(CLLATHEADERBIST)—Offset Ch	0h
10h	13h	(BAR)—Offset 10h	0h
14h	17h	(BAR_HIGH)—Offset 14h	0h
18h	1Fh	(BAR1)—Offset 18h	4h
2Ch	2Fh	(SUBSYSTEMID)—Offset 2Ch	0h
30h	33h	(EXPANSION_ROM_BASEADDR)—Offset 30h	0h
34h	37h	(CAPABILITYPTR)—Offset 34h	80h
3Ch	3Fh	(INTERRUPTREG)—Offset 3Ch	100h
80h	83h	(POWERCAPID)—Offset 80h	48039001h
84h	87h	(PMECTRLSTATUS)—Offset 84h	8h
90h	93h	(PCIDEVIDLE_CAP_RECORD)—Offset 90h	F0140009h
94h	97h	(DEVID_VEND_SPECIFIC_REG)—Offset 94h	1400010h
98h	9Bh	(D0I3_CONTROL_SW_LTR_MMIO_REG)—Offset 98h	0h
9Ch	9Fh	(DEVICE_IDLE_POINTER_REG)—Offset 9Ch	FF100001h
A0h	A3h	(D0I3_MAX_POW_LAT_PG_CONFIG)—Offset A0h	80800h
B0h	B3h	(GEN_REGRW1)—Offset B0h	0h
B4h	B7h	(GEN_REGRW2)—Offset B4h	0h
B8h	BBh	(GEN_REGRW3)—Offset B8h	0h
BCh	BFh	(GEN_REGRW4)—Offset BCh	0h
C0h	C3h	(GEN_INPUT_REGRW)—Offset C0h	1008000Bh

22.1.1 (DEVVENDID)—Offset 0h

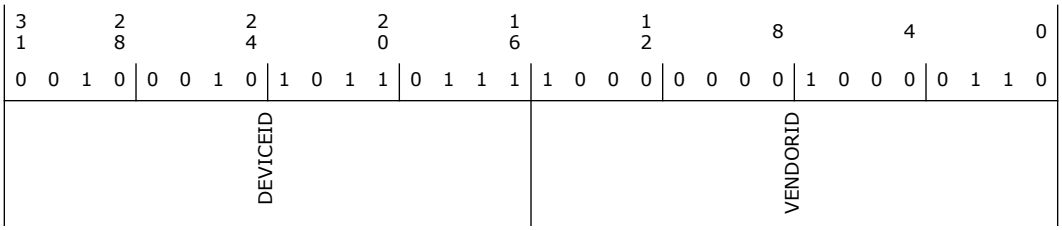
DEVICEVENDORID - Device ID and Vendor ID Register

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 1

Default: 22B78086h



Bit Range	Default & Access	Field Name (ID): Description
31:16	22B7h RO	**DEVICEID:** Device ID identifies the particular PCI device.
15:0	8086h RO	**VENDORID:** Vendor ID is a unique ID which identifies the manufacturer of the device. 8086h = Intel.

22.1.2 (STATUSCOMMAND)—Offset 4h

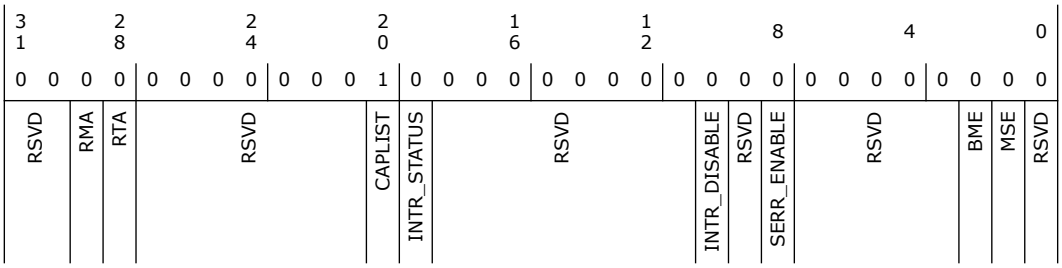
STATUSCOMMAND- Status and Command

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 1

Default: 100000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29	0h RW/1C	**RMA:** If the completion status received from IOSF is UR, the Bridge sets this bit. The software writes a 1 to this bit to clear it.
28	0h RW/1C	**RTA:** If the completion status received from IOSF is CA, the Bridge sets this bit. The software writes a 1 to this bit to clear it.
27:21	0h RO	Reserved.
20	1h RO	**CAPLIST:** Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at the configuration offset 34h.
19	0h RO	**INTR_STATUS:** This bit reflects state of interrupt in the device Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, is the device/function interrupt message sent. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. This bit reflects Legacy interrupt status.

Bit Range	Default & Access	Field Name (ID): Description
18:11	0h RO	Reserved.
10	0h RW	**INTR_DISABLE:** Interrupt Disable: Setting this bit disables INTx assertion from Bridge. The interrupt disabled is legacy INTx# interrupt, which is the Bridge does not send Interrupt Assert message through the IOSF Sideband Channel. Reset value of this bit is 0. This bit has no connection with the interrupt status bit.
9	0h RO	Reserved.
8	0h RW	**SERR_ENABLE:** SERR# Enable: Not implemented
7:3	0h RO	Reserved.
2	0h RW	**BME:** Bus Master Enable: If this bit is 0,the Bridge does not generate any new upstream transaction on IOSF as a master. Reset value of this bit is 0.
1	0h RW	**MSE:** Memory Space Enable: This bit controls Bridge response to downstream memory accesses. When set, accesses to memory space of the device is enabled. Reset value of this bit is 0.
0	0h RO	Reserved.

22.1.3 (REVCLASSCODE)—Offset 8h

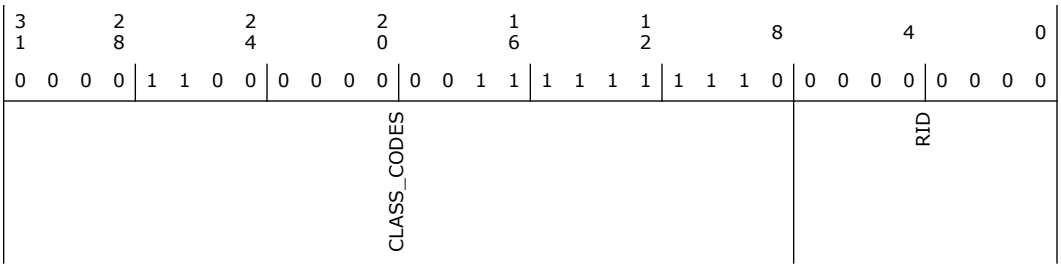
REVCLASSCODE - Revision ID and Class Code

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 1

Default: C03FExxh



Bit Range	Default & Access	Field Name (ID): Description
31:8	C03FEh RO	**CLASS_CODES:** The Class Code register is read-only and is used to identify the generic function of the device, and in some cases, a specific register-level programming interface.
7:0	-- RO	**RID:** Indicates stepping of the host controller. Refer to Device and Revision ID table in Vol1 for specific value.

22.1.4 (CLLATHEADERBIST)—Offset Ch

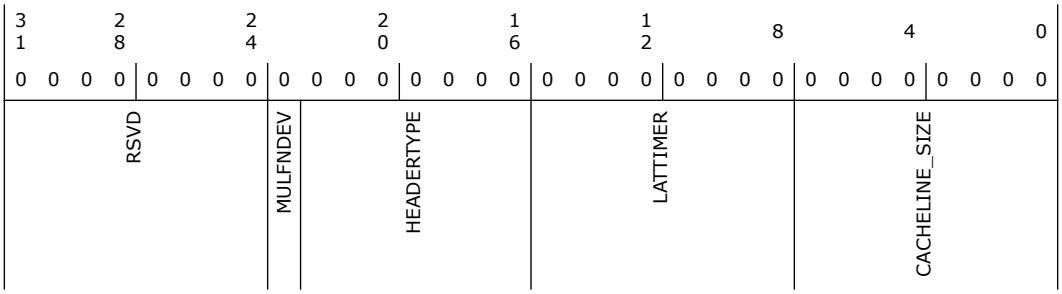
CLLATHEADERBIST - Cache Line Latency Header and BIST

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 1

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RO	**MULFNDEV:** This bit is 0 or 1 depending upon the value assigned o the top level strap
22:16	0h RO	**HEADERTYPE:** Implements Type 0 Configuration header.
15:8	0h RO	**LATTIMER:** This register is implemented as R/W with default as 0. Similar to other Intel IPs.
7:0	0h RW	**CACHELINE_SIZE:** This register is implemented as R/W with default as 0. Similar to other Intel IPs.

22.1.5 (BAR)—Offset 10h

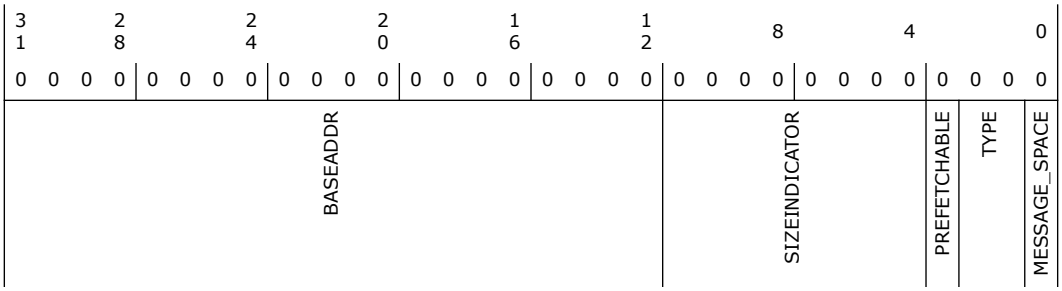
BAR -Base Address Register

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 1

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW	**BASEADDR:** Base address of the OCP fabric memory space. Taken from Strap values as ones. If a 64bit BAR is required then this entire register can be read only, depending upon the size requirement of the registers, such as in the unlikely scenario of the device size itself being greater than 4G.
11:4	0h RO	**SIZEINDICATOR:** Always returns 0. The size of this register depends on the size of the memory space. This size is determined by a top level of STRAP values as zeros.
3	0h RO	**PREFETCHABLE:** Indicates that this BAR is not prefetchable.
2:1	0h RO	**TYPE:** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**MESSAGE_SPACE:** 0 indicates this BAR is present in the memory space.

22.1.6 (BAR_HIGH)—Offset 14h

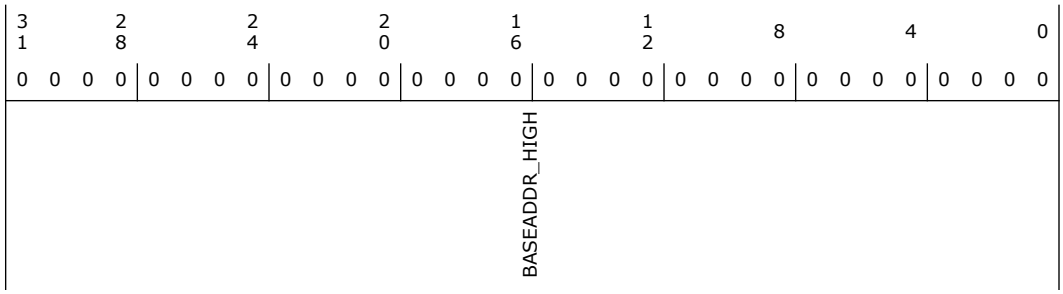
BAR -Base Address Register High

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 1

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**BASEADDR_HIGH:** Base address of the OCP fabric memory space. Taken from Strap values as ones

22.1.7 (BAR1)—Offset 18h

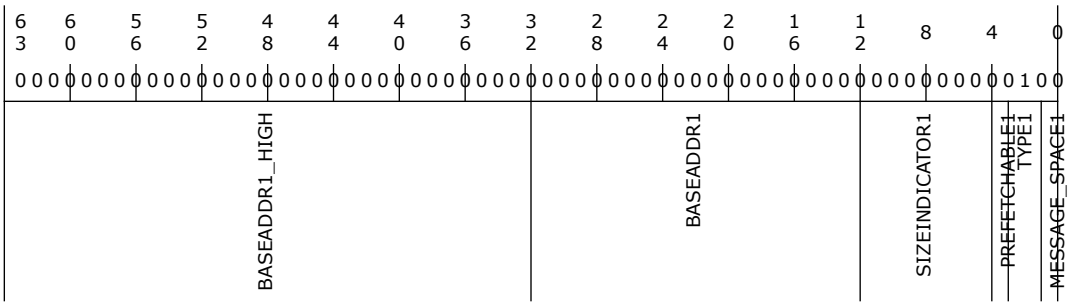
Memory accesses to BAR1 region are aliased to the PCI configuration space. The BAR1 region is always 4K. Software access through BAR1 can only access the regular PCI configuration space. BAR1 memory accesses, which do not access a defined PCI configuration register, are treated as access to reserved register. If this register is disabled then this is RO and always returns 0.

Access Method

Type: CFG Register
(Size: 64 bits)

Device: 20
Function: 1

Default: 4h



Bit Range	Default & Access	Field Name (ID): Description
63:32	0h RW	**BASEADDR1_HIGH:** Base Address: Base address of the OCP fabric memory space. Taken from Strap values as ones
31:12	0h RW	**BASEADDR1:** This field is present if BAR1 is enabled through private configuration space.
11:4	0h RO	**SIZEINDICATOR1:** Always is 0 as minimum size is 4K
3	0h RO	**PREFETCHABLE1:** Indicates that this BAR is not prefetchable.
2:1	2h RO	**TYPE1:** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**MESSAGE_SPACE1:** 0 Indicates this BAR is present in the memory space.

22.1.8 (SUBSYSTEMID)—Offset 2Ch

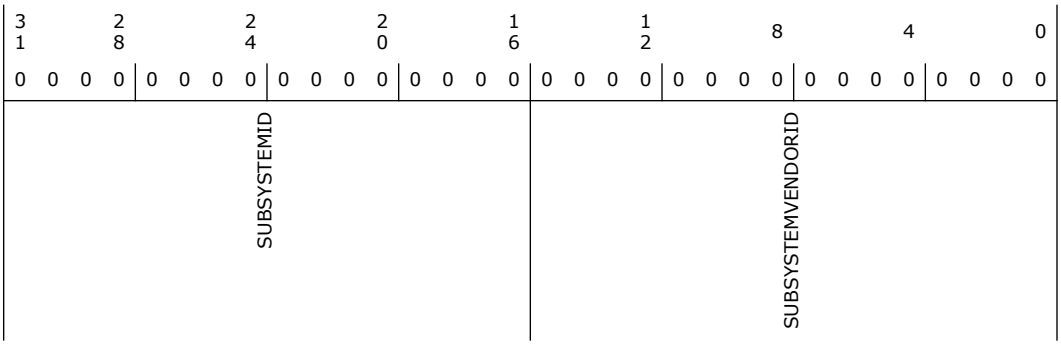
SUBSYSTEMID -Subsystem Vendor and Subsystem ID

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 1

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW/O	**SUBSYSTEMID:** Subsystem ID: This register is implemented for any function that can be instantiated more than once in a given system. The SID register, in combination with the Subsystem Vendor ID register make it possible for the operating environment to distinguish one subsystem from the other. This register is a Read Write Once type register.
15:0	0h RW/O	**SUBSYSTEMVENDORID:** This register must be implemented for any function that can be instantiated more than once in a given system. The SVID register, in combination with the Subsystem ID register, enables the operating environment to distinguish one subsystem from the other. This register is a Read Write Once register

22.1.9 (EXPANSION_ROM_BASEADDR)—Offset 30h

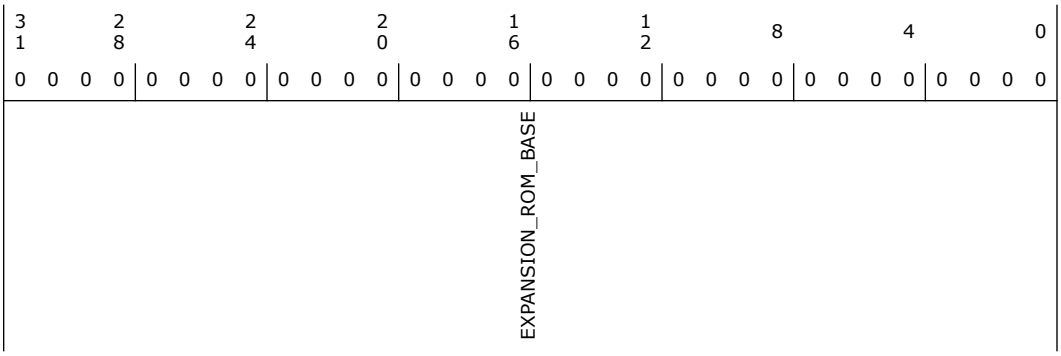
EXPANSION ROM base address

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 1

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**EXPANSION_ROM_BASE:** Expansion ROM Base Address: Value of all zeros indicates no support for Expansion ROM

22.1.10 (CAPABILITYPTR)—Offset 34h

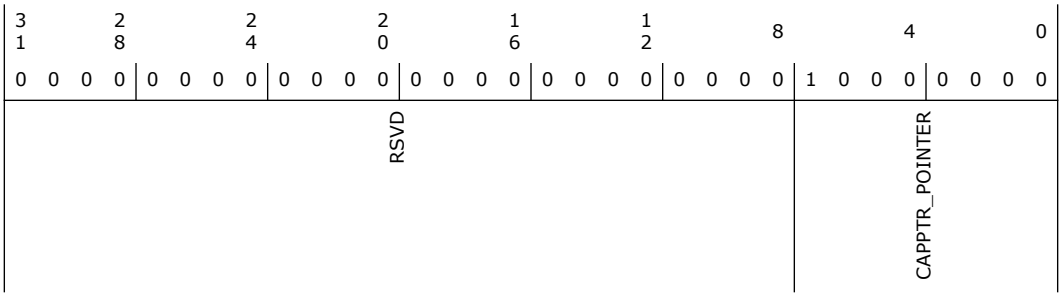
CAPABILITYPTR - Capabilities Pointer

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 1

Default: 80h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	80h RO	**Capabilities Pointer (CAPPTR_POINTER)**

22.1.11 (INTERRUPTREG)—Offset 3Ch

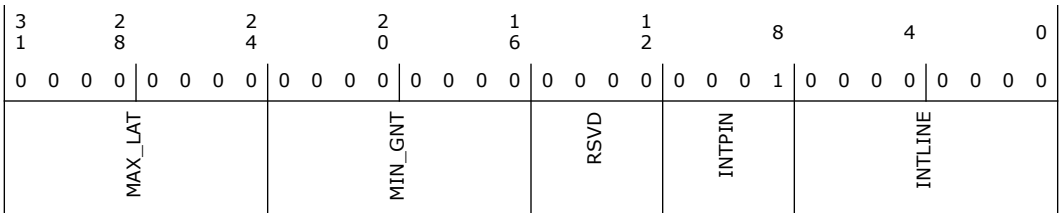
INTERRUPTREG - Interrupt Register

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 1

Default: 100h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**MAX_LAT:** Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	0h RO	**MIN_GNT:** Value of 0 indicates device has no major requirements for the settings of latency timers
15:12	0h RO	Reserved.
11:8	1h RO	**INTPIN:** Interrupt Pin Value in this register is reflected from the IPIN value in the private configuration space. For a single function device, this ideally is INTA.
7:0	0h RW	**INTLINE:** Bridge does not use this field directly. It is used to communicate to software, the interrupt line to which the interrupt pin is connected.

22.1.12 (POWERCAPID)—Offset 80h

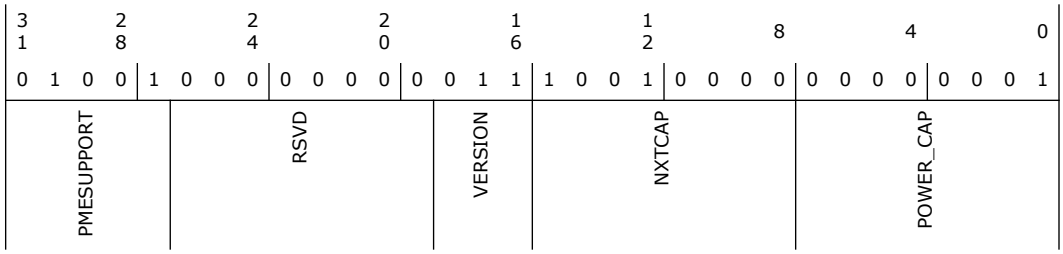
POWERCAPID - PowerManagement Capability ID

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 1

Default: 48039001h



Bit Range	Default & Access	Field Name (ID): Description
31:27	9h RO	**PMESUPPORT:** This 5-bit field indicates the power states in which the function can assert the PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal at the same time in that power state. bit(11) X XXX1b: PME# can be asserted from D0 bit(12) X XX1Xb: PME# can be asserted from D1. Bridge does not support this state. bit(13) X X1XXb: PME# can be asserted from D2. Bridge does not support this state. bit(14) X 1XXXb:PME# can be asserted from D3hot bit(15) 1 XXXXb:PME# can be asserted from D3cold. Bridge does not support this state. This field is taken from the private configuration space PME_Support XORed with the PME_Support strap.
26:19	0h RO	Reserved.
18:16	3h RO	**VERSION:** Indicates support for Revision 1.2 of the PCI Power Management Specification
15:8	90h RO	**NXTCAP:** Points to the next capability structure. This points to NULL.
7:0	1h RO	**POWER_CAP:** Indicates this is power management capability.

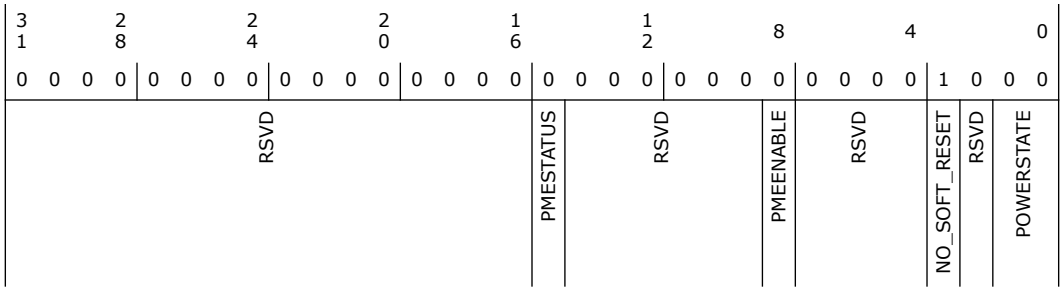
22.1.13 (PMECTRLSTATUS)—Offset 84h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 1

Default: 8h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	0h RW/1C	**PMESTATUS:** 0 Software clears the bit by writing a 1 to it. 1 This bit is set when the PME# signal is asserted independent of the state of the PME Enable bit (bit 8 in this register)
14:9	0h RO	Reserved.
8	0h RW	**PMEENABLE:** 1 Enables the function to assert PME#. 0 PME# message on Sideband is disabled
7:4	0h RO	Reserved.
3	1h RO	**NO_SOFT_RESET:** This bit indicates that devices transitioning from D3hot to D0 because of Powerstate commands do not perform an internal reset. Configuration Context is preserved.
2	0h RO	Reserved.
1:0	0h RW	**POWERSTATE:** This field is used both to determine the current power state and to set a new power state. The values are: 00 D0 state 11 D3HOT state Others Reserved

22.1.14 (PCIDEVIDLE_CAP_RECORD)—Offset 90h

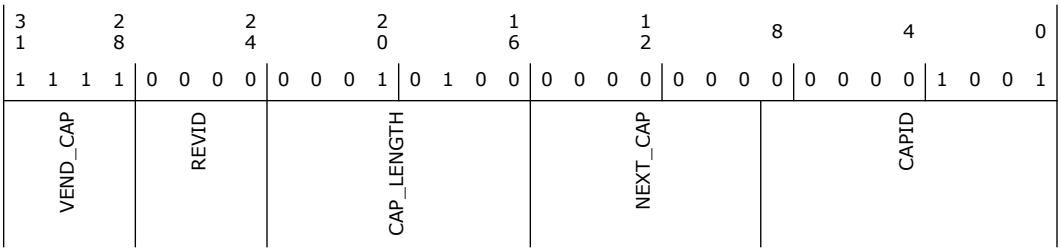
PCI DEVICE IDLE CAPABILITY RECORD

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 1

Default: F0140009h



Bit Range	Default & Access	Field Name (ID): Description
31:28	Fh RO	**VEND_CAP**
27:24	0h RO	**REVID**
23:16	14h RO	**CAP_LENGTH**
15:9	0h RO	**NEXT_CAP**
8:0	9h RO	**CAPID**

22.1.15 (DEVID_VEND_SPECIFIC_REG)—Offset 94h

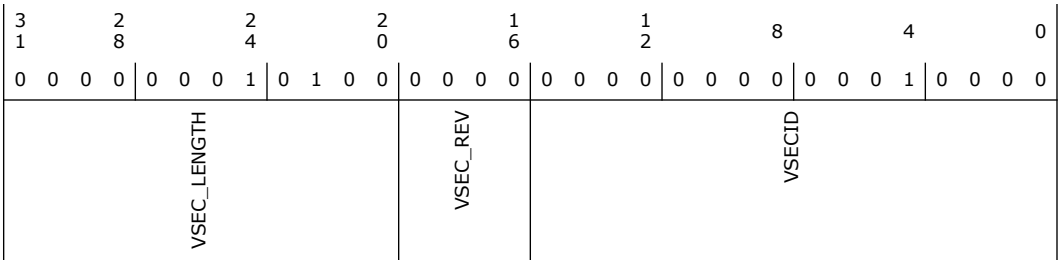
DEVID VENDOR SPECIFIC REG

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 1

Default: 1400010h



Bit Range	Default & Access	Field Name (ID): Description
31:20	14h RO	**VSEC_LENGTH**
19:16	0h RO	**VSEC_REV**
15:0	10h RO	**VSECID**

22.1.16 (D0I3_CONTROL_SW_LTR_MMIO_REG)—Offset 98h

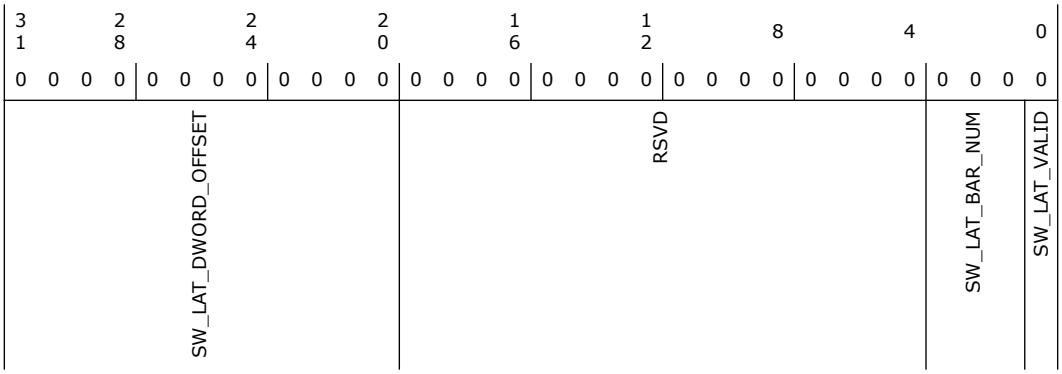
SW LTR Update MMIO Location Register

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 1

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**SW_LAT_DWORD_OFFSET**
19:4	0h RO	Reserved.
3:1	0h RO	**SW_LAT_BAR_NUM**
0	0h RO	**SW_LAT_VALID**

22.1.17 (DEVICE_IDLE_POINTER_REG)—Offset 9Ch

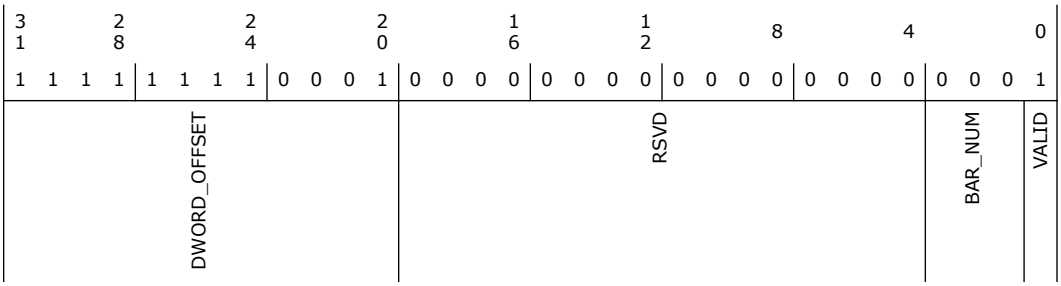
Device IDLE pointer register

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 1

Default: FF100001h



Bit Range	Default & Access	Field Name (ID): Description
31:20	FF1h RO	**DWORD_OFFSET**
19:4	0h RO	Reserved.
3:1	0h RO	**BAR_NUM**
0	1h RO	**VALID**

22.1.18 (D0I3_MAX_POW_LAT_PG_CONFIG)—Offset A0h

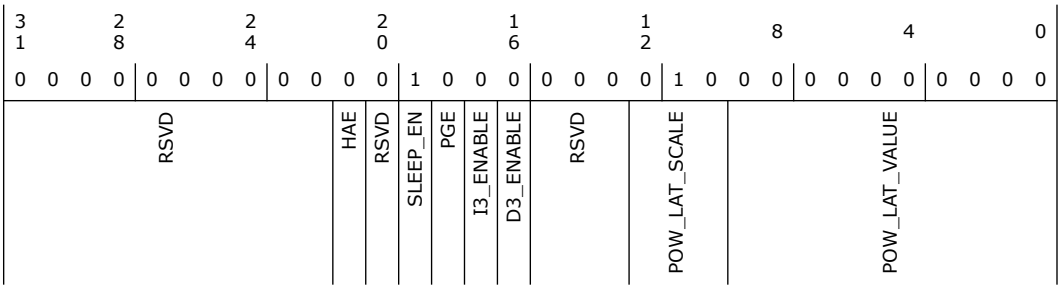
DEVICE PG CONFIG

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 1

Default: 80800h



Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	Reserved.
21	0h RW	**HAE**
20	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
19	1h RW	**SLEEP_EN**
18	0h RW	**PGE**
17	0h RW	**I3_ENABLE**
16	0h RW	**D3_ENABLE**
15:13	0h RO	Reserved.
12:10	2h RW	**POW_LAT_SCALE**
9:0	0h RW	**POW_LAT_VALUE**

22.1.19 (GEN_REGRW1)—Offset B0h

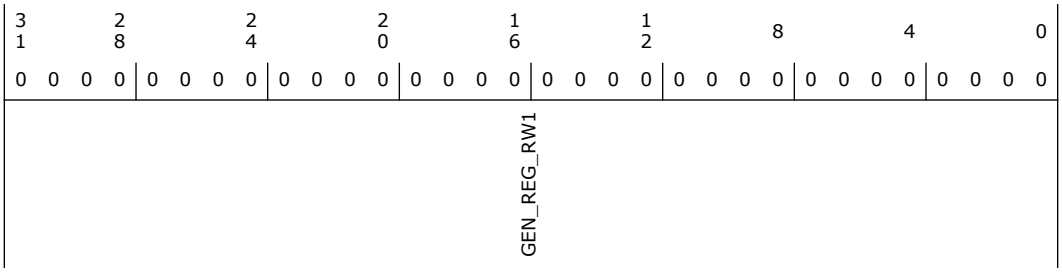
General Purpose Read Write Register1

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 1

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**GEN_REG_RW1**

22.1.20 (GEN_REGRW2)—Offset B4h

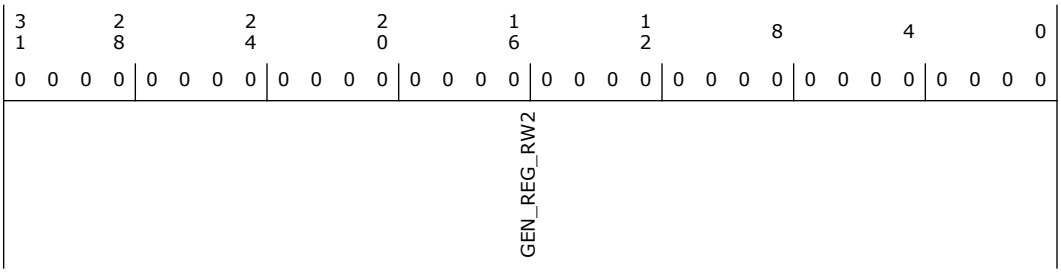
General Purpose Read Write Register2

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 1

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**GEN_REG_RW2**

22.1.21 (GEN_REGRW3)—Offset B8h

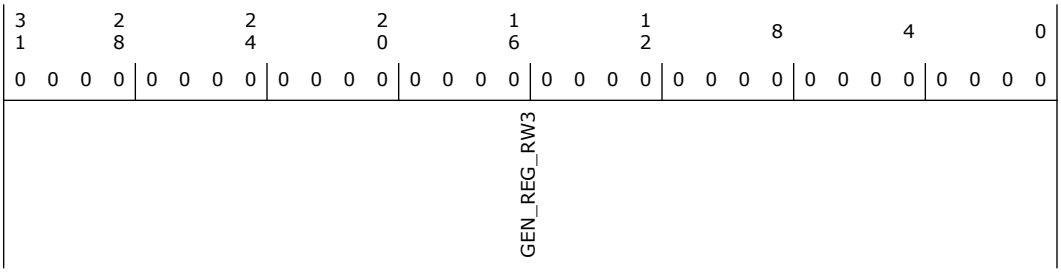
General Purpose Read Write Register3

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 1

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**GEN_REG_RW3**

22.1.22 (GEN_REGRW4)—Offset BCh

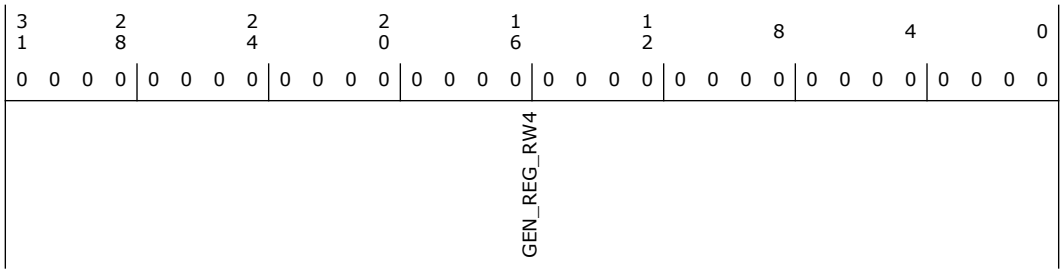
General Purpose Read Write Register4

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 1

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**GEN_REG_RW4**

22.1.23 (GEN_INPUT_REGRW)—Offset C0h

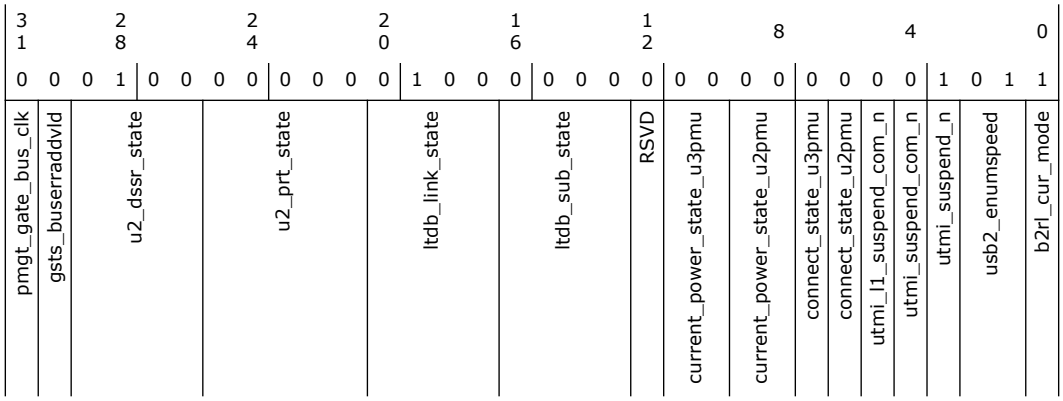
General Purpose Input Register

Access Method

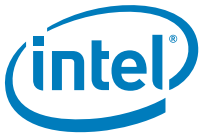
Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 1

Default: 1008000Bh



Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**pmgt_gate_bus_clk:** Indicates that the conditions are appropriate for some internal modules to receive a gated bus_clk. This signal is used by the test environment to verify low power operation.
30	0h RO	**gsts_buserraddvld:** Bus error
29:26	4h RO	**u2_dssr_state:** USB2 DSSR State



Bit Range	Default & Access	Field Name (ID): Description
25:21	0h RO	**u2_prt_state:** USB2 Port State
20:17	4h RO	**ltdb_link_state:** USB3 Link state
16:13	0h RO	**ltdb_sub_state:** USB3 Link sub state
12	0h RO	Reserved.
11:10	0h RO	**current_power_state_u3pmu:** The current power state of the core. When equal to '3', the PMU is controlling the PHY, and when equal to '0', the core is controlling the PHY
9:8	0h RO	**current_power_state_u2pmu:** The current power state of the core. When equal to '3', the PMU is controlling the PHY, and when equal to '0', the core is controlling the PHY
7	0h RO	**connect_state_u3pmu:** When '1', indicates the PMU is maintaining at least one connection to the host or a device (the link is in U3). When '0', indicates the PMU has no connection to the host or any device.
6	0h RO	**connect_state_u2pmu:** When '1', indicates the PMU is maintaining at least one connection to the host or a device (the link is in L1, L2). When '0', indicates the PMU has no connection to the host or any device
5	0h RO	**utmi_l1_suspend_com_n:** Common L1 suspend
4	0h RO	**utmi_suspend_com_n:** Common suspend
3	1h RO	**utmi_suspend_n:** USB 2.0 Port Suspend
2:1	1h RO	**usb2_enumspeed:** Device Enumerated Speed
0	1h RO	**b2rl_cur_mode:** Current Mode. Current Mode 1'b0 Host ,1'b1 Device

22.2 xDCI MMIO Device Registers Summary

Table 22-2. Summary of xDCI MMIO Device Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
C700h	C703h	Device Configuration Register (DCFG)—Offset C700h	80004h
C704h	C707h	Device Control Register (DCTL)—Offset C704h	F00000h
C708h	C70Bh	Device Event Enable Register (DEVTEN)—Offset C708h	0h
C70Ch	C70Fh	Device Status Register (DSTS)—Offset C70Ch	520004h
C710h	C713h	Device Generic Command Parameter (DGCMDPAR)—Offset C710h	0h
C714h	C717h	Device Generic Command Register (DGCMD)—Offset C714h	0h
C720h	C723h	Device Active USB Endpoint Enable (DALEPENA)—Offset C720h	0h
C800h	C803h	Device Physical Endpoint-n Command Parameter 2 Register (DEPCMDPAR2)—Offset C800h	0h

Table 22-2. Summary of xDCI MMIO Device Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
C804h	C807h	Device Physical Endpoint-n Command Parameter 1 Register (DEPCMDPAR1)—Offset C804h	0h
C808h	C80Bh	Device Physical Endpoint-n Command Parameter 0 Register (DEPCMDPAR0)—Offset C808h	0h
C80Ch	C80Fh	Device Physical Endpoint-n Command Register (DEPCMD)—Offset C80Ch	0h

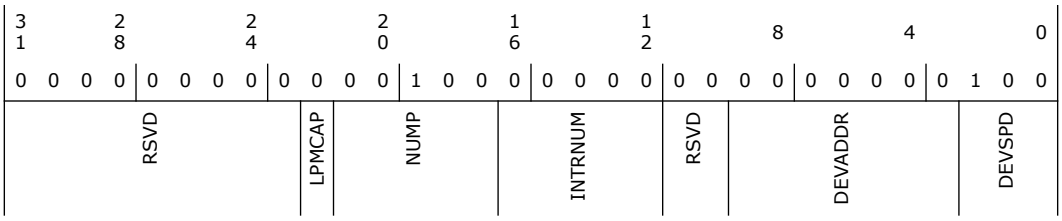
22.2.1 Device Configuration Register (DCFG)—Offset C700h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 20
Function: 1

Default: 80004h



Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	Reserved.
22	0h RW	**LPM Capable (LPMCAP):** The application uses this bit to control the LPM capabilities: 1'b0: LPM capability is not enabled. 1'b1: LPM capability is enabled.
21:17	4h RW	**Number of Receive Buffers (NUMP):** This bit indicates the number of receive buffers to be reported in the ACK TP.
16:12	0h RW	**Interrupt Number (INTRNUM):** Indicates interrupt number on which non-endpoint-specific device-related interrupts are generated.
11:10	0h RO	Reserved.
9:3	0h RW	**Device Address (DEVADDR)**
2:0	4h RW	**Device Speed (DEVSPD):** Indicates the speed at which the application requires the core to connect, or the maximum speed the application can support: 3'b100: SuperSpeed 3'b000: High-speed 3'b001: Full-speed

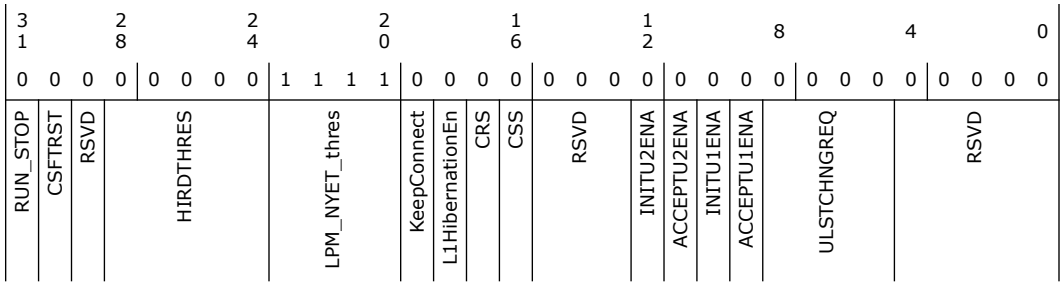
22.2.2 Device Control Register (DCTL)—Offset C704h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 20
Function: 1

Default: F00000h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Run/Stop (RUN_STOP):** The software writes 1 to this bit to start the device controller operation. To stop the device controller operation, the software must remove any active transfers and write 0 to this bit. When the controller is stopped, it sets the DSTS.DevCtrlHlt bit when the core is idle and the lower layer finishes the disconnect process. The Run/Stop bit must be used in following cases as specified: 1.After power-on reset and CSR initialization, the software must write 1 to this bit to start the device controller. The controller does not signal connect to the host until this bit is set. 2.The software uses this bit to control the device controller to perform a soft disconnect. When the software writes 0 to this bit, the host does not see that the device is connected. The device controller stays in the disconnected state until the software writes 1 to this bit. The minimum duration of keeping this bit cleared: SS: 30ms HS/FS/LS: 10ms If the software attempts a connect after the soft disconnect or detects a disconnect event, it must set DCTL[8:5] to 5 before reasserting the Run/Stop bit. 3.When the USB or Link is in a lower power state and the Two Power Rails configuration is selected, software writes 0 to this bit to indicate that it is going to turn off the Core Power Rail. After the software turns on the Core Power Rail again and re-initializes the device controller, it must set this bit to start the device controller.
30	0h RW	**Core Soft Reset (CSFTRST):** Resets the all clock domains
29	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
28:24	0h RW	**HIRD Threshold (HIRDTHRES):** The core asserts output signals utmi_l1_suspend_n and utmi_sleep_n on the basis of this signal: The core asserts utmi_l1_suspend_n to put the PHY into Deep Low-Power mode in L1 when both of the following are true: -HIRD value is greater than or equal to the value in DCTL.HIRD_Thres[3:0] -HIRD_Thres[4] is set to 1'b1. The core asserts utmi_sleep_n on L1 when one of the following is true: -If the HIRD value is less than HIRD_Thres[3:0] or -HIRD_Thres[4] is set to 1'b0. Note: This field must be set to '0' during SuperSpeed mode of operation.
23:20	Fh RW	**LPM NYET Response Threshold (LPM_NYET_thres):** Handshake response to LPM token specified by device application
19	0h RW	**Keep Connect (KeepConnect):** When '1', this bit enables the save and restore programming model by preventing the core from disconnecting from the host when DCTL.RunStop is set to '0'. It also enables the Hibernation Request Event to be generated when the link goes to U3 or L2. The device core disconnects from the host when DCTL.RunStop is set to '0'. This bit indicates whether to preserve this behavior ('0'), or if the core should not disconnect when RunStop is set to 0 ('1'). This bit also prevents the LTSSM from automatically going to U0/ L0 when the host requests resume from U3/L2.
18	0h RW	**L1 Hibernation Enable (L1HibernationEn):** When this bit is set along with KeepConnect, the device core generates a Hibernation Request Event if L1 is enabled and the HIRD value in the LPM token is larger than the threshold programmed in DCTL.HIRD_Thres. The core will not exit the LPM L1 state until software writes Recovery into the DCTL.ULStChngReq field. This prevents corner cases where the device is entering hibernation at the same time the host is attempting to exit L1.
17	0h RW	**Controller Restore State (CRS):** This command initiates the restore process. When software sets this bit to '1', the controller immediately sets DSTS.RSS to '1'. When the controller has finished the restore process, it sets DSTS.RSS to '0'. Note: When read, this field always returns '0'.
16	0h RW	**Controller Save State (CSS):** This command initiates the save process. When software sets this bit to '1', the controller immediately sets DSTS.SSS to '1'. When the controller has finished the save process, it sets DSTS.SSS to '0'. Note: When read, this field always returns '0'.
15:13	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW	**Initiate U2 Enable (INITU2ENA):** 1'b0: May not initiate U2 (default) 1'b1: May initiate U2 On USB reset, hardware clears this bit to ”0”. Software sets this bit after receiving SetFeature(U2_ENABLE), and clears this bit when ClearFeature(U2_ENABLE) is received. If DCTL[11] (AcceptU2Ena) is 0, the link immediately exits U2 state.
11	0h RW	**Accept U2 Enable (ACCEPTU2ENA):** 1'b0: Reject U2 except when Force_LinkPM_Accept bit is set (default) 1'b1: Core accepts transition to U2 state if nothing is pending on the application side. On USB reset, hardware clears this bit to ”0”. Software sets this bit after receiving a SetConfiguration command
10	0h RW	**Initiate U1 Enable (INITU1ENA):** 1'b0: May not initiate U1 1'b1: May initiate U1 On USB reset, hardware clears this bit to “0”. Software sets this bit after receiving SetFeature(U1_ENABLE), and clears this bit when ClearFeature(U1_ENABLE) is received. If DCTL[9] (AcceptU1Ena) is 0, the link immediately exits U1 state.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Accept U1 Enable (ACCEPTU1ENA):** 1'b0: Core rejects U1 except when Force_LinkPM_Accept bit is set (default) 1'b1: Core accepts transition to U1 state if nothing is pending on the application side. On USB reset, hardware clears this bit to "0". Software sets this bit after receiving a SetConfiguration command.
8:5	0h WO	**USB / Link State Change Request (ULSTCHNGREQ):** Software writes this field to issue a USB/Link state change request. A change in this field indicates a new request to the core. If software wants to issue the same request back-to-back, it must write a 0 to this field between the two requests. The result of the state change request is reflected in the USB/Link State in DSTS. These bits are self-cleared on the MAC Layer exiting suspended state. If software is updating other fields of the DCTL register and not intending to force any link state change, then it must write a 0 to this field. SS Compliance mode is normally entered and controlled by the remote link partner. Alternatively, the local link can be forced directly into Compliance mode by resetting the SS link with the RUN/STOP bit set to zero. If then '10' is written to the USB/Link State Change field and '1' to RUN/STOP, the Link will go to Compliance. Once in Compliance, 'zero' and '10' may alternately be written to this field to advance the compliance pattern. In SS mode: ValueRequested Link State Transition: 0:No Action 4:SS.Disabled 5:Rx.Detect 6:SS.Inactive 8:Recovery 10:Compliance Others:Reserved In HS/FS/LS mode: ValueRequested USB state transition 8:Remote wakeup request Others:Reserved The Remote wakeup request should be issued 2µs after the device goes into suspend state. Note: After coming out of hibernation, software should write 8 (Recovery) into this field to confirm exit from the suspended state
4:0	0h RO	Reserved.

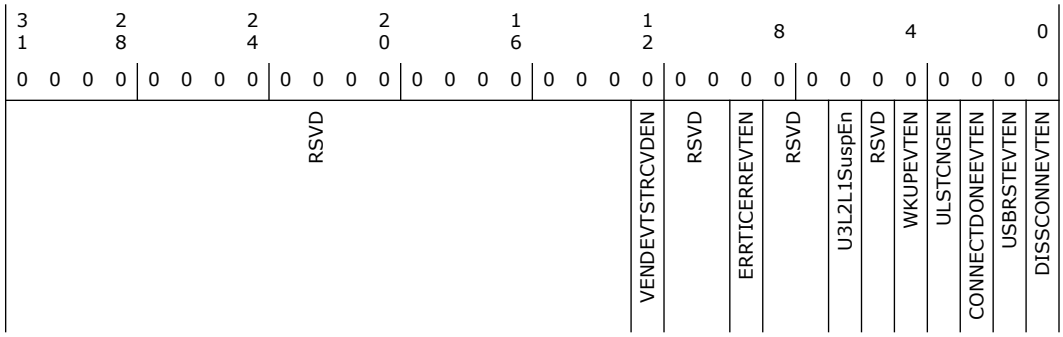
22.2.3 Device Event Enable Register (DEVTEN)—Offset C708h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 20
Function: 1

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	Reserved.
12	0h RW	**Vendor Device Test LMP Received Event (VENDEVTSTRCVDEN)**
11:10	0h RO	Reserved.
9	0h RW	**Erratic Error Event Enable (ERRTICERREVTEN)**
8:7	0h RO	Reserved.
6	0h RW	**U3/L2-L1 Suspend Event Enable (U3L2L1SuspEn)**
5	0h RO	Reserved.
4	0h RW	**Resume/Remote Wakeup Detected Event Enable (WKUPEVTEN)**
3	0h RW	**USB/Link State Change Event Enable (ULSTCNGEN)**
2	0h RW	**Connection Done Enable (CONNECTDONEEVTEN)**
1	0h RW	**USB Reset Enable (USBRSTEVTEN)**
0	0h RW	**Disconnect Detected Event Enable (DISSCONNEVTEN)**

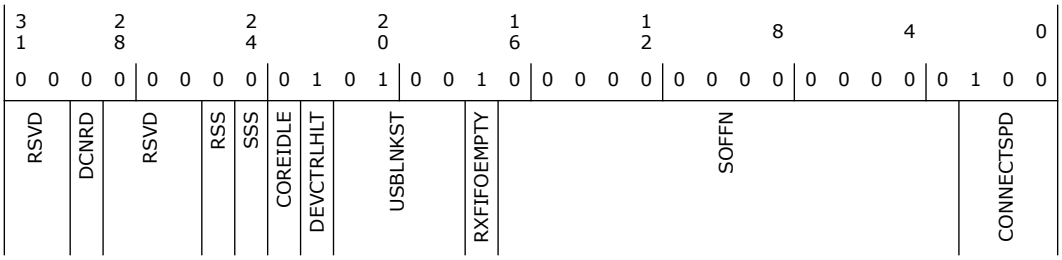
22.2.4 Device Status Register (DSTS)—Offset C70Ch

Access Method

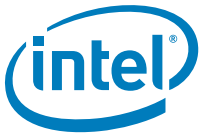
Type: MEM Register
(Size: 32 bits)

Device: 20
Function: 1

Default: 520004h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29	0h RO	**Device Controller Not Ready (DCNRD):** The bit indicates that the core is in the process of completing the state transitions after exiting from hibernation. To complete the state transitions, it takes 256 bus clock cycles from the time DCTL[31].Run/Stop is set. During hibernation, if the UTMI/ULPI PHY is in suspended state, then the 256-bus clock cycle delay starts after the PHY exited suspended state. Software must set DCTL[31].Run/Stop to '1' and wait for this bit to be de-asserted to zero before processing DSTS.USBLnkSt. This bit is valid only when DWC_USB3_EN_PWROPT is set to two and GCTL[1].GblHibernationEn =1.
28:26	0h RO	Reserved.
25	0h RO	**Restore State Status (RSS):** When the controller has finished the restore process, it will complete the command by setting DSTS.RSS to '0'.
24	0h RO	**Save State Status (SSS):** When the controller has finished the save process, it will complete the command by setting DSTS.SSS to '0'.
23	0h RO	**Core Idle (COREIDLE):** The bit indicates that the core finished transferring all RxFIFO data to system memory, writing out all completed descriptors, and all Event Counts are zero.
22	1h RO	**Device Controller Halted (DEVCTRLHLT):** This bit is set to 0 when the Run/Stop bit in the DCTL register is set to 1. The core sets this bit to 1 when, after SW sets Run/Stop to '0', the core is idle and the lower layer finishes the disconnect process. When Halted =1, the core does not generate Device events.



Bit Range	Default & Access	Field Name (ID): Description
21:18	4h RO	**USB/Link State (USBLNKST):** In SS mode: 4'h0: U0 4'h1: U1 4'h2: U2 4'h3: U3 4'h4: SS_DIS 4'h5: RX_DET 4'h6: SS_INACT 4'h7: POLL 4'h8: RECOV 4'h9: HRESET 4'ha: CMPLY 4'hb: LPBK 4'hf: Resume/Reset In HS/FS/LS mode: 4'h0: On state 4'h2: Sleep (L1) state 4'h3: Suspend (L2) state 4'h4: Disconnected state 4'h5: Early Suspend state 4'he: Reset 4'hf: Resume
17	1h RO	**RxFIFO Empty (RXFIFOEMPTY)**
16:3	0h RO	**Frame/Microframe Number of the Received SOF (SOFFN):** When the core is operating at high-speed: [16:6] indicates the frame number [5:3] indicates the microframe number When the core is operating at full-speed: [16:14] is not used. Software can ignore these 3 bits [13:3] indicates the frame number
2:0	4h RO	**Connected Speed (CONNECTSPD):** Indicates the speed at which the core has come up after speed detection through a chirp sequence: 3'b100: SuperSpeed 3'b000: High-speed 3'b001: Full-speed 3'b010: Low-speed 3'b011: Full-speed

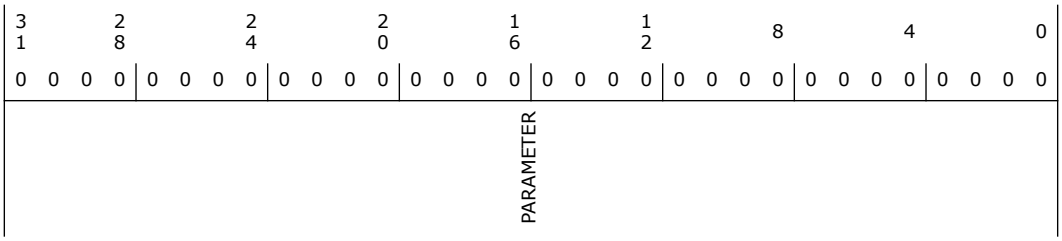
22.2.5 Device Generic Command Parameter (DGCMDPAR)—Offset C710h

Access Method

Type: MEM Register (Size: 32 bits)

Device: 20
Function: 1

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER):** This register indicates the device command parameter. This must be programmed before or along with the device command (DGCMD).

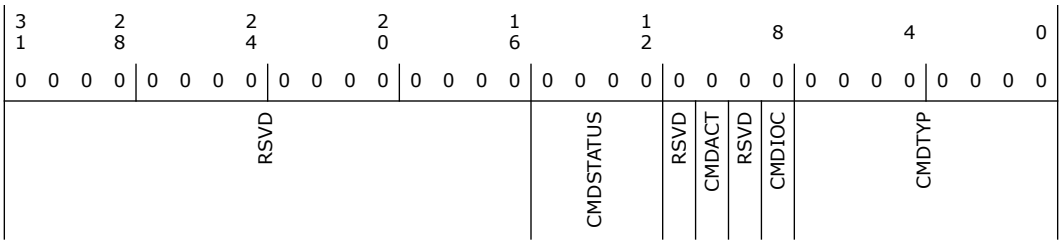
22.2.6 Device Generic Command Register (DGCMD)—Offset C714h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 20
Function: 1

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:12	0h RO	**Command Status (CMDSTATUS):** 1: CmdErr – Indicates that the device controller encountered an error while processing the command. 0: Indicates command success
11	0h RO	Reserved.
10	0h NA	**Command Active (CMDACT):** The software sets this bit to 1 to enable the device controller to execute the generic command. The device controller sets this bit to 0 after executing the command.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RO	Reserved.
8	0h RW	**Command Interrupt on Complete (CMDIOC):** When this bit is set, the device controller issues a Generic Command Completion event after executing the command. Note that this interrupt is mapped to DCFG.IntrNum. Note: This field must not set to '1' if the DCTL.RunStop field is '0'.
7:0	0h RW	**Command Type (CMDTYP):** Specifies the type of command the software driver is requesting the core to perform: 02h: Set Periodic Parameters 04h: Set Scratchpad Buffer Array Address Lo 05h: Set Scratchpad Buffer Array Address Hi 07h:Transmit Device Notification 09h: Selected FIFO Flush 0Ah: All FIFO Flush 0Ch: Set Endpoint NRDY 10h: Run SoC Bus LoopBack Test

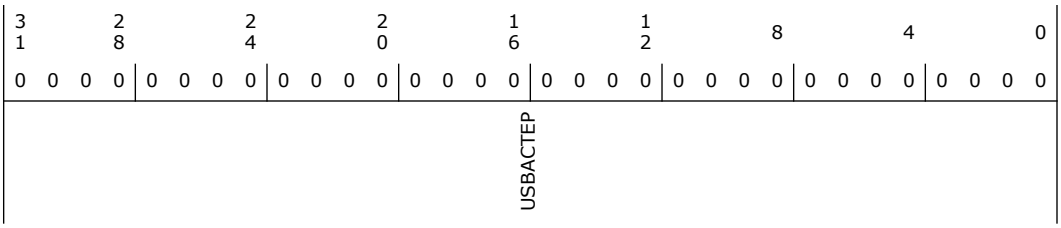
22.2.7 Device Active USB Endpoint Enable (DALEPENA)—Offset C720h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 20
Function: 1

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**USB Active Endpoints (USBACTEP):** This field indicates if a USB endpoint is active in the current configuration and interface. Bit[0]: USB EP0-OUT Bit[1]: USB EP0-IN Bit[2]: USB EP1-OUT Bit[3]: USB EP1-IN

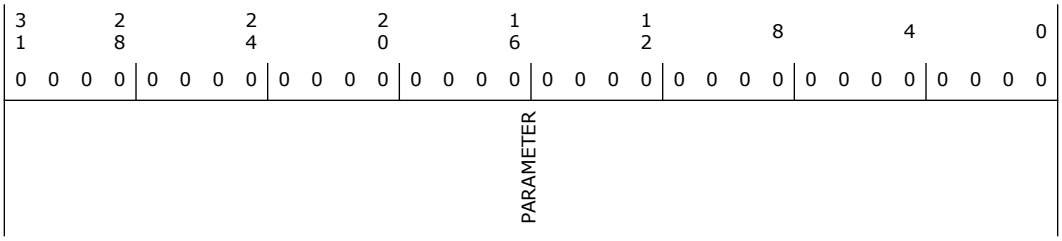
22.2.8 Device Physical Endpoint-n Command Parameter 2 Register (DEPCMDPAR2)—Offset C800h

Physical_Endpoint_number: 0 <= n <= 31; Offset: based offset + (Physical_Endpoint_number * 10’h)

Access Method

Type: MEM Register (Size: 32 bits)
Device: 20
Function: 1

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER):** This register indicates the physical endpoint command Parameter 2. It must be programmed before issuing the command.

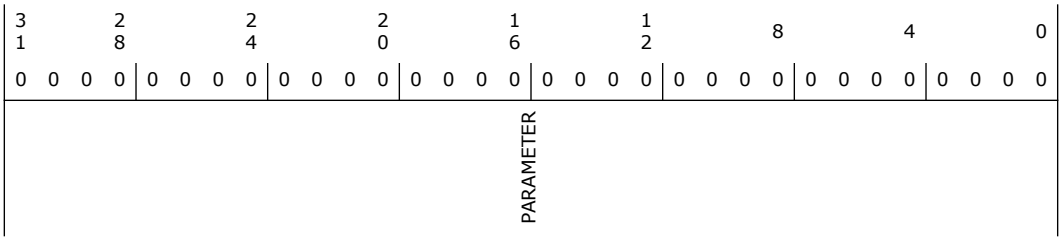
22.2.9 Device Physical Endpoint-n Command Parameter 1 Register (DEPCMDPAR1)—Offset C804h

Physical_Endpoint_number: 0 <= n <= 31; Offset: based offset + (Physical_Endpoint_number * 10’h)

Access Method

Type: MEM Register (Size: 32 bits)
Device: 20
Function: 1

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER):** This register indicates the physical endpoint command Parameter 1. It must be programmed before issuing the command

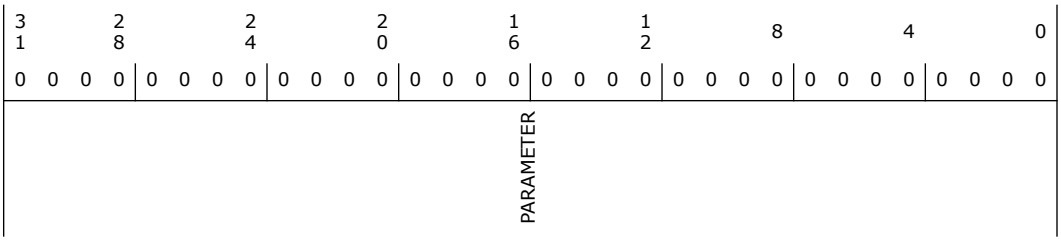
22.2.10 Device Physical Endpoint-n Command Parameter 0 Register (DEPCMDPAR0)—Offset C808h

Physical_Endpoint_number: 0 <= n <= 31; Offset: based offset + (Physical_Endpoint_number * 10’h)

Access Method

Type: MEM Register (Size: 32 bits)
Device: 20
Function: 1

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER):** This register indicates the physical endpoint command parameter 0. This must be programmed before or along with the command. For commands needing only one 32-bit parameter, this register must be programmed with the command register.

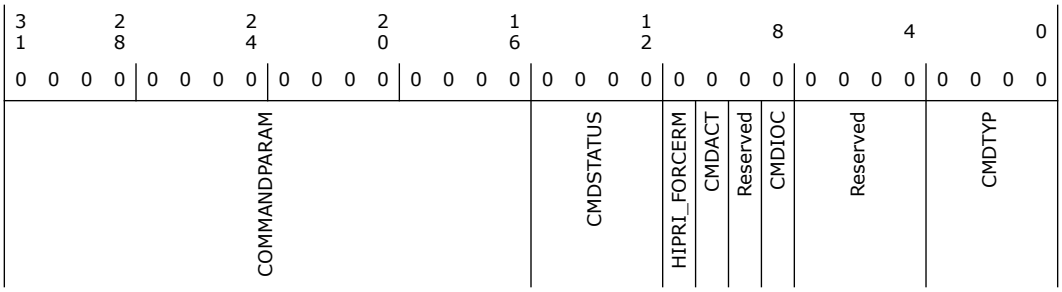
22.2.11 Device Physical Endpoint-n Command Register (DEPCMD)—Offset C80Ch

Physical_Endpoint_number: 0 <= n <= 31; Offset: based offset + (Physical_Endpoint_number * 10’h)

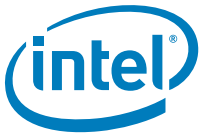
Access Method

Type: MEM Register (Size: 32 bits)
Device: 20
Function: 1

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Command Parameters (COMMANDPARAM):** when this register is written: For Start Transfer command: -[31:16]: StreamID. The USB StreamID assigned to this transfer For Start Transfer command applied to an isochronous endpoint: -[31:16]: StartMicroFramNum: Indicates the (micro)frame number to which the first TRB applies For Update Transfer, End Transfer, and Start New Configuration commands: -[22:16]: Transfer Resource Index (XferRscIdx). The hardware-assigned transfer resource index for the transfer, which was returned in response to the Start Transfer command. The application software-assigned transfer resource index for a Start New Configuration command
15:12	0h RW	**Command Completion Status (CMDSTATUS):** Additional information about the completion of this command is available in this field.
11	0h RW	**HighPriority/ForceRM (HIPRI_FORCERM):** HighPriority: Only valid for Start Transfer command ForceRM: Only valid for End Transfer command ClearPendIN: Only valid for Clear Stall command – Software sets this bit to clear any pending IN transaction (on that endpoint) stuck at the lower layers when a Clear Stall command is issued.
10	0h RW	**Command Active (CMDACT):** Software sets this bit to 1 to enable the device endpoint controller to execute the generic command. The device controller sets this bit to 0 when the CmdStatus field is valid and the endpoint is ready to accept another command. This does not imply that all the effects of the previously-issued command have taken place.
9	0h RW	**Reserved (Reserved)**



Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**Command Interrupt on Complete (CMDIOC):** When this bit is set, the device controller issues a generic Endpoint Command Complete event after executing the command. Note that this interrupt is mapped to DEPCFG.IntrNum. When the DEPCFG command is executed, the command interrupt on completion goes to the interrupt pointed by the DEPCFG.IntrNum in the current command. Note: This field must not set to '1' if the DCTL.RunStop field is '0'.
7:4	0h RW	**Reserved (Reserved)**
3:0	0h RW	**Command Type (CMDTYP):** Specifies the type of command the software driver is requesting the core to perform. 00h: Reserved 01h: Set Endpoint Configuration -64 or 96-bit Parameter 02h: Set Endpoint Transfer Resource Configuration -32-bit Parameter 03h: Get Endpoint State -No Parameter Needed 04h: Set Stall -No Parameter Needed 05h: Clear Stall (see Set Stall) -No Parameter Needed 06h: Start Transfer -64-bit Parameter 07h: Update Transfer -No Parameter Needed 08h: End Transfer -No Parameter Needed 09h: Start New Configuration -No Parameter Needed

22.3 xDCI MMIO Global Registers Summary

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
C100h	C103h	Global SoC Bus Configuration 0 (GSBUSCFG0)—Offset C100h	6h
C104h	C107h	Global SoC Bus Configuration 1 (GSBUSCFG1)—Offset C104h	F00h
C108h	C10Bh	Global Tx Threshold Control (GTXTHRCFG)—Offset C108h	0h
C10Ch	C10Fh	Global Rx Threshold Control (GRXTHRCFG)—Offset C10Ch	24400000h
C110h	C113h	Global Core Control (GCTL)—Offset C110h	2000h
C114h	C117h	GPMSTS (GPMSTS)—Offset C114h	0h
C118h	C11Bh	Global Status (GSTS)—Offset C118h	0h
C130h	C133h	Bus Address Low (GBUSERRADDRLO)—Offset C130h	0h
C134h	C137h	Bus Address High (GBUSERRADDRHI)—Offset C134h	0h
C140h	C143h	GHWPARAMS0 (GHWPARAMS0)—Offset C140h	40204008h
C144h	C147h	GHWPARAMS1 (GHWPARAMS1)—Offset C144h	260C93Bh
C148h	C14Bh	GHWPARAMS2 (GHWPARAMS2)—Offset C148h	8086A0h
C14Ch	C14Fh	GHWPARAMS3 (GHWPARAMS3)—Offset C14Ch	10420085h
C150h	C153h	GHWPARAMS4 (GHWPARAMS4)—Offset C150h	222004h
C154h	C157h	GHWPARAMS5 (GHWPARAMS5)—Offset C154h	4202088h

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
C158h	C15Bh	GHWPARAMS6 (GHWPARAMS6)—Offset C158h	2F60020h
C15Ch	C15Fh	GHWPARAMS7 (GHWPARAMS7)—Offset C15Ch	38507E6h
C160h	C163h	GDBGFIFOSPACE (GDBGFIFOSPACE)—Offset C160h	420000h
C164h	C167h	GDBGLTSSM (GDBGLTSSM)—Offset C164h	41010440h
C168h	C16Bh	GDBGLNMCC (GDBGLNMCC)—Offset C168h	0h
C16Ch	C16Fh	GDBGBMU (GDBGBMU)—Offset C16Ch	0h
C174h	C177h	GDBGLSP (GDBGLSP)—Offset C174h	0h
C178h	C17Bh	GDBGEPINFO0 (GDBGEPINFO0)—Offset C178h	0h
C17Ch	C17Fh	GDBGEPINFO1 (GDBGEPINFO1)—Offset C17Ch	800000h
C300h	C303h	Global Transmit FIFO Size Register N (GTXFIFOSIZ0_0)—Offset C300h	42h
C380h	C383h	GRXFIFOSIZ0_0 (GRXFIFOSIZ0_0)—Offset C380h	385h
C400h	C403h	GEVNTADRLO_0 (GEVNTADRLO_0)—Offset C400h	0h
C404h	C407h	GEVNTADRHI_0 (GEVNTADRHI_0)—Offset C404h	0h
C40Ch	C40Fh	GEVNTCOUNT_0 (GEVNTCOUNT_0)—Offset C40Ch	0h
C610h	C613h	GTXFIFOPRIDEV (GTXFIFOPRIDEV)—Offset C610h	0h

22.3.1 Global SoC Bus Configuration 0 (GSBUSCFG0)—Offset C100h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 6h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	Reserved.
11	0h RW	**Data Access is Big-Endian (DATBIGEND):** This bit controls the endian mode for data accesses. 0: Little-endian (default) 1: Big-endian In big-endian mode, DMA access (both read and write) for packet data will utilize a Byte Invariant Big-Endian mode. Note: Since AXI requires byteinvariant endianness, setting DescBigend and DatBigEnd to one causes an address invariant transform to be applied, which is not appropriate. See section 9.3 and 9.4 of the AMBA AXI Specification. Hence for an AXI master (DWC_USB3_MBUS_TYPE=1), this bit must be set to zero.
10:8	0h RO	Reserved.
7	0h RW	**INCR256 Burst Type Enable (INCR256BRSTENA):** If software set this bit to “1”, the master uses INCR to do the 256-beat burst.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**INCR128 Burst Type Enable (INCR128BRSTENA):** If software set this bit to “1”, the master uses INCR to do the 128-beat burst.
5	0h RW	**INCR64 Burst Type Enable (INCR64BRSTENA):** If software set this bit to “1”, the master uses INCR to do the 64-beat burst.
4	0h RW	**INCR32 Burst Type Enable (INCR32BRSTENA):** If software set this bit to “1”, the master uses INCR to do the 32-beat burst.
3	0h RW	**INCR16 Burst Type Enable (INCR16BRSTENA):** If software set this bit to "1", the master uses INCR to do the 16-beat burst.
2	1h RW	**INCR8 Burst Type Enable (INCR8BRSTENA):** if software set this bit to "1", the master uses INCR to do the 8-beat burst
1	1h RW	**INCR4 Burst Type Enable (INCR4BRSTENA):** When this bit is enabled the controller is allowed to do bursts of beat length 1, 2, 3, and 4
0	0h RW	**Undefined Length INCR Burst Type Enable (INCRBrstEna) Input to BUS-GM (INCRBRSTENA):** When enabled, this has higher priority than other burst types. For the AHB configuration. if this bit is set to 1, AHB master tries to do only one INCR burst for each transfer unless it has to break it at a 1Kbyte boundary. If this bit is set to 0, the AHB master may still use INCR burst type at the beginning and end bursts of transfers to align the address. The middle bursts are INCR4/8/16, depending when the type is enabled.

22.3.2 Global SoC Bus Configuration 1 (GSBUSCFG1)—Offset C104h

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: F00h

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	Reserved.
12	0h RW	**1k Page Boundary Enable (EN1KPAGE):** By default (this bit is disabled) the AXI breaks transfers at the 4k page boundary. When this bit is enabled, the AXI master (DMA data) breaks transfers at the 1k page boundary.
11:8	Fh RW	**AXI Pipelined Transfers Burst Request Limit (PipeTransLimit):** The field controls the number of outstanding pipelined transfers requests the AXI master will push to the AXI slave. Once the AXI master reaches this limit, it will not make more requests on the AXI ARADDR and AWADDR buses until the associated data phases complete. This field is encoded as follows: h0: 1 request h1: 2 requests h2: 3 requests h3: 4 requests ... hF: 16 requests
7:0	0h RO	Reserved.

22.3.3 Global Tx Threshold Control (GTXTHRCFG)—Offset C108h

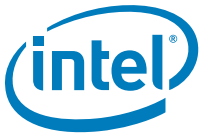
Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29	0h RO	**USB Transmit Packet Count Enable (USBTxPktCntSel):** This field enables/disables the USB transmission multi-packet thresholding: 0: USB transmission multi-packet thresholding is disabled, the core can only start transmission on the USB after the entire packet has been fetched into the corresponding TXFIFO. 1: USB transmission multi-packet thresholding is enabled. The core can only start transmission on the USB after USB Transmit Packet Count amount of packets for the USB transaction (burst) are already in the corresponding TXFIFO This mode is only valid in the host mode. It is only used for SuperSpeed.
28	0h RO	Reserved.



Bit Range	Default & Access	Field Name (ID): Description
27:24	0h RO	**USB Transmit Packet Count (USBTxPktCnt):** This field specifies the number of packets that must be in the TXFIFO before the core can start transmission for the corresponding USB transaction (burst). This field is only valid when the USB Transmit Packet Count Enable field is set to one. Valid values are from 1 to 15.
23:16	0h RW	**USB Maximum TX Burst Size (USBMaxTxBurstSize):** When USBTxPktCntSel is one, this field specifies the Maximum Bulk OUT burst the core should do. When the system bus is slower than the USB, TX FIFO can underrun during a long burst. User can program a smaller value to this field to limit the TX burst size that the core can do. It only applies to SS Bulk, Isochronous, and Interrupt OUT endpoints in the host mode. Valid values are from 1 to 16
15:0	0h RO	Reserved.

22.3.4 Global Rx Threshold Control (GRXTHRCFG)—Offset C10Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 24400000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29	1h RW	**USB ReceivePacket Count Enable (USBRxPktCntSel):** This field enables/disables the USB reception multi-packet thresholding: n 0: The core can only start reception on the USB when the RX FIFO has space for at least one packet. n 1: The core can only start reception on the USB when the RX FIFO has space for at least USBRxPktCnt amount of packets. This mode is only valid in the host mode. It is only used for SuperSpeed.
28	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
27:24	4h RW	**USB Receive Packet Count (USBRxPktCnt):** This field specifies space (in number of packets) that must be available in the RX FIFO before the core can start the corresponding USB RX transaction (burst). This field is only valid when the USB Receive Packet Count Enable field is set to one. The valid values are from 1 to 15.
23:19	8h RW	**USB Maximum Rx Burst Size (USBMaxRxBurstSize):** This field is only valid when USBRxPktCntSel is one. This field specifies the Maximum Bulk IN burst the core should do. When the system bus is slower than the USB, RX FIFO can overrun during a long burst. User can program a smaller value to this field to limit the RX burst size that the core can do. It only applies to SS Bulk, Isochronous, and Interrupt IN endpoints in the host mode. Valid values are from 1 to 16.
18:0	0h RO	Reserved.

22.3.5 Global Core Control (GCTL)—Offset C110h

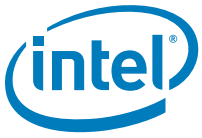
Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 2000h

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	Reserved.
18	0h RW	**Master Filter Bypass (MASTERFILTBYPASS):** When this bit is set to 1'b1, irrespective of the parameter DWC_USB3_EN_BUS_FILTERS chosen, all the filters in the DWC_usb3_filter module will be bypassed. The double synchronizers to mac_clk preceding the filters will also be bypassed. For enabling the filters, this bit should be 1'b0.
17	0h RO	Reserved.
16	0h RW	**U2RSTECN (U2RSTECN):** The super speed connection fails during POLL or LMP exchange, the device connects at non-SS mode. If this bit is set, then device attempts three more times to connect at SS, even if it previously failed to operate in SS mode.



Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RW	**FRMSCLDWN (FRMSCLDWN):** This field scales down device view of a SOF/USOF/ITP duration. For SS/ HS mode: 2'h3 implements interval to be 15. 625 us 2'h2 implements interval to be 31.25 us 2'h1 implements interval to be 62.5 us 2'h0 implements interval to be125us For FS mode, the scale-down value is multiplied by 8.
13:12	2h RW	**Port Capability Direction (PRTCAPDIR):** 2’b01: Reserved 2’b10: for Device configurations 2’b11: Reserved
11	0h RW	**Core Soft Reset (CORESOFTRESET):** 1b0 - No soft reset 1b1 - Soft reset
10:4	0h RO	Reserved.
3	0h RW	**Disable Scrambling (DISSCRAMBLE):** Transmit request to Link Partner on next transition to Recovery or Polling.
2	0h RO	Reserved.
1	0h RW	**Global Hibernation Enable (GblHibernationEn):** This bit enables hibernation at the global level. If hibernation is not enabled via this bit, the PMU immediately accepts the D0->D3 and D3->D0 power state change requests, but does not save or restore any core state. In addition, the PMUs will never drive the PHY interfaces and let the core continue to drive the PHY interfaces.
0	0h RW	**Disable Clock Gating (DSBLCLKGTNG):** When this bit is set to 1 and the core is in Low Power mode, internal clock gating is disabled. You can set this bit to 1’b1 after Power On Reset.

22.3.6 GPMSTS (GPMSTS)—Offset C114h

TBD

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h WO	**PortSel (PortSel)**
27:17	0h RO	Reserved.
16:12	0h RO	**U3Wakeup (U3Wakeup)**
11:10	0h RO	Reserved.
9:0	0h RO	**U2Wakeup (U2Wakeup)**

22.3.7 Global Status (GSTS)—Offset C118h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	Reserved.
6	0h RO	**Device Interrupt Pending (Device_IP):** This field indicates that there is a pending interrupt pertaining to peripheral (device) operation in the Device event queue
5	0h RO	**CSR Timeout (CSRTimeout):** When this bit is 1'b1, it indicates that software performed a write or read to a core register that could not be completed within bus clock cycles (default: 65535).
4	0h RO	**Bus Error Address Valid (BUSERRADDRVLD):** Indicates that the GBUSERRADDR register is valid and reports the first bus address that encounters a bus error.
3:2	0h RO	Reserved.
1:0	0h RO	**Current Mode of Operation (CURMOD):** Indicates the current mode of operation. 2’b00: Device mode 2’b01: Reserved

22.3.8 Bus Address Low (GBUSERRADDRLO)—Offset C130h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**Bus Address Low (BUSERRADDR):** This 64-bit register contains the lower 32 bits of the first bus address that encountered a SoC bus error. It is valid when the GSTS.BusErrAddrVld field is 1. It can only be cleared by resetting the core

22.3.9 Bus Address High (GBUSERRADDRHI)—Offset C134h

22.3.10 GHWPARAMS0 (GHWPARAMS0)—Offset C140h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 40204008h

Bit Range	Default & Access	Field Name (ID): Description
31:24	40h RO	**DWC_USB3_ADWIDTH_31_24 (DWC_USB3_ADWIDTH_31_24)**
23:16	20h RO	**DWC_USB3_SDWIDTH_23_16 (DWC_USB3_SDWIDTH_23_16)**
15:8	40h RO	**DWC_USB3_MDWIDTH_15_8 (DWC_USB3_MDWIDTH_15_8)**
7:6	0h RO	**DWC_USB3_SBUS_TYPE_7_6 (DWC_USB3_SBUS_TYPE_7_6)**
5:3	1h RO	**DWC_USB3_MBUS_TYPE_5_3 (DWC_USB3_MBUS_TYPE_5_3)**
2:0	0h RO	**DWC_USB3_MODE_2_0 (DWC_USB3_MODE_2_0)**

22.3.11 GHWPARAMS1 (GHWPARAMS1)—Offset C144h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 260C93Bh

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	Reserved.
26	0h RO	**DWC_USB3_MAC_PHY_CLKS_SYNC_26 (DWC_USB3_MAC_PHY_CLKS_SYNC_26)**
25:24	2h RO	**DWC_USB3_EN_PWROPT_25_24 (DWC_USB3_EN_PWROPT_25_24)**
23	0h RO	**DWC_USB3_SPRAM_TYP_23 (DWC_USB3_SPRAM_TYP_23)**
22:21	3h RO	**DWC_USB3_NUM_RAMS_22_21 (DWC_USB3_NUM_RAMS_22_21)**
20:15	1h RO	**DWC_USB3_DEVICE_NUM_INT_20_15 (DWC_USB3_DEVICE_NUM_INT_20_15)**
14:12	4h RO	**DWC_USB3_ASPACEWIDTH_14_12 (DWC_USB3_ASPACEWIDTH_14_12)**
11:9	4h RO	**DWC_USB3_REQINFOWIDTH_11_9 (DWC_USB3_REQINFOWIDTH_11_9)**
8:6	4h RO	**DWC_USB3_DATAINFOWIDTH_8_6 (DWC_USB3_DATAINFOWIDTH_8_6)**
5:3	7h RO	**DWC_USB3_BURSTWIDTH_5_3 (DWC_USB3_BURSTWIDTH_5_3)**
2:0	3h RO	**DWC_USB3_IDWIDTH_2_0 (DWC_USB3_IDWIDTH_2_0)**

22.3.12 GHWPARAMS2 (GHWPARAMS2)—Offset C148h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 8086A0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	8086A0h RO	**DWC_USB3_USERID_31_0 (DWC_USB3_USERID_31_0)**

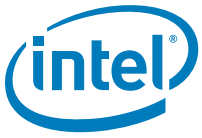
22.3.13 GHWPARAMS3 (GHWPARAMS3)—Offset C14Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 10420085h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	Reserved.
30:23	20h RO	**DWC_USB3_CACHE_TOTAL_XFER_RESOURCES_30_23 (DWC_USB3_CACHE_TOTAL_XFER_RESOURCES_30_23)**
22:18	10h RO	**DWC_USB3_NUM_IN_EPS_22_18 (DWC_USB3_NUM_IN_EPS_22_18)**
17:12	20h RO	**DWC_USB3_NUM_EPS_17_12 (DWC_USB3_NUM_EPS_17_12)**
11	0h RO	**DWC_USB3_ULPI_CARKIT_11 (DWC_USB3_ULPI_CARKIT_11)**
10	0h RO	**DWC_USB3_VENDOR_CTL_INTERFACE_10 (DWC_USB3_VENDOR_CTL_INTERFACE_10)**
9:8	0h RO	**ghwparams3_9_8 (ghwparams3_9_8)**
7:6	2h RO	**DWC_USB3_HSPHY_DWIDTH_7_6 (DWC_USB3_HSPHY_DWIDTH_7_6)**
5:4	0h RO	**DWC_USB3_FSPHY_INTERFACE_5_4 (DWC_USB3_FSPHY_INTERFACE_5_4)**
3:2	1h RO	**DWC_USB3_HSPHY_INTERFACE_3_2 (DWC_USB3_HSPHY_INTERFACE_3_2)**
1:0	1h RO	**DWC_USB3_SSPHY_INTERFACE_1_0 (DWC_USB3_SSPHY_INTERFACE_1_0)**

22.3.14 GHWPARAMS4 (GHWPARAMS4)—Offset C150h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 222004h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	Reserved.
21	1h RO	**DWC_USB3_EXT_BUFF_CONTROL_21 (DWC_USB3_EXT_BUFF_CONTROL_21)**
20:17	1h RO	**DWC_USB3_NUM_SS_USB_INSTANCES_20_17 (DWC_USB3_NUM_SS_USB_INSTANCES_20_17)**
16:13	1h RO	**DWC_USB3_HIBER_SCRATCHBUFS_16_13 (DWC_USB3_HIBER_SCRATCHBUFS_16_13):** Number of external scratchpad buffers the core requires to save its internal state in the device mode. Each buffer is assumed to be 4KB

Bit Range	Default & Access	Field Name (ID): Description
12	0h RO	**ghwparams4_12 (ghwparams4_12)**
11	0h RO	**ghwparams4_11 (ghwparams4_11)**
10:9	0h RO	**ghwparams4_10_9 (ghwparams4_10_9)**
8:7	0h RO	**ghwparams4_8_7 (ghwparams4_8_7)**
6	0h RO	**ghwparams4_6 (ghwparams4_6)**
5:0	4h RO	**DWC_USB3_CACHE_TRBS_PER_TRANSFER_5_0 (DWC_USB3_CACHE_TRBS_PER_TRANSFER_5_0)**

22.3.15 GHWPARAMS5 (GHWPARAMS5)—Offset C154h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 4202088h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	Reserved.
27:22	10h RO	**DWC_USB3_DFQ_FIFO_DEPTH_27_22 (DWC_USB3_DFQ_FIFO_DEPTH_27_22)**
21:16	20h RO	**DWC_USB3_DWQ_FIFO_DEPTH_21_16 (DWC_USB3_DWQ_FIFO_DEPTH_21_16)**
15:10	8h RO	**DWC_USB3_TXQ_FIFO_DEPTH_15_10 (DWC_USB3_TXQ_FIFO_DEPTH_15_10)**
9:4	8h RO	**DWC_USB3_RXQ_FIFO_DEPTH_9_4 (DWC_USB3_RXQ_FIFO_DEPTH_9_4)**
3:0	8h RO	**DWC_USB3_BMU_BUSGM_DEPTH_3_0 (DWC_USB3_BMU_BUSGM_DEPTH_3_0)**

22.3.16 GHWPARAMS6 (GHWPARAMS6)—Offset C158h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 2F60020h

Bit Range	Default & Access	Field Name (ID): Description
31:16	2F6h RO	**DWC_USB3_RAM0_DEPTH_31_16 (DWC_USB3_RAM0_DEPTH_31_16)**
15	0h RO	**BusFltrsSupport (BusFltrsSupport)**
14	0h RO	**BCSupport (BCSupport)**
13	0h RO	**OTG_SS_Support (OTG_SS_Support):** 1’b0: No 3.0 support 1’b1: 3.0 support
12	0h RO	**ADPSupport (ADPSupport)**
11	0h RO	**HNPSupport (HNPSupport)**
10	0h RO	**SRPSupport (SRPSupport):** The application uses this bit to determine the DWC_usb3 core’s SRP support. 1’b0: SRP support is not enabled 1’b1: SRP support is enabled
9:6	0h RO	Reserved.
5:0	20h RO	**DWC_USB3_PSQ_FIFO_DEPTH_5_0 (DWC_USB3_PSQ_FIFO_DEPTH_5_0)**

22.3.17 GHWPARAMS7 (GHWPARAMS7)—Offset C15Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 38507E6h

Bit Range	Default & Access	Field Name (ID): Description
31:16	385h RO	**DWC_USB3_RAM2_DEPTH_31_16 (DWC_USB3_RAM2_DEPTH_31_16)**
15:0	7E6h RO	**DWC_USB3_RAM1_DEPTH_15_0 (DWC_USB3_RAM1_DEPTH_15_0)**

22.3.18 GDBGFIFOSPACE (GDBGFIFOSPACE)—Offset C160h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 420000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	42h RO	**SPACE_AVAILABLE (SPACE_AVAILABLE)**
15:9	0h RO	Reserved.
8:0	0h RW	**FIFO_QUEUE_SELECT (FIFO_QUEUE_SELECT):** [8:5] indicates the FIFO/Queue Type [4:0] indicates the FIFO/Queue Number

22.3.19 GDBGLTSSM (GDBGLTSSM)—Offset C164h

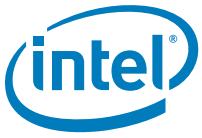
Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 41010440h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	Reserved.
30	1h RO	**RxElecidle (RxElecidle)**
29	0h RO	**X3_XS_SWAPPING (X3_XS_SWAPPING)**
28	0h RO	**X3_DS_HOST_SHUTDOWN (X3_DS_HOST_SHUTDOWN)**
27	0h RO	**PRTDIRECTION (PRTDIRECTION):** 1'b0: Upstream 1'b1: Downstream
26	0h RO	**LTDBTIMEOUT (LTDBTIMEOUT)**
25:22	4h RO	**LTDBLINKSTATE (LTDBLINKSTATE)**
21:18	0h RO	**LTDBSUBSTATE (LTDBSUBSTATE)**
17	0h RO	**ELASTICBUFFERMODE (ELASTICBUFFERMODE)**
16	1h RO	**TXELECLDLE (TXELECLDLE)**
15	0h RO	**RXPOLARITY (RXPOLARITY)**
14	0h RO	**TxDetRxLoopback (TxDetRxLoopback)**



Bit Range	Default & Access	Field Name (ID): Description
13:11	0h RO	**LTDBPhyCmdState (LTDBPhyCmdState):** 000: PHY_IDLE 001: PHY_DET 010: PHY_DET_3 011: PHY_PWR_DLY 100: PHY_PWR_A 101: PHY_PWR_B
10:9	2h RO	**POWERDOWN (POWERDOWN)**
8	0h RO	**RXEQTRAIN (RXEQTRAIN)**
7:6	1h RO	**TXDEEMPHASIS (TXDEEMPHASIS)**
5:3	0h RO	**LTDBClkState (LTDBClkState):** 000: CLK_NORM 001: CLK_TO_P3 010: CLK_WAIT1 011: CLK_P3 100: CLK_TO_P0 101: CLK_WAIT2
2	0h RO	**TXSWING (TXSWING)**
1	0h RO	**RXTERMINATION (RXTERMINATION)**
0	0h RO	**TXONESZEROS (TXONESZEROS)**

22.3.20 GDBGLNMCC (GDBGLNMCC)—Offset C168h

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8:0	0h RO	**LNMCC_BERC (LNMCC_BERC)**

22.3.21 GDBGBMU (GDBGBMU)—Offset C16Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**BMU_BCU (BMU_BCU)**
7:4	0h RO	**BMU_DCU (BMU_DCU)**
3:0	0h RO	**BMU_CCU (BMU_CCU)**

22.3.22 GDBGLSP (GDBGLSP)—Offset C174h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**LSPDEBUG (LSPDEBUG)**

22.3.23 GDBGEPINFO0 (GDBGEPINFO0)—Offset C178h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**EPDEBUG (EPDEBUG)**

22.3.24 GDBGEPINFO1 (GDBGEPINFO1)—Offset C17Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 800000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	800000h RO	**EPDEBUG (EPDEBUG)**

22.3.25 Global Transmit FIFO Size Register N (GTXFIFOSIZ0_0)—Offset C300h

FIFO_number: 0<= n <= 15
Offset: C300h + FIFO_number * 04h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 42h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**TXFSTADDR_N (TXFSTADDR_N)**
15:0	42h RW	**TXFDEP_N (TXFDEP_N)**

22.3.26 GRXFIFOSIZ0_0 (GRXFIFOSIZ0_0)—Offset C380h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 385h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**RXFSTADDR_N (RXFSTADDR_N)**
15:0	385h RW	**RXFDEP_N (RXFDEP_N)**

22.3.27 GEVNTADRLO_0 (GEVNTADRLO_0)—Offset C400h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**EVNTADRLO (EVNTADRLO)**

22.3.28 GEVNTADRHI_0 (GEVNTADRHI_0)—Offset C404h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**EVNTADRHI (EVNTADRHI)**

22.3.29 GEVNTCOUNT_0 (GEVNTCOUNT_0)—Offset C40Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	0h NA	**EVNTCOUNT (EVNTCOUNT)**

22.3.30 GTXFIFOPRIDEV (GTXFIFOPRIDEV)—Offset C610h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	0h RW	**gtxfifopridev (gtxfifopridev)**

§ §

23 Thermal Subsystem (D20: F2)

23.1 Thermal Reporting Configuration Registers Summary

Table 23-1. Summary of Thermal Reporting Configuration Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	1h	Vendor Identification (VID)—Offset 0h	8086h
2h	3h	Device Identification (DID)—Offset 2h	See register
4h	5h	Command (CMD)—Offset 4h	0h
6h	7h	Status (STS)—Offset 6h	10h
8h	8h	Revision Identification (RID)—Offset 8h	See register
9h	9h	Programming Interface (PI)—Offset 9h	0h
Ah	Ah	Sub Class Code (SCC)—Offset Ah	80h
Bh	Bh	Base Class Code (BCC)—Offset Bh	11h
Ch	Ch	Cache Line Size (CLS)—Offset Ch	0h
Dh	Dh	Latency Timer (LT)—Offset Dh	0h
Eh	Eh	Header Type (HTYPE)—Offset Eh	0h
10h	13h	Thermal Base (TBAR)—Offset 10h	4h
14h	17h	Thermal Base High DWord (TBARH)—Offset 14h	0h
2Ch	2Dh	Subsystem Vendor ID (SVID)—Offset 2Ch	0h
2Eh	2Fh	Subsystem ID (SID)—Offset 2Eh	0h
34h	37h	Capabilities Pointer (CAP_PTR)—Offset 34h	50h
3Ch	3Ch	Interrupt Line (INTLN)—Offset 3Ch	0h
3Dh	3Dh	Interrupt Pin (INTPN)—Offset 3Dh	0h
40h	43h	BIOS Assigned Thermal Base Address (TBARB)—Offset 40h	4h
44h	47h	BIOS Assigned Thermal Base High DWord (TBARBH)—Offset 44h	0h
48h	48h	Control Bits (CB)—Offset 48h	0h
50h	51h	PCI Power Management Capability ID (PID)—Offset 50h	8001h
52h	53h	Power Management Capabilities (PC)—Offset 52h	23h
54h	57h	Power Management Control And Status (PCS)—Offset 54h	8h
80h	81h	Message Signaled Interrupt Identifiers (MID)—Offset 80h	5h
82h	83h	Message Signaled Interrupt Message Control (MC)—Offset 82h	0h
84h	87h	Message Signaled Interrupt Message Address (MA)—Offset 84h	0h
88h	8Bh	Message Signaled Interrupt Message Data (MD)—Offset 88h	0h

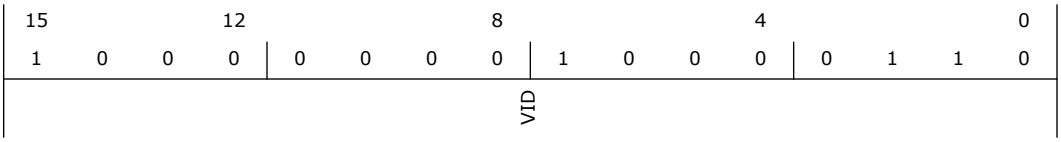
23.1.1 Vendor Identification (VID)—Offset 0h

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 20
Function: 2

Default: 8086h



Bit Range	Default & Access	Field Name (ID): Description
15:0	8086h RO	**Vendor ID (VID):** Indicates that Intel is the vendor.

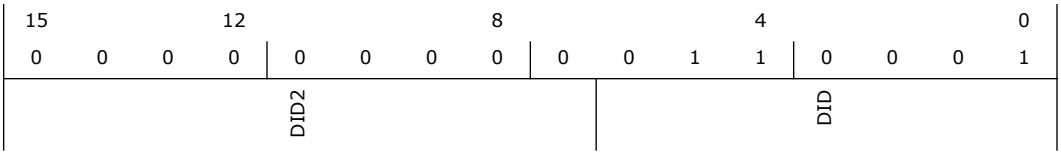
23.1.2 Device Identification (DID)—Offset 2h

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 20
Function: 2

Default: See register



Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RO	**Device ID (DID):** Indicates the device number See the Device and Version ID Table in Volume 1 for the default value.

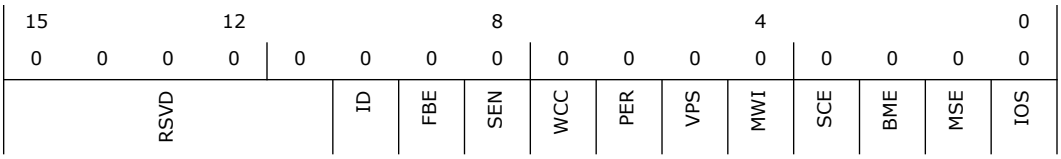
23.1.3 Command (CMD)—Offset 4h

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 20
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:11	0h RO	Reserved.
10	0h RW	**Interrupt Disable (ID):** Enables the device to assert an INTx#. When set, the Thermal logics INTx# signal will be de-asserted. When cleared AND MSI is not enabled, the INTx# signal may be asserted. NOTE: this bit has no affect on MSI generation.
9	0h RO	**Fast Back to Back Enable (FBE):** Not implemented. Hardwired to 0.
8	0h RW	**SERR Enable (SEN):** When set to 1 and an error occurs, SERR# is signaled to the system.
7	0h RO	**Wait Cycle Control (WCC):** Not implemented. Hardwired to 0.
6	0h RO	**Parity Error Response (PER):** Not implemented. Hardwired to 0.
5	0h RO	**VGA Palette Snoop (VPS):** Not implemented. Hardwired to 0.
4	0h RO	**Memory Write and Invalidate Enable (MWI):** Not implemented. Hardwired to 0.
3	0h RO	**Special Cycle Enable (SCE):** Not implemented. Hardwired to 0.
2	0h RW	**Bus Master Enable (BME):** When 1, enables
1	0h RW	**Memory Space Enable (MSE):** When set, enables memory space accesses to the Thermal registers.
0	0h RO	**I/O Space (IOS):** The Thermal logic does not implement IO Space, therefore this bit is hardwired to 0.

23.1.4 Status (STS)—Offset 6h

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 20
Function: 2

Default: 10h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
DPE	SERRS	RMA	RTA	STA	DEVT		MDPE	FBC	RSVD	C66	CLIST	IS	RSVD		

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Detected Parity Error (DPE):** This bit is set whenever a parity error is seen on the internal interface for this function, regardless of the setting of bit 6 in the command register. Software clears this bit by writing a '1' to this bit location. The thermal sensor unit never checks parity.
14	0h RW/1C	**SERR# Status (SERRS):** Not implemented. Hardwired to 0.
13	0h RO	**Received Master Abort (RMA):** Not implemented. Hardwired to 0.
12	0h RO	**Received Target Abort (RTA):** Not implemented. Hardwired to 0.
11	0h RW/1C	**Signaled Target-Abort (STA):** May be asserted on errors
10:9	0h RO	**DEVSEL# Timing Status (DEVT):** Does not apply. Hardwired to 0.
8	0h RO	**Master Data Parity Error (MDPE):** Not implemented. Hardwired to 0.
7	0h RO	**Fast Back to Back Capable (FBC):** Does not apply. Hardwired to 0.
6	0h RO	Reserved.
5	0h RO	**66 MHz Capable (C66):** Does not apply. Hardwired to 0.
4	1h RO	**Capabilities List Exists (CLIST):** Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h.
3	0h RO	**Interrupt Status (IS):** Reflects the state of the INTx# signal at the input of the enable/disable circuit. This bit is a 1 when the INTx# is asserted. This bit is a 0 after the interrupt is cleared (independent of the state of the Interrupt Disable bit in the command register). This bit is not set if MSI is enabled.
2:0	0h RO	Reserved.

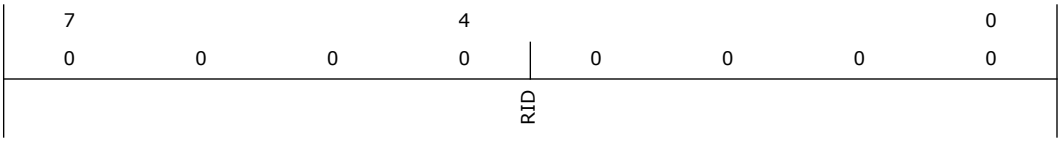
23.1.5 Revision Identification (RID)—Offset 8h

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 20
Function: 2

Default: See register



Bit Range	Default & Access	Field Name (ID): Description
7:0	-- RO/V	**Revision ID (RID):** Indicates the device specific revision identifier. See the Device and Version ID Table in Volume 1 for the default value.

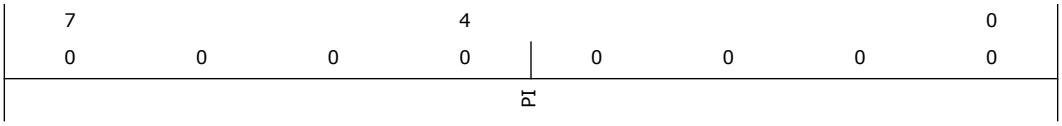
23.1.6 Programming Interface (PI)—Offset 9h

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 20
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RO	**Programming Interface (PI):** PCH Thermal logic has no standard programming interface.

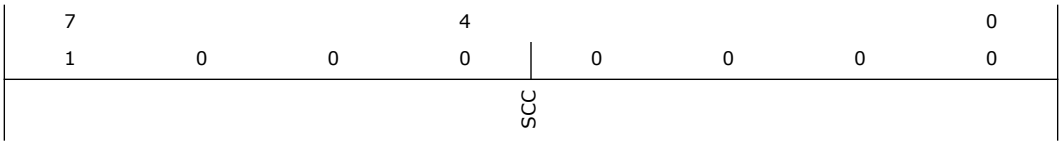
23.1.7 Sub Class Code (SCC)—Offset Ah

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 20
Function: 2

Default: 80h



Bit Range	Default & Access	Field Name (ID): Description
7:0	80h RO	**Sub Class Code (SCC):** Value assigned to PCH Thermal logic.

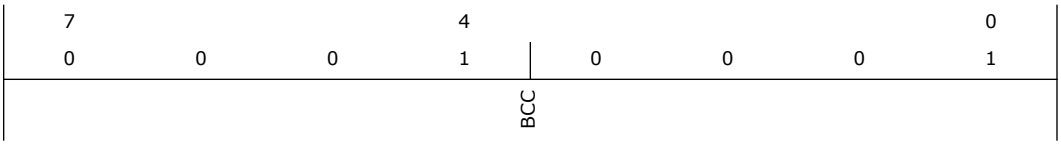
23.1.8 Base Class Code (BCC)—Offset Bh

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 20
Function: 2

Default: 11h



Bit Range	Default & Access	Field Name (ID): Description
7:0	11h RO	**Base Class Code (BCC):** Value assigned to PCH Thermal logic.

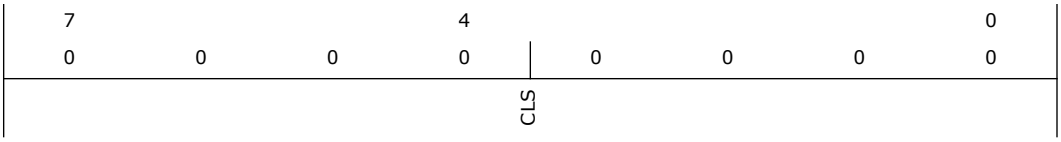
23.1.9 Cache Line Size (CLS)—Offset Ch

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 20
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RO	**Cache Line Size (CLS):** Doesn't apply to PCI Bus Target-only devices.

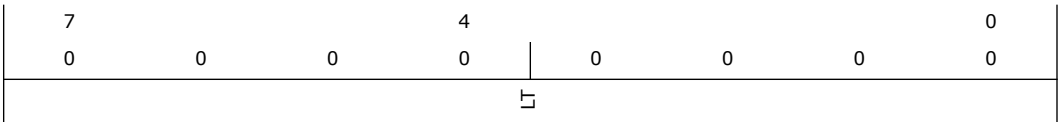
23.1.10 Latency Timer (LT)—Offset Dh

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 20
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RO	**Latency Timer (LT):** Doesn't apply to PCI Bus Target-only devices.

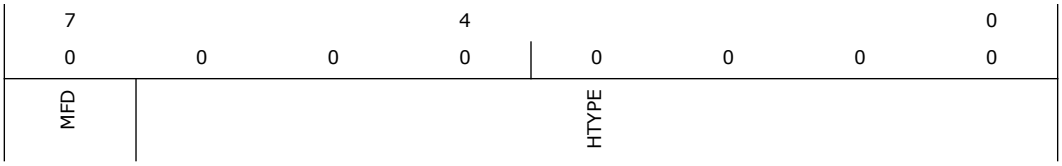
23.1.11 Header Type (HTYPE)—Offset Eh

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 20
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Multi-Function Device (MFD):** This bit is '0' because a multi-function device only needs to be marked as such in Function 0, and the Thermal registers are not in Function 0.
6:0	0h RO	**Header Type (HTYPE):** Implements Type 0 Configuration header.

23.1.12 Thermal Base (TBAR)—Offset 10h

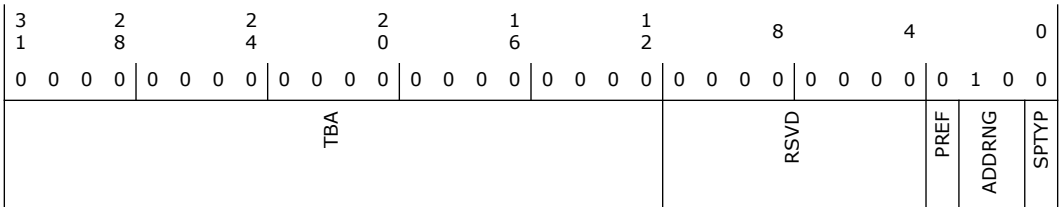
This BAR creates 4K bytes of memory space to signify the base address of Thermal memory mapped configuration registers. This memory space is active when the Command (CMD) register Memory Space Enable (MSE) bit is set and either TBAR[31:12] or TBARH are programmed to a non-zero address. This BAR is owned by the Operating System, and allows the OS to locate the Thermal registers in system memory space.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 2

Default: 4h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW	**Thermal Base Address (TBA):** Base address for the Thermal logic memory mapped configuration registers. 4KB bytes are requested by hardwiring bits 11:4 to 0's.
11:4	0h RO	Reserved.
3	0h RO	**Prefetchable (PREF):** Indicates that this BAR is NOT pre-fetchable.
2:1	2h RO	**Address Range (ADDRNG):** Indicates that this BAR can be located anywhere in 64 bit address space.
0	0h RO	**Space Type (SPTYP):** Indicates that this BAR is located in memory space.

23.1.13 Thermal Base High DWord (TBARH)—Offset 14h

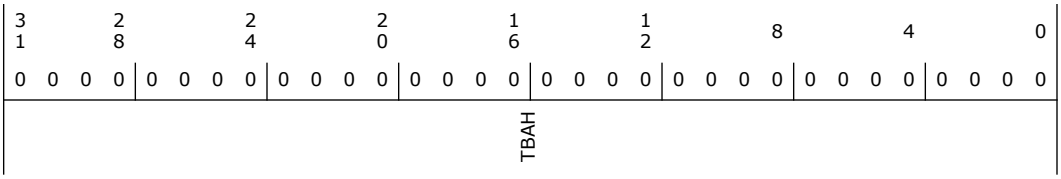
This BAR extension holds the high 32 bits of the 64 bit TBAR. In conjunction with TBAR, it creates 4 KB of memory space to signify the base address of Thermal memory mapped configuration registers.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Thermal Base Address High (TBAH):** TBAR bits 61:32.

23.1.14 Subsystem Vendor ID (SVID)—Offset 2Ch

This register should be implemented for any function that could be instantiated more than once in a given system,. The SVID register, in combination with the Subsystem ID register, enables the operating environment to distinguish one subsystem from the other(s).
Software (BIOS) will write the value to this register. After that, the value can be read, but writes to the register will have no effect. The write to this register should be combined with the write to the SID to create one 32-bit write. This register is not affected by D3HOT to D0 reset.

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 20
Function: 2

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW/O	**SVID (SVID):** These RWO bits have no PCH functionality.

23.1.15 Subsystem ID (SID)—Offset 2Eh

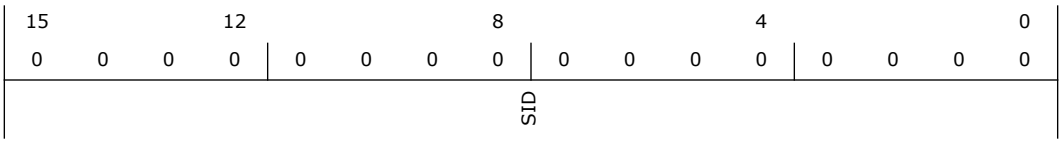
This register should be implemented for any function that could be instantiated more than once in a given system,. The SID register, in combination with the Subsystem Vendor ID register make it possible for the operating environment to distinguish one subsystem from the other(s).
Software (BIOS) will write the value to this register. After that, the value can be read, but writes to the register will have no effect. The write to this register should be combined with the write to the SVID to create one 32-bit write. This register is not affected by D3HOT to D0 reset.

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 20
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW/O	**SID (SID):** These RWO bits have no PCH functionality.

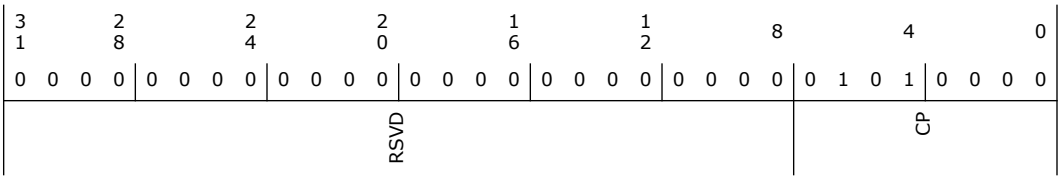
23.1.16 Capabilities Pointer (CAP_PTR)—Offset 34h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 2

Default: 50h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	50h RO	**Capability Pointer (CP):** Indicates that the first capability pointer offset is offset 50h (Power Management Capability).

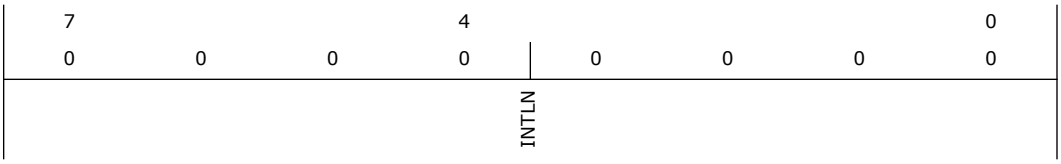
23.1.17 Interrupt Line (INTLN)—Offset 3Ch

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 20
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**Interrupt Line (INTLN):** PCH hardware does not use this field directly. It is used to communicate to software the interrupt line that the interrupt pin is connected to.

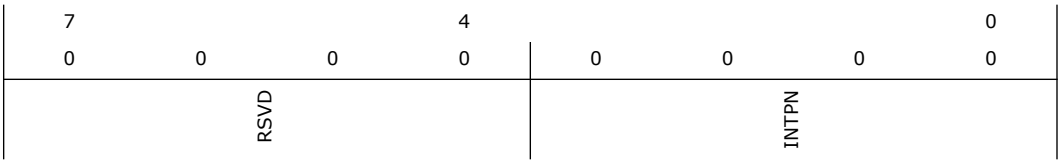
23.1.18 Interrupt Pin (INTPN)—Offset 3Dh

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 20
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7:4	0h RO	Reserved.
3:0	0h RW/O	**Interrupt Pin (INTPN):** This reflects the value of interrupt pin used by this device.

23.1.19 BIOS Assigned Thermal Base Address (TBARB)—Offset 40h

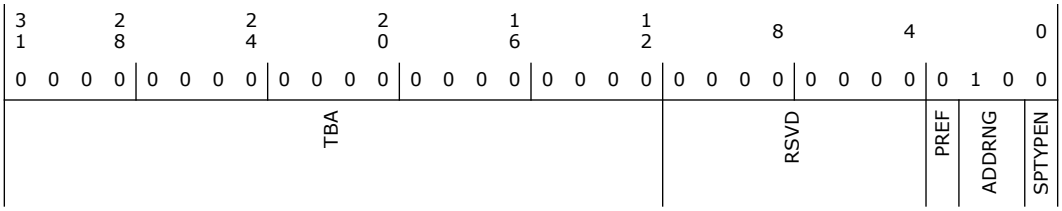
This BAR creates 4K bytes of memory space to signify the base address of Thermal memory mapped configuration registers. This memory space is active when TBARB.SPTYPEN is asserted. This BAR is owned by the BIOS, and allows the BIOS to locate the Thermal registers in system memory space. If both TBAR and TBARB are programmed, then the OS and BIOS each have their own independent view of the Thermal registers, and must use the TSIU, TCIU, and TBIU registers to denote Thermal registers ownership/availability. CONTRADICTS EARLY BLUE STATEMENT

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 2

Default: 4h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW	**Thermal Base Address (TBA):** Base address for the Thermal logic memory mapped configuration registers. 4KB bytes are requested by hardwiring bits 11:4 to 0's.
11:4	0h RO	Reserved.
3	0h RO	**Prefetchable (PREF):** Indicates that this BAR is NOT pre-fetchable.
2:1	2h RO	**Address Range (ADDRNG):** Indicates that this BAR can be located anywhere in 64 bit address space.
0	0h RW	**Space Type Enable (SPTYPEN):** When set to 1b by software, enables the decode of this memory BAR.

23.1.20 BIOS Assigned Thermal Base High DWord (TBARBH)—Offset 44h

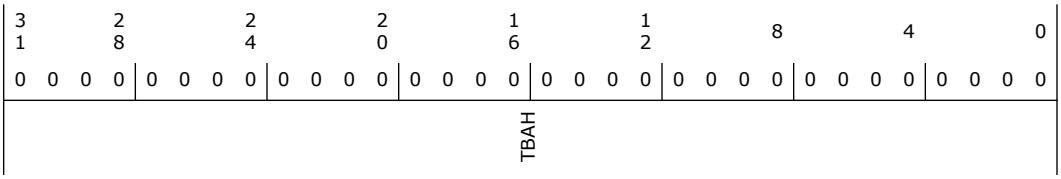
This BAR extension holds the high 32 bits of the 64 bit TBARB.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Thermal Base Address High (TBAH):** TBAR bits 61:32.

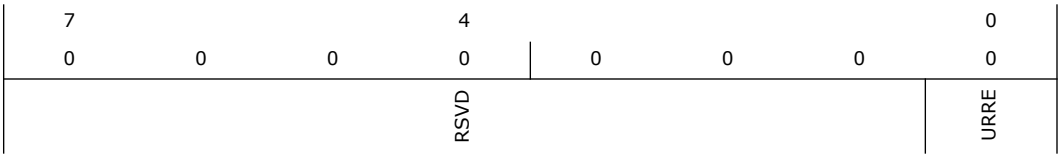
23.1.21 Control Bits (CB)—Offset 48h

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 20
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7:1	0h RO	Reserved.
0	0h RW	**UR Reporting Enable (URRE):** When '1', the agent will set the URD bit. If SERR# enable (SEN) is set, then the agent will also send SERR# to the system. Note that both URRE and SEN must be set to generate an SERR#.

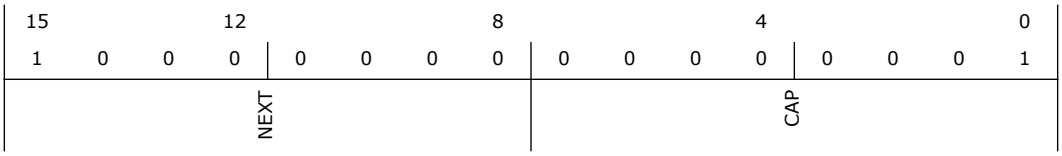
23.1.22 PCI Power Management Capability ID (PID)—Offset 50h

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 20
Function: 2

Default: 8001h



Bit Range	Default & Access	Field Name (ID): Description
15:8	80h RO	**Next Capability (NEXT):** Indicates that the next capability is MSI.
7:0	1h RO	**Cap ID (CAP):** Indicates that this pointer is a PCI power management capability

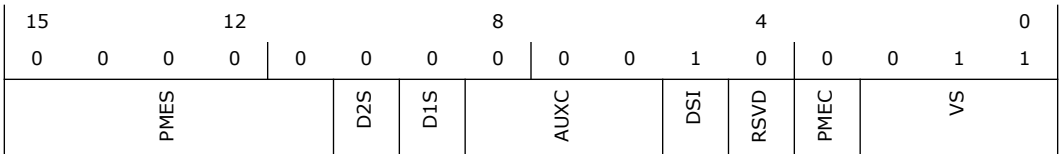
23.1.23 Power Management Capabilities (PC)—Offset 52h

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 20
Function: 2

Default: 23h



Bit Range	Default & Access	Field Name (ID): Description
15:11	0h RO	**PME_Support (PMES):** Indicates PME# is not supported
10	0h RO	**D2_Support (D2S):** The D2 state is not supported.
9	0h RO	**D1_Support (D1S):** The D1 state is not supported.
8:6	0h RO	**Aux_Current (AUXC):** PME# from D3COLD state is not supported, therefore this field is 000b..
5	1h RO	**Device Specific Initialization (DSI):** Indicates that device-specific initialization is required.
4	0h RO	Reserved.
3	0h RO	**PME Clock (PMEC):** Does not apply. Hardwired to 0.
2:0	3h RO	**Version (VS):** Indicates support for Revision 1.2 of the PCI Power Management Specification.

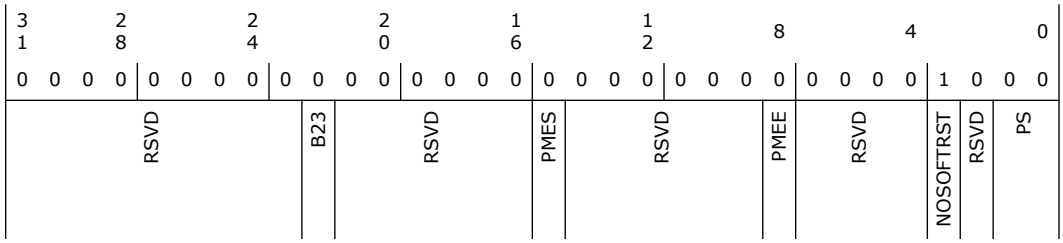
23.1.24 Power Management Control And Status (PCS)—Offset 54h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 2

Default: 8h



Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	Reserved.
22	0h RO	**B2/B3 Support (B23):** Does not apply. Hardwired to 0.
21:16	0h RO	Reserved.
15	0h RO	**PME Status (PMES):** This bit is always zero, since this PCI Function does not generate PME#
14:9	0h RO	Reserved.
8	0h RO	**PME Enable (PMEE):** This bit is always zero, since this PCI Function does not generate PME#
7:4	0h RO	Reserved.
3	1h RO	**No Soft Reset (NOSOFTRST):**), this bit indicates that devices transitioning from D3HOT to D0 becuase of PowerState commands do not perform an internal reset. Configuration context is preserved. Upon transition from D3HOT to D0 initialized state, no additional operating system intervention is required to preserve Configuration Context beyong writing the PowerState bits.
2	0h RO	Reserved.
1:0	0h RW	**Power State (PS):** This field is used both to determine the current power state of the Thermal controller and to set a new power state. The values are: 00 = D0 state 11 = D3HOT state If software attempts to write a value of 10b or 01b in to this field, the write operation must complete normally, however, the data is discarded and no state change occurs. When in the D3HOT states, the Thermal controller's configuration space is available, but the I/O and memory spaces are not. Additionally, interrupts are blocked. When software changes this value from the D3 HOT state to the D0 state, no internal warm (soft) reset is generated.

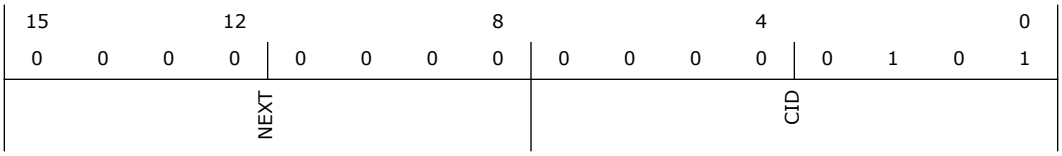
23.1.25 Message Signaled Interrupt Identifiers (MID)—Offset 80h

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 20
Function: 2

Default: 5h



Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Next Pointer (NEXT):** Indicates this is the latst pointer
7:0	5h RO	**Capability ID (CID):** Capabilities ID indicates MSI.

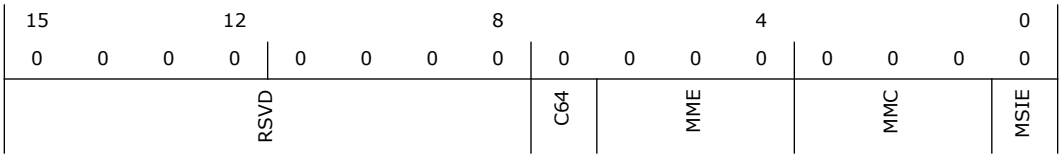
23.1.26 Message Signaled Interrupt Message Control (MC)—Offset 82h

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 20
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	Reserved.
7	0h RO	**64 Bit Address Capable (C64):** Capable of generating a 32-bit message only.
6:4	0h RW	**Multiple Message Enable (MME):** These bits are RW for software compatibility, but only one message is ever sent by the root port.
3:1	0h RO	**Multiple Message Capable (MMC):** Only one message is required.
0	0h RW	**MSI Enable (MSIE):** If set, MSI is enabled and traditional interrupt pins are not used to generate interrupts. CMD.BME must be set for an MSI to be generated. If CMD.BME is cleared, and this bit is set, no interrupts (not even pin based) are generated.

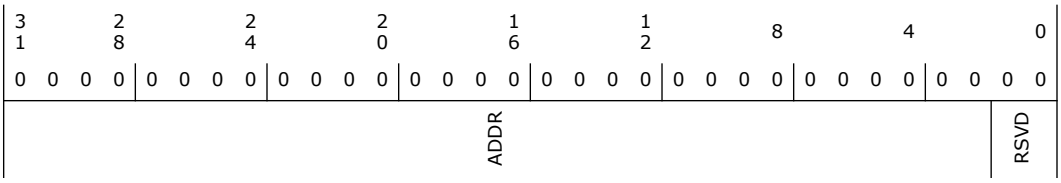
23.1.27 Message Signaled Interrupt Message Address (MA)—Offset 84h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**Address (ADDR):** Lower 32 bits of the system specified message address, always DW aligned.
1:0	0h RO	Reserved.

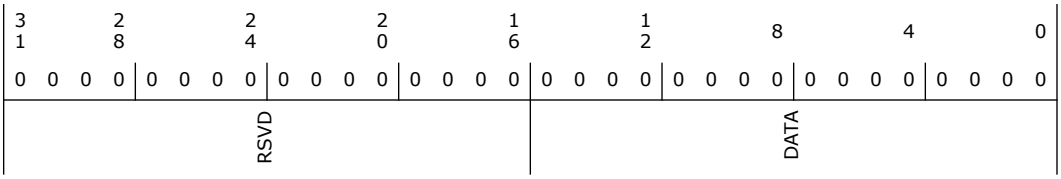
23.1.28 Message Signaled Interrupt Message Data (MD)—Offset 88h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	0h RW	**Data (DATA):** This 16-bit field is programmed by system software if MSI is enabled. Its content is driven onto the lower word (PCI AD[15:0]) during the data phase of the MSI memory write transaction.

23.2 Thermal Reporting Memory Mapped Registers Summary

The Thermal Reporting Registers are located in the Memory Space mapped by TBAR (OS) and/or TBARB (BIOS), in the offset range from 0h to 0FFh.
All registers are reset by PLTRST#.

Table 23-2. Summary of Thermal Reporting Memory Mapped Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	1h	Temperature (TEMP)—Offset 0h	0h
4h	4h	Thermal Sensor Control (TSC)—Offset 4h	0h
6h	6h	Thermal Sensor Status (TSS)—Offset 6h	0h
8h	8h	Thermal Sensor Enable and Lock (TSEL)—Offset 8h	0h
Ah	Ah	Thermal Sensor Reporting Enable and Lock (TSREL)—Offset Ah	0h
Ch	Ch	Thermal Sensor SMI Control (TSMIC)—Offset Ch	0h
10h	11h	Catastrophic Trip Point (CTT)—Offset 10h	1FFh
14h	15h	Thermal Alert High Value (TAHV)—Offset 14h	0h
18h	19h	Thermal Alert Low Value (TALV)—Offset 18h	0h
1Ch	1Dh	Thermal Sensor Power Management (TSPM)—Offset 1Ch	800h
40h	43h	Throttle Levels (TL)—Offset 40h	0h
50h	53h	Throttle Level 2 (TL2)—Offset 50h	0h
60h	61h	PCH Hot Level (PHL)—Offset 60h	0h
62h	62h	PHL Control (PHLC)—Offset 62h	0h
80h	80h	Thermal Alert Status (TAS)—Offset 80h	0h
82h	82h	PCI Interrupt Event Enables (TSPIEN)—Offset 82h	0h
84h	84h	General Purpose Event Enables (TSGPEN)—Offset 84h	0h
F0h	F0h	Thernak Controller Function Disable (TCFD)—Offset F0h	0h

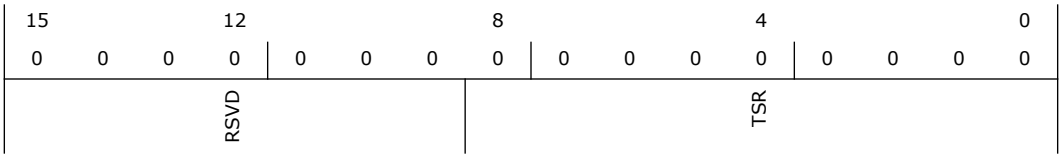
23.2.1 Temperature (TEMP)—Offset 0h

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 20
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:9	0h RO	Reserved.
8:0	0h RO	**TS Reading (TSR):** The die temperature with resolution of degree C and an offset of -50C. Thus a reading of 0x121 is 94.5C.

23.2.2 Thermal Sensor Control (TSC)—Offset 4h

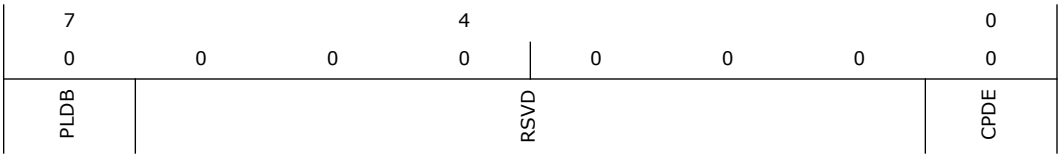
This register controls the operation of the thermal sensor.

Access Method

Type: MEM Register
(Size: 8 bits)

Device: 20
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7	0h RW/O/L	**Policy Lock-Down Bit (PLDB):** When written to 1, this bit prevents any more writes to this register (offset 04h) and to CTT (offset 0x10)
6:1	0h RO	Reserved.
0	0h RW/L	**Catastrophic Power-Down Enable (CPDE):** When set to 1, the power management logic (PMC) transitions to the S5 state when a catastrophic temperature is detected by the sensor. The transition to the S5 state must be unconditional (like the Power Button Override Function). Note that the thermal sensor and response logic is in the core/main power well, therefore, detection of a catastrophic temperature is limited to times when this well is powered and out of reset.

23.2.3 Thermal Sensor Status (TSS)—Offset 6h

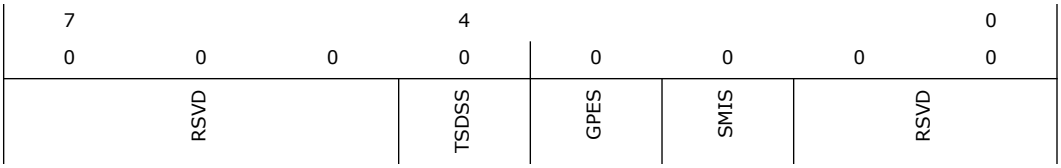
This read only register provides trip point and other status of the thermal sensor.

Access Method

Type: MEM Register
(Size: 8 bits)

Device: 20
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7:5	0h RO	Reserved.
4	0h RO	**Thermal Sensor Dynamic Shutdown Status (TSDSS):** Thermal Sensor Dynamic Shutdown Status (TSDSS): This bit indicates the status of the thermal sensor circuit when TSEL.ETS=1. 1: thermal sensor is fully operational 0: thermal sensor is in a dynamic shutdown state
3	0h RW/1C	**GPE Status (GPES):** Set when GPE is enabled for a trip event. SW must write a 1 to this bit to clear the GPE status. Note that GPE can be configured to cause an SMI or SCI. As long as this bit is set, the GPE indication to the global GPE logic is asserted..
2	0h RW/1C	**SMI Status (SMIS):** Set when SMI is enabled for a trip event. SW must write a 1 to this bit to clear the SMI status. As long as this bit is set, the SMI indication to the global SMI logic is asserted.
1:0	0h RO	Reserved.

23.2.4 Thermal Sensor Enable and Lock (TSEL)—Offset 8h

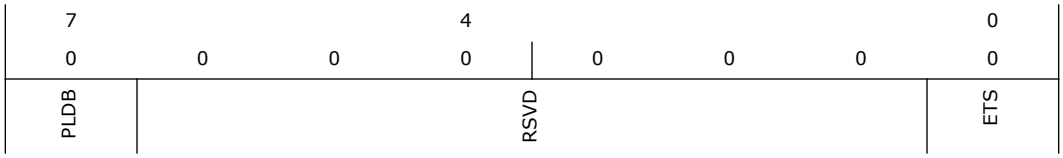
This register controls the operation of the thermal sensor.

Access Method

Type: MEM Register
(Size: 8 bits)

Device: 20
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7	0h RW/O/L	**Policy Lock-Down Bit (PLDB):** Policy Lock-Down Bit: When written to 1, this bit prevents any more writes to this register and to TTCB, Test1, Test2, Test3, Test4, Test5, Test6 and Test7 registers.
6:1	0h RO	Reserved.
0	0h RW/L	**Enable TS (ETS):** 1: Enables the thermal sensor. Until this bit is set, no thermometer readings or trip events will occur. If SW reads the TEMP register before the sensor is enabled, it will read 0x0. The value of this bit is sent to the thermal sensor. NOTE: if the sensor is running and valid temperatures have been captured in TEMP and then ETS is cleared, TEMP will retain its old value. Clearing ETS does not force TEMP to 0x00. 0: Disables the sensor.

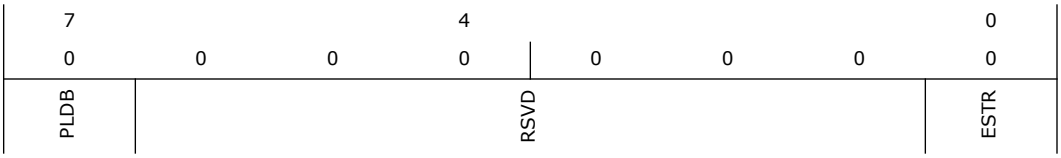
23.2.5 Thermal Sensor Reporting Enable and Lock (TSREL)—Offset Ah

Access Method

Type: MEM Register
(Size: 8 bits)

Device: 20
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7	0h RW/O/L	**Policy Lock-Down Bit (PLDB):** Policy Lock-Down Bit: When written to 1, this bit prevents any more writes to this register (offset 0Ah)
6:1	0h RO	Reserved.
0	0h RW/L	**Enable SMBus Temperature Reporting (ESTR):** 1: Enables the reporting of the PCH temperature to the SMBus. Note that this must also be set if ME needs access to the PCH temperature. Once enabled this bit should not be cleared by SW. If it is cleared then the EC may get an undefined value. SW has no need to dynamically disable and then re-enable this bit. 0: Disables EC temperature reporting.

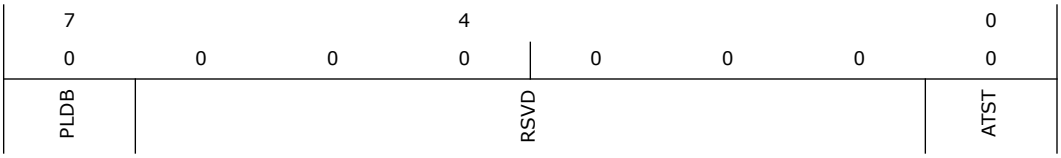
23.2.6 Thermal Sensor SMI Control (TSMIC)—Offset Ch

Access Method

Type: MEM Register
(Size: 8 bits)

Device: 20
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7	0h RW/O/L	**Policy Lock-Down Bit (PLDB):** When written to 1, this bit prevents any more writes to this register (offset 0Ch)
6:1	0h RO	Reserved.
0	0h RW/L	**SMI Enable on Alert Thermal Sensor Trip (ATST):** 1: Enables SMI# assertions on alert thermal sensor events for either low-to-high or high-to-low events. (Both edges are enabled by this one bit.) 0: Disables SMI# assertions for alert thermal events

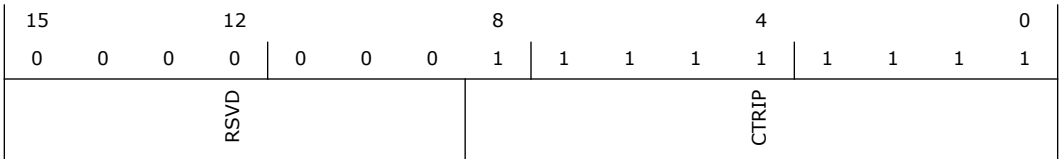
23.2.7 Catastrophic Trip Point (CTT)—Offset 10h

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 20
Function: 2

Default: 1FFh



Bit Range	Default & Access	Field Name (ID): Description
15:9	0h RO	Reserved.
8:0	1FFh RW/L	**Catastrophic Temperature TRIP (CTRIP):** When the current temperature reading is = to the value in this register, a catastrophic trip event is signaled. The value of this register must not be changed while TSEL.ETS is set. The value in this register is sent to the thermal sensor. This register is locked by TSC[7]

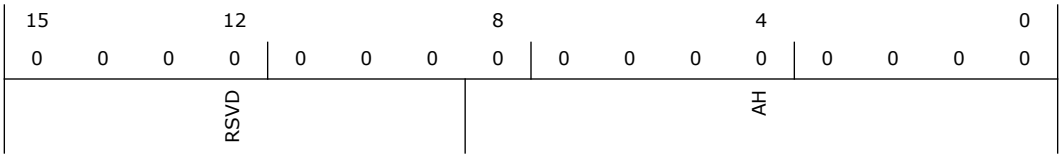
23.2.8 Thermal Alert High Value (TAHV)—Offset 14h

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 20
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:9	0h RO	Reserved.
8:0	0h RW	**Alert High (AH):** Alert High (AH) - Sets the high value for the alert indication. See the later section for usage. The value of this register must not be changed while TSEL.ETS is set. The value in this register is sent to the thermal sensor. This register is not lockable, so that SW can change the values during runtime.

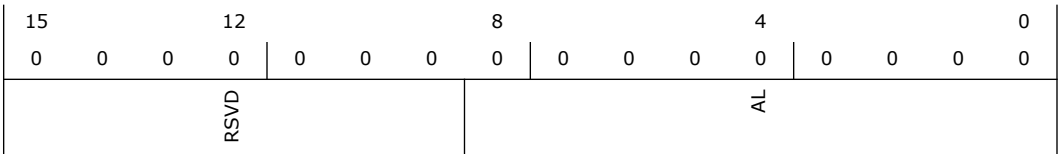
23.2.9 Thermal Alert Low Value (TALV)—Offset 18h

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 20
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:9	0h RO	Reserved.
8:0	0h RW	**Alert Low (AL):** Sets the low value for the alert indication. See the later section for usage. The value of this register must not be changed while TSEL.ETS is set. The value in this register is sent to the thermal sensor. This register is not lockable, so that SW can change the values during runtime.

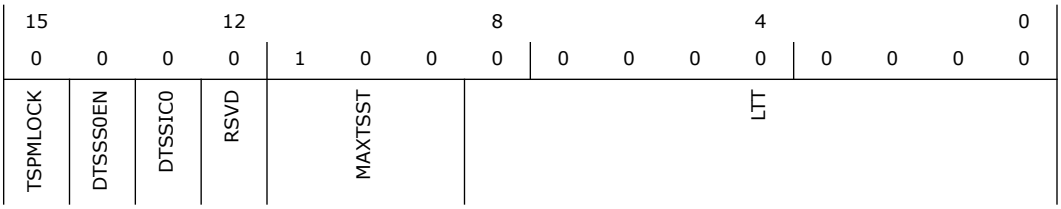
23.2.10 Thermal Sensor Power Management (TSPM)—Offset 1Ch

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 20
Function: 2

Default: 800h



Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/L	**Thermal Sensor Power Management Lock (TSPMLOCK):** Thermal Sensor Power Management Lock (TSPMLOCK): Setting this bit to a 1 causes the rest of the bits in this register to be locked.
14	0h RW/L	**Dynamic Thermal Sensor Shutdown in S0 Idle Enable (DTSSS0EN):** Dynamic Thermal Sensor Shutdown in S0 idle Enable (DTSSS0EN): 1: Dynamic thermal sensor shutdown in S0 idle is enabled. When set to 1, the power management logic shuts down the thermal sensor when the CPU is in a C-state and TEMP.TSR andlt;= LTT.LTT. 0: Dynamic thermal sensor shutdown in S0 idle is disabled
13	0h RW/L	**Dynamic Thermal Sensor Shutdown in C0 Allowed (DTSSIC0):** Dynamic Thermal Sensor Shutdown in C0 Allowed (DTSSIC0) 0: CPU must be in a non-C0 state to allow PCH thermal sensor shutdown 1: CPU can be in a C0 or non-C0 state to allow PCH thermal sensor shutdown.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RO	Reserved.
11:9	4h RW/L	**Maximum Thermal Sensor Shutdown Time (MAXTSST):** Maximum Thermal Sensor Shutdown Time (MAXTSST) - sets the maximum time that the thermal sensor will be held in a shutdown state assuming no other wake conditions. This register is used to set the expiration time of a timer that is used to wake up the thermal sensor on expiration. 000: 1 s 001: 2 s 010: 4 s 011: 8 s 100: 16 s 101-111: Reserved
8:0	0h RW	**Low Temp Threshold (LTT):** Low Temp Threshold (LTT) - Sets the low maximum temp value used for dynamic thermal sensor shutdown consideration. See DTSSS0EN for details. This register field is not lockable, so that SW can change the values during runtime.

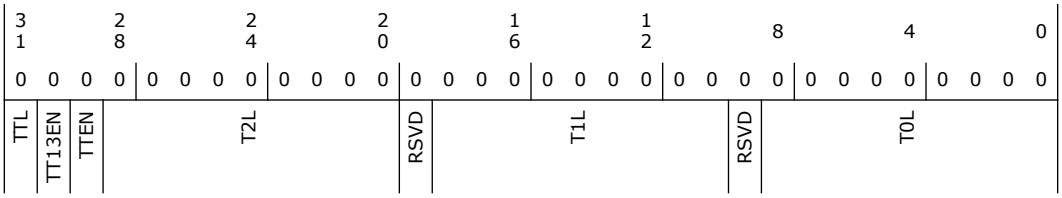
23.2.11 Throttle Levels (TL)—Offset 40h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 20
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**TT.Lock (TTL):** When set to 1, this entire register (TL) is locked and remains locked until the next platform reset.
30	0h RW/L	**TT.State13 Enable (TT13EN):** When set to 1, then PMSync state 13 will force at least T2 state.
29	0h RW/L	**TT Enable (TTEN):** When set the thermal throttling states are enabled. At reset, BIOS must set bits 28:0 and then do a separate write to set bit 29 to enable throttling. SW may set bit 31 at the same time it sets bit 29 if it wishes to lock the register. If SW wishes to change the values of 28:0, it must first clear the TTEN bit, then change the values in 28:0, and then re-enable TTEN. It is legal to set bits 31, 30 and 29 with the same write. This bit must not be set unless the thermal sensor is already enabled (set TSC[7]=1 and TSC[3:2] = 10).
28:20	0h RW/L	**T2 Level (T2L):** When TTEN = 1 AND TSE = 1 AND (T2L = TSR[8:0] T1L), then the system is in T2 state. When TTEN = 1 AND TSE = 1 AND (TSR[8:0] T2L), then the system is in T3 state. NOTE: the T3 condition overrides PMSync[13] and forces the system to T3 if both cases are true. SW NOTE: T2L must be programmed to a value greater than T1L if TTEN=1
19	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
18:10	0h RW/L	**T1 Level (T1L):** When TTEN = 1 AND TSE = 1 AND (T1L = TSR[8:0] T0L), then the system is in T1 state. SW NOTE: T1L must be programmed to a value greater than T0L if TTEN=1
9	0h RO	Reserved.
8:0	0h RW/L	**T0 Level (T0L):** When TEMP.TSR[8:0] is less than or equal to T0L OR TT.Enable is 0 OR TSE = 0, then the system is in T0 state.

23.2.12 Throttle Level 2 (TL2)—Offset 50h

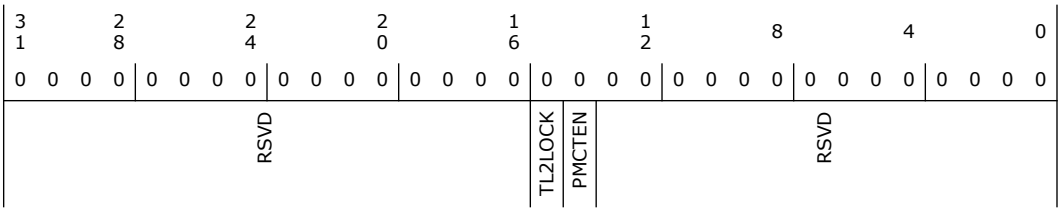
Throttle Level 2

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 20
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	0h RW/L	**TL2 lock (TL2LOCK):** TL2.Lock - When set to 1, this entire register (TL2) is locked and remains locked until the next platform reset.
14	0h RW/L	**PMC Throttling Enable (PMCTEN):** PMC Throttling Enable (PMCTEN) - When set to 1 and the PMC is requesting throttling, force at least the T-state that PMC is requesting.
13:0	0h RO	Reserved.

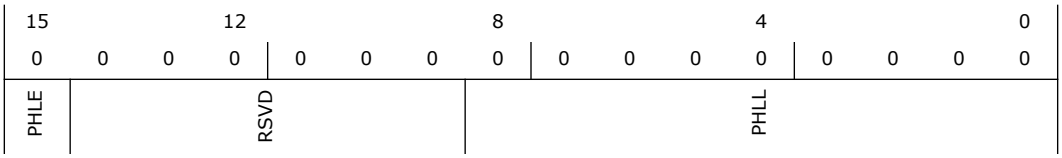
23.2.13 PCH Hot Level (PHL)—Offset 60h

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 20
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/L	**PHL Enable (PHLE):** When set and the current temperature reading, TSR, is greater than or equal to PHLL, then the PCHHOT# pin will be asserted (active low).
14:9	0h RO	Reserved.
8:0	0h RW/L	**PHL Level (PHLL):** Temperature value used for PCHHOT# pin.

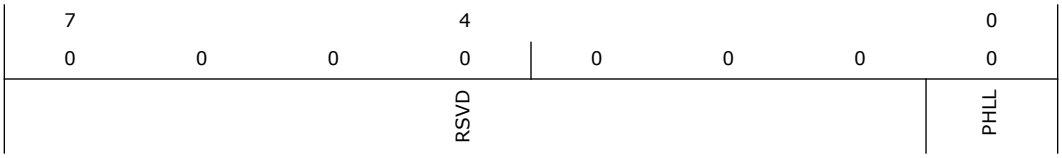
23.2.14 PHL Control (PHLC)—Offset 62h

Access Method

Type: MEM Register
(Size: 8 bits)

Device: 20
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7:1	0h RO	Reserved.
0	0h RW/L	**PHL Lock (PHLL):** When written to a 1, then both PHL and PHLC are locked

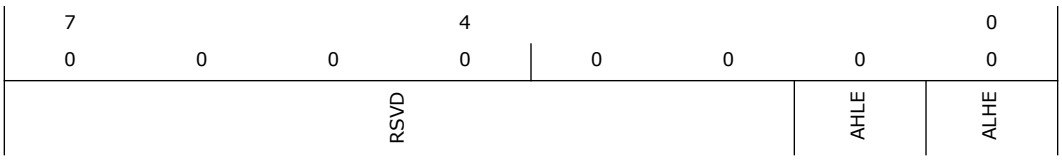
23.2.15 Thermal Alert Status (TAS)—Offset 80h

Access Method

Type: MEM Register
(Size: 8 bits)

Device: 20
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7:2	0h RO	Reserved.
1	0h RW/1C	**Alerth High-to-Low Event (AHLE):** 1: Indicates that a Hot Thermal Sensor trip event occurred based on a lower to higher temperature transition thru the trip point. 0: No trip for this event Software must write a 1 to clear this status bit.
0	0h RW/1C	**Alert Low-to-High Event (ALHE):** 1: Indicates that an Aux Thermal Sensor trip event occurred based on a lower to higher temperature transition thru the trip point. 0: No trip for this event Software must write a 1 to clear this status bit.

23.2.16 PCI Interrupt Event Enables (TSPIEN)—Offset 82h

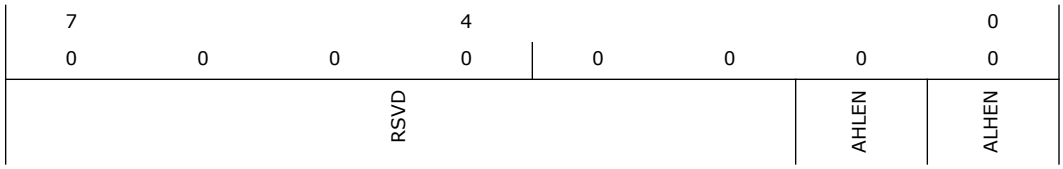
This register controls the conditions that result in the PCI Interrupt signal from the Thermal Sensor (TS) logic to assert.
Note that there is a separate enable register per sensor.

Access Method

Type: MEM Register
(Size: 8 bits)

Device: 20
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7:2	0h RO	Reserved.
1	0h RW	**Alert High-to-Low Enable (AHLEN):** When set to 1, the thermal sensor logic asserts the Thermal logic PCI INTx signal when the corresponding status bit is set in the Thermal Error Status register. When cleared, the corresponding status bit does not result in PCI INTx.
0	0h RW	**Alert Low-to-High Enable (ALHEN):** See the description for bit 1.

23.2.17 General Purpose Event Enables (TSGPEN)—Offset 84h

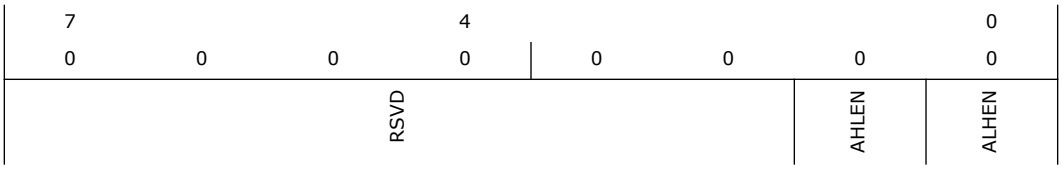
This register controls the conditions that result in the General Purpose Event (GPE) flag (TSS[3]) being set. When the TS GPE signal asserts, the GPE block reports a 1 in the TCOSCI_STS bit.

Access Method

Type: MEM Register
(Size: 8 bits)

Device: 20
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7:2	0h RO	Reserved.
1	0h RW	**Alert High-to-Low Enabble (AHLEN):** When set to 1, the thermal sensor logic asserts its General Purpose Event signal to the GPE block when the corresponding status bit is set in the Thermal Error Status register. When cleared, the corresponding status bit does not result in the GPE signal assertion.
0	0h RW	**Alert Low-to-High Enable (ALHEN):** See the description for bit 1.

23.2.18 Thernak Controller Function Disable (TCFD)—Offset F0h

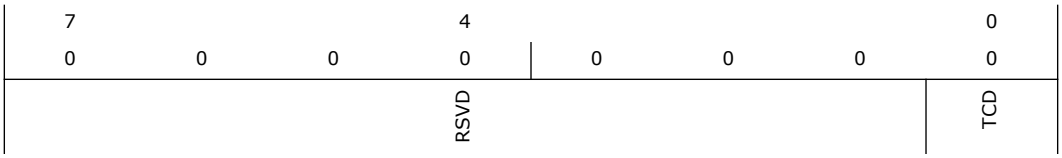
Function Disable bit

Access Method

Type: MEM Register
(Size: 8 bits)

Device: 20
Function: 2

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7:1	0h RO	Reserved.
0	0h RW	**Thermal Controller Disable (TCD):** Thermal Controller Disable (TCD): When set, the the Thermal Controller, is disabled.

23.3

§ §

24 CSI2 Interface (D20:F3)

24.1 CSI-2 Configuration Registers Summary

Table 24-1. Summary of CSI-2 Configuration Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	CFG_ID (CFG_ID)—Offset 0h	9D328086h
4h	7h	CFG_CMD (CFG_CMD_STS)—Offset 4h	100000h
8h	Bh	Revision ID and Class Code (CFG_CC)—Offset 8h	48000XXh
Ch	Fh	CFG_CLS_LT_HTYPE_BIST (CFG_CLS_LT_HTYPE_BIST)—Offset Ch	0h
10h	13h	CFG_CIOLBA (CIOLBA)—Offset 10h	4h
14h	17h	CFG_CIOUBA (CIOUBA)—Offset 14h	0h
2Ch	2Fh	CFG_SSID (SSID)—Offset 2Ch	0h
34h	37h	CFG_CAPPTR (CAPPTR)—Offset 34h	90h
3Ch	3Fh	CFG_INTR (CFG_INTR)—Offset 3Ch	100h
90h	93h	CFG_MID_MMC (CFG_MID_MMC)—Offset 90h	80A005h
94h	97h	CFG_MMLA (CFG_MMLA)—Offset 94h	0h
98h	9Bh	CFG_MMUA (CFG_MMUA)—Offset 98h	0h
9Ch	9Fh	CFG_MMD (CFG_MMD)—Offset 9Ch	0h
A0h	A3h	CFG_AFID (AFID)—Offset A0h	306D013h
A4h	A7h	CFG_AF_CMD_STS (AF_CMD_STS)—Offset A4h	0h
D0h	D3h	CFG_PID_PC (CFG_PID_PC)—Offset D0h	30001h
D4h	D7h	CFG_PMCSR (CFG_PMCSR)—Offset D4h	8h

24.1.1 CFG_ID (CFG_ID)—Offset 0h

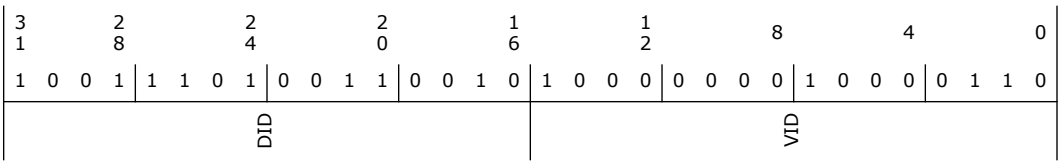
Type 0 PCI Header

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 3

Default: 9D328086h



Bit Range	Default & Access	Field Name (ID): Description
31:16	9D32h RO/V	**Device ID (DID):** Indicates the device number of the controlled.
15:0	8086h RO	**Vendor ID (VID):** Indicates that Intel is the vendor.

24.1.2 CFG_CMD (CFG_CMD_STS)—Offset 4h

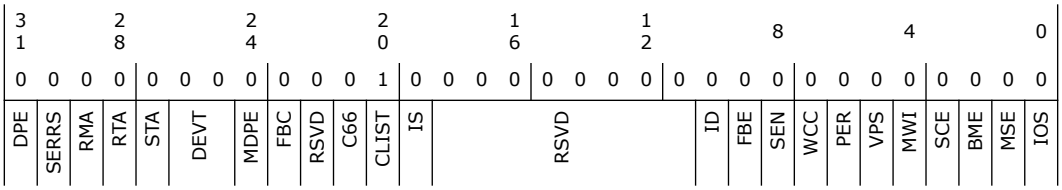
Command

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 3

Default: 100000h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Detected Parity Error (DPE):** not implemented (hardwired to 0)
30	0h RO	**SERR# Status (SERRS):** Not implemented. Hardwired to 0.
29	0h RW/1C/V	**RMA:** Received Master Abort (RMA): If the completion status received from IOSF is UR, this bit is set. SW writes a 1 to this bit to clear it.
28	0h RW/1C/V	**RTA:** Received Target Abort (RTA): If the completion status received from IOSF is CA, this bit is set. SW writes a 1 to this bit to clear it.
27	0h RW/1C/V	**STA:** Not implemented. Hardwired to 0.
26:25	0h RO	**DEVT:** Not implemented. Hardwired to 0.
24	0h RO	**MDPE:** Not implemented. Hardwired to 0.
23	0h RO	**FBC:** Not implemented. Hardwired to 0.
22	0h RO	Reserved.
21	0h RO	**66MHz Capability (C66):** Not implemented. Hardwired to 0.
20	1h RO	**Capabilities List Exists (CLIST):** Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h.

Bit Range	Default & Access	Field Name (ID): Description
19	0h RO/V	**Interrupt Status (IS):** Reflects the state of the INTx# signal at the input of the enable/disable circuit. This bit is a 1 when the INTx# is asserted. This bit is a 0 after the interrupt is cleared.
18:11	0h RO	Reserved.
10	0h RW	**Interrupt Disable (ID):** Enables the device to assert an INTx#. When set, the Camera IO Controller subsystem INTx# signal will be de-asserted. When cleared, the INTx# signal may be asserted.
9	0h RO	**FBE:** Not implemented.
8	0h RW	**SERR Enable (SEN):** Functionality not implemented. This bit is R/W to pass PCIe compliance testing.
7	0h RO	**WCC:** Not implemented.
6	0h RW	**Parity Error Response (PER):** Functionality not implemented. This bit is R/W to pass PCIe compliance testing.
5	0h RO	**VPS:** Not implemented.
4	0h RO	**MWI:** Not implemented.
3	0h RO	**SCE:** Not implemented.
2	0h RW	**Bus Master Enable (BME):** 1 = Enable, 0 = Disable. Controls standard PCI Express bus mastering capabilities for Memory and IO, reads and writes.
1	0h RW	**Memory Space Enable (MSE):** When set, enables memory space accesses to the Camera IO Controller subsystem.
0	0h RO	**I/O Space (IOS):** The Camera IO Controller subsystem does not implement IO Space, therefore this bit is hardwired to 0.

24.1.3 Revision ID and Class Code (CFG_CC)—Offset 8h

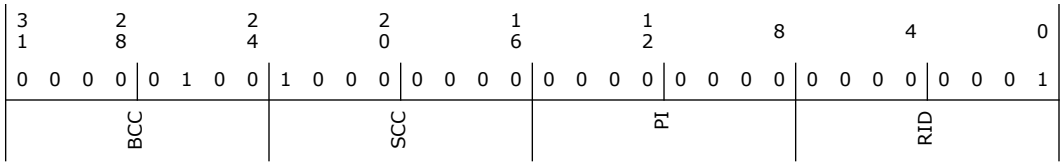
This register contains the device programming interface information related to the Sub-Class Code and Base Class Code definition.
This register also identifies the Base Class Code and the function sub-class in relation to the Base Class Code.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 3

Default: 48000xxh



Bit Range	Default & Access	Field Name (ID): Description
31:24	4h RW/L	**Base Class Code (BCC):** This register indicates that the function implements a multimedia device.
23:16	80h RW/L	**Sub Class Code (SCC):** This indicates the device is an Camera IO Controller device, in the context of a multimedia device.
15:8	0h RW/L	**Programming Interface (PI):** Value assigned to the Camera IO Controller subsystem.
7:0	-- RO/V	**Revision ID (RID):** Indicates the device specific revision identifier. See the Device and Version ID Table in Volume 1 for the default value.

24.1.4 CFG_CLS_LT_HTYPE_BIST (CFG_CLS_LT_HTYPE_BIST)—Offset Ch

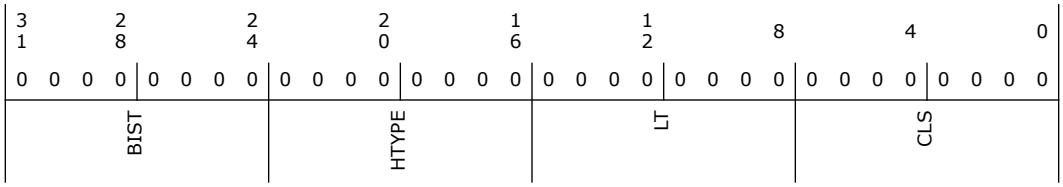
Built-in Self-Test, Header Type, Latency Time, Cache Line Size

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Built-in Self Test (BIST):** Not implemented in the Camera IO Controller subsystem. Hardwired to 00h.
23:16	0h RO	**Header Type (HTYPE):** Implements Type 0 Configuration header.
15:8	0h RW	**Latency Timer (LT):** Maintains RW for Legacy PCI SW compliancy.
7:0	0h RW	**Cache Line Size (CLS):** Doesn't apply to PCI Express. PCI Express spec requires this to be implemented as a R/W register but has no functional impact on the Camera IO Controller subsystem.

24.1.5 CFG_CIOLBA (CIOLBA)—Offset 10h

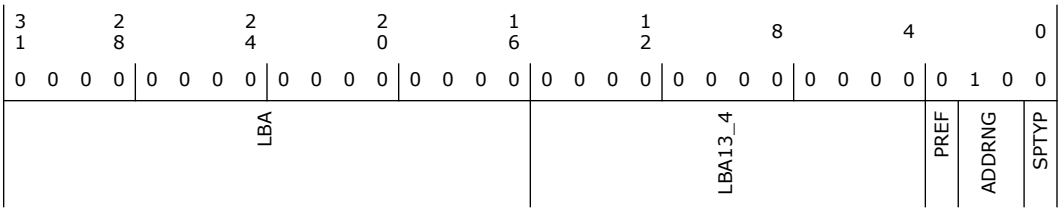
Camera IO Controller Lower Base Address

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 3

Default: 4h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Lower Base Address (LBA):** Base address for the Camera IO Controller subsystems memory mapped configuration registers. 16 Kbytes are requested by hardwiring bits 13:4 to 0s.
15:4	0h RO	**Reserved (LBA13_4):** Hardwired_to_0
3	0h RO	**Prefetchable (PREF):** Indicates that this BAR is NOT prefetchable.
2:1	2h RO	**Address Range (ADDRNG):** Indicates that this BAR can be located anywhere in 64-bit address space.
0	0h RO	**Space Type (SPTYP):** Indicates that this BAR is located in memory space.

24.1.6 CFG_CIOUBA (CIOUBA)—Offset 14h

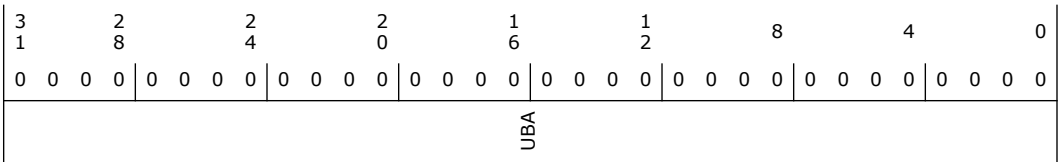
Camera IO Controller Upper Base

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Upper Base Address (UBA):** Upper 32 bits of the Base address for the Camera IO Controller subsystems memory mapped configuration registers.

24.1.7 CFG_SSID (SSID)—Offset 2Ch

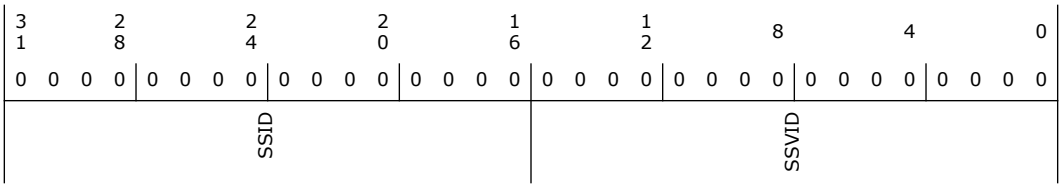
Camera IO Controller Sub System ID

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW/L	**Sub System ID. (SSID):** This register is configured by BIOS. Locked when FNCFG.BCLD = 1.
15:0	0h RW/L	**Sub System Vendor ID (SSVID):** This register is configured by BIOS. Locked when FNCFG.BCLD = 1.

24.1.8 CFG_CAPPTR (CAPPTR)—Offset 34h

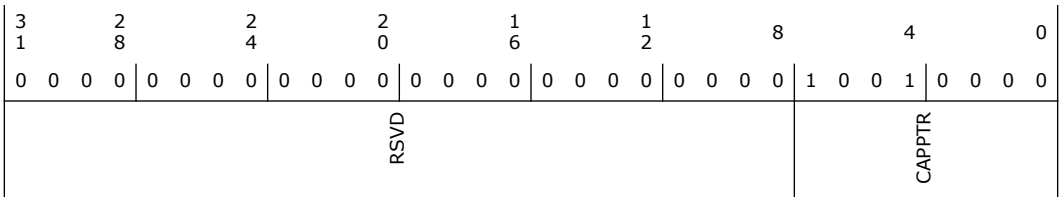
Capabilities Pointer

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 3

Default: 90h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	90h RW/L	**Capability Pointer (CAPPTR):** Indicates that the first capability pointer offset is offset 90h (MSI Capability).

24.1.9 CFG_INTR (CFG_INTR)—Offset 3Ch

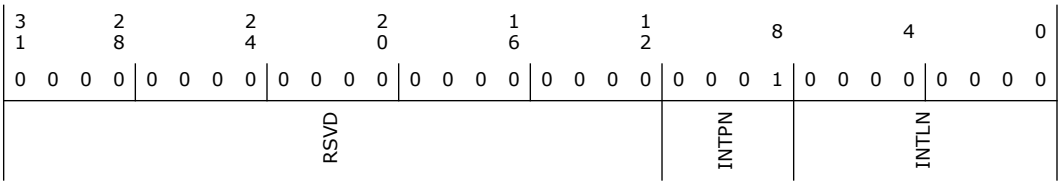
Interrupt Information

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 3

Default: 100h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	Reserved.
11:8	1h RO	**Interrupt Pin (INTPN):** Identifies the interrupt pin the function uses which is INTA.
7:0	0h RW	**Interrupt Line (INTLN):** Hardware does not use this field directly. It is used to communicate to software the interrupt line that the interrupt pin is connected to.

24.1.10 CFG_MID_MMC (CFG_MID_MMC)—Offset 90h

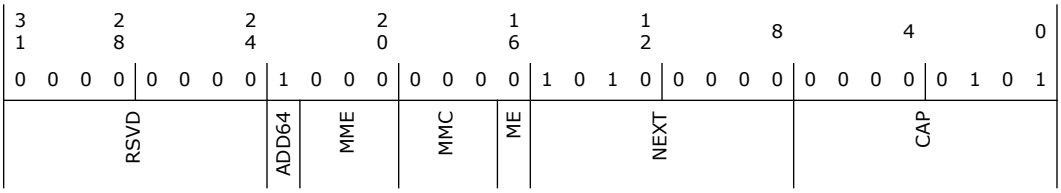
MSI Capability ID

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 3

Default: 80A005h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	1h RO	**64b Address Capability (ADD64):** Indicates the ability to generate a 64-bit message address.
22:20	0h RO	**Multiple Message Enable (MME):** Only 1 message is supported, these bits are hardwired to for 1 message.
19:17	0h RO	**Multiple Message Capable (MMC):** Hardwired to 0 indicating request for 1 message.
16	0h RW	**MSI Enable (ME):** If set to 1 an MSI will be generated instead of an INTx# signal. If set to 0, an MSI may not be generated.
15:8	A0h RW/L	**Next Capability (NEXT):** Points to the next capability structure (Advanced Features).
7:0	5h RO	**Capability ID (CAP):** Indicates that this pointer is MSI a capability.

24.1.11 CFG_MMLA (CFG_MMLA)—Offset 94h

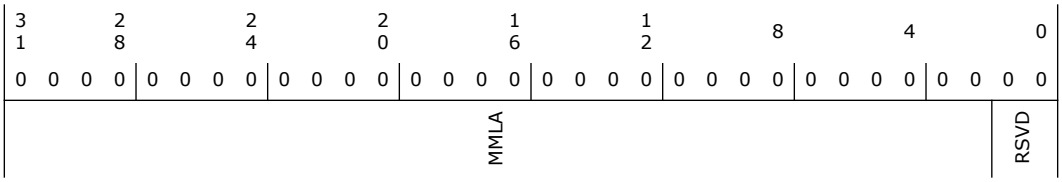
MSI Message Lower Address

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**MSI Message Lower Address (MMLA):** Lower Address used for MSI Message.
1:0	0h RO	Reserved.

24.1.12 CFG_MMUA (CFG_MMUA)—Offset 98h

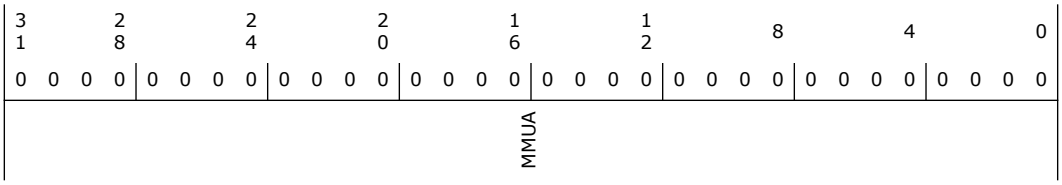
MSI Message Lower Address

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**MSI Message Upper Address (MMUA):** Upper Address used for MSI Message.

24.1.13 CFG_MMD (CFG_MMD)—Offset 9Ch

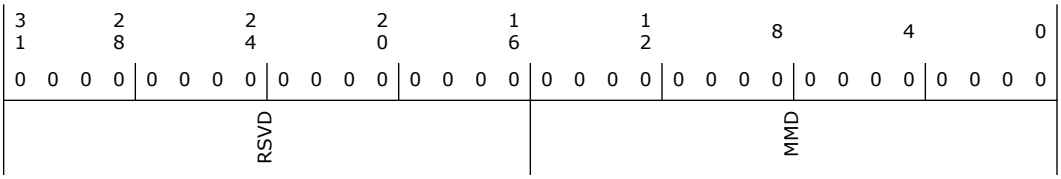
MSI Message Data

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	0h RW	**MSI Message Data (MMD):** Data used for MSI Message.

24.1.14 CFG_AFID (AFID)—Offset A0h

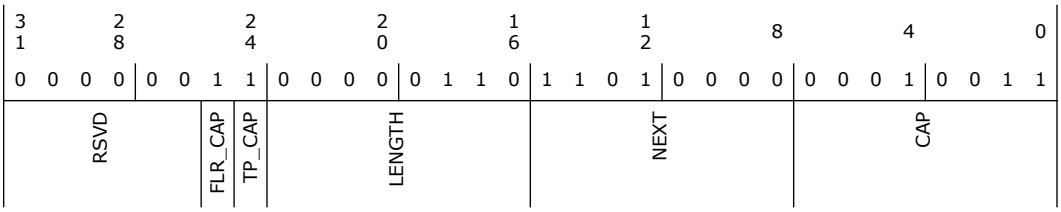
Advanced Features Capability Identifiers

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 3

Default: 306D013h



Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	Reserved.
25	1h RO	**Function Level Reset Capability (FLR_CAP):** Set to 1b to indicate support for Function Level Reset.
24	1h RO	**Transactions Pending Capability (TP_CAP):** Sets to 1b to indicate support for the Transactions Pending (TP) bit. TP must be supported if FLR is supported.

Bit Range	Default & Access	Field Name (ID): Description
23:16	6h RO	**LENGTH (LENGTH):** AF Structure Length (Bytes).
15:8	D0h RW/L	**Next Capability (NEXT):** Points to the next capability structure (Power Management). Locked when FNCFG.BCLD = 1.
7:0	13h RO	**Capability ID (CAP):** The value of 13h in this field identifies the Function as being AF capable.

24.1.15 CFG_AF_CMD_STS (AF_CMD_STS)—Offset A4h

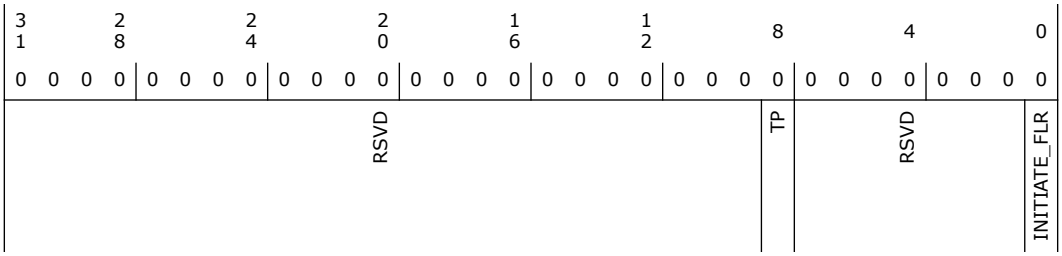
Advanced Features Command and Status Register

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h RO/V	**Transactions Pending (TP):** A value of 1b indicates that the Function has issued one or more non-posted transactions which have not been completed.
7:1	0h RO	Reserved.
0	0h WO	**Initiate Function Level Reset (INITIATE_FLR):** A write of 1b initiates Function Level Reset. FLR requirements are defined in the PCI Express Base Specification.

24.1.16 CFG_PID_PC (CFG_PID_PC)—Offset D0h

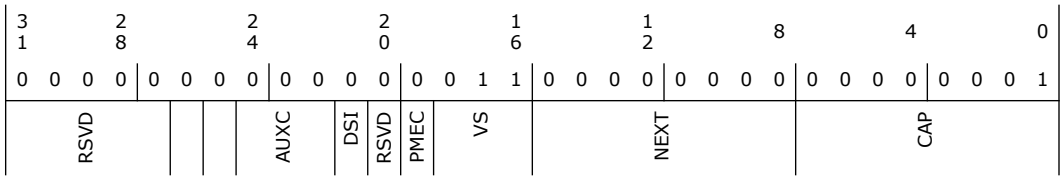
Power Management Capability Identifiers

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 3

Default: 30001h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	Reserved.
26	0h RO	**D2S:** The D2 state is not supported
25	0h RO	**D1S:** The D1 state is not supported
24:22	0h RO	**Auxiliary Current Requirements (AUXC):** This 3 bit field reports the 3.3Vaux auxiliary current requirements for the PCI function. the following bit assignments apply: Bit 3.3Vaux 8 7 6 Max. Current Required 1 1 1 375 mA 1 1 0 320 mA 1 0 1 270 mA 1 0 0 220 mA 0 1 1 160 mA 0 1 0 100 mA 0 0 1 55 mA 0 0 0 0 mA (self powered).
21	0h RO	**Device Specific Initialization (DSI):** Indicates that no device-specific initialization is required.
20	0h RO	Reserved.
19	0h RO	**PME Clock (PMEC):** Not applicable.
18:16	3h RW/L	**Version (VS):** Indicates support for Revision 1.2 of the PCI Power Management Specification. Programmable by BIOS to older revision if compatibility issue is found.Locked when FNCFG.BCLD = 1.
15:8	0h RW/L	**Next Capability (NEXT):** This field has a value of 00h to indicate that this is the last capability structure in the list.Locked when FNCFG.BCLD = 1.
7:0	1h RO	**Capability ID (CAP):** Indicates that this pointer is a PCI power management capability.

24.1.17 CFG_PMCSR (CFG_PMCSR)—Offset D4h

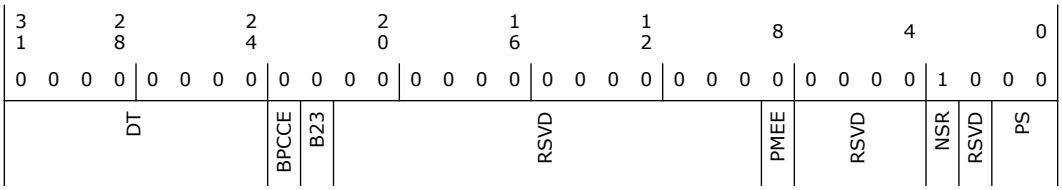
Power Management Control & Status

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 3

Default: 8h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**DT:** Does not apply. Hardwired to 0s.
23	0h RO	**BPCCE:** Does not apply. Hardwired to 0s.
22	0h RO	**B23:** Does not apply. Hardwired to 0.
21:9	0h RO	Reserved.
8	0h RO	**PME Enable (PMEE):** CIO2 do not support PME# generation from any D-state so this bit is read-only always returning a 0 when read by system software.
7:4	0h RO	Reserved.
3	1h RW/L	**No Soft Reset (NSR):** When set (1), this bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved. Upon transition from the D3hot to the D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the PowerState bits.
2	0h RO	Reserved.
1:0	0h RW	**Power State (PS):** This field is used both to determine the current power state of the Camera IO Controller subsystem and to set a new power state.

24.2 CSI2 Memory Mapped I/O Registers Summary

The description for Port-a or Pipe-a are also applicable to the other Ports/Pipes. In most cases, the offsets are documented in the Port-a/Pipe-a description.

Table 24-2. Summary of CSI2 Memory Mapped I/O Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	CSI RX Enable (csi2_pipe_a_csi_rx4_reg_rx_csi_enable)—Offset 0h	0h
4h	7h	Number of enabled data lines (csi2_pipe_a_csi_rx4_reg_rx_csi_nof_enabled_lanes)—Offset 4h	0h
Ch	Fh	Error Handling (csi2_pipe_a_csi_rx4_reg_rx_csi_error_handling)—Offset Ch	0h
10h	13h	Short Frame Config (csi2_pipe_a_csi_rx4_reg_rx_csi_sp_if_config)—Offset 10h	0h
14h	17h	Long Frame Config (csi2_pipe_a_csi_rx4_reg_rx_csi_lp_if_config)—Offset 14h	0h
18h	1Bh	Status Register (csi2_pipe_a_csi_rx4_reg_rx_status)—Offset 18h	0h
24h	27h	Clock Termination Delay (csi2_pipe_a_csi_rx4_reg_rx_csi_dly_cnt_termen_clane)—Offset 24h	0h

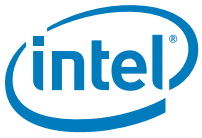


Table 24-2. Summary of CSI2 Memory Mapped I/O Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
28h	2Bh	Settling delay (csi2_pipe_a_csi_rx4_reg_rx_csi_dly_cnt_settle_clane)—Offset 28h	0h
2Ch	2Fh	Delay After Termination (csi2_pipe_a_csi_rx4_reg_rx_csi_dly_cnt_termen_dlane0)—Offset 2Ch	0h
30h	33h	Settling time for Data (csi2_pipe_a_csi_rx4_reg_rx_csi_dly_cnt_settle_dlane0)—Offset 30h	0h
100h	103h	Backend Enable/Disable (csi2_pipe_a_mipi_be_mipi_backend_enable)—Offset 100h	0h
104h	107h	Backend Status (csi2_pipe_a_mipi_be_mipi_backend_status)—Offset 104h	0h
108h	10Bh	Compression and Prediction (csi2_pipe_a_mipi_be_mipi_backend_comp_format_reg_vc0)—Offset 108h	0h
120h	123h	Force raw8 (csi2_pipe_a_mipi_be_mipi_backend_force_raw8_reg)—Offset 120h	0h
124h	127h	IRQ Status (csi2_pipe_a_mipi_be_mipi_backend_irq_status_reg)—Offset 124h	0h
128h	12Bh	Interrupt Clear (csi2_pipe_a_mipi_be_mipi_backend_irq_clear_reg)—Offset 128h	0h
168h	16Bh	Disregard Setting (csi2_pipe_a_mipi_be_mipi_backend_global_lut_disregard_reg)—Offset 168h	0h
16Ch	16Fh	Stalled Packet (csi2_pipe_a_mipi_be_mipi_backend_packet_status_stall_reg)—Offset 16Ch	0h
170h	173h	Parse short packets (csi2_pipe_a_mipi_be_mipi_backend_parse_gsp_through_lp_lut_reg)—Offset 170h	0h
174h	177h	Short packets entry (csi2_pipe_a_mipi_be_mipi_backend_short_packet_lut_entry_0)—Offset 174h	0h
184h	187h	Long packets entry (csi2_pipe_a_mipi_be_mipi_backend_long_packet_lut_entry_0)—Offset 184h	0h
300h	303h	(csi2_pipe_a_irq_ctrl_pipe_irq_edge)—Offset 300h	0h
304h	307h	(csi2_pipe_a_irq_ctrl_pipe_irq_mask)—Offset 304h	0h
308h	30Bh	(csi2_pipe_a_irq_ctrl_pipe_irq_status)—Offset 308h	0h
30Ch	30Fh	(csi2_pipe_a_irq_ctrl_pipe_irq_clear)—Offset 30Ch	0h
310h	313h	(csi2_pipe_a_irq_ctrl_pipe_irq_en)—Offset 310h	0h
314h	317h	(csi2_pipe_a_irq_ctrl_pipe_irq_level_not_pulse)—Offset 314h	0h
1000h	1003h	(gpreg_dev_soft_reset_reg)—Offset 1000h	0h
1004h	1007h	(gpreg_slv_soft_reset_reg)—Offset 1004h	0h
1008h	100Bh	(gpreg_fb_hpll_freq_reg)—Offset 1008h	0h
100Ch	100Fh	(gpreg_isclk_ratio_reg)—Offset 100Ch	0h

24.2.1 CSI RX Enable (csi2_pipe_a_csi_rx4_reg_rx_csi_enable)—Offset 0h

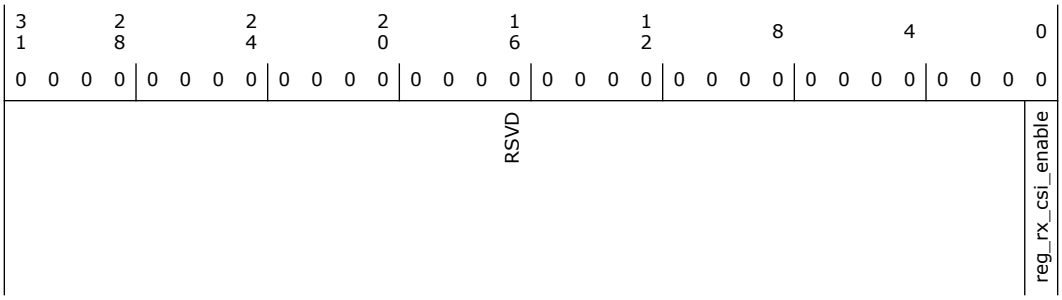
Enable CSI RX4:
Port-a: 0x000
Port-b: 0x400
Port-c: 0x800
Enable CSI RX2:
Port-d: 0xC00.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RW	**reg_rx_csi_enable:** Enable CSI RX

24.2.2 Number of enabled data lines (csi2_pipe_a_csi_rx4_reg_rx_csi_nof_enabled_lanes)—Offset 4h

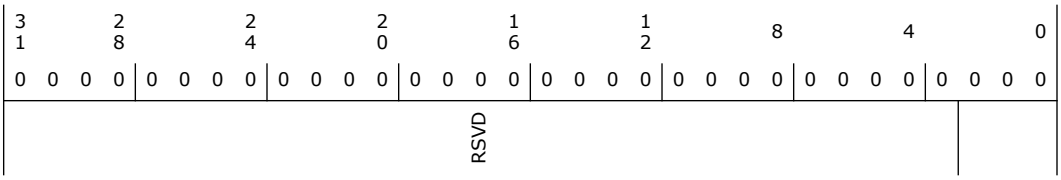
Specify Number of enabled data lanes of CSI RX for port A.
The same register applies to Port B/C/D.
Port-a:0x004h
Port-b:0x404h
Port-c:0x804h
Port-d:0xC04h.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	Reserved.
2:0	0h RW	**Number of enabled data lanes:** Specify Number of enabled data lanes of CSI RX. 0 = No lanes enabled 1 = One lane enabled 2 = Two lanes enabled 3 = Three lanes enabled 4 = Four lanes enabled.

24.2.3 Error Handling (csi2_pipe_a_csi_rx4_reg_rx_csi_error_handling)—Offset Ch

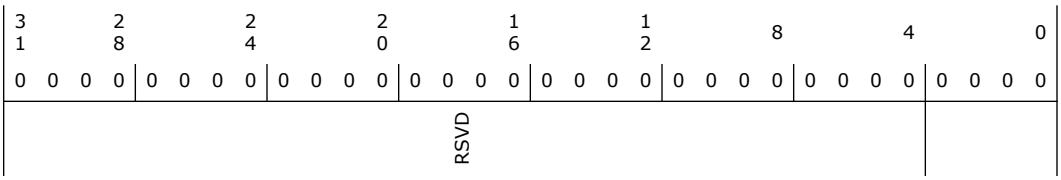
When bit 0 set, packets with more than one errors in packet header are discarded.
Bit 1, when set, a short packet with reserved id is discarded and IRQ is raised
Bit 2, when set, a long packet with reserved id is discarded and IRQ is raised
Bit 3, when set, detection of incomplete packet is disabled, IRQ will not be generated.
Port-a: 0x00C
Port-b: 0x40C
Port-c: 0x80C
Port-d: 0xC0C.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3:0	0h RW	**Error handling register:** When bit 0 set, packets with more than one errors in packet header are discarded. Bit 1, when set, a short packet with reserved id is discarded and IRQ is raised Bit 2, when set, a long packet with reserved id is discarded and IRQ is raised Bit 3, when set, detection of incomplete packet is disabled, IRQ will not be generated.

24.2.4 Short Frame Config (csi2_pipe_a_csi_rx4_reg_rx_csi_sp_if_config)—Offset 10h

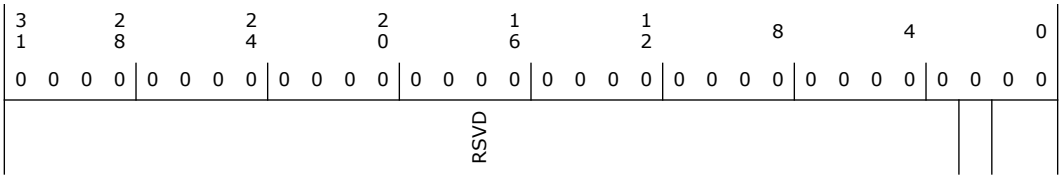
Interframe Short Packet config register.
Port-a: 0x010
Port-b: 0x410
Port-c: 0x810
Port-d: 0xC10.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	Reserved.
2	0h RW	**Field ID1:** 0 = no error flag and no error code added to passed packet 1 = error flag and error code added to passed packet.
1:0	0h RW	**Field ID0:** 00 = filter out all short packets in between frames, no error is communicated (only via IRQ) 01 = filter out inter-frame short packets while VC is inactive, pass when active 10 = always pass 11 = reserved/not used.

24.2.5 Long Frame Config (csi2_pipe_a_csi_rx4_reg_rx_csi_lp_if_config)—Offset 14h

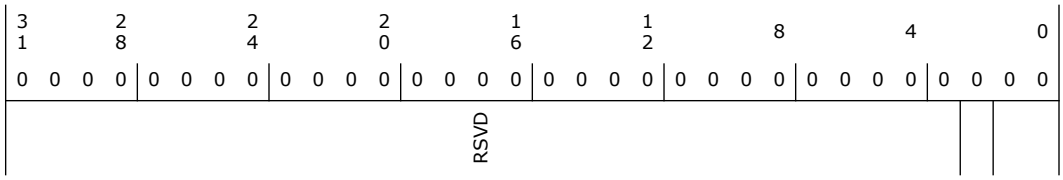
Interframe Long Packet config register.
Pipe-a: 0x014
Pipe-b: 0x414
Pipe-c: 0x814
Pipe-d: 0xC14.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	Reserved.
2	0h RW	**Field ID1:** 0 = no error flag and no error code added to passed packet 1 = error flag and error code added to passed packet.
1:0	0h RW	**Field ID0:** 00 = filter out all long packets in between frames, no error is communicated (only via IRQ) 01 = filter out inter-frame long packets while VC is inactive, pass when active 10 = always pass 11 = reserved/not used.

24.2.6 Status Register (csi2_pipe_a_csi_rx4_reg_rx_status)—Offset 18h

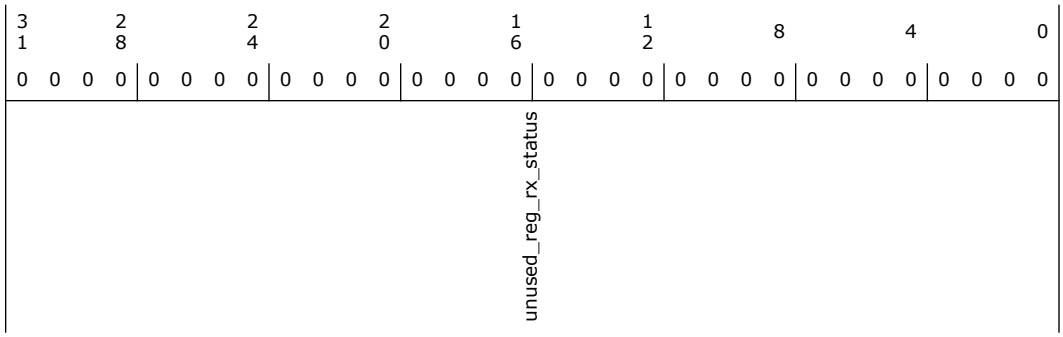
Pipe-a: 0x018
Pipe-a: 0x418
Pipe-a: 0x818
Pipe-a: 0xC18.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**unused_reg_rx_status:** Status register.

24.2.7 Clock Termination Delay (csi2_pipe_a_csi_rx4_reg_rx_csi_dly_cnt_termen_clane) —Offset 24h

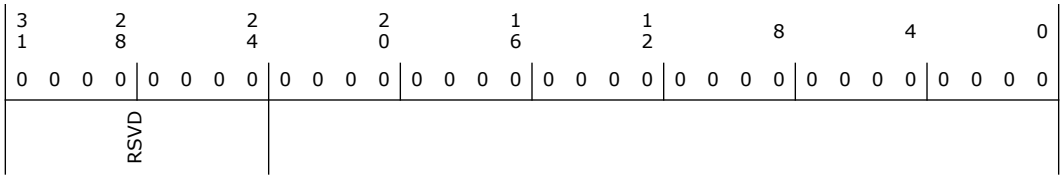
Delay Value after clock termination enabled:
Port-a: 0x024
Port-b: 0x424
Port-b: 0x824
Port-d: 0xC24.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:0	0h RW	**Clock Lane Delay:** Specify the Delay value for Termination enable of Clock lane HS Rx. Counter resolution is 0.0625ns per count number.

24.2.8 Settling delay (csi2_pipe_a_csi_rx4_reg_rx_csi_dly_cnt_settle_clane)—Offset 28h

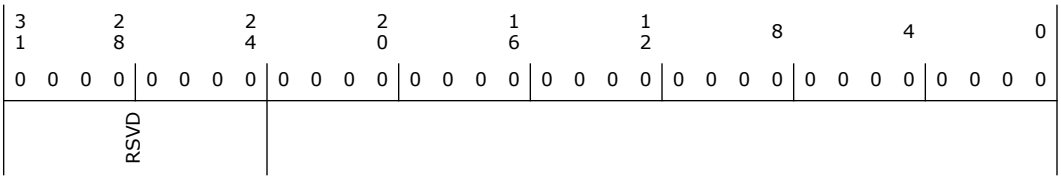
Delay Value for settling time of clock:
Port-a: 0x028
Port-b: 0x428
Port-b: 0x828
Port-d: 0xC28.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:0	0h RW	**Delay Value :** Specify the Delay value for HS Settling time of Clock lane HS Rx data. Counter resolution is 0.0625ns per count number.

24.2.9 Delay After Termination (csi2_pipe_a_csi_rx4_reg_rx_csi_dly_cnt_termen_dlane0)—Offset 2Ch

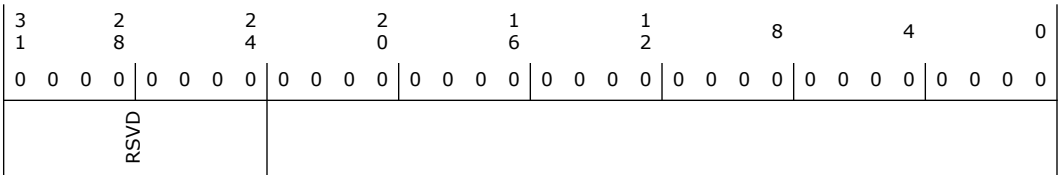
Delay Value after data termination enabled in HS Rx:
Port-a:
Lane0 : 0x02C
Lane1 : 0x034
Lane2 : 0x03C
Lane3 : 0x044.
Port-b:
Lane0 : 0x42C
Lane1 : 0x434
Lane2 : 0x43C
Lane3 : 0x444.
Port-c:
Lane0 : 0x82C
Lane1 : 0x834
Lane2 : 0x83C
Lane3 : 0x844.
Port-d:
Lane0 : 0xC2C
Lane1 : 0xC34

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:0	0h RW	**Delay Value:** Specify the Delay value for Termination enable of Data lane 0 HS Rx. Counter resolution is 0.0625ns per count number.

24.2.10 Settling time for Data (csi2_pipe_a_csi_rx4_reg_rx_csi_dly_cnt_settle_dlane0) —Offset 30h

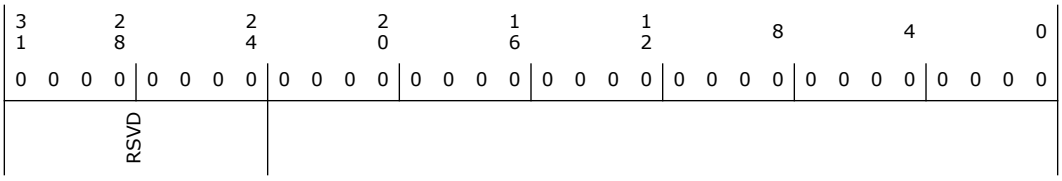
Delay value for Settling time of Data lane in HS Rx:
Port-a:
Lane0 : 0x030
Lane1 : 0x038
Lane2 : 0x040
Lane3 : 0x048.
Port-b:
Lane0 : 0x430
Lane1 : 0x438
Lane2 : 0x440
Lane3 : 0x448.
Port-c:
Lane0 : 0x830
Lane1 : 0x838
Lane2 : 0x840
Lane3 : 0x848.
Port-d:
Lane0 : 0xC30
Lane1 : 0xC38.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:0	0h RW	**:** Specify the Delay value for Settling time of Data lane 0 HS Rx data. Counter resolution is 0.0625ns per count number.

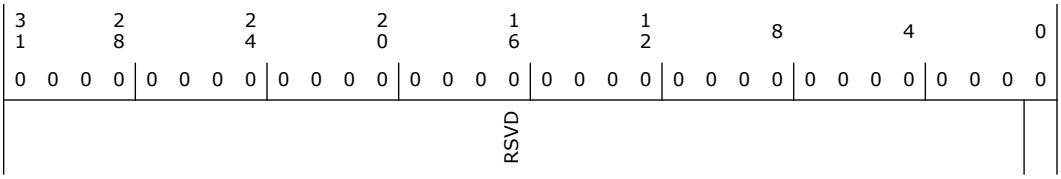
24.2.11 Backend Enable/Disable (csi2_pipe_a_mipi_be_mipi_backend_enable)—Offset 100h

Enable/disable MIPI backend:
Port-a: 0x100
Port-b: 0x500
Port-c: 0x900
Port-d: 0xD00.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RW	**MIPI backend:** Enable/disable MIPI backend.

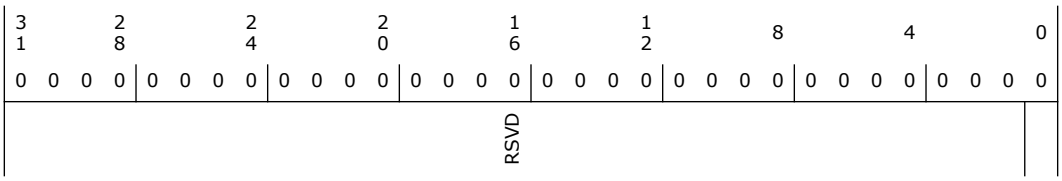
24.2.12 Backend Status (csi2_pipe_a_mipi_be_mipi_backend_status)—Offset 104h

MIPI backend status:
Port-a: 0x104
Port-b: 0x504
Port-c: 0x904
Port-d: 0xD04.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RO	**Backend Status:** Displays status of backend (busy or idle).

24.2.13 Compression and Prediction (csi2_pipe_a_mipi_be_mipi_backend_comp_format_reg_vc0)—Offset 108h

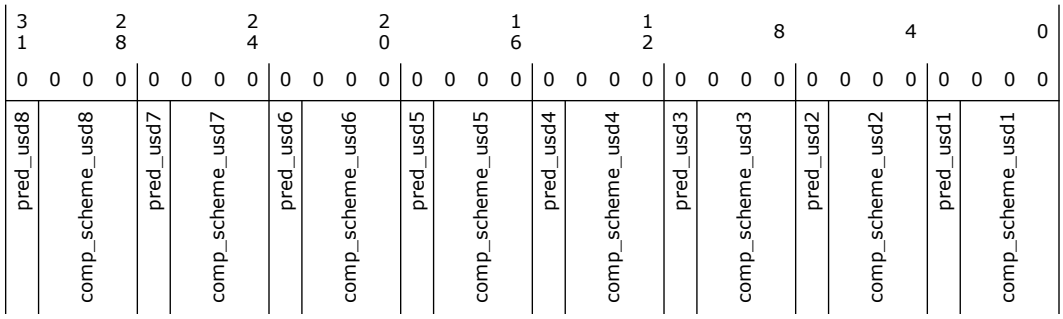
Compression and Prediction scheme registers in this section is applicable to all the ports as followed:
Pipe-a virtual channel
0: 0x108
1: 0x10C
2: 0x110
3: 0x114
Pipe-b virtual channel
0: 0x508
1: 0x50C
2: 0x510
3: 0x514
Pipe-c virtual channel
0: 0x908
1: 0x90C
2: 0x910
3: 0x914
Pipe-d virtual channel
0: 0xD08
1: 0xD0C
2: 0xD10
3: 0xD14.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**predictor (pred_usd8):** predictor for USD8: 0 -> pred1, 1 -> pred2.
30:28	0h RW	**Compression (comp_scheme_usd8):** compression for USD8: value between 0 to 6.
27	0h RW	**Predictor (pred_usd7):** predictor for USD7: 0 -> pred1, 1 -> pred2
26:24	0h RW	**Compression (comp_scheme_usd7):** compression for USD7: value between 0 to 6.
23	0h RW	**Predictor (pred_usd6):** predictor for USD6: 0 -> pred1, 1 -> pred2
22:20	0h RW	**Compression (comp_scheme_usd6):** compression for USD6: value between 0 to 6.
19	0h RW	**Predictor (pred_usd5):** predictor for USD5: 0 -> pred1, 1 -> pred2
18:16	0h RW	**Compression (comp_scheme_usd5):** compression for USD5: value between 0 to 6.
15	0h RW	**Predictor (pred_usd4):** predictor for USD4: 0 -> pred1, 1 -> pred2.
14:12	0h RW	**Compression (comp_scheme_usd4):** compression for USD4: value between 0 to 6.
11	0h RW	**Predictor (pred_usd3):** predictor for USD3: 0 -> pred1, 1 -> pred2.
10:8	0h RW	**Compression (comp_scheme_usd3):** compression for USD3: value between 0 to 6.
7	0h RW	**Predictor (pred_usd2):** predictor for USD2: 0 -> pred1, 1 -> pred2.
6:4	0h RW	**Compression (comp_scheme_usd2):** compression for USD2: value between 0 to 6.
3	0h RW	**Predictor (pred_usd1):** predictor for USD1: 0 -> pred1, 1 -> pred2.
2:0	0h RW	**Compression (comp_scheme_usd1):** compression for USD1: value between 0 to 6.

24.2.14 Force raw8 (csi2_pipe_a_mipi_be_mipi_backend_force_raw8_reg)—Offset 120h

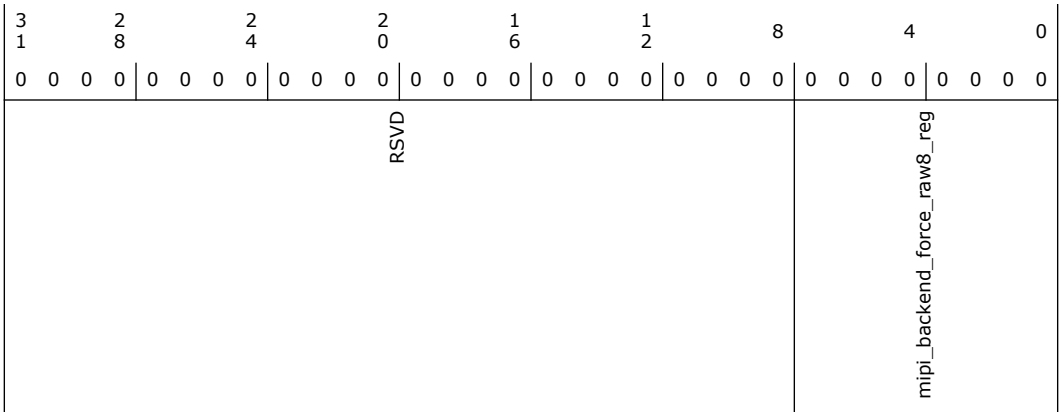
Force raw8 decoding :
Port-a: 0x120
Port-b: 0x520
Port-c: 0x920
Port-d: 0xD20.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	0h RW	**decode Long (mipi_backend_force_raw8_reg):** Force RAW8(byte) decoding for LONG data packets.

24.2.15 IRQ Status (csi2_pipe_a_mipi_be_mipi_backend_irq_status_reg)—Offset 124h

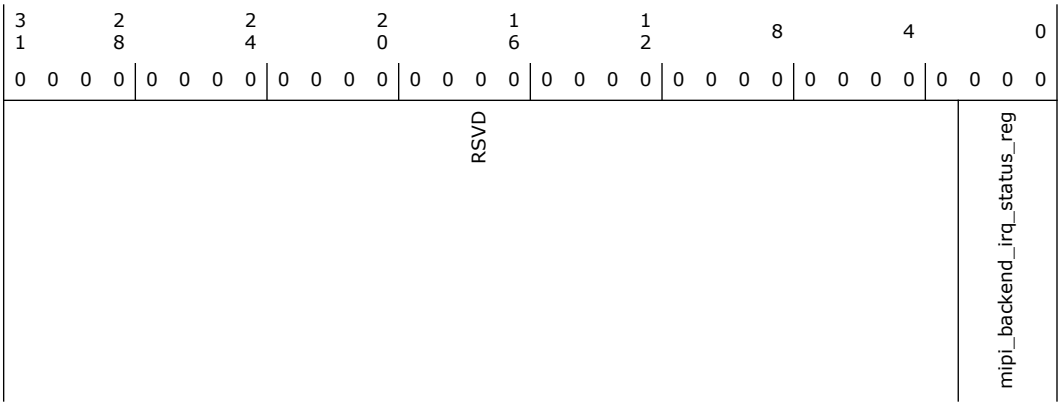
Interrupt status register :
Port-a: 0x124
Port-b: 0x524
Port-c: 0x924
Port-d: 0xD24.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	Reserved.
2:0	0h RO	**mipi_backend_irq_status_reg:** Interrupt status register.

24.2.16 Interrupt Clear (csi2_pipe_a_mipi_be_mipi_backend_irq_clear_reg)—Offset 128h

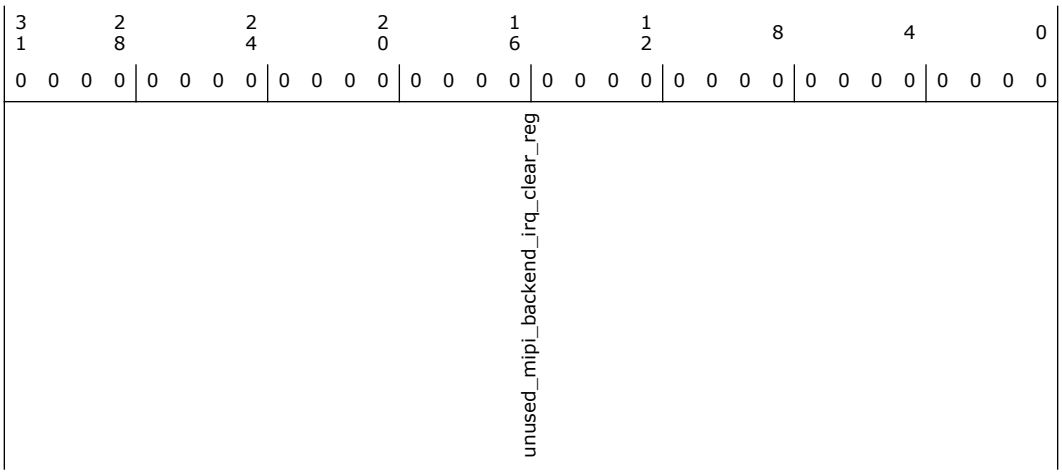
Interrupt clear register :
Port-a: 0x128
Port-b: 0x528
Port-c: 0x928
Port-d: 0xD28.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h WO	**unused_mipi_backend_irq_clear_reg:** Interrupt clear register

24.2.17 Disregard Setting (csi2_pipe_a_mipi_be_mipi_backend_global_lut_disregard_reg)—Offset 168h

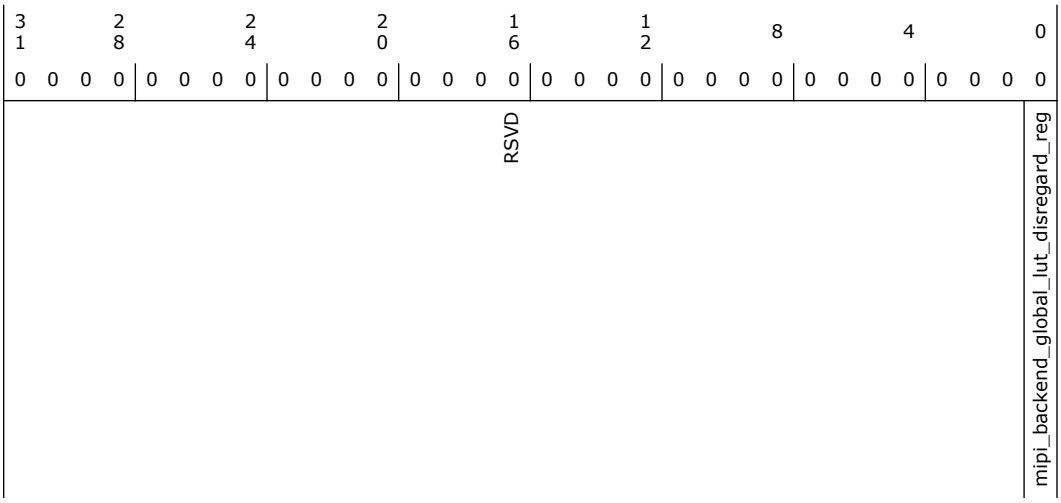
Disregard setting for format types not having a match:
Port-a: 0x168
Port-b: 0x568
Port-c: 0x968
Port-d: 0xD68.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RW	**mipi_backend_global_lut_disregard_reg:** disregard setting for format types not having a match in the LUT, 0=pass, 1=discard

24.2.18 Stalled Packet (csi2_pipe_a_mipi_be_mipi_backend_packet_status_stall_reg)—Offset 16Ch

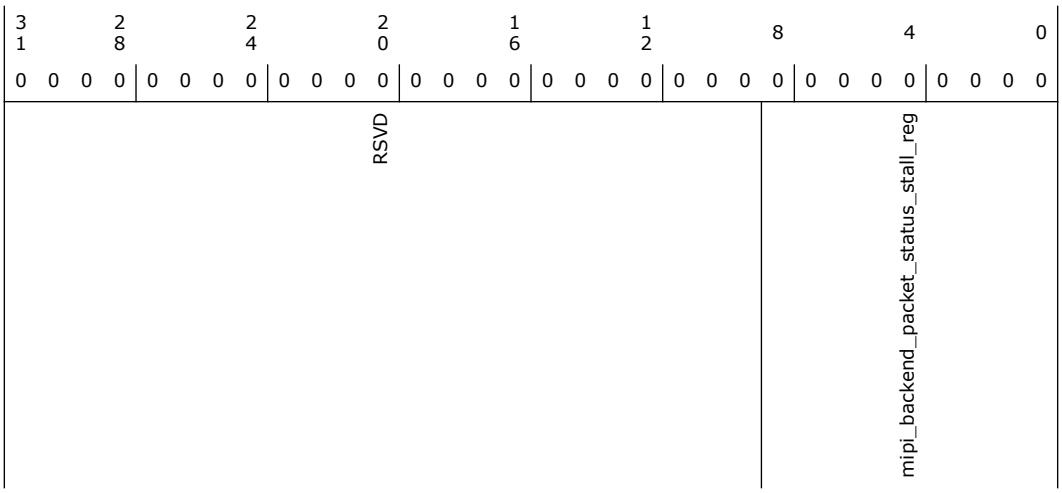
Information about a stalled packet:
Port-a: 0x16C
Port-b: 0x56C
Port-c: 0x96C
Port-d: 0xD6C.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8:0	0h RO	**Status Register (mipi_backend_packet_status_stall_reg):** status register containing information about a stalled packet.

24.2.19 Parse short packets (csi2_pipe_a_mipi_be_mipi_backend_parse_gsp_through_lp_lut_reg)—Offset 170h

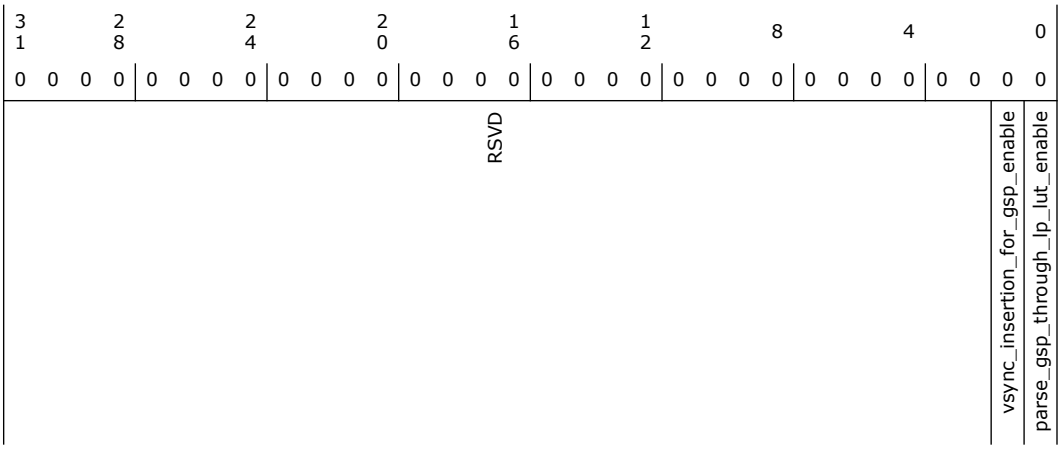
Settings for treating Generic Short Packets as long packets:
Port-a: 0x170
Port-b: 0x570
Port-c: 0x970
Port-d: 0xD70.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1	0h RW	**Vsyncs Insertion (vsync_insertion_for_gsp_enable):** when set, vsyncs are inserted for GSPs
0	0h RW	**Parse Gap (parse_gsp_through_lp_lut_enable):** when set, GSPs are treated as long packets and evaluated against LP LUT

24.2.20 Short packets entry (csi2_pipe_a_mipi_be_mipi_backend_short_packet_lut_entry_0)—Offset 174h

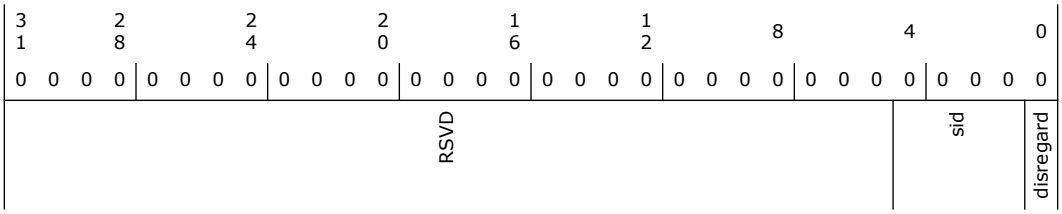
Short Packet Lut Entry for:
Pipe-a, vch_id:
0: 0x174
1: 0x178
2: 0x17C
3: 0x180.
Pipe-b, vch_id:
0: 0x574
1: 0x578
2: 0x57C
3: 0x580.
Pipe-c, vch_id:
0: 0x974
1: 0x978
2: 0x97C
3: 0x980.
Pipe-d, vch_id:
0: 0xD74
1: 0xD78
2: 0xD7C
3: 0xD80.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4:1	0h RW	**sid:** For matching channel ID/ Format type combination.
0	0h RW	**disregard:** disregard bit (pass/discard upon lut match)

24.2.21 Long packets entry (csi2_pipe_a_mipi_be_mipi_backend_long_packet_lut_entry_0)—Offset 184h

Long Packet
Pipe-a, Lut Entry#:
0: 0x184
1: 0x188
2: 0x18C
3: 0x190
4: 0x194
5: 0x198
6: 0x19C
7: 0x1A0
8: 0x1A4
9: 0x1A8
10:0x1AC
11:0x1B0
12:0x1B4
13:0x1B8
14:0x1BC
15:0x1C0.
Pipe-b, Lut Entry#:
0: 0x584
1: 0x588
2: 0x58C
3: 0x590
4: 0x594
5: 0x598
6: 0x59C
7: 0x5A0

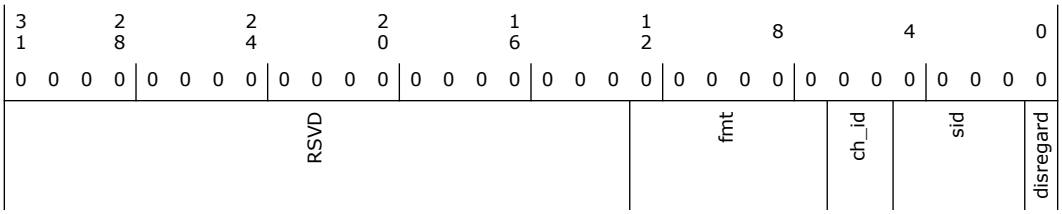
8: 0x5A4
9: 0x5A8
10:0x5AC
11:0x5B0
12:0x5B4
13:0x5B8
14:0x5BC
15:0x5C0.
Pipe-c, Lut Entry#:
0: 0x984
1: 0x988
2: 0x98C
3: 0x990
4: 0x994
5: 0x998
6: 0x99C
7: 0x9A0
8: 0x9A4
9: 0x9A8
10:0x9AC
11:0x9B0
12:0x9B4
13:0x9B8
14:0x9BC
15:0x9C0.
Pipe-d, Lut Entry#:
0: 0xD84
1: 0xD88
2: 0xD8C
3: 0xD90
4: 0xD94
5: 0xD98
6: 0xD9C
7: 0xDA0
8: 0xDA4
9: 0xDA8
10:0xDAC
11:0xDB0
12:0xDB4
13:0xDB8
14:0xDBC
15:0xDC0.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	Reserved.
12:7	0h RW	**Format Type (fmt):** Format type to match
6:5	0h RW	**Channel (ch_id):** Channel ID to match
4:1	0h RW	**sid:** SID for matching channel ID/ Format type combination
0	0h RW	**disregard:** disregard bit (pass/discard upon lut match)

24.2.22 (csi2_pipe_a_irq_ctrl_pipe_irq_edge)—Offset 300h

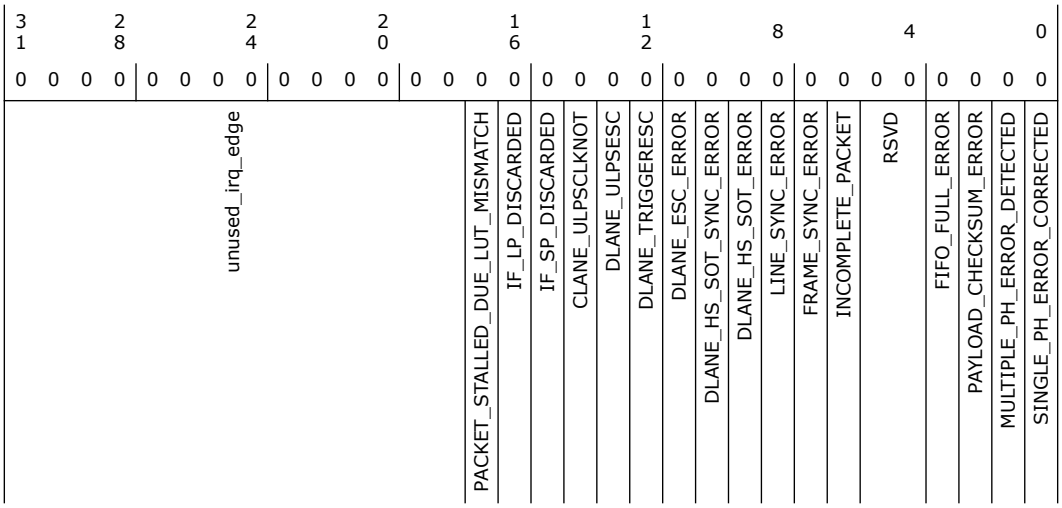
IRQ active edge select per interrupt input. Rising edge: 1, Falling edge: 0

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**unused_irq_edge:** Unused
17	0h RW	**PACKET_STALLED_DUE_LUT_MISMATCH:** Inter-frame long packet discarded
16	0h RW	**IF_LP_DISCARDED:** Inter-frame long packet discarded
15	0h RW	**IF_SP_DISCARDED:** Inter-frame short packet discarded
14	0h RW	**CLANE_ULPSCLKNOT:** Escape mode ultra-low power state exit for clock lane
13	0h RW	**DLANE_ULPSESC:** Escape mode ultra-low power state for data lane(s)
12	0h RW	**DLANE_TRIGGERESC:** Escape mode trigger event
11	0h RW	**DLANE_ESC_ERROR:** Escape mode error
10	0h RW	**DLANE_HS_SOT_SYNC_ERROR:** DPHY synchronization error
9	0h RW	**DLANE_HS_SOT_ERROR:** DPHY start of transmission error
8	0h RW	**LINE_SYNC_ERROR:** Line sync error
7	0h RW	**FRAME_SYNC_ERROR:** Frame sync error
6	0h RW	**INCOMPLETE_PACKET:** Incomplete long packet detected
5:4	0h RO	Reserved.
3	0h RW	**FIFO_FULL_ERROR:** Fifo overflow
2	0h RW	**PAYLOAD_CHECKSUM_ERROR:** Payload checksum (CRC) error
1	0h RW	**MULTIPLE_PH_ERROR_DETECTED:** Multiple packet header errors detected
0	0h RW	**SINGLE_PH_ERROR_CORRECTED:** Single packet header error corrected

24.2.23 (csi2_pipe_a_irq_ctrl_pipe_irq_mask)—Offset 304h

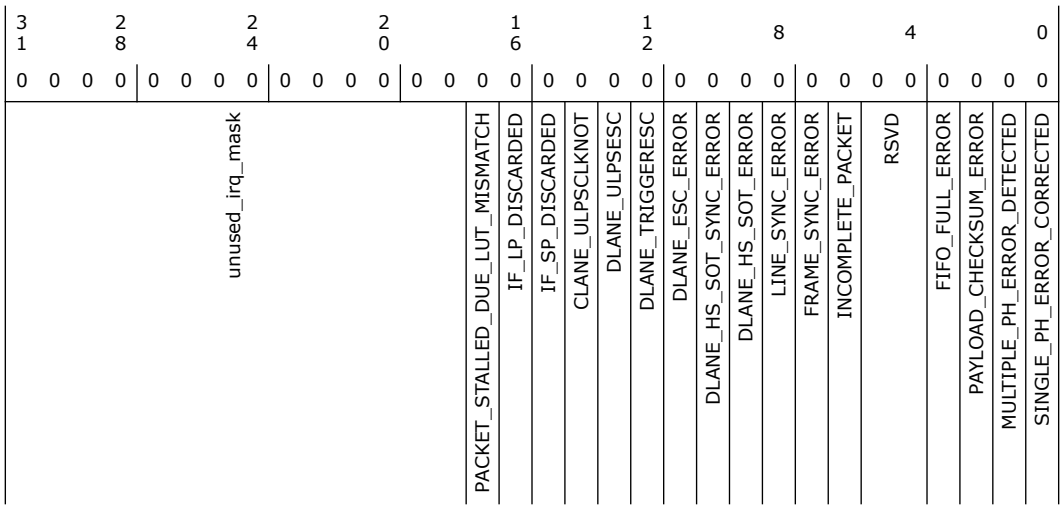
IRQ mask per interrupt

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**unused_irq_mask:** Unused
17	0h RW	**PACKET_STALLED_DUE_LUT_MISMATCH:** Inter-frame long packet discarded
16	0h RW	**IF_LP_DISCARDED:** Inter-frame long packet discarded
15	0h RW	**IF_SP_DISCARDED:** Inter-frame short packet discarded
14	0h RW	**CLANE_ULPSCLKNOT:** Escape mode ultra-low power state exit for clock lane
13	0h RW	**DLANE_ULPSESC:** Escape mode ultra-low power state for data lane(s)
12	0h RW	**DLANE_TRIGGERESC:** Escape mode trigger event
11	0h RW	**DLANE_ESC_ERROR:** Escape mode error
10	0h RW	**DLANE_HS_SOT_SYNC_ERROR:** DPHY synchronization error
9	0h RW	**DLANE_HS_SOT_ERROR:** DPHY start of transmission error
8	0h RW	**LINE_SYNC_ERROR:** Line sync error
7	0h RW	**FRAME_SYNC_ERROR:** Frame sync error
6	0h RW	**INCOMPLETE_PACKET:** Incomplete long packet detected
5:4	0h RO	Reserved.
3	0h RW	**FIFO_FULL_ERROR:** Fifo overflow

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**PAYLOAD_CHECKSUM_ERROR:** Payload checksum (CRC) error
1	0h RW	**MULTIPLE_PH_ERROR_DETECTED:** Multiple packet header errors detected
0	0h RW	**SINGLE_PH_ERROR_CORRECTED:** Single packet header error corrected

24.2.24 (csi2_pipe_a_irq_ctrl_pipe_irq_status)—Offset 308h

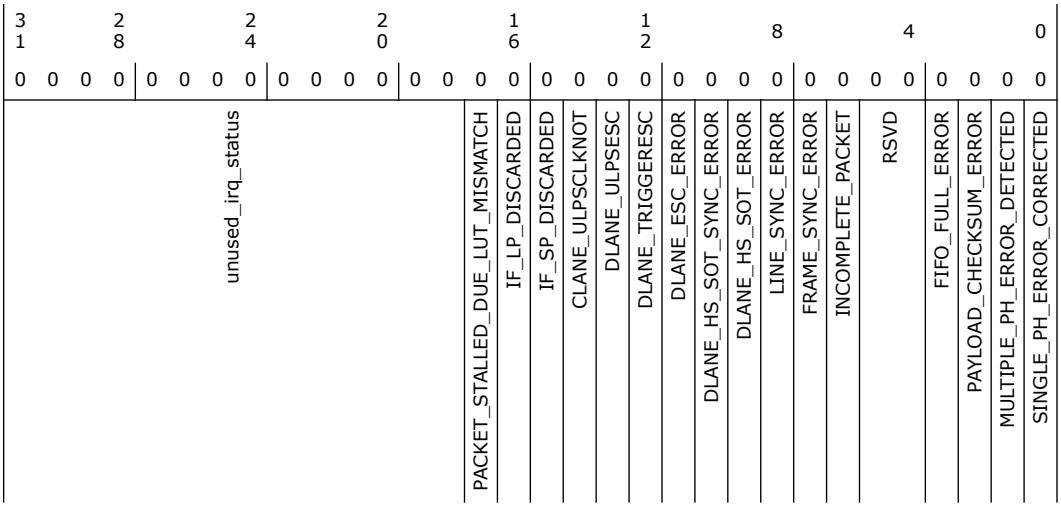
IRQ status for each unmasked interrupt

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**unused_irq_status:** Unused
17	0h RO	**PACKET_STALLED_DUE_LUT_MISMATCH:** Inter-frame long packet discarded
16	0h RO	**IF_LP_DISCARDED:** Inter-frame long packet discarded
15	0h RO	**IF_SP_DISCARDED:** Inter-frame short packet discarded
14	0h RO	**CLANE_ULPSCLKNOT:** Escape mode ultra-low power state exit for clock lane
13	0h RO	**DLANE_ULPSESC:** Escape mode ultra-low power state for data lane(s)

Bit Range	Default & Access	Field Name (ID): Description
12	0h RO	**DLANE_TRIGGERESC:** Escape mode trigger event
11	0h RO	**DLANE_ESC_ERROR:** Escape mode error
10	0h RO	**DLANE_HS_SOT_SYNC_ERROR:** DPHY synchronization error
9	0h RO	**DLANE_HS_SOT_ERROR:** DPHY start of transmission error
8	0h RO	**LINE_SYNC_ERROR:** Line sync error
7	0h RO	**FRAME_SYNC_ERROR:** Frame sync error
6	0h RO	**INCOMPLETE_PACKET:** Incomplete long packet detected
5:4	0h RO	Reserved.
3	0h RO	**FIFO_FULL_ERROR:** Fifo overflow
2	0h RO	**PAYLOAD_CHECKSUM_ERROR:** Payload checksum (CRC) error
1	0h RO	**MULTIPLE_PH_ERROR_DETECTED:** Multiple packet header errors detected
0	0h RO	**SINGLE_PH_ERROR_CORRECTED:** Single packet header error corrected

24.2.25 (csi2_pipe_a_irq_ctrl_pipe_irq_clear)—Offset 30Ch

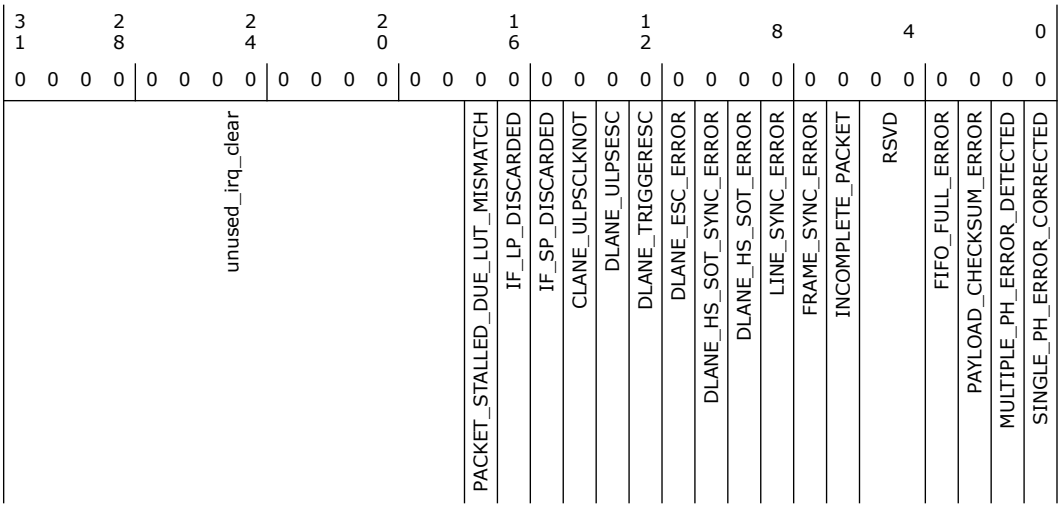
IRQ clear for interrupt set in irq_status

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**unused_irq_clear:** Unused
17	0h WO	**PACKET_STALLED_DUE_LUT_MISMATCH:** Inter-frame long packet discarded
16	0h WO	**IF_LP_DISCARDED:** Inter-frame long packet discarded
15	0h WO	**IF_SP_DISCARDED:** Inter-frame short packet discarded
14	0h WO	**CLANE_ULPSCLKNOT:** Escape mode ultra-low power state exit for clock lane
13	0h WO	**DLANE_ULPSESC:** Escape mode ultra-low power state for data lane(s)
12	0h WO	**DLANE_TRIGGERESC:** Escape mode trigger event
11	0h WO	**DLANE_ESC_ERROR:** Escape mode error
10	0h WO	**DLANE_HS_SOT_SYNC_ERROR:** DPHY synchronization error
9	0h WO	**DLANE_HS_SOT_ERROR:** DPHY start of transmission error
8	0h WO	**LINE_SYNC_ERROR:** Line sync error
7	0h WO	**FRAME_SYNC_ERROR:** Frame sync error
6	0h WO	**INCOMPLETE_PACKET:** Incomplete long packet detected
5:4	0h RO	Reserved.
3	0h WO	**FIFO_FULL_ERROR:** Fifo overflow

Bit Range	Default & Access	Field Name (ID): Description
2	0h WO	**PAYLOAD_CHECKSUM_ERROR:** Payload checksum (CRC) error
1	0h WO	**MULTIPLE_PH_ERROR_DETECTED:** Multiple packet header errors detected
0	0h WO	**SINGLE_PH_ERROR_CORRECTED:** Single packet header error corrected

24.2.26 (csi2_pipe_a_irq_ctrl_pipe_irq_en)—Offset 310h

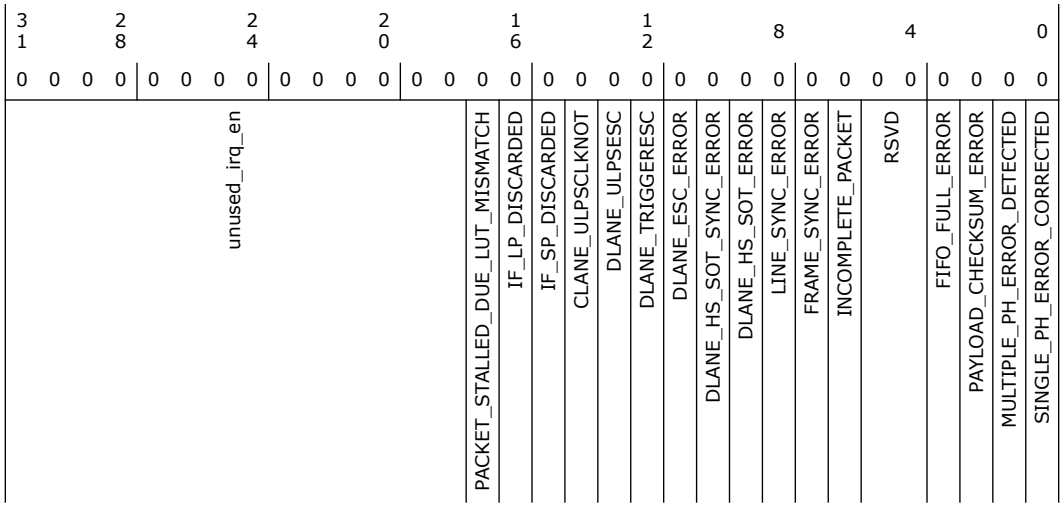
IRQ enable per interrupt bit

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**unused_irq_en:** Unused
17	0h RW	**PACKET_STALLED_DUE_LUT_MISMATCH:** Inter-frame long packet discarded
16	0h RW	**IF_LP_DISCARDED:** Inter-frame long packet discarded
15	0h RW	**IF_SP_DISCARDED:** Inter-frame short packet discarded
14	0h RW	**CLANE_ULPSCLKNOT:** Escape mode ultra-low power state exit for clock lane
13	0h RW	**DLANE_ULPSESC:** Escape mode ultra-low power state for data lane(s)

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW	**DLANE_TRIGGERESC:** Escape mode trigger event
11	0h RW	**DLANE_ESC_ERROR:** Escape mode error
10	0h RW	**DLANE_HS_SOT_SYNC_ERROR:** DPHY synchronization error
9	0h RW	**DLANE_HS_SOT_ERROR:** DPHY start of transmission error
8	0h RW	**LINE_SYNC_ERROR:** Line sync error
7	0h RW	**FRAME_SYNC_ERROR:** Frame sync error
6	0h RW	**INCOMPLETE_PACKET:** Incomplete long packet detected
5:4	0h RO	Reserved.
3	0h RW	**FIFO_FULL_ERROR:** Fifo overflow
2	0h RW	**PAYLOAD_CHECKSUM_ERROR:** Payload checksum (CRC) error
1	0h RW	**MULTIPLE_PH_ERROR_DETECTED:** Multiple packet header errors detected
0	0h RW	**SINGLE_PH_ERROR_CORRECTED:** Single packet header error corrected

24.2.27 (csi2_pipe_a_irq_ctrl_pipe_irq_level_not_pulse)—Offset 314h

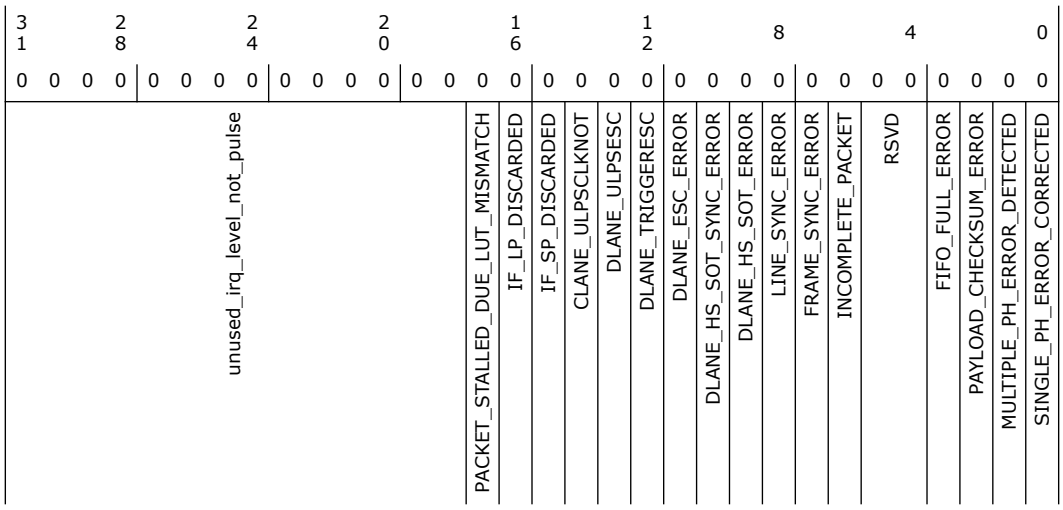
IRQ setting per interrupt bit for level or pulse irq generation at output pin. Level: 1, Pulse: 0

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**unused_irq_level_not_pulse:** Unused
17	0h RW	**PACKET_STALLED_DUE_LUT_MISMATCH:** Inter-frame long packet discarded
16	0h RW	**IF_LP_DISCARDED:** Inter-frame long packet discarded
15	0h RW	**IF_SP_DISCARDED:** Inter-frame short packet discarded
14	0h RW	**CLANE_ULPSCLKNOT:** Escape mode ultra-low power state exit for clock lane
13	0h RW	**DLANE_ULPSESC:** Escape mode ultra-low power state for data lane(s)
12	0h RW	**DLANE_TRIGGERESC:** Escape mode trigger event
11	0h RW	**DLANE_ESC_ERROR:** Escape mode error
10	0h RW	**DLANE_HS_SOT_SYNC_ERROR:** DPHY synchronization error
9	0h RW	**DLANE_HS_SOT_ERROR:** DPHY start of transmission error
8	0h RW	**LINE_SYNC_ERROR:** Line sync error
7	0h RW	**FRAME_SYNC_ERROR:** Frame sync error
6	0h RW	**INCOMPLETE_PACKET:** Incomplete long packet detected
5:4	0h RO	Reserved.
3	0h RW	**FIFO_FULL_ERROR:** Fifo overflow

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**PAYLOAD_CHECKSUM_ERROR:** Payload checksum (CRC) error
1	0h RW	**MULTIPLE_PH_ERROR_DETECTED:** Multiple packet header errors detected
0	0h RW	**SINGLE_PH_ERROR_CORRECTED:** Single packet header error corrected

24.2.28 (gpreg_dev_soft_reset_reg)—Offset 1000h

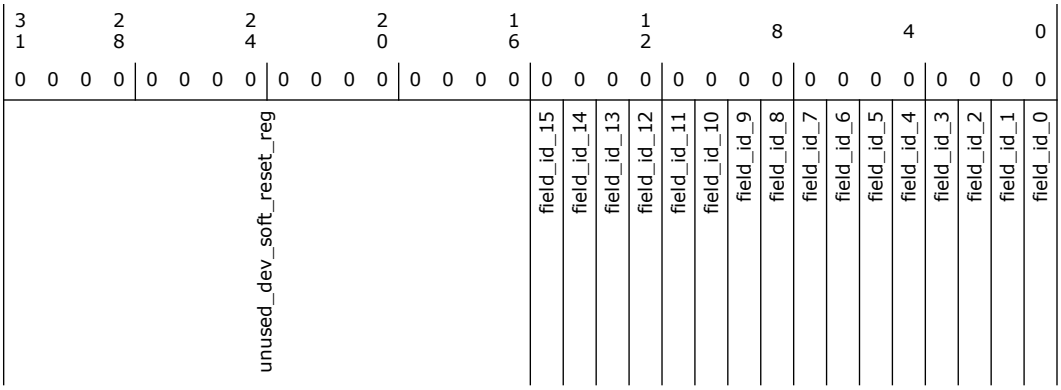
Device soft reset register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**unused_dev_soft_reset_reg:** Unused
15	0h RW	**field_id_15:** softreset stream mux pipe D
14	0h RW	**field_id_14:** softreset pixel generator pipe D
13	0h RW	**field_id_13:** softreset MIPI backend pipe D (pkt2pix)
12	0h RW	**field_id_12:** softreset MIPI frontend pipe D (dphy + csi_rx)
11	0h RW	**field_id_11:** softreset stream mux pipe C
10	0h RW	**field_id_10:** softreset pixel generator pipe C

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**field_id_9:** softreset MIPI backend pipe C (pkt2pix)
8	0h RW	**field_id_8:** softreset MIPI frontend pipe C (dphy + csi_rx)
7	0h RW	**field_id_7:** softreset stream mux pipe B
6	0h RW	**field_id_6:** softreset pixel generator pipe B
5	0h RW	**field_id_5:** softreset MIPI backend pipe B (pkt2pix)
4	0h RW	**field_id_4:** softreset MIPI frontend pipe B (dphy + csi_rx)
3	0h RW	**field_id_3:** softreset stream mux pipe A
2	0h RW	**field_id_2:** softreset pixel generator pipe A
1	0h RW	**field_id_1:** softreset MIPI backend pipe A (pkt2pix)
0	0h RW	**field_id_0:** softreset MIPI frontend pipe A (dphy + csi_rx)

24.2.29 (gpreg_slv_soft_reset_reg)—Offset 1004h

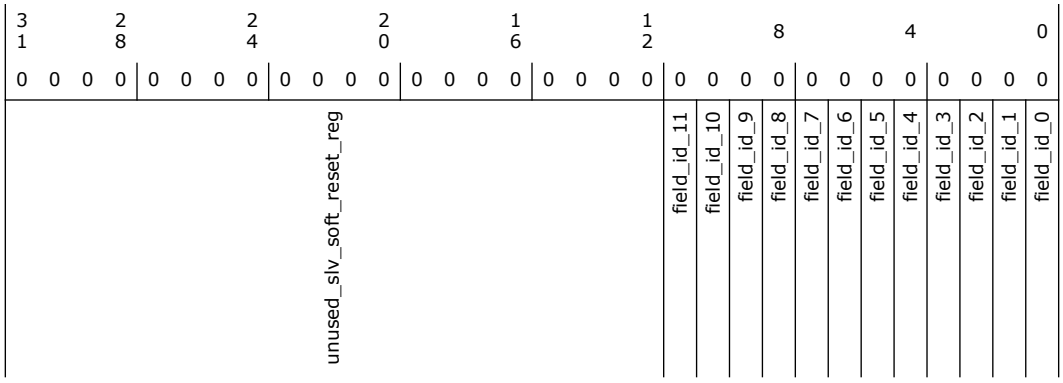
Device configuration soft reset register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**unused_slv_soft_reset_reg:** Unused
11	0h RW	**field_id_11:** softreset configuration registers pixel generator pipe D (dphy + csi_rx)
10	0h RW	**field_id_10:** softreset configuration registers MIPI backend pipe D (dphy + csi_rx)
9	0h RW	**field_id_9:** softreset configuration registers MIPI frontend pipe D (dphy + csi_rx)
8	0h RW	**field_id_8:** softreset configuration registers pixel generator pipe C (dphy + csi_rx)
7	0h RW	**field_id_7:** softreset configuration registers MIPI backend pipe C (dphy + csi_rx)
6	0h RW	**field_id_6:** softreset configuration registers MIPI frontend pipe C (dphy + csi_rx)
5	0h RW	**field_id_5:** softreset configuration registers pixel generator pipe B (dphy + csi_rx)
4	0h RW	**field_id_4:** softreset configuration registers MIPI backend pipe B (dphy + csi_rx)
3	0h RW	**field_id_3:** softreset configuration registers MIPI frontend pipe B (dphy + csi_rx)
2	0h RW	**field_id_2:** softreset configuration registers pixel generator pipe A (dphy + csi_rx)
1	0h RW	**field_id_1:** softreset configuration registers MIPI backend pipe A (dphy + csi_rx)
0	0h RW	**field_id_0:** softreset configuration registers MIPI frontend pipe A (dphy + csi_rx)

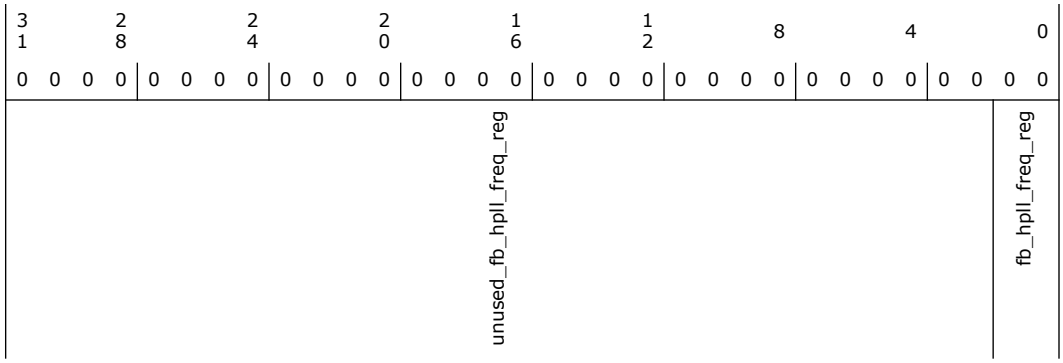
24.2.30 (gpreg_fb_hpll_freq_reg)—Offset 1008h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**unused_fb_hpll_freq_reg:** Unused
1:0	0h RW	**fb_hpll_freq_reg:** hpll frequency setting

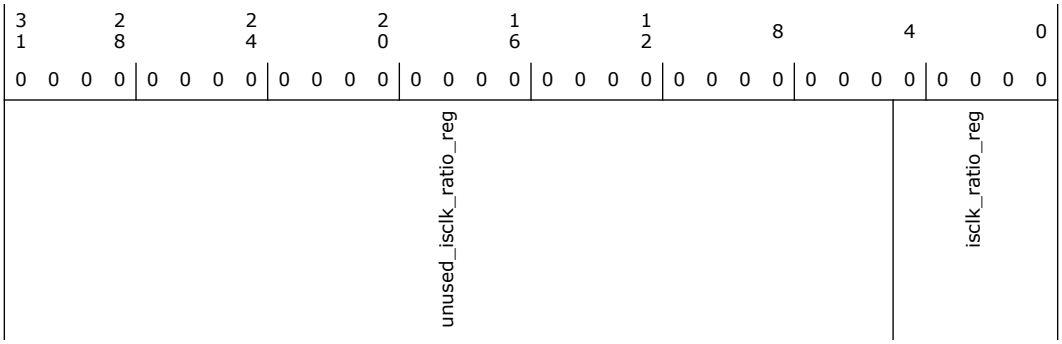
24.2.31 (gpreg_isclk_ratio_reg)—Offset 100Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**unused_isclk_ratio_reg:** Unused
4:0	0h RW	**isclk_ratio_reg:** isclk ratio setting

24.3 Camera CSI2 Host Controller MMIO 1 Registers Summary

Camera Pipe Host Controller's MMIO registers in Primary clock domain

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
1400h	1403h	CIO2_CGC (CIO2_CGC)—Offset 1400h	5300020h
1404h	1407h	CIO2_PGC (CIO2_PGC)—Offset 1404h	56996330h
1408h	140Bh	CIO2_D0I3C (CIO2_D0I3C)—Offset 1408h	8h
140Ch	140Fh	SWReset (SWReset)—Offset 140Ch	0h
1410h	1413h	CSI2_SENSOR_ACTIVE (CSI2_SENSOR_ACTIVE)—Offset 1410h	0h

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
1414h	1417h	INT Status (INT_STS)—Offset 1414h	0h
1418h	141Bh	INT_STS_EXT_OE (INT_STS_EXT_OE)—Offset 1418h	0h
1420h	1423h	INT_EN (INT_EN)—Offset 1420h	0h
1424h	1427h	INT_EN_EXT_OE (INT_EN_EXT_OE)—Offset 1424h	0h
1428h	142Bh	RCOMPCtrl (RCOMPCtrl)—Offset 1428h	1h
1430h	1433h	PCE (PCE)—Offset 1430h	9h
1444h	1447h	MMIO_RID (MMIO_RID)—Offset 1444h	0h
1500h	1503h	Frame Buffer Pointer Table base address (CDMABA[19:0])—Offset 1500h	0h
1504h	1507h	DMA Read Index Register (CDMARI[19:0])—Offset 1504h	0h
1508h	150Bh	CIO2 DMA Control (CDMAC0[19:0])—Offset 1508h	80000000h
150Ch	150Fh	CIO2 DMA Control Register1 (CDMAC1[19:0])—Offset 150Ch	0h

24.3.1 CIO2_CGC (CIO2_CGC)—Offset 1400h

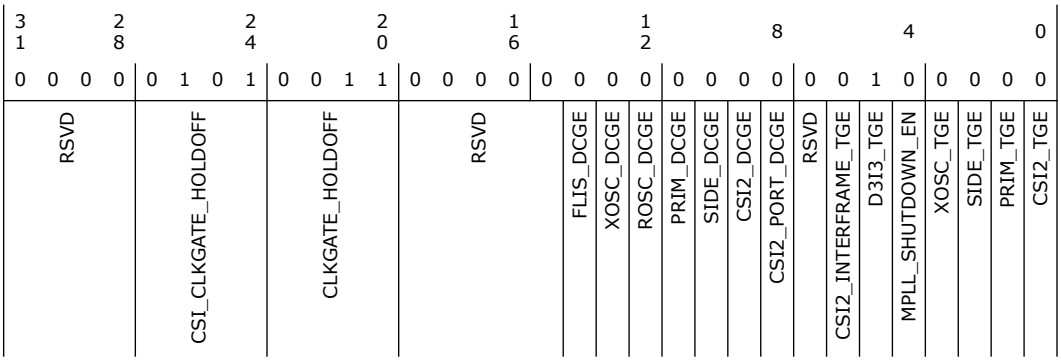
CIO2 Clock Gating Control

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 5300020h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	Reserved.
27:24	5h RW	**CSI_CLKGATE_HOLDOFF (CSI_CLKGATE_HOLDOFF):** Minimum time from the CSI2 CDC detects all clock reqs de-asserted until clock is gated. The actual count is 2^value. For example setting this register to 5 would result in a hold-off time of 32 clock cycles
23:20	3h RW	**CLKGATE_HOLDOFF (CLKGATE_HOLDOFF):** Minimum time from the PRIM/SIDE/ XOSC CDC detects all clock reqs de-asserted until clock is gated. The actual count is 2^value. For example setting this register to 5 would result in a hold-off time of 32 clock cycles

Bit Range	Default & Access	Field Name (ID): Description
19:15	0h RO	Reserved.
14	0h RW	**FLIS_DCGE (FLIS_DCGE):** FLIS Dynamic Gating Enable
13	0h RW	**XOSC_DCGE (XOSC_DCGE):** XTAL OSC Dynamic Gating Enable
12	0h RW	**ROSC_DCGE (ROSC_DCGE):** Ring OSC Dynamic Gating Enable
11	0h RW	**PRIM_DCGE (PRIM_DCGE):** prim clock Dynamic Gating Enable
10	0h RW	**SIDE_DCGE (SIDE_DCGE):** side clock Dynamic Gating Enable
9	0h RW	**CSI2_DCGE (CSI2_DCGE):** CSI2 clock Dynamic Gating Enable. Note: this bit should not be set to '1' as dynamic clock gating is not supported for CSI2 clock.
8	0h RW	**CSI2_PORT_DCGE (CSI2_PORT_DCGE):** Per port CSI2 clock Dynamic Gating Enable
7	0h RO	Reserved.
6	0h RW	**CSI2_INTERFRAME_TGE (CSI2_INTERFRAME_TGE):** When this bit is set, CSI2 clock requests are masked when PLL enable is de-asserted.
5	1h RW	**D3I3_TGE (D3I3_TGE):** This bit enables trunk-gating of all clocks in D3/D0i3. This bit overrides *_TGE bits when in D3/D0i3
4	0h RW	**MPLL_SHUTDOWN_EN (MPLL_SHUTDOWN_EN):** PLL Shut Down Enable: (MPLL_SHUTDOWN_EN) This bit, if set, enables CIO2 to request PLL to shut down
3	0h RW	**XOSC_TGE (XOSC_TGE):** XOSC Trunk Gating Enable: (XOSC_TGE) This bit enables CIO to request clock unit to trunk-gate its clock based on IDLE conditions
2	0h RW	**SIDE_TGE (SIDE_TGE):** SB Trunk Gating Enable: (SIDE_TGE) This bit enables CIO to request clock unit to trunk-gate its clock based on IDLE conditions.
1	0h RW	**PRIM_TGE (PRIM_TGE):** IOSF Fabric Trunk Gating Enable: (PRIM_TGE) This bit enables CIO to request clock unit to trunk-gate its clock based on IDLE conditions
0	0h RW	**CSI2_TGE (CSI2_TGE):** This bit enables CIO to request clock unit to trunk-gate CSI2 clock based on IDLE conditions. Note: this bit should not be set to '1' as trunk clock gating is not supported for CSI2 clock.

24.3.2 CIO2_PGC (CIO2_PGC)—Offset 1404h

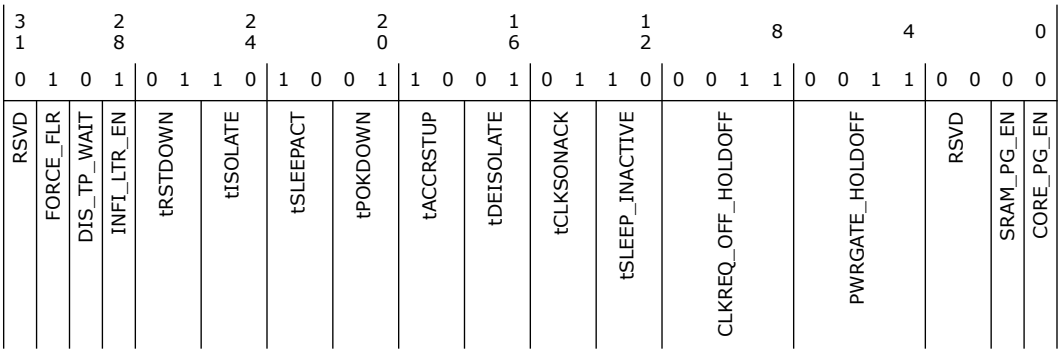
CIO2 Power Gating Control

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 56996330h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	Reserved.
30	1h RW	**FORCE_FLR (FORCE_FLR):** When set, FLR/SWReset does not wait for DMA to indicate idleness on BIU
29	0h RW	**DIS_TP_WAIT (DIS_TP_WAIT):** When set, forced power gating does not wait for no transactions pending
28	1h RW	**INFI_LTR_EN (INFI_LTR_EN):** When set, infinite latency LTR message will be sent before entry to D3/D0I3/FLR
27:26	1h RW	**tRSTDOWN (tRSTDOWN):** Delay after internal reset assertion. The decoding is: '00': 1 clock '01': 2 clocks '10': 8 clocks '11': 256 clocks
25:24	2h RW	**tISOLATE (tISOLATE):** Delay after activating isolation. The decoding is: '00': 1 clock '01': 2 clocks '10': 8 clocks '11': 256 clocks
23:22	2h RW	**tSLEEPACT (tSLEEPACT):** Delay after SLEEP assertion. The decoding is: '00': 1 clock '01': 2 clocks '10': 8 clocks '11': 256 clocks
21:20	1h RW	**tPOKDOWN (tPOKDOWN):** Delay after POK de-assertion. The decoding is: '00': 1 clock '01': 2 clocks '10': 8 clocks '11': 256 clocks
19:18	2h RW	**tACCRSTUP (tACCRSTUP):** Delay after internal Reset de-assertion. The decoding is: '00': 1 clock '01': 2 clocks '10': 8 clocks '11': 256 clocks
17:16	1h RW	**tDEISOLATE (tDEISOLATE):** Delay after isolation removal. The decoding is: '00': 1 clock '01': 2 clocks '10': 8 clocks '11': 256 clocks

Bit Range	Default & Access	Field Name (ID): Description
15:14	1h RW	**tCLKSONACK (tCLKSONACK):** Time of forcing clocks during reset. The decoding is: '00': 1 clock '01': 2 clocks '10': 8 clocks '11': 256 clocks
13:12	2h RW	**tSLEEP_INACTIVE (tSLEEP_INACTIVE):** Delay after PMC_PG_ACK de-assertion. The decoding is: '00': 1 clock '01': 2 clocks '10': 8 clocks '11': 256 clocks
11:8	3h RW	**CLKREQ_OFF_HOLDOFF (CLKREQ_OFF_HOLDOFF):** Time from locking the domain and preparing for power gating until the CDC will de-assert clkreq. The actual count is 2^value.
7:4	3h RW	**PWRGATE_HOLDOFF (PWRGATE_HOLDOFF):** Time from gating clocks until the CDC will start the lock entry and allow power gating. The actual count is 2^value
3:2	0h RO	Reserved.
1	0h RW	**spare_2 (SRAM_PG_EN):** Spare for future use
0	0h RW	**spare_1 (CORE_PG_EN):** Spare for future use

24.3.3 CIO2_D0I3C (CIO2_D0I3C)—Offset 1408h

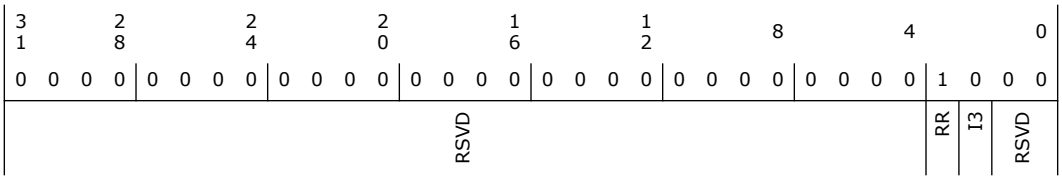
CIO2 D0i3 Control Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 8h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3	1h RW/1C	**RR (RR):** Restore Required. When set (by HW), SW must restore state to the IP. The state may have been lost due to a reset or full power loss. SW clears the bit by writing a '1'. This bit will be set on initial power up.
2	0h RW	**I3 (I3):** D0i3. SW sets this bit to '1' to move the IP into the D0i3 state. Writing this bit to '0' will return the IP to the fully active D0 state (D0i0).
1:0	0h RO	Reserved.

24.3.4 SWReset (SWReset)—Offset 140Ch

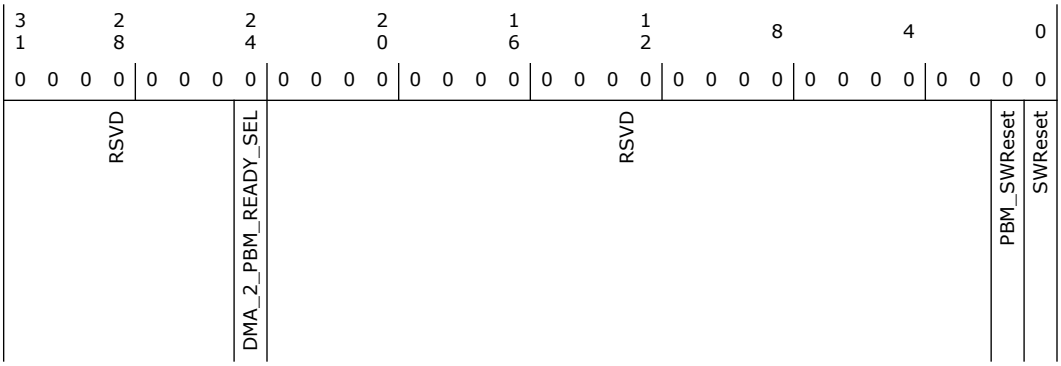
Software Reset

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	Reserved.
24	0h RW	**DMA_2_PBM_READY_SEL (DMA_2_PBM_READY_SEL):** 1- dma_ready indication to PBM resolution is 4kB (default) 0 - dma_ready indication to PBM resolution is 2kB
23:2	0h RO	Reserved.
1	0h RW/V	**Partial_SWReset (PBM_SWReset):** This bit has the same functionality as SWReset, except that all registers, including MMIO registers, does not get reset.
0	0h RW	**SWReset (SWReset):** This bit is used by CIO2 Driver to reset CIO2. The effect of this bit is similar to a Chip Hardware Reset (except Config Space and sideband Private space). When software writes a 1 to this bit, CIO2 resets its timers, counters, state machines, etc. to their initial value. PCI Configuration registers are not affected by this reset. All operational registers, are set to their initial values. This bit is cleared to 0 by CIO2 when the reset process is complete. CIO2 driver cannot terminate the reset process early by writing a 0 to this bit and shall not write to any register while CIO2 Reset is 1. The Reset is asserted for about 1uSec.

24.3.5 CSI2_SENSOR_ACTIVE (CSI2_SENSOR_ACTIVE)—Offset 1410h

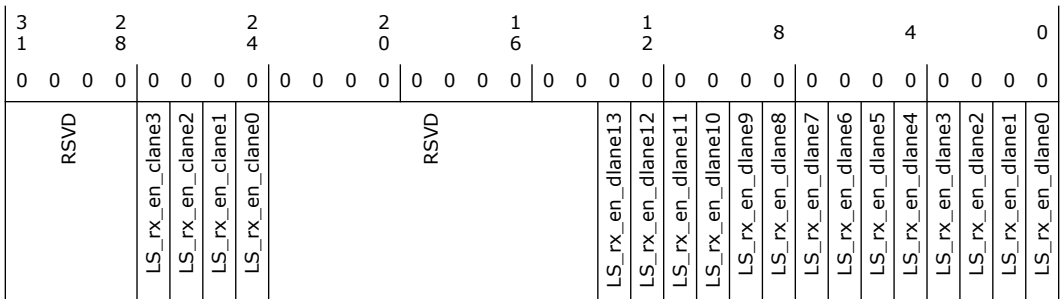
DPHY Port/Lane enable

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	Reserved.
27	0h RO/V	**LS_rx_en_clane3 (LS_rx_en_clane3)**
26	0h RO/V	**LS_rx_en_clane2 (LS_rx_en_clane2)**
25	0h RO/V	**LS_rx_en_clane1 (LS_rx_en_clane1)**
24	0h RO/V	**LS_rx_en_clane0 (LS_rx_en_clane0)**
23:14	0h RO	Reserved.
13	0h RO/V	**LS_rx_en_dlane13 (LS_rx_en_dlane13)**
12	0h RO/V	**LS_rx_en_dlane12 (LS_rx_en_dlane12)**
11	0h RO/V	**LS_rx_en_dlane11 (LS_rx_en_dlane11)**
10	0h RO/V	**LS_rx_en_dlane10 (LS_rx_en_dlane10)**
9	0h RO/V	**LS_rx_en_dlane9 (LS_rx_en_dlane9)**
8	0h RO/V	**LS_rx_en_dlane8 (LS_rx_en_dlane8)**
7	0h RO/V	**LS_rx_en_dlane7 (LS_rx_en_dlane7)**
6	0h RO/V	**LS_rx_en_dlane6 (LS_rx_en_dlane6)**
5	0h RO/V	**LS_rx_en_dlane5 (LS_rx_en_dlane5)**
4	0h RO/V	**LS_rx_en_dlane4 (LS_rx_en_dlane4)**
3	0h RO/V	**LS_rx_en_dlane3 (LS_rx_en_dlane3)**

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO/V	**LS_rx_en_dlane2 (LS_rx_en_dlane2)**
1	0h RO/V	**LS_rx_en_dlane1 (LS_rx_en_dlane1)**
0	0h RO/V	**LS_rx_en_dlane0 (LS_rx_en_dlane0)**

24.3.6 INT Status (INT_STS)—Offset 1414h

CIO2 Interrupt Status - same as IMGU INT Status in Hidden Device mode

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD							IOIRQ	IOOE	IOIE	IOSLN1819	IOSLN1617	IOSLN1415	IOSLN1213	IOSLN1011	IOSLN89	IOSLN67	IOSLN45	IOSLN23	IOSLN01	IOC1819	IOC1617	IOC1415	IOC1213	IOC1011	IOC89	IOC67	IOC45	IOC3	IOC2	IOC1	IOC0

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	Reserved.
24	0h RW/1C/V	**Interrupt on IRQ (IOIRQ):** This is interrupt from the CSI2 core. For interrupt cause SW can find the Sensor asserting the IRQ in the INT_STS_EXT_IE register bits 31/23/15/7. Than it should read CSI2 register IRQ_STATUS in the specific Sensor. IOIRQ bit will only be set when SW enables the specific cause using CSI2 register IRQ_ENABLE register. for clearing IOIRQ status SW should 1st clear the cause in IRQ_STATUS register
23	0h RW/1C/V	**Interrupt on Output Error (IOOE):** This interrupt will be set in the following scenarios: 1) SRAM is full and a FS is received w/o ability to write it. Set by InMgr 2) An in-Valid bit detected by DMA. SW can read INT_STS_EXT_OE register in order to figure out which DMA caused the error or if it was InMgr (SRAM full). In order to clear the IOIE bit, SW should 1st clear the cause in INT_STS_EXT_OE register
22	0h RW/1C/V	**Interrupt on Input Error (IOIE):** This bit is set when enabled input error occurs. In order to find the specific Sensor and specific cause SW should read the INT_STS_EXT_IE register. In order to clear the IOIE bit, SW should 1st clear the cause in INT_STS_EXT_IE register
21	0h RW/1C/V	**IOS/IOLN for DMA18 or DMA19 (IOSLN1819):** IOS/IOLN for DMAs 18 or 19
20	0h RW/1C/V	**IOS/IOLN for DMA16 or DMA17 (IOSLN1617):** IOS/IOLN for DMAs 16 or 17
19	0h RW/1C/V	**IOS/IOLN for DMA14 or DMA15 (IOSLN1415):** IOS/IOLN for DMAs 14 or 15

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW/1C/V	**IOS/IOLN for DMA12 or DMA13 (IOSLN1213):** IOS/IOLN for DMAs 12 or 13
17	0h RW/1C/V	**IOS/IOLN for DMA10 or DMA11 (IOSLN1011):** IOS/IOLN for DMAs 10 or 11
16	0h RW/1C/V	**IOS/IOLN for DMA8 or DMA9 (IOSLN89):** IOS/IOLN for DMAs 8 or 9
15	0h RW/1C/V	**IOS/IOLN for DMA6 or DMA7 (IOSLN67):** IOS/IOLN for DMAs 6 or 7
14	0h RW/1C/V	**IOS/IOLN for DMA4 or DMA5 (IOSLN45):** IOS/IOLN for DMAs 4 or 5
13	0h RW/1C/V	**IOS/IOLN for DMA2 or DMA3 (IOSLN23):** IOS/IOLN for DMAs 2 or 3
12	0h RW/1C/V	**IOS/IOLN for DMA0 or DMA1 (IOSLN01):** IOS/IOLN for DMAs 0 or 1
11	0h RW/1C/V	**IOC for DMA18 or DMA19 (IOC1819):** Interrupt on completion (Frame End pushed to DRAM). Generated only if IOC bit is set in the DMA registers AND in FBPT per the specific buffer (it is possible that SW will request an INT every second buffer for example)
10	0h RW/1C/V	**IOC for DMA16 or DMA17 (IOC1617):** Interrupt on completion (Frame End pushed to DRAM). Generated only if IOC bit is set in the DMA registers AND in FBPT per the specific buffer (it is possible that SW will request an INT every second buffer for example)
9	0h RW/1C/V	**IOC for DMA14 or DMA15 (IOC1415):** Interrupt on completion (Frame End pushed to DRAM). Generated only if IOC bit is set in the DMA registers AND in FBPT per the specific buffer (it is possible that SW will request an INT every second buffer for example)
8	0h RW/1C/V	**IOC for DMA12 or DMA13 (IOC1213):** Interrupt on completion (Frame End pushed to DRAM). Generated only if IOC bit is set in the DMA registers AND in FBPT per the specific buffer (it is possible that SW will request an INT every second buffer for example)
7	0h RW/1C/V	**IOC for DMA10 or DMA11 (IOC1011):** Interrupt on completion (Frame End pushed to DRAM). Generated only if IOC bit is set in the DMA registers AND in FBPT per the specific buffer (it is possible that SW will request an INT every second buffer for example)
6	0h RW/1C/V	**IOC for DMA8 or DMA9 (IOC89):** Interrupt on completion (Frame End pushed to DRAM). Generated only if IOC bit is set in the DMA registers AND in FBPT per the specific buffer (it is possible that SW will request an INT every second buffer for example)
5	0h RW/1C/V	**IOC for DMA6 or DMA7 (IOC67):** Interrupt on completion (Frame End pushed to DRAM). Generated only if IOC bit is set in the DMA registers AND in FBPT per the specific buffer (it is possible that SW will request an INT every second buffer for example)
4	0h RW/1C/V	**IOC for DMA4 or DMA5 (IOC45):** Interrupt on completion (Frame End pushed to DRAM). Generated only if IOC bit is set in the DMA registers AND in FBPT per the specific buffer (it is possible that SW will request an INT every second buffer for example)
3	0h RW/1C/V	**IOC for DMA3 (IOC3):** Interrupt on completion (Frame End pushed to DRAM). Generated only if IOC bit is set in the DMA registers AND in FBPT per the specific buffer (it is possible that SW will request an INT every second buffer for example)
2	0h RW/1C/V	**IOC for DMA2 (IOC2):** Interrupt on completion (Frame End pushed to DRAM). Generated only if IOC bit is set in the DMA registers AND in FBPT per the specific buffer (it is possible that SW will request an INT every second buffer for example)
1	0h RW/1C/V	**IOC for DMA1 (IOC1):** Interrupt on completion (Frame End pushed to DRAM). Generated only if IOC bit is set in the DMA registers AND in FBPT per the specific buffer (it is possible that SW will request an INT every second buffer for example)
0	0h RW/1C/V	**IOC for DMA0 (IOC0):** Interrupt on completion (Frame End pushed to DRAM). Generated only if IOC bit is set in the DMA registers AND in FBPT per the specific buffer (it is possible that SW will request an INT every second buffer for example)

24.3.7 INT_STS_EXT_OE (INT_STS_EXT_OE)—Offset 1418h

CIO2 Interrupt Status Extended for Output Error. SW reads this register if IOOE bit was asserted in the INT_STS register to find out the cause of the interrupt.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
TSWrapAround	RSVD			OES3	OES02	OES1	OES0	RSVD				DMA19OE	DMA18OE	DMA17OE	DMA16OE	DMA15OE	DMA14OE	DMA13OE	DMA12OE	DMA11OE	DMA10OE	DMA9OE	DMA8OE	DMA7OE	DMA6OE	DMA5OE	DMA4OE	DMA3OE	DMA2OE	DMA1OE	DMA0OE

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C/V	**TimeStamp timer wrap-around (TSWrapAround):** This is not an error but an indication to the SW that the TimeStamp counter has wrapped around
30:28	0h RO	Reserved.
27	0h RW/1C/V	**Output error from InMgr from Sensor3 (OES3):** Output error in-between frames – issued by InMgr when SRAM is full and FS arrives when no frame is open (after FE).
26	0h RW/1C/V	**Output error from InMgr from Sensor2 (OES02):** Output error in-between frames – issued by InMgr when SRAM is full and FS arrives when no frame is open (after FE).
25	0h RW/1C/V	**Output error from InMgr from Sensor1 (OES1):** Output error in-between frames – issued by InMgr when SRAM is full and FS arrives when no frame is open (after FE).
24	0h RW/1C/V	**Output error from InMgr from Sensor0 (OES0):** Output error in-between frames – issued by InMgr when SRAM is full and FS arrives when no frame is open (after FE).
23:20	0h RO	Reserved.
19	0h RW/1C/V	**DMA19 Output Error (DMA19OE):** This bit will be set when the DMA reads FBPT with valid bit unset.
18	0h RW/1C/V	**DMA18 Output Error (DMA18OE):** This bit will be set when the DMA reads FBPT with valid bit unset.
17	0h RW/1C/V	**DMA17 Output Error (DMA17OE):** This bit will be set when the DMA reads FBPT with valid bit unset.
16	0h RW/1C/V	**DMA16 Output Error (DMA16OE):** This bit will be set when the DMA reads FBPT with valid bit unset.
15	0h RW/1C/V	**DMA15 Output Error (DMA15OE):** This bit will be set when the DMA reads FBPT with valid bit unset.
14	0h RW/1C/V	**DMA14 Output Error (DMA14OE):** This bit will be set when the DMA reads FBPT with valid bit unset.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW/1C/V	**DMA13 Output Error (DMA13OE):** This bit will be set when the DMA reads FBPT with valid bit unset.
12	0h RW/1C/V	**DMA12 Output Error (DMA12OE):** This bit will be set when the DMA reads FBPT with valid bit unset.
11	0h RW/1C/V	**DMA11 Output Error (DMA11OE):** This bit will be set when the DMA reads FBPT with valid bit unset.
10	0h RW/1C/V	**DMA10 Output Error (DMA10OE):** This bit will be set when the DMA reads FBPT with valid bit unset.
9	0h RW/1C/V	**DMA9 Output Error (DMA9OE):** This bit will be set when the DMA reads FBPT with valid bit unset.
8	0h RW/1C/V	**DMA8 Output Error (DMA8OE):** This bit will be set when the DMA reads FBPT with valid bit unset.
7	0h RW/1C/V	**DMA7 Output Error (DMA7OE):** This bit will be set when the DMA reads FBPT with valid bit unset.
6	0h RW/1C/V	**DMA6 Output Error (DMA6OE):** This bit will be set when the DMA reads FBPT with valid bit unset.
5	0h RW/1C/V	**DMA5 Output Error (DMA5OE):** This bit will be set when the DMA reads FBPT with valid bit unset.
4	0h RW/1C/V	**DMA4 Output Error (DMA4OE):** This bit will be set when the DMA reads FBPT with valid bit unset.
3	0h RW/1C/V	**DMA3 Output Error (DMA3OE):** This bit will be set when the DMA reads FBPT with valid bit unset.
2	0h RW/1C/V	**DMA2 Output Error (DMA2OE):** This bit will be set when the DMA reads FBPT with valid bit unset.
1	0h RW/1C/V	**DMA1 Output Error (DMA1OE):** This bit will be set when the DMA reads FBPT with valid bit unset.
0	0h RW/1C/V	**DMA0 Output Error (DMA0OE):** This bit will be set when the DMA reads FBPT with valid bit unset.

24.3.8 INT_EN (INT_EN)—Offset 1420h

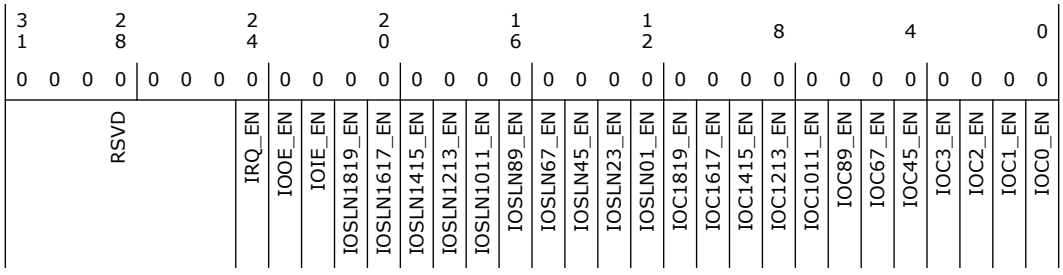
CIO2 Interrupt Enable

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	Reserved.
24	0h RW	**Interrupt on IRQ Enable (IRQ_EN)**
23	0h RW	**Interrupt on Output Error Enable (IOOE_EN)**
22	0h RW	**Interrupt on Input Error Enable (IOIE_EN)**
21	0h RW	**IOS/IOLN for DMA18 or DMA19 Enable (IOSLN1819_EN)**
20	0h RW	**IOS/IOLN for DMA16 or DMA17 Enable (IOSLN1617_EN)**
19	0h RW	**IOS/IOLN for DMA14 or DMA15 Enable (IOSLN1415_EN)**
18	0h RW	**IOS/IOLN for DMA12 or DMA13 Enable (IOSLN1213_EN)**
17	0h RW	**IOS/IOLN for DMA10 or DMA11 Enable (IOSLN1011_EN)**
16	0h RW	**IOS/IOLN for DMA8 or DMA9 Enable (IOSLN89_EN)**
15	0h RW	**IOS/IOLN for DMA6 or DMA7 Enable (IOSLN67_EN)**
14	0h RW	**IOS/IOLN for DMA4 or DMA5 Enable (IOSLN45_EN)**
13	0h RW	**IOS/IOLN for DMA2 or DMA3 Enable (IOSLN23_EN)**
12	0h RW	**IOS/IOLN for DMA0 or DMA1 Enable (IOSLN01_EN)**
11	0h RW	**IOC for DMA18 or DMA19 Enable (IOC1819_EN)**
10	0h RW	**IOC for DMA16 or DMA17 Enable (IOC1617_EN)**
9	0h RW	**IOC for DMA14 or DMA15 Enable (IOC1415_EN)**
8	0h RW	**IOC for DMA12 or DMA13 Enable (IOC1213_EN)**
7	0h RW	**IOC for DMA10 or DMA11 Enable (IOC1011_EN)**
6	0h RW	**IOC for DMA8 or DMA9 Enable (IOC89_EN)**
5	0h RW	**IOC for DMA6 or DMA7 Enable (IOC67_EN)**
4	0h RW	**IOC for DMA4 or DMA5 Enable (IOC45_EN)**
3	0h RW	**IOC for DMA3 Enable (IOC3_EN)**

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**IOC for DMA2 Enable (IOC2_EN)**
1	0h RW	**IOC for DMA1 Enable (IOC1_EN)**
0	0h RW	**IOC for DMA0 Enable (IOC0_EN)**

24.3.9 INT_EN_EXT_OE (INT_EN_EXT_OE)—Offset 1424h

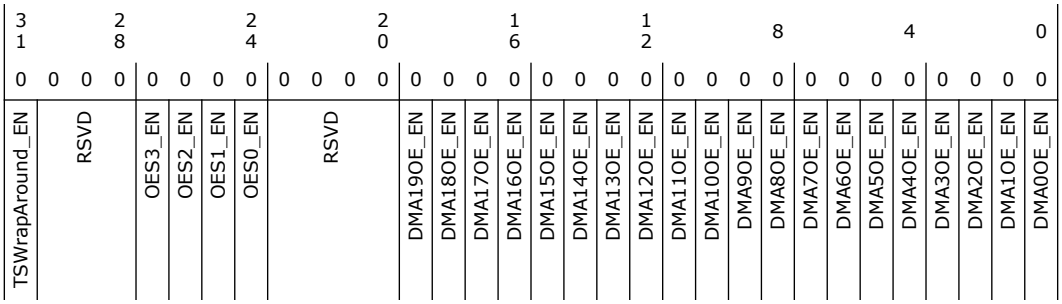
CIO2 Interrupt Status Extended for Output Error

Access Method

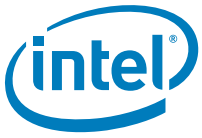
Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**TimeStamp timer wrap-around Enable (TSWrapAround_EN)**
30:28	0h RO	Reserved.
27	0h RW	**Output error from InMgr from Sensor3 Enable (OES3_EN)**
26	0h RW	**Output error from InMgr from Sensor2 Enable (OES2_EN)**
25	0h RW	**Output error from InMgr from Sensor1 Enable (OES1_EN)**
24	0h RW	**Output error from InMgr from Sensor0 Enable (OES0_EN)**
23:20	0h RO	Reserved.
19	0h RW	**DMA19 Output Error Enable (DMA19OE_EN)**
18	0h RW	**DMA18 Output Error Enable (DMA18OE_EN)**



Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**DMA17 Output Error Enable (DMA17OE_EN)**
16	0h RW	**DMA16 Output Error Enable (DMA16OE_EN)**
15	0h RW	**DMA15 Output Error Enable (DMA15OE_EN)**
14	0h RW	**DMA14 Output Error Enable (DMA14OE_EN)**
13	0h RW	**DMA13 Output Error_Enable (DMA13OE_EN)**
12	0h RW	**DMA12 Output Error Enable (DMA12OE_EN)**
11	0h RW	**DMA11 Output Error Enable (DMA11OE_EN)**
10	0h RW	**DMA10 Output Error Enable (DMA10OE_EN)**
9	0h RW	**DMA9 Output Error Enable (DMA9OE_EN)**
8	0h RW	**DMA8 Output Error Enable (DMA8OE_EN)**
7	0h RW	**DMA7 Output Error Enable (DMA7OE_EN)**
6	0h RW	**DMA6 Output Error Enable (DMA6OE_EN)**
5	0h RW	**DMA5 Output Error Enable (DMA5OE_EN)**
4	0h RW	**DMA4 Output Error Enable (DMA4OE_EN)**
3	0h RW	**DMA3 Output Error Enable (DMA3OE_EN)**
2	0h RW	**DMA2 Output Error Enable (DMA2OE_EN)**
1	0h RW	**DMA1 Output Error Enable (DMA1OE_EN)**
0	0h RW	**DMA0 Output Error Enable (DMA0OE_EN)**

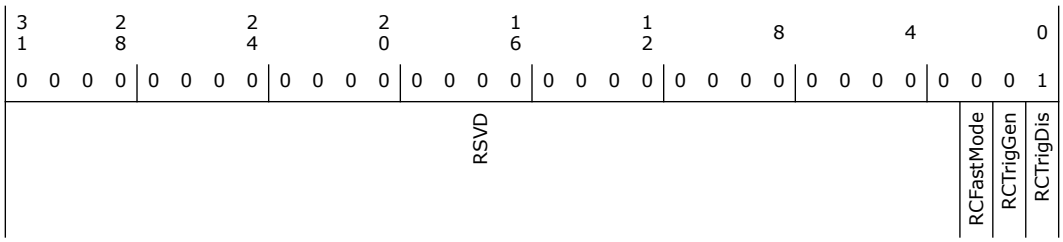
24.3.10 RCOMPCtrl (RCOMPCtrl)—Offset 1428h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 1h



Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	Reserved.
2	0h RW	**RCFastMode (RCFastMode):** When this bit is set, RCOMP period will be 5 us. This bit is for DFX purpose only
1	0h RW	**RCTrigGen (RCTrigGen):** Whenever a '1' is written to this register an RCOMP trigger pulse is sent to the AFE/FLIS. SW should clear this bit in order to send another pulse
0	1h RW	**RCTrigDis (RCTrigDis):** RCOMP Trigger Mechanism Disable 0: Enabled (default) 1: Disabled

24.3.11 PCE (PCE)—Offset 1430h

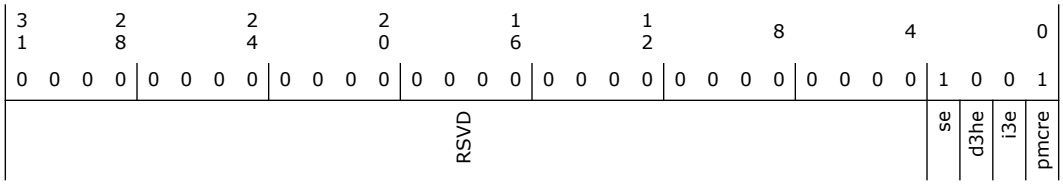
Power Control Enable Register. This register is not affected by FLR/SW reset

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 9h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3	1h RW/L	**SE: Sleep Enable (se):** If clear, then IP will never assert Sleep to the retention flops. If set, then IP may assert Sleep during PG'ing. This bit is locked when PVT_FNCFG.BCLD = 1.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/L	**D3HE: D3-Hot Enable (d3he):** If set, then IP will PG when idle and the PMCSR[1:0] register in the IP ='11'.This bit is locked when PVT_FNCFG.BCLD = 1.
1	0h RW/L	**I3E: I3 Enable (i3e):** If set, then IP will PG when idle and the D0i3 register (D0i3C[2] = '1') is set. This bit is locked when PVT_FNCFG.BCLD = 1.
0	1h RW/L	**PMCRE: PMC Request Enable (pmcre):** If set, then IP will PG when idle and the PMC requests power gating by asserting the pmc_cam_sw_pg_req_b signal. This bit is locked when PVT_FNCFG.BCLD = 1.

24.3.12 MMIO_RID (MMIO_RID)—Offset 1444h

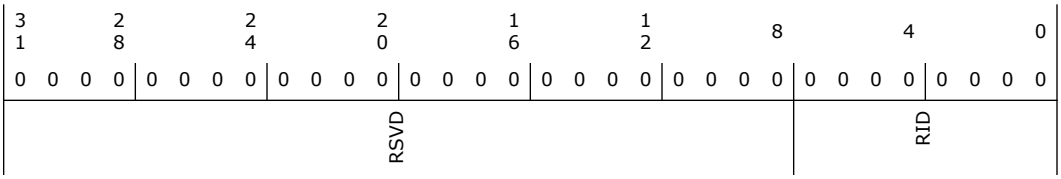
A wired reflection of the RID field in CFG_CC register.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	0h RO/V	**RID (RID):** A wired reflection of the RID field in CFG_CC register

24.3.13 Frame Buffer Pointer Table base address (CDMABA[19:0])—Offset 1500h

CIO2 DMA Base Address Register:
[0]:0X1500h
[1]:0X1510h
[2]:0X1520h
[3]:0X1530h
[4]:0X1540h
[5]:0X1550h
[6]:0X1560h
[7]:0X1570h
[8]:0X1580h
[9]:0X1590h
[10]:0X15A0h
[11]:0X15B0h
[12]:0X15C0h

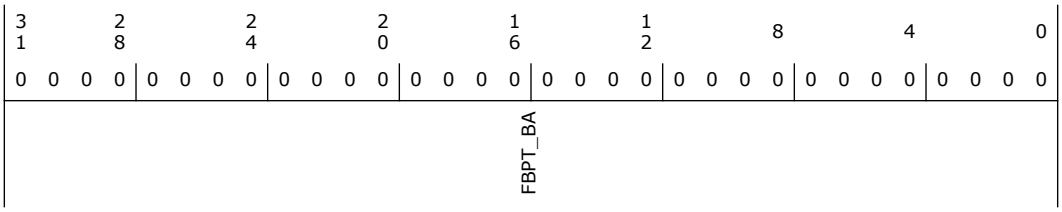
[13]:0X15D0h
[14]:0X15E0h
[15]:0X15F0h
[16]:0X1600h
[17]:0X1610h
[18]:0X1620h
[19]:0X1630h

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**FBPT_BA (FBPT_BA):** Frame Buffer Pointer Table base address index (4K aligned address). FBPT address structure is: {25'b0, FBPT_BA[26:0], 12'b0}

24.3.14 DMA Read Index Register (CDMARI[19:0])—Offset 1504h

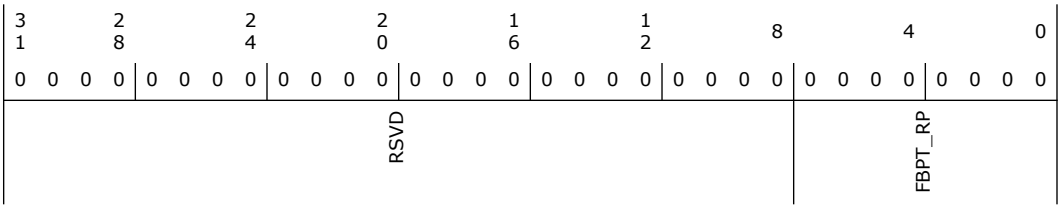
[0]:0X1504h
[1]:0X1514h
[2]:0X1524h
[3]:0X1534h
[4]:0X1544h
[5]:0X1554h
[6]:0X1564h
[7]:0X1574h
[8]:0X1584h
[9]:0X1594h
[10]:0X15A4h
[11]:0X15B4h
[12]:0X15C4h
[13]:0X15D4h
[14]:0X15E4h
[15]:0X15F4h
[16]:0X1604h
[17]:0X1614h
[18]:0X1624h
[19]:0X1634h
.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	0h RO/V	**FBPT_RP (FBPT_RP):** This indicates the HW's current read pointer for the FBPT entry

24.3.15 CIO2 DMA Control (CDMAC0[19:0])—Offset 1508h

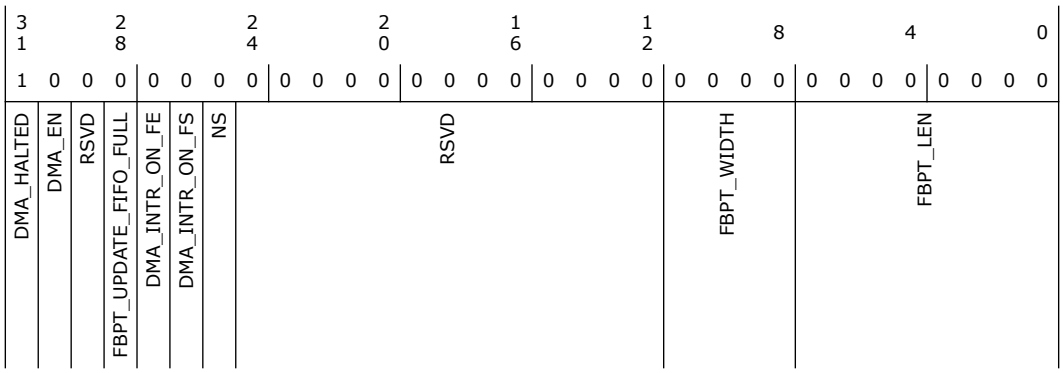
CIO2 DMA Control Register:
[0]:0X1508h
[1]:0X1518h
[2]:0X1528h
[3]:0X1538h
[4]:0X1548h
[5]:0X1558h
[6]:0X1568h
[7]:0X1578h
[8]:0X1588h
[9]:0X1598h
[10]:0X15A8h
[11]:0X15B8h
[12]:0X15C8h
[13]:0X15D8h
[14]:0X15E8h
[15]:0X15F8h
[16]:0X1608h
[17]:0X1618h
[18]:0X1628h
[19]:0X1638h

Access Method

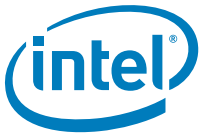
Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 80000000h



Bit Range	Default & Access	Field Name (ID): Description
31	1h RW/1C/V	**DMA_HALTED (DMA_HALTED):** This bit indicates that the DMA is halted. This bit is set by HW, if cr_dma_en is cleared and the DMA transitioned to WT4_DMA_HALTED_CLR state (SW underrun). This bit is cleared by SW. After clearing DMA_HALTED the DMA will retry to get the FBPT and look again for a Valid buffer. More details can be found at section "DMA_EN, DMA_HALTED way of operation".
30	0h RW	**DMA_EN (DMA_EN):** This bit needs to be set to enable DMA operation. If this bit is cleared by SW, during operation, this bit cannot be set again until cr_dma_halted is set by HW. When the SW sets this bit DMA starts reading the pointers (FBPT, LOP) from FBPT base address according to CDMABA register. More details can be found at section "DMA_EN, DMA_HALTED way of operation".
29	0h RO	Reserved.
28	0h RW/1C/V	**FBPT_UPDATE_FIFO_FULL (FBPT_UPDATE_FIFO_FULL):** FBPT_UPDATE_FIFO_FULL asserted when FBPT_UPDATE_FIFO_FULL event occurred. Potential missing of FBPT update. cleared by SW write 1 to this field
27	0h RW	**DMA_INTR_ON_FE (DMA_INTR_ON_FE):** IOC (Interrupt On frame Completion) - This bit enables the DMA to issue interrupts (MSIs or INTA) upon completion of the processing of an FBPT entry with IOC=1. Note that upon error conditions, interrupt generation is still governed by this bit
26	0h RW	**DMA_INTR_ON_FS (DMA_INTR_ON_FS):** IOS (Interrupt On frame Start) - This bit enables the DMA to generate an MSI/INTA upon the processing of FrameStart, for an FBPT entry with IOC=1. Note that the IOS is generated when the new frame is written into the DRAM and not when it enters the CIO2 SRAM (which accumulates the frame until there is a write trigger).
25	0h RW	**NS (NS):** Non-Snoop: marks this buffer should not be snooped – DMA will mark this with ALL the transactions to IOSF for the buffer data. All FBPT and LOP transactions are always snooped. 0: Snooped (default) 1: non-snooped



Bit Range	Default & Access	Field Name (ID): Description
24:12	0h RO	Reserved.
11:8	0h RW	**FBPT_WIDTH (FBPT_WIDTH):** Width of the FBPT entry: This indicates the size of each frames FBPT entry. This is restricted to be a multiple in units of 64B (4 sub-entries). 0000 – illegal 0001 – 4 sub entries, 64B (16MB max buffer) 0010 – 8 sub entries, 128B (32MB max buffer) 0011 – 12 sub entries 192B (48MB max buffer) 0100 – 256B width (64MB max buffer) ... 1111 – 60 sub entries, 960B (240MB max buffer)
7:0	0h RW	**FBPT_LEN (FBPT_LEN):** FBPT_LEN - Number of entries in FBPT. DMA will wrap around the last entry to entry 0. It is SW responsibility to make sure that if FBPT consume more than one page the successive pages are physically contiguous in memory to the first page. 000000 – 1 entry 000001 – 2 entries ... 111111 – 64 entries Note: If FBPT_WIDTH is 0100b, then only 16 entries can be placed in one page of FBPT. In case the driver needs wider entry, or more entries, then the FBPT would consume more than one page. All FBPT pages must be physically contiguous.

24.3.16 CIO2 DMA Control Register1 (CDMAC1[19:0])—Offset 150Ch

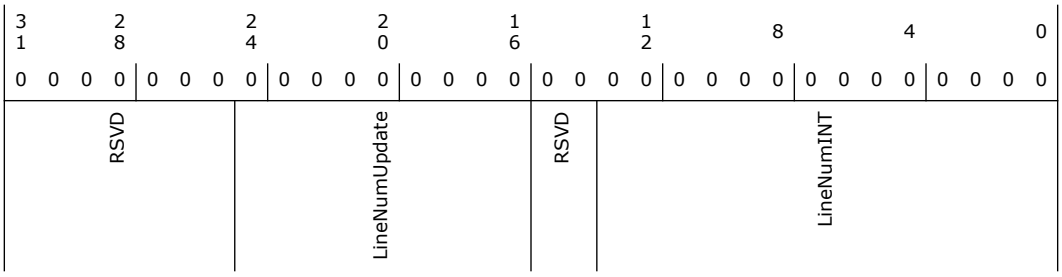
DMA Control Register1:
[0]:0X150Ch
[1]:0X151Ch
[2]:0X152Ch
[3]:0X153Ch
[4]:0X154Ch
[5]:0X155Ch
[6]:0X156Ch
[7]:0X157Ch
[8]:0X158Ch
[9]:0X159Ch
[10]:0X15ACh
[11]:0X15BCh
[12]:0X15CCh
[13]:0X15DCh
[14]:0X15ECh
[15]:0X15FCh
[16]:0X160Ch
[17]:0X161Ch
[18]:0X162Ch
[19]:0X163Ch
.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	Reserved.
24:16	0h RW	**LineNumUpdate (LineNumUpdate):** In how many lines to update the CurLineNum 0 – never update 1 – update every line 2.. – update every 2nd line, 3rd line etc.
15:14	0h RO	Reserved.
13:0	0h RW	**LineNumINT (LineNumINT):** Request to produce an INT on a specific Line Number. LineNumINT=0 means no INT is requested.

24.4 Camera CSI2 Host Controller MMIO 2 Registers Summary

Camera Pipe Host Controller's MMIO registers in CSI2 clock

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
1460h	1463h	PBM_ARB_CTRL (PBM_ARB_CTRL)—Offset 1460h	1E00200h
1464h	1467h	PBM_WMCtrl1 (PBM_WMCtrl1)—Offset 1464h	3151004h
1468h	146Bh	PBM_WMCtrl2 (PBM_WMCtrl2)—Offset 1468h	1030220h
146Ch	146Fh	PBM_TS_COUNT (PBM_TS_COUNT)—Offset 146Ch	0h
1470h	1473h	PBM_TS_SW_W (PBM_TS_SW_W)—Offset 1470h	0h
1474h	1477h	PBM_FOPN_ABORT (PBM_FOPN_ABORT)—Offset 1474h	0h
1480h	1483h	LTRCtrl (LTRCtrl)—Offset 1480h	0h
1484h	1487h	LTRVal1 (LTRVal1)—Offset 1484h	0h
1488h	148Bh	LTRVal0 (LTRVal0)—Offset 1488h	0h
148Ch	148Fh	PBM PLL and frame period (PBM_FRAME_PERIOD_S[3:0])—Offset 148Ch	40000000h
149Ch	149Fh	PBM_FLASH_CTRL (PBM_FLASH_CTRL)—Offset 149Ch	1F0000h
14A0h	14A3h	PBM_FLASH_TM_TO_TRG (PBM_FLASH_TM_TO_TRG)—Offset 14A0h	1h
14A4h	14A7h	PBM_FLASH_TRG_WDT (PBM_FLASH_TRG_WDT)—Offset 14A4h	1h
14A8h	14ABh	PBM_STS_0 (PBM_STS_0)—Offset 14A8h	0h
14ACh	14AFh	PBM_STS_1 (PBM_STS_1)—Offset 14ACh	0h
14B0h	14B3h	PBM_STS_2 (PBM_STS_2)—Offset 14B0h	0h
14B4h	14B7h	PBM_STS_3 (PBM_STS_3)—Offset 14B4h	0h

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
1700h	1703h	PXF formats configurations (PXM_PXF_FMT_Cfg0[0])—Offset 1700h	0h
1720h	1723h	PXM_FRF_cfg (PXM_FRF_cfg[3:0])—Offset 1720h	784h
1724h	1727h	Sensor0 PXM Sidebid (PXM_SID2BID[2-0]Sensor[3:0])—Offset 1724h	0h
179Ch	179Fh	PXM_PXF_FMT_Cfg3 (PXM_PXF_FMT_Cfg3[3])—Offset 179Ch	0h
17C0h	17C3h	Channel Merging (PXM_CHM)—Offset 17C0h	0h
17C4h	17C7h	Number Of CRC (PXM_CRC_S[3:0])—Offset 17C4h	0h
17C8h	17CBh	Number Of ECC (PXM_ECC_S[3:0])—Offset 17C8h	0h
17E4h	17E7h	Interrupt status for input error (INT_STS_EXT_IE)—Offset 17E4h	0h
17E8h	17EBh	Enable interrupt for input error (INT_EN_EXT_IE)—Offset 17E8h	0h

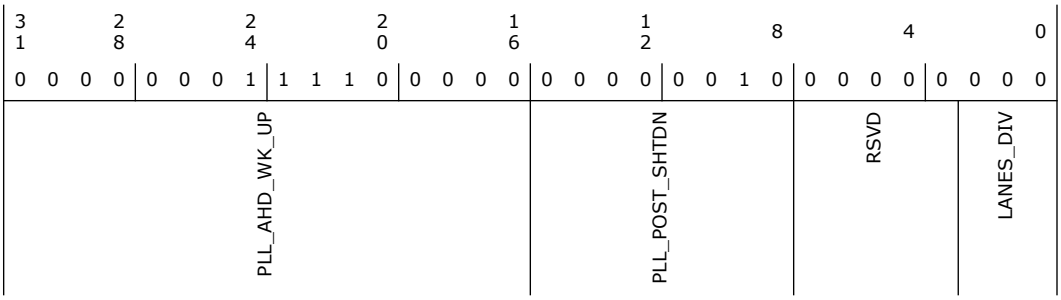
24.4.1 PBM_ARB_CTRL (PBM_ARB_CTRL)—Offset 1460h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 1E00200h



Bit Range	Default & Access	Field Name (ID): Description
31:16	1E0h RW	**PLL_AHD_WK_UP (PLL_AHD_WK_UP):** PLL Shut-Down mechanism: PLL ahead wake-up time before the next frame. Count is in 24MHz XTAL clock. Default should be equivalent to ~20uSec but accurate final value should be determined according to worst-case system parameters (~10uSec is probably enough).

Bit Range	Default & Access	Field Name (ID): Description
15:8	2h RW	**PLL_POST_SHTDN (PLL_POST_SHTDN):** PLL Shut-Down mechanism: Count in 24MHz cycles from frame closed (FrameOpen de-asserted) until PLL can be shut-down (should leave enough cycles for all pipe-line to get the frame out). Default is 10h = 16 cycles which should be enough.
7:3	0h RO	Reserved.
2:0	0h RW	**LANES_DIV (LANES_DIV):** Sensor lanes division – determines the clock division between the sensors (TDM). Sensor with 1,2,3,4 or 8 lanes need to get 4 or 8 clocks respectively The following reflects the maximum number of lanes per configuration: Sensor: // 0 1 2 3 000 // 4 4 2 2 001 // Reserved 010 // 4 4 3 1 011 // 4 4 4 0 100 // 8 0 2 2 101 // Reserved 110 // 8 0 3 1 111 // 8 0 4 0

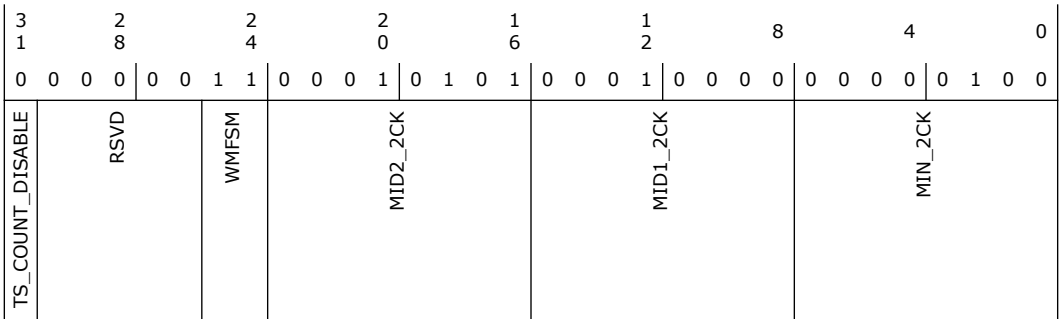
24.4.2 PBM_WMCtrl1 (PBM_WMCtrl1)—Offset 1464h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 3151004h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**TS_COUNT_DISABLE (TS_COUNT_DISABLE):** Disable the timestamp counter from counting for SV purpose.
30:26	0h RO	Reserved.
25:24	3h RO/V	**WMFSM (WMFSM):** Water Mark FSM state – the high WM used for triggering the SRAM draining. 00: Min WM 01: Mid1 WM 10: Mid2 WM 11: HWM

Bit Range	Default & Access	Field Name (ID): Description
23:16	15h RW	**MID2_2CK (MID2_2CK):** The second middle water mark for draining the SRAM, the value written to this register will be multiply by 2.
15:8	10h RW	**MID1_2CK (MID1_2CK):** The first middle water mark for draining the SRAM, the value written to this register will be multiply by 2.
7:0	4h RW	**MIN_2CK (MIN_2CK):** The minimum water mark for draining the SRAM, the value written to this register will be multiply by 2.

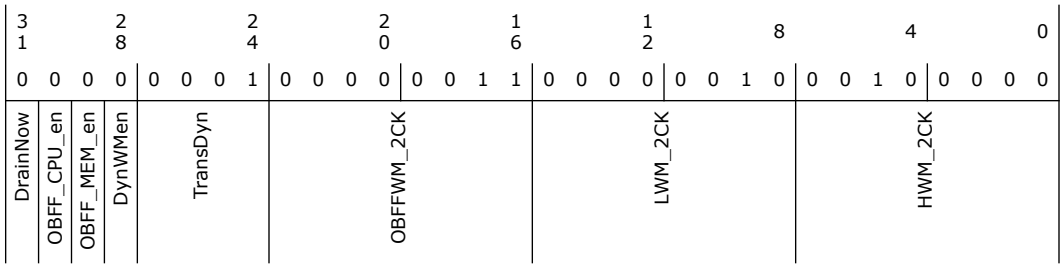
24.4.3 PBM_WMCtrl2 (PBM_WMCtrl2)—Offset 1468h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 1030220h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/V	**DrainNow (DrainNow):** SW write this bit to force immediate SRAM write to DRAM (WrTrgr), write 1'b1 to this bit will trigger drain just once if SRAM is not empty. This bit is write only.
30	0h RW	**OBFF_CPU_en (OBFF_CPU_en):** OBFF CPU bit mechanism enable. 0: disabled (default) 1: enabled When enable, the OBFF WM enabled.
29	0h RW	**OBFF_MEM_en (OBFF_MEM_en):** OBFF memory bit mechanism enable. 0: disabled (default) 1: enabled When enable, the OBFF WM enabled.
28	0h RW	**DynWMen (DynWMen):** Dynamic WM mechanism enable. 0: disabled 1: enabled When disabled, only HWM is used to drain SRAM and does not change upon error as in the dynamic WM mechanism.
27:24	1h RW	**TransDyn (TransDyn):** Represent number of good frames (w/o SRAM err) to allow raising WM after dropped due to an error (MIN=>MID1=>MID2=>HWM).

Bit Range	Default & Access	Field Name (ID): Description
23:16	3h RW	**OBFFWM_2CK (OBFFWM_2CK):** High WM on OBFF mode, this value will be multiply by 2 to get the WM chunk number, HWM Value in OBFF mode. (MIN, MID1, MID2 are ignored in this mode). Once SRAM is filled equal or over OBFFWM_2CK, drain the SRAM until empty (ignore LWM as well).
15:8	2h RW	**LWM_2CK (LWM_2CK):** Low Water Mark. Used to Send LTR message if LTR00 change to other LTRxx state and SRAM filled above LWM. Note: if the trigger for draining was FE – draining does not stop at LWM.
7:0	20h RW	**HWM_2CK (HWM_2CK):** High Water Mark in units of 2 chunks (this value will be multiply by 2). Used to trigger a write (WrTrgr signal) of the SRAM when full enough.

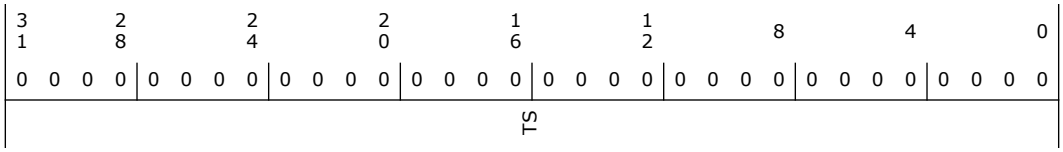
24.4.4 PBM_TS_COUNT (PBM_TS_COUNT)—Offset 146Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**TS (TS):** Time Stamp (TS): Current value of Timestamp counter. Timestamp resolution is 100nSec. Issue an interrupt (IOOE.TSWrapAround – bit31) when counter wraps around from 0xFFFFFFFF to 0.

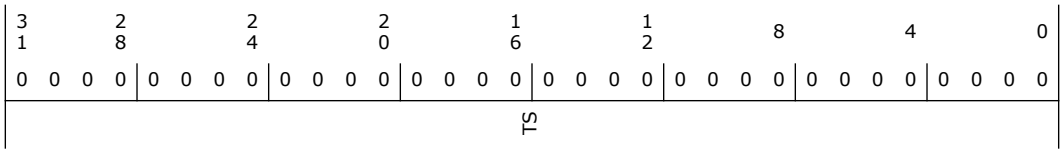
24.4.5 PBM_TS_SW_W (PBM_TS_SW_W)—Offset 1470h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**TS (TS):** Time Stamp value to be written by SW, for sync CIO2 to the system TS. Note: this register is updating the TS value on PBM_TS_COUNT.

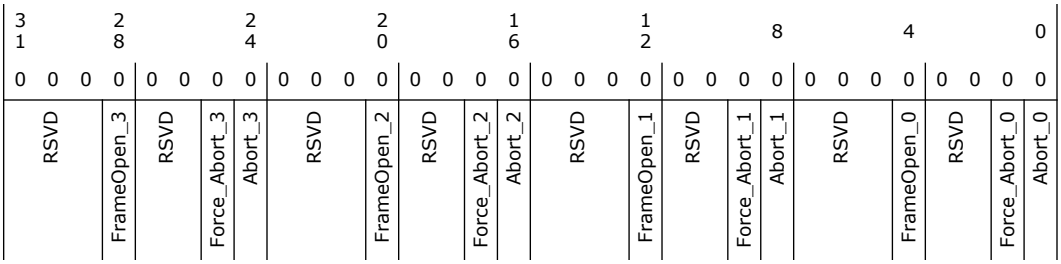
24.4.6 PBM_FOPN_ABORT (PBM_FOPN_ABORT)—Offset 1474h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	Reserved.
28	0h RO/V	**FrameOpen_3 (FrameOpen_3):** Indicate if there is any data related to the sensor 3 in the PBM/SRAM
27:26	0h RO	Reserved.
25	0h RW	**Force_Abort_3 (Force_Abort_3):** Force abort bit for sensor 3. When set to 1, all data from the sensor should be dropped from PBM/SRAM no matter if the chunk is closed. In addition, counters will be reset. Note: Force_Abort should be activated after 2.5us minimum after Abort. Note: Not planned to be used.
24	0h RW	**Abort_3 (Abort_3):** Abort bit for sensor 3. When set to 1, all data from the sensor should be dropped from PBM/SRAM.
23:21	0h RO	Reserved.
20	0h RO/V	**FrameOpen_2 (FrameOpen_2):** Indicate if there is any data related to the sensor 2 in the PBM/SRAM.
19:18	0h RO	Reserved.
17	0h RW	**Force_Abort_2 (Force_Abort_2):** Force abort bit for sensor 2. When set to 1, all data from the sensor should be dropped from PBM/SRAM no matter if the chunk is closed. In addition, counters will be reset. Note: Force_Abort should be activated after 2.5us minimum after Abort. Note: Not planned to be used.
16	0h RW	**Abort_2 (Abort_2):** Abort bit for sensor 2. When set to 1, all data from the sensor should be dropped from PBM/SRAM.
15:13	0h RO	Reserved.
12	0h RO/V	**FrameOpen_1 (FrameOpen_1):** Indicate if there is any data related to the sensor 1 in the PBM/SRAM.
11:10	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Force_Abort_1 (Force_Abort_1):** Force abort bit for sensor 1. When set to 1, all data from the sensor should be dropped from PBM/SRAM no matter if the chunk is closed. In addition, counters will be reset. Note: Force_Abort should be activated after 2.5us minimum after Abort. Note: Not planned to be used.
8	0h RW	**Abort_1 (Abort_1):** Abort bit for sensor 1. When set to 1, all data from the sensor should be dropped from PBM/SRAM.
7:5	0h RO	Reserved.
4	0h RO/V	**FrameOpen_0 (FrameOpen_0):** Indicate if there is any data related to the sensor 0 in the PBM/SRAM.
3:2	0h RO	Reserved.
1	0h RW	**Force_Abort_0 (Force_Abort_0):** Force abort bit for sensor 0. When set to 1, all data from the sensor should be dropped from PBM/SRAM no matter if the chunk is closed. In addition, counters will be reset. Note: Force_Abort should be activated after 2.5us minimum after Abort. Note: Not planned to be used.
0	0h RW	**Abort_0 (Abort_0):** Abort bit for sensor 0. When set to 1, all data from the sensor should be dropped from PBM/SRAM.

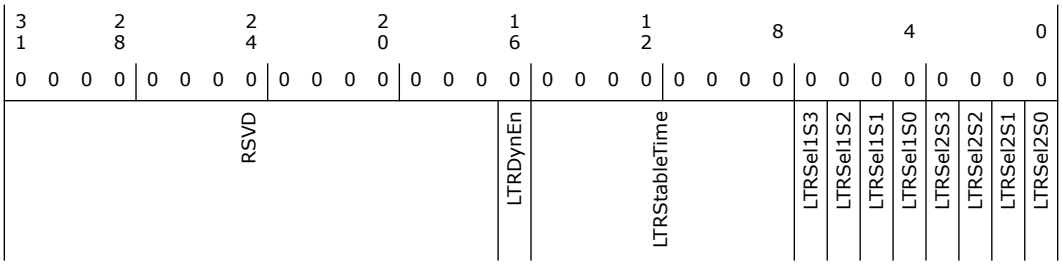
24.4.7 LTRCtrl (LTRCtrl)—Offset 1480h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	Reserved.
16	0h RW	**LTRDynEn (LTRDynEn):** Enable dynamic LTR mechanism. If disabled, only LTR11 is published. 0: disabled (default) (only LTR11 is sent by default) 1: enabled (start at LTR00) When set to 1'b1 will trigger LTR message. Used for both SNOOP and NONSNOOP LTR message.
15:8	0h RW	**LTRStableTime (LTRStableTime):** Value of the stable time before sending an LTR message. Fed from 78.125MHz clock (CSI2 clock divided by 2 to get the PBM clock, every 2 cycle of this clock LTRStableTime counter get +1 to its value)

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**LTRSel1S3 (LTRSel1S3):** Determine if Sensor3 Frame-Open/Frame-Close participates in LTRSel1: 0: no 1: yes
6	0h RW	**LTRSel1S2 (LTRSel1S2):** Determine if Sensor2 Frame-Open/Frame-Close participates in LTRSel1: 0: no 1: yes
5	0h RW	**LTRSel1S1 (LTRSel1S1):** Determine if Sensor1 Frame-Open/Frame-Close participates in LTRSel1: 0: no 1: yes
4	0h RW	**LTRSel1S0 (LTRSel1S0):** Determine if Sensor0 Frame-Open/Frame-Close participates in LTRSel1: 0: no 1: yes
3	0h RW	**LTRSel2S3 (LTRSel2S3):** Determine if Sensor3 Frame-Open/Frame-Close participates in LTRSel2: 0: no 1: yes
2	0h RW	**LTRSel2S2 (LTRSel2S2):** Determine if Sensor2 Frame-Open/Frame-Close participates in LTRSel2: 0: no 1: yes
1	0h RW	**LTRSel2S1 (LTRSel2S1):** Determine if Sensor1 Frame-Open/Frame-Close participates in LTRSel2: 0: no 1: yes
0	0h RW	**LTRSel2S0 (LTRSel2S0):** Determine if Sensor0 Frame-Open/Frame-Close participates in LTRSel2: 0: no 1: yes

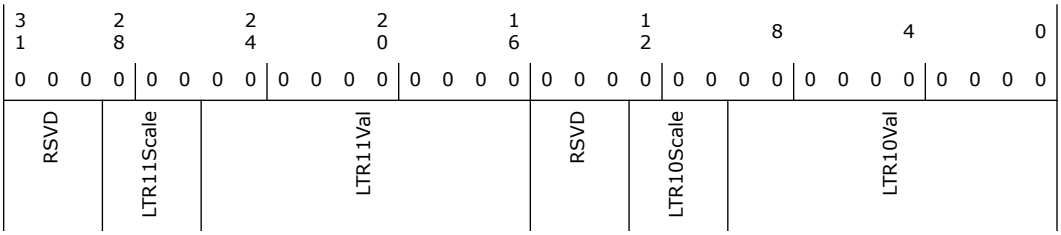
24.4.8 LTRVal1 (LTRVal1)—Offset 1484h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	Reserved.
28:26	0h RW	**LTR11Scale (LTR11Scale):** LTR11 SCALE: Note this is mapped to SNOOP LTR setting. Encodings: 000 – Value times 1 ns 001 – Value times 32 ns 010 – Value times 1,024 ns 011 – Value times 32,768 ns 100 – Value times 1,048,576 ns 101 – Value times 33,554,432 ns 110 - 111 – Not Permitted Used for both SNOOP and NONSNOOP LTR message.
25:16	0h RW	**LTR11Val (LTR11Val):** LTR11 value: This field indicates the default (or smallest, if dynamic LTR is enabled) LTR value which will be published to PMC. Note that Non-snoop LTR setting is set to infinite from camera perspective. The small/default latency tolerance is this value multiplied by SNOOP_SCALE. Used for both SNOOP and NONSNOOP LTR message.
15:13	0h RO	Reserved.
12:10	0h RW	**LTR10Scale (LTR10Scale):** LTR10 SCALE: Note this is mapped to SNOOP LTR setting. Encodings: 000 – Value times 1 ns 001 – Value times 32 ns 010 – Value times 1,024 ns 011 – Value times 32,768 ns 100 – Value times 1,048,576 ns 101 – Value times 33,554,432 ns 110 - 111 – Not Permitted. Used for both SNOOP and NONSNOOP LTR message.
9:0	0h RW	**LTR10Val (LTR10Val):** LTR10 value: This field indicates the LTR10 value if dynamic LTR is enabled to be published to PMC. Note that Non-snoop LTR setting is set to infinite from camera perspective. The small/default latency tolerance is this value multiplied by LTR10Scale. Used for both SNOOP and NONSNOOP LTR message.

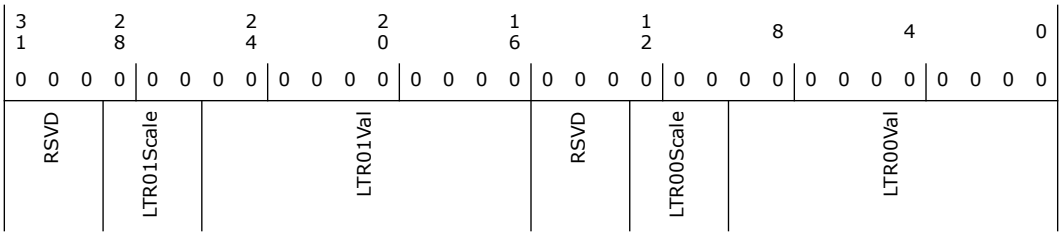
24.4.9 LTRVal0 (LTRVal0)—Offset 1488h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	Reserved.
28:26	0h RW	**LTR01Scale (LTR01Scale):** LTR01 SCALE: Note this is mapped to SNOOP LTR setting. Encodings: 000 – Value times 1 ns 001 – Value times 32 ns 010 – Value times 1,024 ns 011 – Value times 32,768 ns 100 – Value times 1,048,576 ns 101 – Value times 33,554,432 ns 110-111 – Not Permitted Used for both SNOOP and NONSNOOP LTR message.
25:16	0h RW	**LTR01Val (LTR01Val):** LTR01 value: This field indicates the default (or smallest, if dynamic LTR is enabled) LTR value which will be published to PMC. Note that Non-snoop LTR setting is set to infinite from camera perspective. The small/default latency tolerance is this value multiplied by SNOOP_SCALE. Used for both SNOOP and NONSNOOP LTR message.
15:13	0h RO	Reserved.
12:10	0h RW	**LTR00Scale (LTR00Scale):** LTR00 SCALE: Note this is mapped to SNOOP LTR setting. Encodings: 000 – Value times 1 ns 001 – Value times 32 ns 010 – Value times 1,024 ns 011 – Value times 32,768 ns 100 – Value times 1,048,576 ns 101 – Value times 33,554,432 ns 110 - 111 – Not Permitted Used for both SNOOP and NONSNOOP LTR message.
9:0	0h RW	**LTR00Val (LTR00Val):** LTR00 value: This field indicates the default (or small, if dynamic LTR is enabled) LTR value which will be published to PMC. Note that Non-snoop LTR setting is set to infinite from camera perspective. The small/default latency tolerance is this value multiplied by SNOOP_SCALE. Used for both SNOOP and NONSNOOP LTR message.

24.4.10 PBM PLL and frame period (PBM_FRAME_PERIOD_S[3:0])—Offset 148Ch

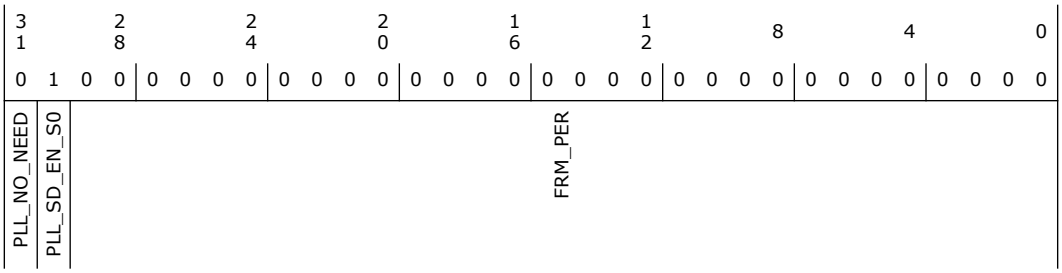
PBM_FRAME_PERIOD_S0: 0x148C
PBM_FRAME_PERIOD_S1: 0x1490
PBM_FRAME_PERIOD_S2: 0x1494
PBM_FRAME_PERIOD_S3: 0x1498.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 40000000h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**PBM_PLL_NO_NEED_S0 (PLL_NO_NEED):** SW sets this bit to mark that as far as this sensor is concerned – the PLL is not needed (sensor not in use). This enables the PLL Shut-down mechanism to shut-down if other sensor do not need the PLL in between frames. 0: PLL needed 1: PLL not needed This bit is not relevant if PLL_SHUT_DOWN_EN is '0' (mechanism is disabled) and should be set before the mechanism is enabled.
30	1h RW	**PLL_SD_EN_S0 (PLL_SD_EN_S0):** PLL shutdown mechanism enable. When disable (0), all counters and FSM are reset and clock is always requested, unless PBM_PLL_NO_NEED_S0 is set.
29:0	0h RW	**PBM_FRAME_PERIOD_S0 (FRM_PER):** Frame counter fed from 24MHz clock – the time between frames (FS to FS) for sensor 0 (for example for 30FPS it is 800,000).

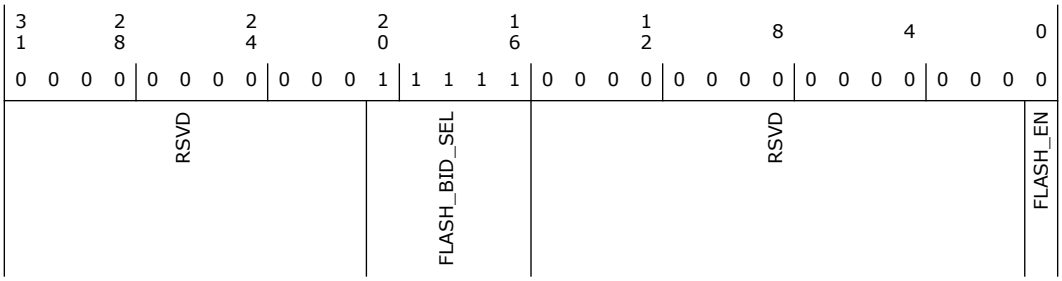
24.4.11 PBM_FLASH_CTRL (PBM_FLASH_CTRL)—Offset 149Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 1F0000h



Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
20:16	1Fh RW	**FLASH_BID_SEL (FLASH_BID_SEL):** Select which related BID will issue the flash triggering.
15:1	0h RO	Reserved.
0	0h RW/V	**FLASH_EN (FLASH_EN):** SW will set this bit to request for flash, upon completion of the flashing sequence (when FlashTrig signal is de-asserted) the HW to clear this bit. Note that FlashSeqStartedInd will be marked at the FBPT update (FE or LineNumeUpdate) after starting to count PBM_FLASH_TM_TO_TRG at FS.

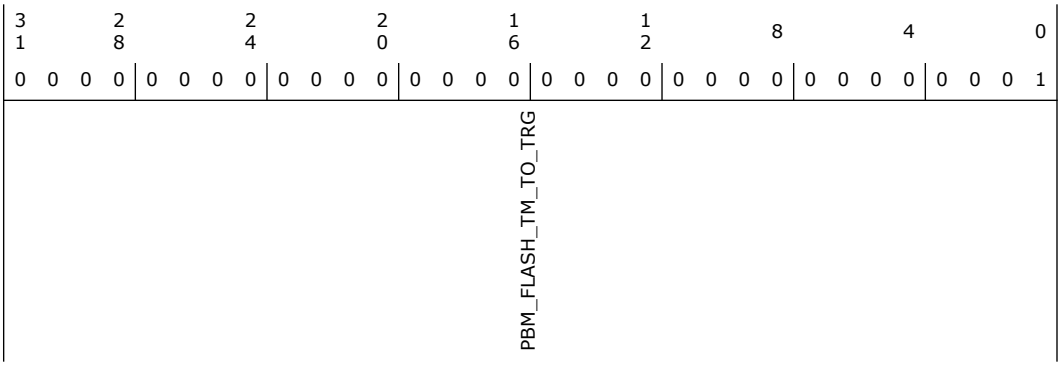
24.4.12 PBM_FLASH_TM_TO_TRG (PBM_FLASH_TM_TO_TRG)—Offset 14A0h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 1h



Bit Range	Default & Access	Field Name (ID): Description
31:0	1h RW	**PBM_FLASH_TM_TO_TRG (PBM_FLASH_TM_TO_TRG):** Time to delay the assertion of the FlashTrig signal from the next frame start of the selected BID after setting the FLASH_EN. This counter is counting at 24MHz AON clock.

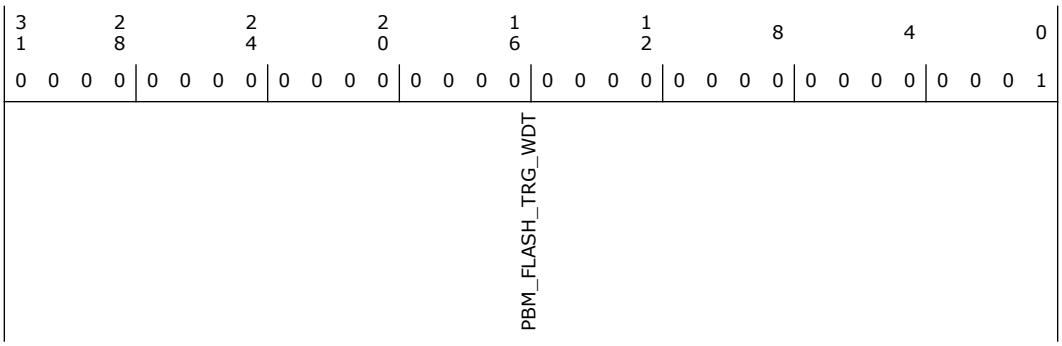
24.4.13 PBM_FLASH_TRG_WDT (PBM_FLASH_TRG_WDT)—Offset 14A4h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 1h



Bit Range	Default & Access	Field Name (ID): Description
31:0	1h RW	**PBM_FLASH_TRG_WDT (PBM_FLASH_TRG_WDT):** Flash pulse width – time to count 24MHz before de-asserting the FlashTrig after asserted. Once FlashTrig is de-asserted the FLASH_EN will be cleared.

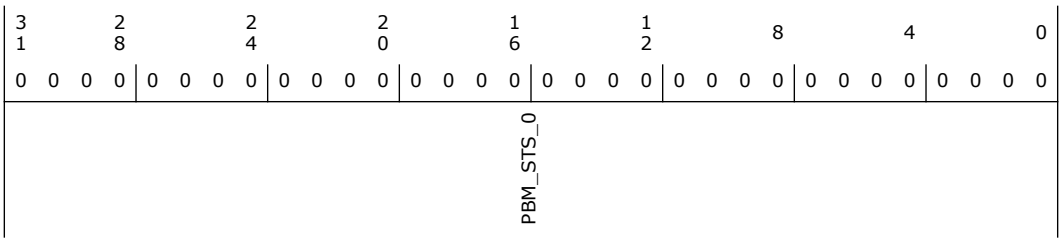
24.4.14 PBM_STS_0 (PBM_STS_0)—Offset 14A8h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**PBM_STS_0 (PBM_STS_0):** PBM internal design status register. Documentation specified in cio2 debug registers spec.

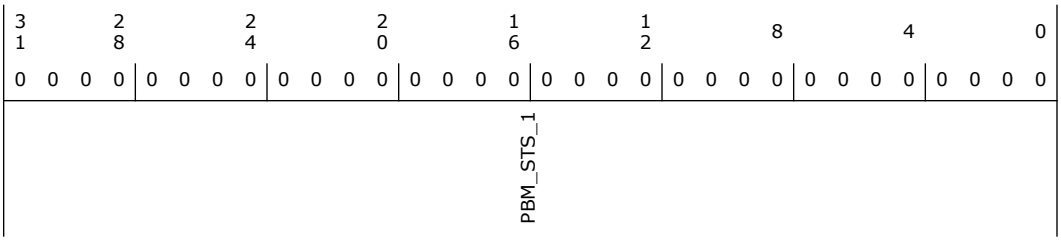
24.4.15 PBM_STS_1 (PBM_STS_1)—Offset 14ACh

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**PBM_STS_1 (PBM_STS_1):** PBM internal design status register. Documentation specified in cio2 debug registers spec.

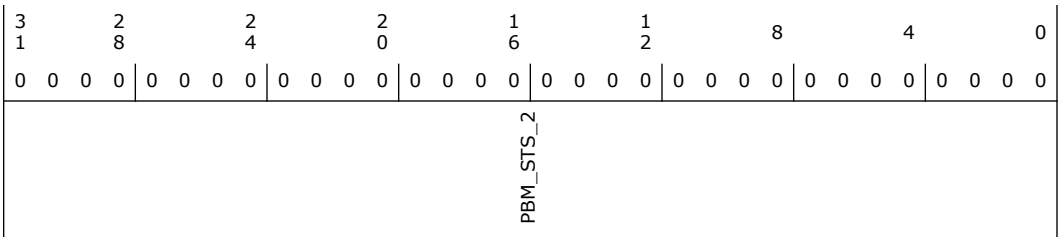
24.4.16 PBM_STS_2 (PBM_STS_2)—Offset 14B0h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**PBM_STS_2 (PBM_STS_2):** PBM internal design status register. Documentation specified in cio2 debug registers spec.

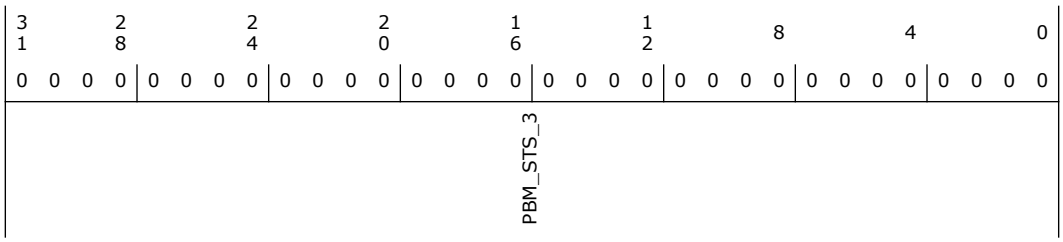
24.4.17 PBM_STS_3 (PBM_STS_3)—Offset 14B4h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**PBM_STS_3 (PBM_STS_3):** PBM internal design status register. Documentation specified in cio2 debug registers spec.

24.4.18 PXF formats configurations (PXM_PXF_FMT_Cfg0[0])—Offset 1700h

PXF formats configurations:
Config0: Sensor 0:0X1700h
Sensor 1:0X1730h
Sensor 2:0X1760h
Sensor 3:0X1790h.
Config1:
Sensor 0:0X1704h
Sensor 1:0X1734h
Sensor 2:0X1764h
Sensor 3:0X1794h.
Config2:
Sensor 0:0X1708h
Sensor 1:0X1738h
Sensor 2:0X1768h
Sensor 3:0X1798h.
Config3:
Sensor 0:0X170Ch
Sensor 1:0X173Ch
Sensor 2:0X176Ch
Sensor 3:0X179Ch.
Config4:
Sensor 0:0X1710h
Sensor 1:0X1740h
Sensor 2:0X1770h
Sensor 3:0X17A0h.
Config5:
Sensor 0:0X1714h
Sensor 1:0X1744h
Sensor 2:0X1774h
Sensor 3:0X17A4h.
Config6:
Sensor 0:0X1718h
Sensor 1:0X1748h
Sensor 2:0X1778h
Sensor 3:0X17A8h.
Config7:

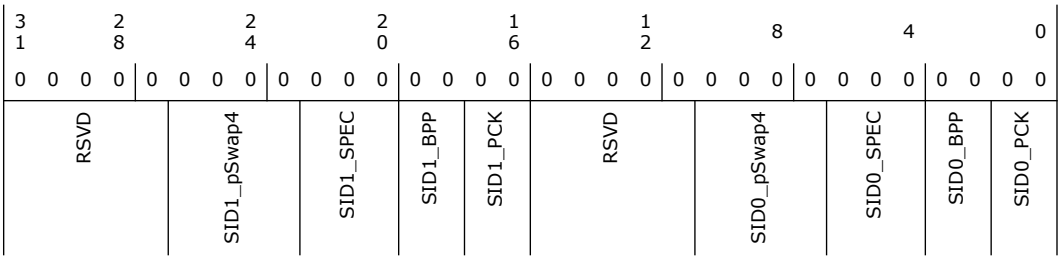
Sensor 0:0X171Ch
Sensor 1:0X174Ch
Sensor 2:0X177Ch
Sensor 3:0X17ACh.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	Reserved.
26:23	0h RW	**SID1_pSwap4 (SID1_pSwap4):** SID1 Byte Swap within 32b if 8bpp is received. bit0 - first stage swap A/B bit1 - first stage swap C/D bit2 - second stage swap A'/C' bit3 - second stage swap B'/D' (!) The swapping is done on the pixel input and completely independent from all other settings.
22:20	0h RW	**SID1_SPEC (SID1_SPEC):** Special format handling, 8bpp only 000: 4ppc (default) 001: 3ppc, add alpha (0) from right (for RGBA) 010: 3ppc, add alpha (0) from left (for ARGB) 011: Planar2 output. YUV420 in. Odd lines to SIDa, Even lines to SIDa and SIDb. SIDa is the input SID. SIDb is SIDa+4. It's the SW responsibility to make sure SIDa+4 is NOT USED! 100: Planar3 output. Separate Y, U, V buffers. YUV420 legacy. 101: NV16 output. Like Plannar2 but all the line like even line. Planar3 use SIDa=input SID, SIDb=SIDa+4, SIDc=SIDa+8.
19:18	0h RW	**SID1_BPP (SID1_BPP):** 00: 08bpp (default) 01: 10bpp 10: 12bpp 11: 14bpp
17:16	0h RW	**SID1_PCK (SID1_PCK):** Packing selection 00: 64B (default) 01: 32B 10: NA 11: NA. (!) NOTE: When padding is added, PXF need to adjust the LE signal accordingly. NOTE: 32B packing require padding to 64B at LE.
15:11	0h RO	Reserved.
10:7	0h RW	**SID0_pSwap4 (SID0_pSwap4):** SID0 Byte Swap within 32b if 8bpp is received. bit0 - first stage swap A/B bit1 - first stage swap C/D bit2 - second stage swap A'/C' bit3 - second stage swap B'/D' (!) The swapping is done on the pixel input and completely independent from all other settings.

Bit Range	Default & Access	Field Name (ID): Description
6:4	0h RW	**SID0_SPEC (SID0_SPEC):** Special format handling, 8bpp only 000: 4ppc (default) 001: 3ppc, add alpha (0) from right (for RGBA) 010: 3ppc, add alpha (0) from left (for ARGB) 011: Planar2 output. YUV420 in. Odd lines to SIDa, Even lines to SIDa and SIDb. SIDa is the input SID. SIDb is SIDa+4. It's the SW responsibility to make sure SIDa+4 is NOT USED! 100: Planar3 output. Separate Y, U, V buffers. YUV420 legacy. 101: NV16 output. Like Plannar2 but all the line like even line. Planar3 use SIDa=input SID, SIDb=SIDa+4, SIDc=SIDa+8.
3:2	0h RW	**SID0_BPP (SID0_BPP):** 00: 08bpp (default) 01: 10bpp 10: 12bpp 11: 14bpp
1:0	0h RW	**SID0_PCK (SID0_PCK):** Packing selection 00: 64B (default) 01: 32B 10: NA 11:NA (!) NOTE: When padding is added, PXF need to adjust the LE signal accordingly NOTE: 32B packing requires padding to 64B at LE.

24.4.19 PXM_FRF_cfg (PXM_FRF_cfg[3:0])—Offset 1720h

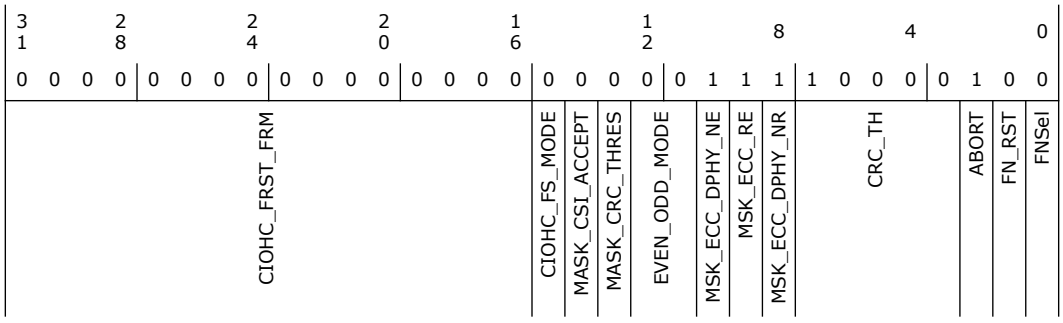
First Frame config:
Sensor:
0:0X1720h
1:0X1750h
2:0X1780h
3:0X17B0h.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 784h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**CIOHC_FRST_FRM (CIOHC_FRST_FRM):** RSVD.
15	0h RW	**CIOHC_FS_MODE (CIOHC_FS_MODE):** RSVD.
14	0h RW	**MASK_CSI_ACCEPT (MASK_CSI_ACCEPT):** 1 - CSI2_spif ACCEPT will always be 1'b1.
13	0h RW	**MASK_CRC_THRES (MASK_CRC_THRES):** Mask the CRC threshold. - When 1'b1 CRC over threshold will not close the frame.
12:11	0h RW	**Even_odd_mode (EVEN_ODD_MODE):** Configure the type of the lines in the frame EVEN_ODD_MODE[0] - Configure the type for first line 0-odd 1-even EVEN_ODD_MODE[1] - Change the type of line at line start 0-change 1-not change
10	1h RW	**MSK_ECC_NE (MSK_ECC_DPHY_NE):** Mask the ecc none recoverable (error cause[3]) counting. 0 - Will mask ECC counter. 1 - Will not mask ECC counter.
9	1h RW	**MSK_ECC_RE (MSK_ECC_RE):** Mask the ecc recoverable (error cause[2]) counting. 0 - Will mask ECC counter. 1 - Will not mask ECC counter.
8	1h RW	**MSK_ECC_DPHY_NR (MSK_ECC_DPHY_NR):** Mask the ecc dphy non recoverable (error cause[1]) counting. 0 - Will mask ECC counter. 1 - Will not mask ECC counter.
7:3	10h RW	**CRC_TH (CRC_TH):** CRC Threshold for number of errors, raise CRC_TH error if number of errors reaches this number (max is 32 errors).
2	1h RW	**ABORT (ABORT):** Abort all further input from this sensor. Generate FE for all open frames, SW can use this bit to block all input if it wants to reset or reconfigure the sensor or block its input.
1	0h RW	**FN_RST (FN_RST):** Reset Internal Frame number to 1.
0	0h RW	**FNSel (FNSel):** Frame Number source selection: 0: from Sensor (default) 1: from internal 4b wrap around counter. Count start from 1 even after counter rollover.

24.4.20 Sensor0 PXM Sidebid (PXM_SID2BID[2-0]Sensor[3:0])—Offset 1724h

PXM Sidebid0:
Sensor 0:0X1724h
Sensor 1:0X1754h
Sensor 2:0X1784h
Sensor 3:0X17B4h.
Sidebid1:
Sensor 1:0X1728h
Sensor 1:0X1758h
Sensor 2:0X1788h
Sensor 3:0X17B8h.
Sidebid2:
Sensor 0:0X172Ch

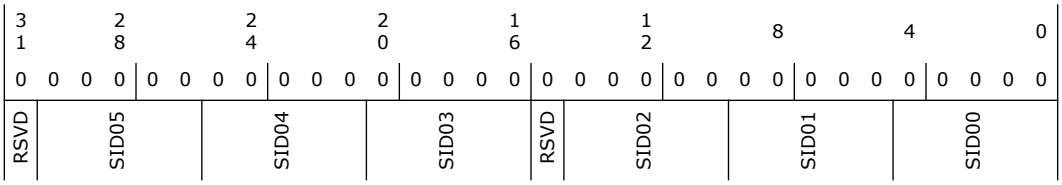
Sensor 1:0X175Ch
Sensor 2:0X178Ch
Sensor 3:0X17BCh.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	Reserved.
30:26	0h RW	**SID05 (SID05):** BIDVal – BID value (DMA ID)
25:21	0h RW	**SID04 (SID04):** BIDVal – BID value (DMA ID)
20:16	0h RW	**SID03 (SID03):** BIDVal – BID value (DMA ID)
15	0h RO	Reserved.
14:10	0h RW	**SID02 (SID02):** BIDVal – BID value (DMA ID)
9:5	0h RW	**SID01 (SID01):** BIDVal – BID value (DMA ID)
4:0	0h RW	**SID00 (SID00):** BIDVal – BID value (DMA ID)

24.4.21 PXM_PXF_FMT_Cfg3 (PXM_PXF_FMT_Cfg3[3])—Offset 179Ch

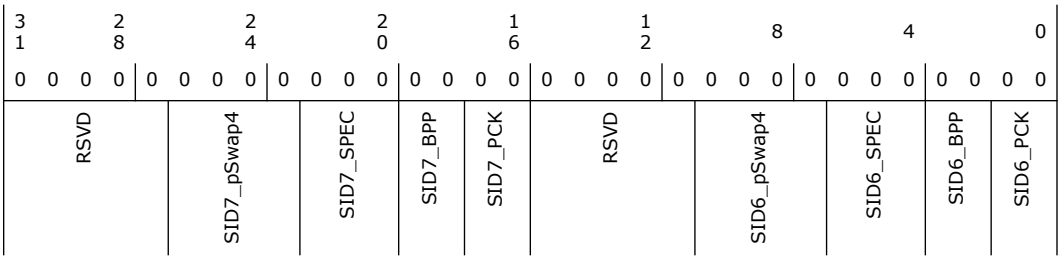
PXF formats configurations

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	Reserved.
26:23	0h RW	**SID7_pSwap4 (SID7_pSwap4):** SID7 Byte Swap within 32b if 8bpp is received. bit0 - first stage swap A/B bit1 - first stage swap C/D bit2 - second stage swap A'/C' bit3 - second stage swap B'/D' (!) The swapping is done on the pixel input and completely independent from all other settings.
22:20	0h RW	**SID7_SPEC (SID7_SPEC):** Special format handling, 8bpp only 000: 4ppc (default) 001: 3ppc, add alpha (0) from right (for RGBA) 010: 3ppc, add alpha (0) from left (for ARGB) 011: Planar2 output. YUV420 in. Odd lines to SIDa, Even lines to SIDa and SIDb. SIDa is the input SID. SIDb is SIDa+4. It's the SW responsibility to make sure SIDa+4 is NOT USED! 100: Planar3 output. Separate Y, U, V buffers. YUV420 legacy. 101: NV16 output. Like Plannar2 but all the line like even line. Planar3 use SIDa=input SID, SIDb=SIDa+4, SIDc=SIDa+8.
19:18	0h RW	**SID7_BPP (SID7_BPP):** 00: 08bpp (default) 01: 10bpp 10: 12bpp 11: 14bpp
17:16	0h RW	**SID7_PCK (SID7_PCK):** Packing selection 00: 64B (default) 01: 32B 10: NA 11: NA (!) NOTE: When padding is added, PXF need to adjust the LE signal accordingly NOTE: 32B packing requires padding to 64B at LE.
15:11	0h RO	Reserved.
10:7	0h RW	**SID6_pSwap4 (SID6_pSwap4):** SID6 Byte Swap within 32b if 8bpp is received. bit0 - first stage swap A/B bit1 - first stage swap C/D bit2 - second stage swap A'/C' bit3 - second stage swap B'/D' (!) The swapping is done on the pixel input and completely independent from all other settings.

Bit Range	Default & Access	Field Name (ID): Description
6:4	0h RW	**SID6_SPEC (SID6_SPEC):** Special format handling, 8bpp only 000: 4ppc (default) 001: 3ppc, add alpha (0) from right (for RGBA) 010: 3ppc, add alpha (0) from left (for ARGB) 011: Planar2 output. YUV420 in. Odd lines to SIDa, Even lines to SIDa and SIDb. SIDa is the input SID. SIDb is SIDa+4. It's the SW responsibility to make sure SIDa+4 is NOT USED! 100: Planar3 output. Separate Y, U, V buffers. YUV420 legacy. 101: NV16 output. Like Plannar2 but all the line like even line. Planar3 use SIDa=input SID, SIDb=SIDa+4, SIDc=SIDa+8.
3:2	0h RW	**SID6_BPP (SID6_BPP):** 00: 08bpp (default) 01: 10bpp 10: 12bpp 11: 14bpp
1:0	0h RW	**SID6_PCK (SID6_PCK):** Packing selection 00: 64B (default) 01: 32B 10: NA 11: NA (!) NOTE: When padding is added, PXF need to adjust the LE signal accordingly NOTE: 32B packing requires padding to 64B at LE.

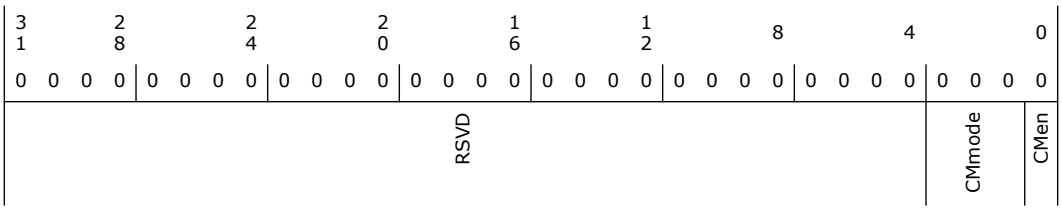
24.4.22 Channel Merging (PXM_CHM)—Offset 17C0h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3:1	0h RW	**CMmode (CMmode):** Channel Merging mode – applicable only if CMen is '1'. 000: Odd/Even 001: Even/Odd 010: 4/4 no swap 011: 4/4 swap 100: reserved 101: reserved 110: reserved 111: reserved
0	0h RW	**CMen (CMen):** Channel Merging Enable 0: disabled (default) 1: enabled

24.4.23 Number Of CRC (PXM_CRC_S[3:0])—Offset 17C4h

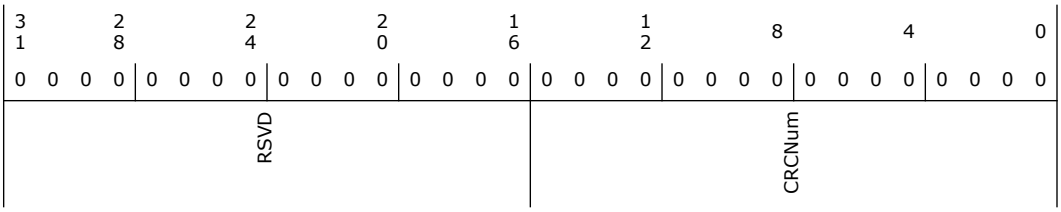
Number of CRC errors from:
Sensor 0:0x17C4
Sensor 1:0x17CC
Sensor 2:0x17D4
Sensor 3:0x17DC.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	0h RO/V	**CRCNum (CRCNum):** Number of CRC errors coming from Sensor0-3

24.4.24 Number Of ECC (PXM_ECC_S[3:0])—Offset 17C8h

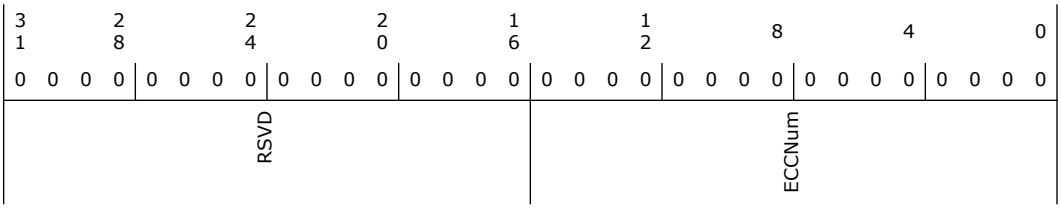
Number of ECC errors from:
Sensor 0:0x17C8
Sensor 1:0x17D0
Sensor 2:0x17DB
Sensor 3:0x17E0.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	0h RO/V	**ECCNum (ECCNum):** Number of accumulated ECC errors (1 or more) from power on for Sensor0. Note that CSI2 controller must be programmed in order to allow to continue because typically it will skip to next FS upon such error (if > 1)

24.4.25 Interrupt status for input error (INT_STS_EXT_IE)—Offset 17E4h

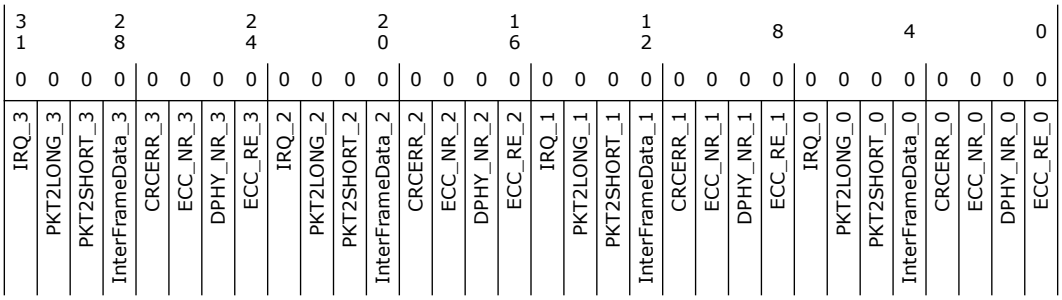
CIO2 Interrupt Status Extended for Input Error. Error reflects CSI2 SPIF errors.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C/V	**IRQ from port 3 (IRQ_3):** This bit indicates IRQ is asserted by port 3.
30	0h RW/1C/V	**Packet too long error from Sensor3 (PKT2LONG_3):** This error is set in the following cases: 1) Current packet is a long packet. Payload counter has reached its end value according to packet header word count field. New data arriving is not a packet header (more payload data comes). 2) Current packet is a short packet (packet header only). New data arriving is not a packet header. This bit will be set for inter-frame errors only.
29	0h RW/1C/V	**Packet too short error from Sensor3 (PKT2SHORT_3):** New start of packet/ packet header is received while payload counter did not reach its end value yet. This bit will be set for inter-frame errors only.
28	0h RW/1C/V	**Inter frame data error from Sensor3 (InterFrameData_3):** Packet is received outside frame boundaries of a certain VC. Meaning received after a frame end, but before a new frame start. This bit will be set for inter-frame errors only.
27	0h RW/1C/V	**CRC error from Sensor3 (CRCERR_3):** The checksum (CRC) error indicates that the payload of a long packet is corrupt. This bit will be set for inter-frame errors only.
26	0h RW/1C/V	**Packet Header Multiple bit error from Sensor3 (ECC_NR_3):** A multiple bit error was detected in the packet header via ECC code. This cannot be corrected and packet header data (virtual channel, format type and word count/data field) is unreliable. This bit will be set for inter-frame errors only.

Bit Range	Default & Access	Field Name (ID): Description
25	0h RW/1C/V	**DPHY NON-recoverable sync error from Sensor3 (DPHY_NR_3):** More than one bits of the sync pattern at the start of a high speed transmission are corrupted. This bit will be set for inter-frame errors only.
24	0h RW/1C/V	**ECC recoverable error from Sensor3 (ECC_RE_3):** A single bit error was detected in the packet header via ECC code. This can be corrected and packet header data (virtual channel, format type and word count/data field) is 100% correct.
23	0h RW/1C/V	**IRQ from port 2 (IRQ_2):** This bit indicates IRQ is asserted by port 2.
22	0h RW/1C/V	**Packet too long error from Sensor2 (PKT2LONG_2):** This error is set in the following cases: 1) Current packet is a long packet. Payload counter has reached its end value according to packet header word count field. New data arriving is not a packet header (more payload data comes). 2) Current packet is a short packet (packet header only). New data arriving is not a packet header. This bit will be set for inter-frame errors only.
21	0h RW/1C/V	**Packet too short error from Sensor2 (PKT2SHORT_2):** New start of packet/ packet header is received while payload counter did not reach its end value yet. This bit will be set for inter-frame errors only.
20	0h RW/1C/V	**Inter frame data error from Sensor2 (InterFrameData_2):** Packet is received outside frame boundaries of a certain VC. Meaning received after a frame end, but before a new frame start. This bit will be set for inter-frame errors only.
19	0h RW/1C/V	**CRC error from Sensor2 (CRCERR_2):** The checksum (CRC) error indicates that the payload of a long packet is corrupt. This bit will be set for inter-frame errors only.
18	0h RW/1C/V	**Packet Header Multiple bit error from Sensor2 (ECC_NR_2):** A multiple bit error was detected in the packet header via ECC code. This cannot be corrected and packet header data (virtual channel, format type and word count/data field) is unreliable. This bit will be set for inter-frame errors only.
17	0h RW/1C/V	**DPHY NON-recoverable sync error from Sensor2 (DPHY_NR_2):** More than one bits of the sync pattern at the start of a high speed transmission are corrupted. This bit will be set for inter-frame errors only.
16	0h RW/1C/V	**ECC recoverable error from Sensor2 (ECC_RE_2):** A single bit error was detected in the packet header via ECC code. This can be corrected and packet header data (virtual channel, format type and word count/data field) is 100% correct.
15	0h RW/1C/V	**IRQ from port 1 (IRQ_1):** This bit indicates IRQ is asserted by port 1.
14	0h RW/1C/V	**Packet too long error from Sensor1 (PKT2LONG_1):** This error is set in the following cases: 1) Current packet is a long packet. Payload counter has reached its end value according to packet header word count field. New data arriving is not a packet header (more payload data comes). 2) Current packet is a short packet (packet header only). New data arriving is not a packet header. This bit will be set for inter-frame errors only.
13	0h RW/1C/V	**Packet too short error from Sensor1 (PKT2SHORT_1):** New start of packet/ packet header is received while payload counter did not reach its end value yet. This bit will be set for inter-frame errors only.
12	0h RW/1C/V	**Inter frame data error from Sensor1 (InterFrameData_1):** Packet is received outside frame boundaries of a certain VC. Meaning received after a frame end, but before a new frame start. This bit will be set for inter-frame errors only.
11	0h RW/1C/V	**CRC error from Sensor1 (CRCERR_1):** The checksum (CRC) error indicates that the payload of a long packet is corrupt. This bit will be set for inter-frame errors only.
10	0h RW/1C/V	**Packet Header Multiple bit error from Sensor1 (ECC_NR_1):** A multiple bit error was detected in the packet header via ECC code. This cannot be corrected and packet header data (virtual channel, format type and word count/data field) is unreliable. This bit will be set for inter-frame errors only.
9	0h RW/1C/V	**DPHY NON-recoverable sync error from Sensor1 (DPHY_NR_1):** More than one bits of the sync pattern at the start of a high speed transmission are corrupted. This bit will be set for inter-frame errors only.
8	0h RW/1C/V	**ECC recoverable error from Sensor1 (ECC_RE_1):** A single bit error was detected in the packet header via ECC code. This can be corrected and packet header data (virtual channel, format type and word count/data field) is 100% correct.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW/1C/V	**IRQ from port 0 (IRQ_0):** This bit indicates IRQ is asserted by port 0.
6	0h RW/1C/V	**Packet too long error from Sensor0 (PKT2LONG_0):** This error is set in the following cases: 1) Current packet is a long packet. Payload counter has reached its end value according to packet header word count field. New data arriving is not a packet header (more payload data comes). 2) Current packet is a short packet (packet header only). New data arriving is not a packet header. This bit will be set for inter-frame errors only.
5	0h RW/1C/V	**Packet too short error from Sensor0 (PKT2SHORT_0):** New start of packet/ packet header is received while payload counter did not reach its end value yet. This bit will be set for inter-frame errors only.
4	0h RW/1C/V	**Inter frame data error from Sensor0 (InterFrameData_0):** Packet is received outside frame boundaries of a certain VC. Meaning received after a frame end, but before a new frame start. This bit will be set for inter-frame errors only.
3	0h RW/1C/V	**CRC error from Sensor0 (CRCERR_0):** The checksum (CRC) error indicates that the payload of a long packet is corrupt. This bit will be set for inter-frame errors only.
2	0h RW/1C/V	**Packet Header Multiple bit error from Sensor0 (ECC_NR_0):** A multiple bit error was detected in the packet header via ECC code. This cannot be corrected and packet header data (virtual channel, format type and word count/data field) is unreliable. This bit will be set for inter-frame errors only.
1	0h RW/1C/V	**DPHY NON-recoverable sync error from Sensor0 (DPHY_NR_0):** More than one bits of the sync pattern at the start of a high speed transmission are corrupted. This bit will be set for inter-frame errors only.
0	0h RW/1C/V	**ECC recoverable error from Sensor0 (ECC_RE_0):** A single bit error was detected in the packet header via ECC code. This can be corrected and packet header data (virtual channel, format type and word count/data field) is 100% correct.

24.4.26 Enable interrupt for input error (INT_EN_EXT_IE)—Offset 17E8h

CIO2 Interrupt Enable Extended for Input Error.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
IRQ_3_EN	PKT2LONG_3_EN	PKT2SHORT_3_EN	InterFrameData_3_EN	CRCERR_3_EN	ECC_NE_3_EN	DPHY_NR_3_EN	DPHY_RE_3_EN	IRQ_2_EN	PKT2LONG_2_EN	PKT2SHORT_2_EN	InterFrameData_2_EN	CRCERR_2_EN	ECC_NE_2_EN	DPHY_NR_2_EN	DPHY_RE_2_EN	IRQ_1_EN	PKT2LONG_1_EN	PKT2SHORT_1_EN	InterFrameData_1_EN	CRCERR_1_EN	ECC_NE_1_EN	DPHY_NR_1_EN	DPHY_RE_1_EN	IRQ_0_EN	PKT2LONG_0_EN	PKT2SHORT_0_EN	InterFrameData_0_EN	CRCERR_0_EN	ECC_NE_0_EN	DPHY_NR_0_EN	DPHY_RE_0_EN

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Interrupt Enable for IRQ from port 3 (IRQ_3_EN):** Enables interrupt assertion when this type of error occurs.
30	0h RW	**Interrupt Enable for Packet too long error from Sensor3 (PKT2LONG_3_EN):** Enables interrupt assertion when this type of error occurs.
29	0h RW	**Interrupt Enable for Packet too short error from Sensor3 (PKT2SHORT_3_EN):** Enables interrupt assertion when this type of error occurs.
28	0h RW	**Interrupt Enable for Inter frame data error from Sensor3 (InterFrameData_3_EN):** Enables interrupt assertion when this type of error occurs.
27	0h RW	**Interrupt Enable for CRC error from Sensor3 (CRCERR_3_EN):** Enables interrupt assertion when this type of error occurs.
26	0h RW	**Interrupt Enable for Packet Header Multiple bit error from Sensor3 (ECC_NE_3_EN):** Enables interrupt assertion when this type of error occurs.
25	0h RW	**Interrupt Enable for DPHY NON-recoverable sync error from Sensor3 (DPHY_NR_3_EN):** Enables interrupt assertion when this type of error occurs.
24	0h RW	**Interrupt Enable for DPHY recoverable sync error from Sensor3 (DPHY_RE_3_EN):** Enables interrupt assertion when this type of error occurs.
23	0h RW	**Interrupt Enable for IRQ from port 2 (IRQ_2_EN):** Enables interrupt assertion when this type of error occurs.
22	0h RW	**Interrupt Enable for Packet too long error from Sensor2 (PKT2LONG_2_EN):** Enables interrupt assertion when this type of error occurs.
21	0h RW	**Interrupt Enable for Packet too short error from Sensor2 (PKT2SHORT_2_EN):** Enables interrupt assertion when this type of error occurs.
20	0h RW	**Interrupt Enable for Inter frame data error from Sensor2 (InterFrameData_2_EN):** Enables interrupt assertion when this type of error occurs.
19	0h RW	**Interrupt Enable for CRC error from Sensor2 (CRCERR_2_EN):** Enables interrupt assertion when this type of error occurs.
18	0h RW	**Interrupt Enable for Packet Header Multiple bit error from Sensor2 (ECC_NE_2_EN):** Enables interrupt assertion when this type of error occurs.
17	0h RW	**Interrupt Enable for DPHY NON-recoverable sync error from Sensor2 (DPHY_NR_2_EN):** Enables interrupt assertion when this type of error occurs.
16	0h RW	**Interrupt Enable for DPHY recoverable sync error from Sensor2 (DPHY_RE_2_EN):** Enables interrupt assertion when this type of error occurs.
15	0h RW	**Interrupt Enable for IRQ from port 1 (IRQ_1_EN):** Enables interrupt assertion when this type of error occurs.
14	0h RW	**Interrupt Enable for Packet too long error from Sensor1 (PKT2LONG_1_EN):** Enables interrupt assertion when this type of error occurs.
13	0h RW	**Interrupt Enable for Packet too short error from Sensor1 (PKT2SHORT_1_EN):** Enables interrupt assertion when this type of error occurs.
12	0h RW	**Interrupt Enable for Inter frame data error from Sensor1 (InterFrameData_1_EN):** Enables interrupt assertion when this type of error occurs.
11	0h RW	**Interrupt Enable for CRC error from Sensor1 (CRCERR_1_EN):** Enables interrupt assertion when this type of error occurs.
10	0h RW	**Interrupt Enable for Packet Header Multiple bit error from Sensor1 (ECC_NE_1_EN):** Enables interrupt assertion when this type of error occurs.
9	0h RW	**Interrupt Enable for DPHY NON-recoverable sync error from Sensor1 (DPHY_NR_1_EN):** Enables interrupt assertion when this type of error occurs.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**Interrupt Enable for DPHY recoverable sync error from Sensor1 (DPHY_RE_1_EN):** Enables interrupt assertion when this type of error occurs.
7	0h RW	**Interrupt Enable for IRQ from port 0 (IRQ_0_EN):** Enables interrupt assertion when this type of error occurs.
6	0h RW	**Interrupt Enable for Packet too long error from Sensor0 (PKT2LONG_0_EN):** Enables interrupt assertion when this type of error occurs.
5	0h RW	**Interrupt Enable for Packet too short error from Sensor0 (PKT2SHORT_0_EN):** Enables interrupt assertion when this type of error occurs.
4	0h RW	**Interrupt Enable for Inter frame data error from Sensor0 (InterFrameData_0_EN):** Enables interrupt assertion when this type of error occurs.
3	0h RW	**Interrupt Enable for CRC error from Sensor0 (CRCERR_0_EN):** Enables interrupt assertion when this type of error occurs.
2	0h RW	**Interrupt Enable for Packet Header Multiple bit error from Sensor0 (ECC_NE_0_EN):** Enables interrupt assertion when this type of error occurs.
1	0h RW	**Interrupt Enable for DPHY NON-recoverable sync error from Sensor0 (DPHY_NR_0_EN):** Enables interrupt assertion when this type of error occurs.
0	0h RW	**Interrupt Enable for DPHY recoverable sync error from Sensor0 (DPHY_RE_0_EN):** Enables interrupt assertion when this type of error occurs.

24.5 CSI2 Additional Configuration Registers Summary

Table 24-3. Summary of CSI2 Additional Configuration Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	CSI0 RX Control (CSI0_RXCNTRL)—Offset 0h	0h
3h	6h	CSI1 RX Control (CSI1_RXCNTRL)—Offset 3h	0h
Ah	Dh	CSI2 RX Control (CSI2_RXCNTRL)—Offset Ah	0h
Fh	12h	(CSI_CLKTRIM)—Offset Fh	0h
10h	13h	CSI3 RX Control (CSI3_RXCNTRL)—Offset 10h	0h
13h	16h	CSI Configuration (CSI_CFG)—Offset 13h	0h
24h	27h	CSI Data Trim (CSI_DATATRIM)—Offset 24h	0h
25h	28h	CSI CTLE (CSI_CTLE)—Offset 25h	0h
30h	33h	(CSI_DATATRIM1)—Offset 30h	0h

24.5.1 CSI0 RX Control (CSI0_RXCNTRL)—Offset 0h

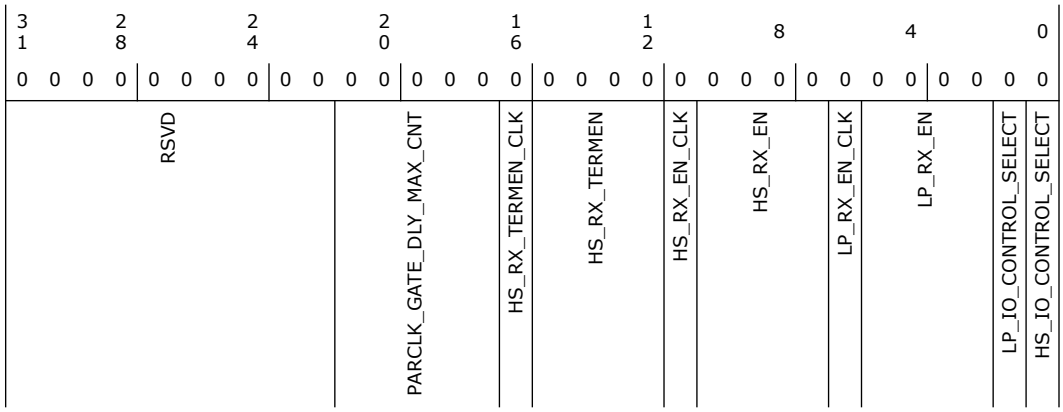
CSI0_RXCNTRL

Access Method

Type: MSG Register (Size: 32 bits)

Device: 20
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	Reserved.
21:17	0h RW	**CSI0 PARCLK Gating max delay Count Value. (PARCLK_GATE_DLY_MAX_CNT)**
16	0h RW	**CSI0 HS RX clk Terminator Enable (HS_RX_TERMEN_CLK)**
15:12	0h RW	**CSI0 HS RX Data Terminator Enable (HS_RX_TERMEN):** CSI0 HS RX data terminator enable (data3, data2, data1, data0)
11	0h RW	**CSI0 HS RX clk Enable (HS_RX_EN_CLK)**
10:7	0h RW	**CSI0 HS RX Data Enable (HS_RX_EN):** CSI0 HS RX data enable (data3, data2, data1, data0)
6	0h RW	**CSI0 LP RX clk Enable (LP_RX_EN_CLK)**
5:2	0h RW	**CSI0 LP RX Data Enable (LP_RX_EN):** CSI0 LP RX data enable (data3, data2, data1, data0)
1	0h RW	**LP IO Control Select (LP_IO_CONTROL_SELECT):** 1 - FLIS control 0 - DPHY control
0	0h RW	**HS IO Control Select (HS_IO_CONTROL_SELECT):** 1 - FLIS control 0 - DPHY control

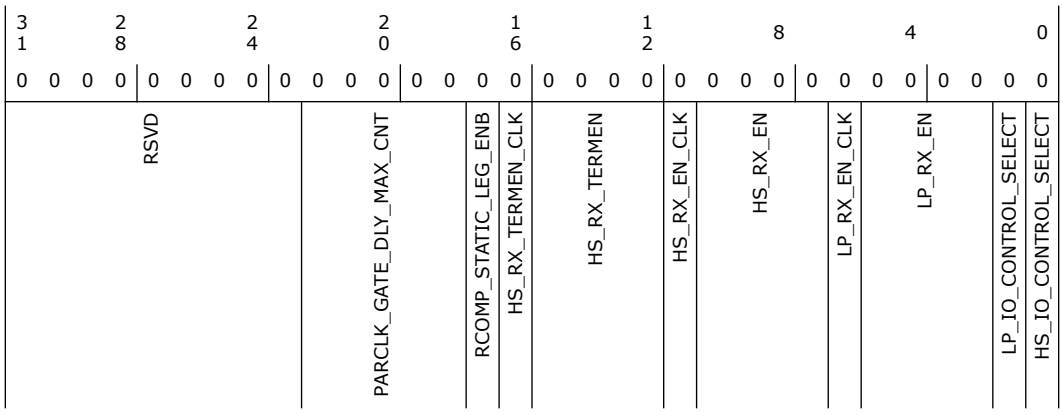
24.5.2 CSI1 RX Control (CSI1_RXCNTRL)—Offset 3h

Access Method

Type: MSG Register
(Size: 32 bits)

Device: 20
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	Reserved.
22:18	0h RW	**CSI1 PARCLK Gating Max Delay Count Value (PARCLK_GATE_DLY_MAX_CNT)**
17	0h RW	**RCOMP Static Leg Enable (RCOMP_STATIC_LEG_ENB):** CSI0/1/2/3 HS term static leg disable.
16	0h RW	**CSI1 HS RX clk Terminator Enable (HS_RX_TERMEN_CLK)**
15:12	0h RW	**CSI1 HS RX Data Terminator Enable (HS_RX_TERMEN):** CSI1 HS RX data terminator enable (data3, data2, data1, data0)
11	0h RW	**CSI1 HS RX clk Enable (HS_RX_EN_CLK)**
10:7	0h RW	**CSI1 HS RX Data Terminator Enable (HS_RX_EN):** CSI1 HS RX data terminator enable (data3, data2, data1, data0)
6	0h RW	**CSI1 LP RX clk Enable (LP_RX_EN_CLK)**
5:2	0h RW	**CSI1 LP RX Data Enable (LP_RX_EN):** CSI1 LP RX data enable (data3, data2, data1, data0)
1	0h RW	**LP IO Control Select (LP_IO_CONTROL_SELECT):** 1 - FLIS control 0 - DPHY control
0	0h RW	**HS IO Control Select (HS_IO_CONTROL_SELECT):** 1 - FLIS control 0 - DPHY control

24.5.3 CSI2 RX Control (CSI2_RXCNTRL)—Offset Ah

Same definition as CSI0_RXCNTRL register.

24.5.4 (CSI_CLKTRIM)—Offset Fh

Adjustment to CSI clock timing.
Enable CSI2 PORT A TRIM: CSI_CLKTRIM[16]=1
Disable CSI2 PORT A TRIM: CSI_CLKTRIM[16]=0
Enable CSI2 PORT B TRIM: CSI_CLKTRIM[17]=1
Disable CSI2 PORT B TRIM: CSI_CLKTRIM[17]=0

Enable CSI2 PORT C TRIM: CSI_CLKTRIM[18]=1
Disable CSI2 PORT C TRIM: CSI_CLKTRIM[18]=0
Enable CSI2 PORT D TRIM: CSI_CLKTRIM[19]=1
Disable CSI2 PORT D TRIM: CSI_CLKTRIM[19]=0.
Clock TRIM Values:
CSI2 PORT A Clock Trim Value: CSI_CLKTRIM[3:0]= user defined 16 bit value
CSI2 PORT B Clock Trim Value: CSI_CLKTRIM[7:4]= user defined 16 bit value
CSI2 PORT C Clock Trim Value: CSI_CLKTRIM[11:8]= user defined 16 bit value
CSI2 PORT D Clock Trim Value: CSI_CLKTRIM[15:12]= user defined 16 bit value.

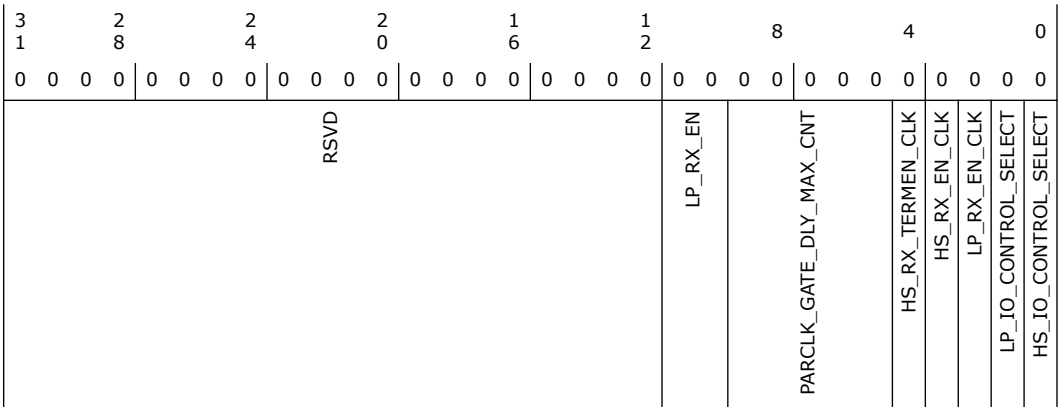
24.5.5 CSI3 RX Control (CSI3_RXCNTRL)—Offset 10h

Access Method

Type: MSG Register
(Size: 32 bits)

Device: 20
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	Reserved.
11:10	0h RW	**CSI3 LP RX Data Enable Control Test Override (LP_RX_EN):** CSI3 LP RX data enable Control Test Override (data1, data0)
9:5	0h RW	**CSI3 PARCLK Gating Max Delay Count Value (PARCLK_GATE_DLY_MAX_CNT)**
4	0h RW	**CSI3 HS RX clk Terminator Enable (HS_RX_TERMEN_CLK)**
3	0h RW	**CSI3 HS RX clk Enable (HS_RX_EN_CLK)**

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**CSI3 LP RX clk Enable (LP_RX_EN_CLK)**
1	0h RW	**LP IO Control Select (LP_IO_CONTROL_SELECT):** 1 - FLIS control 0 - DPHY control
0	0h RW	**HS IO Control Select (HS_IO_CONTROL_SELECT):** 1 - FLIS control 0 - DPHY control

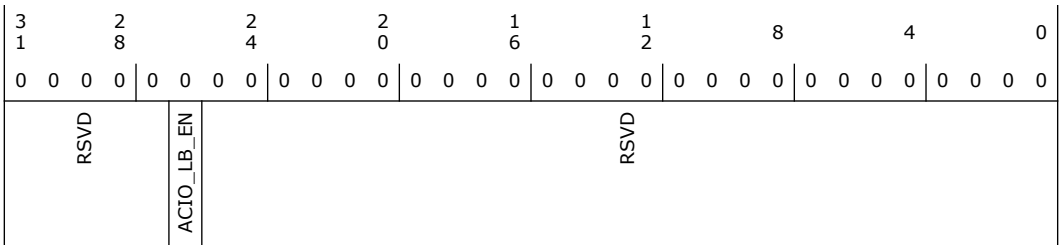
24.5.6 CSI Configuration (CSI_CFG)—Offset 13h

Access Method

Type: MSG Register
(Size: 32 bits)

Device: 20
Function: 3

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	Reserved.
26	0h RW	**Loop Back Enable (ACIO_LB_EN):** The bit is to enable the internal loopback.
25:0	0h RO	Reserved.

24.5.7 CSI Data Trim (CSI_DATATRIM)—Offset 24h

CSI2 PORT A Data Trim Value: CSI_DATATRIM[15:0]= user defined 16 bit value
CSI2 PORT B Data Trim Value: CSI_DATATRIM[31:16]= user defined 16 bit value.

24.5.8 CSI CTLE (CSI_CTLE)—Offset 25h

Enable PORT-A CTLE: CSI_CTLE[9] = 1
Disable PORT-A CTLE: CSI_CTLE[9] = 0
Enable PORT-B CTLE: CSI_CTLE[19]= 1
Disable PORT-B CTLE: CSI_CTLE[19]= 0
Enable PORT-C/D CTLE: CSI_CTLE[29]= 1
Disable PORT-C/D CTLE: CSI_CTLE[29]= 0
CSI2 PORT A CTLE CAP Value: CSI_CTLE[3:0]= 4 bit used defined value
CSI2 PORT A CTLE RES Value CSI_CTLE[8:4]= 5 bit used defined value

CSI2 PORT B CTLE CAP Value: CSI_CTLE[13:10]= 4 bit used defined value
CSI2 PORT B CTLE RES Value: CSI_CTLE[18:14]= 5 bit used defined value
CSI2 PORT C/D CTLE CAP Value: CSI_CTLE[13:20]= 4 bit used defined value
CSI2 PORT C/D CTLE RES Value: CSI_CTLE[28:24]= 5 bit used defined value.

24.5.9 (CSI_DATATRIM1)—Offset 30h

CSI2 PORT C/D Data Trim Value:
CSI_DATATRIM1[15:0]= user defined 16 bit value. Write user defined 16 bit value to CSI DATATRIM1 DATAx Where x is 0,1,2 or 3.

§ §

25 Integrated Sensor Hub (ISH) (D19:F0)

25.1 ISH PCI Configuration Registers Summary

Table 25-1. Summary of ISH PCI Configuration Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	Device and Vendor ID Register (DEVVENDID)—Offset 0h	X_8086h
4h	7h	Status and Command (STATUSCOMMAND)—Offset 4h	100000h
8h	Bh	Revision ID and Class Code (REVCLASSCODE)—Offset 8h	See register
Ch	Fh	Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch	0h
10h	13h	Memory Base Address Register (BAR)—Offset 10h	0h
14h	17h	Memory Base Address Register High (BAR_HIGH)—Offset 14h	0h
18h	1Bh	Memory Base Address 1 (BAR1)—Offset 18h	0h
1Ch	1Fh	Memory Base Address 1 High (BAR1_HIGH)—Offset 1Ch	0h
2Ch	2Fh	Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch	0h
30h	33h	Expansion ROM base address (EXPANSION_ROM_BASEADDR)—Offset 30h	0h
34h	37h	Capabilities Pointer (CAPABILITYPTR)—Offset 34h	80h
3Ch	3Fh	Interrupt (INTERRUPTREG)—Offset 3Ch	100h
80h	83h	PowerManagement Capability ID (POWERCAPID)—Offset 80h	48030001h
84h	87h	Power Management Control and Status (PMECTRLSTATUS)—Offset 84h	8h
A0h	A3h	General Purpose Read Write Register1 (GEN_REGRW1)—Offset A0h	0h
A4h	A7h	General Purpose Read Write Register2 (GEN_REGRW2)—Offset A4h	0h
A8h	ABh	General Purpose Read Write Register3 (GEN_REGRW3)—Offset A8h	0h
ACh	AFh	General Purpose Read Write Register4 (GEN_REGRW4)—Offset ACh	0h
C0h	C3h	General Purpose Input Register (GEN_INPUT_REG)—Offset C0h	0h

25.1.1 Device and Vendor ID Register (DEVVENDID)—Offset 0h

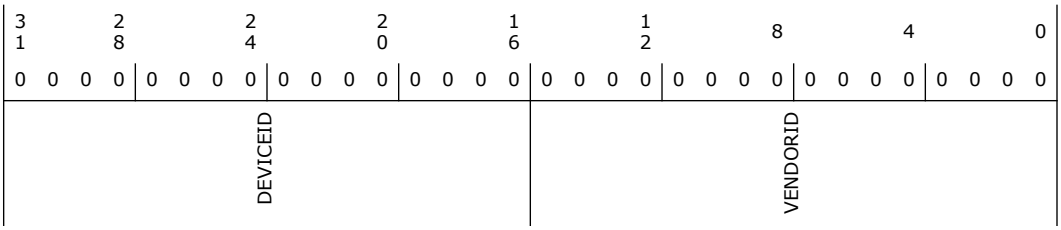
DEVICEVENDORID - Device ID and Vendor ID Register

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 19
Function: 0

Default: xxxx8086



Bit Range	Default & Access	Field Name (ID): Description
31:16	-- RO	**DEVICEID:** This is a 16-bit value assigned to the PCH ISH. See the Device and Version ID Table in Volume 1 for the default value.
15:0	8086h RO	**VENDORID:** This is a 16-bit value assigned to Intel. Intel VID = 8086h

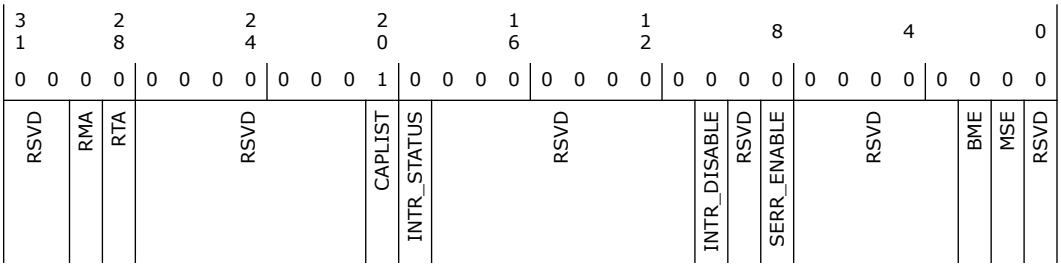
25.1.2 Status and Command (STATUSCOMMAND)—Offset 4h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 19
Function: 0

Default: 100000h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29	0h RW/1C	**RMA**
28	0h RW/1C	**RTA**
27:21	0h RO	Reserved.
20	1h RO	**CAPLIST**
19	0h RO	**Interrupt Status (INTR_STATUS)**
18:11	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW	**Interrupt Disable (INTR_DISABLE):** 0 = Enable 1 = Disables I2C to assert its interrupt signal.
9	0h RO	Reserved.
8	0h RW	**SERR# Enable (SERR_ENABLE):** 0 = Enables SERR# generation. 1 = Disables SERR# generation.
7:3	0h RO	Reserved.
2	0h RW	**Bus Master Enable (BME)**
1	0h RW	**Memory Space Enable (MSE):** 0 = Disables memory mapped configuration space. 1 = Enables memory mapped configuration space
0	0h RO	Reserved.

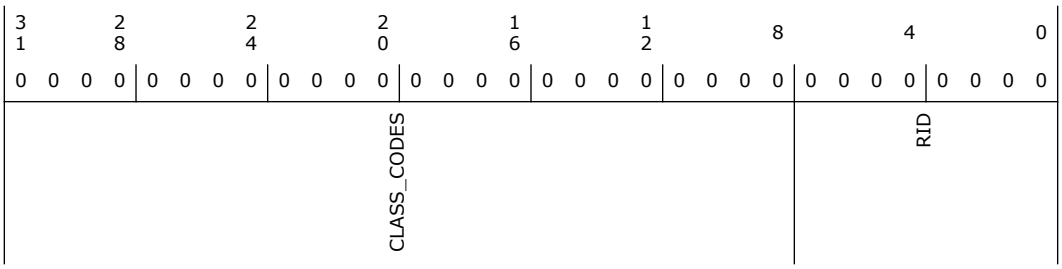
25.1.3 Revision ID and Class Code (REVCLASSCODE)—Offset 8h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 19
Function: 0

Default: See register



Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Class Code (CLASS_CODES)**
7:0	-- RO	**Revision ID (RID)** See the Device and Version ID Table in Volume 1 for the default value.

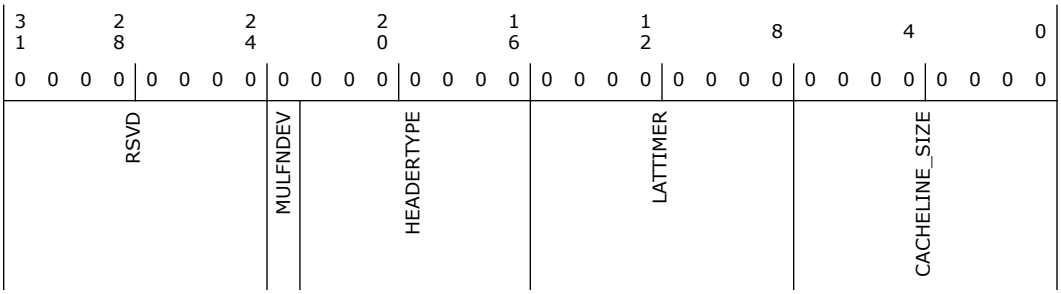
25.1.4 Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 19
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RO	**Multi-Function Device (MULFNDEV)**
22:16	0h RO	**Header Type (HEADERTYPE)**
15:8	0h RO	**Latency Timer (LATTIMER)**
7:0	0h RW	**Cache Line Size (CACHELINE_SIZE)**

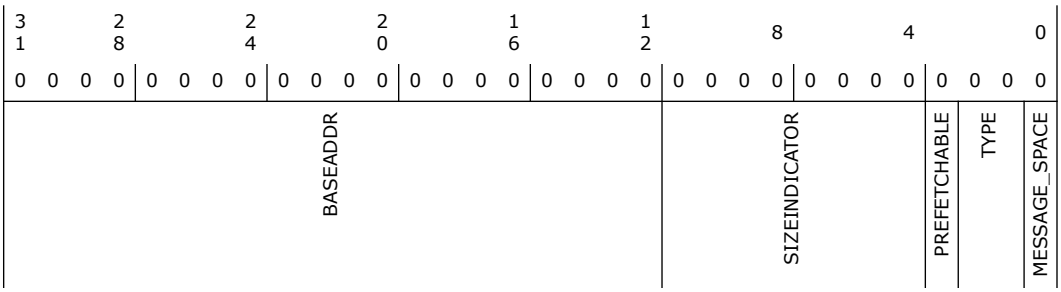
25.1.5 Memory Base Address Register (BAR)—Offset 10h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 19
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW	**Base Address (BASEADDR):** Provides system memory base address.
11:4	0h RO	**Size Indicator (SIZEINDICATOR)**
3	0h RO	**Prefetchable (PREFETCHABLE):** Hardwired to 0. Indicates that ISH BAR is not prefetchable
2:1	0h RO	**Type (TYPE)**
0	0h RO	**Message Space (MESSAGE_SPACE):** This read-only bit always is 0, indicating that the ISH logic is Memory mapped

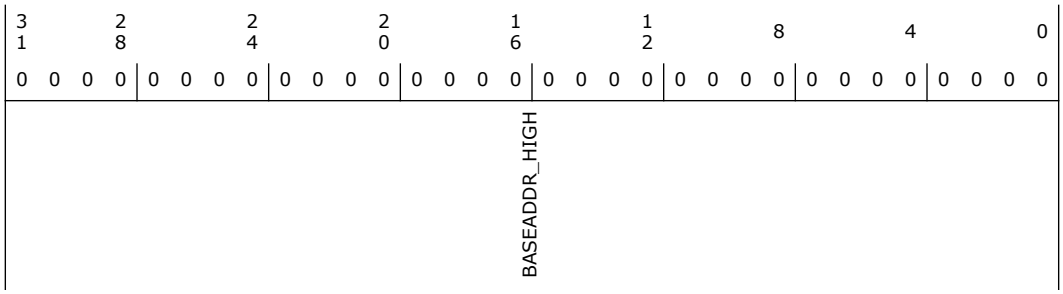
25.1.6 Memory Base Address Register High (BAR_HIGH)—Offset 14h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 19
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Base Address High (BASEADDR_HIGH)**

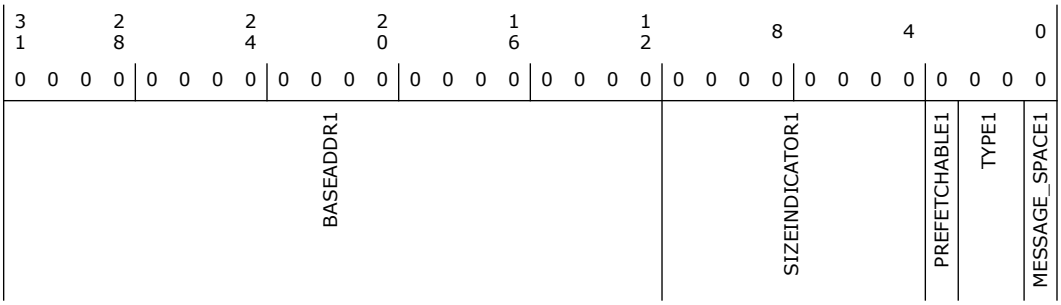
25.1.7 Memory Base Address 1 (BAR1)—Offset 18h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 19
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW	**BASEADDR1**
11:4	0h RO	**SIZEINDICATOR1**
3	0h RO	**PREFETCHABLE1**
2:1	0h RO	**TYPE1**
0	0h RO	**Message Space 1 (MESSAGE_SPACE1)**

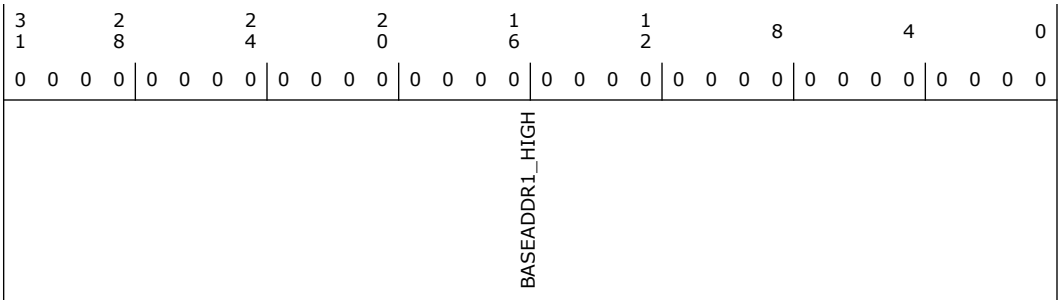
25.1.8 Memory Base Address 1 High (BAR1_HIGH)—Offset 1Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 19
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Base Address 1 High (BASEADDR1_HIGH)**

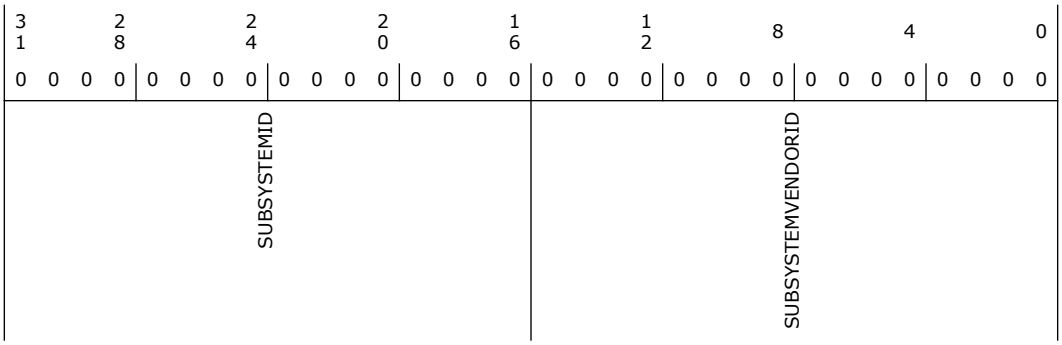
25.1.9 Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 19
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW/O	**Subsystem ID (SUBSYSTEMID):** This register field, in combination with the Sub System Vendor ID register field, enables the operating system (OS) to distinguish subsystems from each other. Note: Software can write to this register only once per core well reset. Writes should be done as a single 16-bit cycle.
15:0	0h RW/O	**Sub System Vendor ID (SUBSYSTEMVENDORID):** This register field, in combination with the Subsystem ID register field, enables the operating system (OS) to distinguish subsystems from each other. Note: Software can write to this register only once per core well reset. Writes should be done as a single 16-bit cycle.

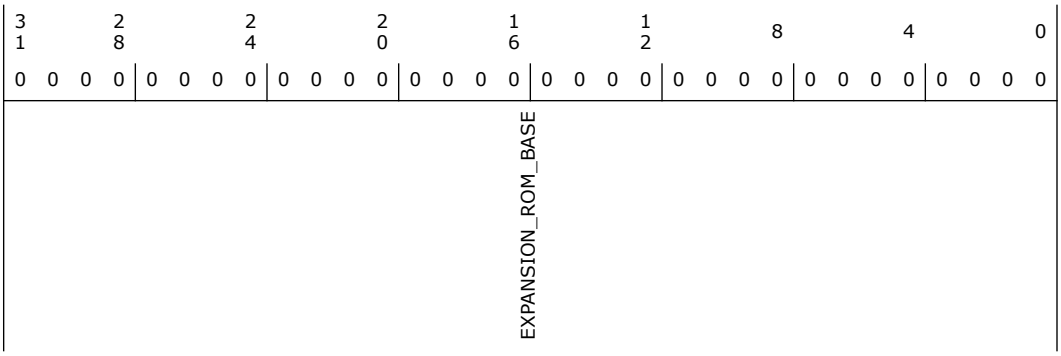
25.1.10 Expansion ROM base address (EXPANSION_ROM_BASEADDR)—Offset 30h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 19
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**Expansion ROM Base Address (EXPANSION_ROM_BASE)**

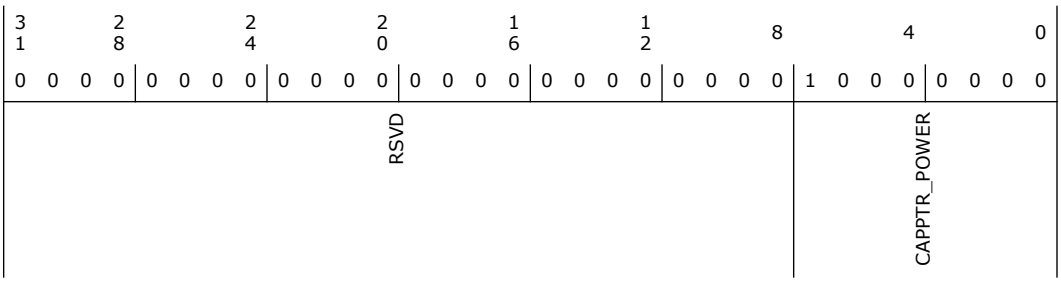
25.1.11 Capabilities Pointer (CAPABILITYPTR)—Offset 34h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 19
Function: 0

Default: 80h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	80h RO	**Power Capability Pointer (CAPPTR_POWER)**

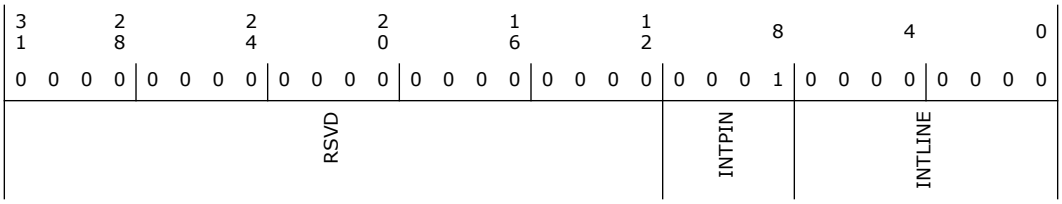
25.1.12 Interrupt (INTERRUPTREG)—Offset 3Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 19
Function: 0

Default: 100h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	Reserved.
11:8	1h RO	**Interrupt Pin (INTPIN):** Hardwired to 1.
7:0	0h RW	**Interrupt Line (INTLINE):** This data is not used by the PCH. It is to communicate to software the interrupt line that the interrupt pin is connected to.

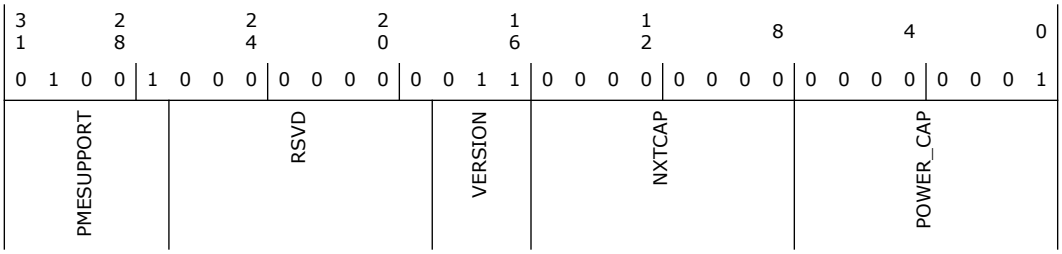
25.1.13 PowerManagement Capability ID (POWERCAPID)—Offset 80h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 19
Function: 0

Default: 48030001h



Bit Range	Default & Access	Field Name (ID): Description
31:27	9h RO	**PME Support (PMESUPPORT)**
26:19	0h RO	Reserved.
18:16	3h RO	**Version (VERSION)**
15:8	0h RO	**Next Capability (NXTCAP)**
7:0	1h RO	**Power Management Cap ID (POWER_CAP):** Hardwired to 1. Indicates that this pointer is a PCI power management capability.

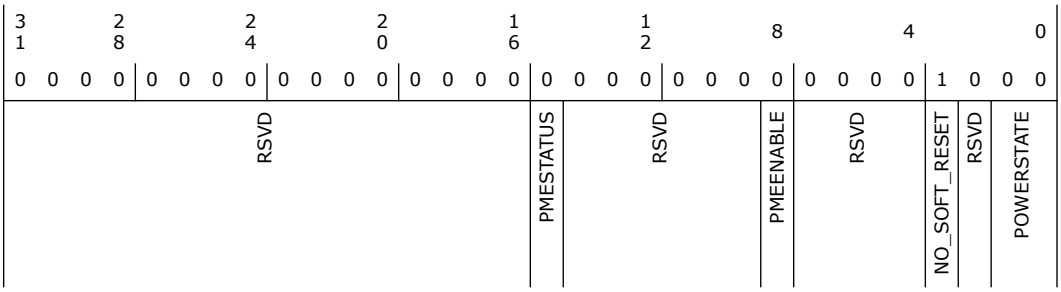
25.1.14 Power Management Control and Status (PMECTRLSTATUS)—Offset 84h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 19
Function: 0

Default: 8h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	0h RW/1C	**PME Status (PMESTATUS)**
14:9	0h RO	Reserved.
8	0h RW	**PME Enable (PMEENABLE)**
7:4	0h RO	Reserved.
3	1h RO	**No Soft Reset (NO_SOFT_RESET)**
2	0h RO	Reserved.
1:0	0h RW	**Power State (POWERSTATE):** This field is used both to determine the current power state and to set a new power state.

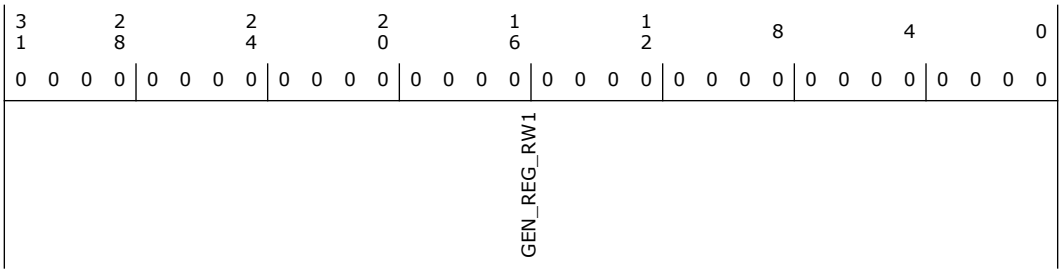
25.1.15 General Purpose Read Write Register1 (GEN_REGRW1)—Offset A0h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 19
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**General Purpose RW (GEN_REG_RW1)**

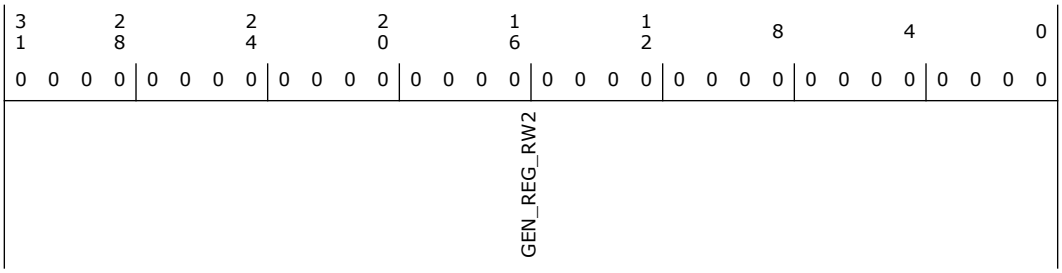
25.1.16 General Purpose Read Write Register2 (GEN_REGRW2)—Offset A4h

Access Method

Type: CFG Register (Size: 32 bits)

Device: 19
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**General Purpose Read Write Register2 (GEN_REG_RW2)**

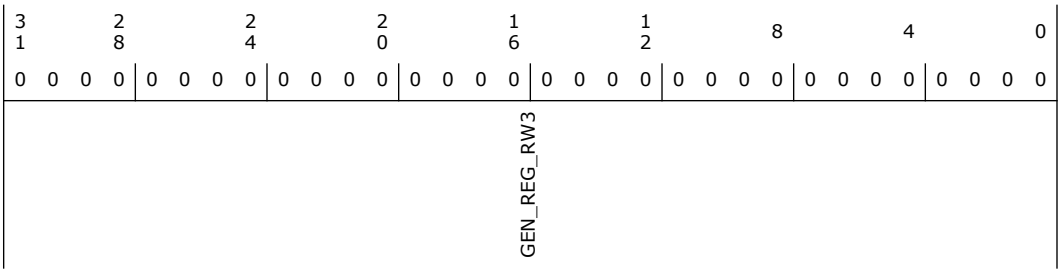
25.1.17 General Purpose Read Write Register3 (GEN_REGRW3)—Offset A8h

Access Method

Type: CFG Register (Size: 32 bits)

Device: 19
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**General Purpose Read Write Register3 (GEN_REG_RW3)**

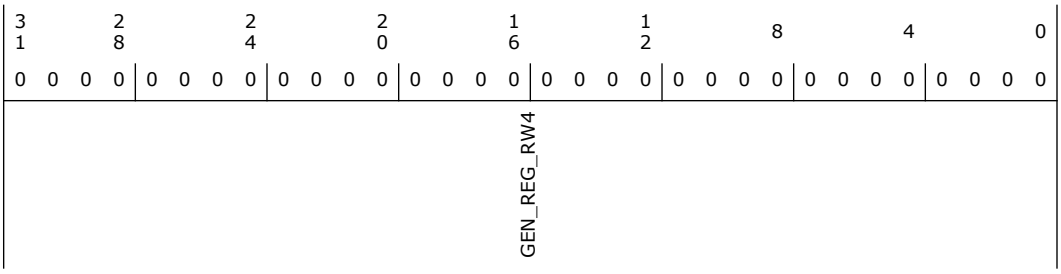
25.1.18 General Purpose Read Write Register4 (GEN_REGRW4)—Offset ACh

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 19
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**General Purpose Read Write Register4 (GEN_REG_RW4)**

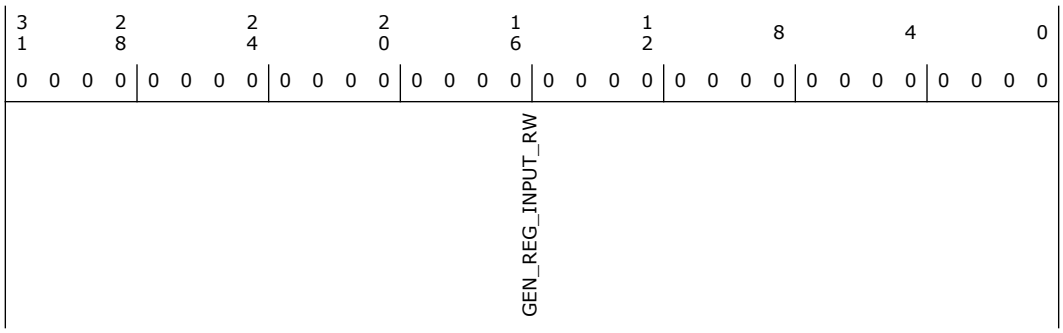
25.1.19 General Purpose Input Register (GEN_INPUT_REG)—Offset C0h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 19
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**General Purpose Input Register (GEN_REG_INPUT_RW)**

25.2 ISH MMIO Registers Summary

Table 25-2. Summary of ISH MMIO Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
34h	37h	ISH Host firmware status (ISH_HOST_FWSTS)—Offset 34h	0h
38h	3Bh	Host Communication (HOST_COMM)—Offset 38h	0h
48h	4Bh	(HOST2ISH_DOORBELL)—Offset 48h	0h
54h	57h	ISH-to-Host DoorBell (ISH2HOST_DOORBELL)—Offset 54h	0h
60h	63h	Message from ISH to HOST (ISH2HOST_MSG)—Offset 60h	0h
E0h	E3h	Message from HOST to ISH (HOST2ISH_MSG1)—Offset E0h	0h
360h	363h	ISH Remap (REMAP)—Offset 360h	0h
6D0h	6D3h	D0i3 Control (IPC_d0i3C_reg)—Offset 6D0h	8h

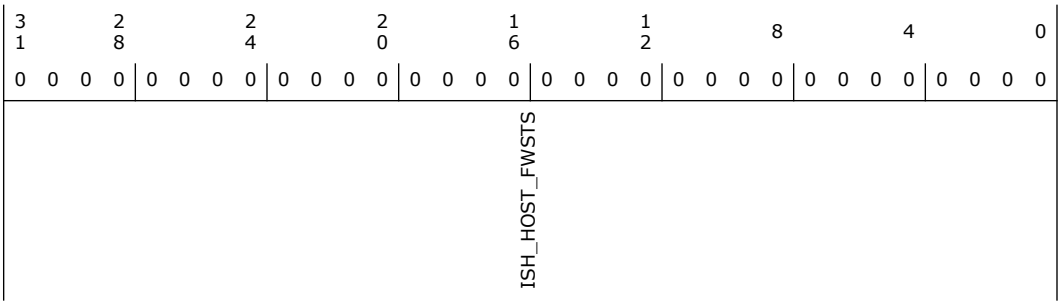
25.2.1 ISH Host firmware status (ISH_HOST_FWSTS)—Offset 34h

Access Method

Type: MEM Register (Size: 32 bits)

Device: 19
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**ISH Host firmware status (ISH_HOST_FWSTS):** This is a 32 bit register which is set to 0 on a system reset or a wakeup from D3Cold. As the ISH firmware comes up after the reset or power cycle it sets bits of this register to indicate its status. There is no interrupt associated with writes or reads to this register.

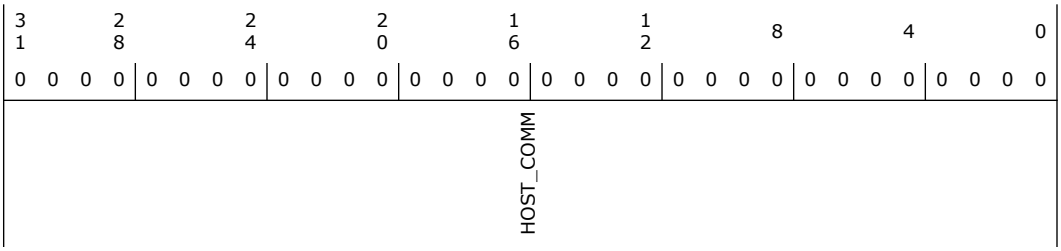
25.2.2 Host Communication (HOST_COMM)—Offset 38h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 19
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Host Communication (HOST_COMM):** This is a 32 bit register which is set to 0 on a system reset or a wakeup from D3Cold. As the Host CPU firmware comes up after the reset or power cycle, it sets bits of this register to indicate its status. There is no interrupt associated with writes or reads to this register.

25.2.3 (HOST2ISH_DOORBELL)—Offset 48h

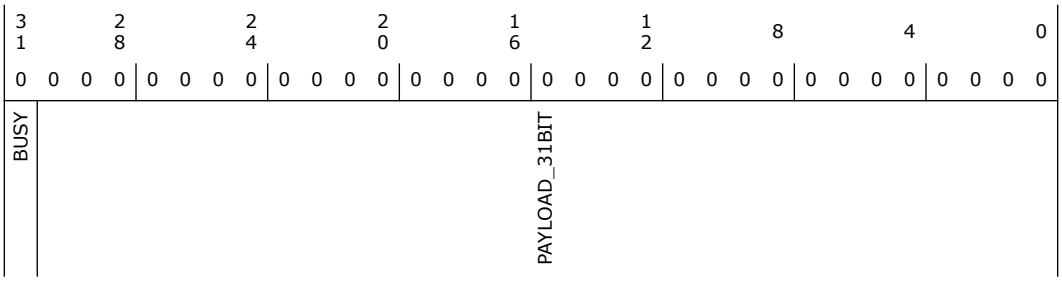
HOST writes to this register, via IOSF-primary using MMIO Write semantics.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 19
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**BUSY (BUSY):** Write a 1 to this bit, from IOSF-PRIMARY by HOST, to cause an interrupt to ISH.
30:0	0h RW	**PAYLOAD_31BIT (PAYLOAD_31BIT):** HOST SW provides indications about the doorbell with [30:0] bits. ISH FW provides acknowledge response of the IPC Message with these bits. These bits have no meaning to hardware.

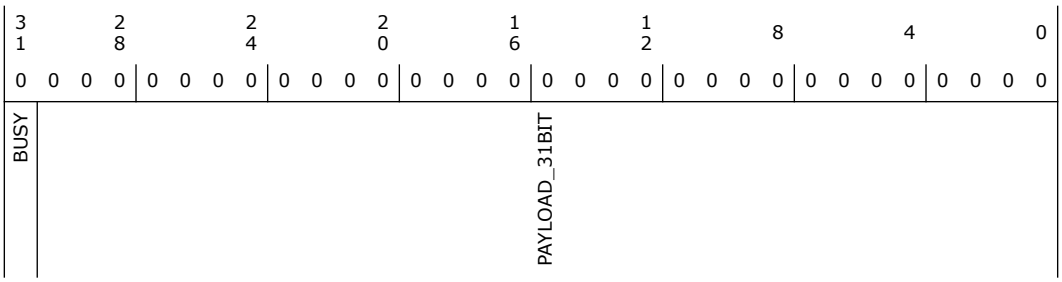
25.2.4 ISH-to-Host DoorBell (ISH2HOST_DOORBELL)—Offset 54h

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 19
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**BUSY (BUSY):** Write a 1 to this bit, by ISH, to cause an interrupt to HOST. Write a 0, from HOST using IOSF-PRIMARY MMIO Write semantics, to this bit to deassert interrupt to HOST AND will also to cause an interrupt to ISH.
30:0	0h RW	**PAYLOAD_31BIT (PAYLOAD_31BIT):** ISH FW provides indications about the doorbell with [30:0] bits. HOST SW provides acknowledge response of the IPC Message with these bits. These bits have no meaning to hardware.

25.2.5 Message from ISH to HOST (ISH2HOST_MSG)—Offset 60h

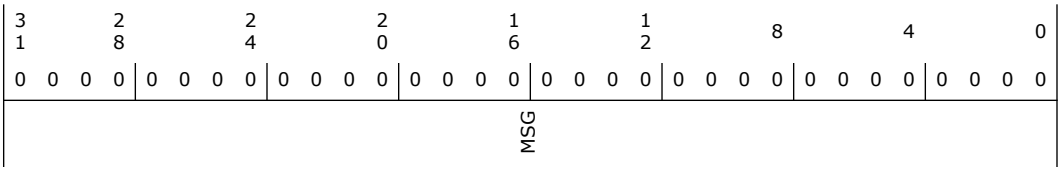
This is a set of 32 registers of 32 bits each (128 bytes total). These registers are available from offset 60h to DCh.
ISH FW will write to these registers.
HOST will read from these registers, using IOSF-PRIMARY MMIO Read semantics, when the ISH2HOST Doorbell bit is written to “1” (indicated via IRQx interrupt).

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 19
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**Message (MSG):** This is used in conjunction with the ISH2HOST Doorbell. ISH FW will write the message to the message register, and then write to the doorbell to interrupt HOST. HOST will then read the ISH2HOST Message register.

25.2.6 Message from HOST to ISH (HOST2ISH_MSG1)—Offset E0h

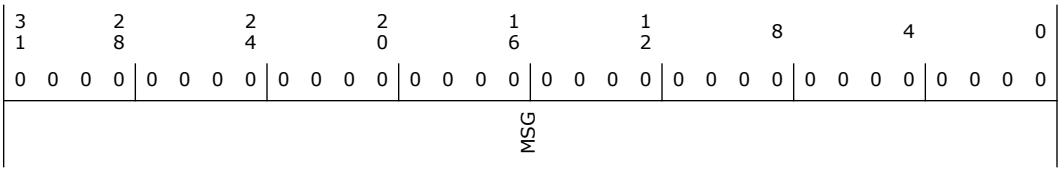
This is a set of 32 registers of 32 bits each (128 bytes total). These register are available at offset from E0h to 15Ch
HOST will write to these registers, using IOSF-PRIMARY MMIO Write semantics.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 19
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Message (MSG):** This is used in conjunction with the HOST2ISH Doorbell. HOST will write the message to the message register, and then write to the doorbell to interrupt the ISH. ISH will then read the HOST2ISH Message register.

25.2.7 ISH Remap (REMAP)—Offset 360h

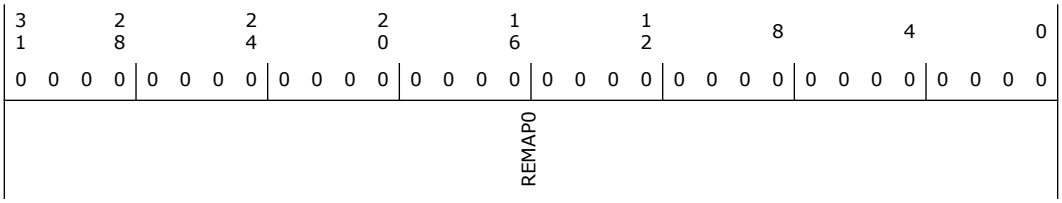
This is a set of 6 registers of 32 bits each (24 bytes total). These registers are available from offset 360h to 374h.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 19
Function: 0

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Remap (REMAP0):** To the Host CPU, each of these registers (1 dword each) appears as a write-once register; it has no specific behaviors other than storing the write data and making it available for reads. At boot time, the Host can write these registers with any dynamically allocated address spaces that ISH will have to access.

25.2.8 D0i3 Control (IPC_d0i3C_reg)—Offset 6D0h

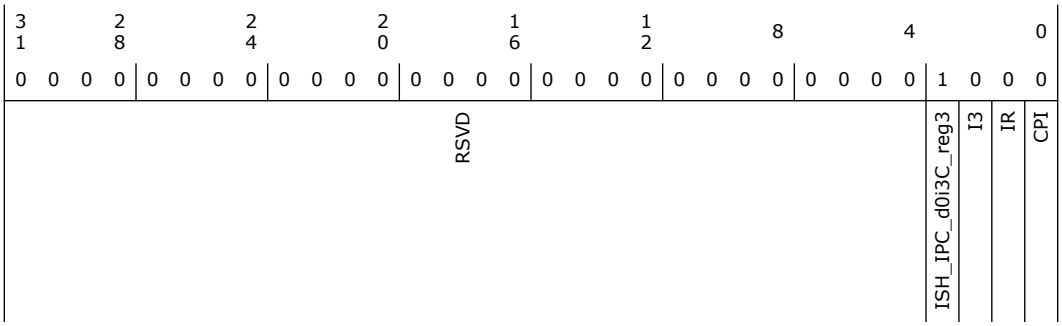
This register provides D0i3 support and also provides support for interrupt generation.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 19
Function: 0

Default: 8h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3	1h RO	**ISH_IPC_d0i3C_reg3:** ish_clk

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**D0I3 (I3):** SW sets this bit to '1' to move the controller into the D0i3 state. Writing this bit to '0' will return the controller to the fully active D0 state (D0i0). Note that this bit is treated by ISH FW as an D0i3 allow indication from SW. This means that if this bit is set to 1, then ISH may be in D0i3 state and if this bit is set to 0, then ISH is precluded from being in D0i3 state.
1	0h RW	**Interrupt Request (IR):** SW sets this bit to '1' to ask for an interrupt to be generated on completion of the command. SW must clear or set this on each write to this register.
0	0h RO	**Command in Progress (CPI):** HW sets this bit on a 1->0 or 0->1 transition of bit [2]. While set, the other bits in this register are not valid and it is illegal for SW to write to any bit in this register. When clear all the other bits in the register are valid and SW may write to any bit. ISH FW will clear this bit, upon internal logging of the D0i3 allow/disallow (1 or 0 state of bit[2]) indication.

§ §

26 8254 Timer

26.1 8254 Timer Registers Summary

Table 26-1. Summary of 8254 Timer Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
40h	40h	Counter 0 - Interval Timer Status Byte Format Register (C0_ITSBFR)—Offset 40h	C4h
40h	40h	Counter 0 - Counter Access Ports Register (C0_CAPR)—Offset 40h	0h
42h	42h	Counter 2 - Interval Timer Status Byte Format Register (C2_ITSBFR)—Offset 42h	0h
42h	42h	Counter 2 - Counter Access Ports Register (C2_CAPR)—Offset 42h	0h
43h	43h	Timer Control Word Register (TCW)—Offset 43h	0h
43h	43h	Read Back Command (RBC)—Offset 43h	C0h
43h	43h	Counter Latch Command (CLC)—Offset 43h	0h

26.1.1 Counter 0 - Interval Timer Status Byte Format Register (C0_ITSBFR)—Offset 40h

Each counter's status byte can be read following a Read Back Command. If latch status is chosen (bit 4=0, Read Back Command) as a read back option for a given counter, the next read from the counter's Counter Access Ports Register (40h for counter 0 and 42h for counter 2) returns the status byte. The status byte returns the following:

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: C4h

7			4				0
1	1	0	0	0	1	0	0
COPS	CRSTS	RW_SLT_STS		MD_SLT_STS			CDT_STS

Bit Range	Default & Access	Field Name (ID): Description
7	1h RO	**Counter OUT Pin State (COPS):** When this bit is a 1, the OUT pin of the counter is also a 1. When this bit is a 0, the OUT pin of the counter is also a 0.
6	1h RO	**Count Register Status (CRSTS):** This bit indicates when the last count written to the Count Register (CR) has been loaded into the counting element (CE). The exact time this happens depends on the counter mode, but until the count is loaded into the counting element (CE), the count value will be incorrect. 0 Count has been transferred from CR to CE and is available for reading. 1 Null Count. Count has not been transferred from CR to CE and is not yet available for reading.
5:4	0h RO	**Read/Write Selection Status (RW_SLT_STS):** These reflect the read/write selection made through bits[5:4] of the control register. The binary codes returned during the status read match the codes used to program the counter read/write selection. 00 Counter Latch Command 01 Read/Write Least Significant Byte (LSB) 10 Read/Write Most Significant Byte (MSB) 11 Read/Write LSB then MSB
3:1	2h RO	**Mode Selection Status (MD_SLT_STS):** These bits return the counter mode programming. The binary code returned matches the code used to program the counter mode, as listed under the bit function above. 000 0 Out signal on end of count (=0) 001 1 Hardware retriggerable one-shot x10 2 Rate generator (divide by n counter) x11 3 Square wave output 100 4 Software triggered strobe 101 5 Hardware triggered strobe
0	0h RO	**Countdown Type Status (CDT_STS):** This bit reflects the current countdown type, ether 0 for binary countdown or a 1 for binary coded decimal (BCD) countdown.

26.1.2 Counter 0 - Counter Access Ports Register (C0_CAPR)—Offset 40h

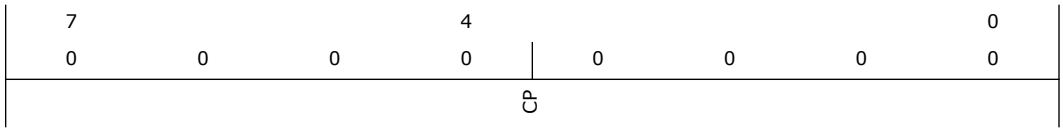
*Address should be 40h

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**Counter Port (CP):** Each counter port address is used to program the 16-bit Count Register. The order of programming, either LSB only, MSB only, or LSB then MSB, is defined with the Interval Counter Control Register at port 43h. The counter port is also used to read the current count from the Count Register, and return the status of the counter programming following a Read Back Command.

26.1.3 Counter 2 - Interval Timer Status Byte Format Register (C2_ITSBFR)—Offset 42h

Same definition as counter 0

26.1.4 Counter 2 - Counter Access Ports Register (C2_CAPR)—Offset 42h

Same definition as Counter 0 - Counter Access Ports Register

26.1.5 Timer Control Word Register (TCW)—Offset 43h

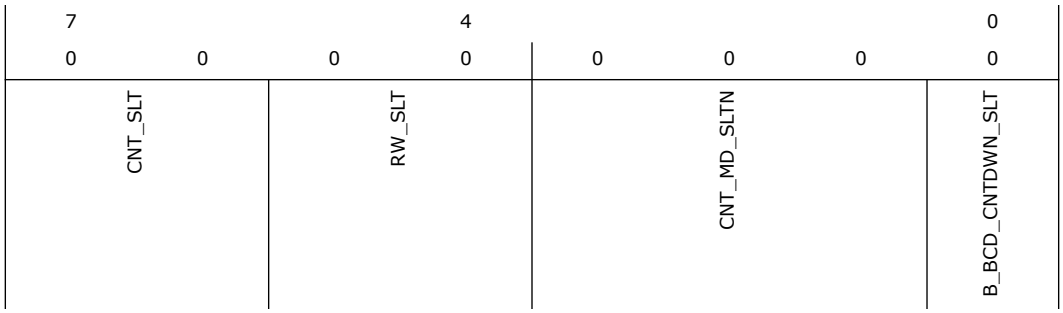
This register is programmed prior to any counter being accessed to specify counter modes. Following reset, the control words for each register are undefined and each counter output is 0. Each timer must be programmed to bring it into a known state. There are two special commands that can be issued to the counters through this register, the Read Back Command and the Counter Latch Command. When these commands are chosen, several bits within this register are redefined.

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7:6	0h WO	**Counter Select (CNT_SLT):** The Counter Selection bits select the counter the control word acts upon as shown below. The Read Back Command is selected when bits[7:6] are both 1 00 Counter 0 select 01 Reserved 10 Counter 2 select 11 Read Back Command
5:4	0h WO	**Read/Write Select: (RW_SLT):** These bits are the read/write control bits. The actual counter programming is done through the counter port (40h for counter 0 and 42h for counter 2) 00 Counter Latch Command 01 Read/Write Least Significant Byte (LSB) 10 Read/Write Most Significant Byte (MSB) 11 Read/Write LSB then MSB
3:1	0h WO	**Counter Mode Selection (CNT_MD_SLTN):** These bits select one of six possible modes of operation for the selected counter. 000 0 Out signal on end of count (=0) 001 1 Hardware retriggerable one-shot x10 2 Rate generator (divide by n counter) x11 3 Square wave output 100 4 Software triggered strobe 101 5 Hardware triggered strobe
0	0h WO	**Binary/BCD Countdown Select (B_BCD_CNTDWN_SLT):** 0 Binary countdown is used. The largest possible binary count is 2^16 1 Binary coded decimal (BCD) count is used.The largest possible BCD count is 10^4

26.1.6 Read Back Command (RBC)—Offset 43h

The Read Back Command is used to determine the count value, programmed mode, and current states of the OUT pin and Null count flag of the selected counter or counters. Status and/or count may be latched in any or all of the counters by selecting the counter during the register write. The count and status remain latched until read, and further latch commands are ignored until the count is read.
Both count and status of the selected counters may be latched simultaneously by setting both bit 5 and bit 4 to 0. If both are latched, the first read operation from that counter returns the latched status. The next one or two reads, depending on whether the counter is programmed for one or two byte counts, returns the latched count. Subsequent reads return an unlatched count.

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: C0h

7				4			0
1	1	0	0	0	0	0	0
RBC		LCSC	LSSC	CNT_2_SLT	RSVD	CNT_0_SLT	RSVD

Bit Range	Default & Access	Field Name (ID): Description
7:6	3h WO	**Read Back Command (RBC):** Must be 11 to select the Read Back Command
5	0h WO	**Latch Count of Selected Counters (LCSC):** 0 Current count value of the selected counters will be latched 1 Current count will not be latched
4	0h WO	**Latch Status of Selected Counters (LSSC):** 0 Status of the selected counters will be latched 1 Status will not be latched
3	0h WO	**Counter 2 Select (CNT_2_SLT):** When set to 1, Counter 2 count and/or status will be latched
2	0h RO	Reserved.
1	0h WO	**Counter 0 Select (CNT_0_SLT):** When set to 1, Counter 0 count and/or status will be latched.
0	0h RO	Reserved.

26.1.7 Counter Latch Command (CLC)—Offset 43h

The Counter Latch Command latches the current count value. This command is used to insure that the count read from the counter is accurate. The count value is then read from each counter's count register through the Counter Ports Access Ports Register (40h for counter 0 and 42h for counter 2). The count must be read according to the programmed format, i.e. if the counter is programmed for two byte counts, two bytes

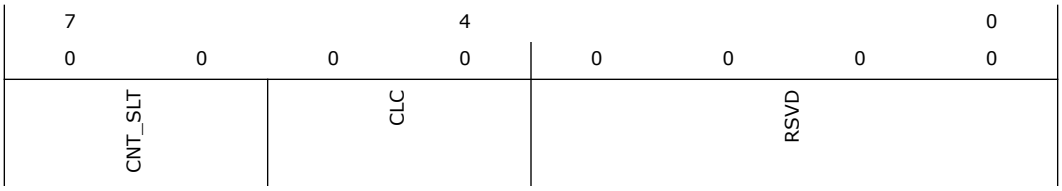
must be read. The two bytes do not have to be read one right after the other (read, write, or programming operations for other counters may be inserted between the reads). If a counter is latched once and then latched again before the count is read, the second Counter Latch Command is ignored.

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7:6	0h WO	**Counter Selection (CNT_SLT):** These bits select the counter for latching. If 11 is written, then the write is interpreted as a read back command. 00 = Counter 0 01 = Reserved 10 = Counter 2
5:4	0h WO	**Counter Latch Command (CLC):** Write 00 to select the Counter Latch Command.
3:0	0h RO	Reserved.

§ §

27 Advanced Programmable Interrupt (APIC)

27.1 APIC Indirect Registers Summary

APIC Indirect Registers lists the registers that can be accessed within the APIC using the Index Register. When accessing these registers, accesses must be done one DWord at a time. For example, software should never access byte 2 from the Data register before accessing bytes 0 and 1. The hardware will not attempt to recover from a bad programming model in this case.

Index Mnemonic Register Name
10-11h RTE0 Redirection Table Entry 0
12-13h RTE1 Redirection Table Entry 1
14-15h RTE2 Redirection Table Entry 2
... ...
3E-3Fh RTE23 Redirection Table Entry 23
40-41h RTE24 Redirection Table Entry 24
... ...
FE-FFh RTE119 Redirection Table Entry 119

Table 27-1. Summary of APIC Indirect Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	Identification Register (ID)—Offset 0h	0h
1h	4h	Version Register (VER)—Offset 1h	770020h
10h	17h	Redirection Table Entry 0 (RTE0)—Offset 10h	10000h
12h	19h	Redirection Table Entry 1 (RTE1)—Offset 12h	0h
14h	1Bh	Redirection Table Entry 2 (RTE2)—Offset 14h	0h
16h	1Dh	Redirection Table Entry 3 (RTE3)—Offset 16h	0h
18h	1Fh	Redirection Table Entry 4 (RTE4)—Offset 18h	0h
1Ah	21h	Redirection Table Entry 5 (RTE5)—Offset 1Ah	0h
1Ch	23h	Redirection Table Entry 6 (RTE6)—Offset 1Ch	0h
1Eh	25h	Redirection Table Entry 7 (RTE7)—Offset 1Eh	0h
20h	27h	Redirection Table Entry 8 (RTE8)—Offset 20h	0h
22h	29h	Redirection Table Entry 9 (RTE9)—Offset 22h	0h
24h	2Bh	Redirection Table Entry 10 (RTE10)—Offset 24h	0h
26h	2Dh	Redirection Table Entry 11 (RTE11)—Offset 26h	0h
28h	2Fh	Redirection Table Entry 12 (RTE12)—Offset 28h	0h
2Ah	31h	Redirection Table Entry 13 (RTE13)—Offset 2Ah	0h
2Ch	33h	Redirection Table Entry 14 (RTE14)—Offset 2Ch	0h
2Eh	35h	Redirection Table Entry 15 (RTE15)—Offset 2Eh	0h
30h	37h	Redirection Table Entry 16 (RTE16)—Offset 30h	0h
32h	39h	Redirection Table Entry 17 (RTE17)—Offset 32h	0h
34h	3Bh	Redirection Table Entry 18 (RTE18)—Offset 34h	0h

Table 27-1. Summary of APIC Indirect Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
36h	3Dh	Redirection Table Entry 19 (RTE19)—Offset 36h	0h
38h	3Fh	Redirection Table Entry 20 (RTE20)—Offset 38h	0h
3Ah	41h	Redirection Table Entry 21 (RTE21)—Offset 3Ah	0h
3Ch	43h	Redirection Table Entry 22 (RTE22)—Offset 3Ch	0h
3Eh	45h	Redirection Table Entry 23 (RTE23)—Offset 3Eh	0h
40h	47h	Redirection Table Entry 24 (RTE24)—Offset 40h	0h
42h	49h	Redirection Table Entry 25 (RTE25)—Offset 42h	0h
44h	4Bh	Redirection Table Entry 26 (RTE26)—Offset 44h	0h
46h	4Dh	Redirection Table Entry 27 (RTE27)—Offset 46h	0h
48h	4Fh	Redirection Table Entry 28 (RTE28)—Offset 48h	0h
4Ah	51h	Redirection Table Entry 29 (RTE29)—Offset 4Ah	0h
4Ch	53h	Redirection Table Entry 30 (RTE30)—Offset 4Ch	0h
4Eh	55h	Redirection Table Entry 31 (RTE31)—Offset 4Eh	0h
50h	57h	Redirection Table Entry 32 (RTE32)—Offset 50h	0h
52h	59h	Redirection Table Entry 33 (RTE33)—Offset 52h	0h
54h	5Bh	Redirection Table Entry 34 (RTE34)—Offset 54h	0h
56h	5Dh	Redirection Table Entry 35 (RTE35)—Offset 56h	0h
58h	5Fh	Redirection Table Entry 36 (RTE36)—Offset 58h	0h
5Ah	61h	Redirection Table Entry 37 (RTE37)—Offset 5Ah	0h
5Ch	63h	Redirection Table Entry 38 (RTE38)—Offset 5Ch	0h
5Eh	65h	Redirection Table Entry 39 (RTE39)—Offset 5Eh	0h
60h	67h	Redirection Table Entry 40 (RTE40)—Offset 60h	0h
62h	69h	Redirection Table Entry 41 (RTE41)—Offset 62h	0h
64h	6Bh	Redirection Table Entry 42 (RTE42)—Offset 64h	0h
66h	6Dh	Redirection Table Entry 43 (RTE43)—Offset 66h	0h
68h	6Fh	Redirection Table Entry 44 (RTE44)—Offset 68h	0h
6Ah	71h	Redirection Table Entry 45 (RTE45)—Offset 6Ah	0h
6Ch	73h	Redirection Table Entry 46 (RTE46)—Offset 6Ch	0h
6Eh	75h	Redirection Table Entry 47 (RTE47)—Offset 6Eh	0h
70h	77h	Redirection Table Entry 48 (RTE48)—Offset 70h	0h
72h	79h	Redirection Table Entry 49 (RTE49)—Offset 72h	0h
74h	7Bh	Redirection Table Entry 50 (RTE50)—Offset 74h	0h
76h	7Dh	Redirection Table Entry 51 (RTE51)—Offset 76h	0h
78h	7Fh	Redirection Table Entry 52 (RTE52)—Offset 78h	0h
7Ah	81h	Redirection Table Entry 53 (RTE53)—Offset 7Ah	0h
7Ch	83h	Redirection Table Entry 54 (RTE54)—Offset 7Ch	0h
7Eh	85h	Redirection Table Entry 55 (RTE55)—Offset 7Eh	0h
80h	87h	Redirection Table Entry 56 (RTE56)—Offset 80h	0h
82h	89h	Redirection Table Entry 57 (RTE57)—Offset 82h	0h
84h	8Bh	Redirection Table Entry 58 (RTE58)—Offset 84h	0h

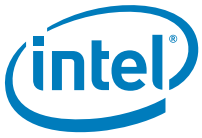


Table 27-1. Summary of APIC Indirect Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
86h	8Dh	Redirection Table Entry 59 (RTE59)—Offset 86h	0h
88h	8Fh	Redirection Table Entry 60 (RTE60)—Offset 88h	0h
8Ah	91h	Redirection Table Entry 61 (RTE61)—Offset 8Ah	0h
8Ch	93h	Redirection Table Entry 62 (RTE62)—Offset 8Ch	0h
8Eh	95h	Redirection Table Entry 63 (RTE63)—Offset 8Eh	0h
90h	97h	Redirection Table Entry 64 (RTE64)—Offset 90h	0h
92h	99h	Redirection Table Entry 65 (RTE65)—Offset 92h	0h
94h	9Bh	Redirection Table Entry 66 (RTE66)—Offset 94h	0h
96h	9Dh	Redirection Table Entry 67 (RTE67)—Offset 96h	0h
98h	9Fh	Redirection Table Entry 68 (RTE68)—Offset 98h	0h
9Ah	A1h	Redirection Table Entry 69 (RTE69)—Offset 9Ah	0h
9Ch	A3h	Redirection Table Entry 70 (RTE70)—Offset 9Ch	0h
9Eh	A5h	Redirection Table Entry 71 (RTE71)—Offset 9Eh	0h
A0h	A7h	Redirection Table Entry 72 (RTE72)—Offset A0h	0h
A2h	A9h	Redirection Table Entry 73 (RTE73)—Offset A2h	0h
A4h	ABh	Redirection Table Entry 74 (RTE74)—Offset A4h	0h
A6h	ADh	Redirection Table Entry 75 (RTE75)—Offset A6h	0h
A8h	AFh	Redirection Table Entry 76 (RTE76)—Offset A8h	0h
AAh	B1h	Redirection Table Entry 77 (RTE77)—Offset AAh	0h
ACh	B3h	Redirection Table Entry 78 (RTE78)—Offset ACh	0h
AEh	B5h	Redirection Table Entry 79 (RTE79)—Offset AEh	0h
B0h	B7h	Redirection Table Entry 80 (RTE80)—Offset B0h	0h
B2h	B9h	Redirection Table Entry 81 (RTE81)—Offset B2h	0h
B4h	BBh	Redirection Table Entry 82 (RTE82)—Offset B4h	0h
B6h	BDh	Redirection Table Entry 83 (RTE83)—Offset B6h	0h
B8h	BFh	Redirection Table Entry 84 (RTE84)—Offset B8h	0h
BAh	C1h	Redirection Table Entry 85 (RTE85)—Offset BAh	0h
BCh	C3h	Redirection Table Entry 86 (RTE86)—Offset BCh	0h
BEh	C5h	Redirection Table Entry 87 (RTE87)—Offset BEh	0h
C0h	C7h	Redirection Table Entry 88 (RTE88)—Offset C0h	0h
C2h	C9h	Redirection Table Entry 89 (RTE89)—Offset C2h	0h
C4h	CBh	Redirection Table Entry 90 (RTE90)—Offset C4h	0h
C6h	CDh	Redirection Table Entry 91 (RTE91)—Offset C6h	0h
C8h	CFh	Redirection Table Entry 92 (RTE92)—Offset C8h	0h
CAh	D1h	Redirection Table Entry 93 (RTE93)—Offset CAh	0h
CCh	D3h	Redirection Table Entry 94 (RTE94)—Offset CCh	0h
CEh	D5h	Redirection Table Entry 95 (RTE95)—Offset CEh	0h
D0h	D7h	Redirection Table Entry 96 (RTE96)—Offset D0h	0h
D2h	D9h	Redirection Table Entry 97 (RTE97)—Offset D2h	0h
D4h	DBh	Redirection Table Entry 98 (RTE98)—Offset D4h	0h

Table 27-1. Summary of APIC Indirect Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
D6h	DDh	Redirection Table Entry 99 (RTE99)—Offset D6h	0h
D8h	DFh	Redirection Table Entry 100 (RTE100)—Offset D8h	0h
DAh	E1h	Redirection Table Entry 101 (RTE101)—Offset DAh	0h
DCh	E3h	Redirection Table Entry 102 (RTE102)—Offset DCh	0h
DEh	E5h	Redirection Table Entry 103 (RTE103)—Offset DEh	0h
E0h	E7h	Redirection Table Entry 104 (RTE104)—Offset E0h	0h
E2h	E9h	Redirection Table Entry 105 (RTE105)—Offset E2h	0h
E4h	EBh	Redirection Table Entry 106 (RTE106)—Offset E4h	0h
E6h	EDh	Redirection Table Entry 107 (RTE107)—Offset E6h	0h
E8h	EFh	Redirection Table Entry 108 (RTE108)—Offset E8h	0h
EAh	F1h	Redirection Table Entry 109 (RTE109)—Offset EAh	0h
ECh	F3h	Redirection Table Entry 110 (RTE110)—Offset ECh	0h
EEh	F5h	Redirection Table Entry 111 (RTE111)—Offset EEh	0h
F0h	F7h	Redirection Table Entry 112 (RTE112)—Offset F0h	0h
F2h	F9h	Redirection Table Entry 113 (RTE113)—Offset F2h	0h
F4h	FBh	Redirection Table Entry 114 (RTE114)—Offset F4h	0h
F6h	FDh	Redirection Table Entry 115 (RTE115)—Offset F6h	0h
F8h	FFh	Redirection Table Entry 116 (RTE116)—Offset F8h	0h
FAh	101h	Redirection Table Entry 117 (RTE117)—Offset FAh	0h
FCh	103h	Redirection Table Entry 118 (RTE118)—Offset FCh	0h
FEh	105h	Redirection Table Entry 119 (RTE119)—Offset FEh	0h

27.1.1 Identification Register (ID)—Offset 0h

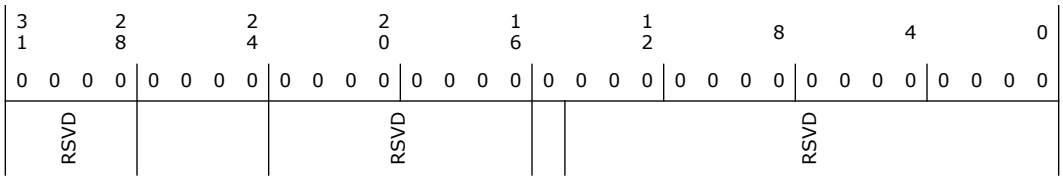
This APIC ID serves as a physical name of the APIC. The APIC bus arbitration ID for the APIC is derived from its I/O APIC ID. This register is reset to 0 on power-up reset.

Access Method

Type: APIC_IDX Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	Reserved.
27:24	0h RW	**APIC ID:** Software must program this value before using the APIC.
23:16	0h RO	Reserved.
15	0h RW	**Scratchpad**
14:0	0h RO	Reserved.

27.1.2 Version Register (VER)—Offset 1h

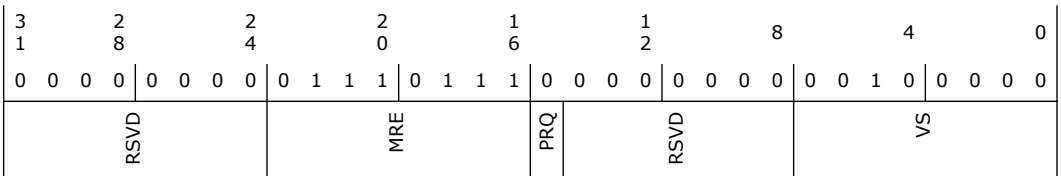
Each I/O APIC contains a hardwired Version Register that identifies different implementation of APIC and their versions. The maximum redirection entry information is also in this register to let software know how many interrupt are supported by this APIC.

Access Method

Type: APIC_IDX Register
(Size: 32 bits)

Device:
Function:

Default: 770020h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:16	77h RW/O	**Maximum Redirection Entries (MRE):** This is the entry number (0 being the lowest entry) of the highest entry in the redirection table. It is equal to the number of interrupt input pins minus one and is in the range of 0 through 239. In PCH this field is defaulted to 17h to indicate 24 interrupts. This field is Read-Write-Once. BIOS must write to this field after PLTRST# to lockdown the value. This allows BIOS to utilize some of the entries for its own purpose and thus advertising fewer IOxAPIC Redirection Entries to OS. BIOS may to program this field up to 78h (maximum 120 entries).
15	0h RO	**Pin Assertion Register Supported (PRQ):** Indicate that the IOxAPIC does not implement the Pin Assertion Register.
14:8	0h RO	Reserved.
7:0	20h RO	**Version (VS):** Identifies the implementation version as IOxAPIC.

27.1.3 Redirection Table Entry 0 (RTE0)—Offset 10h

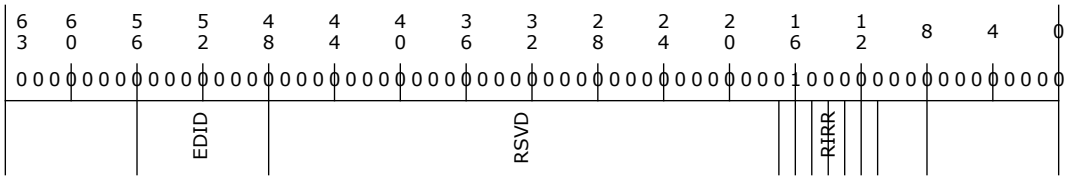
The Redirection Table has a dedicated entry for each interrupt input pin. The information in the Redirection Table is used to translate the interrupt manifestation on the corresponding interrupt pin into an APIC message.
The APIC will respond to an edge triggered interrupt as long as the interrupt is held until after the acknowledge cycle has begun. Once the interrupt is detected, a delivery status bit internally to the I/O APIC is set. The state machine will step ahead and wait for an ackledgement from the APIC unit that the interrupt message was sent. Only then will the I/O APIC be able to recognize a new edge on that interrupt pin. That new edge will only result in a new invocation of the handler if its acceptance by the destination APIC causes the Interrupt Request register bit to go from 0 to 1. (In other words, if the interrupt was not already pending a the destination.)

Access Method

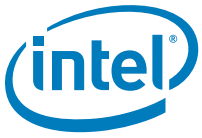
Type: APIC_IDX Register
(Size: 64 bits)

Device:
Function:

Default: 10000h



Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RW	**Destination:** If bit 11 of this entry is 0 (Physical), then bits 59:56 specifies an APIC ID. In this case, bits 63:59 should be programmed by software to 0. If bit 11 of this entry is 1 (Logical), then bits 63:56 specify the logical destination address of a set of processors.
55:48	0h RW	**Extended Destination ID (EDID):** These bits are sent to a local APIC only when in Processor System Bus mode. They become bits 11:4 of the address.
47:17	0h RO	Reserved.
16	1h RW	**Mask:** 0 = Not masked. An edge or level on this interrupt pin results in the delivery of the interrupt to the destination. 1 = Masked. Interrupts are not delivered nor held pending. Setting this bit after the interrupt is accepted by a local APIC has no effect on that interrupt. This behavior is identical to the device withdrawing the interrupt before it is posted to the processor. It is software's responsibility to deal with the case where the mask bit is set after the interrupt message has been accepted by a local APIC unit but before the interrupt is dispensed to the processor.
15	0h RW	**Trigger Mode:** This field indicates the type of signal on the interrupt pin that triggers an interrupt. 0 = The interrupt is edge sensitive. 1 = The interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts; its meaning is undefined for edge triggered interrupts. 0 = Reset when an EOI message is received that matches the VCT field. 1 = Set when IOxAPIC sends the level interrupt message to the CPU. Note, this bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Interrupt Input Pin Polarity:** This bit specifies the polarity of each interrupt signal connected to the interrupt pins. 0 = Signal is active high. 1 = Signal is active low.



Bit Range	Default & Access	Field Name (ID): Description
12	0h RO/V	**Delivery Status:** This field contains the current status of the delivery of this interrupt. 0 = Idle. There is no activity for this interrupt. 1 = Pending. An interrupt has been injected, but delivery is not complete. Note, writes to this bit have no effect.
11	0h RW	**Destination Mode:** This field is used by the local Apic to determine whether it is the destination of the message. 0 = Physical. Destination APIC ID is identified by bits 59:56. 1 = Logical. Destinations are identified by matching bit 63:56 with Logical Destination in the Destination Format register and Logical Destination register in each Local APIC.
10:8	0h RW	**Delivery Mode:** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported 011 Reserved 100 NMI Not supported 101 INIT Not supported 110 Reserved 111 ExtINT
7:0	0h RW	**Vector:** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

27.1.4 Redirection Table Entry 1 (RTE1)—Offset 12h

This register has the same bit definition as RTE0.

27.1.5 Redirection Table Entry 2 (RTE2)—Offset 14h

This register has the same bit definition as RTE0.

27.1.6 Redirection Table Entry 3 (RTE3)—Offset 16h

This register has the same bit definition as RTE0.

27.1.7 Redirection Table Entry 4 (RTE4)—Offset 18h

This register has the same bit definition as RTE0.

27.1.8 Redirection Table Entry 5 (RTE5)—Offset 1Ah

This register has the same bit definition as RTE0.

27.1.9 Redirection Table Entry 6 (RTE6)—Offset 1Ch

This register has the same bit definition as RTE0.

27.1.10 Redirection Table Entry 7 (RTE7)—Offset 1Eh

This register has the same bit definition as RTE0.

27.1.11 Redirection Table Entry 8 (RTE8)—Offset 20h

This register has the same bit definition as RTE0.

27.1.12 Redirection Table Entry 9 (RTE9)—Offset 22h

This register has the same bit definition as RTE0.

27.1.13 Redirection Table Entry 10 (RTE10)—Offset 24h

This register has the same bit definition as RTE0.

27.1.14 Redirection Table Entry 11 (RTE11)—Offset 26h

This register has the same bit definition as RTE0.

27.1.15 Redirection Table Entry 12 (RTE12)—Offset 28h

This register has the same bit definition as RTE0.

27.1.16 Redirection Table Entry 13 (RTE13)—Offset 2Ah

This register has the same bit definition as RTE0.

27.1.17 Redirection Table Entry 14 (RTE14)—Offset 2Ch

This register has the same bit definition as RTE0.

27.1.18 Redirection Table Entry 15 (RTE15)—Offset 2Eh

This register has the same bit definition as RTE0.

27.1.19 Redirection Table Entry 16 (RTE16)—Offset 30h

This register has the same bit definition as RTE0.

27.1.20 Redirection Table Entry 17 (RTE17)—Offset 32h

This register has the same bit definition as RTE0.

27.1.21 Redirection Table Entry 18 (RTE18)—Offset 34h

This register has the same bit definition as RTE0.

27.1.22 Redirection Table Entry 19 (RTE19)—Offset 36h

This register has the same bit definition as RTE0.

27.1.23 Redirection Table Entry 20 (RTE20)—Offset 38h

This register has the same bit definition as RTE0.

27.1.24 Redirection Table Entry 21 (RTE21)—Offset 3Ah

This register has the same bit definition as RTE0.

27.1.25 Redirection Table Entry 22 (RTE22)—Offset 3Ch

This register has the same bit definition as RTE0.

27.1.26 Redirection Table Entry 23 (RTE23)—Offset 3Eh

This register has the same bit definition as RTE0.

27.1.27 Redirection Table Entry 24 (RTE24)—Offset 40h

This register has the same bit definition as RTE0.

27.1.28 Redirection Table Entry 25 (RTE25)—Offset 42h

This register has the same bit definition as RTE0.

27.1.29 Redirection Table Entry 26 (RTE26)—Offset 44h

This register has the same bit definition as RTE0.

27.1.30 Redirection Table Entry 27 (RTE27)—Offset 46h

This register has the same bit definition as RTE0.

27.1.31 Redirection Table Entry 28 (RTE28)—Offset 48h

This register has the same bit definition as RTE0.

27.1.32 Redirection Table Entry 29 (RTE29)—Offset 4Ah

This register has the same bit definition as RTE0.

27.1.33 Redirection Table Entry 30 (RTE30)—Offset 4Ch

This register has the same bit definition as RTE0.

27.1.34 Redirection Table Entry 31 (RTE31)—Offset 4Eh

This register has the same bit definition as RTE0.

27.1.35 Redirection Table Entry 32 (RTE32)—Offset 50h

This register has the same bit definition as RTE0.

27.1.36 Redirection Table Entry 33 (RTE33)—Offset 52h

This register has the same bit definition as RTE0.

27.1.37 Redirection Table Entry 34 (RTE34)—Offset 54h

This register has the same bit definition as RTE0.

27.1.38 Redirection Table Entry 35 (RTE35)—Offset 56h

This register has the same bit definition as RTE0.

27.1.39 Redirection Table Entry 36 (RTE36)—Offset 58h

This register has the same bit definition as RTE0.

27.1.40 Redirection Table Entry 37 (RTE37)—Offset 5Ah

This register has the same bit definition as RTE0.

27.1.41 Redirection Table Entry 38 (RTE38)—Offset 5Ch

This register has the same bit definition as RTE0.

27.1.42 Redirection Table Entry 39 (RTE39)—Offset 5Eh

This register has the same bit definition as RTE0.

27.1.43 Redirection Table Entry 40 (RTE40)—Offset 60h

This register has the same bit definition as RTE0.

27.1.44 Redirection Table Entry 41 (RTE41)—Offset 62h

This register has the same bit definition as RTE0.

27.1.45 Redirection Table Entry 42 (RTE42)—Offset 64h

This register has the same bit definition as RTE0.

27.1.46 Redirection Table Entry 43 (RTE43)—Offset 66h

This register has the same bit definition as RTE0.

27.1.47 Redirection Table Entry 44 (RTE44)—Offset 68h

This register has the same bit definition as RTE0.

27.1.48 Redirection Table Entry 45 (RTE45)—Offset 6Ah

This register has the same bit definition as RTE0.

27.1.49 Redirection Table Entry 46 (RTE46)—Offset 6Ch

This register has the same bit definition as RTE0.

27.1.50 Redirection Table Entry 47 (RTE47)—Offset 6Eh

This register has the same bit definition as RTE0.

27.1.51 Redirection Table Entry 48 (RTE48)—Offset 70h

This register has the same bit definition as RTE0.

27.1.52 Redirection Table Entry 49 (RTE49)—Offset 72h

This register has the same bit definition as RTE0.

27.1.53 Redirection Table Entry 50 (RTE50)—Offset 74h

This register has the same bit definition as RTE0.

27.1.54 Redirection Table Entry 51 (RTE51)—Offset 76h

This register has the same bit definition as RTE0.

27.1.55 Redirection Table Entry 52 (RTE52)—Offset 78h

This register has the same bit definition as RTE0.

27.1.56 Redirection Table Entry 53 (RTE53)—Offset 7Ah

This register has the same bit definition as RTE0.

27.1.57 Redirection Table Entry 54 (RTE54)—Offset 7Ch

This register has the same bit definition as RTE0.

27.1.58 Redirection Table Entry 55 (RTE55)—Offset 7Eh

This register has the same bit definition as RTE0.

27.1.59 Redirection Table Entry 56 (RTE56)—Offset 80h

This register has the same bit definition as RTE0.

27.1.60 Redirection Table Entry 57 (RTE57)—Offset 82h

This register has the same bit definition as RTE0.

27.1.61 Redirection Table Entry 58 (RTE58)—Offset 84h

This register has the same bit definition as RTE0.

27.1.62 Redirection Table Entry 59 (RTE59)—Offset 86h

This register has the same bit definition as RTE0.

27.1.63 Redirection Table Entry 60 (RTE60)—Offset 88h

This register has the same bit definition as RTE0.

27.1.64 Redirection Table Entry 61 (RTE61)—Offset 8Ah

This register has the same bit definition as RTE0.

27.1.65 Redirection Table Entry 62 (RTE62)—Offset 8Ch

This register has the same bit definition as RTE0.

27.1.66 Redirection Table Entry 63 (RTE63)—Offset 8Eh

This register has the same bit definition as RTE0.

27.1.67 Redirection Table Entry 64 (RTE64)—Offset 90h

This register has the same bit definition as RTE0.

27.1.68 Redirection Table Entry 65 (RTE65)—Offset 92h

This register has the same bit definition as RTE0.

27.1.69 Redirection Table Entry 66 (RTE66)—Offset 94h

This register has the same bit definition as RTE0.

27.1.70 Redirection Table Entry 67 (RTE67)—Offset 96h

This register has the same bit definition as RTE0.

27.1.71 Redirection Table Entry 68 (RTE68)—Offset 98h

This register has the same bit definition as RTE0.

27.1.72 Redirection Table Entry 69 (RTE69)—Offset 9Ah

This register has the same bit definition as RTE0.

27.1.73 Redirection Table Entry 70 (RTE70)—Offset 9Ch

This register has the same bit definition as RTE0.

27.1.74 Redirection Table Entry 71 (RTE71)—Offset 9Eh

This register has the same bit definition as RTE0.

27.1.75 Redirection Table Entry 72 (RTE72)—Offset A0h

This register has the same bit definition as RTE0.

27.1.76 Redirection Table Entry 73 (RTE73)—Offset A2h

This register has the same bit definition as RTE0.

27.1.77 Redirection Table Entry 74 (RTE74)—Offset A4h

This register has the same bit definition as RTE0.

27.1.78 Redirection Table Entry 75 (RTE75)—Offset A6h

This register has the same bit definition as RTE0.

27.1.79 Redirection Table Entry 76 (RTE76)—Offset A8h

This register has the same bit definition as RTE0.

27.1.80 Redirection Table Entry 77 (RTE77)—Offset AAh

This register has the same bit definition as RTE0.

27.1.81 Redirection Table Entry 78 (RTE78)—Offset ACh

This register has the same bit definition as RTE0.

27.1.82 Redirection Table Entry 79 (RTE79)—Offset AEh

This register has the same bit definition as RTE0.

27.1.83 Redirection Table Entry 80 (RTE80)—Offset B0h

This register has the same bit definition as RTE0.

27.1.84 Redirection Table Entry 81 (RTE81)—Offset B2h

This register has the same bit definition as RTE0.

27.1.85 Redirection Table Entry 82 (RTE82)—Offset B4h

This register has the same bit definition as RTE0.

27.1.86 Redirection Table Entry 83 (RTE83)—Offset B6h

This register has the same bit definition as RTE0.

27.1.87 Redirection Table Entry 84 (RTE84)—Offset B8h

This register has the same bit definition as RTE0.

27.1.88 Redirection Table Entry 85 (RTE85)—Offset BAh

This register has the same bit definition as RTE0.

27.1.89 Redirection Table Entry 86 (RTE86)—Offset BCh

This register has the same bit definition as RTE0.

27.1.90 Redirection Table Entry 87 (RTE87)—Offset BEh

This register has the same bit definition as RTE0.

27.1.91 Redirection Table Entry 88 (RTE88)—Offset C0h

This register has the same bit definition as RTE0.

27.1.92 Redirection Table Entry 89 (RTE89)—Offset C2h

This register has the same bit definition as RTE0.

27.1.93 Redirection Table Entry 90 (RTE90)—Offset C4h

This register has the same bit definition as RTE0.

27.1.94 Redirection Table Entry 91 (RTE91)—Offset C6h

This register has the same bit definition as RTE0.

27.1.95 Redirection Table Entry 92 (RTE92)—Offset C8h

This register has the same bit definition as RTE0.

27.1.96 Redirection Table Entry 93 (RTE93)—Offset CAh

This register has the same bit definition as RTE0.

27.1.97 Redirection Table Entry 94 (RTE94)—Offset CCh

This register has the same bit definition as RTE0.

27.1.98 Redirection Table Entry 95 (RTE95)—Offset CEh

This register has the same bit definition as RTE0.

27.1.99 Redirection Table Entry 96 (RTE96)—Offset D0h

This register has the same bit definition as RTE0.

27.1.100 Redirection Table Entry 97 (RTE97)—Offset D2h

This register has the same bit definition as RTE0.

27.1.101 Redirection Table Entry 98 (RTE98)—Offset D4h

This register has the same bit definition as RTE0.

27.1.102 Redirection Table Entry 99 (RTE99)—Offset D6h

This register has the same bit definition as RTE0.

27.1.103 Redirection Table Entry 100 (RTE100)—Offset D8h

This register has the same bit definition as RTE0.

27.1.104 Redirection Table Entry 101 (RTE101)—Offset DAh

This register has the same bit definition as RTE0.

27.1.105 Redirection Table Entry 102 (RTE102)—Offset DCh

This register has the same bit definition as RTE0.

27.1.106 Redirection Table Entry 103 (RTE103)—Offset DEh

This register has the same bit definition as RTE0.

27.1.107 Redirection Table Entry 104 (RTE104)—Offset E0h

This register has the same bit definition as RTE0.

27.1.108 Redirection Table Entry 105 (RTE105)—Offset E2h

This register has the same bit definition as RTE0.

27.1.109 Redirection Table Entry 106 (RTE106)—Offset E4h

This register has the same bit definition as RTE0.

27.1.110 Redirection Table Entry 107 (RTE107)—Offset E6h

This register has the same bit definition as RTE0.

27.1.111 Redirection Table Entry 108 (RTE108)—Offset E8h

This register has the same bit definition as RTE0.

27.1.112 Redirection Table Entry 109 (RTE109)—Offset EAh

This register has the same bit definition as RTE0.

27.1.113 Redirection Table Entry 110 (RTE110)—Offset ECh

This register has the same bit definition as RTE0.

27.1.114 Redirection Table Entry 111 (RTE111)—Offset EEh

This register has the same bit definition as RTE0.

27.1.115 Redirection Table Entry 112 (RTE112)—Offset F0h

This register has the same bit definition as RTE0.

27.1.116 Redirection Table Entry 113 (RTE113)—Offset F2h

This register has the same bit definition as RTE0.

27.1.117 Redirection Table Entry 114 (RTE114)—Offset F4h

This register has the same bit definition as RTE0.

27.1.118 Redirection Table Entry 115 (RTE115)—Offset F6h

This register has the same bit definition as RTE0.

27.1.119 Redirection Table Entry 116 (RTE116)—Offset F8h

This register has the same bit definition as RTE0.

27.1.120 Redirection Table Entry 117 (RTE117)—Offset FAh

This register has the same bit definition as RTE0.

27.1.121 Redirection Table Entry 118 (RTE118)—Offset FCh

This register has the same bit definition as RTE0.

27.1.122 Redirection Table Entry 119 (RTE119)—Offset FEh

This register has the same bit definition as RTE0.

27.2 Advanced Programmable Interrupt Controller (APIC) Registers Summary

The APIC is accessed using an indirect addressing scheme. Two registers are visible by software for manipulation of most of the APIC registers. These registers are mapped into memory space. The address bits 19:12 of the address range are programmable through bits 7:0 of OIC register (Chipset Configuration Register: Offset 31FEh). The registers are shown below.

Table 27-2. Summary of Advanced Programmable Interrupt Controller (APIC) Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	Index Register (IDX)—Offset 0h	0h
10h	13h	Data Register (DAT)—Offset 10h	0h
40h	43h	EOI Register (EOIR)—Offset 40h	0h

27.2.1 Index Register (IDX)—Offset 0h

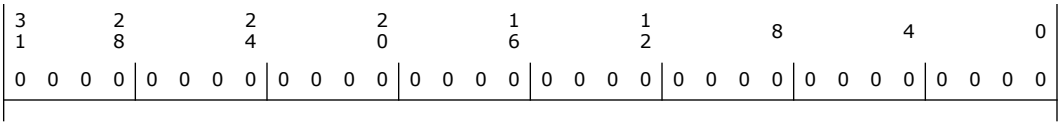
The Index Register will select which APIC indirect register to be manipulated by software. Software will program this register to select the desired APIC internal register.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**APIC Index :** This is an 8 bit pointer into the I/O APIC register table.

27.2.2 Data Register (DAT)—Offset 10h

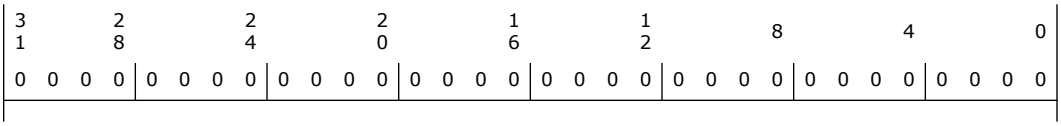
This 32-bit register specifies the data to be read or written to the register pointed to by the Index register. This register can be accessed only in DW quantities.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**APIC Data:** This is a 32-bit register for the data to be read or written to the APIC indirect register pointed to by the Index register (Memory Address FEC0_0000h).

27.2.3 EOI Register (EOIR)—Offset 40h

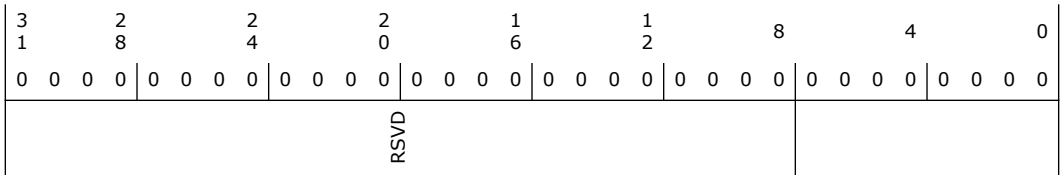
When a write is issued to this register, the IOxAPIC will check the lower 8 bits written to this register, and compare it with the vector field for each entry in the I/O Redirection Table. When a match is found, RTE.RIRR for that entry will be cleared. If multiple entries have the same vector, each of those entries will have RTE.RIRR cleared. Only bits 7:0 are used. Bits 31:8 are ignored.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	0h WO	**Redirection Entry Clear:** When a write is issued to this register, the I/O APIC will check this field and compare it with the vector field for each entry in the I/O Redirection Table. When a match is found, the Remote_IRR bit for that I/O Redirection Entry will be cleared.

§ §

28 Processor Interface

28.1 Processor Interface Memory Registers Summary

Table 28-1. Summary of Processor Interface Memory Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
61h	61h	NMI Status and Control (NMI_STS_CNT)—Offset 61h	0h
70h	70h	NMI Enable (and Real Time Clock Index) (NMI_EN)—Offset 70h	80h
92h	92h	Init Register (PORT92)—Offset 92h	0h
CF9h	CF9h	Reset Control Register (RST_CNT)—Offset CF9h	0h

28.1.1 NMI Status and Control (NMI_STS_CNT)—Offset 61h

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

7			4				0
0	0	0	0	0	0	0	0
SERR_NMI_STS	IOCHK_NMI_STS	TMR2_OUT_STS	RSVD	IOCHK_NMI_EN	PCI_SERR_EN	SPKR_DAT_EN	TIM_CNT2_EN

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**SERR# NMI Source Status (SERR_NMI_STS):** This bit is set by any of the sources of the internal SERR on the PCH backbone, this includes SERR assertions forwarded from the secondary PCI bus, error from a PCIe port, Do_SERR or standard PCIe error message from DMI, or internal Bus 0 functions that generate SERR#. Bit 2 must be cleared in this register in order for this bit to be set. This interrupt source is enabled by setting bit 2 to 0. To reset the interrupt, set bit 2 to 1 and then set it to 0. This bit is read-only. When writing to port 61h, this bit must be 0.
6	0h RO	**IOCHK# NMI Source Status (IOCHK_NMI_STS):** This bit is set if an ISA agent (via SERIRQ) asserts IOCHK# and bit 3 is cleared in this register. This interrupt source is enabled by setting bit 3 to 0. To reset the interrupt, set bit 3 to 1 and then set it to 0. This bit is read-only. When writing to port 61h, this bit must be a 0.
5	0h RO	**Timer Counter 2 OUT Status (TMR2_OUT_STS):** This bit reflects the current state of the 8254 counter 2 output. Counter 2 must be programmed following any PCI reset for this bit to have a determinate value. When writing to port 61h, this bit must be a 0.
4	0h RO	Reserved.
3	0h RW	**IOCHK# NMI Enable (IOCHK_NMI_EN):** When this bit is a 1, IOCHK# NMIs are disabled and cleared. When this bit is a 0, IOCHK# NMIs are enabled.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**PCI SERR# Enable (PCI_SERR_EN):** When this bit is a 1, the SERR# NMIs are disabled and cleared. When this bit is a 0, SERR# NMIs are enabled.
1	0h RW	**Speaker Data Enable (SPKR_DAT_EN):** When this bit is a 0, the SPKR output is a 0. When this bit is a 1, the SPKR output is equivalent to the Counter 2 OUT signal value.
0	0h RW	**Timer Counter 2 Enable (TIM_CNT2_EN):** When this bit is a 0, Counter 2 counting is disabled. Counting is enabled when this bit is 1.

28.1.2 NMI Enable (and Real Time Clock Index) (NMI_EN)—Offset 70h

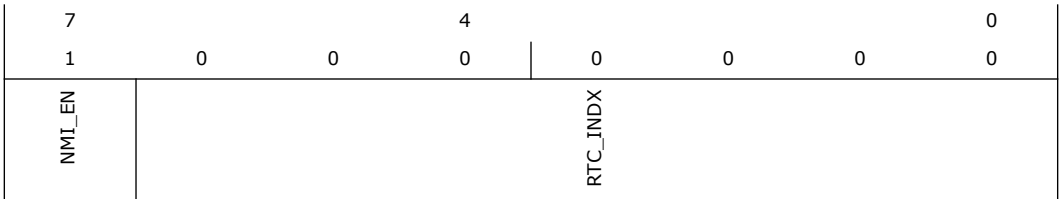
This register is write-only for normal operation. In Alt-Access mode, this register can be read to find the NMI Enable status and the RTC index value. *WO for normal operation, RW if Alternate access mode is enabled. Use RW because there is no equivalent register access attribute in RDL

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 80h



Bit Range	Default & Access	Field Name (ID): Description
7	1h RW	**NMI_EN# (NMI_EN):** When this bit is a 1, all NMI sources are disabled. When this bit is a 0, NMI sources are enabled.
6:0	0h RW	**Real Time Clock Index (Address) (RTC_INDX):** This data goes to the RTC to select which register or CMOS RAM address is being accessed.

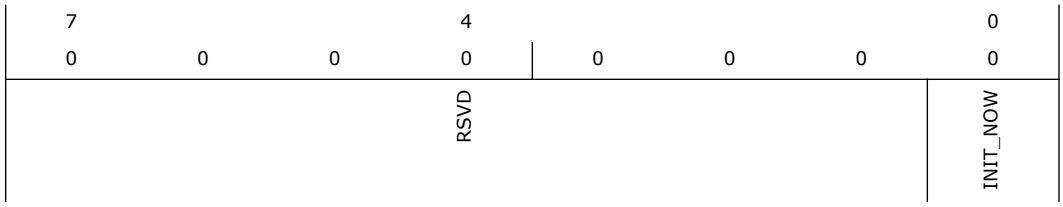
28.1.3 Init Register (PORT92)—Offset 92h

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7:1	0h RO	Reserved.
0	0h RW	**INIT_NOW (INIT_NOW):** When this bit transitions from a 0 to a 1, the PCH will force INIT# active for 16 PCI clocks.

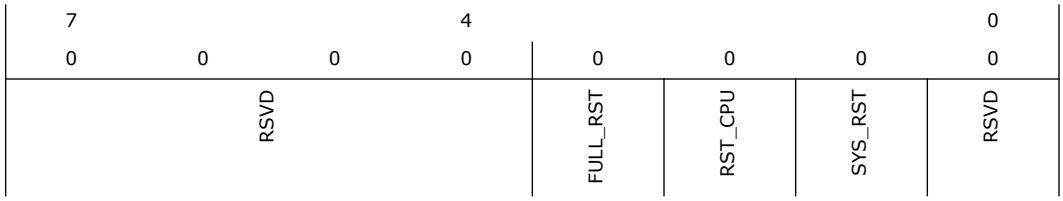
28.1.4 Reset Control Register (RST_CNT)—Offset CF9h

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7:4	0h RO	Reserved.
3	0h RW	**Full Reset (FULL_RST):** When this bit is set to 1 and bit 1 is set to 1 (indicating Hard Reset, not Soft Reset), and the RST_CPU bit (bit 2) is written from 0 to 1, the PCH will do a full reset, including driving SLP_S3#, SLP_S4# and SLP_S5# active (low) for at least 3 (and no more than 5) seconds. When this bit is set, it also causes the full power cycle (SLP_S3/4/5# assertion) in response to SYSRESET#, PWROK#, and Watchdog timer reset sources.
2	0h RW	**Reset CPU (RST_CPU):** This bit will cause either a hard or soft reset to the CPU depending on the state of the SYS_RST bit (bit 1 in this same register). The software will cause the reset by setting bit 2 from a 0 to a 1.
1	0h RW	**System Reset (SYS_RST):** Ths bit determines the type of reset caused via RST_CPU (bit 2 of this register). If SYS_RST is 0 when RST_CPU goes from 0 to 1, then the PCH will force INIT# active for 16 PCI clocks. If SYS_RST is 1 when RST_CPU goes from 0 to 1, then the PCH will force PCI reset active for about 1 ms, however the SLP_S3#, SLP_S4# and SLP_S5# signals assertion is dependent on the value of the FULL_RST (bit3 of this register).
0	0h RO	Reserved.

§ §

29 General Purpose I/O (GPIO)

29.1 GPIO Community 0 Registers Summary

Community 0 Registers are for GPP_A and GPP_B groups.

These registers are within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID + Register Offset).

Table 29-1. Summary of GPIO Community 0 Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
8h	Bh	Family Base Address (FAMBAR)—Offset 8h	300h
Ch	Fh	Pad Base Address (PADBAR)—Offset Ch	400h
10h	13h	Miscellaneous Configuration (MISCCFG)—Offset 10h	43200h
20h	23h	Pad Ownership (PAD_OWN_GPP_A_0)—Offset 20h	0h
24h	27h	Pad Ownership (PAD_OWN_GPP_A_1)—Offset 24h	0h
28h	2Bh	Pad Ownership (PAD_OWN_GPP_A_2)—Offset 28h	0h
30h	33h	Pad Ownership (PAD_OWN_GPP_B_0)—Offset 30h	0h
34h	37h	Pad Ownership (PAD_OWN_GPP_B_1)—Offset 34h	0h
38h	3Bh	Pad Ownership (PAD_OWN_GPP_B_2)—Offset 38h	0h
A0h	A3h	Pad Configuration Lock (PADCFGLOCK_GPP_A)—Offset A0h	0h
A4h	A7h	Pad Configuration Lock (PADCFGLOCKTX_GPP_A)—Offset A4h	0h
A8h	ABh	Pad Configuration Lock (PADCFGLOCK_GPP_B)—Offset A8h	0h
ACh	AFh	Pad Configuration Lock (PADCFGLOCKTX_GPP_B)—Offset ACh	0h
D0h	D3h	Host Software Pad Ownership (HOSTSW_OWN_GPP_A)—Offset D0h	0h
D4h	D7h	Host Software Pad Ownership (HOSTSW_OWN_GPP_B)—Offset D4h	0h
100h	103h	GPI Interrupt Status (GPI_IS_GPP_A)—Offset 100h	0h
104h	107h	GPI Interrupt Status (GPI_IS_GPP_B)—Offset 104h	0h
120h	123h	GPI Interrupt Enable (GPI_IE_GPP_A)—Offset 120h	0h
124h	127h	GPI Interrupt Enable (GPI_IE_GPP_B)—Offset 124h	0h
140h	143h	GPI General Purpose Events Status (GPI_GPE_STS_GPP_A)—Offset 140h	0h
144h	147h	GPI General Purpose Events Status (GPI_GPE_STS_GPP_B)—Offset 144h	0h
160h	163h	GPI General Purpose Events Enable (GPI_GPE_EN_GPP_A)—Offset 160h	0h
164h	167h	GPI General Purpose Events Enable (GPI_GPE_EN_GPP_B)—Offset 164h	0h
184h	187h	SMI Status (GPI_SMI_STS_GPP_B)—Offset 184h	0h
1A4h	1A7h	SMI Enable (GPI_SMI_EN_GPP_B)—Offset 1A4h	0h
1C4h	1C7h	NMI Status (GPI_NMI_STS_GPP_B)—Offset 1C4h	0h
1E4h	1E7h	NMI Enable (GPI_NMI_EN_GPP_B)—Offset 1E4h	0h
400h	403h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_0)—Offset 400h	44000X00h See register for X value

Table 29-1. Summary of GPIO Community 0 Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
404h	407h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_0)—Offset 404h	18h
408h	40Bh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_1)—Offset 408h	44000X00h See register for X value
40Ch	40Fh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_1)—Offset 40Ch	See Register
410h	413h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_2)—Offset 410h	44000X00h See register for X value
414h	417h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_2)—Offset 414h	See Register
418h	41Bh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_3)—Offset 418h	44000X00h See register for X value
41Ch	41Fh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_3)—Offset 41Ch	See Register
420h	423h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_4)—Offset 420h	44000X00h See register for X value
424h	427h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_4)—Offset 424h	See Register
428h	42Bh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_5)—Offset 428h	44000X00h See register for X value
42Ch	42Fh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_5)—Offset 42Ch	See Register
430h	433h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_6)—Offset 430h	44000X00h See register for X value
434h	437h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_6)—Offset 434h	See Register
438h	43Bh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_7)—Offset 438h	44000X00h See register for X value
43Ch	43Fh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_7)—Offset 43Ch	See Register
440h	443h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_8)—Offset 440h	44000X00h See register for X value
444h	447h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_8)—Offset 444h	See Register
448h	44Bh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_9)—Offset 448h	44000X00h See register for X value
44Ch	44Fh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_9)—Offset 44Ch	See Register
450h	453h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_10)—Offset 450h	44000X00h See register for X value
454h	457h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_10)—Offset 454h	See Register
458h	45Bh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_11)—Offset 458h	44000X00h See register for X value

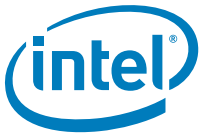


Table 29-1. Summary of GPIO Community 0 Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
45Ch	45Fh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_11)—Offset 45Ch	See Register
460h	463h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_12)—Offset 460h	44000X00h See register for X value
464h	467h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_12)—Offset 464h	See Register
468h	46Bh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_13)—Offset 468h	44000X00h See register for X value
46Ch	46Fh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_13)—Offset 46Ch	See Register
470h	473h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_14)—Offset 470h	44000X00h See register for X value
474h	477h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_14)—Offset 474h	See Register
478h	47Bh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_15)—Offset 478h	44000X00h See register for X value
47Ch	47Fh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_15)—Offset 47Ch	See Register
480h	483h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_16)—Offset 480h	44000X00h See register for X value
484h	487h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_16)—Offset 484h	See Register
488h	48Bh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_17)—Offset 488h	44000X00h See register for X value
48Ch	48Fh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_17)—Offset 48Ch	See Register
490h	493h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_18)—Offset 490h	44000X00h See register for X value
494h	497h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_18)—Offset 494h	See Register
498h	49Bh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_19)—Offset 498h	44000X00h See register for X value
49Ch	49Fh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_19)—Offset 49Ch	See Register
4A0h	4A3h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_20)—Offset 4A0h	44000X00h See register for X value
4A4h	4A7h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_20)—Offset 4A4h	See Register
4A8h	4ABh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_21)—Offset 4A8h	44000X00h See register for X value
4ACh	4AFh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_21)—Offset 4ACh	See Register

Table 29-1. Summary of GPIO Community 0 Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
4B0h	4B3h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_22)—Offset 4B0h	44000X00h See register for X value
4B4h	4B7h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_22)—Offset 4B4h	See Register
4B8h	4BBh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_23)—Offset 4B8h	44000X00h See register for X value
4BCh	4BFh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_23)—Offset 4BCh	See Register
4C0h	4C3h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_0)—Offset 4C0h	44000X00h See register for X value
4C4h	4C7h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_0)—Offset 4C4h	See Register
4C8h	4CBh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_1)—Offset 4C8h	44000X00h See register for X value
4CCh	4CFh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_1)—Offset 4CCh	See Register
4D0h	4D3h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_2)—Offset 4D0h	44000X00h See register for X value
4D4h	4D7h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_2)—Offset 4D4h	See Register
4D8h	4DBh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_3)—Offset 4D8h	44000X00h See register for X value
4DCh	4DFh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_3)—Offset 4DCh	See Register
4E0h	4E3h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_4)—Offset 4E0h	44000X00h See register for X value
4E4h	4E7h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_4)—Offset 4E4h	See Register
4E8h	4EBh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_5)—Offset 4E8h	44000X00h See register for X value
4ECh	4EFh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_5)—Offset 4ECh	See Register
4F0h	4F3h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_6)—Offset 4F0h	44000X00h See register for X value
4F4h	4F7h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_6)—Offset 4F4h	See Register
4F8h	4FBh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_7)—Offset 4F8h	44000X00h See register for X value
4FCh	4FFh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_7)—Offset 4FCh	See Register
500h	503h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_8)—Offset 500h	44000X00h See register for X value

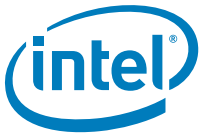


Table 29-1. Summary of GPIO Community 0 Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
504h	507h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_8)—Offset 504h	See Register
508h	50Bh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_9)—Offset 508h	44000X00h See register for X value
50Ch	50Fh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_9)—Offset 50Ch	See Register
510h	513h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_10)—Offset 510h	44000X00h See register for X value
514h	517h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_10)—Offset 514h	See Register
518h	51Bh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_11)—Offset 518h	44000X00h See register for X value
51Ch	51Fh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_11)—Offset 51Ch	See Register
520h	523h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_12)—Offset 520h	44000X00h See register for X value
524h	527h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_12)—Offset 524h	See Register
528h	52Bh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_13)—Offset 528h	44000X00h See register for X value
52Ch	52Fh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_13)—Offset 52Ch	See Register
530h	533h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_14)—Offset 530h	44000X00h See register for X value
534h	537h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_14)—Offset 534h	See Register
538h	53Bh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_15)—Offset 538h	44000X00h See register for X value
53Ch	53Fh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_15)—Offset 53Ch	See Register
540h	543h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_16)—Offset 540h	44000X00h See register for X value
544h	547h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_16)—Offset 544h	See Register
548h	54Bh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_17)—Offset 548h	44000X00h See register for X value
54Ch	54Fh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_17)—Offset 54Ch	See Register
550h	553h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_18)—Offset 550h	44000X00h See register for X value
554h	557h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_18)—Offset 554h	See Register

Table 29-1. Summary of GPIO Community 0 Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
558h	55Bh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_19)—Offset 558h	44000X00h See register for X value
55Ch	55Fh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_19)—Offset 55Ch	See Register
560h	563h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_20)—Offset 560h	44000X00h See register for X value
564h	567h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_20)—Offset 564h	See Register
568h	56Bh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_21)—Offset 568h	44000X00h See register for X value
56Ch	56Fh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_21)—Offset 56Ch	See Register
570h	573h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_22)—Offset 570h	44000X00h See register for X value
574h	577h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_22)—Offset 574h	See Register
578h	57Bh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_23)—Offset 578h	44000X00h See register for X value
57Ch	57Fh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_23)—Offset 57Ch	See Register

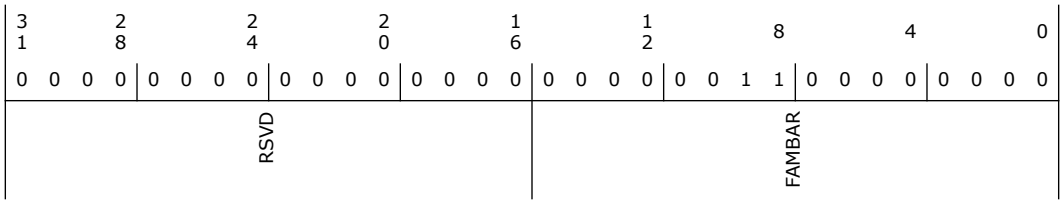
29.1.1 Family Base Address (FAMBAR)—Offset 8h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 300h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	300h RO	**Family Base Address (FAMBAR):** This field provides the starting byte-align address of Family0 register sets. It is meant for software to discover from where the very first Family register (i.e. Family0 register) starts to compute the next Families address offsets.

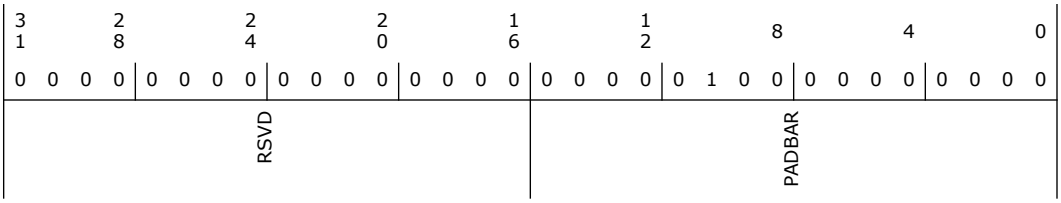
29.1.2 Pad Base Address (PADBAR)—Offset Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 400h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	400h RO	**Pad Base Address (PADBAR):** This field provides the starting byte-align address of Pad0 register sets. It is meant for software to discover from where the very first Pad register (i.e. Pad0 register) starts to compute the next Pad address offsets.

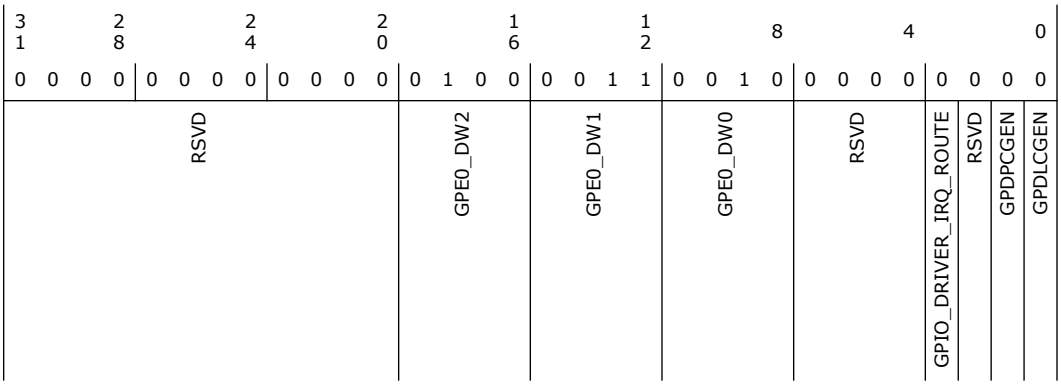
29.1.3 Miscellaneous Configuration (MISCCFG)—Offset 10h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 43200h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	Reserved.
19:16	4h RW	**GPIO Group to GPE_DW0 assignment encoding (GPE0_DW2):** This register assigns a specific GPIO Group to the ACPI GPE0[95:64]. The selected GPIO group will be mapped to lower bits of the GPE register 0h = GPP_A[23:0] mapped to GPE[87:64]; GPE[95:88] not used. 1h = GPP_B[23:0] mapped to GPE[87:64]; GPE[95:88] not used. 2h = GPP_C[23:0] mapped to GPE[87:64]; GPE[95:88] not used. 3h = GPP_D[23:0] mapped to GPE[87:64]; GPE[95:88] not used. 4h = GPP_E[23:0] mapped to GPE[87:64]; GPE[95:88] not used. 5h = GPP_F[23:0] mapped to GPE[87:64]; GPE[95:88] not used. 6h = GPP_G[7:0] mapped to GPE[51:64]; GPE[95:52] not used. 7h = GPD[11:0] mapped to GPE[75:64]; GPE[95:76] not used.
15:12	3h RW	**GPIO Group to GPE_DW0 assignment encoding (GPE0_DW1):** This register assigns a specific GPIO Group to the ACPI GPE0[63:32]. The selected GPIO group will be mapped to lower bits of the GPE register 0h = GPP_A[23:0] mapped to GPE[55:32]; GPE[63:56] not used. 1h = GPP_B[23:0] mapped to GPE[55:32]; GPE[63:56] not used. 2h = GPP_C[23:0] mapped to GPE[55:32]; GPE[63:56] not used. 3h = GPP_D[23:0] mapped to GPE[55:32]; GPE[63:56] not used. 4h = GPP_E[23:0] mapped to GPE[55:32]; GPE[63:56] not used. 5h = GPP_F[23:0] mapped to GPE[55:32]; GPE[63:56] not used. 6h = GPP_G[7:0] mapped to GPE[39:32]; GPE[63:40] not used. 7h = GPD[11:0] mapped to GPE[43:32]; GPE[63:44] not used.
11:8	2h RW	**GPIO Group to GPE_DW0 assignment encoding (GPE0_DW0):** This register assigns a specific GPIO Group to the ACPI GPE0[31:0]. The selected GPIO group will be mapped to lower bits of the GPE register 0h = GPP_A[23:0] mapped to GPE[23:0]; GPE[31:24] not used. 1h = GPP_B[23:0] mapped to GPE[23:0]; GPE[31:24] not used. 2h = GPP_C[23:0] mapped to GPE[23:0]; GPE[31:24] not used. 3h = GPP_D[23:0] mapped to GPE[23:0]; GPE[31:24] not used. 4h = GPP_E[23:0] mapped to GPE[23:0]; GPE[31:24] not used. 5h = GPP_F[23:0] mapped to GPE[23:0]; GPE[31:24] not used. 6h = GPP_G[7:0] mapped to GPE[7:0]; GPE[31:8] not used. 7h = GPD[11:0] mapped to GPE[11:0]; GPE[31:12] not used.
7:4	0h RO	Reserved.
3	0h RW	**GPIO Driver IRQ Route (GPIO_DRIVER_IRQ_ROUTE):** Specifies the APIC IRQ globally for all pads within the current community (GPI_IS with corresponding GPI_IE enable). 0 = IRQ14 1 = IRQ15
2	0h RO	Reserved.
1	0h RW	**GPIO Dynamic Partition Clock Gating Enable (GPDPCGEN):** Specifies whether the GPIO Community should take part in partition clock gating 0 = Disable participation in dynamic partition clock gating 1 = Enable participation in dynamic partition clock gating
0	0h RW	**GPIO Dynamic Local Clock Gating Enable (GPDLCGEN):** Specifies whether the GPIO Community should perform local clock gating. 0 = Disable dynamic local clock gating 1 = Enable dynamic local clock gating

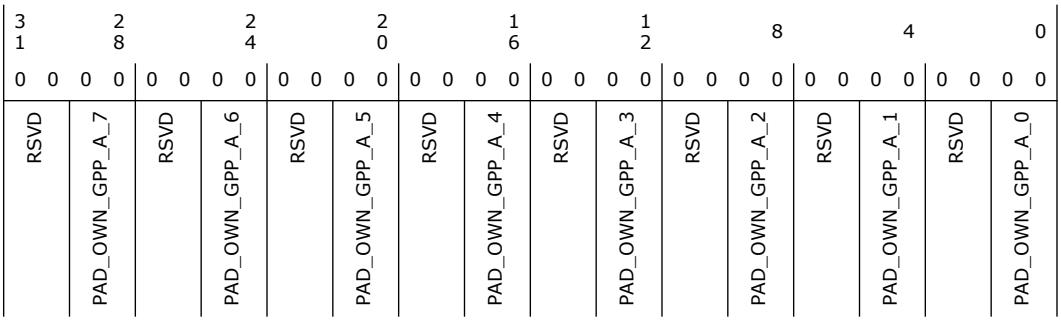
29.1.4 Pad Ownership (PAD_OWN_GPP_A_0)—Offset 20h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29:28	0h RO	**Pad Ownership (PAD_OWN_GPP_A_7):** Same description as bits [1:0], except that the bit field applies to GPP_A7.
27:26	0h RO	Reserved.
25:24	0h RO	**Pad Ownership (PAD_OWN_GPP_A_6):** Same description as bits [1:0], except that the bit field applies to GPP_A6.
23:22	0h RO	Reserved.
21:20	0h RO	**Pad Ownership (PAD_OWN_GPP_A_5):** Same description as bits [1:0], except that the bit field applies to GPP_A5.
19:18	0h RO	Reserved.
17:16	0h RO	**Pad Ownership (PAD_OWN_GPP_A_4):** Same description as bits [1:0], except that the bit field applies to GPP_A4.
15:14	0h RO	Reserved.
13:12	0h RO	**Pad Ownership (PAD_OWN_GPP_A_3):** Same description as bits [1:0], except that the bit field applies to GPP_A3.
11:10	0h RO	Reserved.
9:8	0h RO	**Pad Ownership (PAD_OWN_GPP_A_2):** Same description as bits [1:0], except that the bit field applies to GPP_A2.
7:6	0h RO	Reserved.
5:4	0h RO	**Pad Ownership (PAD_OWN_GPP_A_1):** Same description as bits [1:0], except that the bit field applies to GPP_A1.
3:2	0h RO	Reserved.
1:0	0h RO	**Pad Ownership (PAD_OWN_GPP_A_0):** 00 = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. 01 = ME GPIO Mode. ME has ownership of the pad. 10 = ISH GPIO Mode.ME has ownership of the pad 11 = Reserved

29.1.5 Pad Ownership (PAD_OWN_GPP_A_1)—Offset 24h

Same description as PAD_OWN_GPP_A_0, except that this register is for GPP_A[15:8]

29.1.6 Pad Ownership (PAD_OWN_GPP_A_2)—Offset 28h

Same description as PAD_OWN_GPP_A_0, except that this register is for GPP_A[23:16]

29.1.7 Pad Ownership (PAD_OWN_GPP_B_0)—Offset 30h

Same description as PAD_OWN_GPP_A_0, except that this register is for GPP_B[7:0]

29.1.8 Pad Ownership (PAD_OWN_GPP_B_1)—Offset 34h

Same description as PAD_OWN_GPP_A_0, except that this register is for GPP_B[15:8]

29.1.9 Pad Ownership (PAD_OWN_GPP_B_2)—Offset 38h

Same description as PAD_OWN_GPP_A_0, except that this register is for GPP_B[23:16]

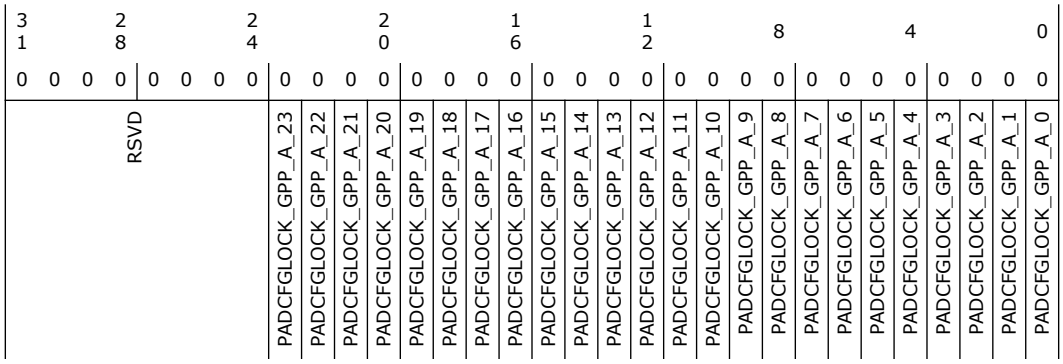
29.1.10 Pad Configuration Lock (PADCFGLOCK_GPP_A)—Offset A0h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_A_23):** Applied to GPP_A23. Same description as PADCFGLOCK_GPP_A_0
22	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_A_22):** Applied to GPP_A22. Same description as PADCFGLOCK_GPP_A_0

Bit Range	Default & Access	Field Name (ID): Description
21	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_A_21):** Applied to GPP_A21. Same description as PADCFGLOCK_GPP_A_0
20	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_A_20):** Applied to GPP_A20. Same description as PADCFGLOCK_GPP_A_0
19	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_A_19):** Applied to GPP_A19. Same description as PADCFGLOCK_GPP_A_0
18	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_A_18):** Applied to GPP_A18. Same description as PADCFGLOCK_GPP_A_0
17	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_A_17):** Applied to GPP_A17. Same description as PADCFGLOCK_GPP_A_0
16	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_A_16):** Applied to GPP_A16. Same description as PADCFGLOCK_GPP_A_0
15	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_A_15):** Applied to GPP_A15. Same description as PADCFGLOCK_GPP_A_0
14	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_A_14):** Applied to GPP_A14. Same description as PADCFGLOCK_GPP_A_0
13	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_A_13):** Applied to GPP_A13. Same description as PADCFGLOCK_GPP_A_0
12	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_A_12):** Applied to GPP_A12. Same description as PADCFGLOCK_GPP_A_0
11	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_A_11):** Applied to GPP_A11. Same description as PADCFGLOCK_GPP_A_0
10	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_A_10):** Applied to GPP_A10. Same description as PADCFGLOCK_GPP_A_0
9	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_A_9):** Applied to GPP_A9. Same description as PADCFGLOCK_GPP_A_0
8	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_A_8):** Applied to GPP_A8. Same description as PADCFGLOCK_GPP_A_0
7	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_A_7):** Applied to GPP_A7. Same description as PADCFGLOCK_GPP_A_0
6	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_A_6):** Applied to GPP_A6. Same description as PADCFGLOCK_GPP_A_0
5	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_A_5):** Applied to GPP_A5. Same description as PADCFGLOCK_GPP_A_0
4	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_A_4):** Applied to GPP_A4. Same description as PADCFGLOCK_GPP_A_0
3	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_A_3):** Applied to GPP_A3. Same description as PADCFGLOCK_GPP_A_0

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_A_2):** Applied to GPP_A2. Same description as PADCFGLOCK_GPP_A_0
1	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_A_1):** Applied to GPP_A1. Same description as PADCFGLOCK_GPP_A_0
0	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_A_0):** Pad Configuration Lock locks specific register fields in the GPP specific registers from being configured. The registers affected become Read-Only and software writes to these registers have no effect. 0 = Unlock 1 = Lock the following register fields as read-only (RO): - Pad Configuration registers (exclude GPIOTXState) - GPI_NMI_EN Register (if implemented) - GPI_SMI_EN Register (if implemented) - GPI_GPE_EN Register (if implemented) When PadCfgLock is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown.

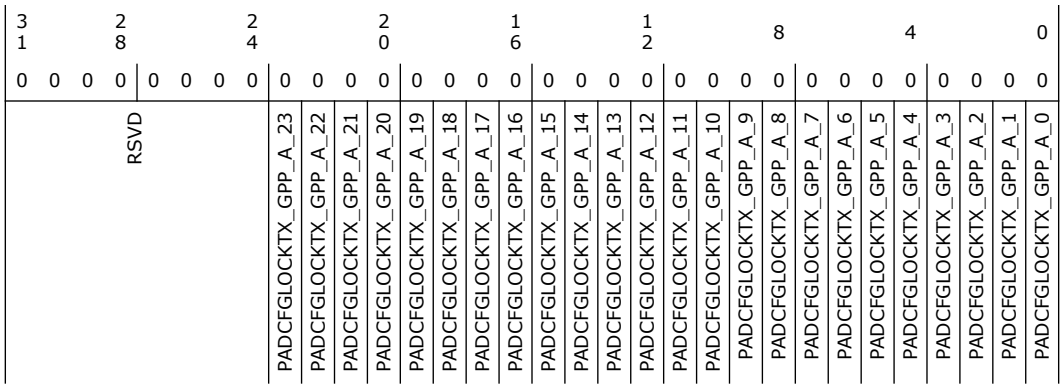
29.1.11 Pad Configuration Lock (PADCFGLOCKTX_GPP_A)—Offset A4h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_A_23):** Applied to GPP_A23. Same description as PADCFGLOCKTX_GPP_A_0
22	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_A_22):** Applied to GPP_A22. Same description as PADCFGLOCKTX_GPP_A_0
21	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_A_21):** Applied to GPP_A21. Same description as PADCFGLOCKTX_GPP_A_0
20	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_A_20):** Applied to GPP_A20. Same description as PADCFGLOCKTX_GPP_A_0

Bit Range	Default & Access	Field Name (ID): Description
19	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_A_19):** Applied to GPP_A19. Same description as PADCFGLOCKTX_GPP_A_0
18	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_A_18):** Applied to GPP_A18. Same description as PADCFGLOCKTX_GPP_A_0
17	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_A_17):** Applied to GPP_A17. Same description as PADCFGLOCKTX_GPP_A_0
16	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_A_16):** Applied to GPP_A16. Same description as PADCFGLOCKTX_GPP_A_0
15	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_A_15):** Applied to GPP_A15. Same description as PADCFGLOCKTX_GPP_A_0
14	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_A_14):** Applied to GPP_A14. Same description as PADCFGLOCKTX_GPP_A_0
13	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_A_13):** Applied to GPP_A13. Same description as PADCFGLOCKTX_GPP_A_0
12	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_A_12):** Applied to GPP_A12. Same description as PADCFGLOCKTX_GPP_A_0
11	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_A_11):** Applied to GPP_A11. Same description as PADCFGLOCKTX_GPP_A_0
10	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_A_10):** Applied to GPP_A10. Same description as PADCFGLOCKTX_GPP_A_0
9	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_A_9):** Applied to GPP_A9. Same description as PADCFGLOCKTX_GPP_A_0
8	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_A_8):** Applied to GPP_A8. Same description as PADCFGLOCKTX_GPP_A_0
7	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_A_7):** Applied to GPP_A7. Same description as PADCFGLOCKTX_GPP_A_0
6	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_A_6):** Applied to GPP_A6. Same description as PADCFGLOCKTX_GPP_A_0
5	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_A_5):** Applied to GPP_A5. Same description as PADCFGLOCKTX_GPP_A_0
4	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_A_4):** Applied to GPP_A4. Same description as PADCFGLOCKTX_GPP_A_0
3	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_A_3):** Applied to GPP_A3. Same description as PADCFGLOCKTX_GPP_A_0
2	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_A_2):** Applied to GPP_A2. Same description as PADCFGLOCKTX_GPP_A_0
1	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_A_1):** Applied to GPP_A1. Same description as PADCFGLOCKTX_GPP_A_0
0	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_A_0):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) When PadCfgLockTx is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown.

29.1.12 Pad Configuration Lock (PADCFGLOCK_GPP_B)—Offset A8h

Same description as PADCFGLOCK_GPP_A register, except this register applies to GPP_B[23:0].

29.1.13 Pad Configuration Lock (PADCFGLOCKTX_GPP_B)—Offset ACh

Same description as PADCFGLOCKTX_GPP_A register, except that this register applies to GPP_B[23:0].

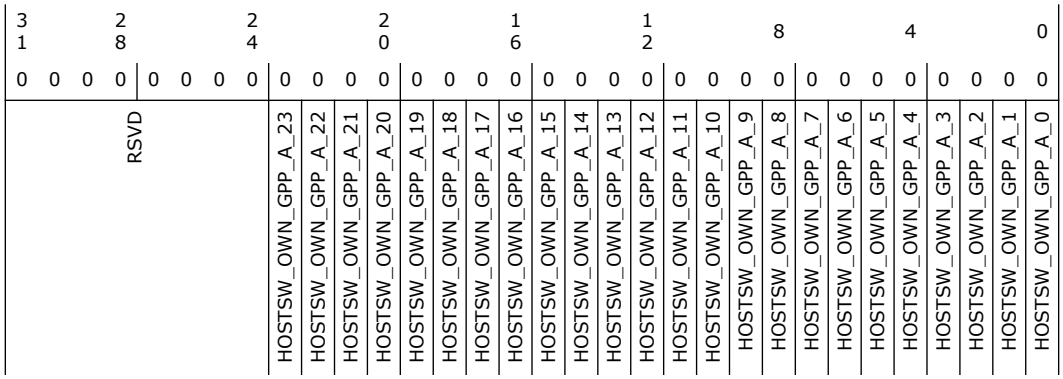
29.1.14 Host Software Pad Ownership (HOSTSW_OWN_GPP_A)—Offset D0h

Access Method

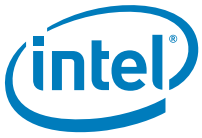
Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_A_23):** Applied to GPP_A23. Same description as bit 0.
22	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_A_22):** Applied to GPP_A22. Same description as bit 0.
21	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_A_21):** Applied to GPP_A21. Same description as bit 0.
20	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_A_20):** Applied to GPP_A20. Same description as bit 0.
19	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_A_19):** Applied to GPP_A19. Same description as bit 0.
18	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_A_18):** Applied to GPP_A18. Same description as bit 0.



Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_A_17):** Applied to GPP_A17. Same description as bit 0.
16	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_A_16):** Applied to GPP_A16. Same description as bit 0.
15	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_A_15):** Applied to GPP_A15. Same description as bit 0.
14	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_A_14):** Applied to GPP_A14. Same description as bit 0.
13	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_A_13):** Applied to GPP_A13. Same description as bit 0.
12	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_A_12):** Applied to GPP_A12. Same description as bit 0.
11	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_A_11):** Applied to GPP_A11. Same description as bit 0.
10	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_A_10):** Applied to GPP_A10. Same description as bit 0.
9	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_A_9):** Applied to GPP_A9. Same description as bit 0.
8	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_A_8):** Applied to GPP_A8. Same description as bit 0.
7	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_A_7):** Applied to GPP_A7. Same description as bit 0.
6	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_A_6):** Applied to GPP_A6. Same description as bit 0.
5	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_A_5):** Applied to GPP_A5. Same description as bit 0.
4	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_A_4):** Applied to GPP_A4. Same description as bit 0.
3	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_A_3):** Applied to GPP_A3. Same description as bit 0.
2	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_A_2):** Applied to GPP_A2. Same description as bit 0.
1	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_A_1):** Applied to GPP_A1. Same description as bit 0.
0	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_A_0):** This register determines the appropriate host status bit update when a pad is under host ownership. 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked.

29.1.15 Host Software Pad Ownership (HOSTSW_OWN_GPP_B)—Offset D4h

Same description as HOSTSW_OWN_GPP_A register, except that this register applies to GPP_B[23:0].

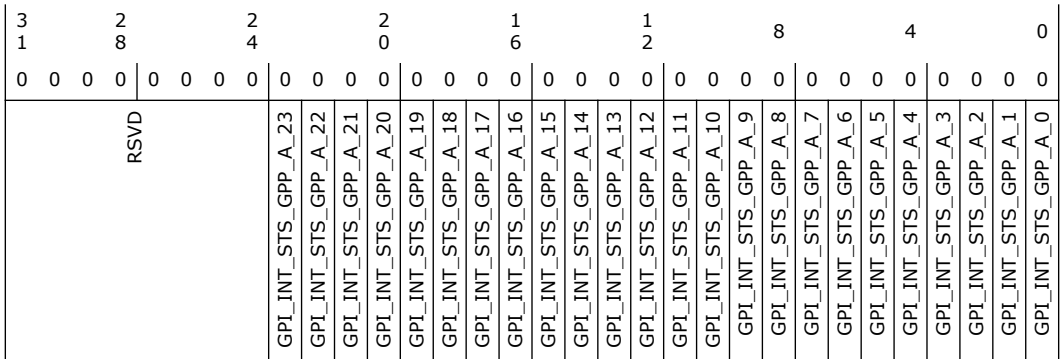
29.1.16 GPI Interrupt Status (GPI_IS_GPP_A)—Offset 100h

Access Method

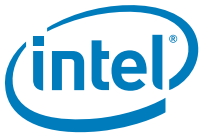
Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_A_23):** Applied to GPP_A23. Same description as bit 0.
22	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_A_22):** Applied to GPP_A22. Same description as bit 0.
21	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_A_21):** Applied to GPP_A21. Same description as bit 0.
20	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_A_20):** Applied to GPP_A20. Same description as bit 0.
19	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_A_19):** Applied to GPP_A19. Same description as bit 0.
18	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_A_18):** Applied to GPP_A18. Same description as bit 0.
17	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_A_17):** Applied to GPP_A17. Same description as bit 0.
16	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_A_16):** Applied to GPP_A16. Same description as bit 0.
15	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_A_15):** Applied to GPP_A15. Same description as bit 0.
14	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_A_14):** Applied to GPP_A14. Same description as bit 0.
13	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_A_13):** Applied to GPP_A13. Same description as bit 0.
12	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_A_12):** Applied to GPP_A12. Same description as bit 0.
11	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_A_11):** Applied to GPP_A11. Same description as bit 0.
10	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_A_10):** Applied to GPP_A10. Same description as bit 0.



Bit Range	Default & Access	Field Name (ID): Description
9	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_A_9):** Applied to GPP_A9. Same description as bit 0.
8	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_A_8):** Applied to GPP_A8. Same description as bit 0.
7	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_A_7):** Applied to GPP_A7. Same description as bit 0.
6	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_A_6):** Applied to GPP_A6. Same description as bit 0.
5	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_A_5):** Applied to GPP_A5. Same description as bit 0.
4	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_A_4):** Applied to GPP_A4. Same description as bit 0.
3	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_A_3):** Applied to GPP_A3. Same description as bit 0.
2	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_A_2):** Applied to GPP_A2. Same description as bit 0.
1	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_A_1):** Applied to GPP_A1. Same description as bit 0.
0	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_A_0):** GPI Interrupt Status (GPI_INT_STS) This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: - The corresponding pad is used in GPIO input mode - HOSTSW_OWN = 1 (i.e. Host GPIO Driver Mode). Writing a value of 1 will clear the bit while writing a value of 0 has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x].

29.1.17 GPI Interrupt Status (GPI_IS_GPP_B)—Offset 104h

Same description as GPI_IS_GPP_A register, except that this register applies to GPP_B[23:0].

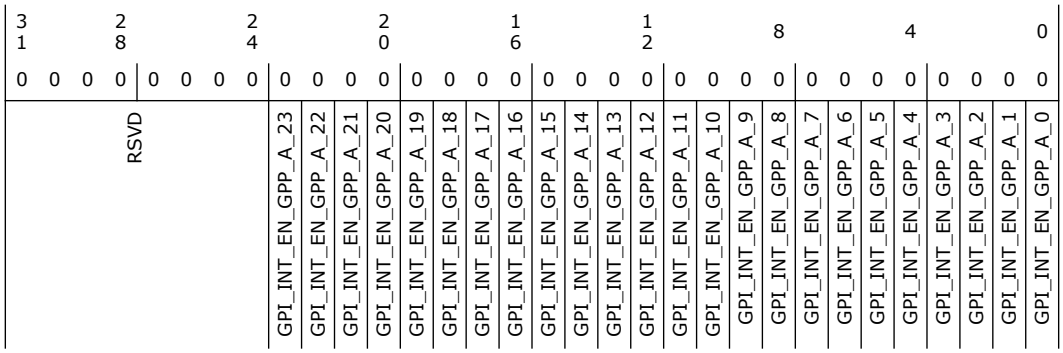
29.1.18 GPI Interrupt Enable (GPI_IE_GPP_A)—Offset 120h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_A_23):** Applied to GPP_A23. Same description as bit 0.
22	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_A_22):** Applied to GPP_A22. Same description as bit 0.
21	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_A_21):** Applied to GPP_A21. Same description as bit 0.
20	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_A_20):** Applied to GPP_A20. Same description as bit 0.
19	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_A_19):** Applied to GPP_A19. Same description as bit 0.
18	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_A_18):** Applied to GPP_A18. Same description as bit 0.
17	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_A_17):** Applied to GPP_A17. Same description as bit 0.
16	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_A_16):** Applied to GPP_A16. Same description as bit 0.
15	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_A_15):** Applied to GPP_A15. Same description as bit 0.
14	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_A_14):** Applied to GPP_A14. Same description as bit 0.
13	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_A_13):** Applied to GPP_A13. Same description as bit 0.
12	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_A_12):** Applied to GPP_A12. Same description as bit 0.
11	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_A_11):** Applied to GPP_A11. Same description as bit 0.
10	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_A_10):** Applied to GPP_A10. Same description as bit 0.
9	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_A_9):** Applied to GPP_A9. Same description as bit 0.
8	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_A_8):** Applied to GPP_A8. Same description as bit 0.
7	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_A_7):** Applied to GPP_A7. Same description as bit 0.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_A_6):** Applied to GPP_A6. Same description as bit 0.
5	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_A_5):** Applied to GPP_A5. Same description as bit 0.
4	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_A_4):** Applied to GPP_A3. Same description as bit 0.
3	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_A_3):** Applied to GPP_A3. Same description as bit 0.
2	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_A_2):** Applied to GPP_A2. Same description as bit 0.
1	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_A_1):** Applied to GPP_A1. Same description as bit 0.
0	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_A_0):** This bit is used to enable/ disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation

29.1.19 GPI Interrupt Enable (GPI_IE_GPP_B)—Offset 124h

Same description as GPI_IE_GPP_A register, except that this register is for GPP_B[23:0].

29.1.20 GPI General Purpose Events Status (GPI_GPE_STS_GPP_A)—Offset 140h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD								GPI_GPE_STS_GPP_A_23	GPI_GPE_STS_GPP_A_22	GPI_GPE_STS_GPP_A_21	GPI_GPE_STS_GPP_A_20	GPI_GPE_STS_GPP_A_19	GPI_GPE_STS_GPP_A_18	GPI_GPE_STS_GPP_A_17	GPI_GPE_STS_GPP_A_16	GPI_GPE_STS_GPP_A_15	GPI_GPE_STS_GPP_A_14	GPI_GPE_STS_GPP_A_13	GPI_GPE_STS_GPP_A_12	GPI_GPE_STS_GPP_A_11	GPI_GPE_STS_GPP_A_10	GPI_GPE_STS_GPP_A_9	GPI_GPE_STS_GPP_A_8	GPI_GPE_STS_GPP_A_7	GPI_GPE_STS_GPP_A_6	GPI_GPE_STS_GPP_A_5	GPI_GPE_STS_GPP_A_4	GPI_GPE_STS_GPP_A_3	GPI_GPE_STS_GPP_A_2	GPI_GPE_STS_GPP_A_1	GPI_GPE_STS_GPP_A_0

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_A_23):** Applied to GPP_A23. Same description as bit 0.
22	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_A_22):** Applied to GPP_A22. Same description as bit 0.
21	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_A_21):** Applied to GPP_A21. Same description as bit 0.
20	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_A_20):** Applied to GPP_A20. Same description as bit 0.
19	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_A_19):** Applied to GPP_A19. Same description as bit 0.
18	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_A_18):** Applied to GPP_A18. Same description as bit 0.
17	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_A_17):** Applied to GPP_A17. Same description as bit 0.
16	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_A_16):** Applied to GPP_A16. Same description as bit 0.
15	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_A_15):** Applied to GPP_A15. Same description as bit 0.
14	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_A_14):** Applied to GPP_A14. Same description as bit 0.
13	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_A_13):** Applied to GPP_A13. Same description as bit 0.
12	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_A_12):** Applied to GPP_A12. Same description as bit 0.
11	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_A_11):** Applied to GPP_A11. Same description as bit 0.
10	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_A_10):** Applied to GPP_A10. Same description as bit 0.
9	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_A_9):** Applied to GPP_A9. Same description as bit 0.
8	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_A_8):** Applied to GPP_A8. Same description as bit 0.
7	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_A_7):** Applied to GPP_A7. Same description as bit 0.
6	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_A_6):** Applied to GPP_A6. Same description as bit 0.
5	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_A_5):** Applied to GPP_A5. Same description as bit 0.
4	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_A_4):** Applied to GPP_A4. Same description as bit 0.
3	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_A_3):** Applied to GPP_A3. Same description as bit 0.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_A_2):** Applied to GPP_A2. Same description as bit 0.
1	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_A_1):** Applied to GPP_A1. Same description as bit 0.
0	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_A_0):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high(or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS bit is set: - If the system is in an S3-S5 state, the event will also wake the system. - If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN does not prevent the setting of GPI_GPE_STS.

29.1.21 GPI General Purpose Events Status (GPI_GPE_STS_GPP_B)—Offset 144h

Same description as PI_GPE_STS_GPP_A register, except that this is for GPP_B[23:0].

29.1.22 GPI General Purpose Events Enable (GPI_GPE_EN_GPP_A)—Offset 160h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD								GPI_GPE_EN_GPP_A_23	GPI_GPE_EN_GPP_A_22	GPI_GPE_EN_GPP_A_21	GPI_GPE_EN_GPP_A_20	GPI_GPE_EN_GPP_A_19	GPI_GPE_EN_GPP_A_18	GPI_GPE_EN_GPP_A_17	GPI_GPE_EN_GPP_A_16	GPI_GPE_EN_GPP_A_15	GPI_GPE_EN_GPP_A_14	GPI_GPE_EN_GPP_A_13	GPI_GPE_EN_GPP_A_12	GPI_GPE_EN_GPP_A_11	GPI_GPE_EN_GPP_A_10	GPI_GPE_EN_GPP_A_9	GPI_GPE_EN_GPP_A_8	GPI_GPE_EN_GPP_A_7	GPI_GPE_EN_GPP_A_6	GPI_GPE_EN_GPP_A_5	GPI_GPE_EN_GPP_A_4	GPI_GPE_EN_GPP_A_3	GPI_GPE_EN_GPP_A_2	GPI_GPE_EN_GPP_A_1	GPI_GPE_EN_GPP_A_0

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_A_23):** Applied to GPP_A23. Same description as bit 0.
22	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_A_22):** Applied to GPP_A22. Same description as bit 0.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_A_21):** Applied to GPP_A21. Same description as bit 0.
20	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_A_20):** Applied to GPP_A20. Same description as bit 0.
19	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_A_19):** Applied to GPP_A19. Same description as bit 0.
18	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_A_18):** Applied to GPP_A18. Same description as bit 0.
17	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_A_17):** Applied to GPP_A17. Same description as bit 0.
16	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_A_16):** Applied to GPP_A16. Same description as bit 0.
15	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_A_15):** Applied to GPP_A15. Same description as bit 0.
14	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_A_14):** Applied to GPP_A14. Same description as bit 0.
13	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_A_13):** Applied to GPP_A13. Same description as bit 0.
12	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_A_12):** Applied to GPP_A12. Same description as bit 0.
11	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_A_11):** Applied to GPP_A11. Same description as bit 0.
10	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_A_10):** Applied to GPP_A10. Same description as bit 0.
9	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_A_9):** Applied to GPP_A9. Same description as bit 0.
8	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_A_8):** Applied to GPP_A8. Same description as bit 0.
7	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_A_7):** Applied to GPP_A7. Same description as bit 0.
6	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_A_6):** Applied to GPP_A6. Same description as bit 0.
5	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_A_5):** Applied to GPP_A5. Same description as bit 0.
4	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_A_4):** Applied to GPP_A4. Same description as bit 0.
3	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_A_3):** Applied to GPP_A3. Same description as bit 0.
2	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_A_2):** Applied to GPP_A2. Same description as bit 0.
1	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_A_1):** Applied to GPP_A1. Same description as bit 0.
0	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_A_0):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'.

29.1.23 GPI General Purpose Events Enable (GPI_GPE_EN_GPP_B)—Offset 164h

Same description as PI_GPI_GPE_EN_GPP_A register, except that this is for GPP_B[23:0].

29.1.24 SMI Status (GPI_SMI_STS_GPP_B)—Offset 184h

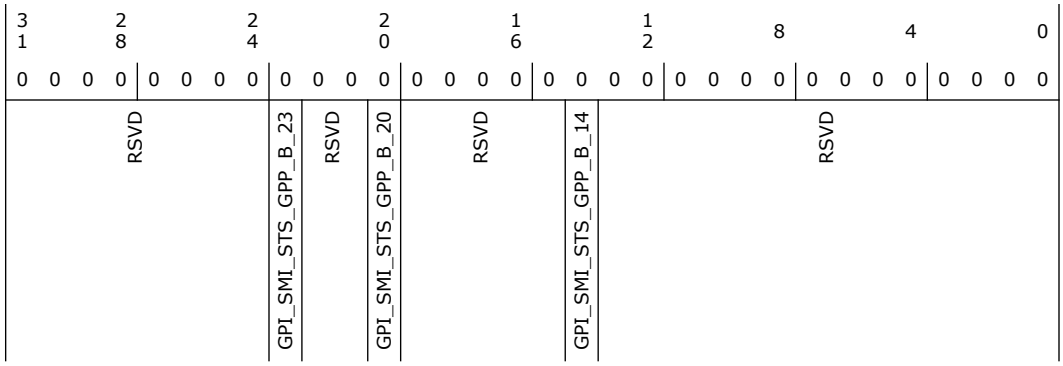
Register bits in this register are implemented for GPP_B signals that have SMI capability only. Other bits are reserved and RO.

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RW1C	**GPI SMI Status (GPI_SMI_STS_GPP_B_23):** Same description as bit 14.
22:21	0h RO	Reserved.
20	0h RW1C	**GPI SMI Status (GPI_SMI_STS_GPP_B_20):** Same description as bit 14.

Bit Range	Default & Access	Field Name (ID): Description
19:15	0h RO	Reserved.
14	0h RW1C	**GPI SMI Status (GPI_SMI_STS_GPP_B_14):** This bit is set to 1 by hardware when a level event (See RxEdCfg,RxInv) is detected, and all the following conditions are true: - The corresponding pad is used in GPIO input mode - The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of 1 will clear the bit while writing a value of 0 has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN does not prevent the setting of GPI_SMI_STS. Defaults for these bits are dependent on the state of the GPI pads.
13:0	0h RO	Reserved.

29.1.25 SMI Enable (GPI_SMI_EN_GPP_B)—Offset 1A4h

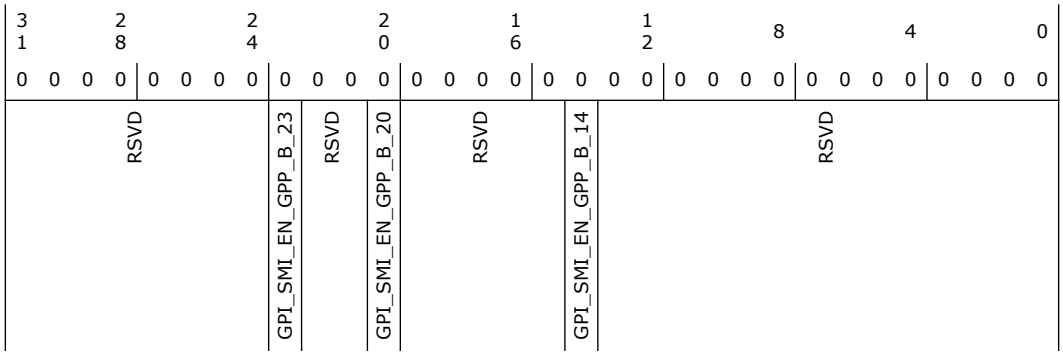
Register bits in this register are implemented for GPP_B signals that have SMI capability only. Other bits are reserved and RO.

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPP_B_23):** Same description as bit 14.
22:21	0h RO	Reserved.
20	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPP_B_20):** Same description as bit 14.

Bit Range	Default & Access	Field Name (ID): Description
19:15	0h RO	Reserved.
14	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPP_B_14):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to 1. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is 1, bit0 of this bit is locked down to read-only.
13:0	0h RO	Reserved.

29.1.26 NMI Status (GPI_NMI_STS_GPP_B)—Offset 1C4h

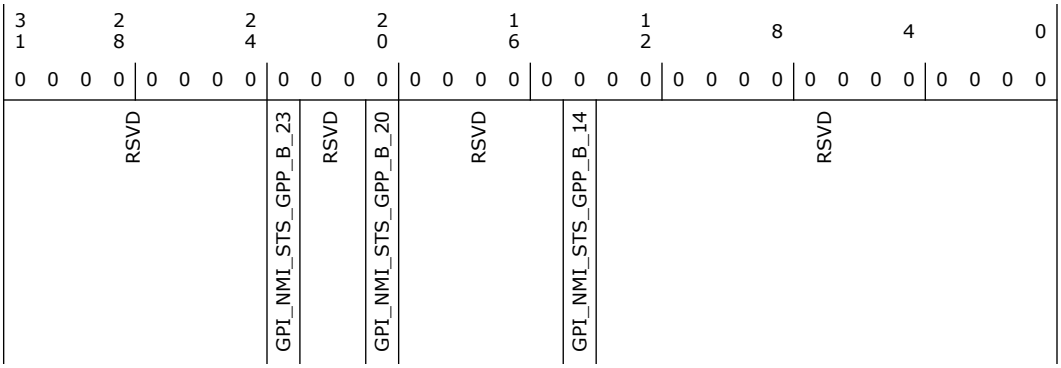
Register bits in this register are implemented for GPP_B signals that have NMI capability only. Other bits are reserved and RO.

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RW1C	**GPI NMI Status (GPI_NMI_STS_GPP_B_23):** Same description as bit 14.
22:21	0h RO	Reserved.
20	0h RW1C	**GPI NMI Status (GPI_NMI_STS_GPP_B_20):** Same description as bit 14.

Bit Range	Default & Access	Field Name (ID): Description
19:15	0h RO	Reserved.
14	0h RW1C	**GPI NMI Status (GPI_NMI_STS_GPP_B_14):** This bit is set to 1 by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: - The corresponding pad is used in GPIO input mode (PMode) - The corresponding GPIONMIRout is set to 1, i.e. programmed to route as NMI - The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). - The corresponding GPI_NMI_EN is set Writing a value of 1 will clear the bit while writing a value of 0 has no effect. 0 = There is no NMI event 1 = There is an NMI event
13:0	0h RO	Reserved.

29.1.27 NMI Enable (GPI_NMI_EN_GPP_B)—Offset 1E4h

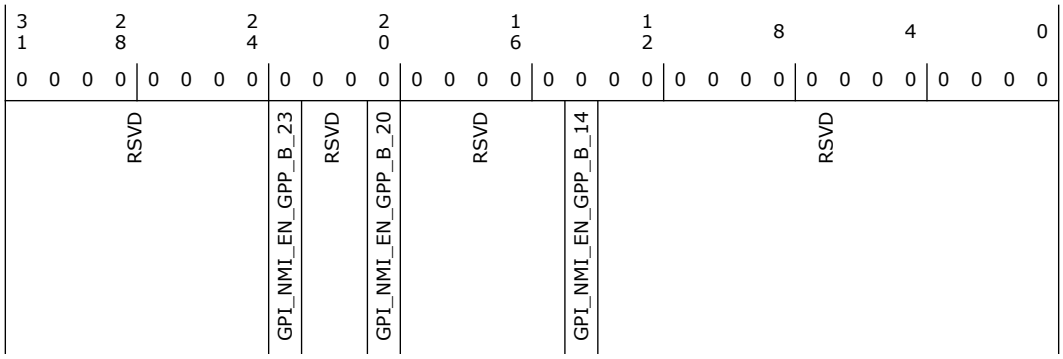
Register bits in this register are implemented for GPP_B signals that have NMI capability only. Other bits are reserved and RO.

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPP_B_23):** Same description as bit 14.
22:21	0h RO	Reserved.
20	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPP_B_20):** Same description as bit 14.

Bit Range	Default & Access	Field Name (ID): Description
19:15	0h RO	Reserved.
14	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPP_B_14):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only.
13:0	0h RO	Reserved.

29.1.28 Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_0)—Offset 400h

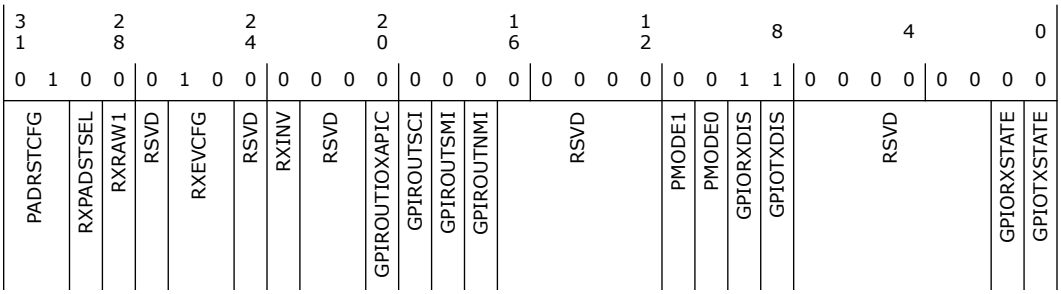
This register applies to GPP_A0.

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 44000x00h



Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset GPIO pad register fields in PAD_CFG_DW0 and PAD_CFG_DW1 registers. This register can be used for Sx isolation of the associated signal if needed. 00 = RSMRST# 01 = Host deep reset. This reset occurs when a host reset (with or without power cycle) is initiated or a global reset is initiated, except that the reset does not assert when in S3/S4/S5. 10 = PLTRST# 11 = Reserved
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determines from which node the RX pad state for native function should be taken from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from RX buffer 1 = Internal RX pad state (subject to RXINV and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field is only applicable when the RX buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally

Bit Range	Default & Access	Field Name (ID): Description
27	0h RO	Reserved.
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determines if the internal RX pad state (synchronized, filtered vs non-filtered version as determined by PreGfRXSel, and is further subject to RXInv) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller . 0h = Level 1h = Edge 2h = Drive '0' 3h = Reserved (implement as setting 0h)
24	0h RO	Reserved.
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field is only applicable when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RO	Reserved.
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determines if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determines if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI. 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s).
18	0h RW	**GPIO Input Route SMI (GPIROUTSMI):** Determines if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s). This bit only applies to a GPIO that has SMI capability. Otherwise, the bit is RO.
17	0h RW	**GPIO Input Route NMI (GPIROUTNMI):** Determines if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit. This bit only applies to a GPIO that has NMI capability. Otherwise, the bit is RO.
16:12	0h RO	Reserved.
11	-- RW	**Pad Mode bit 1 (PMODE1):** See Pad Mode Bit 0 description.

Bit Range	Default & Access	Field Name (ID): Description
10	-- RW	**Pad Mode bit 0 (PMODE0):** This bit is used in conjunction with Pad Mode bit 1. This two-bit field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad. 1h = native function 1, if applicable, controls the Pad 2h = native function 2, if applicable, controls the Pad. Also used to enable the GPIO blink (PWM) capability if applicable (note that not all GPIOs have the blink capability) 3h = native function 3, if applicable, controls the Pad Dedicated (unmuxed) GPIO shall report RO of all 0's in this register field If GPIO vs. native mode is configured via soft strap, this bit has no effect. Default value is determined by the default functionality of the pad.
9	1h RW	**GPIO RX Disable (GPIORXDIS):** 0 = Enable the input buffer (active low enable) of the pad. 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0'.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** 0 = Enable the output buffer (active low enable) of the pad. 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	Reserved.
1	0h RO	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV settings.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** 0 = Drive a level '0' to the TX output pad. 1 = Drive a level '1' to the TX output pad

29.1.29 Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_0)—Offset 404h

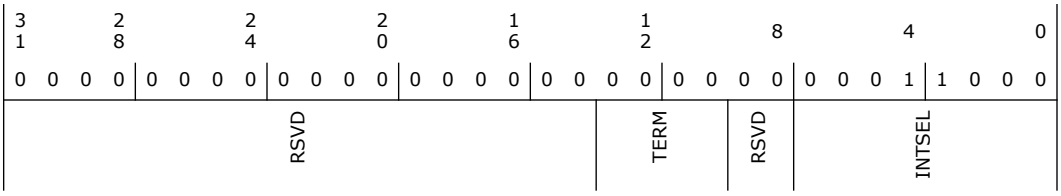
This register applies to GPP_A0.

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 18h



Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings for [13:10] correspond to: 0000: none 0010: 5k pd 0100: 20k pd 1010: 5k pu 1100: 20k pu 1111: Native controller selected by Pad Mode controls the Termination. This setting needs to be set only for GPP_A1 / LAD0, GPP_A2 / LAD1, GPP_A3 / LAD2, GPP_A4 / LAD3, GPD1 / ACPRESENT, and GPD2 / LAN_WAKE#, when the signals are used as native function. Otherwise, the setting is reserved. All others settings not mentioned above are reserved. If a reserved value is programmed, pad may malfunction. The setting of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in sw/fw in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, pu/pd settings should be programmed first to ensure the input does not float momentarily.
9:8	0h RO	Reserved.
7:0	18h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 .... Up to the max IOxAPIC IRQ supported

29.1.30 Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_1)—Offset 408h

This register applies to GPP_A1 and has the same description as PAD_CFG_DW0_GPP_A_0.

29.1.31 Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_1)—Offset 40Ch

This register applies to GPP_A1 and has the same description as PAD_CFG_DW1_GPP_A_0.
Exception:
INTSEL bit field default: 19h
TERM bit field default:
1111b in LPC mode
1100b in eSPI mode

29.1.32 Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_2)—Offset 410h

This register applies to GPP_A2 and has the same description as PAD_CFG_DW0_GPP_A_0.

29.1.33 Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_2)—Offset 414h

This register applies to GPP_A2 and has the same description as PAD_CFG_DW1_GPP_A_0.
Exception:
INTSEL bit field default: 1Ah
TERM bit field default:
1111b in LPC mode
1100b in eSPI mode

29.1.34 Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_3)—Offset 418h

This register applies to GPP_A3 and has the same description as PAD_CFG_DW0_GPP_A_0.

29.1.35 Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_3)—Offset 41Ch

This register applies to GPP_A3 and has the same description as PAD_CFG_DW1_GPP_A_0.
Exception:
INTSEL bit field default: 1Bh
TERM bit field default:
1111b in LPC mode
1100b in eSPI mode

29.1.36 Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_4)—Offset 420h

This register applies to GPP_A4 and has the same description as PAD_CFG_DW0_GPP_A_0.

29.1.37 Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_4)—Offset 424h

This register applies to GPP_A4 and has the same description as PAD_CFG_DW1_GPP_A_0.
Exception:
INTSEL bit field default: 1Ch
TERM bit field default:
1111b in LPC mode
1100b in eSPI mode

29.1.38 Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_5)—Offset 428h

This register applies to GPP_A5 and has the same description as PAD_CFG_DW0_GPP_A_0.

29.1.39 Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_5)—Offset 42Ch

This register applies to GPP_A5 and has the same description as PAD_CFG_DW1_GPP_A_0.
Exception:
INTSEL bit field default: 1Dh
TERM bit field default:
0000b in LPC mode
1100b in eSPI mode

29.1.40 Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_6)—Offset 430h

This register applies to GPP_A6 and has the same description as PAD_CFG_DW0_GPP_A_0.

29.1.41 Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_6)—Offset 434h

This register applies to GPP_A6 and has the same description as PAD_CFG_DW1_GPP_A_0.
Exception: The default value of the INTSEL bit field in this register is : 1Eh

29.1.42 Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_7)—Offset 438h

This register applies to GPP_A7 and has the same description as PAD_CFG_DW0_GPP_A_0.

29.1.43 Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_7)—Offset 43Ch

This register applies to GPP_A7 and has the same description as PAD_CFG_DW1_GPP_A_0.
Exception: The default value of the INTSEL bit field in this register is : 1Fh

29.1.44 Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_8)—Offset 440h

This register applies to GPP_A8 and has the same description as PAD_CFG_DW0_GPP_A_0.

29.1.45 Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_8)—Offset 444h

This register applies to GPP_A8 and has the same description as PAD_CFG_DW1_GPP_A_0.
Exception: The default value of the INTSEL bit field in this register is : 20h

29.1.46 Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_9)—Offset 448h

This register applies to GPP_A9 and has the same description as PAD_CFG_DW0_GPP_A_0.

29.1.47 Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_9)—Offset 44Ch

This register applies to GPP_A9 and has the same description as PAD_CFG_DW1_GPP_A_0.
Exception:
INTSEL bit field default: 21h
TERM bit field default: 0100b

29.1.48 Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_10)—Offset 450h

This register applies to GPP_A10 and has the same description as PAD_CFG_DW0_GPP_A_0.

29.1.49 Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_10)—Offset 454h

This register applies to GPP_A10 and has the same description as PAD_CFG_DW1_GPP_A_0.
Exception:
INTSEL bit field default: 22h
TERM bit field default:
0100b in LPC mode
0000h in eSPI mode

29.1.50 Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_11)—Offset 458h

This register applies to GPP_A11 and has the same description as PAD_CFG_DW0_GPP_A_0.

29.1.51 Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_11)—Offset 45Ch

This register applies to GPP_A11 and has the same description as PAD_CFG_DW1_GPP_A_0.
Exception:
INTSEL bit field default: 23h
TERM bit field default:
1100b in LPC mode
0000b in eSPI mode

29.1.52 Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_12)—Offset 460h

This register applies to GPP_A12 and has the same description as PAD_CFG_DW0_GPP_A_0.

29.1.53 Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_12)—Offset 464h

This register applies to GPP_A12 and has the same description as PAD_CFG_DW1_GPP_A_0.
Exception: The default value of the INTSEL bit field in this register is : 24h

29.1.54 Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_13)—Offset 468h

This register applies to GPP_A13 and has the same description as PAD_CFG_DW0_GPP_A_0.

29.1.55 Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_13)—Offset 46Ch

This register applies to GPP_A13 and has the same description as PAD_CFG_DW1_GPP_A_0.
Exception: The default value of the INTSEL bit field in this register is : 25h

29.1.56 Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_14)—Offset 470h

This register applies to GPP_A14 and has the same description as PAD_CFG_DW0_GPP_A_0.

29.1.57 Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_14)—Offset 474h

This register applies to GPP_A14 and has the same description as PAD_CFG_DW1_GPP_A_0.
Exception: The default value of the INTSEL bit field in this register is : 26h

29.1.58 Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_15)—Offset 478h

This register applies to GPP_A15 and has the same description as PAD_CFG_DW0_GPP_A_0.

29.1.59 Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_15)—Offset 47Ch

This register applies to GPP_A15 and has the same description as PAD_CFG_DW1_GPP_A_0.
Exception:

INTSEL bit field default: 27h
TERM bit field default:
1100b in LPC mode
0000b in eSPI mode

29.1.60 Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_16)—Offset 480h

This register applies to GPP_A16 and has the same description as PAD_CFG_DW0_GPP_A_0.

29.1.61 Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_16)—Offset 484h

This register applies to GPP_A16 and has the same description as PAD_CFG_DW1_GPP_A_0.
Exception: The default value of the INTSEL bit field in this register is : 28h

29.1.62 Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_17)—Offset 488h

This register applies to GPP_A17 and has the same description as PAD_CFG_DW0_GPP_A_0.

29.1.63 Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_17)—Offset 48Ch

This register applies to GPP_A17 and has the same description as PAD_CFG_DW1_GPP_A_0.
Exception: The default value of the INTSEL bit field in this register is : 29h

29.1.64 Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_18)—Offset 490h

This register applies to GPP_A18 and has the same description as PAD_CFG_DW0_GPP_A_0.

29.1.65 Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_18)—Offset 494h

This register applies to GPP_A18 and has the same description as PAD_CFG_DW1_GPP_A_0.
Exception: The default value of the INTSEL bit field in this register is : 2Ah

29.1.66 Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_19)—Offset 498h

This register applies to GPP_A19 and has the same description as PAD_CFG_DW0_GPP_A_0.

29.1.67 Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_19)—Offset 49Ch

This register applies to GPP_A19 and has the same description as PAD_CFG_DW1_GPP_A_0.
Exception: The default value of the INTSEL bit field in this register is : 2Bh

29.1.68 Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_20)—Offset 4A0h

This register applies to GPP_A20 and has the same description as PAD_CFG_DW0_GPP_A_0.

29.1.69 Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_20)—Offset 4A4h

This register applies to GPP_A20 and has the same description as PAD_CFG_DW1_GPP_A_0.
Exception: The default value of the INTSEL bit field in this register is : 2Ch

29.1.70 Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_21)—Offset 4A8h

This register applies to GPP_A21 and has the same description as PAD_CFG_DW0_GPP_A_0.

29.1.71 Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_21)—Offset 4ACh

This register applies to GPP_A21 and has the same description as PAD_CFG_DW1_GPP_A_0.
Exception: The default value of the INTSEL bit field in this register is : 2Dh

29.1.72 Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_22)—Offset 4B0h

This register applies to GPP_A22 and has the same description as PAD_CFG_DW0_GPP_A_0.

29.1.73 Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_22)—Offset 4B4h

This register applies to GPP_A22 and has the same description as PAD_CFG_DW1_GPP_A_0.
Exception: The default value of the INTSEL bit field in this register is : 2Eh

29.1.74 Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_23)—Offset 4B8h

This register applies to GPP_A23 and has the same description as PAD_CFG_DW0_GPP_A_0.

29.1.75 Pad Configuration DW1 (PAD_CFG_DW1_GPP_A_23)—Offset 4BCh

This register applies to GPP_A23 and has the same description as PAD_CFG_DW1_GPP_A_0.
Exception: The default value of the INTSEL bit field in this register is : 2Fh

29.1.76 Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_0)—Offset 4C0h

This register applies to GPP_B0 and has the same description as PAD_CFG_DW0_GPP_A_0.

29.1.77 Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_0)—Offset 4C4h

This register applies to GPP_B0 and has the same description as PAD_CFG_DW1_GPP_A_0.
Exception: The default value of the INTSEL bit field in this register is : 8'h30

29.1.78 Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_1)—Offset 4C8h

This register applies to GPP_B1 and has the same description as PAD_CFG_DW0_GPP_A_0.

29.1.79 Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_1)—Offset 4CCh

This register applies to GPP_B1 and has the same description as PAD_CFG_DW1_GPP_A_0. Exception: The default value of the INTSEL bit field in this register is : 31h

29.1.80 Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_2)—Offset 4D0h

This register applies to GPP_B2 and has the same description as PAD_CFG_DW0_GPP_A_0.

29.1.81 Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_2)—Offset 4D4h

This register applies to GPP_B2 and has the same description as PAD_CFG_DW1_GPP_A_0. Exception: The default value of the INTSEL bit field in this register is : 32h

29.1.82 Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_3)—Offset 4D8h

This register applies to GPP_B3 and has the same description as PAD_CFG_DW0_GPP_A_0.

29.1.83 Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_3)—Offset 4DCh

This register applies to GPP_B3 and has the same description as PAD_CFG_DW1_GPP_A_0. Exception: The default value of the INTSEL bit field in this register is : 33h

29.1.84 Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_4)—Offset 4E0h

This register applies to GPP_B4 and has the same description as PAD_CFG_DW0_GPP_A_0.

29.1.85 Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_4)—Offset 4E4h

This register applies to GPP_B4 and has the same description as PAD_CFG_DW1_GPP_A_0. Exception: The default value of the INTSEL bit field in this register is : 34h

29.1.86 Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_5)—Offset 4E8h

This register applies to GPP_B5 and has the same description as PAD_CFG_DW0_GPP_A_0.

29.1.87 Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_5)—Offset 4ECh

This register applies to GPP_B5 and has the same description as PAD_CFG_DW1_GPP_A_0. Exception: The default value of the INTSEL bit field in this register is : 35h

29.1.88 Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_6)—Offset 4F0h

This register applies to GPP_B6 and has the same description as PAD_CFG_DW0_GPP_A_0.

29.1.89 Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_6)—Offset 4F4h

This register applies to GPP_B6 and has the same description as PAD_CFG_DW1_GPP_A_0. Exception: The default value of the INTSEL bit field in this register is : 36h

29.1.90 Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_7)—Offset 4F8h

This register applies to GPP_B7 and has the same description as PAD_CFG_DW0_GPP_A_0.

29.1.91 Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_7)—Offset 4FCh

This register applies to GPP_B7 and has the same description as PAD_CFG_DW1_GPP_A_0. Exception: The default value of the INTSEL bit field in this register is : 37h

29.1.92 Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_8)—Offset 500h

This register applies to GPP_B8 and has the same description as PAD_CFG_DW0_GPP_A_0.

29.1.93 Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_8)—Offset 504h

This register applies to GPP_B8 and has the same description as PAD_CFG_DW1_GPP_A_0. Exception: The default value of the INTSEL bit field in this register is : 38h

29.1.94 Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_9)—Offset 508h

This register applies to GPP_B9 and has the same description as PAD_CFG_DW0_GPP_A_0.

29.1.95 Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_9)—Offset 50Ch

This register applies to GPP_B9 and has the same description as PAD_CFG_DW1_GPP_A_0. Exception: The default value of the INTSEL bit field in this register is : 39h

29.1.96 Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_10)—Offset 510h

This register applies to GPP_B10 and has the same description as PAD_CFG_DW0_GPP_A_0.

29.1.97 Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_10)—Offset 514h

This register applies to GPP_B10 and has the same description as PAD_CFG_DW1_GPP_A_0. Exception: The default value of the INTSEL bit field in this register is : 3Ah

29.1.98 Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_11)—Offset 518h

This register applies to GPP_B11 and has the same description as PAD_CFG_DW0_GPP_A_0.

29.1.99 Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_11)—Offset 51Ch

This register applies to GPP_B11 and has the same description as PAD_CFG_DW1_GPP_A_0. Exception: The default value of the INTSEL bit field in this register is : 3Bh

29.1.100 Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_12)—Offset 520h

This register applies to GPP_B12 and has the same description as PAD_CFG_DW0_GPP_A_0.

29.1.101 Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_12)—Offset 524h

This register applies to GPP_B12 and has the same description as PAD_CFG_DW1_GPP_A_0. Exception: The default value of the INTSEL bit field in this register is : 3Ch

29.1.102 Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_13)—Offset 528h

This register applies to GPP_B13 and has the same description as PAD_CFG_DW0_GPP_A_0.

29.1.103 Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_13)—Offset 52Ch

This register applies to GPP_B13 and has the same description as PAD_CFG_DW1_GPP_A_0. Exception: The default value of the INTSEL bit field in this register is : 3Dh

29.1.104 Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_14)—Offset 530h

This register applies to GPP_B14 and has the same description as PAD_CFG_DW0_GPP_A_0.

29.1.105 Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_14)—Offset 534h

This register applies to GPP_B14 and has the same description as PAD_CFG_DW1_GPP_A_0.
Exception:
INTSEL bit field default: 3Eh
TERM bit field default: 0100b

29.1.106 Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_15)—Offset 538h

This register applies to GPP_B15 and has the same description as PAD_CFG_DW0_GPP_A_0.

29.1.107 Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_15)—Offset 53Ch

This register applies to GPP_B15 and has the same description as PAD_CFG_DW1_GPP_A_0. Exception: The default value of the INTSEL bit field in this register is : 3Fh

29.1.108 Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_16)—Offset 540h

This register applies to GPP_B16 and has the same description as PAD_CFG_DW0_GPP_A_0.

29.1.109 Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_16)—Offset 544h

This register applies to GPP_B16 and has the same description as PAD_CFG_DW1_GPP_A_0. Exception: The default value of the INTSEL bit field in this register is : 40h

29.1.110 Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_17)—Offset 548h

This register applies to GPP_B17 and has the same description as PAD_CFG_DW0_GPP_A_0.

29.1.111 Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_17)—Offset 54Ch

This register applies to GPP_B17 and has the same description as PAD_CFG_DW1_GPP_A_0. Exception: The default value of the INTSEL bit field in this register is : 41h

29.1.112 Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_18)—Offset 550h

This register applies to GPP_B18 and has the same description as PAD_CFG_DW0_GPP_A_0.

29.1.113 Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_18)—Offset 554h

This register applies to GPP_B18 and has the same description as PAD_CFG_DW1_GPP_A_0. Exception: The default value of the INTSEL bit field in this register is : 42h

29.1.114 Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_19)—Offset 558h

This register applies to GPP_B19 and has the same description as PAD_CFG_DW0_GPP_A_0.

29.1.115 Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_19)—Offset 55Ch

This register applies to GPP_B19 and has the same description as PAD_CFG_DW1_GPP_A_0. Exception: The default value of the INTSEL bit field in this register is : 43h

29.1.116 Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_20)—Offset 560h

This register applies to GPP_B20 and has the same description as PAD_CFG_DW0_GPP_A_0.

29.1.117 Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_20)—Offset 564h

This register applies to GPP_B20 and has the same description as PAD_CFG_DW1_GPP_A_0. Exception: The default value of the INTSEL bit field in this register is : 44h

29.1.118 Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_21)—Offset 568h

This register applies to GPP_B21 and has the same description as PAD_CFG_DW0_GPP_A_0.

29.1.119 Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_21)—Offset 56Ch

This register applies to GPP_B21 and has the same description as PAD_CFG_DW1_GPP_A_0. Exception: The default value of the INTSEL bit field in this register is : 45h

29.1.120 Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_22)—Offset 570h

This register applies to GPP_B22 and has the same description as PAD_CFG_DW0_GPP_A_0.

29.1.121 Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_22)—Offset 574h

This register applies to GPP_B22 and has the same description as PAD_CFG_DW1_GPP_A_0. Exception: The default value of the INTSEL bit field in this register is : 46h

29.1.122 Pad Configuration DW0 (PAD_CFG_DW0_GPP_B_23)—Offset 578h

This register applies to GPP_B23 and has the same description as PAD_CFG_DW0_GPP_A_0.

29.1.123 Pad Configuration DW1 (PAD_CFG_DW1_GPP_B_23)—Offset 57Ch

This register applies to GPP_B23 and has the same description as PAD_CFG_DW1_GPP_A_0. Exception: The default value of the INTSEL bit field in this register is : 47h

29.2 GPIO Community 1 Registers Summary

Community 1 Registers are for GPP_C and GPP_D, and GPP_E groups.

These registers are within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID + Register Offset).

Table 29-2. Summary of GPIO Community 1 Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
8h	Bh	Family Base Address (FAMBAR)—Offset 8h	300h
Ch	Fh	Pad Base Address (PADBAR)—Offset Ch	400h
10h	13h	Miscellaneous Configuration (MISCCFG)—Offset 10h	43200h
20h	23h	Pad Ownership (PAD_OWN_GPP_C_0)—Offset 20h	0h
24h	27h	Pad Ownership (PAD_OWN_GPP_C_1)—Offset 24h	0h
28h	2Bh	Pad Ownership (PAD_OWN_GPP_C_2)—Offset 28h	0h
30h	33h	Pad Ownership (PAD_OWN_GPP_D_0)—Offset 30h	0h
34h	37h	Pad Ownership (PAD_OWN_GPP_D_1)—Offset 34h	0h
38h	3Bh	Pad Ownership (PAD_OWN_GPP_D_2)—Offset 38h	0h
40h	43h	Pad Ownership (PAD_OWN_GPP_E_0)—Offset 40h	0h
44h	47h	Pad Ownership (PAD_OWN_GPP_E_1)—Offset 44h	0h
48h	4Bh	Pad Ownership (PAD_OWN_GPP_E_2)—Offset 48h	0h
A0h	A3h	Pad Configuration Lock (PADCFGLOCK_GPP_C)—Offset A0h	0h
A4h	A7h	Pad Configuration Lock (PADCFGLOCKTX_GPP_C)—Offset A4h	0h
A8h	ABh	Pad Configuration Lock (PADCFGLOCK_GPP_D)—Offset A8h	0h
ACh	AFh	Pad Configuration Lock (PADCFGLOCKTX_GPP_D)—Offset ACh	0h
B0h	B3h	Pad Configuration Lock (PADCFGLOCK_GPP_E)—Offset B0h	0h
B4h	B7h	Pad Configuration Lock (PADCFGLOCKTX_GPP_E)—Offset B4h	0h
D0h	D3h	Host Software Pad Ownership (HOSTSW_OWN_GPP_C)—Offset D0h	0h
D4h	D7h	Host Software Pad Ownership (HOSTSW_OWN_GPP_D)—Offset D4h	0h
D8h	DBh	Host Software Pad Ownership (HOSTSW_OWN_GPP_E)—Offset D8h	0h

Table 29-2. Summary of GPIO Community 1 Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
100h	103h	GPI Interrupt Status (GPI_IS_GPP_C)—Offset 100h	0h
104h	107h	GPI Interrupt Status (GPI_IS_GPP_D)—Offset 104h	0h
108h	10Bh	GPI Interrupt Status (GPI_IS_GPP_E)—Offset 108h	0h
120h	123h	GPI Interrupt Enable (GPI_IE_GPP_C)—Offset 120h	0h
124h	127h	GPI Interrupt Enable (GPI_IE_GPP_D)—Offset 124h	0h
128h	12Bh	GPI Interrupt Enable (GPI_IE_GPP_E)—Offset 128h	0h
140h	143h	GPI General Purpose Events Status (GPI_GPE_STS_GPP_C)—Offset 140h	0h
144h	147h	GPI General Purpose Events Status (GPI_GPE_STS_GPP_D)—Offset 144h	0h
148h	14Bh	GPI General Purpose Events Status (GPI_GPE_STS_GPP_E)—Offset 148h	0h
160h	163h	GPI General Purpose Events Enable (GPI_GPE_EN_GPP_C)—Offset 160h	0h
164h	167h	GPI General Purpose Events Enable (GPI_GPE_EN_GPP_D)—Offset 164h	0h
168h	16Bh	GPI General Purpose Events Enable (GPI_GPE_EN_GPP_E)—Offset 168h	0h
180h	183h	SMI Status (GPI_SMI_STS_GPP_C)—Offset 180h	0h
184h	187h	SMI Status (GPI_SMI_STS_GPP_D)—Offset 184h	0h
188h	18Bh	SMI Status (GPI_SMI_STS_GPP_E)—Offset 188h	0h
1A0h	1A3h	SMI Enable (GPI_SMI_EN_GPP_C)—Offset 1A0h	0h
1A4h	1A7h	SMI Enable (GPI_SMI_EN_GPP_D)—Offset 1A4h	0h
1A8h	1ABh	SMI Enable (GPI_SMI_EN_GPP_E)—Offset 1A8h	0h
1C0h	1C3h	NMI Status (GPI_NMI_STS_GPP_C)—Offset 1C0h	0h
1C4h	1C7h	NMI Status (GPI_NMI_STS_GPP_D)—Offset 1C4h	0h
1C8h	1CBh	NMI Status (GPI_NMI_STS_GPP_E)—Offset 1C8h	0h
1E0h	1E3h	NMI Enable (GPI_NMI_EN_GPP_C)—Offset 1E0h	0h
1E4h	1E7h	NMI Enable (GPI_NMI_EN_GPP_D)—Offset 1E4h	0h
1E8h	1EBh	NMI Enable (GPI_NMI_EN_GPP_E)—Offset 1E8h	0h
204h	207h	PWM Control (PWMC)—Offset 204h	0h
20Ch	20Fh	GPIO Serial Blink Enable (GP_SER_BLINK)—Offset 20Ch	0h
210h	213h	GPIO Serial Blink Command/Status (GP_SER_CMDSTS)—Offset 210h	0h
214h	217h	GPIO Serial Blink Data (GP_SER_DATA)—Offset 214h	0h
400h	403h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_0)—Offset 400h	44000X00h See register for X value
404h	407h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_0)—Offset 404h	48h
408h	40Bh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_1)—Offset 408h	44000X00h See register for X value
40Ch	40Fh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_1)—Offset 40Ch	See register
410h	413h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_2)—Offset 410h	44000X00h See register for X value
414h	417h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_2)—Offset 414h	See register
418h	41Bh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_3)—Offset 418h	44000X00h See register for X value

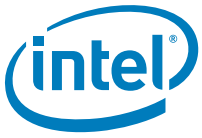


Table 29-2. Summary of GPIO Community 1 Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
41Ch	41Fh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_3)—Offset 41Ch	See register
420h	423h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_4)—Offset 420h	44000X00h See register for X value
424h	427h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_4)—Offset 424h	See register
428h	42Bh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_5)—Offset 428h	44000X00h See register for X value
42Ch	42Fh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_5)—Offset 42Ch	See register
430h	433h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_6)—Offset 430h	44000X00h See register for X value
434h	437h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_6)—Offset 434h	See register
438h	43Bh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_7)—Offset 438h	44000X00h See register for X value
43Ch	43Fh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_7)—Offset 43Ch	See register
440h	443h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_8)—Offset 440h	44000X00h See register for X value
444h	447h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_8)—Offset 444h	See register
448h	44Bh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_9)—Offset 448h	44000X00h See register for X value
44Ch	44Fh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_9)—Offset 44Ch	See register
450h	453h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_10)—Offset 450h	44000X00h See register for X value
454h	457h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_10)—Offset 454h	See register
458h	45Bh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_11)—Offset 458h	44000X00h See register for X value
45Ch	45Fh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_11)—Offset 45Ch	See register
460h	463h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_12)—Offset 460h	44000X00h See register for X value
464h	467h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_12)—Offset 464h	See register
468h	46Bh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_13)—Offset 468h	44000X00h See register for X value
46Ch	46Fh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_13)—Offset 46Ch	See register
470h	473h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_14)—Offset 470h	44000X00h See register for X value
474h	477h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_14)—Offset 474h	See register
478h	47Bh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_15)—Offset 478h	44000X00h See register for X value
47Ch	47Fh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_15)—Offset 47Ch	See register

Table 29-2. Summary of GPIO Community 1 Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
480h	483h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_16)—Offset 480h	44000X00h See register for X value
484h	487h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_16)—Offset 484h	See register
488h	48Bh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_17)—Offset 488h	44000X00h See register for X value
48Ch	48Fh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_17)—Offset 48Ch	See register
490h	493h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_18)—Offset 490h	44000X00h See register for X value
494h	497h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_18)—Offset 494h	See register
498h	49Bh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_19)—Offset 498h	44000X00h See register for X value
49Ch	49Fh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_19)—Offset 49Ch	See register
4A0h	4A3h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_20)—Offset 4A0h	44000X00h See register for X value
4A4h	4A7h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_20)—Offset 4A4h	See register
4A8h	4ABh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_21)—Offset 4A8h	44000X00h See register for X value
4ACh	4AFh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_21)—Offset 4ACh	See register
4B0h	4B3h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_22)—Offset 4B0h	44000X00h See register for X value
4B4h	4B7h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_22)—Offset 4B4h	See register
4B8h	4BBh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_23)—Offset 4B8h	44000X00h See register for X value
4BCh	4BFh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_23)—Offset 4BCh	See register
4C0h	4C3h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_0)—Offset 4C0h	44000X00h See register for X value
4C4h	4C7h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_0)—Offset 4C4h	See register
4C8h	4CBh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_1)—Offset 4C8h	44000X00h See register for X value
4CCh	4CFh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_1)—Offset 4CCh	See register
4D0h	4D3h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_2)—Offset 4D0h	44000X00h See register for X value
4D4h	4D7h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_2)—Offset 4D4h	See register
4D8h	4DBh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_3)—Offset 4D8h	44000X00h See register for X value
4DCh	4DFh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_3)—Offset 4DCh	See register
4E0h	4E3h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_4)—Offset 4E0h	44000X00h See register for X value

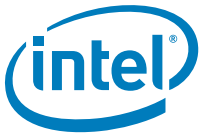


Table 29-2. Summary of GPIO Community 1 Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
4E4h	4E7h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_4)—Offset 4E4h	See register
4E8h	4EBh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_5)—Offset 4E8h	44000X00h See register for X value
4ECh	4EFh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_5)—Offset 4ECh	See register
4F0h	4F3h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_6)—Offset 4F0h	44000X00h See register for X value
4F4h	4F7h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_6)—Offset 4F4h	See register
4F8h	4FBh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_7)—Offset 4F8h	44000X00h See register for X value
4FCh	4FFh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_7)—Offset 4FCh	See register
500h	503h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_8)—Offset 500h	44000X00h See register for X value
504h	507h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_8)—Offset 504h	See register
508h	50Bh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_9)—Offset 508h	44000X00h See register for X value
50Ch	50Fh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_9)—Offset 50Ch	See register
510h	513h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_10)—Offset 510h	44000X00h See register for X value
514h	517h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_10)—Offset 514h	See register
518h	51Bh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_11)—Offset 518h	44000X00h See register for X value
51Ch	51Fh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_11)—Offset 51Ch	See register
520h	523h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_12)—Offset 520h	44000X00h See register for X value
524h	527h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_12)—Offset 524h	See register
528h	52Bh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_13)—Offset 528h	44000X00h See register for X value
52Ch	52Fh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_13)—Offset 52Ch	See register
530h	533h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_14)—Offset 530h	44000X00h See register for X value
534h	537h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_14)—Offset 534h	See register
538h	53Bh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_15)—Offset 538h	44000X00h See register for X value
53Ch	53Fh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_15)—Offset 53Ch	See register
540h	543h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_16)—Offset 540h	44000X00h See register for X value
544h	547h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_16)—Offset 544h	See register

Table 29-2. Summary of GPIO Community 1 Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
548h	54Bh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_17)—Offset 548h	44000X00h See register for X value
54Ch	54Fh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_17)—Offset 54Ch	See register
550h	553h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_18)—Offset 550h	44000X00h See register for X value
554h	557h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_18)—Offset 554h	See register
558h	55Bh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_19)—Offset 558h	44000X00h See register for X value
55Ch	55Fh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_19)—Offset 55Ch	See register
560h	563h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_20)—Offset 560h	44000X00h See register for X value
564h	567h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_20)—Offset 564h	See register
568h	56Bh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_21)—Offset 568h	44000X00h See register for X value
56Ch	56Fh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_21)—Offset 56Ch	See register
570h	573h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_22)—Offset 570h	44000X00h See register for X value
574h	577h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_22)—Offset 574h	See register
578h	57Bh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_23)—Offset 578h	44000X00h See register for X value
57Ch	57Fh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_23)—Offset 57Ch	See register
580h	583h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_0)—Offset 580h	44000X00h See register for X value
584h	587h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_0)—Offset 584h	See register
588h	58Bh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_1)—Offset 588h	44000X00h See register for X value
58Ch	58Fh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_1)—Offset 58Ch	See register
590h	593h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_2)—Offset 590h	44000X00h See register for X value
594h	597h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_2)—Offset 594h	See register
598h	59Bh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_3)—Offset 598h	44000X00h See register for X value
59Ch	59Fh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_3)—Offset 59Ch	See register
5A0h	5A3h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_4)—Offset 5A0h	44000X00h See register for X value
5A4h	5A7h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_4)—Offset 5A4h	See register
5A8h	5ABh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_5)—Offset 5A8h	44000X00h See register for X value

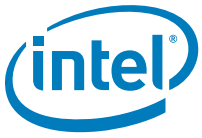


Table 29-2. Summary of GPIO Community 1 Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
5ACh	5AFh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_5)—Offset 5ACh	See register
5B0h	5B3h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_6)—Offset 5B0h	44000X00h See register for X value
5B4h	5B7h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_6)—Offset 5B4h	See register
5B8h	5BBh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_7)—Offset 5B8h	44000X00h See register for X value
5BCh	5BFh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_7)—Offset 5BCh	See register
5C0h	5C3h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_8)—Offset 5C0h	44000X00h See register for X value
5C4h	5C7h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_8)—Offset 5C4h	See register
5C8h	5CBh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_9)—Offset 5C8h	44000X00h See register for X value
5CCh	5CFh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_9)—Offset 5CCh	See register
5D0h	5D3h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_10)—Offset 5D0h	44000X00h See register for X value
5D4h	5D7h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_10)—Offset 5D4h	See register
5D8h	5DBh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_11)—Offset 5D8h	44000X00h See register for X value
5DCh	5DFh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_11)—Offset 5DCh	See register
5E0h	5E3h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_12)—Offset 5E0h	44000X00h See register for X value
5E4h	5E7h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_12)—Offset 5E4h	See register
5E8h	5EBh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_13)—Offset 5E8h	44000X00h See register for X value
5ECh	5EFh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_13)—Offset 5ECh	See register
5F0h	5F3h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_14)—Offset 5F0h	44000X00h See register for X value
5F4h	5F7h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_14)—Offset 5F4h	See register
5F8h	5FBh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_15)—Offset 5F8h	44000X00h See register for X value
5FCh	5FFh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_15)—Offset 5FCh	See register
600h	603h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_16)—Offset 600h	44000X00h See register for X value
604h	607h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_16)—Offset 604h	See register
608h	60Bh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_17)—Offset 608h	44000X00h See register for X value
60Ch	60Fh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_17)—Offset 60Ch	See register

Table 29-2. Summary of GPIO Community 1 Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
610h	613h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_18)—Offset 610h	44000X00h See register for X value
614h	617h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_18)—Offset 614h	See register
618h	61Bh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_19)—Offset 618h	44000X00h See register for X value
61Ch	61Fh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_19)—Offset 61Ch	See register
620h	623h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_20)—Offset 620h	44000X00h See register for X value
624h	627h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_20)—Offset 624h	See register
628h	62Bh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_21)—Offset 628h	44000X00h See register for X value
62Ch	62Fh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_21)—Offset 62Ch	See register
630h	633h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_22)—Offset 630h	44000X00h See register for X value
634h	637h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_22)—Offset 634h	See register
638h	63Bh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_23)—Offset 638h	44000X00h See register for X value
63Ch	63Fh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_23)—Offset 63Ch	See register

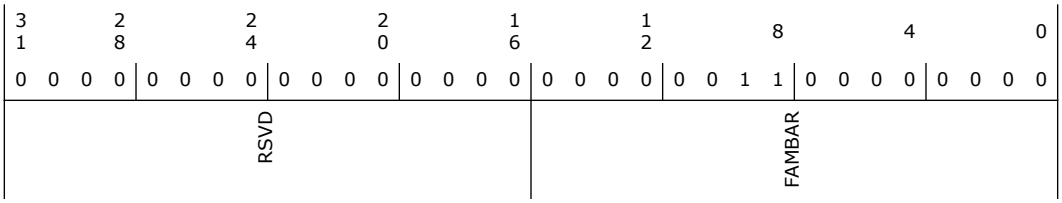
29.2.1 Family Base Address (FAMBAR)—Offset 8h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 300h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	300h RO	**Family Base Address (FAMBAR):** This field provides the starting byte-align address of Family0 register sets. It is meant for software to discover from where the very first Family register (i.e. Family0 register) starts to compute the next Families address offsets.

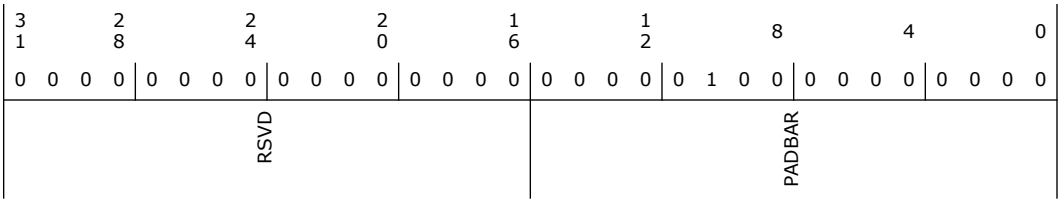
29.2.2 Pad Base Address (PADBAR)—Offset Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 400h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	400h RO	**Pad Base Address (PADBAR):** Pad Base Address (PADBAR) This field provides the starting byte-align address of Pad0 register sets within a Community. It is meant for software to discover from where the very first Pad register (i.e. Pad0 register) starts to compute the next Pad address offsets.

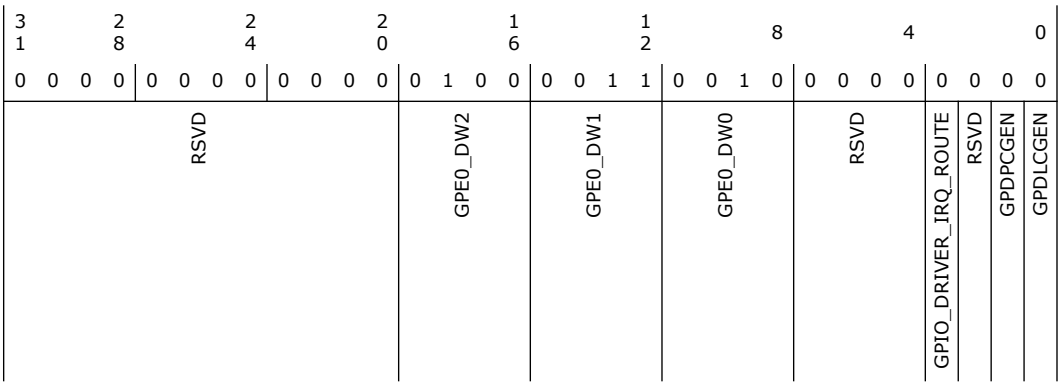
29.2.3 Miscellaneous Configuration (MISCCFG)—Offset 10h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 43200h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	Reserved.
19:16	4h RW	**GPIO Group to GPE_DW0 assignment encoding (GPE0_DW2):** This register assigns a specific GPIO Group to the ACPI GPE0[95:64]. The selected GPIO group will be mapped to lower bits of the GPE register 0h = GPP_A[23:0] mapped to GPE[87:64]; GPE[95:88] not used. 1h = GPP_B[23:0] mapped to GPE[87:64]; GPE[95:88] not used. 2h = GPP_C[23:0] mapped to GPE[87:64]; GPE[95:88] not used. 3h = GPP_D[23:0] mapped to GPE[87:64]; GPE[95:88] not used. 4h = GPP_E[23:0] mapped to GPE[87:64]; GPE[95:88] not used. 5h = GPP_F[23:0] mapped to GPE[87:64]; GPE[95:88] not used. 6h = GPP_G[7:0] mapped to GPE[51:64]; GPE[95:52] not used. 7h = GPD[11:0] mapped to GPE[75:64]; GPE[95:76] not used.
15:12	3h RW	**GPIO Group to GPE_DW0 assignment encoding (GPE0_DW1):** This register assigns a specific GPIO Group to the ACPI GPE0[63:32]. The selected GPIO group will be mapped to lower bits of the GPE register 0h = GPP_A[23:0] mapped to GPE[55:32]; GPE[63:56] not used. 1h = GPP_B[23:0] mapped to GPE[55:32]; GPE[63:56] not used. 2h = GPP_C[23:0] mapped to GPE[55:32]; GPE[63:56] not used. 3h = GPP_D[23:0] mapped to GPE[55:32]; GPE[63:56] not used. 4h = GPP_E[23:0] mapped to GPE[55:32]; GPE[63:56] not used. 5h = GPP_F[23:0] mapped to GPE[55:32]; GPE[63:56] not used. 6h = GPP_G[7:0] mapped to GPE[39:32]; GPE[63:40] not used. 7h = GPD[11:0] mapped to GPE[43:32]; GPE[63:44] not used.
11:8	2h RW	**GPIO Group to GPE_DW0 assignment encoding (GPE0_DW0):** This register assigns a specific GPIO Group to the ACPI GPE0[31:0]. The selected GPIO group will be mapped to lower bits of the GPE register 0h = GPP_A[23:0] mapped to GPE[23:0]; GPE[31:24] not used. 1h = GPP_B[23:0] mapped to GPE[23:0]; GPE[31:24] not used. 2h = GPP_C[23:0] mapped to GPE[23:0]; GPE[31:24] not used. 3h = GPP_D[23:0] mapped to GPE[23:0]; GPE[31:24] not used. 4h = GPP_E[23:0] mapped to GPE[23:0]; GPE[31:24] not used. 5h = GPP_F[23:0] mapped to GPE[23:0]; GPE[31:24] not used. 6h = GPP_G[7:0] mapped to GPE[7:0]; GPE[31:8] not used. 7h = GPD[11:0] mapped to GPE[11:0]; GPE[31:12] not used.
7:4	0h RO	Reserved.
3	0h RW	**GPIO Driver IRQ Route (GPIO_DRIVER_IRQ_ROUTE):** GPIO Driver IRQ_ROUTE[1:0]: Specifies the APIC IRQ globally for all pads within the current community (GPI_IS with corresponding GPI_IE enable). 0 = IRQ14 1 = IRQ15
2	0h RO	Reserved.
1	0h RW	**GPIO Dynamic Partition Clock Gating Enable (GPDPCGEN):** Specifies whether the GPIO Community should take part in partition clock gating 0 = Disable participation in dynamic partition clock gating 1 = Enable participation in dynamic partition clock gating
0	0h RW	**GPIO Dynamic Local Clock Gating Enable (GPDLCGEN):** Specifies whether the GPIO Community should perform local clock gating. 0 = Disable dynamic local clock gating 1 = Enable dynamic local clock gating

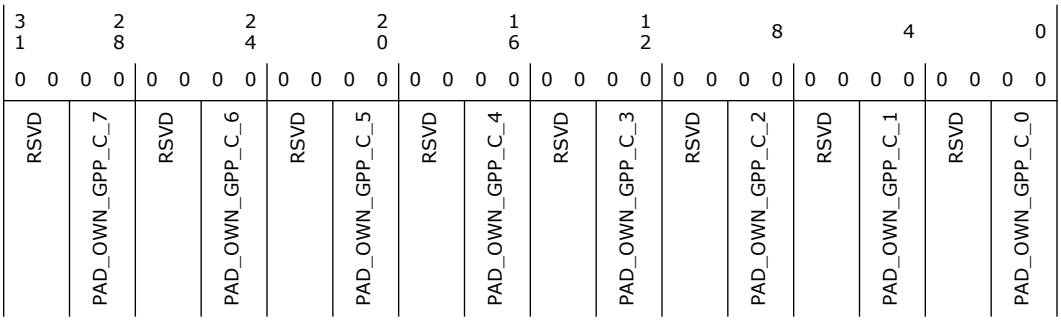
29.2.4 Pad Ownership (PAD_OWN_GPP_C_0)—Offset 20h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29:28	0h RO	**Pad Ownership (PAD_OWN_GPP_C_7):** Same description as bit 0, except that the bit field applies to GPP_C7.
27:26	0h RO	Reserved.
25:24	0h RO	**Pad Ownership (PAD_OWN_GPP_C_6):** Same description as bit 0, except that the bit field applies to GPP_C6.
23:22	0h RO	Reserved.
21:20	0h RO	**Pad Ownership (PAD_OWN_GPP_C_5):** Same description as bit 0, except that the bit field applies to GPP_C5.
19:18	0h RO	Reserved.
17:16	0h RO	**Pad Ownership (PAD_OWN_GPP_C_4):** Same description as bit 0, except that the bit field applies to GPP_C4.
15:14	0h RO	Reserved.
13:12	0h RO	**Pad Ownership (PAD_OWN_GPP_C_3):** Same description as bit 0, except that the bit field applies to GPP_C3.
11:10	0h RO	Reserved.
9:8	0h RO	**Pad Ownership (PAD_OWN_GPP_C_2):** Same description as bit 0, except that the bit field applies to GPP_C2.
7:6	0h RO	Reserved.
5:4	0h RO	**Pad Ownership (PAD_OWN_GPP_C_1):** Same description as bit 0, except that the bit field applies to GPP_C1.
3:2	0h RO	Reserved.
1:0	0h RO	**Pad Ownership (PAD_OWN_GPP_C_0):** 00 = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. 01 = ME GPIO Mode. ME has ownership of the pad. 10 = ISH GPIO Mode.ME has ownership of the pad 11 = Reserved

29.2.5 Pad Ownership (PAD_OWN_GPP_C_1)—Offset 24h

Same description as PAD_OWN_GPP_C_0, except that this register is for GPP_C[15:8]

29.2.6 Pad Ownership (PAD_OWN_GPP_C_2)—Offset 28h

Same description as PAD_OWN_GPP_C_0, except that this register is for GPP_C[23:16]

29.2.7 Pad Ownership (PAD_OWN_GPP_D_0)—Offset 30h

Same description as PAD_OWN_GPP_C_0, except that this register is for GPP_D[7:0]

29.2.8 Pad Ownership (PAD_OWN_GPP_D_1)—Offset 34h

Same description as PAD_OWN_GPP_C_0, except that this register is for GPP_D[15:8]

29.2.9 Pad Ownership (PAD_OWN_GPP_D_2)—Offset 38h

Same description as PAD_OWN_GPP_C_0, except that this register is for GPP_D[23:16]

29.2.10 Pad Ownership (PAD_OWN_GPP_E_0)—Offset 40h

Same description as PAD_OWN_GPP_C_0, except that this register is for GPP_E[7:0]

29.2.11 Pad Ownership (PAD_OWN_GPP_E_1)—Offset 44h

Same description as PAD_OWN_GPP_C_0, except that this register is for GPP_E[15:8]

29.2.12 Pad Ownership (PAD_OWN_GPP_E_2)—Offset 48h

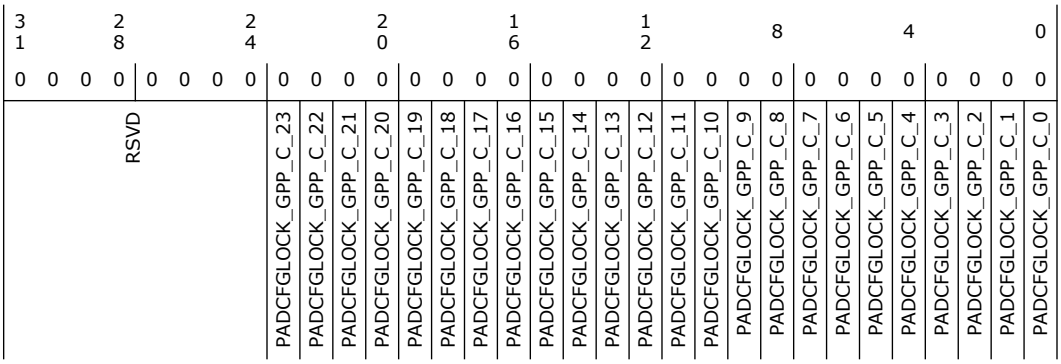
Same description as PAD_OWN_GPP_C_0, except that this register is for GPP_E[23:16]

29.2.13 Pad Configuration Lock (PADCFGLOCK_GPP_C)—Offset A0h

Access Method

Type: MSG Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_C_23):** Applied to GPP_C23. Same description as bit 0.
22	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_C_22):** Applied to GPP_C22. Same description as bit 0.
21	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_C_21):** Applied to GPP_C21. Same description as bit 0.
20	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_C_20):** Applied to GPP_C20. Same description as bit 0.
19	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_C_19):** Applied to GPP_C19. Same description as bit 0.
18	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_C_18):** Applied to GPP_C18. Same description as bit 0.
17	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_C_17):** Applied to GPP_C17. Same description as bit 0.
16	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_C_16):** Applied to GPP_C16. Same description as bit 0.
15	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_C_15):** Applied to GPP_C15. Same description as bit 0.
14	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_C_14):** Applied to GPP_C14. Same description as bit 0.
13	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_C_13):** Applied to GPP_C13. Same description as bit 0.
12	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_C_12):** Applied to GPP_C12. Same description as bit 0.
11	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_C_11):** Applied to GPP_C11. Same description as bit 0.
10	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_C_10):** Applied to GPP_C10. Same description as bit 0.
9	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_C_9):** Applied to GPP_C9. Same description as bit 0.
8	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_C_8):** Applied to GPP_C8. Same description as bit 0.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_C_7):** Applied to GPP_C7. Same description as bit 0.
6	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_C_6):** Applied to GPP_C6. Same description as bit 0.
5	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_C_5):** Applied to GPP_C5. Same description as bit 0.
4	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_C_4):** Applied to GPP_C4. Same description as bit 0.
3	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_C_3):** Applied to GPP_C3. Same description as bit 0.
2	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_C_2):** Applied to GPP_C2. Same description as bit 0.
1	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_C_1):** Applied to GPP_C1. Same description as bit 0.
0	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_C_0):** Pad Configuration Lock locks specific register fields in the GPP specific registers from being configured. The registers affected become Read-Only and software writes to these registers have no effect. 0 = Unlock 1 = Lock the following register fields as read-only (RO): - Pad Configuration registers (exclude GPIOTXState) - GPI_NMI_EN Register (if implemented) - GPI_SMI_EN Register (if implemented) - GPI_GPE_EN Register (if implemented) When PadCfgLock is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown.

29.2.14 Pad Configuration Lock (PADCFGLOCKTX_GPP_C)—Offset A4h

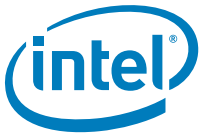
Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD								PADCFGLOCKTX_GPP_C_23	PADCFGLOCKTX_GPP_C_22	PADCFGLOCKTX_GPP_C_21	PADCFGLOCKTX_GPP_C_20	PADCFGLOCKTX_GPP_C_19	PADCFGLOCKTX_GPP_C_18	PADCFGLOCKTX_GPP_C_17	PADCFGLOCKTX_GPP_C_16	PADCFGLOCKTX_GPP_C_15	PADCFGLOCKTX_GPP_C_14	PADCFGLOCKTX_GPP_C_13	PADCFGLOCKTX_GPP_C_12	PADCFGLOCKTX_GPP_C_11	PADCFGLOCKTX_GPP_C_10	PADCFGLOCKTX_GPP_C_9	PADCFGLOCKTX_GPP_C_8	PADCFGLOCKTX_GPP_C_7	PADCFGLOCKTX_GPP_C_6	PADCFGLOCKTX_GPP_C_5	PADCFGLOCKTX_GPP_C_4	PADCFGLOCKTX_GPP_C_3	PADCFGLOCKTX_GPP_C_2	PADCFGLOCKTX_GPP_C_1	PADCFGLOCKTX_GPP_C_0



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_C_23):** Applied to GPP_C23. Same description as bit 0.
22	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_C_22):** Applied to GPP_C22. Same description as bit 0.
21	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_C_21):** Applied to GPP_C21. Same description as bit 0.
20	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_C_20):** Applied to GPP_C20. Same description as bit 0.
19	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_C_19):** Applied to GPP_C19. Same description as bit 0.
18	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_C_18):** Applied to GPP_C18. Same description as bit 0.
17	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_C_17):** Applied to GPP_C17. Same description as bit 0.
16	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_C_16):** Applied to GPP_C16. Same description as bit 0.
15	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_C_15):** Applied to GPP_C15. Same description as bit 0.
14	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_C_14):** Applied to GPP_C14. Same description as bit 0.
13	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_C_13):** Applied to GPP_C13. Same description as bit 0.
12	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_C_12):** Applied to GPP_C12. Same description as bit 0.
11	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_C_11):** Applied to GPP_C11. Same description as bit 0.
10	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_C_10):** Applied to GPP_C10. Same description as bit 0.
9	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_C_9):** Applied to GPP_C9. Same description as bit 0.
8	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_C_8):** Applied to GPP_C8. Same description as bit 0.
7	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_C_7):** Applied to GPP_C7. Same description as bit 0.
6	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_C_6):** Applied to GPP_C6. Same description as bit 0.
5	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_C_5):** Applied to GPP_C5. Same description as bit 0.
4	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_C_4):** Applied to GPP_C4. Same description as bit 0.
3	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_C_3):** Applied to GPP_C3. Same description as bit 0.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_C_2):** Applied to GPP_C2. Same description as bit 0.
1	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_C_1):** Applied to GPP_C1. Same description as bit 0.
0	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_C_0):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) When PadCfgLockTx is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown.

29.2.15 Pad Configuration Lock (PADCFGLOCK_GPP_D)—Offset A8h

Same description as PADCFGLOCK_GPP_C register, except that this is for GPP_D.

29.2.16 Pad Configuration Lock (PADCFGLOCKTX_GPP_D)—Offset ACh

Same description as PADCFGLOCKTX_GPP_C, except this register is for GPP_D

29.2.17 Pad Configuration Lock (PADCFGLOCK_GPP_E)—Offset B0h

Same description as PADCFGLOCK_GPP_C, except that this register is for GPP_E

29.2.18 Pad Configuration Lock (PADCFGLOCKTX_GPP_E)—Offset B4h

Same description as PADCFGLOCKTX_GPP_C, except that this register is for GPP_E

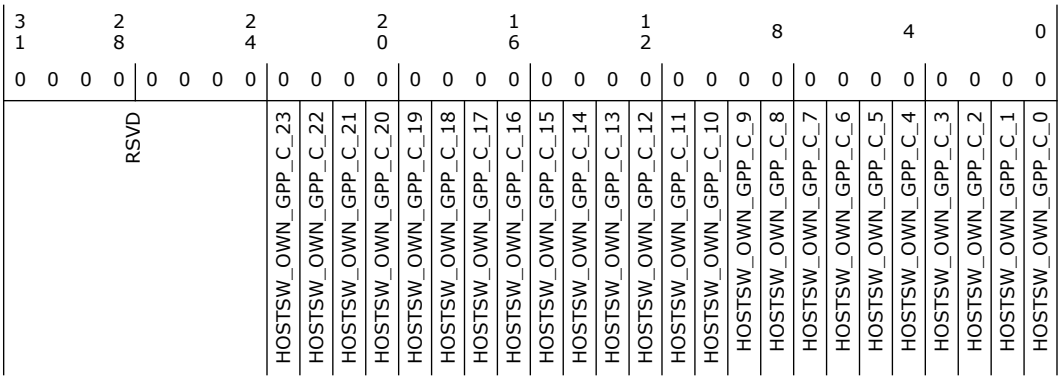
29.2.19 Host Software Pad Ownership (HOSTSW_OWN_GPP_C)—Offset D0h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_C_23):** Applied to GPP_C23. Same description as bit 0.
22	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_C_22):** Applied to GPP_C22. Same description as bit 0.
21	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_C_21):** Applied to GPP_C21. Same description as bit 0.
20	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_C_20):** Applied to GPP_C20. Same description as bit 0.
19	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_C_19):** Applied to GPP_C19. Same description as bit 0.
18	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_C_18):** Applied to GPP_C18. Same description as bit 0.
17	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_C_17):** Applied to GPP_C17. Same description as bit 0.
16	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_C_16):** Applied to GPP_C16. Same description as bit 0.
15	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_C_15):** Applied to GPP_C15. Same description as bit 0.
14	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_C_14):** Applied to GPP_C14. Same description as bit 0.
13	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_C_13):** Applied to GPP_C13. Same description as bit 0.
12	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_C_12):** Applied to GPP_C12. Same description as bit 0.
11	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_C_11):** Applied to GPP_C11. Same description as bit 0.
10	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_C_10):** Applied to GPP_C10. Same description as bit 0.
9	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_C_9):** Applied to GPP_C9. Same description as bit 0.
8	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_C_8):** Applied to GPP_C8. Same description as bit 0.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_C_7):** Applied to GPP_C7. Same description as bit 0.
6	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_C_6):** Applied to GPP_C6. Same description as bit 0.
5	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_C_5):** Applied to GPP_C5. Same description as bit 0.
4	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_C_4):** Applied to GPP_C4. Same description as bit 0.
3	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_C_3):** Applied to GPP_C3. Same description as bit 0.
2	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_C_2):** Applied to GPP_C2. Same description as bit 0.
1	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_C_1):** Applied to GPP_C1. Same description as bit 0.
0	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_C_0):** This register determines the appropriate host status bit update when a pad is under host ownership. 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked.

29.2.20 Host Software Pad Ownership (HOSTSW_OWN_GPP_D)—Offset D4h

Same description as HOSTSW_OWN_GPP_C register, except that the register is for GPP_D.

29.2.21 Host Software Pad Ownership (HOSTSW_OWN_GPP_E)—Offset D8h

Same description as HOSTSW_OWN_GPP_C register, except that the register is for GPP_E.

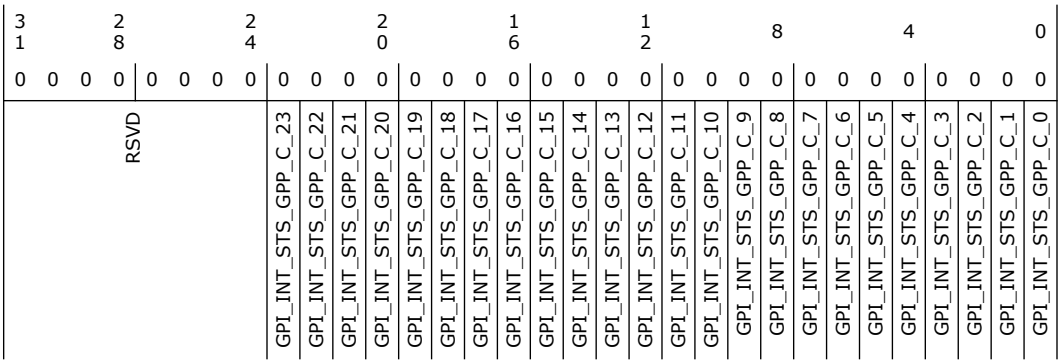
29.2.22 GPI Interrupt Status (GPI_IS_GPP_C)—Offset 100h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_C_23):** Applied to GPP_C23. Same description as bit 0.
22	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_C_22):** Applied to GPP_C22. Same description as bit 0.
21	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_C_21):** Applied to GPP_C21. Same description as bit 0.
20	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_C_20):** Applied to GPP_C20. Same description as bit 0.
19	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_C_19):** Applied to GPP_C19. Same description as bit 0.
18	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_C_18):** Applied to GPP_C18. Same description as bit 0.
17	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_C_17):** Applied to GPP_C17. Same description as bit 0.
16	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_C_16):** Applied to GPP_C16. Same description as bit 0.
15	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_C_15):** Applied to GPP_C15. Same description as bit 0.
14	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_C_14):** Applied to GPP_C14. Same description as bit 0.
13	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_C_13):** Applied to GPP_C13. Same description as bit 0.
12	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_C_12):** Applied to GPP_C12. Same description as bit 0.
11	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_C_11):** Applied to GPP_C11. Same description as bit 0.
10	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_C_10):** Applied to GPP_C10. Same description as bit 0.
9	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_C_9):** Applied to GPP_C9. Same description as bit 0.
8	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_C_8):** Applied to GPP_C8. Same description as bit 0.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_C_7):** Applied to GPP_C7. Same description as bit 0.
6	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_C_6):** Applied to GPP_C6. Same description as bit 0.
5	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_C_5):** Applied to GPP_C5. Same description as bit 0.
4	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_C_4):** Applied to GPP_C4. Same description as bit 0.
3	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_C_3):** Applied to GPP_C3. Same description as bit 0.
2	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_C_2):** Applied to GPP_C2. Same description as bit 0.
1	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_C_1):** Applied to GPP_C1. Same description as bit 0.
0	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_C_0):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: - The corresponding pad is used in GPIO input mode - HOSTSW_OWN = 1 (i.e. Host GPIO Driver Mode). Writing a value of 1 will clear the bit while writing a value of 0 has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN does not prevent the setting of GPI_INT_STS.

29.2.23 GPI Interrupt Status (GPI_IS_GPP_D)—Offset 104h

Same description as GPI_IS_GPP_C register, except that the register is for GPP_D

29.2.24 GPI Interrupt Status (GPI_IS_GPP_E)—Offset 108h

Same description as GPI_IS_GPP_C, except that the register is for GPP_E

29.2.25 GPI Interrupt Enable (GPI_IE_GPP_C)—Offset 120h

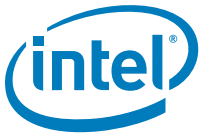
Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD								GPI_INT_EN_GPP_C_23	GPI_INT_EN_GPP_C_22	GPI_INT_EN_GPP_C_21	GPI_INT_EN_GPP_C_20	GPI_INT_EN_GPP_C_19	GPI_INT_EN_GPP_C_18	GPI_INT_EN_GPP_C_17	GPI_INT_EN_GPP_C_16	GPI_INT_EN_GPP_C_15	GPI_INT_EN_GPP_C_14	GPI_INT_EN_GPP_C_13	GPI_INT_EN_GPP_C_12	GPI_INT_EN_GPP_C_11	GPI_INT_EN_GPP_C_10	GPI_INT_EN_GPP_C_9	GPI_INT_EN_GPP_C_8	GPI_INT_EN_GPP_C_7	GPI_INT_EN_GPP_C_6	GPI_INT_EN_GPP_C_5	GPI_INT_EN_GPP_C_4	GPI_INT_EN_GPP_C_3	GPI_INT_EN_GPP_C_2	GPI_INT_EN_GPP_C_1	GPI_INT_EN_GPP_C_0



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_C_23):** Applied to GPP_C23. Same description as bit 0.
22	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_C_22):** Applied to GPP_C22. Same description as bit 0.
21	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_C_21):** Applied to GPP_C21. Same description as bit 0.
20	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_C_20):** Applied to GPP_C20. Same description as bit 0.
19	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_C_19):** Applied to GPP_C19. Same description as bit 0.
18	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_C_18):** Applied to GPP_C18. Same description as bit 0.
17	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_C_17):** Applied to GPP_C17. Same description as bit 0.
16	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_C_16):** Applied to GPP_C16. Same description as bit 0.
15	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_C_15):** Applied to GPP_C15. Same description as bit 0.
14	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_C_14):** Applied to GPP_C14. Same description as bit 0.
13	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_C_13):** Applied to GPP_C13. Same description as bit 0.
12	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_C_12):** Applied to GPP_C12. Same description as bit 0.
11	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_C_11):** Applied to GPP_C11. Same description as bit 0.
10	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_C_10):** Applied to GPP_C10. Same description as bit 0.
9	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_C_9):** Applied to GPP_C9. Same description as bit 0.
8	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_C_8):** Applied to GPP_C8. Same description as bit 0.
7	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_C_7):** Applied to GPP_C7. Same description as bit 0.
6	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_C_6):** Applied to GPP_C6. Same description as bit 0.
5	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_C_5):** Applied to GPP_C5. Same description as bit 0.
4	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_C_4):** Applied to GPP_C4. Same description as bit 0.
3	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_C_3):** Applied to GPP_C3. Same description as bit 0.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_C_2):** Applied to GPP_C2. Same description as bit 0.
1	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_C_1):** Applied to GPP_C1. Same description as bit 0.
0	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_C_0):** This bit is used to enable/ disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing.

29.2.26 GPI Interrupt Enable (GPI_IE_GPP_D)—Offset 124h

Same description as GPI_IE_GPP_C, except that this register is for GPP_D

29.2.27 GPI Interrupt Enable (GPI_IE_GPP_E)—Offset 128h

Same description as GPI_IE_GPP_C, except that this register is for GPP_E.

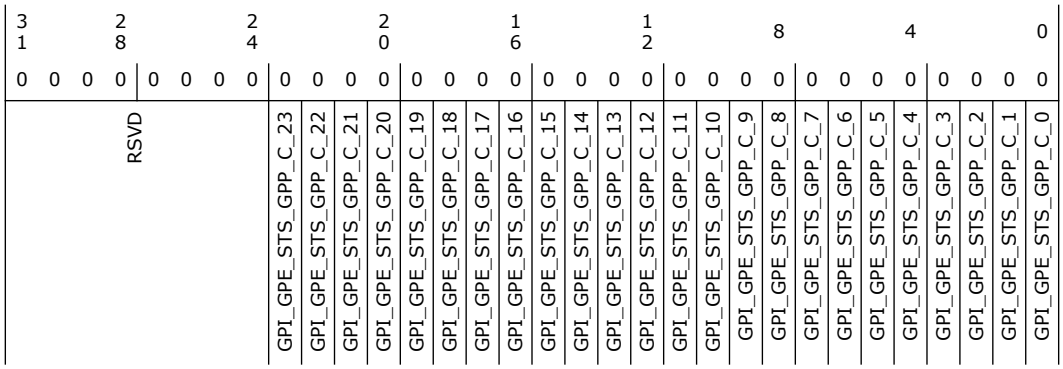
29.2.28 GPI General Purpose Events Status (GPI_GPE_STS_GPP_C)—Offset 140h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_C_23):** Applied to GPP_C23. Same description as bit 0.
22	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_C_22):** Applied to GPP_C22. Same description as bit 0.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_C_21):** Applied to GPP_C21. Same description as bit 0.
20	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_C_20):** Applied to GPP_C20. Same description as bit 0.
19	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_C_19):** Applied to GPP_C19. Same description as bit 0.
18	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_C_18):** Applied to GPP_C18. Same description as bit 0.
17	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_C_17):** Applied to GPP_C17. Same description as bit 0.
16	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_C_16):** Applied to GPP_C16. Same description as bit 0.
15	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_C_15):** Applied to GPP_C15. Same description as bit 0.
14	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_C_14):** Applied to GPP_C14. Same description as bit 0.
13	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_C_13):** Applied to GPP_C13. Same description as bit 0.
12	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_C_12):** Applied to GPP_C12. Same description as bit 0.
11	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_C_11):** Applied to GPP_C11. Same description as bit 0.
10	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_C_10):** Applied to GPP_C10. Same description as bit 0.
9	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_C_9):** Applied to GPP_C9. Same description as bit 0.
8	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_C_8):** Applied to GPP_C8. Same description as bit 0.
7	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_C_7):** Applied to GPP_C7. Same description as bit 0.
6	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_C_6):** Applied to GPP_C6. Same description as bit 0.
5	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_C_5):** Applied to GPP_C5. Same description as bit 0.
4	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_C_4):** Applied to GPP_C4. Same description as bit 0.
3	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_C_3):** Applied to GPP_C3. Same description as bit 0.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_C_2):** Applied to GPP_C2. Same description as bit 0.
1	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_C_1):** Applied to GPP_C1. Same description as bit 0.
0	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_C_0):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high(or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS bit is set: - If the system is in an S3-S5 state, the event will also wake the system. - If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN does not prevent the setting of GPI_GPE_STS.

29.2.29 GPI General Purpose Events Status (GPI_GPE_STS_GPP_D)—Offset 144h

Same description as GPI_GPE_STS_GPP_C, except that this register is for GPP_D.

29.2.30 GPI General Purpose Events Status (GPI_GPE_STS_GPP_E)—Offset 148h

Same description as GPI_GPE_STS_GPP_C, except that this register is for GPP_E.

29.2.31 GPI General Purpose Events Enable (GPI_GPE_EN_GPP_C)—Offset 160h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
RSVD		GPI_GPE_EN_GPP_C_23	GPI_GPE_EN_GPP_C_22	GPI_GPE_EN_GPP_C_21	GPI_GPE_EN_GPP_C_20	GPI_GPE_EN_GPP_C_19	GPI_GPE_EN_GPP_C_18	GPI_GPE_EN_GPP_C_17	GPI_GPE_EN_GPP_C_16	GPI_GPE_EN_GPP_C_15	GPI_GPE_EN_GPP_C_14	GPI_GPE_EN_GPP_C_13	GPI_GPE_EN_GPP_C_12	GPI_GPE_EN_GPP_C_11	GPI_GPE_EN_GPP_C_10	GPI_GPE_EN_GPP_C_9	GPI_GPE_EN_GPP_C_8	GPI_GPE_EN_GPP_C_7	GPI_GPE_EN_GPP_C_6	GPI_GPE_EN_GPP_C_5	GPI_GPE_EN_GPP_C_4	GPI_GPE_EN_GPP_C_3	GPI_GPE_EN_GPP_C_2	GPI_GPE_EN_GPP_C_1	GPI_GPE_EN_GPP_C_0

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_C_23):** Applied to GPP_C23. Same description as bit 0.
22	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_C_22):** Applied to GPP_C22. Same description as bit 0.
21	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_C_21):** Applied to GPP_C21. Same description as bit 0.
20	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_C_20):** Applied to GPP_C20. Same description as bit 0.
19	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_C_19):** Applied to GPP_C19. Same description as bit 0.
18	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_C_18):** Applied to GPP_C18. Same description as bit 0.
17	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_C_17):** Applied to GPP_C17. Same description as bit 0.
16	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_C_16):** Applied to GPP_C16. Same description as bit 0.
15	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_C_15):** Applied to GPP_C15. Same description as bit 0.
14	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_C_14):** Applied to GPP_C14. Same description as bit 0.
13	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_C_13):** Applied to GPP_C13. Same description as bit 0.
12	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_C_12):** Applied to GPP_C12. Same description as bit 0.
11	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_C_11):** Applied to GPP_C11. Same description as bit 0.
10	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_C_10):** Applied to GPP_C10. Same description as bit 0.
9	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_C_9):** Applied to GPP_C9. Same description as bit 0.
8	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_C_8):** Applied to GPP_C8. Same description as bit 0.
7	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_C_7):** Applied to GPP_C7. Same description as bit 0.
6	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_C_6):** Applied to GPP_C6. Same description as bit 0.
5	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_C_5):** Applied to GPP_C5. Same description as bit 0.
4	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_C_4):** Applied to GPP_C4. Same description as bit 0.
3	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_C_3):** Applied to GPP_C3. Same description as bit 0.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_C_2):** Applied to GPP_C2. Same description as bit 0.
1	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_C_1):** Applied to GPP_C1. Same description as bit 0.
0	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_C_0):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'.

29.2.32 GPI General Purpose Events Enable (GPI_GPE_EN_GPP_D)—Offset 164h

Same description as GPI_GPE_EN_GPP_C, except that the register is for GPP_D.

29.2.33 GPI General Purpose Events Enable (GPI_GPE_EN_GPP_E)—Offset 168h

Same description as GPI_GPE_EN_GPP_C, except that the register is for GPP_E.

29.2.34 SMI Status (GPI_SMI_STS_GPP_C)—Offset 180h

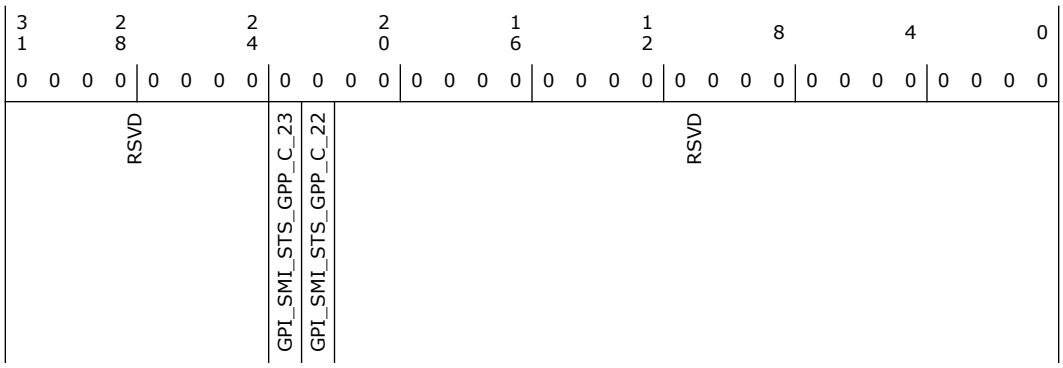
Register bits in this register are implemented for GPP_C signals that have SMI capability only. Other bits are reserved and RO.

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RW1C	**GPI SMI Status (GPI_SMI_STS_GPP_C_23):** Same description as bit 22.
22	0h RW1C	**GPI SMI Status (GPI_SMI_STS_GPP_C_22):** This bit is set to 1 by hardware when a level event (See RxEdCfg,RxInv) is detected, and all the following conditions are true: - The corresponding pad is used in GPIO input mode - The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of 1 will clear the bit while writing a value of 0 has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN does not prevent the setting of GPI_SMI_STS.
21:0	0h RO	Reserved.

29.2.35 SMI Status (GPI_SMI_STS_GPP_D)—Offset 184h

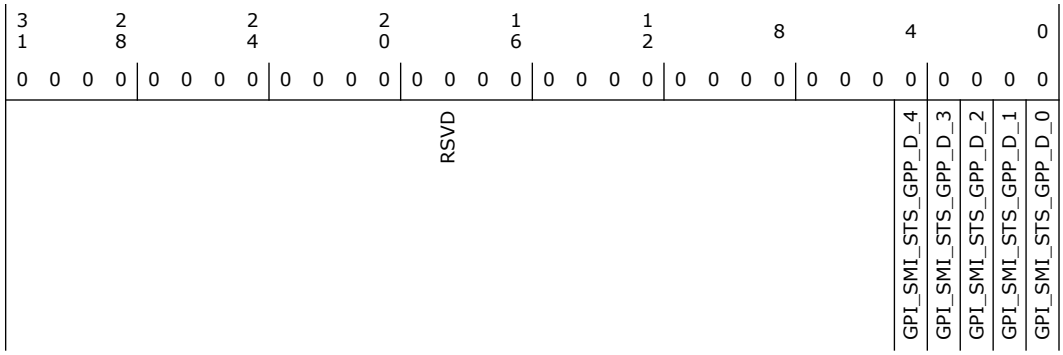
Register bits in this register are implemented for GPP_D signals that have SMI capability only. Other bits are reserved and RO.

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4	0h RW1C	**GPI SMI Status (GPI_SMI_STS_GPP_D_4):** Same description as bit 0.
3	0h RW1C	**GPI SMI Status (GPI_SMI_STS_GPP_D_3):** Same description as bit 0.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW1C	**GPI SMI Status (GPI_SMI_STS_GPP_D_2):** Same description as bit 0.
1	0h RW1C	**GPI SMI Status (GPI_SMI_STS_GPP_D_1):** Same description as bit 0.
0	0h RW1C	**GPI SMI Status (GPI_SMI_STS_GPP_D_0):** This bit is set to 1 by hardware when a level event (See RxEdCfg,RxInv) is detected, and all the following conditions are true: - The corresponding pad is used in GPIO input mode - The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of 1 will clear the bit while writing a value of 0 has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN does not prevent the setting of GPI_SMI_STS.

29.2.36 SMI Status (GPI_SMI_STS_GPP_E)—Offset 188h

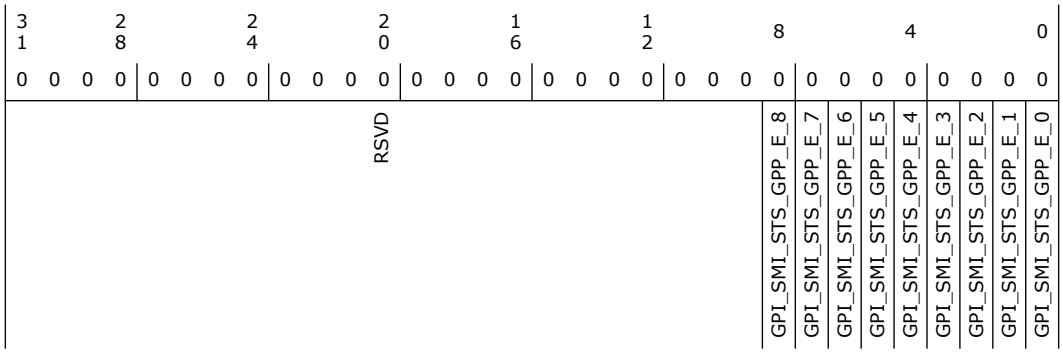
Register bits in this register are implemented for GPP_E signals that have SMI capability only. Other bits are reserved and RO.

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h RW1C	**GPI SMI Status (GPI_SMI_STS_GPP_E_8):** Same description as bit 0.
7	0h RW1C	**GPI SMI Status (GPI_SMI_STS_GPP_E_7):** Same description as bit 0.
6	0h RW1C	**GPI SMI Status (GPI_SMI_STS_GPP_E_6):** Same description as bit 0.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW1C	**GPI SMI Status (GPI_SMI_STS_GPP_E_5):** Same description as bit 0.
4	0h RW1C	**GPI SMI Status (GPI_SMI_STS_GPP_E_4):** Same description as bit 0.
3	0h RW1C	**GPI SMI Status (GPI_SMI_STS_GPP_E_3):** Same description as bit 0.
2	0h RW1C	**GPI SMI Status (GPI_SMI_STS_GPP_E_2):** Same description as bit 0.
1	0h RW1C	**GPI SMI Status (GPI_SMI_STS_GPP_E_1):** Same description as bit 0.
0	0h RW1C	**GPI SMI Status (GPI_SMI_STS_GPP_E_0):** This bit is set to 1 by hardware when a level event (See RxEdCfg,RxInv) is detected, and all the following conditions are true: - The corresponding pad is used in GPIO input mode - The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if the GPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of 1 will clear the bit while writing a value of 0 has no effect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN does not prevent the setting of GPI_SMI_STS.

29.2.37 SMI Enable (GPI_SMI_EN_GPP_C)—Offset 1A0h

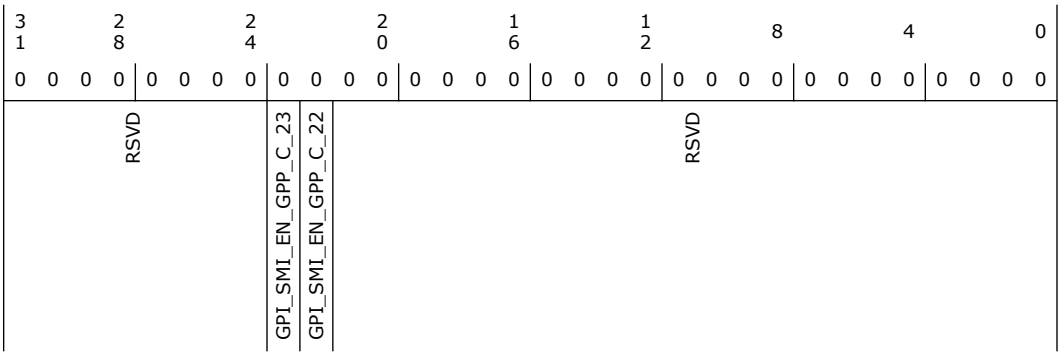
Register bits in this register are implemented for GPP_C signals that have SMI capability only. Other bits are reserved and RO.

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPP_C_23):** Same description as bit 22.
22	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPP_C_22):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to 1. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is 1, bit0 of this bit is locked down to read-only.
21:0	0h RO	Reserved.

29.2.38 SMI Enable (GPI_SMI_EN_GPP_D)—Offset 1A4h

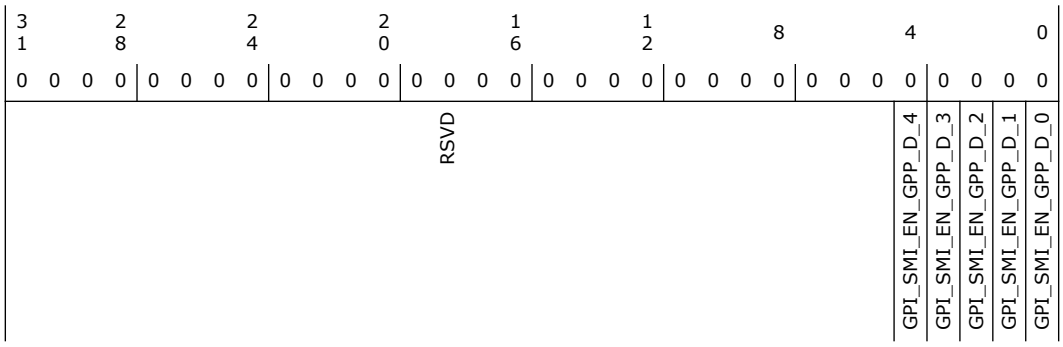
Register bits in this register are implemented for GPP_D signals that have SMI capability only. Other bits are reserved and RO.

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPP_D_4):** Same description as bit 0.
3	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPP_D_3):** Same description as bit 0.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPP_D_2):** Same description as bit 0.
1	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPP_D_1):** Same description as bit 0.
0	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPP_D_0):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to 1. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is 1, bit0 of this bit is locked down to read-only.

29.2.39 SMI Enable (GPI_SMI_EN_GPP_E)—Offset 1A8h

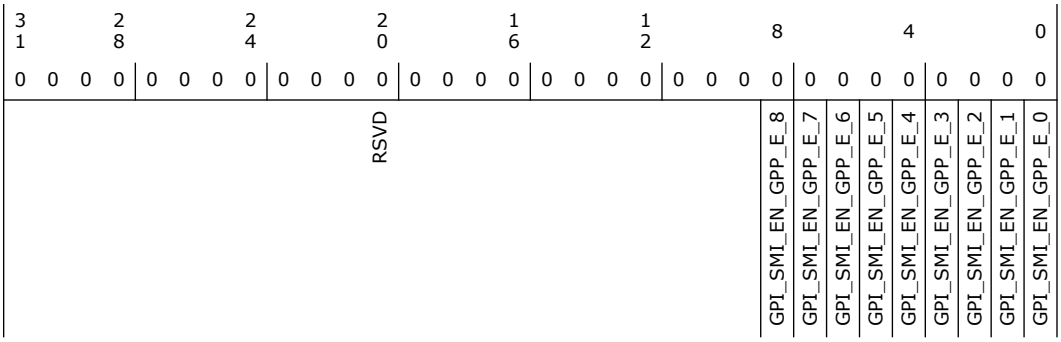
Register bits in this register are implemented for GPP_E signals that have SMI capability only. Other bits are reserved and RO.

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPP_E_8):** Same description as bit 0.
7	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPP_E_7):** Same description as bit 0.
6	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPP_E_6):** Same description as bit 0.
5	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPP_E_5):** Same description as bit 0.
4	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPP_E_4):** Same description as bit 0.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPP_E_3):** Same description as bit 0.
2	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPP_E_2):** Same description as bit 0.
1	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPP_E_1):** Same description as bit 0.
0	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPP_E_0):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to 1. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is 1, bit0 of this bit is locked down to read-only.

29.2.40 NMI Status (GPI_NMI_STS_GPP_C)—Offset 1C0h

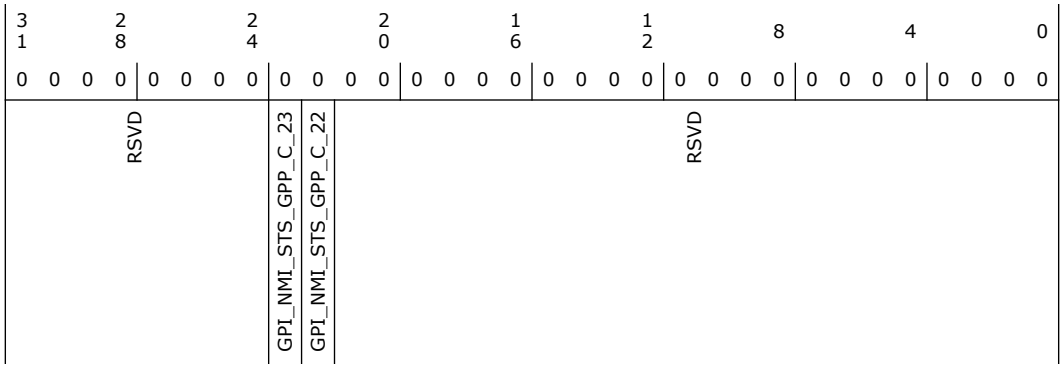
Register bits in this register are implemented for GPP_C signals that have NMI capability only. Other bits are reserved and RO.

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RW1C	**GPI NMI Status (GPI_NMI_STS_GPP_C_23):** Same description as bit 0.
22	0h RW1C	**GPI NMI Status (GPI_NMI_STS_GPP_C_22):** This bit is set to 1 by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: - The corresponding pad is used in GPIO input mode (PMode) - The corresponding GPIONMIRout is set to 1, i.e. programmed to route as NMI - The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). - The corresponding GPI_NMI_EN is set Writing a value of 1 will clear the bit while writing a value of 0 has no effect. 0 = There is no NMI event 1 = There is an NMI event For pads which do not support NMI, the corresponding bit is read-only zero.
21:0	0h RO	Reserved.

29.2.41 NMI Status (GPI_NMI_STS_GPP_D)—Offset 1C4h

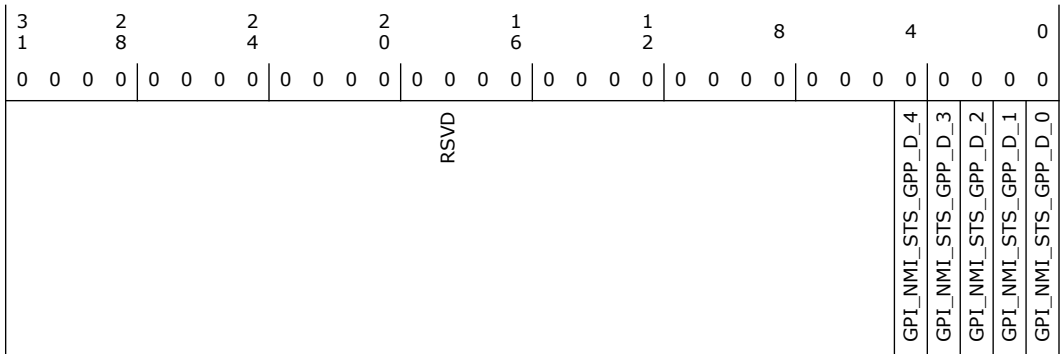
Register bits in this register are implemented for GPP_D signals that have NMI capability only. Other bits are reserved and RO.

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4	0h RW1C	**GPI NMI Status (GPI_NMI_STS_GPP_D_4):** Same description as bit 0.
3	0h RW1C	**GPI NMI Status (GPI_NMI_STS_GPP_D_3):** Same description as bit 0.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW1C	**GPI NMI Status (GPI_NMI_STS_GPP_D_2):** Same description as bit 0.
1	0h RW1C	**GPI NMI Status (GPI_NMI_STS_GPP_D_1):** Same description as bit 0.
0	0h RW1C	**GPI NMI Status (GPI_NMI_STS_GPP_D_0):** This bit is set to 1 by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: - The corresponding pad is used in GPIO input mode (PMode) - The corresponding GPIONMIRout is set to 1, i.e. programmed to route as NMI - The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). - The corresponding GPI_NMI_EN is set Writing a value of 1 will clear the bit while writing a value of 0 has no effect. 0 = There is no NMI event 1 = There is an NMI event For pads which do not support NMI, the corresponding bit is read-only zero.

29.2.42 NMI Status (GPI_NMI_STS_GPP_E)—Offset 1C8h

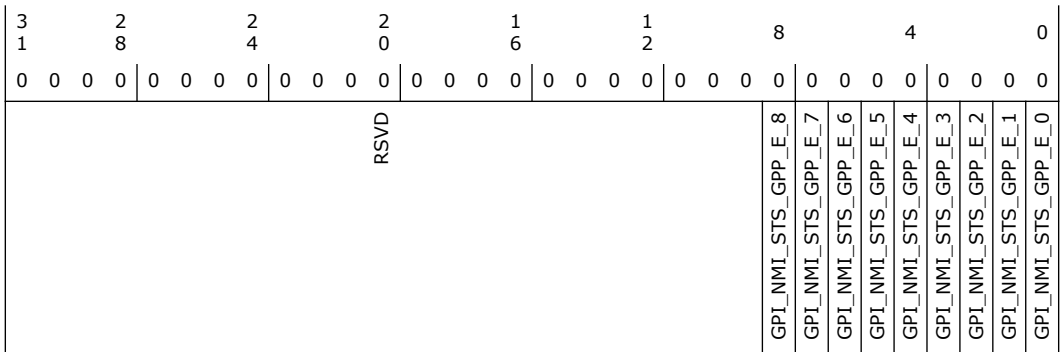
Register bits in this register are implemented for GPP_E signals that have NMI capability only. Other bits are reserved and RO.

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h RW1C	**GPI NMI Status (GPI_NMI_STS_GPP_E_8):** Same description as bit 0.
7	0h RW1C	**GPI NMI Status (GPI_NMI_STS_GPP_E_7):** Same description as bit 0.
6	0h RW1C	**GPI NMI Status (GPI_NMI_STS_GPP_E_6):** Same description as bit 0.
5	0h RW1C	**GPI NMI Status (GPI_NMI_STS_GPP_E_5):** Same description as bit 0.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW1C	**GPI NMI Status (GPI_NMI_STS_GPP_E_4):** Same description as bit 0.
3	0h RW1C	**GPI NMI Status (GPI_NMI_STS_GPP_E_3):** Same description as bit 0.
2	0h RW1C	**GPI NMI Status (GPI_NMI_STS_GPP_E_2):** Same description as bit 0.
1	0h RW1C	**GPI NMI Status (GPI_NMI_STS_GPP_E_1):** Same description as bit 0.
0	0h RW1C	**GPI NMI Status (GPI_NMI_STS_GPP_E_0):** This bit is set to 1 by hardware when an edge event is detected (See RxEdCfg, RxInv) on pad and all the following conditions are true: - The corresponding pad is used in GPIO input mode (PMode) - The corresponding GPIONMIRout is set to 1, i.e. programmed to route as NMI - The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). - The corresponding GPI_NMI_EN is set Writing a value of 1 will clear the bit while writing a value of 0 has no effect. 0 = There is no NMI event 1 = There is an NMI event For pads which do not support NMI, the corresponding bit is read-only zero.

29.2.43 NMI Enable (GPI_NMI_EN_GPP_C)—Offset 1E0h

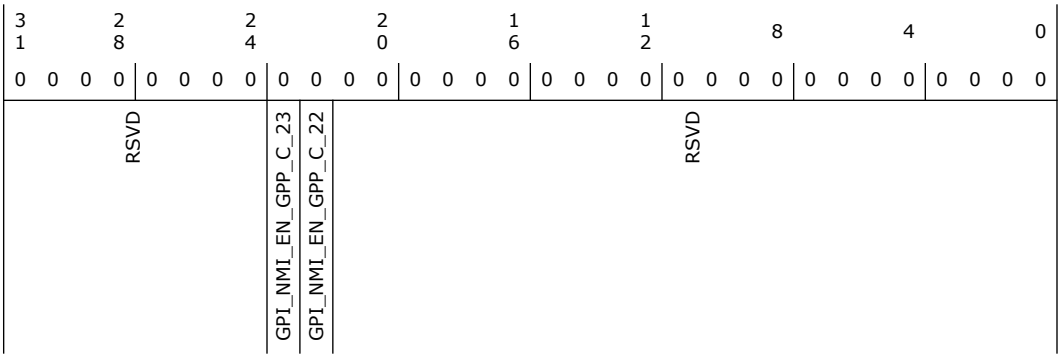
Register bits in this register are implemented for GPP_C signals that have NMI capability only. Other bits are reserved and RO.

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPP_C_23):** Same description as bit 22.
22	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPP_C_22):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. For pads which do not support NMI, the corresponding bit is read-only zero.
21:0	0h RO	Reserved.

29.2.44 NMI Enable (GPI_NMI_EN_GPP_D)—Offset 1E4h

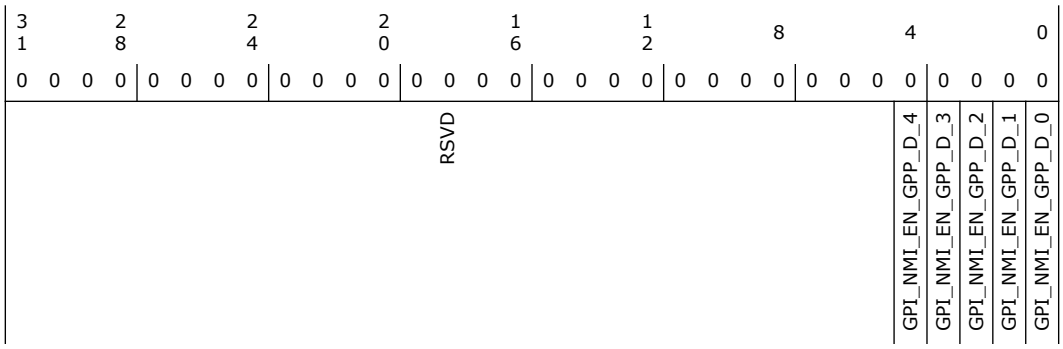
Register bits in this register are implemented for GPP_D signals that have NMI capability only. Other bits are reserved and RO.

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPP_D_4):** Same description as bit 0.
3	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPP_D_3):** Same description as bit 0.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPP_D_2):** Same description as bit 0.
1	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPP_D_1):** Same description as bit 0.
0	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPP_D_0):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. For pads which do not support NMI, the corresponding bit is read-only zero.

29.2.45 NMI Enable (GPI_NMI_EN_GPP_E)—Offset 1E8h

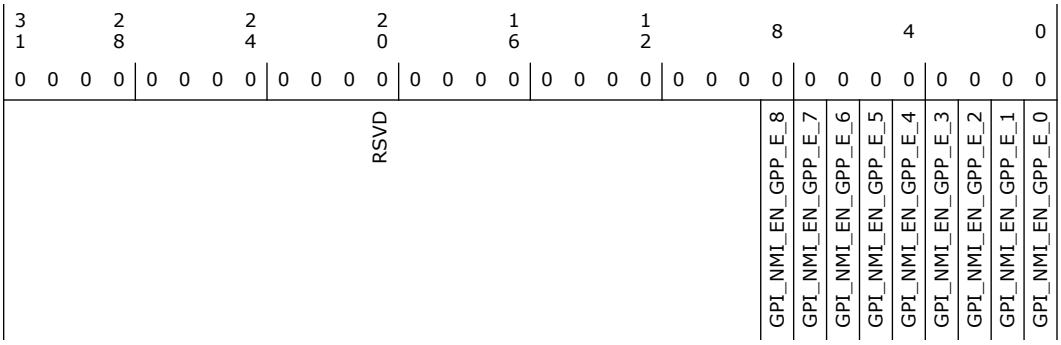
Register bits in this register are implemented for GPP_E signals that have NMI capability only. Other bits are reserved and RO.

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPP_E_8):** Same description as bit 0.
7	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPP_E_7):** Same description as bit 0.
6	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPP_E_6):** Same description as bit 0.
5	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPP_E_5):** Same description as bit 0.
4	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPP_E_4):** Same description as bit 0.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPP_E_3):** Same description as bit 0.
2	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPP_E_2):** Same description as bit 0.
1	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPP_E_1):** Same description as bit 0.
0	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPP_E_0):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only. For pads which do not support NMI, the corresponding bit is read-only zero.

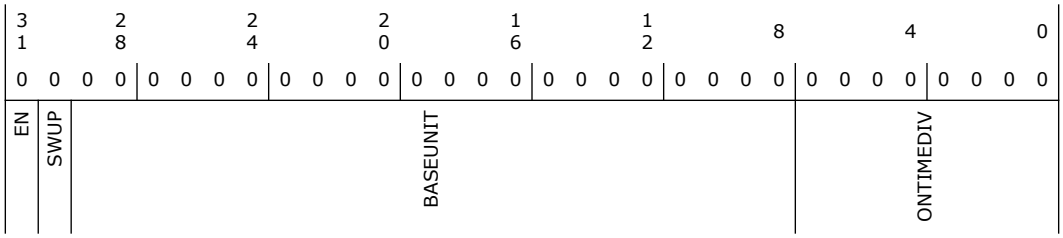
29.2.46 PWM Control (PWMC)—Offset 204h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Enable (EN):** 0 = Disable PWM Output 1 = Enable PWM Output
30	0h RW	**Software Update (SWUP):** Indication that there is an update to PWM settings pending. SW sets this bit to 1 when updating the PWM_base_unit or PWM_on_time_divisor fields. The PWM module will apply the new settings at the end of the current cycle and reset this bit. 0 = No updates pending 1 = Update pending
29:8	0h RW	**Base Unit (BASEUNIT):** Base Unit (BaseUnit) Base unit register. Unsigned 8 integer bits, 14 fraction bits. Used to determine PWM output frequency. The PWM base frequency for SPT is 32.768 KHz.
7:0	0h RW	**On Time Divisor (ONTIMEDIV):** PWM duty cycle = PWM_on-time_divisor/256

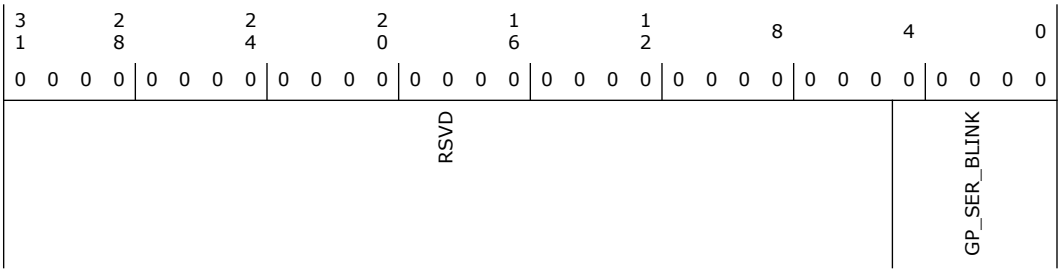
29.2.47 GPIO Serial Blink Enable (GP_SER_BLINK)—Offset 20Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4:0	0h RW	**GP SER BLINK (GP_SER_BLINK):** The setting of this bit has no effect if the corresponding GPIO is programmed as an input, if the corresponding GPIO has the PWM enabled, or if Serial Blink capability does not exist. This bit should be set to a 1 before output buffer is enabled. When set to a '0', the corresponding GPIO will function normally. This bit should be set to a 1 while the corresponding PMode bit is set to 0h (GPIO Mode). Setting the PMode bit to other value (non-GPIO Mode) after the GP_SER_BLINK bit ensures PCH will not drive a 1 on the pin as an output. When this corresponding bit is set to a 1 and the pin is configured to output mode, the serial blink capability is enabled and the programmed message is serialized out through an open-drain buffer configuration. The value of the corresponding GPIOTxState bit remains unchanged and does not impact the serial blink capability in any way. Writes to this register have no effect when the corresponding pin is configured in native mode and the read value returned is undefined. Bit0 = GPP_D0 Bit1 = GPP_D1 Bit2 = GPP_D2 Bit3 = GPP_D3 Bit4 = GPP_D4

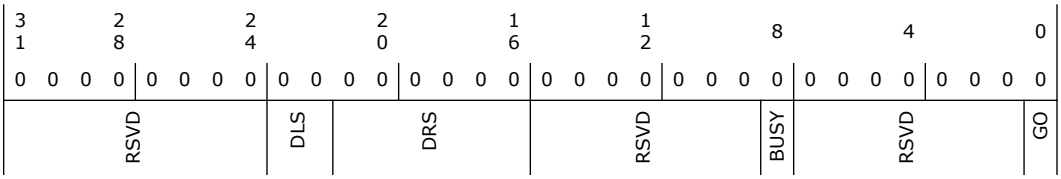
29.2.48 GPIO Serial Blink Command/Status (GP_SER_CMDSTS)—Offset 210h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:22	0h RW	**Data Length Select (DLS):** This read/write field determines the number of bytes to serialize on GPIO 00: Serialize bits 7:0 of GP_GB_DATA (1 byte) 01: Serialize bits 15:0 of GP_GB_DATA (2 bytes) 10: Undefined - Software must not write this value 11: Serialize bits 31:0 of GP_GB_DATA (4 bytes) Software should not modify the value in this register unless the Busy bit
21:16	0h RW	**Data Rate Select (DRS):** Data Rate Select (DRS): This read/write field selects the number of 333.34ns (4 clock periods 12MHz clock) time intervals to count between Manchester data transitions. The default of 8h results in a 2666.67 ns minimum time between transitions. A value of 0h in this register produces undefined behavior. Software should not modify the value in this register unless the Busy bit is clear.
15:9	0h RO	Reserved.
8	0h RO	**Busy (BUSY):** Busy: This read-only status bit is the hardware indication that a serialization is in progress. Hardware sets this bit to 1 based on the Go bit being set. Hardware clears this bit when the Go bit is cleared by the hardware.
7:1	0h RO	Reserved.
0	0h RW	**Go (GO):** Go: This bit is set to 1 by software to start the serialization process. Hardware clears the bit after the serialized data is sent. Writes of 0 to this register have no effect. Software should not write this bit to 1 unless the Busy status bit is cleared.

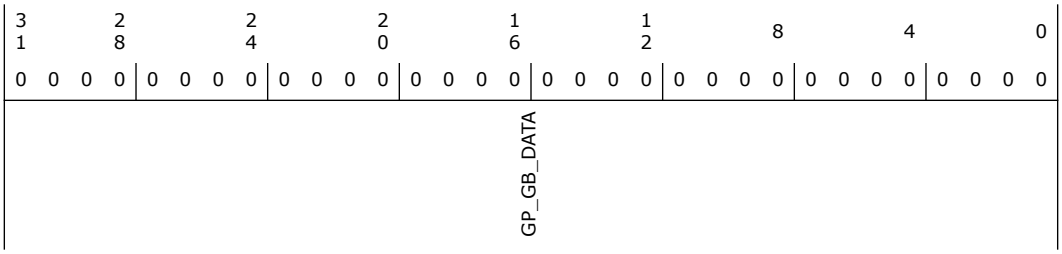
29.2.49 GPIO Serial Blink Data (GP_SER_DATA)—Offset 214h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**GP Serial Blink Data (GP_GB_DATA):** GP_GB_DATA This read-write register contains the data serialized out. The number of bits shifted out is selected through the DLS field in the GP_GB_CMDSTS register. This register should not be modified by software when the Busy bit is set.

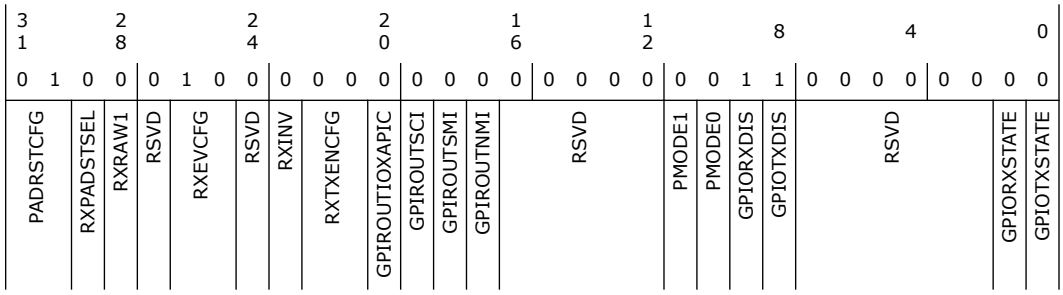
29.2.50 Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_0)—Offset 400h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 44000x00h



Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset GPIO pad register fields in PAD_CFG_DW0 and PAD_CFG_DW1 registers. This register can be used for Sx isolation of the associated signal if needed. 00 = RSMRST# 01 = Host deep reset. This reset occurs when a host reset (with or without power cycle) is initiated or a global reset is initiated, except that the reset does not assert when in S3/S4/S5. 10 = PLTRST# 11 = Reserved
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determines from which node the RX pad state for native function should be taken from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from RX buffer 1 = Internal RX pad state (subject to RXINV and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field is only applicable when the RX buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	Reserved.
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determines if the internal RX pad state (synchronized, filtered vs non-filtered version as determined by PreGfRXSel, and is further subject to RXInv) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller . 0h = Level 1h = Edge 2h = Drive '0' 3h = Reserved (implement as setting 0h)
24	0h RO	Reserved.
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field is only applicable when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion

Bit Range	Default & Access	Field Name (ID): Description
22:21	0h RO	Reserved.
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determines if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determines if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI. 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s).
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determines if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s). This bit only applies to a GPIO that has SMI capability. Otherwise, the bit is RO.
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determines if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit. This bit only applies to a GPIO that has NMI capability. Otherwise, the bit is RO.
16:12	0h RO	Reserved.
11	-- RW	**Pad Mode bit 1 (PMODE1):** See Pad Mode bit 0 description.
10	-- RW	**Pad Mode bit 0 (PMODE0):** This bit is used in conjunction with Pad Mode bit 1. This two-bit field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad. 1h = native function 1, if applicable, controls the Pad 2h = native function 2, if applicable, controls the Pad. Also used to enable the GPIO blink (PWM) capability if applicable (note that not all GPIOs have the blink capability) 3h = native function 3, if applicable, controls the Pad Dedicated (unmuxed) GPIO shall report RO of all 0's in this register field If GPIO vs. native mode is configured via soft strap, this bit has no effect. Default value is determined by the default functionality of the pad.
9	1h RW	**GPIO RX Disable (GPIORXDIS):** 0 = Enable the input buffer (active low enable) of the pad. 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0'.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** 0 = Enable the output buffer (active low enable) of the pad. 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	Reserved.
1	0h RO	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV settings.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** 0 = Drive a level '0' to the TX output pad. 1 = Drive a level '1' to the TX output pad

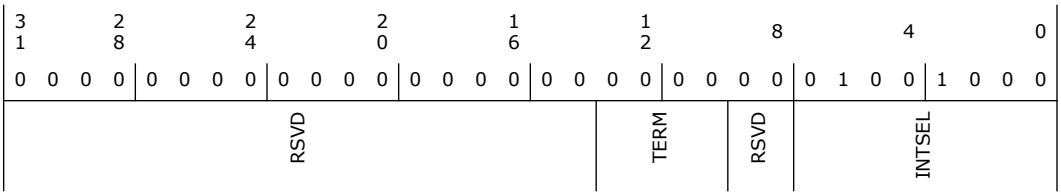
29.2.51 Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_0)—Offset 404h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 48h



Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings for [13:10] correspond to: 0000: none 0010: 5k pd 0100: 20k pd 1010: 5k pu 1100: 20k pu 1111: Native controller selected by Pad Mode controls the Termination. This setting needs to be set only for GPP_A1 / LAD0, GPP_A2 / LAD1, GPP_A3 / LAD2, GPP_A4 / LAD3, GPD1 / ACPRESENT, and GPD2 / LAN_WAKE#, when the signals are used as native function. Otherwise, the setting is reserved. All others settings not mentioned above are reserved. If a reserved value is programmed, pad may malfunction. The setting of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in sw/fw in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, pu/pd settings should be programmed first to ensure the input does not float momentarily.
9:8	0h RO	Reserved.
7:0	48h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 .... Up to the max IOxAPIC IRQ supported

29.2.52 Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_1)—Offset 408h

Same description as PAD_CFG_DW0_GPP_C_0.

29.2.53 Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_1)—Offset 40Ch

Same description as PAD_CFG_DW1_GPP_C_0. Exception: The default value of the INTSEL bit field in this register is: 49h

29.2.54 Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_2)—Offset 410h

Same description as PAD_CFG_DW0_GPP_C_0

29.2.55 Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_2)—Offset 414h

Same description as PAD_CFG_DW1_GPP_C_0. Exception: The default value of the INTSEL bit field in this register is: 4Ah

29.2.56 Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_3)—Offset 418h

Same description as PAD_CFG_DW0_GPP_C_0

29.2.57 Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_3)—Offset 41Ch

Same description as PAD_CFG_DW1_GPP_C_0. Exception: The default value of the INTSEL bit field in this register is: 4Bh

29.2.58 Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_4)—Offset 420h

Same description as PAD_CFG_DW0_GPP_C_0.

29.2.59 Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_4)—Offset 424h

Same description as PAD_CFG_DW1_GPP_C_0. Exception: The default value of the INTSEL bit field in this register is: 4Ch

29.2.60 Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_5)—Offset 428h

Same description as PAD_CFG_DW0_GPP_C_0.

29.2.61 Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_5)—Offset 42Ch

Same description as PAD_CFG_DW1_GPP_C_0. Exception: The default value of the INTSEL bit field in this register is: 4Dh

29.2.62 Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_6)—Offset 430h

Same description as PAD_CFG_DW0_GPP_C_0.

29.2.63 Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_6)—Offset 434h

Same description as PAD_CFG_DW1_GPP_C_0. Exception: The default value of the INTSEL bit field in this register is: 4Eh

29.2.64 Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_7)—Offset 438h

Same description as PAD_CFG_DW0_GPP_C_0.

29.2.65 Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_7)—Offset 43Ch

Same description as PAD_CFG_DW1_GPP_C_0. Exception: The default value of the INTSEL bit field in this register is: 4Fh

29.2.66 Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_8)—Offset 440h

Same description as PAD_CFG_DW0_GPP_C_0.

29.2.67 Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_8)—Offset 444h

Same description as PAD_CFG_DW1_GPP_C_0. Exception: The default value of the INTSEL bit field in this register is: 50h

29.2.68 Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_9)—Offset 448h

Same description as PAD_CFG_DW0_GPP_C_0.

29.2.69 Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_9)—Offset 44Ch

Same description as PAD_CFG_DW1_GPP_C_0. Exception: The default value of the INTSEL bit field in this register is: 51h

29.2.70 Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_10)—Offset 450h

Same description as PAD_CFG_DW0_GPP_C_0.

29.2.71 Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_10)—Offset 454h

Same description as PAD_CFG_DW1_GPP_C_0. Exception: The default value of the INTSEL bit field in this register is: 52h

29.2.72 Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_11)—Offset 458h

Same description as PAD_CFG_DW0_GPP_C_0.

29.2.73 Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_11)—Offset 45Ch

Same description as PAD_CFG_DW1_GPP_C_0. Exception: The default value of the INTSEL bit field in this register is: 53h

29.2.74 Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_12)—Offset 460h

Same description as PAD_CFG_DW0_GPP_C_0.

29.2.75 Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_12)—Offset 464h

Same description as PAD_CFG_DW1_GPP_C_0. Exception: The default value of the INTSEL bit field in this register is: 54h

29.2.76 Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_13)—Offset 468h

Same description as PAD_CFG_DW0_GPP_C_0.

29.2.77 Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_13)—Offset 46Ch

Same description as PAD_CFG_DW1_GPP_C_0. Exception: The default value of the INTSEL bit field in this register is: 55h

29.2.78 Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_14)—Offset 470h

Same description as PAD_CFG_DW0_GPP_C_0.

29.2.79 Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_14)—Offset 474h

Same description as PAD_CFG_DW1_GPP_C_0. Exception: The default value of the INTSEL bit field in this register is: 56h

29.2.80 Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_15)—Offset 478h

Same description as PAD_CFG_DW0_GPP_C_0.

29.2.81 Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_15)—Offset 47Ch

Same description as PAD_CFG_DW1_GPP_C_0. Exception: The default value of the INTSEL bit field in this register is: 57h

29.2.82 Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_16)—Offset 480h

Same description as PAD_CFG_DW0_GPP_C_0.

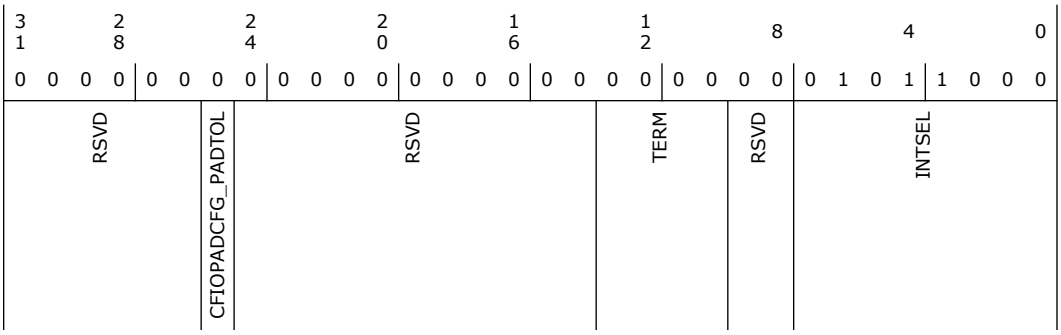
29.2.83 Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_16)—Offset 484h

Note that this register definition also applies to GPP_C[19:17], GPP_D[8:5], and GPP_D[14:13].

Access Method

Type: MSG Register (Size: 32 bits)	**Device:** **Function:**

Default: 58h



Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	Reserved.
25	0h RW	**Pad Voltage Tolerance (CFIOPADCFG_PADTOL):** 0 = pad is 3.3V tolerance (VccIO is 3.3V) 1 = pad is 1.8V tolerance (VccIO is 3.3V).
24:14	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings for [13:10] correspond to: 0000: none 0010: 5k pd 0100: 20k pd 1000: none 1001: 1k pu 1011: 2k pu 1010: 5k pu 1100: 20k pu 1101: 1k & 2k (in parallel) pu All others reserved. If a reserved value is programmed, pad may malfunction. The setting of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in sw/fw in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, pu/pd settings should be programmed first to ensure the input does not float momentarily.
9:8	0h RO	Reserved.
7:0	58h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 .... Up to the max IOxAPIC IRQ supported

29.2.84 Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_17)—Offset 488h

Same description as PAD_CFG_DW0_GPP_C_0.

29.2.85 Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_17)—Offset 48Ch

Same description as PAD_CFG_DW1_GPP_C_16. Exception: The default value of the INTSEL bit field in this register is: 59h

29.2.86 Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_18)—Offset 490h

Same description as PAD_CFG_DW1_GPP_C_16

29.2.87 Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_18)—Offset 494h

Same description as PAD_CFG_DW1_GPP_C_16. Exception: The default value of the INTSEL bit field in this register is: 5Ah

29.2.88 Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_19)—Offset 498h

Same description as PAD_CFG_DW0_GPP_C_0.

29.2.89 Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_19)—Offset 49Ch

Same description as PAD_CFG_DW1_GPP_C_16. Exception: The default value of the INTSEL bit field in this register is: 5Bh

29.2.90 Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_20)—Offset 4A0h

Same description as PAD_CFG_DW0_GPP_C_0.

29.2.91 Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_20)—Offset 4A4h

Same description as PAD_CFG_DW1_GPP_C_0. Exception: The default value of the INTSEL bit field in this register is: 5Ch

29.2.92 Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_21)—Offset 4A8h

Same description as PAD_CFG_DW0_GPP_C_0.

29.2.93 Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_21)—Offset 4ACh

Same description as PAD_CFG_DW1_GPP_C_0. Exception: The default value of the INTSEL bit field in this register is: 5Dh

29.2.94 Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_22)—Offset 4B0h

Same description as PAD_CFG_DW0_GPP_C_0.

29.2.95 Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_22)—Offset 4B4h

Same description as PAD_CFG_DW1_GPP_C_0. Exception: The default value of the INTSEL bit field in this register is: 5Eh

29.2.96 Pad Configuration DW0 (PAD_CFG_DW0_GPP_C_23)—Offset 4B8h

Same description as PAD_CFG_DW0_GPP_C_0.

29.2.97 Pad Configuration DW1 (PAD_CFG_DW1_GPP_C_23)—Offset 4BCh

Same description as PAD_CFG_DW1_GPP_C_0. Exception: The default value of the INTSEL bit field in this register is: 5Fh

29.2.98 Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_0)—Offset 4C0h

Same description as PAD_CFG_DW0_GPP_C_0.

29.2.99 Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_0)—Offset 4C4h

Same description as PAD_CFG_DW1_GPP_C_0. Exception: The default value of the INTSEL bit field in this register is: 60h

29.2.100 Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_1)—Offset 4C8h

Same description as PAD_CFG_DW0_GPP_C_0.

29.2.101 Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_1)—Offset 4CCh

Same description as PAD_CFG_DW1_GPP_C_0. Exception: The default value of the INTSEL bit field in this register is: 61h

29.2.102 Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_2)—Offset 4D0h

Same description as PAD_CFG_DW0_GPP_C_0.

29.2.103 Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_2)—Offset 4D4h

Same description as PAD_CFG_DW1_GPP_C_0. Exception: The default value of the INTSEL bit field in this register is: 62h

29.2.104 Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_3)—Offset 4D8h

Same description as PAD_CFG_DW0_GPP_C_0.

29.2.105 Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_3)—Offset 4DCh

Same description as PAD_CFG_DW1_GPP_C_0. Exception: The default value of the INTSEL bit field in this register is: 63h

29.2.106 Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_4)—Offset 4E0h

Same description as PAD_CFG_DW0_GPP_C_0.

29.2.107 Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_4)—Offset 4E4h

Same description as PAD_CFG_DW1_GPP_C_0. Exception: The default value of the INTSEL bit field in this register is: 64h

29.2.108 Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_5)—Offset 4E8h

Same description as PAD_CFG_DW0_GPP_C_0.

29.2.109 Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_5)—Offset 4ECh

Same description as PAD_CFG_DW1_GPP_C_16. Exception: The default value of the INTSEL bit field in this register is: 65h

29.2.110 Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_6)—Offset 4F0h

Same description as PAD_CFG_DW0_GPP_C_0.

29.2.111 Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_6)—Offset 4F4h

Same description as PAD_CFG_DW1_GPP_C_16. Exception: The default value of the INTSEL bit field in this register is: 66h

29.2.112 Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_7)—Offset 4F8h

Same description as PAD_CFG_DW0_GPP_C_0.

29.2.113 Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_7)—Offset 4FCh

Same description as PAD_CFG_DW1_GPP_C_16. Exception: The default value of the INTSEL bit field in this register is: 67h

29.2.114 Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_8)—Offset 500h

Same description as PAD_CFG_DW0_GPP_C_0.

29.2.115 Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_8)—Offset 504h

Same description as PAD_CFG_DW1_GPP_C_16. Exception: The default value of the INTSEL bit field in this register is: 68h

29.2.116 Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_9)—Offset 508h

Same description as PAD_CFG_DW0_GPP_C_0.

29.2.117 Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_9)—Offset 50Ch

Same description as PAD_CFG_DW1_GPP_C_0. Exception: The default value of the INTSEL bit field in this register is: 69h

29.2.118 Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_10)—Offset 510h

Same description as PAD_CFG_DW0_GPP_C_0.

29.2.119 Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_10)—Offset 514h

Same description as PAD_CFG_DW1_GPP_C_0. Exception: The default value of the INTSEL bit field in this register is: 6Ah

29.2.120 Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_11)—Offset 518h

Same description as PAD_CFG_DW0_GPP_C_0.

29.2.121 Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_11)—Offset 51Ch

Same description as PAD_CFG_DW1_GPP_C_0. Exception: The default value of the INTSEL bit field in this register is: 6Bh

29.2.122 Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_12)—Offset 520h

Same description as PAD_CFG_DW0_GPP_C_0.

29.2.123 Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_12)—Offset 524h

Same description as PAD_CFG_DW1_GPP_C_0. Exception: The default value of the INTSEL bit field in this register is: 6Ch

29.2.124 Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_13)—Offset 528h

Same description as PAD_CFG_DW0_GPP_C_0.

29.2.125 Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_13)—Offset 52Ch

Same description as PAD_CFG_DW1_GPP_C_16. Exception: The default value of the INTSEL bit field in this register is: 6Dh

29.2.126 Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_14)—Offset 530h

Same description as PAD_CFG_DW0_GPP_C_0.

29.2.127 Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_14)—Offset 534h

Same description as PAD_CFG_DW1_GPP_C_16. Exception: The default value of the INTSEL bit field in this register is: 6Eh

29.2.128 Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_15)—Offset 538h

Same description as PAD_CFG_DW0_GPP_C_0.

29.2.129 Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_15)—Offset 53Ch

Same description as PAD_CFG_DW1_GPP_C_0. Exception: The default value of the INTSEL bit field in this register is: 6Fh

29.2.130 Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_16)—Offset 540h

Same description as PAD_CFG_DW0_GPP_C_0.

29.2.131 Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_16)—Offset 544h

Same description as PAD_CFG_DW1_GPP_C_0. Exception: The default value of the INTSEL bit field in this register is: 70h

29.2.132 Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_17)—Offset 548h

Same description as PAD_CFG_DW0_GPP_C_0.

29.2.133 Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_17)—Offset 54Ch

Same description as PAD_CFG_DW1_GPP_C_0. Exception: The default value of the INTSEL bit field in this register is: 71h

29.2.134 Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_18)—Offset 550h

Same description as PAD_CFG_DW0_GPP_C_0.

29.2.135 Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_18)—Offset 554h

Same description as PAD_CFG_DW1_GPP_C_0. Exception: The default value of the INTSEL bit field in this register is: 72h

29.2.136 Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_19)—Offset 558h

Same description as PAD_CFG_DW0_GPP_C_0.

29.2.137 Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_19)—Offset 55Ch

Same description as PAD_CFG_DW1_GPP_C_0. Exception: The default value of the INTSEL bit field in this register is: 73h

29.2.138 Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_20)—Offset 560h

Same description as PAD_CFG_DW0_GPP_C_0.

29.2.139 Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_20)—Offset 564h

Same description as PAD_CFG_DW1_GPP_C_0. Exception: The default value of the INTSEL bit field in this register is: 74h

29.2.140 Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_21)—Offset 568h

Same description as PAD_CFG_DW0_GPP_C_0.

29.2.141 Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_21)—Offset 56Ch

Same description as PAD_CFG_DW1_GPP_C_0. Exception: The default value of the INTSEL bit field in this register is: 75h

29.2.142 Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_22)—Offset 570h

Same description as PAD_CFG_DW0_GPP_C_0.

29.2.143 Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_22)—Offset 574h

Same description as PAD_CFG_DW1_GPP_C_0. Exception: The default value of the INTSEL bit field in this register is: 76h

29.2.144 Pad Configuration DW0 (PAD_CFG_DW0_GPP_D_23)—Offset 578h

Same description as PAD_CFG_DW0_GPP_C_0.

29.2.145 Pad Configuration DW1 (PAD_CFG_DW1_GPP_D_23)—Offset 57Ch

Same description as PAD_CFG_DW1_GPP_C_0. Exception: The default value of the INTSEL bit field in this register is: 77h

29.2.146 Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_0)—Offset 580h

Same description as PAD_CFG_DW0_GPP_C_0.

29.2.147 Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_0)—Offset 584h

Same description as PAD_CFG_DW1_GPP_C_0. Exception: The default value of the INTSEL bit field in this register is: 18h

29.2.148 Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_1)—Offset 588h

Same description as PAD_CFG_DW0_GPP_C_0.

29.2.149 Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_1)—Offset 58Ch

Same description as PAD_CFG_DW1_GPP_C_0. Exception: The default value of the INTSEL bit field in this register is: 19h

29.2.150 Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_2)—Offset 590h

Same description as PAD_CFG_DW0_GPP_C_0.

29.2.151 Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_2)—Offset 594h

Same description as PAD_CFG_DW1_GPP_C_0. Exception: The default value of the INTSEL bit field in this register is: 1Ah

29.2.152 Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_3)—Offset 598h

Same description as PAD_CFG_DW0_GPP_C_0.

29.2.153 Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_3)—Offset 59Ch

Same description as PAD_CFG_DW1_GPP_C_0 Exception: The default value of the INTSEL bit field in this register is : 1Bh

29.2.154 Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_4)—Offset 5A0h

Same description as PAD_CFG_DW0_GPP_C_0.

29.2.155 Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_4)—Offset 5A4h

Same description as PAD_CFG_DW1_GPP_C_0 Exception: The default value of the INTSEL bit field in this register is : 1Ch

29.2.156 Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_5)—Offset 5A8h

Same description as PAD_CFG_DW0_GPP_C_0.

29.2.157 Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_5)—Offset 5ACh

Same description as PAD_CFG_DW1_GPP_C_0 Exception: The default value of the INTSEL bit field in this register is : 1Dh

29.2.158 Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_6)—Offset 5B0h

Same description as PAD_CFG_DW0_GPP_C_0.

29.2.159 Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_6)—Offset 5B4h

Same description as PAD_CFG_DW1_GPP_C_0 Exception: The default value of the INTSEL bit field in this register is : 1Eh

29.2.160 Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_7)—Offset 5B8h

Same description as PAD_CFG_DW0_GPP_C_0.

29.2.161 Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_7)—Offset 5BCh

Same description as PAD_CFG_DW1_GPP_C_0 Exception: The default value of the INTSEL bit field in this register is : 1Fh

29.2.162 Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_8)—Offset 5C0h

Same description as PAD_CFG_DW0_GPP_C_0.

29.2.163 Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_8)—Offset 5C4h

Same description as PAD_CFG_DW1_GPP_C_0 Exception: The default value of the INTSEL bit field in this register is : 20h

29.2.164 Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_9)—Offset 5C8h

Same description as PAD_CFG_DW0_GPP_C_0.

29.2.165 Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_9)—Offset 5CCh

Same description as PAD_CFG_DW0_GPP_C_0. Exception: The default value of the INTSEL bit field in this register is : 21h

29.2.166 Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_10)—Offset 5D0h

Same description as PAD_CFG_DW0_GPP_C_0.

29.2.167 Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_10)—Offset 5D4h

Same description as PAD_CFG_DW0_GPP_C_0. Exception: The default value of the INTSEL bit field in this register is : 22h

29.2.168 Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_11)—Offset 5D8h

Same description as PAD_CFG_DW0_GPP_C_0.

29.2.169 Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_11)—Offset 5DCh

Same description as PAD_CFG_DW0_GPP_C_0. Exception: The default value of the INTSEL bit field in this register is : 23h

29.2.170 Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_12)—Offset 5E0h

Same description as PAD_CFG_DW0_GPP_C_0.

29.2.171 Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_12)—Offset 5E4h

Same description as PAD_CFG_DW0_GPP_C_0. Exception: The default value of the INTSEL bit field in this register is : 24h

29.2.172 Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_13)—Offset 5E8h

Same description as PAD_CFG_DW0_GPP_C_0.

29.2.173 Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_13)—Offset 5ECh

Same description as PAD_CFG_DW0_GPP_C_0. Exception: The default value of the INTSEL bit field in this register is : 25h

29.2.174 Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_14)—Offset 5F0h

Same description as PAD_CFG_DW0_GPP_C_0.

29.2.175 Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_14)—Offset 5F4h

Same description as PAD_CFG_DW0_GPP_C_0. Exception: The default value of the INTSEL bit field in this register is : 26h

29.2.176 Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_15)—Offset 5F8h

Same description as PAD_CFG_DW0_GPP_C_0.

29.2.177 Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_15)—Offset 5FCh

Same description as PAD_CFG_DW0_GPP_C_0. Exception: The default value of the INTSEL bit field in this register is : 27h

29.2.178 Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_16)—Offset 600h

Same description as PAD_CFG_DW0_GPP_C_0.

29.2.179 Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_16)—Offset 604h

Same description as PAD_CFG_DW0_GPP_C_0. Exception: The default value of the INTSEL bit field in this register is : 28h

29.2.180 Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_17)—Offset 608h

Same description as PAD_CFG_DW0_GPP_C_0.

29.2.181 Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_17)—Offset 60Ch

Same description as PAD_CFG_DW0_GPP_C_0. Exception: The default value of the INTSEL bit field in this register is : 29h

29.2.182 Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_18)—Offset 610h

Same description as PAD_CFG_DW0_GPP_C_0.

29.2.183 Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_18)—Offset 614h

Same description as PAD_CFG_DW0_GPP_C_0. Exception: The default value of the INTSEL bit field in this register is : 2Ah

29.2.184 Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_19)—Offset 618h

Same description as PAD_CFG_DW0_GPP_C_0.

29.2.185 Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_19)—Offset 61Ch

Same description as PAD_CFG_DW0_GPP_C_0. Exception: The default value of the INTSEL bit field in this register is : 2Bh

29.2.186 Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_20)—Offset 620h

Same description as PAD_CFG_DW0_GPP_C_0.

29.2.187 Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_20)—Offset 624h

Same description as PAD_CFG_DW0_GPP_C_0. Exception: The default value of the INTSEL bit field in this register is : 2Ch

29.2.188 Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_21)—Offset 628h

Same description as PAD_CFG_DW0_GPP_C_0.

29.2.189 Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_21)—Offset 62Ch

Same description as PAD_CFG_DW0_GPP_C_0. Exception: The default value of the INTSEL bit field in this register is : 2Dh

29.2.190 Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_22)—Offset 630h

Same description as PAD_CFG_DW0_GPP_C_0.

29.2.191 Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_22)—Offset 634h

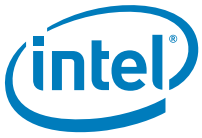
Same description as PAD_CFG_DW0_GPP_C_0. Exception: The default value of the INTSEL bit field in this register is : 2Eh

29.2.192 Pad Configuration DW0 (PAD_CFG_DW0_GPP_E_23)—Offset 638h

Same description as PAD_CFG_DW0_GPP_C_0.

29.2.193 Pad Configuration DW1 (PAD_CFG_DW1_GPP_E_23)—Offset 63Ch

Same description as PAD_CFG_DW0_GPP_C_0. Exception: The default value of the INTSEL bit field in this register is : 2Fh



29.3 GPIO Community 2 Registers Summary

Community 2 Registers are for GPP_DSW group.

These registers are within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID + Register Offset).

Table 29-3. Summary of GPIO Community 2 Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
8h	Bh	Family Base Address (FAMBAR)—Offset 8h	300h
Ch	Fh	Pad Base Address (PADBAR)—Offset Ch	400h
10h	13h	Miscellaneous Configuration (MISCCFG)—Offset 10h	43200h
20h	23h	Pad Ownership (PAD_OWN_GPD_0)—Offset 20h	0h
24h	27h	Pad Ownership (PAD_OWN_GPD_1)—Offset 24h	0h
A0h	A3h	Pad Configuration Lock (PADCFGLOCK_GPD_0)—Offset A0h	0h
A4h	A7h	Pad Configuration Lock (PADCFGLOCKTX_GPD_0)—Offset A4h	0h
D0h	D3h	Host Software Pad Ownership (HOSTSW_OWN_GPD_0)—Offset D0h	0h
100h	103h	GPI Interrupt Status (GPI_IS_GPD_0)—Offset 100h	0h
120h	123h	GPI Interrupt Enable (GPI_IE_GPD_0)—Offset 120h	0h
140h	143h	GPI General Purpose Events Status (GPI_GPE_STS_GPD_0)—Offset 140h	0h
160h	163h	GPI General Purpose Events Enable (GPI_GPE_EN_GPD_0)—Offset 160h	0h
400h	403h	Pad Configuration DW0 (PAD_CFG_DW0_GPD_0)—Offset 400h	4000X00h See register for X value
404h	407h	Pad Configuration DW1 (PAD_CFG_DW1_GPD_0)—Offset 404h	50h
408h	40Bh	Pad Configuration DW0 (PAD_CFG_DW0_GPD_1)—Offset 408h	44000X00h See register for X value
40Ch	40Fh	Pad Configuration DW1 (PAD_CFG_DW1_GPD_1)—Offset 40Ch	See Register
410h	413h	Pad Configuration DW0 (PAD_CFG_DW0_GPD_2)—Offset 410h	44000X00h See register for X value
414h	417h	Pad Configuration DW1 (PAD_CFG_DW1_GPD_2)—Offset 414h	See Register
418h	41Bh	Pad Configuration DW0 (PAD_CFG_DW0_GPD_3)—Offset 418h	44000X00h See register for X value
41Ch	41Fh	Pad Configuration DW1 (PAD_CFG_DW1_GPD_3)—Offset 41Ch	See Register
420h	423h	Pad Configuration DW0 (PAD_CFG_DW0_GPD_4)—Offset 420h	44000X00h See register for X value
424h	427h	Pad Configuration DW1 (PAD_CFG_DW1_GPD_4)—Offset 424h	See Register
428h	42Bh	Pad Configuration DW0 (PAD_CFG_DW0_GPD_5)—Offset 428h	44000X00h See register for X value

Table 29-3. Summary of GPIO Community 2 Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
42Ch	42Fh	Pad Configuration DW1 (PAD_CFG_DW1_GPD_5)—Offset 42Ch	See Register
430h	433h	Pad Configuration DW0 (PAD_CFG_DW0_GPD_6)—Offset 430h	44000X00h See register for X value
434h	437h	Pad Configuration DW1 (PAD_CFG_DW1_GPD_6)—Offset 434h	See Register
438h	43Bh	Pad Configuration DW0 (PAD_CFG_DW0_GPD_7)—Offset 438h	44000X00h See register for X value
43Ch	43Fh	Pad Configuration DW1 (PAD_CFG_DW1_GPD_7)—Offset 43Ch	See Register
440h	443h	Pad Configuration DW0 (PAD_CFG_DW0_GPD_8)—Offset 440h	44000X00h See register for X value
444h	447h	Pad Configuration DW1 (PAD_CFG_DW1_GPD_8)—Offset 444h	See Register
448h	44Bh	Pad Configuration DW0 (PAD_CFG_DW0_GPD_9)—Offset 448h	44000X00h See register for X value
44Ch	44Fh	Pad Configuration DW1 (PAD_CFG_DW1_GPD_9)—Offset 44Ch	See Register
450h	453h	Pad Configuration DW0 (PAD_CFG_DW0_GPD_10)—Offset 450h	44000X00h See register for X value
454h	457h	Pad Configuration DW1 (PAD_CFG_DW1_GPD_10)—Offset 454h	See Register
458h	45Bh	Pad Configuration DW0 (PAD_CFG_DW0_GPD_11)—Offset 458h	44000X00h See register for X value
45Ch	45Fh	Pad Configuration DW1 (PAD_CFG_DW1_GPD_11)—Offset 45Ch	See Register

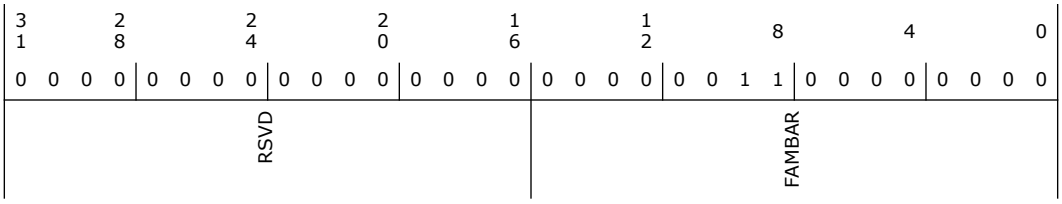
29.3.1 Family Base Address (FAMBAR)—Offset 8h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 300h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	300h RO	**Family Base Address (FAMBAR):** This field provides the starting byte-align address of Family0 register sets. It is meant for software to discover from where the very first Family register (i.e. Family0 register) starts to compute the next Families address offsets.

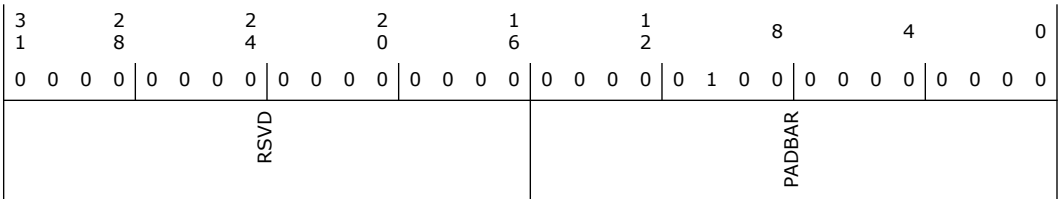
29.3.2 Pad Base Address (PADBAR)—Offset Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 400h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	400h RO	**Pad Base Address (PADBAR):** This field provides the starting byte-align address of Pad0 register sets. It is meant for software to discover from where the very first Pad register (i.e. Pad0 register) starts to compute the next Pad address offsets.

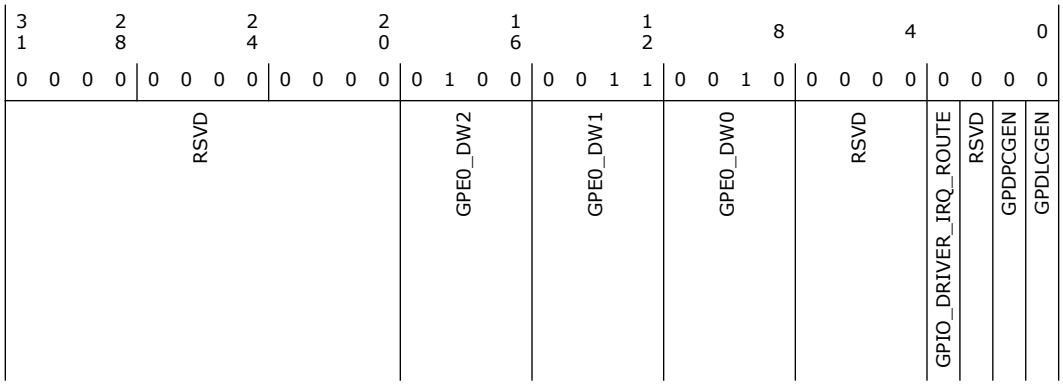
29.3.3 Miscellaneous Configuration (MISCCFG)—Offset 10h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 43200h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	Reserved.
19:16	4h RW	**GPIO Group to GPE_DW0 assignment encoding (GPE0_DW2):** This register assigns a specific GPIO Group to the ACPI GPE0[95:64]. The selected GPIO group will be mapped to lower bits of the GPE register 0h = GPP_A[23:0] mapped to GPE[87:64]; GPE[95:88] not used. 1h = GPP_B[23:0] mapped to GPE[87:64]; GPE[95:88] not used. 2h = GPP_C[23:0] mapped to GPE[87:64]; GPE[95:88] not used. 3h = GPP_D[23:0] mapped to GPE[87:64]; GPE[95:88] not used. 4h = GPP_E[23:0] mapped to GPE[87:64]; GPE[95:88] not used. 5h = GPP_F[23:0] mapped to GPE[87:64]; GPE[95:88] not used. 6h = GPP_G[7:0] mapped to GPE[51:64]; GPE[95:52] not used. 7h = GPD[11:0] mapped to GPE[75:64]; GPE[95:76] not used.
15:12	3h RW	**GPIO Group to GPE_DW0 assignment encoding (GPE0_DW1):** This register assigns a specific GPIO Group to the ACPI GPE0[63:32]. The selected GPIO group will be mapped to lower bits of the GPE register 0h = GPP_A[23:0] mapped to GPE[55:32]; GPE[63:56] not used. 1h = GPP_B[23:0] mapped to GPE[55:32]; GPE[63:56] not used. 2h = GPP_C[23:0] mapped to GPE[55:32]; GPE[63:56] not used. 3h = GPP_D[23:0] mapped to GPE[55:32]; GPE[63:56] not used. 4h = GPP_E[23:0] mapped to GPE[55:32]; GPE[63:56] not used. 5h = GPP_F[23:0] mapped to GPE[55:32]; GPE[63:56] not used. 6h = GPP_G[7:0] mapped to GPE[39:32]; GPE[63:40] not used. 7h = GPD[11:0] mapped to GPE[43:32]; GPE[63:44] not used.
11:8	2h RW	**GPIO Group to GPE_DW0 assignment encoding (GPE0_DW0):** This register assigns a specific GPIO Group to the ACPI GPE0[31:0]. The selected GPIO group will be mapped to lower bits of the GPE register 0h = GPP_A[23:0] mapped to GPE[23:0]; GPE[31:24] not used. 1h = GPP_B[23:0] mapped to GPE[23:0]; GPE[31:24] not used. 2h = GPP_C[23:0] mapped to GPE[23:0]; GPE[31:24] not used. 3h = GPP_D[23:0] mapped to GPE[23:0]; GPE[31:24] not used. 4h = GPP_E[23:0] mapped to GPE[23:0]; GPE[31:24] not used. 5h = GPP_F[23:0] mapped to GPE[23:0]; GPE[31:24] not used. 6h = GPP_G[7:0] mapped to GPE[7:0]; GPE[31:8] not used. 7h = GPD[11:0] mapped to GPE[11:0]; GPE[31:12] not used.
7:4	0h RO	Reserved.
3	0h RW	**GPIO Driver IRQ Route (GPIO_DRIVER_IRQ_ROUTE):** GPIO Driver IRQ_ROUTE[1:0]: Specifies the APIC IRQ globally for all pads within the current community (GPI_IS with corresponding GPI_IE enable). 0 = IRQ14 1 = IRQ15

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	Reserved.
1	0h RW	**GPIO Dynamic Partition Clock Gating Enable (GPDPCGEN):** Specifies whether the GPIO Community should take part in partition clock gating 0 = Disable participation in dynamic partition clock gating 1 = Enable participation in dynamic partition clock gating.
0	0h RW	**GPIO Dynamic Local Clock Gating Enable (GPDLCGEN):** Specifies whether the GPIO Community should perform local clock gating. 0 = Disable dynamic local clock gating 1 = Enable dynamic local clock gating

29.3.4 Pad Ownership (PAD_OWN_GPD_0)—Offset 20h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD	PAD_OWN_GPD_7		RSVD	PAD_OWN_GPD_6		RSVD	PAD_OWN_GPD_5		RSVD	PAD_OWN_GPD_4		RSVD	PAD_OWN_GPD_3		RSVD	PAD_OWN_GPD_2		RSVD	PAD_OWN_GPD_1		RSVD	PAD_OWN_GPD_0								

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29:28	0h RO	**Pad Ownership (PAD_OWN_GPD_7):** Same description as bit 0, except that the bit field applies to GPD_7.
27:26	0h RO	Reserved.
25:24	0h RO	**Pad Ownership (PAD_OWN_GPD_6):** Same description as bit 0, except that the bit field applies to GPD_6.
23:22	0h RO	Reserved.
21:20	0h RO	**Pad Ownership (PAD_OWN_GPD_5):** Same description as bit 0, except that the bit field applies to GPD_5.
19:18	0h RO	Reserved.
17:16	0h RO	**Pad Ownership (PAD_OWN_GPD_4):** Same description as bit 0, except that the bit field applies to GPD_4.
15:14	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
13:12	0h RO	**Pad Ownership (PAD_OWN_GPD_3):** Same description as bit 0, except that the bit field applies to GPD_3.
11:10	0h RO	Reserved.
9:8	0h RO	**Pad Ownership (PAD_OWN_GPD_2):** Same description as bit 0, except that the bit field applies to GPD_2.
7:6	0h RO	Reserved.
5:4	0h RO	**Pad Ownership (PAD_OWN_GPD_1):** Same description as bit 0, except that the bit field applies to GPD_1.
3:2	0h RO	Reserved.
1:0	0h RO	**Pad Ownership (PAD_OWN_GPD_0):** 00 = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. 01 = ME GPIO Mode. ME has ownership of the pad. 10 = ISH GPIO Mode.ME has ownership of the pad 11 = Reserved

29.3.5 Pad Ownership (PAD_OWN_GPD_1)—Offset 24h

Same description as PAD_OWN_GPP_GPD_0, except that this register is for GPD[11:8]

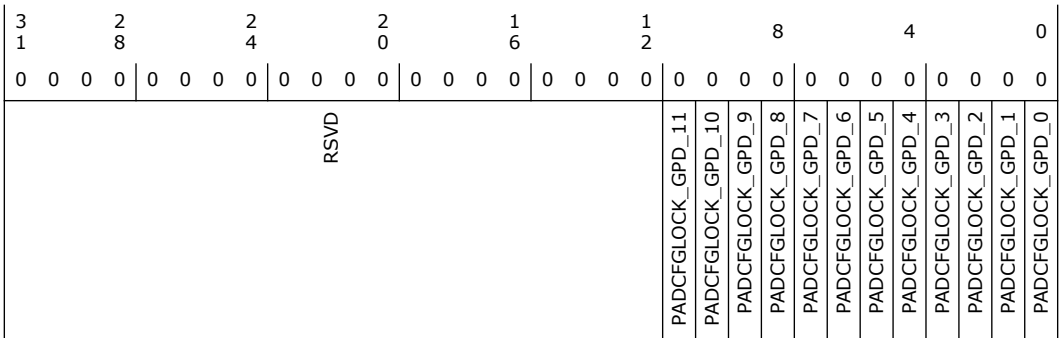
29.3.6 Pad Configuration Lock (PADCFGLOCK_GPD_0)—Offset A0h

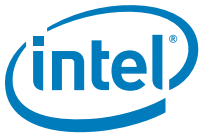
Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h





Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	Reserved.
11	0h RW	**Pad Config Lock (PADCFGLOCK_GPD_11):** Applied to GPD_11. Same description as bit 0.
10	0h RW	**Pad Config Lock (PADCFGLOCK_GPD_10):** Applied to GPD_2. Same description as bit 0.
9	0h RW	**Pad Config Lock (PADCFGLOCK_GPD_9):** Applied to GPD_2. Same description as bit 0.
8	0h RW	**Pad Config Lock (PADCFGLOCK_GPD_8):** Applied to GPD_8. Same description as bit 0.
7	0h RW	**Pad Config Lock (PADCFGLOCK_GPD_7):** Applied to GPD_7. Same description as bit 0.
6	0h RW	**Pad Config Lock (PADCFGLOCK_GPD_6):** Applied to GPD_6. Same description as bit 0.
5	0h RW	**Pad Config Lock (PADCFGLOCK_GPD_5):** Applied to GPD_5. Same description as bit 0.
4	0h RW	**Pad Config Lock (PADCFGLOCK_GPD_4):** Applied to GPD_4. Same description as bit 0.
3	0h RW	**Pad Config Lock (PADCFGLOCK_GPD_3):** Applied to GPD_3. Same description as bit 0.
2	0h RW	**Pad Config Lock (PADCFGLOCK_GPD_2):** Applied to GPD_2. Same description as bit 0.
1	0h RW	**Pad Config Lock (PADCFGLOCK_GPD_1):** Applied to GPD_2. Same description as bit 0.
0	0h RW	**Pad Config Lock (PADCFGLOCK_GPD_0):** Pad Configuration Lock locks specific register fields in the GPP specific registers from being configured. The registers affected become Read-Only and software writes to these registers have no effect. 0 = Unlock 1 = Lock the following register fields as read-only (RO): - Pad Configuration registers (exclude GPIOTXState) - GPI_NMI_EN Register (if implemented) - GPI_SMI_EN Register (if implemented) - GPI_GPE_EN Register (if implemented) When PadCfgLock is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown.

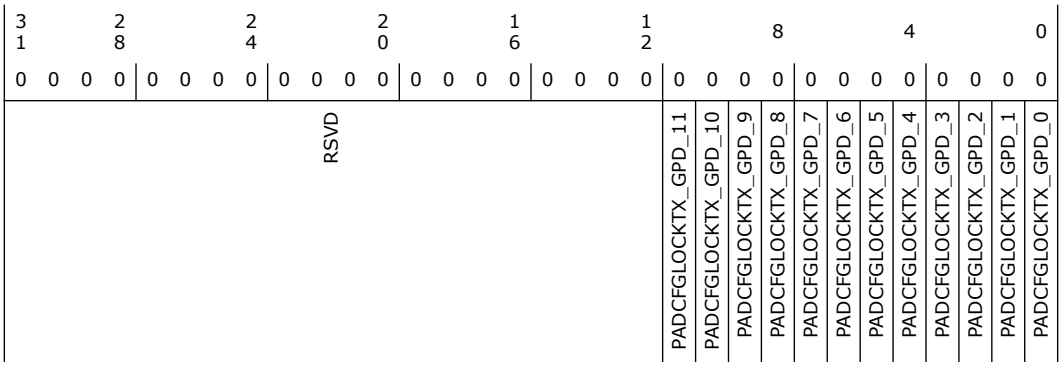
29.3.7 Pad Configuration Lock (PADCFGLOCKTX_GPD_0)—Offset A4h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	Reserved.
11	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPD_11):** Applied to GPD_11. Same description as bit 0.
10	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPD_10):** Applied to GPD_10. Same description as bit 0.
9	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPD_9):** Applied to GPD_9. Same description as bit 0.
8	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPD_8):** Applied to GPD_8. Same description as bit 0.
7	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPD_7):** Applied to GPD_7. Same description as bit 0.
6	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPD_6):** Applied to GPD_6. Same description as bit 0.
5	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPD_5):** Applied to GPD_5. Same description as bit 0.
4	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPD_4):** Applied to GPD_4. Same description as bit 0.
3	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPD_3):** Applied to GPD_3. Same description as bit 0.
2	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPD_2):** Applied to GPD_2. Same description as bit 0.
1	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPD_1):** Applied to GPD_1. Same description as bit 0.
0	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPD_0):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) When PadCfgLockTx is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown.

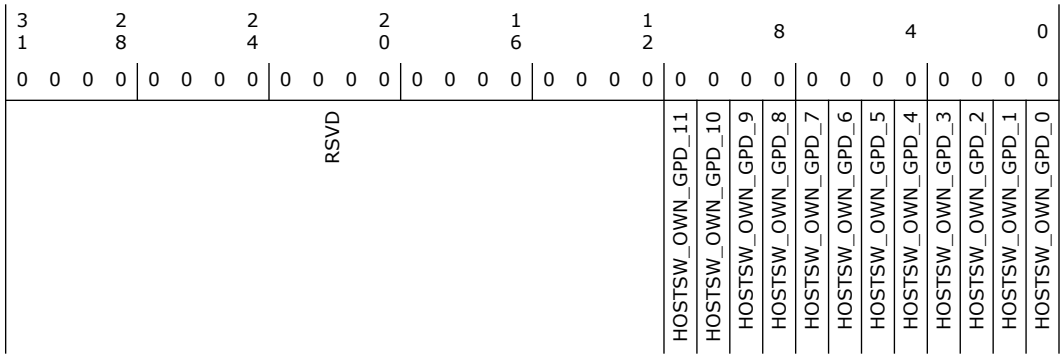
29.3.8 Host Software Pad Ownership (HOSTSW_OWN_GPD_0)—Offset D0h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	Reserved.
11	0h RW	**HostSW_Own (HOSTSW_OWN_GPD_11):** Applied to GPD_11. Same description as bit 0.
10	0h RW	**HostSW_Own (HOSTSW_OWN_GPD_10):** Applied to GPD_10. Same description as bit 0.
9	0h RW	**HostSW_Own (HOSTSW_OWN_GPD_9):** Applied to GPD_9. Same description as bit 0.
8	0h RW	**HostSW_Own (HOSTSW_OWN_GPD_8):** Applied to GPD_8. Same description as bit 0.
7	0h RW	**HostSW_Own (HOSTSW_OWN_GPD_7):** Applied to GPD_7. Same description as bit 0.
6	0h RW	**HostSW_Own (HOSTSW_OWN_GPD_6):** Applied to GPD_6. Same description as bit 0.
5	0h RW	**HostSW_Own (HOSTSW_OWN_GPD_5):** Applied to GPD_5. Same description as bit 0.
4	0h RW	**HostSW_Own (HOSTSW_OWN_GPD_4):** Applied to GPD_4. Same description as bit 0.
3	0h RW	**HostSW_Own (HOSTSW_OWN_GPD_3):** Applied to GPD_3. Same description as bit 0.
2	0h RW	**HostSW_Own (HOSTSW_OWN_GPD_2):** Applied to GPD_2. Same description as bit 0.
1	0h RW	**HostSW_Own (HOSTSW_OWN_GPD_1):** Applied to GPD_1. Same description as bit 0.
0	0h RW	**HostSW_Own (HOSTSW_OWN_GPD_0):** This register determines the appropriate host status bit update when a pad is under host ownership. 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked.

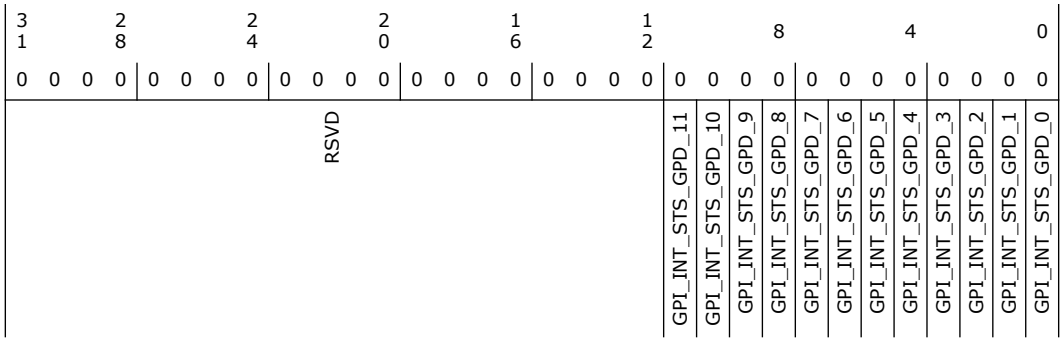
29.3.9 GPI Interrupt Status (GPI_IS_GPD_0)—Offset 100h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	Reserved.
11	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPD_11):** Applied to GPD_11. Same description as bit 0.
10	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPD_10):** Applied to GPD_10. Same description as bit 0.
9	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPD_9):** Applied to GPD_9. Same description as bit 0.
8	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPD_8):** Applied to GPD_8. Same description as bit 0.
7	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPD_7):** Applied to GPD_7. Same description as bit 0.
6	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPD_6):** Applied to GPD_6. Same description as bit 0.
5	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPD_5):** Applied to GPD_5. Same description as bit 0.
4	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPD_4):** Applied to GPD_4. Same description as bit 0.
3	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPD_3):** Applied to GPD_3. Same description as bit 0.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPD_2):** Applied to GPD_2. Same description as bit 0.
1	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPD_1):** Applied to GPD_1. Same description as bit 0.
0	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPD_0):** GPI Interrupt Status (GPI_INT_STS) This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: - The corresponding pad is used in GPIO input mode - HOSTSW_OWN = 1 (i.e. Host GPIO Driver Mode). Writing a value of 1 will clear the bit while writing a value of 0 has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN does not prevent the setting of GPI_INT_STS.

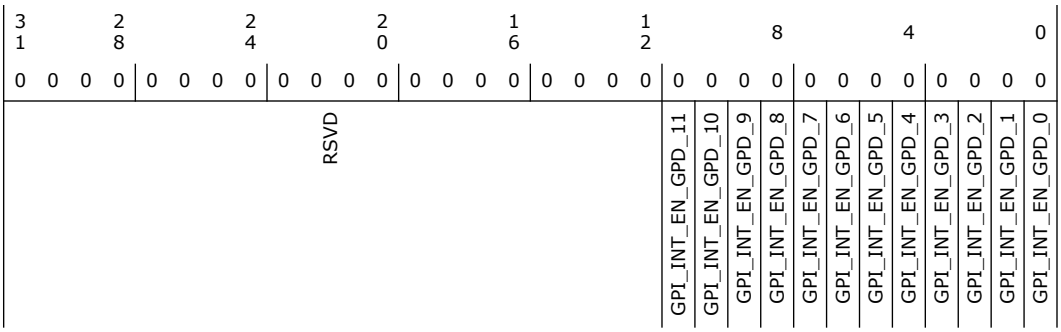
29.3.10 GPI Interrupt Enable (GPI_IE_GPD_0)—Offset 120h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	Reserved.
11	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPD_11):** Applied to GPD_11. Same description as bit 0.
10	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPD_10):** Applied to GPD_10. Same description as bit 0.
9	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPD_9):** Applied to GPD_9. Same description as bit 0.
8	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPD_8):** Applied to GPD_8. Same description as bit 0.
7	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPD_7):** Applied to GPD_7. Same description as bit 0.
6	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPD_6):** Applied to GPD_6. Same description as bit 0.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPD_5):** Applied to GPD_5. Same description as bit 0.
4	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPD_4):** Applied to GPD_4. Same description as bit 0.
3	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPD_3):** Applied to GPD_3. Same description as bit 0.
2	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPD_2):** Applied to GPD_2. Same description as bit 0.
1	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPD_1):** Applied to GPD_1. Same description as bit 0.
0	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPD_0):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing.

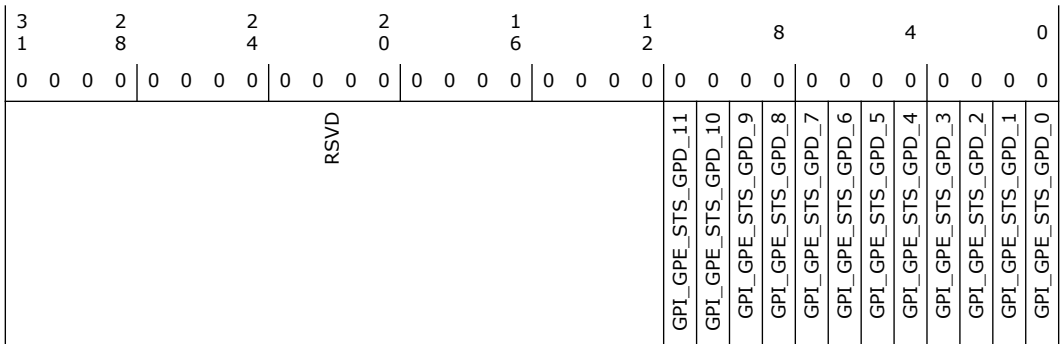
29.3.11 GPI General Purpose Events Status (GPI_GPE_STS_GPD_0)—Offset 140h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	Reserved.
11	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPD_11):** Applied to GPD_11. Same description as bit 0.
10	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPD_10):** Applied to GPD_10. Same description as bit 0.
9	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPD_9):** Applied to GPD_9. Same description as bit 0.
8	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPD_8):** Applied to GPD_8. Same description as bit 0.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPD_7):** Applied to GPD_7. Same description as bit 0.
6	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPD_6):** Applied to GPD_6. Same description as bit 0.
5	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPD_5):** Applied to GPD_5. Same description as bit 0.
4	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPD_4):** Applied to GPD_4. Same description as bit 0.
3	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPD_3):** Applied to GPD_3. Same description as bit 0.
2	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPD_2):** Applied to GPD_2. Same description as bit 0.
1	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPD_1):** Applied to GPD_1. Same description as bit 0.
0	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPD_0):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high(or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS bit is set: - If the system is in an S3-S5 state, the event will also wake the system. - If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN does not prevent the setting of GPI_GPE_STS.

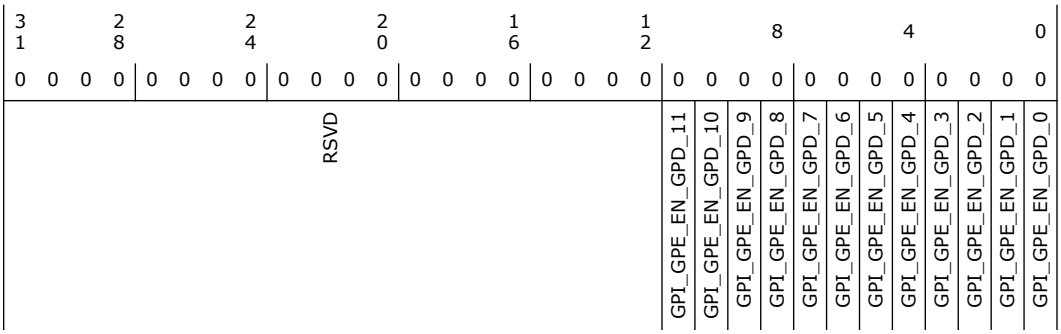
29.3.12 GPI General Purpose Events Enable (GPI_GPE_EN_GPD_0)—Offset 160h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	Reserved.
11	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPD_11):** Applied to GPD_11. Same description as bit 0.
10	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPD_10):** Applied to GPD_10. Same description as bit 0.
9	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPD_9):** Applied to GPD_9. Same description as bit 0.
8	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPD_8):** Applied to GPD_8. Same description as bit 0.
7	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPD_7):** Applied to GPD_7. Same description as bit 0.
6	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPD_6):** Applied to GPD_6. Same description as bit 0.
5	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPD_5):** Applied to GPD_5. Same description as bit 0.
4	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPD_4):** Applied to GPD_4. Same description as bit 0.
3	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPD_3):** Applied to GPD_3. Same description as bit 0.
2	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPD_2):** Applied to GPD_2. Same description as bit 0.
1	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPD_1):** Applied to GPD_1. Same description as bit 0.
0	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPD_0):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'.

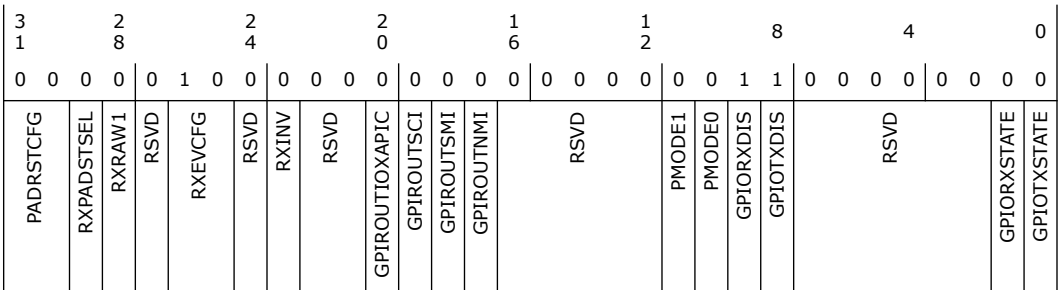
29.3.13 Pad Configuration DW0 (PAD_CFG_DW0_GPD_0)—Offset 400h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 4000X00h



Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset GPIO pad register fields in PAD_CFG_DW0 and PAD_CFG_DW1 registers. This register can be used for Sx isolation of the associated signal if needed. 00 = DSW_PWROK 01 = Host deep reset. This reset occurs when a host reset (with or without power cycle) is initiated or a global reset is initiated, except that the reset does not assert when in S3/S4/S5. 10 = PLTRST# 11 = RSMRST#
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determines from which node the RX pad state for native function should be taken from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from RX buffer 1 = Internal RX pad state (subject to RXINV and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field is only applicable when the RX buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	Reserved.
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determines if the internal RX pad state (synchronized, filtered vs non-filtered version as determined by PreGfRXSel, and is further subject to RXInv) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller . 0h = Level 1h = Edge 2h = Drive '0' 3h = Reserved (implement as setting 0h)
24	0h RO	Reserved.
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field is only applicable when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RO	Reserved.
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determines if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determines if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI. 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s).
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determines if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s). This bit only applies to a GPIO that has SMI capability. Otherwise, the bit is RO.
17	0h RW	**GPIO Input Route NMI (GPIROUTNMI):** Determines if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit. This bit only applies to a GPIO that has NMI capability. Otherwise, the bit is RO.
16:12	0h RO	Reserved.
11	-- RW	**Pad Mode bit 1 (PMODE1):** See description of Pad Mode bit 0.
10	-- RW	**Pad Mode bit 0 (PMODE0):** This bit is used in conjunction with Pad Mode bit 1. This two-bit field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad. 1h = native function 1, if applicable, controls the Pad 2h = native function 2, if applicable, controls the Pad. Also used to enable the GPIO blink (PWM) capability if applicable (note that not all GPIOs have the blink capability) 3h = native function 3, if applicable, controls the Pad Dedicated (unmuxed) GPIO shall report RO of all 0's in this register field If GPIO vs. native mode is configured via soft strap, this bit has no effect. Default value is determined by the default functionality of the pad.
9	1h RW	**GPIO RX Disable (GPIORXDIS):** 0 = Enable the input buffer (active low enable) of the pad. 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0'.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** 0 = Enable the output buffer (active low enable) of the pad. 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	Reserved.
1	0h RO	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV settings.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** 0 = Drive a level '0' to the TX output pad. 1 = Drive a level '1' to the TX output pad

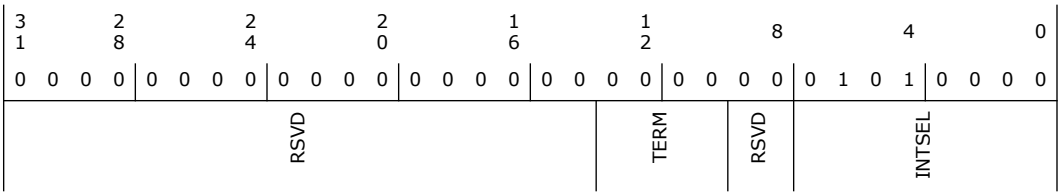
29.3.14 Pad Configuration DW1 (PAD_CFG_DW1_GPD_0)—Offset 404h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 50h



Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings for [13:10] correspond to: 0000: none 0010: 5k pd 0100: 20k pd 1010: 5k pu 1100: 20k pu 1111: Native controller selected by Pad Mode controls the Termination. This setting needs to be set only for GPP_A1 / LAD0, GPP_A2 / LAD1, GPP_A3 / LAD2, GPP_A4 / LAD3, GPD1 / ACPRESENT, and GPD2 / LAN_WAKE#, when the signals are used as native function. Otherwise, the setting is reserved. All others settings not mentioned above are reserved. If a reserved value is programmed, pad may malfunction. The setting of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in sw/fw in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, pu/pd settings should be programmed first to ensure the input does not float momentarily.
9:8	0h RO	Reserved.
7:0	50h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 .... Up to the max IOxAPIC IRQ supported

29.3.15 Pad Configuration DW0 (PAD_CFG_DW0_GPD_1)—Offset 408h

Same description as PAD_CFG_DW0_GPD_0.

29.3.16 Pad Configuration DW1 (PAD_CFG_DW1_GPD_1)—Offset 40Ch

Same description as PAD_CFG_DW1_GPD_0.
Exception:
INTSEL bit field default: 51h
TERM bit default: 1111b

29.3.17 Pad Configuration DW0 (PAD_CFG_DW0_GPD_2)—Offset 410h

Same description as PAD_CFG_DW0_GPD_0.

29.3.18 Pad Configuration DW1 (PAD_CFG_DW1_GPD_2)—Offset 414h

Same description as PAD_CFG_DW1_GPD_0.
Exception:
INTSEL bit field default: 52h
TERM bit default: 1111b

29.3.19 Pad Configuration DW0 (PAD_CFG_DW0_GPD_3)—Offset 418h

Same description as PAD_CFG_DW0_GPD_0.

29.3.20 Pad Configuration DW1 (PAD_CFG_DW1_GPD_3)—Offset 41Ch

Same description as PAD_CFG_DW1_GPD_0.
Exception:
INTSEL bit field default: 53h
TERM bit default: 1100b

29.3.21 Pad Configuration DW0 (PAD_CFG_DW0_GPD_4)—Offset 420h

Same description as PAD_CFG_DW0_GPD_0.

29.3.22 Pad Configuration DW1 (PAD_CFG_DW1_GPD_4)—Offset 424h

Same description as PAD_CFG_DW1_GPD_0. Exception: The default value of the INTSEL bit field in this register is: 54h

29.3.23 Pad Configuration DW0 (PAD_CFG_DW0_GPD_5)—Offset 428h

Same description as PAD_CFG_DW0_GPD_0.

29.3.24 Pad Configuration DW1 (PAD_CFG_DW1_GPD_5)—Offset 42Ch

Same description as PAD_CFG_DW1_GPD_0. Exception: The default value of the INTSEL bit field in this register is: 55h

29.3.25 Pad Configuration DW0 (PAD_CFG_DW0_GPD_6)—Offset 430h

Same description as PAD_CFG_DW0_GPD_0.

29.3.26 Pad Configuration DW1 (PAD_CFG_DW1_GPD_6)—Offset 434h

Same description as PAD_CFG_DW1_GPD_0. Exception: The default value of the INTSEL bit field in this register is: 56h

29.3.27 Pad Configuration DW0 (PAD_CFG_DW0_GPD_7)—Offset 438h

Same description as PAD_CFG_DW0_GPD_0.

29.3.28 Pad Configuration DW1 (PAD_CFG_DW1_GPD_7)—Offset 43Ch

Same description as PAD_CFG_DW1_GPD_0. Exception: The default value of the INTSEL bit field in this register is: 57h

29.3.29 Pad Configuration DW0 (PAD_CFG_DW0_GPD_8)—Offset 440h

Same description as PAD_CFG_DW0_GPD_0.

29.3.30 Pad Configuration DW1 (PAD_CFG_DW1_GPD_8)—Offset 444h

Same description as PAD_CFG_DW1_GPD_0. Exception: The default value of the INTSEL bit field in this register is: 58h

29.3.31 Pad Configuration DW0 (PAD_CFG_DW0_GPD_9)—Offset 448h

Same description as PAD_CFG_DW0_GPD_0.

29.3.32 Pad Configuration DW1 (PAD_CFG_DW1_GPD_9)—Offset 44Ch

Same description as PAD_CFG_DW1_GPD_0. Exception: The default value of the INTSEL bit field in this register is: 59h

29.3.33 Pad Configuration DW0 (PAD_CFG_DW0_GPD_10)—Offset 450h

Same description as PAD_CFG_DW0_GPD_0.

29.3.34 Pad Configuration DW1 (PAD_CFG_DW1_GPD_10)—Offset 454h

Same description as PAD_CFG_DW1_GPD_0. Exception: The default value of the INTSEL bit field in this register is: 5Ah

29.3.35 Pad Configuration DW0 (PAD_CFG_DW0_GPD_11)—Offset 458h

Same description as PAD_CFG_DW0_GPD_0.

29.3.36 Pad Configuration DW1 (PAD_CFG_DW1_GPD_11)—Offset 45Ch

Same description as PAD_CFG_DW1_GPD_0. Exception: The default value of the INTSEL bit field in this register is: 5Bh

29.4 GPIO Community 3 Registers Summary

Community 3 Registers are for GPP_F and GPP_G groups.

These registers are within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID + Register Offset).

Table 29-4. Summary of GPIO Community 3 Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
8h	Bh	Family Base Address (FAMBAR)—Offset 8h	300h
Ch	Fh	Pad Base Address (PADBAR)—Offset Ch	400h
10h	13h	Miscellaneous Configuration (MISCCFG)—Offset 10h	43200h
20h	23h	Pad Ownership (PAD_OWN_GPP_F_0)—Offset 20h	0h
24h	27h	Pad Ownership (PAD_OWN_GPP_F_1)—Offset 24h	0h
28h	2Bh	Pad Ownership (PAD_OWN_GPP_F_2)—Offset 28h	0h
30h	33h	Pad Ownership (PAD_OWN_GPP_G_0)—Offset 30h	0h
A0h	A3h	Pad Configuration Lock (PADCFGLOCK_GPP_F)—Offset A0h	0h
A4h	A7h	Pad Configuration Lock (PADCFGLOCKTX_GPP_F)—Offset A4h	0h
A8h	ABh	Pad Configuration Lock (PADCFGLOCK_GPP_G)—Offset A8h	0h
ACh	AFh	Pad Configuration Lock (PADCFGLOCKTX_GPP_G)—Offset ACh	0h
D0h	D3h	Host Software Pad Ownership (HOSTSW_OWN_GPP_F)—Offset D0h	0h
D4h	D7h	Host Software Pad Ownership (HOSTSW_OWN_GPP_G)—Offset D4h	0h
100h	103h	GPI Interrupt Status (GPI_IS_GPP_F)—Offset 100h	0h
104h	107h	GPI Interrupt Status (GPI_IS_GPP_G)—Offset 104h	0h
120h	123h	GPI Interrupt Enable (GPI_IE_GPP_F)—Offset 120h	0h
124h	127h	GPI Interrupt Enable (GPI_IE_GPP_G)—Offset 124h	0h
140h	143h	GPI General Purpose Events Status (GPI_GPE_STS_GPP_F)—Offset 140h	0h
144h	147h	GPI General Purpose Events Status (GPI_GPE_STS_GPP_G)—Offset 144h	0h
160h	163h	GPI General Purpose Events Enable (GPI_GPE_EN_GPP_F)—Offset 160h	0h
164h	167h	GPI General Purpose Events Enable (GPI_GPE_EN_GPP_G)—Offset 164h	0h

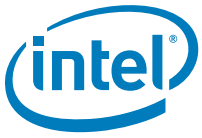


Table 29-4. Summary of GPIO Community 3 Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
400h	403h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_0)—Offset 400h	44000X00h See register for X value
404h	407h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_0)—Offset 404h	30h
408h	40Bh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_1)—Offset 408h	44000X00h See register for X value
40Ch	40Fh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_1)—Offset 40Ch	See register
410h	413h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_2)—Offset 410h	44000X00h See register for X value
414h	417h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_2)—Offset 414h	See register
418h	41Bh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_3)—Offset 418h	44000X00h See register for X value
41Ch	41Fh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_3)—Offset 41Ch	See register
420h	423h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_4)—Offset 420h	44000X00h See register for X value
424h	427h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_4)—Offset 424h	See register
428h	42Bh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_5)—Offset 428h	44000X00h See register for X value
42Ch	42Fh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_5)—Offset 42Ch	See register
430h	433h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_6)—Offset 430h	44000X00h See register for X value
434h	437h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_6)—Offset 434h	See register
438h	43Bh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_7)—Offset 438h	44000X00h See register for X value
43Ch	43Fh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_7)—Offset 43Ch	See register
440h	443h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_8)—Offset 440h	44000X00h See register for X value
444h	447h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_8)—Offset 444h	See register
448h	44Bh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_9)—Offset 448h	44000X00h See register for X value
44Ch	44Fh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_9)—Offset 44Ch	See register
450h	453h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_10)—Offset 450h	44000X00h See register for X value
454h	457h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_10)—Offset 454h	See register
458h	45Bh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_11)—Offset 458h	44000X00h See register for X value
45Ch	45Fh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_11)—Offset 45Ch	See register
460h	463h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_12)—Offset 460h	44000X00h See register for X value

Table 29-4. Summary of GPIO Community 3 Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
464h	467h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_12)—Offset 464h	See register
468h	46Bh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_13)—Offset 468h	44000X00h See register for X value
46Ch	46Fh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_13)—Offset 46Ch	See register
470h	473h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_14)—Offset 470h	44000X00h See register for X value
474h	477h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_14)—Offset 474h	See register
478h	47Bh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_15)—Offset 478h	44000X00h See register for X value
47Ch	47Fh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_15)—Offset 47Ch	See register
480h	483h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_16)—Offset 480h	44000X00h See register for X value
484h	487h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_16)—Offset 484h	See register
488h	48Bh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_17)—Offset 488h	44000X00h See register for X value
48Ch	48Fh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_17)—Offset 48Ch	See register
490h	493h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_18)—Offset 490h	44000X00h See register for X value
494h	497h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_18)—Offset 494h	See register
498h	49Bh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_19)—Offset 498h	44000X00h See register for X value
49Ch	49Fh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_19)—Offset 49Ch	See register
4A0h	4A3h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_20)—Offset 4A0h	44000X00h See register for X value
4A4h	4A7h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_20)—Offset 4A4h	See register
4A8h	4ABh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_21)—Offset 4A8h	44000X00h See register for X value
4ACh	4AFh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_21)—Offset 4ACh	See register
4B0h	4B3h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_22)—Offset 4B0h	44000X00h See register for X value
4B4h	4B7h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_22)—Offset 4B4h	See register
4B8h	4BBh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_23)—Offset 4B8h	44000X00h See register for X value
4BCh	4BFh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_23)—Offset 4BCh	See register
4C0h	4C3h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_G_0)—Offset 4C0h	44000X00h See register for X value
4C4h	4C7h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_G_0)—Offset 4C4h	See register

Table 29-4. Summary of GPIO Community 3 Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
4C8h	4CBh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_G_1)—Offset 4C8h	44000X00h See register for X value
4CCh	4CFh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_G_1)—Offset 4CCh	See register
4D0h	4D3h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_G_2)—Offset 4D0h	44000X00h See register for X value
4D4h	4D7h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_G_2)—Offset 4D4h	See register
4D8h	4DBh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_G_3)—Offset 4D8h	44000X00h See register for X value
4DCh	4DFh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_G_3)—Offset 4DCh	See register
4E0h	4E3h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_G_4)—Offset 4E0h	44000X00h See register for X value
4E4h	4E7h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_G_4)—Offset 4E4h	See register
4E8h	4EBh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_G_5)—Offset 4E8h	44000X00h See register for X value
4ECh	4EFh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_G_5)—Offset 4ECh	See register
4F0h	4F3h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_G_6)—Offset 4F0h	44000X00h See register for X value
4F4h	4F7h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_G_6)—Offset 4F4h	See register
4F8h	4FBh	Pad Configuration DW0 (PAD_CFG_DW0_GPP_G_7)—Offset 4F8h	44000X00h See register for X value
4FCh	4FFh	Pad Configuration DW1 (PAD_CFG_DW1_GPP_G_7)—Offset 4FCh	See register

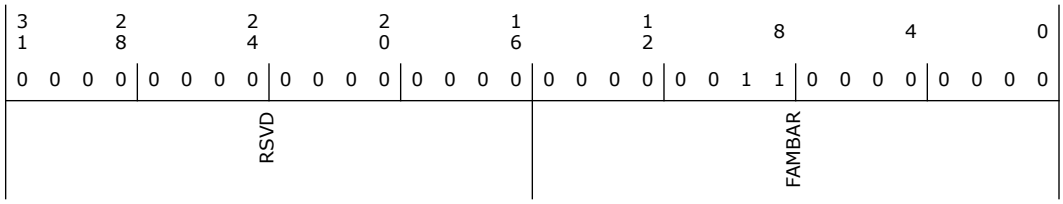
29.4.1 Family Base Address (FAMBAR)—Offset 8h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 300h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	300h RO	**Family Base Address (FAMBAR):** Family Base Address (FAMBAR) This field provides the starting byte-align address of Family0 register sets within a Community. It is meant for software to discover from where the very first Family register (i.e. Family0 register) starts to compute the next Families address offsets.

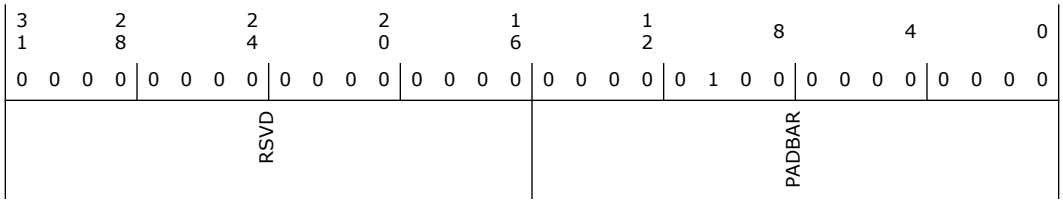
29.4.2 Pad Base Address (PADBAR)—Offset Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 400h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	400h RO	**Pad Base Address (PADBAR):** This field provides the starting byte-align address of Pad0 register sets. It is meant for software to discover from where the very first Pad register (i.e. Pad0 register) starts to compute the next Pad address offsets.

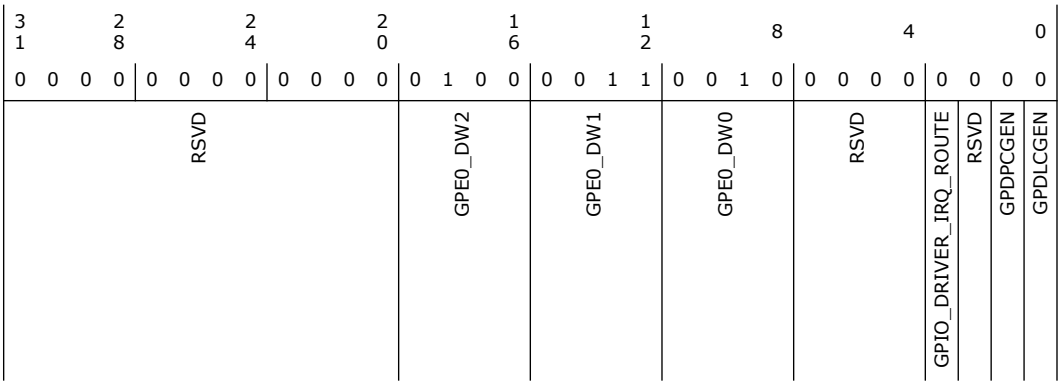
29.4.3 Miscellaneous Configuration (MISCCFG)—Offset 10h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 43200h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	Reserved.
19:16	4h RW	**GPIO Group to GPE_DW0 assignment encoding (GPE0_DW2):** This register assigns a specific GPIO Group to the ACPI GPE0[95:64]. The selected GPIO group will be mapped to lower bits of the GPE register 0h = GPP_A[23:0] mapped to GPE[87:64]; GPE[95:88] not used. 1h = GPP_B[23:0] mapped to GPE[87:64]; GPE[95:88] not used. 2h = GPP_C[23:0] mapped to GPE[87:64]; GPE[95:88] not used. 3h = GPP_D[23:0] mapped to GPE[87:64]; GPE[95:88] not used. 4h = GPP_E[23:0] mapped to GPE[87:64]; GPE[95:88] not used. 5h = GPP_F[23:0] mapped to GPE[87:64]; GPE[95:88] not used. 6h = GPP_G[7:0] mapped to GPE[51:64]; GPE[95:52] not used. 7h = GPD[11:0] mapped to GPE[75:64]; GPE[95:76] not used.
15:12	3h RW	**GPIO Group to GPE_DW0 assignment encoding (GPE0_DW1):** This register assigns a specific GPIO Group to the ACPI GPE0[63:32]. The selected GPIO group will be mapped to lower bits of the GPE register 0h = GPP_A[23:0] mapped to GPE[55:32]; GPE[63:56] not used. 1h = GPP_B[23:0] mapped to GPE[55:32]; GPE[63:56] not used. 2h = GPP_C[23:0] mapped to GPE[55:32]; GPE[63:56] not used. 3h = GPP_D[23:0] mapped to GPE[55:32]; GPE[63:56] not used. 4h = GPP_E[23:0] mapped to GPE[55:32]; GPE[63:56] not used. 5h = GPP_F[23:0] mapped to GPE[55:32]; GPE[63:56] not used. 6h = GPP_G[7:0] mapped to GPE[39:32]; GPE[63:40] not used. 7h = GPD[11:0] mapped to GPE[43:32]; GPE[63:44] not used.
11:8	2h RW	**GPIO Group to GPE_DW0 assignment encoding (GPE0_DW0):** This register assigns a specific GPIO Group to the ACPI GPE0[31:0]. The selected GPIO group will be mapped to lower bits of the GPE register 0h = GPP_A[23:0] mapped to GPE[23:0]; GPE[31:24] not used. 1h = GPP_B[23:0] mapped to GPE[23:0]; GPE[31:24] not used. 2h = GPP_C[23:0] mapped to GPE[23:0]; GPE[31:24] not used. 3h = GPP_D[23:0] mapped to GPE[23:0]; GPE[31:24] not used. 4h = GPP_E[23:0] mapped to GPE[23:0]; GPE[31:24] not used. 5h = GPP_F[23:0] mapped to GPE[23:0]; GPE[31:24] not used. 6h = GPP_G[7:0] mapped to GPE[7:0]; GPE[31:8] not used. 7h = GPD[11:0] mapped to GPE[11:0]; GPE[31:12] not used.
7:4	0h RO	Reserved.
3	0h RW	**GPIO Driver IRQ Route (GPIO_DRIVER_IRQ_ROUTE):** GPIO Driver IRQ_ROUTE[1:0]: Specifies the APIC IRQ globally for all pads within the current community (GPI_IS with corresponding GPI_IE enable). 0 = IRQ14 1 = IRQ15

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	Reserved.
1	0h RW	**GPIO Dynamic Partition Clock Gating Enable (GPDPCGEN):** Specifies whether the GPIO Community should take part in partition clock gating 0 = Disable participation in dynamic partition clock gating 1 = Enable participation in dynamic partition clock gating.
0	0h RW	**GPIO Dynamic Local Clock Gating Enable (GPDLCGEN):** Specifies whether the GPIO Community should perform local clock gating. 0 = Disable dynamic local clock gating 1 = Enable dynamic local clock gating.

29.4.4 Pad Ownership (PAD_OWN_GPP_F_0)—Offset 20h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD		PAD_OWN_GPP_F_7		RSVD		PAD_OWN_GPP_F_6		RSVD		PAD_OWN_GPP_F_5		RSVD		PAD_OWN_GPP_F_4		RSVD		PAD_OWN_GPP_F_3		RSVD		PAD_OWN_GPP_F_2		RSVD		PAD_OWN_GPP_F_1		RSVD		PAD_OWN_GPP_F_0	

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29:28	0h RO	**Pad Ownership (PAD_OWN_GPP_F_7):** Same description as bit 0, except that the bit field applies to GPP_F7.
27:26	0h RO	Reserved.
25:24	0h RO	**Pad Ownership (PAD_OWN_GPP_F_6):** Same description as bit 0, except that the bit field applies to GPP_F6.
23:22	0h RO	Reserved.
21:20	0h RO	**Pad Ownership (PAD_OWN_GPP_F_5):** Same description as bit 0, except that the bit field applies to GPP_F5.
19:18	0h RO	Reserved.
17:16	0h RO	**Pad Ownership (PAD_OWN_GPP_F_4):** Same description as bit 0, except that the bit field applies to GPP_F4.

Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RO	Reserved.
13:12	0h RO	**Pad Ownership (PAD_OWN_GPP_F_3):** Same description as bit 0, except that the bit field applies to GPP_F3.
11:10	0h RO	Reserved.
9:8	0h RO	**Pad Ownership (PAD_OWN_GPP_F_2):** Same description as bit 0, except that the bit field applies to GPP_F2.
7:6	0h RO	Reserved.
5:4	0h RO	**Pad Ownership (PAD_OWN_GPP_F_1):** Same description as bit 0, except that the bit field applies to GPP_F1.
3:2	0h RO	Reserved.
1:0	0h RO	**Pad Ownership (PAD_OWN_GPP_F_0):** 00 = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. 01 = ME GPIO Mode. ME has ownership of the pad. 10 = ISH GPIO Mode.ME has ownership of the pad 11 = Reserved

29.4.5 Pad Ownership (PAD_OWN_GPP_F_1)—Offset 24h

Same description as PAD_OWN_GPP_F_0, except that this register is for GPP_F[15:8]

29.4.6 Pad Ownership (PAD_OWN_GPP_F_2)—Offset 28h

Same description as PAD_OWN_GPP_F_0, except that this register is for GPP_F[23:16]

29.4.7 Pad Ownership (PAD_OWN_GPP_G_0)—Offset 30h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD	PAD_OWN_GPP_G_7			RSVD	PAD_OWN_GPP_G_6			RSVD	PAD_OWN_GPP_G_5			RSVD	PAD_OWN_GPP_G_4			RSVD	PAD_OWN_GPP_G_3			RSVD	PAD_OWN_GPP_G_2			RSVD	PAD_OWN_GPP_G_1			RSVD	PAD_OWN_GPP_G_0		

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29:28	0h RO	**Pad Ownership (PAD_OWN_GPP_G_7):** Same description as bit 0, except that the bit field applies to GPP_G7.
27:26	0h RO	Reserved.
25:24	0h RO	**Pad Ownership (PAD_OWN_GPP_G_6):** Same description as bit 0, except that the bit field applies to GPP_G6.
23:22	0h RO	Reserved.
21:20	0h RO	**Pad Ownership (PAD_OWN_GPP_G_5):** Same description as bit 0, except that the bit field applies to GPP_G5.
19:18	0h RO	Reserved.
17:16	0h RO	**Pad Ownership (PAD_OWN_GPP_G_4):** Same description as bit 0, except that the bit field applies to GPP_G4.
15:14	0h RO	Reserved.
13:12	0h RO	**Pad Ownership (PAD_OWN_GPP_G_3):** Same description as bit 0, except that the bit field applies to GPP_G3.
11:10	0h RO	Reserved.
9:8	0h RO	**Pad Ownership (PAD_OWN_GPP_G_2):** Same description as bit 0, except that the bit field applies to GPP_G2.
7:6	0h RO	Reserved.
5:4	0h RO	**Pad Ownership (PAD_OWN_GPP_G_1):** Same description as bit 0, except that the bit field applies to GPP_G1.
3:2	0h RO	Reserved.
1:0	0h RO	**Pad Ownership (PAD_OWN_GPP_G_0):** 00 = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. 01 = ME GPIO Mode. ME has ownership of the pad. 10 = ISH GPIO Mode.ME has ownership of the pad 11 = Reserved

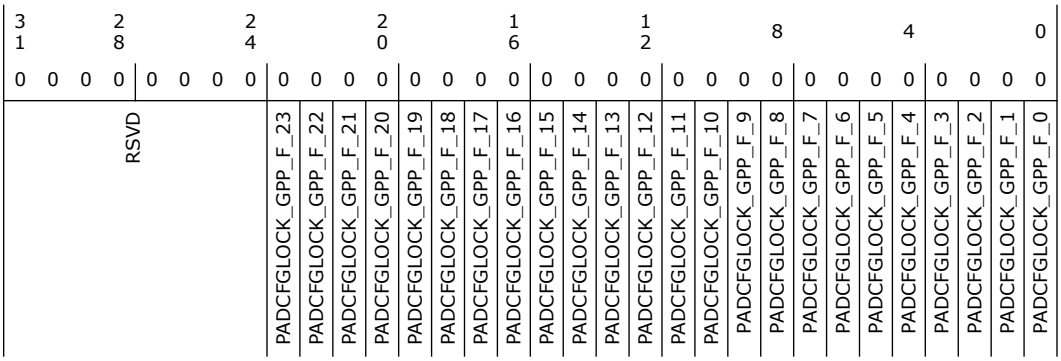
29.4.8 Pad Configuration Lock (PADCFGLOCK_GPP_F)—Offset A0h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_F_23):** Applied to GPP_F23. Same description as bit 0.
22	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_F_22):** Applied to GPP_F22. Same description as bit 0.
21	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_F_21):** Applied to GPP_F21. Same description as bit 0.
20	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_F_20):** Applied to GPP_F20. Same description as bit 0.
19	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_F_19):** Applied to GPP_F19. Same description as bit 0.
18	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_F_18):** Applied to GPP_F18. Same description as bit 0.
17	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_F_17):** Applied to GPP_F17. Same description as bit 0.
16	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_F_16):** Applied to GPP_F16. Same description as bit 0.
15	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_F_15):** Applied to GPP_F15. Same description as bit 0.
14	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_F_14):** Applied to GPP_F14. Same description as bit 0.
13	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_F_13):** Applied to GPP_F13. Same description as bit 0.
12	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_F_12):** Applied to GPP_F12. Same description as bit 0.
11	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_F_11):** Applied to GPP_F11. Same description as bit 0.
10	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_F_10):** Applied to GPP_F10. Same description as bit 0.
9	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_F_9):** Applied to GPP_F9. Same description as bit 0.
8	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_F_8):** Applied to GPP_F8. Same description as bit 0.
7	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_F_7):** Applied to GPP_F7. Same description as bit 0.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_F_6):** Applied to GPP_F6. Same description as bit 0.
5	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_F_5):** Applied to GPP_F5. Same description as bit 0.
4	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_F_4):** Applied to GPP_F4. Same description as bit 0.
3	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_F_3):** Applied to GPP_F3. Same description as bit 0.
2	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_F_2):** Applied to GPP_F2. Same description as bit 0.
1	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_F_1):** Applied to GPP_F1. Same description as bit 0.
0	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_F_0):** Pad Configuration Lock locks specific register fields in the GPP specific registers from being configured. The registers affected become Read-Only and software writes to these registers have no effect. 0 = Unlock 1 = Lock the following register fields as read-only (RO): - Pad Configuration registers (exclude GPIOTXState) - GPI_NMI_EN Register (if implemented) - GPI_SMI_EN Register (if implemented) - GPI_GPE_EN Register (if implemented) When PadCfgLock is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown.

29.4.9 Pad Configuration Lock (PADCFGLOCKTX_GPP_F)—Offset A4h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
RSVD		PADCFGLOCKTX_GPP_F_23	PADCFGLOCKTX_GPP_F_22	PADCFGLOCKTX_GPP_F_21	PADCFGLOCKTX_GPP_F_20	PADCFGLOCKTX_GPP_F_19	PADCFGLOCKTX_GPP_F_18	PADCFGLOCKTX_GPP_F_17	PADCFGLOCKTX_GPP_F_16	PADCFGLOCKTX_GPP_F_15	PADCFGLOCKTX_GPP_F_14	PADCFGLOCKTX_GPP_F_13	PADCFGLOCKTX_GPP_F_12	PADCFGLOCKTX_GPP_F_11	PADCFGLOCKTX_GPP_F_10	PADCFGLOCKTX_GPP_F_9	PADCFGLOCKTX_GPP_F_8	PADCFGLOCKTX_GPP_F_7	PADCFGLOCKTX_GPP_F_6	PADCFGLOCKTX_GPP_F_5	PADCFGLOCKTX_GPP_F_4	PADCFGLOCKTX_GPP_F_3	PADCFGLOCKTX_GPP_F_2	PADCFGLOCKTX_GPP_F_1	PADCFGLOCKTX_GPP_F_0

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_F_23):** Applied to GPP_F23. Same description as bit 0.
22	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_F_22):** Applied to GPP_F22. Same description as bit 0.
21	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_F_21):** Applied to GPP_F21. Same description as bit 0.
20	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_F_20):** Applied to GPP_F20. Same description as bit 0.
19	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_F_19):** Applied to GPP_F19. Same description as bit 0.
18	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_F_18):** Applied to GPP_F18. Same description as bit 0.
17	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_F_17):** Applied to GPP_F17. Same description as bit 0.
16	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_F_16):** Applied to GPP_F16. Same description as bit 0.
15	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_F_15):** Applied to GPP_F15. Same description as bit 0.
14	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_F_14):** Applied to GPP_F14. Same description as bit 0.
13	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_F_13):** Applied to GPP_F13. Same description as bit 0.
12	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_F_12):** Applied to GPP_F12. Same description as bit 0.
11	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_F_11):** Applied to GPP_F11. Same description as bit 0.
10	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_F_10):** Applied to GPP_F10. Same description as bit 0.
9	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_F_9):** Applied to GPP_F9. Same description as bit 0.
8	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_F_8):** Applied to GPP_F8. Same description as bit 0.
7	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_F_7):** Applied to GPP_F7. Same description as bit 0.
6	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_F_6):** Applied to GPP_F6. Same description as bit 0.
5	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_F_5):** Applied to GPP_F5. Same description as bit 0.
4	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_F_4):** Applied to GPP_F4. Same description as bit 0.
3	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_F_3):** Applied to GPP_F3. Same description as bit 0.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_F_2):** Applied to GPP_F2. Same description as bit 0.
1	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_F_1):** Applied to GPP_F1. Same description as bit 0.
0	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_F_0):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) When PadCfgLockTx is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown.

29.4.10 Pad Configuration Lock (PADCFGLOCK_GPP_G)—Offset A8h

Same definition as PADCFGLOCK_GPP_F register, except this register applies to GPP_G group (GPP_G[7:0]). Bits corresponding to unimplemented GPP_G are reserved.

29.4.11 Pad Configuration Lock (PADCFGLOCKTX_GPP_G)—Offset ACh

Same definition as PADCFGLOCKTX_GPP_F register, except this register applies to GPP_G group (GPP_G[7:0]). Bits corresponding to unimplemented GPP_G are reserved.

29.4.12 Host Software Pad Ownership (HOSTSW_OWN_GPP_F)—Offset D0h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD								HOSTSW_OWN_GPP_F_23	HOSTSW_OWN_GPP_F_22	HOSTSW_OWN_GPP_F_21	HOSTSW_OWN_GPP_F_20	HOSTSW_OWN_GPP_F_19	HOSTSW_OWN_GPP_F_18	HOSTSW_OWN_GPP_F_17	HOSTSW_OWN_GPP_F_16	HOSTSW_OWN_GPP_F_15	HOSTSW_OWN_GPP_F_14	HOSTSW_OWN_GPP_F_13	HOSTSW_OWN_GPP_F_12	HOSTSW_OWN_GPP_F_11	HOSTSW_OWN_GPP_F_10	HOSTSW_OWN_GPP_F_9	HOSTSW_OWN_GPP_F_8	HOSTSW_OWN_GPP_F_7	HOSTSW_OWN_GPP_F_6	HOSTSW_OWN_GPP_F_5	HOSTSW_OWN_GPP_F_4	HOSTSW_OWN_GPP_F_3	HOSTSW_OWN_GPP_F_2	HOSTSW_OWN_GPP_F_1	HOSTSW_OWN_GPP_F_0

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_F_23):** Applied to GPP_F23. Same description as bit 0.
22	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_F_22):** Applied to GPP_F22. Same description as bit 0.
21	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_F_21):** Applied to GPP_F21. Same description as bit 0.
20	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_F_20):** Applied to GPP_F20. Same description as bit 0.
19	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_F_19):** Applied to GPP_F19. Same description as bit 0.
18	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_F_18):** Applied to GPP_F18. Same description as bit 0.
17	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_F_17):** Applied to GPP_F17. Same description as bit 0.
16	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_F_16):** Applied to GPP_F16. Same description as bit 0.
15	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_F_15):** Applied to GPP_F15. Same description as bit 0.
14	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_F_14):** Applied to GPP_F14. Same description as bit 0.
13	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_F_13):** Applied to GPP_F13. Same description as bit 0.
12	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_F_12):** Applied to GPP_F12. Same description as bit 0.
11	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_F_11):** Applied to GPP_F11. Same description as bit 0.
10	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_F_10):** Applied to GPP_F10. Same description as bit 0.
9	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_F_9):** Applied to GPP_F9. Same description as bit 0.
8	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_F_8):** Applied to GPP_F8. Same description as bit 0.
7	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_F_7):** Applied to GPP_F7. Same description as bit 0.
6	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_F_6):** Applied to GPP_F6. Same description as bit 0.
5	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_F_5):** Applied to GPP_F5. Same description as bit 0.
4	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_F_4):** Applied to GPP_F4. Same description as bit 0.
3	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_F_3):** Applied to GPP_F3. Same description as bit 0.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_F_2):** Applied to GPP_F2. Same description as bit 0.
1	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_F_1):** Applied to GPP_F1. Same description as bit 0.
0	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_F_0):** This register determines the appropriate host status bit update when a pad is under host ownership. 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked.

29.4.13 Host Software Pad Ownership (HOSTSW_OWN_GPP_G)—Offset D4h

Same definition as HOSTSW_OWN_GPP_F register, except this register applies to GPP_G group (GPP_G[7:0]). Bits corresponding to unimplemented GPP_G are reserved.

29.4.14 GPI Interrupt Status (GPI_IS_GPP_F)—Offset 100h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
RSVD	GPI_INT_STS_GPP_F_23	GPI_INT_STS_GPP_F_22	GPI_INT_STS_GPP_F_21	GPI_INT_STS_GPP_F_20	GPI_INT_STS_GPP_F_19	GPI_INT_STS_GPP_F_18	GPI_INT_STS_GPP_F_17	GPI_INT_STS_GPP_F_16
	GPI_INT_STS_GPP_F_15	GPI_INT_STS_GPP_F_14	GPI_INT_STS_GPP_F_13	GPI_INT_STS_GPP_F_12	GPI_INT_STS_GPP_F_11	GPI_INT_STS_GPP_F_10	GPI_INT_STS_GPP_F_9	GPI_INT_STS_GPP_F_8
	GPI_INT_STS_GPP_F_7	GPI_INT_STS_GPP_F_6	GPI_INT_STS_GPP_F_5	GPI_INT_STS_GPP_F_4	GPI_INT_STS_GPP_F_3	GPI_INT_STS_GPP_F_2	GPI_INT_STS_GPP_F_1	GPI_INT_STS_GPP_F_0

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_F_23):** Applied to GPP_F23. Same description as bit 0.
22	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_F_22):** Applied to GPP_F22. Same description as bit 0.
21	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_F_21):** Applied to GPP_F21. Same description as bit 0.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_F_20):** Applied to GPP_F20. Same description as bit 0.
19	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_F_19):** Applied to GPP_F19. Same description as bit 0.
18	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_F_18):** Applied to GPP_F18. Same description as bit 0.
17	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_F_17):** Applied to GPP_F17. Same description as bit 0.
16	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_F_16):** Applied to GPP_F16. Same description as bit 0.
15	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_F_15):** Applied to GPP_F15. Same description as bit 0.
14	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_F_14):** Applied to GPP_F14. Same description as bit 0.
13	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_F_13):** Applied to GPP_F13. Same description as bit 0.
12	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_F_12):** Applied to GPP_F12. Same description as bit 0.
11	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_F_11):** Applied to GPP_F11. Same description as bit 0.
10	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_F_10):** Applied to GPP_F10. Same description as bit 0.
9	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_F_9):** Applied to GPP_F9. Same description as bit 0.
8	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_F_8):** Applied to GPP_F8. Same description as bit 0.
7	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_F_7):** Applied to GPP_F7. Same description as bit 0.
6	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_F_6):** Applied to GPP_F6. Same description as bit 0.
5	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_F_5):** Applied to GPP_F5. Same description as bit 0.
4	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_F_4):** Applied to GPP_F4. Same description as bit 0.
3	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_F_3):** Applied to GPP_F3. Same description as bit 0.
2	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_F_2):** Applied to GPP_F2. Same description as bit 0.
1	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_F_1):** Applied to GPP_F1. Same description as bit 0.
0	0h RW1C	**GPI Interrupt Status (GPI_INT_STS_GPP_F_0):** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: - The corresponding pad is used in GPIO input mode - HOSTSW_OWN = 1 (i.e. Host GPIO Driver Mode). Writing a value of 1 will clear the bit while writing a value of 0 has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN does not prevent the setting of GPI_INT_STS.

29.4.15 GPI Interrupt Status (GPI_IS_GPP_G)—Offset 104h

Same definition as GPI_IS_GPP_F register, except this register applies to GPP_G group (GPP_G[7:0]). Bits corresponding to unimplemented GPP_G are reserved.

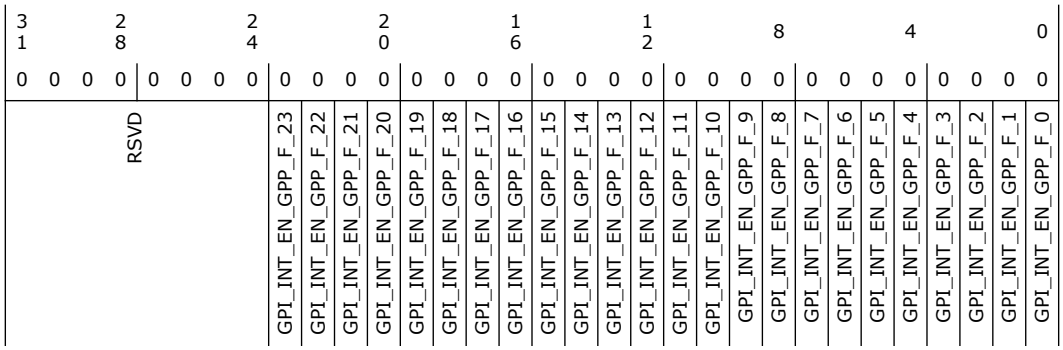
29.4.16 GPI Interrupt Enable (GPI_IE_GPP_F)—Offset 120h

Access Method

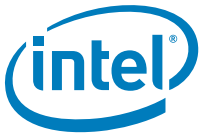
Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_F_23):** Applied to GPP_F23. Same description as bit 0.
22	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_F_22):** Applied to GPP_F22. Same description as bit 0.
21	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_F_21):** Applied to GPP_F21. Same description as bit 0.
20	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_F_20):** Applied to GPP_F20. Same description as bit 0.
19	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_F_19):** Applied to GPP_F19. Same description as bit 0.
18	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_F_18):** Applied to GPP_F18. Same description as bit 0.
17	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_F_17):** Applied to GPP_F17. Same description as bit 0.
16	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_F_16):** Applied to GPP_F16. Same description as bit 0.
15	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_F_15):** Applied to GPP_F15. Same description as bit 0.
14	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_F_14):** Applied to GPP_F14. Same description as bit 0.



Bit Range	Default & Access	Field Name (ID): Description
13	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_F_13):** Applied to GPP_F13. Same description as bit 0.
12	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_F_12):** Applied to GPP_F12. Same description as bit 0.
11	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_F_11):** Applied to GPP_F11. Same description as bit 0.
10	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_F_10):** Applied to GPP_F10. Same description as bit 0.
9	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_F_9):** Applied to GPP_F9. Same description as bit 0.
8	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_F_8):** Applied to GPP_F8. Same description as bit 0.
7	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_F_7):** Applied to GPP_F7. Same description as bit 0.
6	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_F_6):** Applied to GPP_F6. Same description as bit 0.
5	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_F_5):** Applied to GPP_F5. Same description as bit 0.
4	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_F_4):** Applied to GPP_F4. Same description as bit 0.
3	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_F_3):** Applied to GPP_F3. Same description as bit 0.
2	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_F_2):** Applied to GPP_F2. Same description as bit 0.
1	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_F_1):** Applied to GPP_F1. Same description as bit 0.
0	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_F_0):** This bit is used to enable/ disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing.

29.4.17 GPI Interrupt Enable (GPI_IE_GPP_G)—Offset 124h

Same definition as GPI_IE_GPP_F register, except this register applies to GPP_G group (GPP_G[7:0]). Bits corresponding to unimplemented GPP_G are reserved.

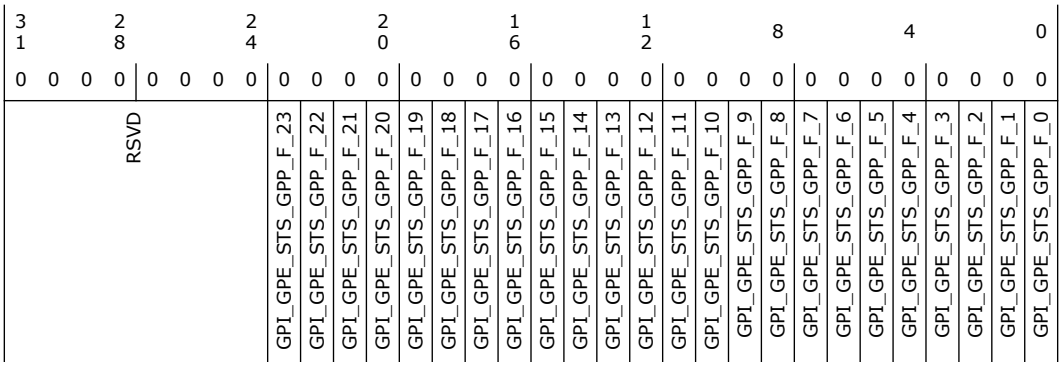
29.4.18 GPI General Purpose Events Status (GPI_GPE_STS_GPP_F)—Offset 140h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_F_23):** Applied to GPP_F23. Same description as bit 0.
22	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_F_22):** Applied to GPP_F22. Same description as bit 0.
21	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_F_21):** Applied to GPP_F21. Same description as bit 0.
20	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_F_20):** Applied to GPP_F20. Same description as bit 0.
19	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_F_19):** Applied to GPP_F19. Same description as bit 0.
18	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_F_18):** Applied to GPP_F18. Same description as bit 0.
17	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_F_17):** Applied to GPP_F17. Same description as bit 0.
16	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_F_16):** Applied to GPP_F16. Same description as bit 0.
15	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_F_15):** Applied to GPP_F15. Same description as bit 0.
14	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_F_14):** Applied to GPP_F14. Same description as bit 0.
13	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_F_13):** Applied to GPP_F13. Same description as bit 0.
12	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_F_12):** Applied to GPP_F12. Same description as bit 0.
11	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_F_11):** Applied to GPP_F11. Same description as bit 0.
10	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_F_10):** Applied to GPP_F10. Same description as bit 0.
9	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_F_9):** Applied to GPP_F9. Same description as bit 0.
8	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_F_8):** Applied to GPP_F8. Same description as bit 0.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_F_7):** Applied to GPP_F7. Same description as bit 0.
6	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_F_6):** Applied to GPP_F6. Same description as bit 0.
5	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_F_5):** Applied to GPP_F5. Same description as bit 0.
4	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_F_4):** Applied to GPP_F4. Same description as bit 0.
3	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_F_3):** Applied to GPP_F3. Same description as bit 0.
2	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_F_2):** Applied to GPP_F2. Same description as bit 0.
1	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_F_1):** Applied to GPP_F1. Same description as bit 0.
0	0h RW1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_F_0):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high(or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS bit is set: - If the system is in an S3-S5 state, the event will also wake the system. - If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN does not prevent the setting of GPI_GPE_STS.

29.4.19 GPI General Purpose Events Status (GPI_GPE_STS_GPP_G)—Offset 144h

Same definition as GPI_GPE_STS_GPP_F register, except this register applies to GPP_G group (GPP_G[7:0]). Bits corresponding to unimplemented GPP_G are reserved.

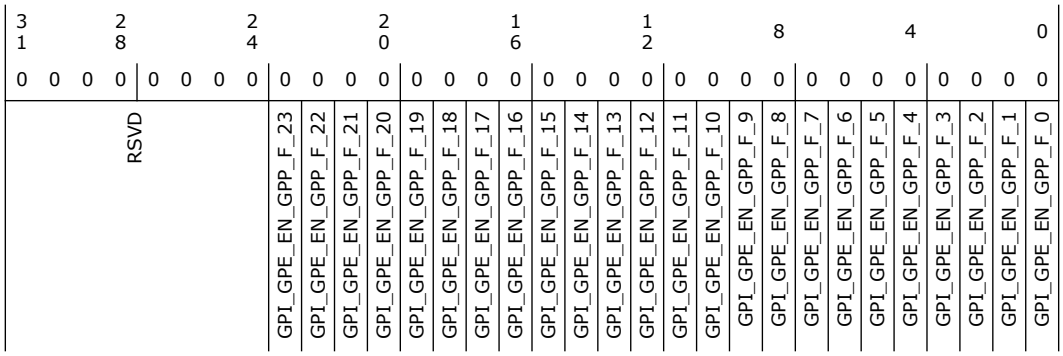
29.4.20 GPI General Purpose Events Enable (GPI_GPE_EN_GPP_F)—Offset 160h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_F_23):** Applied to GPP_F23. Same description as bit 0.
22	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_F_22):** Applied to GPP_F22. Same description as bit 0.
21	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_F_21):** Applied to GPP_F21. Same description as bit 0.
20	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_F_20):** Applied to GPP_F20. Same description as bit 0.
19	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_F_19):** Applied to GPP_F19. Same description as bit 0.
18	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_F_18):** Applied to GPP_F18. Same description as bit 0.
17	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_F_17):** Applied to GPP_F17. Same description as bit 0.
16	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_F_16):** Applied to GPP_F16. Same description as bit 0.
15	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_F_15):** Applied to GPP_F15. Same description as bit 0.
14	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_F_14):** Applied to GPP_F14. Same description as bit 0.
13	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_F_13):** Applied to GPP_F13. Same description as bit 0.
12	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_F_12):** Applied to GPP_F12. Same description as bit 0.
11	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_F_11):** Applied to GPP_F11. Same description as bit 0.
10	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_F_10):** Applied to GPP_F10. Same description as bit 0.
9	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_F_9):** Applied to GPP_F9. Same description as bit 0.
8	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_F_8):** Applied to GPP_F8. Same description as bit 0.
7	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_F_7):** Applied to GPP_F7. Same description as bit 0.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_F_6):** Applied to GPP_F6. Same description as bit 0.
5	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_F_5):** Applied to GPP_F5. Same description as bit 0.
4	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_F_4):** Applied to GPP_F4. Same description as bit 0.
3	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_F_3):** Applied to GPP_F3. Same description as bit 0.
2	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_F_2):** Applied to GPP_F2. Same description as bit 0.
1	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_F_1):** Applied to GPP_F1. Same description as bit 0.
0	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_F_0):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'.

29.4.21 GPI General Purpose Events Enable (GPI_GPE_EN_GPP_G)—Offset 164h

Same definition as GPI_GPE_EN_GPP_F register, except this register applies to GPP_G group (GPP_G[7:0]). Bits corresponding to unimplemented GPP_G are reserved.

29.4.22 Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_0)—Offset 400h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 44000X00h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0
PADRSTCFG	RXPADSTSEL	RXRAW1	RSVD	RXEVCFG		PREGFRXSEL	RXINV	RXTXENCFG		GPIROUTIOXAPIC	GPIROUTSCI	GPIROUTSMI	GPIROUTNMI	RSVD						PMODE1	PMODE0	GPIORXDIS	GPIOTXDIS	RSVD						GPIORXSTATE	GPIOTXSTATE

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset GPIO pad register fields in PAD_CFG_DW0 and PAD_CFG_DW1 registers. This register can be used for Sx isolation of the associated signal if needed. 00 = RSMRST# 01 = Host deep reset. This reset occurs when a host reset (with or without power cycle) is initiated or a global reset is initiated, except that the reset does not assert when in S3/S4/S5. 10 = PLTRST# 11 = Reserved
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determines from which node the RX pad state for native function should be taken from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from RX buffer 1 = Internal RX pad state (subject to RXINV and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field is only applicable when the RX buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	Reserved.
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determines if the internal RX pad state (synchronized, filtered vs non-filtered version as determined by PreGfRXSel, and is further subject to RXInv) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller . 0h = Level 1h = Edge 2h = Drive '0' 3h = Reserved (implement as setting 0h)
24	0h RO	Reserved.
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field is only applicable when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RO	Reserved.
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determines if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determines if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI. 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s).
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determines if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determines if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:12	0h RO	Reserved.
11	-- RW	**Pad Mode bit 1 (PMODE1):** See Pad Mode bit 0 description.
10	-- RW	**Pad Mode bit 0 (PMODE0):** This bit is used in conjunction with Pad Mode bit 1. This two-bit field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad. 1h = native function 1, if applicable, controls the Pad 2h = native function 2, if applicable, controls the Pad. Also used to enable the GPIO blink (PWM) capability if applicable (note that not all GPIOs have the blink capability) 3h = native function 3, if applicable, controls the Pad Dedicated (unmuxed) GPIO shall report RO of all 0's in this register field If GPIO vs. native mode is configured via soft strap, this bit has no effect. Default value is determined by the default functionality of the pad.
9	1h RW	**GPIO RX Disable (GPIORXDIS):** 0 = Enable the input buffer (active low enable) of the pad. 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0'.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** 0 = Enable the output buffer (active low enable) of the pad. 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	Reserved.
1	0h RO	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV settings.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** 0 = Drive a level '0' to the TX output pad. 1 = Drive a level '1' to the TX output pad.

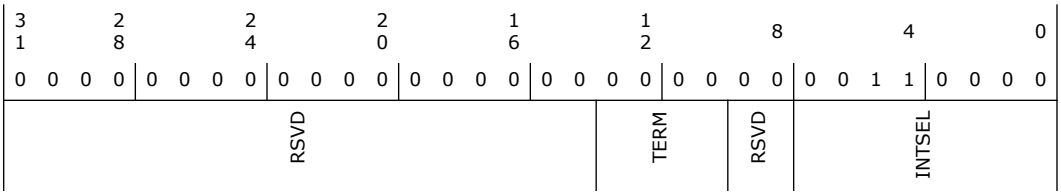
29.4.23 Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_0)—Offset 404h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 30h



Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings for [13:10] correspond to: 0000: none 0010: 5k pd 0100: 20k pd 1010: 5k pu 1100: 20k pu 1111: Native controller selected by Pad Mode controls the Termination. This setting needs to be set only for GPP_A1 / LAD0, GPP_A2 / LAD1, GPP_A3 / LAD2, GPP_A4 / LAD3, GPD1 / ACPRESENT, and GPD2 / LAN_WAKE#, when the signals are used as native function. Otherwise, the setting is reserved. All other settings not mentioned above are reserved. If a reserved value is programmed, pad may malfunction. The setting of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in sw/fw in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, pu/pd settings should be programmed first to ensure the input does not float momentarily.
9:8	0h RO	Reserved.
7:0	30h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 .... Up to the max IOxAPIC IRQ supported

29.4.24 Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_1)—Offset 408h

Same description as PAD_CFG_DW0_GPP_F_0.

29.4.25 Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_1)—Offset 40Ch

Same description as PAD_CFG_DW1_GPP_F_0. Exception: The default value of the INTSEL bit field in this register is : 31h

29.4.26 Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_2)—Offset 410h

Same description as PAD_CFG_DW0_GPP_F_0.

29.4.27 Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_2)—Offset 414h

Same description as PAD_CFG_DW1_GPP_F_0. Exception: The default value of the INTSEL bit field in this register is : 32h

29.4.28 Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_3)—Offset 418h

Same description as PAD_CFG_DW0_GPP_F_0.

29.4.29 Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_3)—Offset 41Ch

Same description as PAD_CFG_DW1_GPP_F_0. Exception: The default value of the INTSEL bit field in this register is : 33h

29.4.30 Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_4)—Offset 420h

Same description as PAD_CFG_DW0_GPP_F_0.

29.4.31 Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_4)—Offset 424h

Same description as PAD_CFG_DW1_GPP_F_0. Exception: The default value of the INTSEL bit field in this register is : 34h

29.4.32 Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_5)—Offset 428h

Same description as PAD_CFG_DW0_GPP_F_0.

29.4.33 Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_5)—Offset 42Ch

Same description as PAD_CFG_DW1_GPP_F_0.
Exception: The default value of the INTSEL bit field in this register is : 35h

29.4.34 Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_6)—Offset 430h

Same description as PAD_CFG_DW0_GPP_F_0.

29.4.35 Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_6)—Offset 434h

Same description as PAD_CFG_DW1_GPP_F_0.
Exception: The default value of the INTSEL bit field in this register is : 36h

29.4.36 Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_7)—Offset 438h

Same description as PAD_CFG_DW0_GPP_F_0.

29.4.37 Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_7)—Offset 43Ch

Same description as PAD_CFG_DW1_GPP_F_0.
Exception: The default value of the INTSEL bit field in this register is : 37h

29.4.38 Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_8)—Offset 440h

Same description as PAD_CFG_DW0_GPP_F_0.

29.4.39 Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_8)—Offset 444h

Same description as PAD_CFG_DW1_GPP_F_0.
Exception: The default value of the INTSEL bit field in this register is : 38h

29.4.40 Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_9)—Offset 448h

Same description as PAD_CFG_DW0_GPP_F_0.

29.4.41 Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_9)—Offset 44Ch

Same description as PAD_CFG_DW1_GPP_F_0.
Exception: The default value of the INTSEL bit field in this register is : 39h

29.4.42 Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_10)—Offset 450h

Same description as PAD_CFG_DW0_GPP_F_0.

29.4.43 Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_10)—Offset 454h

Same description as PAD_CFG_DW1_GPP_F_0.
Exception: The default value of the INTSEL bit field in this register is : 3Ah

29.4.44 Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_11)—Offset 458h

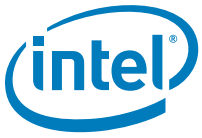
Same description as PAD_CFG_DW0_GPP_F_0.

29.4.45 Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_11)—Offset 45Ch

Same description as PAD_CFG_DW1_GPP_F_0.
Exception: The default value of the INTSEL bit field in this register is : 3Bh

29.4.46 Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_12)—Offset 460h

Same description as PAD_CFG_DW0_GPP_F_0.



29.4.47 Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_12)—Offset 464h

Same description as PAD_CFG_DW1_GPP_F_0. Exception: The default value of the INTSEL bit field in this register is : 3Ch

29.4.48 Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_13)—Offset 468h

Same description as PAD_CFG_DW0_GPP_F_0.

29.4.49 Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_13)—Offset 46Ch

Same description as PAD_CFG_DW1_GPP_F_0. Exception: The default value of the INTSEL bit field in this register is : 3Dh

29.4.50 Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_14)—Offset 470h

Same description as PAD_CFG_DW0_GPP_F_0.

29.4.51 Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_14)—Offset 474h

Same description as PAD_CFG_DW1_GPP_F_0. Exception: The default value of the INTSEL bit field in this register is : 3Eh

29.4.52 Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_15)—Offset 478h

Same description as PAD_CFG_DW0_GPP_F_0.

29.4.53 Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_15)—Offset 47Ch

Same description as PAD_CFG_DW1_GPP_F_0. Exception: The default value of the INTSEL bit field in this register is : 3Fh

29.4.54 Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_16)—Offset 480h

Same description as PAD_CFG_DW0_GPP_F_0.

29.4.55 Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_16)—Offset 484h

Same description as PAD_CFG_DW1_GPP_F_0. Exception: The default value of the INTSEL bit field in this register is : 40h

29.4.56 Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_17)—Offset 488h

Same description as PAD_CFG_DW0_GPP_F_0.

29.4.57 Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_17)—Offset 48Ch

Same description as PAD_CFG_DW1_GPP_F_0. Exception: The default value of the INTSEL bit field in this register is : 41h

29.4.58 Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_18)—Offset 490h

Same description as PAD_CFG_DW0_GPP_F_0.

29.4.59 Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_18)—Offset 494h

Same description as PAD_CFG_DW1_GPP_F_0. Exception: The default value of the INTSEL bit field in this register is : 42h

29.4.60 Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_19)—Offset 498h

Same description as PAD_CFG_DW0_GPP_F_0.

29.4.61 Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_19)—Offset 49Ch

Same description as PAD_CFG_DW1_GPP_F_0. Exception: The default value of the INTSEL bit field in this register is : 43h

29.4.62 Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_20)—Offset 4A0h

Same description as PAD_CFG_DW0_GPP_F_0.

29.4.63 Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_20)—Offset 4A4h

Same description as PAD_CFG_DW1_GPP_F_0. Exception: The default value of the INTSEL bit field in this register is : 44h

29.4.64 Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_21)—Offset 4A8h

Same description as PAD_CFG_DW0_GPP_F_0.

29.4.65 Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_21)—Offset 4ACh

Same description as PAD_CFG_DW1_GPP_F_0. Exception: The default value of the INTSEL bit field in this register is : 45h

29.4.66 Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_22)—Offset 4B0h

Same description as PAD_CFG_DW0_GPP_F_0.

29.4.67 Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_22)—Offset 4B4h

Same description as PAD_CFG_DW0_GPP_F_0. Exception: The default value of the INTSEL bit field in this register is : 46h

29.4.68 Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_23)—Offset 4B8h

Same description as PAD_CFG_DW0_GPP_F_0.

29.4.69 Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_23)—Offset 4BCh

Same description as PAD_CFG_DW1_GPP_F_0. Exception: The default value of the INTSEL bit field in this register is : 47h

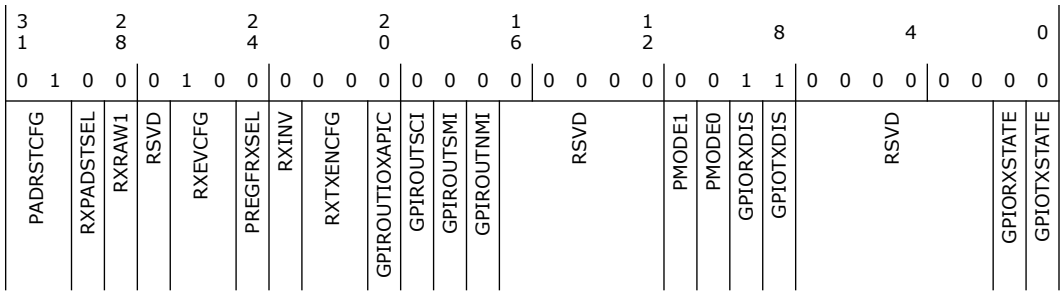
29.4.70 Pad Configuration DW0 (PAD_CFG_DW0_GPP_G_0)—Offset 4C0h

Same description as PAD_CFG_DW0_GPP_F_0.

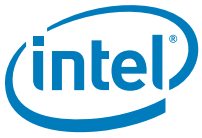
Access Method

Type: MSG Register (Size: 32 bits)	**Device:** **Function:**

Default: 44000300h



Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** Pad Reset Config (PadRstCfg) This register controls which reset is used to reset the specified Pad Register fields. It is the SoC responsibilities to decide the number of configurable reset required with an example below: 00 = Powergood (i.e. sticky reset) 01 = Deep GPIO Reset (i.e. host deep reset: host_deep_rst_b) 10 = GPIO Reset (i.e. host reset: host_rst_b) 11 = Reserved; tied to inactive (i.e. '1' for active low reset) For DSW well pads, this register default to 00b. For Primary well GPIO pads, this register default to 01b Note: The hardware must ensure that when this field is programmed, the muxed reset signal does not glitch to cause momentarily reset assertion.
29	0h RW	**RX Pad State Select (RXPADSTSEL):** RX Pad State Select (RXPadStSel) Determine from which node the RX pad state for native function should be taken from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Internal RX pad state (subject to RXINV and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** RX Raw Override to '1' (RXRAW1) This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	Reserved.
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** RX Level/Edge Configuration (RxEvCfg) Determine if the internal RX pad state (synchronized, filtered vs non-filtered version as determined by PreGfRXSel, and is further subject to RXInv) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller . 0h = Level 1h = Edge 2h = Drive '0' 3h = Reserved (implement as setting 0h)
24	0h RO	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Pre Glitch Filter Stage RX Pad State Select (PreGfRXSel) Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** RX Invert (RXINV) This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RO	**RX/TX Enable Config (RXTXENCFG):** RX/TX Enable Config (RXTXEnCfg) This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** GPIO Input Route IOxAPIC (GPIOIRoutIOxAPIC) Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** GPIO Input Route SCI (GPIOIRoutSCI) Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.



Bit Range	Default & Access	Field Name (ID): Description
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** GPIO Input Route SMI (GPIOIRoutSMI) Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** GPIO Input Route NMI (GPIOIRoutNMI) Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:12	0h RO	Reserved.
11	0h RW	**Pad Mode bit 1 (PMODE1):** Pad Mode (PMode) This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ..... 15 = Function 15 control the Pad
10	0h RW	**Pad Mode bit 0 (PMODE0):** Pad Mode (PMode) This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad ..... 15 = Function 15 control the Pad
9	1h RW	**GPIO RX Disable (GPIORXDIS):** GPIO RX Disable (GPIORxDis) 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0' by CFIO HIP.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** GPIO TX Disable (GPIOTxDis) 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	Reserved.
1	0h RO	**GPIO RX State (GPIORXSTATE):** GPIO RX State (GPIORxState) This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV settings.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** GPIO TX State (GPIOTxState) 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

29.4.71 Pad Configuration DW1 (PAD_CFG_DW1_GPP_G_0)—Offset 4C4h

Same description as PAD_CFG_DW1_GPP_F_0.

29.4.72 Pad Configuration DW0 (PAD_CFG_DW0_GPP_G_1)—Offset 4C8h

Same description as PAD_CFG_DW0_GPP_F_0.

29.4.73 Pad Configuration DW1 (PAD_CFG_DW1_GPP_G_1)—Offset 4CCh

Same description as PAD_CFG_DW1_GPP_F_0. Exception: The default value of the INTSEL bit field in this register is : 49h

29.4.74 Pad Configuration DW0 (PAD_CFG_DW0_GPP_G_2)—Offset 4D0h

Same description as PAD_CFG_DW0_GPP_F_0.

29.4.75 Pad Configuration DW1 (PAD_CFG_DW1_GPP_G_2)—Offset 4D4h

Same description as PAD_CFG_DW1_GPP_F_0. Exception: The default value of the INTSEL bit field in this register is : 4Ah

29.4.76 Pad Configuration DW0 (PAD_CFG_DW0_GPP_G_3)—Offset 4D8h

Same description as PAD_CFG_DW0_GPP_F_0.

29.4.77 Pad Configuration DW1 (PAD_CFG_DW1_GPP_G_3)—Offset 4DCh

Same description as PAD_CFG_DW1_GPP_F_0. Exception: The default value of the INTSEL bit field in this register is : 4Bh

29.4.78 Pad Configuration DW0 (PAD_CFG_DW0_GPP_G_4)—Offset 4E0h

Same description as PAD_CFG_DW0_GPP_F_0.

29.4.79 Pad Configuration DW1 (PAD_CFG_DW1_GPP_G_4)—Offset 4E4h

Same description as PAD_CFG_DW1_GPP_F_0. Exception: The default value of the INTSEL bit field in this register is : 4Ch

29.4.80 Pad Configuration DW0 (PAD_CFG_DW0_GPP_G_5)—Offset 4E8h

Same description as PAD_CFG_DW0_GPP_F_0.

29.4.81 Pad Configuration DW1 (PAD_CFG_DW1_GPP_G_5)—Offset 4ECh

Same description as PAD_CFG_DW1_GPP_F_0. Exception: The default value of the INTSEL bit field in this register is : 4Dh

29.4.82 Pad Configuration DW0 (PAD_CFG_DW0_GPP_G_6)—Offset 4F0h

Same description as PAD_CFG_DW0_GPP_F_0.

29.4.83 Pad Configuration DW1 (PAD_CFG_DW1_GPP_G_6)—Offset 4F4h

Same description as PAD_CFG_DW1_GPP_F_0. Exception: The default value of the INTSEL bit field in this register is : 4Eh

29.4.84 Pad Configuration DW0 (PAD_CFG_DW0_GPP_G_7)—Offset 4F8h

Same description as PAD_CFG_DW0_GPP_F_0.

29.4.85 Pad Configuration DW1 (PAD_CFG_DW1_GPP_G_7)—Offset 4FCh

Same description as PAD_CFG_DW1_GPP_F_0. Exception: The default value of the INTSEL bit field in this register is : 4Fh

§ §

30 High Precision Event Timer (HPET)

30.1 HPET Memory Mapped Registers Summary

The timer registers are memory mapped directly (rather than indexed) to allow the CPU to access each register without having to use an index register. This ensures accesses are safe for multi-threaded environments. The timer register space is 1024 bytes. The registers are generally aligned on 64-bit boundaries to simplify implementation with IA64 processors. In the PCH, there are 4 possible memory address ranges beginning at 1) FED0_0000h, 2) FED0_1000h, 3) FED0_2000h, 4) FED0_3000h. The choice of address range should be selected by assigning the High Performance Event Timer Configuration (HPTC) register fields in the configuration space of the Primary to Sideband Bridge. All registers are implemented in the Primary power well, and all bits are reset by PLTRST#. Reads to reserved registers or bits will return a value of 0.
Behavorial Rules:
1. Software can read or write the various bytes in these registers using 32-bit or 64-bit accesses. Software must not attempt to read or write across register boundaries. For example, a 32-bit access should be to offset x0h, x4h, x8h, or xCh. 32-bit accesses should not be to 01h, 02h, 03h, 05h, 06h, 07h, 09h, 0Ah, 0Bh, 0Dh, 0Eh, or 0Fh. Any accesses to these offsets will result in an unexpected behavior, and may result in a master abort. However, these accesses should not result in system hangs. 64-bit accesses can only be to x0h and must not cross 64-bit boundaries.
2. Software should not write to read-only registers.
3. Software should not expect any particular or consistent value when reading reserved registers or bits.

Table 30-1. Summary of HPET Memory Mapped Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	7h	General Capabilities and ID Register (GEN_CAP_ID)—Offset 0h	27BC86B8086A701h
10h	17h	General Config Register (GEN_CFG)—Offset 10h	0h
20h	27h	General Interrupt Status Register (GEN_INT_STS)—Offset 20h	0h
F0h	F7h	Main Counter Value (MAIN_CNTR)—Offset F0h	0h
100h	107h	Timer n Config and Capabilities (TMRn_CNF_CAP)—Offset 100h	F0000000008030h
108h	10Fh	Timer n Comparator Value (TMRn_CMP_VAL)—Offset 108h	FFFFFFFFFFFFFFFFh

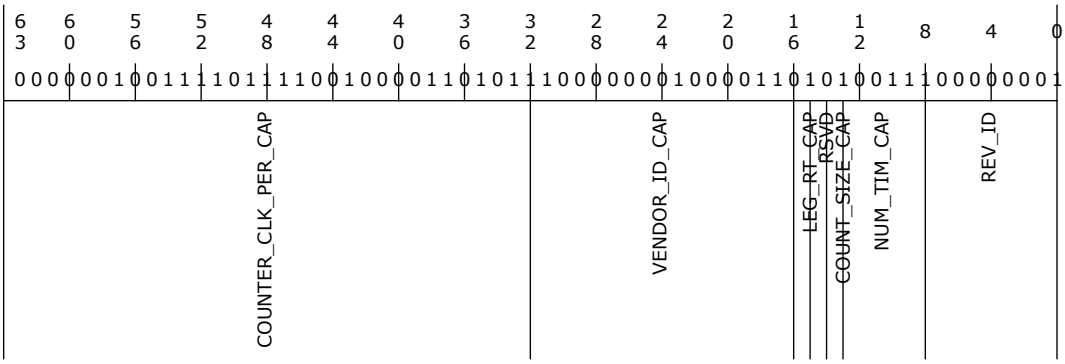
30.1.1 General Capabilities and ID Register (GEN_CAP_ID)—Offset 0h

Access Method

Type: MEM Register (Size: 64 bits)

Device:
Function:

Default: 27BC86B8086A701h



Bit Range	Default & Access	Field Name (ID): Description
63:32	27BC86Bh RO	**Main Counter Tick Period (COUNTER_CLK_PER_CAP):** This read-only field indicates the period at which the counter increments in femtoseconds (10^-15 seconds). The PCH HPET timers use a 24 MHz clock, which has a period of 41,666,667 femtoseconds. Therefore this register will always return 027BC86Bh when read.
31:16	8086h RO	**Vendor ID (VENDOR_ID_CAP):** These bits will return 8086h when read to reflect Intel as the vendor.
15	1h RO	**Legacy Rout Capable (LEG_RT_CAP):** This bit will always be 1 when read, indicating support for the Legacy Interrupt Rout.
14	0h RO	Reserved.
13	1h RO	**Counter Size (COUNT_SIZE_CAP):** This bit will return 1 when read to indicate support for 64-bit counters allowing 64 or 32-bit mode operation.
12:8	7h RO	**Number of Timers (NUM_TIM_CAP):** This value in this field will be 07h to indicate support for 8 timers in the timer block.
7:0	1h RO	**Revision ID (REV_ID):** This field indicates which revision of the function is implemented. Default value will be 01h.

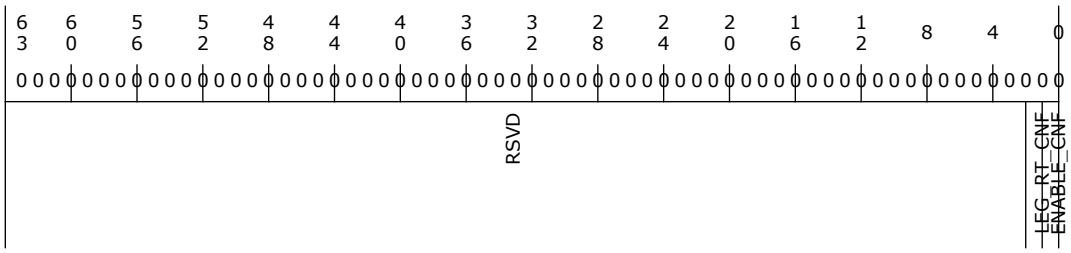
30.1.2 General Config Register (GEN_CFG)—Offset 10h

Access Method

Type: MEM Register
(Size: 64 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
63:2	0h RO	Reserved.
1	0h RW	**Legacy Rout (LEG_RT_CNF):** If the ENABLE_CNF bit and the LEG_RT_CNF bit are both set, the interrupts will be routed as follows: • Timer 0 is routed to IRQ0 in 8259 or IRQ2 in the I/O APIC • Timer 1 is routed to IRQ8 in 8259 or IRQ8 in the I/O APIC • Timer 2-n is routed as per the routing in the timer n Configuration registers. • If the Legacy Replacement Rout bit is set, the individual routing bits for Timers 0 and 1 (APIC) will have no impact. • If the Legacy Replacement Rout bit is not set, the individual routing bits for each of the timers are used. • This bit will default to 0. BIOS can set it to 1 to enable the legacy replacement routing, or 0 to disable the legacy replacement routing.
0	0h RW	**Overall Enable (ENABLE_CNF):** This bit must be set to enable any of the timers to generate interrupts. If this bit is 0, then the main counter will halt (will not increment) and no interrupts will be caused by any of these timers. For level-triggered interrupts, if an interrupt is pending when the ENABLE_CNF bit is changed from 1 to 0, the interrupt status indications (in the various Txx_INT_STS bits) will not be cleared. Software must write to the Txx_INT_STS bits to clear the interrupts. NOTE: This bit will default to 0. BIOS can set it to 1 or 0.

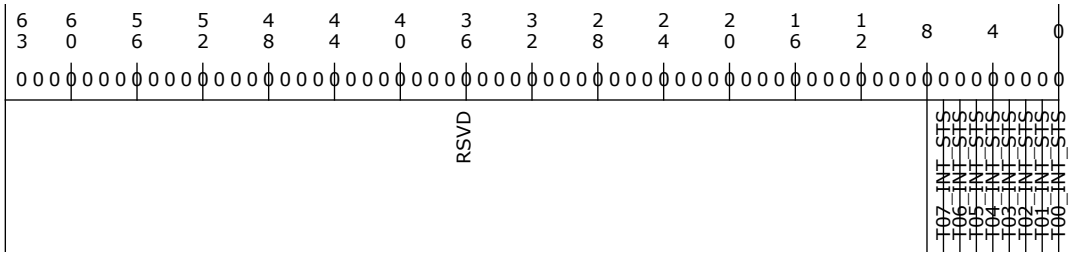
30.1.3 General Interrupt Status Register (GEN_INT_STS)—Offset 20h

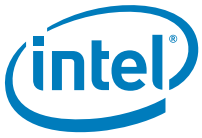
Access Method

Type: MEM Register
(Size: 64 bits)

Device:
Function:

Default: 0h





Bit Range	Default & Access	Field Name (ID): Description
63:8	0h RO	Reserved.
7	0h RW/C	**Timer 7 Interrupt Active (T07_INT_STS):** Same functionality as Timer 0.
6	0h RW/C	**Timer 6 Interrupt Active (T06_INT_STS):** Same functionality as Timer 0.
5	0h RW/C	**Timer 5 Interrupt Active (T05_INT_STS):** Same functionality as Timer 0.
4	0h RW/C	**Timer 4 Interrupt Active (T04_INT_STS):** Same functionality as Timer 0.
3	0h RW/C	**Timer 3 Interrupt Active (T03_INT_STS):** Same functionality as Timer 0.
2	0h RW/C	**Timer 2 Interrupt Active (T02_INT_STS):** Same functionality as Timer 0.
1	0h RW/C	**Timer 1 Interrupt Active (T01_INT_STS):** Same functionality as Timer 0.
0	0h RW/C	**Timer 0 Interrupt Active (T00_INT_STS):** The functionality of this bit depends on whether the edge or level-triggered mode is used for this timer. (default = 0) If set to level-triggered mode: This bit will be set by hardware if the corresponding timer interrupt is active. Once the bit is set, it can be cleared by software writing a 1 to the same bit position. Writes of 0 to this bit will have no effect. If set to edge-triggered mode: This bit should be ignored by software. Software should always write 0 to this bit. NOTE: Defaults to 0. In edge triggered mode, this bit will always read as 0 and writes will have no effect.

30.1.4 Main Counter Value (MAIN_CNTR)—Offset F0h

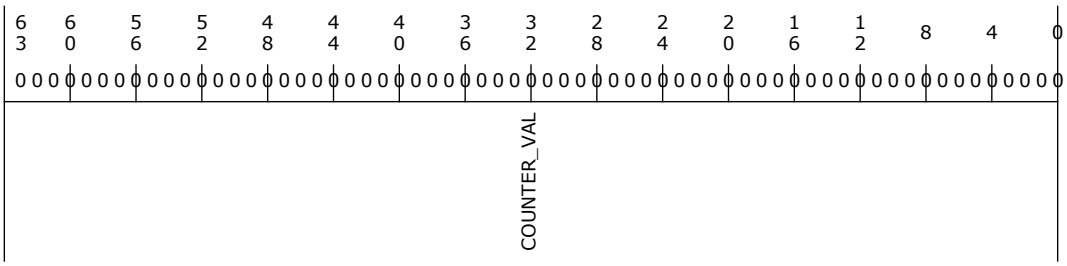
Software can read the various bytes in this register using 32-bit or 64-bit accesses. 32-bit accesses may only be done to offset 0F0h or 0F4h. 64-bit accesses may only be done to 0F0h. Writes to this register should only be done while the counter is halted. Reads to this register return the current value of the main counter. If 32-bit software attempts to read a 64-bit counter, it should first halt the counter. Since this will delay the interrupts for all of the timers, this should be done only if the consequences are understood. It is strongly recommended that 32-bit software only operate the timer in 32-bit mode. Reads to this register are monotonic. No two consecutive reads will return the same value. The second of two reads will always return a larger value (unless the timer has rolled over to 0)

Access Method

Type: MEM Register (Size: 64 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
63:0	0h RW/V	**Counter Value (COUNTER_VAL):** Reads return the current value of the counter. Writes load the new value to the counter. NOTES: 1. Writes to this register should only be done while the counter is halted. 2. Reads to this register return the current value of the main counter. 3. 32-bit counters will always return 0 for the upper 32-bits of this register. 4. If 32-bit software attempts to read a 64-bit counter, it should first halt the counter. Since this will delay the interrupts for all of the timers, this should be done only if the consequences are understood. It is strongly recommended that 32-bit software only operate the timer in 32-bit mode. 5. Reads to this register are monotonic. No two consecutive reads will return the same value. The second of two reads will always return a larger value (unless the timer has rolled over to 0)

30.1.5 Timer n Config and Capabilities (TMRn_CNF_CAP)—Offset 100h

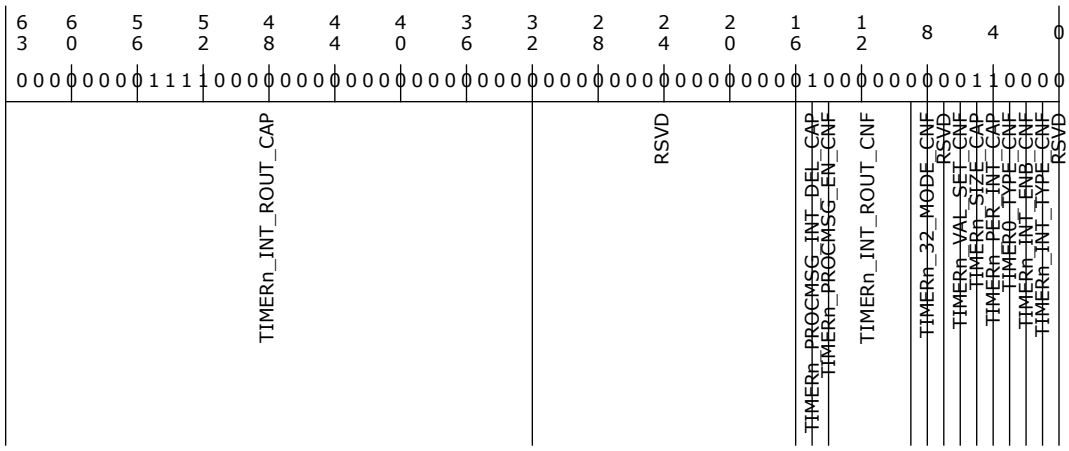
Timer 0: 100–107h,
Timer 1: 120–127h,
Timer 2: 140–147h,
Timer 3: 160–167h,
Timer 4: 180–187h,
Timer 5: 1A0–1A7h,
Timer 6: 1C0–1C7h,
Timer 7: 1E0–1E7h,
The letter n can be 0, 1, 2, 3, 4, 5, 6, or 7 referring to Timer 0, 1, 2, 3, 4, 5, 6, or 7.

Access Method

Type: MEM Register
(Size: 64 bits)

Device:
Function:

Default: F0000000008030h



Bit Range	Default & Access	Field Name (ID): Description
63:32	F00000h RO	**Timer n Interrupt Rout (TIMERn_INT_ROUT_CAP):** This 32-bit read-only field indicates to which interrupts in the 8259 or I/O (x) APIC this timers interrupt can be routed to. This is used in conjunction with the TIMERn_INT_ROUT_CNF field. Writes to this field will have no effect. Note: If interrupt is handled via 8259, only interrupts 0-15 are applicable and valid. Each bit in this field corresponds to a particular interrupt. For example, if this timers interrupt can be mapped to interrupts 16, 18, 20, 22, or 24, then bits 16, 18, 20, 22, and 24 in this field will be set to 1. All other bits will be 0. Timer 0,1 : Bits 20, 21, 22, and 23 in this field will have a value of 1. All other bits will be 0. Timer 2 : Bits 11, 20, 21, 22, and 23 in this field will have a value of 1. All other bits will be 0. If IRQ 11 is used, software should ensure IRQ 11 is not shared with any other devices to guarantee the proper operation of this timer. Timer 3 : Bits 12, 20, 21, 22, and 23 in this field will have a value of 1. All other bits will be 0. If IRQ 12 is used, software should ensure IRQ 12 is not shared with any other devices to guarantee the proper operation of this timer. Timer 4-7: This field is always 0 as interrupts from these timers can only be delivered via direct FSB interrupt messages.
31:16	0h RO	Reserved.
15	1h RO	**Timer n Processor Message Interrupt Delivery Capability (TIMERn_PROCMSG_INT_DEL_CAP):** This bit is always read as 1, since the Intel PCH HPET implementation supports the direct processor interrupt delivery.
14	0h RW	**Timer n Processor Message Interrupt Delivery Enable (TIMERn_PROCMSG_EN_CNF):** When set, this will force the interrupts for Timer n to be delivered directly as processor messages, rather than using the 8259 or I/O (x) APIC. In this case, the TIMERn_INT_ROUTE_CNF field in this register will be ignored and the TIMERn_PROCMSG_ROUT register will be used instead. Timer 0, 1, 2, 3: This bit is a read/write bit. Timer 4, 5, 6, 7: This bit is always Read-Only 1 as interrupt from these timers canonly be delivered via direct FSB interrupt messages.
13:9	0h RW	**Timer n Interrupt Route (TIMERn_INT_ROUT_CNF):** This 5-bit field indicates the routing for the interrupt to the 8259 or I/O APIC. A maximum of 32 interrupts are supported. Software writes to this field to select which interrupt in the 8259 or I/O (x)APIC will be used for this timers interrupt. The default value for this register is 00h. If the Legacy Rout bit is set, then Timers 0 and 1 will have a different routing, and this bit field has no effect for those two timers. If the TIMERn_FSB_EN_CNF bit is set, then the interrupt will be delivered directly to the FSB, and this bit field has no effect. If interrupt is handled via 8259, only interrupts 0-15 are applicable and valid. Software must not program any value other than 0-15 in this field. Software must ensure that the value is valid for a particular timer as indicated by the TIMERn_INT_ROUTE_CAP field for that timer. The PCH logic does not check the validity of the value written. For Timers 4-7, this field is always Read-Only 0 as interrupts from these timers can only be delivered via direct FSB interrupt messages.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**Timer n 32-bit Mode (TIMERn_32_MODE_CNF):** Software can set this bit to force a 64-bit timer to behave as a 32-bit timer. This is typically needed if the software is not willing to halt the main counter to read or write a particular timer, and the software not capable of do an atomic 64-bit read to the timer. When TIMER0_32MODE_CNF is set to '1', the hardware counter will essentially be doing 32-bit operation on comparator match and rollovers. I.e. the upper 32-bit of the Timer 0 Comparator Value register is ignored. The upper 32-bit of the main counter is not involved in any roll over from lower 32-bit of the main counter and becomes all zero's. For timer 0, this bit will be read/write and default to 0. For timers 1-7, this bit will always read as 0 and writes will have no effect (since these seven timers are 32-bits).
7	0h RO	Reserved.
6	0h RO	**Timer n Value Set (TIMERn_VAL_SET_CNF):** Software uses this bit only for timers that have been set to periodic mode. By writing this bit to a 1, the software is then allowed to directly set the timers accumulator. Software does not have to write this bit back to 0 (it automatically clears). This bit will return 0 when read.Software should not write a 1 to this bit position if the timer is set to non-periodic mode. Writes will only have an effect for Timer 0 if it is set to periodic mode. Writes will have no effect for Timers 1-7 as they do not support the periodic mode.
5	1h RO	**Timer n Size (TIMERn_SIZE_CAP):** Read-only Indicator of the timers size capability.1: 64-bits0: 32-bits.The value is 1 (64-bits) for timer 0, and 0 (32-bits) for timers 1-7.
4	1h RO	**Periodic Interrupt Capable (TIMERn_PER_INT_CAP):** If this read-only bit is 1, then the hardware supports a periodic mode for this timers interrupt. The value is 1 (periodic supported) for timer 0, and 0 (not supported) for timers 1-7.
3	0h RW	**Timer 0 Type (TIMER0_TYPE_CNF):** Setting this bit to 1 enables the timer to generate a periodic interrupt if it is capable of doing so. If the TIMERn_PER_INT_CAP bit is 0, then this bit will always return 0 when read and writes will have no impact. For timer 0, this bit will be read/write, with default of 0. For timers 1-7, this bit will be read-only, with a fixed value of 0.
2	0h RW	**Timer n Interrupt Enable (TIMERn_INT_ENB_CNF):** Setting this bit to 1 enables the timer to generate a periodic interrupt if it is capable of doing so. If the TIMERn_PER_INT_CAP bit is 0, then this bit will always return 0 when read and writes will have no impact. For timer 0, this bit will be read/write, with default of 0. For timers 1-7, this bit will be read-only, with a fixed value of 0.
1	0h RW	**Timer Interrupt Type (TIMERn_INT_TYPE_CNF):** Determines whether an edge or level interrupt will be used for this timer (when enabled). 0: Edge-triggered. If another interrupt occurs, another edge will be generated. 1: Level-triggered. The interrupt will be held active until it is cleared by writing to the bit in the General Interrupt Status Register. If another interrupt occurs before the interrupt is cleared, the interrupt will remain active. The default value is 0, edge-triggered. The interrupt type for any timer should be set before that timer generates any interrupts. If the interrupt type is changed dynamically, there will be some delay before the new type takes effect. That delay is not specified. Timer 0-3: This bit is a read/write bit as both edge and level triggered modes are supported. Timer 4-7: This bit is always Read-Only 0 as only edge-triggered mode is supported.
0	0h RO	Reserved.

30.1.6 Timer n Comparator Value (TMRn_CMP_VAL)—Offset 108h

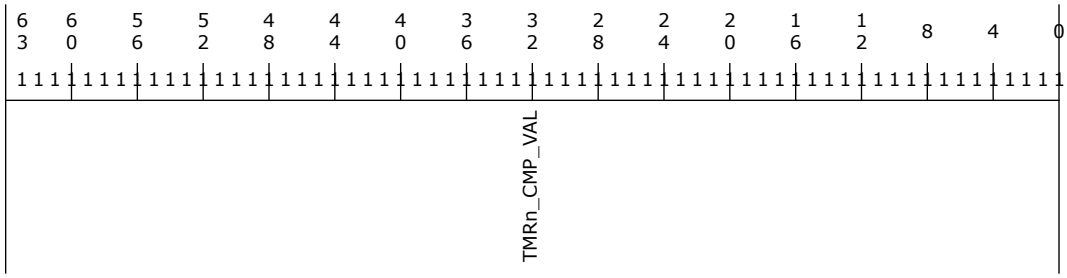
Timer 0: 108h – 10Fh
Timer 1: 128h – 12Fh
Timer 2: 148h – 14Fh
Timer 3: 168h – 16Fh
Timer 4: 188h – 18Fh
Timer 5: 1A8h – 1AFh
Timer 6: 1C8h – 1CFh
Timer 7: 1E8h – 1EFh

Access Method

Type: MEM Register
(Size: 64 bits)

Device:
Function:

Default: FFFFFFFFFFFFFFFFh



Bit Range	Default & Access	Field Name (ID): Description
63:0	FFFFFFFFFFFFFFFFh RW/V	**Timer n Comparator Value (TMRn_CMP_VAL):** If the timer is configured to non-periodic mode, when the main counter equals the value last written to this register, the corresponding interrupt can be generated (if so enabled). The value in this register does not change based on the interrupt being generated. If the timer is configured to periodic mode (supported only for Timer 0), when the main counter equals the value last written to this register, the corresponding interrupt can be generated (if so enabled). When this time out occurs, the value in this register is increased by the value last written to the register. For example, in periodic mode if the value written to the register is 0000123h: 1. An interrupt will be generated when the main counter reaches 00000123h. 2. The value in this register will then be adjusted by the hardware to 00000246h. 3. Another interrupt will be generated when the main counter reaches 00000246h. 4. The value in this register will then be adjusted by the hardware to 00000369h As each periodic interrupt occurs, the value in this register will increment. When the incremented value is greater than the maximum value possible for this register (FFFFFFFFh for a 32-bit timer or FFFFFFFFFFFFFFFFh for a 64-bit timer), the value will wrap around through 0. For example, if the current value in a 32-bit timer is FFFF0000h and the last value written to this register is 20000, then after the next interrupt the value will change to 00010000h The default value for each timer is all 1s for the bits that are implemented. For example, a 32-bit timer will have a default value of 00000000FFFFFFFFh. A 64-bit timer will have a default value of FFFFFFFFFFFFFFFFh. Software can read or write the various bytes in this register using 32-bit or 64-bit accesses. 32-bit accesses may only be done to offset 1x8h or 1xCh. 64-bit accesses may only be done to 1x8h. Comparator value. Timer 0 is 64-bits wide. Timers 1-7 are 32-bits wide.

§ §

31 Integrated Clock (ICC)

31.1 Integrated Clock Controller FW Accessible Registers Summary

The Integrated Clock Controller FW Accessible Registers are distributed within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface using the following Target Port (Destination Port) Identification:

- Target Port (Destination Port) Identification = 0xDC

Table 31-1. Summary of Integrated Clock Controller FW Accessible Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
1000h	1003h	Timing Control SRC Clock (TMCSRCCLK)—Offset 1000h	0h
1004h	1007h	Timing Control SRC Clock Register 2 (TMCSRCCLK2)—Offset 1004h	0h
1008h	100Bh	Enable Control CLKREQ (ENCCKRQ)—Offset 1008h	0h
100Ch	100Fh	Mask Control CLKREQ (MSKCKRQ)—Offset 100Ch	0h
1020h	1023h	ICC Security (ICCSEC)—Offset 1020h	0h
1024h	1027h	CLKREQ Mapping to CLKOUT_SRC (CKRQMAPSRC)—Offset 1024h	76543210h
1028h	102Bh	CLKREQ Mapping to CLKOUT_SRC Register 2 (CKRQMAPSRC2)—Offset 1028h	76543210h
102Ch	102Fh	Power Management (PM)—Offset 102Ch	0h
1034h	1037h	ICC Debug (ICCDBG)—Offset 1034h	0h
2000h	2003h	USB3Gen2PCIe PLL Control (G2PLLCTRL)—Offset 2000h	0h

31.1.1 Timing Control SRC Clock (TMCSRCCLK)—Offset 1000h

Controls minimum enable timing of PCIe SRC Clocks for support of PCIe L1Off using CLKREQ#

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
TclkreqSRC7	TclkreqSRC6	TclkreqSRC5	TclkreqSRC4	TclkreqSRC3	TclkreqSRC2	TclkreqSRC1	TclkreqSRC0

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RW	**Minimum Time from Effective Mapped CLKREQ# assertion to CLKOUT_SRC7 ungated (TclkreqSRC7):** See description for TclkreqSRC0 field[3:0]
27:24	0h RW	**Minimum Time from Effective Mapped CLKREQ# assertion to CLKOUT_SRC6 ungated (TclkreqSRC6):** See description for TclkreqSRC0 field[3:0]
23:20	0h RW	**Minimum Time from Effective Mapped CLKREQ# assertion to CLKOUT_SRC5 ungated (TclkreqSRC5):** See description for TclkreqSRC0 field[3:0]
19:16	0h RW	**Minimum Time from Effective Mapped CLKREQ# assertion to CLKOUT_SRC4 ungated (TclkreqSRC4):** See description for TclkreqSRC0 field[3:0]
15:12	0h RW	**Minimum Time from Effective Mapped CLKREQ# assertion to CLKOUT_SRC3 ungated (TclkreqSRC3):** See description for TclkreqSRC0 field[3:0]

Bit Range	Default & Access	Field Name (ID): Description
11:8	0h RW	**Minimum Time from Effective Mapped CLKREQ# assertion to CLKOUT_SRC2 ungated (TclkreqSRC2):** See description for TclkreqSRC0 field[3:0]
7:4	0h RW	**Minimum Time from Effective Mapped CLKREQ# assertion to CLKOUT_SRC1 ungated (TclkreqSRC1):** See description for TclkreqSRC0 field[3:0]
3:0	0h RW	**Minimum Time from Effective Mapped CLKREQ# assertion to CLKOUT_SRC0 ungated (TclkreqSRC0):** Minimum elapsed time from the Effective Mapped CLKREQ# signal assertion to the corresponding PCIe SRC Clock being allowed to toggle. This minimum time of CLKOUT_SRCn[P/N] staying gated at low voltage allows for the PCIe devices voltage rail to ramp to safe level on the exit from L1Off state before being driven with clock from the PCH. 0000: 0us minimum elapsed time from Effective Mapped CLKREQ# assertion to corresponding CLKOUT_SRCn ungated - Default - This setting is for PCIe device that does not support L1Off. This setting must also be used when corresponding CLKOUT_SRCn is configured for non-PCIe clock use, i.e. as MEX reference clock, etc. 0001: 5us minimum elapsed time ... 0010: 10us minimum elapsed time ... 0011: 15us minimum elapsed time ... 0100: 20us minimum elapsed time ... 0101: 25us minimum elapsed time ... 0110: 30us minimum elapsed time ... 0111: 35us minimum elapsed time ... 1000: 40us minimum elapsed time ... 1001: 45us minimum elapsed time ... 1010: 50us minimum elapsed time ... 1011: 60us minimum elapsed time ... 1100: 70us minimum elapsed time ... 1101: 80us minimum elapsed time ... 1110: 90us minimum elapsed time ... 1111: 100us minimum elapsed time ... Note: The effective time to restart the CLKOUT_SRCn should be the larger of the programmed minimum delay, or of the normal natural latency to restart the clock from the current powered state of ICC. The effective time must not be cummulative. 0us minimum elapsed time setting results in the normal latency that would be incurred to restart the CLKOUT_SRCn from the current state of ICC, i.e. if PLL source is already up and only the CLKOUT_SRCn is being gated, then the effective latency is the normal delay to ungate the clock at the output buffer. If PLL source has been power managed off, then the effective latency is the normal delay to restart the PLL, divider, and to ungate the clock at the output buffer. No other additional delay is incurred. Non-zero minimum elapsed time setting should result in similar delay as 0us minimum case described above when the normal latency for clock restart is naturally larger than the programmed setting. Non-zero minimum elapsed time setting should only result in the programmed latency when the normal latency for clock restart, with respect to the current state of ICC, is smaller than the programmed setting. BIOS is expected to program this register field based on its discovery of the PCIe device capabilities, such as device support for L1Off, and device Tpowerup timing. Trefclk_min is enforced by ICC only when the PCIe link is exiting from L1.OFF state where the device is unpowered. ICC will not enforce Trefclk_min when the link is exiting from other L1 improved states, such as L1.SNOOZE where the device is still powered for lower latency L1 improved exit. PCIe root port communicates this port state distinction to ICC. Port state information is communicated per port and is mapped 1:1 with the raw SRCCLKREQB_n from GPIO, i.e. port 0 state is associated with SRCCLKREQB_0. Thus the mapping function of CLKREQ# to CLKOUTSRC also needs to be applied to port state information prior to use. Implementation Note: ICC core logic does not have visibility of CLKOUT_SRC[...] source multiplexing since MUX control register is buried inside iSCLK HIP. In the event CLKOUT_SRC[...] is not sourcing 100Mhz clock from USB3/Gen2PCIe PLL, i.e. it is sourcing MEX or TBT ref clock instead, the effective mapped CLKREQ# assertion should not result in upstream clock request to 100Mhz source USB3/Gen2PCIe PLL. This case is naturally handled by iSCLK HIPs demuxing effective mapped CLKREQ# that it sees and hierarchically forming clkreq upstream to respective sources since iSCLK HIP has visibility of MUX control. Problematic is the case where ICC core forms surrogate clkreq directly to USB3/Gen2PCIe PLL when effective mapped CLKREQ# asserts. Since ICC does not have visibility of the clock MUX, it does not really know whether the mapped CLKREQ# is targetted USB 3/Gen2PCIe source or MIPI or other sources. The plan to address this case is that ICC core should not assert the surrogate clkreq to USB3/Gen2PCIe PLL unless it is enforcing this L1.Off Trefclkmin timing, i.e. register field at a non-zero setting implies that clock usage is indeed PCIe SRC clock with special case of L1.OFF Trefclkmin enforcement and thus ICC surrogate clkreq assertion will indeed target the right clock source. For the zero setting case, the normal hierarchical clkreq aggregation through iSCLK HIP should always be in control since iSCLK has information to differentiate sources for the effective mapped CLKREQ#.

31.1.2 Timing Control SRC Clock Register 2 (TMCSRCCLK2)—Offset 1004h

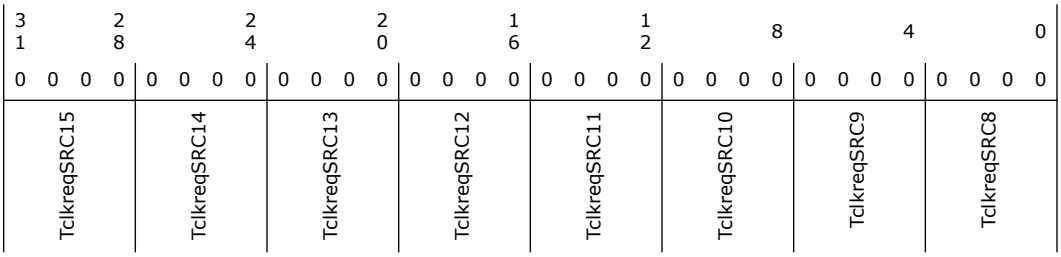
Controls minimum enable timing of PCIe SRC Clocks for support of PCIe L1Off using CLKREQ#

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RW	**Minimum Time from Effective Mapped CLKREQ# assertion to CLKOUT_SRC15 ungated (TclkreqSRC15):** See description for TclkreqSRC0 field[3:0]
27:24	0h RW	**Minimum Time from Effective Mapped CLKREQ# assertion to CLKOUT_SRC14 ungated (TclkreqSRC14):** See description for TclkreqSRC0 field[3:0]
23:20	0h RW	**Minimum Time from Effective Mapped CLKREQ# assertion to CLKOUT_SRC13 ungated (TclkreqSRC13):** See description for TclkreqSRC0 field[3:0]
19:16	0h RW	**Minimum Time from Effective Mapped CLKREQ# assertion to CLKOUT_SRC12 ungated (TclkreqSRC12):** See description for TclkreqSRC0 field[3:0]
15:12	0h RW	**Minimum Time from Effective Mapped CLKREQ# assertion to CLKOUT_SRC11 ungated (TclkreqSRC11):** See description for TclkreqSRC0 field[3:0]
11:8	0h RW	**Minimum Time from Effective Mapped CLKREQ# assertion to CLKOUT_SRC10 ungated (TclkreqSRC10):** See description for TclkreqSRC0 field[3:0]
7:4	0h RW	**Minimum Time from Effective Mapped CLKREQ# assertion to CLKOUT_SRC9 ungated (TclkreqSRC9):** See description for TclkreqSRC0 field[3:0]
3:0	0h RW	**Minimum Time from Effective Mapped CLKREQ# assertion to CLKOUT_SRC8 ungated (TclkreqSRC8):** See description for TclkreqSRC0 field[3:0]

31.1.3 Enable Control CLKREQ (ENCCKRQ)—Offset 1008h

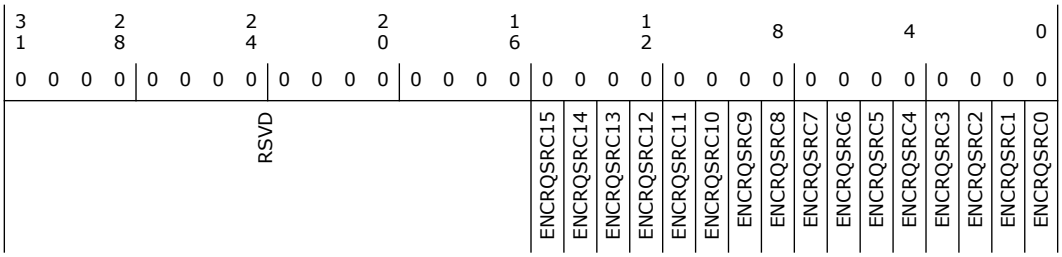
Controls enabling of Mapped CLKREQ#s for SRC clocks

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD):** Reserved
15	0h RW	**Enable Maskable Mapped CLKREQ# for CLKOUT_SRC15 (ENCRQSRC15):** Enable dynamic control of CLKOUT_SRC15 by the Maskable Mapped CLKREQ#. See description for ENCRQSRC0.
14	0h RW	**Enable Maskable Mapped CLKREQ# for CLKOUT_SRC14 (ENCRQSRC14):** Enable dynamic control of CLKOUT_SRC14 by the Maskable Mapped CLKREQ#. See description for ENCRQSRC0.
13	0h RW	**Enable Maskable Mapped CLKREQ# for CLKOUT_SRC13 (ENCRQSRC13):** Enable dynamic control of CLKOUT_SRC13 by the Maskable Mapped CLKREQ#. See description for ENCRQSRC0.
12	0h RW	**Enable Maskable Mapped CLKREQ# for CLKOUT_SRC12 (ENCRQSRC12):** Enable dynamic control of CLKOUT_SRC12 by the Maskable Mapped CLKREQ#. See description for ENCRQSRC0.
11	0h RW	**Enable Maskable Mapped CLKREQ# for CLKOUT_SRC11 (ENCRQSRC11):** Enable dynamic control of CLKOUT_SRC11 by the Maskable Mapped CLKREQ#. See description for ENCRQSRC0.
10	0h RW	**Enable Maskable Mapped CLKREQ# for CLKOUT_SRC10 (ENCRQSRC10):** Enable dynamic control of CLKOUT_SRC10 by the Maskable Mapped CLKREQ#. See description for ENCRQSRC0.
9	0h RW	**Enable Maskable Mapped CLKREQ# for CLKOUT_SRC9 (ENCRQSRC9):** Enable dynamic control of CLKOUT_SRC9 by the Maskable Mapped CLKREQ#. See description for ENCRQSRC0.
8	0h RW	**Enable Maskable Mapped CLKREQ# for CLKOUT_SRC8 (ENCRQSRC8):** Enable dynamic control of CLKOUT_SRC8 by the Maskable Mapped CLKREQ#. See description for ENCRQSRC0.
7	0h RW	**Enable Maskable Mapped CLKREQ# for CLKOUT_SRC7 (ENCRQSRC7):** Enable dynamic control of CLKOUT_SRC7 by the Maskable Mapped CLKREQ#. See description for ENCRQSRC0.
6	0h RW	**Enable Maskable Mapped CLKREQ# for CLKOUT_SRC6 (ENCRQSRC6):** Enable dynamic control of CLKOUT_SRC6 by the Maskable Mapped CLKREQ#. See description for ENCRQSRC0.
5	0h RW	**Enable Maskable Mapped CLKREQ# for CLKOUT_SRC5 (ENCRQSRC5):** Enable dynamic control of CLKOUT_SRC5 by the Maskable Mapped CLKREQ#. See description for ENCRQSRC0.
4	0h RW	**Enable Maskable Mapped CLKREQ# for CLKOUT_SRC4 (ENCRQSRC4):** Enable dynamic control of CLKOUT_SRC4 by the Maskable Mapped CLKREQ#. See description for ENCRQSRC0.
3	0h RW	**Enable Maskable Mapped CLKREQ# for CLKOUT_SRC3 (ENCRQSRC3):** Enable dynamic control of CLKOUT_SRC3 by the Maskable Mapped CLKREQ#. See description for ENCRQSRC0.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Enable Maskable Mapped CLKREQ# for CLKOUT_SRC2 (ENCRQSRC2):** Enable dynamic control of CLKOUT_SRC2 by the Maskable Mapped CLKREQ#. See description for ENCRQSRC0.
1	0h RW	**Enable Maskable Mapped CLKREQ# for CLKOUT_SRC1 (ENCRQSRC1):** Enable dynamic control of CLKOUT_SRC1 by the Maskable Mapped CLKREQ#. See description for ENCRQSRC0.
0	0h RW	**Enable Maskable Mapped CLKREQ# for CLKOUT_SRC0 (ENCRQSRC0):** Enable dynamic control of CLKOUT_SRC0 by the Maskable Mapped CLKREQ#. This register bit may be updated dynamically. Hardware design must support this usage model. 0: Disable dynamic control of CLKOUT_SRCn - Default 1: Enable dynamic control of CLKOUT_SRCn by the maskable mapped CLKREQ# When enabled by this register bit, CLKOUT_SRCn is subject to gating/ungating control by the maskable mapped CLKREQ#. Furthermore, when latency tolerance permits, the maskable mapped CLKREQ# de-assertion allows for PLL source shutdown following the gating of CLKOUT_SRCn. Actual PLL shutdown accounts for votes from all other clock consumers of shared PLL source. When the maskable mapped CLKREQ# re-asserts, the minimum latency to restart the output clock is subject to the L1.Off Trefclkmin field TclkreqSRCn, register TMCSRCCLK. When disabled by this register bit, CLKOUT_SRCn is insensitive to the state of the maskable mapped CLKREQ#. CLKOUT_SRCn is either always running after ICC initialization, or always gated as globally configured via the corresponding CLKEN bit (residing inside iSCLK HIP register set.) Note: The output of this processing is referred to as Effective Mapped CLKREQ# Implementation Note: Effective Mapped CLKREQn# = Maskable Mapped CLKREQn# AND ENCRQSRCn Normally, PMC aggregates latency tolerance (LTR) messages from LTR-capable PCIe devices and communicates as PLL shutdown allow to clocking hardware. As corner case, BIOS will discover existence of any non-LTR-capable PCIe device and communicates to PMC for the purpose of overriding PLL shutdown allow to prevent violating PCIe legacy CLKREQ# to output clock valid timing.

31.1.4 Mask Control CLKREQ (MSKCKRQ)—Offset 100Ch

Controls Masking of Mapped CLKREQ#s for SRC clocks

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RSVD																MSKCRQSRC15	MSKCRQSRC14	MSKCRQSRC13	MSKCRQSRC12	MSKCRQSRC11	MSKCRQSRC10	MSKCRQSRC9	MSKCRQSRC8	MSKCRQSRC7	MSKCRQSRC6	MSKCRQSRC5	MSKCRQSRC4	MSKCRQSRC3	MSKCRQSRC2	MSKCRQSRC1	MSKCRQSRC0

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved (RSVD):** Reserved
15	0h RW	**Mask Enable of Mapped CLKREQ# for CLKOUT_SRC15 (MSKCRQSRC15):** Force to inactive state the Mapped CLKREQ# for CLKOUT_SRC15. See description for MSKCRQSRC0.
14	0h RW	**Mask Enable of Mapped CLKREQ# for CLKOUT_SRC14 (MSKCRQSRC14):** Force to inactive state the Mapped CLKREQ# for CLKOUT_SRC14. See description for MSKCRQSRC0.
13	0h RW	**Mask Enable of Mapped CLKREQ# for CLKOUT_SRC13 (MSKCRQSRC13):** Force to inactive state the Mapped CLKREQ# for CLKOUT_SRC13. See description for MSKCRQSRC0.
12	0h RW	**Mask Enable of Mapped CLKREQ# for CLKOUT_SRC12 (MSKCRQSRC12):** Force to inactive state the Mapped CLKREQ# for CLKOUT_SRC12. See description for MSKCRQSRC0.
11	0h RW	**Mask Enable of Mapped CLKREQ# for CLKOUT_SRC11 (MSKCRQSRC11):** Force to inactive state the Mapped CLKREQ# for CLKOUT_SRC11. See description for MSKCRQSRC0.
10	0h RW	**Mask Enable of Mapped CLKREQ# for CLKOUT_SRC10 (MSKCRQSRC10):** Force to inactive state the Mapped CLKREQ# for CLKOUT_SRC10. See description for MSKCRQSRC0.
9	0h RW	**Mask Enable of Mapped CLKREQ# for CLKOUT_SRC9 (MSKCRQSRC9):** Force to inactive state the Mapped CLKREQ# for CLKOUT_SRC9. See description for MSKCRQSRC0.
8	0h RW	**Mask Enable of Mapped CLKREQ# for CLKOUT_SRC8 (MSKCRQSRC8):** Force to inactive state the Mapped CLKREQ# for CLKOUT_SRC8. See description for MSKCRQSRC0.
7	0h RW	**Mask Enable of Mapped CLKREQ# for CLKOUT_SRC7 (MSKCRQSRC7):** Force to inactive state the Mapped CLKREQ# for CLKOUT_SRC7. See description for MSKCRQSRC0.
6	0h RW	**Mask Enable of Mapped CLKREQ# for CLKOUT_SRC6 (MSKCRQSRC6):** Force to inactive state the Mapped CLKREQ# for CLKOUT_SRC6. See description for MSKCRQSRC0.
5	0h RW	**Mask Enable of Mapped CLKREQ# for CLKOUT_SRC5 (MSKCRQSRC5):** Force to inactive state the Mapped CLKREQ# for CLKOUT_SRC5. See description for MSKCRQSRC0.
4	0h RW	**Mask Enable of Mapped CLKREQ# for CLKOUT_SRC4 (MSKCRQSRC4):** Force to inactive state the Mapped CLKREQ# for CLKOUT_SRC4. See description for MSKCRQSRC0.
3	0h RW	**Mask Enable of Mapped CLKREQ# for CLKOUT_SRC3 (MSKCRQSRC3):** Force to inactive state the Mapped CLKREQ# for CLKOUT_SRC3. See description for MSKCRQSRC0.
2	0h RW	**Mask Enable of Mapped CLKREQ# for CLKOUT_SRC2 (MSKCRQSRC2):** Force to inactive state the Mapped CLKREQ# for CLKOUT_SRC2. See description for MSKCRQSRC0.
1	0h RW	**Mask Enable of Mapped CLKREQ# for CLKOUT_SRC1 (MSKCRQSRC1):** Force to inactive state the Mapped CLKREQ# for CLKOUT_SRC1. See description for MSKCRQSRC0.
0	0h RW	**Mask Enable of Mapped CLKREQ# for CLKOUT_SRC0 (MSKCRQSRC0):** Force to inactive state the Mapped CLKREQ# for CLKOUT_SRC0. This register bit may be updated dynamically. Hardware design must support this usage model. 0: No mask applied on the Mapped CLKREQ# for CLKOUT_SRCn - Default 1: Mask Mapped CLKREQ# for CLKOUT_SRCn to inactive state Note: The output of this processing is referred to as Maskable Mapped CLKREQ# Maskable Mapped CLKREQ# = Mapped CLKREQ# OR MSKCRQSRCn

31.1.5 ICC Security (ICCSEC)—Offset 1020h

Notes:
Exclude ICCSFBV, RO register - Nothing to protect
Hard IP blocks behind CRI of CCU - This architecture is not supported in SPT. Should

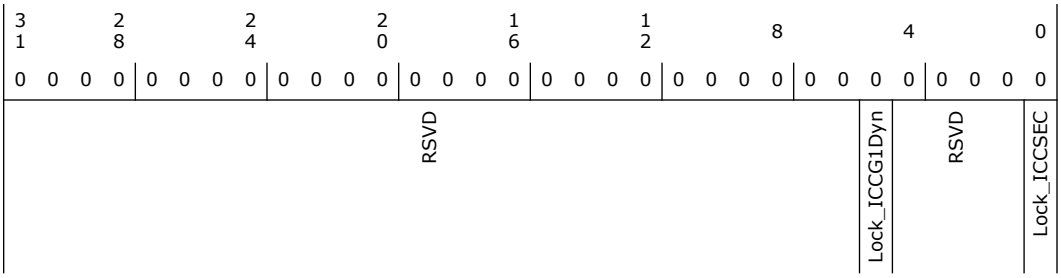
future PCHs move to this chassis-compliant architecture, it is assumed that granularity of lock is that each CRI target is one entire lockable resource. Entire CRI target is or is not to be locked down. No capability to lock at finer granularity of register sets inside each CRI target. With this organization, ICC decodes the address bits representing CRI targets and if that range is locked, ICC suppresses the CRI cycle.
Categorize as dynamic vs. static group of registers -
o Static group intended usage would not involved BIOS programming. So separating them from dynamic group to allow locking down ahead of BIOS boot.
o Dynamic group intended usage could involve BIOS programming and could be left unlocked for BIOS to program, then lock after boot.
Also separate those, if tampered with by malware would only cause host functional failures vs. those if tampered with could potentially cause permanent hardware damage. Those of the latter characteristic would never be left unlocked. Those of the former characteristic could be left unlocked if the usage model required host access.

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW/L	**Lock Bit for Group 1 of Dynamically Configured ICC Registers (Lock_ICCG1Dyn):** This lock bit covers registers TMCSRCCLK, TMCSRCCLK2, ENCCKRQ 0: Target endpoint will accept all incoming requests as normal. 1: Target endpoint will deny incoming requests addressed to above listed ICC Registers, unless those requests are attributed with CSME SAI or PMC SAI. When denying a request, target endpoint will generate a completion packet as follows: Read will complete without data as Unsuccessful on IOSFSB (normally read completes with data as Successful on IOSFSB), Non-posted Write will complete without data as Unsuccessful on IOSFSB (normally non-posted write completes without data as Successful on IOSFSB) and the Write does not take effect at the register (i.e. register content is not affected.) Assumptions on potential usage model of these registers: TMCSRCCLK, TMCSRCCLK2 - BIOS updates values of these registers based on its discovering of PCIe device Tpowerup time and L1.Off capability. Hot plug usage model would require runtime update of register. If not locked, an attack can disable Trefclkmin enforcement and cause PCH to drive into unpowered PCIe device, potentially causing hardware reliability issue to the device. ENCCKRQ - BIOS updates value of this register after having configured the above TMCSRCCLK, TMCSRCCLK2 registers. If not locked, an attack can disable PCH tracking of CLKREQ#, causing PCH to drive clock when not wanted. If the device receiving this unwanted clock happens to be in unpowered state, then there is a potential hardware reliability issue to the device.
4:1	0h RO	Reserved.
0	0h RW/L	**Lock Bit for ICC Security Register (Lock_ICCSEC):** This lock bit covers register ICCSEC, i.e. this same register where this lock bit resides. 0: Target endpoint will accept all incoming requests as normal. 1: Target endpoint will deny incoming requests addressed to ICCSEC register, unless those requests are attributed with CSME SAI. When denying a request, target endpoint will generate a completion packet as follows: Read will complete without data as Unsuccessful on IOSFSB (normally read completes with data as Successful on IOSFSB), Non-posted Write will complete without data as Unsuccessful on IOSFSB (normally non-posted write completes without data as Successful on IOSFSB) and the Write does not take effect at the register (i.e. register content is not affected.)

31.1.6 CLKREQ Mapping to CLKOUT_SRC (CKRQMAPSRC)—Offset 1024h

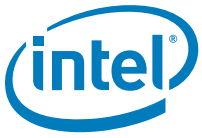
Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 76543210h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	0	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0
CRQSELSRC7				CRQSELSRC6				CRQSELSRC5				CRQSELSRC4				CRQSELSRC3				CRQSELSRC2				CRQSELSRC1				CRQSELSRC0			



Bit Range	Default & Access	Field Name (ID): Description
31:28	7h RW	**CLKRQ# Select for CLKOUT_SRC7 (CRQSELSRC7):** Select version of external input CLKRQ# for dynamic control of the output CLKOUT_SRC7. 0000: SRCCLKREQB_0 controls CLKOUT_SRC7 0001: SRCCLKREQB_1 controls CLKOUT_SRC7 0010: SRCCLKREQB_2 controls CLKOUT_SRC7 0011: SRCCLKREQB_3 controls CLKOUT_SRC7 0100: SRCCLKREQB_4 controls CLKOUT_SRC7 0101: SRCCLKREQB_5 controls CLKOUT_SRC7 0110: SRCCLKREQB_6 controls CLKOUT_SRC7 0111: SRCCLKREQB_7 controls CLKOUT_SRC7 - Default 1000-1111: Reserved Note: The output of this processing is referred to as Mapped CLKREQ#
27:24	6h RW	**CLKRQ# Select for CLKOUT_SRC6 (CRQSELSRC6):** Select version of external input CLKRQ# for dynamic control of the output CLKOUT_SRC6. 0000: SRCCLKREQB_0 controls CLKOUT_SRC6 0001: SRCCLKREQB_1 controls CLKOUT_SRC6 0010: SRCCLKREQB_2 controls CLKOUT_SRC6 0011: SRCCLKREQB_3 controls CLKOUT_SRC6 0100: SRCCLKREQB_4 controls CLKOUT_SRC6 0101: SRCCLKREQB_5 controls CLKOUT_SRC6 0110: SRCCLKREQB_6 controls CLKOUT_SRC6 - Default 0111: SRCCLKREQB_7 controls CLKOUT_SRC6 1000-1111: Reserved Note: The output of this processing is referred to as Mapped CLKREQ#
23:20	5h RW	**CLKRQ# Select for CLKOUT_SRC5 (CRQSELSRC5):** Select version of external input CLKRQ# (or internally generated version when applicable) for dynamic control of the output CLKOUT_SRC5. 0000: SRCCLKREQB_0 controls CLKOUT_SRC5 0001: SRCCLKREQB_1 controls CLKOUT_SRC5 0010: SRCCLKREQB_2 controls CLKOUT_SRC5 0011: SRCCLKREQB_3 controls CLKOUT_SRC5 0100: SRCCLKREQB_4 controls CLKOUT_SRC5 0101: SRCCLKREQB_5 controls CLKOUT_SRC5 - Default 0110: SRCCLKREQB_6 controls CLKOUT_SRC5 - SPT-H only, Reserved for SPT-LP 0111: SRCCLKREQB_7 controls CLKOUT_SRC5 - SPT-H only, Reserved for SPT-LP 1000: UFSCLKREQB controls CLKOUT_SRC5 - Use when CLKOUT_SRC5 is configured to source UFS reference clock (i.e. 19.2Mhz) 1001: Reserved 1010-1111: Reserved Note: The output of this processing is referred to as Mapped CLKREQ#
19:16	4h RW	**CLKRQ# Select for CLKOUT_SRC4 (CRQSELSRC4):** Select version of external input CLKRQ# for dynamic control of the output CLKOUT_SRC4. 0000: SRCCLKREQB_0 controls CLKOUT_SRC4 0001: SRCCLKREQB_1 controls CLKOUT_SRC4 0010: SRCCLKREQB_2 controls CLKOUT_SRC4 0011: SRCCLKREQB_3 controls CLKOUT_SRC4 0100: SRCCLKREQB_4 controls CLKOUT_SRC4 - Default 0101: SRCCLKREQB_5 controls CLKOUT_SRC4 0110: SRCCLKREQB_6 controls CLKOUT_SRC4 - SPT-H only, Reserved for SPT-LP 0111: SRCCLKREQB_7 controls CLKOUT_SRC4 - SPT-H only, Reserved for SPT-LP 1000: Reserved 1001: Reserved 1010-1111: Reserved Note: The output of this processing is referred to as Mapped CLKREQ#
15:12	3h RW	**CLKRQ# Select for CLKOUT_SRC3 (CRQSELSRC3):** Select version of external input CLKRQ# for dynamic control of the output CLKOUT_SRC3. 0000: SRCCLKREQB_0 controls CLKOUT_SRC3 0001: SRCCLKREQB_1 controls CLKOUT_SRC3 0010: SRCCLKREQB_2 controls CLKOUT_SRC3 0011: SRCCLKREQB_3 controls CLKOUT_SRC3 - Default 0100: SRCCLKREQB_4 controls CLKOUT_SRC3 0101: SRCCLKREQB_5 controls CLKOUT_SRC3 0110: SRCCLKREQB_6 controls CLKOUT_SRC3 - SPT-H only, Reserved for SPT-LP 0111: SRCCLKREQB_7 controls CLKOUT_SRC3 - SPT-H only, Reserved for SPT-LP 1000-1111: Reserved Note: The output of this processing is referred to as Mapped CLKREQ#

Bit Range	Default & Access	Field Name (ID): Description
11:8	2h RW	**CLKRQ# Select for CLKOUT_SRC2 (CRQSELSRC2):** Select version of external input CLKRQ# for dynamic control of the output CLKOUT_SRC2. 0000: SRCCLKREQB_0 controls CLKOUT_SRC2 0001: SRCCLKREQB_1 controls CLKOUT_SRC2 0010: SRCCLKREQB_2 controls CLKOUT_SRC2 - Default 0011: SRCCLKREQB_3 controls CLKOUT_SRC2 0100: SRCCLKREQB_4 controls CLKOUT_SRC2 0101: SRCCLKREQB_5 controls CLKOUT_SRC2 0110: SRCCLKREQB_6 controls CLKOUT_SRC2 - SPT-H only, Reserved for SPT-LP 0111: SRCCLKREQB_7 controls CLKOUT_SRC2 - SPT-H only, Reserved for SPT-LP 1000-1111: Reserved Note: The output of this processing is referred to as Mapped CLKREQ#
7:4	1h RW	**CLKRQ# Select for CLKOUT_SRC1 (CRQSELSRC1):** Select version of external input CLKRQ# for dynamic control of the output CLKOUT_SRC1. 0000: SRCCLKREQB_0 controls CLKOUT_SRC1 0001: SRCCLKREQB_1 controls CLKOUT_SRC1 - Default 0010: SRCCLKREQB_2 controls CLKOUT_SRC1 0011: SRCCLKREQB_3 controls CLKOUT_SRC1 0100: SRCCLKREQB_4 controls CLKOUT_SRC1 0101: SRCCLKREQB_5 controls CLKOUT_SRC1 0110: SRCCLKREQB_6 controls CLKOUT_SRC1 - SPT-H only, Reserved for SPT-LP 0111: SRCCLKREQB_7 controls CLKOUT_SRC1 - SPT-H only, Reserved for SPT-LP 1000-1111: Reserved Note: The output of this processing is referred to as Mapped CLKREQ#
3:0	0h RW	**CLKRQ# Select for CLKOUT_SRC0 (CRQSELSRC0):** Select version of external input CLKRQ# for dynamic control of the output CLKOUT_SRC0. 0000: SRCCLKREQB_0 controls CLKOUT_SRC0 - Default 0001: SRCCLKREQB_1 controls CLKOUT_SRC0 0010: SRCCLKREQB_2 controls CLKOUT_SRC0 0011: SRCCLKREQB_3 controls CLKOUT_SRC0 0100: SRCCLKREQB_4 controls CLKOUT_SRC0 0101: SRCCLKREQB_5 controls CLKOUT_SRC0 0110: SRCCLKREQB_6 controls CLKOUT_SRC0 - SPT-H only, Reserved for SPT-LP 0111: SRCCLKREQB_7 controls CLKOUT_SRC0 - SPT-H only, Reserved for SPT-LP 1000-1111: Reserved Note: The output of this processing is referred to as Mapped CLKREQ#

31.1.7 CLKREQ Mapping to CLKOUT_SRC Register 2 (CKRQMAPSRC2)—Offset 1028h

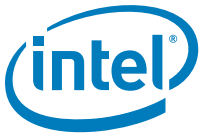
Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 76543210h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	0	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0
CRQSELSRC15				CRQSELSRC14				CRQSELSRC13				CRQSELSRC12				CRQSELSRC11				CRQSELSRC10				CRQSELSRC9				CRQSELSRC8			



Bit Range	Default & Access	Field Name (ID): Description
31:28	7h RW	**CLKRQ# Select for CLKOUT_SRC15 (CRQSELSRC15):** Select version of external input CLKRQ# for dynamic control of the output CLKOUT_SRC15. 0000: SRCCLKREQB_8 controls CLKOUT_SRC15 0001: SRCCLKREQB_9 controls CLKOUT_SRC15 0010: SRCCLKREQB_10 controls CLKOUT_SRC15 0011: SRCCLKREQB_11 controls CLKOUT_SRC15 0100: SRCCLKREQB_12 controls CLKOUT_SRC15 0101: SRCCLKREQB_13 controls CLKOUT_SRC15 0110: SRCCLKREQB_14 controls CLKOUT_SRC15 0111: SRCCLKREQB_15 controls CLKOUT_SRC15 - Default 1000-1111: Reserved Note: The output of this processing is referred to as Mapped CLKREQ#
27:24	6h RW	**CLKRQ# Select for CLKOUT_SRC14 (CRQSELSRC14):** Select version of external input CLKRQ# for dynamic control of the output CLKOUT_SRC14. 0000: SRCCLKREQB_8 controls CLKOUT_SRC14 0001: SRCCLKREQB_9 controls CLKOUT_SRC14 0010: SRCCLKREQB_10 controls CLKOUT_SRC14 0011: SRCCLKREQB_11 controls CLKOUT_SRC14 0100: SRCCLKREQB_12 controls CLKOUT_SRC14 0101: SRCCLKREQB_13 controls CLKOUT_SRC14 0110: SRCCLKREQB_14 controls CLKOUT_SRC14 - Default 0111: SRCCLKREQB_15 controls CLKOUT_SRC14 1000-1111: Reserved Note: The output of this processing is referred to as Mapped CLKREQ#
23:20	5h RW	**CLKRQ# Select for CLKOUT_SRC13 (CRQSELSRC13):** Select version of external input CLKRQ# for dynamic control of the output CLKOUT_SRC13. 0000: SRCCLKREQB_8 controls CLKOUT_SRC13 0001: SRCCLKREQB_9 controls CLKOUT_SRC13 0010: SRCCLKREQB_10 controls CLKOUT_SRC13 0011: SRCCLKREQB_11 controls CLKOUT_SRC13 0100: SRCCLKREQB_12 controls CLKOUT_SRC13 0101: SRCCLKREQB_13 controls CLKOUT_SRC13 - Default 0110: SRCCLKREQB_14 controls CLKOUT_SRC13 0111: SRCCLKREQB_15 controls CLKOUT_SRC13 1000-1111: Reserved Note: The output of this processing is referred to as Mapped CLKREQ#
19:16	4h RW	**CLKRQ# Select for CLKOUT_SRC12 (CRQSELSRC12):** Select version of external input CLKRQ# for dynamic control of the output CLKOUT_SRC12. 0000: SRCCLKREQB_8 controls CLKOUT_SRC12 0001: SRCCLKREQB_9 controls CLKOUT_SRC12 0010: SRCCLKREQB_10 controls CLKOUT_SRC12 0011: SRCCLKREQB_11 controls CLKOUT_SRC12 0100: SRCCLKREQB_12 controls CLKOUT_SRC12 - Default 0101: SRCCLKREQB_13 controls CLKOUT_SRC12 0110: SRCCLKREQB_14 controls CLKOUT_SRC12 0111: SRCCLKREQB_15 controls CLKOUT_SRC12 1000-1111: Reserved Note: The output of this processing is referred to as Mapped CLKREQ#
15:12	3h RW	**CLKRQ# Select for CLKOUT_SRC11 (CRQSELSRC11):** Select version of external input CLKRQ# for dynamic control of the output CLKOUT_SRC11. 0000: SRCCLKREQB_8 controls CLKOUT_SRC11 0001: SRCCLKREQB_9 controls CLKOUT_SRC11 0010: SRCCLKREQB_10 controls CLKOUT_SRC11 0011: SRCCLKREQB_11 controls CLKOUT_SRC11 - Default 0100: SRCCLKREQB_12 controls CLKOUT_SRC11 0101: SRCCLKREQB_13 controls CLKOUT_SRC11 0110: SRCCLKREQB_14 controls CLKOUT_SRC11 0111: SRCCLKREQB_15 controls CLKOUT_SRC11 1000-1111: Reserved Note: The output of this processing is referred to as Mapped CLKREQ#

Bit Range	Default & Access	Field Name (ID): Description
11:8	2h RW	**CLKRQ# Select for CLKOUT_SRC10 (CRQSELSRC10):** Select version of external input CLKRQ# for dynamic control of the output CLKOUT_SRC10. 0000: SRCCLKREQB_8 controls CLKOUT_SRC10 0001: SRCCLKREQB_9 controls CLKOUT_SRC10 0010: SRCCLKREQB_10 controls CLKOUT_SRC10 - Default 0011: SRCCLKREQB_11 controls CLKOUT_SRC10 0100: SRCCLKREQB_12 controls CLKOUT_SRC10 0101: SRCCLKREQB_13 controls CLKOUT_SRC10 0110: SRCCLKREQB_14 controls CLKOUT_SRC10 0111: SRCCLKREQB_15 controls CLKOUT_SRC10 1000-1111: Reserved Note: The output of this processing is referred to as Mapped CLKREQ#
7:4	1h RW	**CLKRQ# Select for CLKOUT_SRC9 (CRQSELSRC9):** Select version of external input CLKRQ# for dynamic control of the output CLKOUT_SRC9. 0000: SRCCLKREQB_8 controls CLKOUT_SRC9 0001: SRCCLKREQB_9 controls CLKOUT_SRC9 - Default 0010: SRCCLKREQB_10 controls CLKOUT_SRC9 0011: SRCCLKREQB_11 controls CLKOUT_SRC9 0100: SRCCLKREQB_12 controls CLKOUT_SRC9 0101: SRCCLKREQB_13 controls CLKOUT_SRC9 0110: SRCCLKREQB_14 controls CLKOUT_SRC9 0111: SRCCLKREQB_15 controls CLKOUT_SRC9 1000-1111: Reserved Note: The output of this processing is referred to as Mapped CLKREQ#
3:0	0h RW	**CLKRQ# Select for CLKOUT_SRC8 (CRQSELSRC8):** Select version of external input CLKRQ# for dynamic control of the output CLKOUT_SRC8. 0000: SRCCLKREQB_8 controls CLKOUT_SRC8 - Default 0001: SRCCLKREQB_9 controls CLKOUT_SRC8 0010: SRCCLKREQB_10 controls CLKOUT_SRC8 0011: SRCCLKREQB_11 controls CLKOUT_SRC8 0100: SRCCLKREQB_12 controls CLKOUT_SRC8 0101: SRCCLKREQB_13 controls CLKOUT_SRC8 0110: SRCCLKREQB_14 controls CLKOUT_SRC8 0111: SRCCLKREQB_15 controls CLKOUT_SRC8 1000-1111: Reserved Note: The output of this processing is referred to as Mapped CLKREQ#

31.1.8 Power Management (PM)—Offset 102Ch

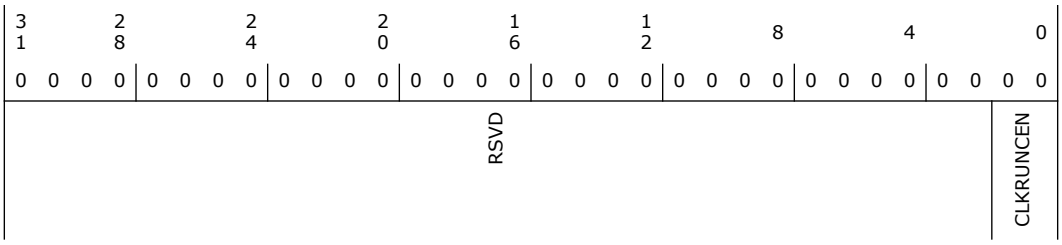
Controls the power management features of clocks

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RW	**CLKRUN Control Enable (CLKRUNCEN):** Controls the enabling of support for CLKRUN protocol. 0 - the corresponding CLKOUT_LPC is free-running, unaffected by CLKRUN protocol 1 - the corresponding CLKOUT_LPC is shut off when CLKRUN protocol turns off LPC clocks

31.1.9 ICC Debug (ICCDBG)—Offset 1034h

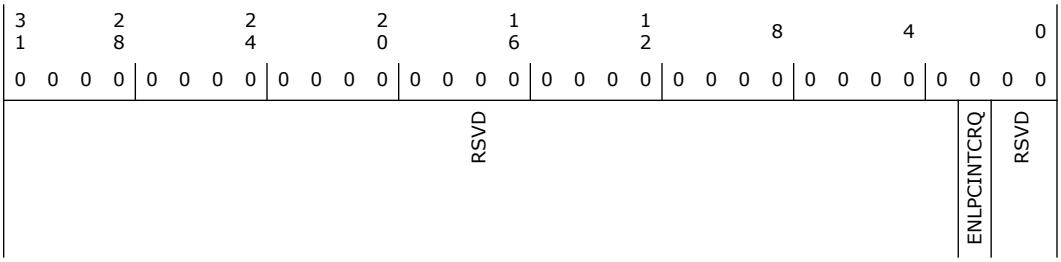
Debug / Chicken Bits for ICC logic

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	Reserved.
2	0h RW	**Enable LPCINTCLKREQ for CLKOUT_LPCINT and CLKOUT_LPCINTDLY (ENLPCINTCRQ):** Enable dynamic control of CLKOUT_LPCINT and CLKOUT_LPCINTDLY by LPCINTCLKREQ from legacy function. 0: Disable dynamic control of CLKOUT_LPCINT and CLKOUT_LPCINTDLY - Default 1: Enable dynamic control of CLKOUT_LPCINT and CLKOUT_LPCINTDLY When enabled by this register bit, CLKOUT_LPCINT and CLKOUT_LPCINTDLY are subject to gating/ungating control by LPCINTCLKREQ from the legacy function. When disabled by this register bit, these clocks are insensitive to the state of LPCINTCLKREQ from the legacy function, and are always running after ICC initialization. Implementation note: Effective LPCINTCLKREQ = LPCINTCLKREQ + ! ENLPCINTCRQ,
1:0	0h RO	Reserved.

31.1.10 USB3Gen2PCIe PLL Control (G2PLLCTRL)—Offset 2000h

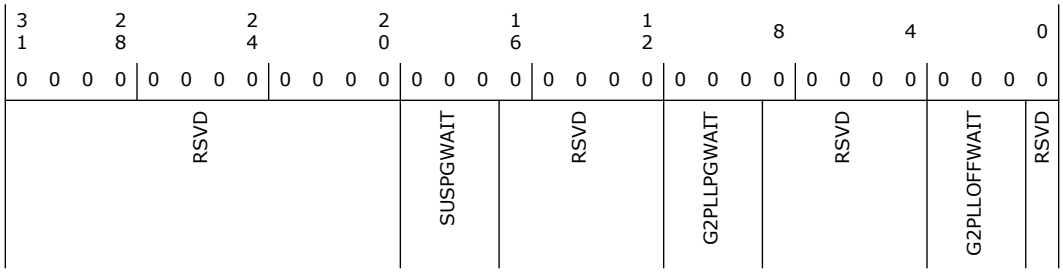
Controls USB3Gen2PCIe PLL and its output clocks behavior. This offset is lockable by setting LOCK_G2PLLC bit (ICCSEC offset 1020h bit 10).

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	Reserved.
19:17	0h RW	**Run-time S0 SUS PG Wait (SUSPGWAIT):** Upon the USB3Gen2PCIe PLL shutdown and power gated, a timer is started. Any wake event occurring before the timer expires causes the timer to reset to SUSPGWAIT value. Once the timer expires and there are no wake events, the SUS well power to ModPHY USB3Gen2PCIe PLL can be gated. 000: 0us - Default 001: 1us 010: 2us 011: 4us 100: 8us 101: 16us 110: 32us 111: reserved
16:12	0h RO	Reserved.
11:9	0h RW	**USB3Gen2PCIe PLL PG Wait (G2PLLPGWAIT):** Upon the USB3Gen2PCIe PLL shutdown, a timer is started. Any wake event occurring before the timer expires causes the timer to reset to G2PLLPGWAIT value. Once the timer expires and there are no wake events, the USB3Gen2PCIe PLL can be power gated. 000: 0us - Default 001: 1us 010: 2us 011: 4us 100: 8us 101: 16us 110: 32us 111: reserved
8:4	0h RO	Reserved.
3:1	0h RW	**USB3Gen2PCIe PLL OFF Wait (G2PLLOFFWAIT):** Upon the event that all conditions (other than this G2PLLOFFWAIT timer itself) are satisfied for USB3Gen2PCIe PLL shutdown, a timer is started. Any wake event occurring before the timer expires causes the timer to reset to G2PLLOFFWAIT value. Once the timer expires and there are no wake events, the USB3Gen2PCIe PLL can be shutdown. 000: 0us - Default 001: 1us 010: 2us 011: 4us 100: 8us 101: 16us 110: 32us 111: reserved
0	0h RO	Reserved.

§ §

32 Interrupt

32.1 Interrupt Registers Summary

Table 32-1. Summary of Interrupt Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
20h	20h	Master Initialization Command Word 1 (MICW1)—Offset 20h	11h
20h	20h	Master Operational Control Word 2 (MOCW2)—Offset 20h	0h
20h	20h	Master Operational Control Word 3 (MOCW3)—Offset 20h	8h
21h	21h	Master Initialization Command Word 2 (MICW2)—Offset 21h	0h
21h	21h	Master Initialization Command Word 3 (MICW3)—Offset 21h	7h
21h	21h	Master Initialization Command Word 4 (MICW4)—Offset 21h	0h
21h	21h	Master Operational Control Word 1 (MOCW1)—Offset 21h	0h
A0h	A0h	Slave Initialization Command Word 1 (SICW1)—Offset A0h	11h
A0h	A0h	Slave Operational Control Word 2 (SOCW2)—Offset A0h	0h
A0h	A0h	Slave Operational Control Word 3 (SOCW3)—Offset A0h	8h
A1h	A1h	Slave Initialization Command Word 2 (SICW2)—Offset A1h	0h
A1h	A1h	Slave Initialization Command Word 3 (SICW3)—Offset A1h	7h
A1h	A1h	Slave Initialization Command Word 4 (SICW4)—Offset A1h	0h
A1h	A1h	Slave Operational Control Word 1 (SOCW1)—Offset A1h	0h
4D0h	4D0h	Master Edge/Level Control (ELCR1)—Offset 4D0h	0h
4D1h	4D1h	Slave Edge/Level Control (ELCR2)—Offset 4D1h	0h

32.1.1 Master Initialization Command Word 1 (MICW1)—Offset 20h

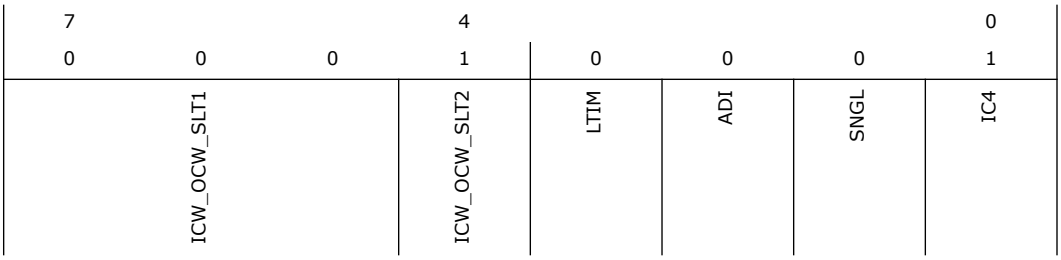
A write to Initialization Command Word 1 starts the interrupt controller initialization sequence, during which the following occurs:
1. The Interrupt Mask register is cleared.
2. IRQ7 input is assigned priority 7.
3. The slave mode address is set to 7.
4. Special Mask Mode is cleared and Status Read is set to IRR.
Once this write occurs, the controller expects writes to ICW2, ICW3, and ICW4 to complete the initialization sequence.

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 11h



Bit Range	Default & Access	Field Name (ID): Description
7:5	0h WO	**ICW/OCW select (ICW_OCW_SLT1):** These bits are MCS-85 specific, and not needed. Should be programmed to 000
4	1h WO	**ICW/OCW select (ICW_OCW_SLT2):** This bit must be a 1 to select ICW1 and enable the ICW2, ICW3, and ICW4 sequence.
3	0h WO	**Edge/Level Bank Select (LTIM):** Disabled. Replaced by the edge/level triggered control registers (ELCR).
2	0h WO	**ADI (ADI):** Ignored for PCH. Should be programmed to 0.
1	0h WO	**Single or Cascade (SNGL):** Must be programmed to a 0 to indicate two controllers operating in cascade mode.
0	1h WO	**ICW4 Write Required (IC4):** This bit must be programmed to a 1 to indicate that ICW4 needs to be programmed.

32.1.2 Master Operational Control Word 2 (MOCW2)—Offset 20h

*address should be 20h
Following a part reset or ICW initialization, the controller enters the fully nested mode of operation. Non-specific EOI without rotation is the default. Both rotation mode and specific EOI mode are disabled following initialization.

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:5	0h WO	**Rotate and EOI Codes (REOI):** R, SL, EOI - These three bits control the Rotate and End of Interrupt modes and combinations of the two. A chart of these combinations is listed above under the bit definition. 000 Rotate in Auto EOI Mode (Clear) 001 Non-specific EOI command 010 No Operation 011 *Specific EOI Command 100 Rotate in Auto EOI Mode (Set) 101 Rotate on Non-Specific EOI Command 110 *Set Priority Command 111 *Rotate on Specific EOI Command *L0 - L2 Are Used
4:3	0h WO	**OCW2 Select (O2S):** When selecting OCW2, bits 4:3 = 00
2:0	0h WO	**Interrupt Level Select (L2, L1, L0) (ILSLT):** L2, L1, and L0 determine the interrupt level acted upon when the SL bit is active. A simple binary code, outlined above, selects the channel for the command to act upon. When the SL bit is inactive, these bits do not have a defined function, programming L2, L1 and L0 to 0 is sufficient in this case.

32.1.3 Master Operational Control Word 3 (MOCW3)—Offset 20h

*address should be 20h

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 8h

7			4				0
0	0	0	0	1	0	0	0
RSVD	SMM	ESMM	O3S		PMC	RRC	

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	Reserved.
6	0h WO	**Special Mask Mode (SMM):** If this bit is set, the Special Mask Mode can be used by an interrupt service routine to dynamically alter the system priority structure while the routine is executing, through selective enabling/ disabling of the other channel's mask bits. Bit 6, the ESMM bit, must be set for this bit to have any meaning.
5	0h WO	**Enable Special Mask Mode (ESMM):** .

Bit Range	Default & Access	Field Name (ID): Description
4:3	1h WO	**OCW3 Select (O3S):** When selecting OCW3, bits 4:3 = 01
2	0h WO	**Poll Mode Command (PMC):** When cleared, poll command is not issued. When set, the next I/O read to the interrupt controller is treated as an interrupt acknowledge cycle. An encoded byte is driven onto the data bus, representing the highest priority level requesting service.
1:0	0h WO	**Register Read Command (RRC):** . To retain the current selection (read ISR or read IRR), always write a 0 to bit 1 when programming this register. The selected register can be read repeatedly without reprogramming OCW3. To select a new status register, OCW3 must be reprogrammed prior to attempting the read. Value Command 00 No Action 01 No Action 10 Read IRQ Register 11 Read IS Register

32.1.4 Master Initialization Command Word 2 (MICW2)—Offset 21h

ICW2 is used to initialize the interrupt controller with the five most significant bits of the interrupt vector address. The value programmed for bits[7:3] is used by the CPU to define the base address in the interrupt vector table for the interrupt routines associated with each IRQ on the controller. Typical ISA ICW2 values are 08h for the master controller and 70h for the slave controller.

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

7				4							0
0	0	0	0	0	0	0	0				
IVBA								IRL			

Bit Range	Default & Access	Field Name (ID): Description
7:3	0h WO	**Interrupt Vector Base Address (IVBA):** Bits [7:3] define the base address in the interrupt vector table for the interrupt routines associated with each interrupt request level input.
2:0	0h WO	**Interrupt Request Level (IRL):** When writing ICW2, these bits should all be 0. During an interrupt acknowledge cycle, these bits are programmed by the interrupt controller with the interrupt to be serviced. This is combined with bits [7:3] to form the interrupt vector driven onto the data bus during the second INTA# cycle. The code is a three bit binary code: Code Master Interrupt Slave Interrupt 000 IRQ0 IRQ8 001 IRQ1 IRQ9 010 IRQ2 IRQ10 011 IRQ3 IRQ11 100 IRQ4 IRQ12 101 IRQ5 IRQ13 110 IRQ6 IRQ14 111 IRQ7 IRQ15

32.1.5 Master Initialization Command Word 3 (MICW3)—Offset 21h

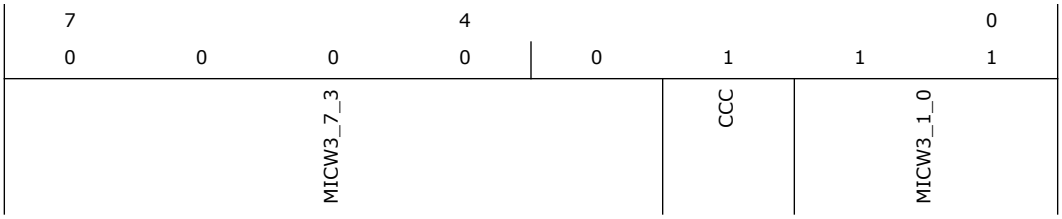
*address should be 21h

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 7h



Bit Range	Default & Access	Field Name (ID): Description
7:3	0h WO	**MICW3 [7:3] (MICW3_7_3):** These bits must be programmed to zero.
2	1h WO	**Cascaded Controller Connection (CCC):** This bit must always be programmed to a 1 to indicate the slave controller for interrupts 8 - 15 is cascaded on IRQ2.
1:0	3h WO	**MICW [1:0] (MICW3_1_0):** These bits must be programmed to zero.

32.1.6 Master Initialization Command Word 4 (MICW4)—Offset 21h

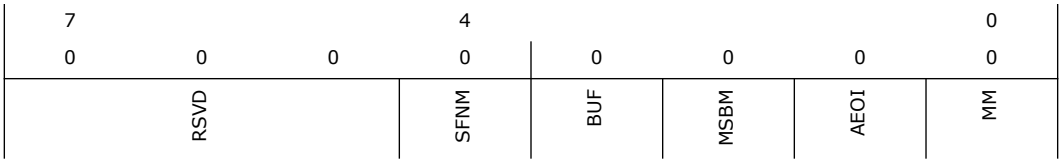
*address should be 21h

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7:5	0h RO	Reserved.
4	0h WO	**Special Fully Nested Mode (SFNM):** Should normally be disabled by writing a 0 to this bit. If SFNM=1, the special fully nested mode is programmed.
3	0h WO	**Buffered Mode (BUF):** Must be cleared for non-buffered mode. Writing 1 will result in undefined behavior.
2	0h WO	**Master/Slave in Buffered Mode (MSBM):** Not used. Should always be programmed to 0.
1	0h WO	**Automatic End of Interrupt (AEOI):** This bit should normally be programmed to 0. This is the normal end of interrupt. If this bit is 1, the automatic end of interrupt mode is programmed.
0	0h WO	**Microprocessor Mode (MM):** This bit must be written to 1 to indicate that the controller is operating in an Intel Architecture-based system. Writing 0 will result in undefined behavior.1

32.1.7 Master Operational Control Word 1 (MOCW1)—Offset 21h

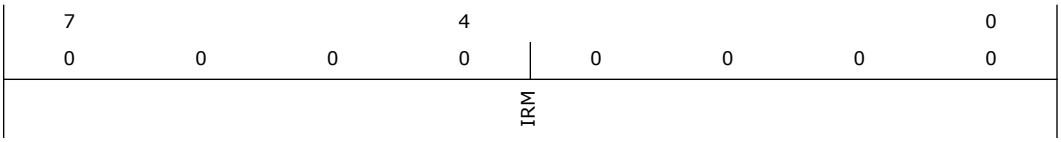
*address should be 21h

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**Interrupt Request Mask (IRM):** When a 1 is written to any bit in this register, the corresponding IRQ line is masked. When a 0 is written to any bit in this register, the corresponding IRQ mask bit is cleared, and interrupt requests will again be accepted by the controller. Masking IRQ2 on the master controller will also mask the interrupt requests from the slave controller.

32.1.8 Slave Initialization Command Word 1 (SICW1)—Offset A0h

A write to Initialization Command Word 1 starts the interrupt controller initialization sequence, during which the following occurs:
1. The Interrupt Mask register is cleared.
2. IRQ7 input is assigned priority 7.
3. The slave mode address is set to 7.
4. Special Mask Mode is cleared and Status Read is set to IRR.
Once this write occurs, the controller expects writes to ICW2, ICW3, and ICW4 to complete the initialization sequence.

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 11h

7			4				0
0	0	0	1	0	0	0	1
ICW_OCW_SLT1			ICW_OCW_SLT2	LTIM	ADI	SNGL	IC4

Bit Range	Default & Access	Field Name (ID): Description
7:5	0h WO	**ICW/OCW select (ICW_OCW_SLT1):** These bits are MCS-85 specific, and not needed. Should be programmed to 000
4	1h WO	**ICW/OCW select (ICW_OCW_SLT2):** This bit must be a 1 to select ICW1 and enable the ICW2, ICW3, and ICW4 sequence.
3	0h WO	**Edge/Level Bank Select (LTIM):** Disabled. Replaced by the edge/level triggered control registers (ELCR).
2	0h WO	**ADI (ADI):** Ignored for PCH. Should be programmed to 0.
1	0h WO	**Single or Cascade (SNGL):** Must be programmed to a 0 to indicate two controllers operating in cascade mode.
0	1h WO	**ICW4 Write Required (IC4):** This bit must be programmed to a 1 to indicate that ICW4 needs to be programmed.

32.1.9 Slave Operational Control Word 2 (SOCW2)—Offset A0h

*address should be A0h
Following a part reset or ICW initialization, the controller enters the fully nested mode of operation. Non-specific EOI without rotation is the default. Both rotation mode and specific EOI mode are disabled following initialization.

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

7			4				0
0	0	0	0	0	0	0	0
REOI			O2S		ILSLT		

Bit Range	Default & Access	Field Name (ID): Description
7:5	0h WO	**Rotate and EOI Codes (REOI):** R, SL, EOI - These three bits control the Rotate and End of Interrupt modes and combinations of the two. A chart of these combinations is listed above under the bit definition. 000 Rotate in Auto EOI Mode (Clear) 001 Non-specific EOI command 010 No Operation 011 *Specific EOI Command 100 Rotate in Auto EOI Mode (Set) 101 Rotate on Non-Specific EOI Command 110 *Set Priority Command 111 *Rotate on Specific EOI Command *L0 - L2 Are Used
4:3	0h WO	**OCW2 Select (O2S):** When selecting OCW2, bits 4:3 = 00
2:0	0h WO	**Interrupt Level Select (L2, L1, L0) (ILSLT):** L2, L1, and L0 determine the interrupt level acted upon when the SL bit is active. A simple binary code, outlined above, selects the channel for the command to act upon. When the SL bit is inactive, these bits do not have a defined function, programming L2, L1 and L0 to 0 is sufficient in this case.

32.1.10 Slave Operational Control Word 3 (SOCW3)—Offset A0h

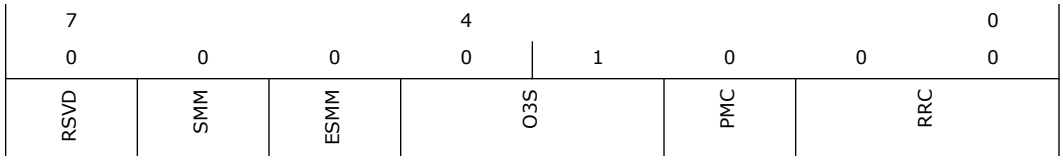
*address should be A0h

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 8h



Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	Reserved.
6	0h WO	**Special Mask Mode (SMM):** If this bit is set, the Special Mask Mode can be used by an interrupt service routine to dynamically alter the system priority structure while the routine is executing, through selective enabling/ disabling of the other channel's mask bits. Bit 6, the ESMM bit, must be set for this bit to have any meaning.
5	0h WO	**Enable Special Mask Mode (ESMM):** .

Bit Range	Default & Access	Field Name (ID): Description
4:3	1h WO	**OCW3 Select (O3S):** When selecting OCW3, bits 4:3 = 01
2	0h WO	**Poll Mode Command (PMC):** When cleared, poll command is not issued. When set, the next I/O read to the interrupt controller is treated as an interrupt acknowledge cycle. An encoded byte is driven onto the data bus, representing the highest priority level requesting service.
1:0	0h WO	**Register Read Command (RRC):** . To retain the current selection (read ISR or read IRR), always write a 0 to bit 1 when programming this register. The selected register can be read repeatedly without reprogramming OCW3. To select a new status register, OCW3 must be reprogrammed prior to attempting the read. Value Command 00 No Action 01 No Action 10 Read IRQ Register 11 Read IS Register

32.1.11 Slave Initialization Command Word 2 (SICW2)—Offset A1h

ICW2 is used to initialize the interrupt controller with the five most significant bits of the interrupt vector address. The value programmed for bits[7:3] is used by the CPU to define the base address in the interrupt vector table for the interrupt routines associated with each IRQ on the controller. Typical ISA ICW2 values are 08h for the master controller and 70h for the slave controller.

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

7			4				0
0	0	0	0	0	0	0	0
IVBA				IRL			

Bit Range	Default & Access	Field Name (ID): Description
7:3	0h WO	**Interrupt Vector Base Address (IVBA):** Bits [7:3] define the base address in the interrupt vector table for the interrupt routines associated with each interrupt request level input.
2:0	0h WO	**Interrupt Request Level (IRL):** When writing ICW2, these bits should all be 0. During an interrupt acknowledge cycle, these bits are programmed by the interrupt controller with the interrupt to be serviced. This is combined with bits [7:3] to form the interrupt vector driven onto the data bus during the second INTA# cycle. The code is a three bit binary code: Code Master Interrupt Slave Interrupt 000 IRQ0 IRQ8 001 IRQ1 IRQ9 010 IRQ2 IRQ10 011 IRQ3 IRQ11 100 IRQ4 IRQ12 101 IRQ5 IRQ13 110 IRQ6 IRQ14 111 IRQ7 IRQ15

32.1.12 Slave Initialization Command Word 3 (SICW3)—Offset A1h

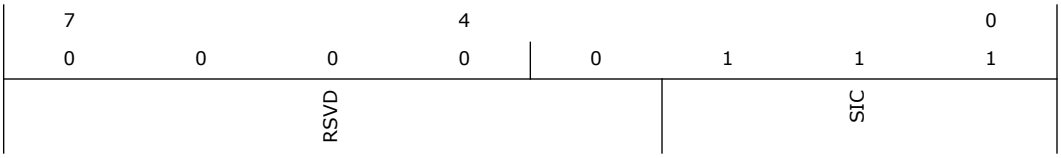
*address should be A1h

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 7h



Bit Range	Default & Access	Field Name (ID): Description
7:3	0h RO	Reserved.
2:0	7h WO	**Slave Identification Code (SIC):** This field must be programmed to 02h to match the code broadcast by the master controller during the INTA# sequence.

32.1.13 Slave Initialization Command Word 4 (SICW4)—Offset A1h

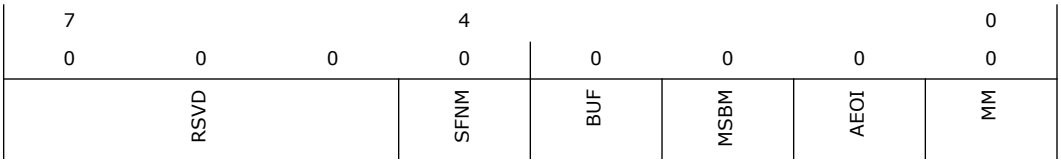
*address should be A1h

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7:5	0h RO	Reserved.
4	0h WO	**Special Fully Nested Mode (SFNM):** Should normally be disabled by writing a 0 to this bit. If SFNM=1, the special fully nested mode is programmed.
3	0h WO	**Buffered Mode (BUF):** Must be cleared for non-buffered mode. Writing 1 will result in undefined behavior.

Bit Range	Default & Access	Field Name (ID): Description
2	0h WO	**Master/Slave in Buffered Mode (MSBM):** Not used. Should always be programmed to 0.
1	0h WO	**Automatic End of Interrupt (AEOI):** This bit should normally be programmed to 0. This is the normal end of interrupt. If this bit is 1, the automatic end of interrupt mode is programmed.
0	0h WO	**Microprocessor Mode (MM):** This bit must be written to 1 to indicate that the controller is operating in an Intel Architecture-based system. Writing 0 will result in undefined behavior.1

32.1.14 Slave Operational Control Word 1 (SOCW1)—Offset A1h

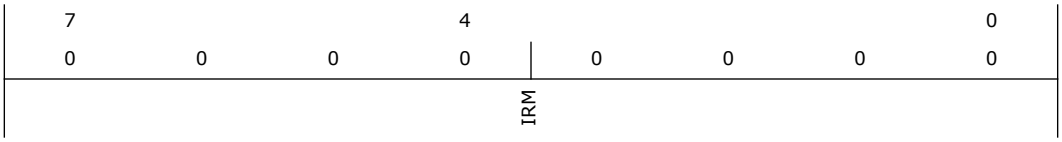
*address should be A1h

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**Interrupt Request Mask (IRM):** When a 1 is written to any bit in this register, the corresponding IRQ line is masked. When a 0 is written to any bit in this register, the corresponding IRQ mask bit is cleared, and interrupt requests will again be accepted by the controller. Masking IRQ2 on the master controller will also mask the interrupt requests from the slave controller.

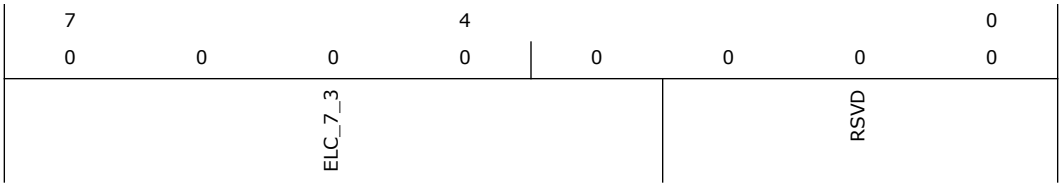
32.1.15 Master Edge/Level Control (ELCR1)—Offset 4D0h

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7:3	0h RW	**Edge Level Control (ELC_7_3):** In edge mode, (bit cleared), the interrupt is recognized by a low to high transition. In level mode (bit set), the interrupt is recognized by a high level.
2:0	0h RO	Reserved.

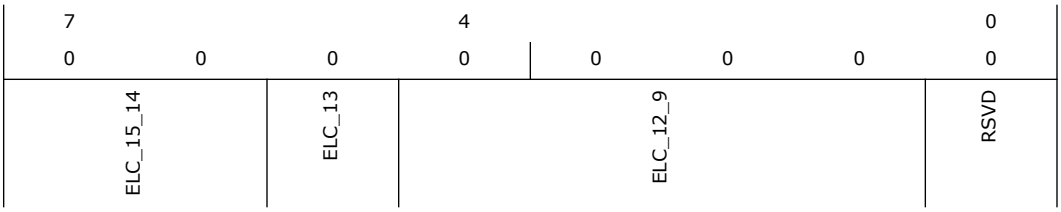
32.1.16 Slave Edge/Level Control (ELCR2)—Offset 4D1h

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RW	**Edge Level Control (ELC_15_14):** In edge mode, (bit cleared), the interrupt is recognized by a low to high transition. In level mode (bit set), the interrupt is recognized by a high level. Bit 7 applies to IRQ15, and bit 6 to IRQ14.
5	0h RW	**Edge Level Control (ELC_13):** In edge mode, (bit cleared), the interrupt is recognized by a low to high transition. In level mode (bit set), the interrupt is recognized by a high level. This bit applies to IRQ13.
4:1	0h RW	**Edge Level Control (ELC_12_9):** In edge mode, (bit cleared), the interrupt is recognized by a low to high transition. In level mode (bit set), the interrupt is recognized by a high level. Bit 4 applies to IRQ12, bit 3 to IRQ11, bit 2 to IRQ10, and bit 1 to IRQ9.
0	0h RO	Reserved.

32.2 Interrupt PCR Registers Summary

These registers are within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID + Register Offset).

Table 32-2. Summary of Interrupt PCR Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
3100h	3100h	PIRQA Routing Control (PARC)—Offset 3100h	80h
3101h	3101h	PIRQB Routing Control (PBRC)—Offset 3101h	80h
3102h	3102h	PIRQC Routing Control (PCRC)—Offset 3102h	80h

Table 32-2. Summary of Interrupt PCR Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
3103h	3103h	PIRQD Routing Control (PDRC)—Offset 3103h	80h
3104h	3104h	PIRQE Routing Control (PERC)—Offset 3104h	80h
3105h	3105h	PIRQF Routing Control (PFRC)—Offset 3105h	80h
3106h	3106h	PIRQG Routing Control (PGRC)—Offset 3106h	80h
3107h	3107h	PIRQH Routing Control (PHRC)—Offset 3107h	80h
31FCh	31FFh	General Interrupt Control (GIC)—Offset 31FCh	0h
3200h	3203h	Interrupt Polarity Control 0 (IPC0)—Offset 3200h	FF0000h
3204h	3207h	Interrupt Polarity Control 1 (IPC1)—Offset 3204h	0h
3208h	320Bh	Interrupt Polarity Control 2 (IPC2)—Offset 3208h	0h
320Ch	320Fh	Interrupt Polarity Control 3 (IPC3)—Offset 320Ch	0h
3300h	3303h	ITSS Power Reduction Control (ITSSPRC)—Offset 3300h	0h
3334h	3335h	Master Message Control (MMC)—Offset 3334h	0h

32.2.1 PIRQA Routing Control (PARC)—Offset 3100h

Access Method

Type: MSG Register
(Size: 8 bits)

Device:
Function:

Default: 80h

7			4				0
1	0	0	0	0	0	0	0
REN	RSVD			IR			

Bit Range	Default & Access	Field Name (ID): Description
7	1h RW	**Interrupt Routing Enable (REN):** When cleared, the corresponding PIRQ is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQ is not routed to the 8259.
6:4	0h RO	Reserved.
3:0	0h RW	**IRQ Routing (IR):** Bits Mapping: 1001: IRQ9 1010: IRQ10 0011: IRQ3 1011: IRQ11 0100: IRQ4 1100: IRQ12 0101: IRQ5 0110: IRQ6 1110: IRQ14 0111: IRQ7 1111: IRQ15 Others: Reserved

32.2.2 PIRQB Routing Control (PBRC)—Offset 3101h

Access Method

Type: MSG Register
(Size: 8 bits)

Device:
Function:

Default: 80h

7			4				0
1	0	0	0	0	0	0	0
REN	RSVD			IR			

Bit Range	Default & Access	Field Name (ID): Description
7	1h RW	**Interrupt Routing Enable (REN):** When cleared, the corresponding PIRQ is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQ is not routed to the 8259.
6:4	0h RO	Reserved.
3:0	0h RW	**IRQ Routing (IR):** Bits Mapping: 1001: IRQ9 1010: IRQ10 0011: IRQ3 1011: IRQ11 0100: IRQ4 1100: IRQ12 0101: IRQ5 0110: IRQ6 1110: IRQ14 0111: IRQ7 1111: IRQ15 Others: Reserved

32.2.3 PIRQC Routing Control (PCRC)—Offset 3102h

Access Method

Type: MSG Register
(Size: 8 bits)

Device:
Function:

Default: 80h

7			4				0
1	0	0	0	0	0	0	0
REN	RSVD			IR			

Bit Range	Default & Access	Field Name (ID): Description
7	1h RW	**Interrupt Routing Enable (REN):** When cleared, the corresponding PIRQ is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQ is not routed to the 8259.
6:4	0h RO	Reserved.
3:0	0h RW	**IRQ Routing (IR):** Bits Mapping: 1001: IRQ9 1010: IRQ10 0011: IRQ3 1011: IRQ11 0100: IRQ4 1100: IRQ12 0101: IRQ5 0110: IRQ6 1110: IRQ14 0111: IRQ7 1111: IRQ15 Others: Reserved

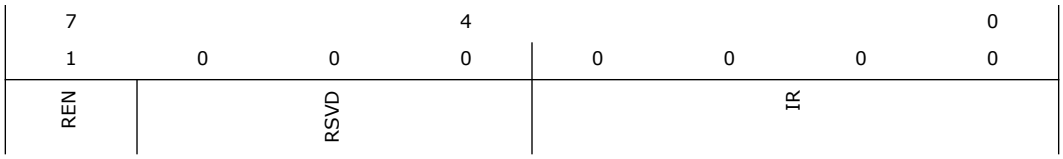
32.2.4 PIRQD Routing Control (PDRC)—Offset 3103h

Access Method

Type: MSG Register
(Size: 8 bits)

Device:
Function:

Default: 80h



Bit Range	Default & Access	Field Name (ID): Description
7	1h RW	**Interrupt Routing Enable (REN):** When cleared, the corresponding PIRQ is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQ is not routed to the 8259.
6:4	0h RO	Reserved.
3:0	0h RW	**IRQ Routing (IR):** Bits Mapping: 1001: IRQ9 1010: IRQ10 0011: IRQ3 1011: IRQ11 0100: IRQ4 1100: IRQ12 0101: IRQ5 0110: IRQ6 1110: IRQ14 0111: IRQ7 1111: IRQ15 Others: Reserved

32.2.5 PIRQE Routing Control (PERC)—Offset 3104h

Access Method

Type: MSG Register
(Size: 8 bits)

Device:
Function:

Default: 80h

7			4				0
1	0	0	0	0	0	0	0
REN	RSVD			IR			

Bit Range	Default & Access	Field Name (ID): Description
7	1h RW	**Interrupt Routing Enable (REN):** When cleared, the corresponding PIRQ is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQ is not routed to the 8259.
6:4	0h RO	Reserved.
3:0	0h RW	**IRQ Routing (IR):** Bits Mapping: 1001: IRQ9 1010: IRQ10 0011: IRQ3 1011: IRQ11 0100: IRQ4 1100: IRQ12 0101: IRQ5 0110: IRQ6 1110: IRQ14 0111: IRQ7 1111: IRQ15 Others: Reserved

32.2.6 PIRQF Routing Control (PFRC)—Offset 3105h

Access Method

Type: MSG Register
(Size: 8 bits)

Device:
Function:

Default: 80h

7			4				0
1	0	0	0	0	0	0	0
REN	RSVD			IR			

Bit Range	Default & Access	Field Name (ID): Description
7	1h RW	**Interrupt Routing Enable (REN):** When cleared, the corresponding PIRQ is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQ is not routed to the 8259.
6:4	0h RO	Reserved.
3:0	0h RW	**IRQ Routing (IR):** Bits Mapping: 1001: IRQ9 1010: IRQ10 0011: IRQ3 1011: IRQ11 0100: IRQ4 1100: IRQ12 0101: IRQ5 0110: IRQ6 1110: IRQ14 0111: IRQ7 1111: IRQ15 Others: Reserved

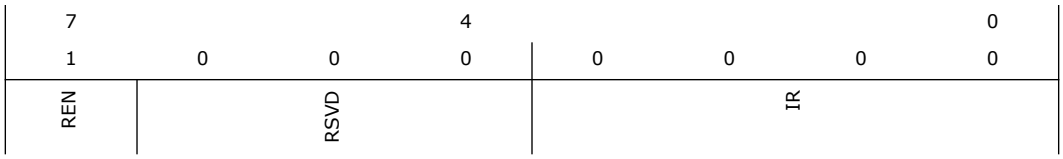
32.2.7 PIRQG Routing Control (PGRC)—Offset 3106h

Access Method

Type: MSG Register
(Size: 8 bits)

Device:
Function:

Default: 80h



Bit Range	Default & Access	Field Name (ID): Description
7	1h RW	**Interrupt Routing Enable (REN):** When cleared, the corresponding PIRQ is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQ is not routed to the 8259.
6:4	0h RO	Reserved.
3:0	0h RW	**IRQ Routing (IR):** Bits Mapping: 1001: IRQ9 1010: IRQ10 0011: IRQ3 1011: IRQ11 0100: IRQ4 1100: IRQ12 0101: IRQ5 0110: IRQ6 1110: IRQ14 0111: IRQ7 1111: IRQ15 Others: Reserved

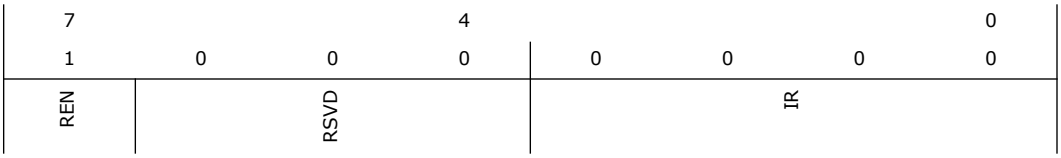
32.2.8 PIRQH Routing Control (PHRC)—Offset 3107h

Access Method

Type: MSG Register
(Size: 8 bits)

Device:
Function:

Default: 80h



Bit Range	Default & Access	Field Name (ID): Description
7	1h RW	**Interrupt Routing Enable (REN):** When cleared, the corresponding PIRQ is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQ is not routed to the 8259.
6:4	0h RO	Reserved.
3:0	0h RW	**IRQ Routing (IR):** Bits Mapping: 1001: IRQ9 1010: IRQ10 0011: IRQ3 1011: IRQ11 0100: IRQ4 1100: IRQ12 0101: IRQ5 0110: IRQ6 1110: IRQ14 0111: IRQ7 1111: IRQ15 Others: Reserved

32.2.9 General Interrupt Control (GIC)—Offset 31FCh

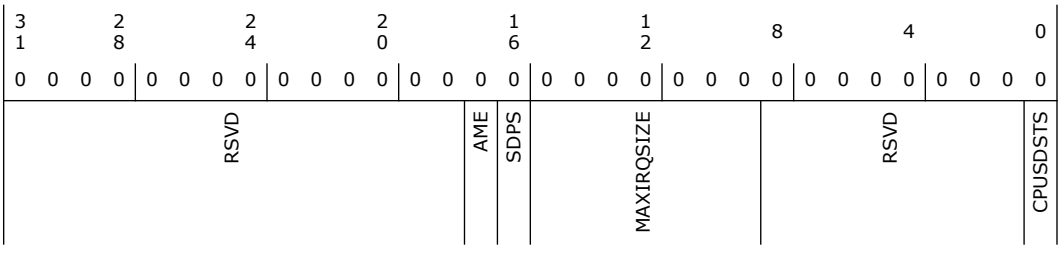
Note: FEC10000h - FEC3FFFFh is allocated to PCIe when Port I/OxApic Enable (PAE) bit is set.

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17	0h RW	**Alternate Access Mode Enable (AME):** When set, read only registers can be written, and write only registers can be read. See section 16.9 for details.
16	0h RW	**Shutdown Policy Select (SDPS):** When cleared (default) the PCH will update INIT# in response to the shutdown Vendor Defined Message (VDM). When set to 1, PCH will treat the shutdown VDM similar to receiving a CF9h I/O write, and will drive PLTRST# active. See Section 16.13 Reset Behavior for variations on whether power is cycled due to this reset source depending on the programming of other bits. BIOS guide note: This register is reset any time PLTRST# asserts.
15:9	0h RW	**MAX_IRQ_ENTRY_SIZE (MAXIRQSIZE):** This field indicates the size of the IOAPIC entry. The default size is 120 entries. 0000000: 120 entry size 0000001: 24 entry size (Legacy mode) 0000010 - 1111111: Reserved
8:1	0h RO	Reserved.
0	0h RO/P	**CPU Shutdown Status (CPUSDSTS):** This bit is set to 1 if the CPU sends the Shutdown Special cycle message. The Shutdown Message is recognized as an INIT# event if the Shutdown Policy Select = 0, else PCH shall treat the Shutodwn Special cycle as a request for CF9 Hard Reset. This is a sticky Read Only bit that is only reset by a loss of core power.

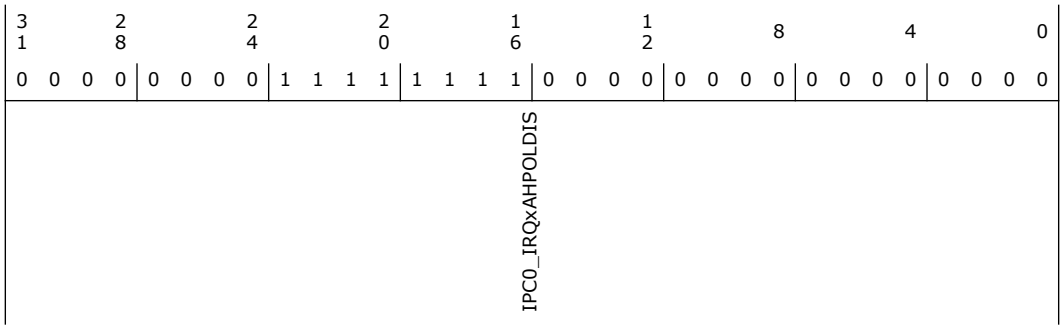
32.2.10 Interrupt Polarity Control 0 (IPC0)—Offset 3200h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: FF0000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	FF0000h RW	**IRQ 31-0 Active High Polarity Disable (IPC0_IRQxAHPOLDIS):** When set to 1, the interrupt polarity associated with IRQ31 down to IRQ0 is inverted to appear as Active Low to IOAPIC. When set to 0, the interrupt is appears as Active High to IOAPIC.

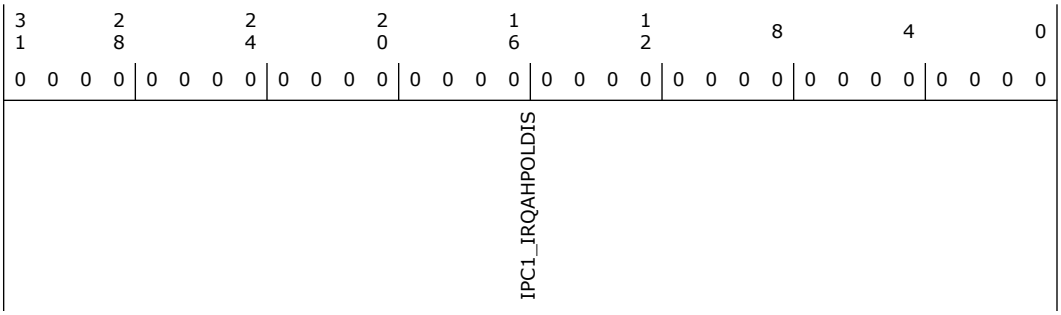
32.2.11 Interrupt Polarity Control 1 (IPC1)—Offset 3204h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**IRQ 63-32 Active High Polarity Disable (IPC1_IRQAHPOLDIS):** When set to 1, the interrupt polarity associated with IRQ63 down to IRQ32 is inverted to appear as Active Low to IOAPIC. When set to 0, the interrupt is appears as Active High to IOAPIC.

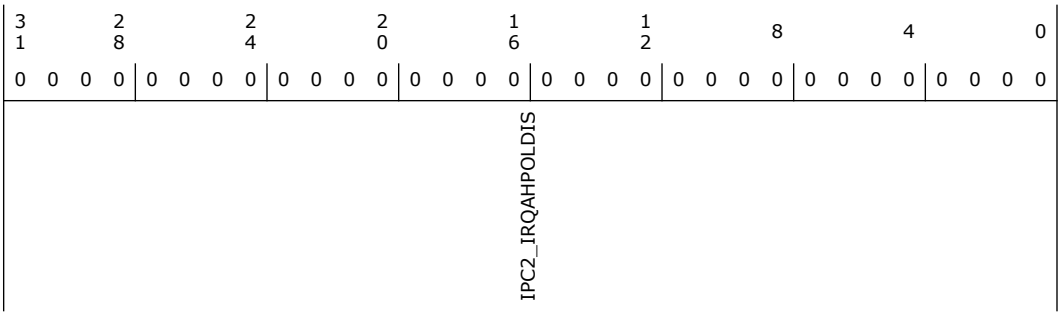
32.2.12 Interrupt Polarity Control 2 (IPC2)—Offset 3208h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**IRQ 95-64 Active High Polarity Disable (IPC2_IRQAHPOLDIS):** When set to 1, the interrupt polarity associated with IRQ95 down to IRQ64 is inverted to appear as Active Low to IOAPIC. When set to 0, the interrupt is appears as Active High to IOAPIC.

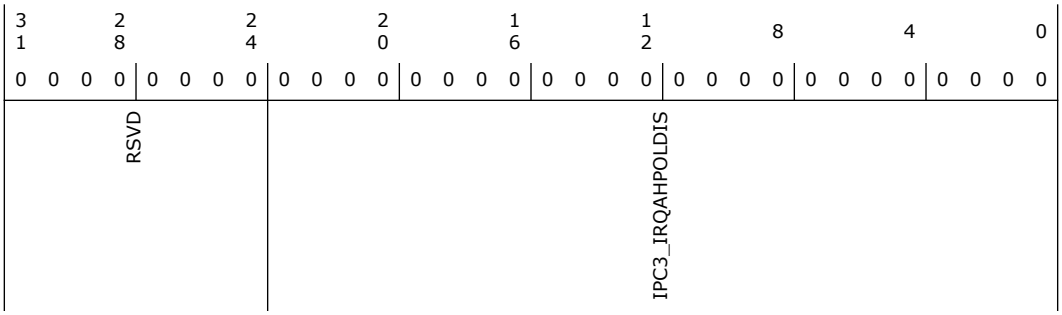
32.2.13 Interrupt Polarity Control 3 (IPC3)—Offset 320Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:0	0h RW	**IRQ 119-96 Active High Polarity Disable (IPC3_IRQAHPOLDIS):** When set to 1, the interrupt polarity associated with IRQ119 down to IRQ96 is inverted to appear as Active Low to IOAPIC. When set to 0, the interrupt is appears as Active High to IOAPIC.

32.2.14 ITSS Power Reduction Control (ITSSPRC)—Offset 3300h

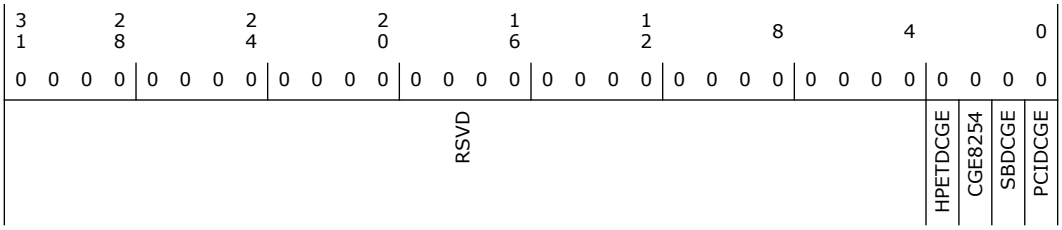
Power controls for the entire interrupt and timer subsystem.

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3	0h RW	**HPET Dynamic Clock Gating Enable (HPETDCGE):** When set, the HPET enables dynamic clock gating.
2	0h RW	**8254 Static Clock Gating Enable (CGE8254):** When set, the 8254 timer is disabled statically. This bit shall be set by BIOS if the 8254 feature is not needed in the system or before BIOS hands off the system that supports C11. Normal operation of 8254 requires this bit to 0.
1	0h RW	**Sideband Dynamic Clock Gating Enable (SBDCGE):** Setting this bit will enable all dynamic clock gating of the Sideband Clock domain.
0	0h RW	**PCI Dynamic Clock Gating Enable (PCIDCGE):** Setting this bit will enable dynamic clock gating for the Interrupt and Timer Sub System Core Logic.

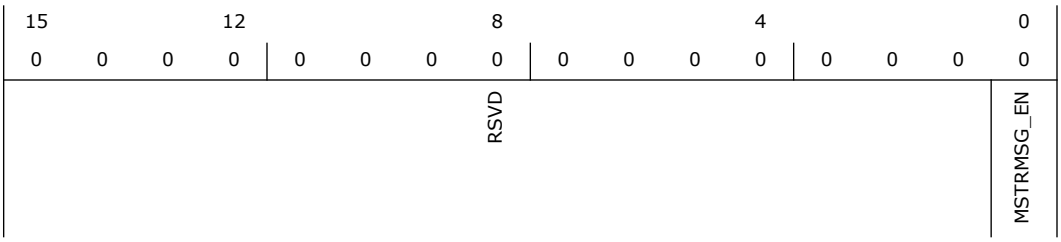
32.2.15 Master Message Control (MMC)—Offset 3334h

Access Method

Type: MSG Register
(Size: 16 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:1	0h RO	Reserved.
0	0h RW/V	**Master Message Enable (MSTRMSG_EN):** When set, allows Interrupt and Timer Subsystem (ITSS) to release any pending/in progress IOAPIC memory write, HPET memory write, virtual wire event or error messages to the IO frabic. When cleared, ITSS prevents these messages from being issued to the IO frabic.

§ §

33 Real Time Clock (RTC)

33.1 Registers Summary

The RTC contains two sets of indexed registers that are accessed using the two separate Index and Target registers (70h/71h or 72h/73h), as shown in the following table:

RTC (Standard) RAM Bank
Index Name
00h Seconds
01h Seconds Alarm
02h Minutes
03h Minutes Alarm
04h Hours
05h Hours Alarm
06h Day of Week
07h Day of Month
08h Month
09h Year
0Ah Register A
0Bh Register B
0Ch Register D
0Dh Register D
0Bh-7Fh 114 Bytes of User RAM

Table 33-1. Summary of Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	0h	Seconds (Sec)—Offset 0h	0h
1h	1h	Seconds Alarm (Sec_Alarm)—Offset 1h	0h
2h	2h	Minutes (Minutes)—Offset 2h	0h
3h	3h	Minutes Alarm (Minutes_Alarm)—Offset 3h	0h
4h	4h	Hours (Hours)—Offset 4h	0h
5h	5h	Hours Alarm (Hours_Alarm)—Offset 5h	0h
6h	6h	Day of Week (Day_of_Week)—Offset 6h	0h
7h	7h	Day of Month (Day_of_Month)—Offset 7h	0h
8h	8h	Month (Month)—Offset 8h	0h
9h	9h	Year (Year)—Offset 9h	0h
Ah	Ah	Register A (RTC_REGA)—Offset Ah	Undefined

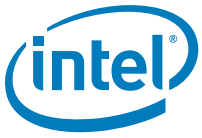


Table 33-1. Summary of Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
Bh	Bh	Register B - General Configuration (Register_B)—Offset Bh	X0X00XXXb (X = undefined)
Ch	Ch	Register C - Flag Register (Register_C)—Offset Ch	00X00000b (X = undefined)
Dh	Dh	Register D - Flag Register (Register_D)—Offset Dh	10XXXXXXb (X = Undefined)

33.1.1 Seconds (Sec)—Offset 0h

Seconds

33.1.2 Seconds Alarm (Sec_Alarm)—Offset 1h

Seconds Alarm

33.1.3 Minutes (Minutes)—Offset 2h

Minutes

33.1.4 Minutes Alarm (Minutes_Alarm)—Offset 3h

Minutes Alarm

33.1.5 Hours (Hours)—Offset 4h

Hours

33.1.6 Hours Alarm (Hours_Alarm)—Offset 5h

Hours Alarm

33.1.7 Day of Week (Day_of_Week)—Offset 6h

Day of Week

33.1.8 Day of Month (Day_of_Month)—Offset 7h

Day of Month

33.1.9 Month (Month)—Offset 8h

Month

33.1.10 Year (Year)—Offset 9h

Year

33.1.11 Register A (RTC_REGA)—Offset Ah

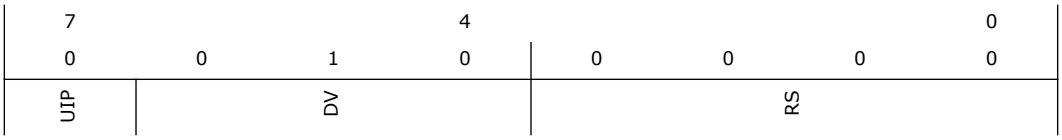
This register is used for general configuration of the RTC functions. None of the bits are affected by RSMRST# or any other reset signal.

Access Method

Type: Register
(Size: 8 bits)

Device:
Function:

Default: Undefined



Bit Range	Default & Access	Field Name (ID): Description
7	-- RW	**UPDATE IN PROGRESS (UIP):** This bit may be monitored as a status flag. 0 = Update cycle will not start for at least 488 micro-seconds. The time, calendar, and alarm information in RAM is always available when the UIP bit is 0. 1 = The update is soon to occur or is in progress.
6:4	-- RW	**Division Chain Select (DV):** These three bits control the divider chain for the oscillator, and are not affected by RSMRST# or any other reset signal.DV2 corresponds to bit 6. DV2 DV1 DV0 Function 0 1 0 Normal Operation 1 1 X Divider Reset 1 0 1 Bypass 15 stages (test mode only) 1 0 0 Bypass 10 stages (test mode only) 0 1 1 Bypass 5 stages (test mode only) 0 0 1 Invalid 0 0 0 Invalid
3:0	-- RW	**Rate Select (RS):** Selects one of 13 taps of the 15 stage divider chain. The selected tap can generate a periodic interrupt if the PIE bit is set in Register B. Otherwise this tap will set the PF flag of Register C. If the periodic interrupt is not to be used, these bits should all be set to zero. RS3 corresponds to bit 3. RS3[4p] RS2 RS1 RS0 Periodic Rate 0 0 0 0 Interrupt never toggles 0 0 0 1 3.90625 ms 0 0 1 0 7.8125 ms 0 0 1 1 122.070 s 0 1 0 0 244.141 s 0 1 0 1 488.281 s 0 1 1 0 976.5625s 0 1 1 1 1.953125 ms 1 0 0 0 3.90625 ms 1 0 0 1 7.8125 ms 1 0 1 0 15.625 ms 1 0 1 1 31.25 ms 1 1 0 0 62.5 ms 1 1 0 1 125 ms 1 1 1 0 250 ms 1 1 1 1 500 ms

33.1.12 Register B - General Configuration (Register_B)—Offset Bh

Access Method

Type: Register
(Size: 8 bits)

Device:
Function:

Default: x0x00xxx (x: undefined)

7			4				0
0	0	0	0	0	0	0	0
SET	PIE	AIE	UIE	SQWE	DM	HOURFORM	DSE

Bit Range	Default & Access	Field Name (ID): Description
7	-- RW	**Update Cycle Inhibit (SET):** Enables/Inhibits the update cycles. 0 = Update cycle occurs normally once each second. 1 = A current update cycle will abort and subsequent update cycles will not occur until SET is returned to zero. When set is one, the BIOS may initialize time and calendar bytes safely. This bit is not affected by RSMRST# nor any other reset signal. Note: Software must ensure this bit is at least transitioned from '1' to '0' once whenever the RTC coin battery is inserted. This is to ensure that the internal RTC time updates occur properly.
6	0h RW	**Periodic Interrupt Enable (PIE):** 0 = Disabled. 1 = Enabled. Allows an interrupt to occur with a time base set with the RS bits of register A. This bit is cleared by RSMRST# assertion, but not on any other reset.
5	-- RW	**Alarm Interrupt Enable (AIE):** 0 = Disabled. 1 = Enabled. Allows an interrupt to occur when the AF is set from an alarm match from the update cycle. An alarm can occur once a second, one an hour, once a day, or once a month. This bit is cleared by RTCRST# assertion, but not on any other reset.
4	0h RW	**Update-ended Interrupt Enable: (UIE):** 0 = Disabled. 1 = Enabled. Allows an interrupt to occur when the update cycle ends. This bit is cleared by RSMRST# assertion, but not on any other reset.
3	0h RW	**Square Wave Enable (SQWE):** The Square Wave Enable bit serves no function in this device, yet is left in this register bank to provide compatibility with the Motorola 146818B. There is not SQW pin on this device. This bit is cleared by RSMRST# assertion, but not on any other reset.
2	-- RW	**Data Mode (DM):** This bit specifies either binary or BCD data representation. 0 = BCD. 1 = Binary. This bit is not affected by RSMRST# nor any other reset signal.
1	-- RW	**Hour Format (HOURFORM):** This bit indicates the hour byte format. 0 = Twelve-hour mode is selected.In twelve hour mode, the seventh bit represents AM as zero and PM as one. 1 = Twenty-four hour mode is selected. This bit is not affected by RSMRST# nor any other reset signal.
0	-- RW	**Daylight Savings Enable (DSE):** The Daylight Savings Enable bit triggers two special hour updates per year when set to one. One is on the first Sunday in April, where time increments from 1:59:59 AM to 3:00:00 AM. The other is the last Sunday in October when the time first reaches 1:59:59 AM, it is changed to 1:00:00 AM. The time mustincrement normally for at least two update cycles (seconds) previous to these conditions for the time change to occur properly. These special update conditions do not occur when the DSE bit is set to zero. The days for the hour adjustment are those specified in United States federal law as of 1987, which is different than previous years. If BUC.DSO bit is set, the DSE bit continues to be a R/W bit, but Daylight Saving is disabled regardless of the DSE bit. This bit is not affected by RSMRST# nor any other reset signal.

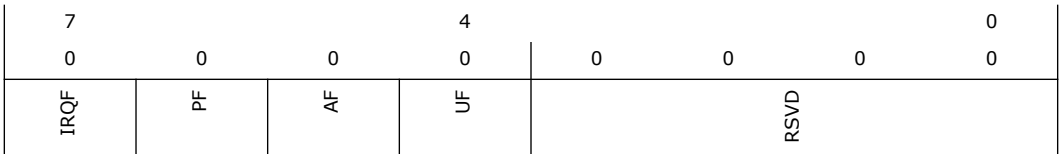
33.1.13 Register C - Flag Register (Register_C)—Offset Ch

Access Method

Type: Register
(Size: 8 bits)

Device:
Function:

Default: 00x00000 (x: undefined)



Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Interrupt Request Flag (IRQF):** Interrupt Request Flag = (PF * PIE) + (AF * AIE) + (UF * UFE). This also causes the RTC Interrupt to be asserted. This bit is cleared upon RSMRST# assertion or a read of Register C.
6	0h RO	**Periodic Interrupt Flag (PF):** Periodic interrupt Flag will be one when the tap as specified by the RS bits of register A is one. If no taps are specified, this flag bit will remain at zero. This bit is cleared upon RSMRST# assertion or a read of Register C.
5	-- RO	**Alarm Flag (AF):** Alarm Flag will be high after all Alarm values match the current time. This bit is cleared upon RTCRST# assertion or a read of Register C.
4	0h RO	**Update-ended Flag (UF):** Updated-ended flag will be high immediately following an update cycle for each second. The bit is cleared upon RSMRST# assertion or a read of Register C.
3:0	0h RO	Reserved.

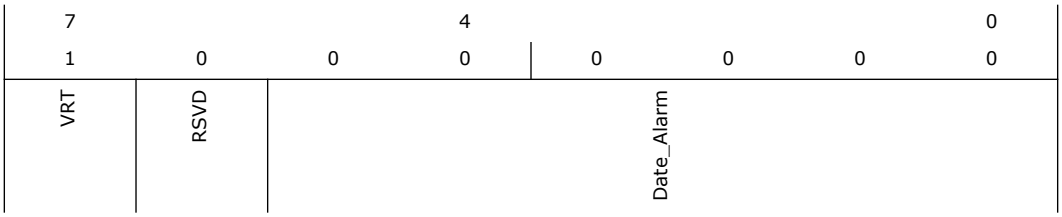
33.1.14 Register D - Flag Register (Register_D)—Offset Dh

Access Method

Type: Register
(Size: 8 bits)

Device:
Function:

Default: 10xxxxxx (x: undefined)



Bit Range	Default & Access	Field Name (ID): Description
7	1h RW	**Valid RAM and Time Bit (VRT):** This bit is hard-wired to 1 in the RTC power well. This bit should always be written as a 0 for write cycle, however it will return a 1 for read cycles.
6	0h RO	Reserved.
5:0	-- RW	**Date Alarm (Date_Alarm):** These bits store the date of month alarm value. If set to 000000, then a dont care state is assumed. The host must configure the dates alarm for these bits to do anything, yet they can be written at any time. If the date alarm is not enabled, these bits will return zeros to mimic the functionality of the Motorola 146818B. These bits are not affected by any reset assertion.

33.2 RTC PCR Registers Summary

These registers are within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID + Register Offset).

Table 33-2. Summary of RTC PCR Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
3400h	3403h	RTC Configuration (RC)—Offset 3400h	0h
3414h	3414h	Backed Up Control (BUC)—Offset 3414h	0h
3F04h	3F07h	RTC Update In Progress SMI Control (UIPSMI)—Offset 3F04h	0h

33.2.1 RTC Configuration (RC)—Offset 3400h

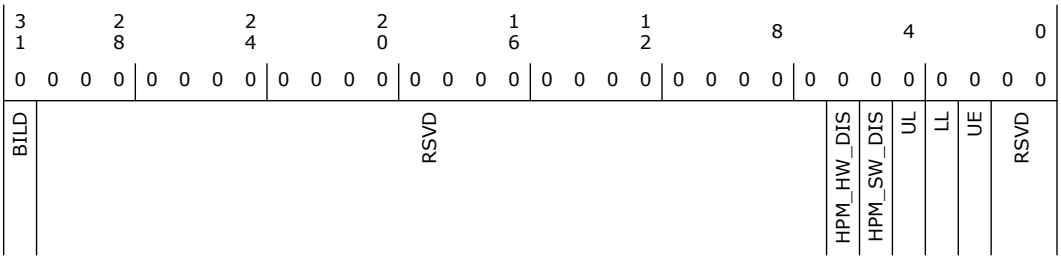
All bits in this register are in the Primary Well and cleared by PLTRST# assertion.

Access Method

Type: Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RWLO	**Bios Interface Lock-Down (BILD):** When set, prevents RTC version of TS (BUC.TS) from being changed. This bit can only be written from 0 to 1 once. This BILD bit has a different function compared to LPC, SPI and eSPI version but BIOS should set all the corresponding bits after reset in order to lock down the BIOS interface correctly.
30:7	0h RO	Reserved.
6	0h RW	**RTC High Power Mode HW Disable (HPM_HW_DIS):** 0 = HW control of the RTC internal VRM is disabled. 1 = The internal VRM that generates the rtc well supply voltage in SUS mode is disabled when SLP_S0# is asserted.
5	0h RW	**RTC High Power Mode SW Disable (HPM_SW_DIS):** 0 = The internal VRM powers the rtc well when RSMRST# is '1'. (default) 1 = The internal VRM that generates the rtc well supply voltage in SUS mode is disabled.
4	0h RWLO	**Upper 128 Byte Lock (UL):** When set, bytes 38h-3Fh in the upper 128 byte bank of RTC RAM are locked and cannot be accessed. Writes will be dropped and reads will not return any guaranteed data. Bit reset on system reset.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RWLO	**Lower 128 Byte Lock (LL):** When set, bytes 38h-3Fh in the lower 128 byte bank of RTC RAM are locked and cannot be accessed. Writes will be dropped and reads will not return any guaranteed data. Bit reset on system reset.
2	0h RW	**Upper 128 Byte Enable (UE):** When set, the upper 128 byte bank of RTC RAM can be accessed.
1:0	0h RO	Reserved.

33.2.2 Backed Up Control (BUC)—Offset 3414h

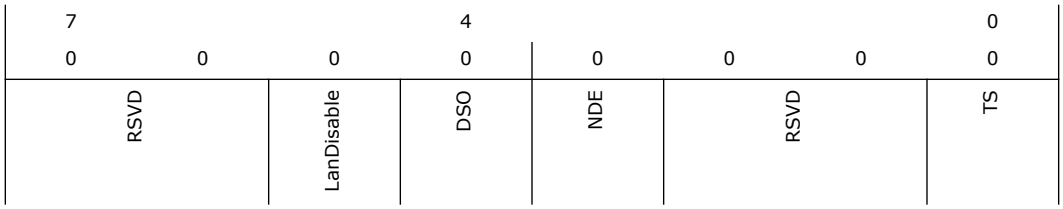
All bits in this register are in the RTC well and only cleared by RTCRST# assertion.

Access Method

Type: Register
(Size: 8 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	Reserved.
5	0h RW/RO/F/L	**LAN Disable (LanDisable):** 0 = LAN is Enabled 1 = LAN is Disabled. This register is reset to 0 on RTCRST# assertion. If the Function Disable SUS Well Lockdown register is set, this bit can not be changed by software.
4	0h RW	**Daylight Savings Override (DSO):** 0 = The DSE bit in the RTC register B bit(0) is a RW bit that is configurable by software to enable the daylight savings. 1 = The DSE bit in the RTC Register B bit(0) is a RW bit but has no effect, daylight savings is hard-disabled internally. System BIOS shall configure this bit accordingly during the boot process before RTC time is initialized.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**NetDetect Enable (NDE):** If this bit is '1' and the South MLink Enable bit is '0' (ME PM RTCPMCFG.SMLEN), then the GPIO(14) input signal is muxed onto the South MLink MLCLK pin as a NetDetect Request signal to the wireless LAN component. If the South MLink Enable bit is a '1', then the South MLink MLCLK pin is used as MLCLK, independent of the value of this register. If both the South MLink Enable bit is '0' and this NetDetect Enable bit is '0', then the South MLink MLCLK pin is tri-stated. This register is in the RTC well instead of the SUS well to maintain state if the SUS well power is removed in S4.
2:1	0h RO	Reserved.
0	0h RW	**Top Swap (TS):** 0 = PCH will not invert A16, A17 or A18. 1 = PCH will invert A16, A17 or A18 for cycles going to the BIOS space. If booting from SPI LPC (FWH), then the boot-block size is 64 KB and A16 is inverted if Top Swap is enabled. If booting from SPI, then the Top Swap Block size soft strap determines if A16, A17 or A18 shoudl be inverted if Top Swap is enabled. If PCH is strapped for Top Swap (GPP_B14/SPKR is high at rising edge of PCH_PWROK), then this bit cannot be cleared by software. The strap jumper should be removed and the system rebooted.

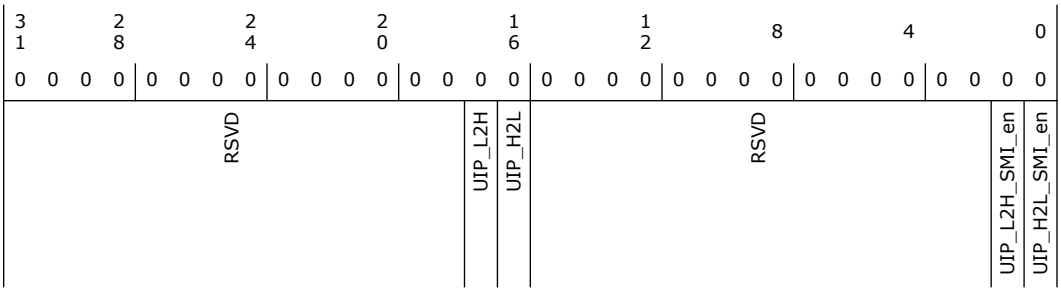
33.2.3 RTC Update In Progress SMI Control (UIPSMI)—Offset 3F04h

Access Method

Type: Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17	0h RWC	**RTC UIP Low-to-High (UIP_L2H):** This sticky status bit is set whenever the RTC Update-In-Progress signal transitions from low to high (i.e., at the start of an update).
16	0h RWC	**RTC UIP High-to-Low (UIP_H2L):** This sticky status bit is set whenever the RTC Update-In-Progress signal transitions from high to low (i.e., at the start of an update).

Bit Range	Default & Access	Field Name (ID): Description
15:2	0h RO	Reserved.
1	0h RWC	**RTC UIP Low-to-High SMI Enable (UIP_L2H_SMI_en):** When this bit is set, a '1' in bit 17 will assert the internal SMI signal to the Power Management SMI logic.
0	0h RWC	**RTC UIP High-to-Low SMI Enable (UIP_H2L_SMI_en):** When this bit is set, a '1' in bit 16 will assert the internal SMI signal to the Power Management SMI logic.

§ §

34 System Management TCO

34.1 SMBus TCO I/O Registers Summary

The TCO I/O registers reside in a 32-byte range that starts from the IO Base Address described in the TCOBAR register in the SMBus PCI Configuration space.

Table 34-1. Summary of SMBus TCO I/O Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	1h	TCO_RLD Register (TRLD)—Offset 0h	4h
2h	2h	TCO_DAT_IN Register (TDI)—Offset 2h	0h
3h	3h	TCO_DAT_OUT Register (TDO)—Offset 3h	0h
4h	5h	TCO1_STS Register (TSTS1)—Offset 4h	0h
6h	7h	TCO2_STS Register (TSTS2)—Offset 6h	0h
8h	9h	TCO1_CNT Register (TCTL1)—Offset 8h	0h
Ah	Bh	TCO2_CNT Register (TCTL2)—Offset Ah	8h
Ch	Dh	TCO_MESSAGE1 and TCO_MESSAGE2 (TMSG)—Offset Ch	0h
Eh	Eh	TCO_WDSTATUS Register (TWDS)—Offset Eh	0h
10h	10h	LEGACY_ELIM Register (LE)—Offset 10h	3h
12h	13h	TCO_TMR Register (TTMR)—Offset 12h	4h

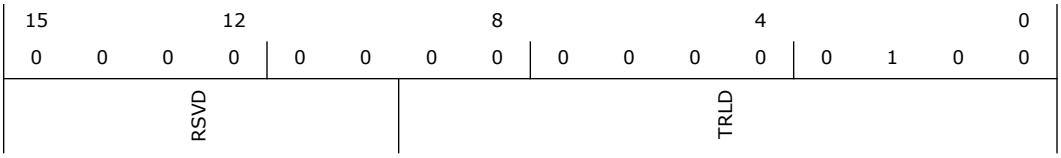
34.1.1 TCO_RLD Register (TRLD)—Offset 0h

Access Method

Type: IO Register
(Size: 16 bits)

Device: 31
Function: 4

Default: 4h



Bit Range	Default & Access	Field Name (ID): Description
15:10	0h RO	Reserved.
9:0	4h RW	**TCORLD (TRLD):** Reading this register will return the current count of the TCO timer. Writing any value to this register will reload the timer to prevent the timeout.

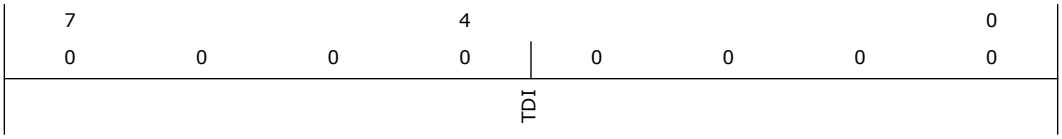
34.1.2 TCO_DAT_IN Register (TDI)—Offset 2h

Access Method

Type: IO Register
(Size: 8 bits)

Device: 31
Function: 4

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**TCO_DAT_IN (TDI):** Data Register for passing commands from the OS to the SMI handler. Writes to this register will cause an SMI and set the OS_TCO_SMI bit in the TCO_STS register.

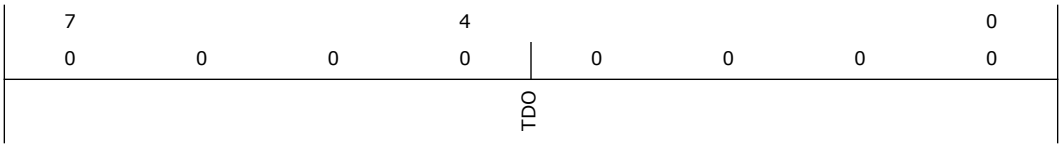
34.1.3 TCO_DAT_OUT Register (TDO)—Offset 3h

Access Method

Type: IO Register
(Size: 8 bits)

Device: 31
Function: 4

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**TCO_DAT_OUT (TDO):** Data Register for passing commands from the SMI handler to the OS. Writes to this register will set the TCO_INT_STS bit in the TCO_STS register. It also causes an interrupt, as selected by the TCO_IRQ_SEL bits.

34.1.4 TCO1_STS Register (TSTS1)—Offset 4h

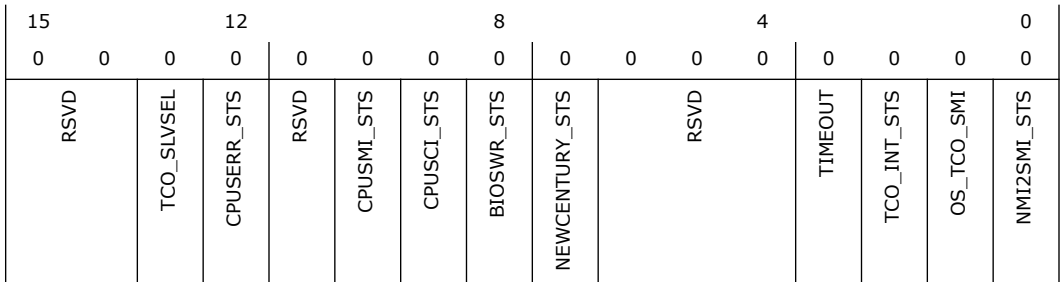
Unless otherwise indicated, these bits are sticky and are cleared by writing a 1 to the corresponding bit position.

Access Method

Type: IO Register
(Size: 16 bits)

Device: 31
Function: 4

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RO	Reserved.
13	0h RO/Strap	**TCO Slave Select (TCO_SLVSEL):** This register bit indicates the value of TCO Slave Select Soft Strap.
12	0h RW/1C	**CPUSERR_STS (CPUSERR_STS):** This bit is set to 1 if the CPU complex sends a DMI special cycle message indicating that it wants to cause an SERR#. The software must read the MCH to find out why it wanted the SERR#. Software must write a 1 back to this bit to clear it.
11	0h RO	Reserved.
10	0h RW/1C	**CPUSMI_STS (CPUSMI_STS):** This bit is set to 1 if the CPU complex sends a DMI special cycle message indicating that it wants to cause an SMI. The software must read the CPU to find out why it wanted the SMI. Software must write a 1 back to this bit to clear it.
9	0h RW/1C	**CPUSCI_STS:** This bit is set to 1 if the CPU complex sends a DMI special cycle message indicating that it wants to cause an SCI. The software must read the CPU to find out why it wanted the SCI. Software must write a 1 back to this bit to clear it.
8	0h RW/1C	**BIOSWR_STS:** Intel PCH sets this bit to 1 and generates an SMI# to indicate an illegal attempt to write to the BIOS located in the FWH that is accessed over the LPC. This occurs when either: a) The BIOSWP bit is changed from 0 to 1 and the LE bit is also set, or b) Any write is attempted to the BIOS and the BIOSWP bit is also set. This bit doesn't get set to 1 when: 1) a or b above occurs on eSPI controller. 2) a or b above occurs on SPI Flash controller. Note: On write cycles attempted to the 4MB lower alias to the BIOS space, the BIOSWR_STS bit will not be set.
7	0h RW/1C	**NEWCENTURY_STS (NEWCENTURY_STS):** This bit will be set when the year rolls over from 1999 to 2000. If the bit is already 1, it will remain 1. This bit can be cleared either by software writing a 1 back to the bit position, or by RTCRST# going active. When this bit is set, an SMI# will be generated. However, this will not be a wake event (i.e. if the system is in a sleeping state when the NEWCENTURY_STS bit is set, the system will not wake up). Note: This bit 7 is not valid when the RTC battery is first put in (or if the RTC battery does not provide sufficient power when the system is unplugged). Software can determine that the RTC well was not maintained by checking the RTC_PWR_STS bit (GEN_PMCON_3 register in the Power Management Controller, D31:F2:A4, bit 2) or by other means (such as doing a checksum on the RTC RAM array). If the RTC well is determined to not have been maintained, the BIOS should set the time to a legal value and then clear the NEWCENTURY_STS bit. Note: This bit may take up to 3 RTCCLKs for the bit to be cleared when a 1 is written to the bit to clear it. After writing a 1 to the NEWCENTURY_STS bit, software should also not exit the SMI handler until after the bit has been cleared. This is to make sure the SMI is not re-entered. BIOS Assumption: When booting, the BIOS checks the NEWCENTURY_STS bit. If set, the BIOS should increment the value in the RTC RAM register associated with the century. The BIOS should then clear the NEWCENTURY_STS bit. This scenario would occur if the system was asleep when the century rolls over. If the system is in an S0 state (not sleeping) and the SMI# occurs with the NEWCENTURY_STS bit sets, the SMI handler should increment the value in the RTC RAM register and clear the NEWCENTURY_STS bit.
6:4	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW/1C	**TIMEOUT (TIMEOUT):** Bit set to 1 by Intel PCH to indicate that the SMI was caused by TCO timer reaching 0. Note: The SMI handler should clear this bit to prevent an immediate re-entry to the SMI handler.
2	0h RW/1C	**TCO_INT_STS (TCO_INT_STS):** Bit set to 1 when SMI handler caused the interrupt by writing to the TCO_DAT_OUT register.
1	0h RW/1C	**OS_TCO_SMI:** Bit set to 1 when OS code caused an SMI# by writing to the TCO_DAT_IN register.
0	0h RO/V	**NMI2SMI_STS:** The PCH sets this bit when an SMI# occurs because an event occurred that would otherwise have caused an NMI.

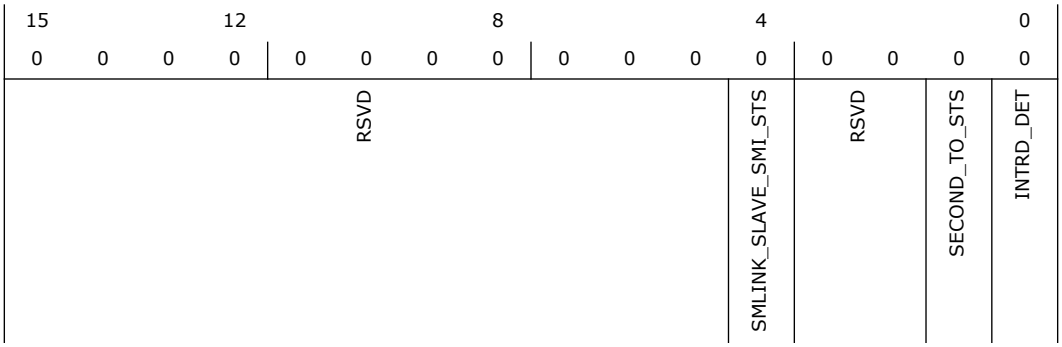
34.1.5 TCO2_STS Register (TSTS2)—Offset 6h

Access Method

Type: IO Register
(Size: 16 bits)

Device: 31
Function: 4

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:5	0h RO	Reserved.
4	0h RW/1C	**SMLINK_SLAVE_SMI_STS:** The PCH will set this bit to 1 when it receives the SMI message (encoding 08h in the command type) on the SMLinks Slave Interface. Software clears the bit by writing a 1 to this bit position. This bit is in the resume well. It is reset by RSMRST#, but not by the PCI Reset associated with exit from S3-S5 states. This allows the software (presumably BIOS) to get the interrupt, see this new bit set, and decidedly go into the pre-determined (by local policy) sleep state.

Bit Range	Default & Access	Field Name (ID): Description
3:2	0h RO	Reserved.
1	0h RW/1C	**SECOND_TO_STS:** Intel PCH sets this bit to 1 to indicate that the TIMEOUT bit had been (or is currently) set and a second timeout occurred before the TCO_RLD register was written. If this bit is set and the NO_REBOOT config bit is 0, then the Intel PCH will reboot the system after the second timeout. The reboot is done by asserting PLTRST#. This bit is only cleared by writing a 1 to this bit or by a RSMRST#.
0	0h RW/1C	**INTRD_DET (INTRD_DET):** The bit is set to 1 by the PCH to indicate that an intrusion was detected. This bit is cleared by writing a 1 to this bit or by RTCRST#. Note: This bit has a recovery time. After writing a 1 to this bit position (to clear it), the bit may be read back as a 1 for up 65 microseconds before it is read as a 0. Software must be aware of this recovery time when reading this bit after clearing it. Note: If the INTRUDER# signal is active when the software attempts to clear the INTRD_DET bit, the bit will remain as a 1, and the SMI# will be generated again immediately. The SMI handler can clear the INTRD_SEL bits to avoid further SMIs. However, if the INTRUDER# signals goes inactive and then active again, there will not be further SMIs. If the INTRUDER# signal goes inactive some point after the INTRD_DET bit is written as a 1, then the INTRD_DET signal will go to a 0 when INTRUDER# input signal goes inactive. Note that this is slightly different than a classic sticky bit, since most sticky bits would remain active indefinitely when the signal goes active and would immediately go inactive when a 1 is written to the bit.

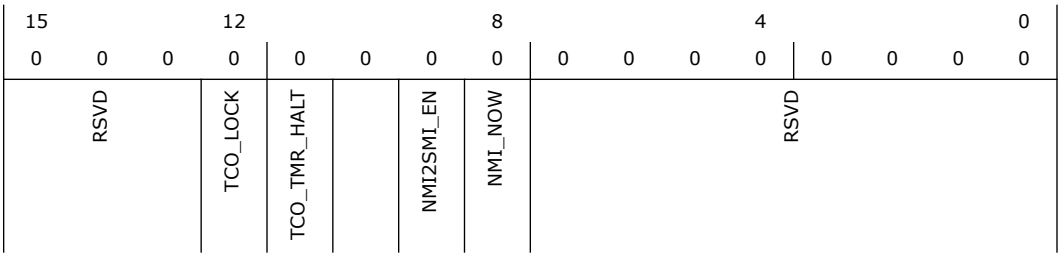
34.1.6 TCO1_CNT Register (TCTL1)—Offset 8h

Access Method

Type: IO Register
(Size: 16 bits)

Device: 31
Function: 4

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO	Reserved.
12	0h RW	**TCO_LOCK:** When set to 1, this bit prevents writes from changing the TCO_EN bit (in offset 30h of Power Management I/O space). Once this bit is set to 1, it can not be cleared by software writing a 0 to this bit location. A core-well reset is required to change this bit from 1 to 0. This bit defaults to 0.
11	0h RW	**TCO_TMR_HALT:** 1 = The TCO timer will halt. It will not count, and thus cannot reach a value that would cause an SMI# or to cause the SECOND_TO_STS bit to be set. This will also prevent rebooting. 0 = The TCO timer is enabled to count. This is the default.
10	0h RW	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**NMI2SMI_EN:** Setting this bit 1 forces all NMIs to instead cause an SMI#, and will be reported in the TCO1_STS register. NMI2SMI_EN bit is set AND the NMI_EN# bit is set to 0, the NMI# will be routed to cause an SMI#. No NMI will be caused. However, if the GBL_SMI_EN bit is not set, then no SMI# will be generated, either. If NMI2SMI_EN is set but the NMI_EN# bit is set to 1, then no NMI or SMI# will be generated. The following table shows the possible combinations: NMI_EN#, GBL_SMI_EN 00: No SMI# based on NMI events (since no SMI# at all because SMI_EN = 0) 01: SMI# will be caused based on NMI events 10: No SMI# at all because SMI_EN is 0 11: No SMI# based on NMI events because NMI_EN#=1
8	0h RW	**NMI_NOW:** Writing a 1 to this bit causes an NMI. This allows the BIOS or SMI handler to force entry to the NMI handler. The NMI handler is expected to clear this bit. Another NMI will not be generated until the bit is cleared by writing a 1 back to the same bit position.
7:0	0h RO	Reserved.

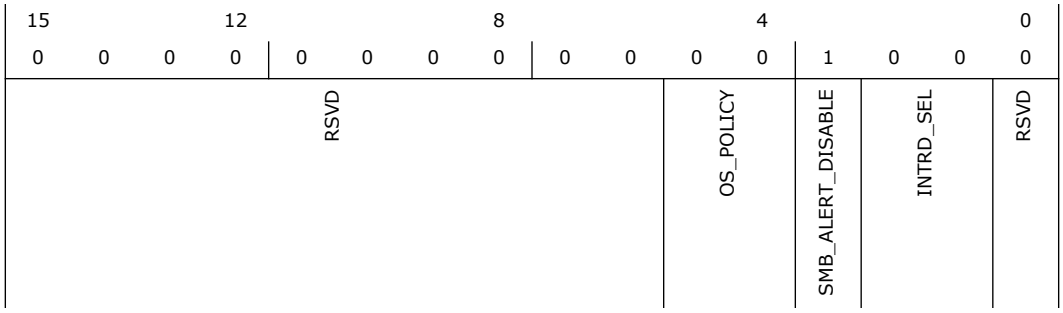
34.1.7 TCO2_CNT Register (TCTL2)—Offset Ah

Access Method

Type: IO Register
(Size: 16 bits)

Device: 31
Function: 4

Default: 8h



Bit Range	Default & Access	Field Name (ID): Description
15:6	0h RO	Reserved.
5:4	0h RW	**OS_POLICY (OS_POLICY):** OS-based software writes to these bits to select the policy that the BIOS will use after the platform resets due the WDT. The following convention is recommended for the BIOS and OS: 00 Boot normally 01 Shut down 10 Dont load OS. Hold in pre-boot state and use LAN to determine next step 11 Reserved Implementation note: These are just scratch pad bits. They should not be reset when the TCO logic resets the platform due to Watchdog Timer.

Bit Range	Default & Access	Field Name (ID): Description
3	1h RW	**SMB_ALERT_DISABLE:** Disables muxed GPIO/SMBALERT# signal as an alert source for the heartbeats and the SMBus slave. At reset (RSMRST# pin assertion only), this bit is set and the muxed GPIO/SMBALERT# alerts are disabled.
2:1	0h RW	**INTRD_SEL (INTRD_SEL):** Selects the action to take if the INTRUDER# signal goes active. 11: Reserved 01: Interrupt (as selected by TCO_INT_SEL). 10: SMI# 00 INTRUDER# doesn't cause SMI# or interrupt
0	0h RO	Reserved.

34.1.8 TCO_MESSAGE1 and TCO_MESSAGE2 (TMSG)—Offset Ch

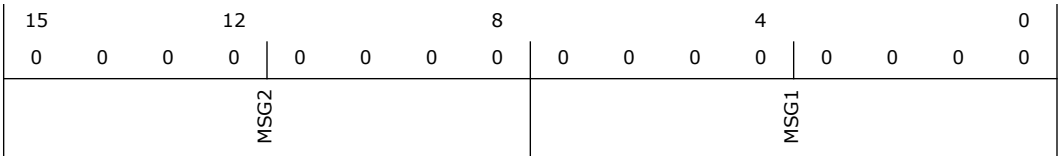
TCOBASE+0Ch (MSG1) TCOBASE+0Dh (MSG2) BIOS can write into these registers to indicate its boot progress. The external microcontroller can read these registers to monitor the boot progress

Access Method

Type: IO Register
(Size: 16 bits)

Device: 31
Function: 4

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RW	**TCO_MESSAGE2 (MSG2)**
7:0	0h RW	**TCO_MESSAGE1 (MSG1)**

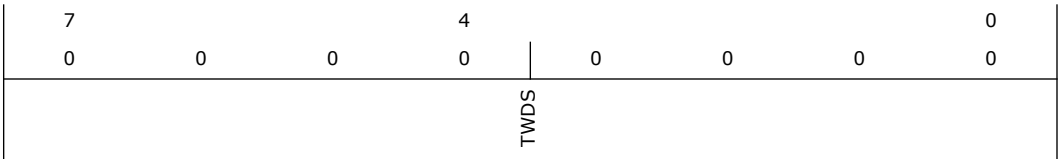
34.1.9 TCO_WDSTATUS Register (TWDS)—Offset Eh

Access Method

Type: IO Register
(Size: 8 bits)

Device: 31
Function: 4

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**TCO_WDSTATUS Register (TWDS):** The BIOS or system management software can write into this register to indicate more details on the boot progress. The register will rest to 00h based on a RSMRST# (but not PCI Reset). The external microcontroller can read this register to monitor boot progress.

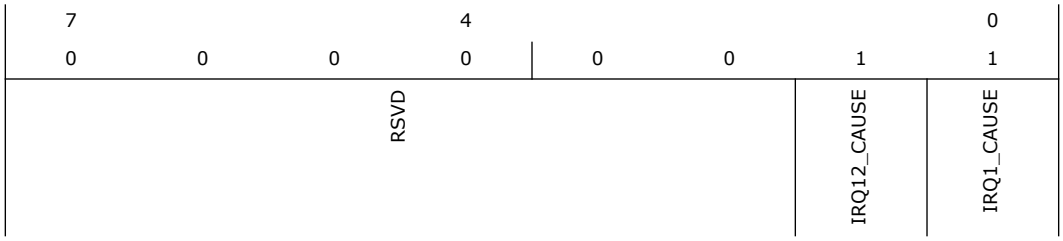
34.1.10 LEGACY_ELIM Register (LE)—Offset 10h

Access Method

Type: IO Register
(Size: 8 bits)

Device: 31
Function: 4

Default: 3h



Bit Range	Default & Access	Field Name (ID): Description
7:2	0h RO	Reserved.
1	1h RW	**IRQ12_CAUSE (IRQ12_CAUSE):** When software sets the bit to 1, IRQ12 will be high (asserted). When software sets the bit to 0, IRQ12 will be low (not asserted). Default for this bit is 1.
0	1h RW	**IRQ1_CAUSE (IRQ1_CAUSE):** When software sets the bit to 1, IRQ1 will be high (asserted). When software sets the bit to 0, IRQ1 will be low (not asserted). Default for this bit is 1.

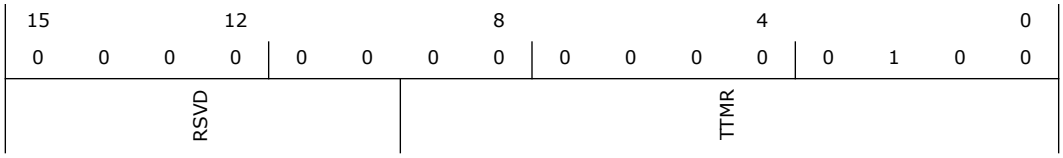
34.1.11 TCO_TMR Register (TTMR)—Offset 12h

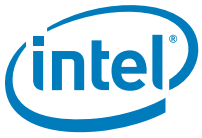
Access Method

Type: IO Register
(Size: 16 bits)

Device: 31
Function: 4

Default: 4h





Bit Range	Default & Access	Field Name (ID): Description
15:10	0h RO	Reserved.
9:0	4h RW	**TCOTMR (TTMR):** Value that is loaded into the timer each time the TCO_RLD register is written. Values of 0000h or 0001h will be ignored and should not be attempted. The timer is clocked at approximately 0.6 seconds, and thus allows timeouts ranging from 1.2 second to 613.8 seconds. Note: The timer has an error of +/- 1 tick (0.6s).

§ §

35 Additional Configuration Registers

35.1 FIA Configuration PCR Registers Summary

These registers are within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID + Register Offset).

Table 35-1. Summary of FIA Configuration PCR Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	Common Control (CC)—Offset 0h	0h
100h	103h	Device Reference Clock Request Mapping 1 (DRCRM1)—Offset 100h	76543210h
104h	107h	Device Reference Clock Request Mapping 2 (DRCRM2)—Offset 104h	BA98h
108h	10Bh	Device Reference Clock Request Mapping 3 (DRCRM3)—Offset 108h	F0000000h
200h	203h	Strap Configuration 1 (STRPFUSECFG1)—Offset 200h	0h
250h	253h	HSIO Lane Owner Status 1 (LOS1)—Offset 250h	0h
254h	257h	HSIO Lane Owner Status 2 (LOS2)—Offset 254h	0h
258h	25Bh	HSIO Lane Owner Status 3 (LOS3)—Offset 258h	0h
25Ch	25Fh	Lane Owner Status 4 (LOS4)—Offset 25Ch	0h

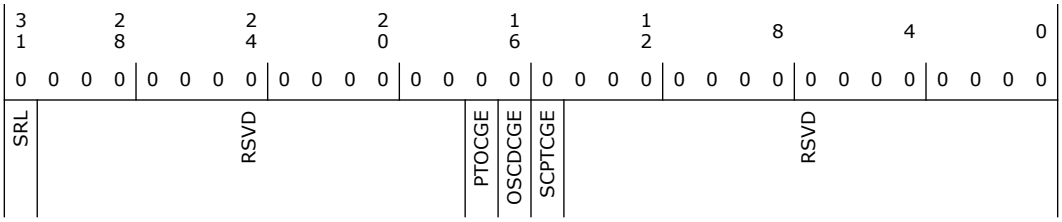
35.1.1 Common Control (CC)—Offset 0h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/O	**Secured Register Lock (SRL):** When this bit is set, all the secured registers will be locked and will be Read-Only.
30:18	0h RO	Reserved.
17	0h RW	**Partition/Trunk Oscillator Clock Gating Enable (PTOCGE):** When set, the oscillator and side clock will be dynamically clock gated when the conditions to clock gate are met. When clear, the oscillator and side clock will never be dynamically clock gated.
16	0h RW	**Oscillator/Side Clock Dynamic Clock Gating Enable (OSCDCGE):** When set, the oscillator and side clock will be dynamically clock gated when the conditions to clock gate are met. When clear, the oscillator and side clock will never be dynamically clock gated.
15	0h RW	**Side Clock Partition/Trunk Clock Gating Enable (SCPTCGE):** When set, the Side Clock will be clock gated at the partition/trunk level when the conditions to clock gate are met. When clear, the Side Clock will never be clock gated at the partition/trunk level.
14:0	0h RO	Reserved.

35.1.2 Device Reference Clock Request Mapping 1 (DRCRM1)—Offset 100h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 76543210h

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	0	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0
P8CKRQM				P7CKRQM				P6CKRQM				P5CKRQM				P4CKRQM				P3CKRQM				P2CKRQM				P1CKRQM			

Bit Range	Default & Access	Field Name (ID): Description
31:28	7h RW/L	**PCI Express Port 8 CLKREQ Mapping (P8CKRQM):** Same description as bit [3:0], except that this field applies to PCIe Port 8.
27:24	6h RW/L	**PCI Express Port 7 CLKREQ Mapping (P7CKRQM):** Same description as bit [3:0], except that this field applies to PCIe Port 7.
23:20	5h RW/L	**PCI Express Port 6 CLKREQ Mapping (P6CKRQM):** Same description as bit [3:0], except that this field applies to PCIe Port 6.
19:16	4h RW/L	**PCIe Express Port 5 CLKREQ Mapping (P5CKRQM):** Same description as bit [3:0], except that this field applies to PCIe Port 5.
15:12	3h RW/L	**PCI Express Port 4 CLKREQ Mapping (P4CKRQM):** Same description as bit [3:0], except that this field applies to PCIe Port 4.
11:8	2h RW/L	**PCI Express Port 3 CLKREQ Mapping (P3CKRQM):** Same description as bit [3:0], except that this field applies to PCIe Port 3.
7:4	1h RW/L	**PCI Express Port 2 CLKREQ Mapping (P2CKRQM):** Same description as bit [3:0], except that this field applies to PCIe Port 2.
3:0	0h RW/L	**PCI Express Port 1 CLKREQ Mapping (P1CKRQM):** The mapping of PCI Express Port 1 to the corresponding CLKREQ# pin is configured by this field. 0000b: Port 1 maps to CLKREQ0# pin. 0001b: Port 1 maps to CLKREQ1# pin. 0010b: Port 1 maps to CLKREQ2# pin. 0011b: Port 1 maps to CLKREQ3# pin. 0100b: Port 1 maps to CLKREQ4# pin. 0101b: Port 1 maps to CLKREQ5# pin. Others: reserved Software must never map multiple Express Ports to the same CLKREQ# pin. The hardware behavior is undefined if this ever happens. Note: This field must be configured prior to enabling any power management features.Configuring this field to map to any unsupported CLKREQ# pins (reserved values) may result in undefined hardware behavior. This register bit is Read-Only when the CC.SRL bit is set. Register Attribute: Static.

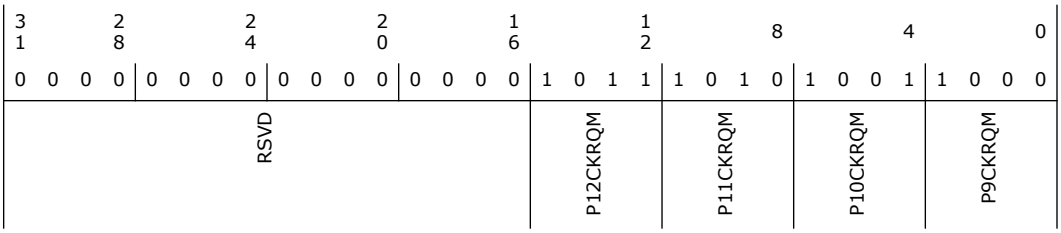
35.1.3 Device Reference Clock Request Mapping 2 (DRCRM2)—Offset 104h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: BA98h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:12	Bh RW/L	**PCI Express Port 12 CLKREQ Mapping (P12CKRQM):** Same description as bit [3:0], except that this field applies to PCIe Port 12.

Bit Range	Default & Access	Field Name (ID): Description
11:8	Ah RW/L	**PCI Express Port 11 CLKREQ Mapping (P11CKRQM):** Same description as bit [3:0], except that this field applies to PCIe Port 11.
7:4	9h RW/L	**PCI Express Port 10 CLKREQ Mapping (P10CKRQM):** Same description as bit [3:0], except that this field applies to PCIe Port 10.
3:0	8h RW/L	**PCI Express Port 9 CLKREQ Mapping (P9CKRQM):** The mapping of PCI Express Port 9 to the corresponding CLKREQ# pin is configured by this field. 0000b: Port 9 maps to CLKREQ0# pin. 0001b: Port 9 maps to CLKREQ1# pin. 0010b: Port 9 maps to CLKREQ2# pin. 0011b: Port 9 maps to CLKREQ3# pin. 0100b: Port 9 maps to CLKREQ4# pin. 0101b: Port 9 maps to CLKREQ5# pin. Others: reserved Software must never map multiple Express Ports to the same CLKREQ# pin. The hardware behavior is undefined if this ever happens. Note: This field must be configured prior to enabling any power management features. Configuring this field to map to any unsupported CLKREQ# pins (reserved values) may result in undefined hardware behavior. This register bit is Read-Only when the CC.SRL bit is set. Register Attribute: Static.

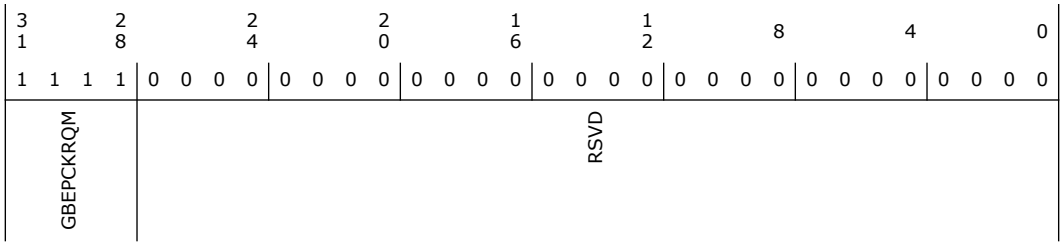
35.1.4 Device Reference Clock Request Mapping 3 (DRCRM3)—Offset 108h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: F0000000h



Bit Range	Default & Access	Field Name (ID): Description
31:28	Fh RW/L	**GbE Port CLKREQ Mapping (GBEPCKRQM):** The mapping of GbE port to the corresponding CLKREQ# pin is configured by this field. 0000b: GbE port maps to CLKREQ0# pin. 0001b: GbE port maps to CLKREQ1# pin. 0010b: GbE port maps to CLKREQ2# pin. 0011b: GbE port maps to CLKREQ3# pin. 0100b: GbE port maps to CLKREQ4# pin. 0101b: GbE port maps to CLKREQ5# pin. Software must never map multiple Express Ports to the same CLKREQ# pin. The hardware behavior is undefined if this ever happens. Note: This field must be configured prior to enabling any power management features. Note: This register bit is Read-Only when the CC.SRL bit is set. Register Attribute: Static.
27:0	0h RO	Reserved.

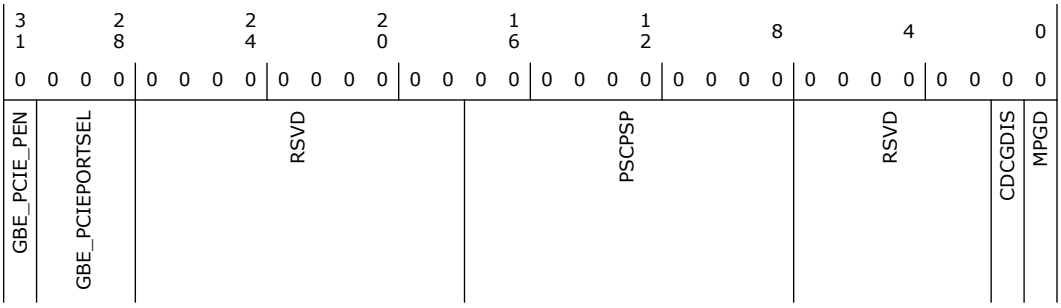
35.1.5 Strap Configuration 1 (STRPFUSECFG1)—Offset 200h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**GbE Over PCI Express Port Enable Strap (GBE_PCIE_PEN):** 0 : GbE MAC/PHY port communication is not enabled over PCI Express. 1 : The PCI Express port will be used for GbE MAC/PHY over PCI Express communication. Note: This field is only applicable if GbE is supported, otherwise this will be RO Reserved bit.
30:28	0h RO/V	**GBE PCIe Port Select Strap (GBE_PCIEPORTSEL):** Used to determine which PCIe port to be used for GbE MAC/PHY over PCI Express communication. 000: Port 3. 001: Port 4. 010: Port 5. 011: Port 9. 100: Port 10. Others: Reserved. Note: This field is only applicable if GbE is supported, otherwise this will be RO Reserved bit.
27:18	0h RO	Reserved.
17:8	0h RO/V	**PCIe/SATA Combo Port Select Polarity (PSCPSP):** 0: When the Combo Port Select pin is '0, PCIe mode is selected. When the Combo Port Select pin is '1, SATA mode is selected. 1: When the Combo Port Select pin is '0, SATA mode is selected. When the Combo Port Select pin is '1, PCIe mode is selected. This field is expected to be set to '1 when the combo port is mapped to M.2 or SATAe connector and set to '0 when the combo port is mapped to mSATA connector.
7:2	0h RO	Reserved.
1	0h RO/V	**Core Dynamic Clock Gating Disable (CDCGDIS):** 0: Core dynamic clock gating enabled. 1: Core dynamic clock gating disabled. This affects clock gating in SATA, DMI, PCIe, PMC, Audio, LAN, and SMBUS.
0	0h RO/V	**mod-PHY Power Gating Disabled (MPGD):** 0b: mod-PHY power gating capability is enabled. 1b: mod-PHY power gating capability is disabled.

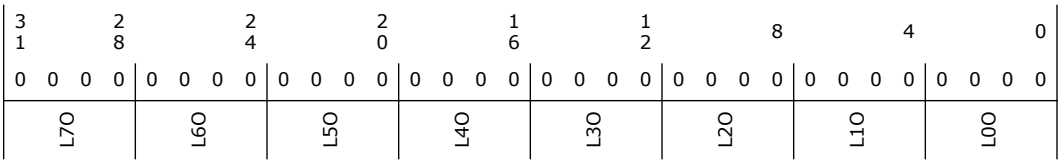
35.1.6 HSIO Lane Owner Status 1 (LOS1)—Offset 250h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO/V	**Lane 7 Owner (L7O):** Same description as bits [3:0].
27:24	0h RO/V	**Lane 6 Owner (L6O):** Same description as bits [3:0].
23:20	0h RO/V	**Lane 5 Owner (L5O):** Same description as bits [3:0].
19:16	0h RO/V	**Lane 4 Owner (L4O):** Same description as bits [3:0].
15:12	0h RO/V	**Lane 3 Owner (L3O):** Same description as bits [3:0].
11:8	0h RO/V	**Lane 2 Owner (L2O):** Same description as bits [3:0].
7:4	0h RO/V	**Lane 1 Owner (L1O):** Same description as bits [3:0].
3:0	0h RO/V	**Lane 0 Owner (L0O):** This register indicates the lane owner for Lane 0. 0000: PCIe/DMI. 0001: USB3. 0010: SATA. 0011: GbE. 0101: SSIC. 0110: CSI2. Others: Reserved.

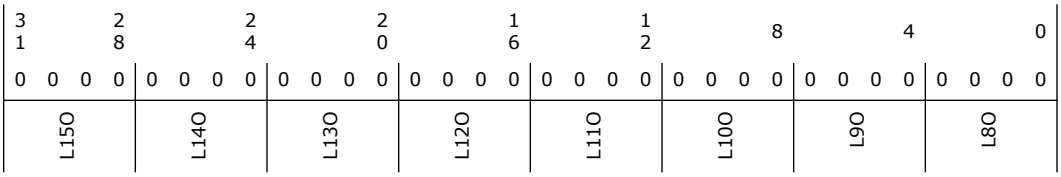
35.1.7 HSIO Lane Owner Status 2 (LOS2)—Offset 254h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO/V	**Lane 15 Owner (L15O):** Same description as bits [3:0].
27:24	0h RO/V	**Lane 14 Owner (L14O):** Same description as bits [3:0].
23:20	0h RO/V	**Lane 13 Owner (L13O):** Same description as bits [3:0].
19:16	0h RO/V	**Lane 12 Owner (L12O):** Same description as bits [3:0].
15:12	0h RO/V	**Lane 11 Owner (L11O):** Same description as bits [3:0].
11:8	0h RO/V	**Lane 10 Owner (L10O):** Same description as bits [3:0].
7:4	0h RO/V	**Lane 9 Owner (L9O):** Same description as bits [3:0].
3:0	0h RO/V	**Lane 8 Owner (L8O):** This register indicates the lane owner for Lane 8. 0000: PCIe/DMI. 0001: USB3. 0010: SATA. 0011: GbE. 0101: SSIC. 0110: CSI2. Others: Reserved.

35.1.8 HSIO Lane Owner Status 3 (LOS3)—Offset 258h

Size:32 bits
FIA Private Configuration Register: Offset 258h: LOS3 - Lane Owner Status 3

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

31 28	27 24	23 20	19 16	15 12	11 8	7 4	3 0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
L23O	L22O	L21O	L20O	L19O	L18O	L17O	L16O

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO/V	**Lane 23 Owner (L23O):** Same description as bits [3:0].
27:24	0h RO/V	**Lane 22 Owner (L22O):** Same description as bits [3:0].
23:20	0h RO/V	**Lane 21 Owner (L21O):** Same description as bits [3:0].
19:16	0h RO/V	**Lane 20 Owner (L20O):** Same description as bits [3:0].
15:12	0h RO/V	**Lane 19 Owner (L19O):** Same description as bits [3:0].
11:8	0h RO/V	**Lane 18 Owner (L18O):** Same description as bits [3:0].
7:4	0h RO/V	**Lane 17 Owner (L17O):** Same description as bits [3:0].
3:0	0h RO/V	**Lane 16 Owner (L16O):** This register indicates the lane owner for Lane 16. 0000: PCIe/DMI. 0001: USB3. 0010: SATA. 0011: GbE. 0101: SSIC. 0110: CSI2. Others: Reserved.

35.1.9 Lane Owner Status 4 (LOS4)—Offset 25Ch

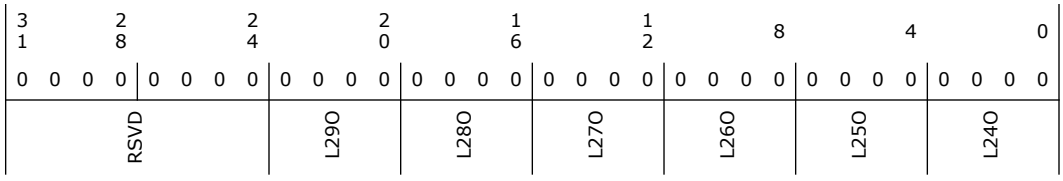
FIA Private Configuration Register: Offset 25Ch: LOS4 - Lane Owner Status 4

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:20	0h RO/V	**Lane 29 Owner (L29O):** Same description as bits [3:0].
19:16	0h RO/V	**Lane 28 Owner (L28O):** Same description as bits [3:0].
15:12	0h RO/V	**Lane 27 Owner (L27O):** Same description as bits [3:0].
11:8	0h RO/V	**Lane 26 Owner (L26O):** Same description as bits [3:0].
7:4	0h RO/V	**Lane 25 Owner (L25O):** Same description as bits [3:0].
3:0	0h RO/V	**Lane 24 Owner (L24O):** This register indicates the lane owner for Lane 24. 0000: PCIe/DMI. 0001: USB3. 0010: SATA. 0011: GbE. 0101: SSIC. 0110: CSI2. Others: Reserved.

35.2 OPI PCR Registers Summary

These registers are within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID + Register Offset).

Table 35-2. Summary of OPI PCR Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	Target Link Speed (TLS)—Offset 0h	0h
2014h	2017h	Virtual Channel 0 Resource Control (V0CTL)—Offset 2014h	80000010h
2018h	201Bh	Virtual Channel 0 Resource Status (V0STS)—Offset 2018h	0h
2020h	2023h	Virtual Channel 1 Resource Control (V1CTL)—Offset 2020h	0h
2024h	2027h	Virtual Channel 1 Resource Status (V1STS)—Offset 2024h	0h
2040h	2043h	ME Virtual Channel (VCm) Resource Control (VMCTL)—Offset 2040h	0h
2046h	2049h	ME Virtual Channel (VCm) Resource Status (VMSTS)—Offset 2046h	0h
2084h	2087h	Uncorrectable Error Status (UES)—Offset 2084h	0h
2088h	208Bh	Uncorrectable Error Mask (UEM)—Offset 2088h	0h
208Ch	208Fh	Uncorrectable Error Severity (UEV)—Offset 208Ch	0h
2090h	2093h	Correctable Error Status (CES)—Offset 2090h	0h
2094h	2097h	Correctable Error Mask (CEM)—Offset 2094h	2000h
20ACh	20AFh	Root Error Command (REC)—Offset 20ACh	0h

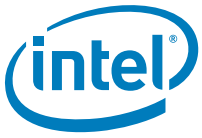


Table 35-2. Summary of OPI PCR Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
20B0h	20B3h	Root Error Status (RES)—Offset 20B0h	0h
20B4h	20B7h	Error Source Identification (ESID)—Offset 20B4h	0h
2234h	2237h	DMI Control Register (DMIC)—Offset 2234h	0h
223Ch	223Fh	IOSF Primary Control And Status (IPCS_IOSFSBCS)—Offset 223Ch	0h
2304h	2307h	DMI Port Link Control (DMILINKC)—Offset 2304h	0h
2320h	2323h	DMI PLL Shutdown (DMIPLLDOWN)—Offset 2320h	0h
2334h	2337h	DMI Power Management Control (DMIPMCTL)—Offset 2334h	0h
2618h	261Bh	Link Configuration (LCFG)—Offset 2618h	0h
2724h	2727h	Thermal Throttling BIOS Assigned Thermal Base Address (TTTBARB)—Offset 2724h	0h
2728h	272Bh	Thermal Throttling BIOS Assigned Thermal Base High Address (TTTBARBH)—Offset 2728h	0h
2730h	2733h	LPC Generic I/O Range 1 (LPCLGIR1)—Offset 2730h	0h
2734h	2737h	LPC Generic I/O Range 2 (LPCLGIR2)—Offset 2734h	0h
2738h	273Bh	LPC Generic I/O Range 3 (LPCLGIR3)—Offset 2738h	0h
273Ch	273Fh	LPC Generic I/O Range 4 (LPCLGIR4)—Offset 273Ch	0h
2740h	2743h	LPC Generic Memory Range (LPCGMR)—Offset 2740h	0h
2744h	2747h	LPC BIOS Decode Enable (LPCBDE)—Offset 2744h	FFCFh
2748h	274Bh	uCode Patch Region (UCPR)—Offset 2748h	1h
274Ch	274Fh	General Control and Status (GCS)—Offset 274Ch	0h
2750h	2753h	I/O Trap Register 1 low (IOT1_LOW)—Offset 2750h	0h
2754h	2757h	I/O Trap Register 1 high (IOT1_HIGH)—Offset 2754h	0h
2758h	275Bh	I/O Trap Register 2 low (IOT2_LOW)—Offset 2758h	0h
275Ch	275Fh	I/O Trap Register 2 high (IOT2_HIGH)—Offset 275Ch	0h
2760h	2763h	I/O Trap Register 3 low (IOT3_LOW)—Offset 2760h	0h
2764h	2767h	I/O Trap Register 3 high (IOT3_HIGH)—Offset 2764h	0h
2768h	276Bh	I/O Trap Register 4 low (IOT4_LOW)—Offset 2768h	0h
276Ch	276Fh	I/O Trap Register 4 high (IOT4_HIGH)—Offset 276Ch	0h
2770h	2773h	LPC I/O Decode Range (LPCIOD)—Offset 2770h	0h
2774h	2777h	LPC I/O Enable (LPCIOE)—Offset 2774h	0h
2778h	277Bh	TCO Base Address (TCOBASE)—Offset 2778h	0h
27ACh	27AFh	PM Base Address (PMBASEA)—Offset 27ACh	0h
27B0h	27B3h	PM Base Control (PMBASEC)—Offset 27B0h	0h
27B4h	27B7h	ACPI Base Address (ACPIBA)—Offset 27B4h	0h
27B8h	27BBh	ACPI Base Destination ID (ACPIBDID)—Offset 27B8h	0h

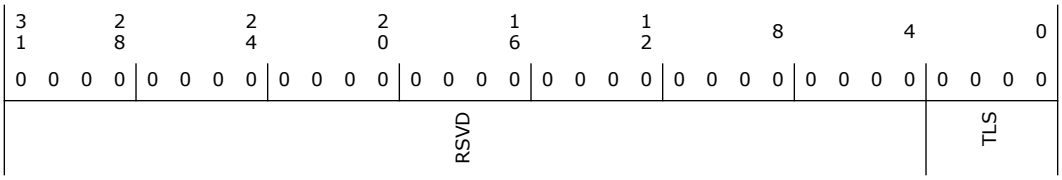
35.2.1 Target Link Speed (TLS)—Offset 0h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3:0	0h RO/S	**Target Link Speed (TLS):** Specifies the Target link speed that should be used if speed change is supported. Bit Description 0000 SPEED0: 100 Mb/s per-lane 0001 SPEED1: 1 Gb/s per-lane 0010 SPEED2: 2 Gb/s per-lane 0011-1111 Reserved Note: The default value of this field is defined by soft strap. This field is Read-only (RO) with TLS value defined by soft-strap.

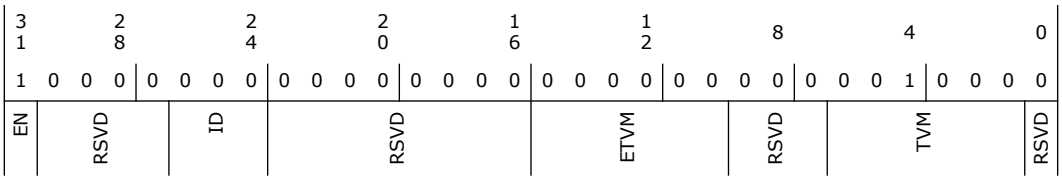
35.2.2 Virtual Channel 0 Resource Control (V0CTL)—Offset 2014h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 80000010h



Bit Range	Default & Access	Field Name (ID): Description
31	1h RO	**Virtual Channel Enable (EN):** Enables the VC when set. Disables the VC when cleared.
30:27	0h RO	Reserved.
26:24	0h RO	**Virtual Channel Identifier (ID):** Indicates the ID to use for this virtual channel
23:16	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
15:10	0h RW/L	**Extended TC/VC Map (ETVM):** Defines the upper 8-bits of the VC0 16-bit TC/VC mapping registers. These registers use the PCI Express reserved TC[3] traffic class bit.This register is locked down if the TCA1.TCLOCKDN register is Read-Only if DMIC.SRL field is set.
9:7	0h RO	Reserved.
6:1	8h RW/L	**Transaction Class / Virtual Channel Map (TVM):** Indicates which transaction classes are mapped to this virtual channel. When a bit is set, this transaction class is mapped to the virtual channel. This register is Read-Only if DMIC.SRL field is set.
0	0h RO	Reserved.

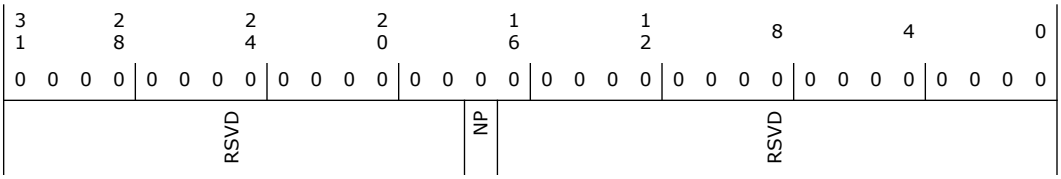
35.2.3 Virtual Channel 0 Resource Status (V0STS)—Offset 2018h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17	0h RO/V	**VC Negotiation Pending (NP):** When set, indicates the virtual channel is still being negotiated with ingress ports.
16:0	0h RO	Reserved.

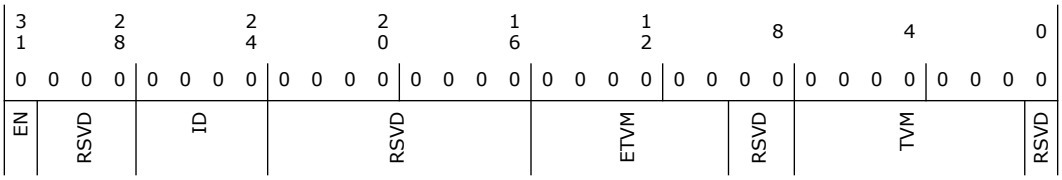
35.2.4 Virtual Channel 1 Resource Control (V1CTL)—Offset 2020h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**Virtual Channel Enable (EN):** Enables the VC when set. Disables the VC when cleared.
30:28	0h RO	Reserved.
27:24	0h RW/L	**Virtual Channel Identifier (ID):** Indicates the ID to use for this virtual channel. Note: BIOS is required to program VCID[3] to 0 when operating at DMI2.
23:16	0h RO	Reserved.
15:10	0h RW/L	**Extended TC/VC Map (ETVM):** Defines the upper 8-bits of the VC1 16-bit TC/VC mapping registers. These registers use the PCI Express reserved TC[3] traffic class bit. This register is Read-Only if the DMIC.SRL field is set. If VC1 is not enabled, the register output sent to the users of this register is forced to 0.
9:8	0h RO	Reserved.
7:1	0h RW/L	**Transaction Class / Virtual Channel Map (TVM):** Indicates which transaction classes are mapped to this virtual channel. When a bit is set, this transaction class is mapped to the virtual channel. This register is Read-Only if the DMIC.SRL field is set. If VC1 is not enabled, the register output sent to the users of this register is forced to 0.
0	0h RO	Reserved.

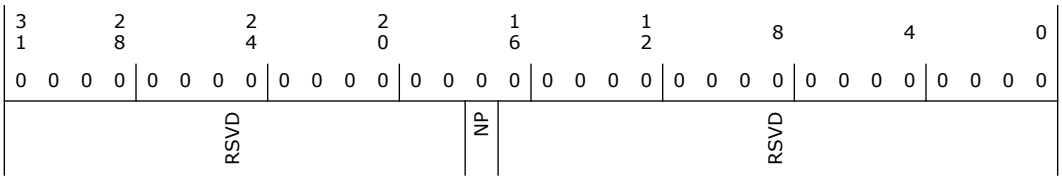
35.2.5 Virtual Channel 1 Resource Status (V1STS)—Offset 2024h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17	0h RO/V	**VC Negotiation Pending (NP):** When set, indicates the virtual channel is still being negotiated with ingress ports.
16:0	0h RO	Reserved.

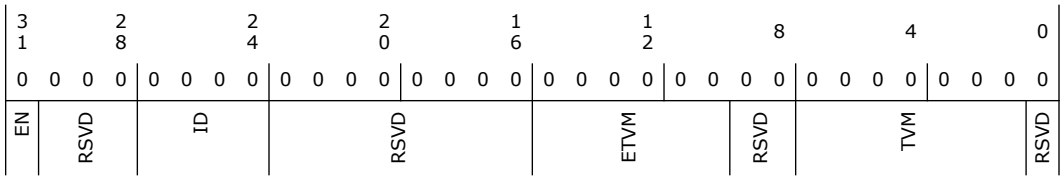
35.2.6 ME Virtual Channel (VCm) Resource Control (VMCTL)—Offset 2040h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**Virtual Channel Enable (EN)**
30:28	0h RO	Reserved.
27:24	0h RW/L	**Virtual Channel Identifier (ID)**
23:16	0h RO	Reserved.
15:10	0h RW/L	**Extended TC/VC Map (ETVM)**
9:8	0h RO	Reserved.
7:1	0h RW/L	**Transaction Class / Virtual Channel Map (TVM)**
0	0h RO	Reserved.

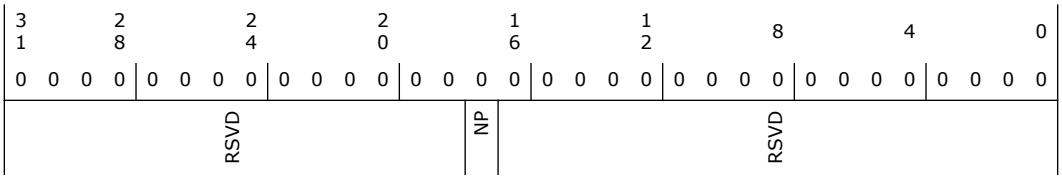
35.2.7 ME Virtual Channel (VCm) Resource Status (VMSTS)—Offset 2046h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17	0h RO/V	**VC Negotiation Pending (NP)**
16:0	0h RO	Reserved.

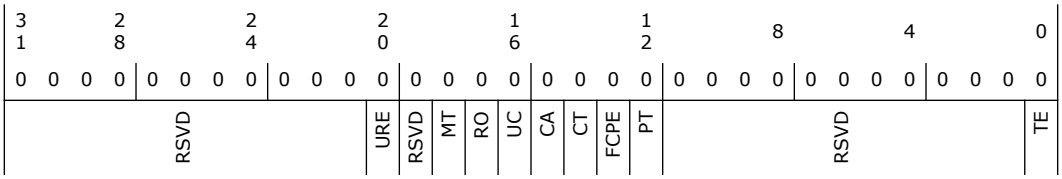
35.2.8 Uncorrectable Error Status (UES)—Offset 2084h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	Reserved.
20	0h RWC/P	**Unsupported Request Error Status (URE):** Indicates an unsupported request was received.
19	0h RO	Reserved.
18	0h RWC/P	**Malformed TLP Status (MT):** Indicates a malformed TLP was received.
17	0h RWC/P	**Receiver Overflow Status (RO):** Indicates a receiver overflow occurred.

Bit Range	Default & Access	Field Name (ID): Description
16	0h RO	**Unexpected Completion Status (UC):** Reserved, not supported.
15	0h RWC/P	**Completer Abort Status (CA):** Indicates a completer abort was received.
14	0h RO	**Completion Timeout Status (CT):** Reserved, not supported.
13	0h RO	**Flow Control Protocol Error Status (FCPE):** Reserved, not supported.
12	0h RWC/P	**Poisoned TLP Status (PT):** Indicates a poisoned TLP was received.
11:1	0h RO	Reserved.
0	0h RO	**Training Error Status (TE)**

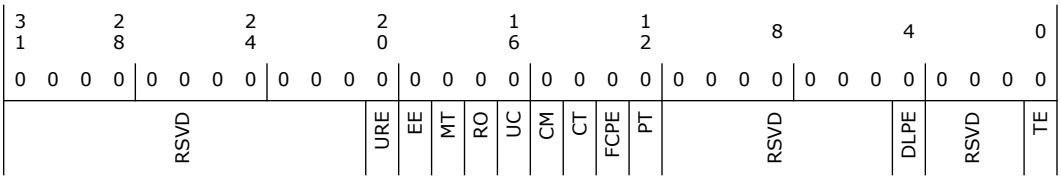
35.2.9 Uncorrectable Error Mask (UEM)—Offset 2088h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	Reserved.
20	0h RW/P	**Unsupported Request Error Mask (URE):** Mask for uncorrectable errors.
19	0h RO	**ECRC Error Mask (EE):** ECRC is not supported.
18	0h RW/P	**Malformed TLP Mask (MT):** Mask for malformed TLPs.
17	0h RW/P	**Receiver Overflow Mask (RO):** Mask for receiver overflows.
16	0h RO	**Unexpected Completion Mask (UC):** Reserved, Not supported.
15	0h RW/P	**Completer Abort Mask (CM):** Mask for completer abort.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RO	**Completion Timeout Mask (CT):** Reserved, not supported.
13	0h RO	**Flow Control Protocol Error Mask (FCPE)**
12	0h RW/P	**Poisoned TLP Mask (PT):** Mask for poisoned TLPs.
11:5	0h RO	Reserved.
4	0h RW/P	**Data Link Protocol Error Mask (DLPE):** Mask for data link protocol errors.
3:1	0h RO	Reserved.
0	0h RO	**Training Error Mask (TE):** Not supported.

35.2.10 Uncorrectable Error Severity (UEV)—Offset 208Ch

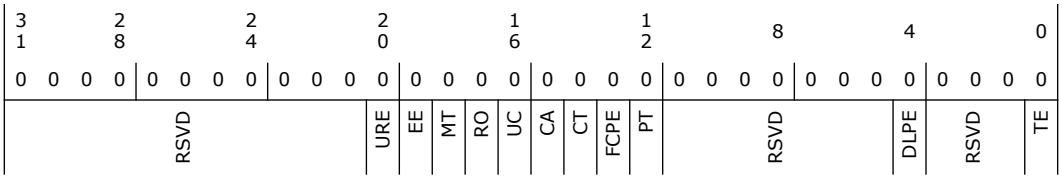
These registers are reset by core PWROK

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	Reserved.
20	0h RW/P	**Unsupported Request Error Severity (URE):** Severity for unsupported request reception.
19	0h RO	**ECRC Error Severity (EE):** Not Supported.
18	0h RW/P	**Malformed TLP Severity (MT):** Severity for malformed TLP reception.
17	0h RW/P	**Receiver Overflow Severity (RO):** Severity for receiver overflow occurrences.
16	0h RO	**Unexpected Completion Severity (UC):** Not supported.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/P	**Completer Abort Severity (CA):** Severity for completer.
14	0h RO	**Completion Timeout Severity (CT):** Not supported.
13	0h RO	**Flow Control Protocol Error Severity (FCPE):** Not supported.
12	0h RW/P	**Poisoned TLP Severity (PT):** Severity for poisoned TLP reception.
11:5	0h RO	Reserved.
4	0h RW/P	**Data Link Protocol Error Severity (DLPE):** Severity for data link protocol errors.
3:1	0h RO	Reserved.
0	0h RW/P	**Training Error Severity (TE):** TE not supported. This bit is RW for ease of implementation.

35.2.11 Correctable Error Status (CES)—Offset 2090h

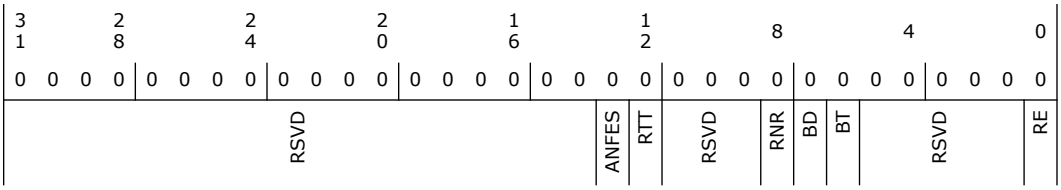
These registers are reset by core PWROK

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13	0h RWC/P	**Advisory Non-Fatal Error Status (ANFES):** When set, indicates that a Advisory Non-Fatal Error occurred.
12	0h RWC/P	**Replay Timer Timeout Status (RTT):** Indicates the replay timer timed out.
11:9	0h RO	Reserved.
8	0h RWC/P	**Replay Number Rollover Status (RNR):** Indicates the replay number rolled over.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RWC/P	**Bad DLLP Status (BD):** Indicates a bad DLLP was received.
6	0h RWC/P	**Bad TLP Status (BT):** Indicates a bad TLP was received.
5:1	0h RO	Reserved.
0	0h RWC/P	**Receiver Error Status (RE):** Indicates a receiver error occurred.

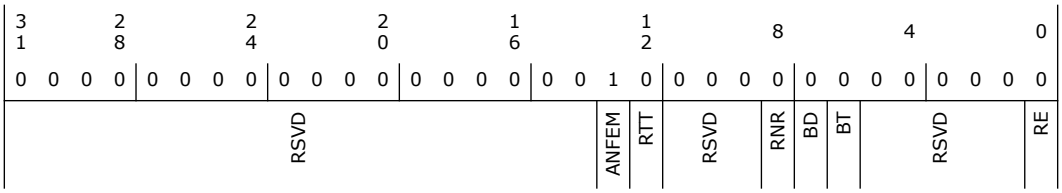
35.2.12 Correctable Error Mask (CEM)—Offset 2094h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 2000h



Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13	1h RW/P	**Advisory Non-Fatal Error Mask (ANFEM):** When set, masks Advisory Non-Fatal errors from (a) signaling ERR_COR to the device control register and (b) updating the Uncorrectable Error Status register. This register is set by default to enable compatibility with software that does not comprehend Role-Based Error Reporting.
12	0h RW/P	**Replay Timer Timeout Mask (RTT):** Mask for replay timer timeout.
11:9	0h RO	Reserved.
8	0h RW/P	**Replay Number Rollover Mask (RNR):** Mask for replay number rollover.
7	0h RW/P	**Bad DLLP Mask (BD):** Mask for bad DLLP reception.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW/P	**Bad TLP Mask (BT):** Mask for bad TLP reception.
5:1	0h RO	Reserved.
0	0h RW/P	**Receiver Error Mask (RE):** Mask for receiver errors.

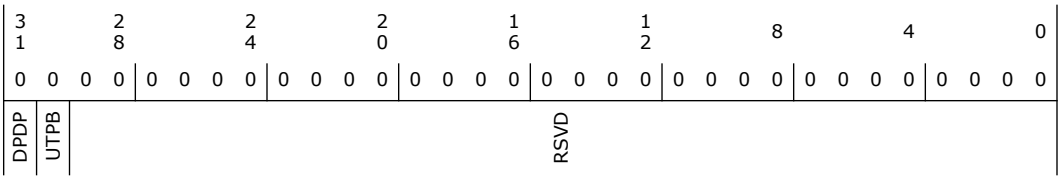
35.2.13 Root Error Command (REC)—Offset 20ACh

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Drop Poisoned Downstream Packets (DPDP):** When set to a '1': if downstream packet on OPI is received with the EP bit set, this packet and all subsquent packets with data received on DMI for any VC will have their Unsupported Transaction (UT) field set causing them to be forwarded to the Error Handler. When cleared to a '0', downstream packets from OPI with the EP bit set are forwarded onto the downstream backbone normally.
30	0h RW	**Unsupported Transaction Policy Bit (UTPB):** When set to 1, the Unsupported Transactions detected on OPI will not set the UES.URE bit. This subsequently ensures that SERR will never be signaled in response to Unsupported Transactions regardless of UEV.URE. When set to 0, the Unsupported Transactions detected on OPI will set the UES.URE bit.
29:0	0h RO	Reserved.

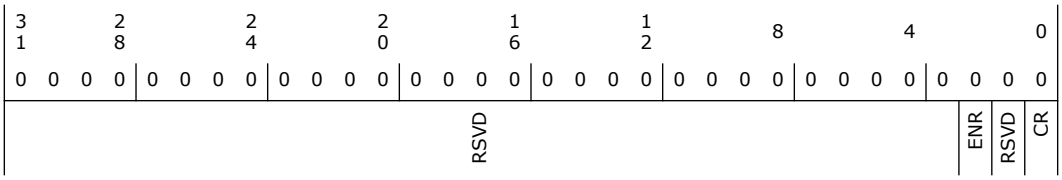
35.2.14 Root Error Status (RES)—Offset 20B0h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	Reserved.
2	0h RWC	**ERR_FATAL/NONFATAL Received (ENR):** Set when either a fatal or a non-fatal error message is received or an internal fatal error is detected (all internal uncorrectable errors are fatal).
1	0h RO	Reserved.
0	0h RWC	**ERR_COR Received (CR):** Set when a correctable error message is received or an internal correctable error is detected.

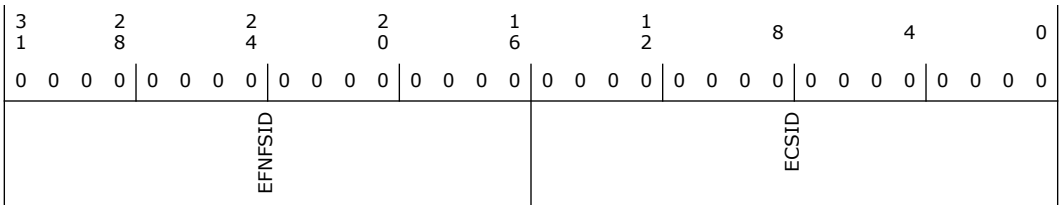
35.2.15 Error Source Identification (ESID)—Offset 20B4h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO/V	**ERR_FATAL/NONFATAL Source Identification (EFNFSID):** Loaded with the requester ID indicated in the received ERR_FATAL or ERR_NONFATAL message when RES.ENR is first set, or the internal requestor ID if an internally detected error.
15:0	0h RO/V	**ERR_COR Source Identification (ECSID):** Loaded with the requester ID indicated in the received ERR_COR message when RES.CR is first set, or the internal requester ID if an internally detected error

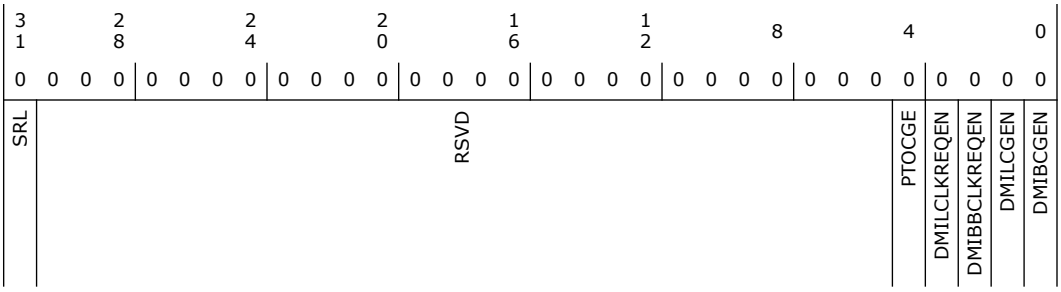
35.2.16 DMI Control Register (DMIC)—Offset 2234h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RWO	**Secured Register Lock (SRL):** When this bit is set, all the secured registers will be locked and will be Read-Only.
30:5	0h RO	Reserved.
4	0h RW	**Partition/Trunk Oscillator Clock Gate Enable (PTOCGE):** When set, this bit allows the oscillator clock to be gated at the partition/trunk level when the conditions are met. When cleared, the oscillator clock gating at the partition/trunk level is disabled.
3	0h RW	**DMI Link CLKREQ Enable (DMILCLKREQEN):** When set, this bit enables DMI to de-assert the DMI link CLKREQ. When cleared, DMI link CLKREQ is not allowed to de-assert.
2	0h RW	**DMI Backbone CLKREQ Enable (DMIBBCLKREQEN):** When set, this bit enables DMI to de-assert the Primary backbone CLKREQ. When cleared, DMI Primary backbone CLKREQ is not allowed to de-assert.
1	0h RW	**DMI Link Dynamic Clock Gate Enable (DMILCGEN):** When set, this bit enables dynamic clock gating on the DMI Link clock domain logic. When cleared, dynamic clock gating on the DMI Link clock domain is disabled.
0	0h RW	**DMI Backbone Dynamic Clock Gate Enable (DMIBCGEN):** When set, this bit enables dynamic clock gating on the DMI backbone domain logic. When cleared, dynamic clock gating on the DMI backbone clock domain is disabled.

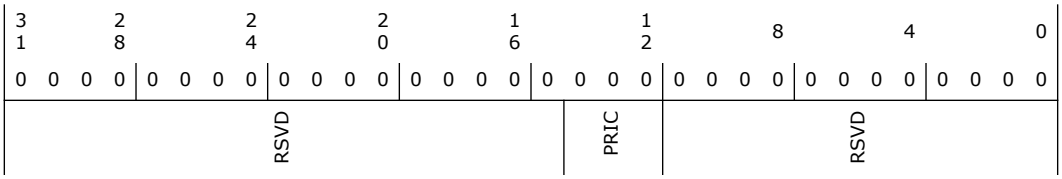
35.2.17 IOSF Primary Control And Status (IPCS_IOSFSBCS)—Offset 223Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RO	Reserved.
14:12	0h RW	**IOSF Primary ISM Idle Counter (PRIC):** BIOS may need to program this register field.
11:0	0h RO	Reserved.

35.2.18 DMI Port Link Control (DMILINKC)—Offset 2304h

BIOS may need to program this register.

35.2.19 DMI PLL Shutdown (DMIPLLDOWN)—Offset 2320h

BIOS may need to program this register.

35.2.20 DMI Power Management Control (DMIPMCTL)—Offset 2334h

BIOS may need to program this register.

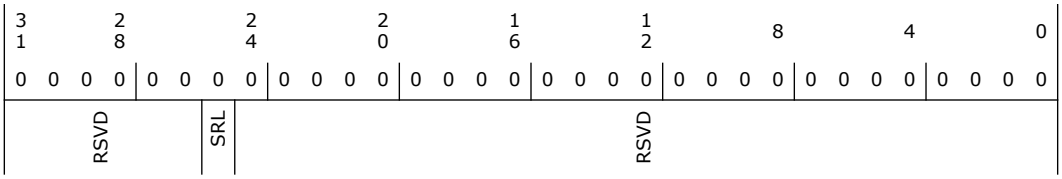
35.2.21 Link Configuration (LCFG)—Offset 2618h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	Reserved.
25	0h RW/L	**Secure Register Lock (SRL):** When set, the secured register will be locked.
24:0	0h RO	Reserved.

35.2.22 Thermal Throttling BIOS Assigned Thermal Base Address (TTTBARB)—Offset 2724h

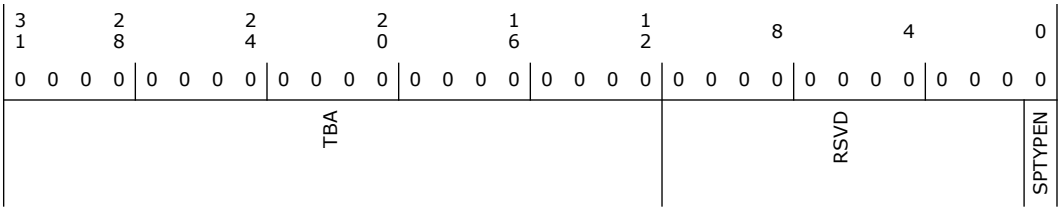
This BAR creates 4K bytes of memory space to signify the base address of Thermal memory mapped configuration registers. This memory space is active when TBARB.SPTYPEN is asserted. This BAR is owned by the BIOS, and allows the BIOS to locate the Thermal registers in system memory space.

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW/L	**Thermal Base Address (TBA):** Base address for the Thermal logic memory mapped configuration registers. 4KB bytes are requested by hardwiring bits 11:4 to 0s. This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.
11:1	0h RO	Reserved.
0	0h RW/L	**Space Type Enable (SPTYPEN):** When set to 1b by software, enables the decode of this memory BAR. This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.

35.2.23 Thermal Throttling BIOS Assigned Thermal Base High Address (TTTBARBH)—Offset 2728h

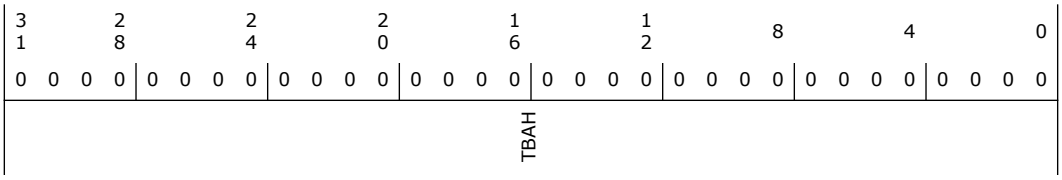
This BAR extension holds the high 32 bits of the 64 bit TBARB.

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/L	**Thermal Base Address High (TBAH):** TBAR bits 61:32. This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.

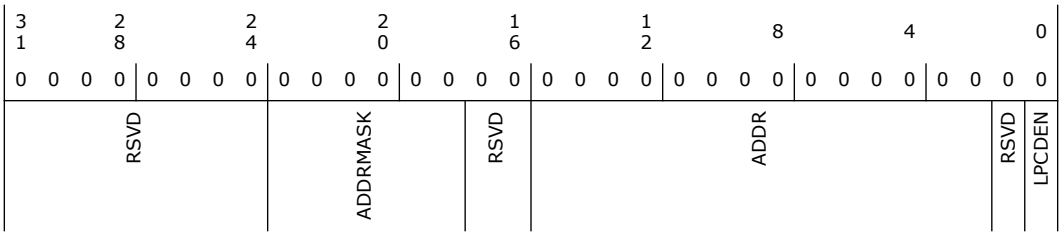
35.2.24 LPC Generic I/O Range 1 (LPCLGIR1)—Offset 2730h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:18	0h RW/L	**Address Mask (ADDRMASK)**
17:16	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
15:2	0h RW/L	**Address (ADDR)**
1	0h RO	Reserved.
0	0h RW/L	**LPC Decode Enable (LPCDEN)**

35.2.25 LPC Generic I/O Range 2 (LPCLGIR2)—Offset 2734h

Same description as LPCLGIR1 register.

35.2.26 LPC Generic I/O Range 3 (LPCLGIR3)—Offset 2738h

Same description as LPCLGIR1 register.

35.2.27 LPC Generic I/O Range 4 (LPCLGIR4)—Offset 273Ch

Same description as LPCLGIR1 register.

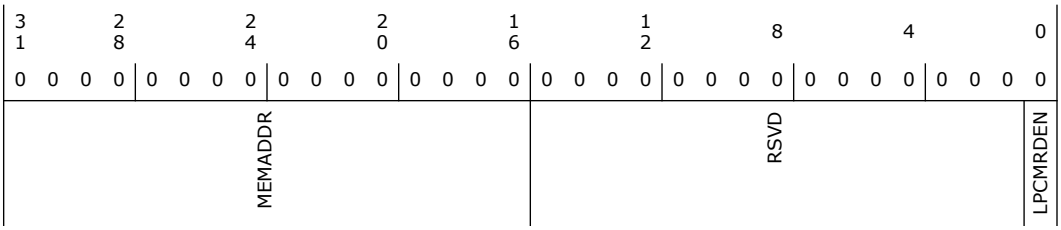
35.2.28 LPC Generic Memory Range (LPCGMR)—Offset 2740h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW/L	**Memory Address (MEMADDR)**
15:1	0h RO	Reserved.
0	0h RW/L	**LPC Memory Range Decode Enable (LPCMRDEN)**

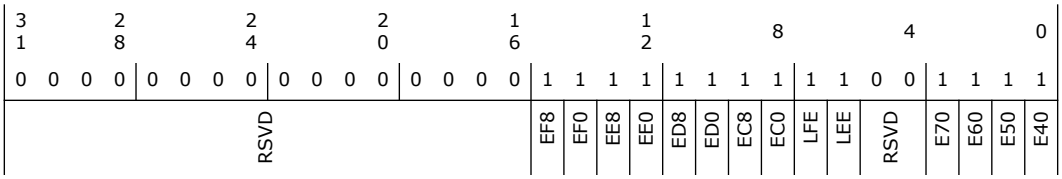
35.2.29 LPC BIOS Decode Enable (LPCBDE)—Offset 2744h

Access Method

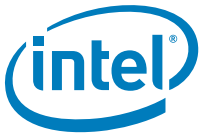
Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: FFCFh



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	1h RO	**F8-FF Enable (EF8):** Enables decoding of 512K of the following BIOS range: Data space: FFF80000h – FFFFFFFFh Feature space: FFB80000h – FFBFFFFFh Register Attribute: Static.
14	1h RW/L	**F0-F8 Enable (EF0):** Enables decoding of 512K of the following BIOS range: Data space: FFF00000h – FFF7FFFFh Feature space: FFB00000h – FFB7FFFFh This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.
13	1h RW/L	**E8-EF Enable (EE8):** Enables decoding of 512K of the following BIOS range: Data space: FFE80000h – FFEFFFFFh Feature space: FFA80000h – FFAFFFFFh This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.
12	1h RW/L	**E0-E8 Enable (EE0):** Enables decoding of 512K of the following BIOS range: Data space: FFE00000h – FFE7FFFFh Feature Space: FFA00000h – FFA7FFFFh This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.
11	1h RW/L	**D8-DF Enable (ED8):** Enables decoding of 512K of the following BIOS range: Data space: FFD80000h – FFDFFFFFh Feature space: FF980000h – FF9FFFFFh This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.
10	1h RW/L	**D0-D7 Enable (ED0):** Enables decoding of 512K of the following BIOS range: Data space: FFD00000h – FFD7FFFFh Feature space: FF900000h – FF97FFFFh This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.



Bit Range	Default & Access	Field Name (ID): Description
9	1h RW/L	**C8-CF Enable (EC8):** Enables decoding of 512K of the following BIOS range: Data space: FFC80000h – FFCFFFFFh Feature space: FF880000h – FF8FFFFFh This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.
8	1h RW/L	**C0-C7 Enable (EC0):** Enables decoding of 512K of the following BIOS range: Data space: FFC00000h – FFC7FFFFh Feature space: FF800000h – FF87FFFFh This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.
7	1h RW/L	**Legacy F Segment Enable (LFE):** This enables the decoding of the legacy 64KB range at F0000h – FFFFFh This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.
6	1h RW/L	**Legacy E Segment Enable (LEE):** This enables the decoding of the legacy 64KB range at E0000h – EFFFFh This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.
5:4	0h RO	Reserved.
3	1h RW/L	**70-7F Enable (E70):** Enables decoding of 1MB of the following BIOS range: Data space: FF700000h – FF7FFFFFh Feature space: FF300000h – FF3FFFFFh This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.
2	1h RW/L	**60-6F Enable (E60):** Enables decoding of 1MB of the following BIOS range: Data space: FF600000h – FF6FFFFFh Feature Space: FF200000h – FF2FFFFFh This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.
1	1h RW/L	**50-5F Enable (E50):** Enables decoding of 1MB of the following BIOS range: Data space: FF500000h – FF5FFFFFh Feature Space: FF100000h – FF1FFFFFh This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.
0	1h RW/L	**40-4F Enable (E40):** Enables decoding of 1MB of the following BIOS range: Data space: FF400000h – FF4FFFFFh Feature space: FF000000h – FF0FFFFFh This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.

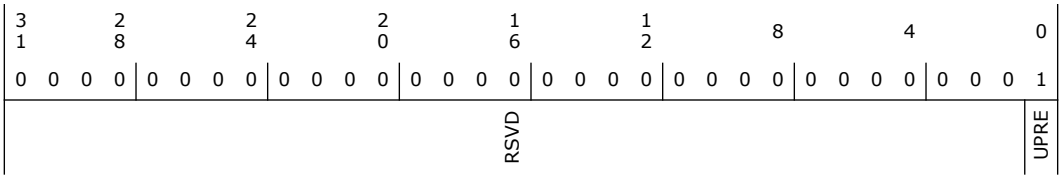
35.2.30 uCode Patch Region (UCPR)—Offset 2748h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 1h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	1h RW/L	**uCode Patch Region Enable (UPRE):** When set, enables memory access targeting the uCode patch region (0xFEF00000 to 0xFEFFFFFF) to be forwarded to SPI Flash. This register is Read-Only if the DMIC.SRL field is set. Note: This bit should never be set if the boot flash is on LPC. This bit can only be set if the boot flash is on SPI. Register Attribute: Static.

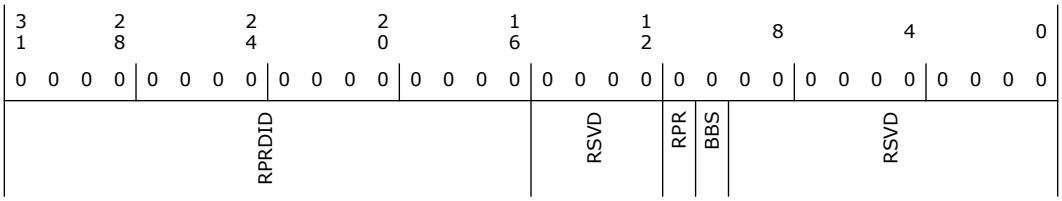
35.2.31 General Control and Status (GCS)—Offset 274Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW/L	**RPR Destination ID (RPRDID)**
15:12	0h RO	Reserved.
11	0h RW/L	**Reserved Page Route (RPR)**
10	0h RW/L/S	**Boot BIOS Strap (BBS)**
9:0	0h RO	Reserved.

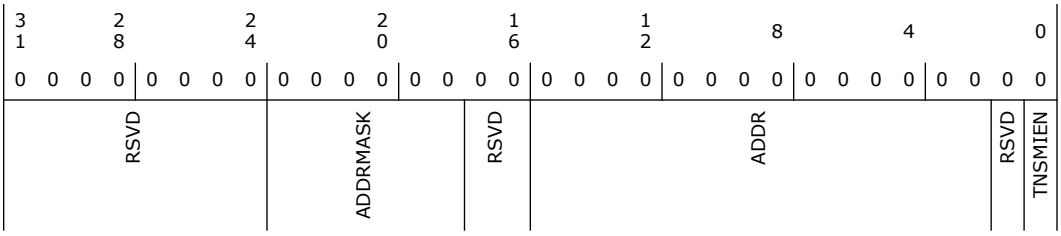
35.2.32 I/O Trap Register 1 low (IOT1_LOW)—Offset 2750h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:18	0h RW	**Address Mask (ADDRMASK):** A 1 in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for traps on address ranges up to 256 bytes in size.
17:16	0h RO	Reserved.
15:2	0h RW	**Address (ADDR):** DWord-aligned address.
1	0h RO	Reserved.
0	0h RW	**Trap and SMI# Enable (TNSMIEN):** When this bit is set to 1, then the trapping logic specified in this register is enabled.

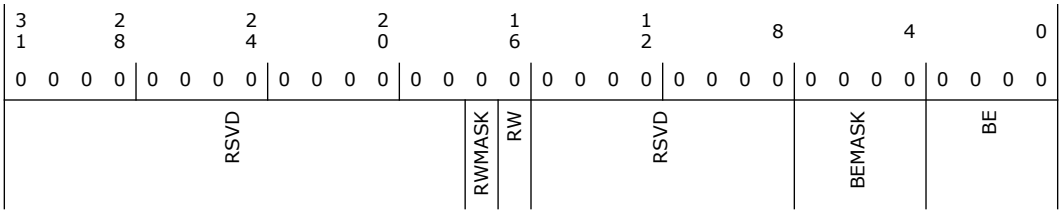
35.2.33 I/O Trap Register 1 high (IOT1_HIGH)—Offset 2754h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17	0h RW	**Read/Write Mask (RWMASK):** When this bit is 1, the trapping logic will operate on both read and write cycles. When this bit is 0, the cycle must match the type specified in bit 16.
16	0h RW	**Read/Write (RW):** 1 = Read 0 = Write The value in this field does not matter if bit 17 is set.
15:8	0h RO	Reserved.
7:4	0h RW	**Byte Enable Mask (BEMASK):** A 1 in any bit position indicates that any value in the corresponding byte enable bit in a received cycle will be treated as a match. The corresponding bit in the Byte Enables field, below, is ignored.
3:0	0h RW	**Byte Enables (BE):** Active-high, DWord-aligned byte enables.

35.2.34 I/O Trap Register 2 low (IOT2_LOW)—Offset 2758h

Same definition as IOT1_LOW register.

35.2.35 I/O Trap Register 2 high (IOT2_HIGH)—Offset 275Ch

Same definition as IOT1_HIGH register.

35.2.36 I/O Trap Register 3 low (IOT3_LOW)—Offset 2760h

Same definition as IOT1_LOW register.

35.2.37 I/O Trap Register 3 high (IOT3_HIGH)—Offset 2764h

Same definition as IOT1_HIGH register.

35.2.38 I/O Trap Register 4 low (IOT4_LOW)—Offset 2768h

Same definition as IOT1_LOW register.

35.2.39 I/O Trap Register 4 high (IOT4_HIGH)—Offset 276Ch

Same definition as IOT1_HIGH register.

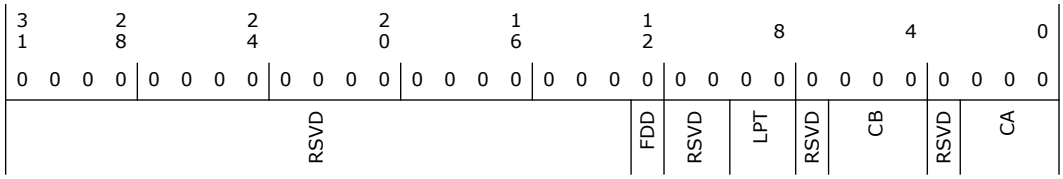
35.2.40 LPC I/O Decode Range (LPCIOD)—Offset 2770h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	Reserved.
12	0h RW/L	**FDD Range (FDD):** The following table describes which range to decode for the FDD Port. Bits Decode Range 0 3F0h – 3F5h, 3F7h (Primary) 1 370h – 375h, 377h (Secondary) This register is Read-Only if the DMIC.SRL field is set.
11:10	0h RO	Reserved.
9:8	0h RW/L	**LPT Range (LPT):** The following table describes which range to decode for the LPT Port. Bits Decode Range 00 378h - 37Fh and 778h – 77Fh 01 278h – 27Fh (port 279h is read only) and 678h – 67Fh 10 3BCh – 3BEh and 7BCh – 7BEh 11 Reserved This register is Read-Only if the DMIC.SRL field is set.
7	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
6:4	0h RW/L	**ComB Range (CB):** The following table describes which range to decode for the COMB Port. Bits Decode Range 000 3F8h – 3FFh (COM1) 001 2F8h – 2FFh (COM2) 010 220h – 227h 011 228h – 22Fh 100 238h – 23Fh 101 2E8h – 2EFh (COM 4) 110 338h – 33Fh 111 3E8h – 3EFh (COM 3) This register is Read-Only if the DMIC.SRL field is set.
3	0h RO	Reserved.
2:0	0h RW/L	**ComA Range (CA):** The following table describes which range to decode for the COMA Port. Bits Decode Range 000 3F8h – 3FFh (COM1) 001 2F8h – 2FFh (COM2) 010 220h – 227h 011 228h – 22Fh 100 238h – 23Fh 101 2E8h – 2EFh (COM 4) 110 338h – 33Fh 111 3E8h – 3EFh (COM 3) This register is Read-Only if the DMIC.SRL field is set.

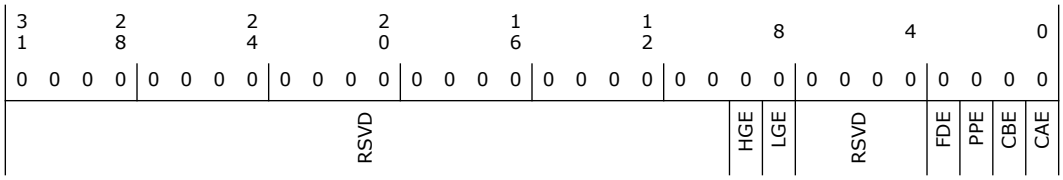
35.2.41 LPC I/O Enable (LPCIOE)—Offset 2774h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9	0h RW/L	**High Gameport Enable (HGE):** Enables decoding of the I/O locations 208h to 20Fh to LPC. This register is Read-Only if the DMIC.SRL field is set.
8	0h RW/L	**Low Gameport Enable (LGE):** Enables decoding of the I/O locations 200h to 207h to LPC. This register is Read-Only if the DMIC.SRL field is set.
7:4	0h RO	Reserved.
3	0h RW/L	**Floppy Drive Enable (FDE):** Enables decoding of the FDD range to LPC. Range is selected by LIOD.FDE. This register is Read-Only if the DMIC.SRL field is set.
2	0h RW/L	**Parallel Port Enable (PPE):** Enables decoding of the LPT range to LPC. Range is selected by LIOD.LPT. This register is Read-Only if the DMIC.SRL field is set.
1	0h RW/L	**Com Port B Enable (CBE):** Enables decoding of the COMB range to LPC. Range is selected by LIOD.CB. This register is Read-Only if the DMIC.SRL field is set.
0	0h RW/L	**Com Port A Enable (CAE):** Enables decoding of the COMA range to LPC. Range is selected by LIOD.CA. This register is Read-Only if the DMIC.SRL field is set.

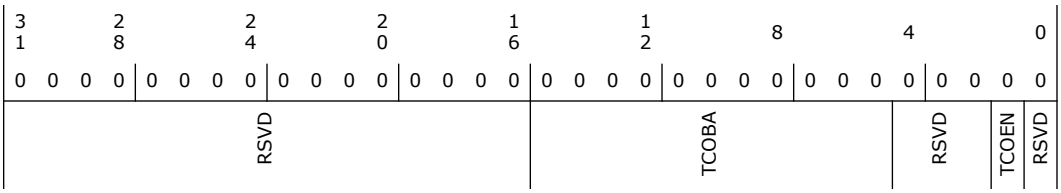
35.2.42 TCO Base Address (TCOBASE)—Offset 2778h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:5	0h RW/L	**TCO Base Address (TCOBA):** Provides the 32 bytes of I/O space for TCO logic, that can be map anywhere in the 64k I/O space on 32-byte boundaries. This register is Read-Only if the DMIC.SRL field is set.
4:2	0h RO	Reserved.
1	0h RW/L	**TCO Enable (TCOEN):** When set, decode of the I/O range specified by the TCO base address. This register is Read-Only if the DMIC.SRL field is set.
0	0h RO	Reserved.

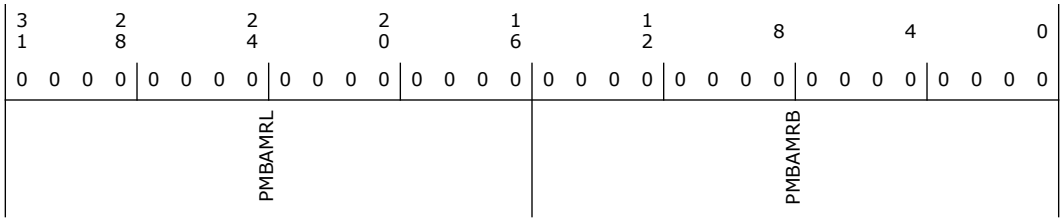
35.2.43 PM Base Address (PMBASEA)—Offset 27ACh

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW/L	**PM Base Address Memory Range Limit (PMBAMRL):** This field specifies limit address bits[31:16] for the PM Base Address memory range. Bits [15:0] are assumed to be FFFFh. This register is Read-Only if the DMIC.SRL field is set.
15:0	0h RW/L	**PM Base Address Memory Range Base (PMBAMRB):** This field specifies base address bits[31:16] for the PM Base Address memory range. Bits [15:0] are assumed to be 0000h. This register is Read-Only if the DMIC.SRL field is set.

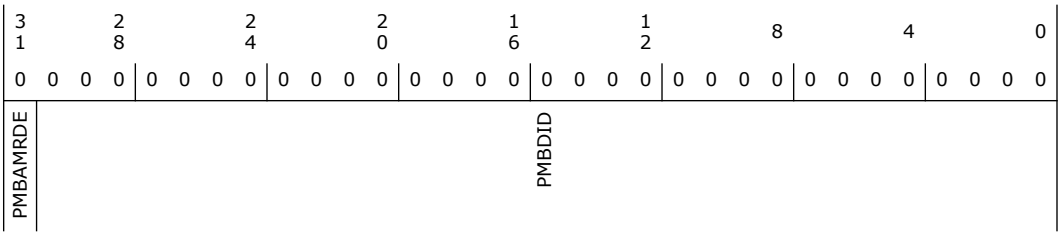
35.2.44 PM Base Control (PMBASEC)—Offset 27B0h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**PM Base Address Memory Range Decode Enable (PMBAMRDE):** When enabled, memory cycles that falls within the PMBASEADDR.PMBAMRB and PMBASEADDR.PMBAMRL range inclusive will be forwarded using source decode to the destination ID specified in PMBASEC.PMBDID field. This register is Read-Only if the DMIC.SRL field is set.
30:0	0h RW/L	**PM Base Destination ID (PMBDID):** The destination ID to be used to forward the cycle decoded to hit the PM Base Address range. BIOS must program the bits which are not used to zeros. Hardware will ignore the unused bits. This register is Read-Only if the DMIC.SRL field is set.

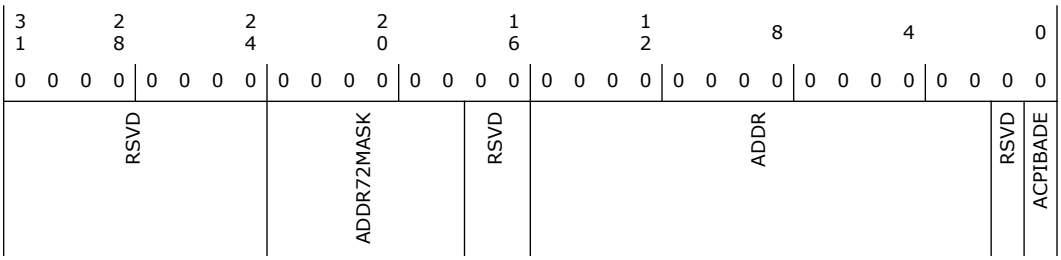
35.2.45 ACPI Base Address (ACPIBA)—Offset 27B4h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:18	0h RW/L	**Address[7:2] Mask (ADDR72MASK):** A 1 in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for decoding blocks up to 256 bytes in size. This register is Read-Only if the DMIC.SRL field is set.
17:16	0h RO	Reserved.
15:2	0h RW/L	**Address[15:2] (ADDR):** DWord-aligned address. Note that PCH does not provide decode down to the word or byte level. This register is Read-Only if the DMIC.SRL field is set.
1	0h RO	Reserved.
0	0h RW/L	**ACPI Base Address Decode Enable (ACPIBADE):** When this bit is set to 1, then the range specified in this register is enabled for decoding to the destination ID specified in ACPIBDID register. This register is Read-Only if the DMIC.SRL field is set.

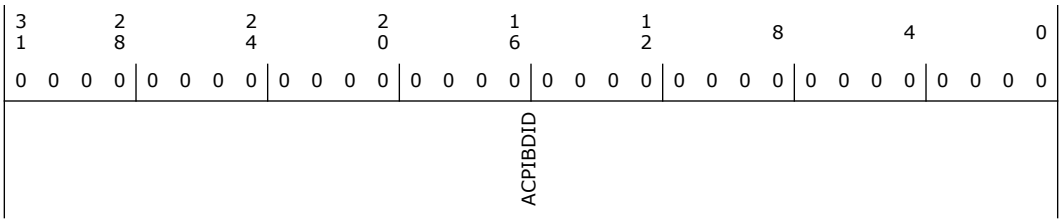
35.2.46 ACPI Base Destination ID (ACPIBDID)—Offset 27B8h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/L	**ACPI Base Destination ID (ACPIBDID):** The destination ID to be used to forward the cycle decoded to hit the ACPI Base Address range. BIOS must program the bits which are not used to zeros. Hardware will ignore the unused bits. This register is Read-Only if the DMIC.SRL field is set.

35.3 DCI PCR Registers Summary

These registers are within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID + Register Offset).

Table 35-3. Summary of DCI PCR Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
4h	7h	DCI Control Register (ECTRL)—Offset 4h	0h

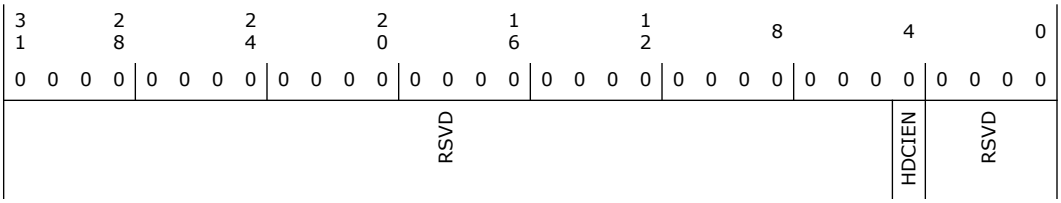
35.3.1 DCI Control Register (ECTRL)—Offset 4h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4	0h RW/L	**Host DCI Enable (HDCIEN):** 0 = Disable DCI 1 = Enable DCI This bit resides in the RTC well and is only reset by RTCRST#. This bit is cleared by writing a 0 to it; writing a 1 has no effect.
3:0	0h RO	Reserved.

35.4 PSF1 PCR Registers Summary

These registers are within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID + Register Offset).

Table 35-4. Summary of PSF1 PCR Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
200h	203h	PCI Base Address (PSF1_T0_SHDW_GBE_REG_BASE)—Offset 200h	0h
21Ch	21Fh	D31:F6 Function Disable (PSF_1_AGNT_T0_SHDW_PCIEN_GBE_RS0_D31_F6_OFFSET2)—Offset 21Ch	0h
300h	303h	PCI Base Address (PSF1_T0_SHDW_CAM_REG_BASE)—Offset 300h	0h
31Ch	31Fh	D20:F3 Function Disable (PSF_1_AGNT_T0_SHDW_PCIEN_CAM_RS0_D20_F3)—Offset 31Ch	0h
338h	33Bh	D20:F3 PCI Configuration Disable (PSF_1_AGNT_T0_SHDW_CFG_DIS_CAM_RS0_D20_F3_OFFSET3)—Offset 338h	0h
41Ch	41Fh	Function Disable (PSF_1_AGNT_T0_SHDW_PCIEN_CSE_RS0_D18_F4_OFFSET4)—Offset 41Ch	0h
61Ch	61Fh	D22:F2 Function Disable (PSF_1_AGNT_T0_SHDW_PCIEN_CSE_RS0_D22_F2)—Offset 61Ch	0h
71Ch	71Fh	D22:F4 Function Disable (PSF_1_AGNT_T0_SHDW_PCIEN_CSE_RS0_D22_F4)—Offset 71Ch	0h
81Ch	81Fh	D22:F1 Function Disable (PSF_1_AGNT_T0_SHDW_PCIEN_CSE_RS0_D22_F1)—Offset 81Ch	0h
A1Ch	A1Fh	D22:F0 Function Disable (PSF_1_AGNT_T0_SHDW_PCIEN_CSE_RS0_D22_F0_OFFSET10)—Offset A1Ch	0h
B1Ch	B1Fh	Offset 0B1Ch: PCI Configuration space enable bits (PSF_1_AGNT_T0_SHDW_PCIEN_PTIO_RS0_D22_F3_OFFSET11)—Offset B1Ch	0h
C1Ch	C1Fh	Offset 0C1Ch: PCI Configuration space enable bits (PSF_1_AGNT_T0_SHDW_PCIEN_PTIO_RS0_D22_F2_OFFSET12)—Offset C1Ch	0h
1000h	1003h	PCI Base Address (PSF1_T0_SHDW_SATA_REG_BASE)—Offset 1000h	0h
101Ch	101Fh	D23:F0 PCI Configuration Space Enable (PSF_1_AGNT_T0_SHDW_PCIEN_VR_RS0_D23_F0_OFFSET16)—Offset 101Ch	0h
203Ch	203Fh	PCIe Port12 PCI Configuration Space Enable (PSF_1_AGNT_T1_SHDW_PCIEN_SPC_RS0_D29_F3)—Offset 203Ch	0h
213Ch	213Fh	PCIe Port11 PCI Configuration Space Enable (PSF_1_AGNT_T1_SHDW_PCIEN_SPC_RS0_D29_F2)—Offset 213Ch	0h
223Ch	223Fh	PCIe Port10 PCI Configuration Space Enable (PSF_1_AGNT_T1_SHDW_PCIEN_SPC_RS0_D29_F1)—Offset 223Ch	0h
233Ch	233Fh	PCIe Port 9 PCI Configuration Space Enable (PSF_1_AGNT_T1_SHDW_PCIEN_SPC_RS0_D29_F0)—Offset 233Ch	0h
243Ch	243Fh	PCIe Port 8 PCI Configuration Space Enable (PSF_1_AGNT_T1_SHDW_PCIEN_SPB_RS0_D28_F7)—Offset 243Ch	0h
253Ch	253Fh	PCIe Port 7 PCI Configuration Space Enable (PSF_1_AGNT_T1_SHDW_PCIEN_SPB_RS0_D28_F6)—Offset 253Ch	0h

Table 35-4. Summary of PSF1 PCR Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
263Ch	263Fh	PCIe Port 6 PCI Configuration Space Enable (PSF_1_AGNT_T1_SHDW_PCIEN_SPB_RS0_D28_F5)—Offset 263Ch	0h
273Ch	273Fh	PCIe Port 5 PCI Configuration Space Enable (PSF_1_AGNT_T1_SHDW_PCIEN_SPB_RS0_D28_F4)—Offset 273Ch	0h
283Ch	283Fh	PCIe Port 4 PCI Configuration Space Enable (PSF_1_AGNT_T1_SHDW_PCIEN_SPA_RS0_D28_F3)—Offset 283Ch	0h
293Ch	293Fh	PCIe Port 3 PCI Configuration Space Enable (PSF_1_AGNT_T1_SHDW_PCIEN_SPA_RS0_D28_F2)—Offset 293Ch	0h
2A3Ch	2A3Fh	PCIe Port 2 PCI Configuration Space Enable (PSF_1_AGNT_T1_SHDW_PCIEN_SPA_RS0_D28_F1)—Offset 2A3Ch	0h
2B3Ch	2B3Fh	PCIe Port 1 PCI Configuration Space Enable (PSF_1_AGNT_T1_SHDW_PCIEN_SPA_RS0_D28_F0)—Offset 2B3Ch	0h
4000h	4003h	PSF Global Configuration (PSF_1_PSF_GLOBAL_CONFIG)—Offset 4000h	0h
4010h	4013h	Rootspace Configuration (PSF_1_ROOTSPACE_CONFIG_RS0)—Offset 4010h	2h
4014h	4017h	Rootspace Configuration (PSF_1_ROOTSPACE_CONFIG_RS1)—Offset 4014h	2h
4018h	401Bh	Offset 4018h: PSF Port Configuration Register (PSF_1_PSF_PORT_CONFIG_PG0_PORT0)—Offset 4018h	0h
403Ch	403Fh	PSF Port Configuration (PSF_1_PSF_PORT_CONFIG_PG1_PORT7)—Offset 403Ch	0h
4050h	4053h	Multicast Control Register (PSF_1_PSF_MC_CONTROL_MCAST0_RS0_EOI)—Offset 4050h	0h
4060h	4063h	Destination ID (PSF_1_PSF_MC_AGENT_MCAST0_RS0_TGT0_EOI)—Offset 4060h	0h
4198h	419Bh	PCI Function Configuration Header (PSF_1_T1_AGENT_FUNCTION_CONFIG_SPA_RS0_D28_F0)—Offset 4198h	1C0h
41CCh	41CFh	Grant Count Reload (PSF_1_DEV_GNTCNT_RELOAD_DGCR0)—Offset 41CCh	4h

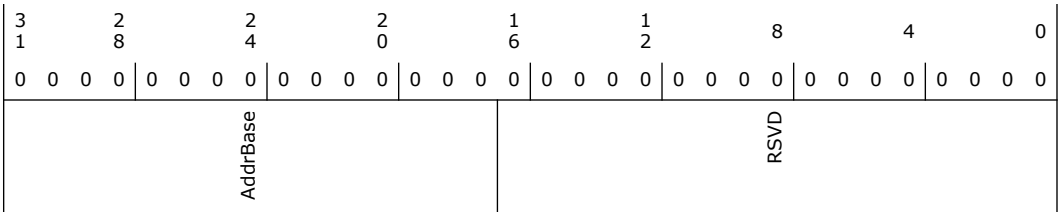
35.4.1 PCI Base Address (PSF1_T0_SHDW_GBE_REG_BASE)—Offset 200h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RW	**GBE PCI BAR (AddrBase)**
16:0	0h RO	Reserved.

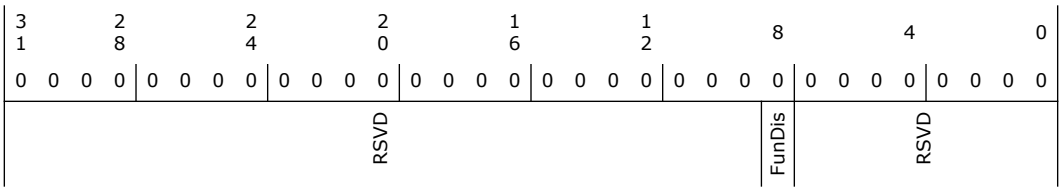
35.4.2 D31:F6 Function Disable (PSF_1_AGNT_T0_SHDW_PCIEN_GBE_RS0_D31_F6_OFFSET2)—Offset 21Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h	**GbE Function Disable (FunDis):** When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be carried out.
7:0	0h RO	Reserved.

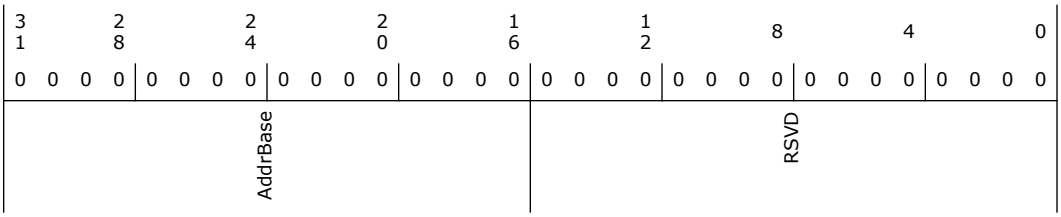
35.4.3 PCI Base Address (PSF1_T0_SHDW_CAM_REG_BASE)—Offset 300h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**CSI2 PCI BAR (AddrBase)**
15:0	0h RO	Reserved.

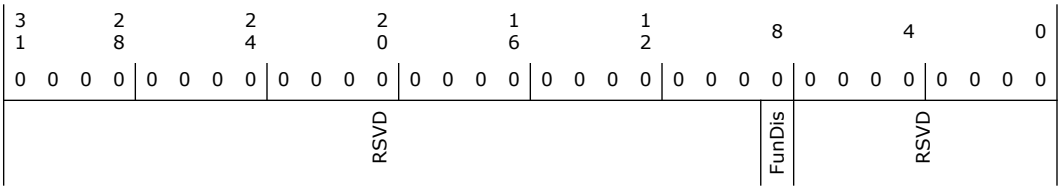
35.4.4 D20:F3 Function Disable (PSF_1_AGNT_T0_SHDW_PCIEN_CAM_RS0_D20_F3)—Offset 31Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h	**Camerera Controller CSI2 Function Disable (FunDis):** When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be carried out.
7:0	0h RO	Reserved.

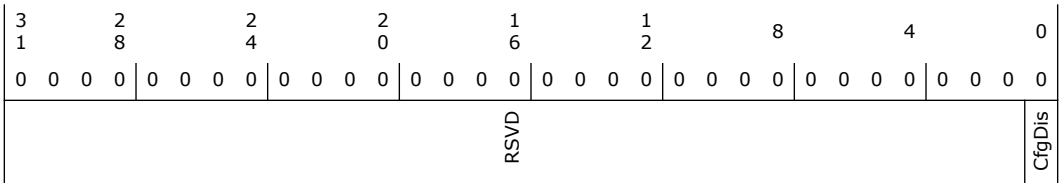
35.4.5 D20:F3 PCI Configuration Disable (PSF_1_AGNT_T0_SHDW_CFG_DIS_CAM_RS0_D20_F3_OFFSET3)—Offset 338h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h	**CfgDis:** If set, the PCI configuration space of this device is switched off, and hidden from the OS.

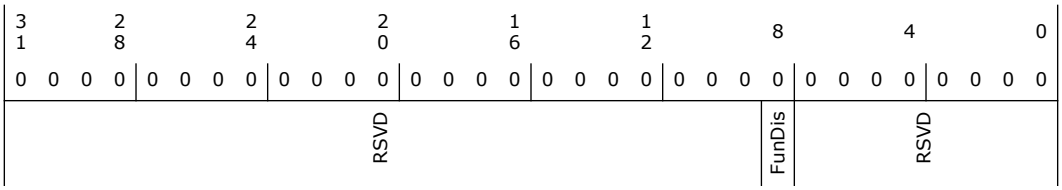
35.4.6 Function Disable (PSF_1_AGNT_T0_SHDW_PCIEN_CSE_RS0_D18_F4_OFFSET4)—Offset 41Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h	**Function Disable (FunDis):** When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be carried out.
7:0	0h RO	Reserved.

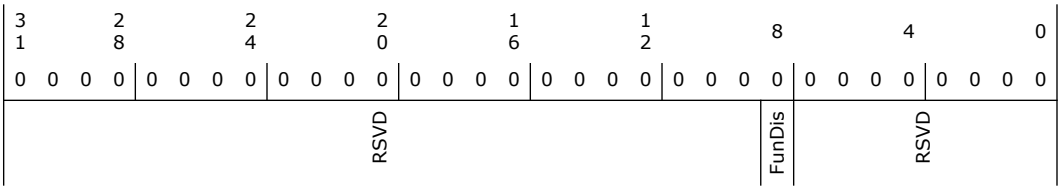
35.4.7 D22:F2 Function Disable (PSF_1_AGNT_T0_SHDW_PCIEN_CSE_RS0_D22_F2)—Offset 61Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h	**IDE-R Function Disable (FunDis):** When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be carried out.
7:0	0h RO	Reserved.

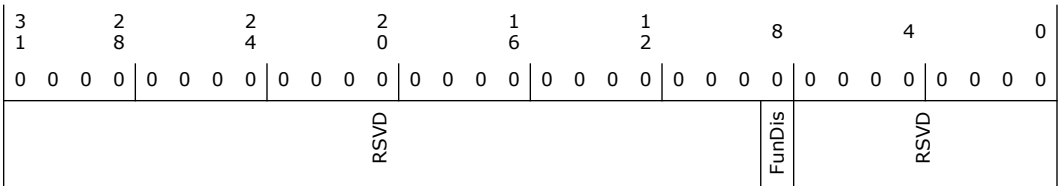
35.4.8 D22:F4 Function Disable (PSF_1_AGNT_T0_SHDW_PCIEN_CSE_RS0_D22_F4)—Offset 71Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h	**Intel(R) MEI #3 Function Disable (FunDis):** When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be carried out.
7:0	0h RO	Reserved.

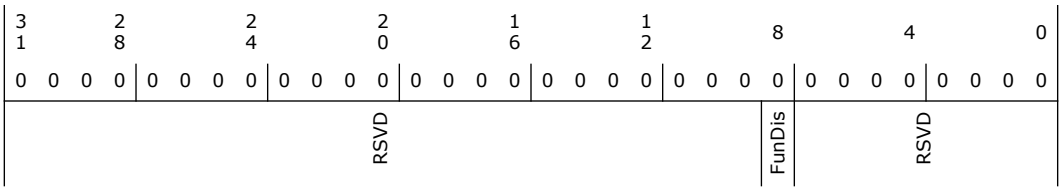
35.4.9 D22:F1 Function Disable (PSF_1_AGNT_T0_SHDW_PCIEN_CSE_RS0_D22_F1)—Offset 81Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h	**Intel(R) MEI #2 Function Disable (FunDis):** When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be carried out.
7:0	0h RO	Reserved.

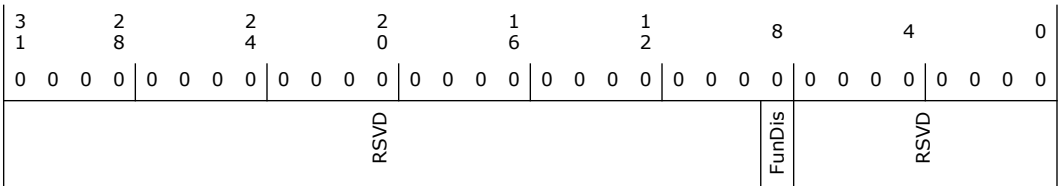
35.4.10 D22:F0 Function Disable (PSF_1_AGNT_T0_SHDW_PCIEN_CSE_RS0_D22_F0_OFFSET10)—Offset A1Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h	**Intel(R) MEI #1 Function Disable (FunDis):** When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be carried out.
7:0	0h RO	Reserved.

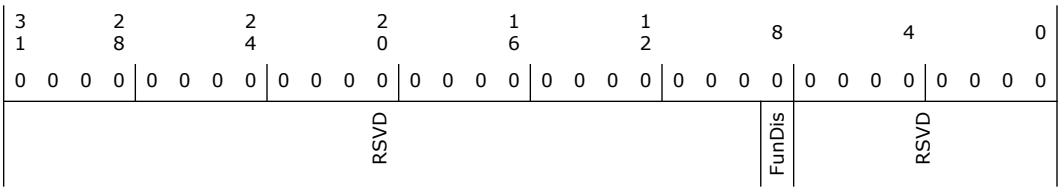
35.4.11 Offset 0B1Ch: PCI Configuration space enable bits (PSF_1_AGNT_T0_SHDW_PCIEN_PTIO_RS0_D22_F3_OFFSET11)—Offset B1Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h	**D22:F3 Function Disable (FunDis):** Default value=0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through IOSF SB interface only.
7:0	0h RO	Reserved.

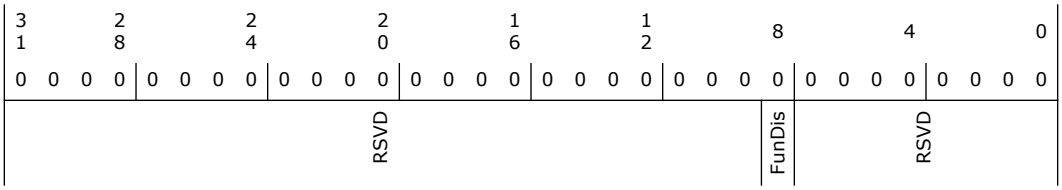
35.4.12 Offset 0C1Ch: PCI Configuration space enable bits (PSF_1_AGNT_T0_SHDW_PCIEN_PTIO_RS0_D22_F2_OFFSET12)—Offset C1Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h	**D22:F2 Function Disable (FunDis):** Default value=0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through IOSF SB interface only.
7:0	0h RO	Reserved.

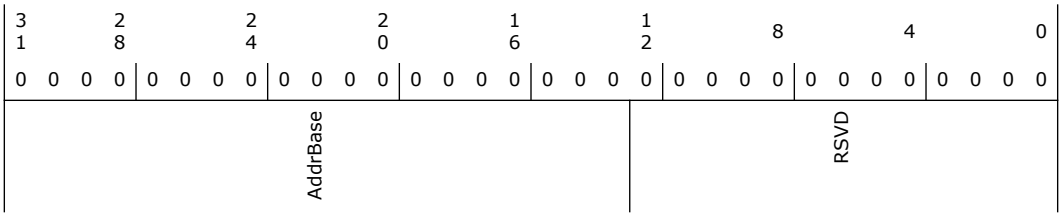
35.4.13 PCI Base Address (PSF1_T0_SHDW_SATA_REG_BASE)—Offset 1000h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RW	**SATA PCI BAR (AddrBase)**
12:0	0h RO	Reserved.

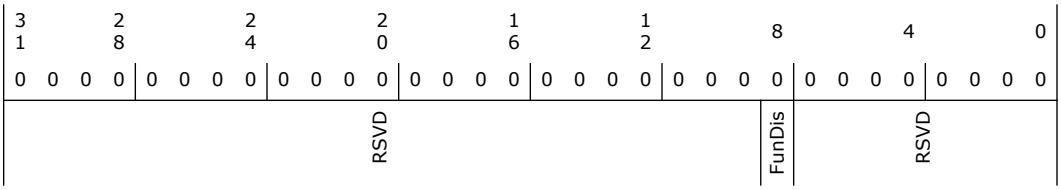
35.4.14 D23:F0 PCI Configuration Space Enable (PSF_1_AGNT_T0_SHDW_PCIEN_VR_RS0_D23_F0_OFFSET16)—Offset 101Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h	**Function Disable (FunDis):** Default value=0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through IOSF SB interface only.
7:0	0h RO	Reserved.

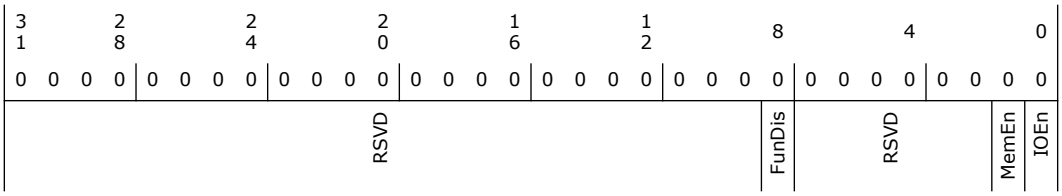
35.4.15 PCIe Port12 PCI Configuration Space Enable (PSF_1_AGNT_T1_SHDW_PCIEN_SPC_RS0_D29_F3)—Offset 203Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h	**Function Disable (FunDis):** When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through IOSF SB interface only.
7:2	0h RO	Reserved.
1	0h RW	**Memory Space Enable (MemEn):** This bit is writable through both IOSF SB interface and through cfgWr transactions on IOSF primary.
0	0h RW	**IO Space Enable (IOEn):** This bit is writable through both IOSF SB interface and through cfgWr transactions on IOSF primary.

35.4.16 PCIe Port11 PCI Configuration Space Enable (PSF_1_AGNT_T1_SHDW_PCIEN_SPC_RS0_D29_F2)—Offset 213Ch

Same definition as PCIe Port 12 PCI Configuration Space Enable register at offset 203Ch.

35.4.17 PCIe Port10 PCI Configuration Space Enable (PSF_1_AGNT_T1_SHDW_PCIEN_SPC_RS0_D29_F1)—Offset 223Ch

Same definition as PCIe Port 12 PCI Configuration Space Enable register at offset 203Ch.

35.4.18 PCIe Port 9 PCI Configuration Space Enable (PSF_1_AGNT_T1_SHDW_PCIEN_SPC_RS0_D29_F0)—Offset 233Ch

Same definition as PCIe Port 12 PCI Configuration Space Enable register at offset 203Ch.

35.4.19 PCIe Port 8 PCI Configuration Space Enable (PSF_1_AGNT_T1_SHDW_PCIEN_SPB_RS0_D28_F7)—Offset 243Ch

Same definition as PCIe Port 12 PCI Configuration Space Enable register at offset 203Ch.

35.4.20 PCIe Port 7 PCI Configuration Space Enable (PSF_1_AGNT_T1_SHDW_PCIEN_SPB_RS0_D28_F6)—Offset 253Ch

Same definition as PCIe Port 12 PCI Configuration Space Enable register at offset 203Ch.

35.4.21 PCIe Port 6 PCI Configuration Space Enable (PSF_1_AGNT_T1_SHDW_PCIEN_SPB_RS0_D28_F5)—Offset 263Ch

Same definition as PCIe Port 12 PCI Configuration Space Enable register at offset 203Ch.

35.4.22 PCIe Port 5 PCI Configuration Space Enable (PSF_1_AGNT_T1_SHDW_PCIEN_SPB_RS0_D28_F4)—Offset 273Ch

Same definition as PCIe Port 12 PCI Configuration Space Enable register at offset 203Ch.

35.4.23 PCIe Port 4 PCI Configuration Space Enable (PSF_1_AGNT_T1_SHDW_PCIEN_SPA_RS0_D28_F3)—Offset 283Ch

Same definition as PCIe Port 12 PCI Configuration Space Enable register at offset 203Ch.

35.4.24 PCIe Port 3 PCI Configuration Space Enable (PSF_1_AGNT_T1_SHDW_PCIEN_SPA_RS0_D28_F2)—Offset 293Ch

Same definition as PCIe Port 12 PCI Configuration Space Enable register at offset 203Ch.

35.4.25 PCIe Port 2 PCI Configuration Space Enable (PSF_1_AGNT_T1_SHDW_PCIEN_SPA_RS0_D28_F1)—Offset 2A3Ch

Same definition as PCIe Port 12 PCI Configuration Space Enable register at offset 203Ch.

35.4.26 PCIe Port 1 PCI Configuration Space Enable (PSF_1_AGNT_T1_SHDW_PCIEN_SPA_RS0_D28_F0)—Offset 2B3Ch

Same definition as PCIe Port 12 PCI Configuration Space Enable register at offset 203Ch.

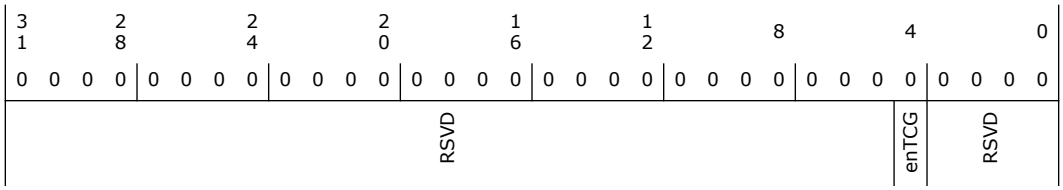
35.4.27 PSF Global Configuration (PSF_1_PSF_GLOBAL_CONFIG)—Offset 4000h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4	0h	**enTCG:** If set, PSF will use its clkreq/ack signals to request and maintain a clock for a transaction. If set to 0, PSF will permanently assert all clkreq and signals.
3:0	0h RO	Reserved.

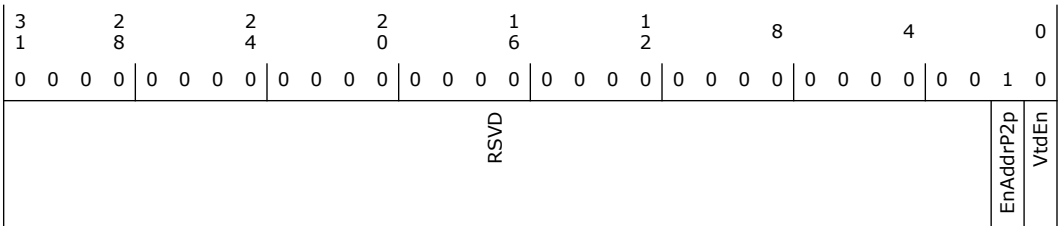
35.4.28 Rootspace Configuration (PSF_1_ROOTSPACE_CONFIG_RS0)—Offset 4010h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 2h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1	1h	**EnAddrP2p:** If set, address-based p2p transactions are allowed for this root space.
0	0h RW	**Vtd Enable (VtdEn):** If set Intel Virtualization Technology for Directed I/O is enabled for this root space. This bit should reflect the system-wide vt-d setting, and is typically maintained by BIOS.

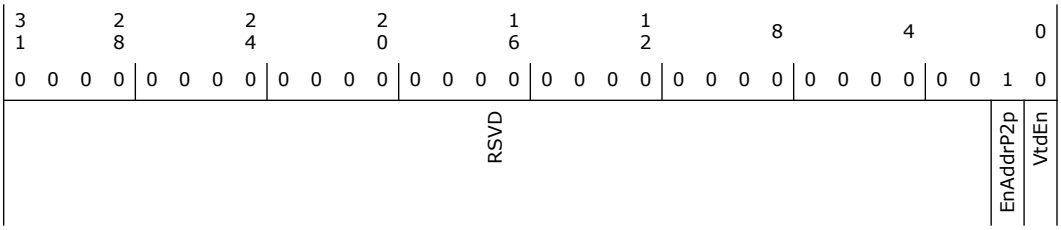
35.4.29 Rootspace Configuration (PSF_1_ROOTSPACE_CONFIG_RS1)—Offset 4014h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 2h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1	1h	**EnAddrP2p:** Default value=1, If set, address-based p2p transactions are allowed for this root space.
0	0h	**VtdEn:** Default value=0, If set Intel Virtualization Technology for Directed I/O is enabled for this root space. This bit should reflect the system-wide vt-d setting, and is typically maintained by BIOS

35.4.30 Offset 4018h: PSF Port Configuration Register (PSF_1_PSF_PORT_CONFIG_PG0_PORT0)—Offset 4018h

BIOS may program this register.

35.4.31 PSF Port Configuration (PSF_1_PSF_PORT_CONFIG_PG1_PORT7)—Offset 403Ch

BIOS may program this register.

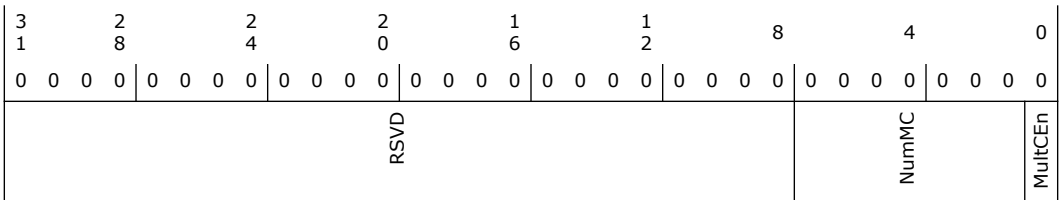
35.4.32 Multicast Control Register (PSF_1_PSF_MC_CONTROL_MCAST0_RS0_EOI)—Offset 4050h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:1	0h	**Multicast (NumMC):** Number of multicast Agents on this root-space on the PSF segment.
0	0h	**Multicast Enable (MultCEn):** Multicast Enable. If set Multicast transactions are supported on this root-space.

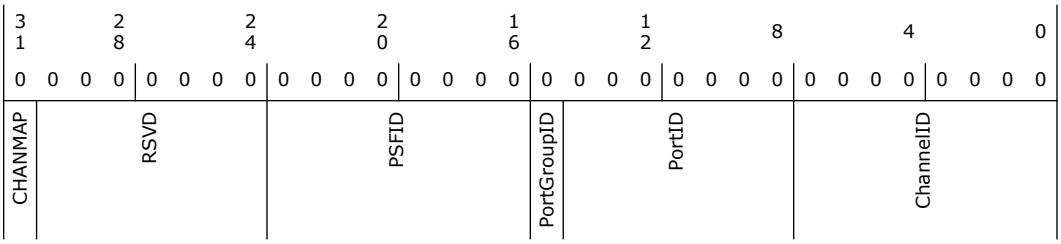
35.4.33 Destination ID (PSF_1_PSF_MC_AGENT_MCAST0_RS0_TGT0_EOI)—Offset 4060h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31	0h	**Channel ID Map (CHANMAP):** If this bit is set, the ChannelID field is ignored and is looked up in the CHANMAP register set that belongs to PortGroupID:PortID
30:24	0h RO	Reserved.
23:16	0h	**PSF ID (PSFID):** Default value=0,
15	0h	**Port Group ID (PortGroupID):** Default value=0
14:8	0h	**Port ID (PortID):** Default value=0, Since 1'b0 indicates source-decode, the port ID needs to be larger than 0
7:0	0h	**Channel ID (ChannelID):** Default value=0

35.4.34 PCI Function Configuration Header (PSF_1_T1_AGENT_FUNCTION_CONFIG_SPA_RS0_D28_F0)—Offset 4198h

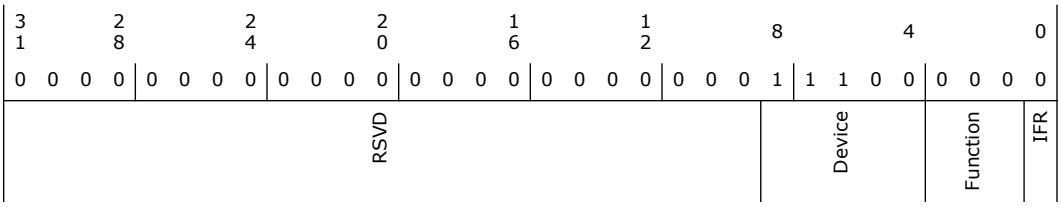
This register controls the PCI configuration header of a PCI function.

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 1C0h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8:4	1Ch	**Device:** Default value=28, Device number of the PCI function. This field resets to the device number as configured at compile time
3:1	0h	**Function:** Default value=0, Function number of the PCI function. This field resets to the function number as configured at compile time
0	0h	**IFR:** Default value=0, If written as a '1', all shadow registers associated with this function will be reset. This bit self-clears after the reset sequence has finished. This bit always reads as 0.

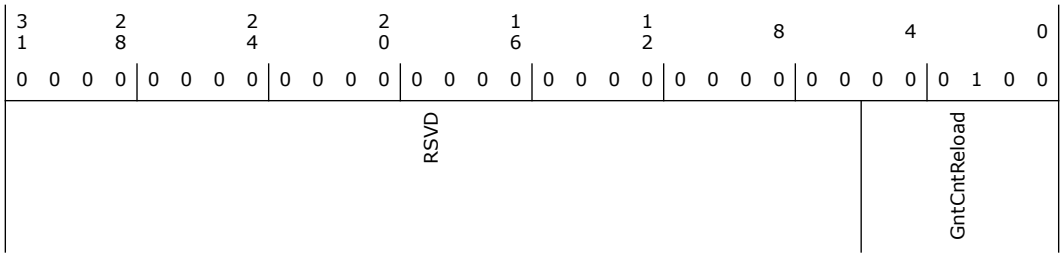
35.4.35 Grant Count Reload (PSF_1_DEV_GNTCNT_RELOAD_DGCR0)—Offset 41CCh

Access Method

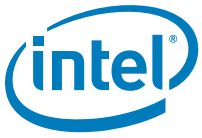
Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 4h



Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	Reserved.
5:0	4h	**GntCntReload:** Default value=4, Value that is used to reload an arbitration grant-counter for a transaction or decode requester. The value 0 is reserved and should not be used. These bits are not synchronized, so they should only be written when there are no IOSF Primary transactions ongoing on PSF. This field width is variable, and dependent on PSF configuration parameters.



35.5 PSF2 PCR Registers Summary

These registers are within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID + Register Offset).

Table 35-5. Summary of PSF2 PCR Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
11Ch	11Fh	D20:F2 Function Disable (PSF_2_AGNT_T0_SHDW_PCIEN_TRH_RS0_D20_F2_OFFSET1)—Offset 11Ch	0h
138h	13Bh	D20:F2 PCI Configuration Disable (PSF_2_AGNT_T0_SHDW_CFG_DIS_TRH_RS0_D20_F2_OFFSET1)—Offset 138h	0h
21Ch	21Fh	D30:F7 Function Disable (PSF_2_AGNT_T0_SHDW_PCIEN_SCC_RS0_D30_F7_OFFSET2)—Offset 21Ch	0h
300h	303h	PCI Base Address (PSF2_T0_SHDW_SDCARD_REG_BASE)—Offset 300h	0h
31Ch	31Fh	D30:F6 Function Disable (PSF_2_AGNT_T0_SHDW_PCIEN_SCC_RS0_D30_F6_OFFSET3)—Offset 31Ch	0h
41Ch	41Fh	D30:F5 Function Disable (PSF_2_AGNT_T0_SHDW_PCIEN_SCC_RS0_D30_F5_OFFSET4)—Offset 41Ch	0h
500h	503h	PCI Base Address (PSF2_T0_SHDW_EMMC_REG_BASE)—Offset 500h	0h
51Ch	51Fh	D30:F4 Function Disable (PSF_2_AGNT_T0_SHDW_PCIEN_SCC_RS0_D30_F4_OFFSET5)—Offset 51Ch	0h
600h	603h	PCI Base Address (PSF2_T0_SHDW_OTG_REG_BASE)—Offset 600h	0h
61Ch	61Fh	D20:F1 Function Disable (PSF_2_AGNT_T0_SHDW_PCIEN_OTG_RS0_D20_F1_OFFSET6)—Offset 61Ch	0h
71Ch	71Fh	D20:F0 Function Disable (PSF_2_AGNT_T0_SHDW_PCIEN_XHCI_RS0_D20_F0_OFFSET7)—Offset 71Ch	0h
4000h	4003h	PSF Global Configuration (PSF_2_PSF_GLOBAL_CONFIG)—Offset 4000h	0h
4010h	4013h	Rootspace Configuration (PSF_2_ROOTSPACE_CONFIG_RS0)—Offset 4010h	2h
4014h	4017h	Rootspace Configuration (PSF_2_ROOTSPACE_CONFIG_RS1)—Offset 4014h	2h

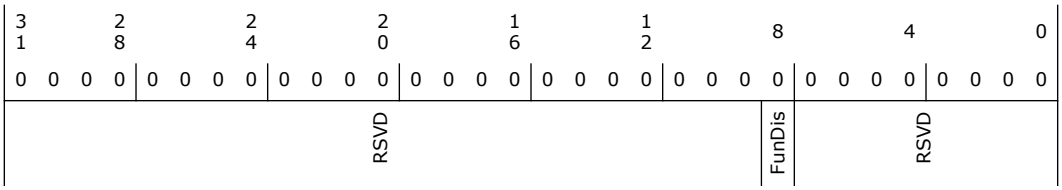
35.5.1 D20:F2 Function Disable (PSF_2_AGNT_T0_SHDW_PCIEN_TRH_RS0_D20_F2_OFFSET1)—Offset 11Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h	**Thermal Reporting Function Disable (FunDis):** When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be carried out.
7:0	0h RO	Reserved.

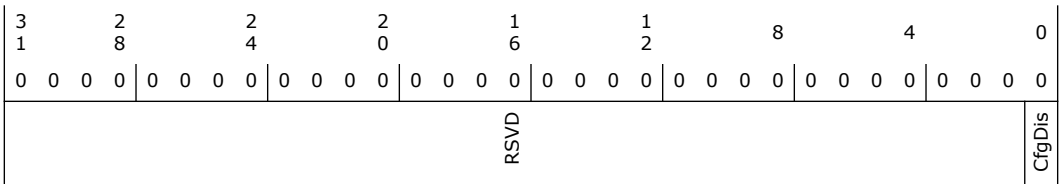
35.5.2 D20:F2 PCI Configuration Disable (PSF_2_AGNT_T0_SHDW_CFG_DIS_TRH_RS0_D20_F2_OFFSET1)—Offset 138h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h	**CfgDis:** Default value=0, If set, the PCI configuration space of this device is switched off, and hidden from the OS. This bit is writable through IOSF SB interface only.

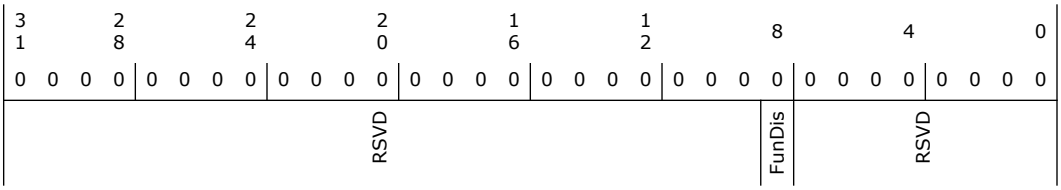
35.5.3 D30:F7 Function Disable (PSF_2_AGNT_T0_SHDW_PCIEN_SCC_RS0_D30_F7_OFFSET2)—Offset 21Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h	**FunDis:** When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be carried out.
7:0	0h RO	Reserved.

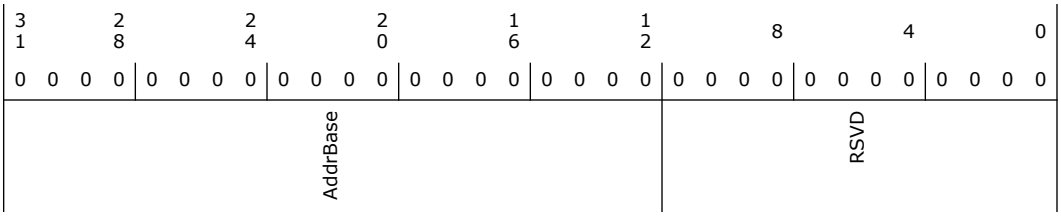
35.5.4 PCI Base Address (PSF2_T0_SHDW_SDCARD_REG_BASE)—Offset 300h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW	**SDXC PCI BAR (AddrBase)**
11:0	0h RO	Reserved.

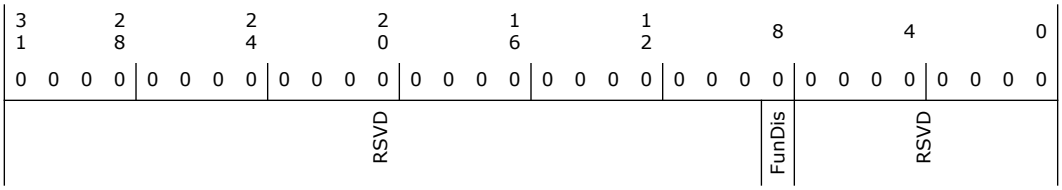
35.5.5 D30:F6 Function Disable (PSF_2_AGNT_T0_SHDW_PCIEN_SCC_RS0_D30_F6_OFFSET3)—Offset 31Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h	**SDXC Function Disable (FunDis):** When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be carried out.
7:0	0h RO	Reserved.

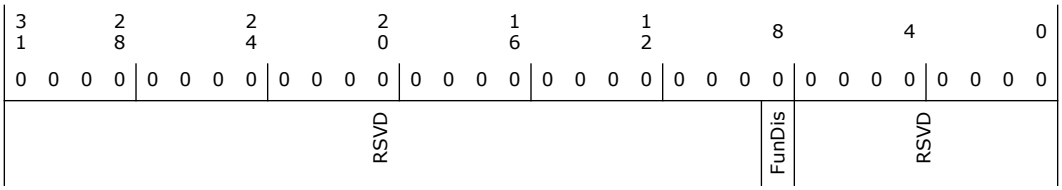
35.5.6 D30:F5 Function Disable (PSF_2_AGNT_T0_SHDW_PCIEN_SCC_RS0_D30_F5_OFFSET4)—Offset 41Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h	**SDIO Function Disable (FunDis):** When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be carried out.
7:0	0h RO	Reserved.

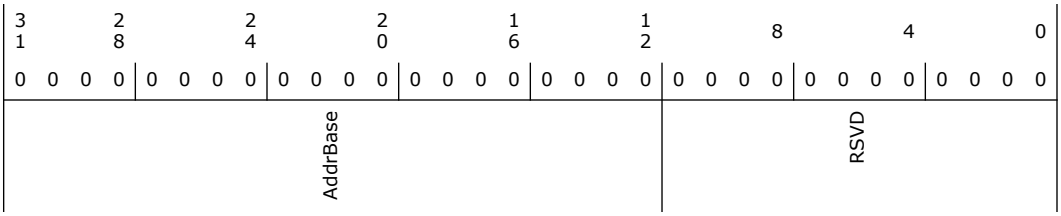
35.5.7 PCI Base Address (PSF2_T0_SHDW_EMMC_REG_BASE)—Offset 500h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW	**eMMC PCI BAR (AddrBase)**
11:0	0h RO	Reserved.

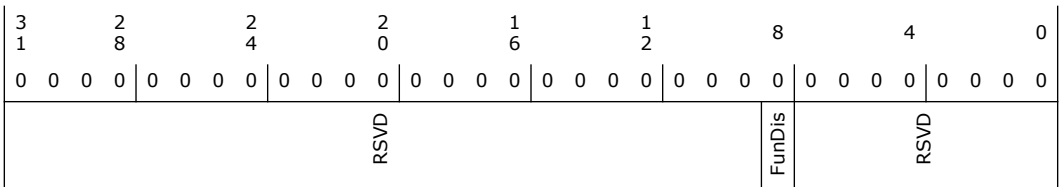
35.5.8 D30:F4 Function Disable (PSF_2_AGNT_T0_SHDW_PCIEN_SCC_RS0_D30_F4_OFFSET5)—Offset 51Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h	**eMMC Function Disable (FunDis):** When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be carried out.
7:0	0h RO	Reserved.

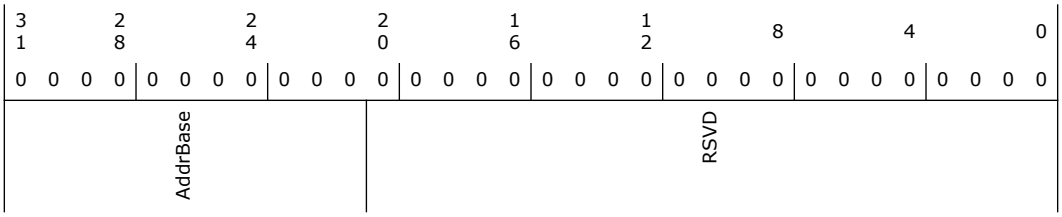
35.5.9 PCI Base Address (PSF2_T0_SHDW_OTG_REG_BASE)—Offset 600h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RW	**xDCI PCI BAR (AddrBase)**
20:0	0h RO	Reserved.

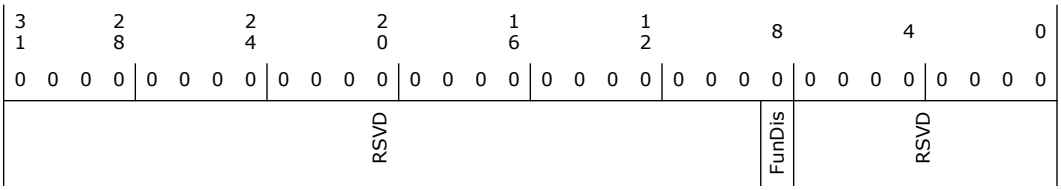
35.5.10 D20:F1 Function Disable (PSF_2_AGNT_T0_SHDW_PCIEN_OTG_RS0_D20_F1_OFFSET6)—Offset 61Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h	**USB Dual Role (OTG) Function Disable (FunDis):** When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be carried out.
7:0	0h RO	Reserved.

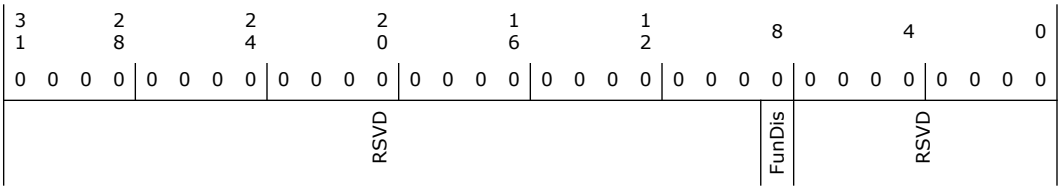
35.5.11 D20:F0 Function Disable (PSF_2_AGNT_T0_SHDW_PCIEN_XHCI_RS0_D20_F0_OFFSET7)—Offset 71Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h	**xHCI Function Disable (FunDis):** When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be carried out.
7:0	0h RO	Reserved.

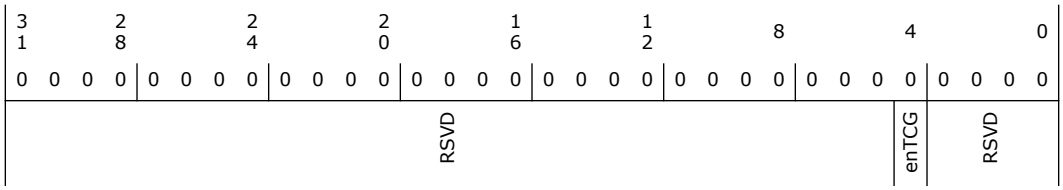
35.5.12 PSF Global Configuration (PSF_2_PSF_GLOBAL_CONFIG)—Offset 4000h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4	0h	**enTCG:** If set, PSF will use its clkreq/ack signals to request and maintain a clock for a transaction. If set to 0, PSF will permanently assert all clkreq and signals.
3:0	0h RO	Reserved.

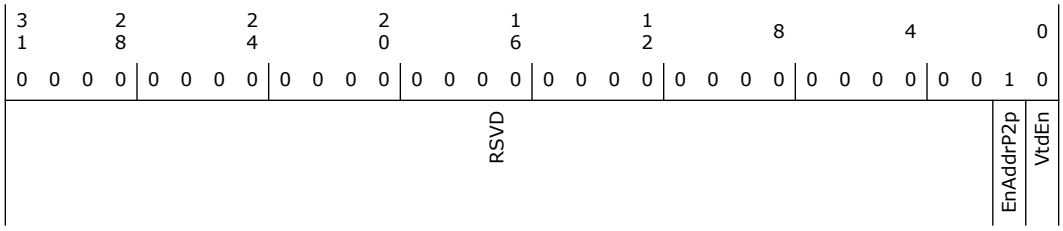
35.5.13 Rootspace Configuration (PSF_2_ROOTSPACE_CONFIG_RS0)—Offset 4010h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 2h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1	1h	**Address Enable (EnAddrP2p):** Default value=1, If set, address-based p2p transactions are allowed for this root space.
0	0h	**VTd Enable (VtdEn):** Default value=0, If set Intel Virtualization Technology for Directed I/O is enabled for this root space. This bit should reflect the system-wide vt-d setting, and is typically maintained by BIOS

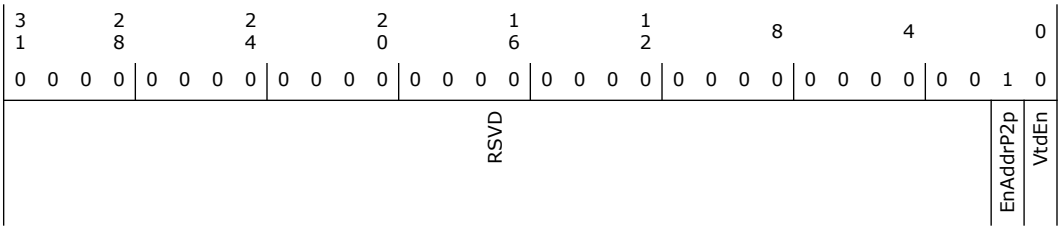
35.5.14 Rootspace Configuration (PSF_2_ROOTSPACE_CONFIG_RS1)—Offset 4014h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 2h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1	1h	**EnAddrP2p:** Default value=1, If set, address-based p2p transactions are allowed for this root space.
0	0h	**VtdEn:** Default value=0, If set Intel Virtualization Technology for Directed I/O is enabled for this root space. This bit should reflect the system-wide vt-d setting, and is typically maintained by BIOS

35.6 PSF3 PCR Registers Summary

These registers are within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID + Register Offset).

Table 35-6. Summary of PSF3 PCR Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
200h	203h	PCI Base Address (PSF3_T0_SHDW_TRACE_HUB_ACPI_REG_BASE)—Offset 200h	0h
21Ch	21Fh	Offset 021Ch: PCI Configuration space enable bits (PSF_3_AGNT_T0_SHDW_PCIEN_NPK_RS0_D20_F4_OFFSET2)—Offset 21Ch	0h
238h	23Bh	Intel Trace Hub PCI Configuration Disable (PSF_3_AGNT_T0_SHDW_CFG_DIS_NPK_RS0_D20_F4_OFFSET2)—Offset 238h	0h
300h	303h	PCI Base Address (PSF3_T0_SHDW_TRACE_HUB_REG_BASE)—Offset 300h	0h
31Ch	31Fh	D31:F7 PCI Configuration Space Enable (PSF_3_AGNT_T0_SHDW_PCIEN_NPK_RS0_D31_F7_OFFSET3)—Offset 31Ch	0h
338h	33Bh	PCI Configuration Disable (PSF_3_AGNT_T0_SHDW_CFG_DIS_NPK_RS0_D31_F7_OFFSET3)—Offset 338h	0h
51Ch	51Fh	PCI Configuration Space Enable (PSF_3_AGNT_T0_SHDW_PCIEN_SMB_RS0_D31_F4_OFFSET5)—Offset 51Ch	0h
538h	53Bh	PCI Configuration Disable (PSF_3_AGNT_T0_SHDW_CFG_DIS_SMB_RS0_D31_F4_OFFSET5)—Offset 538h	0h
800h	803h	PCI Base Address (PSF3_T0_SHDW_ISH_REG_BASE)—Offset 800h	0h
81Ch	81Fh	D19:F0 Function Disable (PSF_3_AGNT_T0_SHDW_PCIEN_ISH_RS0_D19_F0_OFFSET8)—Offset 81Ch	0h
900h	903h	PCI Base Address (PSF3_T0_SHDW_I2C4_REG_BASE)—Offset 900h	0h
91Ch	91Fh	D25:F2 Function Disable (SF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D25_F2_OFFSET9)—Offset 91Ch	0h
938h	93Bh	Offset 0938h: PCI Configuration Disable (PSF_3_AGNT_T0_SHDW_CFG_DIS_LPSS_RS0_D25_F2_OFFSET9)—Offset 938h	0h
A00h	A03h	PCI Base Address (PSF3_T0_SHDW_GSPI1_REG_BASE)—Offset A00h	0h
A1Ch	A1Fh	D30:F3 Function Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D30_F3_OFFSET10)—Offset A1Ch	0h
A38h	A3Bh	Offset 0A38h: PCI Configuration Disable (PSF_3_AGNT_T0_SHDW_CFG_DIS_LPSS_RS0_D30_F3_OFFSET10)—Offset A38h	0h
B00h	B03h	PCI Base Address (PSF3_T0_SHDW_SPI0_REG_BASE)—Offset B00h	0h
B1Ch	B1Fh	Function Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D30_F2_OFFSET11)—Offset B1Ch	0h

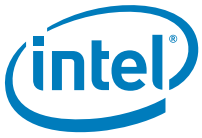


Table 35-6. Summary of PSF3 PCR Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
B38h	B3Bh	Offset 0B38h: PCI Configuration Disable (PSF_3_AGNT_T0_SHDW_CFG_DIS_LPSS_RS0_D30_F2_OFFSET11)—Offset B38h	0h
C00h	C03h	PCI Base Address (PSF3_T0_SHDW_UART1_REG_BASE)—Offset C00h	0h
C1Ch	C1Fh	D30:F1 Function Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D30_F1_OFFSET12)—Offset C1Ch	0h
C38h	C3Bh	Offset 0C38h: PCI Configuration Disable (PSF_3_AGNT_T0_SHDW_CFG_DIS_LPSS_RS0_D30_F1_OFFSET12)—Offset C38h	0h
D00h	D03h	PCI Base Address (PSF3_T0_SHDW_UART0_REG_BASE)—Offset D00h	0h
D1Ch	D1Fh	D30:F0 Function Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D30_F0_OFFSET13)—Offset D1Ch	0h
D38h	D3Bh	Offset 0D38h: PCI Configuration Disable (PSF_3_AGNT_T0_SHDW_CFG_DIS_LPSS_RS0_D30_F0_OFFSET13)—Offset D38h	0h
E00h	E03h	PCI Base Address (PSF3_T0_SHDW_I2C5_REG_BASE)—Offset E00h	0h
E1Ch	E1Fh	D25:F1 Function Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D25_F1_OFFSET14)—Offset E1Ch	0h
E38h	E3Bh	Offset 0E38h: PCI Configuration Disable (PSF_3_AGNT_T0_SHDW_CFG_DIS_LPSS_RS0_D25_F1_OFFSET14)—Offset E38h	0h
F00h	F03h	PCI Base Address (PSF3_T0_SHDW_UART2_REG_BASE)—Offset F00h	0h
F1Ch	F1Fh	D25:F0 Function Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D25_F0_OFFSET15)—Offset F1Ch	0h
F38h	F3Bh	Offset 0F38h: PCI Configuration Disable (PSF_3_AGNT_T0_SHDW_CFG_DIS_LPSS_RS0_D25_F0_OFFSET15)—Offset F38h	0h
1000h	1003h	PCI Base Address (PSF3_T0_SHDW_I2C3_REG_BASE)—Offset 1000h	0h
101Ch	101Fh	D21:F3 Function Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D21_F3_OFFSET16)—Offset 101Ch	0h
1038h	103Bh	Offset 1038h: PCI Configuration Disable (PSF_3_AGNT_T0_SHDW_CFG_DIS_LPSS_RS0_D21_F3_OFFSET16)—Offset 1038h	0h
1100h	1103h	PCI Base Address (PSF3_T0_SHDW_I2C2_REG_BASE)—Offset 1100h	0h
111Ch	111Fh	D21:F2 Function Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D21_F2_OFFSET17)—Offset 111Ch	0h
1138h	113Bh	Offset 1138h: PCI Configuration Disable (PSF_3_AGNT_T0_SHDW_CFG_DIS_LPSS_RS0_D21_F2_OFFSET17)—Offset 1138h	0h
1200h	1203h	PCI Base Address (PSF3_T0_SHDW_I2C1_REG_BASE)—Offset 1200h	0h
121Ch	121Fh	D21:F1 Function Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D21_F1_OFFSET18)—Offset 121Ch	0h
1238h	123Bh	Offset 1238h: PCI Configuration Disable (PSF_3_AGNT_T0_SHDW_CFG_DIS_LPSS_RS0_D21_F1_OFFSET18)—Offset 1238h	0h
1300h	1303h	PCI Base Address (PSF3_T0_SHDW_I2C0_REG_BASE)—Offset 1300h	0h

Table 35-6. Summary of PSF3 PCR Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
131Ch	131Fh	D21:F0 Function Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D21_F0_OFFSET19)—Offset 131Ch	0h
1338h	133Bh	Offset 1338h: PCI Configuration Disable (PSF_3_AGNT_T0_SHDW_CFG_DIS_LPSS_RS0_D21_F0_OFFSET19)—Offset 1338h	0h
171Ch	171Fh	Function Disable (PSF_3_AGNT_T0_SHDW_PCIEN_SPI_RS0_D31_F0_OFFSET23)—Offset 171Ch	0h
1900h	1903h	PCI Base Address (PSF3_T0_SHDW_AUD_REG_BASE)—Offset 1900h	0h
191Ch	191Fh	PCI Configuration Space Enable (PSF_3_AGNT_T0_SHDW_PCIEN_AUD_RS0_D31_F3_OFFSET25)—Offset 191Ch	0h
4000h	4003h	PSF Global Configuration (PSF_3_PSF_GLOBAL_CONFIG)—Offset 4000h	0h
4010h	4013h	Root Space Config (PSF_3_ROOTSPACE_CONFIG_RS0)—Offset 4010h	2h
4014h	4017h	Rootspace Configuration (PSF_3_ROOTSPACE_CONFIG_RS1)—Offset 4014h	2h
404Ch	404Fh	Multicast Control (PSF_3_PSF_MC_CONTROL_MCAST0_RS0_EOI)—Offset 404Ch	0h
4054h	4057h	Destination ID (PSF_3_PSF_MC_AGENT_MCAST0_RS0_TGT0_EOI)—Offset 4054h	0h

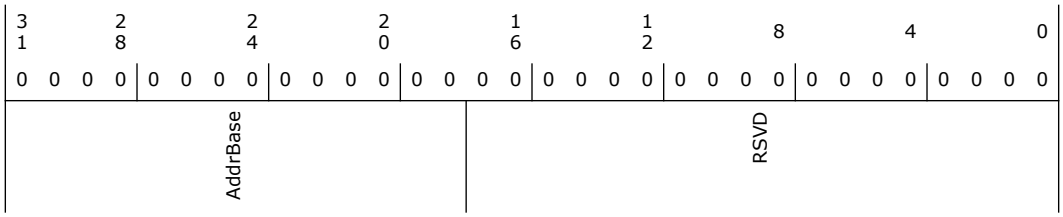
35.6.1 PCI Base Address (PSF3_T0_SHDW_TRACE_HUB_ACPI_REG_BASE)—Offset 200h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RW	**Trace Hub PCI BAR (AddrBase)**
17:0	0h RO	Reserved.

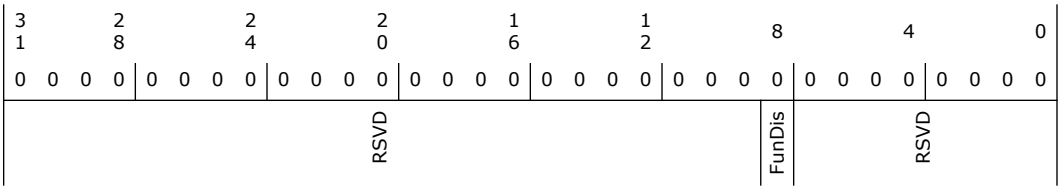
35.6.2 Offset 021Ch: PCI Configuration space enable bits (PSF_3_AGNT_T0_SHDW_PCIEN_NPK_RS0_D20_F4_OFFSET2)—Offset 21Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h	**D20:F4 Function Disable (FunDis):** Default value=0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through IOSF SB interface only.
7:0	0h RO	Reserved.

35.6.3 Intel Trace Hub PCI Configuration Disable (PSF_3_AGNT_T0_SHDW_CFG_DIS_NPK_RS0_D20_F4_OFFSET2)—Offset 238h

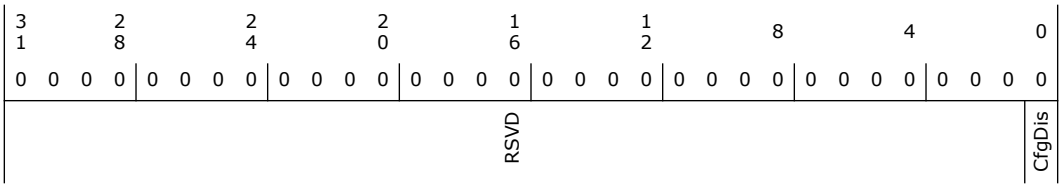
If set, this bit disables the shadowed PCI configuration header of the device. When a PCI configuration header is disabled, cfgWr transactions are no longer shadowed, and whatever the current contents of the address resources (BAR[0..1]) and requester ID (B:D:F) becomes the fixed location of the device in the address space. With its PCI configuration header disabled, the device effectively becomes an ACPI device, with fixed address ranges and requester ID.

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h	**CfgDis:** Default value=0, If set, the PCI configuration space of this device is switched off, and hidden from the OS. This bit is writable through IOSF SB interface only.

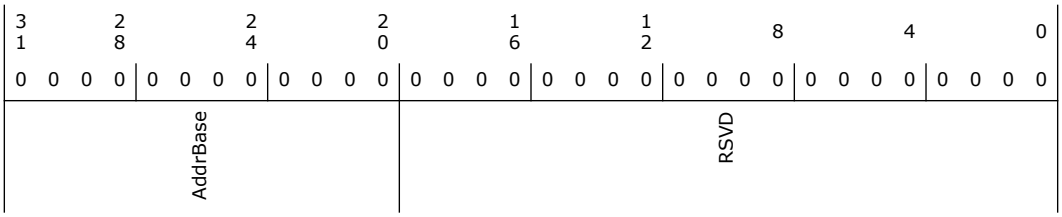
35.6.4 PCI Base Address (PSF3_T0_SHDW_TRACE_HUB_REG_BASE)—Offset 300h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**Trace Hub PCI BAR (AddrBase)**
19:0	0h RO	Reserved.

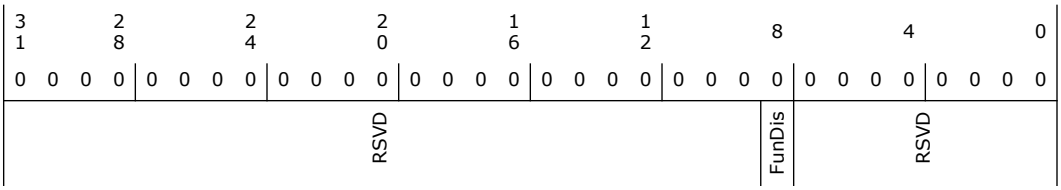
35.6.5 D31:F7 PCI Configuration Space Enable (PSF_3_AGNT_T0_SHDW_PCIEN_NPK_RS0_D31_F7_OFFSET3)—Offset 31Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h	**Function Disable (FunDis):** Default value=0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through IOSF SB interface only.
7:0	0h RO	Reserved.

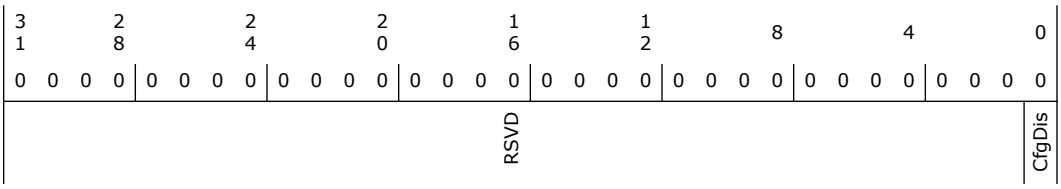
35.6.6 PCI Configuration Disable (PSF_3_AGNT_T0_SHDW_CFG_DIS_NPK_RS0_D31_F7_OFFSET3)—Offset 338h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h	**CfgDis:** Default value=0, If set, the PCI configuration space of this device is switched off, and hidden from the OS. This bit is writable through IOSF SB interface only.

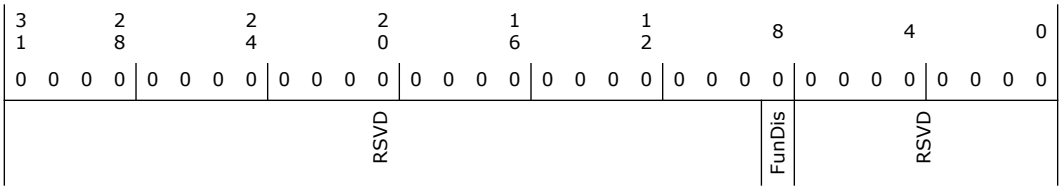
35.6.7 PCI Configuration Space Enable (PSF_3_AGNT_T0_SHDW_PCIEN_SMB_RS0_D31_F4_OFFSET5)—Offset 51Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h	**FunDis:** Default value=0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through IOSF SB interface only.
7:0	0h RO	Reserved.

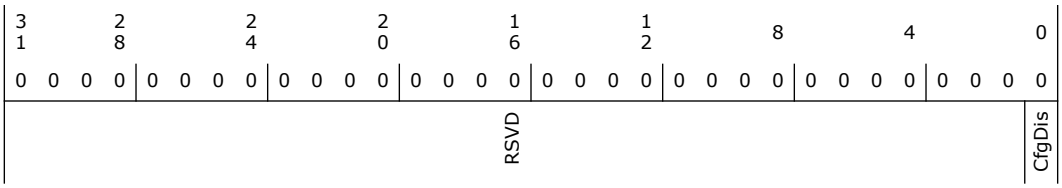
35.6.8 PCI Configuration Disable (PSF_3_AGNT_T0_SHDW_CFG_DIS_SMB_RS0_D31_F4_OFFSET5)—Offset 538h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h	**CfgDis:** Default value=0, If set, the PCI configuration space of this device is switched off, and hidden from the OS. This bit is writable through IOSF SB interface only.

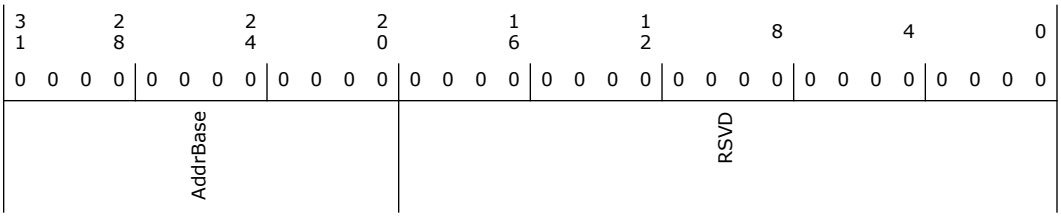
35.6.9 PCI Base Address (PSF3_T0_SHDW_ISH_REG_BASE)—Offset 800h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**ISH PCI BAR (AddrBase)**
19:0	0h RO	Reserved.

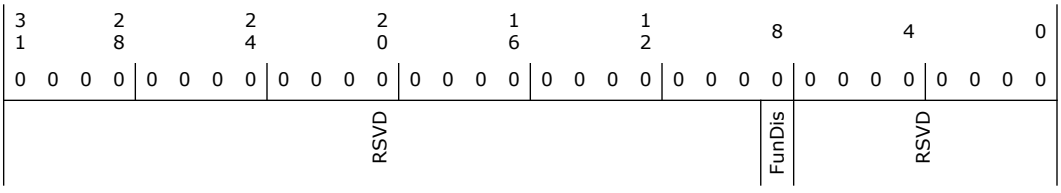
35.6.10 D19:F0 Function Disable (PSF_3_AGNT_T0_SHDW_PCIEN_ISH_RS0_D19_F0_OFFSET8)—Offset 81Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h	**ISH Function Disable (FunDis):** When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be carried out.
7:0	0h RO	Reserved.

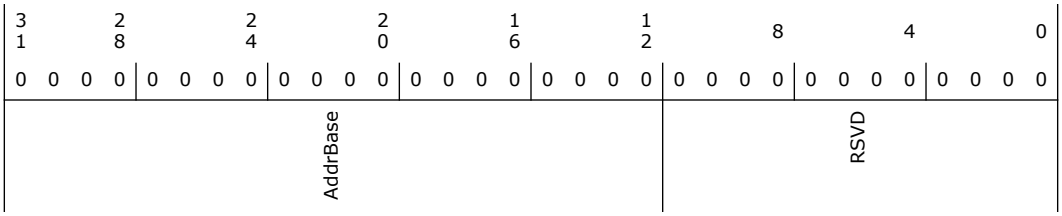
35.6.11 PCI Base Address (PSF3_T0_SHDW_I2C4_REG_BASE)—Offset 900h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW	**I2C4 PCI BAR (AddrBase)**
11:0	0h RO	Reserved.

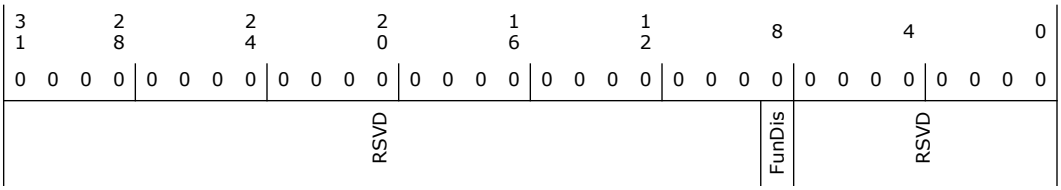
35.6.12 D25:F2 Function Disable (SF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D25_F2_OFFSET9)—Offset 91Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h	**I2C4 Function Disable (FunDis):** When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be carried out
7:0	0h RO	Reserved.

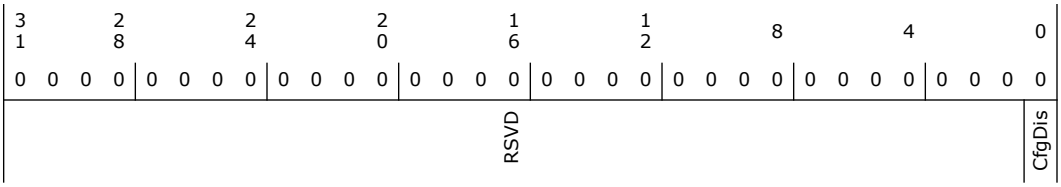
35.6.13 Offset 0938h: PCI Configuration Disable (PSF_3_AGNT_T0_SHDW_CFG_DIS_LPSS_RS0_D25_F2_OFFSET9)—Offset 938h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h	**PCI Config Disable (CfgDis):** Default value=0, If set, the PCI configuration space of this device is switched off, and hidden from the OS. This bit is writable through IOSF SB interface only.

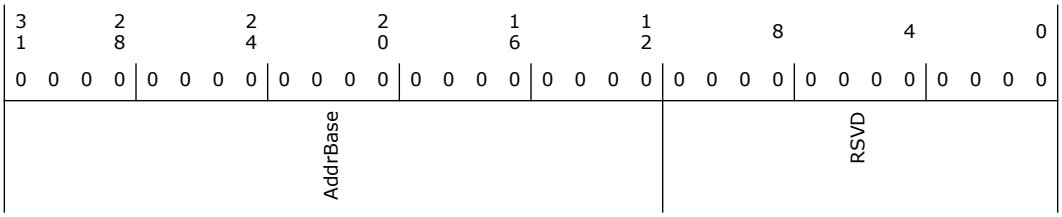
35.6.14 PCI Base Address (PSF3_T0_SHDW_GSPI1_REG_BASE)—Offset A00h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW	**GSPI1 PCI BAR (AddrBase)**
11:0	0h RO	Reserved.

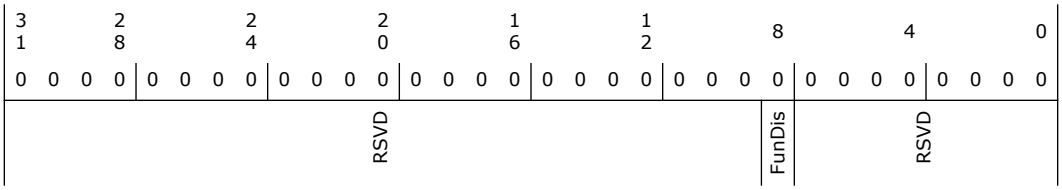
35.6.15 D30:F3 Function Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D30_F3_OFFSET10)—Offset A1Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h	**SPI1 Function Disable (FunDis):** When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be carried out.
7:0	0h RO	Reserved.

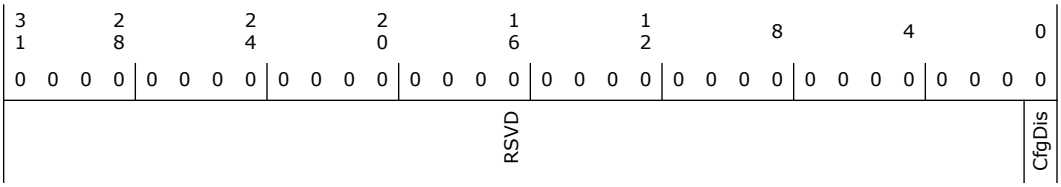
35.6.16 Offset 0A38h: PCI Configuration Disable (PSF_3_AGNT_T0_SHDW_CFG_DIS_LPSS_RS0_D30_F3_OFFSET10)—Offset A38h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h	**PCI Config Disable (CfgDis):** Default value=0, If set, the PCI configuration space of this device is switched off, and hidden from the OS. This bit is writable through IOSF SB interface only.

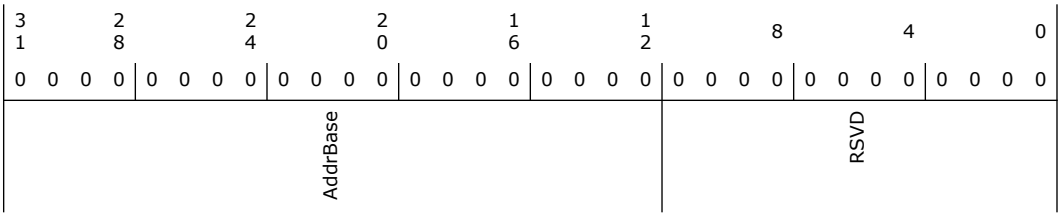
35.6.17 PCI Base Address (PSF3_T0_SHDW_SPI0_REG_BASE)—Offset B00h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW	**GSPI PCI BAR (AddrBase)**
11:0	0h RO	Reserved.

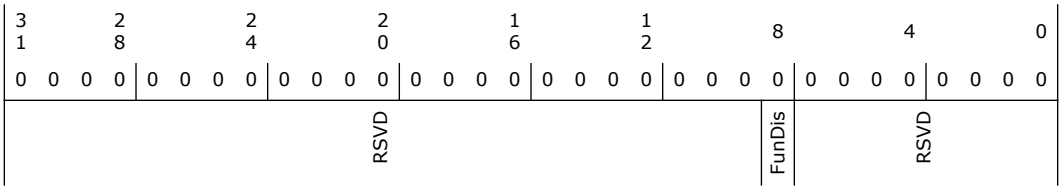
35.6.18 Function Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D30_F2_OFFSET11)—Offset B1Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h	**Function Disable (FunDis):** When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be carried out.
7:0	0h RO	Reserved.

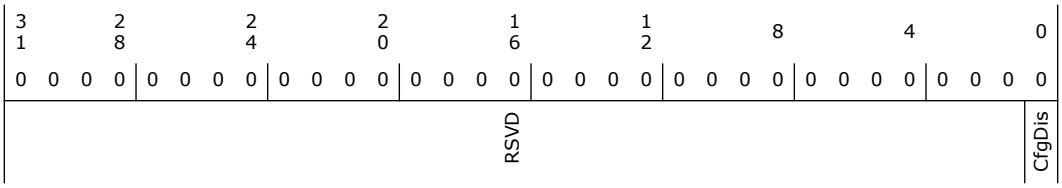
35.6.19 Offset 0B38h: PCI Configuration Disable (PSF_3_AGNT_T0_SHDW_CFG_DIS_LPSS_RS0_D30_F2_OFFSET11)—Offset B38h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h	**PCI Config Disable (CfgDis):** Default value=0, If set, the PCI configuration space of this device is switched off, and hidden from the OS. This bit is writable through IOSF SB interface only.

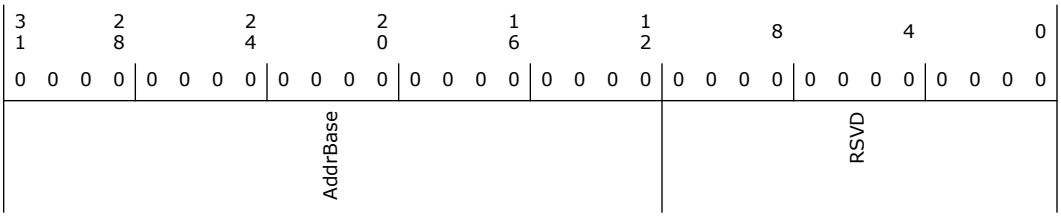
35.6.20 PCI Base Address (PSF3_T0_SHDW_UART1_REG_BASE)—Offset C00h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW	**UART1 PCI BAR (AddrBase)**
11:0	0h RO	Reserved.

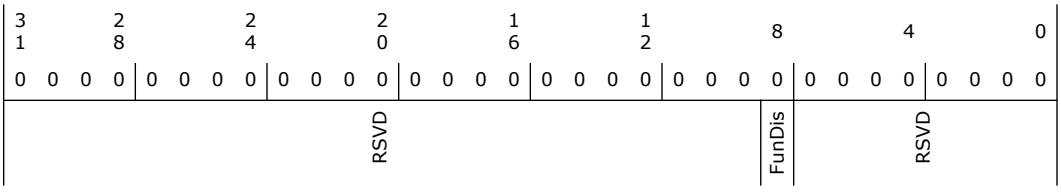
35.6.21 D30:F1 Function Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D30_F1_OFFSET12)—Offset C1Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h	**UART1 Function Disable (FunDis):** When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be carried out.
7:0	0h RO	Reserved.

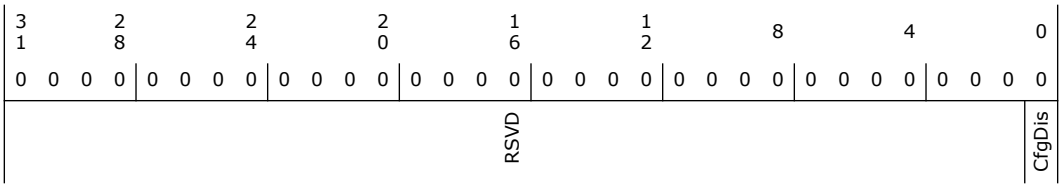
35.6.22 Offset 0C38h: PCI Configuration Disable (PSF_3_AGNT_T0_SHDW_CFG_DIS_LPSS_RS0_D30_F1_OFFSET12)—Offset C38h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h	**PCI Config Disable (CfgDis):** Default value=0, If set, the PCI configuration space of this device is switched off, and hidden from the OS. This bit is writable through IOSF SB interface only.

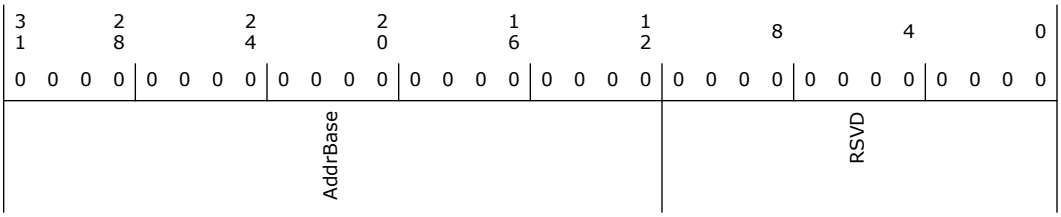
35.6.23 PCI Base Address (PSF3_T0_SHDW_UART0_REG_BASE)—Offset D00h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW	**UART PCI BAR (AddrBase)**
11:0	0h RO	Reserved.

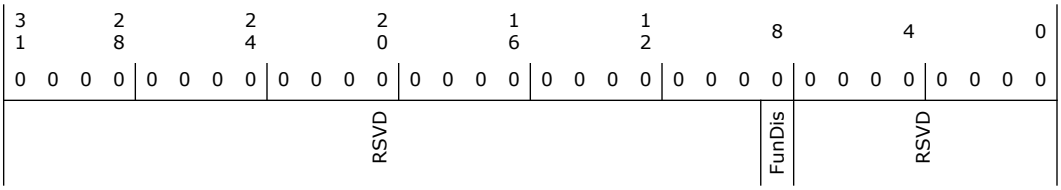
35.6.24 D30:F0 Function Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D30_F0_OFFSET13)—Offset D1Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h	**UART0 Function Disable (FunDis):** When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be carried out.
7:0	0h RO	Reserved.

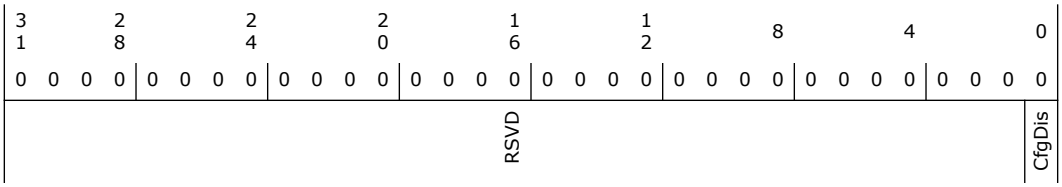
35.6.25 Offset 0D38h: PCI Configuration Disable (PSF_3_AGNT_T0_SHDW_CFG_DIS_LPSS_RS0_D30_F0_OFFSET13)—Offset D38h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h	**PCI Config Disable (CfgDis):** Default value=0, If set, the PCI configuration space of this device is switched off, and hidden from the OS. This bit is writable through IOSF SB interface only.

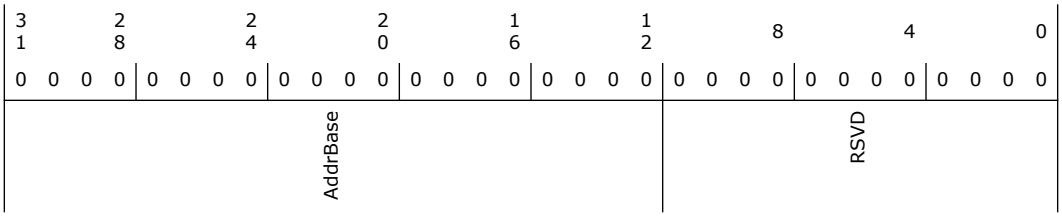
35.6.26 PCI Base Address (PSF3_T0_SHDW_I2C5_REG_BASE)—Offset E00h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW	**I2C5 PCI BAR (AddrBase)**
11:0	0h RO	Reserved.

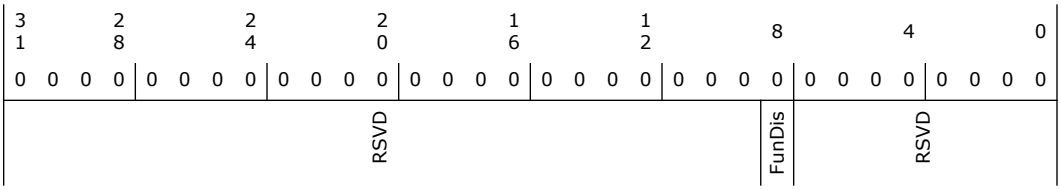
35.6.27 D25:F1 Function Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D25_F1_OFFSET14)—Offset E1Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h	**I2C5 Function Disable (FunDis):** When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be carried out
7:0	0h RO	Reserved.

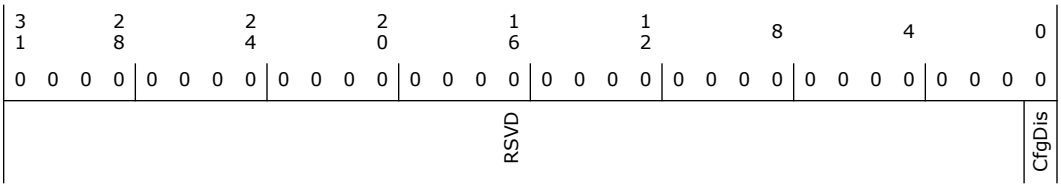
35.6.28 Offset 0E38h: PCI Configuration Disable (PSF_3_AGNT_T0_SHDW_CFG_DIS_LPSS_RS0_D25_F1_OFFSET14)—Offset E38h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h	**PCI Config Disable (CfgDis):** Default value=0, If set, the PCI configuration space of this device is switched off, and hidden from the OS. This bit is writable through IOSF SB interface only.

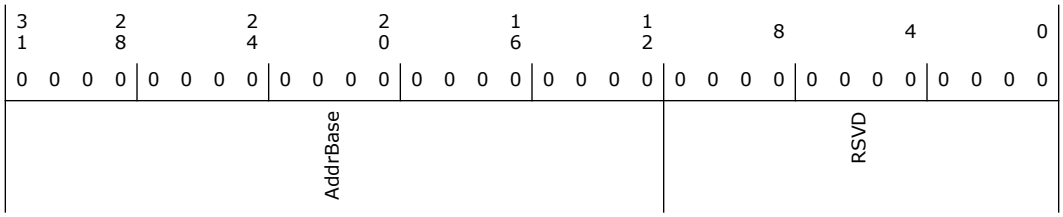
35.6.29 PCI Base Address (PSF3_T0_SHDW_UART2_REG_BASE)—Offset F00h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW	**UART2 PCI BAR (AddrBase)**
11:0	0h RO	Reserved.

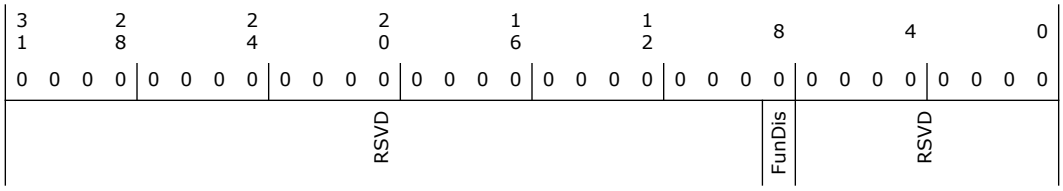
35.6.30 D25:F0 Function Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D25_F0_OFFSET15)—Offset F1Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h	**UART2 Functional Disable (FunDis):** When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be carried out.
7:0	0h RO	Reserved.

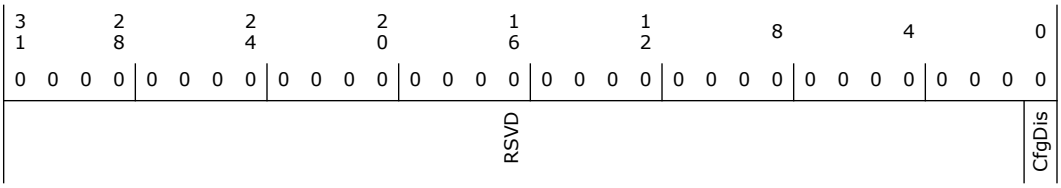
35.6.31 Offset 0F38h: PCI Configuration Disable (PSF_3_AGNT_T0_SHDW_CFG_DIS_LPSS_RS0_D25_F0_OFFSET15)—Offset F38h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h	**PCI Config Disable (CfgDis):** Default value=0, If set, the PCI configuration space of this device is switched off, and hidden from the OS. This bit is writable through IOSF SB interface only.

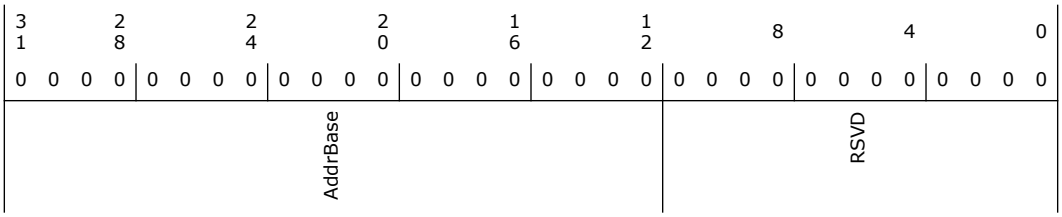
35.6.32 PCI Base Address (PSF3_T0_SHDW_I2C3_REG_BASE)—Offset 1000h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW	**I2C3 PCI BAR (AddrBase)**
11:0	0h RO	Reserved.

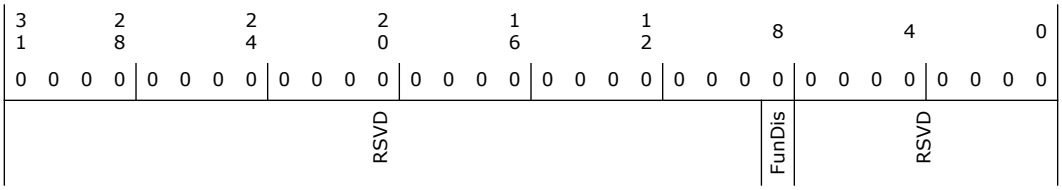
35.6.33 D21:F3 Function Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D21_F3_OFFSET16)—Offset 101Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h	**I2C3 Function Disable (FunDis):** When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be carried out.
7:0	0h RO	Reserved.

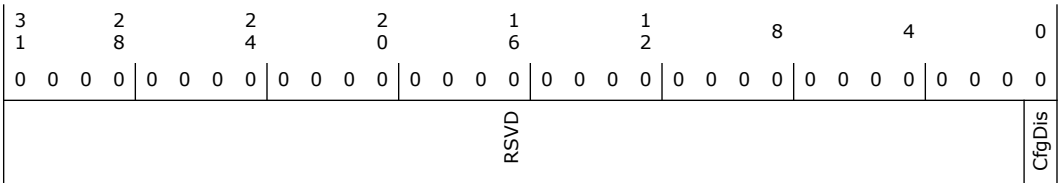
35.6.34 Offset 1038h: PCI Configuration Disable (PSF_3_AGNT_T0_SHDW_CFG_DIS_LPSS_RS0_D21_F3_OFFSET16)—Offset 1038h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h	**PCI Config Disable (CfgDis):** Default value=0, If set, the PCI configuration space of this device is switched off, and hidden from the OS. This bit is writable through IOSF SB interface only.

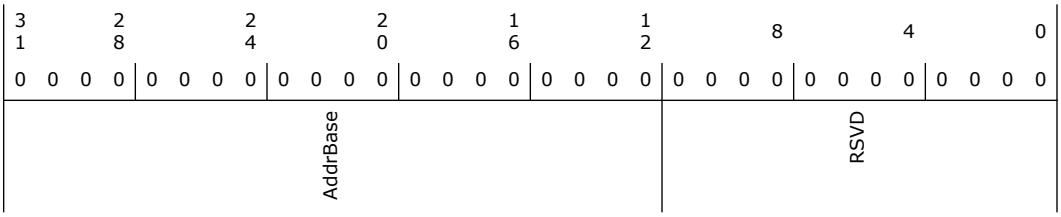
35.6.35 PCI Base Address (PSF3_T0_SHDW_I2C2_REG_BASE)—Offset 1100h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW	**I2C2 PCI BAR (AddrBase)**
11:0	0h RO	Reserved.

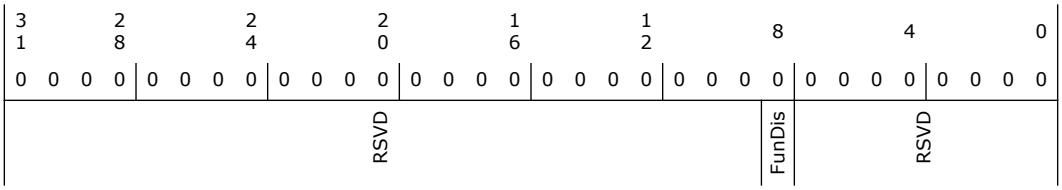
35.6.36 D21:F2 Function Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D21_F2_OFFSET17)—Offset 111Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h	**I2C2 Function Disable (FunDis):** When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be carried out.
7:0	0h RO	Reserved.

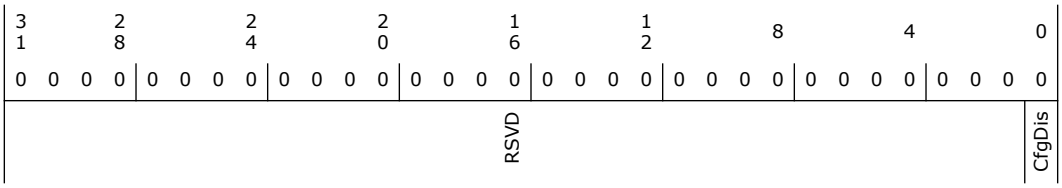
35.6.37 Offset 1138h: PCI Configuration Disable (PSF_3_AGNT_T0_SHDW_CFG_DIS_LPSS_RS0_D21_F2_OFFSET17)—Offset 1138h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h	**PCI Config Disable (CfgDis):** Default value=0, If set, the PCI configuration space of this device is switched off, and hidden from the OS. This bit is writable through IOSF SB interface only.

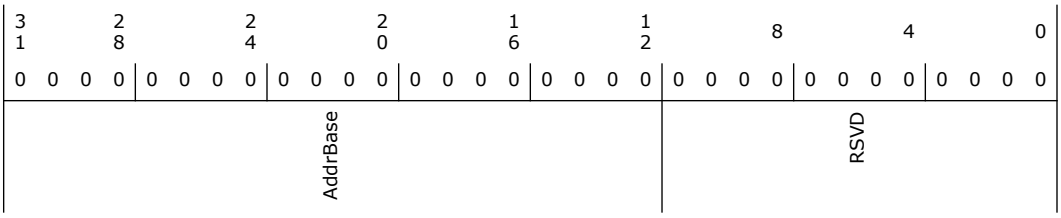
35.6.38 PCI Base Address (PSF3_T0_SHDW_I2C1_REG_BASE)—Offset 1200h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW	**I2C1 PCI BAR (AddrBase)**
11:0	0h RO	Reserved.

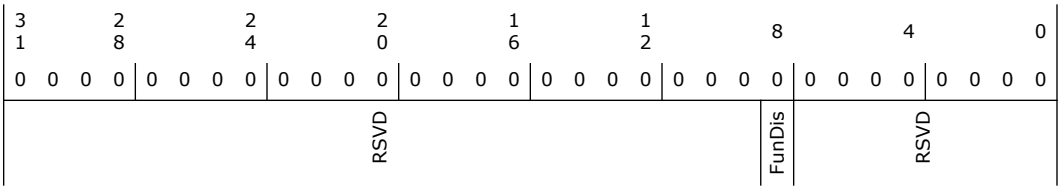
35.6.39 D21:F1 Function Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D21_F1_OFFSET18)—Offset 121Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h	**I2C1 Function Disable (FunDis):** When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be carried out.
7:0	0h RO	Reserved.

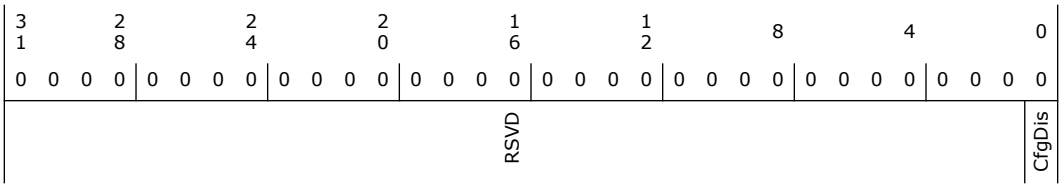
35.6.40 Offset 1238h: PCI Configuration Disable (PSF_3_AGNT_T0_SHDW_CFG_DIS_LPSS_RS0_D21_F1_OFFSET18)—Offset 1238h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h	**PCI Config Disable (CfgDis):** Default value=0, If set, the PCI configuration space of this device is switched off, and hidden from the OS. This bit is writable through IOSF SB interface only.

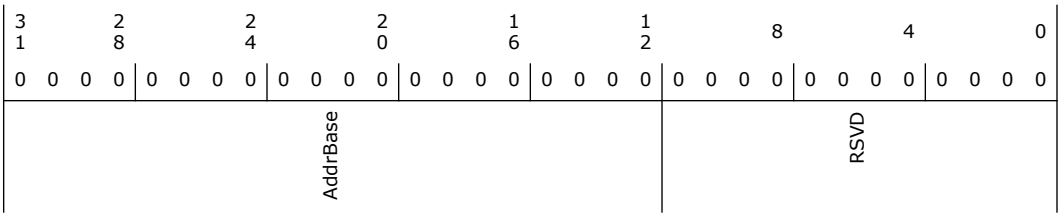
35.6.41 PCI Base Address (PSF3_T0_SHDW_I2C0_REG_BASE)—Offset 1300h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW	**I2C PCI BAR (AddrBase)**
11:0	0h RO	Reserved.

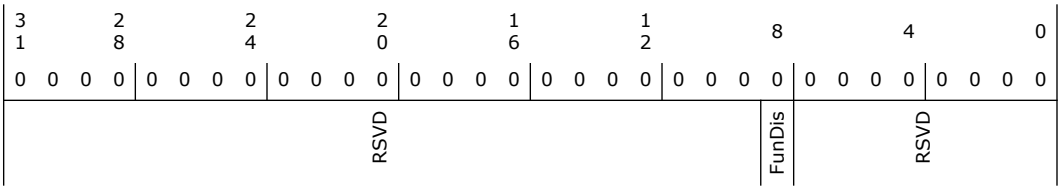
35.6.42 D21:F0 Function Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D21_F0_OFFSET19)—Offset 131Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h	**I2C0 Function Disable (FunDis):** When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be carried out.
7:0	0h RO	Reserved.

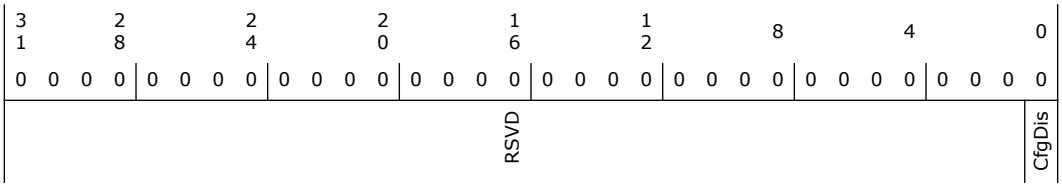
35.6.43 Offset 1338h: PCI Configuration Disable (PSF_3_AGNT_T0_SHDW_CFG_DIS_LPSS_RS0_D21_F0_OFFSET19)—Offset 1338h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h	**PCI Config Disable (CfgDis):** Default value=0, If set, the PCI configuration space of this device is switched off, and hidden from the OS. This bit is writable through IOSF SB interface only.

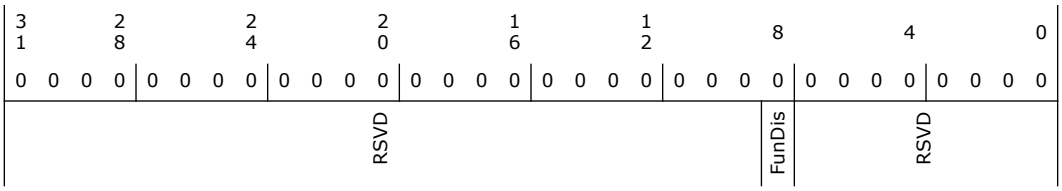
35.6.44 Function Disable (PSF_3_AGNT_T0_SHDW_PCIEN_SPI_RS0_D31_F0_OFFSET23)—Offset 171Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h	**Function Disable (FunDis):** When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be carried out.
7:0	0h RO	Reserved.

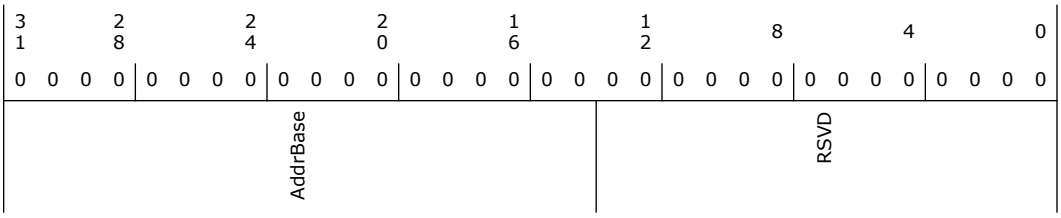
35.6.45 PCI Base Address (PSF3_T0_SHDW_AUD_REG_BASE)—Offset 1900h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RW	**Audio PCI BAR (AddrBase)**
13:0	0h RO	Reserved.

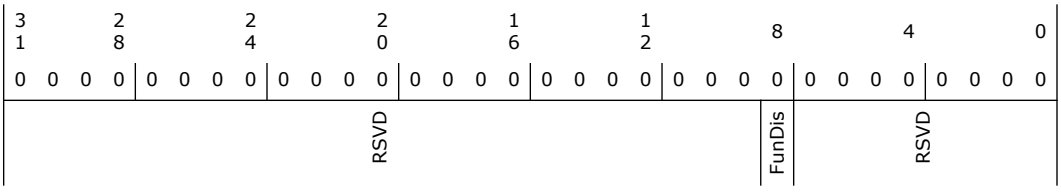
35.6.46 PCI Configuration Space Enable (PSF_3_AGNT_T0_SHDW_PCIEN_AUD_RS0_D31_F3_OFFSET25)—Offset 191Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h	**FunDis:** Default value=0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through IOSF SB interface only.
7:0	0h RO	Reserved.

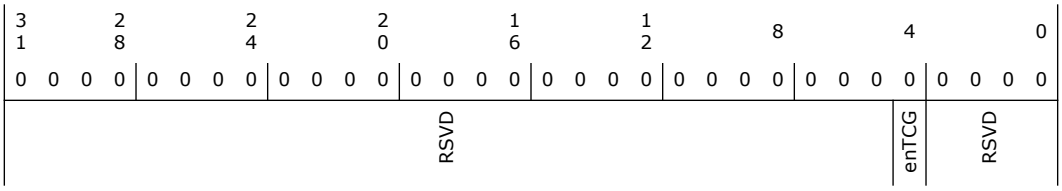
35.6.47 PSF Global Configuration (PSF_3_PSF_GLOBAL_CONFIG)—Offset 4000h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4	0h	**enTCG:** If set, PSF will use its clkreq/ack signals to request and maintain a clock for a transaction. If set to 0, PSF will permanently assert all clkreq and signals.
3:0	0h RO	Reserved.

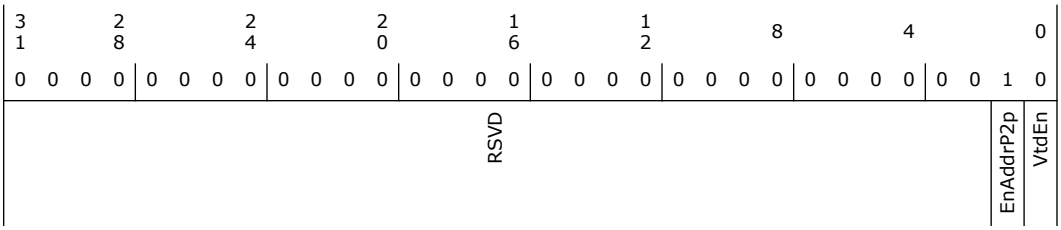
35.6.48 Root Space Config (PSF_3_ROOTSPACE_CONFIG_RS0)—Offset 4010h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 2h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1	1h	**Address Enable (EnAddrP2p):** Default value=1, If set, address-based p2p transactions are allowed for this root space.
0	0h	**VTd Enable (VtdEn):** Default value=0, If set Intel Virtualization Technology for Directed I/O is enabled for this root space. This bit should reflect the system-wide vt-d setting, and is typically maintained by BIOS

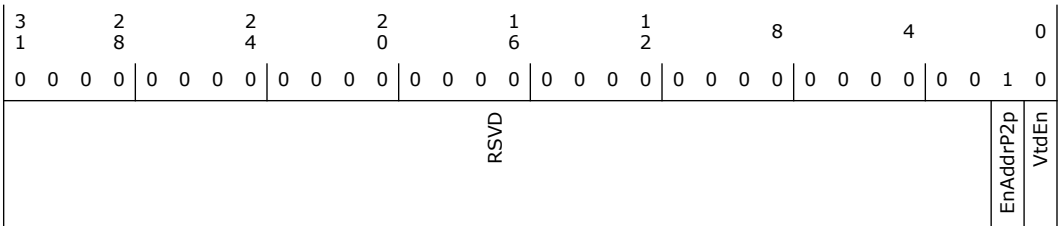
35.6.49 Rootspace Configuration (PSF_3_ROOTSPACE_CONFIG_RS1)—Offset 4014h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 2h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1	1h	**EnAddrP2p:** Default value=1, If set, address-based p2p transactions are allowed for this root space.
0	0h	**VtdEn:** Default value=0, If set Intel Virtualization Technology for Directed I/O is enabled for this root space. This bit should reflect the system-wide vt-d setting, and is typically maintained by BIOS

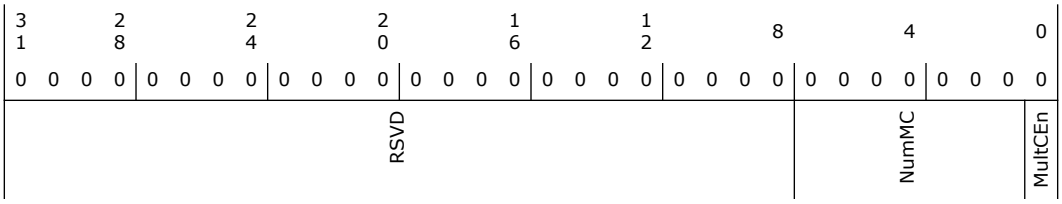
35.6.50 Multicast Control (PSF_3_PSF_MC_CONTROL_MCAST0_RS0_EOI)—Offset 404Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:1	0h	**Multicast Agent (NumMC):** Number of multicast Agents on this root-space on the PSF segment.
0	0h	**Multicast Enable (MultCEn):** Multicast Enable. If set Multicast transactions are supported on this root-space, and can be received on any PSF port.

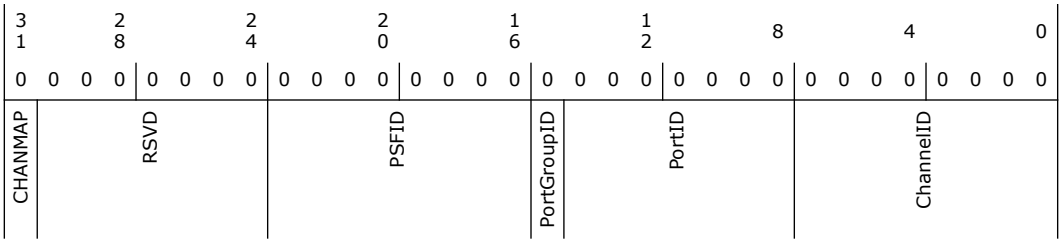
35.6.51 Destination ID (PSF_3_PSF_MC_AGENT_MCAST0_RS0_TGT0_EOI)—Offset 4054h

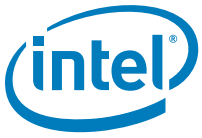
Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h





Bit Range	Default & Access	Field Name (ID): Description
31	0h	**Channel ID Map (CHANMAP):** If this bit is set, the ChannelID field is ignored and looked up in the CHANMAP register set that belongs to PortGroupID:PortID
30:24	0h RO	Reserved.
23:16	0h	**PSF ID (PSFID):** Default value=0x0
15	0h	**Port Group ID (PortGroupID):** Default value=0x0
14:8	0h	**Port ID (PortID):** Since 1'b0 indicates source-decode, the port ID needs to be larger than 0
7:0	0h	**Channel ID (ChannelID):** Default value=0x0

35.7 PSF4 PCR Registers Summary

These registers are within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID + Register Offset).

Table 35-7. Summary of PSF4 PCR Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
4000h	4003h	PSF Global Configuration (PSF_4_PSF_GLOBAL_CONFIG)—Offset 4000h	0h
4010h	4013h	Root Space Configuration (PSF_4_ROOTSPACE_CONFIG_RS0)—Offset 4010h	2h
4014h	4017h	Root Space Configuration (PSF_4_ROOTSPACE_CONFIG_RS1)—Offset 4014h	2h

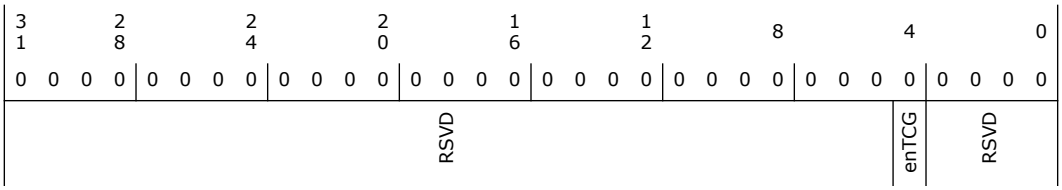
35.7.1 PSF Global Configuration (PSF_4_PSF_GLOBAL_CONFIG)—Offset 4000h

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4	0h	**enTCG:** If set, PSF will use its clkreq/ack signals to request and maintain a clock for a transaction. If set to 0, PSF will permanently assert all clkreq and signals.
3:0	0h RO	Reserved.

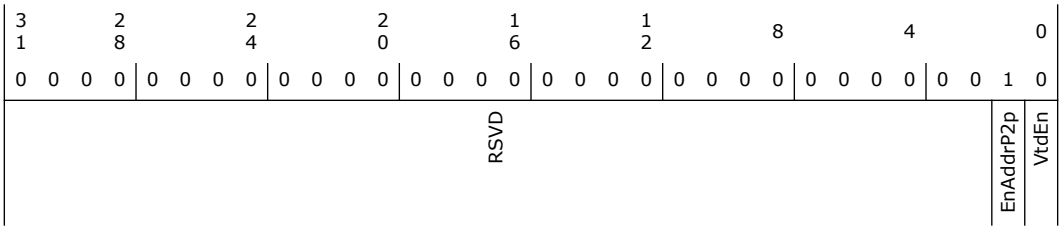
35.7.2 Root Space Configuration (PSF_4_ROOTSPACE_CONFIG_RS0)—Offset 4010h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 2h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1	1h	**Address Enable (EnAddrP2p):** Default value=1, If set, address-based p2p transactions are allowed for this root space.
0	0h	**VTd Enable (VtdEn):** Default value=0, If set Intel Virtualization Technology for Directed I/O is enabled for this root space. This bit should reflect the system-wide vt-d setting, and is typically maintained by BIOS

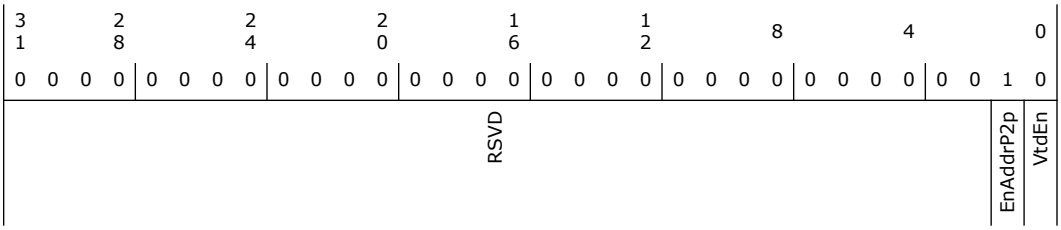
35.7.3 Root Space Configuration (PSF_4_ROOTSPACE_CONFIG_RS1)—Offset 4014h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 2h



Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1	1h	**EnAddrP2p:** Default value=1, If set, address-based p2p transactions are allowed for this root space.
0	0h	**VtdEn:** Default value=0, If set Intel Virtualization Technology for Directed I/O is enabled for this root space. This bit should reflect the system-wide vt-d setting, and is typically maintained by BIOS

35.8 IO Trap Registers Summary

These registers are within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID + Register Offset).

Table 35-8. Summary of IO Trap Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
1D00h	1D03h	PSTH Control Register (PSTHCTL)—Offset 1D00h	0h
1E00h	1E03h	Trap Status Register (TRPSTS)—Offset 1E00h	0h
1E10h	1E13h	Trapped Cycle Register (TRPCYC1)—Offset 1E10h	0h
1E18h	1E1Bh	Trapped Write Data Register (TRPWRDATA1)—Offset 1E18h	0h
1E80h	1E83h	I/O Trap Registers 1 (IOTRP1_1)—Offset 1E80h	0h
1E84h	1E87h	I/O Trap Registers 1 (IOTRP1_2)—Offset 1E84h	0h
1E88h	1E8Bh	I/O Trap Registers 2 (IOTRP2_1)—Offset 1E88h	0h
1E8Ch	1E8Fh	I/O Trap Registers 2 (IOTRP2_2)—Offset 1E8Ch	0h
1E90h	1E93h	I/O Trap Registers 3 (IOTRP3_1)—Offset 1E90h	0h
1E94h	1E97h	I/O Trap Registers 3 (IOTRP3_2)—Offset 1E94h	0h
1E98h	1E9Bh	I/O Trap Registers 4 (IOTRP4_1)—Offset 1E98h	0h
1E9Ch	1E9Fh	I/O Trap Registers 4 (IOTRP4_2)—Offset 1E9Ch	0h

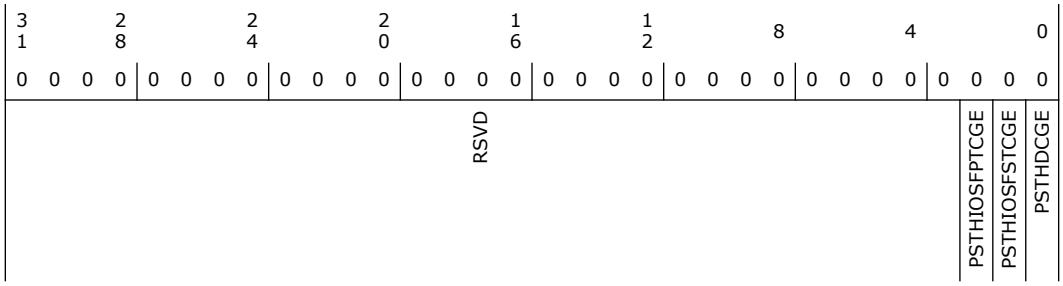
35.8.1 PSTH Control Register (PSTHCTL)—Offset 1D00h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	Reserved.
2	0h RW	**PSTH IOSF Primary Clock Gating Enable (PSTHIOSFPTCGE):** 0 = Disable 1 = Enable
1	0h RW	**PSTH IOSF Sideband Clock Gating Enable (PSTHIOSFSTCGE):** 0 = Disable 1 = Enable
0	0h RW	**PSTH Dynamic Clock Gating Enable (PSTHDCGE):** 0 = Disable 1 = Enable

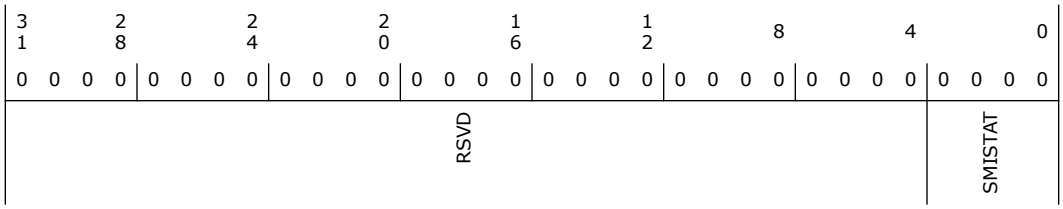
35.8.2 Trap Status Register (TRPSTS)—Offset 1E00h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3:0	0h RWC	**Cycle Trap SMI# Status (SMISTAT):** These bits are set by hardware when the corresponding Cycle Trap register is enabled and a matching cycle is received (and trapped). These bits are OR'ed together to create a single status bit in the Power Management register space.Note that the SMI# and trapping must be enabled in order to set these bits. This is because, in order to do the cycle comparison, packets must be delayed by several clocks from the DMI pins to the internal receiver. This delay is only enabled when at least one of the trap ranges is enabled. These bits are set before the completion is generated for the trapped cycle, thereby guaranteeing that the processor can enter the SMI# handler when the instruction completes. Each status bit is cleared by writing a '1' to the corresponding bit location in this register.

35.8.3 Trapped Cycle Register (TRPCYC1)—Offset 1E10h

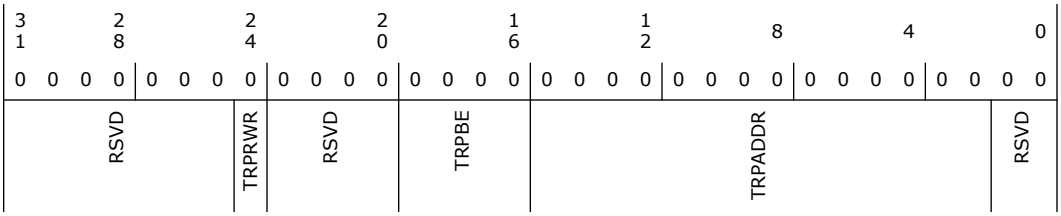
This register saves information about the I/O Cycle that was trapped and generated the SMI# for software to read.

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	Reserved.
24	0h RO/V	**Read-Write (TRPRWR):** 1 = Read, 0 = Write
23:20	0h RO	Reserved.
19:16	0h RO/V	**Active-High Byte Enables (TRPBE):** This is the DWord-aligned byte enables associated with the trapped cycle. A 1 in any bit location indicates that the corresponding byte is enabled in the cycle.
15:2	0h RO/V	**IO Address (TRPADDR):** This is the DWord-aligned address of the trapped cycle.
1:0	0h RO	Reserved.

35.8.4 Trapped Write Data Register (TRPWRDATA1)—Offset 1E18h

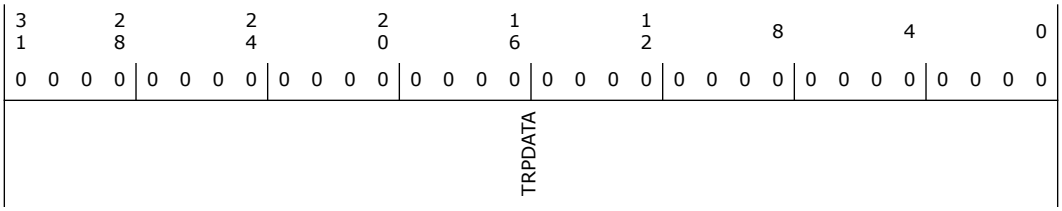
This register saves the data from I/O write cycles that are trapped for software to read

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Data (TRPDATA):** DWord of I/O write data. This field is undefined after trapping a read cycle.

35.8.5 I/O Trap Registers 1 (IOTRP1_1)—Offset 1E80h

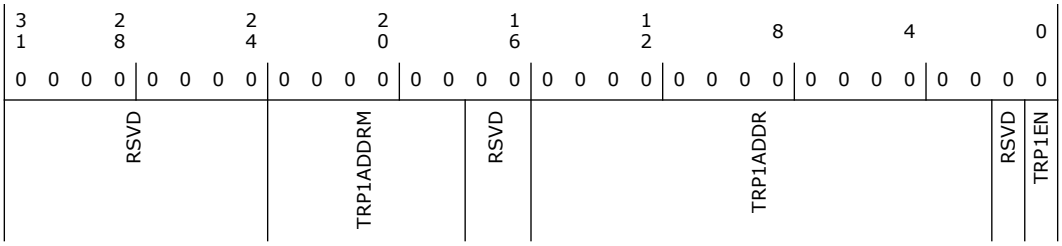
These registers are used to specify the set of I/O cycles to be trapped and to enable this functionality.

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:18	0h RW	**Address Mask (TRP1ADDRM):** A '1' in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for traps on address ranges up to 256 bytes in size.
17:16	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
15:2	0h RW	**Address (TRP1ADDR):** DWord-aligned address
1	0h RO	Reserved.
0	0h RW	**Trap and SMI Enable (TRP1EN):** When this bit is set to 1, then the trapping logic specified in this register is enabled.

35.8.6 I/O Trap Registers 1 (IOTRP1_2)—Offset 1E84h

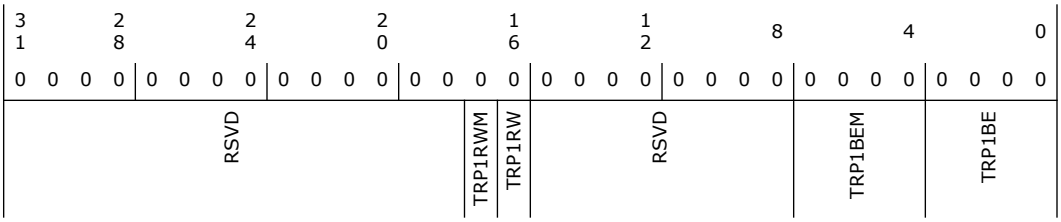
These registers are used to specify the set of I/O cycles to be trapped and to enable this functionality.

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17	0h RW	**Read-Write Mask (TRP1RWM):** When this bit is '1', the trapping logic will operate on both read and write cycles. When this bit is '0', the cycle must match the type specified in bit 48.
16	0h RW	**Read/Write (TRP1RW):** 1 = Read, 0 = Write, the value in this field does not matter if bit 49 is set.
15:8	0h RO	Reserved.
7:4	0h RW	**Byte Enable Mask (TRP1BEM):** A '1' in any bit position indicates that any value in the corresponding byte enable bit in a received cycle will be treated as a match. The corresponding bit in the Byte Enables field, below, is ignored.
3:0	0h RW	**Byte Enables (TRP1BE):** Active-high, DWord-aligned byte enables

35.8.7 I/O Trap Registers 2 (IOTRP2_1)—Offset 1E88h

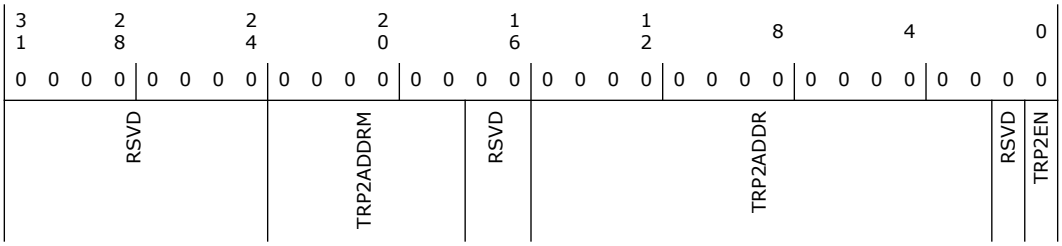
These registers are used to specify the set of I/O cycles to be trapped and to enable this functionality.

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:18	0h RW	**Address Mask (TRP2ADDRM):** A '1' in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for traps on address ranges up to 256 bytes in size.
17:16	0h RO	Reserved.
15:2	0h RW	**Address (TRP2ADDR):** DWord-aligned address
1	0h RO	Reserved.
0	0h RW	**Trap and SMI Enable (TRP2EN):** When this bit is set to 1, then the trapping logic specified in this register is enabled.

35.8.8 I/O Trap Registers 2 (IOTRP2_2)—Offset 1E8Ch

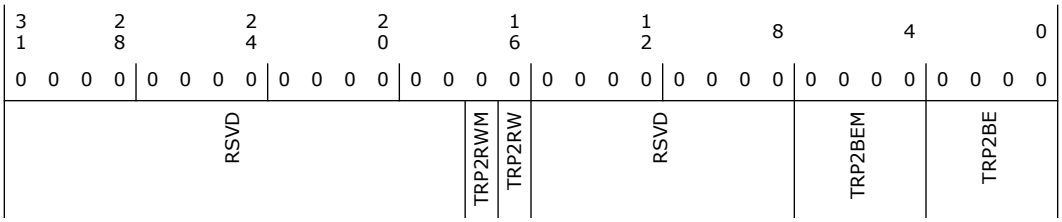
These registers are used to specify the set of I/O cycles to be trapped and to enable this functionality.

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17	0h RW	**Read-Write Mask (TRP2RWM):** When this bit is '1', the trapping logic will operate on both read and write cycles. When this bit is '0', the cycle must match the type specified in bit 48.
16	0h RW	**Read/Write (TRP2RW):** 1 = Read, 0 = Write, the value in this field does not matter if bit 49 is set.
15:8	0h RO	Reserved.
7:4	0h RW	**Byte Enable Mask (TRP2BEM):** A '1' in any bit position indicates that any value in the corresponding byte enable bit in a received cycle will be treated as a match. The corresponding bit in the Byte Enables field, below, is ignored.
3:0	0h RW	**Byte Enables (TRP2BE):** Active-high, DWord-aligned byte enables

35.8.9 I/O Trap Registers 3 (IOTRP3_1)—Offset 1E90h

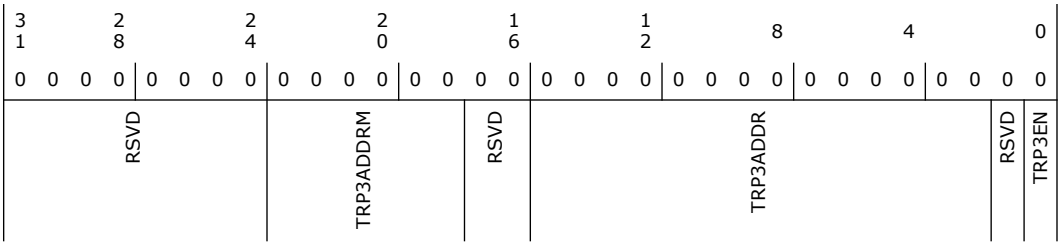
These registers are used to specify the set of I/O cycles to be trapped and to enable this functionality.

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:18	0h RW	**Address Mask (TRP3ADDRM):** A '1' in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for traps on address ranges up to 256 bytes in size.
17:16	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
15:2	0h RW	**Address (TRP3ADDR):** DWord-aligned address
1	0h RO	Reserved.
0	0h RW	**Trap and SMI Enable (TRP3EN):** When this bit is set to 1, then the trapping logic specified in this register is enabled.

35.8.10 I/O Trap Registers 3 (IOTRP3_2)—Offset 1E94h

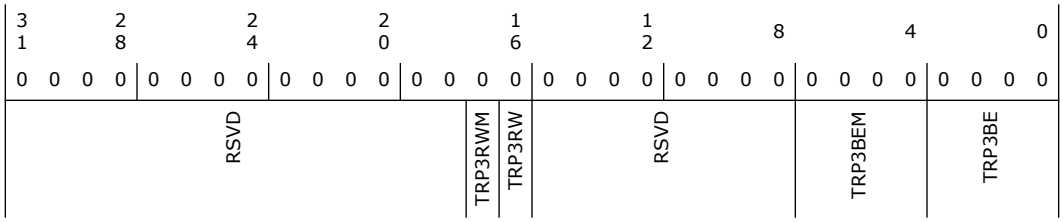
These registers are used to specify the set of I/O cycles to be trapped and to enable this functionality.

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17	0h RW	**Read-Write Mask (TRP3RWM):** When this bit is '1', the trapping logic will operate on both read and write cycles. When this bit is '0', the cycle must match the type specified in bit 48.
16	0h RW	**Read/Write (TRP3RW):** 1 = Read, 0 = Write, the value in this field does not matter if bit 49 is set.
15:8	0h RO	Reserved.
7:4	0h RW	**Byte Enable Mask (TRP3BEM):** A '1' in any bit position indicates that any value in the corresponding byte enable bit in a received cycle will be treated as a match. The corresponding bit in the Byte Enables field, below, is ignored.
3:0	0h RW	**Byte Enables (TRP3BE):** Active-high, DWord-aligned byte enables

35.8.11 I/O Trap Registers 4 (IOTRP4_1)—Offset 1E98h

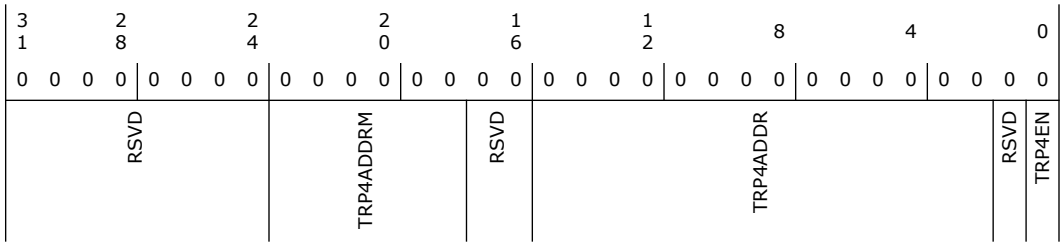
These registers are used to specify the set of I/O cycles to be trapped and to enable this functionality.

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:18	0h RW	**Address Mask (TRP4ADDRM):** A '1' in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for traps on address ranges up to 256 bytes in size.
17:16	0h RO	Reserved.
15:2	0h RW	**Reserved (TRP4ADDR):** DWord-aligned address
1	0h RO	Reserved.
0	0h RW	**Trap and SMI Enable (TRP4EN):** When this bit is set to 1, then the trapping logic specified in this register is enabled.

35.8.12 I/O Trap Registers 4 (IOTRP4_2)—Offset 1E9Ch

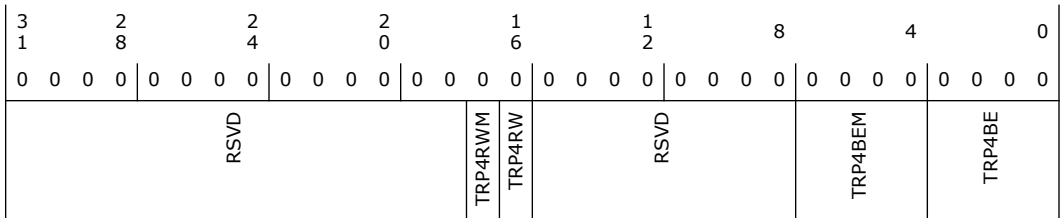
These registers are used to specify the set of I/O cycles to be trapped and to enable this functionality.

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h



Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17	0h RW	**Read-Write Mask (TRP4RWM):** When this bit is '1', the trapping logic will operate on both read and write cycles. When this bit is '0', the cycle must match the type specified in bit 48.
16	0h RW	**Read/Write (TRP4RW):** 1 = Read, 0 = Write, the value in this field does not matter if bit 49 is set.
15:8	0h RO	Reserved.
7:4	0h RW	**Byte Enable Mask (TRP4BEM):** A '1' in any bit position indicates that any value in the corresponding byte enable bit in a received cycle will be treated as a match. The corresponding bit in the Byte Enables field, below, is ignored.
3:0	0h RW	**Byte Enables (TRP4BE):** Active-high, DWord-aligned byte enables

§ §