NI4010A DATA GENERAL ETHERNET COMMUNICATIONS CONTROLLER USER MANUAL

UM-NI4010A (950-0010-AA) (Rev.AA)

MICOM-Interlan, Incorporated
155 Swanson Road
Boxborough, MA 01719

Eastern Area

MICOM-INTERLAN
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155 Swanson Rd.,
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Telephone (617) 263-9929 Telex 95-1909

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PREFACE

This manual describes how to install, program, and maintain the NI4010A Data General ETHERNET/IEEE-802 Communications Controller. It contains five chapters and one appendix. They are

Chapter 1, Introduction. This chapter is a general description of the NI4010A features, specifications, and accessories.

Chapter 2, Installation. This chapter tells you how to unpack, configure, install, and cable the NI4010A.

Chapter 3, Programming Information. This chapter tells you how to program the NI4010A. It contains complete descriptions of NI4010A data formats, all the NI4010A registers, and all the NI4010A commands. It concludes with some programming guidelines.

Chapter 4, Functional Description. This chapter describes the NI4010A architecture. It explains how the NI4010A transmits data, receives data, and executes its onboard diagnostic programs.

Chapter 5, Maintenance. This chapter provides more information about the NI4010A onboard diagnostic programs.

Appendix A, ETHERNET/IEEE-802 Network Planning, Installation, and Test Guidelines. This chapter will help you plan and install an ETHERNET/IEEE-802 network.

You can find more information about ETHERNET and IEEE-802 in

The ETHERNET, a Local Area Network Data Link and Physical Layer Specification, September 30, 1980, Xerox/Intel/Digital.

IEEE P802 LOCAL AREA NETWORK STANDARD PROJECT - CSMA/CD ENVIRONMENT, DRAFT STANDARD P802.3, September, 1982.

Interlan would like to hear any comments, corrections, or suggestions that you might have about this manual. Send correspondence to:

Interlan, Inc.
3 Lyberty Way
Westford, Massachusetts 01886

(617) 692-3900 Telex 95-1909

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CHAPTER ONE

INTRODUCTION

The NI4010A Data General ETHERNET/IEEE-802 Communication Controller is a single board that contains all the data communications controller logic required for interfacing Data General NOVA, ECLIPSE, and 32-bit ECLIPSE/MV minicomputers to the ETHERNET/IEEE-802 local area network.

The NI4010A implements the industry standard ETHERNET and IEEE-802 CSMA/CD local area network specifications - permitting Data General systems to engage in high speed transmission and reception of data with other stations on the 10 Mbps local network.

Figure 1-1 illustrates the ETHERNET/IEEE-802 architecture and its NI4010A implementation.

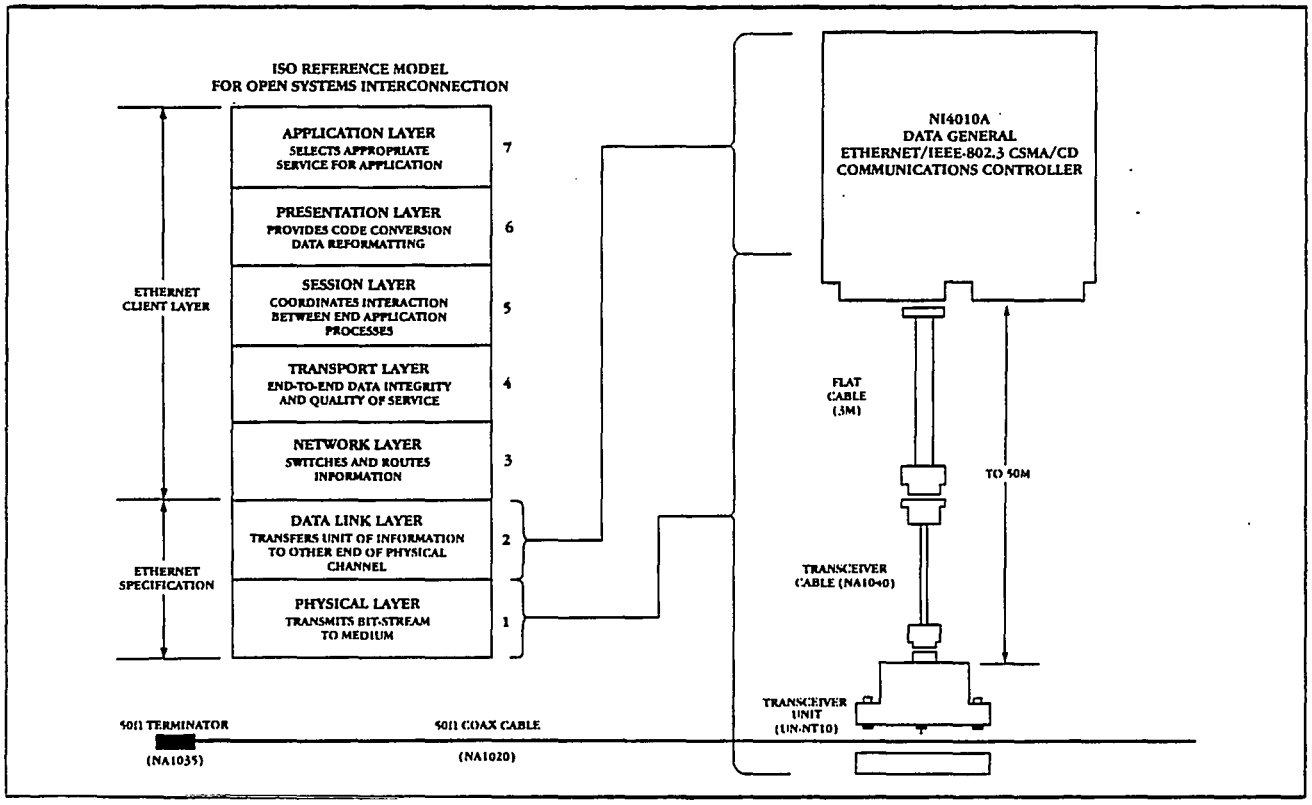


Figure 1-1. ETHERNET/IEEE-802 Architecture and NI4010A Implementation

1.1 NI4010A FEATURES

The NI4010A has a number of important features. The NI4010A:

* Complies with the ETHERNET and IEEE-802 CSMA/CD specifications.

* Performs all network data link functions.

  The NI4010A formats your data into network frames and performs CSMA/CD (carrier sense, multiple access with collision detect).

  When not transmitting a frame, the NI4010A listens to the network. The NI4010A accepts a frame if the frame's destination address matches the NI4010A physical address, one of the NI4010A multicast addresses, or the broadcast address.

  The NI4010A performs CRC generation and CRC checking and tests received frames for alignment errors. You can choose to have the NI4010A accept or reject error frames.

* Performs all network physical channel functions.

  The NI4010A transmits and receives bit streams at 10 Megabits/second. Its electrical and timing specifications are compatible with the ETHERNET and IEEE-802 transceiver cable interface.

  The NI4010A performs the required frame synchronization and manchester encoding/decoding.

  The NI4010A performs the carrier deference and collision detection functions.

* Maintains high station performance while minimizing the service load placed on the host system.

  The NI4010A contains a 13.5 Kbyte receive FIFO buffer. Network frames characteristically arrive with unpredictable arrival times. The NI4010A stores receive frames in its receive buffer. The host can read this buffer at its own convenience.

  The NI4010A performs high speed data channel transfers to and from host memory.

* Provides extensive diagnostic capability.

  After a hardware reset, the NI4010A performs a set of power-up tests. A pass/fail LED indicates the success or failure of these tests. If a confidence test fails, a diagnostic status code provides further information.

  The internal loopback allows frames to be looped from the host transmit buffer to the host receive buffer without being sent onto the network.

  The network loopback verifies that data can be sent and received to and from the network.

  The collision test verifies that the transceiver can detect collisions.

  Network activity LED's indicate when the transceiver transmit, receive, and collision lines are asserted.

* Collects and reports network statistics.

  The NI4010A collects information on network traffic and errors. You can read this information under program control.

1.2 NI4010A SPECIFICATIONS

This section contains network, Data General I/O bus, transceiver, and environmental specifications.

1.2.1 Network Specifications

Data transmission rate	10 Megabits/second
Maximum coaxial cable segment length	500 meters (1640 feet)
Maximum coaxial cable length between two stations	1500 meters (4920 feet)
Maximum length of point-to-point links	1000 meters (3280 feet)
Maximum station separation	2500 meters (1.55 miles)
Maximum distance between the NI4010A and its tranceiver	50 meters (165 feet)
Maximum number of transceivers on a coaxial cable segment	100
Maximum number of repeaters between any two stations	2
Maximum number of stations on a network	1024

1.2.2 Data General I/O Bus Specifications

Power	The NI4010A requires +5Vdc +- 5% @ 6.5 A maximum. The NT10 transceiver requires +12 to +15 Vdc +- 5% @ 0.5 A maximum.
Octal device code (switch selectable)	46 for command operations 47 for transmit operations
Octal mask bit (switch selectable)	14
Transfer rate	2 megabytes per second
Allowed latency	infinite
Memory map support	supports 16 data channel map slots
Mounting	single chassis slot
Cabling	flat transceiver cable from backpanel pins

1.2.3 Transceiver Specifications

Compatibility	All transceiver signals are compatible with the ETHERNET and IEEE-802 CSMA/CD specifications The transceiver connects to the host backpanel connector I/O bus pins

1.2.4 Environmental Specifications

Operating temperature	0 to 50 degrees Celsius (32 to 122 Fahrenheit)
Relative humidity	Maximum of 90%, non-condensing.

1.3 NI4010A RELATED PRODUCTS AND ACCESSORIES

Model number	Description
BD-NI4010A	NI4010A Data General ETHERNET/IEEE-802 communications controller. Does not include any accessories.
DS-NI4010A-MT16	Standalone diagnostic software for the NI4010A. Supplied on 1600 bpi magtape.
UM-NI4010A	User manual for NI4010A controller board.
NS2060-MT16	RDOS ".IDEF" device driver for the NI4010A; includes user manual (UM-NS2060), source code, and supported software license (SL-NS2060-S).
SL-NS2060-U	Software license for right to use NS2060 on an additional host processor system, unsupported.
NS2070-MT16	AOS ".IDEF" device driver for the NI4010A; includes user manual (UM-NS2070), source code, and supported software license (SL-NS2070-S).
SL-NS2070-U	Software license for right to use NS2070 on an additional host processor system, unsupported.
S2080-MT16	AOS/VS ".IDEF" device driver for the NI4010A; includes user manual (UM-NS2080), source code, and supported software license (SL-NS2080-S).
SL-NS2080-U	Software license for right to use NS2080 on an additional host processor system, unsupported.
NA4010A-10	10 foot (3 meters) flat cable with connectors. Connects the NI4010A to the transceiver or to the transceiver cable.
NA1010-xxx	Transceiver cable. Extends between the flat cable and the ETHERNET/IEEE-802 transceiver. Available in lengths of 10, 50, and 150 feet.
NA1020-xxx	ETHERNET/IEEE-802 50 ohm coaxial cable. Available in lengths of 77, 230, and 385 feet.
NA1035	50 ohm N-type female cable terminator (two are required per cable segment)
UN-NT10	NT10 ETHERNET/IEEE-802 transceiver unit
IK-NT10	Installation kit for NT10 transceiver unit.

CHAPTER TWO

INSTALLATION

The NI4010A is a single board assembly that is mechanically, electrically, and architecturally compatible with Data General's standards for I/O bus compatibility. You can install the NI4010A in any Data General host system that uses the 15 inch form factor.

This chapter tells you how to configure the NI4010A, install it in a Data General host system, and cable it to the ETHERNET. Section 2.5 contians a checklist to help you install the NI4010A.

2.1 UNPACKING AND INSPECTION

To protect against damage during shipment, INTERLAN packages each NI4010A in a special carton.

Open the carton from the top and remove the contents.

Carefully inspect the NI4010A board and other enclosed material for any visible sign of damage. If you detect any damage, immediately notify Interlan Customer Service and the carrier responsible for shipment.

Save all shipping cartons and packing material in case you need to reship the product.

2.2 NI4010A ETHERNET/IEEE-802 CONSIDERATIONS

The NI4010A is completely compatible with the ETHERNET and IEEE-802 local area network specifications. Appendix A will help you install and test an ETHERNET/IEEE-802 coaxial cable transmission system.

2.2.1 Transceiver Placement

All transceiver connections to the network transmission cable introduce a finite bridging impedance that causes some (albeit small) amount of signal reflection. To ensure that reflections from transceivers do not cause transmission errors, you must control the placement of transceivers along the cable.

Approved network coaxial cable is marked with annular rings at 2.5 meter intervals. By only placing a transceiver at one of of these rings, you minimize the likelihood of having transceiver reflections with phase angles that add.

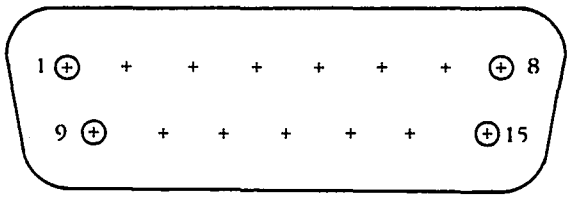
The total number of transceivers on a cable segment must not exceed 100.

2.2.2 NI4010A Transceiver Interface and Cable Requirements

The NI4010A connects to the network via the host backpanel connector pins, with the transceiver connection through either one or two cables. You can connect the NI4010A directly to the transceiver with the NA4010-10 cable; or you can mate the NA4010-10 cable with the NA1010 cable, which then connects to the transceiver. The total length of cable between the NI4010A and its transceiver must not exceed 50 meters (165 feet).

> The NA4010-10 cable is a flat cable intended for flexible interconnection in an internal cabinet environment. Its length must not exceed 3 meters (10 feet).
>
> The NA1010 is a twisted-pair round cable. It has less loss than an equivalent length of flat cable.

The transceiver end of the NA4010-10 Flat Cable has a 15-pin D subminiature female connector with a slide lock assembly (Cinch type DA 51220-1). Figure 2-1 shows the pin assignments for this connector.



15 Position

Figure 2-1. NA4010-10 Transceiver Cable Connector (Transceiver End)

1	Shield (see note)		
2	Collision Presence +	9	Collision Presence -
3	Transmit +	10	Transmit -
4	Reserved (N/C)	11	Reserved (N/C)
5	Receive +	12	Receive -
6	Power Return	13	Power
7	Reserved (N/C)	14	Reserved (N/C)
8	Reserved (N/C)	15	Reserved (N/C)

N/C = no connection

NOTE: For proper electrical integrity and safety, the shield of the transceiver cable must be connected to the frame of the equipment enclosure, and the frame of the equipment enclosure must be connected to the safety ground (third wire) of the AC power line. The shield of the transceiver cable SHOULD NOT be connected to the NI4010A logic ground, only to the frame of the cabinet. To assist in making this frame connection, the NA4010-10 cable has an integral metal mounting bracket that is suitable for mounting on rack cabinets.

2.2.3 NI4010A Addresses

Interlan has assigned each NI4010A a unique physical address. You may assign the NI4010A up to 63 different multicast addresses.

2.2.3.1 NI4010A Physical Address

Each NI4010A has a unique 48-bit physical address. Interlan selected this address from within a contiguous block of ETHERNET physical addresses obtained from Xerox Corporation through their ETHERNET licensing arrangement. The NI4010A physical address is distinct from the physical address of any other station on any ETHERNET.

The NI4010A physical address resides in ROM, and cannot be altered. The board has a label displaying the factory programmed physical address. You can read the NI4010A physical address by using the Report Physical Address (025-027) commands described in Chapter 3.

The following are Interlan ETHERNET physical addresses:

	Physical Address Byte:	A	B	C	D	E	F
	start of physical address block:	02	07	01	00	00	00
	end of physical address block:	02	07	01	FF	FF	FF
(hexadecimal)							
	24 bits assigned by...	Xerox			Interlan		

2.2.3.2 Multicast Addresses

The ETHERNET Specification allows for multiple-destination addresses, associated with one or more stations on a given ETHERNET. There are two kinds of multicast addresses. They are:

* Multicast-group addresses. These are addresses associated by higher level convention with a group of logically related stations.

* The broadcast address. A predefined multicast address (a destination address of all ones) that specifies the set of all stations on a given ETHERNET.

The NI4010A recognizes the broadcast address and up to 63 user-assigned multicast addresses. See Chapter 3 for a complete description of how to use the NI4010A multicast address capability.

2.3 CONFIGURING THE NI4010A FOR THE HOST SYSTEM

Configuring the NI4010A for the host system involves:

* Setting the desired device codes.
* Setting the desired interrupt priority mask bit.
* Selecting the extended data channel map support, if desired.
* Changing the transceiver power connection, if needed.

2.3.1 NI4010A Factory Configuration

Each NI4010A has the following configuration when shipped from the factory:

The command device code is octal 46.

The receive device code is octal 47.

The interrupt maskout bit is decimal 12.

The extended data channel map functions are disabled.

Transceiver power is connected through I/O bus pins B87 and B88.

2.3.2 Setting the Device Code

The NI4010A uses two consecutive device codes for programmed I/O operation. The first device code corresponds to the command section of the NI4010A while the second device code corresponds to the receive section. The command device code is determined by the setting of DIP switch U45 on the NI4010A. You can select any even device code between octal 00 and 76, although you should be careful not to choose a device code that is used by another device. The receive device code will always be one greater than the selected command device code.

Switches 1-5 select the most significant 5 bits of the command device code. When a switch is ON, the corresponding device code bit is '0'. For example, to select octal device code 46, the switch should have

U45-1	DS0	OFF	'1'
U45-2	DS1	ON	'0'
U45-3	DS2	ON	'0'
U45-4	DS3	OFF	'1'
U45-5	DS4	OFF	'1'

Figure 2-2 shows the location of this DIP switch.

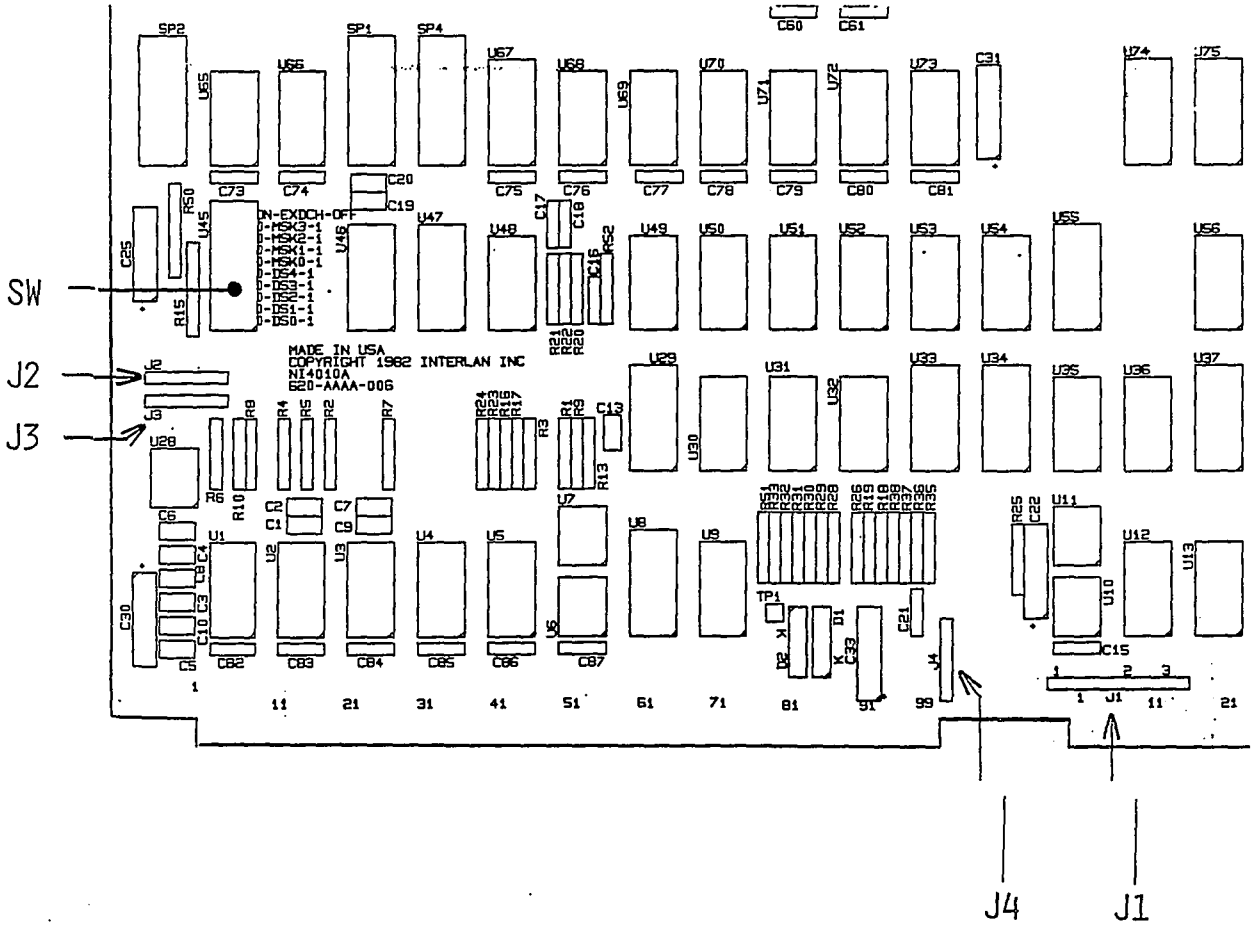


Figure 2-2. NI4010A DIP Switch and Jumper Locations

2.3.3 Setting the Interrupt Maskout Bit

You can select the interrupt maskout bit by DIP switch U45. You can select any of the sixteen possible bits. Switches 6-9 determine the selected interrupt maskout bit. When a switch is ON, that bit is '0'. For example, to select interrupt maskout bit 12 decimal, the switch should have

U45-9	MSK3	ON	'0'
U45-8	MSK2	ON	'0'
U45-7	MSK1	OFF	'1'
U45-6	MSK0	OFF	'1'

2.3.4 Enabling the Extended Data Channel Mapping

Some Data General host systems have extended data channel address support that can be used with special programming. The NI4010A supports this feature, but maintains compatibility with systems that do not have the extended data channel address support. If you wish to use this, turn switch U45-10 ON, otherwise leave it OFF. Additionally, you must insert jumper wires into locations J2, J3, and J4.

2.3.5 Selecting Transceiver Power Source

A wire jumper determines whether transceiver power will be taken from I/O bus pin A10 or from I/O bus pins B88 and B87. All newer Data General host systems supply the power on pins B88 and B87, and the NI4010A is factory configured as such. The NOVA 4 series, ECLIPSE S120, ECLIPSE S140, and all 32-bit ECLIPSE/MV computers are compatible with the factory configuration. If there is any doubt, you should examine the processor schematics to determine the transceiver power source. A wire jumper between J1-2 and J1-3 will take power from pins B88 and B87. A wire jumper between J1-1 and J1-2 will take power from pin A10.

2.4 DATA GENERAL SYSTEM INSTALLATION

2.4.1 Power Requirements

The NI4010A and the ETHERNET/IEEE-802 transceiver are powered directly from the host backplane and have the following power requirements. (see section 2.3.5)

+4.75 to +5.25 Vdc @ 6.5 A maximum (NI4010A board only)

+11.4 to +15.6 Vdc @ 0.5 A maximum (transceiver unit only)

The NI4010A provides power to the ETHERNET/IEEE-802 transceiver from the +12Vdc or +15Vdc power on the host backplane.

CAUTION: Before installing the NI4010A, verify that your power supply can satisfy the current requirements of the NI4010A and its transceiver. After installation, check that your power supply's +5Vdc and +12Vdc (or +15Vdc) voltages are still within the required levels.

2.4.2 Environmental Requirements

Interlan has designed the NI4010A to operate in a standard Data General host I/O bus slot. If you operate the NI4010A in free air (that is, without forced air flow across its surface) the ambient temperature must be below 25 degrees Celsius and the NI4010A must be placed away from objects that impede convective air flow.

You may operate the NI4010A in an environment with relative humidity up to 90%, provided that moisture does not condense on the board.

2.4.3 I/O Bus Priority Chains

In order to properly function, the NI4010A must be installed in a host I/O bus slot that has intact interrupt and data channel priority chains. If a blank slot is between the CPU and the NI4010A, then it must have jumpers on the interrupt and data channel priority chains. The interrupt chain propagates on I/O bus pins A95 and A96. The data channel priority chain propagates on I/O bus pins A93 and A94.

2.4.4 Transceiver Cable Backplane Installation

Pin 1 of the backplane connector of the flat transceiver cable (NA4010-10) must be connected to the host I/O bus pin A99. The backplane connector pushes onto the backplane wirewrap pins. Make sure the cable is installed on the correct slot. The chassis plate of the flat transceiver cable may be bolted to a convenient chassis rail, or may be connected directly to the transceiver.

2.5 NI4010A INSTALLATION CHECK LIST

Follow the steps on this checklist to make sure you have installed the NI4010A correctly.

1. Select device codes _____
2. Select interrupt maskout bit _____
3. Select extended data channel mapping _____
4. Select transceiver power source _____
5. Select a host I/O bus slot with intact interrupt and data channel priority chains _____
6. Check your power supply for adequate capacity _____
7. With the system power off, place the NI4010A in the selected host I/O bus slot _____
8. Connect the NA4010-10 flat cable to the host backpanel _____
9. Connect the flat cable (NA4010-10) to the transceiver, either directly or via the transceiver cable (NA1010 or equivalent) _____
10. Connect the transceiver to the ETHERNET/IEEE-802 coax cable _____

You are now ready to power up the NI4010A.

2.6 POWERING UP THE NI4010A

When power is applied to the NI4010A, the "LOOPBACK" LED should light for approximately one-half (0.5) second, then go out. If the "LOOPBACK" LED should stay lit, the NI4010A power-on self-test has failed. Refer to Chapter 5, Maintenance, for additional information.

Further verification of the NI4010A functionality may be performed by running the NI4010A standalone diagnostics (DS-NI4010A).

CHAPTER THREE

PROGRAMMING INFORMATION

3.1 OVERVIEW

This chapter tells you how to program the NI4010A Data General ETHERNET/IEEE-802 Communications Controller. It tells you:

* The formats for transmit data buffers and receive data buffers.
* How to use the program accessible registers.
* What the NI4010A commands do and how to issue them.
* What functions your host programs might perform.

The NI4010A is a high speed data channel device that is controlled by a simple programmed I/O (PIO) programming interface. Logically the NI4010A is split into separate command (including transmit) and receive sections with separate BUSY/DONE, interrupt, and data channel logic.

The NI4010A assumes a reset state after a power up reset, an IORST instruction, a Reset (377) command, or a Run Diagnostic (015) command. In the reset state, the NI4010A is in an off-line state and any traffic on the network will be ignored. From the reset state the NI4010A may be issued commands as described in the following sections.

Table 3-1
NI4010A COMMAND FUNCTION CODES

COMMAND CODE (octal)	COMMAND FUNCTION
000	Transmit Frame
001	Load Transmit Data
002	Load Physical Address
003	Load Group Address
004	Delete Group Address
005	Set Loopback Mode
006	Clear Loopback Mode
007	Set Promiscuous Mode
010	Clear Promiscuous Mode
011	Set Receive-On-Error Mode
012	Clear Receive-On-Error Mode
013	Go Offline
014	Go Online
015	Run Diagnostic
016	Set Insert-Source-Address Mode
017	Clear Insert-Source-Address-Mode
020	Set Default Physical Address
021	Set Receive-All-Multicast Frames
022	Clear Receive-All-Multicast Frames
023	Report Collision Retry Count
024	Report Collision Delay Time
025	Report Physical Address Word 1
026	Report Physical Address Word 2
027	Report Physical Address Word 3
030	Report and Reset Receive Count
031	Report Receive Buffer Frame Count
032	Report and Reset Transmit Count
033	Report and Reset Excess Collision Count
034	Report and Reset Collision Fragment Count
035	Report and Reset Receive Buffer Overflow Count
036	Report and Reset Multicast Accept Count
037	Report and Reset Multicast Reject Count
040	Report and Reset Collision Count
041	Report and Reset Out-of-Window Collision Count
042	Report Board Identification
043	Run Network Loopback Test
044	Run Collision Detect Test
045-376	Should Not Be Used
377	Reset

3.2 DATA FORMATS

This section describes the format of transmit and receive buffers in system memory.

3.2.1 Transmit Data Buffer in System Memory

The host transfers data to the NI4010A by setting up a transmit buffer in its own memory, writing the NI4010A command memory address register with the buffer starting address, writing the NI4010A command word count register with the buffer word count, and then initiating a transmit operation by issuing a transmit command to the NI4010A command register.

The host must set up that transmit buffer in a particular format. Figure 3-1 shows that format.

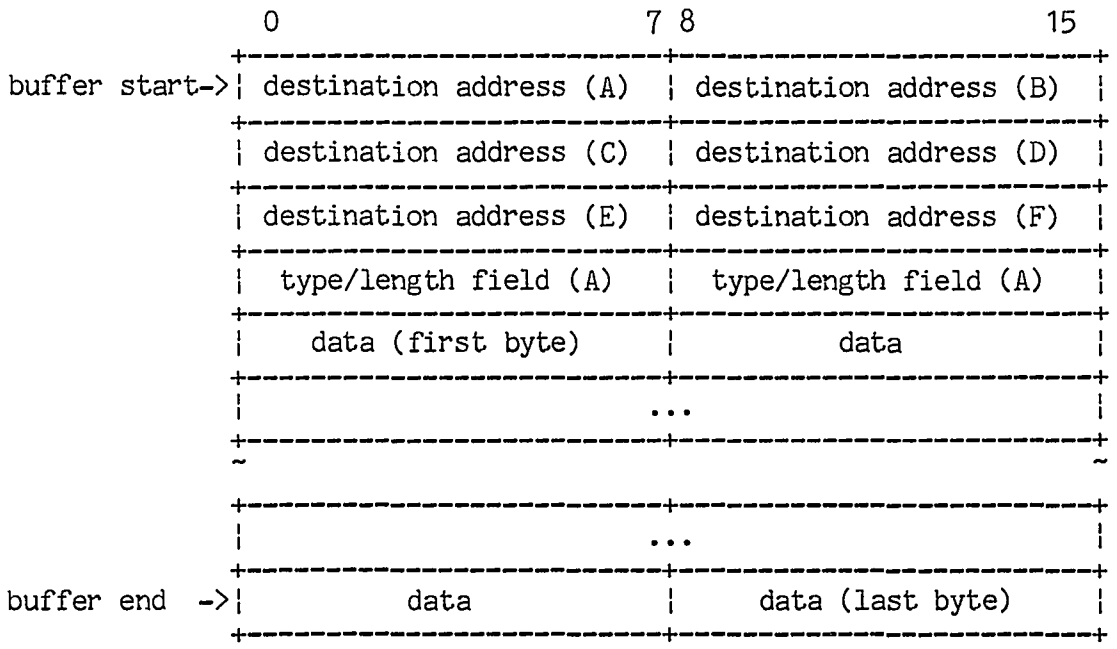


Figure 3-1

Transmit Data Buffer in Host Memory.
(source address insertion mode)

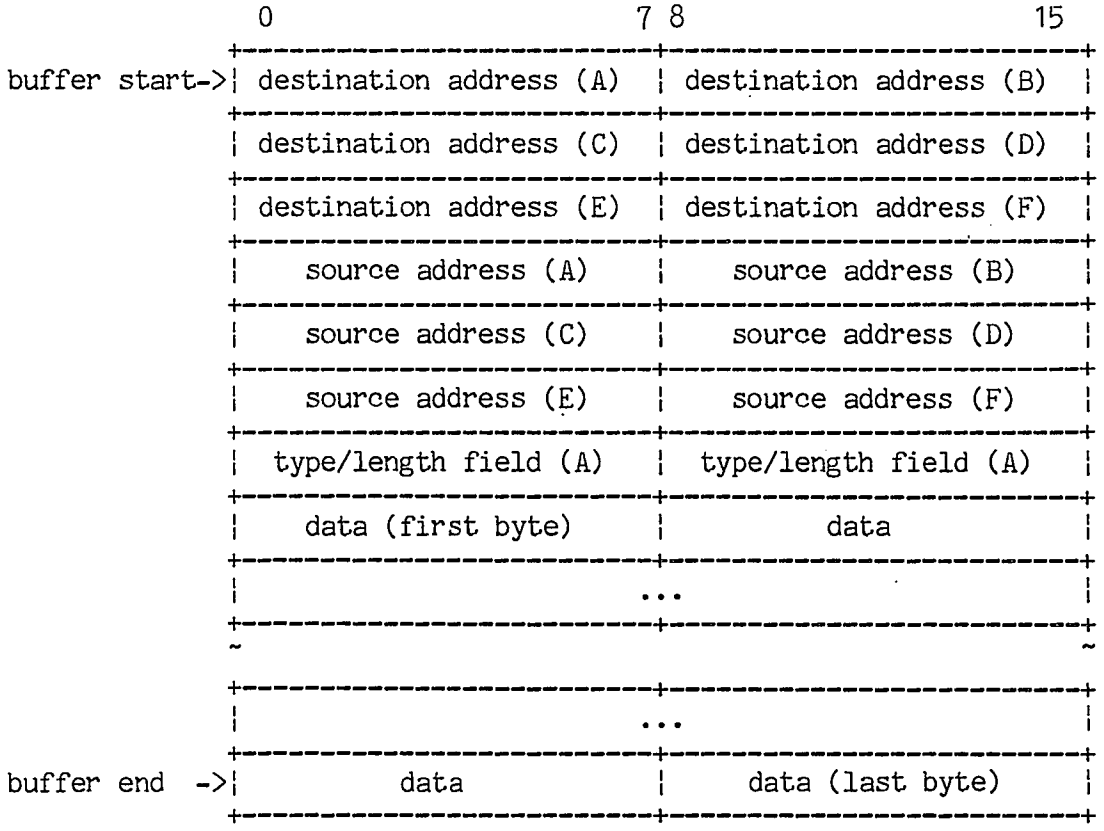


Figure 3-1a

Transmit Data Buffer in Memory
(not in source address insertion mode)

The minimum length of the data field in an ETHERNET/IEEE-802 frame is 46 bytes. If you supply less than this number, the NI4010A pads the data field with null characters to make 46 data bytes. A null character has all bits equal to 0. If you supply a transmit frame of less than 8 bytes (no data field and incomplete destination and type/length fields), the Transmit Frame command (000) returns a failure status code of 100006 indicating that the frame was too small.

The maximum length of the data field in an ETHERNET/IEEE-802 frame is 1500 bytes. If you supply a transmit frame of more than 1508 bytes (1500 data bytes plus 8 bytes for the destination and type fields), a Transmit Frame command (000) returns a failure status code of 100002 indicating that the frame was too large.

Only load the NI4010A transmit FIFO with one frame at a time. When you issue a Transmit Frame command (000), the NI4010A transmits all the data in its transmit FIFO as an ETHERNET/IEEE-802 frame. It adds the preamble, the source address (if in insert source address mode), and the CRC value.

3.2.2 Receive Data Format in System Memory

When the NI4010A receives an ETHERNET/IEEE-802 frame, it strips off the preamble and stores the rest of the frame in the NI4010A receive FIFO. The rest of the frame includes 6 bytes of destination address, 6 bytes of source address, 46 to 1500 bytes of data, and 4 bytes of CRC. The minimum receive frame is 64 bytes, and the maximum received frame is 1518 bytes.

The host transfers data from the NI4010A by setting up a receive buffer in its own memory, writing the NI4010A receive memory address register with the buffer starting address, writing the NI4010A receive word count register with the buffer word count, and then initiating a receive data channel operation by selecting the appropriate receive condition in the NI4010A receive condition register. When the data transfer is complete, the receive frame will be located in the host memory receive buffer. Figure 3-2 shows the receive frame format.

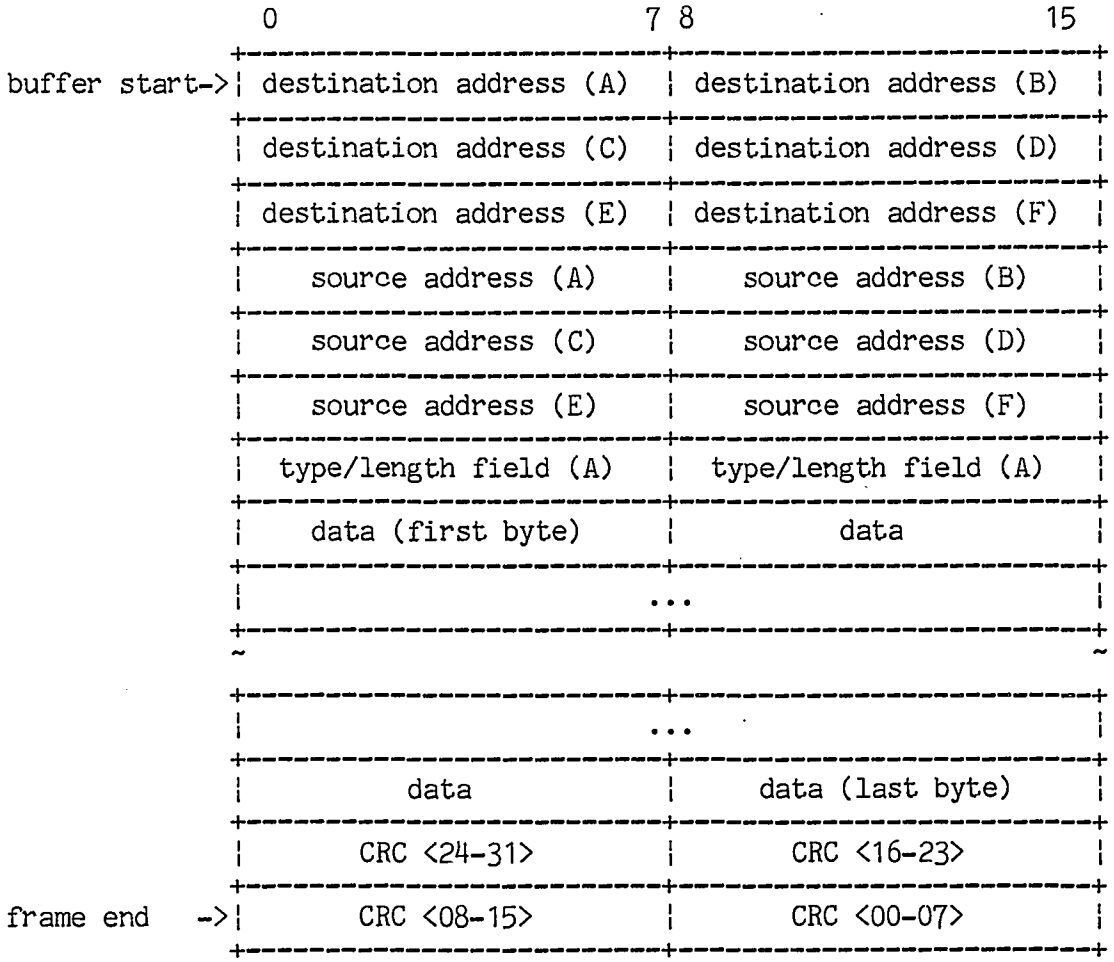


Figure 3-2

Receive Data Frame in System Memory

The CRC value is 32 bits (CRC<0:31>) long. The transmitting station sends the most significant bit of the CRC value (CRC<31>) first. In the received frame the CRC value appears as 4 bytes. The most significant byte appears first. Bit 0 of each CRC byte contains the most significant bit of that byte, and bit 7 contains the least significant bit.

3.3 THE NI4010A INTERNAL REGISTERS

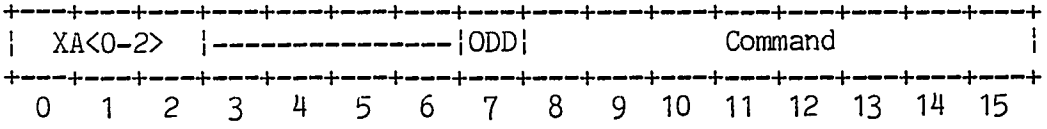
The NI4010A has eight program accessible internal registers:

Command Register
Command Memory Address Register
Command Word Count Register
Command Status Register
Receive Condition Register
Receive Memory Address Register
Receive Word Count Register
Receive Status Register

The host accesses the NI4010A internal registers by issuing the appropriate I/O instructions as explained in the following sections.

3.3.1 The Command Register

Specify Command (DOAS ac,46)



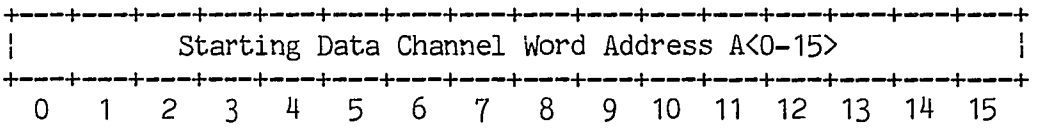
XA<0-2> - EXTENDED ADDRESS
The most significant 3 bits of the extended data channel address. These bits can be disabled from driving the I/O bus as described in section 2.3.4. Along with A<0-15>, they form a 19-bit starting data channel address for command operations.

ODD - ODD BYTE COUNT
If set, the number of words to be data channelled contains one extra byte that is not part of the frame.

COMMAND
This 8-bit field determines which command will be executed by the NI4010A. Command execution begins on the START pulse.

3.3.2 The Command Memory Address Register

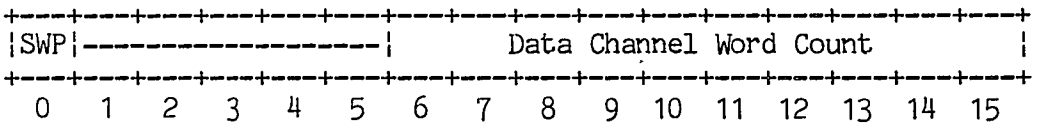
Load Command Memory Address Register (DOB ac,46)



This 16-bit field, along with XA<0-2>, determines a starting address for data channel operations. It must be loaded prior to issuing any command that will cause a command data channel operation.

3.3.3 The Command Word Count Register

Load Command Data Channel Word Count (DOC ac,46)

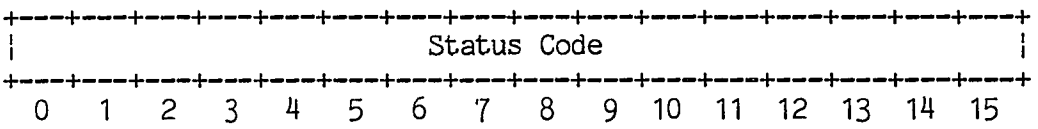


SWP - SWAP BYTES
If set to 1, the NI4010A will assume that the words transferred in a data channel operation will have the byte order swapped (ie: the first byte transmitted is from bits <8-15> and the second byte transmitted is from bits <0-7>). The normal byte ordering has the first byte transmitted from bits <0-7> and the second byte transmitted from bits <8-15>.

DATA CHANNEL WORD COUNT
This 10-bit field determines the size, in words, of the data channel buffer. It must be loaded prior to issuing any command that will cause a command data channel operation.

3.3.4 The Command Status Register

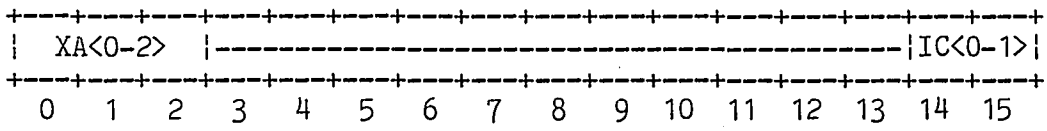
Read Command Status (DIA ac,46)



STATUS CODE - This 16-bit field contains the status returned from completion of a command.

3.3.5 The Receive Condition Register

Specify Receive Conditions (DOAS ac,47)



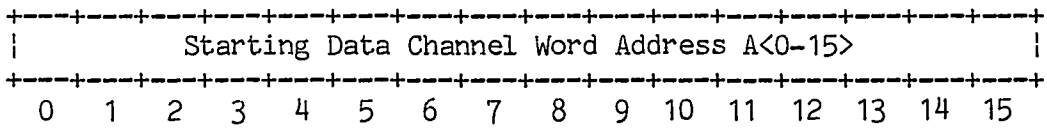
XA<0-2> - EXTENDED ADDRESS
The most significant 3 bits of the extended data channel address bits. These bits can be disabled from driving the I/O bus as described in section 2.3.4. Along with A<0-15>, they form a 19-bit starting data channel address for receive operations.

IC<0-1> - INTERRUPT CONDITION
This 2-bit field determines what conditions will cause the receive done bit to be set (with resultant interrupt if not masked out). Field values are:

IC<0-1>	Function
3	No action will be taken
2	Flush current receive frame
1	Set done when frame is available for transfer
0	Set done on data channel transfer complete

3.3.6 The Receive Memory Address Register

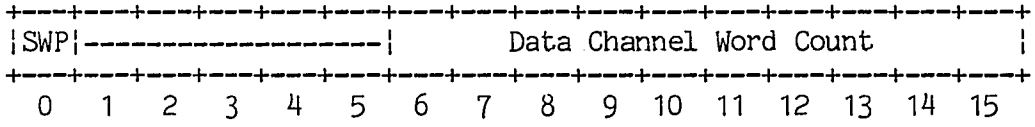
Load Receive Memory Address Register (DOB ac,47)



This 16-bit field, along with XA<0-2>, determines a starting address for data channel operations. It must be loaded prior to issuing a specify receive condition (DOAS ac,47) instruction that will cause a receive data channel operation.

3.3.7 The Receive Word Count Register

Load Receive Data Channel Word Count (DOC ac,47)

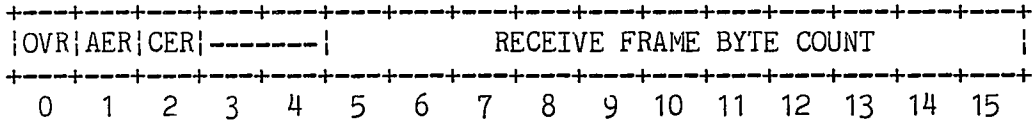


SWP - SWAP BYTES
If set to 1, the NI4010A will assume that the words transferred in a data channel operation will have the byte order swapped (ie: the first byte transmitted is from bits <8-15> and the second byte transmitted is from bits <0-7>). The normal byte ordering has the first byte transmitted from bits <0-7> and the second byte transmitted from bits <8-15>.

DATA CHANNEL WORD COUNT
This 10-bit field determines the size, in words, of the data channel buffer. It must be loaded prior to issuing a specify receive condition (DOAS ac,47) instruction that will cause a command data channel operation.

3.3.8 The Receive Status Register

Read Receive Status (DIA ac,47)



OVR - OVERRUN
If 1, indicates that a frame was unable to be received because the receive FIFO buffer was already filled.

AER - ALIGNMENT ERROR
If 1, indicates that the received frame has an alignment error. It will only be set if the NI4010A is in receive-on-error mode.

CER - CRC ERROR
If 1, indicates that the received frame has a CRC error. It will only be set if the NI4010A is in receive-on-error mode.

RECEIVE FRAME BYTE COUNT
The size in bytes of the received frame.

Note: Status is not valid if a receive operation is in progress (BUSY is set to 1). Status is only valid after the receive operation has completed.

3.4 NI4010A COMMAND DESCRIPTIONS

This section contains a complete description of each NI4010A command. Each command entry tell you:

* What the command does.
* How to issue the command.
* What status codes are possible and what they mean.
* The format of any related data.

3.4.1 Transmit Frame (000)

Description:

The Transmit Frame command moves a frame from host memory into the NI4010A and transmits the frame onto the network. On transmission the Transmit Frame command inserts the current NI4010A physical address into the frame's source address field if source address insertion mode is set. Transmit Frame always appends the CRC to the end of the data field. The NI4010A will, if necessary, pad the data field with nulls to create a minimum sized frame.

The Command Memory Address Register and the Command Word Count Register must have been loaded before issuing this command. If the frame contains an odd number of bytes, the "ODD" bit in the Command Register should be set to 1.

Sequence:

1. Assemble the frame in the host memory buffer.
2. Write the buffer's starting address into the Command Memory Address Register with a DOB ac,46 instruction.
3. Write the frame's word count into the Command Word Count Register with a DOC ac,46 instruction.
4. Write the Transmit Frame command into the Command Register with a DOAS ac,46 instruction.

Status:

000000	Success - frame transmitted with no collisions
000001	Success - frame transmitted with one or more collisions
100002	Failure - frame too large (exceeds 1508 bytes)
100003	Failure - excessive collisions
100004	Failure - transmit timeout (network failure)
100005	Failure - not in online or loopback mode
100006	Failure - frame too small (incomplete type field)

Format:

Refer to section 3.2.1 and figures 3-1 and 3-1a.

3.4.2 Load Transmit Data (001)

Description:

The Load Transmit Data command moves data from host memory into the NI4010A transmit FIFO buffer, but does not transmit the data onto the network. This command may be used to assemble a frame for transmission from several different host memory buffers. The Transmit Frame (000) command will cause the assembled frame to be transmitted.

The Command Memory Address Register and the Command Word Count Register must have been loaded before issuing the Load Transmit Data command. If the frame contains an odd number of bytes, the "ODD" bit in the Command Register should be set to 1.

Sequence:

1. Assemble the frame in the host memory buffer.
2. Write the buffer's starting address into the Command Memory Address Register with a DOB ac,46 instruction.
3. Write the frame's word count into the Command Word Count Register with a DOC ac,46 instruction.
4. Write the Load Transmit Data command into the Command Register with a DOAS ac,46 instruction.

Status:

000000 Success - data has been placed in the transmit buffer
100001 Failure - buffer size exceeded (more than 1508 bytes)

3.4.3 Load Physical Address (002)

Description:

The Load Physical Address command loads a user-specified Ethernet physical address into the NI4010A. The factory-programmed Ethernet physical address will not be used in processing subsequently received frames.

The Command Memory Address Register and the Command Word Count Register must have been loaded before issuing this command.

Sequence:

1. Place the desired physical address in the host memory buffer.
2. Write the buffer's starting address into the Command Memory Address Register with a DOB ac,46 instruction.
3. Write the buffer's word count of 000003 into the Command Word Count Register with a DOC ac,46 instruction.
4. Write the Load Physical Address command into the Command Register with a DOAS ac,46 instruction.

Status:

000000 Success - data supplied is now NI4010A's physical address
100001 Failure - data supplied not 6 bytes in length
100002 Failure - buffer size exceeded (more than 1508 bytes)

Format:

The byte ordering is specified in figure 3-1.

Notes:

The Load Physical Address (002) command is cancelled only by a power up reset, an IORST instruction, a Reset (377) command, a Run Diagnostic (015) command, or a Set Default Physical Address (020) command.

If source address insertion mode is set, the address specified by this command will be inserted as the source address of frames subsequently transmitted.

Different physical addresses may be loaded at any time by this command. Loading a new physical address while the NI4010A is or has been online may give bizarre results (ie: previously acceptable frames waiting in the receive FIFO buffer will be discarded prior to their delivery to a host receive buffer). This mode precludes Promiscuous mode operation.

3.4.4 Load Group Address (003)

Description:

The Load Group Address command loads multicast group address values into the NI4010A for multicast address recognition. The NI4010A will hold 64 values, including the broadcast address which is present after a power up reset, an IORST instruction, a Reset (377) command, or a Run Diagnostic (015) command. Received multicast frames are rejected if the corresponding address has not been loaded. The Command Memory Address Register and the Command Word Count Register must have been loaded before issuing this command.

Sequence:

1. Place the desired group address(es) in the host memory buffer.
2. Write the buffer's starting address into the Command Memory Address Register with a DOB ac,46 instruction.
3. Write the buffer's word count into the Command Word Count Register with a DOC ac,46 instruction.
4. Write the Load Group Address command into the Command Register with a DOAS ac,46 instruction.

Status:

000000	Success - address values supplied are loaded
100001	Failure - group address table full, some values loaded
100002	Failure - buffer size exceeded (more than 1508 bytes)
100003	Failure - buffer not on 6 byte alignment

Format:

The byte ordering is specified in figure 3-1.

3.4.5 Delete Group Address (004)

Description:

The Delete Group Address command removes selected multicast group address values from the NI4010A group address table. The broadcast address may be deleted using this command. The Command Memory Address Register and the Command Word Count Register must have been loaded before issuing this command.

Sequence:

1. Place the group address(es) that are to be deleted in the host memory buffer.
2. Write the buffer's starting address into the Command Memory Address Register with a DOB ac,46 instruction.
3. Write the buffer's word count into the Command Word Count Register with a DOC ac,46 instruction.
4. Write the Delete Group Address command into the Command Register with a DOAS ac,46 instruction.

Status:

000000 Success - address values supplied are deleted
000001 Success - one or more values had not been loaded
100002 Failure - buffer size exceeded (more than 1508 bytes)
100003 Failure - buffer not on 6 byte alignment

Format:

The byte ordering is specified in figure 3-1.

Notes:

The NI4010A does not support a "Flush Group Addresses" command. It is the user's responsibility to keep track of the current contents of the controller's multicast group address table.

3.4.6 Set Loopback Mode (005)

Description:

The Set Loopback Mode command causes the NI4010A to enter a data loopback mode where all frames transmitted by the host are looped back and appear as frames received. When in loopback mode, no frames are actually sent onto the network and no frames are received from the network. The received frames will not have valid CRC bytes, although no CRC error will be reported. The loopback LED indicator will be turned on while in loopback mode.

Sequence:

1. Write the Set Loopback Mode command into the Command Register with a DOAS ac,46 instruction.

Status:

000000 Success - NI4010A is now in loopback mode and offline

3.4.7 Clear Loopback Mode (006)

Description:

The Clear Loopback Mode command clears the data loopback mode previously set by the Set Loopback Mode command. The NI4010A is left in an offline state.

Sequence:

1. Write the Clear Loopback Mode command into the Command Register with a DOAS ac,46 instruction.

Status:

000000 Success - NI4010A is offline and not in loopback mode

3.4.8 Set Promiscuous Mode (007)

Description:

The Set Promiscuous Mode command permits the NI4010A to receive all valid frames which appear on the network, regardless of the value in the frame's destination address field. When in this mode the NI4010A will receive all of its own transmissions.

Sequence:

1. Write the Set Promiscuous Mode command into the Command Register with a DOAS ac,46 instruction.

Status:

000000 Success - NI4010A is in promiscuous mode

Note:

If a Load Physical Address command has been successfully completed, issuing a Set Promiscuous Mode command will have no effect. The board will deliver only those frames addressed to the loaded physical or multicast addresses.

3.4.9 Clear Promiscuous Mode (010)

Description:

The Clear Promiscuous Mode command restores the normal receive mode where the NI4010A only receives those frames which have a destination address value that matches either the NI4010A's physical address or one of the addresses in the group address table. The NI4010A enters this mode automatically after a power up reset, an IORST instruction, a Reset (377) command, a Run Diagnostic (015) command, or a set Default Physical Address command (020).

Sequence:

1. Write the Clear Promiscuous Mode command into the Command Register with a DOAS ac,46 instruction.

Status:

000000 Success - NI4010A is in normal receve mode

3.4.10 Set Receive-On-Error Mode (011)

Description:

The Set Receive-On-Error Mode command permits the NI4010A to receive frames with CRC errors and/or alignment errors. When not in this mode the NI4010A will discard all frames received with CRC and/or alignment errors.

Sequence:

1. Write the Set Receive-On-Error Mode command into the Command Register with a DOAS ac,46 instruction.

Status:

000000 Success - NI4010A is in receive-on-error mode

3.4.11 Clear Receive-On-Error Mode (012)

Description:

The Clear Receive-On-Error command causes the NI4010A to reject all frames received with CRC and/or alignment errors. The NI4010A enters this mode automatically after a power up reset, an IORST instruction, a Reset (377) command, or a Run Diagnostic (015) command.

Sequence:

1. Write the Set Receive-On-Error Mode command into the Command Register with a DOAS ac,46 instruction.

Status:

000000 Success - NI4010A will reject receive frames with errors

3.4.12 Go Offline (013)

Description:

The Go Offline command disconnects the NI4010A transmitter and receiver from the network. Receive frames pending in the receive fifo buffer are not affected by this command. The NI4010A enters the offline state automatically after a power up reset, an IORST instruction, a Reset (377) command, or a Run Diagnostic (015) command.

Sequence:

1. Write the Go Offline command into the Command Register with a DOAS ac,46 instruction.

Status:

000000 Success - NI4010A is offline

3.4.13 Go Online (014)

Description:

The Go Online command connects the NI4010A transmitter and receiver to the network. The NI4010A will begin receiving frames from the network, and will accept frames for transmission.

Sequence:

1. Write the Go Online command into the Command Register with a DOAS ac,46 instruction.

Status:

000000 Success - NI4010A is online

3.4.14 Run Diagnostic (015)

Description:

The Run Diagnostic command causes the NI4010A to execute an onboard diagnostic routine to test the NI4010A functionality. The NI4010A is left in an offline state after executing these diagnostics. During diagnostic execution, the LOOPBACK LED indicator will be turned on, and will turn off only if all tests have been successfully executed. The Run Diagnostic command will take approximately 3 seconds to execute.

Sequence:

1. Write the Run Diagnostic command into the Command Register with a DOAS ac,46 instruction.

Status:

000000	Success - diagnostic detected no faults
100001	Failure - ROM checksum failure
100002	Failure - RAM test failure
100003	Failure - Unable to read on-board Ethernet address
100004	Failure - Transmit/receive serial logic failure
100005	Failure - Transmit timeout (network failure)

3.4.15 Set Insert-Source-Address Mode (016)

Description:

The Insert-Source-Address Mode command causes the NI4010A to insert its current physical address value into the source address field of frames that are transmitted. The NI4010A enters this mode automatically after a power up reset, an IORST instruction, a Reset (377) command, or a Run Diagnostics (015) command.

Sequence:

1. Write the Set Insert-Source-Address Mode command into the Command Register with a DOAS ac,46 instruction.

Status:

000000 Success - NI4010A is in insert-source-address mode

3.4.16 Clear Insert-Source-Address Mode (017)

Description:

The Clear Insert-Source-Address Mode command causes the NI4010A to transmit frames as they appear in host memory (without inserting the source address) unless the data field needs null byte insertion.

Sequence:

1. Write the Clear Insert-Source-Address Mode command into the Command Register with a DOAS ac,46 instruction.

Status:

000000 Success - NI4010A will not insert source addresses

Note:

In this mode, 1514 bytes may be supplied to the board by a Transmit Frame command (000) or Load Transmit Data command (001) before a buffer size exceeded error is reported. This enables the user to transmit maximum length frames when suppling the source address.

3.4.17 Set Default Physical Address (020)

Description:

The Set Default Physical Address command causes the NI4010A to use its factory programmed Ethernet address, cancelling the effect of any other physical address previously loaded by the user. The NI4010A enters this state automatically after a power up reset, an IORST instruction, a Reset (377) command, or a Run Diagnostics (015) command.

Sequence:

1. Write the Set Default Physical Address command into the Command Register with a DOAS ac,46 instruction.

Status:

Possible status returns are:

000000 Success - NI4010A using factory programmed address

Note:

The board will not be in Promiscuous Mode after execution of this command.

3.4.18 Set Receive-All-Multicast Frames (021)

Description:

The Set Receive-All-Multicast Frames command allows the NI4010A to receive all frames from the network whose destination addresses are multicast.

Sequence:

1. Write the Set Receive-All-Multicast Frames command into the Command Register with a DOAS ac,46 instruction.

Status:

Possible status returns are:

000000 Success - NI4010A will receive all multicast frames

3.4.19 Clear Receive-All-Multicast Frames (022)

Description:

The Clear Receive-All-Multicast Frames command causes the NI4010A to only receive multicast frames whose destination address matches one of those previously loaded in the group address table. The NI4010A enters this state automatically after a power up reset, an IORST instruction, a Reset (377) command, or a Run Diagnostic (015) command.

Sequence:

1. Write the Clear Receive-All-Multicast Frames command into the Command Register with a DOAS ac,46 instruction.

Status:

000000 Success - NI4010A will filter receive multicast frames

3.4.20 Report Collision Retry Count (023)

Description:

The Report Collision Retry Count command returns as status the number of retransmission attempts that were made as the result of the most recently issued Transmit Frame (000) command.

Sequence:

1. Write the Report Collision Retry Count command into the Command Register with a DOAS ac,46 instruction.

Status:

000000 to 000020 - number of retransmission attempts

3.4.21 Report Collision Delay Time (024)

Description:

The Report Collision Delay Time command returns as status the number of bits that were transmitted onto the network before a collision occurred. The value is the result of the most recent collision resulting from a Transmit Frame (000) command.The value returned is for the last transmission attempt. This value can be used for locating Ethernet cable faults to within 8 meters.

Sequence:

1. Write the Report Collision Delay Time command into the Command Register with a DOAS ac,46 instruction.

Status:

number of bits transmitted before collision

3.4.22 Report Physical Address Word 1 (025)

Decription:

The Report Physical Address Word 1 command returns as status the A and B bytes of the NI4010A current physical address.

Sequence:

1. Write the Report Physical Address Word 1 command into the Command Register with a DOAS ac,46 instruction.

Status:

bytes A (bits 0-7) and B (bits 8-15) of the physical address

3.4.23 Report Physical Address Word 2 (026)

Decription:

The Report Physical Address Word 2 command returns as status the C and D bytes of the NI4010A current physical address.

Sequence:

1. Write the Report Physical Address Word 2 command into the Command Register with a DOAS ac,46 instruction.

Status:

bytes C (bits 0-7) and D (bits 8-15) of the physical address

3.4.24 Report Physical Address Word 3 (027)

Decription:

The Report Physical Address Word 3 command returns as status the E and F bytes of the NI4010A current physical address.

Sequence:

1. Write the Report Physical Address Word 3 command into the Command Register with a DOAS ac,46 instruction.

Status:

bytes E (bits 0-7) and F (bits 8-15) of the physical address

3.4.25 Report and Reset Receive Count (030)

Description:

The Report and Reset Receive Count command returns as status the number of frames that have been received from the network. The count will be reset to zero after execution of this command.

Sequence:

1. Write the Report and Reset Receive Count command into the Command Register with a DOAS ac,46 instruction.

Status:

16 bit unsigned count of the number of received frames

3.4.26 Report Receive Buffer Frame Count (031)

Description:

The Report Receive Buffer Frame Count command returns as status the number of receive frames currently in the receive FIFO buffer. A frame that is in the process of being transferred to host memory is included in this count. All received multicast frames are included in this count, even though they may be rejected by the multicast filtering.

Sequence:

1. Write the Report Receive Buffer Frame Count command into the Command Register with a DOAS ac,46 instruction.

Status:

16 bit unsigned count of the number received frames in buffer

3.4.27 Report and Reset Transmit Count (032)

Description:

The Report and reset Transmit Count command returns as status the number of frames that have been transmitted onto the network by the NI4010A. The count will be reset to zero after execution of this command.

Sequence:

1. Write the Report and Reset Transmit Count command into the Command Register with a DOAS ac,46 instruction.

Status:

16 bit unsigned count of the number of transmitted frames

3.4.28 Report and Reset Excess Collision Count (033)

Description:

The Report and Reset Excess Collision Count command returns as status the number of times a transmit frame incurred sixteen successive collisions when attempting to transmit onto the network. The count will be reset to zero after execution of this command.

Sequence:

1. Write the Report and Reset Excess Collision Count command into the Command Register with a DOAS ac,46 instruction.

Status:

16 bit unsigned count of the number of excess collisions

3.4.29 Report and Reset Collision Fragment Count (034)

Description:

The Report and Reset Collision Fragment Count command returns as status the number of collision fragments ("runt frames") that were received and discarded by the NI4010A. The count will be reset to zero after execution of this command.

Sequence:

1. Write the Report and Reset Collision Fragment Count command into the Command Register with a DOAS ac,46 instruction.

Status:

16 bit unsigned count of the number of collision fragments

3.4.30 Report and Reset Receive Buffer Overflow Count (035)

Description:

The Report and Reset Receive Buffer Overflow Count command returns as status the number of frames on the network that could not be received because the receive FIFO buffer did not have sufficient space available for an incoming frame. The count will be reset to zero after execution of this command.

Sequence:

1. Write the Report and Reset Receive Buffer Overflow Count command into the Command Register with a DOAS ac,46 instruction.

Status:

16 bit unsigned count of the number of lost frames

3.4.31 Report and Reset Multicast Accept Count (036)

Description:

The Report and Reset Multicast Accept Count command returns as status the number of multicast frames that have been received from the network and transferred into host memory. The count will be reset to zero after execution of this command.

Sequence:

1. Write the Report and Reset Multicast Accept Count command into the Command Register with a DOAS ac,46 instruction.

Status:

16 bit unsigned count of the number of accepted multicast frames

3.4.32 Report and Reset Multicast Reject Count (037)

Description:

The Report and Reset Multicast Reject Count command returns as status the number of multicast frames that have been received from the network but rejected because the address value did not match any value in the group address table. The count will be reset to zero after execution of this command.

Sequence:

1. Write the Report and Reset Multicast Reject Count command into the Command Register with a DOAS ac,46 instruction.

Status:

16 bit unsigned count of the number of rejected multicast frames

3.4.33 Report and Reset Collision Count (040)

Description:

The Report and Reset Collision Count command returns as status the number of transmission attempts that resulted in collisions. The count will be reset to zero after execution of this command.

Sequence:

1. Write the Report and Reset Collision Count command into the Command Register with a DOAS ac,46 instruction.

Status:

16 bit unsigned count of the number of collisions

3.4.34 Report and Reset Out-Of-Window Collision Count (041)

Description:

The Report and Reset Out-Of-Window Collision Count command returns as status the number of transmission attempts that resulted in collisions that were outside of the Ethernet slot time. These collisions occur only if a network node is not deferring correctly. The count will be reset to zero after execution of this command.

Sequence:

1. Write the Report and Reset Out-Of-Window Collision Count command into the Command Register with a DOAS ac,46 instruction.

Status:

16 bit unsigned count of the number of out-of-window collisions

3.4.35 Report Board Identification (042)

Description:

The Report Board Identification command returns as status two ASCII bytes (letter and number) that identify the board type and revision.

Sequence:

1. Write the Report Board Identification command into the Command Register with a DOAS ac,46 instruction.

Status:

ASCII letter (bits 0-7) and ASCII number (bits 8-15)

3.4.36 Run Network Loopback Test (043)

Description:

The Run Network Loopback Test command attempts to send two frames onto the network and verify correct reception.

Sequence:

1. Write the Run Network Loopback Test command into the Command Register with a DOAS ac,46 instruction.

Status:

000000	Success - NI4010A can transmit to and receive from the network
000001	Success - NI4010A detected a collision while transmitting onto the network
100002	Failure - NI4010A is not ONLINE or in LOOPBACK mode
100003	Failure - more than 16 collisions occurred while attempting to transmit on the network
100004	Failure - transmit timeout (network failure)
100005	Failure - transmit timeout in loopback (network failure)
100006	Failure - No CRC error detected on bad frame
100007	Failure - Data error in received frame
100010	Failure - CRC error detected on good frame

3.4.37 Run Collision Detect Test (044)

Description:

The Run Collision Detect Test command will transmit a frame onto the network and verify the presence of the collision test ("heartbeat") signal from the transceiver.

Sequence:

1. Write the Run Collision Detect Test command into the Command Register with a DOAS ac,46 instruction.

Status:

000000	Success - collision test signal was detected
000001	Success - collision test signal was detected after retry
100002	Failure - NI4010A is not in online state
100003	Failure - more than 16 collisions occured while testing
100004	Failure - transmit timeout (network failure)
100005	Failure - collision test signal was not detected

3.4.38 Reserved (045 to 376)

Description:

These command codes should not be issued.

3.4.39 Reset (377)

Description:

The Reset command initializes the NI4010A. Some on-board diagnostics are executed and status is returned. The Reset command executes in approximately 1/2 (0.5) seconds. After the Reset, the following states are assumed by the NI4010A:

Offline - NI4010A transmitter and receiver are disconnected from the network.
Normal Receive - only frames with destination addresses that match the NI4010 factory assigned physical address, or have the broadcast address will be received.
Source Address Insertion - the NI4010A will insert the source address into transmitted frames.
All statistical counters are reset to zero

Sequence:

1. Write the Reset command into the Command Register with a DOAS ac,46 instruction.

Status:

000000 Success - NI4010A has been initialized
100001 Failure - ROM checksum failure
100002 Failure - RAM test failure
100003 Failure - Unable to read on-board ETHERNET address

3.5 NI4010A PROGRAMMING

3.5.1 Issuing an NI4010A Command

To give a command to the NI4010A, use the DOA assembly language instruction in the following format:

```
DOAS ac,46;
```

where ac is the accumulator containing the NI4010A command code.

The receipt of the START pulse will cause BUSY to be set to 1 and DONE to be cleared to 0. The NI4010A will execute the specified command and return status.

To read the status, use the DIA assembly language instruction in the following format:

```
DIAS ac,46;
```

Where ac is the accumulator that will contain the NI4010A status code.

When the status is available, BUSY will be cleared to 0 and DONE will be set to 1. An interrupt will be given when DONE is set to 1 if the command section is not masked out. The CLEAR pulse will clear BUSY to 0 and clear DONE to 0.

Some command codes require that the command memory address and word count registers be loaded by the DOB ac,46 and DOC ac,46 instructions before the DOAS ac,46 command is issued.

Commands should be issued in sequence and a command should not be issued until a previous command has finished. If a second command is given (in error) before a previous command has finished(i.e. BUSY set to 1, DONE set to 0),it may give unexpected results.

3.5.2 Transmitting Data to the Network

Before you initiate transmit activity you must set the NI4010A to the desired transmit mode by issuing the appropriate commands as described in section 3.4. Once the transmitter is enabled with the Go Online (014) command, you can transmit frames using the Transmit Frame (000) command.

There are two basic methods of frame transmission.

1. The simplest method is to assemble the entire transmit frame in a host memory buffer using the format described in section 3.2.1. Then issue a Transmit Frame (000) command as described in section 3.4.1. The host memory buffer will be data channelled into the NI4010A transmit buffer, will be checked for size, and will then be transmitted onto the network. Status will be returned when the transmit is complete.

2. The second method of frame transmission involves using several host memory buffers. Different pieces of the entire transmit frame may be concatenated together in the NI4010A transmit buffer by using the Load Transmit Data (001) command as described in section 3.4.2. The assembled frame may then be transmitted using the Transmit Frame (000) command.

   This method of frame transmission may be useful where the header of a frame resides in one place (ie: a network server program) and the data portion of the frame resides in a user buffer. In this case, no programmed block moves would be required to assemble the transmit frame. The Transmit Frame (000) command may be given a buffer word count of zero, in which case the existing contents of the NI4010A transmit buffer will be sent with no additional data channel transfers.

3.5.3 Receiving Data from the Network

Before initiating receive activity you must set the NI4010A to the desired receive modes by issuing the appropriate commands as described in section 3.4. Once the receiver is enabled with the Go Online (014), the NI4010A can receive command frames from the network and put them into the receive FIFO buffer.

To initiate receive activity, a DOAS ac,47 instruction is executed with the desired interrupt condition field. If the field is set to a value of 0 (to enable a data channel), then the data channel address and word count registers should have been previously loaded by the DOB ac,47 and DOC ac,47 instructions. The receipt of the START pulse will cause BUSY to be set to 1 and DONE to be cleared to 0. The NI4010A will execute the specified receive operation and will return receive status that can be read with a DIAC ac,47 instruction. When the status is available, BUSY will be cleared to 0 and DONE will be set to 1. An interrupt will be given when the DONE bit is set to 1 if the device is not masked out. When status is read, the CLEAR pulse will clear BUSY to 0 and clear DONE to 0. No action will be taken until at least one frame is available in the receive FIFO for delivery to the host.

The receive interrupt condition field creates a flexible software interface, allowing the driver to optimize system software performance. Three methods for handling receive frames are described:

1. For minimum interrupt overhead, the interrupt condition field should be set to a 0 to enable a data channel when a frame becomes available. When a frame is received, the NI4010A will initiate the data channel transfer and generate an interrupt when the transfer is complete. The transfer is complete when either the entire frame has been transferred or the buffer size as specified by the data channel word count has been filled.

2. For maximum control over when data channel activity will occur, the interrupt condition field should first be set to a 1 to cause an interrupt when a frame is received from the network but before a data channel transfer has occurred. The data channel transfer can then be set up as described in (1) above.

3. A single received frame can be "chained" into more than one buffer by setting up several data channel transfers with word counts that are less than the frame byte size. This is very useful when sorting received frames by type field (or other fields). For example, the address and type fields can be transferred into a buffer that resides in the driver area. The driver could then examine the type field to determine which of several tasks would be the final recipient of the frame. The remainder of the frame could then be transferred directly into the task area.

The "flush current receive frame" interrupt condition code can be used to discard the remainder of a frame. This can be useful when sorting frames as described in (3) above. After transferring in a part of a received frame and sorting on that part, the remainder of the frame can be discarded if it is not needed.

To terminate any current receive activity, a NIOC ac,47 instruction should be issued. The CLEAR pulse will clear BUSY to 0 and clear DONE to 0. IF a data channel transfer is in process when Clear pulse is issued,the transfer will complete but no interupt will be generated. An IORST command is the only way to immediately terminate a data channel transfer in progress. This also destroys all information on the board. A Go Offline (013) command should then be executed to ensure that network activity is completed.

3.6 ETHERNET/IEEE-802 Frame Format

An ETHERNET frame consists of five fields;

1) The destination address field

2) The source address field

3) The type field

4) The data field

5) Frame check sequence (FCS)

For receive synchronization purposes, the frame is preceeded by a 64-bit preamble sequence and terminated by a minimum interframe spacing period of 9.6 microseconds. Figure 3-3 illustrates the format of an ETHERNET frame.

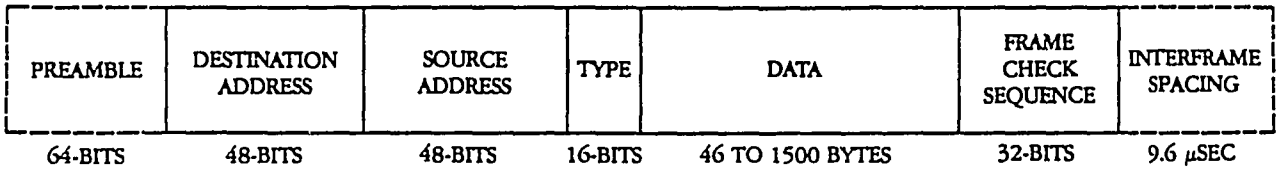


Figure 3-1

ETHERNET/IEEE-802 Frame Format

The NI4010A handles both ETHERNET and the IEEE-802.3 frame format. The IEEE-802.3 frame format is identical to that shown in Figure 3-1 except for the following definitions:

* Instead of a type field value, the user specifies a 16-bit length value for the frame.

* At the first three bytes of the data field, the user specifies a Destination Service Access Point (DSAP), Source Service Access Point (SSAP), and Control field.

3.6.1 Destination Address Field

The destination address specifies the station(s) for which the frame is intended. The address value provided by the user may be either:

1. The physical address of a particular station on the network.

2. A multicast-group address associated with one or more stations on the network.

3. The broadcast address for simultaneous transmission to all stations on the network. The first bit of the destination address distinguishes a physical address from a multicast address (0 = physical, 1 = multicast). For broadcast transmissions an all one-bit pattern is used.

An ETHERNET address consists of six bytes, labeled A, B, C, D, E, and F. The NI4010A transmits them in that order. It transmits the least significant bit of each byte first. The least significant bit of byte A distinguishes a physical address from a multicast address. This bit is 0 for a physical address and 1 for a multicast address. Note that a physical address has an even number in byte A, and a multicast address has an odd number in byte A.

3.6.2 Source Address Field

The source address field specifies the physical address of the transmitting station. To eliminate the possibility of an addressing ambiguity on a network, each NI4010A has a unique 48-bit default physical address value built into it at the time of manufacture. On transmission, this address value (if in insert-source-address mode) is inserted into the source address field of the frame. The NI4010A physical address may be changed with the Load Physical Address (002) command.

3.6.3 Type Field

You the user,can use the ETHERNET frame type field to communicate with the higher level protocols. This field is used by the receiving station(s) to determine how the content of the data field should be interpretted.

3.6.4 Data Field

The data field may contain a variable number of data bytes ranging from a minimum of 46 bytes to a maximum of 1500 bytes.

Should less than 46 bytes of data be provided to the controller for transmission, the NI4010A will automatically insert null characters to complete the 46-byte minimum frame size. A null character is a byte, each bit of which is 0.

The other fields of an ETHERNET frame total 18 bytes. Hence, the minimum size of a frame is 64 bytes, and the maximum size is 1518 bytes. The NI4010A refuses to transmit a frame that exceeds 1518 bytes. It returns an octal status code of 100002, indicating that the host supplied an over-sized frame.

3.6.5 Frame Check Sequence Field

The last field of the frame is the frame check sequence (FCS). This field contains a 32-bit, cyclic redundancy check (CRC) value generated by the NI4010A controller's bit-stream logic during transmission. The NI4010A includes the destination address, the source address, the type, and the data fields (along with any inserted zeros) in its CRC calculation.

CHAPTER FOUR

FUNCTIONAL DESCRIPTION

This chapter contains a functional description of the NI4010A Data General ETHERNET/IEEE-802 Communications Controller. It describes the NI4010A architecture, functional description, ETHERNET/IEEE-802 frame format, transmit process, receive process, diagnostic tools, and performance.

4.1 NI4010A BOARD ARCHITECTURE

4.1.1 Physical Description

The NI4010A is a single board that occupies one I/O bus slot in the Data General host computer. It is a four layer printed circuit board that fits in any 15 inch form factor Data General computer. The connection to the transceiver is through the I/O bus backpanel connector. Handles allow easy board insertion and removal, and a stiffener helps reduce board flexure.

4.1.2 Functional Overview

The NI4010A uses a bit-slice controller design to implement ETHERNET physical and data link operations. The interface is partitioned into five major functional blocks: 1) microprocessor, 2) network receive interface, 3) network transmit interface, 4) host programmed I/O interface, and 5) host data channel interface. All five blocks communicate over an 8-bit wide local data bus. Figure 4-1 is a block diagram of the NI4010A:

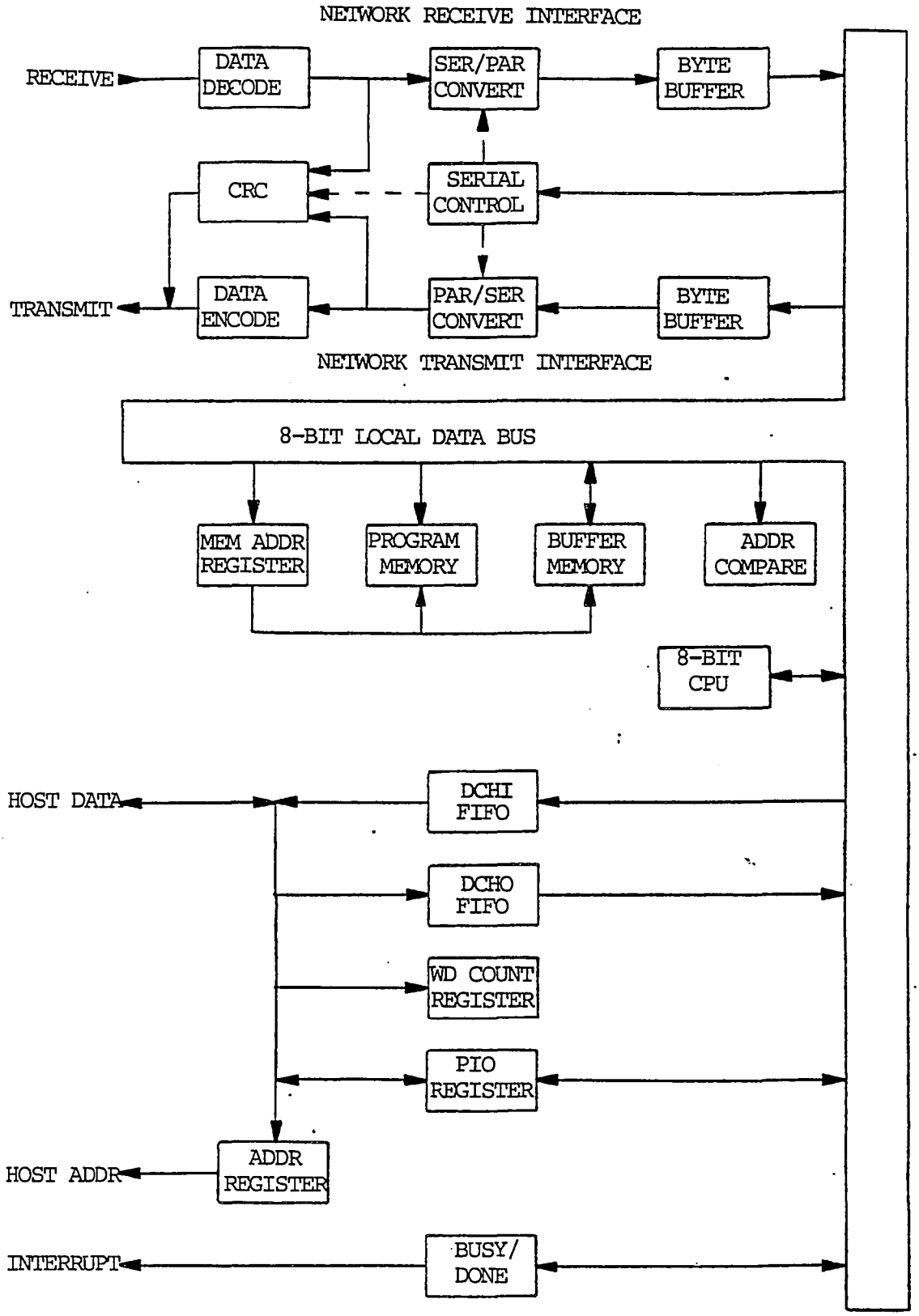


Figure 4-1. NI4010A Block Diagram

4.2 NI4010A Detailed Functional Description

4.2.1 Microprocessor

The microprocessor section is made up of 5 functional sections which control the network interfaces, the I/O bus interface, all data movements, and any processing functions.

The CPU is constructed out of bipolar bit-slice 2901 chips, and has an 8-bit instruction and data path width. A 4kbyte EPROM provides macro-instructions which execute the less time critical functions. A 512 word 56-bit wide bipolar PROM microcode store implements the macro-instruction set as well as any time critical functions. Micro-control is implemented with 2911 micro-sequencers. Micro-instruction cycle time is 200ns, and is implemented with one level of pipelining. The basic macro-instruction execution time is 1.6 us. The macro-instruction set is a subset of the Z-80 instruction set, with added instructions for implementing NI4010A specific functions.

The memory address register is a 16-bit wide auto-incrementing register that generates the addresses for buffer ram or program memory accesses. A one deep stack is included for storage of the program counter during time critical block data transfers on transmit or receive operations.

The buffer ram is 16K bytes in size, and is split into three areas: 1) 1.0 kb of scratchpad, 2) 1.5 kb of transmit buffer, and 3) 13.5 kb of receive buffer.

The program memory is a 4kbyte EPROM that contains the macro-code to control the NI4010A operation. It is addressed by the memory address register.

The address compare section implements hardware address checking for receive operations. As receive data bytes are being transferred on the data bus, they are compared against the NI4010A physical address.

4.2.2 Network Receive Interface

The network receive interface block is made up of 4 functional sections which handle network reception and error checking.

Receive data from the transceiver is decoded into a clock line and a data line by the data decode section. This decoded data is fed into a serial to parallel converter which assembles the bit stream into 8-bit bytes. The ser/par convert section also synchronizes the data to the microprocessor timing. The bytes of receive data are loaded into a register, which stores the data until the microprocessor can transfer it into the buffer ram. Decoded data from the data decode block is also fed into the CRC section which performs error checking on the received bit stream.

4.2.3 Network Transmit Interface

The network transmit interface block is made up of 3 functional sections which handle network transmission and error checking.

Transmit data bytes are transferred from the buffer ram into the parallel to serial converter by the microprocessor. The par/ser convert section changes the bytes of data into a bit stream that is synchronized with the system clock. This bit stream is encoded by the data encode block and is sent to the transceiver. The bit stream from the par/ser convert block is also sent to the CRC section which calculates the frame check sequence. The CRC section appends the frame check sequence to the end of the bit stream from the par/ser convert section for transmission to the transceiver.

The sequencing of operations in the receive, CRC, and transmit blocks is performed by the bit logic control block. The bit logic control block is controlled by the processor, which can write command and mode information to it, and can read status information from it.

4.2.4 Host Programmed I/O Interface

The NI4010A programmed I/O interface consists of two sections with separate BUSY/DONE, interrupt, and data channel logic.

Each section has four program accessible registers as described in section 3.3. The microprocessor can access the DOA and DIA registers a byte at a time over the 8-bit internal data bus. When the program writes into the command register, the microprocessor is interrupted to perform the specified command.

Each section has BUSY/DONE logic which is controlled by the START and CLEAR instructions, as well as by the microprocessor. There is one interrupt priority maskout bit that can be used to disable both DONE flags from requesting an interrupt. When the microprocessor returns status from a command, the BUSY flag is cleared to 0 and the DONE flag is set to 1.

4.2.5 Host Data Channel Interface

The data channel interface also consists of two sections with separate data channel logic for the command and receive sections. Each data channel section has a memory address register, word count register, and FIFO. The memory address registers are 19-bit counters that generate the data channel addresses. The word count registers are 10-bit counters that keep track of how many words are transferred.

The four word deep data channel FIFO's buffer the data channel transfers to and from the host I/O bus. They appear to the microprocessor as 8 byte deep FIFO's.

4.3 NI4010A Transmit Process

The NI4010A transmit process consists of obtaining frames from the host memory, forming them into ETHERNET/IEEE-802 frames, delivering them to the network, and returning status.

The NI4010A performs the specified ETHERNET/IEEE-802 data link and physical layer functions required to form and transmit a frame at 10 Megabits per second.

4.3.1 Transmit Data Channel Transfer

Upon receipt of the Transmit Frame (000) command, the microprocessor will initiate the data channel. It will transfer bytes from the data channel out FIFO to the transmit FIFO buffer until the data channel word count reaches zero. The microprocessor checks that the amount of data transferred does not exceed the size of the transmit FIFO buffer.

4.3.2 Frame Assembly

The microprocessor checks the frame size and puts the 64-bit preamble at the beginning of the frame. The microprocessor also inserts the NI4010A source address (if in insert-source-address mode) in the source address field. At this point the frame is ready to be transmitted. The CRC logic generates a CRC value as the frame is transmitted onto the network which is appended onto the frame. The NI4010A creates a self-synchronizing bit stream through Manchester encoding of the transmitted data.

4.3.3 Channel Access

The NI4010A monitors the network and defers transmission if the network is busy with other traffic. When the network becomes available, the NI4010A continues to defer transmission for 9.6 additional microseconds, thus providing the proper interframe spacing.

If another station transmits while the NI4010A is transmitting, a collision occurs. The NI4010A detects this collision and generates a jam signal. That means it stops transmitting data and transmits instead between 32 and 48 zeros before terminating transmission completely. The jam guarantees that all stations on the network detect the occurrence of the collision. The collision fragment is called a runt frame.

When the NI4010A stops transmitting because of a collision, it waits a short period of time before attempting to transmit the frame again. The NI4010A determines this rescheduling of transmission by an ETHERNET/IEEE-802 process called "truncated binary exponential backoff."

The NI4010A attempts to transmit a frame 16 times before reporting an error.

4.4 NI4010A Receive Process

The NI4010A receive process consists of receiving data from the network into the receive FIFO buffer, deciding whether to accept the data, formatting the data into frames, and transferring accepted frames to the host memory. The NI4010A deletes unaccepted frames from its receive FIFO.

The NI4010A performs the specified ETHERNET/IEEE-802 data link and physical layer functions required to receive a frame from the network at 10 Megabits per second.

4.4.1 Checking the Destination Address

When receiving a frame, the NI4010A synchronizes to and removes the preamble. Then, it separates (by Manchester decoding) the incoming bit stream into a receive data stream and a clock line. The bit stream is assembled into bytes, which are then transferred by the microprocessor into the receive buffer FIFO.

If the NI4010A is in promiscuous mode, it accepts the frame no matter what its destination address is. If the NI4010A is not in promiscuous mode, it tests the destination address field and accepts the frame if the destination address matches; 1) the broadcast address, 2) the NI4010A physical address, or 3) one of the 63 multicast addresses that the user may have assigned to the NI4010A.

4.4.2 Collision Fragment Filtering

Since collisions are a normal (although infrequent) occurrence on the network, the NI4010A CSMA/CD link management process filters out collision fragments by rejecting all received frames that are less than 64 bytes in length.

4.4.3 Error Checking

The NI4010A receives the FCS field and compares this value against the internally generated value. The user can set up the NI4010A to either accept or reject a frame with a CRC error. The normal receive mode is to reject error frames.

The NI4010A also checks to ensure that the received frame was an integral number of bytes in length. The user can set up the NI4010A to either accept or reject a frame with an alignment error. The normal receive mode is to reject error frames.

4.4.4 Receive Buffer Management

The NI4010A manages its receive FIFO buffer as a ring. The microprocessor manages the input pointer, the output pointer and the total byte count of received frames. When the NI4010A receives a frame from the network, it latches the frame's status and the frame's length.

Once the frame is in the receive FIFO buffer, the microprocessor reads the latched status and length bits, calculates a new byte count for the receive FIFO buffer, and stores the frame's status bits along with the new byte count in a received frame status table. If the receive buffer FIFO contains insufficient space to receive a maximum-sized frame (1518 bytes), the microprocessor disables receiver hardware.

Each frame stored in the receive FIFO buffer takes up exactly its size in bytes. The maximum number of frames that the receive FIFO buffer can hold is 177. For this many frames to fit into the receive FIFO buffer, the first 176 of them must be minimum-sized frames.

Occupied space in the buffer becomes available when the NI4010A transfers data to the host memory.

4.4.5 The Receive Data Channel Transfer

When a frame has been accepted into the receive FIFO buffer, the microprocessor examines the receive condition register to determine the action it should take. Refer to section 3.5.3 for a detailed description of the receive condition register operation. The microprocessor transfers the frame from the receive FIFO buffer into the host memory by using the Data Channel In FIFO. The microprocessor also reports the receive status and sets the DONE flag.

4.5 Diagnostic Tools

The NI4010A provides you with three sets of diagnostic tools:

1) Loopback operation.

2) Network testing.

3) Power-up self-tests with a pass/fail LED

Interlan has designed these diagnostic tools to help you isolate a network problem to a field replaceable component.

4.5.1 Loopback Operation

The NI4010A enters this mode when the host issues a Set Loopback Mode command (005). See the description of this command in section 3.4.6 for more information on loopback operation.

4.5.2 Network Testing

The NI4010A is capable of sending network test frames to itself, making use of the controller, the transceiver cable and connectors, the transceiver itself, and the network coaxial cable. To do this, the controller must be in an online state, and two test frames transmitted onto the network by use of the Perform Network Loopback Test (043) command. Refer to section 3.4.36 for a more detailed description of this command.

The NI4010A is also capable of testing the collision detect circuitry of the transceiver by use of the Run Collision Detect Test (044) command. Refer to section 3.4.37 for a more detailed description of this command.

4.5.3 NI4010A Diagnostic Self-Test

The NI4010A contains onboard (ROM resident) diagnostic programs that can be invoked with the Run Diagnostic (015) command. Refer to section 3.4.14 for a more detailed description of this command.

4.6 Performance

Several features of the NI4010A help improve system performance. Receive frames are stored in a 13.5 kbyte fifo memory, relieving the host from time critical receive operations. Receive operations can be set up so that only one interrupt occurs for each received frame. If supported by the host processor, up to 16 data channel maps may be selected (the data channel address space may have up to 19 address lines).

The NI4010A uses the I/O bus data channel facility for all data transfers. Transfers occur consecutively at a transfer rate of up to 2 megabytes per second (depending upon processor type). Data throughput performance is furthur detailed in the following sections.

4.6.1 Transmit Throughput

The NI4010A is capable of high speed transmit operation. The actual sustained throughput rate is determined by a number of factors:

1. NI4010A transmit command overhead -
   Approximately 500 microseconds is spent recognizing the transmit command, setting up the data channel transfer, updating statistics, determining the status, inserting the source address, and returning status.

2. NI4010A transmit data channel time -
   This is the amount of time the NI4010A takes to perform the actual data channel transfer from host memory. This rate is processor type dependent.

3. NI4010A transmit wire time -
   0.8 microseconds per byte is the actual time spent transmitting data onto the network.

For an ECLIPSE S/140 a throughput of approximately 4.3 megabits per second is the sustained rate, transmitting maximum length frames, and not counting host software overhead. A throughput of approximately 0.9 megabits per second is the sustained rate, transmitting minimum length frames, and not counting host software overhead.

4.6.2 Receive Throughput

The NI4010A is capable of high speed receive operation. The actual sustained throughput rate is determined by a number of factors:

1. NI4010A receive overhead -
   Approximately 500 microseconds is spent updating the receive status tables and buffer pointers, updating the statistics, error filtering, and status ouput.

2. NI4010A receive wire time -
   0.8 microseconds per byte is the actual time spent receiving data from the network.

3. NI4010A receive data channel time -
   This is the amount of time the NI4010A takes to perform the actual data channel transfer into host memory. This rate is processor type dependent.

For an ECLIPSE S/140 a throughput of approximately 4.9 megabits per second is the sustained rate, receiving maximum length frames, and not counting host software overhead. A throughput of approximately 0.9 megabits per second is the sustained rate, receiving minimum length frames, and not counting host software overhead.

4.6.3 Other Performance Considerations

When running in loopback mode, the throughput rates will be less than normal transmit and receive operation. This also applies to frames that the NI4010A sends to itself such as broadcast frames, multicast frames, and frames that have the NI4010A physical address in the destination field.

When the Load Physical Address (003) command is used to set the NI4010A physical address, the hardware address compare logic is disabled. Instead, the microprocessor performs the comparison on the frames before they are sent to the host. This results in slower receive throughput.

CHAPTER FIVE

MAINTENANCE

The NI4010A does not require calibration or any special maintenance procedures. You can install it in any host I/O bus slot, connect it to standard ETHERNET transceivers and cables, and put it online. If a problem does develop, Interlan provides on-board diagnostic programs and standalone host diagnostics.

5.1 Verifying Proper Operation

Either upon installation or when in doubt about NI4010A board operation the following sequence should be followed:

1. Verify proper NI4010A reset diagnostic operation by observing that the LOOPBACK LED goes on for approximately 1/2 (0.5) seconds then off when the host system is reset.

2. Verify proper NI4010A operation by the successful completion of the DS-NI4010A standalone diagnostic.

5.2 NI4010A On-Board Diagnostics

A subset of the NI4010A on-board diagnostics are executed on a power up reset or an IORST instuction, and the LOOPBACK LED is left on if any error is detected. The Reset (377) command also executes the same subset, but also returns a status code indicating the error condition (if any). The subset takes approximately 1/2 (0.5) seconds to execute and includes:

1. A checksum of the program memory ROM is calculated, and compared to the value stored in the last two ROM bytes. An error is reported if the values do not match.

2. A memory pattern test is performed on the scratchpad (first 1024 bytes) of the buffer RAM. An error is reported if a memory location is found that cannot be written to or read from.

3. The factory programmed ETHERNET address is checked to make sure it is not all ones or all zeroes.

The Run Diagnostic (015) command takes approximately 3 seconds to execute and performs two additional subtests:

4. A memory pattern test is performed on the full buffer RAM (16 kbytes). An error is reported if a memory location is found that cannot be written to or read from.

5. Two test frames are sent through the transmit and receive logic to verify the entire serial data path including the CRC logic. An error is reported if the frames cannot be sent and received without error. This test does not actually sent data onto the network.

5.3 NI4010A Standalone Diagnostics

5.3.1 Introduction

The Interlan diagnostic program tests the NI4010A interface and the ETHERNET environment. The program runs stand-alone, (without an operating system), on Data General Nova 3, Nova 4, Eclipse series or Eclipse/MV series computers. The program requires a minimum of 64 kbytes of host memory and a system console assigned to device codes 10 and 11.

The diagnostic is supplied on 1600 BPI magnetic tape, (Interlan part number DS-NI4010A). The tape contains two files in binary format; 1) a bootstrap program, and 2) the diagnostic program.

5.3.2 How To Start The Diagnostic Program

The diagnostic program may be executed from the DS-NI4010A distribution tape by using the bootstrap program, also on the tape. The bootstrap has been designed to work with the program load feature of all the Data General processors listed above.

To execute the diagnostic program from tape:

1) Mount the DS-NI4010A distribution tape. There are no restrictions on the device code of the magtape controller, but the tape must be mounted on drive zero of the selected controller.

2) Perform the program load procedure for your processor. The processor will load the bootstrap program from the distribution tape and begin executing it. The prompt 'FROM MTA-0:' should appear on the console.

3) Respond to the prompt by typing, '1' and a NEW-LINE character. The bootstrap program will now load the diagnostic program from the tape and execute it. When it has been successfully started, the diagnostic will print a menu of test selections.

Note: The bootstrap program uses the value in the switch register of the processor as the device code of the bootstrap device. In most Data General processors the correct value is placed in the switch register as part of the program load procedure. In Nova 4 processors however, you must set the switch register explicitly unless the default of 22 is assumed. If the prompt from the bootstrap program appears but the diagnostic will not load, you should verify that the switch register contains the correct value.

The diagnostic may also be transfered from the distribution tape to a disk and executed using the HIPBOOT program available on RDOS systems.

Transfer the diagnostic from the DS-NI4010A distribution tape to disk using the RDOS command XFER. Initialize the tape drive and then transfer the contents of file one on the distribution tape to the disk. For example:

'XFER MT0:1 FOO.SV'

This will leave a file containing the diagnostic on the disk named FOO.SV.

When the diagnostic has been placed in a file on disk, it may be loaded and executed two ways; 1) enter the BOOT command to the RDOS CLI, or 2) perform a program load from the disk device.

To execute the diagnostic program from RDOS enter the BOOT command with the name of the file containing the diagnostic as the argument. For example if the name of the file is FOO.SV as in the example above, you would type;

'BOOT FOO.SV'

This command will cause the processor to load the diagnostic program from the file FOO.SV and begin executing it.

To bootstrap the diagnostic from the disk, perform the program load procedure for the disk device. The processor will load the disk bootstrap program HIPBOOT from the disk and begin executing it. HIPBOOT will prompt you for the name of the file you want loaded by printing 'FILENAME?' on the console. Respond to the prompt by typing the name of the file containing the test program. For example if the name of the file is the same as in the previous examples, the dialogue would look like this;

'FILENAME? FOO.SV'.

The HIPBOOT program will now load the diagnostic from FOO.SV.

In either case, when the diagnostic has been successfully started, it will print the menu of test selections on the console.

5.3.3 Description

The diagnostic program is a stand alone program written in assembly language that provides a set of tools for verifying the NI4010A controller and the Ethernet enviroment.

The diagnostic program consists of a reconfigure utility program and seven test programs. When the diagnostic is first started, a list of these components will be printed on the system console in the form of a menu. The following paragraphs describe the components in the order in which they appear on the menu.

1) Reconfigure Program: This program will enter new values of device code and interrupt mask bit for the NI4010A controller.

When the diagnostic program is first started the Input/Output instructions throughout the diagnostic contain the standard factory values for device code and interrupt mask bit. If the switches on the controller have not been changed from the factory settings, the other tests in the diagnostic will execute properly without having to use the reconfigure program.

If new values for device code or mask bit have been set into the switches on the controller, it will be necesary to run the reconfigure program before attempting to run any other tests.

When selected, the reconfigure program will prompt you for the new values of device code and/or interrupt mask bit. When you have entered the new values the reconfigure program will modify Input/Output instructions throughout the diagnostic by replacing the factory values with the values you have just entered.

When the entire diagnostic program has been updated with the new values the reconfigure program will return you to the main menu. Note that the current values for device code and mask bit are displayed at the top of the menu.

This program does not do any testing and will not return any error messages.

2) Controller Diagnostic Test: This test is designed to verify the NI4010A controller as much as possible without attempting to actually receive or transmit over the Ethernet.

The controller diagnostic test is composed of a set of subtests. Normally, execution begins with the first subtest and procedes until all subtests have been executed. This constitutes one pass of the test and a message will be printed on the system console. Subtests are not independent and must be executed in sequence.

The subtests composing the controller diagnostic are numbered, begining with zero and incrementing by five. The number serves to identify the subtest and is printed as part of the error message if any faults are found by the subtest.

when the controller diagnostic is selected it asks if you want to run all subtests. If you answer 'N' to this question the program asks for the number of the subtest to loop on. You should enter a decimal number in response to this prompt. Execution begins with the first test and procedes until the selected subtest is executed. The selected subtest will then be repeated forever.

The controller diagnostic operates the NI4010A controller in local loopback mode only, therefore, it does not verify the sections of the NI4010A controller that connect to the Ethernet.

3) Network Loop-back Test: The Network Loop-back test verifies that the NI4010A controller can communicate with the Ethernet.

The network loop-back test makes use of a self-test built into the NI4010A controller that allows the controller to generate test data and send it to itself through the network. The self-test causes the NI4010A controller to send two packets, one with a known good CRC, and one with a deliberatly bad CRC. The status returned by the NI4010A indicates the results of the self- test.

The network loop-back test is structured the same as the controller diagnostic test described above. The test is composed of three subtests that invoke the NI4010A's self-test and verify the status returned. All three subtests must be executed in sequence, it is not possible to run only one subtest.

The NI4010A controller may experience a collision when it attempts to transmit the test packets; however, the network loop-back test accepts collisions as normal as long as the number on any one transmit does not exceed sixteen.

The test packets generated by the NI4010A controller will be identified by a value of 7030 hex in the packet type field. Interlan software identifies this value with diagnostic packets and ignores them. This allows diagnostic testing of a node, even if the node is attatched to an active network.

The NI4010A controller generates its own data for the network loop-back test, so the data channel portion of the controller is not exercised by this test.

4) Collision Logic Test: The collision logic, or Heartbeat, test is designed to verify the collision detection hardware of both the transceiver and the controller.

The collision logic test is almost identical in construction with the network loop-back test described above. The test consists of three subtests that invoke a self-test built into the NI4010A controller. In this case, the self test causes the NI4010A to transmit a short packet and then check for the 'Heartbeat' collision signal generated by the transceiver at the end of the transmision.

The self-test in the NI4010A invoked by the collision logic test generates its own data, so again, the data channel portion of the controller is not exercise in this test.

5) Receive Exerciser: The receive exerciser is a tool to exercise the receive portion of the NI4010A controller under varying conditions.

The initial dialogue with the test allows you to set combinations of addressing modes for the receiver. Incoming packets that meet the addressing criteria may then be compared with each other, and/or displayed on the system console.

When the exerciser is started, the first subtest sets up the selected conditions in the controller. This subtest is executed only once.

The second subtest executes forever receiving packets. Pairs of incoming packets are compared, (unless you have defeated that function), and a pass message will be printed on the console for every pair of packets received.

The test compares packets on a byte for byte basis. The first packet received will be compared with the second, the third packet received will be compared with the fourth and so on. The contents of packets may be changed between pairs however, so the first packet need not be the same as the third packet.

If an error occurs, or a packet is lost, the test will wait for a matching pair of packets in an attempt to synchronize itself with the transmitter.

A good source of data for the receive exerciser is another Ethernet node running the transmit exerciser described below.

6) Transmit Exerciser: The transmit exerciser provides a tool to exercise the transmit portions of the NI4010A controller. The exerciser may also be used to provide a source of data on a network.

The initial dialogue prompts you for values for the different fields of an Ethernet packet. The Type field is an exception, the value always being forced to diagnostic type.

The first subtest in the module initializes the controller and executes only once. The second subtest runs forever thereafter and continuosly transmits pairs of packets. The test prints a pass message on the system console after each pair of packets has been successfully transmitted. If any portion of the packet has been specified as random, that portion is changed between pairs of packets.

This test will run in conjunction with the receive test described above. Neither test requires a quiet network, though you should take care with the options you specify if the network is operating.

7) Start-Echo Test: The start-echo test is designed to provide a simulation of actual network operation in the test enviroment.

The start echo test prompts you for the network address of a target node. The test then sends pairs of packets to the node specified and the target is expected to send the packets back.

The test compares each packet received with the one sent and reports an error if they do not match. The test will print a pass message for each pair of packets received.

The start echo test allows you to specify the size and contents of the data field of the test packets. If the data field is specified as random, the size and content of the data field will be changed after each pair of packets has been successfully echoed.

If an error is detected the test will attempt to retransmit the current packet until it is echoed correctly.

The Echo test, described below, can provide the other end of the connection for this test. The test may be run on an active network.

8) Echo Test: The echo test helps to simulate normal network traffic in the test enviroment by implementing target nodes for one or more nodes running the start-echo test described above.

The echo test echos packets by exchanging the source and destination address fields of received packets and retransmitting them. Packets with the destination address of 'broadcast' are an exception to this rule. The test assumes it is to echo only packets specifically addressed to its node; so broadcast packets are not echoed.

The echo test can compare incoming packets in pairs like the receive test described above. The test also prints a pass message after each pair of packets.

One node running echo test can act as target for several nodes running the start-echo test. In this case the echo test cannot compare packets because two packets arriving in sequence may have been sent from different nodes. The echo test provides for this case by asking you if you want the test to compare packets. Typing 'N' to this question will disable the packet compare portion of the test.

5.3.4 How To Run The Diagnostic Tests

When first started the diagnostic program prints a menu on the system console listing its component test programs followed by a prompt. You select a test program for execution by entering the program number from the menu in response to the prompt.

When selected, the test program will print its name and then prompt you for the information it requires to perform its test. The test will then print the settings of the control flags that determine how the test responds to errors and also the error message format. The test will then prompt you for changes to the flag settings.

The control flags are set or cleared with single-character commands described below. Typing the command character will toggle the setting of the associated flag and display the new setting on the console. Other single-character commands report test status or halt execution of the test.

Descriptions of the single-character commands follow:

Character	Command	Function
H	Toggle Halt-On-Error flag	If flag=1 Halt in the subtest that found the error.
L	Toggle Loop-On-Error flag	If flag=1 Loop on the subtest that found the error. Note: If neither flag is set execution will continue with the next subtest.
P	Toggle Print-Error flag	If flag=1 truncate all error messages to a single ASCII Bell Delete the Pass/Fail messages.
V	Toggle Verbose flag	If flag=1 print the number of each subtest as it is started. In addition the Receive exerciser and the Echo test will print the first 28 bytes of received packets if this flag is 1.
R	Report Pass/Fail status	Causes the current number of completed passes and passes with errors of the running test to be output on the console.
F	Report flag status	Displays the current state of the P,V,L and H flags on the system console.
CTRL-A	Abort current test program	Stops execution of the current test leaving interupts off. If the H flag is set, the test halts. On procede, the test gives you the option of resuming the test program or returning to the main menu.
CTRL-C	Cancel current test program	Causes the program to return immediatly to the main menu.

After the test program has prompted for changes to the flag settings all single character commands will be honored; typing CTRL-C, for instance returns you to the main menu without starting the selected test program.

When you type a 'C' to the prompt, the test program will begin execution with the first subtest. You may use all of the single-character commands while the selected test program is running. The test program will run until you stop it with a CTRL-C or CTRL-A command.

The test programs described above provide the basic tools to verify the operation of an Ethernet node based on the NI4010A controller:

1) Configure the diagnostic program for the device code and mask bit selected for the NI4010A controller.

2) Run the controller diagnostic test for at least ten passes. The test uses random data so it is important to give it enough time to try a reasonable number of combinations.

3) Run the network loop-back and collision logic test programs. These tests do not use random data so two passes or so are sufficient.

If the controller diagnostic test does not produce any errors ,however errors occur in the network loop-back or collision logic tests, the fault is most likely due to the cable between the host computer backplane and the transciever or the tap connecting the transceiver to the Ethernet. If the controller diagnostic test fails, the fault is most likely due to the NI4010A controller.

5.3.5 Error Messages

The diagnostic program reports two classes of errors; 1) Fatal errors and, 2) Diagnostic errors.

Fatal errors are reported when the fault is judged severe enough to prevent the diagnostic program from proceeding further. When a fatal error is detected by any test in the diagnostic program, a message describing the problem is displayed on the system console then the program halts. If you procede from the halt the program attempts to restart. The fatal error messages are:

UNEXPECTED PROCESSOR FAULT OR TRAP OCCURED IN TEST: xx

This message reports a fault detected by the host processor; for example, a stack overflow fault. The number given is the number of the subtest within the current test program that was running when the fault occured.

TEST SEQUENCE FAULT: STARTED IN TEST xx, AND ENDED IN TEST xx

The diagnostic program records the number of each subtest when it is begun, and when it completes. If the numbers do not match, indicating a portion of the subtest was destroyed, or skipped, the diagnostic program reports this message.

Diagnostic errors are reported as an aid in isolating a fault. How the diagnostic program responds to these errors depends on the setting of the control flags described above. All diagnostic error messages begin with a line that states the number of the subtest that detected the error, and an error number. The error number indicates what part of the subtest failed. The error message that follows describes the symptoms of the fault. These messages are:

BUSY/DONE FLAG ERROR:	ACTUAL	EXPECTED
BUSY:	x	x
DONE:	x	x

If the values for the busy and done flags of the NI4010A controller were not the expected values, the diagnostic program prints this message.

Note: This error may occur if the diagnostic program is using a different device code than the NI4010A controller. Verify the device code set with the switches on the controller is the same as the device code in use by the diagnostic program.

UNEXPECTED INTERRUPT OCCURED FROM DEVICE CODE xx

The diagnostic program runs with interrupts enabled, however all devices except for the console input and the device under test are masked out. If an interrupting device is not one of those two, this error message will be displayed.

COMMAND TIMEOUT ERROR

When the diagnostic program issues a command to the NI4010A controller it starts a software timer. If the controller does not complete the command with in two seconds the test will display this message.

COMMAND INTERRUPT ERROR
EXPECTED INTERRUPT DID NOT OCCUR

The diagnostic program expects an interrupt when a command is issued to the NI4010A controller and the controller is not masked. This message will be displayed if the controller completes the command without interrupting the diagnostic program.

Note: This error may be caused by configuring the diagnostic program and the NI4010A controller to use different interrupt mask bits. Verify the mask bit selected with the switches on the NI4010A controller is the same as the bit in use by the diagnostic program.

COMMAND INTERRUPT ERROR
INTERRUPT OCCURED UNEXPECTEDLY

This message indicates the diagnostic program was interrupted by the NI4010A controller when no command had been issued.

STATUS ERROR: EXPECTED STATUS = xxxxxx, ACTUAL STATUS = xxxxxx

The diagnostic program examines the status returned by the NI4010A controller for every command issued. If the status returned indicates an error, then this message will be displayed. Refer to section 3.4 of this manual to interpret the status returned.

RECEIVER TIMEOUT ERROR

The diagnostic program sets an upper limit on the amount of time it will wait for the NI4010A controller to receive a packet. If the controller is in local loop-back mode, the diagnostic will wait for sixty seconds. If the controller is on line, the time is extended to two minutes. This error indicates a test packet was lost but does not tell you if the fault is in the transmitter or receiver.

RECEIVER INTERRUPT FAULT
EXPECTED INTERRUPT DID NOT OCCUR

This message indicates a receive operation completed without interupting the diagnostic program. This error is similar to the command interupt fault error.

RECEIVER INTERRUPT FAULT
INTERRUPT OCCURED UNEXPECTEDLY

This message will be displayed if the diagnostic program is unexpectedly interrupted by the receive portion of the NI4010A controller.

BAD STATUS ON RECEIVE: STATUS = xxxxxx

This message will be displayed if an error occurs on any receive operation. Refer to section 3.3.8 of this manual to interpret the status returned by the receiver.

BUFFER COMPARE ERROR: SOURCE BUFFER SIZE = xx,
RESULT BUFFER SIZE = xx

This message may occur when the diagnostic program attempts to compare a test packet with an expected result. It indicates the size of the test packet as received was different than expected. The buffer size is given in bytes.

DATA COMPARE ERROR:		ORIGIN	POINTER	DATA
SOURCE BUFFER	-	xxx(x)	xxx(x)	xxx
RESULT BUFFER	-	xxx(x)	xxx(x)	xxx

This message may occur when the diagnostic program attempts to compare a test packet with an expected result. It indicates the contents of the test packet as received was different than expected. The values labeled SOURCE refer to the expected result, the values labeled RESULT refer to the received test packet.

The ORIGIN is the address of the start of the packet, the value in parens indicates the right byte of a word if it is zero, or the left if it is one. The POINTER is a similar address that points to the byte in error. DATA gives the values for the byte in question.

These messages are designed to aid in isolating a fault. The interpretation of these mesages requires the name of the test and the number of the subtest running when the error occured, and the error number attached to the message.

5.4 Product Warranty

Interlan warrants that the products covered hereby shall be free from defects in material and workmanship for a period of one(1) year from the date of initial shipment by Interlan. The foregoing warranty does not apply to any products which have been subject to misuse, neglect, accident, or modification.

If found defective by Interlan within the terms of this warranty, Interlan's sole obligation shall be to repair or replace at Interlan's option the defective product and carry out the unexpired term of the warranty which was applicable to the defective product. All replaced products become the property of Interlan.

As a condition of this warranty, customers must (1) obtain an Interlan Return Material Authorization (RMA), and shipping instructions, (2) return all products (or approved subassemblies) transportation prepaid and insured to Interlan's Westford, Masachusetts facility or other specified location, and (3) include a written description of the claimed defect.

If Interlan determines that the product is not defective within the terms of this warranty, Customer shall pay all costs of handling and return postage; otherwise normal transportation charges for the return to Customer shall be paid by Interlan within the United States only. This warranty outside of the United Stated excludes all costs of shipping, Customs clearance, and other relate charges.

Except for the express warranties stated above, Interlan disclaims all warranties on products including all implied warranties of merchantability and fitness; and the stated express warranties are in lieu of all obligations or liabilities on the part of Interlan.

5.5 Service Policy

Should a product fail while under the terms of the warranty agreement, it will be repaired or replaced free of charge. For out-of-warranty service, repairs are charged on a time and material basis.

To return a product for out-of-warranty repair:

1. Contact the factory for a Return Material Authorization Number (R.M.A.), shipping instructions, and a non-binding repair cost estimate.

2. Return the product (or approved subassembly) transportation prepaid and insured to Interlan's Westford, MA facility (or other specified location) with the R.M.A. number marked on the outside of the packege.

3. Include a written description of the product's symptomatic problem, and the name and telephone number of a technical contact.

4. Include a purchase order for an amount equal to the estimated repair cost, and the name and telephone number of the purchasing contact.

If Interlan determines the product not to be repairable for less than the quoted estimate repair cost, Interlan will notify the purchasing contact for repair authorization before proceeding. In all cases repairs are performed and charged on a time and materials basis, and the product is returned with transportation charges prepaid and billed.

Repair is performed at the factory only, typically within a 72 hour turnaround time. To avoid delay in processing the return it is absolutely necessary to return products in the manner stated here.

All repairs are warranted for a period of 30 days after return to the customer.

APPENDIX A

ETHERNET/IEEE-802 NETWORK

PLANNING, INSTALLATION, AND TEST GUIDELINES

A.1 Planning

An ETHERNET system provides simplicity of installation and flexibility of layout. The ETHERNET system can be readily enlarged with expanding word and information processing needs. A small ETHERNET system concentrated on one floor, supporting four or five work/information processors can be progressively enlarged to a final system servicing an entire multi-floor building complex with up to 1024 stations of various types and processing power. Such a system can also interact with a local main frame supported data processing system and/or, via external transmission lines, can access remote systems and terminals. Planning and installation activity will vary greatly depending on present and future system size and complexity.

Perform the following steps to provide a total, fully integrated and highly efficient ETHERNET system:

1. Analyze current and expected future information processing needs.

2. Select equipment expected to satisfy current and future information processing needs.

3. Conduct a feasibility study in cases where an ETHERNET system is required to be integrated into an existing data network.

4. Plan the cable route and the distribution of the equipment.

5. Install the cabling and equipment.

6. Purchase the ETHERNET network hardware and controlling software.

7. Conduct system acceptance tests.

An ETHERNET solution to a specific environment can be specified by deciding how the user's current needs will be directly satisfied. System enhancements will also be specified in anticipation of business growth and possible diversification. Specific needs will vary according to the size and nature of the business and the way that business is conducted.

Implementation of an ETHERNET system requires installation plans to be specified showing how and where the ETHERNET cable shall be routed and

where each station shall be sited. The installation of transmission medium hardware (such as cables, transceivers, and repeaters) can be performed by wiring contractors. After cable installation is completed and before system integration of stations, transceivers, and repeaters is initiated, the cable should be subjected to continuity and stress testing. The final stage of implementation is the system acceptance test phase.

A.2 Installation

Before proceeding with the installation of the cable network and its associated components the route must be carefully planned along with the siting of the transceivers, repeaters, and remote repeaters. Prior to drawing up the plans a detailed site inspection must take place in order that the best route is chosen. "Best route" does not necessarily imply the most convenient or the "quickest to install" route. The cable route chosen must take into consideration many factors which will be beyond the control and influence of the system planner and installer. The route must be planned so that it will comply with all ETHERNET specifications listed in Table A-1.

TABLE A-1

ETHERNET CHANNEL REQUIREMENTS

* The maximum station separation on the network is 1500 meters (4920 feet).

* The minimum station separation on the network is 2.5 meters (8 feet 2 inches).

* The maximum length of the transceiver cable between any station and its associated transceiver is 50 meters (165 feet).

* The network is comprised of one or more cable segments.

* Each cable segment is made up of the combined length of one or more cable sections, and is terminated at both ends by a 50 Ohm coaxial cable terminator.

* The maximum combined length allowed for a cable segment is 500 meters (1640 feet).

* Cable segments are interconnected by repeaters and/or remote repeaters.

* Any number of repeaters of either kind can be used, but no more than two repeaters may be inline between any two stations on the network.

* Repeaters are used to extend the length of the channel and to extend the topology from 1 to 3 dimensions.

* Remote repeaters allow point-to-point connection of cable segments many hundreds of feet apart, such as between buildings.

* No more than 1000 meters (3280 feet) of total point-to-point link are allowed.

* Repeaters may be attached at any point on a cable segment as long as the 2.5 meter minimum separation distance requirement is not violated.

* Repeater pairs occupy transceiver positions on both cable segments and count towards the maximum number of stations on each segment.

* A cable segment can accomodate up to 100 station/transceiver pairs and repeater pairs.

* The maximum number of station/transceiver pairs and repeater pairs on a network is 1024.

When installing the ETHERNET transmission medium hardware you should also comply with the following requirements:

* Avoid areas where electrical noise is present.
* Avoid areas where mechanical damage is likely.
* Use the most accessible route.
* Use the route least likely to be disturbed.
* Use the shortest route.

Obviously some of these requirements will conflict; the successful installation incorporates the above mentioned guidelines , making tradeoffs when necessary.

Pre-assembled coaxial cables with metal screw-type coaxial connectors are available from Interlan in three fixed lengths (see section 1.3):

77 feet (23.4m),
230 feet (70.2m), and
384 feet (117m).

The sizes listed above for standard coaxial cable lengths were chosen to eliminate excessive signal reflections.

The ideal coaxial cable has no joints (i.e., it is made from one cable length). This is feasible if the required cable segment can be made from a standard cable length (e.g., 23.4, 70.2, or 117 meters). If cable segments longer than 117 meters are necessary, they must be built up from a combination of cable lengths from the same manufacturer and model type. Use a combination of cable lengths in preference to a number of identical lengths when making up a cable segment.

When constructing a cable layout, be certain that the total length of each segment does not exceed 500 meters (1640 feet) and that the total length of the network does not exceed 1500 meters (4920 feet). The minimum bend radius allowed in a coaxial ETHERNET cable section is 7 inches. If the installed cable is to be exposed, it is suggested that it be secured with cable ties to prevent possible kinking by later disturbances. In addition, the metal connectors used to interconnect cable sections and the metal cable terminators must be sleeved to prevent electrical contact with ground potential structures and electrical conductors such as conduit and cable troughs. Devices are normally attached via one of three additional set lengths of drop cable. The multipair transceiver drop cables are sized in the following lengths:

10 feet,
50 feet, and
150 feet.

If necessary, a combination of drop cable lengths may be joined, provided that the maximum length of 165 feet is not exceeded. The following examples illustrate three basic installation configurations. It should be possible to design a solution to any particular installation using these examples and their accompanying figures.

A) The Typical Minimal Configuration

Minimal configurations lend themselves to cluster-type installations where the stations and devices are situated within relatively close approximation of each other. This type of installation has one cable segment ranging in length from 77 to 1640 feet. It does not require the use of repeaters. The minimal configuration supports up to 100 stations.

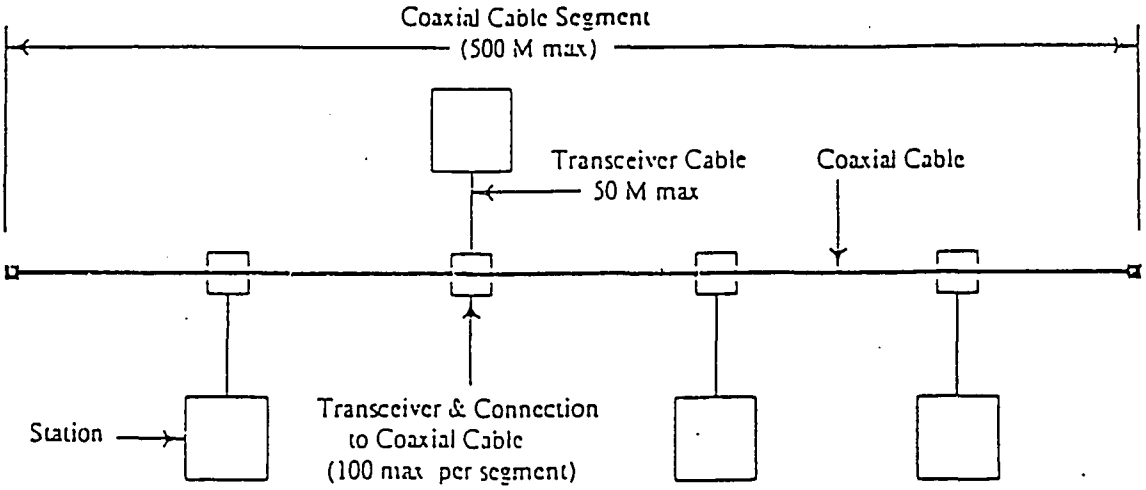


Figure A-1a: The Minimal Configuration

B) The Typical Medium-Scale Configuration

This configuration is typically used for installations that require medium distance interconnection of stations and devices within a one or two story building. A medium-scale configuration employs two cable segments, each from 77 to 1640 feet in length. The two coaxial cable segments are interconnected via a repeater. This configuration can support up to 198 stations.

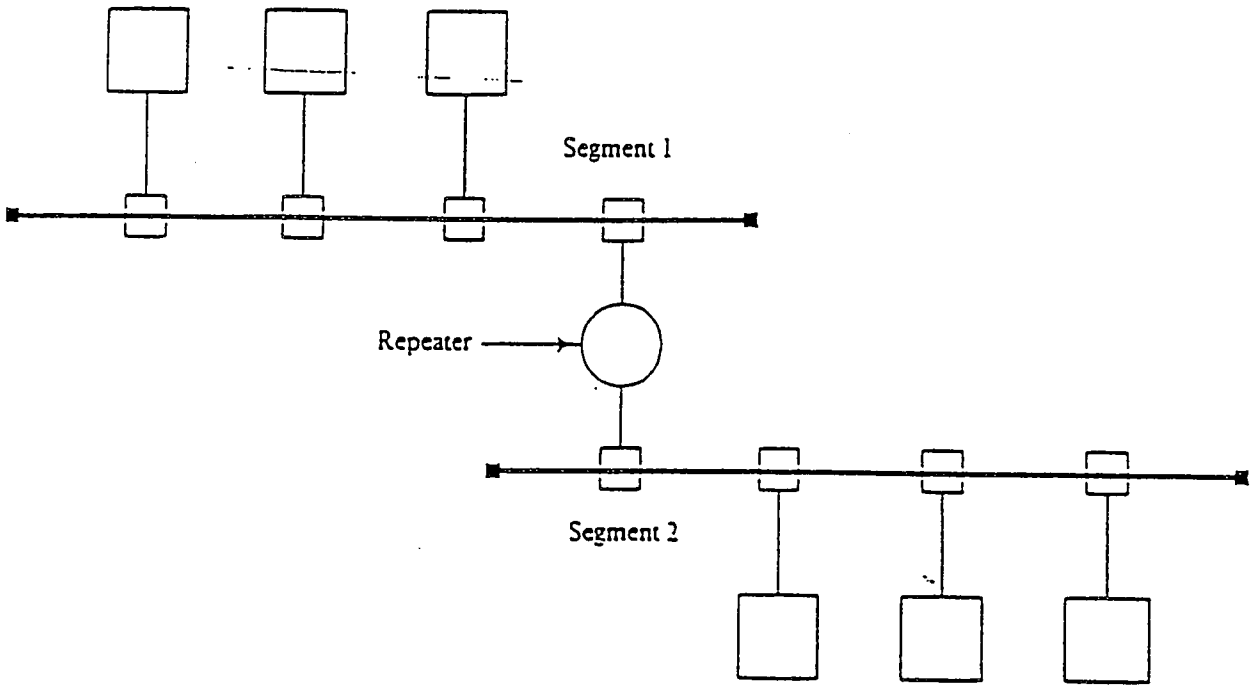


Figure A-1b. A Typical Medium-Scale Configuration

C) The Typical Large-Scale Configuration

This configuration is typically used for installations in multi-floor building complexes with interconnections via remote repeaters to adjacent building(s). This configuration can be a full scale ETHERNET implementation consisting of many cable segments and, if required, several point-to-point links. Note in the figure that segment 3 acts as a central bus, insuring that the maximum of 2 repeaters between any two stations is maintained. If remote repeater(s) are used, remember that the maximum total point-to-point link distance can not exceed 1000 meters (3280 feet).

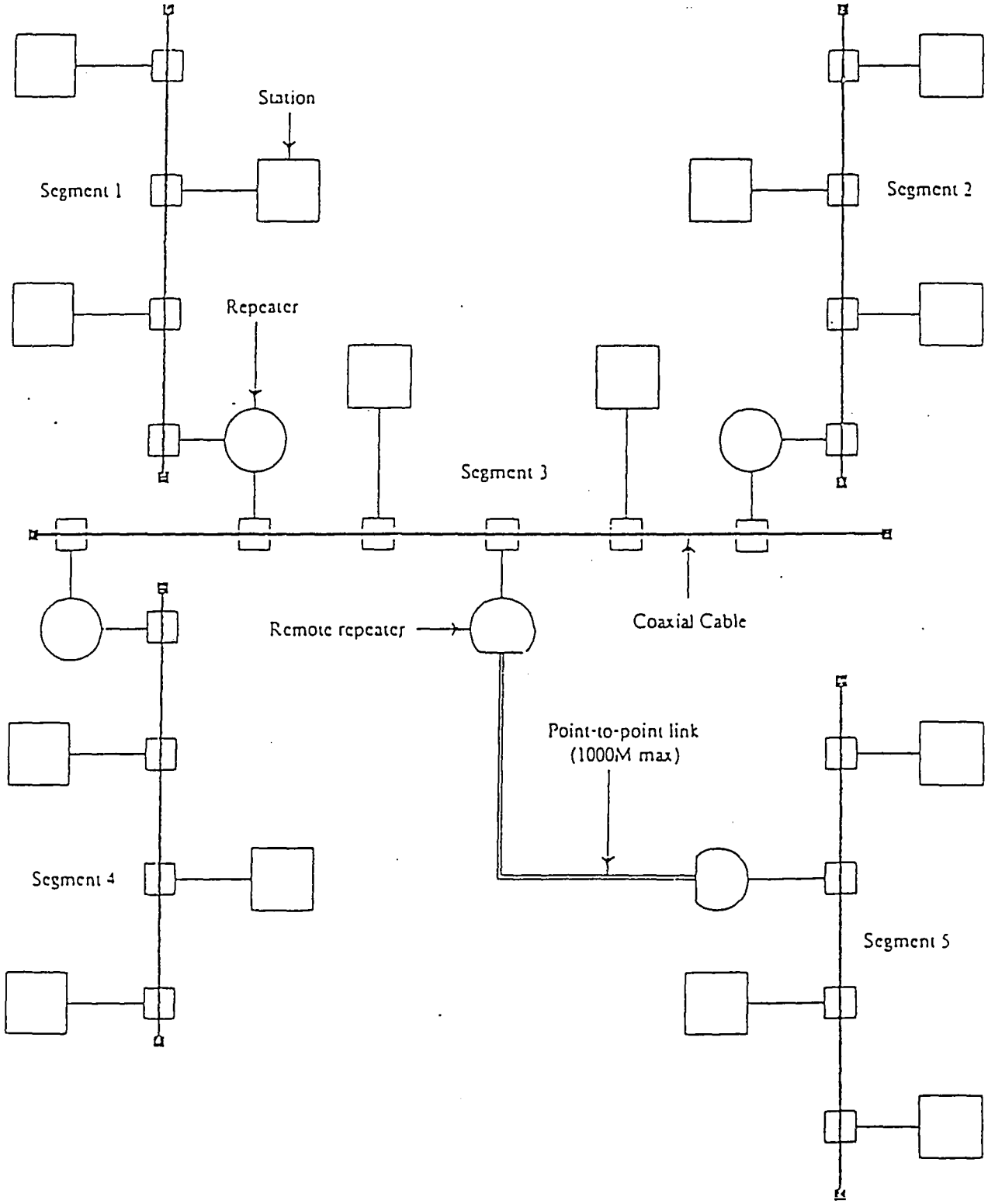


Figure A-1c: A Typical Large-Scale Configuration

SECTION III. TESTING

Testing is done in two phases. The first phase of testing is performed for each coaxial cable segment after interconnection of the individual cable lengths and attachment of the cable segment's coaxial terminators. Each cable segment should be tested individually before it is connected to other tested cable segments and before transceiver connections are made.

The second testing phase is performed to ascertain the proper operation of the network and its interconnected stations, transceivers, repeaters, and devices.

Proper testing of the coaxial cable segment is of paramount importance for successful network operation. Once proper operation of the individual cable segments is verified, testing can proceed to the total system acceptance test.

Cable testing consists of sending a half sine wave voltage pulse down the cable. Each and any cable fault will indicate itself as a point of discontinuity of one type or another and will cause energy to be reflected back down the cable to the enery source, where it is detected. This type of test is known as Time Domain Reflectometry (TDR). Open and shorted areas of cables are displayed on a chart recorder as a dramatic change in amplitude. Lesser variations can indicate frayed and crimped cables. The location of a suspected fault can be ascertained by the time delay between the incident and reflected pulses. Testing and data comparison from both ends of the cable segment provide higher resolution for fault location measurements.