AN 750: Using the Altera PDN Tool to Optimize Your Power Delivery Network Design

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This application note provides guidance on the estimation of FPGA current requirements for the design of a robust FPGA Power Delivery Network (PDN). It provides guidance on how to improve the efficiency of the PDN with the Altera PDN Tool, with an objective of reducing the number of PCB mounted decoupling capacitors.

Altera provides a PDN tool that is based on an Microsoft Excel spreadsheet used to calculate an impedance profile based on user inputs. This PDN Tool helps design a robust PDN, estimate its performance and optimize decoupling solutions and reduce cost. The PDN Tool can be used to analyze all FPGA power supply rails.

This application note should be read in conjunction with the *PDN Tool User guide*, and *PowerPlay Early Power Estimators (EPE)* and *PowerPlay Power Analyzer*.

For more information on PDN design refer to *Printed Circuit Board (PCB) Power Delivery Network (PDN) Design Methodology* and on the *Altera Board Design Resource Center*.

Related Information

- **AN 574: Printed Circuit Board (PCB) Power Delivery Network (PDN) Design Methodology**
- **Support Resources : Board Design**
- **Device-Specific Power Delivery Network (PDN) Tool 2.0 User Guide**
- **PDN Tool User Guide**
- **PowerPlay Early Power Estimators (EPE) and Power Analyzer**

Impact of a Poor PDN

A stable power supply is the foundation of your FPGA design. It helps ensure that the device is within electrical specifications. A robust Power Delivery Network (PDN) that manages voltage ripple, is an important part of your power supply design.

With an increase in current loading, an insufficient PDN can result in excessive voltage ripple, voltage drops, and VRM instability. Voltage ripple on VCC supplies can cause brown-out conditions or timing margin reduction through power supply noise induced jitter. This can lead to data integrity problems.

A robust PDN is important for transceiver designs. A transceivers performance can be adversely affected by voltage ripple on its power supplies. Increased voltage ripple on transceiver power supplies can increase the Bit Error Rate (BER) through increased transmit jitter or reduced jitter tolerance.

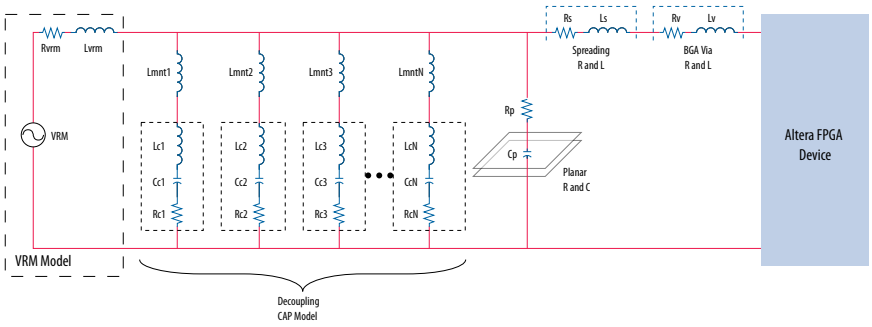
Jitter induced by supply voltage ripple on General Purpose IO (GPIO) and PLL supplies reduces timing margin on External Memory Interfaces (EMIF) such as DDR3 and DDR4. Bit errors can be seen if timing margins are violated.

PDN Circuit Topology

The PDN tool is based on a lumped equivalent model representation of the power delivery network topology. A schematic representation of the circuit topology, modelled as part of the tool is shown in the figure below.

For first order analysis, the voltage regulator module (VRM) can be modelled as a series-connected resistor and inductor. At low frequencies, up to 50 KHz, the VRM has a very low impedance and is capable of responding to the instantaneous current requirements of the FPGA. The ESR and ESL values can be obtained from the VRM manufacturer. At frequencies higher than 50 KHz, the VRM impedance is mostly inductive, that makes it incapable of meeting the transient current requirement. The on-board discrete decoupling capacitors must provide the required low impedance from low to high frequencies, depending on the capacitor intrinsic parasitics (RcN, CcN, LcN) and the capacitor mounting inductance (LmntN). The interplanar capacitance between the power-ground planes typically has lower inductance than the discrete decoupling capacitor network, making it more effective at higher frequencies (10 MHz and higher). The effectiveness of the decoupling capacitors is limited by the PCB spreading inductance and the ball grid array (BGA) via inductance that a given capacitor encounters with respect to the FPGA. To simplify the circuit topology, the PDN tool models the distributed nature of PCB spreading, BGA inductance, and resistance with a single lumped inductor and resistor.

Figure 1: PDN Circuit Topology



From this diagram it is clear that the key to improving the efficiency of the PCB PDN is to reduce component mounting inductance (Lmnt), parasitic inductance (Lc) and spreading inductance (Ls). This application note will provide guidance on methods of reducing these inductances, and how to evaluate this in the PDN Tool.

Estimating the Current Requirements of your FPGA Design

Before designing your PDN, it is important to use accurate current estimates for each FPGA power supply. You should consider worst case scenarios of your design, but do not over-estimate, because it can make the PDN design more challenging.

You can estimate the current requirements of your FPGA design with the *PowerPlay Early Power Estimators (EPE)* and *Quartus PowerPlay Power Analyzer (PPPA)*. The EPE is a spreadsheet based tool that

shows the FPGA design power, based on your design requirement input. The PPPA is a Quartus® software tool that estimates your current requirements, based on the Fit of your Quartus project.

The *PowerPlay Early Power Estimators (EPE)* and *Power Analyzer* userguide provides additional information on these tools.

Related Information

PowerPlay Early Power Estimators (EPE) and Power Analyzer

FPGA Functional Blocks

The current and decoupling requirements increase if the current in your design increases.

To estimate the current requirements of your design, Altera recommends including all functional blocks that you plan to use. Include accurate use of Logic Elements, DSP blocks, PLLs, transceivers, Hard IP, HPS, Internal Memory and IO.

Clock Frequencies

Dynamic power requirements increase with clock frequency. To account for worst case current requirement conditions, Altera recommends using the highest clock frequencies that your design will run at. When using dynamic reconfiguration of PLLs in your design, ensure that your estimates are based on the highest frequency you intend to use for logic clocked by the PLLs.

For multiple clock frequency domains in your design, it is tempting to simplify your estimates by assuming that all clock domains in your design run at the same highest frequency. Estimate each clock domain separately, because over estimation makes the PDN design difficult. The EPE and Power Analyzer allow you to do this estimation.

GPIO

General Purpose IO (GPIO) current requirements are dependent on the IO standard, drive strength, termination use, frequency and toggle rate. Altera recommends using accurate IO standard settings in your estimations.

Transceivers

Power requirements increase with frequency so when using transceivers that can be reconfigured between multiple data rates, you should ensure that you use your highest datarate for your power estimations. The estimates should use the correct, worst case Physical Coding Sub-layers (PCSs) for your design.

Depending on protocol and datarate, transceivers use the following PCSs:

- PCI Express Hard-IP
- Enhanced PCS
- Standard PCS

When implementing dynamic reconfiguration to switch between the Standard and Enhanced PCS, Altera recommends using the PPPA to determine whether the Standard or Enhanced PCS consumes more power for your design.

As an example, dynamic reconfiguration is used to switch between Altera IP 1G/10G Ethernet IP using the Standard PCS for 1Gbs Ethernet and the Enhanced PCS for 10Gbps Ethernet. To determine worst case power estimations, use the 10Gbs Ethernet using the Enhanced PCS.

If you intend to use Decision Feedback Equalization (DFE) or Adaptive Equalization (AEQ) with your transceivers you should include these in your power estimations. Adding DFE and AEQ adaption to your design increases the transceiver power requirements and the PDN design challenges. The estimations should be based on channels that use DFE and AEQ. If you do not use DFE and AEQ for some channels, then do not not include them in your power estimations.

Data Patterns

Power requirements depend on toggle % of the logic in your design. A clock-like data pattern has higher current requirements than a PRBS pattern. A PRBS pattern has higher current requirements than those for a grey-code pattern.

Use the highest toggle % that you expect to see in your design. The PDN design becomes difficult if you over estimate. Although it is design dependent, Altera assumes a 12.5% toggle percentage. Use the PPPA to analyze the toggle % of your design.

When using the Quartus PPPA, base your power estimations on simulation-based input data. It provides accurate power estimations.

Calculating Ztarget

A PDN should have a low enough target impedance (Ztarget) to meet the voltage ripple requirements under maximum dynamic current requirements.

Figure 2: Ztarget Formula

$$Z_{TARGET} = \left[\frac{Voltage\ Rail \times \frac{\%\ Ripple}{100}}{Maximum\ Dynamic\ Current} \right]$$

This formula shows:

- A decrease in voltage rail decreases Ztarget
- A decrease in allowed voltage ripple decreases Ztarget
- An increase in dynamic current decreases Ztarget

Very low target impedances require significant effort to design a sufficient PDN.

It can be challenging to provide PCB decoupling for the FPGA core (VCC), and transceiver VCCR_GXB, VCCT_GXB supplies. The low voltage, high current, VCC supply results in low target impedance. The transceiver VCCR_GXB and VCCT_GXB supplies have lower current than the VCC supply, but have low ripple requirements and hence low target impedance.

Assuming the following requirements, Ztarget can be calculated for the following VCC, VCCR_GXB, and VCCT_GXB cases. The current transient %, and allowable ripple % recommendations can be found on the Introduction tab of the PDN tool.

Table 1: Ztarget Calculations for VCC, VCCR_GXB, and VCCT_GXB Supplies

Supply Name	Nominal Voltage (V)	Allowable Ripple (%)	Imax (A)	Current Transient (%)	Target Impedance (mR)
VCC	0.9	5	30	50	3
VCCR_GXB	1.0	3	6	30	16.67
VCCT_GXB	1.0	2	2	50	20

Additional challenges may occur when sharing supply rails with differing current requirements such as VCCR_GXB and VCCT_GXB. The worst case combination of higher IMax of the VCCR_GXB supply and lower ripple and high current transient of the VCCT_GXB supply, can create very low target impedances. Using the **x** or **x/related** options in the PDN Tool helps reduce the decoupling burden by estimating synchronous versus non-synchronous current switching.

In this application note, the VCCR_GXB and VCCT_GXB supplies are considered separately because it results in decoupling solutions with fewer PCB decoupling capacitors.

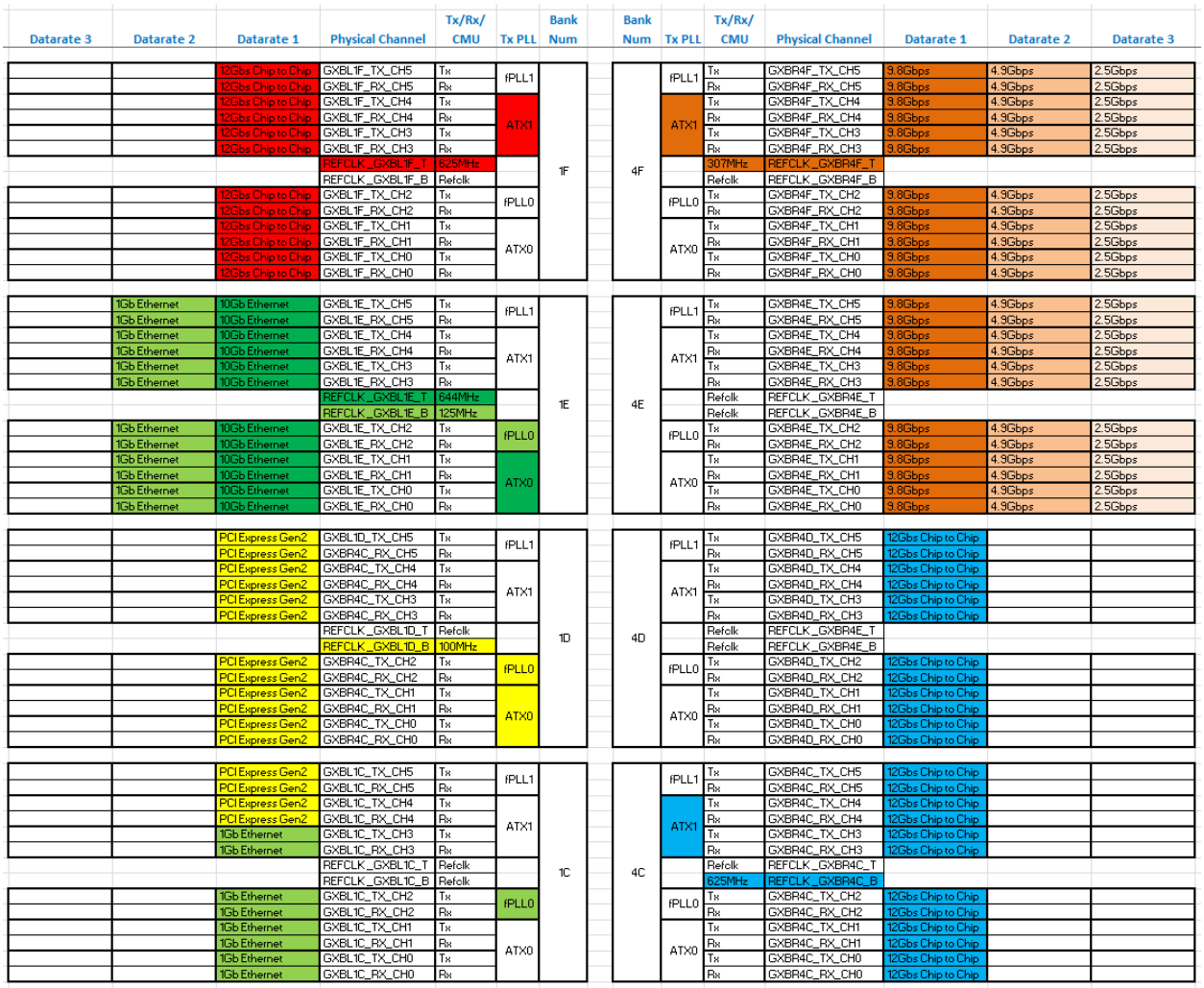
This application note focuses on the FPGA VCC, VCCT_GXB, and VCCR_GXB supplies that have low target impedance and require additional effort to decouple. Altera recommends that you analyze the performance of all design supplies.

Example Design

A Quartus project targeting an Arria 10 10AX115N4F45I3SGE2 device, implementing a transceiver design and core noise generators was used to produce current requirements for the core VCC, and transceiver VCCT_GXB and VCCR_GXB supplies.

The following figure shows the transceiver channel placement of the design used in this application note.

Figure 3: Transceiver Channel Allocation of the Example Design



Datarate 3	Datarate 2	Datarate 1	Physical Channel	Tx/Rx/ CMU	Tx PLL	Bank Num
		12Gbs Chip to Chip	GXBL1F_TX_CH5	Tx	fPLL1	1F
		12Gbs Chip to Chip	GXBL1F_RX_CH5	Rx		
		12Gbs Chip to Chip	GXBL1F_TX_CH4	Tx	ATX1	
		12Gbs Chip to Chip	GXBL1F_RX_CH4	Rx		
		12Gbs Chip to Chip	GXBL1F_TX_CH3	Tx		
		12Gbs Chip to Chip	GXBL1F_RX_CH3	Rx		
			REFCLK_GXBL1F_T	625MHz		
			REFCLK_GXBL1F_B	Refclk		
		12Gbs Chip to Chip	GXBL1F_TX_CH2	Tx	fPLL0	
		12Gbs Chip to Chip	GXBL1F_RX_CH2	Rx		
		12Gbs Chip to Chip	GXBL1F_TX_CH1	Tx	ATX0	
		12Gbs Chip to Chip	GXBL1F_RX_CH1	Rx		
		12Gbs Chip to Chip	GXBL1F_TX_CH0	Tx		
		12Gbs Chip to Chip	GXBL1F_RX_CH0	Rx		
	1Gb Ethernet	10Gb Ethernet	GXBL1E_TX_CH5	Tx	fPLL1	1E
	1Gb Ethernet	10Gb Ethernet	GXBL1E_RX_CH5	Rx		
	1Gb Ethernet	10Gb Ethernet	GXBL1E_TX_CH4	Tx	ATX1	
	1Gb Ethernet	10Gb Ethernet	GXBL1E_RX_CH4	Rx		
	1Gb Ethernet	10Gb Ethernet	GXBL1E_TX_CH3	Tx		
	1Gb Ethernet	10Gb Ethernet	GXBL1E_RX_CH3	Rx		
			REFCLK_GXBL1E_T	644MHz		
			REFCLK_GXBL1E_B	125MHz		
	1Gb Ethernet	10Gb Ethernet	GXBL1E_TX_CH2	Tx	fPLL0	
	1Gb Ethernet	10Gb Ethernet	GXBL1E_RX_CH2	Rx		
	1Gb Ethernet	10Gb Ethernet	GXBL1E_TX_CH1	Tx	ATX0	
	1Gb Ethernet	10Gb Ethernet	GXBL1E_RX_CH1	Rx		
	1Gb Ethernet	10Gb Ethernet	GXBL1E_TX_CH0	Tx		
	1Gb Ethernet	10Gb Ethernet	GXBL1E_RX_CH0	Rx		
		PCI Express Gen2	GXBL1D_TX_CH5	Tx	fPLL1	1D
		PCI Express Gen2	GXBR4C_RX_CH5	Rx		
		PCI Express Gen2	GXBR4C_TX_CH4	Tx	ATX1	
		PCI Express Gen2	GXBR4C_RX_CH4	Rx		
		PCI Express Gen2	GXBR4C_TX_CH3	Tx		
		PCI Express Gen2	GXBR4C_RX_CH3	Rx		
			REFCLK_GXBL1D_T	Refclk		
			REFCLK_GXBL1D_B	100MHz		
		PCI Express Gen2	GXBR4C_TX_CH2	Tx	fPLL0	
		PCI Express Gen2	GXBR4C_RX_CH2	Rx		
		PCI Express Gen2	GXBR4C_TX_CH1	Tx	ATX0	
		PCI Express Gen2	GXBR4C_RX_CH1	Rx		
		PCI Express Gen2	GXBR4C_TX_CH0	Tx		
		PCI Express Gen2	GXBR4C_RX_CH0	Rx		
		PCI Express Gen2	GXBL1C_TX_CH5	Tx	fPLL1	1C
		PCI Express Gen2	GXBL1C_RX_CH5	Rx		
		PCI Express Gen2	GXBL1C_TX_CH4	Tx	ATX1	
		PCI Express Gen2	GXBL1C_RX_CH4	Rx		
		1Gb Ethernet	GXBL1C_TX_CH3	Tx		
		1Gb Ethernet	GXBL1C_RX_CH3	Rx		
			REFCLK_GXBL1C_T	Refclk		
			REFCLK_GXBL1C_B	Refclk		
		1Gb Ethernet	GXBL1C_TX_CH2	Tx	fPLL0	
		1Gb Ethernet	GXBL1C_RX_CH2	Rx		
		1Gb Ethernet	GXBL1C_TX_CH1	Tx	ATX0	
		1Gb Ethernet	GXBL1C_RX_CH1	Rx		
		1Gb Ethernet	GXBL1C_TX_CH0	Tx		
		1Gb Ethernet	GXBL1C_RX_CH0	Rx		

Bank Num	Tx PLL	Tx/Rx/ CMU	Physical Channel	Datarate 1	Datarate 2	Datarate 3
4F	fPLL1	Tx	GXBR4F_TX_CH5	9.8Gbps	4.9Gbps	2.5Gbps
		Rx	GXBR4F_RX_CH5	9.8Gbps	4.9Gbps	2.5Gbps
	ATX1	Tx	GXBR4F_TX_CH4	9.8Gbps	4.9Gbps	2.5Gbps
		Rx	GXBR4F_RX_CH4	9.8Gbps	4.9Gbps	2.5Gbps
		Tx	GXBR4F_TX_CH3	9.8Gbps	4.9Gbps	2.5Gbps
		Rx	GXBR4F_RX_CH3	9.8Gbps	4.9Gbps	2.5Gbps
		307MHz	REFCLK_GXBR4F_T			
		Refclk	REFCLK_GXBR4F_B			
	fPLL0	Tx	GXBR4F_TX_CH2	9.8Gbps	4.9Gbps	2.5Gbps
		Rx	GXBR4F_RX_CH2	9.8Gbps	4.9Gbps	2.5Gbps
	ATX0	Tx	GXBR4F_TX_CH1	9.8Gbps	4.9Gbps	2.5Gbps
		Rx	GXBR4F_RX_CH1	9.8Gbps	4.9Gbps	2.5Gbps
		Tx	GXBR4F_TX_CH0	9.8Gbps	4.9Gbps	2.5Gbps
		Rx	GXBR4F_RX_CH0	9.8Gbps	4.9Gbps	2.5Gbps
4E	fPLL1	Tx	GXBR4E_TX_CH5	9.8Gbps	4.9Gbps	2.5Gbps
		Rx	GXBR4E_RX_CH5	9.8Gbps	4.9Gbps	2.5Gbps
	ATX1	Tx	GXBR4E_TX_CH4	9.8Gbps	4.9Gbps	2.5Gbps
		Rx	GXBR4E_RX_CH4	9.8Gbps	4.9Gbps	2.5Gbps
		Tx	GXBR4E_TX_CH3	9.8Gbps	4.9Gbps	2.5Gbps
		Rx	GXBR4E_RX_CH3	9.8Gbps	4.9Gbps	2.5Gbps
		Refclk	REFCLK_GXBR4E_T			
		Refclk	REFCLK_GXBR4E_B			
	fPLL0	Tx	GXBR4E_TX_CH2	9.8Gbps	4.9Gbps	2.5Gbps
		Rx	GXBR4E_RX_CH2	9.8Gbps	4.9Gbps	2.5Gbps
	ATX0	Tx	GXBR4E_TX_CH1	9.8Gbps	4.9Gbps	2.5Gbps
		Rx	GXBR4E_RX_CH1	9.8Gbps	4.9Gbps	2.5Gbps
		Tx	GXBR4E_TX_CH0	9.8Gbps	4.9Gbps	2.5Gbps
		Rx	GXBR4E_RX_CH0	9.8Gbps	4.9Gbps	2.5Gbps
4D	fPLL1	Tx	GXBR4D_TX_CH5	12Gbs Chip to Chip		
		Rx	GXBR4D_RX_CH5	12Gbs Chip to Chip		
	ATX1	Tx	GXBR4D_TX_CH4	12Gbs Chip to Chip		
		Rx	GXBR4D_RX_CH4	12Gbs Chip to Chip		
		Tx	GXBR4D_TX_CH3	12Gbs Chip to Chip		
		Rx	GXBR4D_RX_CH3	12Gbs Chip to Chip		
		Refclk	REFCLK_GXBR4E_T			
		Refclk	REFCLK_GXBR4E_B			
	fPLL0	Tx	GXBR4D_TX_CH2	12Gbs Chip to Chip		
		Rx	GXBR4D_RX_CH2	12Gbs Chip to Chip		
	ATX0	Tx	GXBR4D_TX_CH1	12Gbs Chip to Chip		
		Rx	GXBR4D_RX_CH1	12Gbs Chip to Chip		
		Tx	GXBR4D_TX_CH0	12Gbs Chip to Chip		
		Rx	GXBR4D_RX_CH0	12Gbs Chip to Chip		
4C	fPLL1	Tx	GXBR4C_TX_CH5	12Gbs Chip to Chip		
		Rx	GXBR4C_RX_CH5	12Gbs Chip to Chip		
	ATX1	Tx	GXBR4C_TX_CH4	12Gbs Chip to Chip		
		Rx	GXBR4C_RX_CH4	12Gbs Chip to Chip		
		Tx	GXBR4C_TX_CH3	12Gbs Chip to Chip		
		Rx	GXBR4C_RX_CH3	12Gbs Chip to Chip		
		Refclk	REFCLK_GXBR4C_T			
		625MHz	REFCLK_GXBR4C_B			
	fPLL0	Tx	GXBR4C_TX_CH2	12Gbs Chip to Chip		
		Rx	GXBR4C_RX_CH2	12Gbs Chip to Chip		
	ATX0	Tx	GXBR4C_TX_CH1	12Gbs Chip to Chip		
		Rx	GXBR4C_RX_CH1	12Gbs Chip to Chip		
		Tx	GXBR4C_TX_CH0	12Gbs Chip to Chip		
		Rx	GXBR4C_RX_CH0	12Gbs Chip to Chip		

The 1GbE and 10GbE capable channels in transceiver block 1E implement transceiver PHYs capable of switching between the Standard PCS (configured for 1.25 Gbps), and the Enhanced PCS (configured for 10.3125 Gbps). To assess worst case transceiver VCCT_GXB, and VCCR_GXB current requirements, the Enhanced PCS (configured for 10.3125 Gbps) is the default PHY configuration.

The 9.8 Gbps, 4.9 Gbps, 2.5 Gbps capable channels in transceiver blocks 4E and 4F are implemented using the Standard PCS. To assess worst case power requirements of these transceiver blocks, the transceiver PHY default configuration is 9.8 Gbps.

DFE and AEQ were not used for any channels in this design.

Multiple clock pattern and PRBS core noise generators filling 83% of the device logic were implemented for this design. Vectorless estimation was used to generate the PowerPlay Power Analyzer results.

You should base your power requirement estimates on your actual design.

Table 2: Total Current Estimates from the PPPA for the VCC, VCCP, VCCERAM, VCCR_GXB, and VCCT_GXB Supplies

Power Supply Pin	Voltage(V)	Current (mA)	Power Group
VCC	0.9	32000.00	1
VCCP	0.9	13500.00	1
VCCERAM	0.9	0.045	1
VCCR_GXBL1C	1.0	224.09	3
VCCR_GXBL1D	1.0	403.75	3
VCCR_GXBL1E	1.0	991.02	3
VCCR_GXBL1F	1.0	1021.69	3
VCCR_GXBR4C	1.0	944.15	3
VCCR_GXBR4D	1.0	955.29	3
VCCR_GXBR4E	1.0	667.44	3
VCCR_GXBR4F	1.0	757.41	3
VCCT_GXBL1C	1.0	56.42	2
VCCT_GXBL1D	1.0	78.86	2
VCCT_GXBL1E	1.0	297.65	2
VCCT_GXBL1F	1.0	372.85	2
VCCT_GXBR4C	1.0	356.23	2
VCCT_GXBR4D	1.0	356.23	2
VCCT_GXBR4E	1.0	281.97	2
VCCT_GXBR4F	1.0	298.58	2

The current estimates from the above table were entered in the PDN Tool as shown below:

Figure 4: Power Group Configuration and Current Entry for the Example Design

Family / Device	Arria_10_GX
Available Devices	10AX115N_F45
Power Rail Configuration	Custom

Power Rail Grouping

Add Group | Remove Group

		Group #	1	2	3	4	5
		Regulator / Separator	switcher	switcher	switcher	switcher	filter
		Parent Group	none	none	none	none	4
Rail	Voltage	I max					
VCC	0.9	32	x				
VCCA_PLL	1.8	0.065					x
VCCBAT	1.8	0					x
VCCERAM	0.9	0.045	x				
VCCH_GXBL	1.8	1.138					x
VCCH_GXBR	1.8	1.272					x
VCCIO2A	1.8	0.05				x/related	
VCCIO2F	1.8	0.002				x/related	
VCCIO2G	1.8	0.004				x/related	
VCCIO2H	1.8	0.004				x/related	
VCCIO2I	1.8	0.001				x/related	
VCCIO2J	1.8	0.004				x/related	
VCCIO2K	1.8	0.004				x/related	
VCCIO2L	1.8	0.004				x/related	
VCCIO3A	1.8	0.004				x/related	
VCCIO3B	1.8	0.004				x/related	
VCCIO3C	1.8	0.004				x/related	
VCCIO3D	1.8	0.05				x/related	
VCCIO3E	1.8	0.004				x/related	
VCCIO3F	1.8	0.004				x/related	
VCCIO3G	1.8	0.004				x/related	
VCCIO3H	1.8	0.007				x/related	
VCCP	0.9	13.5	x				
VCCPGM	1.8	0				x	
VCCPT	1.8	0.792				x	
VCCR_GXBL1C	1	0.224			x/related		
VCCR_GXBL1D	1	0.404			x/related		
VCCR_GXBL1E	1	0.991			x/related		
VCCR_GXBL1F	1	1.022			x/related		
VCCR_GXBR4C	1	0.944			x/related		
VCCR_GXBR4D	1	0.955			x/related		
VCCR_GXBR4E	1	0.667			x/related		
VCCR_GXBR4F	1	0.757			x/related		
VCCT_GXBL1C	1	0.056		x/related			
VCCT_GXBL1D	1	0.078		x/related			
VCCT_GXBL1E	1	0.298		x/related			
VCCT_GXBL1F	1	0.373		x/related			
VCCT_GXBR4C	1	0.356		x/related			
VCCT_GXBR4D	1	0.356		x/related			
VCCT_GXBR4E	1	0.282		x/related			
VCCT_GXBR4F	1	0.299		x/related			

Because of the high number of channels clocked from single ATX PLLs **x/related** is chosen for the VCCT_GXB and VCCR_GXB supplies in this design. With the **x/related** setting, the PDN Tool assumes the supplies have synchronous switching and hence higher dynamic current. This makes the PDN design more challenging, but is a worst case scenario as not all channels are synchronous. Assess if you should select **x** or **x/related** for your design.

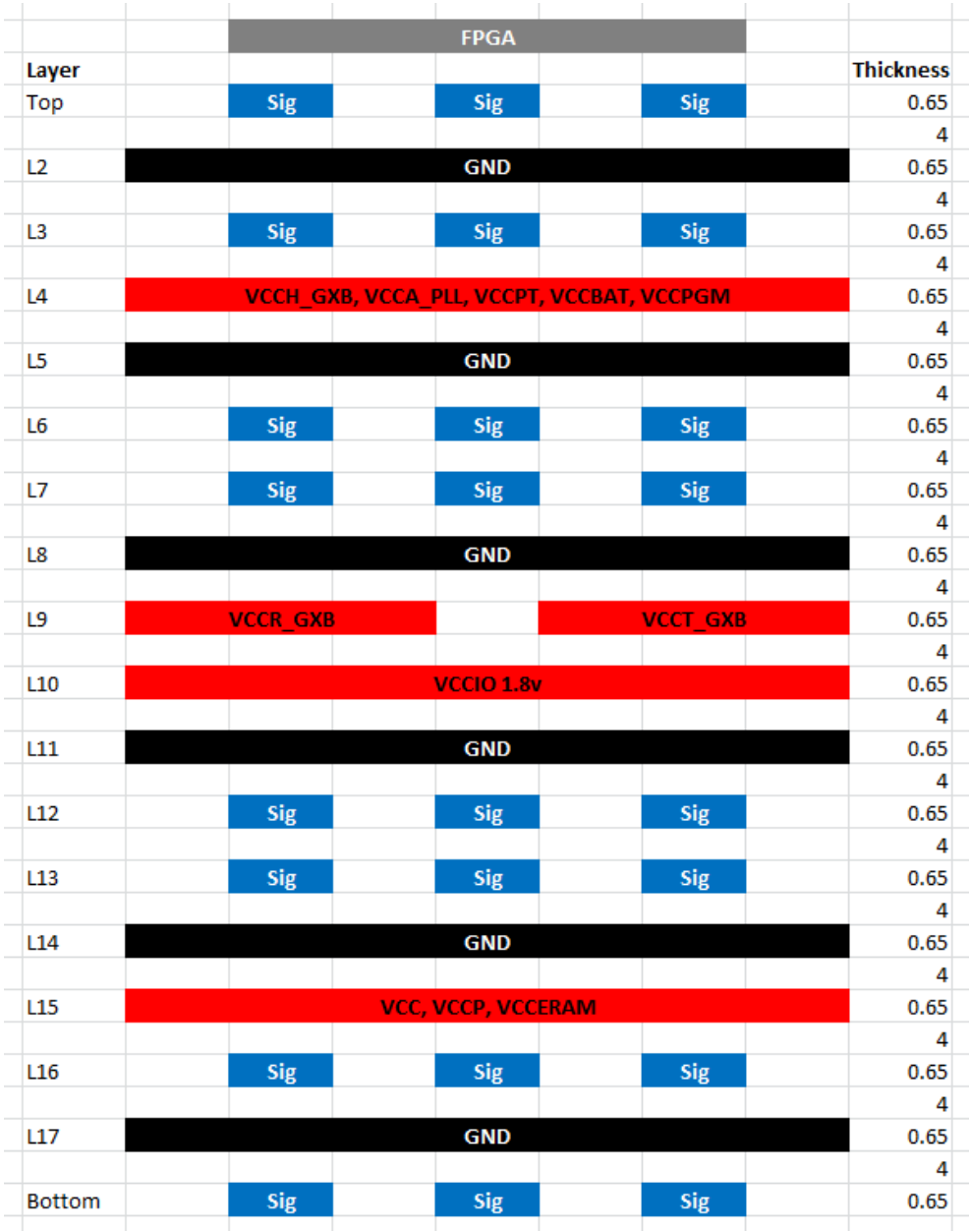
PDN Design Optimization Study

This PDN design optimization study uses the previously determined current estimates with a sub-optimal PCB design in terms of PDN performance. It demonstrates step improvements in the PDN performance at each optimization stage. The goal is to improve the PDN efficiency as observed through an increase in the effective frequency (Feffective) for the VCC supply. It is easier to meet Ztarget with an inefficient PDN, but you should target the highest possible Feffective for your design. The VCCT_GXB and VCCR_GXB supplies have a fixed 70MHz frequency target. Optimizing the PDN results in the total number of PCB mounted decoupling capacitors being reduced. The design study discusses PCB optimization and the importance of minimizing spreading and vertical inductance in the PDN. The importance of increasing the power and ground plane capacitance is also demonstrated. Alternative capacitor technologies and their significant effect on PDN efficiency are then demonstrated resulting in fewer PCB mounted capacitors. Finally, a novel high-frequency de-rating of the VCC supply in the PDN Tool demonstrates a further dramatic reduction in the number of required decoupling capacitors.

Initial Stackup Entry

The initial layer-stack of this design study is shown below.

Figure 5: Initial Stackup



When entered into the PDN Tool, and **Auto** decoupling mode is selected for all power groups, it reports 301 capacitors are required to decouple each of the VCC, VCCT_GXB and VCCR_GXB supplies. When the PDN Tool decoupling mode is set to **Auto**, it will not add more than 301 capacitors. In reality, more than 301 capacitors will be required to decouple the design. Fitting in excess of 903 capacitors for three supplies is unrealistic so optimization of the PCB PDN is required.

Auto decoupling mode is used throughout this application note.

Figure 6: Initial Number of Required Decoupling Capacitors

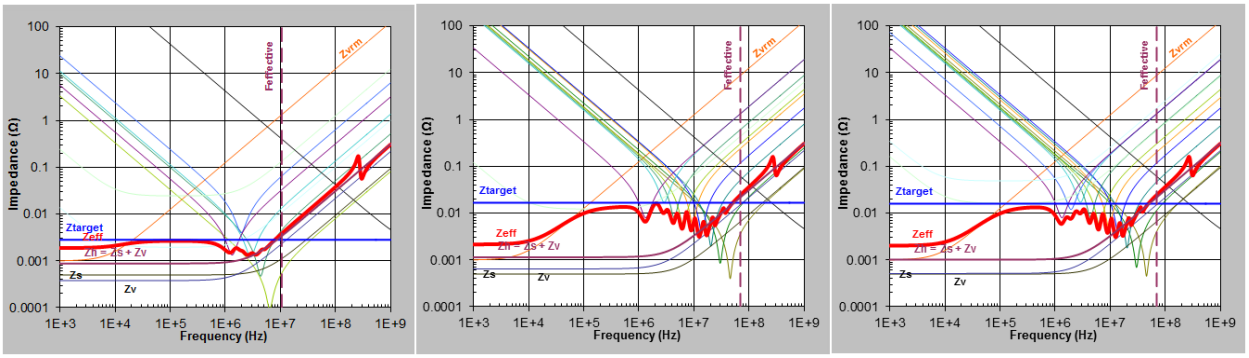
Result Summary

		Decoupling Caps				Rail Group Quantity		
Legend	CAP	Value (µF)	Footprint	Layer	Orientation	1	2	3
Zc1	From Library	0.001	0201	BOTTOM	VOS	0	0	0
Zc2		0.0022	0201	BOTTOM	VOS	0	0	0
Zc3		0.0047	0201	BOTTOM	VOS	0	161	181
Zc4		0.01	0402	BOTTOM	VOS	0	87	71
Zc5		0.022	0402	BOTTOM	VOS	0	24	22
Zc6		0.047	0402	BOTTOM	VOS	0	10	10
Zc7		0.1	0402	BOTTOM	VOS	0	6	5
Zc8		0.22	0402	BOTTOM	VOS	217	4	4
Zc9		0.47	0402	BOTTOM	VOS	34	2	2
Zc10		1	0603	BOTTOM	VOS	14	1	1
Zc11		2.2	0603	BOTTOM	VOS	3	1	0
Zc12		4.7	0603	BOTTOM	VOS	6	1	1
Zc13	User1	0	1206	BOTTOM	VOS	0	0	0
Zc14	User2	0	0201	BOTTOM	VOS	0	0	0
Zc15	User3	0	0603	BOTTOM	VOS	0	0	0
Zc16	User4	0	0201	BOTTOM	VOS	0	0	0

		Bulk Caps				Rail Group Quantity		
Legend	CAP	Value (µF)	Footprint	Layer	Orientation	1	2	3
Zc17	From Library	10	Bulk	N/A	N/A	0	0	0
Zc18		22	Bulk			0	0	0
Zc19		47	Bulk			0	0	0
Zc20		100	Bulk			0	0	0
Zc21		220	Bulk			0	0	0
Zc22		330	Bulk			2	3	4
Zc23		470	Bulk			25	1	0
Zc24	User5	0	Custom			0	0	0
Zc25	User6	0	Custom			0	0	0
		Total Decoupling & Bulk Capacitors Used				301	301	301

The following figure shows the impedance plots for VCC, VCCT_GXB and VCCR_GXB with this initial stackup and PDN Tool configuration.

Figure 7: Initial VCC, VCCT_GXB, and VCCR_GXB Supply Impedance Plots



With this initial stackup and PDN Tool configuration, Feffective for the VCC supply is reported to be just 10.62MHz and the target Feffective of 70MHz for VCCT_GXB and VCCR_GXB supplies are not met. This is because the initial stackup, layer allocation, and PDN is not optimized, resulting in an inefficient PDN.

Figure 8: Initial VCC Supply Feffective

Feffective		Calculate	Calculate	Calculate	Calculate	Calculate
	MHz	10.62	70.00	70.00	70.00	70.00

Using the Correct Number of Power/Ground Via Pairs

Unless you change manually, the PDN Tool sets the **Number of Power/Ground Via Pairs** for each power group to the default value defined on the **Stackup** tab. For this case it is 50 as shown by the figure below.

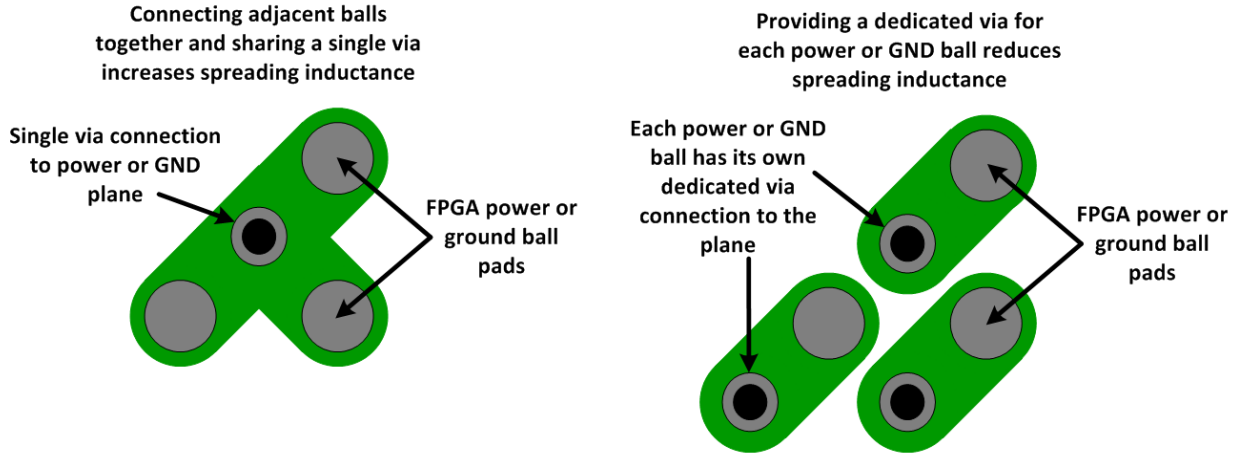
Figure 9: Incorrect Number of Power/Ground Via Pairs and Layer Number

BGA Via		Calculate	Calculate	Calculate	Calculate	Calculate
Number of power/Ground Via Pairs		50	50	50	50	50
Layer Number		18	18	18	18	18
	R(Ω)	0.000355226	0.000355226	0.000355226	0.000355226	0.000355226
	L (nH)	0.034523169	0.034523169	0.034523169	0.034523169	0.034523169

PCB PDN design is highly dependent on the **Number of Power/Ground Via Pairs**. This contributes to the spreading inductance (Ls) in the PDN design. If the actual **Number of Power/Ground Via Pairs** in the PCB is less than the number defined in the PDN Tool, the PDN Tool reports optimistic results. It is important to set the correct **Number of Power/Ground Via Pairs** to match your device and PCB.

Always provide a dedicated via connecting each power and ground pin on the FPGA to the plane. For more information on the importance of the number of power and ground pin pairs refer to *Knowledge Database* note.

Figure 10: Number of power and ground pin pairs



An increase in the **Number of Power/Ground Via Pairs** between the plane and FPGA reduces spreading inductance (Ls) and increases the high-frequency current delivery efficiency from the plane to the FPGA. This results in increasing the maximum effective frequency of the PCB PDN.

Related Information

Can I connect multiple power or GND pins to their planes through a single via with Altera devices?

Using the Correct Number of Power/Ground Via Pairs and Layer Number

Unless you change manually, the PDN Tool initially sets all power groups to the same **Layer Number** . For this example it is 18. You must change this to match your PCB design.

Long vias between the plane and FPGA have higher vertical loop inductance than short vias. The planes placed farther from the FPGA have higher loop inductance. Because inductance impedes high-frequency current delivery, it reduces the effective maximum frequency of the PDN. To reduce loop inductance, you can place planes closer to the FPGA.

Corrected Number of Power/Ground Via Pairs and Layer Numbers

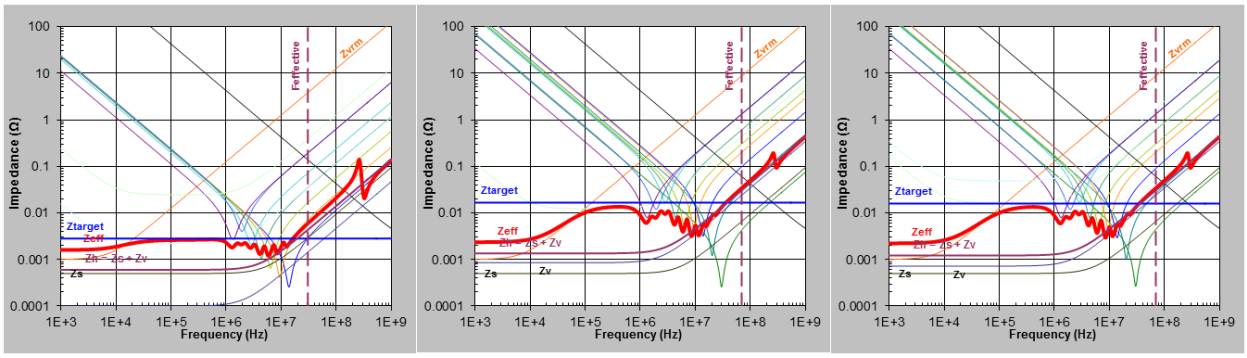
You should use the correct number of power and ground via pairs for your device. This can be found in the device pinout data. This example uses an AX115N_F45 device selection from the PDN Tool and the initial power plane allocation, the **Number of Power/Ground Via Pairs** and **Layer Number** data is corrected and entered into the PDN Tool as shown below:

Figure 11: Correct Number of Power/Ground Via Pairs and Layer Number

BGA Via		Calculate	Calculate	Calculate	Calculate	Calculate
Number of power/Ground Via Pairs		197	16	16	65	11
Layer Number		15	9	9	10	4
	R(Ω)	7.62252E-05	0.000563114	0.000563114	0.000154014	0.000364033
	L (nH)	0.007408063	0.054727069	0.054727069	0.014968087	0.035379115

With the corrected **Number of Power/Ground Via Pairs** and **Layer Number** data, the total number of required decoupling capacitors remains at 301 for the VCC, VCCT_GXB and VCCR_GXB supplies. The VCC, VCCT_GXB, and VCCR_GXB Impedance plots are shown below.

Figure 12: VCC, VCCT_GXB, and VCCR_GXB PDN Performance with corrected Number of Power/Ground Via Pairs and Layer Numbers



The following figure shows that the VCC supply Feffective parameter has increased from 10.62MHz to 30.68MHz. The increase in performance is due to an increase in the number of power/ground vias from 50 to 197, and a reduction in spreading inductance (Ls). The vertical loop inductance is reduced by moving the VCC supply plane closer to the FPGA from Layer 18 to Layer 15.

Figure 13: VCC Supply Feffective with corrected Number of Power/Ground Via Pairs and Layer Numbers

Feffective		Calculate	Calculate	Calculate	Calculate	Calculate
	MHz	30.68	70.00	70.00	70.00	70.00

In contrast, the VCCT_GXB and VCCR_GXB supply impedance plots shows a lower frequency Zeffective and Ztarget intersect and hence worse PDN performance. This is because the **Number of Power/Ground Via Pairs** was corrected from 50 to 16 and the spreading inductance increased. The reduction in performance is despite the planes moving closer to the FPGA from Layer 18 to Layer 9, resulting in a reduction in vertical loop inductance.

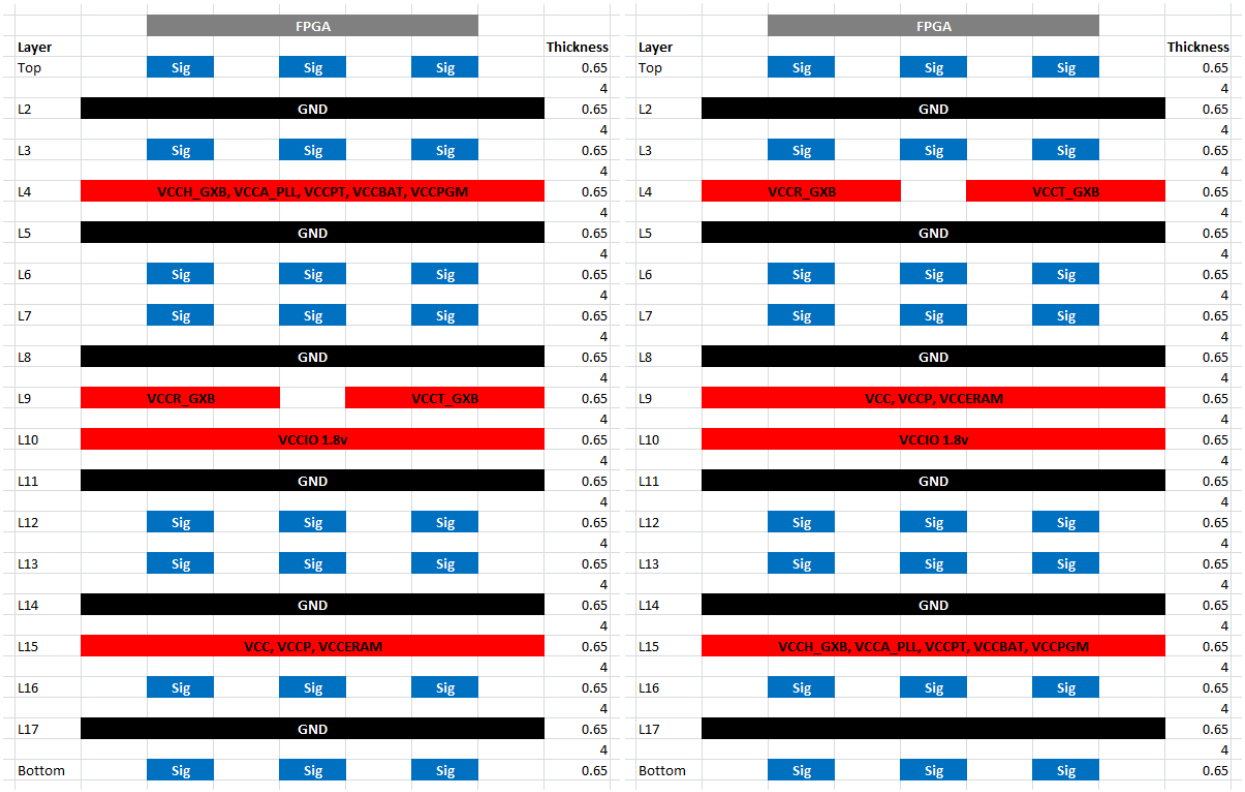
Moving Supplies to Optimal Layers

Reducing the spreading inductance (Ls) between the planes and the FPGA increases the effective frequency of the VCC supply. Re-allocating the FPGA supply rails in the layer-stack so that they have lower vertical inductance, will also show an improvement.

Moving the VCCT_GXB and VCCR GXB supplies from Layer 9 to Layer 4, and the VCC supply from Layer 15 to Layer 9, brings them closer to the FPGA with a lower vertical loop inductance.

The following figure shows a comparison between the initial supply layer allocation on the left with the new allocation on the right.

Figure 14: Original Layer Allocation (Left) Versus New Layer Allocation (Right)



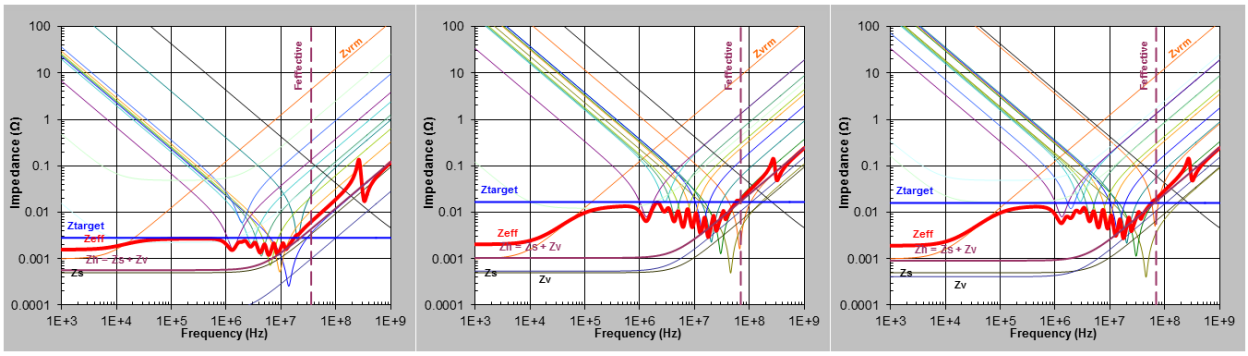
As a result of these changes, the PDN Tool reports that the VCC supply Feffective has improved from 30.68MHz to 35.61MHz.

Figure 15: VCC Supply Feffective with Better Supply Plane Allocation

Feffective		Calculate	Calculate	Calculate	Calculate	Calculate
	MHz	35.61	70.00	70.00	70.00	70.00

The following figure shows that VCCT_GXB and VCCR_GXB supply impedances are close to meeting the 70MHz target. However, further optimization is required because more than 301 capacitors are still required for each of the three supplies.

Figure 16: VCC, VCCT_GXB, and VCCR_GXB Supply PDN Performance with Better Supply Plane Allocation



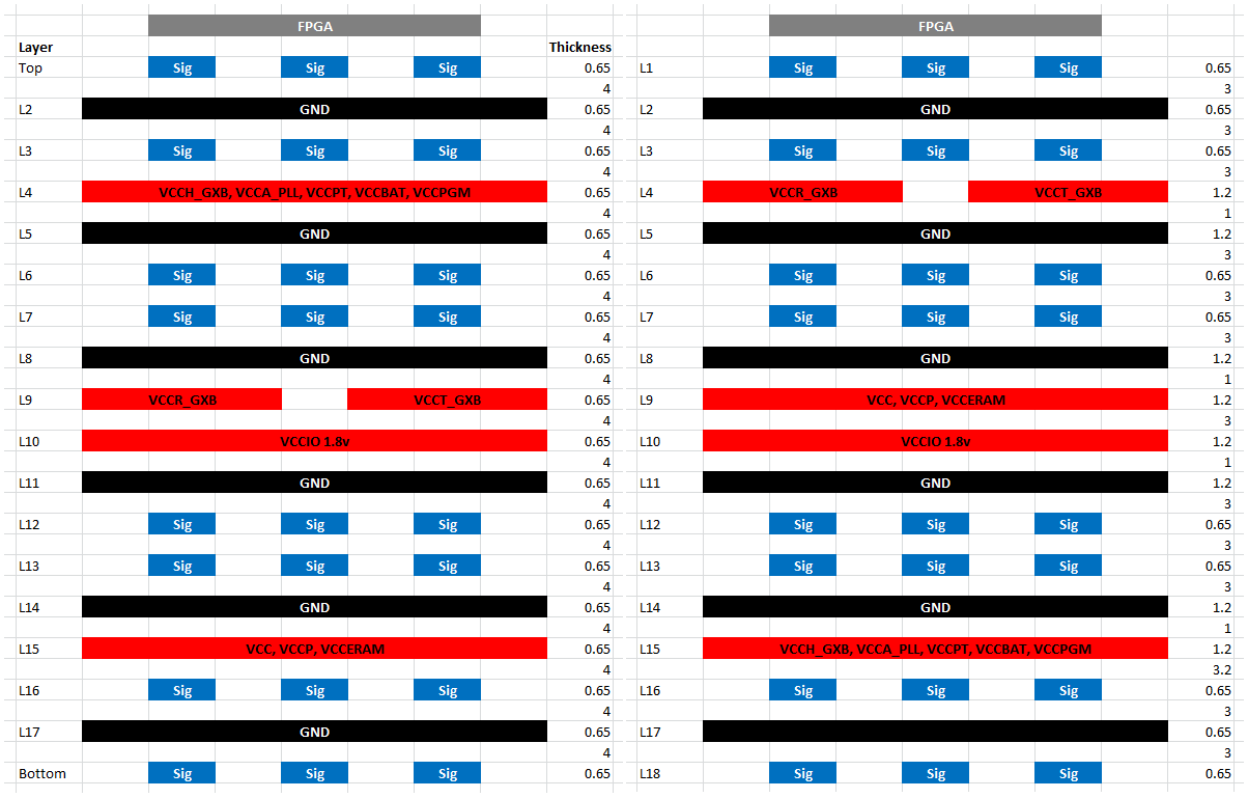
Moving Power and Ground Planes Closer Together

The impedance plots imply the challenge is in meeting the target impedance at high frequencies. Higher frequency decoupling can be achieved by increasing the capacitance of the power and ground supply planes. This can be achieved by moving the power and ground plane pair closer to each other.

Increasing the surface area of the power and ground plane pair also increases the inter-plane capacitance. The default PDN Tool plane size is used throughout this application note. You can change the plane capacitance and resistance for each power group in the PDN Tool.

Reducing the original stackup power and ground separation to 1 mil from 4 mils should show an improvement. In the following example, in order to reduce plane resistance, the plane thickness of the power/ground pairs has been increased to 1.2 mil. The figure below compares the original layer-stack (left) with the new stack (right).

Figure 17: Original Stackup (Left) Versus Revised Stackup with Thinner Power and Ground Plane Separation (Right)



The PDN Tool shows that moving the power and ground planes closer together increases the VCC supply Feffective to 36.71MHz.

Figure 18: VCC Supply Feffective after reducing the Power and Ground Plane Separation

Feffective		Calculate	Calculate	Calculate	Calculate	Calculate
	MHz	36.71	70.00	70.00	70.00	70.00

Moving the power and ground planes closer together reduces the number of decoupling capacitors for the VCCR_GXB supply to 239. More than 301 capacitors are still required for VCC and VCCT_GXB.

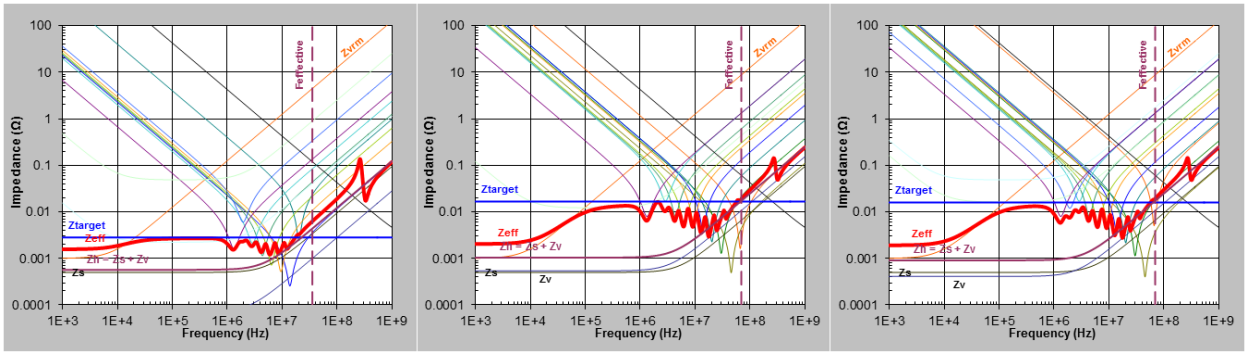
Figure 19: Capacitors Required for the VCC, VCCT_GXB, and VCCR_GXB Supplies after Reducing the Power and Ground Plane Separation

Result Summary

		Decoupling Caps				Rail Group Quantity		
Legend	CAP	Value (µF)	Footprint	Layer	Orientation	1	2	3
Zc1	From Library	0.001	0201	BOTTOM	VOS	0	0	0
Zc2		0.0022	0201	BOTTOM	VOS	0	96	79
Zc3		0.0047	0201	BOTTOM	VOS	0	127	96
Zc4		0.01	0402	BOTTOM	VOS	0	38	33
Zc5		0.022	0402	BOTTOM	VOS	14	16	13
Zc6		0.047	0402	BOTTOM	VOS	162	8	7
Zc7		0.1	0402	BOTTOM	VOS	51	4	2
Zc8		0.22	0402	BOTTOM	VOS	25	3	2
Zc9		0.47	0402	BOTTOM	VOS	11	2	1
Zc10		1	0603	BOTTOM	VOS	8	1	1
Zc11		2.2	0603	BOTTOM	VOS	1	1	1
Zc12		4.7	0603	BOTTOM	VOS	6	1	0
Zc13	User1	0	1206	BOTTOM	VOS	0	0	0
Zc14	User2	0	0201	BOTTOM	VOS	0	0	0
Zc15	User3	0	0603	BOTTOM	VOS	0	0	0
Zc16	User4	0	0201	BOTTOM	VOS	0	0	0

		Bulk Caps				Rail Group Quantity		
Legend	CAP	Value (µF)	Footprint	Layer	Orientation	1	2	3
Zc17	From Library	10	Bulk	N/A	N/A	0	0	0
Zc18		22	Bulk			0	0	0
Zc19		47	Bulk			0	0	0
Zc20		100	Bulk			0	0	4
Zc21		220	Bulk			0	0	0
Zc22		330	Bulk			1	3	0
Zc23		470	Bulk			22	1	0
Zc24	User5	0	Custom			0	0	0
Zc25	User6	0	Custom			0	0	0
		Total Decoupling & Bulk Capacitors Used				301	301	239

Figure 20: VCC, VCCT_GXB, and VCCR_GXB Supply PDN Performance after Reducing the Power and Ground Plane Separation



It is clear that improvements in the PCB result in better VCC performance and requires fewer PCB decoupling capacitors for the VCCR_GXB supply but optimization is still required.

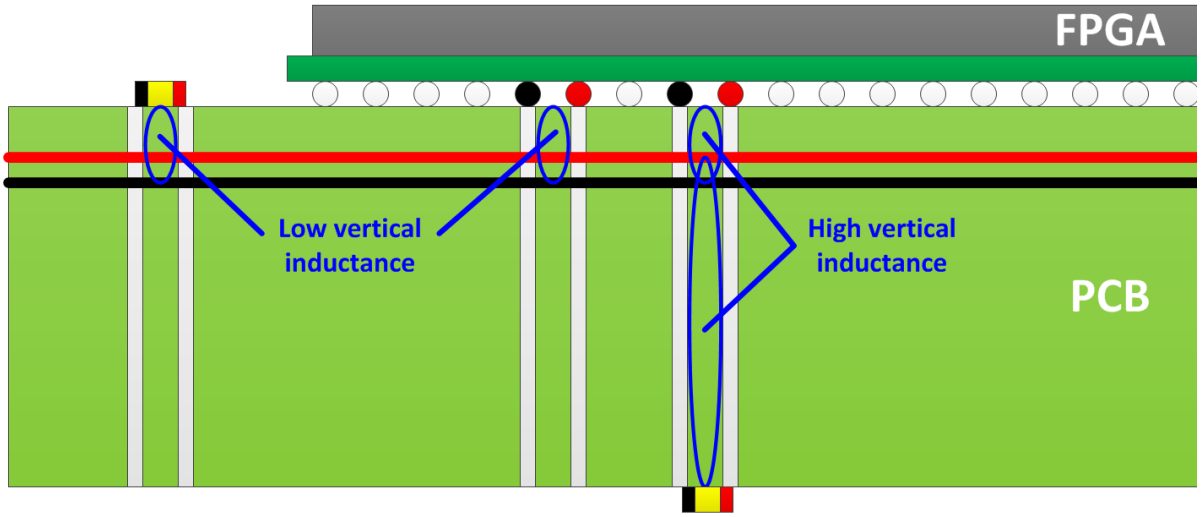
Move Decoupling Capacitors to the Top Surface of the PCB

In all steps so far, the decoupling capacitors are placed on the bottom surface of the PCB and the FPGA is placed on the top.

Traditionally the decoupling capacitors are placed at the bottom side of the PCB, beneath the FPGA and connect directly to the BGA vias. It is assumed that the best electrical position is the closest physical location to the FPGA pins.

In the layer-stack if the power and ground plane pair are close to the FPGA, the total vertical inductance of the vias between the capacitors and plane, and between the plane and FPGA is less if the decoupling capacitors are placed on the top surface of the PCB.

Assuming wide contiguous power and ground planes that have thin separation, the inductance is much lower even though the physical horizontal distance of the capacitors placed around the outside of the FPGA is far greater.



In this 18 Layer example, the VCCT_GXB, and VCCR_GXB supplies are allocated to layer 4 which is closer to the FPGA than the mid point in the layer-stack. Therefore if the capacitors are placed on the top surface of the PCB, the combined vertical loop inductance between decoupling capacitor to plane, and plane to FPGA is lower.

Providing the PDN Tool with the freedom to place capacitors on either the top or bottom surface of the PCB can be achieved by duplicating entries for select capacitor values. You can allocate one to the top surface, and the other to the bottom surface. This is shown below with the effect that the number of capacitors required for the VCCT_GXB, and VCCR_GXB supplies is reduced to 255 and 180 respectively.

Figure 21: Capacitors Required for the VCC, VCCT_GXB, and VCCR_GXB Supplies After Moving Capacitors to the Top Surface

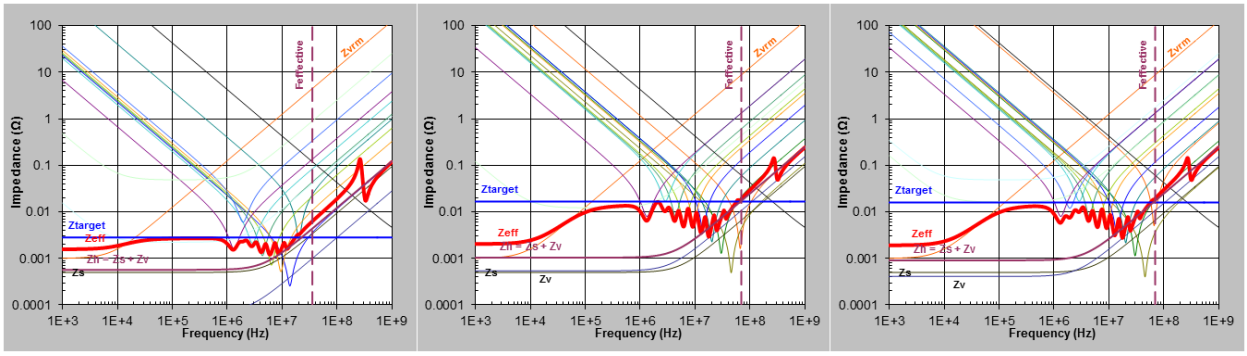
Result Summary

		Decoupling Caps				Rail Group Quantity		
Legend	CAP	Value (µF)	Footprint	Layer	Orientation	1	2	3
Zc1	From Library	0.022	0201	TOP	VOS	0	247	162
Zc2		0.022	0201	BOTTOM	VOS	5	0	0
Zc3		0.1	0201	TOP	VOS	221	3	9
Zc4		0.1	0402	BOTTOM	VOS	0	0	0
Zc5		0.22	0402	TOP	VOS	25	0	2
Zc6		0.22	0402	BOTTOM	VOS	0	0	0
Zc7		0.47	0402	TOP	VOS	10	0	1
Zc8		0.47	0402	BOTTOM	VOS	0	0	0
Zc9		1	0402	TOP	VOS	6	0	0
Zc10		1	0603	BOTTOM	VOS	3	0	2
Zc11		4.7	0603	TOP	VOS	2	1	0
Zc12		4.7	0603	BOTTOM	VOS	6	0	0
Zc13	User1	0	1206	BOTTOM	VOS	0	0	0
Zc14	User2	0	0201	BOTTOM	VOS	0	0	0
Zc15	User3	0	0603	BOTTOM	VOS	0	0	0
Zc16	User4	0	0201	BOTTOM	VOS	0	0	0

		Bulk Caps				Rail Group Quantity		
Legend	CAP	Value (µF)	Footprint	Layer	Orientation	1	2	3
Zc17	From Library	10	Bulk	N/A	N/A	0	0	0
Zc18		22	Bulk			0	0	0
Zc19		47	Bulk			0	0	0
Zc20		100	Bulk			0	4	4
Zc21		220	Bulk			0	0	0
Zc22		330	Bulk			1	0	0
Zc23		470	Bulk			22	0	0
Zc24	User5	0	Custom			0	0	0
Zc25	User6	0	Custom			0	0	0
		Total Decoupling & Bulk Capacitors Used				301	255	180

The target impedance is now met up to 70MHz for the VCCT_GXB, and VCCR_GXB supplies but the large number of high-frequency 22nF capacitors shows there are still challenges in achieving Ztarget at high-frequencies.

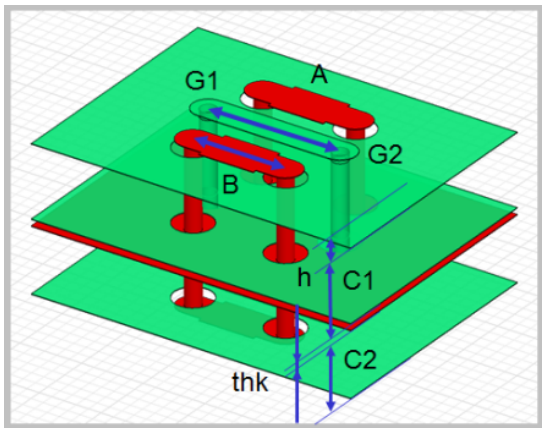
Figure 22: VCC, VCCT_GXB, and VCCR_GXB Supply PDN Performance After Moving Capacitors to the Top Surface



Using X2Y Decoupling Capacitors

As discussed, inductance is a big contributor in failing to meet target impedance at high-frequencies. The decoupling capacitors used already specify Via On Side (VOS) mounting which has lower mounting inductance (Lmnt), than Via On End (VOE). 0402 and 0201 capacitor case sizes that have lower Lmnt than 0603 or 0805 are also used. Previously, significant improvements in performance were found by increasing the number of FPGA power and ground via pairs. Using this technique with ultra-low mounting inductance X2Y capacitors can show significant improvements. The figure below shows an example of an X2Y capacitor mounting with two GND vias and four power vias. Effectively the spreading inductance of the capacitor has been reduced.

Figure 23: Example of a X2Y Capacitor Mounting with two GND Vias and Four Power Vias



Using X2Y capacitors in the PDN Tool reduces the number of capacitors required to meet the target impedance of the VCCT_GXB, and VCCR_GXB supplies from 255 and 180 to 28 and 22 respectively.

Figure 24: Capacitors Required for the VCC, VCCT_GXB, and VCCR_GXB Supplies When Using X2Y Capacitors

Result Summary

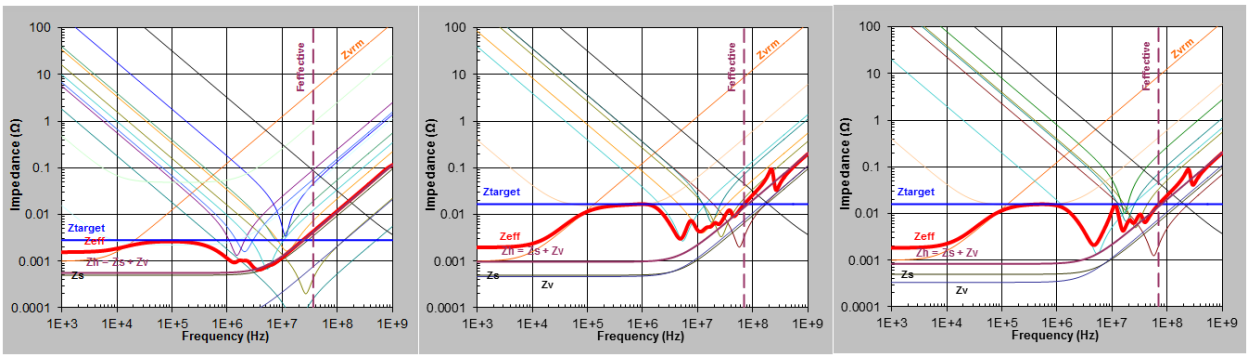
		Decoupling Caps				Rail Group Quantity		
Legend	CAP	Value (µF)	Footprint	Layer	Orientation	1	2	3
Zc1	From Library	0.022	0603_X2Y	TOP	VOS	0	16	10
Zc2		0.022	0603_X2Y	BOTTOM	VOS	0	0	0
Zc3		0.1	0603_X2Y	TOP	VOS	50	2	3
Zc4		0.1	0603_X2Y	BOTTOM	VOS	0	1	0
Zc5		0.22	0603_X2Y	TOP	VOS	200	1	1
Zc6		0.22	0603_X2Y	BOTTOM	VOS	2	0	0
Zc7		0.47	0603_X2Y	TOP	VOS	5	0	2
Zc8		0.47	0603_X2Y	BOTTOM	VOS	0	0	0
Zc9		1	0603_X2Y	TOP	VOS	2	0	0
Zc10		1	0603_X2Y	BOTTOM	VOS	8	4	2
Zc11		4.7	0603	TOP	VOS	5	0	0
Zc12		4.7	0603	BOTTOM	VOS	6	0	0
Zc13	User1	0	1206	BOTTOM	VOS	0	0	0
Zc14	User2	0	0201	BOTTOM	VOS	0	0	0
Zc15	User3	0	0603	BOTTOM	VOS	0	0	0
Zc16	User4	0	0201	BOTTOM	VOS	0	0	0

		Bulk Caps				Rail Group Quantity		
Legend	CAP	Value (µF)	Footprint	Layer	Orientation	1	2	3
Zc17	From Library	10	Bulk	N/A	N/A	0	0	0
Zc18		22	Bulk			0	0	0
Zc19		47	Bulk			0	0	0
Zc20		100	Bulk			0	4	4
Zc21		220	Bulk			0	0	0
Zc22		330	Bulk			1	0	0
Zc23		470	Bulk			22	0	0
Zc24	User5	0	Custom			0	0	0
Zc25	User6	0	Custom			0	0	0
		Total Decoupling & Bulk Capacitors Used				301	28	22

Using X2Y capacitors made a big improvement in the PDN efficiency. The intention of this application note was to first optimize the PCB, and then consider different capacitor technologies. The X2Y capacitors could have been used earlier in the flow, but without the underlying PCB optimization less improvement may be seen.

The impedance plots for the VCCT_GXB, and VCCR_GXB supplies shown below indicate a much cleaner impedance profile than before. The VCC supply still requires more than 301 capacitors so effort is still required to meet the target impedance.

Figure 25: VCC, VCCT_GXB, and VCCR_GXB Supply PDN Performance When Using X2Y Capacitors



Using Ultra–Low ESR Bulk Capacitors

Significant improvements were made using low ESL X2Y capacitors instead of standard packaged capacitors. Some improvements can be made at low frequencies by using ultra-low Effective Series Resistance (ESR) bulk capacitors. Ultra-low ESR bulk capacitors can have very low resistances of 5mR when compared with approximately 50mR for standard bulk capacitors. You can use Ultra-low ESR bulk capacitors to reduce the number of bulk capacitors required for meeting Ztarget at low frequencies.

Enter parameters of your own user capacitors in the **Library** tab of the PDN Tool. In this example, 680uF and 1000uF Panasonic POSCAP Tantalum-Polymer Capacitors with an ESR of 0.005 were used. 0.005 is entered for **User5** and **User6** of the **Bulk Cap ESR(R)** column. On the **System Decap** tab **680** and **1000** is entered for **User5** and **User6**. In this case the higher 680uF and 1000uF may also help to reduce the total capacitor count. The PDN Tool reports that using ultra-low ESR capacitors reduces bulk capacitor count of the VCC, VCCT_GXB, and VCCR_GXB supplies as shown below.

Figure 26: Capacitors Required for the VCC, VCCT_GXB, and VCCR_GXB Supplies when Ultra-Low ESR Bulk Capacitors

Result Summary

		Decoupling Caps				Rail Group Quantity		
Legend	CAP	Value (µF)	Footprint	Layer	Orientation	1	2	3
Zc1	From Library	0.022	0603_X2Y	TOP	VOS	0	16	13
Zc2		0.022	0603_X2Y	BOTTOM	VOS	0	0	0
Zc3		0.1	0603_X2Y	TOP	VOS	53	1	0
Zc4		0.1	0603_X2Y	BOTTOM	VOS	0	1	0
Zc5		0.22	0603_X2Y	TOP	VOS	200	0	3
Zc6		0.22	0603_X2Y	BOTTOM	VOS	2	0	0
Zc7		0.47	0603_X2Y	TOP	VOS	5	0	0
Zc8		0.47	0603_X2Y	BOTTOM	VOS	0	0	0
Zc9		1	0603_X2Y	TOP	VOS	1	1	0
Zc10		1	0603_X2Y	BOTTOM	VOS	10	1	2
Zc11		4.7	0603	TOP	VOS	6	2	1
Zc12		4.7	0603	BOTTOM	VOS	7	0	0
Zc13	User1	0	1206	BOTTOM	VOS	0	0	0
Zc14	User2	0	0201	BOTTOM	VOS	0	0	0
Zc15	User3	0	0603	BOTTOM	VOS	0	0	0
Zc16	User4	0	0201	BOTTOM	VOS	0	0	0

		Bulk Caps				Rail Group Quantity		
Legend	CAP	Value (µF)	Footprint	Layer	Orientation	1	2	3
Zc17	From Library	10	Bulk	N/A	N/A	0	0	0
Zc18		22	Bulk			0	0	0
Zc19		47	Bulk			0	0	0
Zc20		100	Bulk			0	2	2
Zc21		220	Bulk			0	0	0
Zc22		330	Bulk			0	0	0
Zc23		470	Bulk			0	0	0
Zc24	User5	680	Custom			4	1	1
Zc25	User6	1000	Custom			13	0	0
		Total Decoupling & Bulk Capacitors Used				301	25	22

The VCCT_GXB, and VCCR_GXB supplies now require 25 and 22 capacitors respectively. VCC bulk capacitors are reduced from 23 to 17 when using ultra-low ESR bulk capacitors. However the target impedance is still not met at high frequencies.

The PCB, stackup, layer allocation and capacitor use and placement are now highly optimized. Further evaluation of the supply rail layers can still be done. The VCC supply is placed on Layer 9, but VCCT_GXB, and VCCR_GXB are placed on Layer 4. Layer 4 is more optimal because it has less vertical inductance.

Swapping VCC on Layer 9 with VCC, VCCT_GXB, and VCCR_GXB on Layer 4

Swapping VCC on Layer 9 with VCCT_GXB and VCCR_GXB on Layer 4 to see the effect of moving the VCC supply closer to the FPGA at the expense of the VCCT_GXB and VCCR_GXB supplies has the effect of improving the VCC Feffective to 38.78MHz. All three supplies now require greater than 301 capacitors so this is not a viable solution because the VCCT_GXB and VCCR_GXB supplies may be insufficiently decoupled. For this design example, we keep VCC on Layer 9, and VCCT_GXB and VCCR_GXB on Layer 4.

Assessing How Much Total Capacitance Might be Required

Changing the PDN Tool **Decoupling Mode** from **Auto** to **Manual** allows you to enter any number of capacitors instead of limiting you to a maximum of 301. This is useful not only for implementing your own custom scheme, but also to estimate how much total capacitance is required to meet the target impedance with your PCB. For example, by entering 99999 high-frequency 22nF capacitors, you can see that Feffective does not increase much. It is very difficult to optimize the PDN any further even with this unrealistic number of capacitors. In this example we switch back to **Auto** decoupling mode.

In this case you can re-estimate and reduce where possible your power requirements, or you can estimate your **Core Clock Frequency** and **Current Ramp Up Period** parameters for the VCC supply.

Using the Core Clock Frequency and Current Ramp Up Period Parameters

On chip noise can be split into two categories. High frequency noise and low frequency noise. High frequency noise is generated by the transistor switching activities and is mainly regulated by die capacitance. Low frequency noise is generated by the average current fluctuation and has to be regulated by on package and PCB decoupling capacitors. It takes time for the average current to ramp up or down. Some applications, such as DSP and matrix operation, can cause current surge in a short period while current change in normal applications may take 25 clock cycles or more to settle down. The current transition time affects the PCB decoupling requirement and can be used to de-rate the target impedance. For more details refer to *Improving the Target Impedance Method for PCB Decoupling of Core Power*.

Some PDN tool variants allow you to add data for the **Core Clock Frequency** and **Current Ramp Up Period** parameters using the pull-down menus. These values tell the tool how to calculate the current ramp up period for transient events, sometimes reducing transient current changes. The values relate to how fast the clock for the section is running, and the length of the data pipeline. Given a transient change in the input data, there are clock cycles in the pipeline for the algorithm to deliver the results. If the input data change activates a broad yet short pipeline, the transient is abrupt. This results in a large current change for the number of logic elements you are using. If the pipeline is narrow and long, the overall change in current usage is proportionately smaller

You can set the **Core Clock Frequency** parameter to a **High**, **Medium**, **Low**, or **Custom** set of input frequencies. The **Custom** option allows you to enter a specific input frequency.

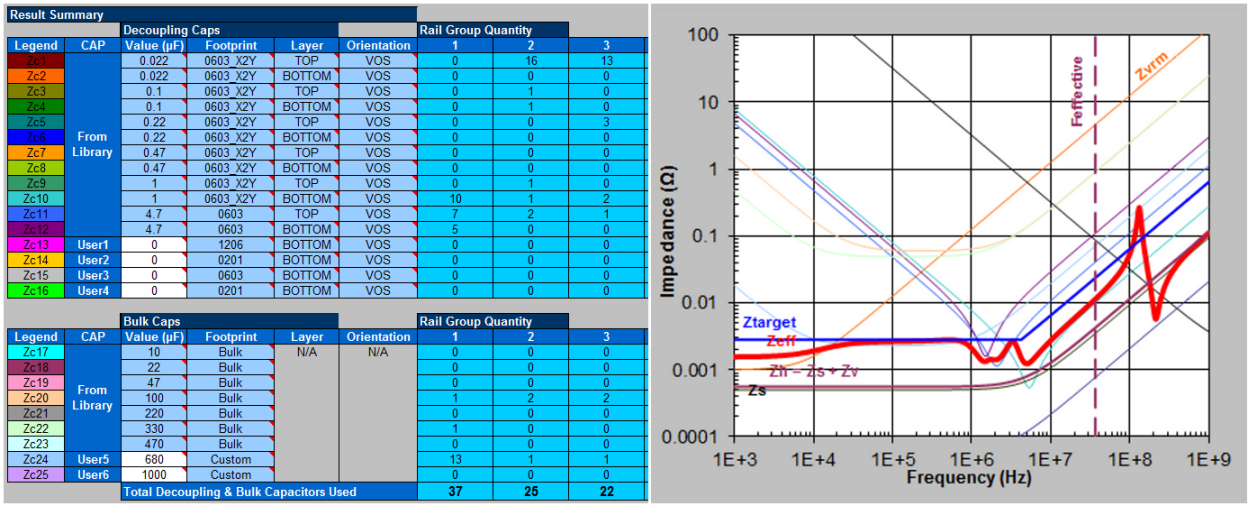
The **Current Ramp Up Period** parameter allows you to specify the number of clock cycles consumed by the pipeline. You can select a **High**, **Medium**, **Low**, or **Custom** setting. Altera recommends using a smaller value unless you have already entered a complete design in Quartus and determined the precise value.

Using the **Core Clock Frequency** and **Current Ramp Up Period** parameters has the effect of de-rating the target impedance at higher frequencies so that it ramps-up and is easier to meet.

In this example, entering a **Medium** 300MHz **Core Clock Frequency** and a **Low** 25 clock cycle **Current Ramp Up Period** , the number of decoupling capacitors required to meet the VCC supply is reduced from 301 to 37.

The Figures below show the capacitors required and impedance plot for the VCC supply.

Figure 27: VCC Supply Capacitors and PDN Performance When Using the Core Clock Frequency and Current Ramp Up Period Parameters



Result Summary

Decoupling Caps

Legend	CAP	Value (µF)	Footprint	Layer	Orientation	Rail Group Quantity 1	2	3
Zc1	From Library	0.022	0603_X2Y	TOP	VOS	0	16	13
Zc2		0.022	0603_X2Y	BOTTOM	VOS	0	0	0
Zc3		0.1	0603_X2Y	TOP	VOS	0	1	0
Zc4		0.1	0603_X2Y	BOTTOM	VOS	0	1	0
Zc5		0.22	0603_X2Y	TOP	VOS	0	0	3
Zc6		0.22	0603_X2Y	BOTTOM	VOS	0	0	0
Zc7		0.47	0603_X2Y	TOP	VOS	0	0	0
Zc8		0.47	0603_X2Y	BOTTOM	VOS	0	0	0
Zc9		1	0603_X2Y	TOP	VOS	0	1	0
Zc10		1	0603_X2Y	BOTTOM	VOS	10	1	2
Zc11		4.7	0603	TOP	VOS	7	2	1
Zc12		4.7	0603	BOTTOM	VOS	5	0	0
Zc13	User1	0	1206	BOTTOM	VOS	0	0	0
Zc14	User2	0	0201	BOTTOM	VOS	0	0	0
Zc15	User3	0	0603	BOTTOM	VOS	0	0	0
Zc16	User4	0	0201	BOTTOM	VOS	0	0	0

Bulk Caps

Legend	CAP	Value (µF)	Footprint	Layer	Orientation	Rail Group Quantity 1	2	3
Zc17	From Library	10	Bulk	N/A	N/A	0	0	0
Zc18		22	Bulk			0	0	0
Zc19		47	Bulk			0	0	0
Zc20		100	Bulk			1	2	2
Zc21		220	Bulk			0	0	0
Zc22		330	Bulk			1	0	0
Zc23		470	Bulk			0	0	0
Zc24	User5	680	Custom			13	1	1
Zc25	User6	1000	Custom			0	0	0
Total Decoupling & Bulk Capacitors Used						37	25	22

Reducing the number of VCC supply capacitors from 301 to 37 is a big improvement. The **Core Clock Frequency** and **Current Ramp Up Period** parameters can be applied earlier in the flow of this application note but it is generally beneficial to optimize the efficiency of the PDN before applying such de-rating effects.

The VCC, VCCT_GXB, and VCCR_GXB supplies are now decoupled with an effective and acceptable decoupling solution for this PCB with the estimated current requirements.

Related Information

References on page 29

Overall Design Study Capacitor Savings

This design study demonstrated the following improvements in PDN performance and the reduction in the number of PCB mounted decoupling capacitors.

Table 3: Study Results showing PDN performance Improvements and reduction in PCB mounted decoupling capacitors

PDN Design Stage	VCC Feffective (MHz)	VCC Caps Required	VCCR_GXB Caps	VCCT_GXB Caps
Original stackup, all supplies on L18, # PWR/GND vias = 50	10.62	>301	>301	>301

PDN Design Stage	VCC Feffective (MHz)	VCC Caps Required	VCCR_GXB Caps	VCCT_GXB Caps
Corrected # PWR/GND vias and layer number Reduced spreading inductance for VCC Increased spreading inductance for VCCR_GXB & VCCT_GXB Reduced vertical inductance for VCC, VCCR_GXB, VCCT_GX	30.68	>301	>301	>301
Reduce vertical inductance by moving supplies to more optimal layers closer to the FPGA	35.61	>301	>301	>301
Increase high-frequency capacitance by moving planes closer together	36.71	>301	>301	239
Reduce vertical inductance by placing decoupling capacitors on top surface	36.71	>301	255	180
Reduce capacitor mounting inductance by using low ESL X2Y caps	36.71	>301	28	22
Improve low-frequency performance by using low ESR bulk caps	36.71	>301	23	17
De-rate VCC high-frequency requirement by using the Core Clock Frequency and Current Ramp Up Period parameters	36.71	37	23	17

The diagrams below compare the original (left) and final (right) PDN Tool number of required capacitors for the VCC, VCCT_GXB, and VCCR_GXB supplies.

Figure 28: Comparison of VCC, VCCT_GXB, and VCCR_GXB Supply Required Capacitors Between the Original (Left) and Final (Right) PDN Designs

Result Summary

		Decoupling Caps				Rail Group Quantity		
Legend	CAP	Value (µF)	Footprint	Layer	Orientation	1	2	3
Zc1	From Library	0.001	0201	BOTTOM	VOS	0	0	0
Zc2		0.0022	0201	BOTTOM	VOS	0	0	0
Zc3		0.0047	0201	BOTTOM	VOS	0	161	181
Zc4		0.01	0402	BOTTOM	VOS	0	87	71
Zc5		0.022	0402	BOTTOM	VOS	0	24	22
Zc6		0.047	0402	BOTTOM	VOS	0	10	10
Zc7		0.1	0402	BOTTOM	VOS	0	6	5
Zc8		0.22	0402	BOTTOM	VOS	217	4	4
Zc9		0.47	0402	BOTTOM	VOS	34	2	2
Zc10		1	0603	BOTTOM	VOS	14	1	1
Zc11		2.2	0603	BOTTOM	VOS	3	1	0
Zc12		4.7	0603	BOTTOM	VOS	6	1	1
Zc13	User1	0	1206	BOTTOM	VOS	0	0	0
Zc14	User2	0	0201	BOTTOM	VOS	0	0	0
Zc15	User3	0	0603	BOTTOM	VOS	0	0	0
Zc16	User4	0	0201	BOTTOM	VOS	0	0	0

		Bulk Caps				Rail Group Quantity		
Legend	CAP	Value (µF)	Footprint	Layer	Orientation	1	2	3
Zc17	From Library	10	Bulk	N/A	N/A	0	0	0
Zc18		22	Bulk			0	0	0
Zc19		47	Bulk			0	0	0
Zc20		100	Bulk			0	0	0
Zc21		220	Bulk			0	0	0
Zc22		330	Bulk			2	3	4
Zc23		470	Bulk			25	1	0
Zc24	User5	0	Custom			0	0	0
Zc25	User6	0	Custom			0	0	0
		Total Decoupling & Bulk Capacitors Used				301	301	301

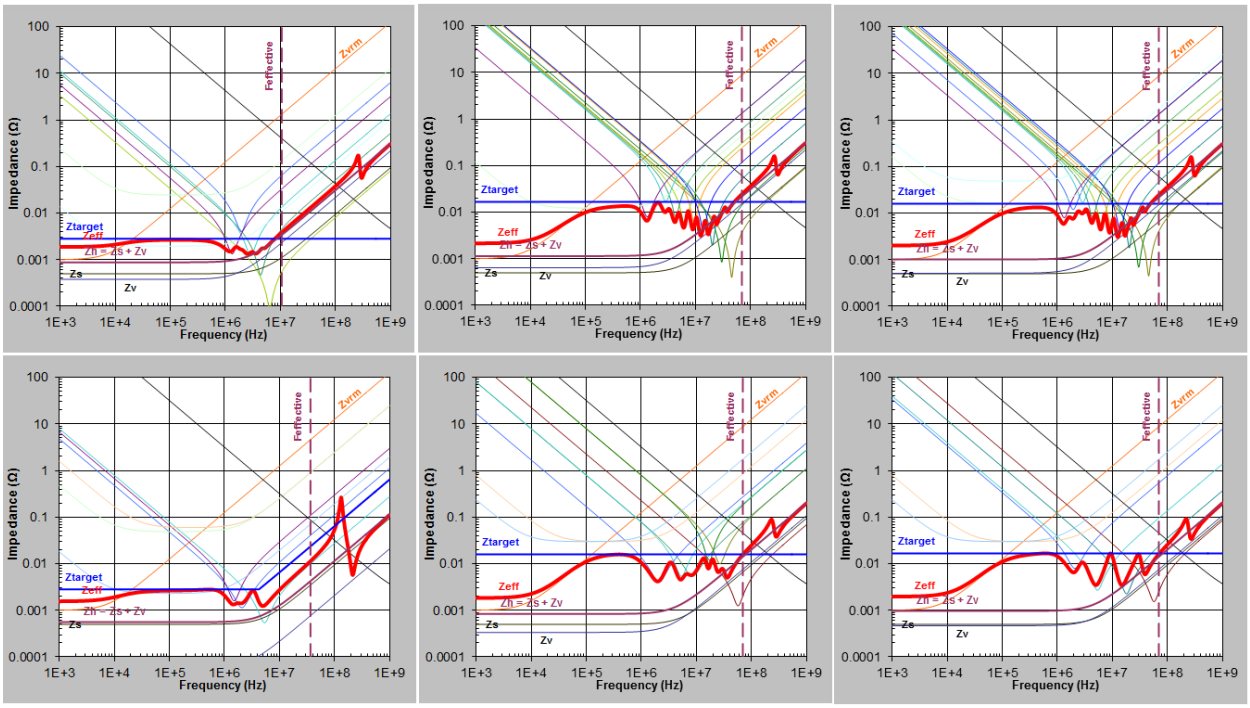
Result Summary

		Decoupling Caps				Rail Group Quantity		
Legend	CAP	Value (µF)	Footprint	Layer	Orientation	1	2	3
Zc1	From Library	0.022	0603_X2Y	TOP	VOS	0	16	13
Zc2		0.022	0603_X2Y	BOTTOM	VOS	0	0	0
Zc3		0.1	0603_X2Y	TOP	VOS	0	1	0
Zc4		0.1	0603_X2Y	BOTTOM	VOS	0	1	0
Zc6		0.22	0603_X2Y	TOP	VOS	0	0	3
Zc3		0.22	0603_X2Y	BOTTOM	VOS	0	0	0
Zc7		0.47	0603_X2Y	TOP	VOS	0	0	0
Zc8		0.47	0603_X2Y	BOTTOM	VOS	0	0	0
Zc9		1	0603_X2Y	TOP	VOS	0	1	0
Zc10		1	0603_X2Y	BOTTOM	VOS	10	1	2
Zc11		4.7	0603	TOP	VOS	7	2	1
Zc12		4.7	0603	BOTTOM	VOS	5	0	0
Zc13	User1	0	1206	BOTTOM	VOS	0	0	0
Zc14	User2	0	0201	BOTTOM	VOS	0	0	0
Zc15	User3	0	0603	BOTTOM	VOS	0	0	0
Zc16	User4	0	0201	BOTTOM	VOS	0	0	0

		Bulk Caps				Rail Group Quantity		
Legend	CAP	Value (µF)	Footprint	Layer	Orientation	1	2	3
Zc17	From Library	10	Bulk	N/A	N/A	0	0	0
Zc18		22	Bulk			0	0	0
Zc19		47	Bulk			0	0	0
Zc20		100	Bulk			1	2	2
Zc21		220	Bulk			0	0	0
Zc22		330	Bulk			1	0	0
Zc23		470	Bulk			0	0	0
Zc24	User5	680	Custom			13	1	1
Zc25	User6	1000	Custom			0	0	0
		Total Decoupling & Bulk Capacitors Used				37	25	22

The diagrams below compare the performance of the original (top row) and final (bottom row) PDN performance of the VCC, VCCT_GXB, and VCCR_GXB supplies.

Figure 29: VCC, VCCT_GXB, VCCR_GXB Supply Performance Comparison Between Original (Top Row), and Final (Bottom Row)



Overall Summary

It is important to analyze the performance of your PDN design given your specific PCB configuration and FPGA current requirements.

Reductions in the decoupling complexity can be made by using accurate power estimates for your design. Decoupling complexity is dependent on the magnitude of dynamic current, and the dynamic current is a percentage of the IMax. Therefore over estimating the IMax for your design can result in an excessive number of decoupling capacitors.

Decoupling capacitor savings can be made by not over-estimating the FPGA current requirements, or with accurate use of the **x** or **x/related** settings in the PDN Tool.

The key to optimizing your PDN design at high-frequencies is to reduce parasitic inductance wherever possible. Increasing power and ground plane pair capacitance also improves high-frequency performance. Reducing effective series resistance can help the PDN performance at low-frequencies. This can be done in the following ways:

- Reduce the spreading inductance from the power and ground plane pair to the FPGA by increasing the number of power and ground vias connecting the planes to the FPGA.
- Reduce the vertical loop inductance from the power and ground plane pair to the FPGA by moving them closer to the surface of the PCB that the FPGA is mounted to.
- Reduce the vertical loop inductance from the decoupling capacitors to the power and ground plane pair by placing them on the surface of the PCB that is closest to the planes.
- Use VOS with lower mounting inductance (Lmnt) instead of VOE capacitor mounting.
- Increase inter-plane capacitance of your power and ground plane pair by reducing their dielectric thickness and increasing their surface area.
- Use ultra-low (Effective Series Resistance) ESR bulk capacitors to help at low frequencies,
- Consider using larger vias with lower ESL to reduce via loop inductance.
- Use larger diameter through hole vias for all power connections to reduce via inductance. Micro-vias should not be used for PDN design.
- Use ultra-low ESL mounting capacitors such as X2Y package styles instead of standard 0603, 0402 or 0201 packages.

By using the **Core Clock Frequency** and **Current Ramp Up Period** parameters, it is possible to de-rate the VCC supply at high frequencies and make the VCC supply PDN design easier.

Using the Altera PDN Tool it is possible to assess the effect of each improvement on the PDN design. Each improvement in the PDN performance improves reliability and saves cost through reduced numbers of PCB mounted decoupling capacitors.

References

Guang Chen and Dan Oh, "Improving the Target Impedance Method for PCB Decoupling of Core Power," in *Electronic Components and Technology Conference (ECTC), 2014 IEEE 64th*.

Related Information

Improving the Target Impedance Method for PCB Decoupling of Core Power

Document Revision History

Table 4: Document Revision History

Chapter	Document Version	Changes Made
Example Design	2015.07.08	Updated the "Power Group Configuration and Current Entry for the Example Design" figure.
PDN Design Optimization Study	2015.07.08	Added a comment about "Feffective increasing with efficiency".

Date	Document Version	Changes Made
July 2015	2015.07.02	Initial release.