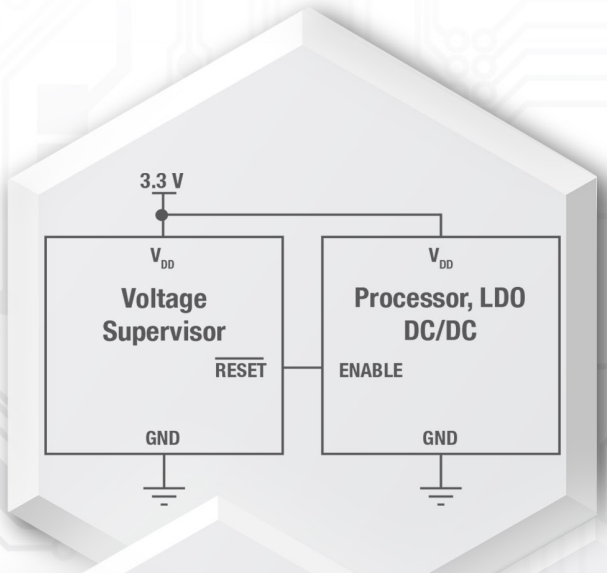


Voltage Supervisor and Reset ICs:

Tips, Tricks and Basics

Texas Instruments

Table of Contents

Preface: Message From the Editors

We depend on the reliable and safe operation of countless electronics all around us – in our homes, cars, workplaces, and factories. To ensure that these systems operate correctly in the diverse and sometimes harsh environments found in industrial and automotive applications, system designers must incorporate accurate and redundant monitoring of the critical power supplies that power the systems' processing and signal-chain blocks.

A voltage supervisor (also known as a reset integrated circuit [IC]) is a type of voltage monitor that monitors a system's power supply. Voltage supervisors are often used with processors, voltage regulators and sequencers – in general, where voltage or current sensing is required. Supervisors monitor voltage rails to ensure power on, detect faults and communicate with embedded processors to ensure system health. Safety integrity levels (SILs) and automotive SILs (ASILs) in industrial and automotive applications require highly accurate voltage monitoring. The Texas Instruments (TI) supervisors portfolio includes low-power, small-size, high-accuracy, watchdog timer, wide input voltage, multichannel and push-button reset ICs to help engineers meet design requirements.

This e-book provides an in-depth overview of voltage supervisors and their applications. The first chapter is an overview of voltage supervisors, explains why they are necessary, and showcases the various features they may include. The second chapter explains the electrical and timing specifications in a typical voltage supervisor data sheet. The third and fourth chapters provide in-depth details on watchdog timers, a feature included in some voltage supervisors that asserts a reset output if the timer does not receive a periodic pulse signal from the monitored processor within a specific time interval. The fifth chapter includes some applications that you can use to enhance your voltage supervisors.

We have compiled these resources from experts across TI to help you learn and enjoy working with supervisors. Through our experience with designers and colleagues throughout the years, we hope to resolve many of the issues you may encounter. We hope you will use this guide for years to come as a key resource for questions about voltage supervisors.

Cory Tran and Abhinav Sharma

1.1. What is a voltage supervisor?

Cory Tran

A voltage supervisor is a device that monitors or "supervises" a voltage rail within a system. Voltage supervisors can either detect for undervoltage events (when a voltage falls below a certain threshold) or overvoltage events (when a voltage rises above a certain threshold). Depending on the device, when a monitored voltage rail falls below or rises above a predetermined threshold voltage, the voltage supervisor will assert a signal to enable, disable or reset another device. Some voltage supervisors can monitor both undervoltage and overvoltage conditions, known as window detectors.

The purpose of a voltage supervisor is to ensure proper system power on, prevent processor brownout conditions, and monitor whenever a voltage rail – out of specification – could lead to performance issues or system failure. Supervisors have a range of different applications, from basic rail monitoring to automotive-grade power-supply monitoring. Voltage supervisors can also help provide extra diagnostic coverage and redundant safety monitoring in systems that require functional safety such as safety integrity level (SIL) or automotive SIL (ASIL) ratings. The device uses an internal comparator and reference voltage to compress a power-management supervisory circuit's function and contain it in a simple integrated circuit (IC).

Voltage supervisors are also known as reset ICs, voltage monitors or voltage detectors.

To learn more about the fundamentals of supervisors, see the TI training series called Voltage Supervisors 101.

1.2. Why monitoring voltages matters

Aaron Paxton

Monitoring voltage rails is about as enthralling as doing yard work. And while most people don't particularly enjoy pulling weeds or hedge trimming, it's necessary to keep things from getting out of hand, or having a significant other yell at you.

Fortunately, there are a myriad of ways to monitor your 1.8-V rails. Unfortunately, it's not always clear which method is best. Let's look at why voltage monitoring is important.

Avoiding brownout

In the digital realm, brownout can cause processors to latch up and malfunction. For example, the minimum supply voltage in the MSP430™ microcontroller (MCU) line is 1.8 V. Dropping the supply voltage below that threshold, even for a transient period, can mean trouble. Fortunately, many MSP430 MCUs incorporate their own reset integrated circuit (IC) to protect against this situation. If brownout occurs, the reset IC puts the processor into reset until the supply voltage rises to a tolerable level. If the voltage monitor is not already integrated into the MCU or if redundancy is required, it's up to you to implement it discretely, as shown in **Figure 1-1**.

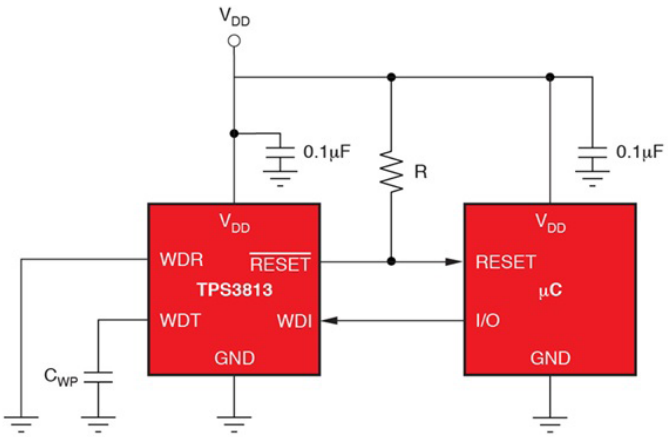


Figure 1-1. Voltage supervisory and window watchdog monitoring with the TPS3813K33 .

Sensing overvoltage events

An IC's absolute voltage rating is critical. Take the TPS61230 – the input-voltage range is rated to 5.5 V during normal operation. The absolute maximum voltage applied at the input is 6 V. Exceeding the absolute maximum voltage may cause reliability issues and/or permanent damage to the IC. Although the TPS61230 may be operating off a nominal 5-V rail, inaccuracies or transient voltages may not be factored in. A 5-V rail rated at 5% accuracy can easily be a 5.25-V rail. With enough

inductance on the line, loading the circuit can cause the voltage to spike, leading to a supply voltage above 6 V. Preventive measures such as eFuses and hot-swap controllers will help protect against these events. A reset IC may also be able to accomplish the same thing in some cases, as shown in **Figure 1-2**.

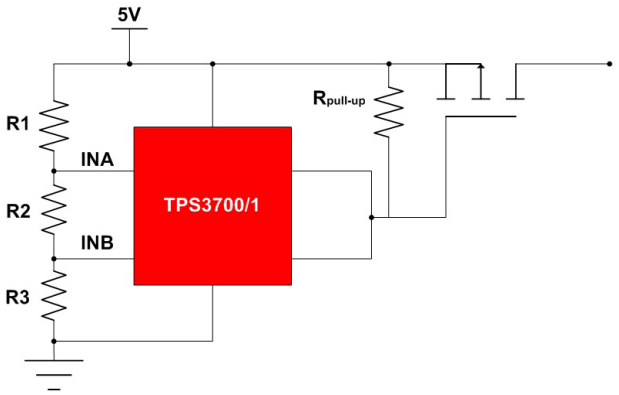


Figure 1-2. Using a window comparator such as the TPS3700 or TPS3701 to sense a 5-V line for overvoltage events.

Battery-level monitoring

Making sure that lithium-ion (Li-ion) and other battery technologies do not stray from their safe operating areas is imperative. This includes preventing undercharge and overcharge states. While this is usually accomplished with battery management systems, voltage monitors can also protect the battery (or batteries) from such events. **Figure 1-3** shows an implementation of a dual voltage monitor to detect a drooping battery voltage.

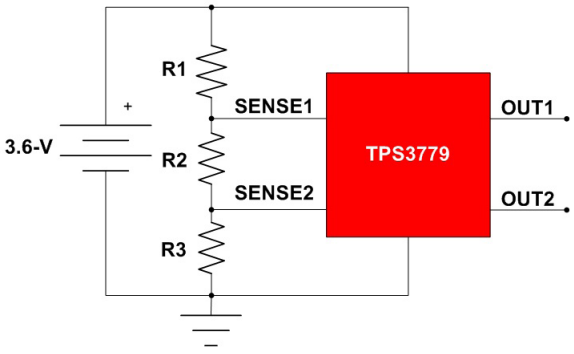


Figure 1-3. Monitoring a 3.6-V Li-ion battery with the TPS3779.

Diagnostics

Aside from protection, a system may need to monitor its rails as part of an overall diagnostics strategy. An example is when a system is attempting to qualify for safety integrity level recognition under the International Electrotechnical Commission (IEC) 61508 standard. Voltage monitors are a means of ensuring that your voltage rails are operating correctly.

1.3. Oh yes! My FPGA application is safe

Amit Benjamin

We all know that new technologies in our life pose great opportunities and possibilities but also new challenges. For example, smartphones and tablets give us 24/7 access to the world around us, but also create such dependency that it might be impossible to put them down.

In the same way, advances in chip-level technology help create endless opportunities but also challenges. With new, smaller process nodes and lower-core voltage rails, we are seeing the benefits of greater integration and higher efficiency. At the same time, these advances have also created challenges with variations in silicon performance due to corner spread and process variations. To combat these silicon process variations, vendors are specifying power-supply rails with tighter tolerances (see **Table 1-1**).

Power rail	Normal voltage (V)	Tolerance	Description
VCCINT	1.0	±3%	Voltage supply for the internal core logic
VCCAUX	1.8	±5%	Voltage supply for auxiliary logic

Table 1-1. Xilinx Virtex-7 power-supply requirements.

From a voltage monitoring/supervision perspective, lower supply rails with tighter tolerances pose challenges for system designers, requiring them to protect the data and move the system to a safe mode when field-programmable gate arrays (FPGAs), application-specific integrated circuits (ASICs) or memory banks are exposed to high voltage spikes.

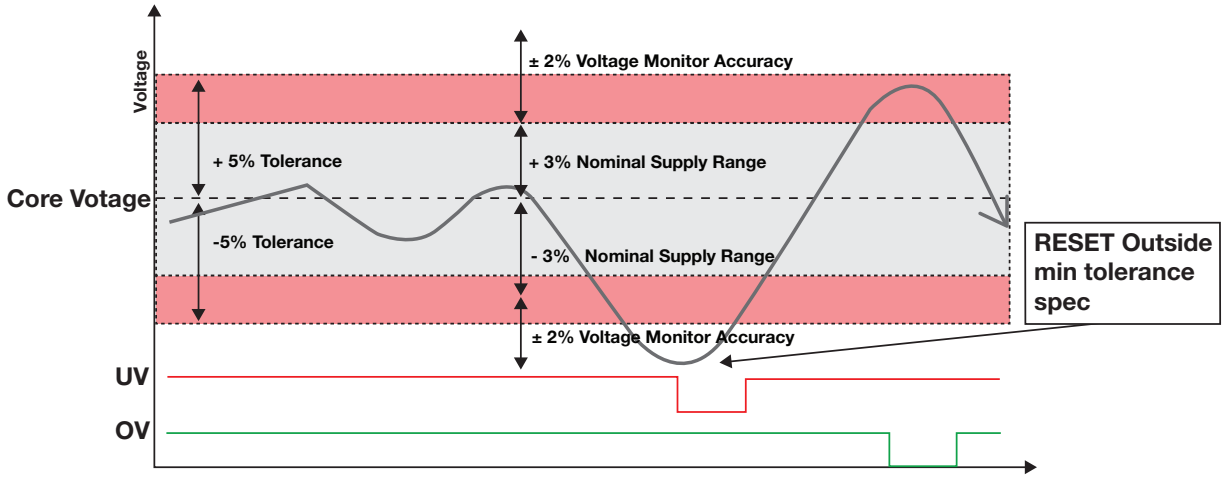


Figure 1-4. A reset occurs outside the safe core-voltage tolerance.

A typical voltage-monitor IC will have wide voltage threshold accuracy, varying hysteresis, poor glitch immunity and no overvoltage detection. These inaccuracies will cause a reset to occur outside the narrow tolerance band (**Figure 1-4**); trigger false resets within the nominal supply range; and create susceptibility to overvoltage and undervoltage transients, which might put the system at risk.

Additionally, more and more safety standards in industrial and automotive applications, such as International Organization for Standardization 26262 and 61508, require highly accurate voltage monitoring with integrated overvoltage detection.

To address these multiple challenges, TI has developed the TPS3702, an over- and undervoltage window comparator with fixed threshold voltages in a small outline transistor (SOT)-23-6 package. A common use case of the TPS3702 is highlighted in **Figure 1-5**, where it can be used to monitor the 1V, 1.2V, and 1.8V rails of the FPGA.

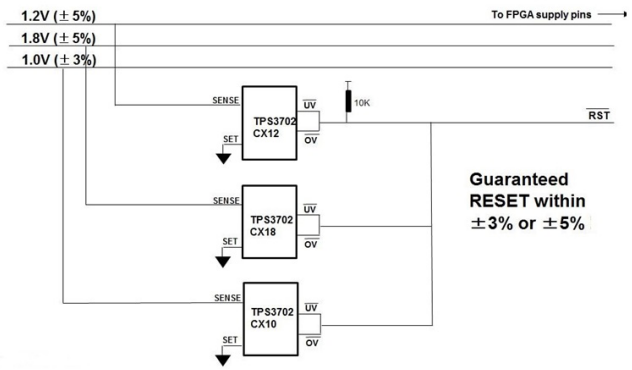


Figure 1-5. A possible application with the TPS3702.

This high accuracy window comparator provides benefits including:

- FPGA/ASIC tight tolerances – the TPS3702 has a 0.9% maximum threshold voltage accuracy over temperature. This is accomplished by trimming the internal resistor dividers at the factory level. Other voltage monitors require external resistor dividers that contribute to threshold voltage inaccuracies. The TPS3702 is a good fit for systems that operate on low-voltage supply rails and have tight supply tolerances. Its very high accuracy guarantees a safe reset before the FPGA minimum/maximum supply tolerances are overruled.
- False reset within the nominal voltage window – low threshold hysteresis options of 0.55% or 1.0% prevent nuisance interrupts while making sure that the reset will be released only when VCC is back to the safe window.
- Immunity to overshoot and undershoot spikes – internal glitch immunity filters further eliminate false resets resulting from erroneous signals.
- Safety integrity level (SIL) and automotive SIL (ASIL) risk classes require accurate overvoltage and undervoltage – the TPS3702 enables you to choose window-wide threshold options around a selected voltage option (±3%, ±5%, ±7%, ±10%) according to your application requirements and safety standard needs.

1.4. Selecting voltage detectors, supervisors and reset ICs for system safety

Michael DeSando

Power-supply voltages in telecom, industrial and avionics applications can vary for many reasons, such as line and load transients, power outages, or a low battery. Voltage detectors and supervisors/reset integrated circuits (ICs) provide an early indication of supply-voltage deviations related to these issues to help protect the system.

Although voltage detectors and supervisors/reset ICs have the same functionality, they are used in different types of systems. A voltage detector monitors a voltage (like a battery voltage) and indicates to users that the voltage is low. Voltage detectors usually don't have a delay, but they do have built-in hysteresis to prevent false triggers if the voltage is hovering around the threshold voltage.

A supervisor/reset IC monitors a supply voltage and resets or turns off another device like a microprocessor if the supply voltage is low. These devices usually have a programmable output delay to prevent the system from returning from reset before the supply voltage is stable.

Voltage detectors and supervisors/reset ICs have different features and parameters, making it tough to choose the right one for a given application. The key to choosing a voltage supervisor is to know the features you need and then select one based on your desired size, package type and price.

The simplest way to monitor voltage

For some applications, you may only want a basic, small and easy-to-implement voltage detector or supervisor/reset IC. These devices provide a low output voltage or reset signal when the supply voltage drops below the factory-programmed reset threshold. The output signal remains active for a fixed time after the supply voltage rises above that threshold. The available threshold options vary by part. Typical values include 2.63 V, 2.93 V, 3.0 V, 3.08 V, 4.38 V and 4.63 V. Accuracy also varies; while usually around 3%, it can be as precise as 0.75% over temperature for some devices.

Basic voltage detectors or reset ICs don't require any external components (except for maybe a pull-up resistor at the output) and are available in small, three-pin packages. **Figure 1-6** shows an example of a simple voltage supervisor, the TI TLV803E.

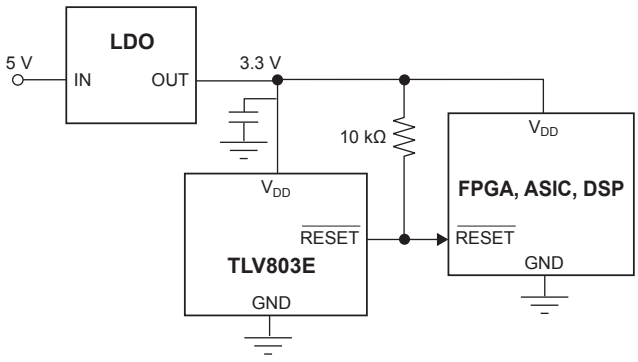


Figure 1-6. TLV803E typical application circuit.

When the supply voltage at VCC drops below the TLV803E's reset threshold, the reset pin drops low and triggers the microprocessor to reset.

Output type: active low vs. active high, push-pull vs. open drain

Active low and active high refer to a reset type. Active-low reset starts high; when the supply voltage drops below the voltage reset threshold, the reset pin goes low. Active-high reset is the exact opposite. The reset starts low, and when the supply voltage drops below the voltage reset threshold, the reset pin goes high. See the application curve in **Figure 1-7**.

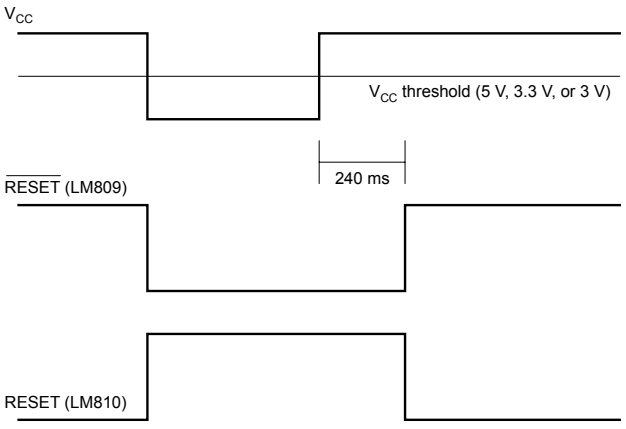
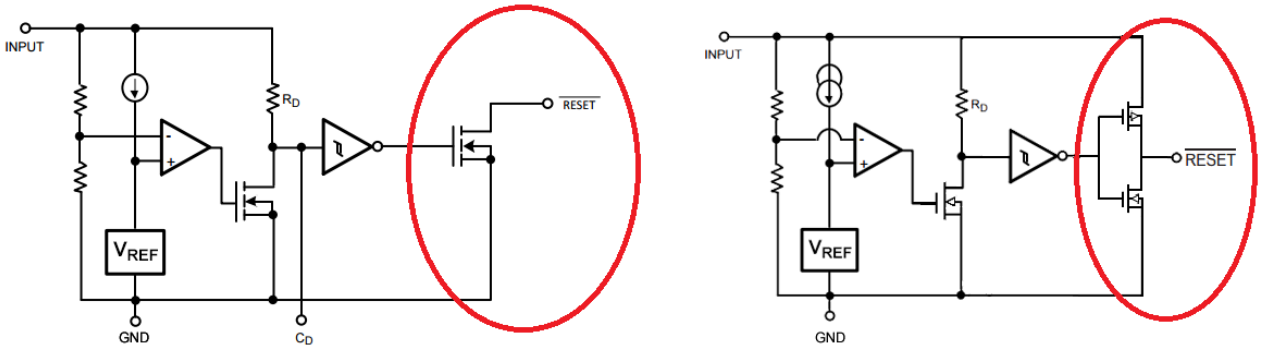


Figure 1-7. Active low (LM809) vs. active high (LM810).



Open-Drain **Push-Pull**

Figure 1-8. Output types.

Push-pull and open drain refer to an output type. Push-pull uses two transistors at the output, with the top transistor turning on to set the output high and the bottom transistor turning on to set the output low. Open drain uses one transistor to set the output low and a pull-up resistor instead of a top transistor to set the output high. The advantage of push-pull is speed and lower power consumption. Open-drain outputs, however, can be wired together to create an OR/AND logic output configuration. **Figure 1-8** illustrates both open-drain and push-pull outputs.

For more information regarding the different output topologies of a voltage supervisor read "Output topology options for a voltage supervisor".

Voltage supervisor features

As designs become more complex, more advanced devices may be required to successfully monitor a voltage. The next sections highlight various features found in voltage detectors and supervisors/reset ICs to help designers select the right one.

Programmable output delay

Voltage supervisors, unlike voltage detectors, usually have a programmable output delay using an external capacitor, making them extremely flexible. They are useful for the proper sequencing of multiple supplies, such as in field-programmable gate array applications or to prevent system glitches. When the supply voltage rises above the voltage threshold (plus the hysteresis, if applicable), this would normally trigger the device to "unflag" the reset signal and return the system from a reset condition. Since there is a delay created by the delay capacitor (C_D), however, the voltage must remain above the voltage threshold plus hysteresis for the specified time delay before the reset signal unflags. This prevents the system from returning from a reset condition prematurely.

Programmable output delay is sometimes referred to as a programmable reset timeout period. A ceramic chip capacitor connected directly to the delay pin (sometimes named CD, SRT or CT) is usually sufficient for a stable, well-defined output delay. As an example, the LM8365, shown in **Figure 1-9**, has a programmable output delay.

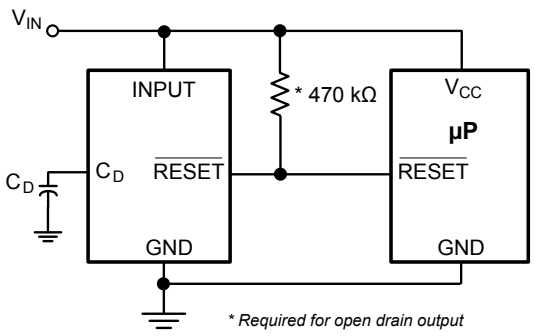


Figure 1-9. LM8365 typical application circuit with programmable output delay.

When the input voltage drops below the reset threshold, the reset pins drops low. When the input voltage rises above the threshold, there is a delay before the reset pin comes back up. By increasing CD, the delay increases. See the timing diagram for the LM8365 in **Figure 1-10**.

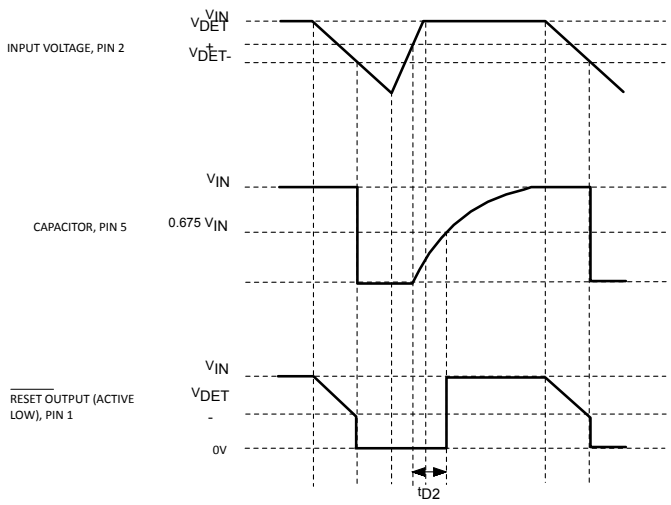


Figure 1-10. Timing diagram for the LM8365.

For more supervisor options with programmable output delay, view the low I_Q TPS3840 or small-package offerings of TPS3890.

Adjustable threshold voltage

Some voltage supervisors come with an adjustable threshold voltage option, where you have the flexibility to monitor any voltage above the device's specified voltage threshold. A good example of this feature is on the TPS3808. By using the TPS3808G01 in the circuit configuration, as shown in **Figure 1-11**, you can implement a resistor divider to adjust the threshold suiting your design needs. Since the threshold on the TPS3808G01 is 0.405 V, **Equation 1** calculates the monitored voltage as:

$$V_{IT,} = \left(1 + \frac{R_1}{R_2}\right) \times 0.405 \quad (1)$$

Adjustable threshold voltage supervisors are helpful in designs that require multiple different voltage monitoring options, in which you can select one supervisor to fit all of your design needs.

A good design rule of thumb when using an adjustable threshold voltage is to make sure that the current going through the resistor divider is at least 100 times higher compared to the current going into the sense pin (I_{SENSE}).

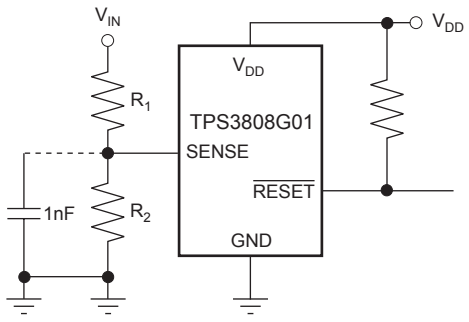


Figure 1-11. Using the TPS3808G01 to monitor a user-defined threshold voltage.

Manual reset

A manual reset input forces a reset when the MR pin is lower than the manual reset threshold (V_{MRT}) for a specific duration, usually on the order of microseconds. The reset pin remains active as long as the MR pin is held low. The pin releases once the reset timeout period expires after MR rises above the V_{MRT}. This feature is useful for microprocessor applications when the user needs to reset. It's also useful in applications that need to reset when detecting a low voltage other than the main supply voltage. Manual reset gives you full control over the reset rather than having only a low supply-voltage trigger.

Power-fail input

Some voltage detectors and supervisors/reset ICs have an additional input for a power-fail warning to monitor a power supply other than the main supply. This additional input can be useful in systems that want to detect if the power is failing before it actually fails. The threshold can vary with different devices, but a typical threshold value is 1.225 V from an internal reference. If the power-fail input (PFI) pin is lower than the power-fail voltage threshold (V_{PFT}), the power-fail output (PFO) drops low.

Typically, the power-fail comparator, driven by a voltage divider connected to the main supply, signals a falling power supply. A voltage at PFI that drops below V_{PFT} several milliseconds before the main supply voltage drops below the reset threshold provides advanced warning of a brownout. The PFI pin can also connect to the MR pin to force a low output signal for voltage detectors or a reset for supervisors/reset ICs.

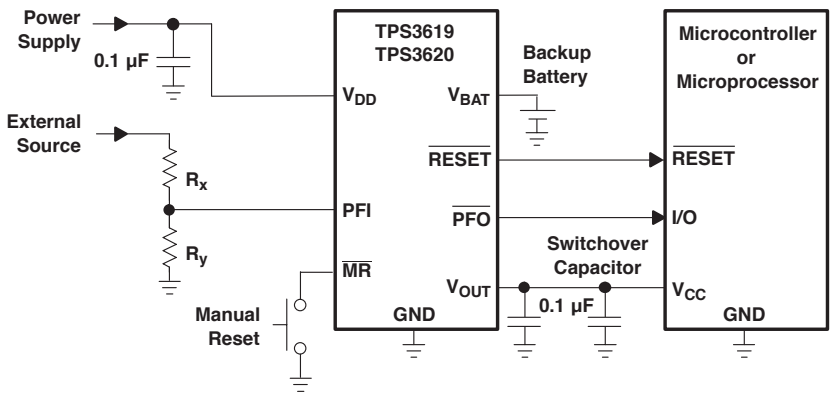


Figure 1-12. Typical operating circuit on the TPS3619.

An example of a device that offers that power-fail input feature is the TPS3619 battery backup supervisor, as shown in **Figure 1-12**. Not only does this device offer the additional voltage monitoring capability from the power-fail input pin, it can also help in systems that need a backup battery to kick in in case of a brownout or power failure on the main voltage supply. This can be extremely useful for data retention of complementary metal-oxide semiconductor random access memory and other applications.

Watchdog timer

Voltage detectors and supervisors/reset ICs with watchdog timers wait for signal activity on the watchdog input (WDI) pin. A reset triggers if the supervisor does not detect a signal within the watchdog window. You can program this window using an external capacitor, making the watchdog window more flexible.

A watchdog timer is usually used for safety-critical applications or for processor monitoring that requires a reset if the microprocessor is not active for a certain duration. This feature prevents the system from continuing to run if the microprocessor is not functioning properly.

An example of a supervisor with watchdog timer can be found on the TPS386000, a quad-channel voltage supervisor with watchdog timeout specifications. This voltage supervisor can be useful for applications that not only need the watchdog feature to monitor the MCU, but also need multiple rails of monitoring, as shown in **Figure 1-13**.

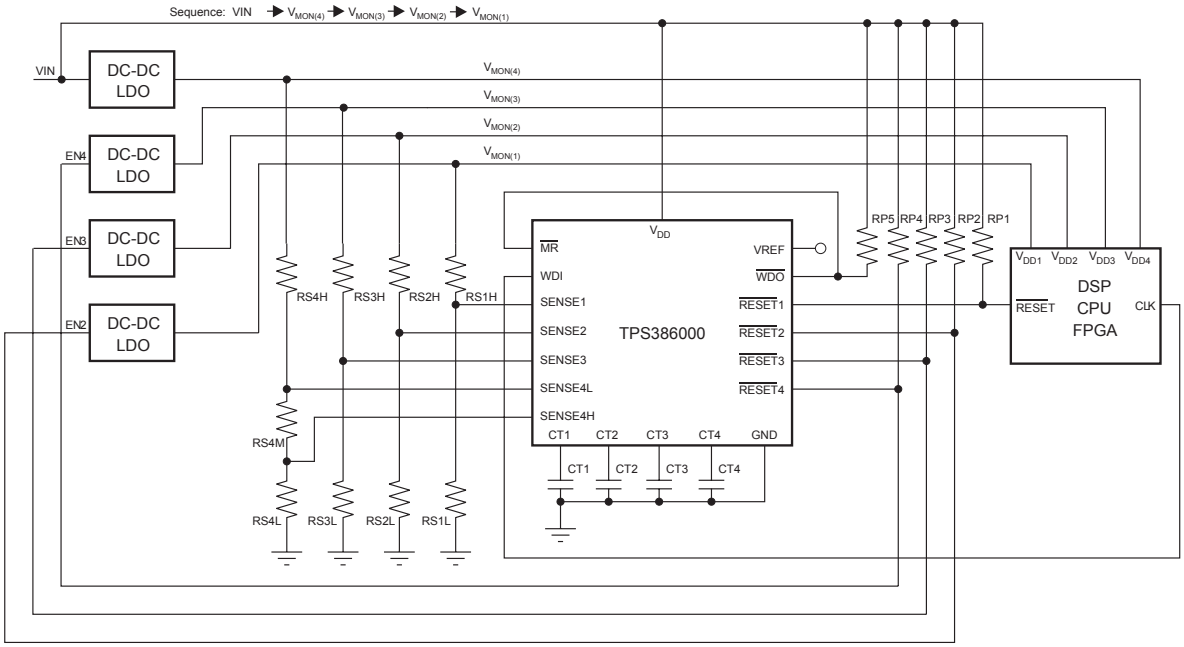
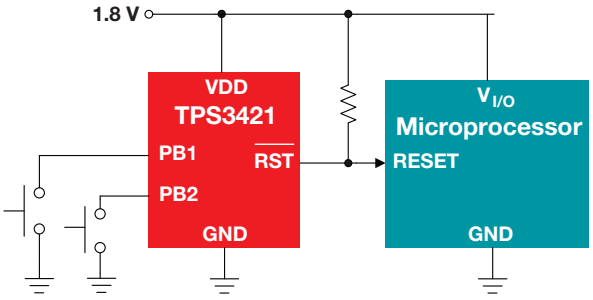


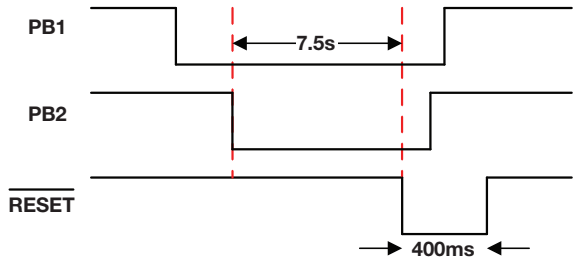
Figure 1-13. TPS386000 typical circuit application.

Push-button reset IC

Being able to reset a system by holding down a button or two is critical in applications where it is not easy to remove the battery. Multiple buttons are also useful when a processor is frozen and a user needs to force the application to reset. In such cases, a push-button reset IC can monitor these user presses and provide a reset after a given time period. Additionally, push-button reset ICs are a good fit in wireless speaker/headphone applications when there is a requirement for the device to perform a certain action when a user presses a button for specific duration. Devices like the TPS3421, as shown in **Figure 1-14**, can help in these situations.



(a)



(b)

Figure 1-14. TPS3421 typical circuit application (a); and timing diagram (b).

Low-line output

This early power-failure warning indicator goes low when the supply voltage drops to a value higher than the reset threshold. The indicator triggers about 2% above the reset threshold to indicate low power without causing a reset.

Figure 1-15 shows an example application circuit for the LM3710, while **Figure 1-16** shows an example timing diagram of the LM3710 with examples of the features reviewed so far.

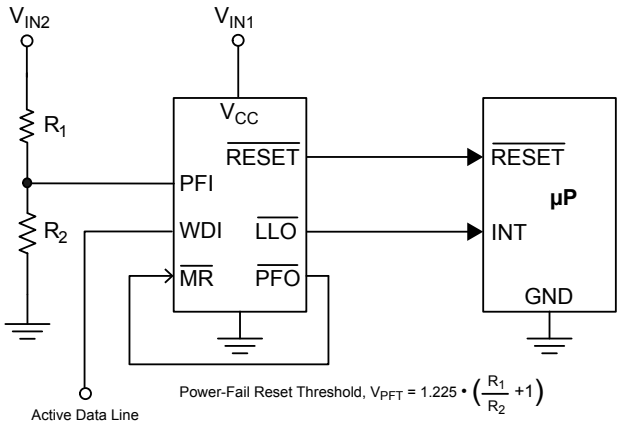


Figure 1-15. LM3710 application circuit.

In addition to the standard reset, the LM3710 has a manual reset, PFI, watchdog timer and low-line output, making it a very flexible device for many applications. The application circuit shown in **Figure 1-15** above uses R1 and R2 as a voltage divider connected to V_{IN2} to set the power-fail reset threshold in order to monitor a second power supply. If the second power supply drops below the power-fail reset threshold, the PFI pin will be low, so the PFO pin will also drop low. Since this pin is connected to the MR pin, a reset will trigger.

A reset will also occur if no activity is detected within the watchdog window on the WDI pin. The WDI pin can connect to the microprocessor to detect if it is still operating correctly by having the microprocessor send an intermittent pulse. The low-line output (LLO) pin will drop low if the supply voltage at V_{CC} drops to within about 2% of the reset voltage threshold. The LLO pin can connect to a microprocessor for detection. When this pin goes active, a signal sent to the microprocessor can cause some other action to occur, such as sending a signal to another device, or a flashing LED or other alert to the user.

The timing diagram in **Figure 1-16** shows an example of monitoring a second voltage input (V_{IN2}). When the V_{IN2} connected to the PFI pin goes low, the PFO pin drops low, causing the MR pin to drop low, which then triggers a reset. There are many ways to use the power-fail and manual reset features, so it is up to you to decide what you need for your application.

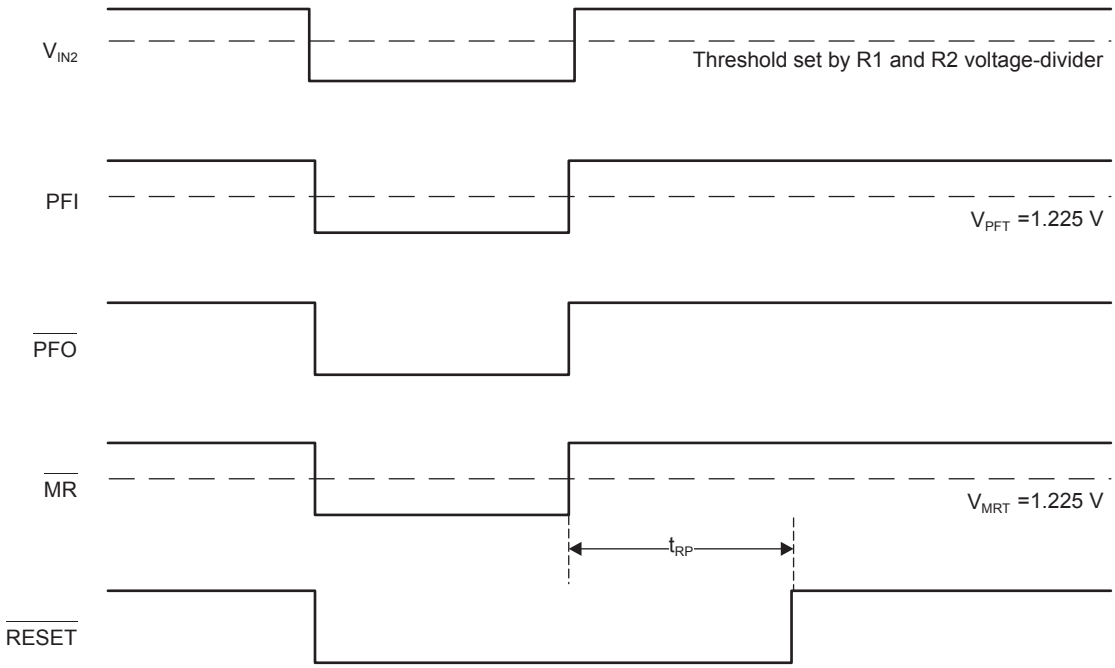


***Figure 1-16.** Example timing diagram for power-fail and manual reset.*

2.1. Electrical characteristics table

Table 2-1 is an electrical characteristics table for the TPS3840. This section will cover how to read and interpret such a table.

Parameter		Test Conditions	Min	Typ	Max	Unit
Common Parameters						
V_{DD}	Input supply voltage		1.5		10	V
V_{IT-}	Negative-going input threshold accuracy(1)	-40°C to 125°C	-1.5	1	1.5	%
V_{HYS}	Hysteresis on V_{IT-} pin	V_{IT-} = 1.6 V to 3.1 V	175	200	225	mV
V_{HYS}	Hysteresis on V_{IT-} pin	V_{IT-} = 3.2 V to 4.9 V	75	100	125	mV
I_{DD}	Supply current into VDD pin	VDD = 1.5 V < VDD < 10 V VDD > V_{IT+} (2) T_A = -40°C to 125°C		300	700	nA
$V_{\overline{MR}\_L}$	Manual reset logic low input(3)				600	mV
$V_{\overline{MR}\_H}$	Manual reset logic low input(3)		0.7 V_{DD}			V
$R_{\overline{MR}}$	Manual reset internal pull-up resistance			100		kΩ
R_{CT}	CT pin internal resistance		350	500	650	kΩ
TPS3840PL (Push-Pull Active-Low)						
V_{POR}	Power on Reset Voltage(4)	$V_{OL(max)}$ = 200 mV $I_{OUT(Sink)}$ = 200 nA			300	mV
V_{OL}	Low level output voltage	1.5 V < V_{DD} < 5 V V_{DD} < VIT- $I_{OUT(Sink)}$ = 2 mA			200	mV
V_{OH}	High level output voltage	1.5 V < V_{DD} < 5 V V_{DD} < V_{IT+} (2) $I_{OUT(Source)}$ = 2 mA	0.8 V_{DD}			V
		5 V < V_{DD} < 10 V V_{DD} < V_{IT+} (2) $I_{OUT(Source)}$ = 2 mA	0.8 V_{DD}			V
TPS3840PH (Push-Pull Active-High)						
V_{POR}	Power on Reset Voltage(4)	V_{OH}, $I_{OUT(Source)}$ = 500 nA			950	mV
V_{OL}	Low level output voltage	1.5 V < V_{DD} < 5 V V_{DD} < V_{IT+} (2) $I_{OUT(Sink)}$ = 2 mA			200	mV
					200	mV
V_{OH}	High level output voltage	1.5 V < V_{DD} < 5 V, V_{DD} < VIT-, $I_{OUT(Source)}$) = 2 mA	0.8 V_{DD}			V
TPS3840DL (Open-Drain)						
V_{POR}	Power on Reset Voltage(4)	$V_{OL(max)}$ = 0.2 V $I_{OUT (Sink)}$ = 5.6 uA			950	mV
V_{OL}	Low level output voltage	1.5 V < V_{DD} < 5 V V_{DD} < V_{IT-} $I_{OUT(Sink)}$ = 2 mA			200	mV
$I_{lkg(OD)}$	Open-Drain output leakage current	RESET pin in High Impedance, V_{DD} = V_{RESET} = 5.5 V V_{IT}+ < V_{DD}			90	nA

(1) V_{IT-} threshold voltage range from 1.6 V to 4.9 V in 100 mV steps, for released versions see Device Voltage Thresholds table.

(2) $V_{IT+} = V_{HYS+} V_{IT-}$

(3) If the logic signal driving $\overline{MR}$ is less than V_{DD}, then additional current flows into V_{DD} and out of $\overline{MR}$

(4) V_{POR} is the minimum V_{DD} voltage level for a controlled output state. V_{DD} slew rate ≤ 100mV/µs

Table 2-1. Electrical characteristics table for the TPS3840.

Common terms

V_{DD} – Input supply voltage. This is the supply voltage range needed to power the IC.

V_{IT-} – Negative input threshold voltage. V_{IT-} can be expressed as a voltage or as an accuracy percentage around the nominal threshold voltage. This is the voltage threshold at which the voltage supervisor detects an undervoltage condition. Notice how in **Figure 2-1** once the voltage drops under V_{IT-} , the reset is activated after the propagation delay or $TP_{\_HL}$.

V_{HYS} – Threshold voltage hysteresis. This is the difference between the rising (V_{IT+}) and falling (V_{IT-}) thresholds to prevent false triggers if the monitored voltage is oscillating around V_{IT-}. Once the monitored voltage rises above VIT+, the supervisor will clear the fault. Follow the timing diagram in **Figure 2-1** for a visual of this action.

I_{DD} – Supply current. This is the current going into the V_{DD} pin from the power supply. I_{DD} is sometimes referred to as quiescent current (I_Q).

$V_{\overline{MR}L}$ – Manual reset logic threshold voltage. This is the maximum input voltage considered logic low at the MR pin.

$V_{\overline{MR}H}$ – Manual reset logic threshold voltage. This is the minimum input voltage considered logic high at the MR pin.

V_{POR} – Power-on-reset voltage. V_{POR} is the minimum input voltage required for a controlled output state. The supervisor output is undefined when V_{DD} is below V_{POR}. To mitigate this glitch, read the section in Chapter 5, "Mitigating the Indeterminate Output of a Voltage Supervisor During Power Up/Down."

V_{OL} – Low-level output voltage. This is the maximum voltage at the supervisor output during a logic low condition.

V_{OH} – Low-level output voltage. This is the minimum voltage at the supervisor output during a logic high condition.

I_{LKG} – Open-drain output leakage current. This is the leakage current that occurs when the internal metal-oxide semiconductor field-effect transistor (MOSFET) turns off due to the pull-up resistor used in open-drain output topologies.

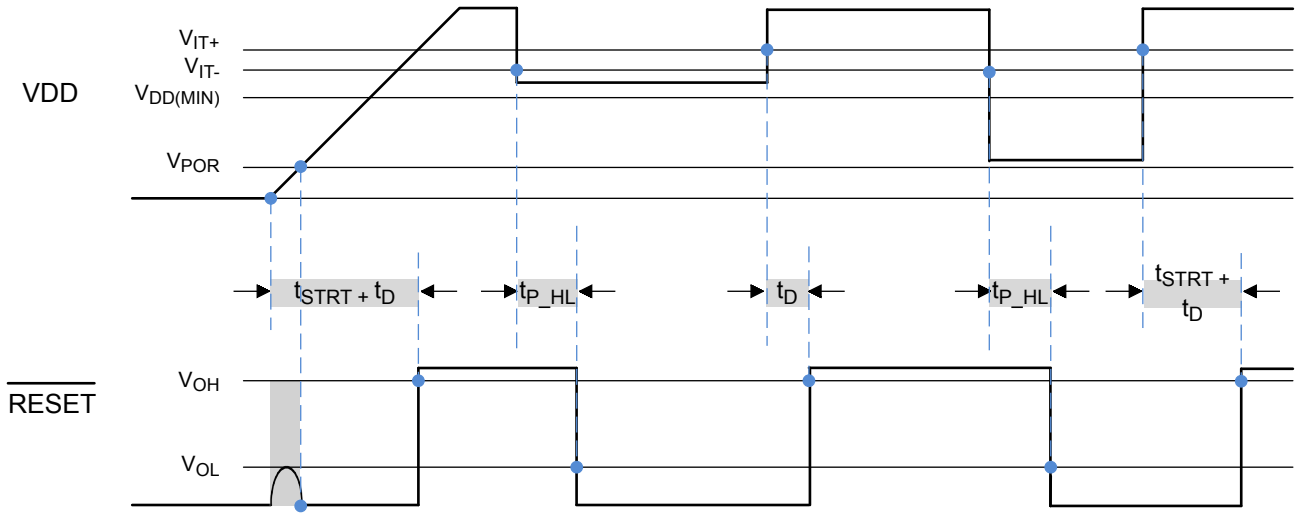


Figure 2-1. TPS3840 timing diagram.

Parameter		Test Conditions	Min	Typ	Max	Unit
T_{STRT}	Startup Delay(1)	CT pin open	100	220	350	µs
T_{P_HL}	Propagation detect delay for V_{DD} falling below V_{IT-}	$V_{DD} = V_{IT+}$ to (V_{IT-}) - 10%(2)		15	30	µs
T_D	Reset time delay	CT pin = open			50	µs
		CT pin = 10 nF		6.2		ms
		CT pin = 1 µF		619		ms
T_{GI_VIT-}	Glitch immunity V_{IT-}	5% V_{IT-} overdrive(3)		10		
T_{MR_PW}	MR pin pulse duration to initiate reset			300		ns
T_{MR_RES}	Propagation delay from $\overline{MR}$ low to reset	V_{DD} = 4.5 V, $\overline{MR} < V_{\overline{MR\_L}}$		700		ns
T_{MR_tD}	Delay from release $\overline{MR}$ to deasert reset	V_{DD} = 4.5 V, $\overline{MR} = V_{\overline{MR\_L}}$ to $V_{\overline{MR\_H}}$		T_D		ms

(1) When V_{DD} starts from less than the specified minimum V_{DD} and then exceeds VIT+, reset is release after the startup delay (t_{STRT}), a capacitor at CT pin will add T_D delay to t_{STRT} time
(2) tP_HL measured from threhold trip point (VIT-) to VOL for active low variants and VOH for active high variants.
(3) Overdrive % = [(V_{DD}/ VIT-) - 1] × 100%

Table 2-2. Timing requirements table for the TPS3840.

2.2. Timing requirements table

Table 2-2 is a timing requirements table for the TPS3840. This section will cover how to read and interpret such a table.

Common terms

T_{STRT} – Startup delay. V_{DD} must be above $V_{DD\ (min)}$ for T_{STRT} before the device is fully functional.

T_{P_HL} – Propagation delay. This is the amount of time it takes for the device to trigger a fault event. See the timing diagram in **Figure 2-1** for a visual of the propagation delay.

T_D – Reset time delay. This is the amount of time it takes for the device to release from a fault condition once there is no longer a fault. Check the reset time delay configuration for the device used, as some supervisors have programmable reset time delays. See the timing diagram in **Figure 2-1** in the Electrical Characteristics section for a visual representation of T_D.

T_{GI_VIT-} – Glitch immunity. This protects the supervisor from pulses or glitches on the monitored voltage rail. The supervisor will ignore any glitch less than T_{GI_VIT-}. The overdrive is defined by how much V_{DD} deviates from the specified threshold and refers to the difference between V_{IT-} and the pulse in percentage.

T_{MR_PW} – MR pulse width. This is the amount of time required for the supervisor to detect a pulse on the MR pin.

T_{MR_RES} – MR propagation delay. This is the amount of time it takes for the device to trigger a fault event caused by the MR pin.

T_{MR_tD} – MR time delay. This is the amount of time it takes for the device to release from the de-assertion of the MR pin.

3.1. What is a watchdog timer and why is it important?

Kelvin Odom

Much like a small, yappy dog that lives in a celebrity's purse, watchdog timers are often considered unnecessary or excessive. To equate the two, however, would do a great disservice to the watchdog. Unlike "purse dogs," watchdogs add critical monitoring features that allow you to internally and externally monitor your system for failure and take action should failure occur.

Just what is a watchdog timer?

Simply put, a watchdog timer is a device that asserts a reset output if it has not received a periodic pulse signal from a processor within a specific time frame. One way this is implemented is by a digital signal output (a general-purpose input/output) from the processor feeding into the watchdog input of an external watchdog timer, as shown in **Figure 3-1**. The TPS3851 is a supervisor with an integrated watchdog timer. This allows it to both supervise the supply rail to the microcontroller (MCU) and monitor the digital pulse emanating from the MCU externally.

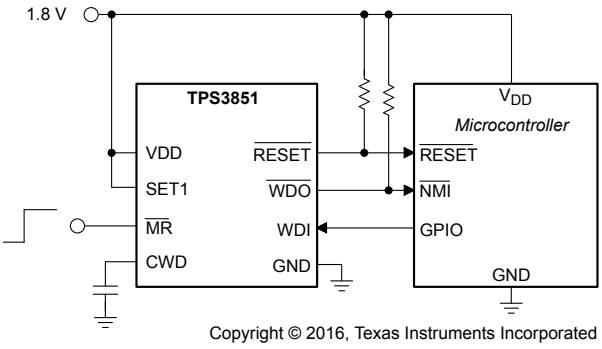


Figure 3-1. Watchdog monitoring provided by the TPS3851.

The processor periodically sends a pulse to the watchdog timer to indicate that the system software is operating properly. If the watchdog timer does not receive this pulse within an allotted time frame (known as the watchdog timeout), the watchdog timer asserts a reset output.

This reset output can notify the system that the processor has experienced a hang or a freeze, or reset the processor itself. **Figure 3-2** illustrates a pulse received within the watchdog timeout and a pulse received after the watchdog timeout has expired.

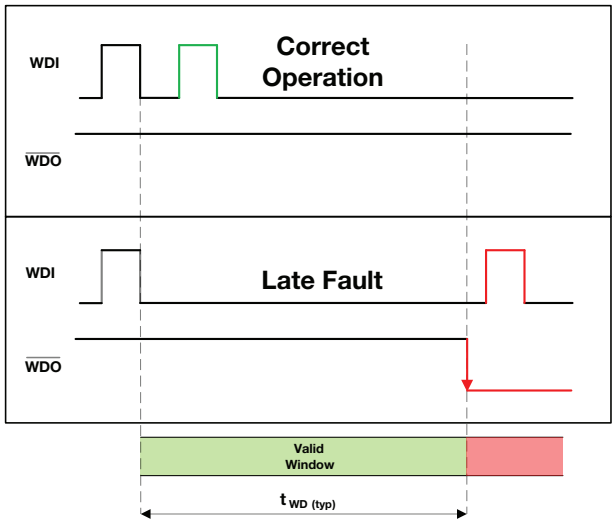


Figure 3-2. Operation of a standard watchdog timer.

Why are watchdog timers so important?

Watchdog timers provide a method for alerting a system or resetting a processor whose software has experienced a freeze or hang. While no one purposely designs software to freeze, good system designers plan for failures anyway – as it's always better to prepare for the unexpected. Without such monitoring, the processor could stay frozen indefinitely and lead to further system failure. An external watchdog timer with an adjustable timeout interval such as the TPS3851 can identify these software freezes within just a few milliseconds and reset the system or processor appropriately. This functionality is especially necessary in embedded or remote systems where manually resetting the system isn't practical or even possible. Safety-critical applications also require external watchdogs to add critical redundancy to systems where a processor may freeze or hang.

How can you implement a watchdog timer in your embedded system?

There are two primary methods for implementing watchdog timers:

- Using a processor with integrated watchdog functionality. Many microcontrollers such as the MSP430F5529 series have integrated watchdog functionality. This is valuable because it is very easy to implement and requires no other integrated circuits. However, it comes with one major caveat: integrated watchdogs may not always work as desired because the code issues that cause the MCU to malfunction could also inadvertently disable the watchdog timer. Again, software is written in such a way that an internal watchdog should be able to detect any freezes or hangs. However, taking the extra steps to monitor the watchdog input in a redundant manner can help account for unforeseen errors in code. TI offers stand-alone watchdog timers such as the TPS3431 to help in these situations.
- Using a voltage supervisor with a watchdog timer. A supervisor with watchdog-timer functionality such as the TPS3851 or TPS3110 enables you to monitor both the supply voltage and watchdog signal in an external, redundant fashion. Should the internal watchdog of the processor fail to detect an errant or missing pulse, the external watchdog timer will add a level of detection not otherwise achievable.

In principle, the functionality of a watchdog timer is not overly complicated. However, its importance in maintaining the reliability of systems cannot be overstated. This is especially true if a human-initiated system reset in case of failure is not possible or is very difficult.

3.2. The difference between a standard watchdog and a window watchdog

TI offers standard watchdog and window watchdog options. The difference between "standard" and "window" watchdogs is the lower boundary specification. In standard watchdogs, a pulse must arrive before the watchdog timeout; otherwise, a fault occurs. Looking at **Figure 3-3a**, you can see that the standard watchdog only alerts the system on late faults. In window watchdogs, a pulse must arrive before the watchdog timeout and after the lower boundary specification; otherwise, a fault occurs. Looking at **Figure 3-3b**, notice how the window watchdog alerts the system on both early and late faults.

For more information about watchdog timer applications and watchdog timer features, read the short article, "Exploring watchdog timer applications," and watch the video, "Voltage Supervisor Features."

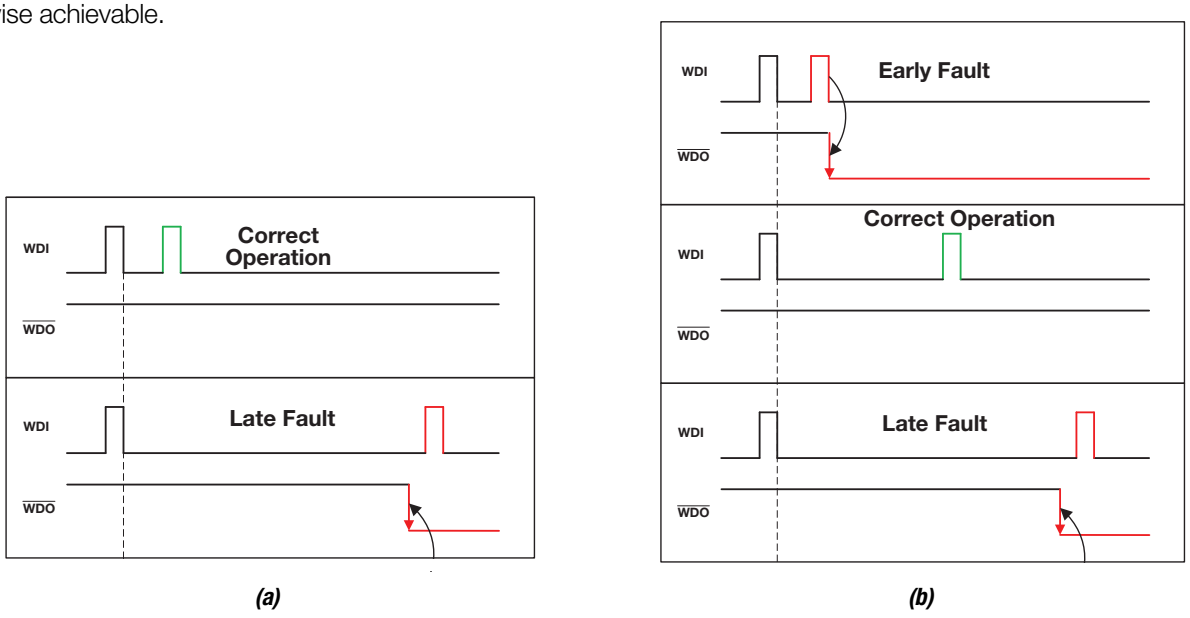


Figure 3-3. Standard watchdog timing diagram (a); window watchdog timing diagram (b).

4.1. Electrical characteristics table

Table 4-1 is an electrical characteristics table for the TPS3850. This device features a window supervisor for overvoltage and undervoltage monitoring, and has a window watchdog feature. This section will cover how to read and interpret such a table.

Parameter		Test Conditions	Min	Typ	Max	Unit
General Characteristics						
V_{DD} (1)(2)(3)	Supply voltage		1.6		6.5	V
I_{DD}	Supply current			10	19	µA
RESET Function						
V_{POR} (2)	Power-on reset voltage	I_{RESET} = 15 µA, $V_{OL(MAX)}$ = 0.25 V			0.8	V
V_{UVLO} (1)	Undervoltage lockout voltage					V
$V_{IT+(OV)}$	Overvoltage SENSE threshold accuracy, entering $\overline{RESET}$		$V_{IT+(nom)}$–0.8%	1.35	$V_{IT+(nom)}$+0.8%	
$V_{IT-(UV)}$	Undervoltage SENSE threshold accuracy, entering $\overline{RESET}$		$V_{IT+(nom)}$–0.8%		$V_{IT+(nom)}$+0.8%	
$V_{IT(ADJ)}$	Falling SENSE threshold voltage, adjustable version only		0.3968	0.4	0.4032	V
V_{HYST}	Hysteresis voltage		0.2%	0.5%	0.8%	
I_{CRST}	CRST pin charge current	CRST = 0.5 V	337	375	413	nA
V_{CRST}	CRST pin threshold voltage		1.192	1.21	1.228	V
Window Watchdog Function						
I_{CWD}	CWD pin charge current	CWD = 0.5 V	337	375	413	nA
V_{CWD}	CWD pin threshold voltage		1.192	1.21	1.228	V
V_{OL}	$\overline{RESET}$, $\overline{WDO}$ output low	VDD = 5 V, I_{SINK} = 3 mA			0.4	V
I_D	$\overline{RESET}$, $\overline{WDO}$ output leakage current	VDD = 1.6 V, $V_{\overline{RESET}}$, = $V_{\overline{WDO}}$ = 6.5 V			1	µA
V_{IL}	Low-level input voltage (SET0, SET1)				0.25	V
V_{IH}	High-level input voltage (SET0, SET1)		0.8			V
$V_{IL(WDI)}$	Low-level input voltage (WDI)				0.3 × V_{DD}	V
$V_{IH(WDI)}$	High-level input voltage (WDI)		0.8 × V_{DD}			V
I_{SENSE}	SENSE pin idle current	TPS3850Xyy(y), V_{SENSE} = 5.0 V, VDD = 3.3 V		2.1	2.5	µA
		TPS3850H01 only, V_{SENSE} = 5.0 V, VDD = 3.3 V	-50		50	nA

(1) When V_{DD} falls below V_{UVLO}, $\overline{RESET}$ is driven low.
(2) When V_{DD} falls below V_{POR}, $\overline{RESET}$ and $\overline{WDO}$ are undefined.
(3) During power-on, V_{DD} must be a minimum 1.6 V for at least 300 µs before the output corresponds to the SENSE voltage.

Table 4-1. Electrical characteristics table for the TPS3850.

Common terms

V_{DD} – Supply voltage. This is the supply voltage range needed to power the IC.

I_{DD} – Supply current. This is the current going into the VDD pin from the power supply. I_{DD} is sometimes referred to as quiescent current (I_Q).

V_{POR} – Power-on reset voltage. V_{POR} is the minimum input voltage required for a controlled output state. The supervisor output is undefined when V_{DD} is below **V_{POR}**. To mitigate this glitch, read the section in Chapter 5, "Mitigating the Indeterminate Output of a Voltage Supervisor During Power Up/Down."

V_{UVLO} – Undervoltage lockout voltage. This is the voltage at the V_{DD} pin to which the device's internal components become functional and the output to the device is defined. For full functionality of the device, V_{DD} will need to reach at least V_{DD} at minimum.

$V_{IT+(OV)}$ – Overvoltage threshold accuracy. This indicates the voltage threshold at which the device detects an overvoltage condition. In some data sheets, this can be expressed as an accuracy percentage or as a voltage.

$V_{IT-(UV)}$ – Undervoltage threshold accuracy. This indicates the voltage threshold at which the device detects an undervoltage condition. In some data sheets, this can be expressed as an accuracy percentage or as a voltage.

V_{HYST} – Hysteresis voltage. This is the difference between the rising (V_{IT+}) and falling (V_{IT-}) thresholds to prevent false triggers if the monitored voltage is oscillating around V_{IT-}. In a window supervisor, there is hysteresis for both the undervoltage and overvoltage thresholds. To be more specific, for an undervoltage condition, the hysteresis voltage equals $V_{IT+(UV)}$ - $V_{IT-(UV)}$. For an overvoltage condition, the hysteresis voltage equals $V_{IT+(OV)}$ - $V_{IT-(OV)}$. For a visual representation, see Section 7.3.3 in the TPS3850 data sheet.

I_{CRST} and I_{CWD} – Pin charge current. This is the charge current across the device's CRST pin or CWD pin.

V_{CRST} and V_{CWD} – Pin threshold voltage. This is the threshold voltage across the device's CRST pin or CWD pin.

V_{OL} – Low-level output voltage. This is the maximum voltage at the supervisor output during a logic-low condition.

I_D – Leakage current. This is the leakage current that occurs when the internal metal-oxide semiconductor field-effect transistor (MOSFET) is turned off due to the pull-up resistor used in open-drain output topologies.

V_{IL} – Low-level input voltage. This is the low-level threshold voltage at the input, to which the device will recognize a low logic level.

V_{IH} – High-level input voltage. This is the high-level threshold voltage at the input, to which the device will recognize a high logic level.

4.2. Timing requirements table

Table 4-2 is a timing requirements table for the TPS3850. This section will cover how to read and interpret such a table to understand when the watchdog will trigger a fault.

			Min	Typ	Max	Unit
General						
t_{INIT}	CWD, CRST pin evaluation period			381		µs
t_{SET}	Time required between changing SET0 and SET1 pins			500		µs
	SET0, SET1 pin setup time			1		µs
	Startup delay(1)			300		µs
RESET Function						
t_{RST}	Reset timeout period	CRST = NC	170	200	230	ms
		CRST = 10 kΩ to VDD	8.5	10	11.5	ms
$t_{RST-DEL}$	V_{SENSE} to RESET delay	VDD = 5 V, $V_{SENSE} = V_{IT+(OV)} + 2.5\%$		35		µs
		VDD = 5 V, $V_{SENSE} = V_{IT-(UV)} - 2.5\%$		17		
Window Watchdog Function						
WD ratio	Window watchdog ratio of lower boundary to upper boundary	CWD = programmable, SET0 = 0, SET1 = 0(2)		1/8		
		CWD = programmable, SET0 = 1, SET1 = 1(2)		1/2		
		CWD = programmable, SET0 = 0, SET1 = 1(2)(3)		3/4		
t_{WDL}	Window watchdog lower boundary	CWD = NC, SET0 = 0, SET1 = 0	19.1	22.5	25.9	ms
		CWD = NC, SET0 = 0, SET1 = 1	1.5	1.85	2.2	ms
		CWD = NC, SET0 = 1, SET1 = 0	Watchdog disabled			
		CWD = NC, SET0 = 1, SET1 = 1	680	800	920	ms
		CWD = 10 kΩ to VDD, SET0 = 0, SET1 = 0	7.7	9.0	10.4	ms
		CWD = 10 kΩ to VDD, SET0 = 0, SET1 = 1	7.7	9.0	10.4	ms
		CWD = 10 kΩ to VDD, SET0 = 1, SET1 = 0	Watchdog disabled			
		CWD = 10 kΩ to VDD, SET0 = 1, SET1 = 1	1.5	1.85	2.2	ms
t_{WDU}	Window watchdog upper boundary	CWD = NC, SET0 = 0, SET1 = 0	46.8	55.0	63.3	ms
		CWD = NC, SET0 = 0, SET1 = 1	22.0	27.5	33.0	ms
		CWD = NC, SET0 = 1, SET1 = 0	Watchdog disabled			
		CWD = NC, SET0 = 1, SET1 = 1	1360	1600	1840	ms
		CWD = 10 kΩ to VDD, SET0 = 0, SET1 = 0	92.7	109.0	125.4	ms
		CWD = 10 kΩ to VDD, SET0 = 0, SET1 = 1	165.8	195.0	224.3	ms
		CWD = 10 kΩ to VDD, SET0 = 1, SET1 = 0	Watchdog disabled			
		CWD = 10 kΩ to VDD, SET0 = 1, SET1 = 1	8.8	11.0	13.2	ms
$t_{WD-setup}$	Setup time required for device to respond to changes on WDI after being enabled			150		µs
	Minimum WDI pulse duration			50		ns
t_{WD-del}	WDI to $\overline{WDO}$ delay			50		ns

(1) During power-on, V_{DD} must be a minimum 1.6 V for at least 300 µs before the output corresponds to the SENSE voltage.

(2) 0 refers to $V_{SET} \leq V_{IL}$, 1 refers to $V_{SET} \geq V_{IH}$.

(3) If this watchdog ratio is used, then $t_{WDL(max)}$ can overlap $t_{WDU(min)}$.

Table 4-2. Timing requirements table for the TPS3850

Common terms

T_{INIT} – Evaluation period. This is the amount of time it takes for the device to recognize different configurations on the CWD and CRST pins.

T_{SET} – SET pin time period. When configuring both the SET0 and SET1 pin, this is the time required between changing SET0 and SET1.

Startup delay – V_{DD} must be above V_{DD} (at minimum) for T_{STRT} before the device is fully functional.

T_{RST} – Reset timeout period. This is the amount of time that the supervisor holds the reset output to the fault state once the system enters a nonfault state. In this example, the TPS3850 will hold the reset low for 200 ms if the CRST pin is left unconnected.

$T_{RST-DEL}$ – V_{SENSE} to $\overline{RESET}$ delay. This is the amount of time it takes for the output to trigger a fault event coming from a nonfault state. This is also known as the propagation delay.

T_{WDL} – Window watchdog lower boundary. For voltage supervisors with a window watchdog function, there is a lower boundary limit on the watchdog timeout. If the watchdog input (WDI) is received before this T_{WDL} period, the watchdog output (WDO) will trigger a fault event.

Figure 4-1 shows that when WDI is received before T_{WDL} ($t < T_{WDL}$), the $\overline{WDO}$ triggers a fault.

T_{WDU} – Window watchdog upper boundary. For voltage supervisors with a window watchdog function, in addition to the lower boundary there is an upper boundary limit on the watchdog timeout. If the WDI input is received after this T_{WDU} period, the WDO will trigger a fault event. **Figure 4-1** shows that when WDI is received before T_{WDU} and after T_{WDL} ($T_{WDL} < t < T_{WDU}$), the $\overline{WDO}$ does not trigger a fault as it is within the window period

Minimum WDI pulse detection – The pulse-width duration on the WDI pin during which the device will detect an event on the WDI.

T_{WD-DEL} – WDI to $\overline{WDO}$ delay. This is the amount of time it takes for the device to react to an event on the WDI pin to trigger a response on the WDO pin. This is also known as propagation delay on the watchdog.

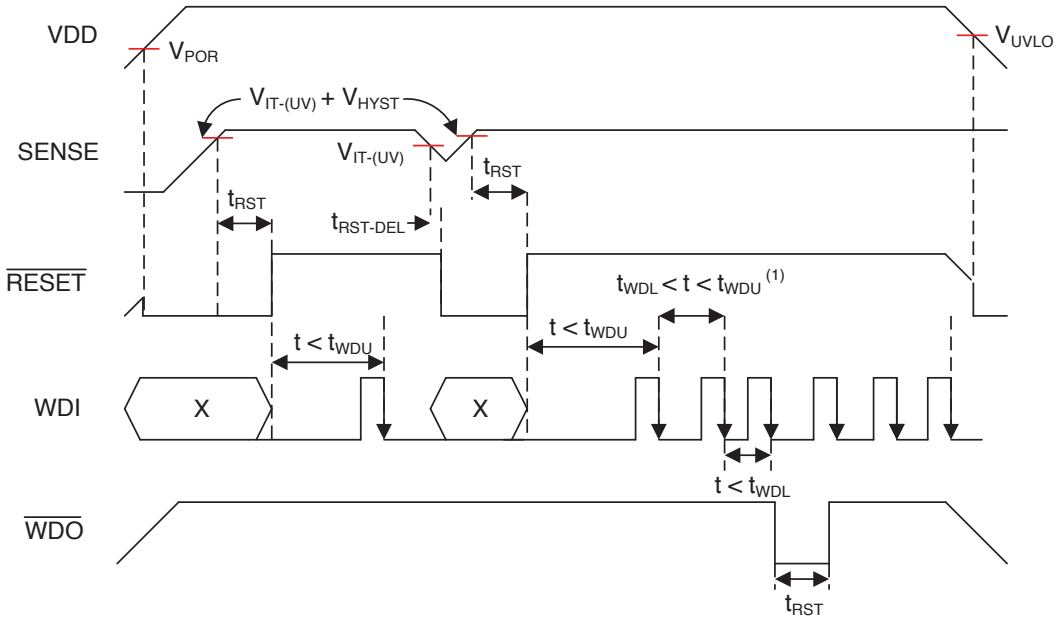


Figure 4-1. TPS3850 timing diagram.

5.1. Adding programmable delay to voltage detectors

Michael DeSando

In many applications with multiple power rails, power-up timing is critical to ensure proper system protection and functionality. The normal operation of a voltage detector monitors a voltage rail and triggers a fault immediately when a fault in the monitored voltage occurs. This fault occurs either because of an undervoltage or overvoltage condition, depending on the voltage detector used. When the fault condition is removed, the voltage detectors return to normal operation after the inherent propagation delay from the output rising from a logic low to a logic high. This is unlike voltage supervisors and reset integrated circuits (IC), which have a fixed or programmable delay before returning to normal operation from a fault condition.

Let's cover some application techniques for adding a reset time delay to voltage detectors with open-drain output topologies. Push-pull devices do not allow an additional reset time delay because the pull-up resistor is replaced with an internal metal-oxide semiconductor field-effect transistor (MOSFET), and there is very little resistance while the MOSFET is on. This causes the capacitor to be shorted out of the circuit, preventing the additional delay at the output.

Not only is adding programmable delay to voltage detectors useful for applications that require a reset time delay, it can also be useful for applications such as those from the automotive and industrial sectors that require wide input voltage (wide VIN), with reset time delay. TI's family of wide VIN voltage detectors (such as those from the TPS3700, TPS3701, TPS3702, TPS3710, and TPS3711) have 18- and 36-V operating voltage ranges and can monitor undervoltage and overvoltage conditions, but don't have a reset delay because they are voltage detectors. By following the techniques explained in this e-book, it's possible to add a programmable reset time delay to these devices, as well as any other open-drain voltage detector.

To add a programmable delay to a voltage detector, use a capacitor followed by a buffer at the output of the voltage detector, as shown in **Figure 5-1**.

The C_d pin adds a programmable reset time delay on the rising edge because when the output rises, the capacitor needs time to charge via the pull-up resistor. **Equation 5-1** calculates the delay as:

$$\text{delay} = C_d \bullet \frac{VIH_{buffer}}{V_{pull-up} / R_{pull-up}} \quad (1)$$

For more information and test results, see the application note, "Adding Reset Delay to Voltage Detectors."

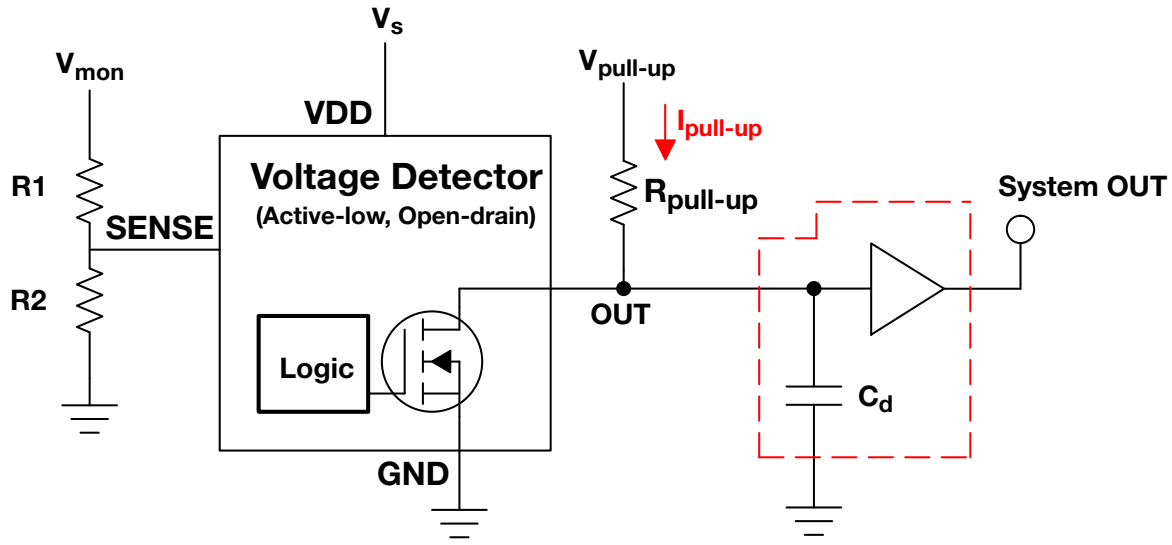


***Figure 5-1.** Adding programmable reset time delay to detectors.*

5.2. Adding hysteresis to supervisors

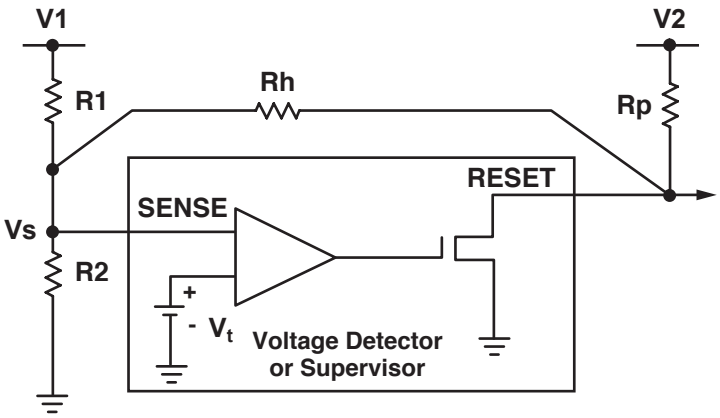
Sureena Gupta

As the input voltage to a system dips below the minimum required voltage for operation, the voltage supervisor asserts a reset signal to turn off the system. When the system is turned off, current flow stops, and the voltage to the voltage supervisor may rise due to the decreased current drop. This erroneous reset lasts as long as the input voltage spikes exceed the threshold voltage or the voltage dips fall below the threshold voltage. This condition can be undesirable for various applications.

In order to avoid an erratic change in input voltage caused by a discharging battery or perhaps a noisy power supply, you can add hysteresis to the supervisor circuitry. **Figure 5-2** illustrates this solution.

The addition of hysteresis implies that the supervisor is turned off when the input voltage falls below the threshold voltage, but is not turned back on until the input voltage rises above another predetermined threshold voltage. For instance, it can be equivalent to the voltage supplied by a newly replaced battery for a battery-supplied input voltage source.

A hysteresis resistor helps increase the hysteresis of the input voltage by increasing the threshold voltage when the input voltage is increasing and decreasing the threshold voltage when the input voltage is decreasing. To learn more about this phenomenon, see the application report, "Adding Hysteresis to a Supply Voltage Supervisor."



Where:

V1 is the input supply voltage;

V2 is the voltage used that the ouput is pulled up to;

Vs is the voltage at the sense pin;

V_t is the threshold voltage or reference voltage;

Rp is used as a pullup on the $\overline{\text{RESET}}$ output;

Rh is the resistor used to increase the hysteresis.

Figure 5-2. *General schematic for a supervisor with increased hysteresis.*

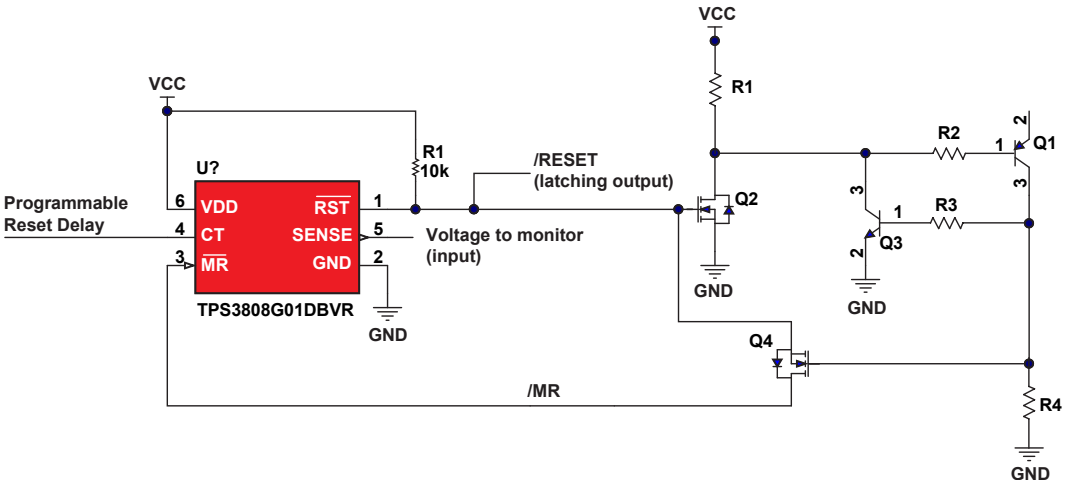


Figure 5-3. TPS3808 with external latch circuitry attached to the output.

5.3. Latching voltage supervisors

Michael DeSando

Certain applications require the output to latch when the voltage rail being monitored drops below the defined threshold and remain low even if the supply comes back up. This type of configuration requires user intervention to go back to normal operation, which can provide an extra measure for safety-critical applications. Other applications that can use a latching output configuration include any application that needs to permanently shut off a device in the system in the event of an undervoltage lockout.

One solution, shown in **Figure 5-3**, uses a TI supervisor/reset integrated circuit with the manual reset feature (MR) such as the TPS3808. By connecting the external latching reset output circuit to the TPS3808, the RESET output of the TPS3808 will now be a latching reset output type. For more information on the circuit analysis of the latching circuit connected to the output of the TPS3808, see the application report, "Latching a Voltage Supervisor (Reset IC)"

A latching feature is also provided in the TPS3703-Q1 window voltage supervisor, as shown in **Figure 5-4**. The TPS3703-Q1 features a voltage latch mode on the RESET pin when connecting the CT pin to ground. In the latch mode, the RESET pins remain low once the RESET pin triggers to the active logic low state regardless of the VSENSE pin status. Putting TPS3703-Q1 into latch mode by connecting the CT pin to ground does not initiate a fault condition or activate the RESET pin to logic low, but only causes the RESET pin to latch logic low once a fault does occur.

Providing a voltage to the CT pin that is greater than the CT pin threshold voltage, V_{CT}, unlatches the device. To ensure that the device is out of latch mode, supply at least 1.2 V to the CT pin. A pull-down resistor along with a series resistor on the CT pin will limit current consumption of the system.

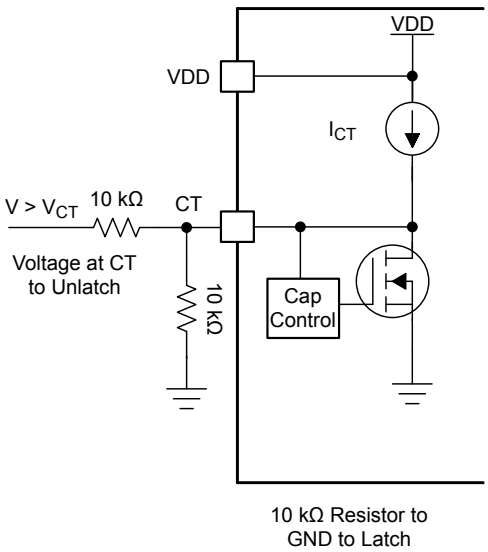


Figure 5-4. TPS3703-Q1 window voltage supervisor latch feature.

5.4. Latching watchdog timers

The purpose of a watchdog feature in a supervisor is to monitor the watchdog input (WDI) pin. This input is usually driven by a microcontroller output. When the system is running properly, software on the microcontroller regularly toggles or pulses a signal output at a specifically defined rate. If the software stops executing properly, this periodically pulsed signal will either speed up, slow down or stop altogether.

A falling pulse signal frequency outside of a defined window range set on the watchdog timer asserts the watchdog output (WDO). This active-low output is usually connected to the RESET input of the microcontroller or it may be used to disable some other device via an enable pin. In this way, a watchdog fault causes a reset of the system or controlled function.

In some applications, such a fault could require further review before the system or function is allowed to resume. In such cases, the WDO must latch and remain active and logic low even if the WDI pin begins pulsing again as expected. Clearing this latched state requires user intervention.

To latch the watchdog output, add in one open-drain buffer and a capacitor between the CRST pin (watchdog reset delay pin) and ground, as shown in **Figure 5-5**. For more details on the circuit analysis and to view bench test results, read the application note, "Latching a Watchdog Timer."

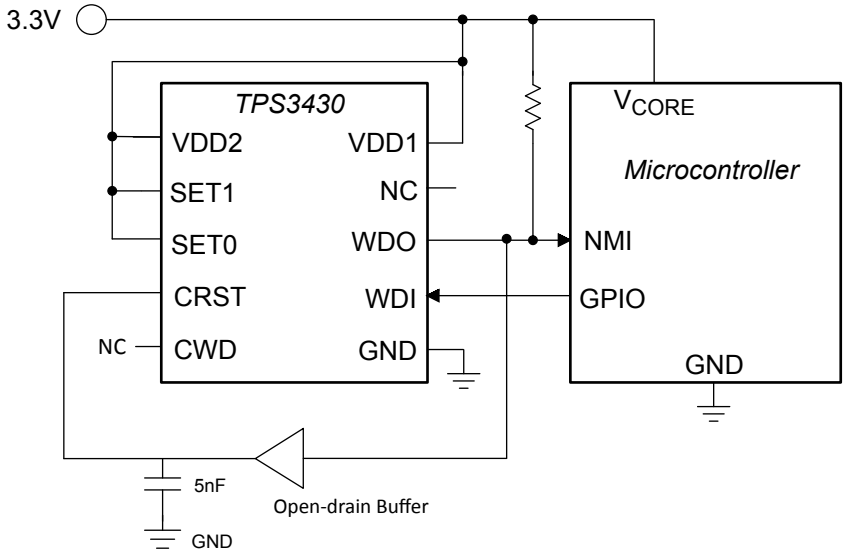


***Figure 5-5.** Latching watchdog circuity using buffer and capacitor.*

5.5. Using a Zener diode or shunt voltage reference to drop the input voltage to a supervisor

Marcoo Zamora

Voltage supervisors typically monitor voltage rails for non-ideal voltage-rail variations such as undervoltage or overvoltage to notify microcontrollers, field-programmable gate arrays, application-specific integrated circuits or system-on-chips about system health.

Since voltage supervisors are normally paired with these kinds of processors, supervisors have fixed voltage thresholds to monitor common processor voltage rails, such as up to 5 V. Thus, the V_{DD} recommended operating condition is also limited to similar voltages, such as 5.5 V on the TPS3890. The challenge arises when design requirements call for a supervisor with TPS3700 or TPS3890 functionality, but for operating and monitoring 12-V voltage rails. This is a challenge in applications that need early detection (such as electric vehicle/hybrid electric vehicle power trains) or factory automation (where 12-V voltage rails need to be continuously monitored).

There are three methods to overcome this challenge. One method is to use a voltage divider (as shown in **Figure 5-6**); however, this solution comes at the expense of power, due to continued leakage current. Another method is to use a Zener diode; however, this method also requires a high amount of leakage current to keep the Zener diode regulated.

The last method uses a shunt voltage reference (as shown in **Figure 5-7**), particularly the LM4040, to clamp the voltage. A shunt voltage reference leaks much less current than the Zener diode and provides the most efficient power loss.

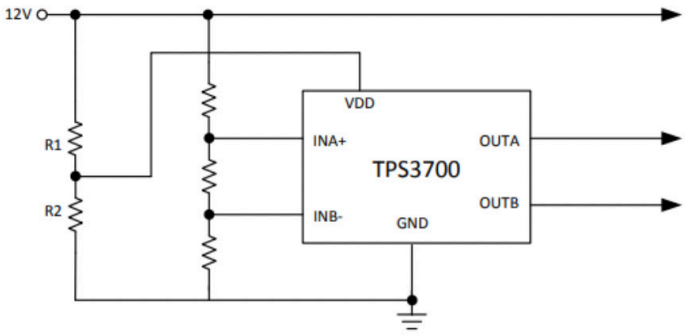


Figure 5-6. Voltage divider method at V_{DD}.

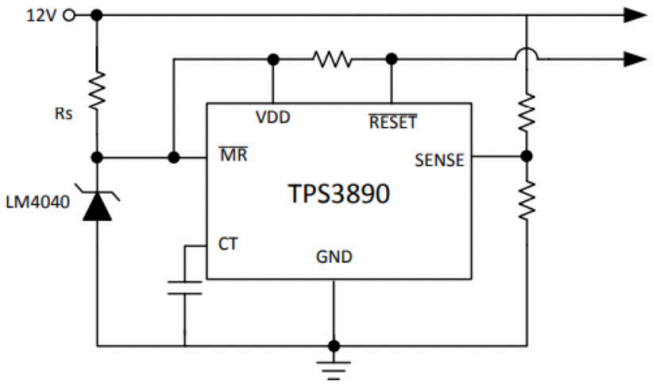


Figure 5-7. Using the LM4040 to clamp the voltage.

To read more on this topic, see the application note, "Using Voltage Supervisors in High Voltage Applications."

5.6. Mitigating the indeterminate output of a voltage supervisor during power up/down

Michael DeSando

Voltage supervisors require a minimum voltage called the power-on-reset voltage (V_{POR}) on the supply voltage pin before the internal circuitry that creates the voltage reference for comparing the sensed voltage is operational. Specifically, V_{POR} defines the minimum required voltage threshold to turn on the internal output metal-oxide semiconductor field-effect transistor (MOSFET) that defines the output logic state.

When the supply voltage is below V_{POR}, the output logic state is undefined and the output voltage is indeterminate. The indeterminate output voltage only appears at the output (RESET) of an active-low voltage supervisor when V_{DD} is below V_{POR}.

To eliminate this effect, use a P-channel junction field effect transistor (JFET), as shown in **Figure 5-8**. The JFET ensures that the output remains low even during power up and power down.

To get a full understanding of how this circuit works, see the application note, "Mitigating the Indeterminate Output of a Voltage Supervisor (Reset IC) During Power Up/Down."

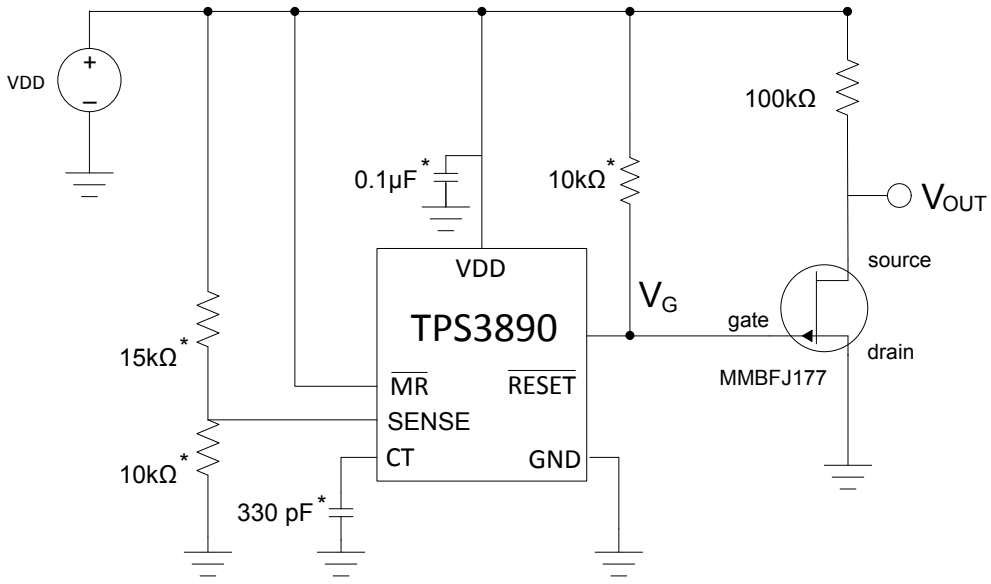


***Figure 5-8.** Adding a P-type JFET to mitigate the indeterminate output voltage.*

5.7. How to Sense a Negative Voltage with a Voltage Supervisor

Michael Hartshorne

Monitoring a negative voltage can be tricky because most systems have ground-referenced logic signals, requiring level shifting to enable communication. One way to accomplish the necessary level shifting is to use open-drain outputs. **Figure 5-9**'s schematic shows how to use the TPS3700 in a negative rail, with the outputs level-shifted up to give positive logic.

In **Figure 5-9**, the monitored voltage (V_{MON}) is a negative voltage relative to ground. You can program the overvoltage and undervoltage limits with R1, R2 and R3 in the same way as for a positive voltage (see product data sheets for more information). The open-drain outputs of the TPS3700 or TPS3701 are independent of V_{DD}, which means that $V_{PULL-UP}$ can be a positive voltage that enables a positive ground-referenced logic voltage to interface with any microcontrollers or processors.

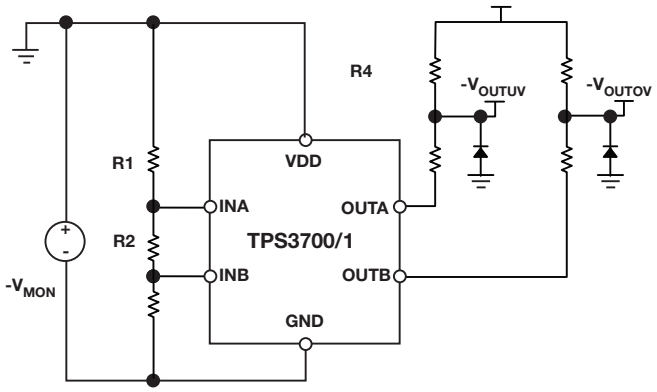


Figure 5-9. TPS3700 configured for negative voltage sensing.

Sensing a negative voltage using the previously described method requires additional diodes and resistors on the output. Another trick for sensing a negative voltage that will have fewer additional components is to use a positive voltage to shift up the resistor-divider voltages so that the divided threshold voltage is positive relative to ground. The four-channel TPS386000 supervisor makes this easy by providing a reference voltage to which you can connect the resistor chain. See **Figure 5-10**.

In **Figure 5-10**, the $V_{MON(4,NEG)}$ node represents the negative monitored voltage and $V_{MON(4,POS)}$ represents the positive monitored voltage. Negative monitoring is possible because the resistor divider is referenced to the V_{REF} pin (a 1.2-V output) instead of ground-referenced, as in the positive channel. The RESET output will go high in **Figure 5-10** when the negative channel falls below -14.92 V and the positive channel rises above 15.04 V, nominally.

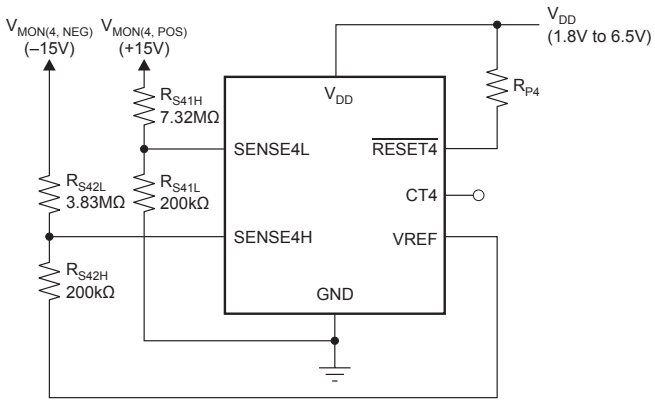


Figure 5-10. Using an external voltage reference to sense a negative voltage.

Additional Resources

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View TI's wide portfolio of voltage supervisors and reset ICs that includes watchdog timers, push-button ICs, voltage detectors, fixed time delay supervisors and programmable time delay supervisors.

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Voltage supervisors 101 video training series

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Voltage Supervisors Frequently Asked Questions

This application note answers the most commonly asked questions for voltage supervisors/reset ICs, voltage detectors, watchdog timers, and all related monitoring devices.

Voltage Supervisors (Reset ICs) Quick Reference Guide

An overview guide to voltage supervisors/reset ICs, including selection tables.

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