PIC32MZ Graphics (DA) Family

PIC32MZ Graphics (DA) Family
Silicon Errata and Data Sheet Clarification

The PIC32MZ Graphics (DA) family devices that you have received conform functionally to the current Device Data Sheet (DS60001361**F**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. If applicable, any silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC32MZ Graphics (DA) family silicon.

> **Note:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table (if applicable) apply to the current silicon revision (**A1**).

Data Sheet clarifications and corrections (if applicable) start on page 17.

The silicon revision level can be identified using the current version of MPLAB® X IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB X IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB X IDE project.
3. Configure the MPLAB X IDE project for the appropriate device and hardware debugger.
4. Select *Window > Dashboard*, and then click the **Refresh Debug Tool Status** icon ( ).
5. The part number and the Device and Revision ID values appear in the **Output** window.

> **Note:** If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The Device and Revision ID values for the various PIC32MZ Graphics (DA) family silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID[1]	Revision ID for Silicon Revision[1]
		A1
PIC32MZ1025DAA169	0x05F0C053	0x1
PIC32MZ1025DAB169	0x05F0D053	
PIC32MZ1064DAA169	0x05F0F053	
PIC32MZ1064DAB169	0x05F10053	
PIC32MZ2025DAA169	0x05F15053	
PIC32MZ2025DAB169	0x05F16053	
PIC32MZ2064DAA169	0x05F18053	
PIC32MZ2064DAB169	0x05F19053	
PIC32MZ1025DAG169	0x05F42053	
PIC32MZ1025DAH169	0x05F43053	
PIC32MZ1064DAG169	0x05F45053	
PIC32MZ1064DAH169	0x05F46053	
PIC32MZ2025DAG169	0x05F4B053	
PIC32MZ2025DAH169	0x05F4C053	
PIC32MZ2064DAG169	0x05F4E053	
PIC32MZ2064DAH169	0x05F4F053	

Note 1: Refer to the **"Memory Organization"** and **"Special Features"** chapters in the current Device Data Sheet (DS60001361**F**) for detailed information on Device and Revision IDs for your specific device.

PIC32MZ Graphics (DA) Family

TABLE 1: **SILICON DEVREV VALUES (CONTINUED)**

Part Number	Device ID[1]	Revision ID for Silicon Revision[1]
		A1
PIC32MZ1025DAA176	0x05F78053	0x1
PIC32MZ1025DAB176	0x05F79053	
PIC32MZ1064DAA176	0x05F7B053	
PIC32MZ1064DAB176	0x05F7C053	
PIC32MZ2025DAA176	0x05F81053	
PIC32MZ2025DAB176	0x05F82053	
PIC32MZ2064DAA176	0x05F84053	
PIC32MZ2064DAB176	0x05F85053	
PIC32MZ1025DAG176	0x05FAE053	
PIC32MZ1025DAH176	0x05FAF053	
PIC32MZ1064DAG176	0x05FB1053	
PIC32MZ1064DAH176	0x05FB2053	
PIC32MZ2025DAG176	0x05FB7053	
PIC32MZ2025DAH176	0x05FB8053	
PIC32MZ2064DAG176	0x05FBA053	
PIC32MZ2064DAH176	0x05FBB053	
PIC32MZ1025DAA288	0x05F5D053	0x1
PIC32MZ1025DAB288	0x05F5E053	
PIC32MZ1064DAA288	0x05F60053	
PIC32MZ1064DAB288	0x05F61053	
PIC32MZ2025DAA288	0x05F66053	
PIC32MZ2025DAB288	0x05F67053	
PIC32MZ2064DAA288	0x05F69053	
PIC32MZ2064DAB288	0x05F6A053	

Note 1: Refer to the **"Memory Organization"** and **"Special Features"** chapters in the current Device Data Sheet (DS60001361**F**) for detailed information on Device and Revision IDs for your specific device.

TABLE 2:   SILICON ISSUE SUMMARY

Module	Feature	Item	Issue Summary	Affected Revisions[1]
				A1
Primary Oscillator	Primary Oscillator Crystal	1.	The Primary Oscillator (POSC) has been tested in a normal power-up sequence and supports specific crystal operation.	X
Secondary Oscillator	Secondary Oscillator Crystal	2.	The Secondary Oscillator (SOSC) does not support crystal operation.	X
Reset	BOR	3.	A system Reset is not generated on a BOR event (VPORIO < VDDIO < VBORIO). This will stop system clocks with all the I/O pin functions frozen in the present state until either VDDIO falls to VPORIO or VDDIO > VBORIO.	X
Reset	HVD Reset	4.	A BOR event also sets the HVD1V8R (RCON<29>) bit.	X
Power-Saving	PMD Bits	5.	Turning off the REFCLK modules through the PMD (PMD6<11:8>) bits causes unpredictable device behavior.	X
DMA	PMD Bits	6.	Setting the PMD bit for DMA (PMD7<4>) does not disable clocks or DMA peripheral.	X
VBAT	—	7.	VBAT is not functional.	X
Deep Sleep	—	8.	Deep Sleep mode is not functional.	X
I^{2}C	—	9.	The I^{2}C module does not function reliably under certain conditions.	X
ADC	Interrupts	10.	ADC Group Early Interrupt is not functional (IRQ205).	X
ADC	Level Trigger	11.	ADC level trigger will not perform burst conversions in debug mode.	X
ADC	DNL	12.	In Differential mode, code 3072 is not within the specification.	X
ADC	Turbo Mode	13.	Turbo mode is not functional.	X
SDHC	Clock	14.	The SDHC module requires System PLL to be turned ON.	X
SDHC	Clock Stability	15.	The SDHC module may not function if the $\overline{\text{SDCD}}$ pin is not used.	X
SDHC	Card Detect Status	16.	Card detect status indication through the CDSLVL bit (SDHCSTAT1<18>) is inverted.	X
SDHC	Write Protect Status	17.	Write protect status indication through the WPSLVL bit (SDHCSTAT1<19>) is inverted.	X
SDHC	Stop at Block Gap	18.	The Stop at Block Gap feature of the SDHC module is not functional.	X
HLVD	—	19.	High/Low-Voltage Detect module is not functional.	X
DDR2C	—	20.	DDR2 is functional only between 0°C and 70°C.	X
DDR2C	Internal DDRVREF Circuit	21.	Internal DDRVREF circuit is not functional.	X
SQI	XIP Mode	22.	SQI XIP mode is not functional in cached memory space (KSEG2).	X
USB	Interrupt	23.	USB General Event Interrupt (IRQ 132) is not persistent.	X
USB	Resume	24.	The USB module does not support remote wake-up.	X
System Bus	Writes	25.	The EERP bit (SBTxECON<24>) is not functional.	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

PIC32MZ Graphics (DA) Family

Module	Feature	Item	Issue Summary	Affected Revisions[1]
				A1
Crypto	Flash Data Access	26.	The Crypto module cannot access data from Flash.	X
UART	Overflow	27.	Clearing the OERR bit (UxSTA<1>) clears the receiver buffer.	X
EBI	Chip Select	28.	For Asynchronous NOR Flash, EBI internal clock specification, T_{EBICLK} (EB10), is not met.	X
CTMU	Triggers	29.	Edge Sequencing mode (EDGSEQEN(CTMUCON<2>)) and Edge modes are not functional.	X
CTMU	TGEN	30.	When the TGEN bit is set, manual current sourcing from CTMU is not possible.	X
Temperature Sensor	—	31.	The temperature sensor does not function.	X
ICSP	TDO	32.	While programming on any ICSP PGECx/PGEDx pair, the TDO pin will toggle.	X
PORTS	V_{IH} Electrical Specification	33.	The V_{IH} specification of $0.65 * V_{DDIO}$ is not met.	X
Primary Oscillator	Automatic Gain Control (AGC)	34.	The Primary Oscillator Automatic Gain Control (AGC) is not functional.	X
Primary Oscillator	Automatic Gain Control (AGC)	35.	The Primary Oscillator AGC Gain Search Step Settling Time Control bits are not functional.	X
Primary Oscillator	Primary Oscillator Fine Gain Control	36.	The Primary Oscillator Fine Gain Control bits are not functional.	X
GPU	GPURESET bit	37.	The GPU Run-time enable/Disable feature is not functional.	X
SDHC	SDWPPOL bit	38.	The SDHC Write-protect Polarity Inversion feature is not functional.	X
PMP	Status Flags	39.	The PMP input buffer full flag, IB0F, and the output buffer underflow, OBUF, are getting set as soon as the PMP module is enabled in Slave mode (PMPTTL bit (PMCON<10>) is equal to '1').	X
I²C	Start/Restart	40.	When the I²C module is in Slave mode, Start and Restart interrupts are not functional.	X
Crypto	Partial Packet	41.	The Crypto Engine does not support partial packet processing.	X
Crypto	Zero-length Packet	42.	The Crypto Engine does not support a Hash operation on an empty string.	X
CTMU	Idle	43.	CTMU current source is not enabled in Idle mode (CTMUSIDL bit in the CTMUCON register is equal to '1'), which prevents ADC if enabled in Idle mode from being able to measure the CTMU temperature sensor.	X
Timer1	Asynchronous Counter	44.	Timer1 in Asynchronous External Counter mode does not reflect the first count from an external T1CK input.	X
Timer1	TMR1 Register	45.	TMR1 register of Timer1 in Asynchronous mode remains at initial set value for five external clock pulses after wake-up from Sleep mode.	X
Timer1	Asynchronous Mode	46.	Timer1 counts beyond the period value in Asynchronous mode when the period is 0x01.	X

Note 1:   Only those issues indicated in the last column apply to the current silicon revision.

TABLE 2: **SILICON ISSUE SUMMARY (CONTINUED)**

Module	Feature	Item	Issue Summary	Affected Revisions[1]
				A1
Timer1	Gated Mode	47.	Timer1 does not work properly in Gated mode with prescaler enabled.	X
Timer1	TMR1 Register Writes	48.	Back-to-back writes to the TMR1 register are not allowed for four PBCLK cycles.	X
Timer1	Asynchronous Timer1	49.	The Asynchronous Timer Write Disable bit, TWDIS (TxCON<12>), and the Asynchronous Timer Write in Progress bit, TWIP (TxCON<11>), are non-functional.	X
UART	High-Speed Mode	50.	The UART Stop bit duration is shorter than expected in High-Speed mode (UxMODE.BRGH =1) for baud rates less than 7.5 Mbps.	X
Sleep	IPD	51.	3 mA increase in sleep current when PB5DIV is disabled.	X
CFG	Unique ID	52.	Unique ID is not programmed on devices which are released earlier than trace code dated 1821xxx.	X

Note 1:   Only those issues indicated in the last column apply to the current silicon revision.

PIC32MZ Graphics (DA) Family

Silicon Errata Issues

> **Note:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A1**).

1. Module: Primary Oscillator

The POSC has been tested in a normal power-up sequence and supports specific crystal operation.

Work around 1

The Primary Oscillator (POSC) has been characterized to operate at 8 MHz and 12 MHz when the circuit shown in Figure 1 is implemented, and the operating conditions listed in Table 3 are met.

Work around 2

Alternatively, use an external clock or Internal FRC Oscillator. Note that communication interfaces (DDR2, USB, etc.,) with tighter clock accuracy requirements will not function with the FRC as clock source.
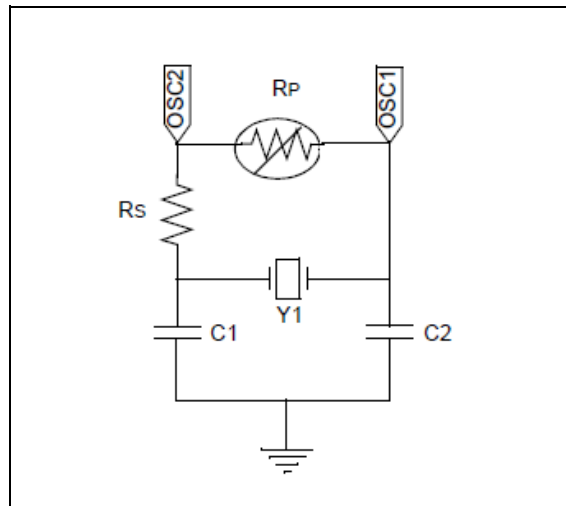
FIGURE 1: Posc CRYSTAL CIRCUIT

TABLE 3: CRYSTAL SPECIFICATION

Crystal Frequency (See Note 1)	Series Resistor Rs	Posc Gain Setting POSCGAIN<1:0> (DEVCFG0<20:19>)	Posc Boost Setting POSCBOOST (DEVCFG0<21>)
8 MHz	2 kΩ	`0b00 (GAIN_0)	`0b1
12 MHz	1 kΩ	`0b00 (GAIN_0)	`0b1

Note 1: Using any other crystal frequency will require special component selection and characterization.

2: A parallel register (RP) should not be used to increase the gain of the POSC.

Affected Silicon Revisions

A1						
X						

2. Module: Secondary Oscillator

A crystal oscillator cannot be used as the input to the Secondary Oscillator (SOSC) pins: SOSCI and SOSCO.

Work around

Use an external clock source (32.768 Hz) applied to the SOSCO pin with the FSOSCEN bit (DEVCFG1<6>) set to '0' (i.e., the SOSC is disabled through the Configuration Word) for a real-time clock base; otherwise, use the internal LPRC for non-precision requirements.

Affected Silicon Revisions

A1						
X						

3. Module: Reset

A system Reset is not generated on a BOR event ($V_{PORIO} < V_{DDIO} < V_{BORIO}$). This will stop system clocks with all the I/O pin functions frozen in the present state until either V_{DDIO} falls to V_{PORIO} or $V_{DDIO} > V_{BORIO}$.

Work around

Reset device using a $\overline{MCLR}$ pin through an external reset supervisor/monitor is shown in Figure 2. Set the SMCLR (DEVCFG2<15>) configuration bit to '0', which makes the $\overline{MCLR}$ to act as a POR Reset instead of a normal system reset.

Table 4 and Table 5 provide a list of external Reset supervisor and regulators with built in Reset supervisors that can be used.

When selecting an external supervisor other than the ones provided in Table 4 and Table 5, the following requirements must be taken into consideration:

- Minimum Reset trip voltage of the external supervisor should be V_{BORIO} (Max)+0.5V.
- The external reset supervisor/LDO output going to $\overline{MCLR}$ should have an open drain output to not interfere with the MPLAB programming/debug tools.

When this work around is implemented, the minimum V_{DDIO} operating voltage of the application needs to be above the reset supervisor maximum trip voltage + 0.2V, where 0.2V compensates for variation in the external reset supervisor voltage.

FIGURE 2:   EXTERNAL RESET CIRCUIT

TABLE 4:   RESET SUPERVISOR/ VOLTAGE MONITOR

Part Number	Reset Trip Voltage	$\overline{MCLR}$ Source
MIC803-26D2VC3	2.63V	Reset pin (Open Drain)

TABLE 5:   LDOs WITH EMBEDDED RESET SUPERVISOR

Part Number	V_IN (Max)	V_OUT	I_OUT	Reset Trip Voltage	$\overline{MCLR}$ Source
MIC5239-3.3YM	30V	3.3V	500 ma	3.3V- 5%	FLG pin (Open Drain)
MIC5239-3.3YMM					
MCP1725-3302E/MC	6V	3.3V	500 ma	3.3V-10%	PWRGD pin (Open Drain)
MCP1727-3302E/MF	6V	3.3V	1500 ma	3.3V-10%	PWRGD pin (Open Drain)

Affected Silicon Revisions

A1							
X							

4. Module: Reset

A BOR event also sets the HVD1V8R bit (RCON<29>).

<u>Work around</u>

True high-voltage detect will set only the HVD1V8R (RCON<29>) bit. This bit should be ignored when it is set along with the BOR (RCON<1>) bit. Also, make sure to clear the HVD1V8R bit on exit from the BOR event, if set.

<u>Affected Silicon Revisions</u>

A1							
X							

5. Module: Power-Saving

Turning off the REFCLK modules through the PMD bits (PMD6<11:8>) causes unpredictable device behavior.

<u>Work around</u>

None. Do not disable the REFCLK modules through the PMD bits.

<u>Affected Silicon Revisions</u>

A1							
X							

6. Module: DMA

Setting the PMD bit for DMA (PMD7<4>) does not disable clocks or DMA peripheral.

<u>Work around</u>

Use the ON bit (DMACON<15>) to enable/disable DMA globally, or use the CHEN bit (DCHxCON<7>) to enable/disable individual channels.

<u>Affected Silicon Revisions</u>

A1							
X							

7. Module: VBAT

The VBAT pin is not functional. Connect the VBAT pin to VDDIO.

<u>Work around</u>

None.

<u>Affected Silicon Revisions</u>

A1							
X							

8. Module: Deep Sleep

Deep-Sleep mode is not functional.

<u>Work around</u>

None.

<u>Affected Silicon Revisions</u>

A1							
X							

9. Module: I^{2}C

Indeterminate I^{2}C module behavior may result when data rates greater than 100 kHz and/or continuous sequential data transfers greater than 500 bytes are used.

The potential false intermittent error signals can result in one of the following error conditions, which are listed in order of decreasing frequency:

- **False Error Condition 1:**
  False Master Bus Collision Detect (Master-mode only) – The error is indicated through the BCL bit (I2CxSTAT<10>).

- **False Error Condition 2:**
  Receive Overflow (Master or Slave modes) – The error is indicated through the I2COV bit (I2CxSTAT<20>).

- **False Error Condition 3:**
  Suspended I^{2}C Module Operations (Master or Slave modes) – I^{2}C transactions in progress are inadvertently suspended without error indications.

> **Note:** All three false errors are recoverable in software.

Work around 1

- **False Error Condition 1:**
  Clear the Master Bus Collision Detect (BCL bit (I2CxSTAT<10>) after the bus returns to an Idle state. The software can monitor the S bit (I2CxSTAT<3>) and the P (I2CxSTAT<4>) bit to wait for an Idle bus. When the software services the bus collision Interrupt Service Routine and the I^{2}C bus is free, the software can resume communication by asserting a new Start condition.

- **False Error Condition 2:**
  Clear the Receive Overflow Status flag I2COV bit (I2CxSTAT<20>), and then resume normal operation.

- **False Error Condition 3:**
  Initialize a Timer to slightly greater than the worst case I^{2}C transaction cycle, (i.e., from Start-to-Stop, including the sum of all other application PC flow latencies, calls, interrupts, etc.). Exact timing is not required, rather just long enough so that a normal transaction is not interrupted. Prior to the beginning of each transaction, start the timer. Be sure to stop and reset the timer after completion of each successful I^{2}C transaction.
  During the Timer interrupt (i.e., the I^{2}C transaction has timed out), disable the I^{2}C module by setting the ON bit (I2CxCON<15>) = 0. After disabling the module, wait 4 instruction cycles, after which time the I2CxSTAT register will automatically be cleared. Re-enable the I^{2}C module by setting the ON bit = 1 and resume normal operation.

Work around 2

Instead of using the hardware I^{2}C module, use a software "bit-bang" implementation.

Affected Silicon Revisions

A1							
X							

10. Module: ADC

The ADC Group Early Interrupt (IRQ 205) feature is not functional.

Work around

Use individual ADC Early Interrupts (IRQ 119 through IRQ 203 and IRQ 206).

Affected Silicon Revisions

A1							
X							

11. Module: ADC

The ADC level trigger will not perform burst conversions in Debug mode.

Work around

Do not use Debug mode with the ADC level trigger.

Affected Silicon Revisions

A1							
X							

12. Module: ADC

In Differential mode, code 3072 has a DNL of +3.

Work around

None.

Affected Silicon Revisions

A1							
X							

13. Module: ADC

Turbo mode is not functional when two channels are linked for the purpose of increasing throughput.

Work around

None.

Affected Silicon Revisions

A1							
X							

14. Module: SDHC

The SDHC module requires the System PLL to be turned ON.

Work around

SPLL should be enabled before using the SD Host Controller (SDHC) module.

Affected Silicon Revisions

A1							
X							

15. Module: SDHC

The SDHC module may not function if the $\overline{\text{SDCD}}$ pin is not used.

Work around 1

Set CDSSEL (SDHCCON1<7>) to '1' and CDTLVL (SDHCCON1<6>) to '0'.

Work around 2

Ensure that the $\overline{\text{SDCD}}$ pin is used and driven to a low state externally.

Affected Silicon Revisions

A1							
X							

16. Module: SDHC

Card-detect status indication through the CDSLVL bit (SDHCSTAT1<18>) is inverted.

Work around 1

Use ACMD42 to detect the card's presence.

Work around 2

If $\overline{\text{SDCD}}$ is used for card detect, add a software work around to invert the CDSLVL (SDHCSTAT1<18>) state.

Affected Silicon Revisions

A1							
X							

17. Module: SDHC

Write-protect status indication through the WPSLVL bit (SDHCSTAT1<19>) is inverted.

Work around

If $\overline{\text{SDWP}}$ is used for Write-protect, add a software work around to invert WPSLVL (SDHCSTAT1<19>) state.

Affected Silicon Revisions

A1						
X						

18. Module: SDHC

The Stop at Block Gap feature of the SDHC module is not functional.

Work around

None.

Affected Silicon Revisions

A1						
X						

19. Module: HLVD

High/Low-Voltage Detect module is not functional.

Work around

None.

Affected Silicon Revisions

A1						
X						

20. Module: DDR2C

DDR2 is functional only between 0°C and 70°C.

Work around

None.

Affected Silicon Revisions

A1						
X						

21. Module: DDR2C

Internal DDRVREF circuit (voltage divider) is not functional.

Work around

Use external voltage divider circuit on the DDRVREF pin to track $V_{DDR1V8}/2$. Make sure to set INTVREFCON<1:0> (CFGMPLL<7:6>) to $0'b00$ before initializing DDR2.

Affected Silicon Revisions

A1						
X						

22. Module: SQI

SQI eXecute-In-Place (XIP) mode is not functional in cached memory space (KSEG2).

Work around

Use KSEG3 (uncached starts at 0xF0000000) address space to access SQI Flash in XIP mode.

Affected Silicon Revisions

A1						
X						

23. Module: USB

USB General Event Interrupt (IRQ 132) is not persistent as expected.

Work around

Handle USB general events in Non-persistent mode.

Affected Silicon Revisions

A1						
X						

24. Module: USB

The USB module does not support remote wake-up through the USBRIE bit (USBCRCON<1>).

Work around

None.

Affected Silicon Revisions

A1						
X						

25. Module: System Bus

The ERRP (SBTxECON<24>) bit is not functional and should not be used.

<u>Work around</u>

None.

<u>Affected Silicon Revisions</u>

A1							
X							

26. Module: Crypto

The Crypto module cannot access data from Flash due to prefetch cache corruption. Both work arounds listed below do not impact CPU performance when L1 cache is used by CPU.

<u>Work around 1</u>

Disable predictive prefetching for all addresses except CPU instructions and data. This can be achieved by NOT setting PREFEN<1:0> (PRECON<5:4>) to `0'b11`.

<u>Work around 2</u>

Set Flash Wait states using the PFMWS<2:0> bits (PRECON<2:0>) to greater than four.

<u>Affected Silicon Revisions</u>

A1							
X							

27. Module: UART

Clearing the receive buffer overrun error through the OERR bit (UxSTA<1>) clears the receive buffer. This condition occurs when the RUNOVF bit (UxMODE<16>) is set, and an overflow condition occurs.

<u>Work around</u>

When a receive buffer overrun error occurs, read the entire receive FIFO through the UxRXREG register before clearing the OERR (UxSTA<1>) bit.

<u>Affected Silicon Revisions</u>

A1							
X							

28. Module: EBI

For Asynchronous NOR Flash, EBI internal clock specification, T_{EBICLK} (EB10) is not met.

<u>Work around</u>

When asynchronous NOR is attached to EBI, the system frequency would have to be reduced to 180 MHz for it to properly function.

<u>Affected Silicon Revisions</u>

A1							
X							

29. Module: CTMU

Edge Sequencing mode (EDGSEQEN (CTMUCON<2>)) and Edge mode are not functional.

<u>Work around</u>

Use level modes.

<u>Affected Silicon Revisions</u>

A1							
X							

30. Module: CTMU

When the TGEN bit is set, manual current sourcing (i.e. setting the EDG1STAT bit) from CTMU is not possible.

<u>Work around</u>

None.

<u>Affected Silicon Revisions</u>

A1							
X							

31. Module: Temperature Sensor

The temperature sensor is not functional.

<u>Work around</u>

None.

<u>Affected Silicon Revisions</u>

A1							
X							

32. Module: ICSP

While programming/debugging the device through any PGECx/PGEDx pair, TDO will toggle.

Work around

None.

Affected Silicon Revisions

A1						
X						

33. Module: PORTS

V_{IH} specification of 0.65 * V_{DDIO} is not met. Use V_{IH} specification of 0.8 * V_{DDIO}.

Work around

None.

Affected Silicon Revisions

A1						
X						

34. Module: Primary Oscillator

The Primary Oscillator (POSC) does not support Automatic Gain Control (AGC). Therefore, the POSCAGC bit (DEVCFG0/ADEVCFG0<27>) is not functional.

Work around

None.

Affected Silicon Revisions

A1						
X						

35. Module: Primary Oscillator

The Primary Oscillator (POSC) does not support Automatic Gain Control (AGC). Therefore, the Primary Oscillator AGC Gain Search Step Settling Time Control bits, POSCAGCDLY<1:0> (DEVCFG0/ADEVCFG0<25:24>), are not functional.

Work around

None.

Affected Silicon Revisions

A1						
X						

36. Module: Primary Oscillator

The Fine Gain Control bits, POSCFGAIN<1:0> (DEVCFG0/ADEVCFG0<23-22>), are not functional.

Work around

None.

Affected Silicon Revisions

A1						
X						

37. Module: GPU

The GPU Run-time enable/disable feature is not functional. Therefore, the GPURESET bit (CFGCON2<0>) is not functional. The GPU is always enabled regardless of the value of the GPURESET bit.

Work around

None.

Affected Silicon Revisions

A1						
X						

38. Module: SDHC

The SDHC write-protect polarity inversion feature is not functional. Therefore, the SDWPPOL bit (CFGCON2<2>) is not functional and should not be used.

Work around

None.

Affected Silicon Revisions

A1						
X						

39. Module: PMP

The PMP Input Buffer 'x' Status Full bit, IB0F (PMSTAT<8>), and the Output Buffer Underflow Status bit, OBUF (PMSTAT<6>), are set as soon as the PMP is turned ON in Slave mode (i.e., PMPTTL bit (PMCON<10>) is equal to '1').

Work around

During PMP slave mode initialization, and before PMP interrupts are enabled, clear the Input Buffer Full Flag (IB0F bit (PMSTAT<8>) and the Output Buffer Underflow Flag (OBUF bit (PMSTAT<6>) when clearing any pending IFSx interrupt flags.

Affected Silicon Revisions

A1							
X							

40. Module: I^{2}C

When the I^{2}C module is in Slave mode, Start and Restart Interrupts are not occurring or properly reflected in the IFSx flag bits.

Work around

Use software polling to test the I^{2}C Start/Restart Status bit, S (I2CxSTAT<3>).

Affected Silicon Revisions

A1							
X							

41. Module: Crypto

The output digest of a partial message cannot be used as the initial vector for continuing the cryptographic operation on the remainder of the message. The full message must be processed in one operation.

Work around

None.

Affected Silicon Revisions

A1							
X							

42. Module: Crypto

The Crypto Engine does not support a Hash operation on an empty string (i.e., string with zero length). The Crypto Engine times out and does not return a valid hash.

Work around

Use the fixed known hash of the empty string.

Affected Silicon Revisions

A1							
X							

43. Module: CTMU

If the ADC module is enabled in Idle mode, it should override the setting of the CTMUSIDL bit (CTMUCON<13>) = 1, (i.e., discontinue CTMU module operation when the device enters Idle mode), and if the ADC module attempts to make a CTMU temperature sensor measurement. However, it cannot because CTMU current sources aren't enabled in Idle mode.

Work around

Set the CTMUSIDL bit to '0' to continue module operation when the device enters Idle mode.

Affected Silicon Revisions

A1							
X							

44. Module: Timer1

In Asynchronous external counter mode, (i.e., TCS bit (T1CON<1> = 1), TSYNC bit (T1CON<2> = 0), and TECS<1:0> (T1CON<9:8> = 'b01)), Timer1 does not reflect the first count from an external T1CLK input.

Work around

None.

Affected Silicon Revisions

A1							
X							

45. Module: Timer1

The Timer1 register (TMR1) in Asynchronous external counter mode, (i.e., TCS bit (T1CON<1> = 1), TSYNC bit (T1CON<2> = 0), and TECS<1:0> (T1CON<9:8> = `0b01`)), remains at the initial set value for five external clock pulses after wake-up from Sleep mode.

Work around

None.

Affected Silicon Revisions

A1							
X							

46. Module: Timer1

Timer1 counts beyond the period value in Asynchronous mode when the period is 0x01.

Work around

Set the Timer1 period, PR1, to a value greater than 1.

Affected Silicon Revisions

A1							
X							

47. Module: Timer1

Timer1 does not work properly in Gated mode (i.e., TGATE bit (T1CON<7> = 1), TCS bit (T1CON<1> = 0) with the prescaler enabled (TCKPS<1:0> bits (T1CON<5:4>) = `0b00`)).

Work around

None.

Affected Silicon Revisions

A1							
X							

48. Module: Timer1

Back-to-back CPU writes to the TMR1 register are not allowed for at least four PBCLK cycles.

Work around

None.

Affected Silicon Revisions

A1							
X							

49. Module: Timer1

The Asynchronous Timer Write Disable bits (TWDIS (TxCON<12>)) and the Asynchronous Timer Write In Progress bits (TWIP (TxCON<11>)) are not functional.

Work around

None.

Affected Silicon Revisions

A1							
X							

50. Module: UART

The UART TX Stop bit duration is shorter than the expected in High-Speed mode (BRGH bit (UxMODE<3>) = 1) for baud rates less than 7.5 Mbps.

Work around

For baud rates less than 7.5 Mbps, operate the UART in Standard-Speed mode, that is, BRGH bit (UxMODE<3> =0). For baud rates greater than 7.5 Mbps operate the UART in High-Speed mode, that is, BRGH bit (UxMODE<3> =1).

Affected Silicon Revisions

A1							
X							

51. Module: Sleep

If the ON bit (PB5DIV<15> = 0), and PBCLK5 is disabled, there is a 3 mA increase in Sleep IPD current.

Work around

Do not disable PBCLK5 before entering Sleep mode.

Affected Silicon Revisions

A1							
X							

52. Module: CFG

Unique ID, DEVSNx<31:0> is not programmed in the devices released earlier than trace code dated 1821xxx.

Work around

None.

Affected Silicon Revisions

A1							
X							

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS60001361**F**):

> **Note:** Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Comparator

In the current device data sheet, the following information was incorrectly stated. The input Common Mode Voltage (VICM) defined in parameter D301 and Common Mode Rejection Ratio (CMRR) in parameter D302 in **Table 44-18 COMPARATOR SPECIFICATIONS** were incorrectly stated.

The correct value is shown in the following table.

DC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature $-40°C \leq T_A \leq +85°C$ for Industrial				
Param. No.	Symbol	Characteristics	Min.	Typ.	Max.	Units	Comments
D301	V_{ICM}	Input Common Mode Voltage	**0.8**	—	**2.37**	V	$AV_{DD} = V_{DDIO}$, $AV_{SS} = V_{SS}$ (Note 2)
D302	CMRR	Common Mode Rejection Ratio	**50**	—	—	dB	Max V_{ICM} = (V_{DDIO} - 1)V (Note 2)

PIC32MZ Graphics (DA) Family

APPENDIX A: REVISION HISTORY

Rev A Document (3/2017)

Initial release of this document, which includes the following silicon issues: 1. (Primary Oscillator), 2. (Secondary Oscillator), 3. (Reset), 4. (Reset), 5. (Power-Saving), 6. (DMA), 7. (V$_{BAT}$), 8. (Deep Sleep), 9. (I^{2}C), 10. (ADC), 11. (ADC), 12. (ADC), 13. (ADC), 14. (SDHC), 15. (SDHC), 16. (SDHC), 17. (SDHC), 18. (SDHC), 19. (HLVD), 20. (DDR2C), 21. (DDR2C), 22. (SQI), 23. (USB), 24. (USB), 25. (System Bus), 26. (Crypto), 27. (UART), 28. (EBI), 29. (CTMU), 30. (CTMU), 31. (Temperature Sensor), 32. (ICSP), 33. (PORTS).

Rev B Document (12/2017)

Silicon issue 25. (System Bus) was updated.

Added silicon issues 34. (Primary Oscillator), 35. (Primary Oscillator), 36. (Primary Oscillator), 37. (GPU), 38. (SDHC), 39. (PMP), 40. (I^{2}C), 41. (Crypto), 42. (Crypto), 43. (CTMU), 44. (Timer1), 45. (Timer1), 46. (Timer1), 47. (Timer1), 48. (Timer1), and 49. (Timer1).

Added data sheet clarifications 1. (), 1. (Comparator), 3. (Device Configuration Word 0 Registers (DEVCFG0/ADEVCFG0)), and 4. (Device Configuration Word 1 Registers (DEVCFG1/ADEVCFG1)).

Rev C Document (9/2018)

Added Silicon Issues 50. (UART), 51. (Sleep), and 52. (CFG).

Removed Previous Data Sheet Clarifications 1, 2, 3, and 4.

Added Data Sheet Clarification 1. (Comparator).

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.

- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.

- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.

- Microchip is willing to work with the customer who is concerned about the integrity of their code.

- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

QUALITY MANAGEMENT SYSTEM

CERTIFIED BY DNV

═ ISO/TS 16949 ═

![Microchip logo]

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://www.microchip.com/
support
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Austin, TX
Tel: 512-257-3370

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Novi, MI
Tel: 248-848-4000

Houston, TX
Tel: 281-894-5983

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453
Tel: 317-536-2380

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608
Tel: 951-273-7800

Raleigh, NC
Tel: 919-844-7510

New York, NY
Tel: 631-435-6000

San Jose, CA
Tel: 408-735-9110
Tel: 408-436-4270

Canada - Toronto
Tel: 905-695-1980
Fax: 905-695-2078

ASIA/PACIFIC

Australia - Sydney
Tel: 61-2-9868-6733

China - Beijing
Tel: 86-10-8569-7000

China - Chengdu
Tel: 86-28-8665-5511

China - Chongqing
Tel: 86-23-8980-9588

China - Dongguan
Tel: 86-769-8702-9880

China - Guangzhou
Tel: 86-20-8755-8029

China - Hangzhou
Tel: 86-571-8792-8115

China - Hong Kong SAR
Tel: 852-2943-5100

China - Nanjing
Tel: 86-25-8473-2460

China - Qingdao
Tel: 86-532-8502-7355

China - Shanghai
Tel: 86-21-3326-8000

China - Shenyang
Tel: 86-24-2334-2829

China - Shenzhen
Tel: 86-755-8864-2200

China - Suzhou
Tel: 86-186-6233-1526

China - Wuhan
Tel: 86-27-5980-5300

China - Xian
Tel: 86-29-8833-7252

China - Xiamen
Tel: 86-592-2388138

China - Zhuhai
Tel: 86-756-3210040

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444

India - New Delhi
Tel: 91-11-4160-8631

India - Pune
Tel: 91-20-4121-0141

Japan - Osaka
Tel: 81-6-6152-7160

Japan - Tokyo
Tel: 81-3-6880- 3770

Korea - Daegu
Tel: 82-53-744-4301

Korea - Seoul
Tel: 82-2-554-7200

Malaysia - Kuala Lumpur
Tel: 60-3-7651-7906

Malaysia - Penang
Tel: 60-4-227-8870

Philippines - Manila
Tel: 63-2-634-9065

Singapore
Tel: 65-6334-8870

Taiwan - Hsin Chu
Tel: 886-3-577-8366

Taiwan - Kaohsiung
Tel: 886-7-213-7830

Taiwan - Taipei
Tel: 886-2-2508-8600

Thailand - Bangkok
Tel: 66-2-694-1351

Vietnam - Ho Chi Minh
Tel: 84-28-5448-2100

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

Finland - Espoo
Tel: 358-9-4520-820

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Garching
Tel: 49-8931-9700

Germany - Haan
Tel: 49-2129-3766400

Germany - Heilbronn
Tel: 49-7131-67-3636

Germany - Karlsruhe
Tel: 49-721-625370

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Germany - Rosenheim
Tel: 49-8031-354-560

Israel - Ra'anana
Tel: 972-9-744-7705

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Italy - Padova
Tel: 39-049-7625286

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Norway - Trondheim
Tel: 47-7289-7561

Poland - Warsaw
Tel: 48-22-3325737

Romania - Bucharest
Tel: 40-21-407-87-50

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

Sweden - Gothenberg
Tel: 46-31-704-60-40

Sweden - Stockholm
Tel: 46-8-5090-4654

UK - Wokingham
Tel: 44-118-921-5800
Fax: 44-118-921-5820