CPS-1848™
PCB Design Application Note

Formal Status
June 22, 2010

6024 Silver Creek Valley Road, San Jose, California 95138
Telephone: (408) 284-8200 • Fax: (408) 284-3572

About this Document

This document is intended for users who are designing systems with the IDT CPS-1848 (80HCPS1848) 2.1 RapidIO switch. The CPS-1848 offers 5 and 6.25 Gbaud lane rates in 1x, 2x, or 4x port configuration. Each S-RIO port is a full duplex, point-to-point interface that uses differential signaling.

A fundamental knowledge of high-speed design techniques is assumed. Details concerning PCB layout and differential impedance design are provided. The critical issues of controlled impedance of traces and connectors, differential routing, termination techniques, and DC balance, must all be considered to get optimal performance from the IC. This application note will help users to get the best possible performance from the IC and ensure first time success in implementing a functional design with exceptional signal quality. It is intended that this document will be used in conjunction with the *CPS-1848 Datasheet*.

Topics discussed include the following:

- Board Material
- Layers Stack-up
- Differential Pair Trace Design
- Via
- S-RIO Receiver DC Blocking Capacitors
- Decoupling Requirement
- Clock Design and Consideration
- High-speed Serial I/O and Layout Guidelines

Document Conventions

Symbols

This symbol indicates important configuration information or suggestions.

This symbol indicates procedures or operating levels that may result in misuse or damage to the device.

Revision History

June 22, 2010, Formal Status

First release of the *CPS-1848 PCB Design Application Note*.

CPS-1848 PCB Design Application Note

Board Material

Printed Circuit Board (PCB) dielectric construction material controls how much noise and cross-talk is contributed from the fast switching I/O signals. This dielectric material can be assigned a dielectric constant, ε r, which affects the impedance of a transmission line, and signals can propagate faster in materials that have a lower ε r.

Proper dielectric material selection enables the PCB designer to minimize the dielectric loss because at frequencies above 1 GHz, dielectric loss is dominant compared to conductor loss. The dielectric loss is dependent on the loss tangent/dissipation factor for a given dielectric material. Smaller loss tangent values offer lower high-frequency attenuation to the high-speed signals. The dielectric constant and the loss tangent information for the various dielectric materials typically used in the PCB design are displayed in Figure 1.

Figure 1: Dielectric Materials Used in PCB Design

Performance	Name	Dielectric Constant (Dk)	Loss Tangent/ Dissipation Factor (Df)	Cost
Low	Standard FR4	4.1 – 4.4	0.019 – 0.024	Low
	Nelco N4000 - 6	4.0	0.022 @ 2.5GHz	
	Isola FR 370 HR	4.04	0.021 @ 2GHz	
Medium	GETEK	3.5	0.010 @ 10GHz	Medium
	Isola FR 408	3.75	0.012 @ 10GHz	
	Nelco 4000 – 13 EP	3.6	0.009 @ 10GHz	
	Nelco 4000 – 13 EPSI	3.2	0.008 @ 10GHz	
High	Rogers RO4350B	3.48	0.0037 @ 10GHz	High
	Arlon 25N	3.38	0.0025 @ 10GHz	

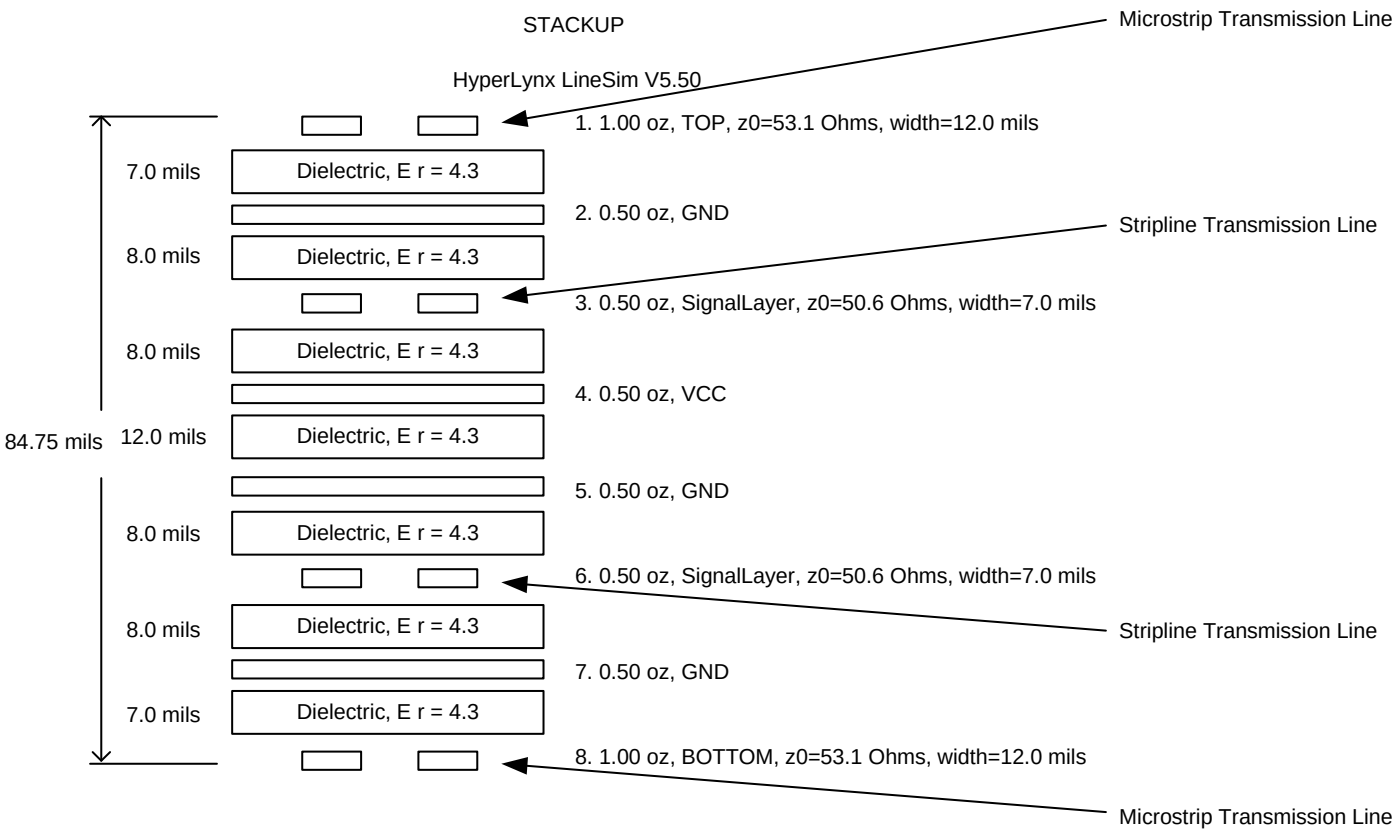
The most widely used dielectric material for PCBs is FR-4, a glass laminate with epoxy resin that meets a wide variety of processing conditions. IDT recommends to work closely with the PCB vendor to design the high-speed channels with the correct impedance and meeting the loss targets.

Layers Stack-up

Multi-layer boards are a must in both daughter board and backplane design. The multiple metal layers facilitate high connection density, minimum crosstalk, and EMI performance. These factors are keys to achieving good signal integrity for all the signal interconnections. When determining a layer stack-up, it is suggested to consider all board layout issues (for example, simultaneous switching output noise (SSN), decoupling, trace layout, vias, etc.). Ideally, all signal layers should be separated from each other by ground or power planes (metal layers). This minimizes crosstalk and provides homogeneous transmission lines, with properly controlled characteristic impedance, between devices and other board components. Best performance is obtained when using dedicated ground and power plane layers that are continuous across the entire board area. When it is not feasible to provide ground or power planes between signal layers, care must be taken to ensure signal line coupling is minimized. Orthogonal routing on adjacent signal layers minimizes coupling and should be used.

The stack-up displayed in Figure 2 demonstrates some parameters that affect the impedance of the board while designing transmission lines. It is shown in the eight-layer stack-up that 12 mils of trace on the top layer will achieve around 53.4 Ohms of impedance when separated by a dielectric of 7 mils from the plane. It is also shown that 7 mil of trace on an internal signal layer will achieve 50.1 Ohms of impedance when separated by 8 mils of dielectric on both sides. These parameters are taken from the Hyperlynx Signal Integrity Line SIM tool. During the design of differential transmission lines, both traces have to be coupled, weakly coupled, or strongly coupled. Coupling will depend on the distance between two traces forming a differential transmission line.

Figure 2: Board Stack-up for Eight Layers



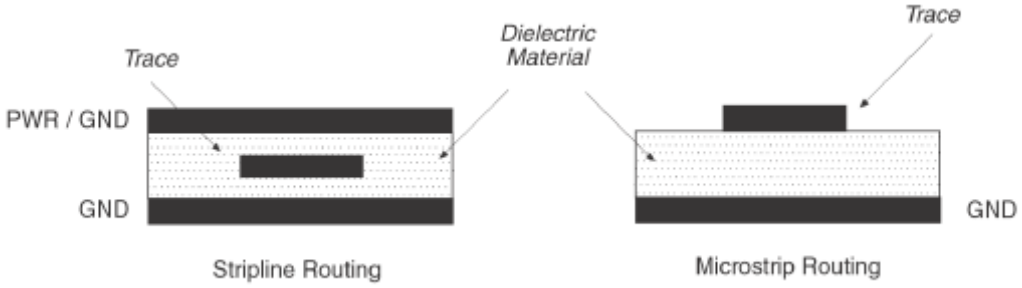
Differential Pair Trace Design

Transmission Line

The high-speed interconnects of S-RIO SerDes are differential signals so these traces should be designed as a differential pair. These signals have very fast rise / fall times in pico seconds, so the interconnects should be treated as transmission lines rather than simple wire connections. The characteristics of transmission lines determine the layout practice. One of the fundamental properties of a transmission line (a mathematical model for a trace on a PCB with power/ground planes) is characteristic impedance, Zo.

Transmission line effect and modeling is another factor to affect signal performance and noise separation. Transmission line is a trace, and has a distributed mixture of resistance (R), inductance (L), capacitance (C) and conductance (G). There are two types of transmission line layouts: Microstrip and Stripline (see Figure 3).

Figure 3: Stripline and Microstrip Signal Routing

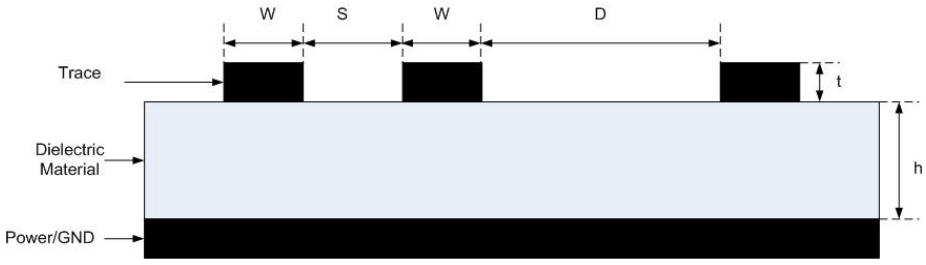


The impedance requirement of the Serial RapidIO interface is *100 Ohms differential*. 100 Ohm characteristic impedance is an industry-standard value for differential signaling. This impedance level is well suited to PCB structures and other components designs where controlled transmission line impedance must be provided. A 100 Ohm differential line can be constructed with two 50 Ohm single-ended lines of equal length.

Microstrip

A differential circuit routed on an outside layer of the PCB with a reference plane below it, constitutes a microstrip layout (see Figure 4). Equations in Figure 5 are used to calculate the impedance of differential microstrip trace pair.

Figure 4: Differential Microstrip Construction



Microstrip Transmission Line Layout

W = Width of trace
t = Thickness of trace
h = Height between trace and reference plane
S = Space between two traces of a differential pair
D = Space between two adjacent differential pairs

Figure 5: Equations for the Differential Microstrip Impedance (in Ohms)

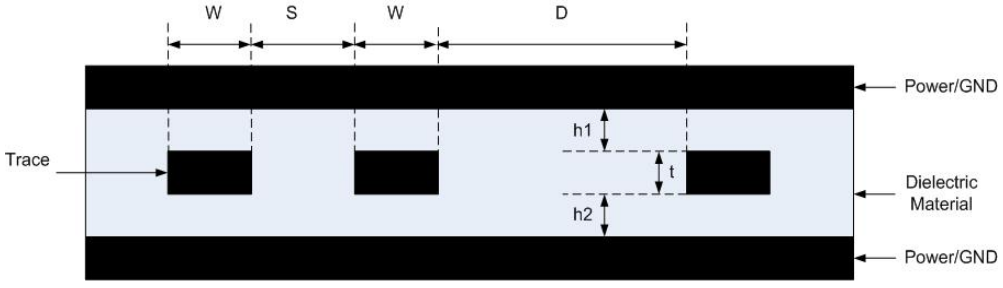
$$Z_o = \frac{60}{\sqrt{0.475\varepsilon_r + 0.67}} \ln\left[\frac{4h}{0.67(0.8w + t)}\right] ohms$$

$$Z_{diff} \cong 2Z_o\left(1 - 0.48e^{-0.96\frac{s}{h}}\right) ohms$$

Stripline

A differential circuit routed on an inside layer of the PCB with two low-voltage reference planes (such as, power and / or GND) constitutes a stripline layout (see Figure 6). Equations in Figure 7 are used to calculate the impedance of a stripline trace pair.

Figure 6: Edge Coupled Differential Stripline Construction



Stripline Transmission Line Layout

W = Width of trace
t = Thickness of trace
S = Space between two traces of a differential pair
D = Space between two adjacent differential pairs

Figure 7: Equations for Differential Stripline Impedance (in Ohms)

$$Zo = \frac{60}{\sqrt{\varepsilon_r}} \times \ln\left(\frac{1.9(2(h1 + h2) + t)}{0.67\,\pi\,(0.8w + t)}\right)$$

$$Zdiff = 2 \times Zo\left(1 - 0.374\; e^{-2.9\left[\frac{s}{h1+h2}\right]}\right)$$

High-speed signal applications perform best with stripline board configurations rather than microstrip configurations. The stripline board configuration provides better protection from crosstalk, and has significantly reduced EMI.

Tracking Topologies

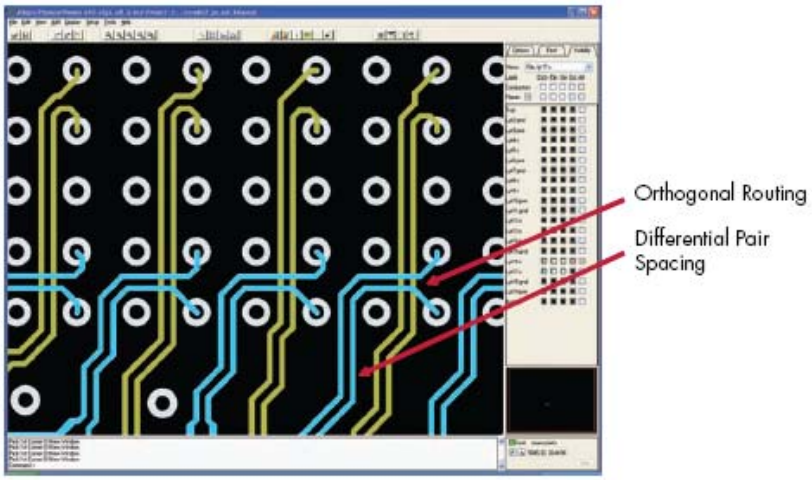
The tracking topologies required to maintain a consistent differential impedance of 100 Ohms to the signal placed on the transmission line are limited to stripline and microstrip types. The designer must decide whether the signaling must be moved to an outer layer of the board using a microstrip topology, or if the signaling can be placed on an inner layer as stripline where shielding by ground and power planes above and below is possible.

- The edge side coupled differential pair geometry, also known as side-to-side, designed for microstrip or stripline configurations are suggested.
  - Edge-coupled microstrip or stripline will allow the thinnest total PCB thickness while optimizing the via stub length
  - High-differential impedance is easily achievable
  - Control length matching and routing through fine pitch holes
- Tight coupling is suggested. It gives higher interconnect density, allows fewer layers, and provides better noise immunity, but requires a certain dielectric thickness for impedance matching. Looser coupling is acceptable if density is not an important driver of a signal layout.
- The two traces should be identical. This means each trace of the differential pair should have the same cross sectional dimensions and must be surrounded by the same type or types of dielectric materials. The spacing between the two traces should also be the same for the entire length of the trace.
- Skew or time delay between the two traces of the differential pair should be zero.
  - In order to prevent consuming received eye margin, +/- track skew of a lane should be constrained to a maximum of 5 mils.
  - Lane-to-lane skew at the input to the receiver must not exceed 11 ns.

- Instead of 90° bends, use mitered 45° bends. Mitered 45° bends reduce reflection on the signal by minimizing impedance discontinuities.
- Do not route pairs on adjacent layers co-parallel in broadside topology. Instead, use orthogonal routing on signal on different layers to avoid crosstalk. Figure 8 shows an example.
- Make sure D (space between two adjacent differential pairs) > 3S (space between two traces of a differential pair) to minimize the crosstalk between the two differential pairs.
- Widen spacing between signal lines as much as routing restrictions will allow. Try not to bring traces closer than three times the dielectric height (S > 3h).

See Figure 4 for the definition for D, S, and h.

Figure 8: Layout Example of How to Avoid Crosstalk



Via

Vias provide two main purposes. One is used for mounting a through-hole component on a PCB. The second is to interconnect traces on different metal layers. Electrically, vias are often modeled as having an inductive and capacitive parasitic value. As more designs move toward high-speed serial links with picoseconds edge rates, any impedance discontinuity in the channel can adversely affect signal quality. One commonly overlooked source of channel discontinuity is the signal via. Vias can add jitter and reduce eye openings that can cause data misinterpretation by the receiver.

Via Construction and Lumped pi Model

Figure 9 shows via construction. Vias can appear as capacitive and/or inductive discontinuities. These capacitive and inductive parasitics contribute to the degradation of the signal as it passes through the vias. Figure 10 shows a simple lumped LC pi model to illustrate via capacitance and inductance effects. Although this model is applicable only if the delay through the via is less than 1/10th of the signal rise time, it is still useful to understand its capacitance and inductance effects.

Figure 9: Via Construction

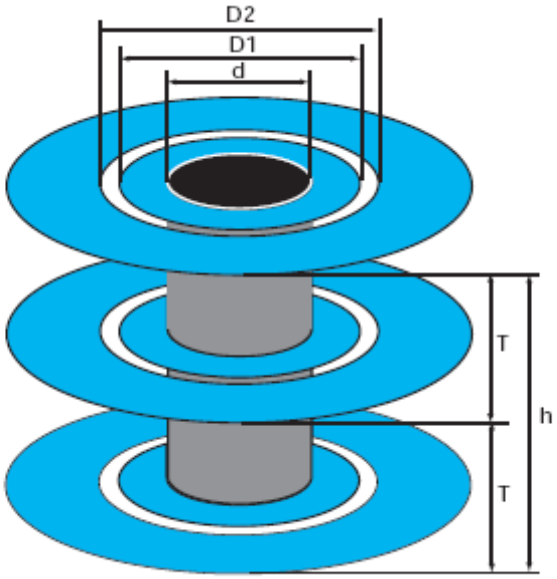


Figure 10: Lumped pi Model of a Via

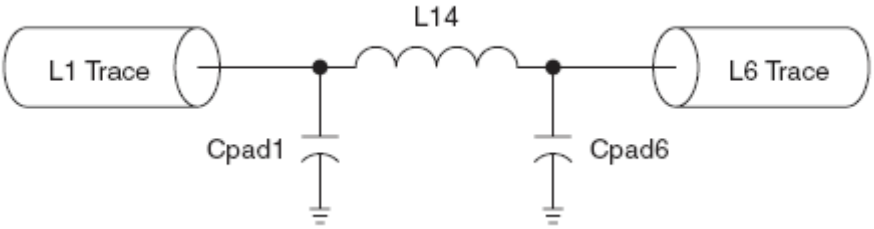


Figure 1 shows the empirical formula for capacitance and inductance of vias when vias are modeled as a lumped LC pi model. Here ε_r is the relative dielectric constant, D1 is the diameter of the via pad, D2 is the diameter of the anti-pad, T is the thickness of the PCB, h is the via length, and d is the via barrel diameter.

Figure 11: Capacitance and Inductance Equations of Via

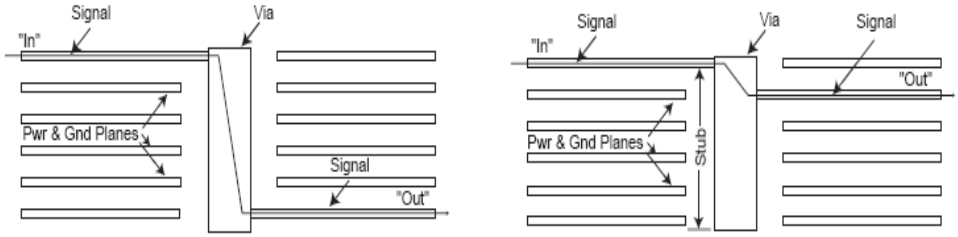
$$Cvia \approx \frac{1.41\varepsilon_r D_1 T}{D_2 - D_1}\text{pF}$$

$$Lvia \approx 5.08h\left[\ln\left(\frac{4h}{d}\right) + 1\right]\text{nH}$$

Via capacitance can be minimized by making the capacitance of via pad small and increasing the diameter of via anti-pad. Similarly, minimizing the length of via barrel and placing a return via close to the signal via will reduce the via loop inductance.

Two cases are shown in Figure 12*:* signal through a via and signal across a via. A through via (without any stub) is recommended wherever necessary because the stub offers a capacitive discontinuity to any high-speed signal.

Figure 12: Signal Through a Via and Signal Across a Via



Signal Through a Via Signal Across a Via

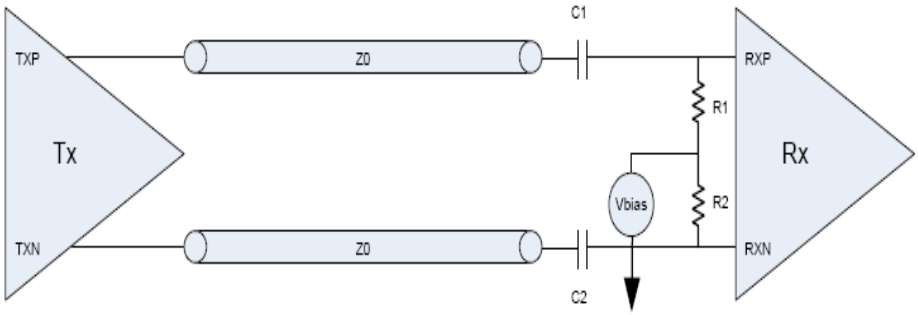
General Rules for Differential Vias

- Keep vias in the signal path to a minimum.
- When routing vias, try to ensure that the vias do not carry any stub especially for high-speed signals.
- The use of buried and blind vias is recommended because in both cases the signal travels through via without any stub.
- Remove all non-functional pads (NFPs).
- Increase vias anti-pad diameter (clearance hole).
- If stubs cannot be avoided, they can be removed by back-drilling or counter-boring the backside of the PCB with a slightly oversized drill bit to remove the parasitic stub. This method demands a cost premium over using standard vias because it requires an additional step in manufacturing the PCB.
- Add adjacent ground vias next to each signal via to provide a better AC return path.
- Place vias adjacent to the capacitor pad. Use wide, short traces between the via and capacitor pads.

S-RIO Receiver DC Blocking Capacitors

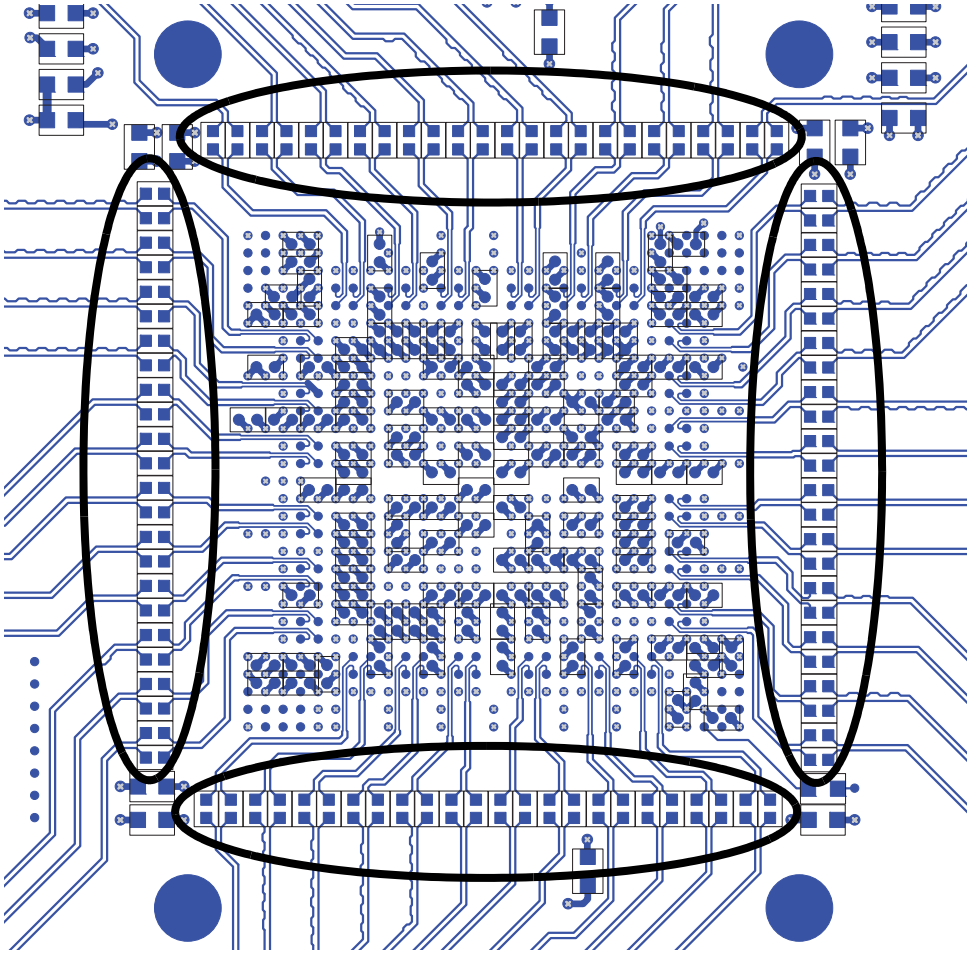
The RapidIO high-speed serial lines are differential CML output voltage swings, and are designed to be AC-coupled. The high-speed serial connections are displayed in Figure 13.

Figure 13: AC-Coupled Differential Interconnect



An inline capacitor C1 and C2 at each input of the receiver provides AC coupling and a DC-block. Thus, any DC bias differential between the two devices on the link is negated. (Note that VBIAS is the internal bias voltage of the device's receiver. R1 and R2 are 50 Ohms each. They are already embedded in the IDT switch). IDT recommends a capacitor value of 0.1uF ceramic in 0402 size (or smaller size). Place the AC coupling capacitors symmetrically placed near the receiver of the device or connector to minimize discontinuity effects (see Figure 14). Do not place the capacitors along the signal trace at a (λ/4) increment from the driver in order to avoid standing wave effects. The *RapidIO Specification (Rev. 2.1)* allows the optional DC coupling for the Level II (5 and 6.25 Gaud) link; however, the CPS-1848 does not support this and only supports AC coupling.

Figure 14: RX Trace Capacitors Placement



Power Distribution

A system can distribute power throughout the PCB with either power planes or a power bus network. Because the power plane covers the full area of the PCB, its DC resistance is very low. The power plane maintains VDD and distributes it equally to all devices while providing very high current-sink capability, noise protection, and shielding for the logic signals on the PCB. IDT recommends using low impedance supply planes to distribute power.

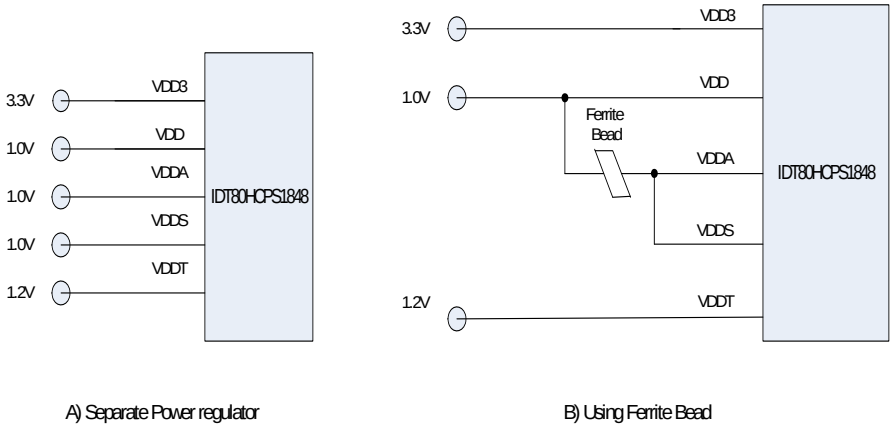
Good layout and bypass techniques to filter the IC's power supply have a significant impact on signal quality. The power distribution impacts system noise. The power supply noise is of major concern as it will couple into the PLL circuits of the transceivers, thereby increasing jitter generation in the transmitter and reducing jitter tolerance in the receiver. The CPS-1848 is a high-speed switch with both digital and analog components in its design. The correct treatment of the power rails, plane assignments, and decoupling, is important to maximize the device's performance. The largest indicator of poor performance on the S-RIO interfaces is the presence of jitter. The die, I/O, and package designs are optimized to provide jitter performance exceeding the limits required by the *RapidIO Specification (Rev. 2.1)*. The guidelines provided below will assist the user in achieving a board layout that will provide the best performance possible.

The CPS-1848 has the following types of power supply pins:

- VDD3 (3.3V) – Digital interface power
- VDD (1.0V) – Digital core power
- VDDA (1.0V) – Analog power

- VDDS (1.0V) – Analog power for SerDes and RX pairs
- VDDT (1.2V) – Analog power for TX pairs

Figure 15: Board Power Supply Diagram



- It is suggested all voltage can be derived from separate voltage regulators.
- VDD, VDDA, VDDS can be derived from the same voltage source with appropriate bypass capacitors and a ferrite bead. A ferrite bead can be used to attenuate the power noise and improve the analog circuit performance in a noisy environment. IDT recommends a Ferrite bead with 4 Amp current, impedance of 50–120 Ohm at 100 MHz and low DC resistance.

Decoupling Requirement

Proper decoupling is critical in high-speed board designs. Select the right decoupling capacitors, power and ground plane stack-up, and voltage regulators, to minimize noise. With the right combination of power and GND planes, decoupling capacitors and voltage-regulator modules will provide decoupling over all frequencies.

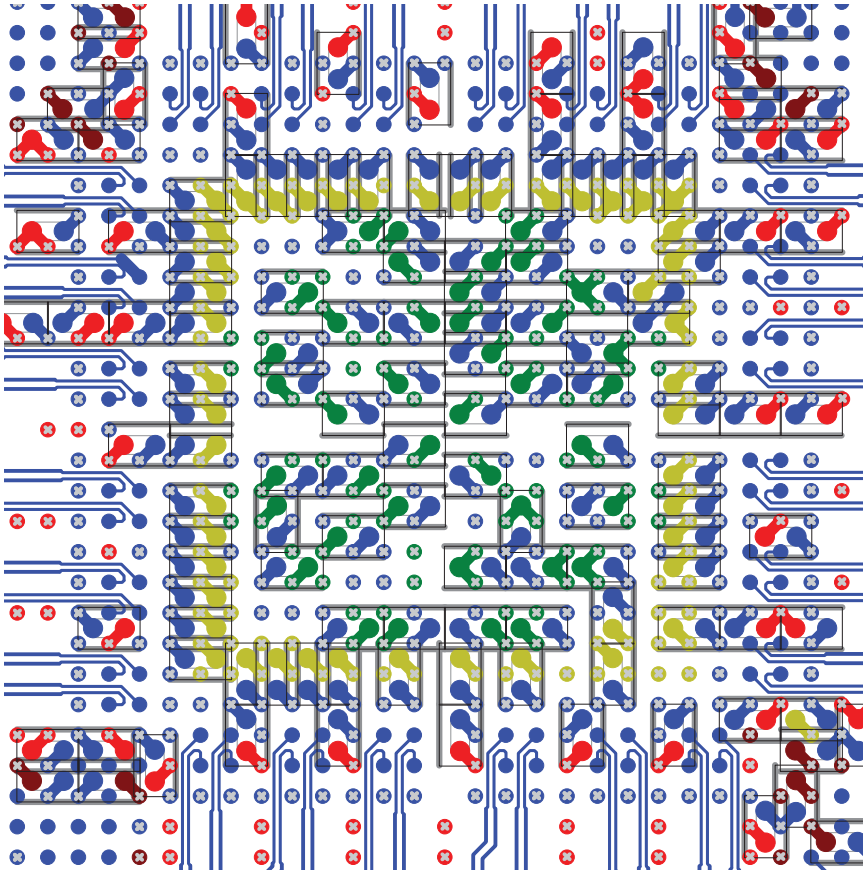
Table 1 shows the decoupling strategy used on the CPS-1848 evaluation board. The capacitors should be selected with the smallest surface mount body that the applied voltage permits in order to minimize the body inductance. IDT recommends ceramic X7R type (0402 or smaller size) for all of the values listed. The larger value capacitors should be low ESR type and placed to the power supply.

Table 1: CPS-1848 Decoupling

Voltage	Usage	Acronym	0.01uF	0.1uF	1uF	10uF	Bulk
3.3V	I/O Power	VDD3	-	10	-	4	~ 300uF
1.0V	Digital Core power	VDD	8	40	-	8	~ 300uF
1.0V	Analog Power	VDDA	24	24	-	12	
1.0V	Analog power for SerDes and Rx pair	VDDS					
1.2V	Analog Power for Tx pairs	VDDT	40	-	8	4	~ 47uF

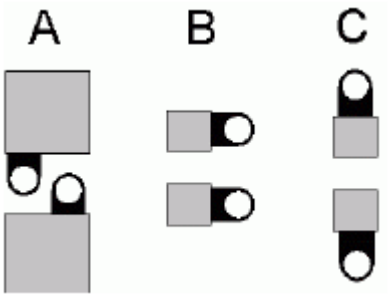
To optimize the effectiveness of decoupling capacitors, surface-mounted capacitors mounted on the bottom side of the PCB keep the parasitic effects to a minimum. Placing capacitors directly underneath the BGA package will improve the high frequency response of very small value capacitors. Figure 16 shows an example of decoupling capacitors placed under the BGA, within the breakout vias.

Figure 16: Proposed Capacitor Placement under CPS-1848



It is suggested to use separate vias for each capacitor and via sharing should be minimized in board design for IDT S-RIO switches. Breakout vias for the decoupling capacitors should be kept as close together as possible. The trace connecting the pad to the via should also be kept as short as possible with a maximum length of 50 mils. Figure 17 shows three recommended designs for decoupling capacitor pads.

Figure 17: Recommended Decoupling Capacitor Pad Designs

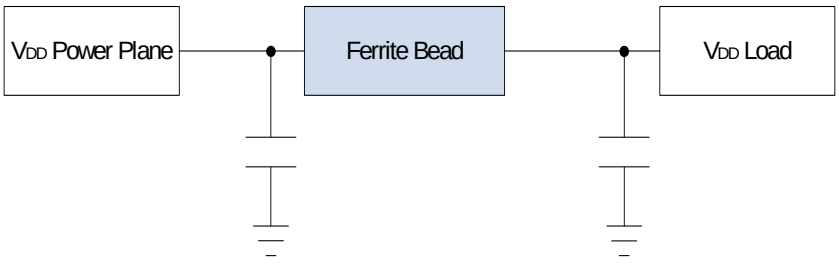


IDT recommends adhering to the following design guidelines to reduce ground bounce:

- Use a bigger via size to connect the capacitor pad to the power and ground plane to minimize the inductance in decoupling capacitors.
- Place the power and ground via as close to each other as possible to increase the mutual inductive coupling between them.
- Traces stretching from power pins to a power plane (or island, or a decoupling capacitor) must be as wide and as short as possible.

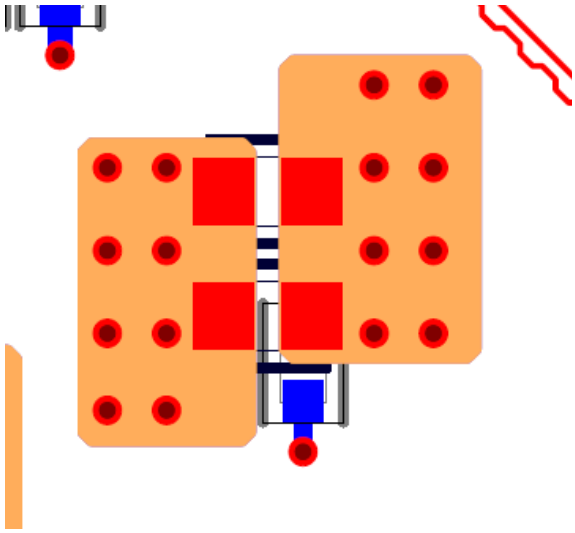
To filter power supply on VDDA/VDDS power planes, use a non-resonant, surface-mount ferrite bead large enough to handle the current in series with the power supply. Elements on the PCB usually add high-frequency noise to the power plane. Place a 10 to 100 uF bypass capacitor next to the ferrite bead. The ferrite bead acts as a short for high-frequency noise coming from the VDD plane. Any low frequency noise is filtered by a large 10uF capacitor after the ferrite bead. Figure 18 is an example of a power noise filter.

Figure 18: Power Noise Filtering Example



Use local copper planes and several vias as per Figure 19 to connect the VDD plane to VDDA/VDDS planes.

Figure 19: Ferrite Connection to Power Planes



Clock Design and Consideration

One of the most common problems in high-speed serial-I/O applications is underestimating the importance of clock jitter. The clock input provides the reference clock (REF_CLK) for the internal PLL, which is multiplied to generate the baud rate clock. Therefore, it is critical that the reference clock be as low-jitter as possible in order to prevent a multiplication of the jitter introduced into the PLL and its baud rate clock. The internal PLL of the S-RIO switch is susceptible to reference clock jitter in the 1 to 20 MHz bandwidth range. Care must be taken to select a PLL-based clock synthesizer, clock oscillator, or system clock, that generates lower phase-jitter than the specified 2 ps RMS in the 1 to 20 MHz range.

Secondly, the clock source must support a frequency accuracy of better than 100 ppm on the REF_CLK input (for 156.25 MHz, this corresponds to +/-15.625 kHz). The accuracy requirement is a S-RIO system-level specification. The total accuracy of a crystal or oscillator clock source is a combination of initial accuracy, aging (frequency drift over time) and temperature stability (frequency drift as a function of the ambient temperature). The 100 ppm S-RIO clock requirement can be met using clock synthesizers with crystal or oscillator sources supporting a total accuracy of 100 ppm or better. Clock synthesizers typically use integer-N feedback PLLs for frequency multiplication and don't add any ppm deviation to the clock signal. Fractional-feedback PLLs add small frequency deviation in the range of 1 ppm or lower. This deviation is often negligible with respect to the crystal-induced frequency deviation.

Suitable clock synthesizer devices with the required low-jitter and zero-ppm deviation characteristics are available as standard products. For example, the IDT FemtoClock™ and FemtoClock™ NG devices offer phase jitter of less than 1.0 ps RMS and less than 0.5 ps RMS, respectively.

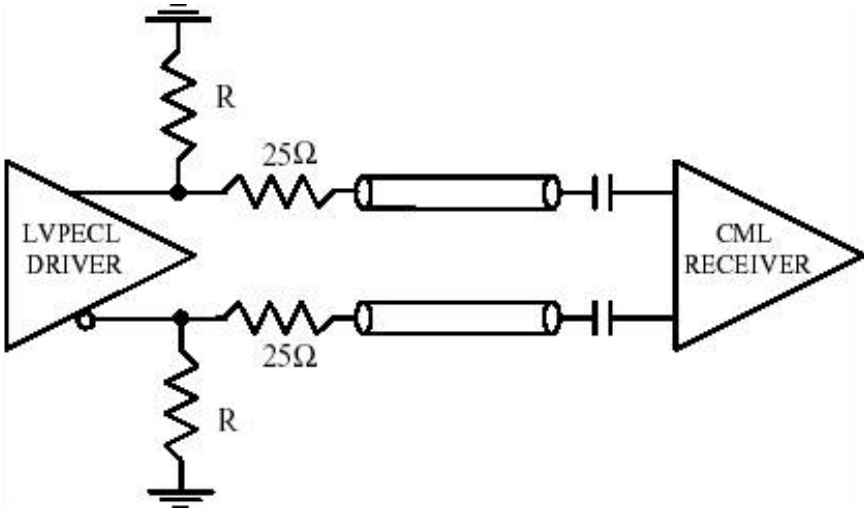
The recommended scheme is to provide the reference clock from a 156.25 MHz clock synthesizer or clock oscillator with the required low-phase noise characteristics. If the clock inputs of several S-RIO switches must be synchronously driven by the same clock source, the use of an integrated synthesizer with fanout or a separate synthesizer and low-skew fanout buffer combination is recommended. The buffer outputs provide separate but synchronous clock signals that are connected by traces of equal length to each load. An integrated synthesizer and buffer device is the most effective solution solving signal integrity and phase jitter design problems.

The power to the clock synthesizer/buffer should be isolated from the digital power plane (for more information, see the clock synthesizer specification). As a minimum, the clock and digital power planes should be decoupled with the use of a ferrite bead/bypass capacitor combination. An adequate decoupling should also be provided for the buffer to filter the power supply noise. The clock signals must be terminated according to the clock output specifications. Correct output termination minimizes reflections and reduces EMI. AC termination is required for the S-RIO reference clock input.

The IDT S-RIO switch reference clock is a CML based differential input. Many clock chips are LVPECL or LVDS based differential outputs. The clock reference must be terminated correctly. Figure 20 shows how to use the AC coupling with LVPECL to CML receiver, and Figure 21 shows how to use the AC coupling with LVDS to CML receiver.

LVPECL to CML Termination

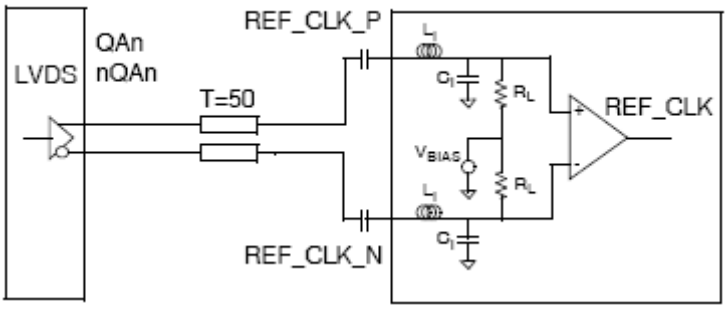
Figure 20: LVPECL to CML Signal Termination



- AC coupling and a 0.1uF ceramic capacitor in 0402 size is suggested.
- Two pull-down resistors are required to dissipate the LVPECL output emitter current (the value can be 142–200 Ohm).
- The 25-Ohm serial resistor is optional when the LVPECL Swing is beyond the CML accepted.
- Place resistors near the transmitter side and place decoupling capacitors near the receiver.
- If possible do not use via in clock transmission lines, and shorten the signal length.

LVDS to CML Termination

Figure 21: LVDS to CML Signal Termination



Recommended Clock Chip Solution

IDT recommends using the ICS841N254i clock synthesizer chip to generate the reference clock for the IDT80HCPS1848 S-RIO switch. For more information, see the *ICS841N254i Datasheet*.

High-speed Serial I/O and Layout Guidelines

Proper PCB layout is important in order to minimize parasitic capacitance and inductance. When implementing a high-speed serial communications link, the importance of layout cannot be overstressed. However, the following simple-to-use guidelines will increase the chance of success and prove easier than most designers anticipate.

- A solid ground plane and power plane are useful in distributing clean power and providing buried capacitance with no inductance, which is essential for the high-speed designs.
- The PCB design should use a controlled impedance process for the high-speed SerDes signals. The high-speed signal traces should be designed for desired differential impedance. The design engineer should work closely with the fabrication house to obtain the desired impedance and PCB thickness.
- Keep traces as short as possible. Initial component placement must be carefully considered. Eliminate all stubs.
- For the receiver, the trace from the BGA pad to the capacitor pad must be on the top layer. On the other side of the capacitor, a via to another layer is permitted.
- The trace widths and separation should be altered based on the board stack-up to meet the 100-Ohm differential impedance requirement.
- A 0402 or smaller size, 0.1 uf capacitor is recommended for AC coupling of the data lines.
- While routing the differential pairs, keep the trace length identical between the two traces.
- Reduce, if not eliminate, the number of vias to minimize impedance discontinuities. Keep vias away from traces by three times the trace width as a minimum.
- Keep high-speed signal traces far from other signals that might capacitively couple noise into the signals. A good rule is that “far” means tens times the width of the trace.
- Do not route the digital signals from other circuits across the area of the transmitter and receiver.

IDT strongly recommends modeling the high-speed channel and to simulate with available HSPICE and IBIS models of IDT devices before committing to PCB design. The HSPICE model is provided for simulating high-speed signals, whereas the IBIS model is used for the slower speed signals. The IDT Applications team is also available to assist with simulation and to review the board schematic in order to achieve first-time success with the PCB design. For additional information or support of these models, please contact IDT Applications team.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

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