DATA HANDBOOK

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Memories MOS, TTL, and ECL

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Philips Components

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MEMORIES MOS, TTL, ECL

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N82S212A N	2304-bit TTL Bipolar RAM (256 x 9) 35 ns	331
N82S212 A	2304-bit TTL Bipolar RAM (256 x 9) 45 ns	331
N82S212 N	2304-bit TTL Bipolar RAM (256 x 9) 45 ns	331
PCA8582BP	256 x 8-bit static EEPROM with I^2C-bus interface for automotive applications	139
PCA8582BT	256 x 8-bit static EEPROM with I^2C-bus interface for automotive applications	139
PCD5101P	256 x 4-bit static RAM	93
PCD5101T	256 x 4-bit static RAM	93
PCD5114P	1024 x 4-bit static RAM	101
PCD5114T	1024 x 4-bit static RAM	101
PCF8570P	256 x 8-bit static RAM with I^2C-bus interface	109
PCF8570T	256 x 8-bit static RAM with I^2C-bus interface	109
PCF8570CP	256 x 8-bit static RAM with I^2C-bus interface	109
PCF8570CT	256 x 8-bit static RAM with I^2C-bus interface	109
PCF8571P	128 x 8-bit static RAM with I^2C-bus interface	109
PCF8571T	128 x 8-bit static RAM with I^2C-bus interface	109
PCF8581P	128 x 8-bit EEPROM with I^2C-bus interface	151
PCF8581T	128 x 8-bit EEPROM with I^2C-bus interface	151
PCF8581CP	128 x 8-bit EEPROM with I^2C-bus interface	151
PCF8581CT	128 x 8-bit EEPROM with I^2C-bus interface	151

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PCF8582AP	256 x 8-bit static CMOS EEPROM with I²C-bus interface	161
PCF8582AT	256 x 8-bit static CMOS EEPROM with I²C-bus interface	161
PCF8582CP	256 x 8-bit static EEPROM with I²C-bus interface for automotive applications	171
PCF8582CT	256 x 8-bit static EEPROM with I²C-bus interface for automotive applications	171
PCF8583P	256 x 8-bit static RAM with I²C-bus interface	119
PCF8583T	256 x 8-bit static RAM with I²C-bus interface	119
10P016 F	16 384-bit ECL Bipolar PROM (4096 x 4) 10 ns	529
100P016 F	16 384-bit ECL Bipolar PROM (4096 x 4) 10 ns	533
10P256 F	256-bit ECL Bipolar PROM (32 x 8) 3 ns	495
100P256 F	256-bit ECL Bipolar PROM (32 x 8) 3 ns	499
10149B F	1024-bit ECL Bipolar PROM (256 x 4) 5 ns	519
10149 F	1024-bit ECL Bipolar PROM (256 x 4) 20 ns	503
100149B F	1024-bit ECL Bipolar PROM (256 x 4) 5 ns	523
100149 F	1024-bit ECL Bipolar PROM (256 x 4) 20 ns	507
10149A F	1024-bit ECL Bipolar PROM (256 x 4) 10 ns	511
100149A F	1024-bit ECL Bipolar PROM (256 x 4) 10 ns	515
27C64AI15 FA	64K-bit CMOS EPROM (8K x 8) 150 ns	185
27C64AI20 FA	64K-bit CMOS EPROM (8K x 8) 200 ns	185
27C64AI15 N	64K-bit CMOS EPROM (8K x 8) 150 ns	185
27C64AI20 N	64K-bit CMOS EPROM (8K x 8) 200 ns	185
27C64AI15 A	64K-bit CMOS EPROM (8K x 8) 150 ns	185
27C64AI20 A	64K-bit CMOS EPROM (8K x 8) 200 ns	185
27C64A-10 N	64K-bit CMOS EPROM (8K x 8) 100 ns	189
27C64A-10 A	64K-bit CMOS EPROM (8K x 8) 100 ns	189
27C64A-12 N	64K-bit CMOS EPROM (8K x 8) 120 ns	193
27C64A-15 N	64K-bit CMOS EPROM (8K x 8) 150 ns	193
27C64A-12 A	64K-bit CMOS EPROM (8K x 8) 120 ns	193
27C64A-15 A	64K-bit CMOS EPROM (8K x 8) 150 ns	193
27C64A-20 N	64K-bit CMOS EPROM (8K x 8) 200 ns	197
27C64A-20 A	64K-bit CMOS EPROM (8K x 8) 200 ns	197
27C64A-10 FA	64K-bit erasable CMOS EPROM (8K x 8) 100 ns	201
27C64A-12 FA	64K-bit erasable CMOS EPROM (8K x 8) 120 ns	205
27C64A-15 FA	64K-bit erasable CMOS EPROM (8K x 8) 150 ns	205
27C64A-20 FA	64K-bit erasable CMOS EPROM (8K x 8) 200 ns	209
27C210-15 N	1M programmable EPROM (64K x 16) 150 ns	273
27C210-20 N	1M programmable EPROM (64K x 16) 200 ns	273
27C210-15 A	1M programmable EPROM (64K x 16) 150 ns	273
27C210-20 A	1M programmable EPROM (64K x 16) 200 ns	273
27C210-15 FA	1M erasable CMOS EPROM (64K x 16) 150 ns	277
27C210-20 FA	1M erasable CMOS EPROM (64K x 16) 200 ns	277
27C256I15 FA	256K-bit EPROM (32K x 8) 150 ns	233
27C256I20 FA	256K-bit EPROM (32K x 8) 200 ns	233
27C256I15 N	256K-bit EPROM (32K x 8) 150 ns	233
27C256I20 N	256K-bit EPROM (32K x 8) 200 ns	233
27C256I15 A	256K-bit EPROM (32K x 8) 150 ns	233
27C256I20 A	256K-bit EPROM (32K x 8) 200 ns	233

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27C256-12 N	256K-bit EPROM (32K x 8) 120 ns	237
27C256-12 A	256K-bit EPROM (32K x 8) 120 ns	237
27C256-15 N	256K-bit EPROM (32K x 8) 150 ns	241
27C256-17 N	256K-bit EPROM (32K x 8) 170 ns	241
27C256-15 A	256K-bit EPROM (32K x 8) 150 ns	241
27C256-17 A	256K-bit EPROM (32K x 8) 170 ns	241
27C256-20 N	256K-bit EPROM (32K x 8) 200 ns	245
27C256-20 A	256K-bit EPROM (32K x 8) 200 ns	245
27C256-12 FA	256K-bit erasable EPROM (32K x 8) 120 ns	249
27C256-15 FA	256K-bit erasable EPROM (32K x 8) 150 ns	253
27C256-17 FA	256K-bit erasable EPROM (32K x 8) 170 ns	253
27C256-20 FA	256K-bit erasable EPROM (32K x 8) 200 ns	257
27C512-15 N	512K-bit CMOS EPROM (64K x 8) 150 ns	263
27C512-17 N	512K-bit CMOS EPROM (64K x 8) 170 ns	263
27C512-20 N	512K-bit CMOS EPROM (64K x 8) 200 ns	263
27C512-15 A	512K-bit CMOS EPROM (64K x 8) 150 ns	263
27C512-17 A	512K-bit CMOS EPROM (64K x 8) 170 ns	263
27C512-20 A	512K-bit CMOS EPROM (64K x 8) 200 ns	263
27C512-15 FA	512K-bit erasable CMOS EPROM (64K x 8) 150 ns	267
27C512-17 FA	512K-bit erasable CMOS EPROM (64K x 8) 170 ns	267
27C512-20 FA	512K-bit erasable CMOS EPROM (64K x 8) 200 ns	267
27HC128-45 N	128K-bit CMOS EPROM (16K x 8) 45 ns	223
27HC128-55 N	128K-bit CMOS EPROM (16K x 8) 55 ns	223
27HC128-45 A	128K-bit CMOS EPROM (16K x 8) 45 ns	223
27HC128-55 A	128K-bit CMOS EPROM (16K x 8) 55 ns	223
27HC128-45 FA	128K-bit erasable CMOS EPROM (16K x 8) 45 ns	227
27HC128-55 FA	128K-bit erasable CMOS EPROM (16K x 8) 55 ns	227
27HC641-45 N	64K-bit CMOS EPROM (8K x 8) 45 ns	213
27HC641-55 N	64K-bit CMOS EPROM (8K x 8) 55 ns	213
27HC641-45 A	64K-bit CMOS EPROM (8K x 8) 45 ns	213
27HC641-55 A	64K-bit CMOS EPROM (8K x 8) 55 ns	213
27HC641-35 FA	64K-bit erasable CMOS EPROM (8K x 8) 35 ns	217
27HC641-45 FA	64K-bit erasable CMOS EPROM (8K x 8) 45 ns	217
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PRO ELECTRON TYPE DESIGNATION CODE FOR INTEGRATED CIRCUITS

This type nomenclature applies to semiconductor monolithic, semiconductor multi-chip, thin-film, thick-film and hybrid integrated circuits.

A basic number consists of:

THREE LETTERS FOLLOWED BY A SERIAL NUMBER

FIRST AND SECOND LETTER

1. DIGITAL FAMILY CIRCUITS

   The FIRST TWO LETTERS identify the FAMILY (see note 1).

2. SOLITARY CIRCUITS

   The FIRST LETTER divides the solitary circuits into:

   S : Solitary digital circuits
   T : Analogue circuits
   U : Mixed analogue/digital circuits

   The SECOND LETTER is a serial letter without any further significance except 'H' which stands for hybrid circuits.

3. MICROPROCESSORS

   The FIRST TWO LETTERS identify microprocessors and correlated circuits as follows:

   MA : { Microcomputer / Central processing unit }
   MB : Slice processor (see note 2)
   MD : Correlated memories
   ME : Other correlated circuits (interface, clock, peripheral controller, etc.)

4. CHARGE-TRANSFER DEVICES AND SWITCHED CAPACITORS

   The FIRST TWO LETTERS identify the following:

   NH : Hybrid circuits
   NL : Logic circuits
   NM : Memories
   NS : Analogue signal processing, using switched capacitors
   NT : Analogue signal processing, using CTDs
   NX : Imaging devices
   NY : Other correlated circuits

Notes

1. A logic family is an assembly of digital circuits designed to be interconnected and defined by its basic electrical characteristics (such as: supply voltage, power consumption, propagation delay, noise immunity).
2. By 'slice processor' is meant: a functional slice of microprocessor.

THIRD LETTER

It indicates the operating ambient temperature range.
The letters A to G give information about the temperature:

A : temperature range not specified
B : 0 to + 70 °C
C : −55 to + 125 °C
D : −25 to + 70 °C
E : −25 to + 85 °C
F : −40 to + 85 °C
G : −55 to + 85 °C

If a circuit is published for another temperature range, the letter indicating a narrower temperature range may be used or the letter 'A'.

Example: the range 0 to + 75 °C can be indicated by 'B' or 'A'.

SERIAL NUMBER

This may be either a 4-digit number assigned by Pro Electron, or the serial number (which may be a combination of figures and letters) of an existing company type designation of the manufacturer.

To the basic type number may be added:

A VERSION LETTER

Indicates a minor variant of the basic type or the package. Except for 'Z', which means customized wiring, the letter has no fixed meaning. The following letters are recommended for package variants:

C : for cylindrical
D : for ceramic DIL
F : for flat pack
L : for chip on tape
P : for plastic DIL
Q : for QIL
T : for miniature plastic (mini-pack)
U : for uncased chip

Alternatively a TWO LETTER SUFFIX may be used instead of a single package version letter, if the manufacturer (sponsor) wishes to give more information.

FIRST LETTER: General shape

C : Cylindrical
D : Dual-in-line (DIL)
E : Power DIL (with external heatsink)
F : Flat (leads on 2 sides)
G : Flat (leads on 4 sides)
K : Diamond (TO-3 family)
M : Multiple-in-line (except Dual-, Triple-, Quadruple-in-line)
Q : Quadruple-in-line (QIL)
R : Power QIL (with external heatsink)
S : Single-in-line
T : Triple-in-line

SECOND LETTER: Material

C : Metal-ceramic
G : Glass-ceramic (cerdip)
M : Metal
P : Plastic

A hyphen precedes the suffix to avoid confusion with a version letter.

RATING SYSTEMS

The rating systems described are those recommended by the International Electrotechnical Commission (IEC) in its Publication 134.

DEFINITIONS OF TERMS USED

Electronic device. An electronic tube or valve, transistor or other semiconductor device.

Note
This definition excludes inductors, capacitors, resistors and similar components.

Characteristic. A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic, or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

Bogey electronic device. An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics which are directly related to the application.

Rating. A value which establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms.

Note
Limiting conditions may be either maxima or minima.

Rating system. The set of principles upon which ratings are established and which determine their interpretation.

Note
The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

ABSOLUTE MAXIMUM RATING SYSTEM

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout life, no absolute maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

DESIGN MAXIMUM RATING SYSTEM

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout life, no design maximum value for the intended service is exceeded with a bogey device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

DESIGN CENTRE RATING SYSTEM

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

HANDLING MOS DEVICES

Though all our MOS integrated circuits incorporate protection against electrostatic discharges, they can nevertheless be damaged by accidental over-voltages. In storing and handling them, the following precautions are recommended.

Caution

Testing or handling and mounting call for special attention to personal safety. Personnel handling MOS devices should normally be connected to ground via a resistor.

Storage and transport

Store and transport the circuits in their original packing. Alternatively, use may be made of a conductive material or special IC carrier that either short-circuits all leads or insulates them from external contact.

Testing or handling

Work on a conductive surface (e.g. metal table top) when testing the circuits or transferring them from one carrier to another. Electrically connect the person doing the testing or handling to the conductive surface, for example by a metal bracelet and a conductive cord or chain. Connect all testing and handling equipment to the same surface.
Signals should not be applied to the inputs while the device power supply is off. All unused input leads should be connected to either the supply voltage or ground.

Mounting

Mount MOS integrated circuits on printed circuit boards *after* all other components have been mounted. Take care that the circuits themselves, metal parts of the board, mounting tools, and the person doing the mounting are kept at the same electric (ground) potential. If it is impossible to ground the printed-circuit board the person mounting the circuits should touch the board before bringing MOS circuits into contact with it.

Soldering

Soldering iron tips, including those of low-voltage irons, or soldering baths should also be kept at the same potential as the MOS circuits and the board.

Static charges

Dress personnel in clothing of non-electrostatic material (no wool, silk or synthetic fibres). After the MOS circuits have been mounted on the board proper handling precautions should still be observed. Until the sub-assemblies are inserted into a complete system in which the proper voltages are supplied, the board is no more than an extension of the leads of the devices mounted on the board. To prevent static charges from being transmitted through the board wiring to the device it is recommended that conductive clips or conductive tape be put on the circuit board terminals.

Transient voltages

To prevent permanent damage due to transient voltages, do not insert or remove MOS devices, or printed-circuit boards with MOS devices, from test sockets or systems with power on.

Voltage surges

Beware of voltage surges due to switching electrical equipment on or off, relays and d.c. lines.

Introduction for type numbers with numerical prefixes

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Product Status

DEFINITIONS		
Data Sheet Identification	**Product Status**	**Definition**
Objective Specification	**Formative or In Design**	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	**Preproduction Product**	This data sheet contains preliminary data and supplementary data will be published at a later date. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	**Full Production**	This data sheet contains Final Specifications. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Ordering Information

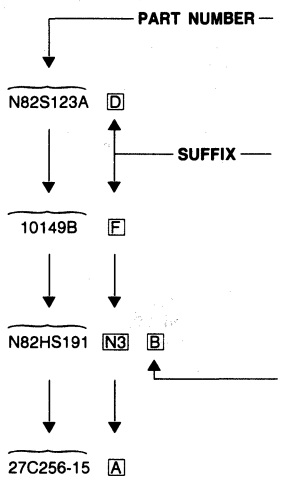
Memory Products

Signetics Memory integrated circuit products may be ordered by contacting either the local Signetics sales office, Signetics representatives and/or Signetics authorized distributors. A complete listing is located in the back of this manual.

The tables shown below provide part number definitions for Signetics memory products. The Signetics part number system allows complete definition for ordering a device. The part number itself and the product description is defined on each data sheet. The suffix is a letter defining a package type. Additional or special processing is defined by adding the processing indicator when required.

The military qualification, Full MIL Signetics or Full JAN slash sheet status, can be determined by contacting Signetics Military Division or referring to the Signetics Military Data Book.

Table 1. Part Number Description



USED TO DEFINE PART

USED TO DEFINE PACKAGE TYPE	
Package Code	**Package Description**
A	20, 28, 32-Leaded Plastic Chip Carrier
D	16, 20-Lead Small Outline
F	16, 18, 20, 22, 24, 28-Lead CERDIP
N	16, 18, 20, 22, 24, 28-Lead DIP Plastic
N3	24-Lead 300mil-wide DIP Plastic
FA	24, 28-Lead CERDIP with Quartz Window

USED TO DEFINE ADDITIONAL PROCESSING		
B	SUPR II B	Operating High Temp. Burn-In

Quality and Reliability

Memory Products

SIGNETICS MEMORY QUALITY

Signetics has put together a winning process for manufacturing Memories. Our standard is zero defects, and current customer quality statistics demonstrate our commitment to this goal.

The memories produced in Signetics must meet rigid criteria as defined by our design rules and as evaluated with a thorough product characterization and quality process. The capabilities of our manufacturing process are measured and the results evaluated and reported through our corporate-wide QA05 data base system. The SURE (Systematic Uniform Reliability Evaluation) program monitors the performance of our product in a variety of accelerated environmental stress conditions. All of these programs and systems are intended to prevent product-related problems and to inform our customers and employees of our progress in achieving zero defects.

RELIABILITY BEGINS WITH THE DESIGN

Quality and reliability must begin with design. No amount of extra testing or inspection will produce reliable ICs from a design that is inherently unreliable. Signetics follows very strict design and layout practices with its circuits. To eliminate the possibility of metal migration, current density in any path cannot exceed 2×10^5 amps/cm^2. Layout rules are followed to minimize the possibility of shorts, circuit anomalies, and SCR type latch-up effects. Numerous ground-to-substrate connections are required to ensure that the entire chip is at the same ground potential, thereby precluding internal noise problems.

PRODUCT CHARACTERIZATION

Before a new design is released, the characterization phase is completed to insure that the distribution of parameters resulting from lot-to-lot variations is well within specified limits. Such extensive characterization data also provides a basis for identifying unique application-related problems which are not part of normal data sheet guarantees. Characterization takes place from −55°C to +125°C and at ± 10% supply voltage.

QUALIFICATION

Formal qualification procedures are required for all new or changed products, processes and facilities. These procedures ensure the high level of product reliability our customers expect. New facilities are qualified by corporate groups as well as by the quality organizations of specific units that will operate in the facility. After qualification, products manufactured by the new facility are subjected to highly accelerated environmental stresses to ensure that they can meet rigorous failure rate requirements. New or changed processes are similarly qualified.

QA05 — QUALITY DATA BASE REPORTING SYSTEM

The QA05 data reporting system collects the results of product assurance testing on all finished lots and feeds this data back to concerned organizations where appropriate action can be taken. The QA05 reports EPQ (Estimated Process Quality) and AOQ (Average Outgoing Quality) results for electrical, visual/mechanical, hermeticity, and documentation audits. Data from this system is available upon request.

THE SURE PROGRAM

The SURE (Systematic Uniform Reliability Evaluation) program audits/monitors products from all Signetics' divisions under a variety of accelerated environmental stress conditions. This program, first introduced in 1964, has evolved to suit changing product complexities and performance requirements.

The SURE program has two major functions: Long-term accelerated stress performance audit and a short-term accelerated stress monitor. In the case of Memory products, samples are selected that represent all generic product groups in all wafer fabrication and assembly locations.

THE LONG-TERM AUDIT

One-hundred devices from each generic family are subjected to each of the following stresses every eight weeks:

- High Temperature Operating Life: T_J = 150°C, 1000 hours, static biased or dynamic operation, as appropriate (worst case bias configuration is chosen)
- High Temperature Storage: T_J = 150°C, 1000 hours
- Temperature Humidity Biased Life: 85°C, 85% relative humidity, 1000 hours, static biased
- Temperature Cycling (Air-to-Air): −65°C to +150°C, 1000 cycles

THE SHORT-TERM MONITOR

Every other week a 50-piece sample from each generic family is run to 168 hours of pressure pot (15psig, 121°C, 100% saturated steam) and 300 cycles of thermal shock (−65°C to +150°C)

In addition, each Signetics assembly plant performs SURE product monitor stresses weekly on each generic family and molded package by pin count and frame type. Fifty-piece samples are run on each stress, pressure pot to 96 hours, thermal shock to 300 cycles.

SURE REPORTS

The data from these test matrices provides a basic understanding of product capability, an indication of major failure mechanisms and an estimated failure rate resulting from each stress. This data is compiled periodically and is available to customers upon request.

Many customers use this information in lieu of running their own qualification tests, thereby eliminating time-consuming and costly additional testing.

RELIABILITY ENGINEERING

In addition to the product performance monitors encompassed in the memory SURE program, Signetics' Corporate and Division Reliability Engineering departments sustain a broad range of evaluation and qualification activities.

Included in the engineering process are:

- Evaluation and qualification of new or changed materials, assembly/wafer-fab processes and equipment, product designs, facilities and subcontractors
- Device or generic group failure rate studies
- Advanced environmental stress development
- Failure mechanism characterization and corrective action/prevention reporting

The environmental stresses utilized in the engineering programs are similar to those utilized for the SURE monitor; however, more highly-accelerated conditions and extended durations typify the engineering projects. Additional stress systems such as biased pressure pot, power-temperature cycling, and cycle-biased temperature-humidity, are also included in the evaluation programs.

FAILURE ANALYSIS

The SURE Program and the Reliability Engineering Program both include failure analysis activities and are complemented by corporate, divisional and plant failure analysis departments. These engineering units provide a service to our customers who desire detailed failure analysis support, who in turn provide Signetics with the technical understanding of the failure modes and mechanisms actually experienced in service. This information is essential in our ongoing effort to accelerate and improve our understanding of product failure mechanisms and their prevention.

ZERO DEFECTS PROGRAM

In recent years, United States industry has increasingly demanded improved product quality. We at Signetics believe that the customer has every right to expect quality products from a supplier. The benefits which are derived from quality products can be summed up in the words, *lower cost of ownership.*

Those of you who invest in costly test equipment and engineering to assure that incoming products meet your specifications have a special understanding of the cost of ownership. And your cost does not end there; you are also burdened with inflated inventories, lengthened lead times and more rework.

SIGNETICS UNDERSTANDS CUSTOMERS' NEEDS

Signetics has long had an organization of quality professionals, inside all operating units, coordinated by a corporate quality department. This broad decentralized organization provides leadership, feedback, and direction for achieving a high level of quality. Special programs are targeted on specific quality issues. For example, in 1978 a program to reduce electrically defective units for a major automotive manufacturer improved outgoing quality levels by an order of magnitude.

In 1980 we recognized that in order to achieve outgoing levels on the order of 100ppm (parts per million), down from an industry practice of 10,000ppm, we needed to supplement our traditional quality programs with one that encompassed all activities and all levels of the company. Such unprecedented low defect levels could only be achieved by contributions from all employees, from the R and D laboratory to the shipping dock. In short, from a program that would effect a total cultural change within Signetics in our attitude toward quality.

QUALITY PAYS OFF FOR OUR CUSTOMERS

Signetics' dedicated programs in product quality improvement, supplemented by close working relationships with many of our customers, have improved outgoing product quality more than twenty-fold since 1980. Today, many major customers no longer test Signetics circuits. Incoming product moves directly from the receiving dock to the production line, greatly accelerating throughput and reducing inventories. Other customers have pared significantly the amount of sampling done on our products. Others are beginning tc adopt these cost-saving practices.

We closely monitor the electrical, visual, and mechanical quality of all our products and review each return to find and correct the cause. Since 1981, over 90% of our customers report a significant improvement in overall quality (see Figure 1).

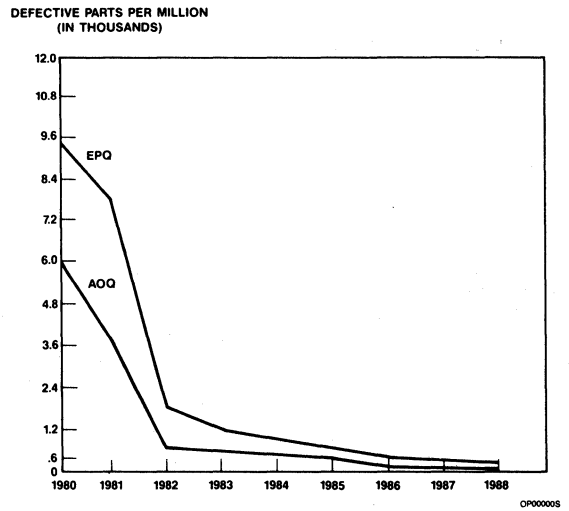


Figure 1. Signetics' Quality Progress

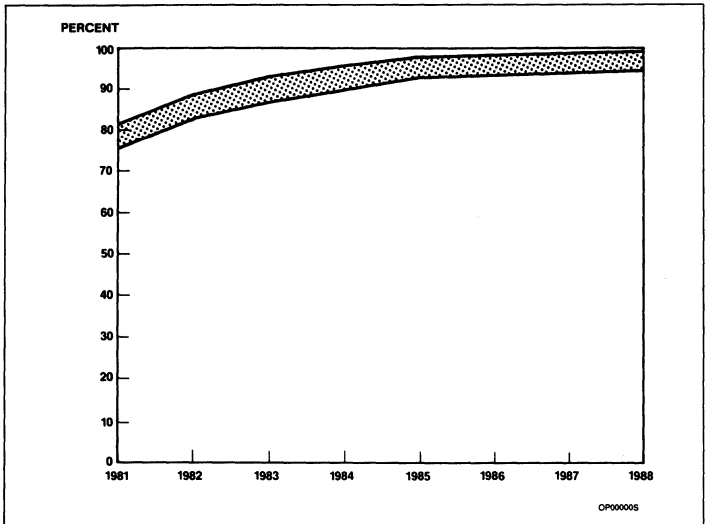


Figure 2. Performance To Schedule On-Time Delivery

At Signetics, quality means more than working circuits. It means on-time delivery of the right product at the agreed-upon price (see Figure 2).

ONGOING QUALITY PROGRAM

The quality improvement program at Signetics is based on "Do it Right the First Time". The intent of this innovative program is to change the perception of Signetics' employees that somehow quality is solely a manufacturing issue where some level of defects is inevitable. This attitude has been replaced by one of acceptance of the fact that all errors and defects are preventable, a point of view shared by all technical and administrative functions equally.

This program extends into every area of the company, and more than 40 quality improvement teams throughout the organization drive its ongoing refinement and progress.

Key components of the program are the Quality College, the "Make Certain" Program, Corrective Action Teams, and the Error Cause Removal System.

The core concepts of doing it right the first time are embodied in the four absolutes of quality:

1. The definition of quality is conformance to requirements.
2. The system to achieve quality improvement is prevention.
3. The performance standard is zero defects.
4. The measurement system is continuous improvement.

QUALITY COLLEGE

Almost continuously in session, Quality College is a prerequisite for all employees. The intensive curriculum is built around the four absolutes of quality; colleges are conducted at company facilities throughout the world.

"MAKING CERTAIN" — ADMINISTRATIVE QUALITY IMPROVEMENT

Signetics' experience has shown that the largest source of errors affecting product and service quality is found in paperwork and in other administrative functions. The "Make Certain" program focuses the attention of management and administrative personnel on error prevention, beginning with each employee's own actions.

This program promotes defect prevention in three ways: by educating employees as to the impact and cost of administrative errors, by changing attitudes from accepting occasional errors to one of accepting a personal work standard of zero defects, and by providing a formal mechanism for the prevention of errors.

CORRECTIVE ACTION TEAMS

Employees with the perspective, knowledge, and necessary skills to solve a problem are formed into ad hoc groups called Corrective Action Teams. These teams, a major force within the company for quality improvement, resolve administrative, technical and manufacturing issues.

ECR SYSTEM (ERROR CAUSE REMOVAL)

The ECR System permits employees to report to management any impediments to doing the job right the first time. Once such an impediment is reported, management is obliged to respond promptly with a corrective program. Doing it right the first time in all company activities produces lower cost of ownership through defect prevention.

PRODUCT QUALITY PROGRAM

To reduce defects in outgoing products, we created the Product Quality Program. This is managed by the Product Engineering Council, composed of the top product engineering and test professionals in the company. This group:

1. Sets aggressive product quality improvement goals;
2. provides corporate-level visibility and focus on problem areas;
3. serves as a corporate resource for any group requiring assistance in quality improvement; and
4. drives quality improvement projects.

As a result of this aggressive program, every major customer who reports back to us on product performance is reporting significant progress.

VENDOR CERTIFICATION PROGRAM

Our vendors are taking ownership of their own product quality by establishing improved process control and inspection systems. They subscribe to the zero defects philosophy. Progress has been excellent.

Through intensive work with vendors, we have improved our lot acceptance rate on incoming materials as shown in Figure 3. Simultaneously, waivers of incoming material have been eliminated.

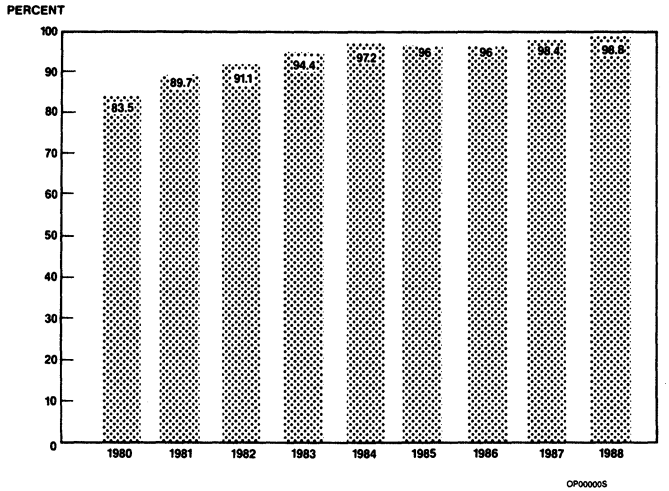


Figure 3. Lot Acceptance Rate From Signetics' Vendors

MATERIAL WAIVERS

1988 – 0
1987 – 0
1986 – 0
1985 – 0
1984 – 0
1983 – 0
1982 – 2
1981 – 134

Higher incoming quality material ensures higher outgoing quality products.

QUALITY AND RELIABILITY ORGANIZATION

Quality and reliability professionals at the divisional level are involved with all aspects of the product, from design through every step in the manufacturing process, and provide product assurance testing of outgoing product. A separate corporate-level group provides direction and common facilities.

Quality and Reliability Functions:

- Manufacturing quality control
- Product assurance testing and qualification
- Laboratory facilities — failure analysis, chemical, metallurgy, thin film, oxides
- Environmental stress testing
- Quality and reliability engineering
- Customer liaison

COMMUNICATING WITH EACH OTHER

For information on Signetics' quality programs or for any question concerning product quality, the field salesperson in your area will provide you with the quickest access to answers. Or, write on your letterhead directly to the corporate VP of quality at the corporate address shown at the back of this manual.

We are dedicated to preventing defects. When product problems do occur, we want to know about them so we can eliminate their causes. Here are some ways we can help each other:

- Provide us with one informed contact within your organization. This will establish continuity and build confidence levels
- Periodic face-to-face exchanges of data and quality improvement ideas between your engineers and ours can help prevent problems before they occur
- Test correlation data is very useful. Line-pull information and field failure reports also help us improve product performance
- Provide us with as much specific data on the problem as soon as possible to speed analysis and enable us to take corrective action
- An advance sample of the devices in question can start us on the problem resolution before physical return of shipment.

This team work with you will allow us to achieve our mutual goal of improved product quality.

MANUFACTURING: DOING IT RIGHT THE FIRST TIME

In dealing with the standard manufacturing flows, it was recognized that significant improvement would be achieved by "doing every job right the first time", a key concept of the quality improvement program. Key changes included such things as implementing 100% temperature testing on all products as well as upgrading test handlers to insure 100% positive binning. Some of the other changes and additions were to tighten the outgoing QA lot acceptance criteria to the tightest in the industry, with zero defect lot acceptance sampling across all three temperatures.

The achievements resulting from the improved process flow have helped Signetics to be recognized as the leading quality supplier of memories. These achievements have also led to our participation in several Ship-to-Stock programs, which our customers use to eliminate incoming inspection. Such programs reduce the user *cost of ownership* by saving both time and money.

Bipolar Reliability Information

Memory Products

OUR GOAL: 100% PROGRAMMING YIELD

Our original goal back in the early 1970s was to develop a broad line of programmable products which would be recognized as having the best programming yield in the industry. Within the framework of a formal quality program, our efforts to improve circuit designs and refine manufacturing controls have resulted in major advances toward that goal.

Also within the framework of our formal quality program, we have now established a stated goal of 100% programming yield. Through the increasing effectiveness of a quality attitude of "Do It Right The First Time" we're moving ever closer to that target.

A significant amount of data on bipolar programming yields has been collected over the past three years. This data is the result of both inhouse programming (customer orders) and reports from major users of fuseable products. The data covers the full range of products from 256-bit PROMs to 64K PROMs and indicates an average level of 97.9% programming yield.

As time goes on the drive for a product line that has Zero Defects will grow in intensity. These efforts will provide both Signetics and our customers with the ability to achieve the mutual goal of improved product quality.

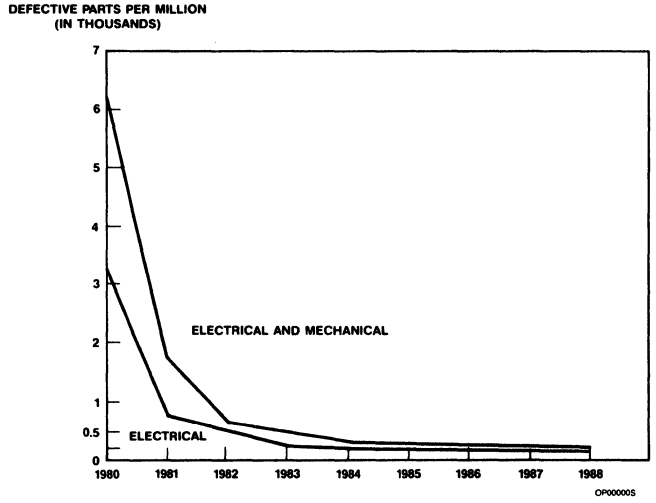
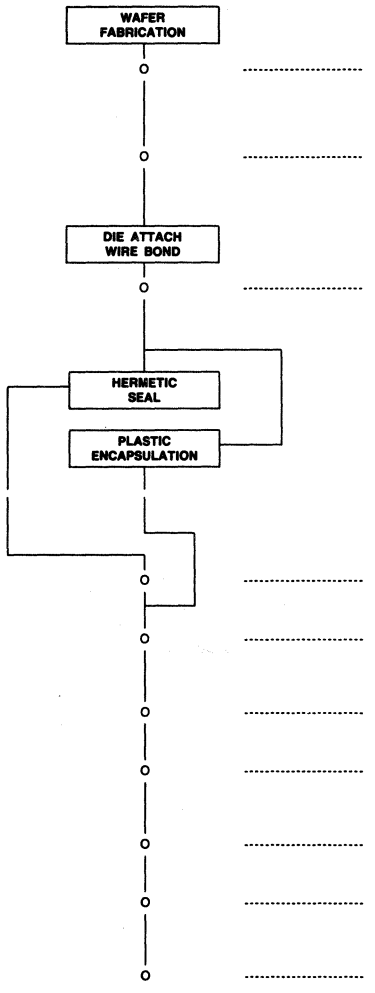


Figure 1. Bipolar Memory AOQ (Average Outgoing Quality)

The Memory Quality Assurance department has monitored Bipolar ppm progress, which can be seen in Figure 1. We are pleased with the progress that has been made, and expect to achieve even more impressive results as the procedures for accomplishing these tasks are fine tuned.

The real measure of any quality improvement program is the result that our customers see. The meaning of *Quality* is more than just working circuits. It means commitment to *On Time Delivery* at the *Right Place* of the *Right Quantity* of the *Right Product* at the *Agreed Upon Price.*



SCANNING ELECTRON MICROSCOPE CONTROL

Wafers are sampled daily by the Quality Control Laboratory from each fabrication area and subjected to SEM analysis. This process control reveals manufacturing defects such as contact and oxide step coverage in the metalization process which may result in early failures.

DIE SORT VISUAL ACCEPTANCE

Product is inspected for defects caused during fabrication, wafer testing, or the mechanical scribe and break operation. Defects such as scratches, smears and glassivated bonding pads are included in the lot acceptance criteria.

PRE-SEAL VISUAL ACCEPTANCE

Product is inspected to detect any damage incurred at the die attach and wire bonding stations. Defects such as scratches, contamination and smeared ball bonds are included in the lot acceptance criteria.

SEAL TESTS

Hermetic package seal integrity is ensured by 100% gross leak testing.

100% ELECTRICAL TEST

Every device is tested for functional and AC/DC parameters at 75°C with guard bands to assure performance to data sheet limits.

BURN IN (SUPR II LEVEL B OPTION)

Devices are burned in for 21 hours at 155°C maximum junction temperature.

SYMBOL

Devices are marked with the Signetics logo, device number and date code or custom symbol per individual specification requirements.

VISUAL

All products are 100% visually inspected per the requirements specified in Signetics or customer documents.

100% PRODUCTION ELECTRICAL TESTING

Every device is tested for functional and AC/DC parameters at 25°C with guard bands to assure performance to data sheet limits.

FINAL QUALITY ASSURANCE GATE

The final QA inspection step gurantees the specified mechanical and electrical AQL's. Every shipment is sealed and identified by QA personnel.

Figure 2. Bipolar Memory Process Flow

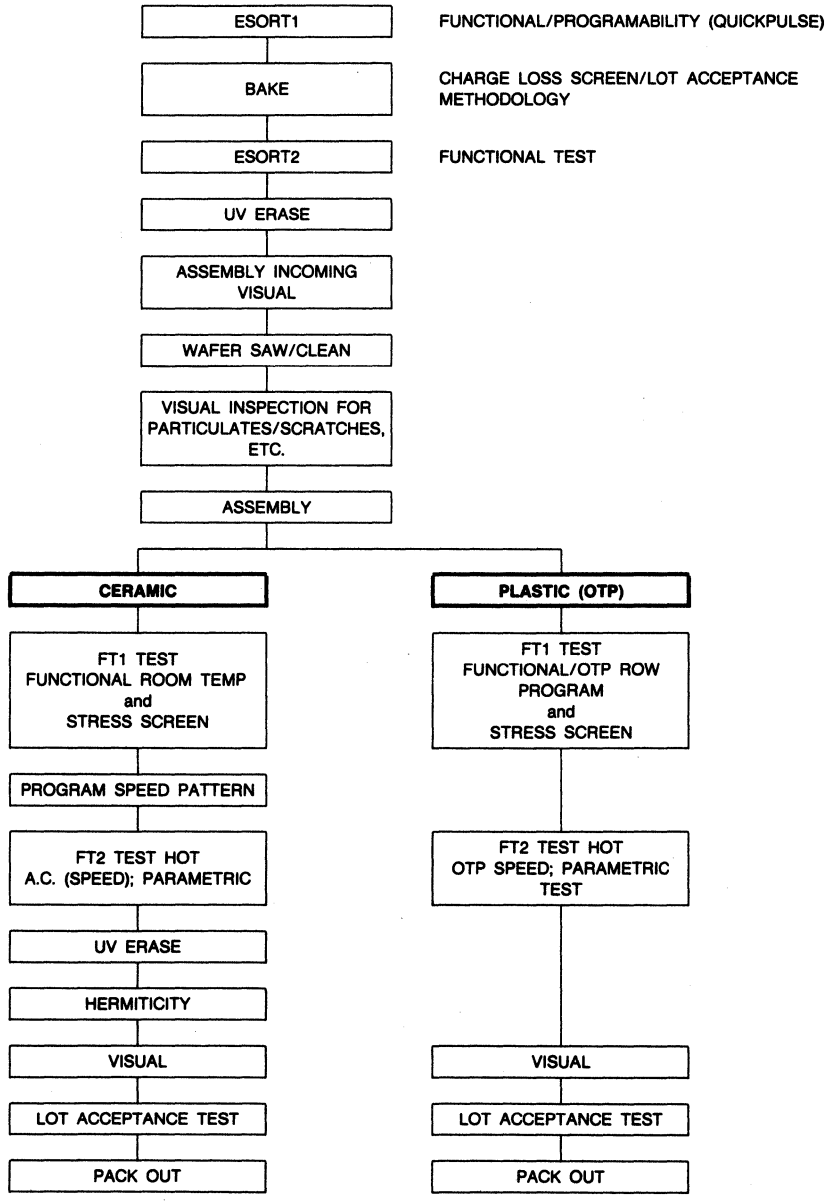


Figure 3. EPROM MEMORY PROCESS FLOW

EPROM Reliability Information

Memory Products

All Signetics' EPROM die are designed as low power UV light erasable and electrically programmable read only memories. They have been designed to perform over military and commercial temperature ranges. These die are assembled in EPROM packages that comply with industry standard packages: Cerdip (Quartz window), Plastic DIP (One Time Programmable) and Plastic Leaded Chip Carrier (One Time Programmable).

The following descriptions are of the tests and calculations performed on each device organization and package type to validate the quality and reliability of the CMOS design and technology. All described tests are performed on each package type, with the exception of the 'Program-erase cycling' test for the One Time Programmable devices.

ELECTROSTATIC DISCHARGE PROTECTION (ESD)

This test is performed to validate the product's tolerance to electrostatic discharge damage.

Both MIL-STD-883 criteria (human body model) and mechanical model charged device test are performed.

HIGH TEMPERATURE STORAGE LIFE TEST (HTSL)

Another popular name for this test is data retention bake. This process is used to thermally accelerate charge loss from the floating gate. The test is performed by subjecting devices that contain a 100% programmed data pattern to a 250°C bake with no applied electrical bias or clocks.

In addition to charge loss, this test is used to detect mechanical reliability (i.e., bond integrity) and process instability.

DYNAMIC LOW TEMPERATURE LIFE TEST (DLTL)

This test is performed at −10°C to detect the effects of hot electron injection into the gate oxide as well as package-related failures (i.e., metal corrosion). The biasing and clocking conditions for this test are identical to the DHTL #1 test.

TEMPERATURE CYCLE (TMCL)

This test consists of performing 200 cycles of ambient air temperature of the chamber and housing the unbiased subject devices from −65°C to +150°C and back. The 200 cycles are performed at 20 minutes per cycle.

DYNAMIC HIGH TEMPERATURE LIFE TEST (DHTL #1)

This test is used to accelerate failure mechanisms by operating the devices at 125°C ambient temperature with worst-case specified power supply voltages of V_{CC} and V_{PP} at 5.5V. The memory is sequentially addressed to exercise the fully-loaded outputs. A checkerboard complement data pattern is used to simulate random patterns expected during actual use.

DYNAMIC HIGH TEMPERATURE LIFE TEST (DHTL #2)

This test is used to accelerate oxide breakdown failures and to further accelerate the failure mechanisms of DHTL #1. The test setup is identical to the one used for the DHTL #1 test except the temperature is 150°C and the V_{CC} and V_{PP} power supply voltages are 6.5V, resulting in a 20% increase over the specified operational electrical field across the gate oxides of the device (1.25mV/cm for 325Å oxide thickness). This represents a 55 × electrical field induced acceleration in addition to the thermal acceleration at 150°C.

PROGRAM-ERASE CYCLING AND PROGRAMMABILITY

All four power supply voltage combinations for V_{CC} and V_{PP} are tested for programmability (V_{CC} = 6.0V ± 0.25V and V_{PP} = 12.5V ± 0.5V in program mode). The number of possible program/erase cycles is then tested to establish program-erase cycling expectations.

FAILURE RATE PREDICTIONS

In preparation for the various life tests, a 168 hour, 125°C, 5.5V production burn-in is performed on the devices. The infant mortality rejects are removed from the population in order to develop long-term failure rate information during the random failure rate portion of the device life cycle.

The failure rate calculation combines all failure mechanisms by activation energies and associated device hours for the 125°C, 5.5V Dynamic Life Test (DHTL #1), the 150°C, 6.5V Dynamic Life Test (DHTL #2), the 150°C, 7.5V Static Life Test and the 250°C Bake.

The activation energies for the various EPROM failure mechanisms are:

Defective bit charge gain/loss (electron hopping conduction)	0.6eV
Oxide breakdown	0.3eV
Silicon defects	0.3eV
Contamination	1.0 − 1.2eV
Intrinsic charge loss	1.4eV

NOTE:
The combined failure rate for the stresses is the sum of failure rates by activation energies.

METHODS OF FAILURE RATE CALCULATIONS

Actual Device Hours = Number of Devices × Number of Hours. In order to determine the Equivalent Hours derated to a given operating temperature, the junction temperatures of the devices should be calculated using the known thermal resistance of the package (θ_{JA}) and the power dissipation of the devices:

$$T_{1,2} = \theta_{JA}\ (IV)_{1,2} + T_{A1,2} \qquad (1)$$

Using the Arrhenius relation, the test temperature and the derated operating temperature will yield the thermal acceleration factor from T_1 to T_2:

$$\frac{R_1}{R_2} = \frac{A \cdot \exp\left[\frac{E_A}{kT_1}\right]}{A \cdot \exp\left[\frac{E_A}{kT_2}\right]} = \exp\left[\frac{E_A}{k}\right]\left[\frac{1}{T_1} - \frac{1}{T_2}\right] \qquad (2)$$

$k = 8.617 \times 10^{-5}$ eV/Kelvin (Boltzmann's constant)
A = proportionality constant for a given failure mechanism
R_1 = mean time to failure @ T_1
R_2 = mean time to failure @ T_2
E_A = activation energy for the failure mechanism
T_1 = operating temperature
T_2 = life test temperature

An additional 55 × acceleration factor should be added for the 150°C/6.5V dynamic life test due to the time-dependent oxide failure acceleration (20% higher than specified power supply voltage).

Multiplying the actual device hours by the acceleration factor for each failure mechanism will result in the equivalent hours.

Poisson statistics are applied to estimate the performance of the population from the life test results of a sample test. This is useful when the probability of failures is small and the failures occur randomly in time. A commonly used formula for estimating the failure rate is the "chi-squared" equation:

$$F_C = \frac{\chi^2}{2nt} \times 100\% \qquad (3)$$

F_C = calculated failure rate estimate (in %/1000 hrs) at upper confidence limit
χ^2 = "chi-squared" value for $2F_A + 2$ degrees of freedom for α where F_A is the number of actual failures (χ^2 comes from available tables for a known α)
α = 1−B, where B is the confidence limit (B is stated in %).
n = number of units in test
t = test time in thousands of hours (equivalent)

Equation 3 will calculate the estimated failure rates/1000 hrs for 60% confidence level (industry standard) for each failure mechanism.

Selection Guide

Memory Products

DEVICE[5]	ORGANIZATION	OUTPUT CIRCUIT[1]	OUTPUT LOGIC[2]	ACCESS TIME[3]	PACKAGE[4]	PINS	MAX I_{CC}
RAMs							
82S25	16 × 4	OC	B	50	N, D	16	105
3101A	16 × 4	OC	B	35	N, D	16	105
74S189	16 × 4	TS	B	35	N, D	16	110
74F189A	16 × 4	TS	—	15	N, D	16, 20	70
82S16	256 × 1	TS	T	50	N, D	16	115
74S301	256 × 1	OC	B	50	N, D	16	130
82LS16	256 × 1	TS	T	40	N, D	16	70
74LS301	256 × 1	OC	B	40	N, D	16	70
82S09	64 × 9	OC	T	45	A, N	28	190
82S09A	64 × 9	OC	T	35	A, N	28	190
82S19	64 × 9	OC	B	35	N	28	190
82S212	256 × 9	TS	B	45	N, A	22	185
82S212A	256 × 9	TS	B	35	N, A	22	185
8X350	256 × 8	TS	B	N/A	N, A	22	185
PROMs							
82S23	32 × 8	OC	—	50	N, A	16, 20	96
82S23A	32 × 8	OC	—	25	N, A, D	16, 20	96
82US23	32 × 8	OC	—	10	N, A, D	16, 20	115
82S123	32 × 8	TS	—	50	N, A	16, 20	96
82S123A	32 × 8	TS	—	25	N, A, D	16, 20	96
82US123	32 × 8	TS	—	13	N, A, D	16, 20	115
10P256	32 × 8	OE	—	3	F	16	150
100P256	32 × 8	OE	—	3	F	16	150
82S126	256 × 4	OC	—	50	N	16, 20	120
82S126A	256 × 4	OC	—	30	N, A, D	16, 20	120
82S129	256 × 4	TS	—	50	N	16, 20	120
82S129A	256 × 4	TS	—	27	N, A, D	16, 20	120
10149	256 × 4	OE	—	20	F	16	160
10149A	256 × 4	OE	—	10	F	16	160
10149B	256 × 4	OE	—	5	F	16	160
100149	256 × 4	OE	—	20	F	16	160
100149A	256 × 4	OE	—	10	F	16	160
100149B	256 × 4	OE	—	5	F	16	160
82S130	512 × 4	OC	—	50	N	16, 20	140
82S130A	512 × 4	OC	—	33	N, A, D	16, 20	140
82S131	512 × 4	TS	—	50	N	16, 20	140
82S131A	512 × 4	TS	—	30	N, A, D	16, 20	140
82LS135	256 × 8	TS	—	100	A, N	20	100
82S135	256 × 8	TS	—	45	A, N, D	20	150
82S115	512 × 8	TS	—	60	N	24	175
82S137	1024 × 4	TS	—	60	N, A	18, 20	140
82S137A	1024 × 4	TS	—	45	N, A	18, 20	140
82S137B	1024 × 4	TS	—	35	N, A	18, 20	140
82S141	512 × 8	TS	—	60	N	24	175
82S141A	512 × 8	TS	—	45	N, N3, A	24	175
82S147	512 × 8	TS	—	60	A, N	20	155
82S147A	512 × 8	TS	—	45	A, N	20	155
82S147B	512 × 8	TS	—	25	N, A	20	155
82S181	1024 × 8	TS	—	70	N	24	175
82S181A	1024 × 8	TS	—	55	N, A	24, 28	175
82S181C	1024 × 8	TS	—	35	N, N3, A	24, 28	175
82S183	1024 × 8	TS	—	60	N, A	24, 28	175
82S185	2048 × 4	TS	—	100	N	18	120

Selection Guide

DEVICE[5]	ORGANIZATION	OUTPUT CIRCUIT[1]	OUTPUT LOGIC[2]	ACCESS TIME[3]	PACKAGE[4]	PINS	MAX I_{CC}
PROMs							
82S185A	2048 × 4	TS	—	50	N	18	155
82S185B	2048 × 4	TS	—	35	N, A	18, 20	155
82HS187	1024 × 8	TS	R	55	N, A	24, 28	175
82HS187A	1024 × 8	TS	R	45	N, A	24, 28	175
82HS189	1024 × 8	TS	R	55	N, A	24, 28	175
82HS189A	1024 × 8	TS	R	45	N, A	24, 28	175
82HS191	2048 × 8	TS	—	25	N, N3, A	24, 28	175
82S191	2048 × 8	TS	—	80	N, A	24, 28	175
82S191A	2048 × 8	TS	—	55	N, A	24, 28	175
82S191C	2048 × 8	TS	—	35	A, N, N3	24	175
82LHS191	2048 × 8	TS	—	35	N, N3, A	24	110
82HS195	4096 × 4	TS	—	45	N	20	145
82HS195A	4096 × 4	TS	—	35	N	20	145
82HS195B	4096 × 4	TS	—	25	N	20	145
10P016	4096 × 4	OE	—	10	F	20	200
100P016	4096 × 4	OE	—	10	F	20	200
82HS321	4096 × 8	TS	—	45	N, A	24, 28	175
82HS321A	4096 × 8	TS	—	35	N, A	24, 28	175
82HS321B	4096 × 8	TS	—	30	N, A, N3	24, 28	175
82HS321C	4096 × 8	TS	—	25	N3, A	24, 28	185
82LHS321	4096 × 8	TS	—	35	N3, A	24, 28	110
82HS641	8192 × 8	TS	—	55	N	24, 28	175
82HS641A	8192 × 8	TS	—	45	N	24, 28	175
82HS641B	8192 × 8	TS	—	35	N	24, 28	175
82HS641C[6]	8192 × 8	TS	—	25	N, A	24, 28	185
27C64A	8192 × 8	TS	—	120	FA, N, A	28, 32	20
27HC641	8192 × 8	TS	—	45	FA, N, A	24, 28	110
27HC128	16384 × 8	TS	—	35	FA, N, A	28, 28	110
27C256	32768 × 8	TS	—	120	FA, N, A	28, 32	20
27C512	65538 × 8	TS	—	150	FA, N, A	28, 32	20
27C210	65538 × 16	TS	—	150	FA, N, A	40, 44	50

NOTES:

1. Output circuit
   OE = Open Emitter
   OC = Open Collector
   TS = 3-State
2. Output logic
   T = Transparent — input data appears on output during Write
   B = Blanked — output is blanked during Write
   R = Registers
3. Commercial (0°C to +75°C)
4. Packages:
   N = Plastic Dual In Line (N3 = 300mil-wide)*
   FA = CERDIP with quartz window
   A = Plastic Square Leaded Chip Carrier
   D = Small Outline Large (SO-L)
   *Whenever a single device is offered in both 300mil-wide and 600mil-wide packages, designate either N3 (300mil) or N (600mil) to assure proper order entry and shipment.
5. Part numbers:
   82Sxxx Junction-Isolated NiCr fuse
   82HSxxx Oxide-Isolated vertical fuse
   82USxxx Oxide-Isolated TiW fuse
   27Cxxx EPROM
   27HCxxx High Speed EPROM
6. Objective specification (under product development)

RAM Cross Reference Guide

Bipolar Memory Products

ORGANIZATION	PKG PINS	SIGNETICS	$\frac{T_{AA}}{I_{CC}}$	FAIRCHILD	$\frac{T_{AA}}{I_{CC}}$	TI	$\frac{T_{AA}}{I_{CC}}$	AMD	$\frac{T_{AA}}{I_{CC}}$	NATIONAL	$\frac{T_{AA}}{I_{CC}}$
16 × 4 OC	16	N3101A	35/105	93403*	NA	SN74S289B	35/105	AM27S02 AM3101A	35/100 35/100	DM74S289	35/110
16 × 4 TS	16	N74S189 N74F189A	35/110 15/55	93405*	NA	SN74S189B	35/110	AM27S03 AM27S03A	35/100 25/100	DM74S189 DM74S189A	35/110 25/100
16 × 4 OC	16	N82S25	50/105	93403*	NA	SN74S289B	35/105	AM27S02	35/100	DM74S289	35/110
64 × 9 OC	28	N82S09 N82S09A T	45/190 35/190								
64 × 9 OC	28	N82S19	35/190	93419 93419A	45/150 35/150						
256 × 1 OC	16	N74S301	50/130			SN74S301	65/140	AM27LS01A	35/115		
256 × 1 OC	16	N74LS301	40/70					AM27LS01	45/70		
256 × 1 TS	16	N82S16 T	50/115	93421* T	NA	SN74S201	65/140	AM27LS00-1A T	35/115	74S200* T	NA
256 × 1 TS	16	N82LS16 T	40/70					AM27LS00-1 T	45/70	74S206* T	NA
256 × 8 TS	22	N8X350	NA/185								
256 × 9 TS	22	N82S212 N82S212A	45/185 35/185	93479 93479A	45/185 35/185						

NOTES:
T: Output is Transparent during write
*: Possibly Discontinued

PROM Cross Reference Guide

Bipolar Memory Products

TI PART NO.	PERFORMANCE t_{AA}/I_{CC}	SIGNETICS PART NO.	PERFORMANCE t_{AA}/I_{CC}
1/4K 32 × 8			
18SA030	40/110	82S23A	25/96
38SA030	25/125	82S23A	25/96
38SA032		82S23A A	25/96
18S030	40/110	82S123A	25/96
38S030	15/125	82US123	10/110
38L030	20/45	82US123*	
38S032	15/125	82S123A A	25/96
38SA030		82US23	10/110
38S030	15/125	82US123	10/110
1K 256 × 4			
24SA10	65/100	82S126A	30/120
34SA10	25/95	82S126A*	
34SA12		82S126A A	30/120
24S10	55/100	82S129A	27/120
34S10	18/95	82S129A*	
34L10	27/50	82S129A*	
34S12	27/150	82S129A A	27/120
34L12	27/150	82S129A	50/120
2K 256 × 8			
28L22	70/100	82S135	45/155
28LA22	75/100	82S135*	
38L22	45/70	82S135*	
38S22	25/125	82S135	45/155
38SA22	30/125	82S135*	
4K 512 × 8			
28SA42	65/135	82S147*	
28L42	95/85	82S147	60/155
28S42	60/135	82S147	60/155
34S42	45/155	82S147A	45/155
28SA46	65/135	82S141*	
28L46	95/85	82S141*	
28S46	60/135	82S141A	45/175
4K 1K × 4			
24SA41	60/140	82S137*	
34SA41	35/110	82S137B*	
34S41	25/120	82S137B	35/140
24S41	60/140	82S137A	45/140
8K 1K × 8			
28L86A	110/80	82S181*	
28S2708A	70/165	82S181*	
28SA86A	70/175	82S181*	
28S86A	65/165	82S181A	55/175
38S86	45/165	82S181C	35/175

NOTE:
* Nearest Equivalent

PROM Cross Reference Guide

TI (Cont'd) PART NO.	PERFORMANCE t_{AA}/I_{CC}	SIGNETICS PART NO.	PERFORMANCE t_{AA}/I_{CC}
8K 2K × 4			
24SA81	70/175	82S185A*	
24S81	70/175	82S185A	50/155
38S85	45/175	82S185B	45/155
16K 2K × 8			
28S166	75/175	82S191A	55/175
28L166	125/110	82LHS191	35/110
38L165	35/100	82LHS191 N3	35/110
38L166	35/100	82LHS191 N	35/110
38L167	35/100	82LHS191 A	35/110
38S165	25/175	82HS191 N3	25/175
38SA165	35/175	82S191C N3*	
38S166	25/175	82HS191 N	25/175
38SA166	35/175	82S191C*	
38S167	35/175	82S191C A	35/175
38SA167	35/175	82S191C*	
16K 4K × 4			
34SA162	35/155	82HS195A*	
34L162	30/100	82HS195B*	
34S162-45	45/155	82HS195	45/155
34S162-35	35/155	82HS195A	35/155
34S162-25	25/155	82HS195B	25/155

NOTE:
* Nearest Equivalent

PACKAGES	TI Suffix	SIGNETICS Suffix
Plastic DIP	N	N
Ceramic DIP	J	F
PLCC (Plastic)	FN	A
LCC (Ceramic)	FK	G
SOL	DW	D
Plastic DIP (Skinny)	NT	N3
Ceramic DIP (Skinny)	JT	F3
Plastic DIP (Wide)	NW	N
Ceramic DIP (Wide)	JW	F
Super II Burn-In	-N3	-B

PROM Cross Reference Guide

AMD PART NO.	PERFORMANCE t_{AA}/I_{CC}	SIGNETICS PART NO.	PERFORMANCE t_{AA}/I_{CC}
1/4K 32 × 8			
27S18A	25/115	82S23A	25/96
27S19A	25/115	82S123A	25/96
27S19SA	15/115	82US123A	10/110
1K 256 × 4			
27S20	45/130	82S126A	30/120
27S20A	30/130	82S126A	30/120
27S21	45/130	82S129A	27/120
27S21A	30/130	82S129A	27/120
2K 512 × 4			
27S16	55/160	82S131	50/140
27S16A	35/160	82S131A	30/140
4K 512 × 8			
27S29	55/160	82S147A	45/155
27S29A	35/160	82S147B	25/155
27S31	55/175	82S141A	45/175
27S31A	35/175	82S141B	35/175
4K 1K × 4			
27S33	55/140	82S137A	45/140
27S33A	35/140	82S137B	35/140
8K 1K × 8			
27S181	60/185	82S181A N	55/175
27S181A	35/185	82S181C N	35/175
27S281	60/185	82S181A N3	55/175
27S281A	35/185	82S181C N3	35/175
8K 2K × 4			
27S185	50/150	82S185A	50/155
27S185A	35/150	82S185C	35/155
8K Registered 1K × 8			
27S35	20/185	82HS187	20/175
27S35A	15/185	82HS187A	15/175
27S37	20/185	82HS189	20/175
27S37A	15/185	82HS189A	15/175
16K 2K × 8			
27S191	50/185	82S191A	55/175
27S191A	35/185	82S191C	35/175
27S191SA	25/185	82HS191	25/185
27S291	50/185	82S191A N3	55/175
27S291A	35/185	82S191C N3	35/175
27S291SA	25/185	82HS191 N3	25/185
16K 4K × 4			
27S41	50/165	82HS195	45/155
27S41A	35/165	82HS195A	35/155
		82HS195B	25/155

AMD (Cont'd) PART NO.	PERFORMANCE t_{AA}/I_{CC}	SIGNETICS PART NO.	PERFORMANCE t_{AA}/I_{CC}
32K 4K × 8			
27S43	55/185	82HS321	45/185
27S43A	40/185	82HS321A	35/185
64K 8K × 8			
27S49	55/190	82HS641	55/185
27S49A	40/190	82HS641B	35/185

PACKAGES	AMD Suffix	SIGNETICS Suffix
Plastic DIP	P	N
Ceramic DIP	D	F
PLCC (Plastic)	J	A
LCC (Ceramic)	L	G
SOL		D
Plastic DIP (Skinny)		N3
Ceramic DIP (Skinny)		F3
Super II Burn-In	B	-B

PROM Cross Reference Guide

NATIONAL SEMI PART NO.	PERFORMANCE t_{AA}/I_{CC}	SIGNETICS PART NO.	PERFORMANCE t_{AA}/I_{CC}
1/4K 32 × 8			
74S188	35/110	82S23A	25/96
74S188A	25/110	82S23A	25/96
74S288	35/110	82S123A	25/96
74S288A	25/110	82S123A	25/96
PL87X288B	15/140	82US123	10/110
1K 256 × 4			
74S387	50/130	82S126A	30/120
74S387A	30/130	82S126A	30/120
74S287	50/130	82S129A	27/120
74S287A	30/130	82S129A	27/120
2K 512 × 4			
74S570A	45/130	82S130A	33/140
74S571A	45/130	82S131A	33/140
74S571B	35/130	82S131A	30/140
2K 256 × 8			
74LS471	60/100	82LS135	100/100
4K 512 × 8			
74S472	60/155	82S147	60/155
74S472A	45/155	82S147A	45/155
74S472B	35/155	82S147B	25/155
74S474	65/170	82S141	60/175
74S474A	45/170	82S141A	45/175
74S474B	35/170	82S141B	35/175
4K 1K × 4			
74S573	60/140	82S137	60/140
74S573A	45/140	82S137A	45/140
74S573B	35/140	82S137B	35/140
8K 1K × 8			
87S181	55/170	82S181A	55/175
87S181A	45/170	82S181C	35/175
87S281	55/170	82S181A N3	55/175
		82S181C N3	35/175
8K 2K × 4			
87S185	55/140	82S185A	50/155
87S185A	45/140	82S185B	45/155
87S185B	35/140	82S185C	35/155
8K Registered 1K × 8			
87SR181	20/175	82HS189	20/175
16K 2K × 8			
87S191	65/175	82S191A N	55/175
87S191A	45/175	82S191C N	35/175
87S191B	35/175	82S191C N	35/175
87S291	65/175	82S191A N3	55/175
87S291A	45/175	82S191C N3	35/175
87S291B	35/175	82S191C N3	35/175

NATIONAL SEMI (Cont'd) PART NO.	PERFORMANCE t_{AA}/I_{CC}	SIGNETICS PART NO.	PERFORMANCE t_{AA}/I_{CC}
16K 4K × 4			
87S195A	45/170	82HS195A	35/155
87S195B	35/170	82HS195A	35/155
32K 4K × 8			
87S321	55/185	82HS321	45/185

PACKAGES	NSC Suffix	SIGNETICS Suffix
Plastic DIP	N	N
Ceramic DIP	J	F
PLCC (Plastic)	V	A
LCC (Ceramic)		G
SOL		D
Plastic DIP (Skinny)	N	N3
Ceramic DIP (Skinny)	J	F3
Plastic DIP (Wide)		N
Ceramic DIP (Wide)		F
Super II Burn-In	–	–B

PROM Cross Reference Guide

MMI (Now AMD) PART NO.	PERFORMANCE t_{AA}/I_{CC}	SIGNETICS PART NO.	PERFORMANCE t_{AA}/I_{CC}
1/4K 32 × 8			
63S081	25/125	82S123A	25/96
PLE5P8C	25/125	82S123A	25/96
63S081A	15/125	82US123A	10/110
PLE5P8AC	15/125	82US123A	10/110
1K 256 × 4			
63S140	45/130	82S126A	30/120
63S141	45/130	82S129A	27/120
63S141A	30/130	82S129A	27/120
PLE8P4C	30/130	82S129A	27/120
2K 512 × 4			
63S240	45/130	82S130A	33/140
63S241	45/130	82S131A	30/140
63S241A	35/130	82S131A	30/140
PLE9P4C	35/130	82S131A	30/140
2K 256 × 8			
63S281	45/140	82S135	45/155
63S285	45/160	82S135	45/155
4K 512 × 8			
63S481	45/155	82S147A	45/155
63S481A	30/155	82S147A	45/155
PLE9P8C	30/155	82S147B	25/155
63S485	45/160	82S141	45/175
4K 1K × 4			
63S441	45/140	82S137A	45/140
63S441A	35/140	82S137B	35/140
PLE10P4C	35/140	82S137B	35/140
8K 1K × 8			
63S881	45/160	82S181C N	35/175
63S881A	30/160	82S181C N	35/175
PLE10P8C	30/160	82S181C N	35/175
63S881 × S	45/160	82S181C N3	35/175
63S881A × S	30/160	82S181C N3	35/175
PLE10P8C × S	30/160	82S181C N3	35/175
8K 2K × 4			
63S841	50/150	82S185A	50/155
63S841A	35/150	82S185C	35/155
PLE11P4C	35/150	82S185C	35/155
8K Registered 1K × 8			
63RA881	20/175	82HS189	20/175
63RA881A	15/175	82HS189A	15/175
16K 2K × 8			
63S1681	50/185	82S191A N	55/175
63S1681A	35/185	82S191C N	35/175
PLE11P8C	35/185	82S191C N	35/175
63S1681 × S	50/185	82S191A N3	55/175
63S1681A × S	35/185	82S191C N3	35/175
PLE11P8C × S	35/185	82S191C N3	35/175

MMI (Now AMD) (Cont'd) PART NO.	PERFORMANCE t_{AA}/I_{CC}	SIGNETICS PART NO.	PERFORMANCE t_{AA}/I_{CC}
16K 4K × 4			
63S1641	50/175	82HS195	45/155
63S1641A	35/170	82HS195A	35/155
PLE12P4C	35/175	82HS195A	35/155
32K 4K × 8			
63S3281	45/185	82HS321	45/185
63S3281A	35/190	82HS321A	35/185
PLE12P8C	35/190	82HS321A	35/185
64K 8K × 8			
63S6481	55/190	82HS641	55/185
63S6481A	45/190	82HS641A	45/185

PACKAGES	MMI Suffix	SIGNETICS Suffix
Plastic DIP	N	N
Ceramic DIP	J	F
PLCC (Plastic)	NL	A
LCC (Ceramic)	L	G
SOL	Not available	D
Plastic DIP (Skinny)	NS	N3
Ceramic DIP (Skinny)	JS	F3
Super II Burn-In	–	–B

PROM Cross Reference Guide

Fairchild (Now National Semi) PART NO.	PERFORMANCE t_{AA}/I_{CC}	SIGNETICS PART NO.	PERFORMANCE t_{AA}/I_{CC}
8K 1K × 8			
93Z451	40/135	82S181C	35/175
16K 2K × 8			
93Z511	45/175	82S191A	55/175
93Z611	25/185	82HS191	25/185
64K 8K × 8			
93Z65	55/180	82HS641	55/185
93Z65A	45/180	82HS641A	45/185
93Z667	40/185	82HS641B	35/185

PACKAGES	FSC Suffix	SIGNETICS Suffix
Plastic DIP	P	N
Ceramic DIP	D	F
PLCC (Plastic)	Not available	A
LCC (Ceramic)	L	G
SOL	Not available	D
Plastic DIP (Skinny)	SP	N3
Ceramic DIP (Skinny)	SD	F3
Super II Burn-In	-N3	-B

EPROM Cross Reference Guide

CMOS Memory Products

Most manufacturers of EPROMs use the same part numbering system with only prefix changes to denote manufacturers and suffix changes to denote packages.

EPROM PACKAGES CROSS REFERENCE

	PACKAGE SUFFIXES								
	AMD	**INTEL**	**ALTERA**	**TI**	**MMI**	**NSC**	**FUJITSU**	**HITACHI**	**SIGNETICS**
DIP (Plastic)	PD	P	P	N	N	N	P	DP	N
DIP (Ceramic)	CD		D	J	J	J	C	DG	F
PLCC (Plastic)	PL	N	L	FN	NL			CG	A
CLCC (Ceramic)	CL/CLR	R	J	FK	L				G
300 DIP (Plastic)				NT	NS			DP	N3
300 DIP (Ceramic)				JT	JS			DG	F3
600 DIP (Ceramic)				JW					F
600 DIP (Plastic)				NW					N
DIP (Ceramic) (with window)			JLCC			Q		DG	FA
DIP (Ceramic) (Side-Brazed)				JD	D	D			I

EPROM Programming Information

CMOS Memory Products

Complete programming system specifications are available upon request from Signetics Memory Marketing.

Signetics encourages the purchase of programming equipment from a manufacturer who has a full line of programming products to offer. Signetics also encourages the manufacturers of EPROM programming equipment to submit their equipment for verification of electrical parameters and programming procedures. Information on manufacturers offering equipment certified by Signetics is available upon request from Signetics Memory Marketing.

PROGRAMMING THE 27HC641

Initially, all bits of the 27HC641 are in an undefined state. Data is introduced by programming "1"s and "0"s into the desired bit locations. Both "1"s and "0"s must be present in the data word to define each bit. Since the 27HC641 is shipped in a virgin (undefined) state, it is recommended that all locations be programmed to remove ambiguous states.

The 27HC641 is in the programming mode when the Output Enable ($\overline{G}$) pin is at 12.5V. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are standard TTL logic levels.

PROGRAMMING THE 27C64A

Caution: Exceeding 14.0V on the V_{PP} Pin may permanently damage the 27C64A.

Initially, all bits of the 27C64A are in the "1" state. Data is introduced by selectively programming "0"s into the desired bit locations. Although only "0"s will be programmed, both "1"s and "0"s can be present in the data word.

The 27C64A is in the programming mode when the V_{PP} input is at 12.5V, and $\overline{CE}$ and $\overline{PGM}$ is at TTL Logic Low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are standard TTL logic levels.

PROGRAMMING THE 27HC128

Caution: Exceeding 14.0V on the V_{PP} Pin may permanently damage the 27HC128.

Initially, all bits of the 27HC128 are in an undefined state. Data is introduced by programming "1"s and "0"s into the desired bit locations. Both "1"s and "0"s must be present in the data word to define each bit.

The 27HC128 is in the programming mode when the Output Enable ($\overline{G}$) pin is at 12.5V. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are standard TTL logic levels.

PROGRAMMING THE 27C256

Caution: Exceeding 14.0V on V_{PP} Pin may permanently damage the 27C256.

Initially, all bits of the 27C256 are in the "1" state. Data is introduced by selectively programming "0"s into the desired bit locations. Although only "0"s will be programmed, both "1"s and "0"s can be present in the data word.

The 27C256 is in the programming mode when the V_{PP} input is at 12.5V, $\overline{CE}$ is at TTL Logic Low, and $\overline{OE}$ is at TTL Logic High. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are standard TTL logic levels.

PROGRAMMING THE 27C512

Caution: Exceeding 14.0V on the $\overline{OE}/V_{PP}$ Pin may permanently damage the 27C512.

Initially, all bits of the 27C512 are in the "1" state. Data is introduced by selectively programming "0"s into the desired bit locations. Although only "0"s will be programmed, both "1"s and "0"s can be present in the data word.

The 27C512 is in the programming mode when the $\overline{OE}/V_{PP}$ input is at 12.75V and $\overline{CE}$ is at TTL Logic Low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are standard TTL logic levels.

PROGRAMMING THE 27C210

Caution: Exceeding 14.0V on V_{PP} Pin may permanently damage the 27C210.

Initially, all bits of the 27C210 are in the "1" state. Data is introduced by selectively programming "0"s into the desired bit locations. Although only "0"s will be programmed, both "1"s and "0"s can be present in the data word.

The 27C210 is in the programming mode when the V_{PP} input is at 12.5V, $\overline{CE}$ and $\overline{PGM}$ is at TTL Logic Low, and $\overline{OE}$ is at TTL Logic High. The data to be programmed is applied 16 bits in parallel to the data output pins. The levels required for the address and data inputs are standard TTL logic levels.

EPROM Programming Information

SIGNETICS EPROM PROGRAMMER REFERENCE GUIDE
Data I/O Corporation
10524 Willows Road, N.E.
Redmond, Washington 98073–9746
Telephone Number: (800) 247–5700

DEVICE	PKG TYPE	FAMILY PINOUT	MODEL 29				SERIES 22	S1000	
			UNIPAK 2	UNIPAK 2B	351B	GANG PAK		REV	SR
27C64A	DIP	5C33	V16	V16	086	V08	--	V13	28
27C64A	DIP	9333	--	--	--	--	--	--	-
27C64A	PLCC	5CC1	--	V18	099	--	V05	--	-
27HC641	DIP	3533	--	--	--	--	--	V14	28
27HC641	DIP	8767	V15	V15	--	V08	--	V14	28
27HC641	PLCC	879A	--	V15	093	--	--	--	-
27C256	DIP	05CF32	--	--	--	--	--	V13	28
27C256	DIP	9332	--	--	--	--	--	--	-
27C256	DIP	5C32	V16	V16	086	V08	--	--	-
27C256	PLCC	5CC3	--	V18	099	--	--	--	-
27C512	DIP	5EA4	V18	V18	086	--	--	V13	-
27C512	PLCC	5EC4	--	V19	099	--	--	V13	*
27C210	DIP	5FA8	V19	V19	095	--	--	V13	40
27C210	PLCC	5F88	--	V19	095P	--	--	V13	*

*Contact Mr. Lloyd Hyden/Data I/O for PLCC Rails.

EPROM Programming Information

UNISITE							MODEL 60		
REV	PLCC	SET SITE	280	201	288	MOD.	REV	360A	BOARD SITE
2.2	----	V2.2	--	--	--	-	--	--	01
--	----	--	VO4	V04	VO1	32	V10	005	--
2.5	CPST	--	--	--	--	-	--	--	01
--	----	--	--	--	1.2	-	--	--	--
2.8	----	--	--	--	--	-	--	--	--
2.8	CPST	--	--	--	--	-	--	--	--
--	----	--	--	--	--	-	--	--	--
2.2	----	V2.2	V04	V04	V01	32	V10	005	--
--	----	--	V04	V04	--	-	--	--	01
2.4	CPST	--	--	--	--	-	--	--	01
2.5	----	V2.5	--	--	--	-	V13	005	--
2.7	CPST	--	--	--	--	-	--	--	--
2.7	----	--	--	--	--	-	--	--	--
2.7	CPST	--	--	--	--	-	--	--	--

ERASURE CHARACTERISTICS

The erasure characteristics are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000 – 4000 Å range. Data shows that constant exposure to room level fluorescent lighting could erase the typical EPROM in approximately three years, while it would take approximately one week to cause erasure when exposed to direct sunlight. If the EPROM is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure for EPROMs is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15Wsec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12,000μW/cm^2 power rating. The package should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose a Signetics EPROM can be exposed to without damage is 7258Wsec/cm^2 (1 week @ 12000μW/cm^2). Exposure of these CMOS EPROMs to high intensity UV light for longer periods may cause permanent damage.

Note that all of the High speed EPROMs, (HCxxx), erase to an undefined state, i.e., neither "1"s or "0"s are stored after erasure. Both "1"s and "0"s *MUST* be programmed into the devices for proper operation.

INTELLIGENT IDENTIFIER

The intelligent identifier provides the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is functional in the 25°± 5°C ambient temperature range. To activate this mode, the equipment must force 11.5V to 12.5V on address A_9. Two bytes may then be read from the device outputs by toggling address line A_0 from V_{IL} to V_{IH}. The $\overline{CE}$, $\overline{OE}$ and all other address lines must be at V_{IL} during interrogation.

The identifier information for Signetics' 27C64A is as follows:

When $A_0 = V_{IL}$	
data is "Manufacturer"	$15_{(HEX)}$
When $A_0 = V_{IH}$	
data is "Product"	$0B_{(HEX)}$

The identifier information for Signetics' 27C256 is as follows:

When $A_0 = V_{IL}$	
data is "Manufacturer"	$15_{(HEX)}$
When $A_0 = V_{IH}$	
data is "Product"	$8C_{(HEX)}$

The identifier information for Signetics' 27C512 is as follows:

When $A_0 = V_{IL}$	
data is "Manufacturer"	$15_{(HEX)}$
When $A_0 = V_{IH}$	
data is "Product"	$1D_{(HEX)}$

The identifier information for Signetics' 27C210 is as follows:

When $A_0 = V_{IL}$	
data is "Manufacturer"	$FF15_{(HEX)}$
When $A_0 = V_{IH}$	
data is "Product"	$FF17_{(HEX)}$

Bipolar Programming Procedures

GENERIC I PROGRAMMING

The Signetics family of Advanced Junction Isolated Schottky PROMs are high performance bipolar devices which use a nickel/chromium (NiCr) alloy fuse to provide the many benefits of field programming. Programming is accomplished by application of voltages above those used for normal operation, therefore, no special pins are required for programming (except the 82S115 which has two fusing pins: FE1 and FE2). The programming voltages and timing requirements make unintentional programming virtually impossible. Arrays of devices may be programmed in the user's circuit, if desirable, as long as proper application of programming voltages is provided.

GENERIC I PROCEDURE

The Generic I family of Schottky PROMs uses no special pins for programming. The address pins remain TTL compatible during the programming procedure and are used to select the unique word to be programmed. The outputs are used to supply fusing current during the programming mode as well as selection of the bit to be programmed. Programming is performed one bit at a time. The programming mode is evoked by raising the V_{CC} pin to 8.75 ± 0.25V. This voltage is referred to as V_{CCP}. After the proper delay the output corresponding to the bit selected is raised to 17.5 ± 0.5V. This voltage is known as V_{OPF} and must be supplied by a voltage source with a low impedance and very fast transient response. Reliable programming depends on the V_{OPF} power supply and circuitry. I_{OPF} is the current which will be drawn by the part during the programming sequence. Again, after the proper delay the chip enable CE is pulsed to a TTL "0" level for 10 to 25μs. It is during this time that the actual fusing of the NiCr link occurs. The actual time for fusing of a Signetics NiCr fuse link has been determined to be between 0.6 to 1.2μs. The shorter the fusing pulse (CE), within the recommended limits, the sooner the total programming sequence is completed. Note that unprogrammed Generic I (Junction Isolated) parts are supplied with all bits at a logic "0" level. Only the bits intended to be "ones" will be programmed. Verification of programming can be performed after each bit or after the entire device has been programmed. A fuse which does not blow during the first programming cycle should be considered a defective device and should be discarded.

GENERIC II PROGRAMMING

The Signetics family of Oxide Isolated Schottky PROMs are high performance bipolar devices which use a vertical diode fuse to provide the benefits of field programming. Programming is accomplished by application of voltages above those used for normal operation, therefore, no special pins are required for programming. The programming voltages and timing requirements make unintentional programming virtually impossible.

GENERIC II PROCEDURE

As with the Generic I devices, the addresses remain TTL compatible during the programming procedure and are used to select the unique word to be programmed. The outputs are used to supply fusing current during the programming mode as well as selection of the bit to be programmed. Programming is performed one bit at a time. The programming mode is evoked by raising the V_{CC} pin to 8.75 ± 0.25V. This voltage is referred to as V_{CCP}. After the proper delay the output corresponding to the bit selected is raised to 20.0 ± 0.5V. This voltage is known as V_{OPF} and must be supplied by a voltage source with a low impedance and very fast transient response. Reliable programming depends on the V_{OPF} power supply and circuitry. I_{OPF} is the current which will be drawn by the part during the programming sequence. Again, after the proper delay the chip enable CE is pulsed to a TTL "0" level for 1μs. The properly blown fuse will verify the TTL "0" level. Note that unprogrammed Generic II (Oxide Isolated) parts are supplied with all bits at a logic "1" level. Only the bits intended to be "zeros" will be programmed.

GENERIC III PROGRAMMING

The Signetics Generic III PROM family consist of those devices constructed with Oxide Isolated Schottky circuitry using Titanium Tungsten horizontal fuses. This results in a very high performance PROM at an optimum cost of manufacture. Programming is accomplished by application of voltages above those used for normal operation, therefore, no special pins are required for programming. The programming voltages and timing requirements make unintentional programming virtually impossible.

GENERIC III PROCEDURE

As with the Generic I devices, the addresses remain TTL compatible during the programming procedure and are used to select the unique word to be programmed. The outputs are used to supply fusing current during the programming mode as well as selection of the bit to be programmed. Programming is performed one bit at a time. The programming mode is evoked by raising the V_{CC} pin to 8.75 ± 0.25V. This voltage is referred to as V_{CCP}. After the proper delay the output corresponding to the bit selected is raised to 14.25 ± 0.25V. This voltage is known as V_{OPF} and must be supplied by a voltage source with a low impedance and very fast transient response. Reliable programming depends on the V_{OPF} power supply and circuitry. I_{OPF}, approximately 300mA, is the current which will be drawn by the part during the programming sequence. Again, after the proper delay the chip enable CE is pulsed to a TTL "0" level for 5μs. The properly blown fuse will verify the TTL "1" or "High" level. Note that unprogrammed Generic III parts are supplied with all bits at a logic "0" or "Low" level. Only the bits intended to be "Ones" will be programmed.

GENERIC IV PROGRAMMING

The Signetics family of ECL PROMs are bipolar devices which use a nickel/chromium (NiCr) alloy fuse, or as in the case of the newest members a Titanium Tungsten (TiW) fuse. Both of these designs are programmed using the same Generic IV method.

GENERIC IV PROCEDURE

Unlike previous methods the addresses used to select the proper word are unique voltage levels which become necessary when the V_{CC} pin is raised to a positive voltage. (ECL normal mode of operation is with the V_{CC} pin held to ground potential.) The outputs are used to supply fusing current during the programming mode as well as select the bit to be programmed. Programming is performed one bit at a time. The programming mode is evoked by raising the V_{CC1} pin to 11.5 ± 0.5V. This voltage is referred to as V_{CCP}. After the proper delay the output corresponding to the bit selected is raised to

12 ± 0.5V for 10μs. The properly blown fuse will verify a "High" level of 4.4V min. Note that unprogrammed Generic IV devices are supplied with all bits at a logic "Low" level. Only the bits intended to be "High" will be programmed.

PROGRAMMING INFORMATION

Complete programming system specifications are available upon request from the Memory Marketing department. Signetics encourages the purchase of programming equipment from a manufacturer who has a full line of programming products to offer. Signetics also encourages the manufacturers of programming equipment to submit their equipment for verification of electrical parameters and programming procedures. Information on manufacturers offering equipment certified by Signetics is available upon request from the Memory Marketing department.

SIGNETICS DISCOURAGES THE CONSTRUCTION AND USE OF "HOMEMADE" PROGRAMMING EQUIPMENT

In order to consistently achieve excellent programming yields, periodic calibration of the programming equipment is required. Consult the equipment manufacturer for the recommended calibration interval. Records of programming yield, by device type, should be kept and any downward trend or sudden change should be considered as an indication of a need to recalibrate the programming equipment.

PROM Programming Information

SIGNETICS PROM PROGRAMMER REFERENCE GUIDE

Data I/O Corporation
10524 Willows Road, N.E.
Redmond, Washington 98073–9746
Telephone Number: (800) 247–5700

SIGNETICS PART #	PACKAGE	PIN CODE	MODEL 29B				SERIES 22	ADAPTOR	UNISITE 40	ADAPTOR
			UNI–PACK2	ADAPTOR	UNI–PACK2B	351B				
100149A	DIP	B1D7	--	-----	--	-----	--	-----	V2.0	-----
10149A	DIP	B1D7	--	-----	--	-----	--	-----	V2.0	-----
82HS187/189	DIP	CE5C	V12	-----	V12	-----	V03	-----	V2.2	-----
82HS191	DIP	CE21	V12	-----	V12	-----	--	-----	V2.4	-----
82HS191	PLCC	CE8B	--	-----	V18	093	--	-----	V2.4	CPSITE
82HS195 A/B	DIP	CF53	V12	-----	V12	-----	V03	351A064	V2.2	-----
82HS195 A/B	PLCC	CE8C	--	-----	V14	090	--	-----	V2.2	CPSITE
82HS321	DIP	CF63	V12	-----	V12	-----	V03	-----	V2.2	-----
82HS321	PLCC	CF8E	--	-----	V17	093	--	-----	V2.4	CPSITE
82HS641	DIP	CE67	V12	-----	V12	-----	V03	-----	V2.2	-----
82HS641	PLCC	CE9A	--	-----	V14	093	--	-----	V2.2	CPSITE
82LHS191	DIP	CE21	V12	-----	V12	-----	--	-----	V2.4	-----
82LHS321	DIP	CF63	V12	-----	V12	-----	V03	V03	V2.2	-----
82LHS321	PLCC	CF8E	--	-----	V17	093	--	-----	V2.4	CPSITE
82LS135	DIP	1008	V03	-----	V07	-----	V02	351A064	V1.4	-----
82S115	DIP	AE83	V07	351A068	V07	-----	V02	-----	V1.1	-----
82S123	DIP	1002	V04	-----	V07	-----	V02	351A064	V1.4	-----
82S123	DIP	106C	--	-----	V15	-----	--	-----	--	-----
82S123	SO	010802	--	-----	--	-----	--	-----	V1.6	CPSITE
82S123	PLCC	010702	--	-----	V15	087	--	-----	V1.6	CPSITE
82S126	DIP	1001	V03	-----	V07	-----	V02	351A064	V1.7	-----
82S129	DIP	1001	V03	-----	V07	-----	V02	-----	V1.7	-----
82S129	PLCC	106B	--	-----	--	-----	--	-----	V2.5	CPSITE
82S130	DIP	1003	V03	-----	V07	-----	V02	351A064	V1.7	-----
82S130	PLCC	106D	--	-----	V18	088	--	-----	V2.4	CPSITE
82S131	DIP	1003	V06	-----	V07	-----	V02	351A064	V1.7	-----
82S131	PLCC	106D	--	-----	V18	088	--	-----	V2.4	CPSITE
82S135	DIP	1008	V03	-----	V07	-----	V02	351A064	V1.4	-----
82S137	DIP	1005	V03	-----	V07	-----	V02	351A064	V1.4	-----
82S137	PLCC	106E	--	-----	V18	088	--	-----	--	-----
82S141	DIP	1015	V03	-----	V07	-----	V02	-----	V1.4	-----
82S141	PLCC	107F	--	-----	V18	093	--	-----	V2.4	CPSITE
82S147	DIP	1009	V03	-----	V07	-----	V02	351A064	V1.4	-----
82S147	PLCC	107C	--	-----	V18	089	--	-----	V2.4	CPSITE
82S181	PLCC	108A	--	-----	V18	093	--	-----	V2.4	CPSITE
82S181/183	DIP	1016	V03	-----	V07	-----	V02	-----	V1.4	-----
82S183	PLCC	108A	--	-----	--	-----	--	-----	V2.5	CPSITE
82S185	DIP	1006	V03	-----	V07	-----	V02	351A064	V1.4	-----
82S191	DIP	1021	V03	-----	V07	-----	V02	-----	V1.4	-----
82S191	PLCC	108B	--	-----	V18	093	--	-----	V2.4	CPSITE
82S23	DIP	1002	V03	-----	V07	-----	V02	351A064	V1.8	-----
82S23	PLCC	010702	--	-----	V15	087	--	-----	V1.6	CPSITE
82S23	SO	010802	--	-----	--	-----	--	-----	V1.4	CPSITE
82US123	DIP	0E02	V15	-----	V15	-----	--	-----	V2.1	-----
82US123	PLCC	0E6C	--	-----	V18	087	--	-----	V2.4	CPSITE
82US23	DIP	0E02	V15	-----	V15	-----	--	-----	V2.1	-----
82US23	PLCC	0E6C	--	-----	V18	087	--	-----	V2.4	CPSITE

MOS MEMORIES

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CMOS STATIC RAM

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8192 X 8-BIT LATCHED STATIC RAM

GENERAL DESCRIPTION

The FCB51C64/65 are 65 536-bit latched static RAMs organized as 8192 words of 8 bits each. Both memory devices are available with TTL (/64) and CMOS (/65) I/O and in standard 600 mil DIL28 and 330 mil SO28 packages.

The devices can operate from a power supply between 2 and 6 V with an access time of between 70 and 150 ns, depending on the supply voltage.

The memories are latched, which means the address must be clocked into the address latch. For every address change a latch clock pulse must be applied to either $\overline{CE1}$, (active going negative) with CE2 high or, to CE2, (active going positive) with $\overline{CE1}$ low. During the time preceding the active latch transition the memory is disabled.

Features

- Full CMOS 6 transistor memory cell
- Power supply 2 to 6 V
- Access times: 150 ns at 2 V, 70 ns at 4.5 V and 65 ns at 6 V
- Active power supply current: 10 mA at 2 V, 40 mA at 4.5 V and 60 mA at 6 V
- Standby current: 2 mA maximum for TTL input
  2 μA maximum for CMOS input

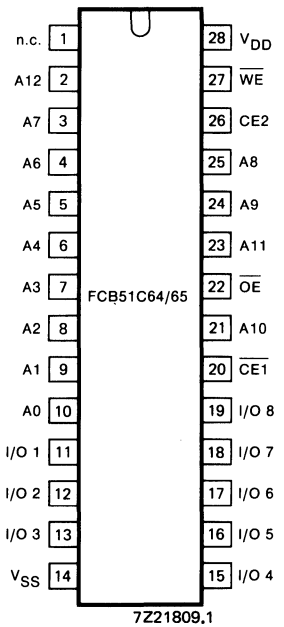


Fig.1 Pinning diagram.

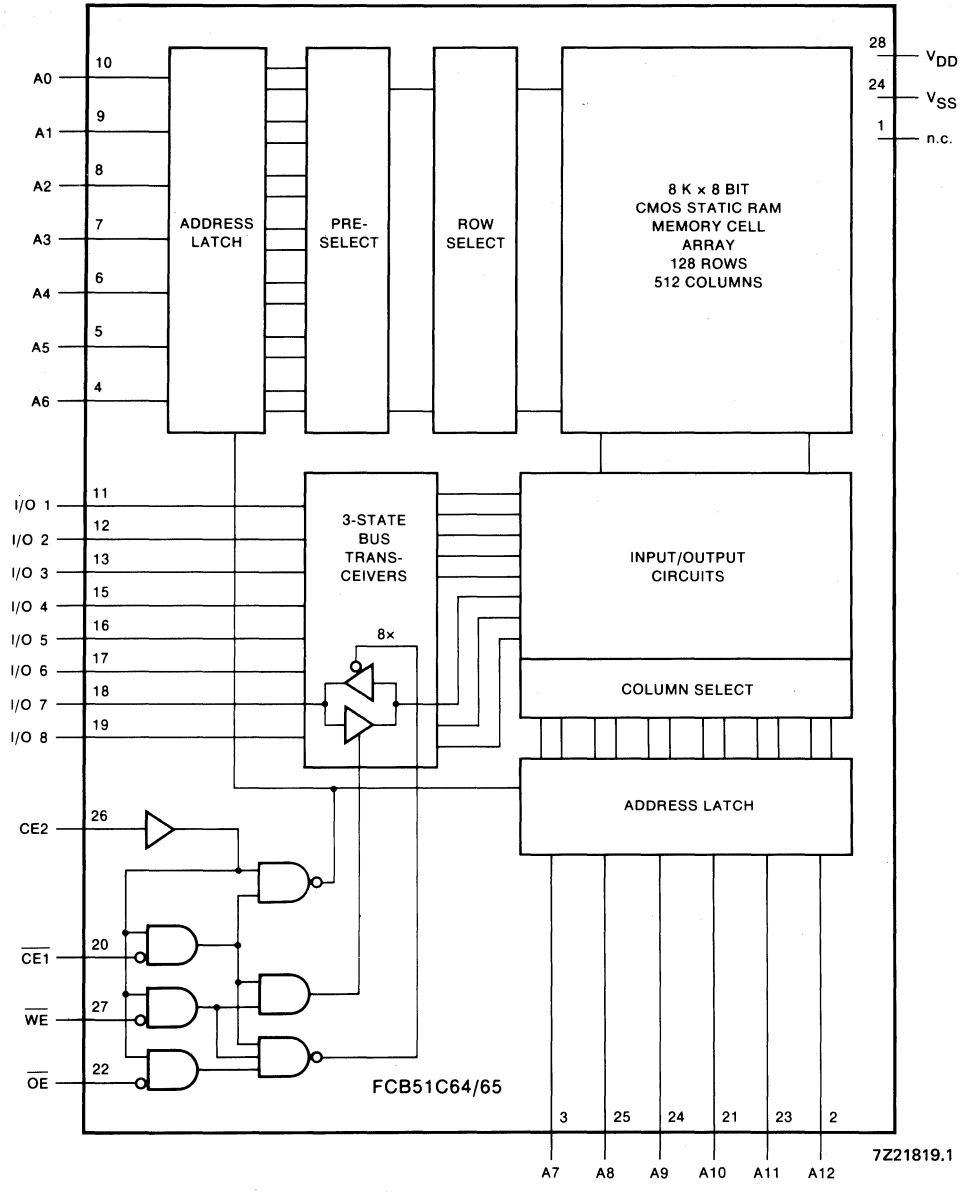


Fig.2 Block diagram.

Philips Components

Data sheet	
status	Product specification
date of issue	June 1990

FCB61C65(L/LL)

8 K x 8 Fast CMOS low-power static RAM

FEATURES

- Operating supply voltage 5 V ± 10%
- Inputs and outputs ESD protected
- Automatic power-down after a completed read access
- Access time: 55 ns and 70 ns
- Low current consumption:
  - active 70 mA max.
  - standby (TTL) 3 mA max.
  - standby (CMOS) 100 µA max. (L-version)
  - standby (CMOS) 1 µA max. (LL-version)
- Suitable for battery back-up operation: (FCB61C65L/LL only)
  - data retention voltage 2 V min.
  - data retention current 50 µA max. (L-version)
  - data retention current 1 µA max. (LL-version)
- Latched data outputs giving stable data between consecutive accesses
- Easy memory expansion
- Common data I/O interface
- All inputs and outputs TTL and CMOS compatible
- All inputs have a Schmitt trigger switching action
- Three-state outputs
- Operating temperature 0 °C to +70 °C

GENERAL DESCRIPTION

The FCB61C65(L/LL) is a 65536-bit fast, low-power, static random access memory organized as 8192 words of 8 bits each.

The chip enable inputs $\overline{CE}1$ and CE2 are available for memory expansion and to control the low-power/ standby mode.

The device operates from a 5 V power supply and has an access time of 55 ns and 70 ns.

The FCB61C65(L/LL) is ideally suited for memory applications where fast access time, low power and ease of use are required.

The FCB61C65(L/LL) is a CMOS device which uses a 6 transistor memory cell.

The IC is fabricated in a CMOS double-metal single-poly process using ion-implanted silicon gate technology.

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
FCB61C65 (L/LL)-XXP	28	DIL (600 mil)	plastic	SOT117
FCB61C65 (L/LL)-XXT	28	SOXL (330 mil)	plastic	SOT213

8 K x 8 Fast CMOS low-power static RAM FCB61C65(L/LL)

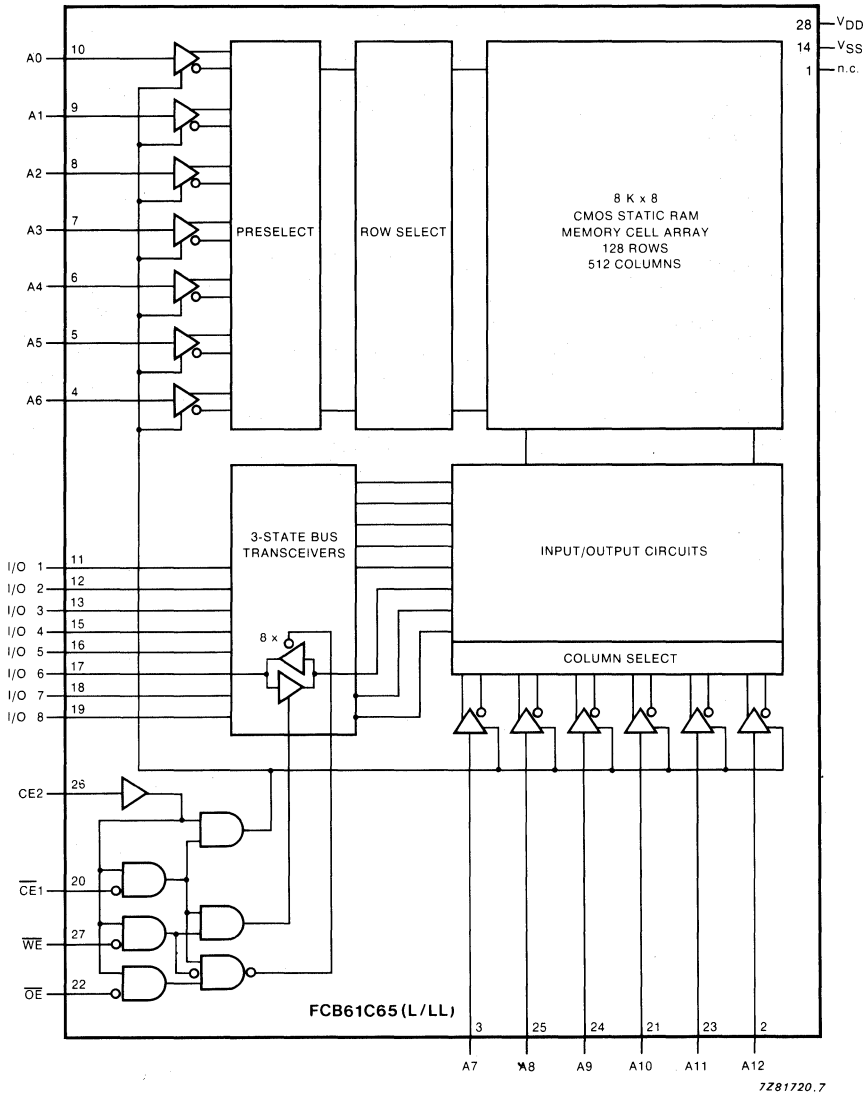


Fig.1 Block diagram.

8 K x 8 Fast CMOS low-power static RAM FCB61C65(L/LL)

TRUTH TABLE

$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	MODE	I_{DD}	I/O PIN	REF. CYCLE
H	X	X	X	not selected	I_{SB}*	HIGH Z	
X	L	X	X	not selected	I_{SB}*	HIGH Z	
L	H	L	H	read	I_{DD}/I_{DD1}*	D OUT	read
L	H	H	L	write	I_{DD}	D IN	write
L	H	L	L	write	I_{DD}	D IN	write
L	H	H	H	ready-read	I_{DD}/I_{DD1}*	HIGH Z	

* Including L/LL versions if input levels are CMOS.

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
A12	2	address input
A7 to A0	3 to 10	address inputs
I/O 1 to I/O 3	11 to 13	data inputs/outputs
V_{SS}	14	ground
I/O 4 to I/O 8	15 to 19	data inputs/outputs
$\overline{CE1}$	20	chip enable 1
A10	21	address input
$\overline{OE}$	22	output enable
A11, A9, A8	23 to 25	address inputs
CE2	26	chip enable 2
$\overline{WE}$	27	write enable
V_{DD}	28	+5 V supply

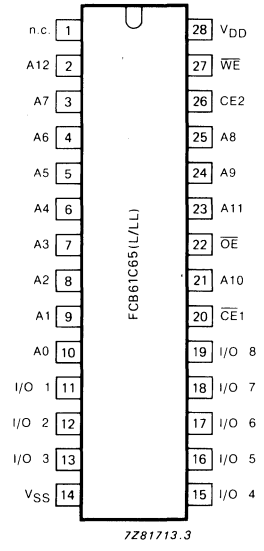


Fig.2 Pinning diagram.

DECOUPLING ARRANGEMENTS

The FCB61C65(L/LL) is an address activated circuit. When an address change occurs, the operation is executed by an internal pulse generated from the Address Transition Detector (ATD). The current variation following an address or chip enable change may induce noise on the supply lines. This noise can be eliminated using a 100 nF capacitor with good high frequency characteristics as close as possible to the memory between V_{DD} and V_{SS}.

LIMITING VALUES

Limiting values are in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_I	voltage range on any pin with respect to V_{SS}	DC inputs	−0.5	+7.0	V
V_I		max. pulse width = 50 ns	−1.5	+7.0	V
T_{amb}	operating ambient temperature		0	+70	°C
T_{bias}	temperature range with bias		−10	+85	°C
T_{stg}	storage temperature range		−55	+125	°C
P_{tot}	total power dissipation		-	1	W

Note

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to operation under the conditions specified in the DC and timing characteristics. Exposure to higher than the rated voltages for extended periods of time could effect device reliability.

HANDLING

Input and outputs are protected against electro static discharge in normal handling, however, to be totally safe it is desirable to take normal precautions appropriate to handling MOS devices.

RECOMMENDED OPERATION CONDITIONS

T_{amb} = 0 to +70 °C

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	4.5	5.5	V
V_{IH}	input voltage HIGH	2.2	V_{DD}+0.5	V
V_{IL}	input voltage LOW	−0.5*	0.8	V

* V_{IL} = −1.5 V for a maximum pulse width of 50 ns.

DC CHARACTERISTICS

V_{DD} = 5 V ± 10%; T_{amb} = 0 to 70 °C. Typical readings taken at V_{DD} = 5 V; T_{amb} = 25 °C. All voltages are referenced to V_{SS} (0 V) unless otherwise specified. DC characteristics are valid after thermal equilibrium has been established.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{LI}	input leakage current	$V_I = V_{SS}$ to V_{DD}	−1	-	1	µA
I_{LO}	output leakage current	$\overline{CE1}$ or $\overline{OE}$ = V_{IH} or CE2 = V_{IL}; $V_{I/O} = V_{SS}$ to V_{DD}	−1	-	1	µA
I_{DD}	average operating current	cycle time 55 ns; 100% duty factor; note 1 $I_{I/O}$ = 0 mA	-	40	70	mA
I_{DD}	average operating current	cycle time 70 ns; 100% duty factor; note 1 $I_{I/O}$ = 0 mA	-	35	60	mA
I_{DD1}	DC operating current	$\overline{WE}$ = V_{IH}; $I_{I/O}$ = 0 mA; f = 0 Hz	-	3	6	mA
		$\overline{WE}$ = CMOSH; V_I = CMOS; note 2				
I_{DDL}	FCB61C65L only		-	2	100	µA
I_{DDLL}	FCB61C65LL only		-	0.05	1.0	µA
I_{SB}	standby current	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL}	-	1.5	3.0	mA
		$\overline{CE1}$ = CMOSH and CE2 = CMOS or CE2 = CMOSL				
I_{SBL}	FCB61C65L only		-	2	100	µA
I_{SBLL}	FCB61C65LL only		-	0.05	1.0	µA
V_{OL}	output voltage LOW	I_{OL} = 4 mA	-	-	0.4	V
V_{OL}	output voltage LOW	I_{OL} = 20 µA	-	-	0.2	V
V_{OH}	output voltage HIGH	I_{OH} = −1 mA	2.4	-	-	V
V_{OH}	output voltage HIGH	I_{OH} = −20 µA	V_{DD}−0.2	-	-	V

Notes to the DC characteristics

1. $I_{DD} \leq 50$ mA at a cycle time of 100 ns and ≤ 45 mA at a cycle time of 120 ns.

2. CMOS = CMOSH: $V_{DD} - 0.2\ V \leq$ level $\leq V_{DD} + 0.2\ V$ or
   CMOSL: $-0.2\ V \leq$ level $\leq +0.2\ V$.

CAPACITANCES

f = 1 MHz; T_{amb} = 25 °C (parameters in this table are sampled and not 100% tested).

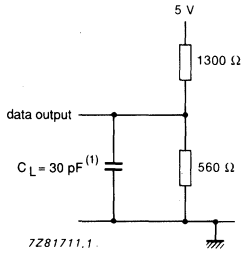
SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
	input capacitance			
C_I	$\overline{CE1}$, CE2, $\overline{WE}$, $\overline{OE}$	V_I = 0 V	8	pF
C_I	all other inputs	V_I = 0 V	7	pF
$C_{I/O}$	input/output capacitance	$V_{I/O}$ = 0 V	8	pF

TIMING CHARACTERISTICS

V_{DD} = 5 V ± 10%; T_{amb} = 0 to 70 °C; inputs pulse levels = 0.4 to 2.4 V; input rise and fall times = 5 ns; input and output timing reference levels = 1.5 V and output loading as in Figure 3; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	55 TYPE		70 TYPE		UNIT
			MIN.	MAX.	MIN.	MAX.	
Read cycle							
t_{RC}	read cycle time		55	-	70	-	ns
t_{AA}	address access time		-	55	-	70	ns
t_{ACE}	chip enable access time		-	55	-	70	ns
t_{OE}	output enable access time		-	30	-	35	ns
t_{CLZ}	chip enable to output LOW Z	note 6	5	-	5	-	ns
t_{OLZ}	output enable to output LOW Z	note 6	5	-	5	-	ns
t_{CHZ}	chip disable to output HIGH Z	note 6	-	30	-	30	ns
t_{OHZ}	output disable to output HIGH Z	note 6	-	30	-	30	ns
t_{OH}	output hold time		10	-	10	-	ns
Write cycle							
t_{WC}	write cycle time		55	-	70	-	ns
t_{CW}	chip enable to end of write	note 11	50	-	65	-	ns
t_{AW}	address valid to end of write		50	-	65	-	ns
t_{AS}	address set up time		0	-	0	-	ns
t_{WP}	write pulse width	note 9	30	-	35	-	ns
t_{WR}	write recovery time	note 10	0	-	0	-	ns
t_{WHZ}	write enable to output HIGH Z	note 16	-	20	-	25	ns
t_{DW}	data to write time overlap		25	-	30	-	ns
t_{DH}	data hold from write time		5	-	5	-	ns
t_{OW}	end of write to output LOW Z	note 16	5	-	5	-	ns

Output load



(1) C_L = 5 pF for t_{CLZ}, t_{CHZ}, t_{WHZ}, t_{OLZ}, t_{OHZ} and t_{OW}.

Fig.3 Output load.

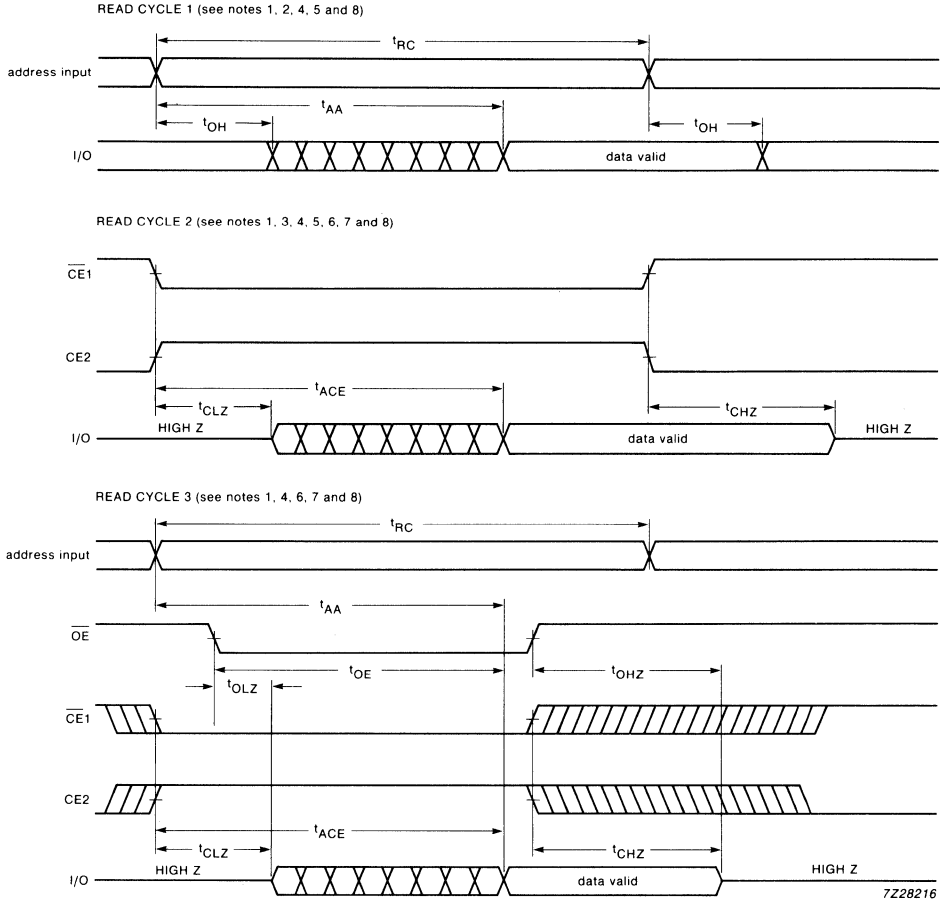


Fig.4 Read cycle timing.

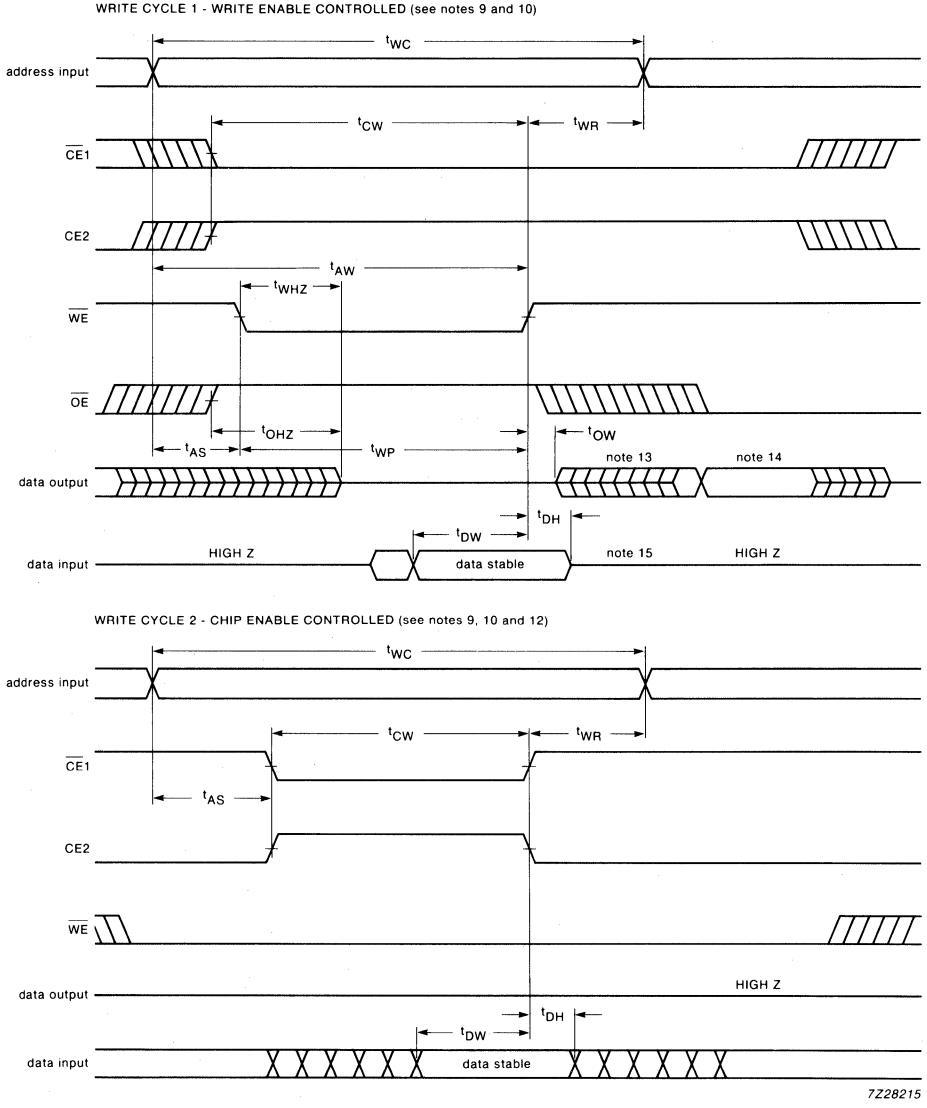


Fig.5 Write cycle timing.

Notes to the timing characteristics

Read cycle (see Fig.4)

1. $\overline{WE}$ is HIGH for read cycle.
2. Device is continuously selected, $\overline{CE}1$ is LOW and CE2 is HIGH.
3. Address is valid prior to or coincident with $\overline{CE}1$ LOW or CE2 HIGH transition.
4. When $\overline{CE}1$ is LOW and CE2 HIGH, the address inputs may not be floating.
5. $\overline{OE}$ is LOW.
6. C_L = 5 pF for t_{CLZ}, t_{CHZ}, t_{OLZ}, output transition measured at ± 200 mV from preceding steady state. These parameters are sampled and not 100% tested.
7. t_{CLZ} and t_{ACE} are measured from the last $\overline{CE}1$ going LOW or CE2 going HIGH. t_{CHZ} is measured from the first of $\overline{CE}1$ going HIGH or CE2 going LOW.
8. If D OUT in two consecutive read cycles is the same, D OUT remains stable.

Write cycle (see Fig.5)

9. A write occurs during an overlap of LOW $\overline{CE}1$, a HIGH CE2 and a LOW $\overline{WE}$.
10. t_{WR} is measured from the earlier of CE2 going to LOW or $\overline{CE1}$ or $\overline{WE}$ going HIGH at the end of a write cycle.
11. If the $\overline{CE}1$/CE2 transition occurs simultaneously to or after the $\overline{WE}$ LOW transition the outputs remain in a high impedance state.
12. $\overline{OE}$ is continuously LOW.
13. D OUT is in the same phase as the write data of this write cycle.
14. D OUT is the read data of the next address.
15. If $\overline{CE}1$ is LOW (CE2 is HIGH) and I/O pins are in the output state during this period then input data signals of opposite phase to the outputs must not be applied.
16. C_L = 5 pF for t_{WHZ} and t_{OW}, measured at ± 200 mV from steady state. These parameters are sampled and not 100% tested.

DATA RETENTION CHARACTERISTICS FOR LOW POWER/STANDBY MODE

(FCB61C65L/LL only)

T_{amb} = 0 to +70 °C; $I_{DRL/LL}$ measurements are valid after thermal equilibrium has been established.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DR}	supply voltage for data retention	$\overline{CE1}$ = CMOSH or CE2 = CMOSL with other V_I = CMOS; note 1	2.0	-	5.5	V
	supply current during data retention	V_{DR} = 3 V; $\overline{CE2}$ = CMOSL; other V_I = CMOS or $\overline{CE1}$ = CMOSH; other V_I = CMOS				
I_{DRL}	FCB61C65L only		-	2	50	µA
I_{DRLL}	FCB61C65LL only		-	0.05	1	µA
Timing						
t_{CDR}	chip disable to data retention time		0	-	-	ns
t_R	recovery time to fully active	note 2	t_{RC}	-	-	ns

Notes to the data retention characteristics

1. CMOS = CMOSH: $V_{DR} - 0.2\ V \leq$ level $\leq V_{DR} + 0.2\ V$ or
   CMOSL: $-0.2\ V \leq$ level $\leq +0.2\ V$.

2. t_{RC} = read cycle time.

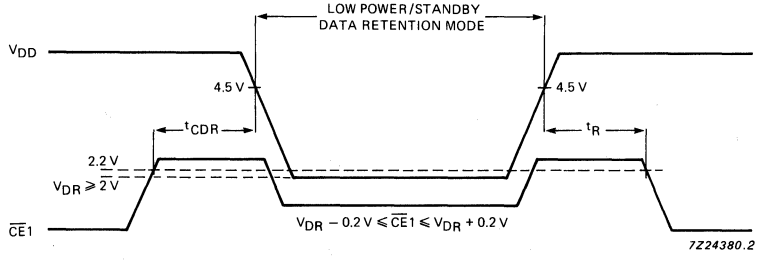


Fig.6 Data retention waveform ($\overline{CE1}$ controlled).

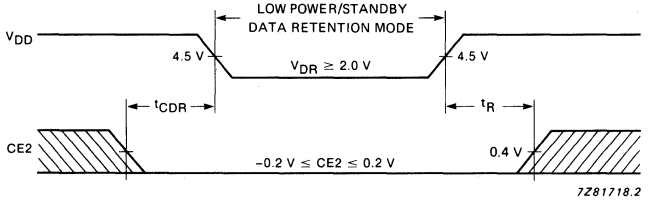


Fig.7 Data retention waveform (CE2 controlled).

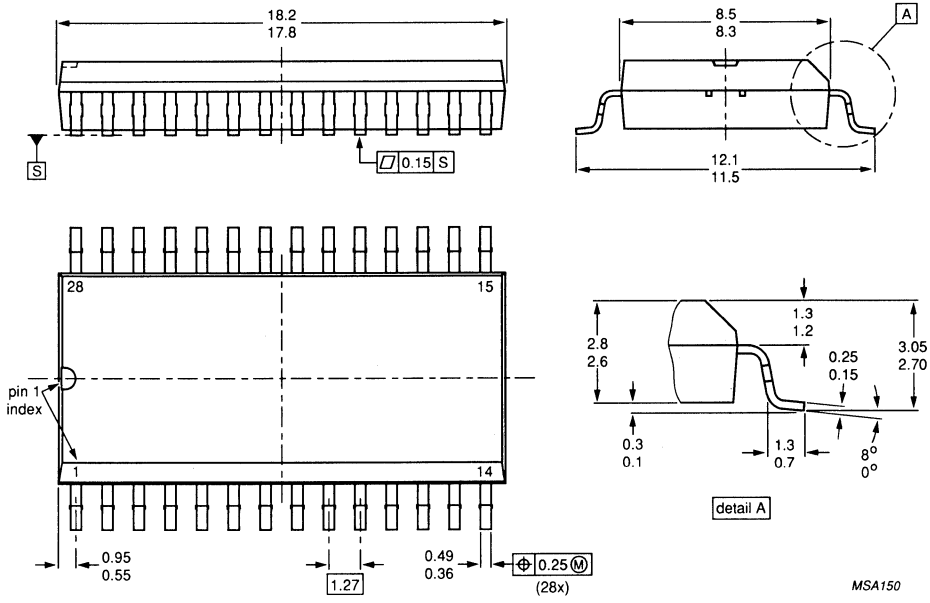


Fig.9 28-lead mini-pack; plastic (SO28XL; SOT213); conforms to IEC121E and JEDEC MO-059 AD.

262 144 X 1-BIT STATIC RAM

GENERAL DESCRIPTION

The FCB61C251 is a 256 K-bit static RAM memory organized as 262 144 words of 1 bit each.

The FCB61C251 operates from a power supply of 5 V and is available with access times of 20, 25, 35 and 45 ns.

The inputs and outputs are TTL-level compatible; with a small DC load the outputs will generate CMOS compatible levels.

The FCB61C251 is suitable for use in very large and very fast computer memories. The FCB61C251 has some unique built-in test features. These features enable the user to check if the redundancy circuits on the chip have been used; to electrically check to vendor ID code; or to put the device in a very low power mode ($I_{SB} < 10\ \mu A$). It is also possible to bypass the peripheral circuits on the chip to directly stress the memory matrix, for, for example, reliability testing.

The device is available in the standard 24-pin 300 mil DIP and SOJ packages.

Features

- Operating supply voltage: 5 V
- Access times: 20, 25, 35 and 45 ns
- Active power dissipation: 120 mA (maximum)
- Standby power: 10 mA (maximum)
- Five built-in test modes

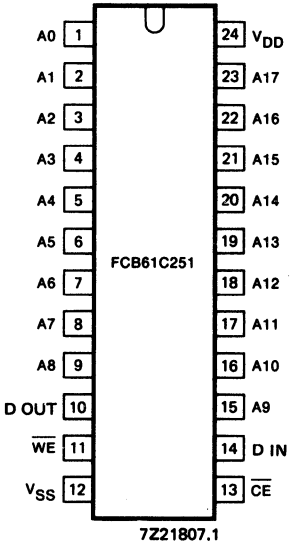


Fig.1 Pinning diagram.

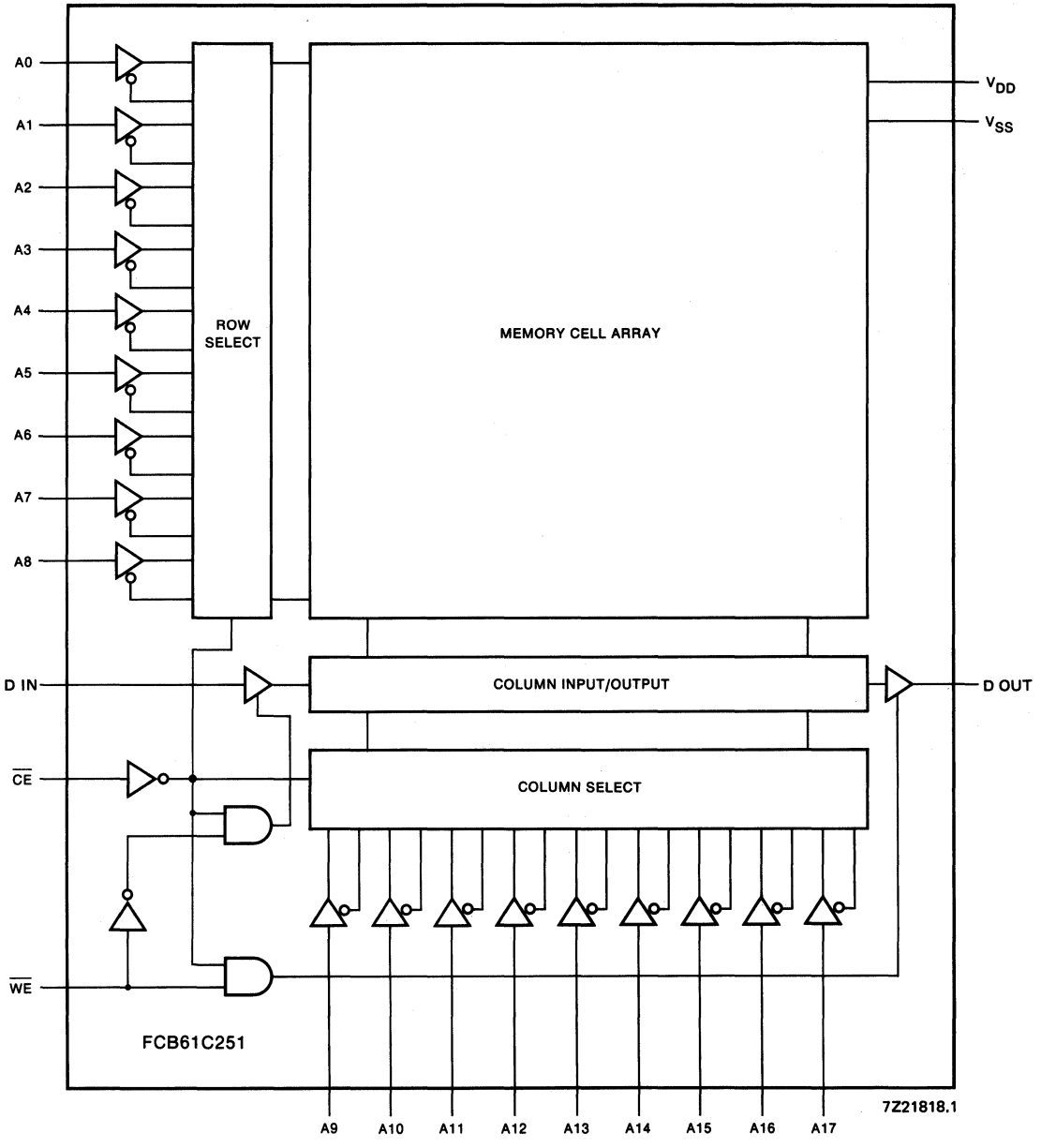


Fig.2 Block diagram.

DEVELOPMENT DATA

TRUTH TABLE

$\overline{CE}$	$\overline{WE}$	mode	V_{DD} current	output	ref. cycle
H	X	not selected	I_{SB}	HIGH Z	
L	H	read	I_{DD}	D OUT	read cycle
L	L	write	I_{DD}	HIGH Z	write cycle

DC CHARACTERISTICS

V_{DD} = 5 V ± 10%; V_{SS} = 0 V; T_{amb} = 0 to 70 °C

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_{DD}	4.5	5.0	5.5	V
Input voltage HIGH		V_{IH}	2.2	3.5	V_{DD} + 0.5	V
Input voltage LOW*		V_{IL}	−0.3	–	0.8	V
Average operating current	min. cycle, $I_{I/O}$ = 0 mA	I_{DD}	–	50	120	mA
Standby current	$\overline{CE} = V_{IH}$	I_{SB}	–	5	10	mA
Output voltage LOW	I_{OL} = 8 mA	V_{OL}	–	–	0.4	V
Output voltage LOW	I_{OL} = 20 μA	V_{OL}	–	–	0.2	V
Output voltage HIGH	I_{OH} = −4 mA	V_{OH}	2.4	–	–	V
Output voltage HIGH	I_{OH} = −20 μA	V_{OH}	V_{DD}−0.2	–	–	V

CAPACITANCE

f = 1 MHz; V_{DD} = 5 V; T_{amb} = 25 °C

parameter	conditions	symbol	typ.	max.	unit
Input capacitance	V_I = 0 V	C_I	4	6	pF
Input/output capacitance	$V_{I/O}$ = 0 V	$C_{I/O}$	5	8	pF

* V_{IL} = −3.5 V for maximum pulse width of 20 ns.

TIMING CHARACTERISTICS

V_{DD} = 5 V ± 10%; T_{amb} = 0 to 70 °C; input pulse levels = 0 to 3 V; input rise and fall times = 5 ns; input and output timing reference levels = 1.5 V; C_L = 30 pF; unless otherwise specified.

parameter	symbol	−20		−25		−35		−45		unit
		min.	max.	min.	max.	min.	max.	min.	max.	
Read cycle										
Read cycle time	t_{RC}	20	–	25	–	35	–	45	–	ns
Address access time	t_{AA}	–	20	–	25	–	35	–	45	ns
Chip enable access time	t_{ACE}	–	20	–	25	–	35	–	45	ns
Chip enable to output LOW Z*	t_{CLZ}	5	–	5	–	5	–	5	–	ns
Chip enable to output HIGH Z*	t_{CHZ}	–	10	–	15	–	15	–	15	ns
Output hold time*	t_{OH}	5	–	5	–	5	–	5	–	ns
Write cycle										
Write cycle time	t_{WC}	20	–	25	–	35	–	45	–	ns
Chip enable to end of write	t_{CW}	17	–	20	–	30	–	40	–	ns
Address valid to end of write	t_{AW}	17	–	20	–	30	–	40	–	ns
Address set-up time	t_{AS}	0	–	0	–	0	–	0	–	ns
Write pulse width	t_{WP}	15	–	15	–	25	–	35	–	ns
Write recovery time	t_{WR}	0	–	0	–	0	–	0	–	ns
Write enable to output HIGH Z*	t_{WHZ}	–	10	–	15	–	15	–	15	ns
Data to write time overlap	t_{DW}	10	–	15	–	20	–	25	–	ns
Data hold from write time	t_{DH}	0	–	0	–	0	–	0	–	ns
End of write to output LOW Z*	t_{OW}	5	–	5	–	5	–	5	–	ns

* C_L = 5 pF for t_{CLZ}, t_{CHZ}, t_{OH}, t_{WHZ} and t_{OW}. Measured at 200 mV from a steady state.

65 536 X 4-BIT STATIC RAM

GENERAL DESCRIPTION

The FCB61C252/253 are 256 K-bit static RAM memories organized as 65 536 words of 4 bits each.

The FCB61C252/253 operate from a power supply of 5 V and are available with access times of 20, 25, 35 and 45 ns.

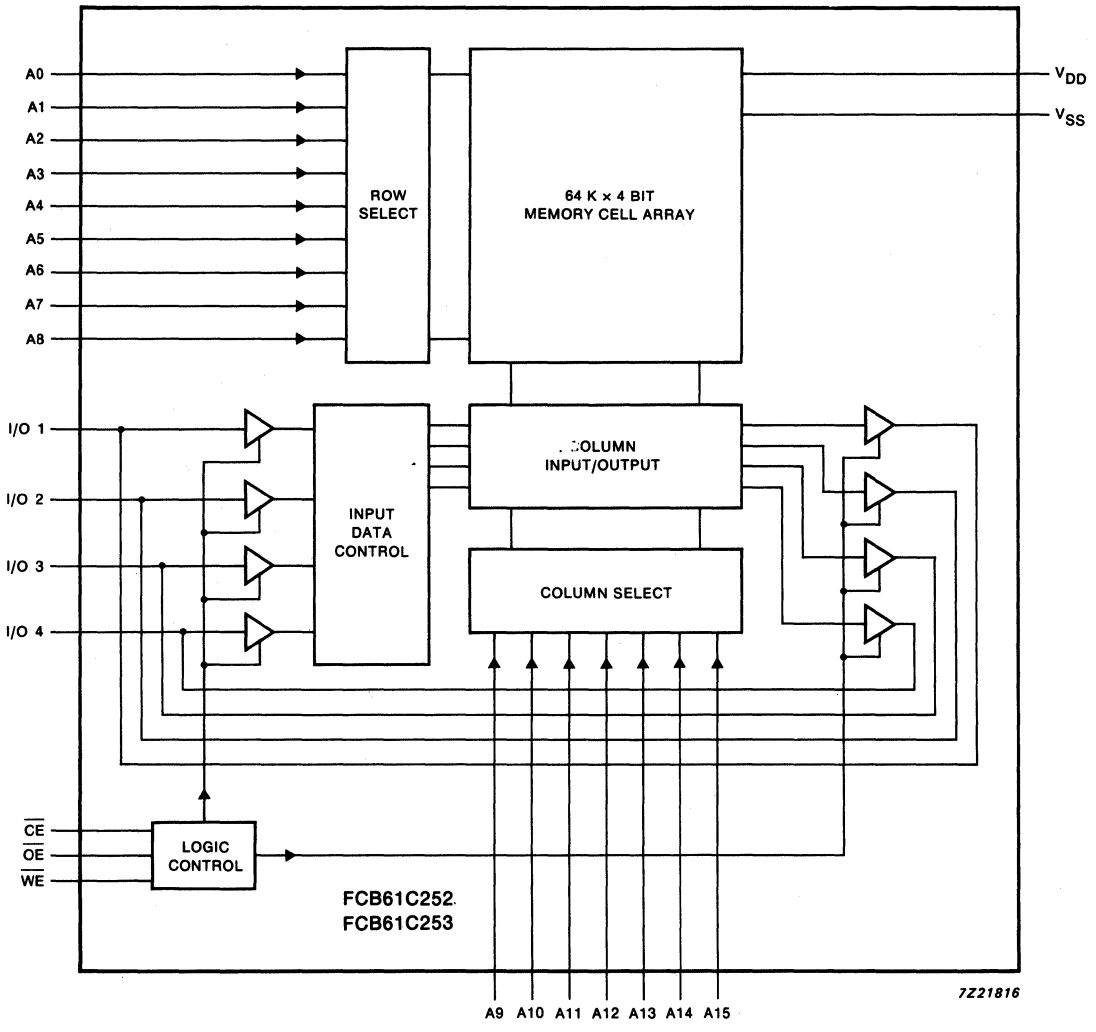
The inputs and outputs are TTL-level compatible; with a small DC load the outputs will generate CMOS compatible levels.

The FCB61C252/253 are suitable for use in very large and very fast computer memories. The FCB61C252/253 have some unique built-in test features. These features enable the user to check if the redundancy circuits on the chip have been used; or to electrically check the vendor ID code. It is also possible to bypass the peripheral circuits on the chip to directly stress the memory matrix, for, for example, reliability testing.

The FCB61C253 has an additional output enable pin to provide extra control for the output buffers and is available in the standard 28-pin 300 mil DIP and SOJ packages. The FCB61C252 is available in the standard 24-pin 300 mil DIP and SOJ packages.

Features

- Operating supply voltage: 5 V
- Access times: 20, 25, 35 and 45 ns
- Active power dissipation: 120 mA (maximum)
- Standby power: 10 mA (maximum)
- Four built-in test modes



$\overline{OE}$ input for FCB61C253 only.

Fig.1 Block diagram.

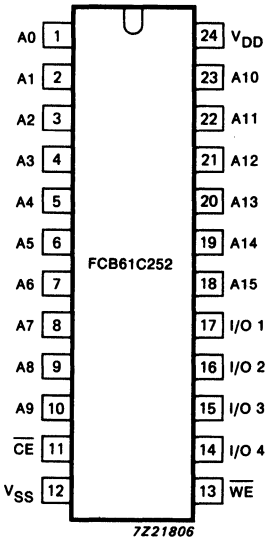


Fig.2(a) Pinning diagram (FCB61C252).

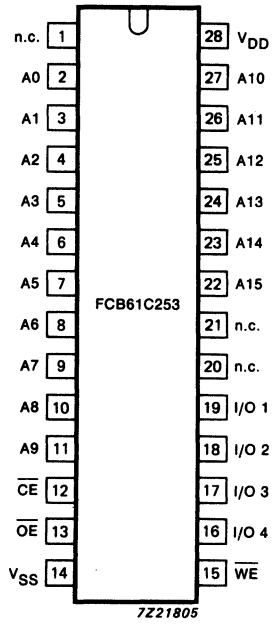


Fig.2(b) Pinning diagram (FCB61C253).

DEVELOPMENT DATA

TRUTH TABLE

$\overline{CE}$	$\overline{WE}$	mode	V_{DD} current	output	ref. cycle
H	X	not selected	I_{SB}	HIGH Z	
L	H	read	I_{DD}	D OUT	read cycle
L	L	write	I_{DD}	HIGH Z	write cycle

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF state

CAPACITANCE

f = 1 MHz; V_{DD} = 5 V; T_{amb} = 25 °C (parameters in this table are sampled not 100% tested)

parameter	conditions	symbol	typ.	max.	unit
Input capacitance	V_I = 0 V	C_I	4	6	pF
Input/output capacitance	$V_{I/O}$ = 0 V	$C_{I/O}$	5	8	pF

DC CHARACTERISTICS

V_{DD} = 5 V ± 10%; V_{SS} = 0 V; T_{amb} = 0 to 70 °C

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_{DD}	4.5	5.0	5.5	V
Input voltage HIGH		V_{IH}	2.2	3.5	V_{DD} + 0.5	V
Input voltage LOW*		V_{IL}	−0.3	–	0.8	V
Average operating current	min. cycle, $I_{I/O}$ = 0 mA	I_{DD}	–	50	120	mA
Standby current	$\overline{CE} = V_{IH}$	I_{SB}	–	5	10	mA
Output voltage LOW	I_{OL} = 8 mA	V_{OL}	–	–	0.4	V
Output voltage LOW	I_{OL} = 20 μA	V_{OL}	–	–	0.2	V
Output voltage HIGH	I_{OH} = −4 mA	V_{OH}	2.4	–	–	V
Output voltage HIGH	I_{OH} = −20 μA	V_{OH}	V_{DD}−0.2	–	–	V

* V_{IL} = −3.5 V for maximum pulse width of 20 ns.

DEVELOPMENT DATA

TIMING CHARACTERISTICS

V_{DD} = 5 V ± 10%; T_{amb} = 0 to 70 °C; input pulse levels = 0 to 3 V; input rise and fall times = 5 ns; input and output timing reference levels = 1.5 V; C_L = 30 pF; unless otherwise specified.

parameter	symbol	–20 –		–25		–35		–45		unit
		min.	max.	min.	max.	min.	max.	min.	max.	
Read cycle										
Read cycle time	t_{RC}	20	–	25	–	35	–	45	–	ns
Address access time	t_{AA}	–	20	–	25	–	35	–	45	ns
Chip enable access time	t_{ACE}	–	20	–	25	–	35	–	45	ns
Chip enable to output LOW Z*	t_{CLZ}	5	–	5	–	5	–	5	–	ns
Chip enable to output HIGH Z*	t_{CHZ}	–	10	–	15	–	15	–	15	ns
Output hold time*	t_{OH}	5	–	5	–	5	–	5	–	ns
Output enable access time**	t_{OE}	–	10	–	15	–	20	–	30	ns
Output enable to output LOW Z**	t_{OLZ}	0	–	0	–	0	–	0	–	ns
Write cycle										
Write cycle time	t_{WC}	20	–	25	–	35	–	45	–	ns
Chip enable to end of write	t_{CW}	17	–	20	–	30	–	40	–	ns
Address valid to end of write	t_{AW}	17	–	20	–	30	–	40	–	ns
Address set-up time	t_{AS}	0	–	0	–	0	–	0	–	ns
Write pulse width	t_{WP}	15	–	15	–	25	–	35	–	ns
Write recovery time	t_{WR}	0	–	0	–	0	–	0	–	ns
Write enable to output HIGH Z*	t_{WHZ}	–	10	–	15	–	15	–	15	ns
Data to write time overlap	t_{DW}	10	–	15	–	20	–	25	–	ns
Data hold from write time	t_{DH}	0	–	0	–	0	–	0	–	ns
End of write to output LOW Z*	t_{OW}	5	–	5	–	5	–	5	–	ns

* C_L = 5 pF for t_{CLZ}, T_{CHZ}, t_{OH}, t_{WHZ} and t_{OW}. Measured at 200 mV from a steady state.
** Only applicable for FCB61C253.

32 768 X 8-BIT STATIC RAM

GENERAL DESCRIPTION

The FCB61C257(L/LL) is a 256 K-bit static random access memory organized as 32 768 of 8 bits each.

The FCB61C257(L/LL) operates from a power supply of 5 V and is available with access times of 55, 70 and 100 ns. The inputs and outputs are TTL-level compatible; without a DC load, the outputs will generate CMOS compatible levels.

The device has low active and very low standby power and is suitable for use in battery back-up applications.

The FCB61C257(L/LL) is available in the standard 28-pin mil DIL and SOG packages.

Features

- Operating supply voltage: 5 V
- Access times: 55, 70 and 100 ns maximum
- Active power dissipation: 80 mA maximum
- Standby power: 5 μA maximum

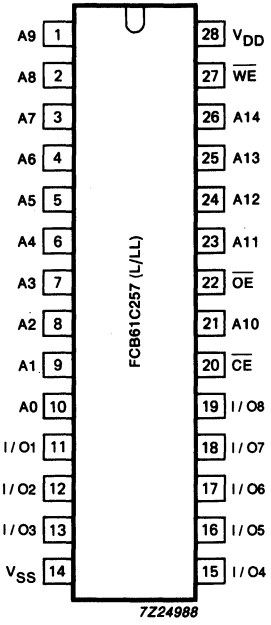


Fig.1 Pinning diagram.

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	mode	V_{DD} current	I/O pin	ref. cycle
H	X	X	not selected	I_{SB}	HIGH Z	
L	L	H	read	I_{DD}	D OUT	read (1) - (2)
L	H	L	write	I_{DD}	D IN	write (1)
L	L	L	write	I_{DD}	D IN	write (2)
L	H	H	ready-read	I_{DD}	HIGH Z	

DATA RETENTION CHARACTERISTICS FOR LOW POWER/STANDBY MODE

T_{amb} = 0 to 70 °C

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage for data retention	$\overline{CE}$ = CMOSL, other V_I = CMOS	V_{DR}	2.0	–	5.5	V
Supply current during data retention	V_{DR} = 3 V; $\overline{CE}$ = CMOSL other V_I = CMOS					
FCB61C257L only		I_{DRL}	–	–	50	μA
FCB61C257LL only		I_{DRLL}	–	–	5	μA
Timing						
Chip select to data retention time		t_{CDR}	0	–	–	ns
Recovery time to fully active		t_R	t_{RC}*	–	–	ns

* t_{RC} = read cycle time.

RECOMMENDED DC OPERATING CONDITIONS

T_{amb} = 0 to 70 °C

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{DD}	4.5	5.0	5.5	V
Input voltage HIGH	V_{IH}	2.2	3.5	V_{DD} +0.5	V
Input voltage LOW	V_{IL}	−0.5*	–	0.8	V

DC CHARACTERISTICS

V_{DD} = 5 V ± 10%; T_{amb} = 0 to 70 °C. (Typical readings taken at V_{DD} = 5 V; T_{amb} = 25 °C). All voltages are with reference to V_{SS} (0 V) unless otherwise specified; L/LL current measurements are valid after thermal equilibrium has been established.

parameter	conditions	symbol	min.	typ.	max.	unit
Input leakage current	$V_I = V_{SS}$ to V_{DD}	I_{LI}	−1.0	–	1.0	μA
Output leakage current	$\overline{CE}$ or $\overline{OE}$ = V_{IH}; $V_{I/O} = V_{SS}$ to V_{DD}	I_{LO}	−1.0	–	1.0	μA
Standby current	$\overline{CE} \geqslant V_{IH}$	I_{SB}	–	1.5	3.0	mA
FCB61C257L only	all V_I = CMOS**	I_{SBL}	–	10	100	μA
FCB61C257LL only	all V_I = CMOS**	I_{SBLL}	–	0.1	5	μA
DC read current	$\overline{WE}$ = V_{IH}; I/O = 0 mA	I_{DD1}	–	3	10	mA
FCB61C257L only	all V_I = CMOS*	I_{DDL}	–	10	100	μA
FCB61C257LL only	all V_I = CMOS*	I_{DDLL}	–	0.1	5	μA
Average operating current	minimum cycle time; $I_{I/O}$ = 0 mA	I_{DD}	–	50	80	mA
Output voltage LOW	I_{OL} = 4 mA	V_{OL}	–	–	0.4	V
Output voltage LOW	I_{OL} = 20 μA	V_{OL}	–	–	0.2	V
Output voltage HIGH	I_{OH} = −2 mA	V_{OH}	2.4	–	–	V
Output voltage HIGH	I_{OH} = −20 μA	V_{OH}	V_{DD}−0.2	–	–	V

DEVELOPMENT DATA

* V_{IL} = −1.5 V for a maximum pulse width of 50 ns.

** CMOS = CMOSH: V_{DD} −0.2 ⩽ level ⩽ V_{DD} +0.2 or CMOSL: −0.2 ⩽ level ⩽ 0.2 V.

TIMING CHARACTERISTICS

V_{DD} = 5 V ± 10%; T_{amb} = 0 to 70 °C; input levels = 0 to 3 V; input rise and fall times = 5 ns; input and output timing reference levels = 1.5 V; C_L = 30 pF; unless otherwise specified.

parameter	symbol	−55		−70		−100		unit
		min.	max.	min.	max.	min.	max.	
Read cycle								
Read cycle time	t_{RC}	55	–	70	–	100	–	ns
Address access time	t_{AA}	–	55	–	70	–	100	ns
Chip enable access time	t_{ACE}	–	55	–	70	–	100	ns
Output enable access time	t_{OE}	–	30	–	35	–	50	ns
Chip enable to output LOW Z	t_{CLZ}	5	–	5	–	5	–	ns
Output enable to output LOW Z	t_{OLZ}	5	–	5	–	5	–	ns
Chip disable to output HIGH Z	t_{CHZ}	–	20	–	30	–	35	ns
Output disable to output HIGH Z	t_{OHZ}	–	30	–	30	–	35	ns
Output hold time	t_{OH}	10	–	10	–	10	–	ns
Write cycle								
Write cycle time	t_{WC}	55	–	70	–	100	–	ns
Chip enable to end of write	t_{CW}	50	–	65	–	80	–	ns
Address valid to end of write	t_{AW}	50	–	65	–	80	–	ns
Address set-up time	t_{AS}	0	–	0	–	0	–	ns
Write pulse width	t_{WF}	45	–	55	–	70	–	ns
Write recovery time	t_{WR}	0	–	0	–	0	–	ns
Write enable to output HIGH Z	t_{WHZ}	–	20	–	25	–	30	ns
Data to write time overlap	t_{DW}	25	–	30	–	40	–	ns
Data hold from write time	t_{DH}	5	–	5	–	5	–	ns
End of write to output LOW Z	t_{OW}	5	–	5	–	5	–	ns

131 072 X 8-BIT STATIC RAM

GENERAL DESCRIPTION

The FCB61C1025(L/LL) is a 1 M-bit static RAM memory organized as 131 072 words of 8 bits each.

The FCB61C1025(L/LL) operates from a power supply of 5 V and is available with access times of 35, 45, and 55 ns. The inputs and outputs are TTL-level compatible; without a DC load, the outputs will generate CMOS compatible levels.

The device has low active and very low standby power and is suitable for use in battery back-up applications.

The FCB61C1025(L/LL) is available in the standard 32-pin mil DIL and SOG packages.

Features

- Operating supply voltage: 5 V
- Access times: 35, 45, and 55 ns maximum
- Active power dissipation: 60 mA maximum
- Standby power: 2 μA maximum (FCB61C1025LL only)

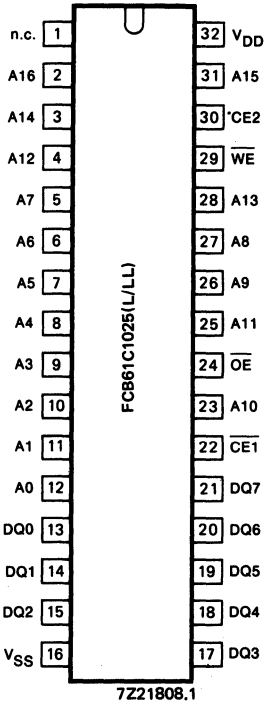


Fig.1 Pinning diagram.

TRUTH TABLE

CE2	$\overline{CE1}$	$\overline{OE}$	$\overline{WE}$	mode	V_{DD} current	I/O pin	ref. cycle
L	X	X	X	not selected	I_{SB}	Z	
X	H	X	X	not selected	I_{SB}	Z	
H	L	L	H	read	I_{DD}	D OUT	read (1) – (3)
H	L	H	L	write	I_{DD}	D IN	write (1)
H	L	L	L	write	I_{DD}	D IN	write (2)
H	L	H	H	ready-read	I_{DD}	Z	

DATA RETENTION CHARACTERISTICS FOR LOW POWER/STANDBY MODE

T_{amb} = 0 to 70 °C

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage for data retention	CE2 = CMOSL, other V_I = CMOS	V_{DR}	2.0	–	5.5	V
Supply current during data retention	V_{DR} = 3 V; CE2 = CMOSL other V_I = CMOS					
FCB61C1025L		I_{DRL}	–	–	50	μA
FCB61C1025LL		I_{DRLL}	–	–	2	μA
Timing						
Chip select to data retention time		t_{CDR}	0	–	–	ns
Recovery time to fully active		t_R	t_{RC}*	–	–	ns

* t_{RC} = read cycle time.

RECOMMENDED DC OPERATING CONDITIONS

T_{amb} = 0 to 70 °C

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{DD}	4.5	5.0	5.5	V
Input voltage HIGH	V_{IH}	2.2	3.5	V_{DD}+0.5	V
Input voltage LOW	V_{IL}	−0.3*	–	0.8	V

DC CHARACTERISTICS

V_{DD} = 5 V ± 10%; T_{amb} = 0 to 70 °C. (Typical readings taken at V_{DD} = 5 V; T_{amb} = 25 °C). All voltages are with reference to V_{SS} (0 V) unless otherwise specified; L/LL current measurements are valid after thermal equilibrium has been established.

parameter	conditions	symbol	min.	typ.	max.	unit
Input leakage current	$V_I = V_{SS}$ to V_{DD}	I_{LI}	−1.0	–	1.0	μA
Output leakage current	$\overline{CE1}$ or $\overline{OE}$ = V_{IH} or CE2 = V_{IL}; $V_{I/O} = V_{SS}$ to V_{DD}	I_{LO}	−1.0	–	1.0	μA
Standby current	CE2 ⩽ V_{IL} or $\overline{CE1}$ ⩾ V_{IH}	I_{SB}	–	1.5	3.0	mA
FCB61C1025L only	all V_I = CMOS*	I_{SBL}	–	10	100	μA
FCB61C1025LL only	all V_I = CMOS*	I_{SBLL}	–	0.1	2.0	μA
DC read current	$\overline{WE}$ = V_{IH}; I/O = 0 mA	I_{DD1}	–	4	10	mA
FCB61C1025L only	all V_I = CMOS*	I_{DDL}	–	10	100	μA
FCB61C1025LL only	all V_I = CMOS*	I_{DDLL}	–	0.1	2.0	μA
Average operating current	minimum cycle time; $I_{I/O}$ = 0 mA	I_{DD}	–	55	80	mA
Output voltage LOW	I_{OL} = 4 mA	V_{OL}	–	–	0.4	V
Output voltage LOW	I_{OL} = 20 μA	V_{OL}	–	–	0.2	V
Output voltage HIGH	I_{OH} = −2 mA	V_{OH}	2.4	–	–	V
Output voltage HIGH	I_{OH} = −20 μA	V_{OH}	V_{DD}−0.2	–	–	V

* CMOS = CMOSH: V_{DD} −0.2 ⩽ level ⩽ V_{DD} + 0.2 or CMOSL: −0.2 ⩽ level ⩽ 0.2 V.

DEVELOPMENT DATA

* V_{IL} = −1.5 V with a maximum pulse width duration of 50 ns.

TIMING CHARACTERISTICS

V_{DD} = 5 V ± 10%; T_{amb} = 0 to 70 °C; input pulse levels = 0 to 3 V; input rise and fall times = 5 ns; input and output timing reference levels = 1.5 V; C_L = 30 pF; unless otherwise specified.

parameter	symbol	–35		–45		–55		unit
		min.	max.	min.	max.	min.	max.	
Read cycle								
Read cycle time	t_{RC}	35	–	45	–	55	–	ns
Address access time	t_{AA}	–	35	–	45	–	55	ns
Chip enable access time	t_{ACE}	–	35	–	45	–	55	ns
Output enable access time	t_{OE}	–	20	–	25	–	30	ns
Chip enable to output LOW Z	t_{CLZ}	10	–	10	–	10	–	ns
Output enable to output LOW Z	t_{OLZ}	5	–	5	–	5	–	ns
Chip disable to output HIGH Z	t_{CHZ}	–	15	–	20	–	25	ns
Output disable to output HIGH Z	t_{OHZ}	–	15	–	20	–	25	ns
Output hold time	t_{OH}	5	–	5	–	5	–	ns
Write cycle								
Write cycle time	t_{WC}	35	–	45	–	55	–	ns
Chip enable to end of write	t_{CW}	30	–	40	–	50	–	ns
Address valid to end of write	t_{AW}	30	–	40	–	50	–	ns
Address set-up time	t_{AS}	0	–	0	–	0	–	ns
Write pulse width	t_{WP}	25	–	35	–	45	–	ns
Write recovery time	t_{WR}	0	–	0	–	0	–	ns
Write enable to output HIGH Z	t_{WHZ}	–	15	–	20	–	25	ns
Data to write time overlap	t_{DW}	20	–	25	–	25	–	ns
Data hold from write time	t_{DH}	0	–	0	–	0	–	ns
End of write to output LOW Z	t_{OW}	5	–	5	–	5	–	ns

256 × 4-BIT STATIC RAM

GENERAL DESCRIPTION

The PCD5101 is a very low-power 1024-bit static CMOS random access memory, organized as 256 words by 4 bits. It is suitable for low power and high speed applications where battery standby power is required to ensure non-volatility of data. All inputs and outputs are fully TTL compatible and pinning is compatible with 2101-type NMOS static RAMs and 5101-type CMOS static RAMs.

There are two chip enable inputs, $\overline{CE1}$ and CE2, selection being made when $\overline{CE1}$ is LOW and CE2 is HIGH. The memory has an output disable function, OD, which allows the inputs/outputs to be used separately, or to be tied together for use in common data I/O systems.

Features

- Operating supply voltage range 2,5 to 5,5 V
- Low data retention voltage min. 1 V
- Low power consumption in both operating and standby modes
- Access time 150 ns at V_{DD} = 5 V; 400 ns at V_{DD} = 3 V
- Three-state outputs
- All inputs and outputs directly TTL compatible
- Choice of two package types

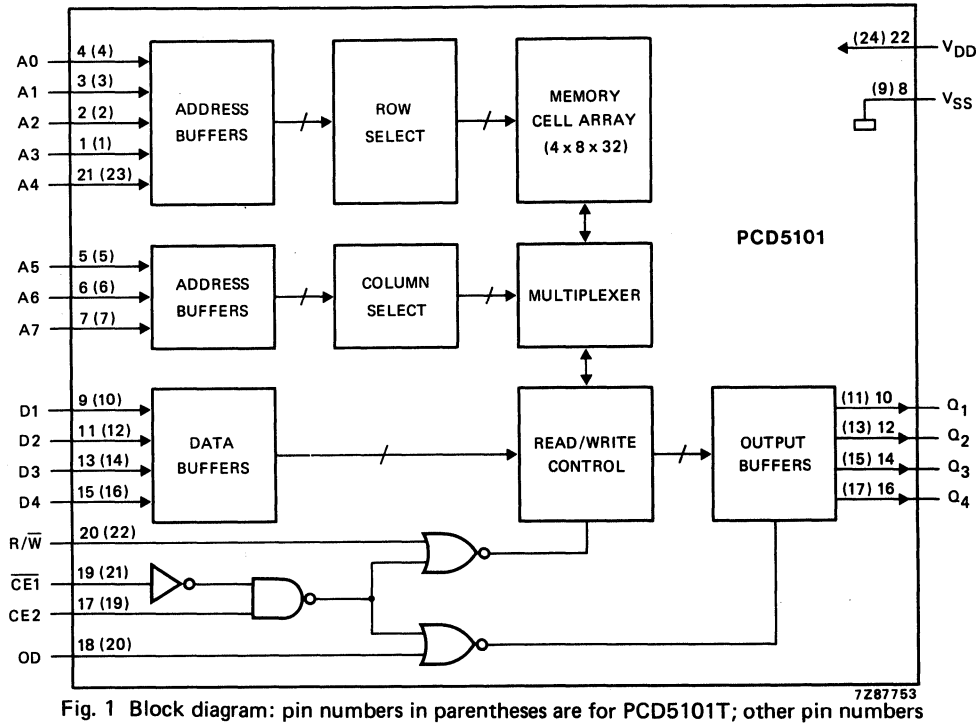


Fig. 1 Block diagram: pin numbers in parentheses are for PCD5101T; other pin numbers are applicable to PCD5101P.

PACKAGE OUTLINES

PCD5101P: 22-lead DIL; plastic (SOT116).
PCD5101T: 24-lead mini-pack; plastic (SO24; SOT137A).

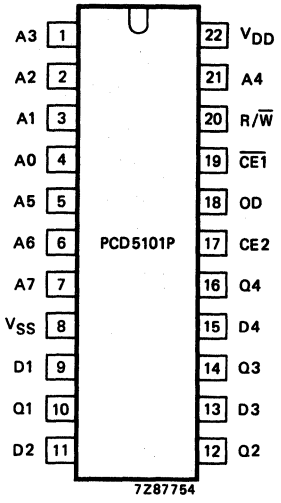


Fig. 2 Pinning diagram for PCD5101P.

PINNING

D1, D2, D3, D4	data inputs
A0, A1, A2, A3, A4, A5, A6, A7	address inputs
R/$\overline{W}$	read/write input
$\overline{CE1}$, CE2	chip enable inputs
OD	output disable
Q1, Q2, Q3, Q4	data outputs
V_{DD}	positive supply
V_{SS}	negative supply
n.c.	not connected

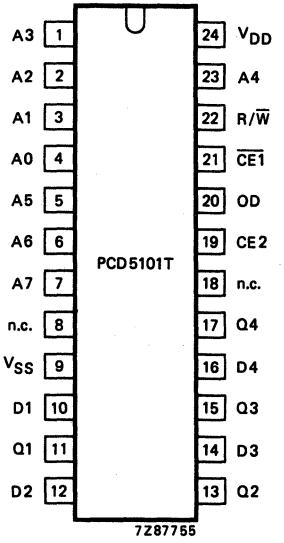


Fig. 3 Pinning diagram for PCD5101T.

OPERATING MODES

Table 1 Mode selection

$\overline{CE1}$	CE2	R/$\overline{W}$	OD	mode of operation	output state
H	X	X	X	standby	high impedance
X	L	X	X	standby	high impedance
L	H	L	H	write	high impedance
L	H	L	L	write	equal to input data
L	H	H	L	read	data valid
L	H	H	H	read	high impedance

Separate input/output: write cycle OD = X; read cycle OD = L.

Common input/output: write cycle OD = H; read cycle OD = L.

H = HIGH voltage level
L = LOW voltage level
X = don't care

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}	−0,3 to 8,0 V
Input voltage range (any pin)	V_I	V_{SS} − 0,3 to V_{DD} +0,3 V
Operating temperature range	T_{amb}	−25 to +70 °C
Storage temperature range	T_{stg}	−55 to +125 °C

D.C. CHARACTERISTICS (V_{DD} = 5 V)

V_{DD} = 5 ± 0,5 V; V_{SS} = 0 V; T_{amb} = −25 to +70 °C

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	4,5	5,0	5,5	V
Operating supply current at V_I = V_{DD} or V_{SS}; f = 1 MHz; outputs open	I_{DD}	–	10	17	mA
at V_I = 0,8 or 2,0 V; f = 1 MHz; outputs open	I_{DD}	–	10	17	mA
at V_I = 0,8 or 2,0 V; f = 5 MHz; outputs open	I_{DD}	–	12	20	mA
Standby supply current at CE2 = V_{SS}	I_{SB}	–	0,02	5,0	μA
Input leakage current at V_I = V_{SS} to V_{DD}	$\|I_{IL}\|$	–	–	0,1	μA
Input voltage LOW	V_{IL}	−0,3	–	+0,8	V
Input voltage HIGH	V_{IH}	2,0	–	V_{DD}+0,3	V
Output leakage current at V_O = V_{SS} to V_{DD}; OD = HIGH or chip disabled	$\|I_{OL}\|$	–	–	0,2	μA
Output voltage LOW at I_{OL} = 4,0 mA	V_{OL}	–	–	0,4	V
Output voltage HIGH at $-I_{OH}$ = 2,0 mA	V_{OH}	2,4	–	–	V

D.C. CHARACTERISTICS (V_{DD} = 3 V)

V_{DD} = 3 ± 0,5 V; V_{SS} = 0 V; T_{amb} = −25 to +70 °C

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	2,5	3,0	3,5	V
Operating supply current at V_I = V_{DD} or V_{SS}; f = 1 MHz; outputs open	I_{DD}	–	5	8	mA
at V_I = 0,4 or 1,6 V; f = 1 MHz; outputs open	I_{DD}	–	5	8	mA
Standby supply current at CE2 = V_{SS}	I_{SB}	–	0,02	5,0	μA
Input leakage current at V_I = V_{SS} to V_{DD}	$\|I_{IL}\|$	–	–	0,1	μA
Input voltage LOW	V_{IL}	−0,3	–	+0,4	V
Input voltage HIGH	V_{IH}	1,6	–	V_{DD}+0,3	V
Output leakage current at V_O = V_{SS} to V_{DD}; OD = HIGH or chip disabled	$\|I_{OL}\|$	–	–	0,2	μA
Output voltage LOW at I_{OL} = 1,0 mA	V_{OL}	–	–	0,3	V
Output voltage HIGH at $-I_{OH}$ = 1,0 mA	V_{OH}	1,7	–	–	V

A.C. TEST CONDITIONS (V_{DD} = 5 V)

Input pulse levels	0,8 V to 2,0 V
Input rise and fall times	5 ns
Input timing reference levels	1,5 V
Output timing levels	1,5 V
Output timing levels for high/low impedance	1,2 V and 2,8 V
Output load (2 TTL inputs and load capacitance C_L)	Fig. 4

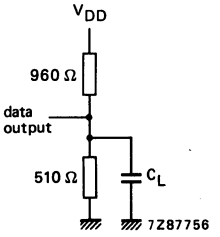


Fig. 4 Test load.

A.C. CHARACTERISTICS (V_{DD} = 5 V)

V_{DD} = 5 ± 0,5 V; V_{SS} = 0 V; T_{amb} = −25 to + 70 °C; loads as per Fig. 4 with C_L = 100 pF unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Read cycle					
Read cycle time	t_{RC}	150	–	–	ns
Address access time	t_{AA}	–	–	150	ns
Chip enable $\overline{CE1}$ to output	t_{CO1}	–	–	150	ns
Chip enable CE2 to output	t_{CO2}	–	–	150	ns
Output disable OD to output	t_{OD}	–	–	70	ns
Data output to high impedance state at C_L = 5 pF	t_{DF}	10	–	70	ns
Previously read data valid with respect to address change	t_{OH1}	10	–	–	ns
Previously read data valid with respect to chip enable	t_{OH2}	10	–	–	ns
Write cycle					
Write cycle time	t_{WC}	150	–	–	ns
Write delay time	t_{AW}	0	–	–	ns
Chip enable $\overline{CE1}$ to write	t_{CW1}	120	–	–	ns
Chip enable CE2 to write	t_{CW2}	120	–	–	ns
Data set-up time	t_{DW}	70	–	–	ns
Data hold time	t_{DH}	0	–	–	ns
Write pulse duration	t_{WP}	70	–	–	ns
Write recovery time	t_{WR}	0	–	–	ns
Output disable OD set-up time	t_{DS}	70	–	–	ns

A.C. TEST CONDITIONS (V_{DD} = 3 V)

Input pulse levels	0,4 V to 1,6 V
Input rise and fall times	5 ns
Input timing reference levels	1,0 V
Output timing levels	1,0 V
Output timing levels for high/low impedance	0,7 V and 1,7 V
Output load	Fig. 5

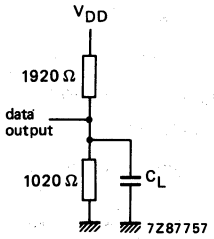


Fig. 5 Test load.

A.C. CHARACTERISTICS (V_{DD} = 3 V)

V_{DD} = 3 ± 0,5 V; V_{SS} = 0 V; T_{amb} = −25 to +70 °C; loads as per Fig. 5 with C_L = 100 pF unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Read cycle					
Read cycle time	t_{RC}	400	–	–	ns
Address access time	t_{AA}	–	–	400	ns
Chip enable $\overline{CE1}$ to output	t_{CO1}	–	–	400	ns
Chip enable CE2 to output	t_{CO2}	–	–	400	ns
Output disable OD to output	t_{OD}	–	–	200	ns
Data output to high impedance state at C_L = 5 pF	t_{DF}	10	–	200	ns
Previously read data valid with respect to address change	t_{OH1}	10	–	–	ns
Previously read data valid with respect to chip enable	t_{OH2}	10	–	–	ns
Write cycle					
Write cycle time	t_{WC}	400	–	–	ns
Write delay time	t_{AW}	0	–	–	ns
Chip enable $\overline{CE1}$ to write	t_{CW1}	300	–	–	ns
Chip enable CE2 to write	t_{CW2}	300	–	–	ns
Data set-up time	t_{DW}	200	–	–	ns
Data hold time	t_{DH}	0	–	–	ns
Write pulse duration	t_{WP}	200	–	–	ns
Write recovery time	t_{WR}	0	–	–	ns
Output disable OD set-up time	t_{DS}	200	–	–	ns

WAVEFORMS

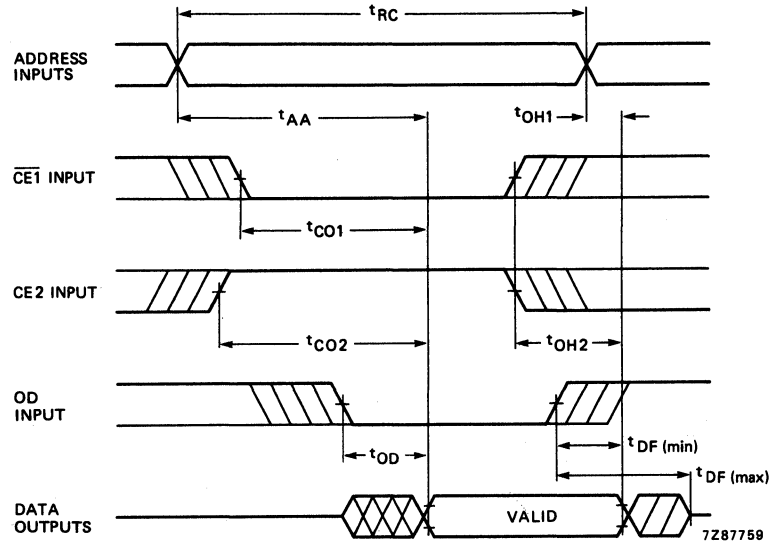


Fig. 6 Read cycle timing; R/$\overline{W}$ = HIGH.

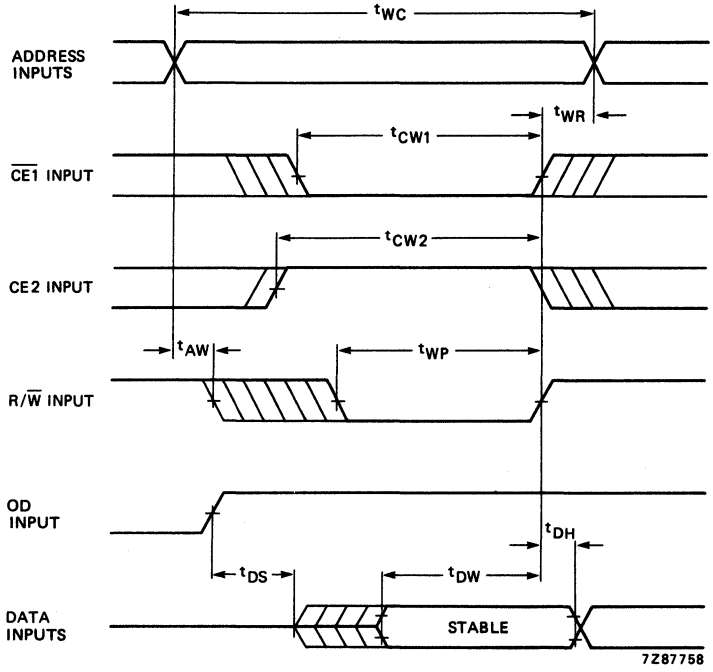


Fig. 7 Write cycle timing.

LOW SUPPLY VOLTAGE DATA RETENTION CHARACTERISTICS

$CE2 \leqslant 0{,}2$ V; $T_{amb} = -25$ to $+70$ °C.

parameter	symbol	min.	typ.	max.	unit
Supply voltage for data retention	V_{DR}	1,0	–	5,5	V
Data retention current at V_{DD} = 1,5 V	I_{DR}	–	0,02	2,0	μA
Chip deselect to data retention time	t_{CDR}	0	–	–	ns
Operation recovery time	t_R	0	–	–	ns

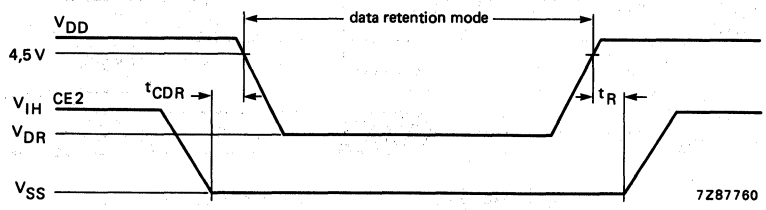


Fig. 8 Low supply voltage data retention characteristics.

1024 x 4-BIT STATIC RAM

GENERAL DESCRIPTION

The PCD5114 is a low-power, high-speed 4096-bit static CMOS RAM, organized as 1024 words of 4 bits each. The IC is suitable for low power and high speed applications, for battery operation and where battery backup is required. Inputs R/$\overline{W}$ and $\overline{CE}$ control the read/write operation and standby mode respectively. The PCD5114 is pin compatible with the SBB2114 types.

Features

- Operating supply voltage — 2,5 V to 5,5 V
- Low data retention voltage — min. 1,0 V
- Low standby current — max. 5 μA
- Cycle time = access time — max. 200 ns
- Static operation requiring no clock or timing strobe
- Low power consumption
- 3-state common data input/output interface
- All inputs and outputs directly TTL compatible
- Pin compatible with SBB2114 variants
- 18-lead DIL package
- 20-lead SO package

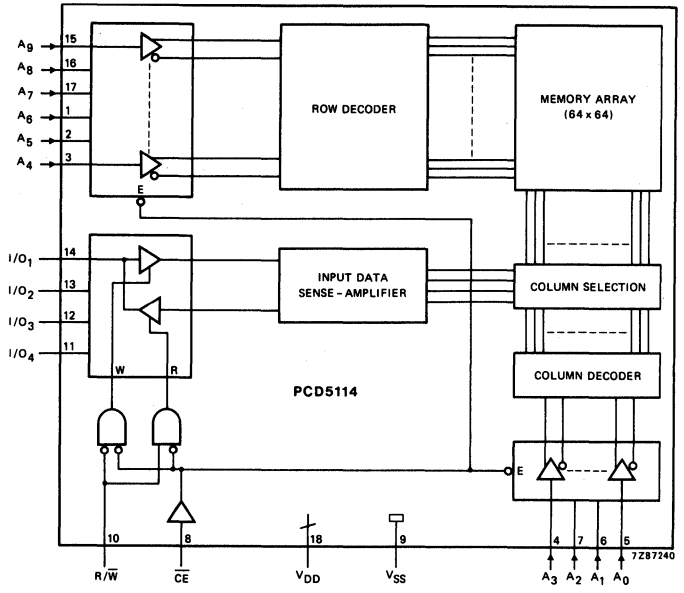


Fig. 1 Block diagram.

PACKAGE OUTLINES

PCD5114P: 18-lead DIL; plastic (SOT102G).
PCD5114T: 20-lead mini-pack; plastic (SO20; SOT163A).

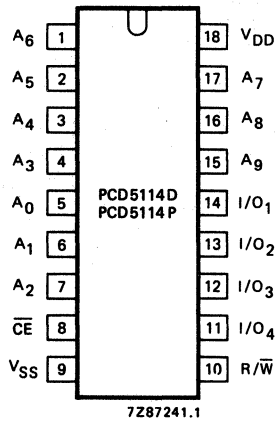


Fig. 2 Pinning diagram: PCD5114D; PCD5114P.

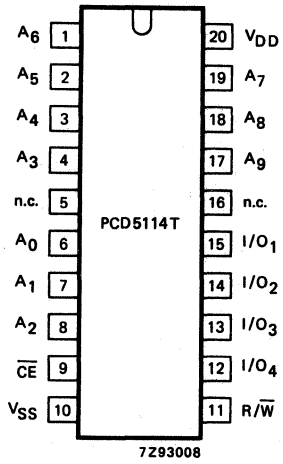


Fig. 3 Pinning diagram: PCD5114T.

A_0 to A_3	column address inputs
A_4 to A_9	row address inputs
$\overline{CE}$	chip enable input
$R/\overline{W}$	read/write input
I/O_1 to I/O_4	data input/output
V_{SS}	negative supply (ground)
V_{DD}	positive supply (+ 5 V)

Table 1 Mode selection

$\overline{CE}$	$R/\overline{W}$	mode	output	power
H	H	not selected	high impedance	standby
H	L	not selected	high impedance	standby
L	H	read	active	active
L	L	write	high impedance	active

H = HIGH logic level (the most positive voltage)
L = LOW logic level (the most negative voltage)

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}	−0,3 to + 8 V
Input voltage range (any pin)	V_I	V_{SS}−0,3 to V_{DD} + 0,3 V
Storage temperature range	T_{stg}	−55 to + 125 °C
Operating ambient temperature range	T_{amb}	−25 to + 70 °C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see "Handling MOS Devices").

DEVELOPMENT DATA

D.C. CHARACTERISTICS

V_{DD} = 5 V ± 0,5 V; V_{SS} = 0 V; T_{amb} = −25 to + 70 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Operating supply current					
at $V_I = V_{DD}/V_{SS}$; f = 1 MHz; outputs open	I_{DD}	–	10	17	mA
at V_I = 0,8 V/2,0 V; f = 1 MHz; outputs open	I_{DD}	–	10	17	mA
at V_I = 0,8 V/2,0 V; f = 5 MHz; outputs open	I_{DD}	–	12	20	mA
Standby current					
at $\overline{CE} = V_{DD}$	I_{SB}	–	0,02	5	μA
Input voltage HIGH	V_{IH}	2,0	–	V_{DD} + 0,3	V
Input voltage LOW	V_{IL}	−0,3	–	+0,8	V
Input leakage current					
at $V_I = V_{SS}$ to V_{DD}	$\pm I_{IL}$	–	–	0,1	μA
Output voltage HIGH					
at $-I_{OH}$ = 2 mA	V_{OH}	2,4	–	–	V
Output voltage LOW					
at I_{OL} = 4 mA	V_{OL}	–	–	0,4	V
Output leakage current					
at $V_O = V_{SS}$ to V_{DD}; $\overline{CE}$ = HIGH	$\pm I_{OL}$	–	–	0,5	μA

D.C. CHARACTERISTICS

V_{DD} = 3 V ± 0,5 V; V_{SS} = 0 V; T_{amb} = −25 to + 70 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Operating supply current					
at $V_I = V_{DD}/V_{SS}$; f = 1 MHz; outputs open	I_{DD}	–	5	8	mA
at V_I = 0,4 V/1,6 V; f = 1 MHz; outputs open	I_{DD}	–	5	8	mA
Standby current					
at $\overline{CE} = V_{DD}$	I_{SB}	–	0,02	5	μA
Input voltage HIGH	V_{IH}	1,6	–	V_{DD} + 0,3	V
Input voltage LOW	V_{IL}	−0,3	–	+0,4	V
Input leakage current					
at $V_I = V_{SS}$ to V_{DD}	$\pm I_{IL}$	–	–	0,1	μA
Output voltage HIGH					
at $-I_{OH}$ = 1 mA	V_{OH}	1,7	–	–	V
Output voltage LOW					
at I_{OL} = 1 mA	V_{OL}	–	–	0,3	V
Output leakage current					
at $V_O = V_{SS}$ to V_{DD}; $\overline{CE}$ = HIGH	$\pm I_{OL}$	–	–	0,5	μA

A.C. CHARACTERISTICS

V_{DD} = 5 V ±0,5 V; V_{SS} = 0 V; T_{amb} = −25 to + 70 °C; measured in Fig. 4, C_L = 100 pF; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Read cycle					
Read cycle time	t_{RC}	200	–	–	ns
Address access time	t_{AA}	–	–	200	ns
Chip select access time	t_{AC}	–	–	200	ns
Output hold from address change	t_{OHA}	20	–	–	ns
Output hold from chip select	t_{OHC}	20	–	–	ns
Output to low impedance from chip selection at C_L = 5 pF	t_{CLZ}	20	–	–	ns
Output to high impedance from chip deselection at C_L = 5 pF	t_{CHZ}	–	–	80	ns
Write cycle					
Write cycle time	t_{WC}	200	–	–	ns
Chip selection to end of write	t_{CW}	120	–	–	ns
Address set-up time	t_{AS}	0	–	–	ns
Write pulse duration	t_{WP}	140	–	–	ns
Write recovery time	t_{WR}	0	–	–	ns
Data set-up time	t_{DS}	80	–	–	ns
Data hold time	t_{DH}	0	–	–	ns
Output to high impedance from write enabled at C_L = 5 pF	t_{WZ}	–	–	60	ns
Output active from end of write at C_L = 5 pF	t_{RZ}	20	–	–	ns

A.C. TEST CONDITIONS (see Fig. 4)

Input pulse levels	0,8 V to 2,0 V
Input rise and fall times	5 ns
Input timing reference levels	1,5 V
Output timing levels	1,5 V
Output timing levels for high/low impedance	1,2 V and 2,8 V
Output load	2 TTL gates and C_L = 100 pF

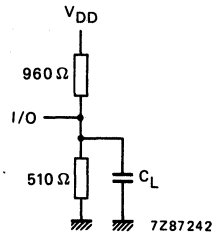


Fig. 4 Load for a.c. test conditions (V_{DD} = 5 V ± 0,5 V).

DEVELOPMENT DATA

A.C. CHARACTERISTICS

V_{DD} = 3 V ± 0,5 V; V_{SS} = 0 V; T_{amb} = −25 to + 70°C; measured in Fig. 5, C_L = 100 pF; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Read cycle					
Read cycle time	t_{RC}	500	–	–	ns
Address access time	t_{AA}	–	–	500	ns
Chip select access time	t_{AC}	–	–	500	ns
Output hold from address change	t_{OHA}	20	–	–	ns
Output hold from chip select	t_{OHC}	20	–	–	ns
Output to low impedance from chip selection at C_L = 5 pF	t_{CLZ}	20	–	–	ns
Output to high impedance from chip deselection at C_L = 5 pF	t_{CHZ}	–	–	200	ns
Write cycle					
Write cycle time	t_{WC}	500	–	–	ns
Chip selection to end of write	t_{CW}	300	–	–	ns
Adress set-up time	t_{AS}	0	–	–	ns
Write pulse duration	t_{WP}	350	–	–	ns
Write recovery time	t_{WR}	0	–	–	ns
Data set-up time	t_{DS}	200	–	–	ns
Data hold time	t_{DH}	0	–	–	ns
Output to high impedance from write enabled at C_L = 5 pF	t_{WZ}	–	–	150	ns
Output active from end of write at C_L = 5 pF	t_{RZ}	20	–	–	ns

A.C. TEST CONDITIONS (see Fig. 5)

Input pulse levels	0,4 V to 1,6 V
Input rise and fall times	5 ns
Input timing reference levels	1,0 V
Output timing levels	1,0 V
Output timing levels for high/low impedance	0,7 V and 1,7 V
Output load	2 TTL gates and C_L = 100 pF

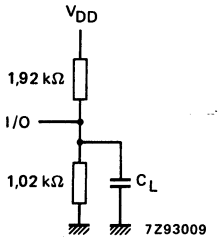


Fig. 5 Load for a.c. test conditions (V_{DD} = 3 V ± 0,5 V).

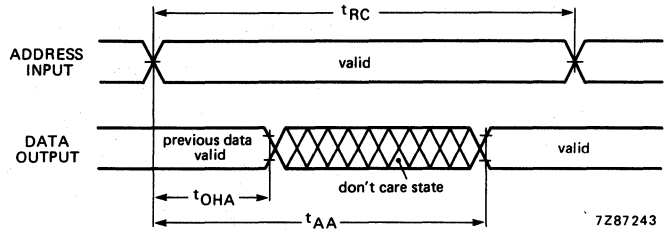


Fig. 6 Read cycle timing (1): R/$\overline{W}$ is HIGH; $\overline{CE}$ is LOW for a read cycle.

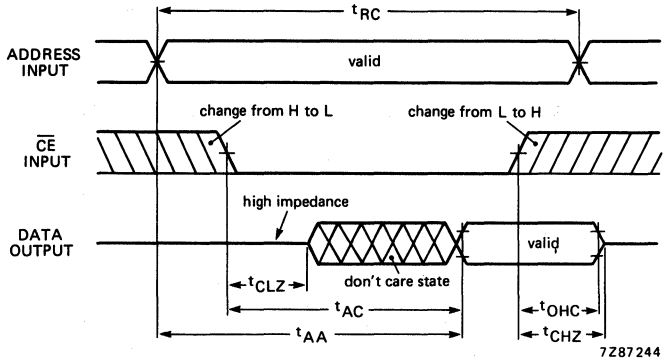


Fig. 7 Read cycle timing (2): R/$\overline{W}$ is HIGH for a read cycle.

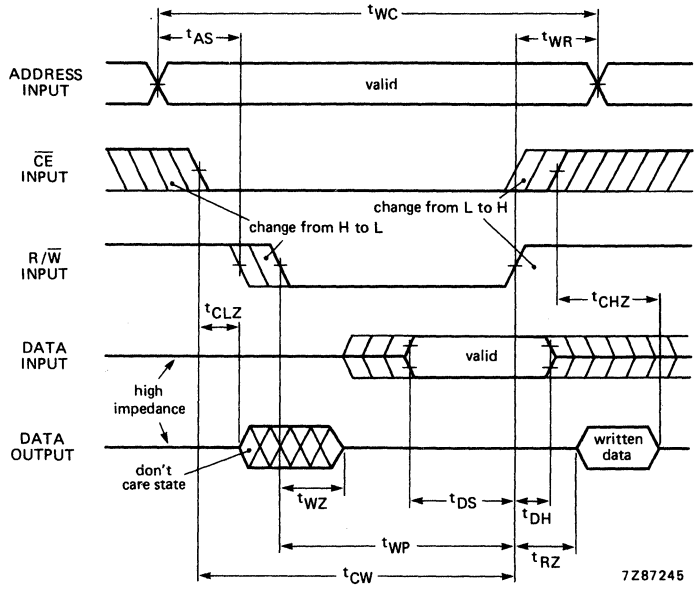


Fig. 8 Write cycle (1): R/$\overline{W}$ controlled.

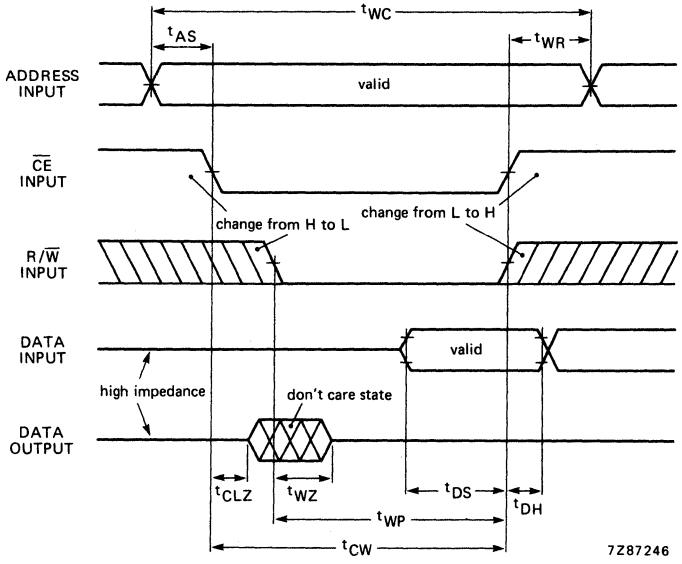


Fig. 9 Write cycle (2): $\overline{CE}$ controlled.

Note : If the $\overline{CE}$ low transition occurs after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.

DEVELOPMENT DATA

CAPACITANCE

$f = 1$ MHz; $T_{amb} = 25\ ^{o}C$

parameter	symbol	min.	typ.	max.	unit
Input capacitance at $V_I = V_{SS}$	C_I	–	–	5	pF
Output capacitance at $V_O = V_{SS}$	C_O	–	–	5	pF

LOW V_{DD} DATA RETENTION CHARACTERISTICS

$T_{amb} = -25$ to $+70\ ^{o}C$

parameter	symbol	min.	typ.	max.	unit
V_{DD} for data retention at $\overline{CE} = V_{DDR} \pm 0{,}2$ V; $V_I = V_{DDR}$ to V_{SS}	V_{DDR}	1	–	5,5	V
Data retention current at $V_{DDR} = 1{,}5$ V	I_{DDR}	–	0,02	2	μA
Chip deselect to data retention time	t_{CR}	0	–	–	ns
Operation recovery time	t_R	0	–	–	ns

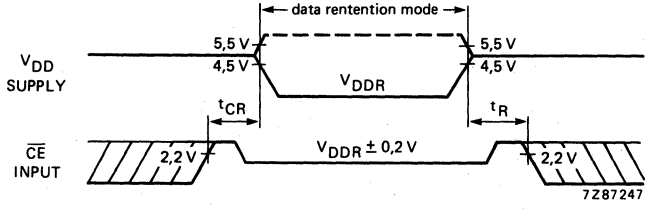


Fig. 10 LOW V_{DD} data retention.

128 X 8-BIT/256 X 8-BIT STATIC RAMS WITH I²C-BUS INTERFACE

GENERAL DESCRIPTION

The PCF8570, PCF8570C and PCF8571 are low-power static CMOS RAMs. The PCF8570 and PCF8570C are organized as 256 words by 8-bits and the PCF8571 is organized as 128 words by 8-bits. Addresses and data are transferred serially via a two-line bidirectional bus (I²C). The built-in word address register is incremented automatically after each written or read data byte. Three address pins A0, A1 and A2 are used for hardware address, allowing the use of up to eight devices connected to the bus without additional hardware. For system expansion over 8 devices the PCF8570/71 can be used in conjunction with the PCF8750C which has an alternative slave address for memory extension up to 16 devices.

Features

- Operating supply voltage 2.5 V to 6 V
- Low data retention voltage min. 1.0 V
- Low standby current max. 15 μA
- Power saving mode typ. 50 nA
- Serial input/output bus (I²C)
- Address by 3 hardware address pins
- Automatic word address incrementing
- 8-lead DIL package

Applications

- Telephony — RAM expansion for stored numbers in repertory dialling (e.g. PCD3343 applications)
- Radio and television — channel presets
- Video cassette recorder — channel presets
- General purpose — RAM expansion for the microcontroller families MAB8400, PCF84CXX and most other microcontrollers

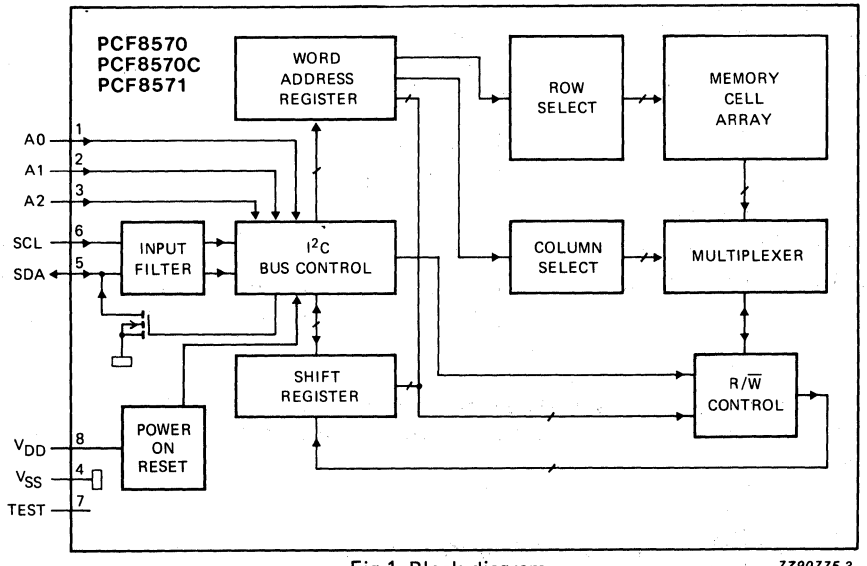


Fig.1 Block diagram.

PACKAGE OUTLINES

PCF8570/PCF8570C/PCF8571/P: 8-lead DIL; plastic (SOT97).
PCF8570/PCF8570C/PCF8571/T: 8-lead mini-pack (SO8L; SOT176C).

PINNING

1 to 3	A0 to A2	address inputs
4	V_{SS}	negative supply
5	SDA	serial data line (I²C-bus)
6	SCL	serial clock line (I²C-bus)
7	TEST	test input for test speed-up; must be connected to V_{SS} when not in use (power saving mode, see Figs 12 and 13)
8	V_{DD}	positive supply

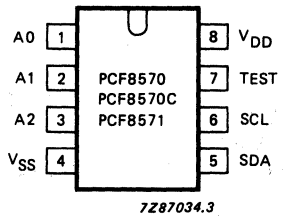


Fig.2 Pinning diagram.

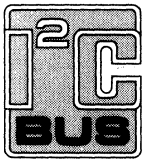
RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range	V_{DD}	−0.8	+8.0	V
Input voltage range	V_I	−0.8	V_{DD} + 0.8	V
DC input current	$\pm I_I$	−	10	mA
DC output current	$\pm I_O$	−	10	mA
V_{DD} or V_{SS} current	$\pm I_{DD}$; $\pm I_{SS}$	−	50	mA
Total power dissipation	P_{tot}	−	300	mW
Power dissipation per output	P_O	−	50	mW
Operating ambient temperature range	T_{amb}	−40	+85	°C
Storage temperature range	T_{stg}	−65	+150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is good practice to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

CHARACTERISTICS

V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage		V_{DD}	2.5	–	6.0	V
Supply current	$V_I = V_{DD}$ or V_{SS}					
operating	f_{SCL} = 100 kHz	I_{DD}	–	–	200	μA
standby	f_{SCL} = 0 Hz	I_{DDO}	–	–	15	μA
	T_{amb} = −25 to +70 °C	I_{DDO}	–	–	5	μA
Power-on reset level	note 1	V_{POR}	1.5	1.9	2.3	V
Inputs, input/output SDA						
Input voltage LOW	note 2	V_{IL}	−0.8	–	0.3 V_{DD}	V
Input voltage HIGH	note 2	V_{IH}	0.7 V_{DD}	–	V_{DD} + 0.8	V
Output current LOW	V_{OL} = 0.4 V	I_{OL}	3	–	–	mA
Leakage current	$V_I = V_{DD}$ or V_{SS}	$\|I_L\|$	–	–	1	μA
Inputs A0 to A2; TEST						
Input leakage current	$V_I = V_{DD}$ or V_{SS}	$\pm I_{LI}$	–	–	250	nA
Inputs SCL; SDA						
Input capacitance	$V_I = V_{SS}$	C_I	–	–	7	pF
LOW V_{DD} data retention						
Supply voltage for data retention		V_{DDR}	1	–	6	V
Supply current	V_{DDR} = 1 V	I_{DDR}	–	–	5	μA
Supply current	V_{DDR} = 1 V; T_{amb} = −25 to +70 °C	I_{DDR}	–	–	2	μA
Power saving mode	see Figs 12 and 13					
Supply current	TEST = V_{DD}; T_{amb} = 25 °C					
PCF8570/PCF8570C		I_{DDR}	–	50	400	nA
PCF8571		I_{DDR}	–	50	200	nA
Recovery time		t_{HD2}	–	50	–	μs

Notes to the characteristics

1. The power-on reset circuit resets the I²C-bus logic when $V_{DD} < V_{POR}$. The status of the device after a power-on reset condition can be tested by sending the slave address and testing the acknowledge bit.
2. If the input voltages are a diode voltage above or below the supply voltage V_{DD} or V_{SS} an input current will flow: this current must not exceed ± 0.5 mA.

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

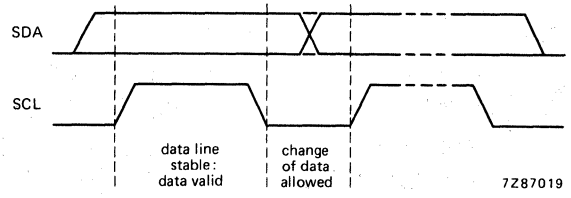


Fig.3 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

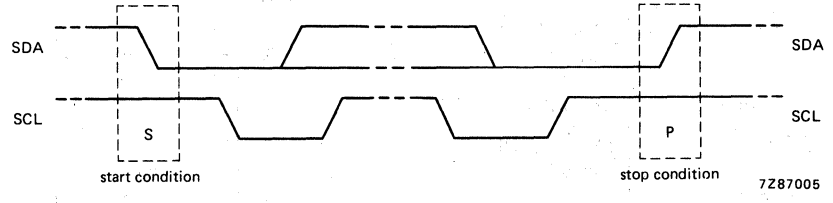


Fig.4 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

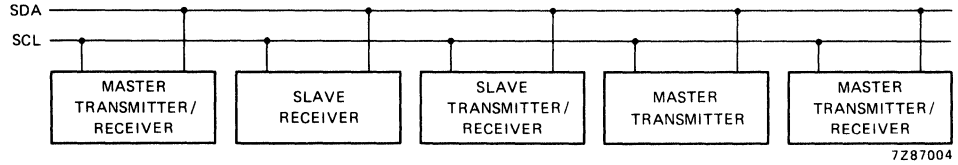


Fig.5 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

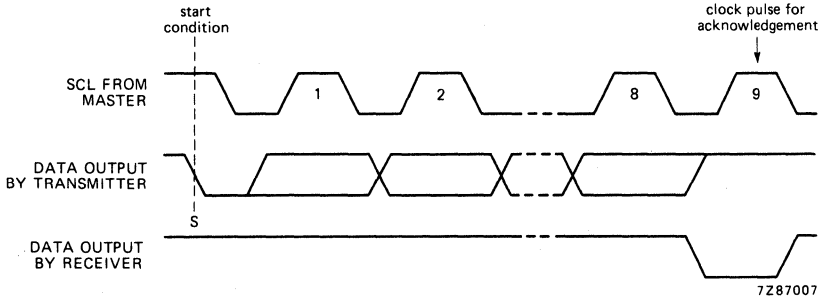


Fig.6 Acknowledgement on the I²C-bus.

Timing specifications

All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

parameter	symbol	min.	typ.	max.	unit
SCL clock frequency	f_{SCL}	–	–	100	kHz
Tolerable spike width on bus	t_{SW}	–	–	100	ns
Bus free time	t_{BUF}	4.7	–	–	μs
Start condition set-up time	$t_{SU;STA}$	4.7	–	–	μs
Start condition hold time	$t_{HD;STA}$	4.0	–	–	μs
SCL LOW time	t_{LOW}	4.7	–	–	μs
SCL HIGH time	t_{HIGH}	4.0	–	–	μs
SCL and SDA rise time	t_r	–	–	1.0	μs
SCL and SDA fall time	t_f	–	–	0.3	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Data hold time	$t_{HD;DAT}$	0	–	–	ns
SCL LOW to data out valid	$t_{VD;DAT}$	–	–	3.4	μs
Stop condition set-up time	$t_{SU;STO}$	4.0	–	–	μs

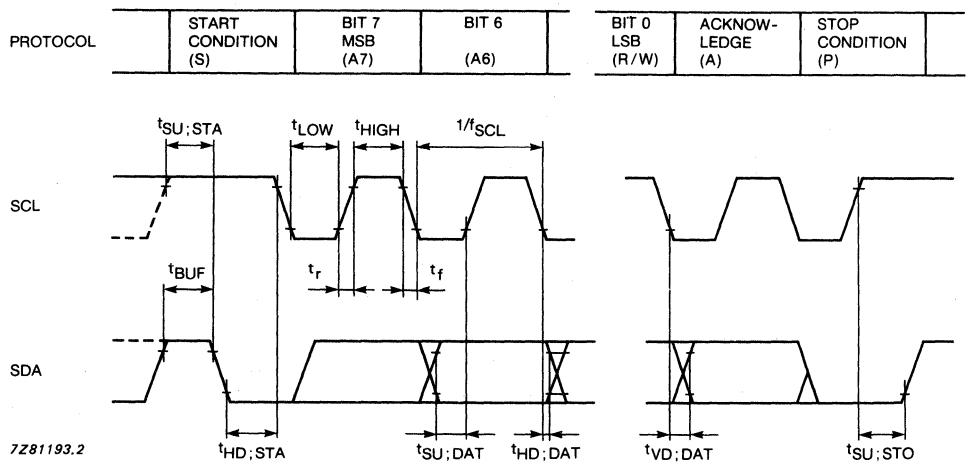


Fig.7 I²C-bus timing diagram.

Bus protocol

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure. The I²C-bus configuration for different PCF8570/PCF8570C/PCF8571 READ and WRITE cycles is shown in Fig.8.

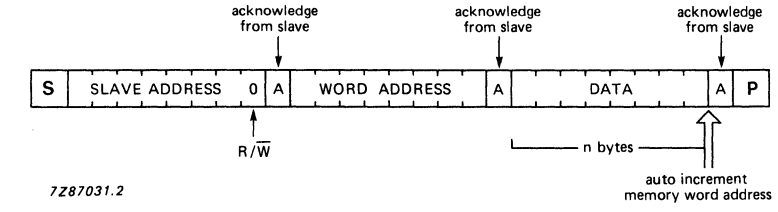


Fig.8(a) Master transmits to slave receiver (WRITE mode).

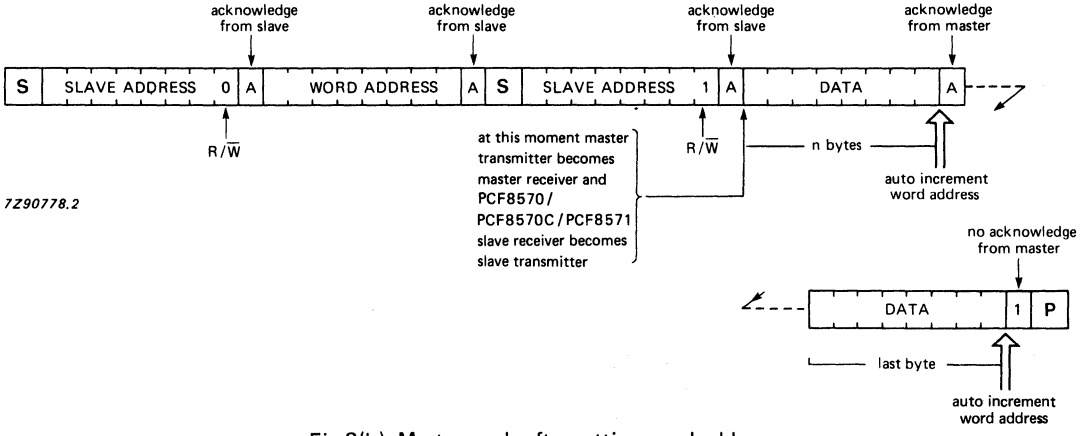


Fig.8(b) Master reads after setting word address (WRITE word address; READ data).

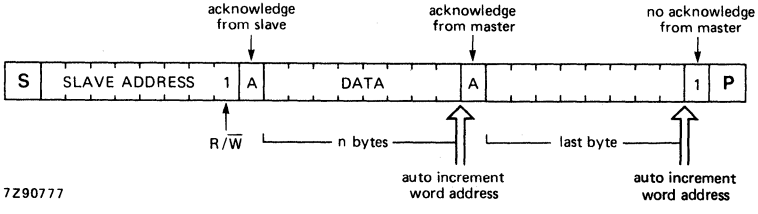


Fig.8(c) Master reads slave immediately after first byte (READ mode).

APPLICATION INFORMATION

The PCF8570/PCF8571 slave address has a fixed combination 1010 as group 1, while group 2 is fully programmable (see Fig.9). The PCF8570C has slave address 1011 as group 1, while group 2 is fully programmable (see Fig.10).

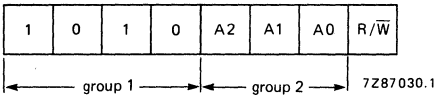


Fig.9 PCF8570 and PCF8571 address.

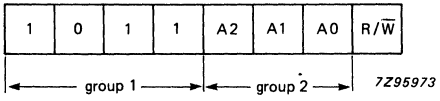
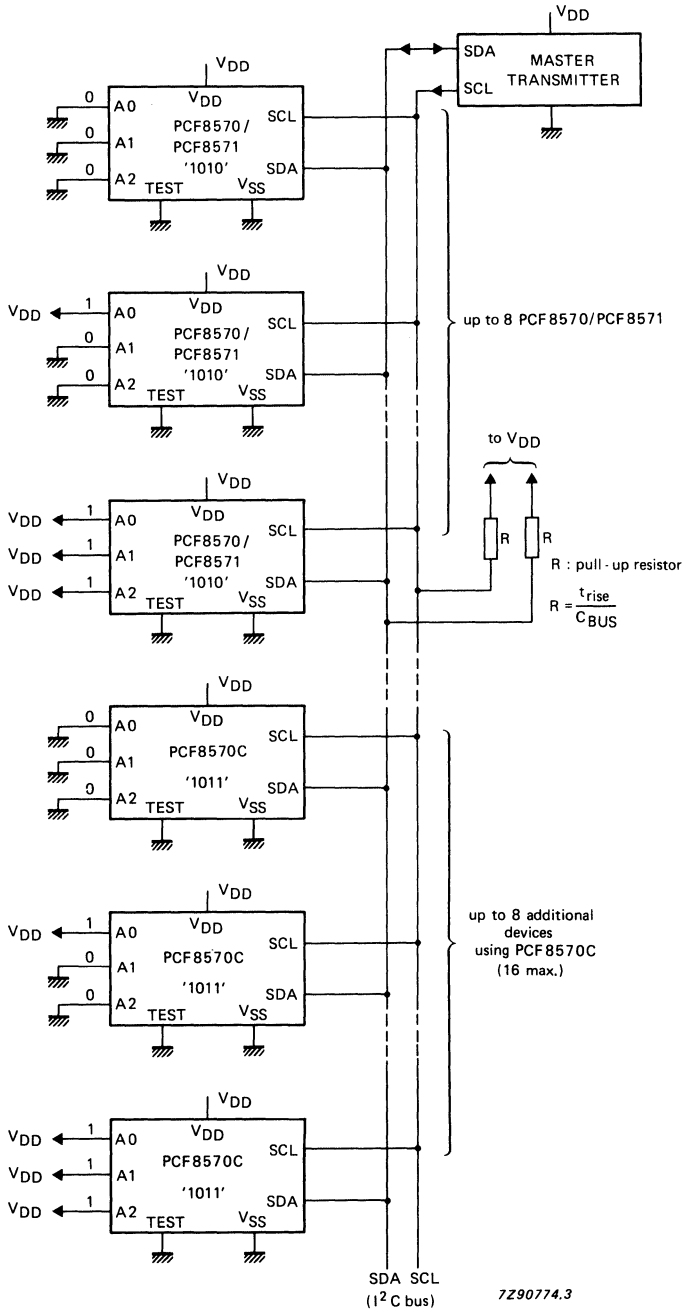


Fig.10 PCF8570C address.

Note

A0, A1, and A2 inputs must be connected to V_{DD} or V_{SS} but not left open-circuit.

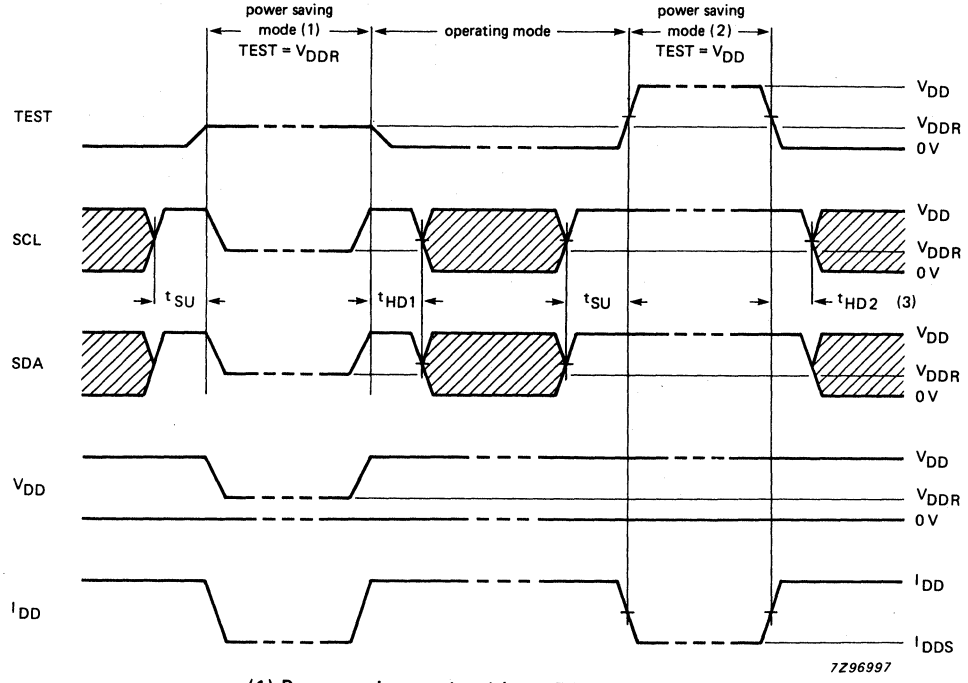


It is recommended that a 4.7 μF/10 V solid aluminium capacitor (SAL) be connected between V_{DD} and V_{SS}.

Fig.11 Application diagram.

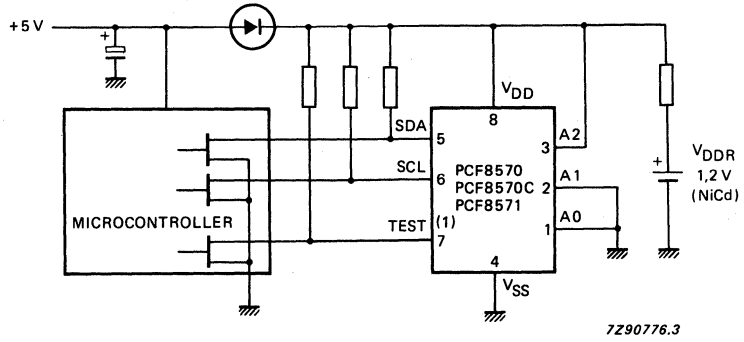
POWER SAVING MODE

With the condition **TEST** = V_{DD} or V_{DDR} the PCF8570/PCF8570C/PCF8571 goes into the power saving mode and I^2C-bus logic is reset.



(1) Power saving mode without 5 V supply voltage.
(2) Power saving mode with 5 V supply voltage.
(3) t_{SU} and $t_{HD1} \geqslant 4\ \mu s$ and $t_{HD2} \geqslant 50\ \mu s$.

Fig.12 Timing for power saving mode.



(1) In the operating mode TEST = 0; In the power saving mode TEST = V_{DDR}.

It is recommended that a 4.7 μF/10 V solid aluminium capacitor (SAL) be connected between V_{DD} and V_{SS}.

Fig.13 Application example for power saving mode.

CLOCK CALENDAR WITH 256 X 8-BIT STATIC RAM

GENERAL DESCRIPTION

The PCF8583 is a low power 2048-bit static CMOS RAM organized as 256 words by 8-bits. Addresses and data are transferred serially via a two-line bidirectional bus (I^2C). The built-in word address register is incremented automatically after each written or read data byte. One address pin A0 is used for programming the hardware address, allowing the connection of two devices to the bus without additional hardware. The built-in 32.768 kHz oscillator circuit and the first 8 bytes of the RAM are used for the clock/calendar and counter functions. The next 8 bytes may be programmed as alarm registers or used as free RAM space.

Features

- I^2C-bus interface operating supply voltage: 2.5 V to 6 V
- Clock operating supply voltage (0 to 70 °C): 1.0 V to 6 V
- Data retention voltage: 1.0 V to 6 V
- Operating current (f_{SCL} = 0 Hz): max. 50 μA
- Clock function with four year calendar
- 24 or 12 hour format
- 32.768 kHz or 50 Hz time base
- Serial input/output bus (I^2C)
- Automatic word address incrementing
- Programmable alarm, timer and interrupt function

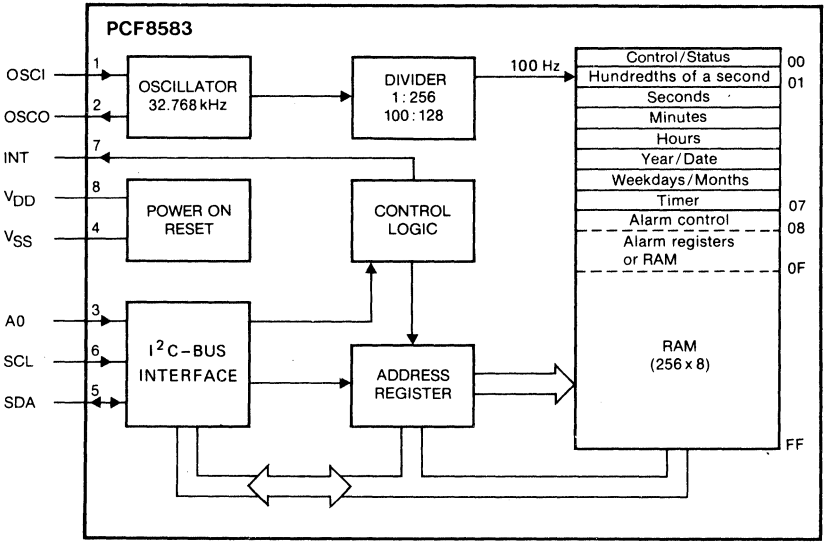


Fig.1 Block diagram.

PACKAGE OUTLINES

PCF8583P: 8-lead DIL; plastic (SOT97).
PCF8583T: 8-lead mini-pack; plastic (SO8L; SOT176A).

PINNING

1	OSCI	oscillator input, 50 Hz or event-pulse input
2	OSCO	oscillator output
3	A0	address input
4	V_{SS}	negative supply
5	SDA	serial data line (I²C-bus)
6	SCL	serial clock line (I²C-bus)
7	INT	open drain interrupt output (active low)
8	V_{DD}	positive supply

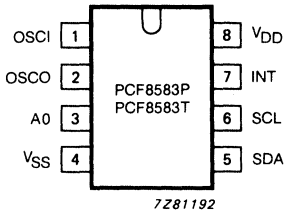


Fig.2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range (pin 8)	V_{DD}	−0.8	+ 7.0	V
Supply current (pin 4 or pin 8)	I_{DD}; I_{SS}	−	50	mA
Input voltage range	V_I	−0.8 to V_{DD}	+ 0.8	V
DC input current	I_I	−	10	mA
DC output current	I_O	−	10	mA
Power dissipation per package	P_{tot}	−	300	mW
Power dissipation per output	P_O	−	50	mW
Operating ambient temperature range	T_{amb}	−40	+ 85	°C
Storage temperature range	T_{stg}	−65	+ 150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is good practice to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

FUNCTIONAL DESCRIPTION

The PCF8583 contains a 256 by 8-bit RAM with an 8-bit auto-increment address register, an on-chip 32.768 kHz oscillator circuit, a frequency divider, a serial two-line bidirectional I^2C-bus interface and a power-on reset circuit.

The first 8 bytes of the RAM (memory addresses 00 to 07) are designed as addressable 8-bit parallel registers. The first register (memory address 00) is used as a control/status register. The memory addresses 01 to 07 are used as counters for the clock function. The memory addresses 08 to 0F are free RAM locations or may be programmed as alarm registers.

Counter function modes

When the control/status register is set a 32.768 kHz clock mode, a 50 Hz clock mode or an event-counter mode can be selected.

In the clock modes the hundredths of a second, seconds, minutes, hours, date, month (four year calendar) and weekdays are stored in a BCD format. The timer register stores up to 99 days. The event-counter mode is used to count pulses applied to the oscillator input (OSCO left open). The event counter stores up to 6 digits of data.

When one of the counters is read (memory locations 01 to 07), the contents of all counters are strobed into capture latches at the beginning of a read cycle. Therefore faulty reading of the count during a carry condition is prevented.

When a counter is written, other counters are not affected.

Alarm function modes

By setting the alarm enable bit of the control/status register the alarm control register (address 08) is activated.

By setting the alarm control register a dated alarm, a daily alarm, a weekday alarm or a timer alarm may be programmed. In the clock modes, the timer register (address 07) may be programmed to count hundredths of a second, seconds, minutes, hours or days. Days are counted when an alarm is not programmed.

Whenever an alarm event occurs the alarm flag of the control/status register is set. A timer alarm event will set the alarm flag and an overflow condition of the timer will set the timer flag. The open drain interrupt output is switched on (active LOW) when the alarm or timer flag is set (enabled). The flags remain set until directly reset by a write operation.

When a timer function without any alarm function is programmed the remaining alarm registers (addresses 09 to 0F) may be used as free RAM space.

Control/status register

The control/status register is defined as the memory location 00 with free access for reading and writing via the I²C-bus. All functions and options are controlled by the contents of the control/status register (see Fig.3).

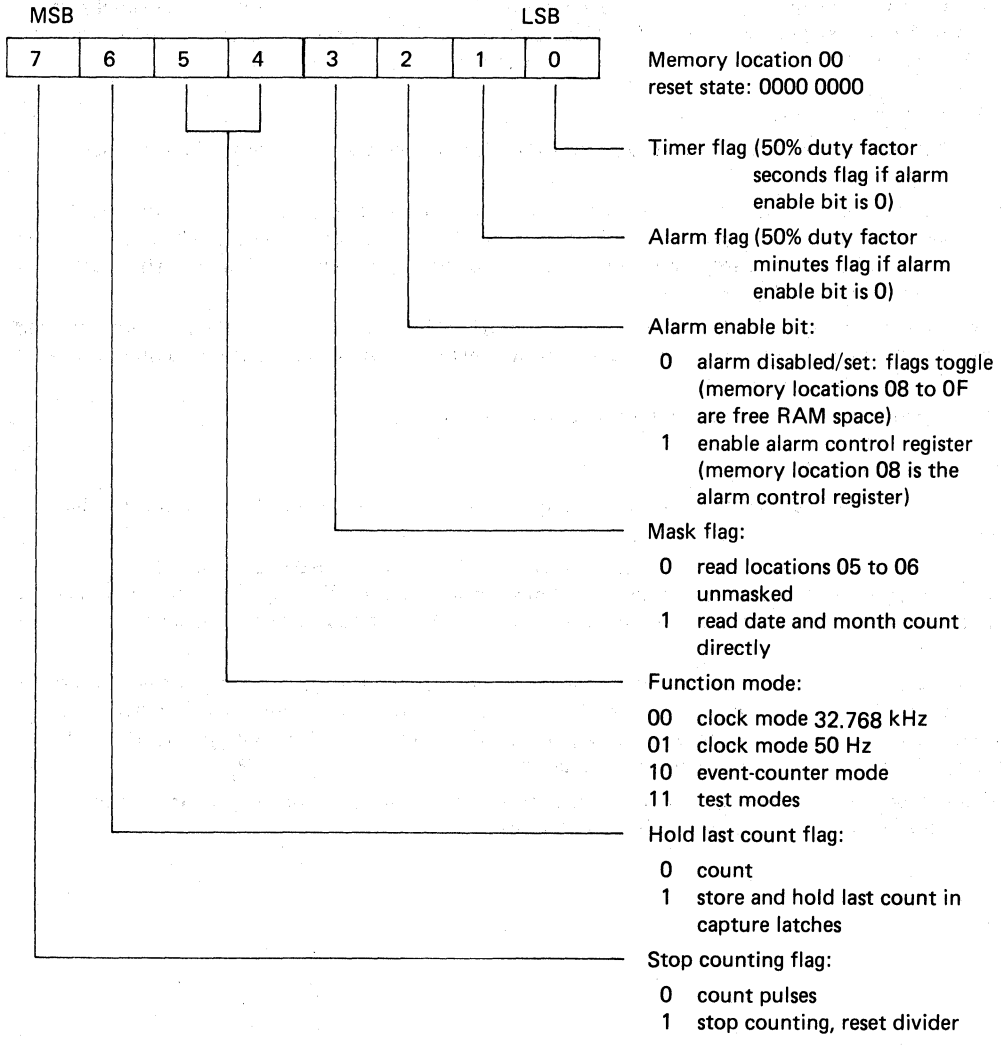


Fig.3 Control/status register.

Counter registers

In the different modes the counter registers are programmed and arranged as shown in Fig.4. Counter cycles are listed in Table 1.

In the clock modes 24 h or 12 h format can be selected by setting the most significant bit of the hours counter register. The format of the hours counter is shown in Fig.5.

The year and date are packed into memory location 05 (see Fig.6). The weekdays and months are packed into memory location 06 (see Fig.7). When reading these memory locations the year and weekdays are masked out when the mask flag of the control/status register is set. This allows the user to read the date and month count directly.

In the event-counter mode events are stored in BCD format. D5 is the most significant and D0 the least significant digit. The divider is by-passed.

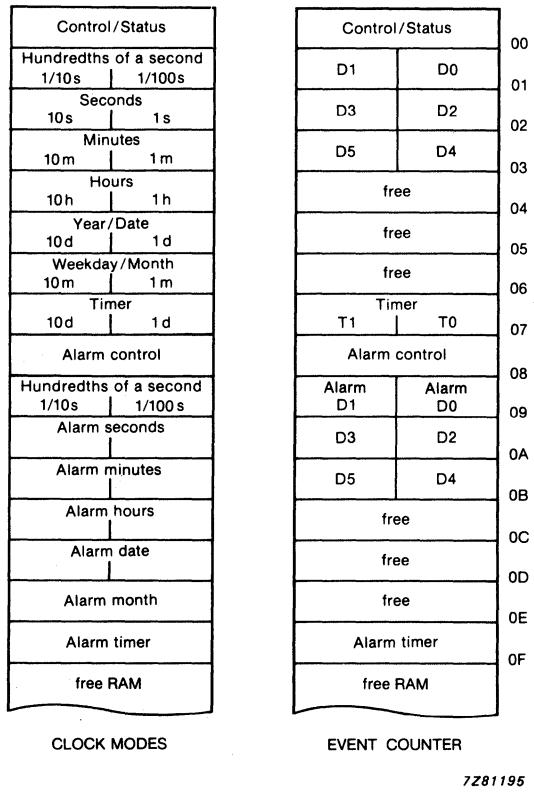
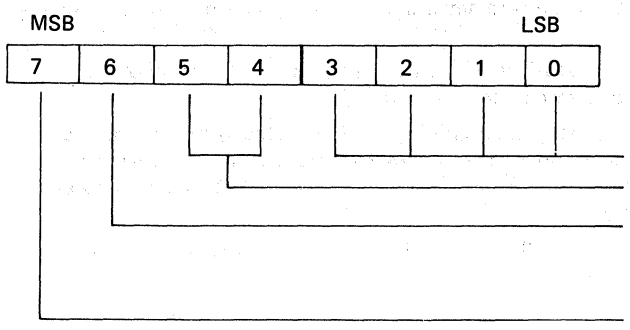


Fig.4 Register arrangement.

Counter registers (continued)



Memory location 04 (hours counter)
reset state: 0000 0000

Unit hours BCD

Ten hours (0 to 2 binary)

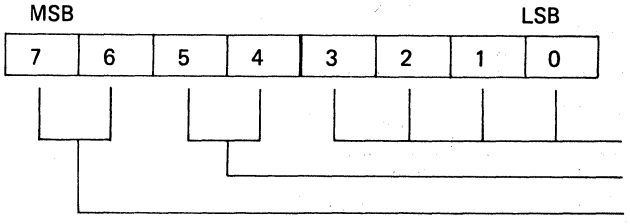
AM/PM flag:

0 AM
1 PM

Format:

0 24 h format, AM/PM flag remains unchanged
1 12 h format, AM/PM flag will be updated

Fig.5 Format of the hours counter.



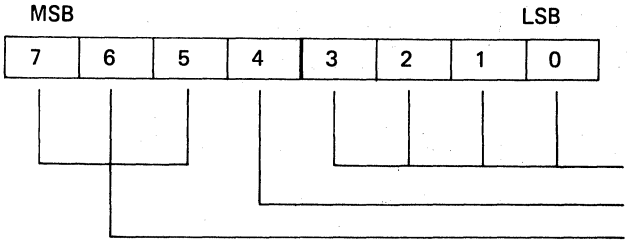
Memory location 05 (year/date)
reset state: 0000 0001

Unit days BCD

Ten days (0 to 3 binary)

Year (0 to 3 binary, read as 0 if the mask flag is set)

Fig.6 Format of the year/date counter.



Memory location 06 (weekdays/months)
reset state: 0000 0001

Unit months BCD

Ten months

Weekdays (0 to 6 binary, read as 0 if the mask flag is set)

Fig.7 Format of the weekdays/months counter.

Table 1 Cycle length of the time counters, clock modes

unit	counting cycle	carry to the next unit	contents of the month counter
hundredths of a second	00 to 99	99 to 00	
seconds	00 to 59	59 to 00	
minutes	00 to 59	59 to 00	
hours (24 h)	00 to 23	23 to 00	
hours (12 h)	12 AM, 01 AM to 11 AM, 12 PM, 01 PM to 11 PM	11 PM to 12 AM	
date	01 to 31 01 to 30 01 to 29 01 to 28	31 to 01 30 to 01 29 to 01 28 to 01	1, 3, 5, 7, 8, 10, 12 4, 6, 9, 11 2, year = 0 2, year = 1, 2, 3
months	01 to 12	12 to 01	
year	0 to 3		
weekdays	0 to 6	6 to 0	
timer	00 to 99	no carry	

DEVELOPMENT DATA

Alarm control register

When the alarm enable bit of the control/status register is set the alarm control register (address 08) is activated. All alarm, timer and interrupt output functions are controlled by the contents of the alarm control register (see Figs 8a and 8b).

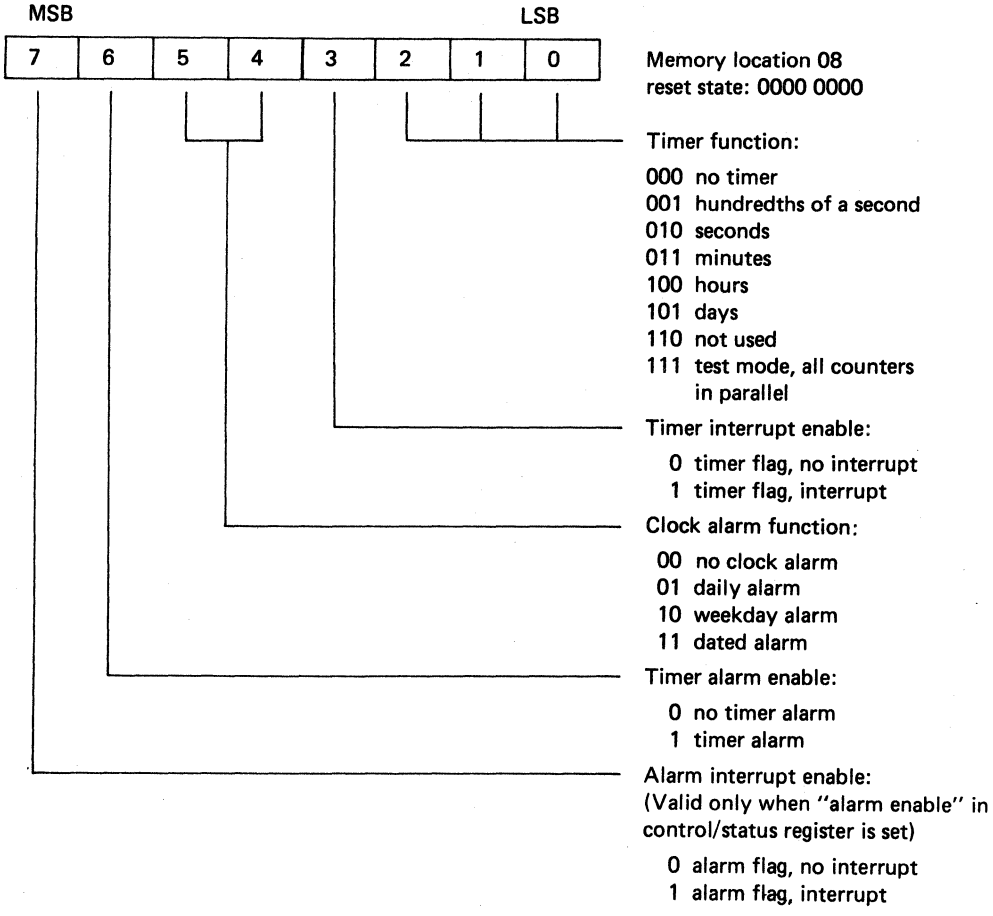


Fig.8a Alarm control register, clock modes.

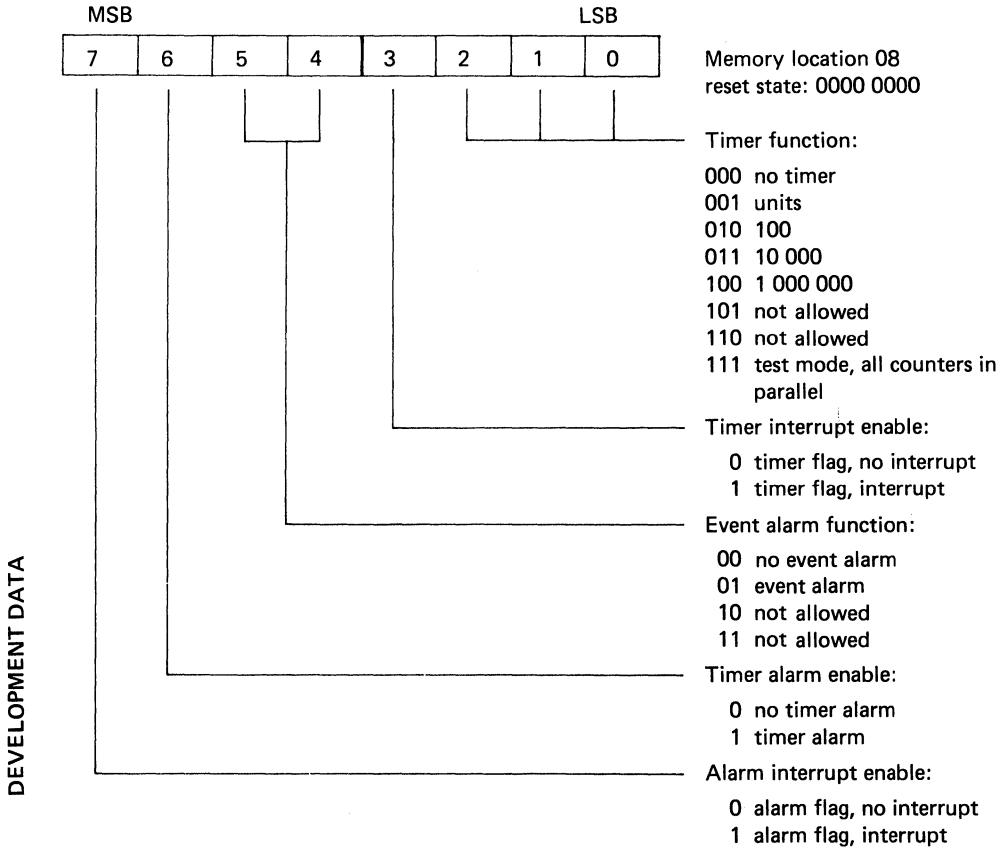


Fig.8b Alarm control register, event-counter mode.

Alarm registers

All alarm registers are allocated with a constant address offset of hex 08 to the corresponding counter registers.

An alarm goes off when the contents of the alarm registers matches bit-by-bit the contents of the involved counter registers. The year and weekday bits are ignored in a dated alarm. A daily alarm ignores the month and date bits. When a weekday alarm is selected, the contents of the alarm weekday/month register will select the weekdays on which an alarm is activated (see Fig.9).

Note: In the 12 h mode bits 6 and 7 of the alarm hours register must be the same as the hours counter.

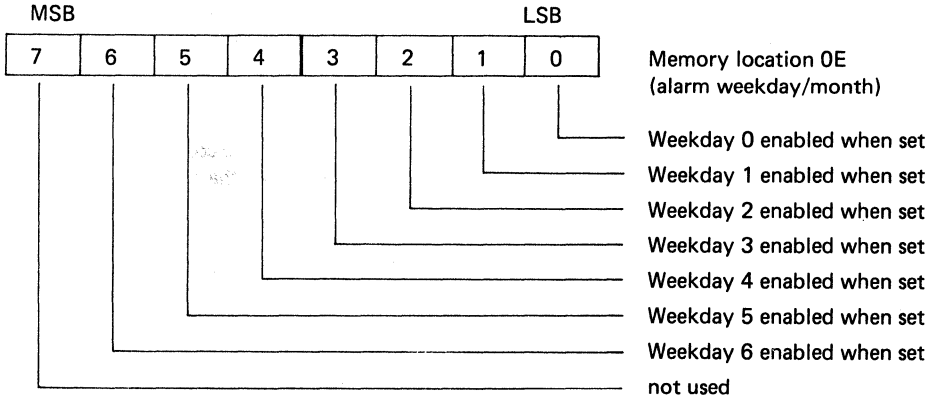


Fig.9 Selection of alarm weekdays.

Interrupt output

The open-drain n-channel interrupt output is programmed by setting the alarm control register. It is switched on (active LOW) when the alarm flag or the timer flag is set. In the clock mode without alarm the output sequence is controlled by the timer flag. The OFF voltage of the interrupt output may exceed the supply voltage.

Oscillator and divider

A 32.768 kHz quartz crystal has to be connected to OSCI (pin 1) and OSCO (pin 2). A trimmer capacitor between OSCI and V_{DD} is used for tuning the oscillator (see quartz frequency adjustment). A 100 Hz clock signal is derived from the quartz oscillator for the clock counters.

In the 50 Hz clock mode or event-counter mode the oscillator is disabled and the oscillator input is switched to a high impedance state. This allows the user to feed the 50 Hz reference frequency or an external high speed event signal into the input OSCI.

Initialization

When power-up occurs the I²C-bus interface, the control/status register and all clock counters are reset. The device starts time keeping in the 32.768 kHz clock mode with the 24 h format on the first of January at 0.00.00: 00. 1 Hz is output at the interrupt (starts HIGH). This can be disabled by setting the alarm enable bit in the control/status register.

A second level-sensitive reset signal to the I²C-bus interface is generated as soon as the supply voltage drops below the interface reset level. This reset signal does not affect the control/status or clock counter registers.

It is recommended to set the stop counting flag of the control/status register before loading the actual time into the counters. Loading of illegal states will lead to a clock malfunction but will not latch-up the device.

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

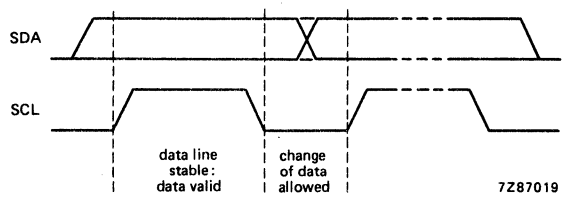


Fig.10 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH, is defined as the stop condition (P).

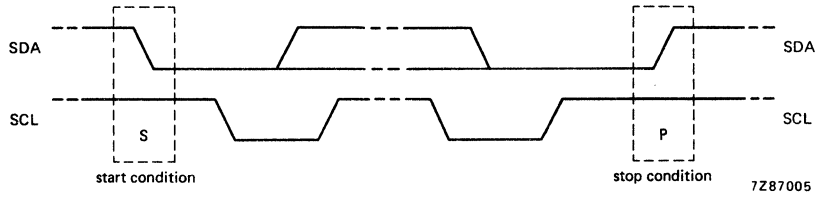


Fig.11 Definition of start and stop condition.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

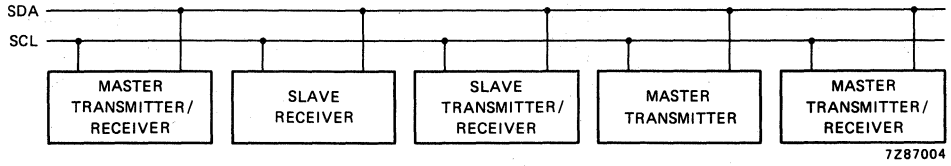


Fig.12 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each data byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master also generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledge has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

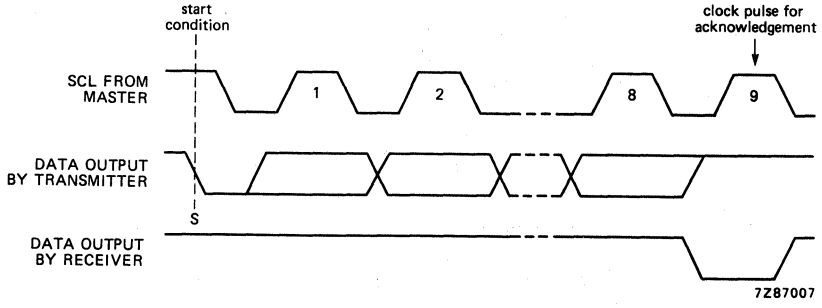


Fig.13 Acknowledgement on the I²C-bus.

DEVELOPMENT DATA

Timing specifications

All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

parameter	symbol	min.	typ.	max.	unit
SCL clock frequency	f_{SCL}	–	–	100	kHz
Tolerable spike width on bus	t_{SW}	–	–	100	ns
Bus free time	t_{BUF}	4.7	–	–	μs
Start condition set-up time	$t_{SU;STA}$	4.7	–	–	μs
Start condition hold time	$t_{HD;STA}$	4.0	–	–	μs
SCL LOW time	t_{LOW}	4.7	–	–	μs
SCL HIGH time	t_{HIGH}	4.0	–	–	μs
SCL and SDA rise time	t_r	–	–	1.0	μs
SCL and SDA fall time	t_f	–	–	0.3	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Data hold time	$t_{HD;DAT}$	0	–	–	ns
SCL LOW to data out valid	$t_{VD;DAT}$	–	–	3.4	μs
Stop condition set-up time	$t_{SU;STO}$	4.0	–	–	μs

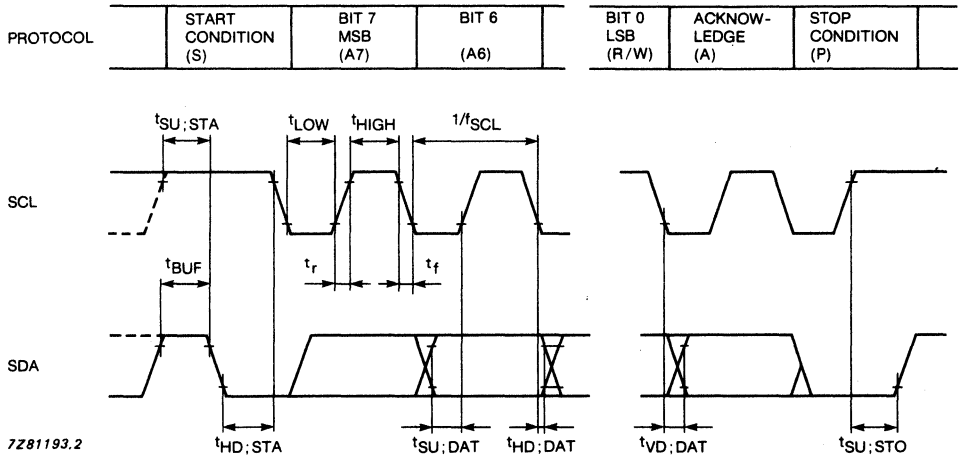


Fig. 14 I^2C-bus timing diagram; rise and fall times refer to V_{IL} and V_{IH}.

I²C-bus protocol

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure. The I²C-bus configuration for the different PCF8583 READ and WRITE cycles is shown in Fig.15.

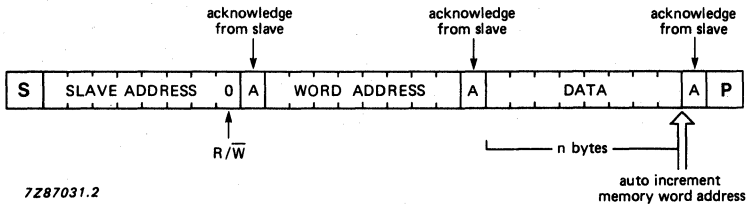


Fig.15a Master transmits to slave receiver (WRITE mode).

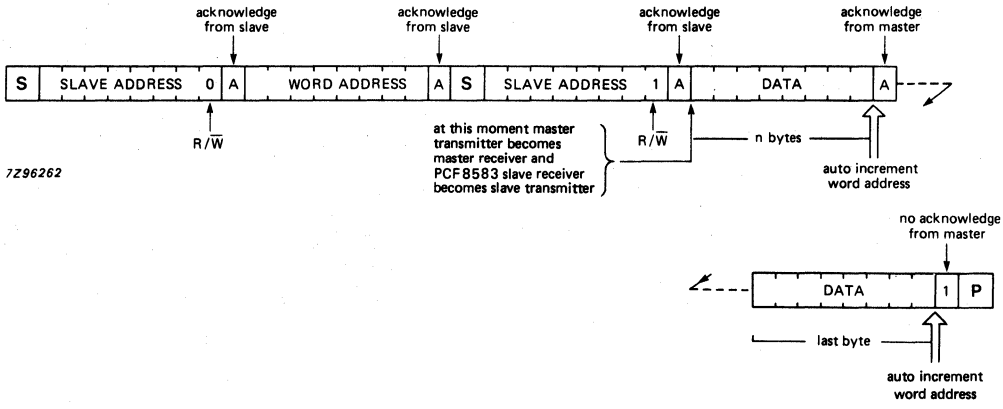


Fig.15b Master reads after setting word address (WRITE word address; READ data).

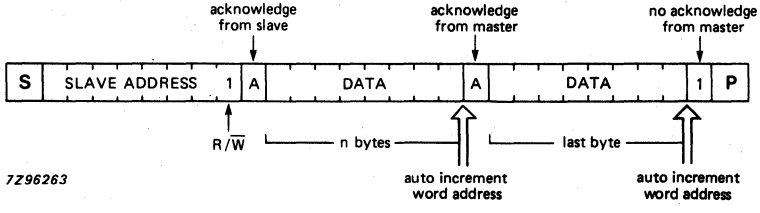


Fig.15c Master reads slave immediately after first byte (READ mode).

DEVELOPMENT DATA

CHARACTERISTICS

V_{DD} = 2.5 to 6.0 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage						
operating		V_{DD}	2.5	–	6.0	V
clock	T_{amb} = 0 to + 70 °C	V_{DD}	1.0	–	6.0	V
Supply current						
operating	f_{SCL} = 100 kHz	I_{DD}	–	–	200	μA
clock	V_{DD} = 5 V	I_{DDO}	–	10	50	μA
clock	V_{DD} = 1 V	I_{DDO}	–	2	10	μA
Power-on reset voltage level	note 1	V_{POR}	1.5	1.9	2.3	V
Inputs; Input/output SDA						
Input voltage LOW	note 2	V_{IL}	−0.8	–	$0.3V_{DD}$	V
Input voltage HIGH	note 2	V_{IH}	$0.7V_{DD}$	–	V_{DD} + 0.8	V
Output current LOW	V_{OL} = 0.4 V	I_{OL}	3	–	–	mA
Leakage current	$V_I = V_{DD}$ or V_{SS}	$\|I_L\|$	–	–	1	μA
A0; OSCI						
Input leakage current	$V_I = V_{DD}$ or V_{SS}	$\|I_{LI}\|$	–	–	250	nA
SCL; SDA						
Input capacitance	$V_I = V_{SS}$	C_I	–	–	7	pF
Output INT						
Output current LOW	V_{OL} = 0.4 V	I_{OL}	3	–	–	mA
Leakage current	$V_I = V_{DD}$ or V_{SS}	$\|I_L\|$	–	–	1	μA
LOW V_{DD} data retention						
Supply voltage for data retention		V_{DDR}	1	–	6	V
Supply current	note 3					
	V_{DDR} = 1 V T_{amb} = −25 to + 70 °C;	I_{DDR}	–	–	5	μA
	V_{DDR} = 1 V	I_{DDR}	–	–	2	μA

parameter	conditions	symbol	min.	typ.	max.	unit
Oscillator						
Integrated oscillator capacitance		C_{OSC}	–	40	–	pF
Oscillator stability for ΔV_{DD} = 100 mV	T_{amb} = 25 °C; V_{DD} = 1.5 V	f/fOSC	–	2×10^{-7}	–	
Input frequency	note 4	f_i	–	–	1	MHz
Quartz crystal parameters						
Frequency = 32.768 kHz						
Series resistance		R_S	–	–	40	kΩ
Parallel capacitance		C_L	–	10	–	pF
Trimmer capacitance		C_T	5	–	25	pF

Notes to the characteristics

1. The power-on reset circuit resets the I²C-bus logic when $V_{DD} < V_{POR}$.
2. When the voltages are a diode voltage above or below the supply voltage V_{DD} or V_{SS} an input current will flow; this current must not exceed ± 0.5 mA.
3. Event or 50 Hz mode only (no Quartz).
4. Event mode only.

APPLICATION INFORMATION

Quartz frequency adjustment

Method 1: Fixed OSCI capacitor

By evaluating the average capacitance necessary for the application layout a fixed capacitor can be used. The frequency is best measured via the 1 Hz signal available after power-on at the interrupt output (pin 7). The frequency tolerance depends on the quartz crystal tolerance, the capacitor tolerance and the device-to-device tolerance (on average ± 5×10^{-6}). Average deviations of ± 5 minutes per year can be achieved.

Method 2: OSCI Trimmer

Using the alarm function (via the I²C-bus) a signal faster than 1 Hz can be generated at the interrupt output for fast setting of a trimmer.

Procedure:

Power-on
Initialization (alarm function)

Routine:

Set clock to time T and set alarm to time T + dT.
At time T + dT (interrupt) repeat routine.

If time dT is approximately 10 ms a frequency of approximately 40 Hz is obtained.

DEVELOPMENT DATA

APPLICATION INFORMATION (continued)

The PCF8583 slave address has a fixed combination 1010 as group 1.

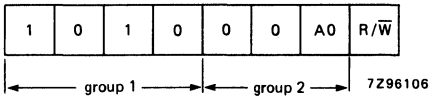
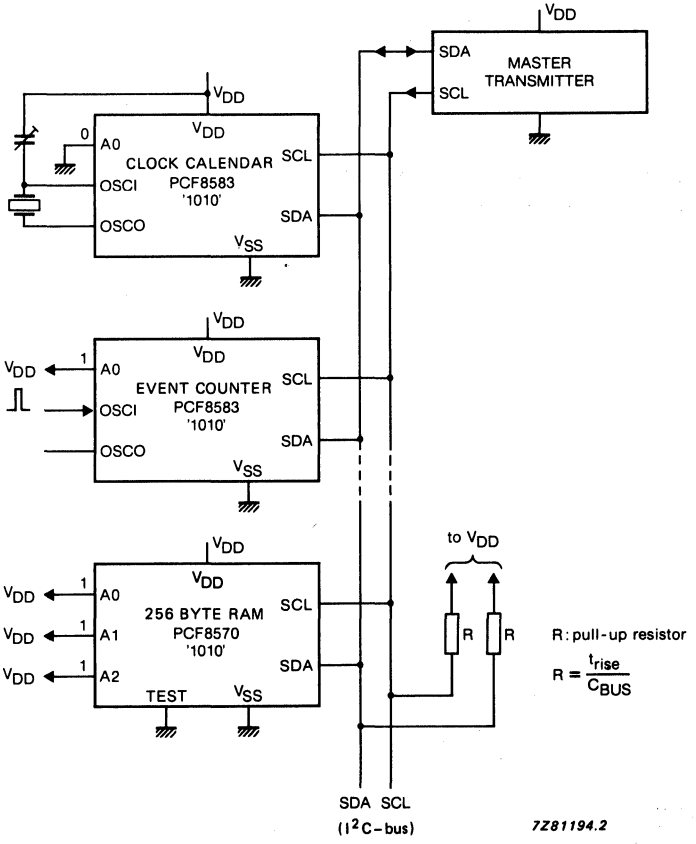


Fig.16 PCF8583 address.



Recommendation:
Connect a 4.7 μF 10 V solid aluminium (SAL) capacitor between V_{DD} and V_{SS}.

Fig.17 PCF8583 application diagram.

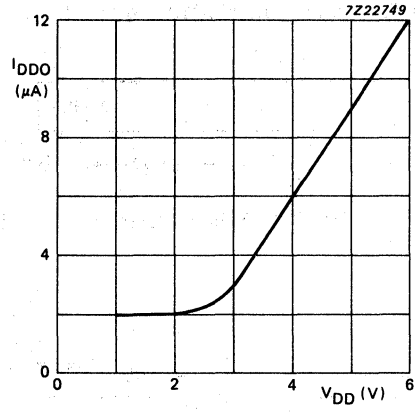


Fig.18 Typical supply current as a function of supply voltage (clock); $T_{amb} = -40$ to + 85 °C.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

CMOS EEPROM

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PCA8582B	**256 x 8-bit static EEPROM with I^2C-bus interface for automotive applications**	**139**
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PCF8582C	**256 x 8-bit static EEPROM with I^2C-bus interface for automotive applications**	**171**

256 x 8-BIT STATIC CMOS EEPROM WITH I²C-BUS INTERFACE FOR AUTOMOTIVE APPLICATIONS

GENERAL DESCRIPTION

The PCA8582B is a 2 Kbit (256 x 8 bit) floating gate electrically erasable programmable read only memory (EEPROM). By using an internal redundant storage code it is fault tolerant to single bit errors. This feature dramatically increases reliability compared to conventional EEPROM memories.

Power consumption is low due to the full CMOS technology used. The programming voltage is generated on chip using a voltage multiplier.

As data bytes are received and transmitted via the serial I²C-bus, an eight pin DIL package is sufficient. Up to eight PCA8582B devices may be connected to the I²C-bus.

Chip select is accomplished by three address inputs.

Timing of the Erase/Write cycle can be done in two ways: either by connecting an external clock to the "Programming Time Control (PTC)" pin (7) or by using an internal oscillator. In the latter application an RC time constant must be connected to pin 7.

Features

- Non-volatile storage of 2 Kbits organized as 256 x 8 bits
- High reliability by using a redundant storage code (single bit error correction)
- Only one power supply required
- On chip voltage multiplier for erase/write
- Serial input/output bus (I²C)
- Automatic word address incrementing
- Low power consumption
- One point erase/write timer
- Power on reset
- Up to 500 000 erase/write cycles per byte
- 10 years non-volatile data retention time
- Infinite number of read cycles
- Pin and address compatible to PCF8570, PCF8571 and PCD8572
- External clock signal possible
- Extended temperature range: −40 to + 125 °C

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage range	V_{DD}	4.5	5	5.5	V
Operating supply current READ	I_{DD}	–	–	0.6	mA
Operating supply current WRITE/ERASE	I_{DD}	–	–	2	mA
Standby supply current	I_{DD0}	–	–	20	μA

PACKAGE OUTLINES

PCA8582BP: 8-lead DIL, plastic (SOT97).
PCA8582BT: 16-lead mini-pack; plastic (SO16L; SOT162A).

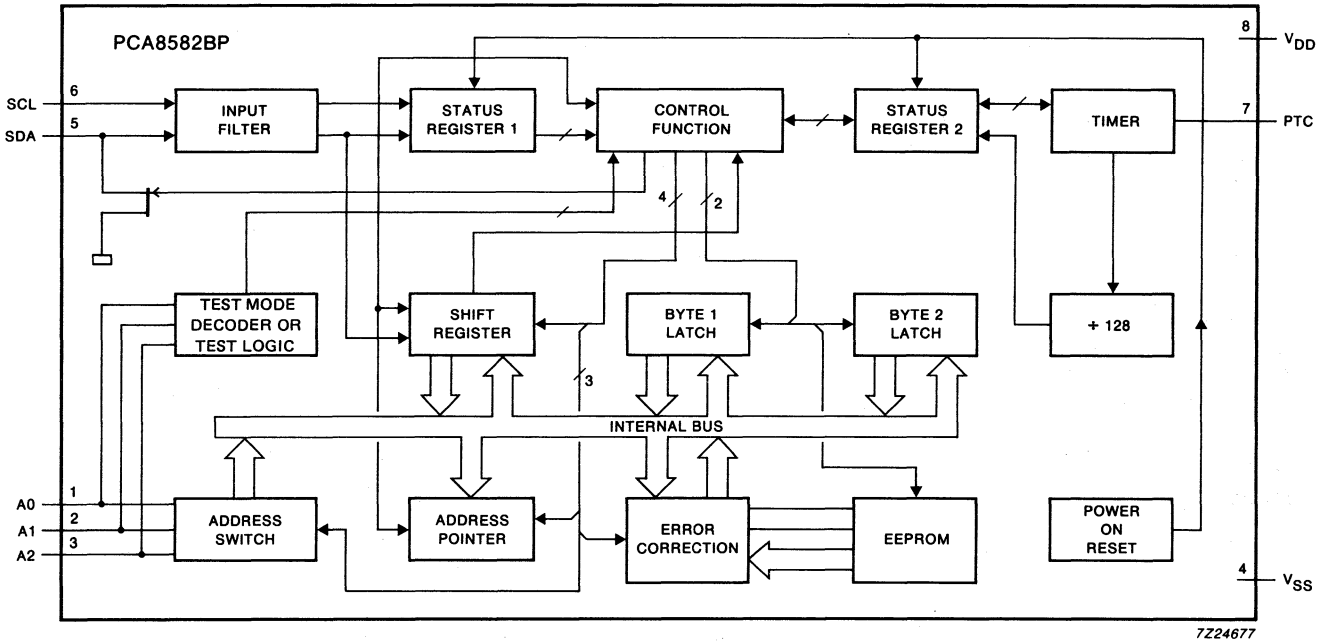


Fig.1 Block diagram for PCA8582BP.

DEVELOPMENT DATA

PINNING

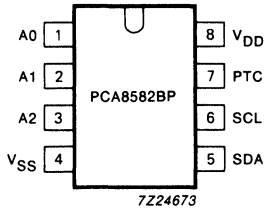


Fig.2 (a) Pinning diagram (PCA8582BP).

1	A0	address inputs
2	A1	
3	A2	
4	V_{SS}	ground
5	SDA	I^2C-bus lines
6	SCL	
7	PTC	programming time control
8	V_{DD}	positive supply voltage

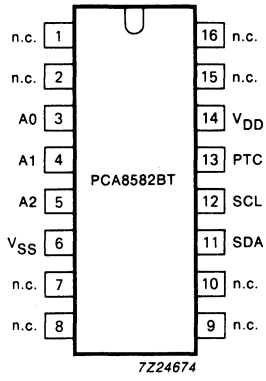


Fig.2 (b) Pinning diagram (PCA8582BT).

1	n.c.	not connected
2	n.c.	
3	A0	address inputs
4	A1	
5	A2	
6	V_{SS}	ground
7	n.c.	not connected
8	n.c.	
9	n.c.	
10	n.c.	
11	SDA	I^2C-bus lines
12	SCL	
13	PTC	programming time control
14	V_{DD}	positive supply voltage
15	n.c.	not connected
16	n.c.	

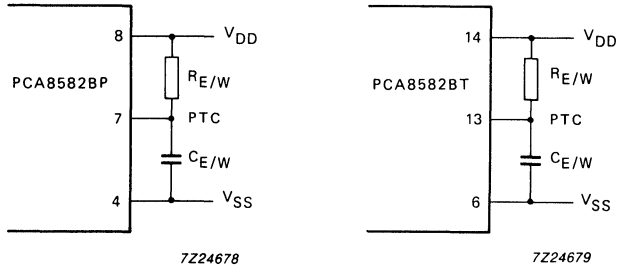


Fig.3 PTC circuit when using an internal oscillator (a) PCA8582BP (b) PCA8582BT.

FUNCTIONAL DESCRIPTION

Characteristics of the I²C-bus

The I²C-bus is intended for communication between different ICs. This serial bus consists of two bidirectional lines: one for data signals (SDA), and one for clock signals (SCL). Both the SDA and the SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

The following bus conditions have been defined:

Bus not busy: both data and clock lines remain HIGH.
Start data transfer: a change in the state of the data line, from HIGH-to-LOW, while the clock is HIGH defines the start condition.
Stop data transfer: a change in the state of the data line, from LOW-to-HIGH, while the clock is HIGH, defines the stop condition.
Data valid: the state of the data line represents valid data when, after a start condition, the data line is stable for the duration of the HIGH period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition; the number of the data bytes, transferred between the start and stop conditions is limited to two bytes in the ERASE/WRITE mode and unlimited in the READ mode. The information is transmitted in bytes and each receiver acknowledges with a ninth bit.

Within the I²C-bus specifications a low speed mode (2 kHz clock rate) and a high speed mode (100 kHz clock rate) are defined. The PCA8582B operates in both modes.

By definition a device that sends a signal is called a "transmitter", and the device which receives the signal is called a "receiver". The device which controls the signal is called the "master". The devices that are controlled by the master are called "slaves".

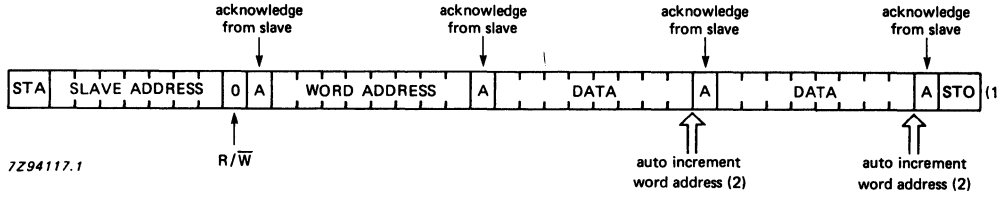
Each byte of eight bits is followed by one acknowledge bit. This acknowledge bit is a HIGH level put on the bus by the transmitter. The master generates an extra acknowledge related clock pulse.
The slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte.
The master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.
The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse.
Set-up and hold times must be taken into account. A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master generation of the stop condition.

Note

Detailed specifications of the I²C-bus are available on request.

I²C-Bus Protocol

The I²C-bus configurations for different READ and WRITE cycles of the PCA8582B are shown in Fig.4, (a) (b) and (c).



(1) After this stop condition the erase/write cycle starts and the bus is free for another transmission. Its duration is 30 ms if only one byte is written and 60 ms if two bytes are written. During the erase/write cycle the slave receiver does not send an acknowledge bit if addressed via the I²C-bus.
(2) The second data byte is voluntary. It is not allowed to erase/write more that two bytes.

Fig.4 (a) Master transmitter transmits to PCA8582B slave receiver (ERASE/WRITE mode).

DEVELOPMENT DATA

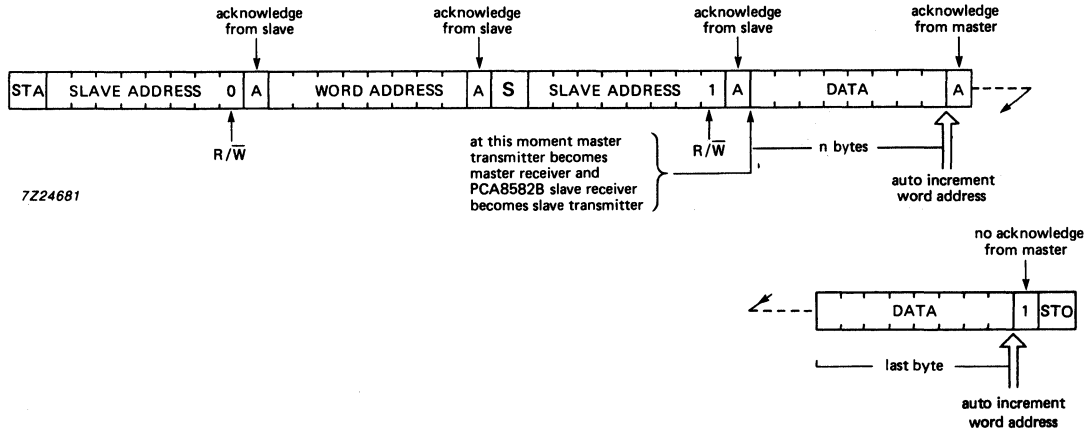


Fig.4 (b) Master reads PCA8582B slave after setting word address (WRITE word address; READ data).

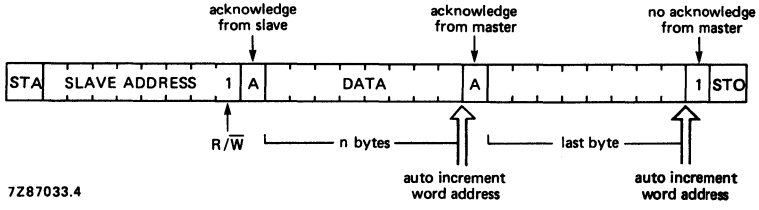


Fig.4 (c) Master reads PCA8582B slave immediately after first byte (READ mode).

FUNCTIONAL DESCRIPTION (continued)

Chip address (slave address) allocation

Three chip address inputs (A0, A1, A2) can produce eight different chip addresses. This means that up to eight different PCA8582B devices may be connected to the I²C-bus. Address allocation is illustrated by Fig.5.

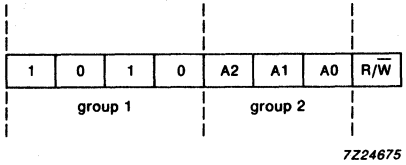


Fig.5 Slave address.

I²C-bus timing

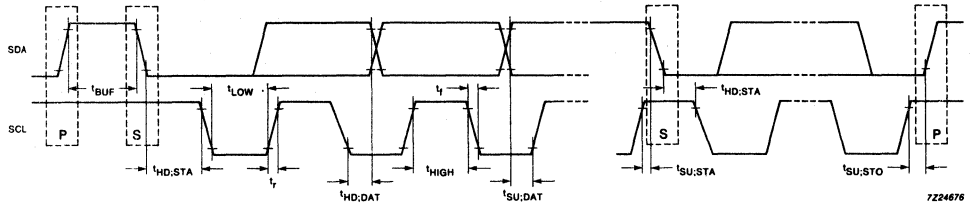


Fig.6 I²C-bus timing.

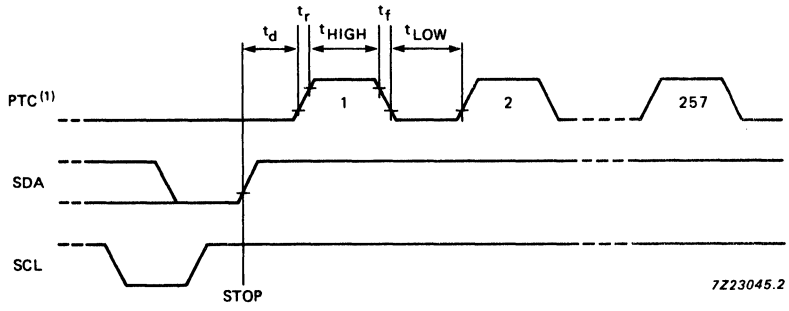


Fig.7 (a) One byte ERASE/WRITE cycle.

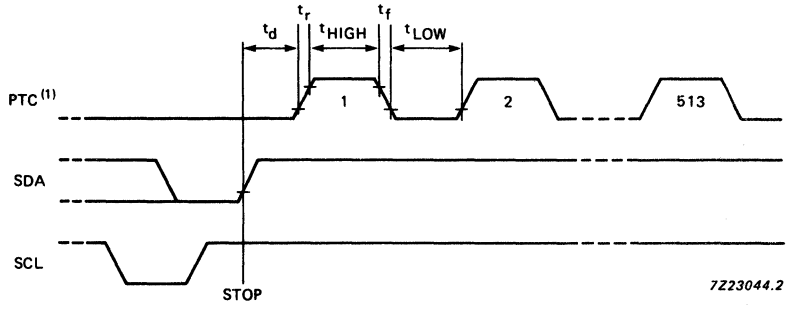


Fig.7 (b) Two byte ERASE/WRITE cycles.

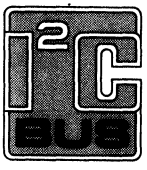
DEVELOPMENT DATA

(1) If an external clock is chosen for the PTC, this information is latched internally by leaving pin 7 LOW after transmission of the eighth bit of the word address (negative edge of SCL). The state of the PTC then, may be previously undefined.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	V_{DD}	−0.3	+7	V
Voltage on any input pin input impedance > 500 Ω	V_I	V_{SS} − 0.8	V_{DD} + 0.8	V
Operating ambient temperature range	T_{amb}	−40	+ 125	°C
Storage temperature range	T_{stg}	−65	+ 150	°C
Current into any input pin	$\|I_I\|$	−	1	mA
Output current	$\|I_O\|$	−	10	mA



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

DEVELOPMENT DATA

CHARACTERISTICS

V_{DD} = 5 V; V_{SS} = 0 V; T_{amb} = −40 to + 125 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Operating supply voltage		V_{DD}	4.5	5	5.5	V
Operating supply current READ	V_{DD} = 5.5 V; f_{SCL} = 100 kHz	I_{DD}	–	–	0.6	mA
Operating supply current WRITE/ERASE	V_{DD} = 5.5 V	I_{DDW}	–	–	2.0	mA
Standby supply current	V_{DD} = 5.5 V	I_{DDO}	–	–	20	μA
Input PTC						
Input voltage HIGH		V_{IH}	V_{DD}−0.3	–	–	V
Input voltage LOW		V_{IL}	–	–	V_{SS}+0.3	V
Input SCL and input/output SDA						
Input voltage HIGH		V_{IH}	3.0	–	V_{DD}+0.8	V
Input voltage LOW		V_{IL}	−0.3	–	1.5	V
Output voltage LOW	I_{OH} = 3 mA; V_{DD} = 4.5 V	V_{OL}	–	–	0.4	V
Output leakage current HIGH	$V_{OH} = V_{DD}$	I_{LO}	–	–	10	μA
Input leakage current (SCL)	$V_I = V_{DD}$ or V_{SS}	$\pm I_{LI}$	–	–	10	μA
Clock frequency	$V_I = V_{SS}$	f_{SCL}	0	–	100	kHz
Input capacitance (SCL; SDA)		C_I	–	–	7	pF
Time the bus must be free before new transmission can start		t_{BUF}	4.7	–	–	μs
Start condition hold time after which first clock pulse is generated		$t_{HD;STA}$	4	–	–	μs
The LOW period of the clock		t_{LOW}	4.7	–	–	μs
The HIGH period of the clock		t_{HIGH}	4	–	–	μs
Set-up time for start condition	repeated start	$t_{SU;STA}$	4.7	–	–	μs
Data hold time for I²C-bus compatible masters		$t_{HD;DAT}$	5	–	–	μs

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Data hold time for I^2C devices	note 1	$t_{HD;DAT}$	0	–	–	ns
Data set-up time		$t_{SU;DAT}$	250	–	–	ns
Rise time for SDA and SCL lines		t_r	–	–	1	μs
Fall time for SDA and SCL lines		t_f	–	–	300	ns
Set-up time for stop condition		$t_{SU,STO}$	4.7	–	–	μs
Erase/write cycle time		$t_{E/W}$	5	–	40	ms
Endurance (E/W cycles per byte)	note 2					
	T_{amb} = 125 °C $t_{E/W}$ = 5-40 ms	$N_{E/W}$	–	–	50 000	cycles
	T_{amb} = 85 °C $t_{E/W}$ = 5-40 ms	$N_{E/W}$	–	–	100 000	cycles
	T_{amb} = 33 °C $t_{E/W}$ = 10 ms	$N_{E/W}$	–	–	500 000	cycles
Data retention time	T_{amb} = 55 °C	t_S	10	–	-	years

Notes to the characteristics

1. An internal transmitter must provide a hold time (max. 300 ns) to bridge the undefined region of the falling edge of SCL.
2. Technical note in preparation.

E/W programming time control

A. Using an internal oscillator

Resistor $R_{E/W}$ connected between pin 7 and V_{DD} and capacitor $C_{E/W}$ connected between pin 7 and V_{SS} (see Table 1).

Table 1 Recommended RC combinations

$R_{E/W}$ (kΩ) note 1	$C_{E/W}$ (nF) note 2	$t_{E/W}$ (typ.) (ms) note 3
56	3.3	34
56	2.2	21
22	3.3	13
22	2.2	7.5 (note 4)

Notes to Table 1

1. Maximum tolerance is 10%.
2. Maximum tolerance is 5%.
3. E/W times are mainly influenced by the tolerances in values of R and C.
4. Minimum allowed $t_{E/W}$ is 5 ms (see CHARACTERISTICS). The tolerances of R and C over the whole temperature range.

B. Using an external clock (see Table 2 and Fig.7)

Table 2 E/W programming time control using an external clock

parameter	symbol	min.	max.	unit
frequency	f_p	10	50	kHz
period LOW	t_{LOW}	9	–	μs
period HIGH	t_{HIGH}	9	–	μs
rise time	t_r	–	300	ns
fall time	t_f	–	300	ns
delay time	t_d	0	t_{LOW}	ns

128 x 8-BIT EEPROM WITH I²C-BUS INTERFACE

GENERAL DESCRIPTION

The PCF8581 and PCF8581C are low-power CMOS EEPROMs with standard and wide operating voltage:
4.5 to 5.5 V (PCF8581); 2.5 to 6.0 V (PCF8581C).

In the following text, the generic term "PCF8581" is used to refer to both types in all packages except where specified.

The PCF8581 is organized as 128 words by 8-bits.

Addresses and data are transferred serially via a two-line bidirectional bus (I²C). The built-in word address register is incremented automatically after each written or read data byte. All bytes can be read in a single operation. Up to eight bytes can be written in one operation, reducing the total write time per byte. Three address pins A0, A1 and A2 are used to define the hardware address, allowing the use of up to eight devices connected to the bus without additional hardware.

Features

- Operating supply voltage: 4.5 to 5.5 V (PCF8581); 2.5 to 6.0 V (PCF8581C)
- Integrated voltage multiplier and timer for writing (no external components required)
- Automatic erase before write
- Low standby current max. 10 μA
- Eight-byte page write mode
- Serial input/output bus (I²C)
- Address by 3 hardware address pins
- Automatic word address incrementing
- Designed for 10 000 write cycles per byte minimum
- 10 years minimum non-volatile data retention
- Infinite number of read cycles
- Pin and address compatibility to PCF8570, PCF8571 and PCF8582

PACKAGE OUTLINES

PCF8581P/PCF8581CP: 8-lead DIL; plastic (SOT97).
PCF8581T/PCF8581CT: 8-lead mini-pack (SO-8L; SOT176C).

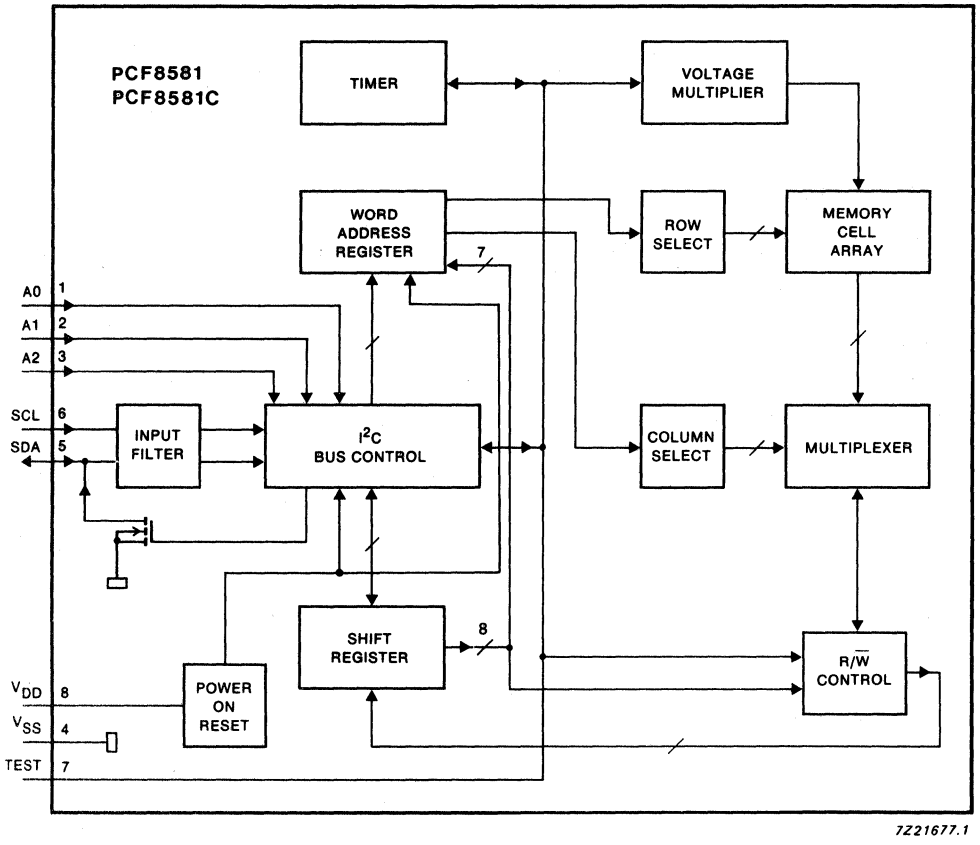


Fig.1 Block diagram.

DEVELOPMENT DATA

PINNING

1	A0	hardware address inputs	
2	A1		
3	A2		
4	V_{SS}	negative supply	
5	SDA	serial data input/output	I²C-bus
6	SCL	serial clock input	
7	TEST	test output can be connected to V_{SS}, V_{DD} or left open-circuit	
8	V_{DD}	positive supply	

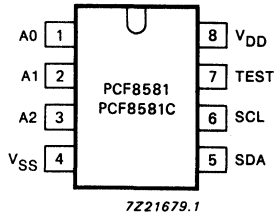


Fig.2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

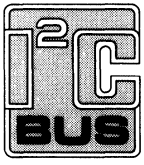
parameter	symbol	min.	max.	unit
Supply voltage range (pin 8)	V_{DD}	−0.3	7.0	V
Voltage range on any input*	V_I	−0.8	V_{DD}+0.8	V
DC input current (any input)	$\pm I_I$	–	10	mA
DC output current (any output)	$\pm I_O$	–	10	mA
Total power dissipation	P_{tot}	–	150	mW
Power dissipation per output	P	–	50	mW
Storage temperature range	T_{stg}	−65	+ 150	°C
Operating ambient temperature range	T_{amb}	−40	+ 85	°C

* Measured via a 500 Ω resistor.

CHARACTERISTICS

V_{DD} = 2.5 to 6 V (PCF8581C) 4.5 to 5.5 V (PCF8581); V_{SS} = 0 V; T_{amb} = −40 to + 85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range						
PCF8581C		V_{DD}	2.5	–	6.0	V
PCF8581		V_{DD}	4.5	–	5.5	V
Supply current						
standby	f_{SCL} = 0 Hz	I_{DD}	–	–	10	μA
operating	f_{SCL} = 100 kHz	I_{DD}	–	–	400	μA
during write	see bus protocol	I_{DD}	–	–	1000	μA
Inputs						
A0, A1, A2, SCL, SDA						
Input voltage LOW		V_{IL}	–	–	$0.3V_{DD}$	V
Input voltage HIGH		V_{IH}	$0.7V_{DD}$	–	–	V
Input leakage current	pin at V_{SS} or V_{DD}	I_{LI}	–	–	1	μA
Input capacitance	pin at V_{SS}	C_I	–	–	7	pF
Outputs						
SDA						
Output current LOW	pin at 0.4 V	I_{OL}	3	–	–	mA
TEST						
Output leakage current	pin at V_{SS} or V_{DD}	I_{LO}	–	–	1	μA
Erase/write data						
Write time		t_{WR}	6	–	12	ms
Data retention time		t_{RET}	10	–	–	years



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for two-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

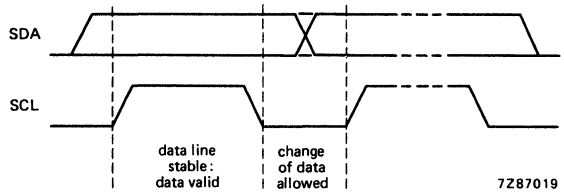


Fig. 3 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

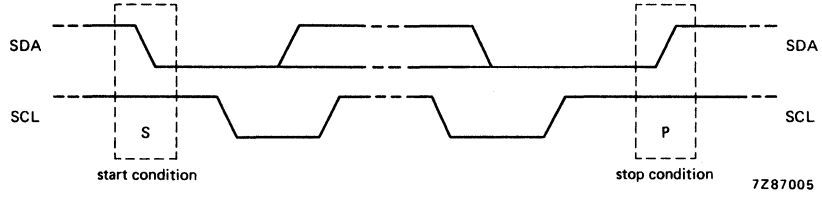


Fig. 4 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

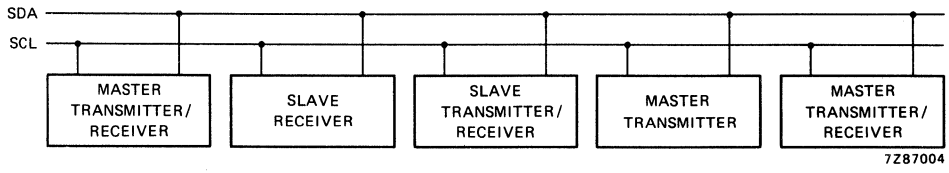


Fig. 5 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eigth bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by **not** generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

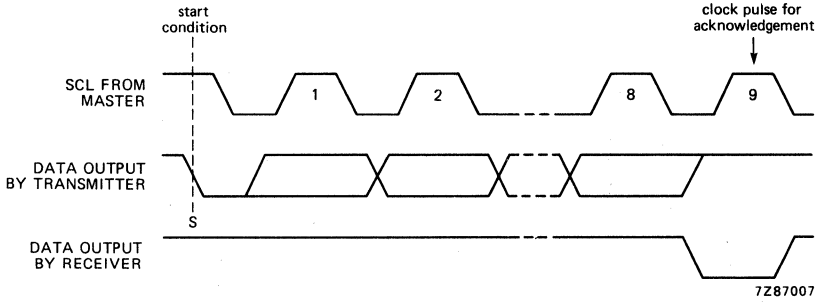


Fig. 6 Acknowledgement on the I^2C-bus.

DEVELOPMENT DATA

Timing specifications

All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

parameter	symbol	min.	typ.	max.	unit
SCL clock frequency	f_{SCL}	–	–	100	kHz
Tolerable spike width on bus	t_{SW}	–	–	100	ns
Bus free time	t_{BUF}	4.7	–	–	μs
Start condition set-up time	$t_{SU;STA}$	4.7	–	–	μs
Start condition hold time	$t_{HD;STA}$	4.0	–	–	μs
SCL LOW time	t_{LOW}	4.7	–	–	μs
SCL HIGH time	t_{HIGH}	4.0	–	–	μs
SCL and SDA rise time	t_r	–	–	1.0	μs
SCL and SDA fall time	t_f	–	–	0.3	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Data hold time	$t_{HD;DAT}$	0	–	–	ns
SCL LOW to data out valid	$t_{VD;DAT}$	–	–	3.4	μs
Stop condition set-up time	$t_{SU;STO}$	4.0	–	–	μs

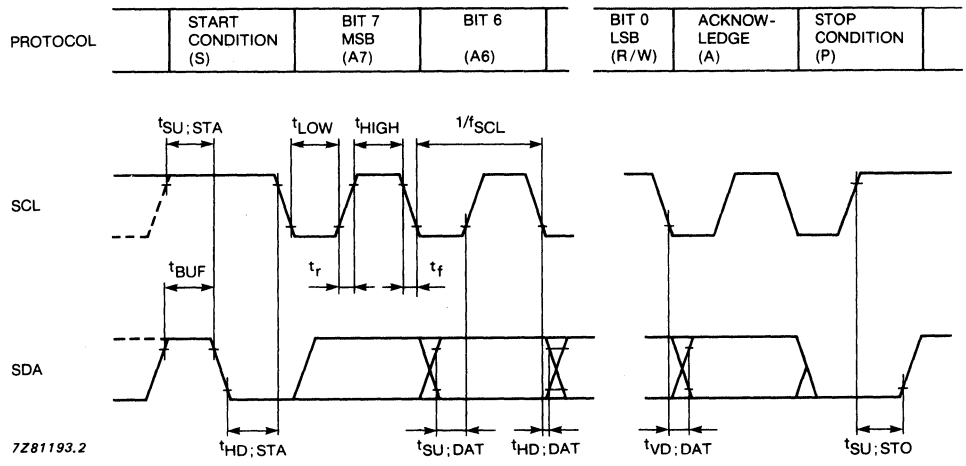


Fig. 7 I²C-bus timing diagram.

Bus protocol

Before any data is transmitted on the I^2C-bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure. The I^2C-bus configuration for PCF8581 WRITE cycle is shown in Fig. 8 and READ cycle in Figs 10 and 11.

Writing

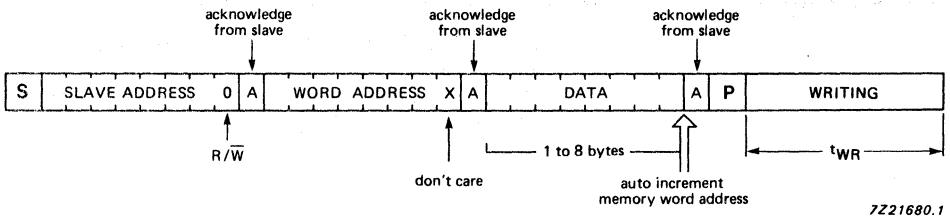


Fig. 8 Master transmits to slave receiver (WRITE mode).

After the word address, one to eight data bytes can be sent. The address is automatically incremented, but the four highest address bits (row) are internally latched. Therefore all bytes are written in the same row.

An example of writing eight bytes with word address X0000000 and six bytes with word address X0010101 is shown in Fig. 9. Where X = don't care.

word address	row	bytes							
X0000000	0	1 →	2 →	3 →	4 →	5 →	6 →	7 →	8 →
X0000001	1								
X0010101	2	4 →	5 →	6			1 →	2 →	3 →
X0011101	3								
	•								
	•								
column		0	1	2	3	4	5	6	7

Fig. 9 Writing eight and six bytes with different word addresses.

To transmit eight bytes in sequential order, begin with the lowest address bits 000. The data is written after a stop is detected. The data is only written if complete bytes have been received and acknowledged. Writing takes a time t_{WR} (6 to 12 ms) during which the device will not respond to its slave address. Note that to write the next row, a new write operation is required (start, slave address, row address, data, stop).

LIFE SUPPORT APPLICATIONS

Faselec's product is not designed for use in life support appliances, devices or systems where malfunction of above product can reasonably be expected to result in a personal injury. Faselec's customers using or selling Faselec's PCF8581/81C for use in life support applications do so at their own risk and agree to fully indemnify Faselec for any damages resulting from such improper use or sale.

Reading

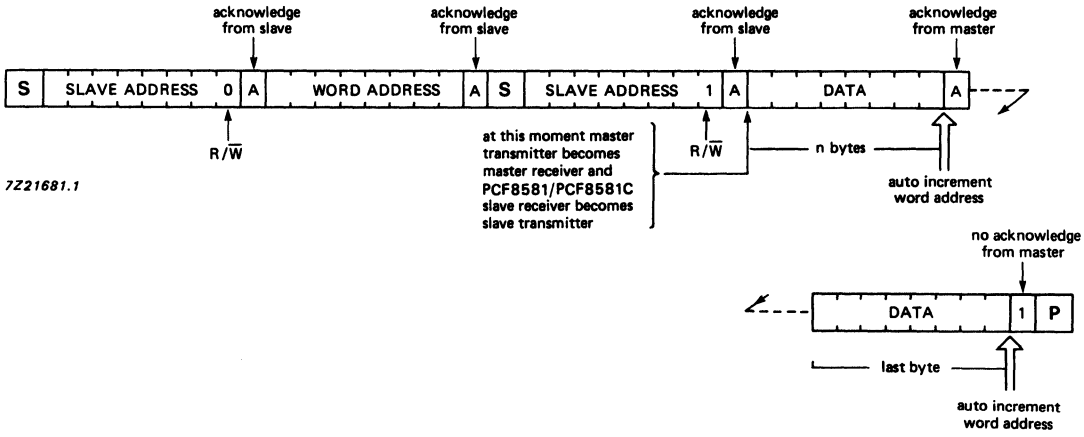


Fig. 10 Master reads after setting word address (WRITE word address; READ data).

DEVELOPMENT DATA

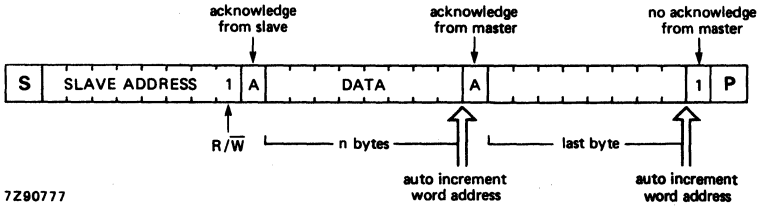


Fig. 11 Master reads slave immediately after first byte (READ mode).

An unlimited number of data bytes can be read in one operation. The address is automatically incremented. If a read without setting the word address is performed after a write operation, the address pointer may point at a byte in the row after the previously written row. This occurs if, during writing, the three lowest address bits (column) rolled over.

APPLICATION INFORMATION

The PCF8581 slave address has a fixed combination 1010 as group 1, while group 2 is fully programmable (see Fig. 12).

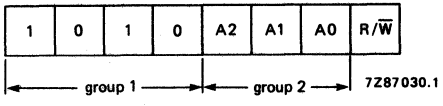


Fig. 12 PCF8581 address.

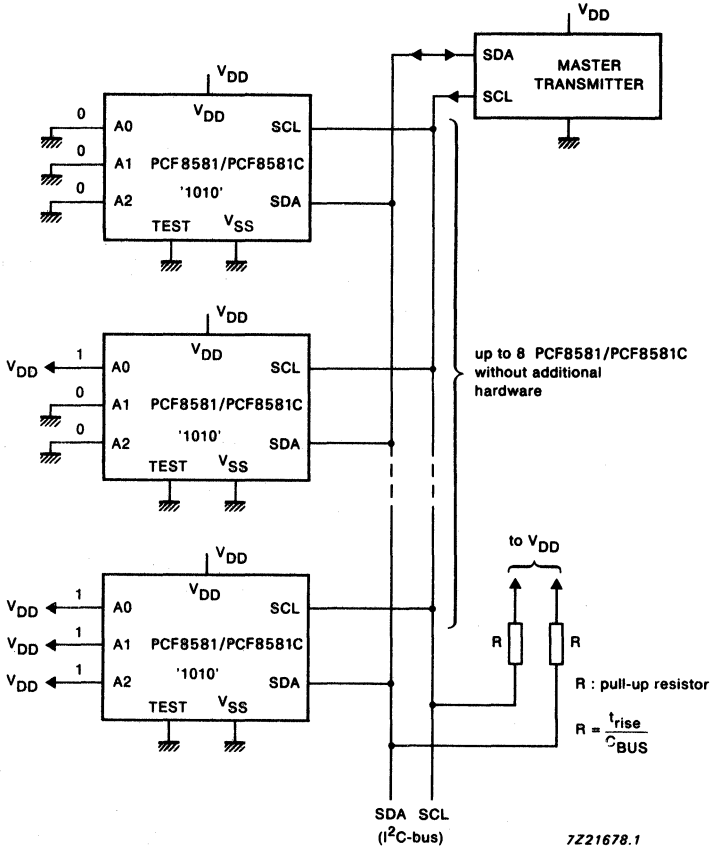


Fig. 13 Application diagram.

Note

A0, A1 and A2 inputs must be connected to V_{DD} or V_{SS} but not left open-circuit.

256 × 8-bit STATIC CMOS EEPROM WITH I²C-BUS INTERFACE

GENERAL DESCRIPTION

The PCF8582A is a 2 Kbits 5 Volt electrically erasable programmable read only memory (EEPROM) organized as 256 by 8-bits. It is designed in a floating gate CMOS technology.

As data bytes are received and transmitted via the serial I²C-bus, an eight pin DIL package is sufficient. Up to eight PCF8582A devices may be connected to the I²C-bus.

Chip select is accomplished by three address inputs.

Timing of the Erase/Write cycle can be done in two different ways; either by connecting an external clock to the "Programming Timing Control", pin (7 or 13), or by using an internal oscillator. If the latter is used an RC time constant must be connected to pin 7 or 13.

Features

- Non-volatile storage of 2 Kbits organized as 256 x 8
- Only one power supply required (5 V)
- On chip voltage multiplier for erase/write
- Serial input/output bus (I²C)
- Automatic word address incrementing
- Low power consumption
- One point erase/write timer
- Power on reset
- 10,000 erase/write cycles per byte
- 10 years non-volatile data retention
- Infinite number of read cycles
- Pin and address compatible to PCF8570, PCF8571, PCF8582 and PCD8572
- External clock signal possible.

PACKAGE OUTLINE

PCF8582AP; 8-lead dual in line; plastic (SOT97).
PCF8582AT; 16-lead mini-pack; plastic (SO16L; SOT162A).

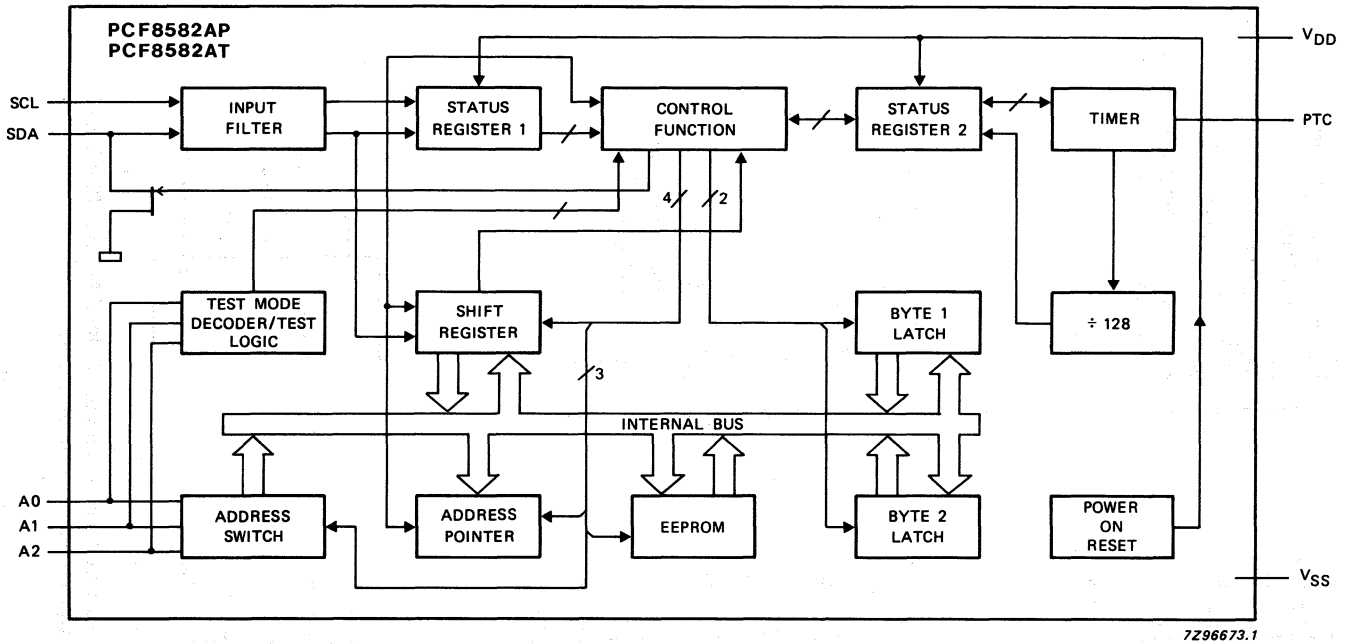
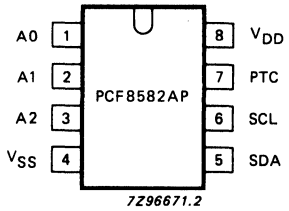
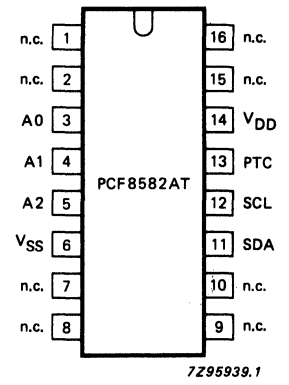


Fig. 1 Block diagram.



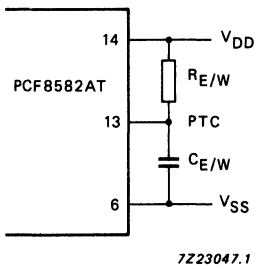
1	A0	address inputs/test mode select
2	A1	
3	A2	
4	V_{SS}	ground
5	SDA	I^2C-bus lines
6	SCL	
7	PTC	programming time control
8	V_{DD}	positive supply

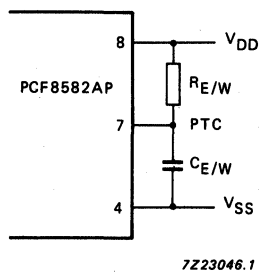
Fig. 2 (a) Pinning diagram.



1	n.c.	
2	n.c.	
3	A0	address inputs/test mode select
4	A1	
5	A2	
6	V_{SS}	ground
7	n.c.	
8	n.c.	
9	n.c.	
10	n.c.	
11	SDA	I^2C-bus lines
12	SCL	
13	PTC	programming time control
14	V_{DD}	positive supply
15	n.c.	
16	n.c.	

Fig. 2 (b) Pinning diagram.





Figs. 3 (a) and (b) RC circuit connections to PCF8582AP and PCF8582AT when using the internal oscillator

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

Characteristics of the I²C-bus

The I²C-bus is intended for communication between different ICs. The serial bus consists of two bi-directional lines, one for data signals (SDA), and one for clock signals (SCL). Both the SDA and the SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:

Data transfer may be initiated only when the bus is not busy.
During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

The following bus conditions have been defined:

Bus not busy; both data and clock lines remain HIGH.
Start data transfer; a change in the state of the data line, from HIGH to LOW, while the clock is HIGH defines the start condition. Stop data transfer; a change in the state of the data line, from LOW to HIGH, while the clock is HIGH, defines the stop condition.
Data valid; the state of the data line represents valid data when, after a start condition, the data line is stable for the duration of the HIGH period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition; the number of the data bytes, transferred between the start and stop conditions is limited to two bytes in the ERASE/WRITE mode and unlimited in the READ mode. The information is transmitted in bytes and each receiver acknowledges with a ninth bit.

Within the I²C-bus specifications a low speed mode (2 kHz clock rate) and a high speed mode (100 kHz clock rate) are defined. The PCF8582A operates in both modes.

By definition a device that sends a signal is called a "transmitter", and the device which receives the signal is called a "receiver". The device which controls the signal is called the "master". The devices that are controlled by the master are called "slaves".

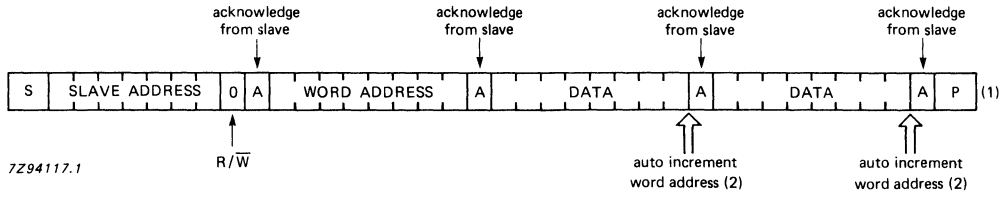
Each word of eight bits is followed by one acknowledge bit. This acknowledge bit is a HIGH level put on the bus by the transmitter. The master generates an extra acknowledge related clock pulse.
The slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte.
The master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.
The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge clock pulse in clock pulse.
Set-up and hold times must be taken into account. A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this condition the transmitter must leave the data line HIGH to enable the master generation of the stop condition.

Note

Detailed specifications of the I²C-bus are available on request.

I²C-Bus Protocol

The I²C-bus configurations for different READ and WRITE cycles of the PCF8582A are shown in Fig. 4, (a), (b) and (c).



(1) After this stop condition the erase/write cycle starts and the bus is free for another transmission. The duration of the erase/write cycle is approximately 30 ms if only one byte is written and 60 ms if two bytes are written. During the erase/write cycle the slave receiver does not send an acknowledge bit if addressed via the I²C-bus.

(2) The second data byte is voluntary. It is not allowed to erase/write more than two types.

Fig. 4(a) Master transmitter transmits to PCF8582A slave receiver (ERASE/WRITE mode).

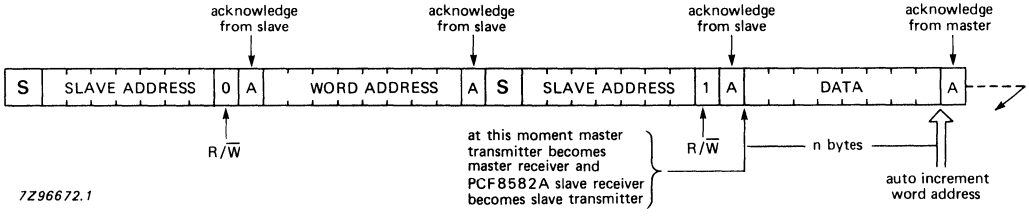
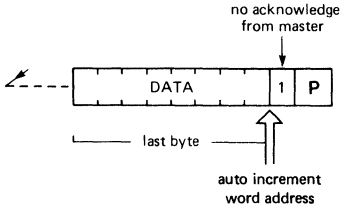


Fig. 4(b) Master reads PCF8582A slave after setting word address (write word address; READ data).



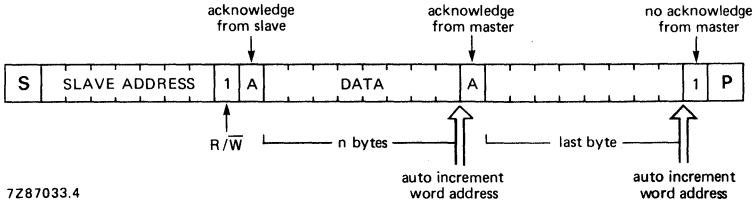


Fig. 4(c) Master reads PCF8582A slave immediately after first byte (READ mode).*

Note: the slave address is defined in accordance with the I²C-bus specification as:

1	0	1	0	A2	A1	A0	R/W

* The device can be used as read only without the programming clock.

I²C-bus timing

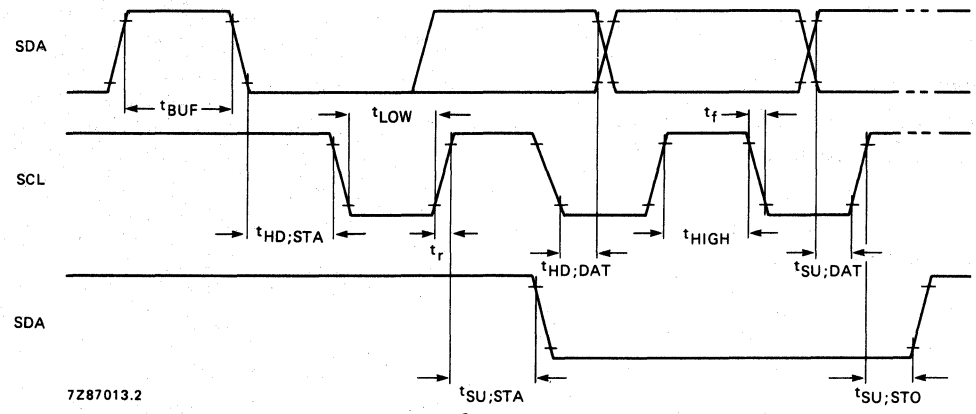
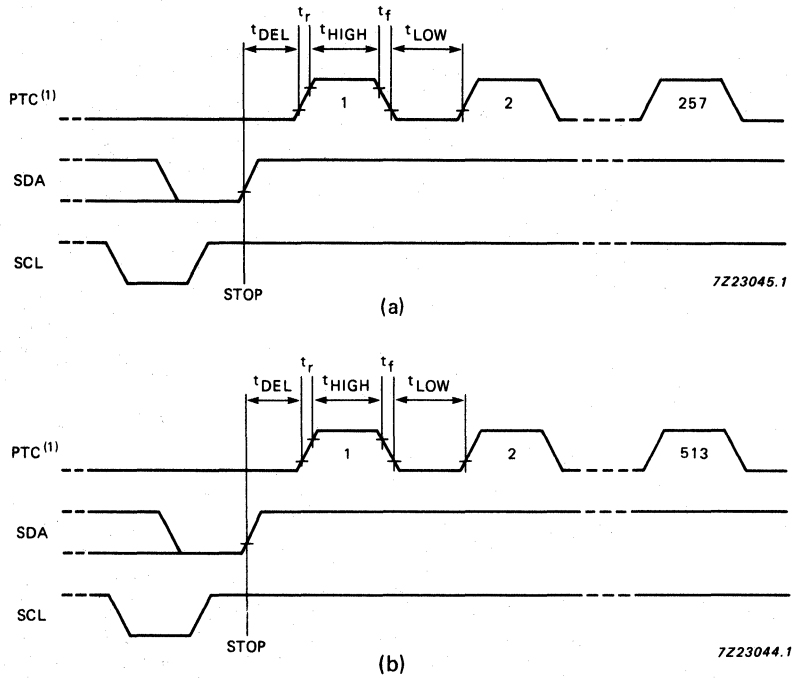


Fig. 5 I²C-bus timing.



(1) If external clock for PTC is chosen, this information is latched internally by leaving pin 7 LOW after transmission of the eight bit of the word address (negative edge of SCL). The state of PTC then, may be previously undefined.

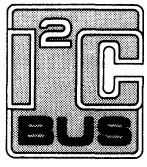
Fig. 6 (a) One-byte ERASE/WRITE cycle; (b) two-byte ERASE/WRITE cycle.

Ratings

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	V_{DD}	−0.3	+7	V
Voltage on any input pin input impedance 500 Ω	V_I	$V_{SS} - 0.8$	$V_{DD} + 0.8$	V
Operating temperature range	T_{amb}	−40	+85	°C
Storage temperature range	T_{stg}	−65	+150	°C
Current into any input pin	$\|I_I\|$	–	1	mA
Output current	$\|I_O\|$	–	10	mA

DEVELOPMENT DATA



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

CHARACTERISTICS

V_{DD} = 5 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Operating supply voltage		V_{DD}	4.5	5.0	5.5	V
Operating supply current READ	V_{DD} max. f_{SCL} = 100 kHz	I_{DD}	–	–	0.4	mA
Operating supply current WRITE/ERASE	V_{DD} max.	I_{DDW}	–	–	2.0	mA
Standby supply current	V_{DD} max.	I_{DDO}	–	–	10	μA
Input PTC						
Input voltage HIGH			V_{DD} − 0.3	–	–	V
Input voltage LOW			–	–	V_{SS} + 0.3	V
Input SCL and input/output SDA						
Input voltage LOW		V_{IL}	−0.3	–	1.5	V
Input voltage HIGH		V_{IH}	3.0	–	V_{DD} + 0.8	V
Output voltage LOW	I_{OL} = 3 mA V_{DD} = 4.5 V	V_{OL}	–	–	0.4	V
Output leakage current HIGH	$V_{OH} = V_{DD}$	I_{LO}	–	–	1	μA
Input leakage current (SCL)	$V_I = V_{DD}$ or V_{SS}	I_{LI}	–	–	1	μA
Clock frequency		f_{SCL}	0	–	100	kHz
Input capacitance (SCL; SDA)		C_I	–	–	7	pF
Time the bus must be free before new transmission can start		t_{BUF}	4.7	–	–	μs
Start condition hold time after which first clock pulse is generated		$T_{HD;STA}$	4	–	–	μs

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
The LOW period of the clock		t_{LOW}	4.7	–	–	μs
The HIGH period of the clock		t_{HIGH}	4.0	–	–	μs
Set-up time for start condition	repeated start only	$t_{SU;STA}$	4.7	–	–	μs
Data hold time for I²C-bus compatible masters		$t_{HD;DAT}$	5.0	–	–	μs
Data hold time for I²C devices	note 1	$t_{HD;DAT}$	0	–	–	ns
Date set up time		$t_{SU;DAT}$	250	–	–	ns
Rise time for SDA and SCL lines		t_r	–	–	1	μs
Fall time for SDA and SCL lines		t_f	–	–	300	ns
Set-up time for stop condition		$T_{SU;STO}$	4.7	–	–	μs
Programming time control						
Erase/write cycle time		$t_{E/W}$	5	–	40	ms
Capacitor used for E/W cycle of 30 ms	max. tolerance ±10%; using internal oscillator (Fig. 3)	$C_{E/W}$	–	3.3	–	nF
Resistor used for E/W cycle of 30 ms	max. tolerance ±5%; using internal oscillator (Fig. 3)	$R_{E/W}$	–	56.0	–	kΩ
Programming frequency using external clock						
Frequency		f_p	10	–	50	kHz
Period LOW		t_{LOW}	10.0	–	–	μs
Period HIGH		t_{HIGH}	10.0	–	–	μs
Rise-time		t_r	–	–	300	ns
Fall-time		t_f	–	–	300	ns
Delay-time		t_d	0	–		ns
Data retention time	T_{amb} = 55 °C	t_S	10	–	–	years

Note to the characteristics

1. The hold time required to bridge the undefined region of the falling edge of SCL must be internally provided by a transmitter. It is not greater than 300 ns.

CHARACTERISTICS (continued)

E/W programming time control

A. Using external resistor $R_{E/W}$ and capacitor $C_{E/W}$ (see Table 1)

Table 1 Recommended R, C combinations

$R_{E/W}$ (kΩ) note 1	$C_{E/W}$ (nF) note 2	$t_{E/W}$ (typ.) (ms) note 3
56	3.3	34
56	2.2	21
22	3.3	13
22	2.2	7.5 (note 4)

Notes to Table 1

1. Maximum tolerance is 10%.
2. Maximum tolerance is 5%.
3. Actual E/W lines are mainly influenced by the tolerances in values of R and C.
4. Minimum allowed $t_{E/W}$ is 5 ms (see CHARACTERISTICS).

B. Using an external clock (see Table 2 and Fig.6)

Table 2 E/W programming time control using an external clock

parameters	symbol	min.	max.	unit
frequency	f_p	10.0	50.0	kHz
period LOW	t_{LOW}	10.0	–	s
period HIGH	t_{HIGH}	10.0	–	s
rise time	t_r	–	300	ns
fall time	t_f	–	300	ns
delay time	t_d	0	–	ns

256 x 8-BIT STATIC CMOS EEPROM WITH I²C-BUS INTERFACE FOR AUTOMOTIVE APPLICATIONS

GENERAL DESCRIPTION

The PCF8582C is a 2 Kbit (256 x 8-bit) floating gate electrically erasable programmable read only memory (EEPROM). By using an internal redundant storage code it is fault tolerant to single bit errors. This feature dramatically increases reliability compared to conventional EEPROM memories.

Power consumption is low due to the full CMOS technology used. The programming voltage is generated on chip using a voltage multiplier.

As data bytes are received and transmitted via the serial I²C-bus, a package using eight pins is sufficient. Up to eight PCF8582C devices may be connected to the I²C-bus.

Chip select is accomplished by the three address inputs, which may also be used to choose between eleven test modes which simplify circuit testing.

Timing of the Erase/Write cycle is done internally so no external components are needed. Pin 7 must be connected to either V_{DD} or left open.

There is an option (described in PCF8582A and PCA8582B data sheets) of using an external clock for timing the length of an Erase/Write cycle.

Features

- Non-volatile storage of 2 Kbits organized as 256 x 8 bits
- High reliability by using a redundant storage code (single bit error correction)
- Only one power supply required
- On chip voltage multiplier
- Serial input/output bus (I²C)
- Automatic word address incrementing
- Low power consumption
- Extended supply voltage range (2.5 to 6 V)
- Internal timer for writing (no external components)
- Power on reset
- 500 000 erase/write cycles per byte with low failure rate
- 10 years non-volatile data retention time
- Infinite number of read cycles
- Pin and address compatible to PCF8570, PCF8571, PCD8572 and PCF8582A

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage range	V_{DD}	2.5	–	6	V
Operating supply current READ	I_{DD}	0.25	–	1.6	mA
Operating supply current WRITE/ERASE	I_{DD}	0.35	–	2.5	mA
Standby supply current	I_{DDO}	3.5	–	10	μA

PACKAGE OUTLINES

PCF8582P: 8-lead DIL; plastic (SOT97).
PCF8582T: 16-lead mini-pack; plastic (SO16L; SOT162A).

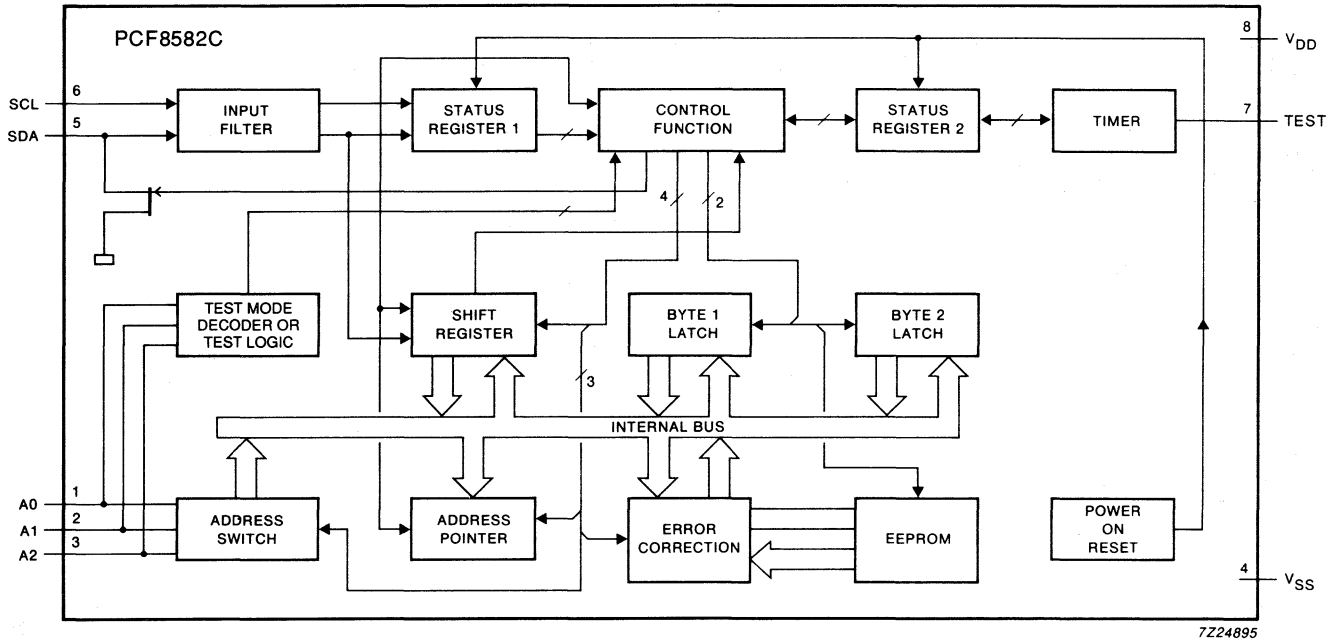
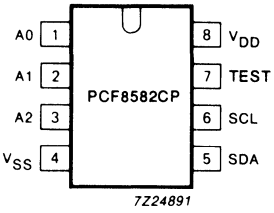


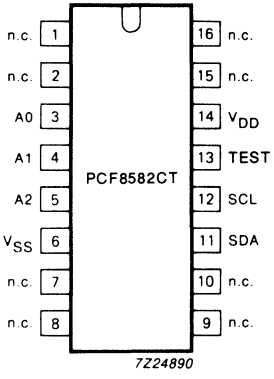
Fig.1 Block diagram for PCF8582CP.

PINNING



1	A0	address inputs or test mode select
2	A1	
3	A2	
4	V_{SS}	ground
5	SDA	I²C-bus lines
6	SCL	
7	TEST	can be connected to V_{DD} or left open
8	V_{DD}	positive supply voltage

Fig.2(a) Pinning diagram; PCF8582CP.



1	n.c.	not connected
2	n.c.	
3	A0	address inputs or test mode select
4	A1	
5	A2	
6	V_{SS}	ground
7	n.c.	not connected
8	n.c.	
9	n.c.	
10	n.c.	
11	SDA	I²C-bus lines
12	SCL	
13	TEST	can be connected to V_{DD} or left open
14	V_{DD}	positive supply voltage
15	n.c.	not connected
16	n.c.	

Fig.2(b) Pinning diagram; PCF8582CT.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

Characteristics of the I²C-bus

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The serial bus consists of two bidirectional lines: one for data signals (SDA), and one for clock signals (SCL). Both the SDA and the SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

The following bus conditions have been defined:

Bus not busy: both data and clock lines remain HIGH.
Start data transfer: a change in the state of the data line, from HIGH-to-LOW, while the clock is HIGH defines the start condition.
Stop data transfer: a change in the state of the data line, from LOW-to-HIGH, while the clock is HIGH, defines the stop condition.
Data valid: the state of the data line represents valid data when, after a start condition, the data line is stable for the duration of the HIGH period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition; the number of the data bytes, transferred between the start and stop conditions is limited to two bytes in the ERASE/WRITE mode and unlimited in the READ mode. The information is transmitted in bytes and each receiver acknowledges with a ninth bit.

Within the I²C-bus specifications a low speed mode (2 kHz clock rate) and a high speed mode (100 kHz clock rate) are defined. The PCF8582C operates in both modes.

By definition a device that sends a signal is called a "transmitter", and the device which receives the signal is called a "receiver". The device which controls the signal is called the "master". The devices that are controlled by the master are called "slaves".

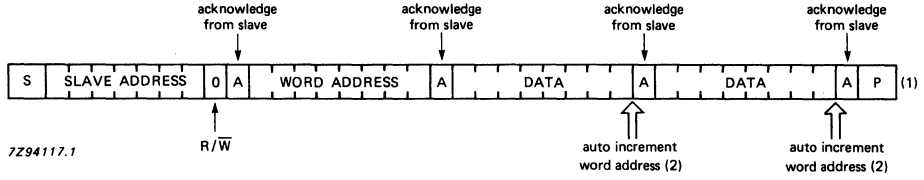
Each byte of eight bits is followed by one acknowledge bit. This acknowledge bit is a HIGH level put on the bus by the transmitter. The master generates an extra acknowledge related clock pulse.
The slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte.
The master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.
The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse.
Set-up and hold times must be taken into account. A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master generation of the stop condition.

Note

Detailed specifications of the I²C-bus are available on request.

I²C-bus Protocol

The I²C-bus configurations for different READ and WRITE cycles of the PCF8582C are shown in Fig.3 (a), (b) and (c).



(1) After this stop condition the erase/write cycle starts and the bus is free for another transmission. Its duration is 30 ms if only one byte is written and 60 ms if two bytes are written. During the erase/write cycle the slave receiver does not send an acknowledge bit if addressed via the I²C-bus.
(2) The second data byte is voluntary. It is not allowed to erase/write more than two bytes.

Fig.3(a) Master transmitter transmits to PCF8582C slave receiver (ERASE/WRITE mode).

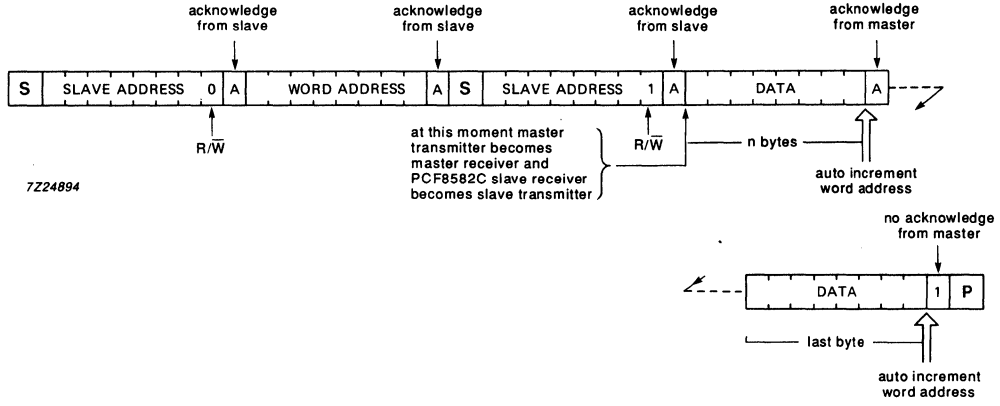


Fig.3(b) Master reads PCF8582C slave after setting word address (WRITE word address; READ data).

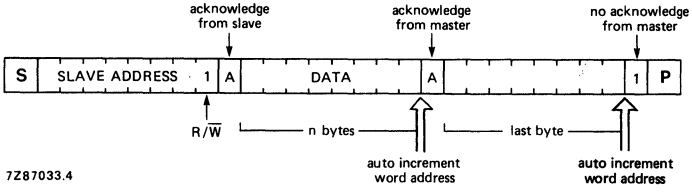


Fig.3(c) Master reads PCF8582C slave immediately after first byte (READ mode).

FUNCTIONAL DESCRIPTION (continued)

Chip address (slave address) allocation

Three chip address inputs (A0, A1, A2) can produce eight different chip addresses. This means that up to eight different PCF8582C devices may be connected to the I^2C-bus. Address allocation is illustrated by Fig.4.

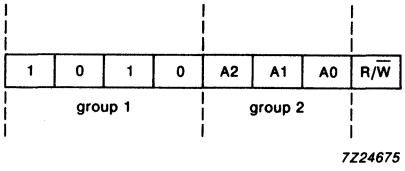


Fig.4 Slave address.

DEVELOPMENT DATA

I²C-bus timing

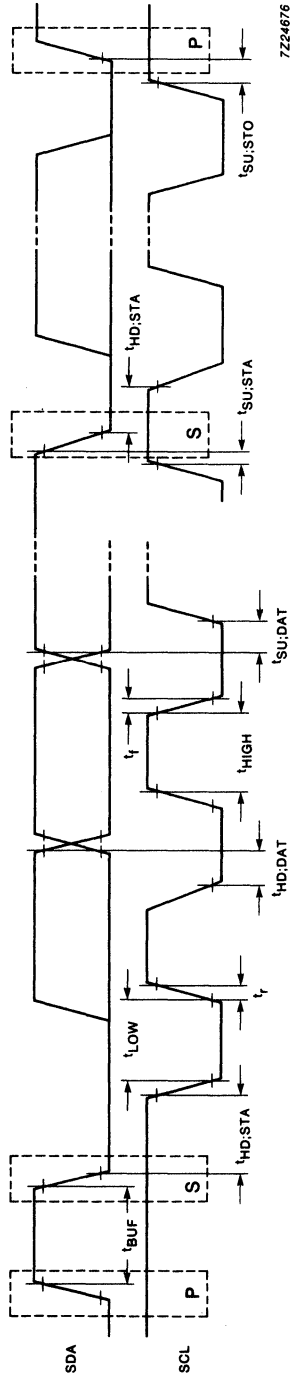


Fig.5 I²C-bus timing.

FUNCTIONAL DESCRIPTION (continued)

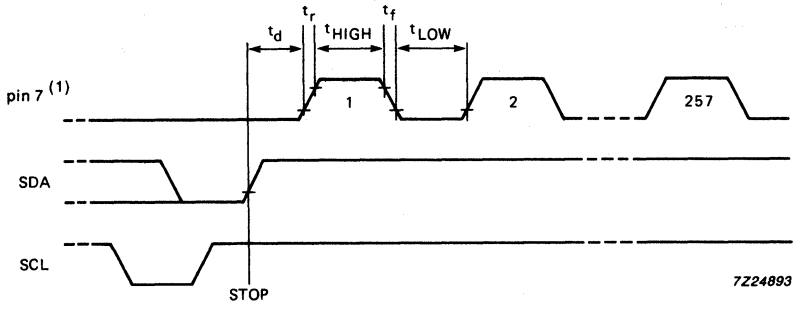


Fig.6(a) One byte ERASE/WRITE cycle.

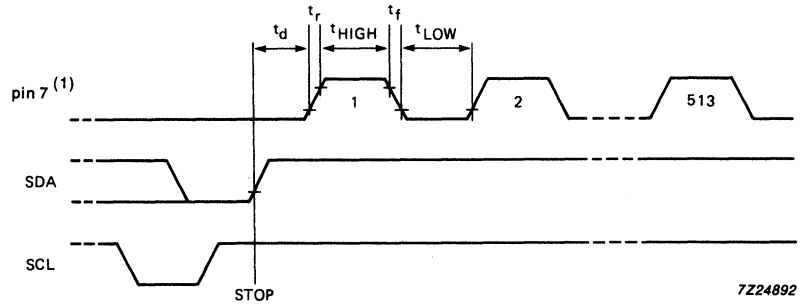


Fig.6(b) Two byte ERASE/WRITE cycles.

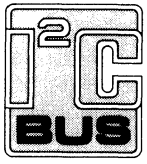
(1) If an external clock is chosen, this information is latched internally by leaving pin 7 (Test) LOW after transmission of the eighth bit of the word address (negative edge of SCL). The state of pin 7 then, may be previously undefined.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	V_{DD}	−0.3	+ 7	V
Voltage on any input pin input impedance > 500 Ω	V_I	V_{SS} − 0.8	V_{DD} + 0.8	V
Operating ambient temperature range	T_{amb}	−40	+ 85	°C
Storage temperature range	T_{stg}	−65	+ 150	°C
Current into any input pin	$\|I_I\|$	−	1	mA
Output current	$\|I_O\|$	−	10	mA

DEVELOPMENT DATA



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

CHARACTERISTICS

V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Operating supply voltage		V_{DD}	2.5	–	6	V
Operating supply current READ	V_{DD} = 3 V; f_{SCL} = 100 kHz	I_{DDR}	–	–	0.25	mA
	V_{DD} = 6 V; f_{SCL} = 100 kHz	I_{DDR}	–	–	1.6	mA
Operating supply current WRITE/ERASE	V_{DD} = 3 V; f_{SCL} = 100 kHz	I_{DDW}	–	–	0.35	mA
	V_{DD} = 6 V; f_{SCL} = 100 kHz	I_{DDW}	–	–	2.5	mA
Standby supply current	V_{DD} = 3 V; f_{SCL} = 100 kHz	I_{DDO}	–	–	3.5	μA
	V_{DD} = 6 V; f_{SCL} = 100 kHz	I_{DDO}	–	–	10	μA
Input Test						
Input voltage HIGH		V_{IH}	$0.9V_{DD}$	–	V_{DD} + 0.8	V
Input voltage LOW		V_{IL}	−0.8	–	$0.1V_{DD}$	V
Input SCL and input/output SDA						
Input voltage HIGH		V_{IH}	$0.7V_{DD}$	–	V_{DD} + 0.8	V
Input voltage LOW		V_{IL}	−0.8	–	$0.3V_{DD}$	V
Output voltage LOW	I_{OH} = 3 mA; V_{DD} = 2.5 V	V_{OL}	–	–	0.4	V
Output leakage current HIGH	$V_{OH} = V_{DD}$	I_{LO}	–	–	10	μA
Input leakage current (SCL)	$V_I = V_{DD}$ or V_{SS}	$\pm I_{LI}$	–	–	10	μA
Clock frequency		f_{SCL}	0	–	100	kHz
Input capacitance (SCL; SDA)	$V_I = V_{SS}$	C_I	–	–	7	pF

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Time the bus must be free before a new transmission can start		t_{BUF}	4.7	–	–	μs
Start condition hold time. After this period the first clock pulse is generated		$T_{HD;STA}$	4	–	–	μs
The LOW period of the clock		t_{LOW}	4.5	–	–	μs
The HIGH period of the clock		t_{HIGH}	4	–	–	μs
Set-up time for start condition	repeated start	$t_{SU;STA}$	4.7	–	–	μs
Data hold time for I²C-bus compatible masters		$t_{HD;DAT}$	5	–	–	μs
Data hold time for I²C devices	note 1	$t_{HD;DAT}$	0	–	–	ns
Data set-up time		$t_{SU;DAT}$	250	–	–	ns
Rise time for SDA and SCL lines		t_r	–	–	1	μs
Fall time for SDA and SCL lines		t_f	–	–	300	ns
Set-up time for stop condition		$t_{SU;STO}$	4.7	–	–	μs
Erase/write cycle time		$t_{E/W}$	5	–	25	ms
Endurance (E/W cycles per byte)	T_{amb} = 85 °C; $t_{E/W}$ = 5–25 ms			100 000		cycles
	T_{amb} = 33 °C; $t_{E/W}$ = 10 ms			500 000		cycles
Data retention time	T_{amb} = 55 °C	t_S	10	–	–	years

Note to the characteristics

1. An internal transmitter must provide a hold time (max. 300 ns) to bridge the undefined region of the falling edge of SCL.

E/W programming time control

A. Using an internal oscillator

Using an internal oscillator $t_{E/W}$ has a minimum value of 5 ms and a maximum value of 25 ms; the typical value is 10 ms.

B. Using an external clock (see Table 1 and Fig.6)

Table 1 E/W programming time control using an external clock

parameter	symbol	min.	max.	unit
frequency	f_p	10	50	kHz
period LOW	t_{LOW}	5	–	μs
period HIGH	t_{HIGH}	5	–	μs
rise time	t_r	–	300	ns
fall time	t_f	–	300	ns
delay time	t_d	0	t_{LOW}	μs

64K-bit CMOS EPROM

		page
27C64A-IND	64K-bit CMOS EPROMs (8K x 8) 150 ns; 200 ns	185
27C64A O.T.P.	64K-bit CMOS EPROM (8K x 8) 100 ns	189
27C64A O.T.P.	64K-bit CMOS EPROMs (8K x 8) 120 ns; 150 ns	193
27C64A O.T.P.	64K-bit CMOS EPROM (8K x 8) 200 ns	197
27C64A U.V.	64K-bit erasable CMOS EPROM (8K x 8) 100 ns	201
27C64A U.V.	64K-bit erasable CMOS EPROMs (8K x 8) 120 ns; 150 ns	205
27C64A U.V.	64K-bit erasable CMOS EPROM (8K x 8) 200 ns	209
27HC641 O.T.P.	64K-bit CMOS EPROMs (8K x 8) 45 ns; 55 ns	213
27HC641 U.V.	64K-bit erasable CMOS EPROMs (8K x 8) 35 ns; 45 ns; 55 ns	217

27C64A-IND

Industrial Temperature Range 64K-Bit CMOS EPROMs (8K × 8)

Product Specification

Application Specific Products

DESCRIPTION

Signetics 27C64A CMOS EPROM is a 64K-bit 5V only memory organized as 5,536 words of 8 bits each. It employs advanced CMOS circuitry for systems requiring low power, high-performance speeds, and immunity to noise. The 27C64A has a non-multiplexed addressing interface and is plug-compatible with the industry standard 27C64.

The 27C64A is specified to operate over the INDUSTRIAL TEMPERATURE RANGE of −40°C to +85°C with no degradation in performance.

The 27C64A is available in both the windowed ceramic DIP, the plastic DIP and the PLCC packages. This device can be programmed with standard EPROM programmers.

FEATURES

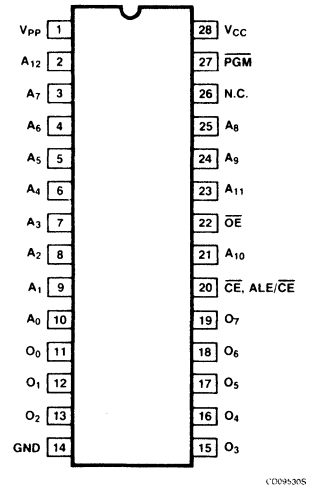
- **Quick pulse programming algorithm for high speed production programming (3 second typical programming time)**
- **High-performance speeds**
  - **27C64AI15: 150ns maximum access time**
  - **27C64AI20: 200ns maximum access time**
- **Noise immunity features**
  - **± 10% V_{CC} tolerance**
  - **Maximum latch-up immunity through epitaxial processing**

PIN DESCRIPTION

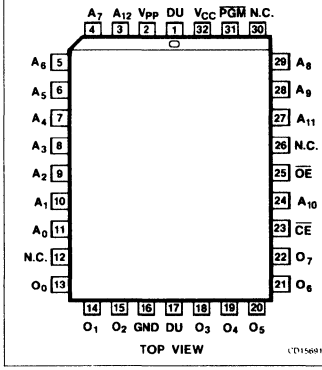
$A_0 - A_{12}$	Addresses
$O_0 - O_7$	Outputs
$\overline{OE}$	Output Enable
$\overline{CE}$	Chip Enable
GND	Ground
V_{PP}	Program voltage
V_{CC}	Power supply
D.U.	Don't Use
$\overline{PGM}$	Program strobe
N.C.	No Connection

PIN CONFIGURATIONS

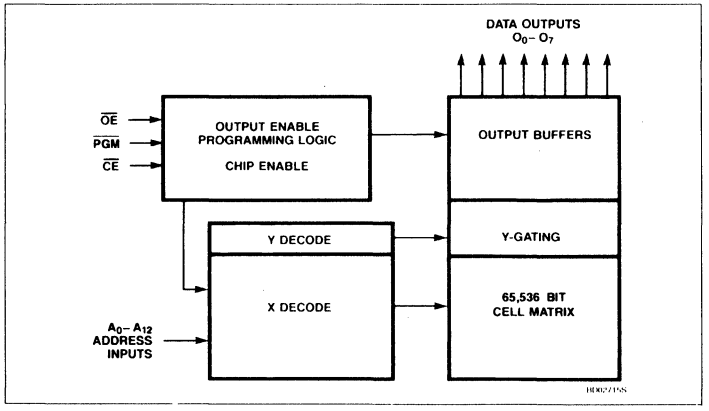
FA and N Packages



A Package



BLOCK DIAGRAM



READ MODE: 27C64A

The 27C64A has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins. Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been Low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

STANDBY MODE

The 27C64A has a standby mode which reduces the maximum V_{CC} current to 100μA. It is placed in the Standby mode when $\overline{CE}$ is in the High state. When in the Standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
28-pin CERDIP with quartz window (600mil-wide)	27C64AI15 FA 27C64AI20 FA
28-pin Plastic Dual in-line (600mil-wide)	27C64AI15 N 27C64AI20 N
32-pin Plastic Leaded Chip Carrier (450 × 550mil)	27C64AI15 A 27C64AI20 A

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
T_A	Temperature under bias	−55 to +125	°C
T_{STG}	Storage temperature range	−65 to +150	°C
V_I, V_O	Voltage inputs and outputs	−2.0 to (V_{CC} + 1)	V
V_H	Voltage on A_9[2] (During intelligent identifier interrogation)	−2.0 to +13.5	V
V_{PP}	Voltage on V_{PP}[2] (During programming)	−2.0 to +14.0	V
V_{CC}	Supply voltage[2]	−2.0 to +7.0	V

NOTE:

1. Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DEVICE OPERATION[2]

MODE	$\overline{CE}$	$\overline{OE}$[10]	$\overline{PGM}$[10]	V_{PP}[8]	OUTPUTS
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	D_{OUT}
Output disable	V_{IL}	V_{IH}	V_{IH}	V_{CC}	Hi-Z
Standby	V_{IH}	X	X	V_{CC}	Hi-Z

Notes on following page.

DC ELECTRICAL CHARACTERISTICS $-40°C \leq T_A \leq +85°C$, $+4.5V \leq V_{CC} \leq +5.5V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[3]	Max	
Input current						
I_{IH}	Leakage	$V_{IN} = 5.5V = V_{CC}$		0.01	1.0	µA
I_{IL}	Low	$V_{IL} = 0.45V$		0.01	1.0	µA
I_{PP}	V_{PP} read	$V_{PP} = V_{CC}$			100	µA
Output current						
I_{LO}	Leakage	$\overline{OE}$ or $\overline{CE} = V_{IH}$ $V_{OUT} = 5.5V = V_{CC}$			1.0	µA
		$V_{OUT} = 0V = GND$			1.0	µA
I_{OS}	Short circuit[7, 9]	$V_{OUT} = 0V$			100	mA
Supply current						
I_{CC} TTL	Operating (TTL inputs)[4]	$\overline{CE} = \overline{OE} = V_{IL}$, f = 6.7MHz $V_{PP} = V_{CC}$ $O_{0-7} = 0mA$			20	mA
I_{SB} TTL	Standby (TTL inputs)[4]	$\overline{CE} = V_{IH}$			1.0	mA
I_{SB} CMOS	Standby (CMOS inputs)[5, 6]	$\overline{CE} = V_{IH}$			100	µA
Input voltage[2]						
V_{IL}	Low (TTL)	$V_{PP} = V_{CC}$	−0.5		0.8	V
V_{IL}	Low (CMOS)	$V_{PP} = V_{CC}$	−0.2		0.2	V
V_{IH}	High (TTL)	$V_{PP} = V_{CC}$	2.0		$V_{CC} + 0.5$	V
V_{IH}	High (CMOS)	$V_{PP} = V_{CC}$	$V_{CC} - 0.2$		$V_{CC} + 0.2$	V
V_{PP}	Read[8]	(Operating)	$V_{CC} - 0.7$		V_{CC}	V
Output voltage[2]						
V_{OL}	Low	$I_{OL} = 2.1mA$			0.45	V
V_{OH}	High	$I_{OH} = -2.5mA$	3.5			V
Capacitance[9] $T_A = 25°C$						
C_{IN}	Address and control	$V_{CC} = 5.0V$ f = 1.0MHz $V_{IN} = 0V$ $V_{OUT} = 0V$			6	pF
C_{OUT}	Outputs				12	pF

NOTES:

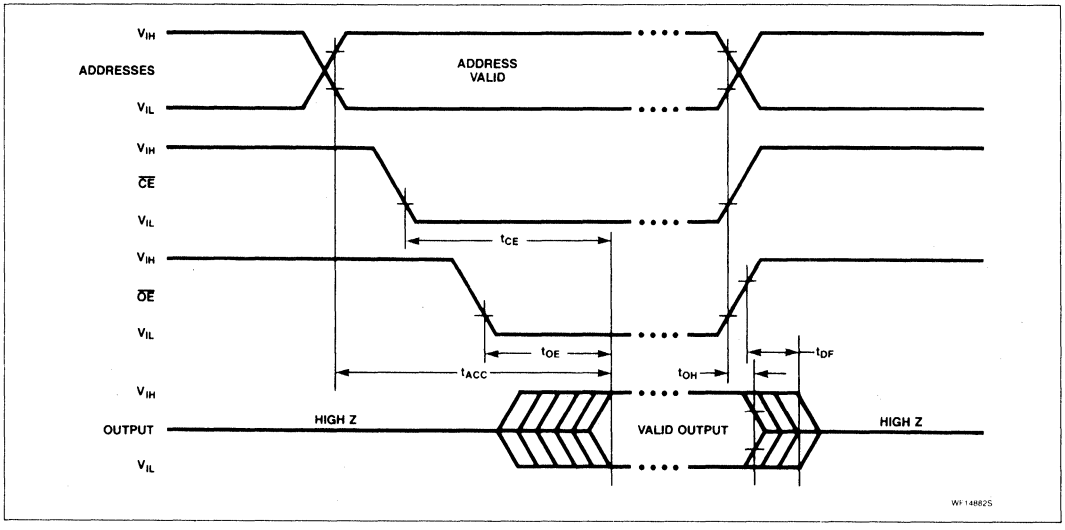
1. Minimum DC input voltage is −0.5V. During transitions the inputs may undershoot to −2.0V for periods less than 20ns.
2. All voltages are with respect to network ground.
3. Typical limits are at $V_{CC} = 5V$, $T_A = 25°C$.
4. TTL inputs: Spec V_{IL}, V_{IH} levels.
   CMOS inputs: GND ± 0.2V to V_{CC} + 0.2V.
5. $\overline{CE}$ is V_{CC} ± 0.2V. All other inputs can have any value within spec.
6. Maximum active power usage is the sum of $I_{PP} + I_{CC}$ and is measured at a frequency of 5MHz.
7. Test one output at a time, duration should not exceed 1 second.
8. V_{PP} may be one diode voltage drop below V_{CC}, and can be connected directly to V_{CC}.
9. Guaranteed by design, not 100% tested.
10. X can be V_{IH} or V_{IL}.

AC ELECTRICAL CHARACTERISTICS $-40°C \leq T_A \leq +85°C$, $+4.5V \leq V_{CC} \leq +5.5V$, $R_L = 660\Omega$, $C_L = 100pF$

SYMBOL	TO	FROM	27C64AI15		27C64AI20		UNIT
			Min	Max	Min	Max	
Access time[1]							
t_{ACC}	Output	Address		150		200	ns
t_{CE}	Output	$\overline{CE}$		150		200	ns
t_{OE}[3]	Output	$\overline{OE}$		65		75	ns
Disable time[2]							
t_{DF}[4]	Output Hi-Z	$\overline{OE}$ or $\overline{CE}$		45		55	ns
t_{OH}	Output hold	Address, $\overline{CE}$ or $\overline{OE}$	0		0		ns

NOTES:
1. AC characteristics are tested at $V_{IH} = 2.4V$ and $V_{IL} = 0.45V$. Timing measurements made at $V_{OL} = 0.8V$ and $V_{OH} = 2.0V$.
2. Guaranteed by design, not 100% tested.
3. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.
4. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

AC VOLTAGE WAVEFORMS



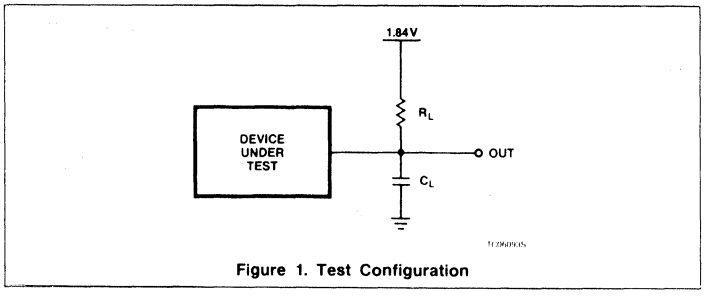


Figure 1. Test Configuration

27C64A O.T.P.
One Time Programmable 64K-Bit CMOS EPROM (8K × 8)

Product Specification

Application Specific Products

DESCRIPTION

Signetics' 27C64A CMOS O.T.P. EPROM is a 64K-bit 5V only memory organized as 8,192 words of 8 bits each. It employs advanced CMOS circuitry for systems requiring low power, high-performance speeds, and immunity to noise. The 27C64A has a non-multiplexed addressing interface and is plug-compatible with the industry standard 2764.

The 27C64A O.T.P. is offered in plastic DIP and plastic leaded chip carrier (PLCC) packages. Plastic EPROMs provide optimum cost effectiveness in production environments. Quick-pulse programming is employed on plastic devices which may speed up programming by as much as one hundred times. In the absence of quick-pulse programming equipment, the intelligent programming algorithm may be utilized.

FEATURES

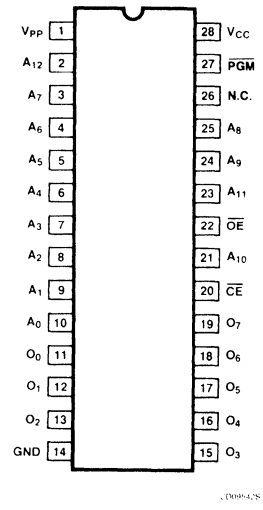
- **Low power consumption**
  - **100μA maximum CMOS standby current**
- **High-performance speeds**
  - **27C64A-10: 100ns maximum access time**
- **Noise immunity features**
  - **± 10% V_{CC} tolerance**
  - **Maximum latch-up immunity through Epitaxial processing**
- **Quick-pulse programming algorithm (3 second typical programming times)**

PIN DESCRIPTION

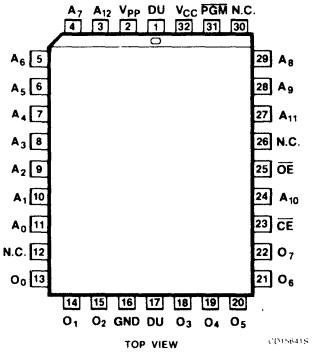
$A_0 - A_{12}$	Addresses
$O_0 - O_7$	Outputs
$\overline{OE}$	Output enable
$\overline{CE}$	Chip enable
N.C.	No connection
GND	Ground
V_{PP}	Program voltage
V_{CC}	Power supply
DU	Don't use
$\overline{PGM}$	Program strobe

PIN CONFIGURATIONS

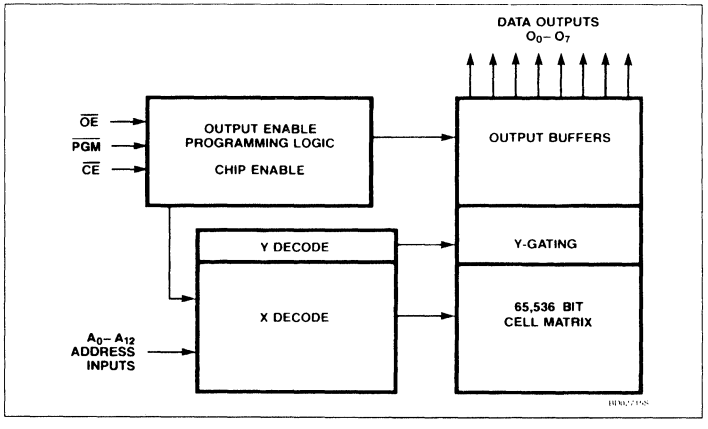
Dual In-Line (DIP) Package



PLCC Package



BLOCK DIAGRAM



One Time Programmable 64K-Bit CMOS EPROM (8K × 8)

READ MODE: 27C64A

The 27C64A has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins. Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

STANDBY MODE

The 27C64A has a standby mode which reduces the maximum V_{CC} current to 100μA. It is placed in the Standby mode when $\overline{CE}$ is in the High state. When in the Standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

ORDERING INFORMATION

PACKAGE DESCRIPTION	ORDER CODE
28-pin Plastic Dual in-line 600mil-wide	27C64A-10 N
32-pin Plastic Leaded Chip Carrier 450mil × 550mil	27C64A-10 A

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
T_A	Temperature under bias	−10 to +80	°C
T_{STG}	Storage temperature range	−65 to +125	°C
V_I, V_O	Voltage inputs and outputs	−2.0 to (V_{CC} + 1)	V
V_H	Voltage on A_9[2] (During intelligent identifier interrogation)	−2.0 to +13.5	V
V_{PP}	Voltage on V_{PP}[2] (During programming)	−2.0 to +14.0	V
V_{CC}	Supply voltage[2]	−2.0 to +7.0	V

NOTE:

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. All voltages are with respect to network ground.

DEVICE OPERATION[2]

MODE	$\overline{CE}$	$\overline{OE}$[10]	$\overline{PGM}$[10]	V_{PP}[8]	OUTPUTS
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	D_{OUT}
Output disable	V_{IL}	V_{IH}	V_{IH}	V_{CC}	Hi-Z
Standby	V_{IH}	X	X	V_{CC}	Hi-Z

Notes on following page.

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +70°C$, $+4.5V \leq V_{CC} \leq +5.5V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[3]	Max	
Input current						
I_{IH}	Leakage	$V_{IN} = 5.5V = V_{CC}$		0.01	1.0	μA
I_{IL}	Low	$V_{IL} = 0.45V$		0.01	1.0	μA
I_{PP}	V_{PP} read	$V_{PP} = V_{CC}$			100	μA
Output current						
I_{LO}	Leakage	$\overline{OE}$ or $\overline{CE} = V_{IH}$ $V_{OUT} = 5.5V = V_{CC}$			1.0	μA
		$V_{OUT} = 0V = GND$			1.0	μA
I_{OS}	Short circuit[7, 9]	$V_{OUT} = 0V$			100	mA
Supply current						
I_{CC} TTL	Operating (TTL inputs)[4]	$\overline{CE} = \overline{OE} = V_{IL}$, f = 10.0MHz $V_{PP} = V_{CC}$ $O_{0-7} = 0mA$			20	mA
I_{SB} TTL	Standby (TTL inputs)[4]	$\overline{CE} = V_{IH}$			1.0	mA
I_{SB} CMOS	Standby (CMOS inputs)[5, 6]	$\overline{CE} = V_{IH}$			100	μA
Input voltage[2]						
V_{IL}	Low (TTL)	$V_{PP} = V_{CC}$	−0.5		0.8	V
V_{IL}	Low (CMOS)	$V_{PP} = V_{CC}$	−0.2		0.2	V
V_{IH}	High (TTL)	$V_{PP} = V_{CC}$	2.0		$V_{CC} + 0.5$	V
V_{IH}	High (CMOS)	$V_{PP} = V_{CC}$	$V_{CC} - 0.2$		$V_{CC} + 0.2$	V
V_{PP}	Read[8]	(Operating)	$V_{CC} - 0.7$		V_{CC}	V
Output voltage[2]						
V_{OL}	Low	$I_{OL} = 2.1mA$			0.45	V
V_{OH}	High	$I_{OH} = -2.5mA$	3.5			V
Capacitance[9] $T_A = 25°C$						
C_{IN}	Address and control	$V_{CC} = 5.0V$ f = 1.0MHz			6	pF
C_{OUT}	Outputs	$V_{IN} = 0V$ $V_{OUT} = 0V$			12	pF

NOTES:
1. Minimum DC input voltage is −0.5V. During transitions the inputs may undershoot to −2.0V for periods less than 20ns.
2. All voltages are with respect to network ground.
3. Typical limits are at $V_{CC} = 5V$, $T_A = 25°C$.
4. TTL inputs: Spec V_{IL}, V_{IH} levels.
   CMOS inputs: GND ±0.2V to V_{CC} ±0.2V.
5. $\overline{CE}$ is V_{CC} ±0.2V. All other inputs can have any value within spec.
6. Maximum active power usage is the sum of $I_{PP} + I_{CC}$ and is measured at a frequency of 5MHz.
7. Test one output at a time, duration should not exceed 1 second.
8. V_{PP} may be one diode voltage drop below V_{CC}, and can be connected directly to V_{CC}.
9. Guaranteed by design, not 100% tested.
10. X can be V_{IH} or V_{IL}.

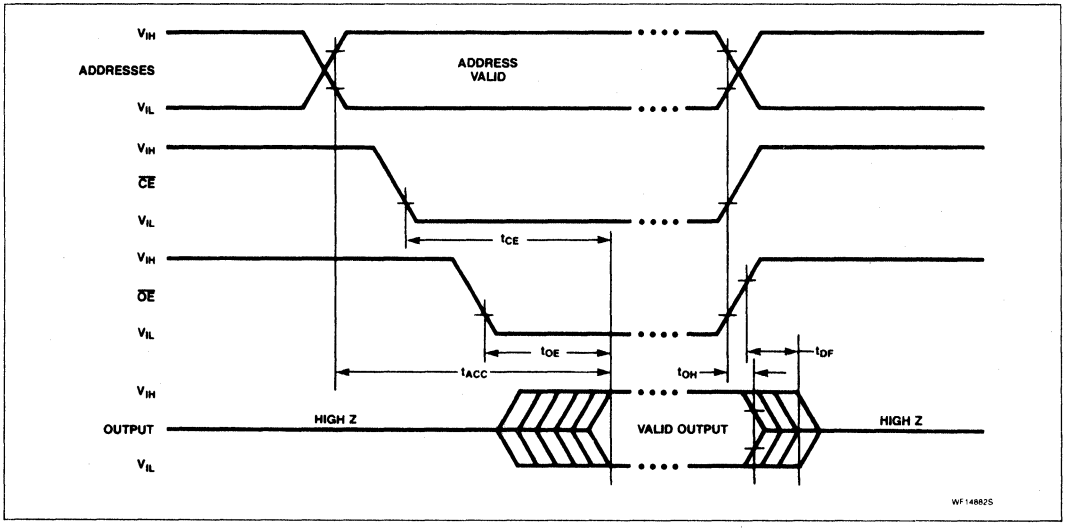
One Time Programmable 64K-Bit CMOS EPROM (8K × 8)

AC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +70°C$, $+4.5V \leq V_{CC} \leq +5.5V$, $R_L = 660\Omega$, $C_L = 100pF$

SYMBOL	TO	FROM	27C64A - 10		UNIT
			Min	Max	
Access time[1]					
t_{ACC}	Output	Address		100	ns
t_{CE}	Output	$\overline{CE}$		100	ns
t_{OE}[3]	Output	$\overline{OE}$		35	ns
Disable time[2]					
t_{DF}[4]	Output Hi-Z	$\overline{OE}$ or $\overline{CE}$		25	ns
t_{OH}	Output hold	Address, $\overline{CE}$ or $\overline{OE}$	0		ns

NOTES:
1. AC characteristics are tested at $V_{IH} = 2.4V$ and $V_{IL} = 0.45V$. Timing measurements made at $V_{OL} = 0.8V$ and $V_{OH} = 2.0V$.
2. Guaranteed by design, not 100% tested.
3. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.
4. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

AC VOLTAGE WAVEFORMS



AC TESTING LOAD CIRCUIT

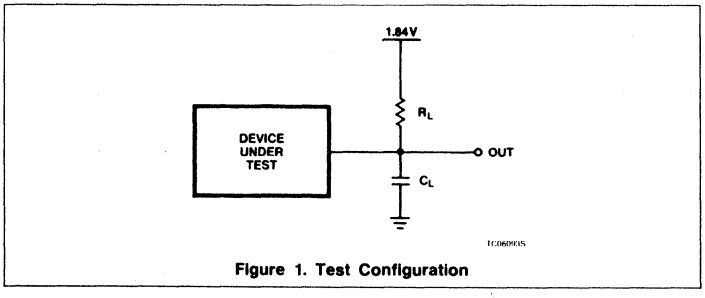


Figure 1. Test Configuration

27C64A O.T.P.

One Time Programmable 64K (8K × 8) EPROMs

Product Specification

Application Specific Products

FEATURES

- **Low power consumption**
  - **100μA maximum CMOS standby current**
- **High–performance speeds**
  - **27C64A–12: 120ns maximum access time**
  - **27C64A–15: 150ns maximum access time**
- **Noise immunity features**
  - **±10% V_{CC} tolerance**
  - **Maximum latch–up immunity through Epitaxial processing**
- **Quick–pulse programming algorithm (3 second typical programming times)**

DESCRIPTION

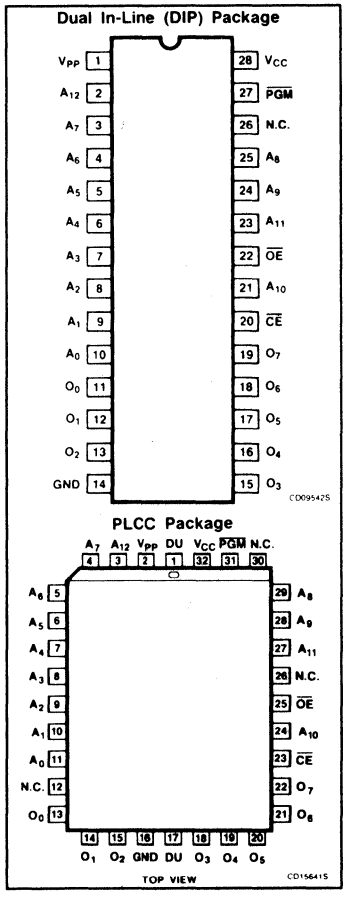
Signetics 27C64A CMOS O.T.P. EPROM is a 64K–bit 5V only memory organized as 8,192 words of 8 bits each. It employs advanced CMOS circuitry for systems requiring low power, high–performance speeds, and immunity to noise. The 27C64A has a non–multiplexed addressing interface and is plug–compatible with the industry standard 2764.

The 27C64A O.T.P. is offered in plastic DIP and plastic leaded chip carrier (PLCC) packages. Plastic EPROMS provide optimum cost effectiveness in production environments. Quick–pulse programming is employed on plastic devices which may speed up programming by as much as one hundred times. In the absence of quick–pulse programming equipment, the intelligent programming algorithm may be utilized.

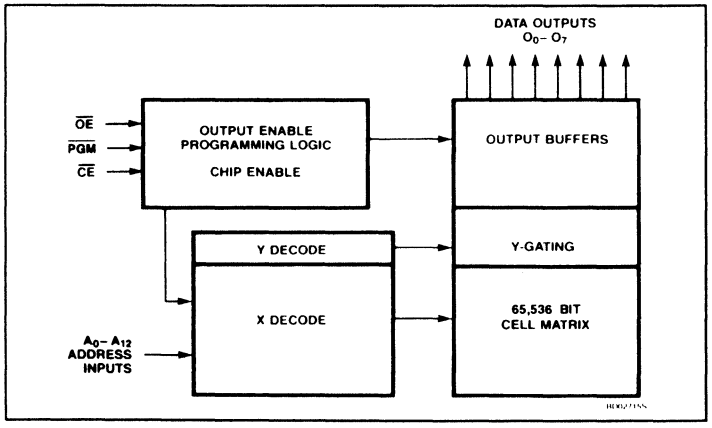
PIN DESCRIPTION

$A_0 - A_{12}$	Addresses
$O_0 - O_7$	Outputs
$\overline{OE}$	Output enable
$\overline{CE}$	Chip enable
N.C.	No connection
GND	Ground
V_{PP}	Program voltage
V_{CC}	Power supply
DU	Don't use
$\overline{PGM}$	Program strobe

PIN CONFIGURATIONS



BLOCK DIAGRAM



One Time Programmable 64K (8K × 8) EPROMs

27C64A O.T.P.

READ MODE: 27C64A

The 27C64A has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins. Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

STANDBY MODE

The 27C64A has a standby mode which reduces the maximum V_{CC} current to 100μA. It is placed in the Standby mode when $\overline{CE}$ is in the High state. When in the Standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

ORDERING INFORMATION

PACKAGE DESCRIPTION	ORDER CODE
28-Pin Plastic Dual in-line 600mil-wide	27C64A-12 N 27C64A-15 N
32-Pin Plastic Leaded Chip Carrier 450mil × 550mil	27C64A-12 A 27C64A-15 A

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
T_A	Temperature under bias	-10 to +80	°C
T_{STG}	Storage temperature range	-65 to +125	°C
V_I, V_O	Voltage inputs and outputs	-2.0 to (V_{CC} + 1)	V
V_H	Voltage on A_9[2] (During intelligent identifier interrogation)	-2.0 to +13.5	V
V_{PP}	Voltage on V_{PP} (During programming)	-2.0 to +14.0	V
V_{CC}	Supply voltage[2]	-2.0 to +7.0	V

NOTES:
1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. All voltages are with respect to network ground.

DEVICE OPERATION[1]

MODE	$\overline{CE}$	$\overline{OE}$[2]	$\overline{PGM}$[2]	V_{PP}[3]	OUTPUTS
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	D_{OUT}
Output disable	V_{IL}	V_{IH}	V_{IH}	V_{CC}	Hi-Z
Standby	V_{IH}	X	X	V_{CC}	Hi-Z

NOTES:
1. All voltages are with respect to network ground.
2. X can be V_{IH} or V_{IL}.
3. V_{PP} may be one diode voltage drop below V_{CC}, and can be connected directly to V_{CC}.

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +70°C$, $+4.5V \leq V_{CC} \leq +5.5V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS Min	LIMITS Typ[3]	LIMITS Max	UNIT
Input current						
I_{IH}	Leakage	$V_{IN} = 5.5V = V_{CC}$		0.01	1.0	µA
I_{IL}	Low	$V_{IL} = 0.45V$		0.01	1.0	µA
I_{PP}	V_{PP} read	$V_{PP} = V_{CC}$			100	µA
Output current						
I_{LO}	Leakage	$\overline{OE}$ or $\overline{CE} = V_{IH}$ $V_{OUT} = 5.5V = V_{CC}$			1.0	µA
		$V_{OUT} = 0V = GND$			1.0	µA
I_{OS}	Short circuit[7, 9]	$V_{OUT} = 0V$			100	mA
Supply current						
I_{CC} TTL	Operating (TTL inputs)[4]	$\overline{OE} = \overline{CE} = V_{IL}$, f = 8.0MHz $V_{PP} = V_{CC}$ $O_{0-7} = 0mA$			20	mA
I_{SB} TTL	Standby (TTL inputs)[4]	$\overline{CE} = V_{IH}$			1.0	mA
I_{SB} CMOS	Standby (CMOS inputs)[5, 6]	$\overline{CE} = V_{IH}$			100	µA
Input voltage[2]						
V_{IL}	Low (TTL)	$V_{PP} = V_{CC}$	–0.5		0.8	V
V_{IL}	Low (CMOS)	$V_{PP} = V_{CC}$	–0.2		0.2	V
V_{IH}	High (TTL)	$V_{PP} = V_{CC}$	2.0		$V_{CC} + 0.5$	V
V_{IH}	High (CMOS)	$V_{PP} = V_{CC}$	$V_{CC} - 0.2$		$V_{CC} + 0.2$	V
V_{PP}	Read[8]	(Operating)	$V_{CC} - 0.7$		V_{CC}	V
Output voltage[2]						
V_{OL}	Low	$I_{OL} = 2.1mA$			0.45	V
V_{OH}	High	$I_{OH} = -2.5mA$	3.5			V
Capacitance[9] $T_A = 25°C$						
C_{IN}	Address and control	$V_{CC} = 5.0V$ f = 1.0MHz			6	pF
C_{OUT}	Outputs	$V_{IN} = 0V$ $V_{OUT} = 0V$			12	pF

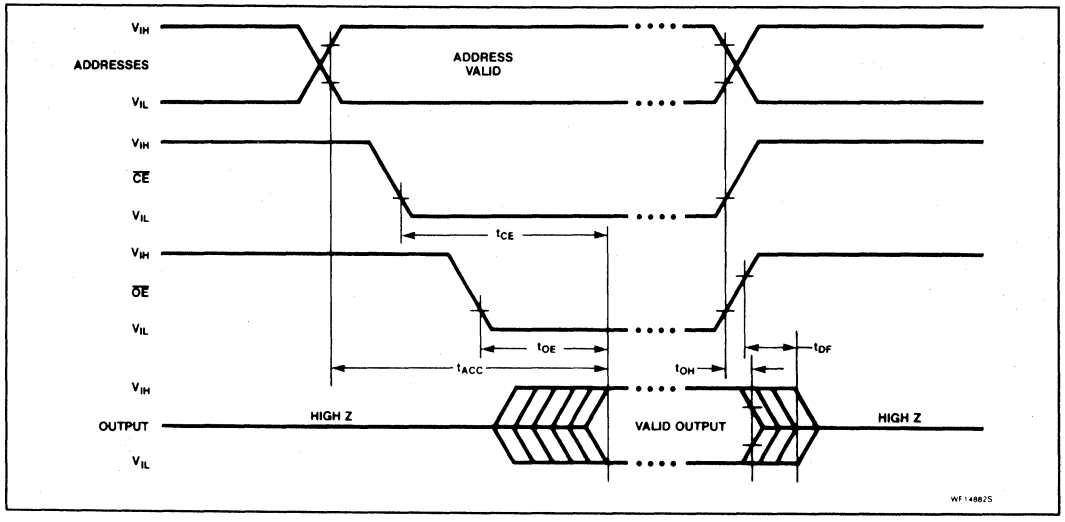
NOTES:
1. Minimum DC input voltage is –0.5V. During transitions the inputs may undershoot to –2.0V for periods less than 20ns.
2. All voltages are with respect to network ground.
3. Typical limits are at $V_{CC} = 5V$, $T_A = 25°C$.
4. TTL inputs: Spec V_{IL}, V_{IH} levels.
   CMOS inputs: GND ± 0.2V to V_{CC} ± 0.2V.
5. $\overline{CE}$ is V_{CC} ± 0.2V. All other inputs can have any value within spec.
6. Maximum active power usage is the sum of $I_{PP} + I_{CC}$ and is measured at a frequency ofd 5MHz.
7. Test one output at a time, duration should not exceed 1 second.
8. V_{PP} may be one diode voltage drop below V_{CC}, and can be connected directly to V_{CC}.
9. Guaranteed by design, not 100% tested.
10. X can be V_{IH} or V_{IL}.

AC ELECTRICAL CHARACTERISTICS $0°C \le T_A \le +70°C$, $+4.5V \le V_{CC} \le +5.5V$, $R_L = 660\Omega$, $C_L = 100pF$

SYMBOL	TO	FROM	27C64A–12		27C64A–15		UNIT
			Min	Max	Min	Max	
Access time[1]							
t_{ACC}	Output	Address		120		150	ns
t_{CE}	Output	$\overline{CE}$		120		150	ns
t_{OE}[3]	Output	$\overline{OE}$		60		65	ns
Disable time[2]							
t_{DF}[4]	Output Hi–Z	$\overline{OE}$ or $\overline{CE}$		30		45	ns
t_{OH}	Output hold	Address, $\overline{CE}$ or $\overline{OE}$	0		0		ns

NOTES:
1. AC characteristics are tested at $V_{IH} = 2.4V$ and $V_{IL} = 0.45V$. Timing measurements made at $V_{OL} = 0.8V$ and $V_{OH} = 2.0V$.
2. Guaranteed by design, not 100% tested.
3. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.
4. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

AC VOLTAGE WAVEFORMS



AC TESTING LOAD CIRCUIT

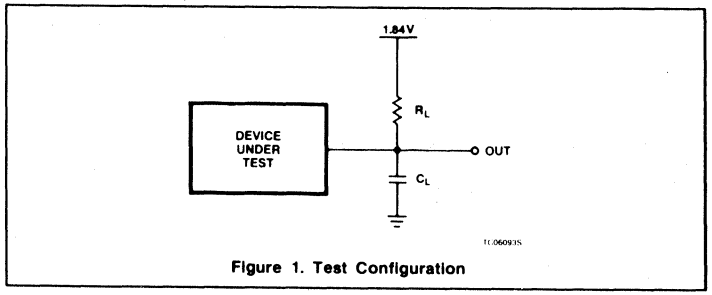


Figure 1. Test Configuration

27C64A O.T.P.

One Time Programmable 64K (8K × 8) EPROMs

Product Specification

Application Specific Products

FEATURES

- **Low power consumption**
  - **100μA maximum CMOS standby current**
- **High–performance speeds**
  - **27C64A–20: 200ns maximum access time**
- **Noise immunity features**
  - **±10% V_{CC} tolerance**
  - **Maximum latch–up immunity through Epitaxial processing**
- **Quick–pulse programming algorithm (3 second typical programming times)**

DESCRIPTION

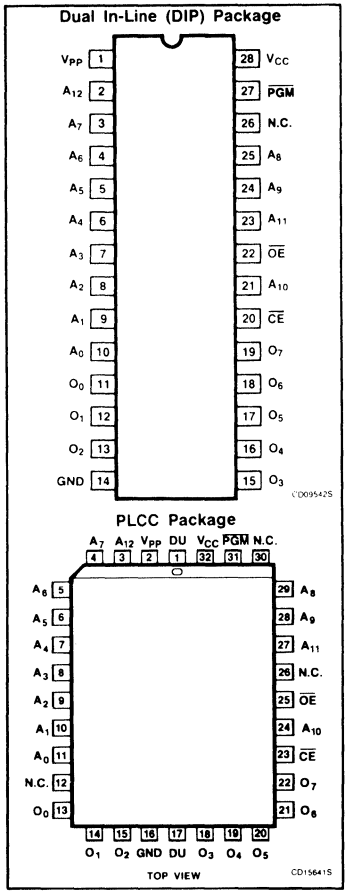
Signetics 27C64A CMOS O.T.P. EPROM is a 64K–bit 5V only memory organized as 8,192 words of 8 bits each. It employs advanced CMOS circuitry for systems requiring low power, high–performance speeds, and immunity to noise. The 27C64A has a non–multiplexed addressing interface and is plug–compatible with the industry standard 2764.

The 27C64A O.T.P. is offered in plastic DIP and plastic leaded chip carrier (PLCC) packages. Plastic EPROMS provide optimum cost effectiveness in production environments. Quick–pulse programming is employed on plastic devices which may speed up programming by as much as one hundred times. In the absence of quick–pulse programming equipment, the intelligent programming algorithm may be utilized.

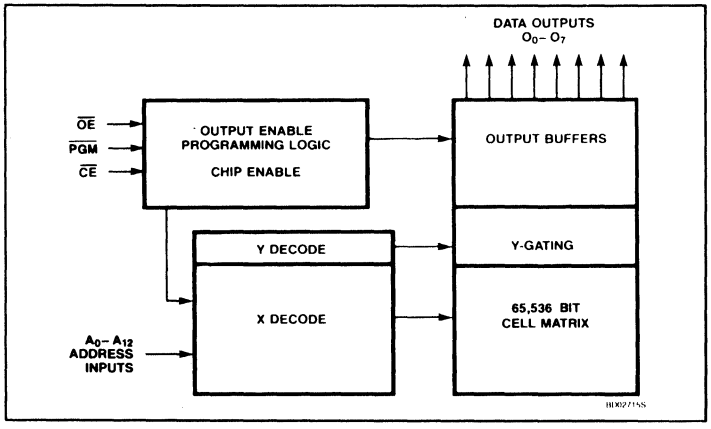
PIN DESCRIPTION

$A_0 - A_{12}$	Addresses
$O_0 - O_7$	Outputs
$\overline{OE}$	Output enable
$\overline{CE}$	Chip enable
N.C.	No connection
GND	Ground
V_{PP}	Program voltage
V_{CC}	Power supply
DU	Don't use
$\overline{PGM}$	Program strobe

PIN CONFIGURATIONS



BLOCK DIAGRAM



READ MODE: 27C64A

The 27C64A has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins. Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

STANDBY MODE

The 27C64A has a standby mode which reduces the maximum V_{CC} current to 100μA. It is placed in the Standby mode when $\overline{CE}$ is in the High state. When in the Standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

ORDERING INFORMATION

PACKAGE DESCRIPTION	ORDER CODE
28-Pin Plastic Dual in-line 600mil-wide	27C64A-20 N
32-Pin Plastic Leaded Chip Carrier 450mil × 550mil	27C64A-20 A

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
T_A	Temperature under bias	-10 to +80	°C
T_{STG}	Storage temperature range	-65 to +125	°C
V_I, V_O	Voltage inputs and outputs	-2.0 to (V_{CC} + 1)	V
V_H	Voltage on A_9[2] (During intelligent identifier interrogation)	-2.0 to +13.5	V
V_{PP}	Voltage on V_{PP} (During programming)	-2.0 to +14.0	V
V_{CC}	Supply voltage[2]	-2.0 to +7.0	V

NOTES:
1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and funtional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. All voltages are with respect to network ground.

DEVICE OPERATION[1]

MODE	$\overline{CE}$	$\overline{OE}$[2]	$\overline{PGM}$[2]	V_{PP}[3]	OUTPUTS
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	D_{OUT}
Output disable	V_{IL}	V_{IH}	V_{IH}	V_{CC}	Hi-Z
Standby	V_{IH}	X	X	V_{CC}	Hi-Z

NOTES:
1. All voltages are with respect to network ground.
2. X can be V_{IH} or V_{IL}.
3. V_{PP} may be one diode voltage drop below V_{CC}, and can be connected directly to V_{CC}.

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +70°C$, $+4.5V \leq V_{CC} \leq +5.5V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[3]	Max	
Input current						
I_{IH}	Leakage	$V_{IN} = 5.5V = V_{CC}$		0.01	1.0	µA
I_{IL}	Low	$V_{IL} = 0.45V$		0.01	1.0	µA
I_{PP}	V_{PP} read	$V_{PP} = V_{CC}$			100	µA
Output current						
I_{LO}	Leakage	$\overline{OE}$ or $\overline{CE} = V_{IH}$ $V_{OUT} = 5.5V = V_{CC}$			1.0	µA
		$V_{OUT} = 0V = GND$			1.0	µA
I_{OS}	Short circuit[7, 9]	$V_{OUT} = 0V$			100	mA
Supply current						
I_{CC} TTL	Operating (TTL inputs)[4]	$\overline{OE} = \overline{CE} = V_{IL}$, f = 5.0MHz $V_{PP} = V_{CC}$ $O_{0-7} = 0mA$			20	mA
I_{SB} TTL	Standby (TTL inputs)[4]	$\overline{CE} = V_{IH}$			1.0	mA
I_{SB} CMOS	Standby (CMOS inputs)[5, 6]	$\overline{CE} = V_{IH}$			100	µA
Input voltage[2]						
V_{IL}	Low (TTL)	$V_{PP} = V_{CC}$	–0.5		0.8	V
V_{IL}	Low (CMOS)	$V_{PP} = V_{CC}$	–0.2		0.2	V
V_{IH}	High (TTL)	$V_{PP} = V_{CC}$	2.0		$V_{CC} + 0.5$	V
V_{IH}	High (CMOS)	$V_{PP} = V_{CC}$	$V_{CC} - 0.2$		$V_{CC} + 0.2$	V
V_{PP}	Read[8]	(Operating)	$V_{CC} - 0.7$		V_{CC}	V
Output voltage[2]						
V_{OL}	Low	$I_{OL} = 2.1mA$			0.45	V
V_{OH}	High	$I_{OH} = -2.5mA$	3.5			V
Capacitance[9] $T_A = 25°C$						
C_{IN}	Address and control	$V_{CC} = 5.0V$ f = 1.0MHz			6	pF
C_{OUT}	Outputs	$V_{IN} = 0V$ $V_{OUT} = 0V$			12	pF

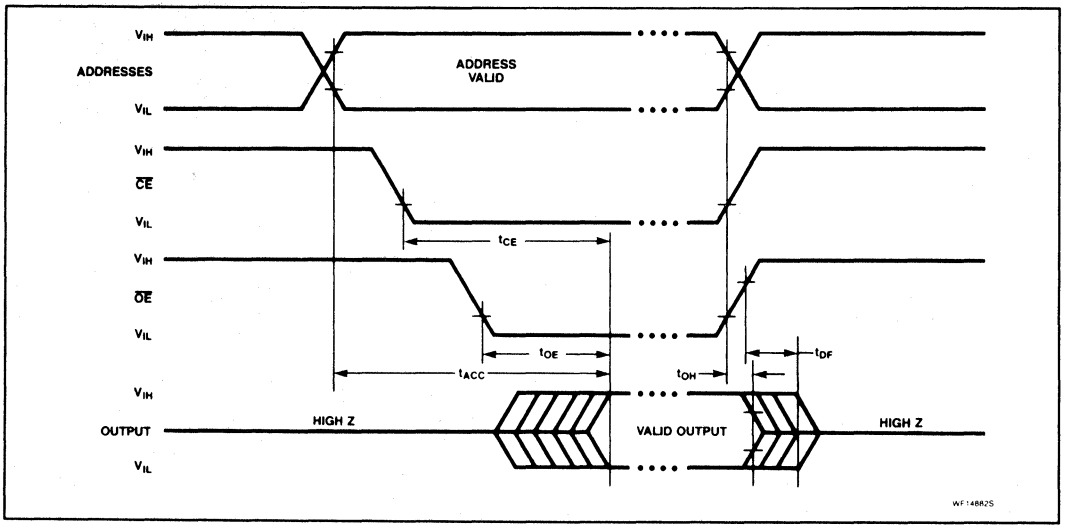
NOTES:
1. Minimum DC input voltage is –0.5V. During transitions the inputs may undershoot to –2.0V for periods less than 20ns.
2. All voltages are with respect to network ground.
3. Typical limits are at $V_{CC} = 5V$, $T_A = 25°C$.
4. TTL inputs: Spec V_{IL}, V_{IH} levels.
   CMOS inputs: GND ± 0.2V to V_{CC} ± 0.2V.
5. $\overline{CE}$ is V_{CC} ± 0.2V. All other inputs can have any value within spec.
6. Maximum active power usage is the sum of $I_{PP} + I_{CC}$ and is measured at a frequency ofd 5MHz.
7. Test one output at a time, duration should not exceed 1 second.
8. V_{PP} may be one diode voltage drop below V_{CC}, and can be connected directly to V_{CC}.
9. Guaranteed by design, not 100% tested.
10. X can be V_{IH} or V_{IL}.

AC ELECTRICAL CHARACTERISTICS $0°C \le T_A \le +70°C$, $+4.5V \le V_{CC} \le +5.5V$, $R_L = 660\Omega$, $C_L = 100pF$

SYMBOL	TO	FROM	27C64A–20 Min	27C64A–20 Max	UNIT
Access time[1]					
t_{ACC}	Output	Address		200	ns
t_{CE}	Output	$\overline{CE}$		200	ns
t_{OE}[3]	Output	$\overline{OE}$		75	ns
Disable time[2]					
t_{DF}[4]	Output Hi–Z	$\overline{OE}$ or $\overline{CE}$		55	ns
t_{OH}	Output hold	Address, $\overline{CE}$ or $\overline{OE}$	0		ns

NOTES:
1. AC characteristics are tested at $V_{IH} = 2.4V$ and $V_{IL} = 0.45V$. Timing measurements made at $V_{OL} = 0.8V$ and $V_{OH} = 2.0V$.
2. Guaranteed by design, not 100% tested.
3. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.
4. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

AC VOLTAGE WAVEFORMS



AC TESTING LOAD CIRCUIT

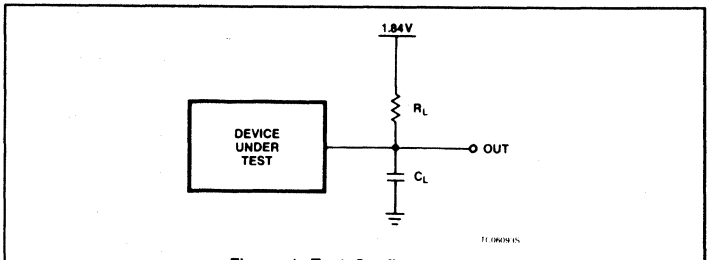


Figure 1. Test Configuration

27C64A U.V.

64K-Bit Erasable CMOS EPROM (8K × 8)

Product Specification

Application Specific Products

DESCRIPTION

Signetics' 27C64A CMOS EPROM is a 64K-bit 5V only memory organized as 8,192 words of 8 bits each. It employs advanced CMOS circuitry for systems requiring low power, high-performance speeds, and immunity to noise. The 27C64A has a non-multiplexed addressing interface and is plug-compatible with the industry standard 2764.

The 27C64A achieves both high performance and low power consumption, making it ideal for high performance, portable equipment. The 27C64A is offered in a ceramic DIP package. This device can be programmed with standard EPROM programmers, and the intelligent programming algorithm may be used.

FEATURES

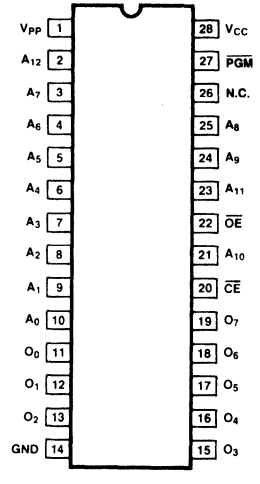
- **Low power consumption**
  - **100μA maximum CMOS standby current**
- **High-performance speeds**
  - **27C64A-10: 100ns maximum access time**
- **Noise immunity features**
  - **± 10% V_{CC} tolerance**
  - **Maximum latch-up immunity through epitaxial processing**

PIN DESCRIPTION

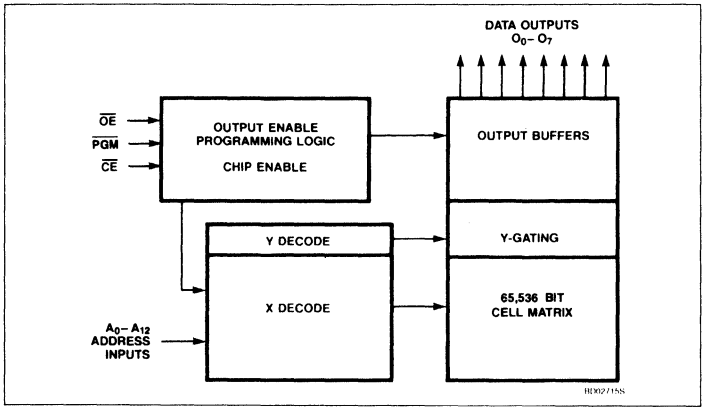
$A_0 - A_{12}$	Addresses
$O_0 - O_7$	Outputs
$\overline{OE}$	Output enable
$\overline{CE}$	Chip enable
N.C.	No connection
GND	Ground
V_{PP}	Program voltage
V_{CC}	Power supply
$\overline{PGM}$	Program strobe

PIN CONFIGURATION

FA Package



BLOCK DIAGRAM



64K-Bit Erasable CMOS EPROM (8K × 8) — 27C64A U.V.

READ MODE: 27C64A

The 27C64A has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins. Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been Low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

STANDBY MODE

The 27C64A has a standby mode which reduces the maximum V_{CC} current to 100μA. It is placed in the Standby mode when $\overline{CE}$ is in the High state. When in the Standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
28-pin Ceramic DIP with quartz window (600mil-wide)	27C64A-10 FA

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
T_A	Temperature under bias	−10 to +80	°C
T_{STG}	Storage temperature range	−65 to +125	°C
V_I, V_O	Voltage inputs and outputs	−2.0 to (V_{CC} + 1)	V
V_H	Voltage on A_9[2] (During intelligent identifier interrogation)	−2.0 to +13.5	V
V_{PP}	Voltage on V_{PP}[2] (During programming)	−2.0 to +14.0	V
V_{CC}	Supply voltage[2]	−2.0 to +7.0	V

NOTES:

1. Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. All voltages are with respect to network ground.

DEVICE OPERATION[2]

MODE	$\overline{CE}$	$\overline{OE}$[10]	$\overline{PGM}$[10]	V_{PP}[8]	OUTPUTS
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	D_{OUT}
Output disable	V_{IL}	V_{IH}	V_{IH}	V_{CC}	Hi-Z
Standby	V_{IH}	X	X	V_{CC}	Hi-Z

Notes on following page.

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +70°C$, $+4.5V \leq V_{CC} \leq +5.5V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[3]	Max	
Input current						
I_{IH}	Leakage	$V_{IN} = 5.5V = V_{CC}$		0.01	1.0	μA
I_{IL}	Low	$V_{IL} = 0.45V$		0.01	1.0	μA
I_{PP}	V_{PP} read	$V_{PP} = V_{CC}$			100	μA
Output current						
I_{LO}	Leakage	$\overline{OE}$ or $\overline{CE} = V_{IH}$ $V_{OUT} = 5.5V = V_{CC}$			1.0	μA
		$V_{OUT} = 0V = GND$			1.0	μA
I_{OS}	Short circuit[7, 9]	$V_{OUT} = 0V$			100	mA
Supply current						
I_{CC} TTL	Operating (TTL inputs)[4]	$\overline{CE} = \overline{OE} = V_{IL}$, f = 10MHz $V_{PP} = V_{CC}$ $O_{0-7} = 0mA$			20	mA
I_{SB} TTL	Standby (TTL inputs)[4]	$\overline{CE} = V_{IH}$			1.0	mA
I_{SB} CMOS	Standby (CMOS inputs)[5, 6]	$\overline{CE} = V_{IH}$			100	μA
Input voltage[2]						
V_{IL}	Low (TTL)	$V_{PP} = V_{CC}$	−0.5		0.8	V
V_{IL}	Low (CMOS)	$V_{PP} = V_{CC}$	−0.2		0.2	V
V_{IH}	High (TTL)	$V_{PP} = V_{CC}$	2.0		$V_{CC} + 0.5$	V
V_{IH}	High (CMOS)	$V_{PP} = V_{CC}$	$V_{CC} - 0.2$		$V_{CC} + 0.2$	V
V_{PP}	Read[8]	(Operating)	$V_{CC} - 0.7$		V_{CC}	V
Output voltage[2]						
V_{OL}	Low	$I_{OL} = 2.1mA$			0.45	V
V_{OH}	High	$I_{OH} = -2.5mA$	3.5			V
Capacitance[9] $T_A = 25°C$						
C_{IN}	Address and control	$V_{CC} = 5.0V$ f = 1.0MHz $V_{IN} = 0V$ $V_{OUT} = 0V$			6	pF
C_{OUT}	Outputs				12	pF

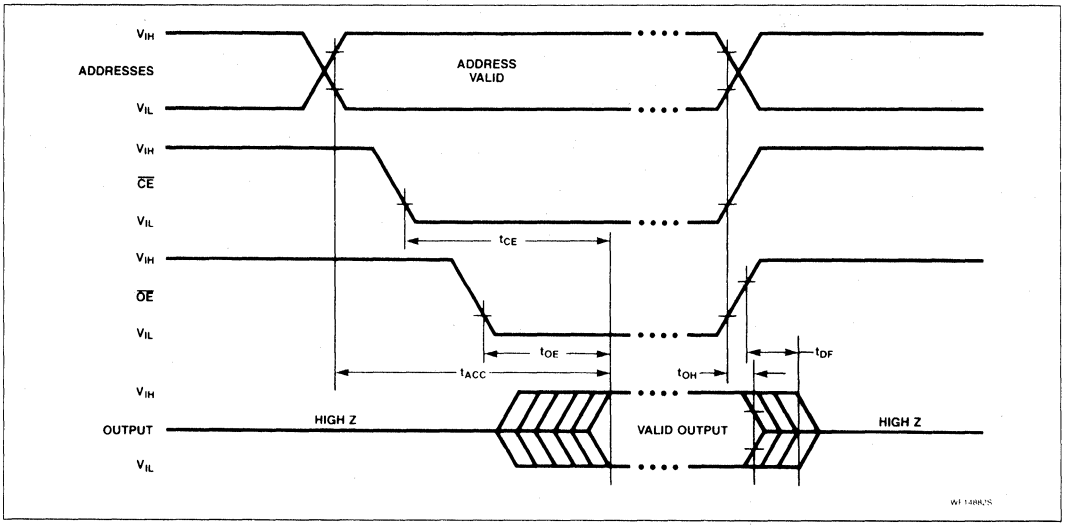
NOTES:
1. Minimum DC input voltage is −0.5V. During transitions the inputs may undershoot to −2.0V for periods less than 20ns.
2. All voltages are with respect to network ground.
3. Typical limits are at $V_{CC} = 5V$, $T_A = 25°C$.
4. TTL inputs: Specification V_{IL}, V_{IH} levels.
   CMOS inputs: GND ± 0.2V to V_{CC} ± 0.2V.
5. $\overline{CE}$ is V_{CC} ± 0.2V. All other inputs can have any value within specification.
6. Maximum active power usage is the sum of $I_{PP} + I_{CC}$ and is measured at a frequency of 5MHz.
7. Test one output at a time, duration should not exceed 1 second.
8. V_{PP} may be one diode voltage drop below V_{CC}, and can be connected directly to V_{CC}.
9. Guaranteed by design, not 100% tested.
10. X can be V_{IH} or V_{IL}.

AC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +70°C$, $+4.5V \leq V_{CC} \leq +5.5V$, $R_L = 660\Omega$, $C_L = 100pF$

SYMBOL	TO	FROM	27C64A - 10		UNIT
			Min	Max	
Access time[1]					
t_{ACC}	Output	Address		100	ns
t_{CE}	Output	$\overline{CE}$		100	ns
t_{OE}[3]	Output	$\overline{OE}$		35	ns
Disable time[2]					
t_{DF}[4]	Output Hi-Z	$\overline{OE}$ or $\overline{CE}$		25	ns
t_{OH}	Output hold	Address, $\overline{CE}$ or $\overline{OE}$	0		ns

NOTES:
1. AC characteristics are tested at $V_{IH} = 2.4V$ and $V_{IL} = 0.45V$. Timing measurements made at $V_{OL} = 0.8V$ and $V_{OH} = 2.0V$.
2. Guaranteed by design, not 100% tested.
3. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.
4. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

AC VOLTAGE WAVEFORMS



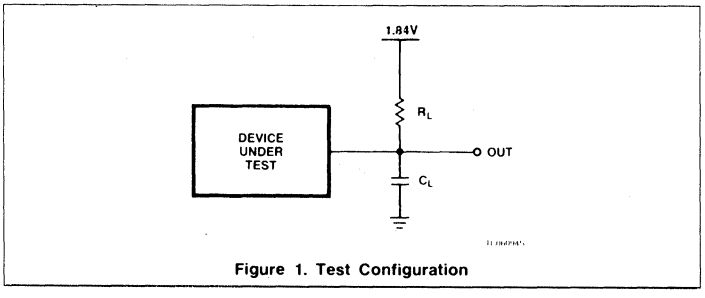


Figure 1. Test Configuration

27C64A U.V.

UV Erasable
64K (8K × 8) EPROMs

Product Specification

Application Specific Products

FEATURES

- **Low power consumption**
  - **100μA maximum CMOS standby current**
- **High–performance speeds**
  - **27C64A–12: 120ns maximum access time**
  - **27C64A–15: 150ns maximum access time**
- **Noise immunity features**
  - **±10% V_{CC} tolerance**
  - **Maximum latch–up immunity through Epitaxial processing**

DESCRIPTION

Signetics 27C64A CMOS EPROM is a 64K–bit 5V only memory organized as 8,192 words of 8 bits each. It employs advanced CMOS circuitry for systems requiring low power, high–performance speeds, and immunity to noise. The 27C64A has a non–multiplexed addressing interface and is plug–compatible with the industry standard 2764.

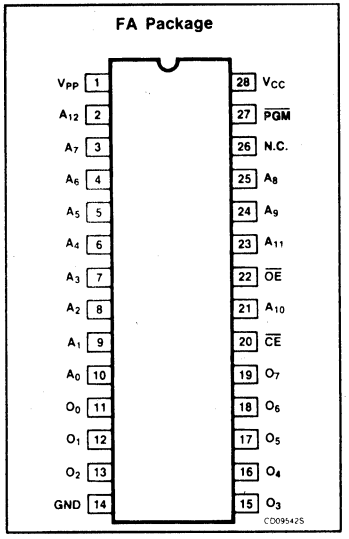
The 27C64A achieves both high performance and low power consumption, making it ideal for high performance, portable equipment. The 27C64A is offered in a ceramic DIP package. This device can be programmed with standard EPROM programmers, and the intelligent programming algorithm may be used.

PIN DESCRIPTION

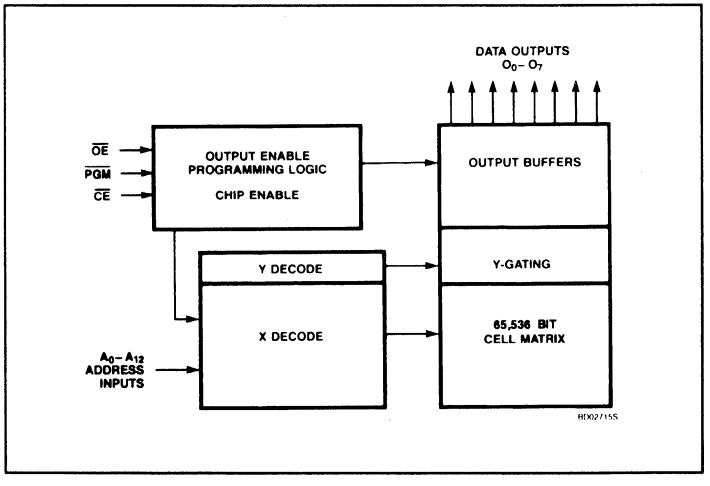
$A_0 - A_{12}$	Addresses
$O_0 - O_7$	Outputs
$\overline{OE}$	Output enable
$\overline{CE}$	Chip enable
N.C.	No connection
GND	Ground
V_{PP}	Program voltage
V_{CC}	Power supply
$\overline{PGM}$	Program strobe

PIN CONFIGURATION

FA Package



BLOCK DIAGRAM



READ MODE: 27C64A

The 27C64A has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins. Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been Low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

STANDBY MODE

The 27C64A has a standby mode which reduces the maximum V_{CC} current to 100μA. It is placed in the Standby mode when $\overline{CE}$ is in the High state. When in the Standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

ORDERING INFORMATION

PACKAGE DESCRIPTION	ORDER CODE
28-Pin CERDIP with quartz window (600mil-wide)	27C64A-12 FA 27C64A-15 FA

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
T_A	Temperature under bias	−10 to +80	°C
T_{STG}	Storage temperature range	−65 to +125	°C
V_I, V_O	Voltage inputs and outputs	−2.0 to (V_{CC} + 1)	V
V_H	Voltage on A_9[2] (During intelligent identifier interrogation)	−2.0 to +13.5	V
V_{PP}	Voltage on V_{PP}[2] (During programming)	−2.0 to +14.0	V
V_{CC}	Supply voltage[2]	−2.0 to +7.0	V

NOTES:
1. Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. All voltages are with respect to network ground.

DEVICE OPERATION[1]

MODE	$\overline{CE}$	$\overline{OE}$[2]	$\overline{PGM}$[2]	V_{PP}[3]	OUTPUTS
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	D_{OUT}
Output disable	V_{IL}	V_{IH}	V_{IH}	V_{CC}	Hi-Z
Standby	V_{IH}	X	X	V_{CC}	Hi-Z

NOTES:
1. All voltages are with respect to network ground.
2. X can be V_{IH} or V_{IL}.
3. V_{PP} may be one diode voltage drop below V_{CC}, and can be connected directly to V_{CC}.

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +70°C$, $+4.5V \leq V_{CC} \leq +5.5V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[3]	Max	
Input current						
I_{IH}	Leakage	$V_{IN} = 5.5V = V_{CC}$		0.01	1.0	µA
I_{IL}	Low	$V_{IL} = 0.45V$		0.01	1.0	µA
I_{PP}	V_{PP} read	$V_{PP} = V_{CC}$			100	µA
Output current						
I_{LO}	Leakage	$\overline{OE}$ or $\overline{CE} = V_{IH}$			1.0	µA
		$V_{OUT} = 5.5V = V_{CC}$ $V_{OUT} = 0V = GND$			1.0	µA
I_{OS}	Short circuit[7, 9]	$V_{OUT} = 0V$			100	mA
Supply current						
I_{CC} TTL	Operating (TTL inputs)[4]	$\overline{OE} = \overline{CE} = V_{IL}$, f = 8.0MHz $V_{PP} = V_{CC}$ $O_{0-7} = 0mA$			20	mA
I_{SB} TTL	Standby (TTL inputs)[4]	$\overline{CE} = V_{IH}$			1.0	mA
I_{SB} CMOS	Standby (CMOS inputs)[5, 6]	$\overline{CE} = V_{IH}$			100	µA
Input voltage[2]						
V_{IL}	Low (TTL)	$V_{PP} = V_{CC}$	–0.5		0.8	V
V_{IL}	Low (CMOS)	$V_{PP} = V_{CC}$	–0.2		0.2	V
V_{IH}	High (TTL)	$V_{PP} = V_{CC}$	2.0		$V_{CC} + 0.5$	V
V_{IH}	High (CMOS)	$V_{PP} = V_{CC}$	$V_{CC} - 0.2$		$V_{CC} + 0.2$	V
V_{PP}	Read[8]	(Operating)	$V_{CC} - 0.7$		V_{CC}	V
Output voltage[2]						
V_{OL}	Low	$I_{OL} = 2.1mA$			0.45	V
V_{OH}	High	$I_{OH} = -2.5mA$	3.5			V
Capacitance[9] $T_A = 25°C$						
C_{IN}	Address and control	$V_{CC} = 5.0V$ f = 1.0MHz			6	pF
C_{OUT}	Outputs	$V_{IN} = 0V$ $V_{OUT} = 0V$			12	pF

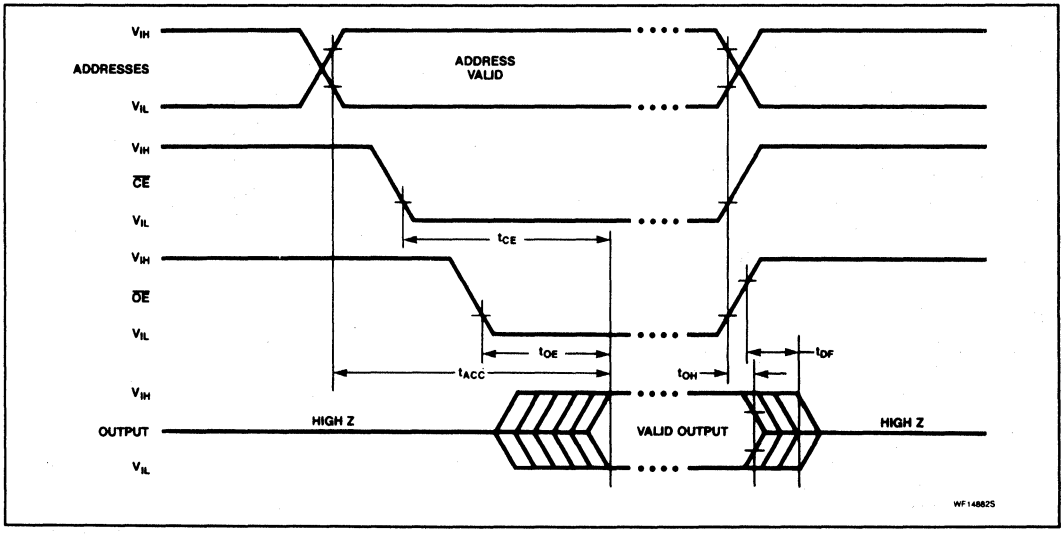
NOTES:
1. Minimum DC input voltage is –0.5V. During transitions the inputs may undershoot to –2.0V for periods less than 20ns.
2. All voltages are with respect to network ground.
3. Typical limits are at $V_{CC} = 5V$, $T_A = 25°C$.
4. TTL inputs: Spec V_{IL}, V_{IH} levels.
   CMOS inputs: GND ± 0.2V to V_{CC} ± 0.2V.
5. $\overline{CE}$ is V_{CC} ± 0.2V. All other inputs can have any value within specifications.
6. Maximum active power usage is the sum of $I_{PP} + I_{CC}$ and is measured at a frequency ofd 5MHz.
7. Test one output at a time, duration should not exceed 1 second.
8. V_{PP} may be one diode voltage drop below V_{CC}, and can be connected directly to V_{CC}.
9. Guaranteed by design, not 100% tested.
10. X can be V_{IH} or V_{IL}.

AC ELECTRICAL CHARACTERISTICS $0°C \le T_A \le +70°C$, $+4.5V \le V_{CC} \le +5.5V$, $R_L = 660\Omega$, $C_L = 100pF$

SYMBOL	TO	FROM	27C64A–12		27C64A–15		UNIT
			Min	Max	Min	Max	
Access time[1]							
t_{ACC}	Output	Address		120		150	ns
t_{CE}	Output	$\overline{CE}$		120		150	ns
t_{OE}[3]	Output	$\overline{OE}$		60		65	ns
Disable time[2]							
t_{DF}[4]	Output Hi–Z	$\overline{OE}$ or $\overline{CE}$		30		45	ns
t_{OH}	Output hold	Address, $\overline{CE}$ or $\overline{OE}$	0		0		ns

NOTES:
1. AC characteristics are tested at $V_{IH} = 2.4V$ and $V_{IL} = 0.45V$. Timing measurements made at $V_{OL} = 0.8V$ and $V_{OH} = 2.0V$.
2. Guaranteed by design, not 100% tested.
3. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.
4. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

AC VOLTAGE WAVEFORMS



AC TESTING LOAD CIRCUIT

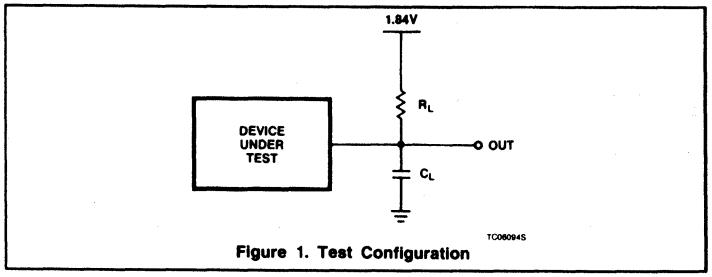


Figure 1. Test Configuration

27C64A U.V.

64K-Bit Erasable CMOS EPROM (8K × 8)

Product Specification

Application Specific Products

DESCRIPTION

Signetics' 27C64A CMOS EPROM is a 64K-bit 5V only memory organized as 8,192 words of 8 bits each. It employs advanced CMOS circuitry for systems requiring low power, high-performance speeds, and immunity to noise. The 27C64A has a non-multiplexed addressing interface and is plug-compatible with the industry standard 2764.

The 27C64A achieves both high performance and low power consumption, making it ideal for high performance, portable equipment. The 27C64A is offered in a ceramic DIP package. This device can be programmed with standard EPROM programmers, and the intelligent programming algorithm may be used.

FEATURES

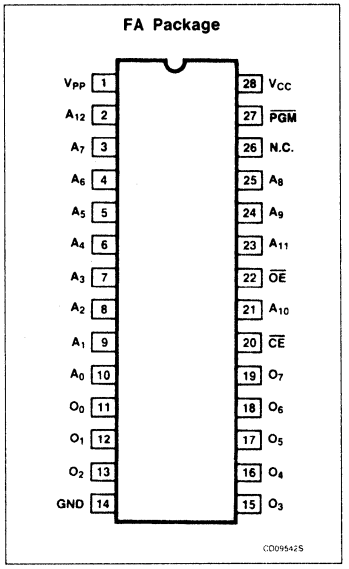
- **Low power consumption**
  - **100μA maximum CMOS standby current**
- **High-performance speeds**
  - **27C64A-20: 200ns maximum access time**
- **Noise immunity features**
  - **± 10% V_{CC} tolerance**
  - **Maximum latch-up immunity through epitaxial processing**

PIN DESCRIPTION

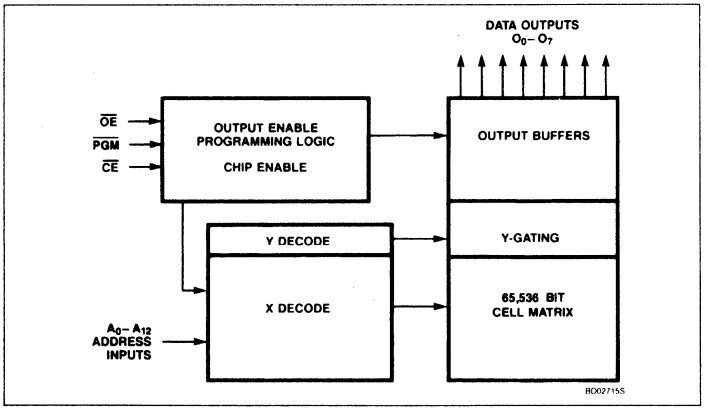
$A_0 - A_{12}$	Addresses
$O_0 - O_7$	Outputs
$\overline{OE}$	Output enable
$\overline{CE}$	Chip enable
N.C.	No connection
GND	Ground
V_{PP}	Program voltage
V_{CC}	Power supply
$\overline{PGM}$	Program strobe

PIN CONFIGURATION

FA Package



BLOCK DIAGRAM



64K-Bit Erasable CMOS EPROM (8K × 8) 27C64A U.V.

READ MODE: 27C64A

The 27C64A has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins. Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been Low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

STANDBY MODE

The 27C64A has a standby mode which reduces the maximum V_{CC} current to 100μA. It is placed in the Standby mode when $\overline{CE}$ is in the High state. When in the Standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
28-pin CERDIP with quartz window (600mil-wide)	27C64A-20 FA

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
T_A	Temperature under bias	−10 to +80	°C
T_{STG}	Storage temperature range	−65 to +125	°C
V_I, V_O	Voltage inputs and outputs	−2.0 to (V_{CC} + 1)	V
V_H	Voltage on A_9[2] (During intelligent identifier interrogation)	−2.0 to +13.5	V
V_{PP}	Voltage on V_{PP}[2] (During programming)	−2.0 to +14.0	V
V_{CC}	Supply voltage[2]	−2.0 to +7.0	V

NOTE:

1. Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. All voltages are with respect to network ground.

DEVICE OPERATION[2]

MODE	$\overline{CE}$	$\overline{OE}$[10]	$\overline{PGM}$[10]	V_{PP}[8]	OUTPUTS
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	D_{OUT}
Output disable	V_{IL}	V_{IH}	V_{IH}	V_{CC}	Hi-Z
Standby	V_{IH}	X	X	V_{CC}	Hi-Z

Notes on following page.

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +70°C$, $+4.5V \leq V_{CC} \leq +5.5V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[3]	Max	
Input current						
I_{IH}	Leakage	$V_{IN} = 5.5V = V_{CC}$		0.01	1.0	μA
I_{IL}	Low	$V_{IL} = 0.45V$		0.01	1.0	μA
I_{PP}	V_{PP} read	$V_{PP} = V_{CC}$			100	μA
Output current						
I_{LO}	Leakage	$\overline{OE}$ or $\overline{CE} = V_{IH}$			1.0	μA
		$V_{OUT} = 5.5V = V_{CC}$ $V_{OUT} = 0V = GND$			1.0	μA
I_{OS}	Short circuit[7, 9]	$V_{OUT} = 0V$			100	mA
Supply current						
I_{CC} TTL	Operating (TTL inputs)[4]	$\overline{CE} = \overline{OE} = V_{IL}$, f = 5MHz $V_{PP} = V_{CC}$ $O_{0-7} = 0mA$			20	mA
I_{SB} TTL	Standby (TTL inputs)[4]	$\overline{CE} = V_{IH}$			1.0	mA
I_{SB} CMOS	Standby (CMOS inputs)[5, 6]	$\overline{CE} = V_{IH}$			100	μA
Input voltage[2]						
V_{IL}	Low (TTL)	$V_{PP} = V_{CC}$	-0.5		0.8	V
V_{IL}	Low (CMOS)	$V_{PP} = V_{CC}$	-0.2		0.2	V
V_{IH}	High (TTL)	$V_{PP} = V_{CC}$	2.0		$V_{CC} + 0.5$	V
V_{IH}	High (CMOS)	$V_{PP} = V_{CC}$	$V_{CC} - 0.2$		$V_{CC} + 0.2$	V
V_{PP}	Read[8]	(Operating)	$V_{CC} - 0.7$		V_{CC}	V
Output voltage[2]						
V_{OL}	Low	$I_{OL} = 2.1mA$			0.45	V
V_{OH}	High	$I_{OH} = -2.5mA$	3.5			V
Capacitance[9] $T_A = 25°C$						
C_{IN}	Address and control	$V_{CC} = 5.0V$ f = 1.0MHz			6	pF
C_{OUT}	Outputs	$V_{IN} = 0V$ $V_{OUT} = 0V$			12	pF

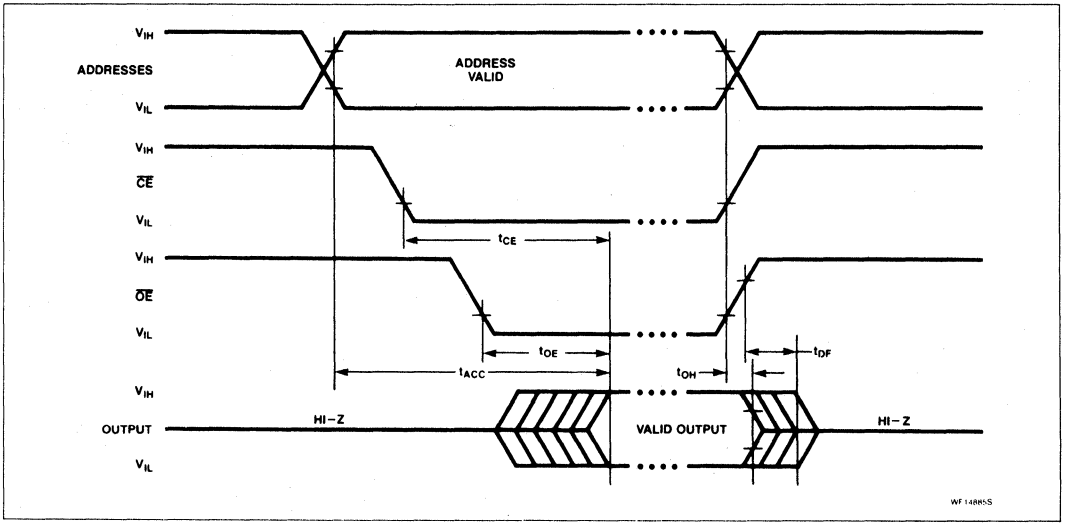
NOTES:
1. Minimum DC input voltage is -0.5V. During transitions the inputs may undershoot to -2.0V for periods less than 20ns.
2. All voltages are with respect to network ground.
3. Typical limits are at $V_{CC} = 5V$, $T_A = 25°C$.
4. TTL inputs: Specification V_{IL}, V_{IH} levels.
   CMOS inputs: GND ± 0.2V to V_{CC} ± 0.2V.
5. $\overline{CE}$ is V_{CC} ± 0.2V. All other inputs can have any value within specification.
6. Maximum active power usage is the sum of $I_{PP} + I_{CC}$ and is measured at a frequency of 5MHz.
7. Test one output at a time, duration should not exceed 1 second.
8. V_{PP} may be one diode voltage drop below V_{CC}, and can be connected directly to V_{CC}.
9. Guaranteed by design, not 100% tested.
10. X can be V_{IH} or V_{IL}.

AC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +70°C$, $+4.5V \leq V_{CC} \leq +5.5V$, $R_L = 660\Omega$, $C_L = 100pF$

SYMBOL	TO	FROM	27C64A - 20		UNIT
			Min	Max	
Access time[1]					
t_{ACC}	Output	Address		200	ns
t_{CE}	Output	$\overline{CE}$		200	ns
t_{OE}[3]	Output	$\overline{OE}$		75	ns
Disable time[2]					
t_{DF}[4]	Output Hi-Z	$\overline{OE}$ or $\overline{CE}$		55	ns
t_{OH}	Output hold	Address, $\overline{CE}$ or $\overline{OE}$	0		ns

NOTES:
1. AC characteristics are tested at $V_{IH} = 2.4V$ and $V_{IL} = 0.45V$. Timing measurements made at $V_{OL} = 0.8V$ and $V_{OH} = 2.0V$.
2. Guaranteed by design, not 100% tested.
3. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.
4. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

AC VOLTAGE WAVEFORMS



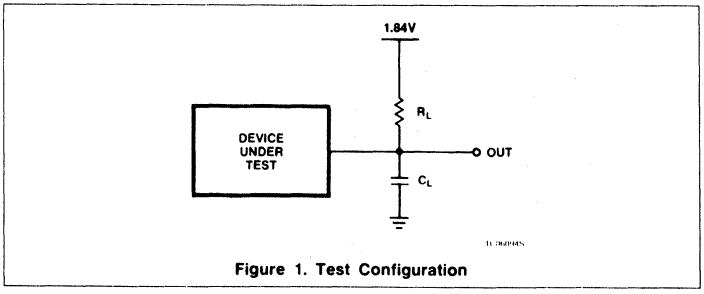


Figure 1. Test Configuration

27HC641 O.T.P.
One Time Programmable 64K-Bit CMOS EPROM (8K × 8)

Product Specification

Application Specific Products

DESCRIPTION

The 27HC641 CMOS, O.T.P. EPROM is a high-speed electrically programmable Read Only Memory. It is organized as 8192 words of 8 bits and operates from a single 5V ±10% power supply. All outputs offer 3-State operation and are fully TTL compatible.

The 27HC641 uses advanced CMOS circuitry which allows operation at bipolar PROM speeds while consuming lower power. The highest degree of protection against latch-up is achieved through epitaxial processing simplifying the design of electronic equipment which is subject to high noise environments.

The 27HC641 is available in industry standard packages with the same pinout as most 64K bipolar PROMs. This makes it easy to upgrade systems currently using bipolar PROMs and provide a lower power memory system solution.

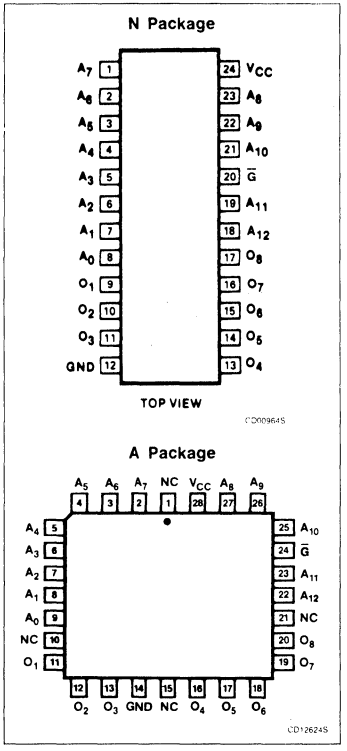
FEATURES

- **Address access time:**
  - **27HC641-55 55ns max**
  - **27HC641-45 45ns max**
- **Operating I_{CC}: 110mA max**
- **3-State outputs**
- **JEDEC standard 24-pin DIP and 28-pin PLCC package**
- **Direct replacement for standard 64K TTL PROMs**
- **Fully TTL compatible**

APPLICATIONS

- **Prototyping and volume production**
- **High-performance mini- and microcomputers**
- **High-speed program store and look-up tables**

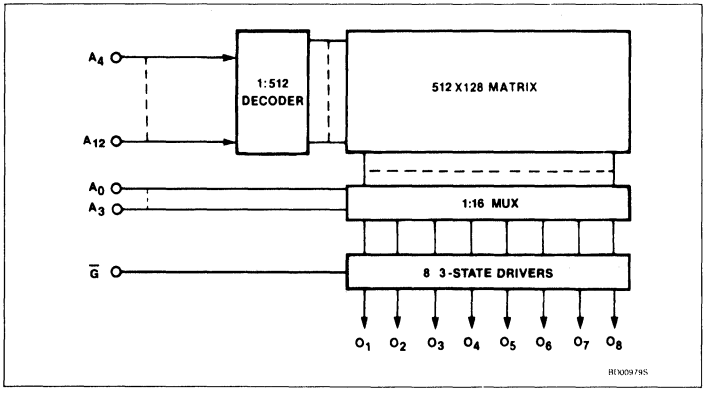
PIN CONFIGURATIONS



ORDERING INFORMATION

DESCRIPTION	ORDER CODE	
	45ns	55ns
24-pin plastic DIP (600mil-wide)	27HC641-45 N	27HC641-55 N
28-pin plastic leaded chip carrier	27HC641-45 A	27HC641-55 A

BLOCK DIAGRAM



PIN NAMES

$A_0 - A_{12}$	Address inputs
$O_1 - O_8$	Data outputs
$\overline{G}$	Output Enable
V_{CC}	Supply voltage
NC	No Connect
GND	Ground (V_{SS})

One Time Programmable 64K-Bit CMOS EPROM (8K × 8)

27HC641 O.T.P.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
V_I, V_O	Voltage on any pin[2]	−0.5 to V_{CC} + 1V	V
T_A	Temperature under bias	−10 to +85	°C
T_{STG}	Storage temperature range	−65 to +150	°C
V_{PP}	Voltage on $\overline{G}$ pin	−0.5 to 13.5	V

DC OPERATING CONDITIONS $0°C \leq T_A \leq +70°C$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Supply voltage						
V_{CC}		GND = 0V	4.5	5.0	5.5	V
Input voltage						
V_{IH}	High		2.0		V_{CC} + 0.5	V
V_{IL}	Low		−0.1		0.8	V

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +70°C$, $4.5V \leq V_{CC} \leq 5.5V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Input Current						
I_{IH}	High	$V_{IN} = V_{CC}$			10	μA
I_{IL}[3]	Low	V_{IN} = 0.45V			10	μA
Output Current						
I_{LO}	Leakage	V_{OUT} = 0 to V_{CC}			±10	μA
I_{OS}	Output short-circuit current[4]	V_{OUT} = 0V, $\overline{G} = V_{IL}$	−15		−70	mA
Supply Current						
I_{CC}	V_{CC} operating current	$\overline{G} = V_{IH}$, O_{1-8} = 0mA, f = 20MHz			110	mA
Input Voltage						
V_{IC}	Input clamp voltage	I_{IC} = −12mA			−1.2	V
Output Voltage						
V_{OH}	High	I_{OH} = −4mA	2.4			V
V_{OL}	Low	I_{OL} = 16mA			0.45	V
Capacitance[5]						
C_{IN}	Input	f = 1MHz, T_A = 25°C, V_{CC} = 5.0V, V_{IN} = 0V			6	pF
C_{OUT}	Output	V_{OUT} = 5.0V			12	pF

NOTES:
1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Minimum DC input voltage is −0.5V. During transitions the inputs may undershoot to −2.0V for periods less than 20ns.
3. Input current for $\overline{G}$ input only = −100μA.
4. Test one output at a time for 1 sec max.
5. Capacitance limits are sampled and not 100% tested.

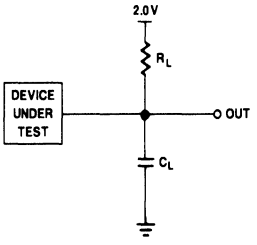
One Time Programmable 64K-Bit CMOS EPROM (8K × 8)

27HC641 O.T.P.

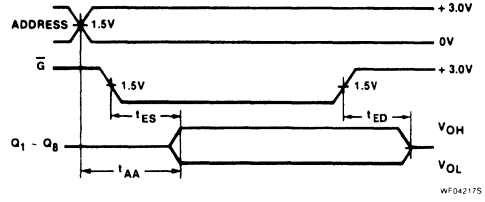
AC ELECTRICAL CHARACTERISTICS C_L = 30pF, R_L = 98Ω, 0°C ≤ T_A ≤ +70°C, 4.5V ≤ V_{CC} ≤ 5.5V

SYMBOL	PARAMETER	TO	FROM	27HC641-45		27HC641-55		UNIT
				Min	Max	Min	Max	
t_{AA}	Address access time	Output	Address		45		55	ns
t_{ES}	Output Enable access time	Output	Output Enable		25		30	ns
t_{ED}	Output disable time	Output	Output Enable		25		30	ns

AC TEST LOAD CIRCUIT



VOLTAGE WAVEFORMS



NOTE:
1. All inputs: $t_r = t_f$ = 5ns (10% to 90%)

27HC641 U.V.

64K-Bit Erasable CMOS EPROM (8K × 8)

Product Specification

Application Specific Products

DESCRIPTION

The 27HC641 is a CMOS, high-speed ultraviolet light erasable electrically programmable Read Only Memory. It is organized as 8192 words of 8 bits and operates from a single 5V ± 10% power supply. All outputs offer 3-State operation and are fully TTL-compatible.

The 27HC641 uses advanced CMOS circuitry which allows operation at bipolar PROM speeds while consuming lower power. The highest degree of protection against latch-up is achieved through epitaxial processing, simplifying the design of electronic equipment which is subject to high noise environments.

The 27HC641 is available in an industry standard 24-pin dual in-line package with the same pinout as most 64K bipolar PROMs. This makes it easy to upgrade systems currently using bipolar PROMs and provide a lower power memory system solution.

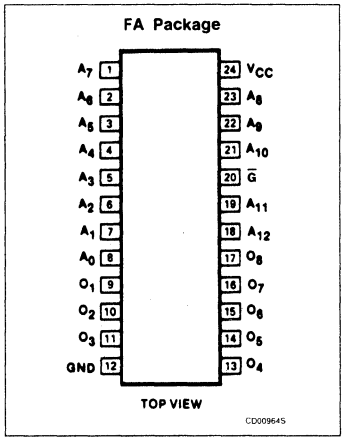
FEATURES

- **Address access time:**
  - **27HC641-55 55ns max**
  - **27HC641-45 45ns max**
  - **27HC641-35 35ns max**
- **Operating I_{CC}: 110mA max**
- **3-State outputs**
- **JEDEC standard 24-pin DIP package**
- **Direct replacement for standard 64K TTL PROMs**
- **Fully TTL-compatible**

APPLICATIONS

- **Prototyping and volume production**
- **High-performance mini- and microcomputers**
- **High-speed program store and look-up tables**

PIN CONFIGURATION



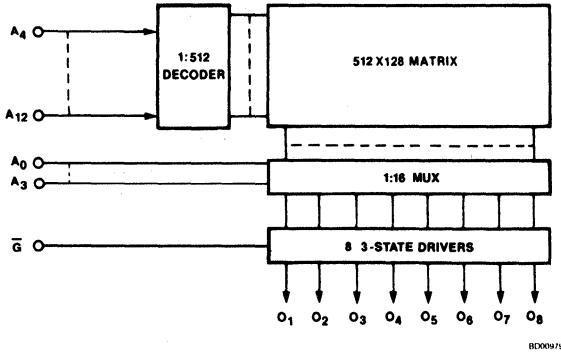
PIN NAMES

$A_0 - A_{12}$	Address inputs
$O_1 - O_8$	Data outputs
$\overline{G}$	Output Enable
V_{CC}	Supply voltage
GND	Ground (V_{SS})

ORDERING INFORMATION

PACKAGE DESCRIPTION	ORDER CODE		
	35ns	45ns	55ns
24-pin ceramic DIP with quartz window 600mil-wide	27HC641-35 FA	27HC641-45 FA	27HC641-55 FA

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
V_I, V_O	Voltage on any pin[2]	−0.5 to V_{CC} + 1V	V
T_A	Temperature under bias	−10 to +85	°C
T_{STG}	Storage temperature range	−65 to +150	°C
V_{PP}	Voltage on Pin 20[2]	−0.5 to 13.5	V

DC OPERATING CONDITIONS $0°C \leq T_A \leq +70°C$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Supply voltage						
V_{CC}		GND = 0V	4.5	5.0	5.5	V
Input voltage						
V_{IH}	High		2.0		V_{CC} + 0.5	V
V_{IL}	Low		−0.1		0.8	V

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +70°C$, $4.5V \leq V_{CC} \leq 5.5V$

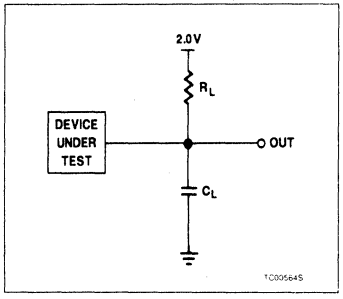
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Input Current						
I_{IH}	High	$V_{IN} = V_{CC}$			10	μA
I_{IL}[3]	Low	$V_{IN} = 0.45V$			10	μA
Output Current						
I_{LO}	Leakage	$V_{OUT} = 0$ to V_{CC}			±10	μA
I_{OS}	Output short-circuit current[4]	$V_{OUT} = 0V$, $\overline{G} = V_{IL}$	−15		−70	mA
Supply Current						
I_{CC}	V_{CC} operating current	$\overline{G} = V_{IH}$, $O_{1-8} = 0mA$, f = 20MHz			110	mA
Input Voltage						
V_{IC}	Input clamp voltage	$I_{IC} = -12mA$			−1.2	V
Output Voltage						
V_{OH}	High	$I_{OH} = -4mA$	2.4			V
V_{OL}	Low	$I_{OL} = 16mA$			0.45	V
Capacitance[5]						
C_{IN}	Input	f = 1MHz, T_A = 25°C, V_{CC} = 5.0V, V_{IN} = 0V			6	pF
C_{OUT}	Output	V_{OUT} = 5.0V			12	pF

NOTES:
1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Minimum DC input voltage is −0.5V. During transitions the inputs may undershoot to −2.0V for periods less than 20ns.
3. Input current for $\overline{G}$ input only = −100μA.
4. Test one output at a time for 1 sec max.
5. Capacitance limits are sampled and not 100% tested.

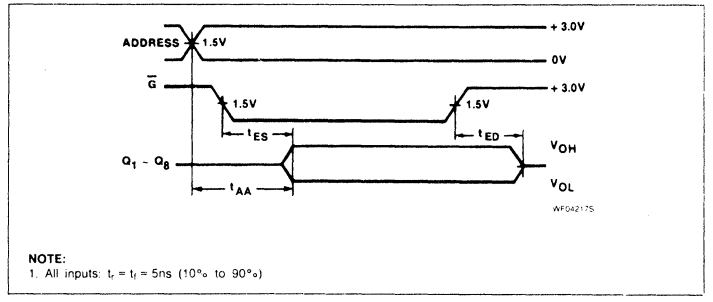
AC ELECTRICAL CHARACTERISTICS $C_L = 30pF$, $R_L = 98\Omega$, $0°C \leq T_A \leq +70°C$, $4.5V \leq V_{CC} \leq 5.5V$

SYMBOL	PARAMETER	TO	FROM	27HC641-35		27HC641-45		27HC641-55		UNIT
				Min	Max	Min	Max	Min	Max	
t_{AA}	Address access time	Output	Address		35		45		55	ns
t_{ES}	Output Enable access time	Output	Output Enable		20		25		30	ns
t_{ED}	Output disable time	Output	Output Enable		20		25		30	ns

AC TEST LOAD CIRCUIT



VOLTAGE WAVEFORMS



NOTE:
1. All inputs: $t_r = t_f = 5ns$ (10% to 90%)

128K-bit CMOS EPROM

page

27HC128 O.T.P. **128K-bit CMOS EPROMs (16K x 8) 45 ns; 55 ns** **223**

27HC128 U.V. **128K-bit erasable CMOS EPROMs (16K x 8) 45 ns; 55 ns** **227**

27HC128 O.T.P.
One Time Programmable 128K (16K × 8) EPROMs

Preliminary Specification

Application Specific Products

DESCRIPTION

The 27HC128 CMOS, O.T.P. EPROM is a high-speed electrically programmable Read Only Memory. It is organized as 16,384 words of 8 bits and operates from a single 5V ±10% power supply. All outputs offer 3-State operation and are fully TTL compatible.

The 27HC128 uses advanced CMOS circuitry which allows operation at bipolar PROM speeds while consuming lower power. The highest degree of protection against latch-up is achieved through epitaxial processing simplifying the design of electronic equipment which is subject to high noise environments.

The 27HC128 is available in industry standard packages with the same pinout as most 128K bipolar PROMs. This makes it easy to upgrade systems currently using bipolar PROMs and provide a lower power memory system solution.

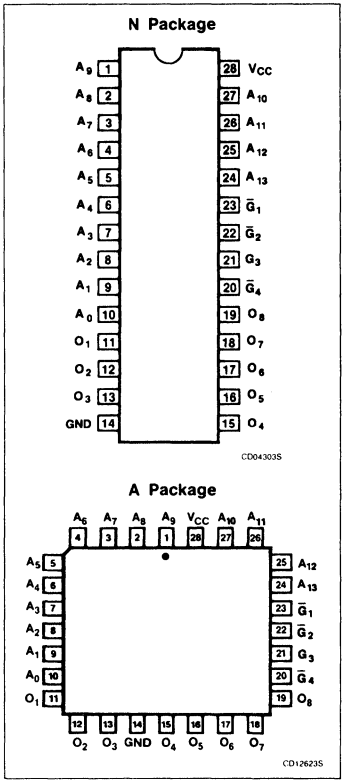
FEATURES

- **Address access time:**
  - **27HC128-55 55ns max**
  - **27HC128-45 45ns max**
- **Operating I_{CC}: 110mA max**
- **3-State outputs**
- **JEDEC standard 28-pin DIP and 28-pin PLCC package**
- **Direct replacement for standard 128K TTL PROMs**
- **Fully TTL compatible**

APPLICATIONS

- **Prototyping and volume production**
- **High-performance mini- and microcomputers**
- **High-speed program store and look-up tables**

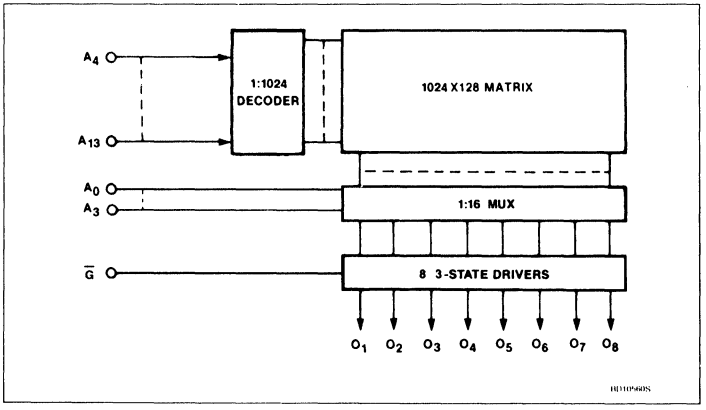
PIN CONFIGURATIONS



ORDERING INFORMATION

DESCRIPTION	ORDER CODE	
	45ns	55ns
28-pin plastic DIP (600mil-wide)	27HC128-45 N	27HC128-55 N
28-pin plastic leaded chip carrier	27HC128-45 A	27HC128-55 A

BLOCK DIAGRAM



PIN NAMES

$A_0 - A_{13}$	Address inputs
$O_1 - O_8$	Data outputs
$\overline{G} - G$	Output Enables
V_{CC}	Supply voltage
GND	Ground (V_{SS})

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
V_I, V_O	Voltage on any pin[2]	−0.5 to V_{CC} + 1V	V
T_A	Temperature under bias	−10 to +85	°C
T_{STG}	Storage temperature range	−65 to +150	°C
V_{PP}	Voltage on $\overline{G}$ pin	−0.5 to 13.5	V

DC OPERATING CONDITIONS $0°C \leq T_A \leq +70°C$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Supply voltage						
V_{CC}		GND = 0V	4.5	5.0	5.5	V
Input voltage						
V_{IH}	High		2.0		V_{CC} + 0.5	V
V_{IL}	Low		−0.1		0.8	V

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +70°C$, $4.5V \leq V_{CC} \leq 5.5V$

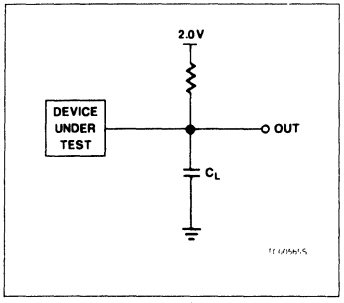
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Input Current						
I_{IH}	High	$V_{IN} = V_{CC}$			10	μA
I_{IL}[3]	Low	$V_{IN} = 0.45V$			10	μA
Output Current						
I_{LO}	Leakage	$V_{OUT} = 0$ to V_{CC}			±10	μA
I_{OS}	Output short-circuit current[4]	$V_{OUT} = 0V$, $\overline{G} = V_{IL}$	−15		−70	mA
Supply Current						
I_{CC}	V_{CC} operating current	$\overline{G} = V_{IH}$, O_{1-8} = 0mA, f = 20MHz			110	mA
Input Voltage						
V_{IC}	Input clamp voltage	$I_{IC} = -12mA$			−1.2	V
Output Voltage						
V_{OH}	High	$I_{OH} = -4mA$	2.4			V
V_{OL}	Low	$I_{OL} = 16mA$			0.45	V
Capacitance[5]						
C_{IN}	Input	f = 1MHz, T_A = 25°C, V_{CC} = 5.0V, V_{IN} = 0V			6	pF
C_{OUT}	Output	V_{OUT} = 5.0V			12	pF

NOTES:
1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Minimum DC input voltage is −0.5V. During transitions the inputs may undershoot to −2.0V for periods less than 20ns.
3. Input current for $\overline{G}$ input only = −100μA.
4. Test one output at a time for 1 sec max.
5. Capacitance limits are sampled and not 100% tested.

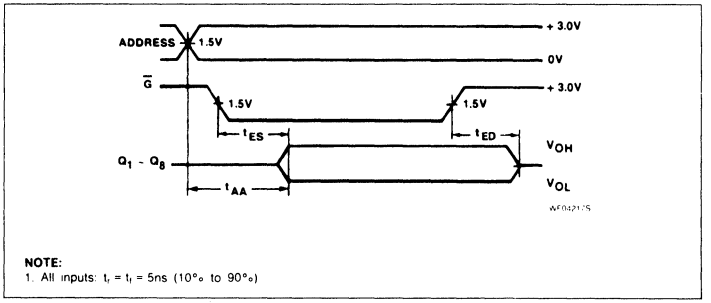
AC ELECTRICAL CHARACTERISTICS C_L = 30pF, R_1 = 98Ω, 0°C < T_A < +70°C, 4.5V < V_{CC} < 5.5V

SYMBOL	PARAMETER	TO	FROM	27HC128-45		27HC128-55		UNIT
				Min	Max	Min	Max	
t_{AA}	Address access time	Output	Address		45		55	ns
t_{ES}	Output Enable access time	Output	Output Enable		25		30	ns
t_{ED}	Output disable time	Output	Output Enable		25		30	ns

AC TEST LOAD CIRCUIT



VOLTAGE WAVEFORMS



NOTE:
1. All inputs: t_r = t_f = 5ns (10% to 90%)

27HC128 U.V.
128K Erasable CMOS (16K × 8) EPROM

Product Specification

Application Specific Products

DESCRIPTION

The 27HC128 is a CMOS, high-speed Ultra-violet light erasable electrically programmable Read Only Memory. It is organized as 16,384 words of 8 bits and operates from a single 5V ± 10% power supply. All outputs offer 3-State operation and are fully TTL-compatible.

The 27HC128 uses advanced CMOS circuitry which allows operation at bipolar PROM speeds while consuming lower power. The highest degree of protection against latch-up is achieved through epitaxial processing, simplifying the design of electronic equipment which is subject to high noise environments.

The 27HC128 is available in an industry standard 24-pin dual-in-line package with the same pin out as most 128K bipolar PROMs. This makes it easy to upgrade systems currently using bipolar PROMs and provide a lower power memory system solution.

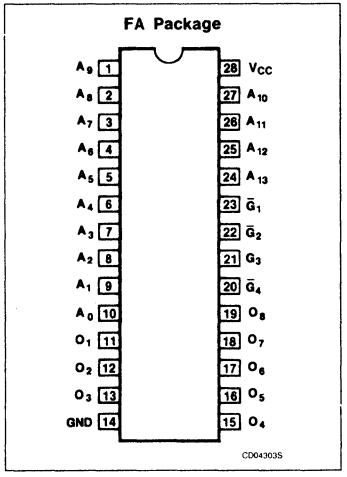
FEATURES

- **Address access time:**
  - **27HC128-55 55ns max**
  - **27HC128-45 45ns max**
- **Operating I_{CC}: 110mA max**
- **3-State outputs**
- **JEDEC standard 24-pin DIP package**
- **Direct replacement for standard 128K TTL PROMs**
- **Fully TTL compatible**

APPLICATIONS

- **Prototyping and volume production**
- **High-performance mini- and microcomputers**
- **High-speed program store and look-up tables**

PIN CONFIGURATION



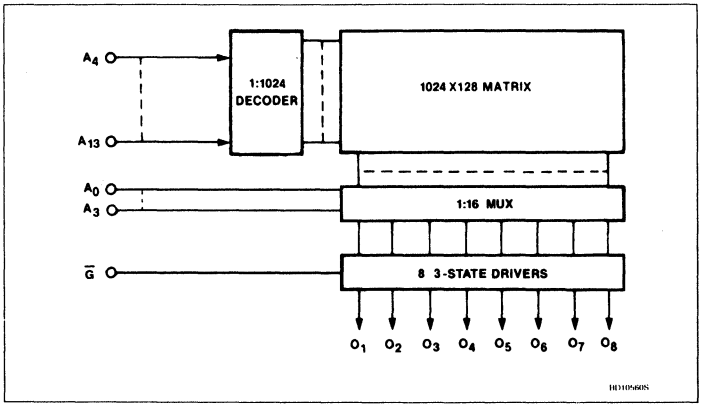
PIN NAMES

$A_0 - A_{13}$	Address inputs
$O_1 - O_8$	Data outputs
$\overline{G}$	Output Enable
V_{CC}	Supply voltage
GND	Ground (V_{SS})

ORDERING INFORMATION

PACKAGE DESCRIPTION	ORDER CODE	
	45ns	55ns
28-pin ceramic DIP with quartz window 600mil-wide	27HC128-45 FA	27HC128-55 FA

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
V_I, V_O	Voltage on any pin[2]	−0.5 to V_{CC} + 1V	V
T_A	Temperature under bias	−10 to +85	°C
T_{STG}	Storage temperature range	−65 to +150	°C
V_{PP}	Voltage on Pin 20[2]	−0.5 to 13.5	V

DC OPERATING CONDITIONS $0°C \leq T_A \leq +70°C$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Supply voltage						
V_{CC}		GND = 0V	4.5	5.0	5.5	V
Input voltage						
V_{IH}	High		2.0		V_{CC} + 0.5	V
V_{IL}	Low		−0.1		0.8	V

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +70°C$, $4.5V \leq V_{CC} \leq 5.5V$

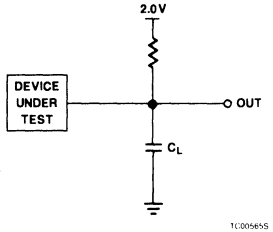
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Input Current						
I_{IH}	High	$V_{IN} = V_{CC}$			10	μA
I_{IL}[3]	Low	V_{IN} = 0.45V			10	μA
Output Current						
I_{LO}	Leakage	V_{OUT} = 0 to V_{CC}			± 10	μA
I_{OS}	Output short-circuit current[4]	V_{OUT} = 0V, $\overline{G} = V_{IL}$	−15		−70	mA
Supply Current						
I_{CC}	V_{CC} operating current	$\overline{G} = V_{IH}$, O_{1-8} = 0mA, f = 20MHz			110	mA
Input Voltage						
V_{IC}	Input clamp voltage	I_{IC} = −12mA			−1.2	V
Output Voltage						
V_{OH}	High	I_{OH} = −4mA	2.4			V
V_{OL}	Low	I_{OL} = 16mA			0.45	V
Capacitance[5]						
C_{IN}	Input	f = 1MHz, T_A = 25°C, V_{CC} = 5.0V, V_{IN} = 0V			6	pF
C_{OUT}	Output	V_{OUT} = 5.0V			12	pF

NOTES:
1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Minimum DC input voltage is −0.5V. During transitions the inputs may undershoot to −2.0V for periods less than 20ns.
3. Input current for $\overline{G}$ input only = −100μA.
4. Test one output at a time for 1 sec max.
5. Capacitance limits are sampled and not 100% tested.

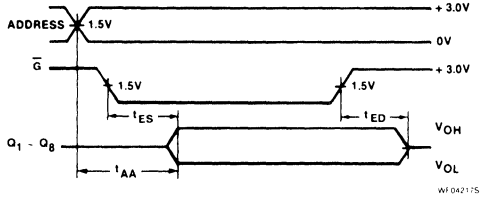
AC ELECTRICAL CHARACTERISTICS $C_L = 30pF$, $R_L = 98\Omega$, $0°C \leq T_A \leq +70°C$, $4.5V \leq V_{CC} \leq 5.5V$

SYMBOL	PARAMETER	TO	FROM	27HC128-45		27HC128-55		UNIT
				Min	Max	Min	Max	
t_{AA}	Address access time	Output	Address		45		55	ns
t_{ES}	Output Enable access time	Output	Output Enable		25		30	ns
t_{ED}	Output disable time	Output	Output Enable		25		30	ns

AC TEST LOAD CIRCUIT



VOLTAGE WAVEFORMS



NOTE:
1. All inputs: $t_r = t_f = 5ns$ (10% to 90%)

256K-bit CMOS EPROM

		page
27C256-IND	256K-bit EPROMs (32K x 8) 150 ns; 200 ns	233
27C256 O.T.P.	256K-bit EPROM (32K x 8) 120 ns	237
27C256 O.T.P.	256K-bit EPROMs (32K x 8) 150 ns; 170 ns	241
27C256 O.T.P.	256K-bit EPROM (32K x 8) 200 ns	245
27C256 U.V.	256K-bit erasable EPROM (32K x 8) 120 ns	249
27C256 U.V.	256K-bit erasable EPROMs (32K x 8) 150 ns; 170 ns	253
27C256 U.V.	256K-bit erasable EPROM (32K x 8) 200 ns	257

27C256–IND
256K (32K × 8) EPROMs
Industrial Temperature Range

Product Specification

Application Specific Products

DESCRIPTION

Signetics 27C256 CMOS EPROM is a 256K-bit 5V only memory organized as 131,072 words of 8 bits each. It employs advanced CMOS circuitry for systems requiring low power, high-performance speeds, and immunity to noise. The 27C256 has a non-multiplexed addressing interface and is plug-compatible with the industry standard 27256.

The 27C256 is specified to operate over the industrial temperature range of −40°C to +85°C with no degradation in performance.

The 27C256 is available in both the windowed Ceramic DIP, the plastic DIP and the PLCC Packages. This device can be programmed with standard EPROM programmers.

FEATURES

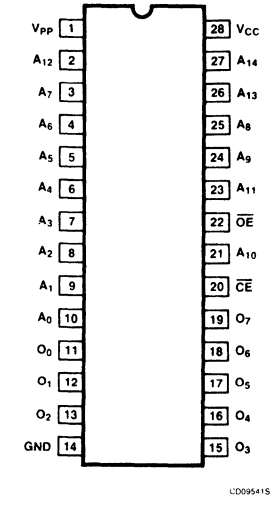
- **Low power consumption**
  - **100μA maximum CMOS standby current**
- **Quick pulse programming algorithm for high-speed production programming (4 second typical programming times)**
- **High-performance speeds**
  - **27C256I15: 150ns maximum access time**
  - **27C256I20: 200ns maximum access time**
- **Noise immunity features**
  - **± 10% V_{CC} tolerance**
  - **Maximum latch-up immunity through epitaxial processing**

PIN DESCRIPTION

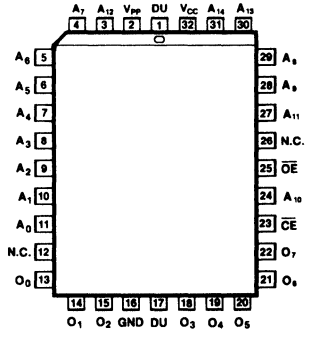
$A_0 - A_{14}$	Addresses
$O_0 - O_7$	Outputs
$\overline{OE}$	Output Enable
$\overline{CE}$	Chip Enable
GND	Ground
V_{PP}	Program voltage
V_{CC}	Power supply
N.C.	No Connection
D.U.	Don't Use

PIN CONFIGURATIONS

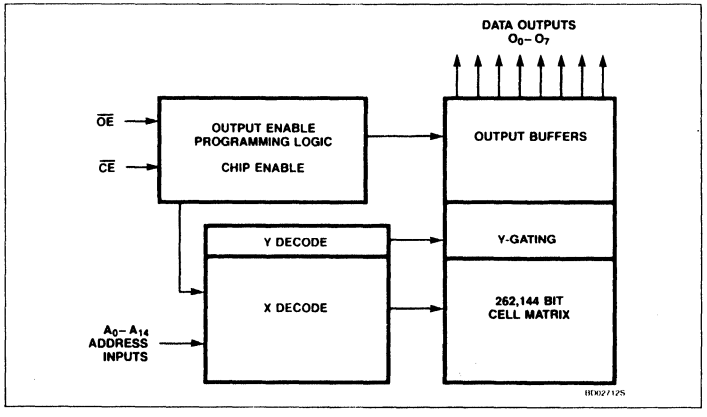
FA and N Packages



A Package



BLOCK DIAGRAM



READ MODE: 27C256

The 27C256 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins. Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been Low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

STANDBY MODE

The 27C256 has a standby mode which reduces the maximum V_{CC} current to 100μA. It is placed in the Standby mode when $\overline{CE}$ is in the High state. When in the Standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
28-pin CERDIP with quartz window (600mil-wide)	27C256I15 FA 27C256I20 FA
28-pin Plastic Dual in-line (600mil-wide)	27C256I15 N 27C256I20 N
32-pin Plastic Leaded Chip Carrier (450 × 550mil)	27C256I15 A 27C256I20 A

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
T_A	Temperature under bias	−55 to +125	°C
T_{STG}	Storage temperature range	−65 to +150	°C
V_I, V_O	Voltage inputs and outputs	−2.0 to (V_{CC} + 1)	V
V_H	Voltage on A_9[2] (During intelligent identifier interrogation)	−2.0 to +13.5	V
V_{PP}	Voltage on V_{PP}[2] (During programming)	−2.0 to +14.0	V
V_{CC}	Supply voltage[2]	−2.0 to +7.0	V

NOTE:

1. Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. All voltages are with respect to network ground.

DEVICE OPERATION[2]

MODE	$\overline{CE}$	$\overline{OE}$[10]	V_{PP}[8]	OUTPUTS
Read	V_{IL}	V_{IL}	V_{CC}	D_{OUT}
Output disable	V_{IL}	V_{IH}	V_{CC}	Hi-Z
Standby	V_{IH}	X	V_{CC}	Hi-Z

Notes on following page.

DC ELECTRICAL CHARACTERISTICS $-40°C \leq T_A \leq +85°C$, $+4.5V \leq V_{CC} \leq +5.5V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[3]	Max	
Input current						
I_{IH}	Leakage	$V_{IN} = 5.5V = V_{CC}$		0.01	1.0	μA
I_{IL}	Low	$V_{IL} = 0.45V$		0.01	1.0	μA
I_{PP}	V_{PP} read	$V_{PP} = V_{CC}$			100	μA
Output current						
I_{LO}	Leakage	$\overline{OE}$ or $\overline{CE} = V_{IH}$ $V_{OUT} = 5.5V = V_{CC}$			1.0	μA
		$V_{OUT} = 0V = GND$			1.0	μA
I_{OS}	Short circuit[7, 9]	$V_{OUT} = 0V$			100	mA
Supply current						
I_{CC} TTL	Operating (TTL inputs)[4]	$\overline{CE} = \overline{OE} = V_{IL}$, f = 6.7MHz $V_{PP} = V_{CC}$ $O_{0-7} = 0mA$			20	mA
I_{SB} TTL	Standby (TTL inputs)[4]	$\overline{CE} = V_{IH}$			1.0	μA
I_{SB} CMOS	Standby (CMOS inputs)[5, 6]	$\overline{CE} = V_{IH}$			100	μA
Input voltage[2]						
V_{IL}	Low (TTL)	$V_{PP} = V_{CC}$	-0.5		0.8	V
V_{IL}	Low (CMOS)	$V_{PP} = V_{CC}$	-0.2		0.2	V
V_{IH}	High (TTL)	$V_{PP} = V_{CC}$	2.0		$V_{CC} + 0.5$	V
V_{IH}	High (CMOS)	$V_{PP} = V_{CC}$	$V_{CC} - 0.2$		$V_{CC} + 0.2$	V
V_{PP}	Read[8]	(Operating)	$V_{CC} - 0.7$		V_{CC}	V
Output voltage[2]						
V_{OL}	Low	$I_{OL} = 2.1mA$			0.45	V
V_{OH}	High	$I_{OH} = -2.5mA$	3.5			V
Capacitance[9] $T_A = 25°C$						
C_{IN}	Address and control	$V_{CC} = 5.0V$ f = 1.0MHz $V_{IN} = 0V$ $V_{OUT} = 0V$			6	pF
C_{OUT}	Outputs				12	pF

NOTES:

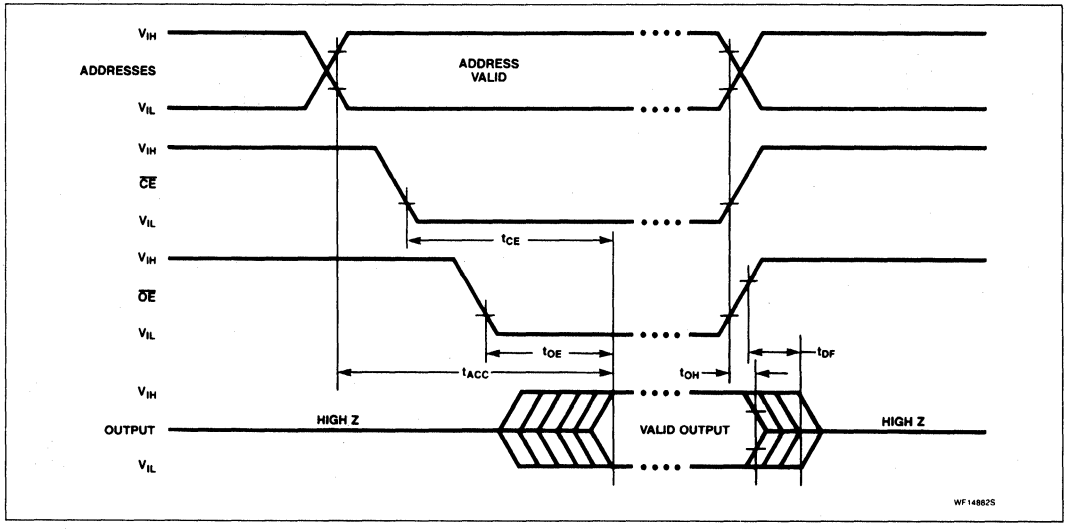
1. Minimum DC input voltage is −0.5V. During transitions the inputs may undershoot to −2.0V for periods less than 20ns.
2. All voltages are with respect to network ground.
3. Typical limits are at $V_{CC} = 5V$, $T_A = 25°C$.
4. TTL inputs: Specification V_{IL}, V_{IH} levels.
   CMOS inputs: GND ±0.2V to V_{CC} ±0.2V.
5. $\overline{CE}$ is V_{CC} ±0.2V. All other inputs can have any value within specification.
6. Maximum active power usage is the sum of $I_{PP} + I_{CC}$ and is measured at a frequency of 5MHz.
7. Test one output at a time, duration should not exceed 1 second.
8. V_{PP} may be one diode voltage drop below V_{CC}, and can be connected directly to V_{CC}.
9. Guaranteed by design, not 100% tested.
10. X can be V_{IH} or V_{IL}.

AC ELECTRICAL CHARACTERISTICS $-40°C \leq T_A \leq +85°C$, $+4.5V \leq V_{CC} \leq +5.5V$, $R_L = 660\Omega$, $C_L = 100pF$

SYMBOL	TO	FROM	27C256I15		27C256I20		UNIT
			Min	Max	Min	Max	
Access time[1]							
t_{ACC}	Output	Address		150		200	ns
t_{CE}	Output	$\overline{CE}$		150		200	ns
t_{OE}[3]	Output	$\overline{OE}$		65		75	ns
Disable time[2]							
t_{DF}[4]	Output Hi-Z	$\overline{OE}$ or $\overline{CE}$		45		55	ns
t_{OH}	Output hold	Address, $\overline{CE}$ or $\overline{OE}$	0		0		ns

NOTES:
1. AC characteristics are tested at $V_{IH} = 2.4V$ and $V_{IL} = 0.45V$. Timing measurements made at $V_{OL} = 0.8V$ and $V_{OH} = 2.0V$.
2. Guaranteed by design, not 100% tested.
3. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.
4. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

AC VOLTAGE WAVEFORMS



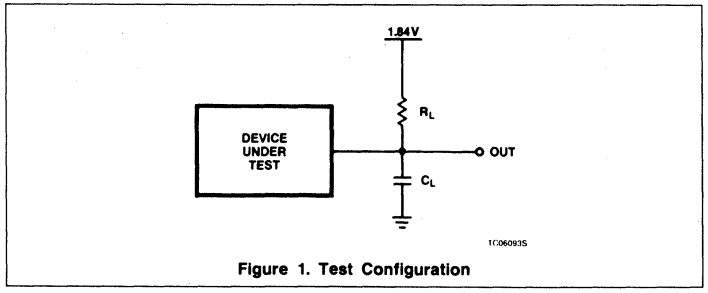


Figure 1. Test Configuration

27C256 O.T.P.
One Time Programmable 256K (32K × 8) EPROMs

Product Specification

Application Specific Products

DESCRIPTION

Signetics' 27C256 CMOS O.T.P. EPROM is a 256K-bit 5V only memory organized as 32,768 words of 8 bits each. It employs advanced CMOS circuitry for systems requiring low power, high-performance speeds, and immunity to noise. The 27C256 has a non-multiplexed addressing interface and is plug-compatible with the industry standard 27256.

The 27C256 O.T.P. is offered in plastic DIP and plastic leaded chip carrier (PLCC) packages. Plastic EPROMs provide optimum cost effectiveness in production environments. Quick-pulse programming is employed on plastic devices which may speed up programming by as much as one hundred times.

FEATURES

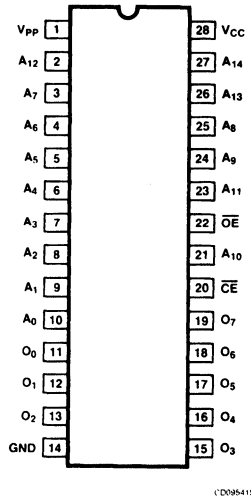
- **Low power consumption**
  - **100μA maximum CMOS standby current**
- **Quick-pulse programming algorithm for high-speed production programming**
- **High-performance speeds**
  - **27C256-12: 120ns maximum access time**
- **Noise immunity features**
  - **± 10% V_{CC} tolerance**
  - **Maximum latch-up immunity through epitaxial processing**

PIN DESCRIPTION

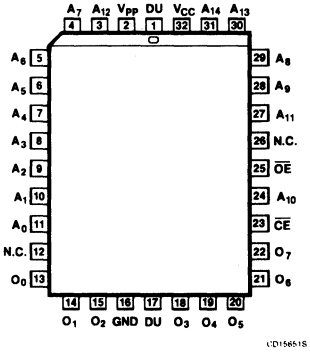
$A_0 - A_{14}$	Addresses
$O_0 - O_7$	Outputs
$\overline{OE}$	Output enable
$\overline{CE}$	Chip enable
N.C.	No connection
GND	Ground
V_{PP}	Program voltage
V_{CC}	Power supply
DU	Don't use

PIN CONFIGURATIONS

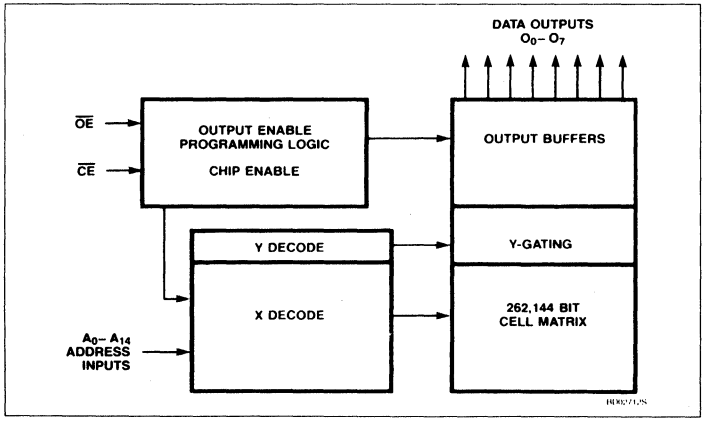
N Package



A Package



BLOCK DIAGRAM



READ MODE: 27C256

The 27C256 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins. Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

STANDBY MODE

The 27C256 has a standby mode which reduces the maximum V_{CC} current to 100μA. It is placed in the Standby mode when $\overline{CE}$ is in the High state. When in the Standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
28-pin plastic DIP (600mil-wide)	27C256-12 N
32-pin plastic leaded chip carrier (450mil × 550mil)	27C256-12 A

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
T_A	Temperature under bias	−10 to +80	°C
T_{STG}	Storage temperature	−65 to +125	°C
V_I, V_O	Voltage inputs and outputs	−2.0 to (V_{CC} + 1)	V
V_H	Voltage on A_9[2] (During intelligent identifier interrogation)	−2.0 to +13.5	V
V_{PP}	Voltage on V_{PP}[2] (During programming)	−2.0 to +14.0	V
V_{CC}	Supply voltage[2]	−2.0 to +7.0	V

NOTE:

1. Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. All voltages are with respect to network ground.

DEVICE OPERATION[2]

MODE	$\overline{CE}$	$\overline{OE}$[10]	V_{PP}[8]	OUTPUTS
Read	V_{IL}	V_{IL}	V_{CC}	D_{OUT}
Output disable	V_{IL}	V_{IH}	V_{CC}	Hi-Z
Standby	V_{IH}	X	V_{CC}	Hi-Z

Notes on following page.

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +70°C$, $+4.5V \leq V_{CC} \leq +5.5V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[3]	Max	
Input current						
I_{IH}	Leakage	$V_{IN} = 5.5V = V_{CC}$		0.01	1.0	µA
I_{IL}	Low	$V_{IL} = 0.45V$		0.01	-1.0	µA
I_{PP}	V_{PP} read	$V_{PP} = V_{CC}$			100	µA
Output current						
I_{LO}	Leakage	$\overline{OE}$ or $\overline{CE} = V_{IH}$ $V_{OUT} = 5.5V = V_{CC}$			1.0	µA
		$V_{OUT} = 0V = GND$			-1.0	µA
I_{OS}	Short circuit[7, 9]	$V_{OUT} = 0V$			-100	mA
Supply current						
I_{CC} TTL	Operating (TTL inputs)[4]	$\overline{CE} = \overline{OE} = V_{IL}$, f = 8.0MHz $V_{PP} = V_{CC}$ $O_{0-7} = 0mA$			20	mA
I_{SB} TTL	Standby (TTL inputs)[4]	$\overline{CE} = V_{IH}$			1.0	µA
I_{SB} CMOS	Standby (CMOS inputs)[5, 6]	$\overline{CE} = V_{IH}$			100	µA
Input voltage[2]						
V_{IL}	Low (TTL)	$V_{PP} = V_{CC}$	-0.5		0.8	V
V_{IL}	Low (CMOS)	$V_{PP} = V_{CC}$	-0.2		0.2	V
V_{IH}	High (TTL)	$V_{PP} = V_{CC}$	2.0		$V_{CC} + 0.5$	V
V_{IH}	High (CMOS)	$V_{PP} = V_{CC}$	$V_{CC} - 0.2$		$V_{CC} + 0.2$	V
V_{PP}	Read[8]	(Operating)	$V_{CC} - 0.7$		V_{CC}	V
Output voltage[2]						
V_{OL}	Low	$I_{OL} = 2.1mA$			0.45	V
V_{OH}	High	$I_{OH} = -2.5mA$	3.5			V
Capacitance[9] $T_A = 25°C$						
C_{IN}	Address and control	$V_{CC} = 5.0V$ f = 1.0MHz			6	pF
C_{OUT}	Outputs	$V_{IN} = 0V$ $V_{OUT} = 0V$			12	pF

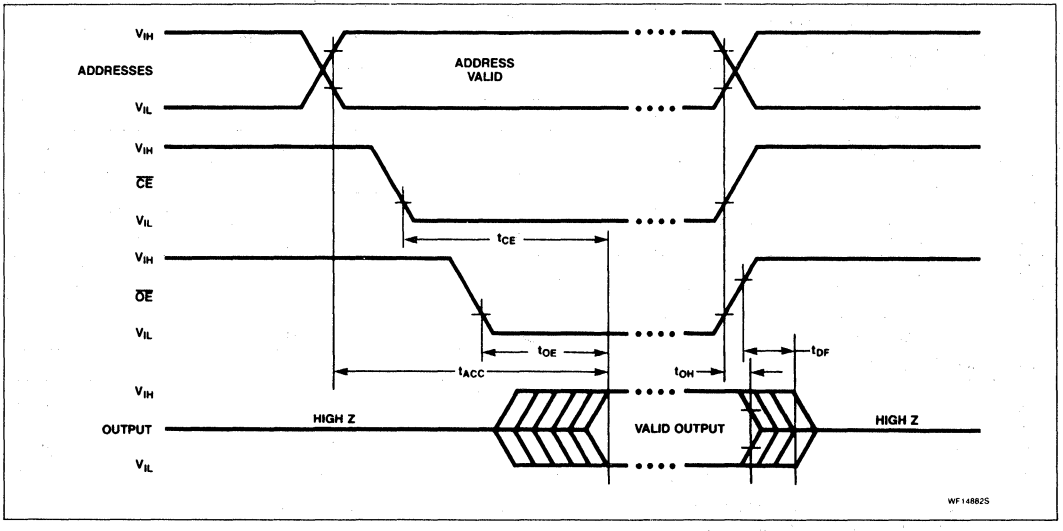
NOTES:
1. Minimum DC input voltage is -0.5V. During transitions the inputs may undershoot to -2.0V for periods less than 20ns.
2. All voltages are with respect to network ground.
3. Typical limits are at $V_{CC} = 5V$, $T_A = 25°C$.
4. TTL inputs: Spec V_{IL}, V_{IH} levels.
   CMOS inputs: GND ± 0.2V to V_{CC} ± 0.2V.
5. $\overline{CE}$ is V_{CC} ± 0.2V. All other inputs can have any value within spec.
6. Maximum active power usage is the sum of $I_{PP} + I_{CC}$ and is measured at a frequency of 5MHz..
7. Test one output at a time, duration should not exceed 1 second.
8. V_{PP} may be one diode voltage drop below V_{CC}, and can be connected directly to V_{CC}.
9. Guaranteed by design, not 100% tested.
10. X can be V_{IH} or V_{IL}.

AC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +70°C$, $+4.5V \leq V_{CC} \leq +5.5V$, $R_L = 660\Omega$, $C_L = 100pF$

SYMBOL	TO	FROM	27C256 – 12		UNIT
			Min	Max	
Access time[1]					
t_{ACC}	Output	Address		120	ns
t_{CE}	Output	$\overline{CE}$		120	ns
t_{OE}[3]	Output	$\overline{OE}$		60	ns
Disable time[2]					
t_{DF}[4]	Output High-Z	$\overline{OE}$ or $\overline{CE}$		30	ns
t_{OH}	Output hold	Address, $\overline{CE}$ or $\overline{OE}$	0		ns

NOTES:
1. AC characteristics are tested at $V_{IH} = 2.4V$ and $V_{IL} = 0.45V$. Timing measurements made at $V_{OL} = 0.8V$ and $V_{OH} = 2.0V$.
2. Guaranteed by design, not 100% tested.
3. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.
4. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

AC VOLTAGE WAVEFORMS



AC TESTING LOAD CIRCUIT

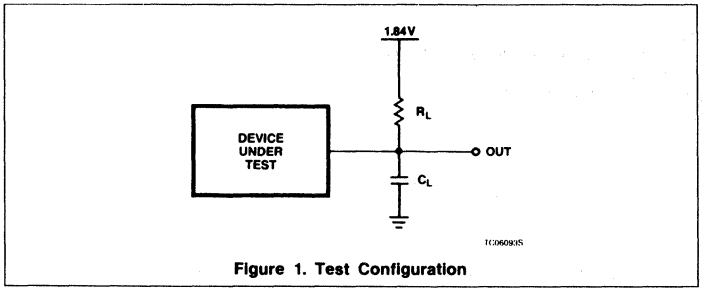


Figure 1. Test Configuration

27C256 O.T.P.
One Time Programmable 256K (32K × 8) EPROMs

Product Specification

Application Specific Products

DESCRIPTION

Signetics 27C256 CMOS O.T.P. EPROM is a 256K-bit 5V only memory organized as 32,768 words of 8 bits each. It employs advanced CMOS circuitry for systems requiring low power, high-performance speeds, and immunity to noise. The 27C256 has a non-multiplexed addressing interface and is plug-compatible with the industry standard 27256.

The 27C256 O.T.P. is offered in plastic DIP and plastic leaded chip carrier (PLCC) packages. Plastic EPROMs provide optimum cost effectiveness in production environments. Quick-pulse programming is employed on plastic devices which may speed up programming by as much as one hundred times.

FEATURES

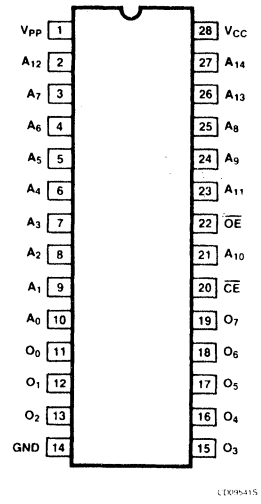
- **Low power consumption**
  - **100μA maximum CMOS standby current**
- **Quick-pulse programming algorithm for high-speed production programming**
- **High-performance speeds**
  - **27C256-15: 150ns maximum access time**
  - **27C256-17: 170ns maximum access time**
- **Noise immunity features**
  - **± 10% V_{CC} tolerance**
  - **Maximum latch-up immunity through epitaxial processing**

PIN DESCRIPTION

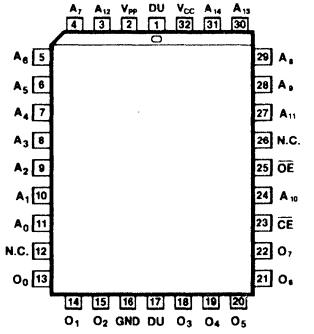
$A_0 - A_{14}$	Addresses
$O_0 - O_7$	Outputs
$\overline{OE}$	Output enable
$\overline{CE}$	Chip enable
N.C.	No connection
GND	Ground
V_{PP}	Program voltage
V_{CC}	Power supply
DU	Don't use

PIN CONFIGURATIONS

N Package

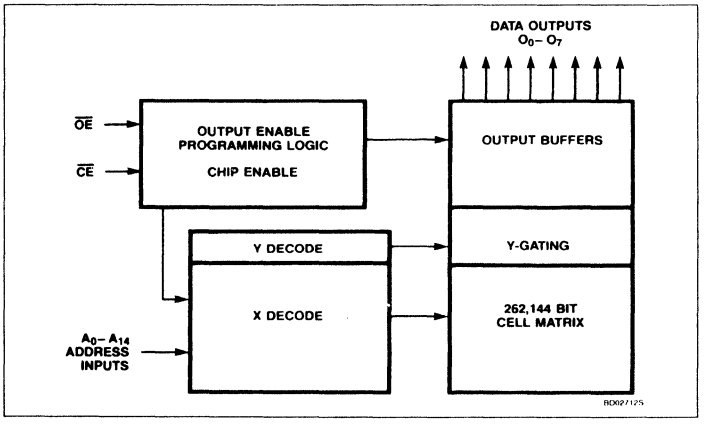


A Package



TOP VIEW

BLOCK DIAGRAM



READ MODE: 27C256

The 27C256 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins. Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

STANDBY MODE

The 27C256 has a standby mode which reduces the maximum V_{CC} current to 100μA. It is placed in the Standby mode when $\overline{CE}$ is in the High state. When in the Standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
28-pin plastic dual in-line (600mil-wide)	27C256-15 N 27C256-17 N
32-pin plastic leaded chip carrier (450mil × 550mil)	27C256-15 A 27C256-17 A

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
T_A	Temperature under bias	−10 to +80	°C
T_{STG}	Storage temperature range	−65 to +125	°C
V_I, V_O	Voltage inputs and outputs	−2.0 to (V_{CC} + 1)	V
V_H	Voltage on A_9[2] (During intelligent identifier interrogation)	−2.0 to +13.5	V
V_{PP}	Voltage on V_{PP}[2] (During programming)	−2.0 to +14.0	V
V_{CC}	Supply voltage[2]	−2.0 to +7.0	V

NOTE:

1. Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. All voltages are with respect to network ground.

DEVICE OPERATION[2]

MODE	$\overline{CE}$	$\overline{OE}$[10]	V_{PP}[8]	OUTPUTS
Read	V_{IL}	V_{IL}	V_{CC}	D_{OUT}
Output disable	V_{IL}	V_{IH}	V_{CC}	Hi-Z
Standby	V_{IH}	X	V_{CC}	Hi-Z

Notes on following page.

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +70°C$, $+4.5V \leq V_{CC} \leq +5.5V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[3]	Max	
Input current						
I_{IH}	Leakage	$V_{IN} = 5.5V = V_{CC}$		0.01	1.0	μA
I_{IL}	Low	$V_{IL} = 0.45V$		0.01	−1.0	μA
I_{PP}	V_{PP} read	$V_{PP} = V_{CC}$			100	μA
Output current						
I_{LO}	Leakage	$\overline{OE}$ or $\overline{CE} = V_{IH}$ $V_{OUT} = 5.5V = V_{CC}$			1.0	μA
		$V_{OUT} = 0V = GND$			−1.0	μA
I_{OS}	Short circuit[7, 9]	$V_{OUT} = 0V$			−100	mA
Supply current						
I_{CC} TTL	Operating (TTL inputs)[4]	$\overline{CE} = \overline{OE} = V_{IL}$, f = 6.7MHz $V_{PP} = V_{CC}$ $O_{0-7} = 0mA$			20	mA
I_{SB} TTL	Standby (TTL inputs)[4]	$\overline{CE} = V_{IH}$			1.0	μA
I_{SB} CMOS	Standby (CMOS inputs)[5, 6]	$\overline{CE} = V_{IH}$			100	μA
Input voltage[2]						
V_{IL}	Low (TTL)	$V_{PP} = V_{CC}$	−0.5		0.8	V
V_{IL}	Low (CMOS)	$V_{PP} = V_{CC}$	−0.2		0.2	V
V_{IH}	High (TTL)	$V_{PP} = V_{CC}$	2.0		$V_{CC} + 0.5$	V
V_{IH}	High (CMOS)	$V_{PP} = V_{CC}$	$V_{CC} - 0.2$		$V_{CC} + 0.2$	V
V_{PP}	Read[8]	(Operating)	$V_{CC} - 0.7$		V_{CC}	V
Output voltage[2]						
V_{OL}	Low	$I_{OL} = 2.1mA$			0.45	V
V_{OH}	High	$I_{OH} = -2.5mA$	3.5			V
Capacitance[9] $T_A = 25°C$						
C_{IN}	Address and control	$V_{CC} = 5.0V$ f = 1.0MHz $V_{IN} = 0V$ $V_{OUT} = 0V$			6	pF
C_{OUT}	Outputs				12	pF

NOTES:

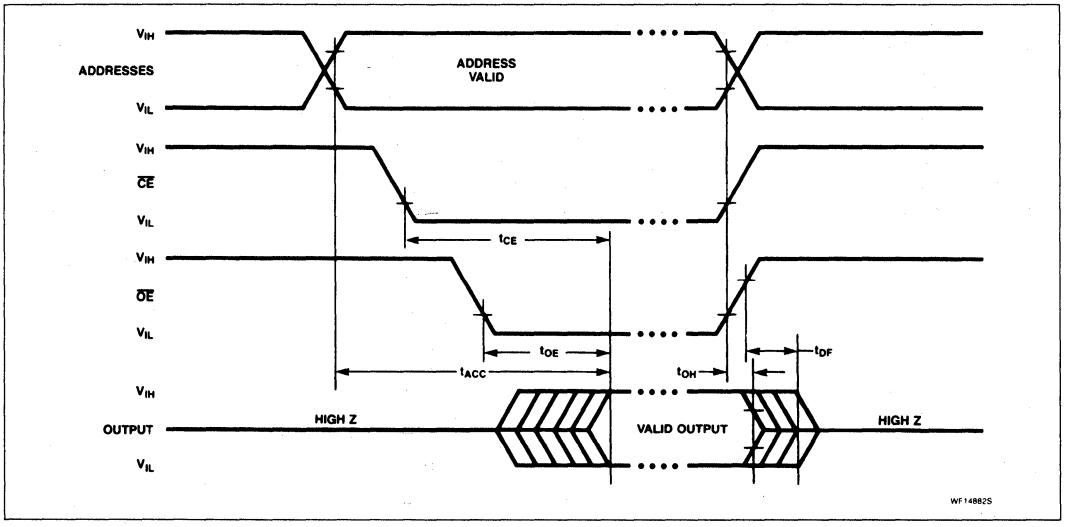
1. Minimum DC input voltage is −0.5V. During transitions the inputs may undershoot to −2.0V for periods less than 20ns.
2. All voltages are with respect to network ground.
3. Typical limits are at $V_{CC} = 5V$, $T_A = 25°C$.
4. TTL inputs: Spec V_{IL}, V_{IH} levels.
   CMOS inputs: GND ±0.2V to V_{CC} ±0.2V.
5. $\overline{CE}$ is V_{CC} ±0.2V. All other inputs can have any value within spec.
6. Maximum active power usage is the sum of $I_{PP} + I_{CC}$ and is measured at a frequency of 5MHz.
7. Test one output at a time, duration should not exceed 1 second.
8. V_{PP} may be one diode voltage drop below V_{CC}, and can be connected directly to V_{CC}.
9. Guaranteed by design, not 100% tested.
10. X can be V_{IH} or V_{IL}.

AC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +70°C$, $+4.5V \leq V_{CC} \leq +5.5V$, $R_L = 660\Omega$, $C_L = 100pF$

SYMBOL	TO	FROM	27C256 - 15		27C256 - 17		UNIT
			Min	Max	Min	Max	
Access time[1]							
t_{ACC}	Output	Address		150		170	ns
t_{CE}	Output	$\overline{CE}$		150		170	ns
t_{OE}[3]	Output	$\overline{OE}$		65		70	ns
Disable time[2]							
t_{DF}[4]	Output Hi-Z	$\overline{OE}$ or $\overline{CE}$		45		55	ns
t_{OH}	Output hold	Address, $\overline{CE}$ or $\overline{OE}$	0		0		ns

NOTES:
1. AC characteristics are tested at $V_{IH} = 2.4V$ and $V_{IL} = 0.45V$. Timing measurements made at $V_{OL} = 0.8V$ and $V_{OH} = 2.0V$.
2. Guaranteed by design, not 100% tested.
3. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.
4. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

AC VOLTAGE WAVEFORMS



AC TESTING LOAD CIRCUIT

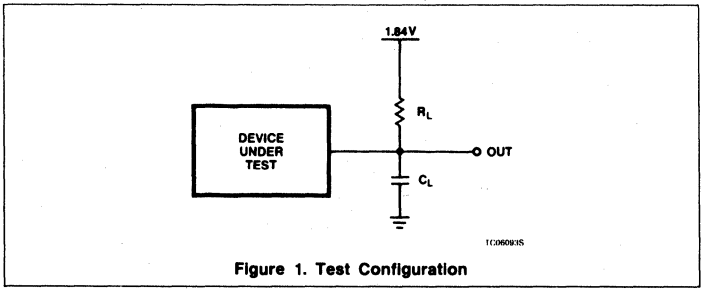


Figure 1. Test Configuration

27C256 O.T.P.
One Time Programmable 256K (32K × 8) EPROMs

Product Specification

Application Specific Products

DESCRIPTION

Signetics' 27C256 CMOS O.T.P. EPROM is a 256K-bit 5V only memory organized as 32,768 words of 8 bits each. It employs advanced CMOS circuitry for systems requiring low power, high-performance speeds, and immunity to noise. The 27C256 has a non-multiplexed addressing interface and is plug-compatible with the industry standard 27256.

The 27C256 O.T.P. is offered in plastic DIP and plastic leaded chip carrier (PLCC) packages. Plastic EPROMs provide optimum cost effectiveness in production environments. Quick-pulse programming is employed on plastic devices which may speed up programming by as much as one hundred times.

FEATURES

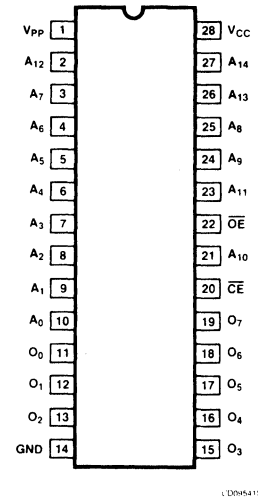
- **Low power consumption**
  - **100μA maximum CMOS standby current**
- **High-performance speeds**
  - **27C256-20: 200ns maximum access time**
- **Noise immunity features**
  - **± 10% V_{CC} tolerance**
  - **Maximum latch-up immunity through Epitaxial processing**
- **Quick-pulse programming algorithm**

PIN DESCRIPTION

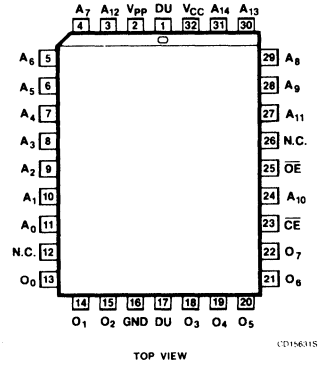
$A_0 - A_{14}$	Addresses
$O_0 - O_7$	Outputs
$\overline{OE}$	Output enable
$\overline{CE}$	Chip enable
N.C.	No connection
GND	Ground
V_{PP}	Program voltage
V_{CC}	Power supply
DU	Don't use

PIN CONFIGURATIONS

N Package

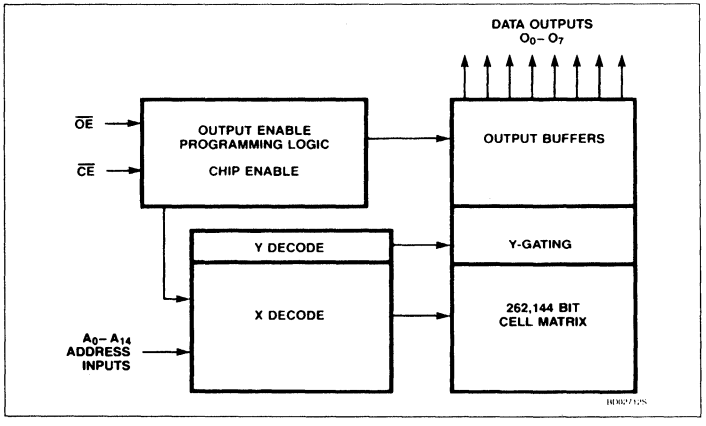


A Package



TOP VIEW

BLOCK DIAGRAM



READ MODE: 27C256

The 27C256 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins. Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

STANDBY MODE

The 27C256 has a standby mode which reduces the maximum V_{CC} current to 100μA. It is placed in the Standby mode when $\overline{CE}$ is in the High state. When in the Standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
28-pin plastic DIP 600mil-wide	27C256-20 N
32-pin plastic leaded chip carrier 450mil × 550mil	27C256-20 A

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
T_A	Temperature under bias	−10 to +80	°C
T_{STG}	Storage temperature	−65 to +125	°C
V_I, V_O	Voltage inputs and outputs	−2.0 to (V_{CC} + 1)	V
V_H	Voltage on A_9[2] (During intelligent identifier interrogation)	−2.0 to +13.5	V
V_{PP}	Voltage on V_{PP}[2] (During programming)	−2.0 to +14.0	V
V_{CC}	Supply voltage[2]	−2.0 to +7.0	V

NOTE:

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. All voltages are with respect to network ground.

DEVICE OPERATION[2]

MODE	$\overline{CE}$	$\overline{OE}$[10]	V_{PP}[8]	OUTPUTS
Read	V_{IL}	V_{IL}	V_{CC}	D_{OUT}
Output disable	V_{IL}	V_{IH}	V_{CC}	Hi-Z
Standby	V_{IH}	X	V_{CC}	Hi-Z

Notes on following page.

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +70°C$, $+4.5V \leq V_{CC} \leq +5.5V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[3]	Max	
Input current						
I_{IH}	Leakage	$V_{IN} = 5.5V = V_{CC}$		0.01	1.0	μA
I_{IL}	Low	$V_{IL} = 0.45V$		0.01	1.0	μA
I_{PP}	V_{PP} read	$V_{PP} = V_{CC}$			100	μA
Output current						
I_{LO}	Leakage	$\overline{OE}$ or $\overline{CE} = V_{IH}$ $V_{OUT} = 5.5V = V_{CC}$			1.0	μA
		$V_{OUT} = 0V = GND$			1.0	μA
I_{OS}	Short circuit[7, 9]	$V_{OUT} = 0V$			100	mA
Supply current						
I_{CC} TTL	Operating (TTL inputs)[4]	$\overline{CE} = \overline{OE} = V_{IL}$, f = 5.0MHz $V_{PP} = V_{CC}$ $O_{0-7} = 0mA$			20	mA
I_{SB} TTL	Standby (TTL inputs)[4]	$\overline{CE} = V_{IH}$			1.0	mA
I_{SB} CMOS	Standby (CMOS inputs)[5, 6]	$\overline{CE} = V_{IH}$			100	μA
Input voltage[2]						
V_{IL}	Low (TTL)	$V_{PP} = V_{CC}$	−0.5		0.8	V
V_{IL}	Low (CMOS)	$V_{PP} = V_{CC}$	−0.2		0.2	V
V_{IH}	High (TTL)	$V_{PP} = V_{CC}$	2.0		$V_{CC} + 0.5$	V
V_{IH}	High (CMOS)	$V_{PP} = V_{CC}$	$V_{CC} + 0.2$		$V_{CC} + 0.2$	V
V_{PP}	Read[8]	(Operating)	$V_{CC} - 0.7$		V_{CC}	V
Output voltage[2]						
V_{OL}	Low	$I_{OL} = 2.1mA$			0.45	V
V_{OH}	High	$I_{OH} = -2.5mA$	3.5			V
Capacitance[9] $T_A = 25°C$						
C_{IN}	Address and control	$V_{CC} = 5.0V$ f = 1.0MHz $V_{IN} = 0V$ $V_{OUT} = 0V$			6	pF
C_{OUT}	Outputs				12	pF

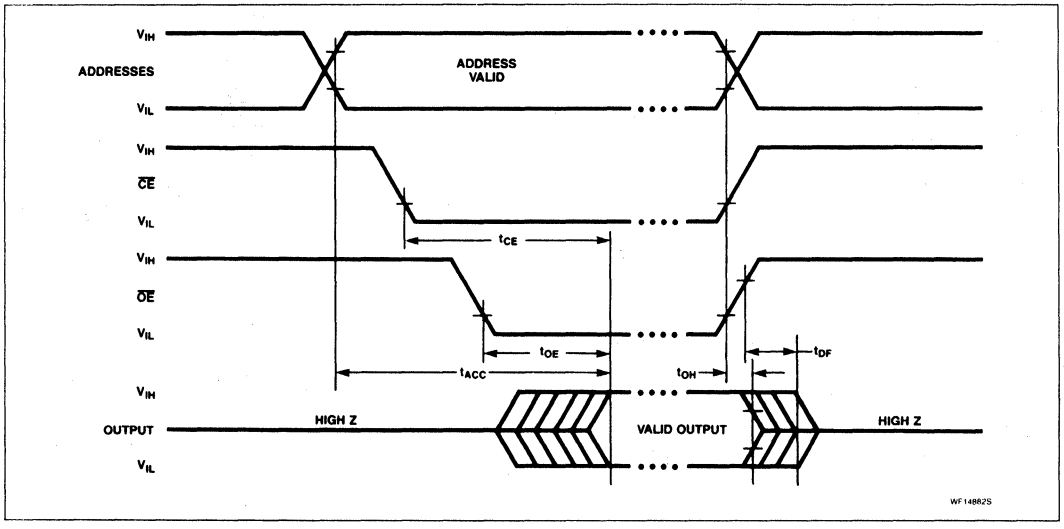
NOTES:
1. Minimum DC input voltage is −0.5V. During transitions the inputs may undershoot to −2.0V for periods less than 20ns.
2. All voltages are with respect to network ground.
3. Typical limits are at $V_{CC} = 5V$, $T_A = 25°C$.
4. TTL inputs: Spec V_{IL}, V_{IH} levels.
   CMOS inputs: GND ± 0.2V to V_{CC} ± 0.2V.
5. $\overline{CE}$ is V_{CC} ± 0.2V. All other inputs can have any value within spec.
6. Maximum active power usage is the sum of $I_{PP} + I_{CC}$ and is measured at a frequency of 5MHz.
7. Test one output at a time, duration should not exceed 1 second.
8. V_{PP} may be one diode voltage drop below V_{CC}, and can be connected directly to V_{CC}.
9. Guaranteed by design, not 100% tested.
10. X can be V_{IH} or V_{IL}.

AC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +70°C$, $+4.5V \leq V_{CC} \leq +5.5V$, $R_L = 660\Omega$, $C_L = 100pF$

SYMBOL	TO	FROM	27C256 – 20		UNIT
			Min	Max	
Access time[1]					
t_{ACC}	Output	Address		200	ns
t_{CE}	Output	$\overline{CE}$		200	ns
t_{OE}[3]	Output	$\overline{OE}$		75	ns
Disable time[2]					
t_{DF}[4]	Output Hi-Z	$\overline{OE}$ or $\overline{CE}$		55	ns
t_{OH}	Output hold	Address, $\overline{CE}$ or $\overline{OE}$	0		ns

NOTES:
1. AC characteristics are tested at $V_{IH} = 2.4V$ and $V_{IL} = 0.45V$. Timing measurements made at $V_{OL} = 0.8V$ and $V_{OH} = 2.0V$.
2. Guaranteed by design, not 100% tested.
3. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.
4. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

AC VOLTAGE WAVEFORMS



AC TESTING LOAD CIRCUIT

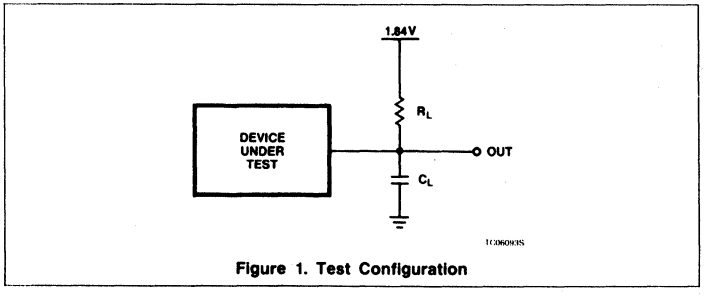


Figure 1. Test Configuration

27C256 U.V. Erasable 256K (32K × 8) EPROMs

Product Specification

Application Specific Products

DESCRIPTION

Signetics' 27C256 CMOS EPROM is a 256K-bit 5V only memory organized as 32,768 words of 8 bits each. It employs advanced CMOS circuitry for systems requiring low power, high-performance speeds, and immunity to noise. The 27C256 has a non-multiplexed addressing interface and is plug-compatible with the industry standard 27256.

The 27C256 available in a ceramic DIP package, achieves both high performance and low power consumption, making it ideal for high-performance, portable equipment. This device can be programmed with standard EPROM programmers.

FEATURES

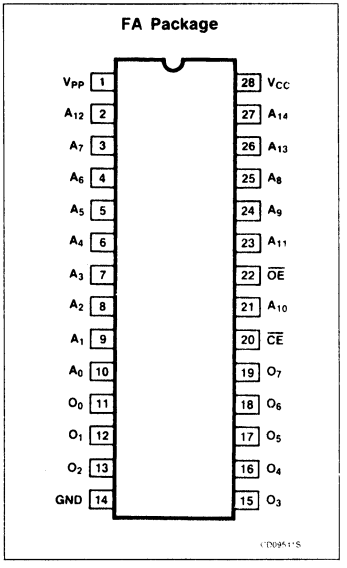
- **Low power consumption**
  - **100μA maximum CMOS standby current**
- **Quick pulse programming algorithm for high-speed production programming**
- **High-performance speeds**
  - **27C256-12: 120ns maximum access time**
- **Noise immunity features**
  - **± 10% V_{CC} tolerance**
  - **Maximum latch-up immunity through epitaxial processing**

PIN DESCRIPTION

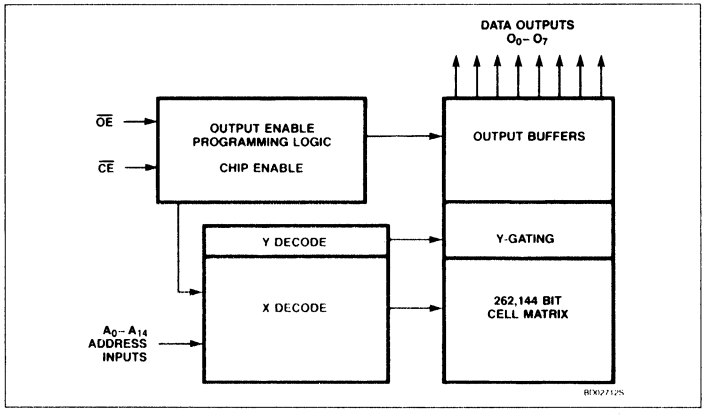
$A_0 - A_{14}$	Addresses
$O_0 - O_7$	Outputs
$\overline{OE}$	Output enable
$\overline{CE}$	Chip enable
GND	Ground
V_{PP}	Program voltage
V_{CC}	Power supply

PIN CONFIGURATION

FA Package



BLOCK DIAGRAM



READ MODE: 27C256

The 27C256 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins. Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been Low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

STANDBY MODE

The 27C256 has a standby mode which reduces the maximum V_{CC} current to 100μA. It is placed in the Standby mode when $\overline{CE}$ is in the High state. When in the Standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
28-pin Ceramic DIP with quartz window (600mil-wide)	27C256-12 FA

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
T_A	Temperature under bias	−10 to +80	°C
T_{STG}	Storage temperature	−65 to +125	°C
V_I, V_O	Voltage inputs and outputs	−2.0 to (V_{CC} + 1)	V
V_H	Voltage on A_9[2] (During intelligent identifier interrogation)	−2.0 to +13.5	V
V_{PP}	Voltage on V_{PP}[2] (During programming)	−2.0 to +14.0	V
V_{CC}	Supply voltage[2]	−2.0 to +7.0	V

NOTE:

1. Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. All voltages are with respect to network ground.

DEVICE OPERATION[2]

MODE	$\overline{CE}$	$\overline{OE}$[10]	V_{PP}[8]	OUTPUTS
Read	V_{IL}	V_{IL}	V_{CC}	D_{OUT}
Output disable	V_{IL}	V_{IH}	V_{CC}	Hi-Z
Standby	V_{IH}	X	V_{CC}	Hi-Z

Notes on following page.

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +70°C$, $+4.5V \leq V_{CC} \leq +5.5V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[3]	Max	
Input current						
I_{IH}	Leakage	$V_{IN} = 5.5V = V_{CC}$		0.01	1.0	µA
I_{IL}	Low	$V_{IL} = 0.45V$		0.01	-1.0	µA
I_{PP}	V_{PP} read	$V_{PP} = V_{CC}$			100	µA
Output current						
I_{LO}	Leakage	$\overline{OE}$ or $\overline{CE} = V_{IH}$ $V_{OUT} = 5.5V = V_{CC}$			1.0	µA
		$V_{OUT} = 0V = GND$			-1.0	µA
I_{OS}	Short circuit[7, 9]	$V_{OUT} = 0V$			-100	mA
Supply current						
I_{CC} TTL	Operating (TTL inputs)[4]	$\overline{CE} = \overline{OE} = V_{IL}$, f = 8.0MHz $V_{PP} = V_{CC}$ $O_{0-7} = 0mA$			20	mA
I_{SB} TTL	Standby (TTL inputs)[4]	$\overline{CE} = V_{IH}$			1.0	µA
I_{SB} CMOS	Standby (CMOS inputs)[5, 6]	$\overline{CE} = V_{IH}$			100	µA
Input voltage[2]						
V_{IL}	Low (TTL)	$V_{PP} = V_{CC}$	-0.5		0.8	V
V_{IL}	Low (CMOS)	$V_{PP} = V_{CC}$	-0.2		0.2	V
V_{IH}	High (TTL)	$V_{PP} = V_{CC}$	2.0		$V_{CC} + 0.5$	V
V_{IH}	High (CMOS)	$V_{PP} = V_{CC}$	$V_{CC} - 0.2$		$V_{CC} + 0.2$	V
V_{PP}	Read[8]	(Operating)	$V_{CC} - 0.7$		V_{CC}	V
Output voltage[2]						
V_{OL}	Low	$I_{OL} = 2.1mA$			0.45	V
V_{OH}	High	$I_{OH} = -2.5mA$	3.5			V
Capacitance[9] $T_A = 25°C$						
C_{IN}	Address and control	$V_{CC} = 5.0V$ f = 1.0MHz $V_{IN} = 0V$ $V_{OUT} = 0V$			6	pF
C_{OUT}	Outputs				12	pF

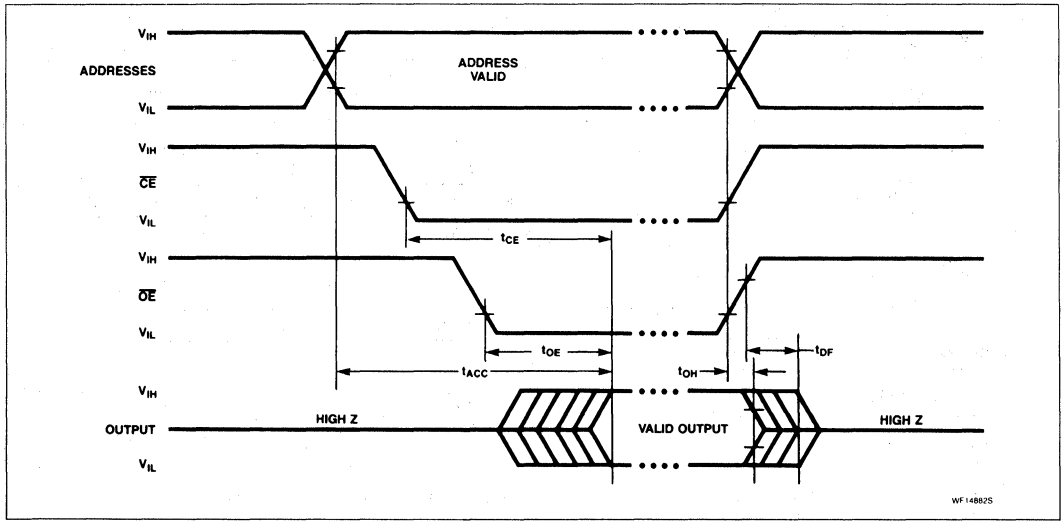
NOTES:
1. Minimum DC input voltage is -0.5V. During transitions the inputs may undershoot to -2.0V for periods less than 20ns.
2. All voltages are with respect to network ground.
3. Typical limits are at $V_{CC} = 5V$, $T_A = 25°C$.
4. TTL inputs: Specification V_{IL}, V_{IH} levels.
   CMOS inputs: GND ± 0.2V to V_{CC} ± 0.2V.
5. $\overline{CE}$ is V_{CC} ± 0.2V. All other inputs can have any value within specification
6. Maximum active power usage is the sum of $I_{PP} + I_{CC}$ and is measured at a frequency of 5MHz.
7. Test one output at a time, duration should not exceed 1 second.
8. V_{PP} may be one diode voltage drop below V_{CC}, and can be connected directly to V_{CC}.
9. Guaranteed by design, not 100% tested.
10. X can be V_{IH} or V_{IL}.

AC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +70°C$, $+4.5V \leq V_{CC} \leq +5.5V$, $R_L = 660\Omega$, $C_L = 100pF$

SYMBOL	TO	FROM	27C256 – 12		UNIT
			Min	Max	
Access time[1]					
t_{ACC}	Output	Address		120	ns
t_{CE}	Output	$\overline{CE}$		120	ns
t_{OE}[3]	Output	$\overline{OE}$		60	ns
Disable time[2]					
t_{DF}[4]	Output Hi-Z	$\overline{OE}$ or $\overline{CE}$		30	ns
t_{OH}	Output hold	Address, $\overline{CE}$ or $\overline{OE}$	0		ns

NOTES:
1. AC characteristics are tested at $V_{IH} = 2.4V$ and $V_{IL} = 0.45V$. Timing measurements made at $V_{OL} = 0.8V$ and $V_{OH} = 2.0V$.
2. Guaranteed by design, not 100% tested.
3. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.
4. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

AC VOLTAGE WAVEFORMS



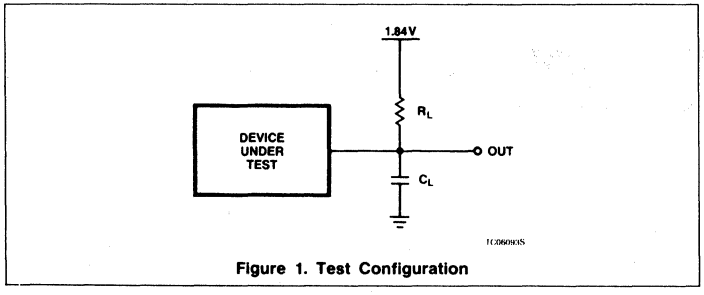


Figure 1. Test Configuration

27C256 U.V.
Erasable 256K (32K × 8) EPROMs

Product Specification

Application Specific Products

DESCRIPTION

Signetics 27C256 CMOS EPROM is a 256K-bit 5V only memory organized as 32,768 words of 8 bits each. It employs advanced CMOS circuitry for systems requiring low power, high-performance speeds, and immunity to noise. The 27C256 has a non-multiplexed addressing interface and is plug-compatible with the industry standard 27256.

The 27C256 available in a ceramic DIP package, achieves both high performance and low power consumption, making it ideal for high-performance, portable equipment. This device can be programmed with standard EPROM programmers.

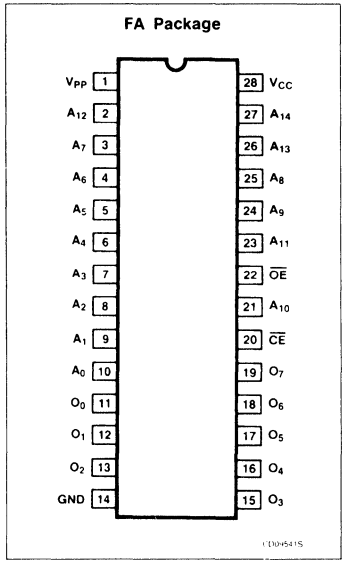
FEATURES

- **Low power consumption**
  - **100μA maximum CMOS standby current**
- **Quick pluse programming algorithm for high-speed production programming**
- **High-performance speeds**
  - **27C256-15: 150ns maximum access time**
  - **27C256-17: 170ns maximum access time**
- **Noise immunity features**
  - **± 10% V_{CC} tolerance**
  - **Maximum latch-up immunity through epitaxial processing**

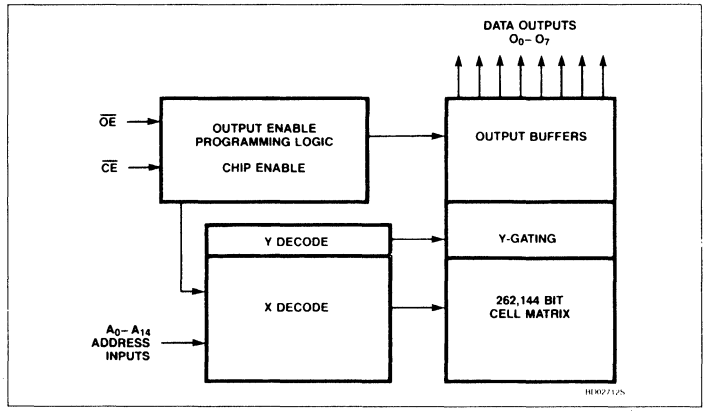
PIN DESCRIPTION

$A_0 - A_{14}$	Addresses
$O_0 - O_7$	Outputs
$\overline{OE}$	Output enable
$\overline{CE}$	Chip enable
GND	Ground
V_{PP}	Program voltage
V_{CC}	Power supply

PIN CONFIGURATION



BLOCK DIAGRAM



READ MODE: 27C256

The 27C256 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins. Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been Low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

STANDBY MODE

The 27C256 has a standby mode which reduces the maximum V_{CC} current to 100μA. It is placed in the Standby mode when $\overline{CE}$ is in the High state. When in the Standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
28-pin cerdip with quartz window (600mil-wide)	27C256-15 FA 27C256-17 FA

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
T_A	Temperature under bias	−10 to +80	°C
T_{STG}	Storage temperature	−65 to +125	°C
V_I, V_O	Voltage inputs and outputs	−2.0 to (V_{CC} + 1)	V
V_H	Voltage on A_9[2] (During intelligent identifier interrogation)	−2.0 to +13.5	V
V_{PP}	Voltage on V_{PP}[2] (During programming)	−2.0 to +14.0	V
V_{CC}	Supply voltage[2]	−2.0 to +7.0	V

NOTE:

1. Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. All voltages are with respect to network ground.

DEVICE OPERATION[2]

MODE	$\overline{CE}$	$\overline{OE}$[10]	V_{PP}[8]	OUTPUTS
Read	V_{IL}	V_{IL}	V_{CC}	D_{OUT}
Output disable	V_{IL}	V_{IH}	V_{CC}	Hi-Z
Standby	V_{IH}	X	V_{CC}	Hi-Z

Notes on following page.

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +70°C$, $+4.5V \leq V_{CC} \leq +5.5V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[3]	Max	
Input current						
I_{IH}	Leakage	$V_{IN} = 5.5V = V_{CC}$		0.01	1.0	μA
I_{IL}	Low	$V_{IL} = 0.45V$		0.01	-1.0	μA
I_{PP}	V_{PP} read	$V_{PP} = V_{CC}$			100	μA
Output current						
I_{LO}	Leakage	$\overline{OE}$ or $\overline{CE} = V_{IH}$			1.0	μA
		$V_{OUT} = 5.5V = V_{CC}$ $V_{OUT} = 0V = GND$			-1.0	μA
I_{OS}	Short circuit[7, 9]	$V_{OUT} = 0V$			-100	mA
Supply current						
I_{CC} TTL	Operating (TTL inputs)[4]	$\overline{CE} = \overline{OE} = V_{IL}$, f = 6.7MHz $V_{PP} = V_{CC}$ $O_{0-7} = 0mA$			20	mA
I_{SB} TTL	Standby (TTL inputs)[4]	$\overline{CE} = V_{IH}$			1.0	μA
I_{SB} CMOS	Standby (CMOS inputs)[5, 6]	$\overline{CE} = V_{IH}$			100	μA
Input voltage[2]						
V_{IL}	Low (TTL)	$V_{PP} = V_{CC}$	-0.5		0.8	V
V_{IL}	Low (CMOS)	$V_{PP} = V_{CC}$	-0.2		0.2	V
V_{IH}	High (TTL)	$V_{PP} = V_{CC}$	2.0		$V_{CC} + 0.5$	V
V_{IH}	High (CMOS)	$V_{PP} = V_{CC}$	$V_{CC} - 0.2$		$V_{CC} + 0.2$	V
V_{PP}	Read[8]	(Operating)	$V_{CC} - 0.7$		V_{CC}	V
Output voltage[2]						
V_{OL}	Low	$I_{OL} = 2.1mA$			0.45	V
V_{OH}	High	$I_{OH} = -2.5mA$	3.5			V
Capacitance[9] $T_A = 25°C$						
C_{IN}	Address and control	$V_{CC} = 5.0V$ f = 1.0MHz $V_{IN} = 0V$ $V_{OUT} = 0V$			6	pF
C_{OUT}	Outputs				12	pF

NOTES:

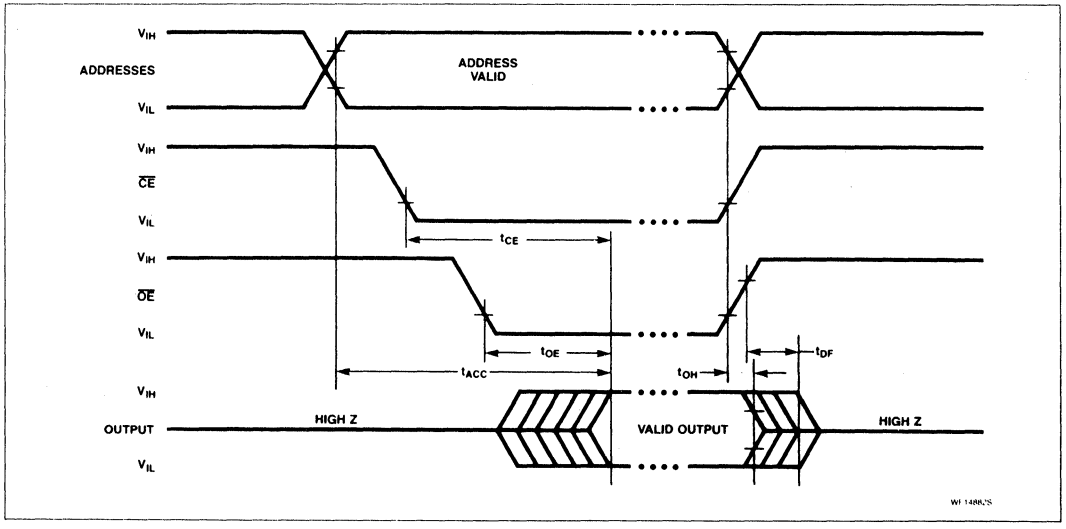
1. Minimum DC input voltage is -0.5V. During transitions the inputs may undershoot to -2.0V for periods less than 20ns.
2. All voltages are with respect to network ground.
3. Typical limits are at $V_{CC} = 5V$, $T_A = 25°C$.
4. TTL inputs: Specification V_{IL}, V_{IH} levels.
   CMOS inputs: GND ±0.2V to V_{CC} ±0.2V.
5. $\overline{CE}$ is V_{CC} ±0.2V. All other inputs can have any value within specification
6. Maximum active power usage is the sum of $I_{PP} + I_{CC}$ and is measured at a frequency of 5MHz.
7. Test one output at a time, duration should not exceed 1 second.
8. V_{PP} may be one diode voltage drop below V_{CC}, and can be connected directly to V_{CC}.
9. Guaranteed by design, not 100% tested.
10. X can be V_{IH} or V_{IL}.

AC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +70°C$, $+4.5V \leq V_{CC} \leq +5.5V$, $R_L = 660\Omega$, $C_L = 100pF$

SYMBOL	TO	FROM	27C256 – 15		27C256 – 17		UNIT
			Min	Max	Min	Max	
Access time[1]							
t_{ACC}	Output	Address		150		170	ns
t_{CE}	Output	$\overline{CE}$		150		170	ns
t_{OE}[3]	Output	$\overline{OE}$		65		70	ns
Disable time[2]							
t_{DF}[4]	Output Hi-Z	$\overline{OE}$ or $\overline{CE}$		45		55	ns
t_{OH}	Output hold	Address, $\overline{CE}$ or $\overline{OE}$	0		0		ns

NOTES:
1. AC characteristics are tested at $V_{IH} = 2.4V$ and $V_{IL} = 0.45V$. Timing measurements made at $V_{OL} = 0.8V$ and $V_{OH} = 2.0V$.
2. Guaranteed by design, not 100% tested.
3. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.
4. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

AC VOLTAGE WAVEFORMS



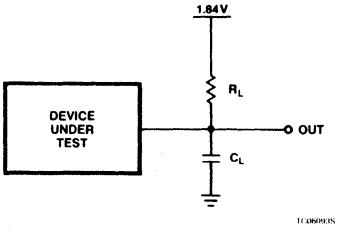


Figure 1. Test Configuration

27C256 U.V.
Erasable 256K (32K × 8) EPROMs

Product Specification

Application Specific Products

DESCRIPTION

Signetics' 27C256 CMOS EPROM is a 256K-bit 5V only memory organized as 32,768 words of 8 bits each. It employs advanced CMOS circuitry for systems requiring low power, high-performance speeds, and immunity to noise. The 27C256 has a non-multiplexed addressing interface and is plug-compatible with the industry standard 27256.

The 27C256 available in a ceramic DIP package, achieves both high performance and low power consumption, making it ideal for high-performance, portable equipment. This device can be programmed with standard EPROM programmers, and the intelligent programming algorithm may be used.

FEATURES

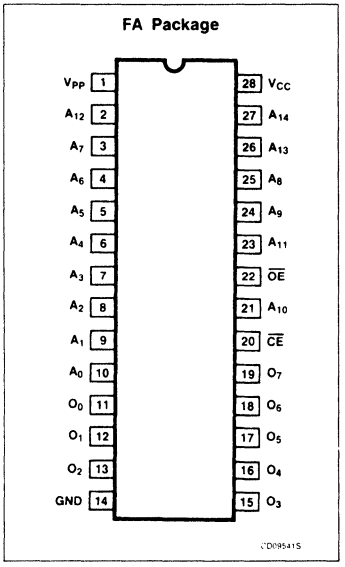
- **Low power consumption**
  - **100μA maximum CMOS standby current**
- **High-performance speeds**
  - **27C256-20: 200ns maximum access time**
- **Noise immunity features**
  - **± 10% V_{CC} tolerance**
  - **Maximum latch-up immunity through epitaxial processing**

PIN DESCRIPTION

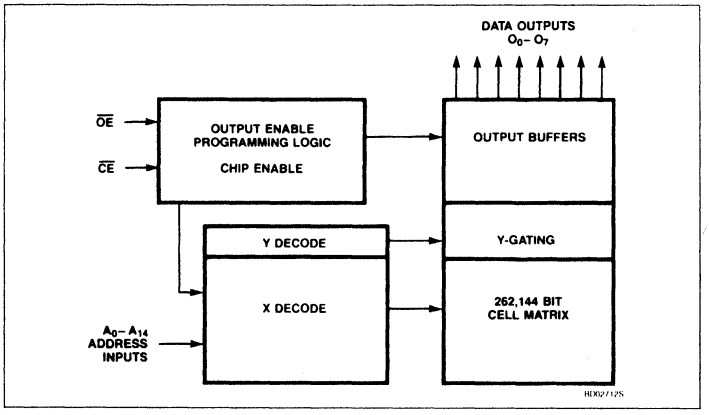
$A_0 - A_{14}$	Addresses
$O_0 - O_7$	Outputs
$\overline{OE}$	Output enable
$\overline{CE}$	Chip enable
GND	Ground
V_{PP}	Program voltage
V_{CC}	Power supply

PIN CONFIGURATION

FA Package



BLOCK DIAGRAM



READ MODE: 27C256

The 27C256 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins. Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been Low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

STANDBY MODE

The 27C256 has a standby mode which reduces the maximum V_{CC} current to 100μA. It is placed in the Standby mode when $\overline{CE}$ is in the High state. When in the Standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
28-pin Ceramic DIP with quartz window (600mil-wide)	27C256-20 FA

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
T_A	Temperature under bias	−10 to +80	°C
T_{STG}	Storage temperature	−65 to +125	°C
V_I, V_O	Voltage inputs and outputs	−2.0 to (V_{CC} + 1)	V
V_H	Voltage on A_9[2] (During intelligent identifier interrogation)	−2.0 to +13.5	V
V_{PP}	Voltage on V_{PP}[2] (During programming)	−2.0 to +14.0	V
V_{CC}	Supply voltage[2]	−2.0 to +7.0	V

NOTE:

1. Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. All voltages are with respect to network ground.

DEVICE OPERATION[2]

MODE	$\overline{CE}$	$\overline{OE}$[10]	V_{PP}[8]	OUTPUTS
Read	V_{IL}	V_{IL}	V_{CC}	D_{OUT}
Output disable	V_{IL}	V_{IH}	V_{CC}	Hi-Z
Standby	V_{IH}	X	V_{CC}	Hi-Z

Notes on following page.

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +70°C$, $+4.5V \leq V_{CC} \leq +5.5V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[3]	Max	
Input current						
I_{IH}	Leakage	$V_{IN} = 5.5V = V_{CC}$		0.01	1.0	μA
I_{IL}	Low	$V_{IL} = 0.45V$		0.01	1.0	μA
I_{PP}	V_{PP} read	$V_{PP} = V_{CC}$			100	μA
Output current						
I_{LO}	Leakage	$\overline{OE}$ or $\overline{CE} = V_{IH}$ $V_{OUT} = 5.5V = V_{CC}$			1.0	μA
		$V_{OUT} = 0V = GND$			1.0	μA
I_{OS}	Short circuit[7, 9]	$V_{OUT} = 0V$			100	mA
Supply current						
I_{CC} TTL	Operating (TTL inputs)[4]	$\overline{CE} = \overline{OE} = V_{IL}$, f = 5.0MHz $V_{PP} = V_{CC}$ $O_{0-7} = 0mA$			20	mA
I_{SB} TTL	Standby (TTL inputs)[4]	$\overline{CE} = V_{IH}$			1.0	μA
I_{SB} CMOS	Standby (CMOS inputs)[5, 6]	$\overline{CE} = V_{IH}$			100	μA
Input voltage[2]						
V_{IL}	Low (TTL)	$V_{PP} = V_{CC}$	−0.5		0.8	V
V_{IL}	Low (CMOS)	$V_{PP} = V_{CC}$	−0.2		0.2	V
V_{IH}	High (TTL)	$V_{PP} = V_{CC}$	2.0		$V_{CC} + 0.5$	V
V_{IH}	High (CMOS)	$V_{PP} = V_{CC}$	$V_{CC} - 0.2$		$V_{CC} + 0.2$	V
V_{PP}	Read[8]	(Operating)	$V_{CC} - 0.7$		V_{CC}	V
Output voltage[2]						
V_{OL}	Low	$I_{OL} = 2.1mA$			0.45	V
V_{OH}	High	$I_{OH} = -2.5mA$	3.5			V
Capacitance[9] $T_A = 25°C$						
C_{IN}	Address and control	$V_{CC} = 5.0V$ f = 1.0MHz $V_{IN} = 0V$ $V_{OUT} = 0V$			6	pF
C_{OUT}	Outputs				12	pF

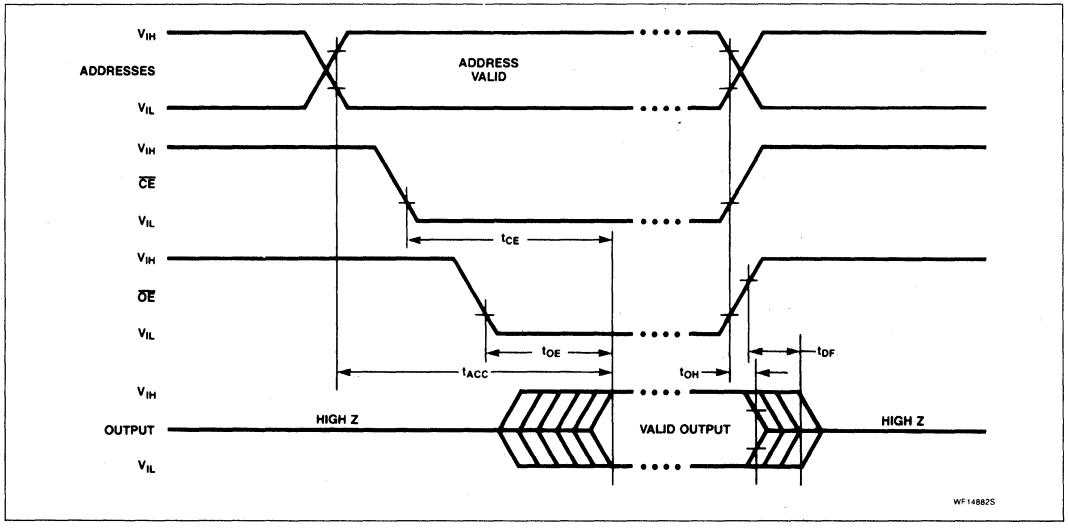
NOTES:
1. Minimum DC input voltage is −0.5V. During transitions the inputs may undershoot to −2.0V for periods less than 20ns.
2. All voltages are with respect to network ground.
3. Typical limits are at $V_{CC} = 5V$, $T_A = 25°C$.
4. TTL inputs: Specification V_{IL}, V_{IH} levels.
   CMOS inputs: GND ± 0.2V to V_{CC} ± 0.2V.
5. $\overline{CE}$ is V_{CC} ± 0.2V. All other inputs can have any value within specification
6. Maximum active power usage is the sum of $I_{PP} + I_{CC}$ and is measured at a frequency of 5MHz.
7. Test one output at a time, duration should not exceed 1 second.
8. V_{PP} may be one diode voltage drop below V_{CC}, and can be connected directly to V_{CC}.
9. Guaranteed by design, not 100% tested.
10. X can be V_{IH} or V_{IL}.

AC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +70°C$, $+4.5V \leq V_{CC} \leq +5.5V$, $R_L = 660\Omega$, $C_L = 100pF$

SYMBOL	TO	FROM	27C256 – 20		UNIT
			Min	Max	
Access time[1]					
t_{ACC}	Output	Address		200	ns
t_{CE}	Output	$\overline{CE}$		200	ns
t_{OE}[3]	Output	$\overline{OE}$		75	ns
Disable time[2]					
t_{DF}[4]	Output High-Z	$\overline{OE}$ or $\overline{CE}$		55	ns
t_{OH}	Output hold	Address, $\overline{CE}$ or $\overline{OE}$	0		ns

NOTES:
1. AC characteristics are tested at $V_{IH} = 2.4V$ and $V_{IL} = 0.45V$. Timing measurements made at $V_{OL} = 0.8V$ and $V_{OH} = 2.0V$.
2. Guaranteed by design, not 100% tested.
3. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.
4. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

AC VOLTAGE WAVEFORMS



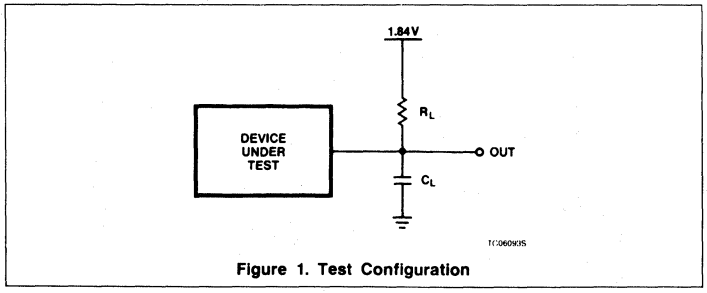


Figure 1. Test Configuration

516K-bit CMOS EPROM

page

27C512 O.T.P. **512K-bit CMOS EPROMs (64K x 8)**
150 ns; 170 ns; 200 ns **263**

27C512 U.V. **512K-bit erasable CMOS EPROMs (64K x 8)**
150 ns; 170 ns; 200 ns **267**

27C512 O.T.P.
512K-Bit CMOS EPROMs (64K × 8)

Product Specification

Application Specific Products

DESCRIPTION

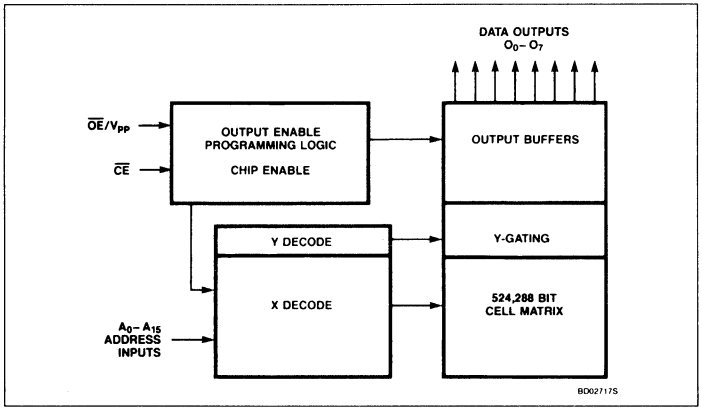
Signetics 27C512 CMOS O.T.P. EPROM is a 512K-bit 5V only memory organized as 65,536 words of 8 bits each. It employs advanced CMOS circuitry for systems requiring low power, high-performance speeds, and immunity to noise. The 27C512 has a non-multiplexed addressing interface and is plug-compatible with the industry standard 27512.

The 27C512 O.T.P. is offered in plastic DIP and plastic leaded chip carrier (PLCC) packages. Plastic EPROMs provide optimum cost effectiveness in production environments. Quick-pulse programming is employed on plastic devices which may speed up programming by as much as one hundred times.

FEATURES

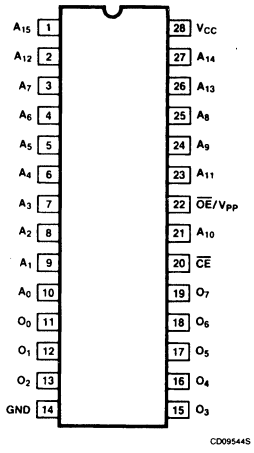
- **Low power consumption**
  - **100μA maximum CMOS standby current**
- **Quick-pulse programming algorithm for high-speed production programming**
- **High-performance speeds**
  - **27C512-15: 150ns maximum access time**
  - **27C512-17: 170ns maximum access time**
  - **27C512-20: 200ns maximum access time**
- **Noise immunity features**
  - **± 10% V_{CC} tolerance**
  - **Maximum latch-up immunity through epitaxial processing**

BLOCK DIAGRAM



PIN CONFIGURATIONS

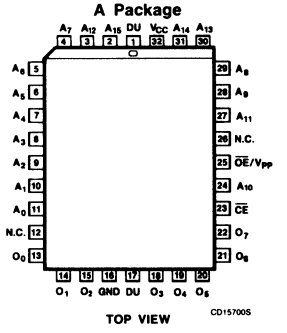
N Package



PIN DESCRIPTION

$A_0 - A_{15}$	Addresses
$O_0 - O_7$	Outputs
$\overline{OE}/V_{PP}$	Output enable/ Programming Voltage
$\overline{CE}$	Chip enable
N.C.	No connection
GND	Ground
V_{CC}	Power supply
DU	Don't use

A Package



READ MODE: 27C512

The 27C512 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output enable $\overline{OE}/V_{PP}$ is the output control and should be used to gate data from the output pins. Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}/V_{PP}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

STANDBY MODE

The 27C512 has a standby mode which reduces the maximum V_{CC} current to 100μA. It is placed in the Standby mode when $\overline{CE}$ is in the High state. When in the Standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}/V_{PP}$ pin.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
28-Pin Plastic DIP (600mil-wide)	27C512-15 N 27C512-17 N 27C512-20 N
32-Pin Plastic Leaded Chip Carrier (450mil × 550mil)	27C512-15 A 27C512-17 A 27C512-20 A

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS	UNIT
T_A	Operating temperature range	−10 to +80	°C
T_{STG}	Storage temperature range	−65 to +125	°C
V_I, V_O	Voltage inputs and outputs	−2.0 to (V_{CC} + 1)	V
V_H	Voltage on A_9[2] (during intelligent identifier interrogation)	−2.0 to +13.5	V
V_{PP}	Voltage on $\overline{OE}/V_{PP}$ pin (during programming)	−2.0 to +14.0	V
V_{CC}	Supply voltage[2]	−2.0 to +7.0	V

NOTE:

1. Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. All voltages are with respect to network ground.

DEVICE OPERATION[1]

MODE	$\overline{CE}$	$\overline{OE}/V_{PP}$	OUTPUT
Read	V_{IL}	V_{IL}	D_{OUT}
Output disable	V_{IL}	V_{IH}	Hi-Z
Standby	V_{IH}	X[2]	Hi-Z

NOTES:

1. All voltages are with respect to network ground.
2. X can be V_{IH} or V_{IL}.

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +70°C$, $+4.5V \leq V_{CC} \leq +5.5V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[3]	Max	
Input current						
I_{IH}	Leakage	$V_{IN} = 5.5V = V_{CC}$			10	μA
I_{IL}	Low	$V_{IL} = 0.45V$			−10	μA
Output current						
I_{LO}	Leakage	$\overline{OE}/V_{PP}$ or $\overline{CE} = V_{IH}$ $V_{OUT} = 5.5V = V_{CC}$			1.0	μA
		$V_{OUT} = 0V = GND$			−1.0	μA
I_{OS}	Short circuit[6, 7]	$V_{OUT} = 0V$			−100	mA
Supply current						
I_{CC} TTL	Operating (TTL inputs)[4]	$\overline{CE} = \overline{OE} = V_{IL}$, f = 6.7MHz $V_{PP} = V_{CC}$, $O_{0-7} = 0mA$			20	mA
I_{SB} TTL	Standby (TTL inputs)[4]	$\overline{CE} = V_{IH}$			1.0	mA
I_{SB} CMOS	Standby (CMOS inputs)[5, 6]	$\overline{CE} = V_{IH}$			100	μA
Input voltage[2]						
V_{IL}	Low (TTL)		−0.5		0.8	V
V_{IL}	Low (CMOS)		−0.2		0.2	V
V_{IH}	High (TTL)		2.0		$V_{CC} + 0.5$	V
V_{IH}	High (CMOS)		$V_{CC} - 0.2$		$V_{CC} + 0.2$	V
Output voltage[2]						
V_{OL}	Low	$I_{OL} = 2.1mA$			0.45	V
V_{OH}	High	$I_{OH} = -2.5mA$	3.5			V
Capacitance[7] $T_A = 25°C$						
C_{IN}	Address and $\overline{CE}$	$V_{CC} = 5.0V$ f = 1.0MHz $V_{IN} = 0V$ $V_{OUT} = 0V$			6	pF
C_{OUT}	Outputs				12	pF
C_{IN}	$\overline{OE}/V_{PP}$				25	pF

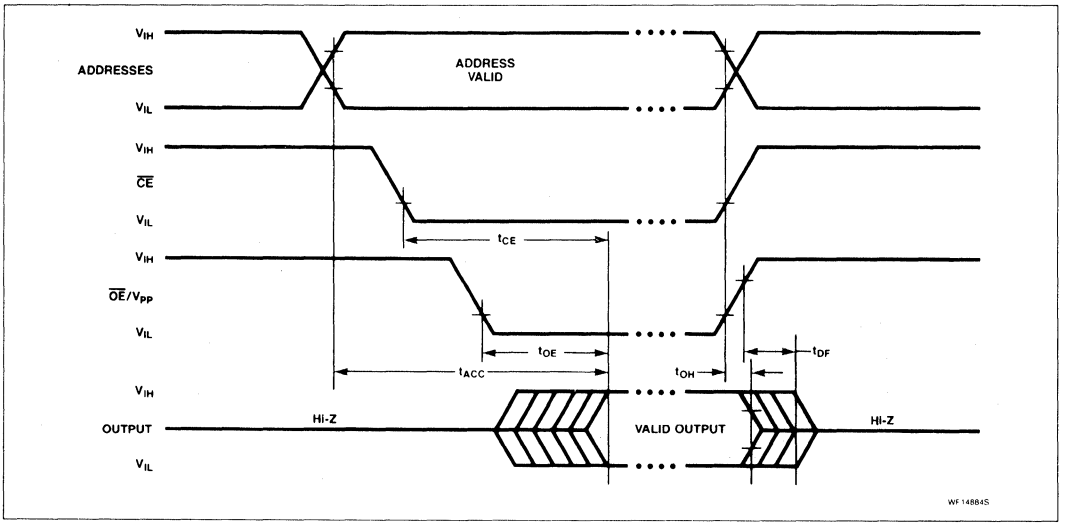
NOTES:
1. Minimum DC input voltage is −0.5V. During transitions the inputs may undershoot to −2.0V for periods less than 20ns.
2. All voltages are with respect to network ground.
3. Typical limits are at $V_{CC} = 5V$, $T_A = 25°C$.
4. TTL inputs: Spec V_{IL}, V_{IH} levels.
   CMOS inputs: GND + 0.2V to V_{CC} + 0.2V.
5. $\overline{CE}$ is V_{CC} + 0.2V. All other inputs can have any value within specification.
6. Test one output at a time, duration should not exceed 1 second.
7. Guaranteed by design, not 100% tested.

AC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +70°C$, $+4.5V \leq V_{CC} \leq +5.5V$, $R_L = 660\Omega$, $C_L = 100pF$

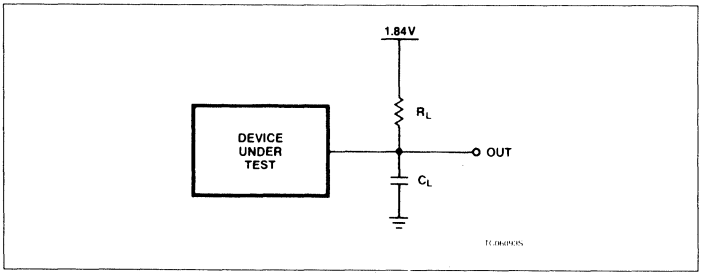
SYMBOL	TO	FROM	27C512 – 15		27C512 – 17		27C512 – 20		UNIT
			Min	Max	Min	Max	Min	Max	
Access time[1]									
t_{ACC}	Output	Address		150		170		200	ns
t_{CE}	Output	$\overline{CE}$		150		170		200	ns
t_{OE}[3]	Output	$\overline{OE}/V_{PP}$		60		60		75	ns
Disable time[2]									
t_{DF}[4]	Output Hi-Z	$\overline{OE}/V_{PP}$ or $\overline{CE}$		45		50		55	ns
t_{OH}	Output hold	Address, $\overline{CE}$ or $\overline{OE}/V_{PP}$	0		0		0		ns

NOTES:
1. AC characteristics are tested at $V_{IH} = 2.4V$ and $V_{IL} = 0.45V$. Timing measurements made at $V_{OL} = 0.8V$ and $V_{OH} = 2.0V$.
2. Guaranteed by design, not 100% tested.
3. $\overline{OE}/V_{PP}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.
4. t_{DF} is specified from $\overline{OE}/V_{PP}$ or $\overline{CE}$, whichever occurs first.

AC VOLTAGE WAVEFORMS



AC TESTING LOAD CIRCUIT



27C512 U.V.

512K-Bit Erasable CMOS EPROMs (64K × 8)

Product Specification

Application Specific Products

DESCRIPTION

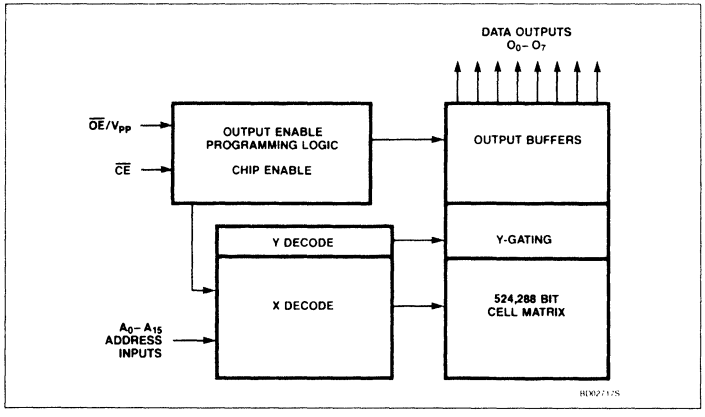
Signetics 27C512 CMOS EPROM is a 512K-bit, 5V-only memory organized as 65,536 words of 8 bits each. It employs advanced CMOS circuitry for systems requiring low power, high-performance speeds, and immunity to noise. The 27C512 has a non-multiplexed addressing interface and is plug-compatible with the industry standard 27512.

The 27C512 available in a ceramic DIP package, achieves both high performance and low power consumption, making it ideal for high-performance, portable equipment. This device can be programmed with standard EPROM programmers.

FEATURES

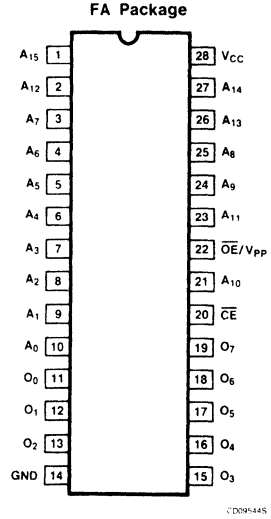
- **Low power consumption**
  - **100μA maximum CMOS standby current**
- **Quick pluse programming algorithm for high-speed production programming**
- **High-performance speeds**
  - **27C512-15: 150ns maximum access time**
  - **27C512-17: 170ns maximum access time**
  - **27C512-20: 200ns maximum access time**
- **Noise immunity features**
  - **± 10% V_{CC} tolerance**
  - **Maximum latch-up immunity through epitaxial processing**

BLOCK DIAGRAM



PIN CONFIGURATION

FA Package



PIN DESCRIPTION

$A_0 - A_{15}$	Addresses
$O_0 - O_7$	Outputs
$\overline{OE}/V_{PP}$	Output enable/ Programming Voltage
$\overline{CE}$	Chip enable
GND	Ground
V_{CC}	Power supply

READ MODE: 27C512

The 27C512 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable $\overline{OE}/V_{PP}$ is the output control and should be used to gate data from the output pins. Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}/V_{PP}$, assuming that $\overline{CE}$ has been Low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

STANDBY MODE

The 27C512 has a standby mode which reduces the maximum V_{CC} current to 100μA. It is placed in the Standby mode when $\overline{CE}$ is in the High state. When in the Standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}/V_{PP}$ pin.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
28-Pin Ceramic DIP with Quartz Window (600mil-wide)	27C512-15 FA 27C512-17 FA 27C512-20 FA

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS	UNIT
T_A	Operating temperature range	−10 to +80	°C
T_{STG}	Storage temperature range	−65 to +125	°C
V_I, V_O	Voltage inputs and outputs	−2.0 to (V_{CC} + 1)	V
V_H	Voltage on A_9[2] (during intelligent identifier interrogation)	−2.0 to +13.5	V
V_{PP}	Voltage on $\overline{OE}/V_{PP}$ pin (during programming)	−2.0 to +14.0	V
V_{CC}	Supply voltage[2]	−2.0 to +7.0	V

NOTE:

1. Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. All voltages are with respect to network ground.

DEVICE OPERATION[1]

MODE	$\overline{CE}$	$\overline{OE}/V_{PP}$	OUTPUT
Read	V_{IL}	V_{IL}	D_{OUT}
Output disable	V_{IL}	V_{IH}	Hi-Z
Standby	V_{IH}	X[2]	Hi-Z

NOTES:

1. All voltages are with respect to network ground.
2. X can be V_{IH} or V_{IL}.

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +70°C$, $+4.5V \leq V_{CC} \leq +5.5V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[3]	Max	
Input current						
I_{IH}	Leakage	$V_{IN} = 5.5V = V_{CC}$			10	μA
I_{IL}	Low	$V_{IL} = 0.45V$			−10	μA
Output current						
I_{LO}	Leakage	$\overline{OE}/V_{PP}$ or $\overline{CE} = V_{IH}$ $V_{OUT} = 5.5V = V_{CC}$			1.0	μA
		$V_{OUT} = 0V = GND$			−1.0	μA
I_{OS}	Short circuit[6, 7]	$V_{OUT} = 0V$			−100	mA
Supply current						
I_{CC} TTL	Operating (TTL inputs)[4]	$\overline{CE} = \overline{OE} = V_{IL}$, f = 6.7MHz $V_{PP} = V_{CC}$, $O_{0-7} = 0mA$			20	mA
I_{SB} TTL	Standby (TTL inputs)[4]	$\overline{CE} = V_{IH}$			1.0	mA
I_{SB} CMOS	Standby (CMOS inputs)[5, 6]	$\overline{CE} = V_{IH}$			100	μA
Input voltage[2]						
V_{IL}	Low (TTL)		−0.5		0.8	V
V_{IL}	Low (CMOS)		−0.2		0.2	V
V_{IH}	High (TTL)		2.0		$V_{CC} + 0.5$	V
V_{IH}	High (CMOS)		$V_{CC} - 0.2$		$V_{CC} + 0.2$	V
Output voltage[2]						
V_{OL}	Low	$I_{OL} = 2.1mA$			0.45	V
V_{OH}	High	$I_{OH} = -2.5mA$	3.5			V
Capacitance[7] $T_A = 25°C$						
C_{IN}	Address and $\overline{CE}$	$V_{CC} = 5.0V$ f = 1.0MHz $V_{IN} = 0V$ $V_{OUT} = 0V$			6	pF
C_{OUT}	Outputs				12	pF
C_{IN}	$\overline{OE}/V_{PP}$				25	pF

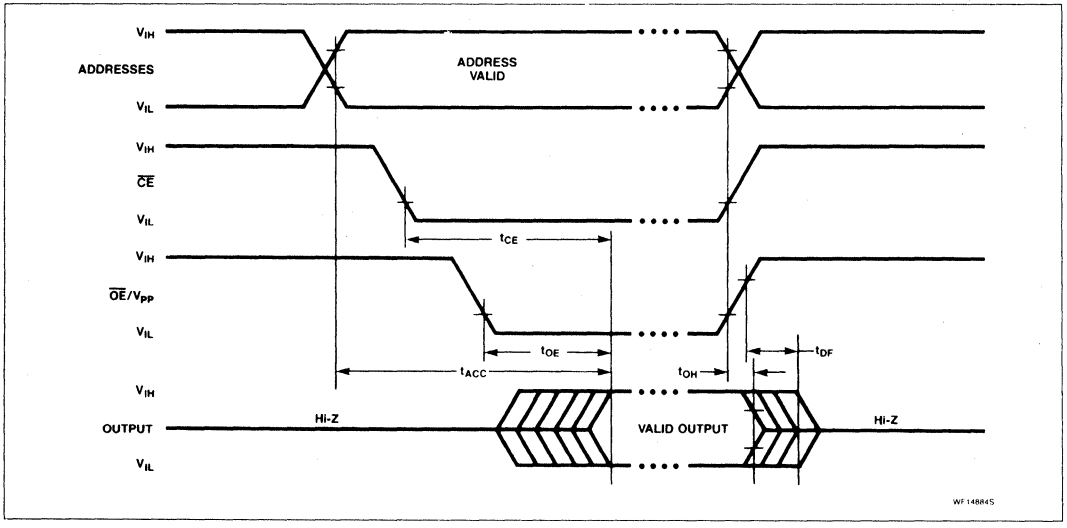
NOTES:
1. Minimum DC input voltage is −0.5V. During transitions the inputs may undershoot to −2.0V for periods less than 20ns.
2. All voltages are with respect to network ground.
3. Typical limits are at $V_{CC} = 5V$, $T_A = 25°C$.
4. TTL inputs: Specification V_{IL}, V_{IH} levels.
   CMOS inputs: GND ± 0.2V to V_{CC} ± 0.2V.
5. $\overline{CE}$ is V_{CC} ± 0.2V. All other inputs can have any value within specification.
6. Test one output at a time, duration should not exceed 1 second.
7. Guaranteed by design, not 100% tested.

AC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +70°C$, $+4.5V \leq V_{CC} \leq +5.5V$, $R_L = 660\Omega$, $C_L = 100pF$

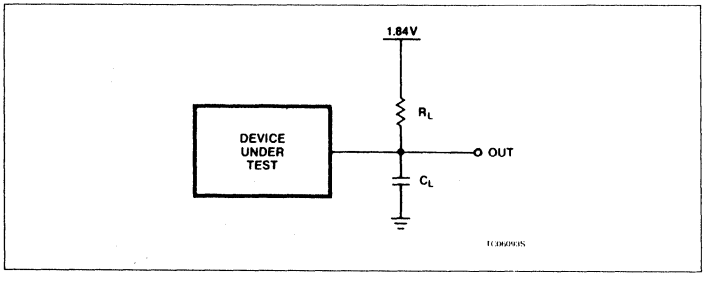
SYMBOL	TO	FROM	27C512-15		27C512-17		27C512-20		UNIT
			Min	Max	Min	Max	Min	Max	
Access time[1]									
t_{ACC}	Output	Address		150		170		200	ns
t_{CE}	Output	$\overline{CE}$		150		170		200	ns
t_{OE}[3]	Output	$\overline{OE}$		60		60		75	ns
Disable time[2]									
t_{DF}[4]	Output Hi-Z	$\overline{OE}$ or $\overline{CE}$		45		50		55	ns
t_{OH}	Output hold	Address, $\overline{CE}$ or $\overline{OE}$	0		0		0		ns

NOTES:
1. AC characteristics are tested at $V_{IH} = 2.4V$ and $V_{IL} = 0.45V$. Timing measurements made at $V_{OL} = 0.8V$ and $V_{OH} = 2.0V$.
2. Guaranteed by design, not 100% tested.
3. $\overline{OE}/V_{PP}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.
4. t_{DF} is specified from $\overline{OE}/V_{PP}$ or $\overline{CE}$, whichever occurs first.

AC VOLTAGE WAVEFORMS



AC TESTING LOAD CIRCUIT



1M-bit CMOS EPROM

page

27C210 O.T.P. 1M programmable EPROMs (64K x 16) 150 ns; 200 ns 273

27C210 O.V. 1M erasable EPROMs (64K x 16) 150 ns; 200 ns 277

27C210 O.T.P.
Programmable 1 MEG (64K × 16) EPROM

Application Specific Products

Objective Specification

DESCRIPTION

Signetics 27C210 CMOS O.T.P. EPROM is a 1,048,576–bit 5V only memory organized as 65,536 words of 16 bits each. It employs advanced CMOS circuitry for systems requiring low power, high–performance speeds, and immunity to noise. The 27C210 has a non–multiplexed addressing interface and is plug–compatible with the industry standard 27210.

The 27C210 O.T.P. is offered in plastic DIP and Plastic Leaded Chip Carrier (PLCC) packages. Plastic EPROMs provide optimum cost effectiveness in production environments. Quick–pulse programming is employed on plastic devices which may speed up programming by as much as one hundred time. In the absence of quick–pulse programming equipment, the intelligent programming algorithm may be utilized.

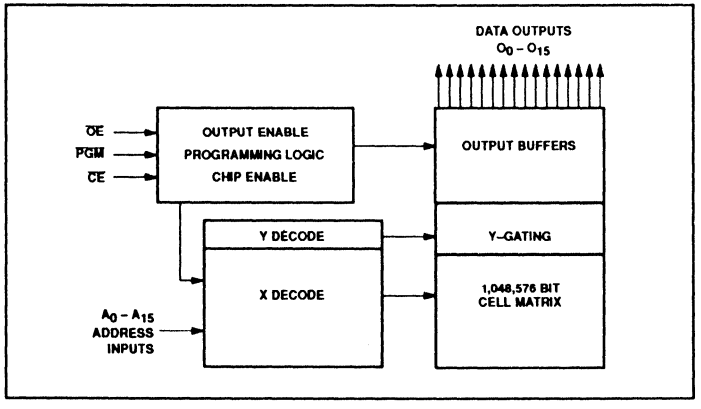
FEATURES

- **Low power consumption**
  - **100μA maximum CMOS standby current**
- **High–performance speeds:**
  - **150ns maximum access time**
  - **200ns maximum access time**
- **Noise immunity features:**
  - **±10% V_{CC} tolerance**
  - **Maximum latch–up immunity through Epitaxial processing**
- **Quick–pulse programming algorithm**

PIN DESCRIPTION

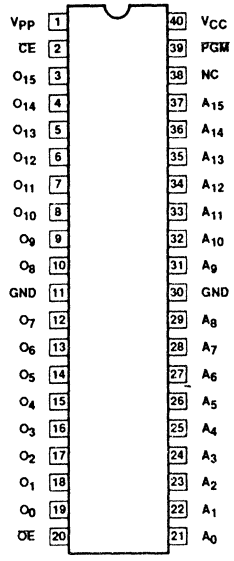
$A_0 - A_{15}$	Address
$O_0 - O_{15}$	Outputs
$\overline{OE}$	Output Enable
$\overline{CE}$	Chip Enable
$\overline{PGM}$	Program
NC	No Connection
GND	Ground
V_{PP}	Program voltage
V_{CC}	Power supply
DU	Don't Use

BLOCK DIAGRAM

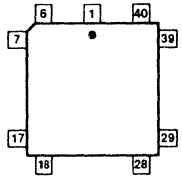


PIN CONFIGURATIONS

N Package



A Package



Pin	Function	Pin	Function	Pin	Function
1	DU	16	O_5	31	A_7
2	V_{PP}	17	O_4	32	A_8
3	$\overline{CE}$	18	O_3	33	NC
4	O_{15}	19	O_2	34	GND
5	O_{14}	20	O_1	35	A_9
6	O_{13}	21	O_0	36	A_{10}
7	O_{12}	22	$\overline{OE}$	37	A_{11}
8	O_{11}	23	DU	38	A_{12}
9	O_{10}	24	A_0	39	A_{13}
10	O_9	25	A_1	40	A_{14}
11	O_8	26	A_2	41	A_{15}
12	GND	27	A_3	42	NC
13	NC	28	A_4	43	$\overline{PGM}$
14	O_7	29	A_5	44	V_{CC}
15	O_6	30	A_6		

Programmable 1 MEG (64K × 16) EPROM

27C210 O.T.P.

READ MODE: 27C210

The 27C210 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins. Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been Low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

STANDBY MODE

The 27C210 has a standby mode which reduces the maximum V_{CC} current to 100µA. It is placed in the Standby mode when $\overline{CE}$ is in the High state. When in the Standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

DEVICE OPERATION

The modes of operation of the 27C210 are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A_9 for Signetics Identifier.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
40–Pin Plastic Dual–In–Line (600mil–wide)	27C210–15 N
40–Pin Plastic Dual–In–Line (600mil–wide)	27C210–20 N
44–Pin Plastic Leaded Chip Carrier (0.69 × 0.6)	27C210–20 A
44–Pin Plastic Leaded Chip Carrier (0.69 × 0.6)	27C210–15 A

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
T_A	Temperature under bias	–10 to +80	°C
T_{STG}	Storage temperature range	–65 to +125	°C
V_I, V_O	Voltage inputs and outputs	–0.6 to (V_{CC} + 1)	V
V_H	Voltage on A_9[2] (during intelligent identifier interrogation)	–0.6 to +13.0	V
V_{PP}	Voltage on V_{PP}[2] (during programming)	–0.6 to +14.0	V
V_{CC}	Supply voltage[2]	–0.6 to +7.0	V

NOTES:
1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. All voltages are with respect to network ground.

Table 1. Modes Selection

Pins / Mode		$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A_9	A_0	V_{PP}	V_{CC}	Outputs
Read		V_{IL}	V_{IL}	X	X[1]	X	X	5.0V	D_{OUT}
Output Disable		V_{IL}	V_{IH}	X	X	X	X	5.0V	Hi–Z
Standby		V_{IH}	X	X	X	X	V_{CC}	5.0V	Hi–Z
Programming		V_{IL}	V_{IH}	V_{IL}	X	X	Note 4	Note 4	D_{IN}
Program Verify		V_{IL}	V_{IL}	V_{IH}	X	X	Note 4	Note 4	D_{OUT}
Program Inhibit		V_{IH}	X	X	X	X	Note 4	Note 4	Hi–Z
Signetics	Manufactured[2]	V_{IL}	V_{IL}	X	V_H[2]	V_{IL}	V_{CC}	5.0V	FF15
Identifier	Device[3]	V_{IL}	V_{IL}	X	V_H[2]	V_{IH}	V_{CC}	5.0V	FF17

NOTES:
1. X can be V_{IL} or V_{IH}
2. $V_H = 12.0V \pm 0.5V$
3. $A_1 - A_8$, $A_{10} - A_{15} = V_{IL}$
4. See Table 2 for V_{CC} and V_{PP} voltages.

DC ELECTRICAL CHARACTERISTICS $0°C \le T_A \le +70°C$, $+4.5V \le V_{CC} \le +5.5V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS Min	LIMITS Typ[3]	LIMITS Max	UNIT
Input current						
I_{IH}	Leakage	$V_{IN} = 5.5V = V_{CC}$		0.01	1.0	µA
I_{IL}	Low	$V_{IL} = 0.45V$		0.01	1.0	µA
I_{PP}	V_{PP} read	$V_{PP} = V_{CC}$			10	µA
Output current						
I_{OL}	Leakage	$\overline{OE}$ or $\overline{CE} = V_{IH}$			10.0	µA
		$V_{OUT} = 5.5V = V_{CC}$			10.0	µA
		$V_{OUT} = 0V = GND$			10.0	µA
I_{OS}	Short circuit[7, 9]	$V_{OUT} = 0V$			100	mA
Supply current						
I_{CC} TTL	Operating (TTL inputs)[4]	$\overline{CE} = \overline{OE} = V_{IL}$, f = 5.0MHz $V_{PP} = V_{CC}$ $O_{0-15} = 0mA$			50	mA
I_{SB} TTL	Standby (TTL inputs)[4]	$\overline{CE} = V_{IH}$			1	mA
I_{SB} CMOS	Standby (CMOS inputs)[5, 6]	$\overline{CE} = V_{IH}$			100	µA
Input voltage[2]						
V_{IL}	Low (TTL)	$V_{PP} = V_{CC}$	–0.5		0.8	V
V_{IL}	Low (CMOS)	$V_{PP} = V_{CC}$	–.02		0.2	V
V_{IH}	High (TTL)	$V_{PP} = V_{CC}$	2.0		$V_{CC} + 0.5$	V
V_{IH}	High (CMOS)	$V_{PP} = V_{CC}$	$V_{CC} - 0.2$		$V_{CC} + 0.2$	V
V_{PP}	Read[8]	(Operating)	$V_{CC} - 0.7$		V_{CC}	V
Output voltage[2]						
V_{OL}	Low	$I_{OL} = 2.1mA$			0.45	V
V_{OH}	High	$I_{OH} = -400µA$	2.4			V
Capacitance[9] $T_A = 25°C$						
C_{IN}	Address and control	$V_{CC} = 5.0V$ f = 1.0MHz			6	pF
C_{OUT}	Outputs	$V_{IN} = 0V$ $V_{OUT} = 0V$			12	pF

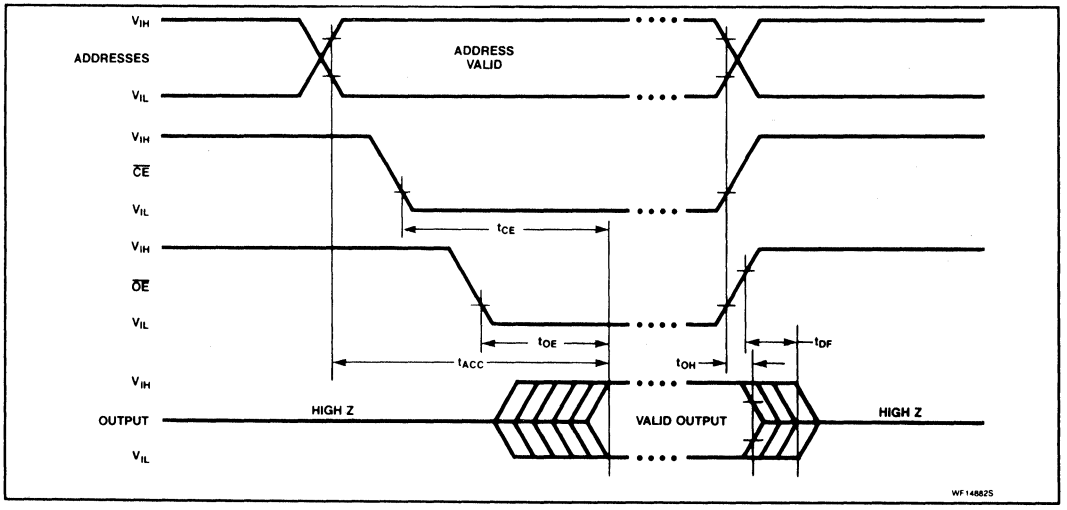
NOTES:
1. Minimum DC input voltage is –0.5V. During transitions the inputs may undershoot to –2.0V for periods less than 20ns.
2. All voltages are with respect to network ground.
3. Typical limits are at $V_{CC} = 5V$, $T_A = 25°C$.
4. TTL inputs: Spec V_{IL}, V_{IH} levels.
   CMOS inputs: GND ±0.2V to V_{CC} ±0.2V.
5. $\overline{CE}$ is V_{CC} ±0.2V. All other inputs can have any value within spec.
6. Maximum active power usage is the sum of $I_{PP} + I_{CC}$ and is measured at a frequency of 5MHz.
7. Test one output at a time, duration should not exceed 1 second.
8. V_{PP} may be one diode voltage drop below V_{CC}, and can be connected directly to V_{CC}.
9. Guaranteed by design, not 100% tested.
10. X can be V_{IH} or V_{IL}.

AC ELECTRICAL CHARACTERISTICS $0°C \le T_A \le +70°C$, $+4.5V \le V_{CC} \le +5.5V$, $R_L = 3.3k\Omega$, $C_L = 100pF$

SYMBOL	TO	FROM	27C210–15		27C210–20		UNIT
			Min	Max	Min	Max	
Access time[1]							
t_{ACC}	Output	Address		150		200	ns
t_{CE}	Output	$\overline{CE}$		150		200	ns
t_{OE}[3]	Output	$\overline{OE}$		75		85	ns
Disable time[2]							
t_{DF}[4]	Output Hi–Z	$\overline{OE}$ or $\overline{CE}$		55		60	ns
t_{OH}	Output hold	Address, $\overline{CE}$ or $\overline{OE}$	0		0		ns

NOTES:
1. AC characteristics are tested at $V_{IH} = 2.4V$ and $V_{IL} = 0.45V$. Timing measurements made at $V_{OL} = 0.8V$ and $V_{OH} = 2.0V$.
2. Guaranteed by design, not 100% tested.
3. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.
4. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

AC VOLTAGE WAVEFORMS



AC TESTING LOAD CIRCUIT

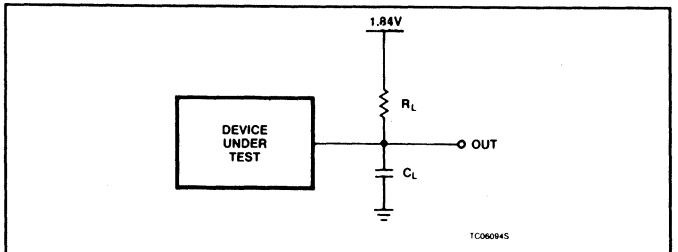


Figure 1. Test Configuration

27C210 U.V.

1 MEG Erasable CMOS EPROM (64K × 16)

Application Specific Products

Objective Specification

DESCRIPTION

Signetics 27C210 CMOS EPROM is a 1M–bit 5V only memory organized as 65,536 words of 16 bits each. It employs advanced CMOS circuitry for systems requiring low power, high–performance speeds, and immunity to noise. The 27C210 has a non–multiplexed addressing interface and is plug–compatible with the industry standard 27210.

The 27C210, available in a ceramic DIP package, achieves both high performance and low power consumption, making it ideal for high–performance, portable equipment. This device can be programmed with standard EPROM programmers.

FEATURES

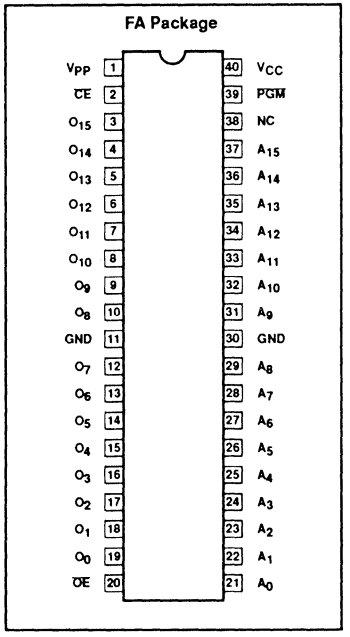
- **Low power consumption**
  - **100μA maximum CMOS standby current**
- **Quick pulse programming algorithm for high–speed production programming**
- **High–performance speeds:**
  - **27C210–15: 150ns maximum access time**
  - **27C210–20: 200ns maximum access time**
- **Noise immunity features:**
  - **±10% V_{CC} tolerance**
  - **Maximum latch–up immunity through Epitaxial processing**
- **Quick–pulse programming algorithm**

PIN DESCRIPTION

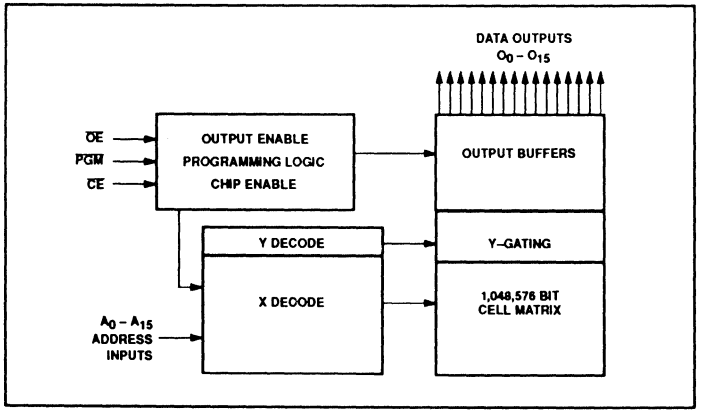
$A_0 - A_{15}$	Address
$O_0 - O_{15}$	Outputs
$\overline{OE}$	Output Enable
$\overline{CE}$	Chip Enable
$\overline{PGM}$	Program
NC	No Connection
GND	Ground
V_{PP}	Program voltage
V_{CC}	Power supply

PIN CONFIGURATION

FA Package



BLOCK DIAGRAM



1 MEG Erasable CMOS EPROM (64K × 16) 27C210 U.V.

READ MODE: 27C210

The 27C210 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins. Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

STANDBY MODE

The 27C210 has a standby mode which reduces the maximum V_{CC} current to 100µA. It is placed in the Standby mode when $\overline{CE}$ is in the High state. When in the Standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

DEVICE OPERATION

The modes of operation of the 27C210 are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A_9 for Signetics Identifier.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
40-pin CERDIP with quartz window (600mil-wide)	27C210-15 FA
40-pin CERDIP with quartz window (600mil-wide)	27C210-20 FA

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
T_A	Temperature under bias	-10 to +80	°C
T_{STG}	Storage temperature range	-65 to +125	°C
V_I, V_O	Voltage inputs and outputs	-0.6 to (V_{CC} + 1)	V
V_H	Voltage on A_9[2] (during intelligent identifier interrogation)	-0.6 to +13.0	V
V_{PP}	Voltage on V_{PP}[2] (during programming)	-0.6 to +14.0	V
V_{CC}	Supply voltage[2]	-0.6 to +7.0	V

NOTES:
1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. All voltages are with respect to network ground.

Table 1. Modes Selection

Mode \ Pins		$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A_9	A_0	V_{PP}	V_{CC}	Outputs
Read		V_{IL}	V_{IL}	X	X[1]	X	X	5.0V	D_{OUT}
Output Disable		X	V_{IH}	X	X	X	X	5.0V	Hi-Z
Standby		V_{IH}	X	X	X	X	V_{CC}	5.0V	Hi-Z
Programming		V_{IL}	V_{IH}	V_{IL}	X	X	Note 4	Note 4	D_{IN}
Program Verify		V_{IL}	V_{IL}	V_{IH}	X	X	Note 4	Note 4	D_{OUT}
Program Inhibit		V_{IH}	X	X	X	X	Note 4	Note 4	Hi-Z
Signetics	Manufactured[2]	V_{IL}	V_{IL}	X	V_H[2]	V_{IL}	V_{CC}	5.0V	FF15
Identifier	Device[3]	V_{IL}	V_{IL}	X	V_H[2]	V_{IH}	V_{CC}	5.0V	FF17

NOTES:
1. X can be V_{IL} or V_{IH}
2. V_H = 12.0V ±0.5V
3. $A_1 - A_8$, $A_{10} - A_{15}$ = V_{IL}
4. See Table 2 for V_{CC} and V_{PP} voltages.

1 MEG Erasable CMOS EPROM (64K × 16) 27C210 U.V.

DC ELECTRICAL CHARACTERISTICS $0°C \le T_A \le +70°C$, $+4.5V \le V_{CC} \le +5.5V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[3]	Max	
Input current						
I_{IH}	Leakage	$V_{IN} = 5.5V = V_{CC}$		0.01	1.0	µA
I_{IL}	Low	$V_{IL} = 0.45V$		0.01	1.0	µA
I_{PP}	V_{PP}	$V_{PP} = V_{CC}$			10	µA
Output current						
I_{OL}	Leakage	$\overline{OE}$ or $\overline{CE} = V_{IH}$			10.0	µA
		$V_{OUT} = 5.5V = V_{CC}$			10.0	µA
		$V_{OUT} = 0V = GND$			10.0	µA
I_{OS}	Short circuit[7, 9]	$V_{OUT} = 0V$			100	mA
Supply current						
I_{CC} TTL	Operating (TTL inputs)[4]	$\overline{CE} = \overline{OE} = V_{IL}$, f = 5.0MHz $V_{PP} = V_{CC}$ $O_{0-15} = 0mA$			50	mA
I_{SB} TTL	Standby (TTL inputs)[4]	$\overline{CE} = V_{IH}$			1	mA
I_{SB} CMOS	Standby (CMOS inputs)[5, 6]	$\overline{CE} = V_{IH}$			100	µA
Input voltage[2]						
V_{IL}	Low (TTL)	$V_{PP} = V_{CC}$	–0.5		0.8	V
V_{IL}	Low (CMOS)	$V_{PP} = V_{CC}$	–.02		0.2	V
V_{IH}	High (TTL)	$V_{PP} = V_{CC}$	2.0		$V_{CC} + 0.5$	V
V_{IH}	High (CMOS)	$V_{PP} = V_{CC}$	$V_{CC} - 0.2$		$V_{CC} + 0.2$	V
V_{PP}	Read[8]	(Operating)	$V_{CC} - 0.7$		V_{CC}	V
Output voltage[2]						
V_{OL}	Low	$I_{OL} = 2.1mA$			0.45	V
V_{OH}	High	$I_{OH} = -400µA$	2.4			V
Capacitance[9] $T_A = 25°C$						
C_{IN}	Address and control	$V_{CC} = 5.0V$ f = 1.0MHz			6	pF
C_{OUT}	Outputs	$V_{IN} = 0V$ $V_{OUT} = 0V$			12	pF

NOTES:
1. Minimum DC input voltage is –0.5V. During transitions the inputs may undershoot to –2.0V for periods less than 20ns.
2. All voltages are with respect to network ground.
3. Typical limits are at $V_{CC} = 5V$, $T_A = 20°C$.
4. TTL inputs: Spec V_{IL}, V_{IH} levels.
   CMOS inputs: GND ±0.2V to V_{CC} ±0.2V.
5. $\overline{CE}$ is V_{CC} ±0.2V. All other inputs can have any value within spec.
6. Maximum active power usage is the sum of $I_{P-P} + I_{CC}$ and is measured at a frequency of 5MHz.
7. Test one output at a time, duration should not exceed 1 second.
8. V_{PP} may be one diode voltage drop below V_{CC}, and can be connected directly to V_{CC}.
9. Guaranteed by design, not 100% tested.
10. X can be V_{IH} or V_{IL}.

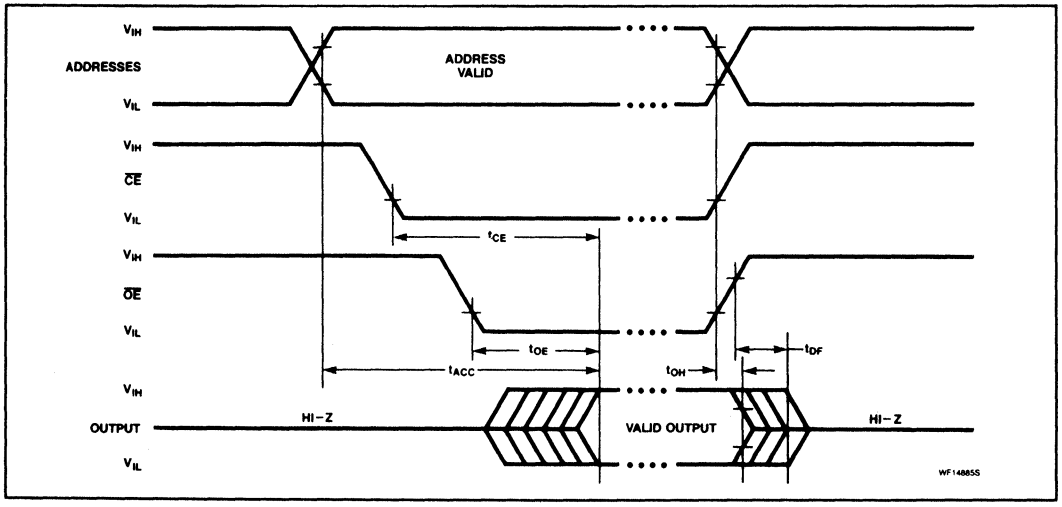
1 MEG Erasable CMOS EPROM (64K × 16) — 27C210 U.V.

AC ELECTRICAL CHARACTERISTICS $0°C \le T_A \le +70°C$, $+4.5V \le V_{CC} \le +5.5V$, $R_L = 3.3k\Omega$, $C_L = 100pF$

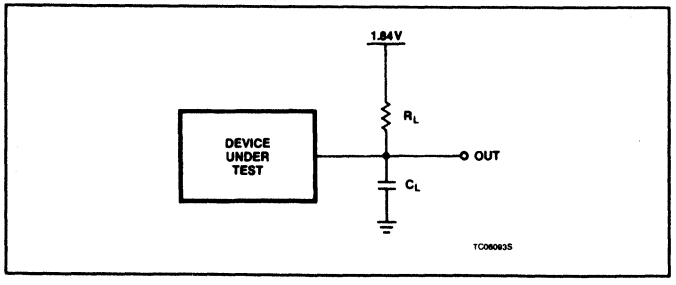
SYMBOL	TO	FROM	27C210–15		27C210–20		UNIT
			Min	Max	Min	Max	
Access time[1]							
t_{ACC}	Output	Address		150		200	ns
t_{CE}	Output	$\overline{CE}$		150		200	ns
t_{OE}[3]	Output	$\overline{OE}$		75		85	ns
Disable time[2]							
t_{DF}[4]	Output Hi–Z	$\overline{OE}$ or $\overline{CE}$		55		60	ns
t_{OH}	Output Hold	Address, $\overline{CE}$ or $\overline{OE}$	0		0		ns

NOTES:
1. AC characteristics are tested at $V_{IH} = 2.4V$ and $V_{IL} = 0.45V$. Timing measurements made at $V_{OL} = 0.8V$ and $V_{OH} = 2.0V$.
2. Guaranteed by design, not 100% tested.
3. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.
4. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

AC VOLTAGE WAVEFORMS



AC TESTING LOAD CIRCUIT



TTL MEMORIES

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64-bit TTL RAM

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310A/74S189	64-bit RAM (16 x 4) 35 ns	285
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74F410	64-bit Register stack (16 x 40) 19.5 ns	297

82S25
3101A
74S189
64-Bit TTL Bipolar RAM

Bipolar Memory Products

Product Specification

DESCRIPTION

This family of Read/Write Random Access Memories is ideal for use in scratch pad and high-speed buffer memory applications.

These products are fully decoded memory arrays with separate input and output lines. They feature PNP inputs and 1 Chip Enable line for ease of memory expansion.

During Write, the outputs of each product assume the logic state defined in the truth table.

Ordering information can be found on the following page.

The 82S25 and 74S189 devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

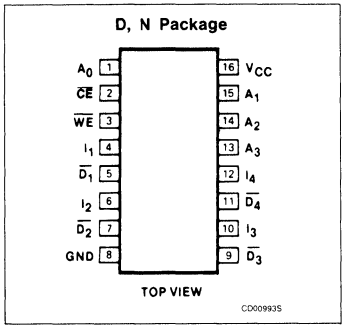
FEATURES

- **Output access time:**
  - **N82S25: 50ns max**
  - **N3101A: 35ns max**
  - **N74S189: 35ns max**
- **Power dissipation: 6.25mW/bit, typ**
- **Input loading: −100μA max**
- **On-chip address decoding**
- **One Chip Enable input**
- **Output options:**
  - **N82S25: Open-Collector**
  - **N3101A: Open-Collector**
  - **N74S189: 3-State**
- **Schottky clamped**
- **TTL compatible**

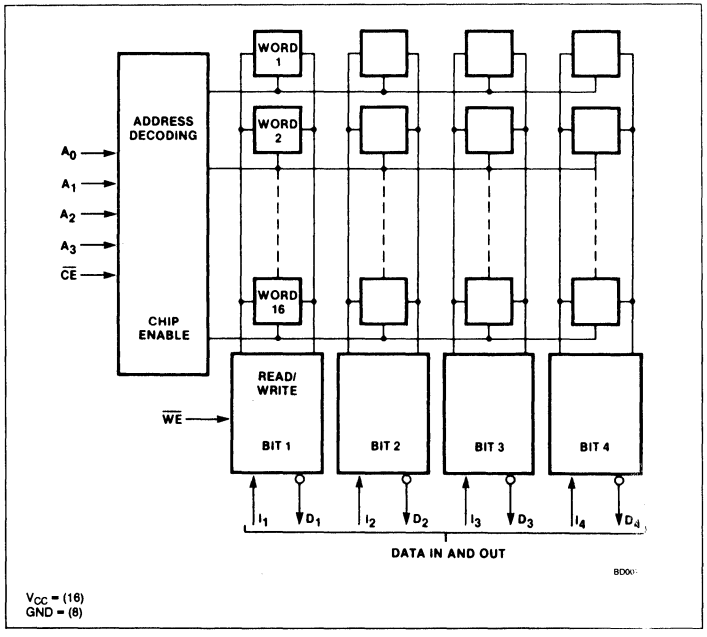
APPLICATIONS

- **Scratch pad memory**
- **Buffer memory**
- **Push down stacks**
- **Control store**

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-pin Plastic DIP 300mil-wide	N82S25 N • N3101A N • N74S189 N
16-pin Plastic Small Outline 300mil-wide	N82S25 D • N3101A D • N74S189 D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_{OH}	Output voltage High	+5.5	V_{DC}
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temperature range	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Input voltage[1]						
V_{IL}	Low	V_{CC} = 4.75V			0.8	V
V_{IH}	High	V_{CC} = 5.25V	2.0			V
V_{IC}	Clamp[7]	I_{IN} = −12mA, V_{CC} = 4.75V			−1.5	V
Output voltage[1]						
		$\overline{CE}$ = Low				
V_{OL}	Low[2,3]	I_{OUT} = 16mA, V_{CC} = 4.75V			0.45	V
V_{OH}	High (74S189)	I_{OUT} = −2mA	2.4			V
Input current[5]						
I_{IL}	Low	V_{IN} = 0.45V			−100	μA
I_{IH}	High	V_{IN} = 5.5V			10	μA
Output current[5]						
I_{OLK}	Leakage	$\overline{CE}$ = High, V_{OUT} = 5.5V, V_{CC} = 4.75V			100	μA
I_{OS}	Short circuit (74S189)	$\overline{CE}$ = Low, V_{OUT} = 0V			−100	mA
I_{OZ}	Hi-Z (74S189)	$2.4 \geq V_{OUT} \geq 0.4V$			±50	μA
Supply current[6]						
I_{CC}	82S25	V_{CC} = 5.25V			105	
	3101A	V_{CC} = 5.25V			105	mA
	74S189	V_{CC} = 5.25V			110	
Capacitance						
		V_{CC} = 5.0V				
C_{IN}	Input	V_{IN} = 2.0V		5		pF
C_{OUT}	Output	V_{OUT} = 2.0V, $\overline{CE}$ = High		8		pF

TRUTH TABLE

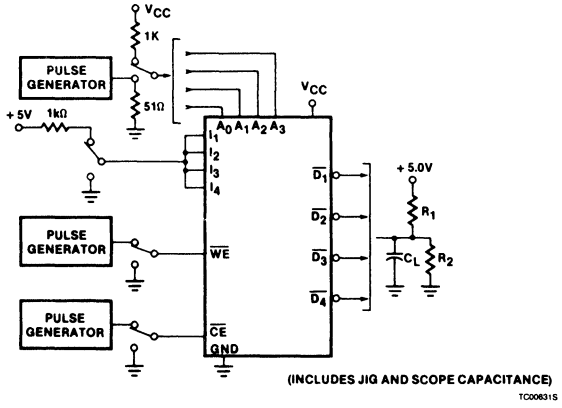
MODE	$\overline{CE}$	$\overline{WE}$	D_{IN}	82S25	3101A	74S189
				Data Out		
Read	0	1	X	Stored $\overline{Data}$	Stored $\overline{Data}$	Stored $\overline{Data}$
Write "0"	0	0	0	1	1	Hi-Z
Write "1"	0	0	1	1	1	Hi-Z
Disable	1	X	X	1	1	Hi-Z

AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TO	FROM	N82S25			N3101A, N74S189			UNIT
				Min	Typ	Max	Min	Typ	Max	
Access time										
t_{AA}	Address					50			35	ns
t_{CE}	Chip Enable					35			17	
Disable time[8]										
t_{CD}		Output	Chip Enable			35			17	ns
Response time[8]										
t_{WD}		Output	Write Enable			25			25	ns
Write recovery time										
t_{WR}						50			35	ns
Setup and hold time										
t_{WSA}[9]	Setup time	Write	Address	5			0			ns
t_{WHA}	Hold time	Enable		5			0			
t_{WSD}	Setup time	Write	Data in	30			25			ns
t_{WHD}	Hold time	Enable		5			0			
t_{WSC}	Setup time	Write	$\overline{CE}$	0			0			ns
t_{WHC}	Hold time	Enable		5			0			
Pulse width[4]										
t_{WP}[10]	Write Enable			30			25			ns

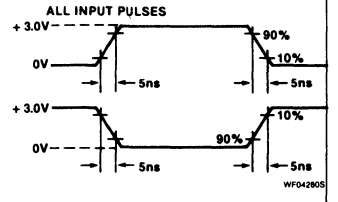
NOTES:
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. Output sink current is supplied through a resistor to V_{CC}.
3. All sense outputs in Low state.
4. To guarantee a Write into the slowest bit.
5. Positive current is defined as into the terminal referenced.
6. I_{CC} is measured with the Write enable and memory enable inputs grounded, all other inputs at 0.45V, and the outputs open.
7. Test each input one at a time.
8. Measured at a delta of 0.5V from the logic level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
9. Measured with minimum t_{WP}.
10. Measured with minimum t_{WSA}.

TEST LOAD CIRCUIT



Loading Conditions

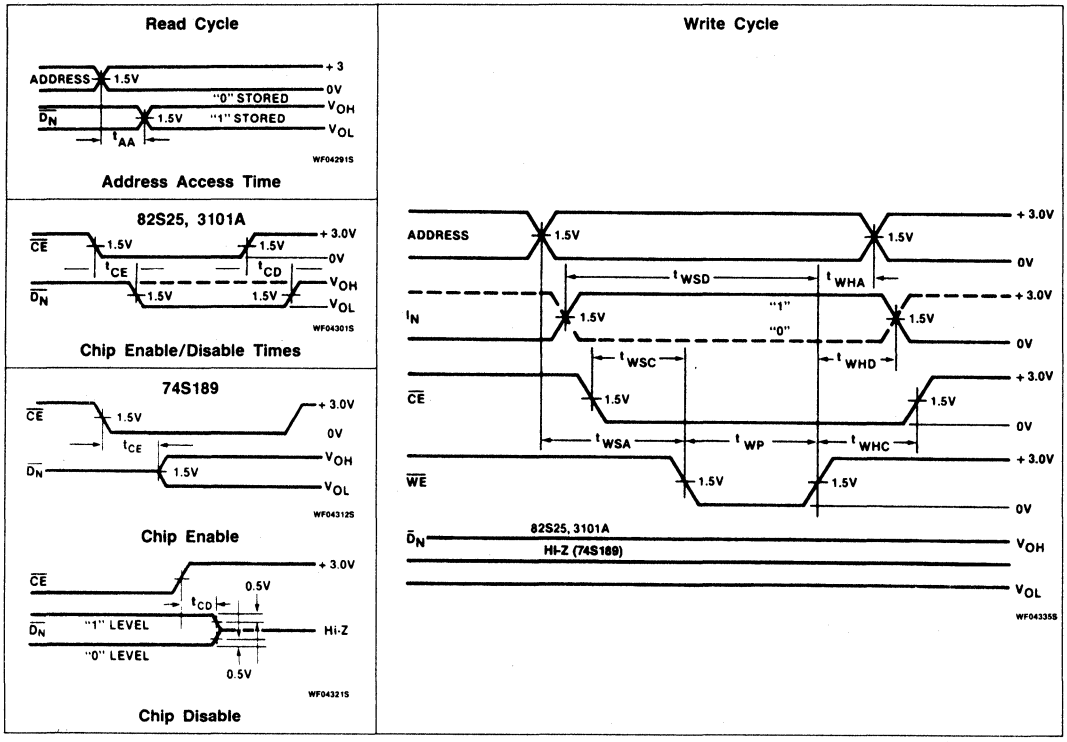
VOLTAGE WAVEFORMS



Measurements: All circuit delays are measured at the +1.5V level of inputs and output.

Input Pulses

TIMING DIAGRAM



74F189A
64-Bit TTL Bipolar RAM

Preliminary Specification

Bipolar Memory Products

DESCRIPTION

The 74F189A is a high-speed, 64-bit RAM organized as a 16-word by 4-bit array. Address inputs are buffered to minimize loading and are fully decoded on-chip. The outputs are 3-State and are in the high-impedance state whenever the Chip Select ($\overline{CE}$) input is High. The outputs are active only in the Read mode and the output data is the complement of the stored data.

Ordering information can be found on the following page.

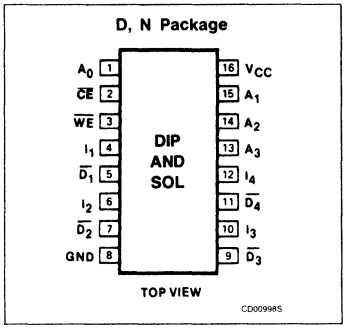
FEATURES

- **Address access time: 15ns max**
- **Power dissipation: 4.3mW/bit typ**
- **Schottky clamped TTL**
- **One Chip Enable input**
- **I/O**
  - **Inputs: PNP Buffered**
  - **Outputs: 3-State**

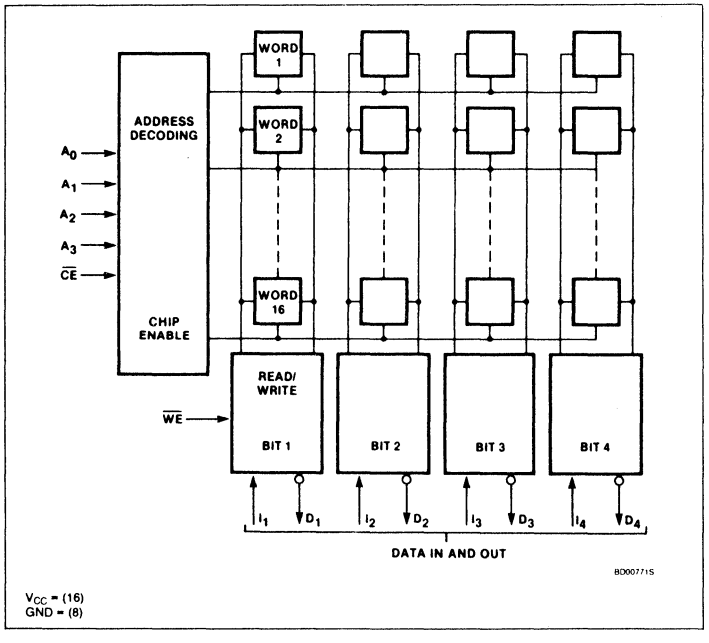
APPLICATIONS

- **Scratch pad memory**
- **Buffer memory**
- **Push down stacks**
- **Control store**

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-pin Plastic DIP 300mil-wide	N74F189A N
16-pin Plastic Small Outline 300mil-wide	N74F189A D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V_{DC}
V_{IN}	Input voltage	−0.5 to +7.0	V_{DC}
V_{OH}	Output voltage High	−0.5 to +5.5	V_{DC}
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temperature range	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[3]	Max	
Input voltage[2]						
V_{IC}[7]	Clamp	V_{CC} = 5.25V, I_I = −18mA			−1.2	V
Output voltage						
V_{OH}	High	V_{CC} = 4.75V, V_{IH} = 2.0V, V_{IL} = 0.8V I_{OH} = −3.0mA	2.4			V
V_{OL}[2,3]	Low	I_{OL} = 20mA		0.35	0.5	V
Input current						
I_{IH}	High	V_{CC} = 5.25V V_{IN} = 5.5V			40	μA
I_{IL}	Low	V_{IN} = 0.5V			0.6	μA
Output current						
I_{OZ}	Off-State	V_{CC} = 5.25V V_{IH} = 2.0V, 2.4V ≥ V_{OUT} ≥ 0.5V			±50	μA
I_{OS}	Short circuit	V_{CC} = 5.25V	−60		−150	mA
Supply current[6]						
I_{CC}		V_{CC} = 5.25V, $\overline{WE}$, $\overline{CE}$ = GND			70	mA
Capacitance						
C_{IN}	Input	V_{CC} = 5.0V V_{IN} = 2.0V		5		pF
C_{OUT}	Output	V_{OUT} = 2.0V		8		pF

TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	D_{IN}	DATA OUT
Read	0	1	X	Stored $\overline{Data}$
Write "0"	0	0	0	Hi-Z
Write "1"	0	0	1	Hi-Z
Disable	1	X	X	Hi-Z

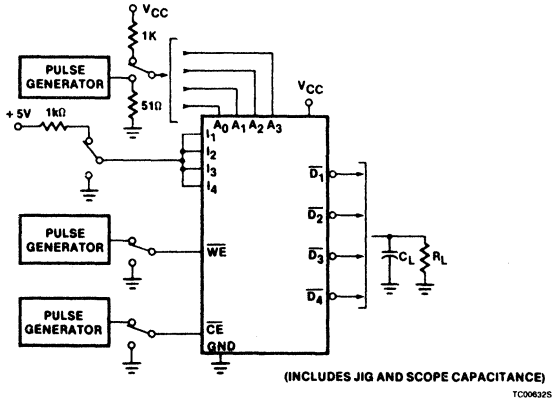
X = Don't care

AC ELECTRICAL CHARACTERISTICS $R_L = 500\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ	Max	
Access time							
t_{AA} t_{CE}	Address Chip Enable					15 13	ns
Disable time[8]							
t_{CD}		Output	Chip Enable			9	ns
Response time[8]							
t_{WD}		Output	Write Enable			9	ns
Write recovery time							
t_{WR}		Output	Write Enable			13	ns
Setup and hold time							
t_{WSA}[9] t_{WHA}	Setup time Hold time	Write Enable	Address	3 2			ns
t_{WSD} t_{WHD}	Setup time Hold time	Write Enable	Data in	13 2			ns
t_{WSC} t_{WHC}	Setup time Hold time	Write Enable	$\overline{CE}$	3 2			ns
Pulse width[4]							
t_{WP}[10]	Write Enable			10			ns

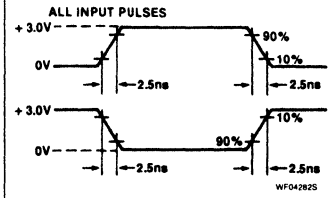
NOTES:
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. Output sink current is supplied through a resistor to V_{CC}.
3. All sense outputs in Low state.
4. To guarantee a Write into the slowest bit.
5. Positive current is defined as into the terminal referenced.
6. I_{CC} is measured with the Write enable and memory enable inputs grounded, all other inputs at 0.45V, and the output open.
7. Test each input one at a time.
8. Measured at a delta of 0.5V from the logic level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
9. Measured with minimum t_{WP}.
10. Measured with minimum t_{WSA}.

TEST LOAD CIRCUIT



Loading Conditions

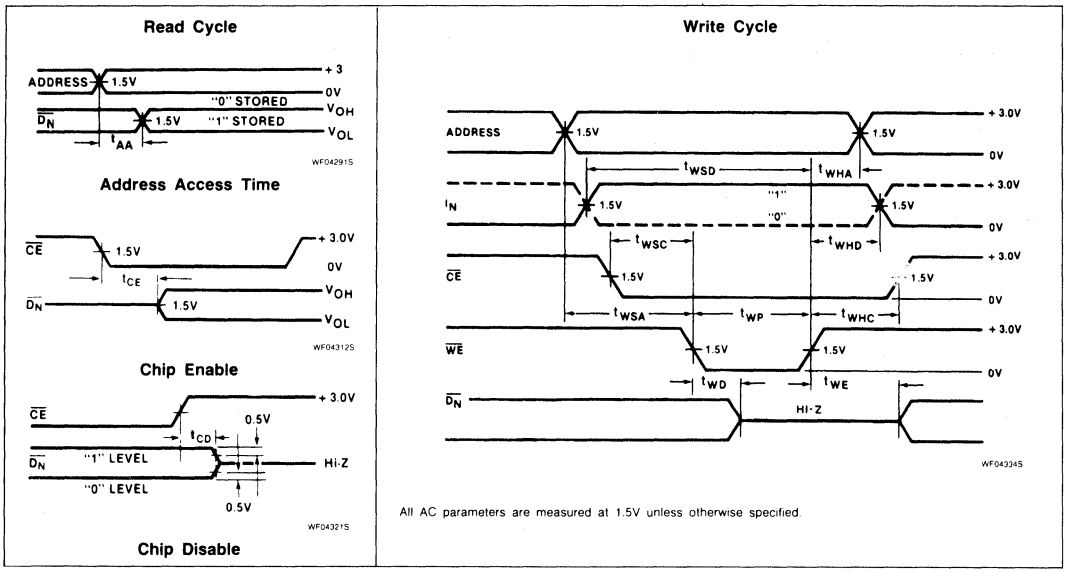
VOLTAGE WAVEFORMS



MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and output.

Input Pulses

TIMING DIAGRAM



All AC parameters are measured at 1.5V unless otherwise specified.

FAST 74F219A
64-Bit TTL Bipolar RAM

Preliminary Specification

Bipolar Memory Products

DESCRIPTION

The 74F219A is a high-speed, 64-bit RAM organized as a 16-word by 4-bit array. Address inputs are buffered to minimize loading and are fully decoded on-chip. The outputs are 3-State and are in the High-impedance state whenever the Chip Select ($\overline{CE}$) input is High. The outputs are active only in the Read mode and are of the same polarity as of the stored data.

Ordering information can be found on the following page.

FEATURES

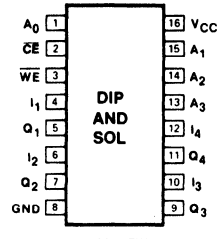
- **Address access time: 10ns max**
- **Power dissipation: 4.3mW/bit typ**
- **Schottky clamped TTL**
- **One chip enable input**
- **Non-inverting data outputs. (For inverting see 74F189A)**
- **I/O**
  - **Inputs: PNP Buffered**
  - **Outputs: 3-State**

APPLICATIONS

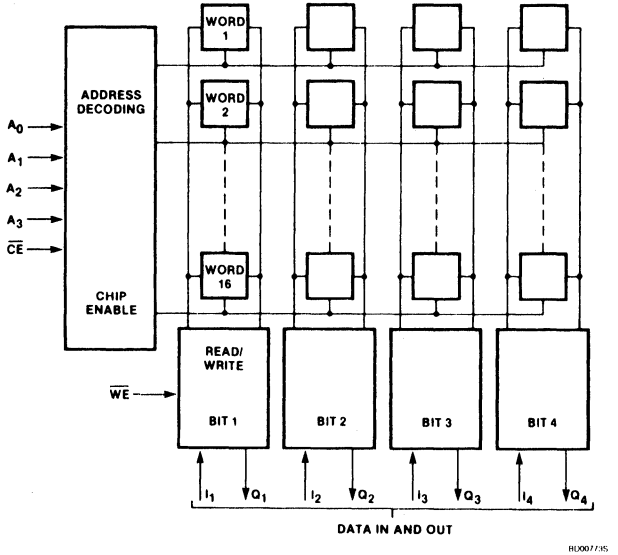
- **Scratch pad memory**
- **Buffer memory**
- **Push down stacks**
- **Control store**

PIN CONFIGURATION

D, N Packages



BLOCK DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-Pin Plastic Dual-In-Line 300mil-wide	N74F219N
16-Pin Plastic Small Outline 300mil-wide	N74F219D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V_{DC}
V_{IN}	Input voltage	−0.5 to +7.0	V_{DC}
V_{OH}	Output voltage High	−0.5 to +5.5	V_{DC}
T_A	Operating temperature range	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +70°C$, $4.75V \leq V_{CC} \leq 5.25V$.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[3]	Max	
Input voltage[2]						
V_{IC}[7]	Clamp	V_{CC} = 5.25V, I_I = −18mA			−1.2	V
Output voltage						
V_{OH}	High	V_{CC} = 4.75V, V_{IH} = 2.0V, V_{IL} = 0.8V I_{OH} = −3.0mA	2.4			V
V_{OL}[2,3]	Low	I_{OL} = 20mA		0.35	0.5	
Input current						
I_{IH}	High	V_{CC} = 5.25V V_{IN} = 5.5V			40	µA
I_{IL}	Low	V_{IN} = 0.5V			0.6	
Output current						
I_{OZ}	Off-state	V_{CC} = 5.25V V_{IH} = 2.0V, 2.4V ≥ V_{OUT} ≥ 0.5V			± 50	µA
I_{OS}[11]	Short circuit	(See Note)	−60		−150	mA
Supply current[6]						
I_{CC}		V_{CC} = 5.25V, $\overline{WE}$, $\overline{CE}$ = GND			70	mA
Capacitance						
C_{IN}	Input	V_{CC} = 5.0V V_{IN} = 2.0V		5		pF
C_{OUT}	Output	V_{OUT} = 2.0V		8		

TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	I_n	Q_n
Read	0	1	X	Same polarity as stored data
Write "0"	0	0	0	Hi-Z
Write "1"	0	0	1	Hi-Z
Disable	1	X	X	Hi-Z

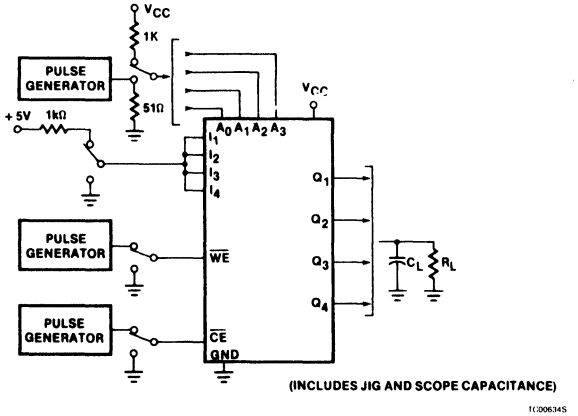
X = Don't care

AC ELECTRICAL CHARACTERISTICS $R_L = 500\Omega$, $C_L = 50pF$, $0°C \leq T_A \leq +70°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ	Max	
Access time							
t_{AA}	Address	Output	Address			10.5	ns
t_{CE}	Chip enable	Output	Chip enable			7.5	ns
Disable time[8]							
t_{CD}		Output	Chip enable			7.5	ns
Response time[8]							
t_{WD}		Output	Write enable			8.5	ns
Write recovery time							
t_{WR}		Output	Write enable			7.5	ns
Setup and hold time							
t_{WSA}[9] t_{WHA}	Setup time Hold time	Write enable	Address	0.5 0			ns
t_{WSD} t_{WHD}	Setup time Hold time	Write enable	Data in	5 0			
t_{WSC} t_{WHC}	Setup time Hold time	Write enable	$\overline{CE}$	4.5 4.5			
Pulse width							
t_{WP}[10]	Write enable			6.5			ns

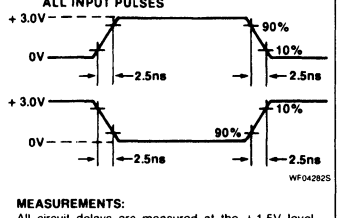
NOTES:
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. Output sink current is supplied through a resistor to V_{CC}.
3. All sense outputs in Low state.
4. To guarantee a Write into the slowest bit.
5. Positive current is defined as into the terminal referenced.
6. I_{CC} is measured with the Write enable and memory enable inputs grounded, all other inputs at 0.45V, and the output open.
7. Test each input one at a time.
8. Measured at a delta of 0.3V from the logic level with $R_1 = 500\Omega$, $R_2 = 500\Omega$ and $C_L = 50pF$.
9. Measured with minimum t_{WP}.
10. Measured with minimum t_{WSA}.
11. For I_{OS} test: V_{CC} = 5.75 V V_{OUT} = 0.5 V

TEST LOAD CIRCUIT



Loading Conditions

VOLTAGE WAVEFORM

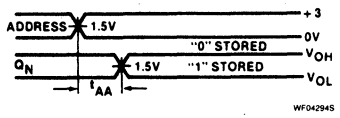


MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and output.

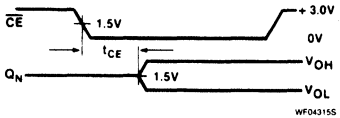
Input Pulses

TIMING DIAGRAMS

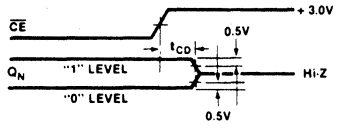
Read Cycle



Address Access Time

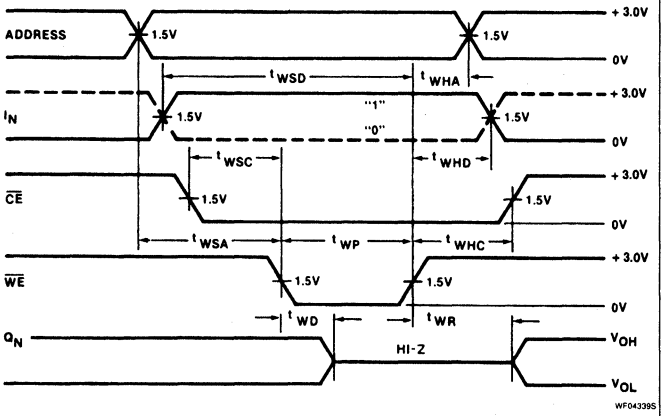


Chip Enable



Chip Disable

Write Cycle



All AC parameters are measured at 1.5V unless otherwise specified.

FAST 74F410
Register Stack — 16 X 4 RAM 3-State Output Register

Product Specification

Bipolar Memory Products

FEATURES
- **Edge-triggered output register**
- **Typical access time of 19.5ns**
- **3-State outputs**
- **Optimized for register stack operation**
- **18-pin package**

DESCRIPTION
The 74F410 is a register-oriented high-speed 64-bit Read/Write Memory organized as 16-words by 4-bits. An edge-triggered 4-bit output register allows new input data to be written while previous data is held. 3-State outputs are provided for maximum versatility. The 74F410 is fully compatible with all TTL families.

TYPE	TYPICAL ACCESS TIME	TYPICAL SUPPLY CURRENT (TOTAL)
74F410	19.5ns	45mA

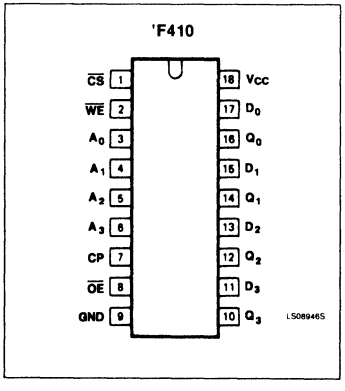
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
18-Pin Plastic Dual-In-Line 300mil-wide	N74F410N

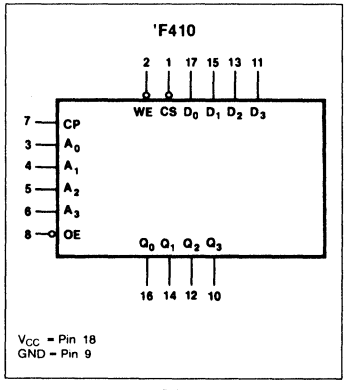
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_0 - A_3$	Address Inputs	1.0/1.0	20μA/0.6mA
$D_0 - D_3$	Data Inputs	1.0/1.0	20μA/0.6mA
$\overline{CS}$	Chip Select Input (active-Low)	1.0/2.0	20μA/1.2mA
$\overline{OE}$	Output Enable Input (active-Low)	1.0/1.0	20μA/0.6mA
$\overline{WE}$	Write Enable Input (active-Low)	1.0/1.0	20μA/0.6mA
CP	Clock Input (outputs change on Low-to-High transition)	1.0/2.0	20μA/1.2mA
$Q_0 - Q_3$	Data outputs	150/40	3mA/24mA

PIN CONFIGURATION



LOGIC SYMBOL



Register Stack — 16 X 4 RAM
3-State Output Register

FAST 74F410

FUNCTIONAL DESCRIPTION

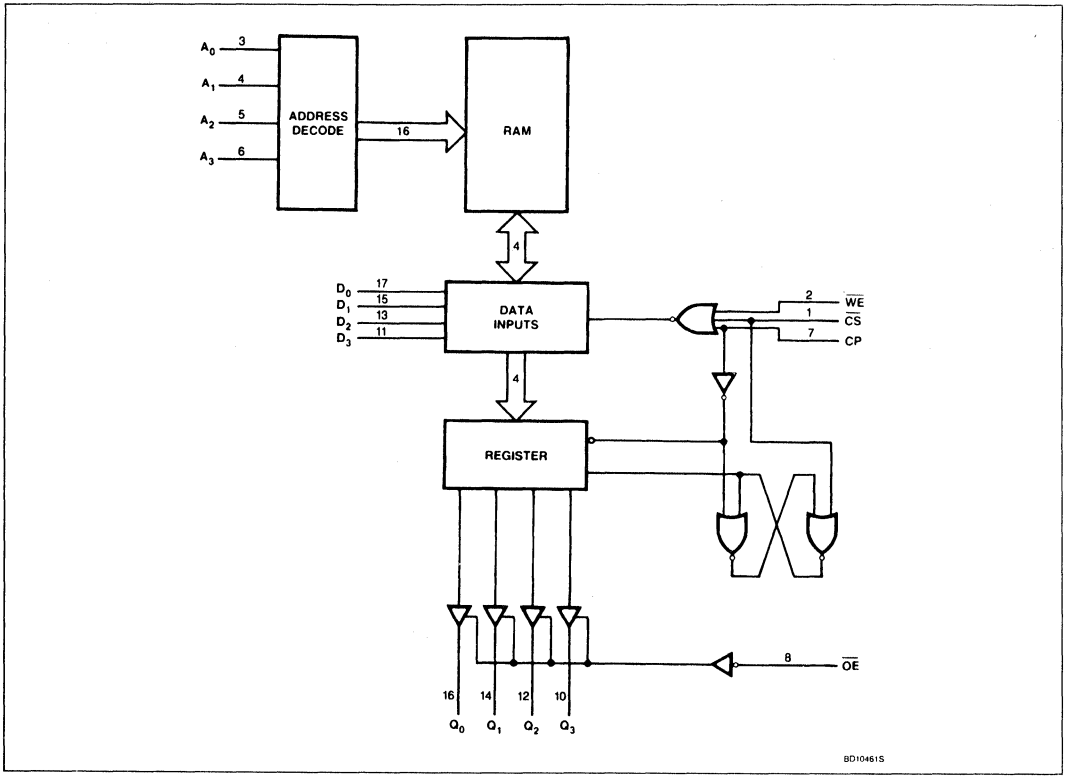
Write Operation — When the three control inputs, Write Enable ($\overline{WE}$), Chip Select ($\overline{CS}$), and Clock (CP), are Low the information on the data inputs ($D_0 - D_3$) is written into the memory location selected by the address inputs ($A_0 - A_3$). If the input data changes while $\overline{WE}$, $\overline{CS}$, and CP are Low, the contents of the selected memory location follow these changes, provided setup and hold time criteria are met.

Read Operation — Whenever $\overline{CS}$ is Low, $\overline{WE}$ is High, and CP goes from Low-to-High, the contents of the memory location selected by the address inputs ($A_0 - A_3$) are edge-triggered into the Output Register.

When $\overline{WE}$ is Low, $\overline{CS}$ is Low, and CP goes from Low-to-High, the data at the Data Inputs is edge-triggered into the output register.

The ($\overline{OE}$) input controls the output buffers. When $\overline{OE}$ is High the four outputs ($Q_0 - Q_3$) are in a high-impedance or OFF-state; when $\overline{OE}$ is Low, the outputs are determined by the state of the Output Register.

BLOCK DIAGRAM



Register Stack — 16 X 4 RAM 3-State Output Register

FAST 74F410

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = MAX	±10% V_{CC}	2.4			V
					±5% V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = MAX	±10% V_{CC}		0.35	0.5	V
					±5% V_{CC}		0.35	0.5	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}					−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current	$A_0 - A_3$, $D_0 - D_3$, $\overline{WE}$, $\overline{OE}$	V_{CC} = MAX, V_I = 0.5V					−0.6	mA
		CP, $\overline{CS}$						−1.2	mA
I_{OZH}	OFF-state output current, High-level voltage applied		V_{CC} = MAX, V_{OUT} = 2.7V					50	μA
I_{OZL}	OFF-state output current, Low-level voltage applied		V_{CC} = MAX, V_{OUT} = 0.5V					−50	μA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			−60		−150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX				45	70	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value under the recommended operating conditions for the applicable conditions.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} should be performed last.

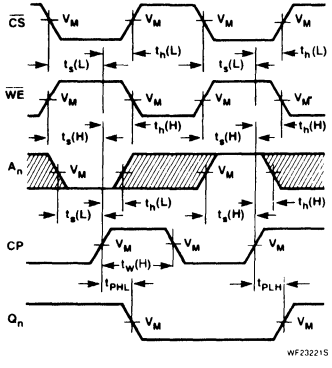
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay CP ↑ to Q_n	Waveform 1	4.0 4.5	6.5 6.5	8.5 9.0	3.5 4.0	9.5 10.0	ns
t_{PZH} t_{PZL}	Enable time $\overline{OE}$ to Q_n	Waveform 3, 4	3.0 4.5	4.5 6.0	7.5 9.0	2.5 3.5	8.5 9.5	ns
t_{PHZ} t_{PLZ}	Disable time $\overline{OE}$ to Q_n	Waveform 3, 4	2.0 2.0	3.5 3.5	6.0 6.5	1.5 2.0	6.5 7.0	ns

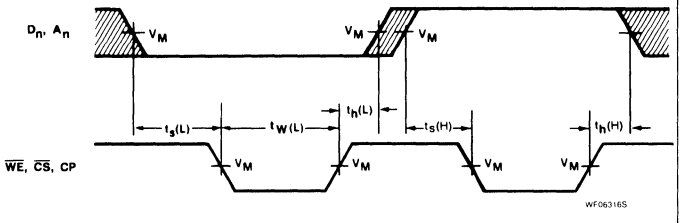
AC SETUP AND HOLD REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
READ MODE								
$t_s(L)$	Setup time Low $\overline{CS}$ to CP ↑	Waveform 1	4.0			4.5		ns
$t_h(L)$	Hold time Low $\overline{CS}$ to CP ↑	Waveform 1	3.5			4.5		ns
$t_s(H)$ $t_s(L)$	Setup time High or Low A_n to CP ↑	Waveform 1	13.0 13.0			15.0 15.0		ns
$t_h(H)$ $t_h(L)$	Hold time High or Low A_n to CP ↑	Waveform 1	0 0			0 0		ns
$t_s(H)$	Setup time High $\overline{WE}$ to CP ↑	Waveform 1	13.0			15.0		ns
$t_h(H)$	Hold time High $\overline{WE}$ to CP ↑	Waveform 1	0			0		ns
$t_w(H)$	CP pulse width, High	Waveform 1	5.0			6.0		ns
WRITE MODE								
$t_s(H)$ $t_s(L)$	Setup time High or Low A_n to $\overline{WE}$, $\overline{CS}$, CP	Waveform 2	0 0			0 0		ns
$t_h(H)$ $t_h(L)$	Hold time High or Low A_n to $\overline{WE}$, $\overline{CS}$, CP	Waveform 2	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time High or Low D_n to $\overline{WE}$, $\overline{CS}$, CP	Waveform 2	6.0 6.0			8.0 8.0		ns
$t_h(H)$ $t_h(L)$	Hold time High or Low D_n to $\overline{WE}$, $\overline{CS}$, CP	Waveform 2	0 0			0 0		ns
t_w	$\overline{WE}$ pulse width, Low	Waveform 2	7.0			8.0		ns
t_w	$\overline{CS}$ pulse width, Low	Waveform 2	6.0			7.0		ns
t_w	CP pulse width, Low	Waveform 2	7.0			8.0		ns

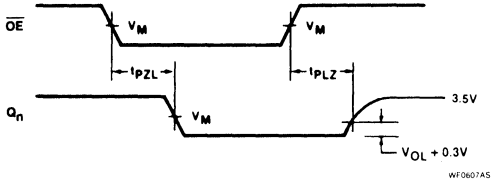
AC WAVEFORMS



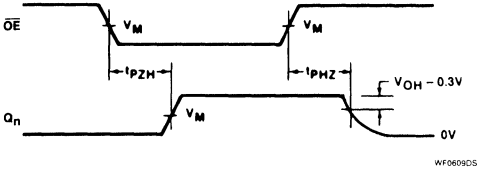
Waveform 1. Read Cycle Timing



Waveform 2. Write Cycle Timing

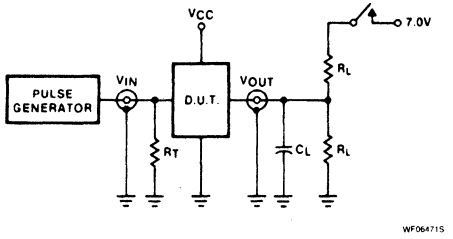


Waveform 3. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

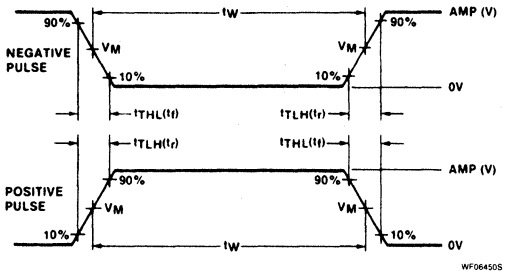


Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS
R_L = Load resistor to GND; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

256-bit TTL RAM

		page
82S16	256-bit RAM (256 x 1) 50 ns	305
82LS16	256-bit RAM (256 x 1) 40 ns	309
74S301	256-bit RAM (256 x 1) 50 ns	313
74LS301	256-bit RAM (256 x 1) 40 ns	317

82S16
256-Bit TTL Bipolar RAM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82S16 is a Read/Write memory array which features 3-State outputs for optimization of word expansion in bused organizations. Memory expansion is further enhanced by full on-chip address decoding, 3 Chip Enable inputs and PNP input transistors which reduce input loading.

During Write operation, the logical state of the output follows the complement of the data input being written. This feature allows faster execution of Write/Read cycles, enhancing the performance of systems utilizing indirect addressing modes, and/or requiring immediate verification following Write cycle.

The 82S16 has fast Read access and Write cycle times, and thus is ideally suited in high-speed memory applications such as cache, buffers, scratch pads, writable control stores, etc.

Ordering information can be found on the following page.

The 82S16 devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data book.

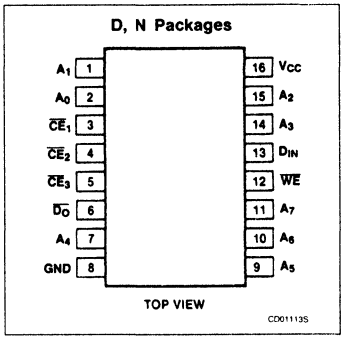
FEATURES

- **Address access time: 50ns max**
- **Write cycle time: 50ns max**
- **Power dissipation: 1.5mW/bit typ**
- **Input loading: −100μA max**
- **Output follows complement of data input during Write**
- **Three Chip Enable inputs**
- **On-chip address decoding**
- **Output: 3-State**
- **Schottky clamped**
- **TTL compatible**

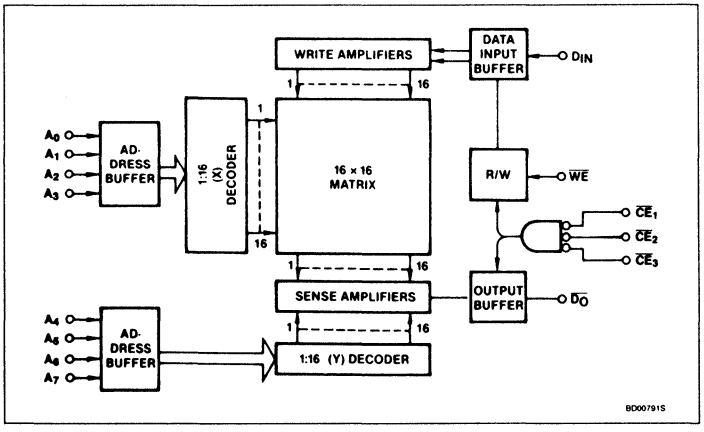
APPLICATIONS

- **Buffer memory**
- **Writable control store**
- **Memory mapping**
- **Push down stack**
- **Scratch pad**

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-pin Plastic DIP 300mil-wide	N82S16 N
16-pin Plastic Small Outline 300mil-wide	N82S16 D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_{OUT}	Output voltage High (open-collector)	+5.5	V_{DC}
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temperature range	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[1]	Max	
Input voltage[2]						
V_{IH}	High	V_{CC} = Max	2.0			V
V_{IL}	Low	V_{CC} = Min			0.8	V
V_{IC}	Clamp[3]	V_{CC} = Min, I_{IN} = −12mA		−1.0	−1.5	V
Output voltage[2]						
		V_{CC} = Min				
V_{OH}	High	I_{OH} = −3.2mA	2.6			V
V_{OL}	Low[5]	I_{OL} = 16mA		0.35	0.45	V
Input current[3]						
		V_{CC} = Max				
I_{IH}	High	V_{IN} = 5.5V		1	25	μA
I_{IL}	Low	V_{IN} = 0.45V		−10	−100	μA
Output current						
I_{OZ}	Hi-Z state[6]	V_{OUT} = 5.5V		1	40	μA
		V_{OUT} = 0.45V		−1	−40	
I_{OS}	Short circuit[7]	V_{CC} = Max, V_O = 0V	−15		−70	mA
Supply current[8]						
I_{CC}		V_{CC} = 5.25V		80	115	mA
Capacitance						
		V_{CC} = 5.0V				
C_{IN}	Input	V_{IN} = 2.0V		5		pF
C_{OUT}	Output	V_{OUT} = 2.0V		8		pF

TRUTH TABLE

MODE	$\overline{CE}$*	$\overline{WE}$	D_{IN}	D_{OUT}
Read	0	1	X	Stored $\overline{Data}$
Write "0"	0	0	0	1
Write "1"	0	0	1	0
Disabled	1	X	X	Hi-Z

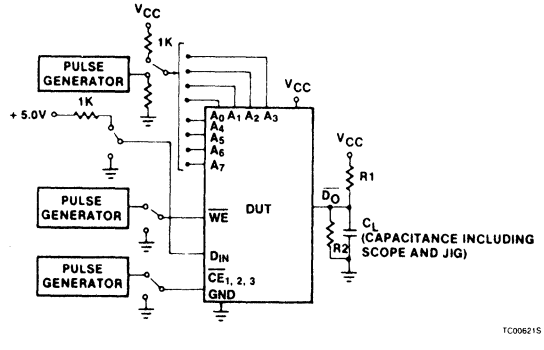
*"0" = All $\overline{CE}$ inputs Low; "1" = One or more $\overline{CE}$ inputs High. X = Don't care.

AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[1]	Max	
Access time							
t_{AA} t_{CE}	Address Chip Enable	Output Output	Address Chip Enable		40 30	50 40	ns
Disable time[10]							
t_{CD} t_{WD}	 Valid time	Output Output	Chip Enable Write Enable		30 30	40 40	ns
Setup and hold time							
t_{WSA}[11] t_{WHA}	Setup time Hold time	Write Enable	Address	15 5	5 0		ns
t_{WSD} t_{WHD}	Setup time Hold time	Write Enable	Data in	40 5	30 0		ns
t_{WSC} t_{WHC}	Setup time Hold time	Write Enable	$\overline{CE}$	10 5	0 0		ns
Pulse width[9]							
t_{WP}[12]	Write Enable			30	15		ns

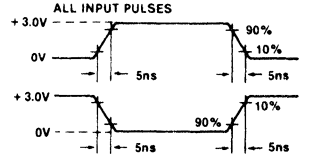
NOTES:
1. All typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
2. All voltage values are with respect to network ground terminal.
3. Test each input one at a time.
4. Measured with a logic Low stored and V_{IL} applied to $\overline{CE}_1$, $\overline{CE}_2$ and $\overline{CE}_3$.
5. Measured with a logic High stored. Output sink current is supplied through a resistor to V_{CC}.
6. Measured with V_{IH} applied to $\overline{CE}_1$, $\overline{CE}_2$ and $\overline{CE}_3$.
7. Duration of the short-circuit should not exceed 1 second.
8. I_{CC} is measured with the Write enable and memory enable inputs grounded, all other inputs at 0.45V, and the output open.
9. Minimum required to guarantee a Write into the slowest bit.
10. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
11. Measured with minimum t_{WP}.
12. Measured with minimum t_{WSA}.

TEST LOAD CIRCUIT



Loading Condition

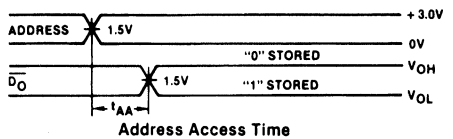
VOLTAGE WAVEFORMS



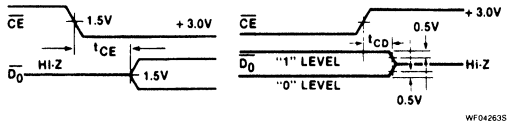
Measurements:
All circuit delays are measured at the+ 1.5 level of inputs and output.

Input Pulses

TIMING DIAGRAM

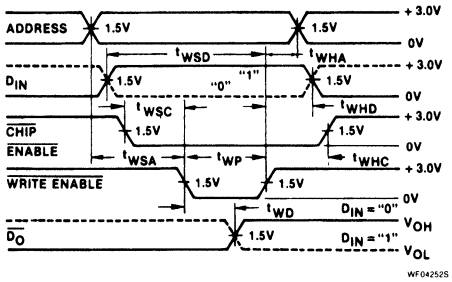


Address Access Time



Chip Enable Chip Disable

Read Cycle



NOTES:
All inputs $t_r = t_f = 5ns$ (10% to 90%)
All AC parameters are measured at 1.5V unless otherwise specified.

Write Cycle

MEMORY TIMING DEFINITIONS

SYMBOL	PARAMETER
t_{CE}	Delay between beginning of Chip Enable Low (with Address valid) and when Data Output becomes valid.
t_{CD}	Delay between when Chip Enable becomes High and Data Output is in off-state.
t_{AA}	Delay between beginning of valid Address (with Chip Enable Low) and when Data Output becomes valid.
t_{WSC}	Required delay between beginning of valid Chip Enable and beginning of Write Enable pulse.
t_{WHD}	Required delay between end of Write Enable pulse and end of valid input data.
t_{WP}	Width of Write Enable pulse.
t_{WSA}	Required delay between beginning of valid Address and beginning of Write Enable pulse.
t_{WSD}	Required delay between beginning of valid Data Input and end of Write Enable pulse.
t_{WD}	Delay between beginning of Write Enable pulse and when Data Output reflects complement of Data Input.
t_{WHC}	Required delay between end of Write Enable pulse and end of Chip Enable.
t_{WHA}	Required delay between end of Write Enable pulse and end of valid Address.

82LS16
256-Bit TTL Bipolar RAM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82LS16 is a Read/Write memory array which features 3-State outputs for optimization of word expansion in bused organizations. Memory expansion is further enhanced by full on-chip address decoding, 3 Chip Enable inputs and PNP input transistors which reduce input loading.

During Write operation, the logical state of the output follows the complement of the data input being written. This feature allows faster execution of Write/Read cycles, enhancing the performance of systems utilizing indirect addressing modes, and/or requiring immediate verification following Write cycle.

The 82LS16 has fast Read access and Write cycle times, as well as low power requirements and thus is ideally suited in high-speed memory applications such as cache, buffers, scratch pads, writable control stores, where power limitations are of major concern.

Ordering information can be found on the following page.

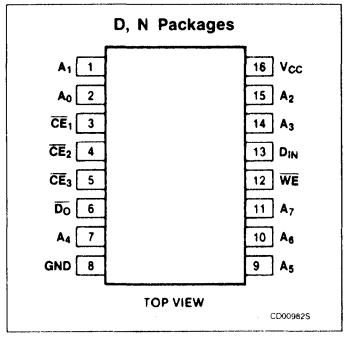
FEATURES

- **Address access time: 40ns max**
- **Write cycle time: 45ns max**
- **Power dissipation: 0.98mW/bit typ**
- **Input loading: −100μA max**
- **Output follows complement of data input during Write**
- **On-chip address decoding**
- **Three Chip Enable inputs**
- **Output: 3-State**
- **Schottky clamped**
- **TTL compatible**

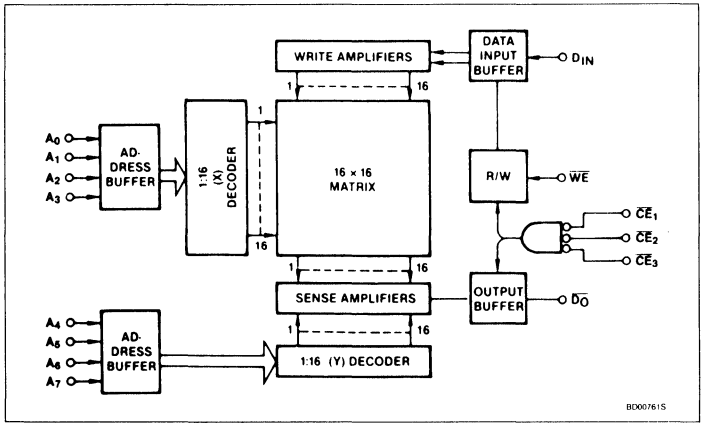
APPLICATIONS

- **Buffer memory**
- **Writable control store**
- **Memory mapping**
- **Push down stack**
- **Scratch pad**

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-pin Plastic DIP 300mil-wide	N82LS16 N
16-pin Plastic Small Outline 300mil-wide	N82LS16 D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_{OUT}	Output voltage High (open-collector)	+5.5	V_{DC}
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temperature range	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[1]	Max	
Input voltage[2]						
V_{IH}	High	V_{CC} = 5.25V	2.0			V
V_{IL}	Low	V_{CC} = 4.75V			0.8	V
V_{IC}	Clamp[3]	V_{CC} = 4.75V, I_{IN} = −12mA		−1.0	−1.5	V
Output voltage[2]						
V_{OH}	High	V_{CC} = 4.75V, I_{OH} = −3.2mA	2.6			V
V_{OL}	Low[5]	I_{OL} = 16mA		0.35	0.45	V
Input current[3]						
I_{IH}	High	V_{CC} = 5.25V, V_{IN} = 5.5V		1	25	μA
I_{IL}	Low	V_{IN} = 0.45V		−10	−100	μA
Output current						
I_{OZ}	Hi-Z state[6]	V_{OUT} = 5.5V		1	40	μA
		V_{OUT} = 0.45V		−1	−40	
I_{OS}	Short circuit[7]	V_{CC} = 5.25V, V_O = 0V	−15		−70	mA
Supply current[8]						
I_{CC}		V_{CC} = 5.25V		50	70	mA
Capacitance						
C_{IN}	Input	V_{CC} = 5.0V, V_{IN} = 2.0V		5		pF
C_{OUT}	Output	V_{OUT} = 2.0V		8		pF

TRUTH TABLE

MODE	$\overline{CE}$*	$\overline{WE}$	D_{IN}	D_{OUT}
Read	0	1	X	Stored $\overline{Data}$
Write "0"	0	0	0	1
Write "1"	0	0	1	0
Disabled	1	X	X	Hi-Z

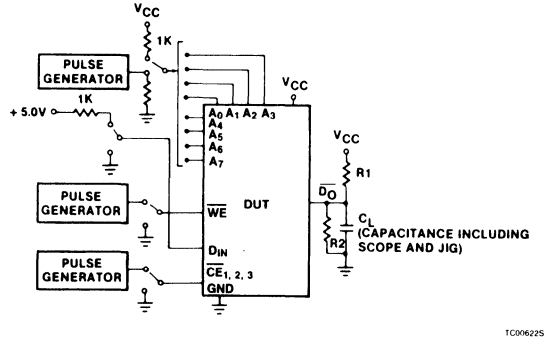
*"0" = All $\overline{CE}$ inputs Low; "1" = One or more $\overline{CE}$ inputs High. X = Don't care.

AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[1]	Max	
Access time							
t_{AA}	Address	Output	Address		30	40	ns
t_{CE}	Chip Enable	Output	Chip Enable		15	25	
Disable time[10]							
t_{CD}		Output	Chip Enable		15	25	ns
t_{WD}	Valid time	Output	Write Enable		30	40	
Setup and hold time							
t_{WSA}[11]	Setup time	Write Enable	Address	0	−5		ns
t_{WHA}	Hold time			0	−5		
t_{WSD}	Setup time	Write Enable	Data in	25	15		ns
t_{WHD}	Hold time			0	−5		
t_{WSC}	Setup time	Write Enable	$\overline{CE}$	0	−5		ns
t_{WHC}	Hold time			0	−5		
Pulse width[9]							
t_{WP}[12]	Write Enable			25	15		ns

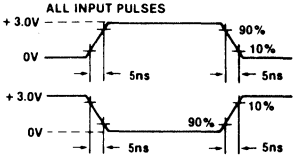
NOTES:
1. All typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
2. All voltage values are with respect to network ground terminal.
3. Test each input one at a time.
4. Measured with a logic Low stored and V_{IL} applied to $\overline{CE}_1$, $\overline{CE}_2$ and $\overline{CE}_3$.
5. Measured with a logic High stored. Output sink current is supplied through a resistor to V_{CC}.
6. Measured with V_{IH} applied to $\overline{CE}_1$, $\overline{CE}_2$ and $\overline{CE}_3$.
7. Duration of the short-circuit should not exceed 1 second.
8. I_{CC} is measured with the Write enable and memory enable inputs grounded, all other inputs at 0.45V, and the output open.
9. Minimum required to guarantee a Write into the slowest bit.
10. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
11. Measured with minimum t_{WP}.
12. Measured with minimum t_{WSA}.

TEST LOAD CIRCUIT



Loading Condition

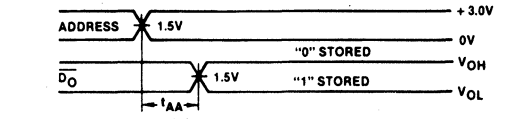
VOLTAGE WAVEFORMS



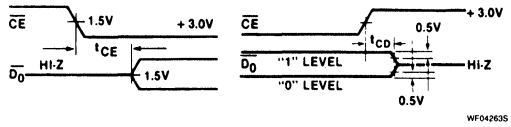
Measurements:
All circuit delays are measured at the+ 1.5 level of inputs and output.

Input Pulses

TIMING DIAGRAM

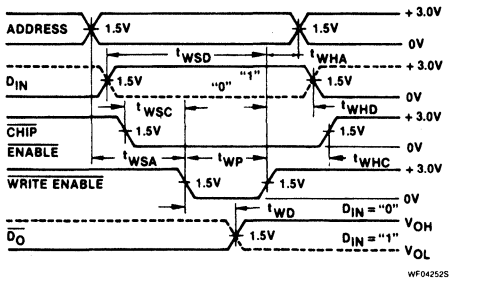


Address Access Time



Chip Enable Chip Disable

Read Cycle



NOTES:
All inputs $t_r = t_f = 5ns$ (10% to 90%)
All AC parameters are measured at 1.5V unless otherwise specified.

Write Cycle

MEMORY TIMING DEFINITIONS

SYMBOL	PARAMETER
t_{CE}	Delay between beginning of Chip Enable Low (with Address valid) and when Data Output becomes valid.
t_{CD}	Delay between when Chip Enable becomes High and Data Output is in off-state.
t_{AA}	Delay between beginning of valid Address (with Chip Enable Low) and when Data Output becomes valid.
t_{WSC}	Required delay between beginning of valid Chip Enable and beginning of Write Enable pulse.
t_{WHD}	Required delay between end of Write Enable pulse and end of valid input data.
t_{WP}	Width of Write Enable pulse.
t_{WSA}	Required delay between beginning of valid Address and beginning of Write Enable pulse.
t_{WSD}	Required delay between beginning of valid Data Input and end of Write Enable pulse.
t_{WD}	Delay between beginning of Write Enable pulse and when Data Output reflects complement of Data Input.
t_{WHC}	Required delay between end of Write Enable pulse and end of Chip Enable.
t_{WHA}	Required delay between end of Write Enable pulse and end of valid Address.

74S301
256-Bit TTL Bipolar RAM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 74S301 is a Read/Write memory array which features an Open-Collector output for optimization of word expansion in bused organizations. Memory expansion is further enhanced by full on-chip address decoding, 3 Chip Enable inputs and PNP input transistors, which reduce input loading.

The additional feature of output blanking during Write ($\overline{D_O}$ terminal High) permits $\overline{D_O}$ and D_{IN} terminals to share a common I/O line to reduce system interconnections. These devices have fast Read access and Write cycle times, and thus are ideally suited in high speed memory applications such as cache, buffers, scratch pads, writable control stores, etc.

Ordering information can be found on the following page.

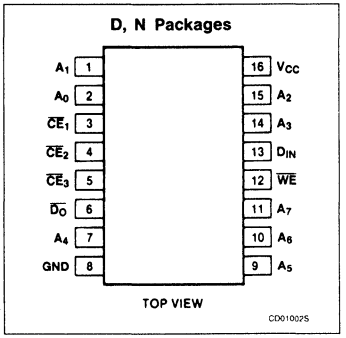
FEATURES

- **Address access time: 50ns max**
- **Write cycle time: 55ns max**
- **Power dissipation: 1.5mW/bit typ**
- **Input loading: −100μA max**
- **Output blanking during Write**
- **On-chip address decoding**
- **Schottky clamped**
- **TTL compatible**
- **Three Chip Enable inputs**
- **Output: Open-Collector**

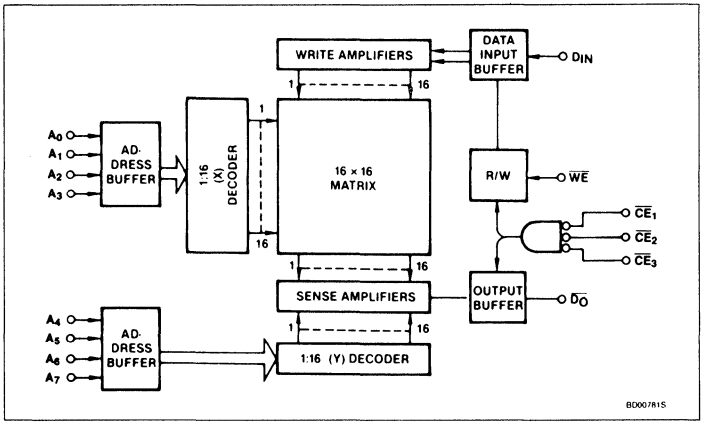
APPLICATIONS

- **Buffer memory**
- **Writable control store**
- **Memory mapping**
- **Push down stack**
- **Scratch pad**

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-pin Plastic DIP 300mil-wide	N74S301 N
16-pin Plastic Small Outline 300mil-wide	N74S301 D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_{OUT}	Output voltage High (open-collector)	+5.5	V_{DC}
T_A	Operating temperature Range	0 to +75	°C
T_{STG}	Storage temperature Range	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[1]	Max	
Input voltage						
V_{IL}	Low	V_{CC} = 4.75V			0.8	V
V_{IH}	High	V_{CC} = 5.25V	2.0			V
V_{IC}	Clamp[3]	V_{CC} = 4.75V, I_{IN} = −12mA		−1.0	−1.2	V
Output voltage						
V_{OL}	Low[5]	V_{CC} = 4.75V, I_{OL} = 16mA		0.35	0.45	V
Input current						
I_{IL}	Low	V_{CC} = 5.25V, V_{IL} = 0.45V			−100	μA
I_{IH}	High	V_{IH} = 2.7V			25	μA
Output current						
I_{OLK}	Leakage	V_{IH} = 2V, V_O = 5.5V			40	μA
Supply current[8]						
I_{CC}		V_{CC} = 5.25V, T_A = +125°C		80	130	mA
Capacitance						
C_{IN}	Input	V_{CC} = 5.0V, V_{IN} = 2.0V		5		pF
C_{OUT}	Output	V_{OUT} = 2.0V		8		pF

TRUTH TABLE

MODE	$\overline{CE}$*	$\overline{WE}$	D_{IN}	D_{OUT}
Read	0	1	X	Stored $\overline{Data}$
Write "0"	0	0	0	1
Write "1"	0	0	1	1
Disabled	1	X	X	1

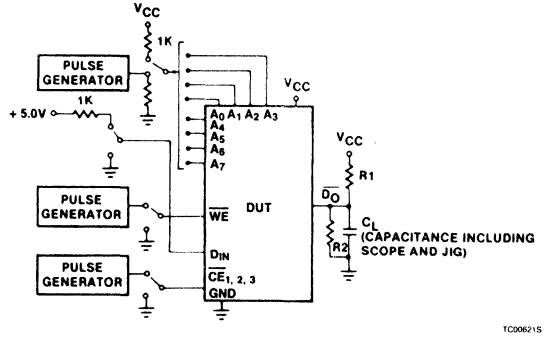
*"0" = All $\overline{CE}$ inputs Low: "1" = One or more $\overline{CE}$ inputs High.
X = Don't care.

AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[1]	Max	
Access time							
t_{AA} t_{CE}	Address Chip Enable	Output Output	Address Chip Enable		40 30	50 40	ns
Disable time[10]							
t_{CD} t_{WD}	Valid time	Output Output	Chip Enable Write Enable		30 30	40 40	ns
Setup and hold time							
t_{WSA}[11] t_{WHA}	Setup time Hold time	Write Enable	Address	20 5	5 0		ns
t_{WSD} t_{WHD}	Setup time Hold time	Write Enable	Data in	40 5	30 0		ns
t_{WSC} t_{WHC}	Setup time Hold time	Write Enable	$\overline{CE}$	10 5	0 0		ns
Pulse width[9]							
t_{WP}[12]	Write Enable			30	15		ns

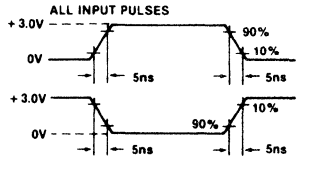
NOTES:
1. All typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
2. All voltage values are with respect to network ground terminal.
3. Test each input one at a time.
4. Measured with a logic Low stored and V_{IL} applied to $\overline{CE}_1$, $\overline{CE}_2$ and $\overline{CE}_3$.
5. Measured with a logic High stored. Output sink current is supplied through a resistor to V_{CC}.
6. Measured with V_{IH} applied to $\overline{CE}_1$, $\overline{CE}_2$ and $\overline{CE}_3$.
7. Duration of the short-circuit should not exceed 1 second.
8. I_{CC} is measured with the Write enable and memory enable inputs grounded, all other inputs at 0.45V, and the output open.
9. Minimum required to guarantee a Write into the slowest bit.
10. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
11. Measured with minimum t_{WP}.
12. Measured with minimum t_{WSA}.

TEST LOAD CIRCUIT



Loading Condition

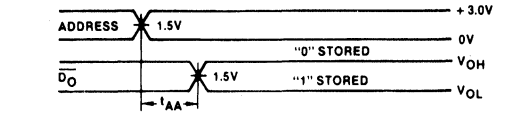
VOLTAGE WAVEFORMS



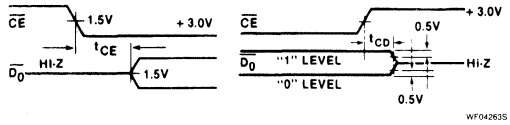
MEASUREMENTS:
All circuit delays are measured at the+1.5 level of inputs and output.

Input Pulses

TIMING DIAGRAM

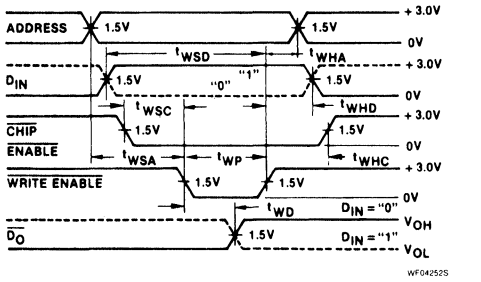


Address Access Time



Chip Enable Chip Disable

Read Cycle



NOTES:
All inputs $t_r = t_f = 5ns$ (10% to 90%)
All AC parameters are measured at 1.5V unless otherwise specified.

Write Cycle

MEMORY TIMING DEFINITIONS

SYMBOL	PARAMETER
t_{CE}	Delay between beginning of Chip Enable Low (with Address valid) and when Data Output becomes valid.
t_{CD}	Delay between when Chip Enable becomes High and Data Output is in off-state.
t_{AA}	Delay between beginning of valid Address (with Chip Enable Low) and when Data Output becomes valid.
t_{WSC}	Required delay between beginning of valid Chip Enable and beginning of Write Enable pulse.
t_{WHD}	Required delay between end of Write Enable pulse and end of valid input data.
t_{WP}	Width of Write Enable pulse.
t_{WSA}	Required delay between beginning of valid Address and beginning of Write Enable pulse.
t_{WSD}	Required delay between beginning of valid Data Input and end of Write Enable pulse.
t_{WD}	Delay between beginning of Write Enable pulse and when Data Output reflects complement of Data Input.
t_{WHC}	Required delay between end of Write Enable pulse and end of Chip Enable.
t_{WHA}	Required delay between end of Write Enable pulse and end of valid Address.

74LS301
256-Bit TTL Bipolar RAM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 74LS301 is a Read/Write memory array which features an Open-Collector output for optimization of word expansion in bused organizations. Memory expansion is further enhanced by full on-chip address decoding, 3 Chip Enable inputs and PNP input transistors, which reduce input loading.

The additional feature of output blanking during Write ($\overline{D_O}$ terminal High) permits $\overline{D_O}$ and D_{IN} terminals to share a common I/O line to reduce system interconnections. These devices have fast Read access and Write cycle times, and thus are ideally suited in high-speed memory applications such as cache, buffers, scratch pads, writable control stores, etc.

Ordering information can be found on the following page.

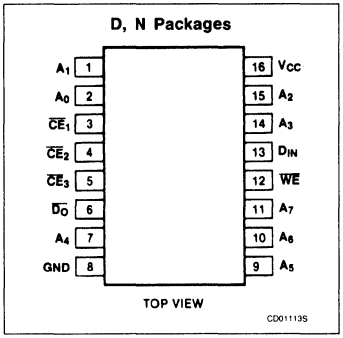
FEATURES

- **Address access time: 40ns max**
- **Write cycle time: 45ns max**
- **Power dissipation: 0.98mW/bit typ**
- **Input loading: −100μA max**
- **Output blanking during Write**
- **On-chip address decoding**
- **Schottky clamped**
- **TTL compatible**
- **Three Chip Enable inputs**
- **Open-Collector output**

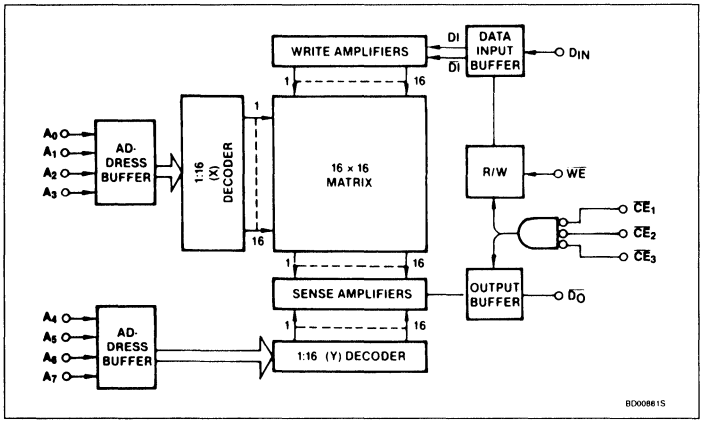
APPLICATIONS

- **Buffer memory**
- **Writable control store**
- **Memory mapping**
- **Push down stack**
- **Scratch pad**

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-pin Plastic DIP 300mil-wide	N74LS301 N
16-pin Plastic Small Outline 300mil-wide	N74LS301 D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_{OUT}	Output voltage High (open-collector)	+5.5	V_{DC}
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temperature range	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Input voltage[2]						
V_{IL}	Low	V_{CC} = 4.75V			0.8	V
V_{IH}	High	V_{CC} = 5.25V	2.0			V
V_{IC}	Clamp[3]	V_{CC} = 4.75V, I_{IN} = −12mA			−1.2	V
Output voltage						
V_{OL}	Low[5]	V_{CC} = 4.75V, I_{OL} = 16mA			0.45	V
Input current[2]						
I_{IL}	Low	V_{CC} = 5.25V, V_{IL} = 0.45V			−100	μA
I_{IH}	High	V_{IH} = 2.7V			25	μA
Output current						
I_{OLK}	Leakage[5]	V_{IH} = 2V, V_O = 5.5V			40	μA
Supply current[8]						
I_{CC}		V_{CC} = 5.25V		50	70	mA
Capacitance						
C_{IN}	Input	V_{CC} = 5.0V, V_{IN} = 2.0V		5		pF
C_{OUT}	Output	V_{OUT} = 2.0V		8		pF

TRUTH TABLE

MODE	$\overline{CE}$*	$\overline{WE}$	D_{IN}	D_{OUT}
Read	0	1	X	Stored $\overline{Data}$
Write "0"	0	0	0	1
Write "1"	0	0	1	1
Disabled	1	X	X	1

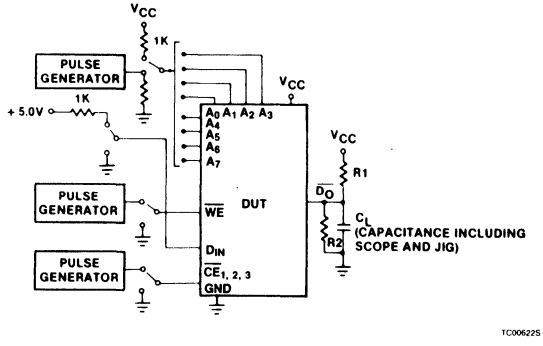
*"0" = All $\overline{CE}$ inputs Low: "1" = One or more $\overline{CE}$ inputs High.
X = Don't care.

AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[1]	Max	
Access time							
t_{AA}	Address	Output	Address		30	40	ns
t_{CE}	Chip Enable	Output	Chip Enable		15	25	
Disable time[10]							
t_{CD}		Output	Chip Enable		15	25	ns
t_{WD}	Valid time	Output	Write Enable		30	40	
Setup and hold time							
t_{WSA}[11]	Setup time	Write Enable	Address	0	−5		ns
t_{WHA}	Hold time			0	−5		
t_{WSD}	Setup time	Write Enable	Data in	25	15		ns
t_{WHD}	Hold time			0	−5		
t_{WSC}	Setup time	Write Enable	$\overline{CE}$	0	−5		ns
t_{WHC}	Hold time			0	−5		
Pulse width[9]							
t_{WP}[12]	Write Enable			25	15		ns

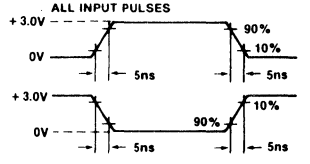
NOTES:
1. All typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
2. All voltage values are with respect to network ground terminal.
3. Test each input one at a time.
4. Measured with a logic low stored and V_{IL} applied to $\overline{CE}_1$, $\overline{CE}_2$ and $\overline{CE}_3$.
5. Measured with a logic high stored. Output sink current is supplied through a resistor to V_{CC}.
6. Measured with V_{IH} applied to $\overline{CE}_1$, $\overline{CE}_2$ and $\overline{CE}_3$.
7. Duration of the short-circuit should not exceed 1 second.
8. I_{CC} is measured with the Write enable and memory enable inputs grounded, all other inputs at 0.45V, and the output open.
9. Minimum required to guarantee a Write into the slowest bit.
10. Measured at a delta of 0.5V from logic levels with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
11. Measured with minimum t_{WP}.
12. Measured with minimum t_{WSA}.

TEST LOAD CIRCUIT



Loading Condition

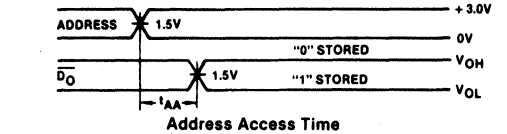
VOLTAGE WAVEFORMS



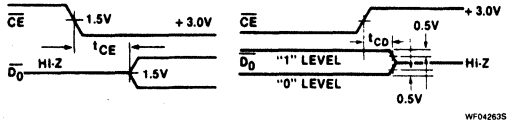
MEASUREMENTS:
All circuit delays are measured at the+ 1.5 level of inputs and output.

Input Pulses

TIMING DIAGRAM

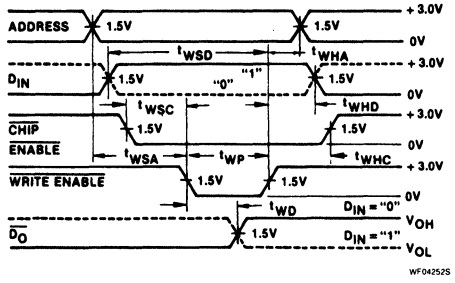


Address Access Time



Chip Enable Chip Disable

Read Cycle



NOTES:
All inputs $t_r = t_f = 5ns$ (10% to 90%)
All AC parameters are measured at 1.5V unless otherwise specified.

Write Cycle

MEMORY TIMING DEFINITIONS

SYMBOL	PARAMETER
t_{CE}	Delay between beginning of Chip Enable Low (with Address valid) and when Data Output becomes valid.
t_{CD}	Delay between when Chip Enable becomes High and Data Output is in off-state.
t_{AA}	Delay between beginning of valid Address (with Chip Enable Low) and when Data Output becomes valid.
t_{WSC}	Required delay between beginning of valid Chip Enable and beginning of Write Enable pulse.
t_{WHD}	Required delay between end of Write Enable pulse and end of valid input data.
t_{WP}	Width of Write Enable pulse.
t_{WSA}	Required delay between beginning of valid Address and beginning of Write Enable pulse.
t_{WSD}	Required delay between beginning of valid Data Input and end of Write Enable pulse.
t_{WD}	Delay between beginning of Write Enable pulse and when Data Output reflects complement of Data Input.
t_{WHC}	Required delay between end of Write Enable pulse and end of Chip Enable.
t_{WHA}	Required delay between end of Write Enable pulse and end of valid Address.

Byte-Organized TTL RAM

		page
82S09	**576-bit TTL Bipolar RAM (64 x 9) 45 ns**	**323**
82S09A	**576-bit TTL Bipolar RAM (64 x 9) 35 ns**	**323**
82S19	**576-bit TTL Bipolar RAM (64 x 9) 35 ns**	**327**
82S212	**2304-bit TTL Bipolar RAM (256 x 9) 45 ns**	**331**
82S212A	**2304-bit TTL Bipolar RAM (256 x 9) 35 ns**	**331**
8X350	**2048-bit TTL Bipolar RAM (256 x 8)**	**335**

82S09
82S09A
576-Bit TTL Bipolar RAM

Product Specification

Bipolar Memory Products

DESCRIPTION

The organization of this device allows byte storage of data, including parity. Where parity is not monitored, the ninth bit can be used as a tag or status indicator for each word stored. Ideal for scratch pad, push down stacks, buffer memories, and other internal memory applications in which cost and performance requirements dictate a wide data path in favor of word depth.

The 82S09/09A features Open-Collector outputs, Chip Enable input, and a very low current PNP input structure to enhance memory expansion.

Ordering information can be found on the following page.

The 82S09 and 82S09A devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

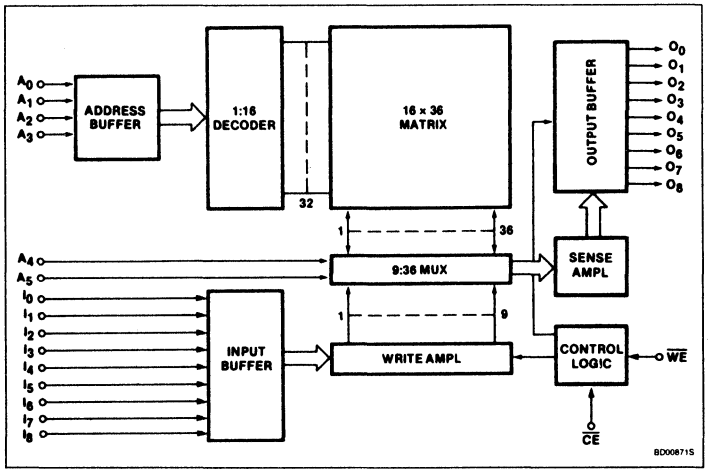
FEATURES

- **Address access time:**
  - **N82S09: 45ns max**
  - **N82S09A: 35ns max**
- **Write cycle time:**
  - **N82S09/09A: 45ns max**
- **Power dissipation: 1.3mW/bit typ**
- **Input loading: −100μA max**
- **On-chip address decoding**
- **Schottky clamped**
- **Fully TTL compatible**
- **Output is non-blanked during Write**
- **One Chip Enable input**
- **Outputs: Open-Collector**

APPLICATIONS

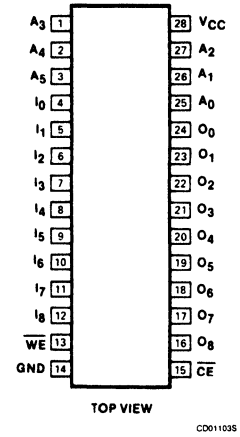
- **Buffer memory**
- **Control register**
- **FIFO memory**
- **Push down stack**
- **Scratch pad**

BLOCK DIAGRAM

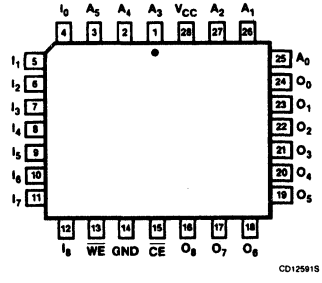


PIN CONFIGURATIONS

N Package



A Package



ORDERING INFORMATION

DESCRIPTION	ORDER CODE
28-pin Plastic DIP 600mil-wide	N82S09 N · N82S09A N
28-pin Plastic Leaded Chip Carrier 450mil-square	N82S09 A · N82S09A A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_{OH}	Output voltage High	+5.5	V_{DC}
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temperature range	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leqslant T_A \leqslant +75°C,\ 4.75V \leqslant V_{CC} \leqslant 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Input voltage[1]						
V_{IL}	Low	V_{CC} = 4.75V			0.8	V
V_{IH}	High	V_{CC} = 5.25V	2.0			V
V_{IC}	Clamp[2]	V_{CC} = 4.75V Min, I_{IN} = −12mA			−1.5	V
Output voltage[1]						
V_{OL}	Low[3]	V_{CC} = 4.75V, I_{OL} = 8.0mA			0.5	V
Input current						
I_{IL}	Low	V_{IN} = 0.45V			−100	μA
I_{IH}	High	V_{IN} = 5.5V			25	μA
Output current						
I_{OLK}	Leakage[4]	V_{CC} = 5.25V, V_{OUT} = 5.5V			40	μA
Supply current[5]						
I_{CC}		V_{CC} = 5.25V			190	mA
Capacitance						
		V_{CC} = 5.0V				
C_{IN}	Input	V_{IN} = 2.0V		5		pF
C_{OUT}	Output	V_{OUT} = 2.0V		8		pF

Notes on following page.

TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	I_N	O_N
Read	0	1	X	Stored $\overline{Data}$
Write "0"	0	0	0	1
Write "1"	0	0	1	0
Disabled	1	X	X	1

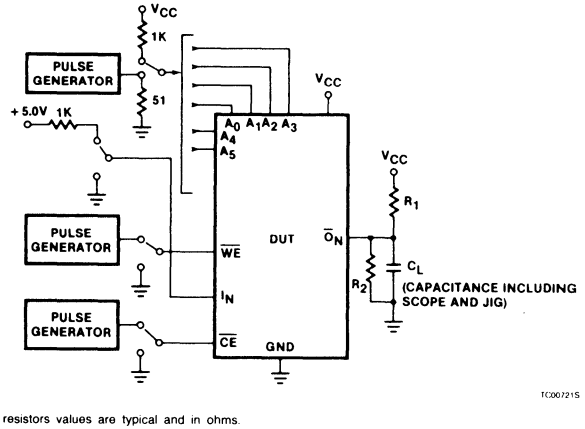
X = Don't care

AC ELECTRICAL CHARACTERISTICS $R_1 = 600\Omega$, $R_2 = 900\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TO	FROM	N82S09			N82S09A			UNIT
				Min	Typ	Max	Min	Typ	Max	
Access time										
t_{AA}	Address					45			35	ns
t_{CE}	Chip Enable					30			25	
Disable time[8]										
t_{CD}		Output	Chip Enable			30			25	ns
t_{WA}	Valid time	Output	Write Enable			30			25	
Setup and hold time										
t_{WSA}[9]	Setup time	Write	Address	5			5			ns
t_{WHA}	Hold time	Enable		5			5			
t_{WSD}	Setup time	Write	Data in	35			30			ns
t_{WHD}	Hold time	Enable		5			5			
t_{WSC}	Setup time	Write	$\overline{CE}$	5			5			ns
t_{WHC}	Hold time	Enable		5			5			
Pulse width[6]										
t_{WP}[10]	Write Enable			35			35			ns

NOTES:
1. All voltage values are with respect to network ground.
2. Test each input one at a time.
3. Measured with the logic low stored. Output sink current is applied through a resistor to V_{CC}.
4. Measured with V_{IH} applied to $\overline{CE}$.
5. I_{CC} is measured with the Write enable and chip enable input grounded, all other inputs at 0.45V, and the outputs open.
6. Minimum required to guarantee a Write into the slowest bit.
7. The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2-minute warm-up.
8. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
9. Measured with minimum t_{WP}.
10. Measured with minimum t_{WSA}.

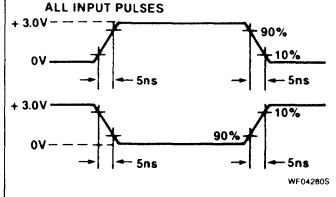
TEST LOAD CIRCUIT



All resistors values are typical and in ohms.

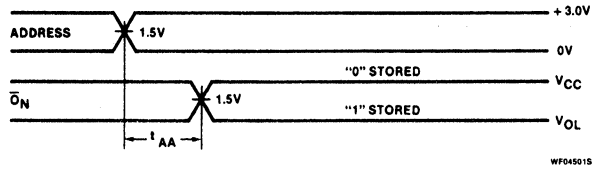
Loading Condition

VOLTAGE WAVEFORMS

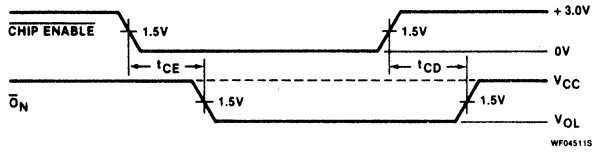


Input Pulses

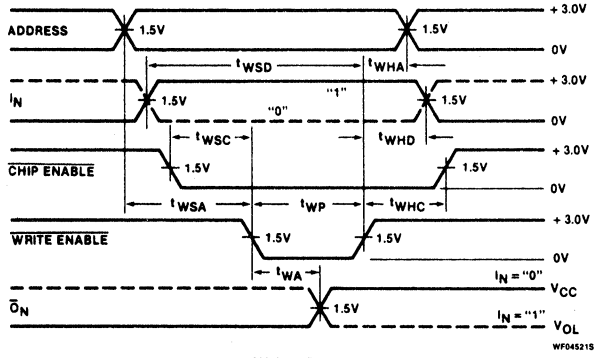
TIMING DIAGRAM



Read Cycle



Address Access Time
Chip Enable/Disable Times



Write Cycle

MEMORY TIMING DEFINITIONS

SYMBOL	PARAMETER
t_{CE}	Delay between beginning of Chip Enable Low (with Address valid) and when Data Output becomes valid.
t_{AA}	Delay between beginning of valid Address (with Chip Enable Low) and when Data Output becomes valid.
t_{WSC}	Required delay between beginning of valid Chip Enable and beginning of Write Enable pulse.
t_{WHD}	Required delay between end of Write Enable pulse and end of valid input data.
t_{WP}	Width of Write Enable pulse.
t_{WSA}	Required delay between beginning of valid Address and beginning of Write Enable pulse.
t_{WSD}	Required delay between beginning of valid Data Input and end of Write Enable pulse.
t_{WD}	Delay between beginning of Write Enable pulse and when Data Output goes High (blanks).
t_{WHC}	Required delay between end of Write Enable pulse and end of Chip Enable.
t_{WHA}	Required delay between end of Write Enable pulse and end of valid Address.
t_{WR}	Delay between end of Write Enable pulse and when Data Output becomes valid. (Assuming Address still valid.)
t_{WA}	Delay between beginning of Write Enable pulse and when Data Output reflects complement of Data Input.

82S19
576-Bit TTL Bipolar RAM

Product Specification

Bipolar Memory Products

DESCRIPTION

The organization of this device allows byte storage of data, including parity. Where parity is not monitored, the ninth bit can be used as a tag or status indicator for each word stored. Ideal for scratch pad, push down stacks, buffer memories, and other internal memory applications in which cost and performance requirements dictate a wide data path in favor of word depth.

The 82S19 features Open Collector outputs, Chip Enable input, and a very low current PNP input structure to enhance memory expansion.

During Write operation, the 82S19 output goes to a "1".

Ordering information can be found on the following page.

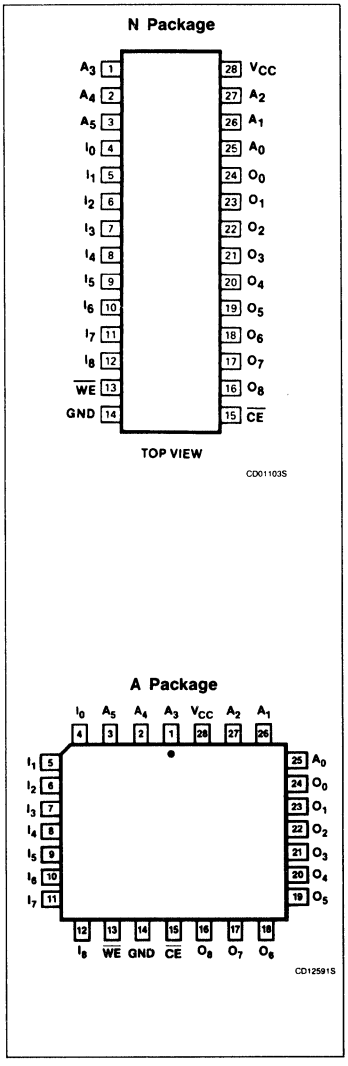
FEATURES

- **Address access time: 35ns max**
- **Write cycle time: 45ns max**
- **Power dissipation: 1.3mW/bit typ**
- **Input loading: −100μA max**
- **On-chip address decoding**
- **Schottky clamped**
- **Fully TTL compatible**
- **One Chip Enable input**
- **Output is blanked during Write**
- **Outputs: Open-Collector**

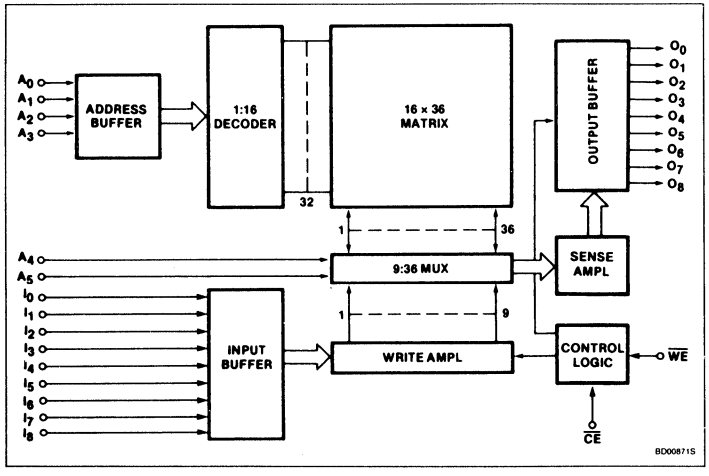
APPLICATIONS

- **Buffer memory**
- **Control register**
- **FIFO memory**
- **Push down stack**
- **Scratch pad**

PIN CONFIGURATIONS



BLOCK DIAGRAM



576-Bit TTL Bipolar RAM (64 × 9) 82S19

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
28-pin Plastic DIP 600mil-wide	N82S19 N
28-pin Plastic Leaded Chip Carrier 450mil-square	N82S19 A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_{OH}	Output voltage High	+5.5	V_{DC}
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temperature range	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leqslant T_A \leqslant +75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Input voltage						
V_{IL}	Low	V_{CC} = 4.75V			0.8	V
V_{IH}	High	V_{CC} = 5.25V	2.0			V
V_{IC}	Clamp[2]	V_{CC} = 4.75V, I_{IN} = −12mA			−1.5	V
Output voltage						
V_{OL}	Low[3]	V_{CC} = 4.75V, I_{OL} = 8.0mA			0.5	V
Input current						
I_{IL}	Low	V_{IN} = 0.45V			−100	μA
I_{IH}	High	V_{IN} = 5.5V			26	μA
Output current						
I_{OLK}	Leakage[4]	V_{CC} = 5.25V, V_{OUT} = 5.5V			40	μA
Supply current[3,5]						
I_{CC}		V_{CC} = 5.25V			190	mA
Capacitance						
		V_{CC} = 5.0V				
C_{IN}	Input	V_{IN} = 2.0V		5		pF
C_{OUT}	Output	V_{OUT} = 2.0V		8		pF

Notes on following page.

TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	I_N	$\overline{O}_N$
Read	0	1	X	Stored $\overline{Data}$
Write "0"	0	0	0	1
Write "1"	0	0	1	1
Disabled	1	X	X	1

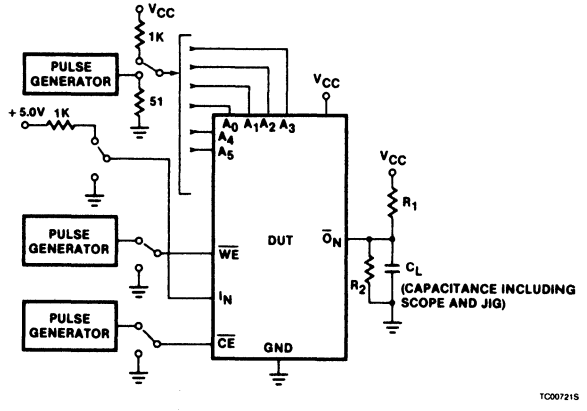
X = Don't care

AC ELECTRICAL CHARACTERISTICS $R_1 = 600\Omega$, $R_2 = 900\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ	Max	
Access time							
t_{AA}	Address					35	ns
t_{CE}	Chip Enable					25	
t_{CD}	Disable time	Output	Chip Enable			25	ns
t_{WD}	Valid time	Output	Write Enable			25	
t_{WR}	Write recovery time	Output	Write Enable			25	
Setup and hold time							
t_{WSA}[8]	Setup time	Write Enable	Address	5			ns
t_{WHA}	Hold time			5			
t_{WSD}	Setup time	Write Enable	Data in	30			ns
t_{WHD}	Hold time			5			
t_{WSC}	Setup time	Write Enable	$\overline{CE}$	5			ns
t_{WHC}	Hold time			5			
Pulse width[6]							
t_{WP}[9]	Write enable			35			ns

NOTES:
1. All voltage values are with respect to network ground terminal.
2. Test each input one at a time.
3. Measured with a logic low stored and V_{IL} applied to $\overline{CE}_1$, $\overline{CE}_2$ and $\overline{CE}_3$.
4. Measured with V_{IH} applied to $\overline{CE}$.
5. I_{CC} is measured with the Write enable and chip enable inputs grounded, all other inputs at 0.45V, and the outputs open.
6. Minimum required to guarantee a Write into the slowest bit.
7. The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2-minute warm-up.
8. Measured with minimum t_{WP}.
9. Measured with minimum t_{WSA}.

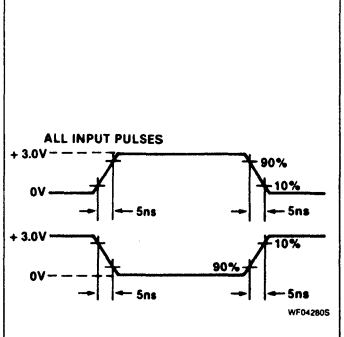
TEST LOAD CIRCUIT



All resistors values are typical and in ohms.

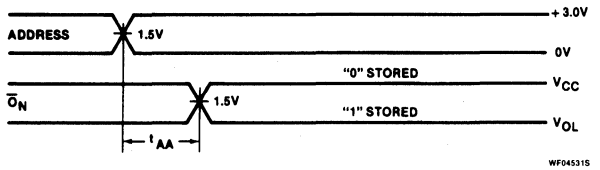
Loading Condition

VOLTAGE WAVEFORMS

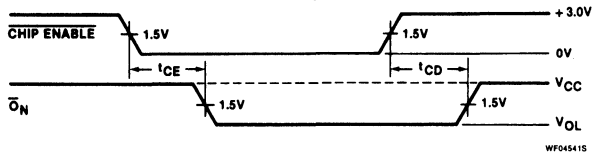


Input Pulses

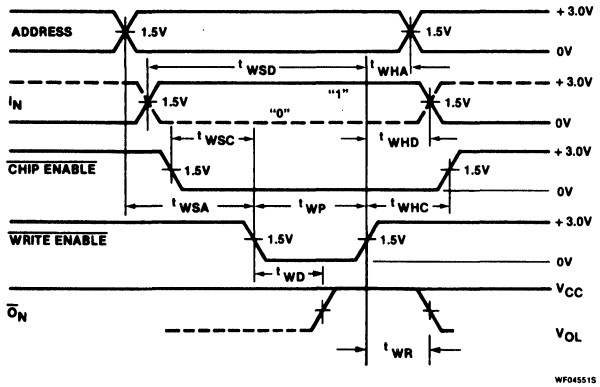
TIMING DIAGRAM



Read Cycle



Address Access Time
Chip Enable/Disable Times



Write Cycle
Chip Enable/Disable Times

MEMORY TIMING DEFINITIONS

SYMBOL	PARAMETER
t_{CE}	Delay between beginning of Chip Enable Low (with Address valid) and when Data Output becomes valid.
t_{CD}	Delay between when Chip Enable becomes High and Data Output is in off-state.
t_{AA}	Delay between beginning of valid Address (with Chip Enable Low) and when Data Output becomes valid.
t_{WSC}	Required delay between beginning of valid Chip Enable and beginning of Write Enable pulse.
t_{WHD}	Required delay between end of Write Enable pulse and end of valid input data.
t_{WP}	Width of Write Enable pulse.
t_{WSA}	Required delay between beginning of valid Address and beginning of Write Enable pulse.
t_{WSD}	Required delay between beginning of valid Data Input and end of Write Enable pulse.
t_{WD}	Delay between beginning of Write Enable pulse and when Data Output goes High (blanks).
t_{WHC}	Required delay between end of Write Enable pulse and end of Chip Enable.
t_{WHA}	Required delay between end of Write Enable pulse and end of valid Address.
t_{WR}	Delay between end of Write Enable pulse and when Data Output becomes valid. (Assuming Address still valid.)

82S212
82S212A
2304-Bit TTL Bipolar RAM

Product Specification

Bipolar Memory Products

DESCRIPTION

The organization of the 82S212 and 82S212A allows byte wide storage of data, including parity. Where parity is not required, the ninth bit can be used as a tag for each word stored. The 82S212 and 82S212A are ideal for scratch pad, push down stacks, buffer memories, and other internal memory applications in which space and performance requirements dictate a wide data path in favor of word depth.

Data inputs and outputs are common (common I/O) with separate output disable (OD) line that allows ease of Read/Write operations using a common bus.

Ordering information can be found on the following page.

The 82S212 and 82S212A devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

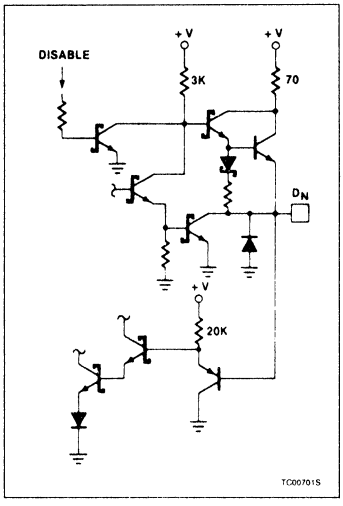
FEATURES

- **Address access time:**
  - **N82S212: 45ns max**
  - **N82S212A: 35ns max**
- **Power dissipation: 0.3mW/bit typ**
- **Schottky clamped TTL**
- **One Chip Enable input**
- **Common I/O**
  - **Inputs: PNP Buffered**
  - **Outputs: 3-State**

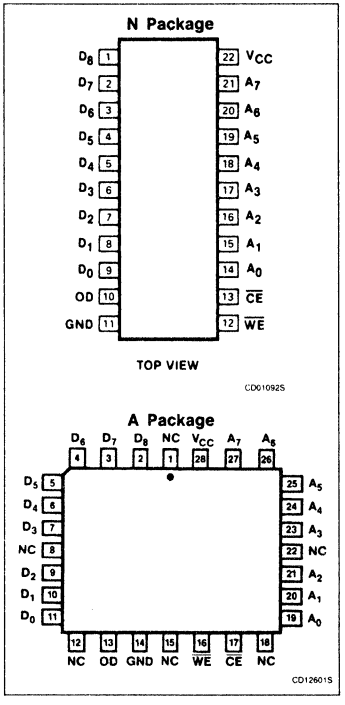
APPLICATIONS

- **Cache memory**
- **Buffer storage**
- **Writable control store**

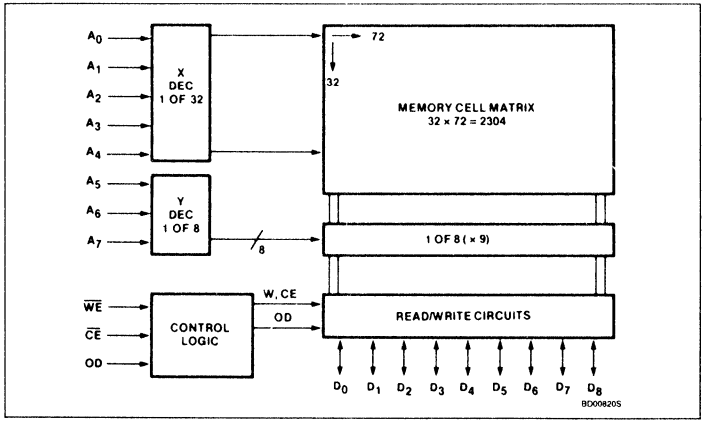
TYPICAL I/O STRUCTURE



PIN CONFIGURATIONS



BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	ORDER CODE
22-pin Plastic DIP 400mil-wide	N82S212 N · N82S212A N
28-pin Plastic Leaded Chip Carrier 450mil-square	N82S212 A · N82S212A A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_{OUT}	Output voltage High (open-collector)	+5.5	V_{DC}
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temperature range	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leqslant T_A \leqslant +75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[3]	Max	
Input voltage[2]						
V_{IL}	Low	V_{CC} = 4.75V			0.80	V
V_{IH}	High	V_{CC} = 5.25V	2.0			V
V_{IC}	Clamp[4]	V_{CC} = 4.75V, I_{IN} = −12mA			−1.5	V
Output voltage[2]						
V_{OH}	High	I_{OH} = −2mA	2.4			V
V_{OL}	Low	V_{CC} = 4.75V, I_{OL} = 8.0mA			0.5	V
Input current						
I_{IL}	Low	V_{IN} = 0.45V			−100	μA
I_{IH}	High	V_{IN} = 5.5V			25	μA
Output current						
I_{OZ}	Hi-Z State	$\overline{CE}$ = High, or OD = High, V_{OUT} = 5.5V			40	μA
		$\overline{CE}$ = High or OD = High, V_{OUT} = 0.5V			−100	
I_{OS}	Short circuit[4,5]	$\overline{CE}$ = OD = Low, V_{OUT} = 0V	−15		−70	mA
Supply current[7]						
I_{CC}		V_{CC} = 5.25V		135	185	mA
Capacitance						
		V_{CC} = 5.0V				
C_{IN}	Input	V_{IN} = 2.0V		5		pF
C_{OUT}	Output	V_{OUT} = 2.0V		8		pF

TRUTH TABLE

MODE	$\overline{WE}$	$\overline{CE}$	OD	D_N IN/OUT
Disable output	X	X	1	Hi-Z
Disable R/W	X	1	X	Hi-Z
Write	0	0	1	Data in
Read	1	0	0	Data out

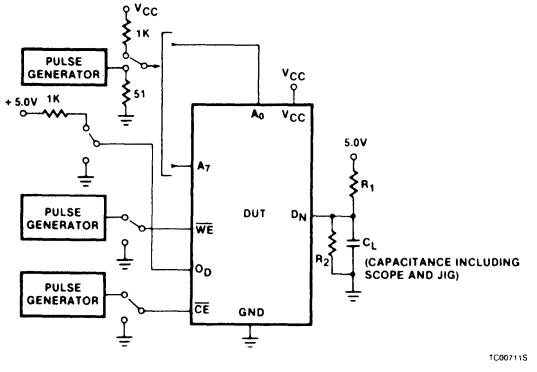
X = Don't care

AC ELECTRICAL CHARACTERISTICS $R_1 = 600\Omega$, $R_2 = 900\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER[1]	TO	FROM	N82S212			N82S212A			UNIT
				Min	Typ[3]	Max	Min	Typ[3]	Max	
Access time										
t_{AA}	Address	Output	Address			45			35	ns
Enable time										
t_{OE}	Output	Output	OD	5		25			25	ns
t_{CE}	Output	Output	Chip Enable			25			25	
Disable time[6]										
t_{OD}	Output	Output	OD			25			25	ns
t_{CD}	Output	Output	Chip Enable			25			25	
Pulse width										
t_{WP}[8]	Write			25			25			ns
Setup and hold time										
t_{SWC}	Setup time	Write	Chip Enable	5			5			ns
t_{WHD}	Hold time	Chip Enable	Write	5			5			
t_{WSD}	Setup time	Write	Data	25			25			ns
t_{WHD}	Hold time	Data	Write	5			5			
t_{WSA}[9]	Setup time	Write	Address	5			5			ns
t_{WHA}	Hold time	Address	Write	5			5			
t_{SO}	Setup time (from disabled state)	Chip Enable	OD	5			5			ns
t_{HO}	Hold time	OD	Chip Enable	5			5			

NOTES:
1. The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2-minute warmup.
2. All voltages are with respect to network ground terminal.
3. All typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
4. Measured on one pin at a time.
5. Duration of I_{OS} test should not exceed one second.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
7. I_{CC} is measured with the Write enable and memory enable inputs grounded, all other inputs at 0.45V, and the outputs open.
8. Measured with minimum t_{WSA}.
9. Measured with minimum t_{WP}.

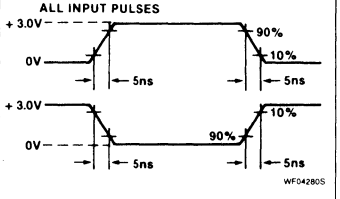
TEST LOAD CIRCUIT



All resistors values are typical and in ohms.

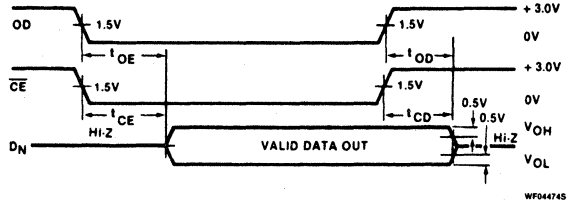
Loading Condition

VOLTAGE WAVEFORMS



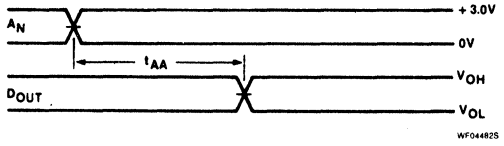
Input Pulses

TIMING DIAGRAM

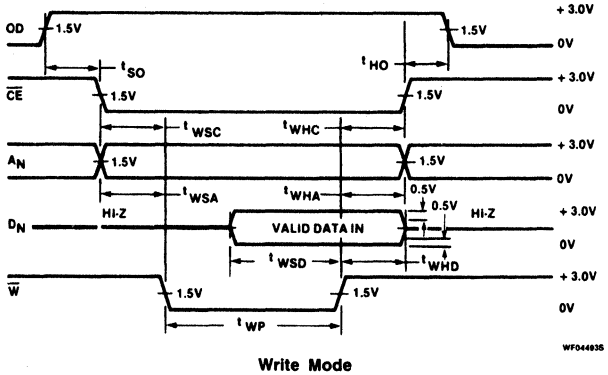


Enable/Disable

NOTE:
Assumes t_{AA} from address to valid data $\overline{W}$ = High



Read Mode



Write Mode

CAUTION:
Data Bus conflict can occur with $\overline{CE}$ = 0, apply data source after t_{OD}(max.) and remove data source before t_{OE}(min.).

8X350
2048-Bit TTL Bipolar RAM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 8X350 bipolar RAM is designed principally as a working storage element in an 8X305 based system. Internal circuitry is provided for direct use in 8X305 applications. When used with the 8X305, the RAM address and data buses are tied together and connected to the IV bus of the system.

The data inputs and outputs share a common I/O bus with 3-State outputs.

Ordering information can be found on the following page.

The 8X350 devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

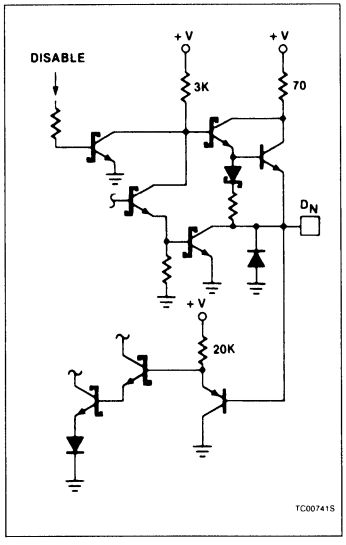
FEATURES

- **On-chip address latches**
- **Schottky clamped**
- **One Master Enable input**
- **Directly interfaces with the 8X305 bipolar microprocessor with no external logic**
- **May be used on left or right bank**
- **Common I/O:**
  - **Inputs: PNP buffered**
  - **Outputs: 3-State**

APPLICATIONS

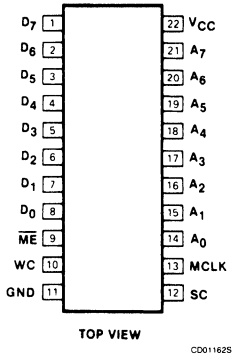
- **8X300 or 8X305 working storage**

TYPICAL I/O STRUCTURE

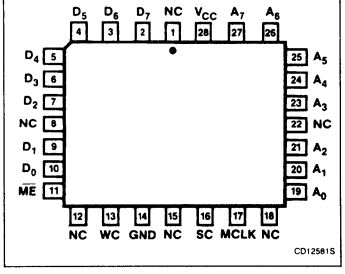


PIN CONFIGURATIONS

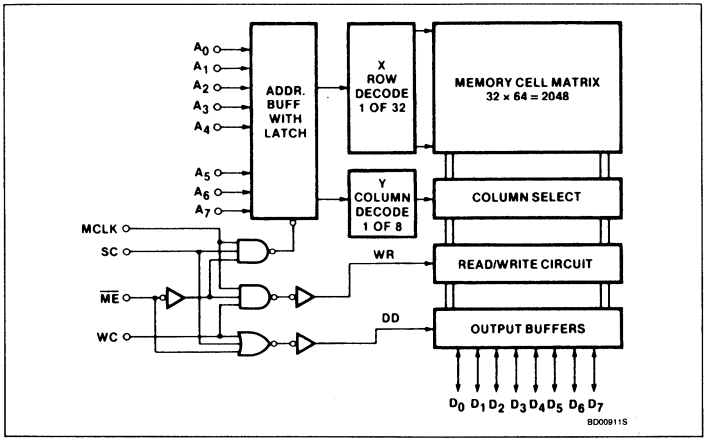
N Package



A Package



BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	ORDER CODE
22-pin Plastic DIP 400mil-wide	N8X350 N
28-pin Plastic Leaded Chip Carrier 450mil-square	N8X350 A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_{OH} V_O	Output voltage High Off-stage	 +5.5 +5.5	V_{DC}
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temperature range	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leqslant T_A \leqslant +75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Input voltage						
V_{IL}	Low	V_{CC} = 4.75V			0.8	V
V_{IH}	High	V_{CC} = 5.25V	2.0			V
V_{IC}	Clamp[3]	V_{CC} = 4.75V, I_{IN} = −12mA			−1.2	V
Output voltage						
V_{OL}	Low[4]	V_{CC} = 4.75V I_{OL} = 9.6mA			0.5	V
V_{OH}	High[5]	I_{OH} = −2mA	2.4			V
Input current						
I_{IL}	Low	V_{IN} = 0.45V			−100	μA
I_{IH}	High	V_{IN} = 5.5V			25	μA
Output current						
I_{OZ}	Hi-Z State	$\overline{ME}$ = High, V_{OUT} = 5.5V			40	μA
		$\overline{ME}$ = High, V_{OUT} = 0.5V			−100	
I_{OS}	Short circuit[3,6]	SC = WC, $\overline{ME}$ = Low, V_{OUT} = 0V, High stored	−15		−70	mA
Supply current[7]						
I_{CC}		V_{CC} = 5.25V			185	mA
Capacitance						
C_{IN}	Input	$\overline{ME}$ = High, V_{CC} = 5.0V V_{IN} = 2.0V		5		pF
C_{OUT}	Output	V_{OUT} = 2.0V		8		pF

TRUTH TABLE

MODE	$\overline{ME}$	SC	WC	MCLK	BUSSED DATA/ADDRESS LINES
Hold address Disable data out	1	X	X	X	Hi-Z data out
Input new address	0	1	0	1	Address Hi-Z
Hold address Disable data out	0	1	0	0	Hi-Z data out
Hold address Write data	0	0	1	1	Data in
Hold address Disable data out	0	0	1	0	Hi-Z data out
Hold address Read data	0	0	0	X	Data out
Undefined state[12]	0	1	1	1	–
Hold address[12] Disable data out	0	1	1	0	Hi-Z data out

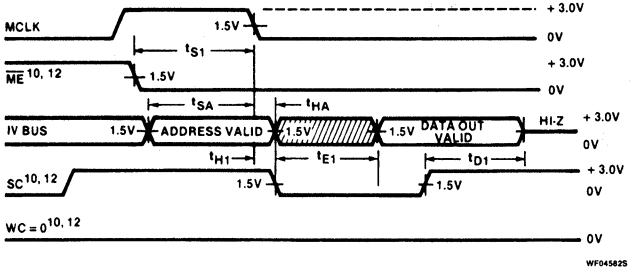
NOTE:
X = Don't care

AC ELECTRICAL CHARACTERISTICS $R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

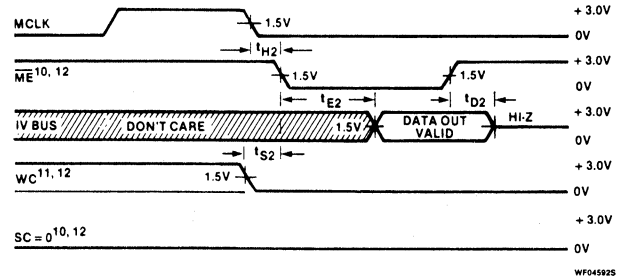
SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ	Max	
Enable time							
t_{E1} t_{E2}	Output Output	Data out Data out	$\overline{SC}$– $\overline{ME}$–			35 35	ns
Disable time[13]							
t_{D1} t_{D2}	Output Output	Data out Data out	SC+ $\overline{ME}$+			35 35	ns
Pulse width[8]							
t_W	Master clock			40			ns
Setup and hold time							
t_{SA} t_{HA}	Setup time Hold time	MCLK– Address	Address MCLK–	30 5			ns
t_{SD} t_{HD}	Setup time Hold time	MCLK– Data in	Data in MCLK–	35 5			ns
t_{S3} t_{H3}	Setup time Hold time	MCLK– $\overline{ME}$+	$\overline{ME}$– MCLK–	40 5			ns
t_{S1} t_{H2}	Setup time Hold time	MCLK– $\overline{ME}$–	$\overline{ME}$– MCLK–	30 5			ns
t_{S2} t_{H1} t_{H4}	Setup time Hold time Hold time	$\overline{ME}$– SC– WC–	SC–, WC– MCLK– MCLK–	0 5 5			ns

NOTES:
1. All voltage values are with respect to network ground terminal.
2. The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2-minute warm-up.
3. Test each pin one at a time.
4. Measured with a logic Low stored. Output sink current is supplied through a resistor to V_{CC}.
5. Measured with a logic High stored.
6. Duration of the short circuit should not exceed 1 second.
7. I_{CC} is measured with the Write enable and memory enable inputs grounded, all other inputs at 0.45V, and the output open.
8. Minimum required to guarantee a Write into the slowest bit.
9. Applied to the 8X300 based system with the data and address pins tied to the IV Bus.
10. SC + ME = 1 to avoid bus conflict.
11. WC + ME = 1 to avoid bus conflict.
12. The SC and WC outputs from the 8X300 are never at 1 simultaneously.
13. Measured at at delta of 0.5V from the logic level with $R_1 = 750\Omega$, $R_2 = 500\Omega$, and $C_L = 5pF$.

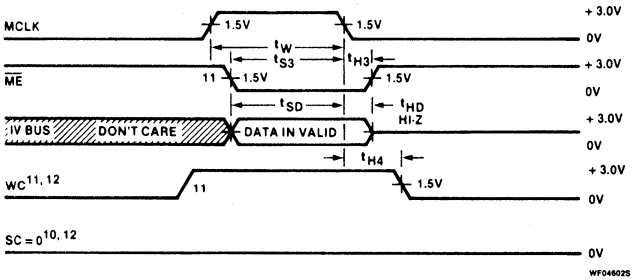
TIMING DIAGRAM



Transparent Address Read Cycle



Latched Address Read Cycle



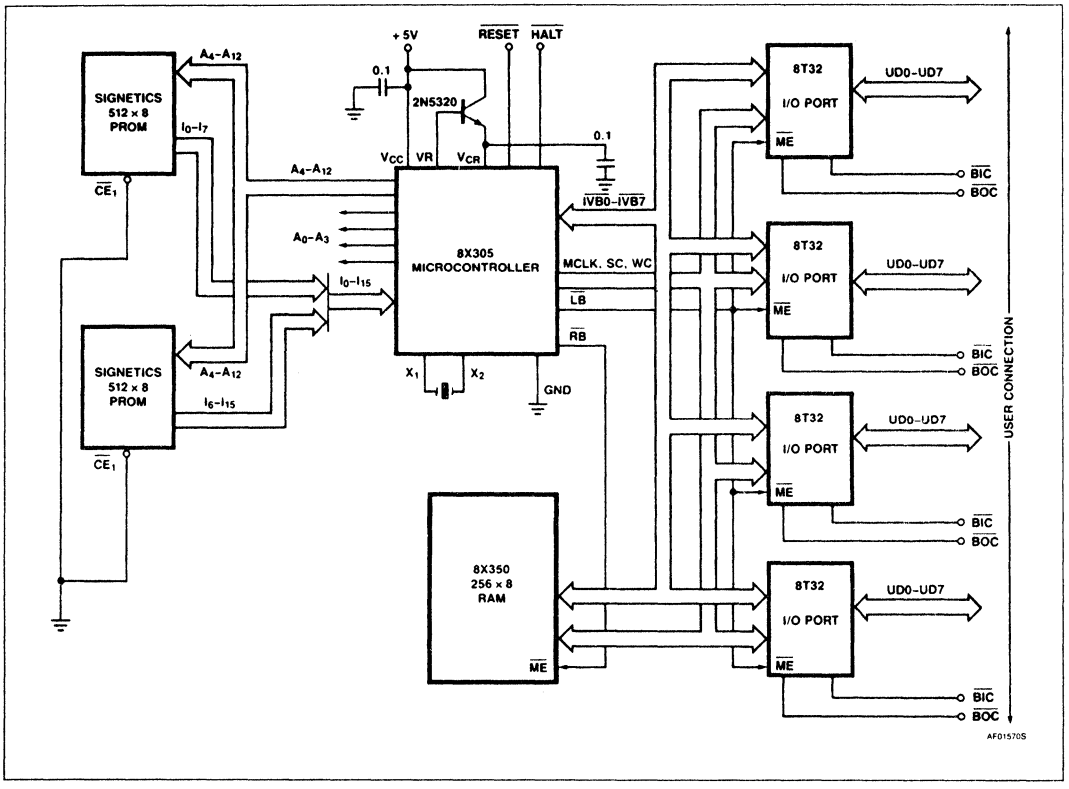
Latched Address Write Cycle

MEMORY TIMING DEFINITIONS

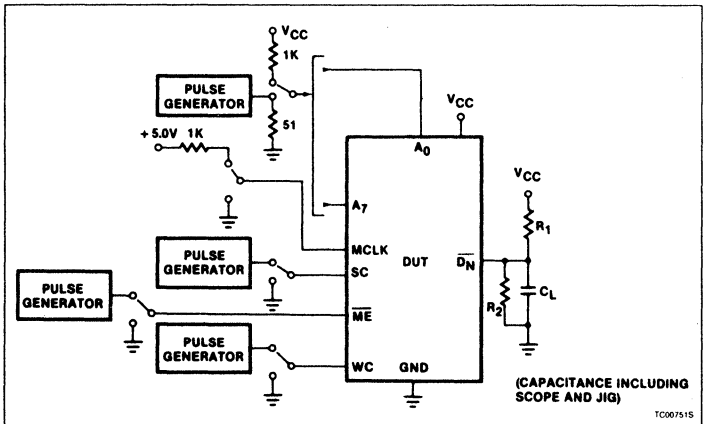
SYMBOL	PARAMETER
t_{S1}	Required delay between beginning of Master Enable Low and falling edge of Master Clock.
t_{SA}	Required delay between beginning of valid Address and falling edge of Master Clock.
t_{HA}	Required delay between falling edge of Master Clock and end of valid Address.
t_{H1}	Required delay between falling edge of Master Clock and when Select Command becomes Low.
t_{E1}	Delay between beginning of Select Command Low and beginning of valid Data Output on the IV Bus.
t_{D1}	Delay between when Select Command becomes High and end of valid Data Output on the IV Bus.
t_{H2}	Required delay between falling edge of Master Clock and when Master Enable becomes Low.
t_{E2}	Delay between when Master Enable becomes Low and beginning of valid Data Output on the IV Bus.
t_{D2}	Delay between when Master Enable becomes High and end of valid Data Output on the IV Bus.
t_{S2}	Required delay between when Select Command or Write Command becomes Low and when Master Enable becomes Low.
t_W	Minimum width of the Master Clock pulse.
t_{S3}	Required delay between when Master Enable becomes Low and falling edge of Master Clock.
t_{H3}	Required delay between falling edge of Master Clock and when Master Enable becomes High.
t_{SD}	Required delay between beginning of valid Data Input on the IV Bus and falling edge of Master Clock.
t_{HD}	Required delay between falling edge of Master Clock and end of valid Data Input on the IV Bus.
t_{H4}	Required delay between falling edge of Master Clock and when Write Command becomes Low.

2048-Bit TTL Bipolar RAM (256 × 8) 8X350

TYPICAL 8X350 APPLICATION



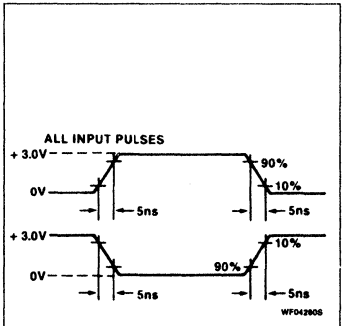
TEST LOAD CIRCUIT



All resistors values are typical and in ohms.

Loading Condition

VOLTAGE WAVEFORMS



Measurements: All circuit delays are measured at the+ 1.5V level of inputs and output.

Input Pulses

Low Complexity TTL PROM

		page
82S23/82S123	256-bit TTL Bipolar PROM (32 x 8) 50 ns	343
82S23A/82S123A	256-bit TTL Bipolar PROM (32 x 8) 25 ns	347
82US23	256-bit TTL Bipolar PROM (32 x 8) 13 ns	351
82US123	256-bit TTL Bipolar PROM (32 x 8) 10 ns	351
82S126/82S129	1024-bit TTL Bipolar PROM (256 x 4) 50 ns	355
82S126A	1024-bit TTL Bipolar PROM (256 x 4) 30 ns	359
82S129A	1024-bit TTL Bipolar PROM (256 x 4) 27 ns	359
82S130/82S131	2048-bit Bipolar PROM (512 x 4) 50 ns	363
82S130A	2048-bit Bipolar PROM (512 x 4) 33 ns	367
82S131A	2048-bit Bipolar PROM (512 x 4) 30 ns	367
82S135	2048-bit Bipolar PROM (256 x 8) 45 ns	371
82LS135	2048-bit Bipolar PROM (256 x 8) 100 ns	375

82S23
82S123
256-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82S23 and 82S123 are field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The 82S23 and 82S123 devices are supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing a Ni-Cr link matrix.

These devices include on-chip decoding and 1 Chip Enable input for memory expansion. They feature either Open-Collector or 3-State outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

The 82S23 and 82S123 devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

FEATURES

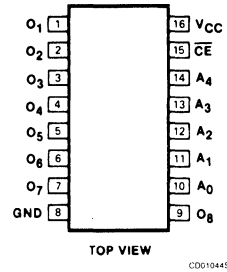
- **Address access time: 50ns max**
- **Power dissipation: 1.3mW/bit typ**
- **Input loading: −100μA max**
- **On-chip address decoding**
- **One Chip Enable input**
- **Output options:**
  - **N82S23: Open-Collector**
  - **N82S123: 3-State**
- **No separate fusing pins**
- **Unprogrammed outputs are Low level**
- **Fully TTL compatible**

APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Format conversion**
- **Hardwired algorithms**
- **Random logic**
- **Code conversion**

PIN CONFIGURATIONS

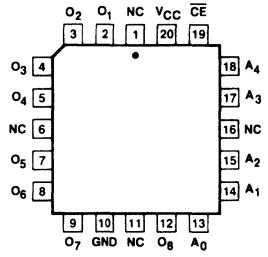
N Package



TOP VIEW

CD01044S

A Package



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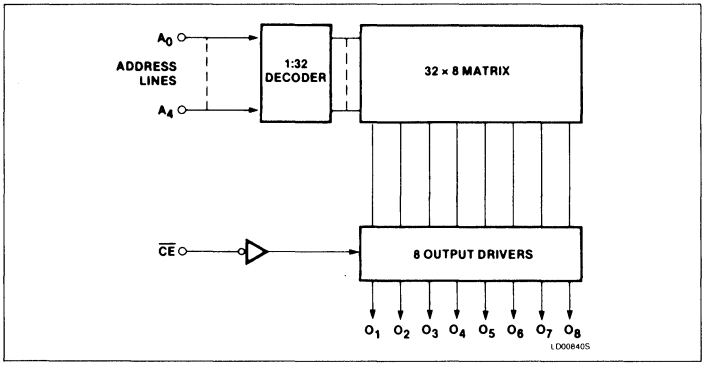
BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-pin Plastic DIP 300mil-wide	N82S23 N • N82S123 N
20-pin Plastic Leaded Chip Carrier 350mil-square	N82S23 A • N82S123 A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_{OH} V_O	Output voltage High (82S23) Off-State (82S123)	+5.5	V_{DC}
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temperature range	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leqslant T_A \leqslant +75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage						
V_{IL}	Low	V_{CC} = 4.75V			0.8	V
V_{IH}	High	V_{CC} = 5.25V	2.0			V
V_{IC}	Clamp	I_{IN} = −12mA			−1.2	V
Output voltage						
		$\overline{CE}$ = Low				
V_{OL}	Low	I_{OUT} = 16mA			0.45	V
V_{OH}	High	I_{OUT} = −2mA	2.4			V
Input current						
I_{IL}	Low	V_{IN} = 0.45V			−100	μA
I_{IH}	High	V_{IN} = 5.5V			50	μA
Output current						
I_{OLK}	Leakage (82S23)	$\overline{CE}$ = High, V_{OUT} = 5.5V			40	μA
I_{OZ}	Hi-Z State (82S123)	$\overline{CE}$ = High, V_{OUT} = 5.5V			40	
		$\overline{CE}$ = High, V_{OUT} = 0.5V			−40	
I_{OS}	Short circuit (82S123)[3]	$\overline{CE}$ = Low, V_{OUT} = 0V, High stored	−15		−90	mA
Supply current[7]						
I_{CC}		V_{CC} = 5.25V			96	mA
Capacitance						
		$\overline{CE}$ = High, V_{CC} = 5.0V				
C_{IN}	Input	V_{IN} = 2.0V		5		pF
C_{OUT}	Output	V_{OUT} = 2.0V		8		pF

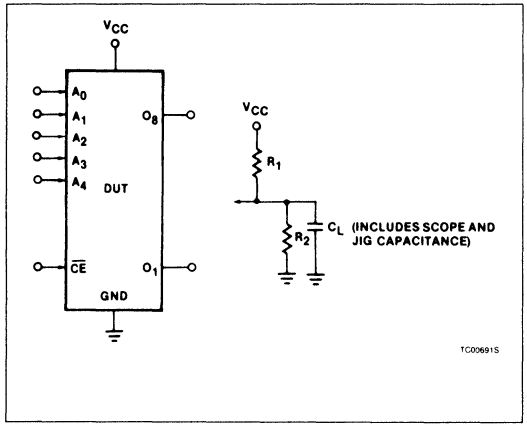
Notes on following page.

AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

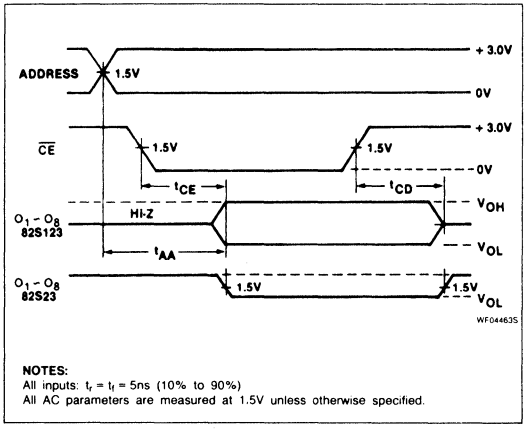
SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[5]	Max	
Access time[4]							
t_{AA}		Output	Address		45	50	ns
t_{CE}		Output	Chip Enable			35	ns
Disable time[6]							
t_{CD}		Output	Chip Enable			35	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground terminal.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μs.
5. Typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
7. Measured with all inputs grounded and all outputs open.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORMS



NOTES:
All inputs: $t_r = t_f = 5ns$ (10% to 90%)
All AC parameters are measured at 1.5V unless otherwise specified.

82S23A
82S123A
256-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82S23A and 82S123A are field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The 82S23A and 82S123A devices are supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

These devices include on-chip decoding and 1 Chip Enable input for memory expansion. They feature either Open-Collector or 3-State outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

The 82S23A and 82S123A devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

FEATURES

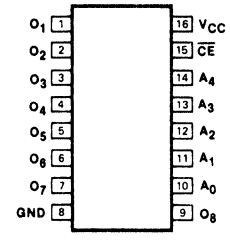
- **Address access time: 25ns max**
- **Power dissipation: 1.3mW/bit typ**
- **Input loading: −100μA max**
- **On-chip address decoding**
- **One Chip Enable input**
- **Output options:**
  - **N82S23A: Open-Collector**
  - **N82S123A: 3-State**
- **No separate fusing pins**
- **Unprogrammed outputs are Low level**
- **Fully TTL compatible**

APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Format conversion**
- **Hardwired algorithms**
- **Random logic**
- **Code conversion**

PIN CONFIGURATIONS

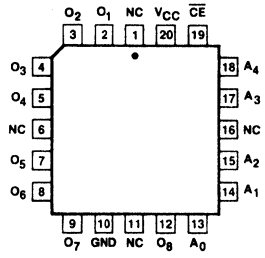
D, N Package



TOP VIEW

CD01044S

A Package



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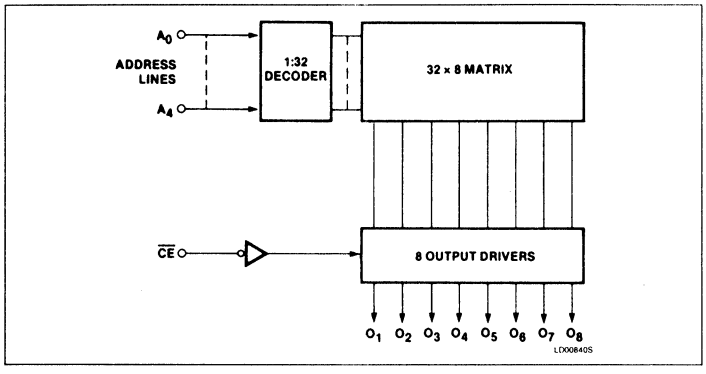
LOGIC DIAGRAM



ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-pin Plastic DIP 300mil-wide	N82S23A N • N82S123A N
16-pin Plastic SO 300mil-wide	N82S23A D • N82S123A D
20-pin Plastic Leaded Chip Carrier 350mil-square	N82S23A A • N82S123A A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_{OH} V_O	Output voltage High (82S23A) Off-State (82S123A)	+5.5 +5.5	V_{DC}
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temperature range	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage						
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			V
V_{IC}	Clamp	I_{IN} = −12mA			−1.2	V
Output voltage						
		$\overline{CE}$ = Low				
V_{OL}	Low	I_{OUT} = 16mA			0.45	V
V_{OH}	High	I_{OUT} = −2mA	2.4			V
Input current						
I_{IL}	Low	V_{IN} = 0.45V			−100	μA
I_{IH}	High	V_{IN} = 5.5V			50	
Output current						
I_{OLK}	Leakage (82S23A)	$\overline{CE}$ = High, V_{OUT} = 5.5V			40	μA
I_{OZ}	Hi-Z State (82S123A)	$\overline{CE}$ = High, V_{OUT} = 5.5V			40	
		$\overline{CE}$ = High, V_{OUT} = 0.5V			−40	
I_{OS}	Short circuit (82S123A)[3]	$\overline{CE}$ = Low, V_{OUT} = 0V, High stored	−15		−90	mA
Supply current[7]						
I_{CC}		V_{CC} = 5.25V			96	mA
Capacitance						
		$\overline{CE}$ = High, V_{CC} = 5.0V				
C_{IN}	Input	V_{IN} = 2.0V		5		pF
C_{OUT}	Output	V_{OUT} = 2.0V		8		pF

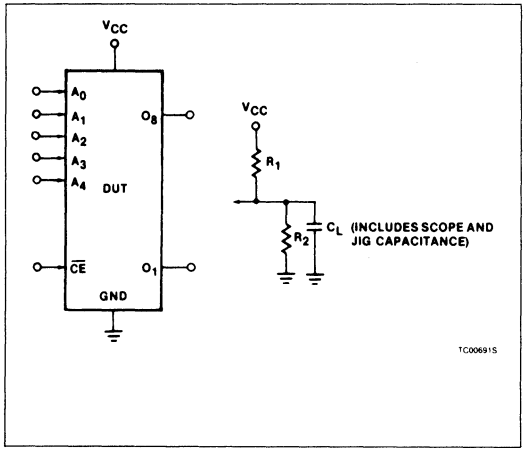
Notes on following page.

AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

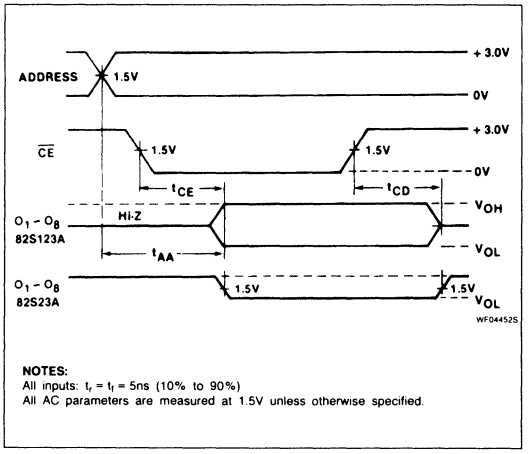
SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[5]	Max	
Access time							
t_{AA}[4]		Output	Address		20	25	ns
t_{CE}		Output	Chip Enable			18	ns
Disable time[6]							
t_{CD}		Output	Chip Disable			18	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μs.
5. Typical values are at $V_C = 5V$, $T_A = +25°C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
7. Measured with all inputs grounded and all outputs open.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORMS



NOTES:
All inputs: $t_r = t_f = 5ns$ (10% to 90%)
All AC parameters are measured at 1.5V unless otherwise specified.

82US23
82US123
256-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82US23 and 82US123 are field programmable, which means that custom patterns are immediately available by following the Signetics Generic III fusing procedure. The 82US23 and 82US123 devices are supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ti-W link matrix.

These devices include on-chip decoding and 1 Chip Enable input for memory expansion. They feature either Open Collector or 3-State outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

The 82US23 and 82US123 devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

FEATURES

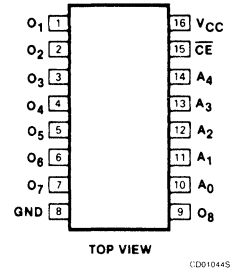
- **Address access time:**
  - **82US23: 13ns max**
  - **82US123: 10ns max**
- **Power dissipation: 2.3mW/bit typ**
- **Input loading: −100μA max**
- **On-chip address decoding**
- **One Chip Enable input**
- **Output options:**
  - **N82US23: Open Collector**
  - **N82US123: 3-State**
- **No separate fusing pins**
- **Unprogrammed outputs are Low level**
- **Fully TTL compatible**

APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Format conversion**
- **Hardwired algorithms**
- **Random logic**
- **Code conversion**

PIN CONFIGURATIONS

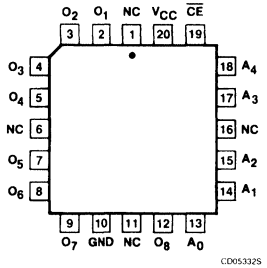
N, D Packages



TOP VIEW

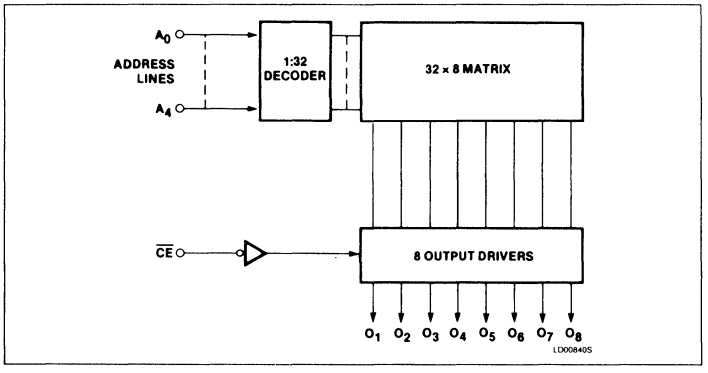
CD01044S

A Package



CD05332S

LOGIC DIAGRAM



ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-pin Plastic DIP 300mil-wide	N82US23 N • N82US123 N
16-pin Plastic SOL 300mil-wide	N82US23 D • N82US123 D
20-pin Plastic Leaded Chip Carrier 350mil-square	N82US23 A • N82US123 A

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_{OH} V_O	Output voltage High (82US23) Off-state (82US123)	+5.5 +5.5	V_{DC}
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temperature range	−65 to +150	°C

NOTE:

1. Stress above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any conditions other than those described in the AC and DC Electrical Characteristics section of this specification is not implied.

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS[1, 2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage						
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			V
V_{IC}	Clamp	$I_{IN} = -18mA$			−1.2	V
Output voltage						
		$\overline{CE}$ = Low				
V_{OL}	Low	$I_{OUT} = 16mA$			0.45	V
V_{OH}	High	$I_{OUT} = -2mA$	2.4			V
Input current						
I_{IL}	Low	$V_{IN} = 0.45V$			−250	μA
I_{IH}	High	$V_{IN} = 5.5V$			50	μA
Output current						
I_{OLK}	Leakage (82US23)	$\overline{CE}$ = High, $V_{OUT} = 5.5V$			40	μA
I_{OZ}	Hi-Z State (82US123)	$\overline{CE}$ = High, $V_{OUT} = 5.5V$			40	
		$\overline{CE}$ = High, $V_{OUT} = 0.5V$			−40	
I_{OS}	Short circuit (82US123)[3]	$\overline{CE}$ = Low, V_{OUT} = 0V, High stored	−15		−90	mA
Supply current[7]						
I_{CC}		$V_{CC} = 5.25V$			115	mA
Capacitance						
		$\overline{CE}$ = High, $V_{CC} = 5.0V$				
C_{IN}	Input	$V_{IN} = 2.0V$		5		pF
C_{OUT}	Output	$V_{OUT} = 2.0V$		8		pF

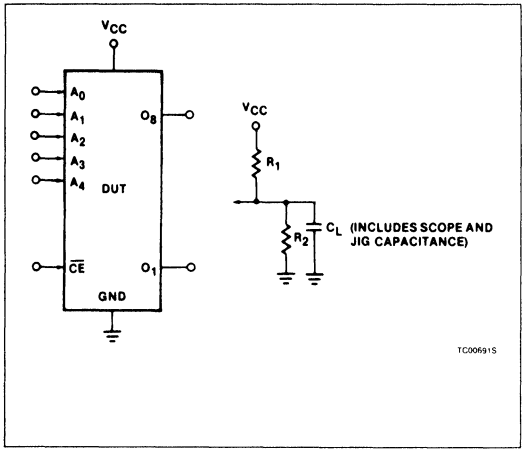
Notes on following page.

AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

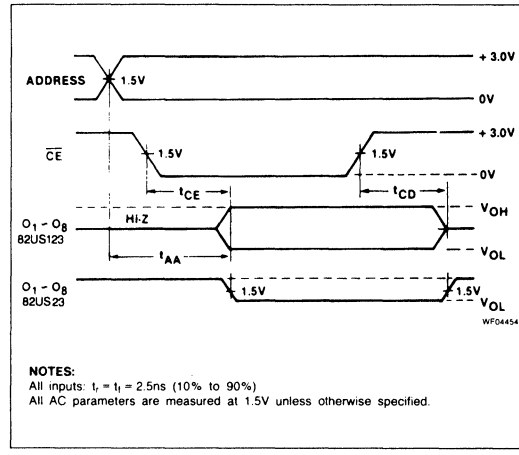
SYMBOL	PARAMETER	TO	FROM	N82US23			N82US123			UNIT
				Min	Typ[5]	Max	Min	Typ[5]	Max	
Access time[4]										
t_{AA}		Output	Address			13			10	ns
t_{CE}		Output	Chip Enable			8			7	ns
Disable time[6]										
t_{CD}		Output	Chip Enable			8			7	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μs.
5. Typical values are at $V_C = 5V$, $T_A = +25°C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
7. Measured with all inputs grounded and all outputs open.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



NOTES:
All inputs: $t_r = t_f = 2.5ns$ (10% to 90%)
All AC parameters are measured at 1.5V unless otherwise specified.

82S126
82S129
1K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82S126 and 82S129 are field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The 82S126 and 82S129 devices are supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

These devices include on-chip decoding and 2 Chip Enable inputs for ease of memory expansion. They feature either Open Collector or 3-State outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

The 82S126 and 82S129 devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

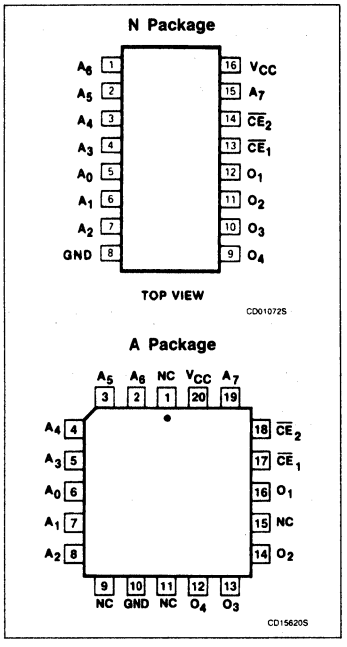
FEATURES

- **Address access time: 50ns max**
- **Power dissipation: 0.5mW/bit typ**
- **Input loading: −100μA max**
- **On-chip address decoding**
- **Two Chip Enable inputs**
- **Output options:**
  - **N82S126: Open Collector**
  - **N82S129: 3-State**
- **No separate fusing pins**
- **Unprogrammed outputs are Low level**
- **Fully TTL compatible**

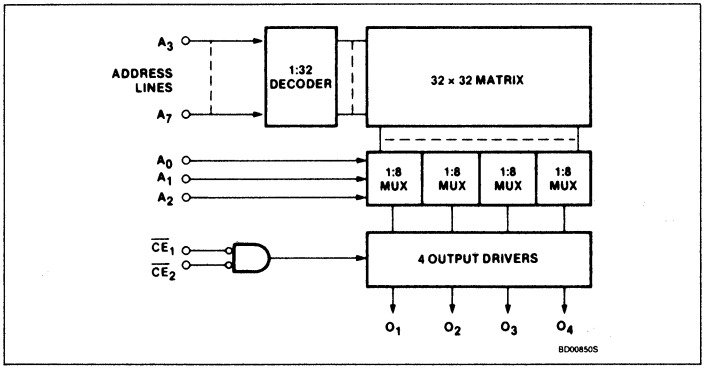
APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATIONS



BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-pin Plastic DIP 300mil-wide	N82S126 N • N82S129 N
20-pin Plastic Leaded Chip Carrier 350mil-square	N82S126 A • N82S129 A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_{OH} V_O	Output voltage High (82S126) Off-State (82S129)	+5.5 +5.5	V_{DC}
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temperature range	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage						
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			V
V_{IC}	Clamp	$I_{IN} = -12mA$			−1.2	V
Output voltage						
		$\overline{CE}_{1,2}$ = Low				
V_{OL}	Low	I_{OUT} = 16mA			0.45	V
V_{OH}	High (82S129)	$I_{OUT} = -2.0mA$	2.4			V
Input current						
I_{IL}	Low	$V_{IN} = 0.45V$			−100	μA
I_{IH}	High	$V_{IN} = 5.5V$			40	μA
Output current						
I_{OLK}	Leakage (82S126)	$\overline{CE}_1$ or $\overline{CE}_2$ = High, $V_{OUT} = 5.5V$			40	μA
I_{OZ}	Hi-Z State (82S129)	$\overline{CE}_1$ or $\overline{CE}_2$ = High, $V_{OUT} = 5.5V$			40	
		$\overline{CE}_1$ or $\overline{CE}_2$ = High, $V_{OUT} = 0.5V$			−40	
I_{OS}	Short circuit (82S129)[3]	$\overline{CE}_{1,2}$ = Low, $V_{OUT} = 0V$, High stored	−15		−70	mA
Supply current[7]						
I_{CC}		$V_{CC} = 5.25V$			120	mA
Capacitance						
		$\overline{CE}_1$ or $\overline{CE}_2$ = High, $V_{CC} = 5.0V$				
C_{IN}	Input	$V_{IN} = 2.0V$		5		pF
C_{OUT}	Output	$V_{OUT} = 2.0V$		8		pF

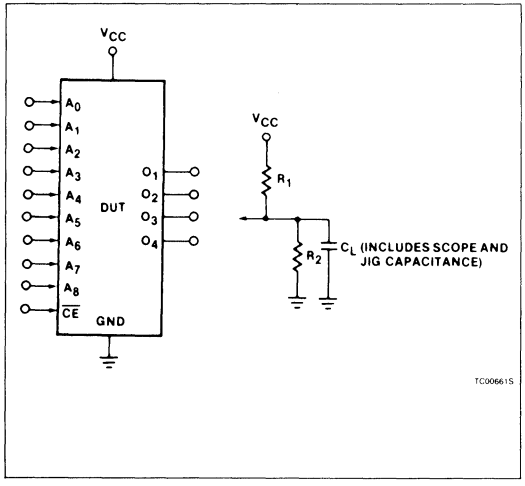
Notes on following page.

AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

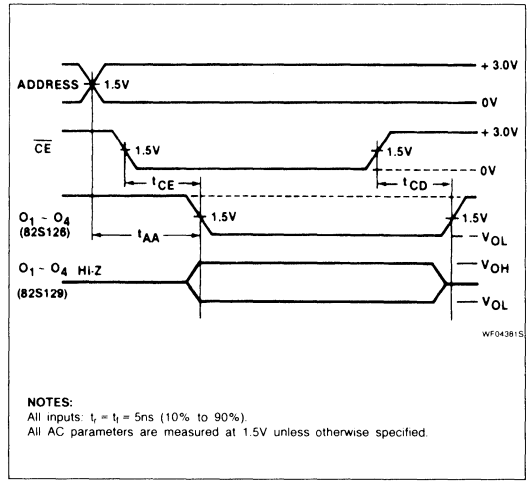
SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[5]	Max	
Access time[4]							
t_{AA}		Output	Address		40	50	ns
t_{CE}		Output	Chip Enable			25	ns
Disable time[6]							
t_{CD}		Output	Chip Disable			25	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μs.
5. Typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
7. Measured with all inputs grounded and all outputs open.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORMS



NOTES:
All inputs: $t_r = t_f = 5ns$ (10% to 90%).
All AC parameters are measured at 1.5V unless otherwise specified.

82S126A
82S129A
1K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82S126A and 82S129A are field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The 82S126A and 82S129A devices are supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

These devices include on-chip decoding and 2 Chip Enable inputs for ease of memory expansion. They feature either Open Collector or 3-State outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

The 82S126A and 82S129A devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

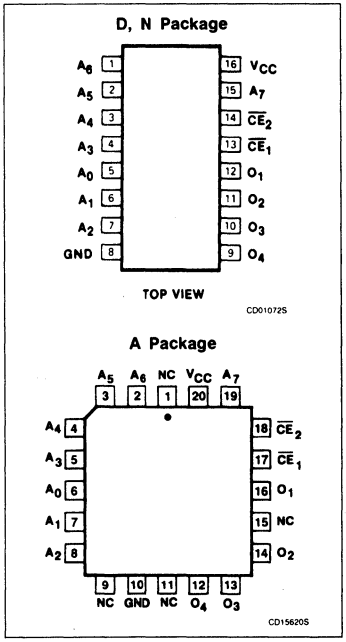
FEATURES

- **Address access time:**
  - **N82S126A: 30ns max**
  - **N82S129A: 27ns max**
- **Power dissipation: 0.5mW/bit typ**
- **Input loading: −100μA max**
- **On-chip address decoding**
- **Two Chip Enable inputs**
- **Output options:**
  - **82S126A: Open-Collector**
  - **82S129A: 3-State**
- **No separate fusing pins**
- **Unprogrammed outputs are Low level**
- **Fully TTL compatible**

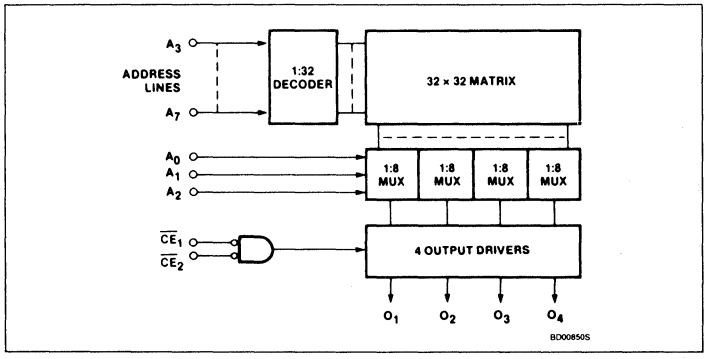
APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATIONS



BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-pin Plastic DIP 300mil-wide	N82S126A N • N82S129A N
16-pin Plastic SO 300mil-wide	N82S126A D • N82S129A D
20-pin Plastic Leaded Chip Carrier 350mil-square	N82S126A A • N82S129A A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_{OH} V_O	Output voltage High (82S126) Off-state (82S129)	 +5.5 +5.5	V_{DC}
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temperature range	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage						
V_{IL}	Low	V_{CC} = 4.75V			0.8	V
V_{IH}	High	V_{CC} = 5.25V	2.0			V
V_{IC}	Clamp	V_{CC} = 4.75V, I_{IN} = −12mA			−1.2	V
Output voltage						
		$\overline{CE}_{1,2}$ = Low				
V_{OL}	Low	I_{OUT} = 16mA			0.45	V
V_{OH}	High (82S129A)	I_{OUT} = −2.0mA	2.4			V
Input current						
I_{IL}	Low	V_{IN} = 0.45V			−100	μA
I_{IH}	High	V_{IN} = 5.5V			40	μA
Output current						
I_{OLK}	Leakage (82S126A)	$\overline{CE}_1$ or $\overline{CE}_2$ = High, V_{OUT} = 5.5V			40	μA
I_{OZ}	Hi-Z State (82S129A)	$\overline{CE}_1$ or $\overline{CE}_2$ = High, V_{OUT} = 5.5V			40	
		$\overline{CE}_1$ or $\overline{CE}_2$ = High, V_{OUT} = 0.5V			−40	
I_{OS}	Short circuit (82S129A)[3]	$\overline{CE}_{1,2}$ = Low, V_{OUT} = 0V, High stored	−15		−70	mA
Supply current[7]						
I_{CC}		V_{CC} = 5.25V			120	mA
Capacitance						
		$\overline{CE}_1$ or $\overline{CE}_2$ = High, V_{CC} = 5.0V				
C_{IN}	Input	V_{IN} = 2.0V		5		pF
C_{OUT}	Output	V_{OUT} = 2.0V		8		pF

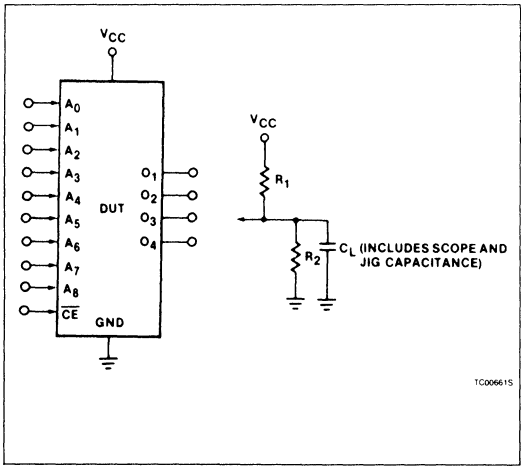
Notes on following page.

AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

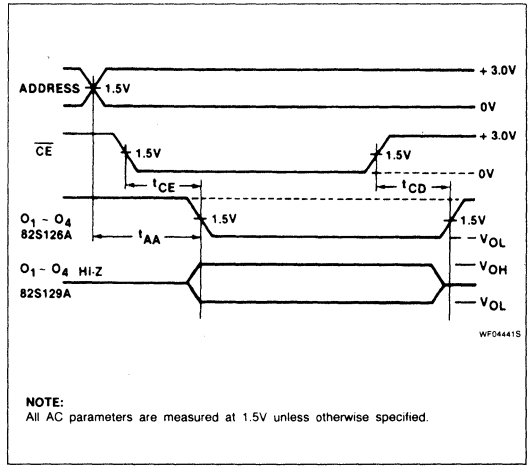
SYMBOL	PARAMETER	TO	FROM	N82S129A			N82S126A			UNIT
				Min	Typ[5]	Max	Min	Typ[5]	Max	
Access time[4]										
t_{AA}		Output	Address		17	27		17	30	ns
t_{CE}		Output	Chip Enable		10	20		10	20	ns
Disable time[6]										
t_{CD}		Output	Chip Enable		6	15		6	15	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μs.
5. Typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
7. Measured with all inputs grounded and all outputs open.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORMS



NOTE:
All AC parameters are measured at 1.5V unless otherwise specified.

82S130
82S131
2K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82S130 and 82S131 are field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The standard 82S130 and 82S131 are supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

These devices include on-chip decoding and 1 Chip Enable input for ease of memory expansion. They feature either Open Collector or 3-State outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

The 82S130 and 82S131 devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

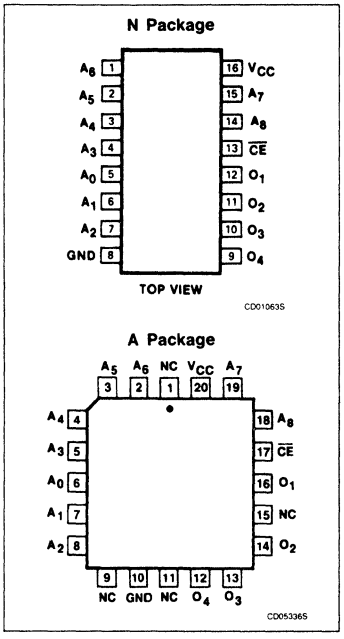
FEATURES

- **Address access time: 50ns max**
- **Power dissipation: 0.3mW/bit typ**
- **Input loading: −100μA max**
- **On-chip address decoding**
- **One Chip Enable input**
- **Output options:**
  - **N82S130: Open-Collector**
  - **N82S131: 3-State**
- **No separate fusing-pins**
- **Unprogrammed outputs are Low level**
- **Fully TTL compatible**

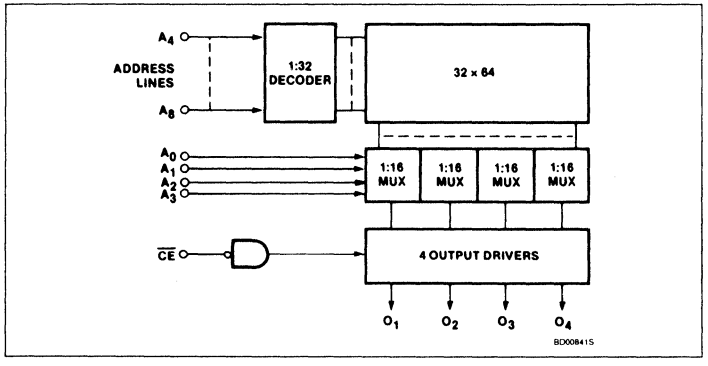
APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATIONS



BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-pin Plastic DIP 300mil-wide	N82S130 N • N82S131 N
20-pin Plastic Leaded Chip Carrier 350mil-square	N82S130 A • N82S131 A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_{OH} V_O	Output voltage High (82S130) Off-State (83S131)	+5.5 +5.5	V_{DC}
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temperature range	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage						
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			V
V_{IC}	Clamp	I_{IN} = −12mA			−1.2	V
Output voltage						
		$\overline{CE}$ = Low				
V_{OL}	Low	I_{OUT} = 16mA			0.45	V
V_{OH}	High (82S131)	I_{OUT} = −2mA	2.4			V
Input current						
I_{IL}	Low	V_{IN} = 0.45V			−100	μA
I_{IH}	High	V_{IN} = 5.5V			40	μA
Output current						
I_{OLK}	Leakage (82S130)	$\overline{CE}$ = High, V_{OUT} = 5.5V,			40	μA
I_{OZ}	Hi-Z State (82S131)	$\overline{CE}$ = High, V_{OUT} = 5.5V			40	μA
		$\overline{CE}$ = High, V_{OUT} = 0.5V			−40	
I_{OS}	Short circuit (82S131)[3]	$\overline{CE}$ = Low, V_{OUT} = 0V, High stored	−15		−70	mA
Supply current[7]						
I_{CC}		V_{CC} = 5.25V			140	mA
Capacitance						
		$\overline{CE}$ = High, V_{CC} = 5.0V				
C_{IN}	Input	V_{IN} = 2.0V		5		pF
C_{OUT}	Output	V_{OUT} = 2.0V		8		pF

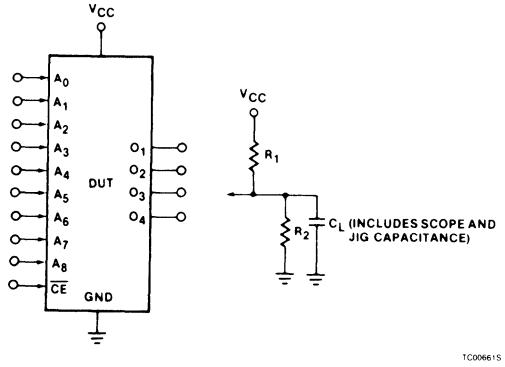
Notes on following page.

AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[5]	Max	
Access time[4]							
t_{AA}		Output	Address			50	ns
t_{CE}		Output	Chip Enable			30	ns
Disable time[6]							
t_{CD}		Output	Chip Disable			30	ns

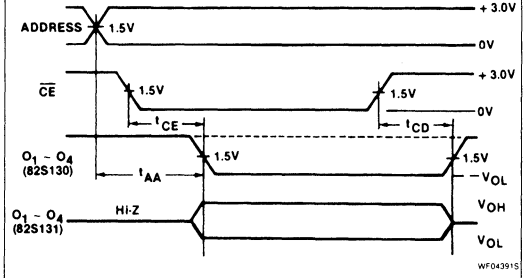
NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1 μs.
5. Typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
7. Measured with all inputs grounded and all outputs open.

TEST LOAD CIRCUIT



NOTE:
All inputs $t_r = t_f = 5ns$ (10% to 90%).

VOLTAGE WAVEFORMS



NOTE:
All AC parameters are measured at 1.5V unless otherwise specified.

Read Cycle

82S130A
82S131A
2K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82S130A and 82S131A are field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The standard 82S130A and 82S131A are supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

These devices include on-chip decoding and 1 Chip Enable input for ease of memory expansion. They feature either Open Collector or 3-State outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

The 82S130A and 82S131A devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

FEATURES

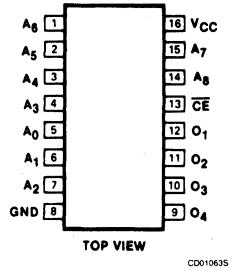
- **Address access time:**
  - **N82S130A: 33ns max**
  - **N82S131A: 30ns max**
- **Power dissipation: 0.3mW/bit typ**
- **Input loading: −100μA max**
- **On-chip address decoding**
- **One Chip Enable input**
- **Output options:**
  - **N82S130A: Open-Collector**
  - **N82S131A: 3-State**
- **No separate fusing pins**
- **Unprogrammed outputs are Low level**
- **Fully TTL compatible**

APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATIONS

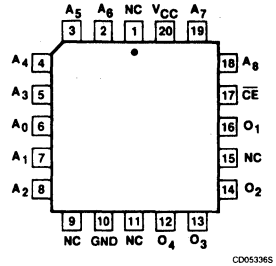
D, N Package



TOP VIEW

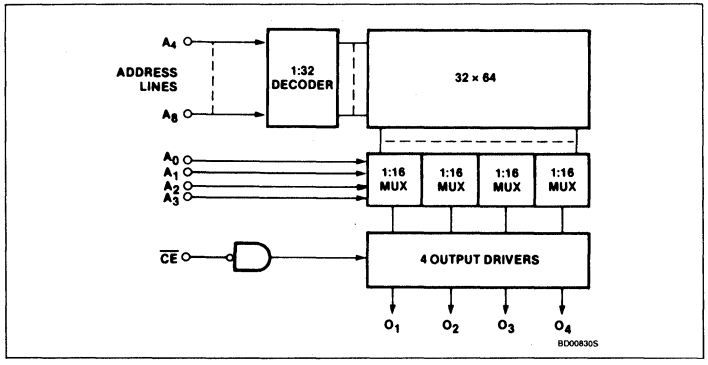
CD01063S

A Package



CD05336S

BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-pin Plastic DIP 300mil-wide	N82S130A N • N82S131A N
16-pin Plastic SO 300mil-wide	N82S130A D • N82S131A D
20-pin Plastic Leaded Chip Carrier 350mil-square	N82S130A A • N82S131A A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_{OH} V_O	Output voltage High (82S130) Off-State (82S131)	+5.5 +5.5	V_{DC}
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temperature range	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS[1, 2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage						
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			V
V_{IC}	Clamp	$I_{IN} = -12mA$			−1.2	V
Output voltage						
		$\overline{CE}$ = Low				
V_{OL}	Low	$I_{OUT} = 16mA$			0.45	V
V_{OH}	High (82S131)	$I_{OUT} = -2mA$	2.4			V
Input current						
I_{IL}	Low	$V_{IN} = 0.45V$			−100	μA
I_{IH}	High	$V_{IN} = 5.5V$			40	μA
Output current						
I_{OLK}	Leakage (82S130A)	$\overline{CE}$ = High, $V_{OUT} = 5.5V$			40	μA
I_{OZ}	Hi-Z State (82S131A)	$\overline{CE}$ = High, $V_{OUT} = 5.5V$			40	μA
		$\overline{CE}$ = High, $V_{OUT} = 0.5V$			−40	
I_{OS}	Short circuit (82S131A)[3]	$\overline{CE}$ = Low, V_{OUT} = 0V, High stored	−15		−70	mA
Supply current[7]						
I_{CC}		$V_{CC} = 5.25V$			140	mA
Capacitance						
		$\overline{CE}$ = High, $V_{CC} = 5.0V$				
C_{IN}	Input	$V_{IN} = 2.0V$		5		pF
C_{OUT}	Output	$V_{OUT} = 2.0V$		8		pF

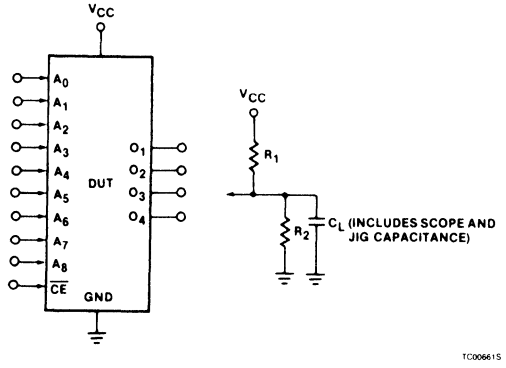
Notes on following page.

AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TO	FROM	N82S131A			N82S130A			UNIT
				Min	Typ[5]	Max	Min	Typ[5]	Max	
Access time[4]										
t_{AA}		Output	Address		18	30		18	33	ns
t_{CE}		Output	Chip Enable		10	20		10	20	ns
Disable time[6]										
t_{CD}		Output	Chip Enable		6	15		6	15	ns

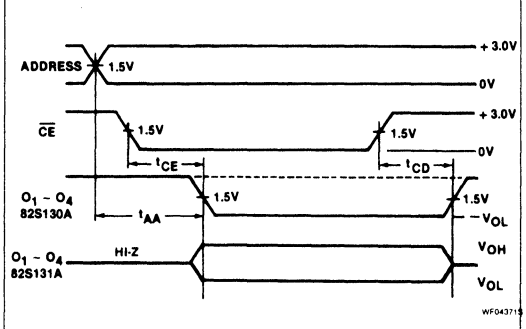
NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μs.
5. Typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
7. Measured with all inputs grounded and all outputs open.

TEST LOAD CIRCUIT



NOTE:
All inputs $t_r = t_f = 5ns$ (10% to 90%).

VOLTAGE WAVEFORMS



NOTE:
All AC parameters are measured at 1.5V unless otherwise specified.

Read Cycle

82S135
2K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82S135 is field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The standard devices are supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

The 82S135 includes on-chip decoding and two Chip Enable inputs for ease of memory expansion, and features 3-State outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

The 82S135 devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

FEATURES

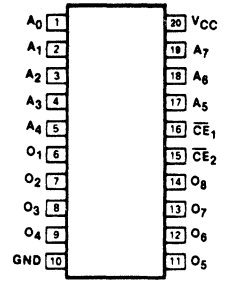
- **Address access time: 45ns max**
- **Power dissipation: 329μW/bit typ**
- **Input loading: -100μA max**
- **Two Chip Enable inputs**
- **On-chip address decoding**
- **No separate fusing pins**
- **Fully TTL compatible**
- **Outputs: 3-State**
- **Unprogrammed outputs are Low level**

APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATIONS

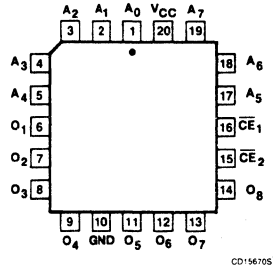
D, N Package



TOP VIEW

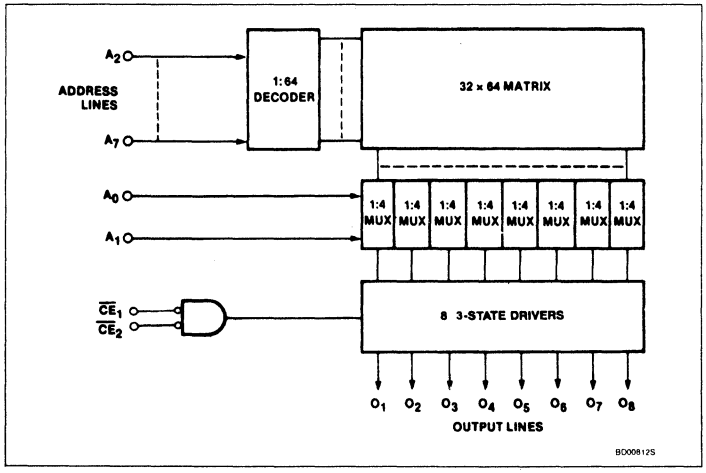
CD01033S

A Package



CD15670S

BLOCK DIAGRAM



2K-Bit TTL Bipolar PROM (256 × 8) 82S135

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
20-pin Plastic DIP 300mil-wide	N82S135 N
20-pin Plastic SO 300mil-wide	N82S135 D
20-pin Plastic Leaded Chip Carrier 350mil-square	N82S135 A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Power supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-State	+5.5	V_{DC}
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temperature range	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage						
V_{IL}	Low	V_{CC} = 4.75V			0.8	V
V_{IH}	High	V_{CC} = 5.25V	2.0			V
V_{IC}	Clamp	I_{IN} = −12mA			−1.2	V
Output voltage						
V_{OL}	Low	I_{OUT} = 9.6mA			0.5	V
V_{OH}	High	$\overline{CE}_1$, $\overline{CE}_2$ = Low, I_{OUT} = −2mA, High stored	2.4			V
Input current						
I_{IL}	Low	V_{IN} = 0.45V			−100	μA
I_{IH}	High	V_{IN} = 5.5V			40	μA
Output current						
I_{OZ}	Hi-Z State	$\overline{CE}_1$, $\overline{CE}_2$ = High, V_{OUT} = 0.5V			−40	μA
		$\overline{CE}_1$, $\overline{CE}_2$ = High, V_{OUT} = 5.5V			40	
I_{OS}	Short circuit[3]	$\overline{CE}_1$, $\overline{CE}_2$ = Low, V_{OUT} = 0V, High stored	−15		−75	mA
Supply current[7]						
I_{CC}		V_{CC} = 5.25V		135	150	mA
Capacitance						
		V_{CC} = 5.0V, $\overline{CE}$ = High				
C_{IN}	Input	V_{IN} = 2.0V		5		pF
C_{OUT}	Output	V_{OUT} = 2.0V		8		pF

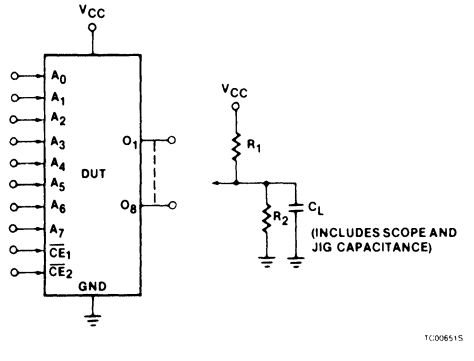
Notes on following page.

AC ELECTRICAL CHARACTERISTICS $R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

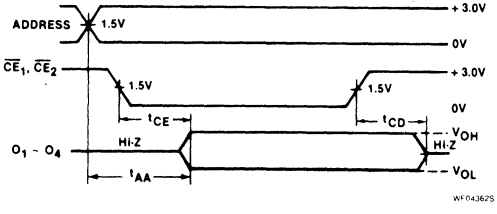
SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[5]	Max	
Access time[4]							
t_{AA}		Output	Address		40	45	ns
t_{CE}		Output	Chip Enable		20	25	ns
Disable time[6]							
t_{CD}		Output	Chip Disable		20	35	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μs.
5. Typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
7. Measured with all inputs grounded and all outputs open.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORMS



NOTE:
All AC parameters are measured at 1.5V unless otherwise specified.

82LS135
2K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82LS135 is field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The standard devices are supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

The 82LS135 includes on-chip decoding and two Chip Enable inputs for ease of memory expansion, and features 3-State outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

FEATURES

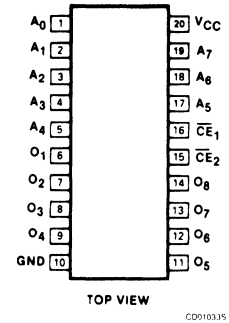
- **Address access time: 100ns max**
- **Power dissipation: 200μW/bit typ**
- **Input loading: −100μA max**
- **Two Chip Enable inputs**
- **On-chip address decoding**
- **No separate fusing pins**
- **Fully TTL compatible**
- **Unprogrammed outputs are at Low level**
- **Outputs: 3-State**

APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATIONS

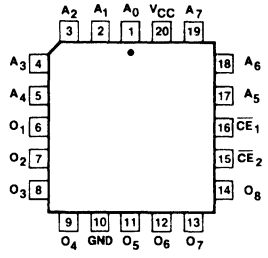
D, N Package



TOP VIEW

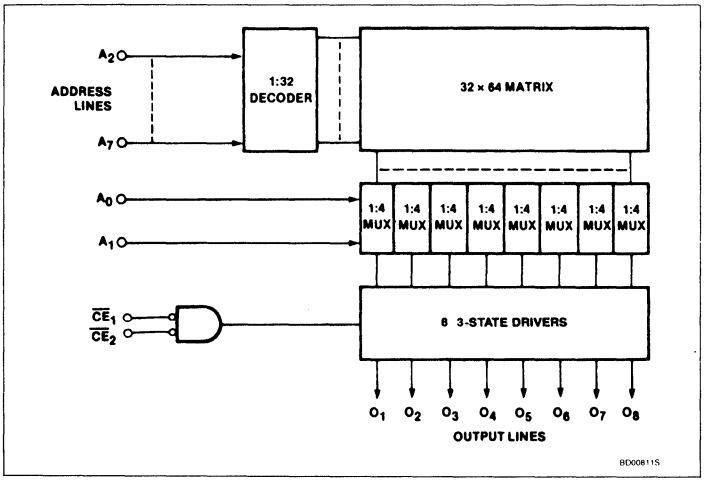
CD01033S

A Package



CD15680S

BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	ORDER CODE
20-pin Plastic DIP 300mil-wide	N82LS135 N
20-pin Plastic SO 300mil-wide	N82LS135 D
20-pin Plastic Leaded Chip Carrier 350mil-square	N82LS135 A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-state	+5.5	V_{DC}
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temperature range	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage						
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			V
V_{IC}	Clamp	$I_{IN} = -12mA$			−1.2	V
Output voltage						
V_{OL}	Low	$I_{OUT} = 16mA$			0.5	V
V_{OH}	High	$I_{OUT} = -2mA$, High stored	2.4			V
Input current						
I_{IL}	Low	$V_{IN} = 0.45V$			−100	μA
I_{IH}	High	$V_{IH} = 5.5V$			40	μA
Output current						
I_{OZ}	Hi-Z State	$\overline{CE}_1$, $\overline{CE}_2$ = High, $V_{OUT} = 0.5V$			−40	μA
		$\overline{CE}_1$, $\overline{CE}_2$ = High, $V_{OUT} = 5.5V$			40	
I_{OS}	Short circuit[3]	$\overline{CE}_1$, $\overline{CE}_2$ = Low, $V_{OUT} = 0V$, High stored	−15		−75	mA
Supply current[7]						
I_{CC}		$V_{CC} = 5.25V$		80	100	mA
Capacitance						
		$V_{CC} = 5.0V$, $\overline{CE}$ = High				
C_{IN}	Input	$V_{IN} = 2.0V$		5		pF
C_{OUT}	Output	$V_{OUT} = 2.0V$		8		pF

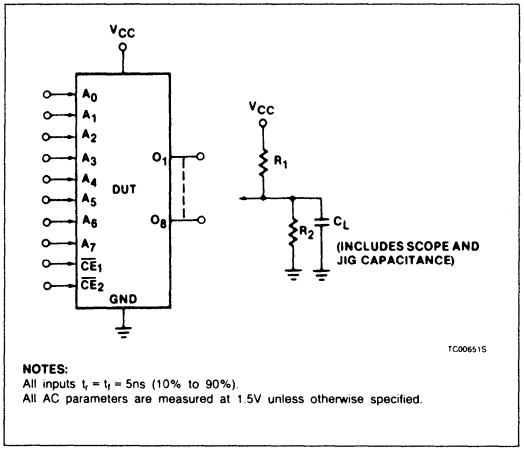
Notes on following page.

AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[5]	Max	
Access time[4]							
t_{AA}		Output	Address		70	100	ns
t_{CE}		Output	Chip Enable		30	50	ns
Disable time[6]							
t_{CD}		Output	Chip Disable		30	60	ns

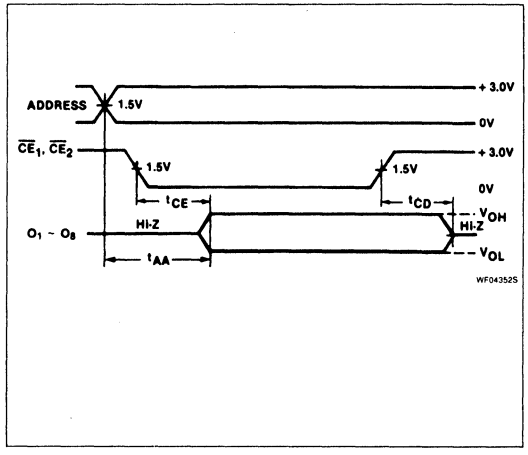
NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μs.
5. Typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
7. Measured with all inputs grounded and all outputs open.

TEST LOAD CIRCUIT



NOTES:
All inputs $t_r = t_f = 5ns$ (10% to 90%).
All AC parameters are measured at 1.5V unless otherwise specified.

VOLTAGE WAVEFORMS



4K-bit TTL PROM

		page
82S115	4096-bit PROM (512 x 8) 60 ns	381
82S137	4096-bit PROM (1024 x 4) 60 ns	385
82S137A	4096-bit PROM (1024 x 4) 45 ns	389
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82S141A	4096-bit PROM (512 x 8) 45 ns	393
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82S147A	4096-bit PROM (512 x 8) 45 ns	397
82S147B	4096-bit PROM (512 x 8) 25 ns	401

82S115
4K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82S115 is field programmable and includes on-chip decoding and 2 chip enable inputs for ease of memory expansion. It features 3-State outputs for optimization of word expansion in bused organizations. A D-type latch is used to enable the 3-State output drivers. In the Transparent Read mode, stored data is addressed by applying a binary code to the address inputs while holding Strobe High. In this mode the bit drivers will be controlled solely by $\overline{CE}_1$ and CE_2 lines.

In the Latched Read mode, outputs are held in their previous state (High, Low, or Hi-Z) as long as Strobe is Low, regardless of the state of Address or Chip Enable. A positive Strobe transition causes data from the applied address to reach the outputs if the chip is enabled, and causes outputs to go to the Hi-Z State if the chip is disabled.

A negative Strobe transition causes outputs to be locked into their last Read Data condition if the chip was enabled, or causes outputs to be locked into the Hi-Z condition if the chip was disabled.

Ordering information can be found on the following page.

This device is also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

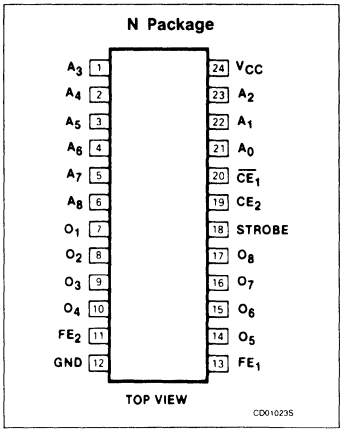
FEATURES

- **Address access time: 60ns max**
- **Power dissipation: 165μW/bit typ**
- **Input loading: -100μA max**
- **Two Chip Enable inputs**
- **On-chip storage latches**
- **Schottky clamped**
- **Fully TTL compatible**
- **Outputs: 3-State**

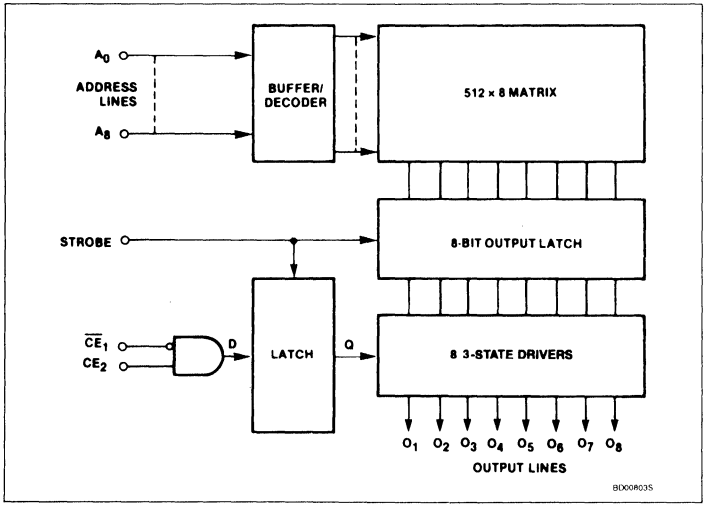
APPLICATIONS

- **Microprogramming**
- **Hardware algorithms**
- **Character generation**
- **Control store**
- **Sequential controllers**

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	ORDERING CODE
24-pin Plastic DIP 600mil-wide	N82S115 N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temperature range	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS[5]	LIMITS			UNIT
			Min	Typ[6]	Max	
Input voltage						
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			V
V_{IC}	Clamp	$I_{IN} = -12mA$		−0.8	−1.2	V
Output voltage						
		$\overline{CE}_1$ = Low, CE_2 = High				
V_{OL}	Low	$I_{OUT} = 9.6mA$		0.4	0.45	V
V_{OH}	High	$I_{OUT} = -2mA$	2.7			V
Input current[5]						
I_{IL}	Low	$V_{IN} = 0.45V$			−100	μA
I_{IH}	High	$V_{IN} = 5.5V$			25	μA
Output current[5]						
I_{OZ}	Hi-Z State	$\overline{CE}_1$ = High or CE_2 = Low, $V_{OUT} = 5.5V$			40	μA
		$\overline{CE}_1$ = High or CE_2 = Low, $V_{OUT} = 0.5V$			−40	
I_{OS}	Short circuit[1]	$\overline{CE}_1$ = Low, CE_2 = High, $V_{OUT} = 0V$, High stored	−15		−70	mA
Supply current[10]						
I_{CC}		$V_{CC} = 5.25V$		130	175	mA
Capacitance						
		$\overline{CE}_1$ = High or CE_2 = Low, $V_{CC} = 5.0V$				
C_{IN}	Input	$V_{IN} = 2.0V$		5		pF
C_{OUT}	Output	$V_{OUT} = 2.0V$		8		pF

Notes on following page.

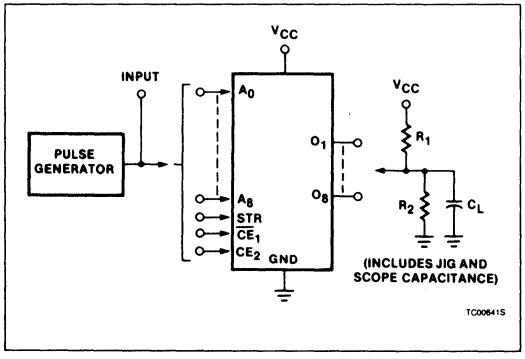
AC ELECTRICAL CHARACTERISTICS $R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$, $0° \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TO	FROM	TEST CONDITIONS	LIMITS			UNIT
					Min	Typ[8]	Max	
Access time[6]								
t_{AA} t_{CE}		Output Output	Address Chip Enable	Latched or transparent Read[2,4]		40 20	60 40	ns ns
Disable time[9]								
t_{CD}		Output	Chip Disable	Latched or transparent Read[2,4]		20	40	ns
Setup and hold time								
t_{CDS} t_{CDH}	Setup time Hold time	Output	Chip Enable	Latched Read only[3,4]	40 10			ns ns
Hold time								
t_{ADH}	Hold time	Address	Strobe	Latched Read only[3,4]		0		ns
Pulse Width								
t_{SW}	Strobe			Latched Read only[3,4]	30	15		ns
Latch time								
t_{SL}	Strobe			Latched Read only[3,4]	60	35		ns
Delatch time[9]								
t_{DL}	Strobe			Latched Read only[3,4]			35	ns

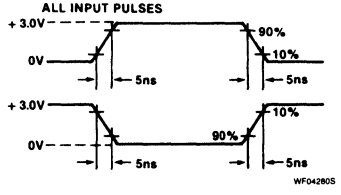
NOTES:

1. No more than one output should be grounded at the same time and strobe should be disabled Strobe is in the High state.
2. If the Strobe is High, the device functions in a manner identical to conventional bipolar ROMs. The timing diagram shows valid data will appear T_{AA} nanoseconds after the address has changed or T_{CE} nanoseconds after the output circuit is enabled.
3. In latched Read Mode data from any selected address will be held on the output when Strobe is lowered only when Strobe is raised will new location data be transferred and chip enable conditions be stored. The new data will appear on the outputs if the chip enable conditions enable the outputs.
4. During operation the fusing pins FE_1 and FE_2 must be grounded or left floating.
5. Positive current is defined as into the terminal referenced.
6. Tested at an address cycle time of 1μs.
7. Areas shown by crosshatch are latched data from previous address.
8. Typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
9. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$, and $C_L = 5pF$.
10. Measured with all inputs grounded and all outputs open.

TEST LOAD CIRCUIT

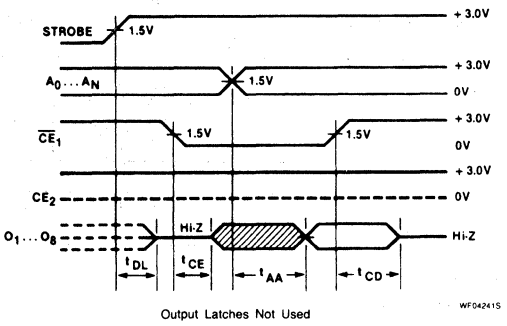


VOLTAGE WAVEFORMS



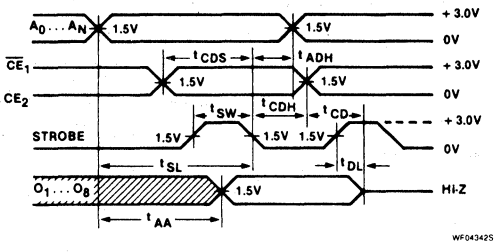
Input Pulses

TIMING DIAGRAM



Output Latches Not Used

Transparent Read[2, 7]



Output Latches Used

Latched Read[3, 7]

82S137
4K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82S137 is field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The 82S137 is supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

These devices include on-chip decoding and 2 Chip Enable inputs for ease of memory expansion. They feature 3-State outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

The 82S137 devices are also processed to military requirements for operation over the military temperature range, for specifications and ordering information consult the Signetics Military Data Book.

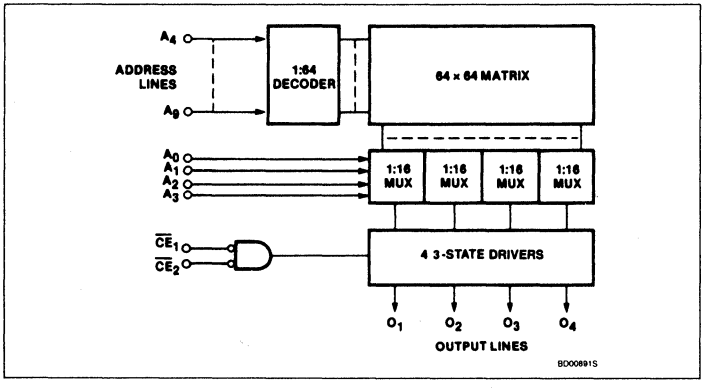
FEATURES

- **Address access time: 60ns max**
- **Power dissipation: 0.13mW/bit typ**
- **Input loading: −100μA max**
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are Low level**
- **Fully TTL compatible**
- **Two Chip Enable inputs**
- **Outputs: 3-State**

APPLICATIONS

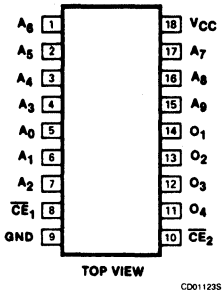
- **Sequential controllers**
- **Control store**
- **Random logic**
- **Code conversion**

BLOCK DIAGRAM

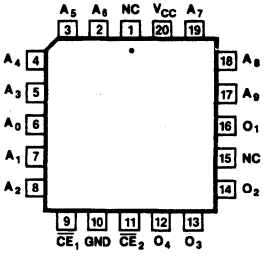


PIN CONFIGURATIONS

N Package



A Package



ORDERING INFORMATION

DESCRIPTION	ORDER CODE
18-pin Plastic DIP 300mil-wide	N82S137 N
20-pin Plastic Leaded Chip Carrier 350mil-square	N82S137 A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-state	+5.5	V_{DC}
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temperature range	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leqslant T_A \leqslant +75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage						
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			V
V_{IC}	Clamp	$I_{IN} = -12mA$			−1.2	V
Output voltage						
		$\overline{CE}_{1,2}$ = Low				
V_{OL}	Low	$I_{OUT} = 16mA$			0.45	V
V_{OH}	High	$I_{OUT} = -2mA$	2.4			V
Input current						
I_{IL}	Low	$V_{IN} = 0.45V$			−100	μA
I_{IH}	High	$V_{IN} = 5.5V$			40	μA
Output current						
I_{OZ}	Hi-Z State	$\overline{CE}_{1,2}$ = High, $V_{OUT} = 0.5V$			−40	μA
		$\overline{CE}_{1,2}$ = High, $V_{OUT} = 5.5V$			40	
I_{OS}	Short circuit[3]	$\overline{CE}_{1,2}$ = Low, V_{OUT} = 0V, High stored	−15		−70	mA
Supply current[7]						
I_{CC}		$V_{CC} = 5.25V$			140	mA
Capacitance						
		$\overline{CE}_{1,2}$ = High, $V_{CC} = 5.0V$				
C_{IN}	Input	$V_{IN} = 2.0V$		5		pF
C_{OUT}	Output	$V_{OUT} = 2.0V$		8		pF

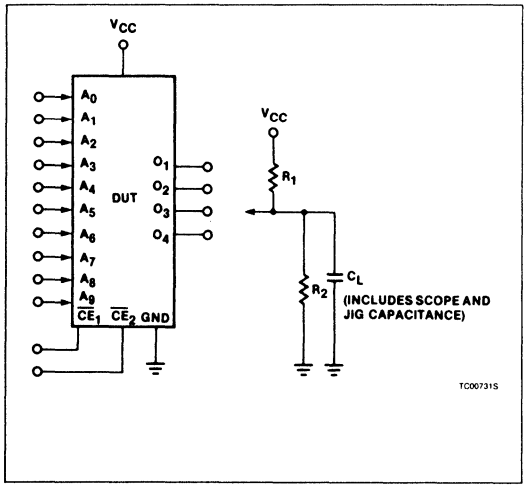
Notes on following page.

AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

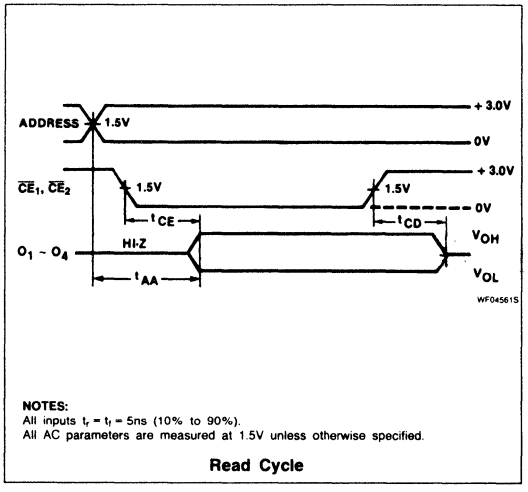
SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[5]	Max	
Access time[4]							
t_{AA}		Output	Address		40	60	ns
t_{CE}		Output	Chip Enable		25	30	ns
Disable time[6]							
t_{CD}		Output	Chip Enable		25	30	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μs.
5. Typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
7. Measured with all inputs grounded and all outputs open.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORMS



NOTES:
All inputs $t_r = t_f = 5ns$ (10% to 90%).
All AC parameters are measured at 1.5V unless otherwise specified.

Read Cycle

82S137A
82S137B
4K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82S137A and 82S137B are field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The 82S137A and 82S137B are supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

These devices include on-chip decoding and 2 Chip Enable inputs for ease of memory expansion. They feature 3-State outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

The 82S137A devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

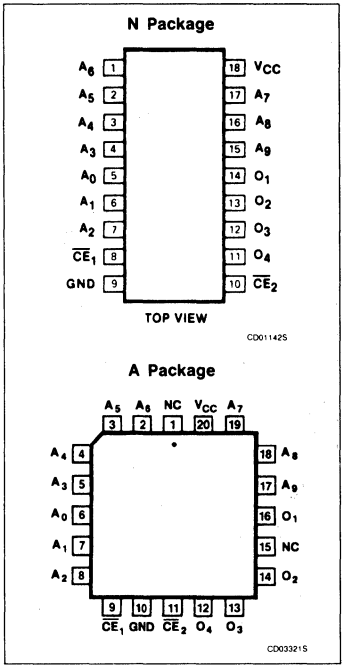
FEATURES

- **Address access time:**
  - **N82S137A: 45ns max**
  - **N82S137B: 35ns max**
- **Power dissipation: 0.13mW/bit typ**
- **Input loading: −100μA max**
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are Low level**
- **Fully TTL compatible**
- **Two Chip Enable inputs**
- **Outputs: 3-State**

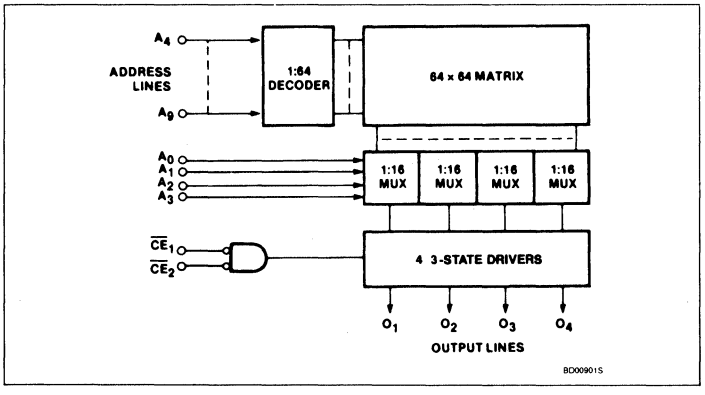
APPLICATIONS

- **Control store**
- **Sequential controllers**
- **Random logic**
- **Code conversion**

PIN CONFIGURATIONS



BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	ORDER CODE
18-pin Plastic DIP 300mil-wide	N82S137A N • N82S137B N
20-pin Plastic Leaded Chip Carrier 350mil-square	N82S137A A • N82S137B A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-State	+5.5	V_{DC}
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temperature range	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leqslant T_A \leqslant +75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25V$

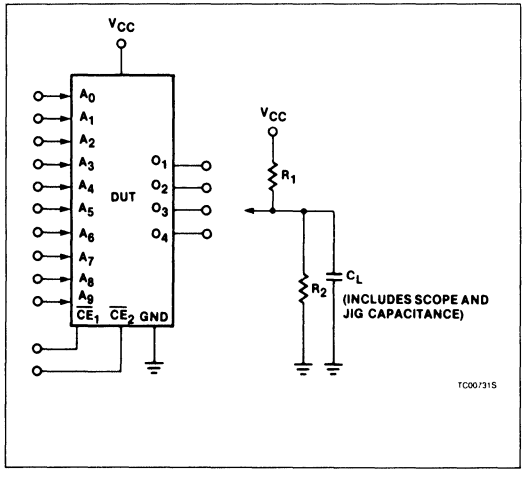
SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage						
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			V
V_{IC}	Clamp	$I_{IN} = -12mA$		−0.8	−1.2	V
Output voltage						
		$\overline{CE}_{1,2}$ = Low				
V_{OL}	Low	$I_{OUT} = 16mA$			0.45	V
V_{OH}	High	$I_{OUT} = -2mA$	2.4			V
Input current						
I_{IL}	Low	$V_{IN} = 0.45V$			−100	μA
I_{IH}	High	$V_{IN} = 5.5V$			40	μA
Output current						
I_{OZ}	Hi-Z State	$\overline{CE}_{1,2}$ = High, $V_{OUT} = 0.5V$			40	μA
		$\overline{CE}_{1,2}$ = High, $V_{OUT} = 5.5V$			−40	
I_{OS}	Short circuit[3]	$\overline{CE}_{1,2}$ = Low, $V_{OUT} = 0V$ High stored	−15		−70	mA
Supply current[7]						
I_{CC}		$V_{CC} = 5.25V$		85	140	mA
Capacitance						
		$\overline{CE}_{1,2}$ = High, $V_{CC} = 5.0V$				
C_{IN}	Input	$V_{IN} = 2.0V$		5		pF
C_{OUT}	Output	$V_{OUT} = 2.0V$		8		pF

AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

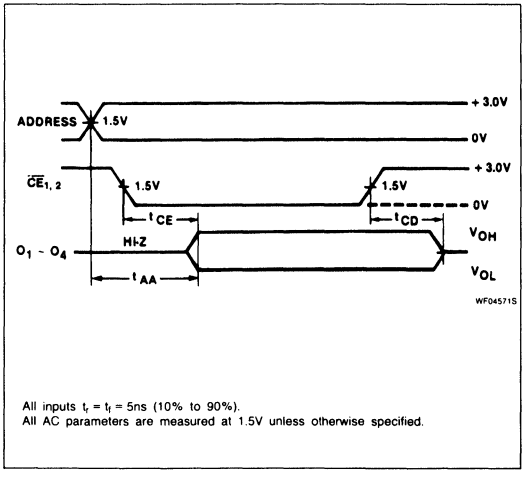
SYMBOL	PARAMETER	TO	FROM	N82S137A			N82S137B			UNIT
				Min	Typ[5]	Max	Min	Typ[5]	Max	
Access time[4]										
t_{AA}		Output	Address		35	45		30	35	ns
t_{CE}		Output	Chip Enable		20	30		15	25	ns
Disable time[6]										
t_{CD}		Output	Chip Disable		20	30		15	25	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μs.
5. Typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
7. Measured with all inputs grounded and all outputs open.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORMS



All inputs $t_r = t_f = 5ns$ (10% to 90%).
All AC parameters are measured at 1.5V unless otherwise specified.

82S141
82S141A
4K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82S141 and 82S141A are field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The 82S141 and 82S141A are supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

This device includes on-chip decoding and 4 Chip Enable inputs for ease of memory expansion. It features 3-State outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

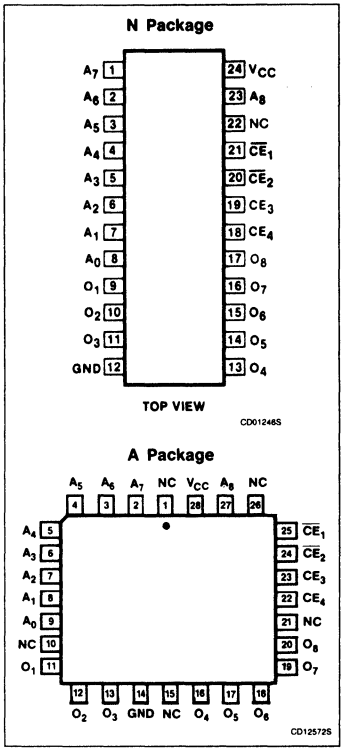
FEATURES

- **Address access time:**
  - **N82S141: 60ns max**
  - **N82S141A: 45ns max**
- **Power dissipation: 76μW/bit typ**
- **Input loading: −100μA max**
- **On-chip address decoding**
- **Four Chip Enable inputs**
- **Outputs: 3-State**
- **No separate fusing pins**
- **Unprogrammed outputs are Low level**
- **Fully TTL compatible**

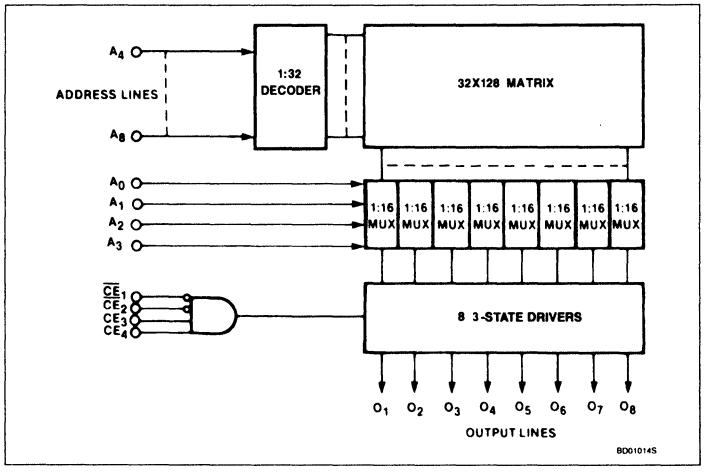
APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-pin Plastic DIP 300 mil-wide	N82S141 N3 • N82S141A N3
24-pin Plastic DIP 600mil-wide	N82S141 N • N82S141A N
28-pin Plastic Leaded Chip Carrier 450mil-square	N82S141A A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-state	+5.5	V_{DC}
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temperature range	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

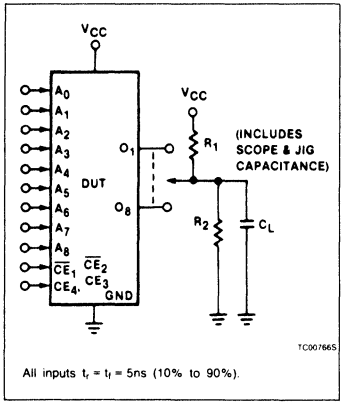
SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage[2]						
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			V
V_{IC}	Clamp	$I_{IN} = -12mA$		−0.8	−1.2	V
Output voltage[2]						
		$\overline{CE}_{1,2}$ = Low, $CE_{3,4}$ = High				
V_{OL}	Low	$I_{OUT} = 9.6mA$			0.45	V
V_{OH}	High	$I_{OUT} = -2mA$	2.4			V
Input current[1]						
I_{IL}	Low	$V_{IN} = 0.45V$			−100	μA
I_{IH}	High	$V_{IN} = 5.5V$			40	μA
Output current[1]						
I_{OZ}	Hi-Z state	$\overline{CE}_{1,2}$ = High, $CE_{3,4}$ = Low, $V_{OUT} = 5.5V$,			40	μA
		$\overline{CE}_{1,2}$ = High, $CE_{3,4}$ = Low, $V_{OUT} = 0.5V$			−40	
I_{OS}	Short circuit[3]	$\overline{CE}_{1,2}$ = Low, $CE_{3,4}$ = High, $V_{OUT} = 0V$ High stored	−15		−70	mA
Supply current[7]						
I_{CC}		$V_{CC} = 5.25V$		125	175	mA
Capacitance						
		$\overline{CE}_{1,2}$ = High, $V_{CC} = 5.0V$				
C_{IN}	Input	$V_{IN} = 2.0V$		5		pF
C_{OUT}	Output	$V_{OUT} = 2.0V$		8		pF

AC ELECTRICAL CHARACTERISTICS $R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TO	FROM	N82S141			N82S141A			UNIT
				Min	Typ[5]	Max	Min	Typ[5]	Max	
Access time[4]										
t_{AA}		Output	Address			60			45	ns
t_{CE}		Output	Chip Enable			40			30	ns
Disable time[6]										
t_{CD}		Output	Chip disable			40			30	ns

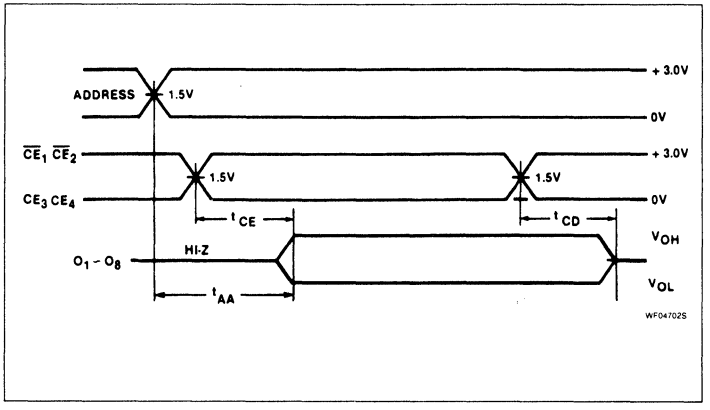
NOTES:
1. Positive current is defined as into the terminal referenced.
1. All voltages with respect to network ground.
3. Duration of the short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μs.
5. Typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
7. Measured with all inputs grounded and all outputs open.

TEST LOAD CIRCUIT



All inputs $t_r = t_f = 5ns$ (10% to 90%).

VOLTAGE WAVEFORMS



82S147
82S147A
4K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82S147 and 82S147A are field-programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The standard devices are supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

The 82S147 and 82S147A includes on-chip decoding and one Chip Enable input for ease of memory expansion, and features 3-State outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

The 82S147 and 82S147A devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

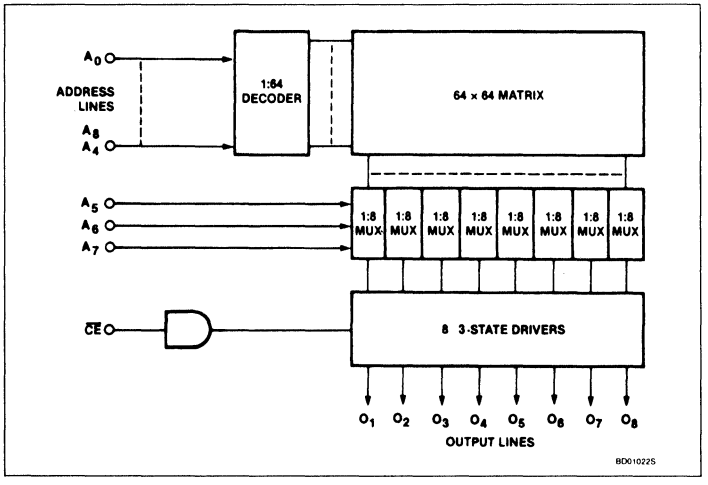
FEATURES

- **Address access time:**
  - **N82S147: 60ns max**
  - **N82S147A: 45ns max**
- **Power dissipation: 625mW typ**
- **Input loading: −100μA max**
- **One Chip Enable input**
- **On-chip address decoding**
- **No separate fusing pins**
- **Fully TTL compatible**
- **Outputs: 3-State**
- **Unprogrammed outputs are Low level**

APPLICATIONS

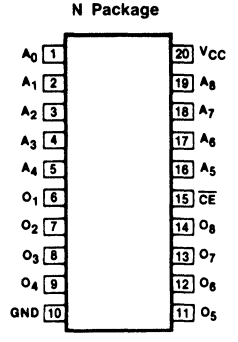
- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

BLOCK DIAGRAM

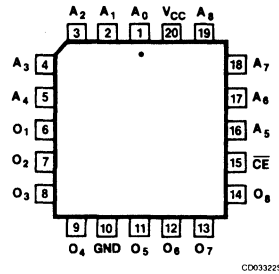


PIN CONFIGURATIONS

N Package



A Package



ORDERING INFORMATION

PACKAGES	ORDER CODE
20-pin Plastic DIP 300mil-wide	N82S147 N • N82S147A N
20-pin Plastic Leaded Chip Carrier 300mil-square	N82S147 A • N82S147A A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Power supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-state	+5.5	V_{DC}
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temperature range	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

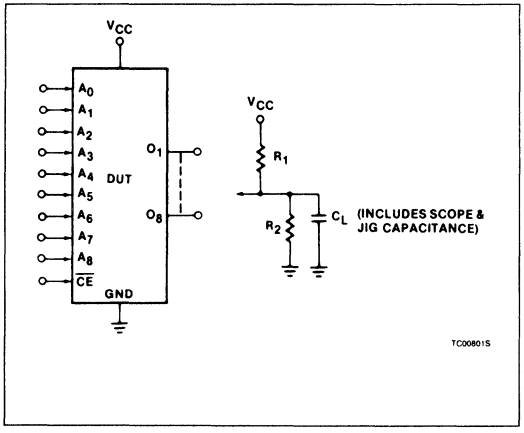
SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage						
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			V
V_{IC}	Clamp	$I_{IN} = -12mA$		−0.8	−1.2	V
Output voltage						
		$\overline{CE}$ = Low				
V_{OL}	Low	$I_{OUT} = 9.6mA$			0.45	V
V_{OH}	High	$I_{OUT} = -2mA$	2.4			V
Input current						
I_{IL}	Low	$V_{IN} = 0.45V$			−100	μA
I_{IH}	High	$V_{IN} = 5.5V$			40	μA
Output current						
I_{OZ}	Hi-Z State	$\overline{CE}$ = High, $V_{OUT} = 5.5V$			40	μA
		$\overline{CE}$ = High, $V_{OUT} = 0.5V$			−40	
I_{OS}	Short circuit[3]	$\overline{CE}$ = Low, $V_{OUT} = 0V$	−15		−70	mA
Supply current[7]						
I_{CC}		$V_{CC} = 5.25V$		125	155	mA
Capacitance						
		$\overline{CE}$ = High, $V_{CC} = 5.0V$				
C_{IN}	Input	$V_{IN} = 2.0V$		5		pF
C_{OUT}	Output	$V_{OUT} = 2.0V$		8		pF

AC ELECTRICAL CHARACTERISTICS $R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

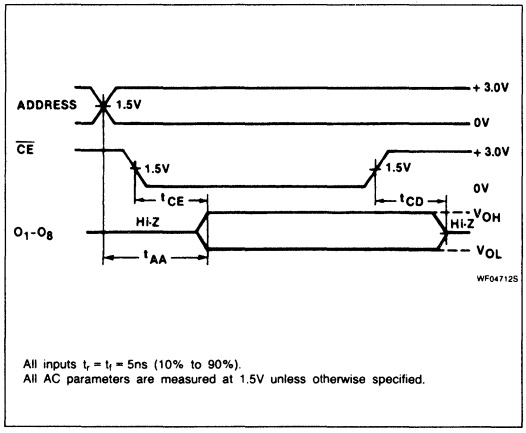
SYMBOL	PARAMETER	TO	FROM	N82S147			N82S147A			UNIT
				Min	Typ[5]	Max	Min	Typ[5]	Max	
Access time[4]										
t_{AA}		Output	Address		45	60		40	45	ns
t_{CE}		Output	Chip Enable		20	35		20	30	ns
Disable time[6]										
t_{CD}		Output	Chip Disable		20	35		20	30	ns

NOTES:
1. All voltage values are with respect to network ground terminal.
2. Positive current is defined as into the terminal referenced.
3. Duration of the short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μs.
5. Typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
7. Measured with all inputs grounded and all outputs open.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORMS



All inputs $t_r = t_f = 5ns$ (10% to 90%).
All AC parameters are measured at 1.5V unless otherwise specified.

82S147B
4K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82S147B is field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The standard devices are supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

The 82S147B includes on-chip decoding and one Chip Enable input for ease of memory expansion, and features 3-State outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

The 82S147B device is also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

FEATURES

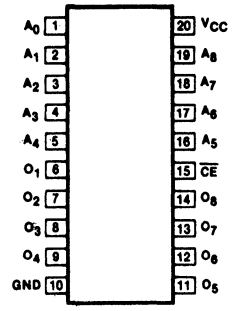
- **Address access time: 25ns max**
- **Power dissipation: 625mW typ**
- **Input loading: −100μA max**
- **One Chip Enable input**
- **On-chip address decoding**
- **No separate fusing pins**
- **Fully TTL compatible**
- **Outputs: 3-State**
- **Unprogrammed outputs are Low level**

APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATIONS

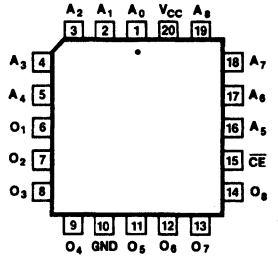
N Package



TOP VIEW

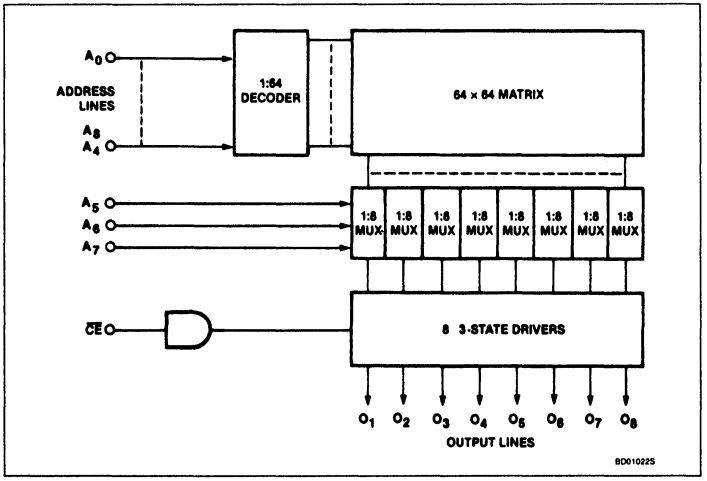
CD01253S

A Package



CD03322S

BLOCK DIAGRAM



ORDERING INFORMATION

PACKAGES	ORDER CODE
20-pin Plastic DIP 300mil-wide	N82S147B N
20-pin Plastic Leaded Chip Carrier 350mil-square	N82S147B A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-State	+5.5	V_{DC}
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temperature range	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage						
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			V
V_{IC}	Clamp	$I_{IN} = -12mA$		−0.8	−1.2	V
Output voltage						
		$\overline{CE}$ = Low				
V_{OL}	Low	$I_{OUT} = 9.6mA$			0.45	V
V_{OH}	High	$I_{OUT} = -2mA$	2.4			V
Input current						
I_{IL}	Low	$V_{IN} = 0.45V$			−100	μA
I_{IH}	High	$V_{IN} = 5.5V$			40	μA
Output current						
I_{OZ}	Hi-Z State	$\overline{CE}$ = High, $V_{OUT} = 5.5V$			40	μA
		$\overline{CE}$ = High, $V_{OUT} = 0.5V$			−40	
I_{OS}	Short circuit[3]	$\overline{CE}$ = Low, $V_{OUT} = 0V$	−15		−70	mA
Supply current[7]						
I_{CC}		$V_{CC} = 5.25V$		125	155	mA
Capacitance						
		$\overline{CE}$ = High, $V_{CC} = 5.0V$				
C_{IN}	Input	$V_{IN} = 2.0V$		5		pF
C_{OUT}	Output	$V_{OUT} = 2.0V$		8		pF

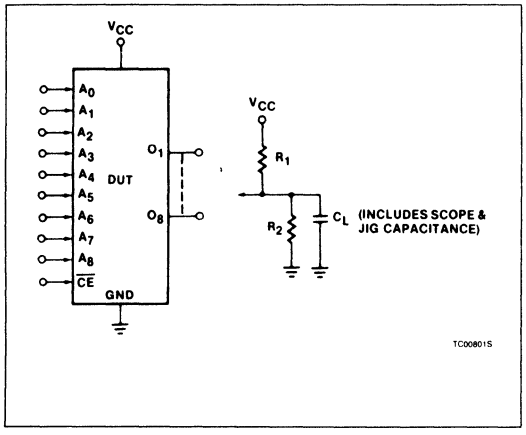
Notes on following page.

AC ELECTRICAL CHARACTERISTICS $R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

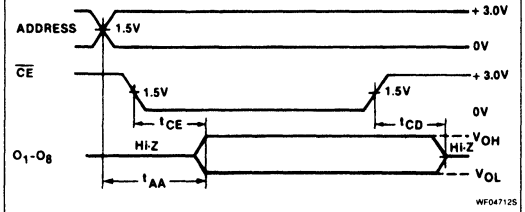
SYMBOL	PARAMETER	TO	FROM	N82S147B			UNIT
				Min	Typ[5]	Max	
Access time[4]							
t_{AA}		Output	Address			25	ns
t_{CE}		Output	Chip Enable			15	ns
Disable time[6]							
t_{CD}		Output	Chip Disable			15	ns

NOTES:
1. All voltage values are with respect to network ground terminal.
2. Positive current is defined as into the terminal referenced.
3. Duration of the short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μs.
5. Typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
7. Measured with all inputs grounded and all outputs open.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORMS



All inputs $t_r = t_f = 5ns$ (10% to 90%).
All AC parameters are measured at 1.5V unless otherwise specified.

8K-bit TTL PROM

		page
82S181	8192-bit PROM (1024 x 8) 70 ns	407
82S181A	8192-bit PROM (1024 x 8) 55 ns	407
82S181C	8192-bit PROM (1024 x 8) 35 ns	411
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82HS189	8192-bit PROM (1024 x 8) 55 ns	435
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82S181
82S181A
8K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82S181 and 82S181A are field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The 82S181 and 82S181A are supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

This device includes on-chip decoding and 4 Chip Enable inputs for ease of memory expansion. It features 3-State outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

The 82S181 and 82S181A devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

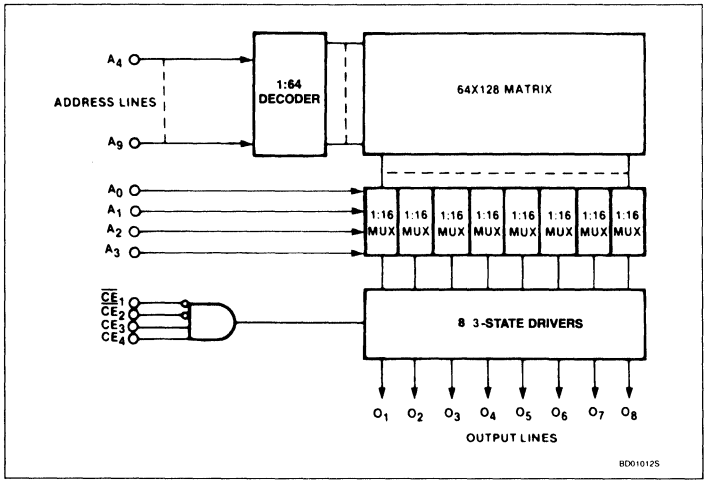
FEATURES

- **Address access time:**
  - **N82S181: 70ns max**
  - **N82S181A: 55ns max**
- **Power dissipation: 76μW/bit typ**
- **Input loading: −100μA max**
- **On-chip address decoding**
- **Four Chip Enable inputs**
- **Outputs: 3-State**
- **No separate fusing pins**
- **Unprogrammed outputs are Low level**
- **Fully TTL compatible**

APPLICATIONS

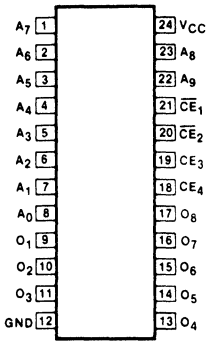
- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

BLOCK DIAGRAM



PIN CONFIGURATIONS

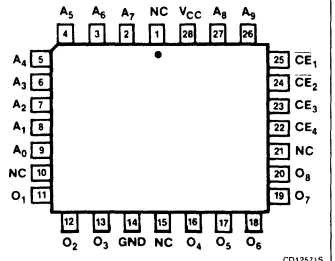
N Package



TOP VIEW

CD01244S

A Package



CD12571S

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-pin Plastic DIP 600mil-wide	N82S181 N • N82S181A N
28-pin Plastic Leaded Chip Carrier 450mil-square	N82S181 A • N82S181A A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-State	+5.5	V_{DC}
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temperature range	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C,\ 4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage[2]						
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			V
V_{IC}	Clamp	$I_{IN} = -12mA$		−0.8	−1.2	V
Output voltage[2]						
		$\overline{CE}_{1,2}$ = Low, $CE_{3,4}$ = High				
V_{OL}	Low	$I_{OUT} = 9.6mA$			0.45	V
V_{OH}	High	$I_{OUT} = -2mA$	2.4			V
Input current[1]						
I_{IL}	Low	$V_{IN} = 0.45V$			−100	μA
I_{IH}	High	$V_{IN} = 5.5V$			40	μA
Output current[1]						
I_{OZ}	Hi-Z State	$\overline{CE}_{1,2}$ = High, $CE_{3,4}$ = Low, $V_{OUT} = 5.5V$,			40	μA
		$\overline{CE}_{1,2}$ = High, $CE_{3,4}$ = Low, $V_{OUT} = 0.5V$			−40	
I_{OS}	Short circuit[3]	$\overline{CE}_{1,2}$ = Low, $CE_{3,4}$ = High, $V_{OUT} = 0V$ High stored	−15		−70	mA
Supply current[7]						
I_{CC}		$V_{CC} = 5.25V$		125	175	mA
Capacitance						
		$\overline{CE}_{1,2}$ = High, $V_{CC} = 5.0V$				
C_{IN}	Input	$V_{IN} = 2.0V$		5		pF
C_{OUT}	Output	$V_{OUT} = 2.0V$		8		pF

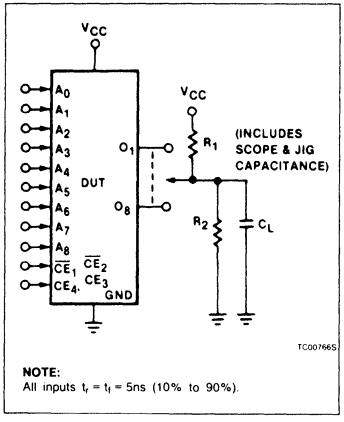
Notes on following page.

AC ELECTRICAL CHARACTERISTICS $R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TO	FROM	N82S181			N82S181A			UNIT
				Min	Typ[5]	Max	Min	Typ[5]	Max	
Access time[4]										
t_{AA}		Output	Address		50	70		45	55	ns
t_{CE}		Output	Chip Enable		25	40		25	40	ns
Disable time[6]										
t_{CD}		Output	Chip Disable		25	40		25	40	ns

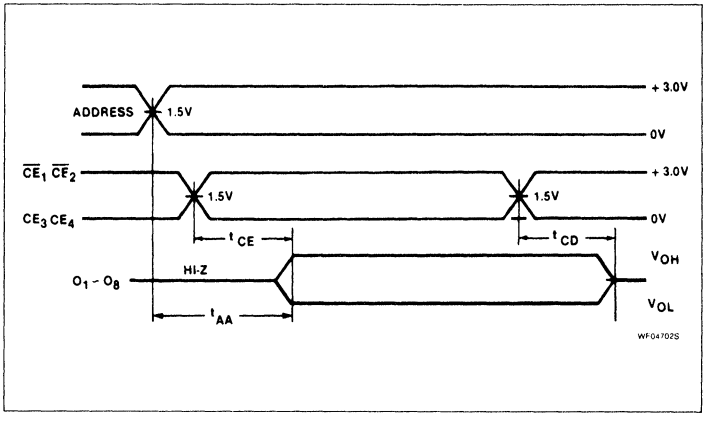
NOTES:
1. Positive current is defined as into the terminal referenced.
1. All voltages with respect to network ground.
3. Duration of the short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μs.
5. Typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
7. Measured with all inputs grounded and all outputs open.

TEST LOAD CIRCUIT



NOTE:
All inputs $t_r = t_f = 5ns$ (10% to 90%).

VOLTAGE WAVEFORMS



82S181C
8K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82S181C is field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The 82S181C is supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

This device includes on-chip decoding and 4 Chip Enable inputs for ease of memory expansion. It features 3-State outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

This device is also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

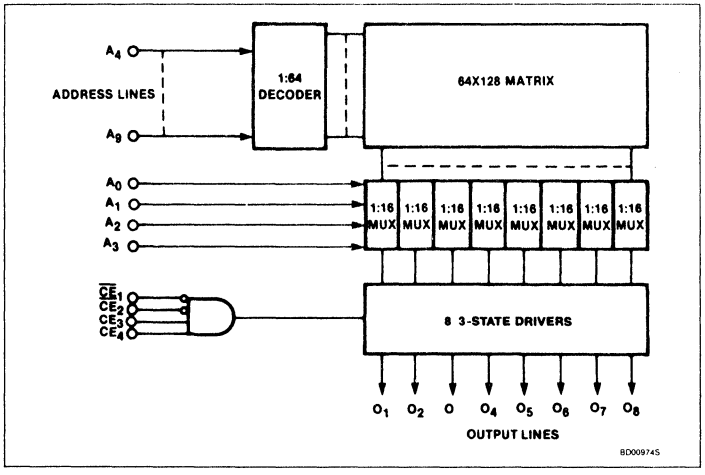
FEATURES

- **Address access time: 35ns max**
- **Power dissipation: 76μW/bit typ**
- **Input loading: −100μA max**
- **On-chip address decoding**
- **Four Chip Enable inputs**
- **Outputs: 3-State**
- **No separate fusing pins**
- **Unprogrammed outputs are Low level**
- **Fully TTL compatible**

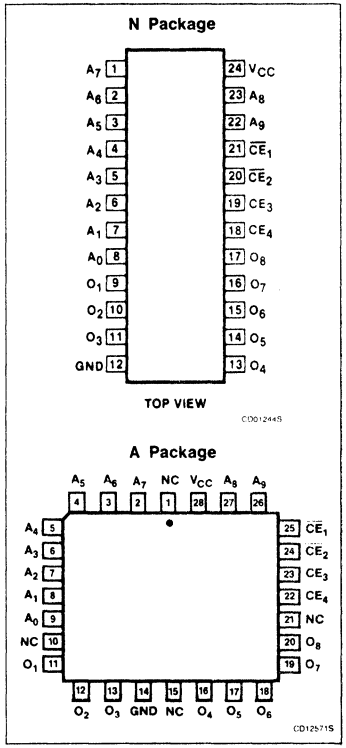
APPLICATIONS

- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

BLOCK DIAGRAM



PIN CONFIGURATIONS



ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-pin Plastic DIP 600mil-wide	N82S181C N
24-pin Plastic DIP 300mil-wide	N82S181C N3
28-pin Plastic Leaded Chip Carrier 450mil-square	N82S181C A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-State	+5.5	V_{DC}
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temperature range	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C,\ 4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS[1, 2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage[2]						
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			V
V_{IC}	Clamp	$I_{IN} = -12mA$		−0.8	−1.2	V
Output voltage[2]						
		$\overline{CE}_{1,2}$ = Low, $CE_{3,4}$ = High				
V_{OL}	Low	$I_{OUT} = 9.6mA$			0.45	V
V_{OH}	High	$I_{OUT} = -2mA$	2.4			V
Input current[1]						
I_{IL}	Low	$V_{IN} = 0.45V$			−100	μA
I_{IH}	High	$V_{IN} = 5.5V$			40	μA
Output current[1]						
I_{OZ}	Hi-Z State	$\overline{CE}_{1,2}$ = High, $CE_{3,4}$ = Low, $V_{OUT} = 5.5V$			40	μA
		$\overline{CE}_{1,2}$ = High, $CE_{3,4}$ = Low, $V_{OUT} = 0.5V$			-40	
I_{OS}	Short circuit	$\overline{CE}_{1,2}$ = Low, $CE_{3,4}$ = High, $V_{OUT} = 0V$ High stored	−15		−70	mA
Supply current[7]						
I_{CC}		$V_{CC} = 5.25V$		125	175	mA
Capacitance						
		$\overline{CE}_{1,2}$ = High, $V_{CC} = 5.0V$				
C_{IN}	Input	$V_{IN} = 2.0V$		5		pF
C_{OUT}	Output	$V_{OUT} = 2.0V$		8		pF

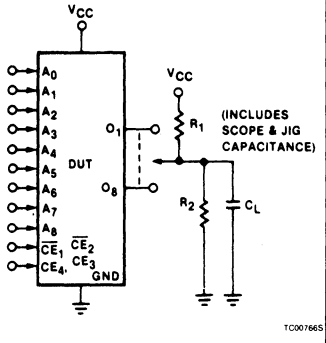
Notes on following page.

AC ELECTRICAL CHARACTERISTICS $R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[5]	Max	
Access time[4]							
t_{AA}		Output	Address		25	35	ns
t_{CE}		Output	Chip Enable		15	20	ns
Disable time[6]							
t_{CD}		Output	Chip Disable		15	20	ns

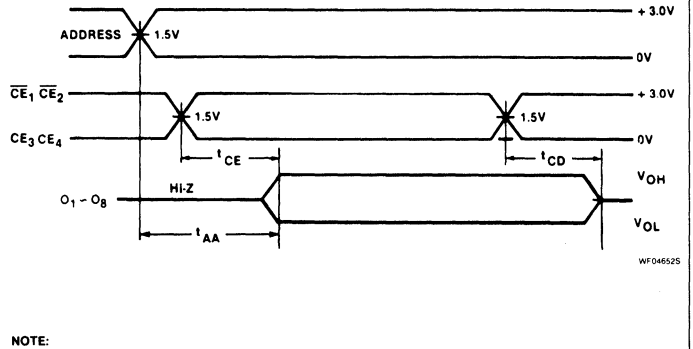
NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μs.
5. Typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
7. Measured with all inputs grounded and all outputs open.

TEST LOAD CIRCUIT



NOTE:
All inputs: $t_r = t_f = 5ns$ (10% to 90%).

VOLTAGE WAVEFORMS



NOTE:
All AC parameters are measured at 1.5V unless otherwise specified.

82S183
8K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82S183 is field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The standard 82S183 is supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

This device includes on-chip decoding and 3 Chip Enable inputs for ease of memory expansion. It features 3-State outputs for optimization of word expansion in bused organizations.

In the Transparent Read mode, stored data is addressed by applying a binary code to the address inputs while holding Strobe High. In this mode the output drivers are controlled solely by $\overline{CE}_1$, $\overline{CE}_2$, and CE_3 lines.

A D-type latch is used to enable the 3-State output drivers. In the Latched Read mode, outputs are held in their previous state (High, Low, or Hi-Z) as long as Strobe is Low, regardless of the state of Address or Chip Enable. A positive Strobe transition causes data from the applied address to reach the outputs if the chip is enabled, and causes outputs to go to the Hi-Z state if the chip is disabled.

A negative Strobe transition causes outputs to be locked into their last Read Data condition if the chip was enabled, or causes outputs to be locked into the Hi-Z condition if the chip was disabled.

Ordering information can be found on the following page.

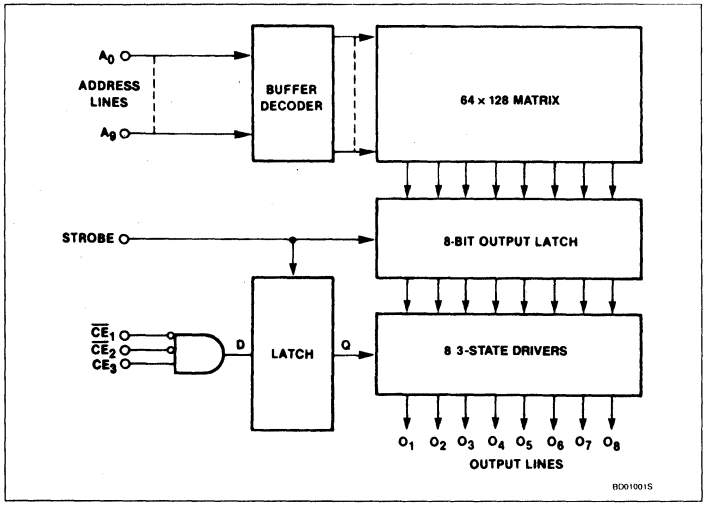
FEATURES

- **Address access time: 60ns max**
- **Power dissipation: 80μW/bit typ**
- **Input loading: −100μA max**
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are Low level**
- **Fully TTL compatible**
- **Three Chip Enable inputs**
- **Outputs: 3-State**

APPLICATIONS

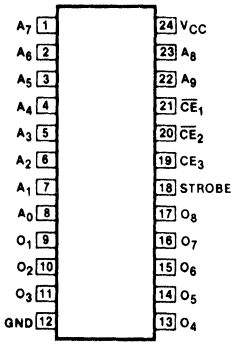
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Code conversion**

BLOCK DIAGRAM



PIN CONFIGURATIONS

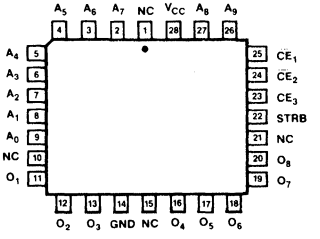
N Package



TOP VIEW

CD01231S

A Package



CD12561S

8K-Bit TTL Bipolar PROM (1024 × 8) — 82S183

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-pin Plastic DIP 600mil-wide	N82S183 N
28-pin Plastic Leaded Chip Carrier 450mil-square	N82S183 A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temperature range	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS[4]	LIMITS			UNIT
			Min	Typ[6]	Max	
Input voltage						
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			V
V_{IC}	Clamp	$I_{IN} = -12mA$		−0.8	−1.2	V
Output voltage						
		$\overline{CE}_{1,2}$ = Low, CE_3 = Strobe = High				
V_{OL}	Low	$I_{OUT} = 9.6mA$			0.45	V
V_{OH}	High	$I_{OUT} = -2.0mA$	2.4			V
Input current[4]						
I_{IL}	Low	$V_{IN} = 0.45V$			−100	μA
I_{IH}	High	$V_{IN} = 5.5V$	25		25	μA
Output current[4]						
I_{OZ}	Hi-Z State	$\overline{CE}$ = High or CE = Low, $V_{OUT} = 5.5V$			40	μA
		$\overline{CE}$ = High or CE = Low, $V_{OUT} = 0.5V$			−40	
I_{OS}	Short circuit[1]	$\overline{CE}$ = Low, CE = High, V_{OUT} = 0V, High stored	−15		−70	mA
Supply current[9]						
I_{CC}		$V_{CC} = 5.25V$		130	175	mA
Capacitance						
		$\overline{CE}_{1,2}$ = High or CE_3 = Low, $V_{CC} = 5.0$				
C_{IN}	Input	$V_{IN} = 2.0V$		5		pF
C_{OUT}	Output	$V_{OUT} = 2.0V$		8		pF

Notes on following page.

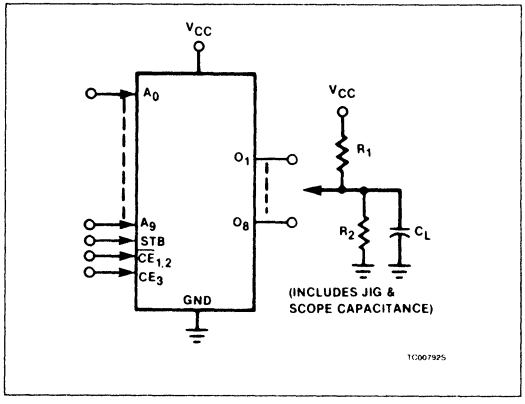
AC ELECTRICAL CHARACTERISTICS $R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TO	FROM	TEST CONDITIONS	MIN	TYP[6]	MAX	UNIT
Access time[2]								
t_{AA} t_{CE}		Output Output	Address Chip Enable	Latched or transparent read		45 25	60 40	ns ns
Disable time[2,7]								
t_{CD}		Output	Chip Disable	Latched or transparent read		25	40	ns
Setup and hold time[3]								
t_{CDS} t_{CDH}	Setup time Hold time	Output	Chip Enable	Latched read only	40 10			ns
t_{ADH}	Hold time	Output	Address		0			ns
Pulse width[3]								
t_{SW}	Strobe			Latched read only	30	15		ns
Latch time[3]								
t_{SL}	Strobe			Latched read only	60	35		ns
Delatch time[3,7]								
t_{DL}	Strobe			Latched read only			30	ns

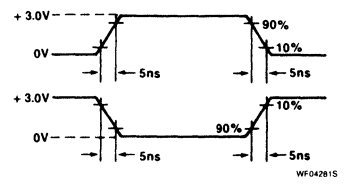
NOTES:

1. No more than one output should be grounded at the same time and Strobe should be disabled. Strobe is in High state.
2. If the Strobe is High, the device functions in a manner identical to conventional bipolar ROMs. The timing diagram shows valid data will appear T_{AA} nanoseconds after the address has changed the T_{CE} nanoseconds after the output circuit is enabled. T_{CD} is the time required to disable the output and switch it to an off or High impedance state after it has been enabled.
3. In Latched Read Mode data from any selected address will be held on the output when Strobe is lowered. Only when Strobe is raised will new location data be transfered and chip enable conditions be stored. The new data will appear on the output if the chip enable conditions enable the outputs.
4. Positive current is defined as into the terminal referenced.
5. Areas shown by crosshatch are latched data from previous address.
6. Typical values are $V_{CC} = 5V$, $T_A = +25°C$.
7. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.

TEST LOAD CIRCUIT



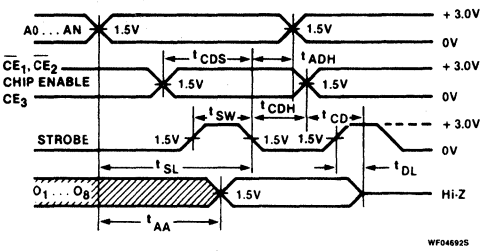
VOLTAGE WAVEFORMS



Input Pulses

TIMING DIAGRAMS

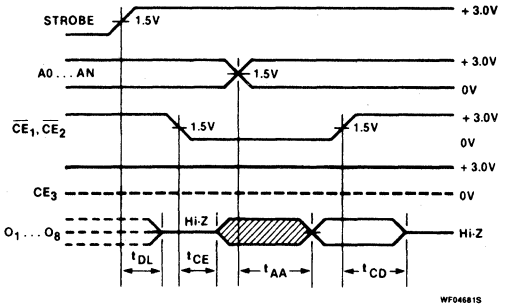
Transparent Read



NOTE:
All AC parameters are measured at 1.5V unless otherwise specified.

Output Latches Not Used

Latched Read



Output Latches Used

82S185
8K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82S185 is field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The standard 82S185 is supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

This device includes on-chip decoding and 1 Chip Enable input for memory expansion. It features 3-State outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

The 82S185 devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

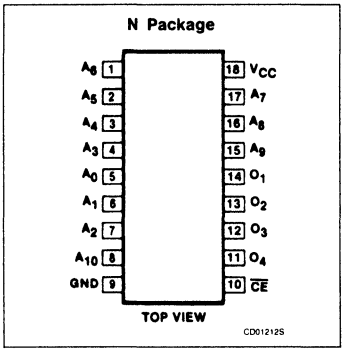
FEATURES

- **Low power dissipation: 50μW/bit typ**
- **Address access time: 100ns max**
- **Input loading: -100μA max**
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are Low level**
- **Fully TTL compatible**
- **One Chip Enable input**
- **Outputs: 3-State**

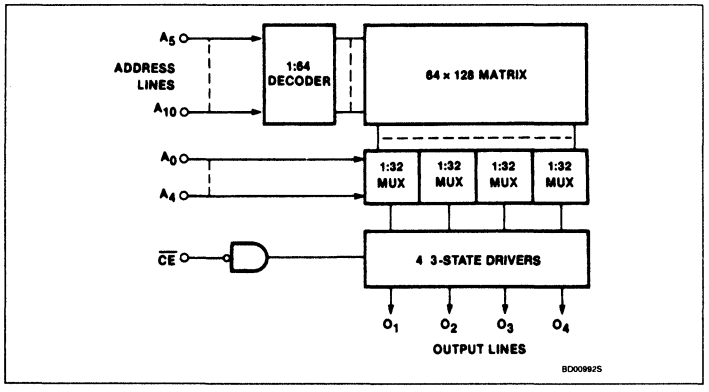
APPLICATIONS

- **Sequential controllers**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	ORDER CODE
18-pin Plastic DIP 300mil-wide	N82S185 N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-State	+5.5	V_{DC}
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temperature range	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage[1]						
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			V
V_{IC}	Clamp	$I_{IN} = -12mA$		−0.8	−1.2	V
Output voltage[1]						
		$\overline{CE}$ = Low				
V_{OL}	Low	$I_{OUT} = 16mA$			0.45	V
V_{OH}	High	$I_{OUT} = -2mA$	2.4			V
Input current[2]						
I_{IL}	Low	$V_{IN} = 0.45V$			−100	μA
I_{IH}	High	$V_{IN} = 5.5V$			40	μA
Output current						
I_{OZ}	Hi-Z State	$\overline{CE}$ = High, $V_{OUT} = 0.5V$			−40	μA
		$\overline{CE}$ = High, $V_{OUT} = 5.5V$			40	
I_{OS}	Short circuit[3]	$\overline{CE}$ = Low, V_{OUT} = 0V, High stored	−15		−70	mA
Supply current[7]						
I_{CC}		$V_{CC} = 5.25V$		90	120	mA
Capacitance						
		$\overline{CE}$ = High, $V_{CC} = 5.0V$				
C_{IN}	Input	$V_{IN} = 2.0V$		5		pF
C_{OUT}	Output	$V_{OUT} = 2.0V$		8		pF

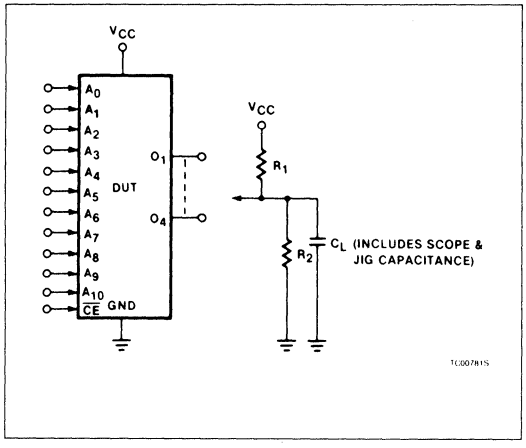
Notes on following page.

AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

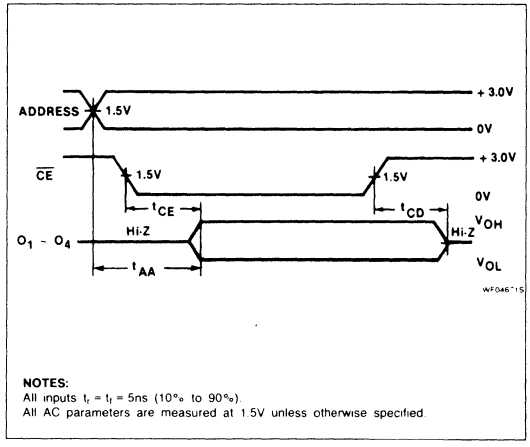
SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[5]	Max	
Access time[4]							
t_{AA}		Output	Address		70	100	ns
t_{CE}		Output	Chip Enable		30	40	ns
Disable time[6]							
t_{CD}		Output	Chip Disable		30	40	ns

NOTES:
1. All voltage values are with respect to network ground terminal.
2. Positive current is defined as into the terminal referenced.
3. Duration of the short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μs.
5. All typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
7. Measured with all inputs grounded and all outputs open.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORMS



NOTES:
All inputs $t_r = t_f = 5ns$ (10% to 90%).
All AC parameters are measured at 1.5V unless otherwise specified.

82S185A
8K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82S185A is field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The devices are supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

This device includes on-chip decoding and 1 Chip Enable input for memory expansion. It features 3-State outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

The 82S185A device is also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

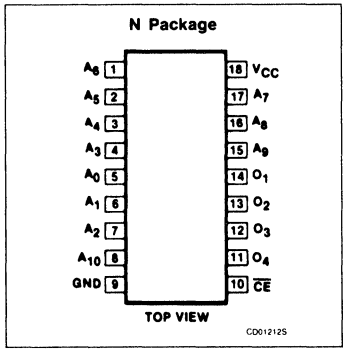
FEATURES

- **Low power dissipation: 70μW/bit typ**
- **Address access time: 50ns max**
- **Input loading: -100μA max**
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are Low level**
- **Fully TTL compatible**
- **One Chip Enable input**
- **Outputs: 3-State**

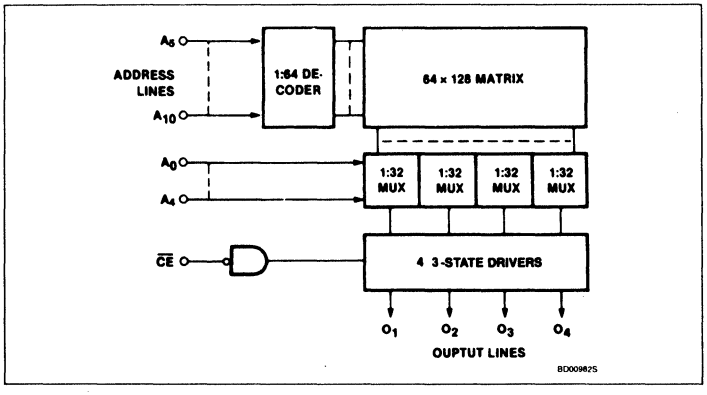
APPLICATIONS

- **Microprogramming**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATION



BLOCK DIAGRAM



8K-Bit TTL Bipolar PROM (2048 × 4) 82S185A

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
18-pin Plastic DIP 300mil-wide	N82S185A N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-State	+5.5	V_{DC}
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temperature range	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C,\ 4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage						
V_{IL}	Low	$V_{CC} = 4.75V$			0.8	V
V_{IH}	High	$V_{CC} = 5.25V$	2.0			V
V_{IC}	Clamp	$I_{IN} = -12mA$		−0.8	−1.2	V
Output voltage						
		$\overline{CE}$ = Low				
V_{OL}	Low	$I_{OUT} = 16mA$			0.45	V
V_{OH}	High	$I_{OUT} = -2mA$	2.4			V
Input current						
I_{IL}	Low	$V_{IN} = 0.45V$			−100	μA
I_{IH}	High	$V_{IN} = 5.5V$			40	μA
Output current						
I_{OZ}	Hi-Z State	$\overline{CE}$ = High, $V_{OUT} = 0.5V$			−40	μA
		$\overline{CE}$ = High, $V_{OUT} = 5.5V$			40	
I_{OS}	Short circuit[3]	$\overline{CE}$ = Low, $V_{OUT} = 0V$ High stored	−15		−70	mA
Supply current[7]						
I_{CC}		$V_{CC} = 5.25V$		110	155	mA
Capacitance						
		$\overline{CE}$ = High, $V_{CC} = 5.0V$				
C_{IN}	Input	$V_{IN} = 2.0V$		5		pF
C_{OUT}	Output	$V_{OUT} = 2.0V$		8		pF

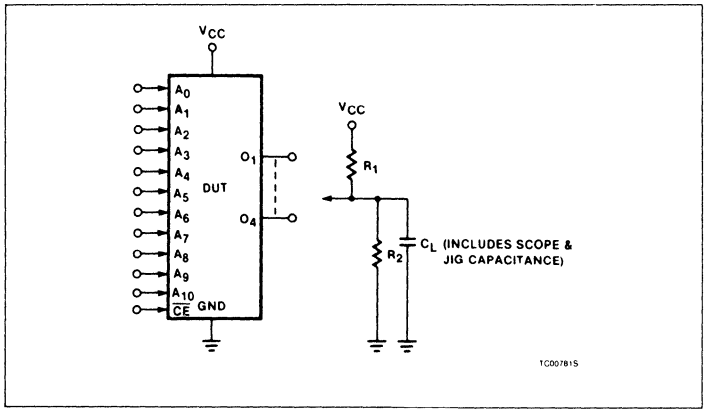
Notes on following page.

AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

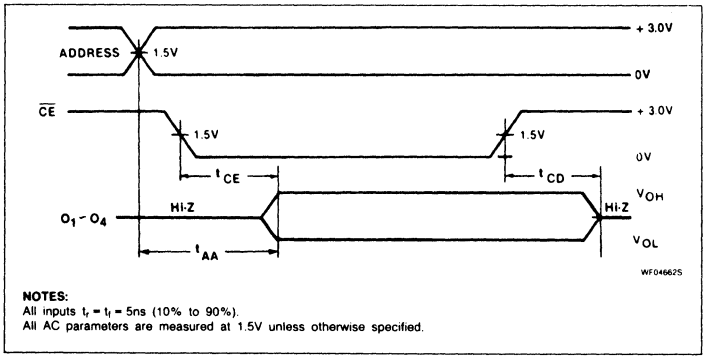
SYMBOL	PARAMETER	TO	FROM	N82S185A			UNIT
				Min	Typ[5]	Max	
Access time[4]							
t_{AA}		Output	Address		40	50	ns
t_{CE}		Output	Chip Enable		20	30	ns
Disable time[6]							
t_{CD}		Output	Chip Disable		20	30	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μs.
5. Typical values are at $V_C = 5V$, $T_A = +25°C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
7. Measured with all inputs grounded and all outputs open.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORMS



NOTES:
All inputs $t_r = t_f = 5ns$ (10% to 90%).
All AC parameters are measured at 1.5V unless otherwise specified.

82S185B
8K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82S185B is field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The devices are supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

This device includes on-chip decoding and 1 Chip Enable input for memory expansion. It features 3-State outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

The 82S185B device is also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

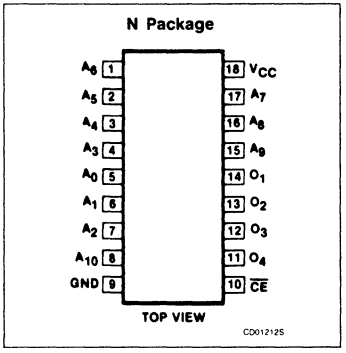
FEATURES

- **Address access time: 35ns max**
- **Low power dissipation: 70μW/bit typ**
- **Input loading: −100μA max**
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are Low level**
- **Fully TTL compatible**
- **One Chip Enable input**
- **Outputs: 3-State**

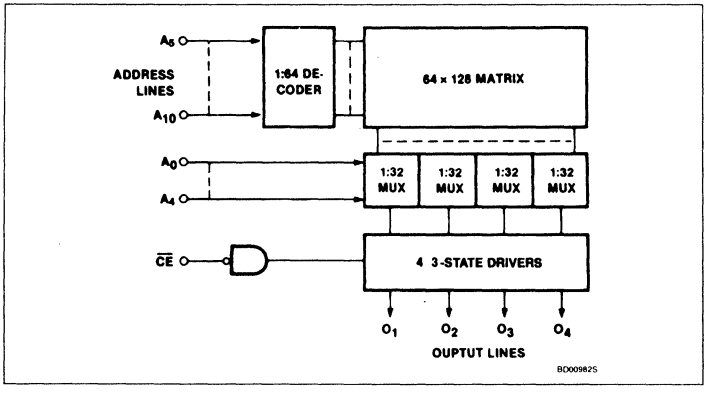
APPLICATIONS

- **Microprogramming**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATION



BLOCK DIAGRAM



8K-Bit TTL Bipolar PROM (2048 × 4) 82S185B

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
18-pin Plastic DIP 300mil-wide	N82S185B N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-State	+5.5	V_{DC}
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temperature range	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage						
V_{IL}	Low	V_{CC} = 4.75V			0.8	V
V_{IH}	High	V_{CC} = 5.25V	2.0			V
V_{IC}	Clamp	I_{IN} = −12mA		−0.8	−1.2	V
Output voltage						
		$\overline{CE}$ = Low				
V_{OL}	Low	I_{OUT} = 16mA			0.45	V
V_{OH}	High	I_{OUT} = −2mA	2.4			V
Input current						
I_{IL}	Low	V_{IN} = 0.45V			−100	μA
I_{IH}	High	V_{IN} = 5.5V			40	μA
Output current						
I_{OZ}	Hi-Z State	$\overline{CE}$ = High, V_{OUT} = 0.5V			−40	μA
		$\overline{CE}$ = High, V_{OUT} = 5.5V			40	
I_{OS}	Short circuit[3]	$\overline{CE}$ = Low, V_{OUT} = 0V High stored	−15		−70	mA
Supply current[7]						
I_{CC}		V_{CC} = 5.25V		110	155	mA
Capacitance						
		$\overline{CE}$ = High, V_{CC} = 5.0V				
C_{IN}	Input	V_{IN} = 2.0V		5		pF
C_{OUT}	Output	V_{OUT} = 2.0V		8		pF

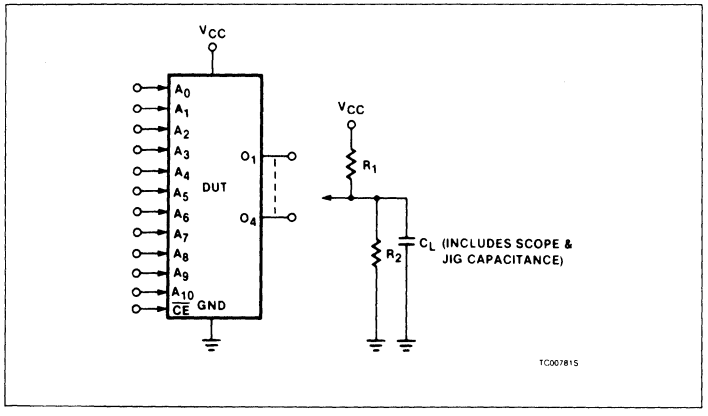
Notes on following page.

AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

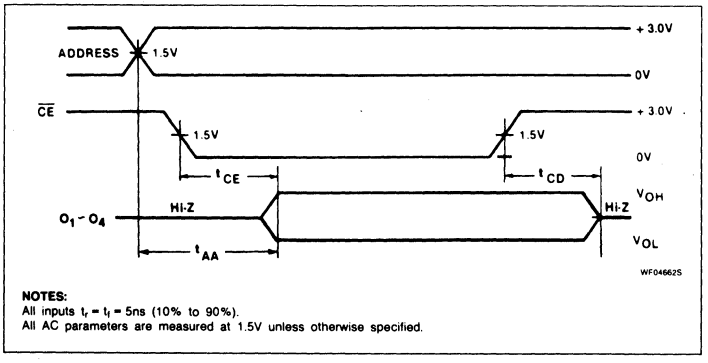
SYMBOL	PARAMETER	TO	FROM	N82S185C			UNIT
				Min	Typ[5]	Max	
Access time[4]							
t_{AA}		Output	Address		20	35	ns
t_{CE}		Output	Chip Enable		12	20	ns
Disable time[6]							
t_{CD}		Output	Chip Disable		12	20	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μs.
5. Typical values are at $V_C = 5V$, $T_A = +25°C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
7. Measured with all inputs grounded and all outputs open.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORMS



NOTES:
All inputs $t_r = t_f = 5ns$ (10% to 90%).
All AC parameters are measured at 1.5V unless otherwise specified.

82HS187
82HS187A
8K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82HS187 is a programmable read only memory containing D-type, master-slave data registers. The 82HS187 contains 1024 words of 8 bits each. The unprogrammed state is with all outputs at a High level and can be selectively programmed to a Low level by following the Signetics Generic II programming method. The output structure is 3-State for ease in connection to bus-organized systems. The combination of on-chip registers and 3-State outputs will substantially reduce cost and size of pipelined microprogrammed systems and other designs where accessed PROM data is temporarily stored in a register.

All outputs will go into the third state or Hi-Z condition whenever the Asynchronous Chip Enable ($\overline{G}$) is High. The outputs are enabled when ($\overline{GS}$) is brought Low before the rising edge of the clock and ($\overline{G}$) is held Low. The ($\overline{GS}$) flip-flop is designed to power-up in the third state or Hi-Z condition with the application of V_{CC}.

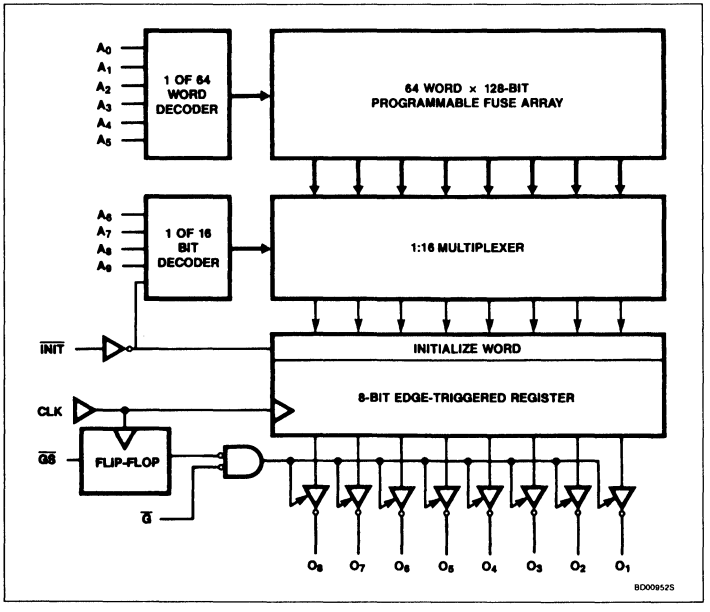
The 82HS187 also features an initialize function, $\overline{INIT}$. The initialize function provides the user with an extra word of programmable memory which is accessed with single-pin control by applying a Low on $\overline{INIT}$. The initialize function is asynchronous and is loaded into the Output Register and will appear at the outputs upon an application of a Low on $\overline{INIT}$ if the outputs are enabled, and will control the state of the data registers independent of all other inputs. The unprogrammed state of $\overline{INIT}$ is all ones.

Data is read from the PROM by first applying an address to inputs A_0 to A_9. During the setup time the output of the array is loaded into the master flip-flop of the data register. During the rising edge (Low-to-High transition) of the clock, the data is transferred to the slave of the flip-flop and will appear on the output if the output is enabled. Following the rising edge clock transition, the Addresses and Synchronous Chip Enable can be removed and the output data will remain stable.

FEATURES

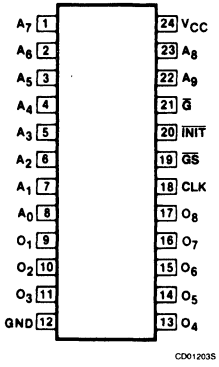
- **On-chip edge-triggered registers**
- **Programmable register with Asynchronous initialize function**
- **24-pin 300mil-wide DIP package**
- **Read cycle "Address setup plus clock to output delay"**
  - **N82HS187: 55ns max**
  - **N82HS187A: 45ns max**
- **Outputs: 3-State**
- **Unprogrammed outputs are High level**
- **Synchronous and Asynchronous Enables for word expansion**

BLOCK DIAGRAM

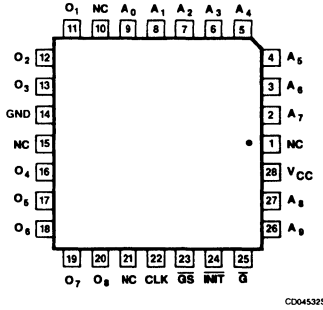


PIN CONFIGURATIONS

N Package



A Package



ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-pin Plastic DIP 300mil-wide	N82HS187 N • N82HS187A N
28-pin Plastic Leaded Chip Carrier 450mil-square	N82HS187 A • N82HS187A A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-State	+5.5	V_{DC}
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temperatue range	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage[2]						
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			V
V_{IC}	Clamp	$I_{IN} = -18mA$		−0.8	−1.2	V
Output voltage[2]						
		$\overline{G}$, $\overline{GS}$ = Low				
V_{OL}	Low	$I_{OUT} = 16mA$			0.5	V
V_{OH}	High	$I_{OUT} = -2mA$	2.4			V
Input current[1]						
I_{IL}	Low	$V_{IN} = 0.45V$			−250	μA
I_{IH}	High	$V_{IN} = 5.25V$			40	μA
Output current[1]						
I_{OZ}	Hi-Z State	$\overline{G}$ = High, $V_{OUT} = 5.25V$			40	μA
		$\overline{G}$ = High, $V_{OUT} = 0.5V$			−40	
I_{OS}	Short circuit[3]	$\overline{G}$, $\overline{GS}$ = Low, $V_{OUT} = 0V$ High stored	−15		−70	mA
Supply current[7]						
I_{CC}		$V_{CC} = 5.25V$		125	175	mA
Capacitance						
		$\overline{G}$ = High, $V_{CC} = 5.0V$				
C_{IN}	Input	$V_{IN} = 2.0V$		5		pF
C_{OUT}	Output	$V_{OUT} = 2.0V$		8		pF

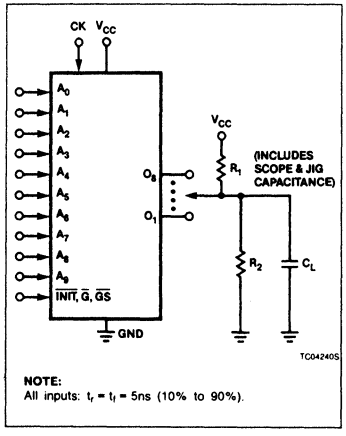
Notes on following page.

AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER[4]	TO	FROM	N82HS187			N82HS187A			UNIT
				Min	Typ[5]	Max	Min	Typ	Max	
t_{CSA} t_{CHA}	Setup Hold	CLK	Address	35 0			30 0			ns
t_{OC}	Delay	Output	CLK			20	0		15	ns
t_{WC}	Width	H & L	CLK	20	10		15	10		ns
t_{CSGS} t_{CHGS}	Setup Hold	CLK	$\overline{GS}$	15 5			10 5			ns
t_{OIN}	Delay	Output	$\overline{INIT}$		12	30			25	ns
t_{CIN}	Recovery	CLK	$\overline{INIT}$	20	9		15			ns
t_{WIN}	Width		$\overline{INIT}$	25			20			ns
t_{OG}	Delay	Output	$\overline{G}$		11	25			20	ns
t_{OZC}[6]	Delay	Output	CLK		16	25			20	ns
t_{OZG}[6]	Delay	Output	$\overline{G}$		14	25			20	ns

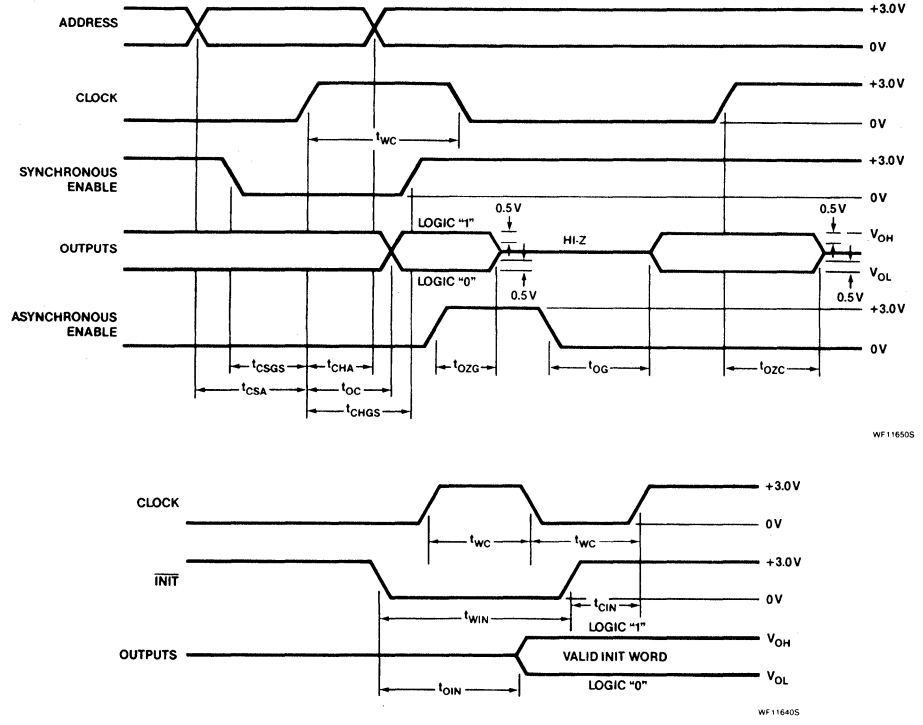
NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μs.
5. Typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
7. Measured with all inputs grounded and all outputs open.

TEST LOAD CIRCUIT



NOTE:
All inputs: $t_r = t_f = 5ns$ (10% to 90%).

VOLTAGE WAVEFORMS



NOTE:
All AC parameters are measured at 1.5V unless otherwise specified.

82HS189
82HS189A
8K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82HS189 is a programmable read only memory containing D-type, master-slave data registers. The 82HS189 contains 1024 words of 8 bits each. The unprogrammed state is with all outputs at a High level and can be selectively programmed to a Low level by following the Signetics Generic II programming method. The output structure is 3-State for ease in connection to bus-organized systems. The combination of on-chip registers and 3-State outputs will substantially reduce cost and size of pipelined microprogrammed systems and other designs where accessed PROM data is temporarily stored in a register.

All outputs will go into the third state or Hi-Z condition if the Asynchronous Chip Enable ($\overline{G}$) is held High. The outputs are enabled when ($\overline{GS}$) is brought Low before the rising edge of the clock and ($\overline{G}$) is held Low. The ($\overline{GS}$) flip-flop is designed to power-up in the third state or Hi-Z condition with the application of V_{CC}.

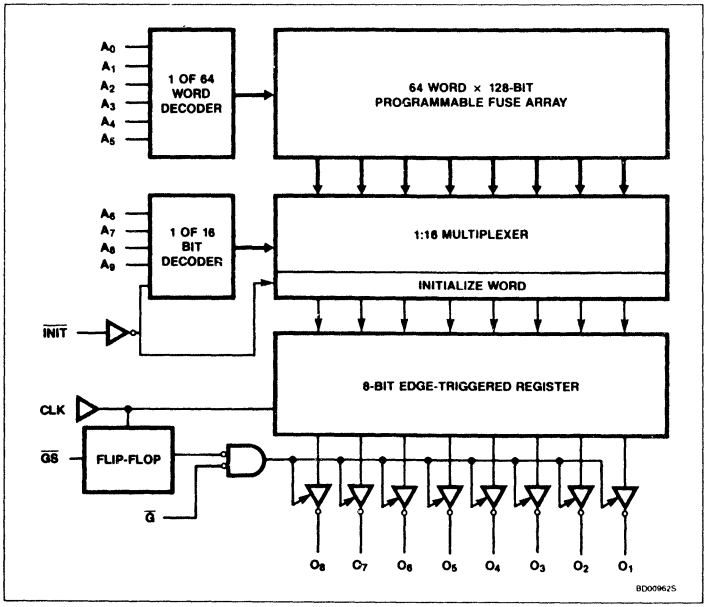
The 82HS189 also features an initialize function, $\overline{INIT}$. The initialize function provides the user with an extra word of programmable memory which is accessed with single-pin control by applying a Low on $\overline{INIT}$. The initialize function is synchronous and is loaded into the Output Register on the next rising edge of the clock. The unprogrammed state of $\overline{INIT}$ is all ones.

Data is read from the PROM by first applying an address to inputs A_0 to A_9. During the setup time the output of the array is loaded into the master flip-flop of the data register. During the rising edge (Low-to-High transition) of the clock, the data is transferred to the slave of the flip-flop and will appear on the output if the output is enabled. Following the rising edge clock transition, the Addresses and Synchronous Chip Enable can be removed and the output data will remain stable.

FEATURES

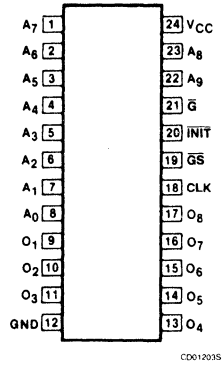
- **On-chip edge-triggered registers**
- **Asynchronous and Synchronous Enables for word expansion**
- **Programmable register with synchronous initialize function**
- **24-pin 300mil-wide package**
- **Read cycle "Address setup plus clock to output delay"**
  - **N82HS189: 55ns max**
  - **N82HS189A: 45ns max**
- **Unprogrammed outputs are High level**
- **Outputs: 3-State**

BLOCK DIAGRAM

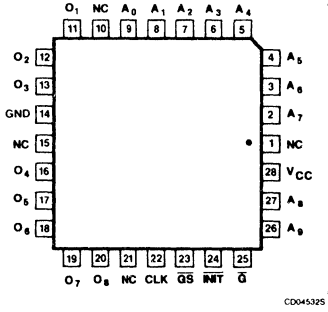


PIN CONFIGURATIONS

N Package



A Package



ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-pin Plastic DIP 300mil-wide	N82HS189 N • N82HS189A N
28-pin Plastic Leaded Chip Carrier 450mil-square	N82HS189 A • N82HS189A A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-State	+5.5	V_{DC}
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temperature range	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C,\ 4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage[2]						
V_{IL}	Low				0.8	
V_{IH}	High		2.0			V
V_{IC}	Clamp	$I_{IN} = -18mA$		−0.8	−1.2	V
Output voltage[2]						
		$\overline{G}$, $\overline{GS}$ = Low				
V_{OL}	Low	$I_{OUT} = 16mA$			0.5	V
V_{OH}	High	$I_{OUT} = -2mA$	2.4			V
Input current[1]						
I_{IL}	Low	$V_{IN} = 0.45V$			−250	μA
I_{IH}	High	$V_{IN} = 5.25V$			40	μA
Output current[1]						
I_{OZ}	Hi-Z State	$\overline{G}$ = High, $V_{OUT} = 5.25V$			40	μA
		$\overline{G}$ = High, $V_{OUT} = 0.5V$			−40	
I_{OS}	Short circuit[3]	$\overline{G}$, $\overline{GS}$ = Low, $V_{OUT} = 0V$ High stored	−15		−70	mA
Supply current[7]						
I_{CC}		$V_{CC} = 5.25V$		125	175	mA
Capacitance						
		$\overline{G}$ = High, $V_{CC} = 5.0V$				
C_{IN}	Input	$V_{IN} = 2.0V$		5		pF
C_{OUT}	Output	$V_{OUT} = 2.0V$		8		pF

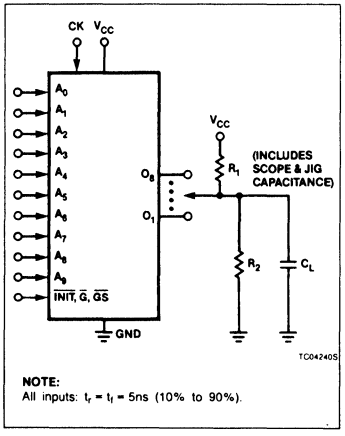
Notes on following page.

AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER[4]	TO	FROM	N82HS189			N82HS189A			UNIT
				Min	Typ[5]	Max	Min	Typ	Max	
t_{CSA} t_{CHA}	Setup Hold	CLK	Address	35 0			30 0			ns
t_{OC}	Delay	Output	CLK		10	20	0		15	ns
t_{WC}	Width	H & L	CLK	20	10		15			ns
t_{CSGS} t_{CHGS}	Setup Hold	CLK	$\overline{GS}$	15 5			10 5			ns
t_{CSIN} t_{CHIN}	Setup Hold	CLK	$\overline{INIT}$	25 0	8		20 0			ns
t_{OG}	Delay	Output	$\overline{G}$		11	25			20	ns
t_{OZC}[6]	Delay	Output	CLK		16	25			20	ns
t_{OZG}[6]	Delay	Output	$\overline{G}$		14	25			20	ns

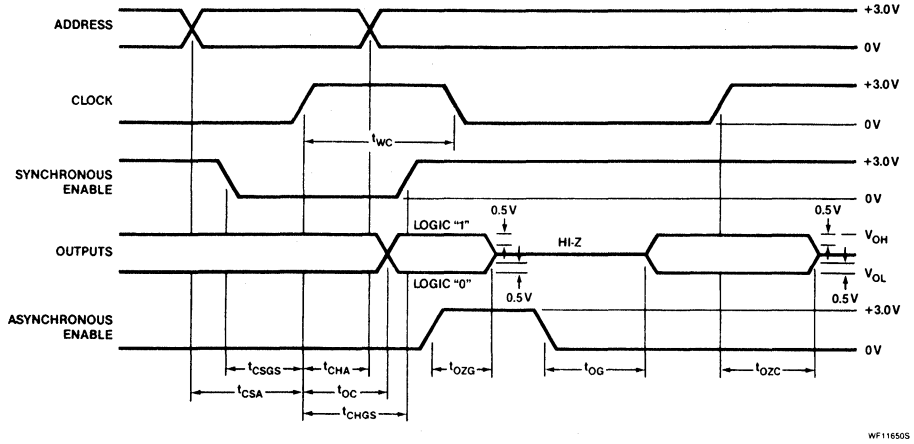
NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μs.
5. Typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
7. Measured with all inputs grounded and all outputs open.

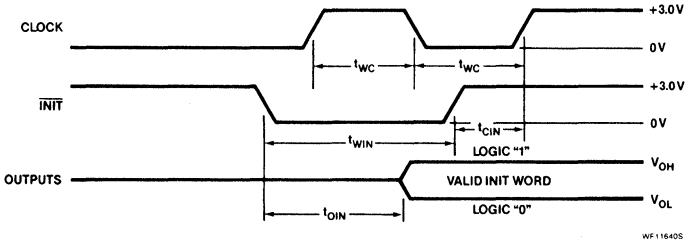
TEST LOAD CIRCUIT



NOTE:
All inputs: $t_r = t_f = 5ns$ (10% to 90%).

VOLTAGE WAVEFORMS





NOTE:
All AC parameters are measured at 1.5V unless otherwise specified.

16K-bit TTL PROM

		page
82S191	**16 384-bit TTL PROM (2048 x 8) 80 ns**	**441**
82S191A	**16 384-bit TTL PROM (2048 x 8) 55 ns**	**441**
82S191C	**16 384-bit TTL PROM (2048 x 8) 35 ns**	**445**
82HS191	**16 384-bit TTL PROM (2048 x 8) 25 ns**	**449**
82LHS191	**16 384-bit TTL PROM (2048 x 8) 35 ns**	**453**
82HS195	**16 384-bit TTL PROM (4096 x 4) 45 ns**	**457**
82HS195A	**16 384-bit TTL PROM (4096 x 4) 35 ns**	**457**
82HS195B	**16 384-bit TTL PROM (4096 x 4) 25 ns**	**457**

Signetics

82S191
82S191A
16K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82S191 and 82S191A are field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The 82S191 and 82S191A are supplied with all outputs at a logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

This device includes on-chip decoding and 3 Chip Enable inputs for ease of memory expansion. It features 3-State outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

The 82S191 and 82S191A devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

FEATURES

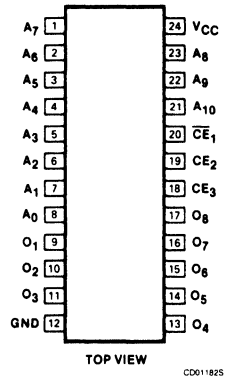
- **Address access time:**
  - **N82S191: 80ns max**
  - **N82S191A: 55ns max**
- **Power dissipation: 40μW/bit typ**
- **Input loading: −100μA max**
- **Three Chip Enable inputs**
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are Low level**
- **Fully TTL compatible**
- **Outputs: 3-State**

APPLICATIONS

- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATIONS

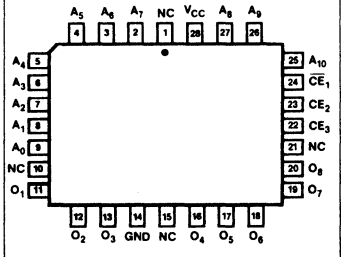
N Package



TOP VIEW

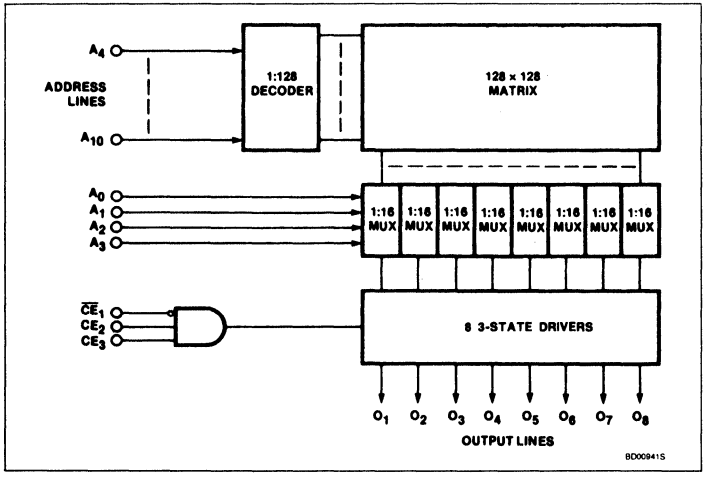
CD01182S

A Package



CD12551S

BLOCK DIAGRAM



ORDERING INFORMATION

PACKAGE DESCRIPTION	ORDER CODE
24-pin Plastic DIP 600mil-wide	N82S191 N • N82S191A N
28-pin Plastic Leaded Chip Carrier 450mil-square	N82S191 A • N82S191A A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-State	+5.5	V_{DC}
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temperature range	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage						
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			V
V_{IC}	Clamp	$I_{IN} = -12mA$		−0.8	−1.2	V
Output voltage						
		$\overline{CE}_1$ = Low, $CE_{2,3}$ = High				
V_{OL}	Low	I_{OUT} = 9.6mA			0.45	V
V_{OH}	High	$I_{OUT} = -2mA$	2.4			V
Input current[1]						
I_{IL}	Low	V_{IN} = 0.45V			−100	μA
I_{IH}	High	V_{IN} = 5.5V			40	μA
Output current[1]						
I_{OZ}	Hi-Z state	$\overline{CE}_1$ = High, $CE_{2,3}$ = Low, V_{OUT} = 0.5			−40	μA
		$\overline{CE}_1$ = High, $CE_{2,3}$ = Low, V_{OUT} = 5.5			40	
I_{OS}	Short circuit[3]	$\overline{CE}_1$ = Low, $CE_{2,3}$ = High, V_{OUT} = 0V	−15		−70	mA
Supply current[7]						
I_{CC}		V_{CC} = 5.25V		130	175	mA
Capacitance						
		$\overline{CE}_1$ = High, $CE_{2,3}$ = Low, V_{CC} = 5.0V				
C_{IN}	Input	V_{IN} = 2.0V		5		pF
C_{OUT}	Output	V_{OUT} = 2.0V		8		pF

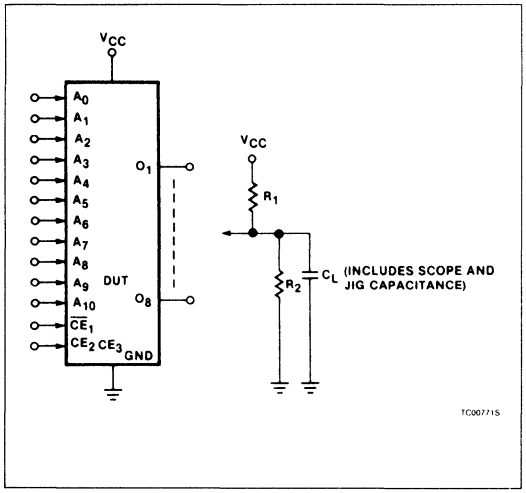
Notes on following page.

AC ELECTRICAL CHARACTERISTICS $R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

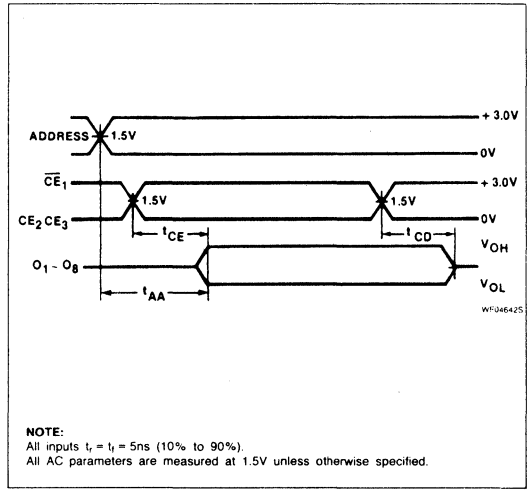
SYMBOL	PARAMETER	TO	FROM	N82S191			N82S191A			UNIT
				Min	Typ[5]	Max	Min	Typ	Max	
Access time[4]										
t_{AA}		Output	Address		50	80		50	55	ns
t_{CE}		Output	Chip Enable		30	40		20	30	ns
Disable time[6]										
t_{CD}		Output	Chip Disable		30	40		20	30	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μs.
5. Typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
7. Measured with all inputs grounded and all outputs open.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORMS



NOTE:
All inputs $t_r = t_f = 5ns$ (10% to 90%).
All AC parameters are measured at 1.5V unless otherwise specified.

82S191C
16K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82S191C is field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The 82S191C is supplied with all outputs at a logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

This device includes on-chip decoding and 3 Chip Enable inputs for ease of memory expansion. It features 3-State outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

The 82S191C devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

FEATURES

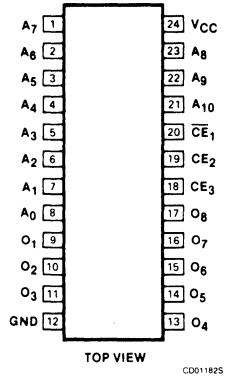
- **Address access time: 35ns max**
- **Power dissipation: 40μW/bit typ**
- **Input loading: −100μA max**
- **Three Chip Enable inputs**
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are Low level**
- **300mil-wide Plastic DIP**
- **Fully TTL compatible**
- **Outputs: 3-State**

APPLICATIONS

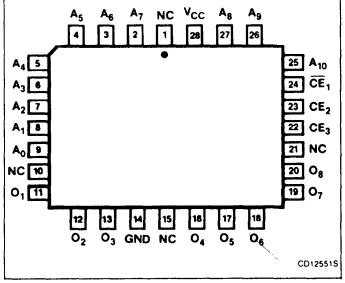
- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATIONS

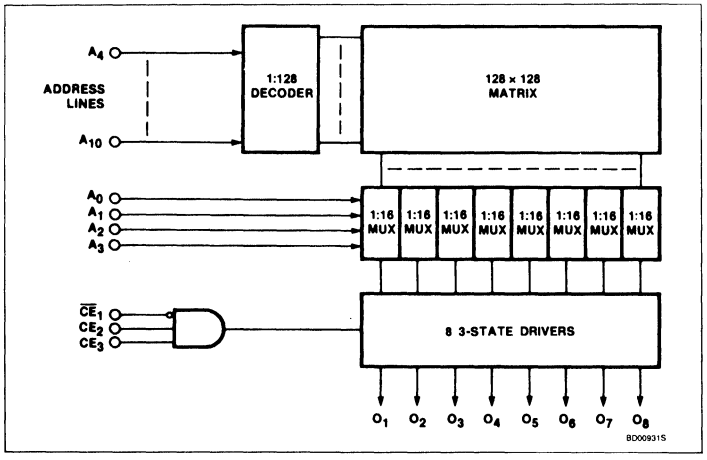
N Package



A Package



BLOCK DIAGRAM



ORDERING INFORMATION

PACKAGE DESCRIPTION	ORDER CODE
24-pin Plastic DIP 600mil-wide	N82S191C N
24-pin Plastic DIP 300mil-wide	N82S191C N3
28-pin Plastic Leaded Chip Carrier 450mil-square	N82S191C A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-State	+5.5	V_{DC}
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temperature range	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage						
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			V
V_{IC}	Clamp	$I_{IN} = -12mA$		−0.8	−1.2	V
Output voltage						
V_{OL}	Low	$\overline{CE}_1$ = Low, $CE_{2,3}$ = High, $I_{OUT} = 9.6mA$			0.45	V
V_{OH}	High	$I_{OUT} = -2mA$	2.4			V
Input current						
I_{IL}	Low	$V_{IN} = 0.45V$			−100	μA
I_{IH}	High	$V_{IN} = 5.5V$			40	μA
Output current[1]						
I_{OZ}	Hi-Z state	$\overline{CE}_1$ = High, $CE_{2,3}$ = Low, $V_{OUT} = 0.5$			−40	μA
		$\overline{CE}_1$ = High, $CE_{2,3}$ = Low, $V_{OUT} = 5.5$			40	
I_{OS}	Short circuit[3]	$\overline{CE}_1$ = Low, $CE_{2,3}$ = High, $V_{OUT} = 0V$	−15		−70	mA
Supply current[7]						
I_{CC}		$V_{CC} = 5.25V$		130	175	mA
Capacitance						
C_{IN}	Input	$V_{CC} = 5.0V$, $V_{IN} = 2.0V$		5		pF
C_{OUT}	Output	$V_{OUT} = 2.0V$		8		pF

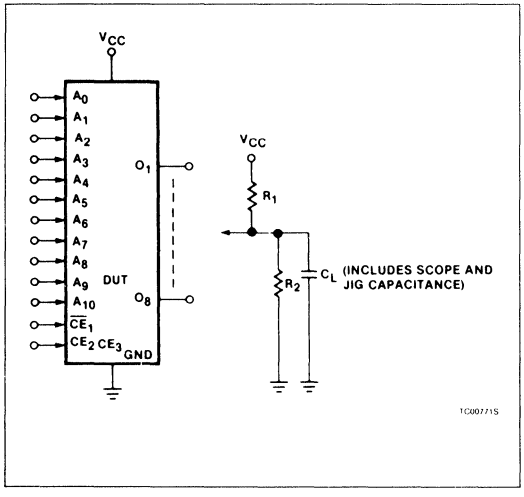
Notes on following page.

AC ELECTRICAL CHARACTERISTICS $R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

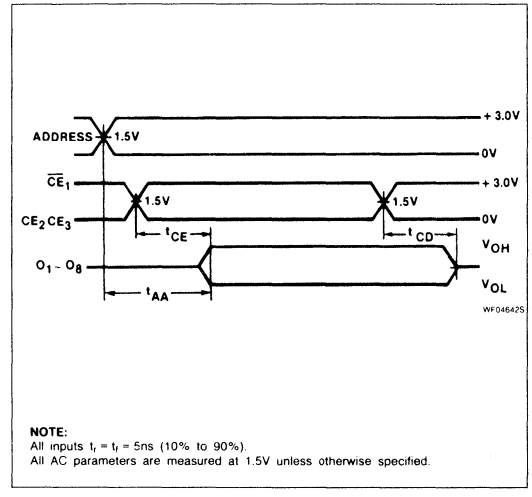
SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[5]	Max	
Access time[4]							
t_{AA}		Output	Address		30	35	ns
t_{CE}		Output	Chip Enable		15	20	ns
Disable time[6]							
t_{CD}		Output	Chip Disable		15	20	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μs.
5. Typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
7. Measured with all inputs grounded and all outputs open.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORMS



NOTE:
All inputs $t_r = t_f = 5ns$ (10% to 90%).
All AC parameters are measured at 1.5V unless otherwise specified.

82HS191
16K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82HS191 is field programmable, which means that custom patterns are immediately available by following the Signetics Generic II fusing procedure. The 82HS191 is supplied with all outputs at a logical High. Outputs are programmed to a logic Low level at any specified address by fusing the vertical junction matrix.

This device includes on-chip decoding and 3 Chip Enable inputs for ease of memory expansion. It features 3-State outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

The 82HS191 devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

FEATURES

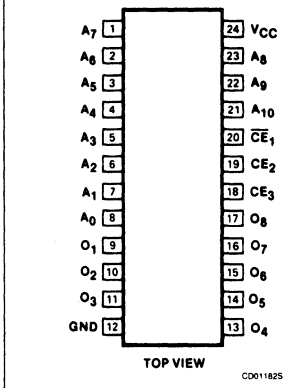
- **Address access time: 25ns max**
- **Power dissipation: 40μW/bit typ**
- **Input loading: −250μA max**
- **Three Chip Enable inputs**
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are High level**
- **300mil-wide Plastic DIP**
- **Fully TTL compatible**
- **Outputs: 3-State**

APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATIONS

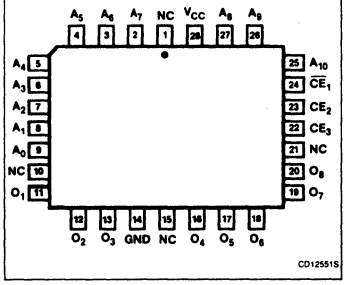
N Package



TOP VIEW

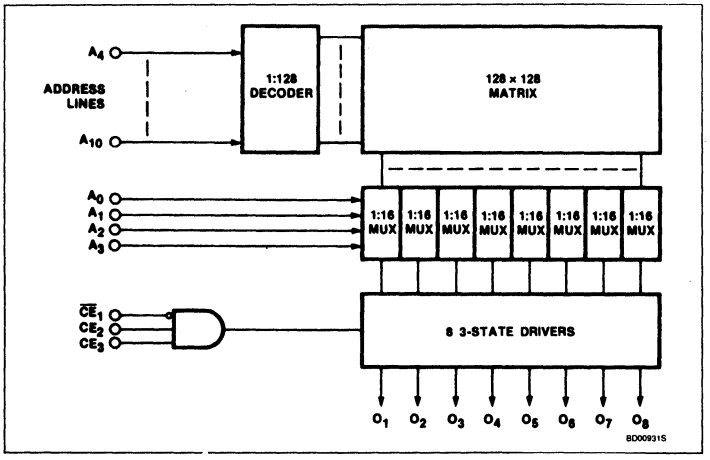
CD01182S

A Package



CD12551S

BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-pin Plastic DIP (600mil-wide)	N82HS191 N
24-pin Plastic DIP (300mil-wide)	N82HS191 N3
28-pin Plastic Leaded Chip Carrier (450mil-square)	N82HS191 A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-State	+5.5	V_{DC}
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temperature range	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leqslant T_A \leqslant +75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage						
V_{IL}	Low[3]				0.8	V
V_{IH}	High[3]		2.0			V
V_{IC}	Clamp	$I_{IN} = -18mA$		−0.8	−1.2	V
Output voltage						
V_{OL}	Low	$\overline{CE}_1$ = Low, $CE_{2,3}$ = High I_{OUT} = 16mA			0.5	V
V_{OH}	High	$\overline{CE}_1$ = Low, $CE_{2,3}$ = High $I_{OUT} = -2mA$	2.4			V
Input current						
I_{IL}	Low	$V_{IN} = 0.45V$			−250	μA
I_{IH}	High	$V_{IN} = 5.25V$			40	μA
Output current						
I_{OZ}	Hi-Z state	$\overline{CE}_1$ = High, $CE_{2,3}$ = Low, $V_{OUT} = 0.5$ $\overline{CE}_1$ = High, $CE_{2,3}$ = Low, $V_{OUT} = 5.25$			−40 40	μA
I_{OS}	Short circuit[3]	$\overline{CE}_1$ = Low, $CE_{2,3}$ = High, $V_{OUT} = 0V$	−15		−70	mA
Supply current[7]						
I_{CC}		$V_{CC} = 5.25V$		125	175	mA
Capacitance						
C_{IN}	Input	$\overline{CE}_1$ = High, $CE_{2,3}$ = Low, $V_{CC} = 5.0V$ $V_{IN} = 2.0V$		5		pF
C_{OUT}	Output	$\overline{CE}_1$ = High, $CE_{2,3}$ = Low, $V_{OUT} = 2.0V$		8		pF

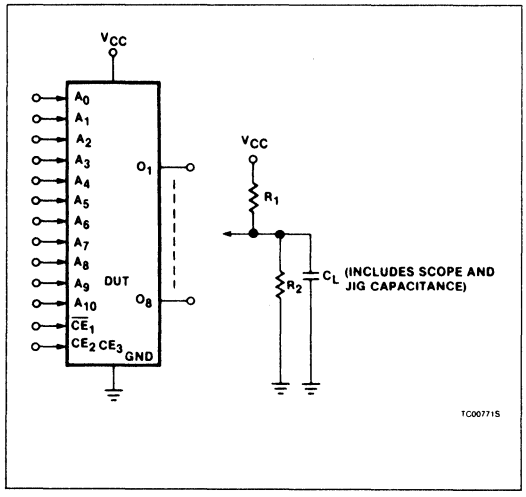
Notes on following page

AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

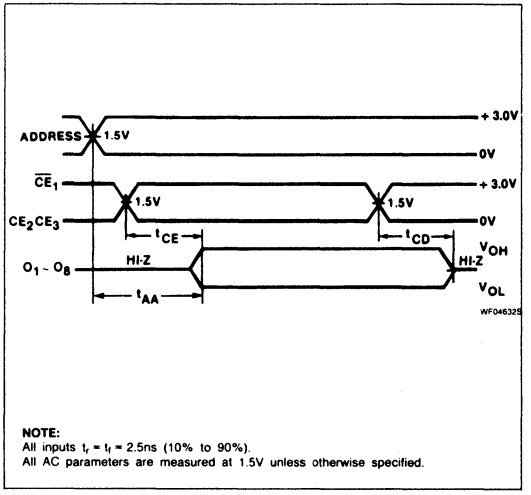
SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[5]	Max	
Access time[4]							
t_{AA}		Output	Address		15	25	ns
t_{CE}		Output	Chip enable		10	15	ns
Disable time[6]							
t_{CD}		Output	Chip disable		10	15	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μs.
5. Typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
7. Measured with all inputs grounded and all outputs open.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORMS



NOTE:
All inputs $t_r = t_f = 2.5ns$ (10% to 90%).
All AC parameters are measured at 1.5V unless otherwise specified.

82LHS191
16K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82LHS191 is field programmable, which means that custom patterns are immediately available by following the Signetics Generic II fusing procedure. The 82LHS191 is supplied with all outputs at a logical High. Outputs are programmed to a logic Low level at any specified address by fusing the vertical junction matrix.

This device includes on-chip decoding and 3 Chip Enable inputs for ease of memory expansion. It features 3-State outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

The 82LHS191 devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

FEATURES

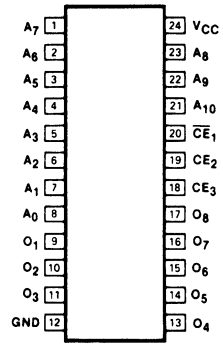
- **Address access time: 35ns max**
- **Power dissipation: 32μW/bit typ**
- **Input loading: −250μA max**
- **Three Chip Enable inputs**
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are High level**
- **300 mil-wide Plastic DIP**
- **Fully TTL compatible**
- **Outputs: 3-State**

APPLICATIONS

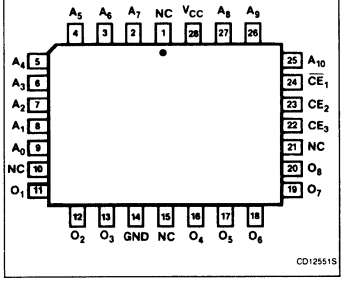
- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATIONS

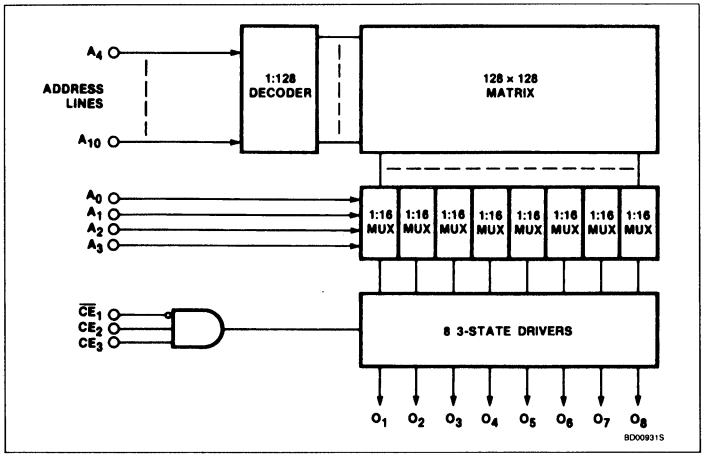
N Package



A Package



BLOCK DIAGRAM



16K-Bit TTL Bipolar PROM (2048 × 8) 82LHS191

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-pin Plastic DIP (600mil-wide)	N82LHS191 N
24-pin Plastic DIP (300mil-wide)	N82LHS191 N3
28-pin Plastic Leaded Chip Carrier (450mil-square)	N82LHS191 A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-State	+5.5	V_{DC}
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temperature range	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage						
V_{IL}	Low[3]				0.8	V
V_{IH}	High[3]		2.0			V
V_{IC}	Clamp	$I_{IN} = -18mA$		−0.8	−1.2	V
Output voltage						
V_{OL}	Low	$\overline{CE}_1$ = Low, $CE_{2,3}$ = High, I_{OUT} = 16mA			0.5	V
V_{OH}	High	$\overline{CE}_1$ = Low, $CE_{2,3}$ = High, $I_{OUT} = -2mA$	2.4			V
Input current						
I_{IL}	Low	$V_{IN} = 0.45V$			−250	μA
I_{IH}	High	$V_{IN} = 5.25V$			40	μA
Output current						
I_{OZ}	Hi-Z state	$\overline{CE}_1$ = High, $CE_{2,3}$ = Low, $V_{OUT} = 0.5$			−40	μA
		$\overline{CE}_1$ = High, $CE_{2,3}$ = Low, $V_{OUT} = 5.25$			40	
I_{OS}	Short circuit[3]	$\overline{CE}_1$ = Low, $CE_{2,3}$ = High, $V_{OUT} = 0V$	−15		−70	mA
Supply current[7]						
I_{CC}		$V_{CC} = 5.25V$		100	110	mA
Capacitance						
C_{IN}	Input	$\overline{CE}_1$ = High, $CE_{2,3}$ = Low, $V_{CC} = 5.0V$, $V_{IN} = 2.0V$		5		pF
C_{OUT}	Output	$\overline{CE}_1$ = High, $CE_{2,3}$ = Low, $V_{OUT} = 2.0V$		8		pF

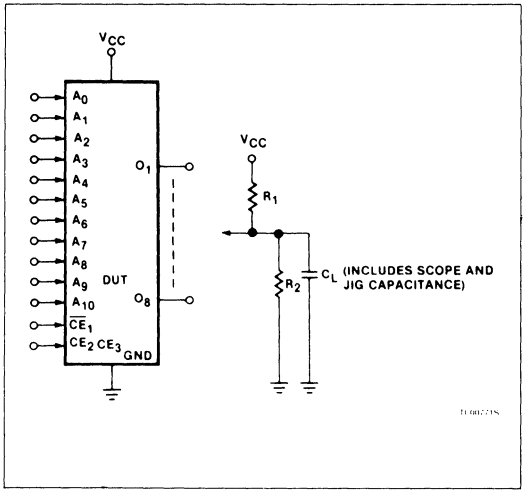
Notes on following page

AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

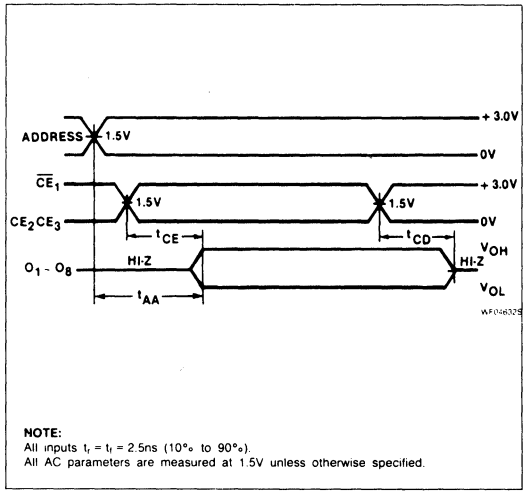
SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[5]	Max	
Access time[4]							
t_{AA}		Output	Address		30	35	ns
t_{CE}		Output	Chip enable		15	20	ns
Disable time[6]							
t_{CD}		Output	Chip disable		15	20	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μs.
5. Typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
7. Measured with all inputs grounded and all outputs open.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORMS



NOTE:
All inputs $t_r = t_f = 2.5ns$ (10% to 90%).
All AC parameters are measured at 1.5V unless otherwise specified.

82HS195
82HS195A
82HS195B
16K-Bit TTL Bipolar PROM

Bipolar Memory Products

Product Specification

DESCRIPTION

The 82HS195 is field programmable, which means that custom patterns are immediately available by following the Generic II fusing procedure. The Signetics 82HS195 is supplied with all outputs at logical High. Outputs are programmed to a logic Low level at any specified address by fusing a programmable matrix.

This device includes on-chip decoding and 2 Chip Enable inputs for memory expansion. It features 3-State outputs for optimization of word expansion in bused organizations.

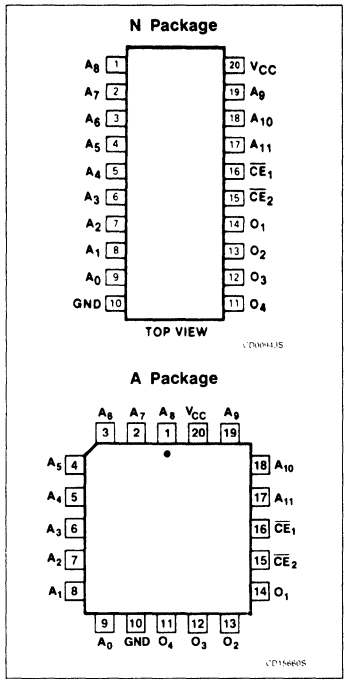
Ordering information can be found on the following page.

This device is also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

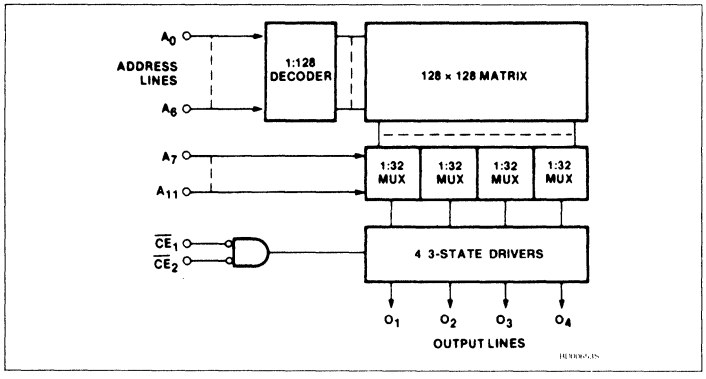
FEATURES

- **Low power dissipation: 35μW/bit typ**
- **Address access time:**
  - **N82HS195: 45ns max**
  - **N82HS195A: 35ns max**
  - **N82HS195B: 25ns max**
- **Input loading: −250μA max**
- **Two Chip Enable inputs**
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are High level**
- **Fully TTL compatible**
- **Outputs: 3-State**
- **SMD packaging 20-pin PLCC**

PIN CONFIGURATIONS



BLOCK DIAGRAM



ORDERING INFORMATION

PACKAGE DESCRIPTION	ORDER CODE
20-pin Plastic DIP 300mil-wide	N82HS195 N • N82HS195A N • N82HS195B N
20-pin Plastic Leaded Chip Carrier	N82HS195 A • N82HS195A A • N82HS195B A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-State	+5.5	V_{DC}
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temperature range	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS[1, 2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage						
V_{IL}	Low[3]				0.8	V
V_{IH}	High[3]		2.0			V
V_{IC}	Clamp	$I_{IN} = -12mA$		−0.8	−1.2	V
Output voltage						
		$\overline{CE}_1$ & $\overline{CE}_2$ = Low				
V_{OL}	Low	$I_{OUT} = 16mA$			0.45	V
V_{OH}	High	$I_{OUT} = -2mA$	2.4			V
Input current						
I_{IL}	Low	$V_{IN} = 0.45V$			−250	μA
I_{IH}	High	$V_{IN} = 5.25V$			40	μA
Output current						
I_{OZ}	Hi-Z State	$\overline{CE}_1$ & $\overline{CE}_2$ = High, $V_{OUT} = 0.5V$			−40	μA
		$\overline{CE}_1$ & $\overline{CE}_2$ = High, $V_{OUT} = 5.25V$			40	
I_{OS}	Short circuit[4]	$\overline{CE}_1$ & $\overline{CE}_2$ = Low, V_{OUT} = 0V, High stored	−15		−70	mA
Supply current[8]						
I_{CC}		$V_{CC} = 5.25V$		120	145	mA
Capacitance						
		$\overline{CE}_1$ & $\overline{CE}_2$ = High, $V_{CC} = 5.0V$				
C_{IN}	Input	$V_{IN} = 2.0V$		5		pF
C_{OUT}	Output	$V_{OUT} = 2.0V$		8		pF

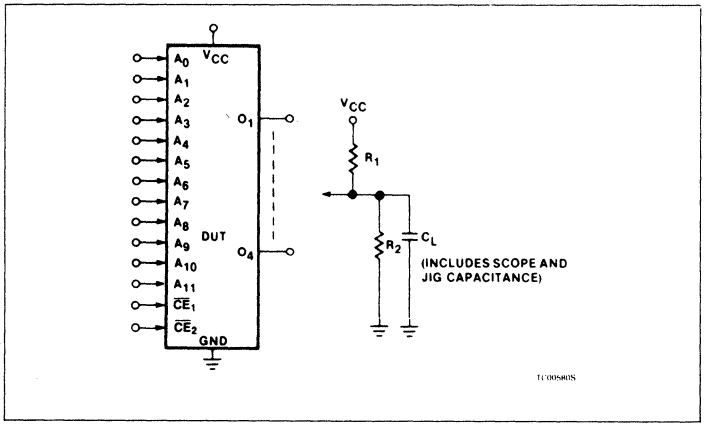
Notes on following page.

AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

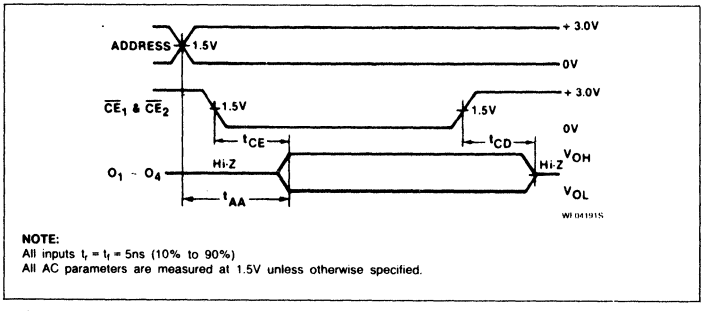
SYMBOL	PARAMETER	TO	FROM	N82HS195			N82HS195A			N82HS195B			UNIT
				Min	Typ[5]	Max	Min	Typ[5]	Max	Min	Typ[5]	Max	
Access time[7]													
t_{AA}		Output	Address		35	45		25	35		20	25	ns
t_{CE}		Output	Chip Enable		20	25		15	20		10	15	ns
Disable time[6]													
t_{CD}		Output	Chip Disable		20	25		15	20		10	15	ns

NOTES:
1. All voltage values are with respect to network ground terminal.
2. Positive current is defined as into the terminal referenced.
3. Measured with one output switching from a Logic "1" to a Logic "0".
4. Duration of the short circuit should not exceed 1 second.
5. Typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$, $C_L = 5pF$.
7. Tested at an address cycle time of $1\mu s$.
8. Measured with all inputs grounded and all outputs open.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORMS



NOTE:
All inputs $t_r = t_f = 5ns$ (10% to 90%)
All AC parameters are measured at 1.5V unless otherwise specified.

32K-bit TTL PROM

page

82HS321 **32 768-bit PROM (4096 x 8) 45 ns** **463**

82HS321A **32 768-bit PROM (4096 x 8) 35 ns** **463**

82HS321B **32 768-bit PROM (4096 x 8) 30 ns** **463**

82HS321C **32 768-bit PROM (4096 x 8) 25 ns** **467**

82LHS321 **32 768-bit PROM (4096 x 8) 35 ns** **471**

82HS321
82HS321A
82HS321B
32K-Bit TTL Bipolar PROM

Bipolar Memory Products

Product Specification

DESCRIPTION

The 82HS321 is field programmable, which means that custom patterns are immediately available by following the Signetics Generic II fusing procedure. The 82HS321 is supplied with all outputs at a logical High. Outputs are programmed to a logic Low level at any specified address by fusing a programmable matrix.

This device includes on-chip decoding and 2 Chip Enable inputs for ease of memory expansion. It features 3-State outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

This device is also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

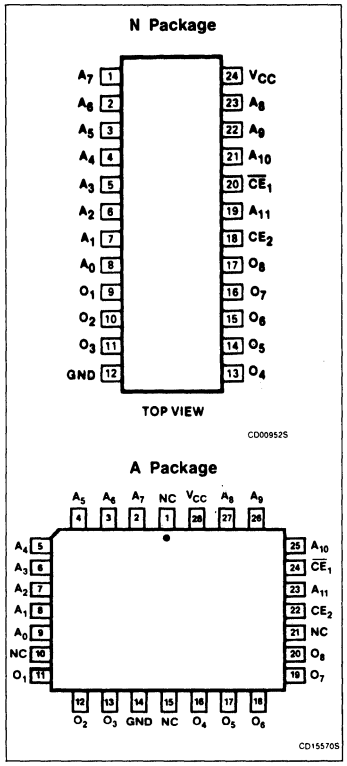
FEATURES

- **Address access time:**
  N82HS321: 45ns max
  N82HS321A: 35ns max
  N82HS321B 30ns max
- **Power dissipation: 20μW/bit typ**
- **Input loading: −250μA max**
- **Two Chip Enable inputs**
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are High level**
- **Fully TTL compatible**
- **Outputs: 3-State**

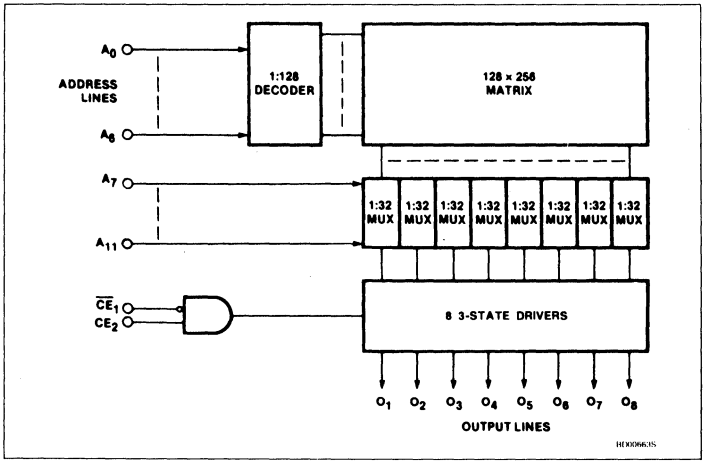
APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATIONS



BLOCK DIAGRAM



ORDERING INFORMATION

PACKAGE DESCRIPTION	ORDER CODE
24-pin Plastic DIP 600mil-wide	N82HS321 N • N82HS321A N • N82HS321B N
24-pin Ceramic DIP 600mil-wide	N82HS321 F • N82HS321A F • N82HS321B F
28-pin Plastic Leaded Chip Carrier 450mil-square	N82HS321 A • N82HS321A A • N82HS321B A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-State	+5.5	V_{DC}
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temperature range	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage						
V_{IL}	Low[3]				0.8	V
V_{IH}	High[3]		2.0			V
V_{IC}	Clamp	$I_{IN} = -18mA$		−0.8	−1.2	V
Output voltage						
		$\overline{CE}_1$ = Low, CE_2 = High				
V_{OL}	Low	$I_{OUT} = 16mA$			0.5	V
V_{OH}	High	$I_{OUT} = -2mA$	2.4			V
Input current						
I_{IL}	Low	$V_{IN} = 0.45V$			−250	μA
I_{IH}	High	$V_{IN} = 5.25V$			40	μA
Output current						
I_{OZ}	Hi-Z state	$\overline{CE}_1$ = High, CE_2 = Low, $V_{OUT} = 0.5$			−40	μA
		$\overline{CE}_1$ = High, CE_2 = Low, $V_{OUT} = 5.25$			40	
I_{OS}	Short circuit[4]	$\overline{CE}_1$ = Low, CE_2 = High, $V_{OUT} = 0V$	−15		−70	mA
Supply current[6]						
I_{CC}		$V_{CC} = 5.25V$		130	175	mA
Capacitance						
		$\overline{CE}_1$ = High, CE_2 = Low, $V_{CC} = 5.0V$				
C_{IN}	Input	$V_{IN} = 2.0V$		5		pF
C_{OUT}	Output	$V_{OUT} = 2.0V$		8		pF

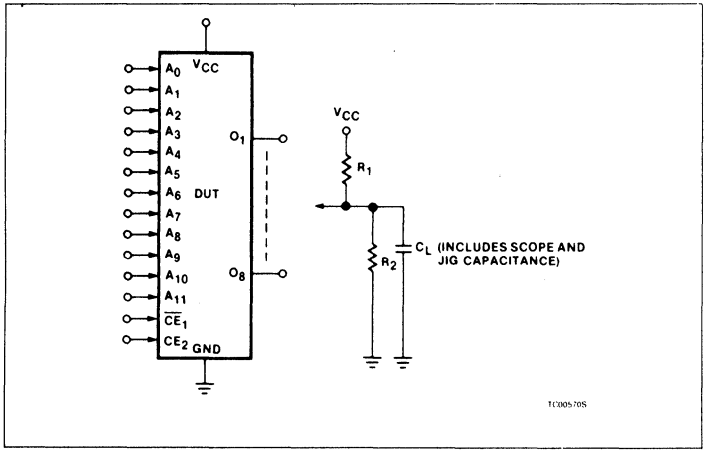
Notes on following page

AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

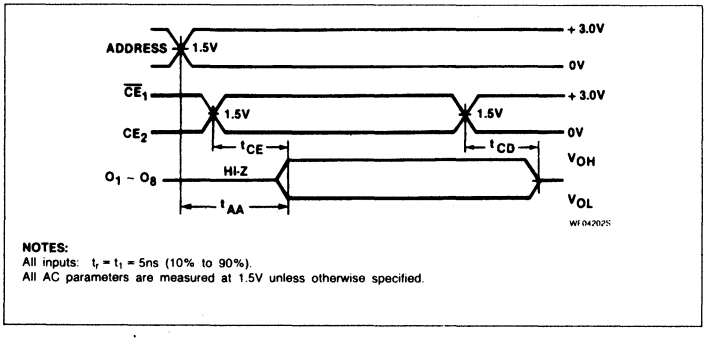
SYMBOL	PARAMETER	TO	FROM	N82HS321			N82HS321A			N82HS321B			UNIT
				Min	Typ[5]	Max	Min	Typ[5]	Max	Min	Typ[5]	Max	
Access time[7]													
t_{AA}		Output	Address		40	45		30	35		25	30	ns
t_{CE}		Output	Chip Enable		25	30		20	25		18	20	ns
Disable time[6]													
t_{CD}		Output	Chip Disable		25	30		20	25		18	20	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Measured with one output switching from from a Logic "1" to a Logic "0".
4. Duration of short circuit should not exceed 1 second.
5. Typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$, $C_L = 5pF$.
7. Tested at an address cycle time of $1\mu s$.
8. Measured with all inputs grounded and all outputs open.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



NOTES:
All inputs: $t_r = t_f = 5ns$ (10% to 90%).
All AC parameters are measured at 1.5V unless otherwise specified.

82HS321C
32K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82HS321 is field programmable, which means that custom patterns are immediately available by following the Signetics Generic II fusing procedure. The 82HS321 is supplied with all outputs at a logical High. Outputs are programmed to a logic Low level at any specified address by fusing a programmable matrix.

This device includes on-chip decoding and 2 Chip Enable inputs for ease of memory expansion. It features 3-State outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

This device is also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

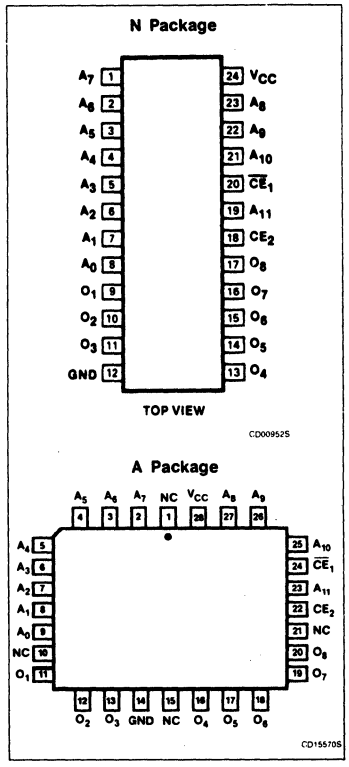
FEATURES

- **Address access time: N82HS321C: 25ns max**
- **Power dissipation: 20μW/bit typ**
- **Input loading: −250μA max**
- **Two Chip Enable inputs**
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are High level**
- **300mil-wide plastic DIP**
- **Fully TTL compatible**
- **Outputs: 3-State**

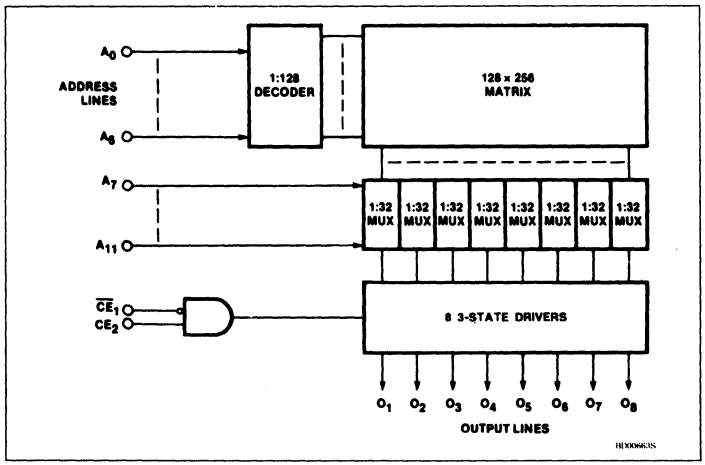
APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATIONS



BLOCK DIAGRAM



ORDERING INFORMATION

PACKAGE DESCRIPTION	ORDER CODE
24-pin Plastic DIP 600mil-wide	• N82HS321C N
24-pin Plastic DIP 300mil-wide	• N82HS321C N3
24-pin Ceramic DIP 600mil-wide	• N82HS321C F
28-pin Plastic Leaded Chip Carrier 450mil-square	• N82HS321C A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-State	+5.5	V_{DC}
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temperature range	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C,\ 4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage						
V_{IL}	Low[3]				0.8	V
V_{IH}	High[3]		2.0			V
V_{IC}	Clamp	$I_{IN} = -18mA$		−0.8	−1.2	V
Output voltage						
V_{OL}	Low	$\overline{CE}_1$ = Low, CE_2 = High I_{OUT} = 16mA			0.5	V
V_{OH}	High	$I_{OUT} = -2mA$	2.4			V
Input current						
I_{IL}	Low	$V_{IN} = 0.45V$			−250	μA
I_{IH}	High	$V_{IN} = 5.25V$			40	μA
Output current						
I_{OZ}	Hi-Z state	$\overline{CE}_1$ = High, CE_2 = Low, $V_{OUT} = 0.5$			−40	μA
		$\overline{CE}_1$ = High, CE_2 = Low, $V_{OUT} = 5.25$			40	
I_{OS}	Short circuit[4]	$\overline{CE}_1$ = Low, CE_2 = High, $V_{OUT} = 0V$	−15		−70	mA
Supply current[8]						
I_{CC}		$V_{CC} = 5.25V$		130	175	mA
Capacitance						
C_{IN}	Input	$\overline{CE}_1$ = High, CE_2 = Low, $V_{CC} = 5.0V$ $V_{IN} = 2.0V$		5		pF
C_{OUT}	Output	$V_{OUT} = 2.0V$		8		pF

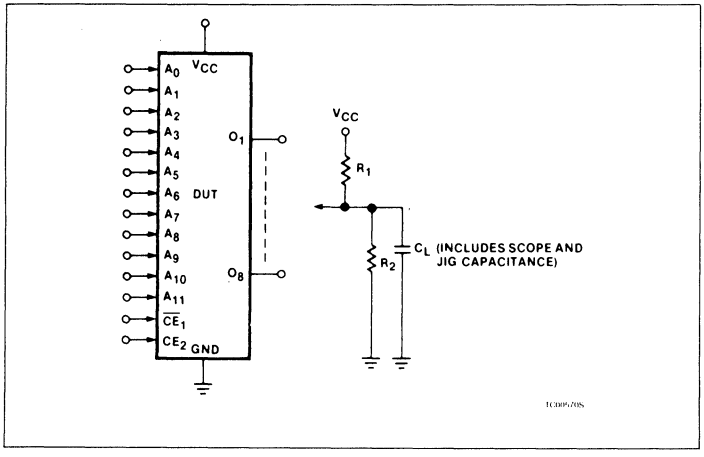
Notes on following page

AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

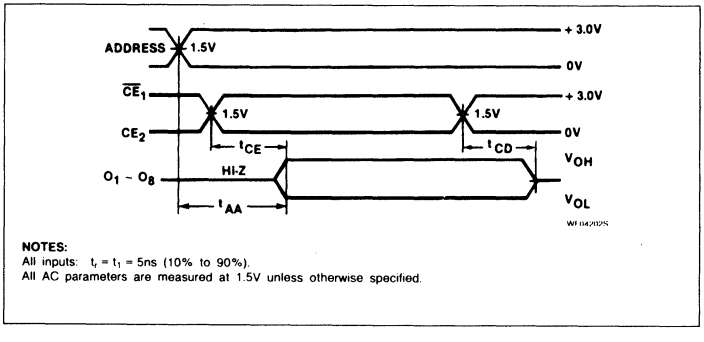
SYMBOL	PARAMETER	TO	FROM	N82HS321C			UNIT
				Min	Typ[5]	Max	
Access time[7]							
t_{AA}		Output	Address		20	25	ns
t_{CE}		Output	Chip Enable		10	15	ns
Disable time[6]							
t_{CD}		Output	Chip Disable		10	15	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Measured with one output switching from from a Logic "1" to a Logic "0".
4. Duration of short circuit should not exceed 1 second.
5. Typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$, $C_L = 5pF$.
7. Tested at an address cycle time of $1\mu s$.
8. Measured with all inputs grounded and all outputs open.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



NOTES:
All inputs: $t_r = t_f = 5ns$ (10% to 90%).
All AC parameters are measured at 1.5V unless otherwise specified.

82LHS321

32K–Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82LHS321 is field programmable, meaning that custom patterns are immediately available by following the Signetics Generic II fusing procedure. The 82LHS321 is supplied with all outputs at a logical High. Outputs are programmed to a logic Low level at any specified address by fusing the vertical junction matrix.

This device includes on–chip decoding and 2 Chip Enable inputs for ease of memory expansion. It features 3–State outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

This device is also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

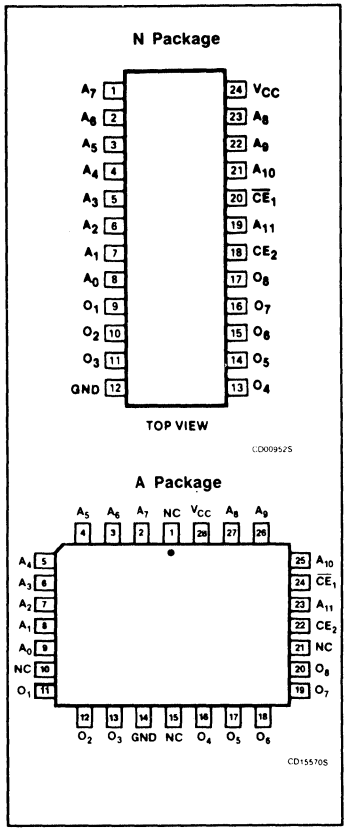
FEATURES

- **Address access time:**
  N82LHS321: 35ns max
- **Power dissipation: 16μW/bit typ**
- **Input loading: –250μA max**
- **Two Chip Enable Inputs**
- **On–chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are High level**
- **Fully TTL compatible**
- **Outputs: 3–State**

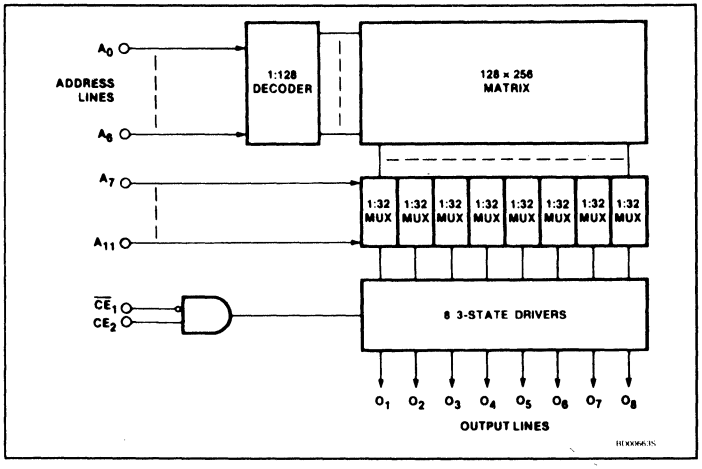
APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATIONS



BLOCK DIAGRAM



32K–Bit TTL Bipolar PROM (4096 × 8)

82LHS321

ORDERING INFORMATION

PACKAGE DESCRIPTION	ORDER CODE
24–pin Plastic DIP 600mil–wide	N82LHS321 N
24–pin Plastic DIP 300mil–wide	N82LHS321 N3
28–pin Plastic Leaded Chip Carrier 450mil–square	N82LHS321 A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off–State	+5.5	V_{DC}
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temperature range	–65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \le T_A \le +75°C, 4.75V \le V_{CC} \le 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS Min	LIMITS Typ[5]	LIMITS Max	UNIT
Input voltage						
V_{IL}	Low[3]				0.8	V
V_{IH}	High[3]		2.0			V
V_{IC}	Clamp	$I_{IN} = -18mA$		–0.8	–1.2	V
Output voltage						
		$\overline{CE}_1$ = Low, CE_2 = High				
V_{OL}	Low	$I_{OUT} = 16mA$			0.5	V
V_{OH}	High	$I_{OUT} = -2mA$	2.4			V
Input current						
I_{IL}	Low	$V_{IN} = 0.45V$			–250	µA
I_{IH}	High	$V_{IN} = 5.25V$			40	µA
Output current						
I_{OZ}	Hi–Z state	$\overline{CE}_1$ = High, CE_2 = Low, $V_{OUT} = 0.5$			–40	µA
		$\overline{CE}_1$ = High, CE_2 = Low, $V_{OUT} = 0.5$			40	
I_{OS}	Short circuit[4]	$\overline{CE}_1$ = Low, CE_2 = High, $V_{OUT} = 0V$	–15		–70	mA
Supply current[6]						
I_{CC}		$V_{CC} = 5.25V$		100	110	mA
Capacitance						
		$\overline{CE}_1$ = High, CE_2 = Low				
		$V_{CC} = 5.0V$				
C_{IN}	Input	$V_{IN} = 2.0V$		5		pF
C_{OUT}	Output	$V_{OUT} = 2.0V$		8		pF

NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Measured with one output switching from a Logic "1" to a Logic "0".
4. Duration of short circuit should not exceed 1 second.
5. Typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
6. Measured with all inputs grounded and all outputs open.

32K–Bit TTL Bipolar PROM (4096 × 8) 82LHS321

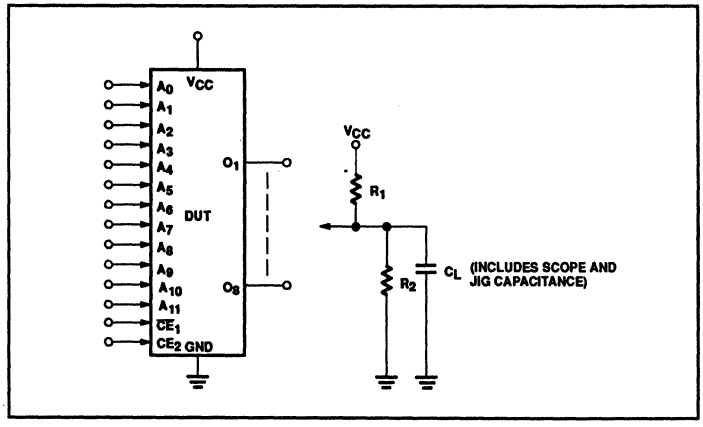
AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$

SYMBOL	PARAMETER	TO	FROM	LIMITS Min	LIMITS Typ[1]	LIMITS Max	UNIT
Access time[2]							
t_{AA}		Output	Address		30	35	ns
t_{CE}		Output	Chip Enable		20	25	ns
Disable time[3]							
t_{CD}		Output	Chip Disable		20	25	ns

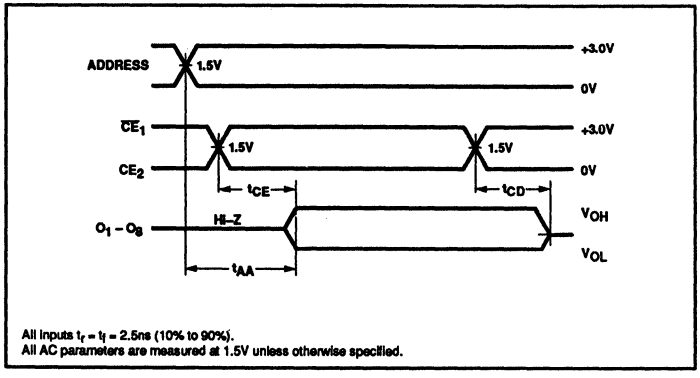
NOTES:

1. Typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
2. Tested at an address cycle time of 1µs.
3. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$, $C_L = 5pF$.

TEST LOAD CIRCUITS



VOLTAGE WAVEFORMS



All inputs $t_r = t_f = 2.5ns$ (10% to 90%).
All AC parameters are measured at 1.5V unless otherwise specified.

64K-bit TTL PROM

		page
82HS641	**65 536-bit PROM (8192 x 8) 55 ns**	**477**
82HS641A	**65 536-bit PROM (8192 x 8) 45 ns**	**477**
82HS641B	**65 536-bit PROM (8192 x 8) 35 ns**	**477**
82HS641C	**65 536-bit PROM (8192 x 8) 25 ns**	**481**

82HS641
82HS641A
82HS641B
64K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

The 82HS641 is field programmable, which means that custom patterns are immediately available by following the Signetics Generic II fusing procedure. The 82HS641 is supplied with all outputs at a logical High. Outputs are programmed to a logic Low level at any specified address by fusing the vertical junction matrix.

This device includes on-chip address decoding with 1 Chip Enable input for ease of memory expansion. It features 3-State outputs for optimization of word expansion in bused applications.

Ordering information can be found on the following page.

This device is also processed to military requirements for operating over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

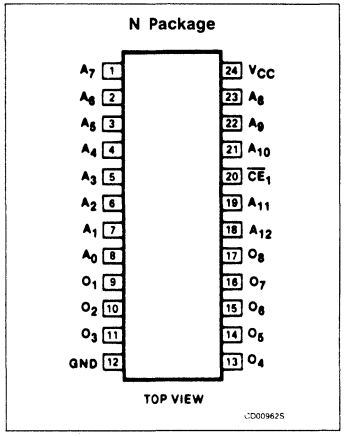
FEATURES

- **Address access time:**
  - **N82HS641 55ns max**
  - **N82HS641A 45ns max**
  - **N82HS641B 35ns max**
- **Power dissipation: 10μW/bit typ**
- **Input loading: -250μA max**
- **One Chip Enable input**
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are High level**
- **Fully TTL compatible**
- **Outputs: 3-State**

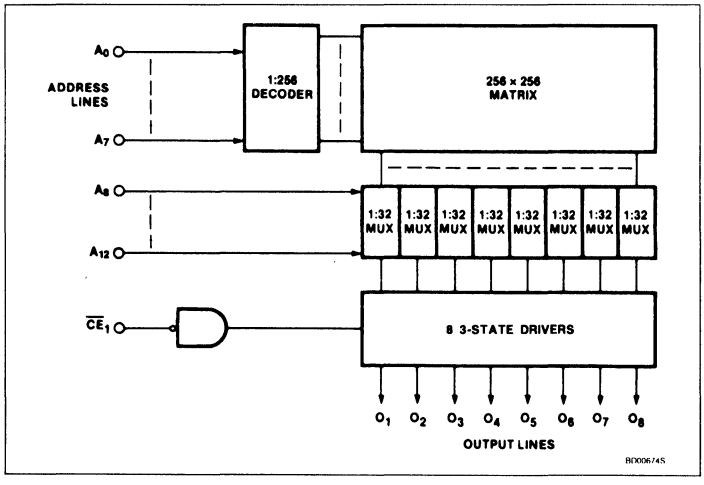
APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

PACKAGE DESCRIPTION	ORDER CODE
24-pin Plastic DIP 600mil-wide	N82HS641 N • N82HS641A N • N82HS641B N
24-pin Ceramic DIP 600mil-wide	N82HS641 F • N82HS641A F • N82HS641B F

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-state	+5.5	V_{DC}
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temperature range	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage						
V_{IL}	Low[3]				0.8	V
V_{IH}	High[3]		2.0			V
V_{IC}	Clamp	$I_{IN} = -18mA$		−0.8	−1.2	V
Output voltage						
		$\overline{CE}_1$ = Low				
V_{OL}	Low	$I_{OUT} = 16mA$			0.5	V
V_{OH}	High	$I_{OUT} = -2mA$	2.4			V
Input current						
I_{IL}	Low	$V_{IN} = 0.45V$			−250	μA
I_{IH}	High	$V_{IN} = 5.25V$			40	μA
Output current						
I_{OZ}	Hi-Z State	$\overline{CE}_1$ = High, $V_{OUT} = 0.5V$			−40	μA
		$\overline{CE}_1$ = High, $V_{OUT} = 5.25V$			40	
I_{OS}	Short circuit[4]	$\overline{CE}_1$ = Low, $V_{OUT} = 0V$	−15		−70	mA
Supply current[8]						
I_{CC}		$V_{CC} = 5.25V$		130	175	mA
Capacitance						
		$\overline{CE}_1$ = High				
		$V_{CC} = 5.0V$				
C_{IN}	Input	$V_{IN} = 2.0V$		5		pF
C_{OUT}	Output	$V_{OUT} = 2.0V$		8		pF

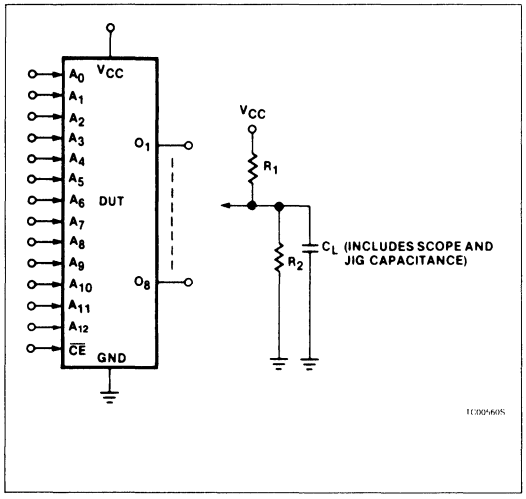
Notes on following page.

AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

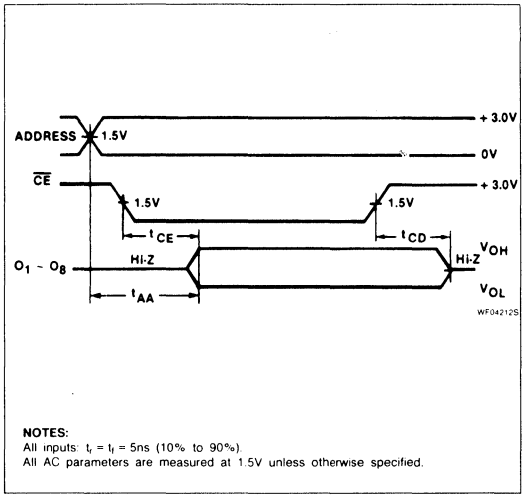
SYMBOL	PARAMETER	TO	FROM	N82HS641			N82HS641A			N82HS641B			UNIT
				Min	Typ[5]	Max	Min	Typ[5]	Max	Min	Typ[5]	Max	
Access time[7]													
t_{AA}		Output	Address		50	55		40	45		30	35	ns
t_{CE}		Output	Chip Enable		30	35		20	25		15	20	ns
Disable time[6]													
t_{CD}		Output	Chip Disable		30	35		20	25		15	20	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Measured with one output switching from a Logic "1" to a Logic "0".
4. Duration of short circuit should not exceed 1 second.
5. Typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$, $C_L = 5pF$.
7. Tested at an address cycle time of $1\mu s$.
8. Measured with all inputs grounded and all outputs open.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



NOTES:
All inputs: $t_r = t_f = 5ns$ (10% to 90%).
All AC parameters are measured at 1.5V unless otherwise specified.

82HS641C
64K-Bit TTL Bipolar PROM

Preliminary Specification

Bipolar Memory Products

The 82HS641 is field programmable, which means that custom patterns are immediately available by following the Signetics Generic II fusing procedure. The 82HS641 is supplied with all outputs at a logical High. Outputs are programmed to a logic Low level at any specified address by fusing the vertical junction matrix.

This device includes on-chip address decoding with 1 Chip Enable input for ease of memory expansion. It features 3-State outputs for optimization of word expansion in bused applications.

Ordering information can be found on the following page.

This device is also processed to military requirements for operating over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

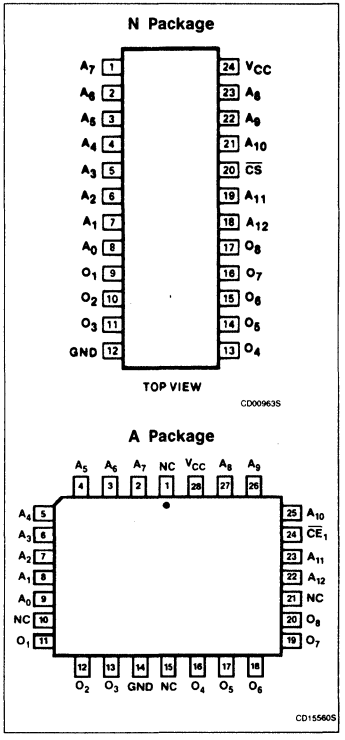
FEATURES

- **Address access time:**
  - **N82HS641C 25ns**
- **Power dissipation: 10μW/bit typ**
- **Input loading: −250μA max**
- **One Chip Enable input**
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are High level**
- **Fully TTL compatible**
- **Outputs: 3-State**

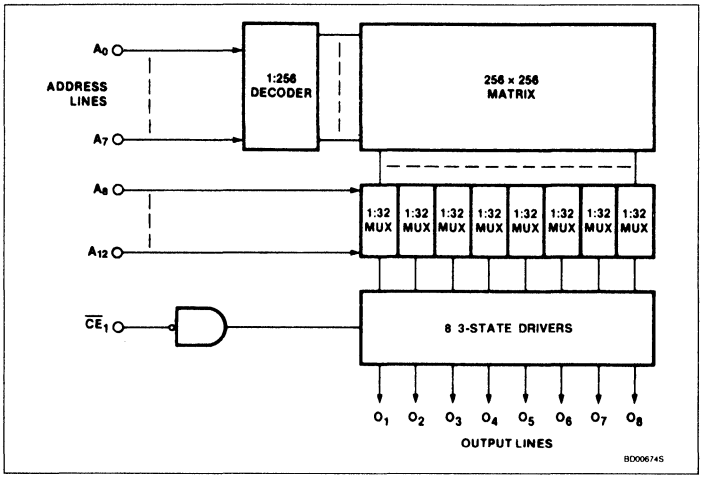
APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

PACKAGE DESCRIPTION	ORDER CODE
24-pin Plastic DIP 600mil-wide	• N82HS641C N
24-pin Ceramic DIP 600mil-wide	• N82HS641C F
28-pin Plastic PLCC 450mil-square	• N82HS641C A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-State	+5.5	V_{DC}
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temperature range	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage						
V_{IL}	Low[3]				0.8	V
V_{IH}	High[3]		2.0			V
V_{IC}	Clamp	$I_{IN} = -18mA$		−0.8	−1.2	V
Output voltage						
		$\overline{CE}_1$ = Low				
V_{OL}	Low	$I_{OUT} = 16mA$			0.5	V
V_{OH}	High	$I_{OUT} = -2mA$	2.4			V
Input current						
I_{IL}	Low	$V_{IN} = 0.45V$			−250	μA
I_{IH}	High	$V_{IN} = 5.25V$			40	μA
Output current						
I_{OZ}	Hi-Z State	$\overline{CE}_1$ = High, $V_{OUT} = 0.5V$			−40	μA
		$\overline{CE}_1$ = High, $V_{OUT} = 5.25V$			40	
I_{OS}	Short circuit[4]	$\overline{CE}_1$ = Low, $V_{OUT} = 0V$	−15		−70	mA
Supply current[8]						
I_{CC}		$V_{CC} = 5.25V$		130	175	mA
Capacitance						
		$\overline{CE}_1$ = High				
		$V_{CC} = 5.0V$				
C_{IN}	Input	$V_{IN} = 2.0V$		5		pF
C_{OUT}	Output	$V_{OUT} = 2.0V$		8		pF

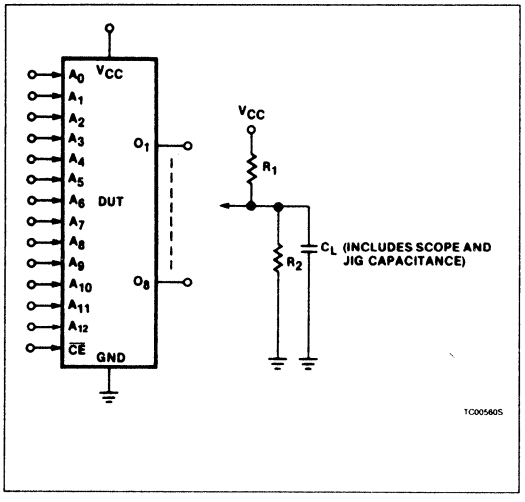
Notes on following page.

AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

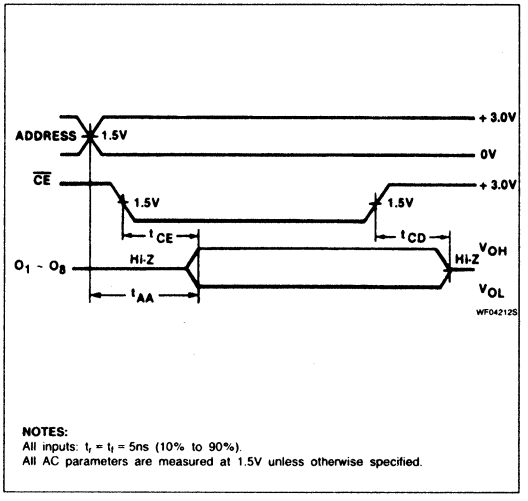
SYMBOL	PARAMETER	TO	FROM	N82HS641C			UNIT
				Min	Typ[5]	Max	
Access time[7]							
t_{AA}		Output	Address		22	25	ns
t_{CE}		Output	Chip Enable		14	15	ns
Disable time[6]							
t_{CD}		Output	Chip Disable		14	15	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Measured with one output switching from a Logic "1" to a Logic "0".
4. Duration of short circuit should not exceed 1 second.
5. Typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$, $C_L = 5pF$.
7. Tested at an address cycle time of $1\mu s$.
8. Measured with all inputs grounded and all outputs open.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



NOTES:
All inputs: $t_r = t_f = 5ns$ (10% to 90%).
All AC parameters are measured at 1.5V unless otherwise specified.

128K-bit TTL PROM

page

82HS1281 **131 072-bit PROM (16 384 x 8) 45 ns 487**

Document No.	
ECN No.	
Date of Issue	November 1986
Status	Objective Specification
Bipolar Memory Products	

82HS1281

128K–Bit TTL Bipolar PROM

DESCRIPTION

The 82HS1281 is field programmable, which means that custom patterns are immediately available by following the Signetics Generic II fusing procedure. The 82HS1281 is supplied with all outputs at a logical High. Outputs are programmed to a logic Low level at any specified address by fusing the vertical junction matrix.

This device includes on–chip address decoding with 4 Chip Enable inputs for ease of memory expansion. It features 3–State outputs for optimization of word expansion in bused organizations.

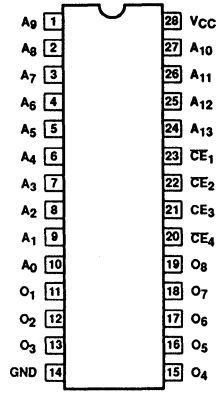
Ordering information can be found on the following page.

FEATURES

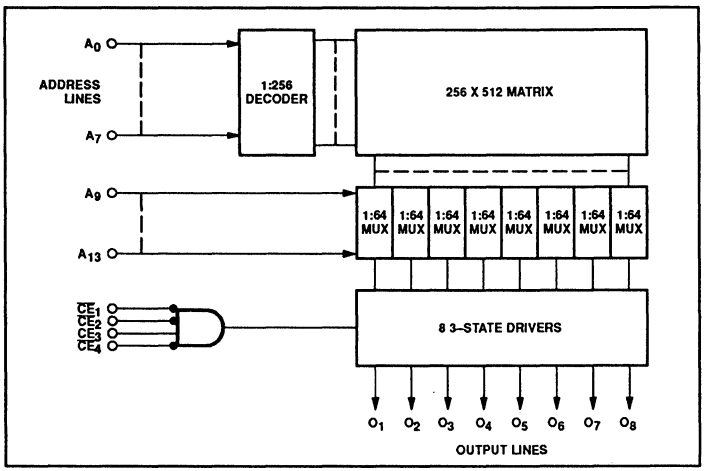
- Address access time: 45ns max
- Power dissipation: 5μW/bit typ
- Input loading: –250μA max
- Four Chip Enable inputs
- On–chip address decoding
- No separate fusing pins
- Unprogrammed outputs are High level
- Fully TTL compatible
- Outputs: 3–State

PIN CONFIGURATION

N Package



BLOCK DIAGRAM



APPLICATIONS

- Prototyping/volume production
- Sequential controllers
- Microprogramming
- Hardwired algorithms
- Control store
- Random logic
- Code conversion

128K–Bit TTL Bipolar PROM (16384 × 8)

82HS1281

ORDERING INFORMATION

PACKAGE DESCRIPTION	ORDER CODE
28–Pin Plastic DIP 600mil–wide	N82HS1281 N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off–State	+5.5	V_{DC}
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temperature range	–65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage						
V_{IL}	Low[3]				0.8	V
V_{IH}	High[3]		2.0			V
V_{IC}	Clamp	I_{IN} = –18mA		–0.8	–1.2	V
Output voltage						
		$\overline{CE}_3$ = High, $\overline{CE}_{1,2,4}$ = Low				
V_{OL}	Low	I_{OUT} = 16mA			0.5	V
V_{OH}	High	I_{OUT} = –2mA	2.4			V
Input current						
I_{IL}	Low	V_{IN} = 0.45V			–250	µA
I_{IH}	High	V_{IN} = 5.25V			40	µA
Output current						
I_{OZ}	Hi–Z state	CE_3 = Low, $\overline{CE}_{1,2,4}$ = High, V_{OUT} = 0.5V			–40	
		CE_3 = Low, $\overline{CE}_{1,2,4}$ = High, V_{OUT} = 5.25V			40	
I_{OS}	Short circuit[4]	CE_3 = High, $\overline{CE}_{1,2,4}$ = Low, V_{OUT} = 0V	–15		–70	mA
Supply current[6]						
I_{CC}		V_{CC} = 5.25V		100	110	mA
Capacitance						
		CE_3 = High, $\overline{CE}_{1,2,4}$ = Low V_{CC} = 5.0V				
C_{IN}	Input	V_{IN} = 2.0V		5		pF
C_{OUT}	Output	V_{OUT} = 2.0V		8		pF

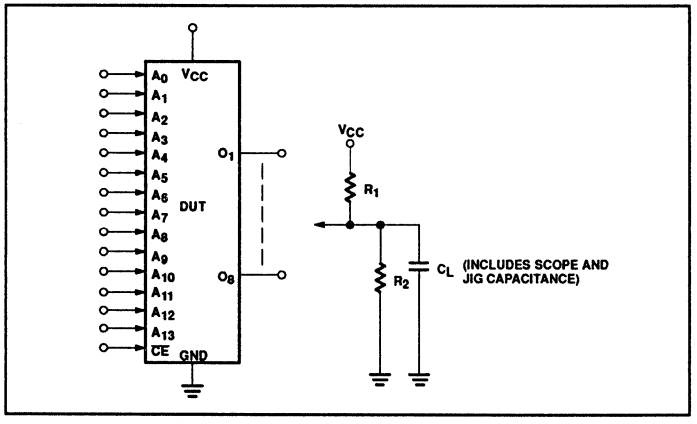
NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Measured with one output switching from a Logic "1" to a Logic "0".
4. Duration of short circuit should not exceed 1 second.
5. Typical values are at V_{CC} = 5V, T_A = +25°C.
6. Measured with all inputs grounded and all outputs open.

AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$

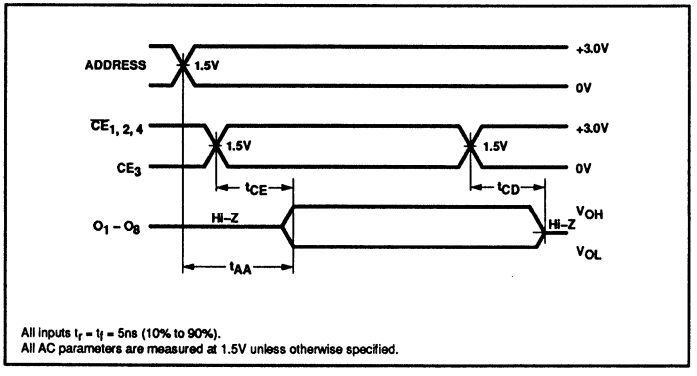
SYMBOL	PARAMETER	TO	FROM	LIMITS Min	LIMITS Typ[1]	LIMITS Max	UNIT
Access time[2]							
t_{AA}		Output	Address			45	ns
t_{CE}		Output	Chip Enable			25	ns
Disable time[3]							
t_{CD}		Output	Chip Disable			25	ns

NOTES:
1. Typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
2. Tested at an address cycle time of 1µs.
3. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$, $C_L = 5pF$.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORMS



All inputs $t_r = t_f = 5ns$ (10% to 90%).
All AC parameters are measured at 1.5V unless otherwise specified.

ECL MEMORIES

page

Low Complexity ECL PROM **493**
16K-bit ECL PROM **527**

Low Complexity ECL PROM

		page
10P256	**256-bit ECL Bipolar PROM (32 x 8) 3 ns**	**495**
100P256	**256-bit ECL Bipolar PROM (32 x 8) 3 ns**	**499**
10149	**1024-bit ECL Bipolar PROM (256 x 4) 20 ns**	**503**
100149	**1024-bit ECL Bipolar PROM (256 x 4) 20 ns**	**507**
10149A	**1024-bit ECL Bipolar PROM (256 x 4) 10 ns**	**511**
100149A	**1024-bit ECL Bipolar PROM (256 x 4) 10 ns**	**515**
10149B	**1024-bit ECL Bipolar PROM (256 x 4) 5 ns**	**519**
100149B	**1024-bit ECL Bipolar PROM (256 x 4) 5 ns**	**523**

10P256

256–Bit ECL Bipolar PROM

Preliminary Specification

Bipolar Memory Products

DESCRIPTION

The 10P256 is field programmable, meaning that custom patterns are immediately available by following the Signetics Generic IV Programming procedure. The device is supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the TiW link matrix.

The 10P256 is suitable for use in high–performance ECL systems. The outputs are capable of driving 50Ω loads.

The 10P256 has power pins placed in the center of the package to provide low inductance paths for output drive current.

A Chip Enable input is provided for ease of memory expansion.

Ordering information can be found on the following page.

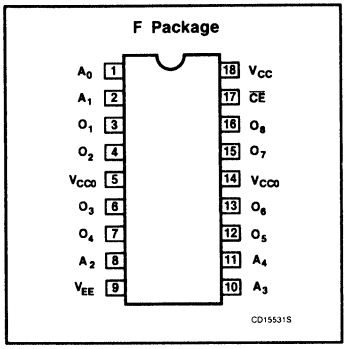
FEATURES

- **Address access time: 3ns max**
- **Power dissipation: 2.6mW/bit typ**
- **High–impedance inputs (50KΩ pulldown)**
- **One Chip Enable input**
- **Open Emitter outputs (50Ω drive)**
- **On–chip address decoding**
- **No separate fusing pins**
- **Fully compatible with ECL 10K series**
- **Center package power pins**

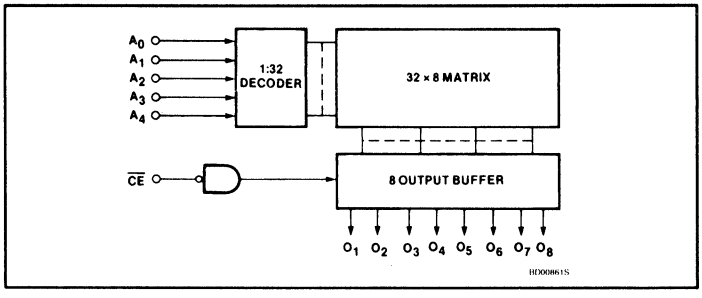
APPLICATIONS

- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATION



BLOCK DIAGRAM



256–Bit ECL Bipolar PROM (32 × 8)

10P256

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
18–pin Ceramic DIP (300mil–wide)	10P256 F

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER[1]	RATING	UNIT
V_{EE}	Supply voltage (V_{CC} = 0)	–8	V_{DC}
V_{IN}	Input voltage (V_{CC} = 0)	0 to –3	V_{DC}
I_O	Output source current	40	mA_{DC}
T_A	Operating temperature range	–0 to +75	°C
T_{STG}	Storage temperature range	–55 to +165	°C

NOTE:
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A < +75°C, -4.94V \leq V_{EE} \leq -5.46V$

			0°C		+25°C			+75°C		
SYMBOL	PARAMETER[1]	TEST CONDITIONS	Min	Max	Min	Typ[3]	Max	Min	Max	UNIT
Input voltage[2,3]										
V_{IL}	Low		–1.870		–1.850			–1.830		V
V_{IH}	High			–0.840			–0.810		–0.720	V
V_{ILA}	Low threshold			–1.480			–1.475		–1.445	V
V_{IHA}	High threshold		–1.150		–1.105			–1.040		V
Output voltage										
V_{OL}	Low	V_{IH} = Max	–1.870	–1.665	–1.850		–1.650	–1.830	–1.625	V
V_{OH}	High	V_{IL} = Min	–1.000	–0.840	–0.960		–0.810	–0.900	–0.720	V
V_{OLA}	Low threshold	V_{IHA} = Min, V_{ILA} = Max		–1.640			–1.630		–1.600	V
V_{OHA}	High threshold	V_{IHA} = Min, V_{ILA} = Max	–1.020		–0.980			–0.920		V
Input current[4]										
I_{IL}	Low	V_{IH} = Max			0.5					µA
I_{IH}	High	V_{IL} = Min		250			250		250	µA
Supply drain current										
I_{EE}		V_{EE} = –5.2V		150		130	150		150	mA

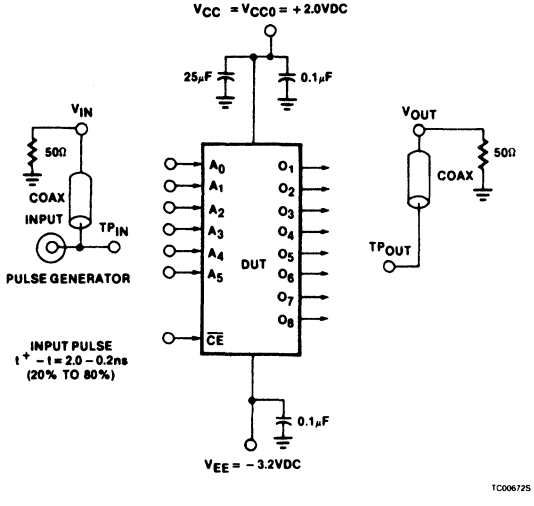
NOTES:
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. Each ECL 10K series device has been designed to meet the DC specification after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 4mV with an air flow of 200 linear fpm. Outputs are terminated through a 50Ω resistor to –2V.
3. Typical values are at V_{EE} = –5.2V, T_A = +25°C.
4. Unused inputs must have 10KΩ min to V_{EE} or be connected to $-2V_{DC}$.

AC ELECTRICAL CHARACTERISTICS $R_1 = 50\Omega$, $0°C \leq T_A \leq +75°C$, $-4.94V \leq V_{EE} \leq -5.46V$

SYMBOL	PARAMETER	TO	FROM	LIMITS Min	LIMITS Typ[1]	LIMITS Max	UNIT
Access time							
t_{AA}		Output	Address			3	ns
t_{CE}		Output	Chip Enable		1.3	2	ns
Disable time							
t_{CD}		Output	Chip Disable		1.3	2	ns
Rise and fall time							
t_+	Rise time (20–80%)				1.0		ns
t_-	Fall time (80–20%)				1.0		ns

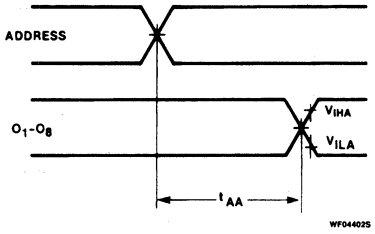
NOTES:
1. Typical values are at $V_{EE} = -5.2V$, $T_A = +25°C$.

TEST LOAD CIRCUIT

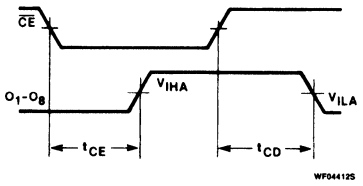


NOTES:
1. For AC tests, all input and output cables to the scope are equal lengths of 50Ω coaxial cable. Wire length should be < ¼ inch from TP_{IN} to input pin and TP_{OUT} to output pin. A 50Ω termination to ground is located in each scope input. Unused outputs are connected to a 50Ω resistor to ground.
2. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
3. Normal practice in test fixtures layout should be followed. Lead lengths, particularly to the power supply, should be as short as possible. A 10μF capacitor between V_{CC} and V_{CCO} terminals, located as close to the device as possible, is recommended to reduce ringing.

VOLTAGE WAVEFORMS



Address Access Time



Chip Enable/Disable Propagation Delays

100P256

256–Bit ECL Bipolar PROM

Preliminary Specification

Bipolar Memory Products

DESCRIPTION

The 100P256 is field programmable, meaning that custom patterns are immediately available by following the Signetics Generic IV Programming procedure. The device is supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the TiW link matrix.

The 100P256 is suitable for use in high–performance ECL systems. The outputs are capable of driving 50Ω loads.

The 100P256 has power pins placed in the center of the package to provide low inductance paths for output drive current.

A Chip Enable input is provided for ease of memory expansion.

Ordering information can be found on the following page.

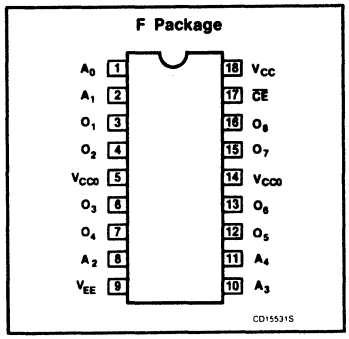
FEATURES

- **Address access time: 3ns max**
- **Power dissipation: 2.2mW/bit typ**
- **High–impedance inputs (50KΩ pulldown)**
- **One Chip Enable input**
- **Open Emitter outputs (50Ω drive)**
- **On–chip address decoding**
- **No separate fusing pins**
- **Fully compatible with ECL 100K series**
- **Center package power pins**

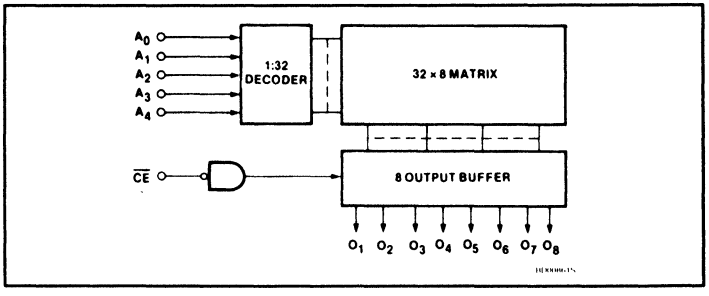
APPLICATIONS

- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATION



BLOCK DIAGRAM



256–Bit ECL Bipolar PROM (32 × 8) 100P256

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
18–pin Ceramic DIP (300mil–wide)	100P256 F

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{EE}	Supply voltage (V_{CC} = 0)	–8	V_{DC}
V_{IN}	Input voltage (V_{CC} = 0)	0 to –3	V_{DC}
I_O	Output source current	40	mA_{DC}
T_A	Operating temperature range	–0 to +75	°C
T_{STG}	Storage temperature range	–55 to +165	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A < +75°C, -4.275V \leq V_{EE} \leq -4.725V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[4]	Max	
Input voltage						
V_{IL}	Low		–1.810			V
V_{IH}	High				–0.880	V
V_{ILA}	Threshold Low				–1.475	V
V_{IHA}	Threshold High		–1.165			V
Output voltage						
V_{OL}	Low	V_{IL} = Min	–1.810		–1.620	V
V_{OH}	High	V_{IH} = Max	–1.025		–0.880	V
V_{OLA}	Threshold Low	V_{IL} = Max			–1.610	V
V_{OHA}	Threshold High	V_{IH} = Min	–1.035			V
Input current[5]						
I_{IL}	Low	V_{IL} = Min	0.5			µA
I_{IH}	High	V_{IH} = Max			220	µA
Supply current						
I_{EE}		V_{EE} = –4.5V		130	150	mA

NOTES:
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. Each ECL 100K series device has been designed to meet the DC specification after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 400 linear fpm is maintained. Voltage levels will shift approximately 4mV with an air flow of 200 linear fpm. Outputs are terminated through a 50Ω resistor to –2V.
3. For current measurements, maximum is defined as the maximum absolute value.
4. Typical values are at V_{EE} = –4.5V, T_A = +25°C.
5. Unused inputs must have 10KΩ min to V_{EE} or be connected to $-2V_{DC}$.

256–Bit ECL Bipolar PROM (32 × 8) 100P256

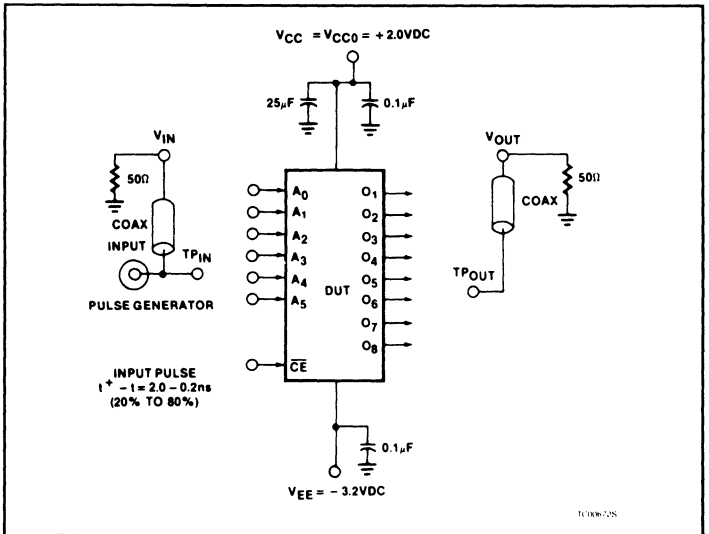
AC ELECTRICAL CHARACTERISTICS $R_1 = 50\Omega$, $0°C \leq T_A \leq +75°C$, $-4.275V \leq V_{EE} \leq -4.725V$

SYMBOL	PARAMETER	TO	FROM	LIMITS Min	LIMITS Typ[1]	LIMITS Max	UNIT
Access time							
t_{AA}		Output	Address			3	ns
t_{CE}		Output	Chip enable		1.3	2	ns
Disable time							
t_{CD}		Output	Chip disable		1.3	2	ns
Rise and fall time							
t^+	Rise time (20–80%)				1.0		ns
t^-	Fall time (80–20%)				1.0		ns

NOTE:

1. Typical values are at $V_{EE} = -4.5V$, $T_A = +25°C$.

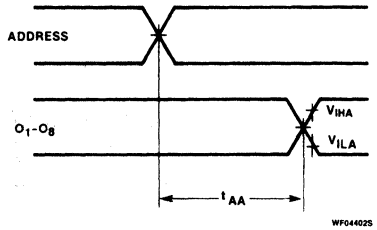
TEST LOAD CIRCUIT



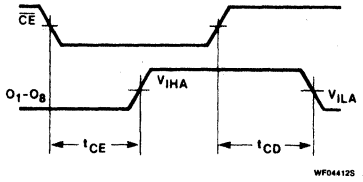
NOTES:

1. For AC tests, all input and output cables to the scope are equal lengths of 50Ω coaxial cable. Wire length should be ≤ ¼ inch from TP_{IN} to input pin and TP_{OUT} to output pin. A 50Ω termination to ground is located in each scope input. Unused outputs are connected to a 50Ω resistor to ground.
2. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
3. Normal practice in test fixtures layout should be followed. Lead lengths, particularly to the power supply, should be as short as possible. A 10μF capacitor between V_{CC} and V_{CCO} terminals, located as close to the device as possible, is recommended to reduce ringing.

VOLTAGE WAVEFORMS



Address Access Time



Chip Enable/Disable Propagation Delays

10149
1K-Bit ECL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 10149 is field programmable, meaning that custom patterns are immediately available by following the Generic IV fusing procedure. The device is supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

The 10149 is suitable for use in high-performance ECL systems. The outputs are capable of driving 50Ω loads.

A Chip Enable input is provided for ease of memory expansion.

Ordering information can be found on the folowing page.

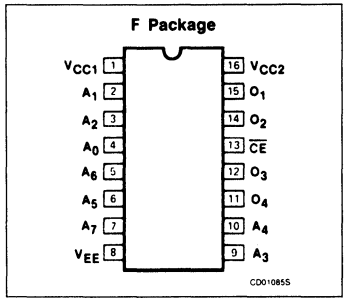
FEATURES

- **Address access time: 20ns max**
- **Power dissipation: 0.66mW/bit typ**
- **High impedance inputs (50kΩ pulldown)**
- **One Chip Enable input**
- **Open Emitter outputs (50Ω drive)**
- **On-chip address decoding**
- **No separate fusing pins**
- **Fully compatible with ECL 10K series**

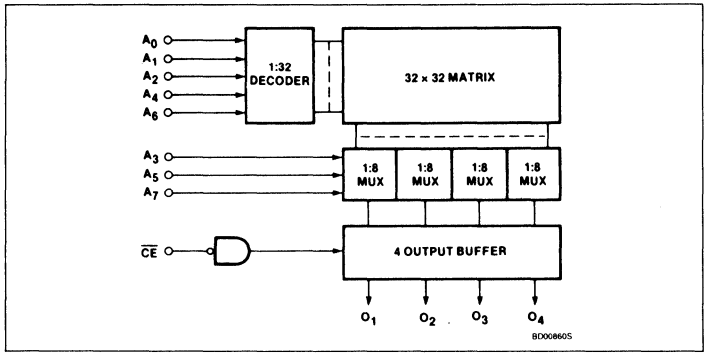
APPLICATIONS

- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATION



BLOCK DIAGRAM



1K-Bit ECL Bipolar PROM (256 × 4) 10149

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-pin Ceramic DIP 300mil-wide	10149 F

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER[1]	RATING	UNIT
V_{EE}	Supply voltage (V_{CC} = 0)	−8	V_{DC}
V_{IN}	Input voltage (V_{CC} = 0)	0 to V_{EE}	V_{DC}
I_O	Output source current	40	mA_{DC}
T_A	Operating temperature range	−30 to +85	°C
T_{STG}	Storage temperature range	−55 to +165	

DC ELECTRICAL CHARACTERISTICS $-30°C \leq T_A < +85°C$, $-4.94V \leq V_{EE} \leq -5.46V$

SYMBOL	PARAMETER[1]	TEST CONDITIONS	−30°C		+25°C			+85°C		UNIT
			Min	Max	Min	Typ[3]	Max	Min	Max	
Input voltage[2,3]										
V_{IL}	Low		−1.890		−1.850			−1.825		V
V_{IH}	High			−0.890			−0.810		−0.700	
V_{ILA}	Low threshold			−1.500			−1.475		−1.440	
V_{IHA}	High threshold		−1.205		−1.105			−1.035		
Output voltage										
V_{OL}	Low	V_{IH} = Max	−1.89	−1.675	−1.85		−1.65	−1.825	−1.615	V
V_{OH}	High	V_{IL} = Min	−1.06	−0.89	−0.96		−0.81	−0.89	−0.70	
V_{OLA}	Low threshold	V_{IHA} = Min, V_{ILA} = Max		−1.655			−1.63		−1.595	
V_{OHA}	High threshold		−1.08		−0.98			−0.91		
Input current										
I_{IL}	Low	V_{IH} = Max			0.5					μA
I_{IH}	High	V_{IL} = Min		250			250		250	
Supply drain current										
I_{EE}		V_{EE} = −5.2V		160		150	160		160	mA

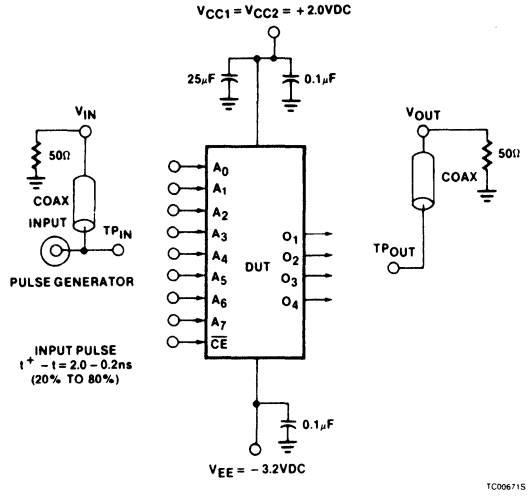
AC ELECTRICAL CHARACTERISTICS $R_1 = 50\Omega$, $-30°C \leq T_A \leq +85°C$, $-4.94V \leq V_{EE} \leq -5.46V$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[3]	Max	
Access time							
t_{AA}		Output	Address		14	20	ns
t_{CE}		Output	Chip Enable		4	8	
Disable time							
t_{CD}		Output	Chip Enable		4	8	ns
Rise and fall time							
t_+	Rise time (20-80%)				4.0		ns
t_-	Fall time (80-20%)				4.0		

NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. Each ECL 10K series device has been designed to meet the DC specification after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 4mV with an air flow of 200 linear fpm. Outputs are terminated through a 50Ω resistor to −2V.
3. Typical values are at V_{EE} = −5.2V, T_A = +25°C.

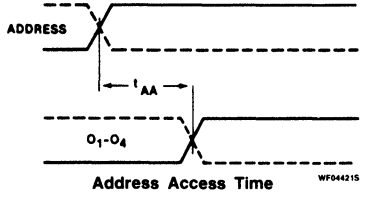
TEST LOAD CIRCUIT



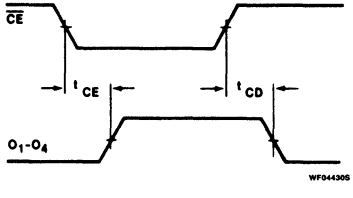
NOTES:

1. For AC tests, all input and output cables to the scope are equal lengths of 50Ω coaxial cable wire length should be < ¼ inch from TP_{IN} to input pin and TP_{OUT} to output pin. A 50Ω termination to ground is located in each scope input. Unused outputs are connected to a 50Ω resistor to ground.
2. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
3. Normal practice in test fixtures layout should be followed. Lead lengths, particularly to the power supply, should be as short as possible. A 10μF capacitor between V_{CC1} and V_{CC2} terminals, located as close to the device as possible, is recommended to reduce ringing.

VOLTAGE WAVEFORMS



Address Access Time



Chip Enable/Disable Propagation Delays

100149
1K-Bit ECL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 100149 is field programmable, meaning that custom patterns are immediately available by following the Generic IV fusing procedure. The device is supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

The 100149 is suitable for use in high-performance ECL systems. The outputs are capable of driving 50Ω loads.

A Chip Enable input is provided for ease of memory expansion.

Ordering information can be found on the following page.

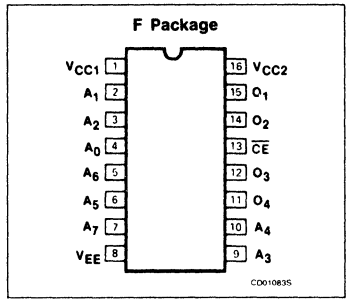
FEATURES

- **Address access time: 20ns max**
- **Power dissipation: 0.66mW/bit typ**
- **High impedance inputs (50kΩ pulldown)**
- **One Chip Enable input**
- **Open Emitter outputs (50Ω drive)**
- **On-chip address decoding**
- **No separate fusing pins**
- **Fully compatible with ECL 100K series**

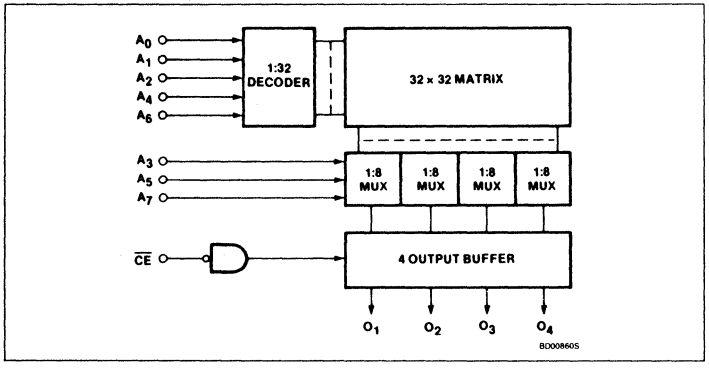
APPLICATIONS

- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-pin Ceramic DIP 300mil-wide	100149 F

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{EE}	Supply voltage (V_{CC} = 0)	−8	V_{DC}
V_{IN}	Input voltage (V_{CC} = 0)	0 to V_{EE}	V_{DC}
I_O	Output source current	40	mA_{DC}
T_A	Operating temperature range	−0 to +75	°C
T_{STG}	Storage temperature range	−55 to +165	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leqslant T_A \leqslant +75°C$, $-4.275V \leqslant V_{EE} \leqslant -4.725V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[4]	Max	
Input voltage						
V_{IL}	Low		−1.810			V
V_{IH}	High				−0.880	V
V_{ILA}	Threshold Low				−1.475	V
V_{IHA}	Threshold High		−1.165			V
Output voltage						
V_{OL}	Low	V_{IL} = Min	−1.810		−1.620	V
V_{OH}	High	V_{IH} = Max	−1.025		−0.880	V
V_{OLA}	Threshold Low	V_{IL} = Max			−1.610	V
V_{OHA}	Threshold High	V_{IH} = Min	−1.035			V
Input current						
I_{IL}	Low	V_{IL} = Min	0.5			μA
I_{IH}	High	V_{IH} = Max			220	μA
Supply current						
I_{EE}		V_{EE} = −4.5V		150	180	mA

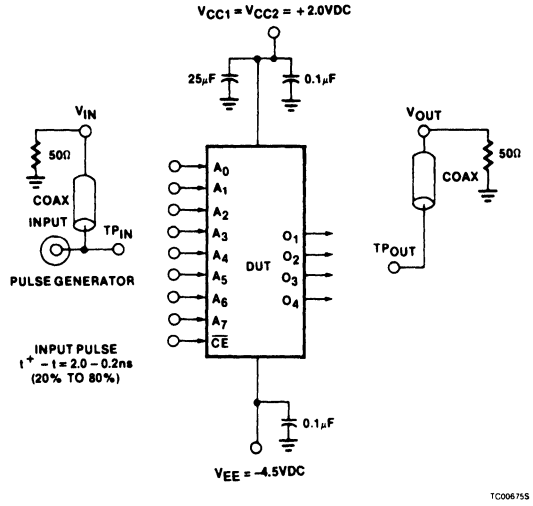
AC ELECTRICAL CHARACTERISTICS $R_1 = 50\Omega$, C_L = 30pF, $0°C \leqslant T_A \leqslant +75°C$, $-4.275V \leqslant V_{EE} \leqslant -4.725V$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[5]	Max	
Access time							
t_{AA}		Output	Address		15	20	ns
t_{CE}		Output	Chip Enable		5	8	ns
Disable time							
t_{CD}		Output	Chip Disable		5	8	ns
Rise and fall time							
t^+	Rise time (20-80%)				4.0		ns
t^-	Fall time (80-20%)				4.0		ns

NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. Each ECL 100K series device has been designed to meet the DC specification after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 400 linear fpm is maintained. Voltage levels will shift approximately 4mV with an air flow of 200 linear fpm. Outputs are terminated through a 50Ω resistor to −2V.
3. For current measurements, maximum is defined as the maximum absolute value.
4. Typical values are at V_{EE} = −4.5V, T_A = +25°C.

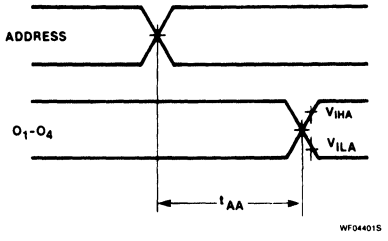
TEST LOAD CIRCUIT



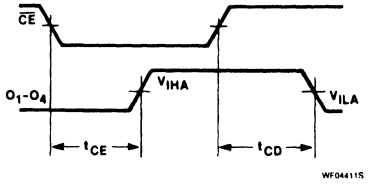
NOTES:

1. For AC tests, all input and output cables to the scope are equal lengths of 50Ω coaxial cable. Wire length should be < ¼ inch from TP_{IN} to input pin and TP_{OUT} to output pin. A 50Ω termination to ground is located in each scope input. Unused outputs are connected to a 50Ω resistor to ground.
2. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
3. Normal practice in test fixtures layout should be followed. Lead lengths, particularly to the power supply, should be as short as possible. A 10μF capacitor between V_{CC1} and V_{CC2} terminals, located as close to the device as possible, is recommended to reduce ringing.

VOLTAGE WAVEFORMS



Address Access Time



Chip Enable/Disable Propagation Delays

10149A
1K-Bit ECL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 10149A is field programmable, meaning that custom patterns are immediately available by following the Generic IV fusing procedure. The device is supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

The 10149A is suitable for use in high-performance ECL systems. The outputs are capable of driving 50Ω loads.

A Chip Enable input is provided for ease of memory expansion.

Ordering information can be found on the following page.

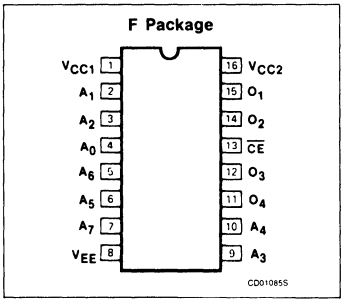
FEATURES

- **Address access time: 10ns max**
- **Power dissipation: 0.66mW/bit typ**
- **High impedance inputs (50kΩ pulldown)**
- **One Chip Enable input**
- **Open Emitter outputs (50Ω drive)**
- **On-chip address decoding**
- **No separate fusing pins**
- **Fully compatible with ECL 10K series**

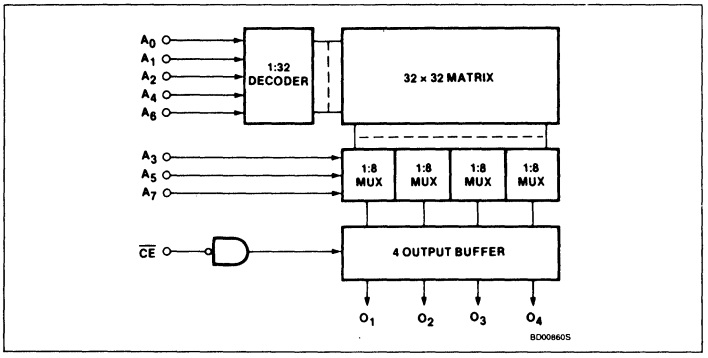
APPLICATIONS

- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-pin Ceramic DIP (300mil-wide)	10149A F

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER[1]	RATING	UNIT
V_{EE}	Supply voltage (V_{CC} = 0)	−8	V_{DC}
V_{IN}	Input voltage (V_{CC} = 0)	0 to V_{EE}	V_{DC}
I_O	Output source current	40	mA_{DC}
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temperature range	−55 to +165	°C

DC ELECTRICAL CHARACTERISTICS $-30°C \leq T_A < +75°C$, $-4.94V \leq V_{EE} \leq -5.46V$

SYMBOL	PARAMETER[1]	TEST CONDITIONS	0°C		+25°C			+75°C		UNIT
			Min	Max	Min	Typ[3]	Max	Min	Max	
Input voltage[2,3]										
V_{IL}	Low		−1.870		−1.850			−1.830		V
V_{IH}	High			−0.840			−0.810		−0.720	V
V_{ILA}	Low threshold			−1.480			−1.475		−1.445	V
V_{IHA}	High threshold		−1.150		−1.105			−1.040		V
Output voltage										
V_{OL}	Low	V_{IH} = Max	−1.870	−1.665	−1.850		−1.650	−1.830	−1.625	V
V_{OH}	High	V_{IL} = Min	−1.000	−0.840	−0.960		−0.810	−0.900	−0.720	V
V_{OLA}	Low threshold	V_{IHA} = Min, V_{ILA} = Max		−1.640			−1.630		−1.600	V
V_{OHA}	High threshold		−1.020		−0.980			−0.920		V
Input current										
I_{IL}	Low	V_{IH} = Max			0.5					μA
I_{IH}	High	V_{IL} = Min		250			250		250	μA
Supply drain current										
I_{EE}		V_{EE} = −5.2V		160		150	160		160	mA

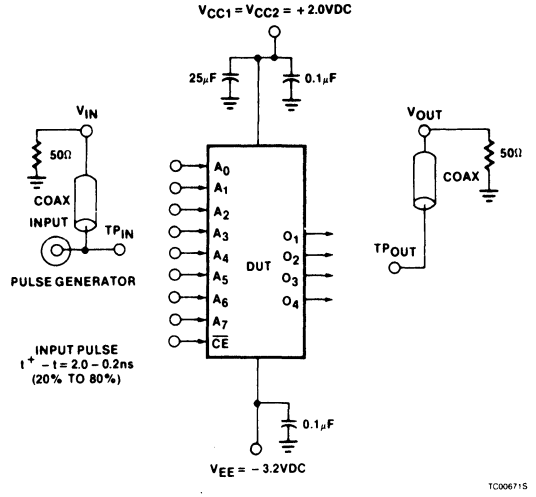
AC ELECTRICAL CHARACTERISTICS $R_1 = 50\Omega$, C_L = 30pF, $0°C \leq T_A \leq +75°C$, $-4.94V \leq V_{EE} \leq -5.46V$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[3]	Max	
Access time							
t_{AA}		Output	Address			10	ns
t_{CE}		Output	Chip enable		4	6	ns
Disable time							
t_{CD}		Output	Chip enable		4	6	ns
Rise and fall time							
t_+	Rise time (20-80%)				4.0		ns
t_-	Fall time (80-20%)				4.0		ns

NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. Each ECL 10K series device has been designed to meet the DC specification after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 4mV with an air flow of 200 linear fpm. Outputs are terminated through a 50Ω resistor to −2V.
3. Typical values are at V_{EE} = −5.2V, T_A = +25°C.

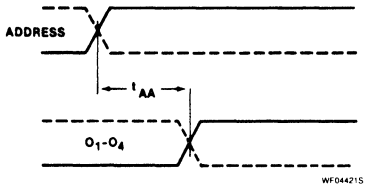
TEST LOAD CIRCUIT



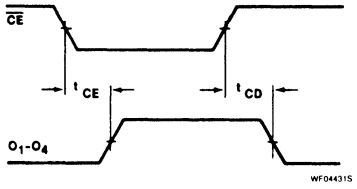
NOTES:

1. For AC tests, all input and output cables to the scope are equal lengths of 50Ω coaxial cable wire length should be < ¼ inch from TP_{IN} to input pin and TP_{OUT} to output pin. A 50Ω termination to ground is located in each scope input. Unused outputs are connected to a 50Ω resistor to ground.
2. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
3. Normal practice in test fixtures layout should be followed. Lead lengths, particularly to the power supply, should be as short as possible. A 10μF capacitor between V_{CC1} and V_{CC2} terminals, located as close to the device as possible, is recommended to reduce ringing.

VOLTAGE WAVEFORMS



Address Access Time



Chip Enable/Disable Propagation Delays

100149A
1K-Bit ECL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 100149A is field programmable, meaning that custom patterns are immediately available by following the ECL fusing procedure. The device is supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

The 100149A is suitable for use in high-performance ECL systems. The outputs are capable of driving 50Ω loads.

A Chip Enable input is provided for ease of memory expansion.

Ordering information can be found on the following page.

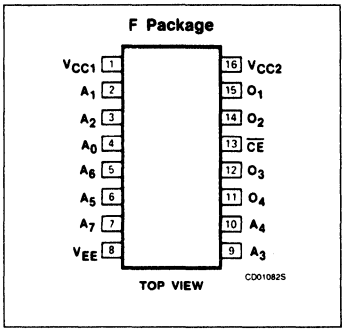
FEATURES

- **Address access time: 10ns max**
- **Power dissipation: 0.66mW/bit typ**
- **High impedance inputs (50kΩ pulldown)**
- **One Chip Enable input**
- **Open Emitter outputs (50Ω drive)**
- **On-chip address decoding**
- **No separate fusing pins**
- **Fully compatible with ECL 100K series**

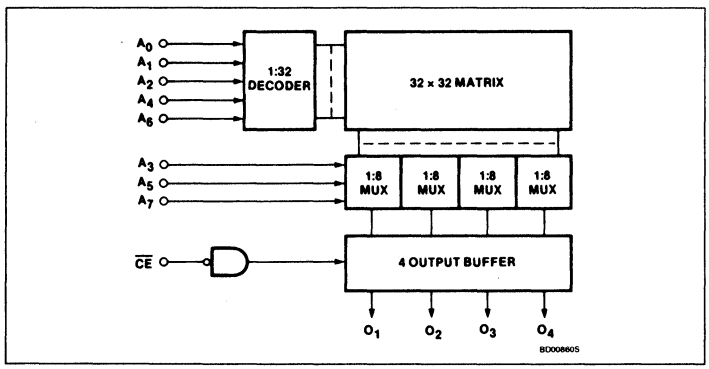
APPLICATIONS

- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-pin Ceramic DIP (300mil-wide)	100149A F

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{EE}	Supply voltage (V_{CC} = 0)	−8	V_{DC}
V_{IN}	Input voltage (V_{CC} = 0)	0 to V_{EE}	V_{DC}
I_O	Output source current	40	mA_{DC}
T_A	Operating temperature range	−0 to +75	°C
T_{STG}	Storage temperature range	−55 to +165	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leqslant T_A \leqslant +75°C$, $-4.275V \leqslant V_{EE} \leqslant -4.725V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[4]	Max	
Input voltage						
V_{IL}	Low		−1.810			
V_{IH}	High				−0.880	V
V_{ILA}	Threshold Low				−1.475	
V_{IHA}	Threshold High		−1.165			
Output voltage						
V_{OL}	Low	V_{IL} = Min	−1.810		−1.620	
V_{OH}	High	V_{IH} = Max	−1.025		−0.880	V
V_{OLA}	Threshold Low	V_{IL} = Max			−1.610	
V_{OHA}	Threshold High	V_{IH} = Min	−1.035			
Input current						
I_{IL}	Low	V_{IL} = Min	0.5			μA
I_{IH}	High	V_{IH} = Max			220	
Supply current						
I_{EE}		V_{EE} = −4.5V		150	160	mA

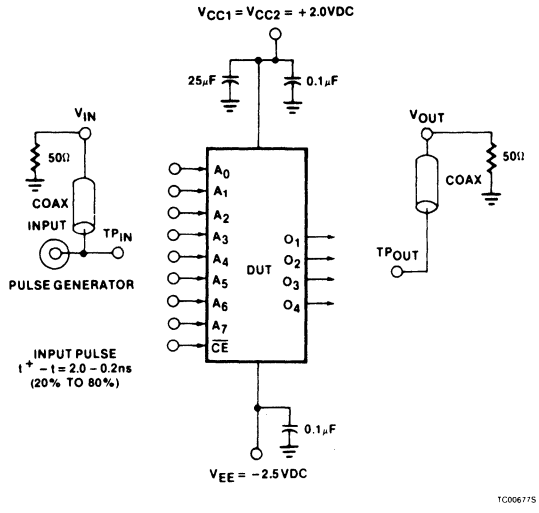
AC ELECTRICAL CHARACTERISTICS $R_1 = 50\Omega$, C_L = 30pF, $0°C \leqslant T_A \leqslant +75°C$, $-4.275V \leqslant V_{EE} \leqslant -4.725V$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[5]	Max	
Access time							
t_{AA}		Output	Address			10	ns
t_{CE}		Output	Chip enable		5	6	
Disable time							
t_{CD}		Output	Chip disable		5	6	ns
Rise and fall time							
t^+	Rise time (20-80%)				4.0		ns
t^-	Fall time (80-20%)				4.0		

NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. Each ECL 100K series device has been designed to meet the DC specification after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 400 linear fpm is maintained. Voltage levels will shift approximately 4mV with an air flow of 200 linear fpm. Outputs are terminated through a 50Ω resistor to −2V.
3. For current measurements, maximum is defined as the maximum absolute value.
4. Typical values are at V_{EE} = −4.5V, T_A = +25°C.

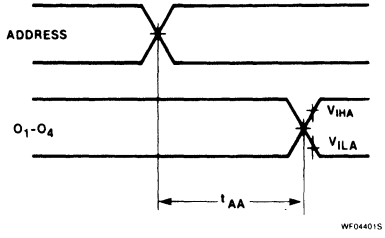
TEST LOAD CIRCUIT



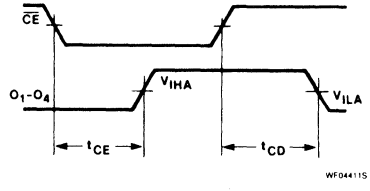
NOTES:

1. For AC tests, all input and output cables to the scope are equal lengths of 50Ω coaxial cable. Wire length should be < ¼ inch from TP_{IN} to input pin and TP_{OUT} to output pin. A 50Ω termination to ground is located in each scope input. Unused outputs are connected to a 50Ω resistor to ground.
2. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
3. Normal practice in test fixtures layout should be followed. Lead lengths, particularly to the power supply, should be as short as possible. A 10μF capacitor between V_{CC1} and V_{CC2} terminals, located as close to the device as possible, is recommended to reduce ringing.

VOLTAGE WAVEFORMS



Address Access Time



Chip Enable/Disable Propagation Delays

10149B

1K–Bit ECL Bipolar PROM

Preliminary Specification

Bipolar Memory Products

DESCRIPTION

The 10149B is field programmable, meaning that custom patterns are immediately available by following the Signetics Generic IV Programming procedure. The device is supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the TiW link matrix.

The 10149B is suitable for use in high–performance ECL systems. The outputs are capable of driving 50Ω loads.

A Chip Enable input is provided for ease of memory expansion.

Ordering information can be found on the following page.

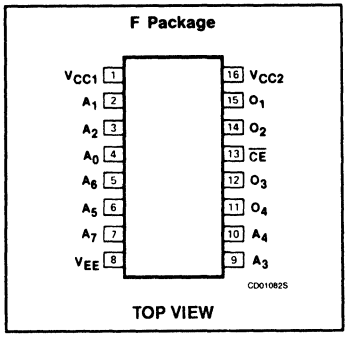
FEATURES

- **Address access time: 5ns max**
- **Power dissipation: 0.76mW/bit typ**
- **High–impedance inputs (50KΩ pulldown)**
- **One Chip Enable input**
- **Open Emitter outputs (50Ω drive)**
- **On–chip address decoding**
- **No separate fusing pins**
- **Fully compatible with ECL 10K series**

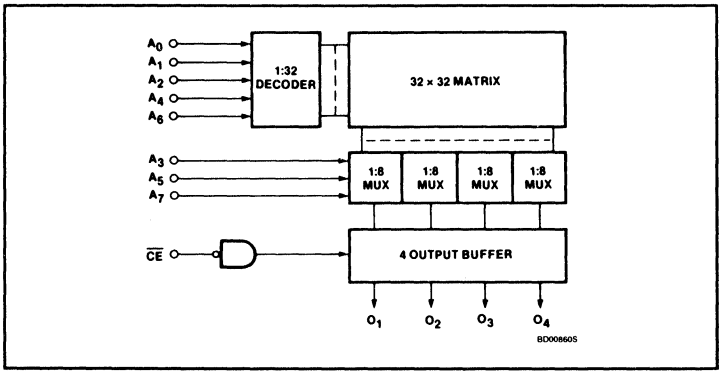
APPLICATIONS

- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATION



BLOCK DIAGRAM



1K–Bit ECL Bipolar PROM (256 × 4) 10149B

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16–pin Ceramic DIP (300mil–wide)	10149B F

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER[1]	RATING	UNIT
V_{EE}	Supply voltage (V_{CC} = 0)	–8	V_{DC}
V_{IN}	Input voltage (V_{CC} = 0)	0 to –3	V_{DC}
I_O	Output source current	40	mA_{DC}
T_A	Operating temperature range	–0 to +75	°C
T_{STG}	Storage temperature range	–55 to +165	°C

NOTES:
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C, -4.94V \leq V_{EE} \leq -5.46V$

			0°C		+25°C			+75°C		
SYMBOL	PARAMETER[1]	TEST CONDITIONS	Min	Max	Min	Typ[3]	Max	Min	Max	UNIT
Input voltage[2,3]										
V_{IL}	Low		–1.870		–1.850			–1.830		V
V_{IH}	High			–0.840			–0.810		–0.720	V
V_{ILA}	Low threshold			–1.480			–1.475		–1.445	V
V_{IHA}	High threshold		–1.150		–1.105			–1.040		V
Output voltage										
V_{OL}	Low	V_{IH} = Max	–1.870	–1.665	–1.850		–1.650	–1.830	–1.625	V
V_{OH}	High	V_{IL} = Min	–1.000	–0.840	–0.960		–0.810	–0.900	–0.720	V
V_{OLA}	Low threshold	V_{IHA} = Min, V_{ILA} = Max		–1.640			–1.630		–1.600	V
V_{OHA}	High threshold	V_{IHA} = Min, V_{ILA} = Max	–1.020		–0.980			–0.920		V
Input current[4]										
I_{IL}	Low	V_{IH} = Max			0.5					µA
I_{IH}	High	V_{IL} = Min		250			250		250	µA
Supply drain current										
I_{EE}		V_{EE} = –5.2V		160		150	160		160	mA

NOTES:
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. Each ECL 10K series device has been designed to meet the DC specification after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 4mV with an air flow of 200 linear fpm. Outputs are terminated through a 50Ω resistor to –2V.
3. Typical values are at V_{EE} = –5.2V, T_A = +25°C.
4. Unused input pins must have 10KΩ min to V_{EE} or be connected to $-2V_{DC}$.

1K–Bit ECL Bipolar PROM (256 × 4) 10149B

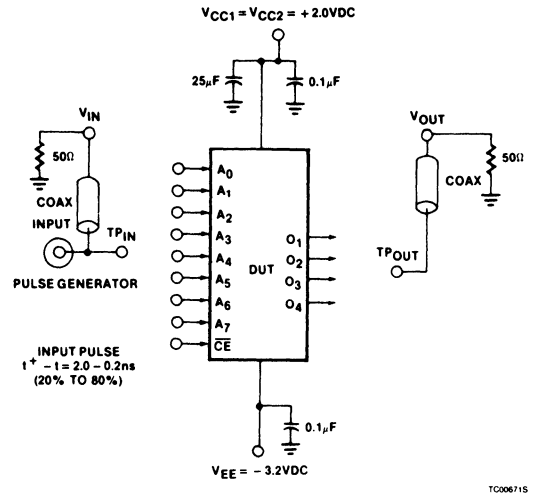
AC ELECTRICAL CHARACTERISTICS $R_1 = 50\Omega$, $0°C \leq T_A \leq +75°C$, $-4.94V \leq V_{EE} \leq -5.46V$

SYMBOL	PARAMETER	TO	FROM	LIMITS Min	LIMITS Typ[1]	LIMITS Max	UNIT
Access time							
t_{AA}		Output	Address			5	ns
t_{CE}		Output	Chip Enable		2	3	ns
Disable time							
t_{CD}		Output	Chip Disable		2	3	ns
Rise and fall time							
t_+	Rise time (20–80%)				2.0		ns
t_-	Fall time (80–20%)				2.0		ns

NOTE:

1. Typical values are at $V_{EE} = -5.2V$, $T_A = +25°C$.

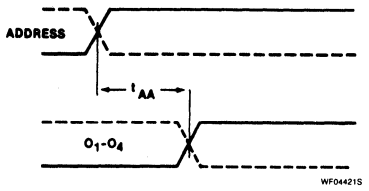
TEST LOAD CIRCUITS



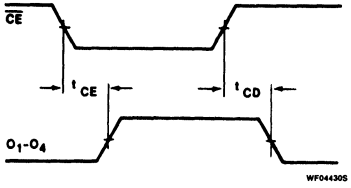
NOTES:

1. For AC tests, all input and output cables to the scope are equal lengths of 50Ω coaxial cable wire length should be < ¼ inch from TP_{IN} to input pin and TP_{OUT} to output pin. A 50Ω termination to ground is located in each scope input. Unused outputs are connected to a 50Ω resistor to ground.
2. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
3. Normal practice in test fixtures layout should be followed. Lead lengths, particularly to the power supply, should be as short as possible. A 10μF capacitor between V_{CC1} and V_{CC2} terminals, located as close to the device as possible, is recommended to reduce ringing.

VOLTAGE WAVEFORMS



Address Access Time



Chip Enable/Disable Propagation Delays

100149B
1K–Bit ECL Bipolar PROM

Preliminary Specification

Bipolar Memory Products

DESCRIPTION

The 100149B is field programmable, meaning that custom patterns are immediately available by following the Signetics Generic IV Programming procedure. The device is supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the TiW link matrix.

The 100149B is suitable for use in high–performance ECL systems. The outputs are capable of driving 50Ω loads.

A Chip Enable input is provided for ease of memory expansion.

Ordering information can be found on the following page.

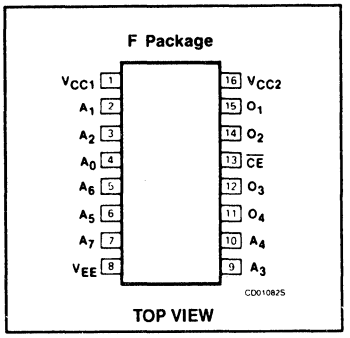
FEATURES

- **Address access time: 5ns max**
- **Power dissipation: 0.66mW/bit typ**
- **High–impedance inputs (50KΩ pulldown)**
- **One Chip Enable input**
- **Open Emitter outputs (50Ω drive)**
- **On–chip address decoding**
- **No separate fusing pins**
- **Fully compatible with ECL 100K series**

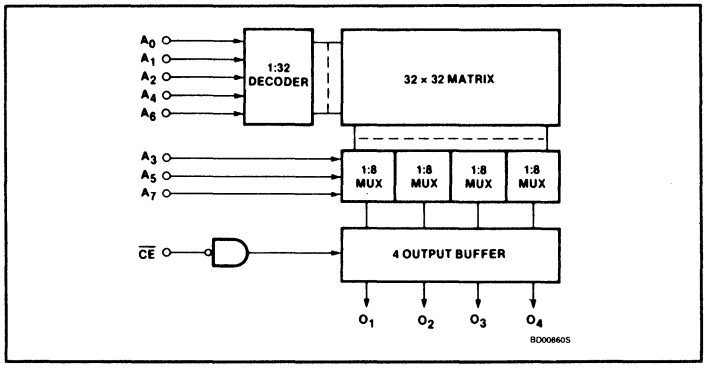
APPLICATIONS

- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATION



BLOCK DIAGRAM



1K–Bit ECL Bipolar PROM (256 × 4) 100149B

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16–pin Ceramic DIP (300mil–wide)	100149B F

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{EE}	Supply voltage (V_{CC} = 0)	–8	V_{DC}
V_{IN}	Input voltage (V_{CC} = 0)	0 to –3	V_{DC}
I_O	Output source current	40	mA_{DC}
T_A	Operating temperature range	–0 to +75	°C
T_{STG}	Storage temperature range	–55 to +165	°C

DC ELECTRICAL CHARACTERISTICS 0°C ≤ T_A ≤ +75°C, –4.275V ≤ V_{EE} ≤ –4.725V

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[4]	Max	
Input voltage						
V_{IL}	Low		–1.810			V
V_{IH}	High				–0.880	V
V_{ILA}	Threshold Low				–1.475	V
V_{IHA}	Threshold High		–1.165			V
Output voltage						
V_{OL}	Low	V_{IL} = Min	–1.810		–1.620	V
V_{OH}	High	V_{IH} = Max	–1.025		–0.880	V
V_{OLA}	Threshold Low	V_{IL} = Max			–1.610	V
V_{OHA}	Threshold High	V_{IH} = Min	–1.035			V
Input current[5]						
I_{IL}	Low	V_{IL} = Min	0.5			µA
I_{IH}	High	V_{IH} = Max			220	µA
Supply current						
I_{EE}		V_{EE} = –4.5V		150	160	mA

NOTES:
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. Each ECL 100K series device has been designed to meet the DC specification after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 400 linear fpm is maintained. Voltage levels will shift approximately 4mV with an air flow of 200 linear fpm. Outputs are terminated through a 50Ω resistor to –2V.
3. For current measurements, maximum is defined as the maximum absolute value.
4. Typical values are at V_{EE} = –4.5V, T_A = +25°C.
5. Unused inputs must have 10KΩ minimum to V_{EE} or be connected to $-2V_{DC}$.

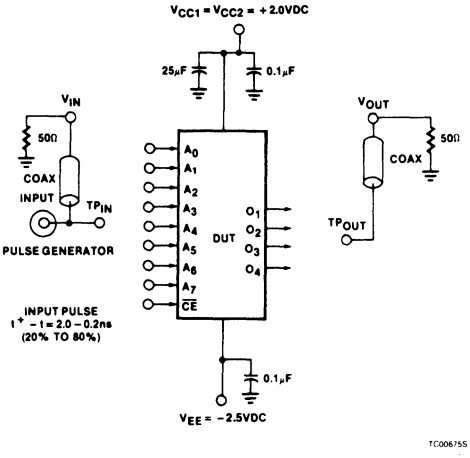
AC ELECTRICAL CHARACTERISTICS $R_1 = 50\Omega$, $0°C \leq T_A \leq +75°C$, $-4.275V \leq V_{EE} \leq -4.725V$

SYMBOL	PARAMETER	TO	FROM	LIMITS Min	LIMITS Typ[1]	LIMITS Max	UNIT
Access time							
t_{AA}		Output	Address			5	ns
t_{CE}		Output	Chip Enable		2	3	ns
Disable time							
t_{CD}		Output	Chip Disable		2	3	ns
Rise and fall time							
t^+	Rise time (20–80%)				2.0		ns
t^-	Fall time (80–20%)				2.0		ns

NOTES:

1. Typical values are at $V_{EE} = -4.5V$, $T_A = +25°C$.

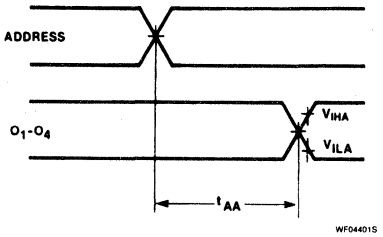
TEST LOAD CIRCUIT



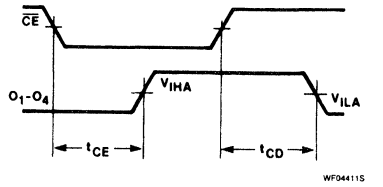
NOTES:

1. For AC tests, all input and output cables to the scope are equal lengths of 50Ω coaxial cable. Wire length should be < ¼ inch from TP_{IN} to input pin and TP_{OUT} to output pin. A 50Ω termination to ground is located in each scope input. Unused outputs are connected to a 50Ω resistor to ground.
2. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
3. Normal practice in test fixtures layout should be followed. Lead lengths, particularly to the power supply, should be as short as possible. A 10μF capacitor between V_{CC1} and V_{CC2} terminals, located as close to the device as possible, is recommended to reduce ringing.

VOLTAGE WAVEFORMS



Address Access Time



Chip Enable/Disable Propagation Delays

16K-bit ECL PROM

		page
10P016	**16 384-bit ECL Bipolar PROM (4096 x 4) 10 ns**	**529**
100P016	**16 384-bit ECL Bipolar PROM (4096 x 4) 10 ns**	**533**

10P016

16K–Bit ECL Bipolar PROM

Objective Specification

Bipolar Memory Products

DESCRIPTION

The 10P016 is field programmable, meaning that custom patterns are immediately available by following the Signetics Generic IV Programming procedure. The device is supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the TiW link matrix.

The 10P016 is suitable for use in high–performance ECL systems. The outputs are capable of driving 50Ω loads.

A Chip Enable input is provided for ease of memory expansion.

Ordering information can be found on the following page.

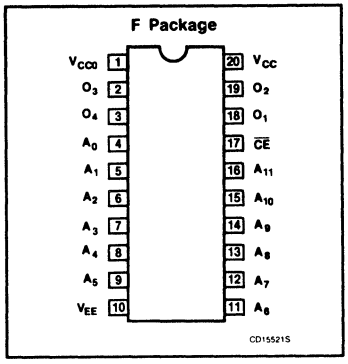
FEATURES

- **Address access time: 10ns max**
- **Power dissipation: 57μW/bit typ**
- **High–impedance inputs (50KΩ pulldown)**
- **One Chip Enable input**
- **Open Emitter outputs (50Ω drive)**
- **On–chip address decoding**
- **No separate fusing pins**
- **Fully compatible with ECL 10K series**

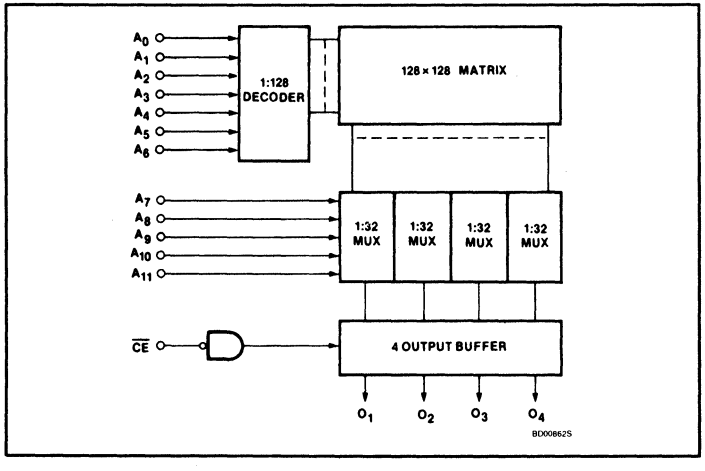
APPLICATIONS

- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATION



BLOCK DIAGRAM



16K–Bit ECL Bipolar PROM (4096 × 4)

10P016

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
20–pin Ceramic DIP (300mil–wide)	10P016 F

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER[1]	RATING	UNIT
V_{EE}	Supply voltage (V_{CC} = 0)	–8	V_{DC}
V_{IN}	Input voltage (V_{CC} = 0)	0 to –3	V_{DC}
I_O	Output source current	40	mA
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temperature range	–55 to +165	°C

NOTE:
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A < +75°C, -4.94V \leq V_{EE} \leq -5.46V$

			0°C		+25°C			+75°C		
SYMBOL	PARAMETER[1]	TEST CONDITIONS	Min	Max	Min	Typ[3]	Max	Min	Max	UNIT
Input voltage[2,3]										
V_{IL}	Low		–1.870		–1.850			–1.830		V
V_{IH}	High			–0.840			–0.810		–0.720	V
V_{ILA}	Low threshold			–1.480			–1.475		–1.445	V
V_{IHA}	High threshold		–1.150		–1.105			–1.040		V
Output voltage										
V_{OL}	Low	V_{IH} = Max	–1.870	–1.665	–1.850		–1.650	–1.830	–1.625	V
V_{OH}	High	V_{IL} = Min	–1.000	–0.840	–0.960		–0.810	–0.900	–0.720	V
V_{OLA}	Low threshold	V_{IHA} = Min, V_{ILA} = Max		–1.640			–1.630		–1.600	V
V_{OHA}	High threshold	V_{IHA} = Min, V_{ILA} = Max	–1.020		–0.980			–0.920		V
Input current[4]										
I_{IL}	Low	V_{IH} = Max			0.5					µA
I_{IH}	High	V_{IL} = Min		250			250		250	µA
Supply drain current										
I_{EE}		V_{EE} = –5.2V		200		180	200		200	mA

NOTE:
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. Each ECL 10K series device has been designed to meet the DC specification after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 4mV with an air flow of 200 linear fpm. Outputs are terminated through a 50Ω resistor to –2V.
3. Typical values are at V_{EE} = –5.2V, T_A = +25°C.
4. Unused inputs must have 10KΩ min to V_{EE} or be connected to $-2V_{DC}$.

16K–Bit ECL Bipolar PROM (4096 × 4)

10P016

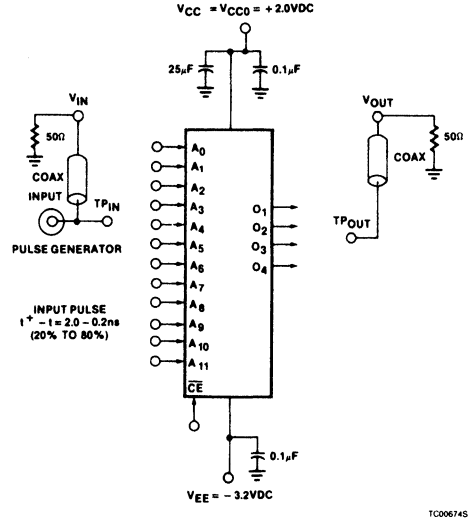
AC ELECTRICAL CHARACTERISTICS $R_1 = 50\Omega$, $0°C \leq T_A \leq +75°C$, $-4.94V \leq V_{EE} \leq -5.46V$

SYMBOL	PARAMETER	TO	FROM	LIMITS Min	LIMITS Typ[1]	LIMITS Max	UNIT
Access time							
t_{AA}		Output	Address		6	10	ns
t_{CE}		Output	Chip Enable		2	5	ns
Disable time							
t_{CD}		Output	Chip Disable		2	5	ns
Rise and fall time							
t_+	Rise time (20–80%)				1.0		ns
t_-	Fall time (80–20%)				1.0		ns

NOTE:

1. Typical values are at $V_{EE} = -5.2V$, $T_A = +25°C$.

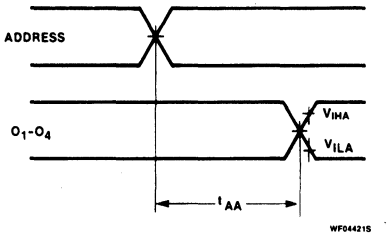
TEST LOAD CIRCUIT



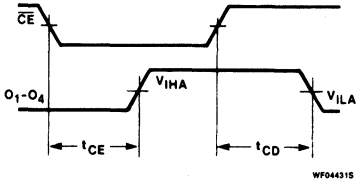
NOTES:

1. For AC tests, all input and output cables to the scope are equal lengths of 50Ω coaxial cable. Wire length should be < ¼ inch from TP_{IN} to input pin and TP_{OUT} to output pin. A 50Ω termination to ground is located in each scope input. Unused outputs are connected to a 50Ω resistor to ground.
2. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
3. Normal practice in test fixtures layout should be followed. Lead lengths, particularly to the power supply, should be as short as possible. A 10μF capacitor between V_{CC} and V_{CCO} terminals, located as close to the device as possible, is recommended to reduce ringing.

VOLTAGE WAVEFORMS



Address Access Time



Chip Enable/Disable Propagation Delays

100P016
16K–Bit ECL Bipolar PROM

Objective Specification

Bipolar Memory Products

DESCRIPTION

The 100P016 is field programmable, meaning that custom patterns are immediately available by following the Signetics Generic IV Programming procedure. The device is supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the TiW link matrix.

The 100P016 is suitable for use in high–performance ECL systems. The outputs are capable of driving 50Ω loads.

A Chip Enable input is provided for ease of memory expansion.

Ordering information can be found on the following page.

FEATURES

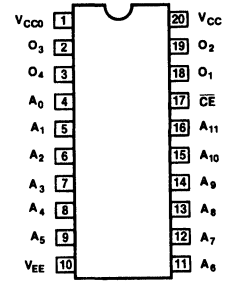
- **Address access time: 10ns max**
- **Power dissipation: 49μW/bit typ**
- **High–impedance inputs (50KΩ pulldown)**
- **One Chip Enable input**
- **Open Emitter outputs (50Ω drive)**
- **On–chip address decoding**
- **No separate fusing pins**
- **Fully compatible with ECL 100K series**

APPLICATIONS

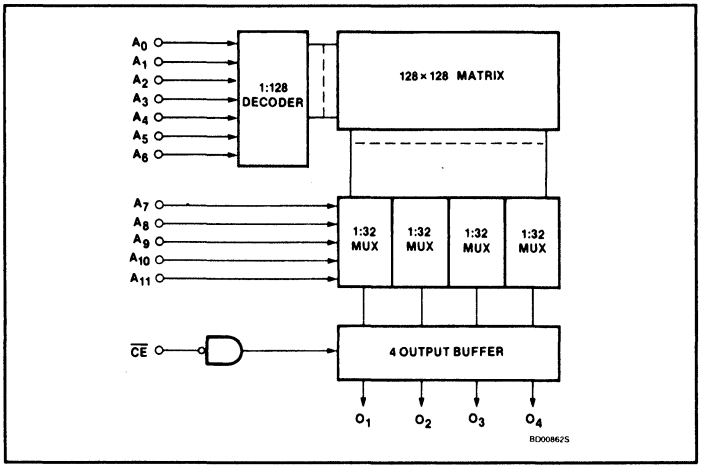
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATION

F Package



BLOCK DIAGRAM



16K–Bit ECL Bipolar PROM (4096 × 4) 100P016

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
20–pin Ceramic DIP (300mil–wide)	100P016 F

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{EE}	Supply voltage (V_{CC} = 0)	–8	V_{DC}
V_{IN}	Input voltage (V_{CC} = 0)	0 to –3	V_{DC}
I_O	Output source current	40	mA
T_A	Operating temperature range	–0 to +75	°C
T_{STG}	Storage temperature range	–55 to +165	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C, -4.275V \leq V_{EE} \leq -4.725V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[4]	Max	
Input voltage						
V_{IL}	Low		–1.810			V
V_{IH}	High				–0.880	V
V_{ILA}	Threshold Low				–1.475	V
V_{IHA}	Threshold High		–1.165			V
Output voltage						
V_{OL}	Low	V_{IL} = Min	–1.810		–1.620	V
V_{OH}	High	V_{IH} = Max	–1.025		–0.880	V
V_{OLA}	Threshold Low	V_{IL} = Max			–1.610	V
V_{OHA}	Threshold High	V_{IH} = Min	–1.035			V
Input current[5]						
I_{IL}	Low	V_{IL} = Min	0.5			µA
I_{IH}	High	V_{IH} = Max			220	µA
Supply current						
I_{EE}		V_{EE} = –4.5V		180	200	mA

NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. Each ECL 100K series device has been designed to meet the DC specification after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 400 linear fpm is maintained. Voltage levels will shift approximately 4mV with an air flow of 200 linear fpm. Outputs are terminated through a 50Ω resistor to –2V.
3. For current measurements, maximum is defined as the maximum absolute value.
4. Typical values are at V_{EE} = –4.5V, T_A = +25°C.
5. Unused inputs must have 10KΩ min to V_{EE} or be connected to $-2V_{DC}$.

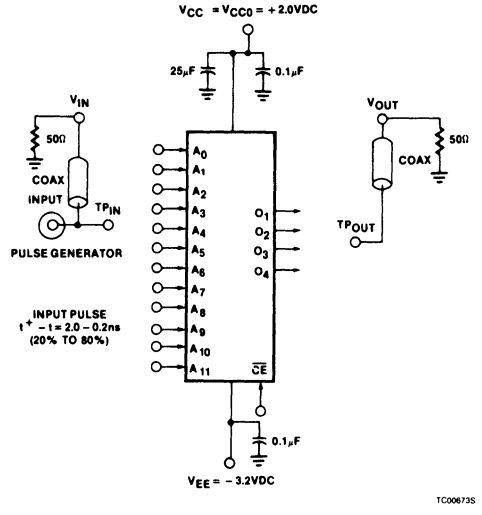
16K–Bit ECL Bipolar PROM (4096 × 4) 100P016

AC ELECTRICAL CHARACTERISTICS $R_1 = 50\Omega$, $0°C \leq T_A \leq +75°C$, $-4.275V \leq V_{EE} \leq -4.725V$

SYMBOL	PARAMETER	TO	FROM	LIMITS Min	LIMITS Typ[1]	LIMITS Max	UNIT
Access time							
t_{AA}		Output	Address		6	10	ns
t_{CE}		Output	Chip Enable		2	5	ns
Disable time							
t_{CD}		Output	Chip Disable		2	5	ns
Rise and fall time							
t^+	Rise time (20–80%)				1.0		ns
t^-	Fall time (80–20%)				1.0		ns

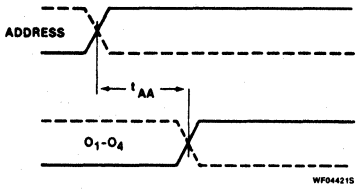
NOTE:
1. Typical values are at $V_{EE} = -4.5V$, $T_A = +25°C$.

TEST LOAD CIRCUIT

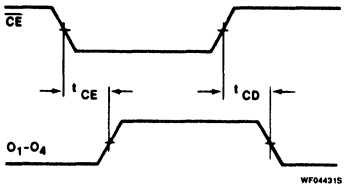


NOTES:
1. For AC tests, all input and output cables to the scope are equal lengths of 50Ω coaxial cable wire length should be < ¼ inch from TP_{IN} to input pin and TP_{OUT} to output pin. A 50Ω termination to ground is located in each scope input. Unused outputs are connected to a 50Ω resistor to ground.
2. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
3. Normal practice in test fixtures layout should be followed. Lead lengths, particularly to the power supply, should be as short as possible. A 10μF capacitor between V_{CC} and V_{CCO} terminals, located as close to the device as possible, is recommended to reduce ringing.

VOLTAGE WAVEFORMS



Address Access Time



Chip Enable/Disable Propagation Delays

PACKAGE INFORMATION

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Package outlines for product with prefixes: FCB, PCA, PCD, PCF
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PACKAGE OUTLINES

page

Introduction **541**
Plastic Leaded Chip Carrier **543**
Plastic Small Outline **545**
Ceramic DIP **547**
Plastic DIP **551**

Package Outlines

Bipolar Memory Products

INTRODUCTION

The following information applies to packages currently used for Memories. For information on other package configurations, refer to the respective Data Manual for each product.

GENERAL

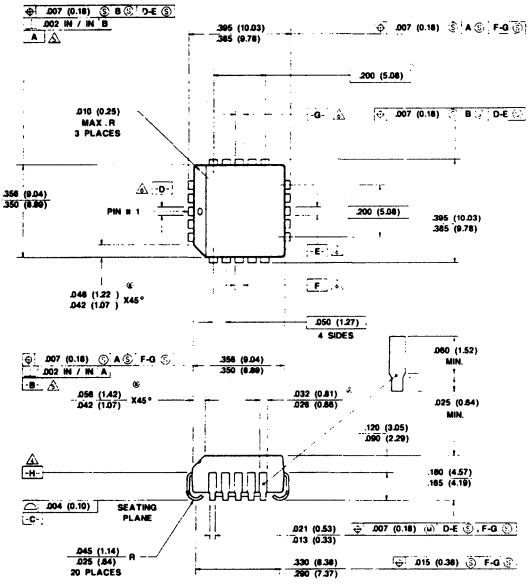
1. The following pages contain information on plastic DIP and CERDIP packages ranging from 16 pins to 28 pins, SOLs 16 to 20-pin, and Plastic Leaded Chip Carriers from 20 pins to 32 pins.
2. Information for each package such as notes and reference standards are included on each drawing for easy reference.
3. Thermal resistance values have been determined by utilizing the linear temperature dependence of the forward voltage drop across the substrate diode in a digital device to monitor the junction temperature rise during known power application across V_{CC} and ground. Since thermal resistance values are dependent on die size and the value of power dissipated, measurements were made on packages containing various die sizes. The information in the tables shown here are typical values for a mid memory die size for a given package. For more detailed information on thermal performance of specific packages please contact your Signetics sales representative and request the latest publication of Thermal Performance Data published by Signetics Corporate Package Engineering.

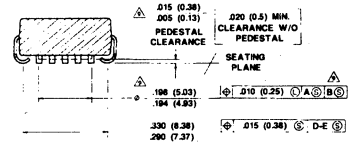
PLASTIC LEADED CHIP CARRIER (PLCC)

NO. OF LEADS	PACKAGE CODE	θ_{JA}/θ_{JC}	DESCRIPTION
20	A	72/31	350mil-square
28	A	60/24	450mil-square
32	A	58/18	450 × 550mil-rectangular

1. Lead material: Olin 194 (Copper Alloy) or equivalent, solder dipped.
2. Body material: Plastic (Epoxy).
3. Thermal test Fixture: Device soldered to a glass epoxy test board with the dimensions 1.58" × 0.75" × 0.059" with 0.009" stand off.

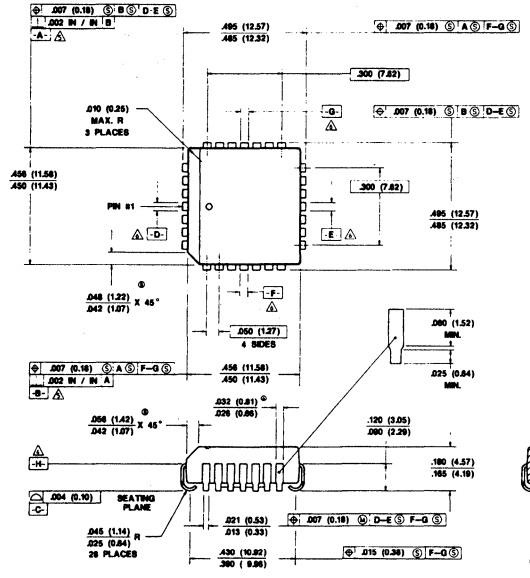
20-PIN PLASTIC LEADED CHIP CARRIER





NOTES:
1. Package dimensions conform to JEDEC specification MO-047-AA for plastic leaded chip carrier 20 leads, .050 inch lead spacing, square. (issue A, 10/31/84).
2. Controlling dimensions: inches. Metric dimensions in mm are shown in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M-1982.
4. Datum plane "H" located at the top of mold parting line and coincident with top of lead. Where lead exists plastic body.
5. Location to datum "A" and "B" to be determined at plane "H". These datums do not include mold flash. Mold flash protrusion shall not exceed .006" (0.15mm) on any side.
6. Datum "D-E" and "F-G" are determined where these center leads exit from the body at plane "H".
7. Pin numbers continue counterclockwise to pin #20 (top view).
8. Signetics order code for product packaged in a PLCC is the suffix "A" after the product number.
9. Applicable to packages with pedestal only.

28-PIN PLASTIC LEADED CHIP CARRIER

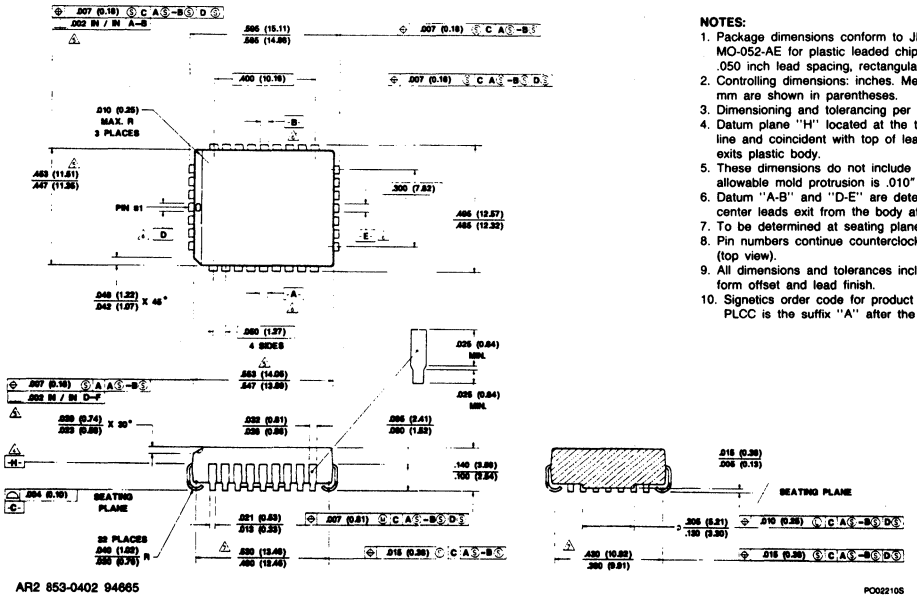


AQ1 853-0401 93885

PO02200S

NOTES:
1. Package dimensions conform to JEDEC specification MO-047-AB for plastic leaded chip carrier 28 leads, .050 inch lead spacing, square. (issue A, 10/31/84).
2. Controlling dimensions: inches. Metric dimensions in mm are shown in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M-1982.
4. Datum plane "H" located at the top of mold parting line and coincident with top of lead. Where lead exits plastic body.
5. Location to datum "A" and "B" to be determined at plane "H". These Datums do not include mold flash. Mold flash protrusion shall not exceed .006" (0.15 mm) on any side.
6. Datum "D-E" and "F-G" are determined where these center leads exit from the body at plane "H".
7. Pin numbers continue counterclockwise to pin #28 (top view).
8. Signetics order code for product packaged in a PLCC is the suffix "A" after the product number.
9. Applicable to packages with pedestal only.

32-PIN PLASTIC LEADED CHIP CARRIER



AR2 853-0402 94665

PO02210S

NOTES:
1. Package dimensions conform to JEDEC specification MO-052-AE for plastic leaded chip carrier 32 leads, .050 inch lead spacing, rectangular. (issue A, 8/1/85).
2. Controlling dimensions: inches. Metric dimensions in mm are shown in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M-1982.
4. Datum plane "H" located at the top of mold parting line and coincident with top of lead, where leads exits plastic body.
5. These dimensions do not include mold protrusion. allowable mold protrusion is .010" (.254 mm).
6. Datum "A-B" and "D-E" are determined where these center leads exit from the body at plane "H".
7. To be determined at seating plane "C".
8. Pin numbers continue counterclockwise to pin #32 (top view).
9. All dimensions and tolerances include lead trim and form offset and lead finish.
10. Signetics order code for product packaged in a PLCC is the suffix "A" after the product number.

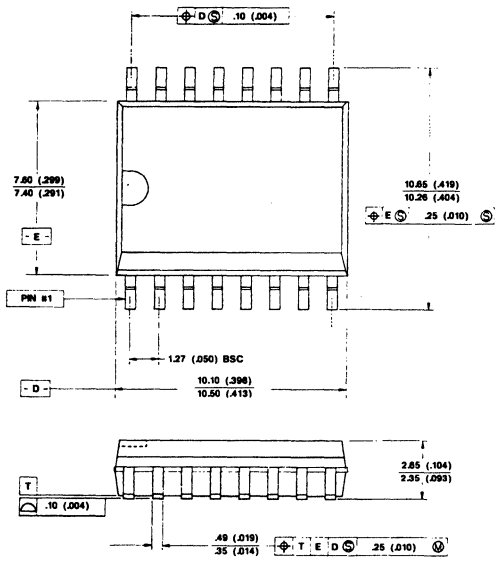
Package Outlines

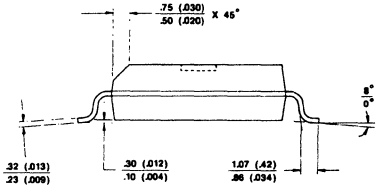
PLASTIC SMALL OUTLINE PACKAGES (SOL)

NO. OF LEADS	PACKAGE CODE	θ_{JA}/θ_{JC}	DESCRIPTION
16	D	95/27	300mil-wide
20	D	86/23	300mil-wide

1. Lead material: Olin 194 (Copper Alloy) or equivalent, solder dipped.
2. Body material: Plastic (Epoxy).
3. Thermal test fixture: Device soldered to a glass epoxy test board with the dimensions of 1.58" × 0.75" × 0.059" with 0.009" stand off.

16-PIN PLASTIC SMALL OUTLINE (SOL)



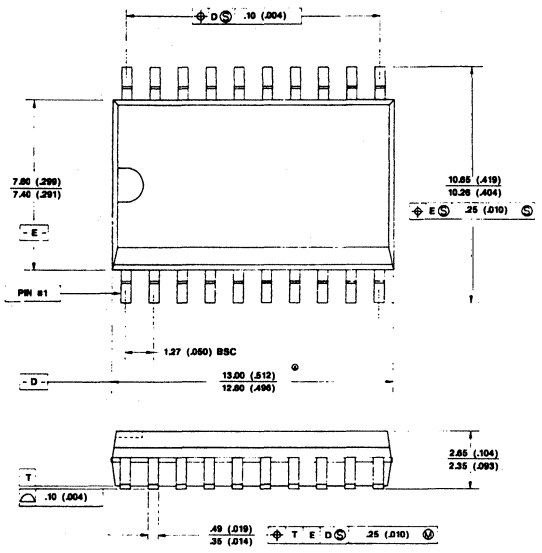


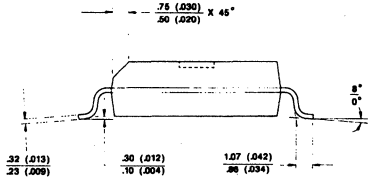
DJ2 853-0171 81218

P002290S

NOTES:
1. Package dimensions conform to JEDEC specification MS-013-AA for standard small outline (SO) package, 16 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

20-PIN PLASTIC SMALL OUTLINE (SOL)





NOTES:

1. Package dimensions conform to JEDEC specification MS-013-AC for standard small outline (SO) package, 20 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #20 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

DL2 853-0172 82948

PO02350S

Package Outlines

CERAMIC DUAL-IN-LINE PACKAGES

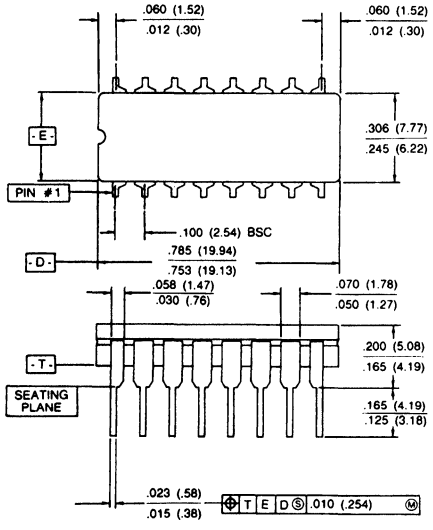
NO. OF LEADS	PACKAGE CODE	θ_{JA}/θ_{JC}	DESCRIPTION
16	F	77/12	300mil-wide
18	F	73/9	300mil-wide
20	F	72/8	300mil-wide
22	F	66/7	400mil-wide
24	F, F3[1]	63/6	300mil-wide
24	F, FA	62/5	600mil-wide
28	F, FA	45/5	600mil-wide

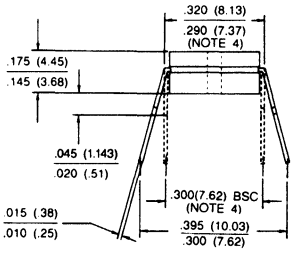
NOTES:
1. Order coded as F3 when both 600 and 300mil-wide packages are available.

CERDIP

1. Lead material: ASTM alloy F-30 (Alloy 42) or equivalent – tin plated or solder dipped.
2. Body Material: Ceramic with glass seal at leads.
3. Thermal test fixture: Device secured in Textool ZIF socket with 0.04" stand off.

16-PIN HERMETIC CERDIP





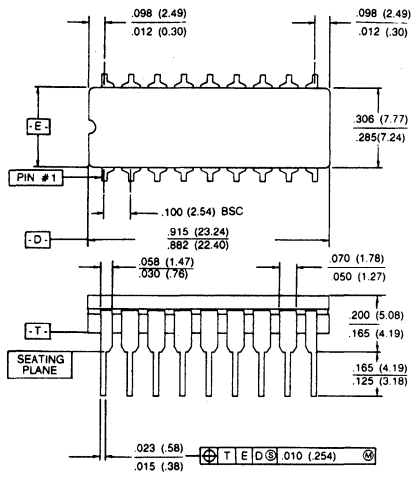
NOTES:
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M – 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from the top.

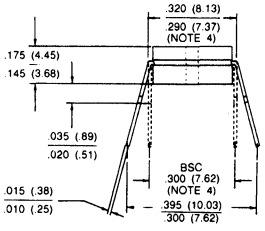
FJ1 853-0582 88375

PO00491S

Package Outlines

18-PIN HERMETIC CERDIP



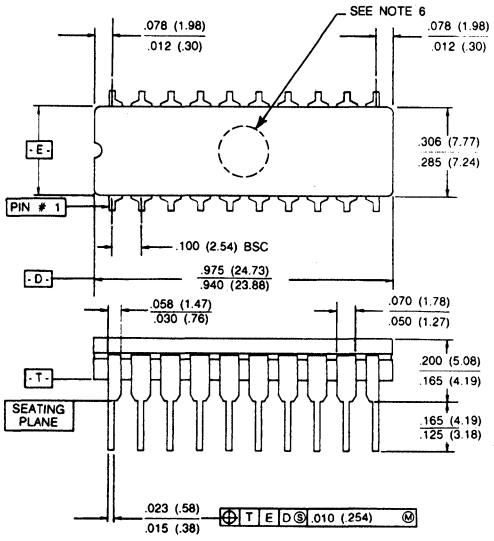


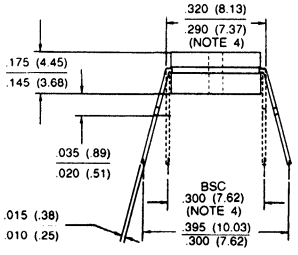
NOTES:
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M - 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #18 when viewed from the top.

FK1 853-0583 81594

PO00470S

20-PIN HERMETIC CERDIP





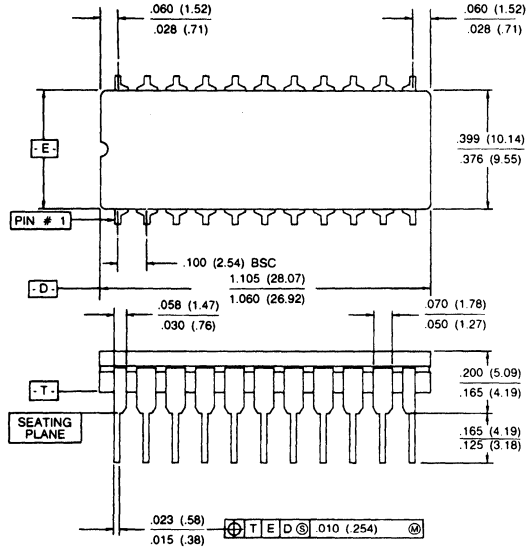
NOTES:
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M - 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #20 when viewed from the top.
6. Denotes window location for EPROM products.

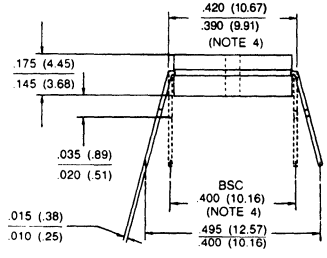
FL1 853-0584 88099

PO00431S

Package Outlines

22-PIN HERMETIC CERDIP



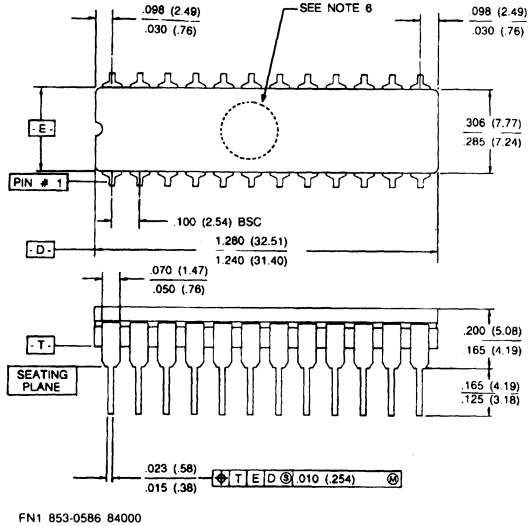


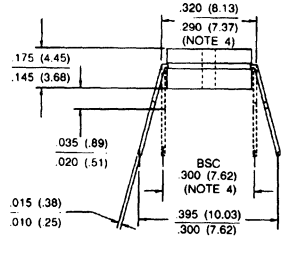
NOTES:
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M - 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #22 when viewed from the top.

FM2 853-0585 88274

PO00421S

24-PIN HERMETIC CERDIP (300mil-wide)





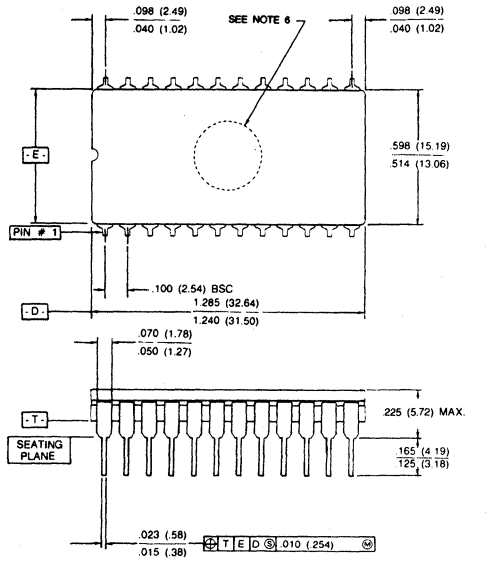
NOTES:
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M - 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #24 when viewed from the top.
6. Denotes window location for EPROM products.

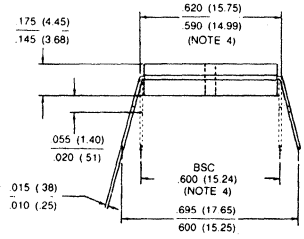
FN1 853-0586 84000

PO00402S

Package Outlines

24-PIN HERMETIC CERDIP (600mil-wide)



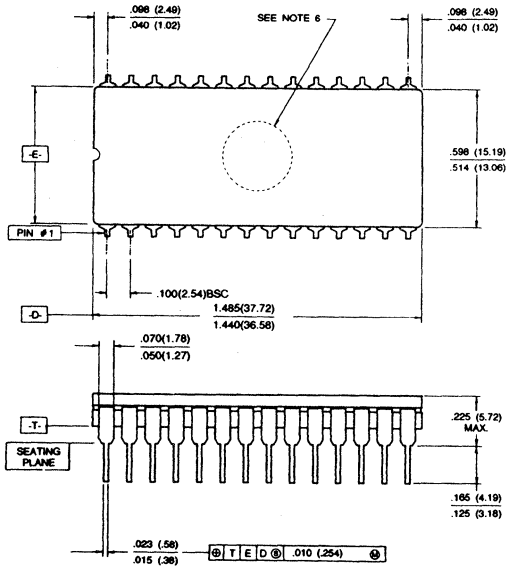


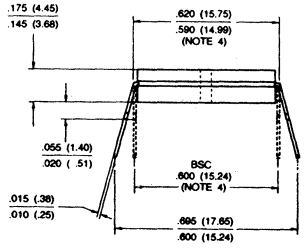
NOTES:
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M - 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #24 when viewed from the top.
6. Denotes window location for EPROM products.

FN3 853-0588 84221

PO00464S

28-PIN CERDIP (600mil-wide)





NOTES:
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M - 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #28 when viewed from the top.
6. Denotes window location for EPROM products.

FQ3 853-0589 84000

PO00660S

Package Outlines

PLASTIC DUAL-IN-LINE PACKAGES

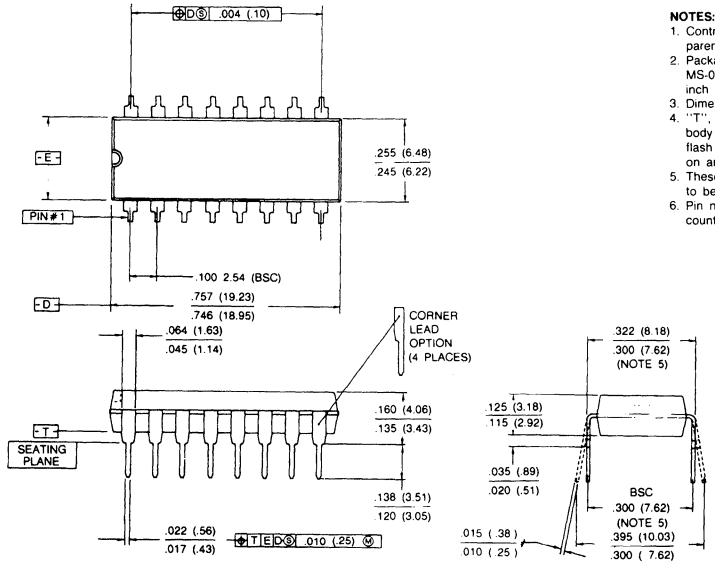
NO. OF LEADS	PACKAGE CODE	θ_{JA}/θ_{JC}	DESCRIPTION
16	N	76/26	300mil-wide
18	N	63/24	300mil-wide
20	N	60/24	300mil-wide
22	N	56/21	400mil-wide
24	N/N3[1]	52/20	300mil-wide
24	N	44/18	600mil-wide
28	N	42/16	600mil-wide

NOTES:
1. Order coded as N3 when both 600mil and 300mil-wide packages are available.

PLASTIC DIP

1. Lead material: Olin 194 (Copper Alloy) or equivalent, solder dipped.
2. Body material: Plastic (Epoxy).
3. Thermal test fixture: Device secured in a Textool ZIF socket with 0.04" stand off.

16-PIN PLASTIC DUAL IN-LINE (PDIP)



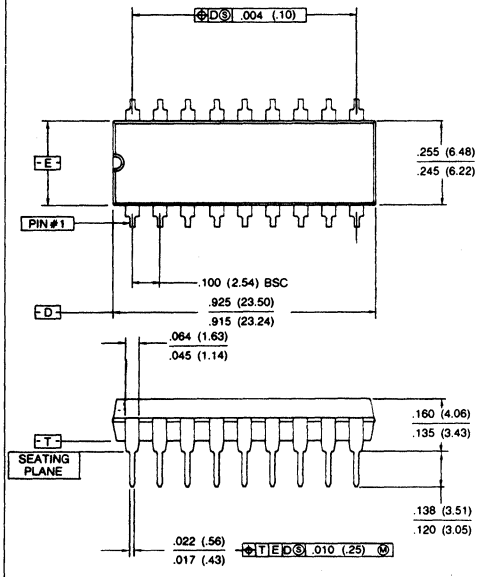
NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AA for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 16 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from the top.

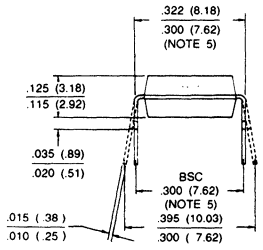
NJ1 853-0406 81232

PO00280S

Package Outlines

18-PIN PLASTIC DUAL IN-LINE (PDIP)



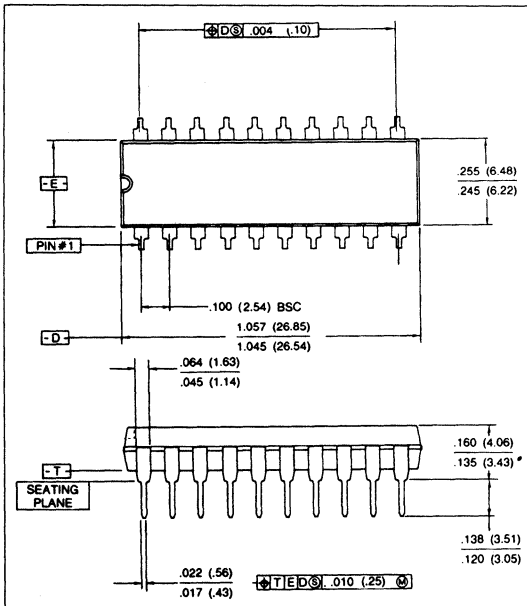


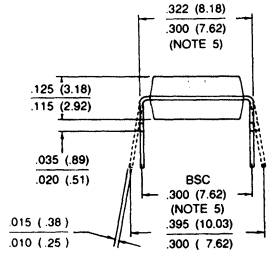
NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AD for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 18 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #18 when viewed from the top.

NK1 853-0407 81233

PO00300S

20-PIN PLASTIC DUAL IN-LINE (PDIP)



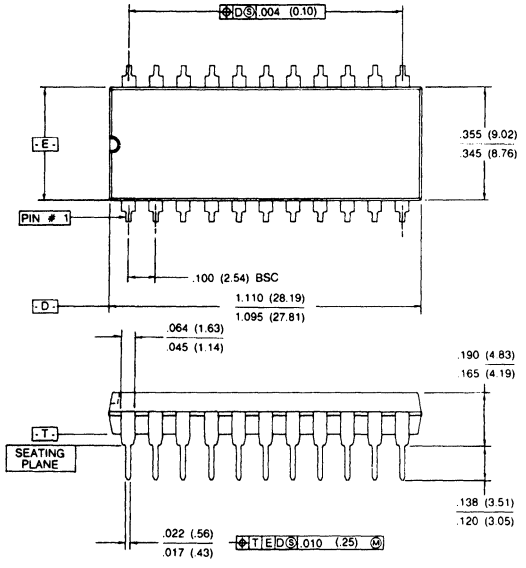


NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AE for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 20 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #20 when viewed from the top.

NL1 853-0408 81234

PO00290S

22-PIN PLASTIC DUAL IN-LINE (PDIP)

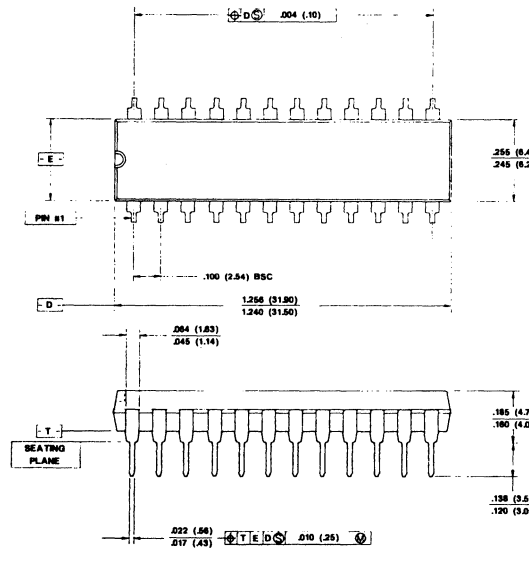


NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-010-AA for standard dual in-line (DIP) package .400 inch row spacing (PLASTIC) 22 leads (issue A. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #22 when viewed from the top.

NM2 853-0409 81235

PO00341S

24-PIN PLASTIC DUAL IN-LINE (PDIP)



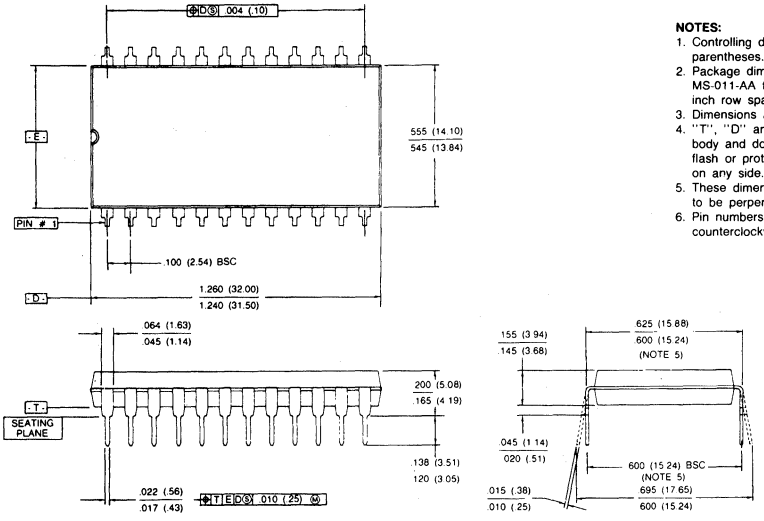
NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AF for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 24 leads (issue B. 7/85)
3. Dimension and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #24 when viewed from the top.

NN1 853-0410 93852

PO02400S

Package Outlines

24-PIN PLASTIC DIP (600mil-wide)

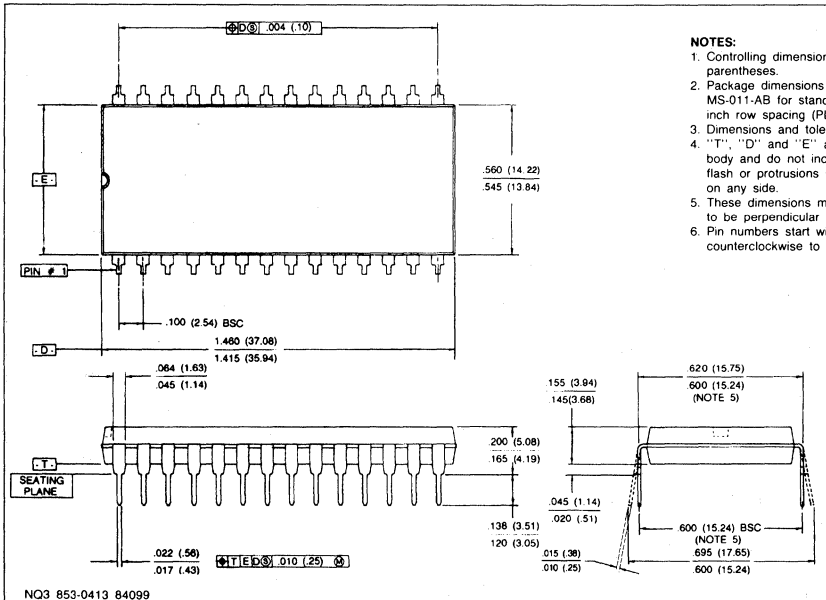


NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-011-AA for standard dual in-line (DIP) package .600 inch row spacing (PLASTIC) 24 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #24 when viewed from the top.

853-0412 81238

PO00361S

28-PIN PLASTIC DUAL IN-LINE (600mil-wide)



NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-011-AB for standard dual in-line (DIP) package .600 inch row spacing (PLASTIC) 28 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #28 when viewed from the top.

NQ3 853-0413 84099

PO00372S

PACKAGE OUTLINES

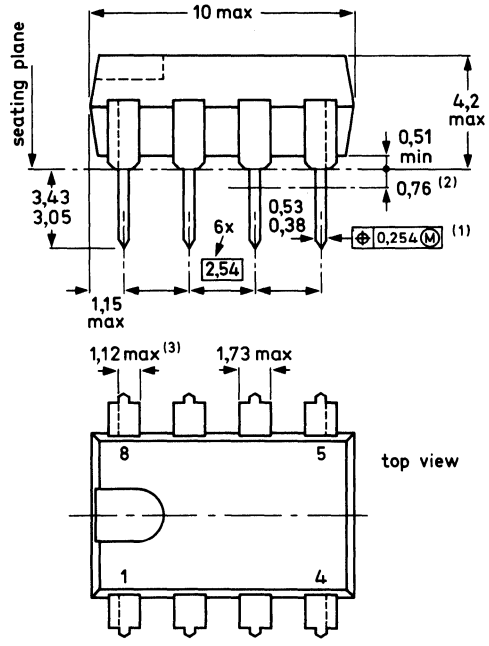
page

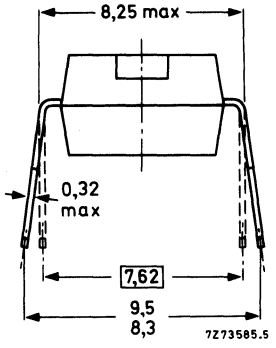
Introduction
for Prefixes: FCB, PCA, PCD, PCF 555

The package information for each type number is given below:

type number	description and package code	page
FCB51C64P	28-lead dual in-line; plastic (SOT117)	561
FCB51C64T	28-lead mini-pack; plastic (SO28XL; SOT213)	568
FCB51C65P	28-lead dual in-line; plastic (SOT117)	561
FCB51C65T	28-lead mini-pack; plastic (SO28XL; SOT213)	568
FCB61C65(L/LL)P	28-lead dual in-line; plastic (SOT117)	561
FCB61C65(L/LL)T	28-lead mini-pack; plastic (SO28XL; SOT213)	568
FCB61C251P	24-lead dual in-line; plastic (SOT101A,B,F,G,L)	558
FCB61C251T	24-lead mini-pack; plastic (SOJ24; SOT239)	570
FCB61C252P	24-lead dual in-line; plastic (SOT101A,B,F,G,L)	558
FCB61C252T	24-lead mini-pack; plastic (SOJ24; SOT239)	570
FCB61C253P	28-lead dual in-line; plastic (SOT117)	561
FCB61C253T	28-lead mini-pack; plastic (SO28XL; SOT213)	568
FCB61C257(L/LL)P	28-lead dual in-line; plastic (SOT117)	561
FCB61C257(L/LL)T	28-lead mini-pack; plastic (SO28XL; SOT213)	568
FCB61C1025(L/LL)P	32-lead dual in-line; plastic (SOT201)	567
FCB61C1025(L/LL)T	32-lead mini-pack; plastic (SO32 2XL; SOT221)	569
PCA8582BP	8-lead dual in-line; plastic (SOT97)	557
PCA8582BT	16-lead mini-pack; plastic (SO16L; SOT162A)	563
PCD5101P	22-lead dual in-line; plastic (SOT116)	560
PCD5101T	24-lead mini-pack; plastic (SO24; SOT137A)	562
PCD5114P	18-lead dual in-line; plastic (SOT102G, N, PE)	559
PCD5114T	20-lead mini-pack; plastic (SO20; SOT163A)	564
PCF8570P	8-lead dual in-line; plastic (SOT97)	557
PCF8570T	8-lead mini-pack; plastic (SO8L; SOT176C)	566
PCF8570CP	8-lead dual in-line; plastic (SOT97)	557
PCF8570CT	8-lead mini-pack; plastic (SO8L; SOT176C)	566
PCF8571P	8-lead dual in-line; plastic (SOT97)	557
PCF8571T	8-lead mini-pack; plastic (SO8L; SOT176C)	566
PCF8581P	8-lead dual in-line; plastic (SOT97)	557
PCF8581T	8-lead mini-pack; plastic (SO8L; SOT176C)	566
PCF8581CP	8-lead dual in-line; plastic (SOT97)	557
PCF8581CT	8-lead mini-pack; plastic (SO8L; SOT176C)	566
PCF8582AP	8-lead dual in-line; plastic (SOT97)	557
PCF8582AT	16-lead mini-pack; plastic (SO16L; SOT162A)	563
PCF8582CP	8-lead dual in-line; plastic (SOT97)	557
PCF8582CT	16-lead mini-pack; plastic (SO16L; SOT162A)	563
PCF8583P	8-lead dual in-line; plastic (SOT97)	557
PCF8583T	8-lead mini-pack; plastic (SO8L; SOT176A)	565

8-LEAD DUAL IN-LINE; PLASTIC (SOT97)





⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

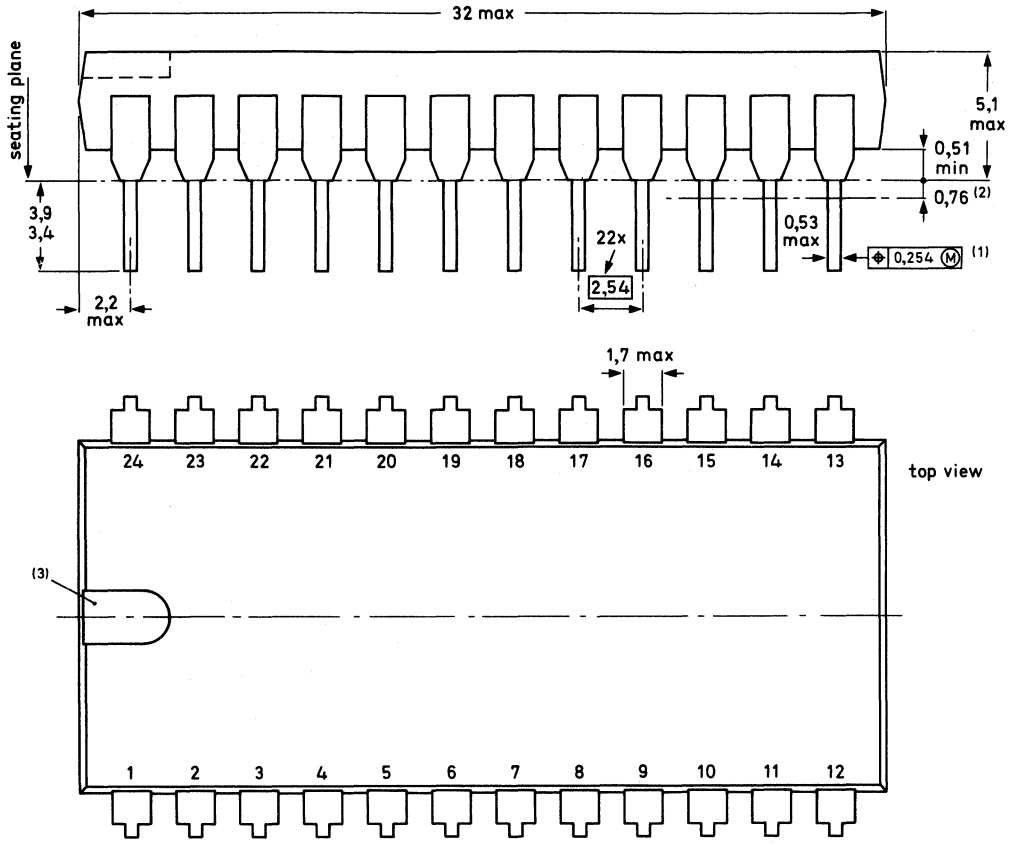
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

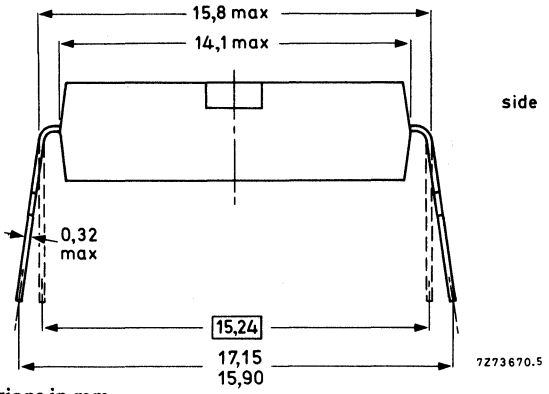
(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Only for devices with asymmetrical end-leads.

Dimensions in mm

24-LEAD DUAL IN-LINE; PLASTIC (SOT101A, B, F, G, L)





⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

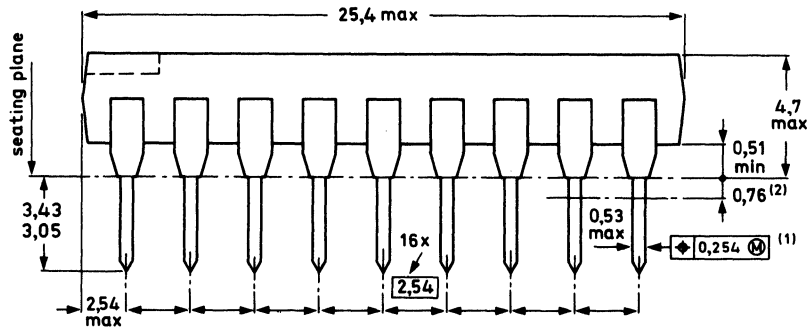
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

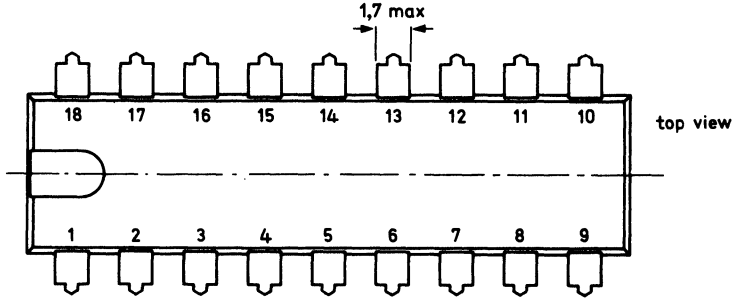
(2) Lead spacing tolerances apply from seating plane to the line indicated.

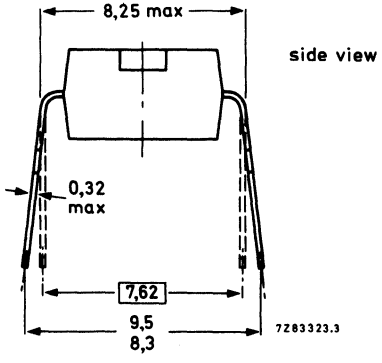
(3) Index may be horizontal as shown, or vertical.

Dimensions in mm

18-LEAD DUAL IN-LINE; PLASTIC (SOT102G, N, PE)







⊕ Positional accuracy.

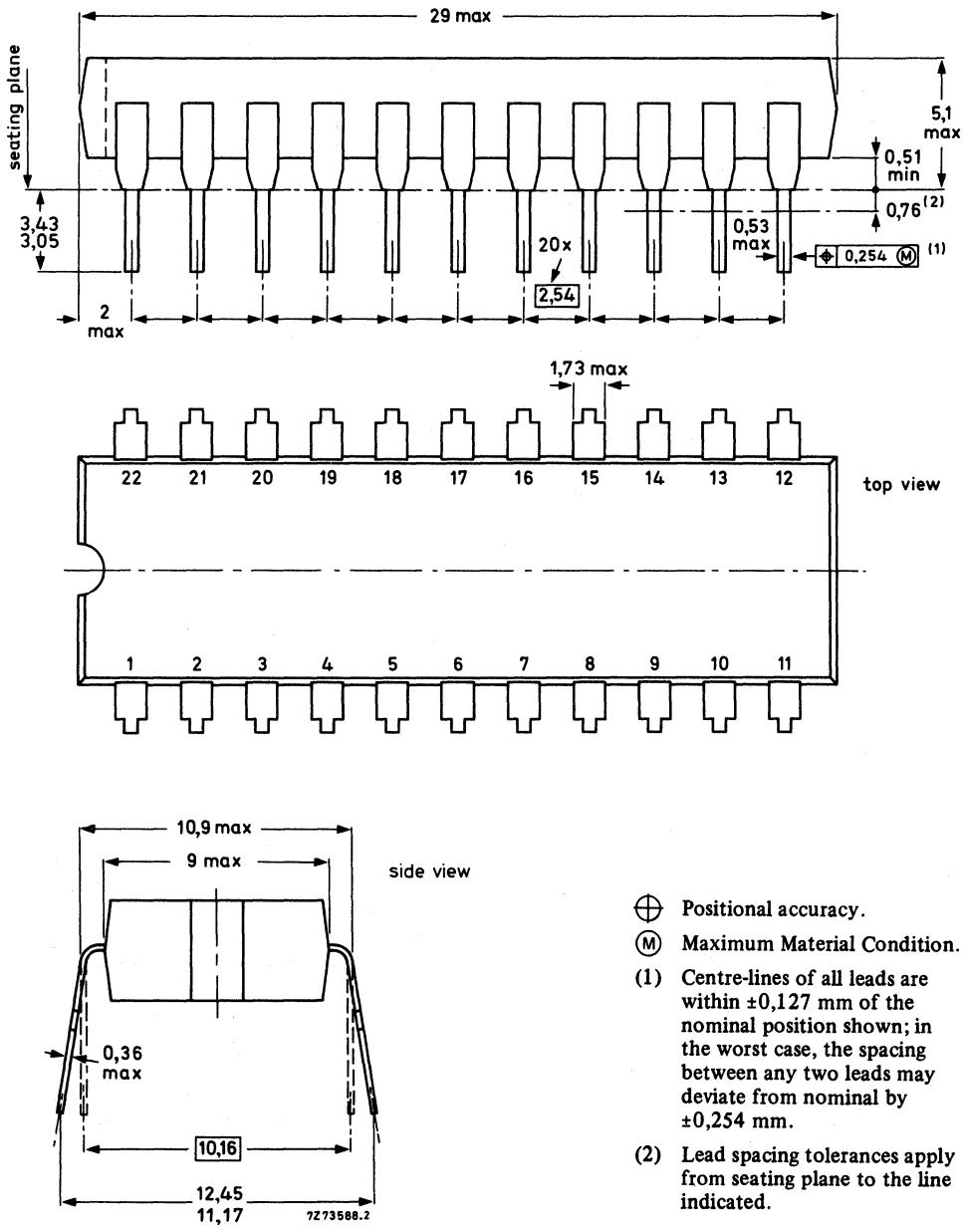
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

22-LEAD DUAL IN-LINE; PLASTIC (SOT116)



⊕ Positional accuracy.

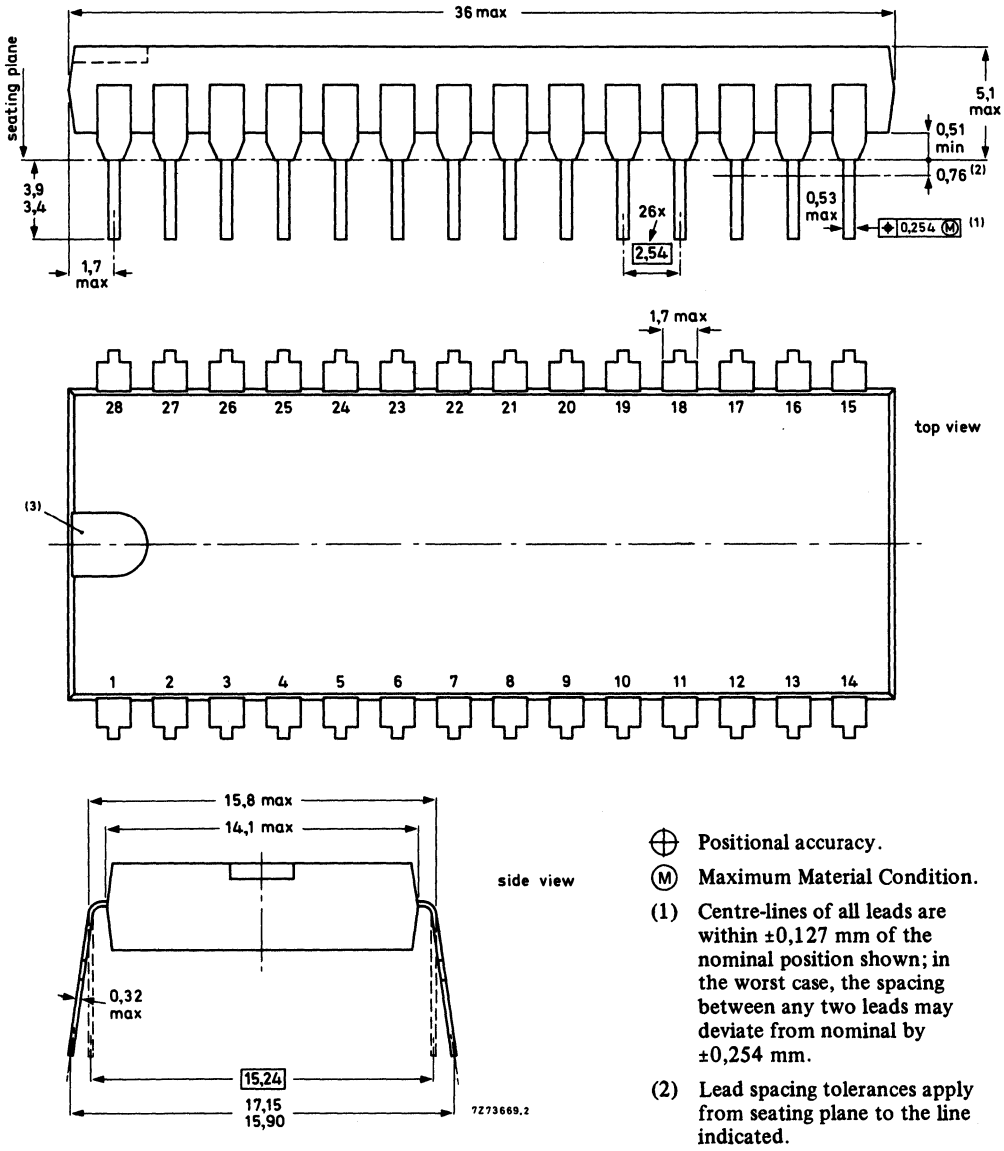
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

28-LEAD DUAL IN-LINE; PLASTIC (SOT117)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

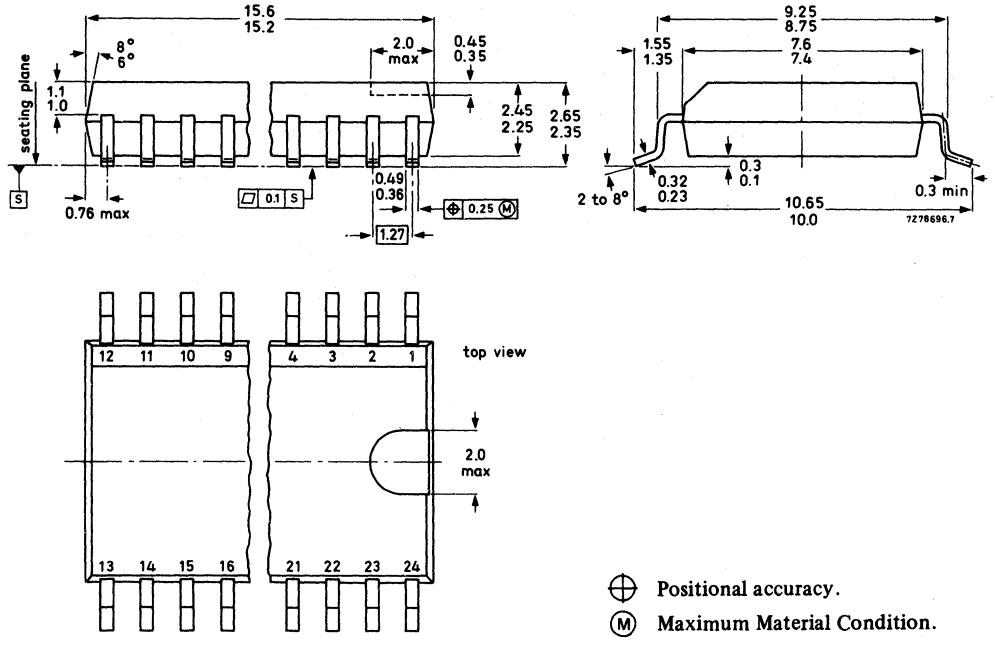
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

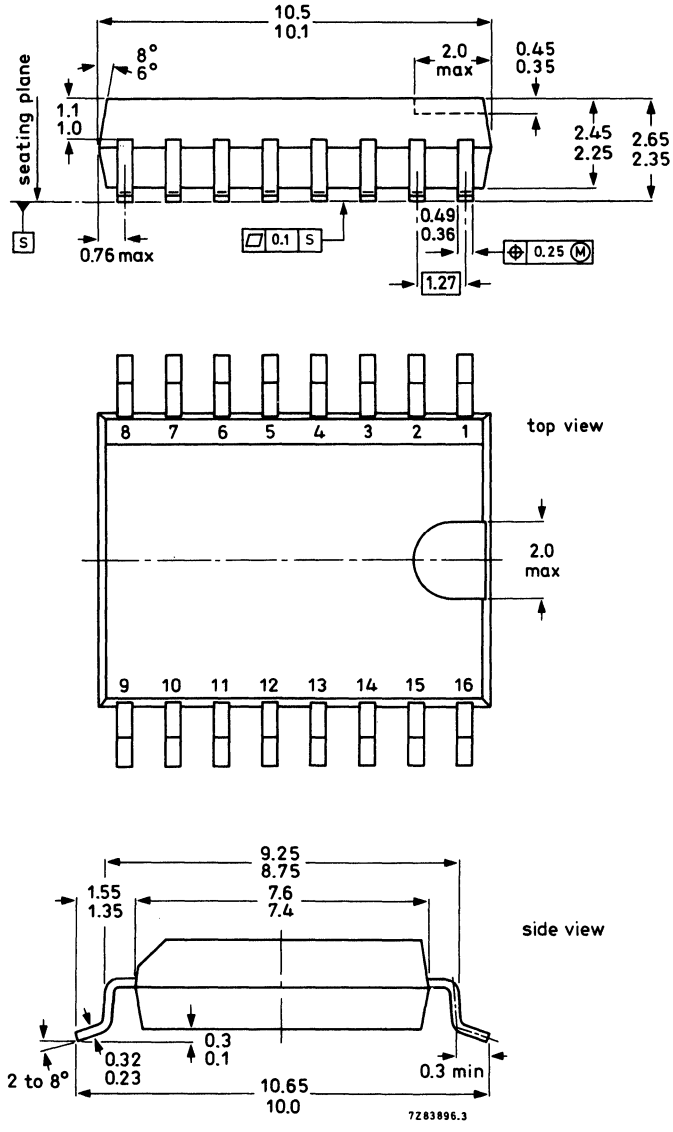
Dimensions in mm

24-LEAD MINI-PACK; PLASTIC (SO24; SOT137A)



Dimensions in mm

16-LEAD MINI-PACK; PLASTIC (SO16L; SOT162A)

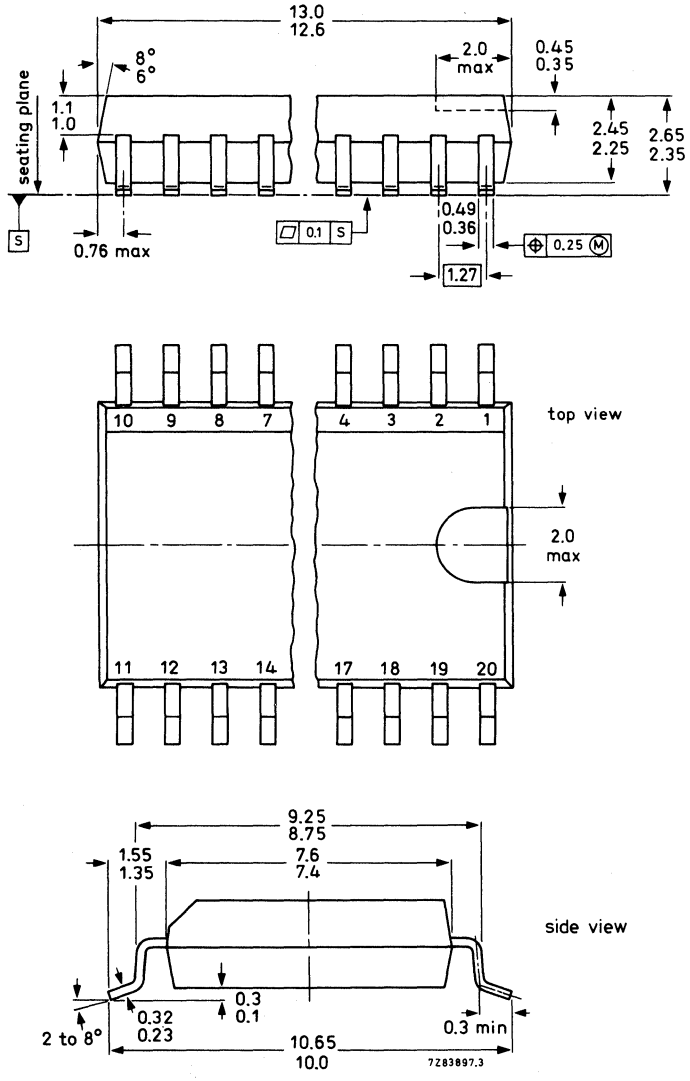


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

20-LEAD MINI-PACK; PLASTIC (SO20; SOT163A)

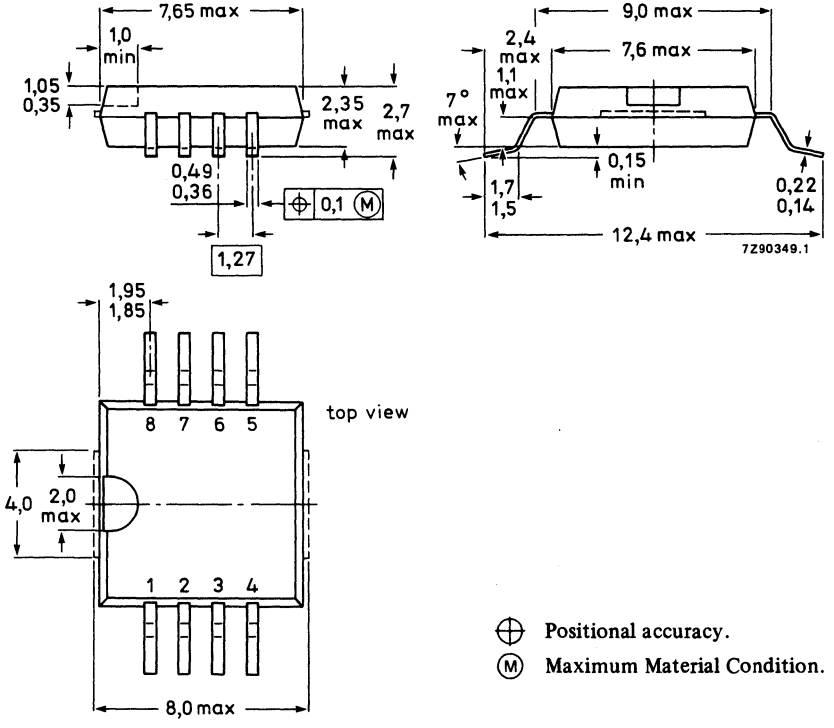


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

8-LEAD MINI-PACK; PLASTIC (SO8L; SOT176A)

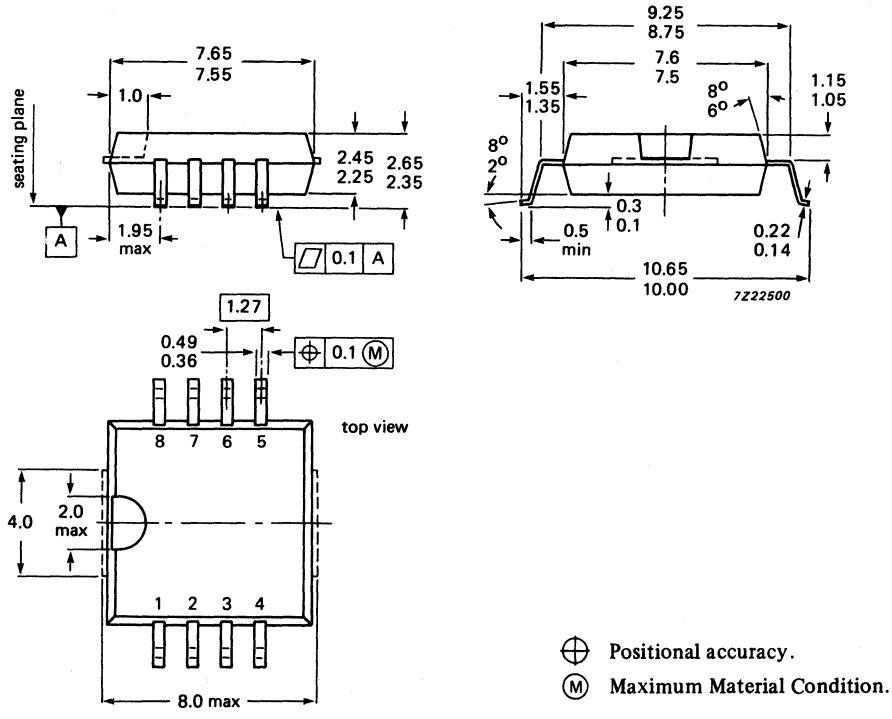


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

8-LEAD MINI-PACK; PLASTIC (SO8L; SOT176C)

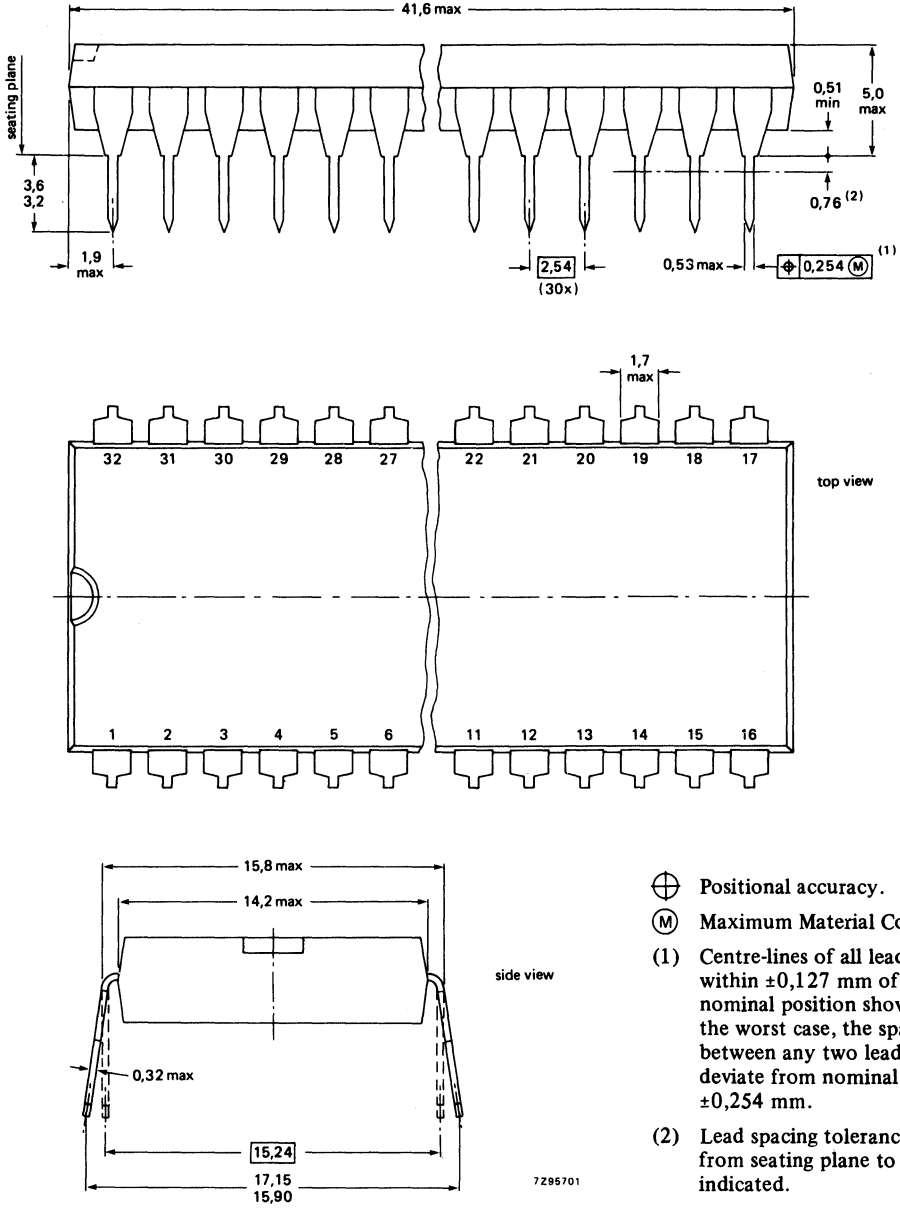


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

32-LEAD DUAL IN-LINE; PLASTIC WITH INTERNAL HEAT SPREADER (SOT201)



⊕ Positional accuracy.

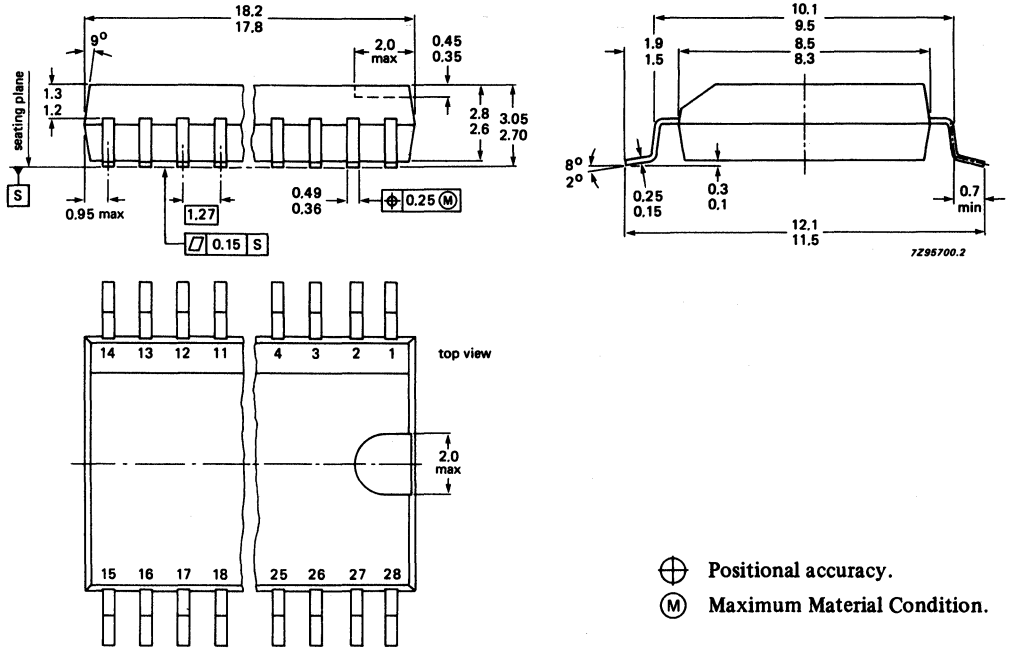
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

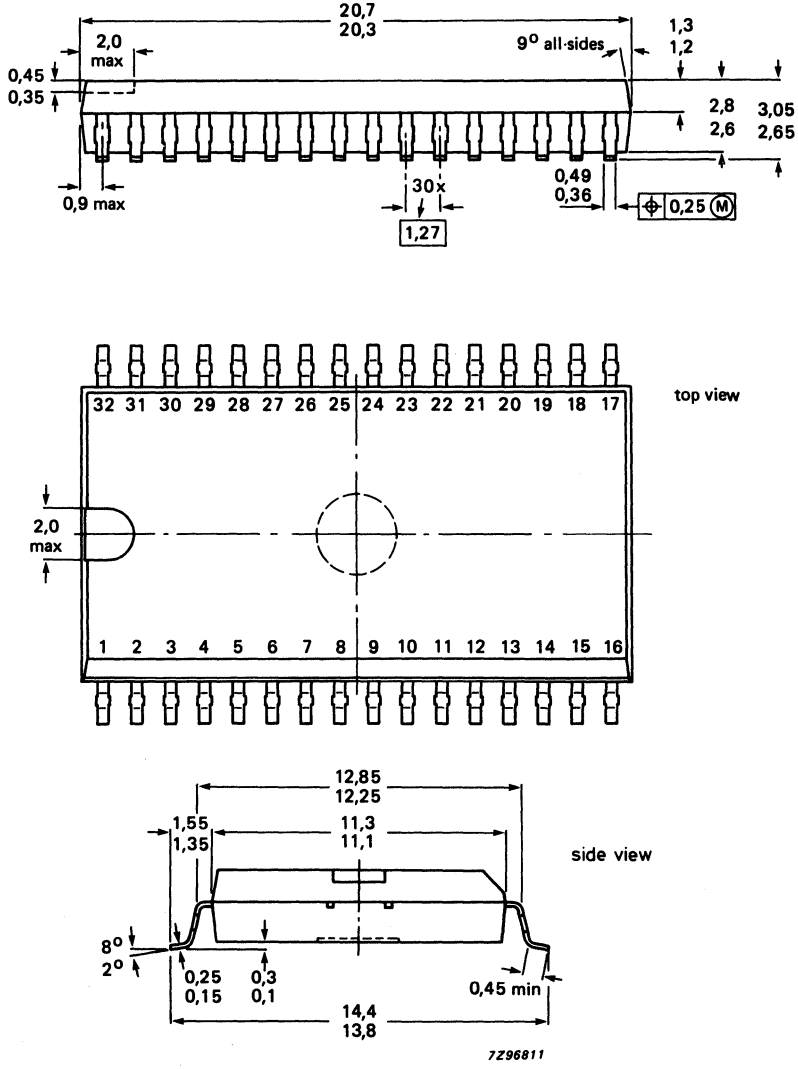
Dimensions in mm

28-LEAD MINI-PACK; PLASTIC (SO28XL; SOT213)



Dimensions in mm

32-LEAD MINI-PACK; PLASTIC (SO32 2XL; SOT221)

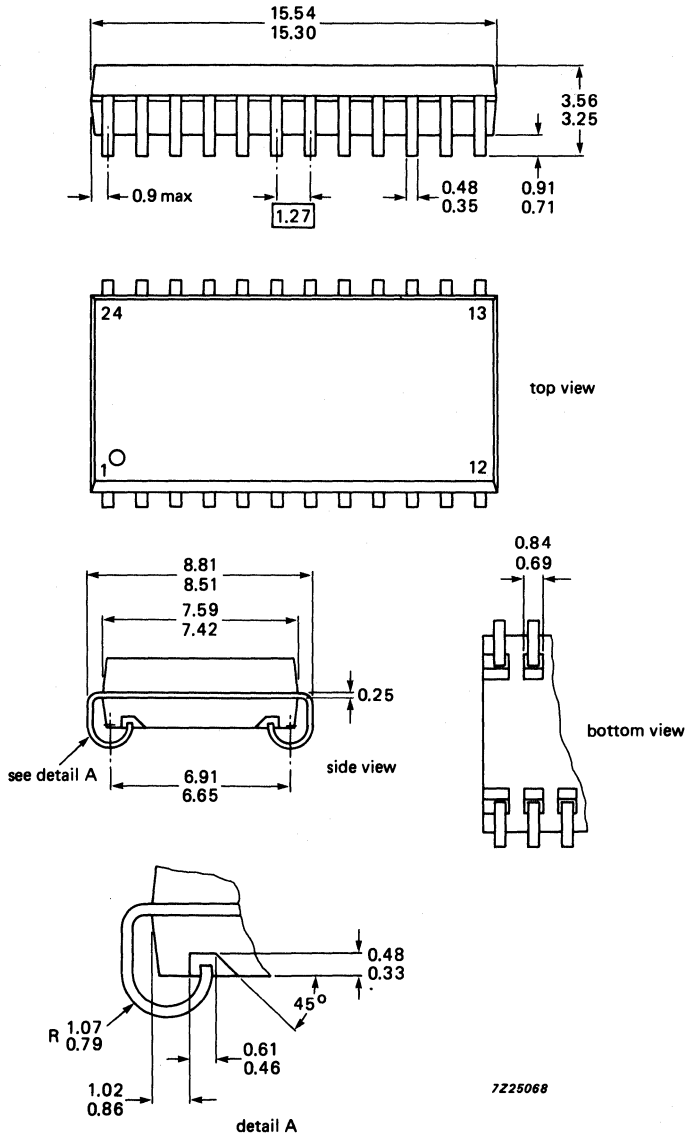


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

24-LEAD MINI-PACK; PLASTIC (J-BENT LEADS) (SOJ24; SOT239)



Dimensions in mm

SOLDERING

page

Plastic dual in-line (DIL) packages **573**
Plastic mini-pack (SO) packages **573**

SOLDERING PLASTIC MINI-PACKS

1. By hand-held soldering iron or pulse-heated solder tool

Fix the component by first soldering two, diagonally opposite end leads. Apply the heating tool to the flat part of the lead only. Contact time must be limited to 10 seconds at up to 300 °C. When using proper tools, all other leads can be soldered in one operation within 2 to 5 seconds at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages).

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to substrate by dipping or by an extra thick tin/lead plating before package placement.

2. By wave

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 seconds, if allowed to cool to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

3. By solder paste reflow

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing, for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 seconds according to method. Typical reflow temperatures range from 215 to 250 °C.

Pre-heating is necessary to dry paste and evaporate binding agent.

Pre-heating duration: 45 minutes at 45 °C.

4. Repairing soldered joints

The same precaution and limits apply as in (1) above.

SOLDERING PLASTIC DUAL IN-LINE PACKAGES

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 and 400 °C, for not more than 5 seconds.

2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

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DATA HANDBOOK SYSTEM

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INTEGRATED CIRCUITS

DISCRETE SEMICONDUCTORS

DISPLAY COMPONENTS

PASSIVE COMPONENTS*

PROFESSIONAL COMPONENTS**

MATERIALS*

The contents of each series are listed on pages iii to viii.

The data handbooks contain all pertinent data available at the time of publication, and each is revised and reissued periodically.

When ratings or specifications differ from those published in the preceding edition they are indicated with arrows in the page margin. Where application is given it is advisory and does not form part of the product specification.

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Product specialists are at your service and enquiries will be answered promptly.

* Will replace the Components and materials (green) series of handbooks.
** Will replace the Electron tubes (blue) series of handbooks.

INTEGRATED CIRCUITS

This series of handbooks comprises:

code	handbook title
IC01	**Radio, audio and associated systems** Bipolar, MOS
IC02a/b	**Video and associated systems** Bipolar, MOS
IC03	**ICs for Telecom** Bipolar, MOS Subscriber sets, Cordless Telephones
IC04	**HE4000B logic family** CMOS
IC05	**Advanced Low-power Schottky (ALS) Logic Series**
IC06	**High-speed CMOS; PC74HC/HCT/HCU** Logic family
IC07	**Advanced CMOS logic (ACL)**
IC08	**ECL 10K and 100K logic families**
IC09N	**TTL logic series**
IC10	**Memories** MOS, TTL, ECL
IC11	**Linear Products**
IC12	**I^2C-bus compatible ICs**
IC13	**Semi-custom** Programmable Logic Devices (PLD)
IC14	**Microcontrollers** NMOS, CMOS
IC15	**FAST TTL logic series**
Supplement to IC15	**FAST TTL logic series**
IC16	**CMOS integrated circuits for clocks and watches**
IC17	**ICs for Telecom** Bipolar, MOS Radio pagers Mobile telephones ISDN
IC18	**Microprocessors and peripherals**
IC19	**Data communication products**

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This series of data handbooks comprises:

current code	new code	handbook title
S1	**SC01**	**Diodes** High-voltage tripler units
S2a	**SC02***	**Power diodes**
S2b	**SC03***	**Thyristors and triacs**
S3	**SC04**	**Small-signal transistors**
S4a	**SC05**	**Low-frequency power transistors and hybrid IC power modules**
S4b	**SC06**	**High-voltage and switching power transistors**
S5	**SC07**	**Small-signal field-effect transistors**
S6	**SC08** **SC09**	**RF power transistors** **RF power modules**
S7	**SC10**	**Surface mounted semiconductors**
S8a	**SC11***	**Light emitting diodes**
S8b	**SC12**	**Optocouplers**
S9	**SC13***	**PowerMOS transistors**
S10	**SC14**	**Wideband transistors and wideband hybrid IC modules**
S11	**SC15**	**Microwave transistors**
S15**	**SC16**	**Laser diodes**
S13	**SC17**	**Semiconductor sensors**
S14	**SC18***	**Liquid crystal displays and driver ICs for LCDs**

* Not yet issued with the new code in this series of handbooks.
** New handbook in this series; will be issued shortly.

DISPLAY COMPONENTS

This series of data handbooks comprises:

current code	new code	handbook title
T8	**DC01**	**Colour display components**
T16	**DC02**	**Monochrome monitor tubes and deflection units**
C2	**DC03**	**Television tuners, coaxial aerial input assemblies**
C3	**DC04***	**Loudspeakers**
C20	**DC05**	**Flyback transformers, mains transformers and general-purpose FXC assemblies**

* These handbooks are currently issued in another series; they are not yet issued in the Display Components series of handbooks.

PASSIVE COMPONENTS

This series of data handbooks comprises:

current code	new code	handbook title
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C11	**PA02**	**Varistors, thermistors and sensors**
C12	**PA03**	**Potentiometers and switches**
C7	**PA04**	**Variable capacitors**
C22	**PA05***	**Film capacitors**
C15	**PA06***	**Ceramic capacitors**
C9	**PA07***	**Piezoelectric quartz devices**
C13	**PA08**	**Fixed resistors**

* Not yet issued with the new code in this series of handbooks.

PROFESSIONAL COMPONENTS

This series of data handbooks comprises:

current code	new code	handbook title
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T2a	*	**Transmitting tubes for communications, glass types**
T2b	*	**Transmitting tubes for communications, ceramic types**
T3	**PC01****	**High-power klystrons**
T4	*	**Magnetrons for microwave heating**
T5	**PC02****	**Cathode-ray tubes**
T6	**PC03****	**Geiger-Müller tubes**
T9	**PC04****	**Photo and electron multipliers**
T10	**PC05**	**Plumbicon camera tubes and accessories**
T11	**PC06**	**Circulators and Isolators**
T12	**PC07**	**Vidicon and Newvicon camera tubes and deflection units**
T13	**PC08**	**Image intensifiers**
T15	**PC09****	**Dry reed switches**
C8	**PC10**	**Variable mains transformers; annular fixed transformers**
	PC11	**Solid state image sensors and peripheral integrated circuits**

* These handbooks will not be reissued.
** Not yet issued with the new code in this series of handbooks.

MATERIALS

This series of data handbooks comprises:

current code	new code	handbook title
C4 C5	MA01*	**Soft Ferrites**
C16	MA02**	**Permanent magnet materials**
C19	MA03**	**Piezoelectric ceramics**

* Handbooks C4 and C5 will be reissued as one handbook having the new code MA01.

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