Design Guide: TIDA-00915

Three-phase, 1.25-kW, 200-VAC small form factor GaN inverter reference design for integrated drives

Description

This reference design is a three-phase inverter with a continuous power rating of 1.25 kW at 50°C ambient and 550 W at 85°C ambient for driving 200-V AC servo motors. It features 600-V LMG3411R150 Gallium Nitride (GaN) power modules with an integrated FET and gate driver mounted on an 1.95-mm Insulated Metal Substrate (IMS) board for efficient heat dissipation. Isolation and control circuits are mounted on separate FR-4 boards - the dimensions of the design are 80 mm × 46 mm × 37 mm, including heatsink, control, isolation, and power stage. This ultra-small form factor, coupled with the ability to be natural convection fanless cooled, allows for easy integration of the drive with the motor, reducing the required cabinet space by up to 50% and cable lengths by up to 90 m in 6-axis motor applications including robotics, CNC machines, and so forth.

Resources

TIDA-00915	Design Folder
LMG3411R150	Product Folder
ISO7721	Product Folder
TL431	Product Folder
TLV1117	Product Folder
SN74AHC1G08	Product Folder
SN74LVC1G11	Product Folder
TMDSCNCD280049C	Tool Folder

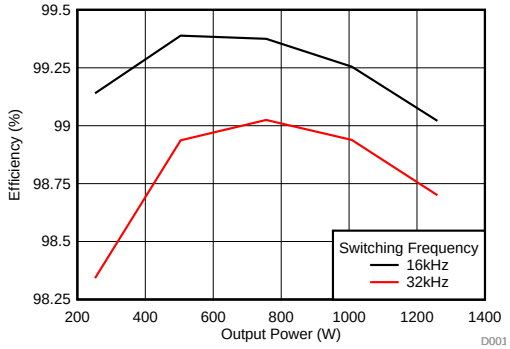
TI E2E™ Community — ASK Our E2E Experts

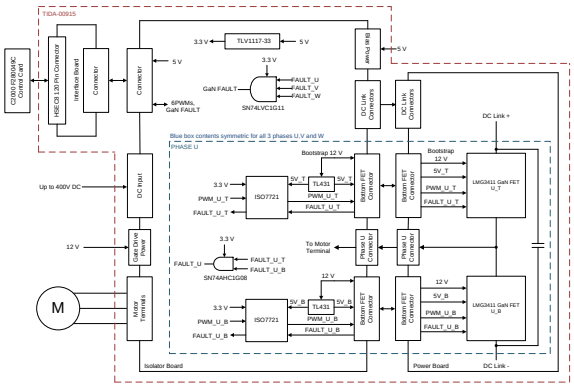
Features

- 600 V, 6-A LMG3411R150 GaN enables a power density of 150 W/in^3 in 50°C ambient conditions up to 1.25 kW and in 85°C ambient conditions up to 550 W
- Ultra-small form factor and natural convection fanless cooling allows easy integration of the drive with the motor saving floor space and cabling costs
- Very fast switching transition (< 5 ns) with minimal switch node voltage ringing reduces EMI
- High-efficiency power stage (peak efficiency > 99% at 32-kHz PWM) reduces heat sink size
- Protection against gate undervoltage, device overcurrent, and overtemperature

Applications

- Motor integrated drive
- Servo drives
- CNC machines
- Robotics





1 System Description

The challenges posed by Industry 4.0 demand miniaturization of manufacturing equipment to save floor space and reduce the time required to install and commission equipment. Motors and drives are at the heart of manufacturing and occupy significant space in a manufacturing environment.

Due to the demands of increased automation at higher efficiency and smaller footprint, there is an increasing need for motor-integrated drives. There is a two-fold benefit to integrating a drive with the motor:

1. It saves floor space since the drive and motor are housed as one unit
2. It eliminates the need for long cables connecting the motor and drive

Cabling can be an involved an expensive and complicated process, especially in multi-axis systems in advanced manufacturing. Additionally, troubleshooting cable faults are cumbersome and leads to increased downtime and loss in productivity. Integrating drive with the motor helps eliminate the cabling problem and also saves floor space, providing an immense benefit.

The major challenge in integrating the drive with the motor is the thermal design – the drive components are exposed to higher ambient temperatures with limited cooling. The drive should be able to deliver the rated power at higher ambient temperatures with limited cooling. This puts a stringent limit on the losses in the drive inverter; and hence, requires a high-efficiency drive.

Conventional IGBT-based inverter drives cannot be easily integrated with the motor due to the high losses in the IGBTs because of the reverse recovery in the diode and slower slew rates. These switching losses necessitate a larger heatsink or forced air or liquid cooling, both of which eliminate the possibility of integration with the motor. The solution to this problem is to use Gallium Nitride (GaN) FETs, which can operate in more challenging conditions than an IGBT with significantly lower switching losses. Table 1 shows the advantages of TI GaN FET modules over conventional Si-IGBTs, FETs

Table 1. Comparison of Silicon MOSFET and TI's GaN FET (HEMT)

PARAMETER	Si-FET	TI's GaN (HEMT)	COMMENTS
Device structure	Vertical	Lateral	The TI GaN FET and driver are in the same package, which reduces parasitic inductances and optimizes switching performance
$R_{DS(on)}$, area metric	> 10 mΩ-cm^2	Lateral 5 to 8 mΩ-cm^2	Lower conduction losses
Output charge Q_{OSS}	Approximately 25 nC	Approximately 5 nC	Enables faster switching, higher switching frequencies, and lower switching losses
Reverse recovery Q_{RR}	Approximately 2 to 15 µC-Ω	—	Zero reverse-recovery enables efficient half-bridge inverters and reduces or eliminates ringing in hard switching

GaN FETs can switch much faster than silicon IGBTs, which allows the potential to achieve lower switching losses. However, at high slew rates, certain package types can limit GaN FET switching performance. Integrating the GaN FET and driver in the same package reduces parasitic inductances and optimizes switching performance. The faster switching is achieved with little or no turnon or turnoff ringing, which reduces the electromagnetic interferences. For more details, see the *GaN FET module performance advantage over silicon* white paper.

The low-power dissipation benefits servo and integrated drives. In servo drives, the low-power dissipation results in a small form factor. In integrated drives, the drive electronics is enclosed inside the motor hub, and the inverter uses the motor frame as the heat sink. Here, the inverter has to operate at high ambient temperatures with natural convection fanless cooling. The low-power dissipation allows the embedded drive inverter to deliver more power for the same operating temperature.

The TIDA-00915 reference design is a 1.25-kW, three-phase inverter for driving 200-VAC motors. It features a 600-V LMG3411R150 GaN power module with an integrated FET, gate driver and protection circuitry. The TIDA-00915 design provides the required isolation between the microcontroller and power stage. This reference design also generates an active low signal to indicate a GaN fault. The TIDA-00915 supports an interface to a C2000™ F280049C control card through an interface board.

1.1 Key System Specifications

Table 2. Key System Specifications

PARAMETER	SPECIFICATION
DC link voltage	300 V (200 to 400 V)
Output voltage	Three-phase 200 V AC
Output current*	3.5 A_{RMS} continuous at 50°C, 1.5 A_{RMS} continuous at 85°C
Ambient temperature	85°C maximum
Nominal output power*	1.25 kW at 50°C, 550 W at 85°C
Slew rate	50 V/ns (unloaded)
PWM switching frequency	32 kHz maximum at 85°C; up to 100 kHz at room temperature
PWM dead-band	100 ns; load current based adaptive dead-time can improve efficiency further
Efficiency	> 99.3% peak efficiency at 16 kHz
Protection	UVLO protection on gate drive power supply (8.5 V) Cycle-by-cycle overcurrent protection (30 A) Overtemperature protection (165°C)
Host controller interface	3.3-V I/Os with: • 6×PWM signals for three phase inverter • 1 GaN fault signal
Power PCB form factor	80 mm × 46 mm x 1.95 mm 2 layers IMS
Isolator PCB form factor	80 mm × 46 mm x 0.8 mm 4 layers FR-4

* - maximum values depend on thermal system design; GaN module is capable of delivering continuous current of 6-A_{RMS}

2 System Overview

2.1 Block Diagram

Figure 1 shows the system block diagram of the TIDA-00915 reference design. The reference design consists of 3 separate PCBs - power board, isolator board, and interface board.

The power board is a 2-layer, 1.95-mm Insulated Metal Substrate (IMS) PCB that employs six 600-V, 6-A LMG3411R150 GaN power modules. The power board receives the DC link power, PWM signals from the isolator board through 6-pin connectors. The power board transmits phase current and fault signals back to the isolator board through similar connectors.

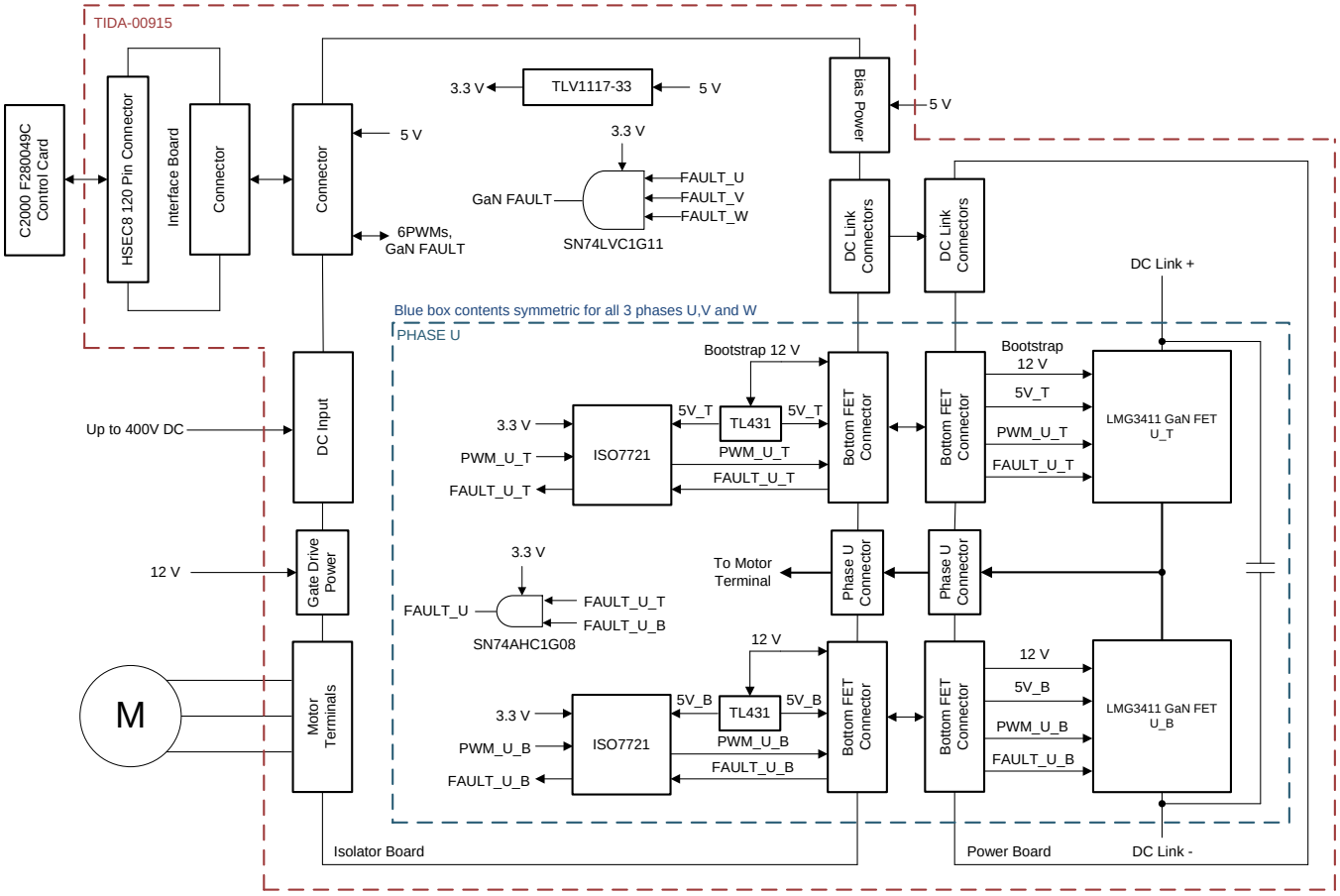
The isolator board is a 4-layer, 0.8-mm FR-4 PCB that consists of six ISO7721F digital isolators that provide isolation between the microcontroller and power stage for transferring PWM and fault signals; in addition it also contains the logic circuits (SN74AHC1G08, SN74LVC1G11) for combining the active-low fault signals from each of the six GaN power modules into one active low GaN fault signal. The isolator board holds all the input and output terminals - DC link input, 12-V input for gate drive power supply, 5-V input for control and logic circuitry, and 3-terminal output for motor connection.

The 12-V gate drive power supply biases the three bottom side GaN modules. The top-side GaN modules are biased using three separate bootstrap rails derived from the 12-V input. 5 V for isolator high side V_{DD} and GaN low-power mode pullup is derived from the 12-V biasing each GaN module (either the 12-V input or bootstrap rail) using the TL431 device in voltage-regulator mode. 5-V input is converted to 3.3 V for isolator low side V_{DD} and logic circuits using an LDO TLV1117. The isolator board connects to the interface board through a 14-pin connector - six PWM signals, one combined GaN fault signal and 5-V power are transmitted via this connector to the interface board.

The interface board is a 4-layer, 0.8-mm FR-4 PCB that connects to the C2000 TMDSCNCD280049C control card via a 120-pin HSEC8 connector. The C2000 control card implements a simple space vector modulated PWM to generate a rotating voltage vector where the frequency of the voltage vector and magnitude can be controlled and also monitors the GaN fault signal.

The TIDA-00915 three-phase inverter accepts voltages from 200- to 400-V DC at the DC link input. The nominal DC input voltage is 300 V DC. The GaN module has built-in undervoltage lockout (UVLO) on the gate drive input, overcurrent protection, and overtemperature protection.

Figure 1. TIDA-00915 Block Diagram



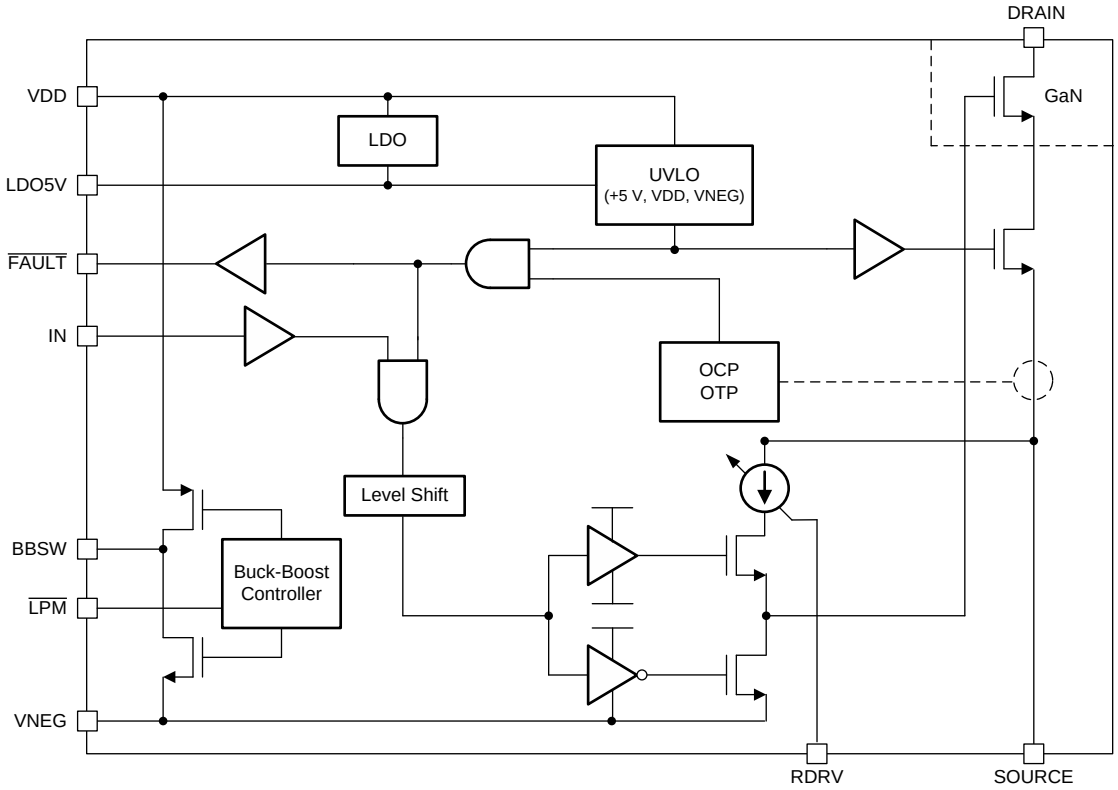
2.2 Highlighted Products

2.2.1 LMG3411R150

The LMG3411R150 GaN power stage with integrated driver and protection enables designers to achieve new levels of power density and efficiency in power electronics systems. The inherent advantages of the LMG3411 device over silicon MOSFETs include ultra-low input and output capacitance, zero reverse recovery to reduce switching losses by as much as 80%, and low switch node ringing to reduce EMI.

The LMG3411R150 device provides a smart alternative to traditional cascode GaN and standalone GaN FETs by integrating a unique set of features to simplify design, maximize reliability, and optimize the performance of any power supply. Integrated gate drive enables 100 V/ns switching with near zero Vds ringing, < 100-ns current limiting self-protects against unintended shoot-through events. Overtemperature shutdown prevents thermal runaway, and system interface signals provide self-monitoring capability.

Figure 2. LMG3411R150 Functional Block Diagram

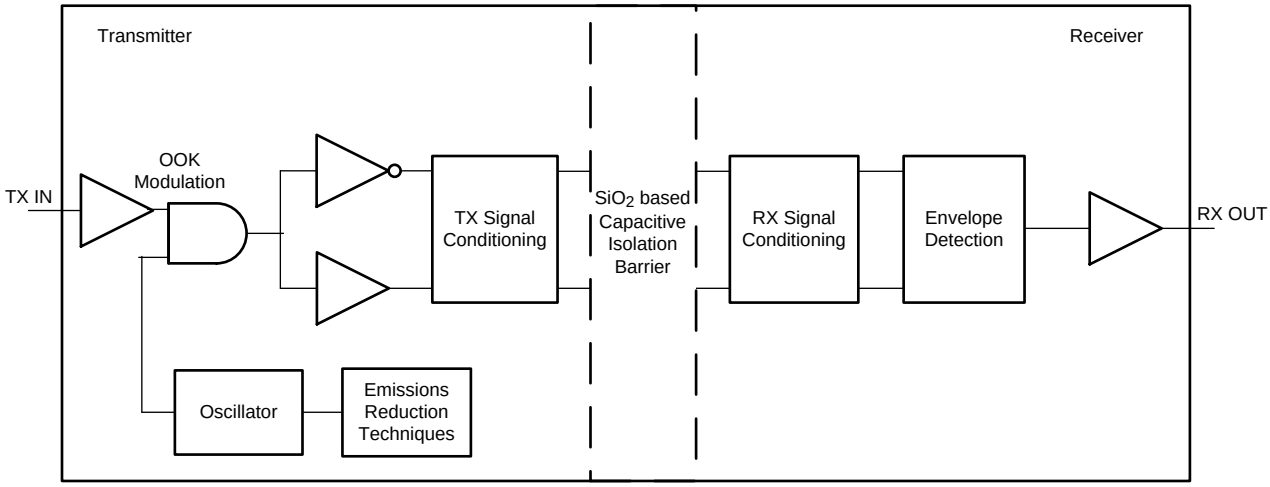


2.2.2 ISO7721

The ISO7721x devices are high-performance, dual-channel digital isolators with 3000-V_{RMS} (D package) isolation ratings per UL 1577. These devices are also certified by VDE, TUV, CSA, and CQC.

The ISO7721x devices provide high electromagnetic immunity and low emissions at low power consumption, while isolating CMOS or LVCMOS digital I/Os. Each isolation channel has a logic input and output buffer separated by a double capacitive silicon dioxide (SiO2) insulation barrier. The ISO7721x device has both channels in the opposite direction. In the event of input power or signal loss, the default output is high for devices without suffix F and low for devices with suffix F.

Figure 3. ISO7721 Functional Block Diagram

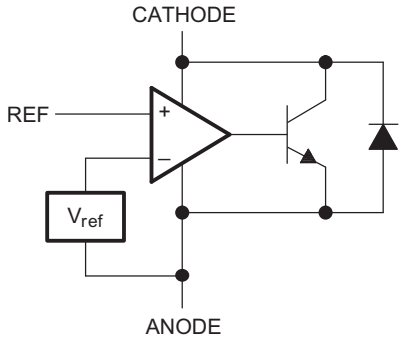


2.2.3 TL431

The TL431 and TL432 devices are three-terminal adjustable shunt regulators, with specified thermal stability over applicable automotive, commercial, and military temperature ranges. The output voltage can be set to any value between Vref (approximately 2.5 V) and 36 V, with two external resistors.

The TL431 device is offered in three grades, with initial tolerances (at 25°C) of 0.5%, 1%, and 2%, for the B, A, and standard grade, respectively. In addition, low output drift versus temperature ensures good stability over the entire temperature range.

Figure 4. TL431 Functional Block Diagram



2.2.4 TLV1117

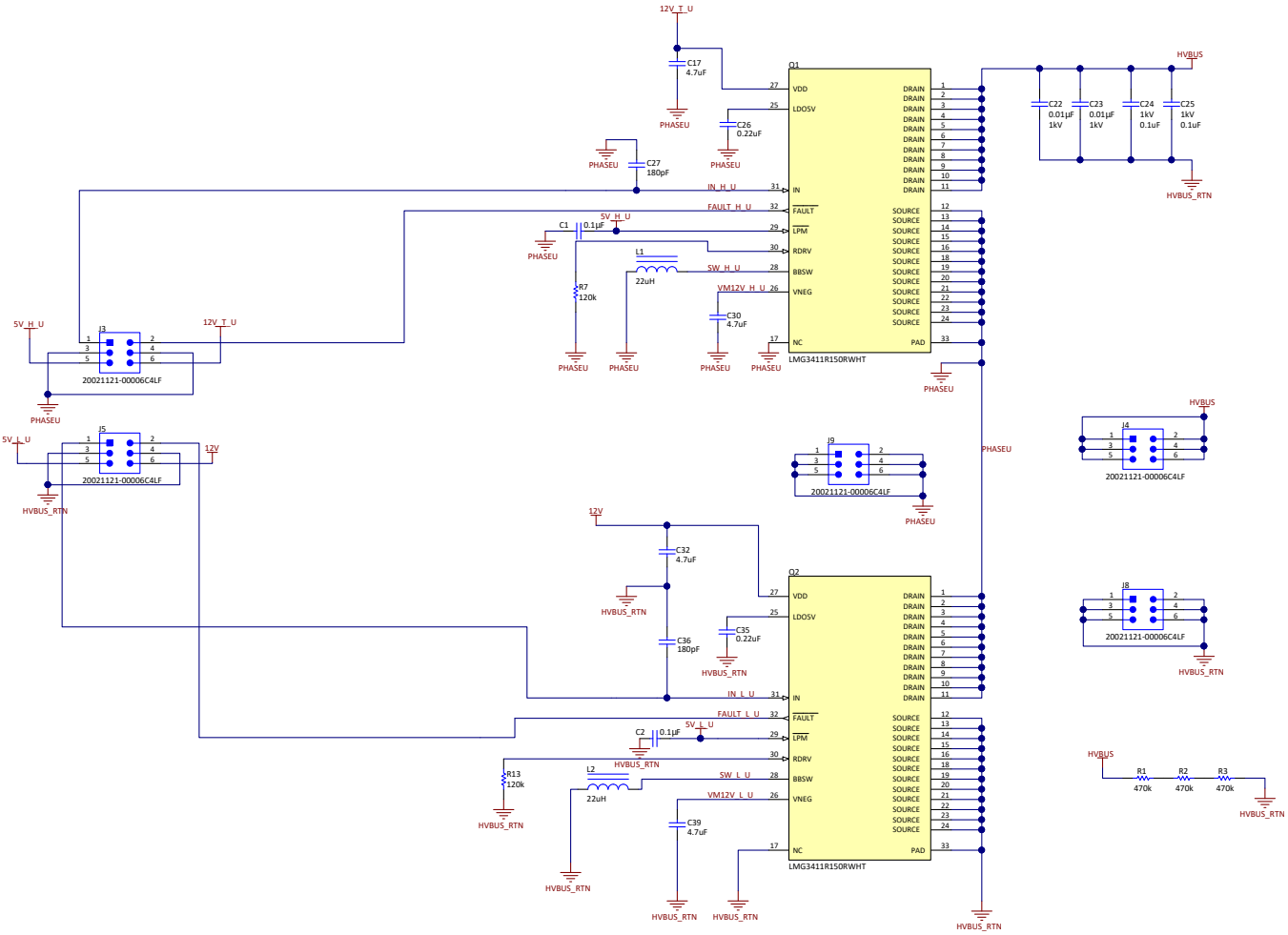
The TLV1117 device is a positive low-dropout voltage regulator designed to provide up to 800 mA of output current. The device is available in 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V, and adjustable-output voltage options. All internal circuitry is designed to operate down to 1-V input-to-output differential. Dropout voltage is specified at a maximum of 1.3 V at 800 mA, decreasing at lower load currents. The TLV1117 device is designed to be stable with tantalum and aluminum electrolytic output capacitors having an ESR between 0.2 and 10 Ω. Unlike pnp-type regulators, in which up to 10% of the output current is wasted as quiescent current, the quiescent current of the TLV1117 device flows into the load, increasing efficiency.

2.3 System Design Theory

2.3.1 Three-Phase GaN Inverter Power Stage

The three-phase GaN inverter is realized with six LMG3411R150 GaN modules. Figure 5 shows one half-bridge of the three-phase GaN inverter and the DC link connectors J4 and J8 on the power board. Bleeder resistors R1–R3 are used to discharge the bypass capacitors when DC link power is switched off.

Figure 5. GaN Inverter Half-Bridge Schematic



2.3.1.1 Bypass Capacitors

Each half-bridge has high-voltage (1 kV) ceramic bypass capacitors (C22 to C25 in Figure 5) providing a total capacitance of 0.22 µF per half-bridge. These bypass capacitors handle the high-frequency currents in the half-bridge during switching events. The bulk capacitors, which are usually kept after the AC-to-DC rectification in the end application, are not available in the reference design. The end system using the GaN inverter should have this to reduce voltage variation when operating from AC mains. However, for lab testing, this is inconsequential as the DC link is powered from a well-regulated high-voltage power supply.

2.3.1.2 Inverter Peak Power Capability

The LMG3411R150 device can deliver a continuous current of up to 6 A_{RMS} at a junction temperature of 125°C. The 6-A_{RMS} value should not be exceeded during operation. The 6-A_{RMS} is an intermittent maximum current rating for the TIDA-00915 design. The continuous current capability of the inverter (which will be ≤ 6 A_{RMS}) is determined by the thermal design. The peak power capability (P_{PEAK}) of the GaN inverter assuming a 3-phase output voltage (V_{OUT}) of 200 V_{RMS} and unity power factor (PF) is given by Equation 1:

$$P_{PEAK} = \sqrt{3} \times V_{OUT} \times I_{OUT} \times PF = \sqrt{3} \times 200 \times 6 \times 1 = 2078 \text{ W} \quad (1)$$

P_{PEAK} is the absolute maximum power the GaN inverter can handle - the continuous power rating of the GaN inverter is decided by thermal design and peak ambient temperature.

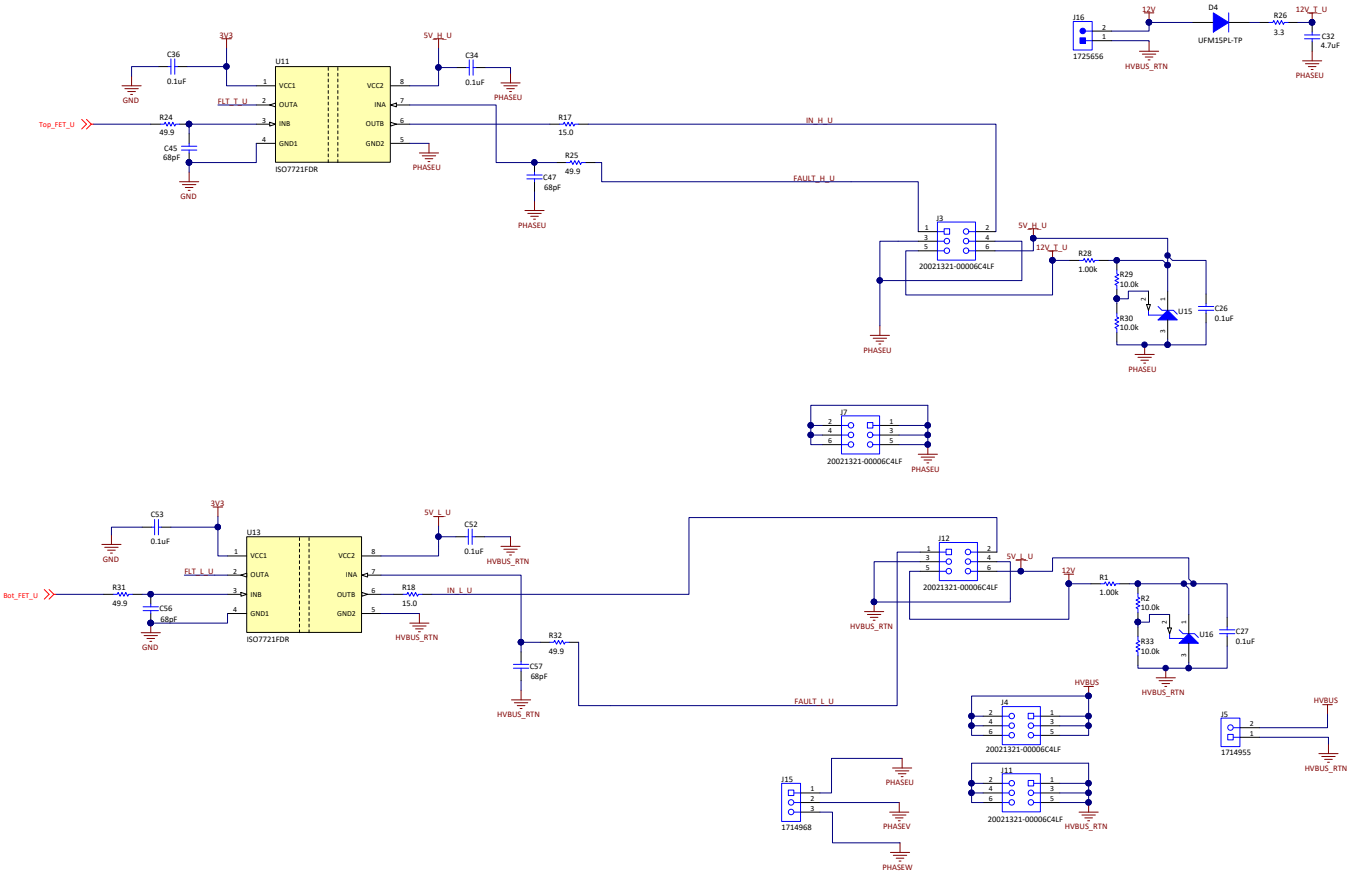
2.3.1.3 Power Stage Half Bridge

The power stage consist of three identical half bridges; Figure 5 shows one of the half bridges. C17 and C32 in Figure 5 are the bulk capacitors for the 12-V V_{DD} supply to the GaN modules. C17 corresponds to the top-side FET; this is, in effect, the bootstrap capacitor and needs to be sized appropriately for proper operation. The design of the bootstrap circuitry is detailed in Section 2.3.1.5. The GaN module also generates a negative 12-V power supply rail for the gate drive using an internal switching regulator; L1 and C30, and L2 and C39 are the passive components for this regulator. In addition, the GaN module generates a regulated 5 V using an internal LDO; C26 and C35 are decoupling capacitors for this regulated 5 V. The RDRV pin of the GaN module is used to set the drain slew rate, a 39 kΩ value sets the drain slew rate to 50 V/ns for an unloaded switching node. Drain slew rate can vary due to additional capacitance at the switching node from cables and motor windings. The GaN module has an active-low, low-power mode (LPM) pin - this is disabled by pulling to 5 V. C1 and C2 decouple the LPM pins from high-frequency noise.

Connectors J3 and J5 transfer the PWM and fault signals between the power board and isolator board. Connector J9 is tied to the phase node and transfers the phase current to the isolator board. See the PCB layout recommendations for suggestions on good layout practices how to avoid noise-related issues.

Isolation is required between the GaN module, which is on the high-voltage side, and the controller generating the PWM, which is on the low-voltage side. Figure 6 shows the isolation section of one half bridge in the isolator board. The digital isolator ISO7721F is chosen to provide a suitable isolation barrier (3000 V_{RMS}), and also support a very high CMTI of 100 V/ns. Each GaN module is connected to a corresponding digital isolator on the isolator board through the 6-pin connector pairs (for example, J3 in Figure 5 and J3 in Figure 6, or J5 in Figure 5 and J12 in Figure 6). The PWM signal, fault signal, 12 V (directly from input or bootstrap rail) for powering the GaN module, 5 V (derived from corresponding 12 V to GaN module using TL431) for LPM pin pull-up and source of corresponding GaN module are tied through this connector pair for each GaN module.

Figure 6. Isolation Section of Half-Bridge Schematic



In Figure 6, J5 is the 2 terminal input connector for DC link, J15 is the 3 terminal output connector for motor connections, J16 is the two-terminal input connector for the 12-V gate drive power supply. J4 (connects to J4 in Figure 5) and J11(connects to J8 in Figure 5), in Figure 6, are 6-pin connectors to transfer the DC link power from isolator board to power board. J9 in Figure 5 and J7 in Figure 6 form a connector pair that tie together to form phase U output that is tied to the motor terminal connector.

2.3.1.4 Gate Drive Power Supply

The bottom side GaN modules for all three phases are powered using 12 V, which is supplied externally from connector J16 as Figure 6 shows. The top-side GaN modules are supplied through bootstrap arrangement from the 12-V power supply. Table 3 calculates the current requirement for the gate-drive power supply. The current consumption is considered maximum worst case from their respective data sheets. The 2.4 mA for the ISO7721 is the current consumed on the isolator high-side V_{DD} at 5 V and for a square waveform with a 1-Mbps transmission rate.

Table 3. Current Consumption of Gate Drive Power Supply

CIRCUIT POWERED FROM GATE DRIVE POWER SUPPLY	CURRENT
6 × LMG3411R150 (32 kHz)	6 x 2.3 mA
6 x ISO7721 (equivalent current of 1 mA at 12 V)	6 x 1 mA
6 x cathode current in TL431 (current in resistors R1 and R28 in Figure 6)	6 x 7 mA
Total	61.8 mA

12-V power supply should be able to supply a minimum of 62 mA–100 mA is recommended current limit with sufficient margin.

2.3.1.5 Bootstrap Power Supply

The top three LMG3410 devices are powered by a bootstrap power supply configuration consisting of a bootstrap capacitor (C_{BOOT} is C32 in Figure 6 and C17 in Figure 5), bootstrap diode (D4 in Figure 6) and bootstrap resistor (R_{BOOT} is R26 in Figure 6). C17 in Figure 5 is necessary to provide bulk capacitance since C32 in Figure 6 is in a different PCB and will have restricted ability in providing charge due to connector inductance. Hence, C17 is sized the same as C32. The maximum voltage that the bootstrap capacitor (V_{BS}) can reach is dependent on the elements of the bootstrap circuit. Consider the voltage drop across R_{BOOT}, V_F of the bootstrap diode, and the drop across the low-side switch (V_{DS_ON}, depending on the direction of current flow through the switch). Also, before the inverter is started, the bottom GaN module should be turned on for a sufficient duration to allow the bootstrap capacitor to charge.

2.3.1.6 Selection of Bootstrap Capacitor (C_{BOOT})

The bootstrap capacitor is charged when the bottom GaN module is on and is discharged when the top GaN module is on. C_{BOOT} must be sized to maintain enough voltage throughout the PWM period. The current required to supplied is 2.3 mA (LMG3411R150 at 32-kHz PWM) + 1 mA (ISO7721) + 7 mA (TL431 cathode current) = 10.3 mA. For 32 kHz, the PWM period is 31.25 µs. This corresponding charge that has to be stored on C_{BOOT} is 31.25 µs × 10 mA = 0.3125 µC. A good guideline is to size C_{BOOT} to store ten times the charge over the PWM period (that is, C_{BOOT} should store Q_{BOOT} = 10 × 0.3125 µC). The bootstrap capacitor has to supply this charge. C_{BOOT} is calculated as Q_{BOOT} / ΔV_{BOOT}, which is 3.125 µC / 1 V = 3.125 µF. C_{BOOT} is chosen to be 4.7 µF.

2.3.1.7 Selection of Bootstrap Diode

The voltage that the bootstrap diode encounters is the same as the full DC bus voltage (in this case, a maximum of 400 V DC). The bootstrap diode voltage rating must be greater than the DC bus rail voltage. The bootstrap diode must be a fast-recovery diode to minimize the recovery charge and thereby the charge that feeds from the bootstrap capacitor from the 12-V supply. The diode must be able to carry a pulsed peak current of 4.43 A (discussed in Section 2.3.1.8). However, the average current is much smaller and depends on the switching frequency and the bootstrap charge. The selected diode is UFM15PL which is a 600-V, 1-A diode with a fast reverse recovery.

The bootstrap diode power dissipation (P_{DBOOT}) can be estimated based on the switching frequency, diode forward voltage drop, and the switching frequency of the PWM signal (f_{SW}). In the TIDA-00915 design, the maximum switching frequency has been set to 32 kHz. The estimated power loss for the bootstrap diode is:

$$P_{DBOOT} = ½ \times Q_{BOOT} \times V_{DBOOT} \times f_{SW} = 0.5 \times 3.125\ \mu C \times 1.7\ V \times 32\ kHz = 85\ mW.$$

2.3.1.8 Selection of Current Limiting Resistor for Bootstrap Diode (R_{BOOT})

The bootstrap charge Q_{BOOT} flows through R_{BOOT} for a minimum charging time of 1.56 µs (based on assumption maximum duty cycle is 95% at 32-kHz switching frequency); the average resistor current should be $I_{CH} = Q_{BOOT} / t = 0.3125\ \mu C / 1.56\ \mu s = 0.2$ A.

With the voltage drop across the diode being 1.7 V, the maximum value of $R_{BOOT} = V_{DBOOT} / I_{CH} = 1.7\ V / 0.2\ A \leq 8.5\ \Omega$.

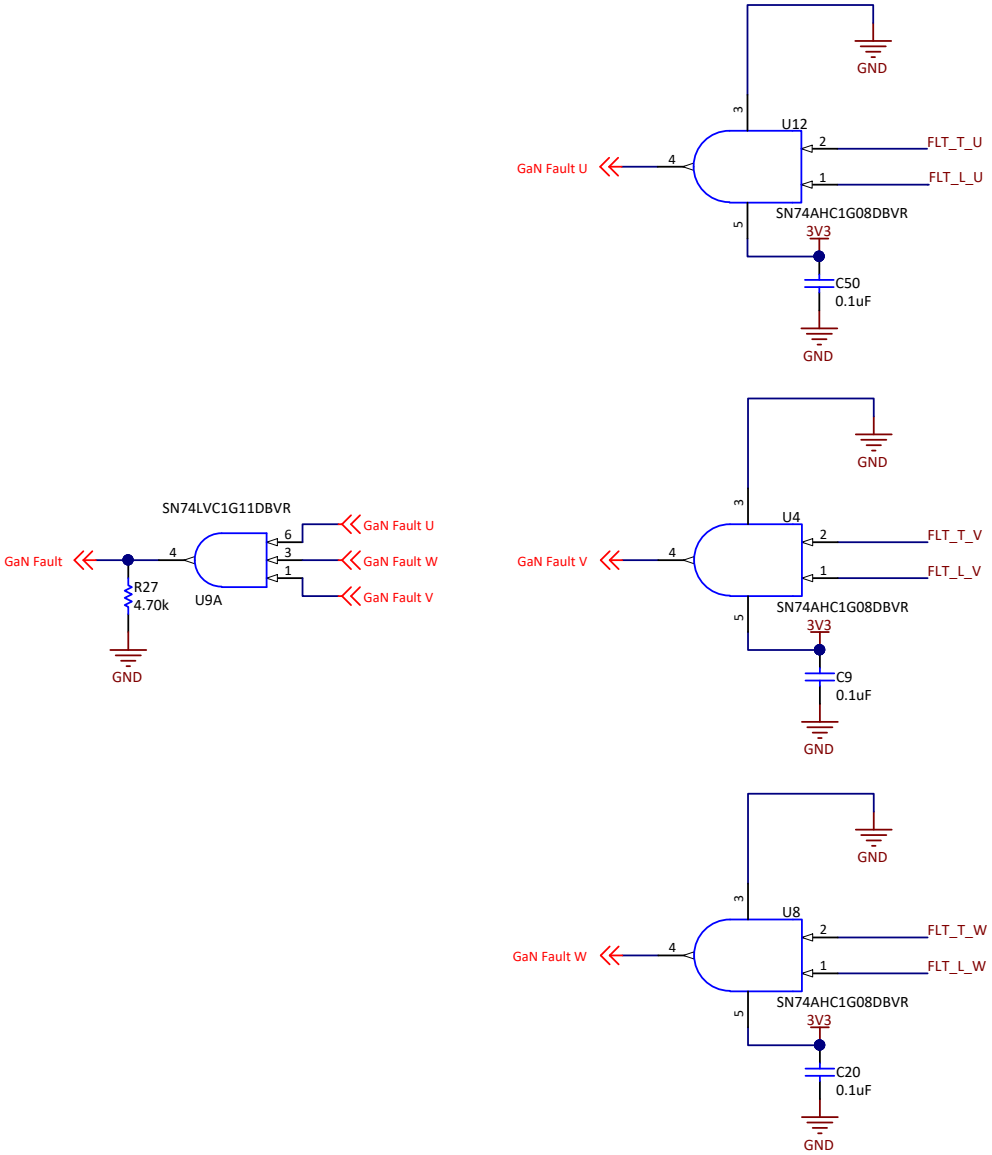
The TIDA-00915 reference design uses an R_{BOOT} value of 1 Ω. This is to allow sufficient charge to the bootstrap capacitor during the high-duty cycle region of *Space Vector PWM* to ensure the top side GaN module V_{DD} stays above UVLO limit of 8.5 V.

The peak resistor current is $(12\ V - V_{DBOOT}) / R_{BOOT} = (12\ V - 1.7\ V) / 1\ \Omega = 10.3$ A. The R_{BOOT} resistor should be able to supply this peak current and the average current of 0.2 A.

2.3.1.9 Inverter Protection and GaN Fault Feedback

The LMG3411 device has UVLO, overcurrent detection, and overtemperature with cycle-by-cycle turnoff of the GaN module. The UVLO is used to prevent improper operation due to a sub-optimal gate-drive power supply. The overtemperature and overcurrent protection ensures the GaN modules are protected against short-circuit faults of the inverter. There are six GaN modules each with an active-low fault signal, which are brought to the low-voltage side using digital isolators. Figure 7 shows how the fault signals are combined using the logic circuit.

Figure 7. GaN Fault Logic Circuit



2.3.2 5-V and 3.3-V Low-Voltage Power Rail

An external 5-V bias power supply is required to bias all the circuits on the low-voltage side of the board. Figure 8 shows the 5-V rail input. The diode D1 protects against accidental reverse polarity connection of the 5-V input. The TLV1117 device is the LDO used for generating the 3.3-V rail.

Figure 8. 3.3-V Power Supply

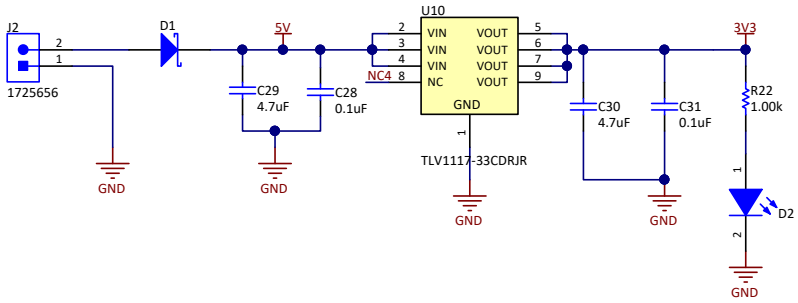


Table 4 shows the power consumption by the different circuit biased by the 3.3-V rail. There are six digital isolators ISO7721, an indication LED, and GaN fault combination circuitry using AND gates powered from this 3.3-V rail. The current consumption is considered maximum worst case from their respective data sheets. The 2.4 mA for ISO7721 device is the current consumed on the low-voltage side bias at 3.3 V and for a square waveform with a 1-Mbps transmission rate.

Table 4. Current Consumption of 5-V Rail Power Supply

CIRCUITS POWERED FROM 3.3-V LDO	CURRENT
ISO7721 × 6	6 × 2.4 mA
SN74AHC1G08 × 3	3 × 4 mA
SN74LVC1G11 × 1	16 mA
Indication LED × 1	10 mA

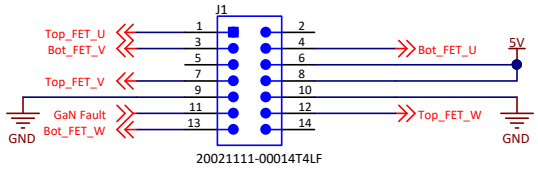
The total worst-case power consumption is about 52 mA. The power dissipation in the LDO is:

$P_{LDO} = (V_{IN} – V_{OUT}) \times I_{OUT} = (5 – 3.3) \times 0.052 = 0.088$ W

2.3.3 Signal Interface to Control Card

A 14-pin connector is used for connecting the isolator board to the interface board. Figure 9 shows the signals transferred between the interface board and isolator board - six PWM signals, one combined GaN fault signal, 5-V power, low-voltage ground. The 5 V is given from isolator board to the interface board to power the C2000 control card TMDSCNCD280049C. The 5 V is required to be supplied to the C2000 F280049C control card TMDSCNCD280049C, where the 5-V rail is stepped down to 3.3 V by an LDO to power the C2000 MCU on the control card. The interface signals are all 3.3-V logic signals.

Figure 9. 14-Pin Connector to Interface Board



2.3.4 Interface Board

The interface board is an adapter board between the 120-pin C2000 F280049C control card TMDSCNCD280049C and the isolator board. The interface board allows a small footprint 14-pin connector on the isolator board for connecting to the 120-pin control card. Also, the 14-pin connector enables sufficient clearance between the C2000 control card and the high-voltage sections of the isolator board.

3 Hardware, Software, Testing Requirements, and Test Results

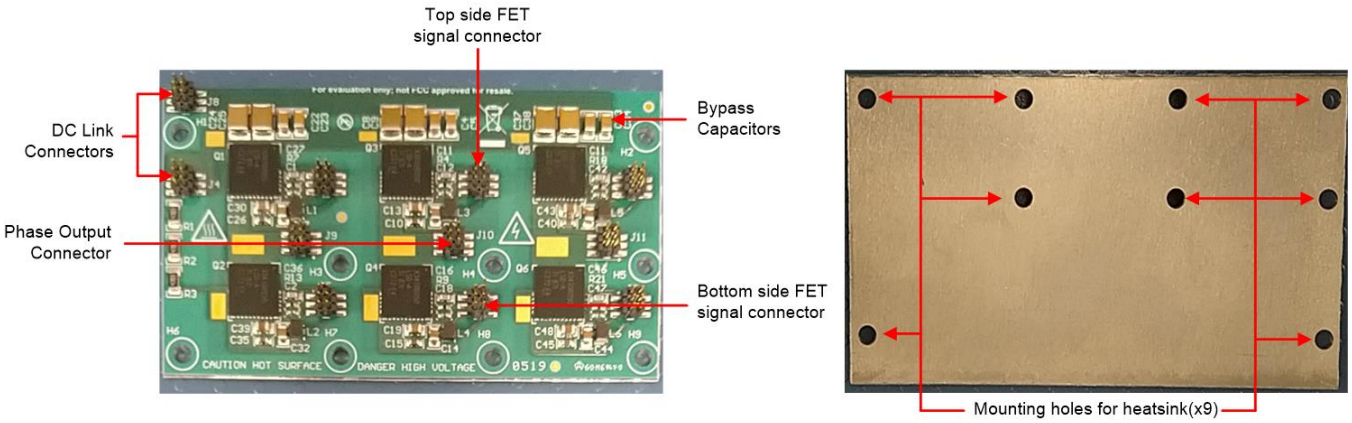
3.1 Required Hardware and Software

3.1.1 Hardware

3.1.1.1 Power PCB

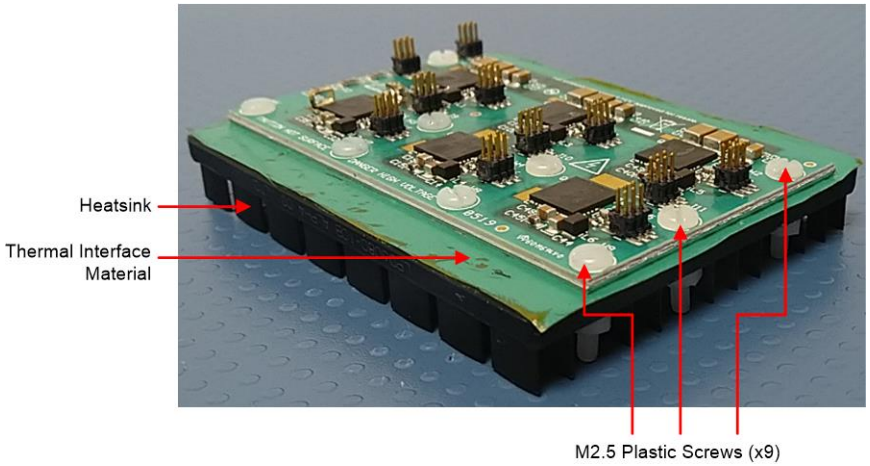
Figure 10 shows the top and bottom views of the IMS Power PCB of the TIDA-00915 reference design. 6-pin male connectors are used to transfer power and signals between power PCB and isolator PCB. The locations of the different function connectors are as marked in Figure 10. Each half-bridge has 0.22 µF of bypass capacitors for high-frequency current ripple. Nine mounting holes of M2.5 size are provided for making a firm and uniform contact with the heatsink.

Figure 10. TIDA-00915 Power PCB



The LPD6080-10B heatsink is chosen and the thermal interface material (TIM) is HF300P-0.001-00-0404. M2.5 holes are drilled in the heatsink and TIM and mounted onto the PCB using plastic screws (for isolation) as Figure 11 shows. The TIM chosen is phase-change material owing to superior thermal properties at temperatures > 55°C. The thermal impedance of the system can be further reduced by using thermal grease instead of TIM. An IMS board insulates the bottom side aluminium from electrical circuits and hence thermal grease can be used instead of TIM.

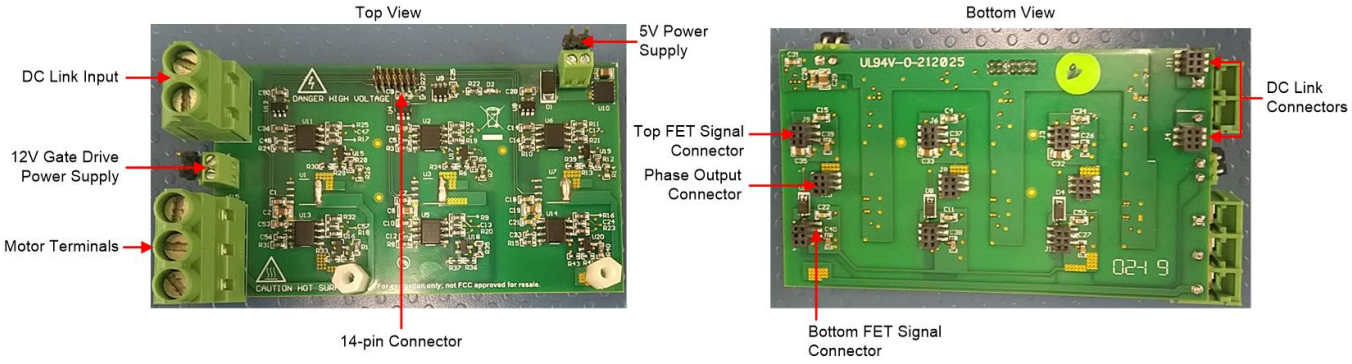
Figure 11. TIDA-00915 Power PCB Mounted on Heatsink



3.1.1.2 Isolator PCB

Figure 12 shows the top and bottom views of the isolator PCB of the TIDA-00915 design. All input and output terminals of TIDA-00915 are in isolator PCB. The top views show the DC link input, 12-V gate drive power supply, 5-V power supply connectors, the motor terminal connector, and the 14-pin male connector for the interface board for PWM and GaN fault signal. The bottom view shows the 6-pin female connectors that connect with the corresponding male connectors on the power PCB.

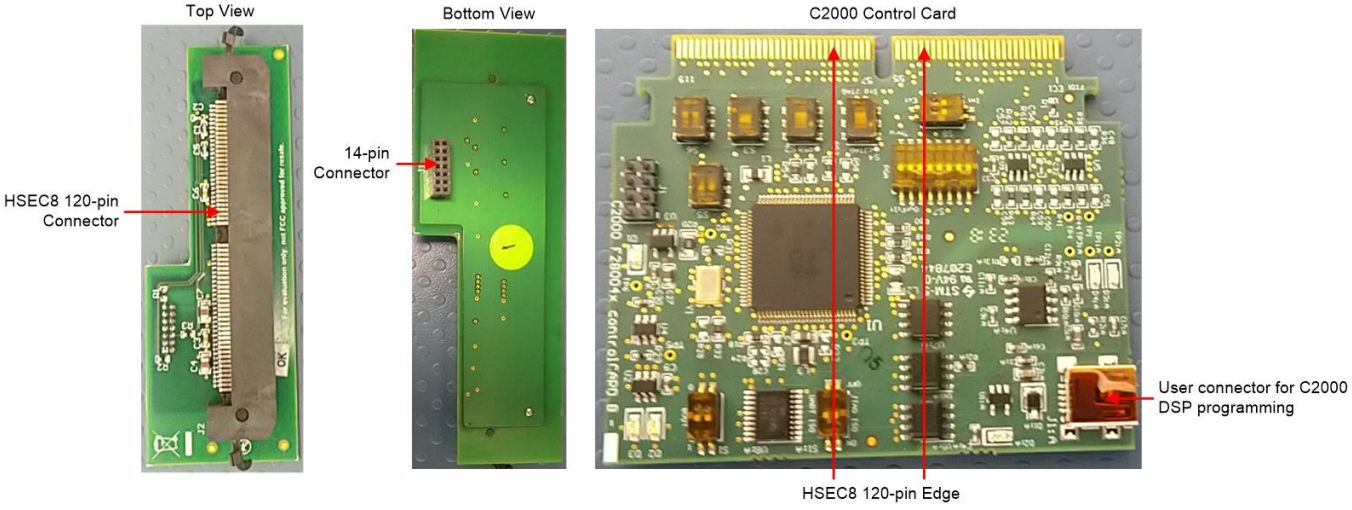
Figure 12. TIDA-00915 Isolator PCB



3.1.1.3 Interface PCB and C2000™ Control Card

Figure 13 shows the top and bottom views of the interface PCB and the top view of the C2000 Control Card. The top view of the interface PCB shows the HSEC8 120-pin connector to connect to the C2000 control card at the corresponding HSEC8 120-pin edge. The bottom view shows the 14-pin female connector to connect to the corresponding male connector in the isolator PCB. The C2000 control card receives power from the 5-V power supply in the isolator PCB via the 14-pin connector - an LDO in the C200 control card converts the 5 V to 3.3 V for C2000DSP power. The C2000 control card also has an isolated USB to connect to a computer for programming the C2000 DSP.

Figure 13. TIDA-00915 Interface PCB and C2000 Control Card



3.1.1.4 Assembling the PCBs

Figure 14 shows the alignment and order of assembling the PCBs. The double-sided arrow indicates the corresponding mating connectors on each PCB. The number indicates the order in which the PCBs connections should be made for ease of assembly.

Figure 14. Assembling the PCBs

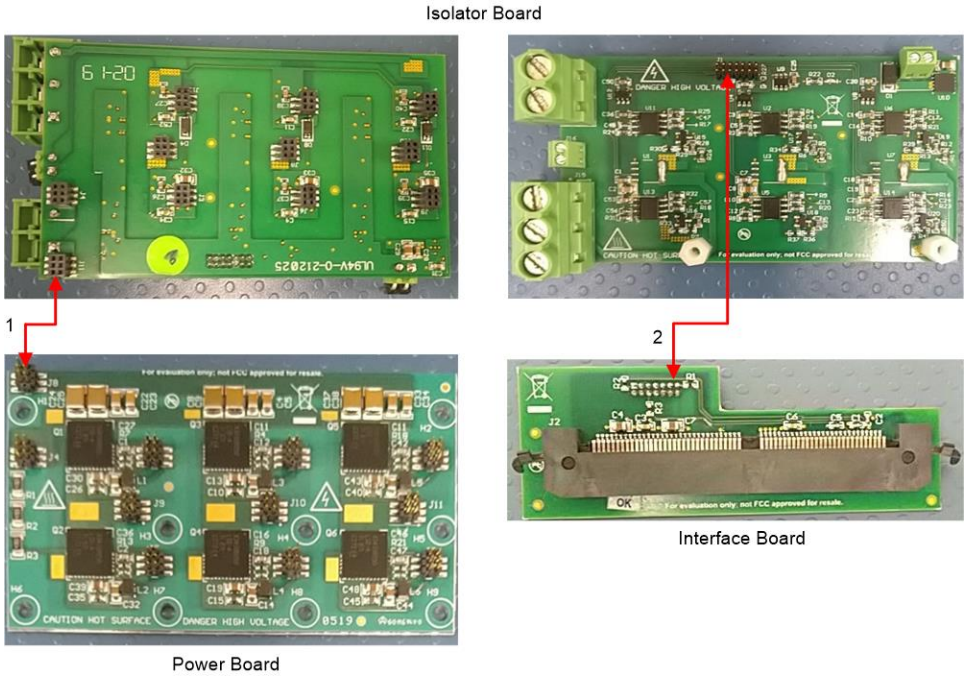
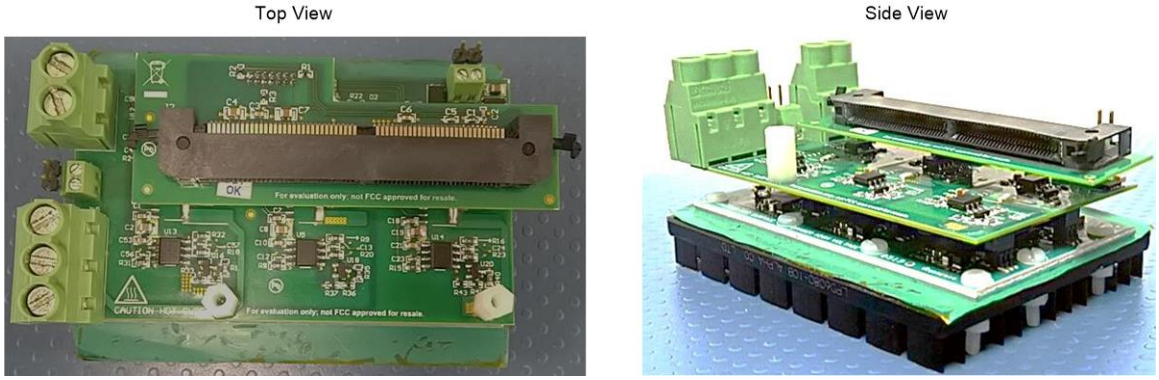


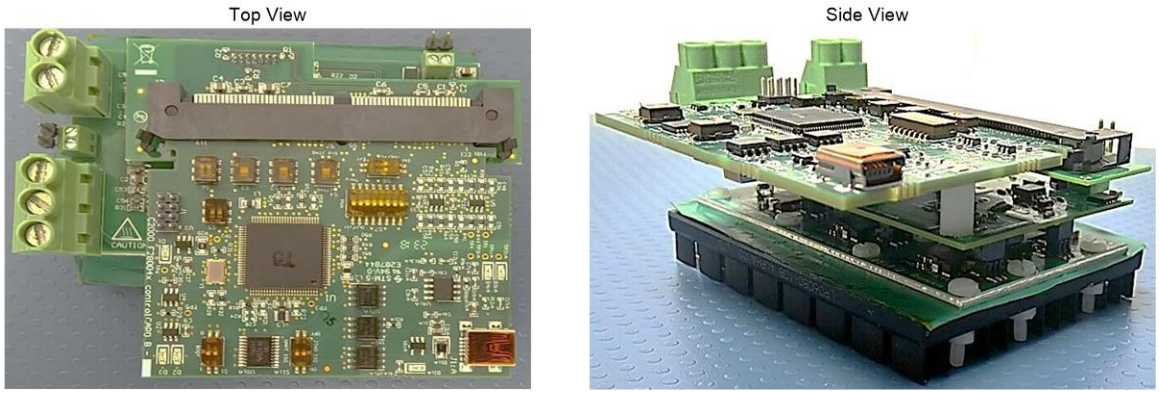
Figure 15 shows the top and side views of the assembled TIDA-00915.

Figure 15. Assembled TIDA-00915



The C2000 control card can be slotted into the HSEC8 120-pin connector on the interface PCB as in Figure 16.

Figure 16. TIDA-00915 With C2000™ Control Card



3.2 Testing and Results

3.2.1 Test Setup

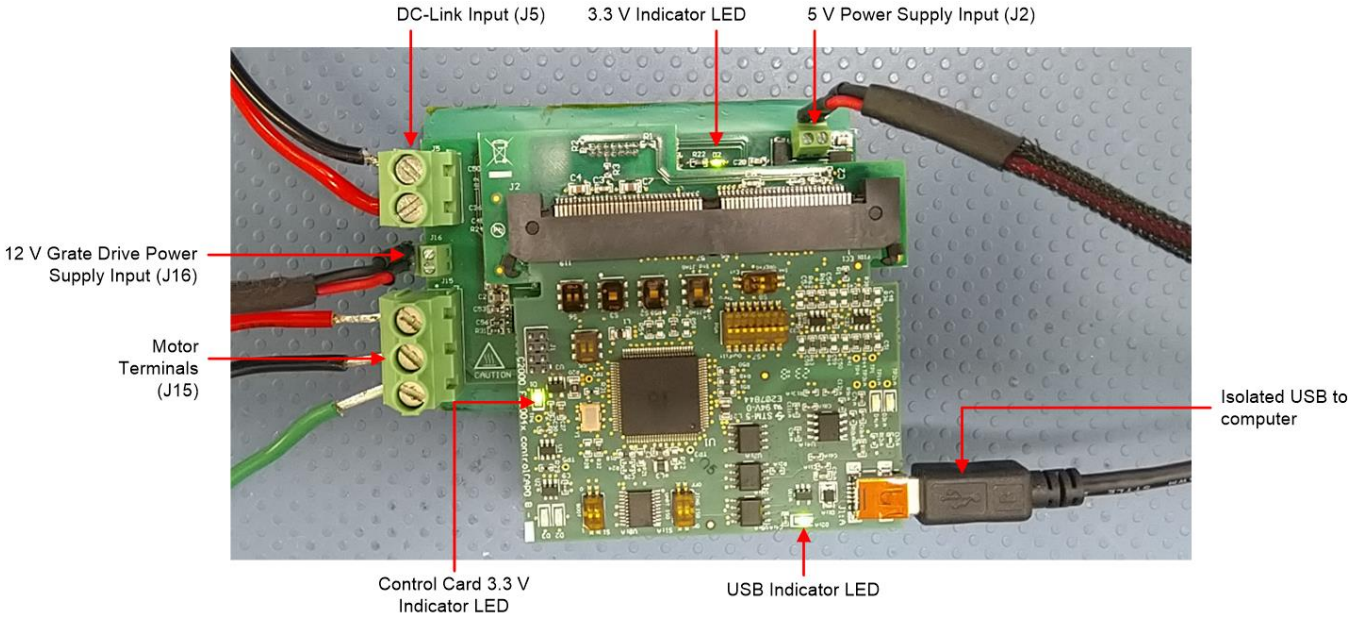
Table 5 lists the key test equipment. The board is powered from three power supplies: 300 V for the DC link, 12 V for the gate drive power supply, and 5 V for the low-voltage power supply for the microcontroller and logic circuits. All power supplies are isolated from each other.

Table 5. Key Test Equipment

DESCRIPTION	PART NUMBER
High-speed oscilloscope	Agilent MSO6104A
High-voltage isolated probe	Agilent N2790A
High-voltage non-isolated probe	Keysight 10076C
Low-voltage probes	Tektronix TPP0101
Isolated current probe	Keysight N2783B
C2000 F280049C control card	Texas Instruments TMDSCNCD280049C
Regulated power supply	Agilent E3631A (x2)
High-voltage power supply	Sorensen SGI 1000/5
Thermal camera	Fluke Ti480
Power analyzer	Tektronix PA4000
Inverter load	3.7 kW, 1460 rpm (0.5 to 100 Hz), 415 V_{RMS} ±10%, η = 83%, cosφ = 0.74

Figure 17 shows the TIDA-00915 connections: DC link input, 12-V gate-drive power supply, 5-V power supply for low-voltage bias, motor terminals and isolated USB connection to computer for C2000 DSP programming. For the input terminals (DC link, 12 V and 5 V) the red wire denotes positive polarity and the black wire denotes negative polarity.

Figure 17. TIDA-00915 Test Connections

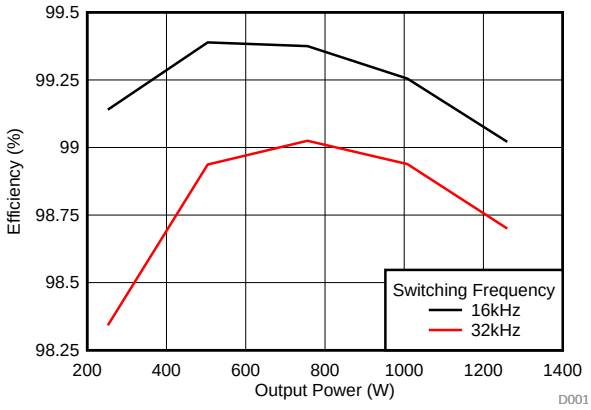


3.2.2 Test Results

3.2.2.1 Efficiency

Figure 18 shows the efficiency vs output power of the TIDA-00915 at two switching frequencies – 16 and 32 kHz and an ambient temperature of 25°C. Peak efficiency at 16 kHz is 99.37% at 750 W and at 32 kHz is 99% at 750 W. Full-load (1.25 kW) efficiency is 99% at 16 kHz and 98.7% at 32 kHz. Such high efficiencies enable GaN inverter operation with a small heatsink and natural convection fanless cooling. IGBT-based inverters cannot reach these high efficiency numbers and hence need a larger thermal system, eliminating possibility of motor integration.

Figure 18. Efficiency vs Output Power - no Airflow



3.2.2.2 Thermal Performance

Figure 19 shows the temperature rise of the GaN module case vs motor phase current at 16 and 32 kHz. During thermal data collection, the ambient temperature was 23°C, DC link input was 300 V, and dead-time was 100 ns. Thermal data was recorded using a thermal imager after steady state was reached following prolonged operation at every current value (minimum of 40 minutes). From the temperature rise data it can be seen that the GaN inverter can supply a maximum current of 3.5 A at 16 kHz, and maximum current of 3 A at 32 kHz in an ambient temperature of 50°C (maximum case temperature limited to 110°C). For an ambient temperature of 85°C, the maximum currents drop to 1.5 A at 16 kHz and 1 A at 32 kHz.

Figure 19. Temperature Rise vs Current - no Airflow

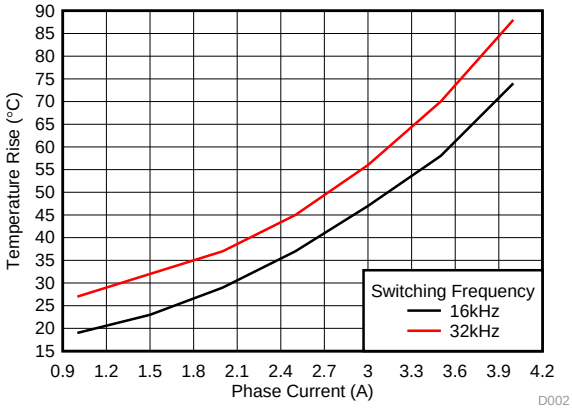


Figure 20 shows the thermal images of different GaN modules at 3.5 A, 16 kHz. The maximum case temperature of 79.7°C is seen in top side GaN modules - bottom side GaN modules are slightly cooler (by 4–5°C) due to more mounting screws giving a better contact. This temperature difference is marginal and does not affect relative lifetime of the GaN modules.

Figure 20. Thermal Data at 3.5 A, 16 kHz

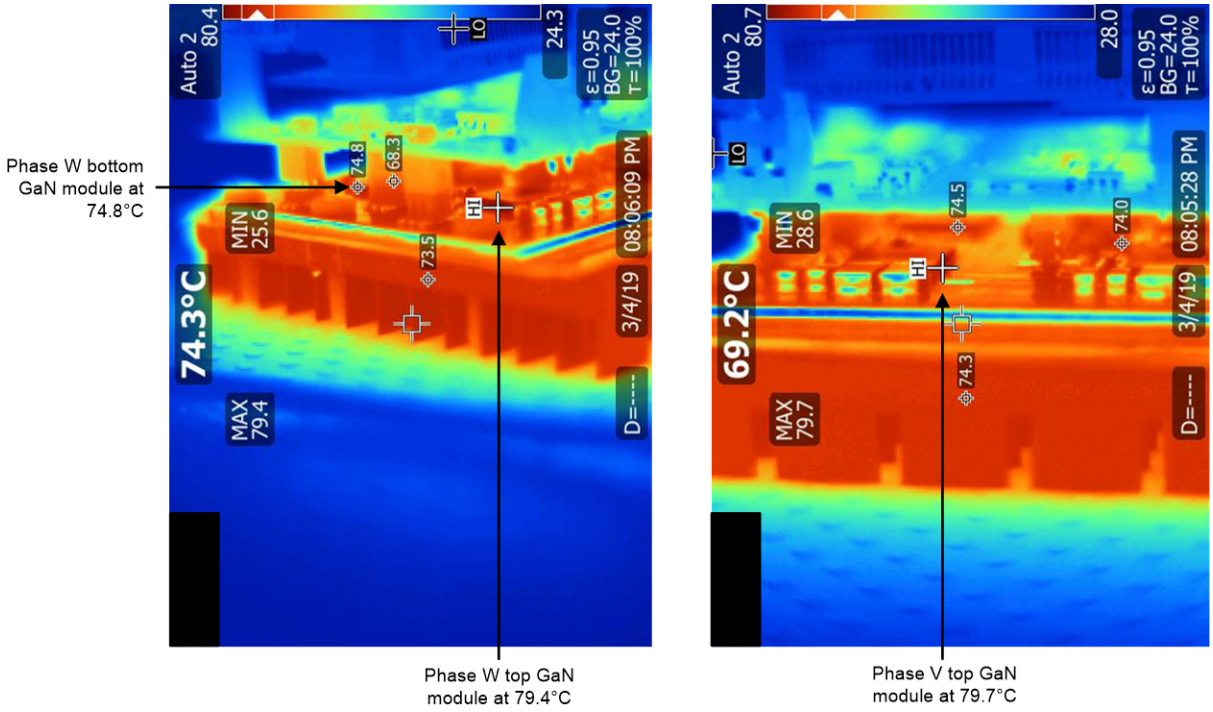


Figure 21 captures similar thermal data but for 1.5 A, 16 kHz. At lower current values, the difference between top and bottom side GaN module temperatures is also lower (2–3°C)

Figure 21. Thermal Data at 1.5 A, 16 kHz

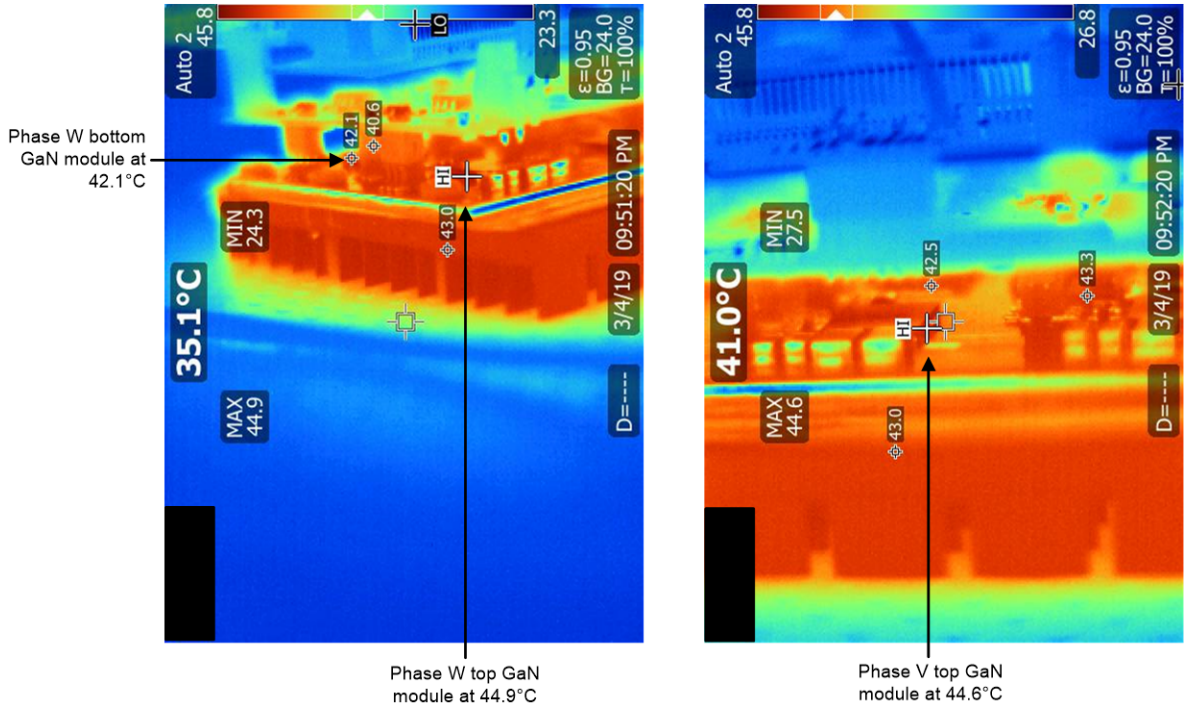


Figure 22 and Figure 23 show thermal data for phase currents of 3.5 A and 1.5 A, respectively, at 32 kHz. Increased switching losses compared to 16 kHz is seen as proportional increase in GaN module case temperature.

Figure 22. Thermal Data at 3.5 A, 32 kHz

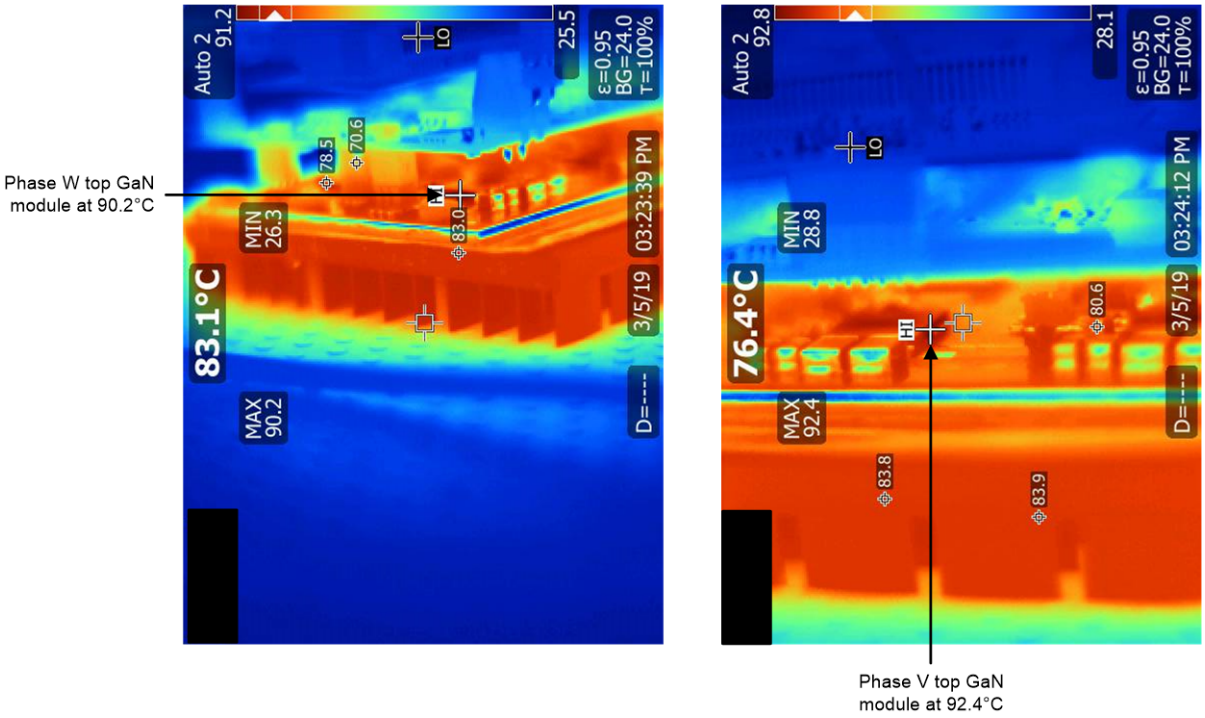
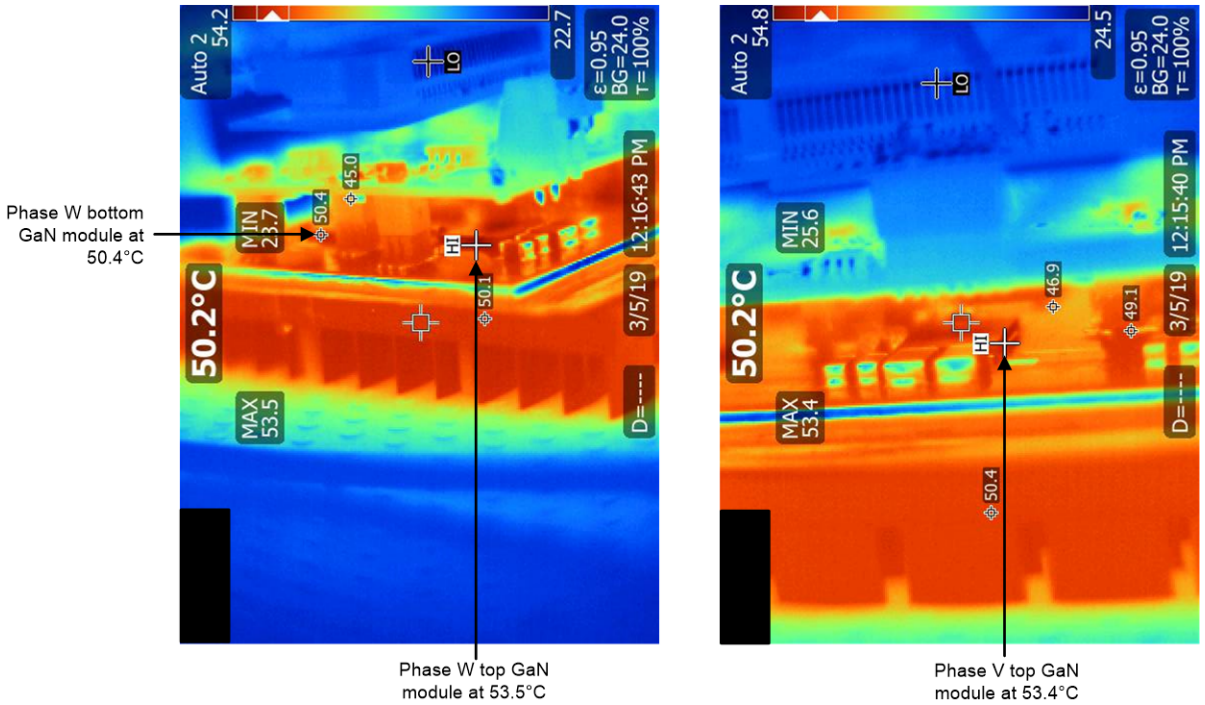


Figure 23. Thermal Data at 1.5 A, 32 kHz



3.2.2.3 Drain Slew Rate

The TI GaN module has a controllable drain slew rate during turn-on transitions. The drain slew rate is set using the RDRV resistor. Higher slew rate reduces switching losses but increases EMI. However, due to the minimal switch node ringing, EMI is significantly reduced and hence higher slew rates can be used to attain better efficiency. Additionally, in motor integrated drives, cables between the motor and drive are much shorter compared to conventional motor-drive system and this enables much higher dv/dt and lower switching losses, due to negligible cable reflected voltage.

Figure 24 shows the drain slew rate during turn-on transition for RDRV of 39 kΩ at 0.3-A drain current. The fall time observed is 5.6 ns, the measured drain slew rate is 180 V / 5.6 ns = 32 V / ns.

Figure 24. Turn-on Transition at 0.3 A

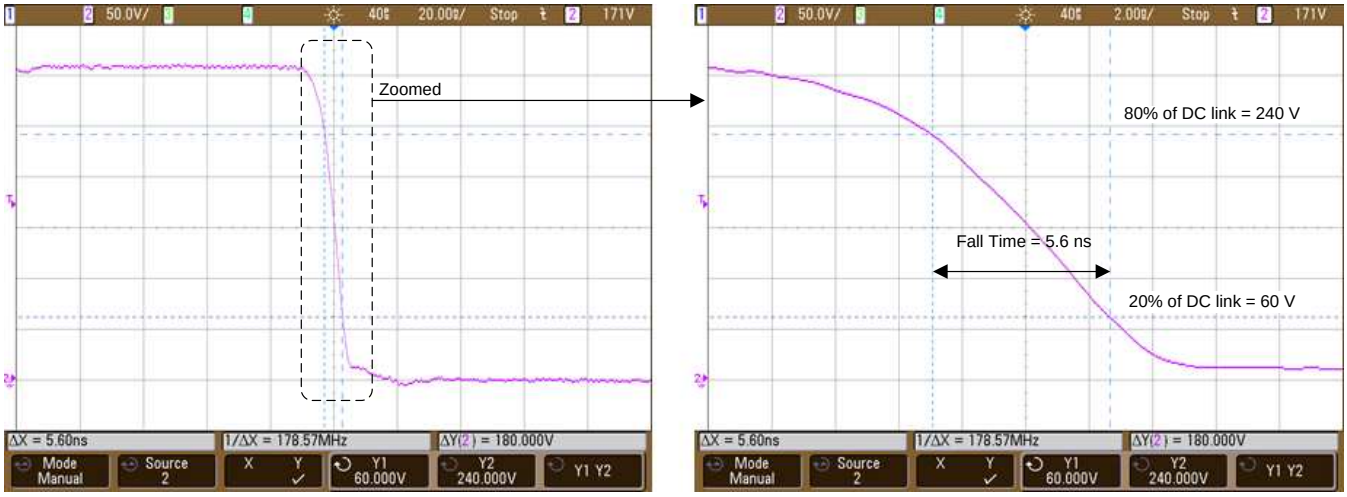


Figure 25 shows the drain slew rate during turn-on transition for RDRV of 39 kΩ at 1.6-A drain current. The fall time observed is 5.5 ns, the same as in the previous case. Similar fall time and drain slew rate as Figure 24 shows that the fall time is controlled solely by RDRV and independent of load current.

Measured slew rate is lower than set value due to additional capacitance at switching node from cables and motor windings.

Figure 25. Turn-on Transition at 1.6 A

Turn-off transitions; however, depend largely on the load current as Figure 26 and Figure 27 illustrate. In Figure 26, the drain current is 0.2 A and the rise time is 4.9 ns; whereas, in Figure 27, the drain current is 1.6 A and the rise time is 3.5 ns.

Figure 26. Turn-off Transition at 0.2 A

Figure 27. Turn-off Transition at 1.6 A

3.2.2.4 Bootstrap Power Supply Ripple

Figure 28 shows the bootstrap V_{DD} ripple at 16-kHz switching frequency and at no-load (1.6 A_{RMS}) . It is seen that at a high duty cycle and negative current, bootstrap V_{DD} falls to it's lowest value of 10.3 V. This is because at negative current V_{DD} is decided only by the bootstrap current and not by third quadrant V_{SD} drop - since diode has a forward drop of 1.6 V at 1.5 A forward current (decided by R_{BOOT} and difference between V_{BOOT} and 12 V) V_{DD} gets charged only to 10.3 V. However, this is within acceptable limits since lowest V_{DD} is well above UVLO (8.5 V).

Conversely, bootstrap V_{DD} reaches its maximum value at positive current - positive current adds the third quadrant V_{SD} drop to the V_{DD} and hence contributes to a V_{DD} higher than theoretical maximum. The maximum bootstrap V_{DD} is directly proportional to deadtime and peak current; hence deadtime should be chosen so as to not increase the V_{DD} above recommended values - GaN modules can take a maximum V_{DD} of 20 V and hence bootstrap V_{DD} should not be allowed to exceed 18 V.

Figure 28. Bootstrap V_{DD} Ripple at 16 kHz

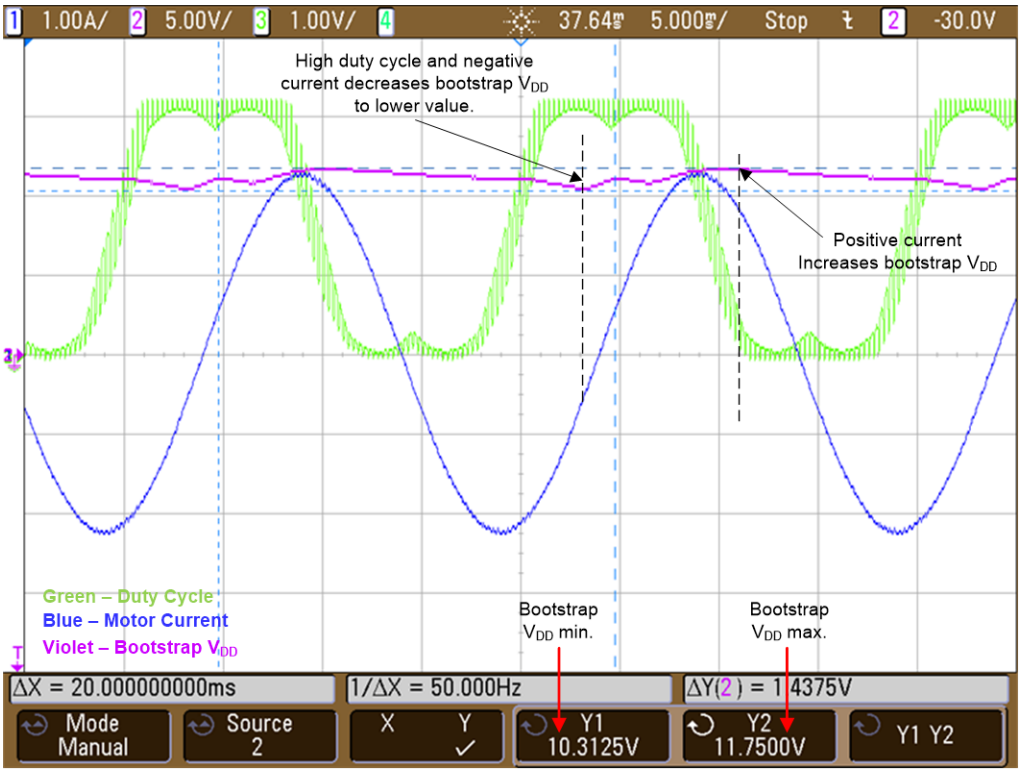
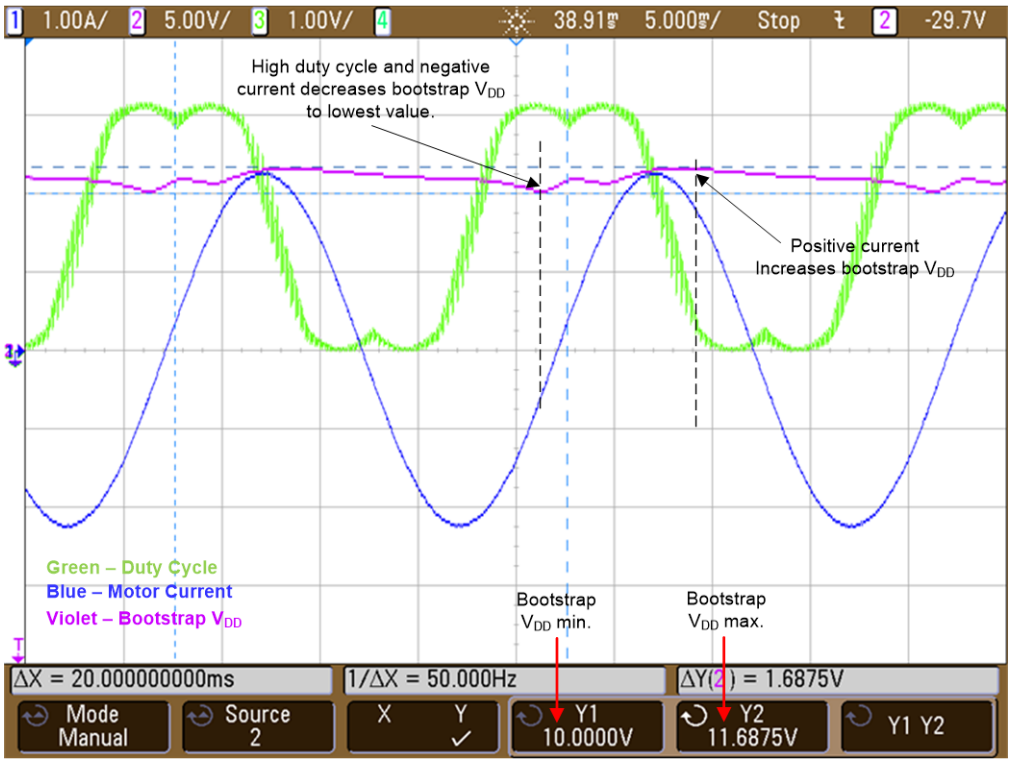


Figure 29 shows a bootstrap V_{DD} ripple at a 32-kHz switching frequency and at no-load (1.6 A_{RMS}). Similar to Figure 29, minimum and maximum V_{DD} occur at high duty cycle, negative current and at positive current, respectively. However, the minimum and maximum values are lower than in Figure 28 due to higher current drawn by the GaN module at a higher switching frequency.

Figure 29. Bootstrap V_{DD} Ripple at 32 kHz



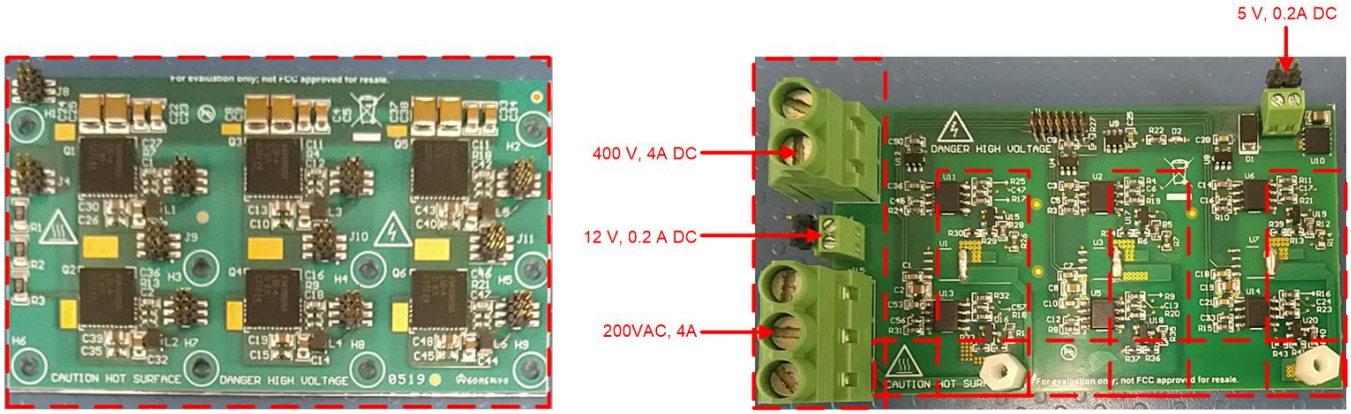
3.2.3 Test Precautions

3.2.3.1 High Voltage (HV)

The TIDA-00915 board works with an HV input of up to 400 V DC. These HV sections are exposed to human contact and hence extreme care must be exercised while testing. The HV areas are marked in the PCB with the text "DANGER HIGH VOLTAGE" and the warning symbol in Figure 30. The HV sections are also marked in Figure 31 with a dotted red rectangle - users must ensure proper HV safety precautions are observed before and while testing. All exposed terminals (high voltage or otherwise) should **not** be handled directly when power is turned on - all connections must be done only in a powered-down state. Figure 31 also shows the voltage, current, and power ratings of all the power connectors of the TIDA-00915 board.

Figure 30. High Voltage Warning

Figure 31. High Voltage Areas on the TIDA-00915



The power supply used to power the DC link, 12-V gate drive power supply, and 5-V bias power need to have suitable current limits set as in Figure 31. This is critical to ensure that the TIDA-00915 board is safe from overtemperature and fire hazards in the event of a short-circuit failure.

3.2.3.2 High Temperature (HT)

During operation at room temperature (25°C), some components and parts of the PCB surface can reach high temperatures (up to 110°C). Some of these are marked on the PCB with the text "CAUTION HOT SURFACE" and the warning symbol in Figure 32. The high temperature areas are also marked in Figure 33 within the red dotted rectangle.

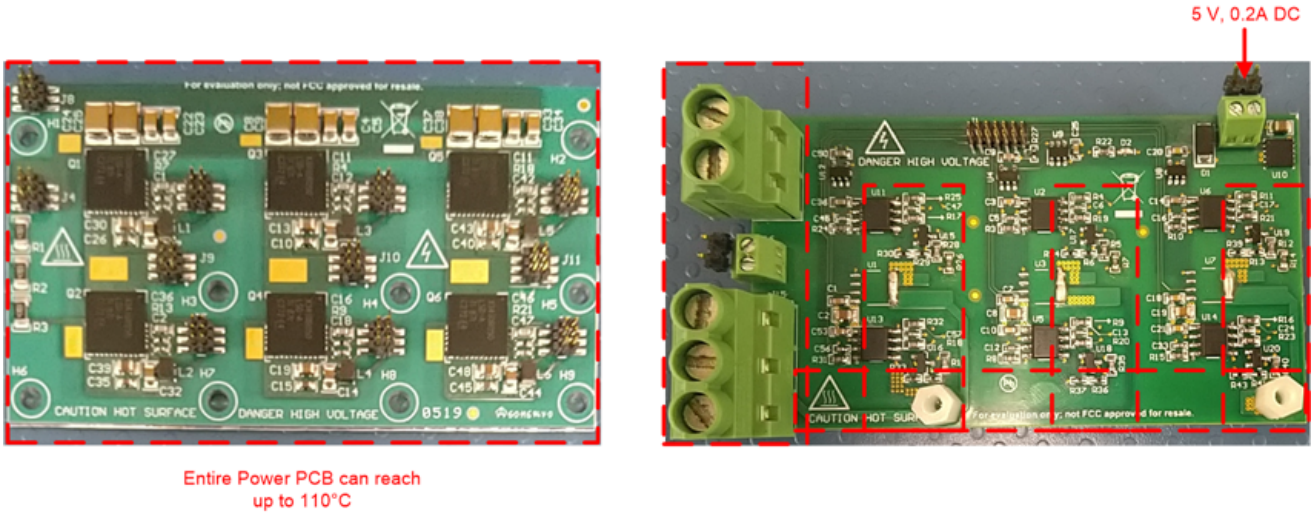
See Figure 20 through Figure 23 in Section 3.2.2.2 for detailed information on the maximum temperature of specific parts and PCB surfaces.

WARNING

Exercise adequate caution during and after testing to avoid burns and other risks linked to high temperature. Also, remember that the components and PCB surface can take a long time (approximately 30 minutes) to cool down to room temperature after shutting down power.

Figure 32. High Temperature Warning

Figure 33. High Temperature Areas on the TIDA-00915



4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-00915.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00915.

4.3 PCB Layout Recommendations

Figure 34. Split Switching Node Planes

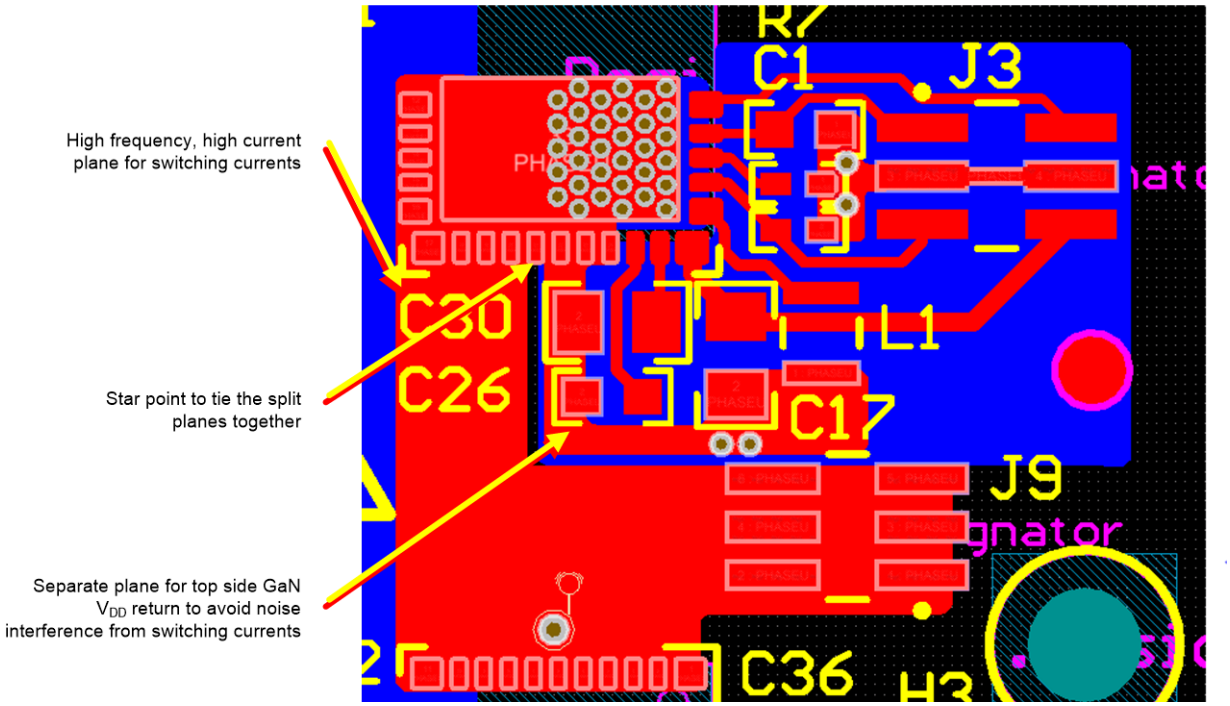
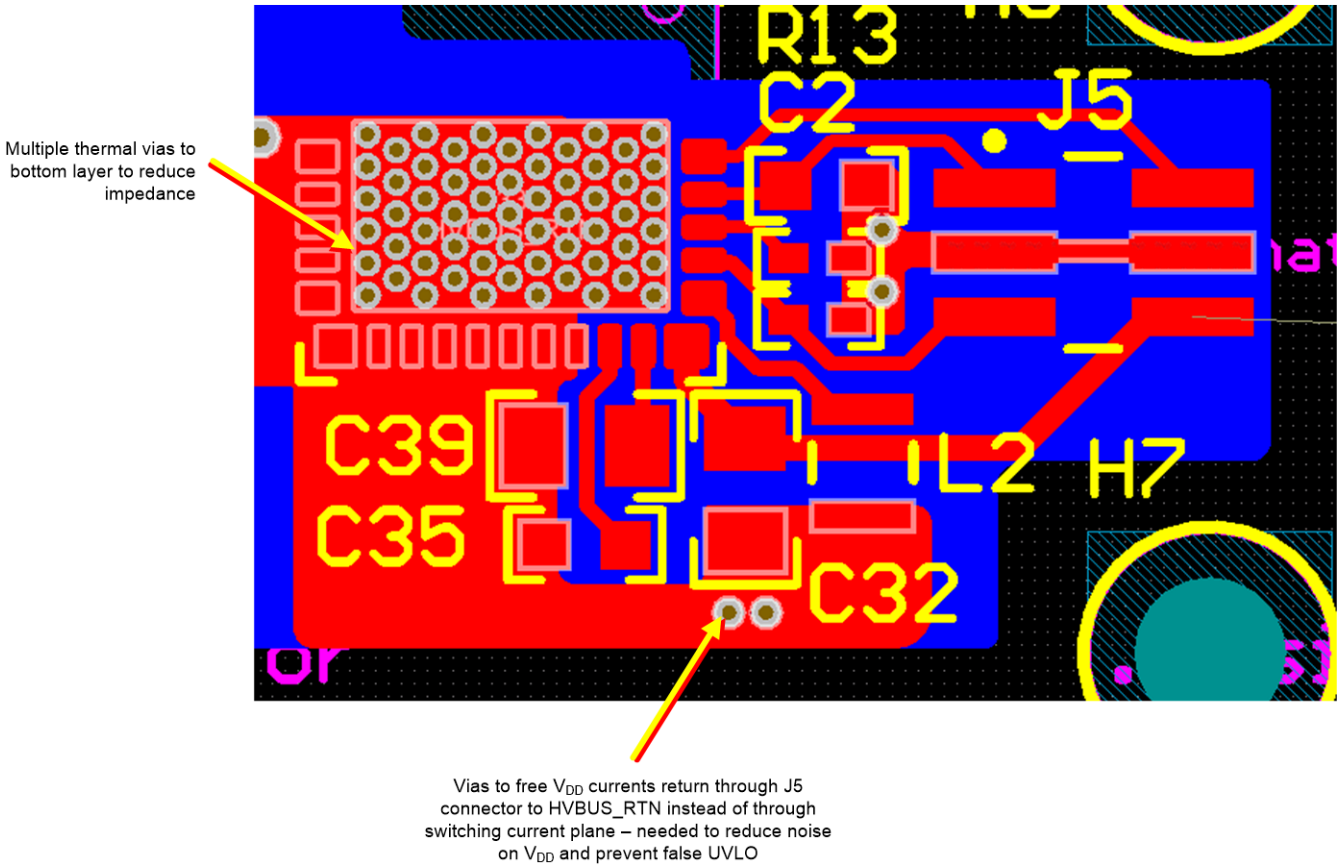


Figure 35. Bottom Side GaN V_{DD} Return



4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-00915.

4.4 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-00915.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00915.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00915.

5 Related Documentation

1. Texas Instruments, *High voltage half bridge design guide for LMG3410x family of integrated GaN FETs application report*
2. Texas Instruments, *GaN FET module performance advantage over silicon white paper*

5.1 Trademarks

C2000 is a trademark of Texas Instruments.
Altium Designer is a registered trademark of Altium LLC or its affiliated companies.

6 Terminology

GaN— Gallium nitride

IGBT— Isolated gate bipolar transistor

UVLO— Undervoltage lockout

CMTI— Common-mode transient immunity

HEMT— High electron mobility transistor

7 About the Authors

SIVABALAN MOHAN is a Systems Engineer at Texas Instruments where he is responsible for developing reference design solutions for industrial drives.

N. NAVANEETH KUMAR is a Systems Manager in the Industrial Systems-Motor Drive team at Texas Instruments, where he is responsible for specifying and developing reference designs for industrial drives.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265