i.MX53 Quick Start Board

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1. Introduction

This document is the Hardware Reference Manual for the i.MX53 Quick Start board based on the Freescale Semiconductor i.MX53 Applications Processor. This board is fully supported by Freescale Semiconductor. This Manual includes system setup and debugging, and provides detailed information on the overall design and usage of the i.MX53 Quick Start board from a Hardware Systems perspective.

1.1. i.MX53-QUICK START Board Overview

The Quick Start Board is an i.MX535 platform designed to showcase many of the most commonly used features of the i.MX535 Applications Processor in a small, low cost package. The MCIMX53-START is an entry level development board and a near perfect subset of its larger sister board, the MCIMX53SMD, which is available as a full, near-form factor tablet. Developers can start working with code on the Quick Start board, and then port it over to the SMD Tablet if additional features are desired. This gives the developer the option of becoming familiar with the i.MX535 Applications Processor before investing a large amount or resources in more specific designs. Features of the i.MX53 Quick Start board are:

Processor:	Freescale Applications Processor	MCIMX535DVV1B
DRAM Memory:	Micron 8Gb DDR3 SDRAM	MT41J128M16HA-187E:D
PMIC:	Dialog Semiconductor	DA9053
Mass Storage:	5 in 1 SD/MMC/SDIO Card Connector microSD Card Connector 7-pin SATA Data Connector	
Video Output:	15-Pin D-Sub VGA Connector 30-Pin LVDS Connector	
Ethernet:	RJ-45 Connector for 10/100 Base-T	
USB:	Dedicated HS USB 2.0 Standard-A Host Connector Shared HS USB 2.0 Standard - Host and Micro-B Device Connectors	
Audio Connectors:	3.5mm Stereo Head Phone output 3.5mm Mono-Microphone input and Mono Head Phone (right channel) output	
Power Connectors:	5V mm Barrel Connector	
Debug Connectors:	9-Pin D-Sub Debug UART Connector 20-Pin Standard ARM JTAG Connector	
Expansion Header:	120-Pin Header (Populated) to Support 1 of the following: Optional HDMI Output Daughter Card (orderable) Optional WVGA and WQVGA LCD Display Daughter Cards (orderable) Camera Daughter Card (custom) SDIO Based WiFi Daughter card (custom)	

User Interface Buttons:	Power, Reset, 2 User-Defined Buttons
Indicators:	8 Status LEDs – External Power, PMIC ON, Fault Condition, and more
Li-ION Battery Connector:	3-Pin Header (unpopulated) for Li-ION Battery for Low Power Operation
Coin Cell:	Connection point for 2-Pin Coin Cell (unpopulated) for RTC Operation
PCB:	3.0 inch x 3.0 inch (76.2 mm x 76.2 mm), 10 - layer board

1.2. i.MX53-QUICK START Board Kit Contents

The i.MX53-Quick Start Board comes with the following items:

- i.MX53-QUICK START Board
- microSD Card preloaded with Ubuntu Demonstration Software
- USB Cable (Standard-A to Micro-B connectors)
- 5V/2.0A Power Supply
- Quick Start Guide
- Documentation DVD

1.3. i.MX53 Quick Start Board Revision History

- Rev A – Proof of Concept
- Rev B – Prototype (Internal Freescale Development)
- Rev C – Prototype (Internal Freescale Development)
- Rev D – Production (Silicon: i.MX53 Rev 2.0, DA9053 Rev AA)
- Rev E – Production (Silicon: i.MX53 Rev 2.0, DA9053 Rev BB)

The board assembly version will be printed on a label, usually attached to the side of the Ethernet/Dual USB Connector (J2). The assembly version will be the letter designation following the schematic revision:

700-26565 REV _

2. List of Acronyms

The following acronyms will be used throughout this document.

AC97	- Audio Codec '97
CMC	- Common Mode Choke
CODEC	- Compression/Decompression
DDR	- Double Data Rate
DNP	- Do Not Populate
HDMI	- High Definition Multimedia Interface
I2C	- Inter-Integrated Circuit
I2S	- Integrated Interchip Sound
IC	- Integrated Circuit
IDE	- Integrated Debug Environment
LAN	- Local Area Network
LCB	- i.MX53 Smart-Start
LCD	-Liquid Crystal Display
LPDDR2	- Low Power DDR2
MMC	- Multi Media Card
PMIC	- Power Management Companion IC
RMII	- Reduced Media Independent Interface
RTC	- Real-Time Clock
SDRAM	- Synchronous Dynamic Random Access Memory
SD	- Secure Digital
SPI	- Serial Peripheral Interface
SSI	- Synchronous Serial Interface
ULPI	- UTMI Low Pin Interface
USB	- Universal Serial Bus
UTMI	- Universal Transceiver Macrocell Interface
WDOG	- Watch Dog
WLAN	- Wireless LAN

3. Specifications

3.1. i.MX535 Processor

The i.MX535 Applications Processor (AP) is based on ARM Cortex-A8^{TM} Platform, which has the following features:

- MMU, L1 Instruction and L1 Data Cache
- Unified L2 cache
- Target frequency of the core (including Neon, VFPv3 and L1 Cache): 1.0 GHz
- Neon coprocessor (SIMD Media Processing Architecture) and Vector Floating Point (VFP-Lite) coprocessor supporting VFPv3
- TrustZone

The memory system consists of the following components:

- Level 1 Cache:
  - Instruction (32 Kbyte)
  - Data (32 Kbyte)
- Level 2 Cache:
  - Unified instruction and data (256 Kbyte)
- Level2 (internal) memory:
  - Boot ROM, including HAB (64 Kbyte)
  - Internal multimedia/shared, fast access RAM (128 Kbyte)
  - Secure/non-secure RAM (16 Kbyte)
- External memory interfaces:
  - 16/32-bit DDR2-800, LV-DDR2-800 or DDR3-800 up to 2 Gbyte
  - 32 bit LPDDR2
  - 8/16-bit NAND SLC/MLC Flash, up to 66 MHz, 4/8/14/16-bit ECC
  - 16-bit NOR Flash. All WEIMv2 pins are muxed on other interfaces (data with NFC pins). I/O muxing logic selects WEIMv2 port, as primary muxing at system boot.
  - 16-bit SRAM, cellular RAM
  - Samsung One NAND^{TM} and managed NAND including eMMC up to rev 4.4 (in muxed I/O mode)

The i.MX53 system is built around the following system on chip interfaces:

- 64-bit AMBA AXI v1.0 bus – used by ARM platform, multimedia accelerators (such as VPU, IPU, GPU3D, GPU2D) and the external memory controller (EXTMC) operating at 200 MHz.
- 32-bit AMBA AHB 2.0 bus – used by the rest of the bus master peripherals operating at 133 MHz.
- 32-bit IP bus – peripheral bus used for control (and slow data traffic) of the most system peripheral devices operating at 66 MHz.

The i.MX53 makes use of dedicated hardware accelerators to achieve state-of-the-art multimedia performance. The use of hardware accelerators provides both high performance and low power consumption while freeing up the CPU core for other tasks.

The i.MX53 incorporates the following hardware accelerator:

- VPU, version 3 – video processing unit
- GPU3D – 3D graphics processing unit, OpenGL ES 2.0, version 3, 33 Htri/s, 200 Mpix/s, and 800 Mpix/s z-plane performance, 256 Kbyte RAM memory.
- GPU2D – 2D graphics accelerator, OpenVG 1.1, version 1, 200 Mpix/s performance.
- IPU, version 3M – image processing unit
- ASRC – asynchronous sample rate converter

The I.MX53 includes the following interfaces to external devices:

NOTE

Not all the interfaces are available simultaneously depending on I/O multiplexer configuration.

- Hard disk drives:
  - PATA, up to U-DMA mode 5, 100 MByte/s
  - SATA II, 1.5 Gbps
- Displays:
  - Five interfaces available. Total rate of all interfaces is up to 180 Mpixels/s, 24 bpp. Up to two interfaces may be active as once.
  - Two parallel 24-bit display ports. The primary port is up to 165 Mpix/s (for example, UXGA @ 60 Hz).
  - LVDS serial ports: one dual channel port up to 165 Mpix/s or two independent single channel ports up to 85 MP/s (for example, WXGA @ 60 Hz) each.
  - TV-out/VGA port up to 150 Mpix/s (for example, 1080p60).
- Camera sensors:
  - Two parallel 20-bit camera ports. Primary up to 180-MHz peak clock frequency, secondary up to 120-MHz peak clock frequency.
- Expansion cards:
  - Four SD/MMC card ports: three supporting 416 Mbps (8-bit i/f) and one enhanced port supporting 832 Mbps (8-bit, eMMC 4.4)
- USB
  - High-speed (HS) USB 2.0 OTG (up to 480 Mbps), with integrated HS USB PHY
  - Three USB 2.0 (480 Mbps) hosts:
    - High-speed host with integrated on-chip high speed PHY
    - Two high-speed hosts for external HS/FS transceivers through ULPI/serial, support IC-USB

- Miscellaneous interfaces:
  - One-wire (OWIRE) port
  - Three I2S/SSI/AC97 ports, supporting up to 1.4 Mbps, each connected to audio multiplexer (AUDMUX) providing four external ports.
  - Five UART RS232 ports, up to 4.0 Mbps each. One supports 8-wire, the other four support 4-wire.
  - Two high speed enhanced CSPI (ECSPI) ports plus one CSPI port
  - Three I2C ports, supporting 400 kbps.
  - Fast Ethernet controller, IEEE1588 V1 compliant, 10/100 Mbps
  - Two controller area network (FlexCAN) interfaces, 1 Mbps each
  - Sony Philips Digital Interface (SPDIF), Rx and Tx
  - Enhanced serial audio interface (ESAI), up to 1.4 Mbps each channel
  - Key pad port (KPP)
  - Two pulse-width modulators (PWM)
  - GPIO with interrupt capabilities
  - Secure JTAG controller (SJC)

The system supports efficient and smart power control and clocking:

- Supporting DVFS (Dynamic Voltage and Frequency Scaling) and DPTC (Dynamic Process and Temperature Compensation) techniques for low power modes.
- Power gating SRPG (State Retention Power Gating) for ARM core and Neon
- Support for various levels of system power modes.
- Flexible clock gating control scheme
- On-chip temperature monitor
- On-chip oscillator amplifier supporting 32.768 kHZ external crystal
- On-chip LDO voltage regulators for PLLs

Security functions are enabled and accelerated by the following hardware:

- ARM TrustZone including the TZ architecture (separation of interrupts, memory mapping, and so on)
- Secure JTAG controller (SJC) – Protecting JTAC from debug port attacks by regulating or blocking the access to the system debug features.
- Secure real-time clock (SRTC) – Tamper resistant RTC with dedicated power domain and mechanism to detect voltage and clock glitches.
- Real-time integrity checker, version 3 (RTICv3) – RTIC type 1, enhanced with SHA-256 engine
- SAHARAv4 Lite – Cryptographic accelerator that includes true random number generator (TRNG)
- Security controller, version 2 (SCCv2) – Improved SCC with AES engine, secure/nonsecure RAM and support for multiple keys as well as TZ/non-TZ separation.
- Central Security Unit (CSU) – Enhancement for the IIM (IC Identification Module). CSU is configured during boot and by e-fuses and determines the security level operation mode as well as the TrustZone (TZ) policy.
- Advanced High Assurance BOOT (A-HAB) – HAB with the next embedded enhancements: SHA-256, 2046-bit RSA key, version control mechanism, warm boot, CSU and TZ initialization.

3.2. DDR3 DRAM Memory

The i.MX53-Quick Start board uses four 2-Gigabit DDR3 SDRAM ICs manufactured by Micron for a total onboard RAM memory of 1 GigaByte. The SDRAM data width for each IC is 16-bits. The chips are arranged in pairs that are controlled by each of the two chip select pins to form 32-bit words for the i.MX53 CPU. On Die Termination (ODT) functionality has been implemented on the board, as well as the ability to separate out the I/O Voltage Supply from the main SDRAM Voltage Supply if desired.

3.3. Dialog DA9053 PMIC

The DA9053 device is a small (7 x 7 mm, 0.5mm pitch) 169 ball VFBGA that provides nearly all power supply functions for the Quick Start board. The following is a feature list of the major functionality provided by the DA9053 PMIC for the Quick Start board:

- Power Supply resources:
  - 12 Low Drop Out (LDO) regulators
    - 1 for internal PMIC purposes only (LDOCORE)
    - 1 for charging optional back up coin cell
    - 10 for platform needs
  - 4 DC/DC Buck Converters (3 with DVS)
    - 1 for the ARM Core supply (VBUCKCORE)
    - 1 for the Peripheral Core supply (VBUCKPRO)
    - 1 for the external SDRAM memory (VBUCKMEM)
    - 1 for the internal cache memory (VBUCKPERI)
  - 1 White LED driver and boost converter
- Li-ION battery Charger
- Resistive touch screen interface
- Expansion Port Card ID detect
- Wall voltage supply over-voltage protection
- 1 HS-I2C interface
- External LDO regulator enable

3.4. MicroSD Card Slot (J4)

The microSD Card slot is used as the primary means to boot the Quick Start board. The power source for the microSD Card slot is VLDO3_3V3. The microSD Card slot is not normally configured with a card detect feature. The MicroSD Card slot can be configured to boot from a MMCmicro card with an alternate boot option setting (see section on Boot Options).

3.5. SD Card Slot (J5)

The SD Card slot is a 5-in-1 SD/MMC connector that acts as a secondary external memory media slot. The power source for the SD Card Slot is the auxiliary LDO regulator (DCDC_3V2). The SD Card slot can be configured as the boot source with an alternate boot option setting, as well as being configured for either SD or MMC card operation (see section on Boot Options). The SD Card Slot supports full 8-bit parallel data transfers and can support SDIO cards (WiFi, BT, etc) designed to fit in a standard SD card slot. The Quick Start board has specifically been tested with an Atheros SD-25 WiFi card.

3.6. SATA 7-pin Data Connector (J7)

The SATA connector provides the means to connect an external SATA memory device to the Quick Start board. Commonly, this would be an External hard drive or a DVD/CD reader. Power for the SATA device needs to be supplied externally by the user via a 12-pin power connector. It is possible to boot from a SATA drive by making OTP fuse changes. Once the fuse changes are made, they cannot be reversed.

3.7. VGA Video Output (J8)

A standard VGA signal is output directly from the i.MX53 Processor with minimum external components required. Power for the TVE module of the i.MX535 Processor is supplied by VLDO7 of the PMIC and is set to 2.75V. If VGA output is not desired, it is possible to program the PMIC to turn off VLDO7 to conserve power. The VGA output supports a variety of video formats up to 150 Mega-Pixels per second. Level shifters are required on the Horizontal and Vertical Synchronization signals as well as the VGA I2C communications signals in order to meet VGA specifications.

3.8. LVDS Video Output (J9)

The LVDS module of the i.MX53 Processor is connected to a 30-pin LVDS connector. While the i.MX53 Processor is capable of outputting to two separate LVDS displays, only one connector is pinned out on the Quick Start board. The pin outs on the LVDS connector match the optional cable and 10" HannStar LVDS display that can be purchased optionally from Freescale. The single LVDS connector will support video formats up to 165 Mega-Pixels per second. The power source for the LVDS module is a switchable output of the VBUCKPERI DCDC converter. This rail is shared with the SATA module and the USB module. If these modules are not being used, the PMIC can be programmed to turn off power to these three modules without affecting other 2.5V supplies to the remainder of the i.MX53 Applications Processor.

3.9. Ethernet (J2B)

The i.MX53 Processor Fast Ethernet Module outputs RMII formatted signals to an external Ethernet PHY. The processor is capable of 10/100 Base-T speeds. The Quick Start board uses the SMSC LAN8720A Ethernet Transceiver in a QFN-24 package. 3.2V power is supplied to the Ethernet IC from the external LDO regulator. The output of the Ethernet PHY is connected to an RJ45 jack with integrated magnetic.

3.10. Dual USB Host Connector (J2A)

The USB module of the i.MX53 Processor provides two high speed USB PHYs that are connected to each of the USB-A Host Jacks on connector J2. One PHY provides Host-only functionality and is connected to the upper USB jack on the connector tower. The second PHY is USB 2.0 OTG capable and is connected to the lower USB jack on the connector tower. Both jacks receive 5V power directly from the 5V Wall Power Supply, via a FET that can be controlled by software, and a 1.1A Poly-fuse. The PMIC provides an over-voltage functionality to limit voltage applied to the USB jack in the event that a DC Power Supply other than the original supply provided is used. Also, there is no current regulating device to limit current supplied to each jack, other than the Poly-fuse.

NOTE

The lower USB Host Jack is cross connected with the Micro-B USB Device connector. This was done as a convenience to the user as cables with micro-A plugs are still uncommon at the time the board was designed. The USB OTG PHY will switch to 'device' mode if a USB Host is attached to the micro-B connector with a cable. This design is not recommended for release to the general electronics consumer population. This board has not been tested for USB compliance.

3.11. Micro-B USB Device Connector (J3)

The micro-B USB connector is connected to the USB OTG PHY on the i.MX53 Processer, and is also connected to the Lower USB Host Jack on the connector tower. The connector's external USB 5V power pin is connected to the USB_OTG_ID pin, which is normally pulled to ground via a 3.3K Ohm resistor. When a powered USB Host device is attached to the micro-B USB connector, the USB_OTG_ID pin is pulled high and sends a signal to the USB OTG PHY to operate in device mode. The connector's external USB 5V power pin is not connected to the PMIC, or any other power rails on the Quick Start board. Therefore, it is not possible to supply power to the Quick Start board via the USB connections.

3.12. Audio Input/Output (J6/J18)

Analog audio input and output are provided by Freescale's Low Power Stereo Codec, SGTL5000. The audio codec is connected to the i.MX53 Applications Processor via 4-wire I2S communications, utilizing the AUDMUX5 port of the processor. The audio codec's Headphone Amp provides up to 58 mW output to 16-Ohm headphones at a typical SNR of 98 dB and THD+N of -86 dB. Typical power consumption is 11.6 mW. In addition, the audio codec can perform several enhancements to the output including virtual surround, added bass and three different types of equalization. The Microphone Input module of the Stereo Codec is also used, with the microphone input connected to the tip pin of the Microphone Jack (J6). Microphone Bias voltage is applied on the Quick Start board and not as a separate connection to the Microphone Jack. If the user desires to use a combined microphone, mono headphone device, the ferrite bead on L25 can be moved to the L22 pads, redirecting the right channel output to the Microphone Jack. A 2.5mm to 3.5mm adapter may be necessary to convert the microphone, mono headphone device to fit the Microphone Jack. On both the Headphone Jack and Microphone jack, a fourth pin is used to detect the insertion of a plug into either jack. When a standard 3-pin device is inserted into the 4-pin jack, the detect line is grounded, indicating to the i.MX53 Processor that the plug has been inserted.

3.13. 5V Power Connector (J1)

A 2.0mm x 6.5mm barrel connector is used which should fit standard DC Plugs with an inner dimension of 2.1mm and an outer dimension of 5.5mm. If an alternate power supply is used (not the original, supplied power supply), it should supply no more than 5.25V / 3A output. If the PMIC senses too high voltage at the connector input, it will turn off isolation FET Q1 to protect the Quick Start board. In between the Power Connector and the isolation FET is a single blow, fast acting fuse to protect the Quick Start board from an over current situation fault. If a Wall Power Supply is properly connected to the Quick Start board, and the green 5V power LED indicator is not lit, it could mean that either the fuse has been blown, or that the voltage output of the power supply is too high.

3.14. Debug UART Connector (J16)

UART1 of the i.MX53 Processor is connected to an RS-232 output to be used as a debug output for the developer. The Transmit (TX) and Receive (RX) signals are sent through two 1.8V to 3.2V level shifters to convert the logic signal voltages to the correct values for the Sipex SP3232 RS-232 transceiver. The CTS and RTS signals are not used on the Quick Start board. The RS-232 transceiver receives its power from the external 3.2V LDO Regulator. If the output of the regulator is turned off for power savings measures, debug output will be lost.

If the designer wishes to use the port as an Applications UART Port, changes can be made in software to reconfigure the port. A male-to-male gender changer can be used to properly convert the port.

To access the debug data output during development, connect the Debug UART Connector to a suitable host computer and open a terminal emulation program (ie, Teraterm or HyperTerminal). Proper settings for the terminal program are:

- BAUD RATE: 115,200
- DATA: 8 bit
- PARITY: None
- STOP BIT: 1-bit
- FLOW CONTROL: None

3.15. JTAG Connector (J15)

A standard 20-pin ARM JTAG connector is provided on the Quick Start board. Logic signals to the JTAG connector are 1.8V signals. A 1.8V reference signal is provided to pin 1 of the connector so that the attached JTAG tool can automatically configure the logic signals for the right voltage. If the JTAG tool does not have an automatic logic voltage sense, make sure that the tool is configured for 1.8V logic.

JTAG tools that have been specifically tested with the Quick Start board are:

- JTAG Commander (Macraigor)
- DS-5 and RealView (ARM Ltd.)
- Trace32 (Lauterbach)
- J-Link (Segger/Codesourcery)
- J-Link (IAR)

3.16. Expansion Header (J13)

A 120-pin Expansion Port Header is provided on the Quick Start board for use with many optionally expansion boards available from Freescale, or for custom designed boards made be the developer. At the time of initial production, the following expansion boards are available from Freescale:

- MCIMXHDMICARD — HDMI signal output daughter card
- MCIMX28LCD — 4.3" WVGA Touch Panel LCD Display

The Expansion Port makes the following features of the i.MX53 Processor available to be used on a custom built expansion card:

- Two Serial Peripheral Interfaces (SPI) — CSPI, eCSDPI2
- Two I2S/SSI/AC97 Ports — AUDMUX4, AUDMUX5
- Two Inter-Integrated Circuits (I2C) — I2C1, I2C2
- 2 UARTs — UART4, UART5
- SPDIF Audio
- USB ULPI Port — USBH2
- 24-bit Data and display control signals
- Resistive Touch Screen Interface
- Various Voltage rails

3.17. User Interface Buttons

There are four user interface buttons on the Quick Start board. Their functionality is as follows:

POWER: In the 'Power Off' state, momentarily pressing the POWER button will begin the PMIC power on cycle. The PMIC supplied voltage rails will come up in the proper sequence to power the i.MX53 Processor. When the processor is fully powered, the boot cycle will be initiated.

In the 'Power On' state, momentarily pressing the POWER button will send a signal to a GPIO port for user defined action, but will not initiate a hardware shutdown.

In the 'Power On' state, holding the power button down for greater than 5 seconds will result in the PMIC initiating a shutdown to the 'Standby' power condition. This will also be the result from the 'Power Off' state as the PMIC will transition into the 'Power On' state and will still see the POWER button as held down.

RESET: Pressing the RESET button in the 'Power On' state will force the i.MX53 Applications Processor to immediately turn off, and reinitiate a boot cycle from the Processor Power Off state. The RESET button has no effect on the PMIC or the voltage rails.

Pressing the RESET button when the Quick Start board is powered off will have no effect.

USERDEF1:
USERDEF2: These two buttons are user defined buttons attached to PATA_DATA14 (P6) for USERDEF1 and PATA_DATA15 (P5) for USERDEF2. The two GPIO pins are normally pulled high by an internal resistor. The two buttons function by connecting the pins to ground, thus inserting a low signal. The developer is left to determine the actions of these two pins in code. Sample codes do not assign functionality to either pin.

3.18. User Interface LED Indicators

There are eight LED status indicators located next to the microSD card connector. These LEDs have the following functions:

5V: The 5V status LED (D1) is a Green LED connected directly to the 5V_MAIN power rail. This LED indicates that 5V wall power is being properly supplied to the Quick Start board. If this light is not lit, it would indicate one of three problems:

1) Fuse F1 has been blown and needs to be replaced.
2) Voltage from the wall supply is greater than 5.5V and the over voltage protection feature is disabling power to the board.
3) The DC Power supply is not plugged in or malfunctioning.

PMIC: The PMIC status LED (D9) is a Green LED gated by the PMIC SYS_UP signal from the PMIC. This LED indicates that the PMIC is in the fully on condition and supplying power to the processor and other voltage rails as directed by software.

USER: The User status LED (D16) is a Green LED gated by the PATA_DATA1 (L3) GPIO pin. The developer is left to determine the action of this pin in code. Sample codes do not assign functionality to the pin. The LED comes on by default when the processor starts up.

FLT: The FLT status LED (D14) is a Red LED gated by the NVDD_FAULT signal from the PMIC. The LED will turn on anytime the PMIC is not outputting the requested voltages or when the PMIC senses a fault condition and will begin to power down the voltage rails. This may aid in trouble shooting power problems if both the PMIC and FLT LEDs are on at the same time, it indicates that the PMIC is causing a shutdown based on a fault it has sensed.

3.3V: The 3.3V status LED (D10) is a Blue LED gated by the External Regulator 3.2V power rail. This power rail can be turned off by software for power savings measures. This LED provides an easy visual recognition as to the status of this bus.

SATA: The SATA status LED (D11) is a Blue LED gated by the SATA_1V3 (VLDO5) power rail. This power rail can be turned off by software for power savings measures. This LED provides an easy visual recognition as to the status of this bus.

VGA: The VGA status LED (D12) is a Blue LED gated by the TVDAC_2V75 (VLDO7) power rail. This power rail can be turned off by software for power savings measures. This LED provides an easy visual recognition as to the status of this bus.

LCD: The LCD status LED (D13) is a Blue LED gated by the LCD_3V2 power rail. Normally the LCD_3V2 power rail receives power directly from the DCDC_3V2 power rail, but the LCD can also be configured to receive power from VIOHI_2V772 (VLDO4). In the alternate voltage supply configuration, this LED will provide visual recognition as to the status of the LCD bus.

3.19. Optional Li-ION Battery Connector (J14)

On the Quick Start board, there is a footprint (J14) available to solder a three pin wafer connector (Molex 0530470310 or equivalent). This connector will mate to Li-ION batteries commercially available as replacement batteries to commonly available MP3 players. The developer should make sure that the polarity of the battery matches the polarity of the connector as replacement batteries may vary from different manufacturers. When installed, a battery can be charged from the external 5V wall power source. A battery will not be charged when only a USB cable is connected to the Quick Start board. When powering a board from only a battery, the 5V power rail and the DCDC_3V2 power rail will not be powered. Therefore, the Ethernet subsystem and Audio subsystem will not be operational under normal board configurations. Depending on the battery capacity, it may be necessary to power down additional subsystem voltage rails to extend battery life to a usable amount.

The battery charging feature is an autonomous operation of the Dialog DA9053 PMIC that does not require software support. Battery charging may be prevented by software by making registry changes to the PMIC. The developer may need to verify in software that PMIC registry settings are proper for battery charging operations. The footprints for testing with a battery were included for skilled developers looking to experiment.

3.20. Optional Back-Up Coin Cell posts (JP1, JP2)

On the Quick Start board, there are two through-holes (JP1 and JP2) next to the power connector. These through-holes are positioned to hold a Lithium coin cell battery (Sanyo ML1220-VM1 or equivalent). For proper operation, the coin cell posts should be soldered direction to the Quick Start board, with the positive terminal connected to JP1 and the negative terminal connected to JP2. The DA9053 PMIC will charge the coin cell when 5V Wall Power is available. When 5V Wall Power is removed, the coin cell will provide power only to the RTC power rail (VLDO1) supplying power to the i.MX53 processor. The length of time a coin cell can power the RTC subsystem may vary.

3.21. PCB Shorting Traces

On the Quick Start PCB, there are 29 sets of standard footprints with a copper trace between them to short the two pads together. The PCB is produced with these pads unpopulated. These shorting traces are placed throughout the PCB at locations in line with major power rails and critical components. The purpose of these shorting traces it to allow the skilled developer to manually cut the trace between the pads to either:

1) Isolate power to major subsystems or components.
2) Install small value precision resistors to measure current consumption of major subsystems.
3) Or reconfigure power sources to subsystems or components using wires soldered to the pads.

To restore a shorting trace back to normal after the trace is cut, it is only necessary to solder a Zero Ohm resistor to the pads.

4. Quick Start Board Connectors and Expansion Port

The Quick Start board provides a number of connectors for a variety of inputs and outputs to and from the board. The following subsections describe these connections in detail.

4.1. Wall 5V Power Jack (J1)

The 5V/2A AC-to-DC power supply that comes with the Quick Start board is plugged into the Power Jack (J1) on the board as show in **Figure 1**. If the original power supply is lost, it is possible to use a substitute power supply for the Quick Start board. Voltage above 5.5V, and below 12V, will trigger the Over-Voltage protection circuitry on the board. It is not recommended to use a higher voltage since, in the event of a failure to the protection circuitry, damage to the board will result. A voltage supply above 12V will damage the PMIC part.

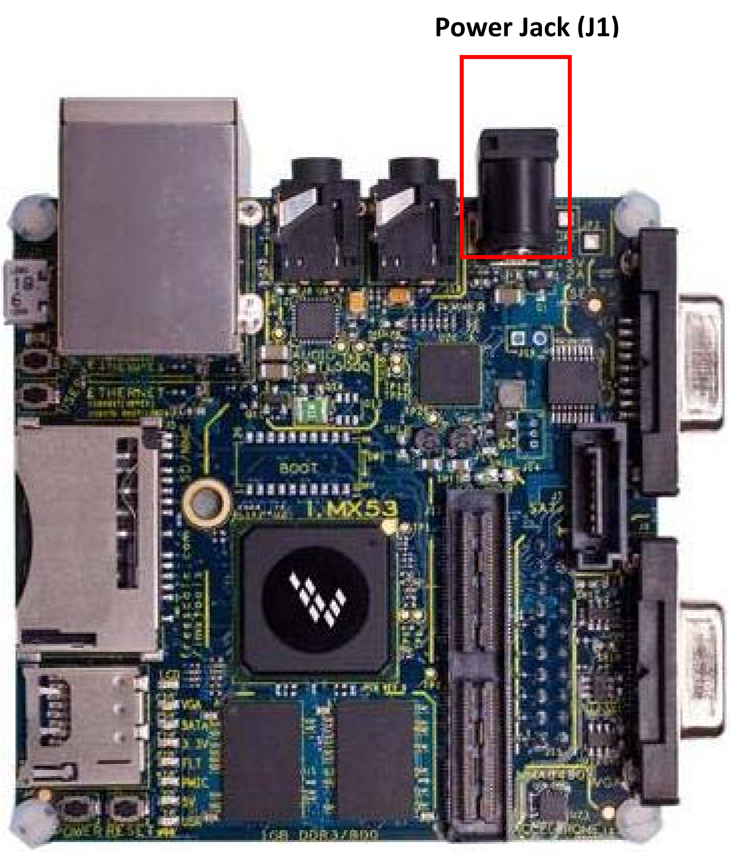


Figure 1. DC Power Jack

4.2. RJ45 Ethernet Connector (J2B)

A standard Cat-V Ethernet cable is attached to the Quick Start board at the Ethernet/Dual USB connector J2. The connector contains integrated magnetic which allows the Ethernet IC to auto configure the port for the correct connection to either a switch or directly to a host PC on a peer-to-peer network. It is not necessary to use a crossover cable when connecting directly to another computer. The Ethernet/Dual USB connector is shown in **Figure 2**.

Ethernet/Dual USB Connector (J2)

Figure 2a. Ethernet Port

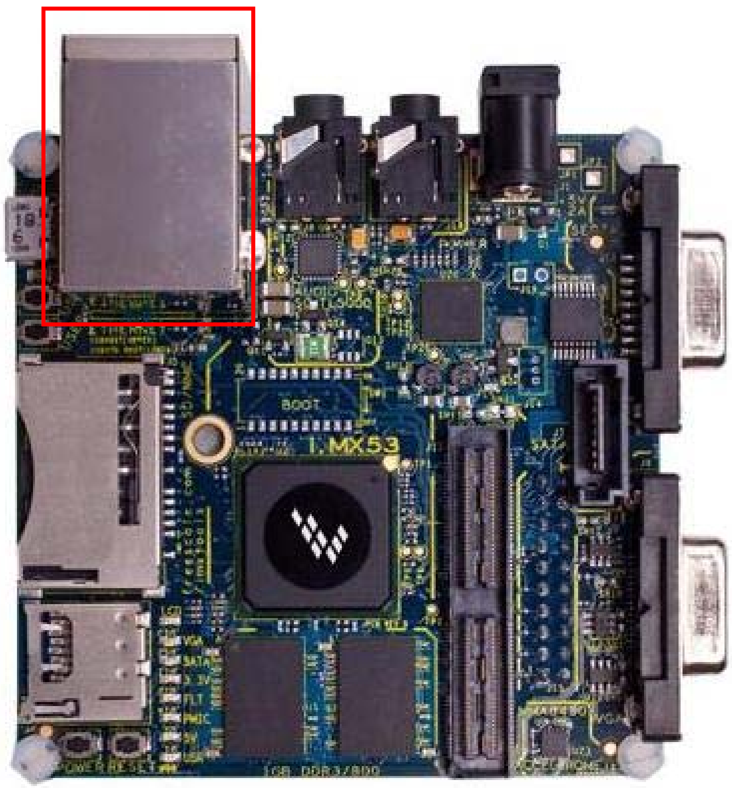


Figure 2. RJ45 Ethernet Connector

4.3. VGA DB15 Connector (J8)

To connect the Quick Start board to a computer monitor in the base configuration, a VGA cable is required. Connect the free end of the VGA cable to connector J8 to the point shown in **Figure 3**.

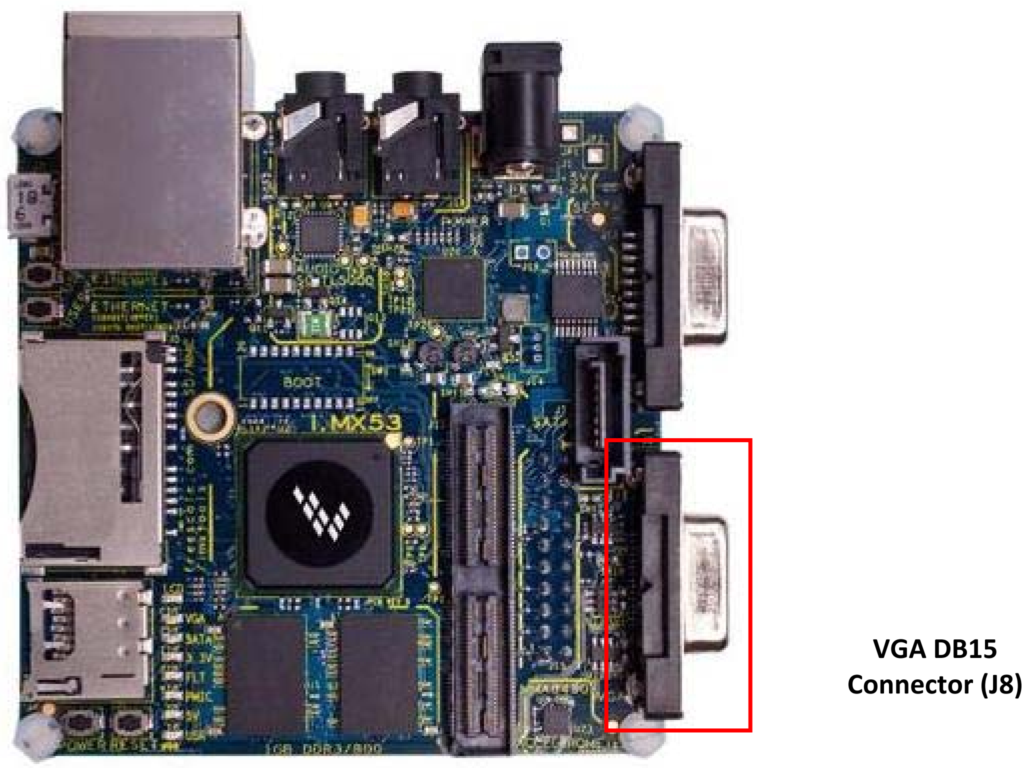


Figure 3. VGA Connector

4.4. Debug UART DB9 Connector (J16)

To connect a host PC to the Quick Start board to receive Debugging information, a Null Modem serial cable is required. This cable is not supplied with the Quick Start kit. The male plug end of the serial cable is connected to the board at the point shown in **Figure 4**. The other end of the serial cable is connected to a PC. For newer generation computers that do not have a serial port, a USB-to-Serial cable can be used. There is no need for any special cabling to support debug information output.

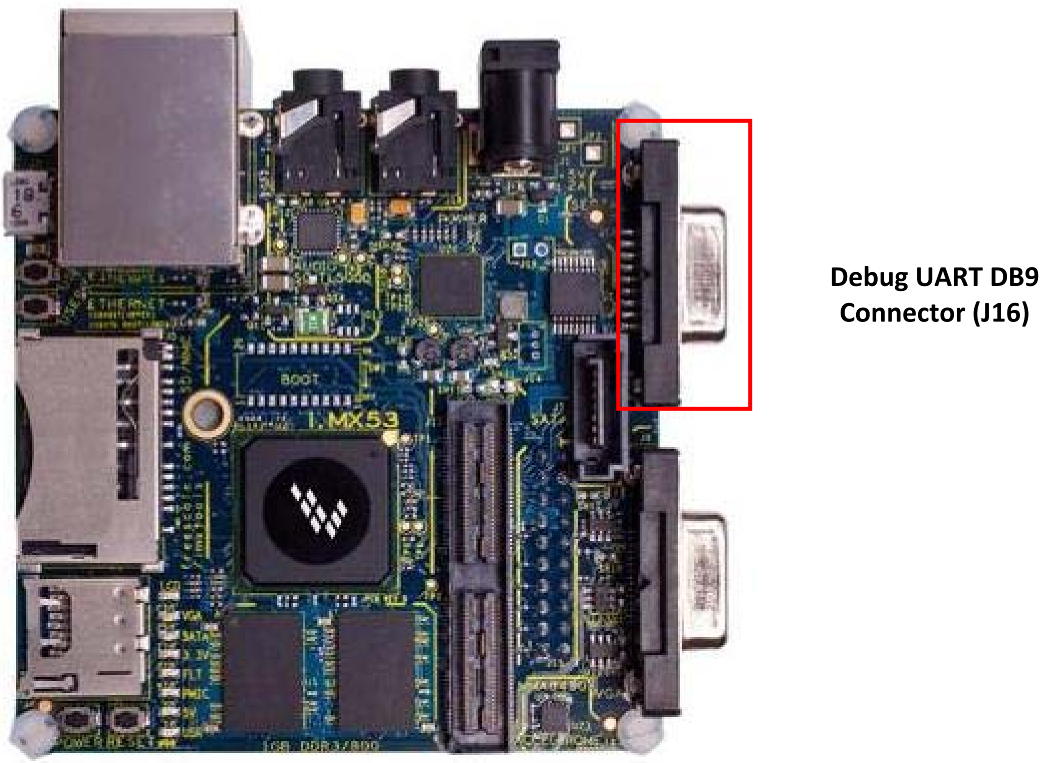


Figure 4. Debug UART Connector

4.5. Headphone Output Connector (J18)

Any set of ear buds or head phones with a standard 3.5mm stereo jack can be connected to the Audio Output jack at the point shown in **Figure 5.** Ear buds are not supplied as part of the Quick Start kit.

Head Phone Connector (J18)

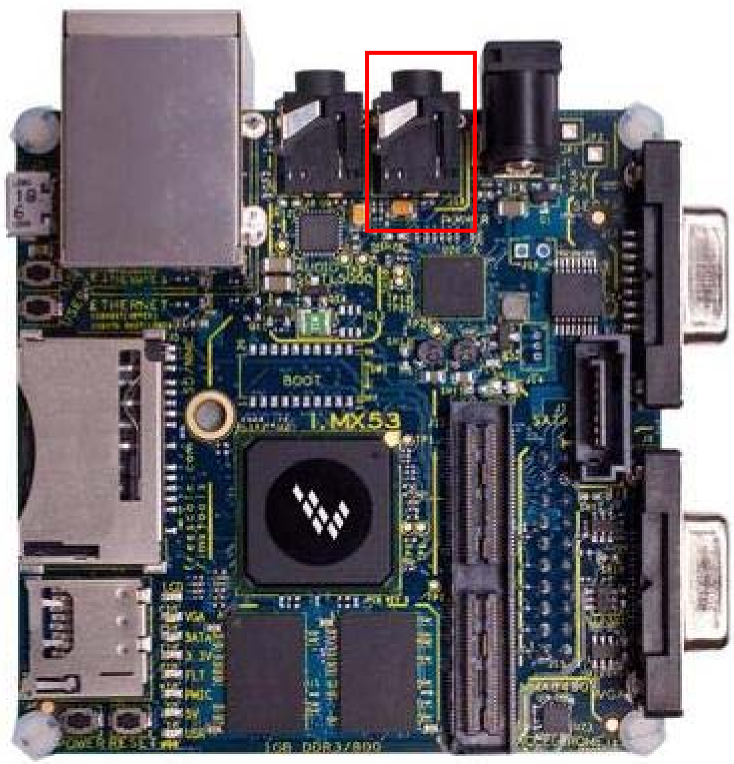


Figure 5. Headphone Output Connector

4.6. Microphone Input Connector (J6)

The Quick Start board provides a 3.5mm stereo connector for a microphone input. The microphone is not provided as part of the Quick Start kit. The developer has several choices as to the type of device plugged into this connector. A mono microphone will input its signal though the tip of the 3.5mm plug. The microphone bias is applied on the Quick Start board, therefore a microphone which uses a wire to send the bias signal to the actual condenser is not necessary, but will not interfere with the microphone operation. The Quick Start board can also be configured for use with a microphone/mono-output ear bud commonly used on cellular phones. To have right channel sound output on this connector, it would be necessary for the developer to move the ferrite bead from the L25 pads and solder it to the L22 pads. This will remove the signal from the headphone output connector. The developer may also find it necessary to use a 2.5mm to 3.5mm adapter with most cellular microphone/earphone sets. As manufactured, the developer may also use a two plug headphone, microphone set commonly used for VOIP services on a PC. The microphone is connecter at the point shown in **Figure 6.**

Microphone Connector (J6)

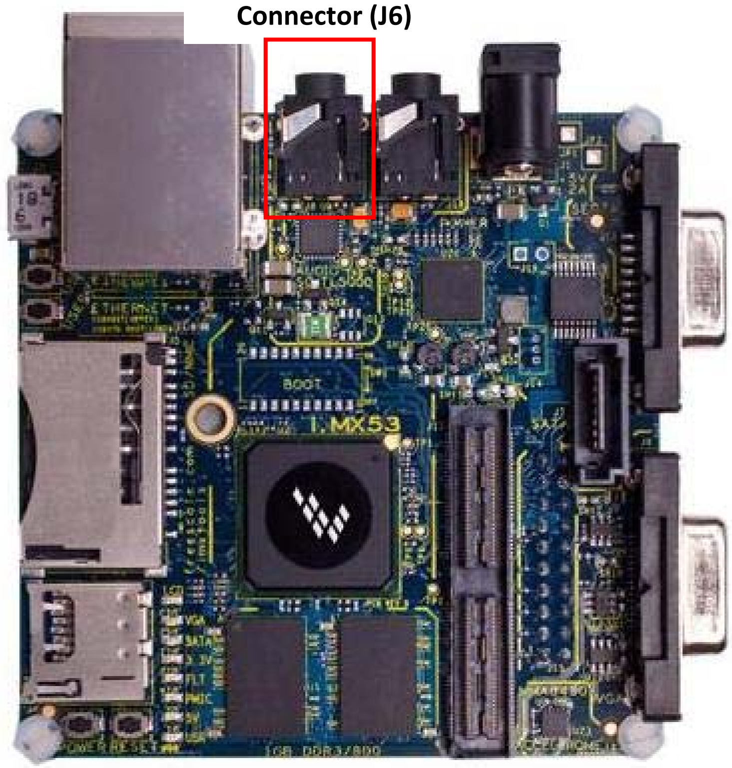


Figure 6. Microphone Connector (J6)

4.7. Dual USB Host Jack (J2)

The Quick Start board has two USB Host only connectors that can be used to support USB devices. The upper USB port is connected to the High-speed (HS) USB 2.0 module of the i.MX53 processor and can support; 1) Any single, high-power USB device, 2) Any combination of USB devices though a self-powered hub not to exceed 500 mA current draw, or 3) Any combination of USB devices through a powered hub. The lower USB port is connected to the High-speed (HS) USB 2.0 OTG module of the i.MX53 processor and is cross-connected with the micro-B USB device connector (J3). As long as the Quick Start board is not connected to a USB Host device through the micro-B USB connector, the same combinations of USB devices can be used on the lower port as used on the upper port. The lower USB port requires configuration as a Host port in software, and is not available as a Host port during the initial boot sequence. USB cables can be inserted into the Dual USB connector at the point shown in **Figure 7**.

Ethernet/Dual USB Connector (J2)

Figure 7a. USB Connectors

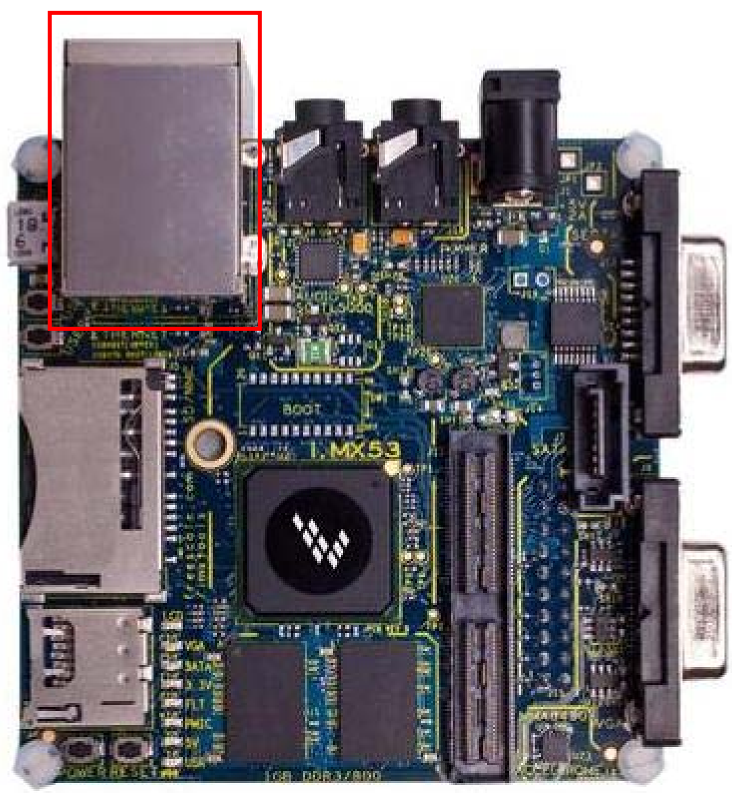


Figure 7. Dual USB Host Connectors (J2)

4.8. micro-B USB Device Connector (J3)

The Quick Start board has one micro-B USB device connector that can be used to connect the Quick Start board to a USB Host computer. The micro-B connector is connected to the High-speed (HS) USB 2.0 OTG module of the i.MX53 processor and is cross connected with the lower USB Host port on J2. When a 5V supply is seen on the micro-B connector (from the USB Host), the i.MX53 processor will configure the OTG module for device mode, which will prevent the lower USB Host port from operating correctly. The 5V power provided by the attached USB Host is only used by the i.MX53 processor for sensing that the host is present. The Quick Start board will not draw power from the connected USB Host and will not operate without a 5V DC power source or charged Li-ION battery. The micro-B connector is keyed and will not accept a micro-A plug from a cable. A micro-B to USB-A cable is supplied as part of the Quick Start kit and can be inserted into the micro-B USB connector at the point shown in **Figure 8**.

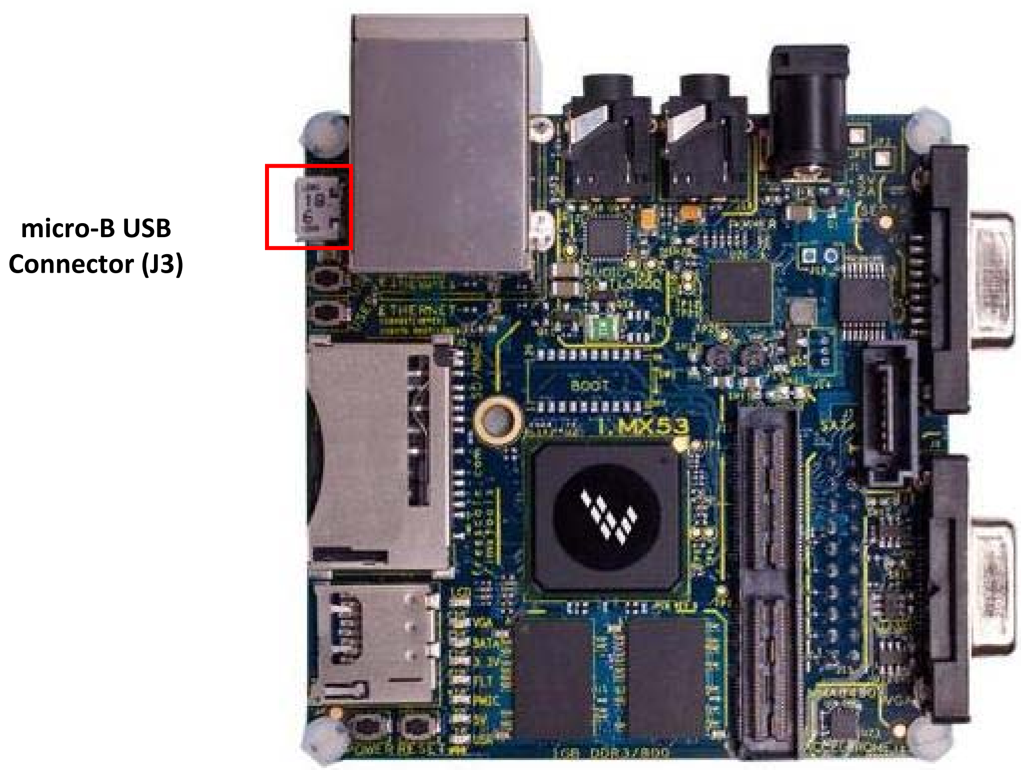


Figure 8. micro-B USB Device Connector (J3)

4.9. SATA 7-pin Data Connector (J7)

A SATA 7-pin Data connector (J7) is provided on the Quick Start Board and is connected to the SATA module of the i.MX53 processor. The Quick Start board is capable of communicating with any standard SATA device, such as a hard drive or optical DVD/CD reader. The SATA device, SATA cables and power supply for the SATA device are not provides as part of the Quick Start kit and are the responsibility of the developer. It is possible to initiate a boot from an attached SATA device. See the software reference manuals for instructions on how to configure the Quick Start board for SATA boot. The SATA Data cable is plugged into the Quick Start board at the location shown in **Figure 9**.

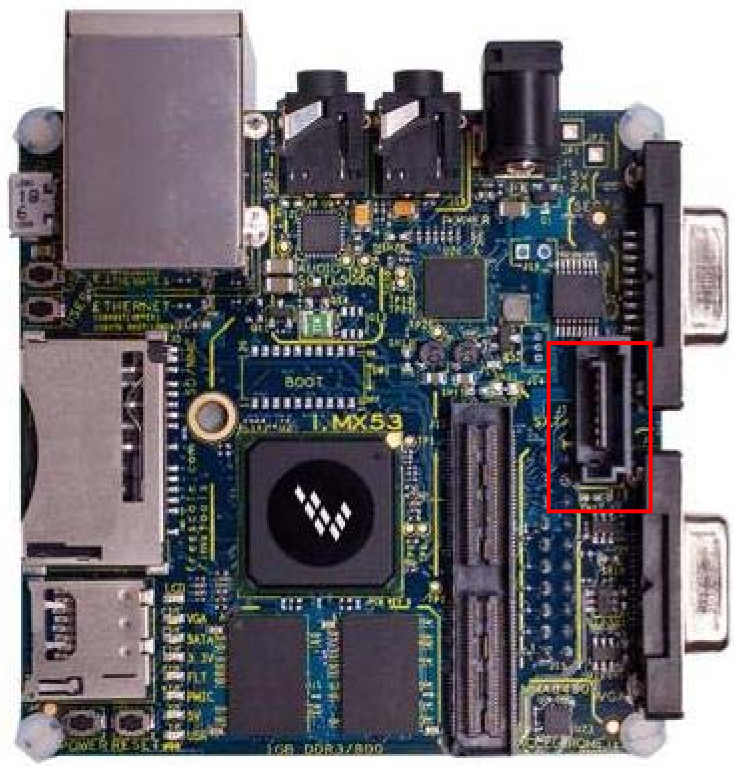


Figure 9. SATA Data Connector (J7)

4.10. SD Card Connector (J5)

The Quick Start board has one full size SD/MMC connector that can be used for memory, or for third-party SDIO type cards such as WiFi or Bluetooth. The SD Card Connector (J5) connects a full 8-bit parallel data bus to the SD3 port of the i.MX53 processor. The SD Card Connector receives power from the DCDC_3V2 power rail supplied by the supplementary Voltage Regulator. The Quick Start board does not come pre-configured to boot from the full size SD Card Connector, but the board can be modified to support booting from this connector instead of the microSD Card Connector. See the section on Quick Start boot options on how to make the necessary changes (Section 5.4.2). The SD Card Connector is not spring loaded, so pushing the card into the slot will not initiate an action to disengage the SD Card. The SD Card is inserted facing up at the location shown in **Figure 10**.

SD Card Connector (J5)

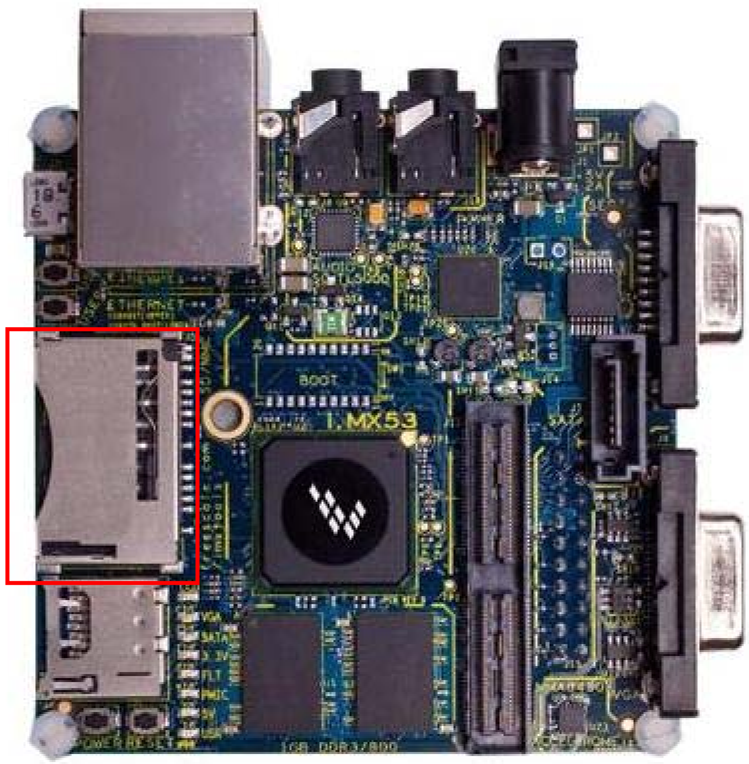


Figure 10. SD Card Connector (J5)

4.11. microSD Card Connector (J4)

The Quick Start board has one micro SD/MMC connector that can be used for memory. The micro SD Card Connector (J4) connects a 4-bit parallel data bus to the SD1 port of the i.MX53 processor. The micro SD Card Connector receives power from the VLDO3 power rail. The Quick Start board comes configured to boot from the micro SD Card Connector by default. The micro SD Card Connector is spring loaded and will eject a properly inserted card if the card is pushed in again. Caution: If the card is ejected while serving as the file system, the processor will undergo a software crash. The micro SD Card is inserted facing up at the location shown in **Figure 11**.

microSD Connector (J4)

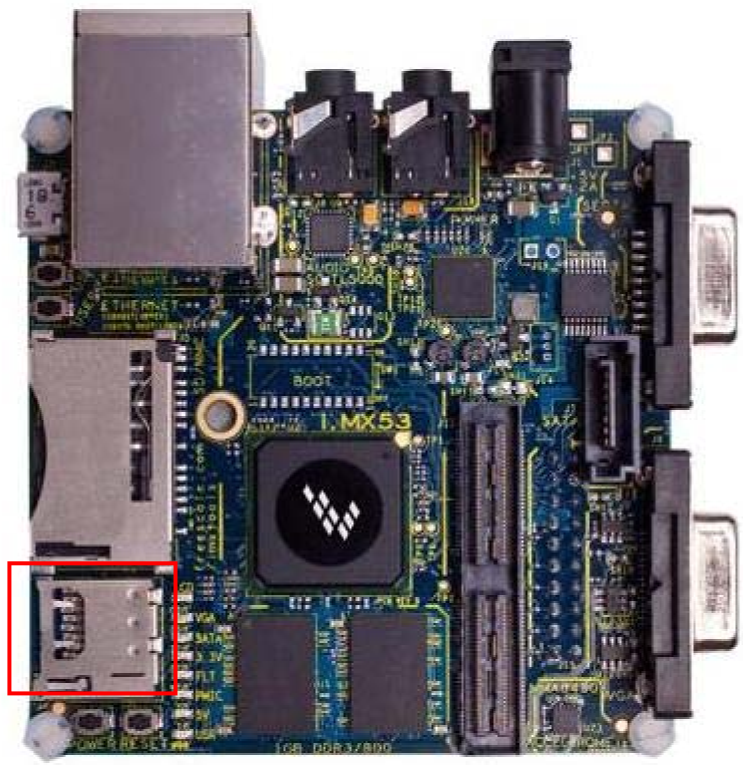


Figure 11. microSD Card Connector (J4)

4.12. 20-pin ARM JTAG Connector (J15)

The Quick Start board contains a standard 20-pin ARM JTAG connector (J15) for advanced debugging with a third-party emulator. The header is configured for use with 1.8V data signals. The developer should exercise caution when selecting the appropriate debugging tools. If an emulator set for 3.3V power and data is connected to the Quick Start board, the i.MX53 processor will be damaged. The emulator JTAG cable is connected to the bottom side of the Quick Start board at the location shown in **Figure 12**.

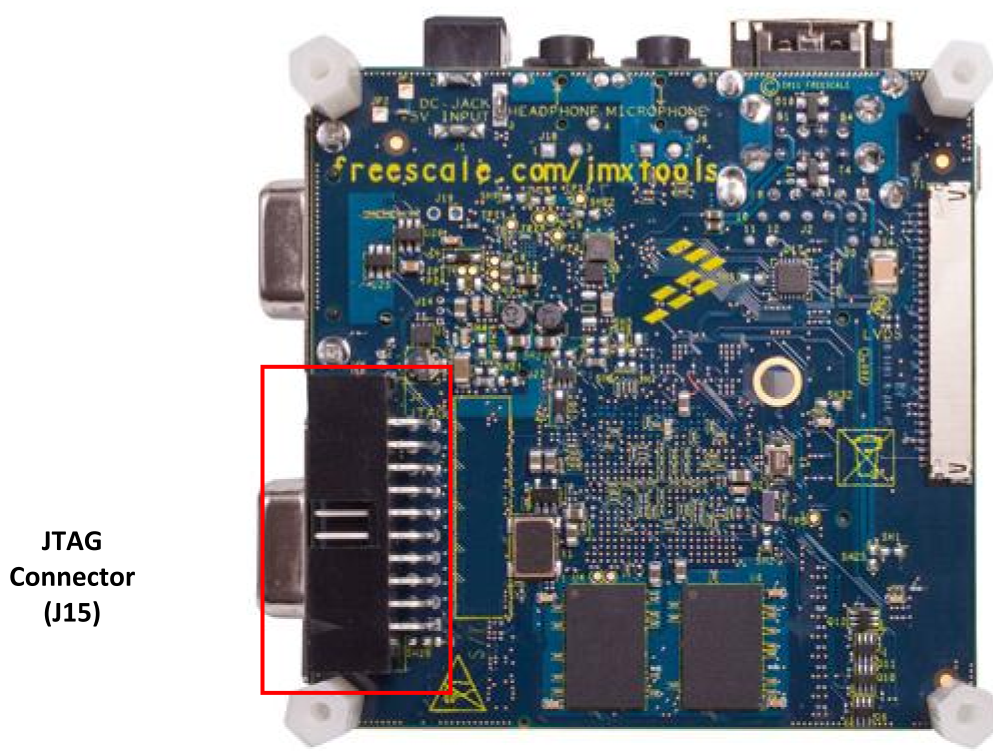
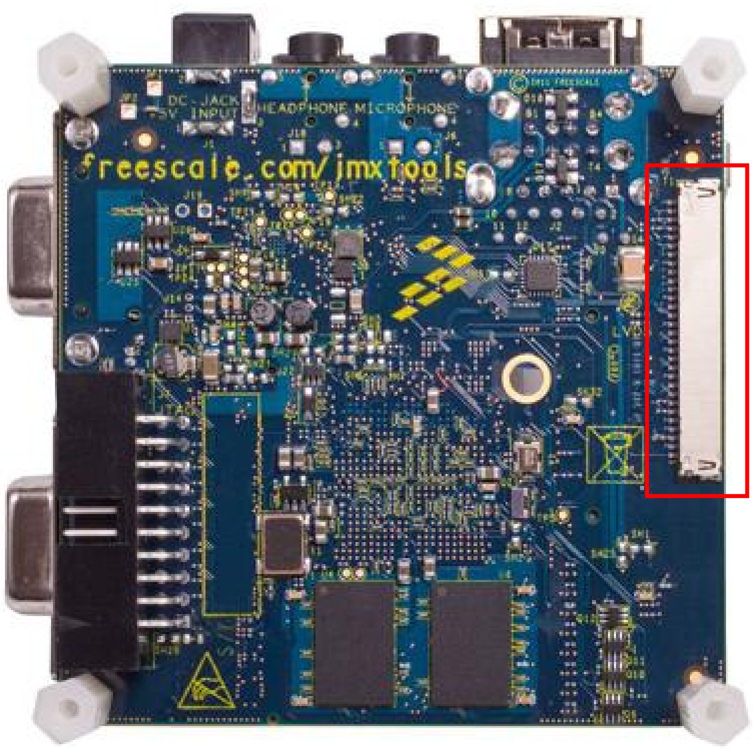


Figure 12. JTAG Connector (J15)

4.13. LVDS Connector (J9)

The Quick Start board includes a 30-pin (Hirose, DF19G-30P-1H(56)) connector for use with an LVDS display. The developer can create custom cables that will allow the Quick Start board to be used with a wide variety of commercially available LVDS displays. The pin-out for this connector is used on other Freescale designed boards in the i.MX53 series, such as the MCIMX53SMD tablet. Freescale has available a cable and LVDS display (HannStar, HSD100PXN1-A00-C11) for purchase if the developer wishes to use a pre-tested configuration. The LVDS display can be used in conjunction with the optional LCD display, the VGA output or the optional HDMI card, as long as the total video output does not exceed the specified limits of the i.MX53 processor. The pin-out table for the connector is located in different section of this user guide. This connector is located on the bottom side of the board in the location shown in **Figure 13.**



LDVS Connector (J9)

Figure 13. LDVS Connector (J9)

5. Quick Start Board Architecture and Design

This section is designed to provide the developer detailed information about the electrical design and practical considerations that went into the Quick Start board. This section is organized to discuss each block in the following high level block diagram of the Quick Start board, as shown in **Figure 14**.

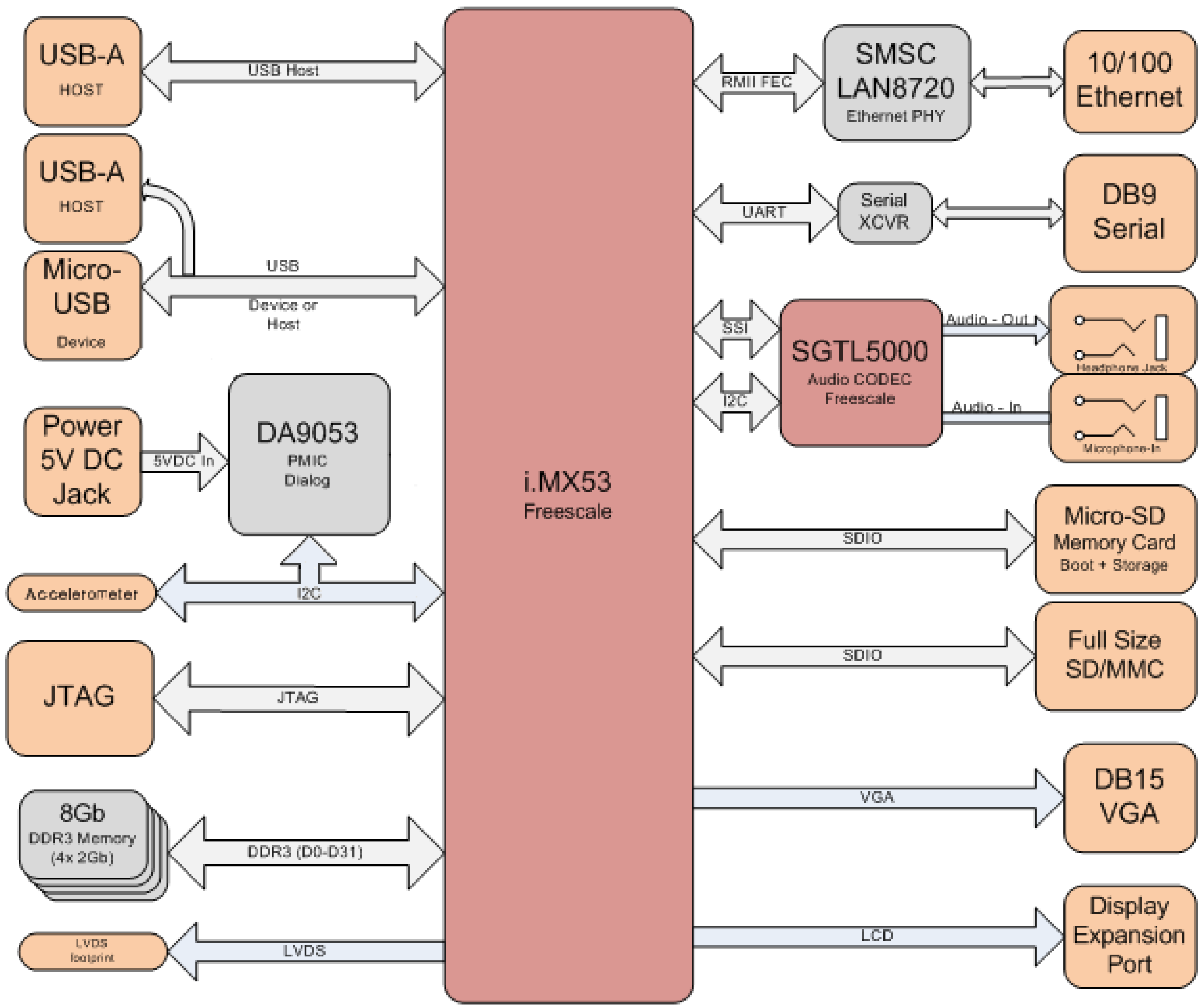


Figure 14. i.MX53 Smart-Start Block Diagram

5.1. 5V Power Supply

5V power from an external wall power supply is connected to the Quick Start board at connector J1. From the connector, the 5V supply is sent directly to a 3A over current protection fuse (F1). In between the connector and the fuse, there are two capacitors to bleed off voltage transients and a single trace that leads to the sense pin for the over-voltage protection circuitry of the Dialog PMIC. From the protection fuse, the 5V supply is connected to the over-voltage protection POWERFET Q1 which is controlled by the PMIC. This circuit limits to a very small area of the Quick Start board the physical location of where unprotected 5V power can reach. The 5V_MAIN power seen by the rest of the Quick Start board is protected from over-voltage and over-current. The circuit is shown below in **Figure 15.**

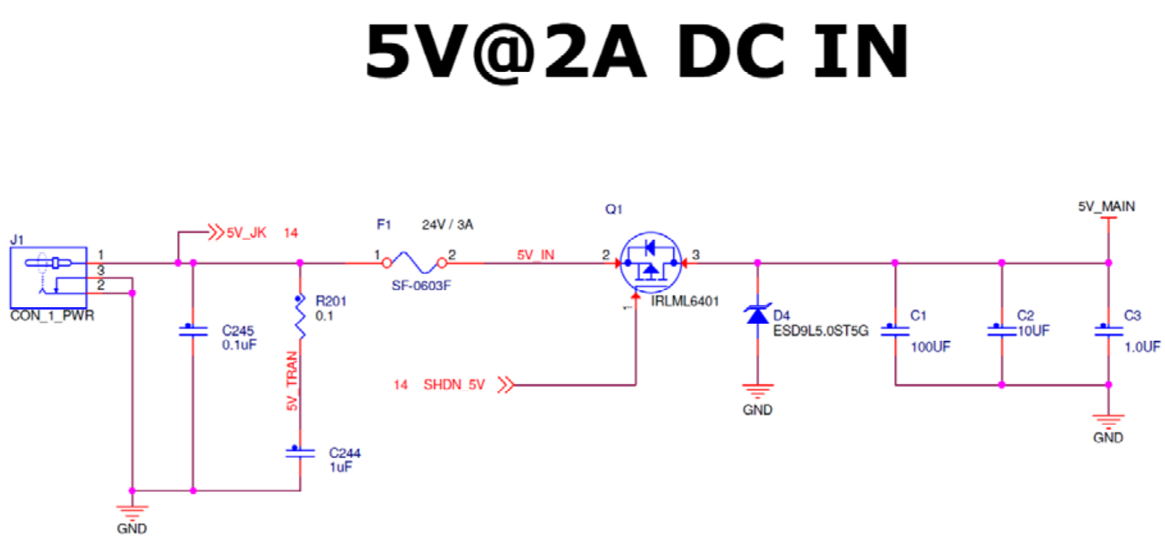


Figure 15. Board Main Power Circuit.

5.2. Dialog DA9053 PMIC

The Dialog PMIC provides all regulated power to the Quick Start board with the exception of a supplemental 3.2V/1A voltage regulator. Physically, the PMIC is located in the upper right corner of the Quick Start board, as close to the power connector as possible, while still maintaining room for supporting components. From this location, power is supplied to the rest of the board.

When 5V power is first attached to the Quick Start board, the PMIC will remain in an OFF state until the POWER button is pressed. In the OFF state, the PMIC will generate power on the VDDOUT rail at approximately 3.6V (different if Li-ION battery attached) for use by the PMIC as a supply for all regulators. In addition, the PMIC generates a VDDCORE voltage of 2.5V for internal PMIC use, and to serve as a pull-up source for the nONKEY/KEEPACT and nSHUTDOWN control inputs. This ensures that these two button are active whenever power is available to the Quick Start boar.

When the POWER button is initially pressed, the PMIC senses the Active Low signal on the nONKEY pin and begins to power on all voltage rails in preprogrammed sequence. The sequence is determined primarily by the order in which power must be supplied to the i.MX53 processor. Once the core operations of the processor are fully powered, other power rails are turned on.

The first voltage regulator to power on is always VLDO1. This regulator supplies a maximum of 40 mA current at 1.3V and powers on only the Secure RTC module of the i.MX53 Processor. This turns on the RTC Clock (32.768KHz) and Watch Dog features. In the event a System Reset is triggered, or the Quick Start board is placed into Standby, VLDO1 will remain powered ON. The only time that VLDO1 will turn off is if all power is removed from the Quick Start board, or if a software command is sent to the PMIC to turn off VLDO1. In the case that a developer attaches an optional coin cell to JP1/JP2, the coin cell will provide power to keep VLDO1 operating.

The power sequence requirements for the i.MX53 Applications Processor from the data sheet are as follows:

1. NVCC_SRTC_POW (VLDO1)
2. VCC, VDDA, VDDGP, VDD_REG [in any order]
3. All other supplies [in any order]

NOTE: in case the internal regulator is used for VDDA generation, the VDD_REG should be powered up together with VCC and VDDGP, before the other supplies. In case the internal regulator is not used to generate VDDA (as on the Quick Start board), the VDD_REG is independent and has no power-up restrictions.

The power on timing sequence shown in **Table 1** is the sequence programmed into the Dialog PMIC. It is one way of providing sequences power to the i.MX53 processor. Designers are free to change the power timing sequence on their own board designs as long as the timing requirements are met. Freescale has not formally tested other power on timing sequences.

Regulator	Time Slot
VBUCKPRO	19 mSEC
VBUCKPERI VLDO6 VLDO8 VLDO10	23 mSEC
VBUCKCORE	27 mSEC
VBUCKMEM VBUCKPERI/SW VLDO2 VLDO5	31 mSEC
VLDO4 VLDO7	35 mSEC
VLDO3 VLDO9 DCDC_3V2	64 mSEC

Table 1. Regulator Timing Sequence

The Dialog PMIC will enter a SHUTDOWN/STANDBY condition by one of three ways; By a command from the i.MX53 Processor via I2C communications, by i.MX53 Processor action to hold the nONKEY/KEEPACT pin low for at least five seconds, or by hardware if the user holds down the POWER button for more than five seconds. All three actions result in the Dialog PMIC powering down the voltage regulators in reverse order of the power on sequence, except for VLDO1. A subsequent press of the POWER button will initiate the same power on sequence as shown in **Table 1**.

The various power rails supplied by the PMIC are discussed in the section on Quick Start Power Rails. Other features of the Dialog PMIC implemented by the Quick Start board are discussed in subsequent sub-sections including: Li-ION Battery Charging, Backlight LED Driver, Touch-Screen Operation, Miscellaneous.

5.2.1. Quick Start Power Rails

Table 2 shows all the voltage supply rails used on the Quick Start board, their voltages and the major subsystems they supply on the board:

Regulator	Voltage	Named Rails	Powers
VBUCKCORE	1.1V	VBUCKCORE VDDGP	VDDGP
VBUCKPRO	1.3V	VBUCKPRO VCC_1V3	VCC
VBUCKMEM	1.5V	VBUCKMEM DDR_1.5V DDRQ_1.5V	NVCC_EMI_DRAM DDR3 SDRAM
VBUCKMEM/SW	1.5V	VMEM_SW DDR_1.5V (ALT) DDRQ_1.5V (ALT)	ALTERNATE FOR: DDR3 SDRAM LOGIC DDR3 SDRAM CORE
VBUCKPERI	2.5V	VBUCKPERI VDD_REG_2V5 NVCC_XTAL_2V5 LVDS_2V5 (ALT) SATA_PHY_2V5 (ALT) VUSB_2V5 (ALT)	VDD_REG NVCC_XTAL ALTERNATE FOR: LVDS MODULE SATA MODULE USB MODULE 2.5V
VBUCKPERI/SW	2.5V	VPERI_SW LVDS_2V5 SATA_PHY_2V5 VUSB_2V5	LVDS MODULE SATA MODULE USB MODULE 2.5V
BOOST	Current Source	VLCD_BLT	EXPANSION PORT LCD BACKLIGHT SUPPLY
VLDO1	1.3V	VLDO1_1V3_RTC NVCC_SRTC	NVCC_SRTC
VLDO2	1.3V	DIG_PLL_1V3	ALTERNATE FOR: DIG_PLL
VLDO3	3.3V	VLDO3_3V3 SD1_3V3	MICROSD CARD (SD1) I2C1/I2C2 BOOT_SEL NVCC-EIM-MAIN NVCC_EIM_SEC NVCC_SD1&2 NVCC_PATA NVCC_FEC NVCC_GPIO NVCC_KEYPAD

Table 2. Quick Start Board Power Supply Rails

VLDO4	2.775V	VIOHI_2V775 LCD_3V2 (ALT)	NVCC_LCD1 NVCC_LCD2 EXPANSION PORT (LCD)
VLDO5	1.3V	VLDO5_1V3 SATA_1V3	SATA MODULE 1.3V
VLDO6	1.3V	VLDO6_1V3 VDDAL_1V3	VDDAL
VLDO7	2.75V	VLDO7_2V75 TVDAC_2V75	VGA MODULE (TV DCA)
VLDO8	1.8V	VLDO8_1V8	NVCC_RESET NVCC_JTAG NVCC_CKIH NVCC_NANDF NVCC_CSI VDD_ANA_PLL BOOT_SEL
VLDO9	1.5V	VLDO9_1V5	EXPANSION PORT
VLDO10	1.3V	VLDO10_1V3 VDDA_1V3	VDDAL
DCDC-3V2	3.2V	DCDC-3V2 AUDIO_3V2 FEC_3V2 VDD_FUSE LCD_3V2	ETHERNET AUDIO VGA_IO_SIGNALS USB 3.3V SD CARD (SD3) EXPANSION PORT

Table 2. Quick Start Board Power Supply Rails (con)

5.2.2. Li-ION Battery Charging

The Dialog PMIC contains a fully autonomous Li-ION battery charger. When wall power is first applied to the Quick Start board, the PMIC will begin to apply a pre-charge to the positive battery terminal. If the PMIC senses a fully discharged battery or a fault condition (eg, no battery), the PMIC will disconnect VDDOUT from the battery and allow the regulators to receive power independent what is attached to VBAT. The footprints for testing with a battery were included for skilled developers looking to experiment. As manufactured, the Quick Start board does not support Li_ION battery operations without modifications by the developer.

If the PMIC senses the battery voltage above the BAT_FAULT threshold for 40 msec, the PMIC will then begin a fast linear charge of the Li-ION battery by controlling the voltage on VDDOUT. If the PMIC is unable to increase VDDOUT above VBAT to continue charging the battery, the PMIC has an alternate current charging method using an active diode. Charging will continue until the battery voltage reaches the programmed level. The Li-ION charging circuit also makes use of a temperature sensor (thermistor) attached to the body of the battery. If the resulting voltage measurement at TBAT falls outside the threshold value programmed into the registry settings, the PMIC will suspend the charging current until the battery temperature reduces back to with the threshold values. See the Dialog PMIC datasheet for a more detailed explanation.

The PMIC is initially programmed with default settings to charge most Li-ION batteries. These settings may be changed by software and the software documentation should be consulted for actually PMIC registry values. These values can be changed in software as the developer sees fit. For more detailed information on how the battery charging function works and how to change default charging parameters. Since the 5V power pin of the USB micro-B connector is not connected to the PMIC, all discussion concerning battery charge current limits due to exceeding the USB standards do not apply to the Quick Start board.

In designing a board using the Dialog PMIC, it is important to include a capacitor of 47 uF or greater attached to the VBAT pin if any operations are planned without a Li-ION battery. If during the initial pre-charge phase, the Dialog PMIC does not sense any voltage present when the pre-charge voltage is momentarily removed and VBAT voltage is measured, the PMIC will assume a massive board failure and will not supply any voltage via the regulators.

5.2.3. Backlight LED Driver

The Dialog PMIC provides a Boost circuit which controls an external MOSFET Q8. The PMIC is capable of driving 3 independent strings of up to 5 white LEDs each with a voltage of approximately 24 Volts and a maximum of 50 mA. The Quick Start board does not have a direct connection for white backlight LEDs, but does supply one connection to the Expansion Port that can be used to support an attached LCD Daughter Card. The Expansion Port uses the LED1_IN port of the PMIC.

When designing a circuit to use the Backlight LED driver, it is important to connect the cathode (negative) end of the LED string directly to the LED_IN port of the PMIC. The PMIC controls the supply voltage to the Backlight LEDs by ensuring that the voltage sensed on the LED_IN port is above a threshold voltage of 0.7V. If more than one LED_IN ports are used, the lowest port must be above the threshold value. If the designer connects the cathode end of the Backlight LED string to GROUND, the boost circuit will not work.

The MOSFET used in the boost circuit should have a low ON Resistance value for best efficiency. The MOSTFET chosen for the Quick Start board, ON Semiconductor NTLJF4156NT1G, also contains a necessary diode used in the boost circuitry. This helps reduce the number of components.

5.2.4. Touch-Screen Operation

The Dialog PMIC contains an autonomous Touch Screen Interface which will measure the XY positions from a standard 4-WIRE resistive touch panel. The single ADC channel will detect the presence of a pen touch on the panel, and that will trigger a series of voltage measurements on each of the four touch panel wires (X+, X-, Y+, Y-) by the ADC in a pre-selected sequence. The resulting voltage readings are then reported to the i.MX53 Applications Processor for conversion to a panel X-Y position via the I2C communications link.

To ensure the Touch Screen Interface wakes up autonomously with a pen stroke, it is necessary to supply a 1.8V reference voltage to the TSIREF_GPIO_7 pin of the PMIC. It is recommended that one of the high PSSR Regulators of the PMIC be used to supply this voltage. VLDO6 – VLDO9 are possible sources for supplying this reference voltage.

5.2.5. Miscellaneous

If a coin cell battery is attached to the Quick Start board, it will automatically charge using the programmed charging settings whenever wall power is supplied to the Quick Start board. When the battery voltage reaches the programmed level, charging will stop. Battery discharge will not begin until wall power is removed from the board and, if a Li-ION battery is attached, the main battery discharges to the battery cut off level.

There are two port ID traces connected from the Expansion Port header to two of the ADC pins of the PMIC. Each unique Daughter Card designed by Freescale has a different resistor value attached to the two ID traces on the Daughter Card. It is possible to use this voltage divider identification system to determine at boot time if a daughter card is attached, and if so, which specific daughter card it is. Resistor values for the two daughter cards commonly used with the Quick start board are shown in **Table 3**.

	PORT_ID0	Measured Voltage	PORT_ID1	Measured Voltage
MCIMX28LCD	18.0K	1.61 V	130.0K	2.32 V
MCIMXHDMICARD	2.74K	0.54 V	130.0K	2.32 V

Table 3. Port ID Resistor Values

Over-Voltage protection is sensed by the DCIN (B4) pin of the PMIC. The voltage sensed by this pin must be between 4.5V and 5.5V. If the voltage meets this threshold value, the voltage seen at DCIN is blocked from the DCIN_SEL (B3) pin and the P-Channel MOSFET turns ON. Otherwise, DCIN_SEL remains high and power is blocked from the rest of the Quick Start Board.

The TP (L5) pin of the PMIC must be connected to ground. When designing with a 0.5mm pitch uBGA package, there is limited space for vias and traces under the BGA. To assist with layout, Freescale has confirmed that all pins labeled 'NO CONNECT' on the PMIC are in no manner bonded out to the silicon. Therefore, for routing purposes, it is possible to route the trace from an interior pin through one or more 'NO CONNECT' pins, or to place a via directly under a 'NO CONNECT' pin without requiring a via-in-pad technique. If the CAD Layout Engineer decides to place a via under a 'NO CONNECT' pin, the via should not be tented as trapped gases during the assembly process may cause the solder ball from the 'NO CONNECT' pin to blow out into other pins and cause internal shorts under the BGA.

The I2C communications channel between the Processor and the PMIC is Channel 1. This channel is only shared with the accelerometer. This channel operates at TTL logic level of 1.8V. The NRESET (F10) pin of the PMIC is directly connected to the Active Low POR_B (C19) pin of the i.MX Processor. The PMIC will hold the Processor in the RESET state until all the power rails are fully powered. The NIRQ (E10) pin of the PMIC is connected to the GPIO_ 16 (C6) pin of the Processor. This pin is not a dedicated pin for an interrupt request, but can be programmed in Software to inform the Processor that the PMIC has information to be given to the Processor.

The PMIC has several different options for Pull-Up levels on each of its output pins. In some cases, VDDOUT is one option, along with power supplied to both the VDD_IO1 (L4) and VDD_IO2 (K4) pins as Pull-Up source. The exact source of Pull-Up power is determined by the registry settings of the PMIC and can be pre-programmed at the factory as the designer wishes. Some Pull-Up registry settings apply to groups of pins, so care must be made in selecting which source power source is used for a particular grouping of pins. The Dialog PMIC Datasheet contains much more detailed information on the registry settings. For the Quick Start board, VLDO3 (3.3V) is connected to VDD_IO1 primarily to ensure that the 3V3_EN signal sent to the external regulator is sufficient to turn on the regulator, and VLDO8 (1.8V) is connected to VDD_IO2 to provide for proper I2C TTL logic levels.

5.3. 3.2V Secondary Voltage Regulator

To provide power in excess of the Dialog PMIC's capability, an external Voltage Regulator (Richtek, RT8010) is used. The regulator is adjustable and is set to 3.2V so that, in the event the processor may see two different sources for the required 3.3V power supply, the i.MX53 processor will preferentially draw from VLDO3_3V3. The regulator is controlled (enabled) from the PWR_UP_GP_FB2 (J10) pin of the Dialog PMIC. This is the only GPIO pin that can be programmed to turn on during the voltage timing sequence of the Dialog PMIC and is timed to turn on at the same time VLDO3_3V3 comes on. The internal pull-up power source for this GPIO is programmed to be from VDD_IO1 (VLDO3_3V3) which is the same voltage source for the Dialog RTC system. Since the i.MX53 standby power system is operated at 1.3V, this prevented using the Dialog RTC system as an input to the i.MX53 processor. If the developer does not want to enable the external voltage regulator from the Dialog GPIO pin, it would be possible to reconfigure VDD_IO1 to be 1.3V and use the Dialog RTC clock instead. This is a design choice for the developer.

The external voltage regulator supplies power to the following general board areas and is expected to supply up to the maximum specified currents as follows:

- i.MX53 USB Phy 10 mA
- VGA Connector Output 10 mA
- Audio 10 mA
- Debug UART 60 mA
- Ethernet 100 mA
- Expansion Port (HDMI) 30 mA
- SD Card 60 mA

For the Expansion Port and the SD Card socket, it may be that the current draws exceed the above estimates if a custom designed board is added to the Expansion Port, or if an SDIO device is plugged into the SD Card Socket (ie, WiFi, Bluetooth). The external voltage regulator is capable of supplying up to 1A of current and should be capable of accommodating most custom configurations.

Since the Quick Start board was originally designed, it has been found that VDDA, VDDAL, and DIG_PLL can all be powered internally by the i.MX53 processor (with the correct eFuse settings). This would then free the PMIC VLDO2, VLDO6 and VLDO10 power sources for other uses. VLDO6 and VLDO10 will be able to supply the above expected loads, provided a high current draw SDIO card is not inserted in the SD Card Socket. The designer is free to rearrange power rails as desired.

5.4. i.MX53 Applications Processor

The i.MX53 Applications Processor is physically located in the central portion of the Quick Start board. The most critical components for placement after the processor are the DDR3 SDRAM ICs. The remainder of the components and connectors are arranged around the periphery of the board in locations that minimize trace routing. The i.MX53 Processor is a highly integrated system-on-chips with many modules controlled by the main Arm Cortex-A8 core. Most modules have Logic Voltage inputs which allow the designer to modify logic levels to suit the needs of connected ICs. A more detailed explanation of these Logic Voltage Inputs is presented in the **Peripheral Module Logic Voltage Levels** subsection. The information for voltage levels and other chip specific details come from the I.MX53 Data Sheet, which may be revised from time to time. In the event that the most recent data sheet and the User Guide do not agree, the Data Sheet should always take precedence. Every effort will be made to keep the User Guide current to the most recent Data Sheet.

The i.MX53 Processor initializes out of reset according to its preprogrammed ROM code. After initial wakeup, it then attempts to read the logic levels on 26 different pins. Depending which pins are high/low, the Processor will then select one of the allowed boot options to begin the boot process. This is further explained in the subsection on **Boot Mode Operations and Selections**.

The clock signals required by the i.MX53 Processor and the rest of the Quick Start board are further explained in the section on **Clock Signals**. The i.MX53 Processor has the ability to supply a limited amount of filtered power for internal purposes using an internal voltage regulator. The operation of this regulator is explained further in the **i.MX53 Internal Regulator** subsection. The Processor also has an internal Watch Dog Timer (WDOG) circuit that can be used to reset the Processor in the event it stops functioning correctly. The supporting circuitry is explained in further detail in the subsection titled **Watch Dog Time**.

5.4.1. Peripheral Module Logic Voltage Levels

By convention, pins used on the I.MX53 Processor to set module logic voltage levels begin with NVCC_. This is to aid the developer in the design of a project based on the i.MX53 Processor. There are 25 such pins used, and practically speaking, they supply the internal pull-up voltages for pins designated for data output. These 25 pins are shown in detail in **Table 4. Module Voltage Supplies**. Once a voltage level is selected for a particular module, all pins within that module will use the same voltage level. It is important for the developer not to try to use an external pull-up to a different voltage level for individual pins. Level shifters must be used if certain pins need to have different voltage levels to interface with external ICs. If a different voltage level is used on an external pull-up, one or both of the affected power rails will most likely have a different voltage level than intended throughout the design. On a newly designed board that shows unexpected voltage levels, this may be the first thing to check.

On the Quick Start board, there are a number of unpopulated pull-up resistors. This is a result of the initial design being conservative, and the addition of external pull-up resistors to supplement internal i.MX53 pull-up supply voltage. Subsequent Quick Start board usage has shown these pull-ups to be unnecessary, so they are unpopulated.

	Module	Allowed Values	Quick Start board
NVCC_EMI_DRAM_1 NVCC_EMI_DRAM_2 NVCC_EMI_DRAM_3 NVCC_EMI_DRAM_4 NVCC_EMI_DRAM_5	External Memory Interface	1.425V - 1.9V	1.5V (Match DDR3 Memory)
NVCC_NANDF	NAND Flash	1.65V - 3.6V	1.8V
NVCC_EIM_MAIN_1 NVCC_EIM_MAIN_2 NVCC_EIM_SEC	External Interface Module	1.65V - 3.6V	3.3V
NVCC_RESET	Reset Logic Levels	1.65V - 3.1V	1.8V (Match PMIC)
NVCC_SD1	SD Card Module 1	1.65V - 3.6V	3.3V (Match SD Cards)
NVCC_SD2	SD Card Module 2	1.65V - 3.6V	3.3V
NVCC_PATA	Parallel ATA	1.65V - 3.6V	3.3V
NVCC_LCD_1 NVCC_LCD_2	LCD Module	1.65V - 3.1V	2.775V
NVCC_CSI	Camera Sensor Interface	1.65V - 3.6V	1.8V
NVCC_FEC	Fast Ethernet Controller	1.65V - 3.6V	3.3V (Match Ethernet PHY)
NVCC_GPIO	General Purpose I/O	1.65V - 3.6V	3.3V
NVCC_JTAG	JTAG Module	1.65V - 3.1V	1.8V
NVCC_KEYPAD	Keypad Port	1.65V - 3.6V	3.3V (Match Audio CODEC)
NVCC_CKIH	Clock Amplifier Circuit	1.65V - 1.95V	1.8V
NVCC_XTAL	24MHz Crystal Supply	2.25V - 2.75V	2.5V
NVCC_SRTC_POW	Secure Real Time Clock	1.1V - 1.3V	1.3V
NVCC_LVDS	Low Voltage Differential Signaling	2.375V - 2.625V	2.5V
NVCC_LVDS_BG	LVDS Band Gap	2.375V - 2.625V	2.5V

Table 4. Module Voltage Supplies

5.4.2. Boot Mode Operations and Selections

The i.MX53 Applications Processor can be directed to boot from the logic levels on 24 different pins designated for boot mode configurations, or it can be directed to boot from internal eFUSE settings, or it can be directed to boot from a serial downloader (USB/UART). The method used to determine where the Processor finds its boot information is from two dedicated BOOT_MODE pins. **Table 5** shows the values used of each of these methods.

It is important for the developer to remember that these two pins are tied to the NVCC_RESET modules, and therefore, on the Quick Start board, use a 1.8V logic level (unlike the Boot Configuration pins which use a 3.3V logic level). The default boot selection for the Quick Start board is 00 – Boot from hardware settings. Since it is not expected that developers will want to burn eFUSES on the Quick Start board, the two BOOT_MODE pins are tied together through one switch position of the optional DIP Switch (SW1). If the developer wishes to populate SW1, the position 10 switch can be moved to ON so that the BOOT_MODE pins are both pulled high. Then the developer will be able to use the serial downloader method of loading bootable code into the Processor.

BOOT_MODE1	BOOT_MODE0	Boot Source
0	0	Determined By Board Hardware
0	1	Reserved
1	0	Determined By eFUSE Settings
1	1	Use Serial Downloader

Table 5. BOOT_MODE pin Settings

If the method of determining the bootable source code is selected to be from hardware, then 21 i.MX53 pins are sampled at the beginning of the boot process. These 21 pins are shown in **Tables 6A – 6C** along with their default setting on the Quick Start Board. Note that three bits in the BOO_CFG words do not have corresponding pins to read.

	BOOT_ CFG1[7]	BOOT_ CFG1[6]	BOOT_ CFG1[5]	BOOT_ CFG1[4]	BOOT_ CFG1[3]	BOOT_ CFG1[2]	BOOT_ CFG1[1]	BOOT_ CFG1[0]
PIN	EIM_A22	EIM_A21	EIM_A20	EIM_A19	EIM_A18	EIM_A17	EIM_A16	EIM_LBA
Default	0	1	0	0	0	0	0	1

Table 6A. BOOT_CFG Word1

	BOOT_ CFG2[7]	BOOT_ CFG2[6]	BOOT_ CFG2[5]	BOOT_ CFG2[4]	BOOT_ CFG2[3]	BOOT_ CFG2[2]	BOOT_ CFG2[1]	BOOT_ CFG2[0]
PIN	EIM_EB0	EIM_EB1	EIM_DA0	EIM_DA1	EIM_DA2	EIM_DA3	N/A	N/A
Default	0	0	1	1	1	0	-	-

Table 6B. BOOT_CFG Word2

	BOOT_ CFG3[7]	BOOT_ CFG3[6]	BOOT_ CFG3[5]	BOOT_ CFG3[4]	BOOT_ CFG3[3]	BOOT_ CFG3[2]	BOOT_ CFG3[1]	BOOT_ CFG3[0]
PIN	EIM_DA4	EIM_DA5	EIM_DA6	EIM_DA7	EIM_DA8	EIM_DA9	EIM_DA10	N/A
Default	0	0	0	0	0	0	0	-

Table 6C. BOOT_CFG Word3

Of these 21 pins, four of them have the same meaning regardless of the selected boot source. These four BOOT_CFG bits with their meanings are as follows:

BOOT_CFG1[1] Processor Speed setting during boot:
0 – 800 MHz
1 – 400 MHz

BOOT_CFG1[0] MMU Enabled during boot:
0 – MMU not enabled
1 – Initializing MMU with L1 Cache during boot

BOOT_CFG2[3] AXI/DDR Speed setting during boot:
0 – PLL2: 400MHz
1 – PLL2: 333MHz

BOOT_CFG2[2] Oscillator Frequency Select:
0 – Auto Detect
1 – Set to 24MHz

The six pins that determine where bootable code is stored are BOOT_CFG1[7:2]. Depending on which boot source is selected, some of these pins may have different meanings. Those pins will show up as an 'X' for logic level. The specific logic levels and their meanings are as follows:

BOOT_CFG1[7:2] Boot Code Source Selection

0000 - NOR/OneNAND Boot
0001 - Reserved
0010 - PATA/SATA Boot
0011 - Serial ROM (I2C/SPI) Boot
01XX - SD/MMC (eSD/eMMC) Boot
1XXX - NAND Flash Boot

For each of the bootable source selections, the remaining BOOT_CFG pins have different meanings. The pins are meant to choose initialization settings required for each specific boot source. The following paragraphs will specify those choices base by bootable source:

NOR/OneNAND

BOOT_CFG1[3]	Memory Type	0 – NOR Flash 1 – OneNAND
BOOT_CFG2[7:6]	Muxing Scheme	00 – Muxed, 16-bit data (low half) interface 01 – Not muxed, 16-bit data (high half) interface 10 – Reserved 11 – Reserved
BOOT_CFG3[7:6]	OneNAND Page Size	00 – 1KB 01 – 2KB 10 – 4KB 11 – Reserved

HD (PATA/SATA)

BOOT_CFG1[3]	HD Type	0 – PATA 1 – SATA

Serial-ROM

BOOT_CFG1[3]	Serial ROM Select	0 – I2C 1 – SPI
BOOT_CFG2[5]	SPI Addressing	0 – 2-byte (16-bit) 1 – 3-byte (24-bit)
BOOT_CFG3[5:4]	Port Select	00 – I2C1/eCSPI1 01 – I2C2/eCSPI2 10 – I2C3/CSPI 11 – Reserved
BOOT_CFG3[3:2]	Chip Select (SPI Only)	00 – CS0 01 – CS1 10 – CS2 11 – CS3

SD/eSD

BOOT_CFG1[4]	Fast Boot	0 – Regular 1 – Fast Boot
BOOT_CFG1[3]	SD/MMC Speed	0 – High 1 – Normal
BOOT_CFG2[5]	Bus Width	0 – 1-bit 1 – 4-bit
BOOT_CFG3[5:4]	Port Select	00 – eSDHC1 01 – eSDHC2 10 – eSDHC3 11 – eSDHC4

MMC/eMMC

BOOT_CFG1[4]	Fast Boot	0 – Regular Boot 1 – Fast Boot
BOOT_CFG1[3]	SD/MMC Speed	0 – High 1 – Normal
BOOT_CFG2[7:5]	Bus Width	000 – 1-bit 001 – 4-bit 010 – 8-bit 011 – Reserved 100 – Reserved 101 – 4-bit DDR (MMC 4.4) 110 – 8-bit DDR (MMC 4.4) 111 – Reserved
BOOT_CFG3[5:4]	Port Select	00 – eSDHC1 01 – eSDHC2 10 – eSDHC3 (eMMC4.4) 11 – eSDHC4
BOOT_CFG3[3]	DLL Override	0 – Use Default ROM 1 – Use eFUSE DLL Override
BOOT_CFG3[2]	Fast Boot Acknowledge	0 – Enabled 1 – Disabled

NAND

BOOT_CFG1[6]	Muxed On:	0 – PATA 1 – WEIM
BOOT_CFG1[5:4]	Interleave Scheme:	00 – No Interleaving 01 – 2 Device 10 – 4 Device 11 – Reserved
BOOT_CFG1[3:2]	Address Cycles:	00 – 3 01 – 4 10 – 5 11 – 6
BOOT_CFG2[7:6]	Page Size:	00 – 512 + 16 Bytes (4-bit ECC) 01 – 2KB + 64 Bytes 10 – 4KB + 128 Bytes 11 – 4KB + 218 Bytes
BOOT_CFG2[5]	NAND Interface	0 – 8-bit 1 – 16-bit
BOOT_CFG2[2]	NAND Flash Clock Frequency	0 – AXI DDR Frequency divide by 12 1 – AXI DDR Frequency divide by 28
BOOT_CFG3[7]	Bad Block Skip Step (Stride Size)	0 – 1 Block 1 – 8 Block
BOOT_CFG3[6]	LBA-NAND Select	0 – Non LBA (11ms delay) 1 – LBA (22ms delay)
BOOT_CFG3[5]	NAND use R/nB Signals?	0 – No 1 – Yes
BOOT_CFG3[4:3]	ECC/Spare Select	00 – 8-bit ECC 01 – 14-bit ECC 10 – 16-bit ECC 11 – ECC Off
BOOT_CFG3[2:1]	Pages in Block	00 – 32 Pages 01 – 64 Pages 10 – 128 Pages 11 – 256 Pages

When the Quick Start board was originally designed, several of the BOOT_CFG pins were selectable by the 10 position DIP Switch (SW1). After initial testing of the Quick Start board, the optimum BOOT_CFG settings for flexibility and ease of use were determined. These are the default settings on the board, which set the microSD card connector (SD1) as the default boot source. As the developer becomes more familiar with the board and wishes to experiment more, it is recommended that the next step for the developer is to write code for the microSD card to initialize as alternative boot source and pass off the boot process to the new source.

As further experience is gained, the developer may wish to install the optional DIP switch on SW1 (Multicomp MCNHDS-10-T). The boot-switch was originally removed to improve ease of use and ensure all members of the community are developing the same way. Installing the boot-switch will allow the developer to gain access to selecting either SD card socket as the bootable source, or to select the serial downloader method. Finally, for the skilled developers, it is possible to desolder and rearrange some of the pull-up and pull-down resistors on the Quick Start board. **Figures 16 and 17** highlight all of the pull-up and pull-down resistors used, and also highlights sources of either high (3.3V) or low (GND) logic levels.

Figure 16. Boot Mode Resistor Locations TOP

Resistor	Boot Configuration Bit	Pull UP/Down
R46	BOOT_CGF1[6]	Pull Up
R47	BOOT_CGF1[7]	Pull Down
R48	BOOT_CGF2[7]	Pull Up (DNP)

Table 7. Boot Mode Resistors TOP

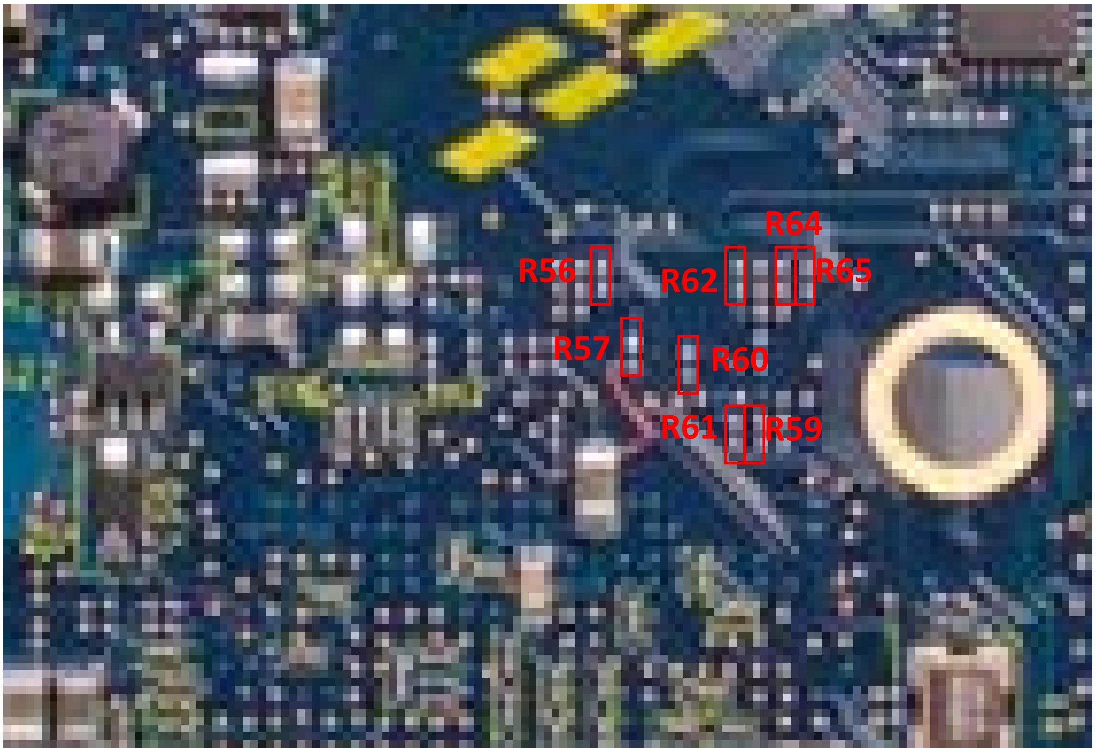


Figure 17. Boot Mode Resistor Locations BOTTOM

Resistor	Boot Configuration Bit	Pull UP/Down
R56	BOOT_CGF1[1]	Pull Down
R62	BOOT_CGF2[3]	Pull Up
R64	BOOT_CGF3[4]	Pull Down
R65	BOOT_CGF3[3]	Pull Down
R57	BOOT_CGF1[0]	Pull Up
R60	BOOT_CGF2[5]	Pull Up
R61	BOOT_CGF2[4]	Pull Up
R59	BOOT_CGF2[6]	Pull Down

Table 8. Boot Mode Resistors BOTTOM

5.4.3. Clock Signals

The Quick Start board has three external clocks, two of which are dedicated to the i.MX53 Processor, and one dedicated to the Ethernet PHY. The 24 MHz crystal (Y1) is the main clock source for the Processor. The crystal is located on the bottom side of the board as shown in **Figure 18**. It is driven by its own 2.5V supply pin, NVCC_XTAL. Although the crystal frequency for the board is set to be 24MHz, the default BOOT_CFG2[2] pin that controls specifying the frequency is left to auto detect. In the case of 24MHz, the actual setting is not important. If a clock oscillator is used, it would be connected to the pin EXTAL (AB11) and the pin XTAL (AC11) should be left floating. The 24 MHz clock signal can be output from any GPIO pin for use in other locations. On the Quick Start board, the clock signal is output on GPIO_0 and is the net is labeled GPIO_0(CLK0). The clock signal is sent to the Audio Codec as the clock source for the audio sub-system, and it is also sent to the expansion port as an available clock signal for a custom designed card as needed.

The 32.768KHz crystal (QZ1) is the clock source used by the i.MX53 Processor for the Secure Real Time Clock module. It receives power from the NVCC_SRTC pin which is connected to the VLDO1 1.3V voltage regulator. The 32.768KHz clock signal is not sent anywhere else on the Quick Start board. The location of the crystal is also shown in **Figure 18**.

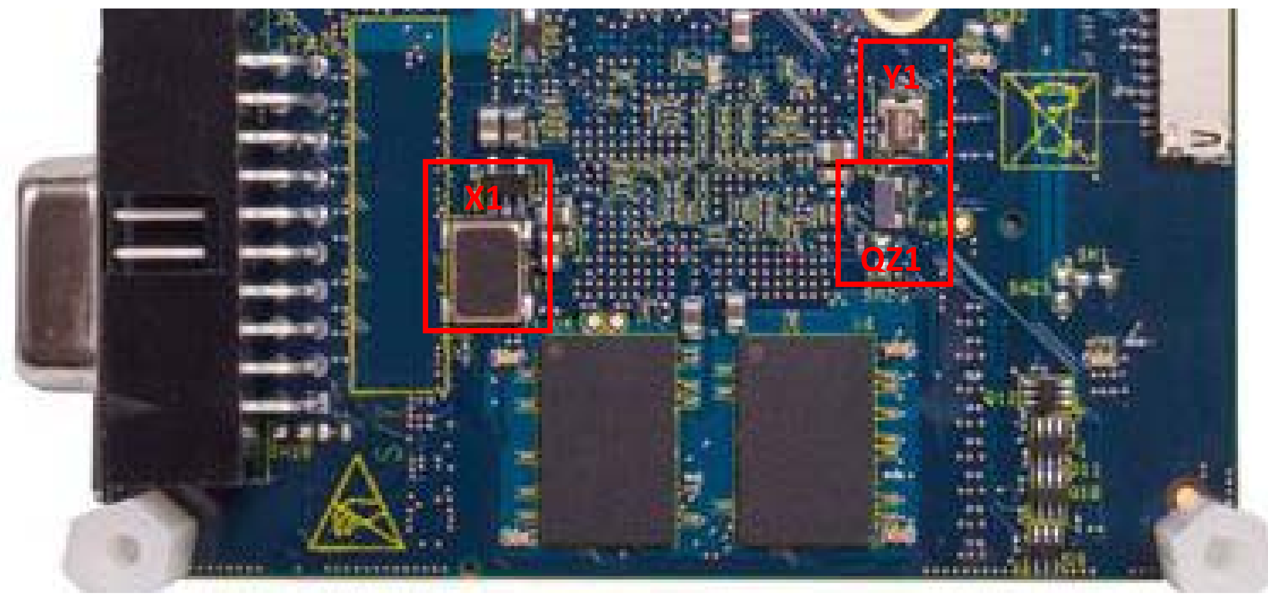


Figure 18. Clock Source Locations

The clock source for the Ethernet PHY is a 50 MHz Oscillator (X1) with an enable pin and is shown in **Figure 18**. The oscillator was originally placed to support both the SATA module and the Ethernet PHY. It is no longer used for the SATA module, and only supplies a clock signal to the Ethernet PHY. It is powered by the DCDC_3V2 power rail and, by default, is always on when the DCDC_3V2 rail is powered on. It is possible for the developer to remove resistor R110 and place a zero Ohm resistor across R197 to give the developer software control of the oscillator through pin GPIO_4 (D4).

5.4.4. i.MX53 Internal Regulators

The i.MX53 Applications Processor contains two internal voltage regulators which can supply VDDA, VDDAL, VDD_DIG_PLL and VDD_ANA_PLL. The power input for this pin is VDD_REG (pin G18). On the Quick Start board, this pin is connected to VBUCKPERI and is set to 2.5V.

The Digital PLL voltage regulator can be selected to supply VDD_DIG_PLL through an internal (on die) connection. The VDD_DIG_PLL pin can also be connected to the VDDA and VDDAL pins through an external connection to allow the Digital PLL regulator to supply these rails as well. The Digital PLL regulator is set to start at a reduced voltage value of 1.2V, but is programmed by software to increase to 1.3V early in the boot process. On the Quick Start board, the VDD_DIG_PLL connection to VLDO2 is not populated by default, so that VDD_DIG_PLL power is supplied by the internal regulator. The VDDA supply pins are connected to VLDO10 through a shorting trace SH22. If the developer wishes to experiment with supplying VDDA from the internal regulator, the trace between the two pads of SH22 can be cut, and a wire soldered between SH22 pin 2 and resistor R210 pin 2. The VDDAL supply pin is connected to VLDO6 through a shorting trace SH24. If the developer wishes to experiment with supplying VDDAL from the internal regulator, the trace between the two pads of SH24 can be cut, and a wire soldered between SH24 pin 2 and resistor R210 pin 2.

The Analog PLL voltage regulator can be selected to supply VDD_ANA_PLL through an internal (on die) connection. The Analog PLL is set to supply a voltage of 1.8V. On the Quick Start board, the VDD_ANA_PLL connection to VLDO8 is not populated by default, so that VDD_ANA_PLL is supply by the internal regulator.

Developer Note: During the boot process, it takes approximately 310msec for VDD_DIG_PLL to change from 1.2V to 1.3V. During this time, the i.MX53 core will not run at full speed/maximum processor loading. It will operate in the reduced power mode, and the limitations of the reduced power mode discussed in the datasheet apply. It is expected that during the first 310msec, processor loading will not be an issue.

5.4.5. Watch Dog Timer

The i.MX53 Application Processor has an internal Watch Dog Timer circuit. On the Quick Start board, the WDOG output is assigned to GPIO_9. The WDOG is an active low signal. The Dialog PMIC does not have a specific pin to accept a Watch Dog signal to force a Processor reset. Therefore, the WDOG signal is modified by hardware components on the Quick Start board and applied to the Processor Reset pin (POR_B, pin C19). By using an active-low enabled buffer, the active low WDOG signal can be transformed into a low pulse, which returns back to the logic high state immediately after the i.MX53 Processor resets (~ 700 nsec). This allows the processor to reset the WDOG signal and then come out of reset. The buffer IC also is in a tri-state condition when the WDOG signal is normally high, thus allowing the push-button reset circuitry to work. The Watch Dog circuitry is shown in **Figure 19**.

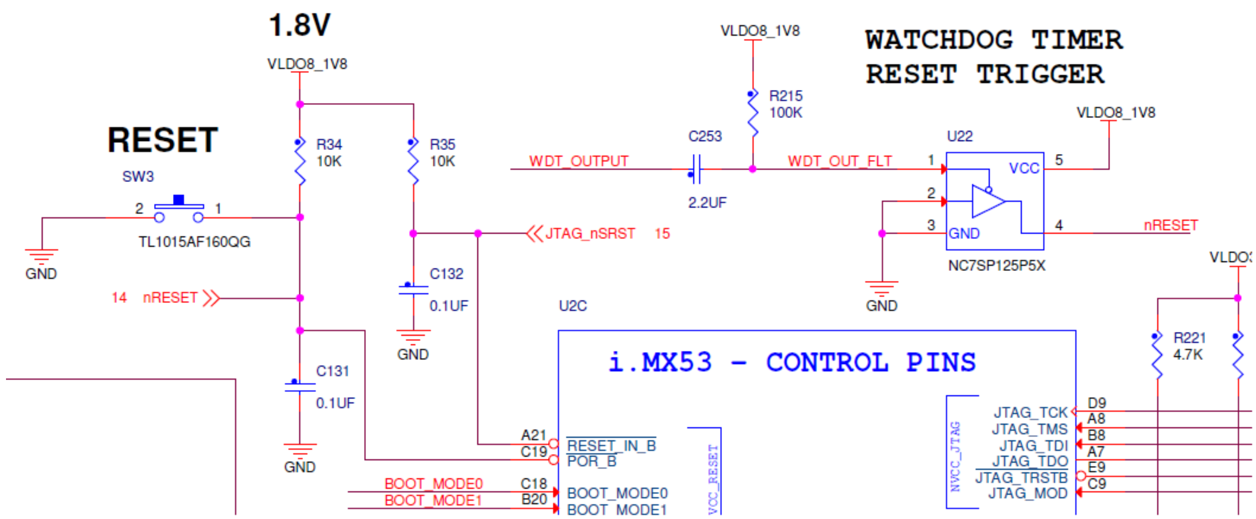


Figure 19. Watch Dog Timer Reset Trigger

In normal operation, WDT_OUTPUT is high, which keeps WDT_OUT_FLT high and the buffer in the OFF state. As soon as the WDOG goes active low, WDT_OUT_FLT is pulled low through C253, and the buffer (U22) is enabled. The always low input to the buffer is then sent to the POR_B pin and forces the Processor into reset. The RC circuit formed by R215 and C253 will then begin to raise the voltage level on WDT_OUT_FLT, until after XX msec, the active low output enable pin of U22 will turn off the Buffer and POR_B will return high. In coming out of reset, the WDOG will then return to the HIGH or OFF state, and the Processor will return to normal operations.

5.4.6. Wakeup After User Initiated Standby

Q13 is a dual P-channel/N-channel MOSFET designed to take a transition from a low state to a high state on PMIC_ON_REQ (pin W15) and turn it into a PMIC nONKEY request to bring the Dialog DA9053 chip out of a standby state to a fully on state. The PMIC_ON_REQ pin has been designed to work with the Freescale companion PMIC chip and is always in a high state even if the user forces the board into standby with the nONKEY. To configure the wakeup after user initiated standby feature, the user first has to program the software to transition the PMIC_ON_REQ to the low state after a start up or resume after standby operation. This will place the circuit in a correct configuration to request a startup from the standby state. Without this software change, pressing the nONKEY after a forced standby will not wake the board back up out of sleep.

To keep the board operating correctly before this software modification is made, Q13 has not been populated on the board. When the developer has modified code to make this work, Q13 can be populated to complete the circuit. Information on Q13 can be found in section 14, Bill of Materials.

5.5. DDR3 SDRAM Memory

The Quick Start board has four 128MX16 DDR3 SDRAM chips for a total of 1GB RAM memory. The chips are organized in two different arrays, differentiated by the chip selects, storing either the upper 16-bits or the lower 16-bits of a 32-bit word. This organization is shown in **Table 9** below.

	Chip Select '0'	Chip Select '1'
Lower 16-bits [15:0]	U3	U4
Upper 16-bits [31:16]	U5	U6

Table 9. DDR3 SDRAM Chip Organization

In this organization, there are 21 traces that connect to all four DDR3 chips and the i.MX53 Processor (14 Address, 3 Bank Address, 3 Control, and Reset). These are the most critical traces since they will see the most loading. The remaining traces are connected to two DDR3 chips and the Processor, and will only see one active DDR3 chip at a time. Note that the two clock traces are tied with the data traces (SDCLK_0 for the lower 16-bits, SDCLK_1 for the upper 16-bits). This limits the clock traces to only one active DDR3 chip at a time as well.

In the physical layout, the DDR3 chips are placed to minimize routing of the address traces. The two chip select '0' chips are placed on top, and the two chip select '1' chips are placed on the bottom side, directly below the chips with the same data traces. The data traces are not necessarily connected to the DDR3 chips in sequential order, but for ease of routing, are connected as best determined by the layout and other critical traces. The i.MX53 Processor has the capability of remapping SDRAM word bit order based on chip select used, so that words can be physically stored in memory in correct order. If this is a feature the developer wishes to implement, there is more information in the software reference manual.

The DDR_VREF is created by a simple voltage divider using 470 Ohm 1% resistors and 0.1 uF capacitors for stability. The relatively small value resistors provide enough current to maintain a steady mid-point voltage. The calibration resistors used by the four DDR3 chips and the Processor are 240 Ohm 1% resistors. This resistor value is specified by the DDR3 Specifications. There is a 200 Ohm resistor between each clock differential pair to maintain the correct impedance between the two traces. The DDR3 SDRAM should be rated for 1066 MHz or faster.

For skilled designers wishing to double the amount of DDR3 SDRAM available for use with the i.MX53 processor using eight x8 width DDR3 chips, the following considerations should be weighed carefully before proceeding: Four DDR3 chips on a chip select line will exceed the current supply capability of the VBUCKMEM power source. An additional 1.5V power source would need to be added. Also, attaching the address lines to eight DDR3 chips is a great amount of loading. Premium PCB materials would be required to reduce losses. Freescale has tested and validated using eight DDR2 SDRAM chips in this manner. Using eight DDR3 SDRAM chips has not yet been tried.

Developers should note that using different configurations of SDRAM requires register changes on the i.MX53 Processor to ensure that timing and address sequencing is set up correctly. Software initialization settings will be different depending on SDRAM configuration.

5.6. Micro SD Card Connector

The microSD Card Connector (J4) is directly connected to the eSDHC channel 1 module of the i.MX53 Applications processor. This card socket will support up to a 4-bit data transfer from an microSD card or a microMMC card inserted into the socket. The Quick Start board is designed to boot a microSD Card from the microSD card socket with no additional modifications. If the developer wishes to boot from a microMMC card, the following options shown in **Table 10** below are available:

Option	Net	Condition	Notes:
SD Card Operations	EIM_A20	Default Low	Position 8 on DIP Switch SW1
MMC Card Operations	EIM_A20	Pull High	Position 8 on DIP Switch SW1

Table 10. Micro-SD Card Boot Options

The main power for the microSD Card Socket is 3.3V from (VLDO3_3V3). This ensures that if the external voltage regulator is turned off for power savings, the microSD Card Socket still has power. Power to the card socket is through SH1. If the developer wants to supply power from a different power source, this trace can be cut. The developer should note that the internal i.MX53 processor eSDHC module is powered by a 3V3 source, so changing the voltage of the cards socket on the Quick Start board is not recommended.

The SD1 Clock trace has a 22 Ohm series termination resistor (R211). This resistor is inserted to prevent a reflected signal from being sensed by the i.M53 processor. This has been found to occur on MMC card operation and is recommended for all designs. In addition, the following eSDHC channel 1 trace is pulled high to 3.3V (VLDO2_3V3).

- SD3 Command (R76)

By default, the Quick Start board is manufactured with a 3M 29-08-05WB-MG part for availability reasons. The combined Data3/Card Detect trace is not supported by the BSP software. It is possible for the developer to remove the original card socket and repopulate the position with an alternate microSD Card Socket made by Proconn, MSPN09-A0-2000. The developer should also then populate R108 with a suitable pull-up resistor (10K). This will then give the developer the option to use the card detect trace for channel 1 connected to EIM_DA13 (pin AC7).

5.7. Full Size SD Card Connector

The full size SD Card connector (J5) is directly connected to the eSDHC channel 3 module of the i.MX53 Applications processor. This card socket will support up to a full 8-bit data transfer from an SD card, SDIO device, or MMC card inserted into the socket. The Quick Start board was designed by default not to boot from the J5 card socket. If the developer wishes to boot from J5, the following options shown in **Table 11** below are available:

Option	Net	Condition	Notes:
Boot From J5 Card Socket	EIM_DA6	Pull High	Position 2 on DIP Switch SW1
High Speed Operations	EIM_A18	Pull High	Position 6 on DIP Switch SW1
Fast Boot	EIM_A19	Pull High	Position 7 on DIP Switch SW1
SD Card Operations	EIM_A20	Default Low	Position 8 on DIP Switch SW1
MMC Card Operations	EIM_A20	Pull High	Position 8 on DIP Switch SW1

Table 11. Full Size SD Card Boot Options

The Quick Start board is configured to have the ROM code try to initiate boot operations in the 4-bit data mode, by setting BOOT_CFG[6:5] to (01). Section 6.4.3.6 explains the SD/MMC boot options in greater detail for the interested developer.

Main power to the SD Card Connector is from the external LDO regulator (DCDC_3V2). If this regulator is turned off for power savings purposes, the card socket will not function. It is possible for the developer to cut the trace between the pads of SH32 and attach a different source of power to the pad next to the card socket via a wire solder. Note that the eSDHC module internal to the i.MX53 processor is operating at 3.3V, therefore it is recommended that the alternate source also be 3.3V. Cutting the SH32 trace should only be used if a SDIO device inserted into the socket is drawing more power than the LDO Regulator is capable of supplying.

The SD3 Clock trace has a 22 Ohm series termination resistor (R212). This resistor is inserted to prevent a reflected signal from being sensed by the i.M53 processor. This has been found to occur on MMC card operation and is recommended for all designs. In addition, the following eSDHC channel 3 traces are pulled high to 3.2V (DCDC_3V2).

- SD3 Command (R89)
- SD3 Card Detect (R88)
- SD3 Write Protect (R87)

5.8. VGA Video Output

The i.MX53 Applications Processor TV Encoder module provides three component video output signals that can be used as either a TV signal or as a VGA signal to a connected monitor. The Quick Start board configures these signals for use as a VGA output through connector J8. In addition to the 3 video signals, Horizontal and Vertical Synchronization signals, I2C Data and Clock and a 5V reference signal are connected to the VGA output in accordance with the VGA Video Standard. The video data signals are referenced to 2.75V (TVDAC_2V75), while all other signals are referenced to 5V. The synchronization signals leave the i.MX53 Processor referenced to 3.3V, but go through a pair of one-way level shifters (U12, U13) to meet the VGA standard required 5V reference. Similarly, the I2C Channel two signals leave the processor referenced to 3.2V, but go through a bi-directional level shifter (U14) to also become referenced to 5V. See the connector section for the actual pin-out of J8.

The Component Video signals are terminated to ground, each with a 75 Ohm resistor to meet cabling requirements. A separate VGA ground plane has been created to minimize noise on the video signals by necking through a small trace. The voltage reference signal for the TVDAC module is provided by placing a 1.05K 1% Ohm resistor at pin Y18. The constant current source provided by the TVDAC module generates the exact voltage reference required by the VGA standard. A 0.1uF capacitor should be connected to pin AA19 to reduce noise on the voltage reference sense point. Each of the Component Video output traces should be connected to their respective feedback pins. This provides the Cable Detection (CD) circuitry the ability to detect whether a cable has been plugged into the connector. The CD circuitry is not active for TV signal output, so it would not be necessary to connect the feedback circuit in that case. If any signal filtering or conditioning components are added to the Component Video traces, the feedback pins should be connected after the additional components (ie, feedback pins should tap into to the connector side of the Component Video signals). A ferrite bead is recommended near the voltage input pins of the TVDAC module to reduce noise in the video module.

5.9. LVDS Video Output

The i.MX53 Applications processor contains two separate LVDS modules that can be operated independently. Each module provides five sets of differential pair signals, four used for data and one pair for the clock signal. The Quick Start board uses only one of the two modules to provide an optional secondary display panel that can be used in conjunction with one of the other primary means of video output, or if desired, to be used as the sole video output. Developers who wish to use two LVDS outputs at the same time may wish to consider the MCIMX53SMD Tablet for development. The Quick Start board makes use of three of the differential pair data pins and the clock pins. These signals, combined with a display enable pin, a contrast pin, two separate channels of I2C communications, an interrupt pin, and power supplies (5V and 3.2V), will provide the necessary signals to support many of the LVDS display panels currently available on the Market. The connector used is a 30-pin connector that meets the LVDS standards for connectors (Hirose, DF19G-30P-1H(56)).

Development work with LVDS panels was done with the Hannstar HSD100PXN1-A00-C11 display. This display determined the signal ordering on the connector. To aid in development work, Freescale has purchased a large number of LVDS display and has contracted to make customer cables that will connect the displays to the Quick Start board. This LVDS display kit will be available from Freescale as described in the board accessory section.

If the developer wishes to use a different LVDS display, a custom cable would most likely be required to ensure the plug on the cable end that connected to the display was the right type and to re-order the signals to match the ordering on the display. For use with other displays, signals are referenced to the following voltages:

LVDS Data/Clock	2.5V (LVDS_2V5)
Display Control	3.3V (VLDO3_3V3)
I2C channel two	3.2V (DCDC_3V2)
I2C channel three	3.3V (VLDO3_3V3)

Isolation resistors on the i2C channel two traces (R213, R214) provide a means of isolating the LVDS connector from other functions on the board if the LVDS connector is interfering with I2C communication. In addition, the empty pads can also serve as attachment points for hand soldered wires if the developer wishes to run different signals to this connector.

The i.MX53 Applications Processor has both an internal and external method to measure Band Gap resistance. If the internal method is chosen by software, pin AA14 can be left floating. If the external method is desired, a 28.0K 1% Ohm resistor should be attached between pin AA14 and ground. It is recommended that this resistor be added routinely to give software the option of choosing between the two methods. It is also recommended to place a 49.9 1% Ohm resistor as the voltage input pin of U14 (NVCC_LVDS_BG) to filter the power used in measuring the Band Gap.

5.10. Expansion Port

The function of the Quick Start board Expansion Port is to bring out many of the i.MX53 pins that are otherwise unused on the Quick Start board. The overriding design considerations for this port were to be able to support HDMI functionality through a daughter card (primary) while also being able to support an existing LCD daughter card (secondary). In meeting these considerations, the Expansion Port was also constrained to meet a general power/signal format adopted across all recent i.MX development board designs, primarily for safety and equipment damage consideration. For these reasons, there may be some functionalities of the i.MX53 chip that are not accessible on the i.MX53 Quick Start board. This board simply cannot be all things to all people. The MCIMX53SMD is available for developers looking for more options.

For developers who are interested in designing custom daughter cards for use with the Quick Start board, the following capabilities are available from the Expansion Port. Please note that many pins are muxed, so that not all features are available at the same time:

• Two Serial Peripheral Interfaces (SPI)	CSPI, eCSDPI2
• Two I2S/SSI/AC97 Ports	AUDMUX4, AUDMUX5
• Two Inter-Integrated Circuits (I2C)	I2C1, I2C2
• 2 UARTs	UART4, UART5
• SPDIF Audio	
• USB ULPI Port	USBH2
• 24-bit Data and display control signals	
• Resistive Touch Screen Interface	
• CSI Camera	

In addition to the Data/Signal traces to support the above functionality, the following power sources are also included on the Expansion Port:

• 5V_MAIN	5V	DC Power Supply
• LCD_3V2	3.2V	DCDC_3V2
• VIOHI_2V775	2.775V	VLDO4
• VLDO8_1V8	1.8V	VLDO8
• VLDO9_1V5	1.5V	VLDO9
• VLCD_BLT	Current Source	PMIC LED Driver

Note that VLDO9 is only used by the Expansion Port on the Quick Start board. The developer is free to reprogram the voltage of the LDO regulator on the PMIC for whatever voltage may be required subject to the following limitations (1.25V – 3.6V, 100mA). The proper connector to mate with Expansion Port J13 is made by Samtec, QTH-060-XX-L-D-A, where XX determines the height of the connector.

For a table of available pin-mux options, see the expansion port pin-out in section 6.

5.11. Audio

The main Audio CODEC used on the Quick Start board is the Freescale SGTL5000 Low Power Stereo Codec with Headphone Amp. The i.MX53 Applications Processor provides digital sound information from the AUDMUX module channel 5 port via I2S communications protocol. The Audio CODEC also receives command instructions from the I2C channel 2 bus and receives a 24 MHz clock input signal from GPIO_0 of the i.MX53 processor. These seven connections with the processor are the only required signals.

The Audio CODEC provides a Left and Right Stereo output signal capable of providing a 16 Ohm set of headphones/earbuds with up to 58 mW of power. The Audio CODEC is also capable of receiving a single microphone channel, and converting the information to a digital format and transmitting it back to the processor. The CODEC also generates the necessary microphone bias voltage to allow proper condenser operation.

The Quick Start board was designed to be used with a range of microphone options, including the mono-microphone/earbud sets commonly used with cellular phones. For this reason, the microphone bias voltage is connected to the microphone input signal on the Quick Start board, rather than connecting the bias voltage signal to a separate channel on the Microphone Jack (J6) and allowing a higher end microphone to connect the bias source closer to the connector. In addition, the right channel audio output of the Audio CODEC can be sent to the Microphone Jack. The Quick Start board does not come with this feature by default, but the developer can easily populate the L22 footprint with a ferrite bead or a zero Ohm jumper.

The Quick Start board is also designed with a cable detect feature on both the Headphone and Microphone Jacks. One option would be to use an audio connector with an internal flag that would make or break depending on whether the connector barrel was inserted into the jack. These connectors are available, but are often more expensive and may have supply problems. On the Quick Start board, a four pin, Audio/Video style connector was chosen to implement the cable detect feature. When a three connector cable is inserted into the connector, the cable detect pin is shorted to the ground pin, sending an active low signal back to the processor to indicate that a cable was inserted. For this reason, the ground pin on the Microphone and Headphone Jacks must be system ground and not a virtual audio ground. Therefore, the Audio CODEC was designed to use the AC Coupled audio mode which makes use of two 220uF capacitors. If the developer wishes to design a board that uses a flagged jack for cable detection or does not implement a cable detection scheme, it would then be possible to use the Direct Drive feature of the Audio CODEC and eliminate the need for the large capacitors.

The Audio CODEC can be reset by software via the I2C channel, but there is no hardware reset pin on the CODEC. Should I2C communications be lost between the Audio CODEC and the Processor, it may be necessary to shutdown DCDC_3V2 power to the Quick Start board and reinitialize the Audio CODEC by the power on sequence.

5.12. Ethernet

The Ethernet subsystem of the Quick Start board is provided by the SMSC LAN8720 Ethernet Transceiver (U17). The Ethernet Transceiver (or PHY) receives standard RMII Ethernet signals from the Fast Ethernet Controller (FEC) of the i.MX53 Applications Processor. The Processor takes care of all Ethernet protocols at the MAC layer and above. The PHY is responsible only for the Link Layer formatting. The PHY receives a 50MHz clock signal from the oscillator X1. On initial versions of the i.MX53 silicon, this clock signal was shared with the SATA module of the i.MX53 Processor. On current versions of the Quick Start board, the 50 MHz clock signal is only used to support the Ethernet subsystem.

The two control traces from the i.MX53 Processor to the Ethernet PHY are and Active low Interrupt trace (FEC_nINT) and an Active Low reset line (FEC_nRST). When the PHY comes out of reset, it is internally programmed to establish communications with an attached Ethernet device and be ready to correctly format all communications, whether they are being transmitted or received by the processor. If communications become unreliable, the processor can restart the PHY by forcing it into reset and allowing the PHY come back out of reset normally.

The PHY is connected directly to the integrated magnetics of the Ethernet/Dual USB connector (J2), with two pairs of differential traces for receive and transmit, and connections to the indicator LEDs. The differential pair traces are biased externally with 49.9 1% Ohm pull-up resistors. The magnetics included in the Ethernet connector were chosen to enable the auto-negotiation feature of the PHY to work correctly. When initially connected to another Ethernet device, the PHY will negotiate to determine if it connected to a switch type device or another Ethernet end device, and will reconfigure the Transmit and Receive inputs to correctly match the device attached. This eliminates the need for cross-over cables when directly connecting to another Ethernet end device.

The LED status indicators are driven by the PHY to show a connected link and activity on the link. It is important to note that the LED control lines from the PHY also serve as PHY feature selection options. At boot time, the LED1 control pin serves to determine whether the 1.2V internal regulator should be turned on or off, and the LED2 control pins determines whether the PHY accepts an external reference clock or internally generates the clock signal and outputs it to the processor for reference. See the LAN8720 datasheet for further details.

If a board designer wishes to reduce costs in the implementation of Ethernet, it is possible to replace the oscillator with a lower cost 50 MHz crystal. The LAN8720 has more information on this implementation. The oscillator was originally designed to support two different subsystems on the board, and is no longer an necessary expense.

5.13. USB Host connections

The i.MX53 Applications Processors contains three USB 2.0 Host ports and one USB 2.0 OTG port. Of these four ports, only two (Host1 and OTG) are connected internally to a transceiver to provide USB Data signals suitable (UTMI) for direct connection to a USB jack. The other two (Host2 and Host3) ports require a connection to an external serial transceiver or a direct connection to another USB device using ULPI communications. On the Quick Start board, only the Host1 and OTG ports are utilized

The Host1 USB Port is connected to the Upper USB-A Host slot of the Ethernet/Dual USB Connector (J2). A Common Mode Choke is inserted in the USB data lines to ensure compliance with North America and Europe emissions testing. The 5V-Main power rail is connected to the USB_5V pins of the Ethernet/Dual USB Connector, after first going through a 1.1A fuse for over-current protection and a PNP MOSFET to allow the Processor to control USB_5V power (USB_PWREN). No attempt is made on the Quick Start board to regulate the actual voltage level of this power rail, nor to regulate the amount of current drawn by each port (except by the 1.1A fuse). Power from the DCDC_3V2 and the VBUS_2V5 voltage rails are supplied to the HOST1 part through small value resistors for noise filtering. The USB_H1_VBUS is a reference voltage signal only and is provide by the 5V_Main power rail via the USB Bus Power control MOSFET.

In much the same way as described above, the OTG Port is connected to the Lower USB-A Host slot of the Ethernet/Dual USB Connector (J2). The USB_5V power source is the same source as supplied to the upper port, but the USB OTG data lines go through a separate Common Mode Choke. The difference between the Host1 and the OTG Port connections is that the OTG Port is also connected to a Micro-B USB Device port. In the normal implementation of OTG, the same connector is used for both Host and Device USB connections. A high or low signal on the USB ID pin would indicate whether a Host (A) plug or a Device (B) plug was attached. Since most Host plugs available today are the full size plugs, but most portable USB Devices are moving toward the Micro-B connector, a two connector approach was implemented on the Quick Start board. The USB_5V power supplied by an attached Host device through the Micro-B connector will provide a TTL logic high signal to the OTG Port through USB_OTG_ID (pin C16). The ID signal is corrected to the proper logic by way of a simple voltage divider. When the OTG Port senses this logic high condition, the OTG Port will switch to device operations, regardless of whether there is a USB Device plugged into the Lower USB Host Port. This USB OTG configuration is used for demonstration purposes only and is not recommended for mass production. The developer is cautioned to only plug one cable into the Lower USB Host Port OR the micro-B Device port at a time, since two cables might degrade the USB signal beyond acceptable operating limits.

The External USB 5V power supplied by a connected USB device is only used in two locations on the Quick Start board. It is used to provide the USB ID signal (passive sense) and to provide the USB_OTG_VBUS reference signal. For the board designer, two 6.04K Ohm 1% resistors are used, one attached to each of the Host1 and OTG Ports. These resistors are used to set the Band Gap levels.

5.14. SATA

The internal SATA PHY of the i.MX53 Applications Processor provides the two differential pair data signals necessary for SATA operations. No external transceiver is required. Each of the four data lines pass through a 0.01 uF capacitor for decoupling. These capacitors are placed as close to the SATA connector as possible. The Processor SATA module receives 2.5V power from VBUCKPERI for the PHY portion of the module and 1.3V power from VLDO5_1V3 for the controller portion of the module. A 191 Ohm 1% resistor is required to be connected to the SATA_REXT pin (C13). This resistor received a small, constant current at the initialization of the SATA module to allow for cable impedance calibration. After module initialization, this resistor is not used.

The i.MX53 Applications Processor provides two pins to receive an external differential pair clock input for use by the SATA module. Testing of the i.MX53 Processor confirms that the internally generated clock signal is working properly. Therefore the external clock components are not populated and the eFuses for the Processor are configured for internal clock operation.

The 7-pin SATA data connector is suitable for use will all SATA capable storage media devices including Hard Drives and Optical Media storage devices (DVD/CD). It is possible to configure the Quick Start Board to boot directly from a SATA device. To enable the Quick Start board to boot from SATA, the developer will have the make the following modifications to the board:

1) Solder a 10-DIP Switch onto the pads for SW1. A suitable switch is manufactured by Multicomp (MCNHDS-10-T). Move Switches 6 and 8 to the ON (UP) position. Alternately, two wires can be soldered between pads 6 & 15 and 8 & 13 on the SW1 footprint (this effectively take the place of moving the switch to the on position.

2) Rotate R46 in the clockwise direction by 90 degrees pivoting around pad R46.2. Add a wire from the unconnected end of the 4.7K Ohm resistor to as suitable ground point. The pad for R47.2 is the closest ground point.

Table 12 below shows the TTL logic levels on the external boot configuration (BOOT_CFG1) scheme to modify the board from SD/MMC boot to use SATA boot.

	CFG1[7]	CFG1[6]	CFG1[5]	CFG1[4]	CFG1[3]
SD/MMC Boot (Default)	0	1	-	-	-
SATA Boot	0	0	1	0	1

Table 12. SATA Boot Mode Configuration Table.

5.15. Debug UART Serial Port

The i.MX53 Applications Processor has 5 independent UART Ports (UART1 – UART5). The Processor will boot by default using UART1 to output serial debugging information, specifically on pins CSI0_DAT10 (pin R5) and CSI0_DAT11 (pinT2). These two pins are output from the NVCC_CSI module, which is pulled up to 1.8V on the Quick Start board. In order to convert the UART Transmit and Receive signal to a 3.2V logic signal, two single-direction level shifters (U25, U26) are used. The level shifted signals are sent to a low cost, RS232 transceiver, which reformats the signals to the correct voltages and drives the signals. The resulting cable ready signals are then connected to the RS232 Debug connector. No RTS or CTS signals are sent from the Processor to the Debug connector since these signals are commonly ignored by most applications. The required terminal settings to receive debug information during the boot cycle are shown in **Table 13**:

Data Rate	115,200 Baud
Data bits	8
Parity	None
Stop bits	1
Flow Control	None

Table 13. **Terminal Setting Parameters**

If the developer wishes to repurpose the Debug UART connector in software into an Applications connector, the Quick Start board can support this using a Null Modem Adapter. The adapters are readily available from most cable and electronics stores at a small cost.

See the section on the Expansion Port to find how to access some of the other UART channels on the Quick Start board.

5.16. JTAG Operations

The i.MX53 Applications Processor accepts five JATG signals from an attached debugging device on dedicated pins. A sixth pin on the processor accepts a board HW configured input specific to the Quick Start board only. The five JTAG signal used by the Processor are:

- JTAG_TCK TAP Clock
- JTAG_TMS TAP Machine State
- JTAG_TDI TAP Data In
- JTAG_TDO TAP Data Out
- JTAG_nTRST TAP Reset Request (Active Low)

The TAP Clock signal is provided by the attached debugging device and serves as a reference for data exchange between the debugging device and the Processor. The TAP Machine State is a logical signal provided by the debugging device to let the Processor (or Target) know what state to enter next. Per JATG specifications, all questions of state have two options that can be selected with either a 'high' or 'low' signal. The TAP Data In and TAP Data Out signal are used only for data transfer.

The Active Low TAP Reset Request is initiated by the debugging device and resets the TAP (JTAG) module within the Processor. This gives the debugging device the ability to reset the internal Processor JTAG module if required without affecting the remainder of the Processor. The system JTAG reset signal provided by the attached debugging device does not go to the JTAG module of the processor, but goes to the external processor reset circuitry which will fully reset the i.MX53 processor, but not the power rails.

The JTAG_MOD pin used by the JTAG module of the i.MX53 Processor determines how much of the i.MX53 processor is connected to the JTAG Debugging device. In the pull-down mode (default on the Quick Start board) allows all of the i.MX53 TAPs (SJC, SDMA, ARM) to be connected to the debugging device in a daisy chain connection. If the JTAG_MOD pin is pulled high, then the attached debugging device can only access the SJC TAP.

Three other common JTAG signals used by debugging devices (Return Clock, Data Enable, and Data Acknowledge) are not used by the i.MX53 Applications Processor and are either pulled-up or pulled-down by the Quick Start board.

On the Quick Start board, the logic signals for JTAG are designed to be 1.8V. A 1.8V reference signal from VLDO8_1V8 is connected to pin 1 of the 20-pin JTAG connector to provide this logic level signal to the attached debugging device. In addition, for debugging devices that required power, a limited amount (~0.5 A) of 3.2V power can be supplied to the debugging device. If the device requires 1.8V power (instead of 3.2V power), the Quick Start board can be configured to supply this as well, but in a very limited amount (100 mA).

6. Connector Pin-Outs

This section fully describes the signals going to each of the 13 connectors used on the Quick Start board. Although this information is available on the schematic, the footprint used in manufacturing the PCB is also included to provide a map to the actual signals on the board. The image of the footprint provide is for the PCB side that the connector mounts. Therefore, to find corresponding pins on the opposite side of the PCB, the image should be reversed. In addition to the pin tables and footprints, there is also a pin-mux table provided for the Expansion Port so that the developer can readily see the possible signals brought out through the Expansion Port. These details are included in the following tables and figures:

Table 14.	**Power Jack (J1)**	**Figure 20.**	**Power Jack (J1)**
Table 15.	**Micro-B USB Connector (J3)**	**Figure 21.**	**Micro-B USB Connector (J3)**
Table 16.	**Ethernet/Dual USB Conn (J2)**	**Figure 22.**	**Ethernet/Dual USB Conn (J2)**
Table 17.	**Headphone Connector (J18)**	**Figure 23.**	**Headphone Connector (J18)**
Table 18.	**Microphone Connector (J6)**	**Figure 24.**	**Microphone Connector (J6)**
Table 19.	**VGA DB15 Connector (J8)**	**Figure 25.**	**VGA DB15 Connector (J8)**
Table 20.	**LVDS Connector (J9)**	**Figure 26.**	**LVDS Connector (J9)**
Table 21.	**SATA Data Connector (J7)**	**Figure 27.**	**SATA Data Connector (J7)**
Table 22.	**SD Card Connector (J5)**	**Figure 28.**	**SD Card Connector (J5)**
Table 23.	**microSD Card Connector (J4)**	**Figure 29.**	**microSD Card Connector (J4)**
Table 24.	**Debug UART Connector (J16)**	**Figure 30.**	**Debug UART Connector (J16)**
Table 25.	**JTAG Connector (J15)**	**Figure 31.**	**JTAG Connector (J15)**
Table 26.	**Expansion Port (J13)**	**Figure 32.**	**Expansion Port (J13)**
Table 27.	**Expansion Port Pin-Mux Table**		

Power Jack (J1)

Positive Terminal	1
Negative Terminal	2
Ground Terminal	3

Table 14. Power Jack (J1)

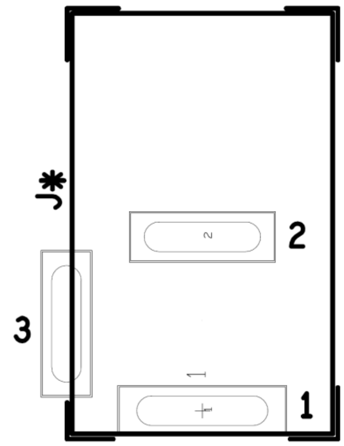


Figure 20. Power Jack (J1)

Micro-B USB (J3)

5V Power	1
Data Negative	2
Data Positive	3
No Connect (ID)	4
Ground	5
Chassis Ground	6
Chassis Ground	7
Chassis Ground	8
Chassis Ground	9
Chassis Ground	10
Chassis Ground	11

Table 15. Micro-B USB Connector (J3)

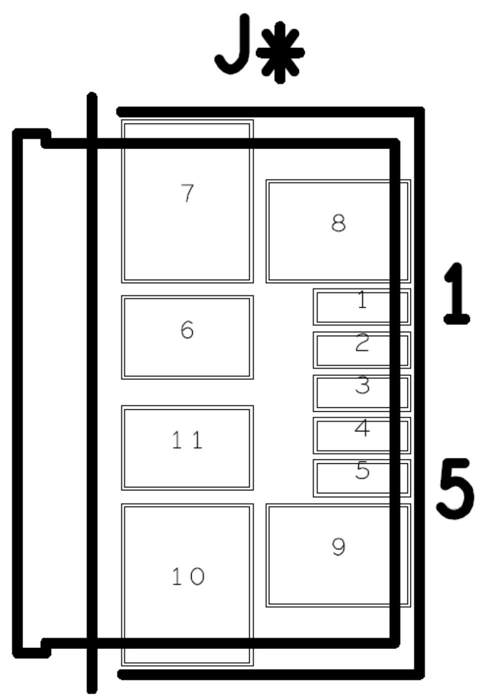


Figure 21. Micro-B USB Connector (J3)

Ethernet/Dual USB (J2)

Transmit Core Tap	1
Transmit Data Positive	2
Transmit Data Negative	3
Receive Data Positive	4
Receive Data Negative	5
NC6	6
NC7	7
NC8	8
NC9	9
Receive Core Tap	10
LED1 Anode	11
LED1 Cathode	12
LED2 Anode	13
LED2 Cathode	14
Top USB 5V Power	T1
Top USB Data Negative	T2
Top USB Data Positive	T3
Top USB Ground	T4
Bottom USB 5V Power	B1
Bottom USB Data Negative	B2
Bottom USB Data Positive	B3
Bottom USB Ground	B4
Shield Ground	S1
Shield Ground	S2
Shield Ground	S3
Shield Ground	S4
Shield Ground	S5
Shield Ground	S6
Shield Ground	S7
Shield Ground	S8

Table 16. Ethernet/Dual USB Conn (J2)

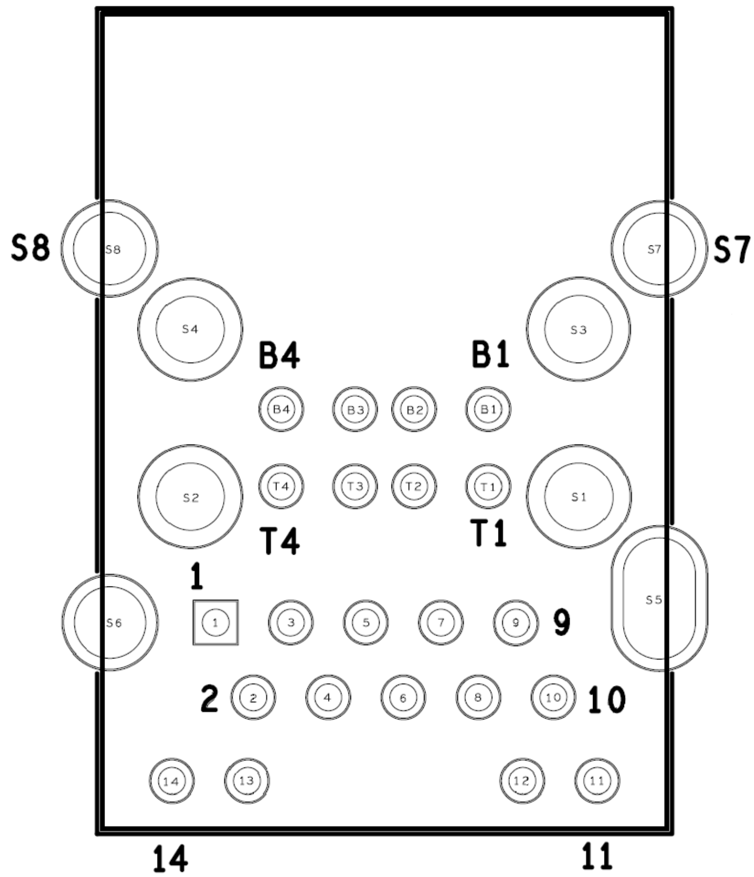


Figure 22. Ethernet/Dual USB Conn (J2)

Headphone Connector (J18)

Right channel	1
Left Channel Ground Flag	3
Left Channel (Tip)	4
Analog Ground (Ring)	5
Plug Sense	6

Table 17. Headphone Connector (J18)

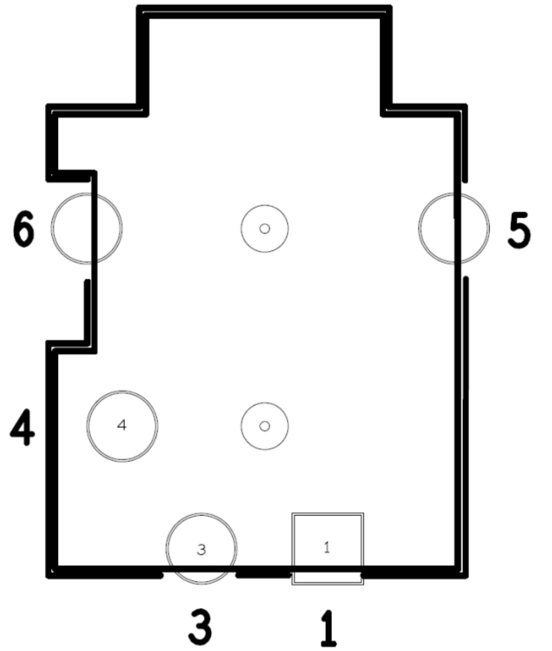


Figure 23. Headphone Connector (J18)

Microphone Connector (J6)

Right channel	1
Microphone Ground Flag	3
Microphone Signal (Tip)	4
Analog Ground (Ring)	5
Plug Sense	6

Table 18. Microphone Connector (J6)

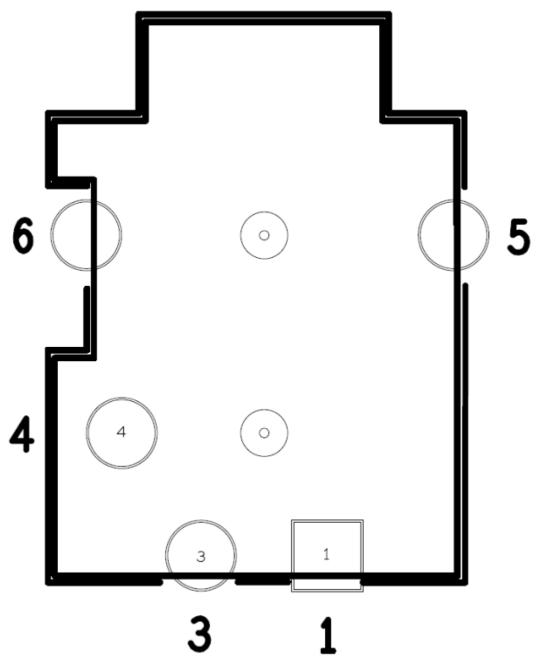


Figure 24. Microphone Connector (J6)

VGA DB15 (J8)

Component Video Pr	1
Component Video Y	2
Component Video Pb	3
No Connect	4
Ground	5
DAC Ref Ground	6
DAC Ref Ground	7
DAC Ref Ground	8
5V VGA REF	9
Ground	10
No Connect	11
VGA I2C (Data)	12
VGA Horiz Synch	13
VGA Vert Synch	14
VGA I2C (Clock)	15

Table 19. VGA DB15 Connector (J8)

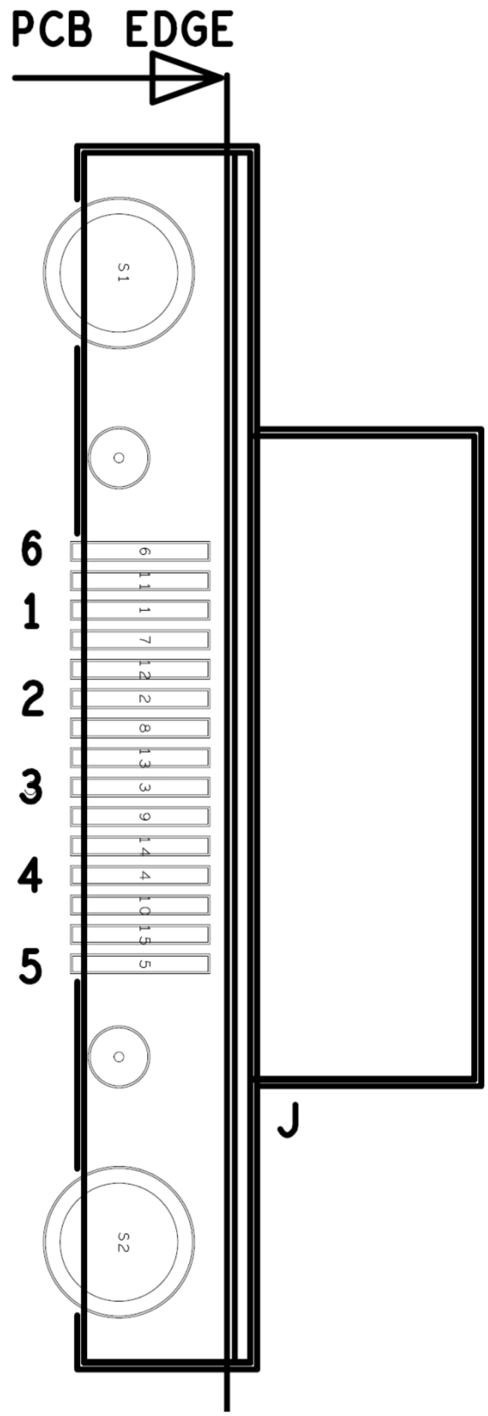


Figure 25. VGA DB15 Connector (J8)

LVDS Connector (J9)

Backlight Enable	1
VCC 3V2 Supply	2
VCC 3V2 Supply	3
EDID 3V2 Supply	4
LED Brightness Adjust	5
EDID I2C (Clock)	6
EDID I2C (Data)	7
LVDS Transmit 0 Negative	8
LVDS Transmit 0 Positive	9
Ground	10
LVDS Transmit 1 Negative	11
LVDS Transmit 1 Positive	12
Ground	13
LVDS Transmit 2 Negative	14
LVDS Transmit 2 Positive	15
Ground	16
LVDS Clock Negative	17
LVDS Clock Positive	18
Ground	19
Touch Panel 5V Supply	20
Touch Panel 5V Supply	21
Ground	22
Ground	23
LED 5V Supply	24
LED 5V Supply	25
LED 5V Supply	26
LVDS I2C (Clock)	27
LVDS I2C (Data)	28
LVDS I2C Interrupt	29
No Connect	30

Table 20. LVDS Connector (J9)

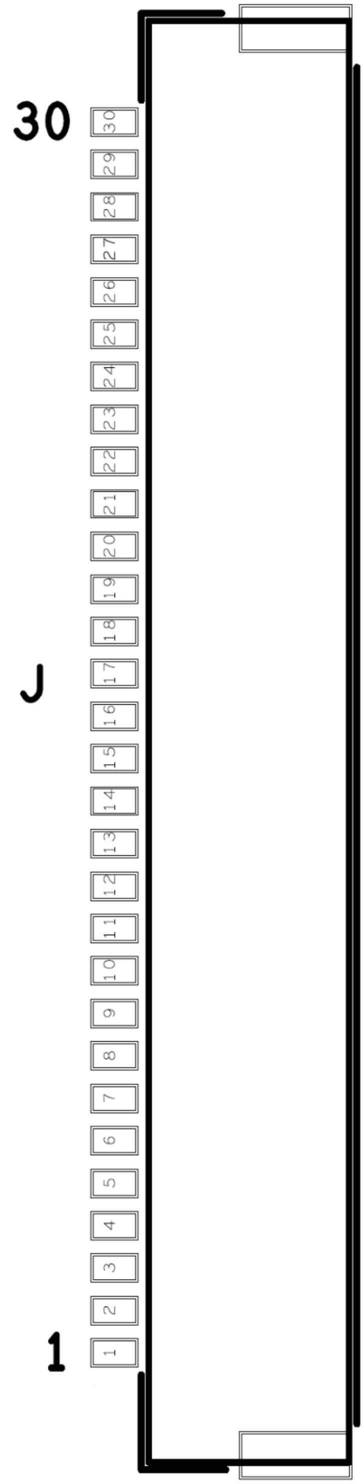


Figure 26. LVDS Connector (J9)

SATA DATA Connector (J7)

Ground	1
Transmit Data Positive	2
Transmit Data Negative	3
Ground	4
Receive Data Negtive	5
Receive Data Positive	6
Ground	7

Table 21. SATA Data Connector (J7)

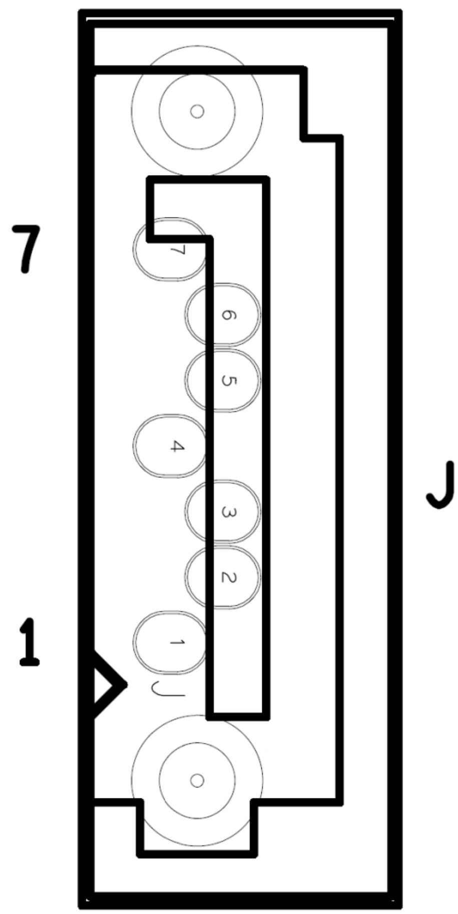


Figure 27. SATA Data Connector (J7)

SD Card Connector (J5)

Data3	1
Command	2
Ground	3
VCC 3V2 Supply	4
Clock	5
Ground	6
Data0	7
Data1	8
Data2	9
Data4	10
Data5	11
Data6	12
Data7	13
Card Detect	14
Write Protect	15
Shield Ground	16
Shield Ground	17
Shield Ground	18
Shield Ground	19

Table 22. SD Card Connector (J5)

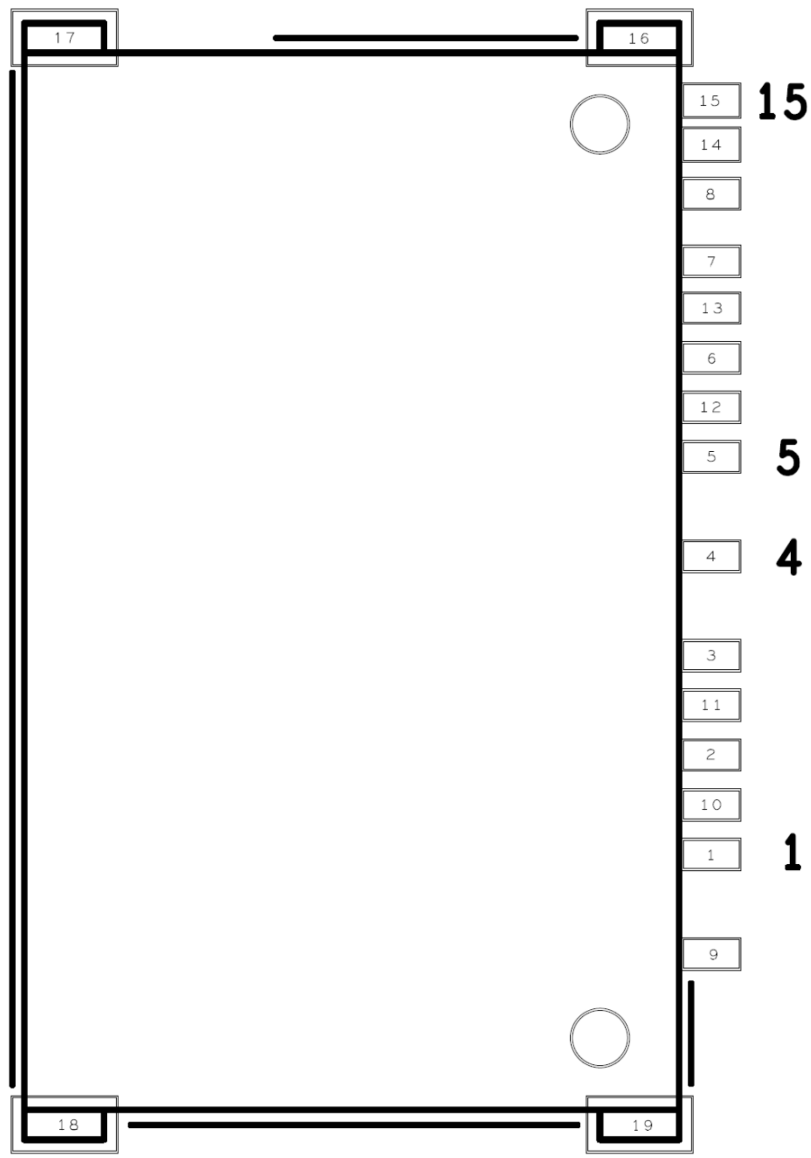


Figure 28. SD Card Connector (J5)

microSD Card Connector (J4)

Data2	1
Data3	2
Command	3
VCC 3V3 Supply	4
Clock	5
Ground	6
Data0	7
Data1	8
Shield GND1	SH1
Shield GND2	SH2
Shield GND3	SH3
Shield GND4	SH4

Table 23. microSD Card Connector (J4)

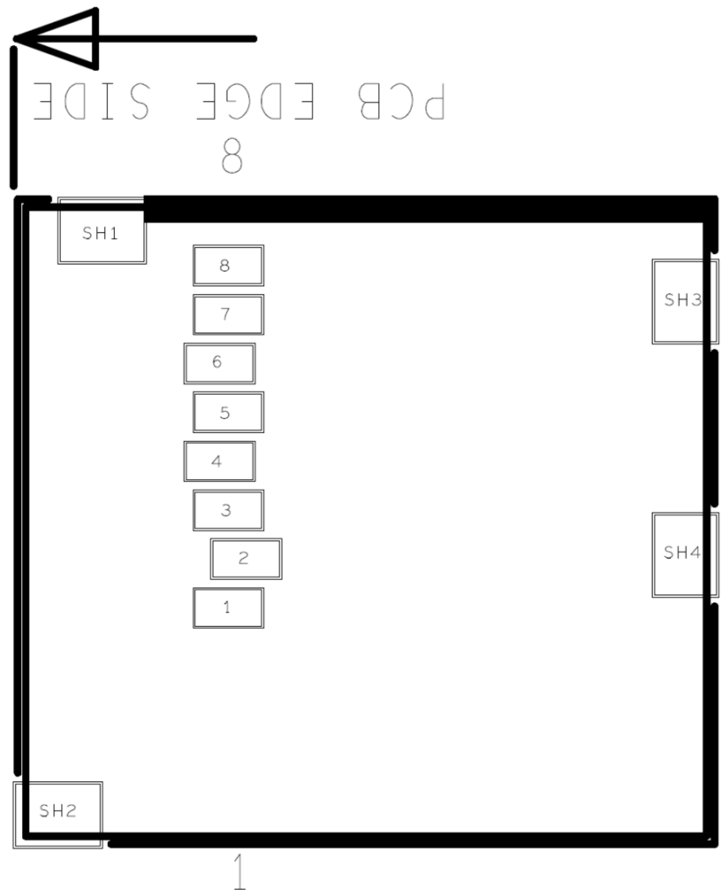


Figure 29. microSD Card Connector (J4)

Debug UART Connector (J16)

No Connect (CD)	1
Data Transmit	2
Data Receive	3
No Connect (DTR)	4
Ground	5
No Connect (DSR)	6
No Connect (RTS)	7
No Connect (CTS)	8
No Connect (RI)	9
Shield Ground	M1
Shield Ground	M2

Table 24. Debug UART Connector (J16)

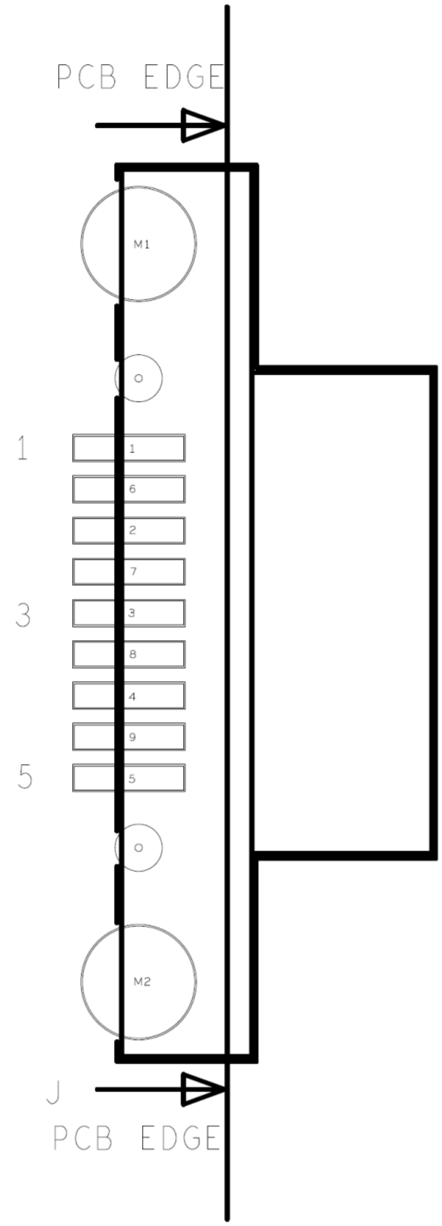


Figure 30. Debug UART Connector (J16)

JTAG

Connector (J15)

1.8V Logic Reference	1
3.3V JTAG Supply Voltage	2
JTAG TAP Reset (Active Low)	3
Ground	4
JTAG Test Data In	5
Ground	6
JTAG TAP Machine State	7
Ground	8
JTAG TAP Clock	9
Ground	10
RTCK (Pulled Low)	11
Ground	12
JTAG Test Data Out	13
Ground	14
JTAG System Reset (Active Low)	15
Ground	16
Debug Request (Pulled High)	17
Ground	18
Debug Acknowledge (Pulled Low)	19
Ground	20

Table 25. JTAG Connector (J15)

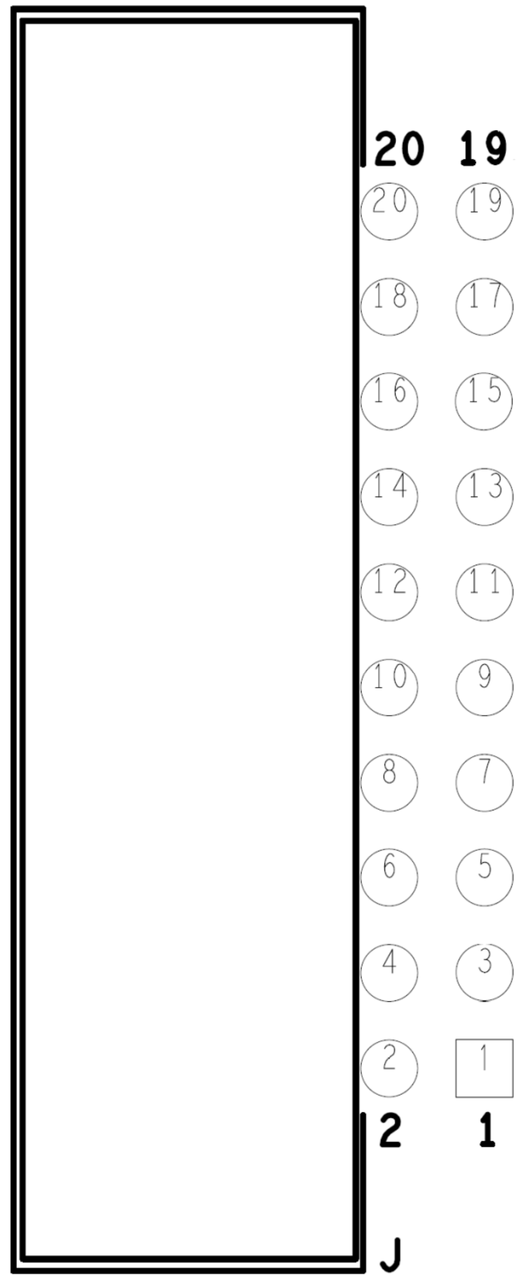


Figure 31. JTAG Connector (J15)

Expansion Port Connector (J13)

SH8	Shield Ground	Shield Ground	SH7
120	No Connect	No Connect	119
118	No Connect	Display Read	117
116	Display Data Ready	1.5V Power (VLDO9)	115
114	Display Horiz Synch	1.5V Power (VLDO9)	113
112	Backlight Brightness Adj	1.5V Power (VLDO9)	111
110	Display Vert Synch	Display Write	109
108	Display Data23	Disp Chip Sel1 (Act Low)	107
106	Display Data22	Disp Chip Sel0 (Act Low)	105
104	Display Data21	Ground	103
102	Display Data20	Touch Screen X-Neg	101
100	Display Data19	Touch Screen X-Pos	99
98	Display Data18	Touch Screen Y-Neg	97
96	Display Data17	Touch Screen Y-Positive	95
94	Display Data16	Ground	93
92	Display Data15	IIS Reset	91
90	Display Data14	IIS Clock	89
88	Display Data13	IIS Master Out-Slave In	87
86	Display Data12	IIS Master In-Slave Out	85
84	Display Data11	Exp Card ID1	83
82	Display Data10	IIS Chip Sel (Active Low)	81
80	Display Data09	Display Power Enable	79
78	Display Data08	5V Power	77
76	Display Data07	5V Power	75
74	Display Data06	5V Power	73
72	Display Data05	No Connect	71
70	Display Data04	No Connect	69
68	Display Data03	No Connect	67
66	Display Data02	No Connect	65
64	Display Data01	Audio System Clock	63
62	Display Data00	Exp Card ID0	61
SH6	Shield Ground	Shield Ground	SH5

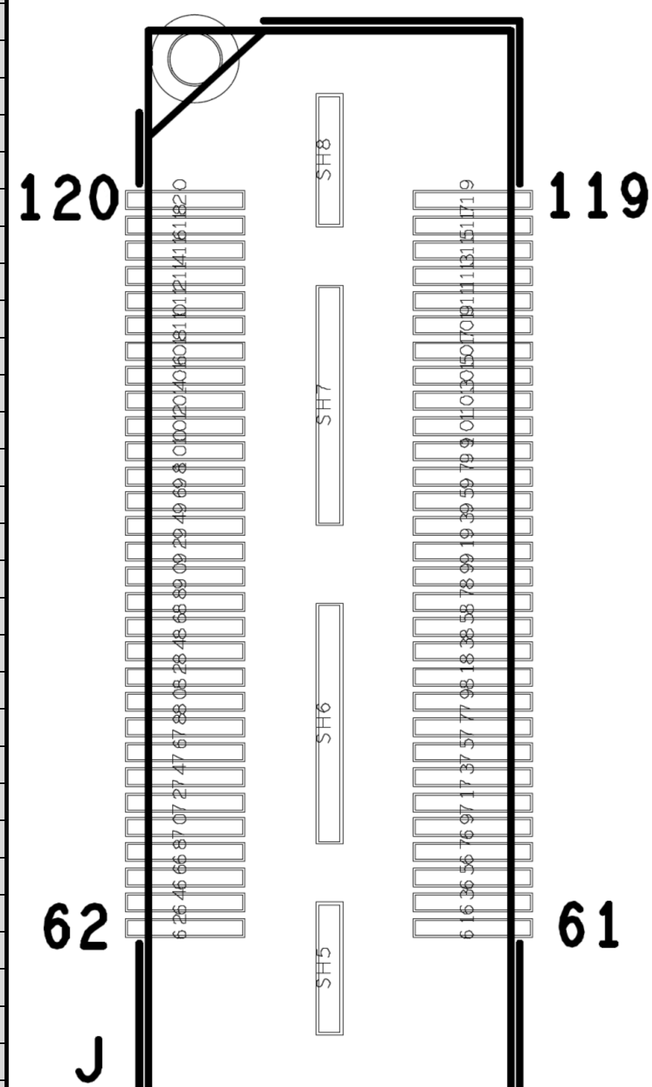


Table 26. Expansion Port (J13)

Figure 32. Expansion Port (J13)

Expansion Port Connector (J13)

SH4	Shield Ground	Shield Ground	SH3
60	Ground	Display Rst (Active Low)	59
58	Display Vert Synch	No Connect	57
56	Display Horiz Synch	No Connect	55
54	Ground	Display Power Down	53
52	Display Data19	No Connect	51
50	Display Data18	3.2V Power	49
48	Ground	3.2V Power	47
46	Display Data17	3.2V Power	45
44	Display Data16	Display Data Clock	43
42	Ground	No Connect	41
40	SPDIF Data Transmit	No Connect	39
38	SPDIF Data Clock	No Connect	37
36	Ground	Display Pixel Clock	35
34	Display Data15	Display Reset	33
32	Display Data14	I2C Clock	31
30	Ground	I2C Data	29
28	Display Data13	No Connect	27
26	Display Data12	1.8V Power (VLDO8)	25
24	Ground	No Connect	23
22	No Connect	No Connect	21
20	No Connect	1.8V Power (VLDO8)	19
18	Ground	1.8V Power (VLDO8)	17
16	No Connect	Display Backlight Return	15
14	No Connect	5V Power	13
12	Ground	5V Power	11
10	No Connect	Display Backlight Power	9
8	5V Power	5V Power	7
6	Ground	3.2V Power	5
4	5V Power	2.775V Power (VLDO4)	3
2	5V Power	1.8V Power (VLDO8)	1
SH2	Shield Ground	Shield Ground	SH1

Table 26. Expansion Port (J13)

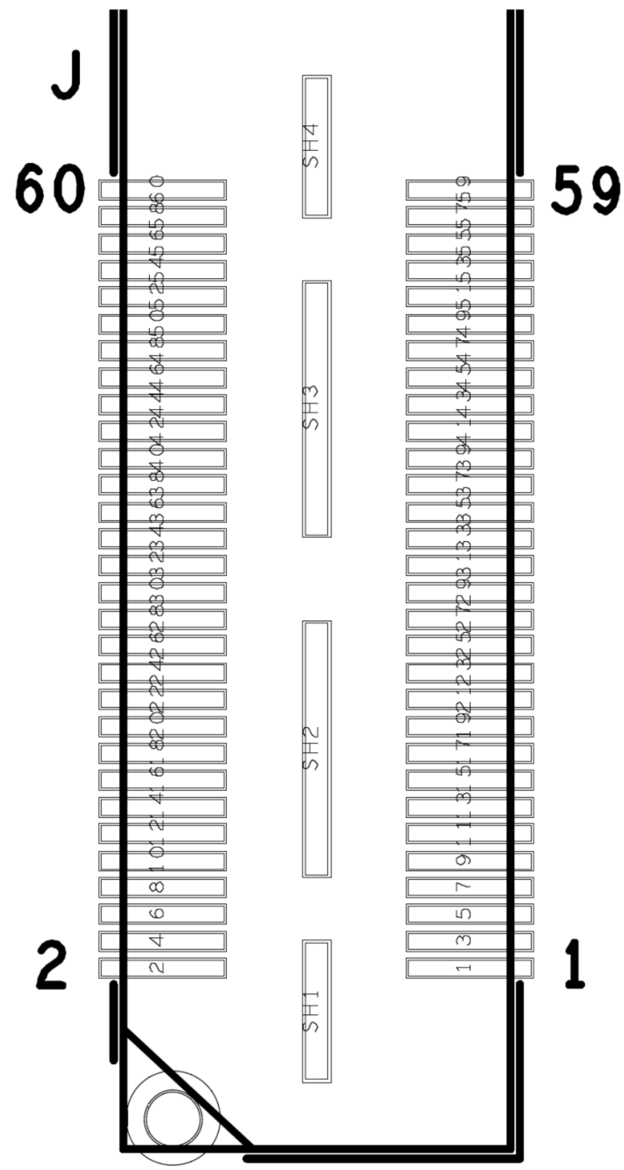


Figure 32. Expansion Port

J13 PIN	J13 Name	i.MX53 Pin Name	ALT(1)	ALT(2)	ALT(3)
26	CSI0_DAT12	CSI0_DAT12	GPIO5_30	uart4 TXD_MUX	
28	CSI0_DAT13	CSI0_DAT13	GPIO5_31	uart4 RXD_MUX	
29	I2C2_SDA	KEY_ROW3	GPIO4_13	H2_DP	ASRC_EXT_CLK
31	I2C2_SCL	KEY_COL3	GPIO4_12	H2_DM	spdif IN1
32	CSI0_DAT14	CSI0_DAT14	GPIO6_0	uart5 TXD_MUX	
33	DISP0_RESET	EIM_WAIT	GPIO5_0	WEIM_DTACK_B	
34	CSI0_DAT15	CSI0_DAT15	GPIO6_1	uart5 RXD_MUX	
35	CSI0_PIXCLK	CSI0_PIXCLK	GPIO5_18		
38	PCLOCK	GPIO_7	GPIO1_7	EPITO	can1 TXCAN
40	SPDIF_TX	GPIO_17	GPIO7_12	SDMA_EXT_EVENT0	PMIC_RDY
43	DISP0_DCLK	DI0_DISP_CLK	GPIO4_16	USBH2_DIR	
44	CSI0_DAT16	CSI0_DAT16	GPIO6_2	uart4 RTS	
46	CSI0_DAT17	CSI0_DAT17	GPIO6_3	uart4 CTS	
50	CSI0_DAT18	CSI0_DAT18	GPIO6_4	uart5 RTS	
52	CSI0_DAT19	CSI0_DAT19	GPIO6_5	uart6 CTS	
53	SCSI0_PWDN	NANDF_RB0	GPIO6_10		
56	CSI0_VSYNCH	CSI0_VSYNCH	GPIO5_21		
58	CSI0_HSYNCH	CSI0_MCLK	GPIO5_19	ccm CSI0_MCLK	
59	CSI0_RSTB	NANDF_WP_B	GPIO6_9		
62	DISP0_DAT0	DISP0_DAT0	GPIO4_21	cspi SCLK	USBH2_DAT0
63	GPIO_0(CLK0)	GPIO_0	GPIO1_0	KEY_COL5	SSI_EXT1_CLK
64	DISP0_DAT1	DISP0_DAT1	GPIO4_22	cspi MOSI	USBH2_DAT1
66	DISP0_DAT2	DISP0_DAT2	GPIO4_23	cspi MISO	USBH2_DAT2
68	DISP0_DAT3	DISP0_DAT3	GPIO4_24	cspi SS0	USBH2_DAT3
70	DISP0_DAT4	DISP0_DAT4	GPIO4_25	cspi SS1	USBH2_DAT4
72	DISP0_DAT5	DISP0_DAT5	GPIO4_26	cspi SS2	USBH2_DAT5
74	DISP0_DAT6	DISP0_DAT6	GPIO4_27	cspi SS3	USBH2_DAT6
76	DISP0_DAT7	DISP0_DAT7	GPIO4_28	cspi RDY	USBH2_DAT7
78	DISP0_DAT8	DISP0_DAT8	GPIO4_29	pwm1 PWMO	wdog1 WDOG_B

Legend

UART4	AUDMUX4	I2C1	ECSPI2	USBH2
UART5	AUDMUX5	I2C2	CSPI	SPDIF

Table 27. Expansion Port Pin-Mux Table

J13 PIN	J13 Name	ALT(4)	ALT(5)	ALT(6)	ALT(7)
26	CSI0_DAT12	USBH3_DATA0	DEBUG_PC6	EMI_DEBUG41	tpiu TRACE9
28	CSI0_DAT13	USBH3_DATA1	DEBUG_PC7	EMI_DEBUG42	tpiu TRACE10
29	I2C2_SDA	i2c2 SDA	32K_OUT	ccm PLL4_BYP	usb1 LINESTATE0
31	I2C2_SCL	i2c2 SCL	ecspi1 SS3	fec CRS	usb1 SIECLOCK
32	CSI0_DAT14	USBH3_DATA2	DEBUG_PC8	EMI_DEBUG43	tpiu TRACE11
33	DISP0_RESET				
34	CSI0_DAT15	USBH3_DATA3	DEBUG_PC9	EMI_DEBUG44	tpiu TRACE12
35	CSI0_PIXCLK		DEBUG_PC0	EMI_DEBUG29	
38	PCLOCK	uart2 TXD_MUX	firi RXD	spdifPLOCK	ccm PLL2_BYP
40	SPDIF_TX	CE_RTC_FSV_TRIG	spdif OUT1	SNOOP2	JTAG_ACT
43	DISP0_DCLK		DEBUG_CORE_STATE0	EMI_DEBUG0	usb1 AVALID
44	CSI0_DAT16	USBH3_DATA4	DEBUG_PC10	EMI_DEBUG45	tpiu TRACE13
46	CSI0_DAT17	USBH3_DATA5	DEBUG_PC11	EMI_DEBUG46	tpiu TRACE14
50	CSI0_DAT18	USBH3_DATA6	DEBUG_PC12	EMI_DEBUG47	tpiu TRACE15
52	CSI0_DAT19	USBH3_DATA7	DEBUG_PC13	EMI_DEBUG48	usb2 BISTOK
53	SCSI0_PWDN				usb1 VSTATUS3
56	CSI0_VSYNCH		DEBUG_PC3	EMI_DEBUG32	tpiu TRACE0
58	CSI0_HSYNCH		DEBUG_PC1		
59	CSI0_RSTB				usb1 VSTATUS2
62	DISP0_DAT0		DEBUG_CORE_RUN	EMI_DEBUG5	usb2 TXREADY
63	GPIO_0(CLK0)	EPITO	SRTC_ALARM_DEB	USBH1_PWR	csu TD
64	DISP0_DAT1		DEBUG_EVENT_CHAN_SEL	EMI_DEBUG6	usb2 RXVALID
66	DISP0_DAT2		DEBUG_MODE	EMI_DEBUG7	usb2 RXACTIVE
68	DISP0_DAT3		DEBUG_EVENT_BUS_ERROR	EMI_DEBUG8	usb2 RXERROR
70	DISP0_DAT4		DEBUG_BUS_RWB	EMI_DEBUG9	usb2 SIECLOCK
72	DISP0_DAT5		DEBUG_MATCHED_DMBUS	EMI_DEBUG10	usb2 LINESTATE0
74	DISP0_DAT6		DEBUG_RTBUFFER_WRITE	EMI_DEBUG11	usb2 LINESTATE1
76	DISP0_DAT7		DEBUG_EVENT_CHANNEL0	EMI_DEBUG12	usb2 VBUSVALID
78	DISP0_DAT8		DEBUG_EVENT_CHANNEL1	EMI_DEBUG13	usb2 AVALID

Legend

UART4	AUDMUX4	I2C1	ECSPI2	USBH2
UART5	AUDMUX5	I2C2	CSPI	SPDIF

Table 27. Expansion Port Pin-Mux Table (con)

J13 PIN	J13 Name	i.MX53 Pin Name	ALT(1)	ALT(2)	ALT(3)
79	DISP0_POWER_EN	EIM_D24	GPIO3_24	uart3 TXD_MUX	ecspi1 SS2
80	DISP0_DAT9	DISP0_DAT9	GPIO4_30	pwm2 PWMO	wdog2 WDOG_B
81	DSIP0_SER_nCS	EIM_D20	GPIO3_20	DI0_PIN16	SER_DISP0_CS
82	DISP0_DAT10	DISP0_DAT10	GPIO4_31	USBH2_STP	
84	DISP0_DAT11	DISP0_DAT11	GPIO5_5	USBH2_NXT	
85	DISP0_SER_MISO	EIM_D22	GPIO3_22	DI0_PIN1	DISPB0_SER_DIN
86	DISP0_DAT12	DISP0_DAT12	GPIO5_6	USBH2_CLK	
87	DISP0_SER_MOSI	EIM_D28	GPIO3_28	uart2 CTS	DISPB0_SER_DIO
88	DISP0_DAT13	DISP0_DAT13	GPIO5_7		AUD5_RXFS
89	DISP0_SER_SCLK	EIM_D21	GPIO3_21	DI0_PIN17	DISPB0_SER_CLK
90	DISP0_DAT14	DISP0_DAT14	GPIO5_8		AUD5_RXC
91	DISP0_SER_RS	EIM_D29	GPIO3_29	uart2 RTS	DISPB0_SER_RS
92	DISP0_DAT15	DISP0_DAT15	GPIO5_9	ecspi1 SS1	ecspi2 SS1
94	DISP0_DAT16	DISP0_DAT16	GPIO5_10	ecspi2 MOSI	AUD5_TXC
96	DISP0_DAT17	DISP0_DAT17	GPIO5_11	ecspi2 MISO	AUD5_TXD
98	DISP0_DAT18	DISP0_DAT18	GPIO5_12	ecspi2 SS0	AUD5_TXFS
100	DISP0_DAT19	DISP0_DAT19	GPIO5_13	ecspi2 SCLK	AUD5_RXD
102	DISP0_DAT20	DISP0_DAT20	GPIO5_14	ecspi1 SCLK	AUD4_TXC
104	DISP0_DAT21	DISP0_DAT21	GPIO5_15	ecspi1 MOSI	AUD4_TXD
105	DISP0_nCS0	EIM_D23	GPIO3_23	uart3 CTS	uart1 DCD
106	DISP0_DAT22	DISP0_DAT22	GPIO5_16	ecspi1 MISO	AUD4_TXFS
107	DISP0_nCS1	EIM_A25	GPIO5_2	ecspi2 RDY	DI1_PIN12
108	DISP0_DAT23	DISP0_DAT23	GPIO5_17	ecspi1 SS0	AUD4_RXD
109	DISP0_WR	EIM_D30	GPIO3_30	uart3 CTS	CSI0_D3
110	DISP0_VSYNCH	DI0_PIN3	GPIO4_19	AUD6_TXFS	
112	DISP0_CONTRAST	GPIO_1	GPIO1_1	KEY_ROW5	SSI_EXT2_CLK
114	DISP0_HSYNCH	DI0_PIN2	GPIO4_18	AUD6_TXD	
116	DISP0_DRDY	DI0_PIN15	GPIO4_17	AUD6_TXC	
117	DISP0_RD	EIM_D31	GPIO3_31	uart3 RTS	CSI0_D2

Legend

UART4	AUDMUX4	I2C1	ECSPI2	USBH2
UART5	AUDMUX5	I2C2	CSPI	SPDIF

Table 27. Expansion Port Pin-Mux Table (con)

J13 PIN	J13 Name	ALT(4)	ALT(5)	ALT(6)	ALT(7)
79	DISP0_POWER_EN	cspi SS2	AUD5_RXFS	ecspi2 SS2	uart1 DTR
80	DISP0_DAT9		DEBUG_EVENT_CHANNEL2	EMI_DEBUG14	usb2 VSTATUS0
81	DSIP0_SER_nCS	cspi SS0	EPITO	uart1 RTS	USBH2_PWR
82	DISP0_DAT10		DEBUG_EVENT_CHANNEL3	EMI_DEBUG15	usb2 VSTATUS1
84	DISP0_DAT11		DEBUG_EVENT_CHANNEL4	EMI_DEBUG16	usb2 VSTATUS2
85	DISP0_SER_MISO	cspi MISO		USBOTG_PWR	
86	DISP0_DAT12		DEBUG_EVENT_CHANNEL5	EMI_DEBUG17	usb2 VSTATUS3
87	DISP0_SER_MOSI	cspi MOSI	i2c1 SDA	EXT_TRIG	DIO_PIN13
88	DISP0_DAT13		DEBUG_EVT_CHN_LINES0	EMI_DEBUG18	usb2 VSTATUS4
89	DISP0_SER_SCLK	cspi SCLK	i2c1 SCL	USBOTG_OC	
90	DISP0_DAT14		DEBUG_EVT_CHN_LINES1	EMI_DEBUG19	usb2 VSTATUS5
91	DISP0_SER_RS	cspi SS0	DI0_PIN15	CSI1_VSYNCH	DI0_PIN14
92	DISP0_DAT15		DEBUG_EVT_CHN_LINES2	EMI_DEBUG20	usb2 VSTATUS6
94	DISP0_DAT16	SDMA_EXT_EVENT0	DEBUG_EVT_CHN_LINES3	EMI_DEBUG21	usb2 VSTATUS7
96	DISP0_DAT17	SDMA_EXT_EVENT1	DEBUG_EVT_CHN_LINES4		
98	DISP0_DAT18	AUD4_RXFS	DEBUG_EVT_CHN_LINES5	EMI_DEBUG23	WEIM_CS2
100	DISP0_DAT19	AUD4_RXC	DEBUG_EVT_CHN_LINES6	EMI_DEBUG24	WEIM_CS3
102	DISP0_DAT20		DEBUG_EVT_CHN_LINES7	EMI_DEBUG25	sata_phy TDI
104	DISP0_DAT21		DEBUG_BUS_DEVICE0	EMI_DEBUG26	sata_phy TDO
105	DISP0_nCS0	DI0_DO_CS	DI1_PIN2	CSI1_DATA_EN	DI1_PIN14
106	DISP0_DAT22		DEBUG_BUS_DEVICE1	EMI_DEBUG27	sata_phy TCK
107	DISP0_nCS1	cspi SS1		DIO_D1_CS	
108	DISP0_DAT23		DEBUG_BUS_DEVICE2	EMI_DEBUG28	sata_phy TMS
109	DISP0_WR	DI0_PIN11	DISP1_DAT21	USBH1_OC	USBH2_OC
110	DISP0_VSYNCH		DEBUG_CORE_STATE3	EMI_DEBUG3	usb1 IDDIG
112	DISP0_CONTRAST	pwm2 PWMO	wdog2 WDOG_B	esdhc1 CD	src TESTER_ACK
114	DISP0_HSYNCH		DEBUG_CORE_STATE2	EMI_DEBUG2	usb1 ENDSSN
116	DISP0_DRDY		DEBUG_CORE_STATE1	EMI_DEBUG1	usb1 BVALID
117	DISP0_RD	DI0_PIN12	DISP1_DAT20	USBH1_PWR	USBH2_PWR

Legend

UART4	AUDMUX4	I2C1	ECSPI2	USBH2
UART5	AUDMUX5	I2C2	CSPI	SPDIF

Table 27. Expansion Port Pin-Mux Table (con)

7. Board Accessories

7.1. HDMI Daughter Card

For developers wishing to output video via HDMI, there is an optional HDMI daughter card which can be purchased for use with the Quick Start board. The part number for the optional card is **MCIMXHDMICARD**, and this card can be purchased directly from Freescale.com. This HDMI card is connected to J13, and occupies the Expansion Port. The brass standoff on the HDMI card is threaded to accept a standard metric M3 machine screw. This will allow for a more sturdy connection if the developer plans to work with HDMI for a long period of time. **Figure 33** below shows the HDMI card that is available.

The schematics for the HDMI daughter card can be found on the **freescale.com/imxquickstart** website. The daughter card uses the Silicon Image SiI9022 HDMI Transmitter to reformat the display signals into the correct HDMI format and drive the video signals out the attached HDMI cable. Common Mode Chokes have been placed on the output of the Transmitter to meet FCC and CE emissions requirements.

Figure 33. Optional HDMI Daughter Card

In order to use the optional HDMI card with the Quick Start board, the environmental variables must be correctly set to support the card. This change needs to be done only one time, when the HDMI card is first used. The change requires the developer to use a host computer running a terminal window. When the power button is first pressed, the developer has 3 seconds to defeat the AUTOBOOT feature by pressing any key on the host computer. Once the boot cycle has been stopped, the developer now has access to change the boot environmental variables on the software image. At the terminal window, the developer should type the following two lines, pressing the enter key after each line:

setenv bootargs_base 'set bootargs console=ttymxc0,115200 ${hdmi}'
saveenv

Once the change is saved (**saveenv**), the Quick Start board can be turned off and then back on, or the developer can type boot on the terminal to restart the boot process. The Quick Start board is now correctly configured for HDMI operation. A note for developers: The HDMI parameters are contained in the U-BOOT code, and the recommended line to change the video output parameters only tells U-BOOT to substitute the stored parameters into the boot process. If the developer wishes to enter the exact string of variables into the U-BOOT code, the following line can be used instead of the first line above:

> ***setenv* bootargs_base 'set bootargs console=ttymxc0,115200 video=mxcdi0fb:RGB24,1024x768M-16@60'**

The above entry is all one line. After the line entry is made, the **saveenv** entry is also needed.

7.2. LCD Display Daughter Card

For developers wishing to output video to a touch screen LCD, there is an optional WVGA daughter card which can be purchased for use with the Quick Start board. The part number for the optional card is **MCIMX28LCD**, and this card can be purchased directly from Freescale.com. This LCD Display card is connected to J13, and occupies the Expansion Port. The brass standoff on the LCD Display card nearest the connector is threaded to accept a standard metric M3 machine screw. This will allow for a more sturdy connection if the developer plans to work with LCD display for a long period of time. In addition, the developer may also wish to screw into the remaining 3 brass stand-offs metric M3 machines screws that are approximately 25mm long. The screws can be adjust to provide support to the LCD card as it hangs over the Quick Start board. **Figure 34** below shows the LCD card that is available.

The schematics for the LCD Display daughter card can be found on the **freescale.com/imxquickstart** website. The daughter card uses the Seiko 43WVF1G-0 WVGA display, and provides all the power required for correct operations, regulated on the Display card. Power for the LCD Display, with the exception of the back light circuitry, comes from the MAIN_5V power source and does not go through the Dialog DA9053 PMIC.

Figure 34. MCIMX28LCD 4.3" WVGA Display Daughter Card

In order to use the optional LCD daughter card with the Quick Start board, the environmental variables must be correctly set to support the card. This change needs to be done only one time, when the LCD Display card is first used. The change requires the developer to use a host computer running a terminal window. When the power button is first pressed, the developer has 3 seconds to defeat the AUTOBOOT feature by pressing any key on the host computer. Once the boot cycle has been stopped, the developer now has access to change the boot environmental variables on the software image. At the terminal window, the developer should type the following two lines, pressing the enter key after each line:

setenv bootargs_base 'set bootargs console=ttymxc0,115200 ${lcd}'
saveenv

Once the change is saved (**saveenv**), the Quick Start board can be turned off and then back on, or the developer can type boot on the terminal to restart the boot process. The Quick Start board is now correctly configured for LCD operation. A note for developers: The LCD parameters are contained in the U-BOOT code, and the recommended line to change the video output parameters only tells U-BOOT to substitute the stored parameters into the boot process. If the developer wishes to enter the exact string of variables into the U-BOOT code, the following line can be used instead of the first line above:

> ***setenv*** **bootargs_base 'set bootargs console=ttymxc0,115200 video=mxcdi0fb:RGB24,SEIKO-WVGA**

The above entry is all one line. After the line entry is made, the **saveenv** entry is also needed.

7.3. LVDS Display Set (Coming Soon)

For developers wishing to output video to a LVDS panel, there is an optional LVDS panel which can be purchased for use with the Quick Start board. The part number for the optional card is **MCIMX-LVDS**, and may be purchased directly from Freescale.com. The LVDS Display kit comes with the panel, mounted in a frame, and a 15 inch cable that will connect directly to the LVDS connector (J9) on the Quick Start board. The LVDS panel can be used in parallel with the other video outputs (VGA, HDMI, LCD) giving the developer a second screen if desired. **Figure 35** below shows the LVDS Display available.

The LVDS display is the same panel used on the i.MX53 SMD Tablet. The LVDS module is manufactured by HannStar Display Corp and is part number HSD100PXN1-A00-C11. The two support legs can be inserted in the corresponding slots on the frame to allow the developer to chose any desired display orientation.

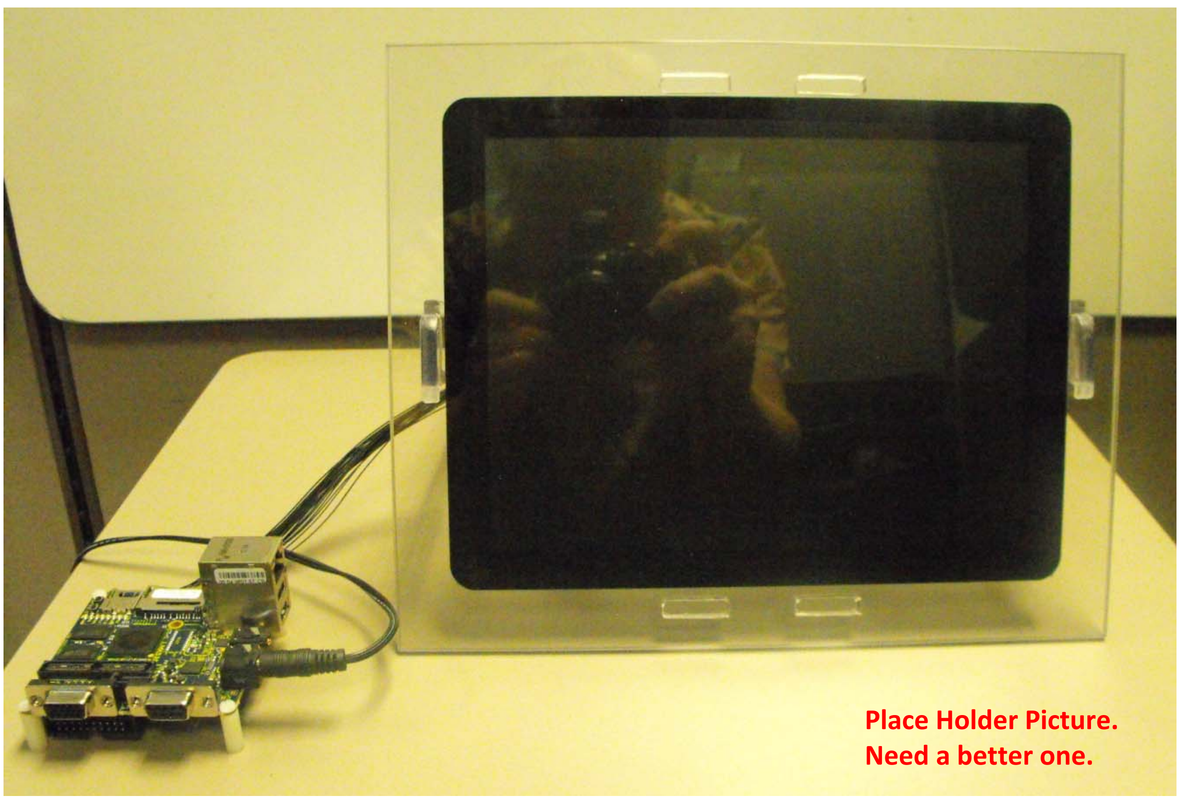


Figure 35. LVDS Display Kit

In order to use the optional LVDS Display Panel with the Quick Start board, the environmental variables must be correctly set to support the card. This change needs to be done only one time, when the LVDS Panel is first used. The change requires the developer to use a host computer running a terminal window. When the power button is first pressed, the developer has 3 seconds to defeat the AUTOBOOT feature by pressing any key on the host computer. Once the boot cycle has been stopped, the developer now has access to change the boot environmental variables on the software image. At the terminal window, the developer should type the following two lines, pressing the enter key after each line:

setenv bootargs_base 'set bootargs console=ttymxc0,115200 ${lvds}'
saveenv

Once the change is saved (**saveenv**), the Quick Start board can be turned off and then back on, or the developer can type boot on the terminal to restart the boot process. The Quick Start board is now correctly configured for outputting video to the LVDS panel. A note for developers: The LVDS sd

parameters are contained in the U-BOOT code, and the recommended line to change the video output parameters only tells U-BOOT to substitute the stored parameters into the boot process. If the developer wishes to enter the exact string of variables into the U-BOOT code, the following line can be used instead of the first line above:

setenv **bootargs_base 'set bootargs console=ttymxc0,115200 video=mxcdi0fb:RGB666,XGA ldb'**

The above entry is all one line. After the line entry is made, the **saveenv** entry is also needed.

8. Mechanical PCB Information

The overall dimensions of the i.MX53 Quick Start PCB are shown in **Figure 36. Quick Start Board Dimensions.**

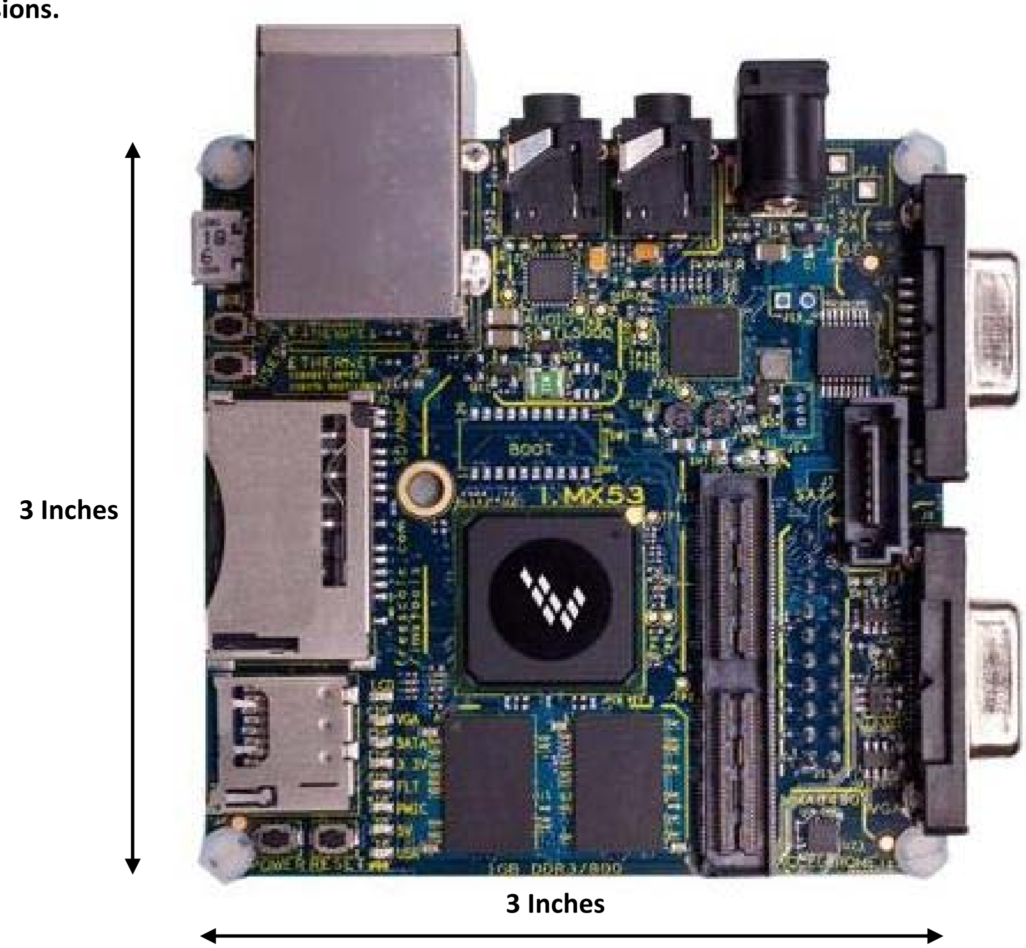


Figure 36. Quick Start Board Dimensions

The Printed Circuit Board was made using standard 8-layer technology. The material used was FR-4 Hi Temp. The board stack up is as follows:

- Top Layer
- Ground-1 Layer
- Signal-1 Layer
- Power-1 Layer
- Power-2 Layer
- Signal-2 Layer
- Ground-2 Layer
- Bottom Layer

The stack up information provided by the PCB Fabrication Facility is as shown in **Table 28. Board Stack up information**. Widths and thickness are shown in mils. Impedances are shown in Ohms. The material used in calculating this stack up was 370HR.

				Single End Trace				Differential Pair Traces					
Layer	Thickness	Description	Copper Oz.	Trace Width	Calculated Impedance	Target Impedance	Reference Plane	Trace Width	Space Width	Diff Pairs (Pitch)	Calculated Impedance	Target Impedance	Reference Plane
	0.70	Mask											
	1.20	Plating											
1	0.60	Signal	0.50	8.50	50.32	50	2	4.75	5.25	10	100.82	100	2
				3.25	73.94	75	2	6.25	4.75	11	89.51	90	2
	5.00	Prepreg											
2	0.60	GND	0.50										
	4.00	Core											
3	0.44	Signal	0.37					3.75	6.25	10	89.69	90	2,4
				3.25	49.60	50	2,4	3.00	6.00	9	99.88	100	2,4
	3.00	Prepreg											
4	0.60	Power	0.50										
	30.00	Core											
5	0.60	Power	0.50										
	3.00	Prepreg											
6	0.44	Signal	0.37					3.75	6.25	10	89.69	90	5,7
				3.25	49.60	50	5,7	3.00	6.00	9	99.88	100	5,7
	4.00	Core											
7	0.60	GND	0.50										
	5.00	Prepreg											
8	0.60	Signal	0.50	8.50	50.32	50	7	4.75	5.25	10	100.82	100	7
				3.25	73.94	75	7	6.25	4.75	11	89.51	90	7
	1.20	Plating											
	0.70	Mask											

62.28 = Total Thickness

Table 28. Board Stack up information

9. Board Verification

The On Board Diagnostic Scan (OBDS) tool used by the factory acceptance test tools is included on the MicroSD card image that is shipped with the i.MX53 Quick Start board. If the original image is corrupted or over-written by the software developer, a fresh image can be downloaded from the freescale.com/imxquickstart web site.

To access the OBDS tool, a serial cable and a host PC running a terminal program (Tera Term, HyperTerminal, etc) will be required. After connecting the host terminal to the Quick Start board, press the power button on the board. Before U-BOOT completes the Autoboot countdown (3 seconds) press any key on the host computer. This will stop the Ubuntu Kernel from continuing the boot process and allow the developer to access the code on the MicroSD card. On the host computer terminal window, type the following line:

Ext2load mmc 0:1 0x70800000 /unit_tests/obds.bin

After the prompt returns:

Loading file "/unit_tests/obds.bin" from mmc device 0:1 (xxa1)
XXXXXX bytes read

Type:

go 70800000

This will begin the OBDS diagnostic tool. The tool has 16 tests that it can perform. They are as follows:

MAC Address confirmation
Debug UART Test
DDR3 Test
USBH1 Enumeration Test (Upper Host Port)
Secure Real Time Clock Test
Dialog PMIC ID Test
SATA Test
I2C Device Test
GPIO Test
Ethernet Test
I2S Audio Test
LCD Daughter Card Test
LVDS Display Test
VGA Video Test
HDMI Daughter Card Test
MMC/SD Card Test

The first question that the user will be asked by the OBDS test is if the user would like to AUTORUN the OBDS test. A yes answer (y or Y) will keep the OBDS test from prompting the user for any test that does not require direct user action. Any other key press will cause the OBDS test to prompt for all tests. A yes answer to this question is primarily for mass testing of Quick Start boards. Single users of this test can run this test with prompts without significant loss of time.

The tests are straight forward, and if a supporting piece of equipment is required, the test will prompt the user for it. In order to complete all the tests, you would need to have the following equipment:

USB HOST1 Test – Attached USB device required
SATA Test – Attached SATA device required.
Ethernet Test – The Ethernet loop back test plug as described below is required.
Head Phone Test – A set of earphones or speakers are required.
LCD Test – The optional LCD Display card is required
LVDS Test – The optional LVDS display kit is required
VGA Video Test – Connection to a VGA monitor is required
HDMI Test – The optional HDMI card is required
MMC/SD Card slot – A full size SD card is required in card slot J5.

If the developer does not have one or more of the above items, the test can easily be skipped when asked if the user would like to perform the test. A complete cycle of tests covers 16 different aspects of the board. When the last test is run, the OBDS tool will print out a summary of the test results. A failure in any one particular area would indicate that there is a hardware fault with the Quick Start board that should be addressed. If all tests pass, but the developer code does not function correctly, the problem is most likely with the code. A more detailed description of the tests is as follows:

1) MAC Address confirmation. The i.MX53 Processor reads the MAC Address programmed into the Processor eFUSEs and prints them out on the terminal window. The resulting print out should match the MAC address label on the Quick Start board. If the two numbers match, the test has passed.

2) UART Test. When the test is running, the test expects different characters to be input from the keyboard of the host computer. After a character is input, the i.MX53 Processor receives the input, transmits to the terminal window the received character, and then asks the user to confirm that the character is correct by pressing the ‘x’ key. The test is exited by typing an ‘x’ as an input character.

3) DDR Test. The test writes predetermined data onto the DDR3 memory, reads those memory blocks back out, and then compares the two values for errors. If the values match, the test passes.

4) USBH1 Enumeration Test. Any USB device is plugged into the upper HOST connector (the lower port is connected to the USBOTG module). After confirming that a USB device is plugged in, the I.MX53 will read the device enumeration data and print it out on the terminal window. If the Processor cannot read enumeration information, the test fails.

5) Secure Real Time Clock Test. The i.MX53 Processor checks to make sure the RTC clock is counting. If the clock is counting, the test passes.

6) PMIC Device ID Test. The i.MX53 Processor attempts to communicate with the PMIC using the attached I2C channel. If the two devices communicate, the test passes.

7) SATA Test. The processor attempts to communicate with an attached SATA device. If the processor detects the internal 50 MHz clock signal and communications coming from an attached SATA device, the test passes.

8) I2C Test. The processor attempts to communicate with one of the I2C devices on the Quick Start board. If communications complete correctly, the test passes.

9) GPIO Test. The Processor drives the USER LED light controlled by PATA_DA_1 (pin L3) alternately high and low. If the user light appears to blink, the test passes.

10) FEC Ethernet Test. The Processor drives a data packet out of the Ethernet Jack, into the loop back cable, and then receives the test packet back. If the received packet matches the sent packet, the test passes.

11) I2S Audio Test. The Processor gives a tone to the Audio CODEC. If the tone can be heard through both speakers of the attached headphones, the test passes. After the user requests the test to be run, the user is prompted to insert a headphone set into jack (J18). When the headphones are connected, the user presses the ‘y’ key to confirm the headphones are attached. A sound will play. The test will then prompt you to replay the tone if needed. If the tone is no longer needed, the test will then prompt for an answer as to whether the tone was heard or not.

12) LCD Display test. If this test is selected, an image will be displayed on the attached LCD card. Once the image is displayed, the test will prompt the user to confirm whether or not the image is seen. If the image is seen, the test passes.

13) LVDS Display test. If this test is selected, an image will be displayed on the attached LVDS Panel. Once the image is displayed, the test will prompt the user to confirm whether or not the image is seen. If the image is seen, the test passes.

14) VGA Video test. If this test is selected, an image will be displayed on the attached video monitor. Once the image is displayed, the test will prompt the user to confirm whether or not the image is seen. If the image is seen, the test passes.

15) HDMI test. If this test is selected, an image will be displayed on the attached video monitor. Once the image is displayed, the test will prompt the user to confirm whether or not the image is seen. If the image is seen, the test passes.

16) MMC/SD Test. If the user selects this test to be run, the user will be prompted to insert an MMC/SD card into the full size SD Card slot (J5). When the user confirms that the card is present, the processor will attempt to read the current SD card settings and manufacturing information on the SD card. If the Processor can read this information, the test passes.

The only special equipment required to complete the bank of OBDS tests is the Ethernet Loop back cable. This can be purchased on line (single plug Ethernet Lookback Cable) or it can be created by the developer by cutting one end of an unneeded Ethernet cable and connecting the wire from pin 1 to the wire from pin3, and connecting the wire from pin 2 to the wire from pin 6. All other wires remain unconnected. The four wires used will be solid Green, solid Orange, Green/White stripe, and Orange/White stripe. The solid colors are connected together and the striped colors are connected together. While the solid colors will always be connected to pins 2 and 6, the specific pin a color is attached to will depend on which plug is used. The same is true for the striped wires connected to pins 1 and 3. A diagram of this cable is shown in **Figure 37** below.

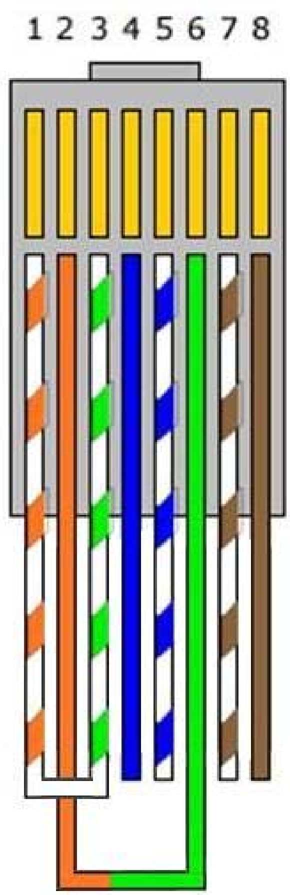


Figure 37. Ethernet Loopback Cable

10. Troubleshooting

The i.MX53 Quick Start board does not have specific troubleshooting features designed into the board. The board has proven robust during the initial test and development periods and should provide years of good service to the developer if treated with due caution. The test pads that are included on the schematic and on the board were not specifically designed for testing, but were placed on the board for developers who wanted to make wire connections to specific pins that might not be available without the test pads. One basic troubleshooting technique that is available to developers is to measure the voltage rails outputs on all the rails coming from the PMIC. The subsection on PMIC voltage rails presents a diagram with points the developer can use to make measurements. A second basic troubleshooting technique would be to measure clock frequencies to ensure the clock are running correctly. The position of the crystals and oscillators are in the design section under the i.MX53 Applications Processor.

Aside from actual hardware difficulties, the **Table 29** presents some other issues that may help the developer solve technical difficulties:

Symptoms	Possible Problem	Action
No 5V power to the Quick Start board, no Green LED light.	Attached power supply is not within the 4.5V – 5.5V window.	Use the power supply that came with the Quick Start board kit.
	Fuse F1 has blown. Use multimeter to check for open.	Replace the fuse with a new 3A, 0603 surface mount fuse.
Intermittent signal on Debug UART, or color issues on VGA video output.	Cold solder connection on connector pins have broken loose after several cable insertions.	Examine the pins on the affected connector (J8 or J16). If a pin can wiggle back and forth, a solder iron should be used to reconnect the pin. Note: There is epoxy over the pins to increase pin strength. The epoxy may need to be removed first.
No Debug information on the Host Computer Terminal Window.	Incorrect Serial Cable used (eg Null modem cable)	Verify that serial cable is correct.
Lower USB Host Port is not working correctly.	Quick Start board is attached to a Host device through the Micro-B Connector.	Remove cable from Micro-B connector if Lower USB Host Port operations is desired.

Table 29. Problem Resolution Table

10.1. PMIC Voltage Rail Test Points

To assist the developer in determining whether the PMIC voltage rails are outputting the correct voltage levels, **Figures 38 and 39** show the output capacitor on each regulator output with the ground pin colored yellow and the power pin colored red. **Tables 30 and 31** show the expected voltage value for each capacitor.

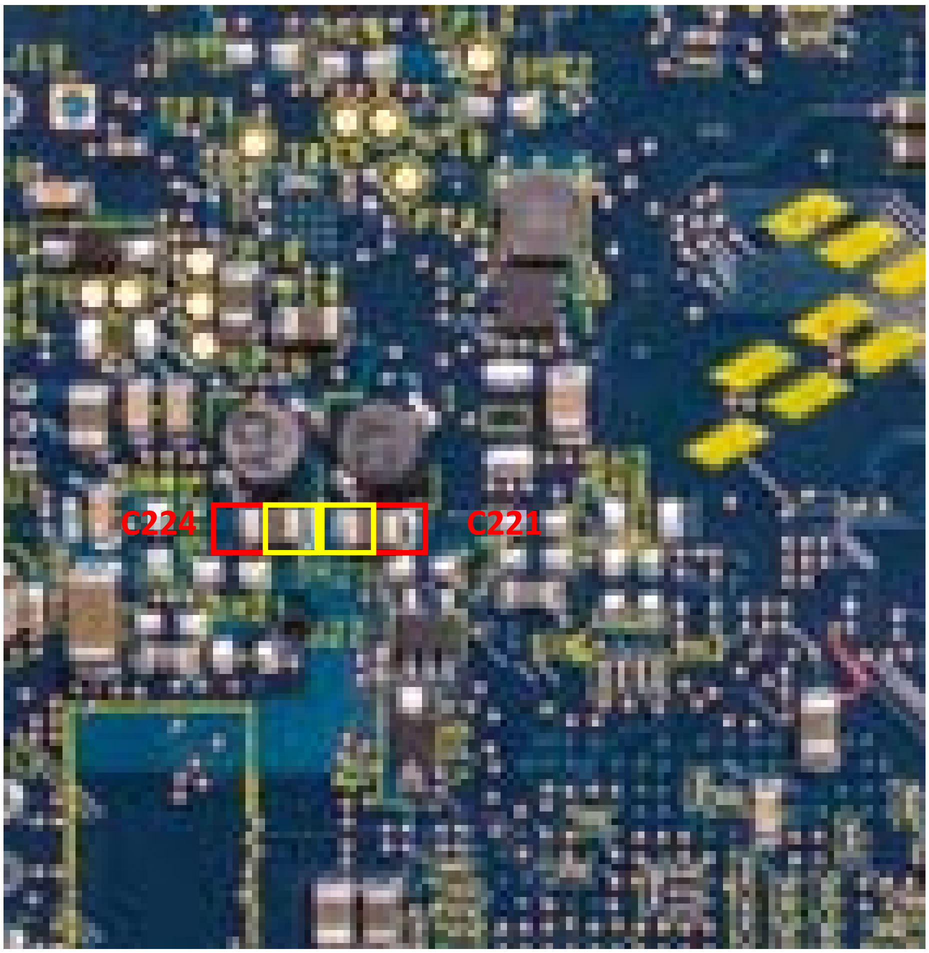


Figure 38. Regulator Output Capacitor Positions Bottom

Capacitor	Regulator	Value
C224	VBUCKMEM	1.5V
C221	VBUCKPERI	2.5V

Table 30. Output Capacitors and Values BOTTOM

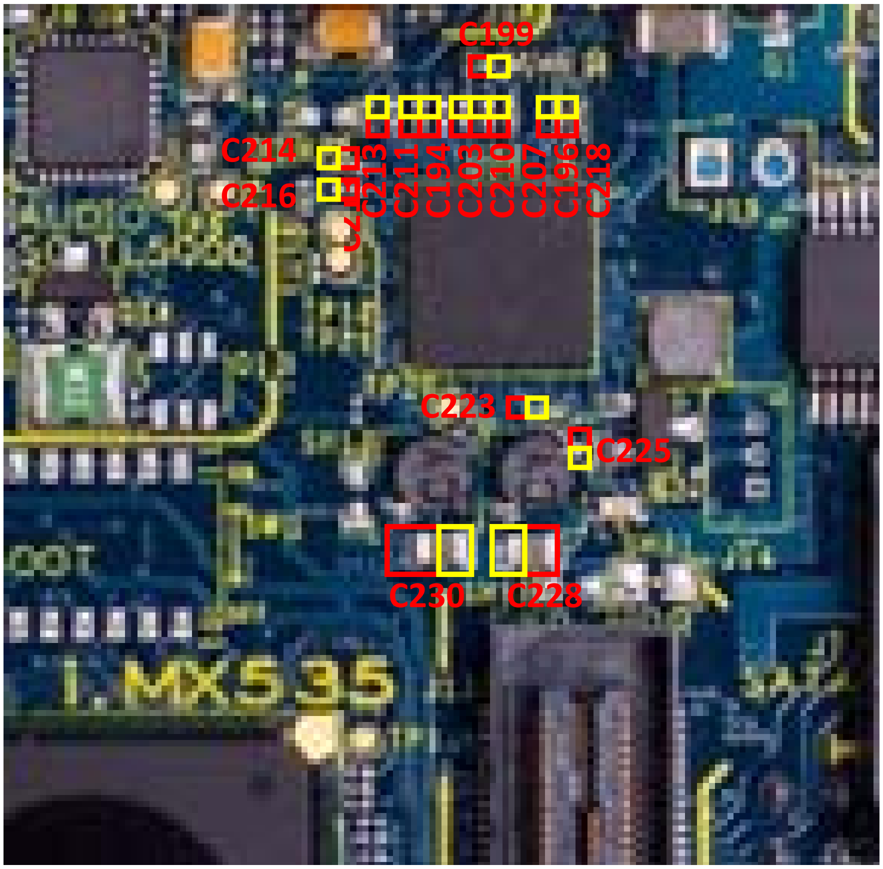


Figure 39. Regulator Output Capacitor Positions Top

Capacitor	Regulator	Value
C199	VDD_DIG_PLL	1.3V
C214	VLDO9	1.5V
C216	VLDO10	1.3V
C213	VLDO8	1.8V
C211	VLDO7	2.75V
C194	VLDO3	3.3V
C203	VLDO4	2.775V
C210	VLDO6	1.3V
C207	VLDO5	1.3V
C196	VLDO1	1.3V
C218	VDDCORE	2.5V
C223	VBUCKPERI	2.5V
C225	VBUCKMEM	1.5V
C230	VBUCKPRO	1.3V
C228	VBUCKCORE	1.1V

Table 31. Output Capacitors and Values TOP

11. Known Issues

At the initial launching of the Quick Start board, the following issues are known to exist:

1) SATA boot will not function with the sample grade i.MX53 ICs (rev 2.0 prototype silicon). The problem is an IC problem related to using the internal SATA clock. Since the external clock components have been removed from the Quick Start board, the SATA boot feature is not usable. The work around is to initialize SATA with minimum code on a microSD card, then pass the boot process to the SATA drive early. This problem is being fixed with the rev 2.1 production silicon i.MX53 Processor.

2) There is a defect in the Video Processing Unit (VPU) of the i.MX53 Processor (rev 2.0). The defect causes the DDR3 SDRAM to miscalculate some blocks in video processing resulting in defects observable on the video output in high processing modes (1080p). This defect is being corrected on the rev 2.1 production silicon i.MX53 processor. For initial production Quick Start boards, the VCC voltage is being raised to 1.35V to allow the VPU to process without errors. On rev 2.1 silicon, VCC will be returned to 1.3V (by removing the software patch). This is not a recommended solution for customer use, but is sufficient for development work on the Quick Start board.

3) The Dialog DA9053 PMIC rev AA silicon has a 1.2A limitation of the VDDOUT supply rail. This is the voltage supply for all the PMIC regulators. The i.MX53 demonstration software is drawing close to the 1.2A limit, and at times, voltage dips occur on the VDDOUT supply rail as the Quick Start board tries to draw more power than the PMIC can supply. This has led to some abrupt shutdowns in the testing cycle, as VDDOUT dips down below the allowed threshold. When it becomes available, the DA9053 rev BB silicon will increase the current limit to 1.8A. For the initial Quick Start boards, a 220 uF capacitor has been placed across JP19 pin2 and JP2 to smooth out sudden momentary drops in voltage. In addition, a MicroElectronics STTH2L06 has been soldered from the 5V_Main (Anode) to JP19 pin2 (Cathode) to provide a direct current path outside the normal PMIC switcher. For this reason, the switcher L13 inductor has been removed from these boards, preventing their use with an attached battery. This fix is only being used for the preliminary rev AA silicon. All boards affected with this modification (in addition to having an obvious capacitor and diode) are labeled “700-26565 Rev D”

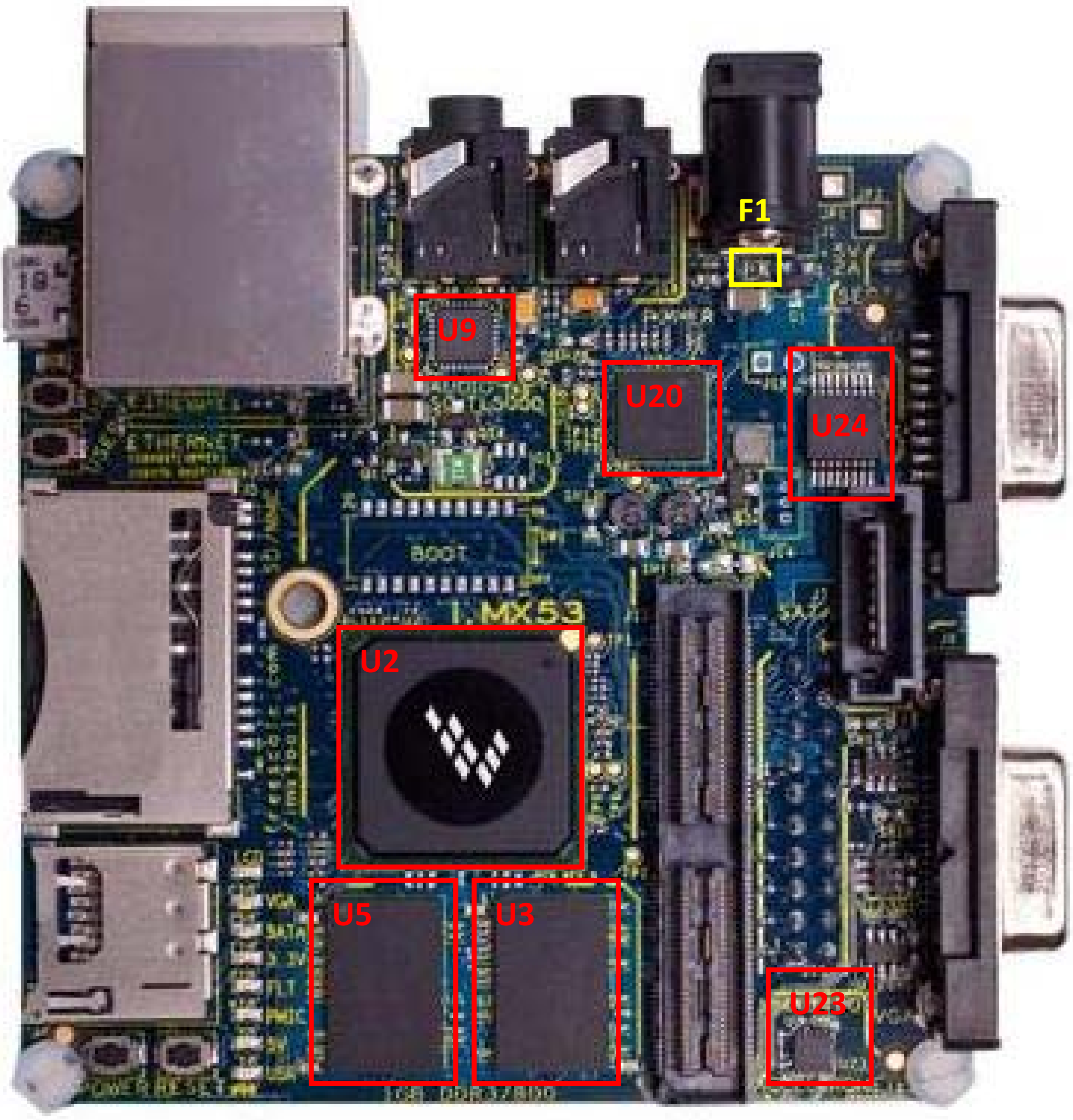
12. PCB Component Locations

To aid the developer in locating major components on the Quick Start board, their locations have been highlighted and annotated in the same way that the connectors have been highlighted. These pictures are presented as the following Figures:

Figure 40. Major Component Highlights Top
Figure 41. Major Component Highlights Bottom

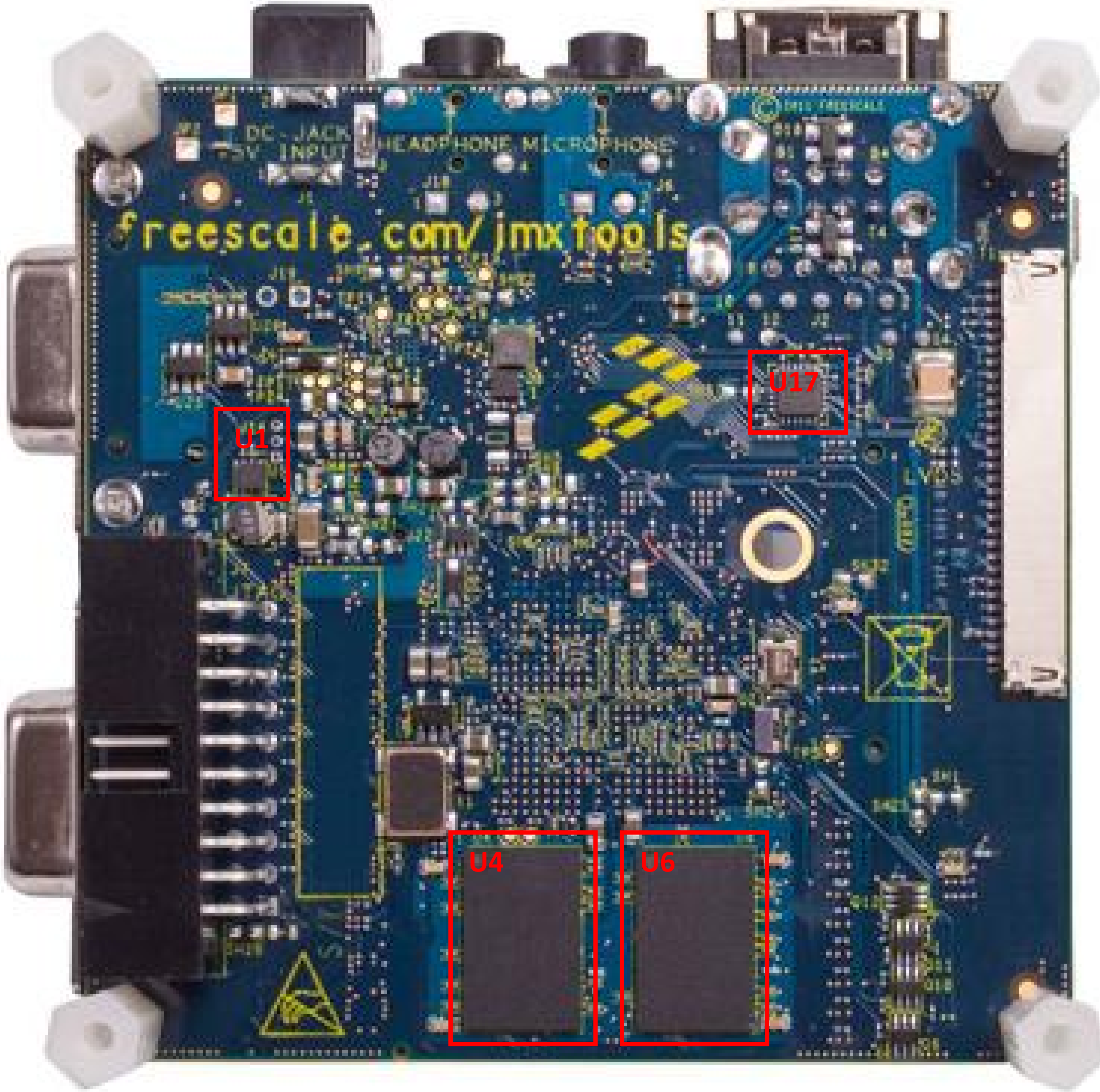
The Assembly Drawings for all component locations are shown in a picture format for easy reference when using this document. The actual Gerber artwork for the assembly drawings is available from the i.MX53 Quick Start web site. The Assembly drawings are shown in the following figures:

Figure 42. Assembly Drawing Top
Figure 43. Assembly Drawing Bottom



U2	i.MX53 Application Processor	U20	Dialog DA9053 PMIC
U3	DDR3 SDRAM	U23	MMA8450QT Accelerometer
U5	DDR3 SDRAM	U24	RS232 UART Transceiver
U9	SGTL5000 Audio CODEC	F1	3A Fuse

Figure 40. Major Component Highlights Top



U1	3.2V Voltage Regulator
U4	DDR3 SDRAM
U6	DDR3 SDRAM
U17	Ethernet PHY

Figure 41. Major Component Highlights Bottom

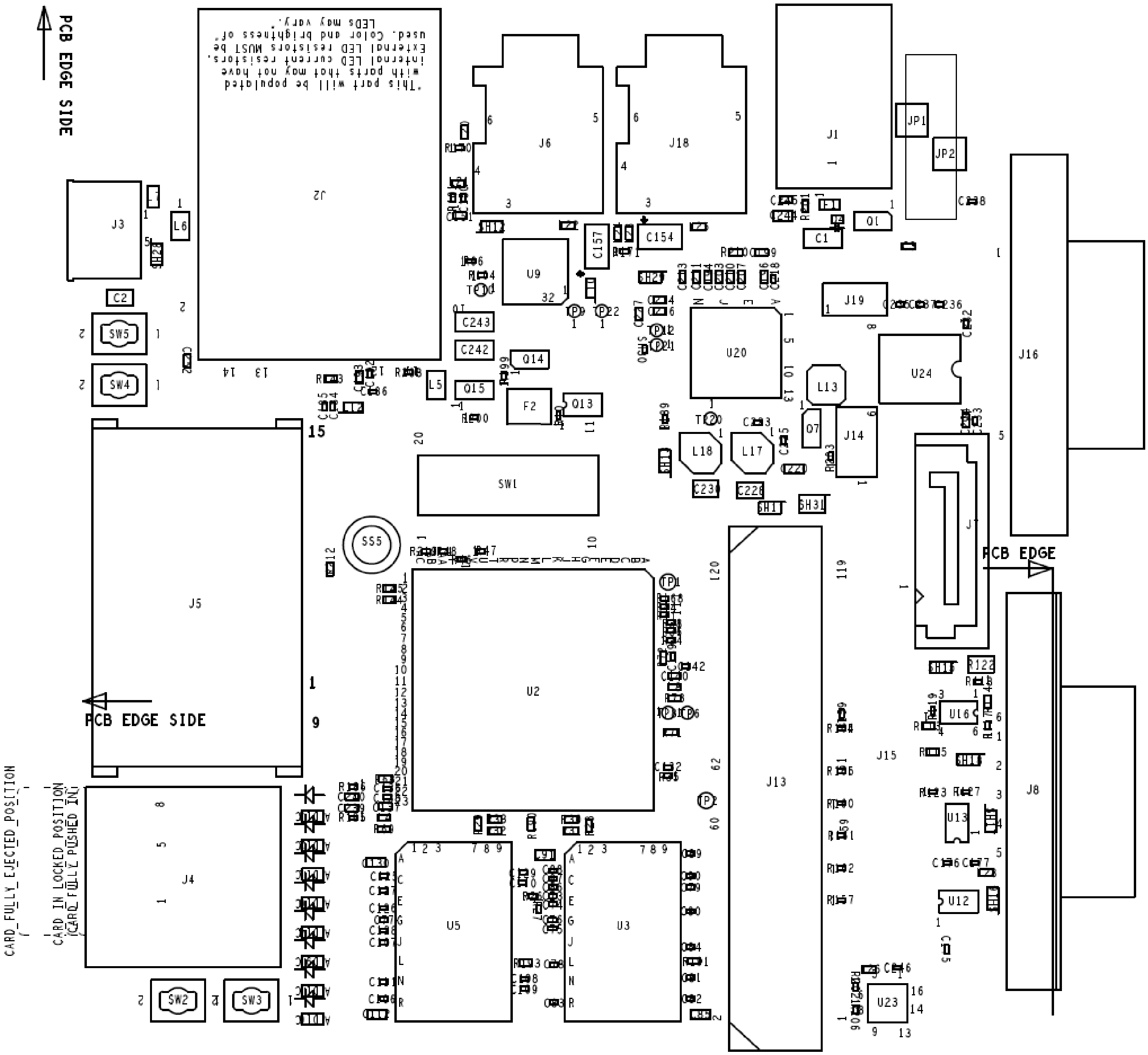


Figure 42. Assembly Drawing Top

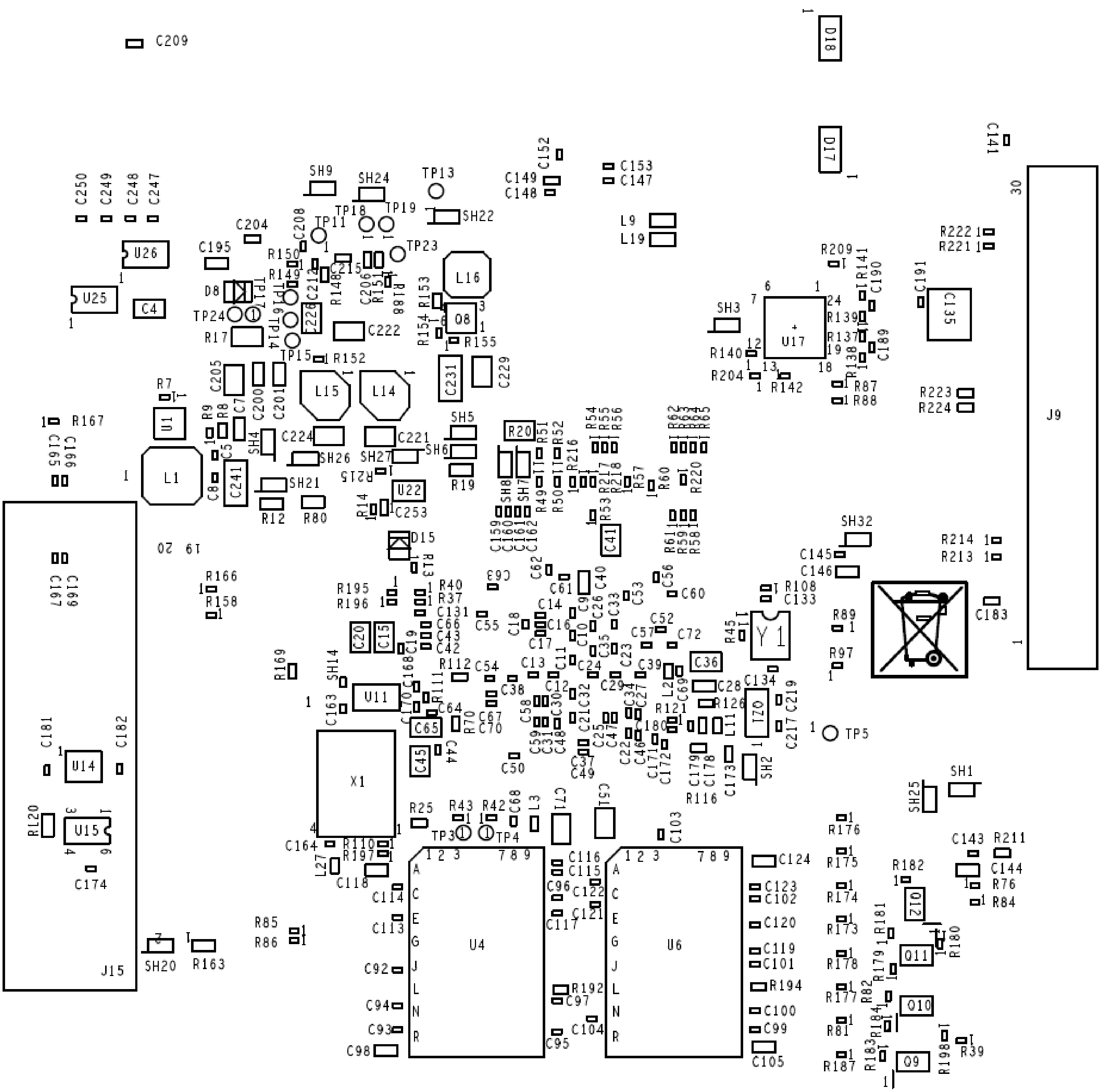
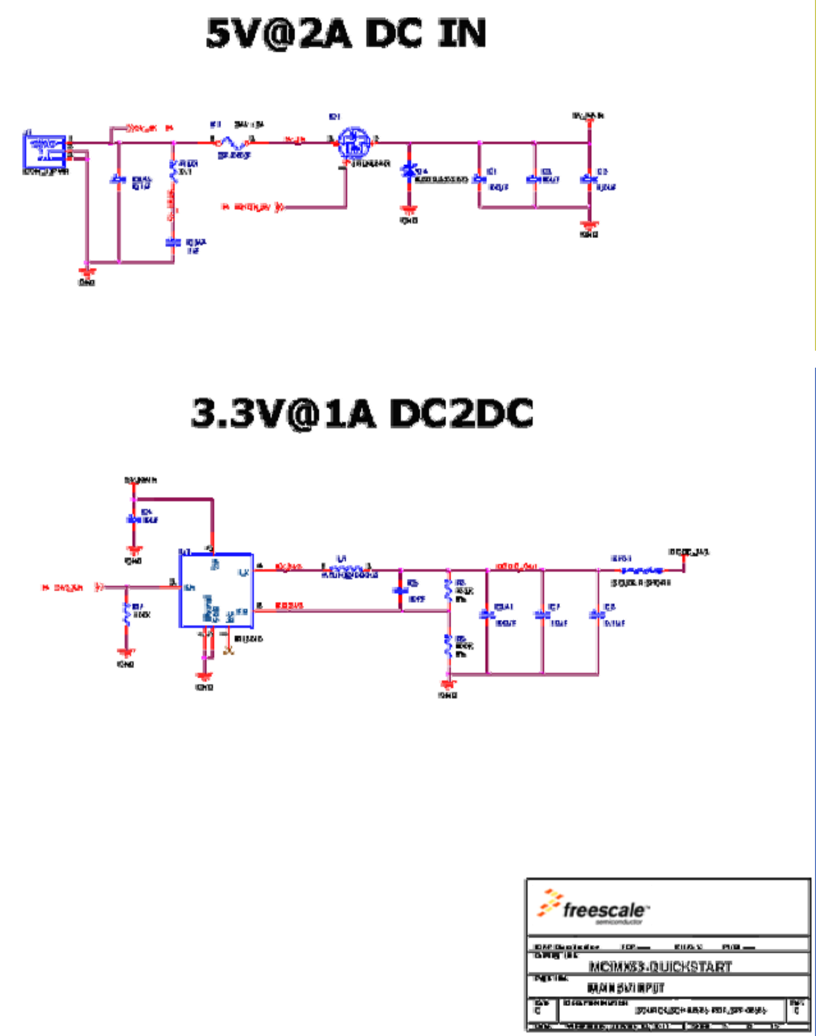


Figure 43. Assembly Drawing Bottom

13. Schematics

The main portion of the schematics consist of 13 pages. These pages are shown here for reference purposes. They can be found in the original Cadence Allegro-OrCAD format (.DSN file) and in a PDF format on the i.MX53 Quick Start web site. The following figures show the schematic pages:



Power Table				
DOMAIN	VOLTAGE	MODULE	SUBSYSTEM	BOOT TIMING
MAIN_5V	5V		EMIC DCDC_3V3 DISPLAY LEDS USB_HOST_PWR VGA_OUTPUT	ALWAYS ON
VLDO1	1V3	NVCC_SRTC		ALWAYS ON
VBUCKPRO	1V3	VCC		19 mSEC
VBUCKPERI	[illegible]	VDD_REG NVCC_XTAL		23 mSEC
VLDO6	1V3	VDDAL		23 mSEC
VLDO8	1V8	NVCC_RESET NVCC_JTAG NVCC_CKIH NVCC_NANDF NVCC_CSI VDD_ANA_PLL	BOOT_SEL	23 mSEC
VLDO10	1V3	VDDA		23 mSEC
VBUCKCORE	1V1	VDDGP		27 mSEC
VBUCKMEM	1V5	NVCC_EMI_DRAM	DDR3	31 mSEC
VBUCKPERI /SW	2V5		LVDS_2V5 SATA_PHY_2V5 USB_2V5	31 mSEC
VLDO2	1V3	VDD_DIG_PLL		31 mSEC
VLDO5	1V3		SATA_1V3	31 mSEC
VLDO4	2V775	NVCC_LCD1&2 VLCMI		35 mSEC
VLDO7	2V75	TVDAC	VGA	35 mSEC
VLDO3	3V3	NVCC_EIM_MAIN NVCC_EIM_SEC NVCC_SD1&2 NVCC_PATA NVCC_FEC NVCC_GPIO NVCC_KEYPAD	SD1 I2C1&2 BOOT_SEL	64 mSEC
VLDO9	1V5		EXT HDR	64 mSEC
DCDC_3V2	3V2	VDD_FUSE	FEC SD3 LCD_PORT USB_3V3 VGA_IO AUDIO	64 mSEC

Figure 44. DC 5V INPUT

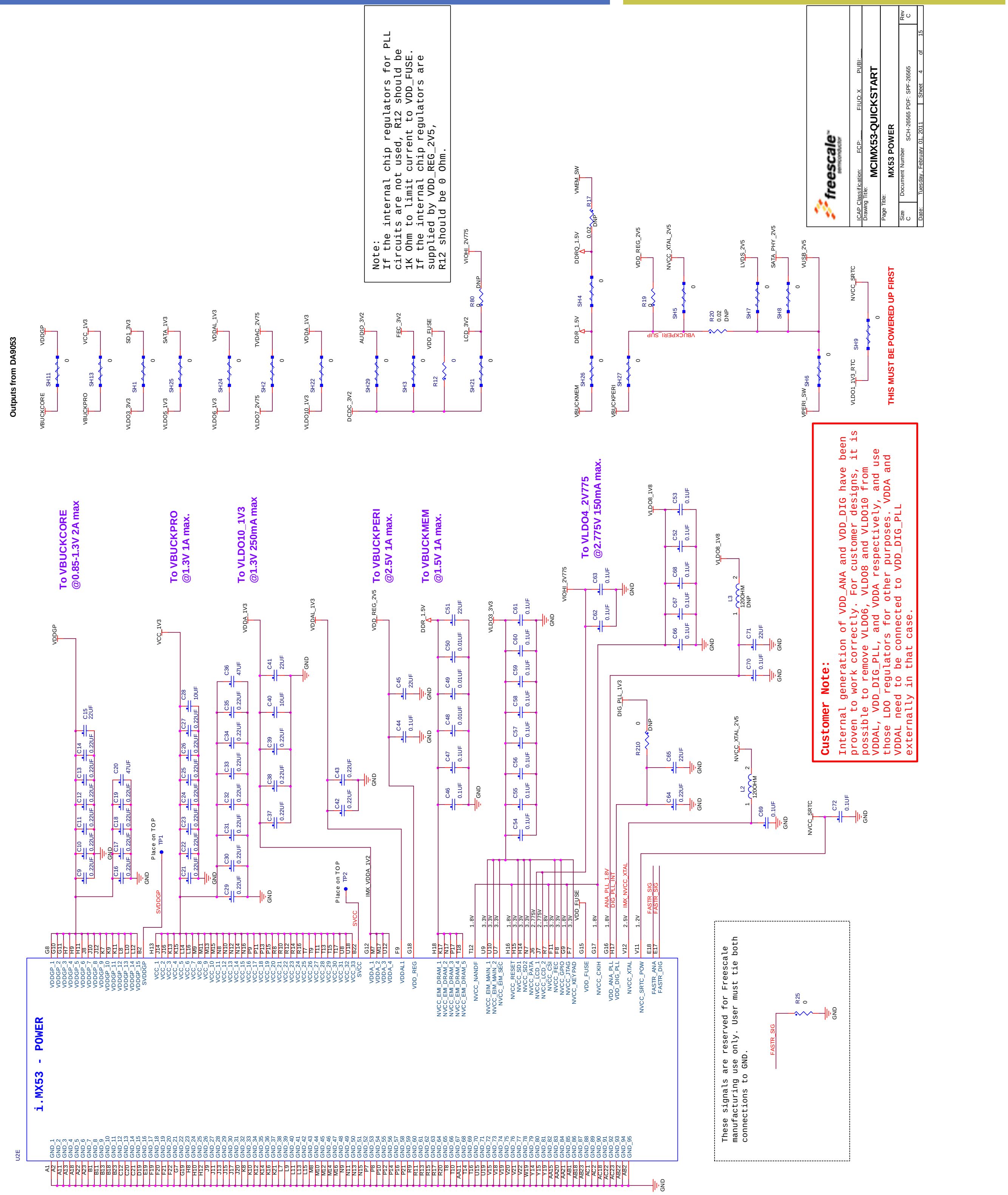


Figure 45. MX53 POWER

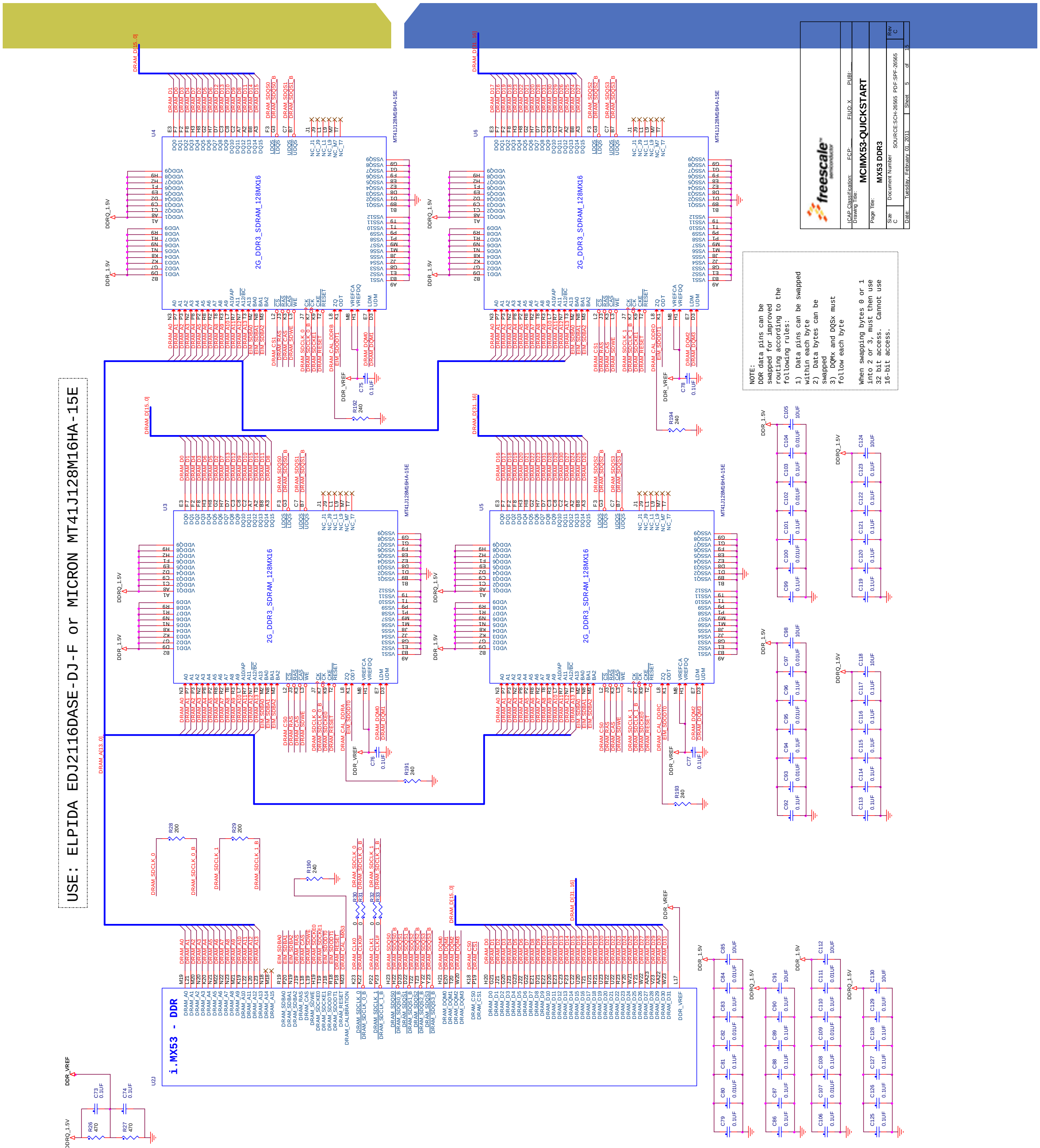


Figure 46. MX53 DDR3 MEMORY

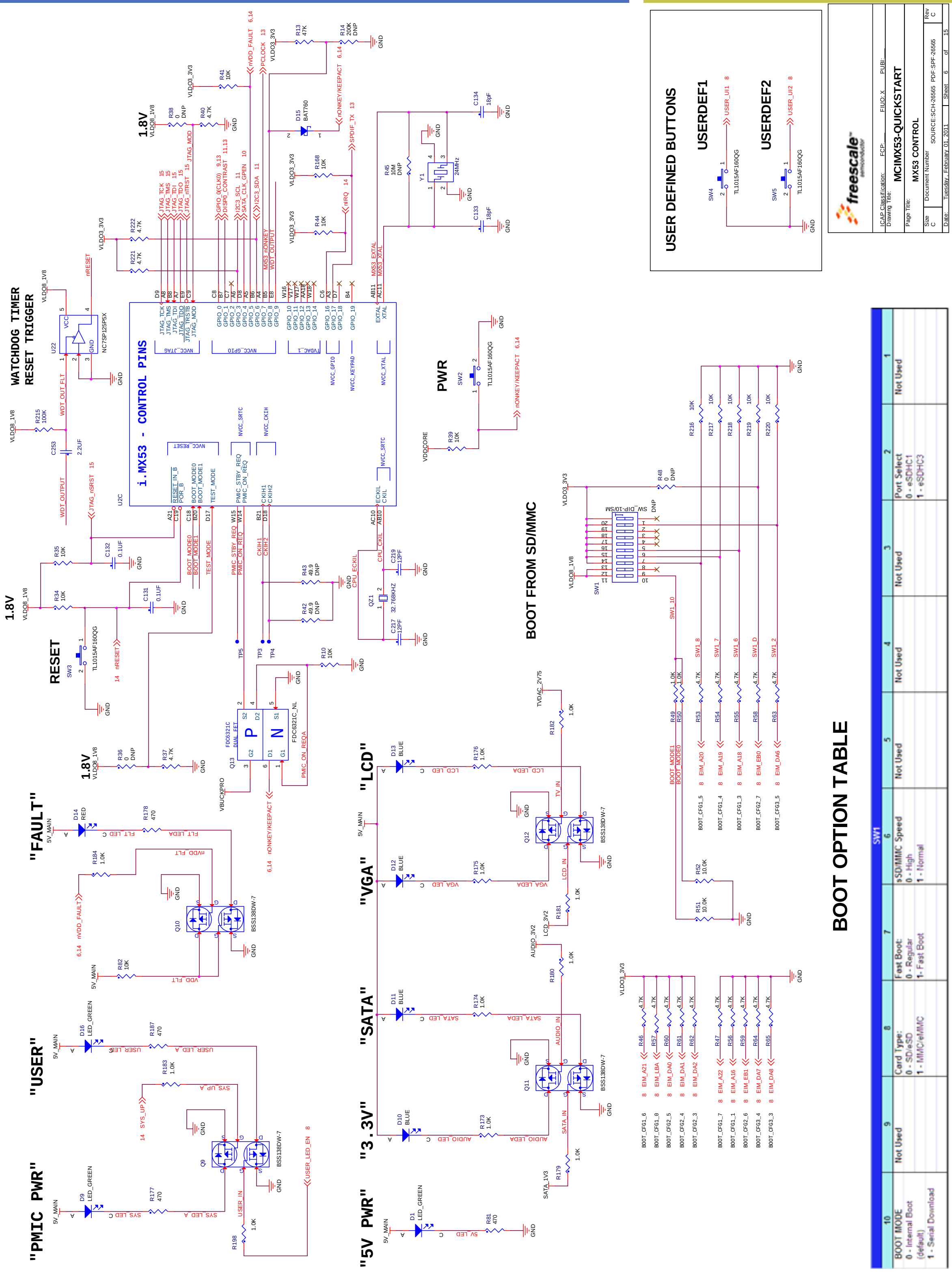


Figure 47. MX53 CONTROL

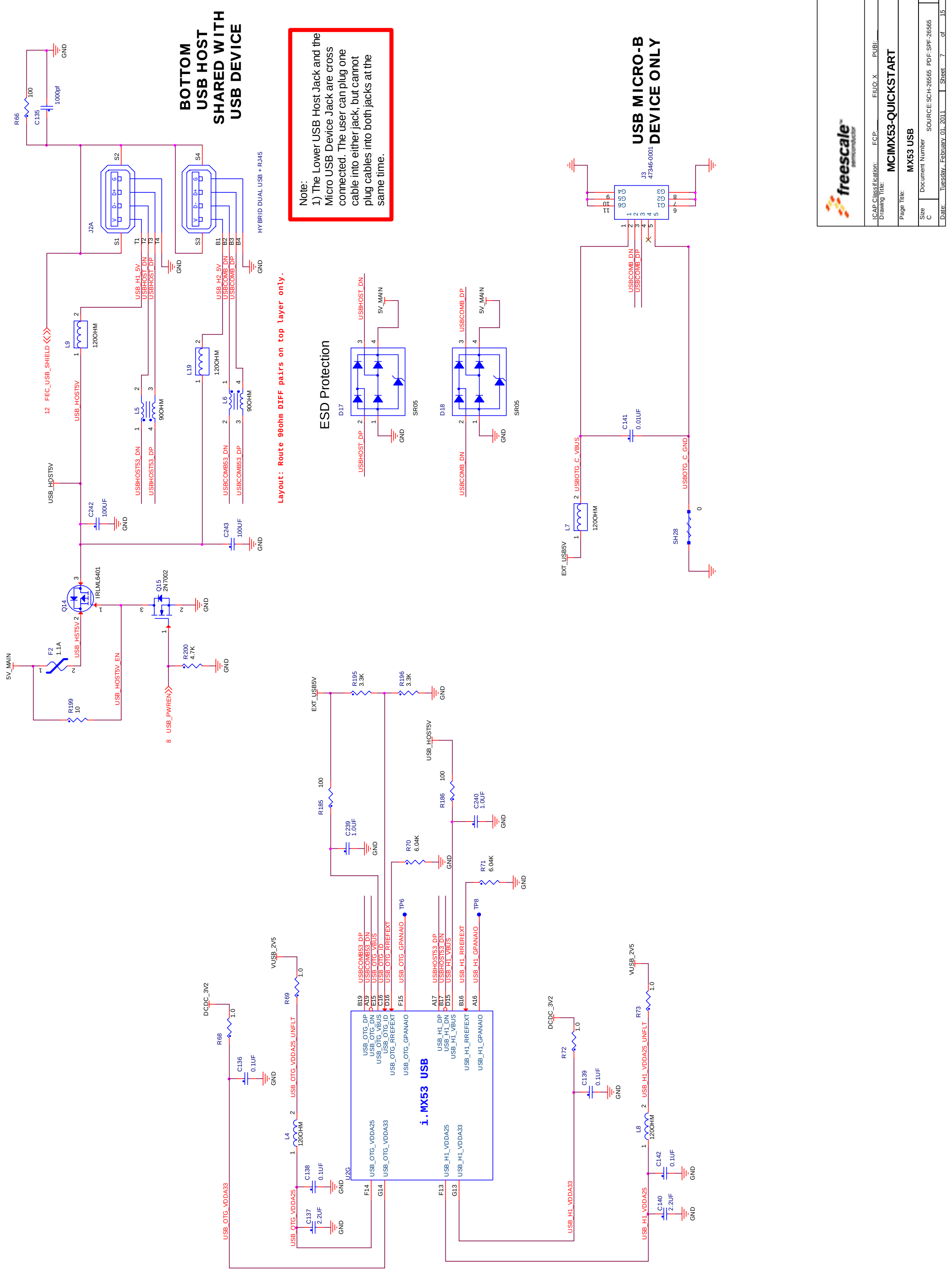


Figure 48. MX53 USB

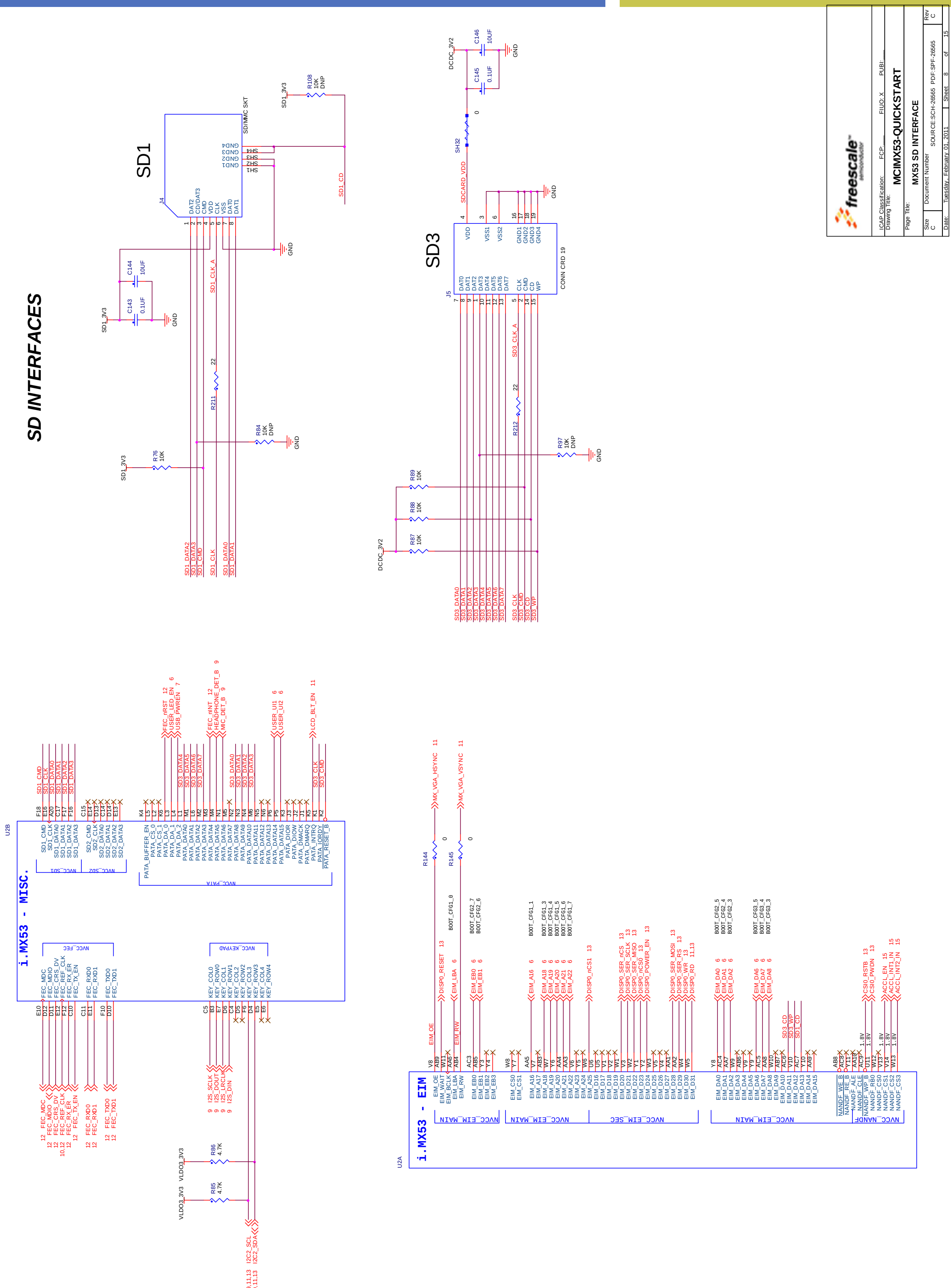


Figure 49. MX53 SD INTERFACE

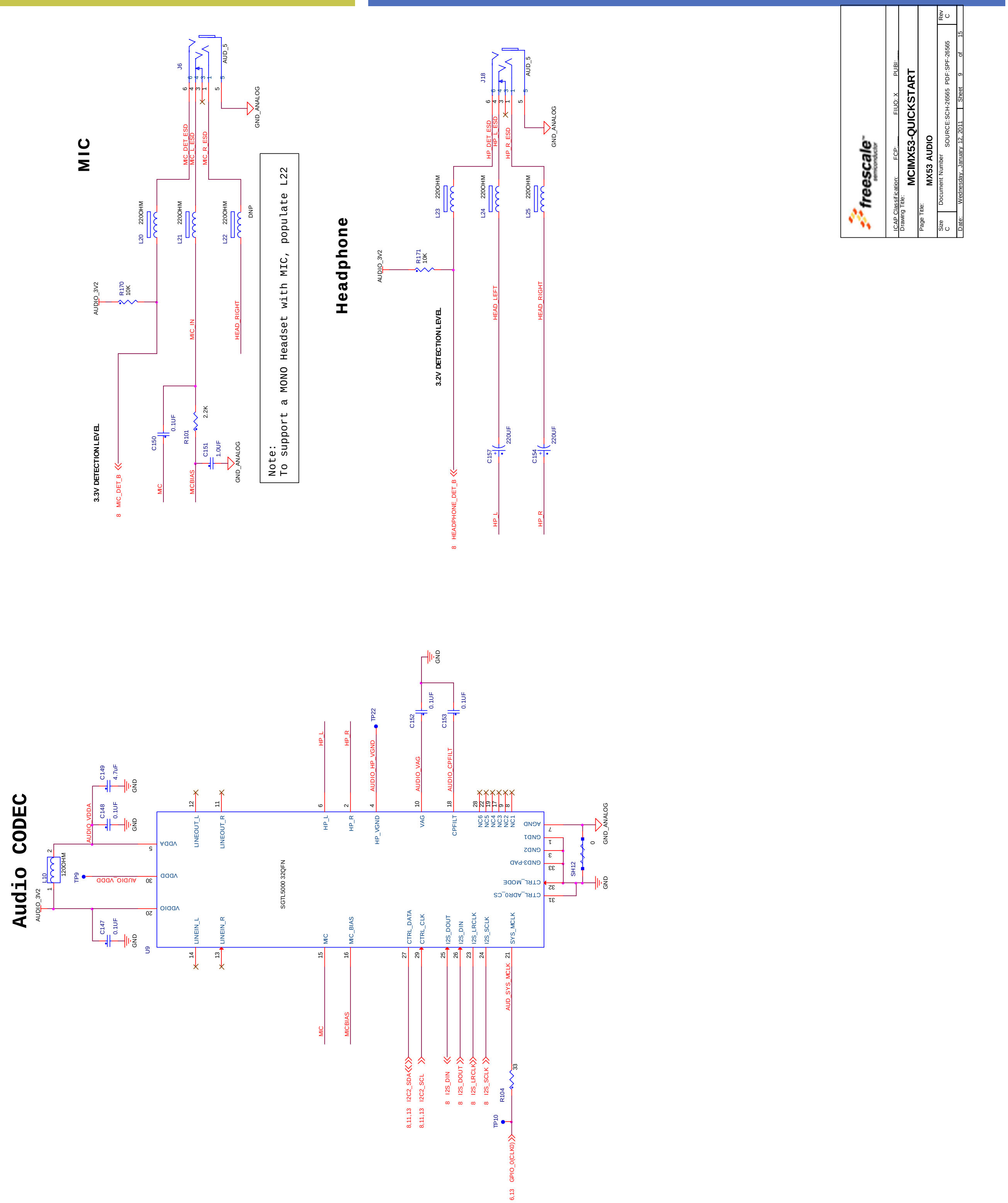


Figure 50. MX53 AUDIO

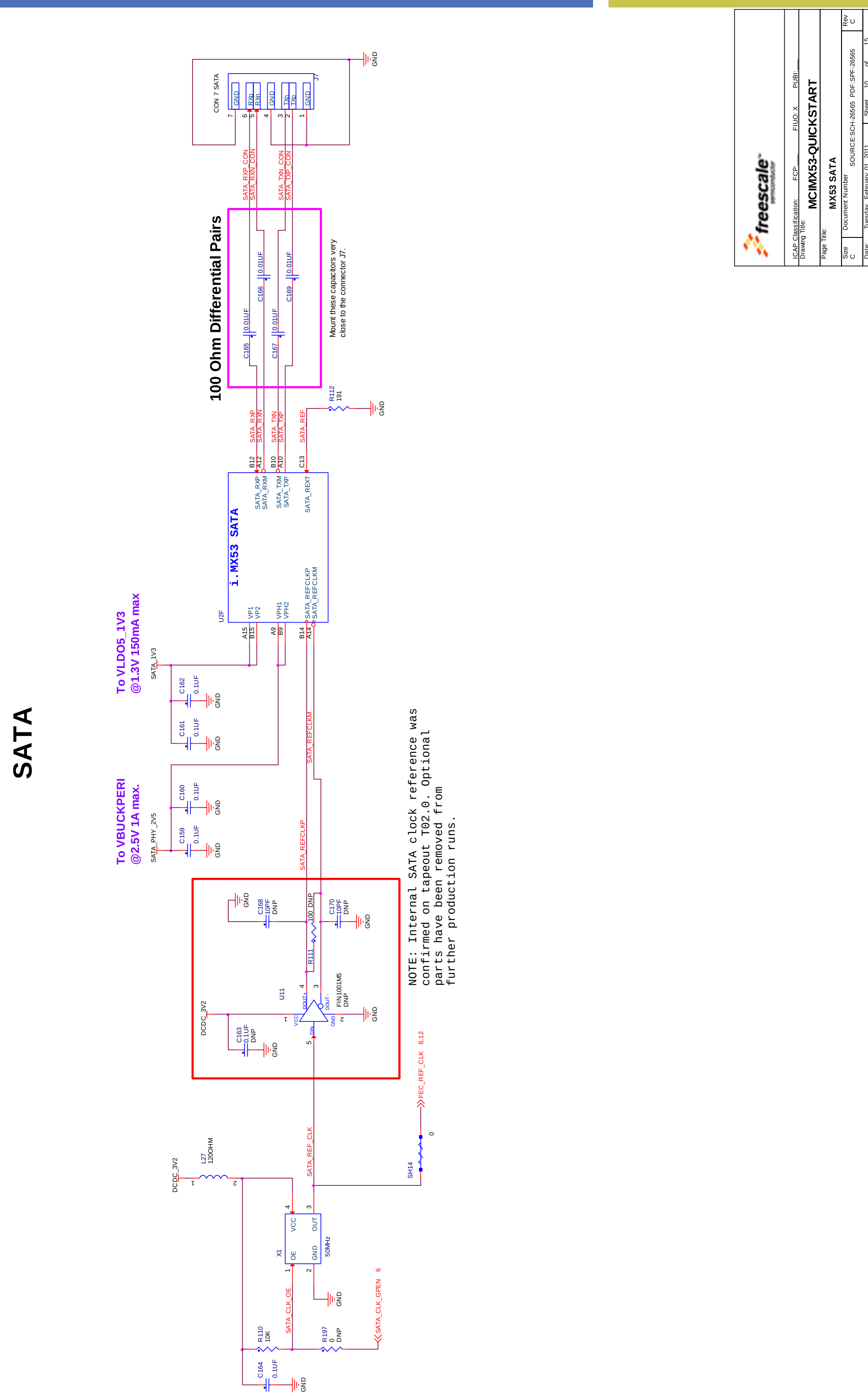


Figure 51. MX53 SATA

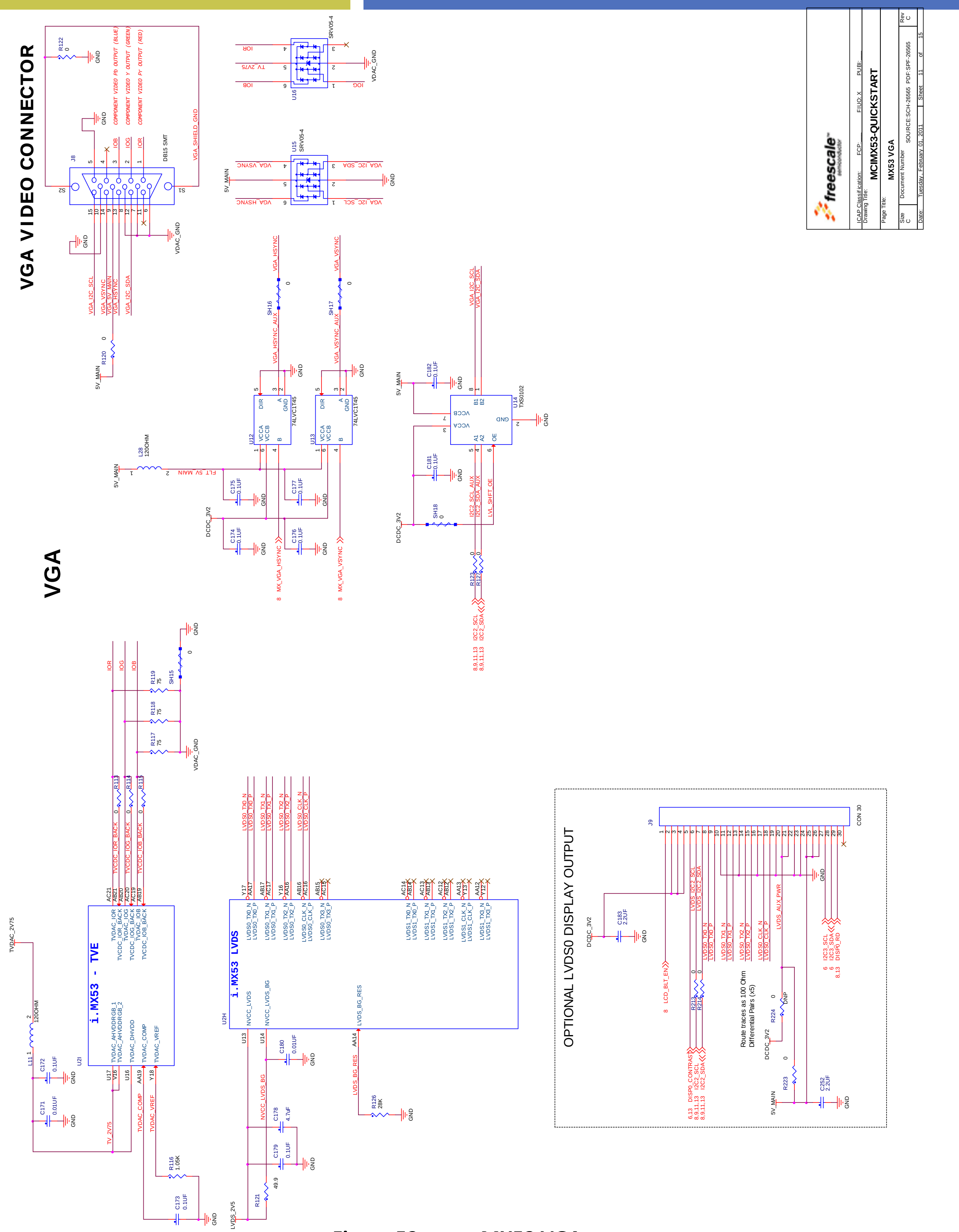


Figure 52. MX53 VGA

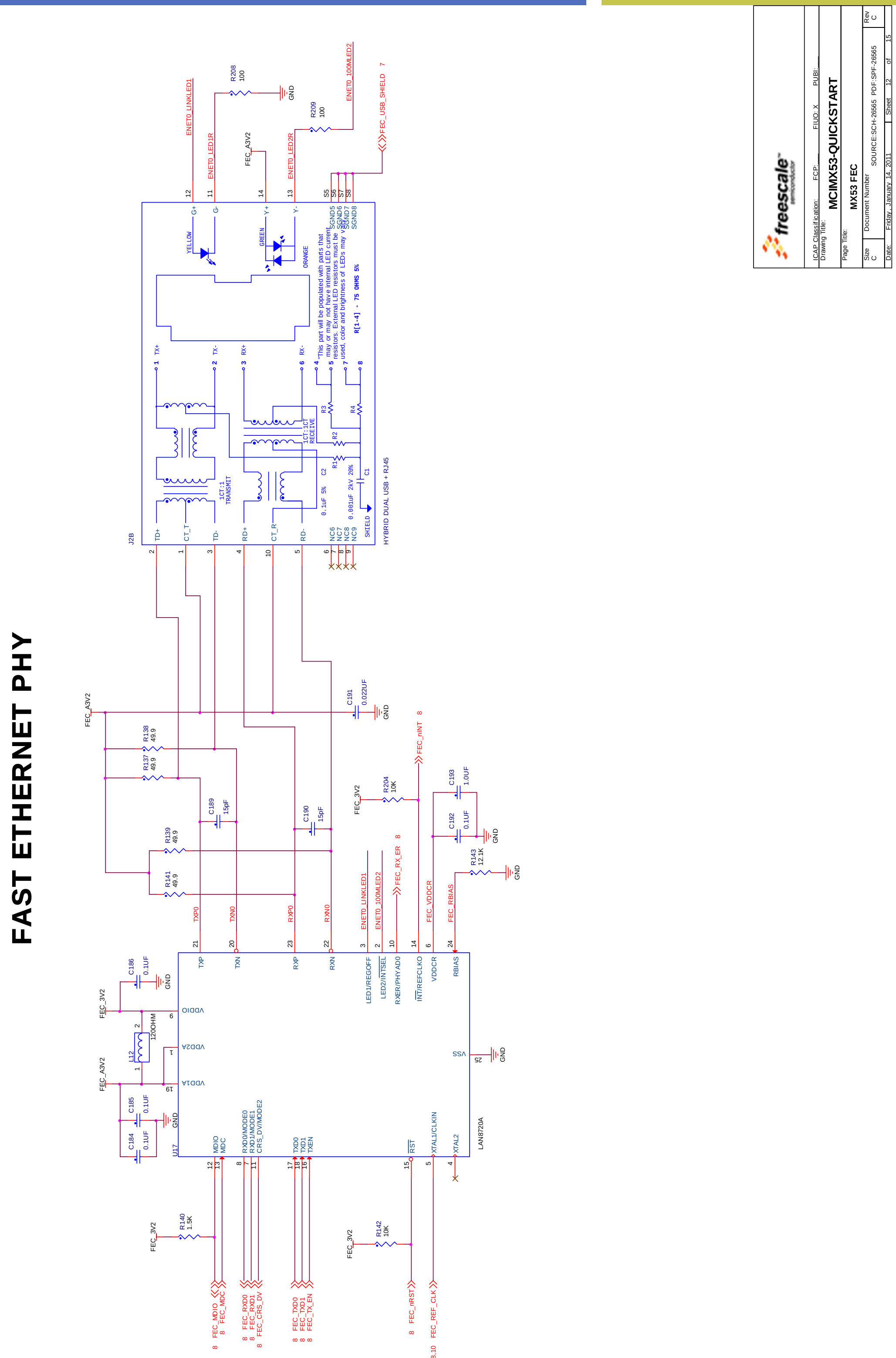


Figure 53. MX53 ETHERNET

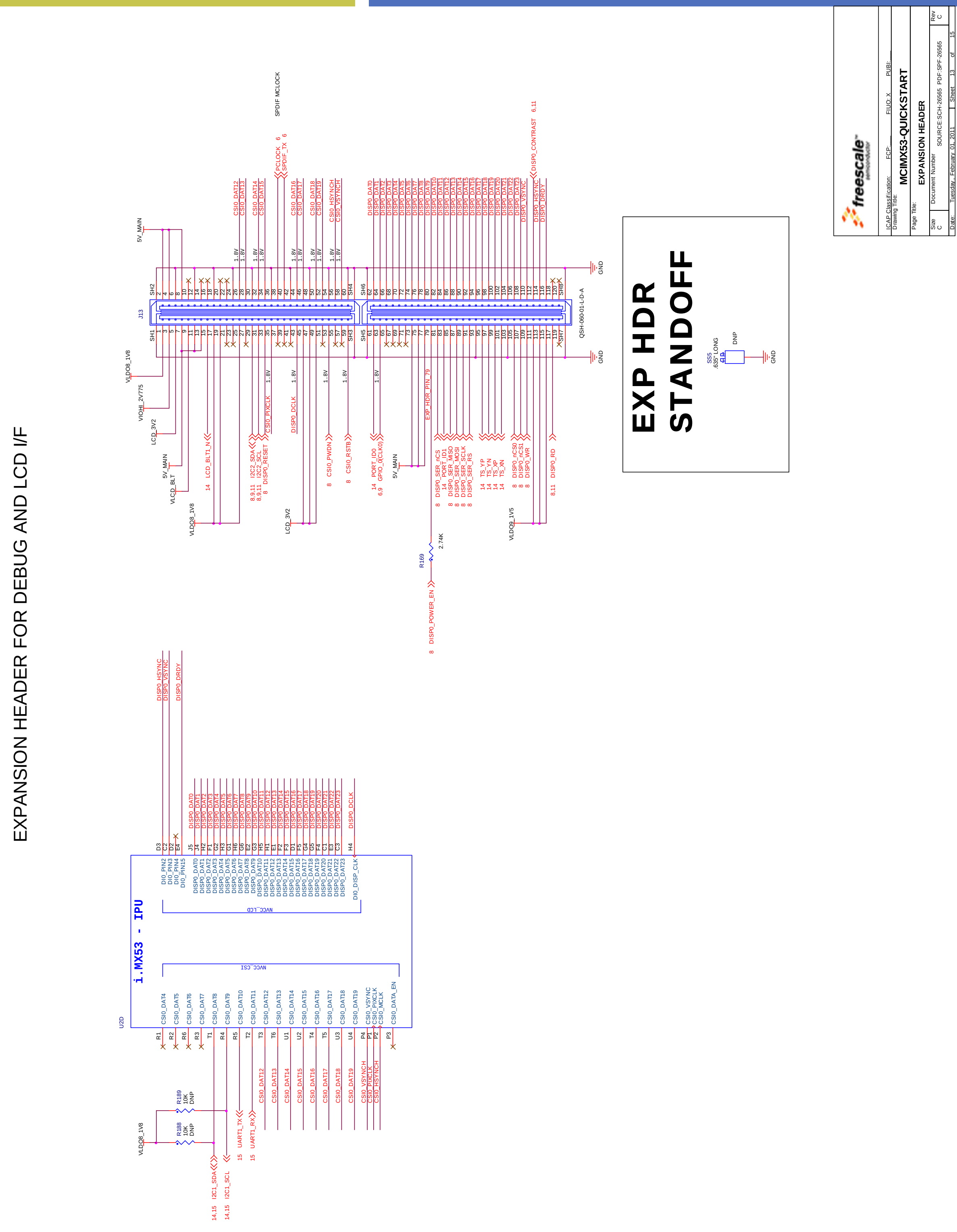


Figure 54. EXPANSION HEADER

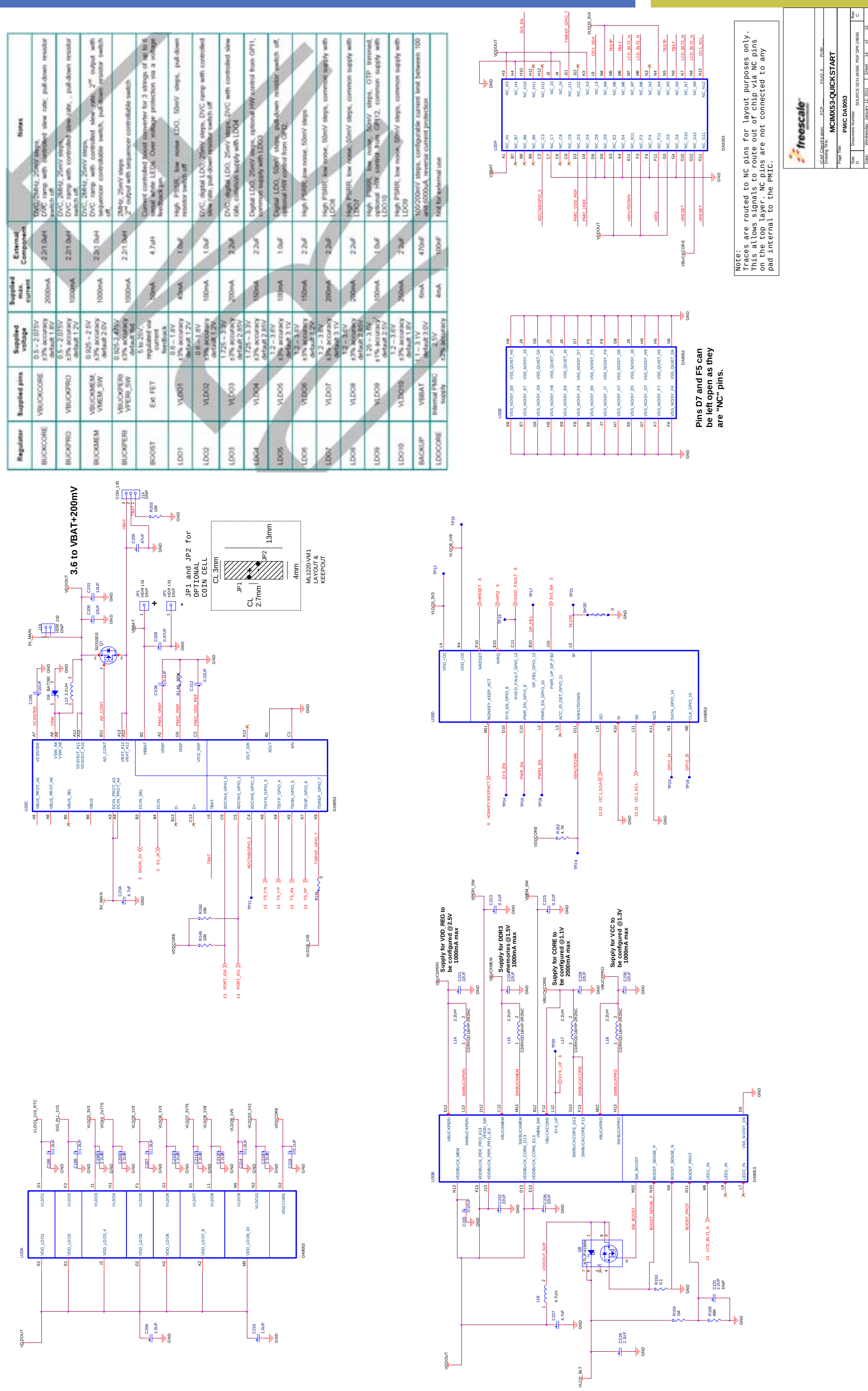


Figure 55. DA9053 PMIC

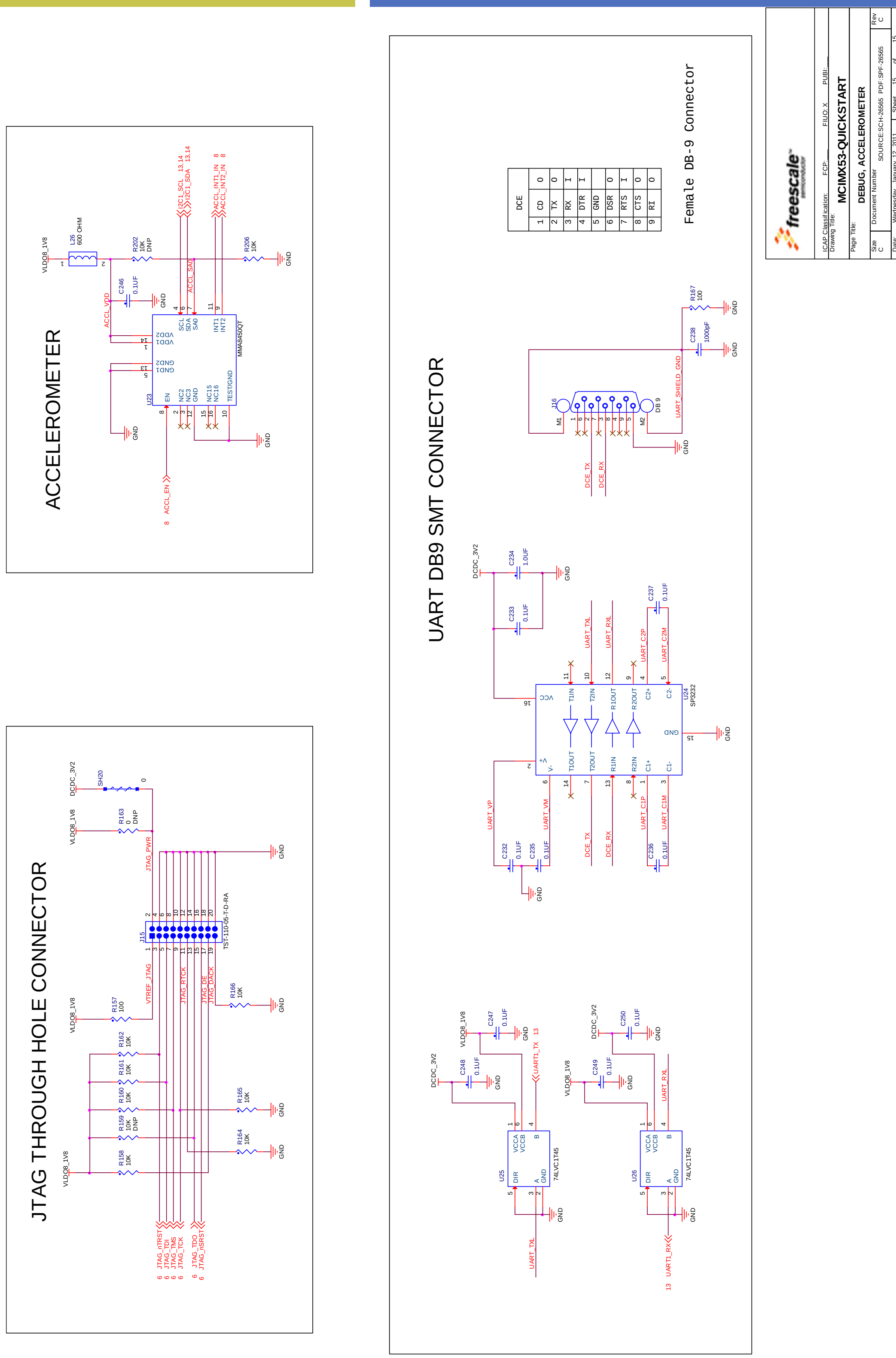


Figure 56. DEBUG, ACCELEROMETER

14. Bill of Materials

The Bill of Materials used to manufacture the Quick Start board is presented in this section. The capacitors and resistors used are considered generic type components and do not include manufacturer names or part numbers. The remainder of the parts have manufactures and part numbers provided for the primary part specified. Second source vendors are not included. The final section of the Bill of materials includes the list of parts not populated on the Quick Start board at the time of manufacture. Parts are listed in the following tables:

Generic Resistors		
Description	**QTY**	**Reference Designator**
RES MF ZERO OHM 1/20W 5% 0201	4	R123, R127, R213, R214
RES MF ZERO OHM 1/16W 5% 0402	12	R25, R30, R31, R32, R33, R113, R114, R115, R144, R145, R151, R223
RES MF ZERO OHM 1/10W -- 0603	3	R12, R19, R120
RES MF ZERO OHM 1/8W -- 0805	1	R122
RES MF 0.1 OHM 1/8W 1% 0402	2	R153, R201
RES MF 1.0 OHM 1/16W 1% 0402	4	R68, R69, R72, R73
RES MF 22 OHM 1/16W 5% 0402	2	R211, R212
RES 10 OHM 1/20W 5% 0201	1	R199
RES MF 33.0 OHM 1/20W 5% 0201	1	R104
RES MF 49.9 OHM 1/20W 1% 0201	5	R121, R137, R138, R139, R141
RES MF 75 OHM 1/20W 5% 0201	3	R117, R118, R119
RES TF 100 OHM 1/20W 5% RC0201	7	R66, R157, R167, R185, R186, R208, R209
RES MF 191 OHM 1/16W 1% 0402	1	R112
RES MF 200 OHM 1/16W 1% 0402	2	R28, R29

Table 32. Generic Resistors

Generic Resistors		
Description	**QTY**	**Reference Designator**
RES MF 240 OHM 1/16W 1% 0402	5	R190, R191, R192, R193, R194
RES MF 470 OHM 1/20W 1% 0201	6	R26, R27, R81, R177, R178, R187
RES MF 1.0K 1/20W 1% 0201	13	R49, R50, R173, R174, R175, R176, R179, R180, R181, R182, R183, R184, R198
RES MF 1.05K 1/16W 1% 0402	1	R116
RES MF 1.5K 1/20W 5% 0201	1	R140
RES MF 2.2K 1/20W 5% 0201	1	R101
RES MF 2.74K 1/16W 1% 0402	1	R169
RES 3.3K 1/20W 5% RC0201 ROHS	2	R195, R196
RES MF 4.7K 1/20W 5% 0201	3	R85, R86, R200
RES MF 4.7K OHM 1/20W 1% 0201	20	R37, R40, R46, R47, R53, R54, R55, R56, R57, R58, R59, R60, R61, R62, R63, R64, R65, R152, R221, R222
RES MF 6.04K 1/16W 1% 0402	2	R70, R71
RES MF 10K 1/20W 5% 0201	33	R10, R34, R35, R39, R41, R44, R76, R82, R87, R88, R89, R110, R142, R149, R150, R158, R160, R161, R162, R164, R165, R166, R168, R170, R171, R203, R204, R206, R216, R217, R218, R219, R220
RES MF 10.0K 1/20W 1% 0201	2	R51, R52
RES MF 12.1K 1/16W 1% 0402	1	R143
RES MF 28K 1/16W 1% 0402	1	R126
RES MF 47K 1/20W 5% 0201	1	R13
RES MF 68K 1/20W 1% 0201	1	R155
RES MF 100K 1/20W 1% 0201	3	R7, R9, R215
RES MF 200K 1/16W 1% 0402	1	R148
RES MF 432K 1/16W 1% 0402	1	R8
RES MF 1.0M 1/20W 5% 0201	1	R154

Table 32. Generic Resistors (con.)

Generic Capacitors		
Description	**QTY**	**Reference Designator**
CAP CER 10PF 25V 5% C0G 0201	1	C5
CAP CER 12PF 25V 5% C0G 0201	2	C217, C219
CAP CER 15PF 25V 5% C0G 0201	2	C189, C190
CAP CER 18PF 25V 5% C0G 0201	2	C133, C134
CAP CER 1000PF 16V 10% X7R 0201	1	C238
CAP CER 1000PF 2KV 10% X7R 1210	1	C135
CAP CER 0.01UF 10V 10% X5R 0201	22	C48, C49, C50, C80, C82, C84, C93, C95, C97, C100, C102, C104, C107, C109, C111, C141, C165, C166, C167, C169, C171, C180
CAP CER 0.022UF 10V 10% X5R 0201	1	C191
CAP CER 0.1UF 6.3V 10% X5R 0201	104	C8, C44, C46, C47, C52, C53, C54, C55, C56, C57, C58, C59, C60, C61, C62, C63, C66, C67, C68, C69, C70, C72, C73, C74, C75, C76, C77, C78, C79, C81, C83, C86, C87, C88, C89, C90, C92, C94, C96, C99, C101, C103, C106, C108, C110, C113, C114, C115, C116, C117, C119, C120, C121, C122, C123, C125, C126, C127, C128, C129, C131, C132, C136, C138, C139, C142, C143, C145, C147, C148, C150, C152, C153, C159, C160, C161, C162, C164, C172, C174, C175, C176, C177, C179, C181, C182, C184, C185, C186, C192, C208, C218, C223, C225, C232, C233, C235, C236, C237, C246, C247, C248, C249, C250
CAP CER 0.1UF 16V 10% X7R 0402	1	C173
CAP CER 0.1UF 35V 10% X5R 0402	1	C245
CAP CER 0.22UF 6.3V 20% X5R 0201	31	C9, C10, C11, C12, C13, C14, C16, C17, C18, C19, C21, C22, C23, C24, C25, C26, C27, C29, C30, C31, C32, C33, C34, C35, C37, C38, C39, C42, C43, C64, C212
CAP CER 0.47UF 6.3V 10% X5R 0402	1	C209
CAP CER 1.0UF 35V 10% X5R 0603	1	C244
CAP CER 1.0UF 10V 10% X5R 0402	12	C3, C151, C193, C196, C199, C206, C207, C214, C215, C234, C239, C240
CAP CER 2.2UF 6.3V 20% X5R 0402	11	C137, C140, C183, C194, C203, C210, C211, C213, C216, C252, C253
CAP CER 2.2UF 25V 10% X5R 0805	1	C229
CAP CER 4.7UF 6.3V 20% X5R 0402	4	C149, C178, C204, C227
CAP CER 10UF 6.3V 20% X5R 0603	17	C7, C28, C40, C85, C91, C98, C105, C112, C118, C124, C130, C144, C146, C195, C200, C201, C220
CAP CER 10UF 10V 10% X5R 0805	2	C2, C4
CAP CER 22UF 6.3V 20% X5R 0805	12	C15, C41, C45, C51, C65, C71, C221, C222, C224, C226, C228, C230
CAP CER 47uF 6.3V 20% X5R 0805	3	C20, C36, C205
CAP CER 100UF 6.3V 20% X5R 1206	4	C1, C241, C242, C243

Table 33. Generic Capacitors

SPECIFIED COMPONENTS				
Description	**QTY**	**Reference Designator**	**Manufacturer**	**Part Number**
CAP TANT 220UF ESR=0.800 OHM 4V 20% -- 3216-10	2	C154,C157	NICHICON	F950G227MSAAQ2
IND FER BEAD 120OHM@100MHZ 2A 25% 0603	3	L7,L9,L19	MURATA	BLM18PG121SH1
IND FER BEAD 120 OHM@100MHZ 500MA 25% 0603	2	L10,L12	MURATA	BLM18AG121SN1J
IND PWR 4.7UH@100KHZ 1.1A 20% SMT	1	L1	TDK	VLF4012AT-4R7M1R1
IND PWR 2.2UH@100KHZ 1.6A 30% SMD	4	L14,L15,L17,L18	SUMIDA ELECTRIC	CDRH2D18/HP-2R2NC
IND CHK 90 OHM@100MHZ 330MA 25% 0805	2	L5,L6	MURATA	DLW21HN900SQ2L
IND FER 120OHM@100MHZ 300MA 25% 0402	6	L2,L4,L8,L11,L27,L28	MURATA	BLM15HB121SN1D
IND FER BEAD 600 OHM@100MHZ 300MA 25% 0402	1	L26	MURATA	BLM15HD601SN1D
IND FER BEAD 220OHM@100MHZ 700MA 25% 0402	5	L20,L21,L23,L24,L25	MURATA	BLM15EG221SN1_
IND PWR 2.2UH@1MHZ 1.5A 20% SMD	1	L13	TDK	VLS3012T-2R2M1R5
IND PWR 4.7UH@1MHZ 1A 20% SMD	1	L16	TDK	VLS3012T-4R7M1R0
CON 1 PWR PLUG DIAM 2.0MM RA TH -- 430H NI	1	J1	CUI STACK	PJ-202A
CON 5 AUD JACK 3.2MM SKT RA TH -- 197H SN 079L	2	J6,J18	CUI STACK	SJ-43515TS
HDR 2X10 RA SHRD TH 100MIL CTR 365H SN 230L	1	J15	SAMTEC	TST-110-05-T-D-RA
CON 1X7 PLUG SATA TH 50MIL SP 331H -- 96L	1	J7	3M	5607-5102-SH
CON 2X60 SKT SMT 0.5MM SP AU	1	J13	SAMTEC	QSH-060-01-L-D-A
CON 19 CRD SKT SMT -- 150H AU	1	J5	PROCONN TECHNOLOGY	SDC013-A0-501F
CON 30 SHRD SKT RA SMT 1MM SP AU	1	J9	HIROSE	DF19G-30P-1H(56)

Table 34. Specified Components

SPECIFIED COMPONENTS				
Description	**QTY**	**Reference Designator**	**Manufacturer**	**Part Number**
CON 5 MICRO USB B RA SHLD SKT 0.65MM SP SMT AU	1	J3	MOLEX	47346-0001
CON 9 DB 0.118 SKT RA SMT 55MIL SP 494H AU	1	J16	NORCOMP	190-009-263R001
CON 12 SKT SD/MMC RA SMT 43MIL SP 78H AU	1	J4	3M	29-08-05WB-MG
CON 15 DB RA SKT SMT 0.76MM SP 425H SN	1	J8	NORCOMP	200-015-263R001
OSC 50MHZ PROG 3.3V	1	X1	FOX ELECTRONICS	FXO-HC736R-50
XTAL 32.768KHZ RSN -- SMT	1	QZ1	MICRO CRYSTAL	CC7V-T1A 32.768KHZ 9PF+/-30PPM
XTAL 24MHZ -- 3.2X2.5MM SMT	1	Y1	SIWARD INTERNATIONAL	XTL571300LLI24.000-10TR
IC BUF TS 0.9-3.6V	1	U22	FAIRCHILD	NC7SP125P5X
IC TRANS 1.65V-5.5V SINGLE SOT23-6	4	U12,U13,U25,U26	TEXAS INSTRUMENTS	SN74LVC1T45DBVR
IC XCVR RS232 120KBPS 3.0-5.5V SSOP16	1	U24	SIPEX	SP3232ECA-L
IC VREG LDO ADJ 0.6-5.3V 1A 2.5-5.5V WDFN-6L	1	U1	RICHTEK	RT8010PQW
IC XCVR ETHERNET 1.6-3.6V QFN24	1	U17	SMSC	LAN8720A-CP-TR
IC AUDIO CODEC STEREO 8-27MHZ 1.8-3.3V QFN32	1	U9	FREESCALE SEMI	SGTL5000XNAA3R2
IC VXLTR 2BIT 1.65-3.6V/2.3-5.5V SOT70-8	1	U14	TEXAS INSTRUMENTS	TXS0102DCUR
IC FIFO 12BIT 1.71-1.89V QFN16	1	U23	FREESCALE SEMI	MMA8450QT
IC LIN PMIC WITH USB PWR MANAGER 5.5V VFBGA169	1	U20	Dialog Semiconductor	DA9053
IC MPU ARM COREA8 1GHZ -- TEPBGA529	1	U2	FREESCALE SEMI	IMX53
IC MEM DDR3 SDRAM 2Gb 128MX16 1.5V FBGA96	4	U3,U4,U5,U6	MICRON	MT41J128M16HA-15E:D

Table 34. Specified Components (con.)

SPECIFIED COMPONENTS				
Description	**QTY**	**Reference Designator**	**Manufacturer**	**Part Number**
LED ULTRA-BRIGHT GREEN SMT 0603	3	D1,D9,D16	LITE ON	LTST-C190KGKT
LED BLUE -- 20MA SMT	4	D10,D11,D12,D13	LITE ON	LTST-C190TBKT
LED ULTRA BRIGHT RED SGL 30MA 0603	1	D14	LITE ON	LTST-C190KRKT
TRAN NMOS 60V 115MA SOT23	1	Q15	ON SEMI	2N7002LT1G
DIODE TVS ARRAY 12A 5V 300W SOT23_S6	2	U15,U16	SEMTECH CORP	SRV05-4.TCT
DIODE SCH 1A 20V SOD323	2	D8,D15	PHILIPS SEMI	BAT760
TRAN NMOS DUAL 200MA 50V SOT363	4	Q9,Q10,Q11,Q12	DIODES INC	BSS138DW-7-F
TRAN PMOS PWR 12V 4.3A SOT23	2	Q1,Q14	INTERNATIONAL RECTIFIER	IRLML6401TRPBF
DIODE TVS ESD PROT ULT LOW CAP 5-5.4V SOD-923	1	D4	ON SEMI	ESD9L5.0ST5G
TRAN NMOS PWR 4.6A 30V DIODE SCHOTTKY 2.0A WDFN6	1	Q8	ON SEMI	NTLJF4156NT1G
TRAN PMOS PWR 4.1A 12V SOT-23	1	Q7	VISHAY INT	SI2333DS-T1-E3
DIODE TVS 2-CH ARRAY 25A 5V 500W SOT-143	2	D17,D18	SEMTECH CORP	SR05.TCT
FUSE PLYSW 1.1A HOLD 6V SMT ROHS	1	F2	TYCO ELECTRONICS	MICROSMD110F-2
FUSE CBKR 3A 24V 0603	1	F1	BOURNS	SF-0603F300-2
SW SPST PB 50MA 12V SMT	4	SW2,SW3,SW4,SW5	E SWITCH	TL1015AF160QG
CON 22 RJ-45/DUAL USB RA TH 50MIL SP 1231H AU 90L	1	J2	PREMIER MAGNETICS	RJ45-103YDD2

Table 34. Specified Components (con.)

NON-POPULATED COMPONENTS				
Description	**QTY**	**Reference Designator**	**Manufacturer**	**Part Number**
CAP CER 10PF 25V 5% C0G 0201	0	C168, C170		
CAP CER 0.1UF 6.3V 10% X5R 0201	0	C163		
CAP CER 2.2UF 50V 10% X7R 1206	0	C231		
IND FER 120OHM@100MHZ 300MA 25% 0402	0	L3	MURATA	BLM15HB121SN1D
IND FER BEAD 220OHM@100MHZ 700MA 25% 0402	0	L22	MURATA	BLM15EG221SN1_
CON 1X3 PLUG SHRD TH 1.25MM 165H SN	0	J14	MOLEX	0530470310
HDR 1X2 TH 100MIL SP 165H AU	0	J19	SAMTEC	TLW-102-06-G-S
HDR 1X1 TH -- 330H SN 115L	0	JP1, JP2	SAMTEC	TSW-101-23-T-S
IC DRV LVDS 1-BIT HIGH SPEED DIFF 3.3V SOT23-5	0	U11	FAIRCHILD	FIN1001M5
MOSFET,DUAL N & P CHANNEL, SOT6 ROHS	0	Q13	FAIRCHILD	FDC6321C_NL
RES MF ZERO OHM 1/20W 5% 0201	0	R36, R38, R48, R197		
RES MF ZERO OHM 1/16W 5% 0402	0	R210, R224		
RES MF ZERO OHM 1/10W -- 0603	0	R80, R163		
RES MF 0.02OHM 1/4W 0.5% 0805	0	R17, R20		
RES MF 49.9 OHM 1/20W 1% 0201	0	R42, R43		
RES TF 100 OHM 1/20W 5% RC0201	0	R111		
RES MF 10K 1/20W 5% 0201	0	R84, R97, R108, R159, R188, R189, R202		
RES MF 200K 1/20W 5% 0201	0	R14		
RES MF 10M 1/20W 5% 0201	0	R45		
SW SPST DIP SMT 50V 100MA DIP10	0	SW1	Multicomp	MCNHDS-10-T

Table 35. Non-Populated Components

15. PCB information

This section provides the Gerber artwork in a picture format for easy reference when using this document. The actual Gerber files are available from the i.MX53 Quick Start web site. The Gerber file package consists of all artwork files and additional supplemental files. The 14 artwork files are shown in the following figures:

Figure 57. **Top Etch Layer**
Figure 58. **Second Etch Layer**
Figure 59. **Third Etch Layer**
Figure 60. **Fourth Etch Layer**
Figure 61. **Fifth Etch Layer**
Figure 62. **Sixth Etch Layer**
Figure 63. **Seventh Etch Layer**
Figure 64. **Bottom Etch Layer**
Figure 65. **Soldermask Top**
Figure 66. **Soldermask Bottom**
Figure 67. **Pastemask Top**
Figure 68. **Pastemask Bottom**
Figure 69. **Silkscreen Top**
Figure 70. **Silkscreen Bottom**

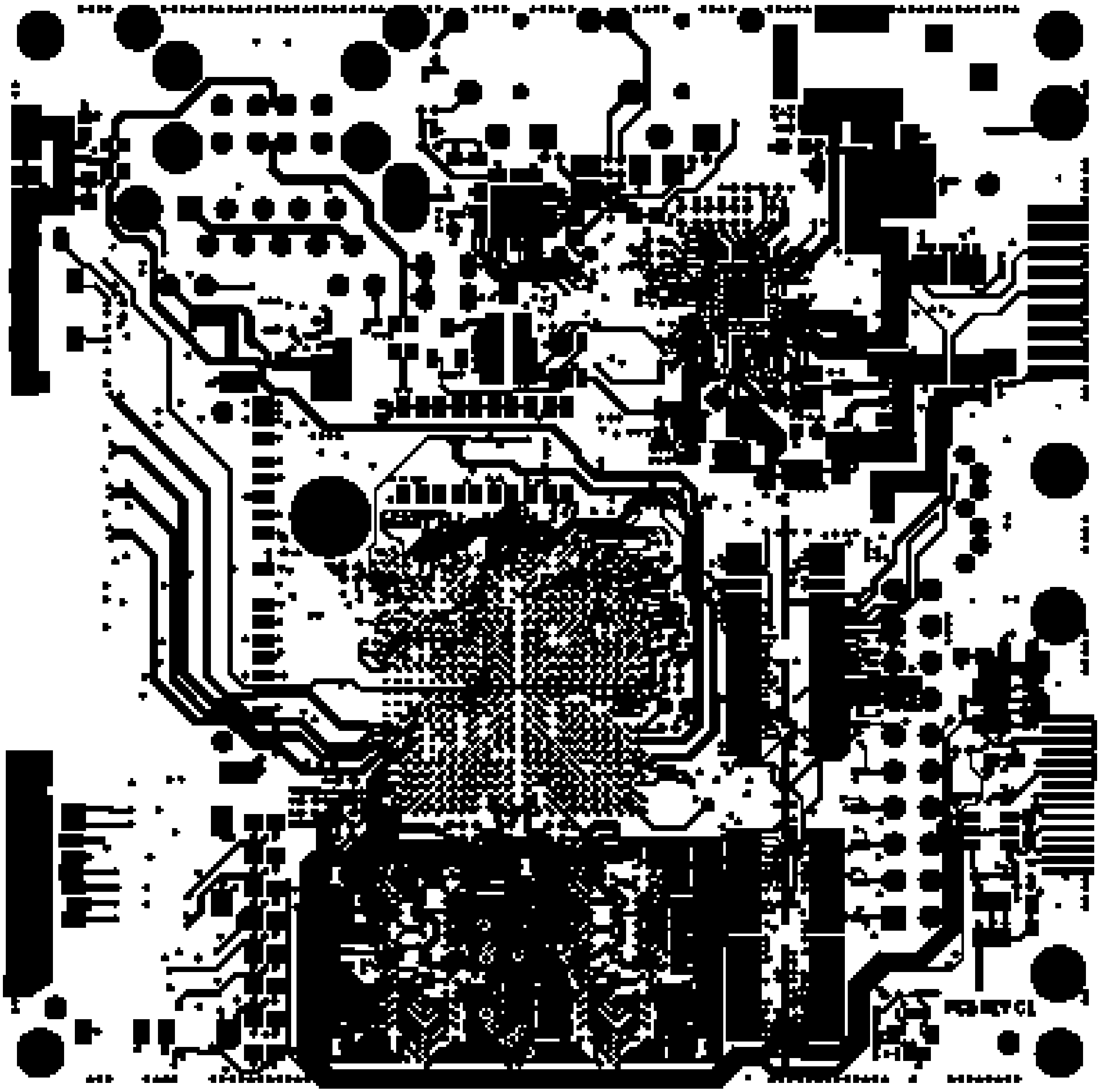


Figure 57. Top Etch Layer

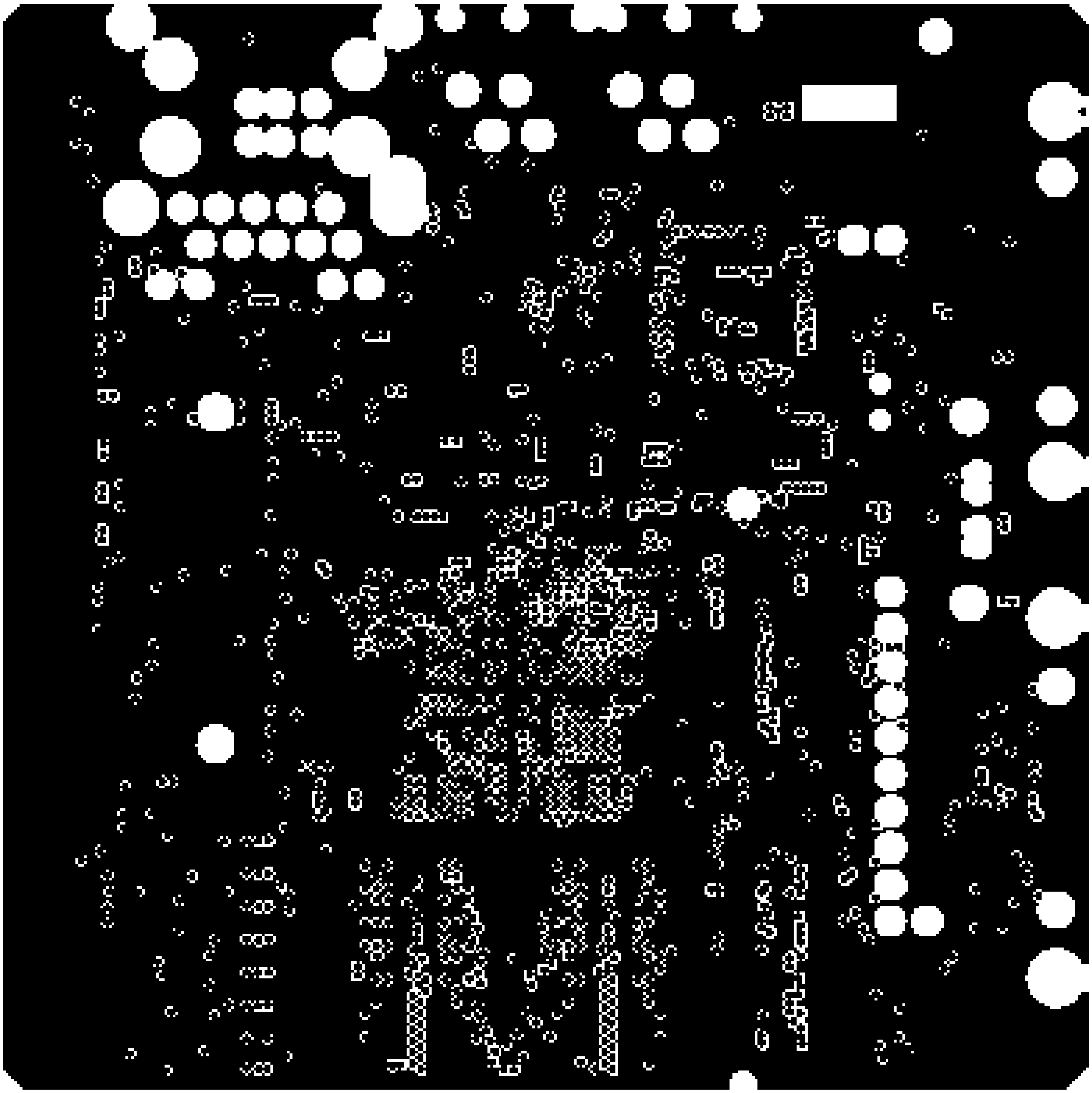


Figure 58. Second Etch Layer

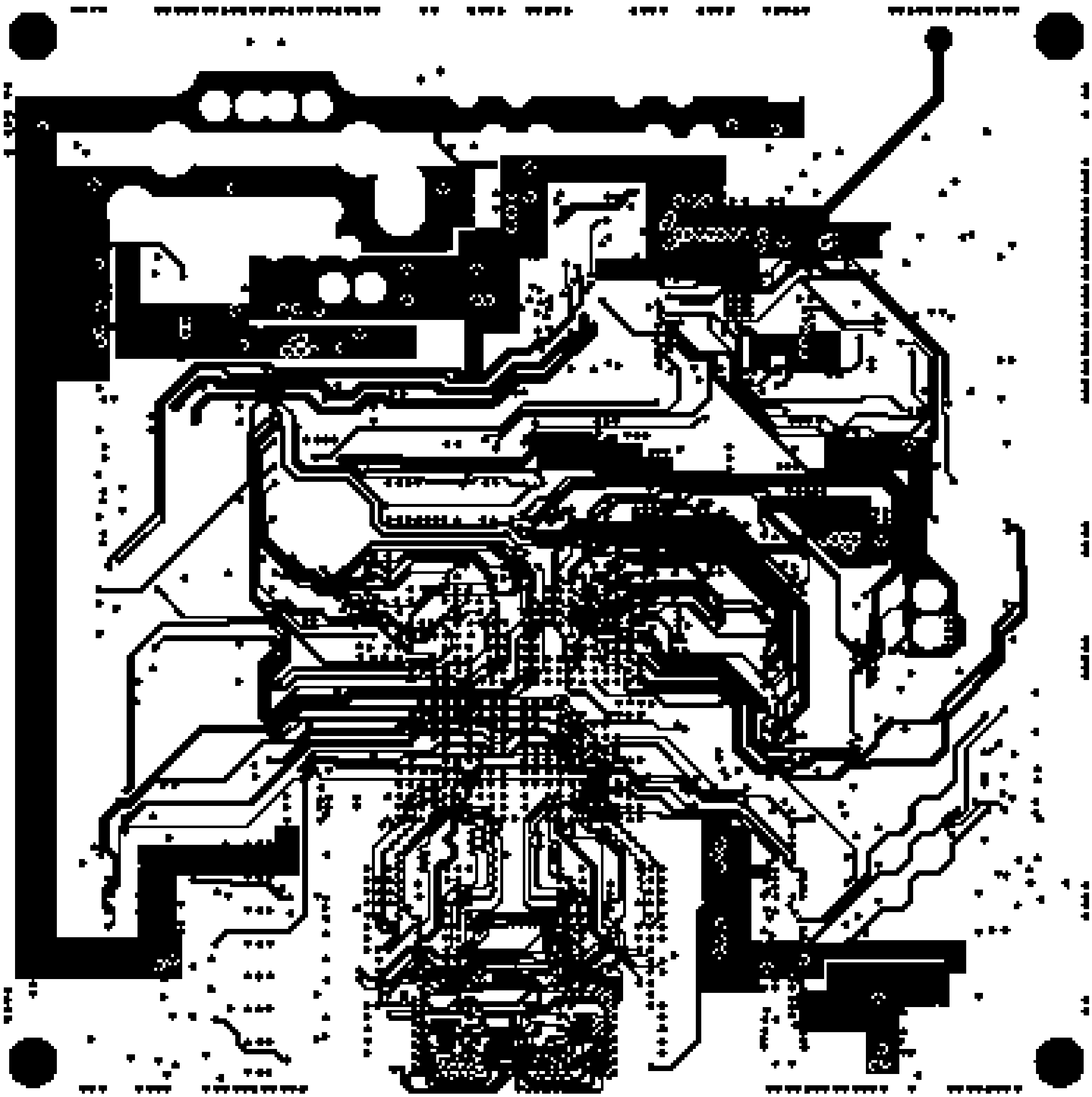


Figure 59. Third Etch Layer

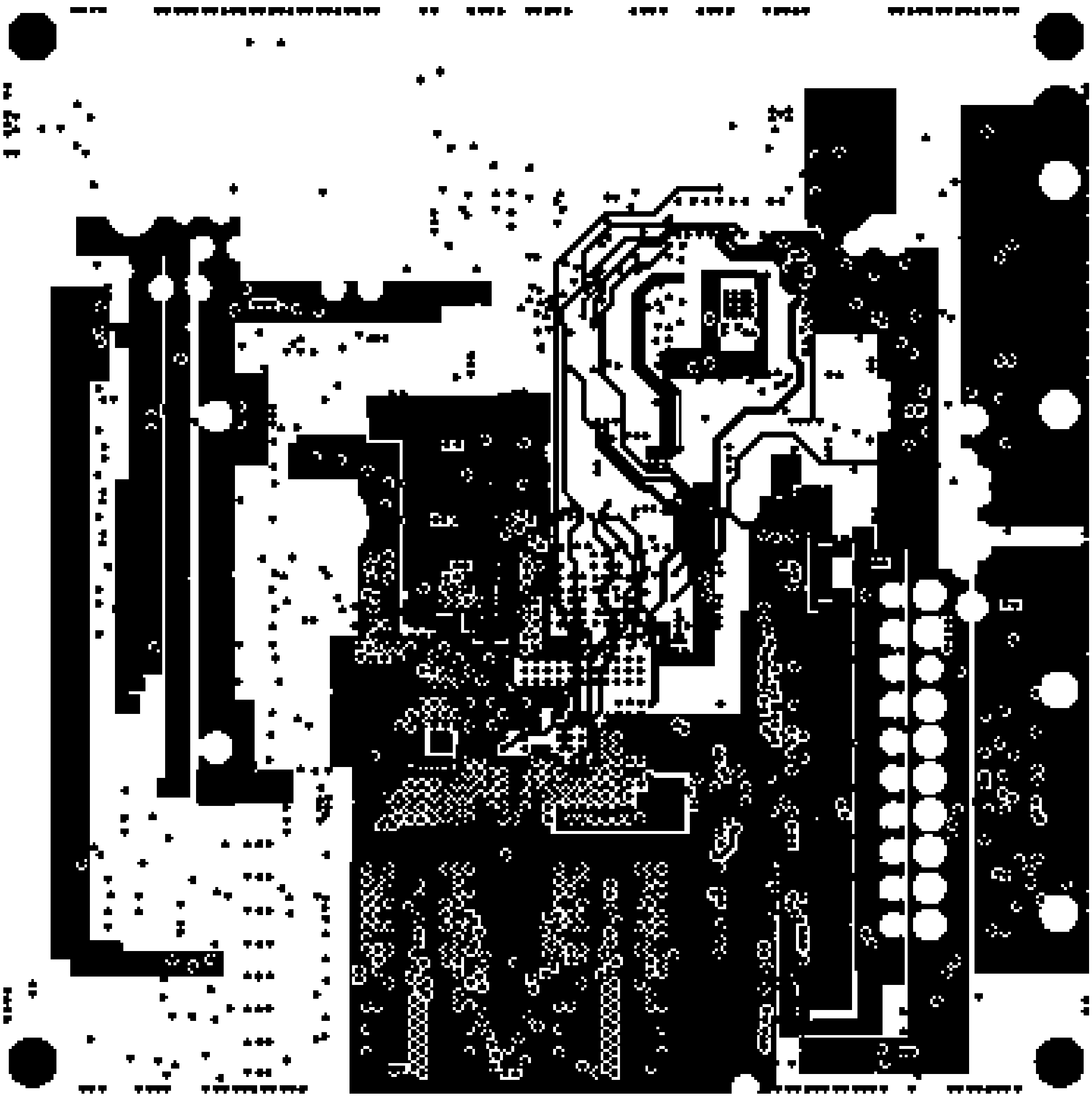


Figure 60. Fourth Etch Layer

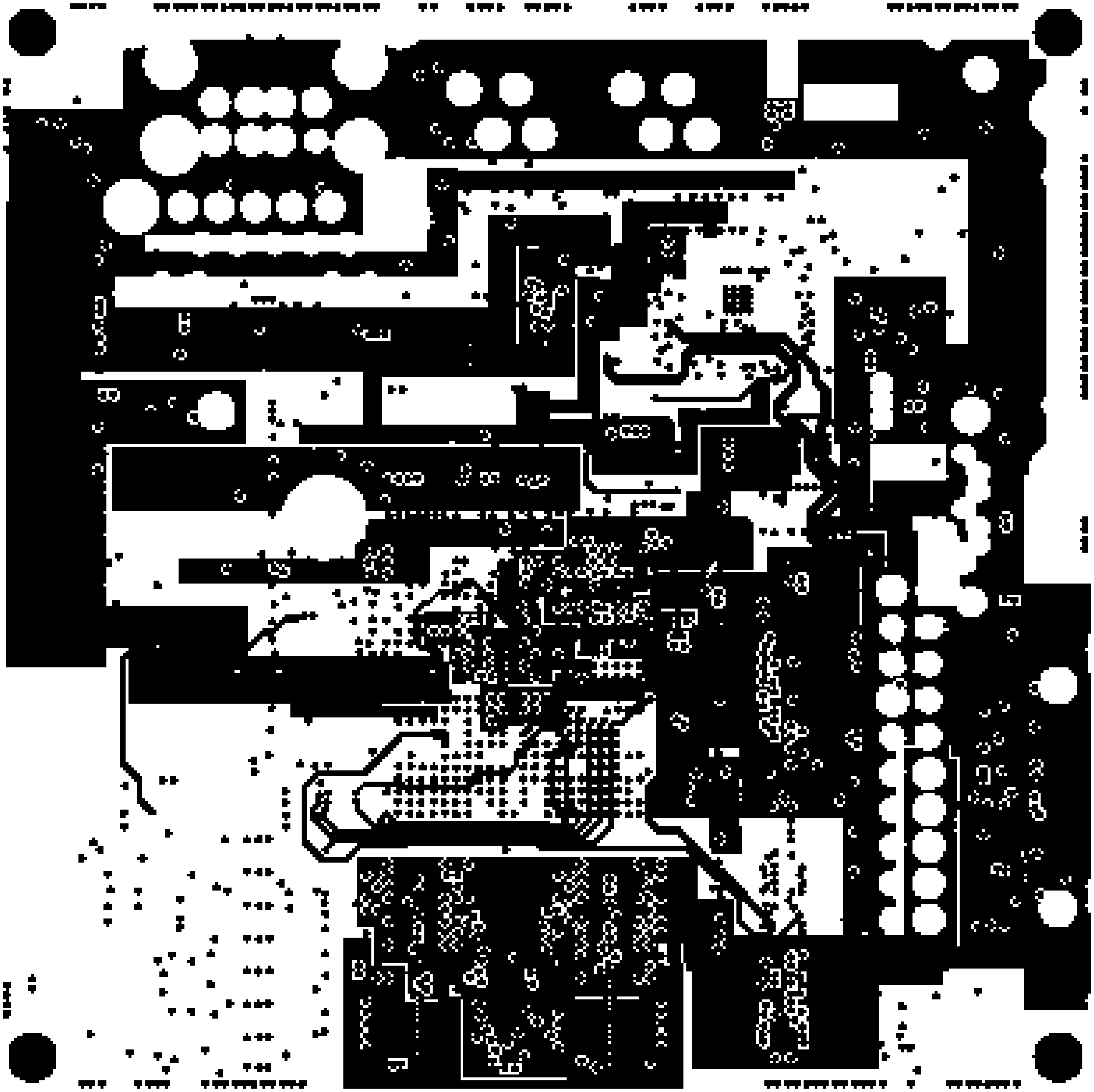


Figure 61. Fifth Etch Layer

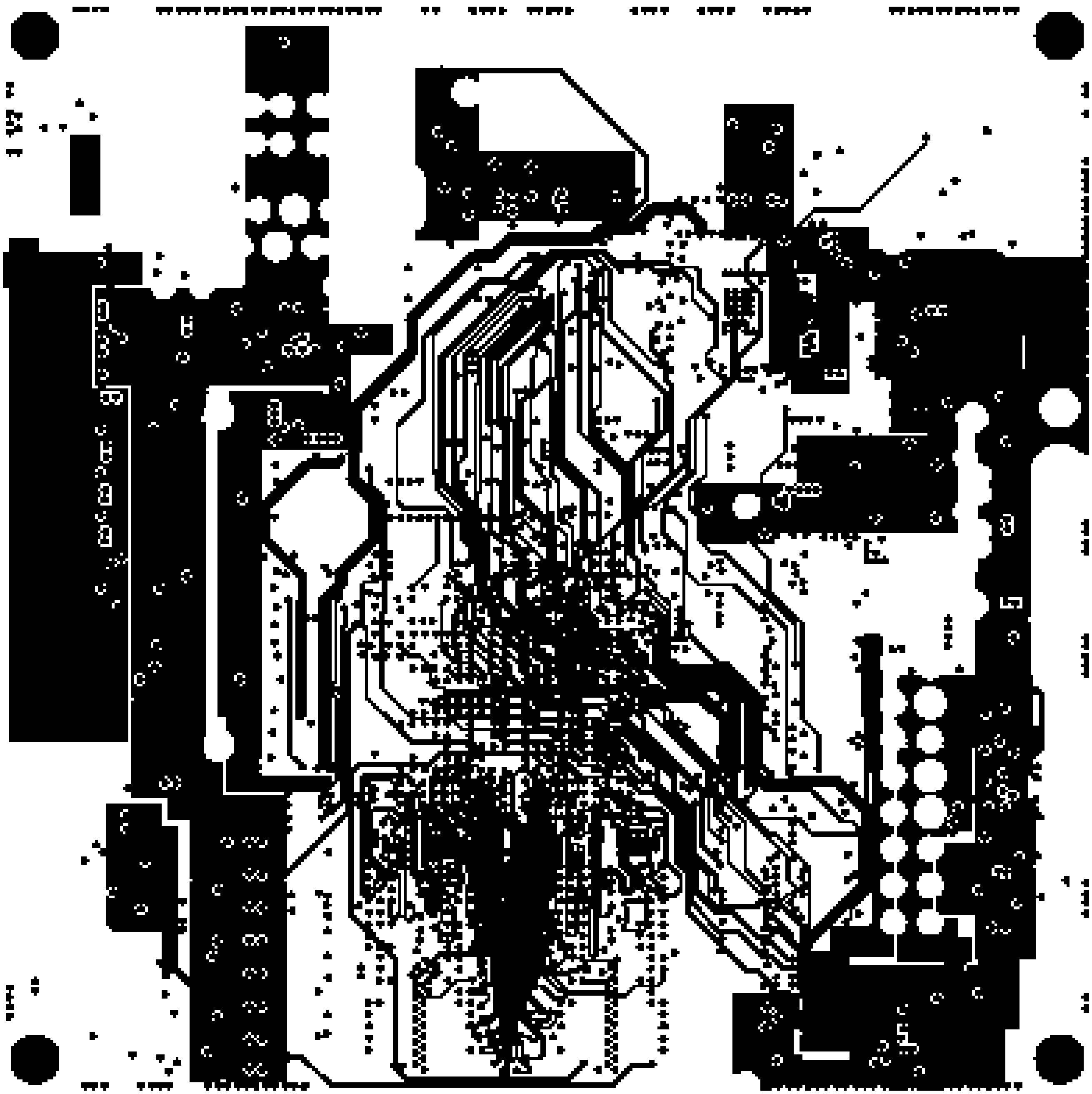


Figure 62. Sixth Etch Layer

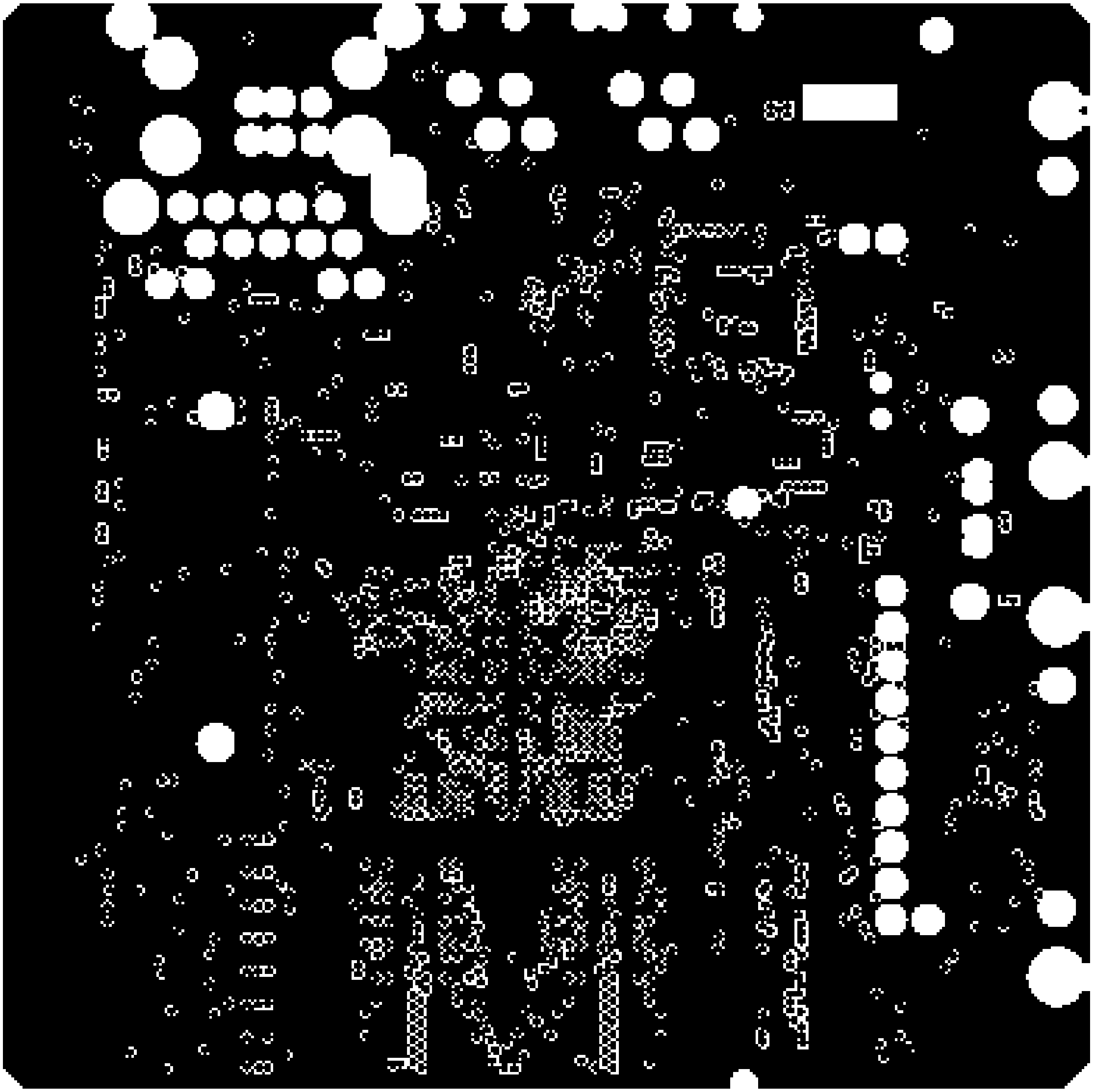


Figure 63. Seventh Etch Layer

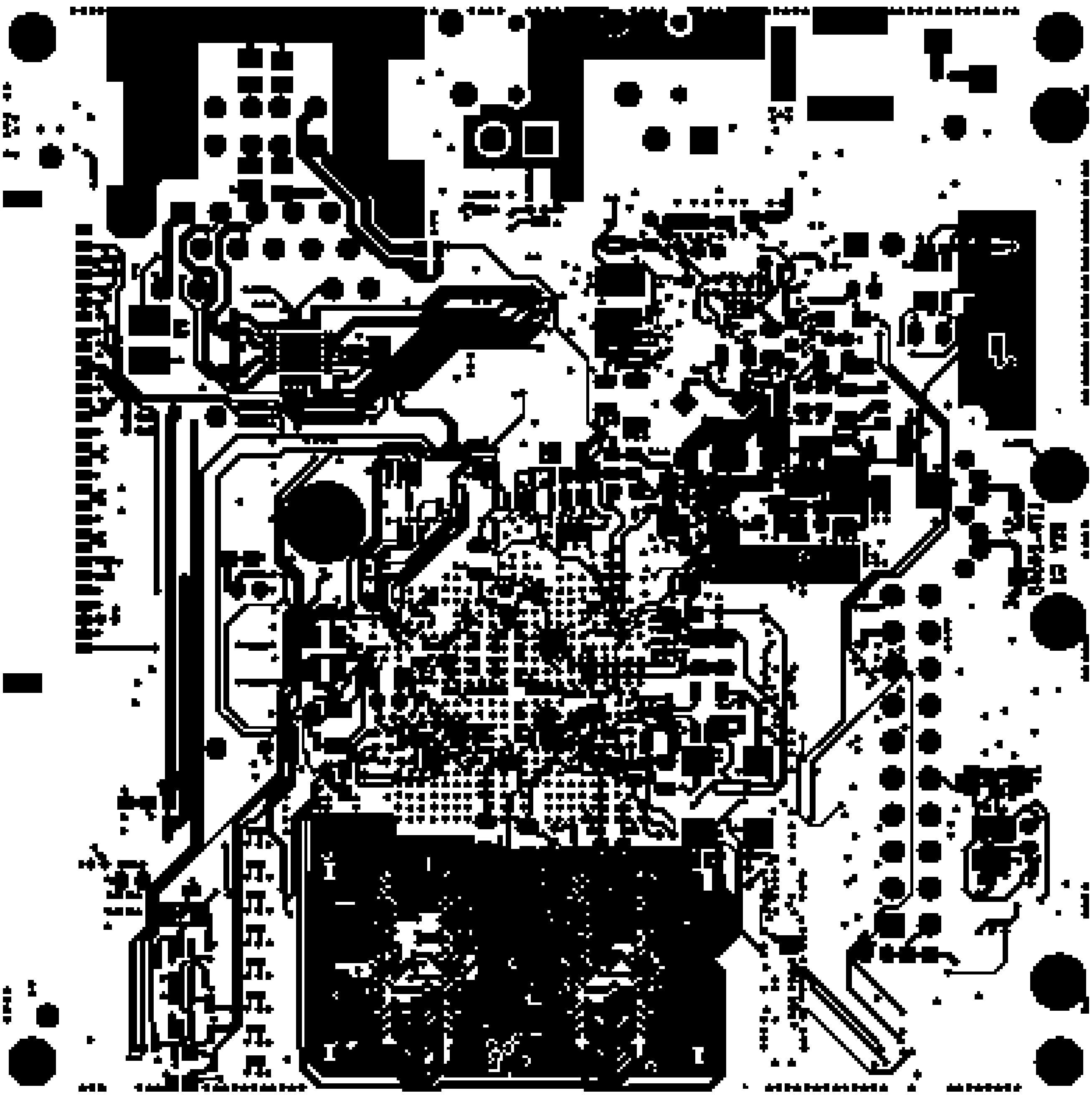


Figure 64. Bottom Etch Layer

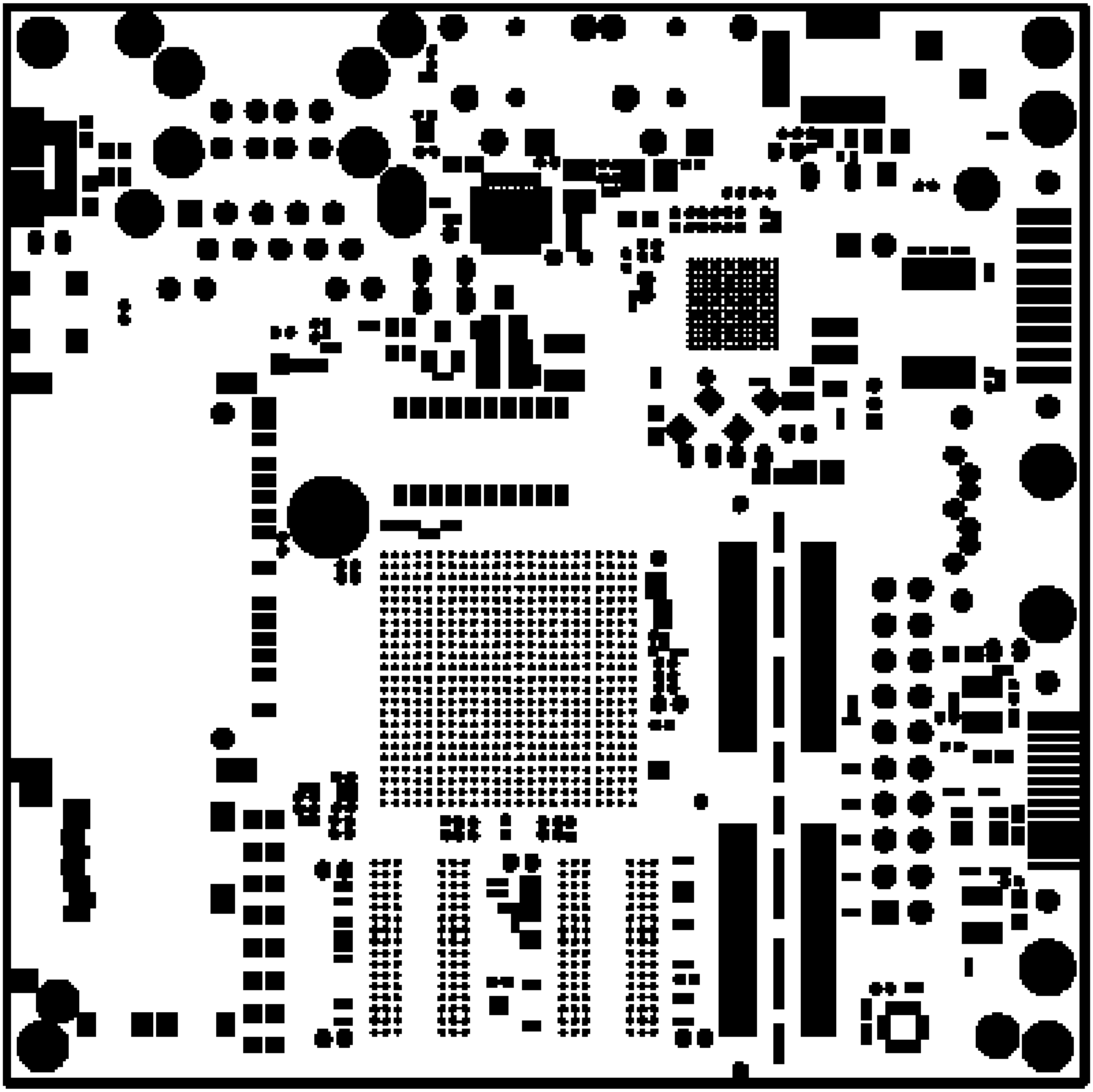


Figure 65. Soldermask Top

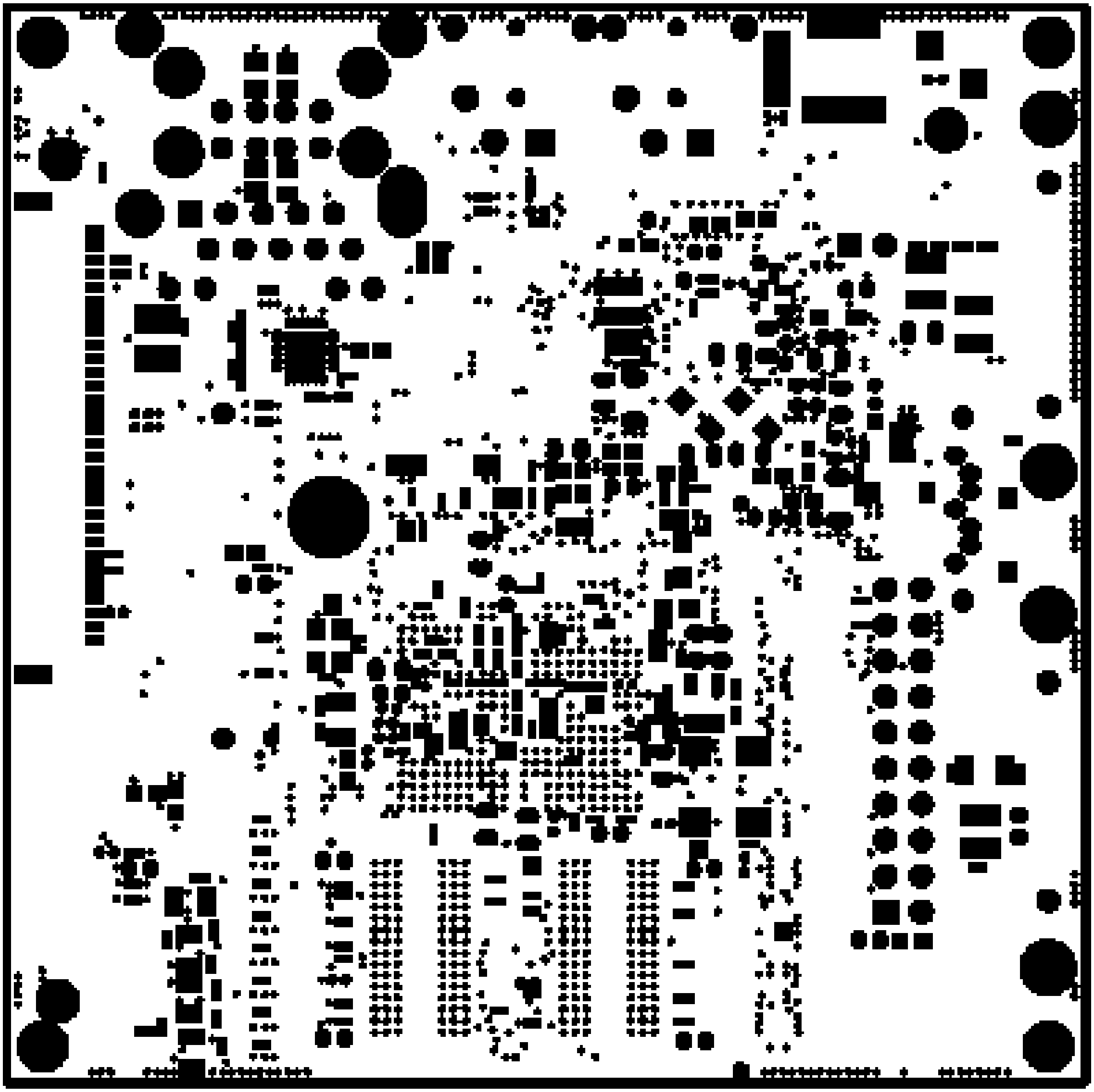


Figure 66. Soldermask Bottom

Figure 67. Pastemask Top

Figure 68. Pastemask Bottom

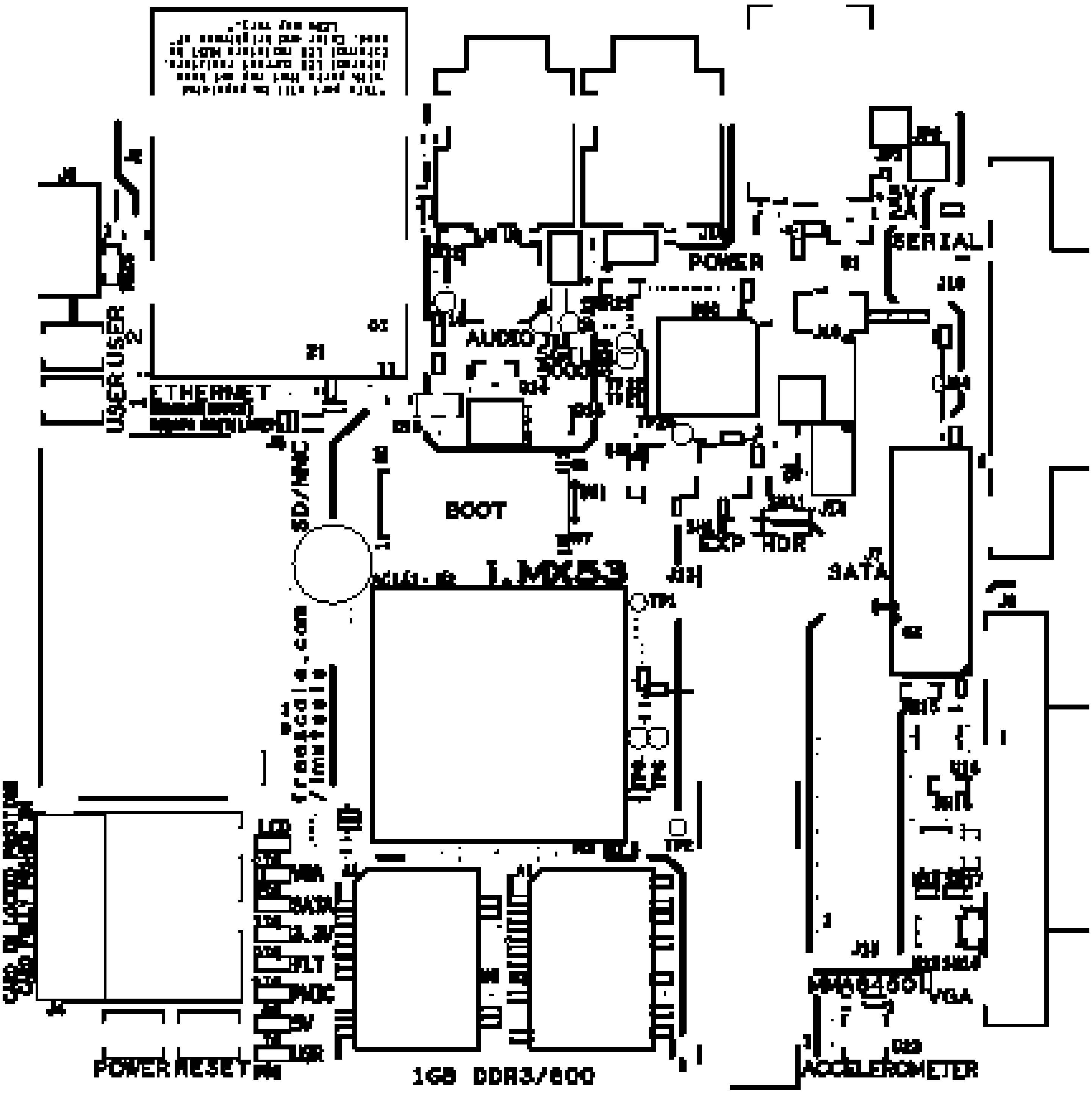


Figure 69. Silkscreen Top

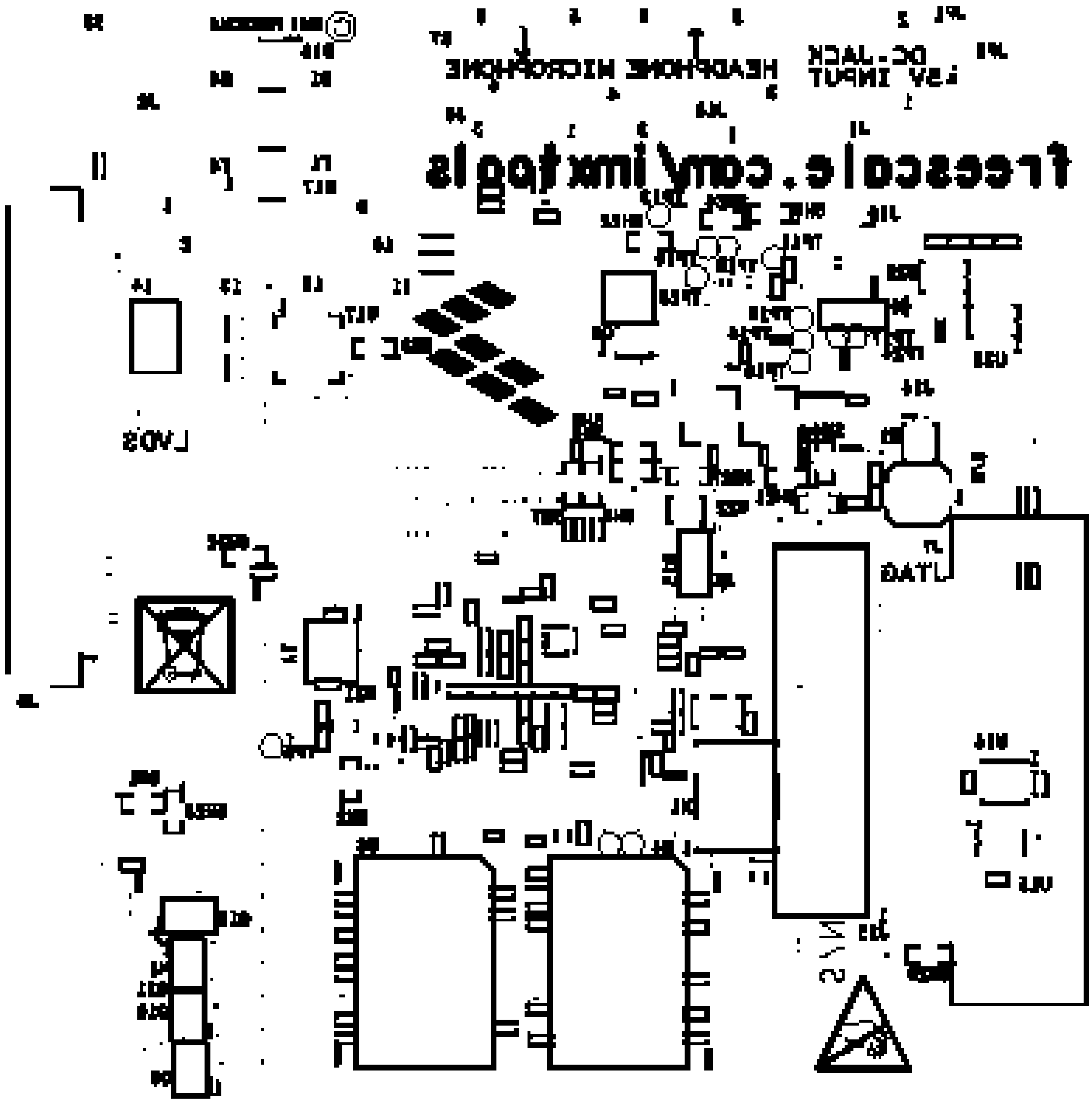


Figure 70. Silkscreen Bottom